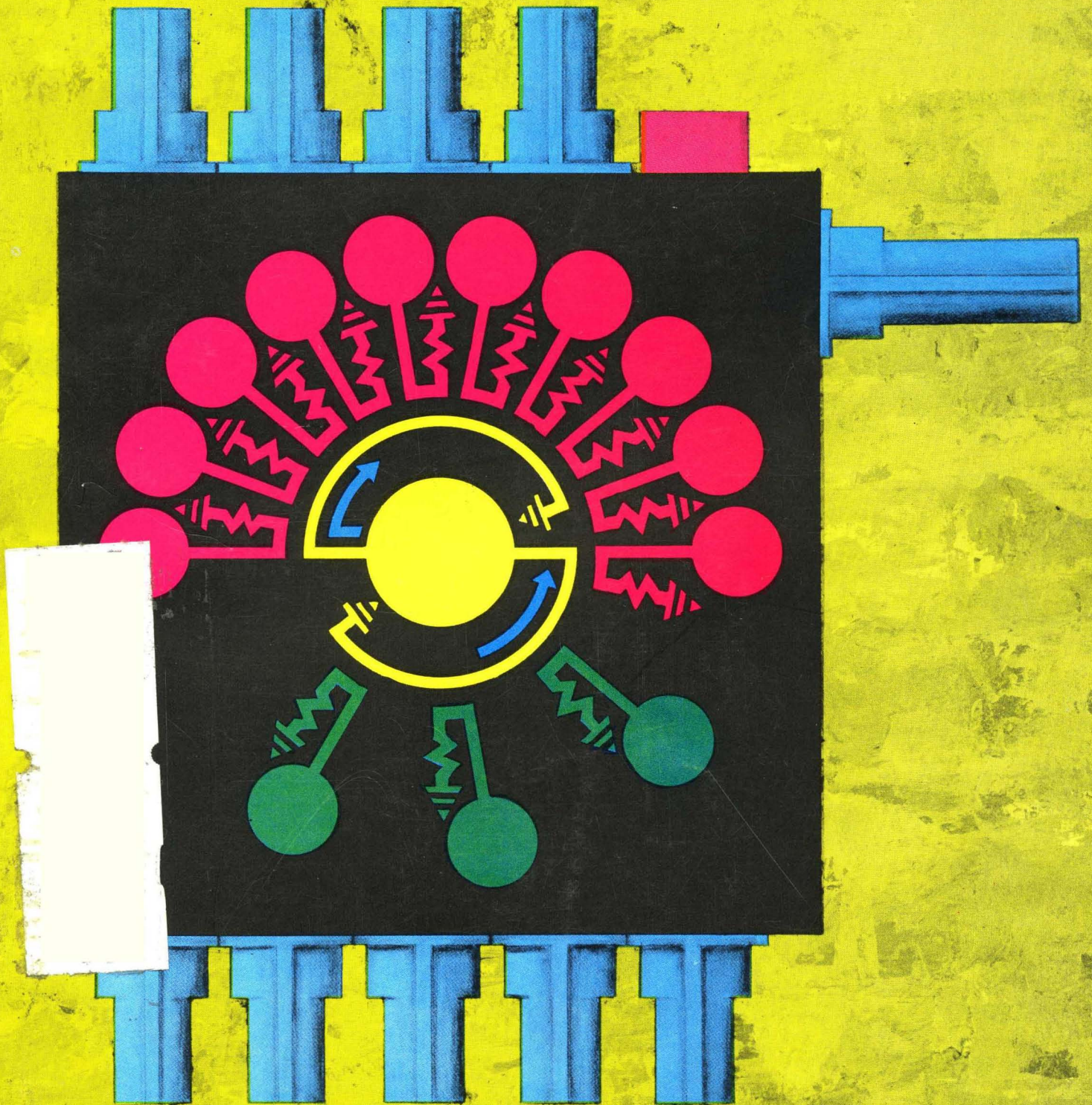


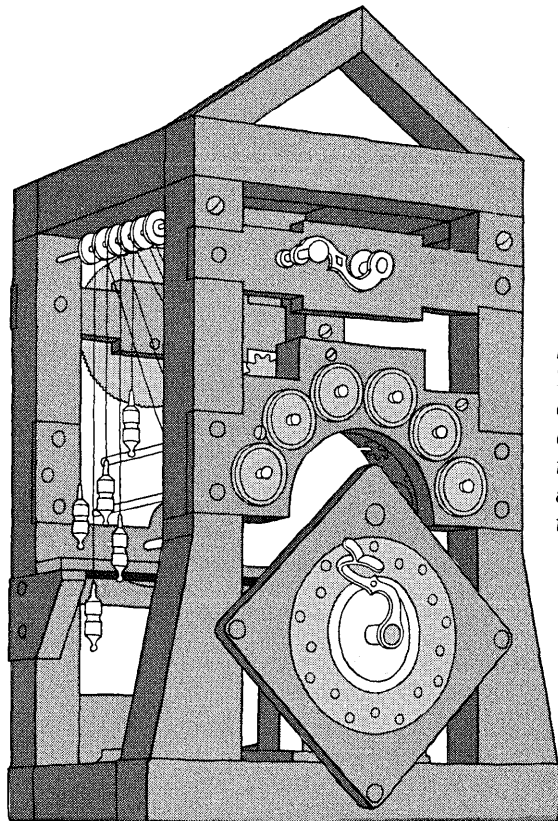
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS MAY 1969



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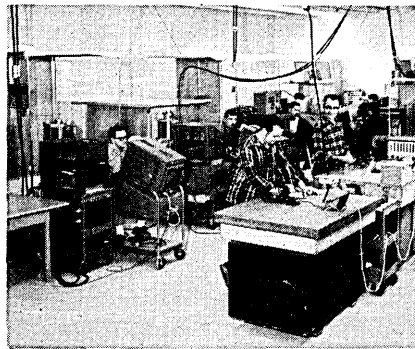
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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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Reader Service Card opposite page 106

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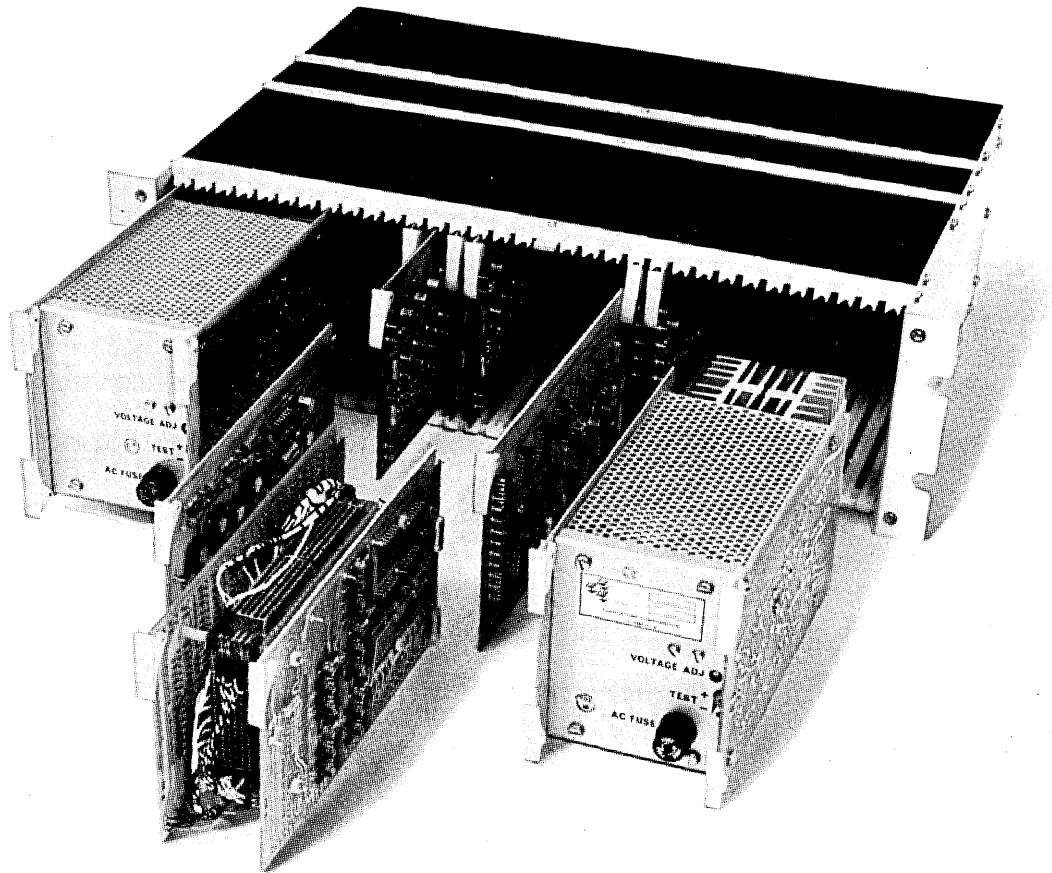
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The two major elements of the design are a 64-position matrix and a six-bit synchronous counter. (The counter is composed of a 9316 four-bit binary counter and a 9020 dual JK flip-flop.) The three Most Significant Bits of the counter output address the 1-of-8 decoder (9301) forming one side of the matrix, sequentially driving its outputs "low". The three Least Significant Bits address the 9312 scanning multiplexer (the other side of the matrix), sequentially looking at its eight inputs. With this arrangement, all multiplexer inputs are scanned once for every change in the decoder output.

Each intersection of the decoder outputs and the multiplexer inputs can be used as a key position. If one of the keys is depressed, a "low" from the decoder is detected by the multiplexer and converted to a "high" on its negation output. This triggers a one-shot that inhibits the counter from advancing further and provides a "data ready" signal. The duration of the one-shot is set to cover any possible contact bounce. The output of the counter can now be used as

the encoded signal, and the matrix can be arranged so that any key closure provides any binary code from 000 000 to 111 111.

The code that appears corresponds to the first key depressed. As long as that key remains down, the retriggerable one-shot continues to receive reset pulses that hold the counter at the count independently of any other switch closures on the board. Once that key is released, the counter resumes its scanning after the one-shot time period has run out.

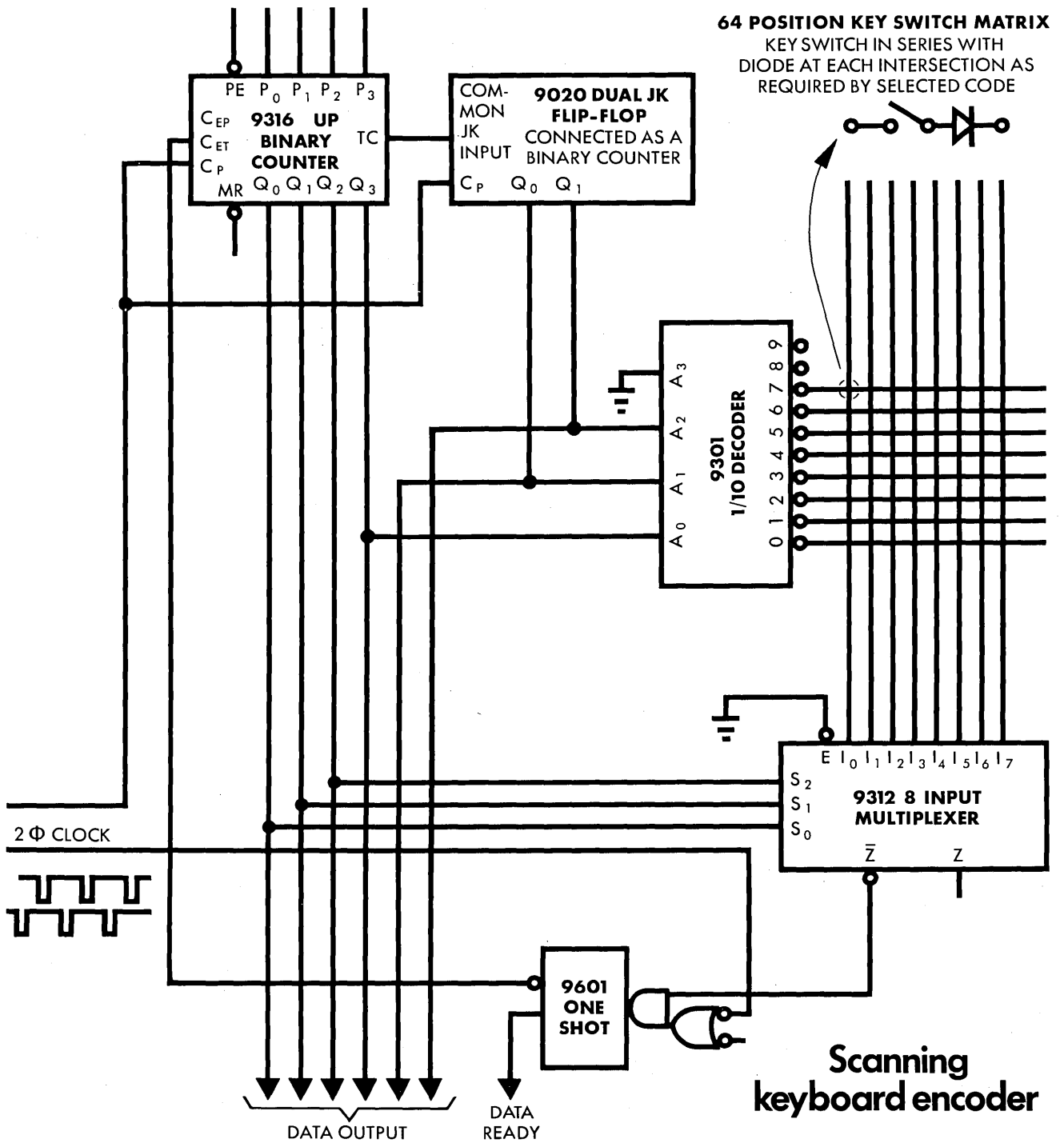
The addition of a few more MSI elements would add even greater capability to this design. As an example, the addition of another 9312, 9316 and 9601 can result in a single serial binary PDM output group in response to each key depression. Additional control inputs could be used to restrict the range of the scan counter if only certain keys should be enabled in a certain mode as is the case in key punch machines. Addition of a 9304 Read-Only Memory would allow the selection of any code output with a single keyboard design. A single monolithic parity generator could be added to provide parity at very little additional cost. Or, you might want to add two Read-Only Memories to drive a character display and a normal output simultaneously.

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CIRCLE NO. 6 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

The B6500 Design group has read your HTI article with great interest, and would like to point out the following:

1. There exists a class of external conditions of such low priority that it is not desirable to provide interrupts. In the B6500, this class includes the READY-STATUS of unassigned peripheral devices. In a multiprocessor system, the first processor to reach the idling state should loop on an interrogation of these conditions.
2. The IDLE-UNTIL-INTERRUPT operation is performed by the initial-load function.
3. On occasion, it becomes necessary for the (current) 'Master' processor to tell the others to 'Get out of the way.' This occurs, for instance, during a system 'breakout' or 'checkpoint.'
4. It is definitely not desirable, in a non-dedicated machine, to allow user programs to idle. The goal of the system is to maximize throughput, not just to exhaust time quanta.
5. If the processor is capable of a non-interruptable state, and attempts to idle in that state, interrupts should be temporarily allowed.

These considerations, as well as those you mention in your article, were involved when we included the idle until interrupt in the instruction repertoire of the B6500—two years ago.

William C. Price
Programming Systems Department
Burroughs Corp.
Pasadena, Calif.

To the Editor:

The technical note in Computer Design/February 1969 on the Halt Til Interrupt instruction was read with interest. Further information on Univac 1100 series hardware and software will be of obvious interest to you.

The Univac 1107 had a WAIT instruction which is very similar to the

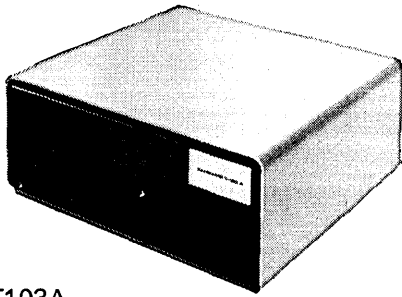
HTI instruction you proposed. Instruction execution in the 1107 halted when a WAIT instruction occurred, until resumed by an interrupt. The 1107 is designed for multiprogramming, but never multiprocessing.

We decided to omit the WAIT instruction during design of the 1108. The 1108 is a unit processor multiprogramming and multiprocessor system. It was felt that the functions of the WAIT instruction could better be performed through other sequences.

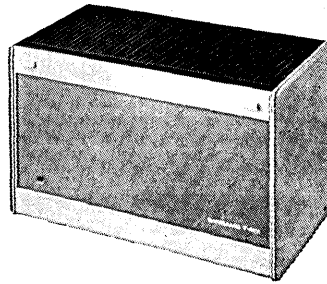
EXEC-8 of the 1108 Operating System has an idle loop consisting of one Block Transfer instruction and a small loop of five tests. The Block Transfer consists of a register to register transfer which is completely harmless in that index register zero is used for the from and to addresses. One core memory reference is required to fetch the instruction, but no data references to core memory are needed for the index registers are internal processor flip flop registers. We can create an arbitrarily long time duration instruction which requires only one core memory reference using the Block Transfer instruction in this manner. The current repeat count used is 1000. The fact that the repeat register of the processor must be used is of little consequence in this case for being in an idle state, we cannot predict for whom the register should be loaded as we are waiting for the external signal to enable some program to again operate. The five test instructions are described later.

The EXEC-8 Block Transfer Instructions then becomes within one memory cycle of being the ideal WAIT instruction. This idle loop code while contained within the Executive operates at a priority level similar to that of the user program. At the same time, a flag is set indicating that no user program is in control. Therefore, at an interrupt the idle loop sequence is merely aborted, no attempt is made to save the state of the idle loop, and control moves to the top of the D spatcher which is our routine for program switching. The D spatcher scans through the Switch List looking for a program which can use processor time. When no activity is found the idle loop is re-initiated.

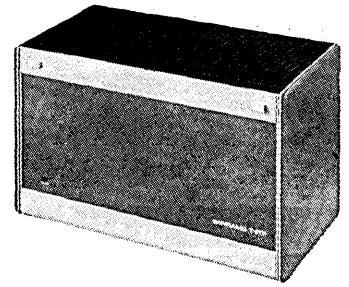
There is one remaining problem in this technique, and is the reason why
continued on page 10



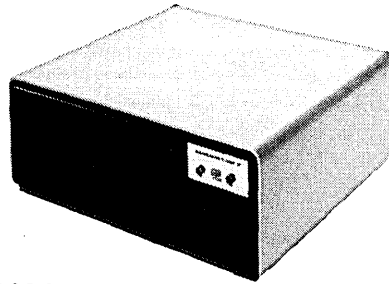
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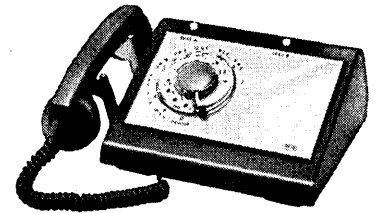
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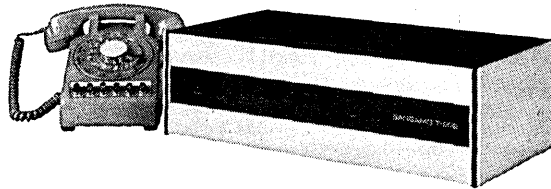
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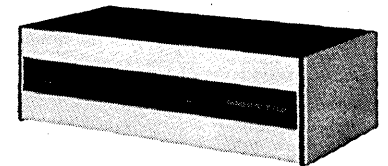
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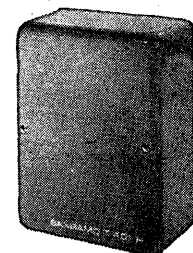
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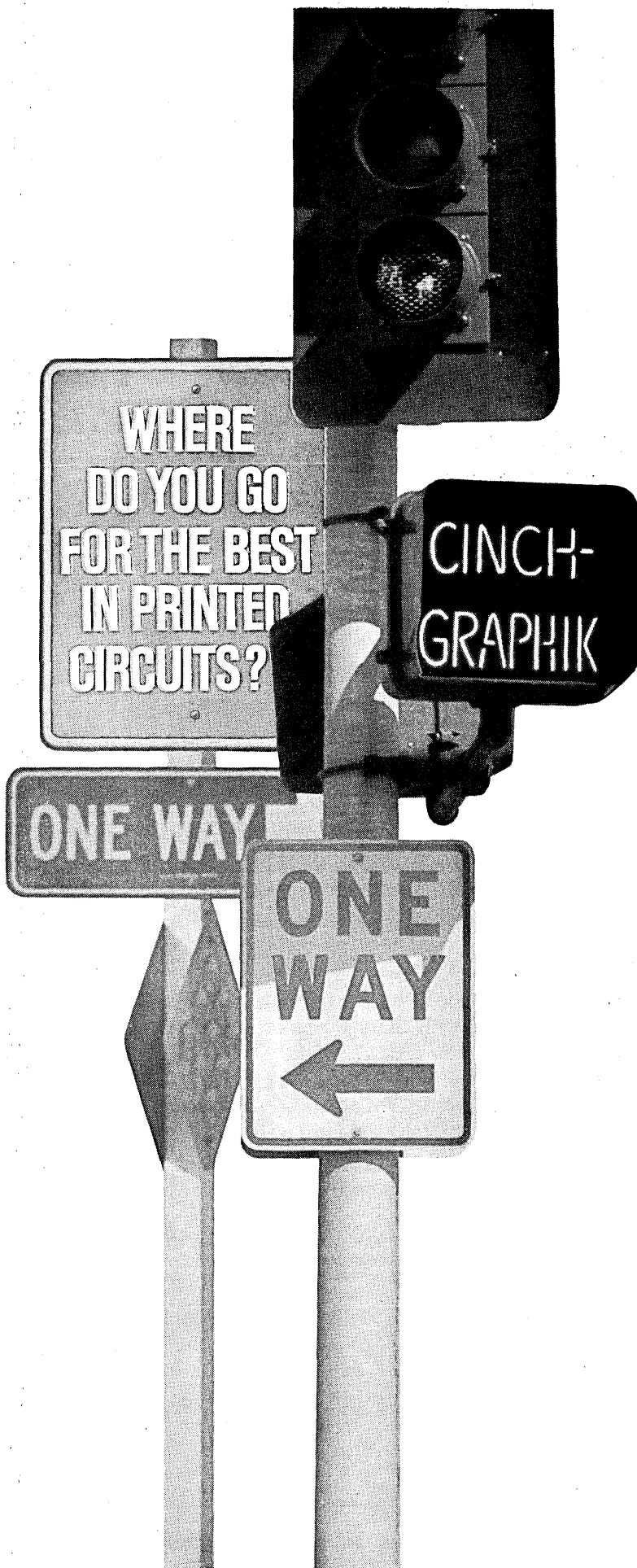


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CIRCLE NO. 7 ON INQUIRY CARD



LETTERS TO THE EDITOR

continued from page 8

the five tests mentioned above must be in the idle loop. In a multi-processor, a processor should be stimulated by an input/output interrupt or by another processor. The second processor may create more activities in need of processing. The active processor must interrupt the idling processor, or the idling processor watch the Switch Lists to observe the introduction of a new activity. In the current EXEC this interrupt scheme from the active to inactive processors does not exist. Each idle processor during the cycle through the idle loop makes a test on each of the five Switch Lists to catch the introduction of the new activities.

We hope this information on Univac systems will be helpful, and stimulate thoughts on an efficient solution to the problem mentioned.

John M. Macgowan Jr.,
Univac Div., Sperry Rand Corp.,
Roseville, Minn.

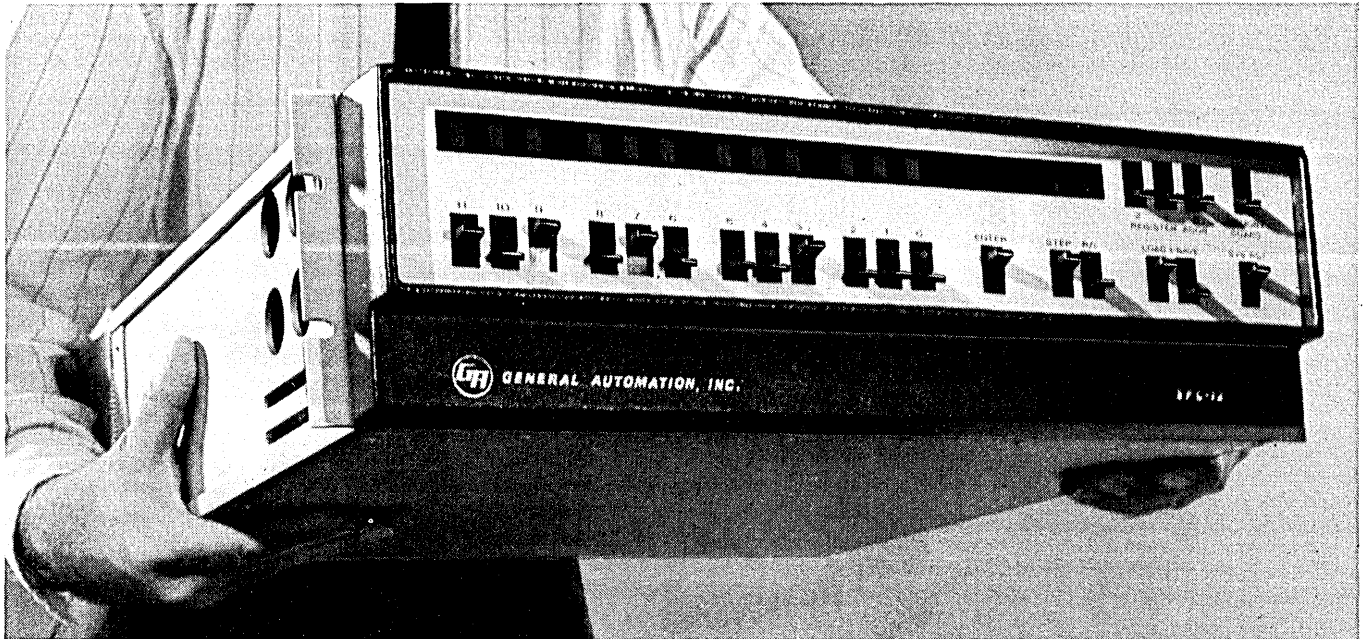
To the Editor:

Re the article, "HTI: An Order to Improve Multiprocessor Performance," Computer Design/February 1969. Mr. Peters has overlooked one of the computers which is used in the pre-launch checkout of the Saturn missiles.

This instruction is called a Halt Interruptible (HTI) and is the same as the Halt instruction (HLT) except that it can be resumed either by depressing the START button on the Maintenance and Control panel or by an interrupt request. When an interrupt occurs, the location of the HTI is stored in a standard memory location depending on the interrupt level. When the interrupt has been serviced, the program can return to the HTI location or any other memory location by using the Return After Interrupt (RAI) instruction. If the START button is used to resume operation, the program begins with the next sequential instruction.

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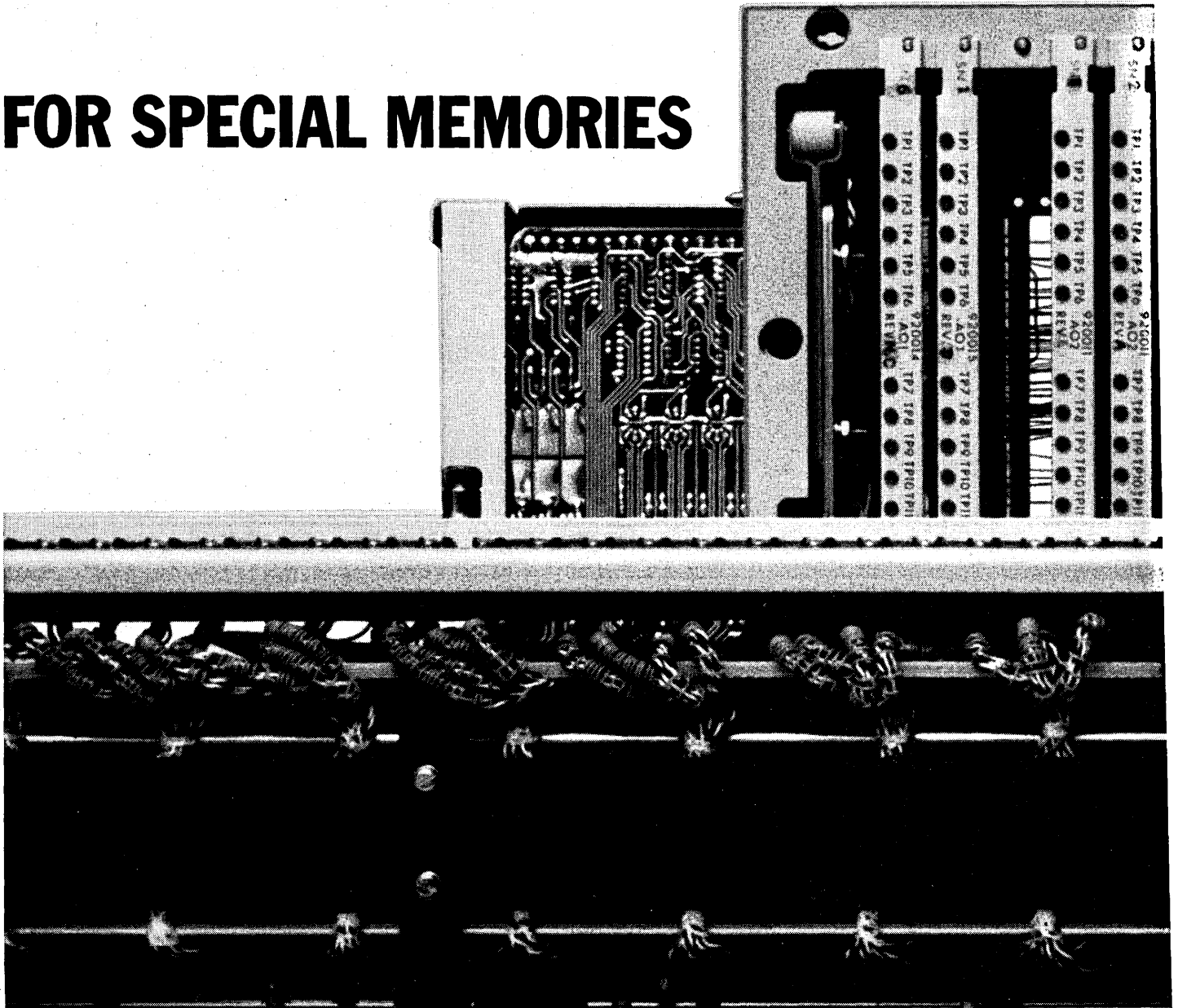
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of MIL-E-5400, MIL-E-4158 and MIL-E-16400.

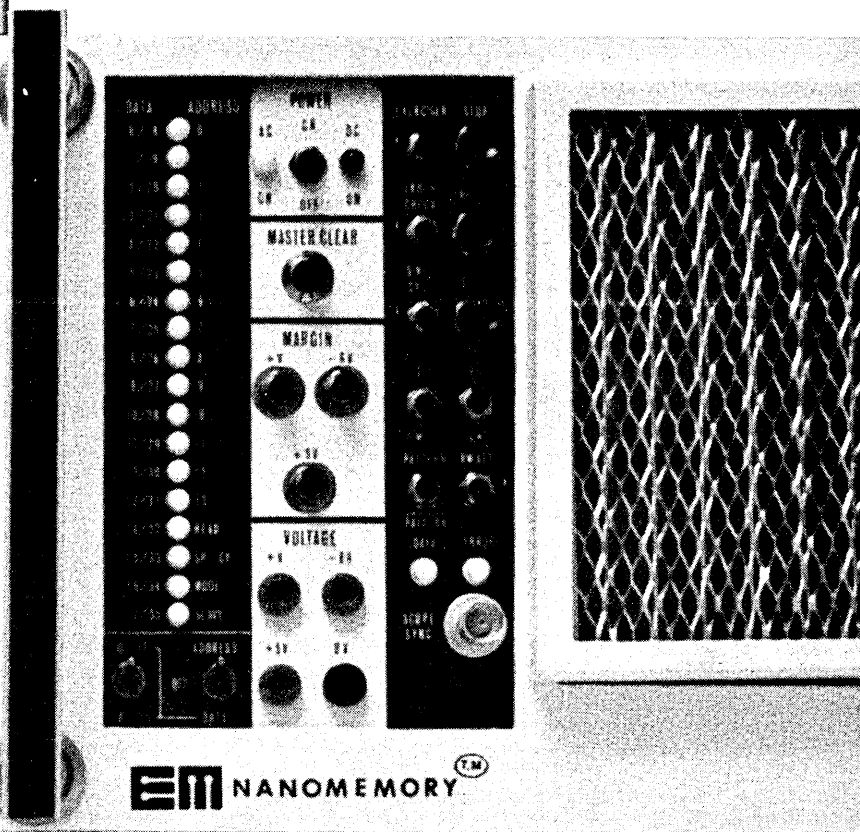
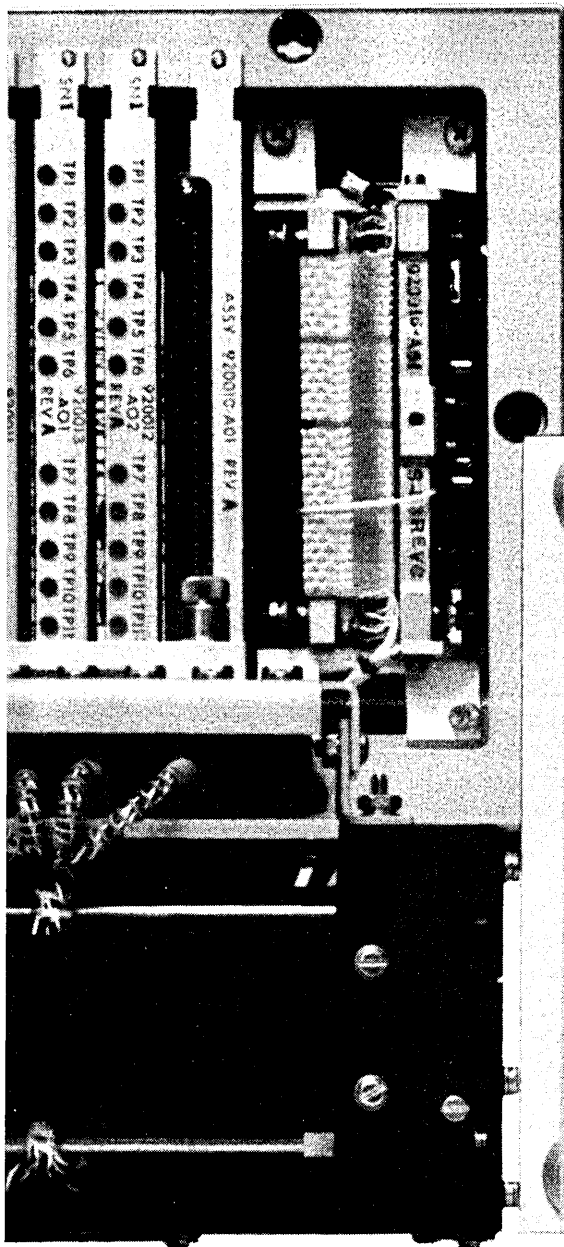
B. If you need a ground-based militarized system, look at our SEMS 7. It's not as small as the SEMS 5, but has more storage (327,680 bits with a $2\mu\text{s}$ cycle time). And it meets all the applicable portions of MIL-E-4158, MIL-E-16400 and SCL-6200.

C. For more speed, there's our NANOMEMORY™ 2650 System. It's built with IC electronics, uses a $2\frac{1}{2}$ D drive and stores up to 294,902 bits with a cycle time of 650ns. You can even get it with a built-in self-tester. All in a $2\frac{5}{8}$ cubic foot module that does everything bulkier systems do.

D. And for low cost systems, use

our MICROMEMORY™ 1000. You get up to 32k bits of storage with a cycle time of $2.5\mu\text{s}$ occupying only 400 cubic inches and dissipating 35W. We use a special 3 D technique that both lowers the component count and increases the MTBF. The MICROMEMORY 1000 comes with no case so there are no special cooling requirements, while true random access and a simple I/O interface make for easy integration into your system.

E. If you're starting further back than that, pick one of our stacks. $2\frac{1}{2}$ D or 3 D. Military or commercial. Miniaturized, heated, folded or split into modules. Whatever's exactly right for your application.



F. Or, if you're working right from scratch, we've got cores. 18 to 80 mil magnesium-manganese cores that operate from 0°C to +65°C, with cycle times that range down to less than 600ns. 18 to 30 mil lithium ferrite cores that operate over the full temperature range from -55°C to +125°C. We've made cores for all the major computer programs and most of the satellites. And we're building them for our own systems. Right now and in volume.

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If you're not at the hardware stage yet, maybe we can help with your design. The group below is our Memory Squad, our senior engineering staff. Write and we'll send you the whole group for a day. They'll give you a one-day seminar on memories in your plant. It will cover



everything from cores to memory systems, with the emphasis on the practical aspects of implementing designs. They've designed and built equipment for the full range of applications from satellites to computers to submarines. Write requesting the seminar and get some of their experience into your systems now. They're standing by.

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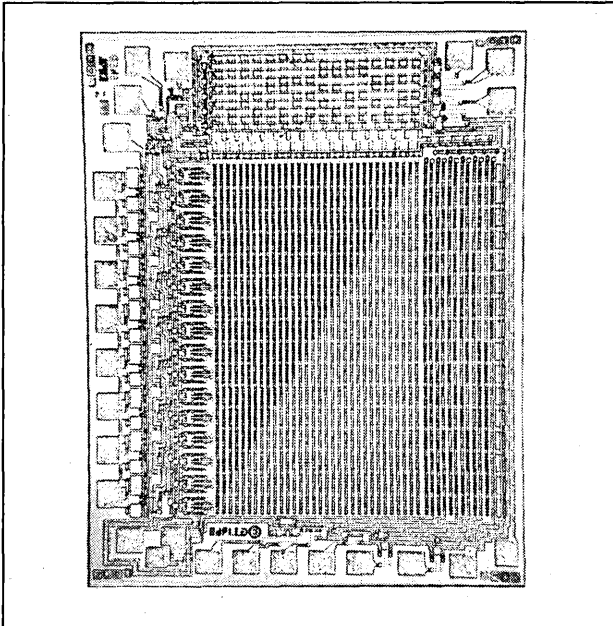


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2048 BIT ROM

READ ONLY MEMORY



Now, for the first time – off-the-shelf customized LSI memory chips organized for low-cost, quick-turn-around, mass production . . . available only from General Instrument.

- Outputs can drive TTL, DTL or MOS without interface hardware
- Up to 11 bit decoding matrix
- Expandable to 2048 x 8 ROM modules without additional hardware
- Power Dissipation 120 mW @ 1MHz
- 1 microsecond access time
- Non-volatile, non-destructive memory

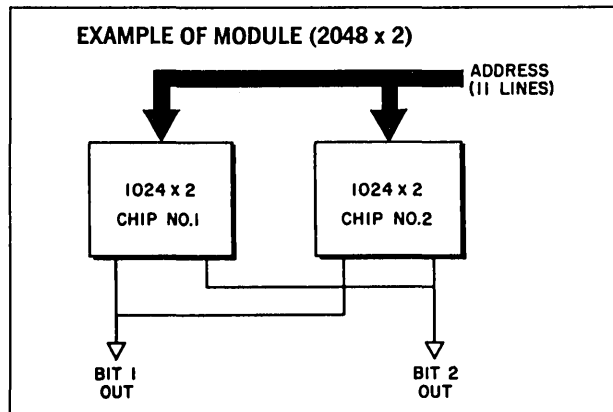
General Instrument's exclusive 2048 bit ROM (Read Only Memory) cell is a four phase MTOS array consisting of 11 bits of two dimensional addressing (5 and 6 bits respectively) and 8 outputs. It permanently stores 2048 bits of information in a 64 bit x 32 bit matrix positioned into 8 segments, each of which contains an 8 bit x 32 bit matrix and an output stage. The ROM chip outputs have internal "wire-or" capability which allows the formation of ROM modules without any other component

< 1 PER BIT*

ROM ORGANIZATION CHART						
No. of Outputs Per Chip	No. of Bits of Addressing Used Per Chip	No. of Bits Available For Chip Select	No. of Bits Per Word	No. of Words Per Chip	No. of Chips Per Module	Total Bits Per Module
1	11	—	1	2048	1	2048
2	10	1	2	1024	2	4096
4	9	2	4	512	4	8192
8	8	3	8	256	8	16384

additions. This organization permits an extremely wide range of operating variations with a modular capability applicable to virtually all ROM systems.

Since any and all changes to the ROM chip, both data pattern and "chip-select," are made by alteration to a single mask only, low cost, quick-turnaround time is guaranteed for customized ROM circuits.



General Instrument's 2048 bit ROM cells are designed to undercost and outperform cores, drums, delay lines and complex logic functions, while providing dramatic savings in space and weight.

Write for full information. (In Europe, to: General Instrument Europe S.P.A., Piazza Amendola 9, 20149 Milano, Italy.)

*At quantities in excess of 25,000 ROMs.



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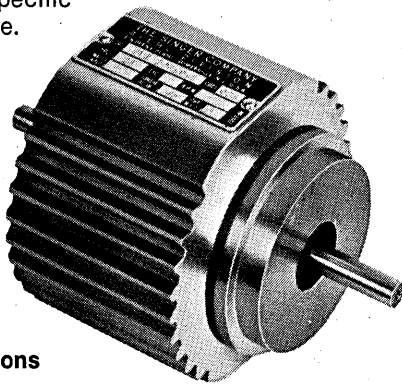
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Some Suggested Applications

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- Counting
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CIRCLE NO. 11 ON INQUIRY CARD

CONFERENCE CALENDAR

May 22-23—Workshop on Applied Magnetics, Sheraton Park Hotel, Washington, D.C. IEEE Magnetics Grp. Info: G. I. Duncan, GE Co., Fort Wayne, Ind. 46804.

May 26—Computer-Aided Device Analysis and Design Seminar, Stevens Inst. of Technology, Hoboken, N.J. IEEE N.Y. Section, Stevens Inst. of Tech. Info: Rene Colen, Hewlett Packard Co., 100 Locust Ave., Berkeley Heights, N.J. 07922.

June 3-5—Conf. on Microelectronics, Congress Theater, Eastbourne, Sussex, England. IEE, IERE, IEEE U.K. Info: IEE, Savoy Place, Victoria Embankment, London, W.C. 2, England.

June 8-12—6th Annual Design Automation Workshop, Hotel Carillon, Miami Beach, Fla. ACM, IEEE, SHARE. Tech. Info: Dr. H. Freitag, IBM Watson Research Ctr., P. O. Box 218, Yorktown Heights, N.Y. 10598.

June 9-11—Int'l Communications Conf., Univ. of Colorado, Boulder, Colo. IEEE Communications Technology Grp. & Denver Section. Info: A. J. Estin, Radio Stds. Eng. Div., NBS, Boulder, Colo. 80302.

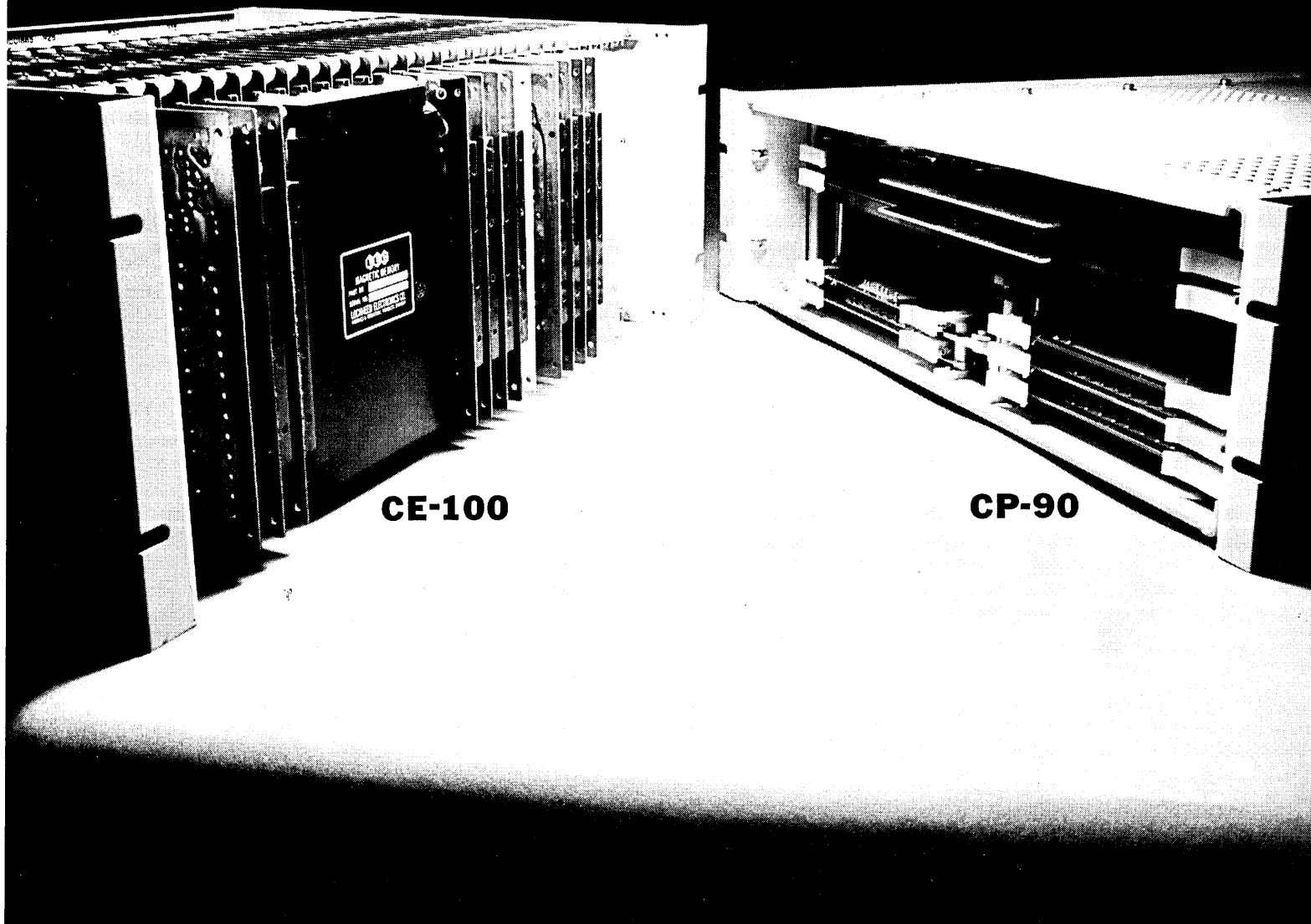
June 17-19—IEEE Computer Conf., Leamington Hotel, Minneapolis, Minn. IEEE Computer Grp. Info: K. S. Foster, Honeywell Inc., 2345 Walnut St., Roseville, Minn. 55113.

July 14-15—Workshop on Computer Reliability, Santa Ynez Inn, Pacific Palisades, Calif. ACM, UCLA. Info: Prof. Algirdas Avizienis, Dept. of Elect. Eng., U. of Calif. Los Angeles, Calif.

July 23-25—Conf. on Digital Methods of Measurement, U. of Kent, Canterbury, Kent, Eng. IERE, IEE, U.K. & Rep. of Ireland Sec. Info: Conference Registrar, IERE, 8/9 Bedford Sq., London, W. C. 1 Eng.

CIRCLE NO. 12 ON INQUIRY CARD →

The case of Lockheed vs. Lockheed



1. Capacity: 4,096 words x 16 bits.
2. Available in capabilities of 4, 8, 16K with 8 to 32 bits.
3. Size: 19" x 7" x 13".
4. Speed: 1 microsecond.
5. Random access time: 450 nanoseconds.
6. Market Response: Excellent.

1. Capacity: 4,096 words x 16 bits.
2. Available in 4K by 16 or 18 bits.
3. Size: 19" x 5¼" x 13".
4. Speed: 900 nanoseconds.
5. Random access time: 400 nanoseconds.
6. Market Response: Too early to form any sort of judgment.

VERDICT

The CE-100 has been the most successful low-cost memory unit on the market (and with good reason). But since the CP-90 is faster, smaller, and since the 16-bit version costs less — it is our considered opinion that the CP-90 will become one of Lockheed's all-time best-selling memory units.

For further information write: Memory Products, Lockheed Electronics Company,
Data Products Division, 6201 East Randolph Street,
Los Angeles, California 90022. Telephone (213) 722-6810.

LOCKHEED ELECTRONICS COMPANY

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BRUNNEN 3167

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Honeywell introduces Ultramation for under \$10,000.

It's the new H316 computer. And when Honeywell hangs an under-\$10K* price tag on a 16-bit computer, you get big-computer-company backup for the first time. That means on-time delivery of one H316 or hundreds . . . world wide support . . . a full line of proven peripherals.

That's Ultramation . . . the ultimate in automation by Honeywell computers. The H316 is the newest and smallest member in the Honeywell Series 16 family of computer systems. It's logically identical to the DDP-516 — same organization, instruction repertoire and interface characteristics. Result: More than 500 programs you know will work. And you can grow into larger Series 16 computer systems without costly reprogramming.

Typical applications: industrial, mil/aero and other real-time control systems; research, scientific data acquisition, hybrid, data storage and retrieval, and communications.

Key Specifications:

Word length — 16 bits.

Cycle time — 1.6 μ secs.

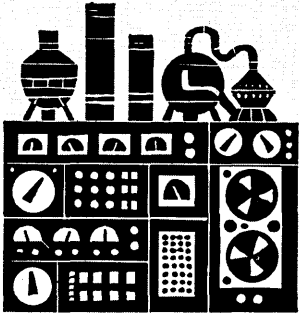
Memory size — 4-16K. 72 instructions.

Hardware index register. Multi-level indirect addressing. Dual register shift capability. Power failure interrupt.

See all 3 models at SJCC (Booth 2801). Discover the meaning of Ultramation in an under \$10K computer. Write for complete specs: Honeywell, Computer Control Division, Dept. 20, Framingham, Mass. 01701.

*Rack-mountable version. Table top and pedestal models also available.

Honeywell
A U T O M A T I O N
CIRCLE NO. 13 ON INQUIRY CARD



INDUSTRY NEWS

SIMPLIFIED COMPILER DESIGN PROPOSED—A simplified method of designing compilers for programming of computerized automatic test equipment used by airlines has been proposed by the Columbus Laboratories of Battelle Memorial Institute.

Details of an 18-month program, aimed at developing the design of a compiler based on a modular scheme, were explained to representatives of some 50 organizations involved in avionics at recent meetings held at the research center and in London.

According to Battelle's Michael Tikson, chief of computation research, the modular approach will allow a substantial part of the compiler used

in translating program language into machine code to be standardized and developed independently of any particular piece of test equipment.

"The need for such compilers," he says, "stems from the increasing use of a variety of testing equipment by airlines and from the development of the Abbreviated Test Language for Avionics Systems (ATLAS) by the Air Lines Communications Administrative Council. Current compilers are tailored to adapt to each piece of test equipment, and they represent a sizeable investment in time and money. This cost can be significantly reduced with the modular approach, making for wider use of the ATLAS language."

Battelle-Columbus proposes that a group of companies share equally in the cost and the results of the research program. Budgeted at \$240,000, the program would require the support of at least 15 companies.

"Although the airlines will undoubtedly realize the greatest reward from early implementation of ATLAS," Tikson observes, "all members of the commercial air-transport community should benefit from the program. This includes airlines, airframe manufacturers, avionics equipment manufacturers, and producers of automatic test equipment. The results of the research will also likely find application in other automatic test environments."

IMPLEMENTATION OF CODE FOR INFORMATION INTERCHANGE—On March 7, 1969, Secretary of Commerce Maurice H. Stans issued detailed instructions to heads of Federal departments and agencies for the implementation of the Federal Standard Code for Information Interchange and related media standards.

These standards were approved as Federal Information Processing Standards by President Johnson on March 11, 1968, to take effect on July 1, 1969. Secretary Stan's action is the latest of a series of steps taken to carry out the provisions of the Brooks Bill (Public Law 89-306), which has the objectives of economical and efficient purchase, lease, maintenance, operation, and utilization of automatic data processing equipment by Federal Government departments and agencies.

The Federal information processing standards program contributes to the objectives of PL 89-306 through improved cost effectiveness, extension of the economic benefits of data processing, increased freedom of selection

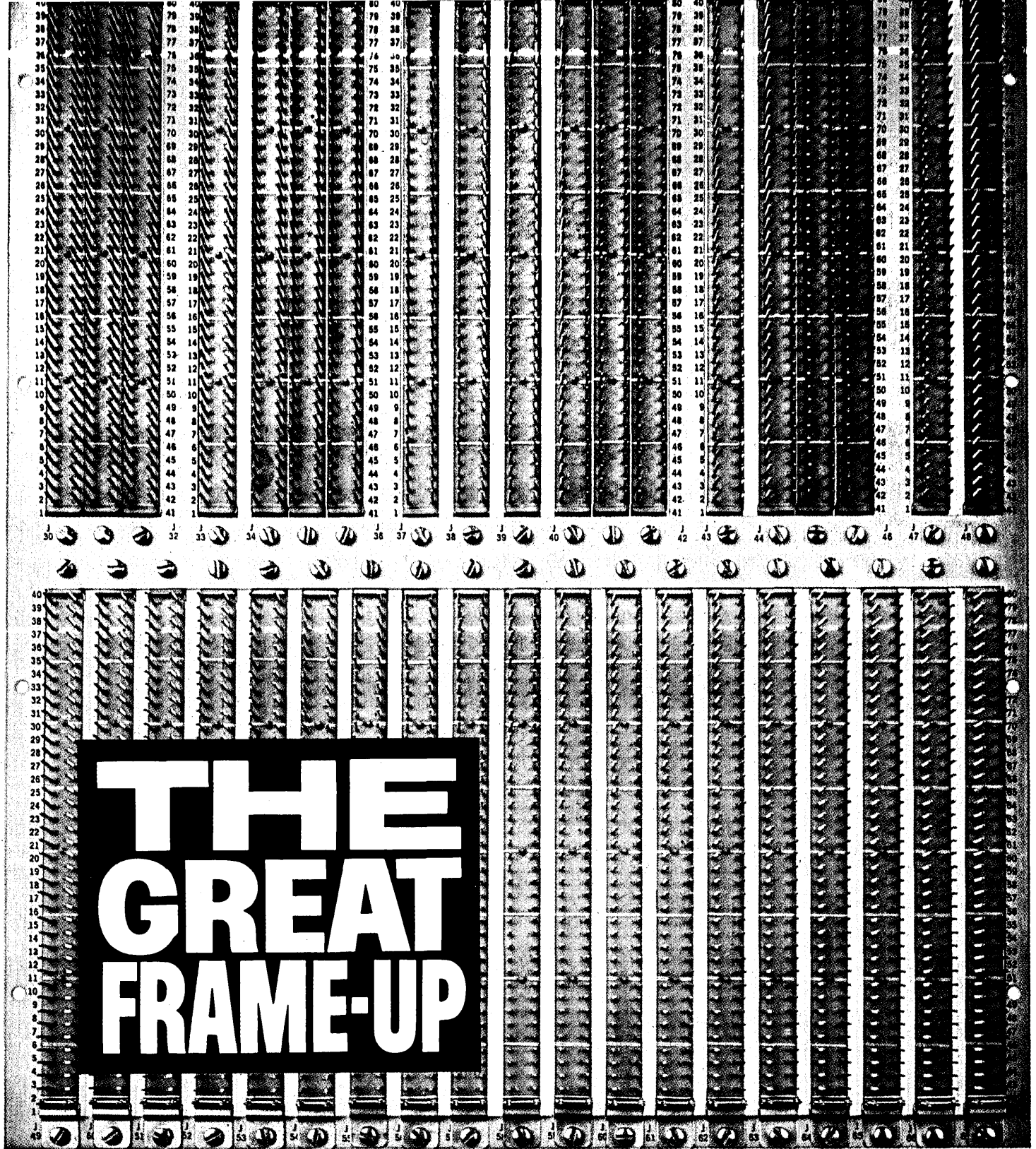
of data processing equipment, and greater flexibility in the use of equipment and programs provided by all suppliers. The basic necessities for achieving compatibility of information interchange are supplied by the new standards.

They include a standard character set, a standard coded representation thereof, a method of representing the coded character set in machine media, and a standard collating sequence. The new standards are to be used for the interchange of information in machine-processible form within and between information systems. They do not, however, extend to the internal structure of the central processing unit or peripheral devices.

The standards and their implementing instructions apply to all computers and related equipment configurations brought into the Federal inventory or acquired or leased with Federal funds as set forth in Bureau of the Budget Circular A-54 revised June 27, 1967. They also apply to data systems developed for implementation by or for Government agencies, and to data de-

veloped outside the Federal Government at Government expense if such data are to be a part of the data base of a Federal agency. Related equipment includes all character-oriented equipment in which magnetic tape or perforated tape is produced for input to a computer based data system or received as output from a computer based data system. They also apply when transmission terminal equipment and facilities are procured primarily in support of a computer based data system.

The effective date is July 1, 1969. Transition from existing equipment is to be on an evolutionary basis as equipment is replaced or added, computers reprogrammed and data systems redesigned. Instructions are provided for new installations, replacements of computers, augmentation of existing configurations, interchange situations, and ADP/telecommunications interfaces. Provision is made for certain specialized techniques such as pure binary, packed numerics, or floating point pending further standards development.



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Our new AccurFrame takes the fuss and bother out of wire-wrapping. It's easy, fast and error-free. And very simple to use.

Here's why. Our HW Series Wire-Wrap* connectors have two polarized alignment holes in the card insertion side of the block. These fit over accurately positioned pins on the alignment tool. There's no chance of a connector being placed wrong-end-to.

With connectors in perfect position, our frame is placed over the assembly; connectors are quickly attached with machine screws. The frame and connectors lift off—ready for automatic wire-wrapping.

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INDUSTRY NEWS

RECORDING SURFACE FOR DISC OR DRUM MEMORIES INCREASES BIT DENSITY—A hard metallic high density recording surface for disc or drum memories, featuring a thin-film nickel-cobalt recording media that is chemically deposited in ultra-thin layers, has been developed by Burton Magnekote, Inc., Culver City, California.

Providing a nominal increase in bit packing capability of three times conventional methods, the surfaces employ a special technique which permits depositing the recording media on any metallic substrate in a homogeneous film less than 0.2 microns thick. This provides a bit density in excess of 6000 flux reversals per inch for saturation recording.

PRELIMINARY PROGRAM ANNOUNCED FOR 1969 IEEE COMPUTER GROUP CONFERENCE—Based on the response to the call for papers for the 1969 Computer Group Conference, Professor Donald L. Epley, technical program chairman, has announced four major sessions. They are: Off-Line Computer Systems in Hospital Data Management; Real Time Systems for the Management of Acutely Ill Patients; Computer Modeling and Analysis; and Biomedical Computing.

The conference, which has as its theme "Today's World of Real Time Systems," will be held on June 17-19 in the Leamington Hotel, Minneapolis, Minnesota.

In addition to the four sessions, the technical program will also cover such topics as high speed data communications, software testing through functional simulation, small time-shared systems, on-line information retrieval systems, languages for process control and new system designs to meet specific real time requirements.

For more information concerning the conference, contact Robert M. Kalb, conference chairman, Univac Division of Sperry Rand, 2276 Highcrest Drive, Roseville, Minnesota 55113.

ACM TURING AWARD WINNER NAMED—Dr. Marvin Minsky, Professor of Electrical Engineering at Massachusetts Institute of Technology, has been named the 1969 A.M. Turing Award winner by the Association for Computing Machinery. The award is presented annually by ACM to the person deemed most deserving for contributions to the field of computer science and engineering. As recipient of the award, Dr. Minsky will deliver the A. M. Turing Lecture which opens the 1969 ACM Conference at the San Francisco Civic Center, August 26-28.

Born in 1927, Dr. Minsky served in the U.S. Navy in 1944-45, received a B.A. from Harvard in 1950 and a Ph.D. from Princeton in 1954. He is a Fellow of the Harvard Society of Fellows, the Institute of Electrical and Electronic Engineers, the American Academy of Arts and Sciences and the New York Academy of Sciences.

GENERAL CHAIRMAN OF '69 ISA CONFERENCE NAMED—Robert L. Mallory, Southwest Area Vice President for Honeywell Inc., has been named General Chairman of the 24th Annual ISA Instrumentation-Automation Conference & Exhibit. Site of the international meeting will be the Astrohall, Houston, Texas from October 27-30, 1969 and will highlight "Instrumentation + Systems + Automation for Greater Productivity."

Other chairmen announced as members of the Conference & Exhibit Host Committee include: H. Buntzel, Jr., Bonner & Moore Associates, Inc., Program Chairman; J. Dvoracek, Rockwell Manufacturing Co., Social Activities Chairman; J. W. Bergfield, Maintenance Engineering Corp., Arrangements Chairman; L. W. Lockwood, General Electric Co., Local Publicity Committee Chairman; T. H. Pierson, Coastal States Petrochemical Co., Industry Advisory Council Chairman; K. K. Wolf, Powell Electrical Manufacturing Co., International Committee Chairman; H. Cannon, Texas Instruments Inc., Public Relations Committee Chairman; E. J. Byrne, Brown & Root, Inc., ISA District VII Vice President.

OCR TYPEWRITER RIBBON STUDY COMPLETED—Technical work on optical character recognition typewriter ribbons has been completed by the NBS Center for Computer Sciences and Technology, U.S. Department of Commerce. The Center's recommendations have been forwarded to the GSA Federal Supply Service for GSA's use in preparing a Federal Specification for OCR Typewriter Ribbons.

OCR reading devices view typewritten images serially in very small areas in contrast to the larger area seen by the human eye. This makes it necessary to measure line thickness as well as imprint density in evaluating typewriter ribbons; consequently, the traditional cross-hatched pattern test for optical density cannot be used. One-time polyethylene-base typewriter ribbon is the only category of material covered by this study. Equipment, test methods, and gages are specified in the recommendations.

1970 IEEE COMPUTER GROUP CONFERENCE CHAIRMAN SELECTED—Bob O. Evans, president of the Federal Systems Division of IBM, has been named chairman of the 1970 annual computer conference sponsored by the Computer Group of the IEEE. The conference will be held at the Washington (D.C.) Hilton Hotel on June 16-18.

The technical program will emphasize the latest advances in computer memory and peripheral equipment technology. In addition to the in-depth technical sessions that have marked past Computer Group conferences, this year, for the first time, the Group will provide space for exhibitors.

Evans has held his present position with IBM since 1965. Previously, he had been a vice president of the Federal Systems Division with the management responsibility for developing large computing systems; the culmination of this work was the IBM/System 360. He joined IBM in 1951 as a junior engineer and has held a variety of engineering and management positions within the corporation.



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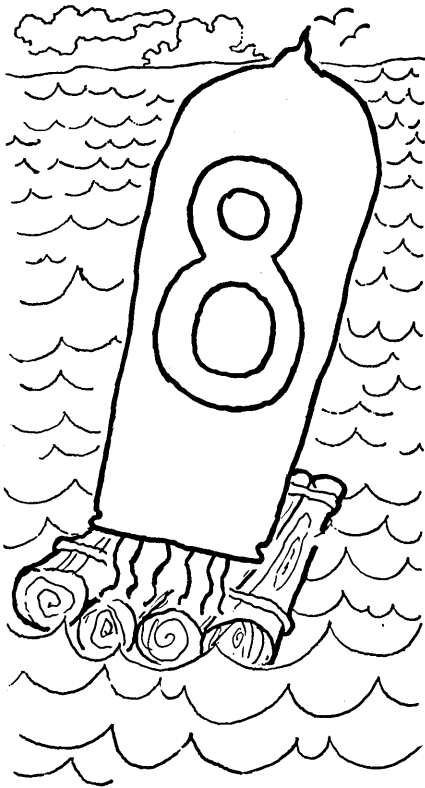
These slim space-savers bend into tight corners . . . hug contours around obstacles . . . keep wiring out of the way. They make high density interconnections easier to handle.

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CIRCLE NO. 16 ON INQUIRY CARD

INDUSTRY NEWS

SEL ENTERS COMPUTER PERIPHERAL FIELD—Systems Engineering Laboratories, Inc. has announced its entry into the computer peripheral field with the formation of a subsidiary, Peripheral Dynamics, Inc. PDI will develop, manufacture and market disc storage systems, magnetic tape units, card readers and line printers. Their initial market will be Systems Engineering's computer systems, but the subsidiary also plans industrial sales to other computer manufacturers. Peripheral Dynamics will be located in Norristown, Pa.

NEW COMPANY TO MANUFACTURE OPTICAL DEVICES FOR PERIPHERALS—Optron Inc., Carrollton, Texas, will couple the optical sensing capabilities of solid state devices of its own manufacture to product applications involving both light emitting and sensing requirements. These applications include computer peripheral equipment, rotary transducers and industrial controls.

Optron's product line will range from silicon photo transistors and diodes; optical detector arrays for card and tape reader applications; and light emitters, to custom products and subsystems utilizing unique applications of optoelectronic devices.

CHAIRMAN OF U.S. COMMITTEE FOR IFIP '71 SELECTED—Dr. Herbert Freeman of New York University has been named Chairman of the U.S. Committee for IFIP Congress '71, to be held in Ljubljana, Yugoslavia in August 1971.

IFIP—the International Federation for Information Processing—was formed in 1960 as a multi-national organization of professional and technical societies concerned with information processing. Its aim is to advance the interests of member societies through international cooperation in the field, including sponsorship of conferences, symposia and triennial world congresses.

CALL FOR PAPERS

Technical papers are solicited for presentation at the 8th Annual (1969) IEEE Region 3 convention on November 19, 20, 21, 1969 in Huntsville, Alabama at the Sheraton Motor Inn. Papers are desired which are commensurate with the convention theme "Engineering for the Seventies" and which represent innovative and advanced concepts of the technologies in such areas as communications, power, aerospace, control systems, computers, quantum electronics, microelectronics, bio-engineering, systems engineering and management.

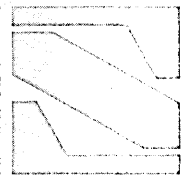
Prospective authors should submit abstracts of their papers, not to exceed 200 words, to the technical program chairman no later than June 2, 1969 for consideration. Papers should be amendable to an oral presentation of 20 minutes in length. Authors will be notified of paper acceptance by July 12, 1969. Final abstracts, suitable for printing in the Convention Record, are due September 22, 1969. Send abstracts to:

Dr. John P. Hallowes, Jr.
P. O. Box 4132
Huntsville, Ala. 35802.

Papers are being invited for the Brunel University international graphics symposium to be held at Uxbridge near London, England on April 14, 15 and 16, 1970. Areas of interest include: Applications of graphic display devices; Case studies from commerce and industry; Presentations by hardware and software companies. Several sessions will also be devoted to actual and potential applications of graphics in specific fields such as: Installations in commerce; Computer-aided design; Real time systems; and Management information systems. Papers describing new work are invited for a special technical session to be devoted to current progress in computer graphics technology.

The organizers would appreciate early notice of possible interest in submitting a paper.

Please contact: Professor M. L. V. Pitteway, Computer Science Department, Brunel University, Uxbridge, Middlesex, England.



MOS BRIEF 6

ARITHMETIC FUNCTIONS USING MOS REGISTERS

An increasing number of desk calculators (and related equipment) are using MOS shift registers for data storage or memory. In most cases the earlier equipment used delay lines for this function. In the transition, it was a natural tendency to use a configuration similar to that used with delay lines. This was reinforced by the penalty of MOS-bipolar interfacing with the earliest MOS registers.

The use of "100" material by National has produced directly compatible MOS/TTL registers. Now the MM415/515 has a structure that utilizes the freedom of the MOS register with the direct bipolar compatibility to simplify the hardware necessary for arithmetic operations.

MM415/MM515 CONFIGURATION

The MM515 is a triple 64 bit MOS shift register. Each of the three registers has independent control over recirculating data or loading from an external source. In addition to the normal 64 bit output, an early 60 bit output is available for each register. While other functional uses are the primary objective, a number of delay line lengths may be made with the device by connecting the 60 or 64 bit sections in series. The pin diagram of Figure 1 illustrates the ease of interconnection, particularly for a 192 bit delay line. (Input to Pin 1, Pin 3 to Pin 4, Pin 6 to Pin 7, Pins 2, 4, and 9 to GND, Output on Pin 10.)

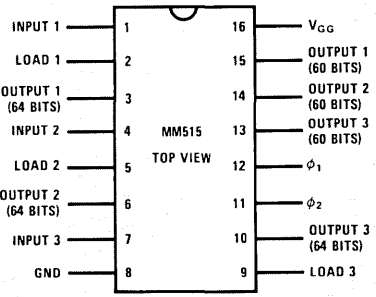


FIGURE 1. 16 Pin DIP

The primary usage of the device is as working registers in a digit and bit serial format of 16, 4 bit, coded numbers. The three registers are sufficient for the basic arithmetic operations. As an example, one contains the multiplier, one the

multiplacand, and the other receives the product. Normally these registers will recirculate with no data change. However during the execution of certain steps of an arithmetic algorithm the data will be loaded under a control command. The input may be a digit from the keyboard, the contents of another register, cleared (or zeroed) data, or the output of an adder. Figure 2 is an example

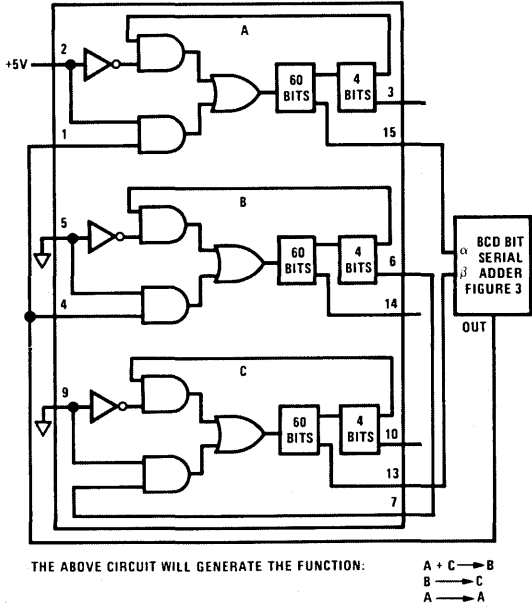


Figure 2. Typical Arithmetic Configuration

showing some of these modes of operation. The three registers are labeled A, B, and C. The data input to A and B is connected to the output of the adder. The load control input to register 1 (Pin 2) is at a logic "0" while the load control for register B (Pin 5) is at a logic "1". This forces the A register to recirculate while the B register is loaded with the output of the adder. With a logic "1" on the load control for C (Pin 9) and the output of B (Pin 6) to the input of C (Pin 7) data would be transferred from the B register to the C register. With these connections and control levels the following data movement occurs during the time the controls are active. A register is recirculated through its internal feedback path. The B register is transferred to the C. The sum of the A and the C registers will be placed in the B.

Special emphasis should be placed on the outputs used for the adder from the A and C registers. To best understand the need for the data out of the 60 bit top, examine Figure 3. In performing coded decimal arithmetic operations, a correction is necessary in addition if the result is greater than 9, or in subtraction, if a borrow is not generated. When a bit serial configuration is used it is necessary to wait until the last bit (T_4) is available before it is known whether correction is needed. One of the simpler methods of handling this is to store the result in a four bit shift register, as shown in Figure 3. During the final bit time of the digit

of the data and it must be right shifted to get it back in "sync" with the remainder of the data. This complicates the timing and control circuitry in addition to taking some time in a synchronous common clock system.

By taking the output from the 60 bit taps, the data is available 4 bits earlier. If the selection of this data is accomplished at the proper time, the output of the adder/subtractor is correct in time to be inserted back into the result register. Referring to Figure 2, the 60 bit output of the A and C registers (Pins 15 and 13) are used for the inputs to the adder.

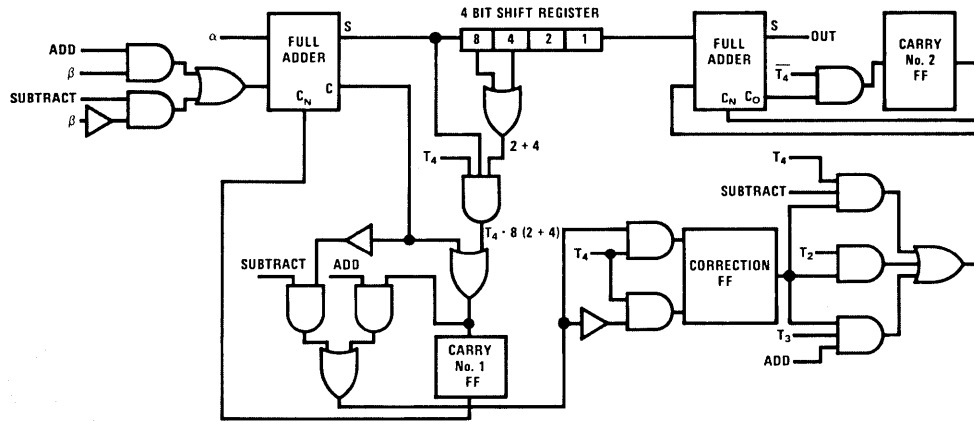


FIGURE 3. Bit Serial Adder/Subtractor

(T_4), the digit is examined for potential correction. If this is required, the correction FF is set and during the next four bit times the proper value is added to the result of this operation so that the output is available four bit times after it went into the adder/subtractor.

Figure 4 provides a more general configuration for the arithmetic operation. Signals g and h select the second source of data for the adder/subtractor. Addition/subtraction is selected by signal i. These signals must be activated four bit times before the other control signals (a - f) that control data flow.

If a normal register/adder configuration is used, the result of the addition (or subtraction) is delayed by four bits. This amounts to a left shift

Write for more information on National's MOS line of shift registers, ROM's, gates, drivers, interface circuits and analog switches.

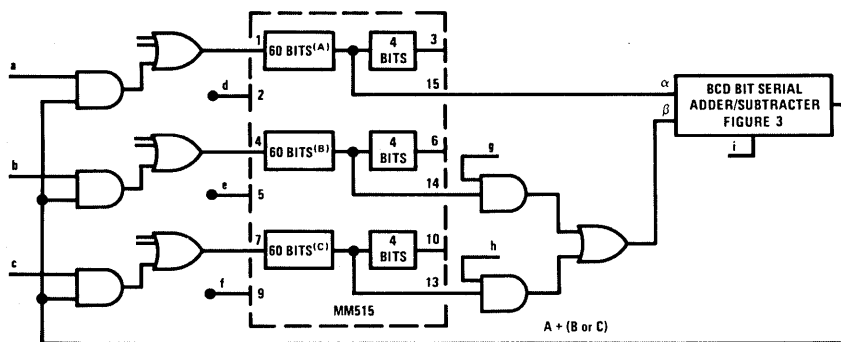
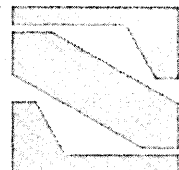


FIGURE 4. BCD Arithmetic Functions Using the MM515 for Register Storage.

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International Data Processing Conference & Business Exposition

June 16-19, 1969
Montreal, Canada

Montreal, Canada is preparing to host the 18th annual International Data Processing Conference and Business Exposition sponsored by the Data Processing Management Association (DPMA). Scheduled for June 16-19, the DPMA 1969 meeting will offer the most expansive conference seminar program and largest display of exhibits in the association's history.

An estimated 4,000 data processing executives and management people are expected to attend the 1969 meeting headquartered at the Queen Elizabeth Hotel. The DPMA business exposition is being staged at Place Bonaventure with 20-25,000 exhibit viewers expected. The event is being hosted by DPMA's Montreal Chapter, with Eric Ustad, coordinator-systems and special projects, Sir George Williams University, serving as general chairman.

The Conference educational seminar program will be the most expansive in the association's history, with ten simultaneous seminars underway for two and one-half days beginning on June 17 and concluding on June 19. The seminar program is structured in series form, covering broad topics of current interest and concern to the information processing and computer management community. The series are broken down into three separate seminar offerings providing in-depth analysis of subject matter.

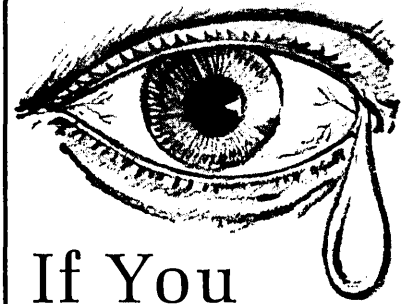
Another program element provides participants with a wide range of "open selection" general interest seminars covering such areas as general management, personal improvement, education, social implications of computers, new technical trends, and the computer utility for tomorrow's business. The overall effect provides a "short course" concept in programming designed to give concentrated attention to technical and management areas along with an overview on industrywide matters of specific interest to individual attendees.

A special seminar of exceptionally wide-ranging interest has been scheduled for evening presentation on June 18 to enable greater participation. The seminar will focus on the "Certificate in Data Processing" program initiated by DPMA in 1961 as an industrywide effort to evaluate and recognize knowledge and proficiency in the science of data processing. Panelists for the seminar will include members of the Certification Council comprised of recognized authorities in the information processing field.

The DPMA 1969 business exposition will offer the largest display of computers, peripheral equipment, supplies and services in the association's history. Most major U.S. computer manufacturers and service suppliers will be represented in the exhibits, along with a number of Canadian organizations serving the data processing community. Several firms have announced plans to unveil new product lines in Montreal, which is considered traditional for the DPMA business exposition. The exhibits will open at 1:00 p.m. on June 16, in the East Hall of Place Bonaventure.

Other highlights of the 1969 meeting in Montreal will include an industry tours program for Conference attendees, a special ladies activities program for wives of participants, and a traditional banquet topped by a professional entertainment program.

Climaxing all official Conference activity will be the traditional banquet and entertainment program, scheduled for Thursday evening, June 19. The entire DPMA Conference schedule has been advanced by one day over past patterns for the 1969 meeting to provide participants with additional time and opportunity to explore the many natural, historic and cultural beauties which exist in the Montreal area and throughout Canada.



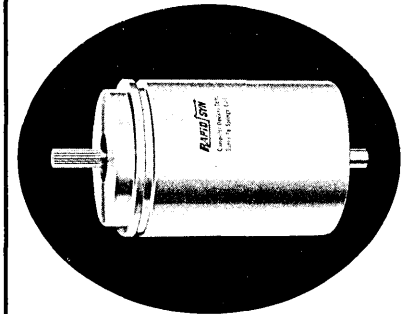
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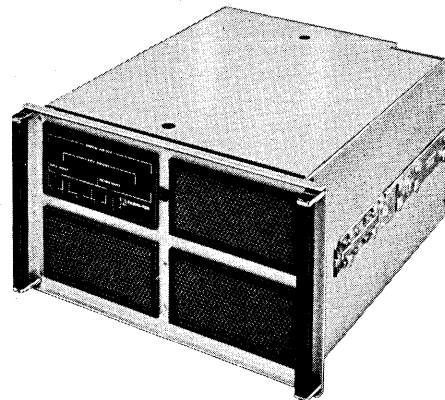


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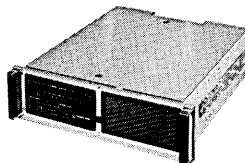
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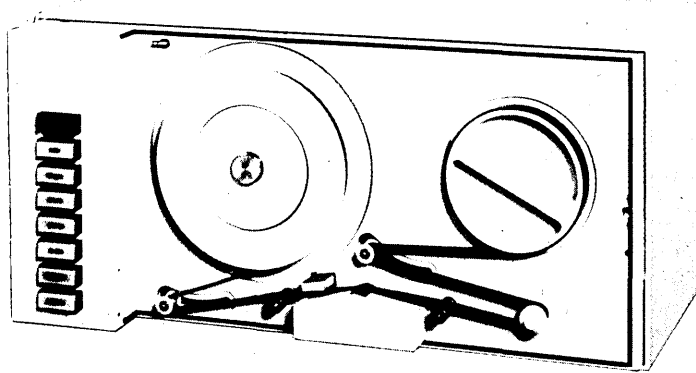
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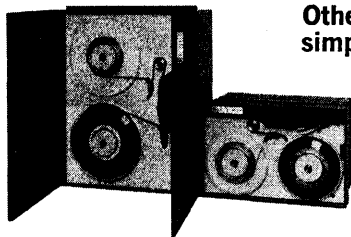
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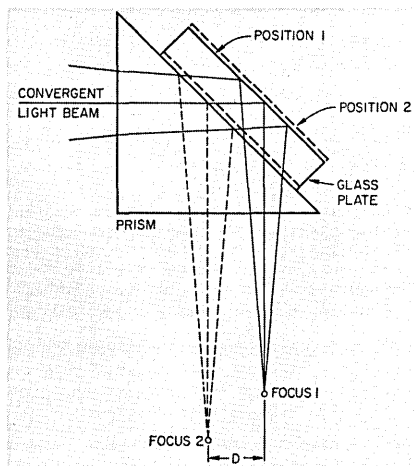
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DEVELOPMENTS

Light Beams Deflected In Thirty-Five Microseconds

An experimental device that could become an important part of future optical memories has been developed at the IBM Systems Development Division Laboratory in San Jose, Calif.¹



This diagram illustrates the basic operating principle of the experimental digital light deflector. When the plate is in contact with the prism as shown in position 1, the beam passes through the prism into the plate and is reflected to Focus 1. If the plate is out of contact as seen in position 2, the beam converges on the back surface of the prism and is deflected to Focus 2.

The device, a digital light deflector, changes the location of a light beam in 35 microseconds by a unique method of moving a glass plate in and out of contact with a prism.

High-speed deflectors of this type are potentially useful in future optical memories to randomly position a laser beam for data recording and reading. Such beam addressable memories are expected to be many times faster than present magnetic storage methods because of the relative speed of relocating a light beam in comparison to moving a bulky recording head.

The experimental deflector works on the principle of total internal reflection which minimizes loss of light. A converging light beam entering a prism is totally reflected at a right angle to its original path and brought to a focus. If not further diverted, this focal point can serve as one location for reading or writing information.

To change the position of this spot, a glass plate is moved into contact with the prism's reflecting surface—in effect making the prism larger. Light entering the prism now passes through the interface to the back of the plate and is reflected to a new focal position.

The glass plate is driven in and out of contact with the prism by a

ceramic piezoelectric disk bonded to the plate. When a voltage is applied to the disk, the ceramic material expands causing the thin plate to arch away from the prism.

The driver need only move the plate about 35 millionths of an inch to prevent the light beam from crossing the boundary and entering the plate. Despite this small distance, early models of the deflector required some 4000 volts to separate the two surfaces.

The San Jose researchers lowered this voltage to 300 volts by introducing structural changes in the plate. For example, grooves ground into the plate allow it to bend more readily, and surface depressions promote a "peeling" action that makes lifting the plate easier. Operating at the lower voltage makes it possible to use solid state components rather than more complex circuitry to activate the driver.

At San Jose, prisms and plates have been combined to form multi-stage deflectors that produce high-quality images at several locations on a recording surface. Since the number of spots increases geometrically with additional prisms and plates, deflectors capable of addressing more than a thousand locations are considered feasible.

1. See R&D Reports, Computer Design, April 1964, p. 38.

Honeywell Targets New Computer at Management Information Usage

Honeywell EDP has introduced a medium-scale computer, the Model 3200, that is targeted at satisfying the demand for corporate-wide management information networks and communications-oriented data processing.

"The new computer meets the demand for fast, medium-priced, communications-oriented systems that will find widespread use in the 1970's," said C. W. Spangle, vice president and general manager of Honeywell's Electronic Data Processing Division.

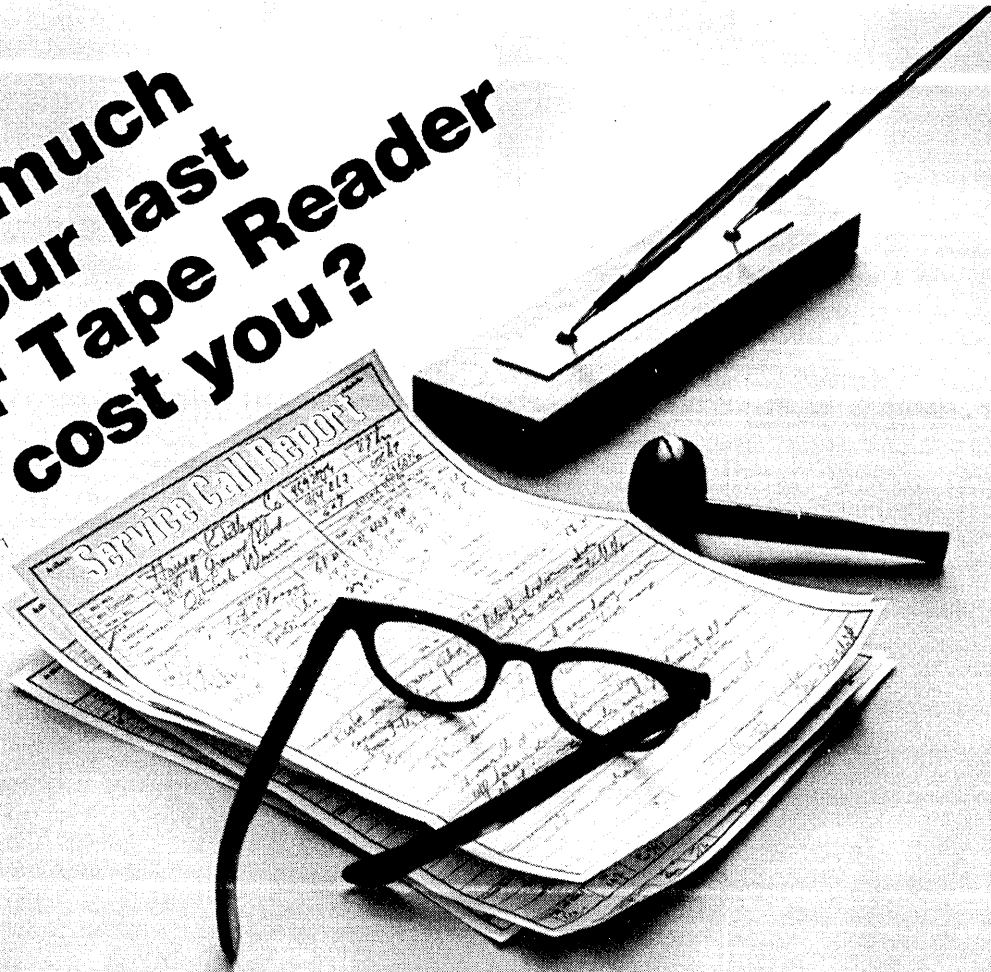
"Computerized corporate-wide management information networks—a usage that will increase seven-fold in five years, from 4 per cent to 28 per cent of the number of installed systems—will require features that are standard on the Model 3200," Spangle said.

"The total number of communications-oriented computer installations is expected to increase more than nine-fold in seven years—from 7,000 to 66,000 installed systems by 1975, although the total number of installed systems will slightly more than double in the same period," he added.

The new central processor fits between the Model 2200 and Model

4200 in price and performance in Honeywell's Series 200 family of compatible computers. It is the tenth member of the family and the fourth to be added in the past 18 months. Features of the 3200 include main memory sizes ranging from 131,072 to 524,288 characters of information, main memory cycle time of one microsecond for two characters, maximum input/output data transfer rate of 1.5-million characters per second, use of any Series 200 peripherals, full use of the Mod 4 operating system that controls up to 20 concurrent data processing jobs, and use of higher-level programming languages, Honeywell said.

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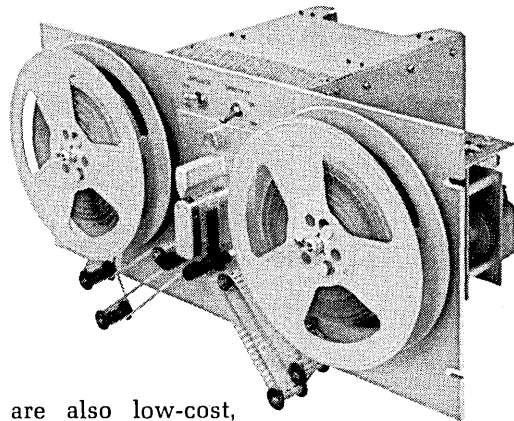
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The 1220 is not just another mechanical gadget designed as an afterthought for an overall system. It is a reliable, flexible, modularly designed piece of precision electronic equipment, built by computer specialists—interface experts—who will define your problems and provide the best equipment to solve them.

The Model 1220 is bidirectional, with synchronous or asynchronous operation. It will read accurately to speeds of 300 characters per second in local or remote locations and can be operated in either in-line or advanced sprocket formats. Completely modular, the Model 1220 can be tailored to fit a variety of applications.

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DEVELOPMENTS

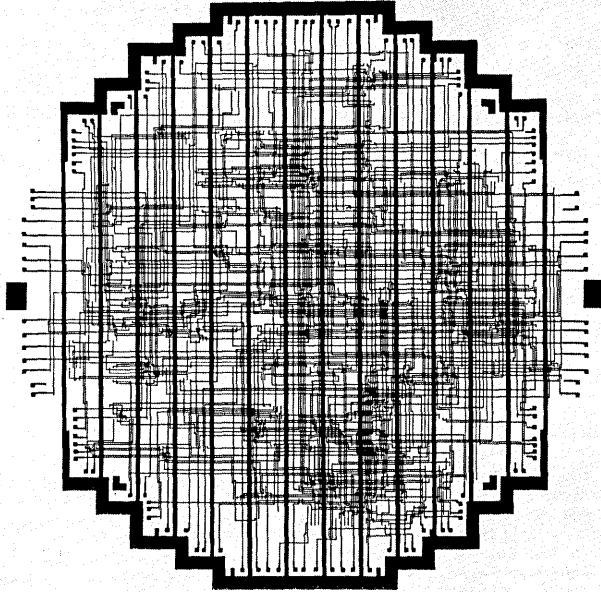
TI Develops LSI Avionics Computer

Using a discretionary-routing technique, Texas Instruments of Dallas, Texas has developed a LSI avionics computer under a contract awarded by the Air Force Avionics Laboratory at Wright-Patterson Air Force Base. The computer, chosen as a demonstration vehicle, is similar to TI's model 2502 which previously had been built with conventional ICs. It is composed of 34 individual arrays (14 different types), with an average of over 200 TTL gates per array. These 34 arrays replace 1,735 IC flat packs.

The computer is a 16-bit machine with a 2 MHz clock rate that has been designed to be compatible with the MERA (Molecular Electronics for Radar Applications) radar system which the Air Force now has under development.

The LSI discretionary-routing technique developed by TI offers numerous advantages to equipment designers in the form of customized arrays to meet specific requirements. With design automation, 200 plus-gate arrays require only a short cycle time from logic-equation inputs to finished prototypes.

High resolution processing is



Composite pattern of the multi-layer discretionary routing on a typical LSI wafer.

used to fabricate unit cells, which may be gates and flip-flops or memory storage cells, either separate or in combination on the full 1-1/2" silicon slice. After a LSI wafer has been probe-tested to determine the location of good cells,

this information along with customer logic requirements is fed to a computer. A high resolution CRT at the computed output then generates the composite pattern of the multi-layer discretionary routing on a photomask.

High-Speed Electrostatic Printer Developed

An electrostatic hard copy printer that will deliver 4800 alphanumeric lines per minute (80 lines of 86 characters) has been developed by the Clevite Corp., Cleveland, Ohio. The printer reproduces signals from any source of digital input or data transmission by telemetry, radio microwave and/or land line. It will accept serial or parallel digital data from computers, mag tape, punched card readers, raster-type CRT display memories, disc or drum memories, and communication lines, and will generate hard copy with graphic capability including multiple alphanumeric fonts, charts, graphs, schematics and patterns.

A typical visual display page is delivered complete in less than one second; a 500,000 element 8.5 x 11 inch page in less than two seconds.

Optical Technique Eliminates Light Box Glare

A new optical technique which is capable of eliminating visual fatigue encountered when small transparencies are viewed on a large illuminated area has been developed by Ingeniucs, Inc., of Gaithersburg, Md.

According to Dwin R. Craig, president of the company, there is wide use foreseen for this masking technique with light boxes used by printed circuit designers.

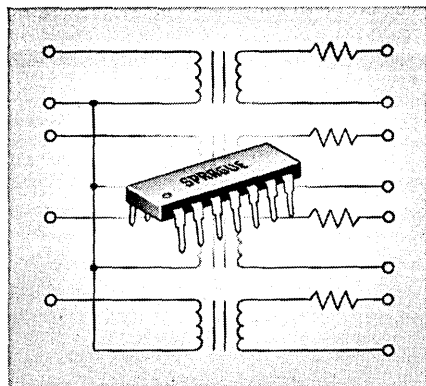
He said light from areas sur-

rounding the film is prevented from reaching the eye of the observer regardless of shape, size or position of the work. Besides eliminating glare, thus reducing eye fatigue, Mr. Craig said the technique also improves contrast within the area of interest because the reduction of glare permits the eye to operate with an open iris at maximum efficiency.

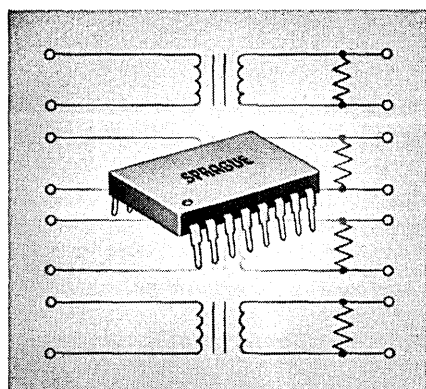
The masking technique works with modern polyester film bases such as Mylar, Cronar, Estar, Ples-tar, and also works with translucent materials such as tracing papers and cloth.

Patent applications are in process and non-exclusive licenses for a five-year period are being made available to equipment manufacturers through Ingeniucs, Mr. Craig noted.

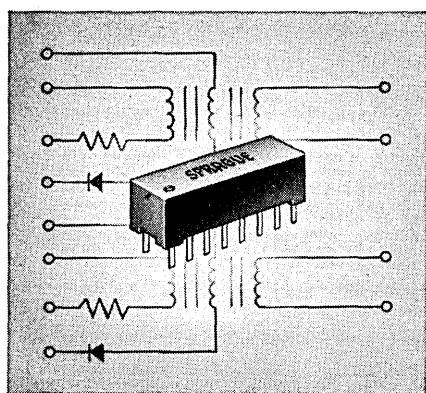
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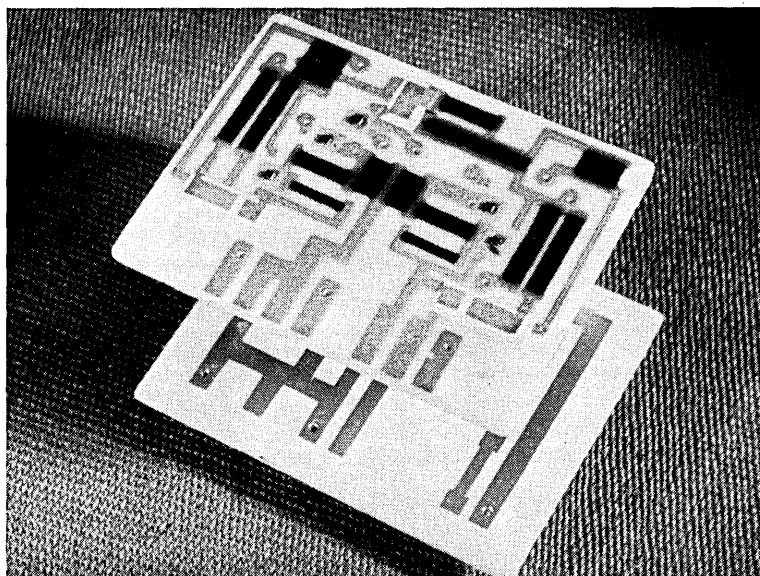


Multilayer Ceramic Wiring Structures Developed

The DuPont Company has developed new multilayer ceramic wiring structures, consisting of high-alumina ceramic parts that contain one or more layers of buried hermetic wiring of high conductivity.

"These structures are intended for use in high density packaging and interconnection of silicon integrated circuit chips," according to Dr. John J. Cox, Jr., electronic products development manager of Du Pont's Electrochemicals Department. "The primary goal of these structures is to facilitate packaging of multichip Hybrid-LSI (HLSI) arrays." Patent applications have been filed covering the new structure system.

One of the unique characteristics of the structures is their ability to be processed in high temperature oxidizing or reducing environments. This means that any one of the three metal technologies—thick film, thin film, or active metal—may be employed on top and



In the exploded view of the two-layer circuit board, one layer of buried metallized wiring appears in the figure on the top surface of the lower piece. Risers connect the buried wiring to the top and bottom of the assembled structure.

bottom surfaces for package sealing and lead attachment.

The new structures are still in the development stage and market needs and extensions of the technology are being researched and

pursued. Orders for small prototype quantities are being accepted and plans are in progress to scale up the DuPont prototype facilities to accommodate increasing demands.

Novel Isolation Methods Cut Cost and Simplify Bipolar Integrated Circuits

New integrated-circuit structures that promise to reduce the cost of bipolar circuits have been developed at Bell Telephone Laboratories, Murray Hill, N.J. The new structures are simpler to process than standard bipolar circuits, and give two to three times as many circuits on the same slice of silicon.

BTL scientists have found novel ways of electrically isolating components of bipolar circuits—the isolation occurs as an integral part of the process of making a component. In standard bipolar circuits, special isolation processing steps are needed which increase processing costs and the area of each component, and tend to reduce the yield.

Two major techniques have been established, and a modification of one yields a third approach. Each of the three fabrication methods results in circuits specifically suited

for a major area of application, determined by operating power levels and speeds.

The first method, collector-diffusion isolation, is suitable for circuits having moderate switching times and moderate power dissipation. Proposed about a year ago and verified in practice since then, collector-diffusion isolation yields circuits that may have wide uses in telephone switching systems.

Circuits made with collector-diffusion isolation use a P-type substrate and a P-type epitaxially grown upper layer. One N-type diffusion step is used to achieve several things at once. This step sets up the collector-contact areas, which also serve as isolating regions, and defines the base of the transistor by creating the isolated region inside the collector-contact ring. The same step is also used to form resistances elsewhere on the substrate.

With collector-diffusion isolation, one or two of the critical masking operations can be eliminated,

and a transistor needs only about 1/4th the area of standard buried-collector types.

The second basic method, base-diffusion isolation, has not been disclosed previously. It can be used for transistors with or without buried collector layers.

With a buried collector, the structure is suitable for applications requiring very fast switching—less than a nanosecond—such as high speed pulse-code modulated (PCM) communication systems.

Without the buried collector, the structure is designed for circuit applications emphasizing very low power consumption—as low as a few fractions of a microwatt. With this approach, a complete IC can be formed just as simply as a single transistor, since up to three masking steps can be eliminated from the standard process. Low power integrated-circuit memories and shift registers are among the specific applications under investigation.

Digitally Controlled Power Sources

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Description2, 3
Features4, 5
Applications6-9
Interfacing10-14
Specifications15

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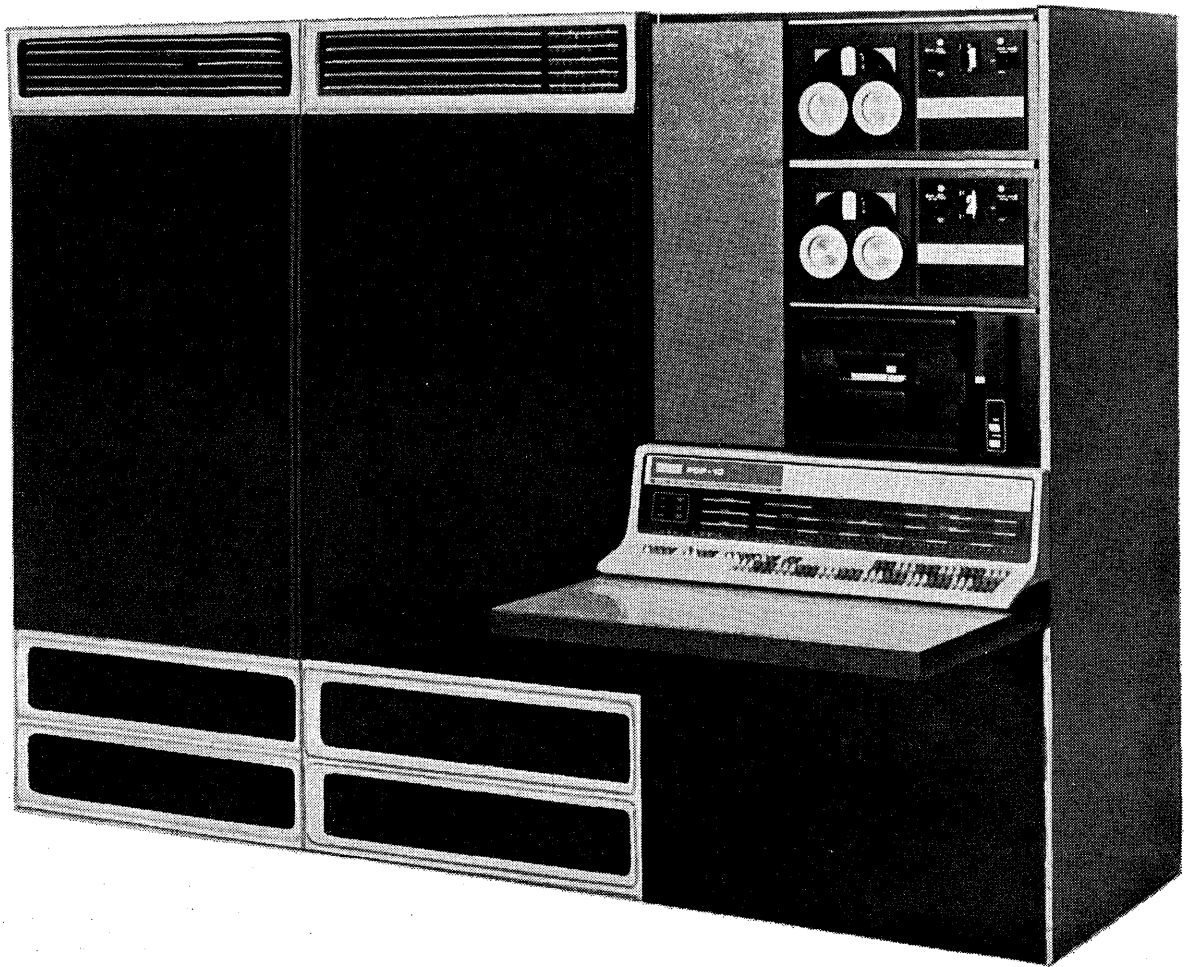
For your copy of this brochure, and immediate information on these new Digitally Controlled Power Sources, contact your local HP Sales Office, or write, Hewlett-Packard, New Jersey Division, 100 Locust Avenue, Berkeley Heights, New Jersey 07922. In Europe: 1217 Meyrin, Geneva, Switzerland.

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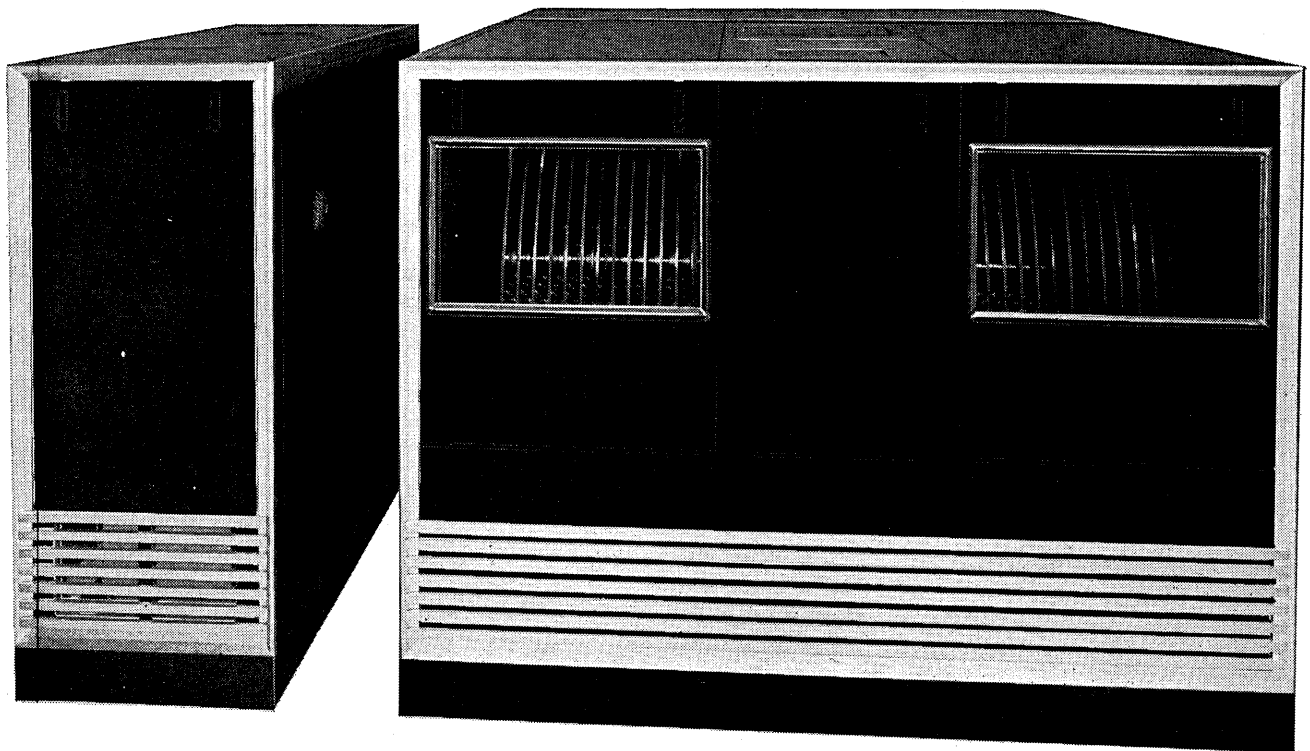
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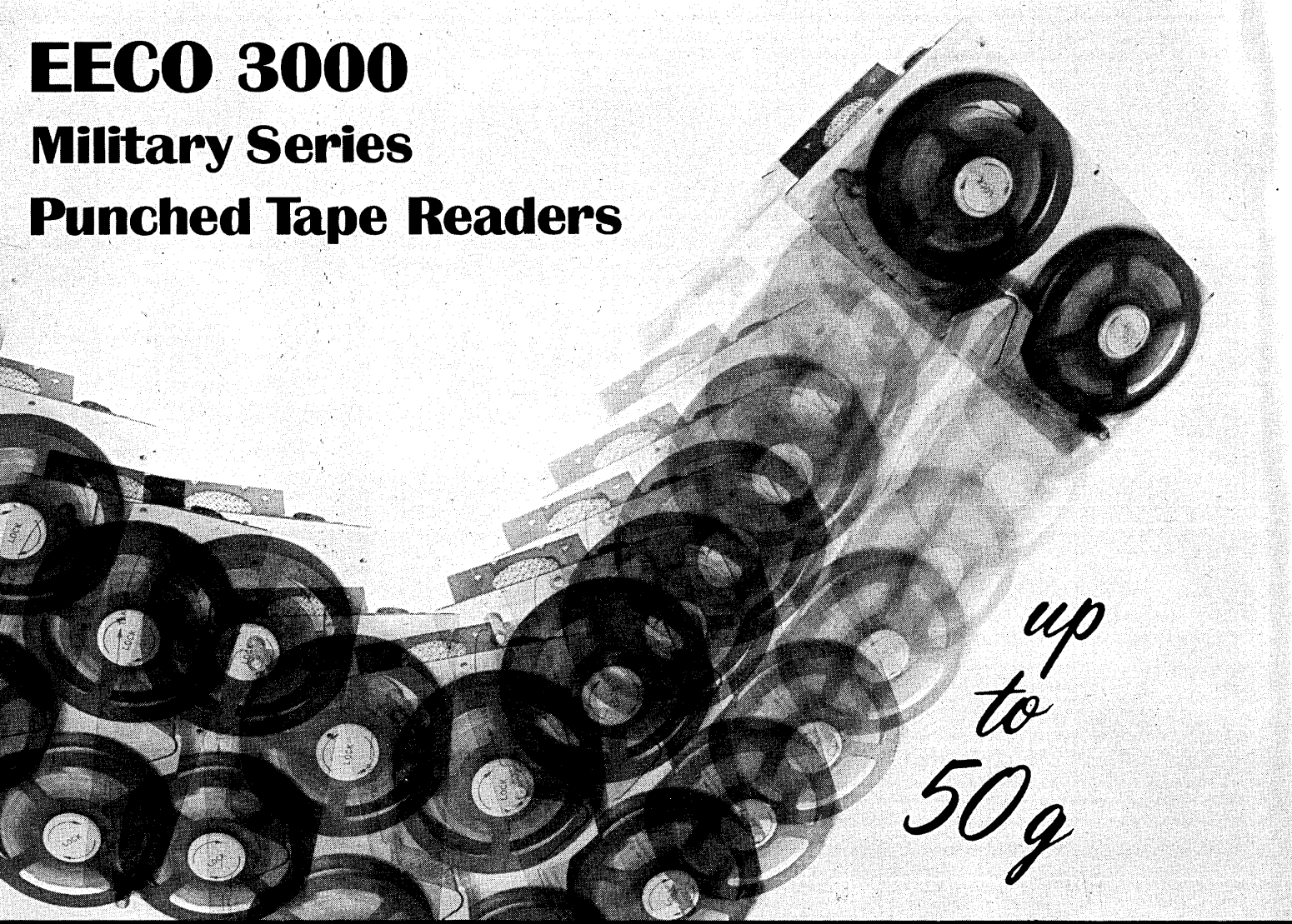
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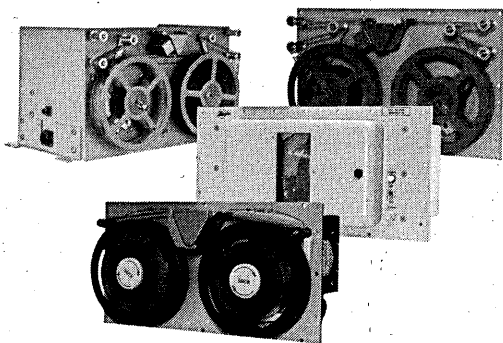
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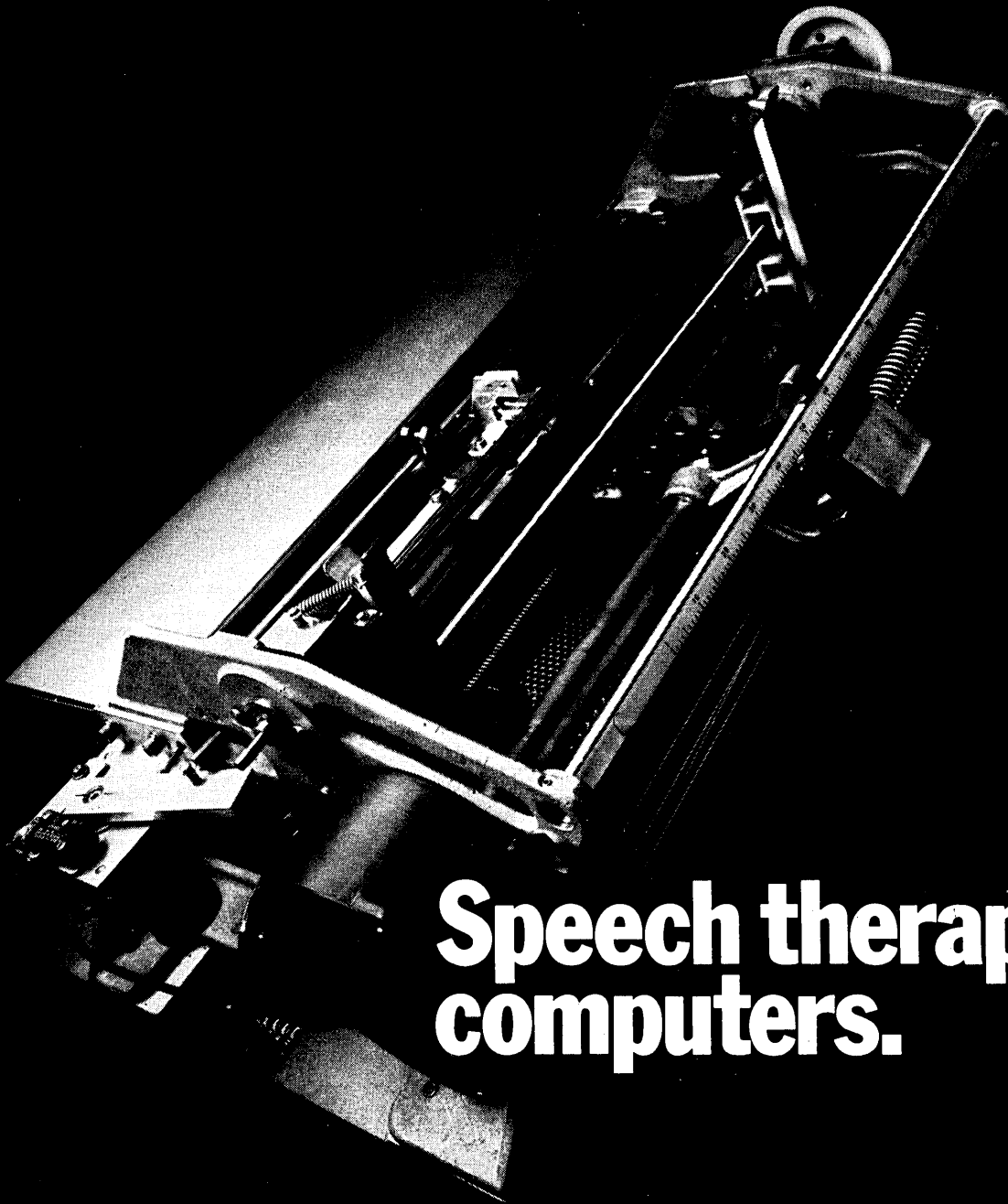


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CIRCLE NO. 24 ON INQUIRY CARD

This article describes a new technique for non-restrictive coupling within a computer system which increases transfer rates and reduces tailgate hardware.

A NEW TOOL IN COMPUTER BUSSING: THE MULTIPLEX DIRECTIONAL COUPLER

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A new tool for linking system components, now being used in the system 360/model 85, provides several significant advantages over usual bussing techniques, including increased transfer rates and configuration flexibility, improved dc isolation and noise rejection, increased loading and long-driving capability, and 50 percent reduction in "tailgate" hardware.

The device, known as a directional coupler, has long been used in microwave transmission. Since the coupler's operation depends upon the steepness of pulse rise and fall times, its use was not feasible for digital transmission before the achievement of nano-

second rates. In data processing systems, the directional coupler has been used, in the past, for such tasks as serial-to-parallel code conversion rather than for transmission among separate units.

Previously, such devices as central processing units and memories have been interconnected by drive and stub transmission lines. The drive lines are serially passed ("daisy-chained") through the various devices while the stubs are coupled to these lines through a T-connector. While such systems have been satisfactory, they have had certain disadvantages—aggravated by the newer data processing speeds—which the new coupling technique reduces or eliminates.

For one, fast rise and fall times are needed for high-speed transfer in the usual serially-connected system. Consequently, stub lines must be short. A common length is around six inches.

Another reason for such stub-length limitation is that information transfer speed is high relative to cable lengths, causing any reflection from a line discontinuity to degrade pulse waveforms. Two 90-ohm lines, meeting in a T, for instance, would give a 45-ohm junction—an intolerable mismatch. To prevent this, all receiving units must be placed near the main bus, each with a high-input impedance so as to produce a near-perfect transmission line, with minimum reflection at receiver stubs.

The short cable and stub lengths in the usual system—relative to the speed of data transfer—also impose additional configuration and packaging limitations. Since cabling is passed through the devices to the stubs in each device to provide input and output connections, pulses arrive at the devices at different times. As a result, layout often is fixed because of critical data transfer timing.

Howard Nick is an advisory engineer in large computer development at the IBM Laboratory in Poughkeepsie, N. Y. In addition to multiplex coupling, he has worked in such areas as circuits, logic design, power, cooling, diagnostic programming, and capacitor read-only storage.

Mr. Nick attended New York University and Brooklyn Polytechnic Institute, and has done graduate work in electrical engineering at Syracuse University and Rensselaer Polytechnic Institute.



Murray Bolt is a staff engineer in custom communication systems in IBM's development laboratory in Research Triangle Park, N. C. For the last several years, he has been applying microwave techniques to high-speed data communication, including the implementation of the directional coupled bus on the System/360 Model 85.

Mr. Bolt received a BS in Engineering Physics from the University of Manitoba, Winnipeg, Canada, and an MSEE from the University of Illinois.



The multiplex coupler consists of two parallel, printed-circuit strip lines sandwiched between two ground planes. These planes are inductively and capacitively coupled in such a way that the edges of fast pulses propagating along one line, produce positive and negative pulses in the other line. The lines are back-coupled: i.e., pulses propagate along the second line in an opposite direction to those on the first line.

The coupler can be used several ways to interconnect a number of data processing units such as memories, channels, or central processing units. In one application, a transmission line is connected to a driver in one of the data processing units. At each of the other units in the system, the transmission line is connected through a directional multiplex coupler to a receiver. The impedances of the couplers are matched to that of the line to minimize any reflections. The impedance of each coupler is not dependent in any critical manner upon the length of stub between the actual coupling and the receiver, thus avoiding any problem of stub-length limitation.

Two types of pulses (Fig. 1) can be used with the directional coupler: one has both leading and rear edges whose rate of change are fast enough to induce positive and negative pulses through the coupler; the second type of pulse has one operative edge and one edge whose rate of change is too slow to produce an effective pulse through the coupler. The first type of pulse produces an output across the coupler which duplicates at least the width of the driver pulse, while the second type can be used for control, turning a latch on and off for variable periods of time.

In another application, two drivers are arranged to propagate pulses along a transmission line in opposite directions, and a single receiver is coupled so as to be responsive to pulses traveling along the line in either direction. Such a system can be further combined with additional receivers and directional couplers that are responsive to pulses traveling in only one direction.

Information can even be sent down a single line in both directions at the same time (Fig. 2). This can be done because the coupler is directional; that is, the coupled pulse only appears in the backward direction and zero voltage is coupled in the forward direction.

The inherent flexibility of directional couplers permits driving long lines without changing driver or receiver circuits. This is done by tying together two couplers to produce twice the pulse width or height (Fig. 3).

THEORY OF THE MULTIPLEX COUPLER

The directional coupler is a strip-line device which has been well-described in the literature. Each consists of two sections: one connected on each end to a transmission line, the other connected between a stub line and a resistor.

A strip-line coupler is operated by the edge of a wave passing along one of the lines; the output follows the input if the rise or fall time is no more than twice the propagation time down the coupler. Advantage can also be taken of the lack of coupling from

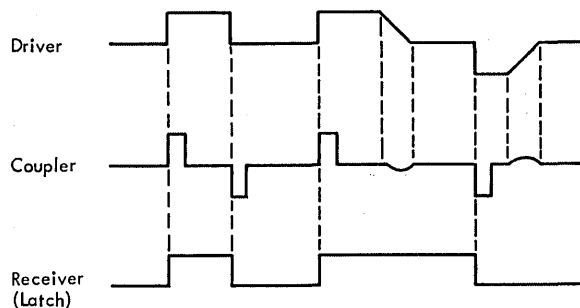


Fig. 1 Waveforms of a system using a directional coupler.

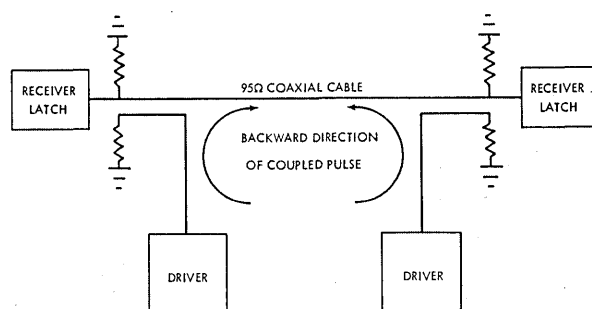


Fig. 2 Multiplex bus with capability of driving in both directions.

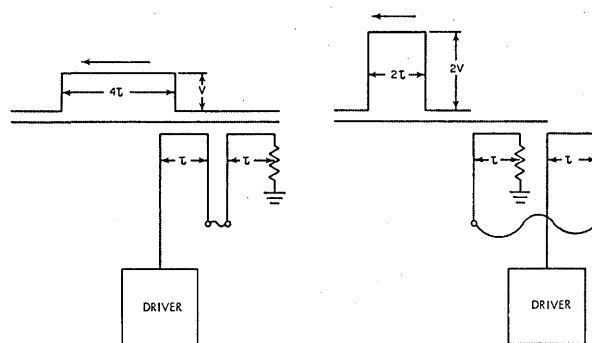


Fig. 3 Two couplers in series with long-drive capability.

slower pulses, using the coupler to screen out, for example, line transients arising from noise or power switching.

The width or duration of the pulse produced by the coupling is determined by the lengths of the two sections in parallel. The performance of the coupler is related to the impedances offered to signals on the transmission lines and the coupling ratio, which are determined by the width of the lines in the coupled region, the thickness of the lines, the distance between ground planes, and the relative dielectric constant of the material. The coupling between the lines alters

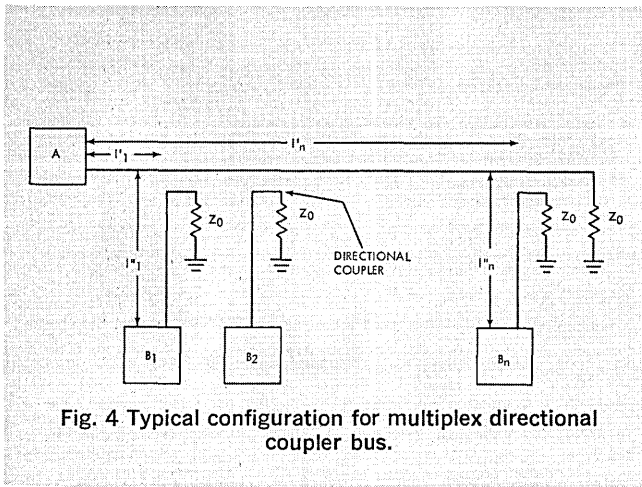


Fig. 4 Typical configuration for multiplex directional coupler bus.

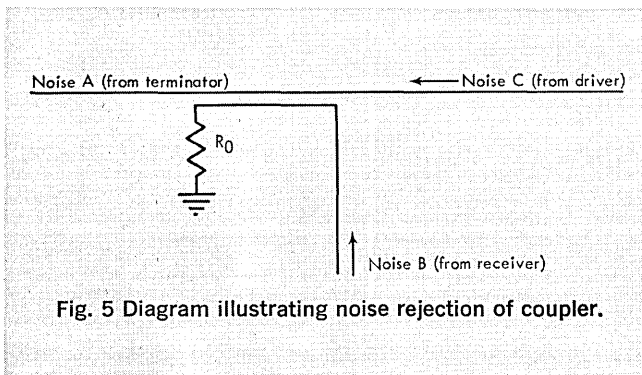


Fig. 5 Diagram illustrating noise rejection of coupler.

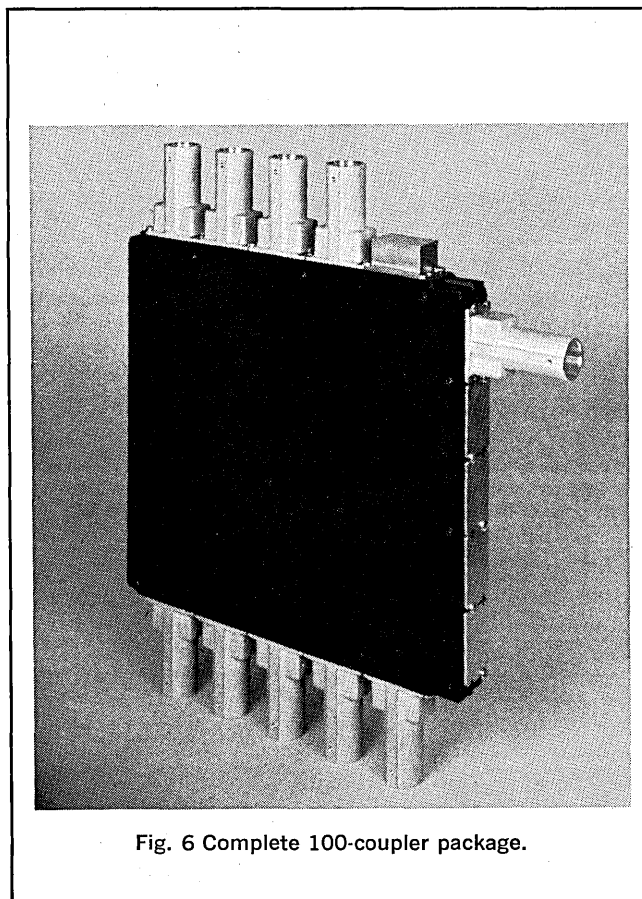


Fig. 6 Complete 100-coupler package.

their characteristic impedance—and their coupling; to compensate, their widths are made narrower at the coupling. A typical system configuration using multiplex couplers is shown in Fig. 4.

If Block A is a driver, then Blocks B_1 through B_n are receivers. Or, if Block A is a receiver, then Blocks B_1 through B_n are drivers.

The maximum length allowed through any coupler ($n = 'n + 'n$) will depend on a number of parameters:

- The type of coupler used (i.e., the coupling efficient and length).
- The number and type of couplers the signal must pass through.
- The driver output characteristics (minimum output swing).
- The receiver input characteristics (maximum threshold).
- The minimum driver on or off time.
- The frequency response of the cable being used.

The directional coupler used in the System/360 Model 85 has strip lines with a 95-ohm characteristic impedance. Each coupler will emit a minimum output pulse of 8 nanoseconds and a maximum output pulse dependent on the total line length and maximum loading.

ADVANTAGES

A number of the advantages of the directional coupler, compared to usual bussing techniques have already been mentioned: greater flexibility and transmission speed, better noise suppression, increased loading and long-driving capability, and hardware reduction. Two of these advantages—flexibility and noise rejection—will now be considered in more detail.

Because the coupler is matched to the transmission line, there is no reflection at the coupler junction. Thus, stubs do not have to be limited to any required length, and various devices can be located at different distances from a transmission line. Stub lines connected to couplers nearest to a driver can be made longer than more remote ones so that pulses can be received simultaneously by various system components. In addition, the effective transmission length through a system can be further varied by changing coupling ratios—thus, the amounts of energy transferred.

The long-stubbing capability eliminates the need to bring cables into and out of a machine in order to attach a driver or receiver circuit; instead, only one input—the connecting stub—is needed between the transmission line and each component for each driver and receiver. This minimum-path bussing makes installation more flexible and improves access time—two major disadvantages of traditional bussing techniques.

Noise suppression is obtained by both the coupling and directional characteristics of the coupler. Spurious signals traveling in the direction of transmissions are reduced by the attenuation characteristics of the coupler, since they would have to be as strong and have the same rise and fall characteristics as the driving voltage to be equally transferred. Any noise signals traveling in the opposite direction would be dissipated in terminating resistors.

If Block A in Fig. 4 is a driver and the input impedance to each receiver is high, the coupled signal will reflect totally from each receiver and again couple onto the main line. To appear as noise in another receiver, the signal must reflect from the driver and recouple onto a receiver line. The inherent isolation is therefore equal to $(k')^2$. The relatively low coupling factors used (.25 to .125) imply that the coupled output can be left open-ended or short circuited without affecting the main bus. Consequently, power-down problems do not exist; defective units can be removed by simply disconnecting input lines.

By maintaining a high input impedance at the receiver for both positive and negative input waveforms, a voltage-doubling effect is created which minimizes the necessary output voltage swing from the driver. Because the coupler is a matched device, noise coupled onto the main bus must pass through the couplers in order to upset the receivers, and noise coupled onto the connecting cables is a problem only when coupled in one direction. Noise spikes A and B (Fig. 5) will terminate in the line's characteristic impedance, while noise C will be reduced by the coupling ratio.

PACKAGING

Part of the directional coupler's uniqueness is in its packaging, which provides high density and minimum interference between couplers for the size of the package. Figure 6 shows a package containing 100 couplers complete with cable connectors, end-of-line terminator caps, and thin throw-away caps (placed on all ports to allow easy modification for use of less than 100 couplers). It is only 12 by 12 by 1.5 inches.

Each coupler package contains three circuit boards which are parallel and in register with one another (Fig. 7). Each of the outside boards contains 25 couplers which wind back and forth between input and output the number of times required to obtain the desired coupling length, density, and package shape. In the unit illustrated, each coupler is 30 inches long and makes three traverses of the package. The center board has the input and output connections for the couplers.

The coupler boards consists of an etched circuit sandwiched between two thin, copper ground planes. A feature of the packaging is the arrangement of the couplers in spaced groups so that identically-manufactured boards can be located opposite each other with minimum interference. Connections on one coupler board do not interfere with those on the facing board because the grouping of the couplers causes the lands on one to be opposite the spaces on the other. The distance from the land to the beginning of the coupling varies with each coupler in a package. These differences are compensated by varying the lengths of the winding loops, in order to prevent skewing the pulses from different couplers.

CONCLUSION

A number of advantages of the multiplex directional coupler have been cited: increased configuration flexi-

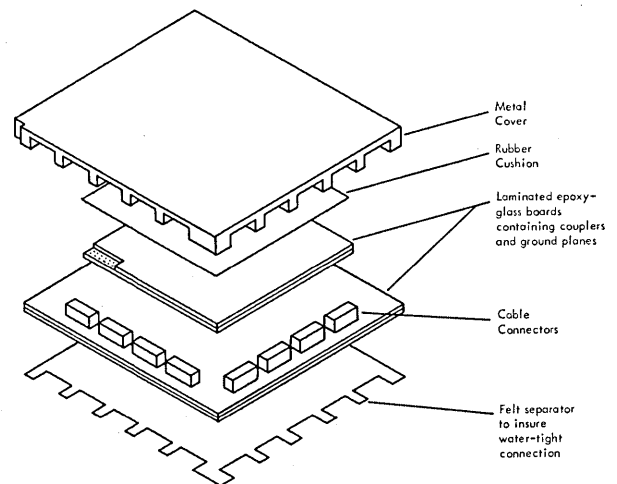


Fig. 7 One-half of a coupler assembly.

bility, noise suppression, faster data transfer, and a significant reduction in hardware. In addition, complete parity checking of information flowing along the bus can be performed without the use of additional logic circuits at either the sending or receiving end of a data transmission.

As computers become faster, directional couplers will become smaller and more easily packaged; as data processing systems and tele-processing networks become more complex, with increasing numbers of terminals and other I/O units, there will be an even greater need for non-restrictive coupling techniques such as the multiplex directional coupler.

Finally, the directional coupler can also add a new dimension to computer logic in other ways, in addition to interconnecting a number of data processing units: in adders, exclusive "OR" configurations, parity check mechanisms, and programmable clock generators—to name a few of the possible applications.

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Some of the ideas basic to the implementation of digital signal processing are discussed in this article, with emphasis on the application of various techniques involved.

DIGITAL SIGNAL PROCESSING

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Signal processing involves various operations used to extract a wanted signal from a background of other signals and noise and until quite recently, analog equipment was used almost exclusively to carry out these operations.

The recent increase in the use of digital signal processing has occurred for many reasons. These include:

1. The ability of digital systems to achieve a very large dynamic range. Each additional bit used in the calculations increases the dynamic range by 6 dB.
2. The flexibility of digital signal processors. Responses can be changed or bandwidths adjusted by modification of the numeric constants used in the processing.



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Bernard Thompson received a BS in Engineering from Imperial College of Science, London University. He is a Principal Engineer, on the staff of the Manager of the Digital Systems Department, Radar and Electronics Laboratory, Missile Systems Division, where he is presently conducting studies on digital pulse compression applications.

3. The compatibility of the output with the digital computations that are often required subsequent to the processor.
4. The ability to process very low frequency signals where analog elements would be of inconveniently large size.
5. The increase in ability to process reasonably high frequency signals. Here, the limits are set by the speed of A/D converters, and the expense of using paralleled digital hardware. The advent of integrated circuits with the resulting reduction in the cost of digital hardware has been of great importance in extending the frequency range.
6. The insensitivity of digital hardware to environmental conditions.

Because of the growth in the use of digital signal processing, the techniques used are becoming of more general interest. This article examines some of the ways to perform this processing.

Digital signal processing can be viewed as a digital simulation of analog operations, either by a general purpose or a special purpose computer. The special purpose computer can achieve operating speeds about two orders of magnitude faster than can a general purpose computer. The choice between them depends on considerations of the trade-off between speed and cost.

The digital simulation differs from the corresponding analog situation in that the data is represented as a sequence of discrete samples of the input signals. Because of this, difference equations and summations are more descriptive of the process than differential equations and integrations. Another consequence of this representation is that the signals must be band-limited, and sampled at least at the Nyquist rate if

unambiguous results are to be achieved. Fortunately, these requirements rarely cause difficulties.

The simulation can be set up in two distinctly different forms. The first form directly implements the difference equations which describe the system. This process is similar to system simulation on an analog computer. The second form uses a method analogous to the Laplace transform. The input data is transformed from time domain representation to frequency domain representation using a discrete Fourier transform. A discrete Fourier transform is quite similar to the Fourier series of the input data samples.

The first method is direct in that the contribution of each input data point can be traced through the system to the output. The second method is indirect because the individual input data points are combined during the transfer from time domain representation to the frequency domain, where they are not individually recognizable. Recently, a new algorithm, the fast Fourier transform (Reference 6 and 9), has significantly reduced the amount of computational effort required to make the transition between the time and frequency domain representations of the signal. This permits the system response to be shaped either in the time domain, or in the frequency domain. This freedom of choice permits the operations required to process the signal to be performed in the domain where they can be done with a minimum of effort. The net effect of this algorithm has been to permit a significant increase in the bandwidth of digital processors without the necessity for a corresponding increase in hardware speeds.

The fast Fourier transform operates on a batch of data samples rather than on a continuous set of samples as does the difference equation method. Fortunately, there are broad classes of practical problems in the signal processing field for which useful solutions can be generated using batched data.

The relative utility of these two approaches in any particular application depends on the amount of calculation required, and the applicability of batch processing. When the impulse response of the network extends over a small number of samples, the difference approach is more attractive. When the impulse response extends over a large number of samples, the transform approach is more attractive. In one of the examples examined below, the transform approach is more attractive even when the impulse response has a duration of only 16 samples.

DIFFERENCE EQUATION SOLUTIONS

One of the simplest of the difference equation signal processors is the two-pulse, or single-delay canceller used in radar MTI systems. Figure 1 is a block diagram of this system.

The operation of the canceller is analogous to that of an analog delay-line canceller, although it is not subject to the phase-delay variation of a delay line. In operation, a succession of samples of the input signal is supplied to the system. Each output is generated by forming the difference between the current samples and the corresponding previous sample

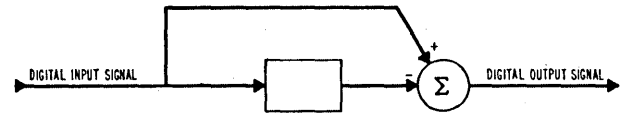


Fig. 1 Two-pulse canceller

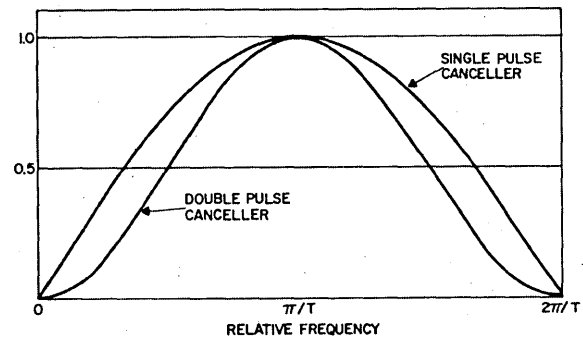


Fig. 2 Response of 2-pulse and 3-pulse cancellers

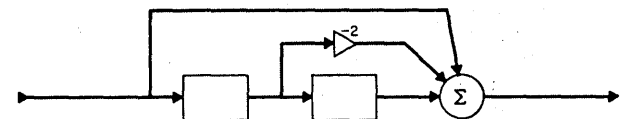


Fig. 3a Three-pulse canceller canonical form

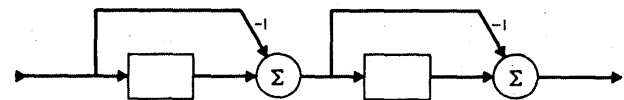


Fig. 3b Three-pulse canceller cascade form

which has been stored in the storage register. The frequency response of this system is given by

$$H(\omega) = k \sin \frac{\omega T}{2}$$

where

ω = the radian frequency of the input signal from which the samples were taken.

T = the time period between samples.

The response is plotted in Fig. 2. Above $\omega = 2\pi/T$ the response repeats periodically. This approach can be extended to include three pulses or two delays to give the system shown in two different forms in Fig. 3.

The three pulse canceller has a response given by

$$H(\omega) = k \sin^2 \frac{\omega T}{2}$$

This response is also shown in Fig. 2.

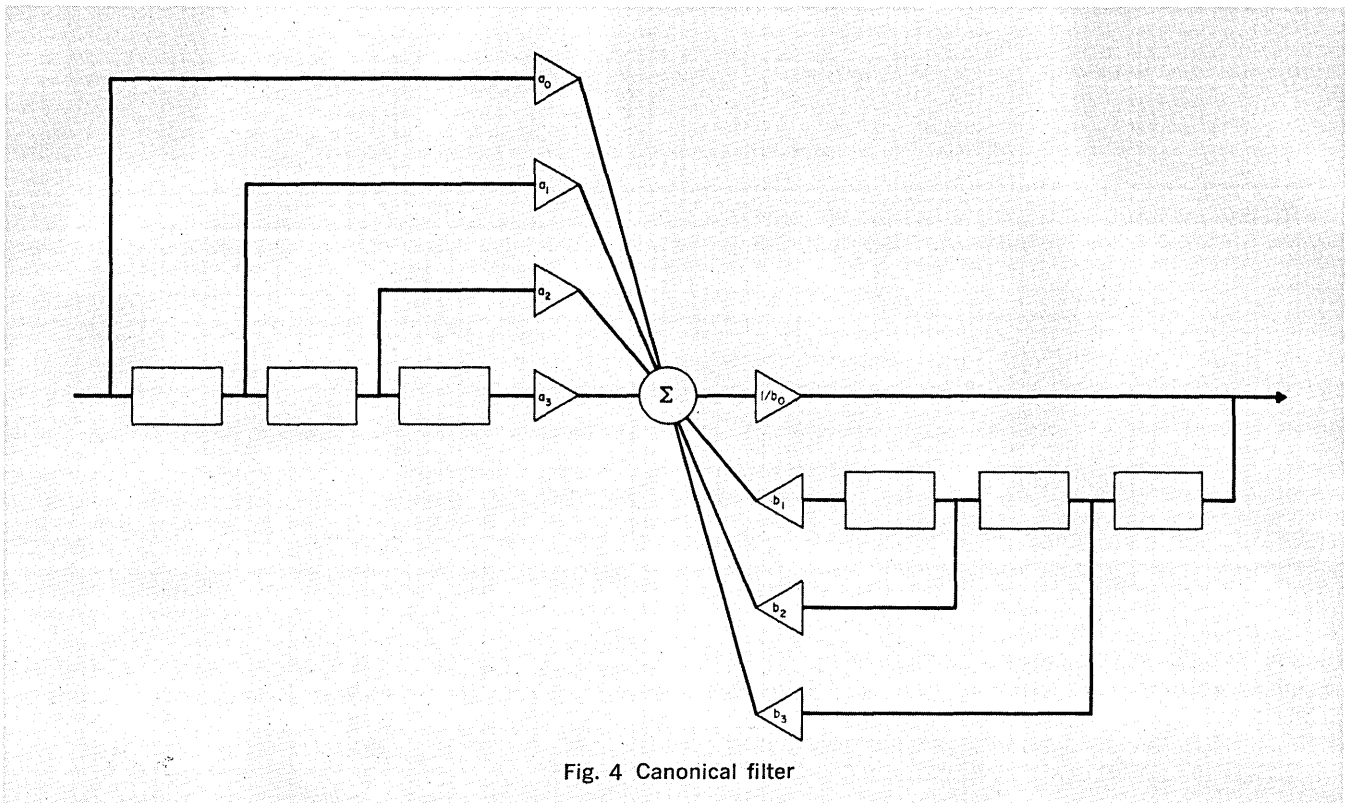


Fig. 4 Canonical filter

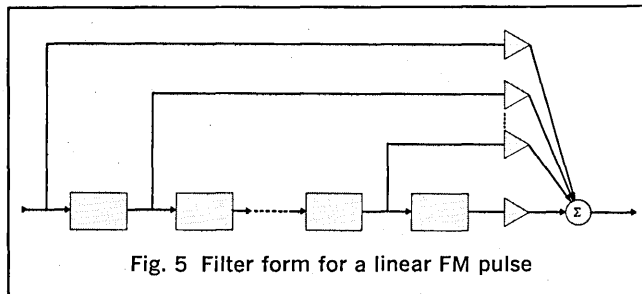


Fig. 5 Filter form for a linear FM pulse

The canonical form of filter can be extended in length and feedback paths added to produce the general form shown in Fig. 4.

In some instances the a_i multipliers can be regrouped and expressed in simpler forms so that multiplications can be replaced by additions. Further reductions can be achieved if the dc gain of the filter need not be controlled.

An example of such a filter¹ might be a low pass Tchebysheff filter having 0.5 dB ripple in the pass band from 0 to 100 Hz when operated with a 1000 Hz sampling rate. This filter can be realized using Fig. 4 with the multiplier constants listed in Table 1.

TABLE I		
Scaling Term		Value
a_0		0.025584
a_1	3 x	0.025584
a_2	3 x	0.025584
a_3		0.025584
b_0		1.604882
b_1		3.169418
b_2		-2.446283
b_3		0.728243

The filter when implemented using the multipliers of Table 1 has a gain of unity at dc. If gain at dc is

acceptable, the filter can be implemented using three multiplications and a moderate number of additions.

The required number of hardware multipliers will depend on the rate at which samples are gathered and the speed of the hardware multiplier. The filter of the example with its 1000 Hz sampling rate could have been implemented on a general purpose computer without any hardware multipliers. If the sampling rate were 10 MHz as it is in some radar applications, each multiplication in the filter would require its own hardware multiplier and each of these would operate at about the full speed capability of today's hardware.

The filter of this example is relatively simple. As the requirements on the frequency response become more severe, more delays and more multiplications would be required.² If the requirements necessitate a 10-pole filter rather than a 3-pole filter of the example, 22 entries would be used in the scaling table that corresponds to Table 1.

A characteristic of these filters that implement the difference equations is that they produce a time domain output from a time domain input. Indeed their operation can be viewed as a convolution of the input signal against an impulse response described by the scaling factors. It is quite possible to arrange the impulse response so that a matched filter results. For instance, a matched filter for a linear FM pulse could consist of a configuration of the type shown in Fig. 5.

A signal of this type that extended for N samples would employ a filter having $N - 1$ storage registers and would perform N multiplications to produce one output. For signals that have a large number of samples this requires a large amount of computation. A comparison between the amount of computation required for the difference equation method and for the fast Fourier transform method is given later in this article.

FREQUENCY DOMAIN MODELLING

The fast Fourier transform algorithm provides the tool necessary for the economic application of digital methods to the frequency domain. In order to understand how this comes about, the discrete Fourier transform must first be considered.

Discrete Fourier Transform

The processing operations in the time domain use discrete samples of the time function. Suppose now discrete samples of the frequency spectrum are considered also. If the time function $f(t)$ is represented by N samples $f(nT)$, and similarly if the spectrum $F(\omega)$ is represented by $F(k\Omega)$, where n and k are integers between the limits $0 \leq n \leq N - 1$, and $0 \leq k \leq N - 1$, the discrete Fourier transform is defined by,

$$F(k\Omega) = \sum_{n=0}^{N-1} f(nT) e^{-jk\Omega nT} \quad (1)$$

where T is the sampling interval in the time domain, Ω the sampling interval in the frequency domain, and $N\Omega T = 2\pi$.

The expression (1) is completely discrete, both in time and frequency, and is therefore suitable for digital computation. It is important to note that because of this sampling, the functions are represented as periodic functions, both in time and frequency. Other than this, the properties of the discrete Fourier transform parallel those of the continuous Fourier transform. Thus, the properties of frequency selectivity, linearity, and convolution all have their counterparts in the discrete transform. Further, an inverse discrete Fourier transform exists that maps a discrete Fourier transform back into the sequence from which it was computed. It is given by

$$f(nT) = \frac{1}{N} \sum_{k=0}^{N-1} F(k\Omega) e^{+jnTk\Omega} \quad (2)$$

which differs from (1) only by a scale factor and the sign of the exponential. This corresponds to the inverse Fourier transform of a continuous function.

The Fast Fourier Transform ^{6, 9}

The direct evaluation of equation (1) requires N^2 complex multiplications and additions and for a moderately large N the cost in computer time would be prohibitive. Recently, however, algorithms have become available that reduce the number of operations required, particularly when the value of N is highly composite. For example, when N is a power of 2, the fast Fourier transform algorithms require a number of computations proportional, not to N^2 , but to $N \log_2 N$. Thus for $N = 1024 = 2^{10}$, there is a computational saving of 99 percent.

These dramatic savings account for the large upsurge of interest in processing via the frequency domain.

Fast Convolution or Correlation ^{7, 8, 10}

The convolution operation is used very frequently in signal processing applications. Since the convolution

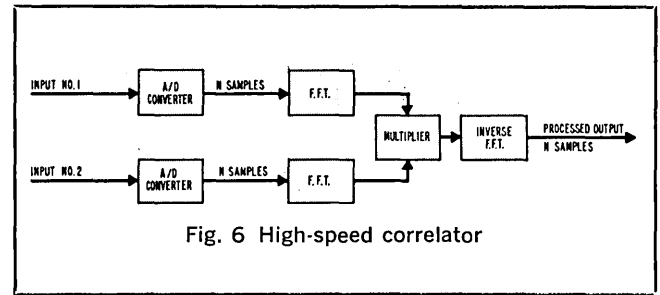


Fig. 6 High-speed correlator

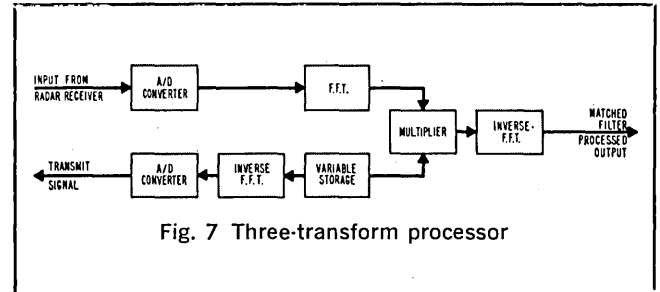


Fig. 7 Three-transform processor

of two functions corresponds to the multiplication of their Fourier transforms, the convolution operation can be exchanged for three Fourier transformations and a multiplication.

Figure 6, which illustrates the arrangement in more detail, shows two N -sample inputs, each with its own discrete Fourier transform operation, a multiplication (point by corresponding point) of the two discrete Fourier transforms, and an inverse discrete Fourier transform operation. Note that the inverse transform uses the same algorithm; only the sign of the complex exponentials has been changed. Furthermore, since correlation and convolution are related by a change in the sign of the time variable, the system can handle correlation equally as well. The N output samples represent the results from the convolution of the two input sample series.

The application of various modifications of this arrangement to typical signal processing problems encountered in radar is discussed in the next section.

SPECIFIC APPLICATIONS

Three examples have been chosen to illustrate the frequency domain method. Although one particular artifice has been introduced in each example, any one of them can be used in all of the systems described.

Three-Transform Application—Flexible Matched Filter

In many signal processing applications, the use of a matched filter yields optimum results.³ A matched filter has a frequency response which is the complex conjugate of the spectrum of the input signal.

Because the requirements of system characteristics such as detection capability, clutter rejection, range resolution, range rate estimation, etc., usually conflict, modern radar systems are often called upon to work in many different modes—the emphasis on particular signal parameters changes from mode-to-mode in order to optimize the performance in each one. A suitable processor can be implemented by a slight modification of the general processor illustrated earlier. This variation is shown in Fig. 7. Suppose

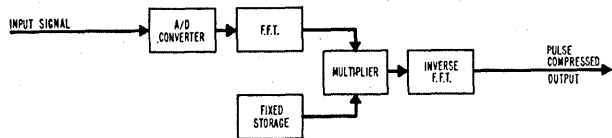


Fig. 8 Two-transform processor

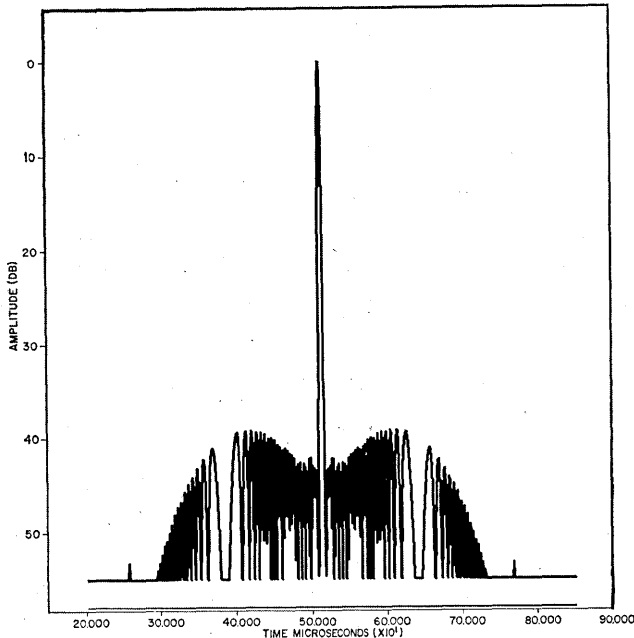


Fig. 9 Compressed pulse output, Hamming weighting

that the radar signal has a large time-bandwidth product, i.e., the transmitted signal has a large bandwidth (for good resolution) and a long time duration (in order to increase the energy without increasing peak power, or to provide good range-rate resolution, or both). Typical examples of such signals are the linear FM sweep and the series of discrete coded waveforms.⁴ The bandwidth of the signal governs the sampling rate, and the duration controls the minimum batch size. Samples are taken of the received signal, at a rate compatible with the bandwidth, and in sufficient number to span the range interval to be examined. As noted later, this batch size is usually made somewhat longer than the minimum size. Indeed, it is a characteristic of this method of processing that long batches can be processed with just one pass through the processor yielding information for all ranges at once. These samples undergo a discrete Fourier transformation and yield samples of the received signal spectrum, which are then multiplied point by point by a set of numbers held in storage. (This set of numbers represents the response of a matched filter, which has been computed in

advance.) The result thus corresponds to the spectrum of the signal after being filtered, and a further inverse discrete Fourier transform brings it back into the time domain, where there is a one-to-one correspondence between the position of the processed target echoes and their position in the original sequence of the received signal.

The transmit waveform is derived from the set of numbers held in storage by means of an inverse discrete Fourier transform (heeding the required conjugate response characteristic) and a digital-to-analog conversion operation. Since the received signal is a delayed and attenuated replica of the transmit waveform, the operation is indeed that of matched filtering. By changing the set of numbers held in the variable storage, any desired waveform characteristic can be achieved on demand.

To illustrate the economy of effort afforded by this method of operation, suppose that the sampling rate has been chosen to be compatible with the system parameters, with one sample per range resolution element. Further, suppose there are n samples within the duration of the transmit waveform (or in the impulse response of the matched filter, which is the same thing) and suppose that the range interval to be examined contains N samples. If processing is carried out by a correlation in the time domain, n multiplications are required per range resolution element. There are $(N - n + 1)$ independent elements contained in the N samples so that the total number of multiply operations required is $n(N - n + 1)$. In the equivalent frequency-domain processing, there are two N -point discrete Fourier transforms and an N -point multiplication which require $N + N/2 [\log_2 (N - 3)] + 2$ multiply operations for one form of the fast Fourier transform algorithm. It can readily be verified that the transform method is much more economical. For example, if the batch size is $N = 2n$, even such a small value of N as 64 requires 1056 multiplications for correlation to produce data for 33 range resolution elements. The corresponding number of multiplications in the transform method is 162. Even more striking savings are realized with larger batch sizes.

Two-Transform Application—Processing for a Known Signal

If the signal to be detected is known a priori, the previous system can be simplified as shown in Fig. 8. The same operations are carried out on the received signal, except that the multiplier stage operates with input from fixed storage.

As an example of a system which operates with a large time-bandwidth product, consider a linear FM signal of 256 μ s duration and frequency sweep of 0.5 MHz. The resolution of this system is 2 μ s; that is, the matched filter output is a compressed pulse of 2 μ s duration. Such a system has been simulated on a digital computer, using a sampling rate of 1 MHz. A range interval of 1024 μ s was selected, so 1024 samples were taken, with 256 samples representing the

received signal that was arbitrarily chosen to fall in the center of the interval. After processing as described earlier (1024 point FFT, 1024 point multiplication by the conjugate spectrum function, followed by a 1024 point inverse FFT), the result was plotted as shown in Fig. 9. The peak occurs at the center of the interval corresponding to the input signal time delay and shows clearly the result of pulse compression. This plot includes the effect of another operation that can be incorporated without any increase in complexity (a slightly mismatched filter to improve the sidelobe response). The output of the normal matched filter closely approximates the $(\sin x)/x$ form, which has high sidelobes, the largest of which is some 13.5 dB below the mainlobe. Thus, a small target could be obscured by the sidelobes of a larger target. It is known that such sidelobes can be reduced by application of a spectrum weighting function. A Hamming weighting function was chosen to illustrate the method and applied by modifying the conjugate spectrum function suitably so that the sidelobes are reduced to about 40 dB, below the main response, as shown in the figure.

One-Transform Application—Spectral Analyser

Finally, the system may be reduced to just one fast Fourier transform box (Fig. 10), which corresponds to a spectrum analyser. If N is the number of samples of the time function used and T is the time between samples, then NT is the input time duration and the fast Fourier transform box can be regarded as giving N filters spaced $1/NT$ apart. The response shape of each filter corresponds to the function $(\sin Nx)/\sin x$, so that the zeroes of one filter fall on the maxima of the other, and vice-versa.

If required, the sidelobe response can be modified in a manner similar to that described in the previous section by the addition of a multiplier box so that a weighting function may be used. Figure 11 shows the response of one filter from a bank of 256 when a Taylor weighting function⁵ of 30 components and a design sidelobe ratio of 80 dB was used.

SUMMARY

In this brief survey, some of the ideas basic to the implementation of digital signal processing have been discussed. These systems operate on samples of the input signal and can be considered in two main classes. Historically, the first method to be used employed difference equations and summations with a time domain representation, but the recent advent of fast Fourier transform algorithms enables processing to be carried out economically in the frequency domain. Several examples of each approach were chosen to illustrate these concepts.

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Fig. 10 One-transform processor

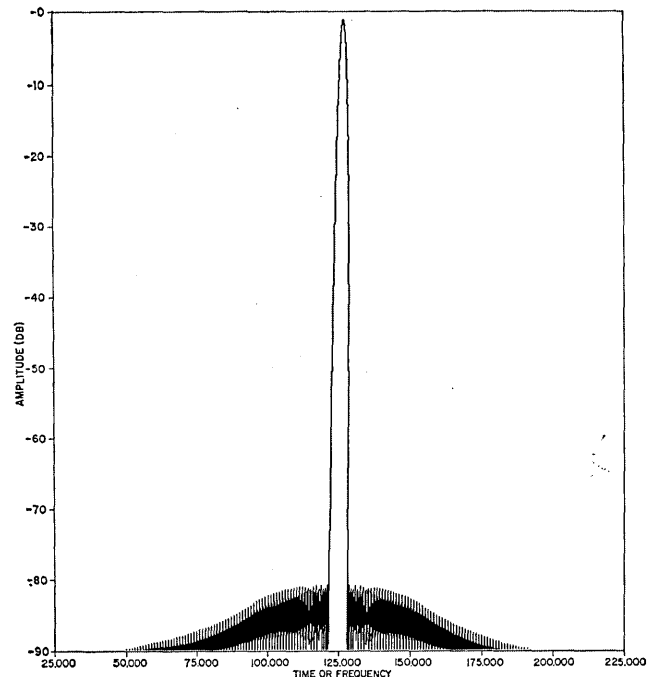


Fig. 11 Spectrum analyser filter response

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Display processing subsystems which serve as a link between the computer and other subsystems and devices found in the computer data display are described in this article.

DISPLAY PROCESSING SUBSYSTEMS FOR COMPUTER DATA DISPLAYS*

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In the modern computer data display, computer data is converted into the signals required to provide visual data on a cathode ray tube. This data conversion process involves the use of special purpose subsystems and devices within the display system.

The first step in the conversion of computer data into display data is accomplished in the "display processing subsystem." Here, the computer input data is processed and put into the form required by the other display subsystems. Also, the display processing subsystem accepts data entry device data and sends it to the computer.

The subsystems and devices which may be found in a typical computer data display are diagrammed in Fig. 1. The block diagram includes: (1) a CRT, (2) a Z-axis subsystem, (3) a deflection subsystem, (4) a character generation subsystem, (5) a line generation subsystem, (6) data entry devices, (7) data entry subsystems, and (8) the display processing subsystem.

The presentation of data on the CRT is controlled by the deflection and Z-axis subsystems. Deflection subsystems are used to control the direction of the electron beam as it passes through the tube and onto the viewing screen. The beam is controlled horizontally and vertically, that is, in the X- and Y-axes

of a rectangular coordinate system. The intensity of the beam, and therefore the brightness of the visual presentation, is controlled by the Z-axis subsystem. The main components of these subsystems are X and Y (horizontal and vertical) deflection amplifiers and the Z-axis (video) amplifier.

The conversion of computer-originated data into driving signals for the deflection and Z-axis subsystems are provided by the character and line generation subsystems as well as by the display processing subsystem. Under the control of computer data, character generation subsystems generate the necessary signals to produce character presentations on the CRT. These presentations may include symbols and alphanumeric (alphabetic and numeric). Line generation subsystems provide the signals required to produce line presentations (sometimes called vectors).

Data entry devices are used to transmit data to the computer via the display system, resulting in some modification of the display presentation. These devices include alphanumeric keyboards, function switches, line data entry devices, and pointer devices. Pointer devices include the light pen, track-ball joystick, voltage pen, and the ultrasonic pen.

Data entry subsystems are used to produce non-computer-controlled data on the CRT. These subsystems may be used to present maps, grids, or special patterns. Included in these subsystems are those that produce a TV raster as a background for computer-generated data or project a slide as background data on the CRT screen. Another type of background might be the presentation of a radar display.



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DISPLAY PROCESSING SUBSYSTEMS

Display processing subsystems provide the input-output interface with the computer in a computer data display system. This subsystem accepts computer data, processes it, and then puts it into the form required to drive the deflection, Z-axis, character generation, and line generation subsystems. Display processing subsystems also accept data from the data entry devices, process this data, and then transmit it to the computer. This two-way communication function is accomplished by the use of logic, storage, and digital-to-analog conversion circuits.

The major sections of display processing subsystems are computer interface logic, computer data storage, and data position generation. Computer interface logic consists of logic circuits which are used to transfer data into and out of the display system. Computer data storage is accomplished by memory circuits which store the computer data for use by the display system. Data position generation circuits are used to convert computer-originated position data from a digital to an analog voltage.

The configuration of the display processing subsystem depends on the relationship between the computer and the display system. There are two basic computer-display relationships which are employed in computer data displays. In one arrangement the "stand alone" display station interfaces directly with the computer and no additional hardware is required in order to present data. In the other arrangement, the multistation display, the computer interfaces with a display control unit which then controls the presentation on all display stations tied to it. Figure 2 shows a block diagram of a "stand alone" display station and Fig. 3 shows a typical multistation display system.

Stand alone display stations contain their own Z-axis, deflection, character generation, line generation, and display processing subsystems along with data entry devices. The display processing subsystem contains computer interface logic, computer data storage, and data position generation circuits all within the display station. In this way each of these display stations can truly stand alone and provide visual data when operated with a computer.

In a multistation configuration, the display processing subsystem is divided between the display control unit and display stations. Figure 3 shows one variation of the many possible multistation configurations. In this figure the display control unit contains the computer interface logic and computer data storage sections of the display processing subsystem. The character generation and line generation subsystems are found in the display station.

When the display control unit contains a single character generation and line generation subsystem along with a single computer data storage section, only one display station can be serviced at a time. Therefore, the maximum number of display stations which can be serviced by a single display control unit depends on the required refresh rate and the time required to present data on each station. The total display time depends on the character and line generation times, the data positioning times, the time required to communicate with the computer, and the

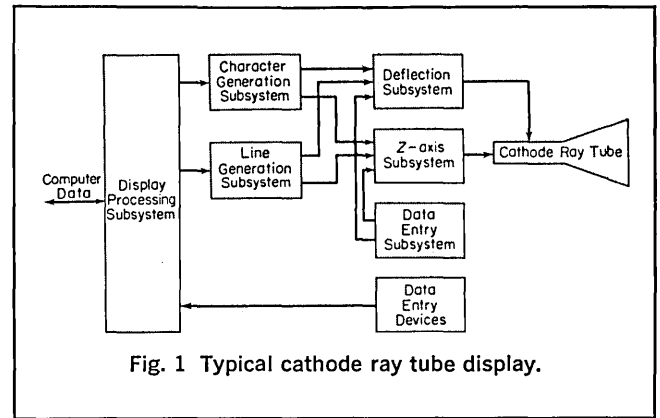


Fig. 1 Typical cathode ray tube display.

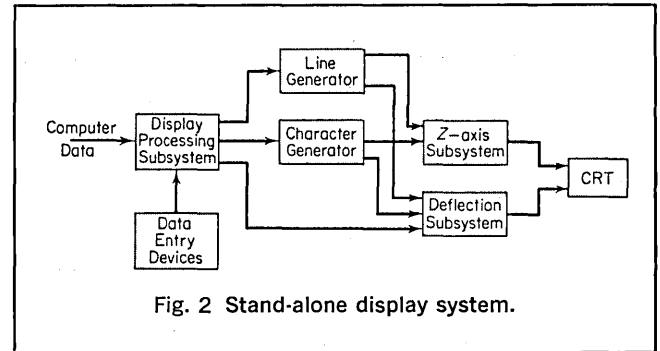


Fig. 2 Stand-alone display system.

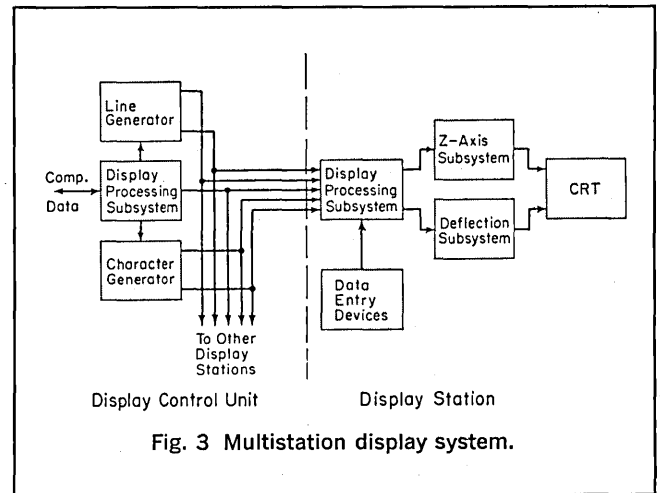


Fig. 3 Multistation display system.

time for data to be stored and retrieved from the computer data storage section. Another factor which influences the display timing is the amount of time which must be allowed to send data from the data entry devices through the display control unit to the computer.

In another multistation arrangement, each display station contains its own character and line generator as well as the computer data storage and data position generation sections. In this case the display control unit acts as a multiplexer and contains the computer interface logic section along with the necessary switching circuits to route computer data to each of the display stations. In this way each station can simultaneously provide its own presentation independent of other display stations. Computer data storage sections of each of these display stations not only store computer data but also refresh it, providing flicker-free presentations.

COMPUTER INTERFACE LOGIC

Computer interface logic within the display processing subsystem contains the necessary logic devices to accept computer input data, process it, and then route the resulting signals to the computer data storage and data position generation sections. This logic also contains the devices necessary to transmit data from the data entry devices to the computer. This logic consists of decoding circuits, registers, line drivers and line receivers. When the logic levels of the display system do not match those of the computer, level translators must also be used.

Not only does the design of the interface logic depend on the computer being used, it also depends on whether serial or parallel data transfer is used. With serial data transfer, a single pair of lines transfer data between the computer and the display system. This is the case when telephone lines are used to connect a remote display to a computer in a time-shared system. However, telephone lines permit data transfer rates of 150 to 4800 bits per second. On the other hand, parallel data transfer uses a multiplicity of lines, but they can transfer data in excess of 500,000 bits per second per line.

For serial data transfer, received serial data is converted to a parallel data format by the display processing subsystem. A parallel data output is required because the deflection and intensification of the CRT are parallel operations. In the display processing subsystem the computer interface logic receives the serial data and then passes it along to the computer data storage section. The serial-to-parallel conversion usually takes place in the output of the computer data storage section. When data is to be transmitted, computer interface logic converts the outgoing data to a serial format for transmission to the computer.

In parallel data transfer, incoming data is received in the computer interface logic. Parallel data words (ranging from 8 to 36 bits) are decoded in the computer interface logic and sent to the computer data storage section. In this case, the computer data is already in a parallel format so no data conversion is required. When parallel data is transmitted, the computer interface logic drives the data lines going to the computer.

COMPUTER DATA STORAGE

Computer data storage in the display processing subsystem can be used merely to store display data or it can also be used to refresh the display presentation. In a conventional CRT, the light output decays after electron beam impact. Therefore, data placed in the screen must be continually repeated, or refreshed, in order to maintain a flicker-free appearance. When the display system contains its own refresh memory, only one cycle of computer data is necessary to store an entire presentation. The circuitry associated with the refresh memory then takes the stored computer data and refreshes the display. If the display system has no refresh memory, the display is refreshed by the com-

puter with a continuous recycling of data. In many cases computer refresh is undesirable because of the excessive time loading on the computer. By using an internal refresh memory the computer need only service the display to update the presentation.

A number of computer data storage techniques are employed in display systems, including flip-flop registers, magnetic core memories, delay lines, shift registers, and magnetic drum memories. These techniques vary according to the time required to store and retrieve data, storage capability, complexity, and cost.

The set-reset flip-flop is the simplest storage technique; it can be used when parallel data stored in a display system is refreshed directly by a computer. In a typical sequence, computer data enters the display system via the interface logic and is stored in the flip-flop register. After the display presentation is completed, the register is reset and the next data word is entered, and the cycle continues.

The magnetic core memory is one form of memory which is used when stored information is refreshed within the display. In this situation, a block of computer data is stored in the memory and continuously refreshed by sequentially reading out data from the memory. New data can be stored either by erasing the entire memory and then inserting a new block of data, or by selectively erasing specific memory addresses and re-inserting new data. Compared to other computer data display storage techniques, the magnetic core memory offers the fastest data storage and retrieval times of large volumes of data.

The delay line memory is used in display processing subsystems where, for the amount of data to be stored, it is less costly than magnetic core storage. A typical delay line storage system consists of a delay medium, an arrangement for inserting data into the medium, and an arrangement for recirculating the data through the medium once it has been inserted. Delay mediums used include glass, quartz, or magnetostrictive materials. This type of storage is usually found in alphanumeric displays where the storage requirements are less than 2,000, 8-bit characters.

MOS or discrete component shift-registers can be arranged to operate as a memory in a manner similar to that described for the delay line memory. That is, data is inserted serially, propagated through the shift register, and then recirculated. Storage in the shift register is provided by individual flip-flops and propagation of the data is accomplished by means of the clock pulses. In the delay line, signals are applied to the input of the line and the delay medium itself produces the storage properties.

The magnetic drum is used in some display systems where low cost storage of a large amount of computer data is required. One way that a magnetic drum memory can be used is to have the drum rotate at the refresh rate of the display. Bits corresponding to computer data are then stored on the drum tracks and are retrieved from the drum as it rotates. Thus, parallel data lines corresponding to stored computer data are obtained from the drum which are refreshed at the drum rotational rate.

DATA POSITION GENERATION

The positioning of computer data on the screen of a CRT is usually accomplished by means of a random scan, textual scan, or raster scan. With random scan, computer data is placed at random positions on the CRT screen. In the textual scan mode, data is positioned incrementally, in an ordered fashion, one line at a time. With raster scan a fixed pattern of horizontal lines is presented on the CRT and data is obtained by intensifying the CRT beam at the proper times.

When random scan is employed, the computer specifies the X and Y viewing screen coordinates where data is to be presented. This position data is obtained by the display system in the form of an X and a Y digital code. A position code of 10 bits both for X and Y provides a capability to present data on a 1,024 by 1,024 matrix. Positioning of the CRT beam is accomplished by converting the digital data into analog voltages which are then applied to the respective X and Y deflection amplifiers. The conversion process is provided by the use of D/A converters.

Textural scan is usually used only for the presentation of alphanumeric data in a "page print" format. Positioning for this format is accomplished without the use of specific computer-derived X and Y position data. Instead, positioning of the CRT beam is derived from internally generated X and Y position signals. With this method of positioning, the CRT beam moves across each line and from line-to-line and passes through every position where alphanumeric data may be presented. By ordering the alphanumeric data in the sequence corresponding to its location on the screen, a presentation is obtained without specific position information.

When raster scan is used in the display system, position, character, and line generation data are converted from a digital to a video format. Data position generation is produced by the circuitry required to form the raster. The positioning of data on the CRT is obtained by intensifying the CRT beam at the proper times, producing characters or lines as a series of closely-spaced dots.

DISPLAY PROCESSING SUBSYSTEMS FOR ALPHANUMERIC, GRAPHIC, AND SITUATION DISPLAY SYSTEMS

CRT computer data displays may be placed in three general categories: alphanumeric, graphic, and situation displays. The alphanumeric display provides a formatted, typewriter-like presentation. In the graphic display, lines may be presented along with randomly placed alphanumerics and symbols. A situation display contains alphanumerics, symbols, and lines along with some form of background information.

Display processing subsystem configurations vary according to the type of display system. A comparison of display processing subsystems used in alphanumeric, graphic, and situation display systems will be

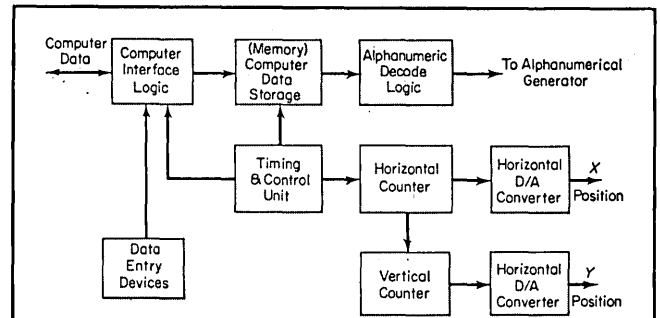


Fig. 4 Block diagram—Display processing subsystem, alphanumeric display.

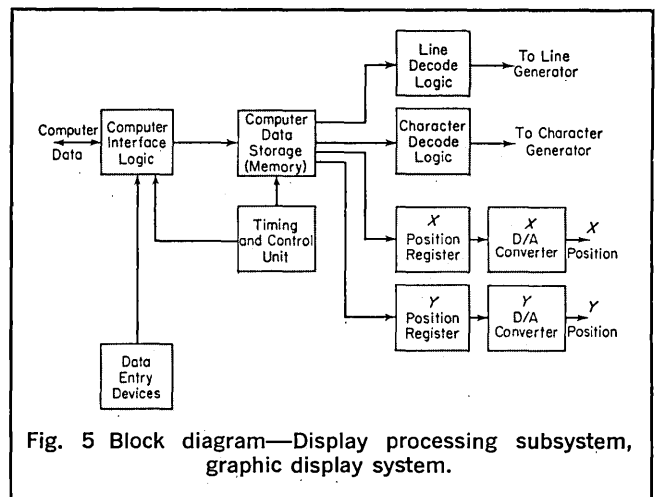


Fig. 5 Block diagram—Display processing subsystem, graphic display system.

presented here. In these examples, either stand alone or multistation arrangements may be used, but will not be specifically considered.

Figure 4 shows a block diagram of the display processing subsystem for an alphanumeric display. The computer interface logic is used to transmit data to the computer from the data entry devices or to accept computer data. When computer data is received, it is entered into the memory. The timing and control unit controls the insertion and extraction of alphanumeric data from the memory as well as incrementing the horizontal counter. Alphanumeric data taken from the memory is applied to the alphanumeric decode logic and the decoded data is sent to the alphanumeric generator. The horizontal counter drives its D/A converter and also the vertical counter. DC outputs from the horizontal and vertical D/A converters provide the positioning voltages for the deflection subsystem.

The display processing subsystem for a graphic display system is shown in Fig. 5. The computer interface logic is used to send data entry commands to the computer or to receive computer input data. When computer data is obtained, it is stored in the computer data memory. This memory is used to store character data, line data, and X and Y position data.

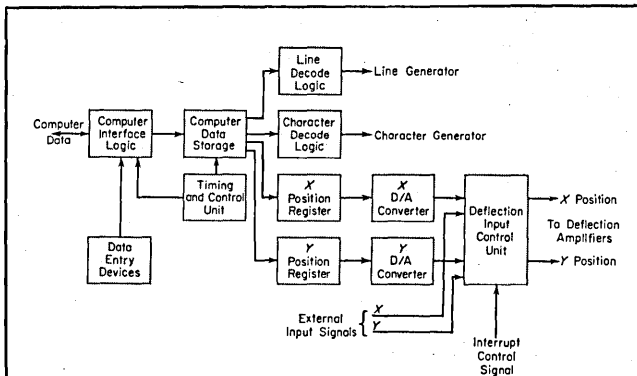


Fig. 6 Block diagram—Display processing subsystem, situation display.

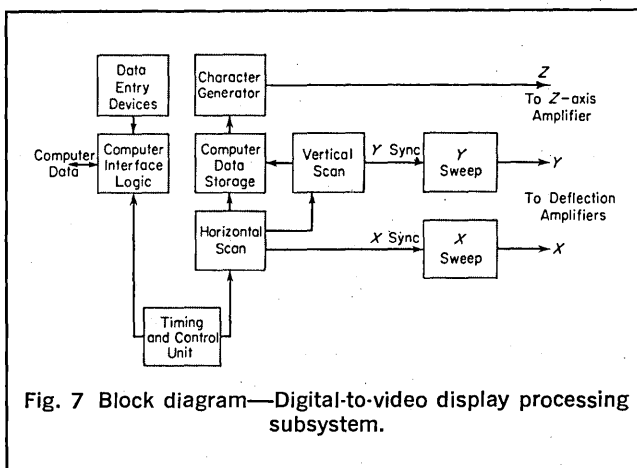


Fig. 7 Block diagram—Digital-to-video display processing subsystem.

The timing and control unit controls the data going into and out of the memory. The character decode logic processes the stored data and delivers alphanumeric and symbol command data to the character generator. Line data is processed in a similar manner and applied to the line generator and X and Y position data is stored in the respective position registers. DC output voltages are obtained from the X and Y D/A converters whose input is derived from the position registers.

Figure 6 shows the display processing subsystem for a situation display system. This subsystem is similar to that of the graphic display of Fig. 5 with the addition of a deflection input control unit. This unit is used to control the position data applied to the X and Y deflection amplifiers. X and Y external input signals are also applied to the deflection input control unit along with an interrupt control signal. This control signal is used to normally allow external input signals to go to the deflection amplifiers. When computer data is received, the external signals are interrupted to display computer data. When the computer data presentation is concluded, the external input signals are once again applied to the deflection amplifiers. Using a single-gun CRT with this time-shared technique provides a display which appears

as though both the fixed background (obtained from the external input signals) and the dynamic computer data are superimposed.

DIGITAL-TO-VIDEO DISPLAY PROCESSING SUBSYSTEMS

The display processing subsystems which have been discussed to this point have all produced displays in which characters were composed of continuous lines or dots. However, a computer data display can also be obtained where information is presented in a television raster. To achieve a television presentation, computer (digital) data is converted to television (video) data, hence the name, digital-to-video display system.

A block diagram for a simple digital-to-video display system is shown in Fig. 7. Under control of the timing and control unit, computer data is entered into the memory in an ordered sequence corresponding to the horizontal and vertical position of the data on the viewing screen. Then the timing and control unit initiates a horizontal and vertical memory scanning process. Every time a horizontal scan is initiated, a horizontal synchronization pulse is generated and whenever the end of the bottom line is reached, a vertical synchronization pulse is generated. The horizontal and vertical synchronization pulses are then used to trigger corresponding sweeps which drive the deflection amplifiers, and in turn the CRT. The result of this scanning, synchronization, and sweeping process is a raster presentation on the CRT.

In order to obtain information from the CRT, its Z-axis must be turned on and off at the proper time in synchronization with the sweep signals. Two methods may be used to obtain the required Z-axis control signals.

In one method, computer data is stored in the memory on a one-to-one relationship with spots to be intensified on the CRT. That is, a 1,000 by 1,000 bit X-Y memory matrix would provide the capability to intensify any of a 1,000 by 1,000 spot matrix on the CRT. In this method, the Z-axis control signals are extracted from the memory by the character generator during the horizontal and vertical scanning process.

In another method, the computer data is stored as 6 to 8-bit coded data corresponding to each character to be presented on the CRT. Here again the data is arranged in the order in which it will appear. In this method, when the memory is scanned, the coded data is extracted and applied to the character generator. The character generator converts the coded computer data into Z-axis control signals corresponding to the character required.

The digital-to-video system lends itself to multi-station display systems. By combining the X and Y synchronization pulses with the Z-axis control signals, a single signal line can be used to connect the display station to the display control unit. In the display station the synchronization pulses and the Z-axis signal are separated and applied to the respective sweep and

Z-axis circuits. By supplying the display controller with multiple outputs, a number of display stations can easily be tied to a single controller.

One factor in the use of a digital-to-video system is the number of horizontal scanning lines which are used. The greater the number of horizontal lines, the better the resolution of the display. However, increasing the number of lines causes a corresponding increase in the bandwidth required of the deflection and Z-axis subsystems (if the vertical scan rate remains constant).

With the digital-to-video system, interlaced scanning is usually used to reduce flicker. In interlaced scanning, first one field consisting of every other horizontal line is produced, then, the missing lines are inserted in the next field. Thus, in two successive fields the complete presentation is made. With commercial television, interlacing reduces the effects of flicker by providing a 60 Hz field rate which does not flicker, although the frame rate is 30 Hz (one frame equivalent to two successive interlaced fields).

Digital-to-video display systems offer some advantages which are not available with conventional displays. Background data can be superimposed on the computer data by merely combining video signals. Display stations can be slaved to a main station when a common synchronization and Z-axis control signal line is used. An advantage of the digital-to-video system which stores each spot is that the amount of data which can be presented is limited only by the number of spots which are available.

CONCLUSION

In the computer data display, the display processing subsystem provides the interface between the computer and the other display subsystems and devices. Since the configuration of the display processing subsystem affects the data that can be presented, there are a number of design factors that should be considered.

One consideration is whether a multistation or stand-alone arrangement is to be used. For stand-alone displays, the number of display stations that can be accommodated should be known. In the multistation system, the characteristics of the display control unit and the number of display stations are important. Another multistation question is whether the character and line generator are contained in the display control unit or display stations.

Another consideration is the type of data transfer that is employed; is it serial or parallel? For parallel transfer, the number of bits per word and their coding are necessary. For serial transfer, the bit transfer rate, bits per character, and start and stop bit arrangement are necessary. In either data transfer method, the coding and arrangement of data transmitted from data entry devices are important.

The coding of data and the arrangement of control signals for that data must be accounted for in the display processing subsystem. The combination of

computer control and data signals are used to put the received computer data into the proper formats for the character, line, and position generators. Along with the coding, the timing of computer data and control signals affects the design of the display processing subsystem.


Another computer-display interface factor is the compatibility between the logic levels of the two systems. This is an important factor since both line receivers and line drivers are usually required for two-way communication with the computer.

Another display processing subsystem design factor is the data storage method to be used. If a refresh memory is to be used, its refresh rate and storage capability must be known. The data storage and retrieval times will control the amount of data that can be transferred from the computer to the display. Each data storage method has its own unique properties which affect the design of the display processing subsystem. In some display systems there is no data storage requirement and the computer itself furnishes the data storage property.

A final consideration involves the data entry devices that are employed. These devices usually require special logic to put data into proper format for transmission to the computer.

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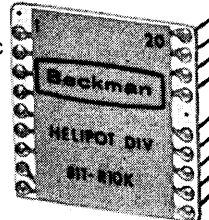
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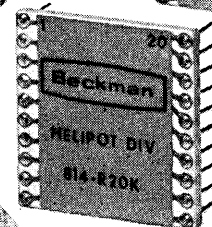
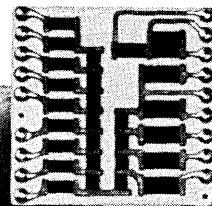
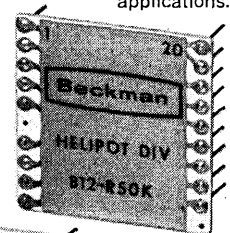
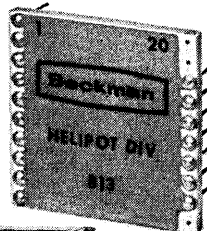
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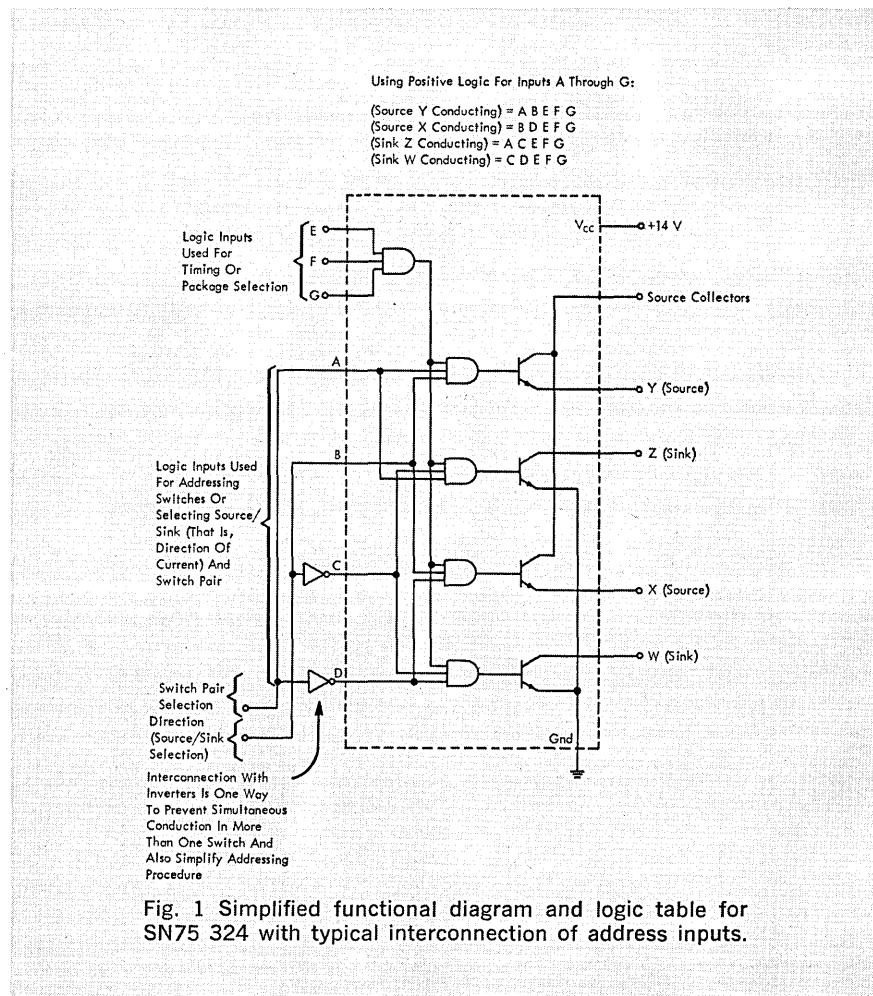
An IC Driver for Magnetic Memory Systems

James Talley
Bill Whittekin
 Texas Instruments, Inc.
 Dallas, Texas

This application note briefly describes the SN75 324 monolithic integrated-circuit memory driver and illustrates how to use it to address and drive a magnetic memory. A functional diagram of the driver appears in Fig. 1.

This unit is designed specifically to replace traditional discrete transistor-transformer circuits in magnetic memory systems; however, it can also be used as a lamp driver, relay driver, or high-fan-out logic gate. It consists of four fast, high-current switches controlled by seven logic inputs (denoted A through G) that are compatible with 54/74 TTL and other standard logic systems with precautions mentioned under "Logic Input" below. One pole of each switch leads outside the unit (outputs W, X, Y, and Z). On their opposite poles, two of the switches connect to the memory current source, and the other two connect to ground. Thus, two outputs are sources and two are sinks for memory drive current.

The decoding circuitry is arranged so that any or all of the switches in a package may be conducting at any given time. However, the unit will overheat if



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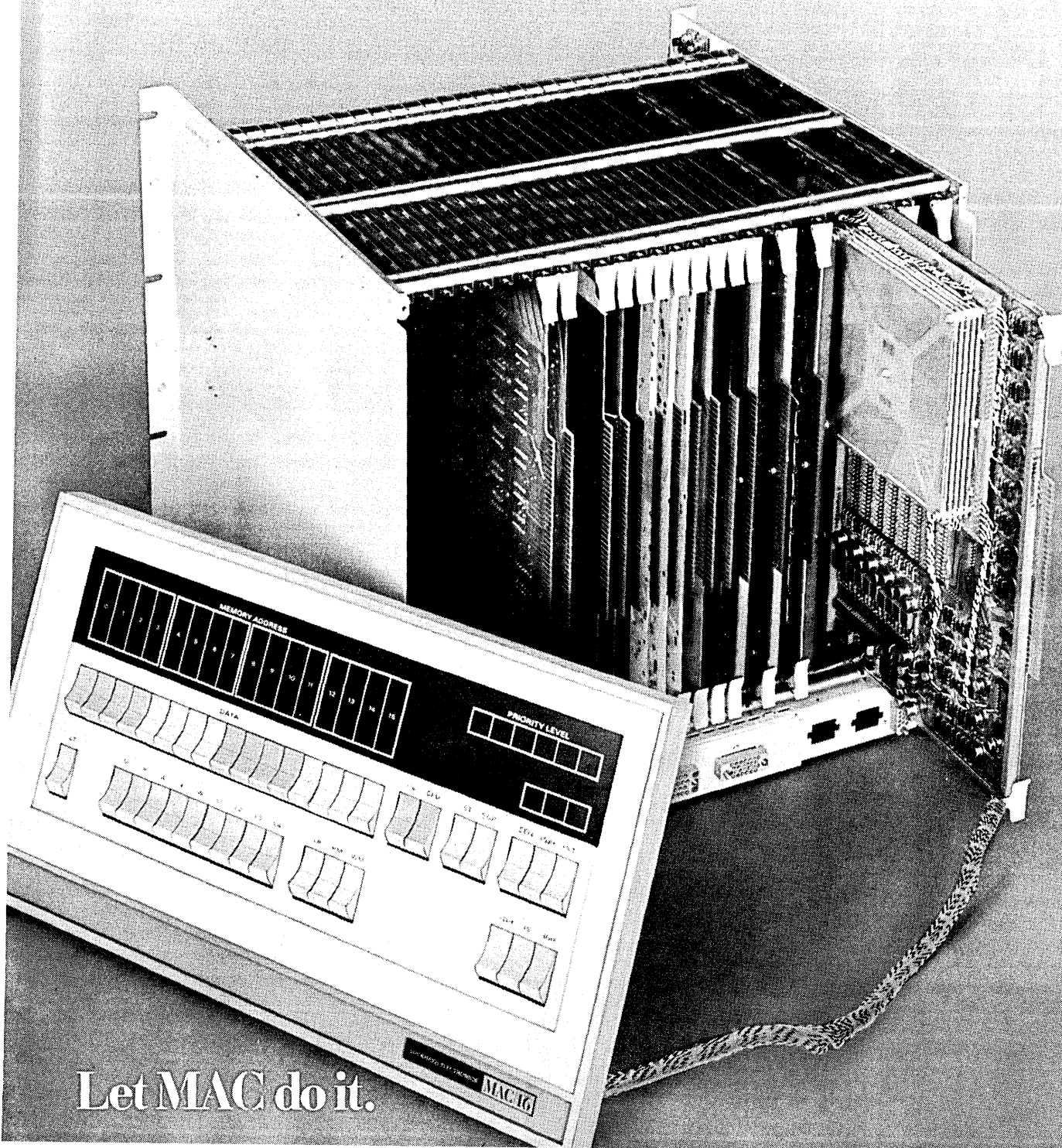
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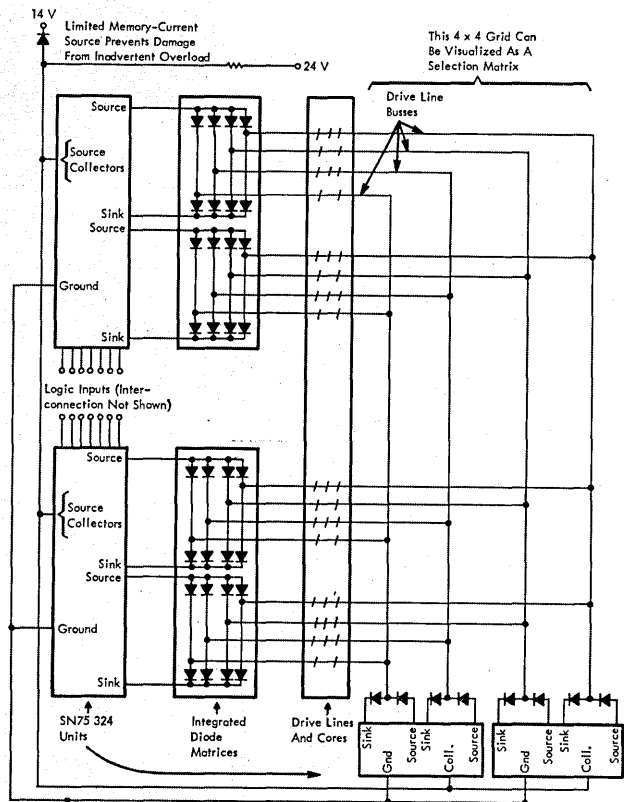


Fig. 2 Typical application of SN75 324 in Memory-drive: a selection scheme for 16 drive lines.

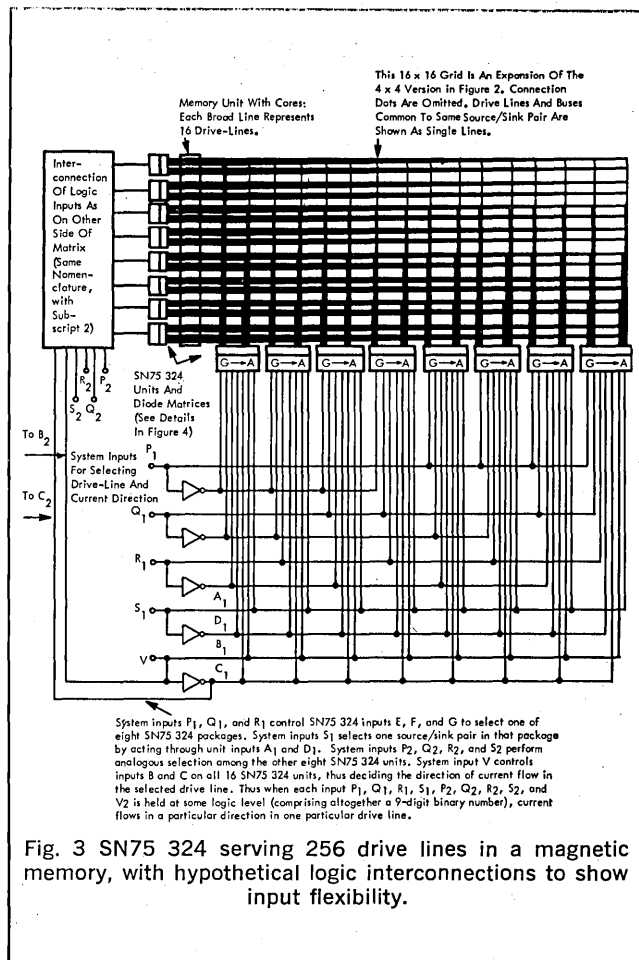


Fig. 3 SN75 324 serving 256 drive lines in a magnetic memory, with hypothetical logic interconnections to show input flexibility.

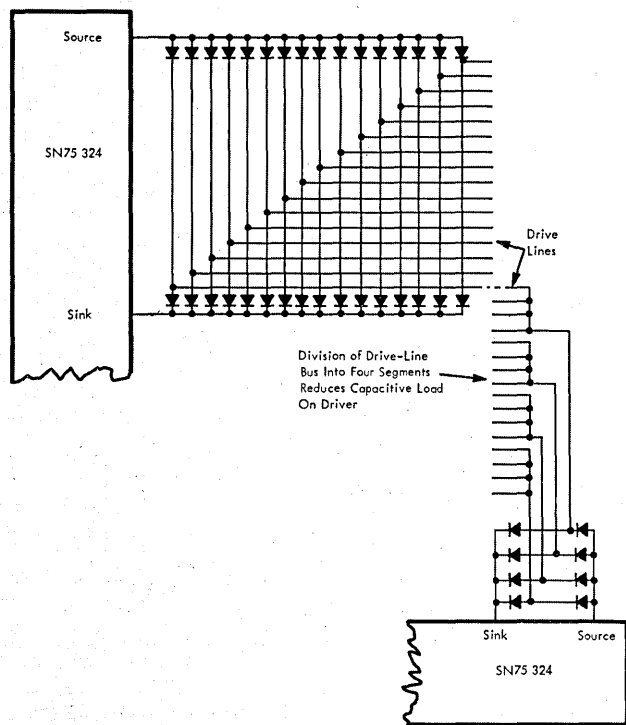


Fig. 4 Details of connection of drive-lines to drivers in Fig. 3.

more than one switch at a time carries memory current. Therefore, the system must be designed to prevent this occurrence by such means as the external logic inverters shown in Fig. 1.

MEMORY-DRIVE APPLICATIONS

In memory-drive applications, the SN75 324 can be connected in any of several fashions. Typically, however, sources and sinks are arranged in pairs from which many drive lines branch off, as shown in Fig. 2. Here each drive line is served by a unique combination of two source/sink pairs, so that a selection matrix is formed. The size of such a matrix is limited only by the number of drive lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive line of the particular system imposes on the driver.

A larger selection matrix is shown in Fig. 3 and 4. The hypothetical interconnection of logic inputs demonstrates one way to take advantage of the multiple logic inputs of the SN75 324.

Characters
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500 to
1000

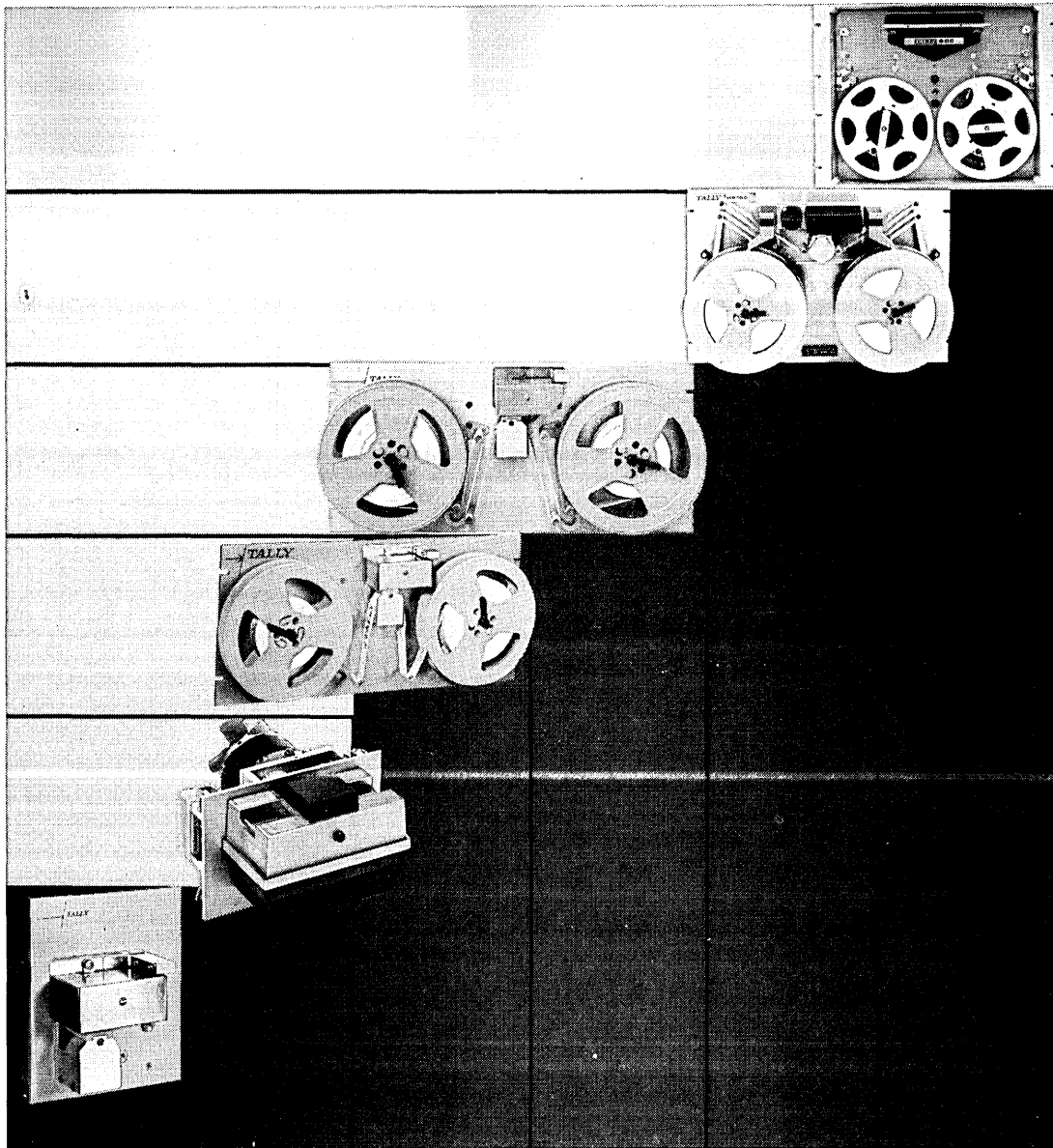
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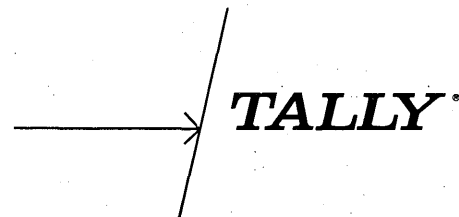
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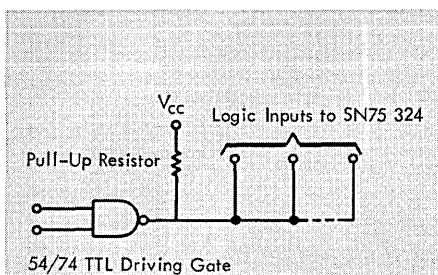
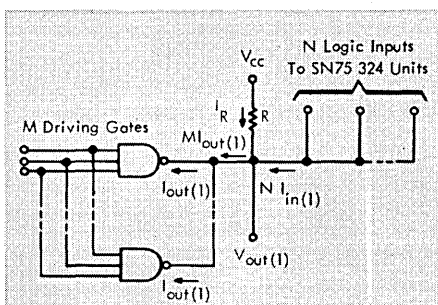
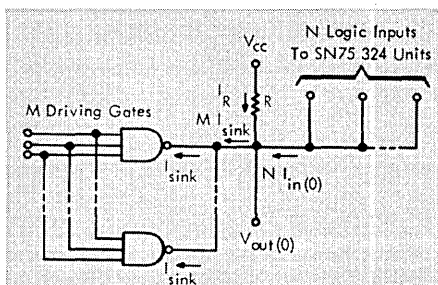


Fig. 5 Input to SN75 324 from 54/74 TTL using pull-up resistor.



Voltage across $R = V_{in} = V_{cc}(\text{min}) - V_{out(1)}$
 Current through $R = I_R = M I_{out(1)} + N I_{in(1)}$
 Therefore $R(\text{max}) = \frac{V_{cc}(\text{min}) - V_{out(1)}}{M I_{out(1)} + N I_{in(1)}}$
 where $V_{out(1)} = 3.5 \text{ V}$ minimum to drive SN75 324 input
 $I_{out(1)} = 250 \text{ uA}$ maximum for 54/74 TTL gate output
 $I_{in(1)} = 100 \text{ uA}$ maximum for SN75 324 timing inputs
 $= 200 \text{ uA}$ maximum for SN75 324 address inputs
 $M =$ number of parallel driving gates
 $N =$ number of parallel SN75 324 inputs

Fig. 6 Calculation of maximum value of pull-up resistor in Fig. 5.



where $I_{in(0)} = 6 \text{ mA}$ maximum for address inputs
 $I_{in(0)} = 12 \text{ mA}$ maximum for timing inputs
 $I_{sink} =$ maximum specified sink current of driving gate
 $V_{out(0)} =$ maximum specified "0" level output voltage of the driving gate ($\leq 1.0 \text{ V}$), which is 0.4 V for 54/74 TTL
 $M =$ number of parallel driving gates
 $N =$ number of parallel SN75 324 inputs

Fig. 7 Calculation of minimum value of pull-up resistor in Fig. 5.

Regardless of the particular line-selection and logic scheme, the SN75 324 can be densely mounted on printed-wiring boards along with monolithic diode arrays and IC logic packages. The result normally is a system that is cheaper, faster, smaller, more reliable, and simpler to connect than a conventional discrete transistor-transformer version.

LOGIC INPUT FROM 54/74 TTL

Because of the high-noise environment in which the SN75 324 is intended to operate, the input logic levels have been purposely designed to be somewhat higher than standard 54/74 TTL logic levels.

The higher logical 0 input level, $V_{in(0)}$ of the SN75 324 guarantees a dc noise margin of 600 mV when driven from 54/74 TTL. However, the higher $V_{in(1)}$ of the SN75 324 (3.5 V) leads to some minor difficulties when using 54/74 TTL. The minimum guaranteed logical 1 level of 2.4 V at a 54/74 TTL output falls short of the 3.5 V minimum level required at the SN75 324 input. However, this problem can be readily solved by the proper selection of a pull-up resistor at the gate output as shown in Fig. 5.

Because of the high logical 0 input current of the SN75 324 (12 mA for the timing inputs, 6 mA for the address inputs), it may be desirable to drive the inputs from 54/74 TTL buffer gates (SN7440 or SN74H40) to assure adequate sink current capability. Each SN7440 buffer gate output is specified at 0.4 V maximum $V_{out(0)}$ at a sink current of 48 mA. The $V_{out(0)}$ for the SN74H40 buffer gate is 0.4 V at a sink current of 60 mA. If additional sink current is required, the inputs and outputs of both gates in the SN7440 or SN74H40 package may be paralleled for 96 and 120 mA capability, respectively. (This parallel connection requires no significant sacrifice, if any, in switching characteristics, but the outputs of these gates should not be paralleled without

also paralleling inputs. Otherwise one or both of the gates can be damaged because of the active pull-up or "totem-pole" output configuration.)

A large number of SN75 324 inputs may also be driven from the output of any of several 54/74 TTL decode/drivers. For example, the output of the SN7445 BCD-to-Decimal Decode/Driver can sink 80 mA at $V_{out(0)}$ of 0.9 V or sink 20 mA at $V_{out(0)}$ of 0.4 V. Since the maximum $V_{in(0)}$ of the SN75 324 is 1.0 V, the SN7445 can drive the SN75 324 with a pull-up resistor.

When a pull-up resistor is used at the driving gate output, its value must be determined to ensure proper logic levels. The worst-case resistor values may be readily calculated using available driving-gate data sheet information, as exemplified below.

The maximum resistor value is calculated to ensure that sufficient current is available when the driving gate output is high (off). This current must supply the SN75 324 input as well as the driving gate output. For a logical 1, it is necessary to maintain 3.5 V minimum at the SN75 324 input. A suggested method of calculating the maximum resistor value is shown in Fig. 6. The minimum value of the resistor is calculated to ensure that its current plus that from the SN75 324 inputs will not cause the output voltage $V_{out(0)}$ of the driving gate to exceed the maximum of 1.0 V. (See Fig. 7).

After determining the worst-case minimum and maximum pull-up resistor values, any value between the limits may be selected. (Obviously, the calculated minimum value must be below the calculated maximum value to be practical). Selecting a resistor value near the minimum limit will raise the logical 1 voltage and thereby improve the logical 1 noise margin.

An example of an SN74H40 buffer gate driving eight SN75 324 address inputs is shown along with

Assume The Following:

N = 8 Address Inputs	$I_{in(0)} = 6 \text{ mA Per Address Pin}$
M = 1	Driving Gate SN74H40:
$V_{out(1)} = 3.5 \text{ V Minimum}$	$I_{sink} = 60 \text{ mA}$
$I_{in(1)} = 200 \mu\text{A Per Address Pin}$	$V_{out(0)} = 0.4 \text{ V Maximum}$
	$I_{out(1)} = 250 \mu\text{A (Assumed)}$

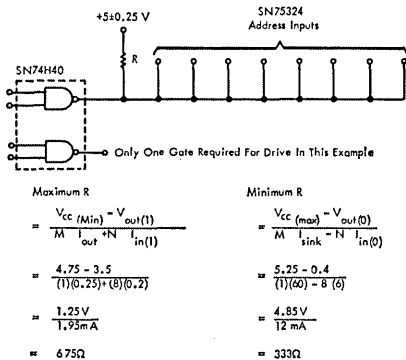


Fig. 8 Sample calculation of pull-up resistor value for SN74H40.

sample calculations in Fig. 8. If, in this example, a value of 400 Ω is selected for the pull-up resistor, the guaranteed logic levels at the SN75 324 inputs are 0.4 V maximum for $V_{in(0)}$ and 4.0 V minimum for $V_{in(1)}$. This resistor results in guaranteed dc noise margins of 600 mV at the logical 0 level and 500 mV at the logical 1 level at worst-case conditions.

CIRCUIT-BOARD PRECAUTIONS

In any memory-drive application, circuit-board mounting of the SN75 324 should be judiciously considered to satisfy the problems of signal transmission, noise, and thermal management. If flat packs are used, they should be mounted flat on a wide copper lamina using a thermal compound, or "base-up" with high-velocity air flowing across them. A row of flat packs should run perpendicular to the cooling air stream rather than along it to avoid accumulated heating of air. If a copper lamina is used, it should be expanded to fill the empty area on the circuit board to enlarge the cooling surface. Furthermore, because memory drive and logic currents share the same electrical ground in a direct-coupled system exemplified in Fig. 2 through 4, it is necessary to take special care to minimize ground noise.



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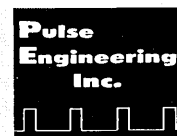
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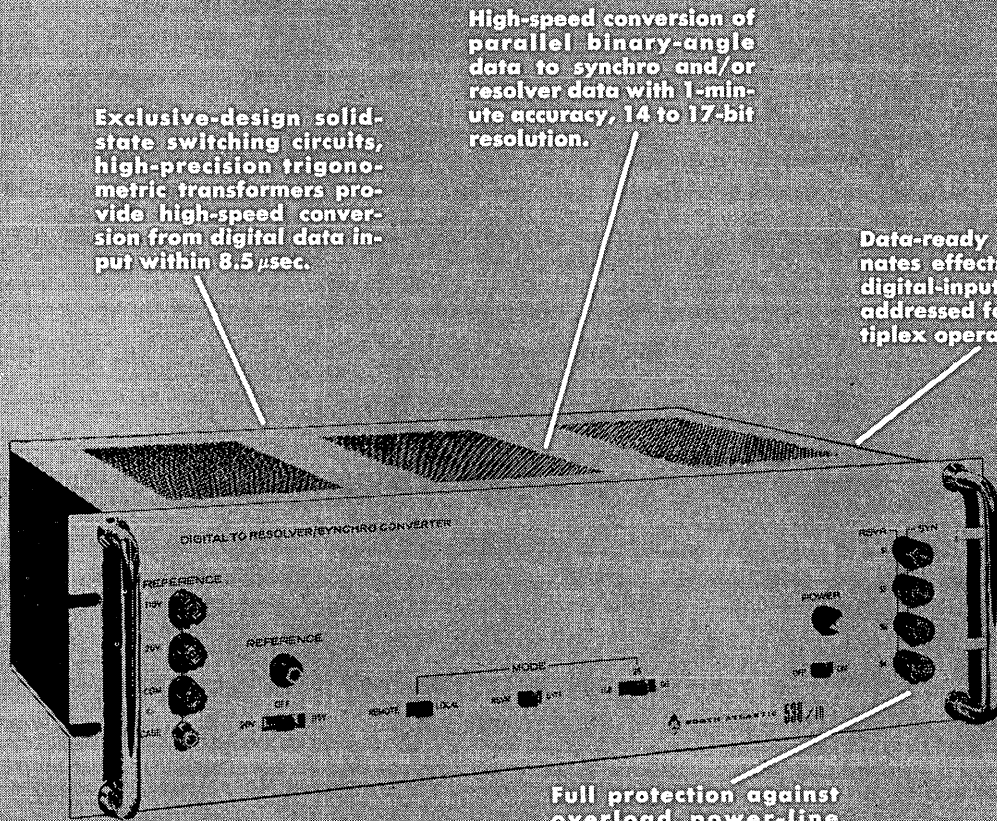
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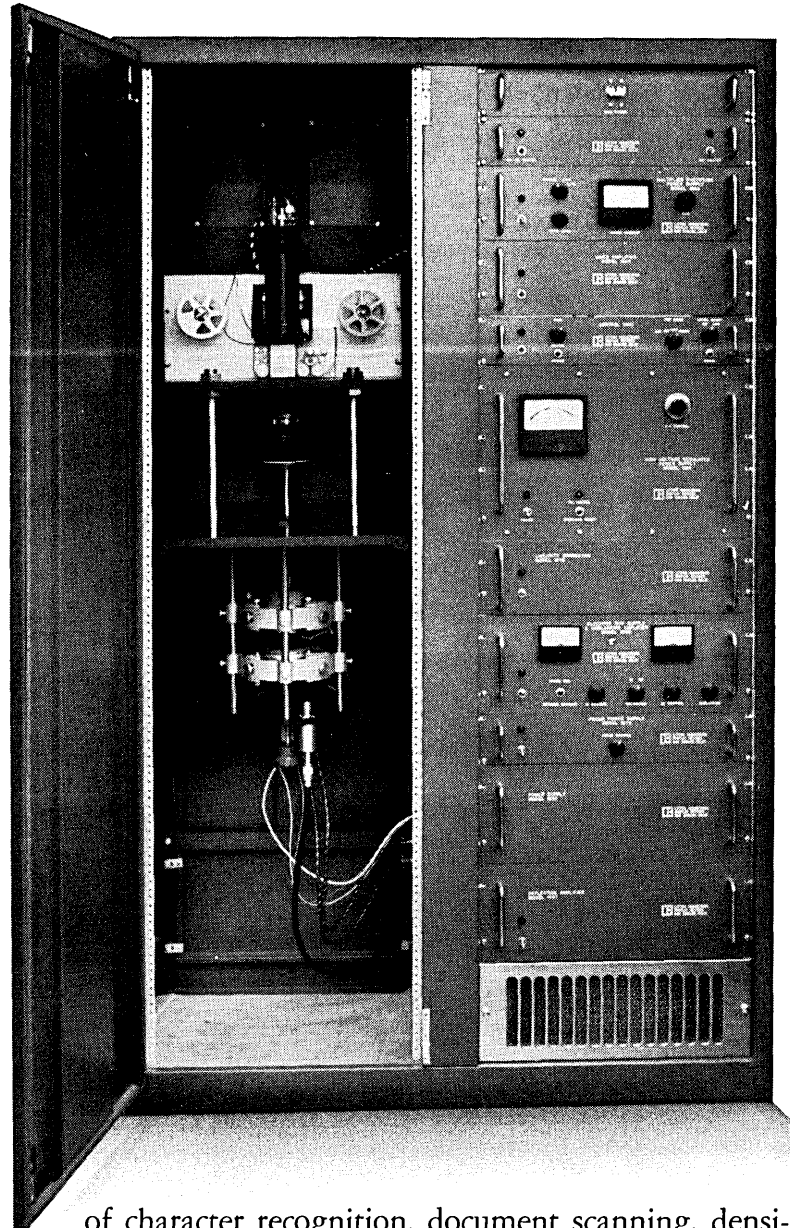
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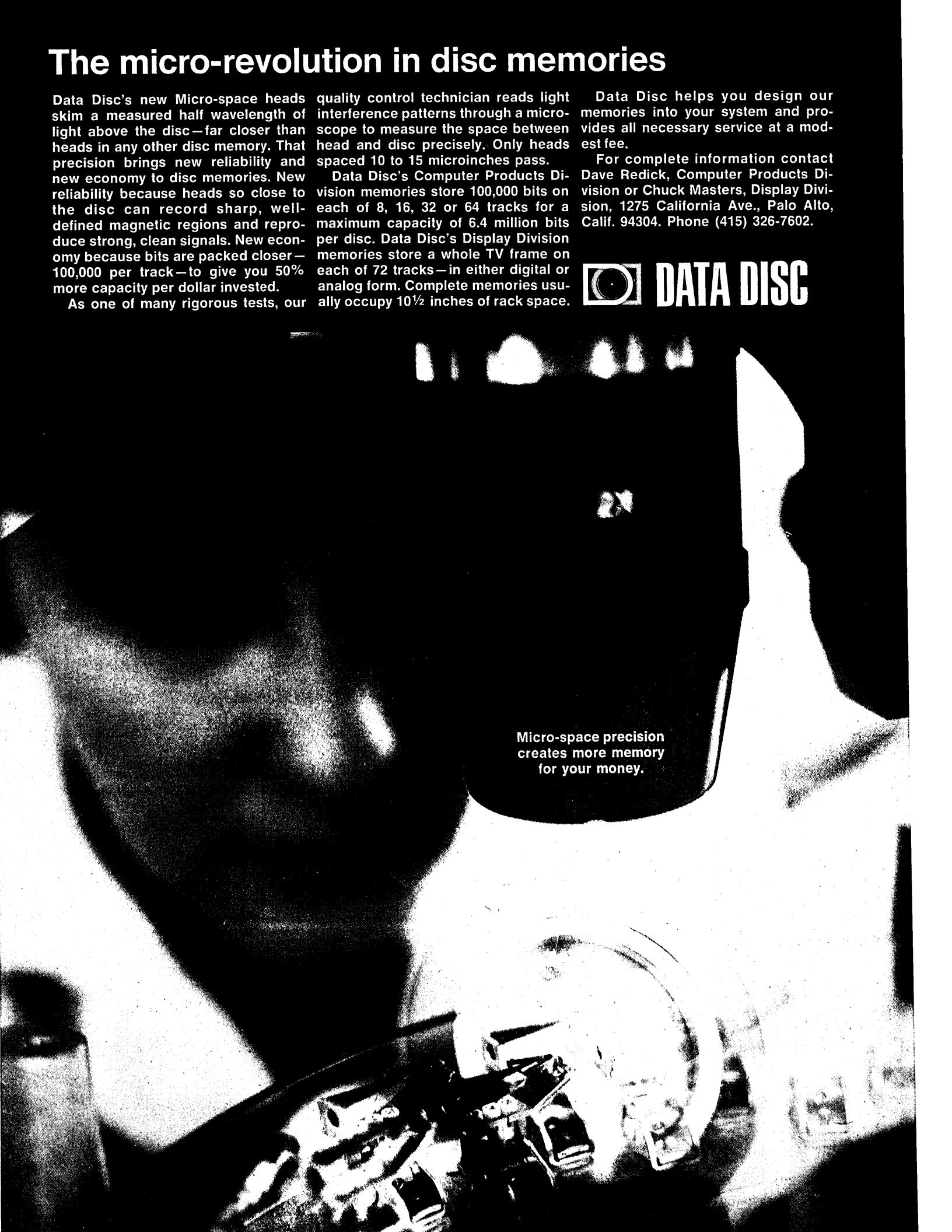
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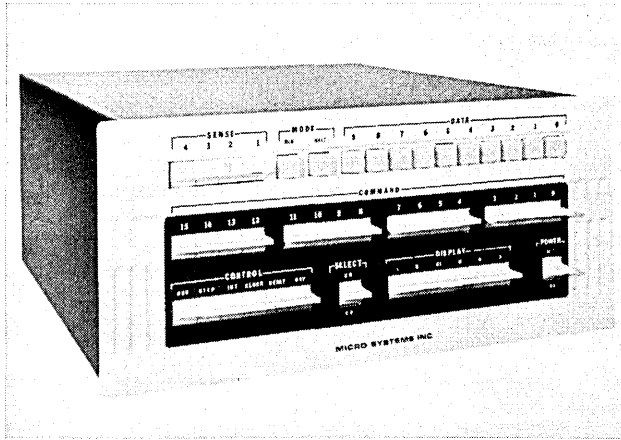
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The MICRO 800 features a 1.1 microsecond full cycle core memory with a micro-command execution time of 220 nanoseconds. Core memory is expandable from zero to 32,768 bytes (8, 9 or 10 bits) in 4096 byte increments to meet the configuration for any application. Read-only storage is expandable from 256 to 1024 words in modules of 256 words. File registers are a set of 16 general-purpose 8-bit registers.

Its microprogramming allows adapting internal organization and instruction repertoire to achieve both speed and core memory efficiency impossible with conventional computers with fixed instructions. With microprogramming, I/O interface hardware is reduced to a minimum in any application. The 800 may also be programmed with a standard instruction set to provide macro-level software solutions. Additionally, the computer may be programmed

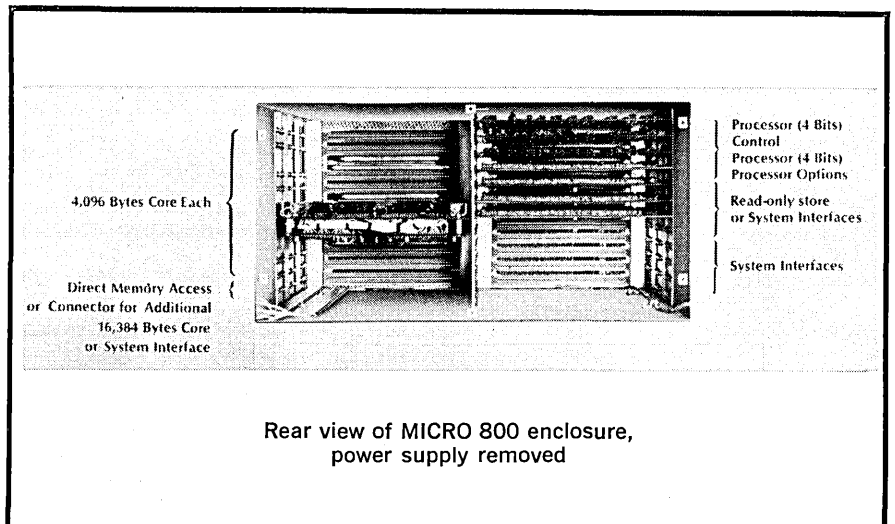
by creating problem oriented macro-instructions and I/O facilities which supplement a standard instruction set to give an optimum software/firmware programming mix.

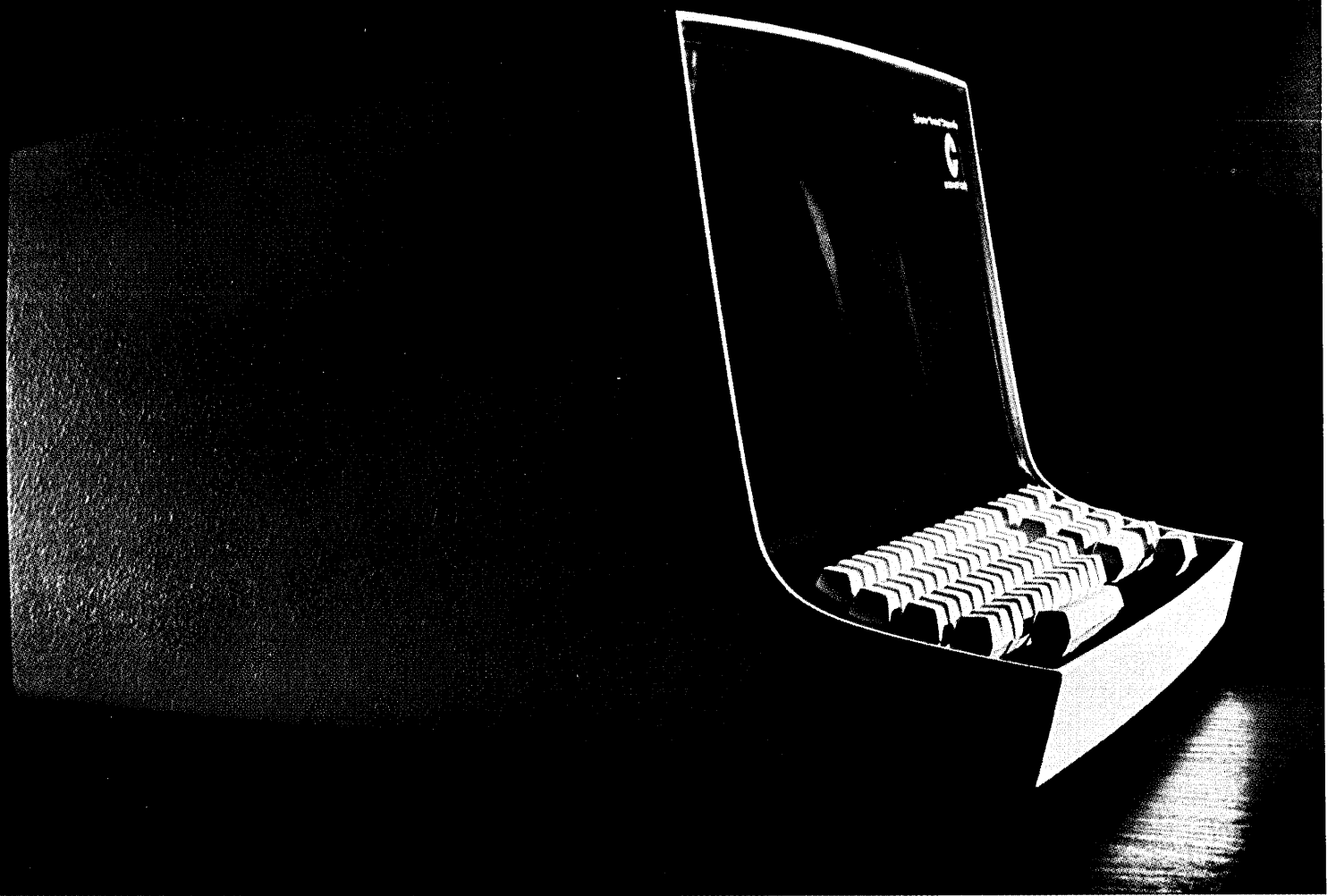
Mechanical and electrical construction of the 800 reduces system costs by providing standard modules for system options such as direct memory address, memory protect, power fail detect/re-start and external interrupts. These elements can be mounted in the basic enclosure along with special system interface boards.

The computer is designed to operate between 0° C and 45° C, and 10-90% relative humidity. Power requirements are 115/230 Vac, 50/60 Hz. The basic cabinet measures 8¾ h x 17¾ w x 23" d, including power supply and fan.

The basic system consisting of the CPU with 256 words of ROS memory is \$2,950. Core memory of 4096 bytes may be added for an additional \$2,500. OEM discounts to 40% are available.

For additional information circle No. 199 on inquiry card.





If you've got something to say to a computer you can say it best with a Datapoint 3300 — Here's why:

- * The Datapoint 3300 is the *first* data terminal to be designed specifically for interactive time sharing use.
- * The Datapoint 3300 is engineered to be *fully compatible* with all time sharing services now using Teletype equipment as terminals.

In developing the Datapoint 3300, Computer Terminal Corporation sought a terminal that would amplify the productivity of the professional as he worked upon problem solutions in interactive dialogue with a computer. We sought to remove the traditional barriers to effective man/machine communications. We succeeded.

A central feature of the 3300 is the CRT display capacity of 1800 characters

in a 25 line/72-character-a-line format. (A high "refresh" rate provides characters that are at once stable and easy to read.) In this expanse of data, a complex program or problem can easily be expressed, and comprehended at a glance. The interactive user, working the standard 64-character-set keyboard, can easily add, delete, correct or manipulate characters and lines of data. The remote computer becomes a powerful and flexible extension of the human thought process, directly responsive to and controlled by the user sitting at the Datapoint 3300.

Because the 3300 is not shackled by the limitations of a mechanical printer, it can make available data transmission rates of up to 600 bits per second

standard, and up to 4800 bps with optional speed buffer. This means the interactive user enjoys faster response from his remote computer; accordingly, his "on-line" time will shrink while his productivity goes up.

The 3300 is noiseless — no hum or clatter of keys to intrude upon the user's concentration. It comes packaged in a handsome, totally self-contained unit, comparable in size to an executive typewriter, which blends well with today's office environment. The female help will love the 3300's appearance, as well as its ease of usage.

We think you'll like it. For further information, simply write to Computer Terminal Corporation, P. O. Box 6967, San Antonio, Texas 78209.



**Computer
Terminal
Corporation**



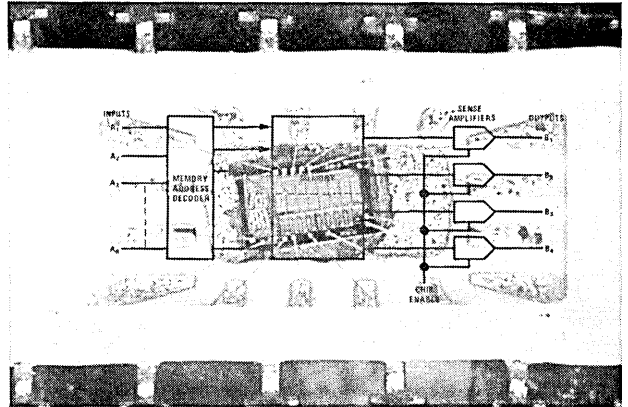
NEW PRODUCTS

MOS READ-ONLY MEMORY

The MM521, arranged as 256 x 4-bit words is constructed on a single silicon chip using a thick oxide P-channel MOS process. Programming of the memory contents is accomplished by changes in one mask during the device fabrication. This procedure produces a non-volatile data storage. Gate protection diodes are used on all inputs to protect against static charge build up.

Key performance features include dc coupled logic on chip with no clocks required and high speed operation of less than 1 μ sec. The MM521 is completely compatible with DTL or TTL logic. Temperature range of the ROM is -25°C to $+70^{\circ}\text{C}$. National Semiconductor Corp., Santa Clara, Calif.

Circle No. 200 on Inquiry Card.



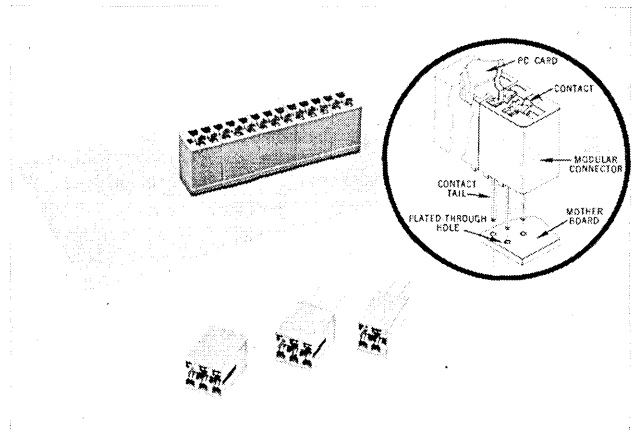
MODULAR PC CONNECTOR

Designed for array-mounting on a mother board, Series 6308 MOJO™ card-edge receptacle combines the advantages of modular design with a completely new contact that eliminates soldering when contact tails are press-fitted into plated-through holes in the board.

The contact tail combines a square wire-wrapping post with a specially designed shoulder which, when press-fitted into the plated-through hole in the mother board, provides a permanent, gas-tight electrical connection without soldering.

Two module sizes are available: connector end modules incorporate 4 dual-readout contacts (two .150"-center card positions) and one molded-in card guide. Center modules incorporate six contacts (3 card positions) and are open-ended. Elco Corp., Willow Grove, Pa.

Circle No. 201 on Inquiry Card.



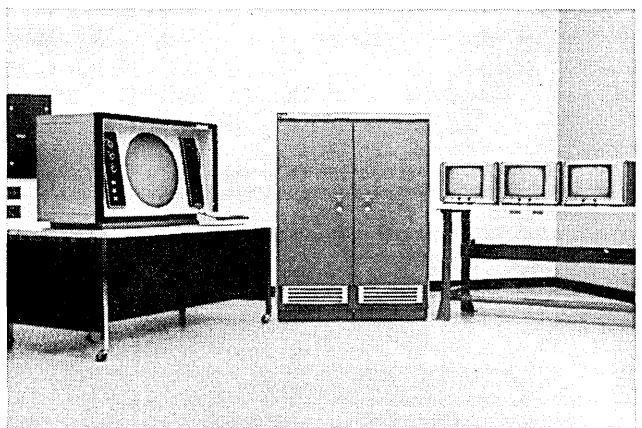
GRAPHIC DISPLAY SYSTEM

The ADDS/900 (Advanced Data Display System) features unique mixed mode and time shared operation of one or more displays, high speed function generation, a variety of editing devices, and a small integral computer with comprehensive software for the system. The system is comprised of four basic elements—a display processor, display generator, data entry devices, and display indicators.

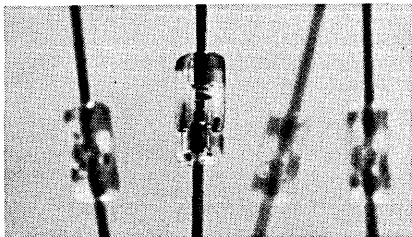
The display processor, with a 1.8 μ s cycle time, features a 16-bit word display processor, and a standard memory capacity of 4096 words expandable to 32,763 words, or 20,480 words with a dual port core.

The display generator is capable of generating character, symbol and line vector information with a dynamic writing speed range of 64 to 1 in multiple steps under control of the display processor. Character generator time is 2.4 μ s typical and vector generator time is 40 μ s for full screen on axis. Sanders Associates, Inc., Nashua, N.H.

Circle No. 202 on Inquiry Card.



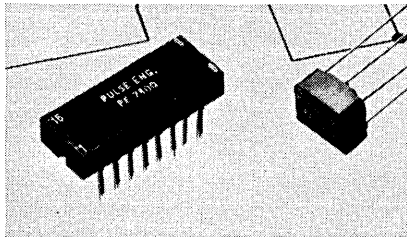
NEW PRODUCTS



SCHOTTKY SWITCHING DIODE

The MA4-A200 is a planar passivated silicon diode, utilizing a unique combination of two Schottky barriers and a P/N junction. The diode has the high breakdown voltage ($>25V$) and operating temperature characteristics of silicon, combined with the low turn-on voltage of germanium and the ultrafast speed of a Schottky barrier device. The diode is well suited to pulse and digital circuits such as clamping, clipping, speed-up, steering and sampling. Microwave Associates, Inc., Sunnyvale, Calif.

Circle No. 264 on Inquiry Card.

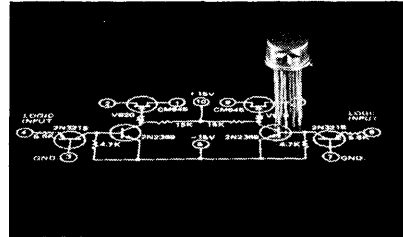


BALUN TRANSFORMER

A pulse transformer series designed to reduce noise in computer memory circuits is available in a four transformer module compatible with integrated circuits as well as in discrete miniature cases. The balun transformers feature ratios of primary inductance to leakage inductance as high as 6600:1.

Balun transformers with primary inductances of 20 microhenries to 2,000 microhenries are available from stock. Pulse Engineering Inc., Santa Clara, Calif.

Circle No. 268 on Inquiry Card.



IC DUAL ANALOG GATES

The CAG13 SPST FET switch hybrid ICs, designed for analog gating, contain two complete circuits in one low profile TO-5 package. Each circuit features 50 ohms maximum on-resistance, ± 9 volt signal range, 300 ns typical switching time, and direct operation from DTL or TTL logic. The unique circuit configuration provides break-before-make switching action and higher off-impedance to high frequency signals. This hybrid microcircuit uses all military grade semiconductors. Crystalonics, A Teledyne Co., Cambridge, Mass.

Circle No. 269 on Inquiry Card.

N/C TAPE PREPARATION UNIT

The Datawriter N/C-1, designed exclusively for numerical control, reproduces tape from master copies and allows tape editing and correcting. The 10 character-per-second unit has an alphanumeric keyboard which is arranged for ease of numerical control program preparation; special symbolic characters are available. The 72 character per line printer provides the operator with hard copy of the program being prepared.

The 10 character per second punch will punch any tape conforming to EIA standards (RS-227) and features "On," "Off," "Tape Release," and "Backspace." The tape reader reads punched tapes so that master tapes can be duplicated and errors corrected or removed from N/C program tapes. The reader controls feature both continuous or single step operation and provide for a free position allowing tape to be moved manually through Reader skipping characters in error. Datron Industries, Inc., Greensburg, Pa.

Circle No. 249 on Inquiry Card.

DIGITAL ISOLATION SWITCHES

Model 601 is an isolating digital circuit with 500 ns response, capable of transmitting dc logic levels. Eight models provide all combinations of inversion, translation and bipolar operation. Dimensions are $0.4" \times 1\frac{1}{8}" \times 1\frac{1}{2}"$. Proper operation requires power be supplied separately on both input and output sides.

Model 602 provides an isolating interface for digital logic signals with 100 ns response. Input-to-output isolation prevents signal contamination in interface processes by eliminating ground loops. Input has variable threshold Schmitt trigger characteristics. Output is fully floating—power is carrier-derived from the input side and is sufficient to provide a dc to 3 MHz response. A single 602 can be used to provide signal inversion, translation, compression or expansion as required, with simple external adjustments. Dimensions are $2" \times 2\frac{1}{2}" \times \frac{3}{4}"$. Dynamics Instrumentation Co., Monterey Park, Calif.

Circle No. 265 on Inquiry Card.

SWITCHING MOS FETS

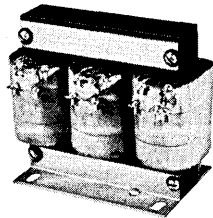
Two p-channel enhancement type MOS FETs for analog and digital switching applications are: the 3N167 which has a maximum drain-source ON resistance $r_{DS(ON)}$ of 20 ohms; and the 3N168 with a maximum $r_{DS(ON)}$ of 40 ohms. The 3N167 has a drain or source cutoff current I_{DSS} or I_{SDS} of less than 0.5 nA; the 3N168 less than 1 nA at room temperature.

The potential problem of oxide breakdown, due to static-charge accumulation on the gate, is eliminated by a built-in Zener diode between gate and body. Gate protection is assured because the 85-volt diode breakdown is much lower than the oxide destructive voltage. Drain-source, gate-source and gate-drain breakdown voltages are all 30 and 25 volts minimum for the 3N167 and 3N168 respectively. Gate threshold voltage is 6 volts maximum. Package is a TO-72. Siliconix Inc., Sunnyvale, Calif.

Circle No. 250 on Inquiry Card.

3 good reasons why you should build your own systems' power system:

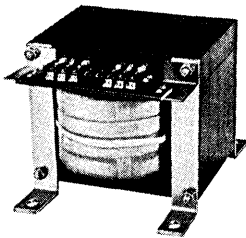
1.



Genisco three phase transformers.

Our three phase transformers are practically all you need to build your primary power system. They come in ranges from 3 to 37.5 KVA, either open or enclosed.

2.



Genisco Control Transformers.

These dry type transformers can do the secondary power system job. Three different groups to choose from. Ratings from 0.250 to 5.00 KVA.

3.



Transient free switch/controller.

This handy device makes sure that all switching on or off occurs at zero crossovers. That way noise-generating discontinuities are eliminated.

Put these components together, add a few transistors and diodes, and you have your own, built in-house power supply. No need to pay someone else to do it. For more reasons why you should build your own consider economy, suitability, availability, and complete control over your product. For more information on our products, circle the reader service number shown below.



Is it the reliability or the low cost that makes Varo computer power supplies so desirable?

Definitely.

Together they're probably the most important factors in any computer power supply buying decision.

Neither one comes easy.

But we're now building a 4% regulating ferroresonant transformer, the Varoformer,TM that does the same job as conventional units, and takes up 30% less computer space doing it.

The Varoformer is not only considerably smaller and simpler in design, but requires much less resonant capacitance, and is highly reliable and competitive in price with conventional off-the-shelf units.

We also take this same high reliability-low cost approach in custom-designing regulated computer power supplies.

We're building this kind of supply with multiple outputs, on-off sequencing, and remote sensing for the computer/peripheral industries.

If you're in the market for computer power supplies, we have a great reliability story for computer engineers and designers.

And another great one for purchasing agents.

Want proof?

Contact our sales manager.

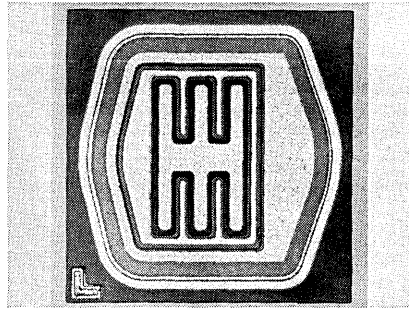


VARO

STATIC POWER DIVISION 1600 DALLAS NORTH PARKWAY, PLANO, TEXAS 75074 (214) AD-1-5111 TWX 910-860-5640

CIRCLE NO. 36 ON INQUIRY CARD

NEW PRODUCTS



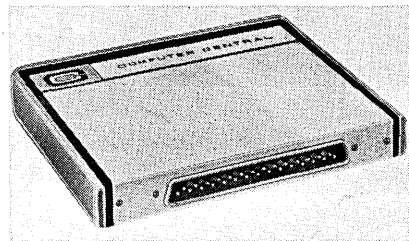
VIDEO OUTPUT TRANSISTORS

Three high voltage video output transistors are designated as the SE-7055, a 220 V unit with a low collector base capacitance of 3.0 pF; the SE7056, a 300 V unit with a 3.5 pF capacitance; and the SE7057, a 450 V unit with a 2.5 pF capacitance.

All three transistors feature power dissipation of 7.0 watts at 25°C case temperature (or 1W in a 25°C ambient temperature) and a typical frequency response of 80 MHz while driving up to 10 mA. Package is a standard TO-39.

Typical applications for the devices, in addition to TV video drive circuits, can be found in storage tube drivers, image converter tube drivers, electro-illuminated displays, and high voltage indicator tube drivers. Fairchild Semiconductor, Mt. View, Calif.

Circle No. 215 on Inquiry Card.

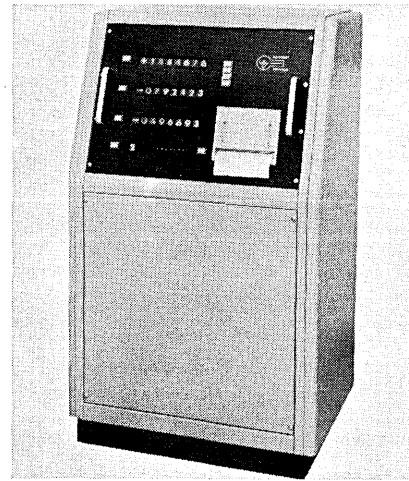


BINARY COMPARATOR

A sign or equality binary comparator may be interconnected to compare any number of bits and is available in a variety of options to assure system compatibility.

The Model 714 binary comparator subtracts two parallel input numbers and converts the difference to one of three non-simultaneous outputs: $A > B$; $A = B$; and $A < B$. It is available with edge-tab or pin type connectors. Compact size is $5\frac{1}{2}$ " x $4\frac{1}{4}$ " x $\frac{7}{8}$ ". Computer Central, Detroit, Mich.

Circle No. 224 on Inquiry Card.



IC DISPLAY/PRINTER

A three axes position display printer for machine tool application, employs TTL IC logic and will display three axes of machine slide motion and print this information on command. The print command can be introduced by a panel mounted push button, by a remote push button, or by a miscellaneous function programmed on a numerical control.

The VU-POINT display printer is easily adapted to numerical controlled or operator controlled machine tools. This device then becomes an in-process inspection tool. The displays show the machine slides to be in proper location and the printed record assures that proper coordinate locations were held. Remex Electronics, Hawthorne, Calif.

Circle No. 235 on Inquiry Card.

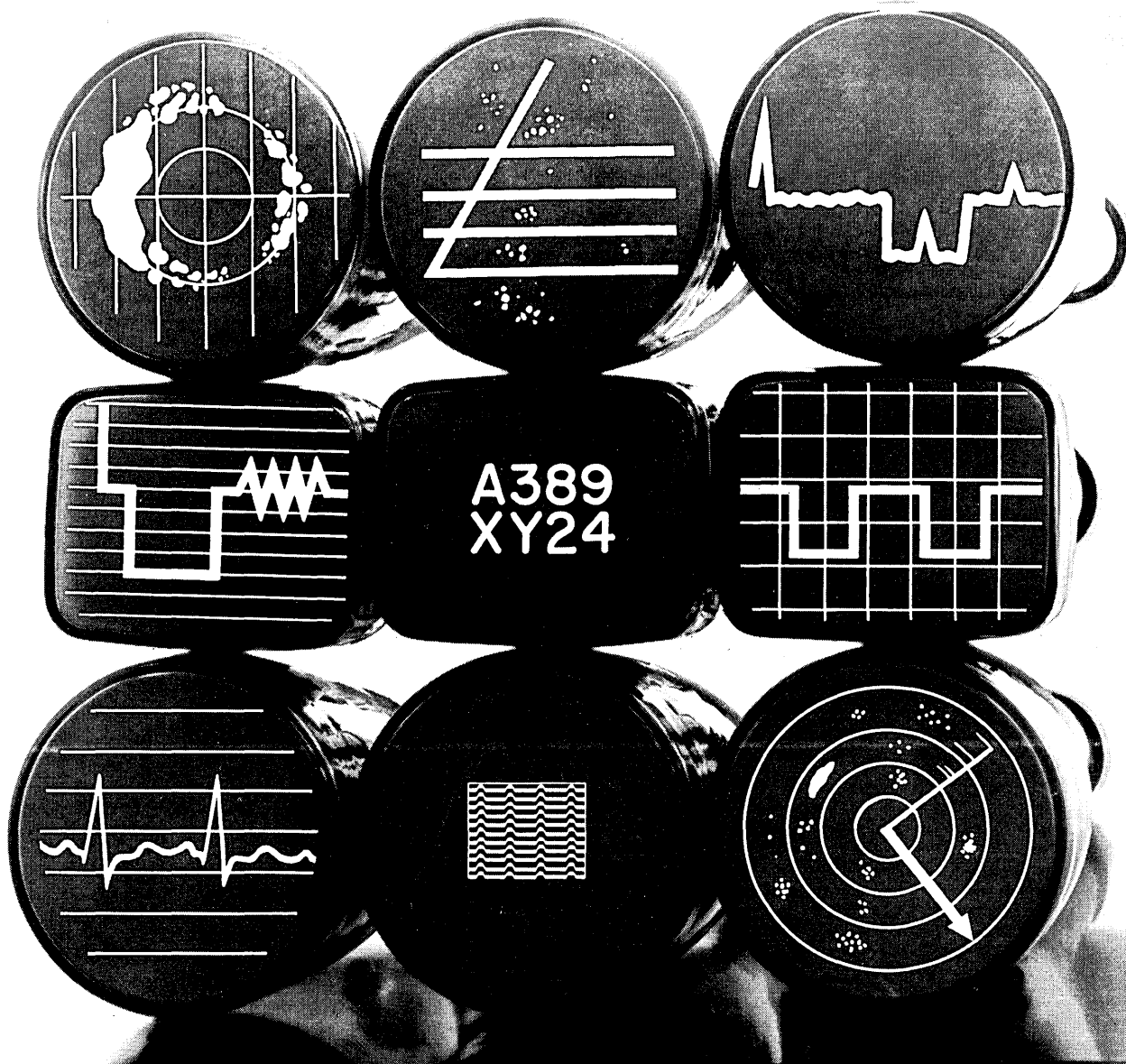
IC SWITCHING CARDS

A series of integrated circuit switching cards, designated MU1 through MU6, provide an isolated digital interface between major elements of a data processing system. Each card contains either two or four IC Iso-Switch[®] cards. These mate directly with DTL and TTL input and output circuitry.

The cards eliminate noise problems commonly encountered when dissimilar data processing equipment is provided with common ground loops. The switching cards solve this noise problem by eliminating such common loops and essentially isolating the equipment.

Six cards are available in the series. Operating currents are 50, 100, and 150 mA, with one two-switch and one four-switch card available at each current level. Raytheon Computer, Santa Ana, Calif.

Circle No. 237 on Inquiry Card.



We offer over 200 talking pictures. Pick one that speaks your language.

Our CRT's have been articulate right from the start. Our first, thirty years ago, told us we were onto a good thing. Some people didn't believe it, but that one spoke our language.

Since then we've gone on to develop and produce CRT's that make up an electronic United Nations.


One speaks to the weather-

man. Another to a heart specialist. There's one that sits on a desk and talks to bookkeepers or accountants. And one that communicates with aircraft control tower personnel. One that strikes up a conversation with geologists. And even one that displays nuclear explosion data to anyone who cares.

That's asking a lot from a CRT.

But then we've always done that. And we'll go right on doing it. Because even as our customers tell us, there's almost no limit to what a CRT can talk about.

Want to start a conversation with a CRT? Call or write us to arrange a meeting... anytime.

Electronic Tube Division,  General Atronics, Philadelphia, Pennsylvania 19118



GENERAL ATRONICS

CIRCLE NO. 37 ON INQUIRY CARD

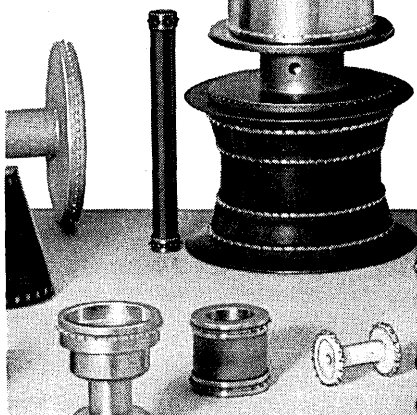


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Whether your tapes, charts or films have round or rectangular perforations, the ideal drive units are LaVeZZi sprockets — Precision parts with every tooth perfectly formed, exactly sized and wholly free of burrs. Inquiries, quote requests invited. Stock items or made to your specs.

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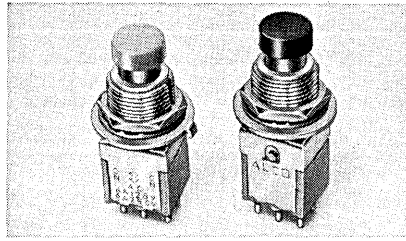
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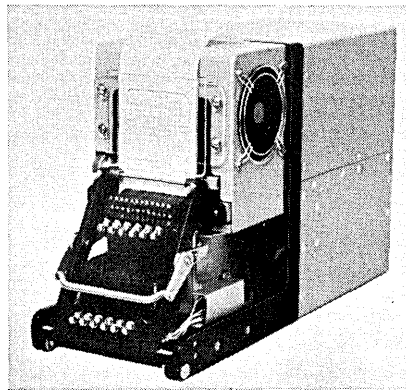
NEW PRODUCTS



MINIATURE PUSH BUTTON

A miniature push button switch features a standard $1\frac{5}{32}$ " hole mounting but has the rear panel space requirements of miniature switches. These push button DPDT switches have a conservative 6 A @ 125 Vac rating and feature solid silver contacts and new type turret lugs to simplify wiring. High voltage barriers are between terminals inside as well as outside. The one-piece unitized case style houses multiple circuits and easily fits in compact areas. Alco Electronic Products, Inc., Lawrence, Mass.

Circle No. 231 on Inquiry Card.

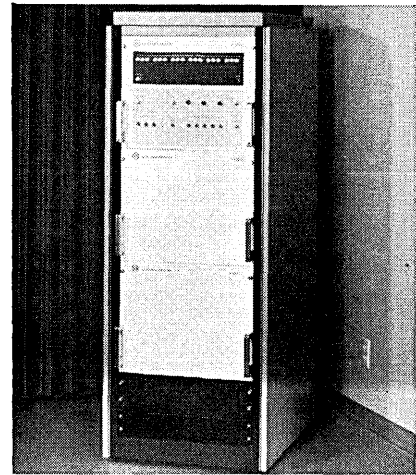


MINIATURIZED PRINTER

The HSP 3608 is capable of operating in a zero "G" hard vacuum environment for prolonged durations and provides 24 columns of printout with 48 characters (ASCII code) and speeds of 10 to 40 characters per second, serially.

Flight version of the 19 lb. unit includes internal cooling system, acoustic enclosure as well as fuel cell power converter. Nominal input of fuel cell power is 40 watts. The complete printer, including mechanism, power supply and electronics, measures 6" wide by $9\frac{7}{8}$ " high by 16" deep. Potter Instrument Co., Inc., Plainview, L. I., N. Y.

Circle No. 233 on Inquiry Card.



RUGGEDIZED GP COMPUTER

A ruggedized version of the 620/i computer is functionally identical to the standard "civilian" computer. Circuit cards are identical; however, the packaging of the cards and the exterior chassis design are completely different. The chassis itself is constructed of heavy aluminum members, assembled into a container 19 inches wide, $15\frac{3}{4}$ inches high, and 24 inches deep. The container is designed to slide in and out of a standard RETMA enclosure on ball-bearing slides.

The assembled unit weighs under 100 pounds. It is designed to meet the shock requirement of 5G, 11 millisecond perpendicular hammer blows and 5G, 11 millisecond horizontal hammer blows. Operating temperatures range from 5° C to 55° C. The non-operating temperature range is -40° C to +75° C. Humidity can range up to 100%. Varian Data Machines, Irvine, Calif.

Circle No. 234 on Inquiry Card.

DATA SET

The FM-300 Data Set is intended for low speed data communications applications up to 300 bits per second as required by such terminals as teletypewriters with EIA interfaces. It is compatible with Western Electric 100 series data sets. With usage of a simple data access box provided by the telephone company, the FM-300 can easily be incorporated onto a dial up network.

The FM-300 will transmit data over 3 KHz voice bandwidth channels conditioned to meet the specifications of type 3002 communications circuits. No conditioning is required. Rixon Electronics, Inc., Silver Spring, Md.

Circle No. 245 on Inquiry Card.

CAPROCON

**The Fairbanks Morse
Caprocon system speeds
the processing of cargo—
automatically,
for United Airlines.**

**A key to the system
is Kleinschmidt**

For high speed in automated communications, there's only one answer: Kleinschmidt.

Take the Fairbanks Morse CAPROCON™ system. At United Airlines Cargo Terminal in Los Angeles, Caprocon, aided by Kleinschmidt data printers, brings new speed and efficiency to the processing of random parcels.

Working at a rate of 800 parcels per hour, Caprocon weighs and measures parcels instantly. It feeds the information on cubage and density to Kleinschmidt data printers. Bills, labels, and shipping instructions are printed out automatically. Result: more efficient palletizing, more economical aircraft loading, faster service than ever before.

Kleinschmidt 311™ Data Printer works at speeds up to 4 times faster than most other teleprinters. And, with 70% fewer moving parts, it's extremely reliable.

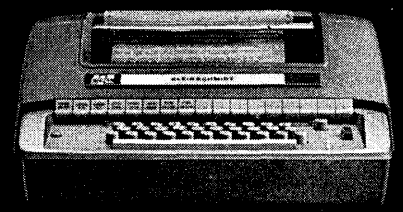
Like other Kleinschmidt data printers, the 311 is compatible with *all* makes of telecommunication equipment. You can fit it directly into your present system or into one being designed for you.

If you have a problem in telecommunications, shouldn't you communicate with Kleinschmidt?

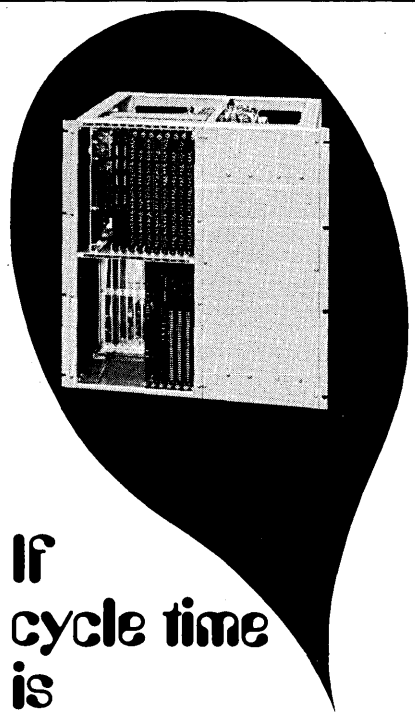
KLEINSCHMIDT

DIVISION OF SCM CORPORATION

DEERFIELD, ILLINOIS 60015 • TELEPHONE: 312 945-1000



CIRCLE NO. 39 ON INQUIRY CARD



If cycle time is the name of your computer game, read the good news:

Toko Woven Plated-Wire Memory System HS-500 is now available.

Toko's woven plated-wire memory planes and stacks are already well known for their low-cost, high-performance characteristics. Now to be marketed for the first time is Toko's complete memory system, with a capacity of 4096 words by 16 bits expandable to 8192 words and 20 bits. Cycle time is a remarkable 500 ns. Other characteristics are 2D organization, destructive read-out operation, and TTL logic level interface. Cost of the system is remarkably low, and fast delivery can be guaranteed.

Besides this standard woven plated-wire memory system, Toko can undertake the manufacture of custom-made systems according to your specifications. Complete technical details from our New York office.

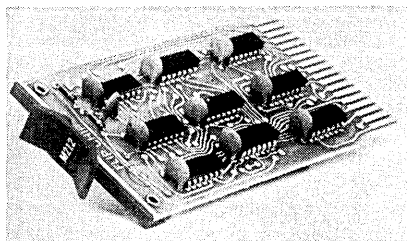


Head Office: 1-17, 2-chome, Higashi-Yukigaya, Ohta-ku, Tokyo, Japan

TOKO N.Y., INC.
350 Fifth Avenue, New York, New York 10001

CIRCLE NO. 40 ON INQUIRY CARD

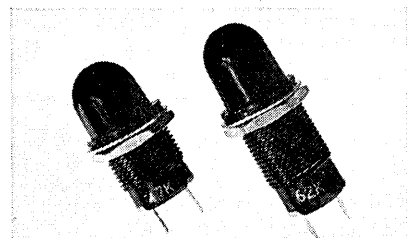
NEW PRODUCTS



SHIFT REGISTER MODULE

The M212 Shift Register is an internally connected left-right shift register/bugger consisting of six edge triggered D type Flip Flops. The M-212 features parallel selection and loading of either of two independent six bit sources, or serial loading and shifting of data in either the left or right direction. Four functional enable inputs define the operation of the module. Vcc: +5 volts. Digital Equipment Corp., Maynard, Mass.

Circle No. 227 on Inquiry Card.



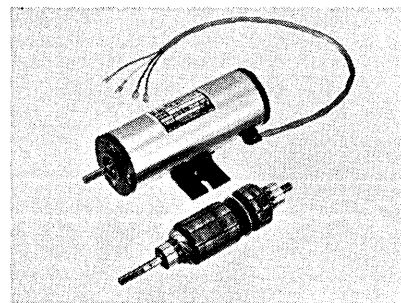
CARTRIDGE INDICATOR LIGHT

An indicator lite that provides up to 25,000 hours of operation at 105-125 volts, Series CM32 Industri-Lite, is available in either long macrodome (CM32-1) or short macrodome (CM32-2) cap styles.

The CM 32-1 is a compact unit that accepts C7A (NE-20) or C9A (NE-2J) long midget flanged base lamps. It is designed for mounting in a 1 1/32" keyed hole in panels up to 1 1/32" thick, and is available with built-in 62K or 27K voltage dropping resistors.

The CM32-2 is similar to the CM32-1, but accepts A1G or A1H short midget flanged lamps, mounts in panels up to 3/32" thick, and is available with built-in 47K or 150K resistors. Both units feature 3/4" center-to-center mounting and black anodized aluminum casings. Chicago Miniature Lamp Works, Chicago, Ill.

Circle No. 258 on Inquiry Card.

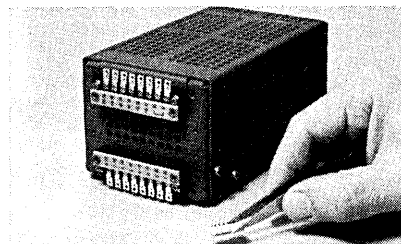


SERVOMOTOR-TACHOMETER

The E-525 is a motor-only version of the earlier 550 series motor-generator, with a continuous rated output of 37 watts (1/20 HP) at 3300 rpm. 18 V rating is standard; 12, 24, 36, 48 and 66 V versions are optional. The motor's acceleration from stall is 10,700 rad/sec², and the unloaded inertial time constant less than 50 ms.

Standard voltage gradient is 14.2 V/krpm, with a maximum unfiltered ripple component of 5% peak-to-peak, at 11 cycles per revolution. A silver generator commutator is used and both motor and generator brush life exceeds 10,000 hours at rated speed. Electro-Craft Corp., Hopkins, Minn.

Circle No. 216 on Inquiry Card.



MODULAR POWER SUPPLY

A modular, dual output power supply, LCD-A Series, is offered in 8 different models with wide voltage output ranges from 0 to 120 Vdc, and is multi-current-rated at 40°, 50°, 60° and 71°C with current ratings to 1 A. The LCD-A features an integrated circuit to provide the regulation system exclusive of input and output capacitors, rectifiers and series regulation transistors. It measures 3 3/16" x 3 3/4" x 6 1/2" and weighs 5 lbs.

The unit is all silicon and convection cooled, with no external heat sinks required. Regulation is 0.01% + 1 mV, line or load. Ripple and noise is specified at 250 μV rms; 1 mV p-p. AC input is 105-132 Vac; 57-63 Hz. Temperature coefficient is 0.01% + 300 μV/°C with external programming resistor. Lambda Electronics Corp., Melville, N. Y.

Circle No. 229 on Inquiry Card.

The beautiful revolution rolls on — Kennedy Model 3110

Meet the newest member of our revolt against high-priced, low-performance recorders — the Kennedy Model 3110 Continuous Magnetic Tape Recorder.

Capable of operating at synchronous speeds up to 25 ips with its high-performance single capstan drive, Model 3110 has read/write rates up to 20 KHz at 800 BPI. Gapping is internally generated. Forward and reverse high-speed search operations can be accommodated at 120 ips. Tape motion is bidirectional with no program restrictions and is under capstan control at all times. Reel size of the Model 3110 is 10½" (2400'). Sound good?

Model 3110 is beautifully simple to interface, and its rugged construction guarantees thousands of hours of trouble-free operation. At \$2800, it's the finest low-cost recorder anywhere. Write or phone for complete information.

KENNEDY CO.

540 WEST WOODBURY ROAD, ALTADENA, CALIFORNIA 91001. (213) 798-0953



CIRCLE NO. 41 ON INQUIRY CARD

san fernando electric manufacturing company

Electronic components
of proven reliability

Aluminum Electrolytic Capacitors

The rugged CAPACITORS by West-Cap that have built-in reliability and durability. Because of their all-welded construction they will withstand more vibration and shock. The elements are made from 99.99% pure etched aluminum foil sealed in high grade aluminum cases.

SERIFS WHC Computer Grade Electrolytic.



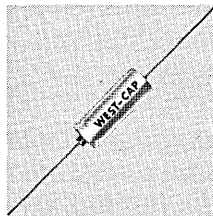
A superior line of energy storage and filter electrolytics which meet all the specifications set by MIL-C-62. In addition, this series will meet all the standard telephone quality standards set by the telephone industry. This electrolytic will meet the most exacting ripple standards.

**Ratings: 200 mfd to 100,000 mfd
from 5 VDC to 150 VDC
Voltages in excess of 150 VDC
to 500 VDC on special order**

SERIES MAC Axial Lead Electrolytic.

They are available in miniature size with 1/4" x 5/8" case and larger.

**Ratings: 2 mfd to 70,000 mfd
from 3 VDC to 150 VDC**



The manufacturing process is completely quality-controlled in West-Cap's modern new facility in the Tucson International Airport Industrial Park. This facility was designed and equipped primarily for the manufacture of high quality electrolytic capacitors at competitive prices.

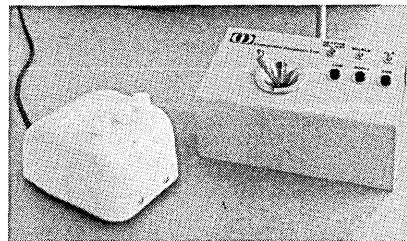
Call your representative of West-Cap high reliability components, or contact West-Cap Arizona, where service and quality count.

WEST-CAP ARIZONA

SUBSIDIARY OF SAN FERNANDO ELECTRIC MANUFACTURING CO.
2201 EAST ELVIRA ROAD, TUCSON, ARIZONA 85706

CIRCLE NO. 42 ON INQUIRY CARD

NEW PRODUCTS



GRAPHIC INPUT DEVICES

Two graphic input devices, the Mouse and the Joystick, are to be used with ARDS and similar CRT display systems. The Mouse is a simple two-dimensional controller for positioning a cursor on the screen. Moving the Mouse around on any flat surface causes the cursor to follow in an identical manner. Three buttons are mounted on the top of the Mouse which allow the user to transmit the cursor position or its vector value to the computer.

The Joystick is an alternate graphic input positioning device. Like the Mouse, it provides analog voltage to control the cursor. The same three push-button controls for generating graphic input messages are provided on the Joystick housing. In addition, switches are provided for selecting solid line input, dotted line input, and returning cursor control to the computer. Computer Displays Inc., Waltham, Mass.

Circle No. 225 on Inquiry Card.

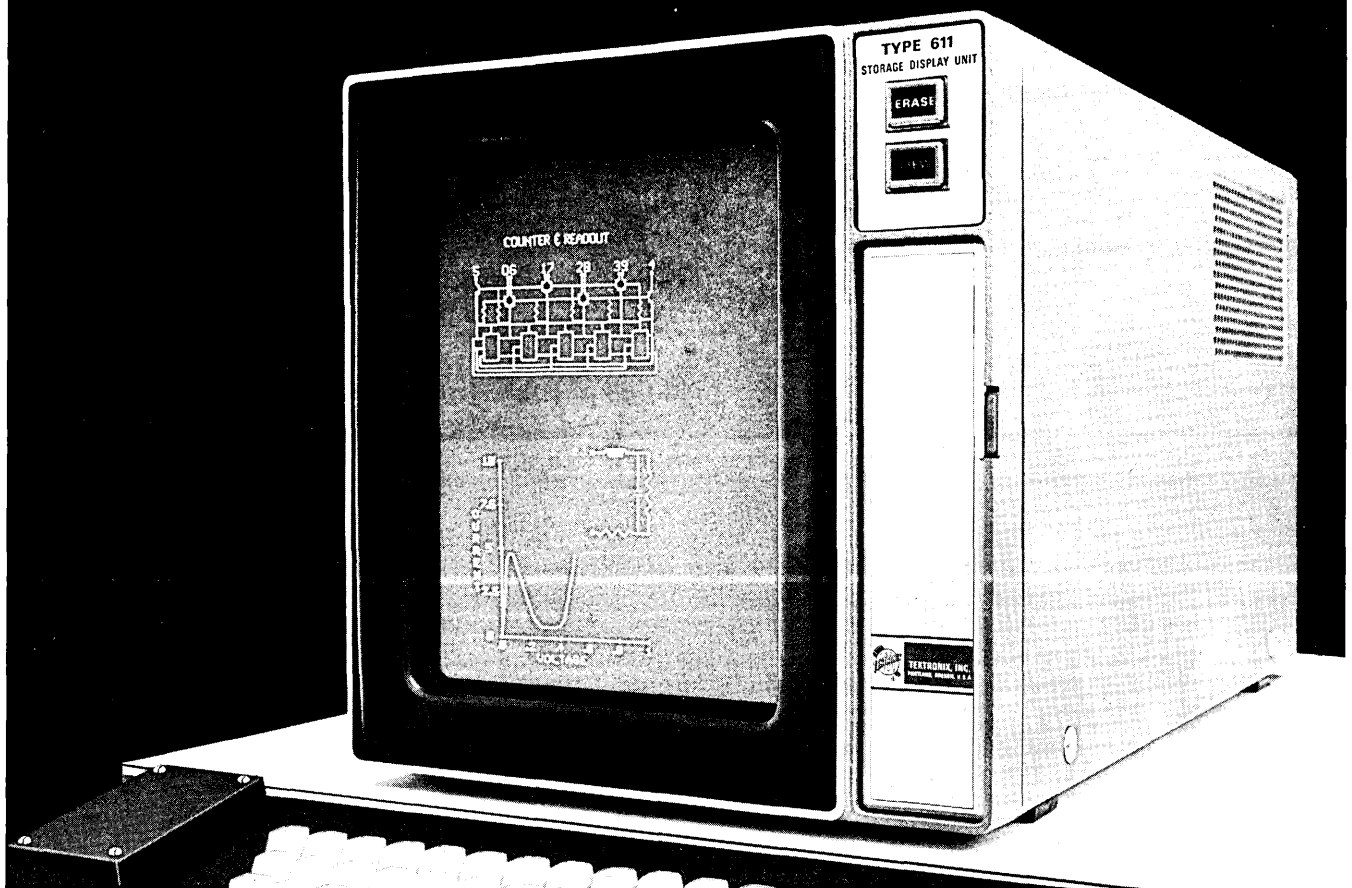
CRT DISPLAY

The SYS-2113-10 CRT display adds instant graphic display capability to the SYS-2113 data acquisition and control system, used in conjunction with IBM 1130 computers for time-sharing in process monitoring and control.

The SYS-2113-10 displays data on a 10-inch screen in a brief portion of the time required to produce the information by conventional on-line plotters. Graph after graph can be quickly projected while adjusting parameters and changing variables. Or, as an alphanumeric display, with an associated keyboard, it performs data retrieval, test formatting, etc. An optional joy stick permits display position control and polaroid cameras are available for hard copies. SYS Associates, Inc., Fort Lee, N. J.

Circle No. 244 on Inquiry Card.

Information Displays Without Refreshing



CRT Storage Affords flicker-free displays of both complex graphics and high-density alphanumeric

The Type 611 Storage Display Unit is designed to function as a readout device for computer consoles and remote terminals. With X, Y and Z inputs provided by peripheral equipment, this new instrument produces displays of high density alphanumeric and complex graphic information without drift or annoying flicker.

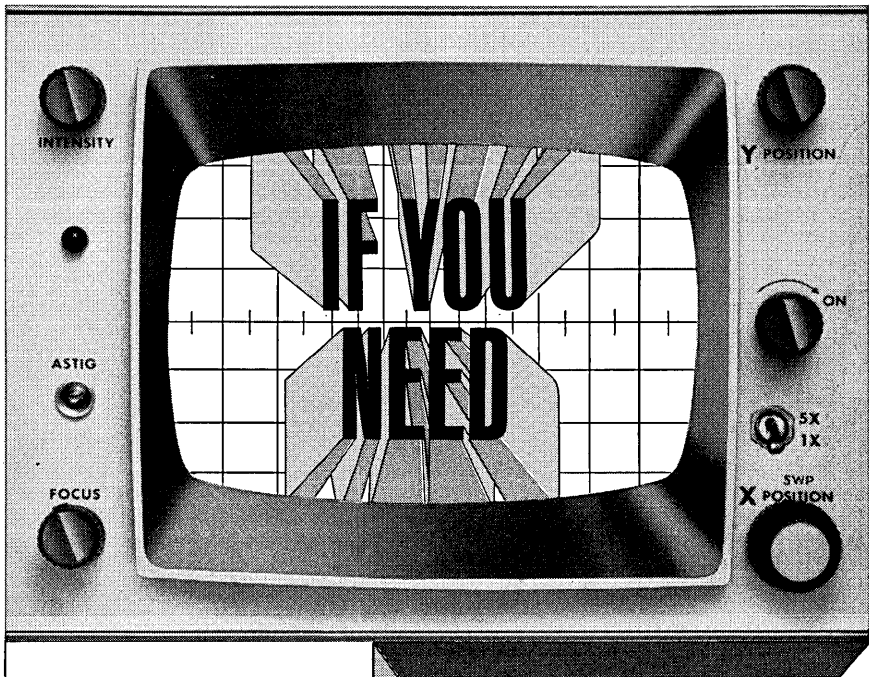
The Type 611 Storage Display Unit features an 11-inch, magnetically deflected, bistable storage display tube. This new storage tube offers high information density and excellent resolution on a 21-cm x 16.3-cm screen. 4000 characters, 90 x 70 mils in size, may be clearly displayed with good spacing. Resolution is equivalent to 400 stored line pairs along the vertical axis and 300 stored line pairs along the horizontal axis. Dot settling time is $3.5 \mu\text{s}/\text{cm} + 5 \mu\text{s}$ and dot writing time is $20 \mu\text{s}$. Time required to erase and return to ready-to-write status is 0.5 seconds. Operating functions are remotely programmable through a rear-panel connector. A "Write-Through" feature provides an index to the writing beam position without storing new information or altering previously stored information.

Type 611 Storage Display Unit \$2500
U.S. Sales Prices FOB Beaverton, Oregon

For a demonstration, contact your nearby Tektronix field engineer or write: Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97005.

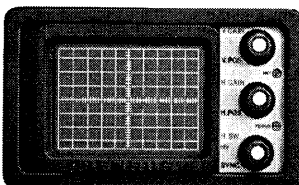
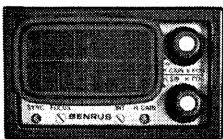


CIRCLE NO. 43 ON INQUIRY CARD



**if you need
a custom
designed
CRT DISPLAY—
one of
our 3,110
variations
might do...**

spedcor
Lavoie
Analab
Benrus
INSTRUMENTS
DIVISION



(And that's not including variations due to options!)

With the Benrus solid state CRT Display, you select the necessary panel height—choice of 3½", 5¼" and 7", as designed to exact modular dimensions Select your own amplifier characteristics in a range of bandwidths and sensitivities for either or both channels And a choice of 40 speed ranges in either "A" or "B" channel sweep Result? A custom-assembled, off-the-line, quality-manufactured unit to your own exacting requirements.

Request catalog 802 for complete details.

ALSO AVAILABLE WITH "BUILDING BLOCK" OPTIONS...the Benrus line of ultra-compact, solid state monitor oscilloscopes for panel installation. A wide range of amplifier, sweep and trigger plug-ins make economy without compromise possible.

Ideally suited for multiple installations because of their modest heat dissipation requirements, the small size, weight and cost of these scopes also makes them adaptable for use in lab, test and inspection...anywhere that these qualities are more important than great versatility.

spedcor electronics, inc.

Lavoie Analab Benrus Instrument Division
70-31 84TH ST., GLENDALE, N. Y. 11227 • 212-894-8100

CIRCLE NO. 45 ON INQUIRY CARD

NEW PRODUCTS

MAGNETIC TAPE SYSTEM

Model MTS 10/1130 is a complete magnetic tape system tailored expressly to IBM 1130 requirements. Completely plug compatible, the MTS 10/1130 provides data transfer rates up to 20K Hz, and 2400 foot storage capacity.

The system utilizes the Model 3110 tape transport, together with interface matching 1130 I/O. The interface will handle one or two transports; to add a second transport it is merely plugged into an existing connector in the interface unit.

Provided as standard in the MTS 10/1130 are two byte per word or packed operation (7 channel, 1800 mode), character assembly/disassembly, record chaining, and parity check. Connections are made to the storage access channel for the greatest flexibility of operation. Tape format is completely IBM-compatible, with either 556 bpi, 7-track or 800 bpi, 9-track available. Kennedy Co., Altadena, Calif.

Circle No. 239 on Inquiry Card.



OPERATIONAL AMPLIFIERS

A fast settling time amplifier, the FST-100, for high speed A/D conversion and multiplexed data acquisition systems, provides a typical gain of 500,000, with 300,000 minimum guaranteed. Stable unity gain frequency of 10 MHz and minimum common mode rejection of 90 dB are specified. It has a minimum slewing rate of 20 V/μs, yet its unity gain (inverting) settling time to 0.01% is less than 1 μs for a 0 to ±10 V step (output), with no appreciable overshoot or ringing. It also features low noise and drift characteristics. Control Logic, Inc., Natick, Mass.

Circle No. 232 on Inquiry Card.

The Friden 1150 Digital Printer: fast, reliable— and inexpensive.

The Friden* 1150 Digital Printer has a printing speed of 50 characters a second.

Because it has fewer moving parts than ordinary medium-speed printers, it is easier to maintain. This means less downtime for your OEM product. The unit contains a single 20-character print wheel and a synchronized print hammer. Both are driven across the tape from right to left at a uniform speed.

The hammer's short impact time ensures quality printing from the continuously rotating wheel. Your output looks good and is easy to read. And we have even eliminated ribbons with a disposable ink roller.

Logic requirements are simple, making it easy for you to integrate the 1150 into your OEM product.

The 1150 is a completely tested and *proven* printer—

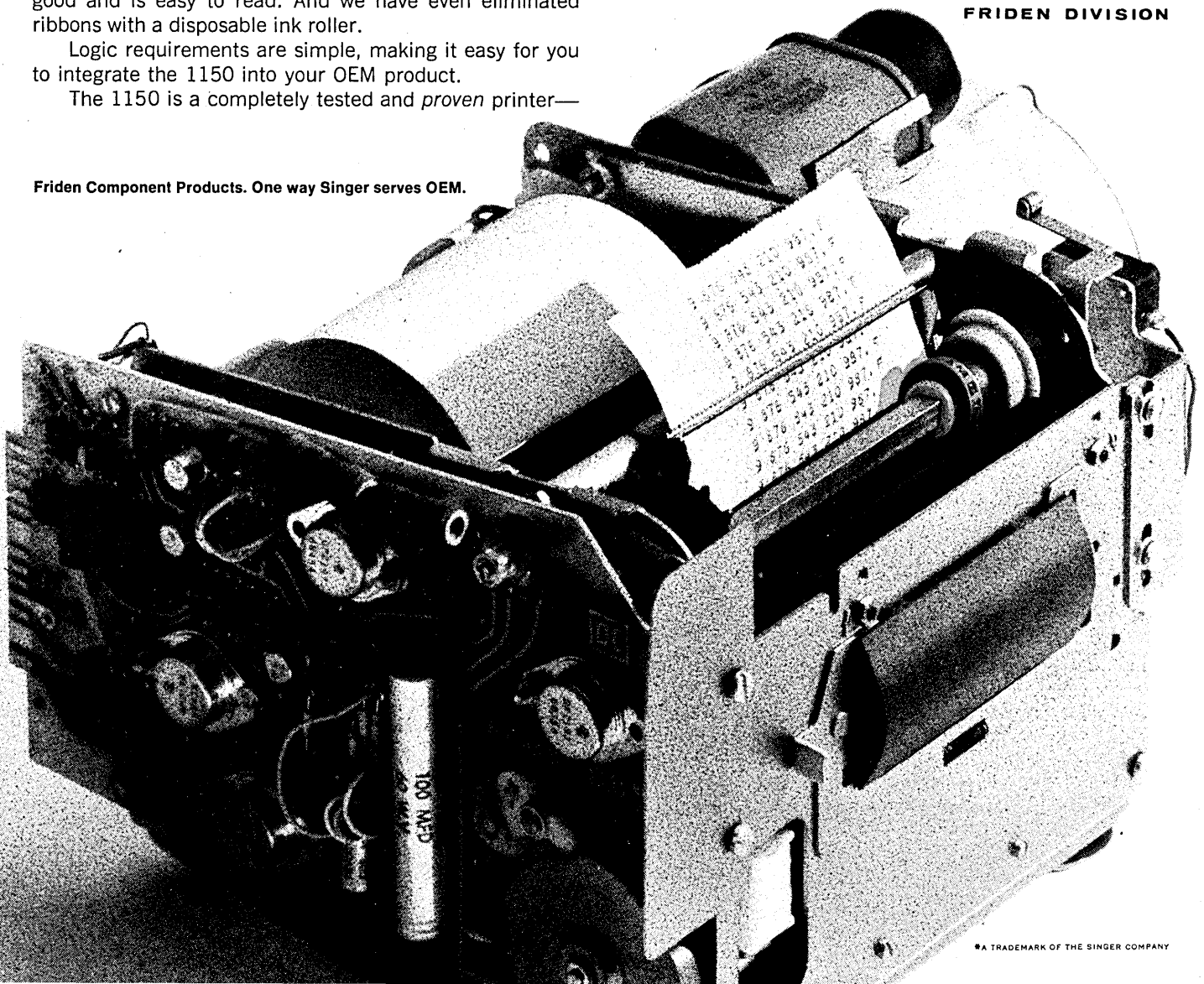
a vital component of Friden electronic printing calculators for nearly two years. And Singer's Friden Division provides maintenance backup throughout the world.

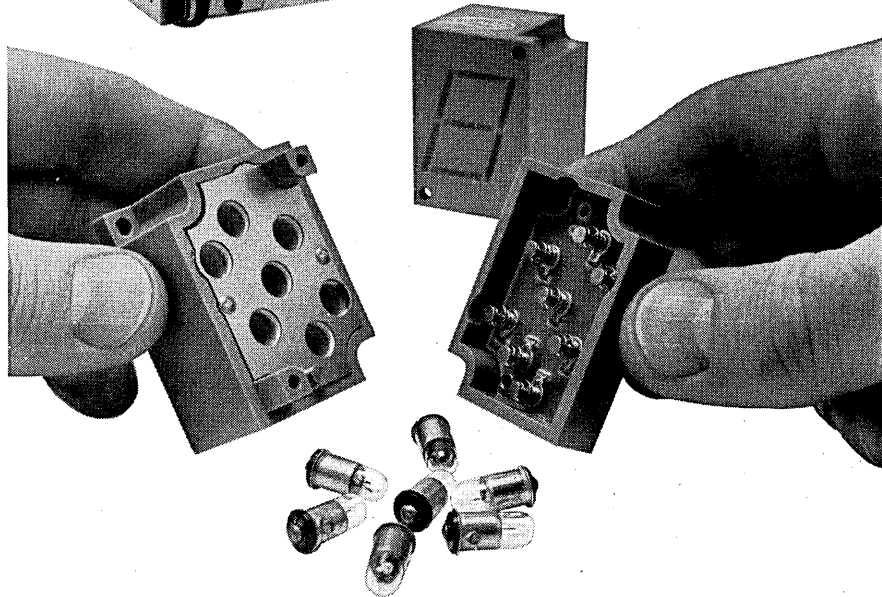
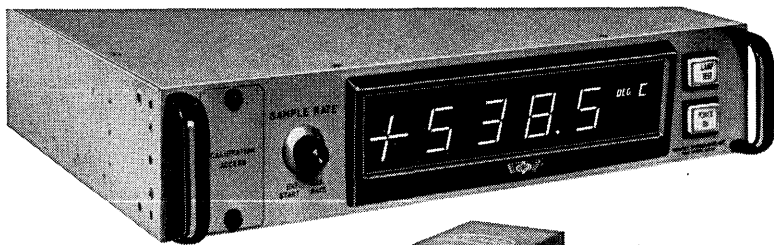
With its low initial cost and desirable operating features, the 1150 gives you a price/performance ratio that is unique among OEM printers.

We'd like you to have complete specifications. Just write Friden Division (Component Products), The Singer Company, San Leandro, California 94577. Ask for Specification 1001.

SINGER
FRIDEN DIVISION

Friden Component Products. One way Singer serves OEM.





What makes low-cost Dialight readouts so reliable and easy-to-read?

Reliable because of simple module construction and long life lamps. Designed for use with neon or incandescent lamps to meet circuit voltage requirements. Easy-to-read from any viewing angle. 1" high characters are formed by unique patented light-gathering cells, and may be read from distances of 30 feet. Sharp contrast makes for easy viewing under high ambient lighting conditions.

Dialight Readout Features

1. Operate at low power.
2. 6V AC-DC, 10V AC-DC, 14-16V AC-DC, 24-28V AC-DC, 150-160V DC or 110-125V AC.
3. Non-glare viewing windows in a choice of colors.
4. Available with RFI-EMI suppression screen.
5. Available with universal BCD to 7 line translator driver.
6. Can be used with integrated circuit decoder devices now universally available.
7. Caption modules available; each can display 6 messages.

Send for catalog

Catalog-folder contains complete specifying and ordering data on numeric and caption modules, translator drivers, mounting accessories. Dialight Corporation, 60 Stewart Avenue, Brooklyn, New York 11237. Phone: (212) 497-7600.

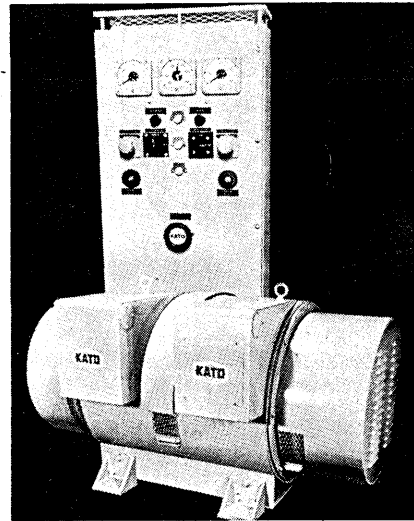
DIALIGHT

CIRCLE NO. 47 ON INQUIRY CARD



DT-126

NEW PRODUCTS



MOTOR-GENERATOR SYSTEMS

An expanded line of load isolation motor-generator sets, typically consists of a motor-generator in common frame, common shaft construction, with complete controls for both motor and generator within a NEMA type steel enclosure of either free standing or wall mounted.

The M-G set illustrated has an input of 220/440 volt, 3 phase, 100 H.P. synchronous motor with a generator output of 62.5 KVA, 120/208 volt, 400 cycle, 3 phase. Both motor and generator have separate rotating brushless exciters to supply the 40-pole motor field and the 6-pole generator field. Output voltage is regulated within $\pm 1\%$ of rated output voltage. Both induction and synchronous motor units can be supplied in both common frame and in separate frame direct coupled drive. Kato Engineering Co., Mankato, Minn.

Circle No. 218 on Inquiry Card.

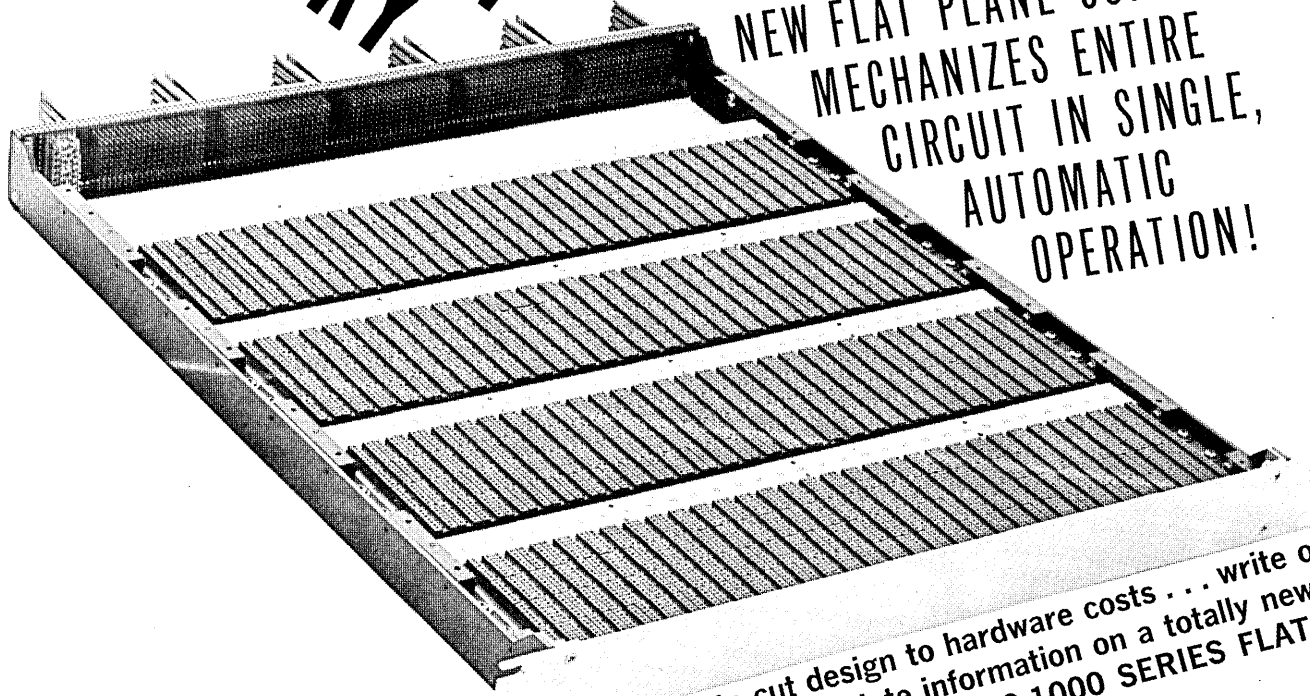
KEY-TO-TAPE SYSTEM

The Mark I key encoder, compatible with any major manufacturer's computer, permits the key-punch operator to determine exactly what data is being programmed. It also indicates errors automatically, and points out the nature of the error, allowing instant correction.

Its equipment includes a typewriter-size encoder which records on cassette tape, and a translator, which pools the cassette's information on computer tape. Cybercom Corp., Sunnyvale, Calif.

Circle No. 242 on Inquiry Card.

INSTANT CIRCUITRY



NEW FLAT PLANE CONCEPT
MECHANIZES ENTIRE
CIRCUIT IN SINGLE,
AUTOMATIC
OPERATION!

Learn how to cut design to hardware costs . . . write or call today for complete information on a totally new design concept . . . the FPC-1000 SERIES FLAT PLANE.

Here is a new approach to the whole problem of circuit design...the incrementally expandable—from 10½" to 6 foot depth—Series FPC-1000 Flat Plane. This unique carrier permits mechanization of entire circuit designs in a single, automatic computer-controlled operation. It eliminates the use of printed circuits, manual wire-wrap, and bread-boarding...it has reduced initial design and engineering costs by as much as 70%.

If you have your own circuit designs, we have proprietary software available and operational that can mechanize them . . . or, we have an exceptional library of proven circuits and the total means to mechanize them to meet your specific requirements.

Whether its your design or ours that is to be mechanized, the American Computer Technology FPC-1000 Flat Plane will offer the shortest possible time lag between concept and operational hardware. A significant cost reduction factor is realized even by equipment manufacturers who produce in small quantities.

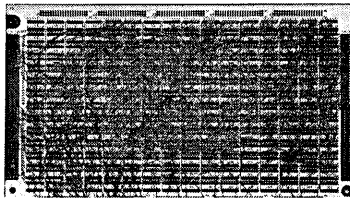
**AMERICAN COMPUTER
TECHNOLOGY, INC.**
8740 SHIRLEY AVENUE
NORTHRIDGE, CALIFORNIA
91324
(213) 886-7440

CIRCLE NO. 48 ON INQUIRY CARD

Cut Here

WIRING PROBLEM SOLVER

(or Short Form RFQ)



There's a Product Improvement Wiring Termination System made for any high density wiring application — just fill out this form describing your production needs and we'll fire back our recommendations plus current literature.

After all, who's better qualified to assist you in making a machine selection? Product Improvement developed the first practical semi-automatic system, is the only source for both moving-table and moving-tool designs, and has more units in the field than all others combined. Now — latest models are available with manual, semi-automatic and automatic terminating heads.

TELL US YOUR APPLICATION—

TYPE OF WIRE

- SOLID
- STRANDED
- PAIRS
- COLOR CODED

PANEL SIZE(S)

- 18"x18" OR UNDER
- OVER 18"x18" BUT LESS THAN 22"x36"
- OVER 22"x36"

TYPE OF TERMINATION PRESENTLY USED

- WRAP
- CLIP-ON
- TAPER PIN INSERTION
- SOLDER

AVERAGE WIRES PER PANEL _____

PRODUCTION NEEDS

- ONE OF A KIND
- REPEATS, BUT FEW
- MULTIPLE RUNS

PRESENT WIRING METHOD

- MANUAL
- OTHER _____

PRESENT WIRING COSTS

\$ _____, PER WIRE

Name _____ Firm _____

Address _____ City _____ State _____ Zip _____

Mail to: Product Improvement Corporation, 150 E. Stevens Ave.,
Santa Ana, Calif. 92707

NEW PRODUCTS

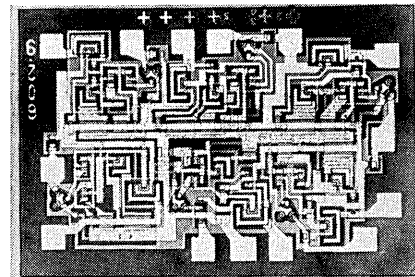
CORE MEMORY SYSTEM

The ICM-160 is a 4,096-word memory, available with 8, 12, or 16 bits per word, and measures 2¾ by 5 by 9 inches. The system is field expandable to other word and bit sizes on a modular basis. Full cycle time is 1.6 µs with an access time of 550 ns

The system is self-contained and includes an address register, internal timing and control, sense amplifiers, and integrated circuit X-Y selection switches. All logic, addressing, decoding, control, X-Y selection switches and sensing functions use integrated circuitry which provides a calculated MTBF of 40,000 hours.

The memory is both electrically and mechanically compatible with other Honeywell Micro-Pac systems, and can be operated from common system power supplies. Honeywell Inc., Computer Control Div., Framingham, Mass.

Circle No. 243 on Inquiry Card.



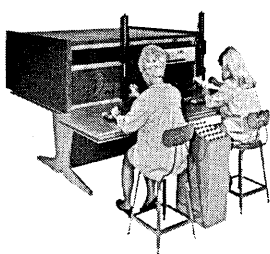
HEX 1-INPUT INVERTER

A Hex 1-input inverter, designated SG370 series in the SUHL I family and SG380 series in the SUHL II line, contains six gates consisting of a single-input inverting gate with a cascade pull-up output network. Each gate functions as a NAND element in positive logic, and each input is protected by a clamp diode.

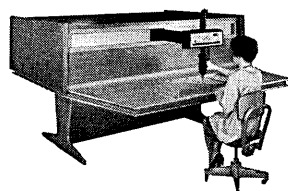
Both SG370 and SG380 series are characterized by high speed at low power, high noise immunity, and high capacitance drive. The SG370 circuits operate at 12 ns typical propagation delay and 22 mW power dissipation per gate function. The SG380 devices are rated at 6 ns and 22 mW.

The ICs are available in full military (-55°C to +125°C) or industrial (0°C to +75°C) temperature ranges, and are available in 14-lead hermetic flat pack or dual-in-line ceramic packages. Sylvania Electric Products, Inc., Semiconductor Div., Woburn, Mass.

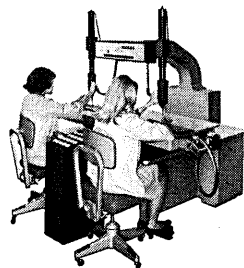
Circle No. 236 on Inquiry Card.



Model 2302—A medium-sized moving head system with dual wiring tools. Single tool head also available.



Model 2701—A moving head system for wiring large panels; also available with dual tool heads.



Model 3182—A small moving table system with dual tool heads; also available in a single-headed version.

All models are available with either incremental or absolute type numerical control units. Various options include side loading or end loading bits, remote readout, foot switch control, wire bins with indicator lights, and card reader input. Product Improvement will also provide all programming and start-up services you may require.

PRODUCT IMPROVEMENT CORPORATION
A SUBSIDIARY OF CAVITRON CORPORATION
150 E. Stevens Avenue, Santa Ana, California 92707
CIRCLE NO. 49 ON INQUIRY CARD





Sounds obvious, doesn't it?
 But in too many companies
 it just isn't so . . . there's no real
 room for an innovative person
 —and his company—to grow.
 The Honeywell Man is **expected** to
 contribute. That's why in 10 years time,
 Honeywell **has grown**; from 200 to
 more than 10,000 people.
 Honeywell is large enough to have the
 facilities a technical specialist might
 want or need, but is small enough that
 everyone can make his achievements
 known. That's another rare thing about
 Honeywell—it's true.
 Honeywell is looking for
 people who want to get
 involved, who will
 contribute in the
 following areas:

HARDWARE SPECIALISTS

- Systems Design
- Communications Subsystems Design
- Peripheral Control Design
- Processor Design
- Logic Design
- Maintainability Design
- Advanced Memory Design
- Circuit Design
- Diagnostic Programming
- Design Automation

*Please forward your resume to
 Mr. Jack Wermuth.*

The Other Computer Company:
Honeywell

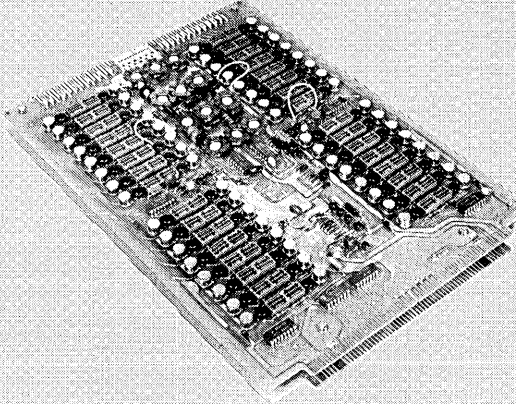
200 Smith Street, Dept. CD-5 Waltham, Massachusetts 02154

Opportunities exist in other Honeywell Divisions. Send resumes to F. E. Laing, Honeywell, Minneapolis, Minnesota 55408. An Equal Opportunity Employer.



MICRO SYSTEMS INC.

Low Cost · 900 Nanosecond



CORE MEMORY

MODEL 140

- 900 nanosecond full cycle time.
- 300 nanosecond access time.
- Wide operating margins.
- Plug-in modularity.

The MSI-140 is a field tested memory module forming a basic low cost building block for implementation of custom memory systems. Modularity allows for a wide range of word capacity/word size configurations.

Address input, data input/output, mode control, and power are supplied externally via a pc connector (specified by the user), providing maximum system flexibility with minimum interface cost. Experienced engineering assistance is available from MSI to support special integration requirements.

Standard memory systems using the MSI-140 are also available. These systems are plug-in expandable and provide such optional features as internal data and address registers, timing, power, and self-test.

Specifications

Size	4096 x 8, 9, 10
Construction	3 wire, 3D, continuous stack wiring
Cycle Time	900 nanoseconds
Address Mode	Random access
Interface	TTL Integrated

WRITE FOR COMPLETE DETAILS IN BULLETIN 140.

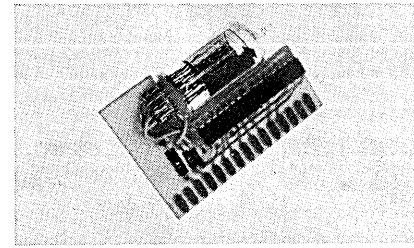


MICRO SYSTEMS INC.

644 East Young St., Santa Ana, California 92705 • (714) 540-6730

CIRCLE NO. 51 ON INQUIRY CARD

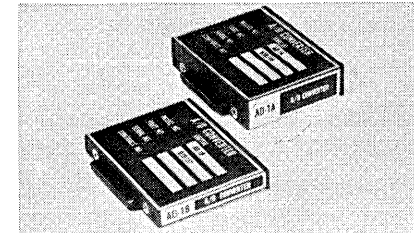
NEW PRODUCTS



DECIMAL DISPLAY UNIT

The DM500 series decimal displays are self-contained plug-in units. The DM519 includes a decade counter with BCD outputs available to the connector as well as the decoder/driver circuit. The DM529 accepts BCD inputs for decoding and display. Computer Products, Inc., Ft. Lauderdale, Fla.

Circle No. 252 on Inquiry Card.



A-TO-D CONVERTER

A series of miniature analog to digital converters typically measure 2.0" x 2.62" x 2.125" with dc-dc converter. Final package outline and dimensions are variable to match individual requirements.

Specially designed for rugged environmental conditions, the A/D converters will withstand temperatures at altitudes from sea level to outer space, from -54° to 100°C; shock of 100 g on any axis; humidity of 0-95% relative, with condensation to 100°F; sine vibration of 40 G, 50 to 2000 Hz, any axis; and random vibration of 3.2 g²/Hz to 3000 Hz, any axis.

Available models have resolution ranges from 6 to 10 bits and are either bi-polar or uni-polar. Power consumption is 0.5 watts per unit for the high speed R-2R types, and less than 0.3 watts for high speed current summing types at 28 Vdc. Radix Telemetry Corp., Anaheim, Calif.

Circle No. 256 on Inquiry Card.

COLLINS' NEW DATA PROGRAM CREATING NEW OPPORTUNITIES

Collins' C-8500 C-System gives users the first completely integrated system with virtually unlimited expansion capability.

This new concept in computer applications is creating exceptional career opportunities for:

DATA COMMUNICATION ENGINEERS (Digital)

Dallas/Cedar Rapids/Newport Beach

To perform advanced state-of-the-art R&D and production improvement utilizing microelectronic components applied to digital data communication and/or data processing equipment. Project responsibilities from design through production release. Experience desired in analog and digital circuit design of active filters, D. C. amplifier modulators, oscillators, digital logic and signal detectors. Prime responsibility would include the use of these microelectronic components and circuits in the design of digital data communications equipment. Computer facilities available for analytical engineering design. Electronic, mechanical and analytical support groups are available to assist the system and equipment project engineers. BSEE or MSEE required. Advanced preparation and/or 4 years experience desired.

LOGIC DESIGN ENGINEERS

Dallas/Cedar Rapids/Newport Beach

To perform logic design of fourth generation computer peripheral equipment utilizing the latest microelectronic components. Responsibility would include design through production release. Capabilities should include experience directly related to the logic design of digital subassemblies for computer equipment. BSEE and 2 years experience required.

MOS INTEGRATED CIRCUIT APPLICATION & DESIGN ENGINEERS

Newport Beach

Degree, MSEE preferred. Capable of working with Collins equipment designs and application of MOS integrated arrays. Will be responsible for design and coordination of the fabrication of these circuits. Experience in digital and logic design required.

HARDWARE DIAGNOSTIC PROGRAMMERS

Dallas/Cedar Rapids

This position involves diagnostic programming for factory and field checkout and maintenance of digital hardware utilized in large multiprocessor computer systems. Applicants must have the ability to develop hardware test plans, write and document off-line and on-line diagnostic programs, and assist in specifying logic required for diagnostic aids. BSEE degree, plus a minimum of 1 year applicable experience is required.

MEMORY DESIGN ENGINEERS

Cedar Rapids

Duties will involve the design and development of high-speed random access memory systems, including storage media, internal timing circuits, data and address buffer register, parity circuits and associated logic. Requires BSEE degree, plus a minimum of 1 year applicable experience.

TECHNICAL WRITERS

Cedar Rapids/Dallas/Newport Beach

Duties will involve preparation of original instruction manuals and documentation for Collins systems used in both industry and the military. Applicants must have a strong electronics theory background and previous technical writing experience. Degree desirable.

COMPUTER INSTRUCTORS

Cedar Rapids/Dallas/Newport Beach

To develop and teach courses in computer engineering design aids, MOS logic design and computer hardware and software. Instructors for engineering design aids and MOS logic design courses should have a Science degree and teaching experience. Software instructors should have a degree, teaching experience and preferably some programming experience. Hardware instructors should have a degree and teaching experience on digital computers. Applicable experience will be considered in lieu of degree for the hardware and software positions.

Please send resume in confidence to Manager of Professional Employment, Dept. #100, Collins Radio Company, Dallas, Texas 75207; Cedar Rapids, Iowa 52406 or Newport Beach, California 92663.



an equal opportunity employer

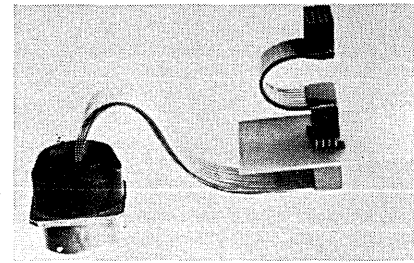
NEW PRODUCTS

SYNCHROS AND RESOLVERS

A group of short length Size 8 synchros and resolvers, identified as the 990 Series, are $\frac{3}{4}$ inch in diameter and less than an inch long. These components include control transmitters, control differential transmitters, control transformers, a transolver, and an RC type resolver. All are housed in an

envelope having the same basic dimensions, and occupy about $\frac{1}{2}$ cubic inch of volume. Operating at 400 Hz, all models with the exception of CX types require an input voltage of 11.8 V. CX's require 26 V. Available in accuracies of ± 5 , ± 7 , or ± 10 minutes maximum error from electrical zero, all operate through a temperature range of -55°C to $+125^{\circ}\text{C}$, weigh 1.2 oz, and exhibit a rotor moment of inertia of 0.6 gm cm^2 . Kearfott Div., Singer-General Precision, Inc., Little Falls, N.J.

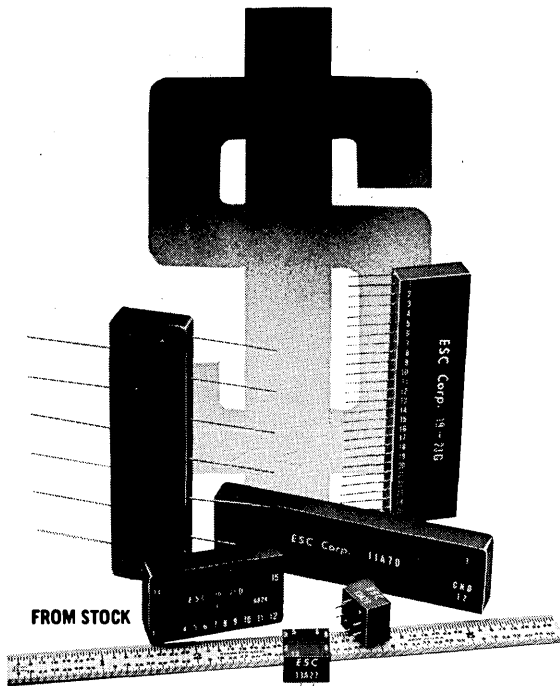
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FLEX-CABLE CONNECTOR SYSTEM

A flex-cable connector system provides input/output to wire-wrap panels and wire-wrap connector frames with .100 contact centers. A male plug with flat, flexible cable attached, interfaces with a receptacle which can be mounted on a wire-wrap panel or circuit board and has .025 square wire-wrap posts which project thru the panel or circuit board. A female plug with flexible cable attached plugs onto the .025 square wrappable posts of the receptacle, leaving space for 2 levels of wrapped wire after engaging. Digital Sensors, Inc., Los Angeles, Calif.

Circle No. 260 on Inquiry Card.



NEW! LOW COST DELAY LINES FOR DIGITAL CIRCUITRY

ESC's new Digit-Line series of epoxy molded delay lines contains 17 different types covering a range of delays from 7 to 1000 nanoseconds. This series exhibits relatively fast pulse rise time, exceptionally fine pulse fidelity and low attenuation. Impedance is approximately 100 ohms. Most important is the versatility of these units due to their fine resolution taps, or adjustable sections. The smallest unit in the series is only .490" L x .490" W x .370" H. All of the units will meet the most frequently encountered military specifications. ESC's staff of design engineers will also be pleased to help you solve your custom delay line and filter problems. Write today for our comprehensive brochure.

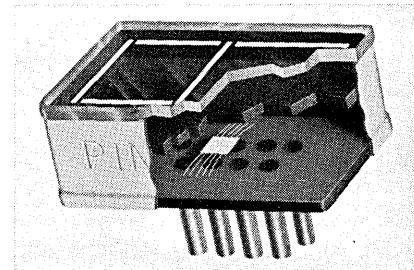


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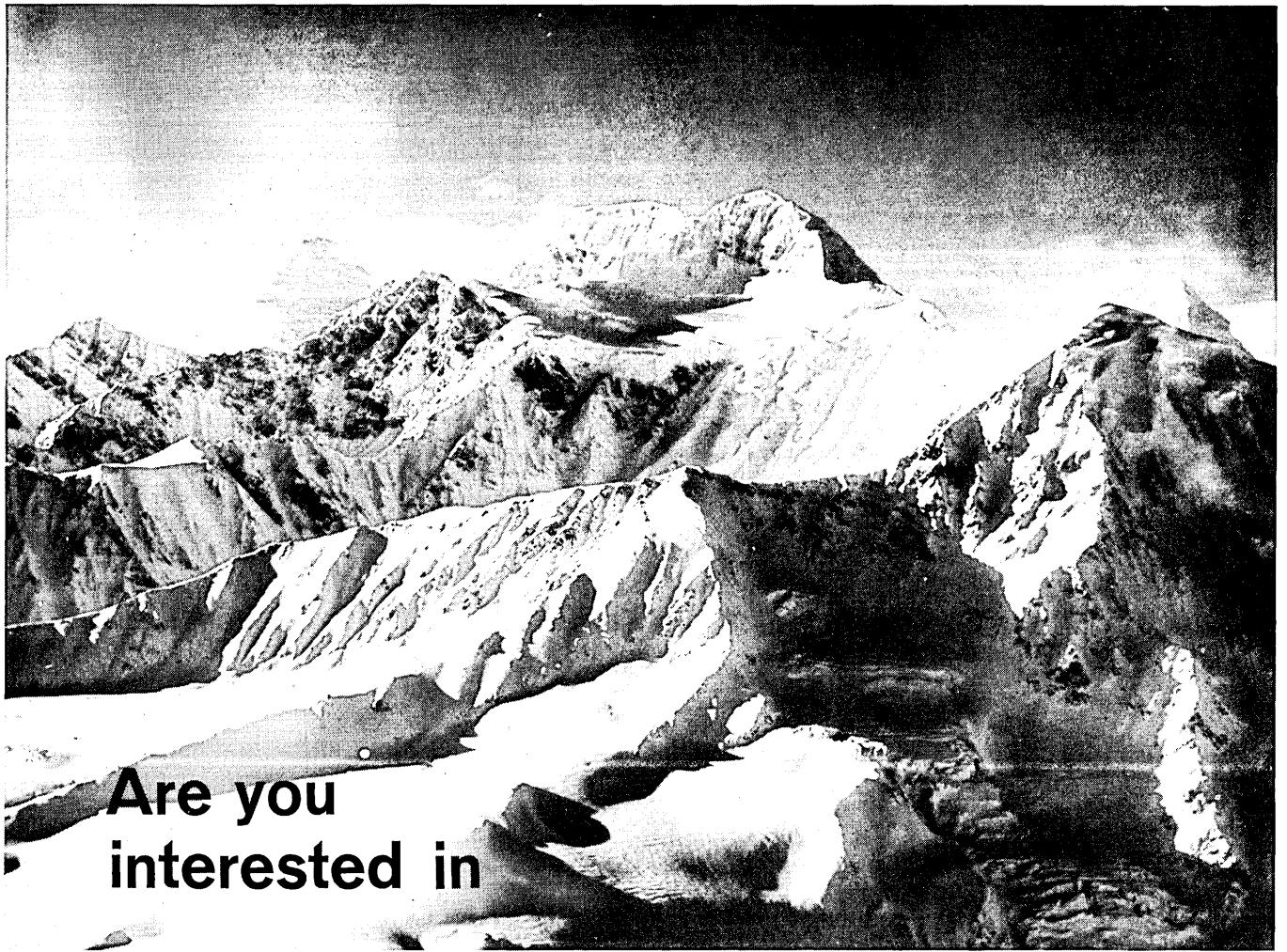


DECODER/DISPLAY SYSTEM

The basic MIDGI-LITE® M Series is a seven segment, direct viewing incandescent tungsten filament (light bar) display. The light bars have a design life of 100,000 hours per segment, or 11 years of continuous data display. Model M6-1C eliminates a separate decoder package. And performs all translation from 8-4-2-1 BCD code to seven segment display within the readout head; with a total combined depth of only $\frac{3}{16}$ ".

Design features include: combined decoder/display power, less than $\frac{1}{2}$ watt; 250 ft. lambert brightness per segment; six of the coder-lites can be stacked in less than one square inch; digital character height is $\frac{5}{16}$ "; military specification performance: MIL-E-5400 Class II. Pinlites Inc., Fairfield, N. J.

Circle No. 214 on Inquiry Card.



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Are you slogging along the trail of computer problems you or others have solved many times before? Would you like to take a crack at **advancing** the technology of

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- Computers for Controlling Advanced Radar Systems
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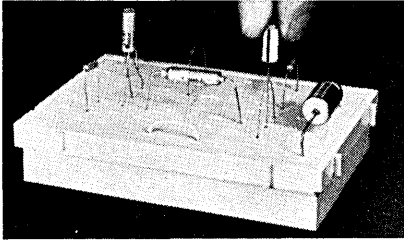
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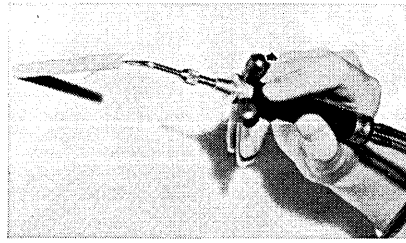
NEW PRODUCTS



ELECTRONIC BREADBOARDING KIT

An electronic breadboarding kit has leaf spring contact points which directly accept component leads up to 0.040 inches in diameter. The S-DeC measures 4½ x 3¼ x ¾ inches and has 14 independent junctions with 70 numbered connection points. Wear and tear on components and board is minimal and flexibility is a main feature of the system. Intratec Div., British Aircraft Corp. (USA), Inc., Arlington, Va.

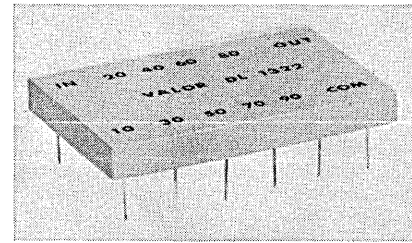
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MINIATURE TORCH

A tiny torch which welds metal smaller than .002" wire and up to 16 gauge steel, called "The Little Torch", uses oxygen and a fuel gas (acetylene, hydrogen, LP-Gas or natural gas) to produce flame temperature to 6300°F. It operates at pressures of 2 to 4 psi, and uses gas at the rate of .023 to 2.54 cfh. The Little Torch is equipped with five different sized tips which swivel 360° for complete handling ease. The two smallest tips (#1, #2) have sapphire jeweled orifices for extra durability and precision performance. These jeweled orifices prevent oxide contamination in the joint. Instrument Div., Tescom Corp., Minneapolis, Minn.

Circle No. 222 on Inquiry Card.



CHIP DELAY LINE

NPC series lumped-constant nano-second chip delay line features typical clock rates of 10 nanoseconds. Designed for printed circuit board mounting with all standard sizes having tap capability at any or all 2.5 ns increments, the NPC series also features low profile packaging (.135 max.). Length is from .815" to 2.615", and width .615".

The NPC series has a cut-off range of 125 MHz, with output ripple 3% typical, and output overshoot 5% typical. This series will meet or exceed the requirements of MIL-Std 202 for shock, vibration, temperature, moisture resistance, life and humidity. Valor Electronics, Inc., Costa Mesa, Calif.

Circle No. 226 on Inquiry Card.

INTERFACING A DRIVE WITH A COMPUTER?

RESPNSYN® STEPPING MOTORS OFFER THESE ADVANTAGES...

- LOW INERTIA** — Basic design eliminates flywheel effect of heavy rotors found in conventional motors.
- HIGH RESOLUTION** — Up to 2,000 steps per revolution for small step angle positioning with a high degree of accuracy.
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- HIGH RESPONSE RATE** — Responds to input signals in less than one millisecond. Instantaneous start rate of 2,000 steps per second.
- HIGH TORQUE CAPABILITY** — Peak torques of up to twice rated capacity can be handled.
- HIGH SYSTEM EFFICIENCIES** — Extremely rapid acceleration and high torque from low horsepower drive.

Compatible logic driver cards, translators and pre-set indexes are also available.

FOR COMPLETE DETAILS WRITE TODAY



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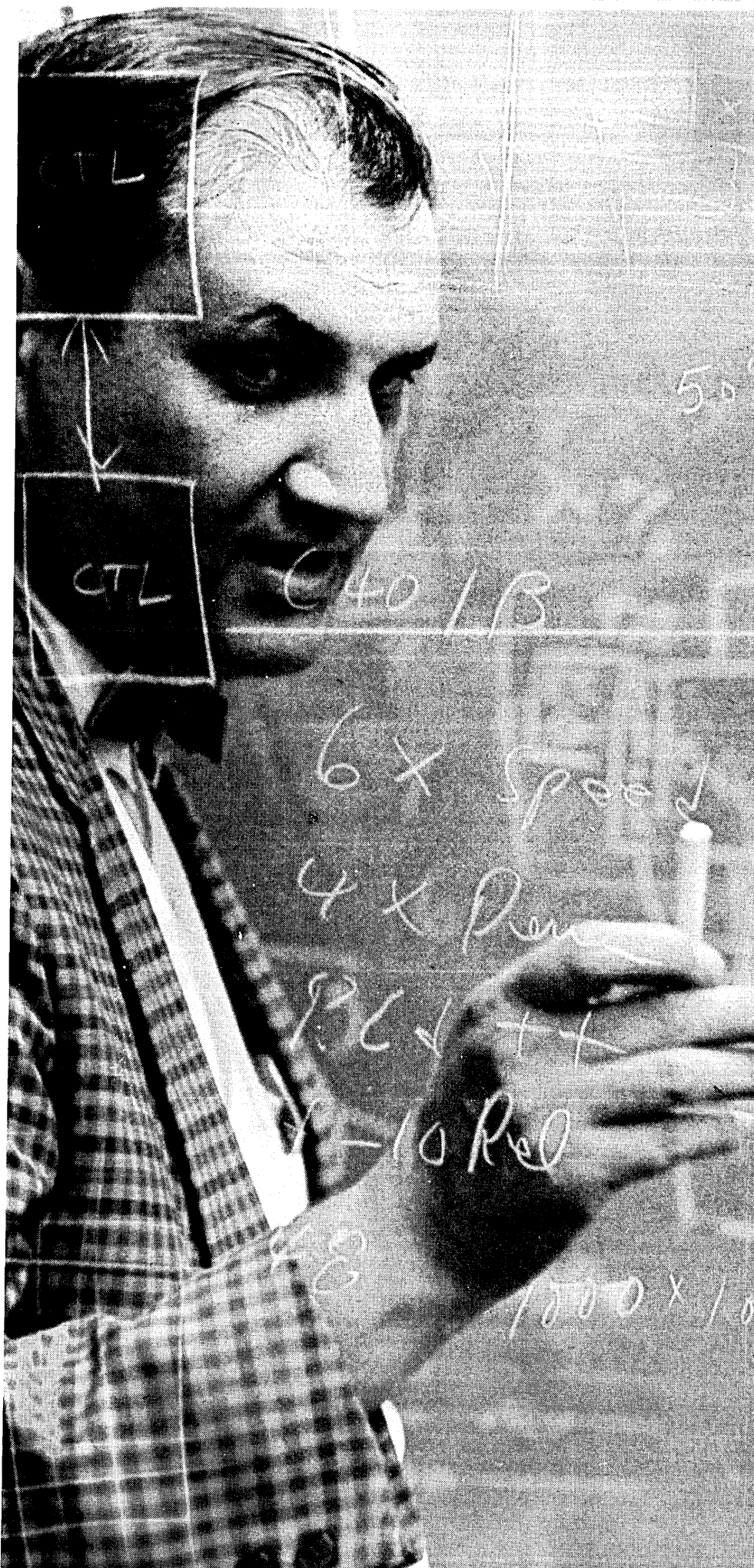
LOW-SPEED MODEM

The TT-103 data set, a low-speed asynchronous modem built on a single PC card, transmits and receives data up to 300 bps. It is compatible with the Bell 103. The majority of the data set is composed of TTL IC logic. Connector pads are provided at one end of the card so that the data set may be utilized either as a plug-in unit or hand-wired within a terminal.

The data set may be used to transmit data over either the switched telephone network or via dedicated 3 KHz type 3002 unconditioned telephone circuits. With either facility, the TT-103 provides full duplex data transmission over a two-wire circuit. To permit the transmission of data on a dial-up network, the TT-103 has been designed to operate with the Bell Data Access Arrangement.

The digital input circuits (for signals from the terminal to the data set) are compatible with RS-232B interfaces. The output circuits are compatible with IC logic input circuits of most terminals. Tel-Tech Corp., Silver Spring, Md.

Circle No. 240 on Inquiry Card.



Logic Design Engineers:

Help IBM design digital systems that have never been designed before.

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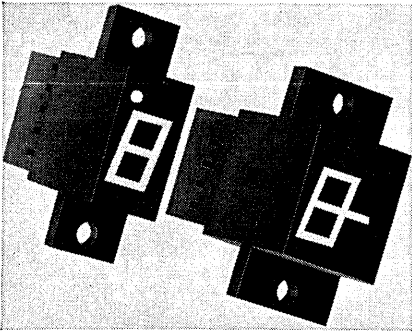
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If you're interested in working on new digital systems, call Jim Dunn at (301) 921-7724 collect any weekday between 9 and 4:30. Or, send a brief letter or resume to him at IBM Corporation, Federal Systems Division, Dept. CE1015 18100 Frederick Pike, Gaithersburg, Maryland 20760.

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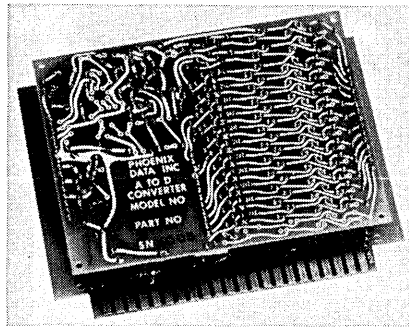
NEW PRODUCTS



MIL-SPEC DIGITAL READOUT

Series 30 DiGiCATOR® readout modules are designed to meet various environmental and performance requirements common to military airborne and ground equipment applications. Character size is approximately 0.3 by 0.2 inches. Lamp characteristics: 20 mA maximum at 5 Vdc, rated life of 50,000 hours. Available in white or with red or green filters. Light output from 10 FL to 200 FL with standard lamps, and up to 1,000 FL with higher current lamps. Discon Corp., Fort Lauderdale, Fla.

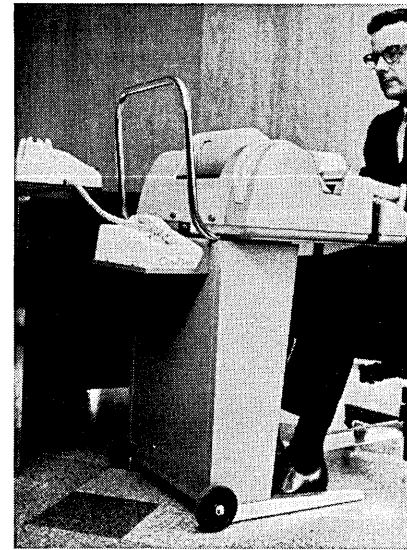
Circle No. 267 on Inquiry Card.



A/D CONVERTER

Model ADC 1370 is capable of encoding $\pm 10V$ full range inputs into 13 binary bits of data with a minimum thruput time of $14\mu s$. Successive approximation measurement is used which provides a resolution of 1 part in 8,191 with an accuracy of $\pm 0.015\%$ of full range. The converter also features a low temperature coefficient of ± 5 parts per million/ $^{\circ}C$; full range input of $\pm 10V$, 0 to $+10V$, or to 5V standard; 100 megohms input impedance with optional amplifier; serial and parallel outputs; 71,428 conversions on command or continuous. Phoenix Data, Inc., Phoenix, Ariz.

Circle No. 266 on Inquiry Card.



PORTABLE TERMINAL/DATA SET

A completely portable modified Model 33 Teletype and acoustic data set has a large range of options which include: paper tape input-output; automatic control of paper tape reader and/or punch; friction or sprocket feed; automatic form feed; 74 or 88 columns per line; mobile stand; separate or built-in acoustic data set providing originate only or originate/answer mode. Originally developed for large volume users, the portable units are now available in single quantity. ComData, Inc., Niles, Ill.

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Replace paper
tape, delay lines,
drums, etc. with...

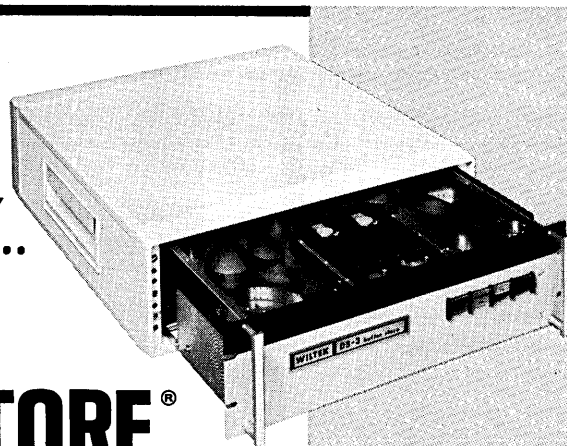
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Magnetic Tape BUFFER-STORE DS-3

- Independent-asynchronous bi-directional read and write
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- Self-contained special interfacing available

Ideal for:

Buffered rate change, data accumulation, editing, message sorting/routing, and other data handling applications.



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EMI FILTERS

A line of miniature EMI filters offer current ratings of .1, .5, 1.0, 5.0, and 10.0 amperes in 50 Vdc, 100 Vdc and 200 Vdc configurations. The lightweight filters are designed to suppress conducted electromagnetic interference over a frequency range of 10 KHz to 1 GHz.

The hermetically-sealed units offer a low dc resistance and a high insertion loss and are designed for operating temperature ranges of $-55^{\circ}C$ to $+85^{\circ}C$, meeting applicable requirements of MIL-F-15733E. Genisco Technology Corp., Compton, Calif.

Circle No. 219 on Inquiry Card.

CIRCLE NO. 55 ON INQUIRY CARD

Causes and Cures of Noise in Digital Systems

J. PAUL JONES
President
Navigation Computer Corp.
Norristown, Pa.

PART 1

Systems Design Considerations

PART 2

Noise Elimination in Digital Modules

PART 3

Control of External Noise

Based on a 3-part series of articles in the 1964 September, October, and November issues of COMPUTER DESIGN magazine, this handbook serves as a practical design guide for solving one of the major problems in designing digital systems. The author's emphasis is on practical tips for eliminating or minimizing noise — generalized rules are highlighted throughout the discussion. In Part 1, the forms of noise that are generated in wiring backplanes are considered and standard precautions that should be taken in systems design are given. Part 2 covers noise elimination in digital modules, and Part 3 discusses the control of external noise.

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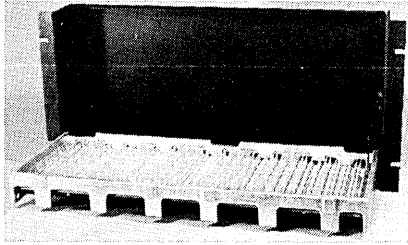
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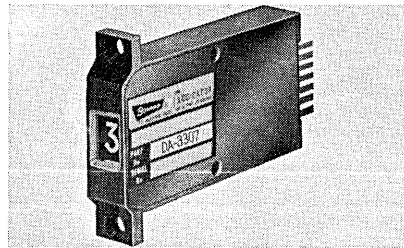
NEW PRODUCTS



RACK MOUNTING CHASSIS

Rack mounting IC panel support hardware features tilt out frame which allows access to wire-wrap terminals or plug-in sockets. Designed to mount in 19 inch panel width RETMA cabinets, the unit requires 8¾ inches of panel height and 3 inches of cabinet depth. Ventilation is provided in top and bottom flanges of frame and cover panel (not shown). Tilt out frame locks in open and closed positions to allow insertion/removal of DIP's and wire-wrap maintenance when mounted in rack. Modular Systems Corp., Chestnut Hill, Mass.

Circle No. 262 on Inquiry Card.



DIGITAL DISPLAY

The DA-3307 Logicator® Electro-magnetic Digital Display features self-contained drive and memory for high speed data acceptance. The Logicator display provides direct readout of digital computer signals with back-lighting for optimum day and night readability. The readout drum of this miniature display is electromagnetically positioned directly from digital computer level voltage.

Specifically, the DA-3307 accepts and stores data at microsecond speed, which means the computer data need only be present for 10 μs while it is being read into the memory of the Logicator. Bowmar Instrument Corp., Fort Wayne, Ind.

Circle No. 259 on Inquiry Card.

POWER SUPPLIES

A bench top or system power supply package offers four supplies in one-half rack width.

Key features of the Model CPS 400-1 series include current overload indications, floating outputs, remote sensing and short circuit protection. The CPS 400-1 series output is adjustable in each section from 100 mV to 36V., 0 to 1.0 amps. Voltage regulation specifications are stated at .05% maximum or 5 mV under worst case combination of 10% line variations during no load to full load conditions.

Other specifications include 0 degree C to 50 degree C operating temperature, complete isolation of all outputs, and current limiting adjustable from 10% to 100% of supply current capacity. Recovery time is 0.5 ms from no load to full load and 5.0 ms from full load to no load. Weight is 16 pounds and dimensions are 5¼" high x 9½" deep x 8½" wide. International Contronics Inc., Sunnyvale, Calif.

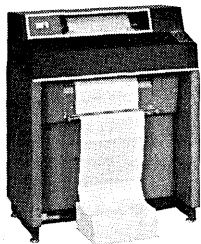
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LOW COST, HIGH RELIABILITY... WITH MDS LOW-SPEED LINE PRINTERS

MDS Series 4000 Low-Speed Line Printers... with speeds up to 300 lines per minute... are especially designed for business or scientific applications where low cost, reliability and performance take precedence over ultra-high speeds.

The "heart" of the Series 4000, the MDS 4013 Printer Mechanism, features a rotating drum, on-the-fly impact printer with "built-in" long life and reliability. The 4013 is available as a separate unit for integration in your own system; in the MDS 4320 Console model, with ready strobe serial buffer; or in the MDS 4300 Console model (unbuffered).

Ask about these MDS Series 4000 features: Print hammers with MDS Penetration Control • 1 to 6 copies (including original) • Tape Control Vertical Format Unit... up to 12 channels • Automatic ribbon tracking mechanism • New Fibre Optics System... only 3 light sources.



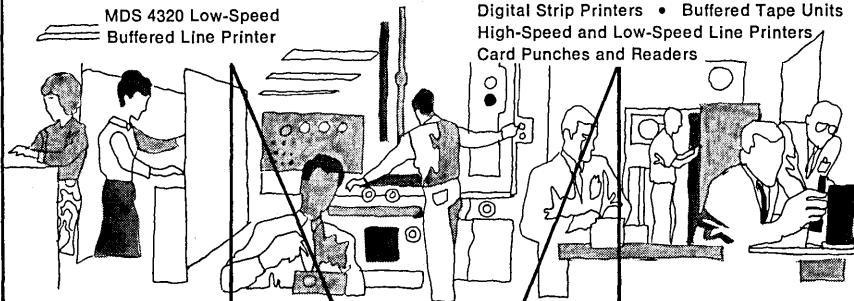
MDS 4320 Low-Speed Buffered Line Printer

Ask for: Folder-file on MDS Series 4000 Low-Speed Line Printers

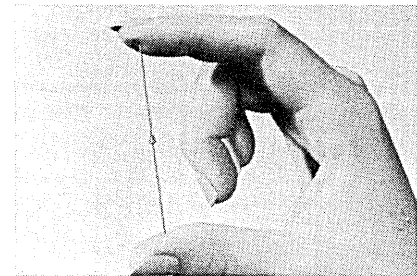
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UNI-TUNNEL DIODES

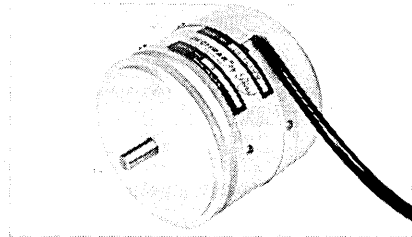
A new version of the Uni-Tunnel® tunnel diode, identified as the U1001 through U1010 series, are silicon "backward diodes" which exhibit high reverse conductance at milliwatt levels. When biased in the forward direction, these diodes operate with leakage tunneling current of microampere magnitude.

Applications include computer logic, modulators, detectors, clamping and limiting circuits, and low temperature coefficient reference voltage.

Furnished in the DO-17 package, all units are hermetically sealed and have gold-plated, weldable Kovar. leads. This series is designed to meet or exceed the environmental exposures of MIL-S-19500 and MIL-STD-750. Centralab Semiconductor Div., Globe Union Inc., Milwaukee, Wisc.

Circle No. 209 on Inquiry Card.

NEW PRODUCTS

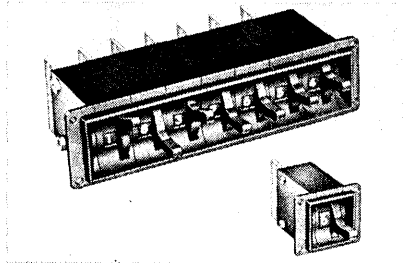


OPTICAL SHAFT ENCODER

An optical incremental shaft encoder features a choice of built-in solid-state electronics. Outputs are generated from two channels to produce a count which is accurate regardless of the direction of shaft rotation. To optimize performance, only a single code disc is used and internal gearing is not employed.

Specifications: Up to 1,000 counts per turn; Rated speed, 4000 rpm; Breakaway torque, .05 in.-oz; Ambient operating temperature, 0°C to 70°C; Size 2½ in. dia. by 1½ in. long (4 in. long with all electronic options). Theta Instrument Corp., Fairfield, N.J.

Circle No. 254 on Inquiry Card.

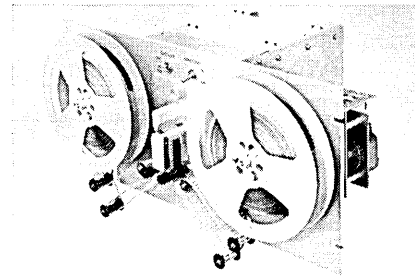


THUMBWHEEL SWITCHES

A line of lever-action thumbwheel switches, called Leverwheel, feature an extended lever that replaces the traditional thumb indents found in regular thumbwheel switches.

A single movement of the lever through its 60° arc is all that's necessary for a complete 10-position cycle. The lever feature also permits instant reset of a complete bank of the Leverwheel rotary switches with a sweep of the hand. A single downward movement returns all the levers to a full down position with every switch in the bank returned to zero setting, ready for easy, quick resetting. Cherry Electrical Products Corp., Highland Park, Ill.

Circle No. 221 on Inquiry Card.



PHOTOELECTRIC TAPE READER

The Model 1220 Photoelectric Tape Reader offers bidirectional operation at rates up to 250 characters per second asynchronous, 300 characters per second synchronous, with stop-on-character capability.

The reader, tape handler, and control circuitry are self-contained in a single compact unit designed for mounting in a standard 19" rack. Industry standard tape formats of 5, 6, 7, or 8 levels can be accommodated without any adjustments to the reader or spooler. In-line or advanced sprocket formats can be selected by a simple mechanical adjustment. Navcor, Inc., Div. of KDI Corp., Norristown, Pa.

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Designers Choice

What's best for your logic system design? CAMBION's Logic Manual tells you all you need to know about CAMBION DTL, TTL, HTL circuits, full MIL capability, complex functions, all types of cards for use in industrial controls, computers, A-to-D converters; interfacing instrumentation, and automatic check-out systems.

CAMBION's new Wire-Wrap* Products and Service Brochure covers our prototype and production wire-wrap activity... plus sockets, cards, files and racks for the designer developing his own cards. Get these two free catalogs today. Cambridge Thermionic Corporation, 457 Concord Avenue, Cambridge, Massachusetts 02138. Phone: (617) 491-5400. In Los Angeles, 8703 La Tijera Boulevard 90045. Phone: (213) 776-0472.

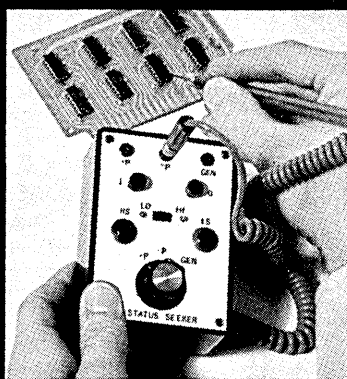
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A compact, lightweight, hand-held unit for field service operation, laboratory and production testing.

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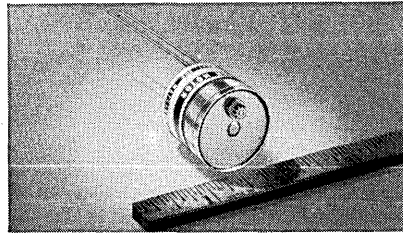
NEW PRODUCTS

MAG TAPE TRANSPORT

The Model BI 830 tape transport records incrementally at 1,000 sps and continuously at 75 ips, with a data transfer rate of 60 kHz. Data packing densities of 1600, 800 or 556 bpi are available. The BI 830 is a single capstan recorder using three heavy duty, high torque printed circuit motors with the optical encoder, tachometer and capstan motor on one rigid shaft. Tape transport mechanics are mounted on a machined heavy casting. There are no mechanical adjustments. The unit is also available with incremental read at 400 sps and continuous read at 75 ips.

Continuous speeds are field adjustable. All tapes, on 8 1/2" reels, are fully IBM compatible, 7 or 9 track, recorded with a high density ferrite recording head. Bright Industries, Inc., San Francisco, Calif.

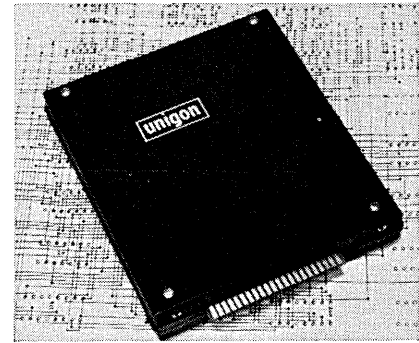
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2-WIRE STEPPER

A 2-wire stepper motor, Series 31300, directly converts electrical impulses into discrete angular steps of the output shaft without need for control logic. For each impulse the rotor turns 360°; 180° when power is applied and 180° more when power is removed. No power is consumed between pulses, making it ideal for battery operated systems when power is limited. Only 1 1/8 in. diameter by 1 1/2 in. long, the motor develops 5 inch-grams torque with 6° step angle at pulse rates up to 15 per second. It has a power input of 2 watts and is positively unidirectional. Haydon Switch & Instrument, Inc., Waterbury, Conn.

Circle No. 255 on Inquiry Card.



HIGH SPEED MULTIPLIER

The MPY-10 digital multiplier accepts a 9 bit 2's complement number and an 8 bit magnitude number and outputs a 10 bit truncated 2's complement product with a maximum delay of 250 nanoseconds. No output control signals are required and interface is TTL, DTL compatible.

Power requirements are 5 volts @ 1.5 amps. Design specifications for the MPY-10 ($Z = XY$) are as follows: Input X, 9 bits including a sign bit, negative values in two's complement form; Input Y, 8 bit magnitude; Output Z, 10 bit truncated product including a sign bit; Input levels, 0 < one < 0.8 volts, 2.5 < zero < 5 volts; Output levels, 2.5 < one < 5 volts, 0 < zero < 0.8 volts; Input loading, 16 mA max; Output drive, 20 mA min. Unigon Industries, Inc., New York, N.Y.

Circle No. 257 on Inquiry Card.

Our CRT Track-balls
withstand up to
30 times greater
pressure
and
shock.



Only Librascope's 2 axes ball to digital or analog transducers have rugged construction with an exclusive bearing arrangement to withstand greater pressure and greater shock than any comparable models available.

Librascope offers a wide selection of Track-balls based upon variations of four basic designs. Ball sizes range from 1 to 3 inches in diameter. Outputs are digital or analog. All models are "coffee proof" sealed and permit continuous rotation on both axes.

For all specs and application assistance, write to Librascope Products, Singer-General Precision, Inc., Dept. 10-415, 808 Western Ave., Glendale, Calif. 91201.

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DIGITAL INTERCOUPLER

Model 210 couples electronic instrument outputs to peripheral equipment such as Teletype equipment, card punches, incremental mag tape recorders, printers and line printers and typewriters. With optional features, the Model 210 can be used to simultaneously drive two output devices such as a paper and card punch, or a paper punch and digital printer.

The digital intercoupler is capable of receiving coded data from standard measuring equipment—DVMs, counters, scalars, timers—and translating the data into computer compatible form to drive the readout devices.

The intercoupler, which can be rack mounted, stands 5 1/4" high, is 19" wide and 17" deep. Depending on the output device, typical operating speeds range from 10 characters per second to 1000 characters. Daedalus Computer Products, Inc., Syracuse, N. Y.

Circle No. 251 on Inquiry Card.



DECODE DISPLAY MODULE

A decode display module using a 7 segmented neon tube display is available as a compact module with the tube mounted on the printed circuit board. All input and output is on a rear connector.

Size of the module is $1\frac{7}{8} \times 2\frac{11}{32}$, and the units can be mounted on a .5" center. Input is BCD 8421 at typical IC logic levels.

Key features include: bright, clear, well-defined numerals; built-in decimal point in lower right hand position and a colon in the upper left hand position; tube width of .5". Integrated Circuit Electronics, Waltham, Mass.

Circle No. 228 on Inquiry Card.

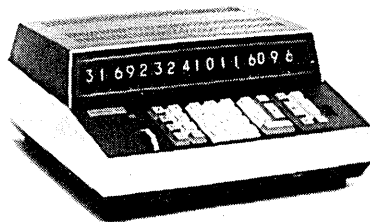
DISK DRIVE

The ISS 701, plug-to-plug compatible with the IBM 2841 controller and data interchangeable with the IBM 2311 disk drive, has an average access time of 30 ms. It features a 15 second start-up time and a data transfer rate of 156,000 bytes per second.

Reliability is substantially improved over other drives through use of an electromagnetic actuator and an electronic positioning control system rather than the typical hydraulic and mechanical devices. In addition, electronics have been substituted for the least reliable mechanical parts, thereby reducing particle generation and head-disk interference.

The 701 utilizes the IBM 1316 disk pack (or equivalent) as the storage medium. Each pack has a storage capacity of 7.25 million bytes. Information Storage Systems, Inc., Cupertino, Calif.

Circle No. 241 on Inquiry Card.

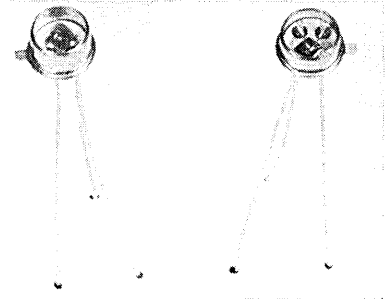


DESKTOP CALCULATOR

The Busicom 162, a desktop 10-key electronic calculator with two memory banks can perform decimal placement, rounding off, accumulation of products and quotients, square root and squaring, raising to a power, and automatic constant in all operations. The machine will also strike a credit balance.

In the event an operator forgets, the two memories in the Busicom remain even though the power is shut off. Either memory can be cleared or recalled at the push of one button. All operations, which include addition, multiplication, subtraction, division, extraction of square root and raising to a power, are displayed instantly on a 16-digit operating register. Busicom USA, New York, N.Y.

Circle No. 217 on Inquiry Card.

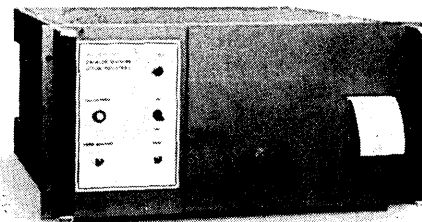


NANOSECOND THYRISTORS

The GA200 series of silicon planar passivated nanosecond thyristor switches have the following unique characteristics: rise time of 10 nanoseconds to 1 amp or 20 nanoseconds to 30 amps; recovery time as fast as 0.5μ secs.; voltage capability of up to 2000 volts with no significant decrease in speed when "series stringing" circuits are used; and surge current capability of up to 50 amps. They are ideal as drivers for solid state lasers, harmonic wave form generators, high-level digital switching, thyratron replacements in low to medium power radar pulse modulators, and as reliable replacements for avalanche transistors. They are available in TO-18 packages. Solid State Products, Salem, Mass.

Circle No. 230 on Inquiry Card.

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NEW PRODUCTS

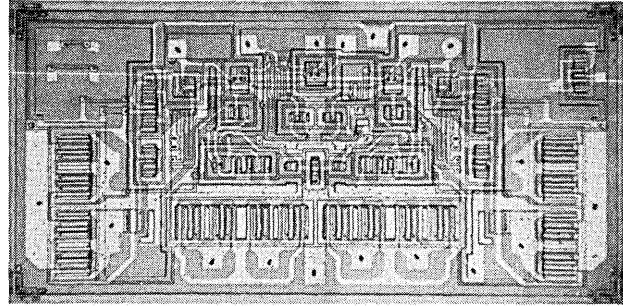
HIGH-SPEED DATA MODEM

The AE-96 high-speed bps data modem is capable of quadrupling the capacity of a 2400 bps voice grade line to 9600 bps. The modem achieves this capacity by means of a specially developed digital adaptive equalizer which allows the AE-96 to automatically measure and compensate for the intersymbol interferences caused by circuit amplitude and delay distortion which had previously limited high-speed data transmission on telephone circuits to a maximum of 4800 bps. Initial circuit equalization requires 3.5 seconds. Thereafter, the adaptive equalizer measures continuously, and compensates for circuit changes eight times each second.

The AE-96 operates on international submarine cable and satellite circuits as well as on U.S. telephone lines and uses a multi-level single-side band amplitude modulation system technique. In its 9600 bps mode of operation, the modem transmits four bits per cycle of bandwidth by means of four amplitude levels. A front panel switch provides an alternative transmission speed of 4800 bps, in which case two amplitude levels are used.

The Modem meets the RS-23B Interface Standard (full duplex) of EIA or MIL Standard 188B. The standard power supply is 115 volts AC \pm 10%, 50-60 Hz, 250 watts. Codex Corp., Watertown, Mass.

Circle No. 206 on Inquiry Card.



COMPUTER-INTERFACE LINEAR IC

A system-interface IC designated SN75324, is a 400 mA core memory driver with logic and decode all in the same packaging.

The SN75324 features the elimination of transformer coupling—thus lower user costs—achieved by locating logic and transistor switching in the same package. The elimination of transformer coupling also allows complete compatibility with TTL circuits.

Another advantage is increased reliability through use of dual sink/source outputs. Other characteristics include: typical output saturation voltage, 0.65 V; nominal output sink or source current, 400 mA; typical average propagation delay time, 60 ns; and operating temperature range, 0°C to 70°C. Texas Instrument Inc., Dallas, Texas.

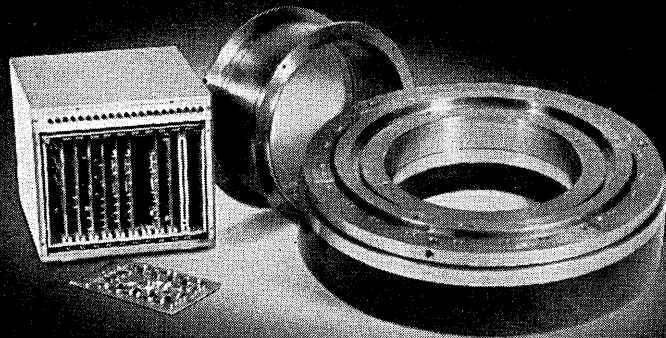
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NEW 21 BIT SHAFT ENCODER

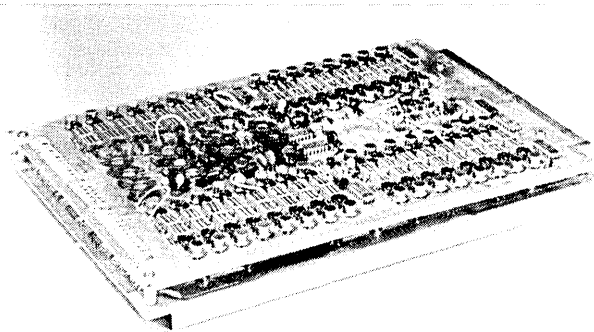
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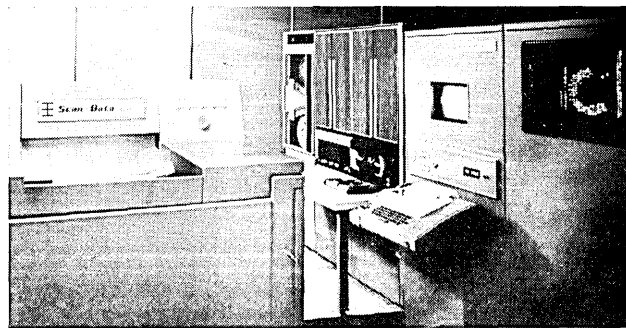
HIGH SPEED CORE MEMORY

Model 140 features 900 nanosecond full cycle time and 300 nanosecond access time. Capacity of the module is 4096 words x 8, 9, 10 bits. Address and timing inputs are supplied by the user.

Design features of the Model 140 include: Full, half, and split cycle modes of operation; random address; parity line data, address, and control line input/output; TTL IC interface; 40 watts average power consumption; 0-50°C operating temperature range. The unit measures 8 $\frac{5}{8}$ " w x 1 $\frac{7}{8}$ " h x 12 $\frac{1}{2}$ " d, and weighs 3.5 lbs.

The MSI-140 may be ordered as a separate memory sub-assembly or as part of a complete system. Standard memory systems expandable up to 32K bytes at 900 nanosecond cycle times, complete with power and full range of options, are available. Micro Systems Inc., Santa Ana, Calif.

Circle No. 261 on Inquiry Card.



PAGE READING OCR SYSTEM

The 200 expandable OCR system reads upper and lower case alphabetic, numerics, punctuation, and symbols, and in a single font mode, OCR-A, OCR-B, Elite (10 or 12 pitch), 1403, and Hand-print reading capabilities are available. In a typical application, the error rate is from 0.001% to 0.0003% on a character basis. A flying spot scanner reads documents at 400 characters per second while it is held in position by vacuum.

On-line and off-line copy correction capabilities are available with the 200. If a character is broken or smudged and therefore unrecognizable, the character in context is presented on a CRT monitor (with the questionable character highlighted). The operator strikes the correct letter on a typewriter keyboard and the information is recorded on the output device. There is no need for physical retrieval of the source document. A set of hand edit characters are read optionally, allowing the user to control source input from forms and text. Scan-Data Corp., Norristown, Pa.

Circle No. 204 on Inquiry Card.

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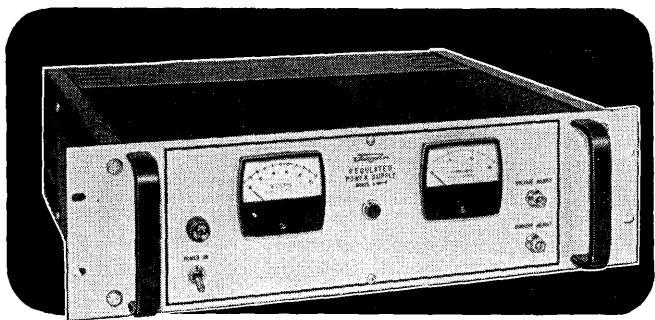
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NEW PRODUCTS



PORTABLE ACOUSTIC DATA TERMINAL

The ADT 233 Acoustic Data Terminal meets the need of the computer time-sharing user who wants a reliable, page printer, teletype terminal, with or without paper type capability, all in one compact package. The unit is shock-mounted in a sturdy, light weight fiberglass case with four wheels for easy movability.

The built-in acoustic data coupler makes extensive use of digital circuit techniques and integrated circuits, and incorporates a digital filter, a digital discriminator, an adjacent band energy monitor, and floating acoustic cups. The terminal will not respond to telephone line or room noise well above its sensitivity threshold for desired signals. Error-free operation and high noise immunity are hallmarks of the Portable ADT 233 design. The case includes a paper tape reader guide, silent butler chad receptacle, and carriage lock. Anderson Jacobson, Inc., Mtn. View, Calif.

Circle No. 205 on Inquiry Card.

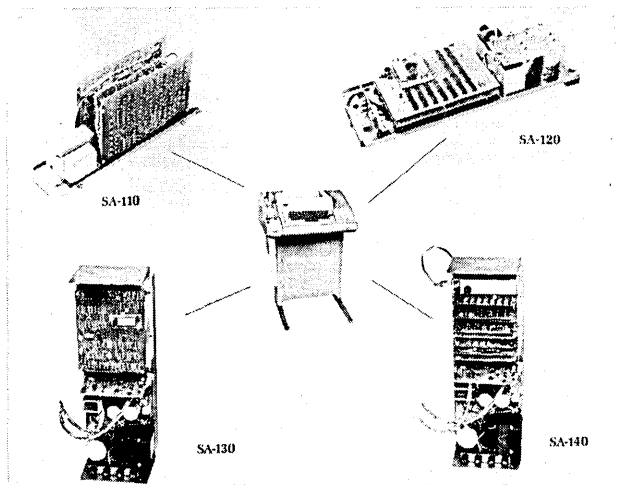
DATA DISPLAY TERMINALS

The 2000 series is a System-360 compatible data terminal that can display up to 2000 cursive-stroke characters or graphs. Its capabilities include full editing and a true typewriterlike tab that can be controlled by the System 360. This tab permits the operator to move from anywhere on the screen to the next variable field. To eliminate the transmission of extraneous blanks, the CPU can be programmed to begin writing messages at specific display locations (automatic character addressing).

The 2000 series includes the Model 2020 stand-alone display and the Model 2030 multi-station version, both of which use cursive-stroke electron beams to form letters, numerals and graphs on their P31 phosphor screens.

Series 2000 equipment is completely hardware and software compatible with any IBM 360 computer and uses the same software as the IBM 2848/2260 display. This prevents disruptions caused by periodic improvements in System 360 programming. It maintains perfect interface with an IBM 2701 teleprocessing data adapter, and can accept or transmit data at 1200 or 2400 bits per second, synchronous or asynchronous, or any other rate up to 4800 bits per second. Atlantic Technology Corp., Somers Pt., N.J.

Circle No. 203 on Inquiry Card.



DATA COMMUNICATIONS ACCESSORIES

Error control for data transmission and automatic answering of remote station teletypewriters are two key features of a series of accessories, called Stuntronic Accessories. The four basic units are designated SA-110, SA-120, SA-130, and SA-140.

Stuntronic Accessories SA-110 and SA-120 are designed for systems where data must be transmitted with great accuracy (payroll, order processing, inventory control, etc.). Both models respond to vertical parity signal errors by generating timed pulses that activate various displays or alarms. At the same time they register errors, the SA-110 and SA-120 improve the signal reception by regenerating signals which have as much as 45% distortion.

The two other units, the Stuntronic Accessory SA-130 and SA-140, provide complex control arrangements. Their station selection and response function makes for a cool, quiet operation in which terminal motors are turned on only by the calling station or computer. All four compact Stuntronic Accessory modules are easily installed within Models 33, 35, 37 and the new high-speed Inktronic terminal equipment. Teletype Corp., Skokie, Ill.

Circle No. 207 on Inquiry Card.

SYNCHRO TO DC CONVERTER

Model A205 transforms a 3-wire synchro or 4-wire resolver input to a linear dc output proportional to the equivalent input angle. Output is completely smooth over the entire 360° angular range and is without transients, even at cardinal points. It is suitable for applications in servo system testing, general computer use or any other area where precise angle indication is required.

This miniature converter is all solid state, lightweight, and features the use of precision multi-tapped toroidal transformers. The high impedance wide band characteristic of the transformers eliminate the need for high gain synchro amplifiers with their resulting gain and stability problems. Consequently, there are no field adjustments required.

Accuracy of standard units is ± 6 minutes of arc at high tracking speeds and retains calibration integrity under voltage and frequency variations as high as 10%. Models are available for 60 Hz or 400 Hz operation. Dimensions are 4" h x 5" w x 5" d, and maximum weight is 4 pounds. Astro-systems, Inc., New Hyde Park, N. Y.

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Data Media Storage Cabinet

A cabinet designed for general purpose, flexible storage of data media and computer room paraphernalia is described in this product sheet. Tab Products Co., San Francisco, Calif.

Circle No. 304 on Inquiry Card.

Miniature Vacuum Lamps

A 4-page folder features a new system of customized miniature vacuum lamps for applications in fiber optic and photo-sensitive devices. Welch Allyn, Inc., Skaneateles Falls, N.Y.

Circle No. 311 on Inquiry Card.

IC's/Discrete Components

This 8-page booklet contains abstracts of over 50 application reports and notes related to solid-state devices and integrated circuits. Texas Instruments Inc., Dallas, Texas.

Circle No. 310 on Inquiry Card.

Data Compression Bibliography

Three bibliographies covering the published literature on data compression are combined in a publication entitled "A Compendium of Data Compression Bibliography." Scientific Data Systems, El Segundo, Calif.

Circle No. 305 on Inquiry Card.

Power Line Assemblies

A series of power line assemblies, designed to shield and eliminate interference on power lines over the range of 14KHz to 10GHz, is described in this catalog. Genisco Technology Corp., Components Div., Compton, Calif.

Circle No. 300 on Inquiry Card.

Century COBOL

A 20-page brochure highlighting COBOL includes the stages of Century COBOL, language considerations, source configurations, divisions of the language, compile time and cost per statement, criteria for evaluating a COBOL compiler and advantages of Century COBOL. The National Cash Register Co., Dayton, Ohio.

Circle No. 325 on Inquiry Card.

Delay Lines

Catalog NS-16 provides complete details and mechanical specifications for a miniature series lumped constant delay lines. Engineered Components Co., Gardena, Calif.

Circle No. 301 on Inquiry Card.

Visual Image Processing

A 12-page color brochure describes and illustrates visual image processing via computer-based optical systems. Information International, Los Angeles, Calif.

Circle No. 303 on Inquiry Card.

Instrumentation Recorder

Complete specifications of the AV-15000R instrumentation magnetic recorder are featured in a 6-page brochure. Newell Industries, Sunnyvale, Calif.

Circle No. 302 on Inquiry Card.

Ribbon Cable/Assemblies

Spectra-Sil flat ribbon cable and harness assemblies made of individual round conductors insulated with silicone rubber are featured in Bulletin 070. Spectra-Strip Corp., Garden Grove, Calif.

Circle No. 308 on Inquiry Card.

High Reliability Transistors

This 74-page catalog describes nearly 400 types of high reliability silicon transistors including specifications, maximum ratings and electrical characteristics. Raytheon Co., Semiconductor Operation, Mountain View, Calif.

Circle No. 307 on Inquiry Card.

Power Supplies

New products listed in this 32-page catalog supplement include the COM-PAK Mark II integrated-circuit power supply LC series, the militarized COM-Pak Mark II MIL-C Series integrated-circuit power modules and three power supply assembly systems, Lambda Electronics Corp., Melville, N.Y.

Circle No. 329 on Inquiry Card.

CRT Data-Screen Terminals

Information and specifications for Series 500 cathode ray tube data-screen terminals are presented in Catalog 682. Transistor Electronics Corp., Minneapolis, Minn.

Circle No. 321 on Inquiry Card.

Computer Port Selector

A high-speed method of switching to expand the line-handling capacity of a time-shared computer is described in this bulletin. Technitrend, Inc., Pennsauken, N. J.

Circle No. 319 on Inquiry Card.

Commercial/Industrial Modems

A Modem Short Form Catalog describes standard commercial and industrial data sets (modems) operating at speeds up to 4800. Rixon Electronics, Inc., Silver Springs, Md.

Circle No. 324 on Inquiry Card.

Information Retrieval System

This 4-page brochure describes the Model 103 high-speed information retrieval system, including hardware requirements and illustrates its many applications. Computer Corporation of America, Cambridge, Mass.

Circle No. 306 on Inquiry Card.

PC Board Core Memory System

This bulletin details complete specifications, memory interface timing, connector pin assignments, and complete dimensions for ECOM-S a low cost, random access economical core memory system. Standard Memories, Inc., Sherman Oaks, Calif.

Circle No. 323 on Inquiry Card.

Synchro to Digital Converter

This data sheet describing aerospace applications and specifications for a multiplexed synchro to digital converter, contains complete information on a new concept in analog conversion featuring a maximum conversion time of 10 ms for 180 degree change of input angle. Astrosystems, Inc., New Hyde Park, N. Y.

Circle No. 318 on Inquiry Card.

Subminiature Lamps/Indicators

A catalog and price list, No. R-690, describes the "Rodan" range of sub-miniature lamps and indicator lights. Inter-Market Inc., Glenview, Ill. Circle No. 328 on Inquiry Card.

Stuntronic Accessories

How Stuntronic Accessories extend the capability of data communications systems is described in this literature. Teletype Corp., Skokie, Ill. Circle No. 327 on Inquiry Card.

Process Computer Transmitters

Two four-page, illustrated product specifications (E21-17 and E31-17) cover an electronic transmitter for differential pressure or for level measurement. Bailey Meter Co., Wickliffe, Ohio. Circle No. 330 on Inquiry Card.

Digital Graphics System

Bulletin 225 describes a high-speed line printer and ultra high-speed electronic/microfilm plotting system. California Computer Products, Inc. Anaheim, Calif. Circle No. 317 on Inquiry Card.

IC Core Memory

Description, specifications and a timing chart of the Model RGX low-cost core memory, designed for such applications as buffer memory in ground-based and airborne data acquisition systems, are contained in booklet CO98. Ampex Corp., Redwood City, Calif. Circle No. 316 on Inquiry Card.

10-Key Solid State Keyboard

Mounting dimensions, power requirements, output capacity (for each of the two isolated outputs per switch), operating characteristics, key spacing, and key assignments for a solid state numeric keyboard are included in this new product sheet. Micro Switch, a division of Honeywell Inc., Freeport, Ill. Circle No. 322 on Inquiry Card.

Alphanumeric/Graphic Display

This data sheet lists all specifications and discusses features and applications for a television display system. Data Disc, Display Div., Palo Alto, Calif. Circle No. 320 on Inquiry Card.

Military Punched Tape Readers

A series of military punched tape readers are featured in an illustrated eight-page brochure. Electronic Engineering Company of California, Instruments Div., Santa Ana, Calif. Circle No. 314 on Inquiry Card.

Hybrid Microcircuits

The use of hybrid microcircuits for light-weight and compact packaging designs is the subject of a 24-page brochure. Fairchild Semiconductor, Mt. View, Calif. Circle No. 315 on Inquiry Card.

Computer Power Sources

An eight-page illustrated brochure describing the advantages of motor generators for computer power sources includes photographs and performance curves. Georator Corp., Manassas, Va. Circle No. 313 on Inquiry Card.

Switches/Panel Components

This catalog lists an expanded line of miniature switches, keyboard switches and push button modules, machined aluminum knobs, ceramic terminal strips, readout indicators, pilot light assemblies and miniature lamps. Alco Switch, Div. of Alco Electronic Products, Inc., Lawrence, Mass. Circle No. 312 on Inquiry Card.

Scan Converter Tube

A comprehensive 6-page catalog includes technical features, electrical data, physical description and performance parameters and application of a new dual-gun, sub-miniature scan converter tube, RW-13EM, with high resolution (up to 1000 TV lines per target diameter). Warnecke Electron Tubes, Inc., Des Plaines, Ill. Circle No. 309 on Inquiry Card.

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