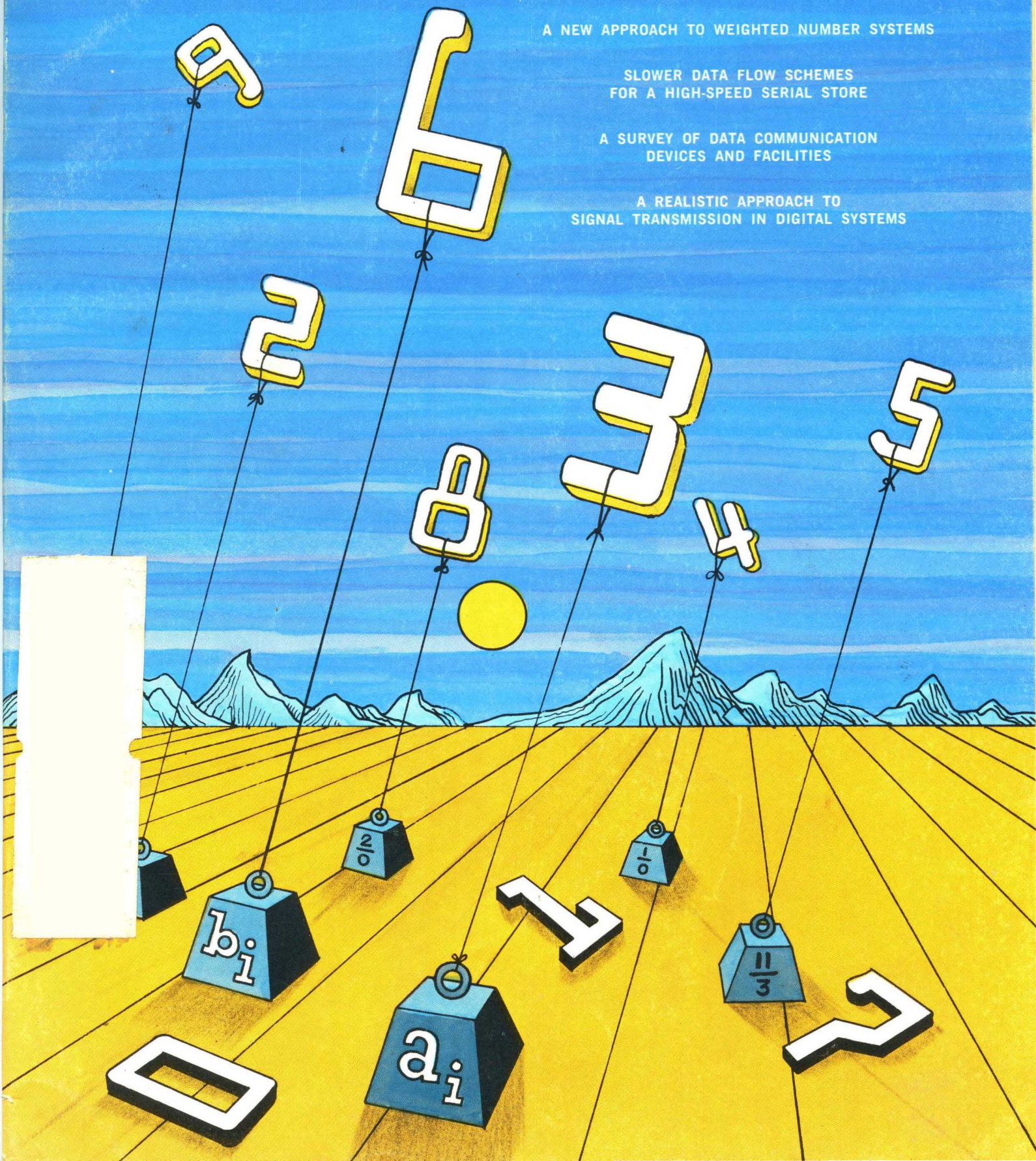
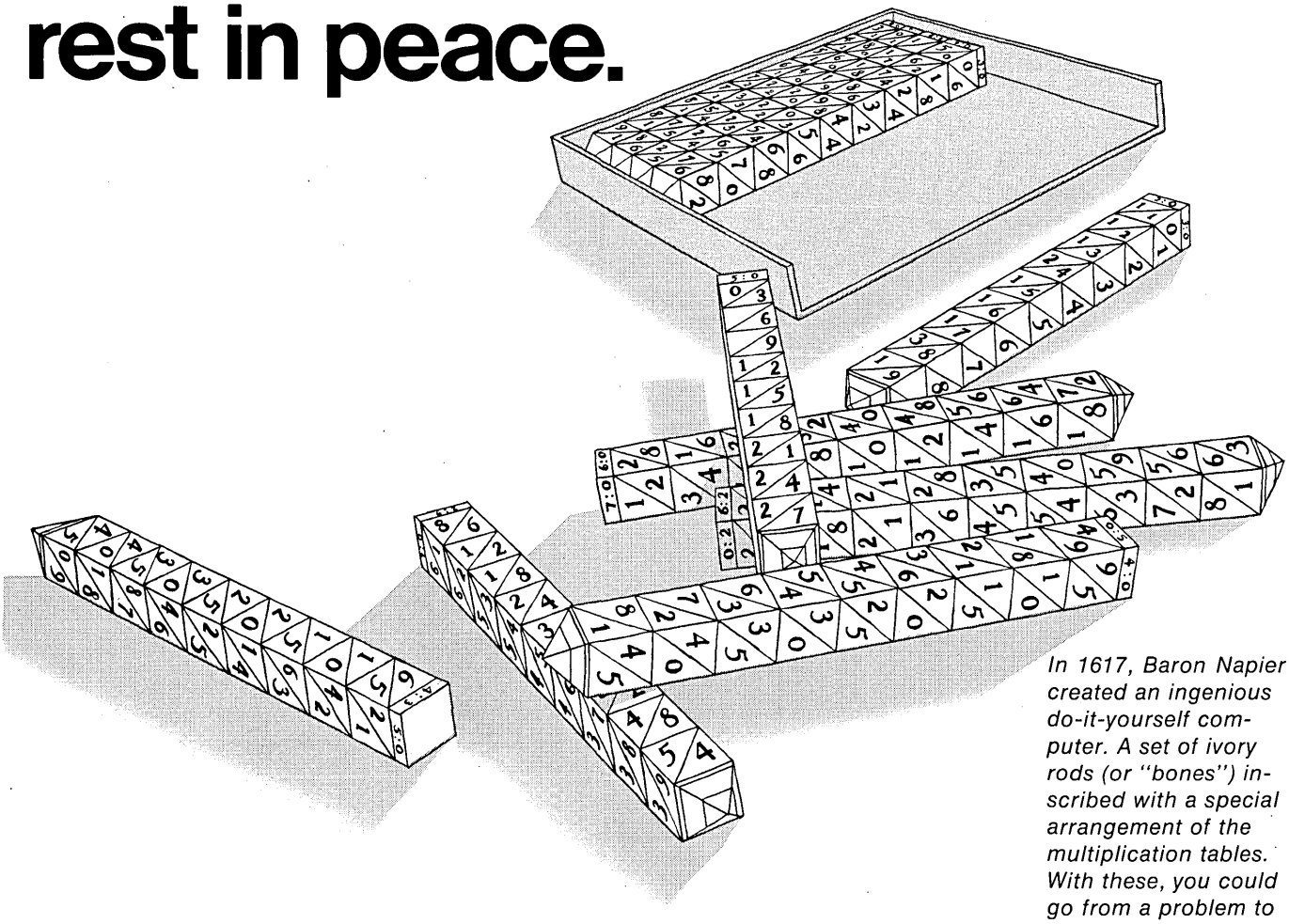
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS JULY 1969



May Napier's bones rest in peace.

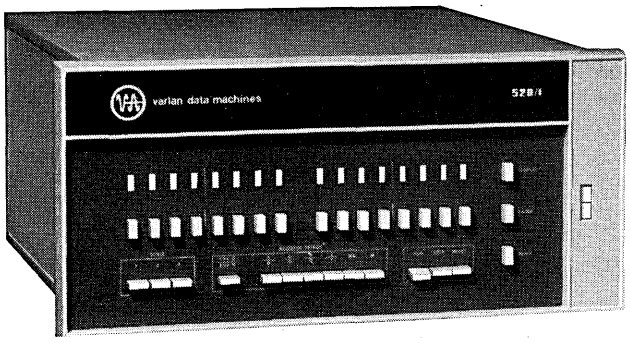


In 1617, Baron Napier created an ingenious do-it-yourself computer. A set of ivory rods (or "bones") inscribed with a special arrangement of the multiplication tables. With these, you could go from a problem to a square root faster than man had ever gone before.

They taught previous computers a trick or two. Which brings us to Varian Data's 520/i.

The 520/i was designed to tackle dual programs for the price of a one-track mind computer.

That took some doing. Such as handling arithmetic functions in 8, 16, 24 or 32 bit lengths within the same program—with precision changeability at any time.



Hardware includes two 32-bit accumulators, two 16-bit index registers, two program counters and two overflow registers. Plus eleven interrupt lines. And its 1.5 μs memory is expandable from 4K to 32K bytes.

The price of our paragon? Just $7,500. Considerably more than Napier's bones—and considerably less than any comparable computer. Why not write for your brochure today?

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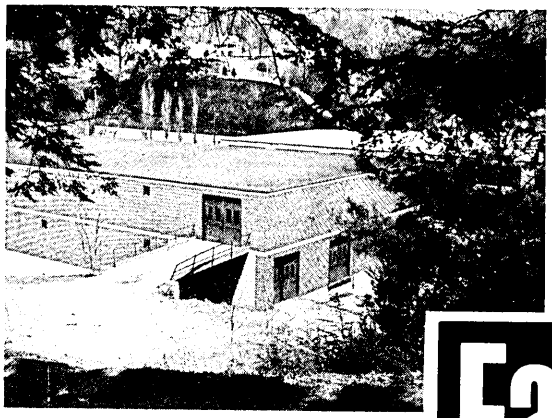
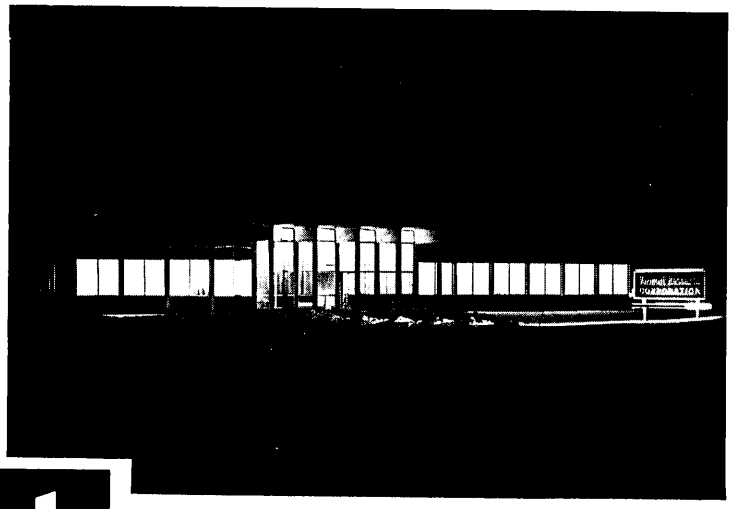
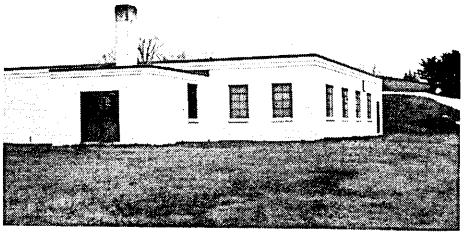
CIRCLE 1 ON INQUIRY CARD





Fact:

DRUM MEMORIES EXPAND THINGS



Drum Memories by Vermont Research expand your computer's capabilities . . . expand the power of your digital controllers . . . expand the usefulness of your timesharing systems . . . and even expand in the field to meet your growing requirements for reliable, fast access storage.

At VRC, our drums have expanded our customer list . . . and our sales. We've had to expand our manufacturing space to fill three buildings.

Have a large drum requirement? Talk to us now . . . while we're feeling expansive.

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When it comes to engineering opportunities (and the good life, North Country style), the place to come is Vermont Research Corporation. For specific information, contact: RICHARD A. STOVER, Vice President-Engineering.

CIRCLE 2 ON INQUIRY CARD

The den mother.

She always knows where all your little printed circuits are.

So in case you want to know anything about your order, just call (213) 722-6810, ext. 513. The Lockheed computerized control system – better known as our Den Mother – will have the answer for you immediately.

She knows how to keep track of thousands of orders, involving many thousands of lots and goodness knows how many parts. We update her daily, and she likes it. This way she can be aware of what and how many have been shipped, where parts and lots are and when others will be shipped.

So it only stands to reason. If we care enough to have a Den Mother just to look after our printed circuits – imagine our printed circuits.

LOCKHEED ELECTRONICS COMPANY

A Division of Lockheed Aircraft Corporation, Los Angeles, California

CIRCLE 3 ON INQUIRY CARD

JULY 1969 • VOLUME 8 • NUMBER 7

COMPUTER DESIGN

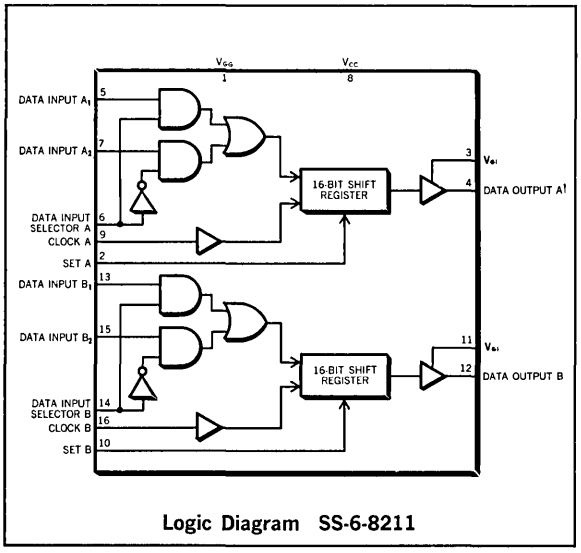
THE MAGAZINE OF DIGITAL ELECTRONICS

Editorial & Executive Offices
Prof. Bldg., Baker Ave.,
W. Concord, Mass. 01781
Tel. 369-6660

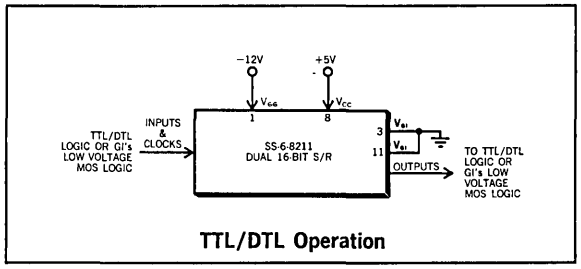
FEATURES

DEPARTMENTS

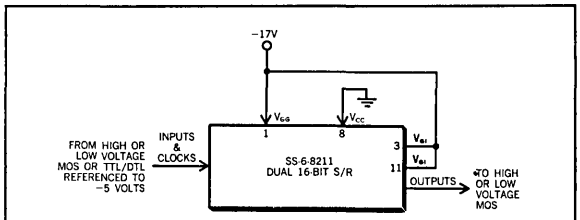
the first static dual 16-bit shift register directly compatible with TTL, DTL and MOS is also the lowest priced* shift register



Logic Diagram SS-6-8211



TTL/DTL Operation



MOS Operation

General Instrument's exclusive MTNS process has now been translated into a line of standard General Instrument LSI circuits.

The Dual 16-bit DC Shift Register is the first of the family of GIANTs (General Instrument Advanced Nitride Technology Products) to be introduced.

This giant step forward results in LSI devices which are totally compatible with TTL, DTL and MOS, and as in the case of the Dual 16-bit DC Shift Register, lower in price than any other such device available.

The well-known performance and reliability advantages inherent to MTNS devices are, of course, present in all GIANT LSI circuits. These advantages include: a reduction in the number of system power supplies required, the elimination of interface circuitry, a reduced parts count and fewer interconnections, lower power dissipation, increased operating frequency and an increased operating temperature range.

The most outstanding feature of General Instrument's Dual 16-bit DC Shift Register—and of every standard GIANT product—is the exclusive V_{BB} terminal, which gives the user a choice of interfacing directly with TTL/DTL or MOS (as shown in the block diagrams above).

This shift register contains two independent 16-bit DC to 2MHz shift registers constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Independent single phase TTL/DTL compatible clock and data inputs are provided for both registers. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logical level of the clock. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition. Separate input data selector controls are provided on each shift register. They determine which of the two inputs shall be shifted into the register. Each shift register also has its own set input which forces all stages of the register to a "1" level.

Among the other features of the Dual 16-bit DC Shift Register are: power dissipation of 120 mW, full military temperature range of −55°C to +125°C, high input impedance, stable threshold over time vs. temperature, multiplexible inputs, the need for fewer packages compared to equivalent TTL/DTL circuits, and set control.

The General Instrument Dual 16-bit DC Shift Registers are truly GIANTs among shift registers. They are immediately available from your authorized General Instrument Distributor.

For full information write, General Instrument Corporation, Dept. D, 600 West John Street, Hicksville, L.I., N.Y. 11802.

(In Europe, write to General Instrument Europe S.P.A., Piazza Amendola 9, 20149 Milano, Italy; in the U.K., to General Instrument U.K., Ltd., Stonefield Way, Victoria Road, South Ruislip, Middlesex, England.)

*$7.50 each in quantities of 100 pcs. in a TO-72 package (GI part #SS-6-8212). Also available in a 16-lead dual in-line package (GI part #SS-6-8211) at $13.80 each in quantities of 100 pcs.

GENERAL INSTRUMENT

GENERAL INSTRUMENT CORPORATION • 600 WEST JOHN STREET, HICKSVILLE, L. I., NEW YORK

CIRCLE 4 ON INQUIRY CARD

The Friden 1150 Digital Printer.

It didn't fail us. So it won't fail you.

For nearly two years now, the Friden* 1150 Digital Printer has been an integral part of our electronic printing calculator.

So we know all about its reliability from first-hand experience, out in the field.

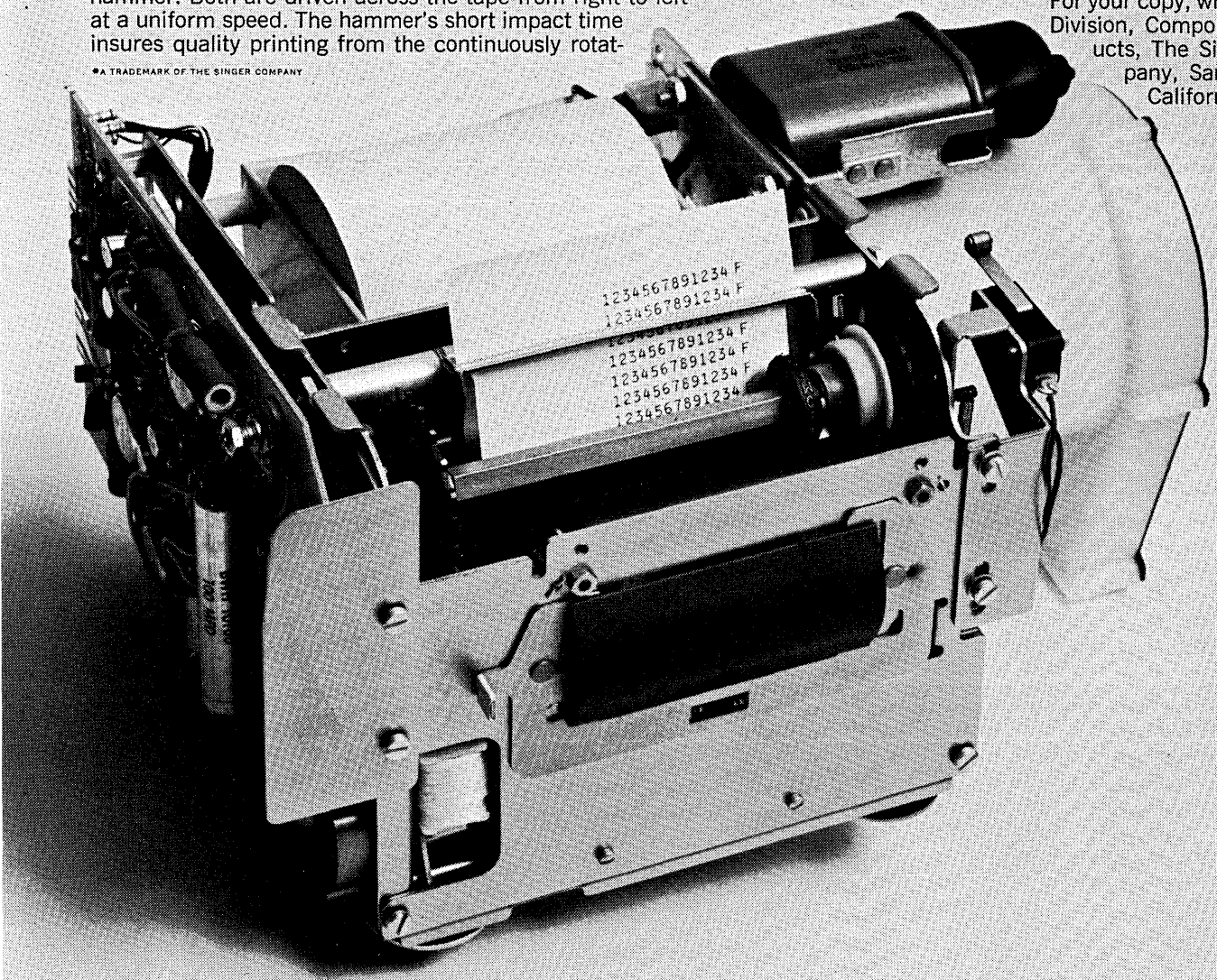
This 50-character-a-second printer is *durable* because it has fewer moving parts than ordinary medium-speed printers. It is easier to maintain. This means less downtime for your OEM product. The 1150 Digital Printer contains a single 20-character print wheel and a synchronized print hammer. Both are driven across the tape from right to left at a uniform speed. The hammer's short impact time insures quality printing from the continuously rotating wheel. And we have eliminated messy ribbons with our disposable ink roller.

Logic requirements are simple, making it easy to integrate the 1150 Digital Printer into your OEM product.

One more important thing: the 1150 Digital Printer is *not* expensive. It just sounds expensive. With its low initial cost and desirable operating features, the 1150 Digital Printer gives you a price/performance ratio unique among OEM printers.

The complete specs are all in our Specification 1001. For your copy, write: Friden Division, Component Products, The Singer Company, San Leandro, California 94577.

*A TRADEMARK OF THE SINGER COMPANY



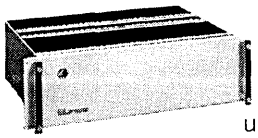
Friden Component Products. One way Singer serves OEM.

SINGER
FRIDEN DIVISION

CIRCLE 5 ON INQUIRY CARD

Throw out less versatile storage techniques. Now our core memories are priced for applications like these:

Digital Instrumentation ☐ Special Purpose Computers ☐ Numerical Control ☐ Data Manipulation ☐ Digital Display ☐ Buffers ☐ Data Acquisition ☐ Business Machines ☐ And Much More



Digital data handling, using devices less reliable and versatile than memory systems, has driven system designers to marvelous flights of ingenuity. We admire them.

The neat solution, though, is to select one of the 140 Ferroxcube FI-3 core memory systems. And now this is usually the low-cost solution, too. Even for applications in which you've never used core memory data storage.

In only 5¼" of panel space, our FI-3 memory system packs capacities from 1024 words of 6 bits to 8192 words of 18 bits in speeds of 3 microseconds and faster. That includes address registers, data registers, power supplies and memory retention.

If you don't need all that, we can plug any of them *out*. The FI-3 is entirely designed around modules that plug in . . . or out. We'll match your needs and your money.

Ferroxcube is first in memory systems with over 15,000 in use. These production-run, catalog standard systems are delivered fast. Often, right off the shelf. For your first switch to core memory design, who could help you more?

Write Peter DePiro for data. And prices you won't believe.

Ferroxcube
Systems Division, Englewood, Colo.
A NORTH AMERICAN PHILIPS COMPANY

Burbank, Calif.—(213) 849-6631; **Cleveland**—Data Tron, (216) EX 1-8421; **Denver**—Wm. J. Purdy Agents, (303) 794-4283; **Minneapolis**—(612) 920-1830; **Northlake, Ill.**—(312) 261-7880; **Orlando, Fla.**—W. A. Brown & Assoc., (305) 425-5505; **Phoenix**—(602) 264-3129; **San Francisco**—Wm. J. Purdy Agents, (415) 347-7701; **Saugerties, N.Y.**—(914) 246-2811; **Union, N.J.**—(201) 964-1844; **Waltham, Mass.**—(617) 899-3110; **Toronto, Ontario**—Philips Electron Devices, Ltd. (416) 425-5161.

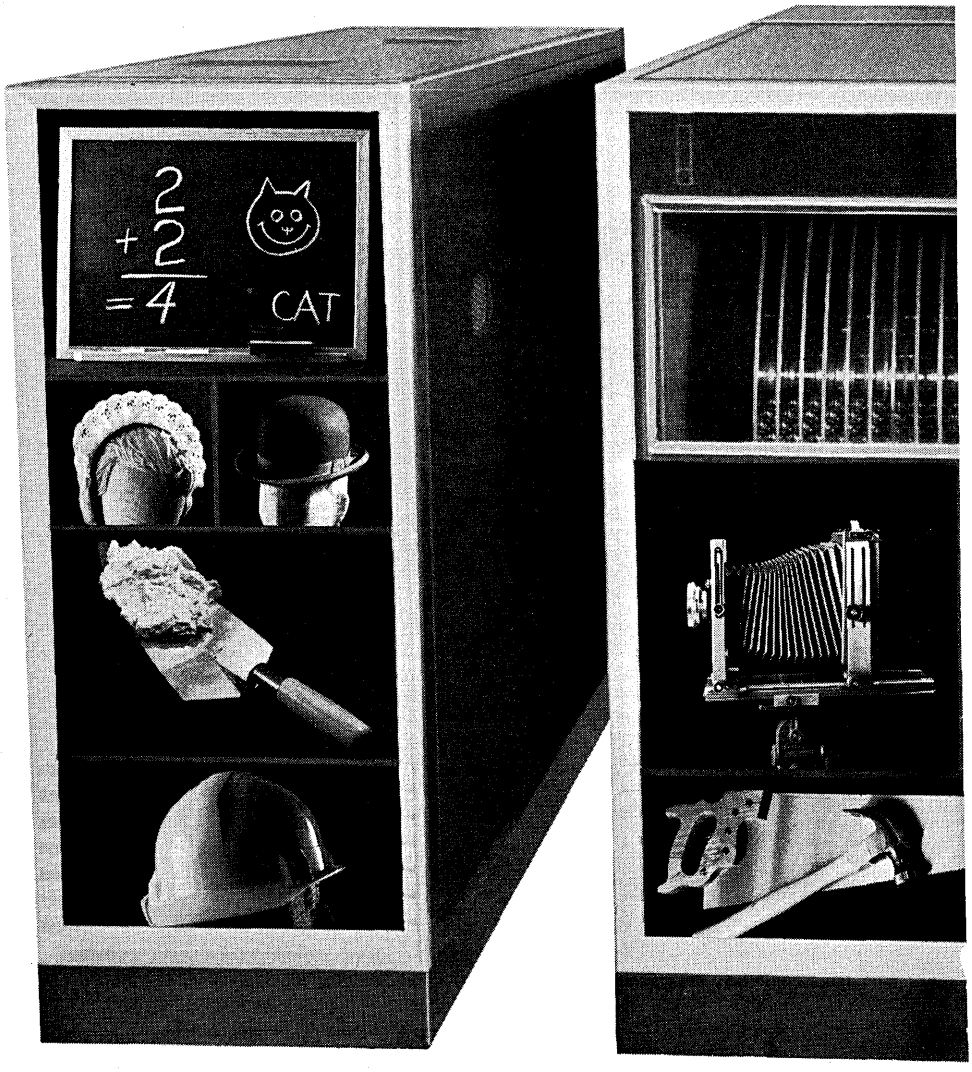
CIRCLE 6 ON INQUIRY CARD

Job

There are almost no limits to the time-sharing capabilities of Bryant equipment.

In this case, a computer and a huge Bryant memory system match the abilities and objectives of people seeking specific professions with those of prospective employers. Similar systems are in use on campuses, in military installations, and businesses of every description.

Bryant offers the largest and most experienced line of random access drum and disc file systems in the world. Systems that are standard with more computer

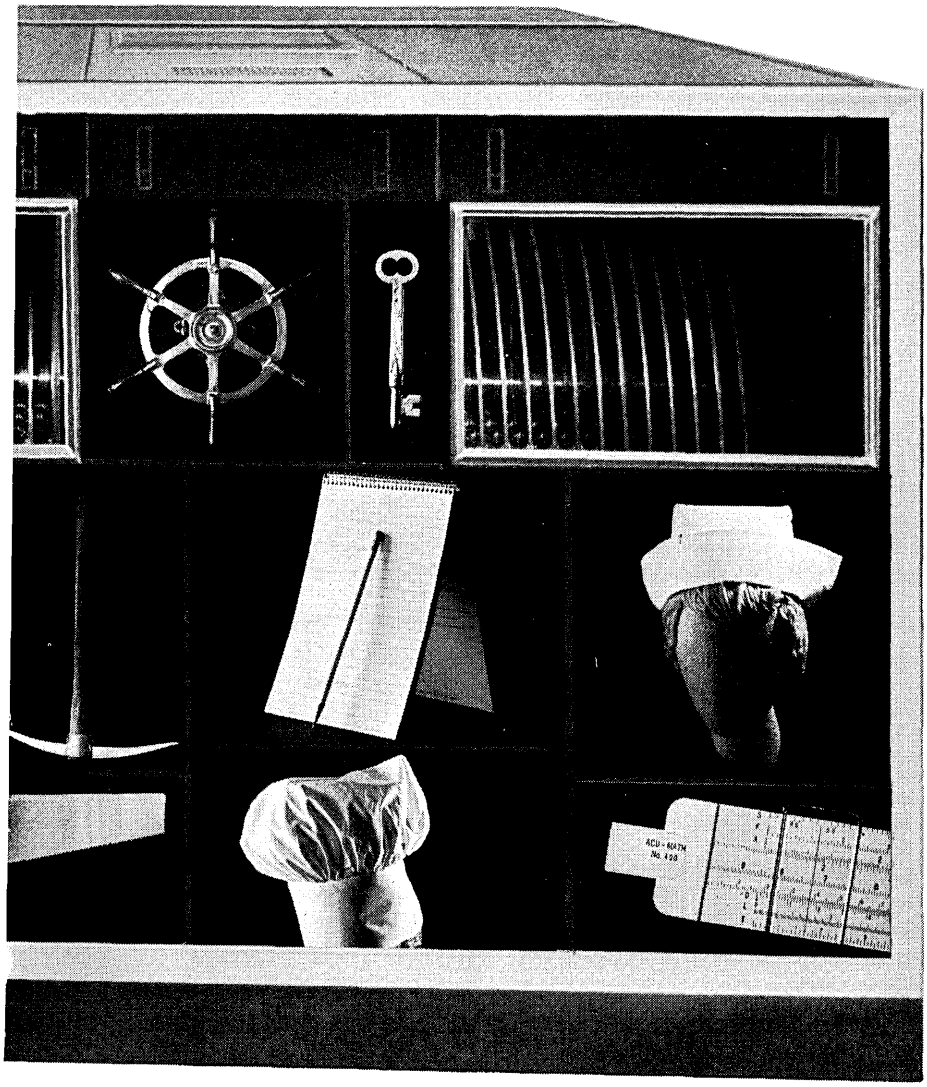


core.

manufacturers and independent time-sharing utilities than any other manufacturer. Most recently, with Digital's outstanding PDP-10.

Why the overwhelming popularity? Bryant has the best price/performance ratio of any computer manufacturer. Plus "tailored" solutions to customer problems and requirements.

Write us at 850 Ladd Rd., Walled Lake, Mich. 48088. We'll prove to you how easy it is to become a "Bryant Believer."



A match for any computer

BRYANT COMPUTER PRODUCTS

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EX-CELL-O CORPORATION

CIRCLE 7 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

In your April issue you published a letter by R. L. Dineley describing a simple method for treating product-of-sums logical expressions. An even simpler method is taught by D. A. Huffman. This method is based on recognizing that the Boolean expression will be zero when any of the factors in the product-of-sums form is zero. Plotting zeroes of factors on a Veitch diagram or Karnaugh map is as easy as locating ones for a sum-of-products expression.

To illustrate, using Dineley's example (A+BC) (A+C):

The zeroes resulting from A+BC will be located wherever both A and BC are zero. Therefore we locate on the map the expression $\overline{A}\cdot\overline{BC}$ (which is equal to $\overline{A}\cdot\overline{B} + \overline{A}\cdot\overline{C}$). Similarly the zeroes of A+C are located and plotted at $\overline{A}\cdot\overline{C}$. With all zeroes located, the rest of the map can be filled with ones. One can be a little more formal and work out algebraically the logical complement of the expression under consideration and then plot zeroes for that resulting expression. In a simple product-of-sums representation, however, the complementary terms can be written by inspection; or the zeroes can be plotted by inspection without writing the complementary expression.

James H. Hayes
Computer Center
University of California
Santa Cruz, Calif.

To the Editor:

I wish to add to my list of references for my article entitled "An Algorithin For the Synthesis of Complex Sequential Networks" published in the March 1969 issue of Computer Design Magazine. The reference is as follows:

Osborne, Thomas E., Lecture entitled: "Classical Reduction Involving Infrequently Used Variables," October 11, 1968, University of Santa Clara.

Mr. Osborne's work draws close similarity to that I presented in this article and thus, would certainly be of interest to those readers seeking further information.

I understand he has done work to apply the technique of infrequent variables to the design of sequential networks constructed from Read Only Memories. Since he has not yet published anything on this area, if readers would like additional information, they can write Mr. Osborne at:

Thomas E. Osborne
Building 1U
1501 Page Mill Road
Palo Alto, California

Thank you for the opportunity to publish with you.

G. W. Schultz
Central Data Systems, Inc.
Sunnyvale, Calif.

To the Editor:

I received the June issue of Computer Design this morning and was very pleased to read the article, "Impact of LSI on the Next Generation of Computers." It was a refreshing break from what has previously been printed on this subject because it presents a balanced point of view. The article was very well presented and whoever is responsible has indeed done a very creditable job of reporting.

I also like the emphasis on special subjects such as process control. Other issues emphasizing digital signal processing, CRT terminals, or communications processors may be worthwhile.

Abhay Bhushan
Project MAC
Massachusetts Institute of Technology
Cambridge, Mass.

Lockheed has the fastest 2½D memory in the world.

For quick home delivery call (213) 722-6810.

Or fast office delivery. Lockheed is the only company in the world that is actually producing 500 nanosecond 2½D memories at the rate of one a week. That's why you can get one faster from us than anyone else.

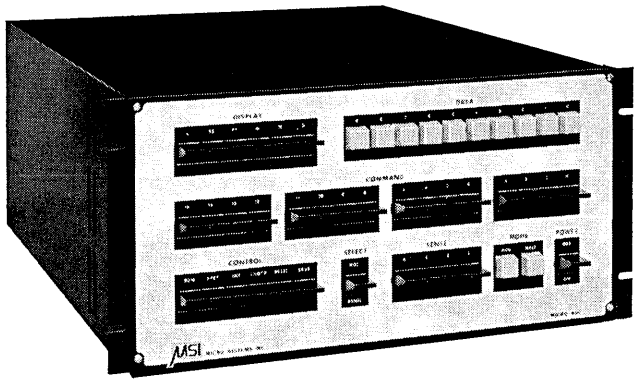
Lockheed's CD-50 is the world's fastest 2½D memory system. And it offers a wide range of standard storage capacities. From 8K to 65K words. The CD-50 provides inherently high operating margins. And total modularity gives it highly flexible interface capability, storage capacities, timing and control. Plus worst-case design gives the CD-50 an exceptional reliability rate.

So for the first human nanosecond response with technical material and full details on the CD-50, write to: Memory Products, Lockheed Electronics Company, Data Products Division, 6201 E. Randolph Street, Los Angeles, California 90022. Or, for fast home delivery call (213) 722-6810.

LOCKHEED ELECTRONICS COMPANY
LEC A Division of Lockheed Aircraft Corporation

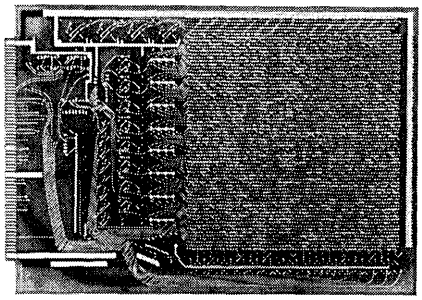
CIRCLE 9 ON INQUIRY CARD

If you're in the market for a mini computer, look at the Micro 800 first.



You'll probably end up with one anyway.

Here's one reason why: Microprogramming



Microprogramming gives you a more efficient system, tailor-made to your requirements, for less money. Since firmware absorbs many functions normally handled by core memory and interface hardware, requirements for both are reduced substantially. On the other hand, standard hardware can be retained even while changing architecture to match your particular demands. With little time and practically no effort, you can optimize computer characteristics for a particular operation without making a single hard wire change.

Here's another: Delivery

We began building 800's before we began selling them, and now we're in volume production. It's only natural then that delivery is off-the-shelf with custom variations taking a modest 30 days extra. Try us. Especially if your requirements are urgent.

Here's one more: Price

The Micro 800 costs $3200 with quantity discounts ranging up to 40%. For $3200 you get a basic processor with 16 multi-purpose registers, 256 words of read-only store, basic console, enclosure and power supply to function as a micro programmed controller. In addition, you get the fastest digital computer in its class with a 1.1μs memory cycle time and a 220ns micro command execution time. Core memory capacity is 0-32K bytes.

We also sell a microprogrammed adaptation of the 800 with 512 words of read-only store, a 4096-word by 8-bit core memory and a teletype interface. We call it the Micro 811 and it goes for $6300. Our third model, the $6900 Micro 810, is like the 811 except that 768 words of read-only store are used to implement an expanded instruction repertoire, including multiply and divide.

Just about any question you'll have is answered in our new mini-seminar booklet. We'll send you a copy gladly. But we'd really rather have you ask for a call from our marketing representative. You'll save a lot of time if you do because we're sure you'll end up with an 800 anyway. It's irresistible.

MSI **MICRO SYSTEMS INC.** 644 EAST YOUNG STREET • SANTA ANA, CALIFORNIA 92705 • TELEPHONE (714) 540-6730

CIRCLE 10 ON INQUIRY CARD

CONFERENCE CALENDAR

July 23-25—Conf. on Digital Methods of Measurement, U. of Kent, Canterbury, Kent, Eng. Spsr: IERE, IEE, U.K. & Rep. of Ireland Sec. Info: Conference Registrar, IERE, 8/9 Bedford Sq., London, W. C. 1 Eng.

Aug. 5-7—Joint Automatic Control Conf., U. of Colorado, Boulder, Colo. Spsr: IEEE Automatic Control Group, AACC, Info: W. E. Schiesser, Dept. of Chem. Engrg., Lehigh U., Bethlehem, Pa.

Aug. 11-16—Current Trends in Automatic Control Theory, Washington U., St. Louis, Mo. Info: Dr. G. L. Esterson, Box 1048, Div. of Continuing Professional Education, Wash. U., St. Louis, Mo.

Aug. 19-22—WESCON, Cow Palace & San Francisco Hilton Hotel, San Francisco, Calif. Spsr: IEEE Region 6, WEMA. Info: WESCON, 3600 Wilshire Blvd., Los Angeles, Calif.

Aug. 19-20—Seminar on "The Science and Technology of Information Display," Polytechnic Inst. of Brooklyn Graduate Ctr., Farmingdale, L.I. Spsrs: Polytechnic Inst. of Brooklyn (Office of Special Programs) and the Soc. for Info. Display. Info: Mrs. Helen Warren, Admin. Off., L.I. Graduate Ctr., Polytechnic Inst. of Brooklyn, Rte. 110, Farmingdale, L.I., N.Y.

Aug. 25-29—Info. Processing Short Course, Purdue U. School of Electrical Engrg. Info: Prof. E. A. Patrick, School of Elec. Engrg., Purdue U., Lafayette, Ind.

Sept. 8-12—Int'l Symposium on Man-Machine Systems, St. John's College, Camb., Eng. Spsr: IEEE. Info: Prof. L. R. Young, Rm. 37-155, M.I.T., Camb., Mass.

Sept. 15-20—Int'l Symposium on "the Design and Applications of Logical Systems," Brussels, Belgium. Spsrs: Societe Royale Belge des Electriciens, Electronics and Automatic Control Labs. U. of Brussels. Info: Dr. J. Florine, Intn. Symposium, Electronic Ind. Lab., U. of Brussels, 50 F. D. Roosevelt Ave., Brussels, Belgium.

Sept. 16-18—Electro-Optical Sys. Design Conf., New York City Coliseum, N.Y. Spsr: Industrial and Scientific Conf. Management, Inc. Info: Tech. Papers Comm., Electro-Optical Syst. Design Conf., 222 W. Adams St., Chicago, Ill.

With every Raytheon computer you get AID... plug-in interface for incompatibles.

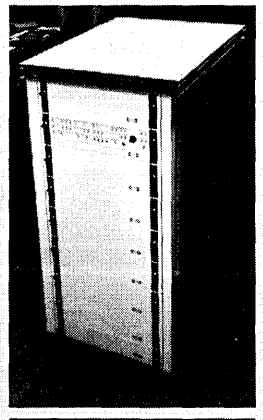
It's one thing to match a systems computer like the 706 to standard peripherals. But what about non-standards? Pick analog and parallel interfaces, scopes, data acquisition systems, or something you happen to have on the shelf.

The AID concept, (Applications Interface Device) for the 706, handles them all. A series of functionally modular blocks lets you interface the 706 with your input or output conveniently, quickly and economically.

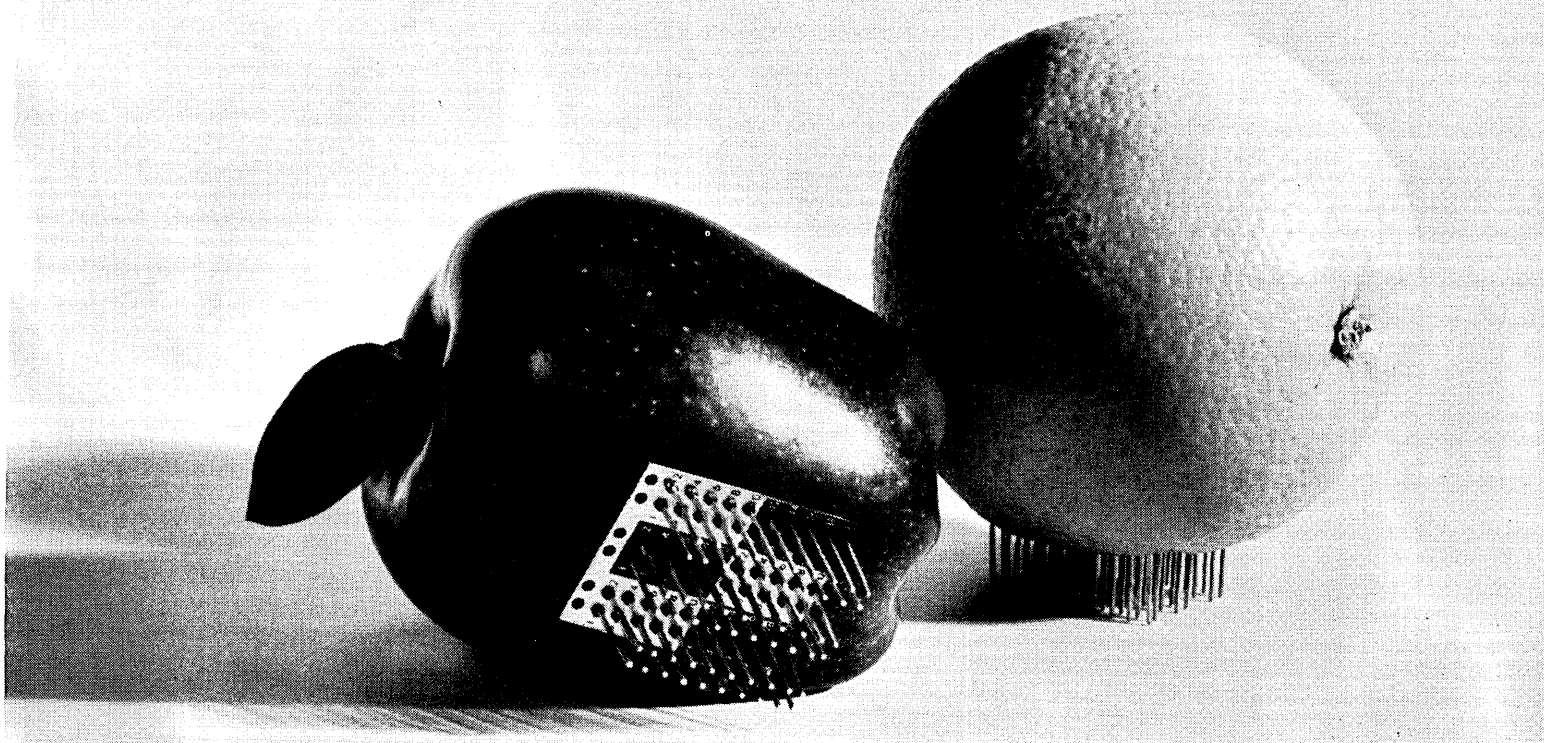
AID blocks go well with standard equipment too. They're compatible with our packaged system instruments like the MINIVERTER™ which combines multiplexing, sample-and-hold and a/d conversion. This means you can get an analog front end, interface, computer and your output devices from one place—RAYTHEON.

AID modules simplify timing, coding, buffering and control logic. Thus expensive systems, design and checkout time is dramatically reduced.

AID is just one more reason why the 706, with a basic price of $19,000, is becoming the systems designer's choice. Write or call today for Data File CB170. Raytheon Computer, 2700 S. Fairview, Santa Ana, California 92704. Telephone (714) 546-7160.



RAYTHEON

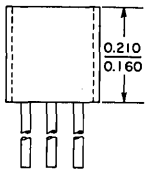


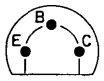
CIRCLE 12 ON INQUIRY CARD

GET

a new source of reliable epoxy case replacements for TO-18 transistors

The General Electric GET transistor series is your new answer to circuit design problems. GET is the most recent member of GE's proved epoxy encapsulated transistor family dating back to 1962 . . . over 6 years of epoxy experience.





GET's package design conforms to TO-18 mounting patterns in existing PC boards. It's the ideal epoxy replacement for "hermetic devices" . . . no expensive redesign necessary.

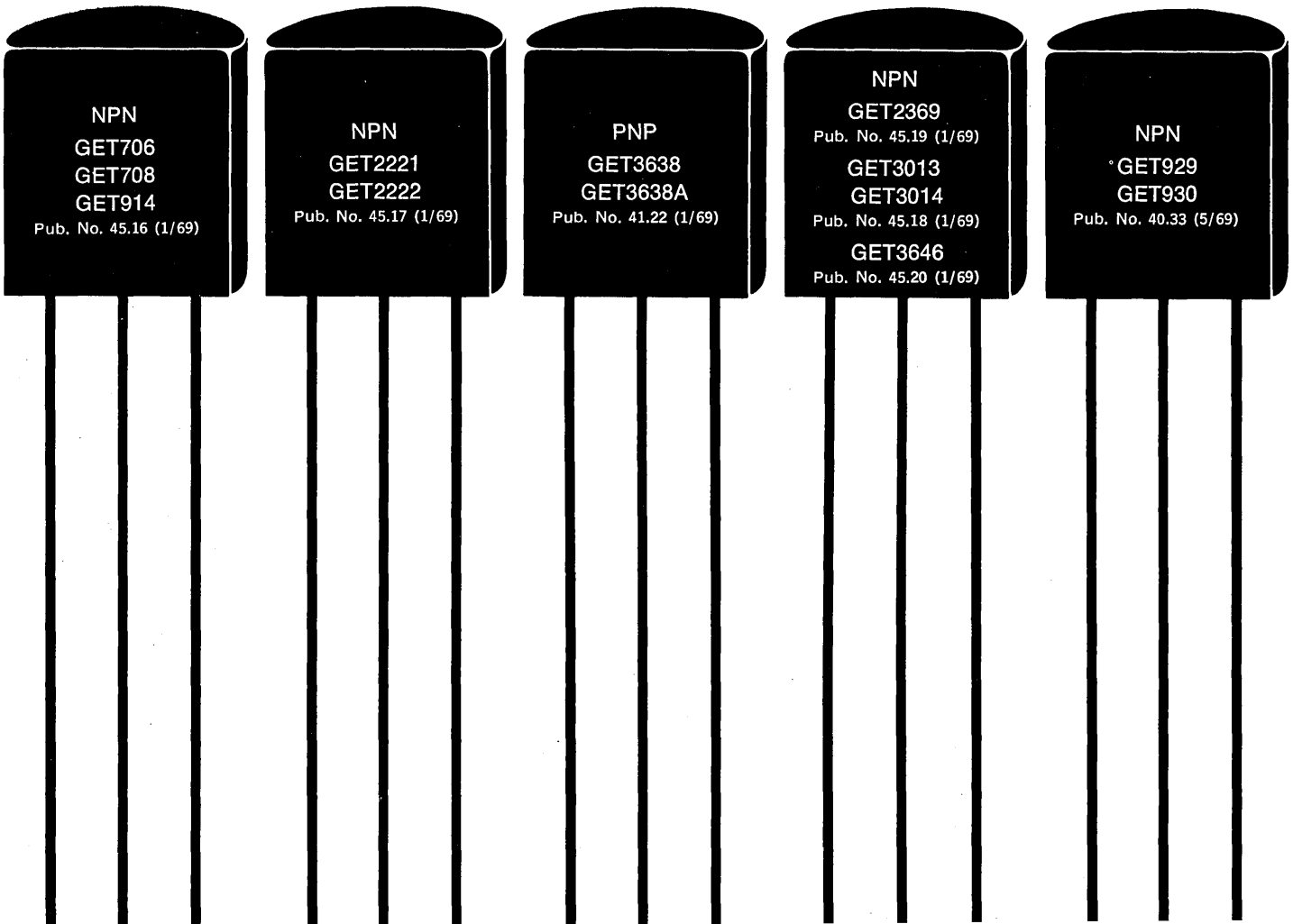
These new units use the same industry proved production methods and quality epoxy that made our TO-98 (D16) series so successful. GE epoxy plastic forms a true chemical bond with metal to curb moisture permeation, eliminate internal wire lead fatigue failures, and vibration destruction. Low profile package design means smaller circuits and lower cost.

General Electric epoxy has the ability to contend successfully with a wide range of environmental conditions as shown in the extensive Reliability Evaluation Program described in Pub. 95.36A. Failures experienced with hermetic devices under these levels of shock, acceleration and stress have been eliminated with GE's solid epoxy encapsulant.

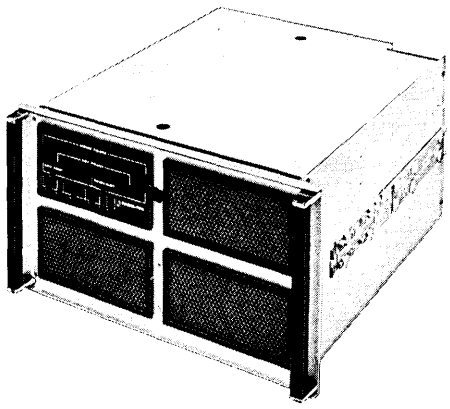
Standard NPN and PNP devices are available now through GE distributors. Five family groups representing GE's new epoxy transistor lines are shown below. Additional family types are being added. For more information on GET's for all applications, plus GE's "specials" capability, call or write your GE sales representative or distributor, or write General Electric Company, Section 220-69, 1 River Road, Schenectady, N.Y. 12305. In Canada: Canadian General Electric, 189 Dufferin Street, Toronto, Ont. Export: Electronic Component Sales, IGE Export Division, 159 Madison Avenue, New York, N.Y. 10016.

GENERAL ELECTRIC

CIRCLE 13 ON INQUIRY CARD



Space trade-offs are a pain in the rack



...and Fabri-Tek's NEW 380 Core Memory System packs 655,380 bits of fast relief in a case that's only 10½" x 19" x 21" ... including complete power supply!

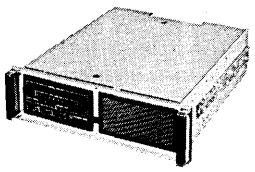
Or maybe you need even more capacity. Fine. The new 380 System is *expandable to over 2.6 megabits!* Which is a lot of storage.

And you don't have to trade off reliability or maintainability to get that kind of capacity, either. We've included plenty of plug-ins for fast access to *all* subassemblies. Interchangeable printed-circuit cards to help simplify trouble-shooting. A pluggable tester (optional) for fast, on-line maintenance. Unique DC coupling in and out of the memory stack (for stable operating margins, fewer components, and increased reliability). Plus sliding mounting arms that permit the chassis to be pulled out of the rack easily and tilted 90° either way for fast servicing.

The 380 also includes our *automatic* DATA SAVER™ feature to minimize recovery time after any unpredicted temporary loss of external power. (Guards against any loss of data, too — *and there's no manual reset required to get back on line!)*

Speed? 950 nanoseconds. And of course word or byte control plus parity generation and checking are available.

If your storage requirements are less than 655,380 bits, you can save even more rack space by going to our **370 system.** It's got the same major advantages as the 380 system scaled down to a 5¼" x 19" x 21" case with a capacity of 163,840 bits (field-expandable in increments to 655,380 bits), and speeds ranging from 750 nanoseconds to 1.5 microseconds. Both systems are ideal for nearly any kind of data processing. See your Fabri-tek Representative for complete specs, or call or write us direct.



Fabri-Tek is a leader in advanced memory research, development and production. Our experienced Application Engineers are ready to help you find solutions to static and dynamic storage applications: Buffer Memories • Extender Memories • Peripheral Mass Memories • Mil-Spec Memories.

FABRI-TEK

5901 South County Road 18 • Minneapolis, Minnesota 55436 • Tel: 612-935-8811 TWX: 910-576-2913
Blantyre Industrial Estate • High Blantyre, Lanarkshire, Scotland • Tel: Blantyre 2474 TWX: 851-778-448

CIRCLE 14 ON INQUIRY CARD

Be a Dr. Doolittle...
TALK TO YOUR CPU

Think about it! What could it mean if you could pick up the phone, call your computer and get your question answered *now!* Your people could make immediate credit checks, keep track of inventory, find out the latest blueprint revision numbers, get the status of savings or checking accounts, or anything else that's programmed into the computer. How? The Cognitronics Speechmaker†— a multiplexed voice response system. Interfaced with your computer (it's compatible with virtually any computer available), Speechmaker provides immediate retrieval of the vital information that's needed quickly for efficient business management. The Input/Output terminal is an inexpensive Touch-Tone® telephone and the Speechmaker vocabulary of up to 189 words is tailored specifically for each application. Multiplexing allows independent, simultaneous multiple outputs over an unlimited number of lines. *Free Demonstration* — For complete information and to arrange for a demonstration of the Speechmaker, write or call today.

Cognitronics Corporation

333 Bedford Road, Mount Kisco, N. Y. 10549 / (914) 666-2941

® Registered Trademark of the Bell System

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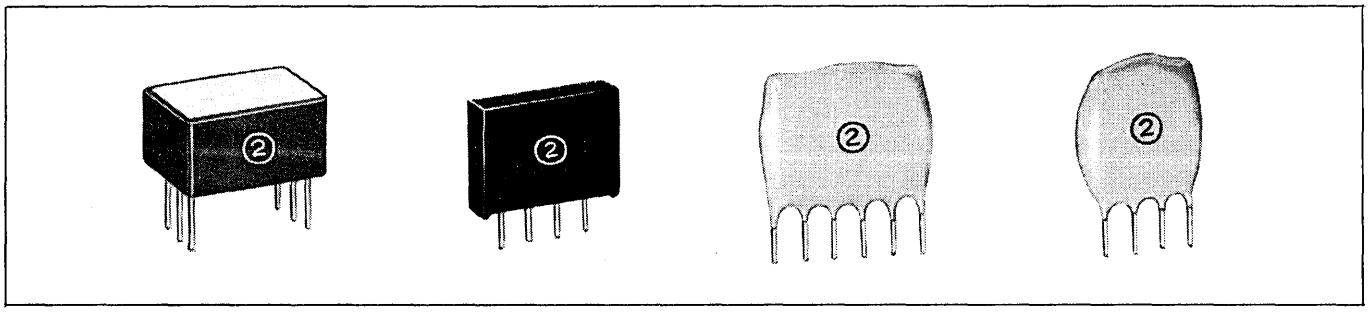
CIRCLE 15 ON INQUIRY CARD

Now from Sprague Electric!

Your *custom* pulse transformer is a *standard* DST* transformer



Some of the case styles in which Sprague DST Pulse Transformers are available. Note the in-line leads.

You can select the transformer design you need from the new Sprague DST Family, a fully-characterized series of Designer Specified Transformers which Sprague Electric has pioneered. It's easy. Start with the two basic parameters dictated by your circuit requirements: primary (magnetizing) inductance and volt-second capacity.

New Sprague engineering data gives basic information from which all nominal sine wave parameters are derived. This data allows you to specify the one transformer from thousands of possibilities which will optimize performance in your application.

Design Style A minimizes magnetizing inductance change as a function of temperature. Typically it's $< \pm 10\%$ change from 0 to 60 C; $< \pm 30\%$ from -55 to $+85$ C.

Design Style B and C give you broad bandpass characteristics, and still keep magnetizing inductance change $< \pm 15\%$ from 0 to 60 C.

Design Style D is *fast*. Associated leakage inductance and coupling capacitance are kept at a minimum. This style is just what you need for interstage and coupling devices in computer drive circuits.

The Sprague DST Series packs a lot of transformer into minimum volume packages — epoxy dipped for minimum cost, or pre-molded. The 100 mil in-line lead spacing is compatible with integrated circuit mounting dimensions on printed wiring boards.

To solve your pulse transformer design, start now. Write for Engineering Bulletin 40,350 to the Technical Literature Service, Sprague Electric Company, 555 Marshall St., North Adams, Massachusetts 01247.

*Trademark

SPRAGUE COMPONENTS

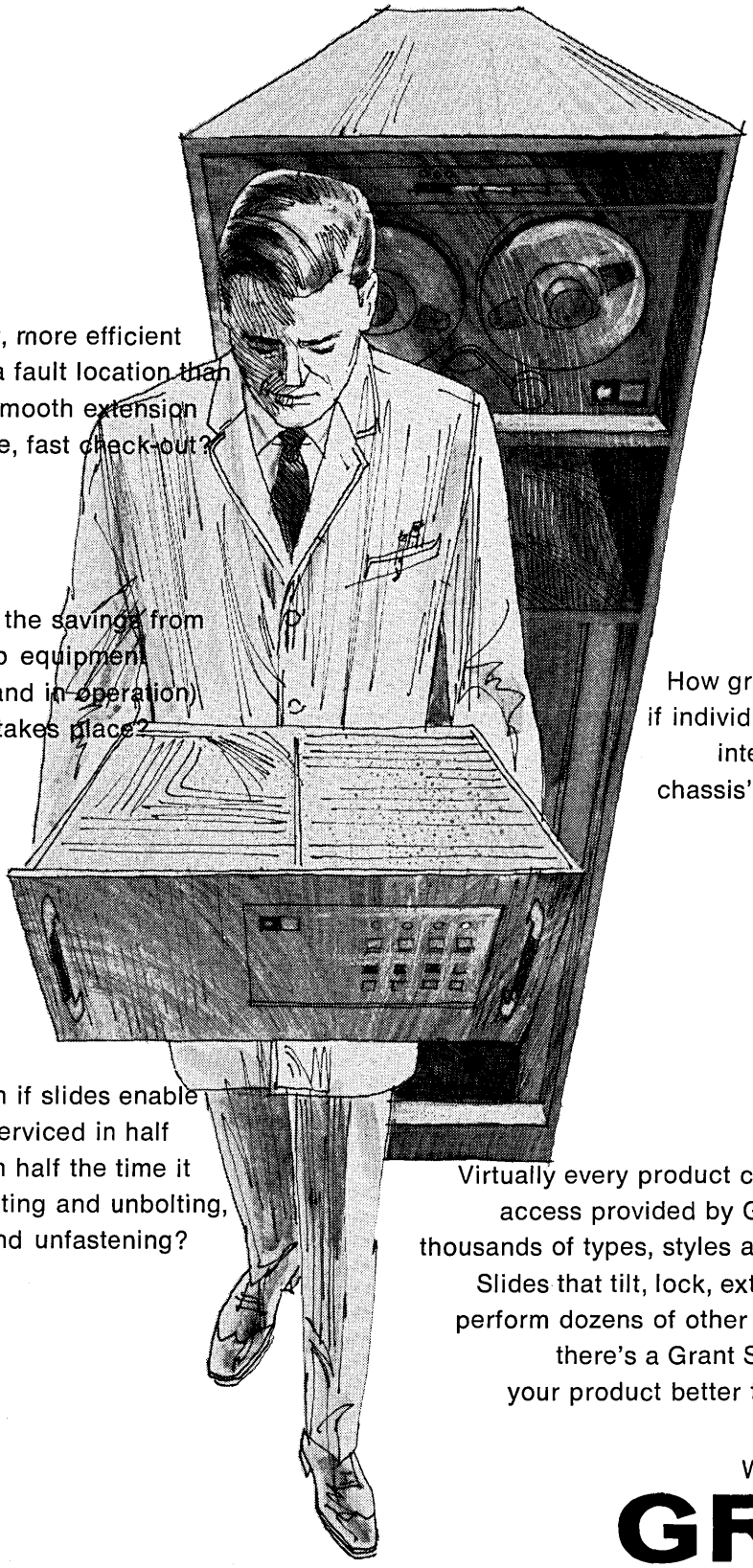
PULSE TRANSFORMERS	INTEGRATED CIRCUITS	CERAMIC-BASE PRINTED NETWORKS
THIN-FILM MICROCIRCUITS	INTERFERENCE FILTERS	PACKAGED COMPONENT ASSEMBLIES
TRANSISTORS	PULSE-FORMING NETWORKS	BOBBIN and TAPE WOUND MAGNETIC CORES
CAPACITORS	TOROIDAL INDUCTORS	SILICON RECTIFIER GATE CONTROLS
RESISTORS	ELECTRIC WAVE FILTERS	FUNCTIONAL DIGITAL CIRCUITS

4SSC-7137R2

SPRAGUE®
THE MARK OF RELIABILITY

CIRCLE 16 ON INQUIRY CARD

So what if Grant Slides save hours of down time?



Is there a quicker, more efficient way to get to a fault location than by immediate and smooth extension of the unit for simple, fast check-out?

Would you guess the savings from being able to keep equipment connected (and in operation) while maintenance takes place?

How great is the value of slides if individual chassis' can be interchanged with similar chassis' in moments?

What's it worth if slides enable equipment to be serviced in half —or less than half the time it ordinarily takes bolting and unbolting, fastening and unfastening?

Virtually every product can use the ready access provided by Grant Slides. There are thousands of types, styles and sizes available. Slides that tilt, lock, extend and lock and perform dozens of other functions. Undoubtedly, there's a Grant Slide that can help make your product better too.

Write for complete data.

GRANT
PULLEY & HARDWARE CORPORATION

EASTERN DIVISION: 230 HIGH STREET, WEST NYACK, NEW YORK 10994
WESTERN DIVISION: 944 LONG BEACH AVE., LOS ANGELES, CALIF. 90021

CIRCLE 17 ON INQUIRY CARD

New System 18/30...

computerized automation in easy, economical steps.

A computerized automation system must first perform today's tasks economically and predictably. The new GA 18/30 industrial computer system is the only automation system to do just that.

The 18/30 system centers around a family of compatible GA automation computers designed to work in distributed management information and control systems. The GA worker-level computers permit the user to automate at the primary control loop first, with predictable results and costs—and then add to these automation functions GA supervisory-level computers for total process optimization.

The heart of our new System 18/30 is the 1804 processor, which is fully software compatible at the binary code level with the IBM 1800 and 1130 computers and will work with or extend existing IBM 1800 installations. The 1804 executes over 400,000 instructions per second, has a core memory with a 960-nanosecond cycle time, has a 16-word MSI scratch pad memory with a 35-nanosecond cycle time, hardware double precision arithmetic with multiply and divide, memory storage protect and parity bits, and a 16-bit word and Input/Output rates over 1,600,000 characters per second.

The 1804 acts as a supervisory computer for several SPC-12 dedicated computers. SPC-12 is our primary control loop computer or worker computer. It ties to your machines, devices, communication networks, sensors and instruments through our unique family of mini-controllers to form a primary control loop automation system. With GA unique Product Software, control programs can be accomplished quickly, economically, and on a fixed price basis. GA terminals, communication pre/post processors, process I/O, and data processing I/O, and computer to computer connectors provide the system building blocks required to take on large scale automation on a step by step basis with each step on a predictable cost and results basis.

Our Automation Sciences Division will provide all the process analysis, engineering, programming, installation and start-up service you need.

So if you have an automation requirement, large or small, ask us about step by step automation at any of our nation-wide sales offices. Or write for our System 18/30 Brochure.

GENERAL AUTOMATION, INC.
Automation Products Division,
706 West Katella, Orange, Calif. (714) 633-1091

Sales Offices: Waltham, Mass. (617) 899-6170 • Willow Grove, Pa. (215) 657-2657 • New Rochelle, N.Y. (914) 235-9300 • Eau Gallie, Fla. (305) 727-3205 • Wheeling, Ill. (312) 537-3500 • Cleveland, O. (216) 333-8366 • Dallas, Tex. (214) 358-0271 • Los Altos, Calif. (415) 941-5963 • Orange, Calif. (714) 633-1091.

CIRCLE 18 ON INQUIRY CARD

30-gage wire needs Kynar®. If you've ever tried to locate a short in thousands of feet of small-gage computer wire, you'll appreciate the toughness found in insulation of Kynar.

With twice the cut-through resistance of totally fluorinated plastics, Kynar eliminates the worry over physical damage to the wire. You can bend it, loop it and pull it over knife-sharp edges without harm. It's compatible with automatic wiring machines or hand tools. And it cuts and strips fast and smoothly.

But Kynar's toughness isn't all mechanical. It resists cleaning solvents, won't degrade with age and operates at temperatures of from −80° to +300°F.

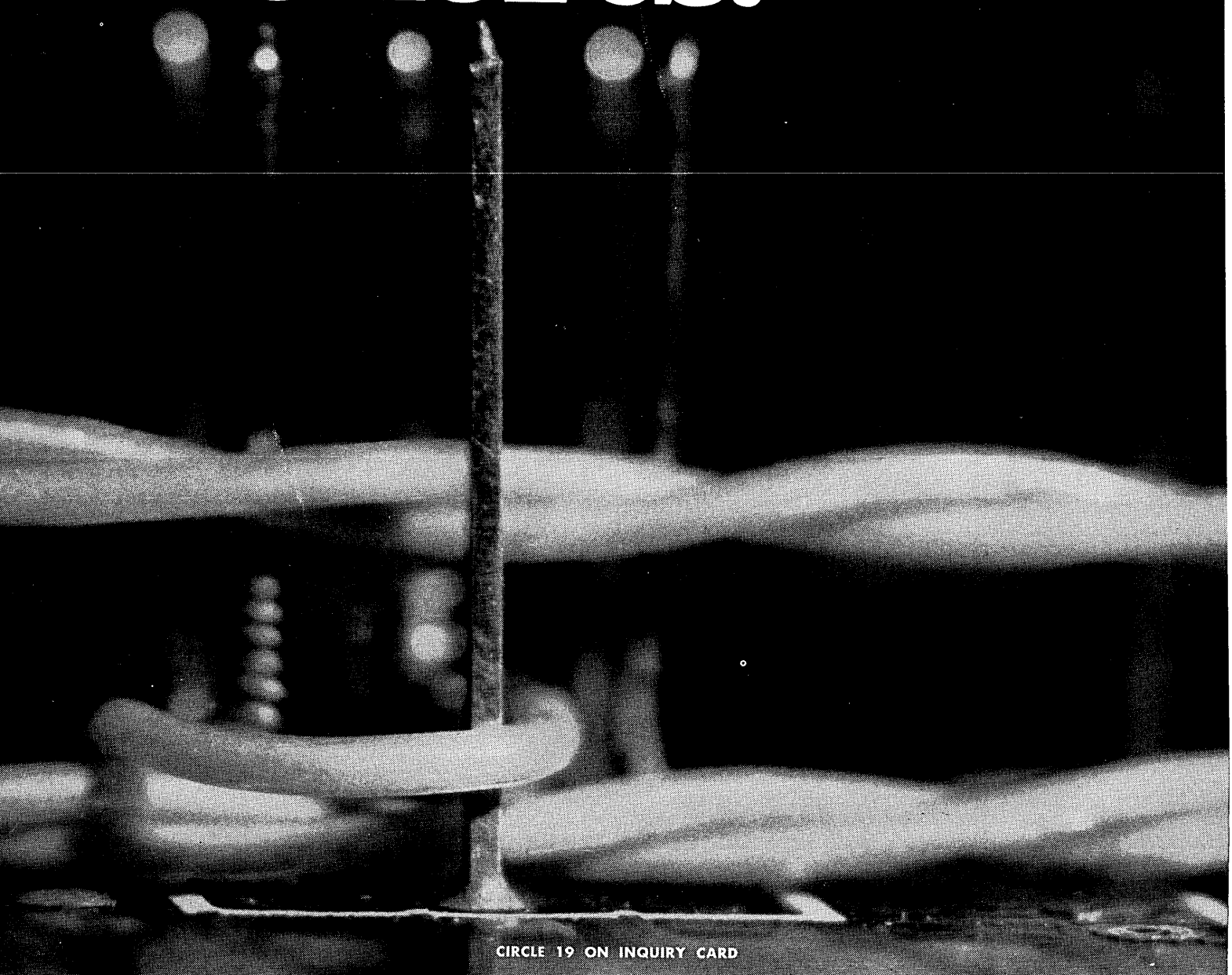
For samples and information, write: Plastics Department, Pennwalt Corporation, 3 Penn Center, Philadelphia, Pennsylvania 19102.

®Kynar is Pennwalt's registered trademark for its vinylidene fluoride resin

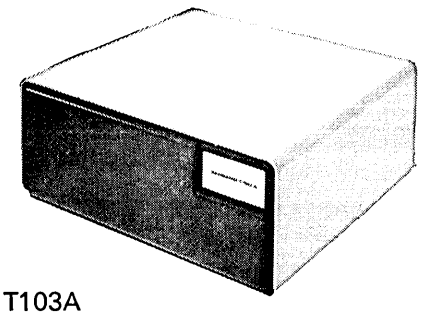
KYNAR®. . . the fluoroplastic that's tough!

PENNWALT
ENGINEERING PLASTICS

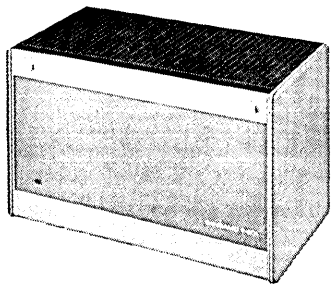
down with shorts.



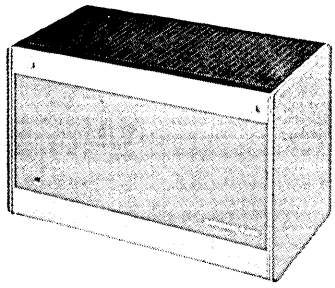
CIRCLE 19 ON INQUIRY CARD



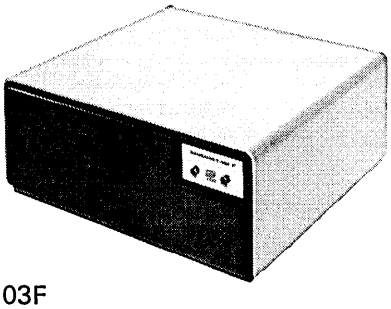
T103A



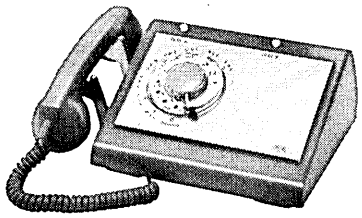
T201B



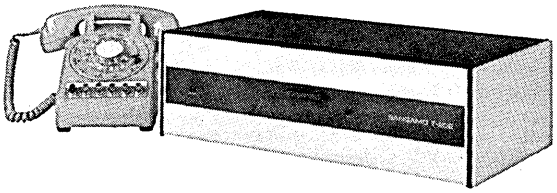
T201A



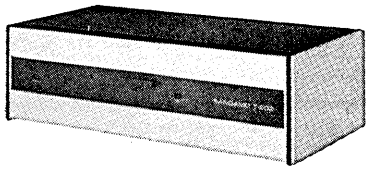
T103F



T401E

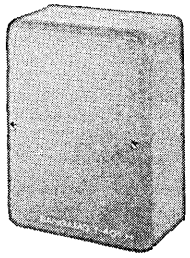


T202C



T202D

SANGAMODEMS...
the most complete line of Bell compatible data sets!



T401H

Have you been purchasing data sets here and there? You don't have to! SANGAMO can supply 93% of your data set requirements with guaranteed Bell compatible units *now*.

Check this listing:

103A1	201A1	202D4	202C7
103A2	201A2	202C1	202C8
103F2	201A3	202C2	401E2
201B1	201A4	202C3	401E3
201B2	202D1	202C4	401E4
201B3	202D2	202C5	401E5
201B4	202D3	202C6	401H1

We can also supply customized variations of these standard sets, with obvious economies for unlimited applications.

Field Service Contracts available on request.

Need Data Sets? Let's communicate!

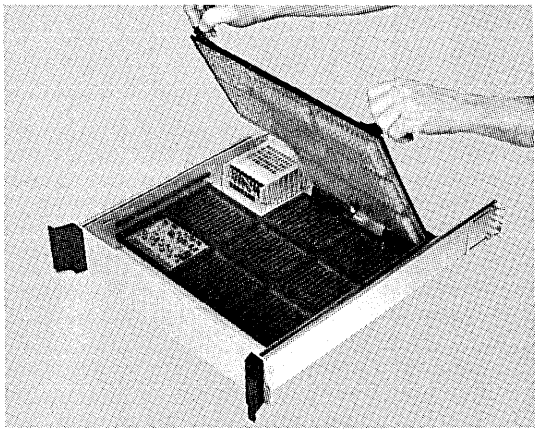
T69-05

Communication Systems
SANGAMO
Electric Company
Springfield, Illinois 62705
217 544-6411

CIRCLE 20 ON INQUIRY CARD

With EECO 2D computer-automated plug-in IC Hardware...

less than 30 days separate schematic and final system...



When you specify EECO 2D Hardware a computer converts your "Pin Logic List"* into a wire plan and checks for errors and omissions before wiring begins. EECO plugs in the IC's, machine Wire-Wraps the backplanes and in days...your schematic is a drawer of working electronics with all necessary computer generated support documentation.

EECO 2D Hardware System provides more than time savings...it's up to 30% more economical...and it's versatile...ready for digital or analog IC's, discrete components, MSI or LSI. It offers higher density — up to 768 IC's and a power supply fit in one 3-1/2" high standard drawer.

Your first step is simple...just phone, write or circle the reply number.

*You simply choose the module and write the signal name by each pin number. You don't worry where the wires go or the order of listing.

Catalog available.

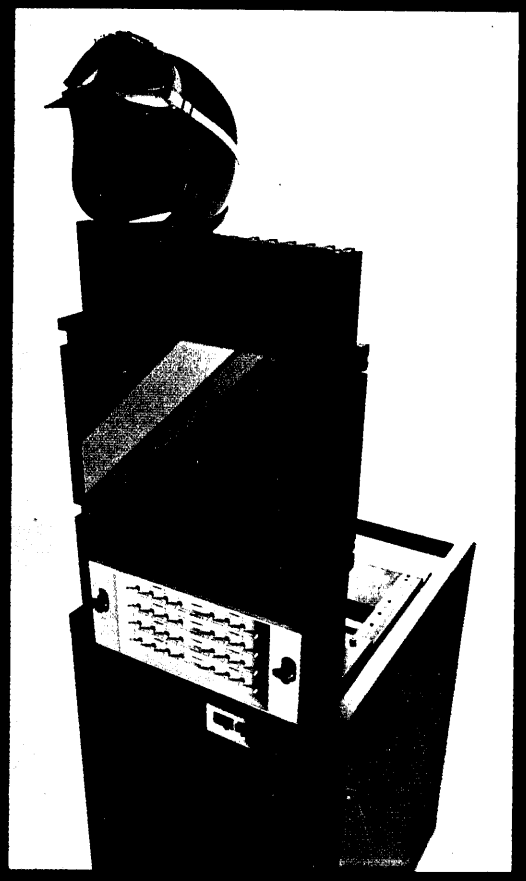
See EECO 2D at Wescon Booth numbers 3814 thru 3817

ELECTRONIC PRODUCTS DIVISION

ELECTRONIC ENGINEERING COMPANY OF CALIFORNIA

1441 EAST CHESTNUT AVENUE · SANTA ANA, CALIFORNIA 92701 · (714) 547-5651

CIRCLE 21 ON INQUIRY CARD



The DSU-8100 "Fastrack."™
A real winner in the mass memory race!

You don't win the Grand Prix or the "500" by driving a truck — or weaving all around the track. The same is true in the mass memory race.

Until now mass disc memories were ponderous brutes. They took up a dozen feet of valuable floor space. Weighed close to a ton. Required thousands of kilo-watts. Most used positioning heads which do have drawbacks. Time lost in positioning. Positioning errors. Positioner wear. Maintenance.

CPC has changed all this with a fast head-per-track disc memory which stores up to 200 million bits in a compact 19" chassis just 40" high. It weighs only 300 pounds. Requires but 1 Kw of power.

The secret to on-site expansion is the modularity. From one through four 25 million and/or 50 million bit disc modules may be used on the same compact drive. 256 "fail-safe" flying heads per surface access data fast. 16.7 milliseconds average. Data transfer rate is 3 MHz.

There's more to tell. Like the single disc security which eliminates the possibility of head avalanche. Or a worst-case-failure recovery time of only minutes. Or the ability to serve up to 3 controllers.

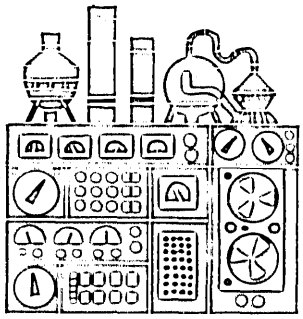
Want the whole exciting story? Request a copy of our DSU-8100 brochure.

cpc **computer peripherals corp.**
5037 Ruffner St., San Diego, Calif. 92111
Telephone (714) 279-7500

CIRCLE 22 ON INQUIRY CARD

DSU-8100 Fastrack™

A new concept in rotating memories . . .
Designed for the exploding world of
Program Swapping, Time Sharing,
Message Switching and Real Time Computing.



INDUSTRY NEWS

GE ENTERS MINI PROCESS COMPUTER MARKET—General Electric Co. has announced its entry into the mini process computer market with a flexible, read-only-memory-based computer which sells for under $10,000.

The GE-PAC 30 features 16-32 instruction programming, direct addressing to 64K bytes, plug-in modular design, and dual in-line IC's. The standard ROM can be unplugged and replaced by a special hardware diagnostic ROM/, which, in combination with a test set and symptom dictionary, permits rapid fault location.

The computer, with models designated GE-PAC 30-1 and 30-2, has software which is fully upward compatible between models, permitting growth without re-programming.

The major difference between the models is in instruction execution times. The 30-1 costs less and is more flexible due to the general-purpose organization of its micro-processor. The 30-2, with more commitment to hardware, is far more powerful at the user level.

Typical applications of the GE-PAC 30 will include production testing of electronic components, process control, loading terminal automation, instrument and sub-system control.

ADAPSO'S POSITION ON OEM PRICING POLICIES—The Association of Data Processing Service Organizations, Inc. recently released its first in a series of position papers on industry views, dealing with "Computer Manufacturers' Pricing Policies."

It is ADAPSO'S general position that the manufacturers' traditional practice of providing a variety of products and services in a single purchase or rental price represents in practice a tie-in sale and a form of price discrimination.

"ADAPSO believes that the best interests of all users (service organizations and others alike)," J. L. Dreyer, executive vice president, stated, "would be served if all computer manufacturers would price separately any service or function which is or can be available in the marketplace or provided by the user himself."

ADAPSO specifically recommends that systems engineering support, educational programs, and application-oriented software or programming be separated from the single price and offered to all customers at prices related to the cost of providing each unit of the service.

DATATROL TO MANUFACTURE ELECTRONICS HARDWARE — Datatrol Inc., a newly formed electronics hardware manufacturing company, has commenced its operations in Hudson, Mass. The company's four principals, Bob Fronk, president, Leon Jackson, vice president, Jack Dumser, and Frank Hibberd, were formerly with the Digital Equipment Corp.

The company will specialize in digital data communications equipment, computer displays, and industrial control systems. Products already being marketed include a display unit and three communications interfaces.

The display is Fastplot, a previewing device for incremental plotters. Using a Tektronix 611 storage tube, it connects directly to any computer equipped with an interface to an incremental plotter and makes use of all the standard plotting software. Interfaces include the CI-12, which provides communications to remote teletypes over full duplex lines using the dial-up network; the CI-15 is a multi-line communications interface providing four full duplex lines; data-talk CI-14 allows any user to call a computer using a touch-tone telephone and receive a response in spoken words.

RYDAX WILL MANUFACTURE DIGITAL MESSAGE SYSTEMS—The formation of Rydax, Inc., in San Rafael, Calif., has been announced by its president, Chandos A. Rypinski.

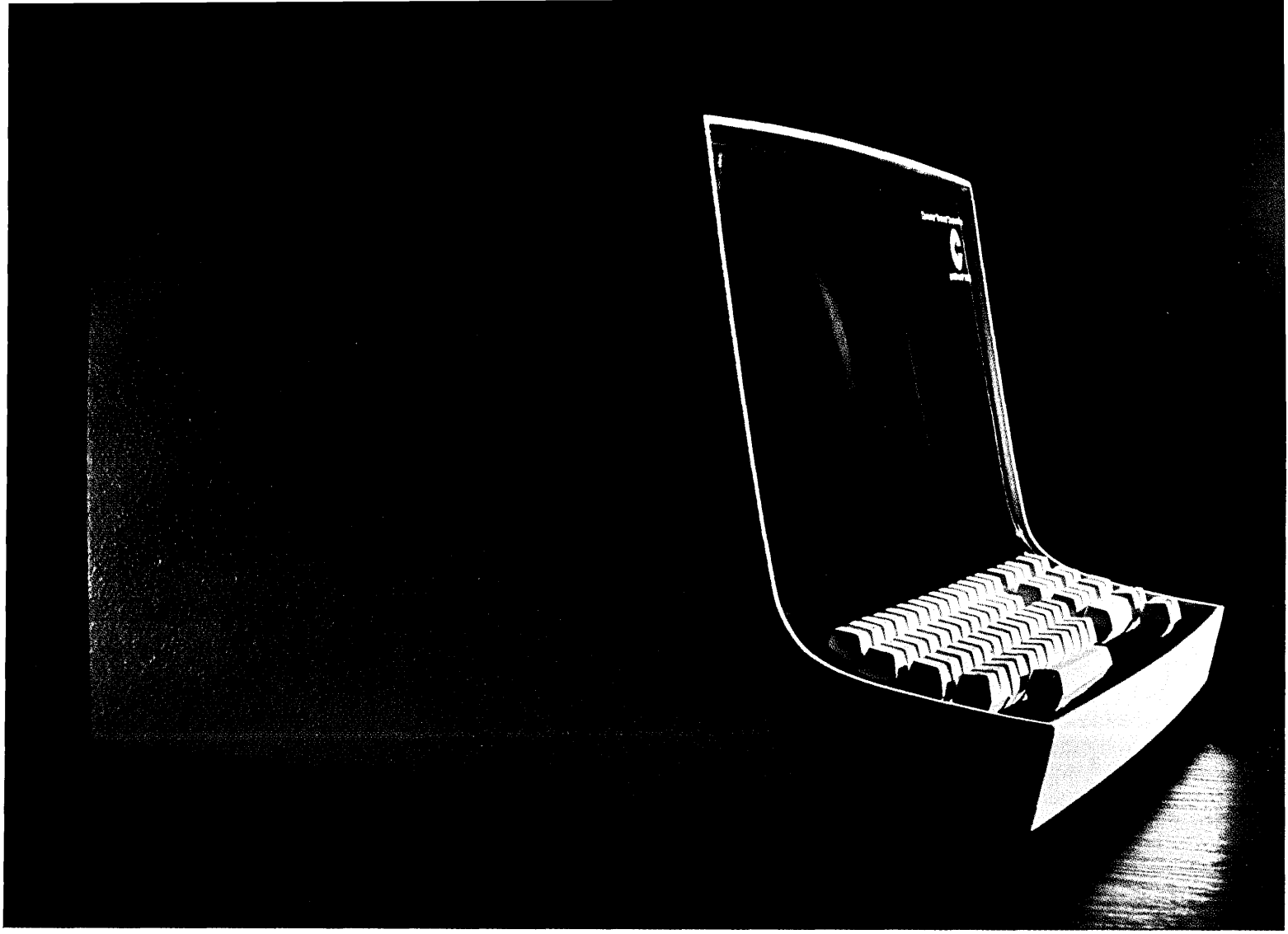
He explains, "There is a tremendous need for specialized digital communications systems in today's complex world. Rydax offers a sophisticated capability on a standard product basis. Among our products is a digital terminal identification system and alarm system module (SAM) built for the Southern California Rapid Transit District. To date more than 200 modules have been installed in its buses, providing automatic identification of all voice transmissions from the bus as well as silent alarms as a crime deterrent."

Marketing vice president Max W. Kuypers, states, "Our major product will be digital message systems for data acquisition, monitoring, and supervisory control systems. Because of their compatibility with all radio, microwave, and telephone line networks, Rydax products are useful for public utilities and transportation systems, as well as industrial monitoring and control applications."

Rydax will also manufacture remote control terminals for teleprinters at attended and unattended high-frequency radio stations, featuring dual channel configuration for error correction, parity error detection and pulse regeneration, as well as address and control features for automatic operation.

SURVEY OF FACSIMILE FEATURED IN AUERBACH DIGEST—The latest edition of the Auerbach Computer Characteristics Digest features an article on facsimile devices, which sketches the historical development of facsimile technology, provides succinct characterizations of 22 general-purpose systems, and surveys the available units that can operate over common-carrier facilities. Selected for more detailed coverage are two representative systems: Xerox-LDX and Stewart Warner-Dial Dataflex.

A discussion of new developments in facsimile networks describes the franchising concept, similar to mail-



If you've got something to say to a computer you can say it best with a Datapoint 3300 — Here's why:

*** The Datapoint 3300 is the *first* data terminal to be designed *specifically* for interactive time sharing use.**
*** The Datapoint 3300 is engineered to be *fully compatible* with all time sharing services now using Teletype equipment as terminals.**

In developing the Datapoint 3300, Computer Terminal Corporation sought a terminal that would amplify the productivity of the professional as he worked upon problem solutions in interactive dialogue with a computer. We sought to remove the traditional barriers to effective man/machine communications. We succeeded.

A central feature of the 3300 is the CRT display capacity of 1800 characters in a 25 line/72-character-a-line format. (A high "refresh" rate provides characters that are at once stable and easy to read.) In this expanse of data, a complex program or problem can easily be expressed, and comprehended at a glance. The interactive user, working the standard 64-character-set keyboard, can easily add, delete, correct or manipulate characters and lines of data. The remote computer becomes a powerful and flexible extension of the human thought process, directly responsive to and controlled by the user sitting at the Datapoint 3300.

Because the 3300 is not shackled by the limitations of a mechanical printer, it can make available data transmission rates of up to 600 bits per second standard, and up to 4800 bps with optional speed buffer. This means the interactive user enjoys faster response from his remote computer; accordingly, his "on-line" time will shrink while his productivity goes up.

The 3300 is noiseless — no hum or clatter of keys to intrude upon the user's concentration. It comes packaged in a handsome, totally self-contained unit, comparable in size to an executive typewriter, which blends well with today's office environment. The female help will love the 3300's appearance, as well as its ease of usage.

We think you'll like it. For further information, simply write to Computer Terminal Corporation, P. O. Box 6967, San Antonio, Texas 78209.

Computer Terminal Corporation

CIRCLE 23 ON INQUIRY CARD

by-phone, which provides customers with facsimile service via the public telephone network.

For additional information or a descriptive brochure, contact the publisher: Auerbach Info, Inc., 121 North Broad St., Philadelphia, Pa. 19107.

COMPUTING SERVICES OFFERED NATIONALLY — A joint marketing agreement has been reached between the Chi Corp., of Cleveland, Ohio, a scientific/engineering computer services company, and Stat:Com—the Statistical Communications division of Statistical Tabulating Corp. (STC), of Chicago, Ill., a firm specializing in commercial data processing services. Stat:Com will market the specialized capability of Chi Corp.'s Univac 1108 through STC's national sales organization, providing scientific and engineering computing services nationally.

According to Stanley Y. Curry, president of Chi, and Michael R. Notaro, STC president, the agreement represents "a blending of skills between the oldest scientific/engineering computing organization and a company with 33 years' data processing experience. The third generation 1108 computer and Chi's excellent staff will provide STC with a logical extension of its services into the area of complex computing, while our established national sales structure and network of data centers will allow Chi to greatly broaden the marketing of their computer time."

COMPUTERS AND COMMUNICATIONS CONFERENCE—The IEEE Mohawk Valley Section and the Communications Technology and Computer Group Chapters will sponsor a conference entitled "Computers and Communications," at the Beeches in Rome, N. Y., September 30 to October 2.

The conference will review recent communications/computer processing developments, taking advantage of computer techniques which may be applicable to problems confronting research and operations personnel in the communications area. The conference will also consider the role of communications techniques in computer systems development. Application and implementation will be emphasized, rather than just theoretical aspects. For further information contact: Computers and Communications Conference, 304 East Chestnut St., Rome, N. Y., 13440.

VRC TO EXPAND FACILITIES—Vermont Research Corp. of No. Springfield, Vt., has announced plans to establish a separate Systems Division in Tempe, Arizona. Headed by Prentiss L. Smith, vice president and founder, the division will produce standard and custom memory systems.

Standard products will include controllers for interfacing standard VRC drum and disk memories to a variety of computers, and off-the-shelf memory/interface packages for any data processing systems requiring peripheral memory. The company has already marketed standard memory systems for the PDP-8, 8/S, and 9; and the Sigma 2, 5, and 7.

"Establishment of a separate systems facility in the west," Smith says, "is a continuation of our rapid growth in Springfield, where increased drum orders have tripled our production capacity since the first of the year. The continued sales growth for drums *and* systems requires expansion of our systems capabilities."

1969 ISA CONFERENCE & EXHIBIT—The Instrument Society of America will conduct three symposia concurrently with the 24th Annual ISA Instrumentation-Automation Conference and Exhibit, October 27 to 30 at the Astrohall in Houston, Texas. Themes of the symposia are data handling and computation, test measurement, metrology.

Registration fees for all technical sessions, including exhibit admission is $12 for ISA members and $18 for non-members. The fee for the exhibit only is $3 for non-members, with no charge to ISA members, or non-members registered by October 3. Registration forms may be obtained from: Public Relations Dept., Instrument Society of America, 530 William Penn Place, Pittsburgh, Pa. 15219.

DIGITAL EQUIPMENT CORP. FORMS CONTROL PRODUCTS GROUP—The creation of a Control Products Group has been announced by Stanley C. Olsen, vice president and group manager of the Digital Equipment Corp. of Maynard, Mass.

Olsen states that "penetration of sophisticated electronic technology into the industrial control market has advanced to the point where specific approaches are becoming well defined. Having followed this penetration for the ten years that DEC has been supplying this market, we are confident that our new approach will allow us to dedicate our resources most effectively to developing products and innovative techniques to meet specific demands."

The product lines will include solid state machine control for repetitive processes—PDP-14—with John Holzer as manager; systems for numerically controlled machinery—n/c products, Russell Doane, manager; control modules for industrial applications—module products, with Frederick Gould as manager; and specialized industrial control systems, drawing on all product areas within DEC, to be managed by Martin S. Gordon. Product line manager is Allan T. Devault, who will be responsible for overall activities within the control products group.

COMPUTER SHORT COURSES SET AT UCLA—Three short courses in the computer sciences will be offered by UCLA Extension's department of engineering and physical sciences in July and August on the UCLA campus. All courses meet Mondays through Fridays, 8:30 a.m. to 5 p.m.

Planners and managers of operational systems whose performance depends strongly on computers will be interested in *Systems Analysis Techniques for Computer-Based Systems,* July 21 through 24, in Room 5436 Boelter Hall. The course will provide a survey of techniques for predicting, measuring and analyzing the performance of computers in an operational environment, of general concepts of systems analysis and of approaches to critical computer problems.

Error Detecting and Correcting Codes: Applications in Digital System Design will be offered, July 28 through August 2 in Room 4277 Boelter Hall. For engineers and scientists with training and/or experience in digital equipment design, the course will constitute a concentrated and self-contained study of current applications of error detecting and correcting codes in the design of digital systems.

Development of Real-Time Computer Systems will conclude the series, August 4 through 15 in Room 5436 Boelter Hall. The course will provide a greater understanding of real-time systems with emphasis on concepts and comparisons; techniques of designing and implementing real-time systems; applications; and computers and society.

Further information is available by writing P.O. Box 24902, Engineering and Physical Sciences Extension, 6115 Math Sciences Building, University of California, Los Angeles, Calif. 90024, or telephone (213) 825-3344 or 825-1295.

Dale Mrazek
National Semiconductor

MOS BRIEF 7

TTL/MOS/DTL INTERFACES

Some of our low-voltage MOS integrated circuits couple directly to TTL or DTL logic circuits, some take a resistor or two. Voltage translators and special buffers are not needed because the data-input stages are designed to accept relatively small changes in signal voltages as well as large MOS-style swings.

Interfaces like Figures 1a and 1b do nicely in most applications. Devices with active pullup and pulldown output stages don't even need a current-sinking resistor (Figure 1b). An input pullup resistor can be used on the shift registers (MM506, MM510 and their cousins) in high-performance applications. We've clocked them at twice the normal MOS rate with the Figure 1c interface.

A pullup resistor is required by some of our larger-scale devices, particularly those containing a lot of logic and memory on the same chip. The MM521 read-only memory in Figure 1d is one of these. But considering that the MM521 stores 256 4-bit words and can replace an entire TTL assembly, we think that a few resistors is a small price to pay.

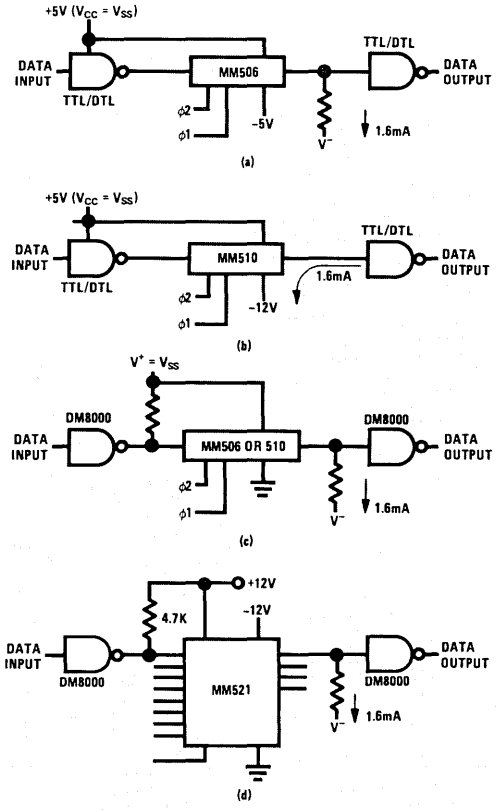


FIGURE 1. Typical TTL/MOS or DTL/MOS Interfaces.

What makes our MOS circuits so compatible? Design improvements based on better MOS processes, of course. The National Semiconductor process lowers the voltage threshold to about 2V, allowing small transitions in the data signals to be handled reliably. TTL and DTL transitions are usually 4V or less, while conventional MOS circuits demand a change of at least 7V. Some look for transitions as great as 18V.

Note, however, that the biases on the shift registers in Figure 1 are positive and negative, a la regular MOS. Although low-voltage elements are used in the input stages, they are designed with ample overdrive to establish proper MOS logic levels for the following stages' storage and switching elements. In fact, any number of our low-voltage MOS circuits can be placed in cascade between two TTL or DTL gates as long as MOS/MOS coupling specifications are met within the string.

You can usually disregard what has been the normal limits on our MOS inputs. Data levels can be as low as V_{SS}–2.5V for an MOS "0" bit and V_{SS} –4.2V for a "1". If V_{SS}, the MOS substrate voltage, is picked off the +5V supply used for TTL V_{CC}, logic levels of 2.5 and 0.4V are acceptable to low-voltage MOS inputs. They'll work even during worst-case V_{CC} ±5% and gate-loading conditions with an input resistor to V_{CC}.

At the output interface, different conditions must be satisfied (they can be calculated with the equations in Table 1). To drive a TTL gate, the MOS output stage must sink 1.6 mA of current and allow the signals to go more positive than +2.4V and more negative than +0.4V. Some designs require an external resistor to provide the negative current path, but devices with output stages like the MM510 do not. The latter design has proven itself in numerous applications, so we are using it in all appropriate new products. Either one meets the voltage spec.

Fanout is normally one, but this can often be improved by trade-offs between V_{SS} and V^-. The voltage transitions for the clock signals (ϕ_1 and ϕ_2) will have the same amplitude as specified for our MOS assemblies, but the levels should be shifted to correspond to V_{SS}. During the logic "0" clock intervals, the clock should be within 1.5V of V_{SS}.

When V_{SS} is the same as V_{CC}, it doesn't make much difference what types of TTL or DTL gates are used as signal sources and receivers. But be sure the gate can withstand its output being pulled up if V_{SS} is higher. That's why we recommend our DM8000 gates in Figures 1c and 1d. Even though its specifications read like a conventional TTL gate's, the DM8000 can be pulled as high as +14V without breakdown (a similar quad 2-input gate circuit, the DM8810, is specified for high breakdown voltages). The DM8000 is protected by a reverse-biased diode in the emitter-follower active-pullup string and a base-to-emitter resistor biases off the output-sinking transistor (see Figure 2). Also, the DM8000 has no trouble sinking the current required for an MOS input at the +0.4V level. It can handle 16 mA.

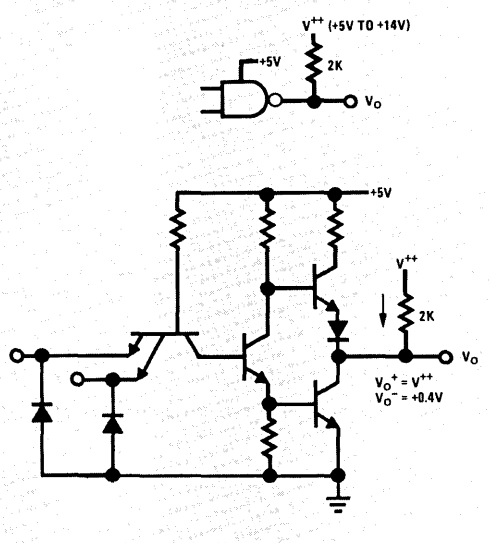


FIGURE 2. DM8000 Output Pullup Technique.

Another handy feature of these DTL or TTL/MOS/TTL interfaces is that there are no logic inversions through the interfaces. Of course, the MOS stages in an application like Figure 3 see each

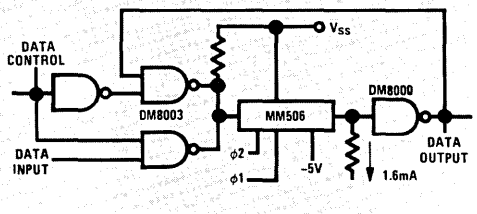


FIGURE 3. Recirculating MOS Delay Line with TTL or DTL Control.

TTL "1" bit as an "0" and vice-versa. But that's of no concern to the rest of the system. Nor need it bother the logician. Furthermore, when there are several MOS circuits between interfaces, TTL data can be taken off the MOS signal connections providing the loads do not severely degrade the MOS logic levels. Don't try this with conventional MOS, though.

Both the 5V and 12V techniques shown reduce interfacing costs to a minimum. Inserting MOS devices into an otherwise TTL or DTL system can lower the cost per bit significantly when the application calls for shift registers, small memories and similar functions. Both methods are equally convenient, since neither requires an additional power-supply connection. Most systems contain 5V and 12V supplies for other purposes. So the choice depends on the voltages that are most compatible with the rest of the system and performance factors such as the operating frequency desired.

Detailed information on low-voltage MOS devices and instructions on clocking and other auxiliary circuits can be found in National Semiconductor literature.

Table 1. Output Conditions

In MOS logic "0" state:

$$\frac{V_{SS} - 2.4V}{Z_o} \geq \frac{2.4V - V^-}{R_o}$$

In MOS logic "1" state:

$$I_1 \leq \frac{0.4V - V^-}{R_o}$$

Definitions:

I_1 = Current through R_o at V_o = +0.4V (1.6 mA)
R_o = Output resistor (internal or external)
Z_o = MOS output impedance
V^- = Supply sinking negative current
V_{SS} = Most positive voltage
V_{DD} = MOS drain voltage

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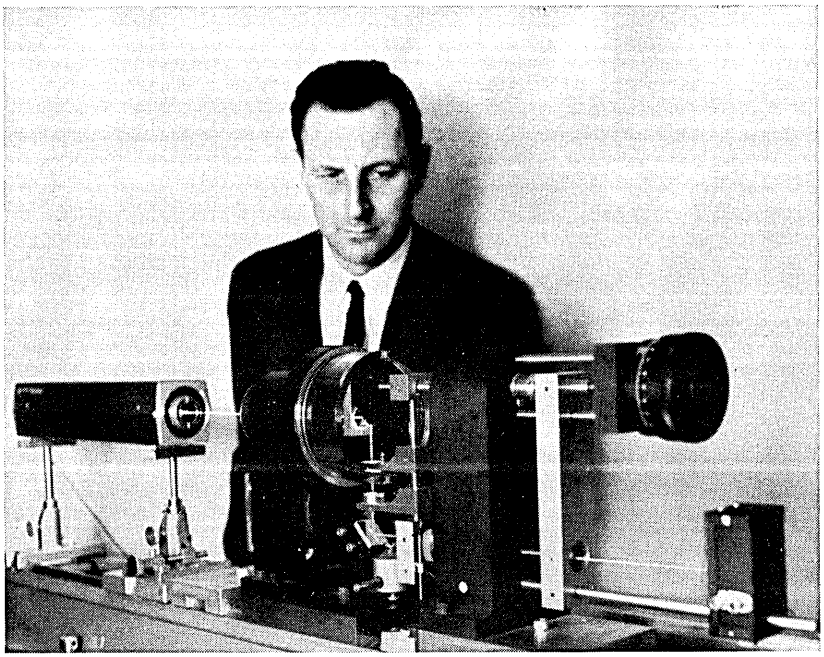
5-69 PRINTED IN U.S.A.

DEVELOPMENTS

Holographic Techniques Point Way To Improved Computer Memories

An experimental computer storage device has been developed by IBM's Systems Development Laboratory in San Jose, Calif., which has attained a storage density of over 2 million bits per square inch of recording space, an average data read rate of 16 Megabits per second and an average access time of 8.5 milliseconds. Tests indicate as feasible a storage density of 6 Megabits per square inch, a data read rate of 160 Megabits/sec and an access time of 1.3 milliseconds. The device uses advance holographic encoding techniques to work with units of one byte of data. An electron beam is employed to write computer-generated binary Fourier holograms on strips of photographic film. Each hologram contains one byte of data, made up of eight data bits and one clock bit. The holograms are organized into 256 tracks of each film strip, and the strips are placed on the inside surface of a transparent drum for readout by a laser beam. The device successfully reads holograms when up to 30% of their area is obscured.



The laser beam above is reading out information from the storage drum of an experimental memory device that has the potential for storing the equivalent of 150,000 English words on a surface smaller than a half dollar. The storage device uses byte-oriented holograms recorded on strips of photographic film as a storage medium. The film is placed on the inside surface of the rotating drum at the center of the photo. When the beam leaves the helium-neon laser source at the left, its path is guided by a light deflector system. After being deflected at the drum's axis to pass downward through the holograms, the beam is deflected again and detected by an array of photodiodes contained in the box at the right.

IBM Develops 32-Channel Multiplexer on Single Chip

A 32-channel multiplexer with 40 analog switching devices on a single LSI MOS chip has been developed by IBM.

The new component, replacing a previously developed 16-channel multiplexer, has circuits for multiplexing, timing logic and two shift registers requiring an external clock and power supplies. The total power requirement is reduced from 250 to about 120 milliwatts, total multiplexer size and weight are reduced, and reliability is greatly improved.

Prior to the 16-channel multiplexer, transistors, relays or switches were used. These, however, were bulky and not reliable for space applications.

For systems applications larger than 32 channels, the chip can be interconnected to form a 64-channel or larger multiplexer in multiples of 32 or in a multiplexer- submultiplexer configuration.

In its present configuration, the chip functions only as a serial multiplexer. However, it was designed to allow modification of masks to produce a random access multiplexer.

The analog switching devices are laid out in the shape of a horseshoe around the outside of the chip. Shift registers and associated logic are contained in the center. By modifying the center section, a holding register can be added to produce a random access capability. Chip design is such that a random access multiplexer could be produced with a minimum of mask modification.

The circuit and chip were developed jointly by IBM's Federal Systems division's Space Systems Center facility in Huntsville, Ala., and the Components division's East Fishkill, N.Y. facility.

The chip is expected to be used in advanced aerospace and avionics systems requiring high reliability with minimum weight, size, and power dissipation.

DEVELOPMENTS

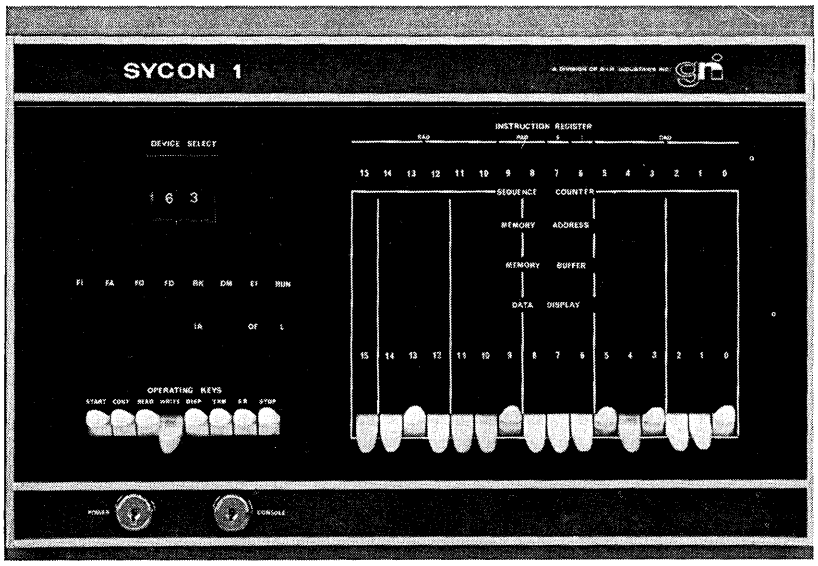
Functionally-Oriented Computer for Process Control

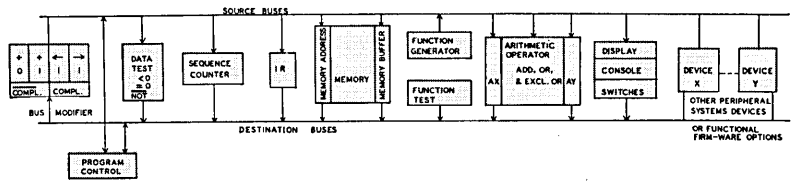
A direct function processor has been developed for the process and numerical control market which can be programmed in the same kind of functional language the system designer must use to define his own overall system requirements. Recently revealed by GR Industries Inc. of Newton, Mass., the GR-909 is a functionally-oriented computer in which every processor or I/O element is directly addressable as if it were part of the internal processor logic. The source and destination buses are not terminated at the computer I/O terminals. Instead, all internal operations are handled by functionally-designed elements connected between the same set of buses as are external devices, so that all internal and external elements are directly addressable using a compiler-like functional language rather than a mathematically-oriented language.

Passage between the source and destination buses is linked by a modifier which can manipulate the data enroute under program control. Thus the bus system is extended into the computer itself; i.e. the elements of the computer are brought outside of the central processor and all elements, such as the instruction register and arithmetic unit are connected across the bus structure.

The key to making this type of structure effective is the addition of a programmable link between the source and destination buses. This programmable path provides a means of getting any data word or control pulses from any of the internal components of the computer appearing on the destination buses back to the source buses to be delivered to any other functional component in the system. Since each active component in the entire system is connected between the buses, any device can send a word in parallel directly to any other device. The memory of the GR-909 is random access core in 1024 and 4096 plug-in modules, which can be expanded to 8K in the basic processor frame without additional wiring. The basic unit has a capacity of 16 bits, and can be expanded to 32K directly addressable words.

GR-909 is now in prototype production and deliveries are expected to be made in the fall. The basic machine will sell for $3,600. The 4K machine with a Teletype interface (not including Teletype unit) will sell for $8,400.





The GRI 909 computer, designed specifically for the OEM control market, utilizes a unique concept that short-circuits the conventional I/O buses and enables the arithmetic operator, sequence counter, various registers, memory elements, and other operators usually found in the central processor unit (CPU) to be directly connected to the same set of buses as the computer peripheral equipment and the devices used in the customers' systems.

NEW PRODUCT NO. 77

μA715 HIGH-SPEED OP AMP

The new Fairchild μA715 is the fastest linear IC op amp available today.

For applications where power bandwidth, acquisition time or slew rate is the prime consideration, the μA715 stands alone. It's ideal for applications such as wide-band amplifiers, high-speed integrators, precision comparators, sample-and-holds and video or deflection amplifiers. You can start raising the performance of your data acquisition, control, communications or display systems today.

The μA715 is a 3-stage amplifier, with a Darlington cascode input for optimized ac and dc performance, a differential second stage and a class AB output for low distortion. Bandwidth is 60MHz, open loop gain is 92dB, input offset current is only 80nA and both input and output are short-circuit protected.

And, even though op amps are available with slew rates higher than the μA715's 60V/μs ($A_v = 100$), it's *still* the fastest op amp available. The curve shown represents the typical response of any op amp to a step input at time T_o. First, there's a short delay, then the output starts rising to its final value at a rate determined by the slew rate ($\Delta V/\Delta T$). But, in most op amps made, there is first an overshoot, then ringing. The final output value is not achieved until the end of the settling time, when the excursions no longer exceed the bounds of the error band. The total time to achieve the final value (acquisition time) is the sum of the first delay, the rise time and the settling time. In most other op amps, the settling time is measured in microseconds. In the μA715, the settling time is just 300ns. Combine this with a maximum initial rise time plus delay of 350ns (for a 10V swing) and you've got a total acquisition time of just 650ns. And the fastest op amp made.

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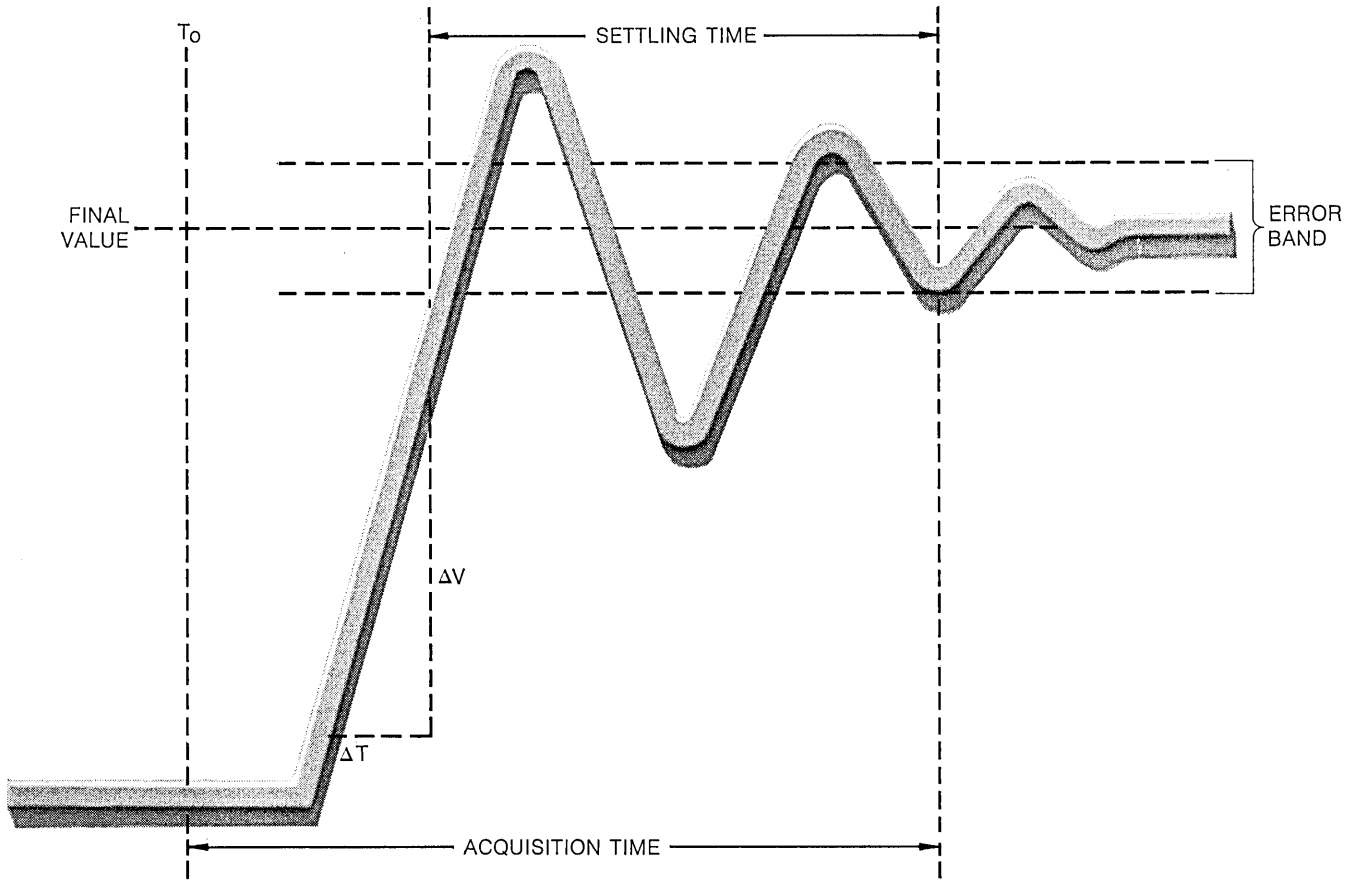
To order the μA715, ask for:

Part No.	Package	Temperature Range	Price
U5F7715312	TO-5	−55°C to +125°C	$48.00
U5F7715393	TO-5	0°C to + 70°C	15.00



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CIRCLE 25 ON INQUIRY CARD

Optically Exciting a Magnetic Memory: A Feasibility Study

A study has been made to determine the feasibility of modifying the magnetic moment of a magnetically-ordered material by optical pumping for digital memory application.

The potential of optically addressed (often referred to as beam addressable) digital memories has been considered by a number of workers and is presently an area of much research. The goal to which these efforts are directed is the achievement of high-density bulk memory with storage capacity of approximately 10^8 bits. This density can be achieved in reasonable size, for example a planar area of 10 x 10 cm, with bit resolution of 10 microns. Such a bit size is about an order of magnitude larger than diffraction-limited resolution of visible light. Thus optical approaches appear attractive. Additionally, the interaction of polarized light with magnetic materials exhibiting the magneto-Kerr and Faraday effects supplies a means for detecting the magnetization state of local region via reflection or transmission providing communication with the "store" without interconnecting wires.

The limiting operation, however, in all presently proposed memory schemes is the write process. This has generally been accomplished by applying heat to the lattice, to effect a change in coercivity of a local spot. The heat source may be a laser or electron beam; both have been proposed and experimentally studied. The use of temperature changes to modify the magnetic state of a memory medium introduces speed performance limitations. In addition to the relatively long thermal time constants, another problem associated with thermal excitation is that of thermal creep. To prevent adjacent bit disturbing effects thermal barriers must be provided between storage element locations, resulting in a reduction of achievable storage density and an increase in the fabrication process complexity. To overcome these limitations associated with thermal excitation, the study sought to determine the feasibility of optically pumping a magnetic material to effect the switching process. This approach provides the potential of achieving excitation and decay times in the submicrosecond range without the problem associated with thermal creep. The experimental work to date has been directed toward the rare earth iron garnets. These materials show a rapid change in coercive force versus temperature at the antiferromagnetic compensation temperature, an effect from slight variations in temperature causing a net magnetic moment to exist. A technique is therefore being sought for holding the lattice temperature constant while the magnetic moment is changed by optical excitation.

It is apparent from the study to date that the gadolinium iron garnet crystals grown by the present molten flux technique will not exhibit the desired characteristics. The conduction band causing the large competing absorption is probably a characteristic of the iron-oxygen combination rather than impurity-induced interband gap levels. As such, the rare earth garnets are all limited by this absorption edge. Only terbium and dysprosium offer a possibility of pumping at energies below the conduction band edge. Antiferromagnets overcome the problem of lattice phonons creating uncompensation, but little is known of the optical properties of the potentially useful materials.

The concept of uncompensating an antiferromagnetically - ordered system is of significant interest both theoretically and practically. The significance of achieving 10^8-bit high-speed random access computer memories with passive element reliability should not be understated. Optical pumping is considered a powerful approach towards achieving that goal.

Patent status:

No patent action is contemplated by NASA. Source: F. L. Grismore and J. E. Rhodes of the Georgia Institute of Technology under contract to Marshall Space Flight Center (MFS-14854).

For $11,950.10, you get MAC, 4 priority interrupts and a cup of coffee.

Why coffee? Because you won't be spending any time programming MAC for priority interrupts—since MAC's interrupts (with automatic store and restore) are in hardware, not software. So you've got to have something to do with your time.

And MAC's internal structure saves you still more time by reducing programming.

On the job, the time saving goes on. MAC responds to interrupts in an average 6 microseconds. Which means it can operate with nearly any real-time or time-sharing system.

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Nothing mentioned here is exclusive with MAC, of course. Other computers offer 4 hardware priority interrupts and most of MAC's other features. They start at around $25,000.

But if you're spending money like that to get a computer like MAC, you may need a strong cup of coffee.

Write to MAC, Lockheed Electronics Company, Data Products Division, 6201 East Randolph Street, Los Angeles, Calif. 90022.

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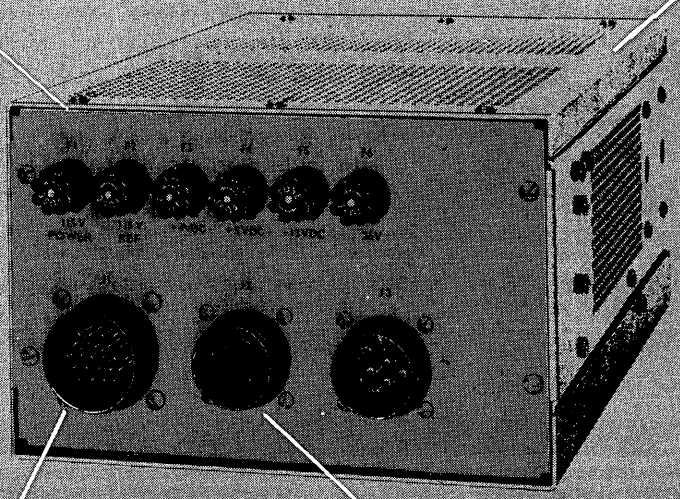

Accepts strobed parallel binary-angle digital input data, with 9 to 13-bit resolution.

Converts to resolver or synchro output with 6 arc-minute accuracy.

North Atlantic Model 538/30 Digital-to-Resolver/Synchro Converter is designed to be integrated into GSE, ATE or aircraft simulators without using front-panel rack space. Optional features and other models to fit specific requirements are available.

This high-accuracy converter is another elegant example of North Atlantic's creativity in automatic test equipment, resolver/synchro instrumentation, and computer interface equipment.

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CIRCLE 27 ON INQUIRY CARD

In addition to demonstrating two techniques for deriving all possible 4-bit BCD weighted codes, this article illustrates the derivation of all 3-digit trinary coded decimal (TCD) codes and explains the relationship between trinary and negatrinary codes

A New Approach to Weighted Number Systems

Monty Walker

Singer Company
Instrumentation Div.
Los Angeles, Calif.

"Weighted Number" is one of the most familiar concepts of the logical designer. The "idea" of weight is a universal concept and is intermeshed in all areas of mathematics. Considering that centuries have been spent investigating the properties of such systems, it would seem pretentious to attempt to modify these concepts. There are, however, several developments that make the attempt worth while: (1) a new interest in non-standard arithmetic systems such as residue arithmetic[1], and (2) new fundamental discoveries such as negative radix arithmetic[2] and the Hartman conversion technique[3].

In this article a more generalized formulation of "weight" will be developed as well as possible applications of the expanded concepts.

CONVENTIONAL WEIGHTED NUMBER SYSTEM

The general form of a conventional weighted number is: $a_n r^n + a_{n-1} r^{n-1} + \ldots + a_0 r^0$, where r is the radix or base of the system and each a_i may have any integral value from 0 to r−1. In the familiar decimal system, r will have the value of 10 and each "a" will be 0,1, . . ., or 9. The decimal number 324 is equivalent to: $3(10^2) + 2(10^1) + 4(10^0)$. In the binary system, r is 2 and each "a" will be either 0 or 1. The binary number 1101 is equivalent to: $1(2^3) + 1(2^2) + 0(2^1) + 1(2^0) = 13$.

Monty Walker recently joined Singer Instrumentation as a project engineer. His duties include the design of specialized digital instruments. Prior to joining Singer, he worked for Litton Data Systems as a logic designer for advanced digital systems. Mr. Walker has written many articles relating to digital theory and design, including "Designing with Binary Decision Trees," (Computer Design, August 1967).

Binary Coded Decimal

To represent a decimal number using binary elements, at least four elements in combination must be used. Of course four binary elements in combination have a maximum of 16 different states, but in representing decimal numbers, only 10 states will actually be used. The remaining 6 will be constrained. This method of using binary elements to represent decimal numbers is called binary coded decimal or BCD.

BCD Codes

Any set of ten binary states can be used to form a BCD code. The total number of four element BCD codes is in excess of 29 billion.* Many of these codes are merely reflections of others, but if reflections are not included, the number is still in excess of one billion.**

$$* \frac{161}{61} = 29{,}059{,}430{,}400 \quad ** \frac{161}{41\ 61} = 1{,}210{,}809{,}600$$

A relatively small number of possible BCD codes have the characteristic of weight; that is, each decimal digit can be formed by adding the "assigned" binary element values (weights). In Figure 1 the 8421, 5211, 8-643 and excess-3 codes are illustrated. Each "1" has the column value and each "0" has the value of zero. The excess-3 code is considered non-weighted. It will be demonstrated later that in a sense it is also weighted.

The total number of four bit weighted BCD codes has been analyzed by several authors[4,5]. There are exactly 17 positive weighted codes, 54 single negative

excess −3

8	4	2	1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

(a)

5	2	1	1	
0	0	0	0	0
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
1	1	1	1	9

(b)

8	−6	4	3	
0	0	0	0	0
0	1	1	1	1
1	1	0	0	2
0	0	0	1	3
0	0	1	0	4
1	1	0	1	5
1	1	1	0	6
0	0	1	1	7
1	0	0	0	8
1	1	1	1	9

(c)

x3	x2	x1	x0	
0	0	1	1	0
0	1	0	0	1
0	1	0	1	2
0	1	1	0	3
0	1	1	1	4
1	0	0	0	5
1	0	0	1	6
1	0	1	0	7
1	0	1	1	8
1	1	0	0	9

(d)

Fig. 1 BCD Codes

	subcodes
3 3 2 1	18
4 2 2 1	32
4 3 1 1	18
4 3 2 1	32
4 3 2 −1	32
4 4 2 1	8
4 4 2 −1	8
4 4 −2 1	8
4 4 3 −2	8
5 2 1 1	32
5 2 2 1	16
5 2 2 −1	16
5 3 1 1	16
5 3 1 −1	32
5 3 2 1	16
5 3 2 −1	16
5 3 −2 1	16
5 4 2 1	8
5 4 2 −1	8
5 4 −2 1	8
5 4 −2 −1	8

	subcodes
5 4 3 −2	8
5 4 −3 2	8
5 4 3 −3	16
6 2 2 1	8
6 2 2 −1	8
6 2 −2 1	16
6 3 1 1	4
6 3 1 −1	16
6 3 −1 −1	8
6 3 2 1	8
6 3 2 −1	8
6 3 −2 1	8
6 −3 2 1	8
6 3 −2 −1	8
6 3 2 −2	16
6 4 2 1	4
6 4 2 −1	4
6 4 −2 1	4
6 −4 2 1	4
6 4 −2 −1	4
6 4 3 −2	4
6 4 −3 2	4
6 −4 3 2	4

	subcodes
6 5 −3 1	4
6 4 −4 2	4
6 5 4 −3	2
6 5 −4 3	2
6 −5 4 3	2
−6 5 4 3	2
7 3 2 1	2
7 3 2 −1	4
7 3 −2 1	4
7 −3 2 1	4
7 3 −2 −1	4
7 −3 2 −1	2
7 4 2 1	2
7 4 2 −1	2
7 4 −2 1	2
7 −4 2 1	2
7 4 −2 −1	2
7 −4 2 −1	2
7 5 −3 1	2
7 5 −3 −1	2
7 5 −4 1	4
7 6 −5 3	1
7 −6 5 3	1
−7 6 5 3	1

	subcodes
8 4 2 1	1
8 4 2 −1	1
8 4 −2 1	1
8 −4 2 1	1
8 4 −2 −1	1
8 −4 2 −1	1
8 −4 −2 1	1
8 4 3 −2	1
8 4 −3 2	1
8 −4 3 2	1
8 4 −3 −2	1
8 −4 3 −2	1
8 5 −4 2	1
8 −5 4 2	1
8 5 −4 −2	1
8 6 −4 1	1
8 −6 4 1	1
8 6 −4 −1	1
8 −6 4 3	1
8 7 −4 −2	1

Fig. 2 Weighted BCD 4-bit Codes

codes, and 17 double negative codes, making 88 in all. In most of these codes, at least one decimal number can be formed in more than one way. Taking these alternates into account, there are 615 sub-codes. Figure 2 lists the basic codes with the number of sub-codes for each.

DERIVATION OF THE BASIC CODES

The derivation of four bit codes is an interesting exercise in combinational mathematics[6]. The procedure is to find all sets of four integers (positive or negative) that can combine by addition to form the positive decimal integers 0 through 9.

Although there are a limitless number of four digit sets, by using common sense and combinational analysis the number of sets to be tested can be reduced to a few hundred. To demonstrate the technique, some typical theorems will be illustrated.

Theorem 1: At least one weight must be odd.

Proof: If all weights are even it is not possible to obtain odd decimal digits by the rule of combination.

Theorem 2: The sum of all the positive weights must be ≥ 9.

Proof: The maximum number that can be obtained by the rule of combination is the sum of the positive weights. If this sum is less than 9, then it is not possible to obtain decimal 9.

Theorem 3: At least two weights must be positive.

Proof: Assume a set of four weights, three being negative; i.e. A, -B, -C, -D. The positive combinations are:

(1) 0	(4) A-C	(7) A-B-D
(2) A	(5) A-D	(8) A-C-D
(3) A-B	(6) A-B-C	(9) A-B-C-D

Since there is a maximum of 9 distinct combinations, it is not possible to obtain 10 decimal numbers.

Several less obvious theorems are listed for the interested reader to prove.

(4) All weights must ≤ 8.

(5) A maximum of two weights can have the same absolute value.

(6) In positive codes the sum of the weights must be ≤ 15.

With the above theorems in mind, a table of integer sets can be made and tested for code validity. There will, of course, be only 88 valid codes in the table and we have absolute assurance that no others exist.

Surprisingly enough, it was not until 1960 when G.P. Weeg[5] used the above techniques to uncover all 88 codes.*

In the next section it will be shown that in one sense there are actually fewer codes than indicated, and in another sense, an infinite number.

A NEW LOOK AT WEIGHT

A characteristic of all weighted numbers is that they have not one, but two values. True, one of the values is zero, but zero is a number and cannot be considered non-existent. The 8421 code is more properly a (8 or 0, 4 or 0, 2 or 0, 1 or 0) code.

To coordinate the material to come, a new notation will now be introduced, $\frac{A}{B}$ In this notation, "A" represents the True or 1 value for a weight and "B" represents the False or 0 value for a weight. The 8421 code can be expressed as $\frac{8}{0}\frac{4}{0}\frac{2}{0}\frac{1}{0}$. By using this method of exhibiting both weights of a weighted code digit, certain rather interesting features can be proved.

Consider the weighted bits $\frac{A}{B}\frac{C}{D}$. As shown in Figure 3, the readout is: If a constant k is added to both the "A" and "B" weights of $\frac{A}{B}$, the new readout will be:

It can be seen in Figure 4 that the code is "shifted" k bits. As an illustration of the above, consider the two bit code $\frac{2}{0}\frac{1}{0}$. The normal readout is 0 through 3. If 4 is "added" to the $\frac{2}{0}$-bit, the new code $\frac{6}{4}\frac{1}{0}$ will have a readout of 4 through 7. This method of adding a constant to both the A and B weights will be called code addition.

It is obvious that the above technique can be extended to any number of weights. It must also follow that if k is code added to one weight and -k is code added to another weight, the read-out will be unchanged. Note that k can have any value; positive, negative, or even non-integral values.

Example: consider the $\frac{8}{0}\frac{4}{0}\frac{2}{0}\frac{1}{0}$ code. If a constant is added to one bit and subtracted from another, the code remains unchanged. To demonstrate this we can arbitrarily add 3 to the $\frac{8}{0}$-bit and subtract 3 from the $\frac{4}{0}$-bit. The resultant code is shown in Figure 5.

Note that the binary representation is unchanged although the weights of the first two digits have been changed. In column A, a "1" has weight 11 and "0" has weight 3, rather than 8 or 0. The implication is, that in a sense, there are an infinite number of weighted codes. Note also that each element is still binary in nature. The characteristic difference is that the "false" weight is not necessarily zero.

GENERATING NEGATIVE CODES

Consider the $\frac{8}{0}\frac{4}{0}\frac{2}{0}\frac{1}{0}$ code. By taking all possible combinations, it is possible to generate an unbroken sequence from 0 through 15. If a constant k is code subtracted from one of the weights, the sequence will be shifted k bits in the negative direction.

In Figure 6a, the basic $\frac{8}{0}\frac{4}{0}\frac{2}{0}\frac{1}{0}$ code is shown—the sequence range is 0 through 15. In 6b, 1 is code subtracted from the $\frac{1}{0}$ weight transforming it into $\frac{0}{-1}$. The sequence range is -1 through 14. In 6c, 4 is code subtracted from the $\frac{4}{0}$ weight and 2 is code subtracted from the $\frac{1}{0}$ weight transforming them into

Fewer theorems and a computer were used to generate and test a table of 13,122 entries

A/B	C/B	
0	0	B+D
0	1	B+C
1	0	A+D
1	1	A+C

Fig. 3 Readout of weighted bits A/B, C/D

A+K/B+K	C/D	
0	0	B+D + k
0	1	B+C + k
1	0	A+D + k
1	1	A+C + k

Fig. 4 Readout of weighted bits with constant k added

A 11/3	B 1/−3	C 2/0	D 1/0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Fig. 5 Addition and subtraction of constant

$\frac{0}{-4}$ and $\frac{0}{-1}$. The sequence range is −5 through 10. In 6d, 5 is code subtracted from the $\frac{8}{0}$ weight transforming it into $\frac{3}{-5}$. The sequence range is −5 through 10 as in 6c.

Comparing 6c with 6d, it can be seen that each decimal digit has the same binary code although the column weights are different. Again it is apparent that there are an infinite number of possible weighings for a given code.

Consider a code such as the $\frac{8\,4\,2\,1}{0\,0\,0\,0}$ being transformed so that each digit will have a "0" for either the True or False position. If the weights with a "0" in the True position are now inverted, the new code will be a standard negative weighted code. If the negative constant has not shifted the code below the maximum for decimal 9, the code will be one of those listed in Figure 2.

EXCESS-3 CODE

The excess-3 BCD code uses the middle 10 of the first 16 binary numbers for the decimal readout. From this it must follow that if the excess-3 is weighted, one or more of the weights must be negative.

Consider the $\frac{8\,4\,2\,1}{0\,0\,0\,0}$ code transformed into the $\frac{8\,4\,0\,0}{0\,0\text{-}2\text{-}1}$. In Figure 7, range r is the conventional excess-3 BCD code. The code is interesting as both the A and B columns are negative weighted *but* from the False side of the weight. By inverting the A and B columns, the new weighing becomes the conventional $\frac{8\,4\text{-}2\text{-}1}{0\,0\,0\,0}$ code as listed in Figure 2.

8/0	4/0	2/0	1/0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

(a)

8/0	4/0	2/0	0/−1	
0	0	0	0	−1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	2
0	1	0	0	3
0	1	0	1	4
0	1	1	0	5
0	1	1	1	6
1	0	0	0	7
1	0	0	1	8
1	0	1	0	9
1	0	1	1	10
1	1	0	0	11
1	1	0	1	12
1	1	1	0	13
1	1	1	1	14

(b)

8/0−4	0/0−1	2/0	0/−1	
0	0	0	0	−5
0	0	0	1	−4
0	0	1	0	−3
0	0	1	1	−2
0	1	0	0	−1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	2
1	0	0	0	3
1	0	0	1	4
1	0	1	0	5
1	0	1	1	6
1	1	0	0	7
1	1	0	1	8
1	1	1	0	9
1	1	1	1	10

(c)

3/−5	4/0	2/0	1/0	
0	0	0	0	−5
0	0	0	1	−4
0	0	1	0	−3
0	0	1	1	−2
0	1	0	0	−1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	2
1	0	0	0	3
1	0	0	1	4
1	0	1	0	5
1	0	1	1	6
1	1	0	0	7
1	1	0	1	8
1	1	1	0	9
1	1	1	1	10

(d)

Fig. 6 Alternate codes from the same sequence

Because the excess-3 is really a weighted code,[7] it is possible to design an excess-3 weighted ladder using conventional techniques.[8] In many instruments where digital to analog conversion is performed, the excess-3 is first encoded into the 8421. Figure 8 shows a three decade excess-3 ladder using conventional design techniques. Those familiar with ladder geometries will recognize that the ladder in Figure 8 is in no way different from the conventional 8421 BCD ladder. The modifications in the design are: (1) the —2 and —1 weights are driven from the False side of their respective flip-flops, and (2) the negative weights are driven from a negative source.

It follows that the same ladder geometry can be used for any code in the same family of transformed codes. The ladder in Figure 8 could be used for the 8421, 842-1, 84-21, 84-2-1, 8-421, 8-42-1, or 8-4-21 codes. If weight inversions are allowed as in the excess-3, there are 112 different codes that can use the 8421 ladder geometry.

BASIC BCD CODES

If four positive weights can combine by addition into ten sequential decimal digits, it is possible to shift the sequence up or down by code adding or subtracting constants to one or more of the weights. It is not known *a-priori* what these sequences are. It might be assumed that they are the transformed families of codes in Figure 2 but this does not prove that no others exist. It may be possible that a code exists that can not be transformed by integral constants to the 0 through 9 format.

By using similar methods to those in deriving the 88 conventionally weighted codes, it is possible to derive all n sequences. A few of the theorems for "10-sequences" will be listed but not proved. Although the proofs are not difficult, some are rather tedious.

(1) At least one weight must be odd.
(2) The sum of the weights must be ≥ 9.
(3) All weights must be ≤ 8.
(4) There must be at least three unique weights.
(5) If two weights have the same value, they must be ≤ 4.
(6) The sum of the two smallest weights must be ≤ 8.

Use of the above theorems (plus several others) allows a table of about 80 code entries to be made and tested. Of the 80 entries, 33 are valid. Figure 9 shows each of the basic codes plus the sequence possible from each.

Comparing the basic 10-sequence codes against the code families of Figure 2 it can be seen that there are no surprises. Each code family is represented once and only once.

From the above it may be fairly stated that since all 4-bit BCD codes are transforms of the basic 10-sequence codes, there are, in a sense, only 33 codes.

WEIGHTED BINARY NUMBERS

As mentioned in the beginning of this article, the general form of a straight binary number is: $a_n 2^n + a_{n-1}2^{n-1} + \ldots + a_0 2^0$, where each a_i can have the value of 0 or 1. In tabular form the code can be written as shown in Figure 10.

Since each weight can have the value of 2^n or 0, the code might more properly be represented as: ...

D	C	B	A	
8	4	0	0	
0	0	−2	−1	
0	0	0	0	−3
0	0	0	1	−2
0	0	1	0	−1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	2
0	1	0	1	3
0	1	1	0	4
1	0	0	0	5
1	0	0	1	6
1	0	1	0	7
1	0	1	1	8
1	1	0	0	9
1	1	1	0	10
1	1	1	0	11
1	1	1	1	12

r

Fig. 7 Excess-3 code weighted

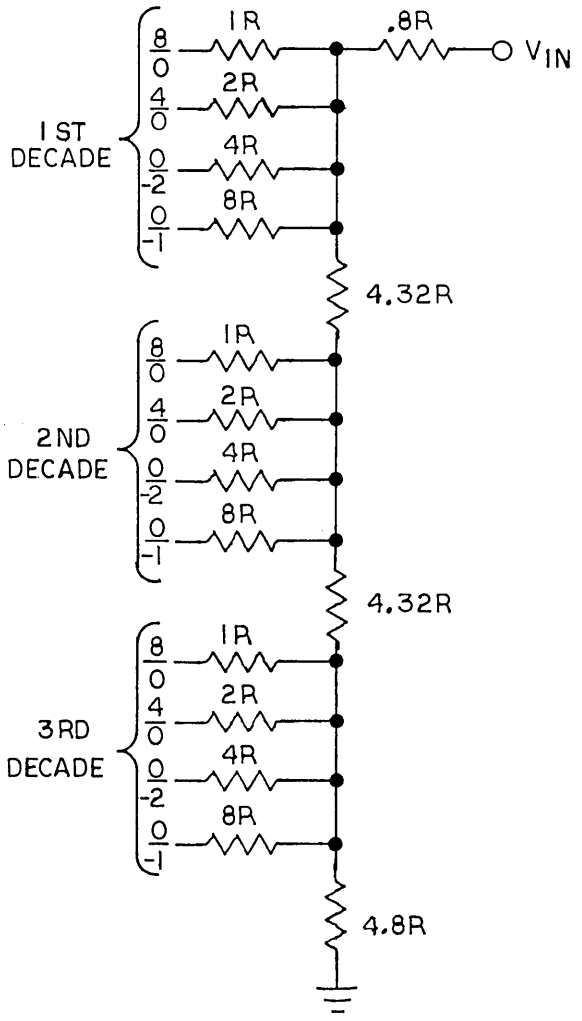

Fig. 8 Excess-3 ladder

		range				range
1.	3 3 2 1	0 – 9	18.	6 4 2 1	0 – 13
2.	4 2 2 1	0 – 9	19.	6 4 3 2	2 – 13
3.	4 3 1 1	0 – 9	20.	6 5 3 1	3 – 12
4.	4 3 2 1	0 – 10	21.	6 5 4 2	4 – 13
5.	4 4 2 1	0 – 11	22.	6 5 4 3	3 – 15
6.	4 4 3 2	2 – 11	23.	7 3 2 1	0 – 13
7.	5 2 1 1	0 – 9	24.	7 4 2 1	0 – 14
8.	5 2 2 1	0 – 9	25.	7 5 3 1	3 – 13
9.	5 3 1 1	0 – 10	26.	7 5 4 1	4 – 13
10.	5 3 2 1	0 – 11	27.	7 6 5 3	5 – 16
11.	5 4 2 1	0 – 12	28.	8 4 2 1	0 – 15
12.	5 4 3 2	2 – 12	29.	8 4 3 2	2 – 15
13.	5 4 3 3	3 – 12	30.	8 5 4 2	4 – 15
14.	6 2 2 1	0 – 11	31.	8 6 4 1	4 – 15
15.	6 3 1 1	0 – 11	32.	8 6 4 3	6 – 15
16.	6 3 2 1	0 – 12	33.	8 7 4 2	6 – 15
17.	6 3 2 2	2 – 11			

Fig. 9 Basic 10-sequence codes

.....	16	8	4	2	1	
0.....	0	0	0	0	0	0
0.....	0	0	0	0	1	1
0.....	0	0	0	1	0	2
0.....	0	0	0	1	1	3
	..	..	..	..	..	..
	..	..	..	..	..	..
0.....	1	0	0	0	0	16
0.....	1	0	0	0	1	17

Fig. 10 Binary Number Table

$\frac{16\,8\,4\,2\,1}{0\,\overline{0\,0\,0\,0}}$. This representation has the same basic properties as the BCD weighted codes just covered. For example, a constant k can be code added to any bit and the code will be shifted k digits.

To illustrate this, consider the $\frac{16\,8\,4\,2\,1}{0\,\overline{0\,0\,0\,0}}$ code. The range of the code is from 0 through 31. If −16 is code added to the $\frac{16}{0}$ bit the range is shifted 16 digits and the code now spans −16 through +15. The new code is represented as $\frac{0}{-2^n} \cdots \frac{4\,2\,1}{0\,0\,0}$. If the $\frac{0}{-2^n}$ weight is inverted, the representation is in no way different than the binary 2^s complement code.

By modifying the basic code to the $\frac{2^n-1}{0}\ \frac{2^{n-1}}{0} \cdots \frac{4\,2\,1}{0\,0\,0}$ code, subtracting $\frac{2^n-1}{2^n-1}$ from the $\frac{2^n-1}{0}$ weight and inverting the weight, the new code becomes $-\frac{2^n-1}{0}\ \frac{2^{n-1}}{0} \cdots \frac{4\,2\,1}{0\,0\,0.}$. This code is identical to the binary 1^s complement code where zero can be represented as either ...00000 or ..11111.

Both the 1^s and 2^s complement codes are widely used in arithmetic units of computers. An example of 2^s and 1^s complement codes are shown in Figure 11 in weighted format.

$\frac{8}{0}$	$\frac{-4}{0}$	$\frac{-2}{0}$	$\frac{-1}{0}$		$\frac{7}{0}$	$\frac{-4}{0}$	$\frac{-2}{0}$	$\frac{-1}{0}$	
0	0	0	0	0	0	0	0	0	0
0	0	0	1	−1	0	0	0	1	−1
0	0	1	0	−2	0	0	1	0	−2
0	0	1	1	−3	0	0	1	1	−3
0	1	0	0	−4	0	1	0	0	−4
0	1	0	1	−5	0	1	0	1	−5
0	1	1	0	−6	0	1	1	0	−6
0	1	1	1	−7	0	1	1	1	−7
1	0	0	0	8	1	0	0	0	7
1	0	0	1	7	1	0	0	1	6
1	0	1	0	6	1	0	1	0	5
1	0	1	1	5	1	0	1	1	4
1	1	0	0	4	1	1	0	0	3
1	1	0	1	3	1	1	0	1	2
1	1	1	0	2	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0

(a) 2^s Complement

(b) 1^s Complement

Fig. 11 Normal Complementary Codes

Note that in Figure 11b, zero can be represented as either 0000 or 1111.

The forms shown in Figure 11 are not the only transformations possible. A special form of complementary codes is possible by transforming all weights except the 2^n (or 2^n-1) weight. In Figure 12, alternate weighings are shown. The computer arithmetic is identical in both the normal and alternate codes except that the decimal numbers will be carried in an inverted form.

DECIMAL CODES

A 10^s or 9^s complement code can be considered a mixed radix weighted code. The usual form for a decimal number is: $a_n10^n + a_{n-1}10^{n-1} + \ldots + a_010^0$, where a_i can have any integral value 0–9. Consider the three-digit weighted code 100 10 1, where the weight is actually a multiplier of the column bit. In the 9^s complement form of this code a negative number is represented as the difference between the normal (positive digit) and 9. Figure 13 shows examples of 9^s and 10^s complement arithmetic.

The total code can be considered a $\frac{-999}{0}\ \frac{100}{0}\ \frac{10}{0}\ \frac{1}{0}$ weighed code. There is, however, one significant difference: the −999 weight is binary and can only take on the value of−999 or 0. The 10^s complement code can likewise be considered a $\frac{-1000}{0}\ \frac{100}{0}\ \frac{10}{0}\ \frac{1}{0}$ weighted code with the −1000 weight taking on only the binary values of −1000 or 0.

As with 1^s and 2^s complement binary codes, the complementary decimal codes can be carried inverted; i.e. $\frac{999}{0}\ \frac{-100}{0}\ \frac{-10}{0}\ \frac{-1}{0}$ and $\frac{1000}{0}\ \frac{-100}{0}\ \frac{-10}{0}\ \frac{-1}{0}$.

TRINARY CODES

The base 3 or trinary* (more properly ternary) num-

ber system is theoretically the most efficient of all weighted codes.[9] Unfortunately practical three-level inverters and three-level memory elements have yet to be invented. If two binary elements are used to represent a trinary number, one state will be wasted thus negating the possible gain of the trinary base.

It is not to be assumed that this condition will last for long. With integrated circuit techniques using MOS devices, three state storage elements and inverters can certainly be developed. In some computers, certain sections are already mechanized by trinary techniques.[10] The coming importance of the trinary base can be ascertained from the large number of papers devoted to the subject in the professional journals. In switching logic an entirely new class of combinational logic is possible using tri-position elements.

In the following pages, the relationships between the two basic base 3 systems will be shown.

CONVENTIONAL TRINARY

The normal form of a trinary number is: $a_n 3^n + a_{n-1} 3^{n-1} + \ldots + a_0 3^0$, where each a_i can have the value of 0,1, or 2. The trinary number 201 is equivalent to $2(3^2) + 0(3^1) + 1(3^0) = 19$. A modified weight symbol will be used for trinary, namely A/B/C where A is the "2" weight, B the "1" weight and C the "0" weight. The general form can be shown in weighted symbols as: . . . 54/27/0, 18/9/0, 6/3/0, 2/1/0. The span of a trinary code is 3^n where n is the number of digits. For a three digit code, the span is $3^3 = 27$, i.e. from 0 through 26. Figure 14a shows the table for a normal two-digit trinary code.

Negatrinary

Consider the trinary code 2a/a/0, 2b/b/0. The range of the code will be 0 through 2a+2b. If "a" is code subtracted from the first weight and "b" code subtracted from the second weight, the new code: a/0/-a, b/0/-b will have a range from -(a+b) through (a+b). This shifted form of representing trinary codes is sometimes called negatrinary (Fig. 14b). There are several real advantages in using negatrinary: (1) a number can be converted to its negative equivalent by merely complementing every non-zero weight; and (2) it is usually more convenient to use equal bipolar voltages (+V and -V) rather than +V and +2V in a digital system.

The relationship between normal and negatrinary is easily seen. Consider a set of trinary digits, each "shifted" −1. This is equivalent to subtracting $111\ldots_3$ from the number. If $111\ldots_3$ (n+1 digits) were first added to the trinary set (mod 3) and then each digit shifted −1, the real value of the number would be the same as the original normal trinary number. Example: Consider the trinary number $02101_3 = 2(27) + 9 + 1 = 64$.

```
 0 2 1 0 1
+1 1 1 1 1
 2 0 2 1 2
 ↓ ↓ ↓ ↓ ↓
 1−1 1 0 1
```

1−1 1 0 1 = 81−27+9+1 = 64

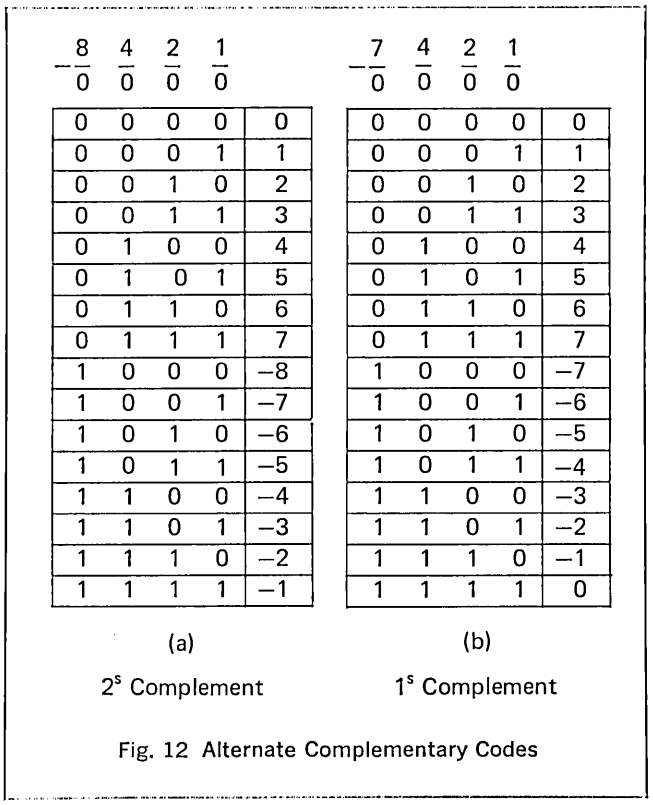

Fig. 12 Alternate Complementary Codes

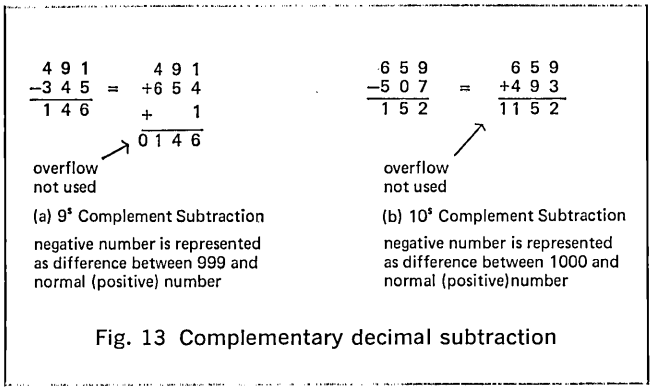

Fig. 13 Complementary decimal subtraction

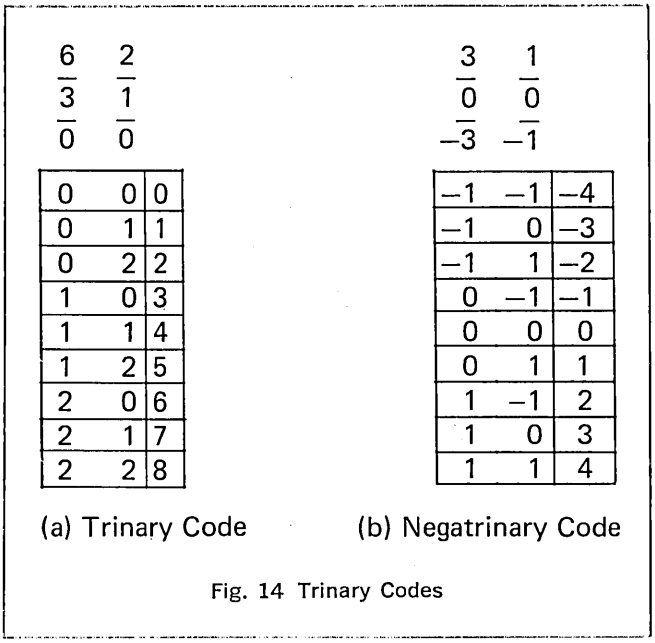

Fig. 14 Trinary Codes

To convert directly from decimal to negatrinary:
(1) add 1 to the number (n)
(2) divide by 3 holding the remainder
(3) add 1 to the dividend
(4) continue dividing by 3 and adding 1 to each new dividend
(5) shift each remainder −1
The new remainders (in reverse order) will be the negatrinary number. Example: Convert decimal 70 to negatrinary:

$$
\begin{array}{rll}
 & 70 & \\
3 & 71 & \\
 & 23 \quad + 2 \longrightarrow & 1 \\
3 & 24 & \\
 & 8 \quad + 0 \longrightarrow & -1 \\
3 & 9 & \\
 & 3 \quad + 0 \longrightarrow & -1 \\
3 & 4 & \\
 & 1 \quad + 1 \longrightarrow & 0 \\
3 & 2 & \\
 & 0 \quad + 2 \longrightarrow & 1
\end{array}
$$

As an interesting byproduct, the recreational mathematics problem of determining the weights to be used on both pans of a balance scale to measure a given integral weight is neatly solved by converting the weight to negatrinary. The negative weights are placed on one pan, the positive on the other.

Trinary Coded Decimal

As with binary, trinary logic must somehow relate to the decimal world. One method of doing this is to use trinary elements in combination to represent decimal integers. Two trinary elements in combination have a maximum of 9 states (one less than is needed). Thus three elements are the minimum necessary for trinary coded decimal or TCD.
The derivation of all TCD codes in similar to the methods used in the derivation of BCD codes. First all 10-sequence trinary sets are derived, then the weights are shifted in all possible integral units that will allow the sequences 0 through 9. The 10-sequence sets are all positive and each digit can take on the value of 0, a, or 2a. Note that a 10-sequence does not necessarily start at 0. It turns out that there are 50 10-sequence trinary sets. These are listed in Figure 15 with the sequence possible from each.
There are four basic types of TCD codes:

(1) All digits positive
(2) One digit negative
(3) Two digits negative
} each digit 0,1, or 2

(4) Negatrinary — each digit −1, 0, or+1

There are 16 positive codes, 74 1-negative codes, 19 2-negative codes, and 19 negatrinary codes, making 128 codes in all. If hybrid mixtures are allowed (e.g. one digit −1, 0, or +1 and other (s) 0, 1, or 2) then 331 additional codes are possible. The basic codes are listed in Figure 16. Note that sequence 4, 16 and 48 cannot be transformed into a basic code.

	A	B	C	range		A	B	C	range
1.	2	2	1	0 – 10	26.	6	5	4	8 – 22
2.	3	1	1	0 – 10	27.	7	2	1	0 – 20
3.	3	2	1	0 – 12	28.	7	3	1	0 – 22
*4.	3	2	2	2 – 12	29.	7	3	2	2 – 22
5.	3	3	1	0 – 14	30.	7	4	1	4 – 20
6.	3	3	2	2 – 14	31.	7	4	2	6 – 20
7.	4	1	1	0 – 12	32.	7	5	1	5 – 21
8.	4	2	1	0 – 14	33.	7	5	3	10– 20
9.	4	3	1	0 – 16	34.	7	5	4	7 – 25
10.	4	3	2	2 – 16	35.	7	6	2	6 – 24
11.	5	1	1	0 – 14	36.	7	6	4	10– 24
12.	5	2	1	0 – 16	37.	8	3	1	0 – 24
13.	5	2	2	4 – 14	38.	8	5	1	5 – 23
14.	5	3	1	0 – 18	39.	8	7	3	13– 23
15.	5	3	2	2 – 18	40.	8	7	5	12– 28
*16.	5	4	1	4 – 16	41.	9	3	1	0 – 26
17.	5	4	2	4 – 18	42.	9	3	2	2 – 26
18.	5	4	3	3 – 21	43.	9	4	3	6 – 26
19.	6	2	1	0 – 18	44.	9	5	3	8 – 26
20.	6	3	1	0 – 20	45.	9	6	1	6 – 26
21.	6	3	2	2 – 20	46.	9	6	2	8 – 26
22.	6	4	1	4 – 18	47.	9	6	4	12– 26
23.	6	4	3	6 – 20	48.	9	6	5	14– 26
24.	6	5	2	4 – 22	49.	9	7	3	12– 26
25.	6	5	3	8 – 20	50.	9	8	3	14– 26

Fig. 15 Ten-sequence trinary sets

In a practical sense, either the positive or the negatrinary codes should suffice for any normal application. The negatrinary codes are actually double codes. Each code has a minimum range of −9 through +9. By using negatrinary rather than conventional positive codes, a bipolar instrument or a digital machine using negative numbers would not require modified logic to represent negative quantities as in binary.

SUMMARY

- Binary codes were shown to be double weighted and as such the False weight need not necessarily be zero.
- By code addition, any n-sequence set can be shifted into any other n-sequence. The range is invariant under the transformation.
- A method of deriving all 10-sequence binary sets has been shown. By shifting these sets, all 4-bit BCD codes can be derived.
- Certain BCD codes usually considered non-weighted were shown to be disguised negative weighted codes.
- Two types of trinary codes and TCD codes were derived in a manner analagous to the BCD codes.

By using the expanded concepts as outlined in the foregoing pages, the mechanization of weighted codes can be exploited in a much freer manner. In digital instruments and machines the advantages of the new concepts should be considerable.

Pos

	A	B	C
1.	2	2	1
2.	3	1	1
3.	3	2	1
4.	3	3	1
5.	4	1	1
6.	4	2	1
7.	4	3	1
8.	5	1	1
9.	5	2	1
10.	5	3	1
11.	6	2	1
12.	6	3	1
13.	7	2	1
14.	7	3	1
15.	8	3	1
16.	9	3	1

1–Neg

	A	B	C		A	B	C
1.	3	2	–1	38.	6	–5	4
2.	3	3	–1	39.	–6	5	4
3.	3	3	–2	40.	7	2	–1
4.	4	1	–1	41.	7	–2	1
5.	4	2	–1	42.	7	3	–1
6.	4	–2	1	43.	7	–3	1
7.	4	3	–1	44.	7	3	–2
8.	4	–3	1	45.	7	–3	2
9.	4	3	–2	46.	7	–4	1
10.	4	–3	2	47.	7	–4	2
11.	5	1	–1	48.	7	–5	1
12.	5	2	–1	49.	7	–5	3
13.	5	–2	1	50.	7	5	–4
14.	5	2	–2	51.	7	–5	4
15.	5	3	–1	52.	–7	5	4
16.	5	–3	1	53.	7	–6	2
17.	5	3	–2	54.	–7	6	2
18.	5	–3	2	55.	7	–6	4
19.	5	4	–2	56.	–7	6	4
20.	5	–4	2	57.	8	3	–1
21.	5	4	–3	58.	8	–3	1
22.	5	–4	3	59.	8	–5	1
23.	–5	4	3	60.	8	–7	3
24.	6	2	–1	61.	8	–7	5
25.	6	–2	1	62.	–8	7	5
26.	6	3	–1	63.	9	3	–1
27.	6	–3	1	64.	9	–3	1
28.	6	3	–2	65.	9	3	–2
29.	6	–3	2	66.	9	–3	2
30.	6	–4	1	67.	9	4	–3
31.	6	4	–3	68.	9	–4	3
32.	6	–4	3	69.	9	–5	3
33.	6	5	–2	70.	9	–6	1
34.	6	–5	2	71.	9	–6	2
35.	–6	5	2	72.	9	–6	4
36.	6	–5	3	73.	9	–7	3
37.	6	5	–4	74.	9	–8	3

2–Neg

	A	B	C
1.	5	–1	–1
2.	5	–2	–1
3.	5	–3	–1
4.	6	–2	–1
5.	6	–3	–1
6.	6	–3	–2
7.	7	–2	–1
8.	7	–3	–1
9.	7	–3	–2
10.	7	–4	–1
11.	7	–5	–1
12.	8	–3	–1
13.	8	–5	–1
14.	9	–3	–1
15.	9	–3	–2
16.	9	–4	–3
17.	9	–5	–3
18.	9	–6	–1
19.	9	–6	–2

Negatrinary

	A	B	C
1.	5	3	1
2.	5	4	3
3.	6	2	1
4.	6	3	1
5.	6	3	2
6.	6	5	2
7.	7	2	1
8.	7	3	1
9.	7	3	2
10.	7	5	4
11.	7	6	2
12.	8	3	1
13.	8	5	1
14.	9	3	1
15.	9	3	2
16.	9	4	3
17.	9	5	3
18.	9	6	1
19.	9	6	2

Fig. 16 TCD Codes

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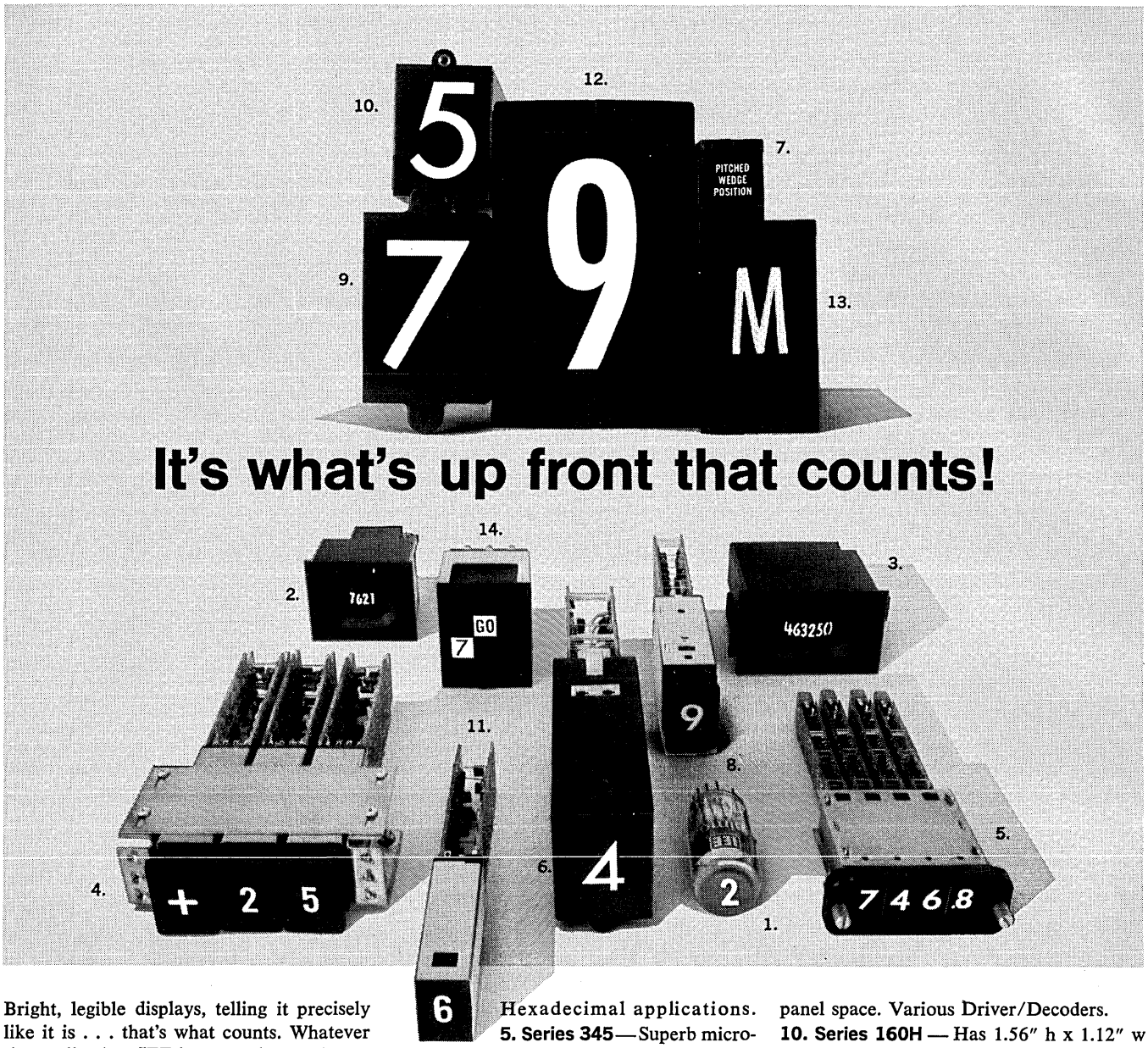

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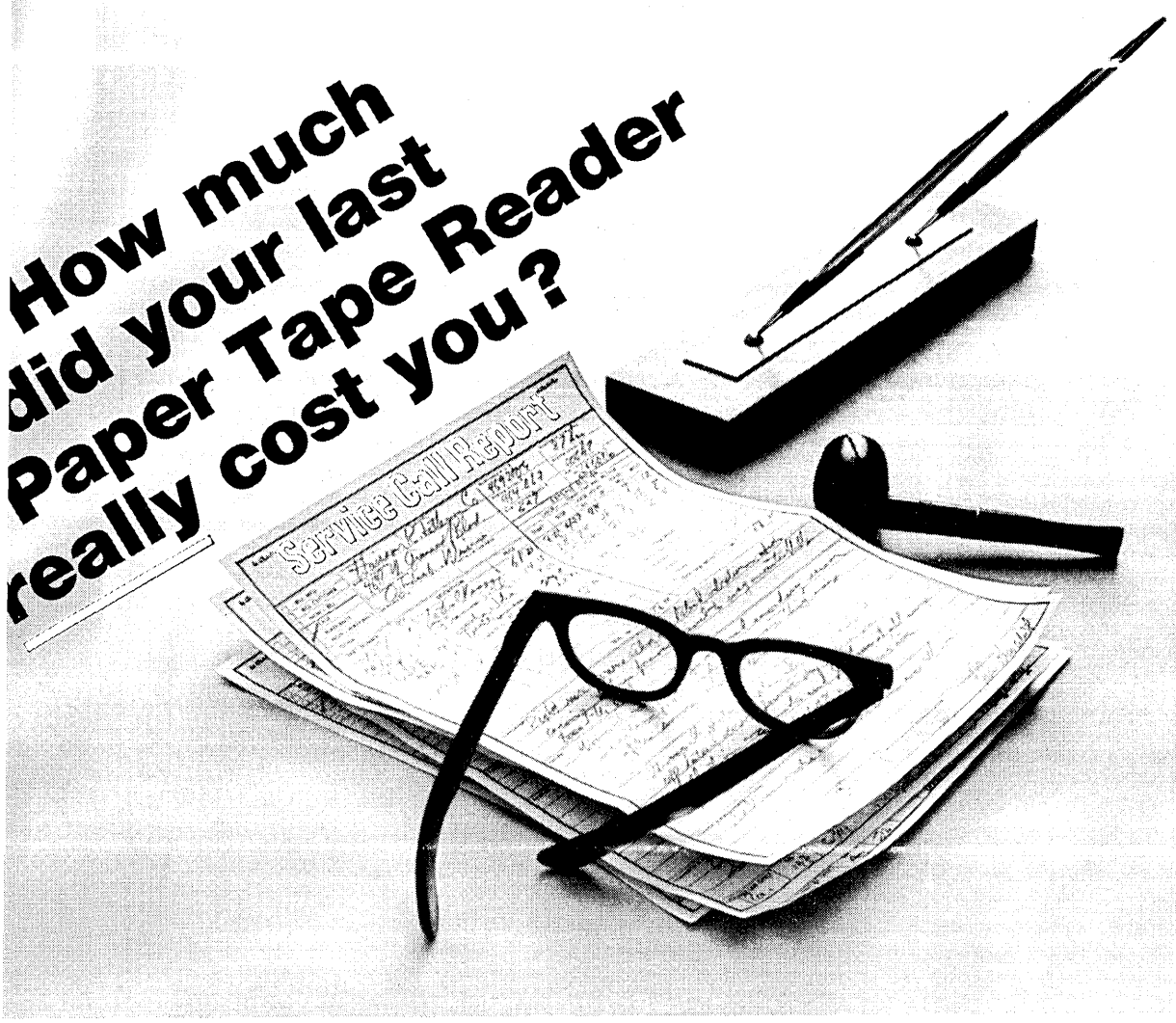

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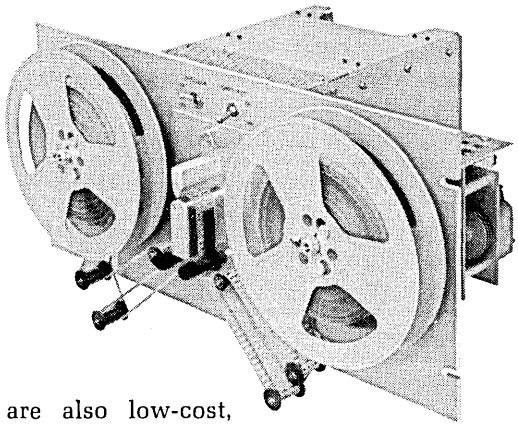

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CIRCLE 29 ON INQUIRY CARD

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A single high-speed serial storage loop may be used in conjunction with slower circuits to form interesting multiple path storage loops of varying lengths

Slower Data Flow Schemes for a High-Speed Serial Store

G. G. Langdon

IBM Corporation
Systems Development Div.
Endicott, New York

Delay lines were used for storage and data flow registers in some of the first generation computers. Today they are popular as buffer-storage in terminal equipment and small capacity data flows.[1] The delay line is economically competitive where a storage requirement of 1,000 to 20,000 bits exists. It is also quite versatile as shown by a number of applications reported by Peatman.[2]

Recently, high-speed delay lines of bit rates in excess of 100 MHz have been reported.[3, 4] Eveleth[3] states that quartz lines "have the unusual characteristic that when the frequency for which they are designed increases, the length can increase—thus maximum capacity increases rapidly with increasing frequency up to a limit of about 50,000 bits" at 150 MHz.

It is also observed that the major cost of a delay line, varying slightly with length, is in the input and output interfaces. In an application where more than one delay line (or serial store) is required, the capability of making a single delay line "look like" several delay lines is economically attractive.

A result of Newman, Davies, and Clayden[5] shows that the bits of an N-bit high-speed cyclic store can be transferred to an N-bit slow-speed cyclic store if the slow-speed bit rate is $1/n^{th}$ of the high-speed bit rate where n (the speed reduction factor) is an integer relatively prime to N. In transferring from the high-speed to the low-speed store, the high-speed group of N sequential bits is repetitively presented n times. On each presentation, each n^{th} bit is transferred so the entire group is transferred after N (slow) bit-times or n·N (fast) clock-times (n clock-times equals one bit-time.) Adjacent bits in the slow-speed store are n bits apart in the high-speed store.

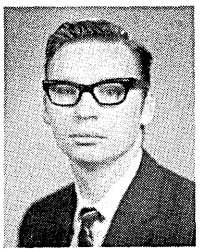
DEFINITIONS

The following discussion of present techniques is presented to introduce terminology and concepts.

A conventional way of using a high-speed store with slower data flows was used in the Saturn V computer made by the IBM Federal Systems Division for NASA.[6] There are four clock-times (W, X, Y, and Z) within a bit-time. These clock-times define four equal-length data channels on the delay line. Data channel 1 is written at clock-time W. Data channels 2, 3, and 4 are written at clock-times X, Y, and Z, respectively.

Each channel is used to store a 26-bit word. In the normal case, four words could be stored on a delay line (Fig. 1). This arrangement could be called the *word-bit interlace*. The bit arrangement on the Saturn V delay line could then be called the *bit-word interlace* (Fig. 2).

The concept of interlace can be extended just as the hierarchies are. If bits are assembled into digits, and digits are assembled into words, then the *simple interlace* would be the *word-digit-bit interlace*. If this is extended to groups of words, the *group-word-digit-bit-interlace* is the simple interlace.



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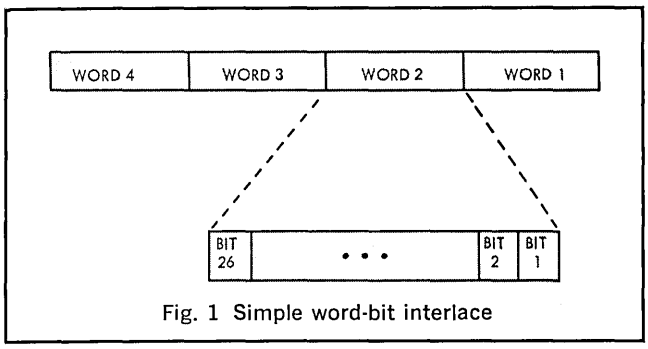

Fig. 1 Simple word-bit interlace

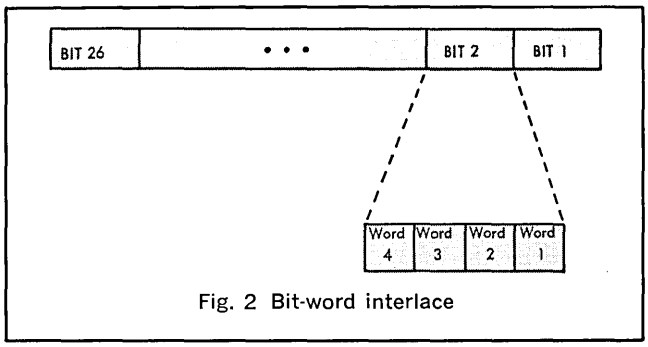

Fig. 2 Bit-word interlace

During a multiply in the Saturn V computer, two of the delay line registers are linked in series to form a data flow path of 52 bits. This is done by feeding the output of channel 1 into the input of channel 2 and the output of channel 2 to the input of channel 1.

As long as the length of the recirculation paths for the channels remains the same, or at least a multiple of the smallest loop length, the data will remain in step. By "in step" it is meant that if one channel reads out a lowest-order bit during a particular bit time, then all channels are reading out a lowest order bit in that bit time. It might be possible to be "in digit step" (bits within a digit or character are in step), but not be "in word step" (digits of unlike order being read off the line by some channels within the same digit time).

During some iterative operations like multiply, it is advantageous to keep the multiplier word out of step. If the multiplier word loop is foreshortened by two bits in each delay line cycle, the two lowest-order bits in the word are treated as operand bits; then, at the end of 13 cycles (iterations) all 26 bits of the multiplier word have served as operands.

Another method of using high-speed recirculating cyclic stores with slower speed data rates is *precession*.[7, 8] Precession can occur by making the data sampling interval, or multiples thereof, unequal to the recirculation time. For example, periodically writing bits at intervals one clock time longer than the recirculation time of the storage loop will produce a bit train with sequential data, one clock time apart. In another example, if the recirculation loop (or path) is made longer than the data to be stored, the information will walk backwards with respect to the timing. If the loop is foreshortened, then the information precesses forward. Precession is commonly used to "shift right" or "shift left" data on a delay line.

In order to foreshorten a recirculating loop containing an untapped delay line, a *window* must first be introduced (Fig. 3).

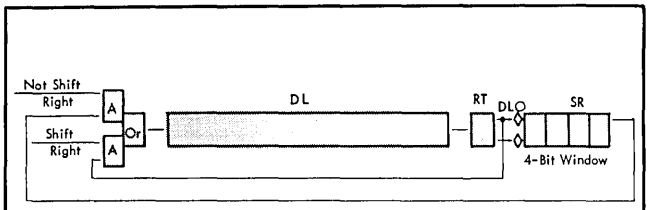

Fig. 3 A delay line recirculation loop

In Figure 3, the specific bit and shifting signals have not been explicitly shown. The bit appearing in the retiming trigger (RT) is shifted at the next clock time into the shift register (SR). It progresses through the four stages of SR and is then rewritten on the delay line (DL). The register SR is the window. *The window length will be called W* (in this case, W=4). Thus the recirculation path may be foreshortened by the window length of W bits by feeding the RT output (DLO) directly to the write driver. Thus a maximum of W bits may be shifted right in one delay line pass (revolution).

The complete system will be said to store N bits. The number N-W will be called the channel length C. (It includes the bit stored in the retiming trigger RT.) In the single channel case of Figure 3, the channel length C is simply equal to the delay line length, DL. In the previously mentioned four-channel scheme, the channel length is DL/4.

In many interesting applications, it may turn out that DL is not a multiple of n. From the Euclidean Algorithm, however, unique integers x and r, $o \leq r < n$, exist that:

$$DL = xn + r.$$

In this case x is defined to be the channel length C. In the Saturn V delay line, C=22 and r=1; this means the bits emerge 22 bit-times and one clock-time after they are written. (There are n clock-times to one bit-time.)

In the case r=0, the *minimum loop length* for a channel (minimum channel loop length) consists of C bits. When $r \neq 0$, the minimum loop length for a channel is C + 1 bits. In the above example, channel 1 is written at X clock-time, and emerges 22 bit-times (and one clock-time) later at clock-time Y. In order to be rewritten into channel 1, it must wait three clock-times for clock time X. Thus the minimum loop length is 23 bits.

The bit read at clock-time Y must be stored somewhere until the next clock-time X. This storage device serves much the same function for the channel data path as the detector does for the delay line sense amplifier output. To carry the analogy further, each device detects (or assembles) a bit sometime during a basic timing period and stores it until the end of that period. In the case of the delay line, the timing period is a clock-time, and at the end of each clock-time, the detector output is shifted to the retiming trigger. In the case of the "channel 1 detector" the basic timing period is one bit-time, and the output is either written back onto the line (for a shift right operation) or shifted into the first stage of channel 1's window. It is noted that the channel 1 detector is not a part of the

window but forms a necessary part of the 23 bit minimum loop of channel 1.

SINGLE PATH UNTAPPED DATA FLOW SCHEME

The definitions and concepts of the previous two sections may now be applied to a high-speed delay line storage system where the logic circuits operate at a much slower speed. One solution is to select n, make DL a multiple of n, and thereby set up n parallel channels (the digit-bit-word interlace). However, in order to keep the n channels in step, n windows must be provided if any shifting is to be done. If n is made equal to the number of bits in a digit, then a serial-by-digit, parallel-by-bit system (the simple interlace) may be designed. However, more logic is required because the data path is now n bits wide.

The high-speed serial store may be operated in the economical serial-by-bit, serial-by-digit mode by slower speed circuitry as shown in the following example.

Example 1

A 12-MHz delay line is available and can be cut to any desired length. The logic circuits to be used with the delay line allow the system bit rate to be no more than 1 MHz. However, special circuits for the 12-MHz clocking, retiming trigger, write driver, etc., are available. For the example a word of eight digits and eight bits per digit is to be recirculated, with a window of at least eight bits so the word may be easily shifted right one digit.

Figure 4 shows the scheme with the following constants:

$$\begin{aligned} 1 \text{ bit time} &= 12 \text{ clock times}, n = 12 \\ DL &= 55 = 4 \cdot 12 + 7 \\ W &= 9 \\ C &= 4 \\ r &= 7 \end{aligned}$$

The signal OSC is assumed to be the last half of a clock time. Thus for the memory regen path, the bit is assembled in the detector and at the fall of the signal OSC is shifted into the RT. It remains in the RT for one clock time, during the latter half of which OSC is valid.

In order to trace the path of a particular bit in Figure 4, assume it is being written on the line from stage 64 at CL5 time. Define bits written at CL5 time to emerge at CL12 time, because r = 7. Thus the bit is rewritten into channel 12. Channel 12 bits emerge at CL7 and hence are rewritten into channel 7. This continues for 12 passes making a 12-channel spiral. A bit makes 12 trips (at 55 clock-times per trip) through the delay line before emerging in the retiming trigger at CL5 time. Thus is spends 55 bit times recirculating in memory before appearing in the "data" detector. Nine bit times are spent in the window, completing the cycle of 64 bit times. The system of Figure 4 contains just one path, and will recirculate 64 bits through the data flow window for any speed reduction factor n relatively prime to 55. The conditions to be satisfied are:

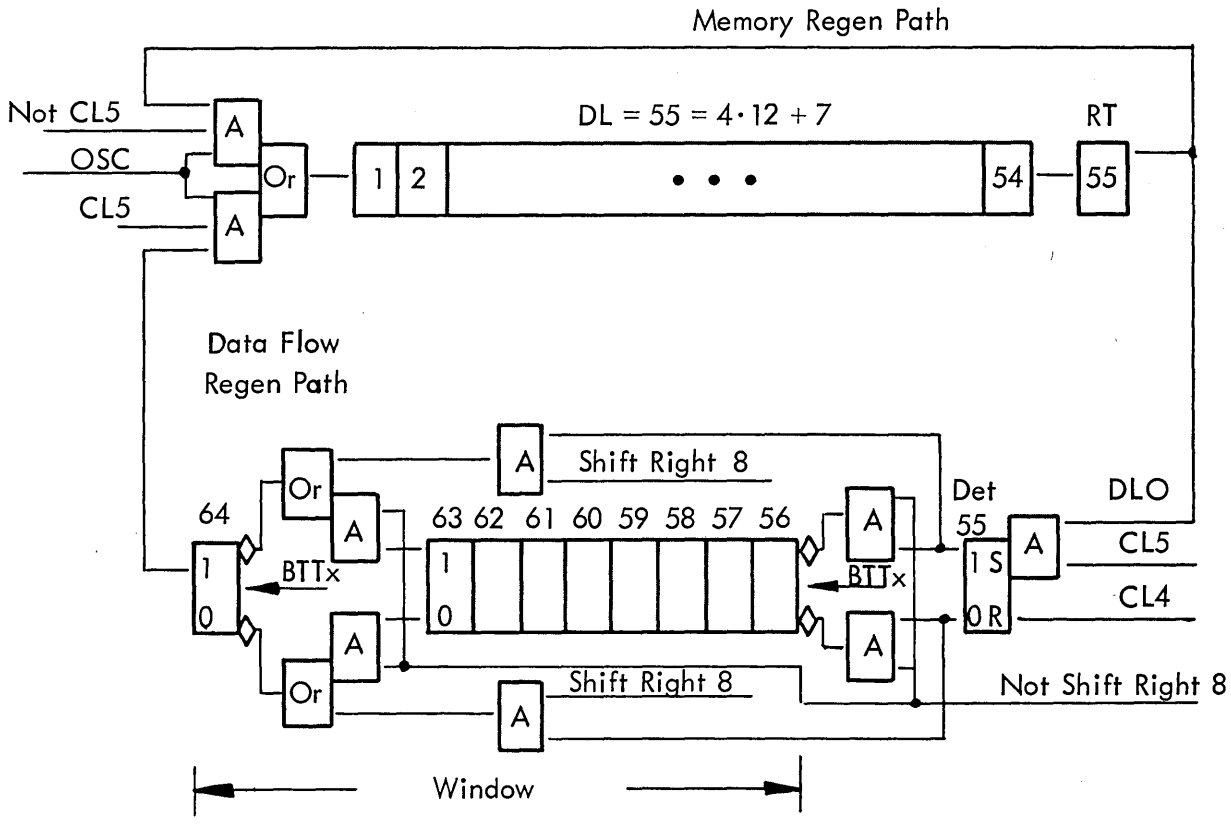

Fig. 4 A low-speed, single-path data flow scheme

1. N = DL + W = number of bits in system.
2. n and DL are relatively prime.

To facilitate the explanation of additional schemes, some definitions will be introduced. The complete path followed by a bit is called the data path. While in the "spiral," the memory bits travel at "clock time speed." After emerging in the data detector, the bits shift at "bit time speed" and the path is called the window and the bits are data bits. The minimum loop length for a data path is defined as the number of bits stored in the path minus the length of the windows in the path. For Figure 4 the minimum loop length is simply DL = N − W.

An example application for a speed-reduced delay line is a serial memory for phase-locked oscillator (PLO) systems. Assume it is desired to store the contents of two punched cards of 80 columns each, 12 bits per column, or 1920 bits. At a PLO bit rate of 100 kHz, the delay line would have to be 19.2 milliseconds long, a range barely attained by presently available delay lines. At a 1-MHz bit rate, however, the line would need to be only 1.92 milliseconds in length.

MULTIPLE PATH DATA FLOW SCHEMES

There are several classes of multiple path data flow schemes, including the simple parallel scheme used in the example drawn from the Saturn V computer. Other schemes will be illustrated by means of examples.

Example 2
Multiple-Path, Equal-Length Data Flow

In Figure 5, DL and n have a largest common divisor (LCD) of 2. This causes the 14 channels to be split into two spirals. One spiral circulates the "odd" bits in seven delay line passes ("spiral A"). The odd bits emerge in RT at CL5 and are shifted through window A before being written into spiral A again. The "even" bits circulate through "spiral B" and then through window B.

Each data path stores 29 bits in the spiral plus 4 bits in the window for a total of 33 bits. The minimum loop length for each path is 33−4 = 29 bits.

To visualize the movement of the bits in data path A, the motion of a bit written at bit 0 CL5 Time is depicted in Figure 6. Since there are n = 14 clock times to one bit time, bits emerge from the delay line C = 4 bit times plus r = 2 clock times after being written. Characteristics of this scheme are:

1. The number of data paths = LCD of n and DL.
2. The number of channels in each spiral is n/LCD.
3. The number of bits stored in each spiral is DL · LCD/n.
4. For the data paths to be of equal length, the windows must be of equal length.
5. The RT sampling times into each data path detector must be properly selected. Any group of LCD consecutive clock times would suffice.
6. The clock time used to gate a data path's bits into the data detector is the same clock time used to write that data path's bits onto the line.

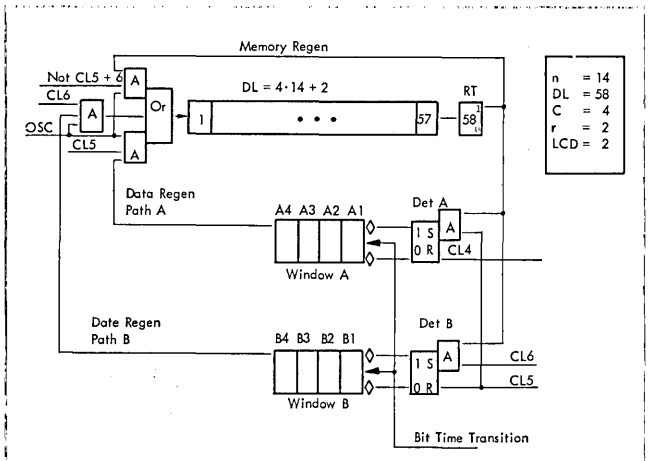

Fig. 5 A two-path, equal-length data flow scheme

Example 3
Single Path "Tapped" Data Flow Schemes

Two or more data paths can be connected in series to form one longer path. In Figure 7 this was accomplished from Figure 5 by writing A4 onto the line at CL6 (instead of CL5) and B4 onto the line at CL5 (instead of CL6). The effect here is to provide a read-write "tap" in the middle of the data flow path.

Multiple path "tapped" schemes, where paths are of equal or unequal length, can be designed from a multiple path equal length scheme by connecting paths as in Example 3 to attain a desired scheme. However, if n is not small, and windows are used, the windows plus data detection may involve a large number of circuits.

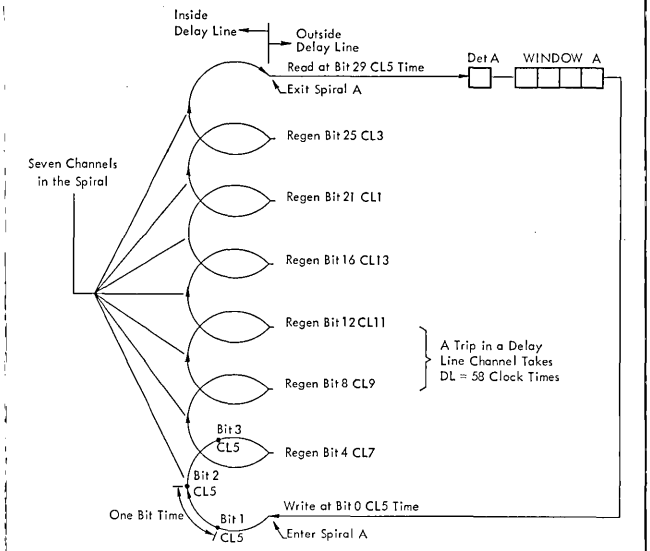

Fig. 6 Depiction of data path A

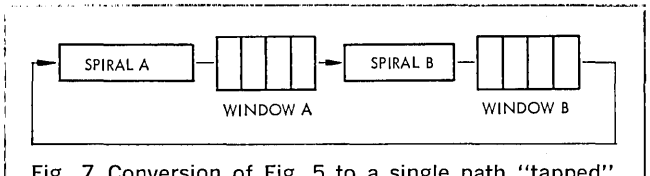

Fig. 7 Conversion of Fig. 5 to a single path "tapped" data flow scheme

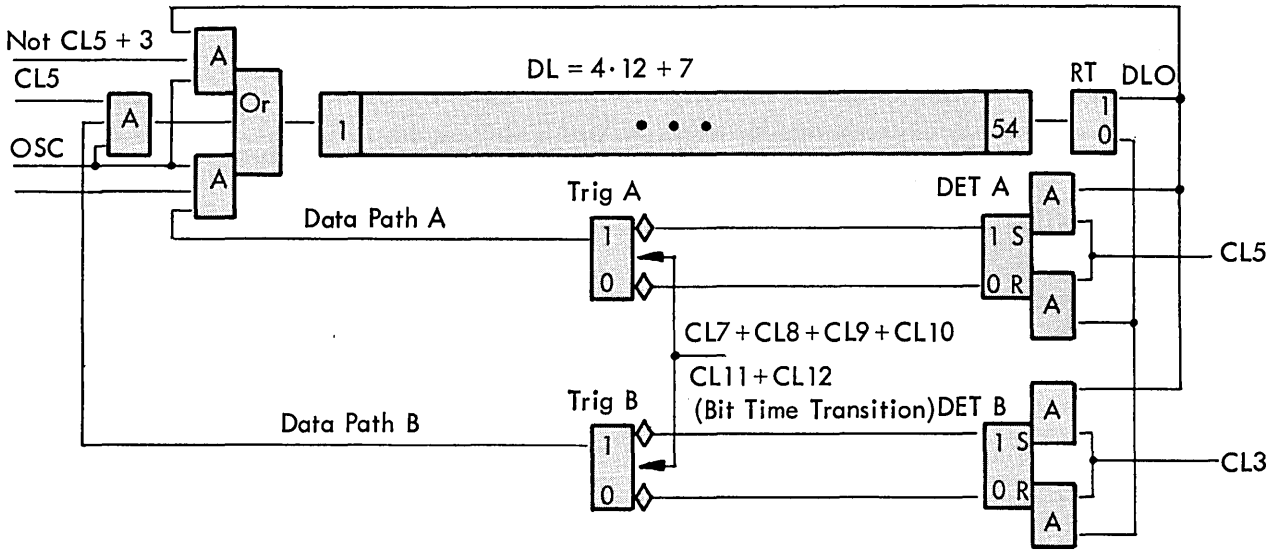

Fig. 8 Two path, unequal-length data flow—n = 12

Example 4

A Multiple Path, Unequal Length, Data Flow Scheme

Spirals of unequal length can be formed by first making n and DL relatively prime as in Example 1. As was seen, this forms a single spiral of n channels because the LCD of DL and n is one. This single spiral may be broken to form 2, 3, or n spirals.

In Figure 8, n = 12, C = 4 and r = 7 as DL = 4 · 12 + 7 as in Example 1.

The timing in the figure has been explicitly shown. The signal advancing the triggers is half a bit time, and will be called "bit time transition." Its "falling" after CL12 initiates the shifting of the data detectors' contents into their associated triggers.

The path of a bit appearing in the RT at CL5 time starts in DET A. At the subsequent bit time transition (from CL12 to CL1) it is shifted into TRIG A. From TRIG A it is written onto the delay line at CL3 time. It spends four bit times (C = 4) plus seven clock-times (r = 7) in channel 3 and then emerges at CL10 time. It is rewritten through the memory regen path. Written at CL10, it emerges in the RT, four bit times and seven clock-times later at CL5 time. This causes it to enter DET A again. Thus data path A consists of a two-channel spiral (55 clock-times per channel) and window A. The window actually consists of only two clock-times; the bit is rewritten onto the line ten clock-times after it appears in RT. Thus window A is not sufficient for a shift right operation (hence has zero length). Data path A stores (2 · 55 + 10)/12 = 10 bits.

A bit appearing in the RT at CL3 time is placed in DET B. It remains there for nine clock-times before being shifted into TRIG B. It remains in TRIG B for five clock-times before being written on the line at CL5 time. It enters spiral B (10 channels) appearing in the RT at the end of each delay line trip at CL12, CL7, CL2, CL9, CL4, CL11, CL6, CL1, CL8, and CL3, in that order. Window B consists of 14 clock times, and spiral B of 55 · 10 = 550 clock times. The length of data path B is 564/12 = 47 bits. By writing the output of DET B onto the line at CL5 time, the bits in the B data path may be shifted right. Thus the minimum loop length for data path B consists of 46 bits, and window B is by definition one bit in length.

In data path A, however, the minimum loop length is already the data path length of 10 bits. Hence window A is zero bits in length. The fact that window A and window B are not the same length is not obvious from observing Figure 8. It is certainly not obvious that window A, with one latch and one trigger, is not at least one bit in length. The failure of window A to be one bit in length results from the data bit being detected at a later clock-time than it is written.

Assume that Figure 8 is changed so that data path A's data bits are detected at CL1 time, and that data bits from TRIG A are written at CL11 time. Then it can be verified that the length of window A is 1 bit, and that data path A is now 11 bits in length—10 bits from spiral A and 1 bit from window A. By the same token, window B is now zero bits in length, and the length of data path B is then only 46 bits of spiral B.

It is noted that in Figure 8 the lengths of the two data paths are relatively prime, hence the two paths are certainly "out of step." However, by adding two shift register stages to window A and one stage to window B, data paths A and B would be 12 and 48 bits in length respectively. If we defined a word to consist of three 4-bit digits, then data path A would be one word long, and data path B would be four words long, so the two data paths would be "in step."

Example 5

A Desk-Top Computer Data Flow Scheme

In Figure 9, the A line and A register (A for accumulator) path stores one word of 8 digits with 8 bits per digit or 64 bits. The D line and D register path

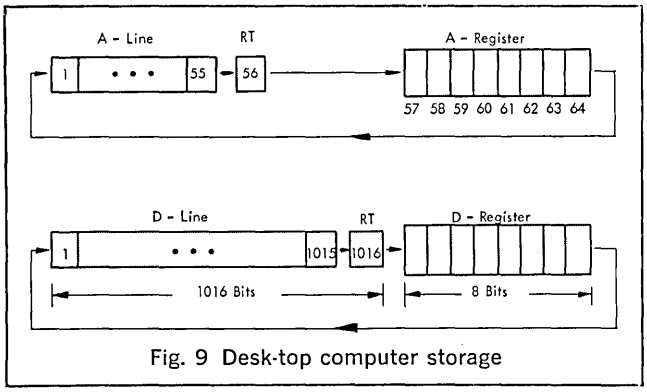

Fig. 9 Desk-top computer storage

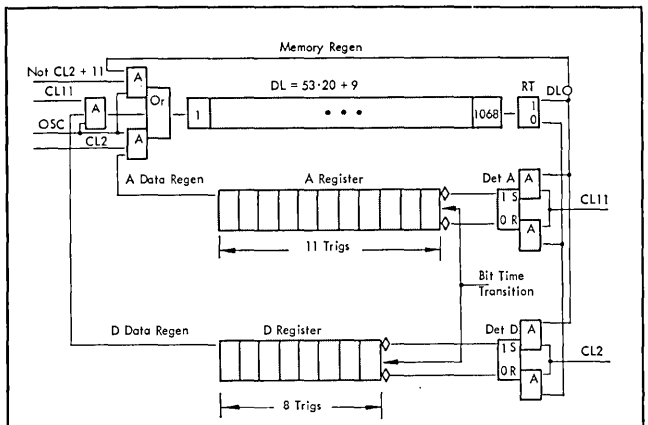

Fig. 10 Desk-top computer data flow scheme—n = 20

stores 16 words of 8 digits per word, 8 bits per digit or 1024 bits. The two paths are in step.

In Figure 10, DL = 1069 and n = 20; from this, 1069 = 53 • 20 + 9, hence C = 53, r = 9. The delay line has 20 channels, 53 bits (and nine clock times) in each channel. Examining window A of Figure 10, the A data bits are written on the line at CL2 time and detected at CL11 time. Since r = 9, and 2 + 9 = 11, spiral A consists of just one channel. (This implies that spiral D consists of 19 channels.)

The minimum loop length for data path A (also the minimum channel loop length) is 54 bits: 53 bits + 1 bit (nine clock-times in the spiral, nine clock-times in the DET A Latch and two clock-times in a trigger). The 11 triggers in the A register, shifting with bit-time transitions (from CL20 to CL1), permit a maximum shift right of 10 bits per pass. This is because A data bits are detected later in a bit-time than they are written. As in data path A of Figure 8, one trigger is needed for retiming and performs no storage function. Hence, window A is 10 bits in length and data path A is 10 + 54 = 64 bits in length.

Spiral D consists of 19 channels of 1069 clock-times per channel or 20,311 clock-times. Dividing by n, this is 1015 bits plus 11 clock-times. The minimum loop length for data path D is then 1016 bits: 1015 bits plus 11 clock-times in spiral D, and nine clock-times in the DET D Latch. Since path D's bits are detected earlier within a bit time than they are written, a trigger is not needed strictly for retiming purposes, and all eight triggers in the B register actually store bits. Thus, window B = 8 bits and data path B is 8 + 1016 = 1024 bits

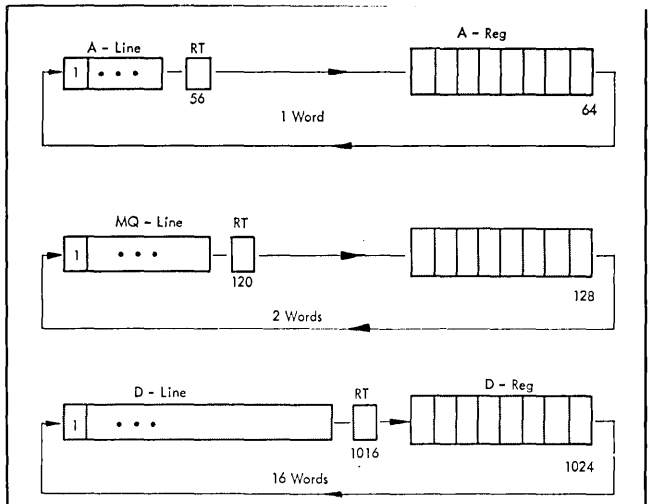

Fig. 11 Three delay line serial-by-bit scheme

in length. Thus it is verified that Figure 10 represents a single delay line scheme which imitates the two-delay-line scheme of Figure 9. With n = 20, a 10-MHz, 106.9-microsecond delay line (as used in Figure 10) would imitate the two 500-kHz lines. The higher speed configuration which imitates a slower speed data flow is not unique. In Figure 10, for example, one trigger could be removed from the A register and one could be added to the D register. Then by detecting A data bits at CL2 and writing them at CL13 (2 + 11 = 13), and detecting D data bits at CL13 and writing them at CL2, it can be verified that the new scheme derived from Figure 10 imitates Figure 9.

The principle of "slowing down" a high-speed cyclic storage loop can thus result in "electronic" read-write taps. A limitation, of course, is when a read-write tap is desired near the end or beginning of a line. Assume, for example, that it is desired to store 81 columns on a delay line, with an electronic read-write tap between the 80th and 81st columns. This implies a minimum of 81 channels on the line, hence a minimum speed reduction factor, *n*, of 81. Depending on the application, a speed reduction factor this high might result in a data bit rate which is too slow. With a 100-MHz delay line, an n of 80 would result in a data bit rate of 1.25 MHz.

The design of single, high-speed delay lines schemes to imitate slower speed schemes proceeds on a trial-and-error basis. This is illustrated by the following example.

Example 6

A Three-Delay-Line Serial-By-Bit Arithmetic System

The scheme of Figure 11 is very similar to Figure 9, where the structure of a word has been retained. However, an additional double-word length MQ is provided. The MQ line is used in conjunction with the A line to perform multiplication, division, and root extraction in less time than the configuration of Figure 9.

The number of bits stored in lines A, MQ, and D is 56 + 120 + 1016 = 1192; hence the length of the high-

speed line DL cannot be over 1192 bits. Assuming delay line A can be replaced by a one channel spiral, then the minimum channel loop length cannot be greater than 64 − 8 or 56. Numbers must be fitted to the following equations:

$$DL = CN + r \quad (1)$$

DL and n are relatively prime (2)

$$DL \leq 1192 \quad (3)$$

$$C \leq 55 \quad (4)$$

For reasons of economy, the values for DL and C should be close to their upper bound because this implies fewer bits to be stored in triggers. From the outset, however, the design should anticipate the use of at least 16 triggers for window MQ. This is eight more triggers than the eight required for the window.

Spiral A is to be a single-channel spiral, hence, spiral MQ will be a two-channel spiral. If C = 55, then spiral MQ can store at most 2C + 2 or 112 bits. The other 16 bits in the data path must be stored in register MQ. (2 was added to 2C because an additional bit could be stored in the spiral if r > n/2.) This gives:

$$DL \leq 1192 - 8 = 1184 \quad (3a)$$

Path D can store at most 1016 bits in its spiral. With C < 56, spiral D must be at least 18 channels (1016/56 = 18 + 20 remainder) which places a lower bound of 18 + 2 + 1 = 21 on n. Since 1184 = 56 · 21 + 8 yields a C > 55, the following is tried:

$$DL = 1183 = 53 \cdot 22 + 17 \quad (3b)$$

As desired, C < 56; however, the 19-channel spiral D would store 53·19 bits plus 17·19 clock-times = 1021 bits + 15 clock-times. This would give D a minimum loop of 1022 bits in length. Since 53 · 19 = 1007, the length of spiral D contributed by r should not exceed nine bit-times or 189 clock-times. Dividing 189 by 19 yields an r of 9. So let:

$$DL = 1175 = 53 \cdot 22 + 9 \quad (3c)$$

Hence DL = 1175, C = 53, n = 22, and r = 9.

Now, properly ordered clock-times are required such that 1-, 2-, and 19-channel spirals are formed. Data path A's bits must be written on the line nine clock-times before they are detected. Data path MQ's bits must be written on the line 18 clock-times before they are detected. The conditions are satisfied if paths A, MQ and D are written at CL7, CL16, and CL12 respectively, and detected at CL16, CL12, and CL7 respectively.

The selection of the clock-times can be done by trial and error. Since a first trial is arbitrary, assume data path A's bits are written on CL1. Since this is nine clock-times before detection, path A's bits are detected at CL10. Now, either path MQ or Path D's bits are to

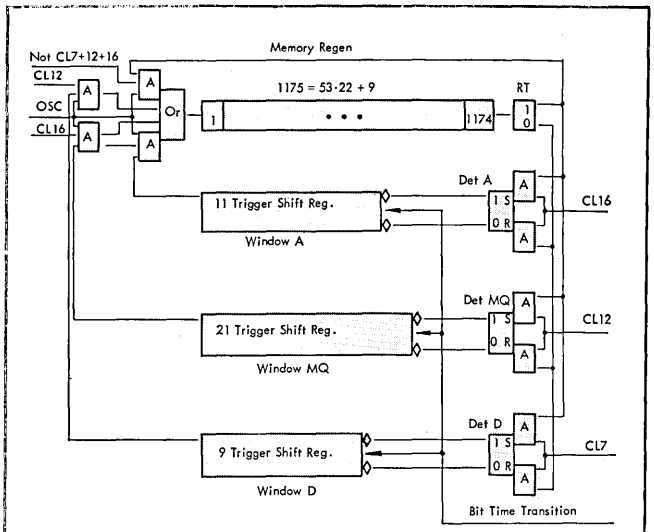

Fig. 12 A triple-path, serial-by-bit system—n = 22

be written at CL10. Assume path MQ. Then 10 + 18 = 28. But there is no CL28; so n is subtracted, and it is found that MQ's data bits are detected at CL6. This means path D must be written at CL6 and detected at CLI. By adding six to each clock-time, (utilizing clock-times toward the "center" of a bit-time) the former solution is obtained.

Spiral A contains 53 bits, nine clock times, so its minimum loop length is 54 bits. Window A is therefore 10 bits in length. Since A data bits are written at an earlier clock time than when they are detected, an extra retiming trigger must be added.

Spiral B contains 106 bits, 18 clock times, so its minimum loop length is 107 bits. Window B is therefore 21 bits in length. This involves more shift register storage than desired, and results from the fact that spiral MQ cannot store more than twice the number of bits in spiral A. This means window MQ is about twice the size of window A.

Spiral D contains 1007 bits plus 9·19 clock times or 1014 bits plus 17 clock times, so the minimum loop length is 1015 bits. Window D is therefore 9 bits in length. The resulting design, shown in Figure 12, imitates the three delay line scheme of Figure 11.

If a 100-MHz delay line were used above, a bit-time would be 220 nanoseconds. One pass of the A path would take 14.08 microseconds.

Example 7
A Parallel-By-Bit System

The techniques of the equal length data flow scheme of Example 2 may be applied to Example 6. By converting the organization of Figure 11 to a serial-by-digit, parallel-by-bit system: the data path has seven digits on the A line and a one digit window; the MQ data path has 15 digits on the MQ line and a one digit window; and the D data path has 127 digits on the D line and a one digit window. The word structure is the same as in the previous example.

Design of the parallel-by-bit system can utilize "digits" and "digit-times", as opposed to previous de-

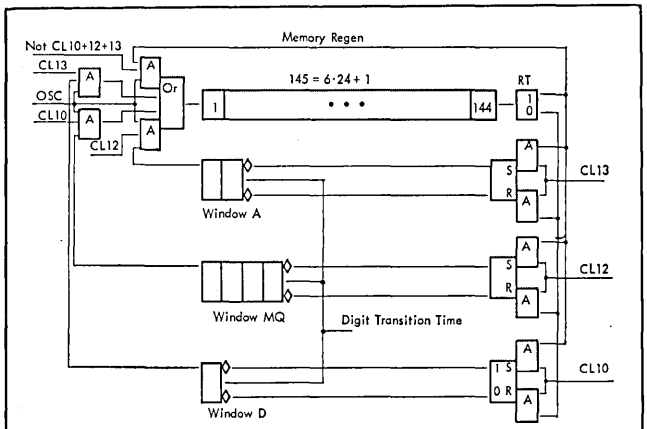

Fig. 13 Three-digit path system—n = 24

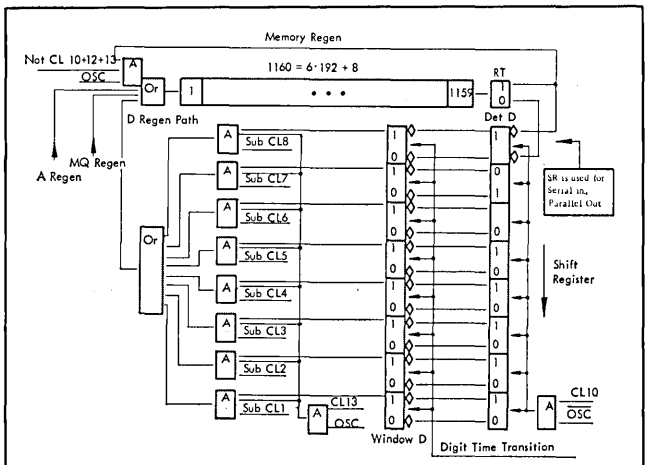

Fig. 14 Partial data flow, parallel-by-bit scheme—n = 192

signs which dealt with bit-times. Figure 13, an interim solution, is based on digits.

Figure 13 may now be "expanded" to form an 8-bit wide path. Let DL be $8 \cdot 45 = 1160$ bits in length, and let the speed reduction factor be $24 \cdot 8 = 192$. The LCD of DL and n is now eight. Spirals A, MQ, and D now have eight equal-length "sub-channels" set up within them.

Rather than show the entire parallel-by-bit scheme, only data path D is shown in Figure 14. Assume that within each of the 24 "clock-times," there are eight "subclock times." Thus the fall of OSC advances the subclock ring; the fall of subclock time 8 advances the clock ring.

As Figure 14 indicates, an 8-wide path requires more complex timing, more high-speed circuits, and a large OR gate into the delay line write driver.

The detector assembles the digits and has been illustrated here as an 8-bit shift register; it could just as easily have been implemented as eight latches. By the same token, the 8-way OR fed by eight 3-way AND's could be replaced by a parallel-in, serial-out, 8-stage shift register.

In the above scheme with a single delay line at a memory bit rate of 100 MHz, one digit time would be 1.92 microseconds. This means that the digits would "flow" at a 520-kHz rate, one pass of the A path would be 15.36 microseconds; one pass of the D path would be about 246 microseconds.

CONCLUSION

This article described how high-speed serial storage loops may be used in conjunction with slower circuits (although high-speed circuits are required in the interface) to form interesting multiple path data flow schemes. The cost of a delay line is usually independent of its length; to replace two or more slow-speed delay lines with one high-speed line may represent a cost advantage. A further advantage is better utilization of a single serial store for slow-speed technologies such as magnetics or FET where data flow rates must be slow.

When two or more delay lines are used in a single data flow scheme, their lengths must be "tuned" so the bits are in step. The single delay line schemes which imitate these data flows do not have this fine-tuning problem. Another advantage lies in connecting one or more spirals together to form electronic "read-write" taps.

Disadvantages lie in the requirement for high-speed interface circuits, and in possibly having to provide electronic storage for bits in excess of the desired window length.

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In any data communication application there are three major equipment considerations: computational facilities, terminal facilities and communications facilities. This survey is concerned with the third aspect—the data communications facility

A Survey of Data Communication Devices and Facilities

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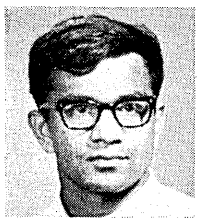
The underlying principles and practices of data communications were established in the telegraph field long before the digital computer was a practical reality, but its large scale use and development began only in the mid-1950's when it was recognized that teletypewriter circuits and machines used for transmitting messages could also be used for transmitting data to and from the computer. Because data communications is a significant aspect of information processing problems, it must naturally be considered by the system designer. There is a case for consideration of this technology whenever the elements of geographic dispersion, impatience for answers, and ultimate involvement of a computer system are present.

In any data communication application there are three major equipment considerations: computational facilities, terminal facilities and communications facilities. This survey is concerned with the third aspect, that is the data communications facility. Particular emphasis has been given to the problems of selecting the communications equipment and services. To aid the perspective user in a comparative evaluation for his needs, comprehensive charts have also been provided. Before proceeding to discuss the communications facilities, it is appropriate to consider the transmission techniques commonly employed and define some of the terms.

Editor's Note: The "Data Communications Terminals, Facilities, and Processing Equipment" section of the 1969-70 Computer Industry Annual is the foundation of this discussion. In addition to the facilities mentioned on the following pages, this section of the annual covers terminal devices, communication modes and processing equipment, data interchange codes, error control, reliability, system structure, design, and applications. Tables have been included illustrating comparative performances of communications-oriented processors, remote multiplexors, audio response units, CRT consoles, teleprinters, and card, tape, and other terminals.



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TRANSMISSION TECHNIQUES

Data transmission systems generally consist of three basic elements—a transmitter or source of information message; a transmission channel or carrier, often called a data link; and a receiver of the transmitted message. The channel or data link is a transmission path between two or more terminals and may be a single wire, a group of wires or a special part of the radio frequency spectrum. Channels are generally

classified on the basis of simultaneity, three basic types being simplex, half-duplex and full-duplex. *Simplex* is strictly unidirectional transmission. *Full-duplex* is the ability to transmit simultaneously in both directions while *half-duplex* is the ability to transmit in both directions but not simultaneously.

In half- or full-duplex modes, the data may be transmitted over 2- or 4-wire facilities. In most instances half-duplex transmission is over a 2-wire circuit. However full-duplex can also be handled by a 2-wire circuit. The 2- or 4-wire selection is the common carrier's responsibility, unless terminal specifications indicate differently.

In addition to simultaneity a channel is characterized by its bandwidth. Generally the greater the bandwidth of a channel, the higher the speed of transmission it will permit. The speed is usually measured in terms of bits per second, though measures such as words per minute or characters per second are still common terminology remnants of telegraphy. These channels are generally classified into three groups:

1. Narrowband channels: characterized by a speed range of 100 to 200 bits/sec; basically capable of handling manual keyboard devices.
2. Voiceband channels: characterized by a speed of 1200 to 3600 bits/sec; basically designed for handling voice transmission; specially prepared voice channels can handle data up to 9600 bits/sec.
3. Broadband channels: basically capable of handling data at a variety of rates ranging from few thousands of bits/sec to well into the megabits/sec range.

While the channels may appear to the user as a single data path, it may take on a variety of guises. The information bits may be transmitted either *serially* on on a single wire or in *parallel* over multiple wires. Except for very short distances (up to a few hundred feet), serial transmission is more efficient and is more prevalent. Many facilities, however, use a combination of serial and parallel transmissions.

There are two basic forms of serial transmission: synchronous and asynchronous. In *synchronous* transmission, the characters (and bits) are transmitted at a fixed rate with the transmitter and receiver synchronized. In *asynchronous* transmission the interval of time between characters can vary arbitrarily. This usually means that start and stop elements must be transmitted with each character. Synchronous transmission, though more difficult to implement, is the more efficient of the two as it obviates the need for start and stop elements. For this reason most computer input/output terminals for high-speed automated links have only the synchronous option available. In manual systems using keyboards, where high efficiency in transmission cannot be achieved because of lack of automation and the nature of interaction, the simpler asynchronous transmission is used.

Half-duplex operation generally makes a more efficient use of the communications facilities but requires time for line-turnarounds when the direction of transmission is to be changed. However, there are applications which require simultaneously bidirectional communications and others in which line-turnarounds are so frequent that full-duplex is the more efficient way to operate. Simplex operation is restricted to unidirectional transmission and finds very limited use.

TRANSMISSION LINE FACILITIES

The concept of distance that characterizes most data communications applications is that of "many miles." Consequently it is necessary to think in terms of obtaining communication facilities from the common carriers, the telephone companies and the Western Union Telegraph Company. While microwave and other radio facilities are doing an excellent job in many application areas, wire is still by far the most widely used medium. The wire circuits supplied by the common carriers are essentially of two grades, telegraph grade or narrowband and voice grade.

There are two basically different types of service that the common carriers offer. One is the public or exchange service which consists of subscriber lines connected to a switching system, as the telephone network. The other is the private line or channel leasing service which consists of full time leased point-to-point or multipoint lines connecting locations belonging to only one customer. The cost of the exchange service usually consists of toll charges based on the distance and length of connection, and a monthly service charge to maintain system access. The cost of private line service consists of a monthly rental based on the length and type of lines. The various common carrier offerings are discussed under the heading of common carrier facilities. Although the communications engineer prefers to measure the capacity of a communications channel in terms of bandwidth, it is much more natural to use the bits/sec or character/sec measure. Of the two measures, bits/sec is more universal as character sizes vary between systems. To achieve a desired transmission rate (in bits/sec) at a satisfactory low error rate, it is necessary to specify not only the nominal channel bandwidth, but also the line quality, the number of wires in the channel and the modulating-demodulating equipment (Modem).

MODEMS

These modems or datasets, as they are sometimes called, are necessary to adapt the modern data communications devices to wire transmission over long distances. These are usually furnished by the common carrier in the switched network or exchange service (public), but may be purchased from other vendors and manufacturers for the private leased line. Recently, in the Carterfone case decision the Federal Communications Commission (FCC), the regulating body for the common carriers, declared their blanket foreign attachments prohibition to be illegal, and has ordered the carriers to permit the attachment for harmless customer supplied equipment to the public switched networks. Thus the data communications user would be able to use the lower cost, higher performance modems supplied by numerous vendors. Voice channels have a nominal bandwidth rating of 4 kHz. Several different quality voice channels are available from the common carriers. The differences lie in the actual achievable bandwidth, the frequency responses and the delay characteristics. The better characteristics of the higher quality channels permit the use of modems with very high data transmission capabilities. The net effect of the combination of line

quality and modem may be best illustrated by an example given below using the information provided by the Rixon Electronics Company.

AT & T Voice Channel Type (All channels are 4 kHz nominal)	Rixom Modem	Transmission
4	Sebit-12M	1200 bits/sec
4A	Sebit-24M	2400 bits/sec
4B	Sebit-36M	3600 bits/sec
4C	Sebit-48M	4800 bits/sec

From this example it can be seen that achievement of desired data transmission rate on a communications facility requires careful engineering of the facility in combination with the modem. The remaining consideration in the communications setup choice is the number of wires in the channel. A two-wire channel can support transmission in one direction only (except when special paralleltone modems are used). The two-wire channel can, however, support transmission alternately in either direction. A four-wire channel can support transmission simultaneously in both directions at considerably less than twice the cost of a two-wire facility.

The choice between two-wire and four-wire facilities depends on the requirements for data transmission and acknowledgements. If a facility is to be used to transmit substantial quantities of data in both directions, then the four-wire channel may be favored. If transmission is primarily unidirectional there still exists the problem of delays due to acknowledgements. All modern systems for data transmission use block-by-block acknowledgement procedures. On a two-wire line, the system must halt transmission after each block and wait for acknowledgement. If the transmission rates are high and the blocks short, the delay experienced in receipt of the acknowledgement may reduce the net achievable transmission rate.

Tables I through IV summarize the equipment characteristics for most common carrier and non-carrier data sets. The cost data has also been included wherever possible. The monthly rentals are given for the common carrier equipment as these are almost always leased; but for the non-common carrier modems the purchase cost has been provided as these are usually purchased outright rather than leased. The prices are only approximate and vary with configurations and options. In the case of common carriers, prices also vary with the operating companies and it is recommended that the perspective buyer check with his local representative.

COMMON CARRIER FACILITIES

The common carriers, mainly the American Telephone and Telegraph Company (AT&T) or the Bell System, General Telephone and Electronics (GT&E) and Western Union Telegraph Company offer a wide variety of communications services and facilities both with and without modems. The services mentioned in this section are presented to give a basic indication of some of the communications facilities available today. The representatives of the communications companies should be consulted in order to obtain current information on rates, availability of service, channels and other devices pertinent to data transmission.

The communications services offered by the carriers take on a variety of forms and names with which the user should become familiar. Some of the communications services of the Bell System are WATS, Telpak, TWX and DATA-PHONE. The names of the services that may be obtained from Western Union are TELEX, INFO-COM, and DIAL-PAK. Western Union also recently placed an advanced digital data network (AUTODIN) service for the Department of Defense. These services are described below:

WATS for Wide-Area-Telephone Service is the name given to a telephone-grade service in which essentially an unlimited number of calls may be made from a single point to any other subscriber within a very large area usually for a fixed monthly charge. Monthly charges are based on the size of the area and not on the number or length of calls. Under the WATS arrangement, the United States is divided into six zones. The subscriber is billed according to the zones to be called on a full-time or measured-time basis. Costs vary widely depending on both the service area and the state in which the customer is located.

TELPAK is the name given to the service in which several telephone-grade lines are leased as a group between two points. It is essentially a pricing arrangement as the rates for service are substantially lower than an equivalent number of voice channels. The group of lines can be employed for any type of usage such as wideband data communications, voice, teletypewriter or facsimile transmission.

TWX and TELEX are the names applied to the teletypewriter exchange services of the Bell System and the Western Union, respectively. These provide direct dial point-to-point connections using input/output equipment such as page printers, keyboards, paper tape readers and paper tape punches.

DATA-PHONE provides for the transmission of data between a variety of terminal equipment using the regular dial telephone network or the WATS service. The cost to the customer is the same as the ordinary communications service cost in addition to a monthly rate for the Data Set.

DATA-PHONE 50 is the name of a recently announced switched wideband data communications service of the Bell system. A subscriber can now dial a call and send data at speeds up to 50,000 bits/sec, a 25-fold increase over the present "voiceband" DATA-PHONE service.

INFO-COM is the name of a new store-and-forward message or data communications service developed by Western Union.

DIAL-PAK is the name of a new concept by Western Union that will provide direct computer-to-computer communications using a 48-kHz wideband switched system.

In addition to the above services, voice grade and telegraph lines can be leased for the exclusive use of the subscriber. Table VI on tariffs for common car-

TABLE I EQUIPMENT CHARACTERISTICS OF COMMON CARRIER MODEMS

MANUFACTURER	AUTOMATIC ELECTRIC	AUTOMATIC ELECTRIC	AUTOMATIC ELECTRIC	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM
MODEL NUMBER	103C	401A/E	101A/C	103A	103B	103F	201A3	201A4	201B1	201B2
SPEED	----	20 char/sec	10 char/sec	200 bits/sec	200 bits/sec	300 bits/sec	2000 bits/sec	2000 bits/sec	2400 bits/sec	2400 bits/sec
SERIAL or PARALLEL	----	Parallel	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Serial
CHANNEL TYPE	Voice	Voice	TWX	Voice	Voice	Voice	Voice	Voice	Voice	Voice
NUMBER of WIRES	----	----	----	2	2	2	2/4	2/4	2/4	2/4
SYNCHRONOUS or ASYNCHRONOUS	----	Async.	Async.	Async.	Async.	Async.	Sync.	Sync.	Sync.	Sync.
SIMPLEX or DUPLEX	Full	Simplex	Simplex Half/full	Half/full	Half/full	Half/full	Full on 4 wire	Full on 4 wire	Full on 4 wire	Full on 4 wire
PRIVATE LINE MANDATORY?	No	----	No	No	Yes	No	No	No	Yes	Yes
AUTOMATIC CALL UNIT?	No	No	No	Yes	No	No	Yes	Yes	No	No
COMMENTS	Alternate voice/data service	Transmit only	Used with Teletype 33 & 35	----	----	----	No voice command, replacing 210A1	No voice command, replacing 201A2	No voice command	No voice command
COST*										
Rental $/month	----	----	----	25	25	25	70	70	70	70
Installation $	----	----	----	25	25	25	100	100	100	100

*Approximate only; prices vary with operating companies. Check with your local representative.

MANUFACTURER	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM
MODEL NUMBER	202A	202B	202C	202D	X202E	203A	301B	303B/C/D	401A	401E
SPEED	1200 bits/sec	1800 bits/sec	1200 bits/sec	1800 bits/sec	600 bits/sec	3600 bits/sec with reverse channel @ 150bps	40,800 bits/sec	19,200/50,000/ 230,400 bits/sec	20 char/sec	20 char/sec
SERIAL or PARALLEL	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Parallel	Parallel
CHANNEL TYPE	Voice	Voice	Voice	Voice	Voice	Voice	Voice	----	Voice	Voice
NUMBER of WIRES	2	2/4	2	2/4	2	2/4	----	----	2	2
SYNCHRONOUS or ASYNCHRONOUS	Async.	Async.	Async.	Async.	Async.	Sync.	Sync.	Sync. Async.	Async.	Async.
SIMPLEX or DUPLEX	Half	Full on 4 wire	Half	Full on 4 wire	Full	Full	Full (voice)	Full (voice)	Simplex Full (voice)	Simplex Full (voice)
PRIVATE LINE MANDATORY?	No	Yes	No	Yes	No	No	No	No	No	No
AUTOMATIC CALL UNIT?	No	No	Yes	Yes	No	Yes	No	No	No	No
COMMENTS	----	----	Replacing 202A	No voice command, replacing 202B		Up to 7200 bits/sec on private line	Sync. mechansim can be external	6/12/60 voice circuits	Transmit only; 24 possible characters	Transmit only; 99 possible characters
COST*										
Rental $/month	----	----	40	40	----	----	250	425/430/450	5	7.50
Installation $	----	----	50	50	----	----	200	300	15	20

*Approximate only; prices vary with operating companies. Check with your local representative.

TABLE II EQUIPMENT CHARACTERISTICS OF COMMON CARRIER MODEMS (CONT.)

MANUFACTURER	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM	BELL SYSTEM
MODEL NUMBER	401J	401H	X401L	X202F	402C	402D	X403A	X403B & C	602A	603A, B, & D
SPEED	20 char/sec	20 char/sec	20 char/sec	600 bits/sec	75 char/sec	75 char/sec	10 char/sec	10 char/sec	----	----
SERIAL or PARALLEL	Parallel	Parallel	Parallel	Serial	Parallel	Parallel	Parallel	Parallel	----	----
CHANNEL TYPE	Voice	Voice	Voice	Voice	Voice	Voice	Voice	Voice	Voice	Voice
NUMBER or WIRES	2	2	2	2	2/4	2/4	----	----	2	----
SYNCHRONOUS or ASYNCHRONOUS	Async.	Async.	Async.	Async.	Async.	Async.	----	----	Sync.	----
SIMPLEX or DUPLEX	Simplex	Simplex	Simplex	Simplex	Simplex	Simplex	Simplex	Simplex	Simplex	----
PRIVATE LINE MANDATORY?	No	No	No	No	No	No	No	No	No	No
AUTOMATIC CALL UNIT?	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	No
COMMENTS	Receive only; 99 possible characters	Transmit only; 99 possible characters	Transmit only	Transmit only	Transmit only	Receive only	Touch tone; receive only	Touch tone; transmit only	Analog transmitter	Analog facsmile transmitter
COST*										
Rental $/month	35	10	----	----	25	75	----	----	30	12-25
Installation $	50	20	----	----	40	100	----	----	40	25-50

*Approximate only; prices vary with operating companies. Check with your local representative.

MANUFACTURER	BELL SYSTEM	BELL SYSTEM	WESTERN UNION	WESTERN UNION	WESTERN UNION	WESTERN UNION	WESTERN UNION	WESTERN UNION	WESTERN UNION
MODEL NUMBER	801a & C	811B	1181-A	1601-A	2121-A	2241-A	100	200	300
SPEED	N/A	10 char/sec	180 bits/sec	600 bits/sec	1200 bits/sec	2400 bits/sec	200 bits/sec	2400 bits/sec	18,000/40,800 bits/sec
SERIAL or PARALLEL	Serial/ Parallel	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Serial
CHANNEL TYPE	Voice/TWX	TWX	----	Voice	Voice/ broadband	Broadband	Voice	Voice	Broadband
NUMBER of WIRES	2/4	2	----	----	----	----	2/4	2/4	2/4
SYNCHRONOUS or ASYNCHRONOUS	Asynchronous Synchronous	Async.	Async.	Async.	Async.	Sync./ Async.	Async.	Async.	Sync.
SIMPLEX or DUPLEX	Simplex Half/full	Simplex Half/full	Half/full	Half/full	Half/full	Half/full	Half/full	Half/full	Half/full
PRIVATE LINE MANDATORY?	N/A	No	No	No	No	Yes	No	Yes	No
AUTOMATIC CALL UNIT?	N/A	Yes	NO	No	No	No	No	No	No
COMMENTS	Automatic calling units	Used with teletype units		Alternate voice/data option					
COST*									
Rental $/month	----	25	30	30	40	42 Async. 72 Sync.	----	----	----
Installation $	----	15	None	50	50	50 Async. 100 Sync.	----	----	----

*Approximate only; prices vary with operating companies. Check with your local representative.

TABLE III EQUIPMENT CHARACTERISTICS OF NON-COMMON CARRIER MODEMS

MANUFACTURER	ANDERSON–JACOBSON	ANDERSON–JACOBSON	COLLINS RADIO	COLLINS RADIO	COLLINS RADIO	GENERAL ELECTRIC	GENERAL ELECTRIC	GENERAL ELECTRIC
MODEL NUMBER	ADC 260	ADC 300	TE-216A-2D	TE-216A-3D	TE-216A-4D	TDM-110	TDM-210	TDM-220
SPEED Bits per second	300	300	2400	3600	4800	300	1000-1800	2400
SERIAL or PARALLEL	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Serial
CHANNEL TYPE	Voice	Voice	Voice, type 3003 or CCITT M89	Voice, type 3004 or CCITT M89	Voice Type 3005	Schedule 4 Type 4 (Voice)	Type 4, 4A, 4B (Voice)	Type 4A (Voice)
NUMBER or WIRES	2	2	4	4	4	2	2/4	2/4
SYNCHRONOUS or ASYNCHRONOUS	Async.	Async.	Sync.	Sync.	Sync.	Async.	Async.	Sync./Async.
SIMPLEX or DUPLEX	Half/full Duplex	Half/full Duplex	Full Duplex	Full Duplex	Full Duplex	Full Duplex	Half/full Duplex	Half/full Duplex
PRIVATE LINE MANDATORY?	No	No	Yes	Yes	Yes	Yes	Yes	Yes
AUTOMATIC UNIT CALL?	No	No	No	No	No	No	No	No
MODULATION SCHEME			Phase-shift (Kineplex)	Phase-shift (Kineplex)	Phase-shift (Kineplex)	Frequency shift	Frequency shift	AM vestigial Sideband
COMMENTS	Portable, originate only	Portable, originate/ answer	Various options available	Various options available	Various options available	Compatible with BELL 103F	Compatible with BELL 202D	Internal clock at 2400 bps in sync. model.
PURCHASE COST*	—	—	—	—	—	$695.	$675.	$1,485 (Async.) $1,950 (Sync.)

*Cost data is approximate. Prices vary with configuarations and options.

MANUFACTURER	GENERAL ELECTRIC	GENERAL ELECTRIC	IBM	IBM	IBM	IBM	LENKURT ELECTRIC	MILGO
MODEL NUMBER	TDM-111	TDM-211	Line Adapter 1	Line Adapter 2	Leased Line	Shared Line	26C	4400/24PB
SPEED Bits per second	300	1200	Up to 600	Up to 600	Up to 600	Up to 134	1200/2400	2400
SERIAL or PARALLEL	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Serial
CHANNEL TYPE	Voice	Voice	Voice	Voice	Voice	Voice	Voice Schedule 4A	Voice Type 3002
NUMBER of WIRES	—	2	2/4	2	2/4	2/4	—	2
SYNCHRONOUS or ASYNCHRONOUS	Async.	Async.	Async.	Async.	—	—	Sync.	Sync.
SIMPLEX or DUPLEX	Full Duplex	Half Duplex	Half/full Duplex	Half Duplex	Half/full Duplex	Half/full Duplex	Simplex Full duplex	Simplex Full duplex Half optional
PRIVATE LINE MANDATORY?	No	No	No	No	No	No	Yes	No
AUTOMATIC CALL UNIT?	—	—	No	No	NO	No	No	—
MODULATION SCHEME	Frequency shift	Frequency shift	—	—	—	—	Duobinary	Phase-shift (Kineplex)
COMMENTS	Compatible with BELL 103A2	Compatible with BELL 202C	Limited Distance	Limited Distance	—	—	—	Simultaneous voice/teletype-transmission possible
PURCHASE COST*	$875-970	$850-1,145	—	—	—	—	—	$4,995

*Cost data is approximate. Prices vary with configurations and options.

For additional information on products listed, circle these numbers on inquiry card:

ANDERSON-JACOBSON 150
COLLINS RADIO 151
GENERAL ELECTRIC 152
IBM 153
LENKURT ELECTRIC 154
MILGO 155

TABLE IV EQUIPMENT CHARACTERISTICS OF NON-COMMON CARRIER MODEMS (CONT.)

MANUFACTURER	MILGO	PHILCO	PHILCO	PHILCO	PHILCO	PHILCO	PHILCO	RFL INDUSTRIES
MODEL NUMBER	4400/48	MD/NY	MC 12/24-2B	MC 12/24-1	Diplexer	EDC 1224	EDC 61-75	Series 2056
SPEED Bits per second	4800	1200/2400	300-2400	300-2400	75	75-2400	75	1200-1800
SERIAL or PARALLEL	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Serial
CHANNEL TYPE	Voice Type 3002	——	Voice	Voice	Voice	——	Teleprinter	Voice
NUMBER of WIRES	2	2/4	——	——	——	——	——	——
SYNCHRONOUS or ASYNCHRONOUS	Sync.	——	Sync.	Sync.	Sync./ Async.	Sync.	Sync.	Async.
SIMPLEX or DUPLEX	Simplex Full duplex Half optional	Half/full Duplex	Full Duplex	Full Duplex	Full Duplex	——	Full Duplex	Half/full Duplex
PRIVATE LINE MANDATORY?	No	Yes	Yes	Yes	No	Yes	No	Yes
AUTOMATIC CALL UNIT?	——	——	——	——	——	——	——	——
MODULATION SCHEME	Phase-shift (Kineplex)	——	——	——	——	——	——	Frequency shift
COMMENTS	——	High frequency radio modems	——	High frequency radio modems	For sending Teletype/voice signal simultaneously	Increased error detection and correction	Increased error detection and correction	Rack Mounting
PURCHASE COST*	$5,885	——	——	——	——	——	——	$625-850

*Cost data is approximate. Prices vary with configurations and options.

MANUFACTURER	RFL INDUSTRIES	RIXON ELECTRONICS	RIXON ELECTRONICS	RIXON ELECTRONICS	RIXON ELECTRONICS	RIXON ELECTRONICS	RIXON ELECTRONICS	RIXON ELECTRONICS
MODEL NUMBER	3227	Sebit-48	Sebit-36	Sebit-24M	PM-24	Sebit Dual 12M	FM-18D	FM-300
SPEED Bits per second	1000	4800	3600	2400	2400	Two channels at 1200	Up to 1800	Up to 300
SERIAL or PARALLEL	Serial	Serial	Serial	Serial	Serial	Serial	Serial	Serial
CHANNEL TYPE	Voice	C-4 Conditioning	C-2 Conditioning	C-1 Conditioning	C-1 Conditioning	C-1 Conditioning	C-2 condition-ing, dependent on speed	Unconditioned
NUMBER of WIRES	——	2/4	2/4	2/4	2/4	2/4	2/4	2
SYNCHRONOUS or ASYNCHRONOUS	Sync.	Sync.	Sync.	Sync.	Sync.	Sync.	Sync./ Async.	Sync.
SIMPLEX or DUPLEX	Half/full Duplex	Simplex Half/full Duplex	Simplex Half/full Duplex	Simplex Half/full Duplex	Simplex Half/full Duplex	Simplex Half/full Duplex	Simplex Half/full Duplex	Full Duplex
PRIVATE LINE MANDATORY?	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
AUTOMATIC CALL UNIT?	——	No	No	No	No	No	No	No
MODULATION SCHEME	Frequency shift	AM Vestigial sidband	AM Vestigial sideband	AM Vestigial sideband	Phase shift 4-level	AM Vestigial sideband	Frequency shift	Frequency shift
COMMENTS	Rack Mounting	Transmission Speeds Switch-selectable	Transmission Speeds Switch-selectable	Transmission Speeds Switch-selectable	Compatible with BELL 201B, 205 & 207 modem	——	Compatible with BELL 202D modem	Compatible with BELL 103F modem
PURCHASE COST*	$900-1,100	$6,000	$5,800	$2,500	——	$5,000	——	——

*Cost data is approximate. Prices vary with configurations and options.

For additional information on products listed, circle these numbers on inquiry card:

MILGO 155
PHILCO 156
RFL INDUSTRIES 157
RIXON ELECTRONICS 158

rier services also provides a summary of the various common carrier services. These are approximate tariffs currently in use and may change, but they do give a good indication of the likely costs of the data communications service. The perspective user is advised to check with his local common carrier representative, especially for the WATS service, as the cost of service depends on areas of use and state of residence of the user.

In most cases, the telephone-grade service can be employed for the transmission of voice as well as data through the use of dataphone subsets supplied by the telephone company. Frequently, this ability permits considerable savings by combining voice and data needs. Telephone coupler (usually acoustic coupling) data sets are also available from the telephone company and others which allow data to be transmitted over the public telephone network via a conventional telephone set. Table VI exhibits the major characteristics of most telephone coupler data sets on the market.

A number of new developments with special interest to computer/communications systems are taking place in the Bell System. One arrangement (203 Data Set) intended for use on the dial telephone network will operate at 3600 bits per second. Thus it will match the asymmetrical characteristics of information flow found in many situations such as keyboard entry and display output. On private-line voiceband circuits, the data set will operate at 4800 bits per second and possibly 7200 bits per second. These increases in speed made possible by multi-level vestigial sideband and automatic adaptive equalization will permit very favorable economies to be made in computer/communications systems.

Another development is that of the touch-tone telephones which can be used very effectively as data terminals. In cases where limited input capability is tolerable and no hard copy is needed (such as banking, credit, and some inquiry systems) the push button telephone provides a very inexpensive and reliable terminal.

The introduction of digital transmission techniques into the communications networks is likely to drastically reduce the cost of data communications. Pulse code modulation (PCM) techniques are gradually being introduced into the Bell System. Since PCM systems transmit on the order of 50 kilobits per second for each voice channel, there is a large potential for substantial economies. The digital carrier systems T1 (1.54 megabits per second), T2 (62 megabits per second), and T4 (281 megabits per second) are currently being developed and used in the Bell Systems. These digital transmission system will use time-division multiplexing extensively thus providing a variety of bit rates.

TABLE IV EQUIPMENT CHARACTERISTICS OF NON-COMMON CARRIER MODEMS (CONT.)

MANUFACTURER	SANGAMO	SANGAMO	SANGAMO	SANGAMO	SANGAMO	SANGAMO	SANGAMO	SANGAMO
MODEL NUMBER	T103A	T103F	T201A	T201B	T202C	T202D	T401E	T401H
SPEED Bits per second	300	300	2000	2400	1800	1800	20 char/sec	20 char/sec
SERIAL or PARALLEL	Serial	Serial	Serial	Serial	Serial	Serial	Parallel	Parallel
CHANNEL TYPE	Voice	Voice	Voice	Voice	Voice	Voice	Voice	Voice
NUMBER of WIRES	2	2	2/4	2/4	2/4	2/4	2	2
SYNCHRONOUS or ASYNCHRONOUS	Async.	Async.	Sync.	Sync.	Async.	Async.	Async.	Async.
SIMPLEX or DUPLEX	Full Duplex	Full Duplex	Half/full Duplex	Half/full Duplex	Half/full Duplex	Half/full Duplex	Transmit Only	Transmit Only
PRIVATE LINE MANDATORY?	No	No	No	Yes	No	No	No	No
AUTOMATIC CALL UNIT?	Optional	No	Yes	Optional	Optional	Optional	No	No
MODULATION SCHEME	Frequency shift	Frequency shift	Phase shift	Phase shift	Frequency shift	Frequency shift	3 of 14 code 99 poss. char.	3 of 14 code 99 poss. char.
COMMENTS	Directly compatible with Bell 103A	Directly compatible with Bell 103F	Directly compatible with Bell 201A	Directly compatible with Bell 201B	Directly compatible with Bell 202C	Designed for operation with Western El. 804	Compatible with Bell 401E; works end-end Bell 401J	Compatible with Bell 401H; works end-end Bell 401J
PURCHASE COST*	$580	$535	$2055-2110	$2130-2200	$1035-1320	$790-1015	$234-254	-----

*Cost data is approximate. Prices vary with configuration and options.

For additional information on products listed, circle 159 on inquiry card.

TABLE V TARIFFS FOR COMMON CARRIER SERVICES

COMMON CARRIER	TYPE OF SERVICE	BANDWIDTH or NOMINAL SPEED	TARIFFS* (Dollars)	COMMENTS
AT&T BELL SYSTEM	TWX dial network	100 words per min.	$1.75 first three minutes 0.60 each additional min. for 2000 miles and over 0.20/min. for 0–50 miles	Charges vary with distance, three minute minimum charge
WESTERN UNION	TELEX dial network	66 words per min.	From $0.175 to 0.60/min. depending on areas. 40% discount on excess if charges exceed $87.50/mo.	No 3 minute min. charge, fractions of min. are propor. charged.
AT&T and WESTERN UNION	Private line services low-speed	60, 75 words/min.	$1.10/channel-mile/month for half-duplex $1.21 for full-duplex	Charges are telescopic, reduce to half after 250 miles and third after 1,000 miles
		100 words/min.	$1.21 for half duplex, 1.331 for full duplex	
		sub-voice 150-180 bps	1.375 for half duplex, 1.513 for full duplex	
AT&T BELL SYSTEM	Public telephone network, dial exchange	voiceband 3000 bps	$1.00 to $2.00/three min. 0.25 to 0.50 each add'l. min. for 2,000 mi. and over $0.30/three min. and 0.10 each add'l. min. for up to 30 mi.	charged by time and distance 3 minute min. charge for call.
	WATS unlimited service	voice network 3,000 bps	$2,300/month for anywhere in USA for unlimited time. $ 500/month for Area 1	cost depends on service areas and the state.
	WATS measured service	voice network 3,000 bps	$610/month for first 15 hours, $34 each add'l. hour for anywhere in USA	cost of service lower for indiv. areas, varies.
WESTERN UNION	BEX Broadband Exchange	2 kc/s	$0.15/minute to $0.65/min. 40% discount on excess of $3000	Rates depend on areas, charges are broken down to tenths of a minute
		4 kc/s	$0.20/minute to $0.75/min. 40% discount on excess of $400	
AT&T and WESTERN UNION	voice-grade leased lines	4KHz	$2.02 for half duplex $2.22 for full duplex (channel-mile/month) $10, $37.50, and $56. channel condition charges for schedule 4A, 4B, and 4C respectively	rates are telescopic drop by approx. 15% after 250 mi. and 25% after 500 miles.
AT&T	TELPAK A	48 kc/s	$15/mile/month	12 voice channels
	TELPAK B	96 kc/s	20/mile/month	24 voice channels
	TELPAK C	240 kc/s	25/mile/month	60 voice channels
	TELPAK D	1,000 kc/s	45/mile/month	240 voice channels

*These are approximate tariffs currently available and may change. Check with your local common carrier representative.

TABLE VI MAJOR CHARACTERISTICS OF ACOUSTIC COUPLERS

MANUFACTURER	ANDERSON–JACOBSON	ANDERSON–JACOBSON	ANDERSON–JACOBSON	COMPUTER COMMUNICATIONS	DATA COMMUNICATIONS SYSTEMS	DATA COMMUNICATIONS SYSTEMS
MODEL	ADC-260	ADC-270	ADC-1210	CC-302	DAC-337	DAC-347
TRANSMISSION						
Speed bits/sec	300	300	1200	300	165	165
Simultaniety	Half or full duplex	Half or full duplex	Half duplex	Half or full duplex	Half or full duplex	Half or full duplex
Code	any	any	any	any	any	any
COUPLING						
Transmit	acoustic	acoustic	acoustic	acoustic	acoustic	acoustic
Receive	acoustic	acoustic	acoustic	inductive	acoustic	acoustic
COMMENT	originate only	answer only	originate only; reverse control chan., 202C compat.	originate only	originate only	originate and answer
COST						
Purchase	$570	$645	$795	$600	$495	$560

MANUFACTURER	GENERAL ELECTRIC	GENERAL ELECTRIC	OMNITECH	OMNITECH	TYMSHARE
MODEL	TDM 114	TDM 115	Telecoupler 700	Telecoupler 723	Mark V
TRANSMISSION					
Speed bits/sec	300	300	500	500	300
Simultaniety	Half or full duplex	Half or full duplex	Half or full duplex	Half or full duplex	Half or full duplex
Code	any	any	any	any	any
COUPLING					
Transmit	acoustic	acoustic	acoustic	acoustic	inductive
Receive	acoustic	acoustic	acous. or induc.	acous. or induc.	acoustic
COMMENT	originate only	originate and answer	originate only	originate only	originate only
COST					
Purchase	$495	$595	$495	$570	$570

*All data sets employ frequency shift keying and serial by bit asynchronous transmission and couple the data terminal (via EIA standard RS232B interface) to the public telephone network using a conventional telephone set (Bell 500 telephone set or equivalent).

For additional information on products listed, circle these numbers on inquiry card:

ANDERSON-JACOBSON 160
COMPUTER COMMUNICATIONS 161
DATA COMMUNICATIONS SYSTEMS 162
GENERAL ELECTRIC 163
OMNITECH 164
TYMSHARE 165

[illegible]

Ivor Catt

Computer Technology Ltd.
Hertz, England

When the output of a logic gate (Fig. 1) switches from false to true, it raises the voltage difference between the output pin of the gate and the reference through a voltage, v, which is called the signal amplitude of the gate. It is important to think of the signal as being a differential mode signal between the front end of the signal line and the reference, which serves as the return path. This reference might be called "ground". This change in voltage difference between the signal and reference lines does not appear instantaneously at the point further down the signal line because there is capacitance between the signal and reference lines. This means that before the new logic level (voltage difference) can be established between the signal and reference lines at all points, an amount of charge $+q$ must have been delivered by the gate to the signal line, and an equal and opposite charge must have been removed from the reference line by the gate, where

$$q = cv,$$

c being the capacitance between the signal line and the reference line. We might suppose that if the logic gate could instantaneously deliver that amount of charge $(+q)$ to the signal line and remove it from the reference line, the signal would appear without delay at the far end. Unfortunately this is not so, because of inductance.

We know that movement of electrical charge is accompanied by the appearance of magnetic flux. Change of the rate of flow of electric charge down the line, (which is necessary if we are to suddenly transfer a charge ϕ to the line) involves change of flux, $\frac{d\phi}{dt,}$ which by Faraday's law creates an induced back electro-motive force which tends to oppose the change of current. So if we try to introduce a charge $+q$ instantaneously into the line, we get an infinite $\frac{d\phi}{dt}$ and so an infinite back emf.

This means that in order to drive the voltage drop between signal line and reference line through a voltage change v instantaneously, we would need an infinite driving voltage for a short time to overcome the back emf.

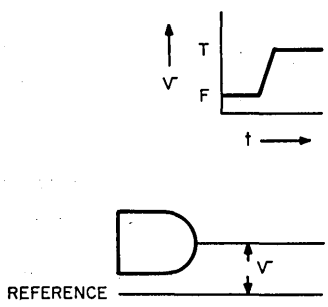
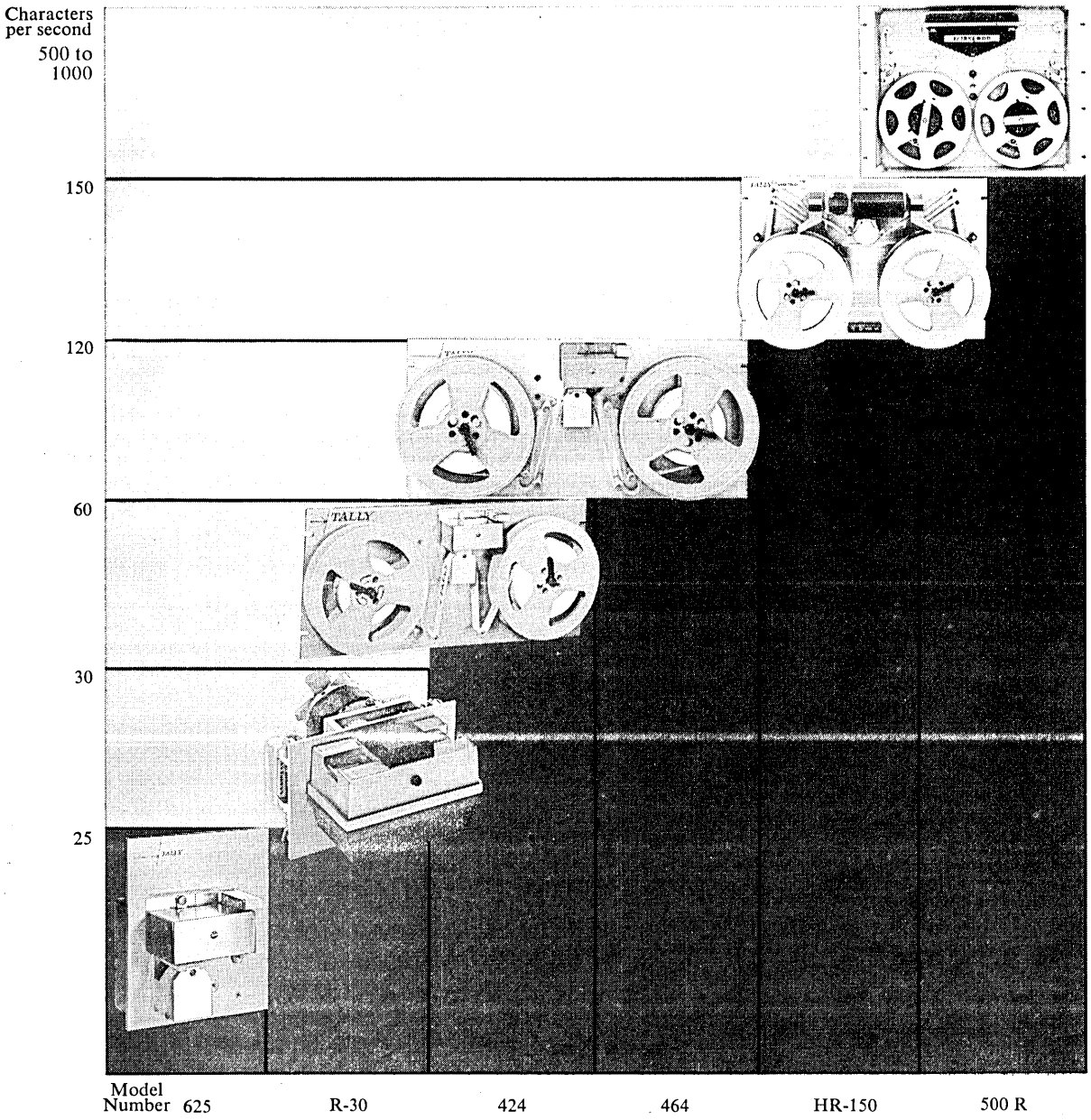


Fig. 1. Output from logic gate



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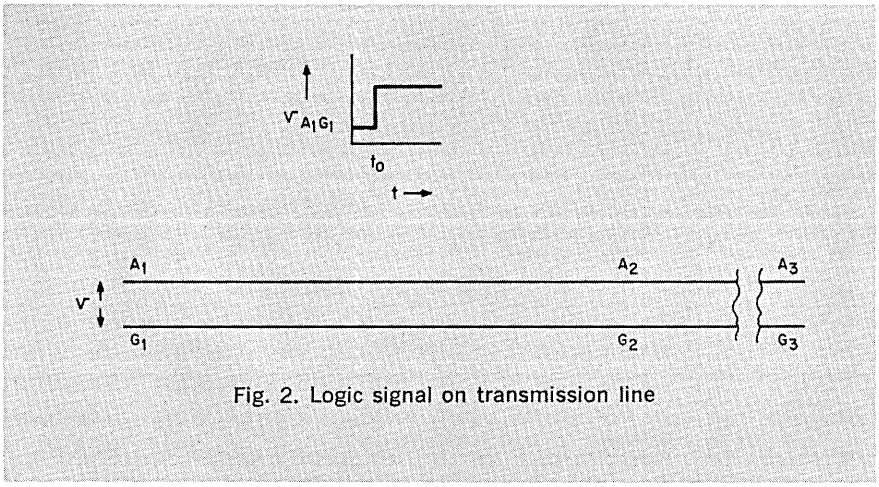


Fig. 2. Logic signal on transmission line

Alternately the signal cannot travel instantaneously because as the electric charge travels down the line, energy appears around the line in the form of magnetic and electric flux. By the principle of energy conservation this energy must have been supplied by the only available source, the logic gate. Now the gate can ideally supply voltage and current instantaneously. However, *vi* makes power but not energy. Power requires a third dimension, time, to give the full dimensions of energy, *vit*. So in the absence of infinite voltage or current, time is necessary for the signal to develop throughout the length of the signal line.

Note that in the above discussion the geometry of signal wire and reference was not specified.

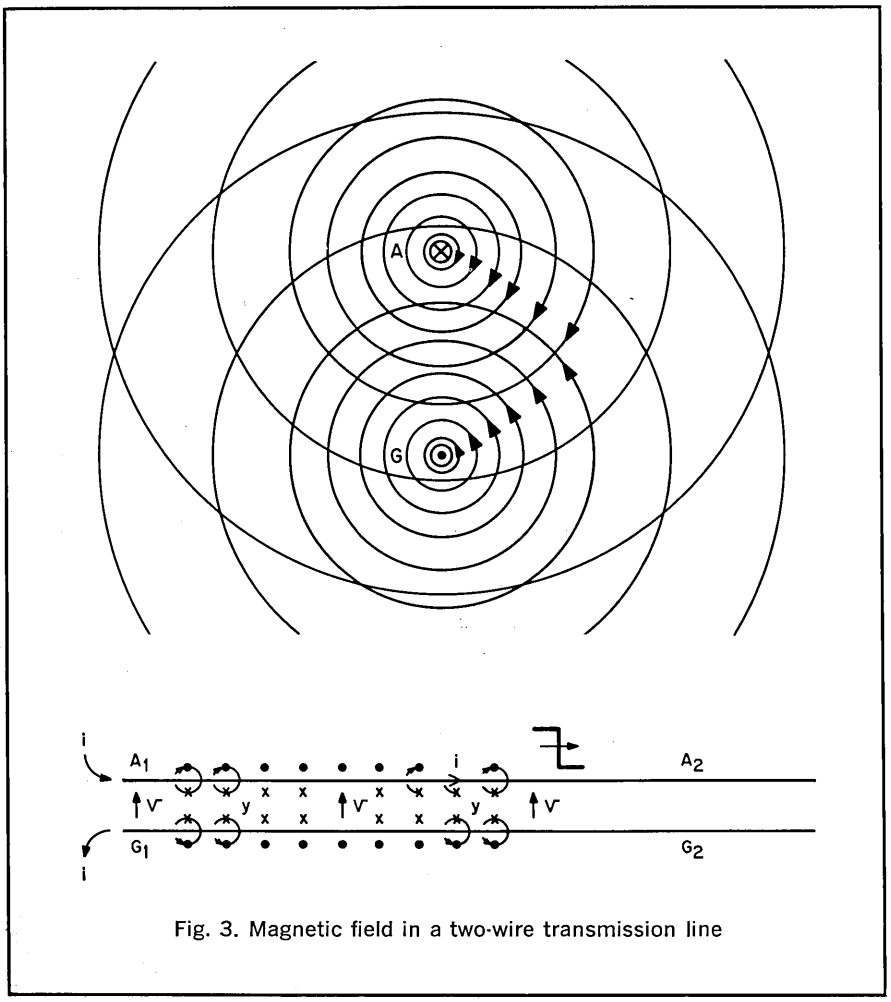


Fig. 3. Magnetic field in a two-wire transmission line

Logic Signal Transfer Down A Uniform Transmission Line

Let us assume that a logic swing v is introduced at A_1G_1 between the signal line A and the reference line G (Fig. 2), at time t_0. We can expect the logic swing to propagate down to the right, so that later in time (t_1) the signal has reached a point A_2G_2. Let us suppose that the capacitance per unit length between A_1A_3 and G_1G_3 is C. This means that if a steady potential difference v existed between the lines the charge on each line would be $(q) = Cv$ per unit length.

Let the self inductance per unit length of the pair of lines A_1A_3 and G_1G_3 be L. The L term means if a steady current $+i$ were flowing down A_1A_3 and a steady current $-i$ were flowing back along G_1G_3, the magnetic flux passing through a surface $A_1A_3G_3G_1$ bounded by the two wires would be $\phi = Li$ per unit length of the pair of lines.

Since the cross-sectional geometries and the surrounding dielectric of the pair of lines AG do not vary along their length, it is reasonable to assume that the signal travels at a constant velocity c. We know that the impedance which the pair of lines AG presents to an impressed signal V_{A1G1} is not infinite, so there must be current as well as voltage contained in the signal. If a current $+i$ is flowing down line A and a current $-i$ is flowing back along line G, we have a magnetic flux field as shown in Figure 3, and this results in a net flux passing between the pair of lines AG. Then in time $\triangle t$, the signal will have traveled a distance equal to $c\triangle t$, and the flux passing through the surface $A_1A_3G_3G_1$ will have increased by

$$\triangle\phi = Lic\triangle t. \qquad (1)$$

Now Faraday's Law of Induction says that if the flux through a loop increases steadily at the rate $\triangle\phi/\triangle t$, an emf is induced equal to $-\triangle\phi/\triangle t$. By Lenz's law, (*"Physics,"* by Hausmann–Slack Van Nostrand, p. 381) this opposes the original signal, and it can be called a back emf. Apart from the original signal v introduced across A_1G_1, this back emf is the only voltage around the loop $A_1A_3G_3G_1$. By

Kirchoff's Second Law, the sum of the voltages around the loop equals zero.

Impressed voltage v + back emf = 0

$$v + \left(-\frac{\triangle\phi}{\triangle t}\right) = 0$$

$$\therefore v = \frac{\triangle\phi}{\triangle t} = Lic \text{ from Eq. (1).}$$

This gives us the first important relationship between voltage, current and velocity.

$$\frac{v}{i} = Lc \qquad (2)$$

The second relationship will be derived from the Principle of Conservation of Charge. We know that a current i is entering the line A at A_1. So in time $\triangle t$, the total charge in line A_1A_3 will have increased by an amount $q = i\triangle t$.

During time $\triangle t$, the signal will have advanced a distance equal to $c\triangle t$, and this new section of line will have been charged up through a voltage v.

The charge absorbed
= capacitance × voltage
= capacitance per unit length × distance × voltage
$= C\,c\triangle t v$

By the principle of conservation of charge this must equal the charge introduced into the line, $i\triangle t$.

$$\therefore i\triangle t = C\,c\triangle t v \qquad (3)$$

This gives us the second important relationship between voltage, current and velocity:

$$\frac{v}{i} = \frac{1}{Cc} \qquad (4)$$

Now if we divide equation (2) by (4) we eliminate v and i, and find that

$$c = \pm\frac{1}{\sqrt{LC}} \qquad (5)$$

This means that all signals, whatever their amplitude, travel at the same velocity,

$$c = \frac{1}{\sqrt{LC}}$$

If we multiply (2) by (4) we eliminate c to get

$$\frac{V}{i} = \pm\sqrt{\frac{L}{C}} \qquad (6)$$

This means that the ratio between v and i is a constant for the line. This constant has been called the Characteristic Impedance, Z_0 of the line.

REFERENCES

1. S. Ramo, J. R. Whinnery and T. Van Duzer, *Fields and Waves in Communication Electronics,* New York, Wiley, 1965.

2. I. Catt, "Crosstalk (Noise) in Digital Systems," IEEE Trans. Electronic Computers, vol. EC-16, pp. 743-763, Dec. 1967.

APPLICATION NOTE

D/A Signal Conversion Using Digitally-Controlled Power Sources

Hewlett Packard Co.
Berkeley Heights, N.J.

Digitally-controlled power sources (DCPS's) are complete digital-to-analog links between a computer (or other digital source) and any application requiring a fast, accurately settable source of dc or low-frequency ac power. Initially these applications may be thought of as requiring a digital-to-analog converter with augmented output power capability, a digitally-controlled power supply, or a digitally-controlled waveform synthesizer.

However, such applications generally require more than a programmable power supply or the simple tandem combination of a D/A converter and an operational amplifier. Interface circuitry must be added to insure compatibility between the computer and D/A converter. Additional circuits required to complement the D/A converter include:

- reference and B+ sources
- isolation between input and output to avoid ground loops between the load ground and the computer main frame.
- internal storage to increase computer operating efficiency and eliminate programming overshoots
- programmable current limiting protection for the output power amplifier and the load
- feedback signals to inform the computer of the power source status

The name "digitally controlled power source" denotes a single compact package which includes interfacing, storage D/A conversion, bipolar power amplification, protection, digital feedback, and all necessary bias supplies. Models 6130B and 6131B DCPS's provide these functions:

All digital inputs are floating and isolated from the floating analog output, thus avoiding troublesome loops between the output ground and computer ground.

Inputs from all digital data lines are stored upon receipt of a gate signal from the computer; this stored information is provided as input to the D/A converter. Fifty-five microseconds after the gate, a flag signal informs the computer that enough time has elapsed for the commanded output voltage level to be achieved. The output level will be maintained until a new gate signal is received, leaving the computer free to perform other tasks in the interval between voltage level commands.

Storage also insures that non-simultaneous arrival of signals on all digital input lines will not cause programming overshoot or undershoot—this eliminates the necessity of programming the output to zero before setting each new output level.

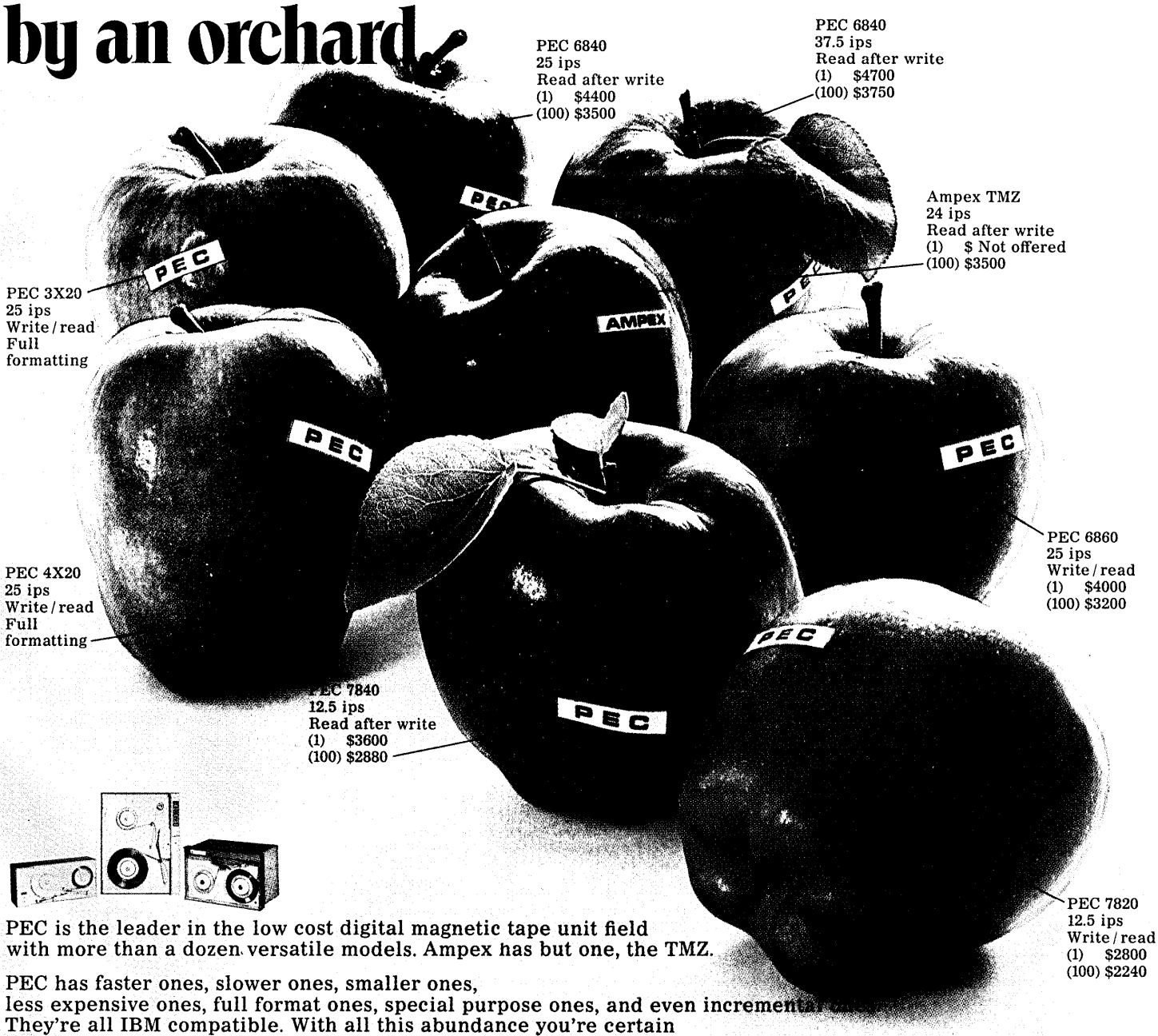
The D/A converter converts one polarity bit plus 16 BCD voltage bits or 15 binary voltage bits to an analog voltage for input to the power amplifier. Resolution is 0.5 millivolt for straight binary and 1 millivolt for BCD operation.

The bipolar power amplifier programs either side of zero or through zero without output polarity switches or "notch" effects, with an accuracy of 1 mV, 5 mV or 10 mV depending on the range and model. Model 6130B programs over ± 50 V @ 0-1A in less than 100 microseconds; model 6131B programs over ±100 V @ 0-0.5A in less than 200 microseconds.

The DCPS provides three feedback signals to the computer. The

When we started comparing apples to apples,

we found that one of them was surrounded by an orchard.



PEC is the leader in the low cost digital magnetic tape unit field with more than a dozen versatile models. Ampex has but one, the TMZ.

PEC has faster ones, slower ones, smaller ones,
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They're all IBM compatible. With all this abundance you're certain
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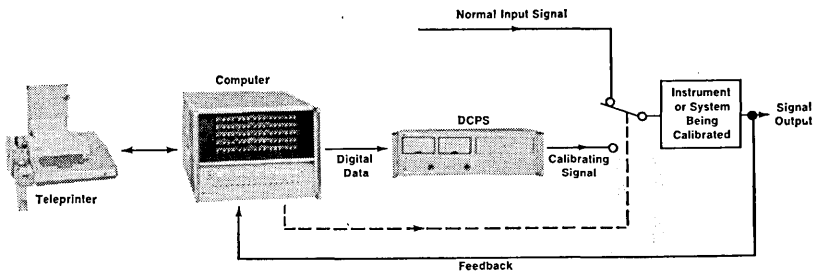
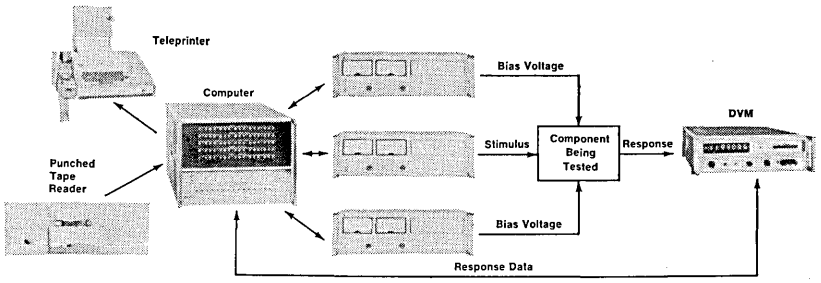


In this computer-controlled calibrator application the digitally-controlled power source (DCPS) is used to provide an automated source of calibrated dc or low-frequency waveforms



Computer-controlled test system for automated component and subassembly testing illustrates the use of digitally-controlled power sources to provide the required programmable voltages and stimulus to the device under test

first of these is a flag (completion of task) signal which occurs 55 microseconds after the input gate signal (2 milliseconds after input gate signal if range is changed) and informs the computer that the programmed level exists at the output. The remaining two bits send overload information through isolated data lines. Thus the computer is continuously informed of any current overload and power amplifier shutdown.

The application areas for DCPS's are practically unlimited—they are useful wherever digital signals must be converted to analog form with accuracy, precision, and a minimum of system interface complication. The digital input signals can be provided by a computer, tape reader, digital voltmeter, counter, external switch closures, etc. The output can be connected to any instrument or system requiring an analog source with power capability up to 50 watts.

Used in conjunction with a computer, a DCPS provides an automated source of calibrated dc or low-frequency waveforms. In the latter case, the waveshape can be designated on an exact point-by-point basis, with a computer specifying a new point every 50 μsec. In some applications, the DCPS output waveform is selected to be a staircase approximation of a sawtooth; the computer then analyzes the linearity of the system by comparing the output and input signals. In other cases a square wave or pulse output from the DCPS is used to calibrate the system gain and check the transient performance.

Computer/DCPS combinations are assuming greater significance because of the increasing thoroughness of systems testing requirements and the need for inexpensive high-speed calibration. Using a computer and a DCPS, system testing and calibration can be accomplished quickly during periods of inactivity or on a time-shared basis without interrupting system operation.

Other factors that contribute to the usefulness of the DCPS in calibration applications include:

- ease of interlacing between the computer and DCPS
- programming speed
- input/output isolation
- bipolar output – smooth propramming through zero

Moreover, the low-output impedance of the DCPS insures the integrity of its accuracy specification even in the face of substantial load current requirements.

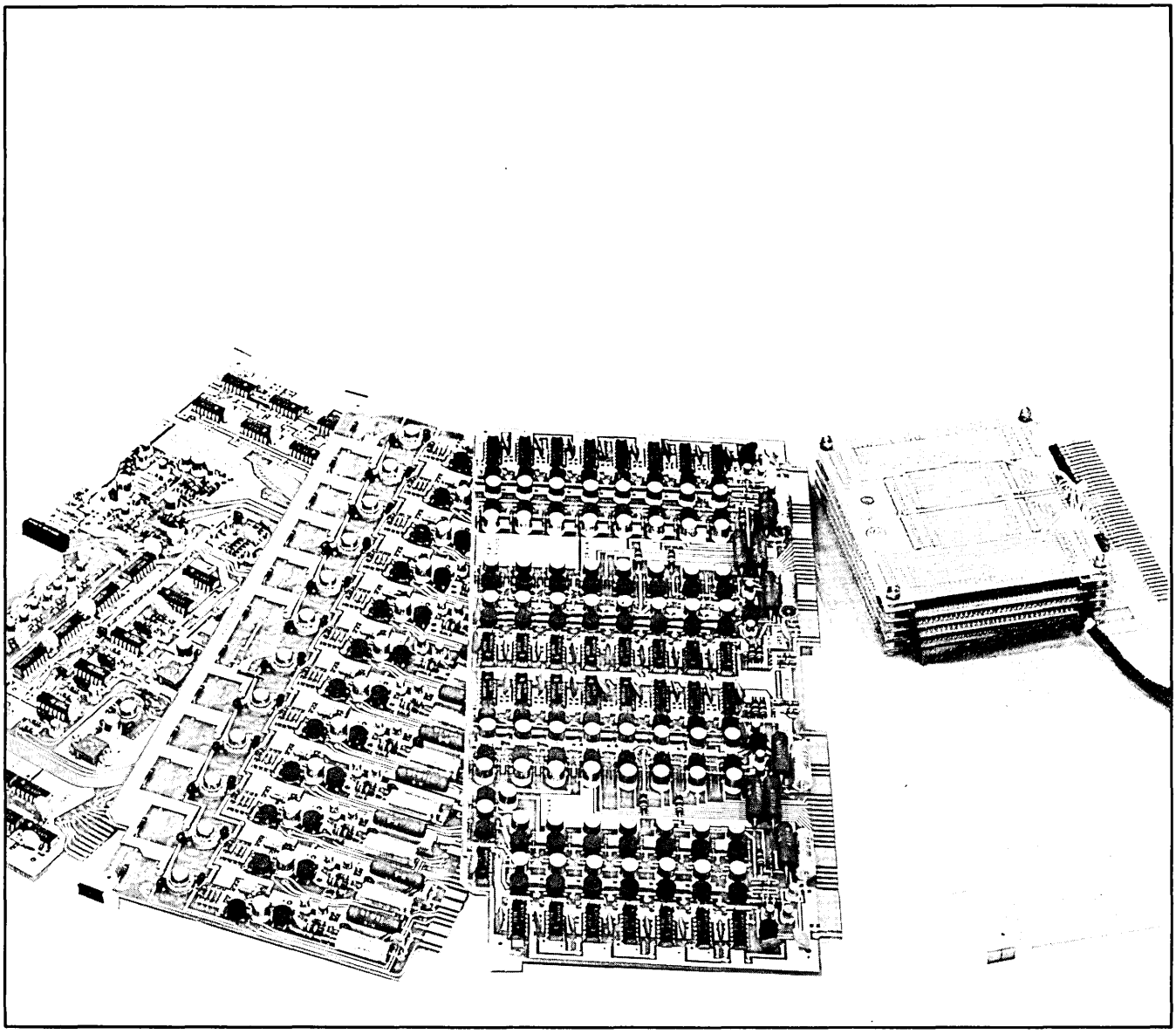
Computer-controlled test systems are finding increasing use in high speed testing and sorting of electronic components, particularly transistors and IC's, as well as larger electronic subassemblies.

In a typical system the computer is controlled either through manual keyboard entry, by previously prepared programs via a punch-tape reader, or from a program stored in computer memory. The number of DCPS's employed depends upon the number of programmable voltages required by the device under test. Used as a stimulus, the DCPS covers a frequency range from dc to 20kHz—particularly valuable in generating complex special-purpose waveforms, and very low frequency test signals below the range of conventional oscillators.

With high-speed testing systems, components can be checked more thoroughly and inexpensively. The DCPS possesses a unique combination of speed, accuracy, resolution, and power output capability, making it ideal for large volume production testing. Its internal storage permits rapid programming between voltage levels without programming to zero between each desired output level to avoid overshoots. The programmable current limit assures that delicate components can be tested and sorted nondestructively; two different current overload signals are fed back from the DCPS so that the computer can distinguish between a short-term or transient violation of the current limit value and a long-term or transient violation of the current limit value, and a long-term or static excess. The bipolar output plus the ability to sink as well as source current permits testing of active as well as passive devices.

In addition to manufacturing separate instruments for connection into an automated test system, HP also manufactures self-contained test systems employing the DCPS, an HP computer, and other instruments tailored to specific applications.

For additional information, circle 198 on inquiry card



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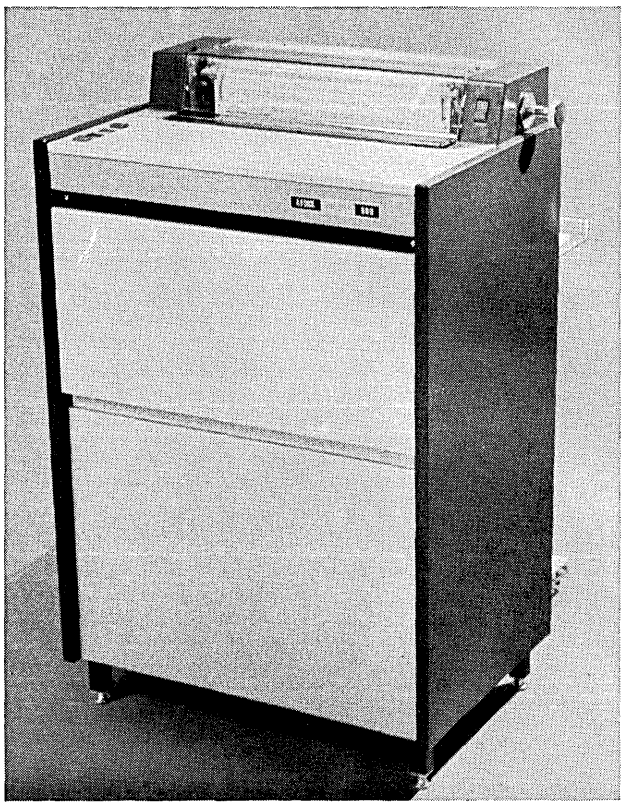
Communication/Data Processing Printer



A. B. DICK CO.
Chicago, Ill.

A quiet, high-speed communications printer built for remote printing via conventional voice-grade public-switched telephone lines has been developed by the A. B. Dick Company of Chicago.

Designated the Videojet 960, the product is a non-impact printer utilizing a stream of controlled ink droplets to print 250 characters per second on conventional business forms ranging in weight from 20- to 125-pound stock, in overall widths from 3½ to 14⅞ inches, using Videojet offset ink and continuous-form masters. The 960 can also direct image masters for reproductions requiring distribution.

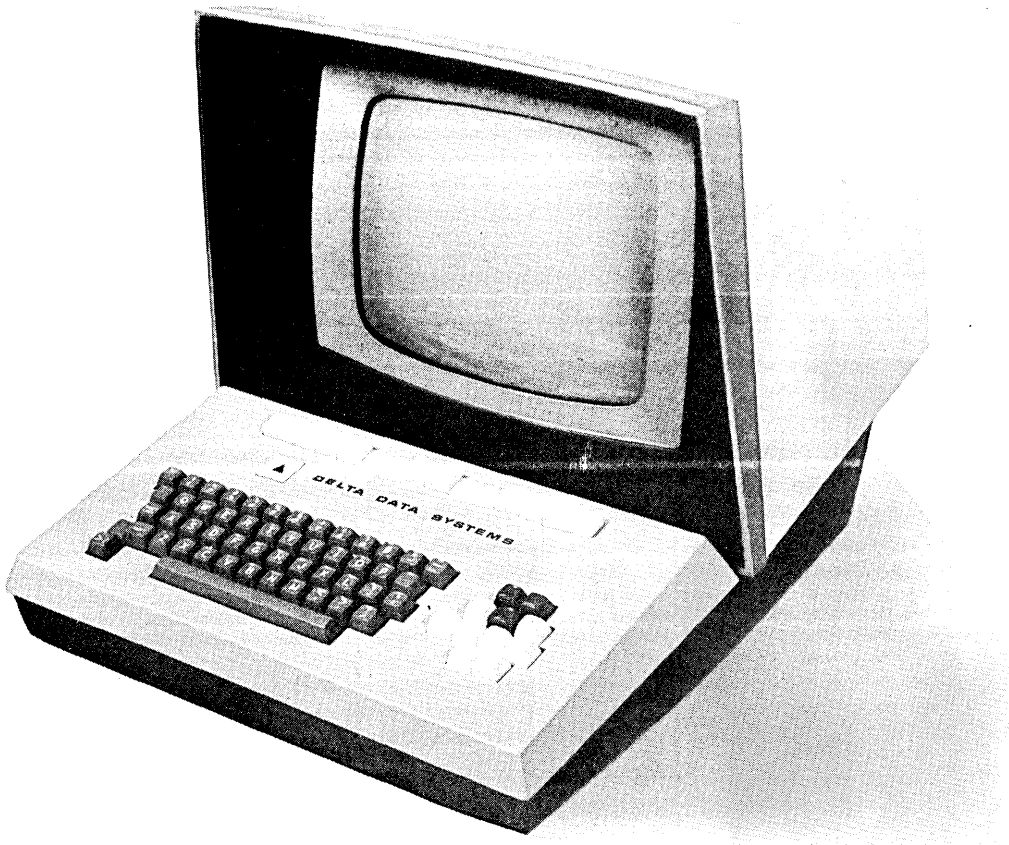
The 960 print rate, 25 times faster than most communications printers, is designed for data transmission in time-sharing networks; remote batch processing with local print requirements; message-switching systems; news wire services; and as a local line printer for use with small "mini" computers. It automatically answers the dataphone subset used in these systems, prints the information transmitted, and terminates the dataphone call—unattended.

Character spacing and line length are set to the industry norm of ten characters per inch and a line length of 136 characters. However, the character spacing is variable from five to fifteen characters per inch allowing up to 204 characters on a single line. It accommodates the 80-character line in communication networks.

Videojet 960's process is based on the principle that if fluid is forced through a nozzle it breaks up into droplets. The nozzle is subjected to a 66-kHz energy source which causes the droplets to be uniform in both size and spacing, a function of pressure at the nozzle, viscosity of ink, and diameter and vibration frequency of the nozzle. Each droplet may be given a precise electrostatic charge as it forms. The voltage present at the time the droplet breaks away from the ink stream induces the charge. Once it breaks, the charge is trapped—staying with the droplet until it reaches its destination. Because the droplets pass between a pair of high-voltage deflection plates, the charge of the droplet determines the precise path of travel and final position of the droplet on paper.

The nozzle is moved in a horizontal plane, driven by a servo-mechanism-controlled, high speed, low inertia motor. The movement of the nozzle provides horizontal deflection of droplets; the high voltage plates provide vertical deflection.

A 9- by 11-dot matrix is used in a character generation to determine the charges for droplets. The 99 dots of the 9 by 11 matrix correspond to 99 droplets. If each droplet were appropriately charged, the resulting character would be a rectangle 9 droplets wide and 11 droplets high. Only those droplets required to form a character are charged. Uncharged droplets are collected and returned to the ink reservoir for reuse. Recirculation of unused ink allows the system to print for forty hours using only one quart of ink.



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The maxi display. That's what we call DELTA 1. A ready-now display terminal for all the minis. Ready with a flexible, high-capacity party line I/O bus for minis like the HP 2116, DATA 620/i, PDP-8/I, INTERDATA Model 4, and NOVA. Think of the applications: scientific/engineering control, process control, automatic test systems, communications systems, graphic arts, and education. You can interface with a CRT display that has a lower cost/performance ratio than any other data display system.

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Delta Data Systems Corporation

Delta 1. The maxi display for the mini computers.

CIRCLE 34 ON INQUIRY CARD

NEW PRODUCTS

CRT DISPLAY

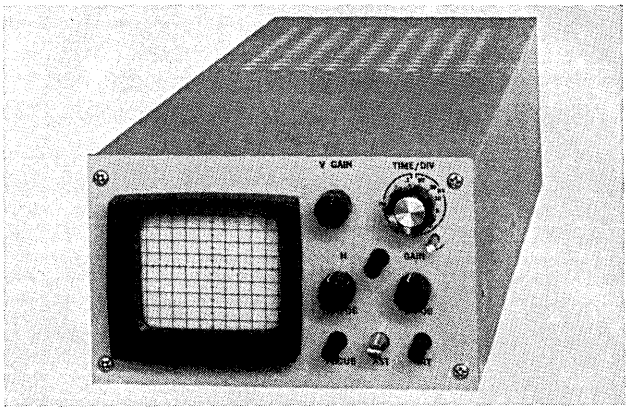
An ultra-compact CRT display series offers the flexibility of the general-purpose lab scope.

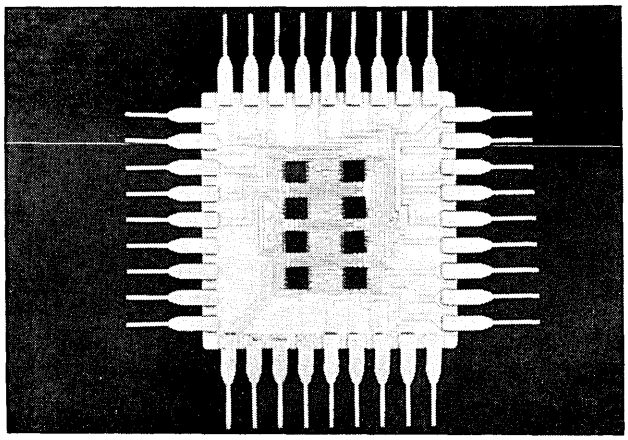
Model 8602 has eleven sweep ranges selectable by a front panel control. Panel size is 3½ by 5¾ inches with a 4- by 5-cm useful screen area. Sweep ranges are: 1 microsecond to 2 milliseconds per division, 10 μs to 20 ms, and 100 μs to 200 ms/div. Front panel signal attenuator is also available.

Model 8601 offers a choice of 18 single-range sweeps from 1 μs/div to 500 ms/div with 2.5:1 vernier.

Model 8601 is the basic x-y unit and may be fitted with front-panel controlled attenuators for both x and y channels. Deflection amplifiers are dc-coupled, high stability, all solid-state design. Indofex, Inc., Waterbury, Conn.

CIRCLE 200 ON INQUIRY CARD





RANDOM ACCESS MEMORY

A 128-bit read/write random access memory, featuring access speeds of 35 nanoseconds, is available in a 1-inch-square multi-chip package. The MμL4027 is a bipolar product with a ceramic substrate incorporating two layers of metallizied interconnects.

The device consists of eight 16-bit chips bonded face-down on the substrate. Memory organization is 64 2-bit words with uncommited collectors that allow easy word or bit expansion. The organization is simplified by eight X and eight Y coincident-select lines.

All outputs are compatible with current sinking logic such as DTL and TTL, with true and complement outputs available for each bit. Fairchild Semiconductor, Mountain View, Calif.

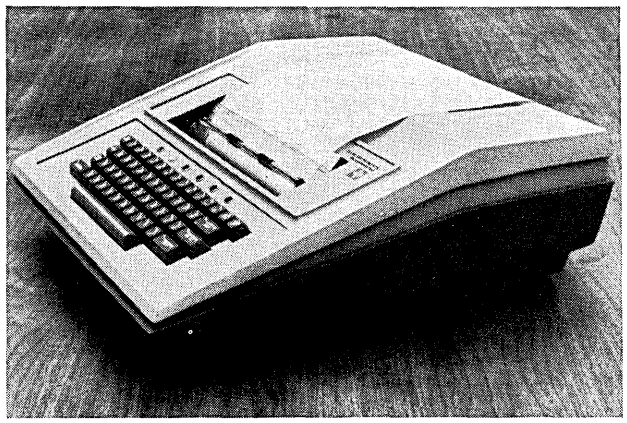
CIRCLE 201 ON INQUIRY CARD

HIGH-SPEED DATA TERMINAL

Series 720, Model 10 high-speed data terminal, utilizes a monolithic, solid-state printhead which produces characters on thermal-sensitive paper. The printer operates at rates up to 400 words per minute (40 characters per second).

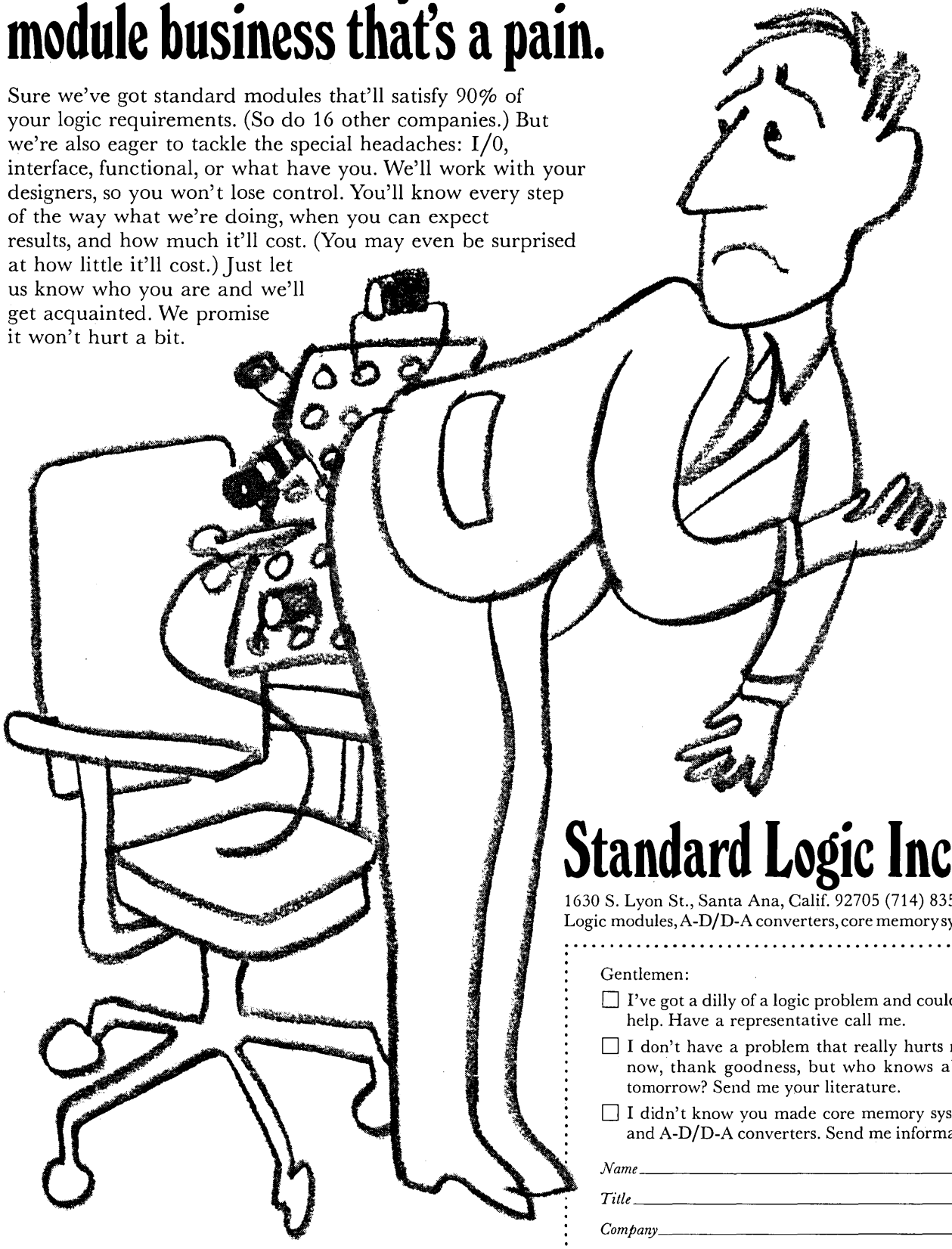
A self-contained buffer memory provides more efficient utilization of lines in multi-drop private-line data systems by allowing twice the number of terminals per line, giving full service to each terminal. The buffer retains up to 50 characters in memory before transmitting them at high speed. The Model 10 is also designed with electronics for multi-station computer terminal operations: It responds to polling, addressing or broadcasting by a CPU in a multi-station network. Texas Instruments, Inc., Industrial Products Div., Houston, Tex.

CIRCLE 202 ON INQUIRY CARD



We want the 10% of your module business that's a pain.

Sure we've got standard modules that'll satisfy 90% of your logic requirements. (So do 16 other companies.) But we're also eager to tackle the special headaches: I/O, interface, functional, or what have you. We'll work with your designers, so you won't lose control. You'll know every step of the way what we're doing, when you can expect results, and how much it'll cost. (You may even be surprised at how little it'll cost.) Just let us know who you are and we'll get acquainted. We promise it won't hurt a bit.



Standard Logic Inc.

1630 S. Lyon St., Santa Ana, Calif. 92705 (714) 835-5466.
Logic modules, A-D/D-A converters, core memory systems.

Gentlemen:

- ☐ I've got a dilly of a logic problem and could use help. Have a representative call me.
- ☐ I don't have a problem that really hurts right now, thank goodness, but who knows about tomorrow? Send me your literature.
- ☐ I didn't know you made core memory systems and A-D/D-A converters. Send me information.

Name _____

Title _____

Company _____

Address _____

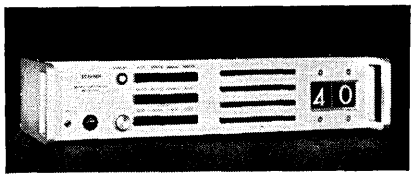
City _____

State _____ *Zip* _____

Area Code _____ *Phone* _____

CIRCLE 35 ON INQUIRY CARD

NEW PRODUCTS



RELAY SCANNER

Designed for use with thermocouples and strain gage systems requiring resolution in the microvolt range is a low-level, 3-wire reed relay scanner. Model 1700 provides 10 to 40 channels in a 3½-inch cabinet and can be expanded to as high as 2,000 channels with the addition of slave units.

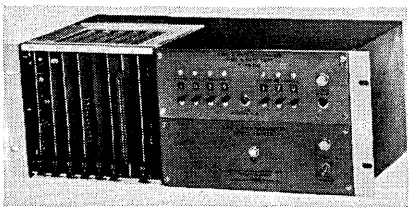
Individual channel selector push-buttons allow unlimited programming. Only the channels selected are scanned, while unselected channels are bypassed in zero time. Scanning rates ranging from 100 channels per second to one channel per 10 seconds are standard. Matrix Corp., Beech Grove, Ind.

CIRCLE 203 ON INQUIRY CARD

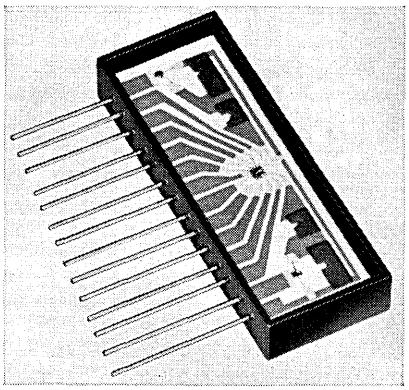
TIME AND DATE GENERATOR

The time and date can be produced in the form of machine-readable sequential signals into a TTY loop or as an optional EIA voltage by a time and date generator. For use with computer-switched teletypewriter communications systems, it offers a flexible method of input for time and date of message transmission. The code generator can also be pre-programmed for two 2-character responses for "answer back." The variable T and D sequence output may contain other fixed-character intelligence.

Code configurations are available for any 5- or 8-level system to generate standard Baudot or 1963 ASCII output with the eighth pulse marking, as well as other codings, such as ASCII odd or even parity, 1966 ASCII, or IBM. Pioneer Electric & Research Corp., Forest Park, Ill.



CIRCLE 204 ON INQUIRY CARD



HYBRID IC MODULES

MCH1002 dual power driver hybrid microcircuit is the first in a series of off-the-shelf hybrid IC modules designed for interfacing high-threshold logic levels with electromechanical hardware. Composed of an expandable dual four-input line driver; two separate high-current, high-voltage discrete switching transistors; and four thick-film resistors, the MCH1002 features a maximum output current of 0.5A; a collector-emitter breakdown voltage of 40V minimum; a typical turn-on time of 115 ns; and typical turn-off time of 260 ns. It is encapsualted in a 14-lead, molded plastic plug-in package.

Also available is the MCH2005 Darlington power driver, housed in the TO-91, 10-lead ceramic flat package. At current gains greater than 1,000, the MCH2005 can convert the TTL output current level of 5 mA into a Darlington output current pulse of 5A—more than adequate to drive high-current ferrite switches used in phaseshifter or phase-array-radar designs, with a total switching time of only 800 ns. Motorola Semiconductor Products, Inc., Phoenix, Ariz.

CIRCLE 205 ON INQUIRY CARD

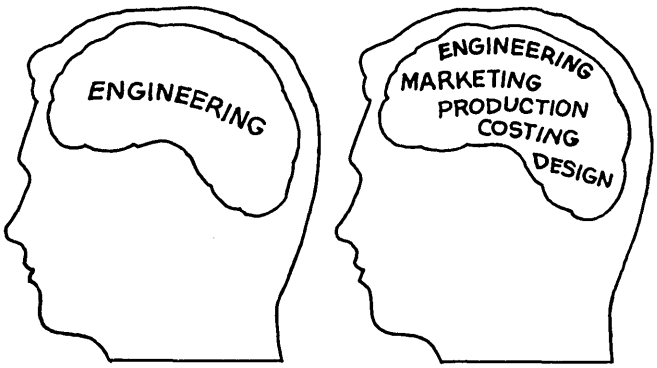
PERMANENT-MAGNET DC MOTOR

A 33-Frame (3¼-inch OD) permanent-magnet fractional-horsepower dc motor is available, in the standard length of 5⅞ inches. Armature windings may be varied by specification to meet application needs, making the motor operable at any desirable voltage with speeds up to 5,000 rpm.

Features include high current capability, long life brushes, double shielded precision ball bearings, Class 155 insulation, four permanent field magnets, stainless steel shafts and welded armature connections. Indiana General Corp., Electro-Mechanical Div., Oglesby, Ill.

CIRCLE 206 ON INQUIRY CARD

Ordinary engineers have their place. Elsewhere.



ORDINARY ENGINEERS OUR ENGINEERS

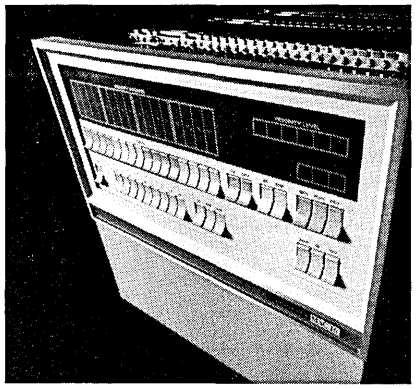
Ordinary engineers are the guys who sit in somebody's bullpen and slave away on a tiny part of some immense project. Doing the same kind of thing. Over and over, without ever really knowing what their contribution amounts to.

We go about things a little differently. And we think that's the reason we've become a leader in computer memories.

Our technique is to let engineers get involved in as many different activities as they can handle. Technical proposals, design, development, costing, production, marketing, planning—you name it, our engineers get involved in it. And the involvement leads to commitment. It's worked out beautifully.

As a result we have a busy and extremely interested engineering staff. And the finest line of memory systems and stacks and interconnect circuitry on the market.

It should surprise no one to learn that we're growing at a healthy clip. Just recently, we introduced our new digital Multi-Application Computer —MAC 16 —and that's going to accelerate our growth.



So, we need more engineers. Good minds. Good technical backgrounds. And the desire to get involved.

We pay well. And, because of our continuing growth, we offer rapid advancement.

If you're interested in us and you've got an M.E. or E.E. and E.D.P. hardware or software experience, let's get together.

Write to me—E. A. Gage—at 6201 E. Randolph Street, Los Angeles, California 90022. Better still, call collect. (213) 722-6810. Naturally, we're an equal opportunity employer.

LOCKHEED ELECTRONICS COMPANY

LEC Data Products Division • A Division of Lockheed Aircraft Corporation

CIRCLE 900 ON INQUIRY CARD

NEW PRODUCTS

DIGITAL ANGLE INDICATOR

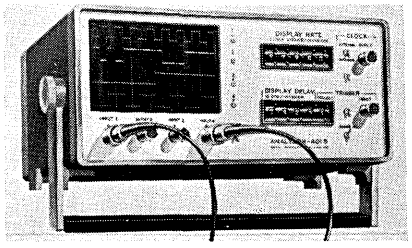
An electronic instrument has been developed for measuring and displaying angular inputs from applied synchros or resolvers—the solid state digital angle indicator.

A visual readout displays the input angle on 1-inch character nixie tubes providing higher visibility and better readability than the normal servo drum dials. To drive printers and other off-line equipment, a four-decade BCD digital output is available without adding an encoder. The digital angle indicator will accept synchro or resolver inputs at 11.8, 26, or 90 volts line-to-line. Astrosystems, Inc., New Hyde Park, N.Y.

CIRCLE 207 ON INQUIRY CARD

MULTI-CHANNEL ANALYZER

A portable multi-channel digital system analyzer which provides fast, positive analysis and evaluation of digital equipment and systems, measures both the direction and spatial or temporal position of signals in transition from one logic level to another. Multiple traces are displayed simultaneously in different colors. Display timing is derived from the external system clock; hence the rate is inherently stable. Display rate is variable from 1 to 99,-999 intervals of 10 display divisions. Data Display Systems, Willow Grove, Pa.



CIRCLE 208 ON INQUIRY CARD

SCHOTTKY SWITCHING DIODE

A triple-barrier Schottky switching diode, the MA4-A200, is a planar passivated silicon diode, utilizing a unique combination of two Schottky barriers and a p-n junction. The diode has the high breakdown voltage (> 25 volts) and operating temperature characteristics of silicon, combined with the low turn-on voltage of germanium and the ultra-fast speed of a Schottky barrier device.

The MA4-A200 is recommended for pulse and analog applications. The diode is suited to pulse and digital circuits for clamping, clipping, speed-up, steering and sampling. Microwave Associates, Inc., Sunnyvale, Calif.

CIRCLE 209 ON INQUIRY CARD

POWER TRANSISTORS

Fast switching 5.0-amp power transistors with turn on time less than 10 nanoseconds, designated the SDT6100 series, are packaged in the TO-5 case.

Typical characteristics are: V_{CEO} = 40 volts, h_{FE} @ 2.0 amp = 20 to 60; V_{CE} (SAT) = 1.5 volt max; t_E @ 2.0 amps = 10 nsec max; and I_c max = 5.0 amps.

The devices have a total switching time of less than 60 nanoseconds and rise time of less than 10 nanoseconds. They feature planar construction and are typically f_T = 500 MHz. Solitron Devices, Inc., Riviera Beach, Fla.

CIRCLE 210 ON INQUIRY CARD

SYNCHRO REPEATER

The size 11 dc synchro repeater, CR4 0928 001, is designed for use as a torque repeater in displays operating directly from sources such as digital or pulse analog computers. The component functions when its two stator windings are energized by dc voltages proportional to the sine and cosine of an angle, causing its permanent magnet rotor to orient in the resultant field to an equivalent angular position. Since the device is a dc equivalent of a conventional ac synchro torque repeater, it can simplify repeater-indicator displays for A/D and D/A conversion and digital computer applications by utilizing digital pulses directly, thereby eliminating the need for more complex and costly ac instrumentation. Singer-General Precision, Inc., Kearfott Div., Little Falls, N.J.

CIRCLE 211 ON INQUIRY CARD

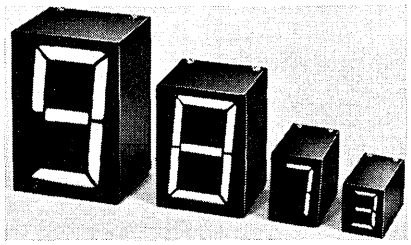
NEW PRODUCTS

NUMERIC DISPLAY SYSTEMS

Three module sizes, 3, 4, and 5-inch, have been added to a line of bulbless C-Rite numeric displays.

The C-Rite is the only 7-bar system capable of producing information up to 5 inches.

The system is available in white or fluorescent, colored, seven-segment display. Unlimited life and reliability is assured using a teflon-suspended balanced rotor magnetic drive system. A self-latching memory insures fail-safe performance and low power consumption. James Electronics Inc., Components Div., Chicago, Ill.

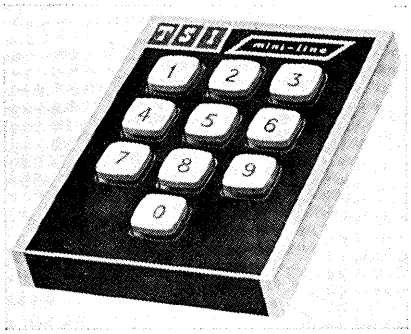


CIRCLE 212 ON INQUIRY CARD

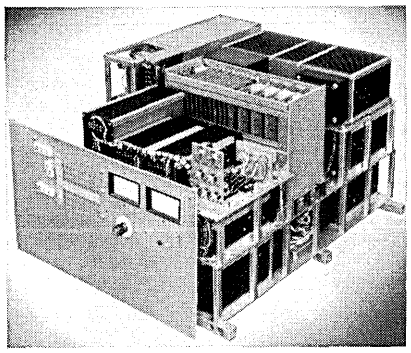
MINIATURE KEYBOARD

A miniature solid-state numeric keyboard, measuring less than 4 inches wide and ½ inch thick, utilizes new infinite-life proximity keys to achieve 100% reliability.

The Mini-Line keyboard is designed for limited space applications. Its ten keys operate with non-contacting proximity transducers, a feature which eliminates key bounce, resultant mechanical wear, and the need for anti-bounce circuitry. Up to eight outputs from single keys eliminate the need for diode matrices. Transducer Systems, Inc., Willow Grove, Pa.



CIRCLE 213 ON INQUIRY CARD



MEMORY POWER SYSTEM

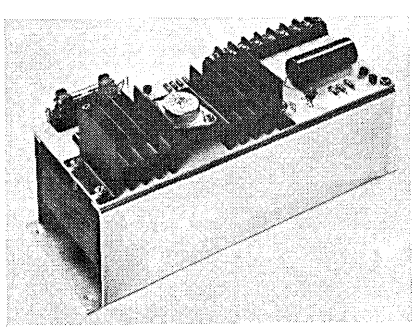
A dc power system used to power thin film memories provides ten separate active outputs and three auxiliary outputs, with the active outputs regulated at ±0.5% with current limiting adjustable from 20 to 110%. Output ratings range from 1,800 to 7 watts. Each output has built-in overvoltage protection and all are adjustable for either ±10% or ±20% of their nominal levels.

The logic enables the system to turn on or off in proper sequence in response to a single computer input; to shift the levels of the ten outputs up or down, all in the same direction or mixed; and to signal the computer when an over or under voltage level has been exceeded. Rowan Industries, Inc., Electronic Measurements Div., Oceanport, N.J.

CIRCLE 214 ON INQUIRY CARD

MULTI-PURPOSE POWER SUPPLY

The PM728 is a compact (3.0-inch by 3.7 by 8.4-inch overall), low-cost regulated dc power supply, using all silicon semiconductors, designed primarily to provide power for digital integrated circuit applications. The output of the PF728 is adjustable from 4.8 to 6.3 Vdc @ 3 amps and will operate from 115 Vac, ±10 at 60 to 400 Hz. Line and load regulation is ±0.05% each and ripple and noise is less than 1.0 mV RMS. Computer Products, Inc., Fort Lauderdale, Fla.



CIRCLE 215 ON INQUIRY CARD

SYSTEMS ENGINEERS

Foxboro offers promising careers/ not a career full of promises.

Our computer control systems aren't just on the boards, they're in use, right now, and more of them are on the way. They're available as standard hardware and software systems or as applied systems, offering unequalled control and supervisory capabilities. They're being used in refinery, power, cement and steam cracking ethylene plants today — and more are on the way.

This proven ability to deliver on promise applies to Foxboro career opportunities, too. You'll work with some of the most experienced and talented professionals in this field. You'll be part of a world-wide organization that offers you the twin advantages of sixty years' technical leadership and a modern management team.

SYSTEMS APPLICATION DEVELOPMENT ENGINEERS

To work in a research and development atmosphere with optimization techniques, (including linear and non-linear programming), math modeling of process units, plant scheduling control strategies, command control packages, and joint customer-Foxboro development studies. These positions offer an unparalleled opportunity to check development results against "real-world problems". Experience in a process industry or design and construction company, and an M.S. degree in chemical or petroleum engineering is desirable.

SYSTEMS ENGINEERS

As a technical design leader of complex digital projects, you will utilize your systems skills in both hardware and software, as well as analysis and applications for the process industries. Discharging these responsibilities demands leadership qualities, communications skills, planning and scheduling capabilities. A degree in engineering with a minimum of five years' experience in instrumentation, process control and on-line computer applications is desired.

SYSTEMS ANALYSTS

We are looking for candidates with a minimum of three years' process experience in the chemical, petro-chemical, pulp and paper or textile industries who can relate process requirements in terms of a digital control system. This experience should include instrumentation and unit operations, coupled with some digital computer background. The work is in a project team environment interfacing with design, programming and customer personnel. B.S. or M.S. degree in chemical engineering is preferred.

SYSTEMS PRODUCT DEVELOPMENT ENGINEERS

You will have overall technical responsibility for the functional design of major product improvements, make key decisions concerning hardware/software trade-offs and contribute to the influence of future Foxboro products. As a member of an *operating* division, you will critically review, comment on, and influence corporate new product designs from a user's point of view. Capabilities to interface with Corporate Development and Marketing personnel is an essential requirement. A B.S. or M.S. degree in Engineering with a minimum of three years' experience in a process industry or computer vendor's organization is desired. Experience should include: digital equipment or program development, customer sales order engineering or participation on a user's digital process control system project team.

Interested individuals should call (617) 543-8750, collect, or write to Tom Bryant, The Foxboro Company, Professional Placement Office, Dept. CD7, Neponset Avenue, Foxboro, Mass. 02035. Foxboro is an equal opportunity employer.

FOXBORO®

CIRCLE 902 ON INQUIRY CARD

NEW PRODUCTS

HIGH TORQUE STEP MOTOR

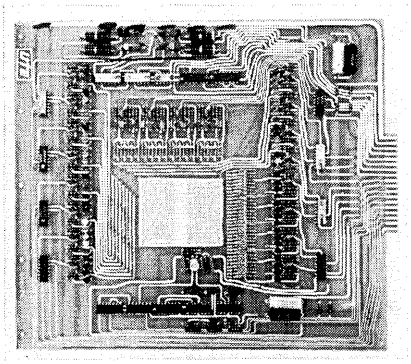
Sequentially switching multiple circuits and at the same time remotely positioning loads in 30°-increments is a 12-position stepping motor. The motor has a breakaway torque of 130 ounce-inches and can drive a constant friction load of 56 ounce-inches. Units are available for both unidirectional and bidirectional positioning. Shaft extensions on both ends permit direct coupling for driving two loads simultaneously. A knob can be added for visual position indication or for manual positioning in either direction.

Positioning accuracy of ±1°, non-accumulative, is maintained by a spring-loaded ball detent which provides near-perfect internal alignment. All working parts are enclosed and permanently lubricated. Life is a minimum of 3,000,000 steps (3,000,000 in each direction for bidirectional models). Ledex, Inc., Dayton, Ohio.

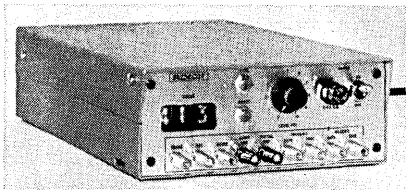
CIRCLE 216 ON INQUIRY CARD

BUFFER MEMORY

The complete 1K by 1 random access high-speed buffer memory, including address decoding, stack drivers, data register and control circuits, occupies a single printed circuit card. The 0 and +5 Vdc TTL logic signal and +12, +5 and—6 regulated power source interface through a single gold-plated edge connector. Cycle speed is 1 microsecond in a read or write mode, and read data access time is 750 nanoseconds. Separate read or write initiate pulse signals activate the coincident current core storage memory. United Telecontrol Electronics, Asbury Park, N.J.



CIRCLE 217 ON INQUIRY CARD

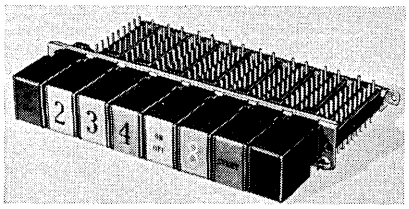


ERROR TEST SET

The modem error rate test set, Model TS-100, is a multi-purpose instrument designed for performance testing of modems alone or on the communication channel over which they are operating. Error rate is clearly displayed on a decimal readout.

Features include the extra length of the pattern generated, 32,767 bits in duration. Additionally, an external error output is provided to attach a counter for long-duration testing. Rixon Electronics, Inc., Silver Spring, Md.

CIRCLE 218 ON INQUIRY CARD



LIGHTED PUSH-BUTTON SWITCHES

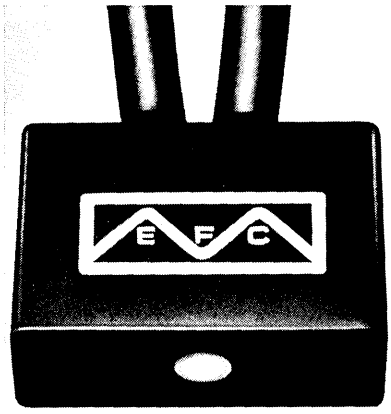
A line of lighted push-button switches is available, with the same electrical specifications as those for non-lighted switches. Basic rating is 0.45 amp @ 115 Vac (1.00 amp @ 28 Vdc). The lighted switches come with a wide range of lens colors and filters to permit adjustment of light diffusion and color intensity. Legends may be hot-stamped on lenses and/or filters; and lenses snap out to facilitate bulb replacement. Centralab, Milwaukee, Wis.

CIRCLE 219 ON INQUIRY CARD

MINIATURE POWER REGULATORS

High-efficiency transistor switching preregulators are offered in a 0.5 cubic-inch package weighing only 0.8 ounce with ratings up to 36 watts. The series is ideal for preregulator functions as they provide a 10:1 typical reduction in input voltage excursions at typical efficiencies of 80 to 90%. Units are available that handle source voltages from 6 to 60 volts dc, and that provide transient and spike protection to MIL-STD-704A. Powercube Corp., Waltham, Mass.

CIRCLE 220 ON INQUIRY CARD



FIBER OPTIC SENSOR

A compact low-cost reflective fiber optic sensor, called the Omni Sensor, uses random bundles to efficiently sense pencil and timing marks, punched holes, label codes and other types of printed or written data. It has double sensing bundles to detect the silvered mylar strips which signal load point and end of reel on computer tapes.

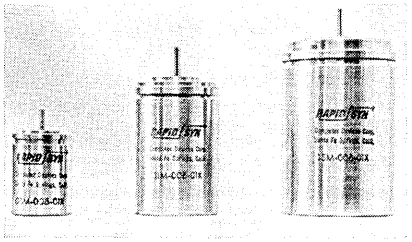
Encased in a phenolic molding, the Omni Sensor has leads from six inches to two feet long. One lead is placed next to a light bulb and the other is fixed to a photodetector selected to meet application requirements.

Designed for plug-in mounting, the package includes a 40,000-hour lens-end bulb and photo transistor coupled to a transistor amplifier circuit. Input is 5V dc at 140 mA. Output to a high impedence load is 5V for switching with a square wave having a rise-time of 2 microseconds. Electro Fiberoptics Corp., Worcester, Mass.

CIRCLE 221 ON INQUIRY CARD

45° STEPPERS

These 28-volt Rapid-Syn steppers in sizes 8, 11, 15 and 20 are available from stock and offer slew speeds up to 2,500 pps, response speed up to 700 pps, and static torque up to 14 oz/in. Other features include Class H insulation, ABEC 5 bearings, a high coersive alnico magnet and a one-billion-cycle endurance rating. Computer Devices Corp., Santa Fe Springs, Calif.



CIRCLE 222 ON INQUIRY CARD

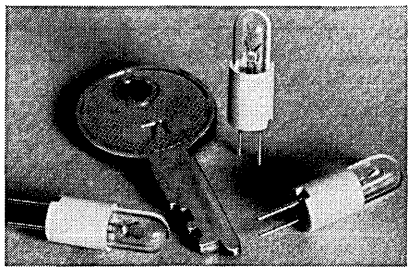
NEW PRODUCTS

MAGNETIC MODULATORS

A line of magnetic modulators, analog voltage multipliers and demodulators in flat pack configurations, with typical dimensions of 0.1-inch thick by 0.5 by 0.75-inch is characterized by drift-free circuitry with superior phase and gain slope stability over a temperature range of −55° to +125°C. They are shock- and vibration-proof, have a MTBF of 0.15 per mm hours, they are not affected by high intensity nuclear radiation, and are capable of operating on carrier frequencies as high as 5 Mhz.

One or more isolated or floating input signals may be used for modulating, multiplying, dividing, squaring or extracting a root. These modules have no external nulling or offset adjustments. No additional components or compensation are required, nor are external operational amplifiers. General Magnetics Inc., Bloomfield, N.J.

CIRCLE 223 ON INQUIRY CARD



BI-PIN LAMPS

T-1¾ lamps are wire terminal models with a tough, plastic, bi-pin base, for printed circuit boards, indicator lights, and switches. Lamps are cemented into the base and lead wires soldered to the pins for permanent contact. Gas vent slots are designed into the base to prevent solder blowout during dip-solder operations.

The base diameter measures .225 ±.005 inch. Overall the lamp is .625 inch, exclusive of pin length. Standard pin length is .250 ±.010 inch, but lengths to .750 inch are optional. Pins are spaced at .125 ±.005 inch. Industrial Electronic Engineers, Van Nuys, Calif.

CIRCLE 224 ON INQUIRY CARD

QUAD D-A-LADDER SWITCH

A hybrid IC quad D-A ladder switch is being offered, for use in binary and BCD-coded voltage summing ladders up to 14 bits with ¼ LSB accuracy. Designated ATF-451, it measures only .550 by .550 by .160 inch, and is claimed to represent the smallest set of four matched switches ever offered in a single hybrid integrated circuit. Input circuitry is fully compatible with standard DTL and TTL monolithic circuits. Based on a thin film/LID hybrid process, the new device, designed around semiconductors and thin film substrates, offers low initial cost, elimination of redundant packaging, and the opportunity for combining multiple switches of high accuracy levels in a single circuit.

The switch has an on-resistance of 4 ± 1 ohm from −25° to +85°C and offset voltage of 1 millivolt maximum. An identical lower-accuracy version, the ATF-452, is also available, with an on-resistance tolerance of ± 3 ohms and maximum offset voltage of 1.25 millivolt. Amperex Electronic Corp., Cranston, R.I.

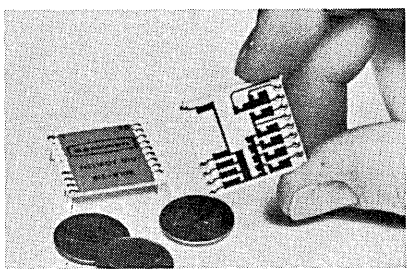
CIRCLE 225 ON INQUIRY CARD

MICROCIRCUIT LADDER NETWORK

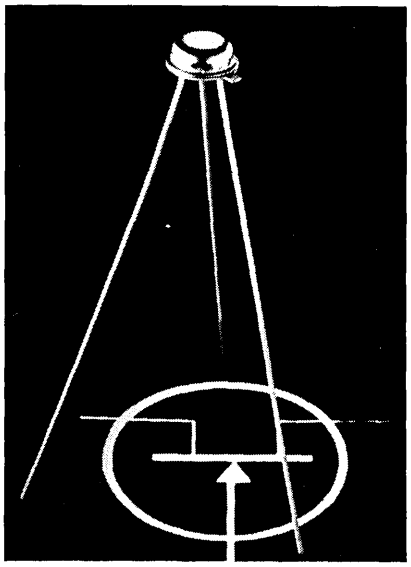
A miniature 8-bit high-speed binary ladder network sells for 75% below the cost of comparable Mil Spec networks. Model 815 meets applicable environmental requirements of Mil Spec 883, including those for thermal shock, temperature cycling, moisture resistance, solderability, shock and vibration.

The unit has a standard resistance value of 10K ohms. Maximum output voltage ratio error is 1,952 ppm over the operating temperature range of −55° to +125°C. The network offers a fast ladder settling time, with output voltage to within 0.1% of final value within 10 nanoseconds after application of input step.

The 815 is less than 0.1 inch thick and occupies only one square inch of board space. Prices are from $4.87 to $6.95. Beckman Instruments, Inc., Fullerton, Calif.



CIRCLE 226 ON INQUIRY CARD

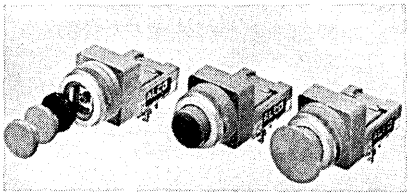


FIELD-EFFECT TRANSISTOR

The CMX740 FET, available from stock, claims extremely low on-resistance of 2.5 ohms maximum, providing high analog switching accuracy in D/A and A/D converters. It is the fastest core-driving transistor, handling short-duration very high current pulses up to ½ amp minimum.

Advantages for D/A and A/D converters are 50- and 75-nanosecond respective on and off times, it is radiation-tolerant, and takes 100 times more radiation than bipolar transistor before its on-resistance is doubled. Crystalonics, Cambridge, Mass.

CIRCLE 227 ON INQUIRY CARD



POWER SWITCHES

Miniature push-button switches are designed for electronic panel controls. Rated to carry 6 amps @ 230 Vac, they may be used to control circuits independently or with optional contractors or starters.

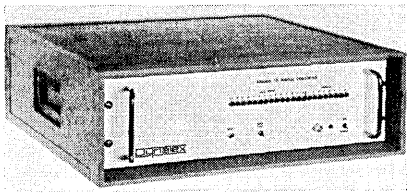
Synthetic rubber seals make the switches oil, water, and vaporproof. The "SW" series features doublebreak solid silver contacts for positive make or break. All switches mount in a one-inch diameter hole, and each model is supplied with a single (NO-NC) block. An additional block is available for converting these switches to a double pole unit. Alco Electronic Products, Inc., Lawrence, Mass.

CIRCLE 228 ON INQUIRY CARD

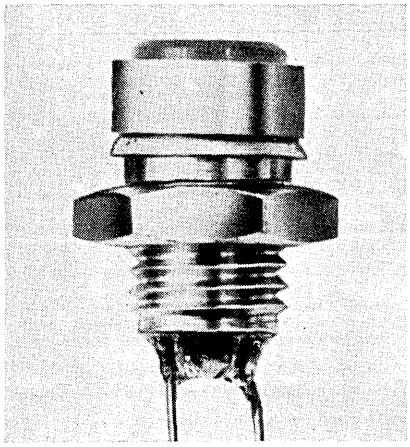
NEW PRODUCTS

HIGH SPEED A/D CONVERTER

The ADX when used in conjunction with the companion differential input multiplexer, provides random or sequential access to as many as 512 analog channels at a rate of 200,000 conversions per second for a 14-bit binary data word. Input impedance is 500K ohms, and system accuracy, including multiplexer, is better than 0.05%. Rack-mounted versions can house up to 256 channels of multiplexer, computer interface and off-line test circuitry within 41¼ panel-inches, while MIL-E-16400 and MIL-E-5400 versions are completely modular to simplify system integration for both original and retrofit installations. Dynalex, Inc., Burbank, Calif.



CIRCLE 229 ON INQUIRY CARD



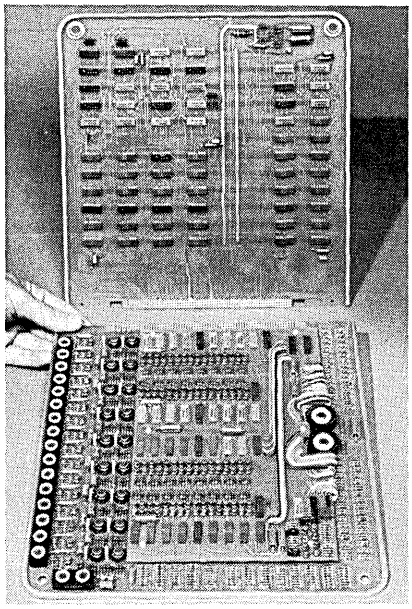
INDICATOR LIGHT

The 104S ultra-miniature neon indicator light assembly mounts on ⅜-inch centers, with lenses available in five styles and a variety of color and materials.

The 104 uses a T1 ⅛ neon lamp 0.3 milliamp with a 30,000-hour life. With a 220K resistor the 104 can be used on a 115-volt commercial line current, and with a 560K resistor, can by used on a 230-volts commercial line current.

Starting voltage for ac is 60 volts; for dc, 90 volts. The Sloan Co., Sun Valley, Calif.

CIRCLE 230 ON INQUIRY CARD



CORE MEMORY SYSTEM

A compact, low cost, expandable core memory system on plug-in cards has been developed. Memcard 418 is a 1.5-microsecond system featuring read/restore, read/write, read/modify/write, and a hybrid cycle—read/write/mask. The total 4096 by 18 system is contained on two 12-inch square plug-in circuit boards—one card providing all I/O electronics necessary to drive 32,768 words by 18 bits of memory. The second, a magnetics board, contains 4,096 words by 18 bits of core storage. All systems are complete with both address and data registers, power/off, protection and temperature compensation from 0° to +50°C operation. Sanders Associates, Inc., Nashua, N.H.

CIRCLE 231 ON INQUIRY CARD

MAGNETIC TAPE SYSTEM

Hewlett-Packard 2114A, 2115B and 2116B computers can sort, match, collate and merge data when equipped with a digital magnetic tape system, the Tri-Data CartriFile 4096-04 cartridge-loaded system, which combines four magnetic-tape transports and is plug-compatible with the H-P computers. A software package providing system input/output, basic control system driver and diagnostic program subroutines is included.

Reading and writing may occur simultaneously at data-transfer rates of 667 8-bit bytes per second in variable-length records, with a storage capacity of 480,000 bytes. Data accuracy is assured by redundant recording and on-the-fly error correction. Tri-Data, Mountain View, Calif.

CIRCLE 232 ON INQUIRY CARD

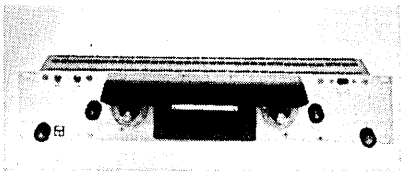


PHOTO-ELECTRIC TAPE READER

The Model 5401 is a photo-electric punched tape reader. It operates from 0 to 300 characters per second, asynchronously, and 625 cps, synchronously, in the standard configuration. Options increase the asynchronous rate to 400 cps and the synchronous rate to 850 cps. The reader stops on character in all modes.

An automatic lamp-brightness control compensates for varying tape opacities with no need for adjustment. The standard ac input is 50-60 Hz, 115 volts. An option for 40- to-800-Hz operation may be specified.

The basic reader occupies 3½ inches of panel space in a standard 19-inch rack. Chalco Engineering Corp., Gardena, Calif.

CIRCLE 233 ON INQUIRY CARD

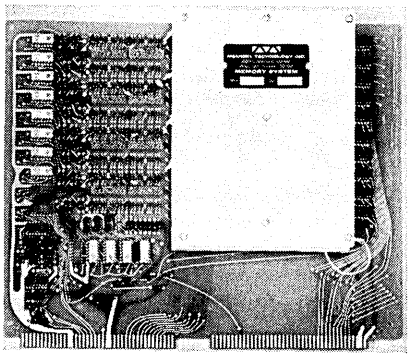
READ-ONLY MEMORY SYSTEM

S-Series read-only memories operate at 500 nanoseconds access time, 900 nanoseconds cycle time, and range in capacity from 64 to 2,048 words, from 10 to 80 bits per word.

The S-Series are pin-for-pin compatible with the F-Series (180 nanoseconds access time, 300 nanoseconds cycle time) and the standard (200 nanoseconds access time, 500 nanoseconds cycle time).

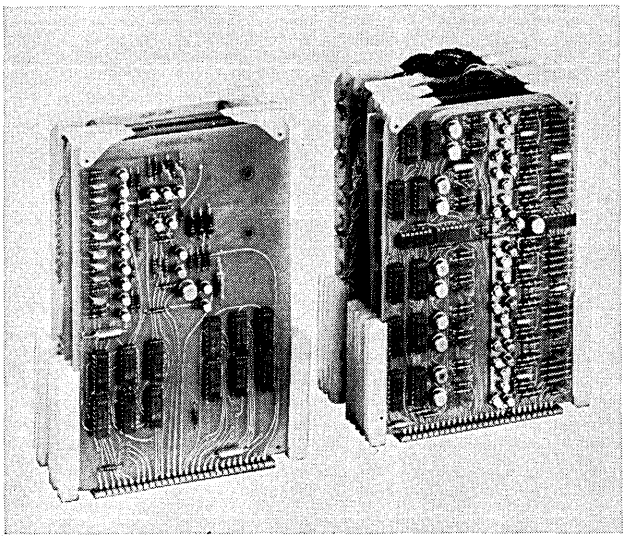
Individual words or the entire memory content may be changed in the field within a few minutes.

The S-Series requires less than 5 watts of power, has TTL and DTL compatible interface, a 0° to +70°C temperature range, nondestructive readout and requires only one power supply (+5 volts). Memory Technology Inc., Waltham, Mass.



CIRCLE 234 ON INQUIRY CARD

NEW PRODUCTS



MAGNETIC MEMORY SYSTEMS

Designated Alpha 10.2 and Alpha 12.2 memory systems, the units feature modular construction, excellent reliability, high density and low cost. Basic modules come in sizes of 1024 and 40,960 bits with expansion to larger capacities through the use of multiple modules. Cycle times are 1.50 microseconds for the Alpha 10.2, which has a maximum module size of 1024 by 10, and 1.75 microseconds for the Alpha 12.2, with module capacities to 4096 by 10.

High-density packages are the result of employing 23 mil cores, three-wire 3D organization and integrated circuits except for final drivers and selection. The Alpha 10.2 and 12.2 require 65 and 130 cubic inches respectively, for complete memories including registers and a temperature compensation regulator for the memory drive voltage. Only silicon semiconductors are used, none are in plastic packages. Tetra Corp., Minneapolis, Minn.

CIRCLE 235 ON INQUIRY CARD

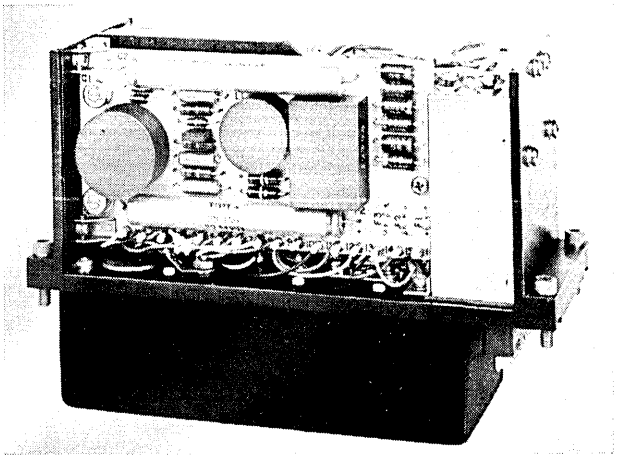
TAPE CARTRIDGE DRIVE

A series of small inexpensive 1/4-inch magnetic tape cartridge drives are oriented towards data communications systems. Called the RJ Delta-Corder 500 series, the drives are designed to mount internally in card readers, keyboard terminals, acoustic couplers and other terminal devices.

Input to the recorder can be any bit serial code, such as 11-bit-serial USASCII. Tape storage capacity is approximately 22,400 characters at eleven bits per character on 400 feet of tape.

Cartridges may be read-out over a Western Electric dataset or similar modem, or an acoustic coupler. Alternatively, the cartridge can be mailed to a central processing formatting area. Reader output is either 110 bits per second for remote transmission or 1,000 bits per second for the converter. RJ Communication Products, Inc., Phoenix, Ariz.

CIRCLE 236 ON INQUIRY CARD

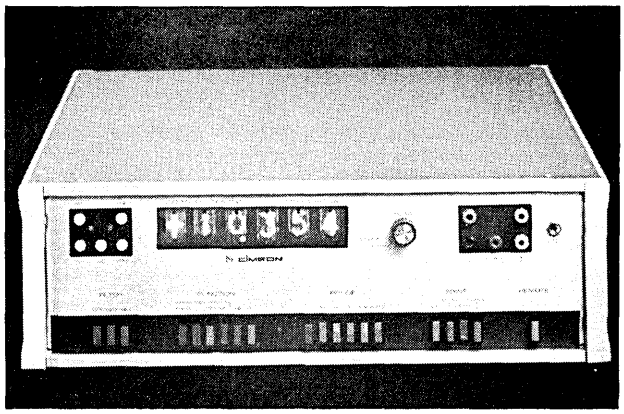


COMPUTER POWER SUPPLIES

The supplies have power densities up to 2.5 watts per cubic inch (5 Vdc at 25 Adc in 50 cu. in.). Incorporating high frequency switching regulators, they meet the line transient requirements of Mil-Std-704A and EMI requirements of Mil-I-6181D.

The supplies weigh 3.5 pounds and require no additional heat sinking for operation between −55° and +85°C. Operation to +105°C is possible with minimal interfacing since all components are suitable for operation at 125°. 76 to 82% efficient, they provide ±0.1% line and 1% load regulation. Of particular significance is the supplies' ability to store energy for 3 milliseconds. Short circuit and overvoltage (crowbar) circuits are included as well as power sequencing with optional power normal and power abnormal signals. Cal-Power Corp., El Segundo, Calif.

CIRCLE 237 ON INQUIRY CARD



DIGITAL MULTIMETER

Designated Model 6653A, the unit is an all IC-logic four-digit instrument with fifth-digit, 10% overrange. It measures dc and dc/dc ratios with an accuracy of ±1 digit from 0 to 1099.9V. Plug-in function options include ac in four ranges, ohms in five, and millivolts in three ranges. Digitized rate is 1,000 readings per second. Sample and hold is a plug-in option. Five print-out options (buffered or non-buffered), auto-ranging and remote control of all front panel functions are available. The unit is standard 19-inch rack-mount. Lear Siegler, Inc., Cimron Div., San Diego, Calif.

CIRCLE 238 ON INQUIRY CARD

NEW PRODUCTS

LOW-LEVEL MULTIPLEXER

Plug-in circuit cards simplify interface of a solid-state low-level multiplexer to digital systems. Designated model 2930A, the unit handles up to 64 analog inputs. MOSFET integrated-circuit switches at each input connect signals one at a time to the instrument's programmable amplifier, which boosts signals in the 10-millivolt range (full scale) and higher to a 10-volt range. The Multiplexer thus makes it possible for an analog-to-digital converter to work with low-level signals, such as those from strain gages, thermocouples, and other low-level transducers. The amplifier's fast settling time, 40 microseconds, allows input multiplexing at rates up to 20 kHz. The analog input signals are completely isolated from the digital circuits.

Digital control signals program the amplifier to one of 11 factors, from 1 to 1024 in binary steps. Amplifier gain accuracy is better than ±0.02% and dc drift is less than 5 microvolts (referred to input) per day. Output impedance is less than 1 ohm, assuring high accuracy when driving an ADC, with input impedance as low as 1,000 ohms. Hewlett-Packard Co., Palo Alto, Calif.

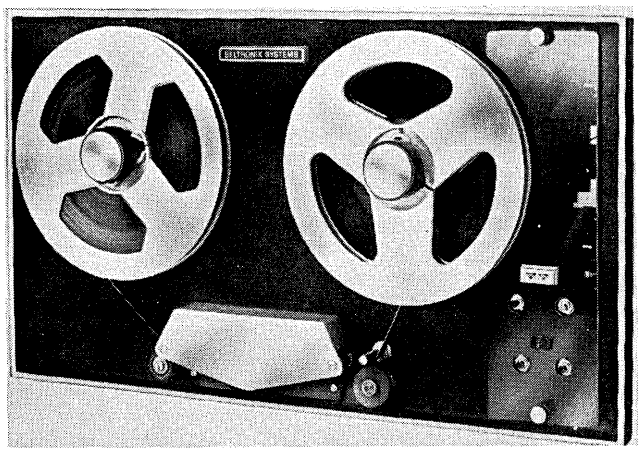
CIRCLE 239 ON INQUIRY CARD

OEM TAPE TRANSPORT

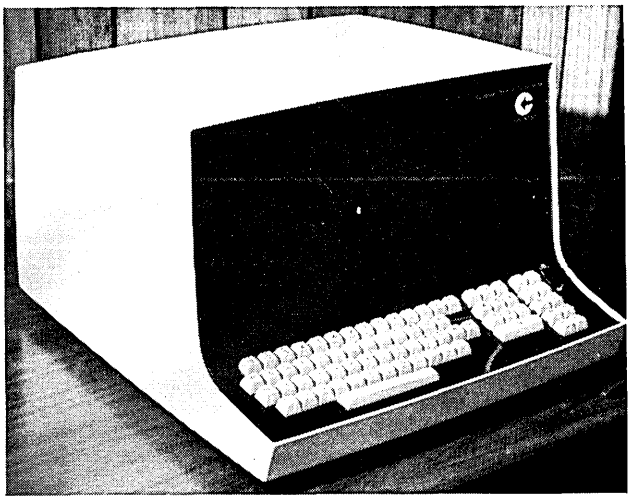
Mechanical and electronic capabilities are features of a tape transport, called the Tape-Dex 5000, which is built on a rugged (4 lbs. +) cast aluminum mainframe and can operate in vertical, horizontal or any intermediate position. All head adjustments are made from the front. Pressure pads have been eliminated through the use of a flutter filter hold-back tension idler.

The transport employs three 4-pole induction motors for fast, automatic operation. Tape speeds are 7½, 3¾, and 1⅞ inches per second. Rewind speed is 45 seconds (1200 feet on a 7-inch reel) with a timing accuracy of ±0.15%. The capstan shaft is made of casehardened steel, ground to an accuracy of ±0.00015 inch. The capstan drive is housed in oil-impregnated bronze bearings.

The standard head mounting accomodates three heads with an optional 5-head mounting. The solid aluminum casting is finished in black, semi-gloss baked enamel with optional vinyl front panel inserts. Dimensions are 10½ inches high by 19 inches wide and will fit all standard rack cabinets. Beltronix Systems, Hauppauge, N.Y.



CIRCLE 240 ON INQUIRY CARD



TIME-SHARING DATA TERMINAL

The Datapoint 3300 is a data terminal which streamlines man/machine communications for the computer time-sharing user.

Standard features of the 3300 include complete interchangeability with standard teletypewriter equipment, high-speed data transmission capabilities, a high capacity and flexible CRT display, easy to read characters, solid state construction, a 64-character set keyboard, and it is self-contained. Optional features include magnetic tape memory, hard copy printer and a ten-key numerical keyboard.

The Datapoint 3300 screen can accommodate 25 lines with 72 characters in each—a total of 1,800 characters in a single display.

Data transmission rates of up to 600 bits per second are available on the standard 3300, and up to 4,800 bps with optional speed buffer equipment. Also available is a magnetic tape memory designed as a companion unit. This memory, which utilizes replaceable tape cassettes, offers the remote user the flexibility of both forward and reverse line-incremental playback of data up to 200 full "frames" (25 lines of 72 characters each). Computer Terminal Corp., San Antonio, Tex.

CIRCLE 241 ON INQUIRY CARD

DATA RATE TAPE UNIT

A high-performance digital magnetic tape unit has the highest data rate of any such unit in the low cost category. The transport features a read-after-write dual stack head, operates at speeds of 37.5, 25, or 12.5 ips and has a rewind speed of 150 ips. The 6 by 40 is equipped with 10½-inch reels and can be ordered either in 9-track 800 bpi or 7-track dual-density configurations. The unit is compatible with IBM 729 and 2401 (Model 1) and IBM 2415 (Models 1-3 and 1-6).

Other features include an adjustment-free tape guiding system, electronic deskewing and low power consumption. It has all drive, control and write/read electronics, bring to load point logic and is organized for multiple transport operation. The low inertia capstan drive provides rapid acceleration and deceleration while maintaining positive control of the tape on the capstan at all times. Control of the tape path is maintained by a precision edge guidance system guaranteeing IBM interchangeability. Peripheral Equipment Corp., Chatsworth, Calif.

CIRCLE 242 ON INQUIRY CARD

Causes and Cures of Noise in Digital Systems

J. PAUL JONES

PART 1

Systems Design Considerations

PART 2

Noise Elimination in Digital Modules

PART 3

Control of External Noise

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NEW PRODUCTS

DATA ACQUISITION/CONVERSION SYSTEM

Designed to meet MIL-E-5400J, MIL-I-6181D, and MIL-STD-704A, Model 460 all-solid-state airborne data acquisition and conversion system includes a multiplexer, differential amplifier, A/D and D/A converters, sample-and-hold data distributor, inverter power supply, and control and timing circuitry. Optional interfaces include computer, tape transport, telemetry, etc.

Features include MOS-FET switches, TTL logic, low-power, high-reliability circuitry, plated-through holes, flame-retardant printed circuit boards, expandability, flexibility in interface and timing, RFI shielding, and self-contained power supply.

The system has 0-64 differential analog low/high-level input channels, 0-32 analog output channels, full-scale input/output voltage (up to ±10.24V), resolution to 12 bits including sign, sampling accuracy to 0.01%, sampling rate to 50 KC, input impedance greater than 10 megohms, and a common mode rejection of 100 db at dc, 94 db at 60 Hz, and 80 at 400 Hz (with 5K source and up to 1K source unbalance). In data distributor output, Model 460 has a conversion accuracy up to 0.01%, decay rate of 160 mv/second, settling time less than 8 microseconds to 0.01%, conversion rate of 100KC, and output drive of 10 mA with up to 500 pF of load.

It operates efficiently between −55° and +71°C, is only 6.25 inches by 15 inches by 9 inches in size, weighs 28 pounds, and operates on 28 Vdc ±6V and less than 2 amps. Dynamic System Electronics, Tempe, Ariz.

CIRCLE 243 ON INQUIRY CARD

MAGNETIC TAPE TRANSPORT

Readily adaptable to all forms of magnetic tape recording by the addition of modular audio or digital electronics is the model TT-1150 universal tape transport, available with two or more tape speeds for record/reproduce.

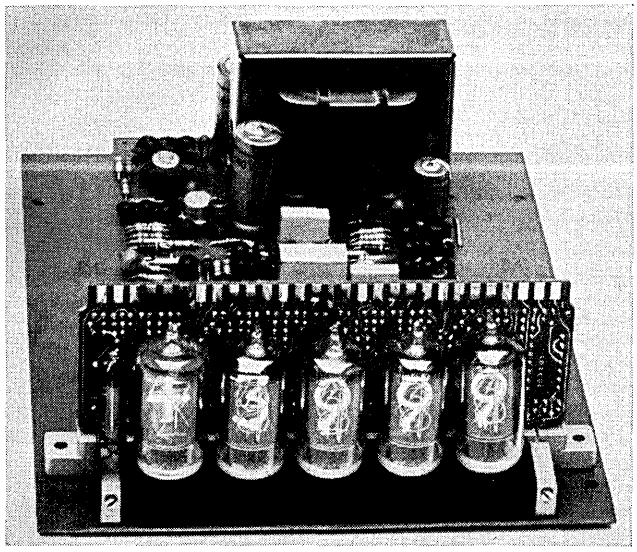
Tape speeds are 3¾-7½ ips selectable at installation; tape width is ¼ inch, reel size is 7 inch maximum; wind-rewind time is 1,200 feet in approximately 45 seconds; capstan assembly consists of a precision-ground spindle-mounted in composite porous bronze and ball bearing housing, permanently lubricated. Wow/flutter is 0.2% rms maximum @ 7.5 ips; 0.3% maximum @ 3.75 ips. A precision polyurethane belt drive is included for flutter control. The transport has fail-safe electro-mechanical-differential band brakes on both supply and take-up spindles, which in the case of power failure stops transport without tape deformation.

The unit can be supplied with or without a search mode having an adjustable or fixed search speed. A precision micrometer azimuth and height adjustment is provided to allow for recordings made on any transports to be reproduced with optimum precision on the TT-1150. All tape-handling components are mounted on a precision prepared tool and jig plate which is tempered after machining to ensure long-term dimensional stability. Lifters allow the tape to contact the heads only in play mode. In the moderate and fast modes of operation the tape contacts the search head only. Telectro Systems Corp., Corona, N.Y.

CIRCLE 244 ON INQUIRY CARD

DIGITAL PANEL METER

A digital panel meter capable of reading from 0000 to 3999 with .05% accuracy features >1000 megohms input impedance, up to 60 readings per second, non-blink display, 300ms step response, 35db at 60Hz normal mode rejection, 400% overrange, programmable decimal point, and display hold capability. Five standard full-scale voltage ranges from 39.99mV to 399.9V, seven current ranges from 399.9nA to 399.9mA, and five resistance ranges from 399.9Ω to 3.999M are available. Options include automatic polarity digital set points, 1- and 10-microvolt resolution preamplifiers, fully buffered BCD and 10-line outputs, wide range zero offset, differential input, remote display and ratio. The reading can be offset up to 2,000 digits, for industrial control applications, for zero suppression, and in weighing systems to provide Tare capability. The digital limits are designed so that each set point can easily be switched between any required number of thumbwheel assemblies in monitoring an automated production line or batching system. Electro-Numerics Corp., Santa Clara, Calif.



CIRCLE 245 ON INQUIRY CARD

DATA ACQUISITION SYSTEMS

The 5400 Series D-DAS (digital data acquisition systems) are assembled from off-the-shelf instrument modules, each of which plugs into the next unit with a single "data-bus" cable. Up to 1,000 data-input channels are accommodated with scanners which expand in 10-channel increments. Data inputs can be dc, ac, resistance or binary-coded decimal as follows: dc: 5 microvolts to 300 volts; ac: 1 to 1,000 volts; ohms: 5 milliohms to 10 megohms; BCD: from digital transducers, shaft encoders, counters, etc. Output is encoded in computer-compatible format on punched or magnetic tape. Teletypewriter and printed paper tape systems are also available to provide a visual record of the digital data.

The systems offer excellent linearity and produce absolute reading accuracies in the 0.025 to 0.5% range. Floating input and data averaging (integration) eliminates superimposed noise effects. Dynamic range capability is over 80 dB (10,000:1). Vidar Instrumentation and Telecommunication Products, Mountain View, Calif.

CIRCLE 246 ON INQUIRY CARD

LITERATURE

Thick Film Hybrid Circuits

Custom circuits, capable of testing, trimming, and retesting up to 800 circuits an hour, for use in operational and differential amplifiers, computer circuitry, microwave applications, ordnance, and high-packaging density power and motor controls, highlight a 4-page bulletin released by the Cermex Division of Frenchtown/CFI, Inc., Frenchtown, N.J.

CIRCLE 300 ON INQUIRY CARD

Microminiature Indicator Lights

Bases, lamp types, and material and cap styles available for microminiature indicator lights that produce greater intensity than units five times their size, are detailed in a data sheet issued by Shelly Associates, of El Segundo, Calif.

CIRCLE 301 ON INQUIRY CARD

Data Terminal

Telephone/computer couplers and tape reader/perforators are features of a data terminal reviewed in a brochure from the Vernitron Corp., of Farmingdale, N.Y.

CIRCLE 302 ON INQUIRY CARD

Digital Control Systems

A 4-page short-form catalog describing systems for data acquisition and/or control of scientific analytical instruments, including digital integrating and spectrogram recorders, comparator and spectrophotometer data systems, a mass spectrum digitizer, x-ray diffractometer control system, and computer operated numerical rotary axis controller, is presented by the Conrac Corp.'s Datex Division, of Duarte, Calif.

CIRCLE 303 ON INQUIRY CARD

Data Processing Equipment

Second and third generation computers, unit record machines, and peripheral equipment as well as advantages of purchasing or leasing equipment, are emphasized in a "full line" brochure released by the IOA Data Corp., New York, N.Y.

CIRCLE 304 ON INQUIRY CARD

Display Deflection Yokes

Details on four highly efficient stator-type high-Q deflection yokes, including features and specifications, dimensional drawings, push-pull coil and single-ended coil data for all types, are presented in a 2-page bulletin by Syntronic Instruments Inc., Addison, Ill.

CIRCLE 305 ON INQUIRY CARD

Digital Memory Modules

Low cost, high speed digital memory modules, made with zero-temperature coefficient glass, which include interfacing circuitry, may be plugged in with standard logic levels, and are capable of storage of from 200 to 200,000 bits with a per-bit cost of 2.5 cents, are described in an illustrated data sheet issued by Corning Glass Works, of Corning, N.Y.

CIRCLE 306 ON INQUIRY CARD

Magnetic Tape Transport

A data sheet, detailing capabilities and applications of a magnetic tape recorder designed for such severe environment applications as rocket sleds and nuclear tests, has been released by the Genisco Technology Corp., of Compton, Calif.

CIRCLE 307 ON INQUIRY CARD

Communications Data Set

The capability of operating over private lines or the direct distance dialing network and transmitting and receiving asynchronous serial digital data, are features of a data set described in an illustrated bulletin from the Sangamo Electric Co., of Springfield, Ill.

CIRCLE 308 ON INQUIRY CARD

Servo & Computing Modules

A short-form catalog listing details and specifications of over 75 solid-state devices for converting and computing, and of synchro input and output devices, and containing application drawings of solid state servos, is available from Transmagnetics, Inc. of Flushing, N.Y.

CIRCLE 309 ON INQUIRY CARD

Data Recorder Integrator

A 4-page brochure detailing an integrating device with potentiometric strip chart recorders, and including an illustrated theory of operation, is available from Disc Instruments Inc., Santa Ana, Calif.

CIRCLE 310 ON INQUIRY CARD

Digital Tape Drives/Memories

Performance and specifications of high-environmental digital tape drives and memories, designed for field data gathering requiring extreme ruggedness, high reliability and generation of IBM-compatible taped data, are described in a brochure from the Ampex Corp., of Redwood City, Calif.

CIRCLE 311 ON INQUIRY CARD

Storage Tubes

Specifications and features of single and dual gun storage tubes for data processing and flying spot scanners are included in a 4-page short-form tube catalog available from Warnecke Electron Tubes, Inc., Des Plaines, Ill.

CIRCLE 312 ON INQUIRY CARD

Time Sharing Systems

A detailed description of systems, their benefits, and a glossary of terms, are featured in an illustrated 28-page booklet obtainable from the General Electric Co., Schenectady, N.Y.

CIRCLE 313 ON INQUIRY CARD

Tape Preparation Centers

On- and off-line paper tape preparation centers with input and output devices ranging from a keyboard-tape punch to a I/O system are described in a brochure available from the Invac Corp. of Waltham, Mass.

CIRCLE 314 ON INQUIRY CARD

Compatible Calculators

Features and functions of all-purpose electronic calculators, including application problems and keyboard solutions, are detailed in a 16-page booklet, from Wang Laboratories, Inc., of Tewksbury, Mass.

CIRCLE 315 ON INQUIRY CARD

Cermet Industrial Trimmers

A data sheet detailing trimming potentiometers, which sell for $3.50 or less and are the first industrial cermet trimmers priced competitively with wirewounds, is available from the Helipot Division of Beckman Instruments, Inc., of Fullerton, Calif.

CIRCLE 316 ON INQUIRY CARD

Germanium Power Transistors

Electrical specifications and characteristic curves for a new series of Ge power transistors in TO-8 cases are provided in a data sheet. KSC Semiconductor Corp., Chelmsford, Mass.

CIRCLE 317 ON INQUIRY CARD

Microcircuit FET-Input Op Amp

Specifications, applications, and performance curves of a 0.25" high by 0.6"-square microcircuit operational amplifier with high impedance FET input circuitry, and with a 5 picoamps guaranteed maximum bias current, are contained in a data sheet from Analog Devices, Inc., of Cambridge, Mass.

CIRCLE 318 ON INQUIRY CARD

Thick Film Circuits

A brochure has been issued, describing the capability of hybrid circuits to bring together the best portions of monolithic integrated circuits, thick film techniques and discrete components, plus the low cost of printed circuitry, combined in a reliable, compact package, by HEI, Inc., of Chaska, Minn.

CIRCLE 319 ON INQUIRY CARD

Optical Scanner

Details of a general-purpose transaction document scanner, equipped to read data recorded by five methods, to read four different machine codes, and to operate off-line without a computer, are the subject of a brochure issued by the Cummins-Chicago Corp. of Chicago, Ill.

CIRCLE 320 ON INQUIRY CARD

Manual Switches/Indicators

A 56-page revised catalog reviewing lighted and unlighted pushbuttons, indicators, matrix-mounted and toggle switches, as well as optional seals, boots, bushings, actuators and contact variations has been published by the Micro Switch division of Honeywell Inc., Freeport, Ill.

CIRCLE 321 ON INQUIRY CARD

Printed Circuit Connectors

Card and tape cable applications, as well as test point connectors for printed circuitry, highlight an 80-page printed circuit connector catalog issued by the Continental Connector Corp. of Woodside, N.Y.

CIRCLE 322 ON INQUIRY CARD

Selector Switches

Emphasizing the availability of a complete switch package from a single source is a 16-page catalog which includes ratings and specifications of the wafer assembly for continuous grounding of inputs, and of the index assembly for instrument design. Available from the CTS Corp., of Elkhart, Ind.

CIRCLE 323 ON INQUIRY CARD

Digital Tape Transport

Operation of the Model TM-7 digital tape transport as an incremental drive unit is described in data sheet C-085. Ampex Corp., Redwood City, Calif.

CIRCLE 324 ON INQUIRY CARD

Microminiature Bite Indicators

Built-in test equipment (BITE) indicators, for use on system, sub-system, module, and individual circuit card levels to sense fault signals and provide a visual indication of monitored equipment conditions, including specifications, dimensions, and application data, are contained in a bulletin issued by the A. W. Haydon Co., of Waterbury, Conn.

CIRCLE 325 ON INQUIRY CARD

MOS Product Guide

Lists of off-the shelf MOS circuits, including shift registers, memories, multiplex arrays, logic circuits, and channel transistors are contained in a 12-page product guide published by American Micro-systems Inc., of Santa Clara, Calif.

CIRCLE 326 ON INQUIRY CARD

Digital I/C Selection Guide

Digital integrated circuits selection has been simplified in a 6-page guide containing a graph-illustrated comparison of integrated circuits' operating characteristics, including operating temperature and power supply range, gate fanout and dissipation, average propagation delay, flip-flop toggle frequency, and noise margins. Copies, requested on company letterhead, may be obtained from Motorola Semiconductor Products Inc., Box 20924, Phoenix, Ariz. 85036.

Computer Support Services

Bulletin B-9550 describes the computer systems support services now available from the Westinghouse Information Systems Laboratory. Included is a discussion of the three criteria for determining the success of a computer system. Westinghouse Electric Corp., Pittsburgh, Pa.

CIRCLE 327 ON INQUIRY CARD

Data Communication Equipment

A thirty-five-page bulletin describes functional specifications, interfaces and applications of a 50 kilobits-per-second wideband data transmission series, including digital information systems for computer data, facsimile and digitized voice in government and military complexes, private microwave networks and dedicated transmission lines, and is available from the General Electric Co., Lynchburg, Va.

CIRCLE 328 ON INQUIRY CARD

Photo-Optical Memory

Details of the photo-optical random access mass memory, a system featuring larger capacity and faster access time, and requiring less space than any other, are presented in a 6-page illustrated brochure from Foto-Mem Inc., of Natick, Mass.

CIRCLE 329 ON INQUIRY CARD

IC Connector Harnesses

An illustrated data sheet describing applications of IC connector harnesses for computers and other electronic equipment, featuring round conductor ribbon cable harnesses with 14- or 16-pin IC compatible connectors on one or both ends, has been published by the Spectra-Strip Corp., of Garden Grove, Calif.

CIRCLE 330 ON INQUIRY CARD

Linear IC Applications

Linear devices for circuit and system designers are described in an applications brochure, including core memory sense and video amplifiers, by the Signetics Corp., of Sunnyvale, Calif.

CIRCLE 331 ON INQUIRY CARD

Standard Machine Controller

A 6-page illustrated description of an electronic machine and process controller, which serves as a solid-state replacement for relay control panels, including logic board, plug-in memory, input and output terminal boards, and system trouble-shooting aids, has been released by Information Instruments Inc., of Ann Arbor, Mich.

CIRCLE 332 ON INQUIRY CARD

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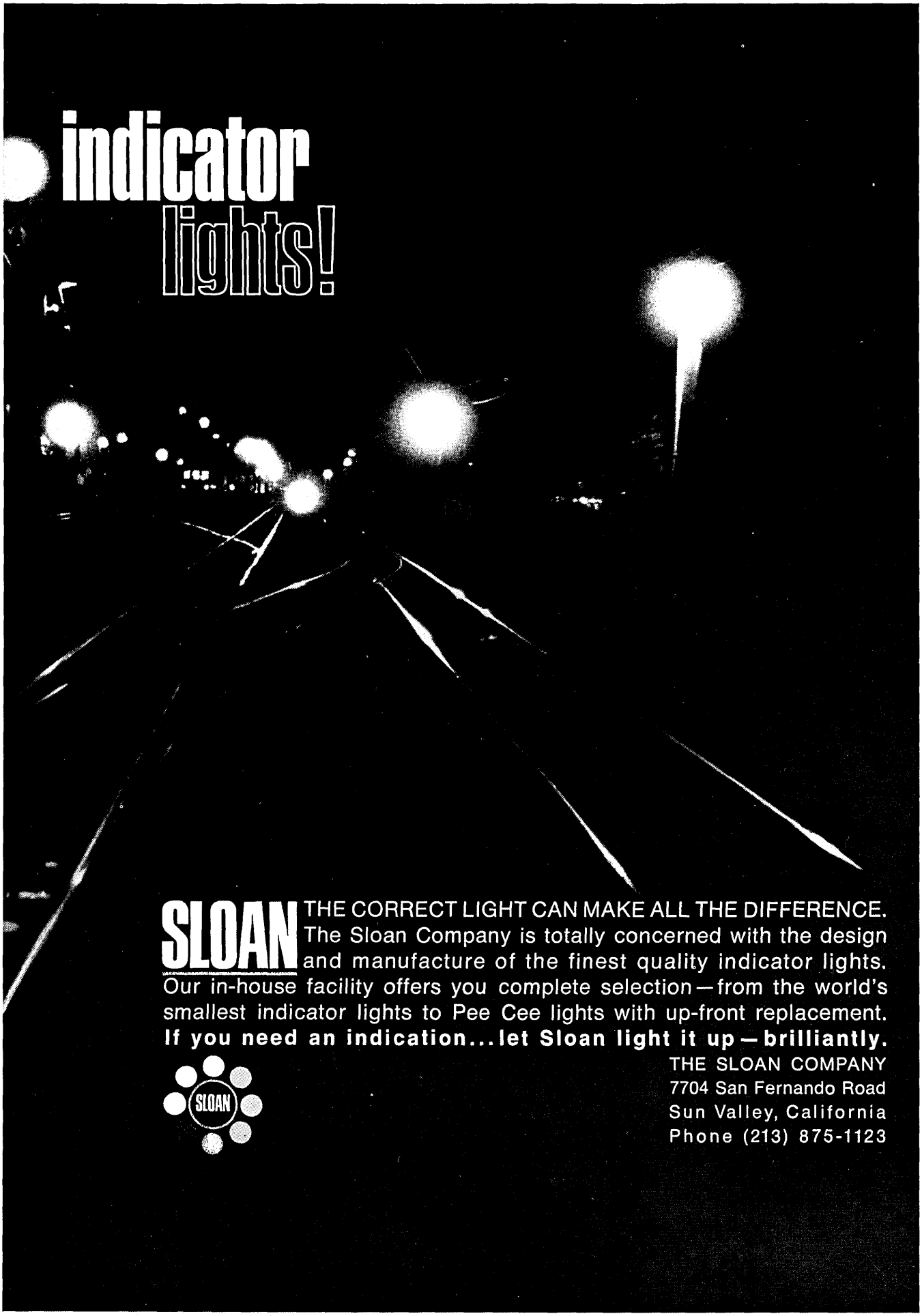

CIRCLE 50 ON INQUIRY CARD

COS/MOS—RCA's technological breakthrough breaks through in economics, too!

New design flexibility! New operating features! RCA-CD4006D brings both to digital circuits with MSI complexity! Newest in RCA's growing line of COS/MOS integrated circuits, this COmplementary Symmetry MOS 18-Stage Static Shift Register gives you:

Flexibility. It provides multiple register sections of 4, 5, 8 and 9 stages or single register sections of 10, 12, 13, 14, 16, 17, and 18 stages. And outputs are available from both fourth and fifth stages. Here's real flexibility—in both design and operation.

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Economy to Match

CD4006D—at $17.25 (1,000 units)—provides full military temperature range operation and 18 flip-flops for less than $1.00 each. That means you get the design and operating advantages of RCA's unique COS/MOS technology with real-world economics.

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- −55° to +125°C operation
- 100 nanowatt quiescent dissipation (typ.)
- Static to 2 MHz shift rate
- Single 6- to 15-volt positive or negative power supply
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- Large fanout—up to 50

CD4006D is only one of the new circuits that are ready now to prove the practicality and economy of COS/MOS. Order now from your local RCA Representative or through your RCA Distributor. For technical data, write to RCA Electronic Components, Commercial Engineering, Section ICZB-7, Harrison, N. J. 07029.

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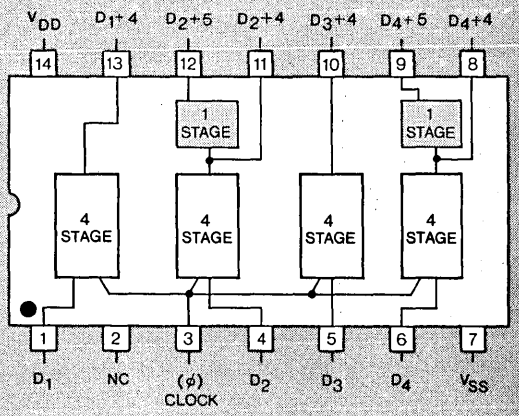
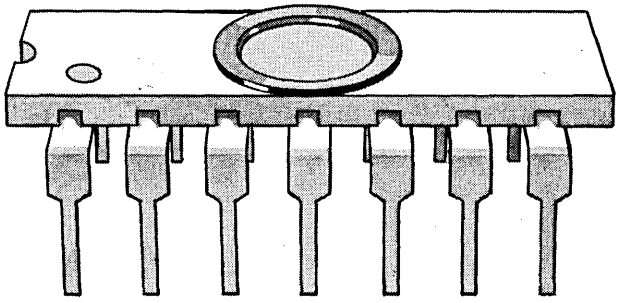
MSI density with design flexibility





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*12-lead TO-5 Style Package

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CIRCLE 51 ON INQUIRY CARD