COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

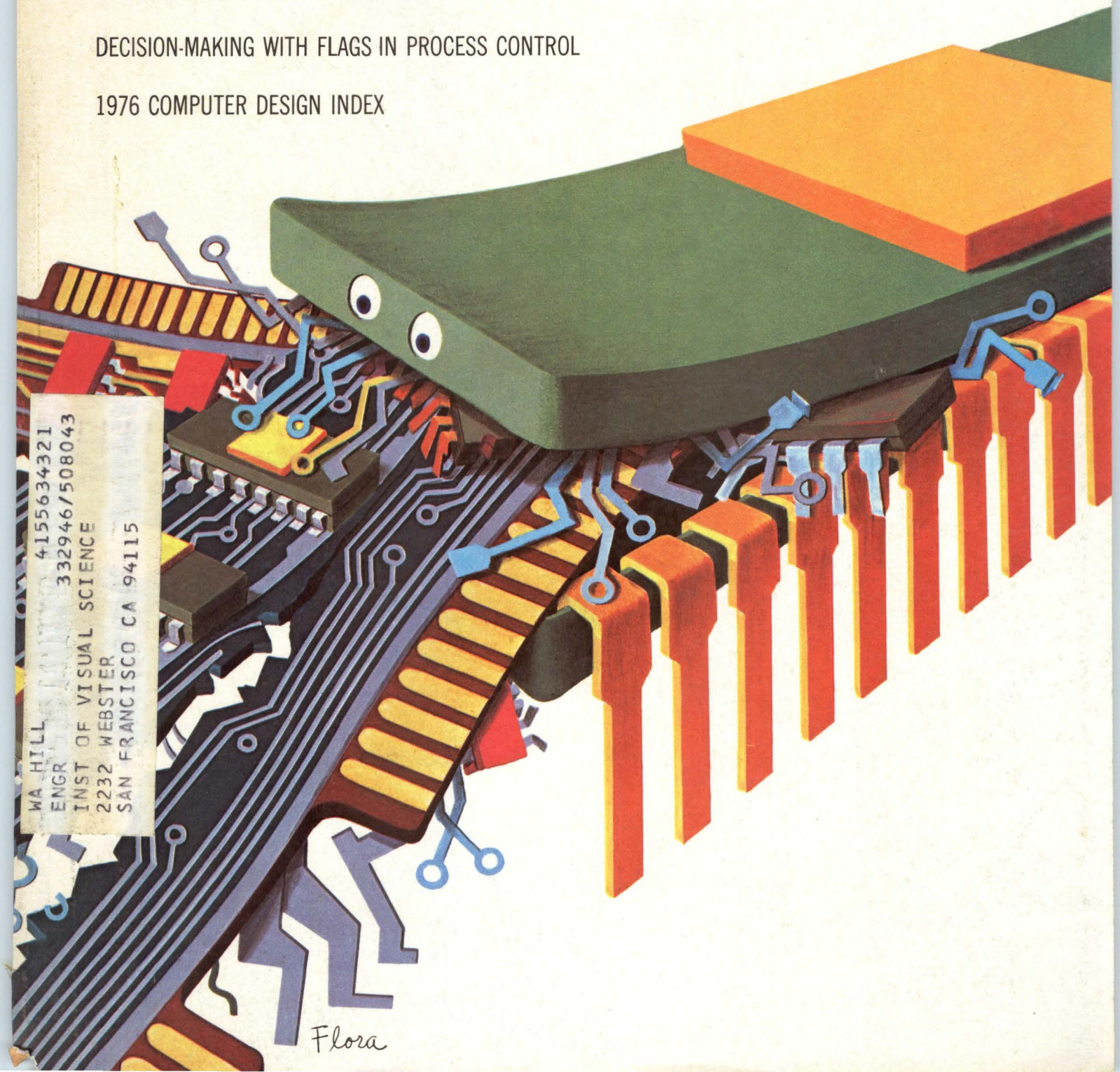
DECEMBER 1976

PUTTING A MICROCOMPUTER ON A SINGLE CHIP

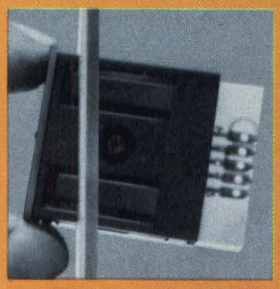
CONSIDERATIONS IN SEMICONDUCTOR TESTER SELECTION

DECISION-MAKING WITH FLAGS IN PROCESS CONTROL

1976 COMPUTER DESIGN INDEX



Intro-ducing our new thumbwheel switch



for 8-mm thumbs.
It's a skinny switch
that we call
the 1800 Series.
It has many of the features of
our notorious 1776 Series
—but simpler,
more standardized,
and cheaper.
For example, just $2.50 for one,
less for more,
with a choice of five codes,
gloss or matte finish,
with or without stops,
and readable by 20/20 eyes
from 10 feet away.

It's got PC board terminations
for plug-in or solder connections,
and it snaps into a panel for mounting
(no tools needed).
It mounts singly
or ganged (up to 20 stations),
and will give at least 500,000 detent operations
before it tires.
So now we've left you with no excuse
for not choosing EECO
when you need a thumbwheel switch.
We've got more versions
for more applications
than any other switch maker in the country.
And more offices to buy from
(87 in the U.S. and Canada).
For *any* thumbwheel switch,
see us first.
WE'VE GOT YOUR SWITCH.

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CIRCLE 1 ON INQUIRY CARD

Introducing Model 9300
Quality that's Quick & Quiet

Model 9300 Vacuum Column digital tape transport has characteristics common to all Kennedy recorders — and a few new ones. It's quick (125ips); quiet (noise level of less than 70db), and it has the built-in quality of all Kennedy products.

Utilizing side-by-side vacuum columns and a capacitive tape-location detector for improved tape life; air bearings and Tribaloy coated read-after-write heads to reduce tape wear and improve data integrity, Model 9300 is ideal for minicomputer and data collection applications requiring complete reliability at high tape speeds.

Model 9300 comes complete with all the operational features of the 9000 Series. Performance is guaranteed by crystal controlled timing, read threshold scanning, our read-after-write shortened skew gate and other exclusive Kennedy features. Operation is simplified by such operator-oriented features as a front-accessible test panel, quick-release hubs and simplified tape loading.

Model 9300 has a standard tape speed of 125ips, with data densities of 200/556cpi or 556/800 on the 7-track unit and 800cpi, 1600cpi or 800/1600cpi on the 9-track transport. The format is NRZI/PE.

Model 9300 is not only quick and quiet — it's very competitive. That's quite a lot, considering the Kennedy quality.

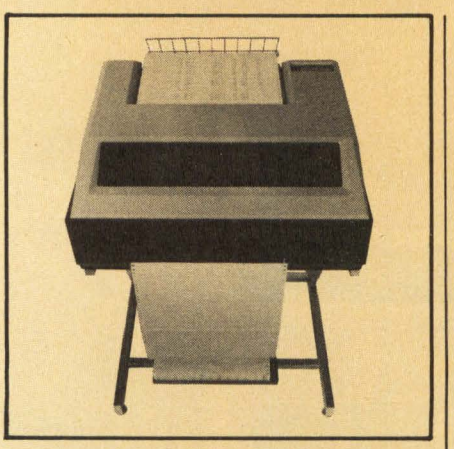
KENNEDY CO.
540 W. WOODBURY RD., ALTADENA, CALIF. 91001
(213) 798-0953

KENNEDY · QUALITY · COUNT ON IT

CIRCLE 2 ON INQUIRY CARD

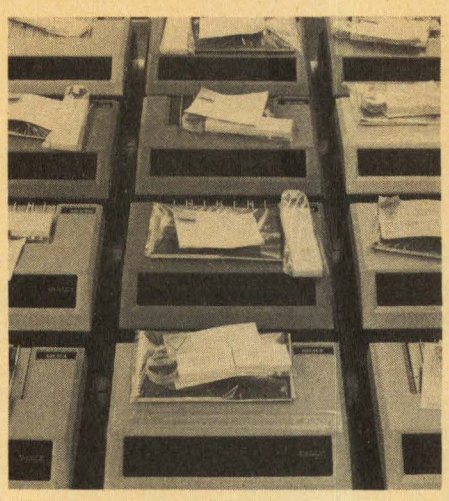
TALLY LINE PRINTERS AT NEW LOW PRICES.

As the volume builds, the prices drop.



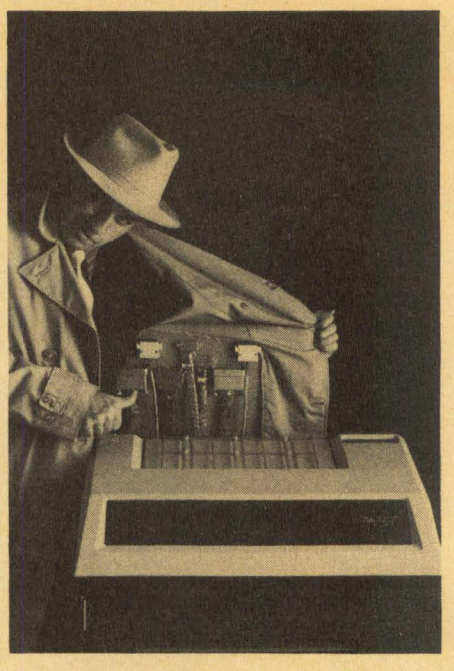
Significant Cost Reductions.

OEM's will realize substantial savings totalling hundreds of dollars. Quantity buyers — thousands of dollars. If you thought you couldn't afford Tally quality before, try again. Re-examine the low cost of ownership you get with Tally. Installation records prove the Model T-2200 requires far, far fewer maintenance calls than the competition.



10,000 Units Delivered.

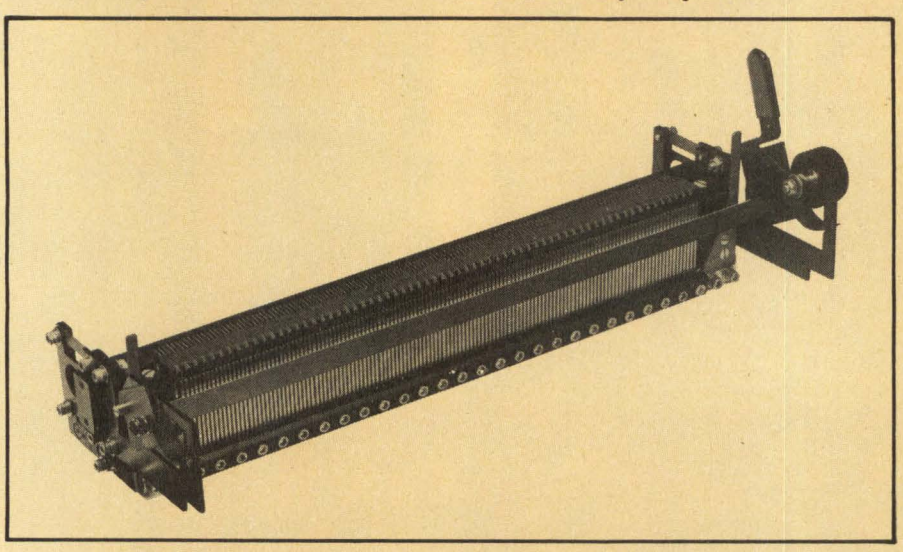
10,000 astute users is ample testimony to the field proven merit of the Tally reliability story. And now because production volume is up, we can pass along our quantity savings to you. And you, in turn, can offer your users the plus performance benefits of Tally line printers.



Interfaces? Lots of Them.

Whatever your mini, micro or remote terminal, the T-2200 works with it. For years, it has been running successfully with:

Data General	Prime
DEC	InterData
Hewlett-Packard	DCC
Lockheed	Intel
MicroData	. . . and many others.



Zero Maintenance.

Tally's unique comb matrix printing technique is the reliability key. Belts, clutches, lubrication points are eliminated. Never any adjustments. Nothing moves if the unit isn't printing. No duty cycle limitations. No preventative maintenance except routine cleaning. A one year warranty.

★ CALL TODAY ★

Get in touch with your nearest Tally sales representative for the new prices. And remember, the more units you buy, the bigger the price reduction. Tally Corporation, 8301 S. 180th St., Kent, WA 98031, Phone (206) 251-5524.

Regional Offices:

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New York (516) 694-8444
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Los Angeles (213) 378-0805
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San Jose (408) 247-0897
Seattle (206) 251-6730

TALLY

CIRCLE 3 ON INQUIRY CARD

THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

DECEMBER 1976 • VOLUME 15 • NUMBER 12

FEATURES

DEPARTMENTS

BPA **CIRCULATION OVER 55,000**

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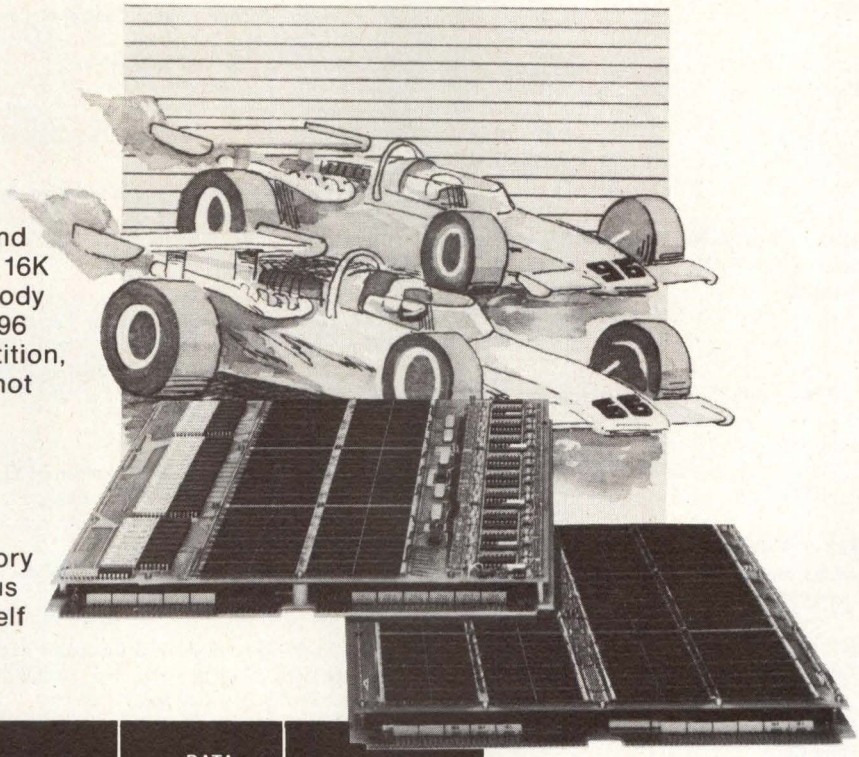
Who's the performance winner in 16k and 32k memory systems?

Check the specs.



Fabri-Tek has packed more speed and total performance into single-board 16K and 32K memory systems than anybody else in the business. Compare our 696 and 698 systems against the competition, and you'll see what we mean. We'll not only beat them in specifications—we're the only company that offers you total upward compatibility to 32K. At competitive prices, too. It's what you'd expect from a company with years of leadership in the memory business. Go with the winner—call us today for the best in both off-the-shelf and custom memory systems.

	FABRI-TEK		EMM		DATA PRODUCTS		DATA RAM	
MODEL	696	698	Micro 3000 D.D.	Micro 3000 Q.D.	Store 1680		DR-103	DR-103
MEMORY SIZE	16K	32K	16K	32K	16K	32K	16K	32K
CYCLE TIME	650	650	650	850	650		650	750
ACCESS TIME	250	250	270	300	280		265	300
PHYSICAL SIZE	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0		11.5x13.7 x1.0	11.5x13.7 x1.0
COMPATIBILITY 16K TO 32K	YES		NO		NO		NO	

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CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

JAN 10-14—Data Communications Equipment Exhibition, U.S. Trade Center, London, England. INFORMATION: Anita F. Brownstein, Dept of Commerce, OIM, United Kingdom, Washington, DC 20230. Tel: (202) 377-4443

JAN 18, FEB 14, and MAR 15—Invitational Computer Conf, Orange County, Calif; Fort Lauderdale, Fla; and Palo Alto, Calif. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

JAN 31-FEB 2—5th Annual ACM Computer Science Conf, Atlanta, Ga. INFORMATION: Vladimir Slamecka, Dir, School of Information and Computer Science, Georgia Institute of Technology, Atlanta, GA 30332

FEB 4—Tenth Technical Sym, U of Southern Calif, Los Angeles, Calif. INFORMATION: Mike Callahan, Conf Chm, Los Angeles Chapter of ACM, PO Box 90698, Los Angeles, CA 90009

FEB 7-9—WINCON 77 (Winter Convention on Aerospace and Electronic Systems), North Hollywood, Calif. INFORMATION: H. S. Abrams, Guidance & Control Systems, Litton Industries, 5500 Canoga Ave, Woodland Hills, CA 91364

FEB 16-18—IEEE Internat'l Solid State Circuits Conf, Philadelphia, Pa. INFORMATION: Lewis Winner, 152 W 42nd St, New York, NY 10036. Tel: (212) 279-3125

FEB 24-25—Sym on Design Automation and Microprocessors, Palo Alto, Calif. INFORMATION: W. M. vanCleemput, Gen'l Chm, Digital Systems Laboratory, Stanford University, Stanford, CA 94305. Tel: (415) 497-1270

FEB 28—Conf on the New Computer Science and Engineering Curricula, Jack Tar Hotel, San Francisco, Calif. INFORMATION: David C. Rine, Gen'l Chm, Computer Science, The U of Texas, San Antonio, TX 78285

FEB 28-MAR 3—COMPCON '77 Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAR 2-6 and MAY 18-22—Hobby Electronics Fairs, Anaheim, Calif and Philadelphia, Pa. INFORMATION: Aaron Kozlov, Project Manager, ISCM, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

MAR 9-11—DATACOMM 77, Washington, DC. INFORMATION: Carol Iredale, DATACOMM 77, 60 Austin St, Newtonville, MA 02160. Tel: (617) 964-4550

MAR 14-16—Second Annual Control of Power Systems Conf and Exposition, Texas A&M U, College Station, Tex. INFORMATION: Dr B. Don Russell, Tech Program Chm, Texas A&M University, Electrical Engineering Dept, College Station, TX 77843. Tel: (713) 845-1423

MAR 16-18—Tenth Annual Simulation Sym, Tampa, Fla. INFORMATION: Chm, Tenth Annual Simulation Symposium, PO Box 22621, Tampa, FL 33622

MAR 16-18—27th IEEE Vehicular Technology Conf, Orlando Hyatt House, Orlando, Fla. INFORMATION: Martin L. Barton, MP-437, Martin Marietta Aerospace, PO Box 5837, Orlando, FL 32805

MAR 21-23—IECI '77 Conf (Industrial Electronics and Control Instrumentation), Philadelphia, Pa. INFORMATION: W. W. Koepsel, Program Chm, IECI '77, Dept of Electrical Engineering, Kansas State U, Manhattan, KS 66506. Tel: (913) 532-5600

MAR 23-25—Fourth Annual Computer Architecture Sym, College Park, Md. INFORMATION: Dr Bruce Wald, Superintendent, Communications Science Div, Naval Research Laboratory, 4555 Overlook Ave, Washington, DC 20390

MAR 28-30—Data Communications INTERFACE '77, Fifth Annual Conf and Exposition, Georgia World Congress Center, Atlanta, Ga. INFORMATION: DataComm INTERFACE, Inc, 160 Speen St, Framingham, MA 01701. Tel: (617) 879-4502

MAR 28-31—IEEE Internat'l Semiconductor Power Converter Conf, Orlando, Fla. INFORMATION: Eberhart Reimers, Gen'l Conf Chm, USAMERDC, AMXFB-EA, Electrical Equipment Div, Fort Belvoir, VA 22060. Tel: (703) 664-5596

MAR 29-31—Computer Systems and Technology Conf, U of Sussex, England. INFORMATION: Conf Dept, Institution of Electronic and Radio Engineers, 8-9 Bedford Sq, London WC1B 3RG England

APR 6-8—Microcomputer '77 Conf and Exposition, Oklahoma City, Okla. INFORMATION: Dr S. C. Lee, School of Electrical Engineering, U of Oklahoma, Norman, OK 73019

APR 6-8—Digital Processing of Signals in Communication, Loughborough, UK. INFORMATION: Institution of Electronic and Radio Engineers, 8-9 Bedford Sq, London WC1B 3RG England

APR 12-14—Internat'l Reliability Physics Sym, Caesars Palace, Las Vegas, Nev. INFORMATION: George Ebel, Singer Co, Kearfott Div, 150 Totowa Rd, Wayne, NJ 07470. Tel: (201) 256-4000

APR 13-15—Interactive Design Systems Conf, Stratford-upon-Avon, England. INFORMATION: Computer Aided Design Centre, Madingley Rd, Cambridge CB3 0HB England

SEMINARS

DEC 20-22 and JAN 10-12—Engineering Applications of Minicomputers; DEC 20-22 and JAN 17-19—Effective Use and Application of Minicomputers; and JAN 12-14—Minicomputer Programming and Interfacing Techniques, Newton, Mass, Kansas City, Mo; New York, NY, Pittsburgh, Pa; and Phoenix, Ariz. INFORMATION: Institute for Advanced Technology, Control Data Corp, 6003 Executive Blvd, Rockville, MD 20852

SHORT COURSES

JAN 10-12, FEB 7-9, and MAR 7-9—8080A Microprocessor Hardware and Software Design, Lexington, Mass. INFORMATION: Diane Y. Michel, Technical Staff, NEC Microcomputers Inc, Five Militia Dr, Lexington, MA 02173. Tel: (617) 862-6410

JAN 10-14—Data Communications Via Fading Channels, JAN 15-FEB 26 (Saturday Mornings)—Practical Digital Design and Applications, and JAN 24-26—Integrated Circuits and Applications, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

JAN 11-14, JAN 18-21, and FEB 8-11—Microprocessors in Manufacturing and Industrial Control, and Software Development Tools and Techniques for Microcomputers; JAN 25-28 and FEB 1-4—Military and Aerospace Microprocessor Systems, and Bit-Slice Microprocessors, PLAs, and Microprogramming, Cincinnati, Oh, Toronto, Canada, Newark, NJ; and Houston, Tex, Boston, Mass. INFORMATION: Integrated Computer Systems, Inc, 4445 Overland Ave, Culver City, CA 90203. Tel: (213) 559-9265

JAN 12-13—Semiconductor Memories and Magnetic Bubble Devices, Fairleigh Dickinson U, Teaneck, NJ. INFORMATION: M. J. Sablik, Physics Dept, Fairleigh Dickinson U, Teaneck, NJ 07666. Tel: (201) 836-6300, X451

More than 4300 of our Cartridge Tape Drives are in use today. Each and every one, an Intelligent Choice.

Mohawk Data Sciences is a pioneer in cartridge tape drives. Since our introduction of this ultra-compact, amazingly capable piece of equipment, MDS has sold more cartridge tape drives to OEM's than anyone else in the business. Quality and value are the major reasons why. We're first in sales—and we'll stay that way—because decision-makers everywhere consider MDS the intelligent choice.

Versatility. You've got it with the MDS 2021/2022 Cartridge Tape Drives. Use them for low-cost intermediate storage for mini-computers. Use them as peripherals for remote data collection, communications terminals, and POS systems. Whatever the usage, count on MDS' engineering excellence and product leadership to back up every job completely.

We've packed in the features. 30-ips read or write, 90-ips search and rewind, read-after-write check, 800-1600 bpi, and phase or biphase encoding on 1, 2 or 4 tracks (total capacity of up to 23 million bits). Plus—a fixed position, dual-gap read-after-write head, interchangeable circuit cards, and a long-life motor that won't let you down.

4300 MDS units are out there now doing the job. A proven record. What better reason to follow the leader! What better reason to make your intelligent choice MDS. For additional details, call or write your nearest MDS, OEM Sales Office.

CIRCLE 6 ON INQUIRY CARD

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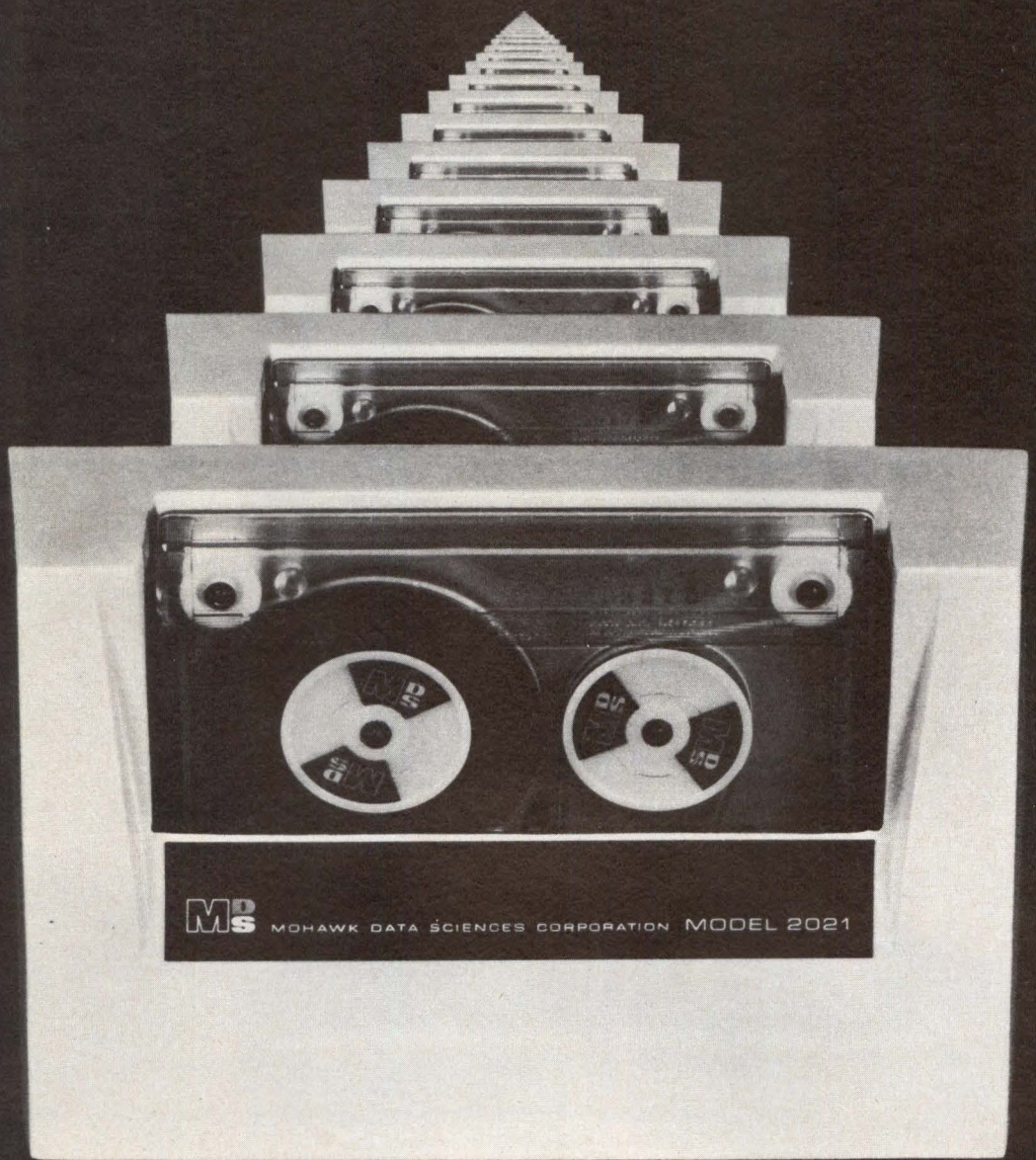
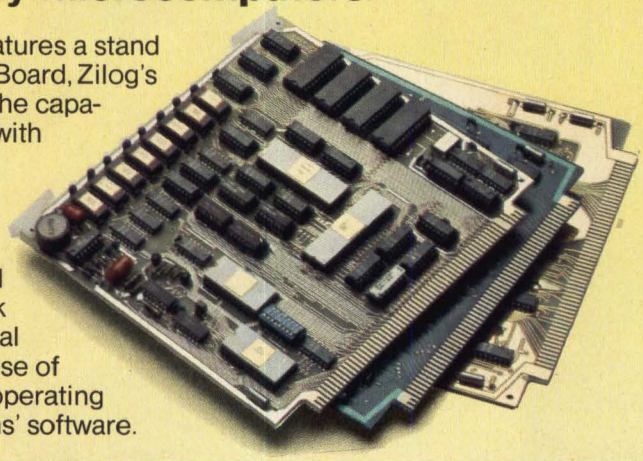


More weapons for The Battle of the 80's

Now a multiple attack against outmoded, large and bulky microcomputers.

This multiple attack features a stand alone Microcomputer Board, Zilog's mighty MCB, that has the capability to communicate with both serial and parallel I/O devices, has its own RAM and ROM capability and is backed up by a second board containing a disk controller and additional memory allowing the use of Zilog's complete disk operating system and applications' software.



Announcing the Z80-MCB. An assault against big board computers.

A single 5-volt power supply does it. And it's small—only 7.7 x 7.5 inches with a standard 122 pin edge connector with 100 mil spacing that is designed for ease of use.

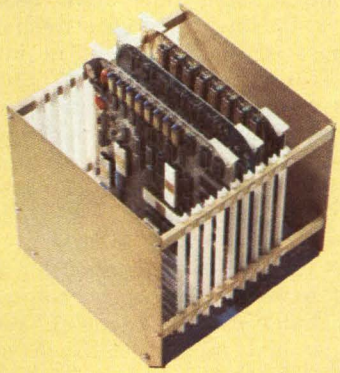
A squad of fighters against obsolete hardware.

Here's what Zilog's new weapon gives you:

- Z80-CPU single-chip n-channel processor with 158 instructions.
- 19.6608MHz crystal oscillator divided to 2.457MHz for Z80-CPU operation and dividable by Z80-CTC to provide any other desired system frequencies.
- 4K bytes dynamic RAM.
- Capacity for 4K bytes on non-volatile memory.
- Programmable serial I/O port with RS-232 or current loop interface.
- Universal parallel I/O with two independent 8 bit ports.
- Z80-CTC for programmable baud rate generation or other user functions such as real time clock.
- Bus drivers are provided for memory and I/O expansion to other boards.
- One-half K-byte monitor software has terminal handler, load and punch routines as well as set and display memory commands. A GoTo command begins execution of user programs. The 1K-byte version adds more debug aids such as set and display registers and breakpoints. The 2K and 4K-byte versions include a floppy disk controller and even more debug capability.

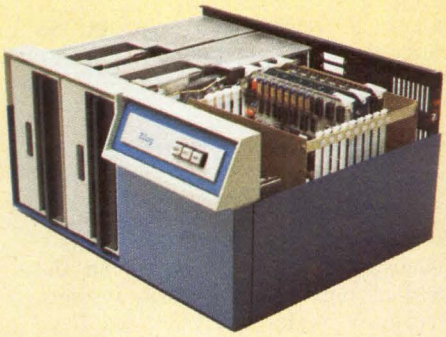
A second board gives you the advantage.

A second board gives you a 4-drive floppy disk controller and additional RAM backed up by a full disk operating system. Plus, you get the applications software you need: file, edit, assemble, debug, and high level languages such as BASIC, and more will be announced soon. This second board contains 12K of dynamic memory and additional 8 bit programmable parallel I/O ports.



Both cards are easily interfaced in a simple, low-cost card cage.

The Mighty Weapon: Zilog's Z80-OEM System.



Start out with a strong front and get performance unmatched by any other microcomputer system in the field.

You get:

- Z80-MCB Microcomputer Board
- Z80-MDC Disk Controller/Memory Board with disk controller capability for up to 4 floppy disk drives.
- Z80-RMB 16K-byte RAM Board with memory expandable to 64K bytes in 16K-byte increments.
- Z80-SCC Standard Card Cage holds up to 9 P.C. cards.
- Z80-MCS Microcomputer System includes a standard card cage, up to 2 floppy disks, power supplies and a push button front panel.

A versatility of attack: you can buy only as much as you need.

We provide a modular approach to complete computing and processing systems. Zilog products are available as a basic CPU card, a card set or a complete self-contained computer with floppy disks and power supplies in one unit.

Behind all this is Zilog's pledge to stay a generation ahead. We're the specialists who are responsible for the development of the most successful first and second generation microprocessors. And we're hard at work on the next step—an advance that will keep us out in front in The Battle of the 80's.

Appropriate assistance will be dispatched upon your written request or telephone call.

CIRCLE 7 ON INQUIRY CARD

Zilog

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LETTERS TO THE EDITOR

To the Editor:

We are writing to discuss a new space research opportunity which appears of likely interest to your readers. The Universities Space Research Association (USRA), an international consortium headquartered at Rice University in Houston, Tex, has as members over 40 universities active in space research. We are administering a new program under the sponsorship of NASA which is aimed at broad participation of the academic community in space research. Our purpose is to solicit, evaluate, and assist in the development and management of space experiments for the Long Duration Exposure Facility (LDEF), a part of the Space Shuttle Transportation System.

LDEF satellites, which will be launched at periodic intervals beginning in late 1979, will carry a large number of experiments into orbit. Each LDEF satellite will remain in orbit for six to nine months, then will be retrieved by another Space Shuttle and returned to earth. LDEF offers long exposure to the orbital environment of micro-gravity, vacuum, radiation, and particle fluxes, together with return of materials and instruments to their owners at the end of the mission.

We are interested in inquiries and proposals for experiments both from experienced investigators and from those who have not had prior space flight research experience or opportunities. Under our program, NASA funding is not available through the Office of Aeronautical and Space Technology, which manages the LDEF program. However, integration and a "free ride" have been promised for those experiments which are approved under the USRA program (christened "LDEF/USE" for University Space Experiments) and whose development can be funded in some other way. We seek research proposals in widely diversified subject areas from both the academic community and private industry (so long as an industrial experimenter is willing to be a member of a team that includes academic people). We are interested in subjects such as microprocessors, in which your readers may be particularly conversant. We offer a flexibility and opportunity for space flight that is new in the Space Program.

Dr Robert S. Corruccini
LDEF/USE Communications Coordinator
Universities Space Research Association
PO Box 3006
Boulder, CO 80303

(Ed Note: Anyone interested in this space research opportunity should contact Dr Corruccini directly.)

To the Editor:

Only in the first week of July 1976, a year after publication, did the article "Cyclic Sequence Generator Increases Security of Alarm Systems" by Ramesh Krishnaiyer and John C. Donovan, *Computer Design*, July 1975, pp 73-77, come to our attention and from it we first learned of another article, published by the same authors in the April 1973 issue of *Computer Design* ("Shift Register Generation of Pseudorandom Binary Sequences," pp 69-74), which we have subsequently received and read.

We thought it might be of great interest to your readers to learn something of our company even though it is not located in the United States. Our activities are specifically in the field of high security alarm systems, inasmuch as for 29 years we have specialized in detection systems and line transmission systems for the Canadian banking community. The appointment of a new manager for our Research and Development Engineering Section, Mr Z. Siemiatkowski, in 1970 brought a breath of fresh air into our approach to electronics even though a system for telephone line transmission, which had been designed and manufactured by our company since 1963, had not been and has not to this day been electronically compromised. The nature of the design of this older system indicated that the rapid advance in electronics could make it obsolete against possible compromise by criminal activity at some time in the reasonably near future. Therefore, a move was made to establish an entirely new line transmission system.

In the early 1970s Canadian banks urgently needed a surveillanced electronic system for the internal wiring within their bank branches which connects the control box (which is normally secured within a reinforced concrete vault) to the various supplementary systems such as holdup, night depository, exit doors, etc. For this purpose we introduced in 1972 an entirely new random digital system. Over the next two years this system was considerably modified and improved to the point where we were able to make a further leap forward in new technology.

In late 1974 it became obvious that there was an urgent need to drastically upgrade the telephone line system against criminal compromise, because, as the authors of your previous articles say, "The line of communication between an area protected by an alarm system and its central monitoring area *is the most accessible and most vulnerable link in the system.*"

Quite independently from outside information (as we have said your articles were unknown to us), we produced a 2-way random digital code system which we have made *absolutely random*. Not only do we provide each system with its unique feedback loops and shift registers so that the random sequence generation of the codes for each installed location is completely different from that of any other installed location, but we have introduced a further design feature. This consists of an entirely new input which ensures that even when the number of bit shifts start to repeat, dependent of course upon the length of the shift register and the feedback connections for that particular installation, the new sequence will not match the previous one on a totally irregular and irrational basis. This prevents even a computer

Introducing The compact 1 from number 1:

The minifloppy™ from Shugart

Give your system the performance of a floppy at a cassette price. Gain the random accessibility, mechanical reliability and data integrity of a flexible disk in a more affordable size. Go minifloppy.

This little half-pint is half the size, half the cost of a standard floppy but Shugart packs a lot of proven technology into that itty-bitty box (3.25″ x 5.75″ x 8.0″).

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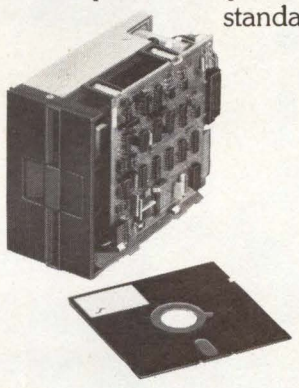
Special minifloppy drive features include direct drive stepping motor actuator, DC servo-controlled spindle drive, and less power dissipation than any standard floppy.



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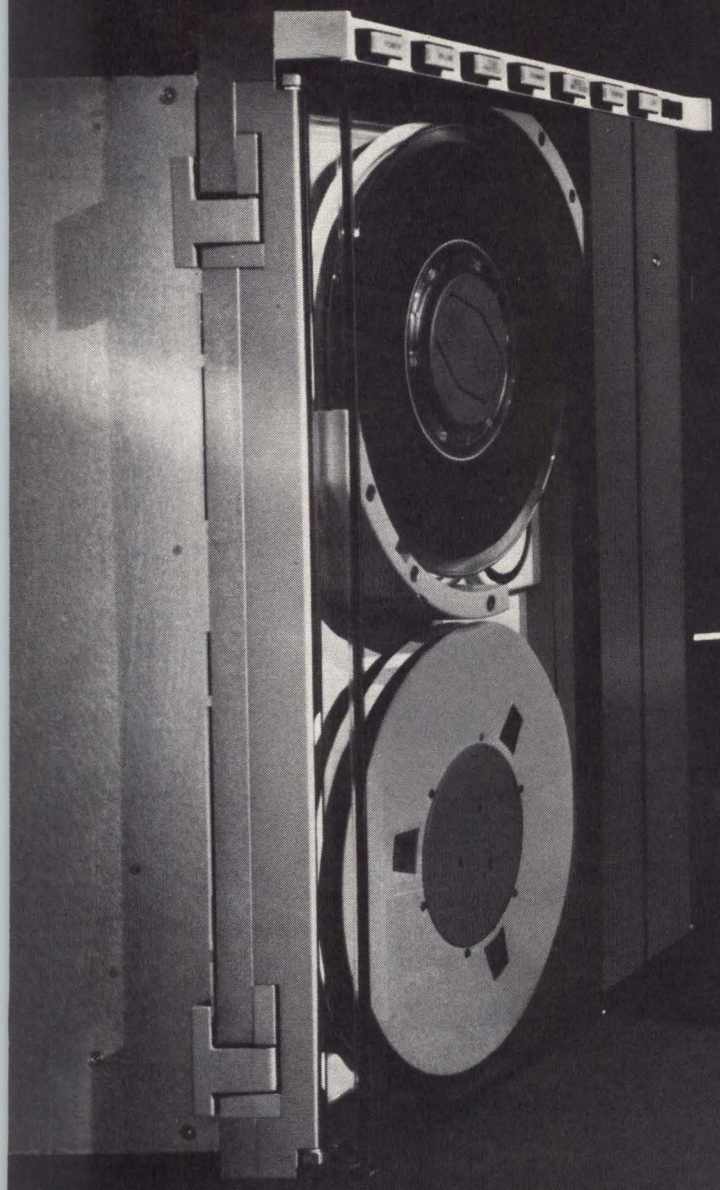

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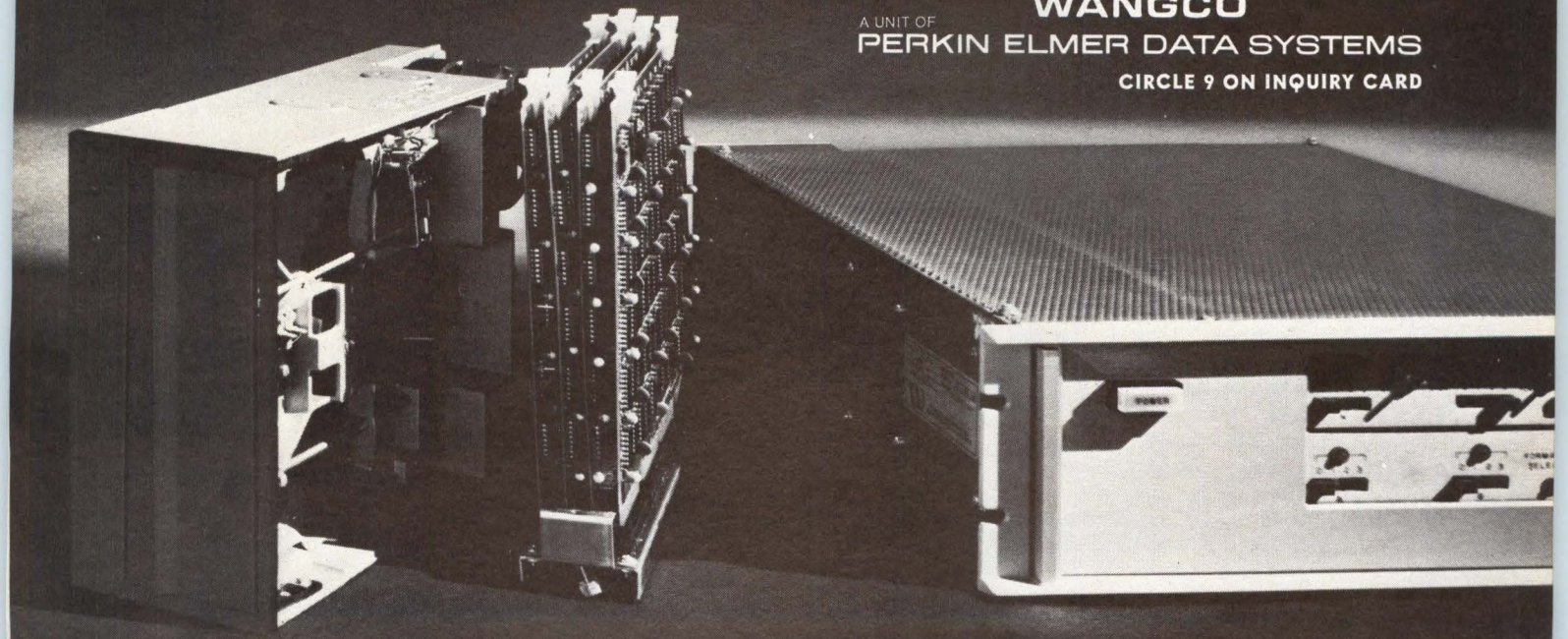


analysis of that particular and individual code formula.

In the article "Cyclic Sequence Generator Increases Security of Alarm Systems" under the heading "Defeat Techniques," we have noted the opening remark, "No security is inviolable." We would certainly endorse this statement and would never wish to guarantee against compromise at some future date. Nevertheless, we are at a complete loss at this juncture to ascertain how the system could in fact be beaten, inasmuch as no rational analysis can be made! It is certainly true that resynchronization is a vulnerable problem and one method of dealing with it is to ensure that whenever it is reset, a new starting point is used for each resynchronization. However, we have taken an entirely different though somewhat costly approach, by ensuring that both the transmitter and receiver remain in identical synchronization for a long period of time, even though completely separated by a total breakdown of the communicating telephone line. The duration of this synchronization ability is of course a security secret but exceeds an amount of time that our thirty years of experience with alarm telephone line failures indicates to be necessary. Therefore, any criminal who attempts to force the resynchronization of the system after a line break, whether short or long, is completely wasting time! We rather think this is the ultimate system to the security requirements on the telephone line, added to which we have achieved the rather remarkable transmission distance of at least 250 kilometers (150 miles) on the minimal grade of telephone or telegraph line available, without requiring intermediate amplification.

I have personally made considerable explorations in both Europe and North America to ascertain if this system is currently being manufactured and installed anywhere in the world by any other company, but I cannot find one. We are therefore presently claiming ourselves as "world leaders in the security of telephone line transmission for alarm systems," a challenge which I throw out to your readers! Our first bank installation in Canada with this new telephone line transmission system took place in September 1975 and we already have installed over 300 of these systems spread across our whole 4000-mile wide nation, from the Atlantic to the Pacific and in all ten of its provinces.

We have recently provided this equipment to the Swedish banks through E. A. Rosengrens AB of Gothenburg who hold the franchise for our product throughout Scandinavia. It has not only met the exceedingly high standards set in Sweden by those authorities who are responsible for the security of their banks, but has also been accepted by the post office, telephone, and telegraph authorities in that country.

A. J. M. Collins
Amplitrol Electronics Ltd
Candiac, Quebec
Canada

To the Editor:

In the February 1976 issue of *Computer Design*, pp 77-85, the article titled "Trends in Computer Hardware Technology," by David A. Hodges, briefly mentions the comparative cell sizes of RAM (MOS), CCD, and magnetic bubble memories (MBs). The author assumes "that pattern definition techniques allow a certain minimum feature size (Δ)." (See Fig. 7 in the article.) His conclusion is "that RAM and CCD have comparable maximum (bit) densities, while the CCD fabrication process is slightly more complex" (assuming also a 1-bit CCD cell). In addition, the author provides figures leading to the assumption that magnetic bubble density is 3.75 times less than either of the other technologies. The conclusion reached, therefore, could lead the average reader to believe that CCD and MB memory storage densities (measured in either cells or bits per square unit) are not superior to current n-MOS RAM technology. This belief is not shared by many other authors, for example as shown in Refs. 1 and 2.

The Information Technology Div, Institute for Computer Sciences and Technology, at NBS, Gaithersburg, Maryland, has done in-depth surveys of charge-transfer and magnetic-domain devices. These are to be published as two documents titled "Foreign and Domestic Accomplishments in Magnetic Bubble Device Technology" and "Foreign and Domestic Accomplishments in Charge-Transfer Device Technology." These surveys include both extensive literature searches as well as interviews with various U.S. technical experts. The conclusions of the article by Mr Hodges are not shared by many other authors of related literature which is cited in these studies.

When comparing CCD and RAM technologies, one finds that CCDs do not require diffusions and contact openings throughout their array structures as do MOS RAM devices. This means that CCD memories can be manufactured (due to inherent simplicity) with higher bit densities at higher yields or larger chip sizes than is possible when using more conventional MOS circuits. One large U.S. company, in fact, is reported to be including CCD cell structures in their MOS RAMs and is expecting significant breakthroughs toward the next level of complexity above the soon-to-appear 16-kilobit (RAM) device.[1,3,4]

With regard to magnetic bubble devices, it is true that MB memories are currently manufactured by leaning heavily on silicon LSI manufacturing techniques. But, the magnetic chevron cell does not require the same edge definition that is necessary for most silicon LSI circuits. Much coarser guide patterns have relatively little effect on bubble dynamics,[5] but in the case of the RAM, such structures could cause catastrophic failures. In any case, there are indications that magnetic bubble technology is moving away from "linewidth patterns" and is searching for topologies that are more congenial to both the bubble and the fabrication techniques. One source proposes a double-sided track consisting of coarse dots while another source is working on self-structuring propagation techniques; the former method places the magnetic bubble cells in the submicron region.[5,6]

A recent technical forecast of RAM, CCD, and MB memories shows the following areas that are required for containing one bit of information.

RAM (4096 bits–MOS): 4 to 5.5 square mils

CCD: 1.4 to 1.6 square mils

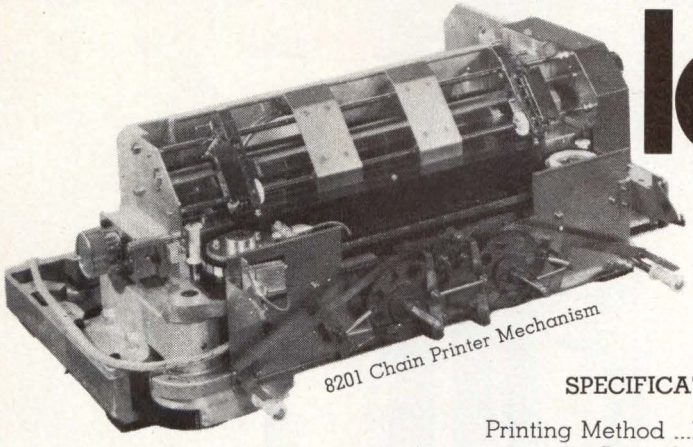
MB: 0.2 to 0.4 square mils (0.01 by 1980)

It is reported that one major manufacturer of MBs is currently making 100K bits on a garnet chip, at silicon LSI yield rates, by using conventional contact photolithography.

Continuous improvements in LSI fabrication techniques are foreseen;

Heavy-duty 300 LPM-132 COL.

Chain Printer Mechanism at low cost.



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Printing Method ...Print train, flying hammer
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Number of characters.....48, 64 or 96
Character spacing .....10 characters/inch
Line spacing .....6 lines/inch
Width of print paper .....Max. 16 inch
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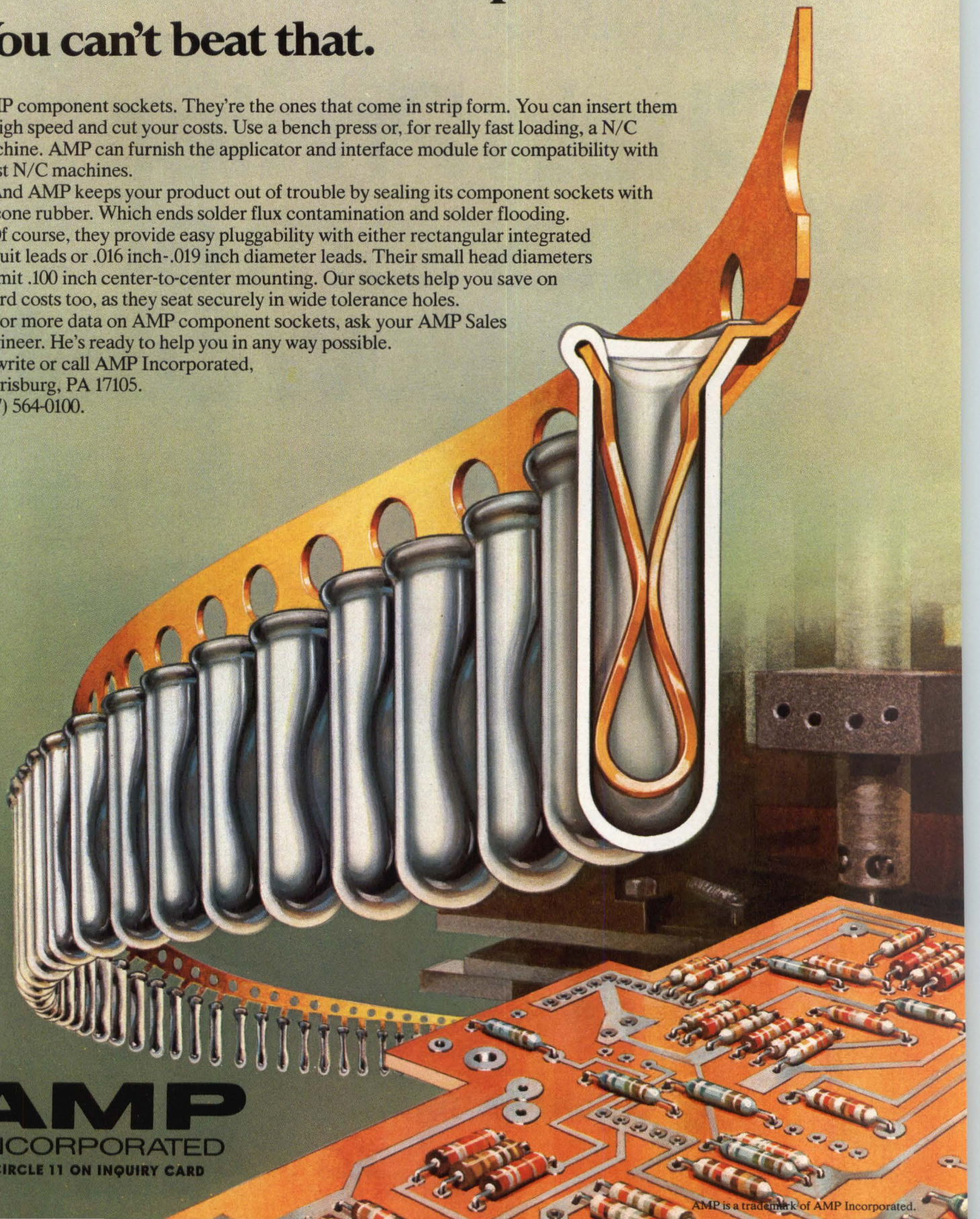

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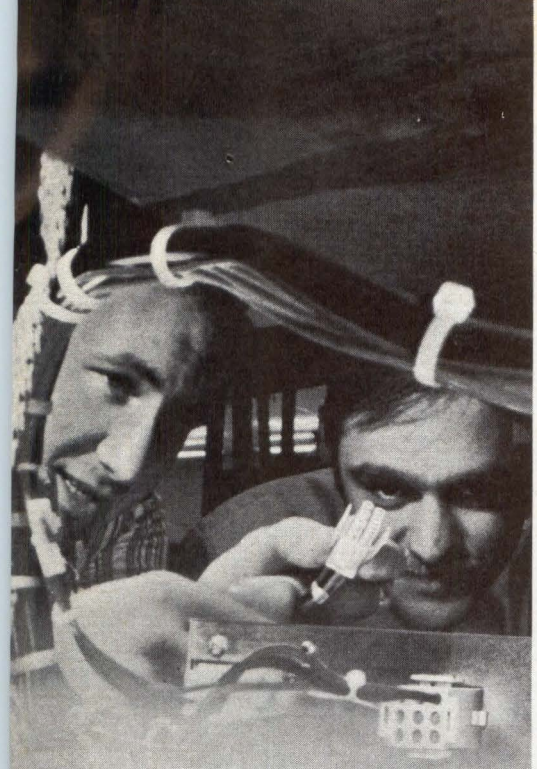

the practical (linewidth) limit of electron beam lithography is currently about 0.4 micrometers. This suggests that future solid-state memories can encounter other obstacles in the quest of improving bit storage densities. Defects arising from lithographic and diffusion processes will continue to be more significant in limiting the performance of silicon-based devices in comparison with garnet-based MB devices in which diffusion is not required and the lithography is relatively simple, regardless of the minimum linewidth achievable at any given time.[7,8]

The statement that "in fact, RAM may always have a cost advantage simply because its development is already advanced" is true today. However, over 18 major magnetic bubble device manufacturers and many large silicon device manufacturing facilities all over the world are trying hard to change that situation.

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Letters to the Editor should be addressed:

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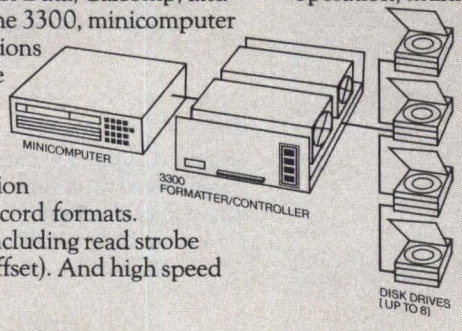

Other 3300 features include multiple drive capability (up to 8), seek overlap operation, multi-record transfers, internal data encoding and decoding, alternate track sparing, and FIFO buffering. Plus additional performance characteristics to facilitate maintenance and configuration flexibility.

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by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Local System Access

Much has been written concerning techniques and guidelines for providing nationwide access to centralized processing centers. The term data communications or data networks tends to stimulate visions of continental communications channels constantly attempting to achieve an optimum balance between economics and effective operation. The vast portion of the efforts to engineer and operate an online data network has been clearly focused on the long distance between a centralized computer and geographically dispersed remote data terminals.

This attention has certainly been warranted by the ever increasing costs for such data networks coupled with the greater dependence of the given application on the reliability and timeliness of these networks. Primary data networks traditionally have represented direct remote terminal to computer configurations. In recent years, with the advent of intelligent networks, the primary data network also includes the inter-node communications channels. Concentrated networks which encompass remote multiplexers or concentrators are typically configured in star configurations. Circuits which interconnect these remote concentration or cluster locations to the central processing center comprise the primary data network.

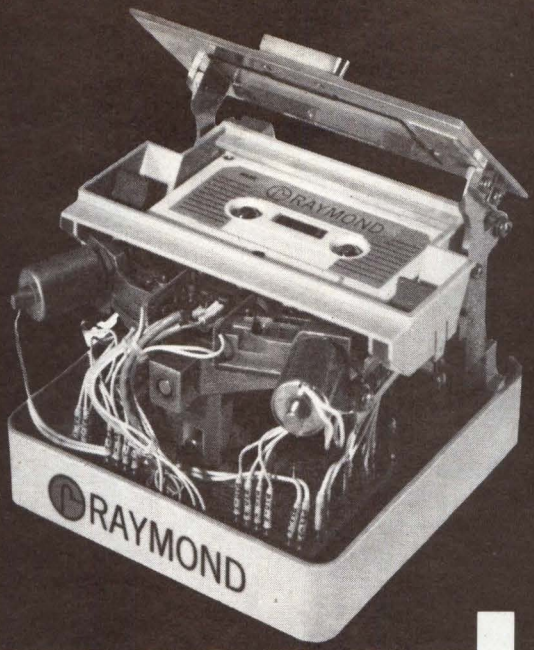
This network has been, and presently is, the sole objective of many data network studies and analyses. Virtually all network modeling and simulation techniques address only this primary data network. Since it typically does encompass a significant geographic area, a major network expense on a recurring monthly basis is always associated with it. This continuing investment and the dynamics and diversification of the present Federal private line tariffs have contributed to the focus on the primary data network and perhaps the neglect of the secondary data network.

The secondary network is not actually a separate entity for those information systems which utilize direct remote terminal to central processor connections. In those systems the primary and secondary data networks are synonymous. Intelligent or concentrated networks, however, have totally unique network considerations for the interconnections between remote terminals and their associated nodes or concentration centers. This area of local system access can properly be termed the secondary data network. Factors and alternatives that must be considered and evaluated apply equally to secondary data networks as well as to any local processing centers that only provide access to remote terminals in the same urban or city area as the processing center.

Admittedly, the primary network easily overshadows the secondary network with respect to economic factors. Monthly charges associated with the primary network can be an order of magnitude greater than the monthly cost of all secondary data networks. In the area of reliability or probability of abnormalities, however, the secondary network can typically exhibit a far greater proportion of data errors or circuit malfunctions. Even though the primary data network has a significantly greater geographical exposure, its data transmission quality and reliability can be multiple orders of magnitude better than the same parameters characterized by its associated secondary networks.

In the design of many data networks, the basic criteria or guidelines for network decisions are defined for the requirements and characteristics of the primary data network. These guidelines are then automatically applied to the secondary network without an individual evalution of its needs; secondary networks which provide local system access can present unique system requirements. In addition, local provisions of many state tariffs can provide facility alternatives that may permit system access at surprisingly low cost. It is important that each local system access area be carefully documented and analyzed for any centralized information system. Available communications facility and tariff alternatives can profoundly affect the selection of the actual data terminals, the anticipated data flow procedures, and even the intelligent node or concentration equipment and programming. Improper decisions in the design and implementation of the local system access will rarely manifest themselves in an inoperative or catastrophically impacted application. It will provide, however, continual undefinable data errors, network malfunctions, and random system access interruptions—all of which weakly point to a number of other system causes.

As in the design of any network, two prime objectives must be realized: lowest communications cost and highest reliability. As with the much longer distance requirements of the primary data network, both switched and leased connections or communications channels can be used in the secondary network. Unlike the primary network though, only one supplier is available: the local telephone company. The system designer must also realize that for each city in which a local system access is to be established, the communications tariff



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provisions and rates will be different. No longer is the tariff application simply a question of federal or state jurisdiction; each local area has a unique definition of communications services and rates for connections within that area.

Leased lines from each remote terminal to the local system access center are commonly used. The rationale for this typically represents an automatic design decision because leased lines were used in the primary data network. Local leased lines should only be used on a point-to-point basis: one remote terminal on one local leased line connected directly to the local system access center. The only justification for a multipoint leased line is to reduce line costs. Sharing of a common leased line, however, imposes a triple burden by requiring that terminals operate at data rates higher than necessary, include the necessary logic or intelligence to respond to network control procedures such as polling, and are willing to be dependent on the common shared line for the necessary system access.

If the local system access center has only a limited number of ports, the decision to use local multipoint lines may appear to be justified. Assuming that time division multiplexers (TDMs) are being used, the ability to reduce the per terminal data rate connected on a point-to-point basis can typically increase the number of possible TDM ports. Consider a leased multipoint line from a remote TDM operating at 2400 bits/s, shared by eight local data terminals. Each terminal is operating only at an effective data rate of 300 bits/s. If each data terminal was directly connected on its own line to the local system access center, the reduced TDM port data rate would correspondingly increase the number of potential TDM ports. Eight local leased lines typically will cost more than the 8-point local leased line. The monthly cost differential is usually minimal and is more than offset by simplified data terminal operation and increased ability to isolate local line malfunctions.

In most systems the use of local leased lines can be totally eliminated. The alternative is to interconnect the data terminals and local system access center by using switched or dialed connections. The local system access center, as a concentrator or node, should be designed to permit point-to-point connection with its associated data terminals. The data terminal usually dials the local system access center only when data exchange is to take place. Using the norms and guidelines of the primary data network, a switched or dialed connection implies a continually growing usage charge as long as the connection is maintained. For long distance communications this axiom is totally true. On a local communications basis, it can be totally false.

Many metropolitan areas charge a flat monthly rate for access to the switched telephone network. That charge, which can be $20 to $30, is independent of actual usage. A remote data terminal can dial up an all-day connection to the local system access center for no additional charge or penalty. The same techniques can even be applied in urban areas that employ a system of message unit ratings for local calling revenue. A slightly more detailed examination of the local message unit tariff provision is required. In a typical large city a low switched telephone network access charge of $10 allows intracity calls to be made for one message unit each, regardless of length. With message units being charged at $0.06, the total monthly connection charge would be $1.20 with the data terminal connected eight continuous hours each day. If the system permitted continuous connections, the data terminal could dial a one-month connection for the monthly charge of one message unit.

Surrounding cities that utilize message units are suburban zones that operate on a multi-message unit basis. Local dialed connections into these areas accumulate message units as the connection duration continues. It is important that the one-month connection is not inadvertently made to a multi-message unit area—in such cases the addition of a short mileage foreign exchange service to the nearest single message unit exchange may be justified. It is also possible in some localities that a higher fixed monthly charge can extend the no message unit or single message unit areas.

A local system access area generally represents the least sophisticated and oldest equipment and channel resources of the local telephone company. It is therefore the most likely source of data errors or circuit malfunctions, and usually takes the longest to diagnose and repair. If switched or dial access is used, a suspected error producing a line condition or connection malfunction can be eliminated by merely redialing the connection. This ease of bypassing the problem can be of particular significance when the local system access center is unattended.

It is extremely important that the system designer consider the associated data network as being a 2-tier configuration. The secondary data network is subject to operational and regulatory factors that are sufficiently unique to warrant their thorough evaluation. In this manner unique system economies and flexibilities can be realized.

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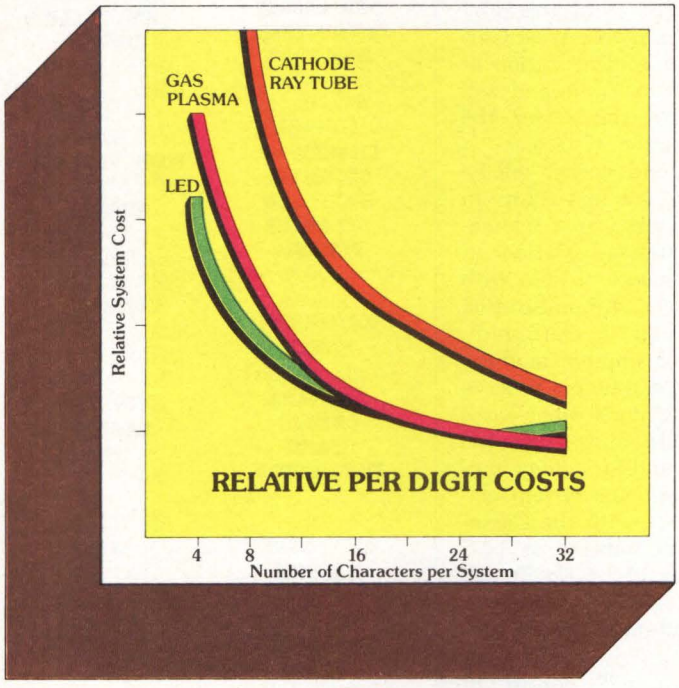
Read our FREE Reliability Evaluation Report.

Our new QA Reliability Report is now available, covering all the quality assurance features of the MAN2A. It details how Monsanto ensures quality and reliability, which ensures maximum cost saving advantages for you—now and in the future.

It is absolutely FREE—simply mail the coupon for fast response.



Monsanto: the science company.

IN EUROPE CONTACT: Monsanto Europe S.A., Electronics Division, Avenue de Tervuren 270-272, B-1150, Brussels, Belgium

Send me your FREE Reliability Report and specifications on the MAN2A LED display.

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Company _____ Street _____

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Mail to: Monsanto Electronics Division
Dept. MCD, 3400 Hillview Ave., Palo Alto, Ca. 94304
Phone (415) 493-3300

CIRCLE 16 ON INQUIRY CARD

Satellite System Will Provide Sudanese Domestic Communications

A satellite communications system intended to provide domestic communications throughout the north African nation of Sudan, the SUDOSAT system will cover the nation's 967,500 sq mile area. The $29 million turnkey system will be built and installed by Harris Corp, Communications and Information Handling, Cleveland, Ohio.

Principal part of the system will consist of 14 earth stations and communications complexes. Supplied by the Harris' Satellite Communication Unit, they will be installed at sites across the Sudan and will have both receive and transmit capability. The system will also include 13 color-TV broadcasting stations, five telephone exchanges, and a 200-kW AM radio station. The first three earth stations are scheduled for installation in February and March of 1977.

Switched Network To Offer Private Interstate Communications Services

The first step toward building a private coast to coast telephone and data network for interstate communications customers has been taken by ITT Corporate Communications Services, Inc, a subsidiary of International Telephone and Telegraph Corp, New York City. Using this network, planned for operation by January 1978, the company will provide switched private network service (SPNS) for small users, and Corporate Communications Switching Equipment (CCSE) for large customers.

Under a $13.5 million contract for computerized switching systems, Rockwell International, Collins Commercial Telecommunications Div, will provide systems in Atlanta, Ga, Chicago, Ill, Cleveland, Ohio, Dallas, Tex, Los Angeles, Calif, Memphis, Tenn, and New York City—the seven cities forming the basic network. A computer-controlled network management center will administer and maintain the network on an automated real-time basis.

Service features planned for customers using SPNS service over the high volume switched network include privacy, detailed per-call billing, traffic statistics, desk-to-desk dialing, abbreviated dialing, hotline service, conference calls, and project billing for specific sub-billing amounts.

Planned CCSE services will allow users to custom-design their own network using switching innovations in conjunction with transmission facilities they own or lease from another common carrier. Features of this service are planned to include 100% automatic message accounting, network conferencing, on-net to off-net calling, alternate routing, common channel interswitch signaling, and centralized traffic statistics.

Satellite System To Be Tested For Use As Ship-to-Shore Facility

To overcome problems caused by atmospheric disturbances in short-wave range ship-to-shore communications, the European Space Administration is planning to test a satellite communication system for use in this application. The MAROTS (Maritime Orbital Test Satellite) is being tested under a project financed by the German Aeronautical and Astronautical Research Institute. In connection with this project, Siemens AG, Erlangen, West Germany will set up a control station at Villafanca del Costillo, Spain and will develop an onboard station for the satellite communication system.

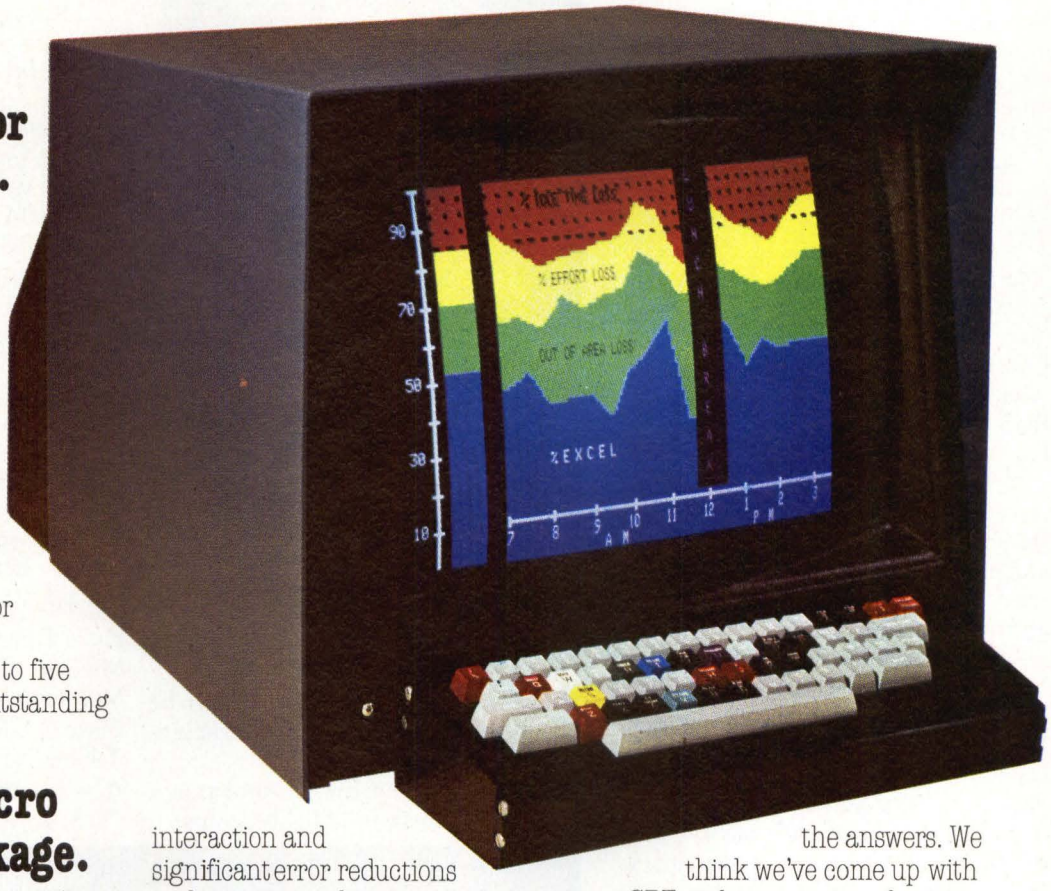
The Spanish ground station will be equipped with an antenna 12-m in diameter and will serve as a telemetering and telecommand station as well as for the exchange of data with the European Space Administration (ESA) control center in Darmstadt. With installation of suitable modulation equipment the station could serve on a trial basis to contact other earth stations via satellite and to switch voice, Telex, data, and facsimile channels to ships. The antenna system, designed in accordance with the Cassegrain principle, will transmit at 14.5 GHz and receive at 11.7 GHz. It will be directed at the satellite via its own internal aiming system or under program control.

Onboard stations will consist of transceiver (I/O equipment, modems, frequency generator, receiver, and sender); the antenna together with its stabilizing and direction system is being developed by Dornier. Onboard terminals will operate at a 1.6-GHz transmit frequency and a receive frequency of approximately 1.5 GHz. Transmitter power will be approximately 40 W.

Onboard stations are expected to be ready for installation by the middle

The Intecolor® 8001

It's an 8-Color Intelligent CRT for $1995.* Or a Micro Computer for an additional $1495. The choice is yours.



A $1995 8-Color CRT. Complete.

When we say complete, we mean complete. The **Intecolor** 8001 has 8080 CPU, 4K RAM Refresh, Selectable Baud Rate to 9600, Keyboard, RS232 I/O, and ASCII Character Set. All in one package. It's a complete stand-alone system which features our unique **Intecolor** 8001 NINE SECTOR CONVERGENCE SYSTEM for minimum set-up time and exceptional stability. Three to five minutes is all it takes for outstanding color registration.

The $1495 Micro Computer Package.

You just give us the word and we'll convert the **Intecolor** 8001 into a stand-alone micro computer with BASIC, Roll, Insert/Delete, Additional 8K RAM Work Space, Graphics Mode with 160X192 Elements, Background Color, Lower Case ASCII, 48 Line X 80 Characters/Line, and 2X Character Height. Plus additional features which make your **Intecolor** personal computer the best buy in the industry.

Which System Is Right For You?

The **Intecolor** 8001 CRT is a smart, inexpensive way to upgrade the CRT's in your present system from black and white to color. And color has definite sales advantages. Like more efficient man-machine interaction and significant error reductions in data entry and recognition. The **Intecolor** 8001 CRT can also be used or marketed as a complete stand-alone micro computer system with computation or control capabilities. It might even replace your whole system!

Whatever your needs, market or application — Process Control, Medical, Credit Checking, Order Entry, Financial Analysis, Research and Development, or for your own personal computer — you won't find a more usable terminal, color or black and white.

Write Or Call For More Information

We know you're going to have some more questions, and we've got the answers. We think we've come up with a CRT and computer package that's hard to beat. And one thing for sure. The **Intecolor** 8001 is by far your best buy today in a color CRT micro computer or intelligent terminal. Make us prove it to you with a demonstration by one of our authorized representatives. Or call us direct and talk to an applications engineer.

Intelligent Systems Corp.®
5965 Peachtree Corners East
Norcross, Georgia 30071
Telephone (404) 449-5961

*Quantity 100 Price.
Unit Price $2,495. Domestic USA Prices

CIRCLE 17 ON INQUIRY CARD

LOGIC BOARD TESTING DOES NOT DEMAND SOFTWARE PROGRAMMERS, AND LOTS OF MONEY.

There is a foolish notion in logic board test circles that says, "Plan on spending all the budget you have, plus a lot more, to get logic board testing results."

What nonsense.

Why, that's as bad as the arguments for testing in the end product. Is there no middle ground? You know, a good testing system for a fair price.

Of course there is. And we built it.

It's our 3000 Series Logic Testers. The 3020A is a console for high-volume production applications. It comes complete with 128 pins for under $30,000*. The 3010A is a compact version for field service and low-volume production at less than half the price.

O.K. So why no high cost?

Most testers share one major shortcoming: the cost and complexity of programming. As logic boards become larger and more complex, test engineers anxiously reach for more computer power and more software.

It just isn't necessary.

The fact is that tediously developed, bit-by-bit sequences are now past history. Instead, we provide powerful groups of general-purpose sequences with various duty cycles and frequencies. Boards respond to them. Their mathematical qualities honor the constraints of your circuits and the laws of logic.

Specifically, the 3000 Series Testers have seven classes of signals. Over 350 unique bit streams and their complements are available to exercise the most complex boards.

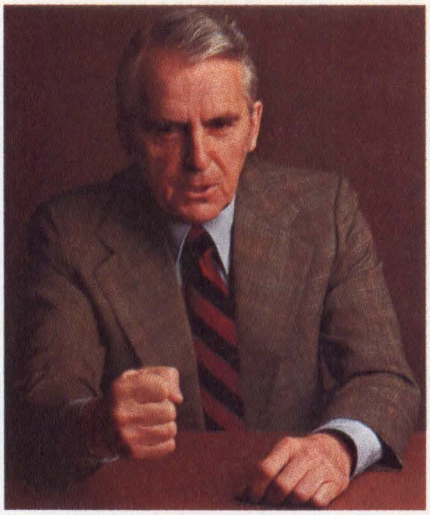
And, where a specific sequence is needed, it is easily added.

The test engineer doesn't program in the conventional sense. He simply develops a test plan which consists of selecting the appropriate stimulus algorithm for each input.

We've pre-programmed the CPU, simplified the peripherals, and eliminated 80% of the programming. That's what keeps the cost down.

The beautiful part is that test confidence ends up higher.

And fault isolation is just as practical as the price. It's hard to imagine



"Prove it."

any other tester making more common sense.

Test program assignments and editing are made on-line by pushbutton. Program debugging is simple. Whenever a pin number is entered, the sequence assignment is displayed. Sequences can be changed simply by depressing the appropriate pushbutton.

Again, there are no assemblers or compilers to fuss with. Highly comprehensive programs are completed in hours, not days or weeks.

And once the test program is entered into memory, you can record it easily on a handy little magnetic credit card that looks exactly like those credit cards in your wallet. The programmed card will function interchangeably with the production Model 3020A, or the field service 3010A.

Maybe we've made our point.

You can get a tester that offers four million tests per second, test sequences to 40 million words, and programmable logic levels without subsidizing a computer center and staff of programmers.

We'll prove it to you in dollars and cents.

Write and ask for "The Economics of Logic Board Testing." Everything you need is there to get you into logic board testing. Economically, for a change.

For data out today, dial (415) 965-0350.

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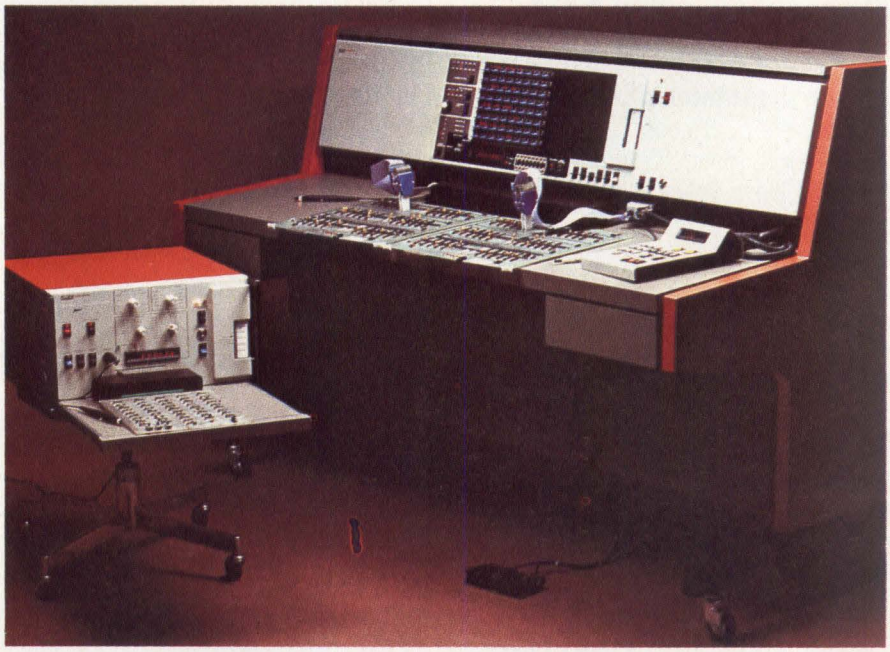
Fluke (Nederland) B.V., P.O. Box 5053, Tilburg, The Netherlands. Phone: (013) 673-973 Telex: 52237

**U.S. price only*



COMMON SENSE 3010A/3020A TESTERS. FLUKE®

of 1978, when MAROTS will be ready for trial ship-to-shore and shore-to-ship communication. By the early 1980s, sufficient information and experience should be at hand to determine whether satellite communications are feasible for use in maritime applications.

Dual-Band Satellite Will Strengthen Canadian Communications Position

Scheduled for launch during 1978, the ANIK-B will join currently operational satellites as part of the first commercial domestic satellite communication system. Described in a paper presented by Robert W. Hoedemaker, RCA Astro-Electronics Div, Princeton, NJ and Derek G. Thorpe, Telesat Canada, Ottawa, Canada, at WESCON in September, the satellite will provide dual-band capabilities which will serve to strengthen Canada's position in the worldwide aerospace and telecommunications industry, by providing commercial communications services in the 14- to 12-GHz frequency band.

One transponder subsystem will furnish 12 channels in the 6- to 4-GHz band, making the satellite's operation compatible with frequencies used by existing Telesat earth facilities, and furnishing capability for handling color television, voice, and data communications traffic for Canada's 10 provinces and two territories. The other transponder subsystem will operate in the 14- to 12-GHz band. This band is planned for initial use by the Communications Technology Satellite (CTS), a joint Canadian-U.S. program. The CTS will test technology and application of new types of high powered orbiting transmitters and will allow scientists to evaluate needs and uses for the communications services such equipment makes possible. The satellite's capability to operate with CTS earth stations will enable the high frequency experimental tasks to be continued into the 1980s. This cooperation between the government and Telesat in development of communications applications in the 14- to 12-GHz band will ensure that Canada is in position to take full advantage of any improvements resulting from the experiments.

The 6- to 4-GHz transponder is made up of three functional parts: broadband receiver driver, multiplexers, and traveling-wave-tube amplifiers (TWTAs). Input multiplexers channelize the receiver output for amplification by TWTAs. Output multiplexers combine outputs of the TWTAs for transmission to antennas. The receiver driver converts the 6-GHz received signal to the 4-GHz band and amplifies it to the drive level required for the TWTA. Input to each redundant receiver has a bandpass filter which provides at least 60 dB of isolation to frequencies in the 4-GHz band. Since ANIK-B is a dual-band satellite, a low-pass input filter must be used to ensure adequate attenuation of 12-GHz signals which may radiate from the 14/12-GHz antenna into the 6/4GHz antenna receive input.

Two input multiplexers separate the amplifier signals into 12 rf channels spaced by 40 MHz. Output of each TWTA is connected to one of two output multiplexers. Each combines six TWTA outputs with each channel on 80-MHz centers. After passing through a low pass filter, the multiplexer output is connected to one of two antenna input ports. Communications operation in this band is provided through a single antenna reflector and a triple feed-horn system.

The 14/12-GHz transponder is based on CTS technology and flight-qualified hardware. Its three main functional parts are broad-band receiver, multiplexers and routing networks, and TWTAs. Input multiplexers and routing networks channelize output of the receiver for amplification by TWTAs. Output multiplexers and routing networks combine outputs of the TWTAs for transmission to one of the regional beams.

A receiver driver converts the 14-GHz received signal to the 12-GHz band and amplifies it to the drive level required by the TWTA. Prior to entry into the receiver, the input signal passes through a 500-MHz bandpass filter. At the input to the receiver, the signal is amplified by a parametric amplifier before being translated 2300-MHz to the 12-GHz band. Further broadband signal amplification is achieved by field-effect-transistor amplifiers (FETAs). Redundant receivers and FETAs can be separately selected by ground command. FETAs drive the TWTAs through the input multiplexer and routing networks. Communication in the 14/12-GHz band is provided by an antenna reflector and horn support tower that is separate from the 6/4-GHz system.

RCA Astro-Electronics is designing and building the spacecraft for Telesat Canada. RCA Limited (Canada) will provide the transponder payload and antennas. Under the $9.1 million contract RCA will also supply earth telemetry, tracking, and command equipment for an earth station at Allan Park, Ontario.

Electronic Switching System Can Complete 240,000 Calls Per Hour

Capable of completing 240,000 calls per hour, the No. 1A ESS developed by Bell Laboratories uses an information processing control unit to provide the necessary operating speed for use in large capacity central offices serving metropolitan areas. Bell System planners estimate that the electronic switching system (ESS) along with its processor's retrofit capability will result in cost savings of $500 million by 1990, through reduced construction and maintenance for additional switching facilities.

Designed to be retrofitted into existing No. 1 ESS machines, the 1A processor executes instructions at the rate of 1.4 million/s, compared with 180,000/s for the currently used processor. It has an electronic memory which includes a replaceable program of instructions that tells the entire system how and when to execute its functions. This stored program control allows additional requirements to be incorporated quickly into the switching system, simply by changing program instructions. The processor is capable of diagnosing problems while they are developing in its own circuits. It can then switch to alternate equipment before the problem becomes evident to customers, and alert maintenance forces to repair or replace the defective equipment.

The No. 1A ESS includes the 1A processor along with the peripheral equipment of the No. 1 ESS. The processor has been tailored to existing units since at least 90% of the frames in a typical switching office are identical to those in the No. 1 ESS. This allows the processor to be retrofitted into in-service units if call-handling capacity needs to be increased. It can replace existing processors without interrupting service.

Since the processor can operate independently of the switching network, it can be installed and tested while the present processor handles calls. Following testing it can be connected and the present processor removed. The replaced processor can then be reused in a switching office that has less stringent call-handling requirements. □

Interactive Display System Supports Distributed Processing, and Provides Powerful Graphics Capabilities

An intelligent interactive computer graphic display system that incorporates two programmable microprocessors, the Graphic 7 supports distributed processing (local or remote operation), and provides powerful graphic capabilities at low cost. Compatible with most computers, and adaptable for use in commercial or military applications, the system provides display image, generation, refresh storage, data entry device handling, cursor control, and communication with the host processor via functional messages; one system can drive three CRT displays.

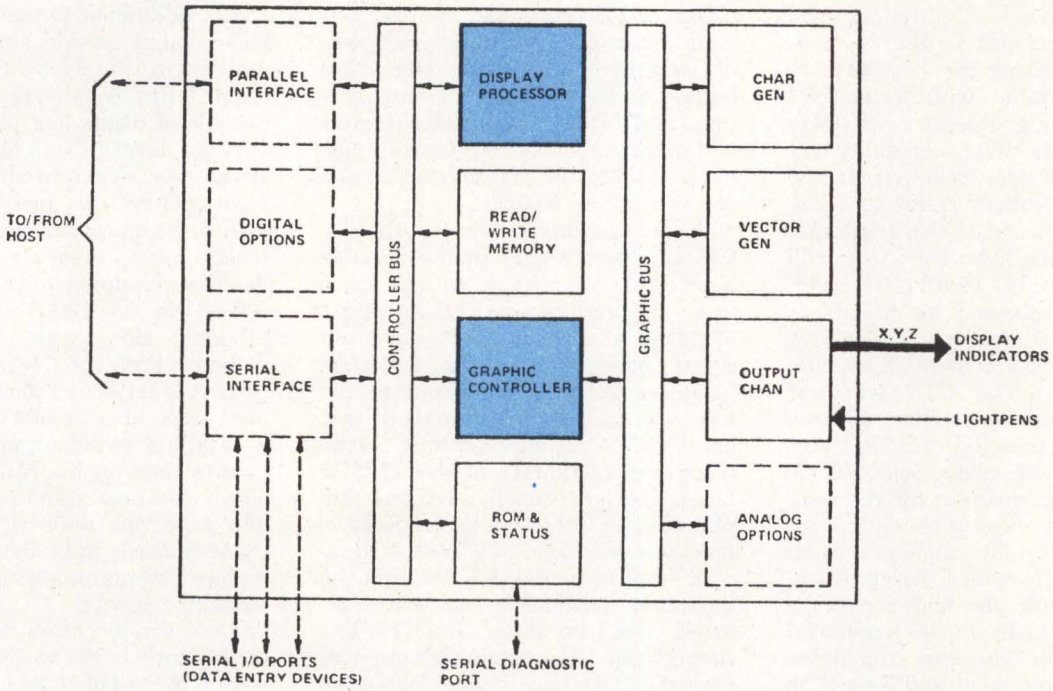
Developed by Sanders Associates, Inc, Daniel Webster Hwy, S, Nashua, NH 03060, the system interfaces to the host via RS-232 or high speed parallel interface, and can be operated as easily as an ordinary desktop computer terminal. It does not require program loading from the host.

Basic system is composed of terminal controller, 21" CRT display, and input devices such as keyboard, lightpen, and trackball. The system is preprogrammed for interactive operations.

In local mode, the operator can examine a memory address, deposit data at the address, transfer program control to an address, transfer to system mode, or transfer to lightpen, keyboard, or test pattern terminal-verification mode. A 1-button initialize feature causes the system to automatically ready itself and allows the operator to communicate immediately with terminal or host computer. Automatic self-test and diagnostics are provided for fault isolation.

Heart of the system is the terminal controller which includes two bipolar microprocessors (MMI 6701), a display processor, and a graphic controller. A general-purpose unit which operates with 16-bit words or 8-bit bytes, the display processor has eight general-purpose registers and an 8K 16-bit read/write memory that is expandable to 24K in 8K increments. The Graphic controller, a 16-bit parallel microprocessor, provides 40 display instructions, 13 display registers, and four general registers as well as 60-, 40-, and 30-Hz refresh rates.

A 4K x 16-bit ROM in the controller contains the control program



Terminal controller within Sanders' Graphic 7 Display System incorporates two programmable microprocessors—functioning as display processor and graphic controller—that enable the system to be operated as easily as a desktop computer terminal

that handles communication between terminal and host computer, controls data entry devices, manages display image refresh, and performs other functions usually done in the host computer.

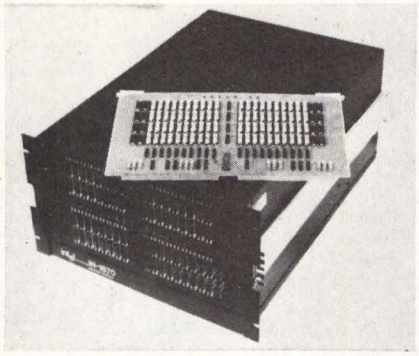
The firmware-committed graphic control program makes intrinsic terminal operations transparent to the user and minimizes host computer involvement in display functions. This frees the system programmer from the task of supporting the graphics terminal and allows him to concentrate on applications software. The task is further simplified by use of optional Graphic Support Software which allows applications programs to be written in FORTRAN.

The vector/position generator provides an array of 2048 x 2048 addressable locations on a 1024 x 1024 viewing area. Character generator furnishes the standard 96-char ASCII set or 32 user-defined characters as an option. The display is a 21" rectangular CRT which gives a 12 x 12" viewing area with a 4:1 contrast ratio. Position accuracy is ±1% of full scale, repeatability is ±0.1% of full scale.

Basic system price is $32,800. Additional equipment includes Photopen®, trackball, and multiple displays. A hardcopy unit is available for $17,000.

Circle 140 on Inquiry Card

Low Cost Memory System Offers 4M Bytes Add-On Capacity for PDP-11/70



Intel's in-1670 adds on up to 4M bytes of memory capacity to the PDP-11/70 computer. Measuring 10½ x 19 x 25", the memory installs directly into the computer's memory cabinet and provides four times the density of competitors

The in-1670, a low cost add-on memory system, offers up to 4M-byte capacity for PDP-11/70 users—four times as much as competitive products in the same physical space. Designed by Intel Memory Systems, 1302 N Mathilda Ave, Sunnyvale, CA 94086, the memory is totally hardware/software compatible with the computer, and has a 750-ns cycle time with 550-ns access.

Error correction checking and error logging circuits enhance reliability and maintainability. All single bit failures are automatically corrected. Double bit failures are automatically detected; the memory address containing the failure is recorded in internal hardware registers for later examination during preventive or corrective maintenance service.

The complete system, including memory cards, chassis, power supply, cooling fans, and controller, installs directly in the -11/70's memory cabinet without modifications. All voltages, currents, timing, and I/O signals are completely compatible with the computer.

A basic system contains 128K bytes and is expandable in 128K increments. Since it stores four times as much in the same physical space as the -11/70 memory, bus length limitations are eliminated, allowing a full 3,932,160 bytes to be installed and accessed by the user.

Circle 141 on Inquiry Card

Large and Medium Scale Computers Rival IBM Equipment

Designed to provide end users with an alternative to IBM while protecting their investment in people, programming, and training, two Advanced System central processing units have been introduced by Itel Corp, Data Products Group, One Embarcadero Ctr, San Francisco, CA 94111. Six models of AS/4 and AS/5 CPUs meet processing requirements of medium- and large-scale users, and cover a range of computing power from 1.4 times that of the System/370 model 148 to the equivalent of a System/370 model 158-3 MP.

The systems are operationally compatible with the model 158, permitting all existing operating systems, program products, and user programs to be run without modification. Serviceability, reliability, and availability have been extended by provision for reconfiguration, spare channel, and chip-level diagnostics.

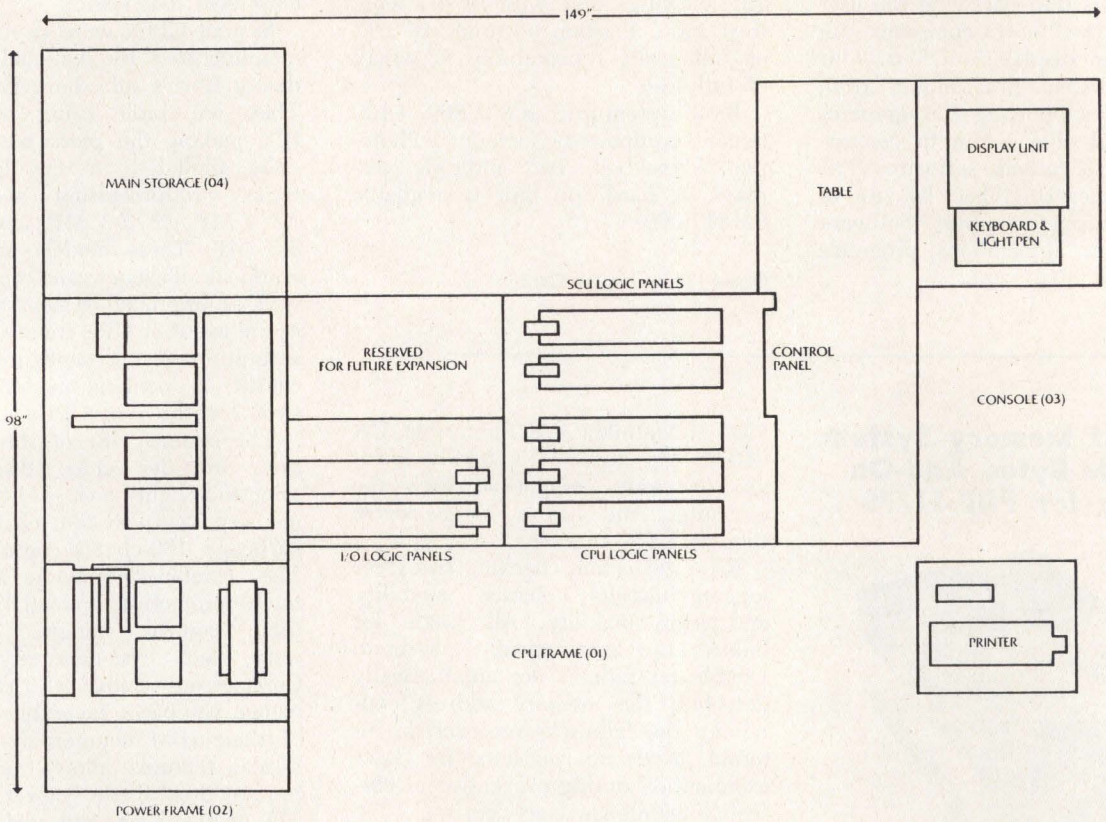
System CPUs were developed and manufactured by National Semiconductor Corp's subsidiary Exsysco Co. They are built using off-the-shelf ICs, making the parts readily available. Included in the family are three multiprocessing models, the AS/4 MP, AS/5-1 MP, and the AS/5-3 MP. These models provide operational efficiency and flexibility as well as improved system availability in the event of CPU failure. Although a multiprocessing configuration must consist of identical models, memory sizes for the two CPUs may differ.

The system's list of standard features includes video display console and light pen, 1M-byte main memory, seven system channels, and hardcopy 180-char/s console printer. The machines provide store and fetch protection, reloadable monolithic control storage, instruction retry, and byte-oriented operands. Comparisons indicate that performance compares favorably with that of their IBM counterparts. Technological features allow the units to require 45% of the power, generate 37% of the heat, and weigh 63% as much as IBM units.

Proven IBM System/360 and /370 architectural techniques are enhanced through the use of ECL and MOS circuits. These high speed circuits perform more functions (each component performs more functions due to higher circuit densities) than components used in equivalent systems. Use of these circuits reduces the number of components, resulting in lower system costs, greater reliability, and reduced space requirements. In addition, the systems run cooler, have half the power consumption, and are easier to service.

Models are field expandable—an AS/4 can be upgraded to an AS/5 without exchanging the CPU. Main memory sizes range from 1M byte to 8M bytes on single processors, to 16M bytes on multiprocessor configurations. Memory can be added in 1M-byte increments using modules formed from 4K n-MOS RAM components.

Six system channels and one spare channel are available in combinations of byte and block multiplexer channels. The standard reconfiguration feature allows users to dial out



Itel's Advanced System uses ECL and MOS components to implement System/370 architectural techniques. High density circuits provide high reliability as well as lower power consumption and 25% less floor space requirement than its IBM counterparts

any failing portion of memory, allowing the system to resume running after initial microprogram loading is complete.

All software currently available for equivalent System/370 models, including operating system and user programs, runs without change. The unit is functionally equivalent to the 158, allowing operators and systems programmers trained on the 158 to use the system immediately.

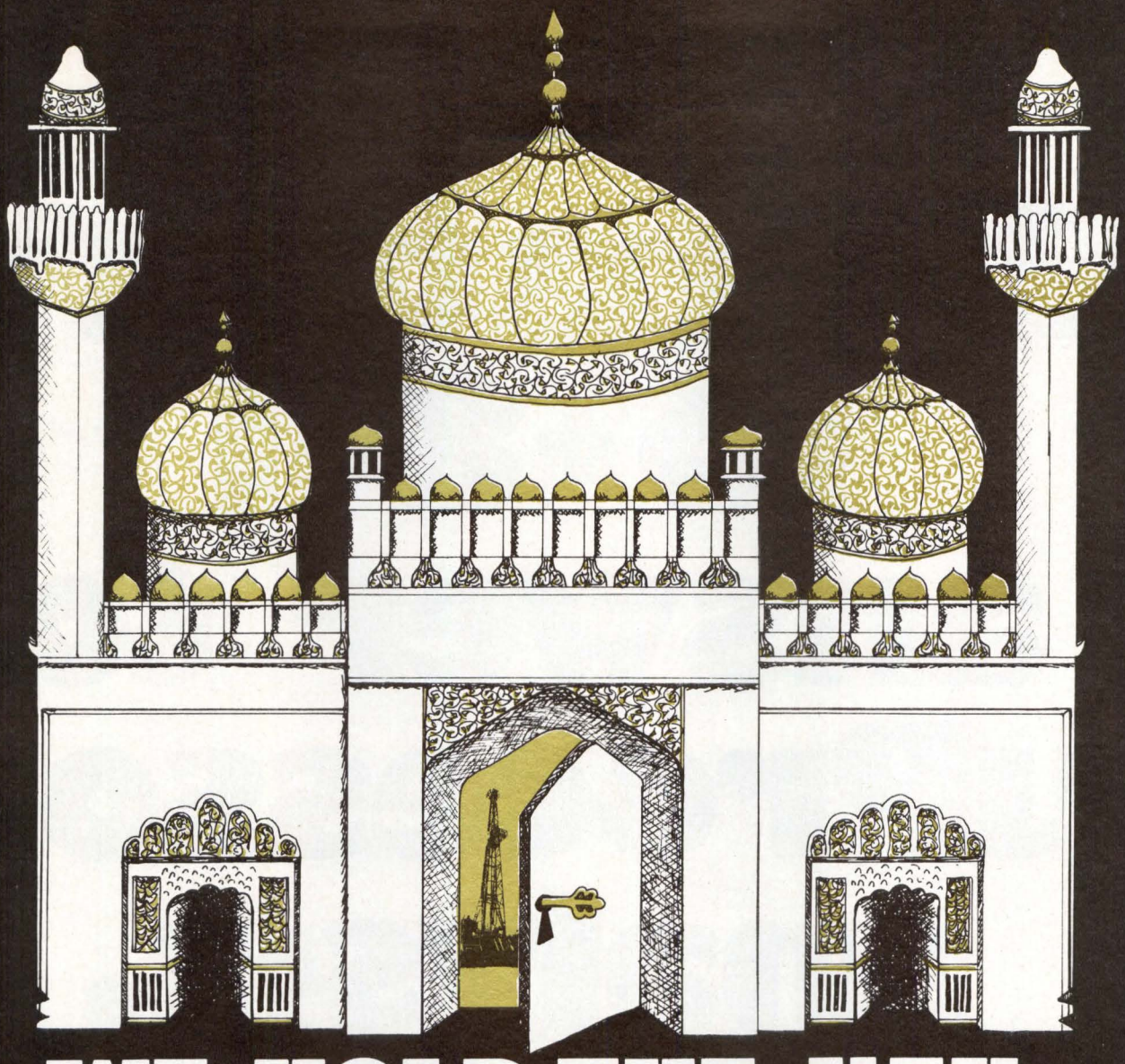
Reliability is enhanced by automatic hardware retry on most failing CPU operations, error checking and correction on main memory, I/O operation retry facility, channel retry, spare channel, and expanded error recording procedures. The reduced number of ICs and memory components minimizes malfunctions and by reducing heat generation allows the system to run cooler and therefore more reliably.

Serviceability is improved by the use of IC and memory devices which are plugged, instead of soldered, into removable circuit boards. Multiple boards are mounted on swingout gates for easy access. Diagnostics trace malfunctions to the chip level, allowing repair by merely replacing the failed component. A high level of component commonality allows a high level of onsite sparing.

Circle 142 on Inquiry Card

Time-Keeping System Permits Efficient Use of Flexible Work Schedule

A computer-based system that handles flexible and fixed working time systems, Multi-Tyme™ may solve the problem of declining worker productivity that confronts industry by permitting the effective initiation of flexible or variable working hours. Requiring no time cards, clocks, or other conventional timekeeping equipment, the system, manufactured by Cardkey Systems, a div of Greer Hydraulics, Inc, 20339 Nordhoff St, Chatsworth, CA 91311, electronically records and maintains a record of all



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Al-Omar Engineering Company is your Gateway to Middle Eastern marketing. Your only gateway.

Until recently, marketing American computer products in the Middle East was difficult. But now, through our import arrangements, we are in a position to accept the representation of dealerships and agencies throughout the Middle East.

Obviously, due to social and economic conditions, the Middle East is on its way to becoming one of the largest computer and peripheral equipment buying powers in the world. And our 60 years experience in dealing with various Middle Eastern public and private sectors will open this market to U. S. companies with the foresight to take advantage of this opportunity.

We offer offices and industrial and sales experience in the states of Kuwait, Iran, Iraq, Jordan, Lebanon, Qatar, Saudi Arabia, Sudan, Syria, United Arab Emirate, United Arab Republic and Yemen.

To discuss how we can open this door for your products, write us today.
Only our key can unlock the door for you.

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CIRCLE 19 ON INQUIRY CARD

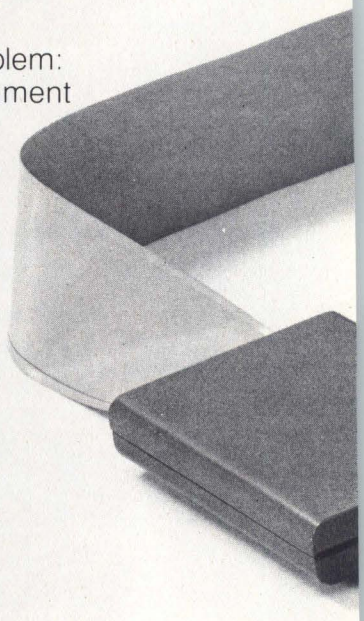
25-bit words:

Biomation's 16+8+1 answer to µProcessor analysis.

The first microprocessor analyzer that really analyzes.
Biomation has developed a new instrument to solve a new problem: How to get inside the mind of your microprocessor. The instrument is our 168-D. The Mind Reader.

In the process, we've invented a new word. 25 bits long. Contains 16 bits of address, 8 bits of data, and one bit that tells you whether your machine is reading or writing. All in hex characters, just like your program listing.

The Mind Reader starts by capturing up to 256 of those 25-bit words at synchronous rates as fast as 10MHz. That's fast enough for anybody. You can dial in a hardware breakpoint and step your system through its program. Or you can monitor your system as it runs free. But that's just the beginning. Now watch:



First, the Big Picture
The Mind Reader takes a first macro-bite out of the territory you're investigating. 256 big words. In Memory Mode you can see the areas of memory where the action occurred. (You're writing into ROM, for heaven's sake!?!)

Then zoom in!
The 168-D gives you a movable cursor that locks onto a location and stays with it through the analysis modes. Once you spot the action you've been looking for, stake it out with the cursor and switch to Page Mode. That gives you the address, data, and read/write information.

Now: A whole new perspective . . .
You've found the program, now switch to Sequential Mode and find out **how it got there.** Where were you coming from, and where did you go from there? Study all time relationships. A powerful new way to analyze the problem!

By switching to the List Mode you display the twenty words surrounding the cursor location you selected in the Page Mode. Address and data are presented in hex along with the R/W bit to let you compare the sequence to your program listing.

In summary: The 168-D lets you record with respect to time and analyze with respect to location.

It's the first microprocessor analyzer that really analyzes. You can put it to work today on **8080A** and **6800** problems. Personality modules for other μP's are currently under development.

So if you're working with microprocessors and want to know whether your software or hardware is giving you problems, Biomation's 168-D Mind Reader will tell all: What happened . . . where . . . and when. You've got to get the data sheet. Circle the number below. Better yet, call Biomation for a demo.
Biomation, 10411 Bubb Road, Cupertino, CA 95014,
(408) 255-9500.
TWX: 910-338-0226.

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The next generation microcomputer is our next industry standard.

The 4K. The 16K. Now the Z80.

High performance memories are a trademark at Mostek. The 4096 4K RAM and the 4116 16K RAM are both unsurpassed in performance and reliability.

Now Mostek introduces the Z80—a third-generation microcomputer that dramatically increases system performance over the 8080A. At the same time the Z80 reduces your total system costs.

High performance memories. High performance microprocessors. All from Mostek.

Increased system performance over the 8080A.

The Z80 outperforms the 8080A by providing more than 50% additional processor throughput with 25% to 50% less program storage space. This is accomplished using the expanded Z80 instruction set which includes all of the 78 instructions of the 8080A plus 80 additional instructions. Plus, there are 9 additional internal registers (including two 16-bit index registers) and special control circuitry for extremely fast interrupt servicing.

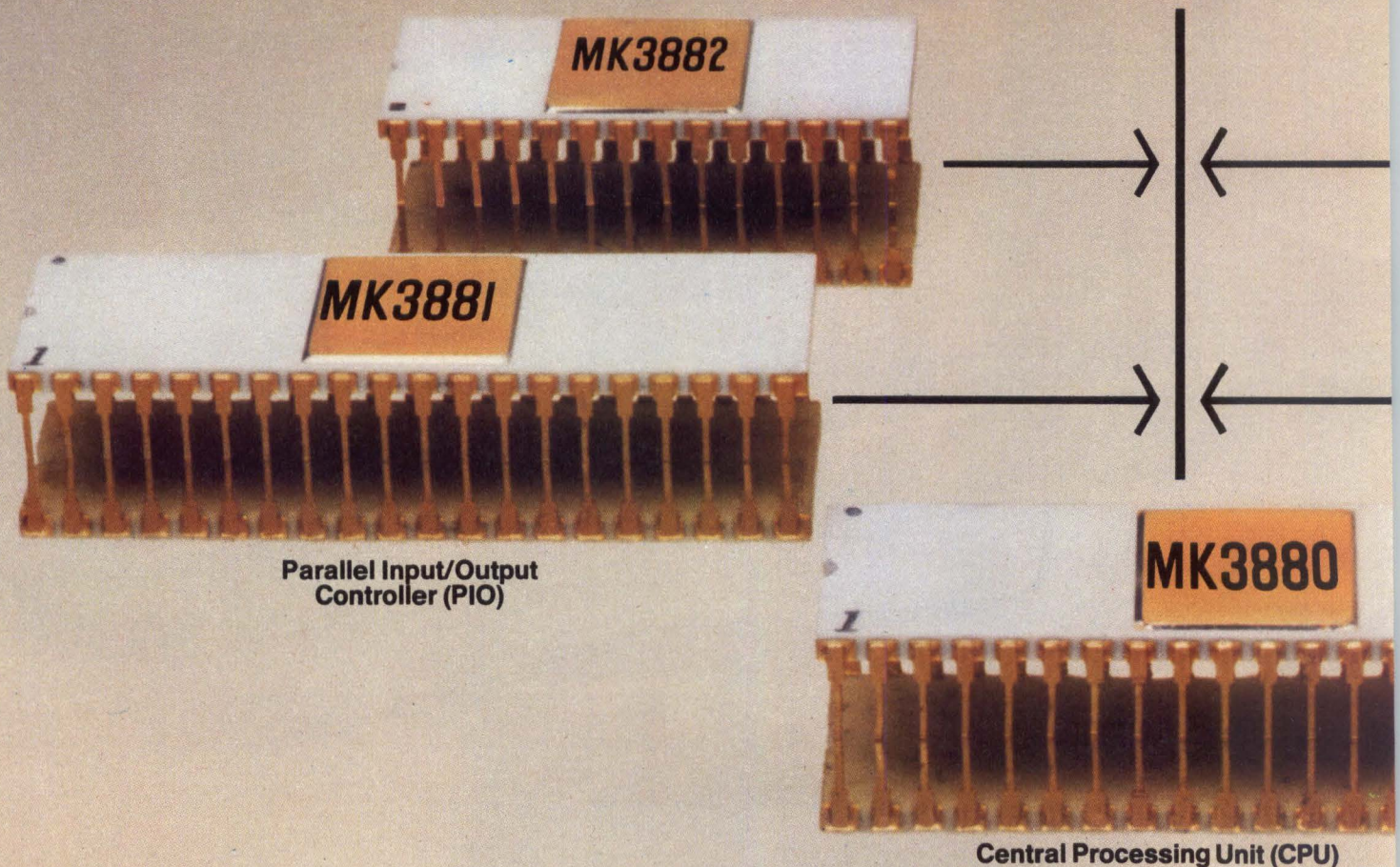
Reduced memory interfacing costs over the 8080A.

The Z80 CPU provides all refresh and timing signals to directly drive dynamic memories so that the Z80 LSI components can interface to most standard 4K dynamic memories with minimum external logic.

Reduced I/O costs over the 8080A.

To reduce I/O costs the Z80 LSI component set includes four general purpose programmable I/O circuits containing all of the logic required to implement fast I/O transfers with minimal CPU overhead.

Mosteks Full Memory Family of Dynamic And Static RAMs ROMs and PROMs.



Counter Timer Circuit (CTC)

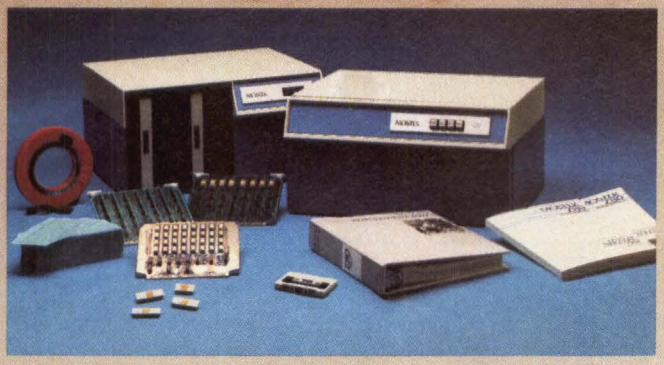
Parallel Input/Output Controller (PIO)

Central Processing Unit (CPU)

Reduced support circuitry costs over the 8080A.

All Z80 devices require a single +5 volt power supply and a single-phase TTL clock. All control signals are directly compatible with I/O and memory devices so that system control circuits are not required. External interrupt control and prioritization circuits are unnecessary since these are included in each Z80 I/O circuit. DMA circuits are usually not required due to an extremely fast interrupt response and powerful I/O block transfer capability within the CPU.

That's just part of the story. Mostek's Z80 is backed by complete documentation, hardware/software support, field application engineers and immediate availability through your local distributor. For additional information visit your local distributor or contact the Mostek sales office in your area.



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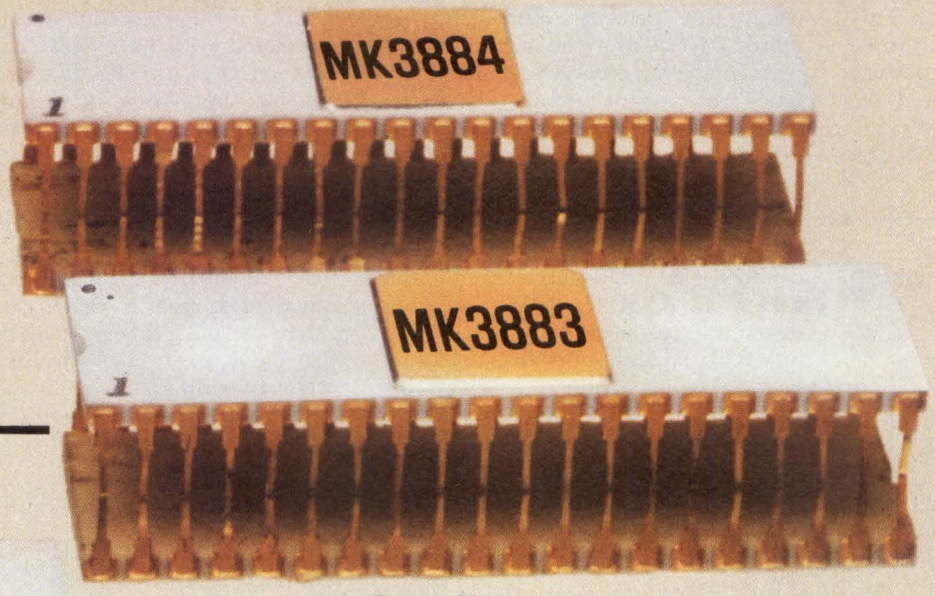
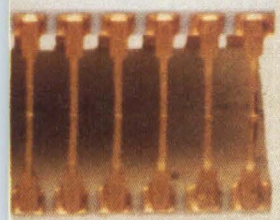
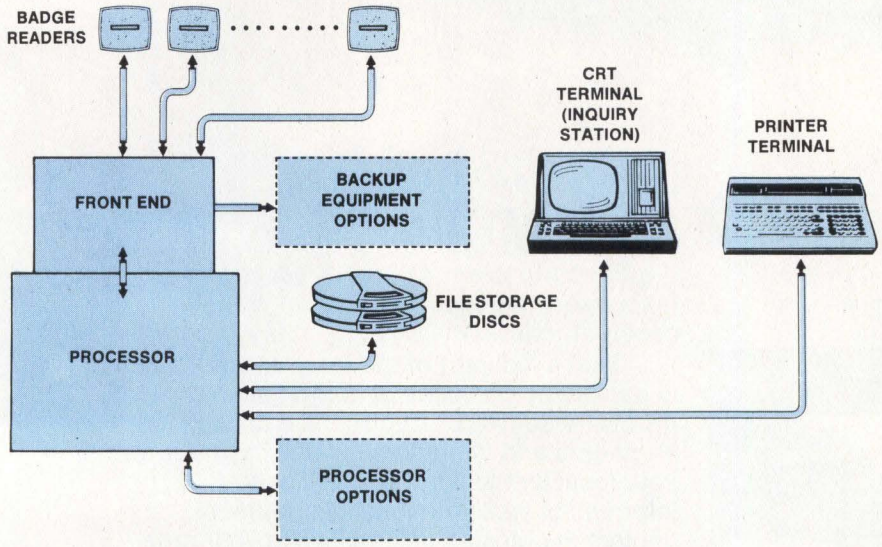
Serial Input/Output Controller (SIO)



Direct Memory Access Controller (DMA)





Cardkey System's Multi-Tyme time-keeping system provides a means of maintaining personnel records, computing accumulated working hours, and providing the resulting data directly to a payroll system. Additional equipment may be installed to provide smoke, fire, and flood detection or to monitor power failures or intrusions into restricted areas

employee entry and exit times; computes accumulated hours; provides video status display of accumulated hours or immediate identification of the available work force; and feeds a compatible output directly into any payroll system.

Basic equipment consists of processor, CRT terminals, printer terminal, disc storage, and badge or card readers. The system is triggered by a single, invisibly coded Securiti-Card® used as an identification badge by personnel. When the card is inserted into a badge or card reader, employee entry and exit times are transmitted to the central computer which is programmed with pertinent data regarding the card holder: name, social security number, emergency and personal data, and required payroll information.

A complete, accurate record of all time and attendance data is maintained; from this accumulated working hours are computed which can be retrieved for management reports, video status display of accumulated hours or identification of the work force, or for payroll input purposes.

The system is field-expandable with security and monitoring equipment. Cardkey access control and security monitoring equipment can be connected with no change in system parameters to provide door and parking lot supervision, alarm monitoring, and other security functions.

Circle 143 on Inquiry Card

System/32 Enhancements Offer Faster Printing, MICR Capability

Among the enhancements announced by International Business Machines Corp, General Systems Div, PO Box 2150, Atlanta, GA 30301, for its System/32 are eight models, created by combinations of printing capability and disc storage capacity; 285-line/min. printing capability; and magnetic ink character recognition capability. Industry applications programs (IAPs) for the /32 now include management accounting systems for general distributors, lumber dealers, and food distributors.

System/32 models A31 through A34 provide bidirectional printing capability at 120 char/s and range from 3.2M to 13.7M bytes in disc capacity. Models C41 through C44 combine the 285-line/min. printer with from 3.2M to 13.7M bytes of disc storage capacity.

MICR capability for banking and financial applications is achieved by attaching the 1255 Magnetic Character Reader. The unit reads and sorts magnetic ink character recognition encoded documents at speeds up to 500 documents/min. (model 1) and 750 documents/min. (models 2 and 3).

Operating on all System/32 models, accounting systems, each consisting of four modular IAPs which can be used separately or in any combination, assist distributors in billing, inventory control, accounts receivable, and sales analysis. Lumber dealer programs highlight functions unique to those who stock inventory in linear feet, board feet, and other measurements peculiar to their business. The food distributor package addresses functions familiar to that industry, ie, catch weight pricing, item substitution, and case label printing. The other program package is generally applicable to most other distributors.

Circle 144 on Inquiry Card

Holographic-Based System Stores 200M Bits On Low Cost 4 x 6" Fiche

Combining laser technology, holograms, and data storage, the system stores up to 200M bits of data on a 4 x 6" fiche—a low cost, almost indestructible media—at an approximately 100:1 reduction in both cost and storage area over magnetic tape; and with superior retrieval speeds

Compare the new Sanders Graphic 7 with other interactive terminals.

You'll draw a graphic conclusion.

Sanders' new Graphic 7 is an intelligent terminal with all necessary hardware and software as standard —not cost-you-extra—features.

But the Graphic 7 doesn't just save you money when you buy it. It also saves you money after you buy it.

Simply wheel your Graphic 7 through the door and plug it in. No installation problems.

Your programmer won't have to spend much time with your Graphic 7. It comes pre-programmed.

And your operators will be able to handle your Graphic 7 after a 10-minute briefing, because it works with a one-button initialize.

Application programs? Our Fortran-based graphic support package can reside in any host that supports Fortran.

And with the intelligence at the terminal, there's minimum impact on the host. You can do more work faster.

Sanders experience? Our graphic terminal systems are used in computerized production projects. Tire-tread design. Avionics defense systems. Flight training. Land-use management. Air traffic control. And dozens of other areas.

Compatible, fully equipped, low priced. What other graphic conclusion can you draw than the new Sanders Graphic 7? Send for specs and specific applications. Sanders Associates, Graphic Systems Marketing, South Nashua, NH 03060. 603-885-5280.

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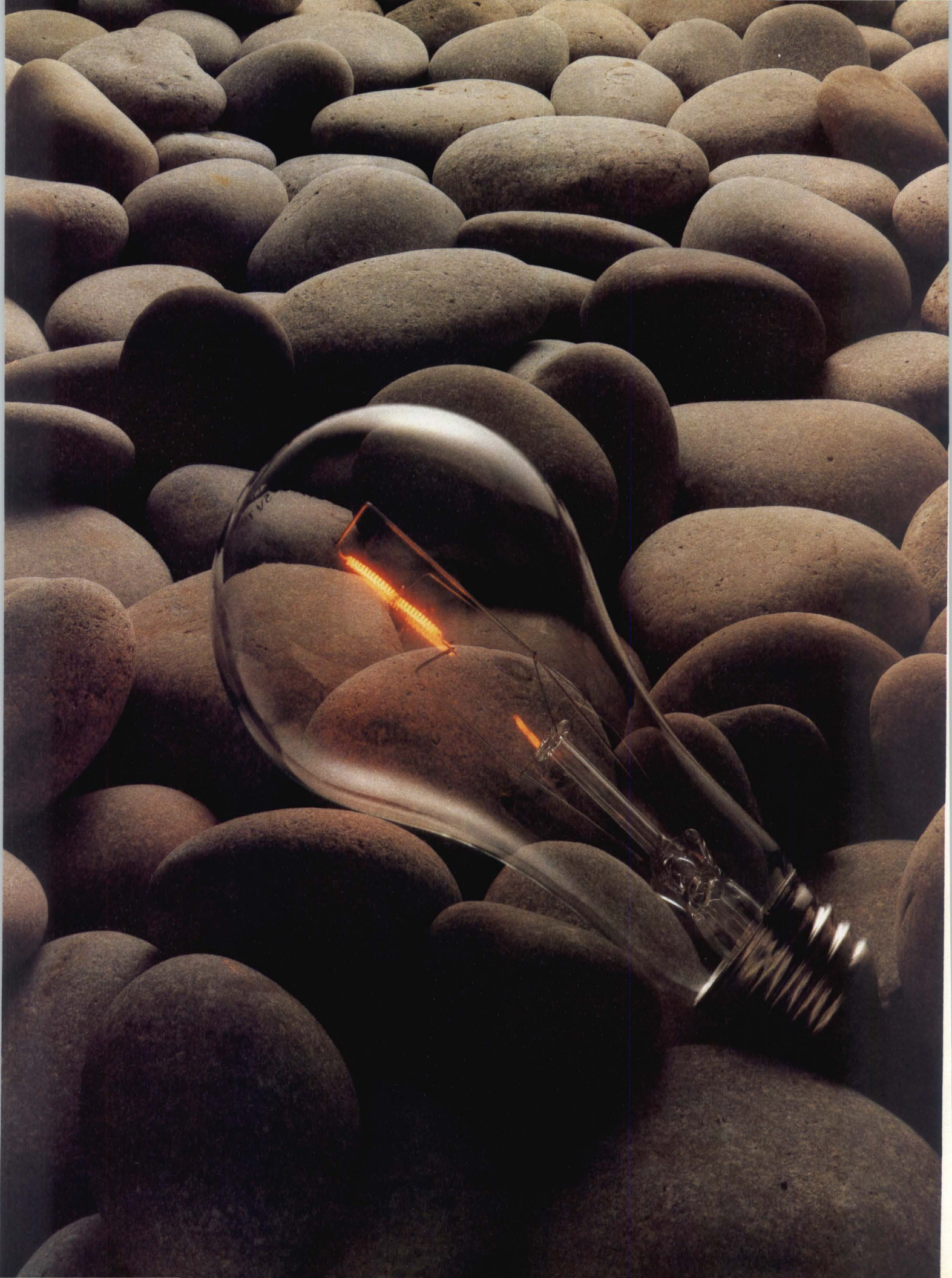
CIRCLE 22 ON INQUIRY CARD



Our bright idea.

More computer power for your dollar.

The SEL 32 family of high performance 32-bit computing systems offers a balance between big computer performance and minicomputer prices. Microprogrammable input/output processors, compatible central processing units, high-speed memory systems, and efficient data processing peripherals make up the hardware elements. On the software side, operating systems, language processors, libraries, application packages, and interactive terminal support balance the scales. Together, SEL 32 hardware and software provide a cost-effective solution to your current requirements, with expansion capability to meet your growth needs.

The SEL 32/35 is the strongest price-performer of any 32-bit single or multiple-CPU system available today. These computers can be configured from 64K bytes to 512K bytes of 900 nsec memory. Resembling its more powerful brothers, the SEL 32/35 is a complete package, including central processor with floating-point arithmetic, memory, chassis, power supplies, and cabinet.

The SEL 32/55, offered in a variety of both single and multiple CPU configurations, can be configured from 32K bytes to 1 million bytes of 600 nsec memory.

The SEL 32/50 is a single chassis computer providing the same CPU, I/O, and memory capability as the 32/55, but for dedicated applications.

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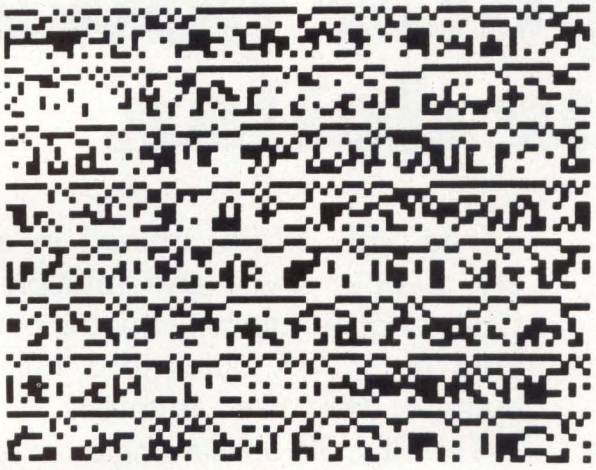
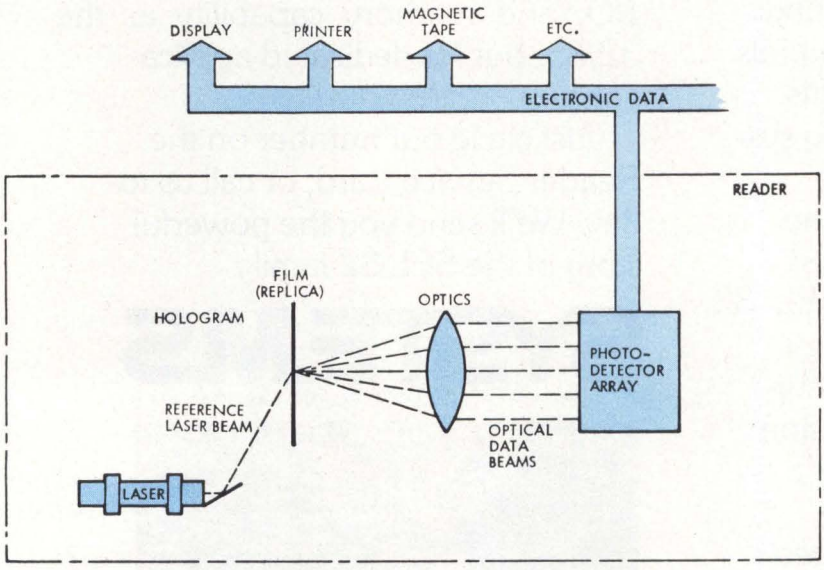


(a)



(b)

The reader in Holofile's data terminal can access an individual hologram (a) containing thousands of data bits within a few seconds. When the laser beam strikes a hologram its binary pattern is converted to electronic data by the optical sensing array (b). Converted data may be displayed, printed, or restored on magnetic media

to microfilm systems. Produced by Holofile Industries Ltd, 21243 Ventura Blvd, Suite 243, Woodland Hills, CA 91364, the system interface to minicomputers, large scale computers, and peripheral devices is accomplished with standard digital devices.

Heart of the system is the holofile memory. The fiche contains thousands of tiny individual holograms, each of which consists of thousands of data bits—the content of an optical data page. Binary numbers are represented optically by a white square for a 1, and a black square for a 0. During the direct conversion of electronic binary data to optical binary data, they are also formatted into an optical data page using a page composer. This data page can correspond to printed page, parts list, or alphabetical list of names. After conversion and formatting the optical page is recorded as a single hologram on ordinary photographic film. Once holograms are recorded, the "master" film is processed using conventional methods, and replicated. "Replicas" become the actual memory in the system.

The holofile system data terminal consists of a reader housing the memory, a laser, an optical sensing array, associated electronics, and a keypad/display for addressing memory. To retrieve data, the film replica is inserted in the reader and the laser beam is addressed to intercept the appropriate hologram via the terminal keyboard, or from a peripheral device. Typical access time is a few seconds.

When the laser beam strikes a particular hologram, the hologram emits a binary light pattern of its entire contents. This pattern is converted to electronic data by the optical sensing array and is clocked out at rates to 5M bits/s. Once converted, data can be displayed, printed, or recorded on a magnetic storage device. One reader can support a number of keypad/displays directly interfaced or over conventional telephone lines.

One example of how holography may impact mass memories concerns the storage of archival data. If the data now stored on the hundreds of thousands of reels of magnetic tape, which are housed in the offices of government agencies (eg, the Bureau of Census, the National Archives), were stored on Holofile fiches, storage space requirements could be reduced to a fraction of the current volume, at approximately 1/100th the cost.

Circle 145 on Inquiry Card

Static Switching System Expanded to Solve Control Problems

The Simatic C1 static switching system and supplementary C2 system functional units have been expanded by the addition of functional modules, remanance units, and power supplies. Siemens AG, Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany has also introduced additional wiring facilities for C1 potted blocks, which with the other extensions make the system capable of solving varied control problems from both the technical and economic points of view.

A static switching system for frequencies up to 80 Hz, the C1 is a high noise immunity surge-proof electronic control system for use in the

Pick a signal and any mini...Using RTP

Let's say you have some relay contacts to monitor, 115 VAC control signals to sense, 4 to 20 mA analog process signals to measure, and you need to provide relay output contact closures and 4 to 20 mA set-point signals.

This application can be handled by a few standard RTP analog and digital input/output cards, a Universal Controller, and an RTP Bus Converter.

First, you select the cards. Our family of process I/O interface cards provides the versatility to match almost all industrial sensors and actuators.

The Universal Controller provides the logic, power and space for up to 16 of these cards, in any combination.

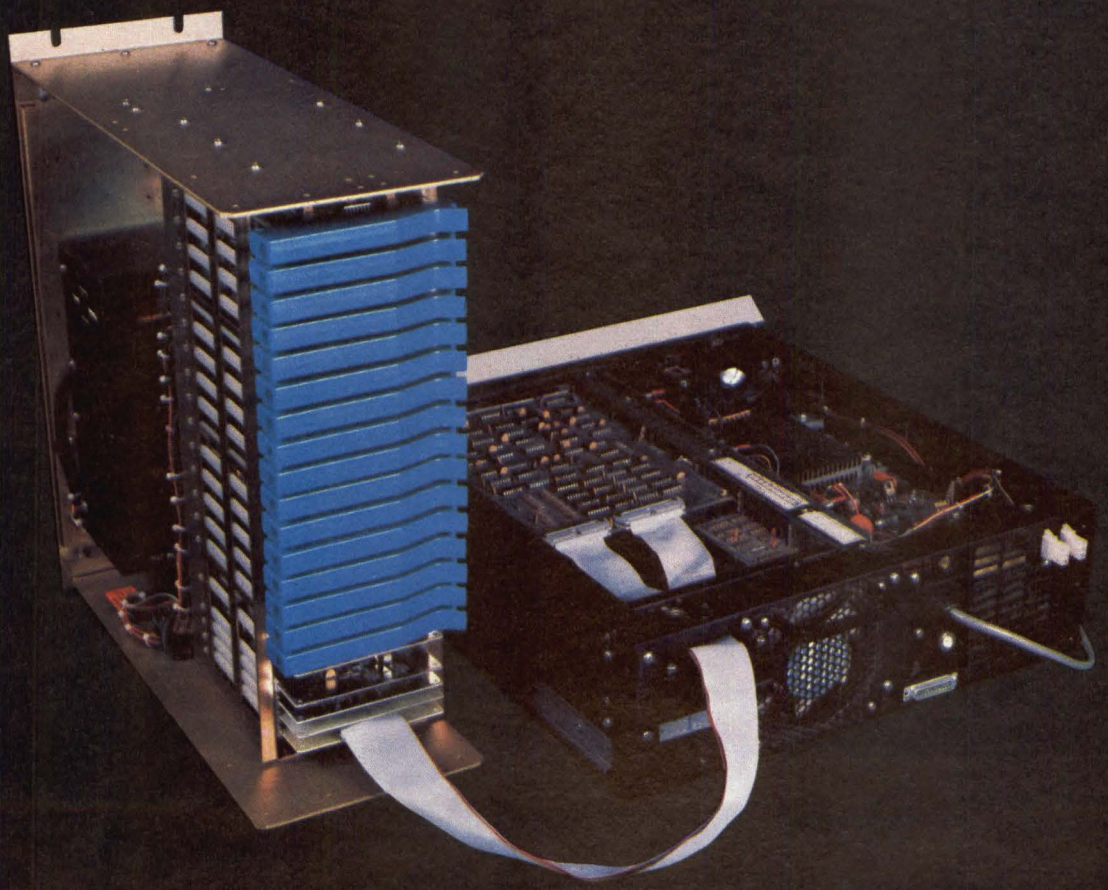
The RTP Bus Converter interfaces the Universal Controller to your mini by converting your mini's parallel I/O bus to the standard RTP parallel bus. Appearing transparent to your computer, it allows the Universal Controller to be directly programmed, as if it were one of the computer's peripherals. Best of all, RTP Bus Converters are available for all popular minicomputers.

Those are the essentials! But it's kind of tough to design a measurement and control system from an ad.

So, we'd like to send you "Using RTP." This booklet will provide you with a concise RTP subsystem design overview. Just circle our number on the Reader Service Card.

Computer Products, inc.

Versatile I/O



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Japanese Distributor: Tamagawa Seiki Co., Ltd. 3-19-9 Shin-Kamata, Ohta-Ku, Tokyo, Japan 144. Phone: 03-731-2131.

CIRCLE 24 ON INQUIRY CARD

Intel® 3000 the overtime out

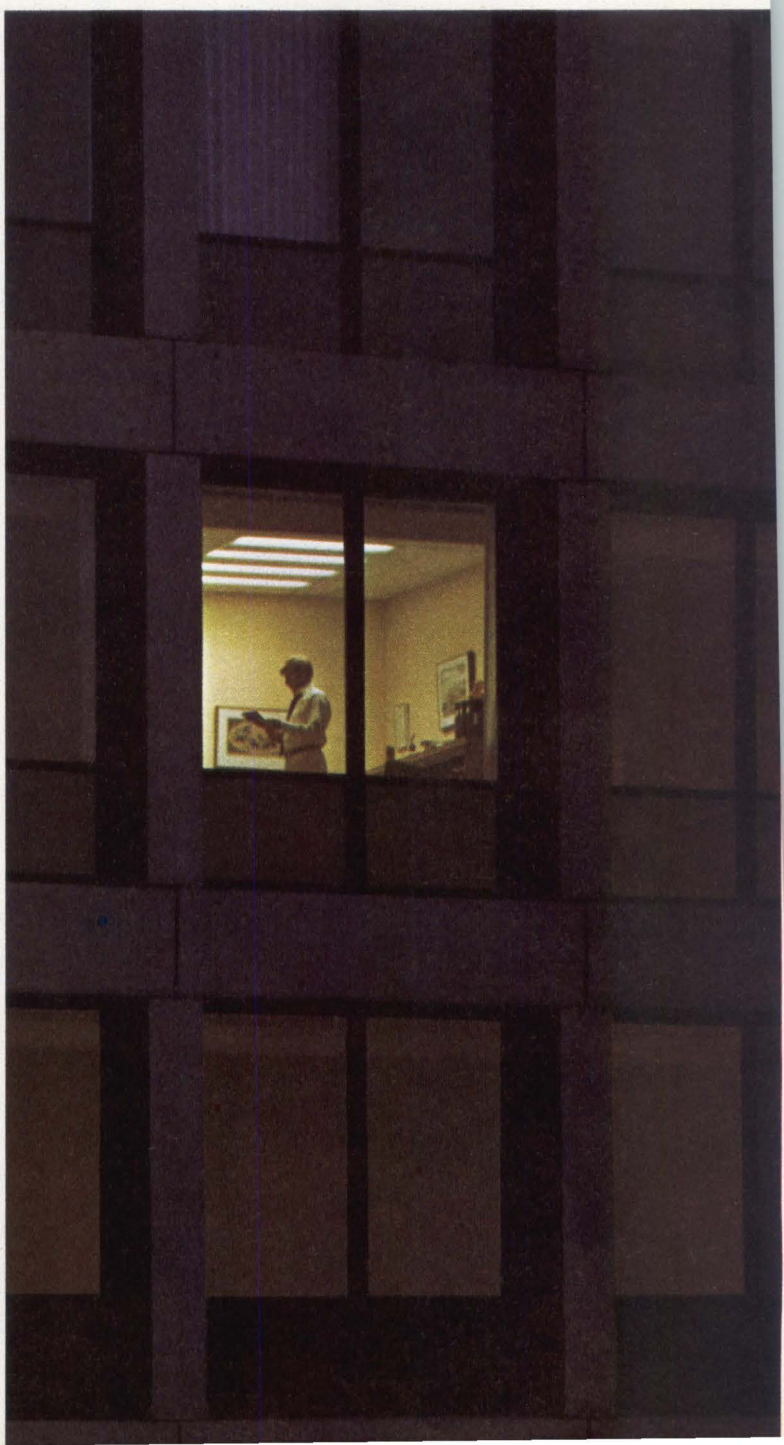
There are two ways to get your bit slice design to market—on your own or with Intel Series 3000 support. The Intel way is faster. Much faster.

Intel Series 3000 components and total support help you save time right from the beginning—from concept through microprogram development to system integration and debug—right through to production.

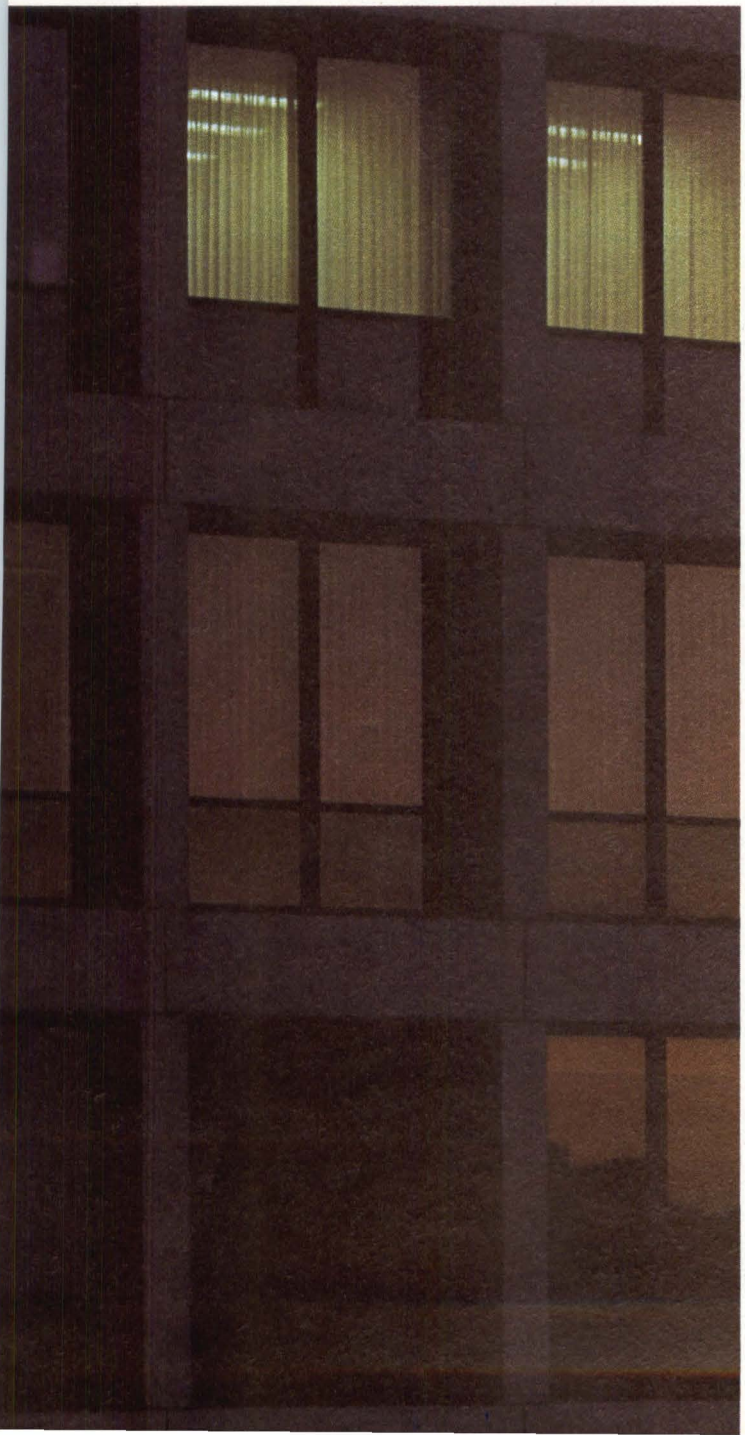
Our Intel Series 3000 bipolar LSI microcomputer components are designed as a compatible family—eliminating the need for special drivers, bus multiplexers, address latches and other components. You can tailor the 3000 to fit your commercial or military application and do it with a minimum number of ancillary components. Your designs will cost less. Much less.

Cut your microprogram development, debug and documentation time with our Series 3000 CROMIS microassembler system. CROMIS is available in ANSI (standard) FORTRAN IV source form or on any of several time sharing networks.

Reduce your system integration and debug time with our Intellec Microcomputer Development System with ICE-30™ in-circuit emulation and ROM simulator (ROM-SIM). This Intellec ICE-30/ROM-SIM capability enables you to quickly isolate program faults and selectively debug portions of microcode. Store your microprogram in ROM-SIM's read/write memory. Then use ICE-30 to set program breakpoints and single step



support takes of bit slice design.



the microprogram. ROM-SIM lets you examine or modify the program without blowing PROMs. Once the microprogram is debugged, you can program PROMs—transferring the microprogram stored in ROM-SIM to your PROM using the Intel Universal PROM Programmer.

Intel support doesn't end with CROMIS or the Intellec Microcomputer Development System. There's more. Field applications engineers are available to answer questions and give suggestions. Series 3000 application notes will give you helpful ideas on simplifying bit slice designs. And we offer customer workshops where you can get "hands on experience."

Whatever your bit slice application, you'll find the total support you get with the Intel Series 3000 cuts months off development time. Intel support makes the big difference. We take the overtime out of bit slice design.

For additional information use the reader service card. For quick response use the coupon below.

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CIRCLE 25 ON INQUIRY CARD

vicinity of power equipment. It is directly compatible with the C2 system which incorporates counters, registers, adders, code converters, and DACs operating at frequencies to 10 kHz. Since operating frequencies are governed only by the delay inherent in the flip-flops, all modules without memory can be combined with modules of the other system.

Among the modules added to the C1 system are an AND gate for inhibiting and enabling signals, an RS flip-flop with negated reset input, and an 8-bit shift register. Remanance units allow signals to be stored for prolonged periods of time in the event of power outages. A Hall generator adapter makes it possible to convert Hall-effect or equivalent voltages (from ±5 V) to system signals, and galvanic isolation of circuits by means of optical couplers and transformers is facilitated by use of 24-, 110-, and 220-Vdc signal adapters.

A 60-mA short-circuit-proof power supply is available for peripheral contact inputs or small control system equipment. Drivers rated between 1 and 15 A at 220 to 500 V permit direct switching of devices in primary circuits even at high switching frequencies.

Modules added to the C2 system include a comparator for information represented in BCD or pure binary code, an adder for the addition or subtraction of two numbers with arbitrary sign, and a DAC for converting from BCD code to analog voltages. Other enhancements are 4-decade thumbwheel setters for counting circuits, pulse-scan and sign-reversal modules which permit users to form the difference between positively and negatively weighted pulses and to drive up-down counters in 2-quadrant operation; and a pulse evaluation module which permits further processing of signals from incremental sensors with direct evaluation and pulse multiplication.

Circle 146 on Inquiry Card

Business Computer System Speeds Throughput With Microprogrammed CPU

In a move intended to provide users with more performance/dollar, Basic/Four Corp, PO Box C19550, Irvine, CA 92703, has introduced the System 700, a transaction processing system that features support for up to 16 terminals, disc storage capacity for up to 400M bytes, and a company-manufactured microprogrammed CPU. Designed to provide large scale data management in a small business computer, the system is claimed to store 10 times more information, provide faster throughput, and incorporate a more sophisticated storage subsystem than the company's other models.

The unit is an interactive, multitasking system that accommodates 16 visual display terminals (VDTs), providing users with up-to-date status information while handling routine jobs that need immediate attention. Minimum system configuration consists of four VDTs, CPU, 300-line/min. printer, two 50M-byte disc drives, and 64K memory (40K user, 24K operating system). The intelligent disc storage subsystem is organized around a programmable LSI microprocessor which handles time-consuming housekeeping chores normally performed by the CPU.

The CPU addresses up to 128K of memory and is equipped with an 8-page firmware set, which gives it a large machine language instruction capability well suited for executing BUSINESS BASIC II. The MOS technology memory has a 600-ns full cycle time, and can be selected in 8K modules. Each module is equipped with automatic parity detection to ensure that any error that may occur is discovered before it can result in an invalid result.

Software spooling provides efficient line printer operation and binary synchronous communications; the system handles up to 16 channels of full duplex asynchronous communications at up to 1800 baud over standard telephone lines.

The operating system permits numeric packing of files before they are written to disc, achieving a 40% reduction in data space requirements. Report generator/inquiry capability is provided through EASY (Exception Analysis System) which supplies fast exception reporting. The Tri-State Language Processor retains online programming advantages of an interpreter and provides compiler efficiency.

Circle 147 on Inquiry Card

Communications Interface Connects Printer to Parallel or Serial Source

A communications interface designed to connect the Digital Equipment Corp LA180 DECprinter to a parallel data source, such as CRT, or serial terminal source via EIA signal levels or 20-mA current loop, the LAZZZ MCI contains a first-in/first-out buffer which smooths data flow to the printer without the need for additional fill characters. Parallel versions accept data into the buffer at up to 9600 baud while serial versions are switch-selectable for speeds up to 1800 baud, parity, and number of stop bits.

The interface, designed by Miscoe Manufacturing Ltd, 6358 Viscount Rd, Mississauga, Ontario, Canada L4V 1H3, uses the 64- to 512-character first-in/first-out (FIFO) buffer to smooth data flow to the printer when the source is transmitting data at a fixed rate; when the blocked data option is implemented, the buffer stores an entire message which can be sent to the printer by the data source after being verified error-free.

Buffer loading logic ignores NULL characters, allowing them to be used as fill characters without using up buffer capacity. Buffer select/deselect logic may be controlled locally or remotely; when the buffer is deselected, incoming data are ignored, allowing the data source to produce hardcopy in conjunction with a CRT terminal.

When serial receiver logic is added to the parallel buffer, received data may be at EIA RS-232-C signal levels or via a 20-mA current loop. Switches on the interface module permit selection of 1200-, 600-, 300-, 150-, or 110-baud rates, with 5, 6, 7, or 8 data bits; odd, even, or no parity; and one or two stop bits. The serial receiver detects parity error, overrun, and framing error conditions. Detection of an error causes the code for a "?" character to be loaded into the buffer in place of the erroneous character.

When the blocked data mode option is added to the serial interface data messages are held in the interface buffer until verified error-free. If an error is detected in the received message, the buffer is cleared and the entire message is retransmitted. When certified error-free messages are sent to the printer. □

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INTRODUCING THE ONLY BOARD TESTERS THAT SHOW WHO'S AT FAULT. SHORTS, BAD COMPONENTS, EVERYTHING.

Now, thanks to our new CAPS VIII software, our GR board testers can take you beyond identifying the faulty node to pinpointing random shorted tracks, opens, and faulty components. And they get there at least twice as fast as other testers that only get you to the node. So they save you both troubleshooting time and repair time and require fewer rework support people.

But that's not all. CAPS VIII software also gives you faster setup, to reduce testing costs even more. This is accomplished through our new Automated Program Generation (APG) Software which includes an incremental simulator, event tracking capability, equation generation and test-generation language. It will give you a test program that detects a greater percentage of faults in less time than any other setup method on the market.

To make CAPS VIII even more attractive, we're also offering a new Smart Clip, a new pulse-catching logic probe, an IEC buss interface, and diagnosis logging capability.

Of course, to get CAPS VIII's big improvements in fault resolution, setup and troubleshooting speed, and cost, you first need a GR digital or hybrid circuit board tester. But that's no problem either.

New Smart Clip reduces diagnostic time.

The number to call is 617-369-8770 ext. 273. Gen Rad, Inc. Test Systems Division, 300 Baker Avenue, Concord, Massachusetts 01742.

THE DIFFERENCE IN SOFTWARE IS THE DIFFERENCE IN TESTERS.

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The only microcomputer with the power of a PDP-11. The PDP-11/03.

If you've been looking for a microcomputer with minicomputer power at a micro price, join the hundreds of OEMs who've already found it with the DIGITAL microcomputer. The PDP-11/03.

The 11/03 gives you everything you could ask for in a small computer. High performance. High reliability. And a low price—just $1,357 in quantities of 50. And that micro price buys you mini features that quickly translate into benefits OEMs appreciate. Features like full PDP-11 instructions with eight general purpose registers for fast program development. RAM (MOS or Core) and PROM memories that let you match the memory with the application. Hardware vectored interrupts with stack processing for real computer power. And multiple-sourced components for sure delivery.

Buying our 11/03 also buys you the chance to start small without staying small. Because you can add up to 32K words of memory, fast floating point instructions, and more. Whenever you and your customers are ready.

Besides growing bigger in size, the 11/03 lets you grow bigger in scope. It's software compatible with every other PDP-11 we offer. From our LSI-11 all the way up to our medium scale PDP-11/70. That means you can take full advantage of Digital PDP-11 software and services.

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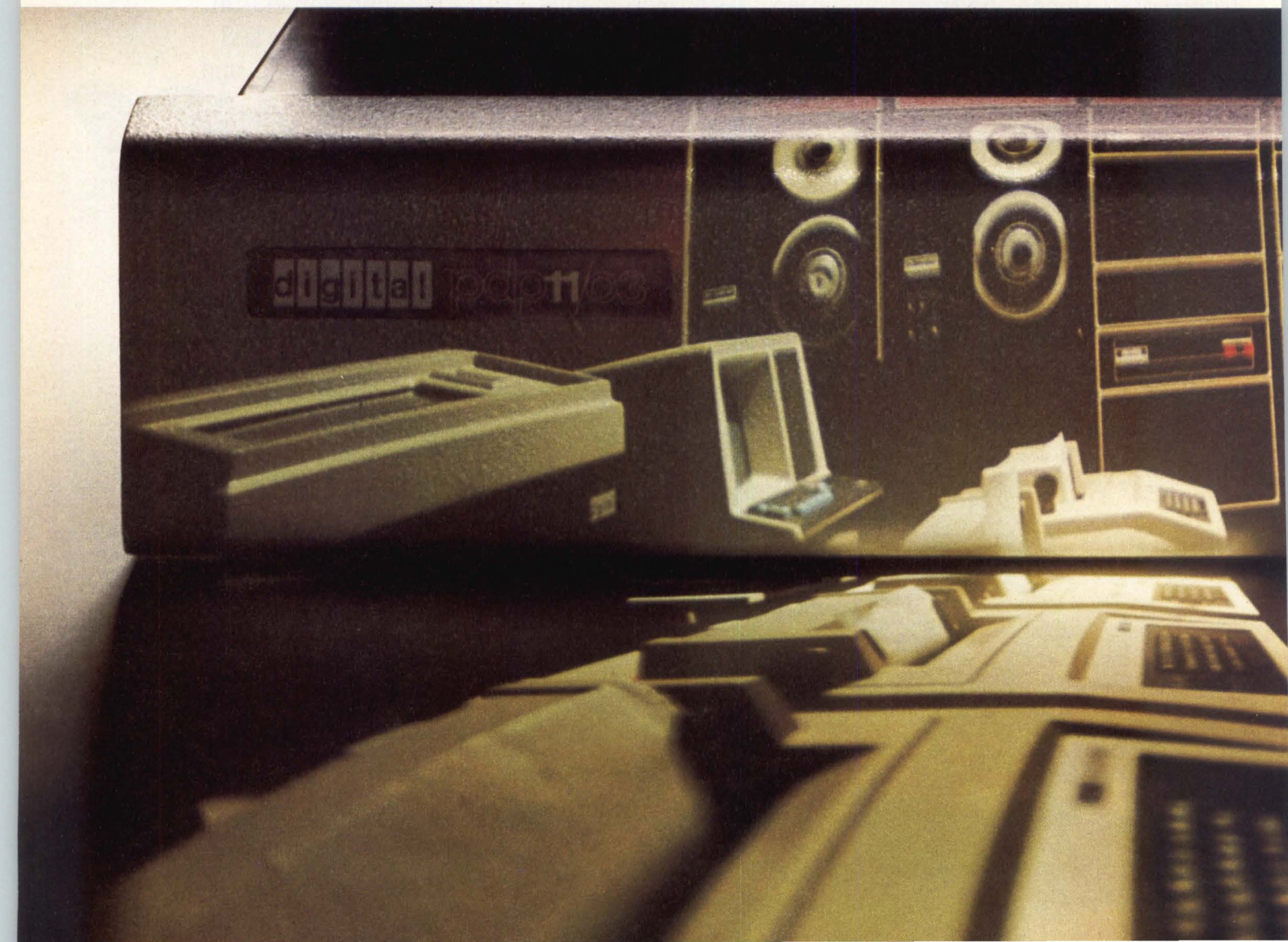

ers and new markets around town and around the world. And it can all start with the PDP-11/03.

So if you're looking for a proven microcomputer with proven power and performance, get the micro with all the power and performance of a PDP-11.

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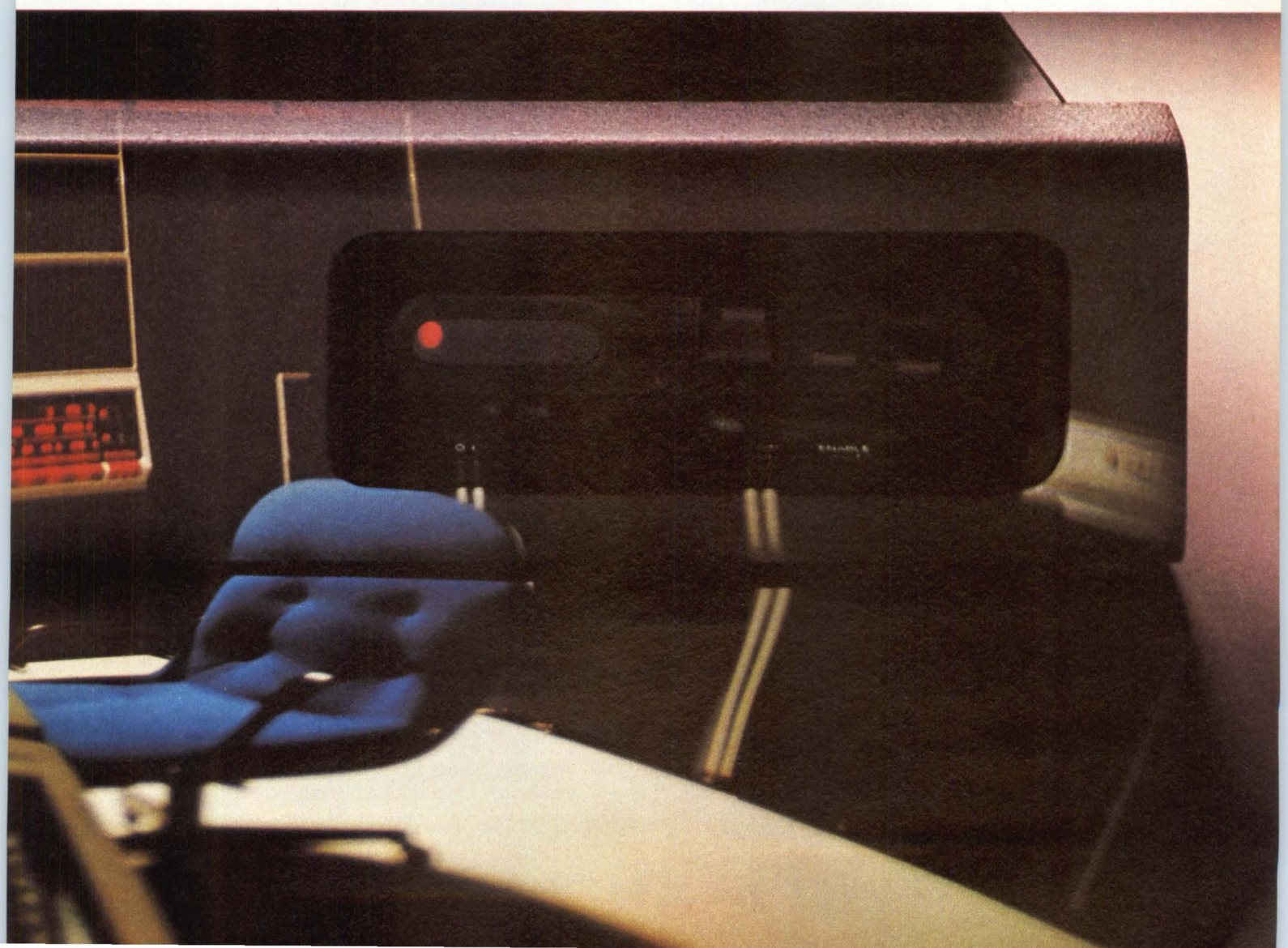

Microprocessor Solves Batch Mixing Problems for Supplier of Bread Ingredients

Mixing large batches of dry ingredients used in making bread can at best be a complicated procedure, especially when the batches weigh up to 5000 pounds. An error can cause an entire batch—worth as much as $1200—to be scrapped. When increased orders necessitate far greater production, the process becomes a major problem.

Roush Bakery Products Co in Cedar Rapids, Iowa is a supplier of dry processed grains to "natural food" bakeries in various parts of the country. There, wet ingredients are added before baking. Ordinarily, up to six processed grains were batched by volume by dumping a number of bags into an open hopper. As the popularity of natural foods increased, this inexact volume method became impractical, particularly when additional output increased the overall number of potential scrapped batches.

To counteract these problems, Roush contracted with Frank Haile and Associates, a designer and builder of food mixing facilities, for a system that would eliminate human error in mixing the dry ingredients. Development of the system was assigned to Micromega Corp of Dallas, Texas. Stipulations included increased repetitive accuracy and delivery of a system within a very short time.

Control System

In the system developed, measurement is by weight rather than volume. Processed grains are stored in silos that are up to 12 ft in diameter and 60 ft high. Ingredients are moved through 5-in. ducts to a weighing hopper by air velocity developed with a 50-hp blower (Fig. 1). Measurement and control are maintained by a 16-bit PACE microprocessor manufactured by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. The human element is minimized but not eliminated. Persons still have to determine which of the six grains are to be included in a particular batch, start the procedure, and stop it if something goes wrong.

Because of the need to develop an operable online system rapidly, Micromega used known components, all basically from the same manufacturer: CPU application card, 1K by 16-bit RAM card, and 1K by 16-bit p/ROM card with empty sockets. Since only 885 words of permanent storage were required, the p/ROM card was loaded with eight 256 by 8-bit MM5203Q MOS p/ROMS. Inclusion of these compatible 4.5-in. sq cards, all from National Semiconductor, allowed control development without time-consuming card design, layout, fabrication, checkout, and component qualification.

Control input is both 16- and 8-bit data (Fig. 2) via the processor's common I/O bus architecture. Inputs from control panel thumbwheel switches, scale digitizer, panel switches, and valve position are 16 bits while "weight-in column," set by thumbwheel switches, is eight bits. Outputs to valve commands, display, and indicator LEDs are 16 bits.

When preparing a batch, an operator first sets thumbwheel switches for the proper weights required for each of six selected ingredients: bran, rolled wheat, soya grits, corn flour, rolled oats, and rye. Then he turns a selector switch to the Auto-Batch position and pushes the Start button (Fig. 3).

Initially, the processor determines the positions of valves controlled by the system—two blower valves (B1, B2); six diverter valves (D1 to D6), and a single fast acting weighing hopper fill valve (S1). An electrically operated apparatus consisting of a vibra-screw and a rotary gate valve is located at the bottom of each silo. The vibra-screw provides an assured flow of grain while the rotary gate valve modulates the air stream in the duct with the ingredient. Selection of a blower valve and a combination of the six diverter valves establishes the air stream. When the hopper fill valve, S1, is operated, the air-entrained ingredients are diverted to the weighing hopper. Otherwise, the air stream and any material deposited in it will return to the silo from which the material was taken.

Ingredient transfer from silo to hopper begins with processor actuation of the blower along with automatic positioning of appropriate blower and diverter valves. Since blockage in the ducts can be catastrophic, requiring dismantling of the pipework, air pressure is monitored continuously. An air pressure increase during startup or any time during the program causes immediate shutdown.

Progressively, the processor then verifies that the chosen valves have moved to the commanded positions and that the others have remained closed. The processor manipulates bit data, through a masking program, and compares valve positions against tables in p/ROM. Valve position reporting requires one 16-bit word.

(Continued on p 52)

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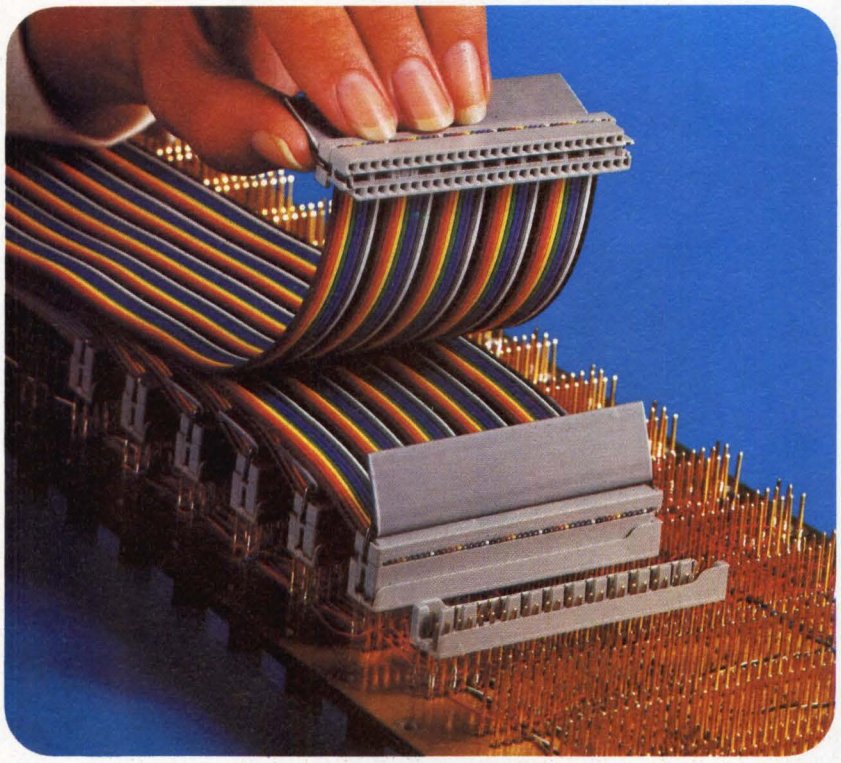

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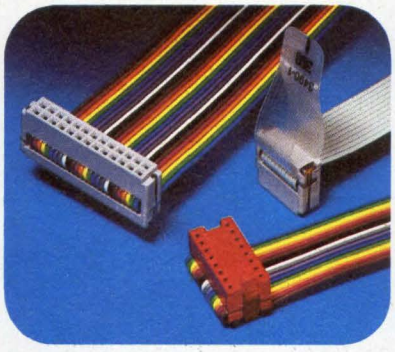

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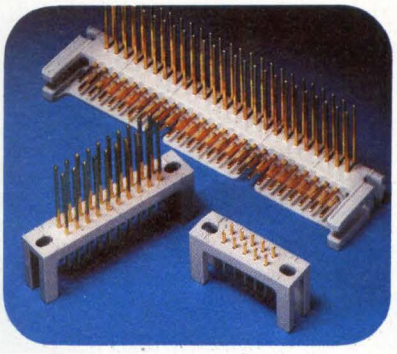

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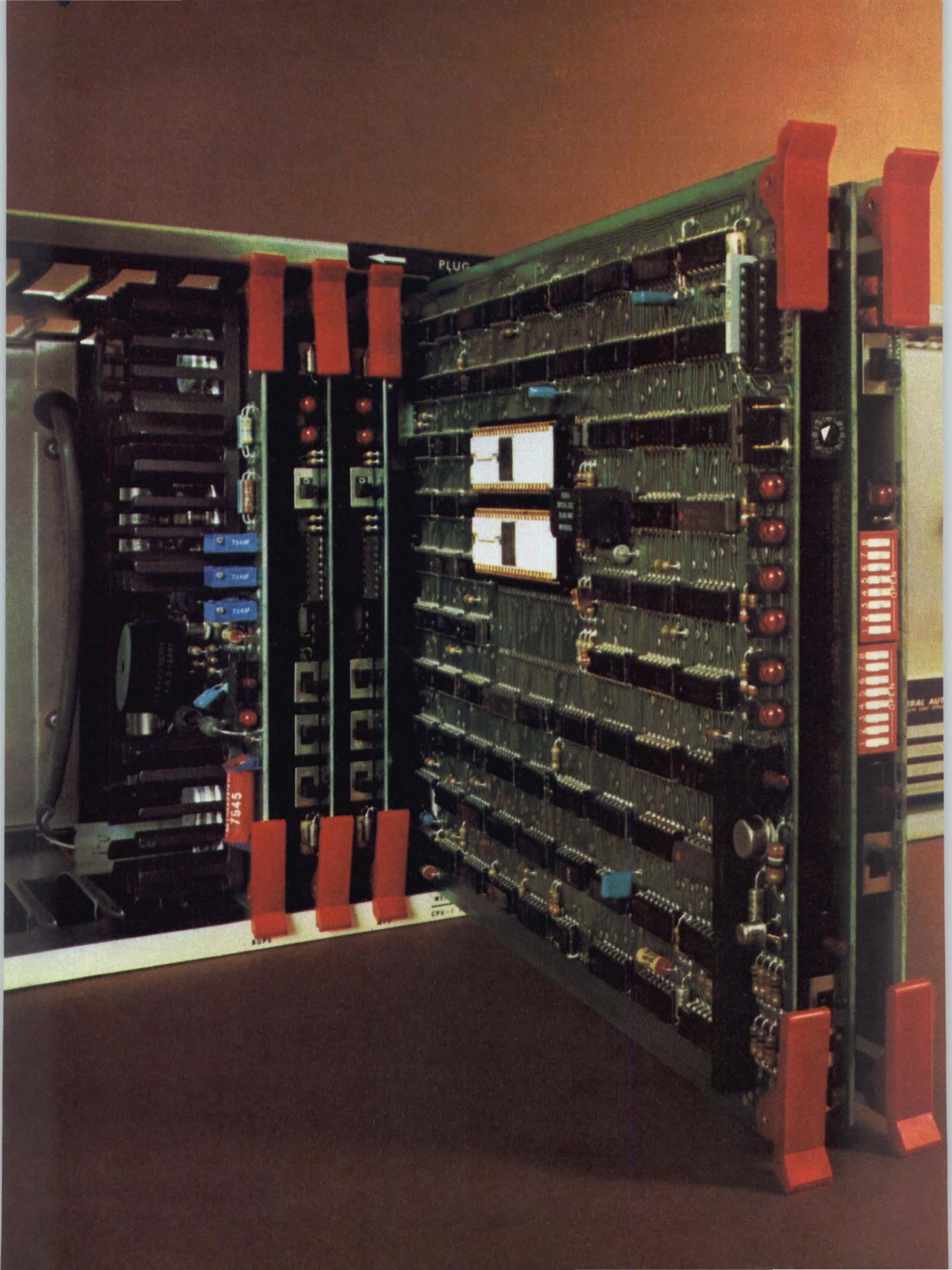
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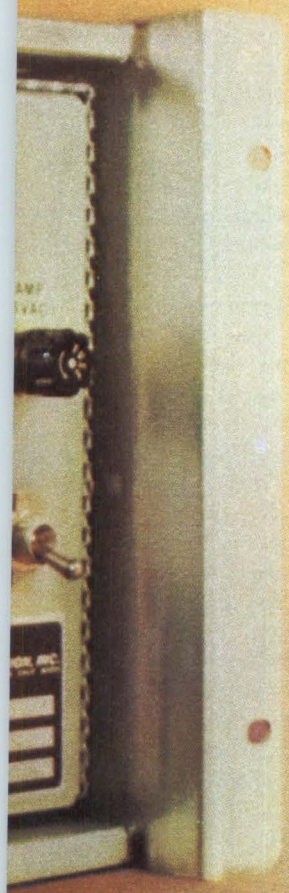

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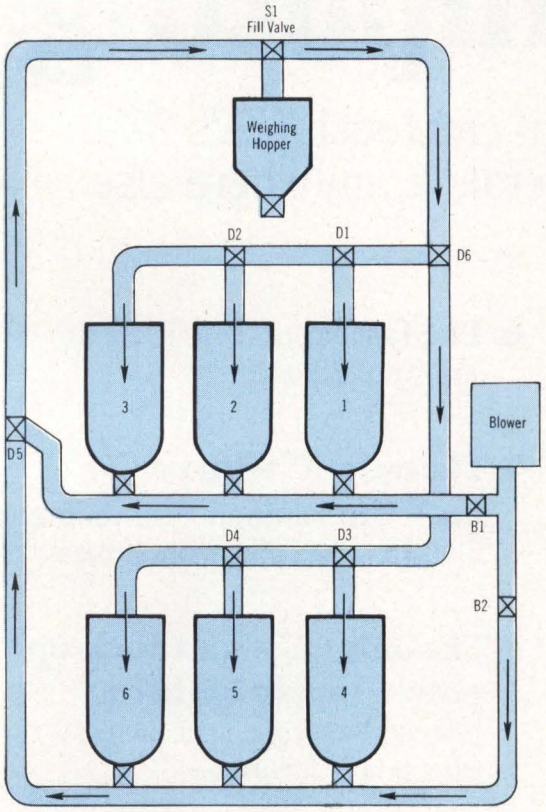

Fig. 1 Bread ingredient mixing plant consists of several silos, up to 60 ft high and 12 ft in diameter, linked with weighing hopper via 5-in. transmission ducts. Process flow (arrows) is controlled by selective actuation of blower valves (B1, B2) and diverter valves (D1 to D6). Vibra-screws and rotating gates in bottom of selected silo move materials into air flow. Fill valve (S1) diverts ingredients into hopper or back into closed-loop system for return to silo

Once valve positioning is approved, the processor concurrently operates the vibra-screw/rotary gate valve pair for the chosen silo and the hopper fill valve (S1), so that material deposited in the air stream goes directly to the weighing hopper. Ingredient weight, measured by hopper load cells, is continually compared to the thumbwheel switch values. The system closes S1 by anticipating the weight of the material in the column between the valve and hopper. A constant from 0 to 99 pounds, set by a "weight-in-column" thumbwheel switch, tailors the shut-off according to plant delivery rate, ingredient density, and physical dimensions of the delivery column.

Simultaneous with S1 release, the vibra-screw and rotating gate are deenergized. When S1 changes position, ingredients in the column continue to fall into the hopper. Final weight is registered and stored in RAM. The register is zeroed prior to entraining the next material.

Since the air duct system operates on a closed-loop principle, bypassed ingredients are returned to the appropriate silo. A 20-s program delay allows line purging before the next ingredient is entrained.

Remaining ingredients required are transferred, under microprocessor control, in a similar manner. Valves are positioned and checked with appropriate delays. The blower remains on, however, once the process has started; material flow is initiated and terminated with the vibra-screw and rotating gates. Individual ingredient weights and cumulative weight are stored in RAM.

When the batching program is completed, the system automatically sequences down. The bottom (dump) valve is then enabled for manual opening and the ingredients are mixed, bagged, and shipped to the bakers.

As the process continues under microprocessor control, LED indicators on the panel not only tell the operator which ingredient is loading but also supply warning and status indications. Pressure transducer and valve position indicators insure the system is operating properly. If something is wrong, LEDs provide error indication, such as Dump Valve Open, Hopper Not Empty, or Valve Position Error. The processor also provides control for transferring ingredients among silos or restocking mixing silos from other silos.

The weight of each ingredient in the hopper is given by a 4-digit, 7-segment LED readout as weight is accrued. A digital interface on the load cell strobes the scale every 400 ms to update the display. When batching is complete, the system steps through, giving the weight of each ingredient (to ± 1 lb) and then the total weight. For verification, the operator may depress a button to repeat the display sequence.

There are three shutdown modes in the system. In the normal mode, shutdown at the end of a batching operation consists of line purging and then blower shutdown. Pressing the Stop button interrupts the hopper filling by deenergizing the silo vibra-screw and rotary gate. Essentially, it interrupts the process in place so that the operator may examine the situation; pressing the Start button allows the process to continue normally. The third mode, which prevents addition of useful product to a bad batch, occurs when the operator presses the Abort button. Then, under program control, the processor deenergizes the blower and returns the procedure to the start of the program.

Background and Future Potential

This microprocessor control system was shipped eight weeks after initial procurement and installed by local electricians. No onsite debugging was required. The only startup problem was a poor cable termination on the scale digitizer. Once control hardware and software were debugged, the system was integrated with the interface circuits. It functioned correctly on the first standalone startup.

(Continued on p 57)

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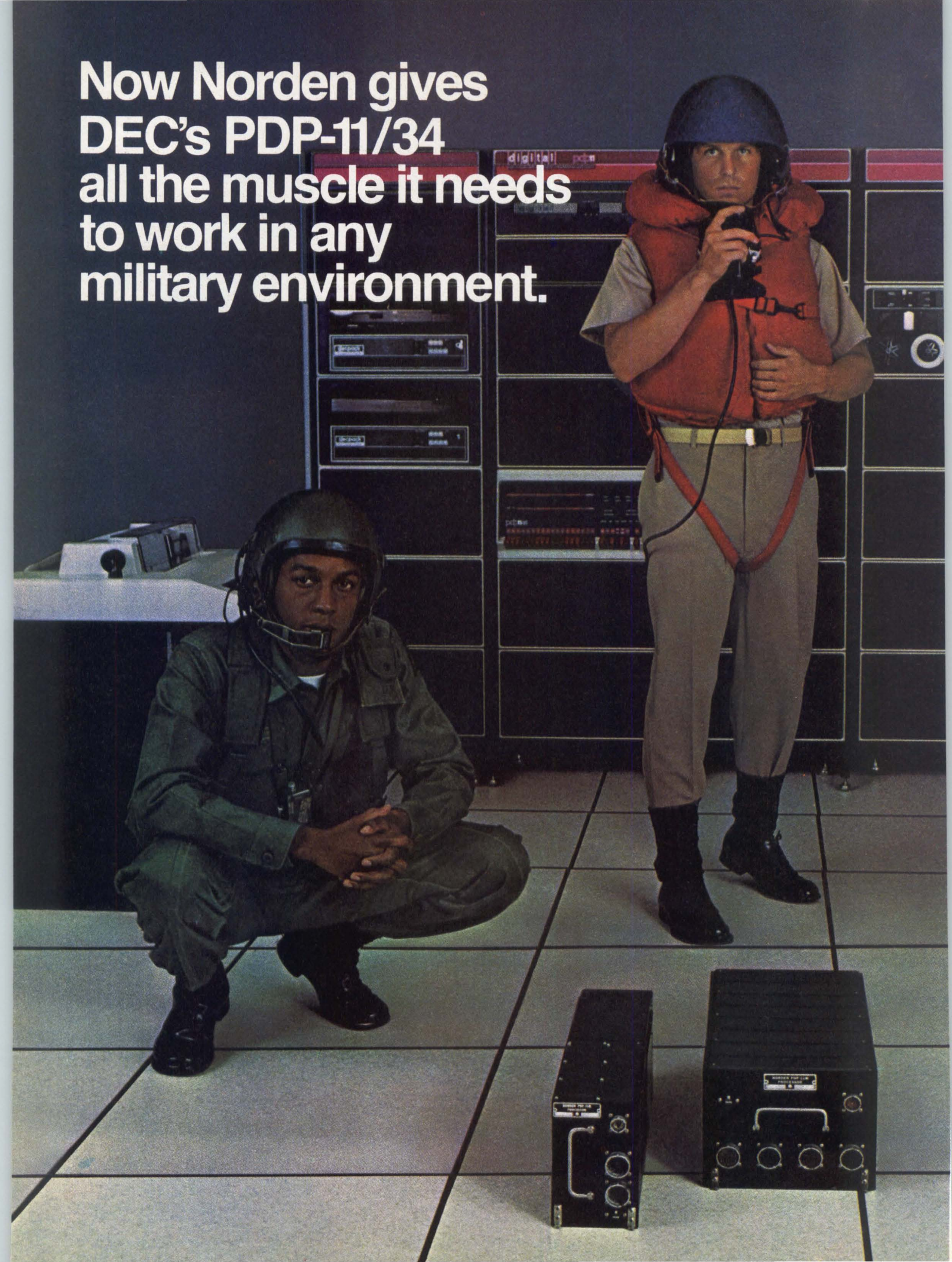
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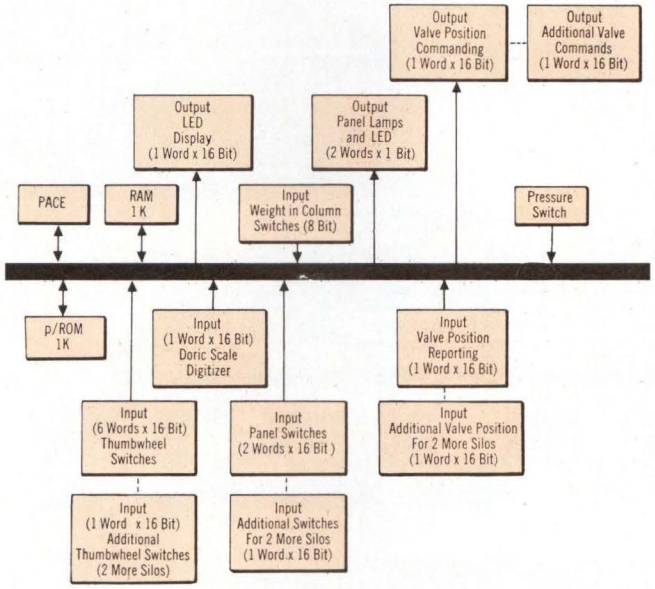


Fig. 2 Simplified diagram of PACE controller illustrates use of 16- and 8-bit input and 16-bit output words. Valve position commands and reporting are accomplished through two 16-bit words, masked selectively so that processor works at bit level

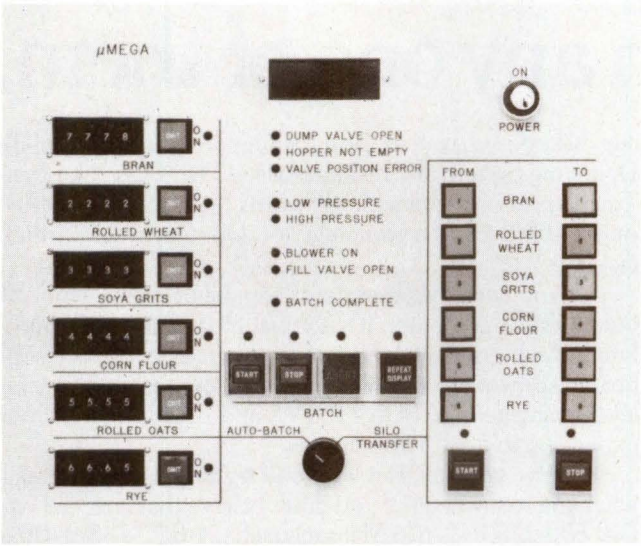


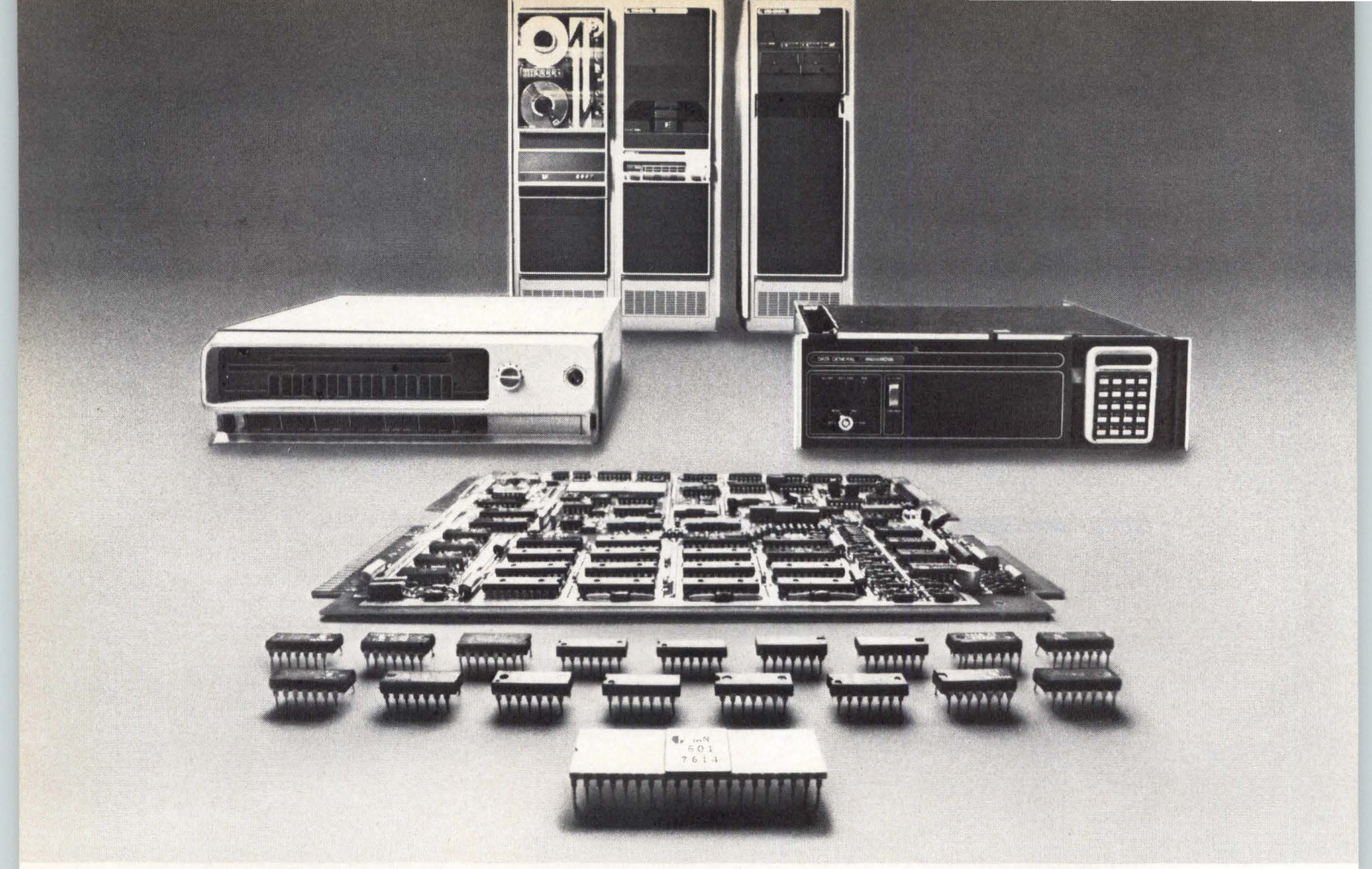
Fig. 3 Panel provides functional control and indication for batch mixing of six dry processed grains

To avoid the electrical noise indigenous to machine operations, all ac input signals, such as valve position reports, are optically isolated. Output is through solid-state relay drivers to customer-supplied interposer relays which operate silo valves and vibra-screws. As a preventative measure, an isolated line from the main service provides input power.

Application programs were written using the prototype 8K conversational editor, assembler, and debug programs while hardware interface circuits were designed. Using a card cage and cable, the processor and RAM application cards were sequentially introduced into the system. Only 80 words of RAM were required. Following further system checkout, p/ROMs were burned, placed in the memory card, and introduced into the system. The prototype emulated system input stimuli in response to processor output.

Under microprocessor control the possibility of human error has been virtually eliminated. The repetitive weighing accuracy has been so precise that the laboratory analysis, previously required for each batch, has been eliminated. Throughput has increased drastically. Design goals called for a 800,000-lb/month yield during the first month, accelerating to 1.2 million pounds during the thirty-sixth month. Actually, during the second month of operation 1.3 million pounds were shipped, while the third month's output was over 2 million pounds.

Because of the short development time, the microprocessor's full capability was not used, but was recognized as residual capacity. Future expansion may include automatic order entry, inventory control, management reporting, and control for additional silos. To further decrease the possibility of human error, the next step might involve elimination of the thumbwheel switches by using stored programming, supplied either locally or remotely from the order office. □



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Applications that have not yet been invaded by microprocessors, for reasons of extreme cost sensitivity or cramped space, are vulnerable to an LSI device that puts on one chip almost all of what usually takes a whole printed circuit board

Putting a Microcomputer On a Single Chip

Howard A. Raphael

Intel Corporation
Santa Clara, California

A better way for manufacturers to achieve their profitability and design goals is provided by the first series of 8-bit single-chip microcomputers with alternate program memory.* Single-chip construction minimizes product development, manufacturing, and service costs, while the family concept allows one basic system to be applied in different product designs to achieve the savings of hardware standardization.

One large-scale integrated (LSI) device can now perform operations that would ordinarily require a complex electromechanical assembly, 50 to 100 transistor-transistor logic (TTL) packages, or a multichip system. If expanded in capability with low cost LSI peripherals, the microcomputer system can replace hundreds of TTL packages. Like other microcomputers, one basic system can be easily modified with software changes, virtually eliminating economic restrictions on the variety of sophisticated features that can be added to a product line now and in the future.

The family, designated the Intel MCS-48 (not an 8080 replacement) was designed with an unusual degree of flexibility in that its three central processors store their programs respectively in a masked read-only memory (ROM), an electrically programmable ROM, and in an external ROM. They are therefore useful in a wide variety of applications, from low-cost, high-volume consumer appliances, to small-volume and development projects, to systems requiring complex programs that will not fit the limited internal program memory. Aside from differences in program memory, the 8-bit processors are alike, incorporating read/write data memory, system utilities, a large input/output (I/O) subsystem, and comprehensive I/O control.

The 8048 is the masked ROM version, while the electrically programmable ROM (EPROM) in the 8748 is intended for product development, field engineering, product customizing, small lot production, and startup of volume manufacturing. In this device the program can be erased by exposing it to ultraviolet light. Both program memories have 1K-byte capacities—generous for most applications. The 8048 is hardware and software compatible with the 8748, and can be directly substituted when a system under development goes into high volume production.

The 8035 is equivalent to the other two devices, but without resident program storage. For example, a low-cost 2-chip system with an even larger I/O subsystem and twice the program storage capacity of the basic 8048 comprises the 8035 and only one other IC, such as the 8355.

Basic Single-Chip Microcomputer

All functions required for digital processing and control are integrated in the microcomputer (Fig. 1), al-

*Other semiconductor manufacturers are known to be developing their own single-chip microcomputers, which, however, do not have the alterable program memory, and are not expected to be in users' hands as soon as the devices described here—hence the use of the word "first." *Ed.*

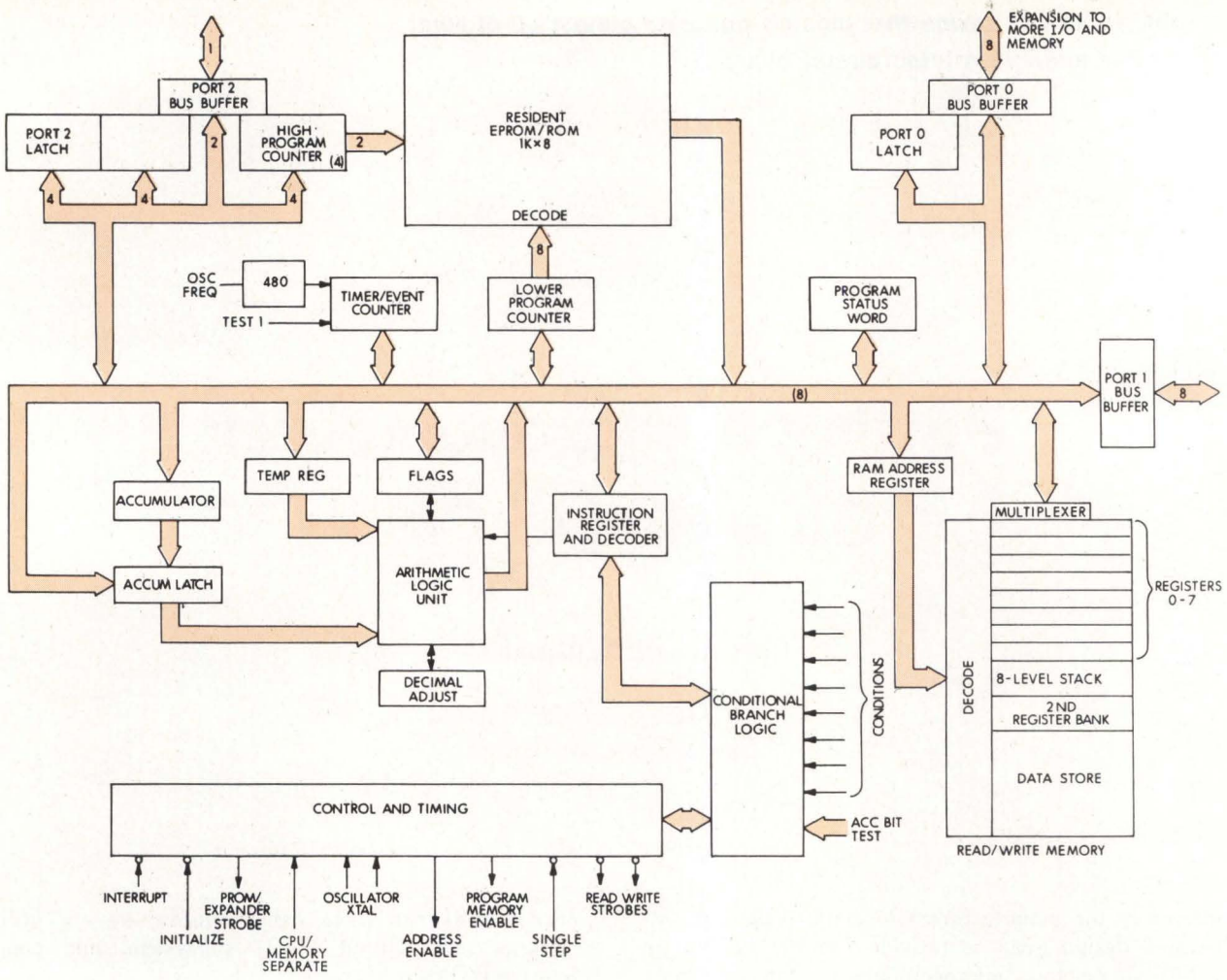


Fig. 1 One-chip computer. A single large-scale integrated circuit now contains all the subsystems required for operation as a computer—including memory and I/O. Its program is in a ROM which can be masked, electrically altered, or external in three versions of the device

lowing it to operate as a single-chip, standalone system, contained in a standard 40-pin package. A large, efficient instruction set enhances throughput, increases effective capacity of resident storage, and simplifies programming. Working registers, hardware stack, and data memory are integrated in a 64-byte static memory, giving the programmer flexibility in his use of read/write storage. The central processor operates in either 8- or 4-bit mode and can perform either binary or BCD arithmetic. It can service individual input and output (I/O) lines on the same port, set and reset bits, and perform logical processing operations on I/O data right at the interface. I/O servicing is further simplified by the placement directly on the chip of many functions, such as the counter/timer and the power-on reset, ordinarily implemented by peripheral circuits, and by facilities for testing external logic states.

All resident subsystems are externally expandable with both I/O and memory modules, standard memory devices, and programmable LSI peripherals developed for use with the 8080 family of 8-bit microprocessors.

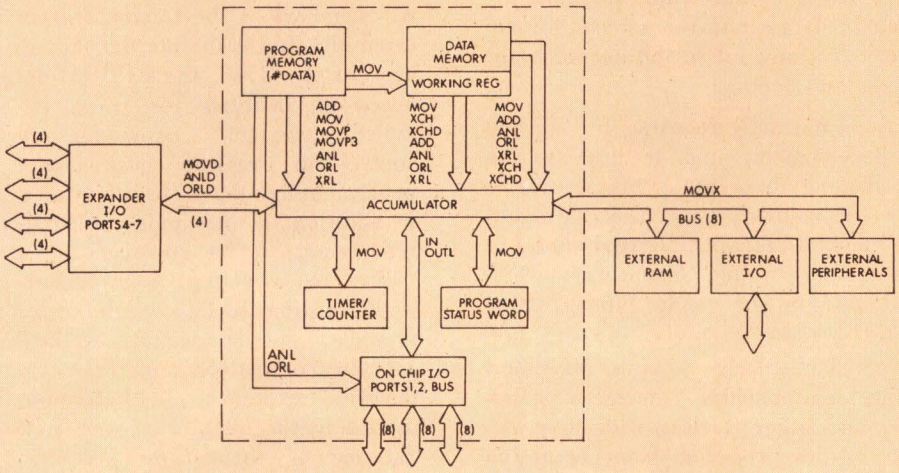
Central Processor

Integration of working registers, hardware stack, and data memory allows the programmer to use the most efficient combinations of these three storage techniques for each application. Resident read/write data storage for all three processors is in a 64-byte static memory. The programmer can assign up to 16 bytes as 8-bit working registers and up to 16 additional bytes as an 8-level, 16-bit-wide stack for nesting addresses and program status words. Working registers are organized as two banks of eight, to permit bank switching for immediate data save during servicing of interrupts and other subroutines. Interrupts come in on dedicated lines, as do certain external device states that are conditions for program jumps. The remaining 32 bytes permit random ac-

MCS-48 Family Instruction Set

Instruction	Accumulator	Register	Data Memory	Immediate	With Carry	Port	Bus	Expander	PSW	Ext Memory	Ext Interrupt	Timer/Counter	Remarks
Add	X	X	X	X	X								
AND/OR	X	X	X	X		X	X	X					
Excl OR	X	X	X	X									
Incr/Decr	X	X	Incr only										
Clear/Comp	X												Also carry and two flags
Decimal Adj													Note 1
Swap	X	X											Note 2
Rotate	X				X								L or R (carry through or past)
Move	X	X	X	X					X	X		X	
Exchange	X	X											Note 2
JMP													Unconditional
JMPP													Indirect
DJNZ													Decrement register and skip
J Cond													13 conditions
Call													
Return													With or without restore status
In	To					From	From	From					
Out	From					To	To	To					
Start/Stop												X	
Enable/Disable											X	X	
Select													Register bank or memory bank
NOP													

Note 1—Corrects two decimal digits packed in accumulator when either exceeds nine
Note 2—Swap a digit with register, or exchange two digits in accumulator



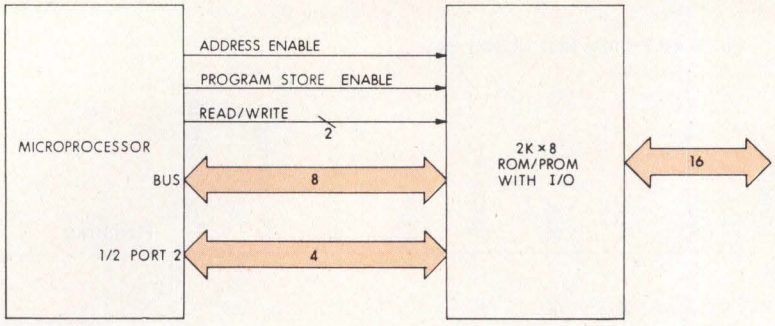


Fig. 2 External program memory interface. For programs that exceed the 1K x 8 internal ROM capacity of the microcomputer, an external memory is attached to one of the I/O ports

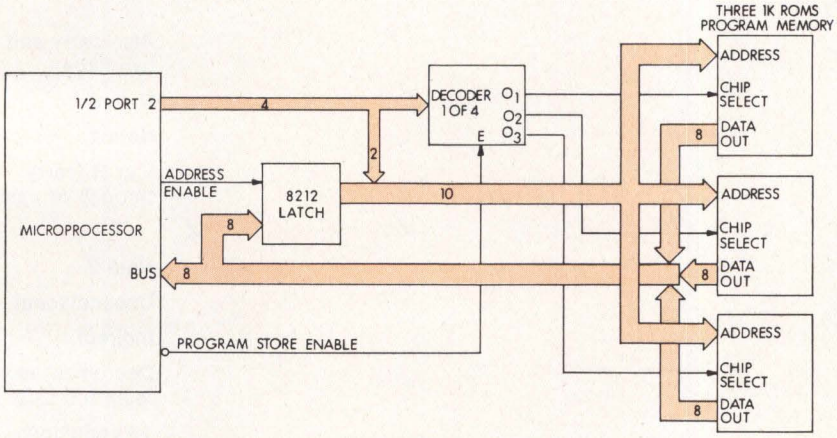


Fig. 3 Expanded program memory with standard devices. Up to 3K bytes of external program memory can be attached—4K if internal storage is not used

cess to data; more space is available when only one register bank or a shallower stack is used.

Most of the 96 instructions (see Table) are single-cycle and single-byte, and the basic instruction cycle time is 2.5 μs. The set includes bit manipulations, direct I/O data manipulation, interrupt, timer/counter, and binary/BCD operations, together with logical, fetch, and indirect operations. The system's I/O processing efficiency also compresses programs, making the 8048/8748 resident ROM/EPROM storage ample for most applications. An unusually large number of conditional branch instructions can test any bit in the accumulator, as well as various flags and inputs.

All auxiliary functions normally required for efficient operation, product development, and testing are included on the chip. Among these are a programmable interval timer and event counter, two maskable interrupt vectors, and a clock oscillator. External circuitry can be as simple as a few timing capacitors and resistors; however, timing can be made more precise with an external clock or crystal oscillator.

The timer/counter is particularly valuable for monitoring and controlling man-machine interfaces, printers, stepping motors, and other devices with long operating delays. It keeps the processor from becoming tied up in software timing loops, because it can interrupt the main program when it overflows—after 32 to 8192 instruction cycles or 1 to 256 external events have occurred. Meanwhile, timer contents can be read into the accumulator at any time, and the processor can test for overflow by a conditional jump instruction. The timer has a divide-by-32 prescaler, and the counter has 8-bit resolution.

Resident Memories

All members of the family contain complete addressing capability for both internal and external program storage. In the 8748, the EPROM is accompanied by the necessary facilities for using it—including an ultraviolet-transparent window for erasure and single-step control for program checkout and debugging. During programming, the 8748 requires a 25-V power supply, in addition to the single 5-V supply that all three processors require for operation.

This extra voltage requirement of the 8748, which would ordinarily be considered a disadvantage, instead presents a unique advantage to the 8048. All three processors are compatible, and the extra voltage is applied to the 8748 through a pin that compatibility might render useless in the 8048. However, by routing power to the data memory through this pin and to the rest of the chip through the regular 5-V pin, the system can shut off power to the rest of the chip while preserving data stored in

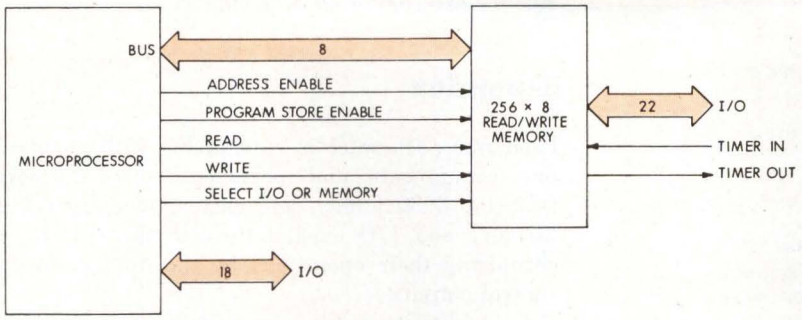


Fig. 4 External data memory interface. The 64-byte internal capacity of the microcomputer—though adequate for some applications—is nevertheless limited. Up to 256 bytes are directly addressable; bank switching extends this capacity virtually without limit

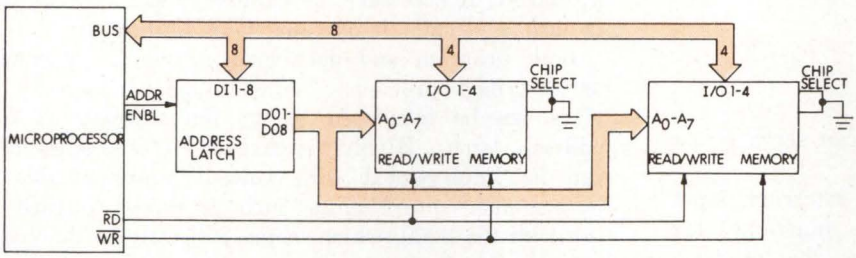


Fig. 5 Standard devices for data memory. Among useful circuits already in production that can be used with the microcomputer are a standard I/O port and latch and various 256 x 4 static read/write memories with access times of from 450 to 650 ns

memory. In this case the current drawn by the memory is only about one-tenth of that drawn by the chip as a whole, so the saving in critical applications can be significant.

To expedite system and product testing, an external access function in the control and timing section disables the internal program memory in the 8048 and 8748. These devices then operate, like the 8035, with all-external memory. This permits the processor to execute an external test routine or any other program stored off-chip.

For applications where 1K byte of program memory is inadequate, external ROM can be added to any of the three types. Whether a combination of internal and external ROM with the 8048, or all-external ROM with the 8035, is used, depends on details of the application and total program memory required, and relative prices of parts used. For example, the 8035 is priced significantly lower than either of the others, but there is little difference in price between an external 1K or 2K ROM.

For program storage (Figs. 2 and 3), the processor directly addresses up to 4K bytes. Of this capacity, 1K is resident and 3K is external, unless the external access function is used, when all 4K is external. For data storage, 256 bytes are directly addressable; when page addressing and bank switching methods are applied, virtually any amount of memory is addressable in 256-byte pages (Figs. 4 and 5). Of the eight working registers in each bank, two can be used to address expanded data storage when installed.

Resident I/O

Each single-chip microcomputer communicates with external equipment and components through 27 parallel I/O lines (Fig. 6). These have buffers, resident controls, and all generally required logic interfaces on the microcomputer chip. In addition, the system's timing and control section generates five control outputs. Data lines themselves are bidirectional, but the program can specify the direction of data flow, and can set and reset bits and perform logical operations on data at the ports.

Of the 27 lines, 24 form three 8-bit general-purpose I/O ports—system bus port, port 1, and port 2. System bus lines are not ordinarily latched, but become active only during data transfers. External memory modules as well as I/O controllers are attached to the system bus. Bus strobes synchronize data transfers with I/O and memory operations. Latches, however, are available on-chip, so that the system bus can also serve as a static port. Both port 1 and port 2 are static, and can operate with some bits incoming and some bits outgoing

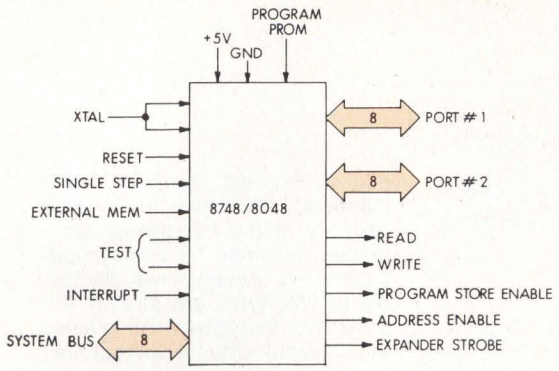


Fig. 6 Pin configuration. Standard 40-pin package includes connections for three I/O buses, two test inputs, and an interrupt line

at the same time. In addition, port 2 can serve as an I/O expander port, as described later.

The other three data lines are an interrupt input and two test inputs. They have various functions; for example, the interrupt input generates the program vector assigned to external interrupt sources, or can be used as an additional test line. With Test 0 and Test 1, external device states can be tested as special jump conditions by the conditional branch logic. Alternatively, Test 0 is an oscillator output derived as follows: the main system oscillator runs at 6 MHz, and its output is divided first by 3 and then by 5. The result of the first division, 2 MHz, is the Test 0 output; the second, 400 kHz, is the internal cycle frequency, or the frequency of the address latch enable line. Similarly Test 1 can be an event counter or second interrupt input —the latter occurring just after the counter overflows.

Five control outputs serve as a strobe for the I/O expander; read and write strobes to gate other devices onto and off the system bus; a cycle clock output that is also an address strobe; and a line to enable the external program memory.

Expansion

Each microcomputer is expandable with standard memory components and peripheral circuits, peripherals from the 8080 family, and custom memory components. Memory and I/O expand through the system bus, synchronizing their operations by the microcomputer's bus control outputs.

In addition, port 2 provides an independent I/O expansion bus. An I/O expander circuit can be attached to four lines of port 2 and to the expander strobe (Fig. 7). Many such circuits can operate on the same four lines, using the other four I/O lines and a decoder, if necessary, as chip-select signals. The 8243 is such a circuit; it contains four 4-bit ports.

Both program and data memory can be expanded, as described previously. Most standard memory devices can be interfaced to the bus through an 8-bit address latch. Highly specialized I/O requirements can be implemented with various programmable interface and control units, such as those designed for use with the 8080, which connect directly to the system bus. These units include a USART (universal synchronous/asynchronous receiver/transmitter), a programmable keyboard display unit, a programmable interval timer, a multilevel interrupt priority circuit, and multimode I/O ports. Use of these and other peripheral circuits is illustrated in Figs. 8 and 9.

Development Systems and Software

The Prompt-48 system programs any MCS-48 system, stores programs in the EPROM of an 8748, and executes programs in real-time, single-step, and multiple-

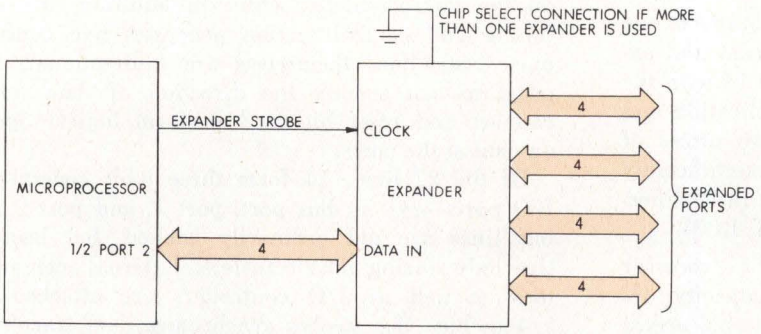


Fig. 7 Expander interface. To attach more I/O devices than the microcomputer can handle directly, an I/O expander chip can be connected to I/O port 2

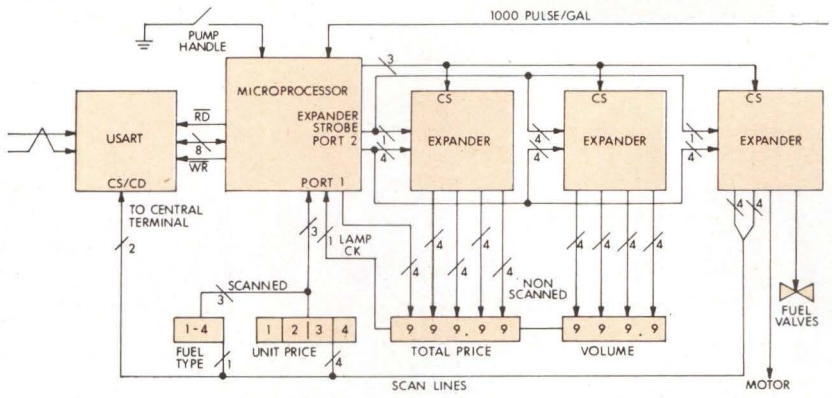


Fig. 8 Microcomputer-controlled gasoline pump. Inputs to the microcomputer are from the main controller via a USART, and from the pump handle, flowmeter, and manually set data on grade and price of fuel. Outputs via expanders control valves and pump motor, and display volume dispensed and total price

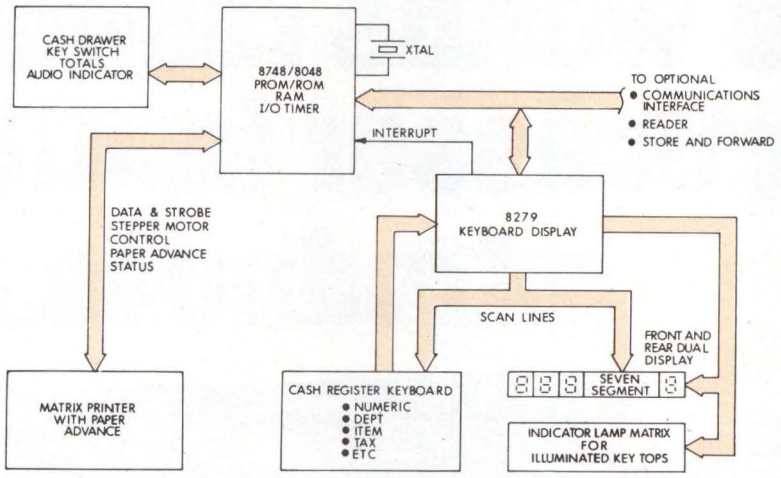


Fig. 9 Point-of-sale terminal. Microcomputer controls cash drawer, printer, and other electromechanical outputs on basis of data from the keyboard and remote data processing system

single-step modes. It includes a hexadecimal keyboard and display for manual entry, and has a teletypewriter interface for paper tape input and output. The system contains an 8748 microcomputer and provides for development of programs on the latter's EPROM, using its own built-in programmer. When the program is finished and debugged, the sock-mounted 8748 is transferred to the system it is destined to run. A second 8748 runs the development system with a resident monitor program. I/O lines from the 8748 are externally available at a connector, so that the unit can directly exercise and debug product breadboards and prototypes.

Similarly, the Intellec MDS supports programming, prototyping, and hardware/software debugging in the product's own environment. Intellec comprises an 8080 microcomputer system and numerous peripherals, such as diskettes, keyboard/CRT display console, line printer, p/ROM programmer, paper tape reader and punch, and teleprinter. After development, the unit stores programs automatically in the p/ROM or EPROM of the subject system. One of its most useful features is an in-circuit emulator—a cable that plugs into a socket in the subject system in place of the microprocessor that eventually will go there. By this means, program changes that will be in ROM in the finished system can be in a read/write memory in Intellec, and thus can be changed quickly and efficiently. An ICE-48 module has been designed for Intellec that extends this capability to the MCS-48, just as it has been used on the 8008, 8080, and other microprocessors.

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"MCS-48 Assembly Language Manual," Intel Corp, 1976
"PROMPT-48 Operator's Manual," Intel Corp, 1976
"Intellect MDS Operators Manual," Intel Corp, 1976

Howard A. Raphael is an engineering graduate of Rochester Institute of Technology and has done graduate work at the University of California. He is currently manager of low-end microcomputer products at Intel Corp.

M10800

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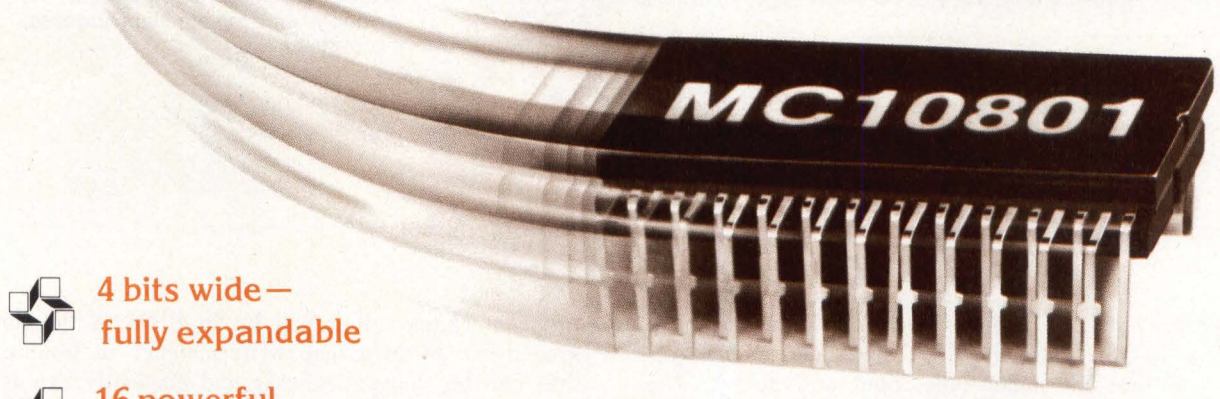

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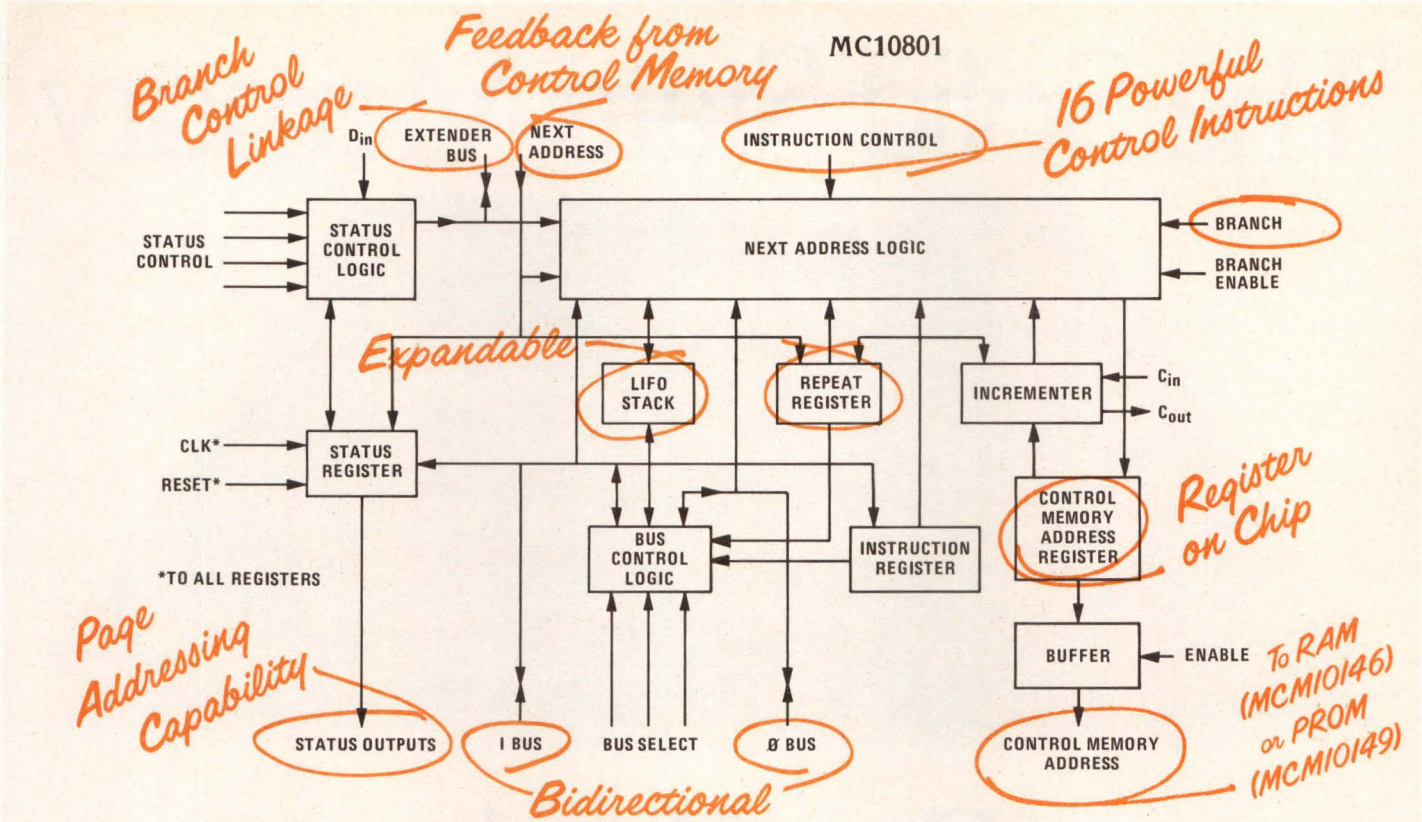
- 16 powerful microinstructions
- Control cycle 52 ns†
- 4 on-chip subroutine levels
- Instruction or subroutine repeat
- Standard MECL* LSI from the ECL leader
- 8 on-chip registers— including expandable 4 X 4 LIFO

Speed alone would place the MC10801 in a microprogram controller class by itself, but with this remarkable MECL LSI building block, speed is just the beginning.

Its 16 microinstructions and on-board registers make the MC10801 the most powerful microprogram controller as well as the fastest. Maximum system flexibility is ensured by five data ports. Generation of the next control memory address is possible from any of seven different sources; either I or Ø bidirectional bus, next address field, incrementer, either repeat or instruction register, or LIFO stack.

When the MC10801's four on-chip subroutine levels are not sufficient, expanding the LIFO stack via the I and Ø buses accomplishes nesting of more than four levels.

And there's still more. The repeat register permits big savings in control memory, particularly in large multiply or divide routines. Repeat capability for an instruction or subroutine is 2^{4n}, with "n" as the number of 10801s in the system. So with just two, you get 256 repeats. The number 256 points out another MC10801 feature, Page Addressing. Using the status register, multiple pages of 256 words can be addressed,

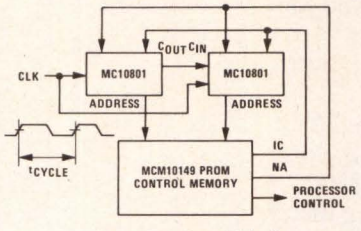


the world's most powerful microprogram controller.

†Control Cycle Speed Calculation

(logic delays – typical)

The MC10801 is the fastest microprogram controller by any measure, but nothing demonstrates that fact better than a system speed calculation like this.



CLK	→	Address Outputs (delay)	10 ns
PROM	→	Access (delay)	20 ns
IC	→	C_{OUT} (delay)	18 ns
C_{IN}	→	Address Register (setup)	4 ns
		t_{cycle} =	52 ns

again with only two units in most systems.

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MC10801	Now
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MC10805 (Bus Translator)	2nd Qtr '77
MC10806 (32 X 9 Dual Addressable Register)	2nd Qtr '77
MC10808 (Expandable 16-Bit Shifter)	2nd Qtr '77

MC10801 Control Instructions

- INC – Increment
- JMP – Jump to N.A. Inputs
- JIB – Jump to I Bus
- JIN – Jump to I Bus and Load Instruction Register
- JPI – Jump to Primary Instruction
- JEP – Jump to External Port (Ø Bus)
- JL2 – Jump to N.A. Inputs and Load Instruction Register
- JLA – Jump to N.A. Inputs and Load Address into Repeat Register
- JSR – Jump to Subroutine
- RTN – Return from Subroutine
- RSR – Repeat Subroutine
- RPI – Repeat Instruction
- BRC – Branch to N.A. Inputs on Condition otherwise Increment
- BSR – Branch to Subroutine on Condition otherwise Increment
- ROC – Return from Subroutine on Condition otherwise Jump to N.A. Inputs
- BRM – Branch and Modify Address with Branch Inputs (Multiway Branch)

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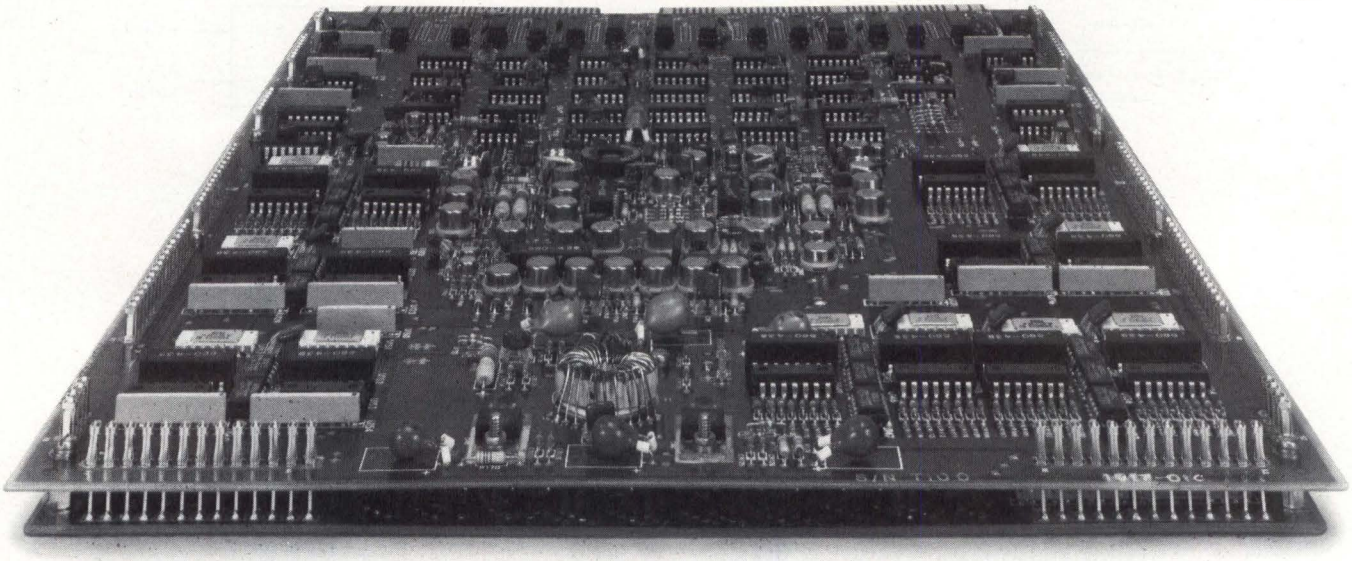
The Solid State Memory



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Choosing a testing system from the variety of models available is not easy, but insisting on characteristics that may not seem immediately essential pays off in the long run

Considerations in Semiconductor Tester Selection

David Alvarez

Mostek Corporation
Carrollton, Texas

Today, when the cost of not testing a large-scale integrated circuit or a metal-oxide semiconductor memory chip exceeds the cost of testing for any user of more than about 50,000 chips, the problem is not in deciding whether or not to test, but in selecting the right tester. The selection process is applicable to any tester, large or small. Regardless of what is to be tested or how much money is available, the goal is the same—to get the job done in the most cost-effective manner. Cost-effectiveness is the key issue in tester selection.

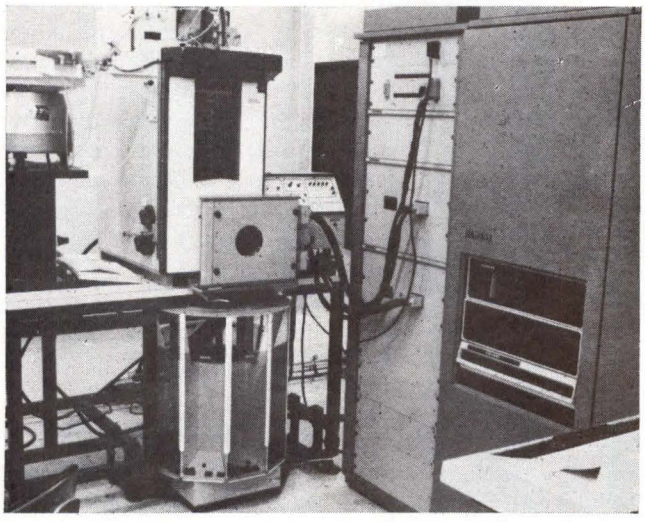

Fig. 1 Production tester. The primary requirements of versatility, reliability, and usability are present in the Siemens 203, which is typical of better testers on the market

At Mostek final production memory testing is done with Siemens 203 Semiconductor Memory Test Systems (Fig. 1); all hardware examples in this article are drawn from these units. However, the process of tester selection is quite general; detailed hardware/software evaluation is the last step in the tester evaluation procedure.

In some companies, a request for tester evaluation contains just two inputs: A panicky plea, "We needed it yesterday," and a sketchy description of the products to be tested. From these data the test department is expected to develop specifications. This dismayed awakening invariably illustrates the proverb, "Buy in haste, repent at leisure."

To avoid such an experience, a memory products test equipment group was established. Its main responsibility is to continually evaluate testers that might be required as they become available. This group neither operates nor maintains test equipment; it determines what equipment will be required, what should be purchased, and when to purchase it. The group maintains a close liaison with design and production engineering which permits it to anticipate the announcement of products that might require new testers.

How Evaluation Begins

Any evaluation process begins by examhining a number of testers. The overall evaluation procedure should consist of two major steps: evaluation of the proposed tester's general capability, and a detailed performance checkout. General capability should be evaluated

against the required testing at *your company*, taking into account versatility, reliability, usability, and cost-effectiveness, while the detailed performance check should confirm that proposed units perform as advertised.

Versatility should be defined broadly. Do not ask the vendor whether or not his tester can run this or that particular test; the reply is almost always "Yes," and by the time the tester is delivered, it will be able to run the test—the capability having been added to it because of the request. More important is the fact that tests are changed frequently, as products change.

Thus the tester must have a versatile approach to all tests. Versatility in this sense depends on the tester's hardware, its microprogram, its pattern generation, and in possible limitations in all these. For instance, some testers are controlled by a microprogram containing decoded instructions. These instructions specify incrementing, complementing, and so forth, but they cannot perform any two of those operations simultaneously because they are decoded, whereas a "bit-per-function" microprogram could. This immediately indicates lack of versatility. A tester with this shortcoming should offer quite a lot in other areas to warrant consideration.

Data Patterns Affect Versatility

Another versatility-sensitive area, particularly in memory testing, is the tester's ability to generate and alter data patterns. For instance, although the parity checking test is widely used on memories, many testers on the market today cannot do it, or can do it only with difficulty. They lack versatility; their data patterns are generated with an algorithm in the microinstructions, and parity can't be generated with an algorithm.

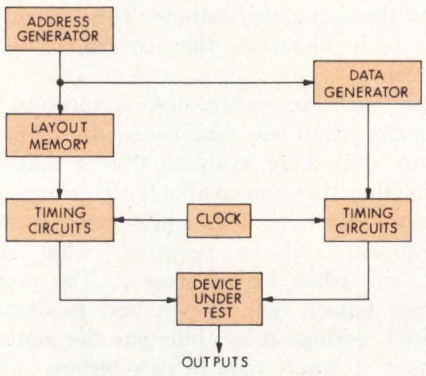

Fig. 2 Separate pattern generators. Although address and data generation can be combined as they are in some testers, versatility is enhanced when they are separate and largely independent

A more versatile tester will have separate address generator (the microprogram) and data generator (Fig. 2). While they are not totally independent—for example, the data generator is controlled by the address—they should not be built as a single unit. Although the microprogram may control the pattern, it should not define the pattern.

Separate data and address generators and "bit-per-function" microinstructions achieve a high level of tester versatility. For instance, they permit the tester to work simply with different chip layouts, such as the many metal-oxide semiconductor (MOS) memory designs in which consecutive addresses do not correspond to adjacent bit cells, but rather to cell locations chosen for reasons of chip layout. (After all, an integrated-circuit chip is like a printed circuit board in the sense that its layout generally bears little resemblance to the circuit schematic.)

The ability to accommodate such designs is very important in the "disturbed-cell test," in which signals are applied in sequence to the four or eight cells physically adjacent to the one under test. Clearly, this requires that the chip layout be known and the address sequence correspondingly scrambled. To do this scrambling in the microprogram would make the programs astronomically large. Conversely, to make a hardware modification for each of a variety of parts while keeping the tester current for at least 5 years after purchase becomes very troublesome. Such modifications are among the prime causes of tester reliability problems. However, if a tester cannot scramble the address sequence, hardware modifications may be the only alternative.

Control of data patterns is straightforward when the tester contains a separate data generator, where data patterns are controlled by the addresses, which in turn are controlled by the microprogram. Most patterns are produced by a simple hardware pattern generator, with provisions to "walk" them across the memory. For example, a "walking diagonal" pattern (Fig. 3) is controlled by an XYP algorithm generator as a function of passes through the memory.

Snowballing Test Times

Efficient data control is highly important because of the ever increasing complexities of MOS memories and the associated testing times. Right now use of 4096-bit MOS memories is rapidly increasing, and 16,384-bit MOS memories have begun to appear in products. They compound the problems found even in 1K memories that demanded a full N^2 test—one that

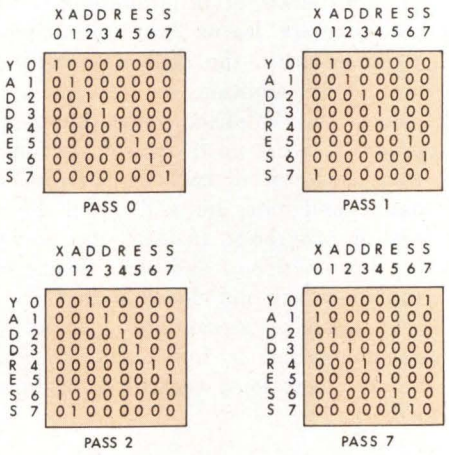

Fig. 3 Walking diagonal. This important test pattern is generated by a simple algorithm based on the relationship $N = X \pm Y \pm P$. N is the number of a bit in a particular row (0 to 7 in this example), while X and Y are the column and row addresses, respectively. When $P = 0$, the sum of X and Y puts a 1 in every bit cell diagonally across the memory array (which, incidentally, need not be square). During subsequent passes, P is incremented, causing the diagonal to "walk" across the array. Plus signs create the patterns shown here; minus signs are used for a diagonal upward to the right

requires the memory to be put through a number of cycles equal to the square of the number of bits in the memory. For a 1K memory, an N^2 test requires more than a million cycles; if each cycle takes only 500 ns, a single test would take half a second. Considering that in an extreme a given device might require as many as 1300 tests, total testing time becomes 650 s, or almost 11 min. For 4K memories, testing time for the same case would be 16 times as long, or about 3 h/device. This, of course, is totally unrealistic. We need not even mention how long the test would take on a 16K memory. (These times do not include printing the results, which, however, becomes negligible for larger arrays.) However, walking diagonal and other tests approximate the results of a full N^2 test without actually running it. Such patterns permit production technicians to spend, on an average, only 5 seconds of testing time on each 4K memory.

Obviously, fast testing is just as important to manufacturers as it is to large-volume users. Thus data generating and controlling capability are aspects of tester versatility that directly enable design of relatively fast but thorough tests.

Sometimes a certain feature of a tester overrides many other considerations. For instance, when the MK4096 4K memory was announced, no test equipment manufacturer had anticipated its multiplexed addressing capability. Multiplexing reduces the number of pins on the package, but requires address bits to be supplied in two batches, one after the other. On some earlier tester models, however, the necessary circuitry could easily be added. Today, several testers include this capability, greatly enhancing their versatility.

Practical Reliability

After versatility, the next general characteristic of a tester is practical reliability. By definition, practical reliability includes any and all factors that ensure maximum uptime or minimum downtime for a tester. This includes many factors other than mean time between failures (MTBF).

First, the tester should be built using reliable, sound engineering practices. This can't be determined by looking at brochures and schematics, but only by looking at the unit. Although it may involve dirty hands, examining a tester closely to determine how well it is built will pay off in spades in the overall evaluation process.

Next point in the reliability evaluation is the MTBF, evaluated in terms of downtime. If a unit goes down once a year, but takes two months to be repaired, it is not as good a buy as a unit with an MTBF of one week and a half-hour repair time.

Thus MTBF is closely related to maintainability. In a simply built tester, all parts are easily accessible, its operation can be clearly understood by maintenance people, and it can usually be fixed in a few minutes. The maintenance staff should consist of your own company's employees. Even if the quality of service provided by the tester manufacturer is very good, the time for an outside serviceman to come to the plant is too costly. (In our experience, one hour of downtime on a tester costs about $1000.)

Downtime can be caused by a number of factors. Some of these are legitimate component failures; others include test program changes and setup time. In addition, to ensure quality product shipments, testers must be kept calibrated. At Mostek, testers are formally

calibrated once every week; however, after each shift a group of known parts is run through each tester to verify its operation. If a tester fails to sort these parts properly, a maintenance crew is sent to determine the cause.

For these reasons simplicity of tester construction and operation are of the utmost importance. When examining a tester for simplicity, one has to ask these questions: Is the unit's design easy for maintenance people to understand? Are major sections laid out so that faulty blocks can be isolated quickly? Are parts that are likely to fail mounted in sockets for quick replacement?

From the maintenance point of view, some blocks of the tester should be usable to diagnose others. A separate data generator is an example of such a block. In troubleshooting it is often very convenient, in isolating a fault in a memory, to be able to scan one-half of memory, and if the fault is still present, to reduce the size by half again and again, until the faulty area is well isolated and can be examined in detail on an oscilloscope. This is easy with a data generator; however, where patterns are generated with a microprogrammed algorithm, every time the size of memory is changed, the microprogram must also be changed. Then after the program is altered, the problem may suddenly disappear. Was it because the tester is not scanning the faulty portion any more, or because the program was altered? In other words, this approach adds more unknowns, and in troubleshooting more unknowns are the last thing one wants.

Not having to change the program means that problem-isolation steps can be very fast. As anyone with troubleshooting experience knows, defining the problem is 90% of the job.

From the reliability point of view, tester versatility is beneficial only if it does not detract from reliability. That is, versatility achieved through complexity is likely to be at the cost of reliability.

Is the Tester Usable?

In a computer-based tester, communication is a serious problem. The only person who can write a really good test program for a given part is the engineer responsible for that particular product. In the case of a semiconductor manufacturer, this is the person who has been concentrating on possible failure mechanisms; in the case of a semiconductor user, the one who designed the system and knows what operational stresses each part will face.

If these people are to write efficient test programs, the tester must be usable. That is, design engineers should not spend excessive time trying to write a program.

To evaluate a tester for usability, write a few programs, based on your understanding of the machine. Writing an actual program is crucially important; it uncovers various eccentricities that every machine has and that, later on, will catch the product engineers who use it.

In testers, as in other applications, there are several different levels of programming. Usually, after a product engineer learns how to write a program for a given machine, the skill stays with him. The difficulty is that in addition to learning a programming language, the engineer must know the tester's microprogram, what each register in the tester is for, and what each bit in each register means. If he does not understand this, he will never be able to write successful programs. Instead, the resulting programs will be slow to debug and slow to execute; and when they run, they will not do what they are supposed to do.

In tester programming, as in all other programming, documentation is important. Poor documentation will hinder operations, regardless of how well the machine is built.

Is the Tester Cost-Effective?

After one or more testers have been determined to be suitable for the job from the standpoint of versatility, reliability, and usability, their relative cost-effectiveness should be considered. In essence, cost-effectiveness is a measure of machine speed, and how this speed compares with that of products to be tested.

The easiest way to determine these is to make comparisons on actual tests. With memories, for example, running time is not necessarily determined by the memory itself. That is, running a 500-ns memory for 1000 cycles, may be completed in 500 μs, or it may take longer. Testing time is increased by "overhead" or "dead" cycles.

A good example of dead cycles occurs in the disturbed-cell test. Suppose, after testing location 5, the effect of cycling location 6 and then location 4 is to be determined. To go from location 5 to location 6 merely requires a register to be incremented. Then, to get to location 4, the tester must either decrement the register by one twice, or have a special decrement-by-two instruction. Testers that decrement twice not only waste time, but do not even run a valid disturbed-cell test, because the two decrements necessarily require two cycles. Although the first of these, as far as the tester is concerned, is dead, to the device under test it is just another command. The device is addressed, executes a cycle, and provides data to the tester—which ignores the data because the cycle is "dead." Nevertheless, this reading process automatically refreshes the addressed cell. Since the purpose of the test is to measure the effect that cycling adjacent cells has on a particular cell, the intermediate refresh operation in the twice-decrementing case is self-defeating.

For some tests such considerations would not matter; the procedure could be eliminated or another one substituted. But the disturbed-cell test is crucially important for MOS devices, because they are very densely

packed. Leakages easily develop between closely packed transistors and capacitors. The disturbed-cell test is a good way to spot such leakage paths quickly. Going around just once may not be enough; some tests go several times around each cell to uncover weak spots.

Using a Tester for Other Jobs

Testers used primarily for production or incoming inspection testing can also be used for other purposes. Their usefulness in those other jobs should be kept in mind during an evaluation.

One heavy use of a tester by a semiconductor manufacturer is in characterization, a detailed study of devices that are being developed. When used in production testing a unit generally produces go/no-go results; in device characterization, however, it serves as a precision measuring instrument, printing all readings as they are taken. These readings establish operating limits of the device.

Versatility and usability considerations are important in evaluating a tester for device characterization, because the ability to perform intricate tests quickly and accurately is particularly important for such work. The tester may also be called upon to correlate test results obtained by other methods and on different testers. For example, a semiconductor user might want to evaluate MOS memories purchased from different vendors. Each vendor may have used a different tester. To compare results of such tests, the user's tester should be able to run a variety of similar tests.

Similarily, a semiconductor manufacturer needs a versatile tester, because occasionally a customer, after running tests on a shipment of semiconductor devices, will return the shipment as defective. When this happens, our first step is to repeat the standard final production test. If the devices pass this test but are still found defective by the customer, attempts are made to reproduce the customer's tests on the manufacturer's testers. Reproducing any customer's test on our system demands a very high degree of versatility in the tester. So does a rather extensive program, called the "Correlation Package," which, together with the results of the reproduced test, usually identifies the problem. The correlation package contains comments collected from various customers over several years, and helps to answer questions concerning part performance under various conditions, such as varying timings and supply voltages with respect to each other, in different combinations. There is a good chance that the customer's test conditions have been duplicated in the correlation package.

Getting Down to the Nitty-Gritty

After evaluation of general capability has been completed, the number of candidate testers is usually reduced to the few machines that are worth checking out in detail. As a first step, more programs should be written. These should examine every register and every bit in each register to verify their purpose and operation. Although they need not be run on a tester, they should make sure that the registers can be used as needed. The programs will be run during acceptance tests, after the machine has been selected, ordered, and delivered.

Next comes evaluation of detailed specifications. It is highly important to understand them from a user's point of view. That is, if the vendor claims a clock resolution of 50 ps, the user's first reaction should be "Why is this desirable?" Some testers have analog clocks and some have digital clocks (Fig. 4); the former supposedly can achieve higher resolution. A digital clock, however, is as reliable as its crystal oscillator (which can be very reliable), while almost any resolution is achievable with a suitable choice of frequency. For example, a standard 125-MHz crystal provides 8-ns

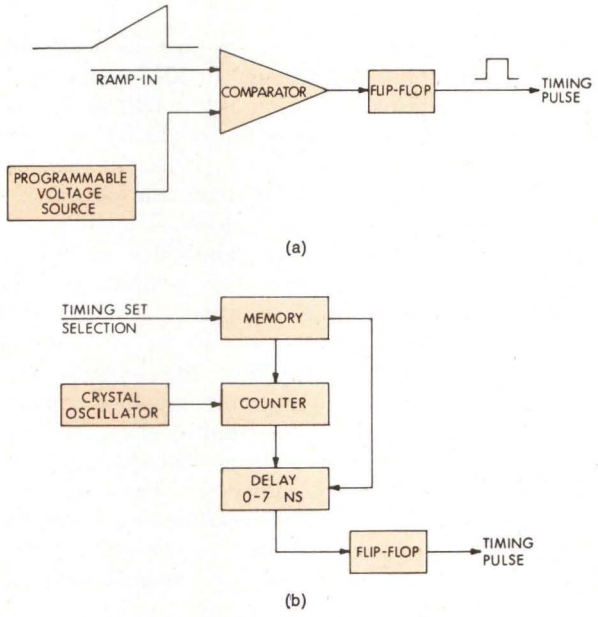

Fig. 4 Two kinds of clocks. Analog clocks (a) are simple and are sometimes claimed to have better resolution; however, they are difficult to program precisely. Digital clocks (b), on the other hand, can have the degree of resolution desired, and can be reprogrammed easily to control any of a variety of tests

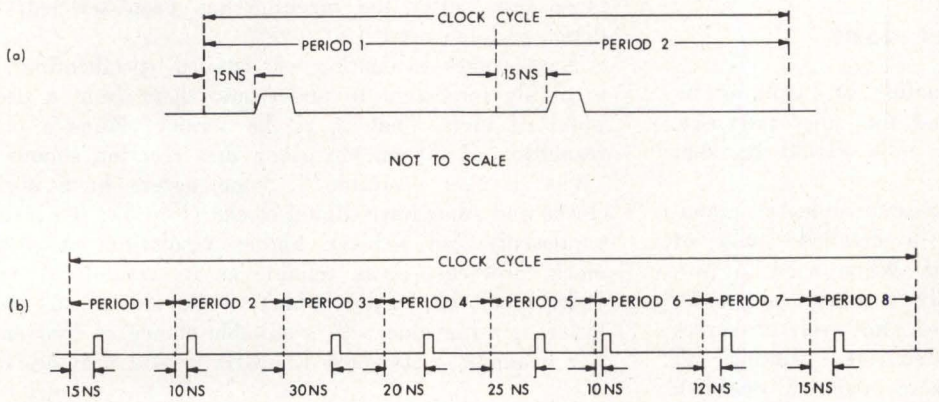

Fig. 5 Clock cycle division. When periods within a clock cycle must be identically subdivided (a), versatility suffers. The Siemens 203 has eight periods (b), each of which can be subdivided 12 ways for a total of 96 independent events

resolution which can be improved to 1 ns with delay lines. This is the arrangement in the tester under discussion. Since 1-ns resolution is enough, except possibly for testing emitter-coupled logic (ECL) memories, which have cycle times of around 10 ns, digital clocks are considerably more flexible than the analog.

In many testers, each clock cycle is divided into two periods, each of which can be subdivided into several timing intervals for controlling data, address, etc (Fig. 5). One of these two periods is usually a subset of the other. That is, if a pulse occurs 15 ns after the beginning of the first period, then the second period must also have a pulse at the corresponding time. In the Siemens 203, however, the digital clock has eight fully independent periods with no subsets, and each period can have up to 12 intervals. Thus up to 96 independent events can be programmed—a very high degree of flexibility. It is difficult to conceive a timing arrangement that could not be programmed with such a clock.

Another important step during the detailed evaluation is to review acceptance procedure. This review determines the purpose of each test, how it relates to proving the tester's versatility, reliability, and usability. It requires a thorough understanding both of the user's needs and of testers in general.

Is the Tester Cost-Effective?

Finally, the cost-effectiveness evaluation should be repeated, on the basis of a good understanding of each candidate, both on general and detailed levels. Here judgment comes into play. For example, if 1-ns resolution is not needed now but will be in the future, and if it does not raise the price too much, it might be worth buying right away.

This kind of examination should be conducted for all the important tester specifications in order to obtain the most per dollar spent, particularly if two or more testers come out nose-to-nose on versatility, reliability, usability, and other considerations.

All in all, the selection of a tester calls for clear understanding of needs and good knowledge of state-of-the-art measurement techniques. It also requires hard work and a lot of common sense.

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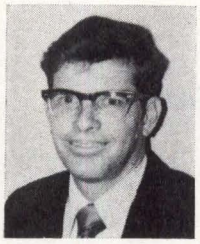
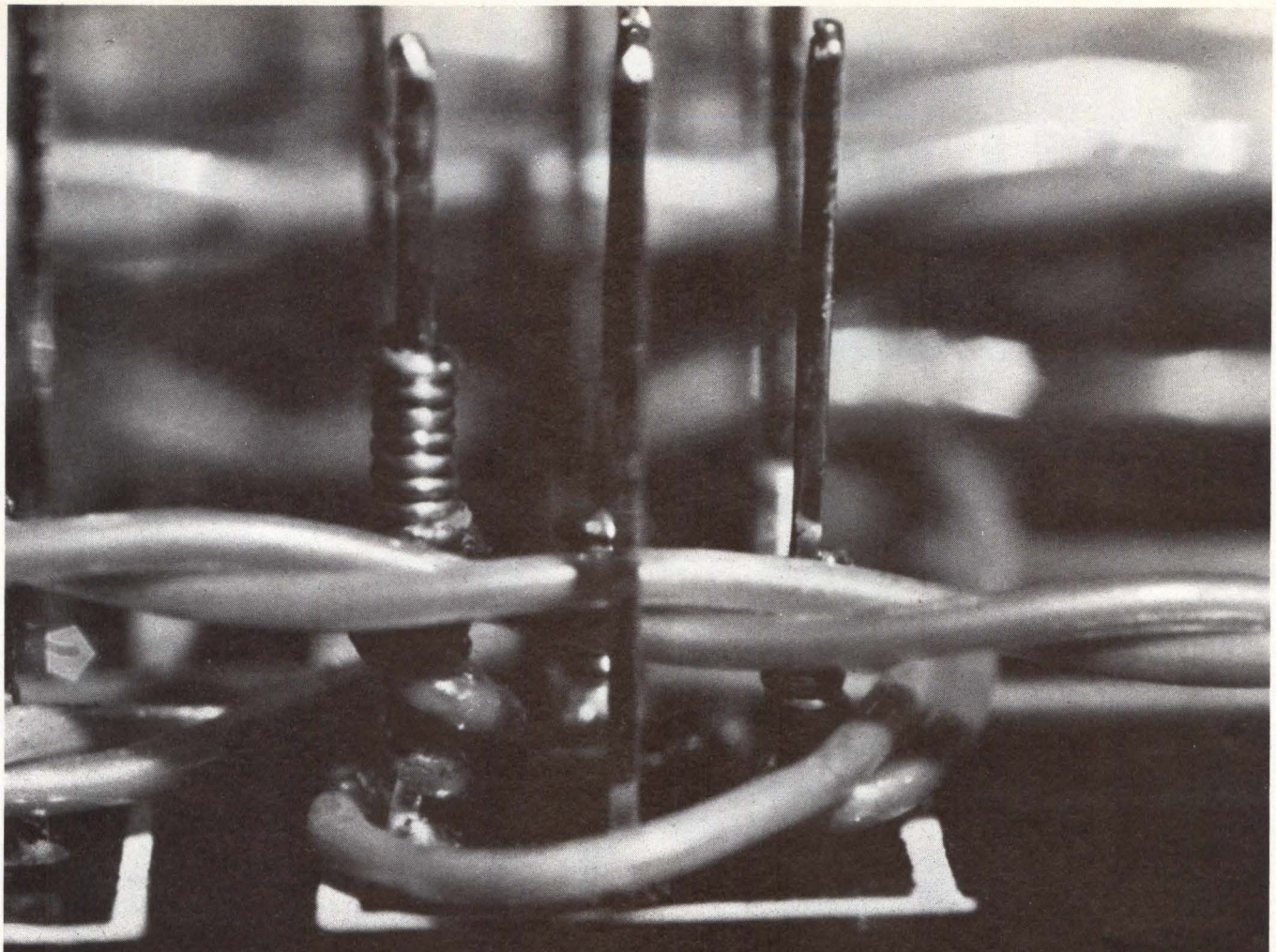


David Alvarez received his BSEE degree from Louisiana State University. Presently the manager of the memory products, test equipment group at Mostek, his experience includes the design of supervisory control and data acquisition systems, and work in memory test systems design.



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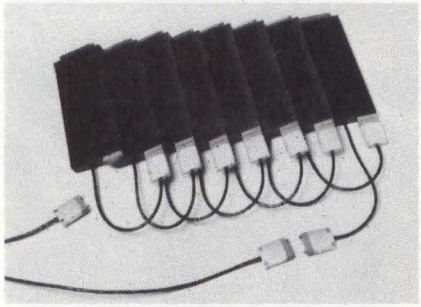

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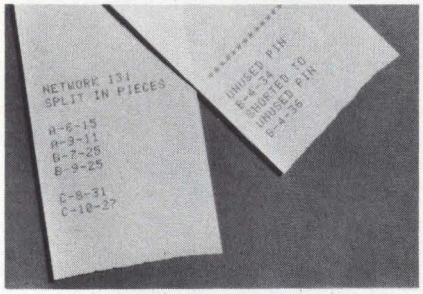

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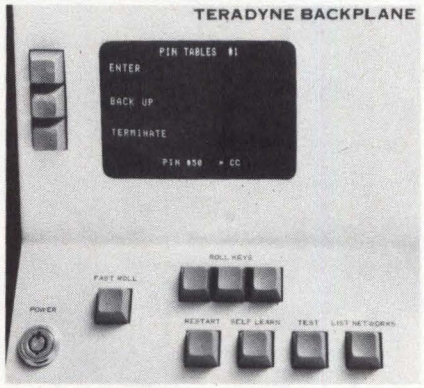

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Control flags permit the process control engineer to make multiple decisions in control programming, to decode various kinds of input signals, and to issue different control signals in response

Decision-Making With Flags in Process Control

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Berkeley, California

Control flags are important elements of microcomputer architecture. These flags provide the process control engineer with decision branch points that are responsive to process condition signals and alarm interrupts in real-time process control applications. To the microcomputer programmer the control flags are essential for development of multiply branched programs. Yet, using control flags effectively in the programming of microcomputers seems to be a black art to some users—unnecessarily, in our opinion.

Most microprocessors contain an arithmetic/logic unit (ALU) that is capable of carrying out a variety of important operations. They also contain a series of flip-flops or latches, which, as a result of these arithmetic and logic operations, are set to the binary values 0 or 1. These values constitute the microprocessor's control "flags." They record conditions which, in conjunction with conditional branching instructions in the microprocessor program, provide the engineer with powerful tools for developing efficient process control programs with multiple branches.

The flags most commonly available in currently available microprocessors are carry (C), zero (Z), sign (S), and parity (P). These are set by arithmetic and logic operations within the microprocessor to the binary values 0 to 1 and are used in an impressively wide number of ways in programming. The state of the condition flags resulting from arithmetic and logical operations are summarized in the Table. It is interesting to note that if any one of the four flags shown in the table were missing, its value could be calculated from values of the other three flag bits and from some additional microprocessor code. Flag bits are the sole repository of information required to effect all conditional branching within the microcomputer program. There is no one use for any of the flag bits; on the contrary, each application can use them in a unique way to implement its own meaning. Furthermore, special uses are often found that do not fit standard usages.

The arithmetic functions add, add with carry, subtract, subtract with borrow, and compare can be executed between any of several registers and the accumulator in the central processing unit (CPU) of a microcomputer, between memory and accumulator, or between an octal number in a program instruction and the accumulator; logical operations, AND, OR, and exclusive OR, can also be executed between the accumulator and any register, as well as a memory location or an immediate operand listed in the program; and counting operations increment and decrement can be performed using several microprocessor storage registers. All of these instructions set or reset one or more control flags depending on the result of the operation. In addition, the operations rotate-accumulator-left and rotate-accumulator-right shift the most and least significant bit of the accumulator, respectively, into the carry flag bit.

Programs make decisions based on conditions recorded in the flags through operations such as call, jump, and return. When these instructions appear in

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Effect of Arithmetic and Logic Instructions on Control Flag Values*

Control Flag	Value	Arithmetic	Boolean	Compare	Shift	Increment/Decrement
Carry	True	Overflow on add Underflow on subtract	—	$X < Y$	Previous bit = 1**	(Not affected)
	False	Result in range	All Boolean operations	$X \geq Y$	Previous bit = 0**	(Not affected)
Zero	True	Result = 0	All bits = 0	$X = Y$	(Not affected)	Result = 0
	False	Result $\neq$ 0	Some bits = 1	$X \neq Y$	(Not affected)	Result $\neq$ 0
Sign	True	MSB = 1	MSB = 1	MSB = 1	(Not affected)	MSB = 1
	False	MSB = 0	MSB = 0	MSB = 0	(Not affected)	MSB = 0
Parity	True	Even number of 1 bits	Even number of 1 bits	Even number of 1 bits	(Not affected)	Even number of 1 bits
	False	Odd number of 1 bits	Odd number of 1 bits	Odd number of 1 bits	(Not affected)	Odd number of 1 bits

*Based in part on "Flags," XKR Research, Richmond, Calif
**Previous bit is MSB (D7) on shift left, LSB (D0) on shift right

the program code and a flag is specified, they are executed only on the correct flag condition, which may be specified as either the true (flag bit value = 1) or false (flag bit value = 0) state. If the flag is not in the specified state, the instruction is not executed. Four flag bits thus provide a total of eight selectable conditions. In fact, exactly three bits of the instruction code are used to encode the possible conditions that the flags present.

Repetitive Operations

Repetitive operations or operational sequences are frequently encountered in process control. Often a series of repetitive tasks must be performed a fixed integral number of times before process conditions are reset, or control is switched to another series of operations. Such repetitive operations are easily controlled in the microcomputer by means of a sequence counter, a comparison operation for setting a control flag, and a conditional jump instruction.

A sequence of operations in a repetitive process can be executed a specified number of times by decrementing a counter initially set equal to the number of repetitions. When the counter value is greater than 0, a conditional jump instruction, jump if not zero, returns the program counter to the beginning of the routine. When the counter is decremented finally to 0, the conditional jump does not execute and the program continues, or "falls through" the loop, to the program continuation.

A sample program using the zero control bit can be written using instructions LBI, DCB, and JFZ (mnemonics for the Intel 8008 microcomputer). LBI precedes the sequence of operations that is to be repeated; it loads register B with the operand of the instruction, which immediately follows the instruction itself. After each pass through the repetitive process, DCB decrements register B, and JFZ returns the program to the beginning of the routine if the decrement did not leave a zero in the register (JFZ = jump on false zero). Eventually, of course, the register will reach zero, the jump will not occur, and the remainder of the program will be executed. Program Listing 1 summarizes this process.

Branching Based on Status Bits

Temporary storage of flag bits in a CPU register or memory address is exceptionally useful whenever the program must be restarted after a program interrupt, caused by one of the devices cooperating in the process control action. If the microprocessor contains a push-pop stack that is accessible to the programmer, this temporary storage can be relatively easy; but it has large advantages even when no stack is available. For example, the Intel 8080 has push and pop instructions in the CPU instruction set for this purpose, whereas the 8008 does not. Any 4-bit binary word containing the flag bits is called a status word; its image, stored in a CPU register or memory location, must be updated following each intermediate result wherever a program interrupt is likely. The status word is accessible with the help of an instruction that moves the word from the register or memory to the accumulator. (In some microprocessors flag bits themselves, not their image, are kept in a memory word, because a limited number of CPU registers are individually accessible.)

The four low-order binary bits of an 8-bit word can be set aside as a status word for storing intermediate flag values in memory. Then, if a program branch is necessary at a later time, after the flags

PROGRAM LISTING 1

Using Zero Control Bit for Repetitive Operations

Address	Mnemonic	Operand	Comments
	LBI	n_8	Load register B with the value n_8
ENTRY1	INST		Main loop (series of instructions)
	INST		
	•		
	•		
	•		
	•		
	INST		
	DCB		Decrement register B (sets zero, sign, and parity flags as appropriate)
	JFZ	ENTRY1	Jump back to start of main loop if zero flag is not set; otherwise continue
	NEXT		Continuation of program

PROGRAM LISTING 2

Branching Based on Status Bits

Address	Mnemonic	Operand	Comments
	LAM		Move status word from memory to accumulator
	RAR		Rotate low-order bit into carry bit
	JFC	ENTRY2	Jump to subroutine if carry flag = 0; otherwise continue in sequence
	NEXT		
	•		
	•		
	•		
ENTRY2	INST		Subroutine
	INST		
	•		
	•		

have been changed by an interrupt or other subsequent processing, the status word stores the necessary conditions. An example of this method in testing the lowest order bit (Program Listing 2) uses the instructions LAM, RAR, and JFC. LAM moves the status word from the memory into the accumulator; RAR shifts the whole word one position to the right, placing the low-order bit, which falls out of the end of the accumulator, into the carry flag; and JFC jumps to a specified subprogram if the carry flag is not set. Additional RAR instructions, up to four, move other status bits into the carry bit; the jump is always taken on the basis of the carry bit value (true or false), even though the condition for the jump is based on one of the other flags.

A status word can also record the states of up to eight latches which, when closed, actuate different process control functions. The status word stores the instantaneous set of process control actions and, therefore, represents the control state.

Branch Points Based on Flag Bits

Three flag bits are sufficient for conditional branching on all four combinations of two control bits. As an example, consider bits 6 and 7 of a test word as control bits set by a preceding operation (Program Listing 3). After loading this test word into the accumulator, all other bits can be set to 0 with the instruction NDI 300. (Note that the AND-immediate instruction NDI operating on 300 gives the logical AND of the octal number 300 and the contents of the accumulator; this operation forces a 0 into accumulator bits 0 through 5 and permits the 0 or 1 state of bits 6 and 7 previously in the accumulator to remain unchanged.

PROGRAM LISTING 3

Branch Points Based on Flag Bits

Address	Mnemonic	Operand	Comments
	LAM		Move test word from memory to accumulator
	NDI	300	Mask bits 6 and 7; set other bits to 0
	JTZ	ENTRY4	Jump to 1st subroutine if zero flag = 1 (ie, if both bits 6 and 7 are 0)
	JTP	ENTRY5	Jump to 2nd subroutine if parity flag = 1 (ie, if both bits are 1)
	JTS	ENTRY6	Jump to 3rd subroutine if sign flag = 1 (ie, if bit 7 = 1, bit 6 = 0)
ENTRY7	INST		Begin 4th subroutine, executed if bit 7 = 0, bit 6 = 1
	INST		
	•		
	•		
	•		
ENTRY4	INST		Begin 1st subroutine
	•		
	•		
ENTRY5	INST		Begin 2nd subroutine
	•		
	•		
ENTRY6	INST		Begin 3rd subroutine
	•		
	•		
	•		

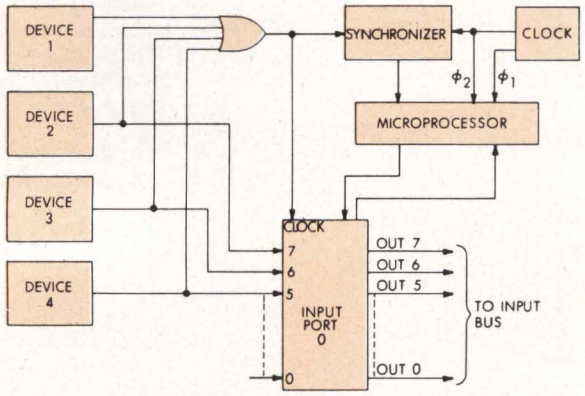

Fig. 1 Interrupt decoder. Any interrupting device except Device 1 sets a latch in the input port. When the microprocessor samples the port, its content identifies the interrupting unit

If bits 6 and 7 are both 0, the whole accumulator now contains eight 0s, the zero flag is set, and the instruction JTZ (jump on true zero) branches to the location specified by program code appearing in the program following the JTZ instruction. If both bits are 1, the parity flag is set, and JTP (jump on true parity) branches to a second location in the program. (Zero test must be made first, because the parity flag is set under both conditions.) If bit 7 = 1 and bit 6 = 0, the parity bit is not set, but since bit 7 represents a negative quantity, the sign flag is set, a condition for branching to a third program location (JTS). (Here again, parity test must be made before sign test, because the sign bit is true both times.) If none of these conditions are met, the program falls through all three tests; the result of this fourth condition (bit 7 = 0, bit 6 = 1) is that the program following immediately in sequence, or reached by an unconditional jump after the JTS instruction, is executed. Thus, the two bits used as a status word allow four possible subprograms to be executed.

Branch Points Based on Process Interrupts

Many dedicated control applications of microcomputers use multiple program interrupts from process alarm devices or from the operator console to change the process flow. In small industrial or laboratory-based microcomputer systems, a number of interrupt devices—process monitors, alarm indicators, or operator inputs—can be separately identified with one interrupt level by decoding the input device signals with a skip-chain technique. This is essentially a series of conditional jumps through which the program falls until it finds an existing condition and jumps to the appropriate subroutine. Sometimes intervening instructions modify the conditions to simplify the jump, as in the following example.

In a single-vector, multiple-device interrupt decoder, three of four interrupt devices, which could be a power-failure indicator, a fire alarm, a real-time clock, and an analog-to-digital converter, are connected through a bidirectional bus driver (input port 0) to the input data bus of a microcomputer (Fig. 1). All four interrupt-request lines are combined at an OR gate and sent to the INT input terminal of the microprocessor through a synchronizer, which insures that the signal arrives at the microprocessor at the same time as the clock phase 2 signal.

When the microprocessor receives a signal pulse from any one of the interrupt devices, the signal is also present on one line of the input data bus through the bidirectional bus driver (except, of course, when the interrupt comes from the one device not connected to the bus). The microprocessor puts the contents of the program counter on the program stack and executes a so-called hardware jump (RST 0) to memory location 000, where it finds the first instruction of an interrupt-decoding program (Program Listing 4).

This first instruction calls a subroutine, SAVEST, which stores the contents of all operating registers and flags

PROGRAM LISTING 4

Branch Points Based on Process Interrupts

Address	Mnemonic	Operand	Comments
	CAL	SAVEST	Save operating status registers and flags in random-access memory
	INP	0	Fetch the interrupt register contents
	JTZ	SERD 1	If zero flag = 1, because interrupt register is all 0s, jump to the service routine for device 1
	RAL		Rotate accumulator left through carry
	JTC	SERD 2	If carry flag = 1, go to service routine for device 2
	JTS	SERD 3	If sign flag = 1, go to service routine for device 3
	JMP	SERD 4	Otherwise go to service routine for device 4
	OUT	0	Clear interrupt register (input port 0)
	CAL	RESTART	Restore program status present at time the interrupt occurred
SERD 1	(Service routine 1)		Execute service routine required by interrupt device 1
•			
•			
•			
SERD 4	(Service routine 4)		Execute service routine required by interrupt device 4
RESTART	(Restore status)		Subroutine to restore program status. Jump to ENTRY8
ENTRY8	(Continuation)		Program continuation

in memory so that they will be available for servicing the interrupts. The difference between a call and a jump is small but important. In the absence of either, instructions are executed in sequence by incrementing the program counter for each one; a jump, instead of incrementing the counter, replaces its contents with (in general) a wholly different address, effectively transferring execution to an entirely different part of the program. A call has the same effect, but before loading the new address into the counter, it stores the old one (which has been incremented) in a stack in a reserved section of memory. As a result, the subroutine to which a call branches can have, as its last instruction, one that brings that stored address out of memory and replaces it in the program counter. Thus a jump burns its bridges behind it; a call does not.

In this way, following execution of the subroutine SAVEST, the program returns to the second instruction in the listing, which brings in the contents of the interrupt register. If device 1 was the one device not connected to the bus and was the source of the interrupt, the interrupt register contains all 0s; bringing it in sets the zero flag. Therefore, the third instruction, JTZ, branches to the appropriate routine, SERD 1, for servicing device 1. If this fails, the next instruction rotates the accumulator one position to the left, bringing the next bit into the most significant position. The old and new bits in this position respectively set (or reset) the carry and sign bits, so that two more conditional jumps take the program to routines for servicing devices 2 and 3. If these too fail, the fourth device must have been the source of the interrupt, and an unconditional jump to its subroutine takes care of it.

Since more than one device can trigger the interrupt simultaneously, all of these tests should be made. For this reason, conditional calls, rather than jumps, are sometimes preferred; they return to the interrupt-decoding routine after each service, and wind up by clearing the interrupt register with the OUT 0 instruction. Conditional call instructions are found in the 8080 instruction set, but not in the 8008 set.

A useful way to terminate the interrupt-decoding program is to use the unconditional call instruction to transfer control to a RESTART routine which restores the registers and values of flags (the opposite of SAVEST) originally present at the time of the interrupt, so that the main program can resume operation.

Examples of service routines include plant subprocess shutdown, transfer to temporary manual operating status, execution of critically timed events, and process continuation with minimum delay following operating cycles involving external, high-speed equipment.

These examples demonstrate the effectiveness of program branching based on four control bits in microcomputer programming. Some currently available microprocessors and others under development have more than four control flags, allowing even greater possibilities in process control and programming.

Accessing the Values of Flag Bits

Although all microprocessors generate control flags in some form, not all maintain a separately accessible register for storing them. Consequently, a software

PROGRAM LISTING 5

Accessing the Values of Flag Bits

Address	Octal Code Op Code	Operand	Symbolic Code Label	Instruction	Operand	Comments
035 000	026	000	FLOUT	LCI	000	Clear C register
	046	000		LEI	000	Clear E register
	056	000		LHI	000	Clear H register
	066	000		LLI	000	Clear L register
	100	015 035		JFC	ENTRY1	Skip if carry flag = 0
	026	001		LCI	001	Set carry flag in C reg
035 015	110	022 035	ENTRY1	JFZ	ENTRY2	Skip if zero flag = 0
	046	001		LEI	001	Set zero flag in E reg
035 022	120	027 035	ENTRY2	JFS	ENTRY3	Skip if sign flag = 0
	056	001		LHI	001	Set sign flag in H reg
035 027	130	034 035	ENTRY3	JFP	ENTRY4	Skip if parity flag = 0
	066	001		LLI	001	Set parity flag in L reg
035 034	106	064 035	ENTRY4	CAL	FLFOR	Print flags
	106	031 030		CAL	OOC	Output octal character from C
	326			LCE		Load reg C from reg E
	106	031 030		CAL	OOC	Output octal character from C
	325			LCH		Load reg C from reg H
	106	031 030		CAL	OOC	Output octal character from C
	326			LCL		Load reg C from reg L
	106	031 030		CAL	OOC	Output octal character from C
	106	161 030		CAL	LFCR	Line feed, carriage return
035 061	104	351 030		JMP	RUTS	Jump to operating system
035 064	106	161 030	FLFOR	CAL	LFCR	Line feed, carriage return
	006	303		LAI	ASCII:C	Set ASCII "C" in accum reg
	106	036 030		CAL	OTC	Output byte in accum
	006	332		LAI	ASCII:Z	Set ASCII "Z" in accum reg
	106	036 030		CAL	OTC	Output byte in accum
035 101	006	323		LAI	ASCII:S	Set ASCII "S" in accum reg
	106	036 030		CAL	OTC	Output byte in accum
	006	320		LAI	ASCII:P	Set ASCII "P" in accum reg
	106	036 030		CAL	OTC	Output byte in accum
	106	161 030		CAL	LFCR	Line feed, carriage return
035 116	007			RET		Return to calling program

program is necessary to interrogate the flag bit values and to transfer them to an output device such as an alphanumeric display or a printer. Interrogating the flag bits, however, poses a unique problem: it must employ no operation that alters or resets the flag bits. Examples of usable instructions are those that load a register directly from the instruction (load-immediate), conditional and unconditional jump and call.

A simple program to interrogate and display the flag bit values (flowchart, Fig. 2) utilizes conditional jumps to test each flag bit in sequence, and to load immediately one of four CPU registers with the numerical value 1 if the flag bit is true. The least significant bit (LSB) of the four registers is then printed on a line below the flag register symbols, "CZSP." Such a program can easily be made a part of the operating system by putting it in a read-only memory.

Such a program for displaying the values of flags, using the instruction set of the Intel 8008 microprocessor, is shown in Program Listing 5, in both mnemonic and octal form. The main program extends between locations 35000 and 35063 inclusive; a subroutine,

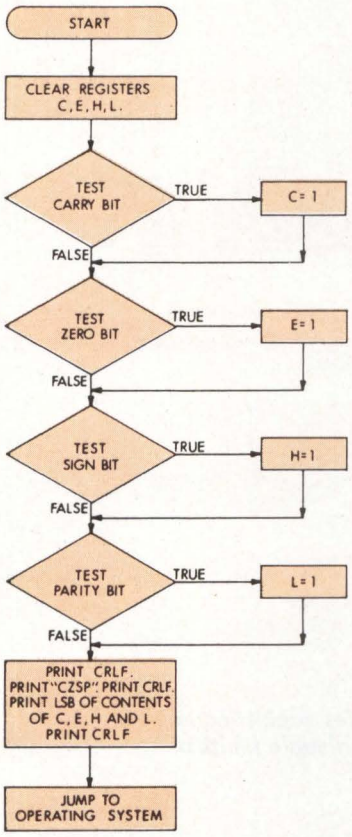

Fig. 2 Flag display. If flags are not directly accessible, they can be displayed by a routine such as this, which samples them without changing them

FLFOR, called by the main routine at location 35034, is also shown at 35064 to 35116. Other subroutines called are not shown.

A peculiarity of the Intel instruction format is evident: 2-byte addresses of instructions are listed with the high-order byte first, so that they read from left to right conventionally, but addresses appearing as operands are listed with the low-order byte first. This is a consequence of the slow memory speeds that were available during the early design stages of the 8008. The low-order byte begins the selection process early via decoders on several chips, perhaps on several cards, while the high-order byte completes the process quickly by bringing up a single chip select line. With faster microprocessors and faster memories this reason is no longer valid, but the practice is retained for the sake of compatibility.

Conclusion

Control flags are indispensable to the microcomputer programmer and the process control engineer. Flag bits, set by arithmetic and logical operations in the central processor, are exceptionally valuable for controlling conditional branching in microcomputer software, and allow the decoding of the process state, alarm conditions, and normal operating alternatives for the execution of effective control responses.

Although flags are an essential part of many microprocessors' instruction sets, they may not be stored in a separate register. Consequently, the process control engineer must develop software, or an operating system, capable of displaying the flags without altering their values, to use them in conditionally branched programs or in program debugging. Once the consequences of arithmetic and logic instructions are learned for a given microcomputer, they become a powerful programming aid in microcomputer-based process control applications.

Acknowledgment

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TECH NOTE

Group-Coded Recording Reliably Doubles Diskette Capacity

Pawitter S. Sidhu

Wangco, Incorporated
Orbis Division
Tustin, California

To squeeze more data onto a standard diskette requires sophisticated encoding in order to avoid exceeding the physically attainable limits of standard codes; GCR is the answer

Ed Note: This is the third of three Tech Notes on the general subject of double-density recording; previous Notes appeared in the September and October issues of *Computer Design*. The Notes, considered together, provide three different solutions to the problem of increasing the capacity and data rate of a flexible disc, and illustrate the tradeoffs that should be considered in choosing one approach over another.—WBR

Diskette drive systems capable of storing more data and transferring them at higher data rates are in increasing demand, and call for improved recording techniques. Higher density recording automatically achieves both increased capacity and increased data rate in a given diskette drive. However, it requires a different magnetic encoding method, because the standard code is already near its density limit. The selected code must both *cope with* and *compensate for* mechanical and recording media imperfections. Group-code recording (GCR) improves the data packing density nearly as far as possible, while offering maximum timing margins, self-clocking, and permitting a unique synchronization pattern of all 1s.

Frequency modulation (FM) is the standard code for diskettes. This technique is a continuance of the recording method for hard discs principally used by IBM. Modified frequency modulation (MFM) or Miller code is one method that has been used for doubling the density. However, MFM results in lower data reliability. After a fresh look at high efficiency codes, particularly nonreturn-to-zero (NRZ), our company selected GCR, a modified NRZ, as the code to double the recording density of floppy discs used on a standard disc drive, instead of modifying an inefficient FM code. The technique is equally applicable to other magnetic recording media where high data density and *reliability* are mandatory.

In a standard FM code, each bit cell boundary is marked by a flux reversal, called a clock. An extra flux reversal for a 1 bit is placed in the middle of the bit cell [Fig. 1(a)]. A 0 bit is indicated by the absence of this extra flux reversal. Since at least one-half of the flux reversals are exclusively for synchronizing or clocking, FM code is limited to a maximum of 50% efficiency. A further disadvantage is the apparent tendency for flux reversals at high density (in any code) to

shift away from one another. Because the minimum nominal time between flux reversals in FM is half the duration of one bit cell, maximum shift allowed for reliable data decoding is ±0.25 bit. More simply, FM encoding has a theoretical maximum margin of ±0.25 bit time.

However, hardware implementation of FM code is simple because, for a clock frequency of f, the code limits the system's bandwidth which lies between f and 2f. If the clock frequency is doubled, the bit cell length is halved, and the allowable shift drops to ±0.125 of the single-density bit cell length, taken as a reference. This is unacceptably small —only 19 microinches or half a microsecond on the innermost track, which already carries 6536 flux reversals per inch (frpi) on a standard FM-coded diskette operating at 250K bits/s.

The FM code may be modified to delete the clock bit transitions. In this technique, successive 1s are represented by flux reversals one bit cell apart; 10 and 01 combinations are represented by flux reversals 1.5 bit cells apart; while two or more 0s are represented by flux reversals at intervals of two bit cells [Fig. 1(b)]. Three frequencies are recorded, but reversals can occur either at the center or at the boundary of the bit cell, or at one-half bit-cell intervals. Thus the shift margin is ±0.25 bit time (the same as in FM code). Because the highest frequency is only f, not 2f as in FM, data density of MFM may be doubled or bit times reduced by half without exceeding the bandwidth of an FM system; the data rate can also be doubled. However, reducing the bit cell by half also reduces the shift margin from ±0.25 to ±0.125 bit time, as with FM. This leaves practically no margin for reliability.

In NRZ a 1 is represented by a change in flux level and a 0 is represented by the absence of such a change [Fig. 1(c)]. Successive flux reversals are one bit cell apart, and the theoretical phase margin is ±0.5 bit. Because only one flux transition is required for one bit, the code is highly efficient. However, a long string of recorded 0s produces no read signal, which could result in loss of data synchronization, and requires a system bandwidth from dc to the data rate f. This larger bandwidth reduces the signal to noise ratio.

Achieving Reliability

In GCR, as in NRZ, a 1 is represented by a flux reversal and a 0 by the absence of a flux reversal [Fig. 1(d)]. However, no more than two 0s are recorded in succession, assuring that synchronization, once achieved, will not be lost, and limiting the bandwidth of the system to between 0.33f and f. This bandwidth is much narrower than that of NRZ or FM, and the shift margin is ±0.5 bit. As a result, data density is doubled or bit time halved, relative to FM, for the same bandwidth. Furthermore, reducing bit cell length by one-half reduces the shift margin from ±0.5 to ±0.25 bit time—twice that of FM or MFM codes.

Group encoding avoids recording more than two 0s in succession by translating four bits into five. Four bits can occur in any of 16 combinations from 0000 to 1111. Of the 32 combinations of five bits, those that begin or end with more than one 0 and those that have more than two 0s internally are not used. After eliminating these, only 17 combinations are left; and of these, the combination 11111 is reserved for synchronization. The remaining 16 combinations of five bits are correlated with the 16 possible combinations of four bits (Table 1). When recording, each group of four bits in a sequence of data is translated into a corresponding group of five and recorded in conventional NRZ form. Then, when reading, the reciprocal five to four translation yields the original four bits of data. This

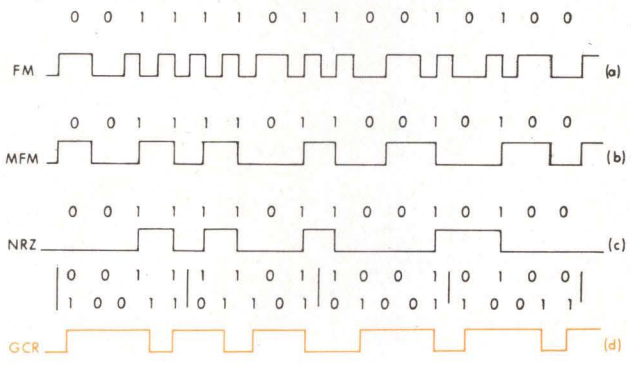

Fig. 1 Various recording codes. Standard code for diskettes is FM (a). Various modifications of FM, such as (b), are in use to increase density, but best approach is a version of NRZ (c) called GCR (d), that eliminates long strings of 0s. All four codes have the same data pattern, but GCR requires a translation of four bits to five as shown.

TABLE 1

Translation Four To Five In GCR Code

4-Bit Data	5-Bit Recorded Data
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

TABLE 2

Comparison of Recording Codes

Code	Data Rate (kbits/s)	Recorded Bit Density (frpi)	Phase Margins	
			Bit Time	μs
FM	250	6536	±0.25	±1.0
MFM	500	6536	±0.125	±0.5
GCR	500	8170	±0.20	±0.8

translation from four bits to five further increases bit density by 25% from 6536 to 8170 frpi, and reduces the bit cell time to 1.6 μs, or 0.4 that of FM—a 20% reduction from the 2.0 μs of the uncoded data. Accordingly, the phase margin is ±0.20 instead of ±0.25.

The distinctions between FM, MFM, and GCR, summarized in Table 2, clearly show the advantages of GCR over MFM in terms of phase margin and data reliability.

Advantages of GCR

In a standard IBM-compatible diskette drive using standard media, data density is doubled simply by using GCR instead of FM. Doubled density automatically increases the data rate to 500K bits/s, while increasing the maximum flux transition density to 8170 frpi. These are increases of 100% and 25% respectively. Any well-designed read/write channel, and most available ferrite heads, can easily handle this 25% increase in flux transition density. In addition, GCR increases data reliability over FM or MFM because its shift margins are 60% larger. Increased phase margins also assure diskette interchangeability when written and read on different drives.

GCR is not without its disadvantages. Chief among these is the extra logic circuitry it requires for group formation and 4-to-5-bit translation. This logic, however, can be assembled inexpensively from standard MSI chips and conceivably could be implemented in software or on a single custom chip.

GCR System

The GCR code is implemented in the Orbis model 86 data encoder on a single printed circuit (PC) board. The data encoder can operate at either the standard rate of 250K bits/s, using FM, or double that rate with GCR. Either way, it accepts data in FM code from an external controller furnished by the user, which translates data from parallel ASCII or whatever code the host computer uses. The controller also distinguishes one record from another by incorporating an address in the recorded data, by keeping track of the angular position of the rotating disc, or by other means.

In standard 250K-bit/s mode, the encoder is logically bypassed, and the data pass directly to and from the controller in FM code. However, in double-capacity mode, the data encoder is a 2-way synchronous translator, communicating with the controller in FM code at 500K bits/s but storing data in GCR at 625K bits/s. Storage density on the innermost track at double capacity is 8170 frpi, corresponding to 6536 bits/in.—compared to 6536 frpi and 3268 bits/in. at single capacity.

Hardware to implement the GCR code has two major sections: a phase-locked oscillator (PLO) to control passage of data through the system, and a 4-to-5-bit data encoder/decoder. The PLO uses two standard integrated circuits (ICs). During either read or write operation, data applied to the PLO inputs bring the output frequency in phase with them. Two counters divide the main oscillator frequency of 5 MHz by 10 and by 8, yielding 500 and 625 kHz respectively (Fig. 2). When data are being read, the PLO follows minor variations in data rate corresponding to diskette speed variations, but averages the rapid variations caused by shifting flux reversals.

All data moving in either direction through the GCR system pass through two 4-bit registers, A and B, and one 5-bit register. The 4-to-5-bit encoder lies between register A and the 5-bit register in the data stream, and the 5-to-4-bit decoder is between the 5-bit register and register B (Fig. 3). Write data, previously coded into FM, are entered serially into register B, then A, at 500 kHz (one bit

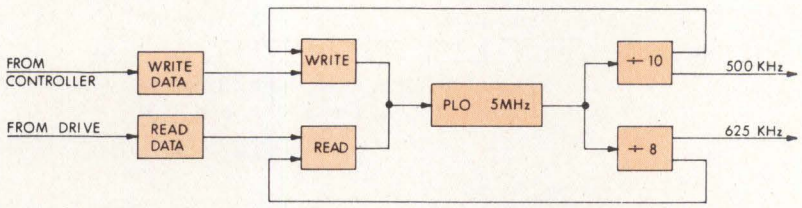

Fig. 2 Phase-locked oscillator. Data passing in either direction synchronize the circuit; two output frequencies control shift registers containing raw or encoded data

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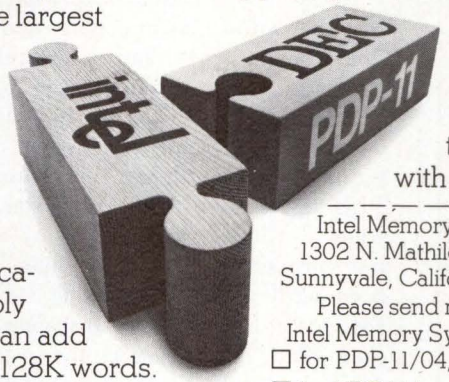

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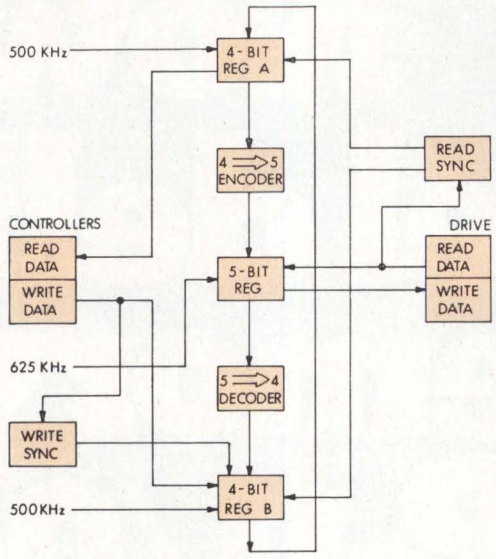


Fig. 3 Data path. Two 4-bit and one 5-bit registers process all data passing to and from the disc, encoding and decoding the GCR format

every 2 μs), translated into the 5-bit code, and strobed by the write sync logic into the 5-bit register at 8-μs intervals. These five bits are serially transferred to the diskette at 625 kHz in NRZ code. During read operation the data pulses, in NRZ code, enter the 5-bit register serially and are decoded to four bits, which are strobed by the read sync logic into register B. From here, again the data pass to register A and then to the host system at 500 kHz.

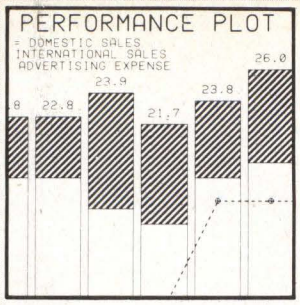
Every record begins with a string of 1s, forming a preamble and a synchronizing byte, and is generated by sending the output of the 625-kHz clock directly to the recording head. The preamble signals the beginning of a record, and synchronizes PLO into step with the data stream when reading. Data, however, are not encoded until the sync byte has been written. When encoding starts, the write logic begins transferring four data bits through the 4-to-5 encoder every 8 μs as described previously. Another sync byte is written at the end of the record, which can be of fixed or variable length as required by the controller and host computer.

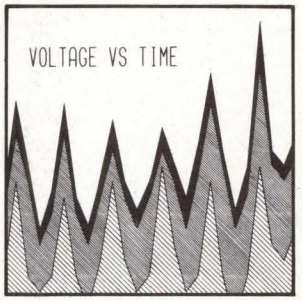
When reading, the logic looks for the unique all 1s pattern, which never occurs in data; having found such a pattern, it then goes into preamble mode until the sync byte is recognized. At that point, decoding begins, and continues until the terminating sync byte is found. The preamble and sync byte, by the way, not only bring the PLO into phase, but also can identify the density of the recorded data—meaning that single- and double-density records can be intermixed on one diskette.

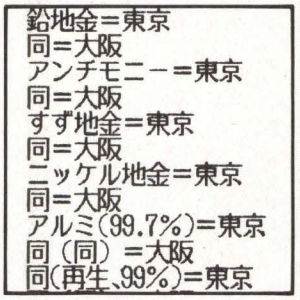
Physically, the encoder/decoder consists of 35 small-scale ICs on a PC board. If some of its functions are incorporated into the user's controller, such as read and write sync logic, translation of host computer logic levels to those of the diskette and vice versa, or using the controller's 625-kHz clock, then the GCR logic can be *reduced* to as little as seven chips unlike decoder for MFM or M²FM (modified, modified frequency modulation).

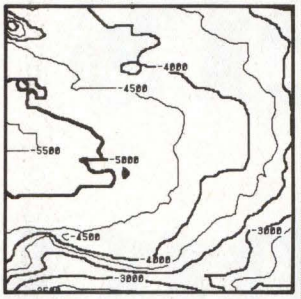
Summary

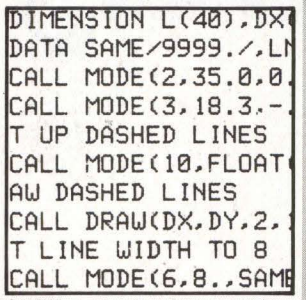
Orbis has chosen the GCR technique for *reliably* doubling the recording density on its flexible discs because of its advantages of larger phase margins, distinctive preamble patterns, and the absence of requirements for write pre-emphasis or distorted timing. Its principal disadvantage, compared to MFM, is the extra hardware that it requires. □

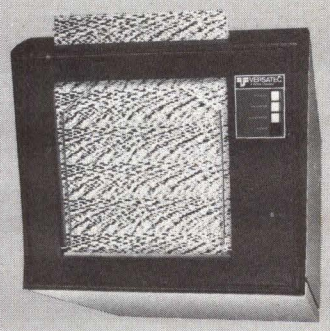












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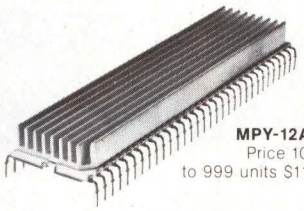

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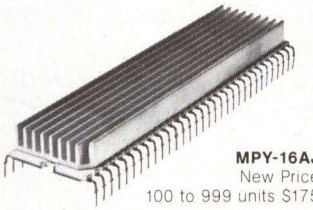

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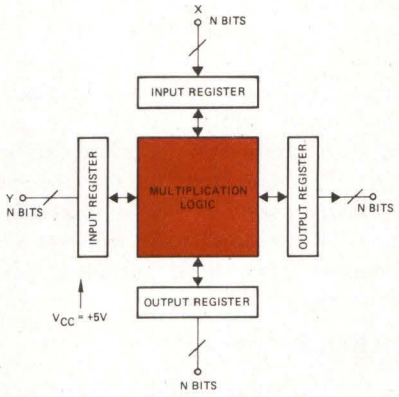

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CIRCLE 39 ON INQUIRY CARD

TECH NOTE

Testing Microcomputer Boards Automatically

Eugene B. Foley, Jr and Anthony H. Firman

Teradyne, Incorporated
Boston, Massachusetts

Although microcomputer boards are very complex, and the expensive microprocessors used on them are highly susceptible to accidental electrical damage, the boards can be tested thoroughly and safely on an automatic system

In spite of the complexity of 1-board microcomputers, manufacturers can still take advantage of the economics of automatic board-test systems in testing them. However, certain special techniques and precautions are necessary to simplify the preparation of test patterns, and to preclude the possibility of damage to the microprocessor.

Board testing is intended to detect and diagnose manufacturing defects, not to detect design errors, or to replace thorough incoming inspection of components. It can hardly obviate systems testing. What board testing can do is find manufacturing defects such as missing, incorrect, and wrongly inserted components; solder-bridges between lands; and open circuits. A reasonably thorough job of board testing does all these things economically.

While an automatic board-test system can do more than can be done by a human, it rapidly becomes much less economical; such a system is best at routine, repetitive jobs, which it does more efficiently and economically than a human technician. A human technician, on the other hand, can perform complex, nonrepetitive jobs more efficiently and economically than the machine. Good management demands that machines and people be used appropriately.

In finding manufacturing faults, a board-test system need not simulate the normal operating environment of the board under test. When a variety of boards is to be tested, such simulation can become prohibitively expensive—and may not significantly improve fault-coverage. On the other hand, good fault-coverage can be achieved by testing the various individual operations of the board. This can be done even to a microcomputer board with its microprocessor removed (Fig. 1).

Of course, a board-test system must not damage sensitive components, but it should ensure also that these components will not be damaged by a faulty board. For example, a microcomputer board can be tested without the microprocessor installed in such a way as to certify that the microprocessor will not be damaged when it is installed subsequently.

Testing Strategy

In testing microcomputer boards, a socket for the microprocessor is essential, as opposed to soldering the device in place. The microprocessor is tested at incoming inspection (with due consideration of the appropriate balance between the cost of exhaustive testing and the risk of passing bad devices), but is not plugged into the microcomputer board until the latter has been tested just as any digital board is. Board tests comprise a variety of logical steps to detect operating errors caused by manufacturing faults. In addition, parametric tests are made at the microprocessor connector (to ensure

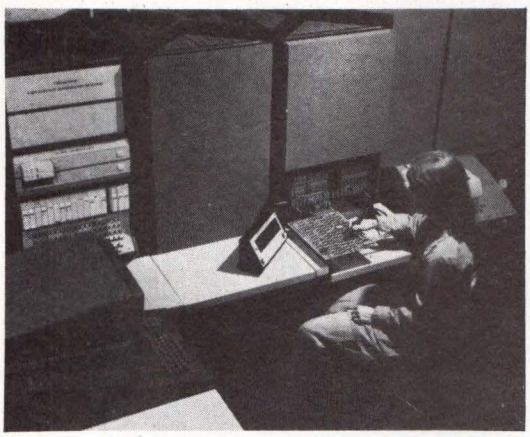

Fig. 1 Board tester. An L125 circuit diagnostic system is used for testing microcomputer boards

that the microprocessor will not be damaged when it is added) and at the edge-connector (to ensure that the board will operate in the assembled system).

Faulty boards are repaired, and recycled to the board-test facility. Good boards are equipped with pretested microprocessors, and subsequently retested using a different set of logical steps. Complete boards are tested as functional computers. The test system effectively functions as the memory for the microcomputer board, and at the same time monitors the board's operation. At this point, tests need not be exhaustive, since the bulk of the board has already been tested; besides, microprocessor failures after incoming inspection tend to be catastrophic, and therefore readily detected.

Making Testing Easier

The engineer who designs any kind of printed circuit board can make the board easier to test in various ways—not only by an automatic board-test system, but also manually. These methods have been explained elsewhere.[1] When the board is specifically a microcomputer board, some particular methods are useful.

For example, *make the microprocessor removable.* Use a socket for this device, and possibly for other devices that are very sensitive to accidental electrical damage. The microprocessor can be plugged in after the board has been found acceptable. This simple and inexpensive technique not only makes testing the board easier, but also assures that the microprocessor will not be damaged if the board is faulty. It avoids the risk of damaging the microprocessor with solder or soldering heat, and enables removal of a microprocessor that proves to be faulty—a difficult task with a 40-pin package that has been soldered into place.

Give the test system access to the microprocessor connector through a mating connector on a cable from the interface board in the test system. With this connection the system can check the drive and load levels that will subsequently be applied to the microprocessor. If incorrect, these levels could destroy this expensive device.

Include a means of disabling the on-board clock, and of using the test-system clock instead. While the overall test procedure must include checking board operation under control of its own clock, much basic testing can be carried out more conveniently using the test system's own timing.

Provide a way to initialize all sequential circuitry to suitable states from the edge-connector. Often this involves nothing more than a suitable reset line.

Make the computer capable of single-cycle operation, in which it executes exactly one instruction, then stops and waits for a new start signal. Single-cycling allows the test system to request individual, complete instructions at its own clock-controlled speed.

Avoid tying an unused input pin to ground or to a supply line; *always use a pull-up or pull-down resistor.* This precaution allows a signal to be placed on an otherwise unused input, to check some aspect of circuit operation or the voltage level to be measured, and to check for internal shorts.

Testing Procedure

To test a microcomputer board without a microprocessor, the board is plugged into the test system, and a cable from the interface board is

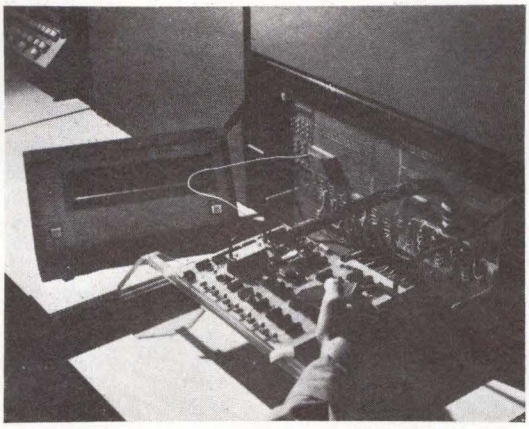

Fig. 2 Initial testing. A microcomputer board is plugged into a board-test system, but the microprocessor is not installed. Test system has access to points within the unit under test via cables from the interface board, and exercises the unit under test without influencing or being influenced by the microprocessor

plugged into the microprocessor connector; the microprocessor is not yet plugged in. Depending on the board design, other jumpers from the interface board may also be connected to points within the board—to disable the clock, for example (Fig. 2).

The board-test system is programmed to perform three kinds of tests: logic tests on the board, parametric tests on the microprocessor connector, and parametric tests on the edge-connector. To perform thorough logical tests on the combinatorial and sequential logic of the board, a connection to the microprocessor socket partitions the board into smaller logic arrays. Partitioning makes test pattern generation easier and fault diagnoses quicker and more accurate.

With parametric tests on the microprocessor connector, inputs to the microprocessor must not be overdriven, and outputs from the microprocessor must not be overloaded. Verifying these levels at this time will ensure that the microprocessor is not damaged when it is plugged in subsequently.

Finally, parametric tests on the edge-connector ensure that the board will function properly when it is finally installed in a system.

In all of these tests, timing is controlled by the test system; the clock on the board under test is disabled. The fourth test category is on the clock itself. Frequency of clock signals must be correct, and phase-relationships between the several clock signals must also be correct.

A board that passes all of this testing should have earned confidence in its integrity. However, it must then have its microprocessor plugged in, and undergo final functional testing. This board is now a complete, functional computer; commonly it includes read/write (R/W) or read-only memory (ROM), or both. It should therefore be tested as a computer, not merely as a board (Fig. 3).

At this point the ability of the board to function in the single-cycle mode becomes important. In this mode the test system can provide the board with a suitable instruction, and can verify that the instruction is executed properly. With single-cycle mode, the test system can provide instructions at one operating speed, while the board executes these instructions at another speed.

A few simple initial instructions can check basic computer operations: operation of the accumulator circuitry, of the bidirectional data bus, and of the address bus. Checking these operations inherently checks various other operations of the computer: movement of data around the computer, functioning of the program counter, and so on. Successful completion of these tests indicates that the computer is essentially functional.

The next step is to check the more specialized operations of the computer: interrupt, hold, and direct memory access, for example. Finally, operation of the onboard memories should be checked. One very effective method of checking a R/W memory is to load a simple program into it, then let the microcomputer execute it; the test system verifies that the microcomputer obtains the correct result. Not only does this program thoroughly exercise the microcomputer board, but it also saves testing time, since the microcomputer usually operates more rapidly than the test system.

The ROM may be checked similarly, if it is socket-mounted, by replacing it with a unit storing a test program; the microcomputer executes the program. (Some manufacturers install a ROM containing a standard set of test routines, which are used at board-test, during system test in the factory, and subsequently for field testing.)

These tests may not be exhaustive, but they can provide considerable exercise for the microcomputer board, and can reveal a great majority of faults. Bear in mind that the basic board without the microprocessor has been thoroughly tested logically, and that if devices as complex as the microprocessor fail during assembly, after incoming inspection, they usually fail catastrophically. Thus a microcomputer that has passed all these tests, with and without the microprocessor, has earned considerable confidence in its ability to perform perfectly.

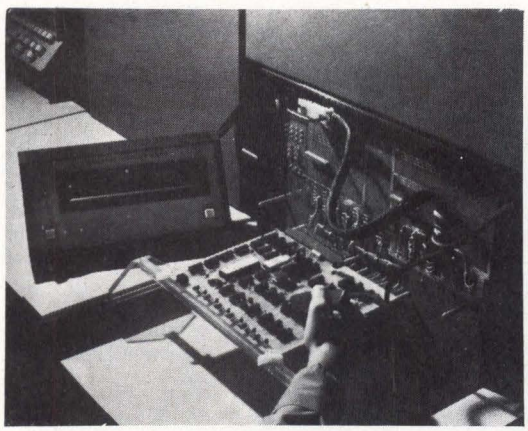

Fig. 3 Functional testing. When the board has been checked out, all components are put in place, and the test system exercises the board as a functional computer. This particular board, part of a control system, includes an 8080 8-bit microprocessor, 1024-bit RAM, and 8192-bit ROM

Conclusions

In spite of their considerable complexity, microcomputer boards can be tested effectively. Automatic board testing offers significant economies, not only in its own right, but also by imposing constraints that save money in other ways. Testing can even preclude the possibility of subsequent damage to a sensitive and expensive component by checking the drive and load levels ahead of time.

Reference

1. "Circuit Designers Can Make Digital Boards Easier to Test," Teradyne, Inc, Boston, Mass

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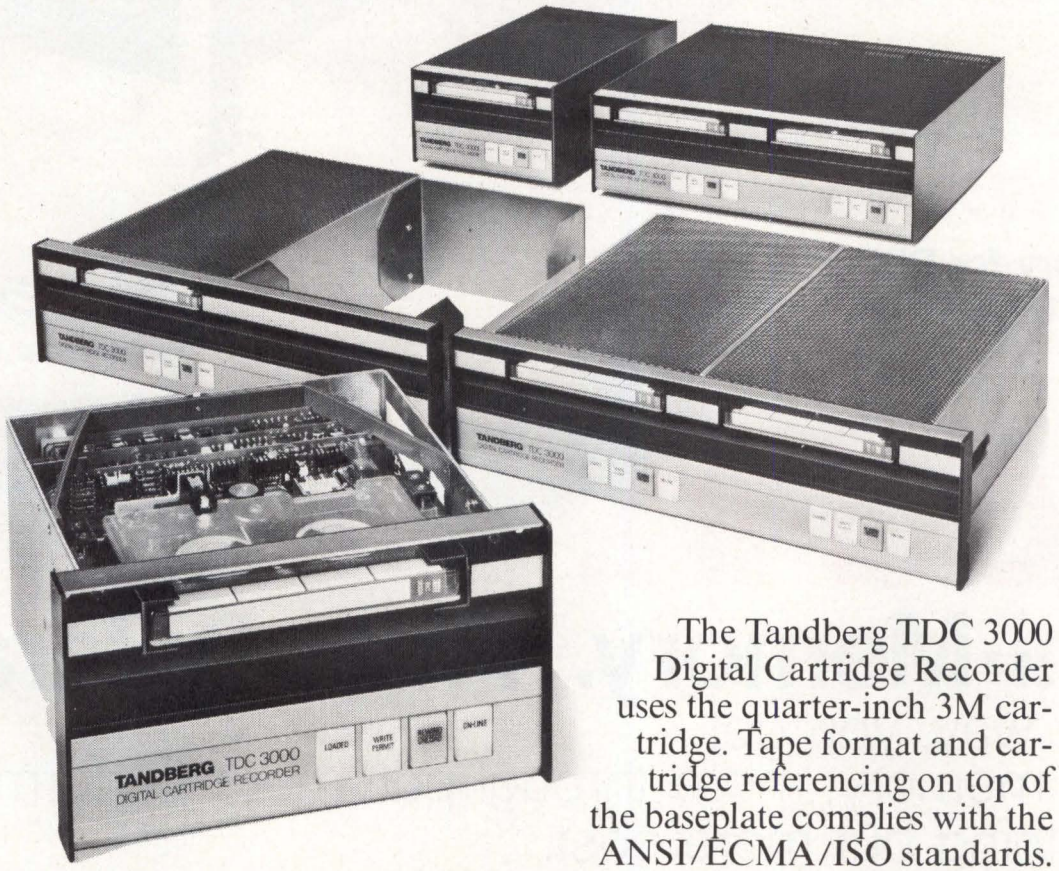

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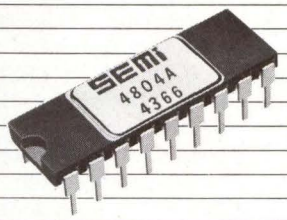

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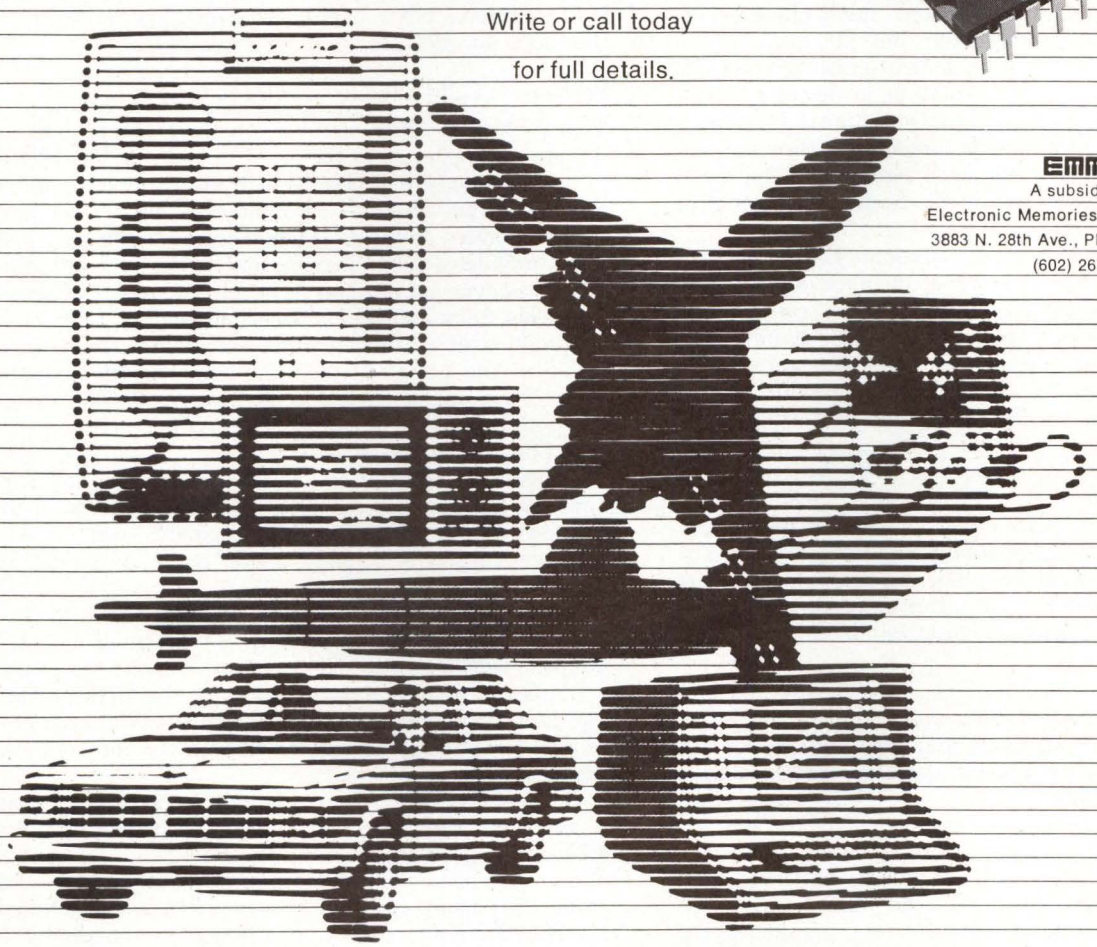

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LSI Data Communication Device Technology Available for Commercial and Industrial Applications

Information on seven large-scale integrated circuits developed for use in the INTELSAT satellite communications network is now being made available on a royalty-free, nonexclusive basis. The only charges will be for defrayal of INTELSAT's expenses for assembly and delivery of three data packages which cover the seven devices.

As part of the program for its satellite communications network, the International Telecommunication Satellite (INTELSAT) Organization sponsored the development of a group of large-scale integrated (LSI) circuits. These circuits perform many functions of the single-channel-per-carrier, pulse-code modulation, multiple access demand-assignment equipment (SPADE) and single-channel-per-carrier (SCPC) channel equipment but potentially have further applications. Devices include a pulse-code modulation (PCM) logic encoder, PCM logic decoder, transmit synchronizer, receive synchronizer, digital bit timing recovery (DBTR) circuit, rate ¾ convolution encoder, and rate ¾ threshold decoder. All seven circuits will be made available on a commercial basis from the respective INTELSAT contractors.

For existing SPADE or SCPC installations, LSI technology allows expansion of the number of channel units accessing the existing common equipment at a considerable reduction in size, power, and maintenance requirements compared to present technology. For this application, the LSI channel unit is completely compatible at the intermediate frequency (IF) subsystem and voice band interfaces with existing channel units.

Channel unit LSI devices, when used with available microprocessors and other "off-the-shelf" commercially available LSI devices, permit development of an entirely different concept for implementing a SPADE terminal. The chips could also be used for other applications requiring such functions as clock recovery, forward error correction, ambiguity resolution, and synchronization.

Channel Unit

A SPADE channel unit handles voice signals, while an SCPC unit processes both voice and data signals. Speech activity is monitored by a voice detector, which is used to gate the channel carrier on when speech is present, thus conserving satellite power as a function of talker activity. Voice detector and PCM encoder outputs are processed in the transmit synchronizer, where timing, buffering, and framing functions are performed. The phase shift keyed (PSK) modem (modulator/demodulator) modulates the assigned carrier with the outgoing bit stream and coherently demodulates the return channel.

Clock information is extracted from the demodulated output by a DBTR circuit. A receive synchronizer establishes frame synchronization, rebuffers the PCM data, and sends those data to the PCM decoder. Appropriate transmit and receive carriers are supplied by a frequency synthesizer.

An SCPC LSI channel unit employs convolutional coding and threshold decoding for forward error correction when transmitting digital data. Since the PCM encoder and decoder chips contain the necessary logic, a complete PCM encoder/decoder primarily requires only the addition of analog components. The transmit synchronizer function is obtained with a single LSI chip and one standard random-access memory (RAM), while the receive synchronizer is composed of one LSI chip and two shift registers. DBTR circuit, convolutional encoder, and threshold decoder are each on single chips.

Package 1: PCM Encoder and Decoder

Two p-channel MOS circuits contain PCM encoder and decoder logic. Input to the PCM encoder is band limited to approximately 3.4 kHz by a transmit filter to prevent aliasing in the subsequent sample-and-hold (S/H) circuit which operates at 8 kHz. Digital logic on the chip essentially provides a successive-approximation analog-to-digital (A-D) conversion. In this type of A-D conversion, progressively finer increments are combined to form an approximation of an analog input signal. An 11-bit quantization of the sampled voice band input is then digitally compressed in the encoder chip to a 7-bit PCM output. The serial PCM bit stream is clocked out of the encoder at a 56K-bit/s rate.

Transfer function of the PCM encoder is a segmented approximation of an A-law compander with A-87.6. Thirteen different straight-line segments are employed (16 segments are actually used, but the middle four are of equal slope).

The PCM decoder performs the inverse 7- to 11-bit code transformation followed by D-A conversion. A resampler, with a narrow pulse output, corrects the $(\sin x)/x$ frequency distortion introduced by the S/H nature of the D-A converter output. Amplitude-modulated pulses from the resampler are filtered to recover the continuous analog waveform.

Only 25% of the space required by previous versions is used by the complete PCM encoder, which occupies a 4.25 x 9" PC board. Since much of this encoder is analog in nature, considerable size and cost reductions have been attained by using commercially available advanced analog integrated circuits (ICs), in addition to the digital LSI chips. For example, the transmit and receive filter functions are implemented with hybrid active filters.

An IC D-A converter and a monolithic S/H circuit also contribute to the improved design. A novel feature of the encoder is the use of two self-contained light

emitting diodes to obtain easy calibration of encoder zero and gain.

Normally the PCM encoder and decoder obtain timing and clock signals from the transmit synchronizer and receive synchronizer, respectively.

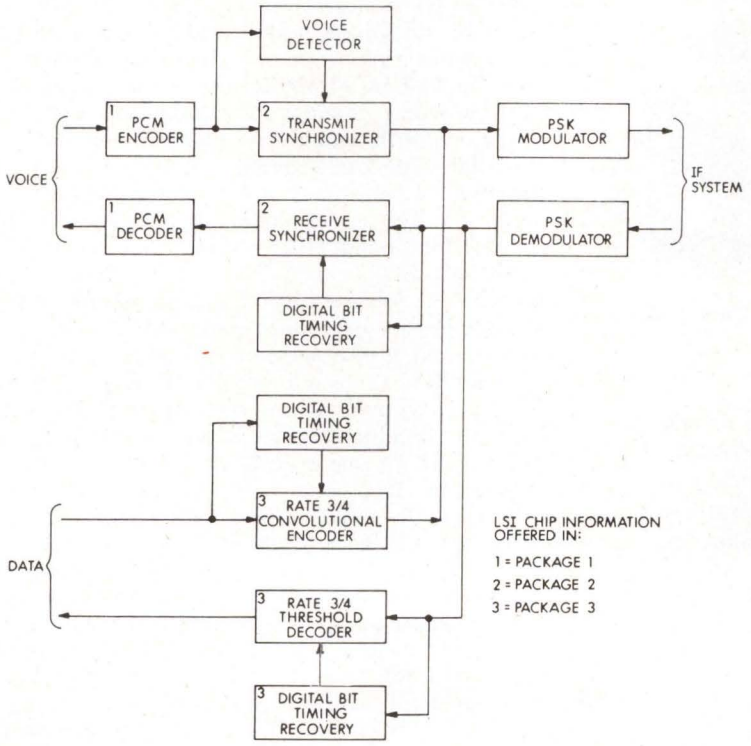
Package 2: Transmit and Receive Synchronizers

Several functions are performed by the transmit synchronizer: generation of appropriate timing and clock signals for the PCM encoder, voice detector, and PSK modulator; initiation of a preamble containing a carrier recovery sequence and a bit timing recovery sequence; and combining a unique bit sequence called start of message (SOM) with the PCM encoded voice data every 32 PCM words. Basically, it consists of timing generator, first-in/first-out (FIFO) memory, and output formatter. The timing generator accepts a 448-kHz master clock and generates a 56-kHz PCM bit clock, an 8-Hz PCM word clock, and a 32-kHz modem clock. It also produces a synchronized carrier-on signal to the modem in response to an asynchronous voice present input.

The CMOS transmit synchronizer chip contains control logic needed to utilize a standard external RAM as a FIFO memory. Data at a 56K-bit/s rate from the encoder are written into the RAM and held for subsequent readout at a 64K-bit/s rate.

When the synchronized carrier-on signal becomes true, the output formatter produces a carrier recovery pattern of 20 bits of "ones" followed by a bit timing recovery sequence of 40 alternating "zeros" and "ones" on each of the 32K-bit/s parallel output channels to the modem. A different 16-bit unique word, or start of message (SOM) character, is then transmitted in each channel. PCM data in the form of 32 words (224 bits) are read out of the RAM at a 64K-bit/s rate and alternate bits are fed to each modem channel at a 32-kHz rate. The sequence of an SOM character followed by 112 PCM data bits in each channel is repeated as long as the "voice present" input is true.

The receive synchronizer performs the following functions: recovery of frame synchronization from SOM detections, generation of appropriate PCM decoder clocks,



Block diagram of SPADE/SCPC LSI channel unit. Three information packages on seven designated circuits are being offered by COMSAT on a royalty-free, nonexclusive basis. The only fees involved cover assembly and delivery of data

resolution of the ambiguity created in a 4-phase coherent PSK demodulator, and extraction of the PCM data.

When an SOM is satisfactorily detected for the first time in each of the two input channels, the CMOS receive synchronizer chip changes from open to closed aperture mode. When two or more such detections are made consecutively, a second closed aperture state is reached in which the circuit coasts through up to five consecutive SOM misses without losing synchronization.

A 448-kHz master clock input generates the 56-kHz bit clock and 8-kHz word clock required by the PCM decoder. These clocks are synchronized to an incoming 32-kHz clock from a demodulator.

The carrier recovery process in a 4-phase PSK demodulator results in an ambiguous condition in which either or both of two input data channels from the modem may be inverted (ie, complemented) and the two channels may also be interchanged (for a total of eight possible combinations). The ambiguity is resolved by noting whether an SOM or its complement is detected and whether it is found in the proper channel.

Ambiguity-corrected PCM data are extracted from the composite bit stream and written into one of two external shift registers at a 64K-bit/s rate. Simultaneously, data are clocked out of the other register at a 56K-bit/s rate and sent to the PCM decoder.

Proper system operation is maintained when the local 448-kHz oscillator used by a receive synchronizer and the oscillator used by the corresponding transmit synchronizer are each offset by up to $\pm 10^{-4}$ from nominal.

Package 3: DBTR Circuit and Rate ¾ Convolutional Encoder and Threshold Decoder

A single p-channel MOS chip contains the DBTR circuit, an all-digital phase-locked loop designed to recover a synchronous clock from a random binary data signal at rates up to 64K bits/s. It incorporates acquisition mode circuitry which provides for rapid phase lock upon initial acquisition with a randomly phased input data sequence.

A differentiator generates a narrow pulse for each transition of the binary input data signal. Then a phase detector compares the differentiator output with the recovered bit timing (RBT) signal and generates either a count-up (CUP) or count-down (CDN) signal. CUP and CDN pulses are totaled in a phase error accumulator. When a phase correction request occurs, an advance signal is generated if the accumulated phase error is positive, while a retard command is issued if the accumulated phase error is negative. The reference clock divider, which nominally divides a master input clock by 30, will divide by 29 or 31 for one cycle if the advance or retard signal, respectively, is present.

When the acquisition input to the integration and mode control section goes high, a phase error accumulator is bypassed and phase correction requests are made for every differentiator output pulse. This state lasts for eight differentiator pulses, at which time the accumulator is switched in and phase corrections are requested every fourth cycle of the RBT waveform. This second state is maintained for 32 RBT cycles, at which time a third or steady state is entered. In this steady-state mode, phase correction requests occur every 64 RBT cycles.

A master clock (30 R), which is nominally 30 times the bit rate of the input data stream, is required. The output is a recovered clock which is phase locked to

the data rate (R). Also, output clocks are produced at frequencies ⅓ R, ½ R, ⅔ R, ¾ R, and 2 R. Included in these outputs are the clocks needed for either the SCPC rate ¾ convolutional encoder or the rate ¾ threshold decoder.

The rate ¾ convolutional encoder, contained on a single p-channel MOS IC, is used as a forward-error-correction encoder in SCPC applications. It accepts serial input data and performs a serial-to-parallel conversion. Three parallel information sequences are shifted through three registers, with each register tapped at four points according to the encoding algorithm. This convolutional code has a constraint length of 80 and a minimum distance of 5. Contents of the tapped stages are added modulo-2 to form a parity sequence which is combined with the three information sequences to generate two parallel output data streams. For incoming data at 48K or 50K bits/s, the output channels to the modulator are clocked at 32K or 33.33K bits/s, respectively.

The rate ¾ threshold decoder, also on a single p-channel MOS IC, is used in conjunction with the convolutional encoder for forward error correction in SCPC applications. It normally obtains necessary clock signals from a DBTR circuit. An ambiguity resolution matrix in the decoder removes the ambiguity introduced by 4-phase PSK demodulation. The matrix is controlled by a state counter which is driven to the proper state to correctly resolve the ambiguity.

A decommutator delivers three information sequences to three shift registers which are tapped to produce an estimate of the parity sequence generated by the encoder. Estimated parity bits are compared to receive parity bits and the results are stored in the syndrome register.

Contents of selected syndrome register stages are used to create correction signals. The correction bit is set to a binary "one" if more than two of the four tapped syndrome register stages contain a "one." When a correction signal is a "one," it indicates an error in the corresponding data register output bit and the data bit is complemented. Corrected data sequences are multiplexed and serially clocked out of the decoder at the original rate at which uncoded data entered the encoder. With a channel error probability of 10^{-4}, the decoded output bit error rate is less than 1×10^{-7}.

Whenever correction signals occur at a rate exceeding a predetermined value, the state counter advances to its next state. This causes the ambiguity resolution matrix to proceed through all possible combinations until ambiguity is properly resolved and a satisfactory correction rate is achieved.

Availability

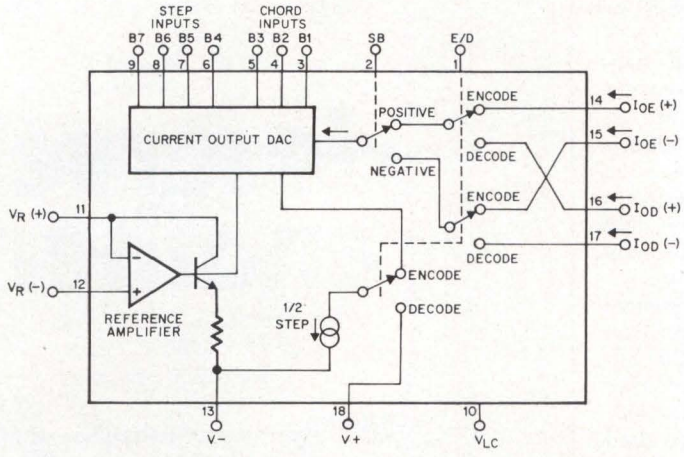
Fees charged for assembly and delivery of data are $1000 for the PCM encoder/decoder package, $600 for the transmit and receive synchronizers package, and $600 for the package containing information on the DBTR circuit, rate ¾ convolution encoder, and rate ¾ threshold decoder. Further information on obtaining any or all of the packages is available from John H. Heck at COMSAT, 950 L'Enfant Plaza SW, Washington, DC 20024, tel: (202)554-6705.

Engineering models will be made available in the very near future at the COMSAT Laboratories, 22300 Comsat Dr, Clarksburg, MD 20734, tel: (301)428-4574. Under suitable arrangements, the devices could be used for testing purposes. For information relative to the circuit technology contact John Snyder at the above address.

CIRCLE 43 ON INQUIRY CARD ⟶

Companding DAC Allows Signal Expansion (D-A) and Compression (A-D)

An exponential transfer function that conforms to the Bell System μ-255 logarithmic companding law for pulse code modulated transmission permits both signal expansion (D-A conversion) and signal compression (A-D conversion) with the monolithic Comdac™ DAC-76. A sign plus 12-bit DAC dynamic range is provided in a sign plus 7-bit format. The companding (compression/expansion) transfer function is implemented by using three bits to select one of eight binary-related segments (chords) and four bits to select one of 16 linearly-related steps within each segment.

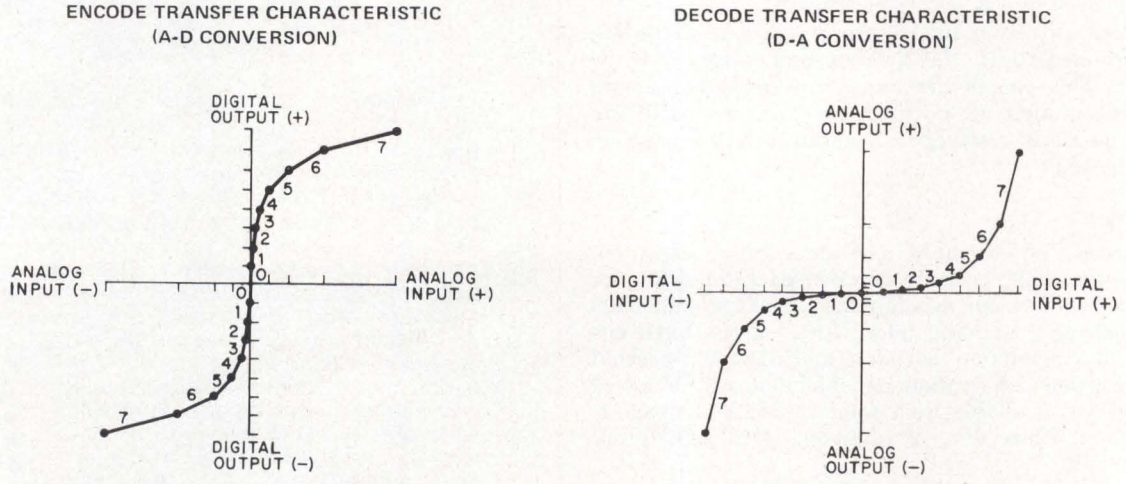


Equivalent circuit of Precision Monolithics companding DAC

In addition to telecommunications, the companding principle has a wide area of application in data acquisition, servo controls, stress and vibration analysis, digital recording, and speech synthesis. The 8-bit format with a sign plus 72-dB dynamic range is particularly apt for control systems using 8-bit microprocessors, RAMs, and ROMs. Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050 claims this to be the first monolithic companding DAC.

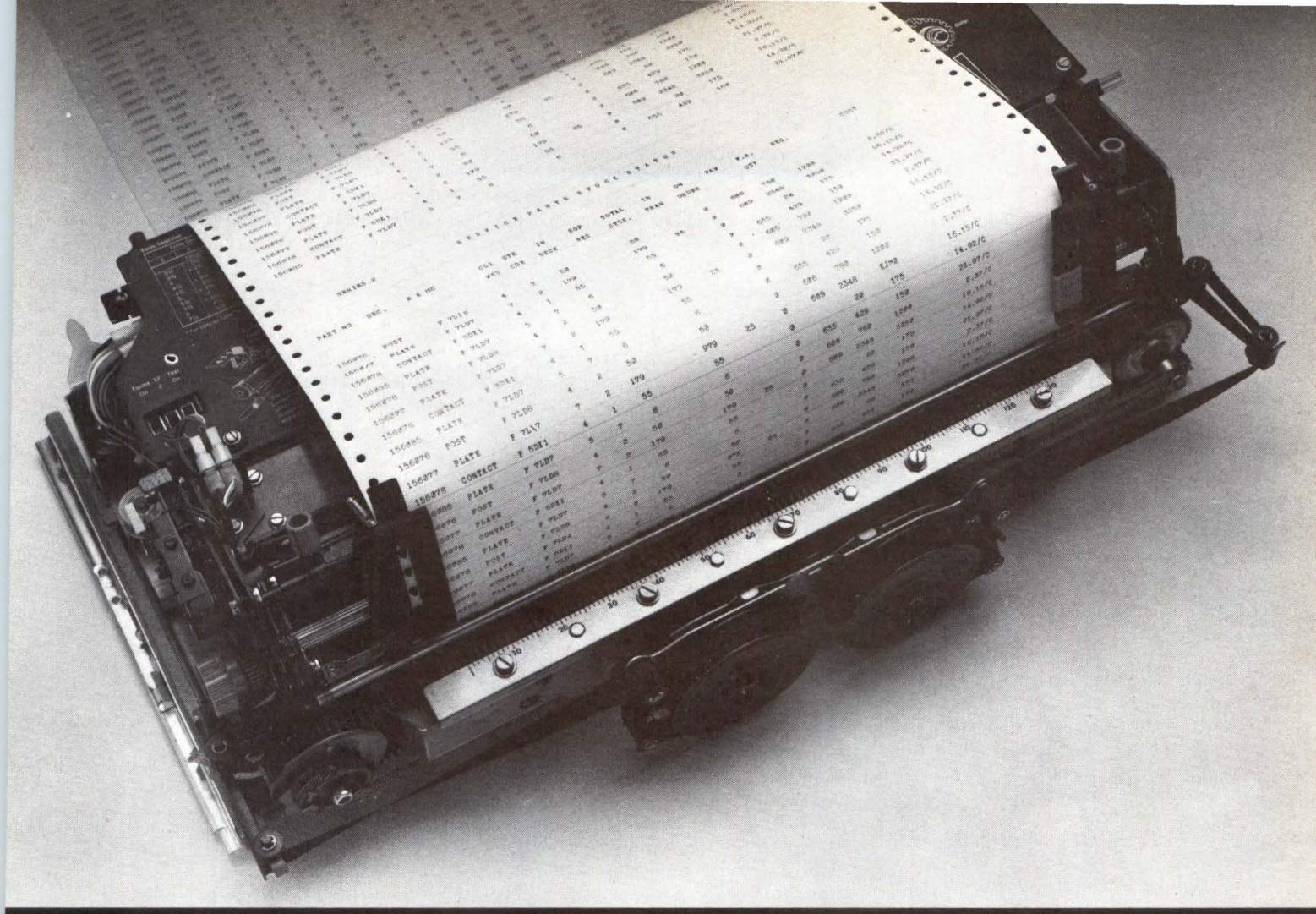
Electrical characteristics include ±128-step resolution, 128-step minimum monotonicity, ±1-step maximum chord endpoint accuracy and step linearity, and 500-ns typical settling time ±1/10 typical and ±½ maximum full scale drift at full −55 to 125°C temperature range. Versions B, C, and E have somewhat different characteristics.

Compressing A-D conversion with the device requires the usual elements in any sign-plus-magnitude ADC: a comparator, an exclusive-OR gate, and a successive approximation register. However, whereas in a conventional (linear) converter, the step size is a constant percentage of full scale, in a compressing ADC, the step size increases as the output changes from zero scale to full scale. The standard half-step bias used in conventional ADCs to keep quantizing error below ±½ step cannot be easily furnished by the user of a compressing ADC. For this reason, the DAC has a ½ step greater output in the encode mode than it has in the decode mode.



Transfer characteristics for DAC-76. If signal compression curve (left) is superimposed on expansion curve (right), average is straight line since compression and expansion must be equal and opposite

Circle 350 on Inquiry Card



The Teletype® model 40 OEM printer. When you look at it from price and performance, you'll find it difficult to look at anything else.

The fact of the matter is simply this:
We don't think any other printer can even come close to the model 40.

And that's no idle boast. Not when you consider the facts.

Consider: Where else can you get a 132-column, heavy-duty impact printer that delivers over 300 lines per minute for less than $2000, or an 80-column printer for under $1400?

The big reason behind the model 40's price/performance advantage is our unique design. Even though it operates at speeds of more than 300 lpm, wear and tear is less than you'd find in a conventional printer operating at considerably slower speed. Fewer moving parts and solid-state components add up to greater reliability and reduced maintenance.

Here's something else to consider: Where else can you get a printer that delivers the kind of flexibility and reliability the model 40 offers?

For complete information, please contact our Sales Headquarters at: 5555 Touhy Ave., Skokie, Ill. 60076. Or call Terminal Central at: (312) 982-2000.

TELETYPE

The Teletype model 40 OEM printer. Nothing even comes close.

CIRCLE 44 ON INQUIRY CARD

Peripheral Drivers Are MOS-Compatible

A series of peripheral driver ICs with one-tenth the input power requirement of competitive units and pnp construction for compatibility with MOS circuits is now available from Signetics, 811 E Arques Ave, Sunnyvale, CA 94086. DS 3611 through DS 3614 are rated for 80-V breakdown in the off state and have a current rating to 300 mA/driver in the on state. They feature high voltage pnp inputs compatible with p-MOS, CMOS, TTL, or DTL circuits. Required input current for the series is 40 μA for a logic input (logical "1") of 2.4 V.

The devices incorporate input clamping diodes for circuit protection. All units are dual drives; DS 3611 is AND, 3612 is NAND, 3613 is OR, and 3614 is NOR. Relevant applications are with high voltage breakdown, high current requirements as power drivers, relay drivers, lamp drivers, MOS drivers, and display drivers in logic-controlled equipment.

Pin-out arrangement for the series is identical to industry-standard 75451 through 75454 driver ICs. Because of the low drive requirement, however, these units can drive more peripheral circuits than standard units with an equivalent output power.

Circle 351 on Inquiry Card

16K ROM Has Complete TTL Compatibility For Microprocessor Systems

According to the manufacturer, the MK 34000 16K ROM is ideally suited for high performance applications such as 8-bit microprocessor systems. The device has a maximum access time of 350 ns and power dissipation of 330 mW.

Organized as a 2K-word by 8-bit device, the ROM requires a single 5-V power supply and has complete TTL compatibility at all inputs and outputs. There is a ±10% tolerance on the power supply and the outputs are capable of driving two TTL loads and 100 pF. Pin-out is compatible with the 2708 1K x 8 EPROM, which allows easy replacement of the ROM with two EPROMs without changing board designs.

Three chip-select inputs can be programmed for any desired combination of active highs or lows or even an optional don't care state. Static operation coupled with the programmable chip-select inputs and 3-state TTL-compatible outputs result in extremely simple interface requirements.

Mostek Corp, 1215 W Crosby Dr, Carrollton, TX 75006 offers contact programming rather than conventional gate mask programming in order to reduce the turnaround time for a custom ROM. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the circuit. Prices in 1000-piece quantities are $14.85 for the MK 34000P (ceramic package) and $13.85 for the MK 34000N (plastic package).

Circle 352 on Inquiry Card

Ladder Networks Offer Application Advantages Of Thin Film Properties

Two thin film ladder networks designed as standard product building blocks for commercial, industrial, and military D-A and A-D converter applications allow flexibility in configuring a converter to unique application requirements. Series 816-50 and -55 were introduced by Beckman Instruments, Inc, Helipot Div, 2500 Harbor Blvd, Fullerton, CA 92634 for test and measurement instrumentation, process and machine control, computer peripheral, medical diagnostic equipment, and other data distribution and control applications.

Series -50 is a 12-bit current switching (R-2R-4R-8R) ladder network for use with standard quad current switches and is housed in a standard 24-pin ceramic DIP. Its characteristics are ideal for applications where the voltage compliance range requirement is <2 V.

Available input code options are complementary straight binary, complementary offset binary, and complementary two's complement. Features include constant reference and supply current for controlled and noise-free bit switching times. Both voltage and current output versions of 0 to 5 V, 0 to 10 V, ±10 V, ±5 V, 0 to 2 mA, and ±1 mA are available.

Series -55 is a 12-bit voltage switching (R-2R) ladder network in a 16-pin ceramic DIP. The ladder, ideal for multiplying DAC applications, features close tolerance and tracking resistors for high conversion accuracy. Input versions are straight binary, offset binary, and two's complement with dc reference options to ±4 V maximum or ac to a peak value of ±4 V maximum. Output combinations available using the device are dc unipolar (0 to 10 V, 0 to −10 V), dc bipolar (±0 V maximum), and ac 2- and 4-quadrant multiply to ±10-V peak value.

Both series are specified over the 0 to 70°C or −55 to 125°C temperature ranges, and are screenable to MIL-STD-883. Prices range from $15 to $30 (100-piece price) depending on model type, accuracy, and temperature range options.

Circle 353 on Inquiry Card

Bipolar Character Generator Features On-Chip Serial Output

A high speed bipolar character generator IC with on-chip serial output has been introduced as a potential replacement for medium-scale ICs that are prevalent standards in CRT displays and matrix printers. The 64-character DM8678 LSI device, providing a 7 x 9 row scan character font, incorporates several CRT system level functions that ordinarily require the use of two to four additional packages: parallel to serial shifting, character address latching, character spacing, and character line spacing.

Produced in a 16-pin package, the 124 x 61 mil chip consists basically of a 6-bit series of fall-through latches for the character address; 4K-bit ROM (64 x 7 x 9) with a standard upper case character set; 7-bit parallel in, serial out shift register; data output buffer with a Tri-State® control; multiplexer; and edge-triggered generator. The onboard ROM, depending on the customer's choice of mask program, can have either of the two standard printer/CRT fonts,

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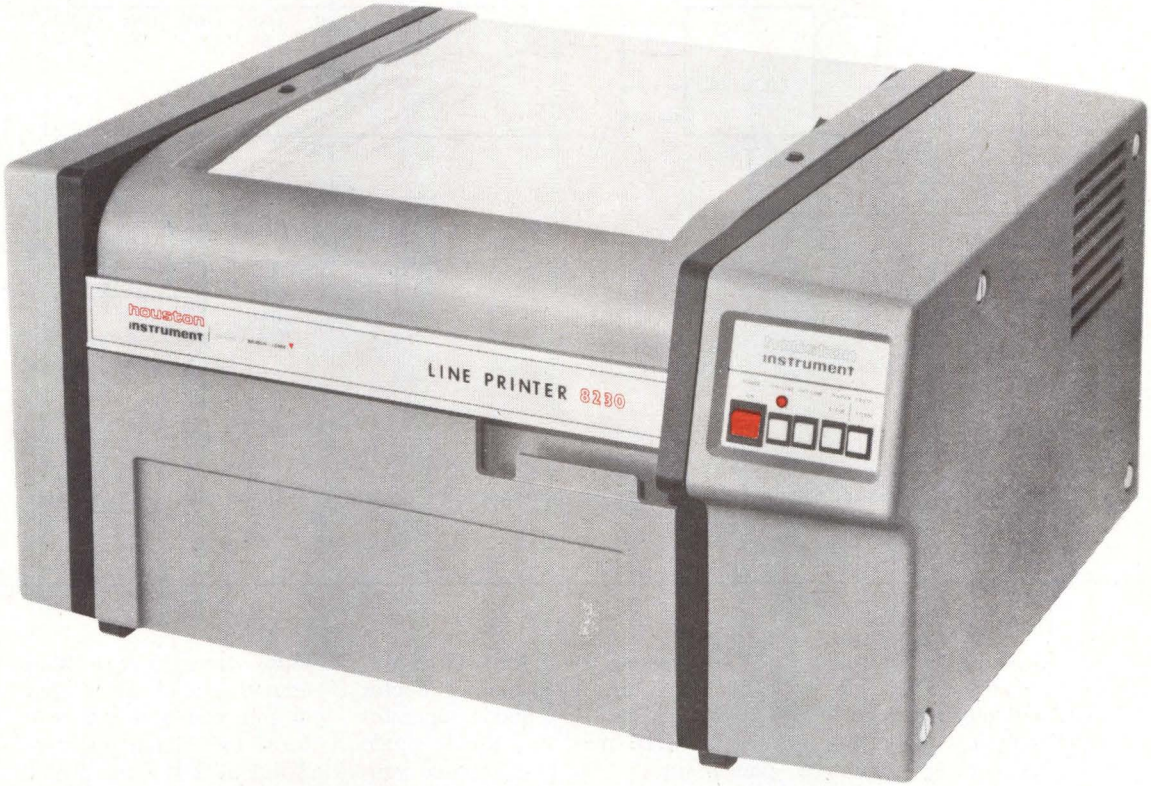
You Are Wasting More In Program Development Costs Than This LINE PRINTER Sells For

2400 LPM – 80 COL.
MODEL 8210 – $3000*

1400 LPM – 132 COL.
MODEL 8230 – $3785*



POWERFUL – A 65K byte dump may be done in 30 secs.

QUIET – The rustle of paper and the cooling motor hum are the loudest noises you'll hear.

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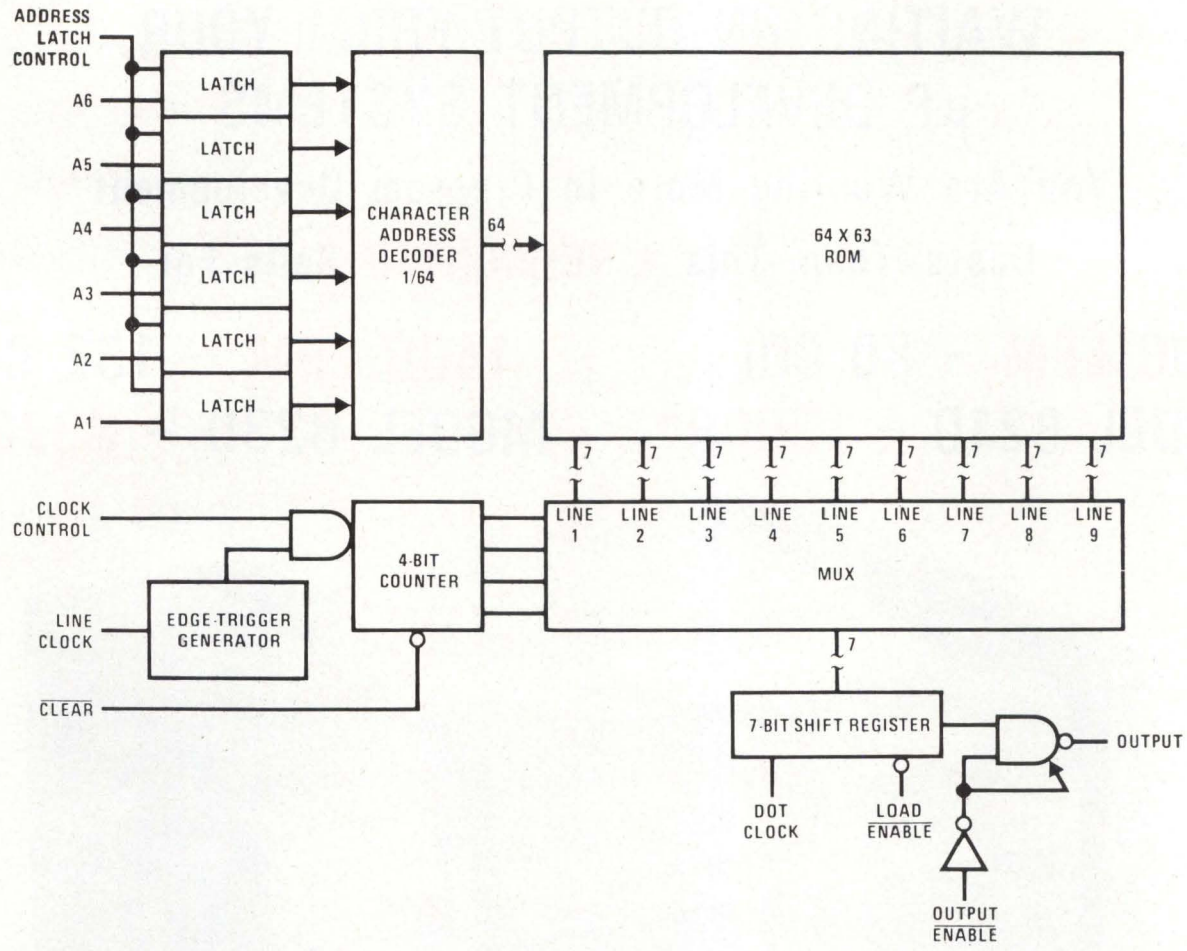
CIRCLE 45 ON INQUIRY CARD



Block diagram of National Semiconductor high speed character generator with on-chip shift register

7 x 9 or 5 x 7, or other custom upper or lower case fonts. These devices can be utilized either for horizontal CRT-style scanning across the page or, with the use of column scan fonts, for vertical dot matrix-printer style scanning down the page.

The device, from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, operates at a 20-MHz speed and uses a single power supply. Its line counter consists of a 4-bit ripple counter with an asynchronous clear input, plus an input clock that is shaped by the edge-triggered clock generator. The output can sink 16 mA at 0.45 V for a low signal out and will source 2 mA at 2.4 V for a high signal out. Total power requirement for the device is 725 mW.

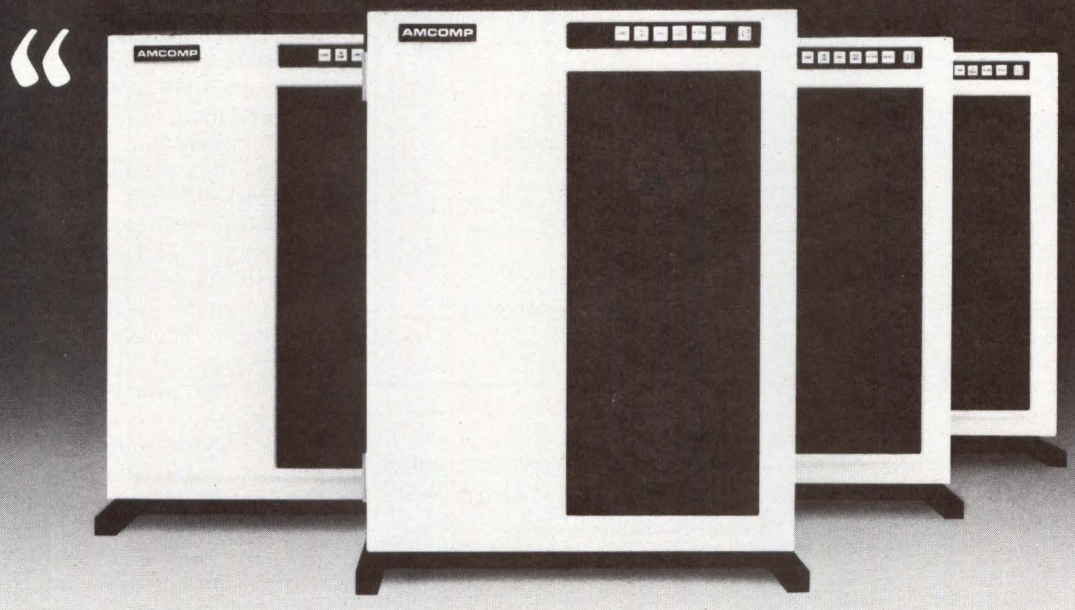
Quad NOR Gates Expand High Noise Immunity Line

Additions to the high noise immunity logic family of Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94040 consist of two quad NOR gates, each made up of two 2-input and two 3-input NOR gates. HiNIL 306 features active pullup outputs and 10-mA output drive current; it can drive lines up to 10 ft without loss of noise immunity. The 307 has open collectors, permitting outputs to be collector ORed. Both operate on 10 to 16 V and are pin-compatible with the 325.

Typical applications include CMOS input interface, industrial controls, medical instrumentation, and marine electronics. Both devices are in standard 16-pin DIPs priced at $0.81 for plastic (J) and $1.08 for ceramic (L) in 100 unit lots.

Absolute maximum ratings are 16.5-V continuous supply voltage, 18-V pulsed supply voltage (<100 ms), −0.5- to 18-V input voltage (any input), 35-mA surge sink cur-

Our commitment to the tape drive market can be summed up this way:



We make four basic tape drives. One of them is just the one you want.

Because the options we've engineered for our basic four effectively give you a choice of over 400 configurations.

Speeds from 12.5 to 125 ips. Tension arm or vacuum column. A variety of electronics options. And more.

Yet with all the differences from drive to drive, there are a number of things the same in every drive.

Simple one-hand loading, dynamic braking, linear sensors and servos, and other engineering advantages.

A near 80% parts commonality. Which makes your spares stocking, training, and servicing a lot easier. An industry-unsurpassed commitment to quality—given meaning by our industry-unsurpassed 13 month warranty. And backed by 24 hour a day, 7 days a week field service.

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AMCOMP. Our strength is our commitment. And our commitment is strong.

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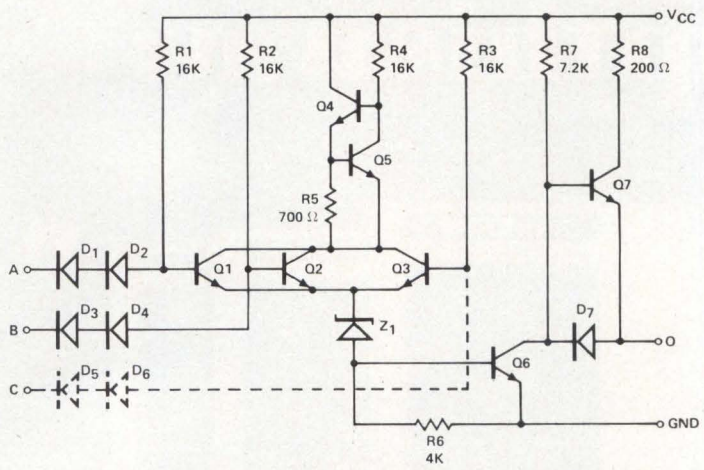
CIRCLE 46 ON INQUIRY CARD

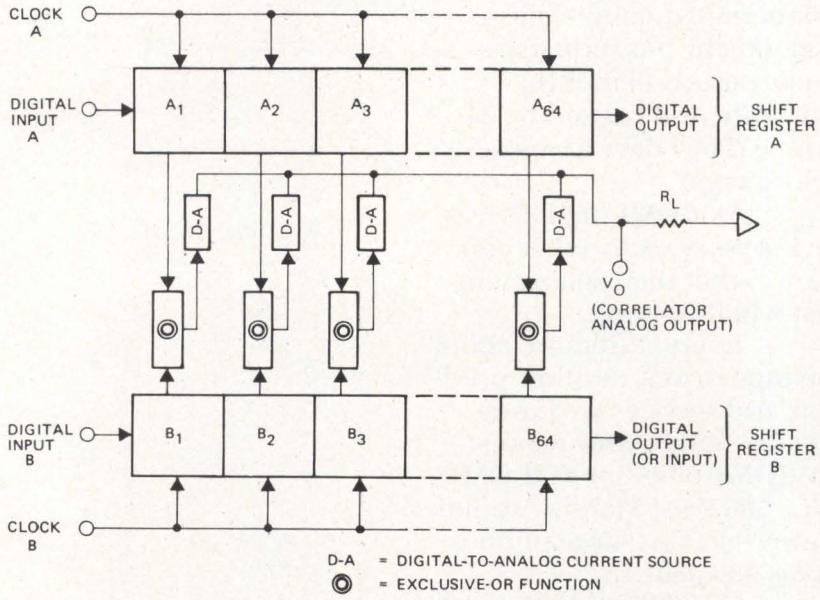


Equivalent circuit of Teledyne Semiconductor HiNIL 306 quad NOR gate

rent (<100 ns at 25°C), and −65 to 150°C storage temperature range. Electrical characteristics at V_{cc} = 13 V include input threshold voltage, 5 V minimum low and 6.5 V maximum high; low input current, −1.3 V maximum at 1.5-V input; output low voltage, 1.5 V maximum; output low voltage driving TTL, 400 mV maximum; output high voltage, 12 V minimum; and loaded output high voltage, 16.5 V minimum.

Circle 354 on Inquiry Card

Bipolar Correlator LSI Circuit Offers Signal Processing Applications



Block diagram of TRW 64-bit parallel digital correlator

A 64-bit parallel digital correlator, developed by TRW Inc's Electronic Systems Div, One Space Park, Redondo Beach, CA 90278, meets the requirements for many digital signal processing applications such as bit synchronization, bit detection, error correction coding, and pulse compression. For instance, parallel digital signal correlation can be maintained with analog output at a 20-MHz operating speed.

Correlation in the 64BCIV circuit occurs when two binary words are serially shifted into two independently clocked shift registers. These words are continually compared bit for bit by exclusive-OR circuits to provide the required function of multiplication. Each exclusive-OR circuit controls a current source DAC. Outputs of the D-A circuits are summed to produce the correlation function.

The device is fully TTL compatible; two standard TTL clocks are required for bit synchronization. Power consumption is <32 mW/correlation bit; total device consumption is 2 W. Both military and commercial temperature range versions of the 40-pin ceramic DIP are available. Current prices are $250 each in quantities of 1 to 24 and $225 each in quantities of 24 to 99, with further discounts for larger quantities.

Circle 355 on Inquiry Card

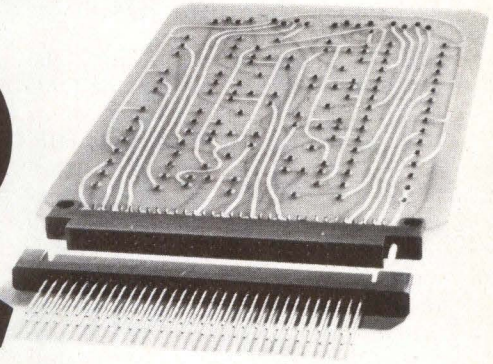
Monolithic Darlingtons Have Good Stability

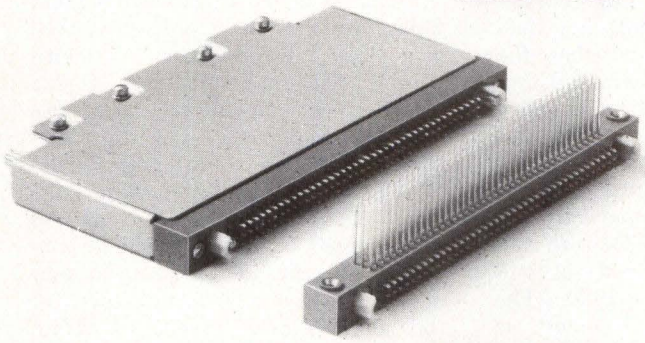
A series of npn power Darlingtons rated for 100 W and 10 A feature hard glass passivation of the silicon chip to provide exceptional stability at high junction temperatures. Designated IR1010 and IR1020, the units offer collector-to-emitter voltage ratings to 120 V. IR1020 has a minimum dc current gain of 1000 at 3 A, 1.5 V; IR1010 has a gain of 500.

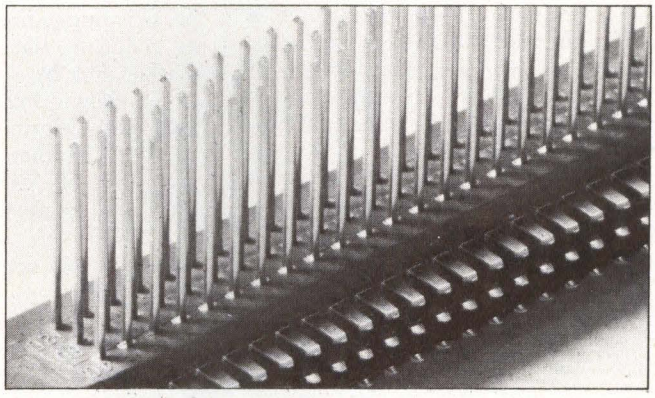
The devices from International Rectifier, Semiconductor Div, 233 Kansas St, El Segundo, CA 90245 are claimed to be especially well suited for applications in inverters, chopper regulators, and switching power supplies. Processing is triple diffused to provide for high voltage operation with fast switching and wide safe operating area. Packaging is a standard JEDEC TO-3 case.

Circle 356 on Inquiry Card

How to get a lot more into a lot less.







First, with 3 rows of contacts on .100 centers, Viking's unique Nordic 2-piece P/C board connectors and I/O I.C. panel plugs get a lot more contacts into a lot less space.

Second, our unusual polarizing system lets you key each mating pair to prevent cross mating with adjacent connectors of the same type. You can stack a series of Nordic connectors next to one another in cramped space and not worry that they might be cross mated.

Our full line includes 64 and 82 contact models as well as the 120. Contacts on I/O connectors are crimp, snap-in, removable, gold plated and use MIL-T- 22520 tools.

Diallyl Phthalate is the insulator in most models. And all connectors are designed to meet conditions of MIL-C-55302.

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O.K. Send me: ☐ Your latest catalog with details on the two-piece PC connectors ...and your nearest rep. I have some questions for him.

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Viking CONNECTORS

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CIRCLE 47 ON INQUIRY CARD

4-Quadrant Multiplying DAC Requires No External Components

Complete and "ready to use," the MN3100 4-quadrant multiplying DAC is claimed to be the first unit of its type in a hermetically-sealed DIP. An operational amplifier and laser-trimmed nichrome resistors are packaged internally, eliminating the need for external components and adjustments. Linearity is specified at better than ±½ LSB from 0 to 70°C and settling time is 50 μs for a 20-V step.

The device is guaranteed against latch up. It has CMOS inputs and consumes 210 mW of power. All key parameters of the 18-pin DIP are fully tested at the extremes of its temperature range.

According to the manufacturer, Micro Networks Corp, 324 Clark St, Worcester, MA 01606, the device is a cost-effective alternative to other devices which require the addition of op amps and trim resistors before they can be used for 4-quadrant multiplication. Priced at $50 in 25-unit quantities, the DAC eliminates the cost of supplementary components as well as the time needed for assembly and adjustment.

Applications include resolver-to-digital converters, as well as digitally controlled analog attenuators and filters where 10-bit linearity is required. It can also be used with a precision voltage reference for high accuracy D-A conversion.

Circle 357 on Inquiry Card

Data On West European IC Market Provided On Subscription Basis

According to information compiled by an international consulting group, the growth rate for ICs in the Western European market from 1976 to 1980 will exceed that for the U.S. market. Total IC market growth in Western Europe will average 17.3% per year through 1980 as compared to 12.0% in the U.S. The growth of MOS LSI, which includes most semiconductor memory and microprocessor devices, will average 26.0% per year for Western Europe and only 15.7% for the U.S.

Currently U.S. semiconductor companies supply more than 80% of the West European MOS LSI market. One of the major questions now facing U.S. producers is whether the steps being taken by Western European manufacturers will be effective in reducing the domination of this market area by U.S. firms.

West European Integrated Circuit Markets (Millions)

Segmentation by Technology

	1974	1976	1980
Bipolar Digital	$ 257	$ 206	$ 327
Bipolar Linear	251	223	378
MOS	135	169	424
Total	$ 643	$ 598	$1129

Segmentation by Country

	1974	1976	1980
West Germany	$ 235 (36.6%)	$ 220 (36.8%)	$ 410 (36.3%)
France	113 (17.6%)	108 (18.1%)	221 (19.6%)
U.K.	127 (19.8%)	113 (18.9%)	206 (18.2%)
Italy	60 (9.3%)	56 (9.4%)	94 (8.3%)
Rest of Europe	108 (16.8%)	101 (16.9%)	198 (17.5%)
Total	$ 643 (100%)	$ 598 (100%)	$1129 (100%)

As shown in the tables, the IC market in Western Europe was lower in 1976 than in 1974—with the exception of MOS devices—but will increase drastically by 1980. The West German market is almost as large as the combined French and U.S. markets.

Continuous strategic and tactical planning and data concerning the IC market in Western Europe will be provided in a subscription service initiated by Mackintosh Consultants, Ltd, 2680 Bayshore Frontage Rd, Mountain View, CA 94040. Annual fee will be $12,000. This program, called International Strategy and Information Service-Integrated Circuits (ISIS-IC), is designed to provide clients with a continuous flow of information about Western Europe as well as access to Mackintosh staff and data bases.

Basic elements include a 5-year market forecast for IC products in terms of end-market and country of use, with market reports issued quarterly for the different West European geographic areas and updated annually; and four "Euroview" reports each year, covering such topics as a detailed analysis of the structure and requirements of a specific end-industry, an analysis of the impact of a new technology, a study of an emerging market, and a description of different strategic alternatives to cope with changes in the European environment.

Other elements include an annual 2-day ISIS Strategy Conference held in a major West European city, with special Executive Summary report covering IC markets and strategies issued in conjunction with the meeting; an individual briefing session tailored to the specific needs of each client which addresses questions and topics posed by the clients; and continuous access to Mackintosh staff and data bases. This last aspect of the service allows clients to obtain near immediate responses to questions submitted by letter, TWX, or telephone.

Circle 358 on Inquiry Card

8K EPROM Adapted for Use With Microcomputers

Data can be freely stored or deleted in the fixed storage of a microprogramming system such as a microcomputer or POS terminal through use of an MB8518 erasable programmable ROM. The 8K device, made by Fujitsu Ltd, Tokyo, Japan, is compatible with the Intel 2708 memory. A ROM MB8308 mask memory permits data to be stored in the memory only once.

Two versions of the memory have been developed: the H version has an access time of 450 ns, the E requires 650 ns. Specifications for both include: power consumption, 850 mW; write time, 100 s/chip; configuration, 1K x 8; and power supplies, 12 and ±5 V. Devices are in 24-pin DIPs. □

Circle 359 on Inquiry Card

YOU WERE HIRED FOR YOUR BRAINS, NOT YOUR BODY.

It's not as silly as it sounds. Because many bright engineers and technicians are still spending their time soldering, desoldering and resoldering. Instead of designing.

Which *is* pretty silly, considering the waste of talent. Especially when there's a better alternative.

With CSC Proto-Board® solderless breadboards, assembling a circuit is practically as fast as designing one. No special jumpers or patch cords required—all types of components—from complex microprocessors to resistors, capacitors and LED's—connect and interconnect as simply as pushing in a lead . . . or short lengths of #22-30 solid hookup wire. And circuit changes are done with the same plug-out, plug-in ease. All thanks to rugged, nickel-silver contacts and CSC's superior use-tested design.

MODEL	NO. OF TIE-POINTS	14-PIN DIP CAPACITY	MFR'S SUGGEST LIST*	OTHER FEATURES
PB-6	630	6	$15.95	Kit—10-minute assembly
PB-100	760	10	19.95	Kit—with larger capacity
PB-101	940	10	29.95	8 distribution buses, higher capacity
PB-102	1240	12	39.95	Large capacity, moderate price
PB-103	2250	24	59.95	Even larger capacity; only 2.7¢ per tie-point
PB-104	3060	32	79.95	Largest capacity; lowest price per tie-point
PB-203	2250	24	75.00	Built-in 1%-regulated 5V, 1A low-ripple power supply
PB-203A	2250	24	120.00	As above plus separate ½-amp +15V and −15V internally adjustable regulated outputs

*Manufacturer's suggested list Prices and specifications subject to change without notice

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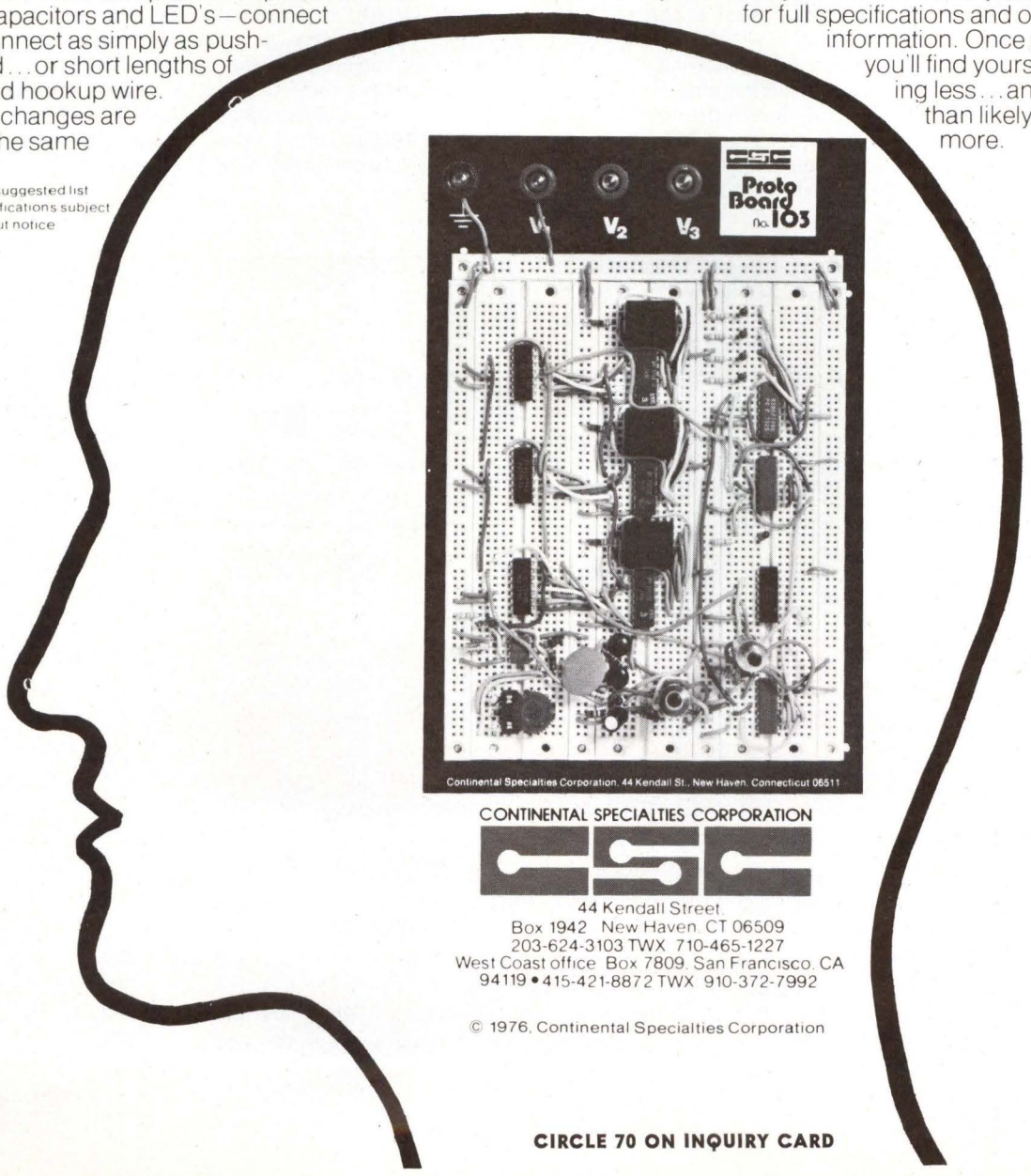

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CIRCLE 70 ON INQUIRY CARD

MICRO PROCESSOR COMPUTER DATA STACK

Microcomputer Interfacing: The Vectored Interrupt

Jonathan A. Titus
Tychon, Inc

Peter R. Rony
Virginia Polytechnic Institute & State University

David G. Larsen
Virginia Polytechnic Institute & State University

As a continuation of the discussion of computer interrupts, this month's emphasis is upon vector interrupt hardware and software associated with the 8080A microprocessor chip. The three signals used in vector interrupt circuits include INT (input pin 14 on the 8080A chip), INTE (output pin 16), and $\overline{\text{INTA}}$ (not available on the 8080A chip but derived externally with additional logic).

A positive clock pulse from an interrupting device supplies a logic 1 state at the INT, or interrupt request, input that generates an interrupt request. The CPU recognizes this either at the end of the current instruction being executed or while the CPU is in the halt state. The INTE, or interrupt enable, output pin indicates the logic state of the interrupt enable flip-flop present within the processor chip. This internal flip-flop can be set (enabled) or cleared (disabled) with the aid of 8080A microcomputer instructions:

363	DI	Disable interrupt flip-flop
373	EI	Enable interrupt flip-flop

When cleared, the interrupt enable flip-flop inhibits interrupts from being accepted by the CPU. The flip-flop is automatically cleared when an interrupt is accepted; it is also cleared by the RESET input signal applied at pin 12 of the processor chip.

The $\overline{\text{INTA}}$ (interrupt acknowledge) control signal is generated by applying INTA and DBIN control signals to a 2-input NAND gate (Fig. 1). A logic 1 at DBIN (output pin 17 on the chip), or data bus in, indicates to external devices that the data bus is in the input mode. The INTA control signal is a positive clock pulse generated as a status output with the aid of a status latch connected to the microprocessor chip.[1,2] (The status latch will be discussed in a subsequent column.) An interesting aspect of the INTA control signal is that it permits an interrupt vector instruction byte to be "jammed" directly into the

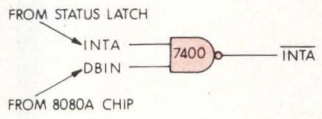


Fig. 1 $\overline{\text{INTA}}$ control signal is generated from DBIN and INTA control signals, only one of which is available on the 8080A chip

Instructions to Jam Instruction Register

307	RST 0	Call subroutine that starts at HI = 000 and LO = 000
317	RST 1	Call subroutine that starts at HI = 000 and LO = 010
327	RST 2	Call subroutine that starts at HI = 000 and LO = 020
337	RST 3	Call subroutine that starts at HI = 000 and LO = 030
347	RST 4	Call subroutine that starts at HI = 000 and LO = 040
357	RST 5	Call subroutine that starts at HI = 000 and LO = 050
367	RST 6	Call subroutine that starts at HI = 000 and LO = 060
377	RST 7	Call subroutine that starts at HI = 000 and LO = 070

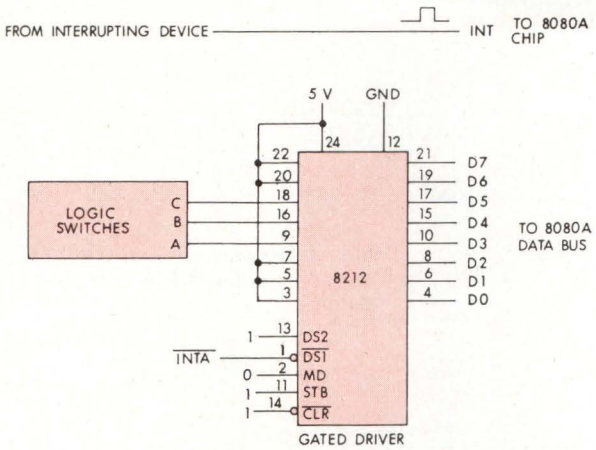


Fig. 2 Interface circuit for jamming of a single-byte instruction into the instruction register of an 8080A microprocessor chip

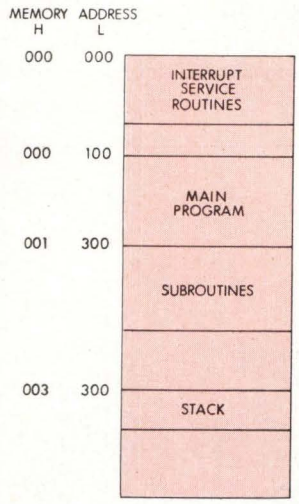


Fig. 3 Possible memory "map" for 8080A microcomputers

instruction register within the chip. This can only be done during an interrupt, but nevertheless it is a unique and interesting operation that is possible with the 8080A microprocessor.

A simple circuit that demonstrates how a single-byte instruction can be jammed into the instruction register is provided in Fig. 2. Assuming that the interrupt enable flip-flop has been previously enabled by the instruction, 373, the interrupting device must supply a logic 1 input at INT in order to generate an interrupt request. The microcomputer finishes the current instruction, then generates the interrupt acknowledge signal, INTA, which jams the desired vector instruction byte on the data bus and into the instruction register. Although any instruction byte can be jammed into the instruction register during an interrupt, usually eight instructions are utilized to produce a useful result (see listing of Instructions to Jam Instruction Register).

Thus, the first 64 memory locations are reserved for interrupt service routines or pointers, extremely short programs often consisting of only a single jump instruction, that tell the 8080 microcomputer what to do or where to go for a specified interrupt condition. Such routines precede the main program and associated subroutines in memory (Fig. 3). If interrupts or restart instructions are not used, this portion of memory has no special significance.

Fig. 4 is probably the simplest priority encoder interrupt circuit that can be used with an 8080 microcomputer. The Intel 8212 chip is used as an 8-bit 3-state buffer that inputs the instruction byte into the instruction register. In the Truth Table for the 74148 8-line-to-3-line priority encoder chip the letter X means that the logic state is irrelevant.

The circuit in Fig. 4 serves to input the restart instruction, 3Y7, into the microcomputer. Five of the eight inputs to the 8212 are tied to a logic 1 state. The remaining three bits supply the encoded vector address of the restart subroutine. By virtue of its truth table, the 74148 priority encoder chip provides eight priority levels. Inputs to this chip should be latched. The encoder provides the 3-bit binary output that corresponds to the highest valued priority input which is at a logic 0 state; inverters invert

Truth Table for 74148 Priority Encoder Chip

Inputs								Outputs			
0	1	2	3	4	5	6	7	C	B	A	E0
X	X	X	X	X	X	X	0	0	0	0	1
X	X	X	X	X	X	0	1	0	0	1	1
X	X	X	X	X	0	1	1	0	1	0	1
X	X	X	X	0	1	1	1	0	1	1	1
X	X	X	0	1	1	1	1	1	0	0	1
X	X	0	1	1	1	1	1	1	0	1	1
X	0	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	0

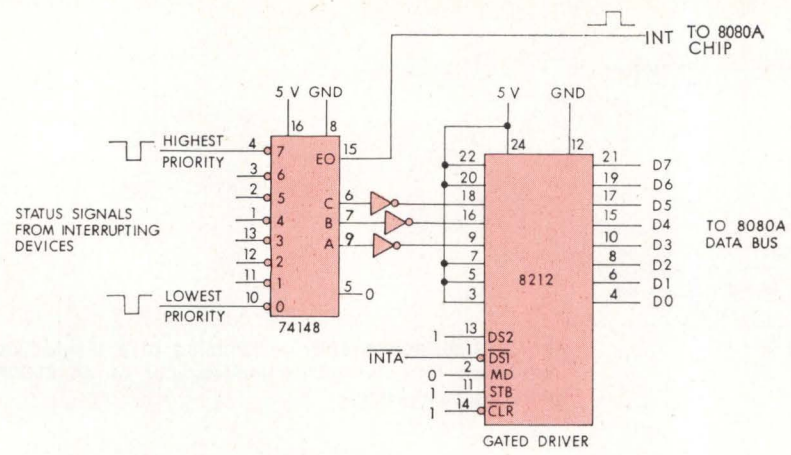


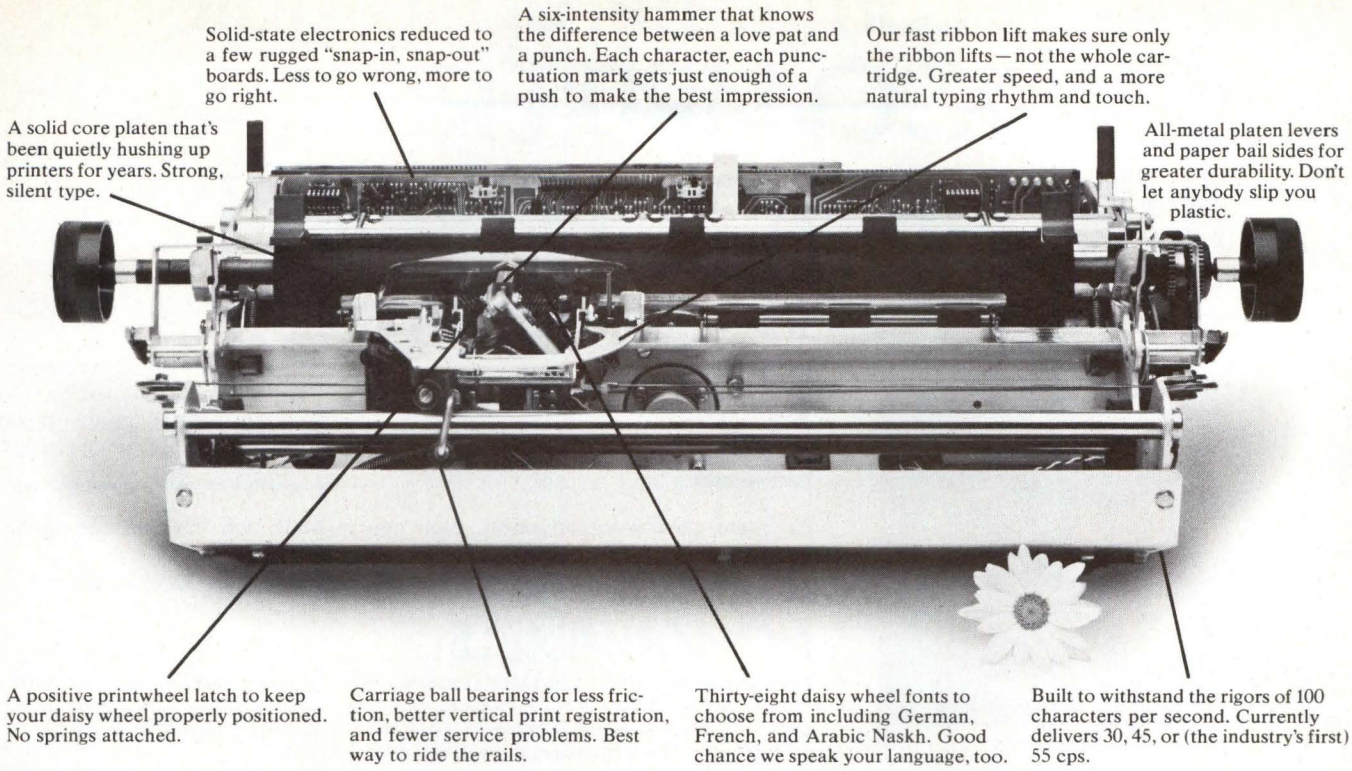
Fig. 4 Priority interrupt encoding scheme for 8080A microcomputers

this information to supply the 3-bit "Y" component of the restart instruction. If there is a logic 0 at any of the inputs to the 74148, a logic 1 output will be generated at the E0 output (pin 15). This output serves as the input to the interrupt request pin, INT, on the 8080A. Upon receiving an interrupt request, the microcomputer responds with an interrupt acknowledge output, $\overline{\text{INTA}}$, that strobes the selected highest priority restart instruction into the instruction register.

References

1. *Intel 8080 Microcomputer Systems User's Manual,* Intel Corp, Santa Clara, Calif, Sept 1975
2. *Bugbook III. Microcomputer Interfacing Experiments Using the Mark 80[R] Microcomputer, an 8080 System,* E & L Instruments, Inc, Derby, Conn, 1975

This article is based, with permission, on a column appearing in *American Laboratory* magazine.



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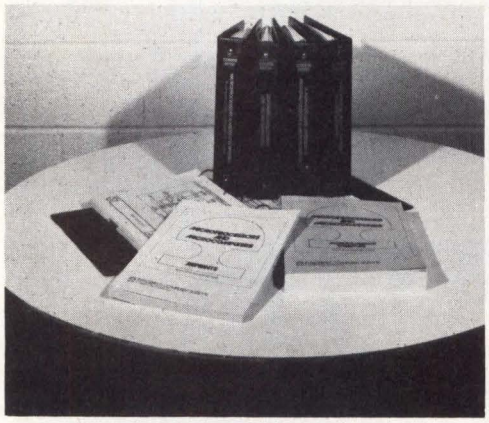

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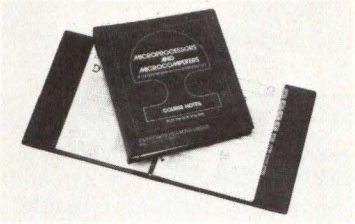

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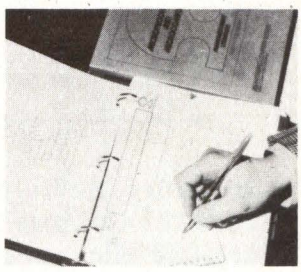

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BASIC Interpreter Aimed at 8080 μComputer Small Business Users

Ease of program development and straightforward 1-step program execution are the goals of BASIC ETC, an interpreter for 8080-based microcomputer small business applications and game programming. (Less frequently used scientific functions of Dartmouth BASIC therefore are not available.) An interpretive translator, which translates and executes programs directly, was chosen over a compiler because it frees the user from deciphering program bugs at the object level.

The memory-efficient program uses the lower 8K of memory plus at least 1K of RAM for scratchpad. Features include full string capability, n-dimensional arrays, variable precision arithmetic, and direct memory and I/O addressing. There are 27 error codes, 31 commands and statements, and eight functions plus user defined functions.

Introduced by Binary Systems, Inc, 6345 Central Expressway, Richardson, TX 75080, the kit, which includes the program on either paper or audio cassette tape and a user's manual, sells for $25.

Circle 170 on Inquiry Card

Hardware/Software Tool Produces Custom Software For 6800 Microprocessor

Providing a complete hardware/software tool for developing custom software packages to run on any Motorola 6800 microprocessor system or on the DynaTermDisk®, the Microcomputer System (DMS), introduced by Dynalogic Corp Ltd, 141 Bentley Ave, Ottawa, Canada K2E 6T7, includes a model 7002A dual-drive DynaTermDisk, 8K of RAM (expandable to 64K), DMS Micro Monitor software with DTD Virtual Memory Editor, plus two RS-232-C ports for interfacing a terminal and line printer. Terminal may be any RS-232-C CRT or hard-copy unit, and the printer may be matrix line or high quality serial impact type.

Software contains a file management system having one file director per diskette. Dynbug, an absolute assembler and powerful symbolic debugging package, provides the facility to examine and change memory locations, insert multiple breakpoints, and symbolically trace program execution in both the local and global sense. Editing of source files is done with the DTD editor.

Basic DMS microcomputer system containing dual-drive DynaTermDisk®, 8K RAM, software, and two RS-232-C ports for terminal and line printer interfacing is a hardware/software tool for developing custom software for 6800 systems

Utilities include an I/O data formatting package and 12-digit floating point math package. Application packages include mailing list preparation and data entry and verification routines.

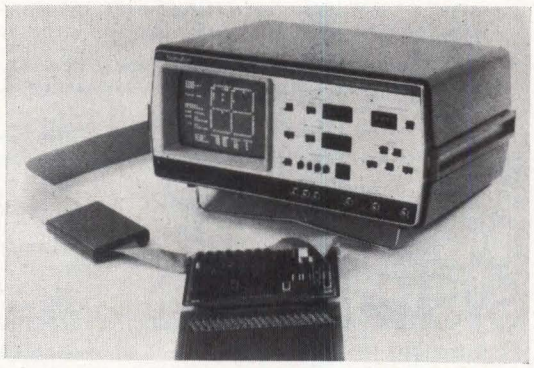
Circle 171 on Inquiry Card

μProcessor Analyzer Uses Four Formats To Study Firmware Activity

Designed for microprocessor-based equipment and systems, the model 168-D microprocessor analyzer captures firmware operations in real time and examines the activity in four analysis formats. A history of up to 256 memory accesses, beginning with a preselected 16-bit start event and/or ending with a preselected stop event, is recorded. The information is then presented on a built-in 9" CRT in one of four alphanumeric formats. Two display formats present data in hexadecimal notation using memory maps; the other two display data in hexadecimal characters as a function of time.

With a movable cursor, specific data words can be located and traced through all display formats. Capable of being completely transparent to the microprocessor, the analyzer can also be set to halt operation and single-step the microprocessor through its program.

Developed by Biomation Corp, 10411 Bubb Rd, Cupertino, CA 95014, the unit has a relatively long 256-word memory. Each word is 25 bits wide—16 bits of address information, eight bits of data, and one bit signifying either a read or write operation—all hex characters. Maximum record rate is 10 MHz which allows the analyzer to be used with both MOS and bipolar microprocessors. An individual personality module for each type of microprocessor connects the system with the analyzer. Mod-



Self-contained microprocessor analyzer with CRT output offers capability of capturing firmware operations in real time and examining activity in four analysis formats

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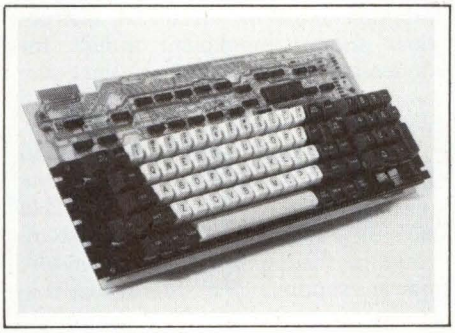

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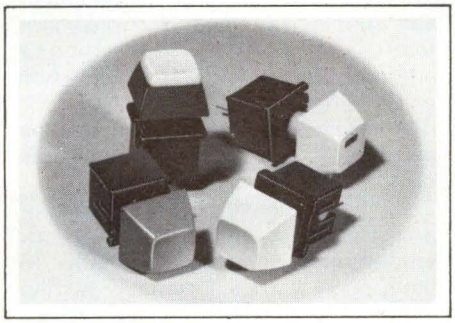

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ules are currently available for the 8080A and 6800 microprocessors. Additional ones are planned.

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Circle 172 on Inquiry Card

Plastic Packaged CPUs Offered at 50% Price Reduction

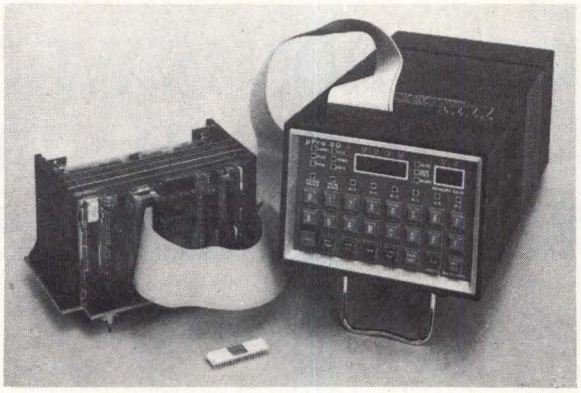
Representing a reduction of more than 50% in CPU costs, two plastic packaged central processor units for the MCS-40™ Microcomputer System 4-bit family are available from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. In quantities of 100 and up, the P4040 (24-pin package) costs $5.50 and P4004 (16-pin package) costs $5.00. Both are supplied in molded epoxy DIPs. An enhanced version of the 4004, P4040 includes 60 instructions, an interrupt mechanism, and single-step control. MCS-40 systems, containing the new CPU, clock generator, memory, and I/O will cost as little as $19.25 in 100-up quantities.

Both CPUs operate at a typical instruction cycle time of 10.8 μs. The "P" series, and hermetic packaged "C" and "D" series, are guaranteed to operate over the 0 to 70°C temperature range at that rate; D and C series are also available with guaranteed operation over the extended industrial temperature range of −40 to 85°C. The different package series are interchangeable in most applications.

Circle 173 on Inquiry Card

In-Circuit Emulator Duplicates 8080 Microprocessor Functions

In-circuit emulation can be added to systems containing 8080A or 8080A-2 microprocessors with the μPro-80-E emulator which duplicates the microprocessor functions and gives the user a comprehensive hexadecimal control/display console. Memory and I/O devices are segmented between the system under test and the emulator. All operations are performed in real time for user system clock periods from 350 to 600 ms.



Shown in typical test situation, modular in-circuit emulator (right) from muPro, Inc features hexadecimal control/display console, 8080 emulator, and interconnecting flat cable for duplicating functions of the 8080A and 8080A-2 microprocessors

With the console, the user can monitor program execution; examine or alter memory locations, registers, or status bits; insert breakpoints at program or data locations; and perform a program trace of up to 64 instructions prior to breakpoint or halt. Independent of the host system, the emulator requires no additional peripheral devices.

Developed by muPro, Inc, 10340 Bubb Rd, Cupertino, CA 95014, the portable modular package, available as either a basic or enlarged system, contains the 8080 emulator, console, power supply, two interchangeable 40-pin headers, interconnecting flat cable, and user's manual. Chassis has six card slots to add memory and peripheral controllers. Systems can also accommodate an 8-slot expansion module for more memory, controllers, and user-defined cards. Up to 64K of memory can be added.

Basic emulator also comes in a development system version (μPro-80-ED) which includes 16K bytes of RAM and peripheral interfaces for CRT or teletypewriter, line printer, paper tape reader, and paper tape punch. It also contains the company's BSAL-80 assembler, relocating linking loader, and text editor software package.

Circle 174 on Inquiry Card

16-Bit Military Microcomputer Chosen for SEM Configuration

Developed under a Naval Air Systems Command digital missile autopilot program, the rugged high speed 16-bit military microcomputer from Hughes Aircraft Co, PO Box 90515, Los Angeles, CA 90009, is to be implemented in U.S. Navy Standard Electronic Modules (SEM) for the Naval Avionics Facility in Indianapolis, Ind. SEMs facilitate design, production, and support of Navy electronic systems. The AN/UYK-30 computer's original configuration is on either two or three 5.6 x 6.2" circuit boards; for the SEM version, the device will be partitioned onto six modules, with each board measuring 1.9 x 5.6".

Bipolar Schottky TTL LSI microprocessor chips are used in the microcomputer to achieve a 340K- to 660K-operation/s capability within military temperature specifications, and to perform arithmetic functions. Also included are an LSI microprogram control chip, four p/ROMs, and 60 MSI/SSI components. All parts are military-qualified and second-sourced. MTBF for the 2-board configuration operated in a missile or unmanned aircraft is 20,000 hours. A 50-instruction set for the device is tailored for military applications.

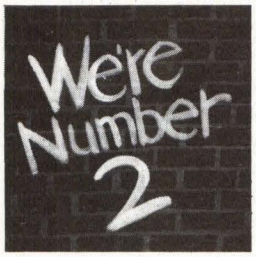
Circle 175 on Inquiry Card

Development System Has In-Circuit Emulation for Several Microprocessors

Reducing the time and cost of getting a prototype system from design into production by speeding hardware and software development, the floppy disc-based universal development system from Millennium Information Systems, Inc, 420 Mathew

While other mini-makers have been pushing & shoving...

one company has quietly become number 2*.



They've quietly shipped over 9,000 computers. In fact, over 400 of their minis are going to OEM's every month.

Because so many computer makers use their minis, they're often called the Computer Company's Computer Company.

Others deliver a mini or two to get an OEM roped in . . . then make them wait for 9 months. While this quiet company ships quantities in 45 days.

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For further information, contact: Digital Computer Controls, Inc.,
12 Industrial Road, Fairfield, N.J. 07006, (201) 575-9100

TWX 7107344310

*In the number of minicomputers currently being shipped to Original Equipment Manufacturers.

CIRCLE 51 ON INQUIRY CARD

St, Santa Clara, CA 95050, interfaces to 8080 and 2650 microprocessors.

The system—Universal One—provides two modes of real-time, in-circuit emulation for the critical phase of integrating hardware and software. In the first mode, the prototype's microprocessor and memory are emulated while I/O functions are controlled by the user's hardware. In the second, the prototype uses its own memory and I/O capabilities. A powerful universal disc operating system (UDOS) is built around a floppy disc to provide several development aids and protection devices, such as automatically allocating and de-allocating file space.

Both dynamic trace and breakpoint analyses are performed with the system. Instruction-by-instruction, the activity of a program can be traced with the dynamic trace capability. The location of each instruction, mnemonic, register contents, and state of the prototype are all displayed. For breakpoint analyses, two hardware registers provide a break and display of the breakpoint address and contents on memory fetch only, memory write only, or memory read/write access.

Other features include a text editor for character and line editing, plus macro and iteration capabilities for combining commands. Front panel sockets are provided for commonly used p/ROMs, the 1702A MOS erasable, and 82S115 family of bipolar p/ROMs. Others will be added in the future, as will capability to interface to the 6800 and other microprocessors.

Circle 176 on Inquiry Card

Intelligent Breadboard Aids in Design and Testing of Circuits

Development of discrete logic circuits and microprocessor software circuits is assisted and expedited by the Intelligent Breadboard System. Supplied as a complete integrated package, the console connects directly to the IMSAI-8080 computer (see *Computer Design*, June 1976, pp 118-119), allowing circuits to be implemented in hardware and transferred to software in a step-by-step manner. Hardware-software tradeoffs can be studied and circuit design tested extensively since the computer and breadboard communicate.

According to IMS Associates, Inc, 14860 Wicks Blvd, San Leandro, CA 94577, the system is an efficient educational and laboratory tool; it can be used to develop I/O interfaces and memory systems outside the computer that connect directly to it, and to function as an aid in writing software.

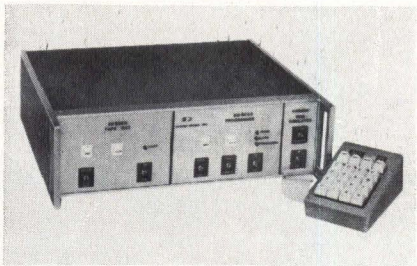
Computer interface to the system is the company's programmable Parallel I/O Board (PIO-6) which brings the address, data, control, and power lines to the console and allows TTL data communication between the program and system. Other features include easy access to signals for probing, connection of multiple computers and breadboards, use of LEDs as latched and unlatched level indicators, and plugging of ICs, resistors, and capacitors into solderless terminal strips. Complete console containing space for 40 16-pin ICs, 10 LEDs, two 5-V regulators, and two 50-pin and one 26-pin connectors costs $435 for the kit, $625 assembled.

Circle 177 on Inquiry Card

Self-Contained ROM Simulation System Combines Three Functions

Simulation, programming, and storage are all combined in a single unit for use with TTL-compatible p/ROMs and ROMs. Introduced by Electro Design, Inc, 8141 Engineer Rd, San Diego, CA 92111, model ED6000 is comprised of an addressable simulator, read/write cassette tape unit, and programmer.

Data entry to the general-purpose memory is from a hand-held hex keyboard (with address and data LED readouts), or any 8-bit data bus, RS-232, or TTY system. The remote/local switch provides for data transfer between the instrument and external circuits via a plug-in cable connected to a 16- to 24-pin ROM socket. All three instrument data sources—simulator memory, tape storage, and programmed ROM—are accessible. Address incrementing is automatic/manual with decrement manual only. Data selection is randomly accessible in half-byte increments to facilitate lookup.



Circle 178 on Inquiry Card

Display Interface Module Stores 3-D Points In High Speed Memory

As an interface with standard 8-bit microprocessors for storing 256 3-dimensional points in high speed recirculating memory (6K of RAM) with 8-bit resolution, model 6711 provides three analog output data streams representing each of three mutually perpendicular deflection axes. The module may be hard-wired directly to the company's model 6114 3-D display generator module.

Connecting to the 8-bit data bus or 8-bit data output port, the interface module appears as a memory location to the microprocessor. Two address lines are required to connect it to either the microprocessor address bus or to another data I/O port. It also requires a strobe or read/write command, and sends back an execution bit when ready to receive more data.

Announced by Optical Electronics, Inc, PO Box 11140, Tucson, AZ 85734, the module utilizes internal address counters which can be incremented by the microprocessor or left to free run. Internal address counters simplify external addressing requirements from the microprocessor.

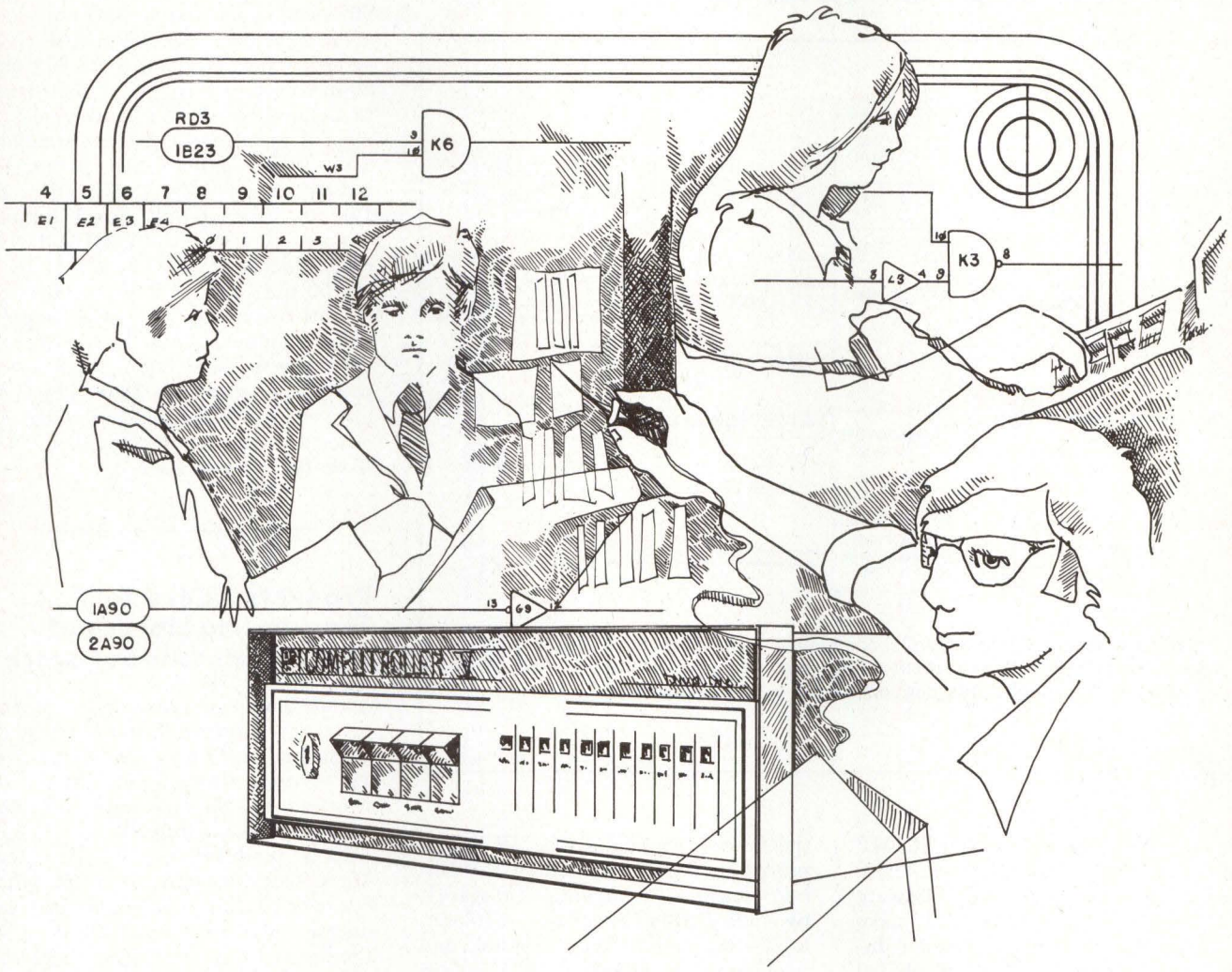
Operating on either standard microcomputer power supply lines or analog lines, the module requires 5 V at 300 mA and −12 and −15 V at 100 mA maximum. Analog outputs are current outputs with ±1-mA full scale limits. Data may be written in at random, or at any rate up to 1.2 kHz. Information is read out at a rate of 300 kHz.

Programs are available for the F8, 8080A, 6800, 2650, 1802, and SC/MP microprocessors; interfacing connection details show exact connections to various evaluation kits utilizing these microprocessors.

Circle 179 on Inquiry Card

INTRODUCING AN INNOVATION IN DISC CONTROLLER DESIGN

DIVA'S COMPUTROLLER V



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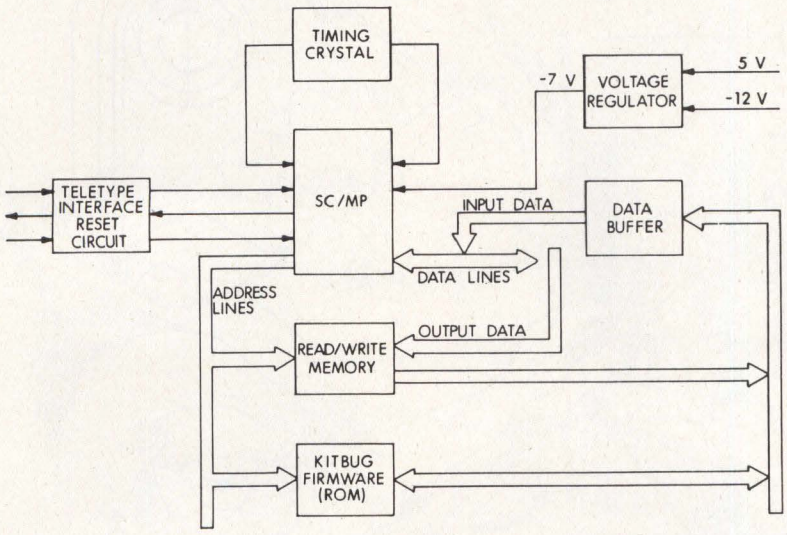
CIRCLE 52 ON INQUIRY CARD

Preassembled Boards Permit Evaluation of Simple Microprocessor



National Semiconductor Corp's completely assembled SC-8 board contains a SC/MP microprocessor chip that controls operation, and all firmware and components needed for full system evaluation

Preassembled and fully tested SC/MP 8-bit microcomputer boards—or SC-8 (skate) boards—include all firmware and components necessary to make a full evaluation of the system. Intended for less electronically-skilled people, the board allows the user to explore the capabilities of the SC/MP microprocessor.

Each of the boards from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 is priced at $125 in quantities up to ten. Measuring 4 x 5" and incorporating a standard 72-pin edge connector, the boards contain a SC/MP microprocessor, ROM (containing the Kitbug monitor/debugging program), two 1K RAMs, a voltage regulator, 8-bit data buffer, timing crystal, and teletypewriter interface device (see *Computer Design*, July 1976, p 128).

The microprocessor's TTL-compatible I/O interface simplifies connection of the user's hardware to the board, enabling real-life test and demonstration circuits to be easily implemented. With the SC/MP instruction set, the user's application programs control the hardware.

Single Board Kit Doubles As Computer and Intelligent Terminal

For use as either a computer or intelligent terminal, Sol Terminal Computer is a one board PC kit with memory and interface electronics including video display, keyboard interface, and audio cassette interface. Built around the 8080 microprocessor, the terminal consists of a PC assembly with 512 8-bit bytes of p/ROM on a plug-in module, 2048 8-bit words of RAM, 1024-character video display generator, keyboard interface, serial and parallel interfaces for connection to external devices, and an edge connector for memory expansion to 65K bytes. Compatible with IMSAI, Altair, and other S-100 bus computers, the computer can accept the line of memory and interface modules also produced by Processor Technology, 6200 Hollis St, Emeryville, CA 94608.

Display is 16 lines of 64 characters per line. The character set contains 96 ASCII upper and lower case characters plus 32 selectable control characters. Serial interface is RS-232 and 20-mA current loop, 75 to 9600 baud asynchronous. Parallel interface is eight data bits for I/O, with standard TTL levels; output bus is 3-state for bidirectional interfaces. Specs include 1.0- to 2.5-V pk-pk signal output; nominal bandwidth is 7 MHz. Power requirements are 5 V at 2.5 A, 12 V at 150 mA; and −12 V at 200 mA.

Options include a power supply, video monitor, ASCII keyboard and case, floppy disc system, high speed paper tape reader, p/ROM programmer, and color graphics interface. All necessary software is provided.

Circle 180 on Inquiry Card

Products Added to Timesharing Library of Microprocessor Software

A substantial increase in its microprocessor software library, currently consisting of 25 microprocessors from 15 manufacturers, has been announced by National CSS, Inc, 542 Westport Ave, Norwalk, CT 06851. Added products include Advanced Micro Devices 908A, Scientific Micro Systems MCCAP, National Semiconductor SC/MP, and Zilog Z-80. Products from American Microsystems, Electronic Arrays, Fairchild, Intel, MOS Technology, Raytheon, RCA, Rockwell International, Signetics, Texas Instruments, and Intermetrics are also available on the network, which is claimed to have the largest library available on an interactive, time-sharing basis.

The flexible approach to microprocessor design provides a convenient method of describing the device, debugging the program and, with many of the devices, performing simulations before committing to a production run. The system punches program outputs to paper tape from which hardware is produced.

The network may be accessed by a terminal and telephone from virtually any geographical location. In addition, the company provides service backup at both the local and corporate levels, and can obtain backup from the manufacturer if the designer requires it.

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Plan to be there when COMPUTER EXPO 77 comes to a city near you.

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In addition to Computer Expo, there are Computer Designer Forums in the five major US design centers. In San Francisco, Los Angeles, Chicago, New York and Boston, we'll also be conducting Designer Forums from 9AM to 1PM each Caravan day. Leading local designers and independent experts will present tutorials and workshops on these important topics:

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Central Processor Contains LSI-11 Microcomputer Module

A powerful central processor, based on the DEC LSI-11 microcomputer module, includes an LSI-11 double-sized backplane and PDP-11 Unibus™ adapter port. The GCR 11/03 from General Robotics Corp, 57 N Main St, Hartford, WI 53027 is therefore a direct replacement for LSI-11, PDP 11/03, /04, or /05 minicomputers.

Housed in a 5¼" chassis suitable for rackmount or tabletop operation, the standard unit has extended instruction set and floating point arithmetic. Other features include 20K words of RAM, extended memory addressing to 512K words, serial I/O module with switch selectable data rates, pseudo switch register accessible with software or ODT, Unibus peripheral port which accepts a standard Unibus cable, and eight additional dual height module slots.

Circle 182 on Inquiry Card

Microprocessor Cross-Assemblers Run On PDP-8 Minicomputers

Designed for Digital Equipment Corp's PDP-8 minicomputers, the series of 2-pass microprocessor cross-assemblers run in 8K of memory under the OS/8 operating system. According to Sierra Digital Systems, 1440 Westfield Ave, Reno, NV 89509, the group, called the X8 series ("Cross-8"), fills a software gap experienced by many PDP-8 users involved with microprocessor program development.

Features include a Universal Assembler Format of common assembler directives and techniques. Pseudo-ops and run-time options provide for conditional assembly and extensive listing control. Arithmetic and logical operators are supported in complete operand expression evaluation. Generated object code can be output in the microprocessor's standard load format or BNPF format for ROM generation. Distributed in PDP-8 binary format on paper tape, DECtape, or DEC floppy diskette, the cross-assemblers are available for the 6502, 6800, and 8080 microprocessors. Assemblers for the 2650 and F8 microprocessors are also near completion.

Circle 183 on Inquiry Card

Memory Provides Nonvolatile Operation for 6800 Microprocessor

Designed for the Motorola EXORciser® and MEC 6800 evaluation module, the MM6800 8K x 8 RAM core memory system eliminates data loss upon power removal—a characteristic of semiconductor memories in the microprocessor development system. Memory boards plug directly into existing EXORciser connectors, ensuring compatibility with existing processor boards.

Measuring 5.75 x 9.75 x 1.0", the system allows both RAM and p/ROM functions to be performed. The module, available from Micro Memory, Inc, 9438 Irondale Ave, Chatsworth, CA 91311, contains timing, control, decode, drive circuits, address registers, and data registers. It has onboard memory expansion in 4K increments up to 64K words. Data access time is 350 ns and cycle time is 1.0 μs. A power status signal is available as a power interrupt vector or power reset signal.

Circle 184 on Inquiry Card

FORTRAN Compiler Is Available for 6500 Microprocessor

The FORTRAN cross-compiler for Synertek/MOS Technology 6500 microcomputers accepts an enhanced version of the FORTRAN IV language and produces as output a well-annotated assembly language program. This is then processed by the company's 6500 cross-assembler to produce an object file in the KIM board, 6500 simulator, Synertek ROM, or various p/ROM programmer formats.

The language contains many data types, and varying length character strings. Specification statements include Common, Data Dimension, Equivalence, Function, and Subroutine. For flow of control the language has the arithmetic IF, logical IF, DO, GOTO, STOP, PAUSE, RETURN, and END statements. Expressions are general; mixed mode assignments and expressions are not allowed, but built-in functions IFIX and FLOAT provide type conversions. Compiler is available from Zeno Systems, Inc, 2210 3rd St, Santa Monica, CA 90405, for a one-time licensing fee of $4000.

Circle 185 on Inquiry Card

Microcomputer Language Allows More Powerful, Easier Programming

A compact powerful system, SLAM (Symbolic Language Adapted for Microcomputers) operates on Intel's Intellec 8/MOD 80 and MDS Microcomputer Systems. Developed by PennMicro, PO Box 5073, Lancaster, PA 17604, the system is claimed to make these microcomputers more powerful and easier to program by providing a text editor and high level language interpreter in a package which occupies less than 3200 bytes of memory.

A program is created using the text editor, and is then run immediately using only the microcomputer and a teletypewriter. This eliminates paper tape operations without the cost of a diskette. Similar to BASIC, the high level language is faster and easier to use for programming microcomputers than assembly language, which is usually used.

SLAM uses 16-bit signed decimal numbers, has powerful I/O and bit masking operations, as well as a variety of conditional and subroutine commands, and is totally symbolic. Neither registers nor memory addresses have to be assigned. An optional feature permits program development while the microcomputer is operating other real-time systems. Supplied on paper tape, SLAM is loaded and entered using the Intel System Monitor.

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Logic Designers

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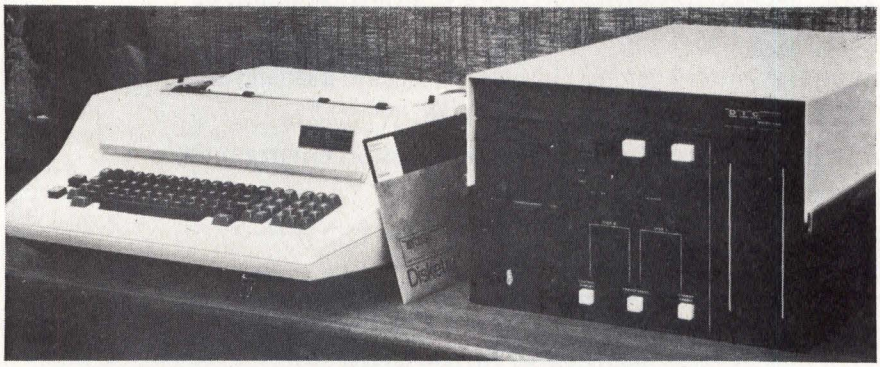
Data General

Standalone Micro File Computer Systems Offer Dual or Quad Discs

Micro File MKII and MKIV standalone microprocessor computer systems have been introduced by Data Terminals and Communications, 1190 Dell Ave, Campbell, CA 95008. MKII has a dual, second generation, flexible disc with over 600,000 characters of storage. There are two RS-232 serial I/O ports: one handles a data terminal, and the other a data communications line (both at independent speeds from 110 to 9600 baud). User memory is 8K bytes of RAM (field programmable to 56K bytes). Otherwise identical to the MKII, the MKIV has two dual drives (four discs), expanding online capacity to 1.2M bytes.

Comprehensive software operating system provides sophisticated file management and utilities for data transmission/reception. Devices are programmable at three levels—machine language, assembler, and extended BASIC (the latter two are software options). A powerful text editor and automatic letter writer are standard packages.

Circle 187 on Inquiry Card



Spark Timing System for Automobiles Uses Microcomputer

Featuring the first use of a microcomputer in a production automobile, the system is an onboard digital computer developed by General Motor's Oldsmobile and Delco-Remy division for the MISAR (Microprocessed Sensing and Automatic Regulation) electronic spark timing system. The MISAR system consists of a control unit containing the microprocessor and several sensors located on the engine. The system improves fuel economy by signaling Delco-Remy's electronic High Energy Ignition System's distributor to fire the spark plug at the right instant.

Two LSI chips containing over 20K transistors and electronic elements comprise the 10-bit microcomputer. One chip—the CPU—contains the I/O ports, scratchpad and I/O registers, and A-D conversion circuitry. The other circuit is a 10,240-bit ROM containing data curves in 3-dimensional format and preprogrammed instructions which control the microcomputer's functions.

Specialized instructions built into the CPU give the microcomputer a table look-up and interpolation function to locate data inputs between stored points on curves, reducing ROM requirements. During operation, all sensed inputs are considered to solve the complex spark firing equation many times per second. This processed technology—p-MOS—has high immunity to noise and environmental conditions in automotive operations.

Rockwell International, Microelectronic Device Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803, is producing the microcomputer as a subassembly under an agreement with GM. The complete system which is to be standard on 1977 Oldsmobile Toronado cars, is built and installed by GM. □

Circle 188 on Inquiry Card

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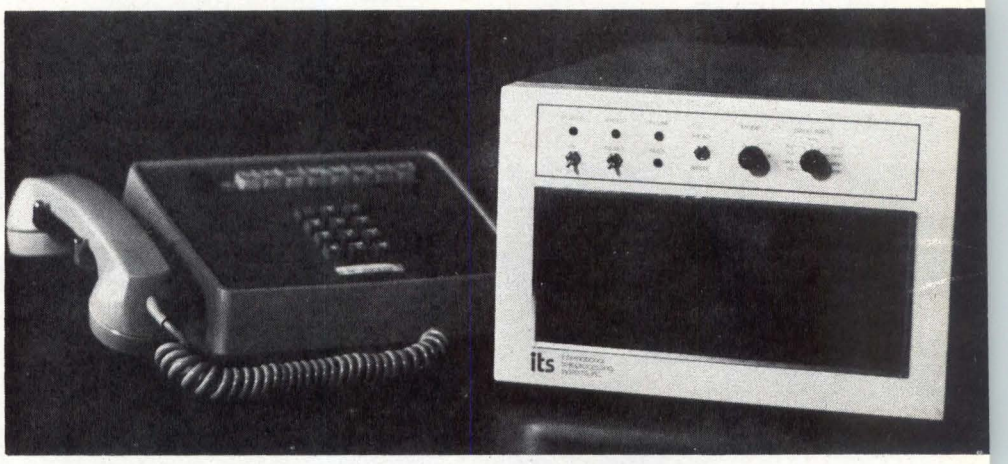
PRODUCT FEATURE

Intelligent Data Storage Device Programmable Communication



Data collection, text editing, and programmable communications with other devices are prime capabilities of the S-76 communications and memory system. The standalone, intelligent data storage device, introduced by International Teleprocessing Systems, Inc, is a complete microcomputer system with 8080A microprocessor, single IBM-compatible floppy disc drive, disc operating system, and dual RS-232 ports. It is structured for ASCII communications; dual ports permit simultaneous connection to a local terminal and to a modem, remote computer, or other communications device.

A disc operating system (DOS) with its simplicity for the operator is the key to the communications system. Directory information is maintained for selection of any one of 150 files in each diskette. Any file can contain up to 100 pages of text. The DOS completely controls the file storage and access mechanism.

Microcomputer programmability permits adaptation to any terminal command structure or special configuration. It also eases upgrading or continues expansion to suit additional configuration requirements.

Operating Features

Standard system memory is 8K bytes of RAM and 1K bytes of ROM. Up to 16K bytes RAM and 8K bytes ROM are optional. Disc storage with standard single-density drive is 256K bytes; optional two disc storage provides 500K bytes single and 1.2M bytes double density.

Data can be entered, deleted, added, replaced, or inserted at any line of the text through a text editor. Lines or characters can be inserted, deleted, or replaced instantly.

An asynchronous ASCII printer or CRT terminal, as well as external data set or coupler, can be attached without either hardware or software alteration. Any of nine communication rates can be operator-selected over a 110- to 9600-baud range (each port independently).

DOS organization allows a user to access disc data either sequentially or randomly from the console or through program interfacing. A sector allocation/deallocation technique assures proper use of disc space. Up to four positions can be accommodated.

All disc files are referenced by as many as eight character names and three character extensions. Five types of files can be stored: *text*, stores ASCII information in variable record lengths, with data packed by a space compression technique such that all available space in any given sector is utilized; *binary*, represents the machine code or program to be loaded and is generated any time an assembly is performed on a file; *physical*, permits random-accessing of binary or ASCII data by logical file and record numbers; *basic*, stores data created by the BASIC-PLUS compiler program when a BASIC-PLUS program is compiled; and *DOS command*, binary files which are loaded and executed immediately when called.

Selectable choices of parity are odd, even, all, or none. Communication may be full or half duplex. All 128 ASCII characters or all 256 binary code characters can be accommodated.

Optional features include dual disc drive configuration, unattended operation/automatic answer back and disconnect, paper tape reader/punch emulation, cassette emulation, parallel I/O interface, additional ports, 20- to 60-mA current loop interface, and memory expansion. Other options include rack mounting, cables, and special command structures.

Functions as System

Specifications

Access times for the floppy disc drive are 83 ms avg latency, and 10 ms avg track to track and settling, both single and double densities. Transfer rates are 31.3K bytes/s single and 62.6K bytes/s double density. Formats are 26 x 128 bytes/sector single and 32 x 256 bytes/sector double density.

Temperature range is 50 to 100°F (10 to 38°C) at 20 to 80% relative humidity, noncondensing. Power requirements are 115/220 Vac, 1ϕ, 50 to 60 Hz, and 4.5 A. Dimensions are 7 x 12.25 x 22″ single drive and 12.5 x 12.25 x 22″ double drive. Weights are 32 and 46 lb, respectively.

Price and Delivery

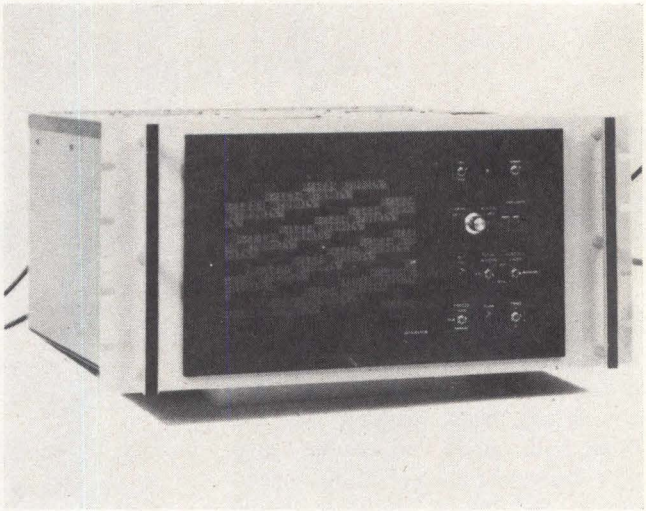
Unit prices for the S-76 communications and memory system are $2980 in lots of 1 to 9, $2757 for 10 to 24, and lower in larger lots for a single density system with one floppy disc, two RS-232 ports, disc operating system software, text editor, firmware, 8K bytes RAM, and communications software. Prices for options include $250 for the 8080A assembler; $300 extra for double density drive; $35 for a cable; $275, $475, and $950 for 4K, 8K, and 16K bytes of memory, respectively. A second drive costs $900 single density, $1200 double density. Delivery of systems is quoted as 45 days ARO. International Teleprocessing Systems, Inc, 398 Martin Ave, Santa Clara, CA 95050. Tel: (408) 244-5511.

For additional information circle 199 on inquiry card.

PRODUCTS

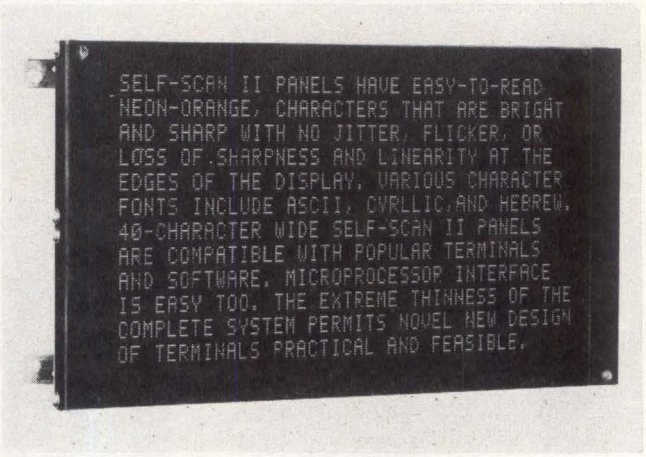
Programmable CRT Monitor Displays Data Communications Transmissions

In combination with Intershake[R] I or II, the Interview[TM] data monitor displays all data traffic or only specific traffic from a selected terminal or location. The unit is designed to expand capabilities by allowing visual observation of up to 1024 hex or octal characters in any code for all characters or control characters only. This provides fast isolation of hardware or software faults in data communications systems. The monitor operates in full or half duplex at rates up to 56K bits/s, and is compatible with any protocol including BISYNC and SDLC. In full duplex, both data streams are displayed on alternate lines in their proper timing relationship. Operating on 115-V/60-Hz or 230-V/50-Hz power, switch selectable, monitor is available in rackmount or portable configuration. It connects directly to the auxiliary interface of Intershake DTM-1 or -2; a video output port connects it to slave CRTs for permanent installations. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.
Circle 200 on Inquiry Card



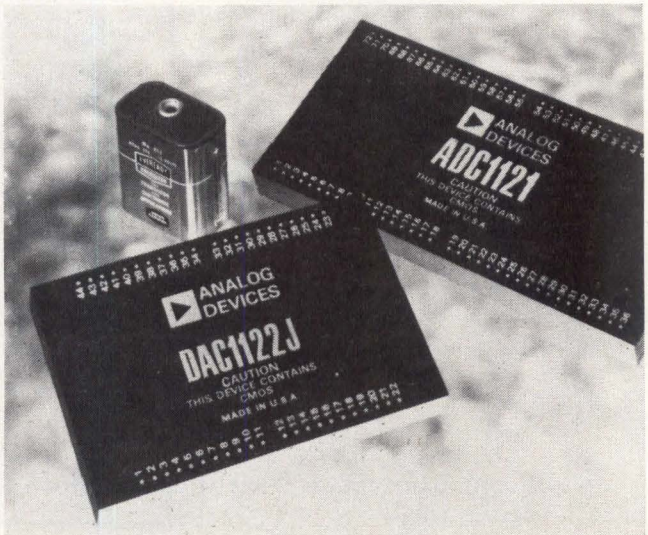
Gas Plasma Data Terminal Panel Displays Operate at Lower Voltages

Capable of being packaged as a complete display subsystem and requiring lower voltages than CRTs, model SII 1240-PD2 contains 480 alphanumeric characters in 12 lines of 40 chars each. The 0.26 x 0.14" neon orange chars against a dark, high contrast background are arranged in a 5 x 7 dot matrix, providing low reader fatigue, high visibility, uniformity, and intensity without edge distortion. Display panel area measures 11 x 6", and is 1¼" deep including drive electronics. Complete with panel driver board which connects through a 26-pin connector, display requires 5- and −12-V input, and −250-V low current supply obtainable from a dc-dc converter. All 64 ASCII chars and over 100 chars and symbolic fonts including Cyrillic, Hebrew, and Katakana can be displayed. Special chars can be produced and displayed using available or customer-developed char generators. **Burroughs Corp, Electronic Components Div,** PO Box 1226, Plainfield, NJ 07061.
Circle 201 on Inquiry Card



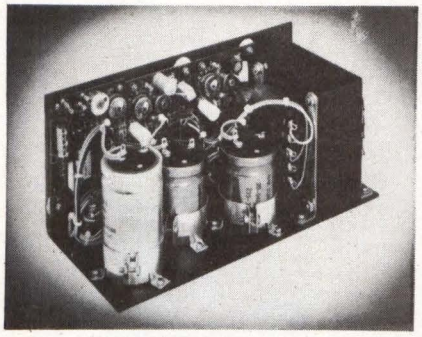
12-Bit ADCs and DACs Consume Low Power And Offer Price-Performance Edge

Claimed to have the industry's lowest power consumptions, the 12-bit DAC and ADC require only 8.5 mW and 300 μW between conversions respectively. Both are CMOS and TTL compatible over the 5- and 15-Vdc operating range. DAC1122 uses internal or variable external reference for fixed or multiplying modes. Digital inputs accept true and complement codes for binary and offset binary coding. Current or voltage outputs are short-circuit protected. With two versions of speed and drift, DAC1122J has 20-μs settling time, 30 ppm/°C gain, and 5 ppm/°C differential nonlinearity tempcos; and DAC1122K has 10-μs settling time, 15 ppm/°C gain, and 3 ppm/°C tempcos. Both measure 3 x 2 x 0.42". ADC1121 requires <6 μJ with power from a single 12- and 15-V source. Features include a ±¼ LSB power supply sensitivity, 59-μs max conversion time, and ±0.01% relative accuracy. Accepting analog inputs in the 0 to 5, 0 to 10, ±5, and ±10-V range, the 4 x 2 x 0.4" unit produces parallel and serial NRZ digital outputs. **Analog Devices,** PO Box 280, Rt 1 Industrial Pk, Norwood, MA 02062.
Circle 202 on Inquiry Card



PRODUCTS

PERIPHERAL EQUIPMENT POWER SUPPLIES



Multiple output, regulated dc supplies specifically designed for use in floppy disc and other peripheral memory systems, SMS series consists of six basic models. With variations in power handling capabilities, units provide voltage combinations of 5, 12, 15, and 24 Vdc regulated to within ±0.1% for line and load, with typ ripple of 50 mV. 24-Vdc outputs absorb 500 ms surge currents of up to 200% over ratings. Universal inputs of 115/230 Vac (±10%) are fully rated from 47 to 440 Hz. **Standard Power, Inc,** 1400 S Village Way, Santa Ana, CA 92705.

Circle 203 on Inquiry Card

DUAL SWITCHING POWER SUPPLY

Dual-output, regulated supply produces two 375-W outputs and a total of up to 750-W power in a 5.1 x 6.5 x 13.50″ package. First and second primary voltages of the MM-520 can be any combination of 2 V at 75 A, 12 V at 31 A, 15 V at 25 A, 18 V at 21 A, and 24 V at 15 A. The unit is up to 80% efficient and features 1% pk-pk or 50-mV pk-pk ripple and noise on output, line regulation of 0.4% over the entire input range, and load regulation of 0.4% from no-load to full load. Response time is 200 μs. **LH Research, Inc,** 1821 Langley Ave, Irvine, CA 92714.

Circle 204 on Inquiry Card

160-CHAR/S MATRIX PRINTER

Optimizing bidirectional printing to achieve throughput speeds of >200 lines/min., the model T-1602 uses a microprocessor to compute the shortest distance to the next print position, printing left to right and right to left, slewing at 8.5 in./s, and moving the print head at an accelerated rate when not printing. Std features include 7 x 7 matrix font, double width capability, u/lc, forms length selection, and self-test. The unit prints an original plus four carbon copies and handles forms from 4 to 15″ wide. **Tally Corp,** 8301 S 180th St, Kent, WA 98031.

Circle 205 on Inquiry Card

MINI LINE PRINTER

A lightweight matrix line printer which adds low cost desktop printing capabilities to the company's System 2200 computers, model 2251 provides an alternative to conventional thermal printers which use heat-sensitized paper and have high energy requirements. Weighing only 8 lb, the unit prints a 40-col char line at 110 char/s on a 3¾″ wide x 220′ paper roll. The full 96-char alphanumeric type set can be printed in blue or red by selecting either color or programming in color changes. **Wang Laboratories, Inc,** 836 North St, Tewksbury, MA 01876.

Circle 206 on Inquiry Card

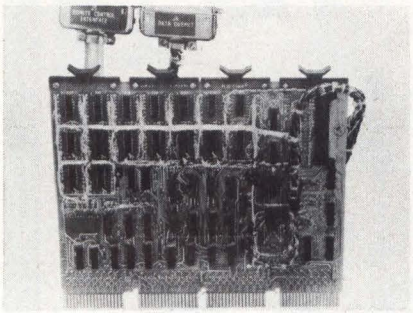
EDGE CONNECTOR SWITCHING MODULE

For packaging with nonlatching or dual-coil magnetic latching relays and designed to function as a low power switching module, the PC board has isolated contacts, positive coil terminal for each of five relays, and one negative coil terminal common to all. All terminate at the 22 double-sided edge-connector fingers. Operating mode can be either selective control of each relay with dpdt or 3pdt output or simultaneous control. Coils are rated at 5, 6, 12, or 24 Vdc with two or three contact blades. **Printact Relay Div, Executone, Inc,** PO Box 1430, Long Island City, NY 11101.

Circle 207 on Inquiry Card

PRODUCTS

RECORDER AND COMPUTER INTERFACE BOARD



The PTR/PDP-11 computer interface module accommodates compatible operation between the company's pulse and transient recorder and Digital Equipment Corp's PDP-11 minicomputers. A complete hardware interface built on a DEC foundation module, the unit plugs into the computer's small peripheral controller slot, providing I/O transfer of data and system control. Input mode selection and control changes are accomplished by addressing the interface module. **American Electronic Laboratories, Inc,** PO Box 552, Lansdale, PA 19446.

Circle 208 on Inquiry Card

INTELLIGENT DUAL FLEXIBLE DISC TERMINAL

The 9600-baud binary synchronous communications capability on model 350 terminal, is available in conjunction with the company's IBM 2770 and 3780 RJE package, which features IBM space compression and decompression, and record blocking. In sample tests, 1000 120-char records were run at 4800 and 9600 baud on a 600-line/min. printer, achieving 86% greater throughput. The unit also communicates using asynchronous protocols from 110 to 1200 baud. **Sycor Inc,** 100 Phoenix Dr, Ann Arbor, MI 48104.

Circle 209 on Inquiry Card

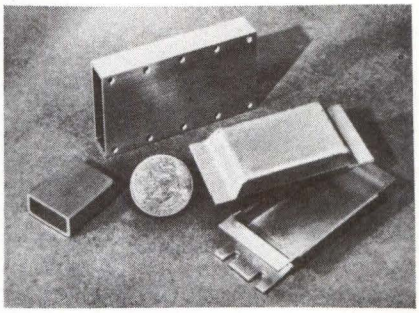
SMALL INCANDESCENT READOUT

A directly viewed 7-segment Pinlite[R] display the 03-15 has a 3/16" high char in a 0.305 x 0.225 x 0.312" package. Patented corner-crossover filament arrangement eliminates open corners for greater char definition in high ambient light conditions. Displays are easily filtered to a wide range of colors, have a 120-deg viewing angle, and stand up to rugged environments. The 1.5-V readout draws 8 mA/segment, and emits 800-ft-lm light output. Accessories include panel mount and combined decoder driver/connectors. **Refac Electronics Corp,** PO Box 809, Winsted, CT 06098.

Circle 210 on Inquiry Card

PRODUCTS

MAGNETIC BUBBLE MEMORY SHIELDS



Protecting highly magnetic-sensitive bubble memory devices from external field, these annealed magnetic shields can be made from two L-shaped pieces of 0.062" shielding material, heliarc welded on opposite corners, with parallelism tolerance of ±0.001", and flatness tolerance of ±0.003"; or constructed by shearing, forming, and heliarc welding on two edges (same tolerances). Another shield assembly consists of two drawn can shells with the two half-shells assembled by automatic welding. **Amuneal Manufacturing Corp,** 4737 Darrah St, Philadelphia, PA 19124.
Circle 211 on Inquiry Card

MINIATURE SOLID-STATE RELAY

Series 501 occupy <0.75 cu in., and provide load ratings of 115 V, 60 Hz. Typ control voltage is 5 Vdc using only 7 mA. Devices are compatible with TTL, DTL, and CMOS logic circuits, are PC board mounted, and require no heat sink. Circuit design desensitizes the unit to input transients. Typ turn-on time is 8 ms. Epoxy encapsulation protects the relay in areas subject to high humidity, condensation, and dust. **North American Philips Controls Corp,** Husky Pk, Frederick, MD 21701.
Circle 212 on Inquiry Card

CODED OUTPUT ROTARY SWITCH

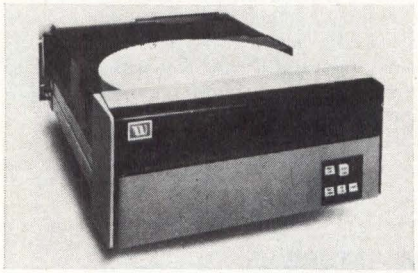
Rotocode[R] combines rotary switch characteristics with coded electrical output of a thumbwheel switch. The switch's rotating "D" shaft drives any number of PC discs, whose concentric traces rotate past stationary contact wipers of precious metal. Both sides of the disc shaped PC board can be used, minimizing behind-panel space. Providing up to 50 positions of output, the device can be PC board or panel mounted. Operating torque is 5 to 25 in.-oz, and life is 1 million detent operations. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.
Circle 213 on Inquiry Card

PRODUCTS

BI-COLORED LED LAMPS

Providing independent red and green emission from the same T-1¾ type package, the lamps contain two integral GaP chips, one green and one red, that operate independently. Devices are IC compatible and feature high luminous intensity, low power consumption, and solid-state life, reliability, and resistance to shock and vibration. Packages are clear diffused dome lens (521-9242), clear nondiffused dome lens (-9244) incorporating a fresnel ring pattern, and clear nondiffused cylindrical lens (-9245) with a lenticular pattern and longitudinal fluting. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 214 on Inquiry Card

HIGH PERFORMANCE DISC DRIVES



Cartridge disc drives, which store 5M, 10M, or 20M bytes of data in the space usually required for 2.5M bytes, are available as Super T, a top load unit which uses an IBM 5540 type cartridge in combination with a fixed disc. It offers data densities to 4400 bits/in. with up to 200 tracks/in. for total capacity of 20M bytes/drive, and transfers at 5M bytes/s with 2400-rpm rotational speed. Super F, a front load unit, uses IBM 2315 type cartridges and provides up to 2200 bits/in., 10M bytes capacity, with transfer rates to 2500K bytes/s. **Wangco Inc,** 5404 Jandy Pl, Los Angeles, CA 90066.
Circle 215 on Inquiry Card

ADD-ON SEMICONDUCTOR MEMORY

The ADD-IN 11 for DEC PDP-11 computers uses dynamic MOS technology and is completely plug-in compatible with PDP-11 models 04, 05, 10, 34, 35, 40, 45, 50, and 55. Offered in 16K x 18-bit and 16K x 16-bit configurations, the memory is contained on a single PC board that plugs into the computer chassis. Capacity may be increased in 16K increments up to 128K words. Operation may be interleaved on 4K boundaries. **Fabri-Tek Inc,** 5901 County Rd 18, Minneapolis, MN 55436.
Circle 216 on Inquiry Card

HIGH RESOLUTION COLOR VIDEO DISPLAY MONITORS

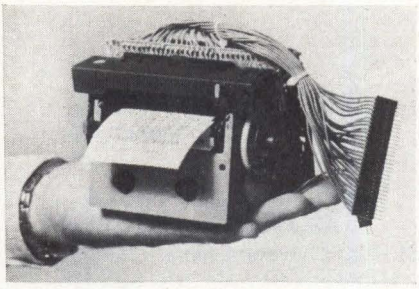
GM-613 and -619, for use in raster scan graphic and imagery display systems, feature resolution of 1800 triads/scan line. Their static convergence system results in ratings of 2000-h mean time between convergence adjustments. RGB input monitors feature increased color purity and reliability, plug-in PC replacement modules with minimal internal adjustments, and video output conforming to EIA Standard RS-170. Units are available with 13 and 19″ diag CRTs, in rack mount or table top models. **Ramtek Corp,** 585 North Mary Ave, Sunnyvale, CA 94086.
Circle 217 on Inquiry Card

SOLID-STATE UP COUNTER

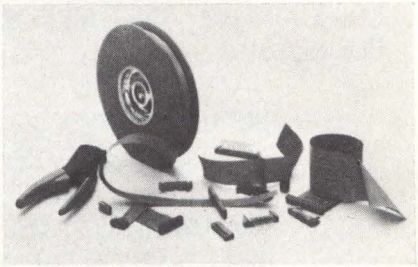
Counting, totaling, or accumulating, and displaying up to seven decades of count information from any signal input source up to 2 MHz, the unit's CMOS circuitry provides a worst case power consumption of 300 mW with 4-V supply; with the display off consumption is 560 μW max. Six front panel control switches provide on/off, preset, input block, reset, store, and display off. Display off mode allows the display only to be turned off with the rest of the counter operating normally. Power requirements are 3 to 6 Vdc. **Counterscan Systems,** PO Box 536, E Hwy 6, Sutton, NB 68979.
Circle 218 on Inquiry Card

NUMERIC PRINTHEADS

A 21-col printhead for instrumentation applications incorporates a pressure printing principle which operates with little noise. Two color printing is achieved using an ink ribbon cassette which allows no-mess ribbon replacement. Devices can be operated with a 100% duty cycle at a print rate of 3 lines/s. Life is 5 million printed lines. Heads can be mounted so that paper exits from top or front, allowing flexible packaging. Individual char wheels in each column allow flexible printing format. **Master Digital Corp,** 1308-F Logan Ave, Costa Mesa, CA 92626.
Circle 219 on Inquiry Card



FLAT CABLE, PLUGS, AND HEADERS



Featuring symmetrical contour on top and bottom for plug termination in either direction, cable is available in 14-, 16-, 20-, 26-, 40-, and 50-conductor sizes, all on 0.050″ center spacing, with every fifth conductor color-coded for fast identification. Plugs have 4-point, insulation-piercing contacts. Male plugs come in 14- and 16-pin sizes, female plugs in 20-, 26-, 40-, and 50-contact sizes. Corresponding headers are provided in straight-through and right-angle configurations for both PC and wire-wrap. **Augat Inc,** 33 Perry Ave, PO Box 779, Attleboro, MA 02703.
Circle 220 on Inquiry Card

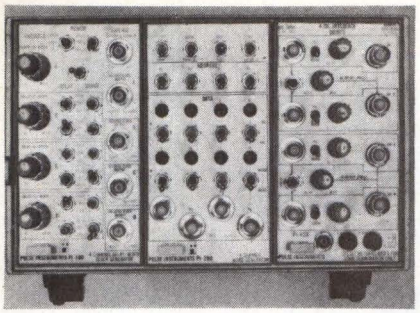
COLOR 7-SEGMENT DISPLAYS

In high efficiency red (5082-7610), yellow (-7620), and green (-7630), 0.3″ (7.62 mm) displays are available as common anode with left-hand decimal, common anode with right-hand decimal, common cathode with right-hand decimal, and ±1 universal overflow with right-hand decimal. They provide wide, evenly lighted segments, wide viewing angle, and matching body color for contrast enhancement, and are designed for low current multiplex operation—as low as 3 mA/segment for red devices. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.
Circle 221 on Inquiry Card

LOW POWER DATA ACQUSITION MODULE

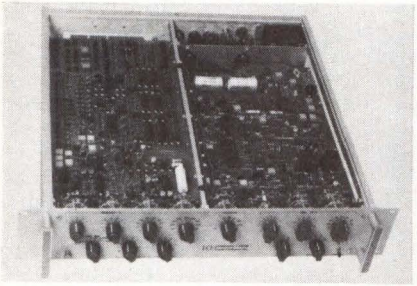
Designed to be pin compatible with the company's DATAX II series, the DT57C01 consumes only 1½ W of power and offers 35-kHz throughput. It provides 12-bit resolution, ±½ LSB linearity, ±0.03% system accuracy, single-ended or differential input configuration, and ±25 ppm/°C tempco. The module contains a 16-channel multiplexer, buffer amp, sample/hold amp, 12-bit ADC, and timing and control logic including 3-state CMOS output data lines for direct connection to microcomputer buses. **Data Translation Inc,** 23 Strathmore Rd, Natick, MA 01760.
Circle 222 on Inquiry Card

OSCILLOSCOPE PLUG-IN UNITS



For use with the Tektronix TM-500 series, the 4-channel PI-100 50-MHz delay/width clock generator; -200, 4-channel x 32 bit 50-MHz word generator; and -400 5-V interface driver with ±5-V offset form compact expandable multichannel signal source systems. -100 is equivalent to timing and control portions of four synchronous pulse generators packaged in one unit; -200 is driven by the companion -100. The -400 functions standalone or as power stage for the -100 and -200. **Pulse Instruments Co,** PO Box 1655, San Pedro, CA 90733.
Circle 223 on Inquiry Card

PROGRAMMABLE FUNCTION GENERATOR

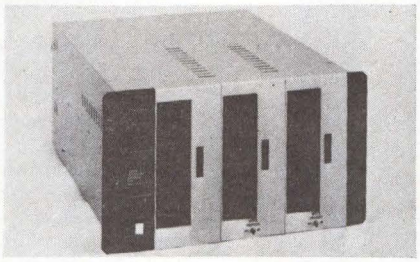


Model 5500AR provides sine, square, triangle, pulse, and sawtooth waveforms over a frequency range of 0.0001 Hz to 5 MHz, and may be triggered or gated or run in the continuous mode. All functions may be remotely controlled. At a main output of 30 V pk-pk (open circuit), the positive waveform duration can be programmed independently of its negative duration; therefore, an additional pulse and sawtooth wave is provided when used in square wave and triangle mode. High speed FET switches give switching time of 100 μs typ. **Krohn-Hite Corp,** Bodwell St, Avon Industrial Pk, Avon, MA 02322.
Circle 224 on Inquiry Card

4-SPEED SWITCHABLE SHORT HAUL MODEM

For economic short haul transmission of digital data over communication lines, the 24/48/72/96 operates at either 2400, 4800, 7200, or 9600 bits/s. Intended for half- or full-duplex operation over unloaded 4-wire, twisted pair lines, the modem employs encoded frequency shift-keyed modulation. The 4-speed selectable feature offers versatility in adapting to systems that incorporate modems of different fixed speeds and for upgrading to higher bit rates. **Penril Corp, Data Communications Div,** 5520 Randolph Rd, Rockville, MD 20852.
Circle 225 on Inquiry Card

MINI/MICROCOMPUTER DISKETTE MEMORY SYSTEM



Designed for use with DEC PDP-11, -8, and LSI-11, model 210 is both DEC instruction-set and IBM 3740 format compatible. Diskette formatting and write protect are std. An 8-bit bipolar microprocessor controls all data transfers, monitors read/write head positionings, and performs data error checks. Self-testing microcode verifies that the system is error-free. A digital phase-lock-loop data separation circuit enhances data reliability. **Data Systems Design, Inc,** 1122 University Ave, Berkeley, CA 94702.
Circle 226 on Inquiry Card

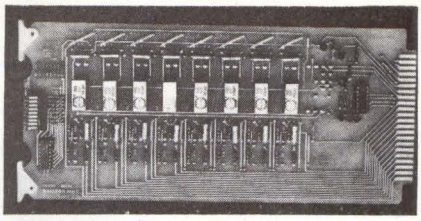
CODED ROTARY SWITCHES

The bidirectional rotating coded PC boards with fixed cantilever brush contacts used in the 3500 series output BCD, direct 7-segment units-and-tens display, and a number of special synthesizing codes. Modules have 18 to 50 detent positions; as many as seven modules can be ganged for multilayer operation from a single shaft. Switches are rated for 2.5 A, nonswitching, and 125 mA, switching, with a dielectric withstanding voltage of 250 Vdc min. Life expectancy is >25,000 bidirectional rotations at rated load. **AMP Inc,** Harrisburg, PA 17105.
Circle 227 on Inquiry Card

MINIATURE SOLID-STATE DIGITAL CONTROLS

Series 7902 Countroller combines LSI circuitry and fast-action presetting in a miniature panel-mount case to provide electronic predetermining up/down counters. For use where electromechanical preset counters cannot meet the fast count rate, frequent reset, and long life, and high reliability requirements, count-up models display actual production count at all times; down units provide continuous display of quantity remaining prior to output. Std units operate on 12 to 15 Vdc and count at speeds to 10 kHz. **Veeder-Root Co,** 70 Sargeant St, Hartford, CT 06102.
Circle 228 on Inquiry Card

MULTIREED RELAY DATA ACQUISITION SYSTEM

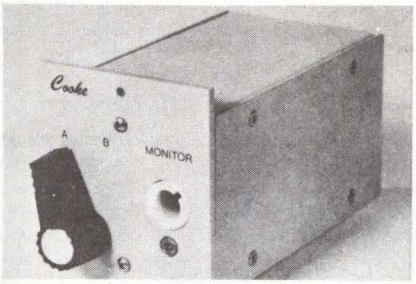


The H4200E measures outputs from temperature sensors and linear millivolt signals from signal conditioners and reads out directly in engineering units, using D2C-COT Multireed[R] relays. Systems scan up to 1000 input channels at 20 channels/s to display and record input signal values. Relays are used in a flying capacitor circuit configuration in the multiplexers. One relay is required per input channel with a typ system including from 200 to 600 channels. **Thermosen, Inc,** 375 Fairfield Ave, Stamford, CT 06904.
Circle 229 on Inquiry Card

SCALABLE ABSOLUTE ENCODERS

Suited to severe electrical and physical environments, units convert shaft input to BCD or binary information corresponding directly to shaft angle with an accuracy of ±1 part in 3600, and provide 3-, 4-, or 5-digit, 0.5" high LED display of angle. Zero point can be reset to any value via an available offset adjustment, and any output scale factor can be provided. Cable runs up to 1000 ft between transducers and electronics can be used. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.
Circle 230 on Inquiry Card

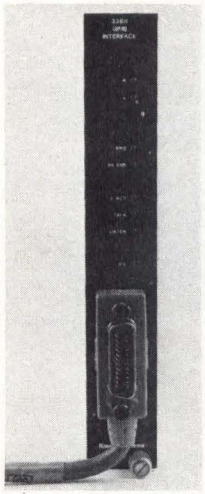
DATA COMMUNICATION FALLBACK SWITCHES



RS-232 A/B switches provide instant switching of the EIA RS-232 interface between two modems and a terminal or optionally between two terminals and a modem. All 24 active leads are switched and ground pin is hardwired through. Allowing data circuit reconfiguration to meet normal operational requirements, the unit handles all data speeds to 9600 bits/s. Optional Dyna-Patch[R] monitor/access jack permits noninterrupting access to the common lead of the switch. **Dynatech Laboratories, Inc, Cooke Engineering Div,** 900 Slaters Lane, Alexandria, VA 22314.
Circle 231 on Inquiry Card

PRODUCTS

GP INTERFACE BUS MODULE



Providing the interface between a CAMAC system and up to 14 other GPIB-interfaced instruments via std GPIB cables, model 3388 is a double-width CAMAC module which meets IEEE Standards 488 and 583 requirements. Module provides GPIB talker, listener, and controller functions; there is a max of one talker and up to 14 listeners at a time. Specs include 16 active signal lines—eight data, three data transfer control, and five bus management message lines. Message transfer scheme is byte-serial, bit-parallel asynchronous data transfer using interlocked 3-wire handshake technique. Data rate is 250K to 500K bytes/s typ over full transmission path. Address capability consists of 31 talk and 31 listen primary addresses, and 961 talk and 961 listen secondary (2-byte) addresses. **KineticSystems,** Maryknoll Dr, Lockport, IL 60441.

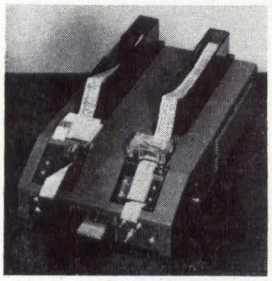
Circle 232 on Inquiry Card

FLOPPY DISC SYSTEM

This Micro-Disc System is a complete, high performance floppy disc storage system for use with the Intel 8080 or Zilog Z80 microcomputer systems. All hardware and software needed to turn on the computer and start loading or saving programs and accessing online data files are included. Disc unit is a compact version of the std Shugart floppy. Drive capacity is approximately 100K bytes/diskette. Measuring 6 x 3 x 8", the unit can be mounted inside the computer cabinet with specified cutout. Power supply requirements permit use of existing computer power supply. Optional cabinet and power supply are available. Controller is a single 5 x 10" PC card compatible with the S-100 (Altair/IMSAI) bus. It controls up to three drives, with or without interrupts. An onboard p/ROM contains power-on bootstrap software. **North Star Computers, Inc,** 2465 Fourth St, Berkeley, CA 94710.

Circle 233 on Inquiry Card

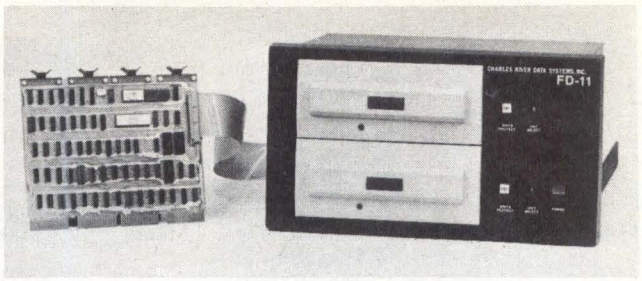
PAPER TAPE READER/PUNCH



Module for code duplication or conversion in data communications systems can be easily connected to a variety of equipment, including IBM Selectric[R] systems, terminals, mini and microcomputer systems, programmable calculators, and CRT displays. Although inherently an ASCII system, it accommodates any code. Programmable code translation from one format to another is achieved with a built-in p/ROM code converter, thereby making it possible to accept and convert any incoming code to Baudot, BCD, EBCDIC, or TTS. Several code translations are optionally available. Module duplicates incoming code or transposes codes at 50 chars/s (max punch speed). Editor option allows paper tape to be read or skipped by character, word, line, or paragraph. Unit is available as a reader only, punch only, or as a complete reader/punch module. **Tycom Systems Corp,** 26 Just Rd, Fairfield, NJ 07006.

Circle 234 on Inquiry Card

FLOPPY DISC ADD-ON



FD11 floppy disc system for the PDP-11 series is hardware, software, and media compatible with the DEC RX-11. Features include write protect switches, unit select switches, 6-ms track-to-track access, modular construction, single Unibus™ load for up to four drives, p/ROM self-diagnostic, and a bootstrap loader. Interface, formatter, p/ROM, and other PDP-11 interface logic are provided on a single "quad" card which plugs directly into one of the processor's small peripheral slots. Card is easily accessible for repair or replacement. Capacity is 77 tracks, 26 sectors/track, and 128 bytes/sector. Power requirements are 100 to 120 Vac at 2.0 A, 200 to 230 Vac at 1.0 A, 50 or 60 Hz ±0.5 Hz; 5 Vdc at 4.2 A. The disc uses an IBM 3740 format and IBM diskette (or equivalent) as storage medium. **Charles River Data Systems, Inc,** 235 Bear Hill Rd, Waltham, MA 02154.

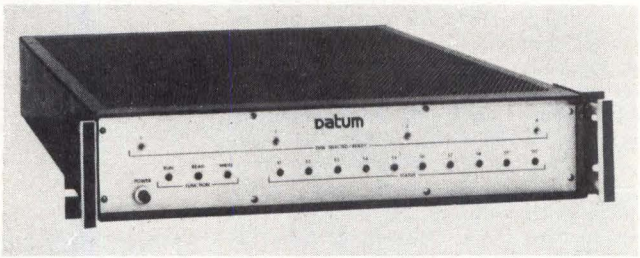
Circle 235 on Inquiry Card

DIGITAL TAPE CASSETTE RECORDING HEAD

A single track, dual-gap data recording head for cassette units, made of ceramic and ferrite material, extends head life up to three times over laminated alloy units. Model FCH-1 is for read-after-write applications in Philips-type data cassettes. Single-piece ferrite construction technique provides a harder material for longer life, and avoids collection of dirt and oxides for greater reliability and better performance. Resolution is 80% min (1600/800 bits/in.). Read output at 10-mA write current is 30 mV. Track width is 0.063" for the write head and 0.039" for the read head; gap-to-gap spacing is 0.150". Unit is for a tape speed of 20 in./s and packing density of 800 bits/in. **Information Magnetics Corp,** 5743 Thornwood Dr, Goleta, CA 93017.

Circle 236 on Inquiry Card

INTELLIGENT DISC CONTROLLER



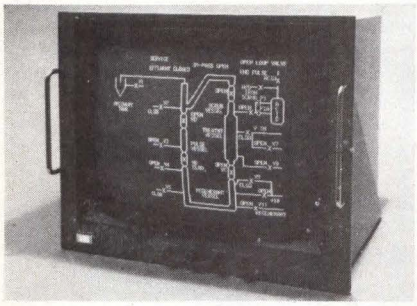
Using an 8-bit bipolar microprocessor to provide fast I/O operations while eliminating "bus hogging," the disc controller interfaces up to eight drives with a total 20M-byte capacity to any DEC PDP-11 minicomputer. Through firmware control, the processor handles seek, read, and write functions and checks, control and drive reset, write lock, and hardware poll. Software interface between the controller and the Unibus™ is provided by seven programmable hardware registers. Model 4091 (E) accommodates two daisy chains each with four single-density, 2.5M-byte drives, or four dual-density, 5M-byte discs in a double daisy-chain configuration. Controller also handles a "10-platter" drive. Unit can expand to accommodate drives with a storage capacity of 60M bytes max. Reprogramming of the controller firmware is optional. **Datum, Inc, Peripheral Products Div,** 1363 S State College Blvd, Anaheim, CA 92806.

Circle 237 on Inquiry Card

OPTO-SWITCHES

Base-mounting, high speed devices for CMOS and TTL circuits have integral slit-masks of 0.010" (STIN-165-1) or 0.005" (-165-2) widths. Mounting directly on stepper and dc-motor housings for encoding, speed control, indexing, and positioning, the switches' STIN-165 photon couples a GaAs IR LED to a phototransistor. A built-in series resistor allows the LED to be connected directly to the power supply. Resistor value is optional. **Sensor Technology,** 21012 Lassen St, Chatsworth, CA 91311.
Circle 238 on Inquiry Card

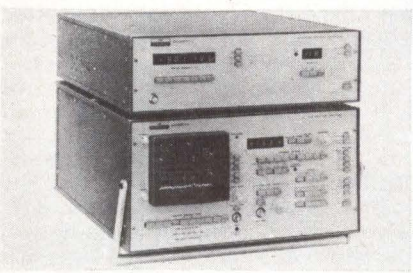
GRAPHIC PANEL CRT DISPLAY



Plain language annunciation of off-normal conditions is displayed in an understandable format by superimposing up to 64 16-char messages on a schematic of the process being monitored. Output relays to drive external audible signal devices are provided and operate in accordance with std ISA annunciation sequences. Erasable p/ROMs are programmed based on a sketch of the flow diagram showing descriptive legends and messages. **Metra Instruments, Inc,** 1161 San Antonio Rd, Mountain View, CA 94041.
Circle 239 on Inquiry Card

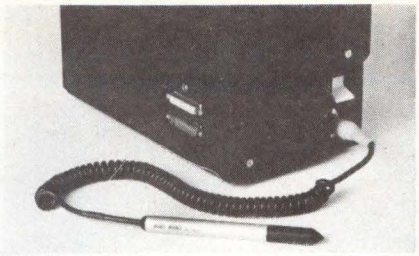
DIGITAL SPECTRUM TRANSLATOR

Operating with the company's 1510-03 real-time spectrum analyzer, model 1520 uses digital signal processing techniques to concentrate full resolution of the analyzer about a selectable point of interest, allowing resolution of two closely spaced discrete frequency components or extraction of high frequency signals buried in noise. Signals as close as 1 Hz can be resolved at 2 MHz. Nine frequency ranges from 25.6 Hz to 10.24 kHz are translatable in 1.0-Hz steps. **EMR-Telemetry,** PO Box 3041, Sarasota, FL 33578.



Circle 240 on Inquiry Card

BAR CODE READER

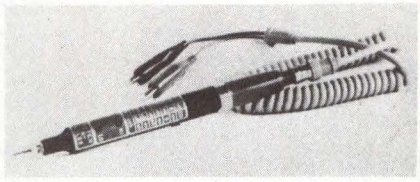


Dual connector feature of model 9110 allows parallel connection with any online RS-232-C equipped terminal; communication between terminal and computer is automatically transferred through the reader. Unit includes Ruby Wand[R] lightpen which scans variable length messages up to 32 data char, coded in the company's Code 39 or 11, bidirectionally at 3 to 25"/s. Communications interface is compatible with asynchronous bit-serial rates from 110 through 9600 baud. **Interface Mechanisms Inc,** 5503-232nd St SW, Mountlake Terrace, WA 98043.
Circle 241 on Inquiry Card

TOLL TEST SYSTEM

An integrated toll-test board, the 113A performs signaling and transmission quality tests on 2-, 4-, and 6-wire toll and interoffice trunks in central offices and local exchanges, allowing rapid isolation and identification of problems, simultaneous testing of two circuits while talking on a third, communication for coordination of trouble repair, and restoration of service by temporary bypass of marginal equipment. The unit features 19 keyset or ring-in/dial-out (POTS) lines. **ADC Telecommunications,** 4900 West 78th St, Minneapolis, MN 55435.
Circle 242 on Inquiry Card

PULSE LOGIC PROBE



Compatible with RTL, DTL, TTL, CMOS, MOS, and microprocessors using a 3.5- to 15-V power supply, the Catch-A-Pulse probe has automatically programmed thresholds for multilogic family operation. Automatic resetting memory allows single or multipulse detection, with no adjustments. Visual indication of logic levels is provided using LEDs to show Hi, Lo, bad level, or open circuit logic or pulses (60 ns). Shirt-pocket portable, the unit has a protective cap over tip, and removable coiled cord. **AVR Electronics,** PO Box 45167, San Diego, CA 92145.
Circle 243 on Inquiry Card

PRODUCTS

FORMATTED TAPE DRIVES

A series of tape drives incorporates a microformatter employing LSI/MSI and low power Schottky TTL electronic components. Claimed to have the first internal formatter that offers both NRZI and phase-encoded tape formats on a single circuit board, the drives offer file search capability, space record commands, and a crystal oscillator for timing. Up to three additional drives can be added in a master/slave configuration. Drives are available in models FT7000, FT8000, and FT9000. The 8 x 16" internal circuit board eliminates the usual separate formatter box and associated cabling. Formatter uses the same power supply as the tape transport. Drives are available for 12.5- to 75-in./s speeds and for 1600- or 800-bit/in. storage density. A simple switch change adapts the formatter to any tape speed from 12.5 to 75 in./s. **Pertec Computer Corp, Pertec Div,** 9600 Irondale Ave, Chatsworth, CA 91311.
Circle 244 on Inquiry Card

CARD PUNCH SERIAL INTERFACE UNIT

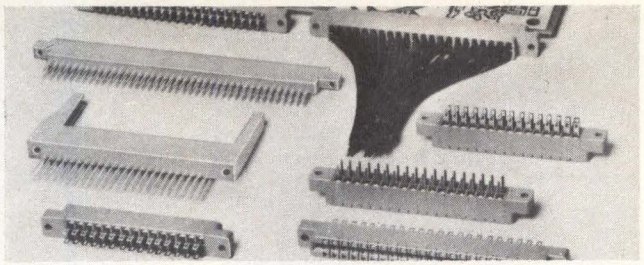
A serial ASCII RS-232-C (or 20-mA current loop) interface that may be installed in the deck portion of any 029 keypunch in 15 min., PC-29 offers a practical method of getting information which is generated in small computers into their larger counterparts. When operated through the PC-29, a keypunch automatically feeds cards from its input hopper, thereby allowing unattended punching of up to 500 cards. Data are transmitted to the interface as if it were a terminal. Upon receiving ASCII CR, it activates the skip function, positioning the next card to column one. The full u/lc ASCII-to-Hollerith conversion is implemented (in a 1702A p/ROM). Punching speed is from 18 to 20 chars/s with 0.25 to 1.25 s to register the next card. Specs include 32 to 115°F (0 to 46°C) operating temp, humidity to 95% noncondensing, and power requirements of 95 to 125 V, 60 Hz, 15 W. **Digital Laboratories,** 600 Pleasant St, Watertown, MA 02172.
Circle 245 on Inquiry Card

UNIVERSAL HIGH SPEED TAPE READER

Model 3722 is a continuous motion tape reader for playing back cassettes written on any of the company's 200, 300, or 500 series low power digital recorder or data logger. Std 300-ft Philips cassette may be read end to end in <3 min. providing parallel data transfers of 8, 12, or 16 bits. At constant speed the unit reads tapes at 20 in./s and rewinds at 100 in./s. User connections are TTL compatible. Std configuration uses complementary NRZI formatting at a data density of 615 bits/in.; it can be factory adjusted to read any density from 300 to 1200 bits/in. Word length may also be adjusted to 8, 12, or 16 bits. Both adjustments are optional as front panel controls. Features include front panel or remote start, stop, and rewind commands, and beginning- and end-of-tape sensing. **Memodyne Corp,** 385 Elliot St, Newton Upper Falls, MA 02164.

Circle 246 on Inquiry Card

CARD EDGE CONNECTORS



Available in 0.125" for crimp and wirewrap contacts and in 0.156" spacings for 0.062" thick PCBs, Card-Edge series connectors are made of gray, glass reinforced, thermoplastic polyester. Contact material is phosphor bronze, with std plating of 10 μin. of gold over nickel or non-noble tin lead. Contacts come in bifurcated or non-bifurcated design. Series 365 has crimp-type contacts on 0.156" centers for dual 15, dual 18, and dual 22 configurations. Series 366 has crimp-type contacts on 0.125" centers for dual 24, dual 36, and dual 40 configurations. The 0.156" x 0.200 grid discrete connectors are made with either wire hole tails for solder-to-round wire, or PC tails for solder-to-PC board. Discrete series offers sizes 40/80, 36/72, and 51/102 in dual configurations or 36, 40, and 51 for single readout applications. **Malco, a Microdot Co,** 12 Progress Dr, Montgomeryville, PA 18936.
Circle 247 on Inquiry Card

DATA ACQUISITION SYSTEM

A system that can log, trend, and alarm up to 1000 points, Trendscan 1000 includes a "Trend Mode" option where a portion of the data is displayed in a bar graph format. Most significant digits of the measurements are presented as numbers and the remaining digits are displayed as an analog bar graph, so that in profiling a group of points or following the trend of a single point any emerging pattern is readily apparent. A complete 20-point system housed in a single 7"-high chassis includes two 10-point input switching relay cards with isothermal connectors, basic point selection, and scanning controls. A clock provides system time or real time with controls for initiating periodic data logs. Ribbonless, nonimpact printer delivers the information in 21 alphanumeric columns at a speed of 6 lines/s. Up to six integral digital alarms are available. **Leeds & Northrup Co,** North Wales, PA 19454.
Circle 248 on Inquiry Card

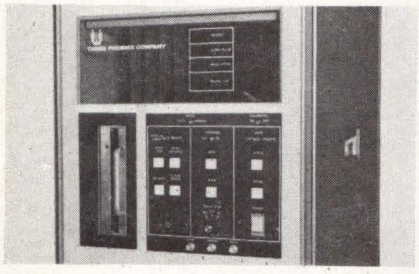
FAST 16- AND 32-BIT BINARY DIVIDERS

Basic model DD163 accepts a 16-bit dividend and 16-bit divisor and delivers an 18-bit quotient in 10 μs. For greater precision, model DD163-DP accepts a 32-bit dividend and a 16-bit divisor, delivering a 32-bit quotient. DD163 is TTL, yet power dissipation is <2.5 W. Self-clocked and functionally complete, it requires only an execute strobe to initiate operation; a data ready line signals when data are available from the output register. An overflow flag line signals if the number field is exceeded, eliminating programming error. Dividers are encapsulated in 3 x 4 x 0.675" modules; pins are DIL socket compatible or can be soldered directly onto PC boards. Divider and compatible fast math, trig function, and floating point units are also used to reduce repetitive routines or to expand speed and precision capabilities of micro or minicomputer-controlled systems. **Interface Engineering Inc,** 386 Lindelof Ave, Stoughton, MA 02072.
Circle 249 on Inquiry Card

8-CHANNEL COMMUNICATIONS MULTIPLEXER

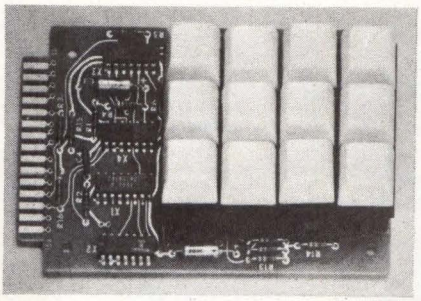
Multiport communications interface for Data General and Digital Controls minicomputers is available in either a 4- or 8-channel configuration. All necessary control logic is on a single 15-in. sq PC board which is inserted into the computer. System expansion capability from a minimum of four to a maximum of 64 lines is provided. Data format and baud rate are jumper-selectable on individual channels. **Custom Systems, Inc,** 2415 Annapolis Lane, Suite 170, Minneapolis, MN 55441.
Circle 250 on Inquiry Card

MPU-CONTROLLED DISC TESTER



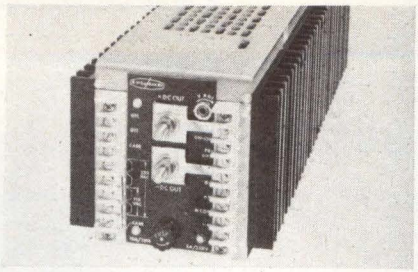
FD-33M uses an Intel 8080 to provide flexibility at reasonable cost. Tests offered include amplitude and resolution, as well as drop out, extra pulse, and modulation. Operators can choose any group of tests for automatic testing or can run the unit manually. Tests normally done on an acceptable quality level basis can be eliminated by switch selection for faster throughput or included for thorough quality analysis. Threshold levels can be set for calibration, and displayed on a 3-place LED. **Three Phoenix Co,** 10632 N 21st Ave, Phoenix, AZ 85029.
Circle 251 on Inquiry Card

MULTIFUNCTION INTERACTIVE KEYBOARD



Providing direct interaction with operating systems, facilitated with independently lighted keytops, keyboard output is fully compatible with microprocessor logic. A microprocessor can be programmed to energize keytop lights to modes such as light on, light off, and blinking light, each carrying a system instruction or operator verification action. The std size 3 x 4 keyboard features encoded output for calculator format and 2-key rollover, N-key lockout. **Brynlaw Products, Inc,** 1707 U.S. Hwy 130 S, Burlington, NJ 08016.
Circle 252 on Inquiry Card

SWITCHING POWER SUPPLY



Model 670, a compact single-output, 500-W supply, is rated 75% efficient, and uses MIL-grade components to assure reliability. Other features include strappable input 102 to 130, 198 to 256 Vac, crowbar overvoltage protection, overload protection, 30,000-h MTBF, remote sense, output on/off control, and parallel operation without additional circuitry. Measuring 5 x 4⅛ x 16", the unit weighs 18 lb, and produces over 1½ W/in.^{3} **Trio Laboratories, Inc,** 80 Dupont St, Plainview, NY 11803.
Circle 253 on Inquiry Card

ALPHANUMERIC LIQUID CRYSTAL DISPLAYS

Series of 16-segment alphanumerics with either light or dark digits on contrasting backgrounds can translate all Arabic numbers and the Roman, Greek, and Russian alphabets. Designed for single edge mounting, either with PC type connectors or conductive elastomers, char sizes range from 0.5" to 6" in height. Several may be grouped or mixed with legends to form annunciator panels. Units are available for both reflective and transmissive light displays. **UCE Inc,** 20 North Main, Norwalk, CT 06854.
Circle 254 on Inquiry Card

p/ROM PROGRAMMER WITH HEX KEYBOARD AND DISPLAY

Using hexadecimal displays to eliminate the need to translate address and/or data from binary and offering a convenient hexadecimal keyboard, model 601 displays master and copy p/ROM's address and data simultaneously. Using an 8-bit microprocessor the unit provides zero field test, automatically incremented address, straight duplication, duplication with change in section of copy p/ROM, verification, and step-by-step reading of p/ROM contents. Options include paper tape and teleprinter interface. **Technitrol, Inc,** 1952 E Allegheny Ave, Philadelphia, PA 19134.
Circle 255 on Inquiry Card

PRODUCTS

DISC DRIVES AND UPGRADING KIT

With a formatted storage capacity of 176M bytes for PDP-11s and 197M 7-bit ASCII chars for DECsystem-10 and -20, the RP06 has double track density. RP05 disc-pack drive is field-upgradable to an RP06 through use of a kit, which includes parts, installation, and an RP06 disc pack. Software support includes D and M forms of RSX-11, RSTS/E, IAS, and MUMPS. For PDP-11s, the RK06 drive accepts a dual-disc cartridge with storage capacity of 14M bytes. A top-loading unit, it also has a track-following servo system, with one of four disc surfaces dedicated to servo control and tracking information. Up to eight drives operate from a single controller, for a storage capacity of 111M bytes max. A nonremovable medium, the RK05F is a double-density version of the RK05 disc pack, with a storage capacity of 5M (for PDP-11) or 6M (for PDP-8) 8-bit bytes. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 256 on Inquiry Card

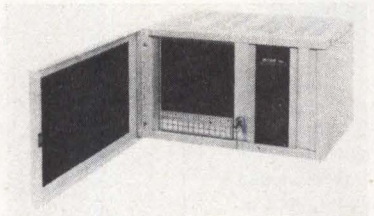
DATA ACQUISITION SYSTEM

The PCI system allows a mixture of up to 256 analog and numerous digital sources to be scanned and recorded on one to 14 tracks of any std instrumentation tape recorder. The recorded data can be reproduced in either analog or digital form or interfaced directly to a computer. Bandwidth of the source data determines scan rate, tape speed, and number of recorder channels required. Set-up is by simple user controls. Data may be recorded and reproduced at different tape speeds to provide time compression and expansion. Recording techniques permit S/N ratios of up to 96 dB. Tape recorder channels not needed for PCI recording may be used without restriction for normal analog recording. Modular construction provides max flexibility with economy. Data channels may be added as required. Portable units may be rackmounted. **Micro Consultants, Inc,** PO Box 10057, Palo Alto, CA 94303.

Circle 257 on Inquiry Card

DIGITAL DATA MULTIPLEXER

Designed for channelizing DDS links, the model 720 is a low-cost, all digital time-division multiplexer which makes it possible for DDS links operating at 4800, 9600, or 56K bits/s to be split into two or more channels, synchronous or asynchronous. Multiplexed channels may be dial-up or leased, full- or half-duplex; the multiplexing of half-duplex, polled multipoint circuits is also supported. System uptime is maximized with redundant common logic and power supplies. Monitoring and fault isolation on the DDS link is available from either end. Multiplexing technique is bit-interleaved. Channel interfaces are EIA RS-232-C, serial asynchronous, and 20 or 62.5 mA neutral, current loop, serial asynchronous; and EIA RS-232-B, serial, synchronous, with internal or external timing. Power requirement is 115 Vac ±10%, 60 Hz ±10%, 5 A max. **Micom Systems Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.

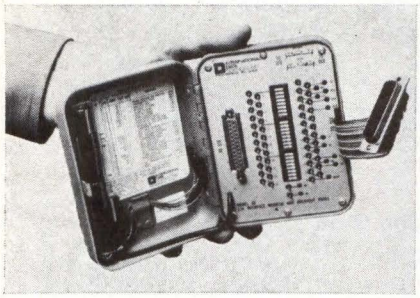


Circle 258 on Inquiry Card

NON-IMPACT NUMERIC PRINTER

Panel-mounting NP-7 provides seven columns of digits or six digits with a sign, at up to 4 lines/s, is supplied with interface electronics for most digital panel meters, accepts BCD data, and is DTL/TTL compatible. Printing occurs as the thermally sensitive paper glides beneath a thermal print head. Paper loading consists of swinging out the front panel, sliding paper roll onto spindle, and inserting paper through drive rollers. **Gulton Industries, Inc, Measurement & Control Systems Div,** East Greenwich, RI 02818.
Circle 259 on Inquiry Card

EIA INTERFACE MONITOR AND BREAKOUT PANEL



A portable pocket-size test set, model 60 provides access to all 25 conductors of the EIA RS-232 interface. States at the source of 12 primary signals are monitored on 12 LEDs; two additional LEDs sense either positive or negative voltage levels greater than ±3 V. Interface conductors (except frame ground on pin 1) can be individually interrupted for isolated testing and observation of signals. Two penlite batteries provide power for >100 h of continuous operation. **International Data Sciences, Inc,** 100 Nashua St, Providence, RI 02904.
Circle 260 on Inquiry Card

VIDEO SOURCE IDENTIFIER

All within a small PC card, the VSID tags electronic video signals in the same technique that electronic cabling and equipment are identified with reference designations. Power consumption in dc volts per card is 5 V, 410 mA; −5 V, 15 mA; −12 V, 7 mA; video inputs are 1.0 to 1.4 V pk-pk, 75-Ω terminated; and outputs are two each 75-Ω source terminated, 40-dB isolation. Frequency response is 0.5 dB to 8 MHz. Tilt and overshoot are less than 1%, and differential gain is 2% at 1 V pk-pk. **QSI Systems, Inc,** 993 Watertown St, West Newton, MA 02165.
Circle 261 on Inquiry Card

PC BOARD DISC DRIVE CONTROLLER

Self-contained TDC 803 interfaces any CalComp Trident series disc drive to Interdata minicomputers. It plugs into one slot in the CPU chassis and is cabled directly to up to four disc drives. An internal RAM with std capacity of 512 bytes permits up to 446 data bytes to be stored per sector. RAM is expandable in 256-byte increments to 2048 bytes for a max 1982 data bytes/sector. Disc reads and writes are fully buffered to accommodate high data rates. Jumper-selectable sector size is variable in 1-byte increments. **MiniComputer Technology,** 1901 Old Middlefield Way, Mountain View, CA 94043.
Circle 262 on Inquiry Card

LOGIC POWER SUPPLY MODULE

Useful to supply 5-V at 600 mA and 0.05% regulation to digital ICs and related circuitry, the P37C, an epoxy-encapsulated module, is short circuit and overvoltage protected, and is constructed to thermally isolate heat sensitive components from heat generating components. Designed for PC mounting, unit can be supplied with fixed voltages from 3.6 to 15 V. Other features include 95- to 125-Vac, 50- to 400-Hz input, and 1-mV rms ripple and noise. **Polytron Devices, Inc,** PO Box 398, River Street Sta, Paterson, NJ 07524.
Circle 263 on Inquiry Card

ARRAY PROCESSOR

For repetitive processing of vectors and arrays, the APS replaces conventional sequential procedures with simultaneous parallel execution of multiprocessor tasks, to upgrade any computer system. A host computer performs I/O and simple housekeeping tasks and passes all arithmetic processing to APS via subroutine calls. At max speed, the unit can perform a 1024-point real FFT in 1.4 ms and a 1024 x 32-point floating-point correlation in 4 ms. **PCS GmbH, Periphere Computer Systeme,** Dompfaffweg 10, D-8000 Munchen 82, West Germany.
Circle 264 on Inquiry Card

DATA TABLET/DIGITIZER INTERFACE

Coupling the company's data tablet digitizer with Digital Equipment Corp's PDP-11 computers, the single quad-width PC board occupies one SPC slot on the Unibus™ making max use of minicomputer and tablet features. The interface transfers X-Y coordinate information from controller to computer, and operates in either programmed I/O or interrupt mode. Interfaces are also available for DEC PDP-8, Data General Nova, Hewlett-Packard calculators, RS-232 communications, and IBM 029 keypunch. **Summagraphics Corp,** 35 Brentwood Ave, Box 781, Fairfield, CT 06430.
Circle 265 on Inquiry Card

LITERATURE

RAM Tester

Core and semiconductor memory testing procedures, features, and specs of the T-115 memory tester are discussed in folder. **Concept Development, Inc,** Costa Mesa, Calif.
Circle 300 on Inquiry Card

Communications System

Brochure describes specs and operation of the electronic Telescriber which transmits handwritten information, operating over std telephone wires. **Telautograph Corp,** Los Angeles, Calif.
Circle 301 on Inquiry Card

Key Tops

Designed as a reference source, illustrated brochure supplies descriptions and application guide for various keytop styles. **Key Tronic Corp,** Spokane, Wash.
Circle 302 on Inquiry Card

Programmable Controller System

Specs, features, and applications of the 1084 programmable controller are listed in brochure illustrated with photos, diagrams, and application drawings. **Modicon Corp,** Andover, Mass.
Circle 303 on Inquiry Card

360/370 Plotting System

Highlighting on/offline versions, software programs, and interfaces for electrostatic plotting systems, illustrated brochure offers model selection chart, sample applications, and specs. **Versatec, a Xerox Co,** Santa Clara, Calif.
Circle 304 on Inquiry Card

Linear and Conversion IC Products

Application notes, selection guides, industry cross reference, and data sheets for IC ADC and DAC products, op amps, comparators, and voltage references are included in 282-page catalog. Write on company letterhead to Jean Littrell, **Precision Monolithics, Inc,** 1500 Space Park Dr, Santa Clara, CA 95050.

Filters for Signal Processing

Complete with curves and diagrams, theory and applications handbook supplies information for using filters in analog and digital signal processing systems. Send $3 (U.S. and Canada; $5 overseas) to **Rockland Systems Corp,** 230 W Nyack Rd, West Nyack, NY 10994.

Microprocessor Technical Library

Describing technical publications, the brochure summarizes user, reference, and programming manuals covering memory systems, single board computers, and the company's microprocessor families. **Intel Corp,** Santa Clara, Calif.
Circle 305 on Inquiry Card

Data Conversion Components and Systems

Featuring monolithic, hybrid, and modular components, the 288-page Engineering Product Handbook is categorized by device performance and has an application section and data sheets. **Datel Systems, Inc,** Canton, Mass.
Circle 306 on Inquiry Card

OEM Line Printer

Data sheet describes features, options, and electrical and physical specs of medium speed, high performance model 2423 line printer. **Data 100 Corp,** Minnetonka, Minn.
Circle 307 on Inquiry Card

In-Circuit Test System

Highlights of the Troubleshooter 400 microprocessor-controlled system for testing complex PC boards are covered in the brochure. **Zehntel Inc,** Concord, Calif.
Circle 308 on Inquiry Card

Microprocessor/Display Interface

Techniques for interfacing microprocessors to alphanumeric displays are described in an application note providing basic hardware and software instructions. **Burroughs Corp, Electronic Components Div,** Plainfield, NJ.
Circle 309 on Inquiry Card

Digital Data System Equipment

Containing drawings and charts, DDS station equipment brochure furnishes specs on the L500A data service and L550A channel service units. **GTE Lenkurt Inc,** San Carlos, Calif.
Circle 310 on Inquiry Card

8-Bit Microprocessor

Written for non-computer-oriented professionals, the 170-page examination of the Intel 8080 covers flowcharting and programming techniques with typ problems. Send $13.95 to **Technitrol, Inc,** 1952 E Allegheny Ave, Philadelphia, PA 19134.

Microcomputers

Microcomputer systems, peripherals, software, and components are among the items offered in catalog which provides reference material to aid in making mail order selections. **Newman Computer Exchange Inc,** Ann Arbor, Mich.
Circle 311 on Inquiry Card

Printer Terminal

Describing the series 30 dot matrix printer (30 char/s, 128 ASCII char), brochure provides a checklist of features, and explains specs and capabilities of RO, KSR, and ASR models. **Di/An Controls, Inc,** Boston, Mass.
Circle 312 on Inquiry Card

Microcomputer Terminology

Pocket-sized LSI-11 glossary contains more than 200 microcomputer-related terms covering both equipment and programming aspects. **Digital Equipment Corp,** Marlborough, Mass.
Circle 313 on Inquiry Card

Acoustic Telephone Coupler

Detailing a concept in acoustic coupling at 1200 baud, flyer outlines features of the "Bawdy 12" data set and its built-in intelligence. **Omnitec Corp,** Phoenix, Ariz.
Circle 314 on Inquiry Card

Clip Strip

Basics of the universal solderless busing system are presented in bulletin which offers features, specs, and test data. **Electronics Stamping Corp,** Gardena, Calif.
Circle 315 on Inquiry Card

Transformer Design

Covering all phases of transformer design, catalog and engineering handbook includes stock tables, technical data, and spec outline sheet. **Inglot Electronics Corp,** Chicago, Ill.
Circle 316 on Inquiry Card

Electrical Contact Components

Descriptions of properties and applications of low energy electrical contact components, plus index to technical aids, are outlined in catalog. **The J. M. Ney Co, Electronics Div,** Bloomfield, Conn.
Circle 317 on Inquiry Card

Hybrid Microcircuits

Data handbook contains detailed information for both specifying and applying special function analog and digital circuits. Send check for $3 (Calif residents add 6% sales tax) to Marketing Services Dept, **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

1976 Computer Design Index

An up-to-date listing of editorial features published this year

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Synchros and Resolvers

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Hybrid Computers and Systems

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GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

SURVEY OF MICROPROCESSOR/ MICROCOMPUTER BUYERS

The publishers of COMPUTER DESIGN and the leading industrial market research company INTERNATIONAL DATA CORPORATION announce a significant new market research report entitled:

Survey of Microprocessor/ Microcomputer Buyers

7000 COMPUTER DESIGN readers were surveyed to determine:

- the type of equipment using μPs/μCs they are currently designing.
- the μP/μC models selected and the criteria for the selection
- the memories selected and the criteria for the selection.
- peripherals used with the equipment.
- various aspects of software and test.
- opinions on current μPs/μCs and peripherals.
- recommendations for their improvement.
- future plans for using μPs/μCs

and much more.

The 150 page report contains more than 50 tabulations of data from the survey, many of them correlating use factors and selection criteria with type of equipment. Each table is accompanied by an explanation of its meaning and an interpretation of its significance.

For a more detailed description of the report, circle 120 on the Reader Inquiry Card,

or write

Survey of Microprocessor/
Microcomputer Buyers

Computer Design
Market Research Group
143 Swanton St.
Winchester, MA 01890

ADVERTISERS' INDEX

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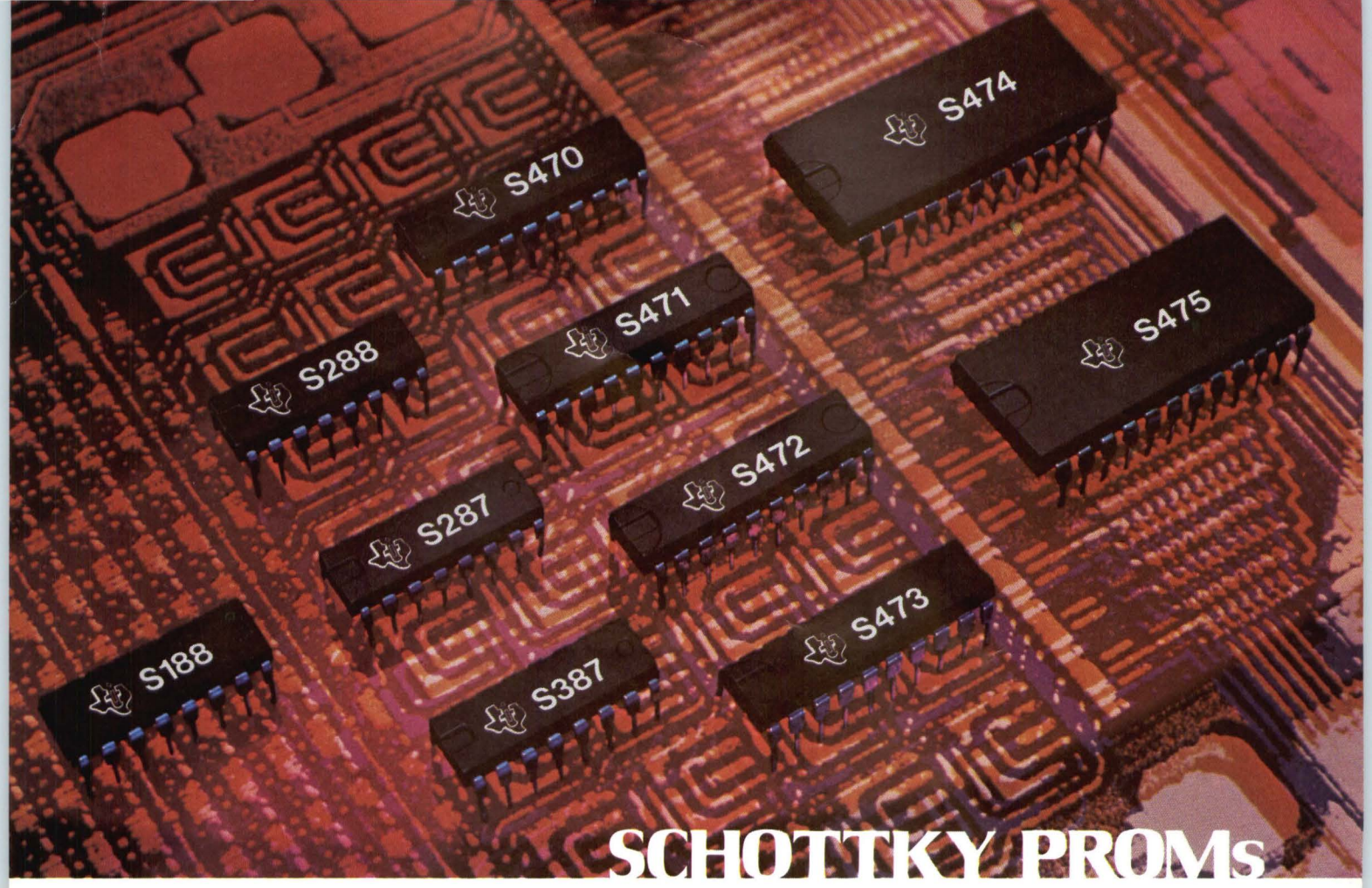

The PROM family. It means more flexibility. Higher efficiency. And lower costs.

TI's broad 10-member family of matched PROMs means plenty of options. And options mean you can design within the PROM family.

So all your PROMs are manufactured using the same process technology. The same design rules. The same packaging. And, what's especially important when using PROMs: All share common programming techniques. This way you not only get more efficient designs but a cost savings too.

Consider these options: You need a small amount of read-only memory. So, use the smaller family members, the 256 or 1K 16-pin PROMs. No need to pay for more memory than you need.

Suppose you're into new designs and want the highest possible board density offered. OK, take advantage of TI's 2K and 4K, space saving 20-pin PROMs. Some designers have cut PC board area by as much as 54%. And they have a wide 8-bit output for use in today's, and tomorrow's, microprocessor based designs.

On the other hand, if you have an older design already committed to the large 24-pin package, TI has you covered there, too. No need to move away from TI's broad family of Schottky PROMs.

All are Schottky clamped for superior speed/power characteristics and are relatively insensitive to variations of temperature and supply voltage. All have low-current, pnp inputs for interface with MOS as well as Bipolar microprocessors.

And finally, all TI PROMs are made with titanium-tungsten fuse links—the result of a unique metallurgical technique in use for over five years. It makes low voltage programming fast and reliable.

Available Now

Order TI PROMs from your authorized TI Distributor. For a copy of TI's Schottky Memory brochure, contact your local TI sales Office, or write Texas Instruments Incorporated, P. O. Box 5012, M/S 308, Dallas, Texas 75222.

TI Schottky PROM Line Summary

Part Number	Description	Address Access Time	Power Dissipation
SN54S/74S188	32W x 8B, 0-C, 16 pins	25ns	400mW
SN54S/74S288	32W x 8B, 3-S, 16 pins	25ns	400mW
SN54S/74S287	256W x 4B, 3-S, 16 pins	42ns	500mW
SN54S/74S387	256W x 4B, 0-C, 16 pins	42ns	500mW
SN54S/74S470	256W x 8B, 0-C, 20 pins	50ns	550mW
SN54S/74S471	256W x 8B, 3-S, 20 pins	50ns	550mW
SN54S/74S472	512W x 8B, 3-S, 20 pins	55ns	600mW
SN54S/74S473	512W x 8B, 0-C, 20 pins	55ns	600mW
SN54S/74S474	512W x 8B, 3-S, 24 pins	55ns	600mW
SN54S/74S475	512W x 8B, 0-C, 24 pins	55ns	600mW

TEXAS INSTRUMENTS
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63097

CIRCLE 66 ON INQUIRY CARD

New Hytype Terminal for OEM's!

Fine print quality, graphics versatility and high speed tabbing.

We call it HyTerm and we've given it all the proven HyType reliability and maintenance ease. HyTerm is controlled by a microprocessor for speed, efficiency and versatility. It utilizes the new Diablo HyType II Printer mechanism noted for its typewriter print quality and speed. HyTerm is interface compatible to RS-232C and communicates in standard ASCII code. Both Receive Only (RO) and Send/Receive (KSR) models are available. All logic and circuitry, microprocessor, memory, and power supply are contained within the cover. Printer flexibility is maintained so software can initiate the mechanism's unique graphics performance, and its inherent high-speed horizontal and vertical tabbing and backwards printing capabilities. Other features: control panel and switches, audible alarm, variable format control, escape-code functions, full ASCII character set, keyboard overflow buffer, 158 character print buffer, and data error detection. Numeric pad, pin feed platen, and form tractor feed options are available. For complete specifications and features, write Diablo Systems, Inc., 24500 Industrial Blvd., Hayward, California 94545, or Diablo Systems, S.A., Avenue de Fre 263, 1180 Brussels, Belgium.

Diablo

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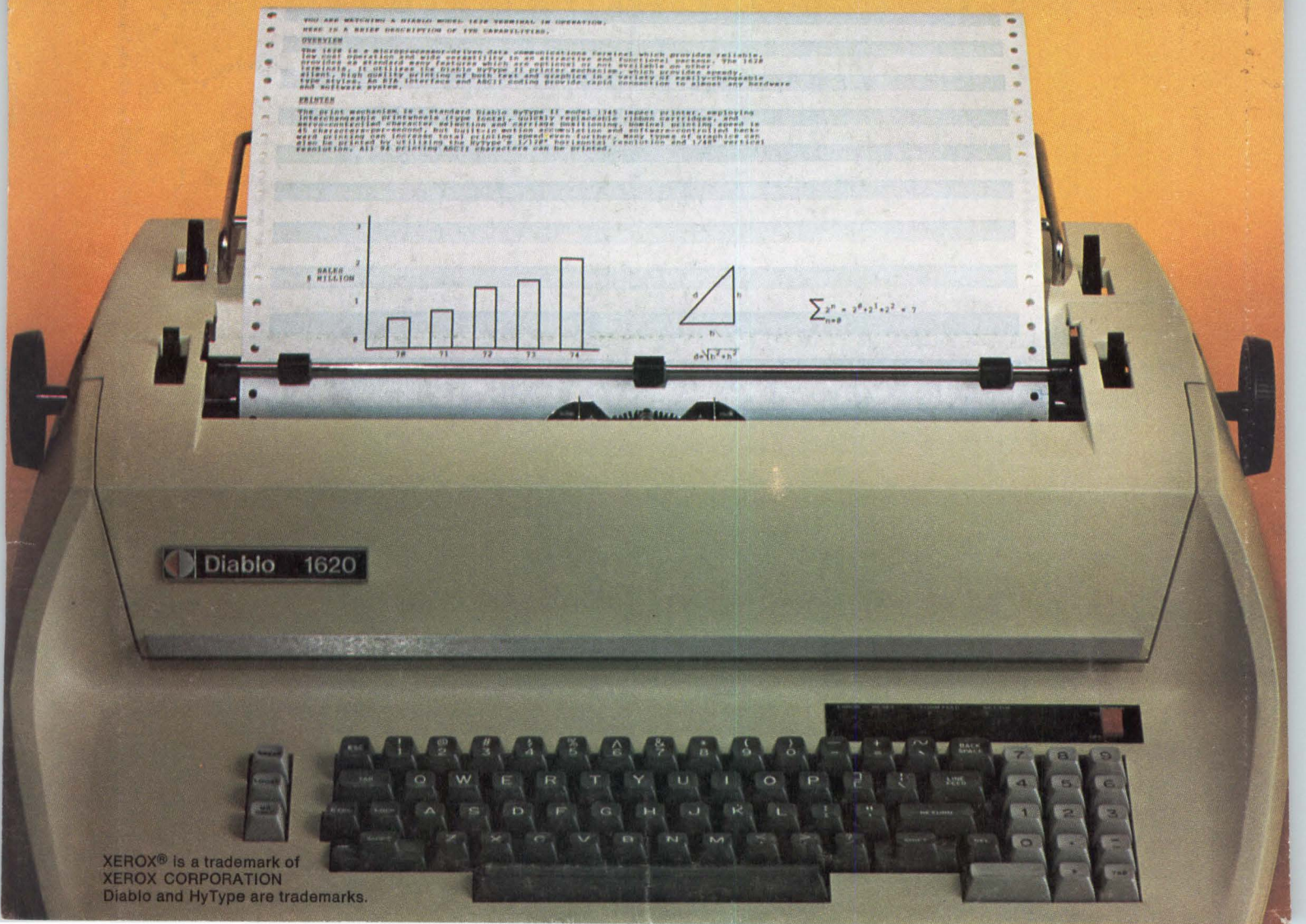
CIRCLE 67 ON INQUIRY CARD



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