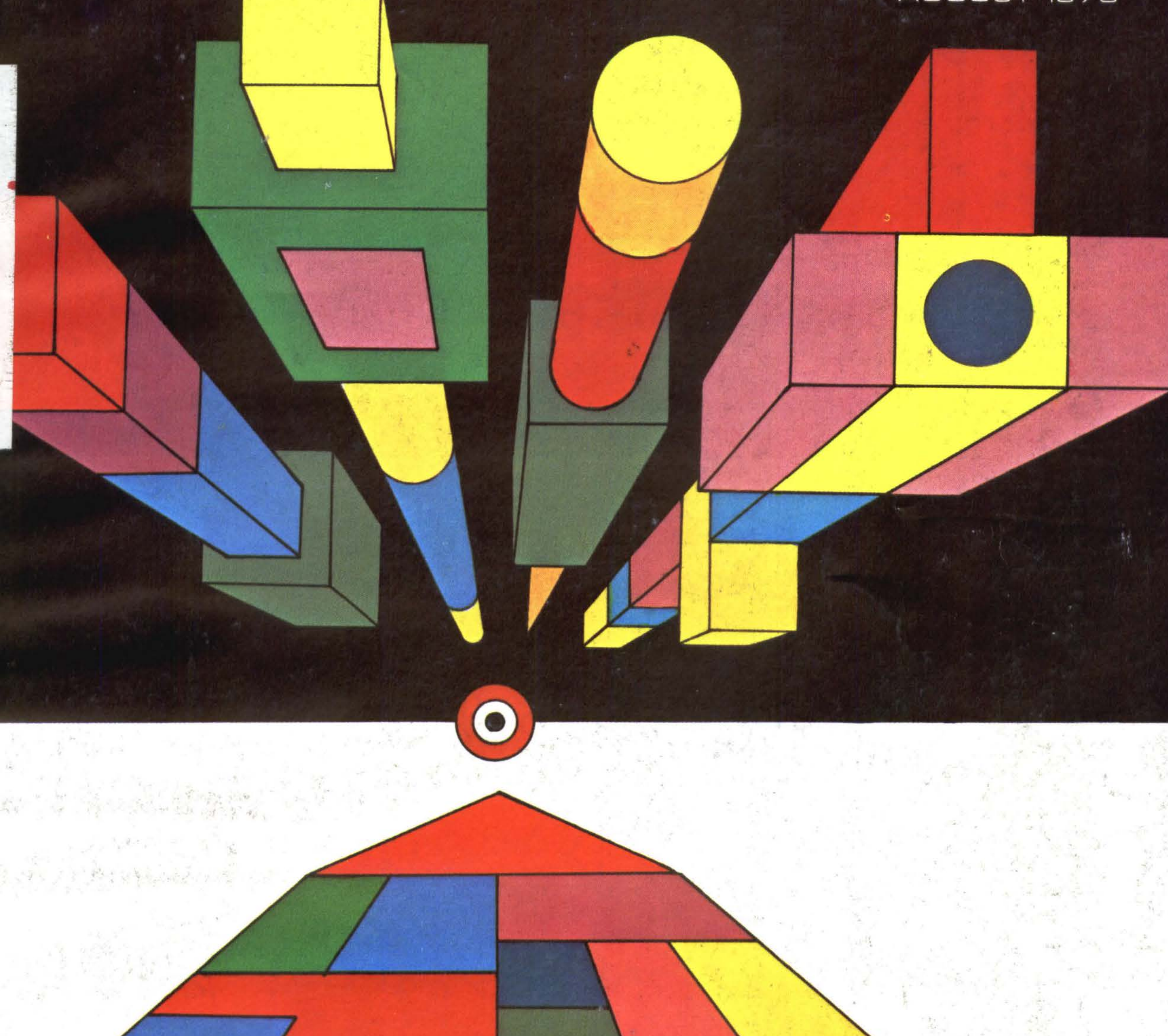
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

AUGUST 1978

INST OF VISUAL SCIENCE



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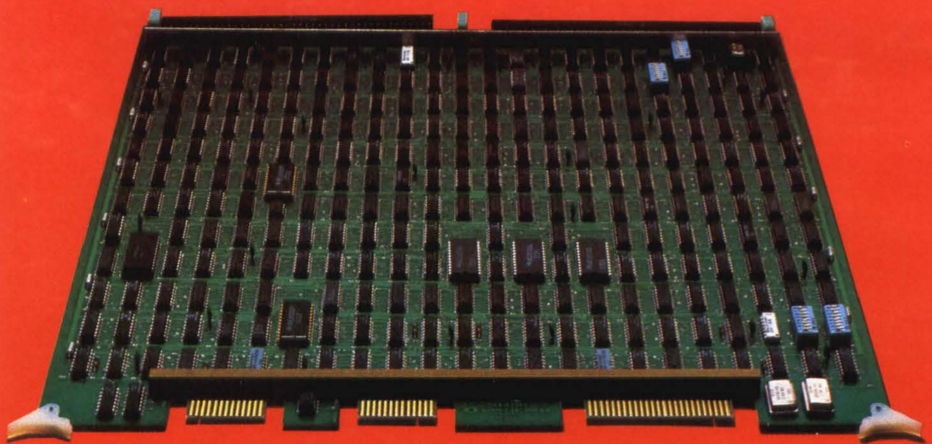

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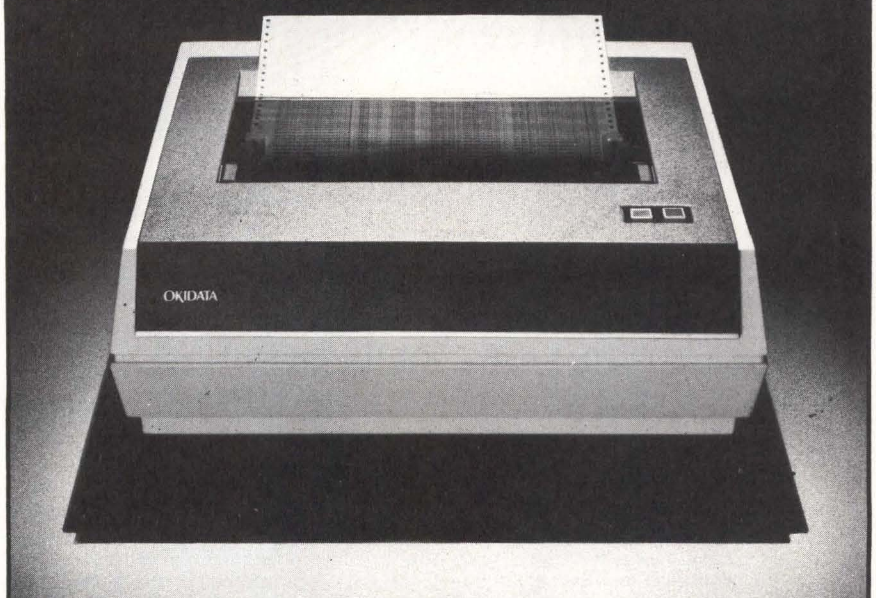
FEATURES

CONFERENCES

The New Slimline Series From Okidata



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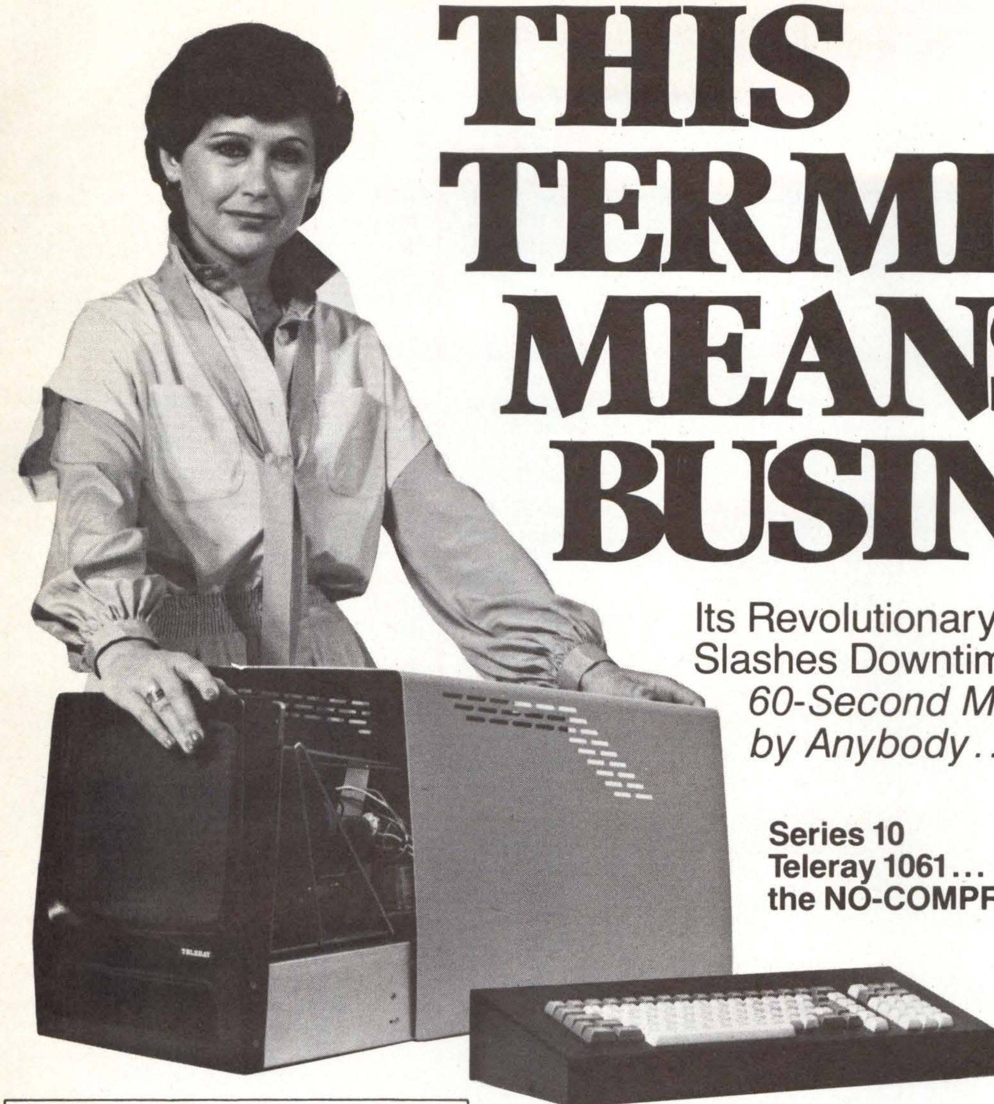

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CALENDAR

CONFERENCES

SEPT 5-8—COMPCON Fall '78, Capitol Hilton, Washington, DC. INFORMATION: COMPCON Fall, PO Box 639, Silver Spring, MD 20961. Tel: (301) 438-7077

SEPT 6-8—FOC '78, Fiber Optic and Communications Expo, Hyatt Regency-O'Hare, Chicago, Ill. INFORMATION: Information Gatekeepers, Inc, 167 Corey Rd, Suite 212, Brookline, MA 02146. Tel: (617) 739-2022

SEPT 12-14—Western Electronic Show and Convention (WESCON), Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: W. C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

SEPT 15-17—Personal and Business Small Computer Show, New York Coliseum, New York, NY. INFORMATION: Personal Computing Expo Inc, 78 E 56th St, New York, NY 10022

SEPT 19-21—Computer Aided Design and Computer Aided Manufacturing Conf (CAD/CAM VI), Hyatt House, Los Angeles Internat'l Airport, Los Angeles, Calif. INFORMATION: Computer and Automated Systems Assoc of the Society of Manufacturing Engineers, 20501 Ford Rd, PO Box 930, Dearborn, MI 48128. Tel: (313) 271-1500, X403

SEPT 20-22—Telecomputer Application Group Conf, Washington, DC. INFORMATION: Hollis J. Sobers, Allied Chemical Corp, PO Box 1039R, Morristown, NJ 07960. Tel: (201) 455-5123

SEPT 26-28—Automatic Test Equipment Conf and Expo (ATEX), Hynes Auditorium, Boston, Mass. INFORMATION: Bill Hickey, Golden Gate Enterprises, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94086

SEPT 26-28—Nat'l Electronics Packaging and Production Conf (Nepcon Central '78), O'Hare Internat'l Trade and Expo Ctr and Hyatt Regency O'Hare Hotel, Rosemont, Ill. INFORMATION: Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

SEPT 29-OCT 1—Internat'l Microcomputer Expo, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Beverly Tanner, Expo Dir, 413 Carillon Tower, 13601 Preston Rd, Dallas, TX 75240. Tel: (214) 271-9311

OCT 3 and OCT 5—Invitational Computer Conf, Valley Forge, Pa; and Washington, DC. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

OCT 6-11—Japan Electronics Show, Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: Japan Electronics Show Assoc, No. 24 Mori Bldg, 11 F, 3-23-5, Nishi-Shinbashi, Minato-ku, Tokyo 105, Japan

OCT 10-12—Conf of the European Cooperation in Informatics (ECI), Venice, Italy. INFORMATION: Prof Dr Peter Lockemann, Institut für Informatik II, Universität Karlsruhe, Postfach 6380, D-7500 Karlsruhe 1, Germany

OCT 10-12—USA/Japan Computer Conf, Jack Tar Hotel, San Francisco, Calif. INFORMATION: AFIPS, Inc, 210 Summit Ave, Montvale, NJ 07645. Tel: (408) 245-5807

OCT 16-19—ISA/78, Instrument Society of America Internat'l Instrumentation-Automation Conf and Exhibit, Philadelphia Civic Ctr, Philadelphia, Pa. INFORMATION: ISA/78, Philadelphia, 400 Stanwix St, Pittsburgh, PA 15222

OCT 18-20—Canadian Conf on Communications and Power, Queen Elizabeth Hotel, Montreal, Canada. INFORMATION: Jean Jacques Archambault, Chm-Technical Program Committee CP/PO 757, Succ C, Montreal, Quebec H2L 4L6, Canada

OCT 25-26—Electronic Connector Sym, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101

OCT 25-27—Sym on Computer Arithmetic, Miramar Hotel, Santa Monica, Calif. INFORMATION: Prof Milos D. Ercegovac, Computer Science Dept, U of Calif, Los Angeles, CA 90024. Tel: (213) 825-2660

OCT 31-NOV 2—Cherry Hill '78 Test Conf, Cherry Hill, NJ. INFORMATION: Pat Regan, Secretary/Registrar, Test Conf Comm, PO Box 2340, Cherry Hill, NJ 08034. Tel: (609) 983-3100

NOV 1-3—Internat'l Sym on Computers, Electronics, and Control (CEC '78), Toronto Hilton, Toronto, Ontario, Canada. INFORMATION: The Secretary, CEC '78, PO Box 3243, Sta B, Calgary, Alberta T2M 4L8, Canada

NOV 6-8—Asilomar Conf on Circuits, Systems, and Computers, Pacific Grove, Calif. INFORMATION: Donald E. Kirk, Electrical Engineering Dept, Naval Postgraduate School, Monterey, CA 93940

NOV 7-9—Mini/Micro Conf and Expo, Astrohall, Houston, Tex. INFORMATION: Robert D. Rankin, Managing Dir, Mini/Micro Conf and Expo, 5528 E La Palma Ave, Suite 1, Anaheim, CA 92807

NOV 13-16—Internat'l Conf on Computer Software and Applications (Compsac 78), The Palmer House, Chicago, Ill. INFORMATION: Wallace A. Depp, Executive Dir, Processor and Computer Software Systems Div, Bell Laboratories, Naperville, IL 60540. Tel: (312) 690-2111

NOV 14-17—Conf on Magnetism and Magnetic Materials, Stouffer's Inn on the Square, Cleveland, Ohio. INFORMATION: Dr Hugh C. Wolfe, American Institute of Physics, 335 E 45th St, New York, NY 10017

NOV 20-22—BIAS Internat'l Conf: Automation and Microcomputer, Milan Fair Ground, Milan, Italy. INFORMATION: Federazione delle Associazioni Scientifiche e Techniche, Piazzale Roldolfo Morandi, 2, 20121 Milan, Italy

DEC 18-20—Internat'l Computer Sym (ICS), Academia Sinica, Nankang, Taipei, Repubiic of China. INFORMATION: K. S. Fu, School of Electrical Engineering, Purdue U, W Lafayette, IN 47907. Tel: (317) 494-8825

SEMINARS

OCT 4-6—Knowing and Understanding Computer Graphics, San Francisco, Calif. INFORMATION: Robert Sanzo, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038. Tel: (212) 233-1080

SHORT COURSES

SEPT 6-8—Magnetic Bubble Memory Technology; and OCT 2-4—Applications of Microcomputers in Control Systems, The George Washington U, Washington, DC. INFORMATION: Martha Augustin, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

SEPT 11-13—Designing with Microcomputers; and SEPT 14-16—Microcomputer Interfacing, Blacksburg Learning Ctr, Blacksburg, Va. INFORMATION: Dr C. Titus, Course Dir, Tychon, Inc, PO Box 242, Blacksburg, VA 24060. Tel: (703) 951-9030

SEPT 14-15—Program Testing Tutorials, San Francisco, Calif. INFORMATION: Software Research Associates, PO Box 2432, San Francisco, CA 94126. Tel: (415) 921-1155

SEPT 19-22 and OCT 3-6—Fiber Optic Communication Systems, Houston, Tex; and San Diego, Calif. INFORMATION: Integrated Computer Systems, Inc, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: (213) 450-2060

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For detailed reasons why TI's 9900 First Family is your confident, low-risk choice, turn the page.

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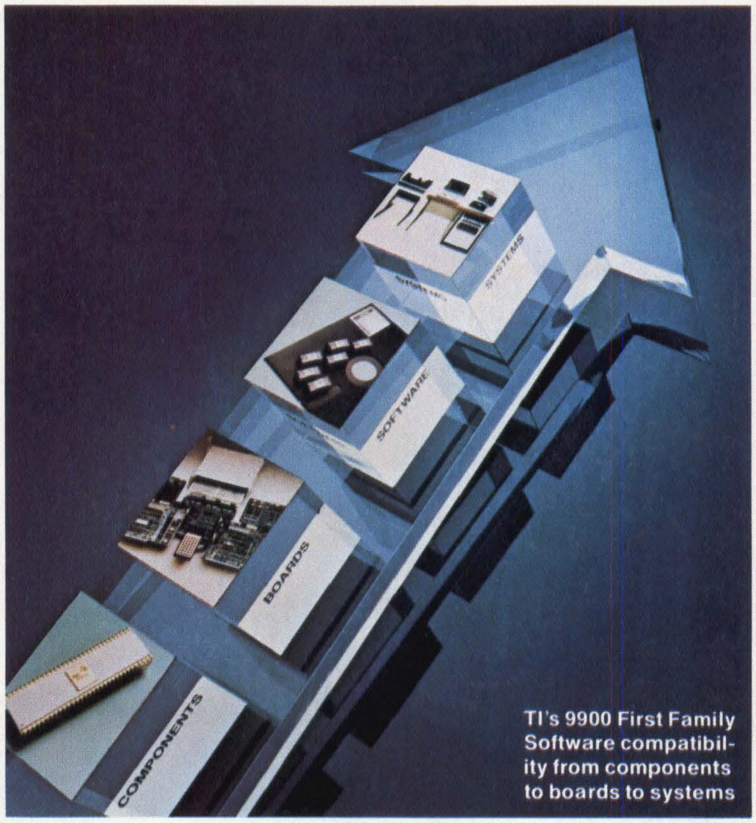

TI's 9900 First Family Software compatibility from components to boards to systems

From the outset, the 9900 First Family was planned to minimize risk by assuring the highest possible degree of protection for your biggest investment – software.

The family has been carefully structured to form a wide selection of compatible microprocessors, microcomputers and minicomputers using the same advanced memory-to-memory architecture. The same instruction set. The same development systems. All software supported and software compatible.

Which means you can begin using the family at any level you wish – components, modules or systems – and develop your software and training accordingly. Then move as you wish within the family while retaining all, or most, of your software.

For example, you may have designed a terminal around the TMS 9900 microprocessor. Now you can switch to the TMS 9940 to reduce system costs. Your software and other system hardware will work as well with the TMS 9940 as it will with the TMS 9900.

Cost-effective CPU choices

The 9900 Family utilizes state-of-the-art technologies (NMOS and I²L) to provide an unmatched choice of microprocessors. A choice that helps you best match price and performance to your design:

- TMS 9900: NMOS 16-bit microprocessor with full minicomputer capability.
- SBP 9900A: Ruggedized I²L 16-bit microprocessor functionally identical to the TMS 9900. Use it wherever operating environments are severe. Versions are available to meet the full military temperature range (–55°C to +125°C).
- TMS 9980/81: NMOS 16-bit microprocessor that minimizes cost of smaller systems by incorporating an 8-bit memory interface, 40-pin plastic packaging, and on-chip clock option.
- TMS 9940: Single-chip, 16-bit microcomputer featuring on-chip instruction memory (2K bytes of EPROM or ROM) and data memory (128 bytes of RAM), plus 32 bits of programmable input/output, and single 5 V operation. Designed to maximize performance at minimum system cost.
- S481 Chip Set: TTL modularly expandable building blocks giving the performance of a customized microcomputer, extremely fast (10 MHz) throughput and complete microprogrammability.

Broad peripheral backup

The 9900 First Family includes a wide selection of peripheral support circuits needed to complete your design. Easily. Economically. With full compatibility. Included are MOS, low-power Schottky TTL, and I²L circuits:

Device	Function
TMS 9901	MOS Programmable Systems Interface
TMS 9902	MOS Asynchronous Communications Controller
TMS 9903	MOS Synchronous Communications Controller
TIM 9904	LS TTL 4-phase Clock Generator
TIM 9905	LS TTL 8-to-1 Multiplexer
TIM 9906	LS TTL 8-bit Latch
TIM 9907	LS TTL 8-to-3 Priority Encoder

Soon to come:

TMS 9909 Floppy Disk Controller
TMS 9911 Direct Memory Access
TMS 9914 General Purpose Interface Bus
TMS 9927 CRT Controller (SMC 5027 equivalent)
SBP 9960 I²L CRU I/O Expander
SBP 9961 I²L Interrupt Controller/Timer
SBP 9965 I²L Peripheral Interface Device

In addition, TI offers a wide variety of MOS memories, including 4K and 16K static RAMs as well as 8K, 16K, and 32K EPROMs, and pin-compatible ROMs.

Low-cost microcomputer modules

To save the time and cost of developing your own hardware, use TI's TM 990 microcomputer modules.

They are preassembled. Pretested. Ready to go. Supported by TI's Advanced Microprocessor Prototyping Lab (AMPL*). And instruction-set compatible with other First Family members. Included in the series:

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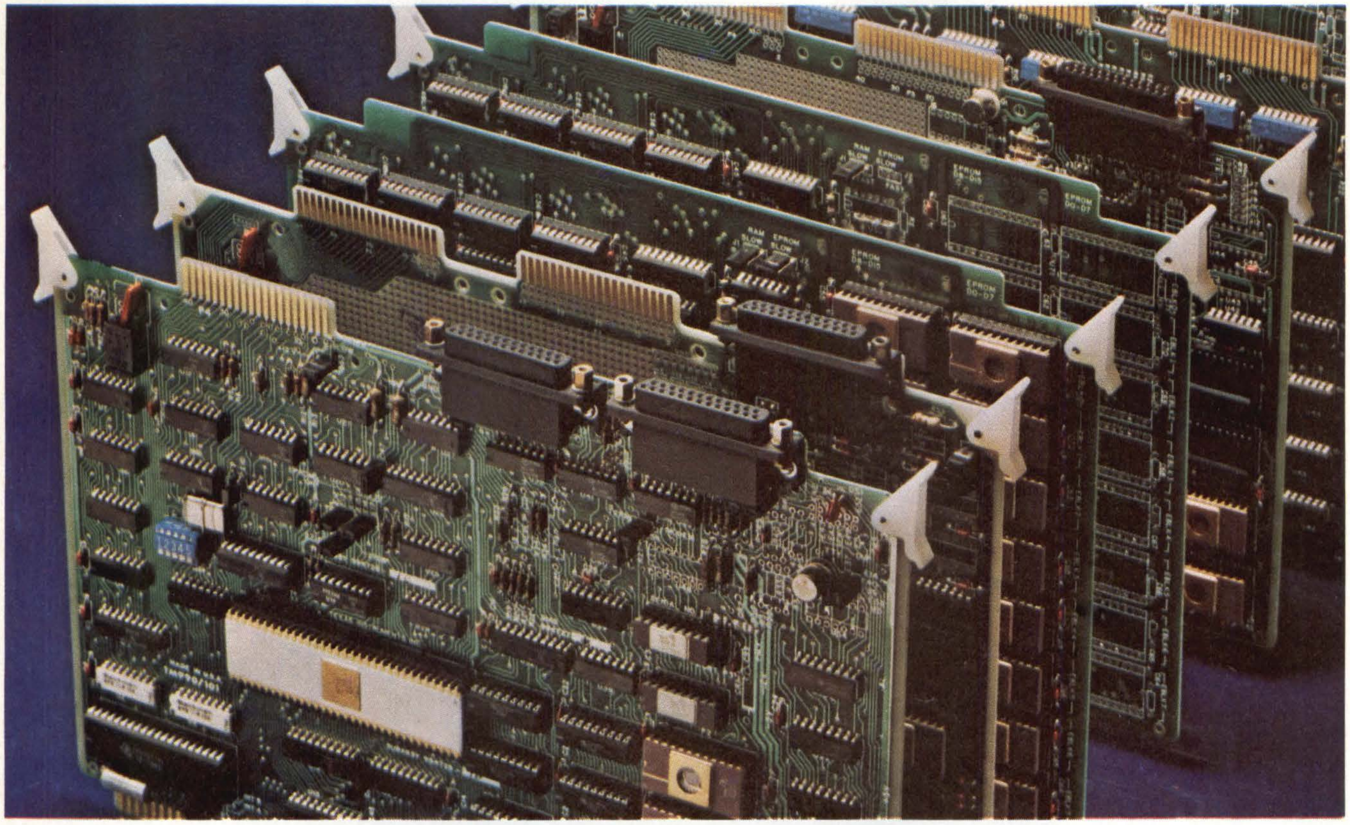
- TM 990/100M: Utilizes TI's NMOS 16-bit TMS 9900 microprocessor, 512 bytes of static RAM, 1K words of EPROM, and programmable serial and parallel I/O to form a powerful single-board microcomputer.
- TM 990/101M: A new and expanded version of the TM 990/100—2K words of static RAM, 4K words of EPROM, two serial RS232C communication ports.
- TM 990/101M-10: Duplicates the 101M but has POWER BASIC* high-level language preprogrammed into the ROM.
- TM 990/180M: 16-bit TMS 9980 microprocessor offers 2.5 MHz operation with 8-bit memory interface for smaller systems.
- TM 990/201: Memory expansion board—8K bytes of EPROM, 4K bytes of static RAM. Expandable to 32K bytes of EPROM and 16K bytes of RAM.
- TM 990/206: Memory expansion board with 8K bytes of static RAM. Expandable to 16K bytes.
- TM 990/301: Microterminal for data entry and display.
- TM 990/310: 48-bit input/output expansion module.
- TM 990/401: Interactive debug monitor (TIBUG*) preprogrammed into EPROM.
- TM 990/402: Line-by-line assembler preprogrammed into the EPROM.
- TM 990/450: Stand-alone evaluation interpreter, using 8K bytes of memory, for exploring POWER BASIC applications.



- TM 990/451: Development interpreter, using 12K bytes of memory, for the design, development, debug and EPROM programming of POWER BASIC programs.
- TM 990/510: Four-slot OEM card cage with 1″ spacing.

Cables, connectors, extender and prototyping boards also available.

Now on the way: a low-cost 9900 family software development board. It will include audio cassette interface, symbolic assembler, text editor, relocating loader, I/O scheduler-handler, debugger, and programmer for EPROMs including the EPROM being incorporated in the TMS-9940E microcomputer. Also coming: a low-cost, stand alone, educational board—complete with tutorial text—for bootstrapping yourself into the 16-bit world.

Cost-cutting compilers

Just as the modules speed development and hold costs in line, so do TI's high-level language compilers.

They are simple to use. Programmers can write more code, and write it faster, with less training. The result is greatly improved programmer productivity and significantly reduced software costs.

Already available: PASCAL and FORTRAN compilers on TI's AMPL. BASIC interpreters on both AMPL and TM 990-based systems.

On the way: Complete runtime support libraries for component-based systems, including pretested executive modules which are easily interfaced with compilers and assemblers.

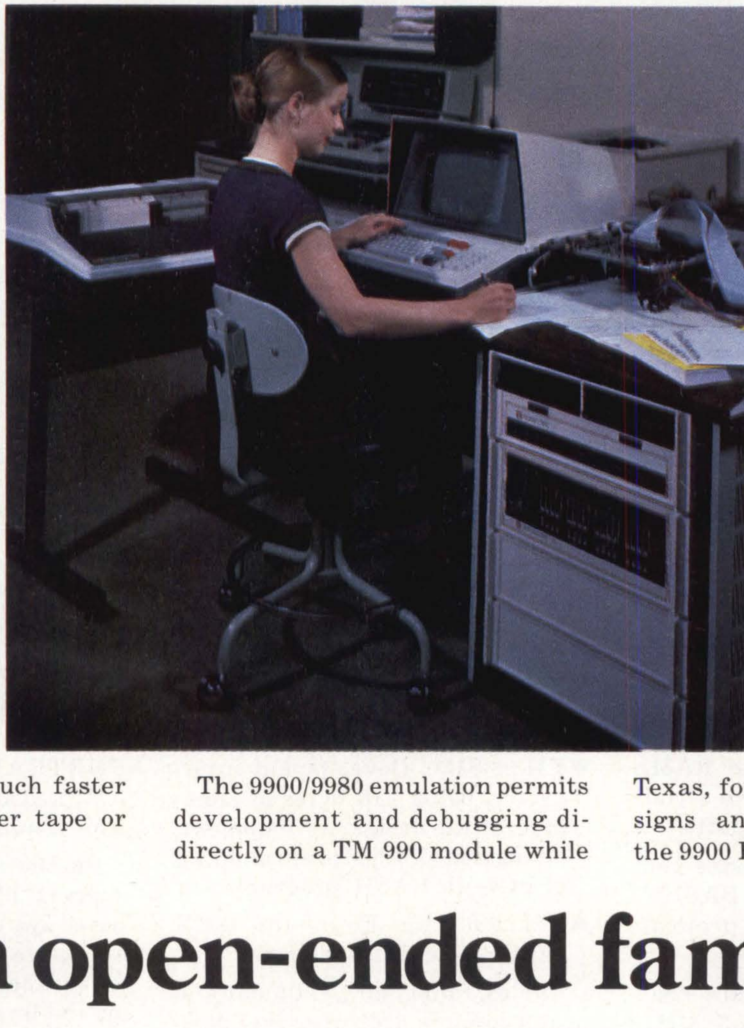
Affordable minicomputer

The DS990 commercial computer system is the First Family's most powerful member. Built to give maximum processing power, it provides the high performance speeds demanded by many applications. It is backed by high-level software languages—PASCAL, RPG II, FORTRAN IV, COBOL and multi-user BASIC—as well as a large selection of peripherals.

What about hardware and software development support for the 9900 spectrum? It's in place in depth. Turn the page.

TI's 9900 First Family

In-depth hardware/software development support



Users of the 9900 First Family have at their disposal the most extensive software support currently available with any microprocessor. It is TI's Advanced Microprocessor Prototyping Lab.

AMPL features the 990 computer, and offers 10 MHz trace capability and universal emulation for the TMS 9900, SBP 9900A, TMS 9980/81 and TMS 9940 microprocessors.

The lab is available as a floppy disk system or as a hard-disk system accommodating multiple users. Programs can be edited, assembled, linked, loaded and executed much faster than conventional paper tape or cassette based systems.

The 9900/9980 emulation permits development and debugging di- directly on a TM 990 module while monitoring and controlling the operation from AMPL.

The interactive process allows simulation/test and emulation/test cycles with minimum delay between identifying and implementing a needed design change. Result: substantial savings in design time and cost.

The First Family is also supported by nationwide timeshare and cross-support—transportable assemblers and simulators—for use with in-house computers.

In addition, TI maintains extensive learning facilities in Austin, Texas, for the study of system designs and applications utilizing the 9900 First Family.

An open-ended family

One final reason to choose the 9900 First Family. It is growing and TI is committed to its continuation and expansion. As your needs change—and as new technologies develop—you can expect other microprocessors and peripherals to join the 990/9900 Family

For total down-the-line support. For protection of your software investment as your performance and cost requirements change with time. For keeping up with tomorrow.

If you are now considering microprocessors for the first time or have used 8 bits and now need the improved performance of 16 bits, your best choice—your confident choice—is TI's 9900 First Family.

For more information on the 9900 First Family, call your TI Field Sales Office or local TI Distributor System Center. Or write Texas Instruments Incorporated, P. O. Box 1443, M/S 653, Houston, Texas 77001.

TEXAS INSTRUMENTS MOVING AHEAD IN MICROPROCESSORS

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MULTI-VENDOR INFORMATION SYSTEMS

John E. Buckley

Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

For many years a prevailing philosophy for computer communications systems procurement has been to obtain necessary equipment components from a single manufacturer. The assumption was that this practice would preclude possibility of equipment incompatibilities, and assure rapid resolution of system malfunctions. In many early online information systems, this procedure could be applied with minimal penalty in system effectiveness, and indeed did seem to relieve many of the more obscure system problems. It was always recognized that at least two vendors would be involved in the user's information system: the utility telephone company and, typically, the computer manufacturer.

With the growth of information system applications and complexity, it became apparent that continued adherence to this archaic philosophy could significantly affect both system effectiveness and system value. Characteristically, a number of different vendors of equipment and services are involved in order to fully satisfy a total information system requirement. One typical application environment involved no fewer than six different equipment and service entities: computer manufacturer, computer-site modem manufacturer, manufacturer of the privately-owned computerized telephone system, utility telephone company, remote-site modem manufacturer, and remote terminal manufacturer. When that remote terminal was online with the central computer, all six maintenance responsibility areas interacted. Data errors as well as other sources of malfunction could reside in any of these elements. The frustrated user had to direct and coordinate the correction process among all these possibilities knowing all the while that each service entity was primarily concerned with demonstrating that its area of responsibility was innocent of any contribution to the problem.

A number of steps that an information system user can implement will facilitate maintenance of satisfactory system operation in a multi-vendor environment. A major premise is that proper operation is the absolute responsibility of the system user. Even where most system components are provided by a single vendor, operational status is the exclusive domain of the system user. Nonacceptance of this premise will only result in recurring frustration as ambiguous system malfunctions continue to occur. The assumption that one or more of the vendors will somehow properly and cooperatively diagnose problems and implement an effective cure is both time-consuming and naive.

Based on acceptance of the above is the need for the system user to select and implement equipment that allows for component isolation. In normal operation, various system equipment components, such as those outlined above, operate in series to effect proper and reliable data flow between remote terminal and centralized computer complex. Malfunction or incompatibility in one or more of these components will result in data errors or even in total application failure. It is important to select equipment components that can operate in isolated configurations and can perform system diagnostics.

Remote terminals should be able to implement a local terminal loopback mode. In this mode, data entered from the keyboard pass through the transmit portion of the terminal to the EIA interface, where output data flow is connected to the terminal's input or receive section. Test data are then returned through terminal to output printer or CRT display. It is important that in this loopback mode as many of the internal electronic circuits of the terminal are involved and therefore verified. All functions such as parity, communications timing, and buffer operation should be included and hence tested. This mode is commonly identified as the half-duplex mode of the remote terminal. Some terminals identify a half-duplex mode but in reality consist of a direct connection between the keyboard and the output printer or display. This version of half-duplex provides no diagnostic advantage since the data are displayed before transmission through the terminal's electronics.

This same type of loopback data flow should be inherent in the modem associated with the remote terminal. Ideally, data flow in the modem loopback should pass through the entire modulator and then be loopbacked through the demodulator. It is recognized that some modems are incapable of this internal full-duplex data flow. To the greatest extent, however, the above operation should be implemented as a desired objective. As with remote terminals, a number of modems advertise loopback capability while in reality the loopback function is accomplished prior to the modulator and demodulator sections of the modem. Digital loopback at the remote modem is also desirable but here the modem checks out with the central computer. The modem's EIA interface should be capable of returning a test signal generated by the central computer to the central computer. This latter loopback is contingent upon the modem being capable of full-duplex operation. In addition, the associated communications channel must be of 4-wire configuration, actual or simulated.

It is in the communication channel that the greatest obstacle to malfunction isolation can be encountered. This problem is due either to the technical configuration of the communication channel or to a short term economic procurement decision. If the communications connection is via the public switched network at a data rate less than 300 bits/s, a simulated 4-wire channel is provided. Over 300 bits/s, with the exception of the Vadic 1200-bits/s modem, the channel is only 2-wire, and therefore cannot be used for simultaneous transmit and receive as required for full loopback diagnostics.

At the computer site, the modem should also provide the same 2-way loopback capability as discussed for the remote modem. The usual failure in this method of loopback isolation is the central computer communications adapter and associated software. Many computer manufacturers have designed communications adapters for "normal" interactive processing of data flow and therefore preclude simultaneous transmit and receive. In a number of cases, the hardware computer adapter may be full-duplex but the controlling software is only half-duplex in its channel activation status and data manipulation.

During the initial design of an online application, these provisions must be addressed. It is usually financially prohibitive to attempt to retrofit an existing system in order to have this level of loopback diagnostics. Even if one or more of the equipment components, ie, communication channel, prohibits by design a loopback testing procedure, similar testing and confirmation of the other components can isolate the problem source by default if not by actual verification.

Every online system must have a fault isolation test procedure to be followed in the event of suspected malfunction or where adverse error rates occur. Before any vendor service is solicited, the system user must perform and log these tests. In this manner the proper service vendor can be notified and supplied with a reasonable description of the problem area and symptoms. Following the attempted correction by the service vendor, the same test that isolated the fault can be performed and the correction confirmed while the vendor service personnel are still at the user's site.

Many system problems are caused by degrees of incompatibility rather than by equipment malfunctions. Many of these incompatibilities are detected at initial installation and are clearly evidenced when the system will not operate. Unfortunately, a significant percentage of incompatibilities allow marginal system operation and can be easily misinterpreted as malfunctions rather than as incompatibility caused by a design error. Typically these situations occur at the interfaces between the various manufacturer's equipments. The traditional EIA interface is a major source of these "grey" problems. Between the digital equipment and the communication channel minimal interface incompatibilities can be expected unless a data connecting arrangement is employed. While data connecting arrangements came into existence with the intent to protect, they have been the greatest source of system problems at the digital-to-analog interface. Fortunately, with the rapid implementation of data and voice communications systems registration, this protection-intended device is being eliminated from the equipment equation.

It is interesting to note that two of the EIA interface leads can account for most of the incompatibility between two equipment components at this interface. These are the Data Set Ready and Data Terminal Ready leads. As an example, this type of incompatibility recently occurred with a dial-access interactive processing application. When the computer channel was initialized by software, the Data Terminal Ready lead was activated. This was interpreted by the channel's associated modem to be receptive to an incoming ring signal. Upon receipt of ringing, the connection was answered and the modem activated its Data Set Ready lead. When the remote caller terminated the dial connection, the Data Set Ready lead was dropped which caused the Data Terminal Ready lead to drop. Without a Data Terminal Ready signal, the modem refused to answer any additional incoming calls. Upon re-initialization of the channel by the computer operator, the next incoming call was answered.

It is important to not only verify which EIA interface leads are used by the two different manufacturers' equipment but also the operational sequence of those leads. The preconditions that must be present to change the status of each lead must be thoroughly reviewed and documented. In this context an important test device for a system user is an EIA interface display tester. This device, typically costing less than $100, can be connected in series with the EIA interface between two digital equipment components. Status of each lead is illustrated, and a means of changing lead status for simulation purposes is provided. It is fallacious to assume that equipment service personnel will always be equipped with such test equipment or that they will properly test the interface on both digital equipment components. Most service organizations agree that it is useful to have knowledgeable service personnel for two equipment components jointly testing onsite at the same time. Many users, however, have been told upon the departure of one service person that the problem is not in their equipment and to notify the service personnel of another equipment component. When a problem is not immediately resolved by the first maintenance attempt, and the user is so advised, he should demand a joint diagnostic effort. When skilled help from a number of equipment components manufacturers jointly and cooperatively address a system problem, the solution is usually forthcoming.

Virtually every equipment manufacturer's policy is to constructively participate in joint diagnostic efforts for a mutual customer. The only exception to this cooperative philosophy was recently promulgated by the Bell System, specifically The Bell Telephone Co of Pennsylvania. The latter organization has a policy that its service personnel will not jointly test on a customer's premises, with service personnel from manufacturers of other communications equipment which connects to their communication channels. Their policy is for the equipment manufacturer's service personnel to identify the deficiency in the telephone company interface to the manufacturer's equipment. Telephone company service personnel will then come to the customer's site and if the deficiency is confirmed, implement the necessary corrections. Despite this myopic exception, the system user should insist on having joint, cooperative service efforts for chronic and prolonged malfunctions.

Reliable system operation is primarly in the lap of the system user. He is exclusively responsible for definitive malfunction isolation diagnostics. This can be accomplished by design and selection of a system that permits loopback testing for all online equipment components. The existence of marginal or sporadic incompatibilities can create the illusion of a malfunctioning system. During actual selection of equipment components, hardware and software, these occasions can be minimized with proper and prudent confirmation of various interface configurations and operations. While all these measures should significantly lessen frustrations caused by chronic malfunctions, even these hopefuly rare events can be constructively addressed by a joint diagnostic effort under the direction of the system user. Multiple vendor systems are commonplace. For optimum effectiveness and value they will continue to be installed and properly operated by knowledgeable customers.

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CIRCLE 7 ON INQUIRY CARD

Communications Conference Shows Impact of Digital Technology

ICC '78, the 14th Annual International Conference on Communications, sponsored by the Communications Society Conference Board and the Toronto Section IEEE, convened in Toronto, Canada June 4-7, 1978. The technical sessions were made up of more than 250 papers by authors from around the globe, and covered a wide spectrum of activities in the communications world. The program was heavily oriented toward the application of digital technology and the influence of computer-derived practices on system design; nor was the rapid emergence of fiber optics as a significant force in future network planning neglected. In the space available here we can present but brief highlights of the program that we consider to be of particular interest to our readers—but it is only the tip of the iceberg.

Reliability in Data Communications

Common Carrier Telephone Plant

Since, for a variety of reasons, most computer communications systems use telephone channels as links, factors determining the reliability of these channels and the impact of this reliability are of importance in the design of communications-based data processing systems.[1] A detailed description of the U.S. common carrier telephone plant was given, with emphasis on the factors that affect the reliability of channels.

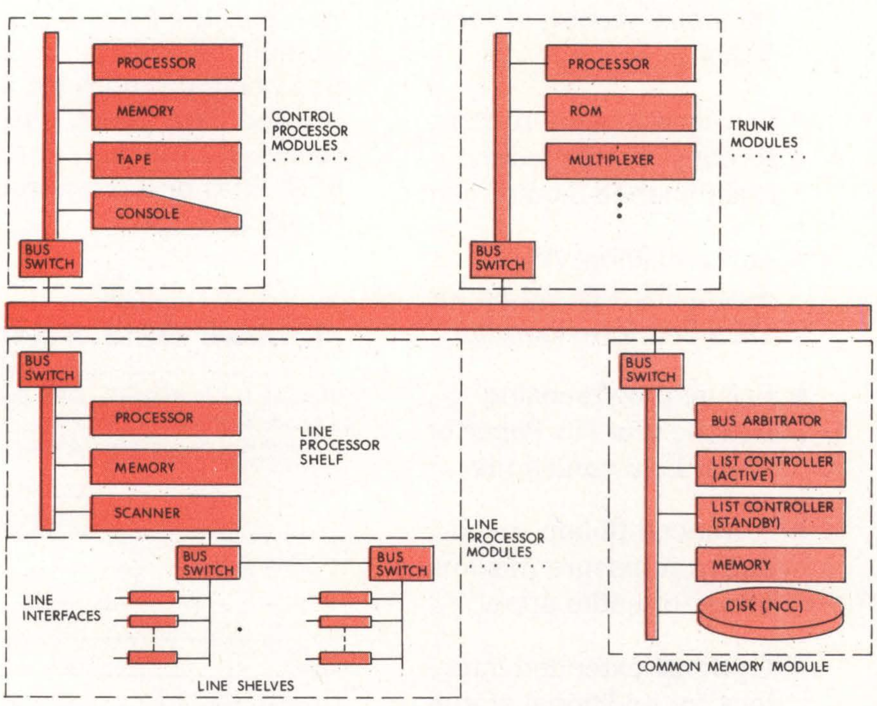
One point stressed is the fact that the state of our knowledge on the reliability of common carrier systems and facilities, and of the techniques for modeling this reliability, are far from satisfactory. A number of possible causes of system failure were examined in switching systems, long- and short-haul carrier systems, as well as probable causes of short-term failures and of long-term outages.

Private line and direct-distance dialing (DDD) circuits were also examined. Private line characteristics are relatively stable; impulse noise is greatly reduced, and line-conditioning can provide more nearly ideal frequency response. However, inexplicable anomalies can occur; for example, a private line in the UK has exhibited a bit error rate (BER) of 2×10^{-5} on Wednesdays and a BER of 3×10^{-7} on Thursdays! AT&T's Digital Data System (DDS) is a special class of private line, too new, relatively, to provide much information on its reliability; but performance goals of DDS systems are good: BERS of 10^{-7}, 99% error-free seconds, and 99.96% availability. All these statistics are far superior to those of current analog systems. Characteristics of DDD lines tend to vary dramatically from call to call.

Impact of common carrier reliability on computer communication systems depends on the type of system being contemplated. The impact is most critical on systems that rely heavily on stringent response times, where occasional failures to obtain a response in a brief time period cannot be tolerated.

Datapac Design Considerations

Datapac is one of the world's first public packet-switched data networks, opened by the Trans-Canada Telephone System (TCTS) early in 1977, and has nodes operating in



Nodal processor, prime Datapac network component. SL-10 data network processor is manufactured by Northern Telecom Ltd; each is a multiprocessor machine using configurable set of functional units designated line, trunk, and control processors, arranged on a common bus structure. High speed trunks interconnect processors to form call-based packet-switching network. One processor is used as a network control center (NCC) to provide centralized control, maintenance, and support. Failure of any individual processor will not result in loss of availability of node

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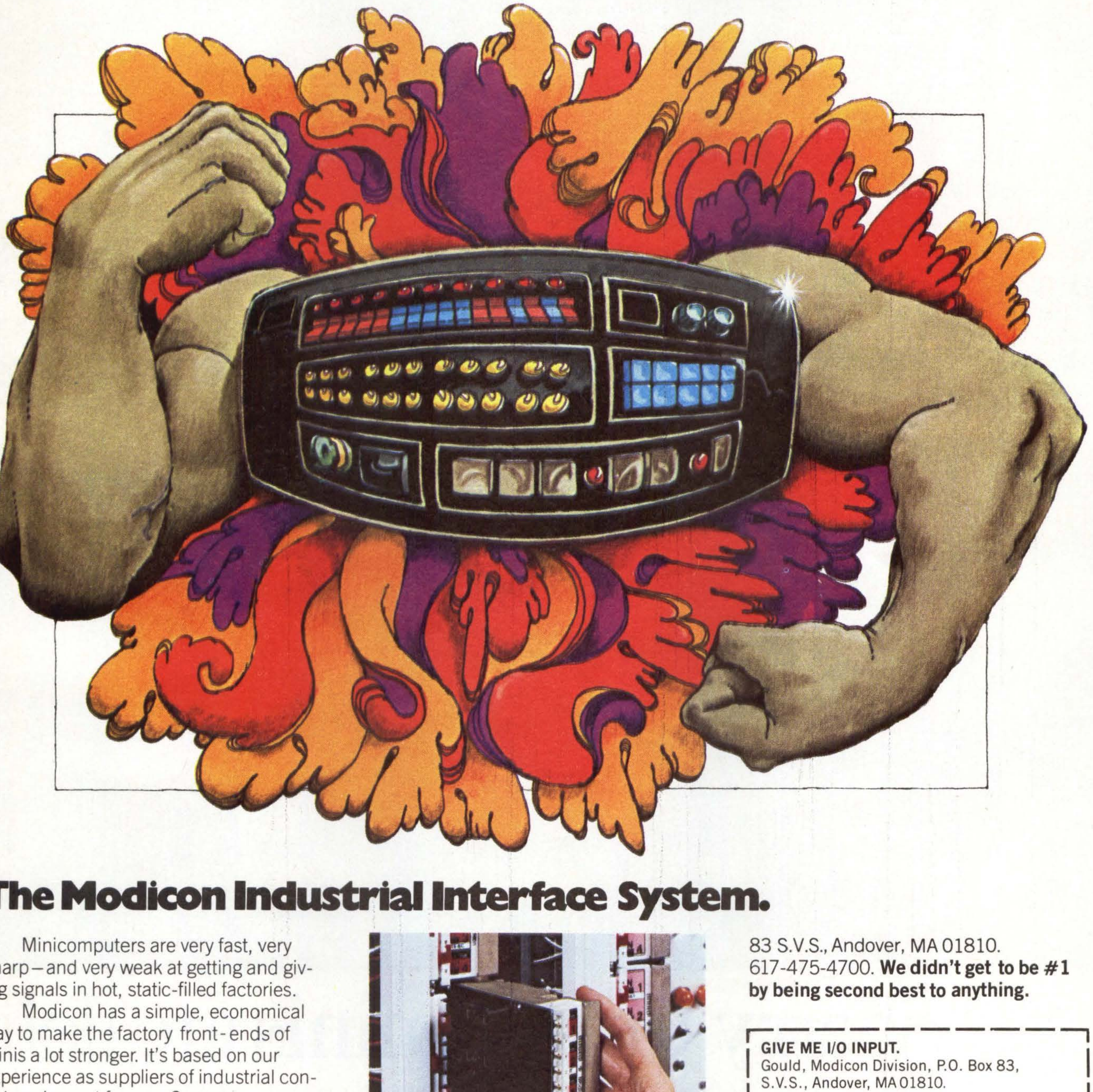

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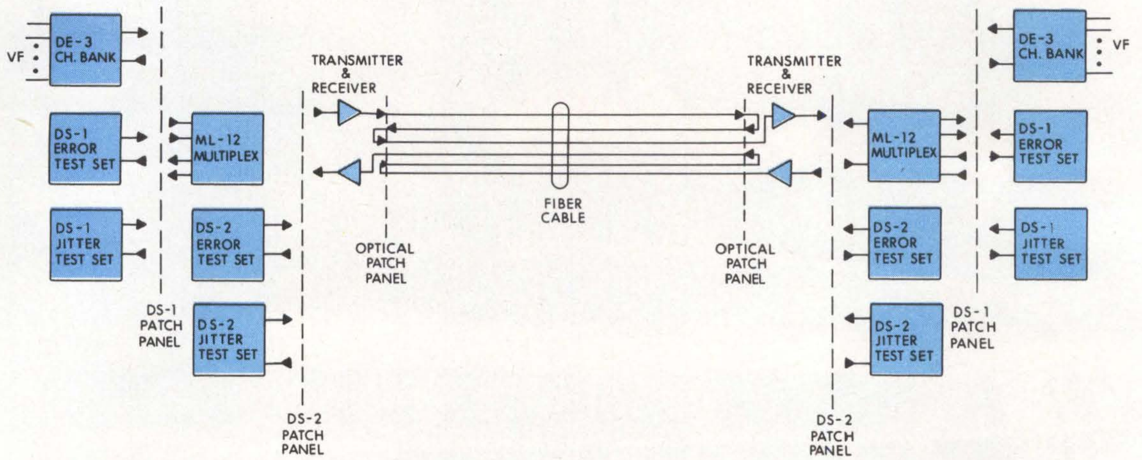

Trial system block diagram. Actual cable length between terminal sites is 1.42 km; cable test lengths of up to 6 km were achieved by looping signal back and forth using connectorized fiber jumpers on optical patch panels at terminal sites. Burrus-type LEDs are used in transmitters and PIN photodetectors in receivers. Fibers are graded-index type, extrusion-coated with plastic for protection

four major centers.[2] The network was developed by Bell Northern Research (BNR) for the Computer Communications Group (CCG) of TCTS. A network such as Datapac must provide a high level of availability for all users, a prime consideration in the network's design and operation.

Many considerations given to design and operation of a public packet-switched network can contribute to high availability and reliability. An economic balance among all these factors—hardware, base software, subnet, customer applications, operating and administrative procedures—is more important than excellence in any one area. As an example, the high reliability of a specific component is redundant if, when it might fail, the resultant outage is excessive due to poor maintenance procedures or faulty diagnostic capabilities. On the other hand an intelligent network can maintain high availability in the presence of poor component performance, either by the use of redundant components or by error detection and correction techniques.

Reliability Modeling

A set of data was collected from operational data communications systems in Western Europe and North America, in order to model reliability of a communications line.[3] Probability distribution functions for line availability and duration of failures resulted in a rule-of-thumb summary of a line. The results indicate a wide variation in line availability—from 99.9% to 10%. Many line failures observed were repaired in a few minutes, but some persisted for more than ten hours. A rule-of-thumb for a line selected at random to transmit data at 2400 bits/s indicates that bit errors will occur about every 40 s; failures lasting 1 min will occur every day; and a 1-hr failure will occur each month. Since the data were gathered from several countries, the results appear to be indicative of telephone lines' performance throughout the world.

The model finds utility in the design of data communication systems. The great variations in performance indicate the uncertainty associated with making design decisions for systems where these lines serve as key components.

Fiber Optic Systems

Trial System in Montreal

In October 1977 an exploratory fiber optic trial system was installed in the interoffice trunk network of Bell Canada in Montreal, connecting two switching centers approximately 1.5 km apart. Cable was 0.5" (1.3-cm) dia, 6 fiber; conventional underground conduit was used. During installation direct pulling through manholes was made, indicating feasibility of long cable pulling. Individual splicing of fibers was successfully carried out in three of the manholes along the route. Average attenuation of the installed cable, including splices, was about 7 dB/km.

Digital signal transmission has been tested over the system since installation at the standard DS-2 rate of 6.312M bits/s, for 96 voice channels. Original performance objectives have been met or exceeded; further testing of video and higher bit rate transmission, and routing of line traffic over the system will be carried out in the near future.[4,5,6,7]

30-Channel Fiber Optic Data Transmission System

This system was designed to operate with the Defense Satellite Communication System (DSCS) ground station in Waihiawa, Hawaii. Here the antenna facility is located about 7000 ft (2.14 km) from the processing facility. To connect the two sites 30 channels were provided, each capable

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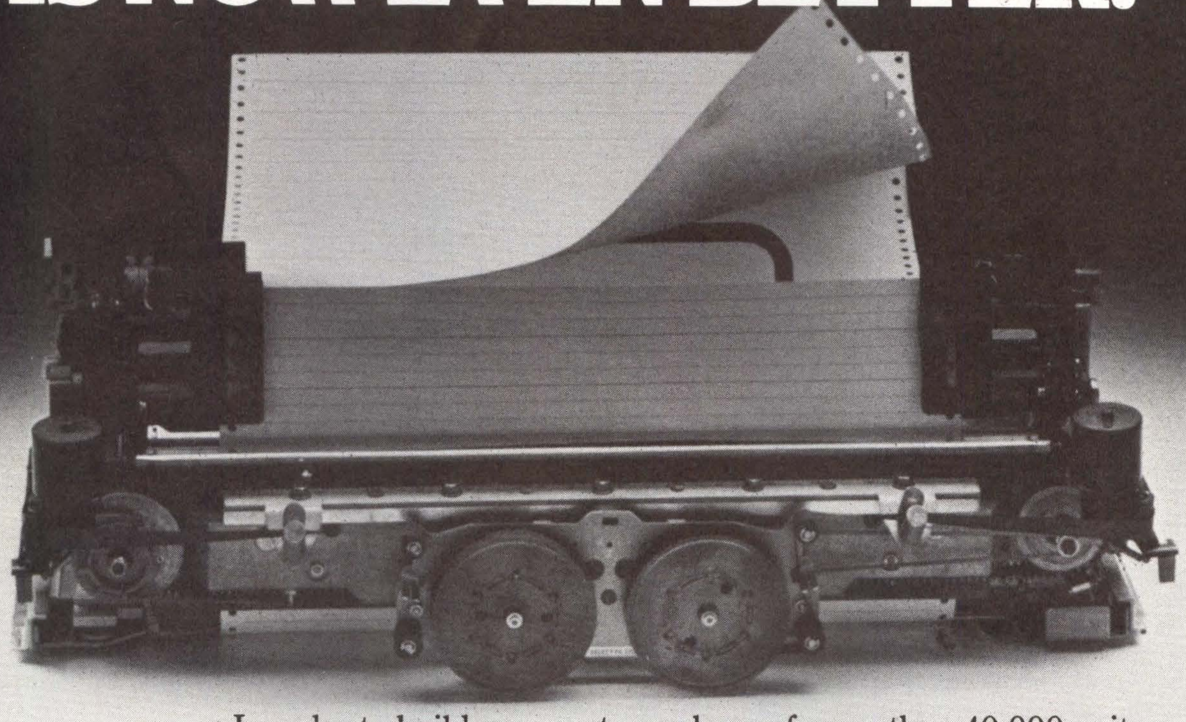

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of data rates up to 20M bits/s (NRZ-L line code). A comprehensive summary of the data channel performance is given in the Table.

This project demonstrates that operational, multiple channel, wideband fiber optic data transmission systems can be readily produced. As the price of fiber optic components continues to come down, more and more similar applications will find the technology an attractive choice on economic grounds alone.[8]

TABLE

Data Channel Specifications

Data rate	20k bits/s to 20M bits/s
Bit error rate	$<10^{-8}$
Mean time between failure	
0-50 °C	>5000 h
Input/output electrical signal	Standard TTL
Data format	NRZ-L
Output electrical signal-digital	
Rise/fall time (1)	<15 ns
Pulse spread (2)	<20 ns
Output electrical signal-analog	
SNR (3)	>30:1
Peak-to-peak voltage (4)	4 ± 1 V
Rise/fall time (1)	<25 ns
Pulse spread (2)	<15 ns
Overshoot	<10%
Droop (5)	<10%

(1) 10% to 90% peak-to-peak amplitude
(2) Change from input pulse width to output pulse width measured at 50% points
(3) Ratio of peak-to-peak 10-MHz square wave signal amplitude out of 10-MHz filter to rms noise out of filter with source constantly on
(4) Measured across a 1-kΩ load
(5) Measured for 100 consecutive logic ones at 20k bits/s, NRZ

Integrated Networks

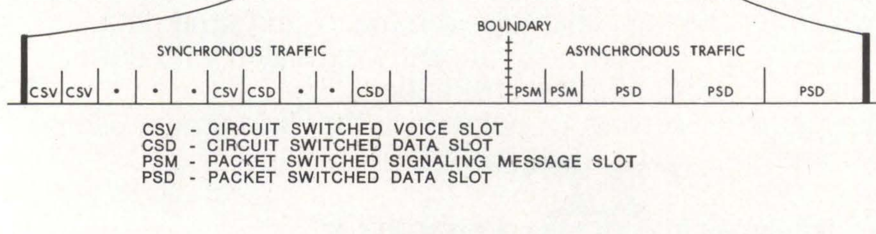
Advances in voice digitizing techniques, as well as in the packet switching concept for data communications, and the relative inefficiency of conventional switching techniques for diverse traffic applications, have focused attention on integrated networks. One paper[9] addresses integrated switching networks as being justified by more efficient utilization of transmission facilities which result from matching the switching concept to the traffic characteristics. A technically viable candidate for the integrated switching superstructure is a synchronous time-division multiplexed frame technique (see Figure).

A design procedure is presented, representing efforts to extend known techniques in the design of circuit- and packet-switched networks to this new area. Cost/performance studies are carried out in the areas of fixed vs movable frame management policies; cost sensitivity to design options; and cost sensitivity to switching alternatives.

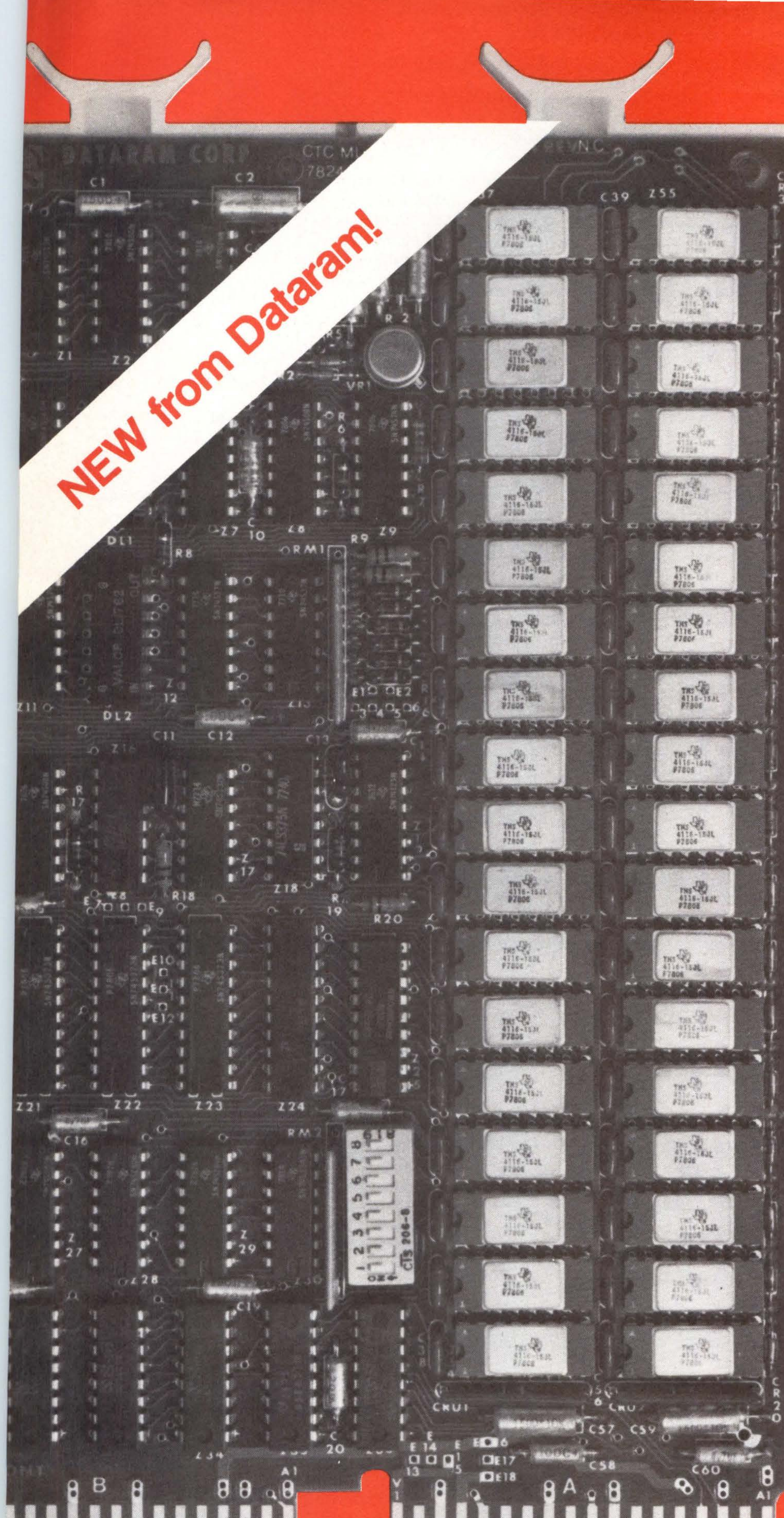
Network Analysis

To cost-effectively determine the number and locations of network access facilities, such as multiplexers, concentrators, packet switches or satellite earth stations, in a hierarchically-structured data/computer communication network, has been generally regarded as theoretically difficult and computationally complex, even for heuristic approaches. An algorithm has been developed that is effective, flexible, and computationally efficient.[10] Through its implementation, various heuristic techniques, taken independently or in combination, have been evaluated in determining optimal topological designs.

Based on results in applying the *add*, *drop*, *exchange*, and *merge* techniques, the *drop* was judged to be the most effective alone than any of the other techniques in combination. Use of more than one heuristic technique is recommended however, to insure that certain pathological cases which may come under evalua-



Example of hybrid switching channel structure illustrating channel multiplexing on an integrated link. Under fixed boundary frame management, partition of link capacity between circuit-switched and packet-switched traffic is fixed. Under movable-boundary management, packet-switched traffic can dynamically utilize idle circuit-switched slots



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tion do not result in a less than optimal solution.

Computer Communication Design and Analysis

Loop Systems

The feasibility of a loop system for local data concentration, in an environment restricted to a single building with up to 150 terminals, was considered.[11] Computer communication networks, such as ARPA, CYCLADES, and DATAPAC, allow users at local terminals access to information stored in a remote computer. With the bursty nature of terminal traffic, it is economical to connect a group of local terminals to a data concentrator, which acts as an interface to the network, in either a point-to-point, multidrop, minimal spanning tree, or loop configuration. In this examination of the latter organization, reliability and performance of three simplex loop systems, ranging from de-centralized to centralized are studied.

Another paper on loop systems described a microprocessor-based controller for a computer communication switching system comprised of a number of stations connected in a loop.[12] At each station a controller is used for protocol management—the established protocol being High Level Data Link Control (HDLC). A prototype controller allows verification and demonstration. A brief description of the use of a loop as an extension for an X.25 network was also given.

Communications Privacy

Aspects of the effects of recent technological development, especially the development of large semiconductor memories, on enciphering techniques were examined.[13] Evidence was presented for the case that the relatively recent availability of inexpensive semiconductor memories and microprocessors is overwhelmingly to the advantage of the cryptographer in his never-ending battle with the cryptanalyst. With the availability of cheap, powerful computing hardware and the right theoretical tools, the development of practical cryptographic systems which are computationally secure, becomes possible.

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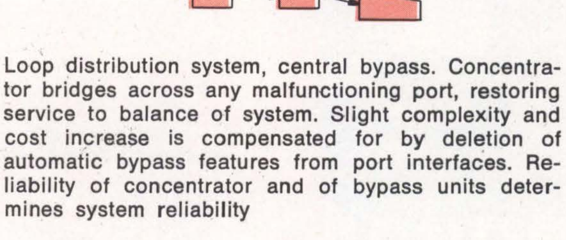
13. R. Rivest, "The Impact of Technology on Cryptography," Vol III, 46.2



Loop distribution system, central bypass. Concentrator bridges across any malfunctioning port, restoring service to balance of system. Slight complexity and cost increase is compensated for by deletion of automatic bypass features from port interfaces. Reliability of concentrator and of bypass units determines system reliability

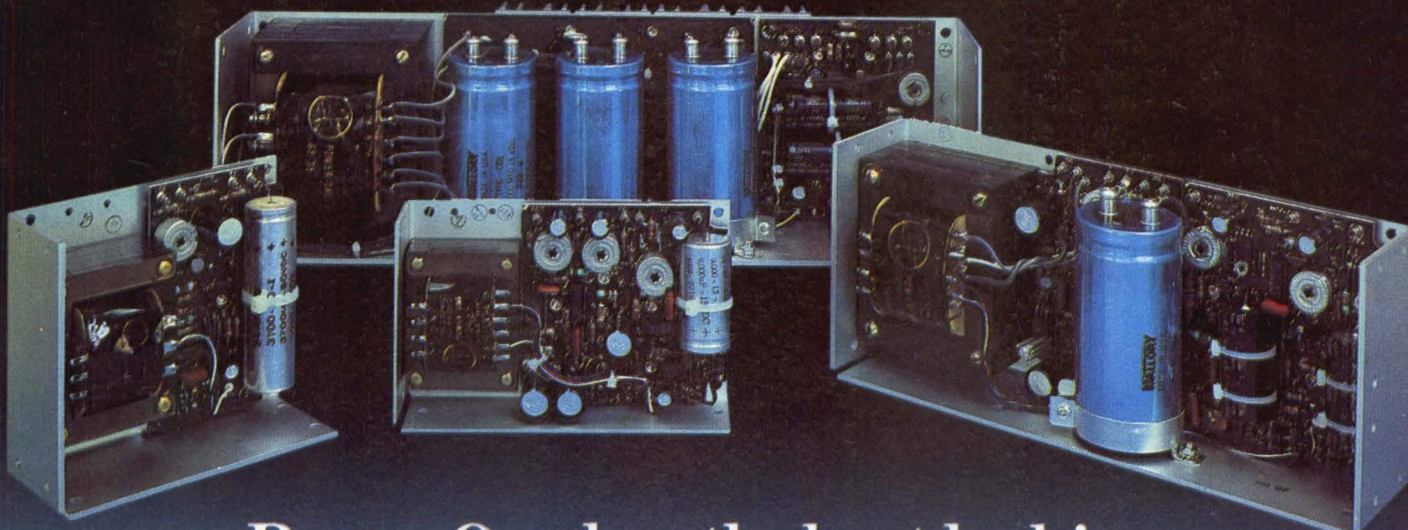
As stated, the above is necessarily a broad-brush treatment of the excellent presentations at ICC '78. Copies of the 3-volume ICC '78 *Conference Record*, containing the full text of the sessions, are available from: IEEE Single Copy Sales, 445 Hoes Lane, Piscataway, NJ 08854. Order by IEEE Catalog Number (78CH 1350-8 CSCB) and title. Price is $50 each set of three volumes. Standard discount is available for IEEE members.

Support Processor Adds Remote Batch Capabilities To 360/370 Mainframes

An attached support processor enables users of IBM 360/370 and equivalent computers which lack teleprocessing features to implement remote batch telecommunications functions. Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, says that DASP™ permits any application that may be executed on a

"Talk about

OPEN FRAMES



Power-One has the best looking power supplies in the world.

(...but who really cares.)

We suspect you share our feelings. We all admire superb craftsmanship and clean, efficient design. However, compared to performance, price, and reliability, "good looks" has to take a back seat.

But isn't it nice to find products like Power-One open-frame power supplies that actually offer *all* these desirable features? The good looks you can see for yourself, so let's talk about what really counts.

Talk about prices...it's still 1973.

It's true. 95% of our standard models are priced the same today as they were five years ago. Take our B case models, for example. In 1973 they sold for $24.95. Today, they're *still $24.95... and holding!* Amazingly, Power-One open-frames were price competitive in '73. Think what they are today.

Talk about reliability...we burn them in so they don't burn out.

Every single unit bearing the Power-One label undergoes a full functional test, followed by a 2-hour burn-in, plus a final full functional test. We repeat — *every single unit!* Compare this to other manufacturers who conduct only a single operational test. That's why no other open-frames match ours for long life and overall reliability.

Talk about selection...we have 84 standard models.

Without a doubt, Power-One has the broadest selection of "off-the-shelf" open-frames in the industry — 84 different models. Single outputs, duals and triples... plus new Floppy-Disk and Microprocessor series. And these are all off-the-shelf *standards,* ready for delivery when you need them. Last year alone, we delivered over 100,000 of these standards — on time! That makes Power-One the largest producer of open-frames in the world.

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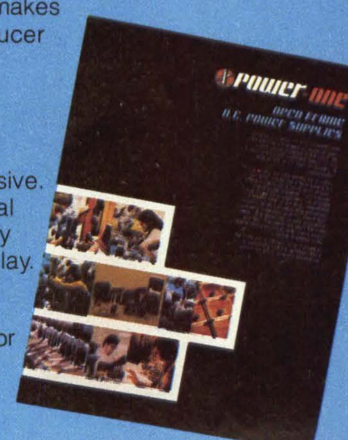
It's all new, and all inclusive. Complete specs, dimensional drawings, and prices on every standard model. So don't delay. Get your free copy now.

Also, for off-the-shelf delivery in your area, call us for the location of your nearest Power-One distributor.



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CIRCLE 12 ON INQUIRY CARD

TEST DATA

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...and this FULL LINE of low-profile R-N ICL sockets is priced very, very competitively.

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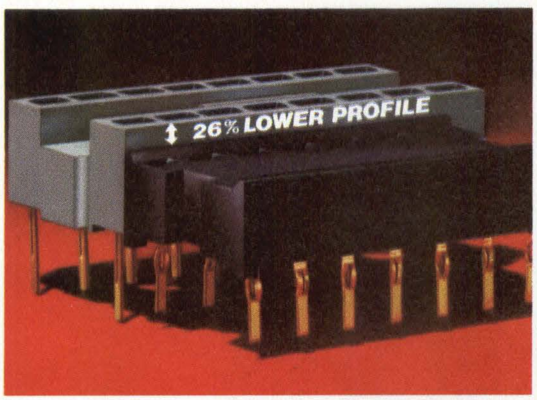
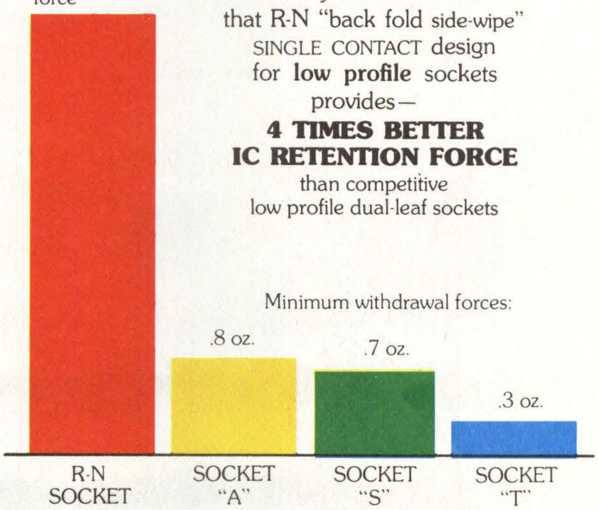
low profile DIP socket MYTH

"...TWO contacts are not more reliable than ONE!"

Surprisingly, a **low profile** (.150" high) DIP socket is a different breed of cat when it comes to engineering in contact reliability. Most standard DIP sockets have dual contacts. (R-N's dual "side-wipe" contacts are among the most reliable in the industry.) But, when you **shorten the contact length** to achieve the "low profile" you lose a great deal of contact force and IC retention strength. So, to achieve effective low profile socket reliability you must **redesign the contacts** and make them out of the **strongest contact material available.**



Low .150" profile of ICL socket reduces board density by 26%.



Fat-Skinny **TESTS PROVE*** that R-N "back fold side-wipe" SINGLE CONTACT design for **low profile** sockets provides—

4 TIMES BETTER IC RETENTION FORCE

than competitive low profile dual-leaf sockets

* In "Fat-Skinny test," withdrawal forces are measured using the smallest size (.008") lead **after** insertion of **largest** size (.012") lead.

Representative NORMAL FORCE Test Scores for 10 R-N ICL low profile sockets

TEST SOCKET	NORMAL FORCE *
1	410 grams
2	465 grams
3	480 grams
4	465 grams
5	395 grams
6	425 grams
7	465 grams
8	395 grams
9	410 grams
10	425 grams

AVERAGE—430 grams

This force is 4 to 5 times greater than average dual contact socket NORMAL FORCE

* NORMAL FORCE means force perpendicular or at right angles to IC lead. The single ICL contact exerts this kind of force against the IC lead when inserted into the socket.

WRITE TODAY for latest R-N "Short Form" Catalog of R-N production DIP sockets. Contains full specs, dimensions and material data. Get yours now.

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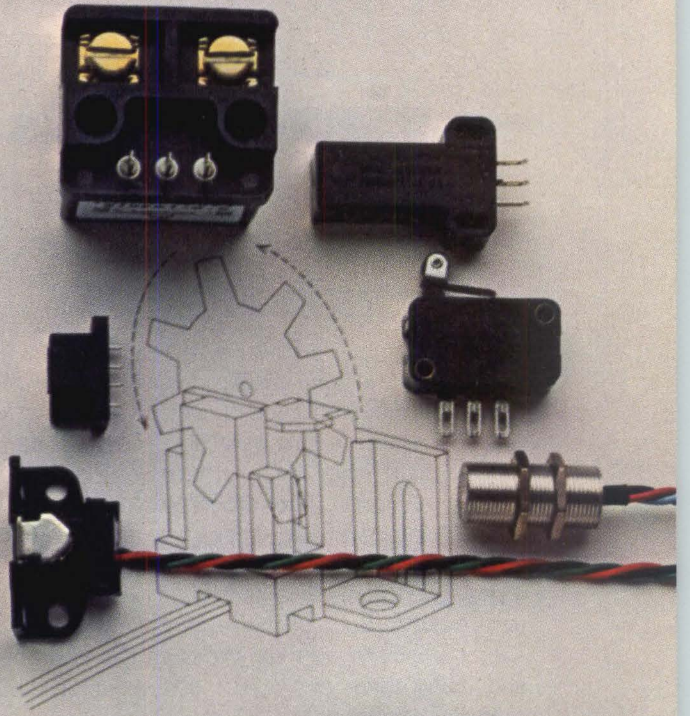
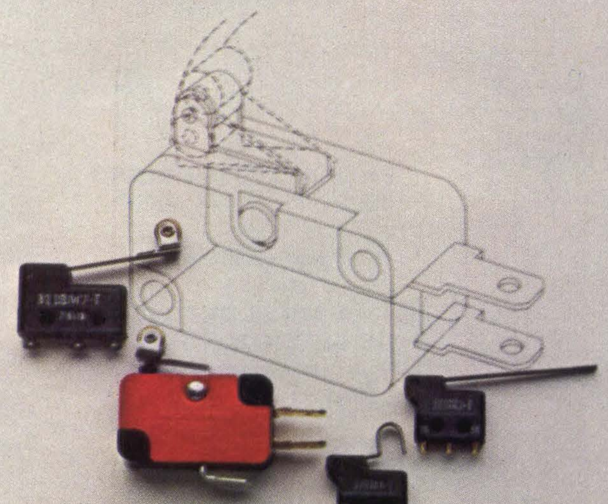
CIRCLE 13 ON INQUIRY CARD

Some of these components will probably never
The others will just come close.

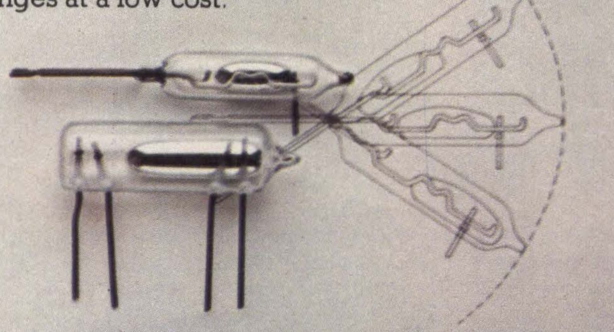
The SR, XL, XK and AV are solid state position sensors featuring almost infinite life. All offer zero speed operation with some up to 100 Khz. ES current sensor utilizes Hall-effect IC and protects against damage from short circuits or overcurrent conditions.





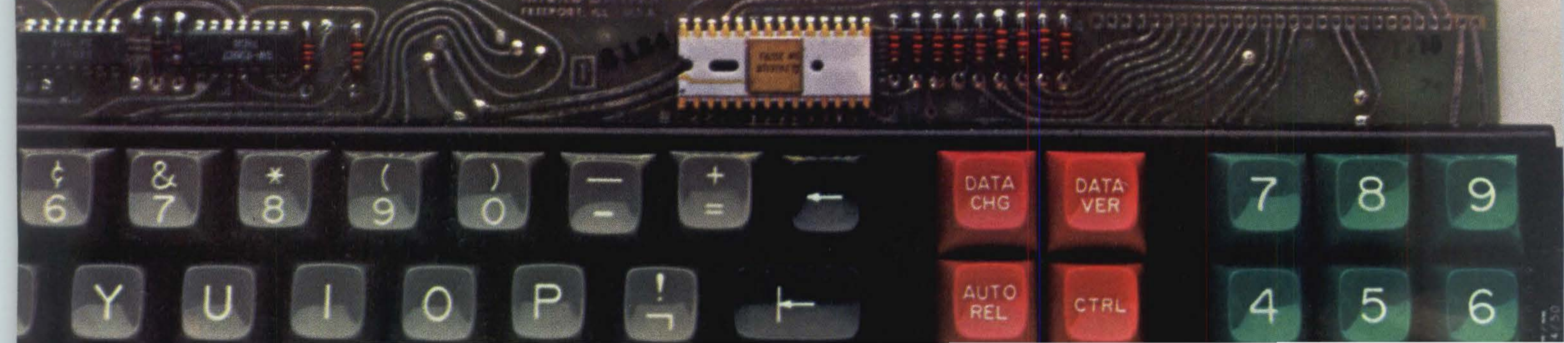
Snap-action V3, SM and SX switches offer wide variety of actuators, electrical capacity and termination.

Mercury switches offer hermetic sealing, a variety of electrical capacity and broad temperature ranges at a low cost.



AML manual devices for low installed cost, electrical flexibility and attractive panel appearance. Series 8 miniature manual switches provide small size and wide variety of operators. DM offers inexpensive snap-in panel mount design.

Solid state keyboards provide high reliability no mechanical keyboard can offer. Panel sealed versions also available.



wear out.

The solid state keyboard, AML lighted pushbuttons and sensors you see here will probably never wear out. Because they're all solid state.

Each is based on a Hall-effect integrated circuit. A circuit that's been tested through billions of operations without failing. And proven by performance in thousands of applications.

The precision electromechanical components you see here come close. Simply because of the careful way they're designed and put together.

Like the long-life versions of our snap-action V3, SM and SX precision switches. Available in a wide variety of sizes, electrical ratings, terminals, actuators, contact forms and operating characteristics—some tested to a mechanical life of over 10,000,000 operations.

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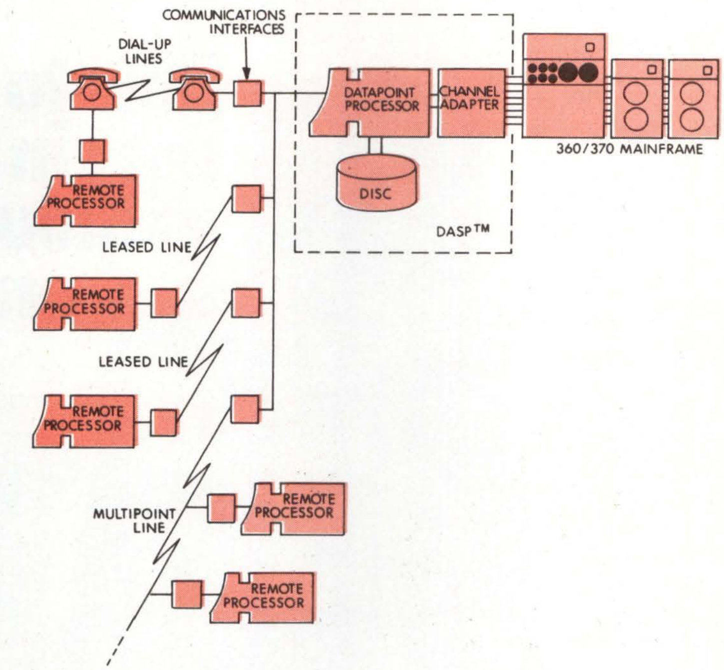

Datapoint Attached Support Processor. DASP™ spools data to its own discs while submitting jobs or accepting completed output through byte multiplexer channel of IBM mainframe. Remote jobs may be submitted to or completed jobs retrieved through systems while mainframe is on other tasks or even completely offline

360/370 to be submitted to it for processing via telephone lines from a distant location. The processor appears to the system it serves as an IBM card reader or punch, line printer, and alternate system console. It can handle thousands of records per minute, requires no IBM teleprocessing hardware or software, and adds no telecommunication or disc retrieval overhead to the IBM system to which it is attached.

Comprising hardware and software components, the processor simultaneously controls up to four telephone lines, in any combination of multipoint, leased point-to-point, or direct dial, and operates at speeds up to 9600 baud. Depending on calling volume, any number of remote sites can be accommodated; additional units can be attached should volume exceed that of a single system.

Time-stamped output and routing feature permits job-entry user to specify who receives completed output, at what time, and delivery method—autodial, polling, or dial-in. An administrative message-switching feature includes storing and routing of administrative messages, memoranda, or data files from any terminal to any other. Messages may be stored and forwarded at night when DDD rates are low. System also compiles statistics by both line and remote processor to support individual billing and accurate system analysis.

Disc storage capacities range up to 160M bytes. A system consisting of an Advanced Business Processor, 5M bytes cartridge disc storage, channel adapter, and all software is priced at $37,500, or may be leased for $1044/mo on a 3-yr basis.

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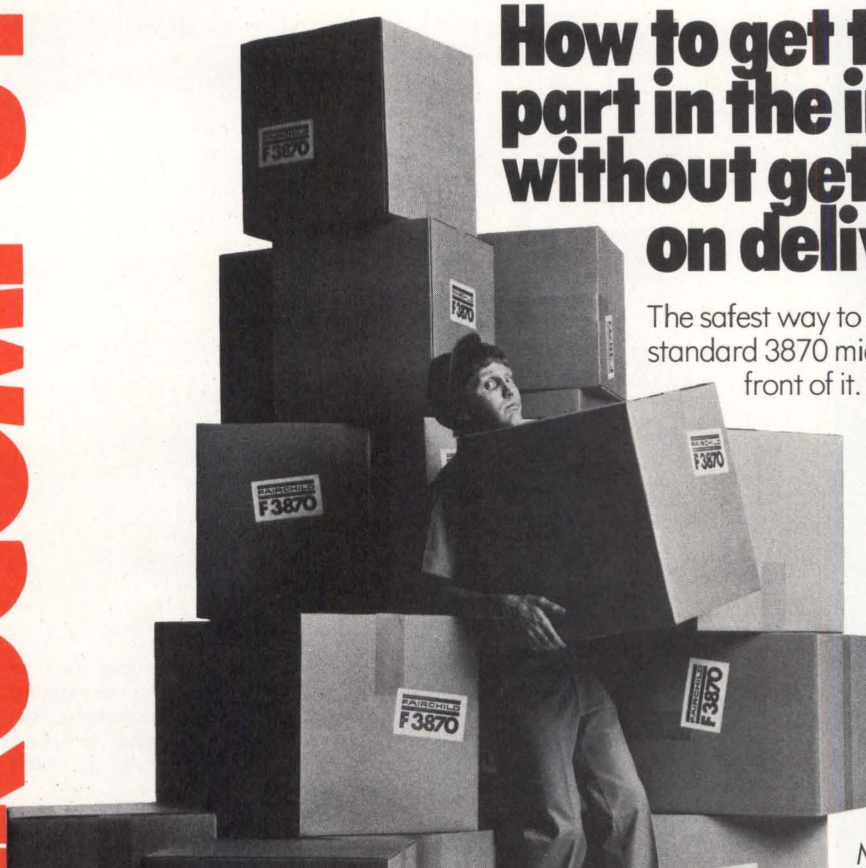
F3870 MICROCOMPUTER

How to get the hottest part in the industry without getting burned on delivery.



The safest way to order the new industry standard 3870 microcomputer is to put an F in front of it. Because Fairchild has more microcomputer capability than anyone else. And we're putting it all to use on the F3870.

So when you order from us, you're getting the most advanced process and production capability in the industry. Which means on time delivery at the lowest possible cost.

It's all due to a technology that's years ahead of its time. We're on-line with a MEBES-Micro Electron Beam System for mask making — an industry first. We've got 4" wafers. And improved projection alignment. All of which adds up to lower cost.

Like money in the bank.

The F3870 saves you money in several ways: It's got an inexpensive + 5 V ± 10% power supply that requires less power.

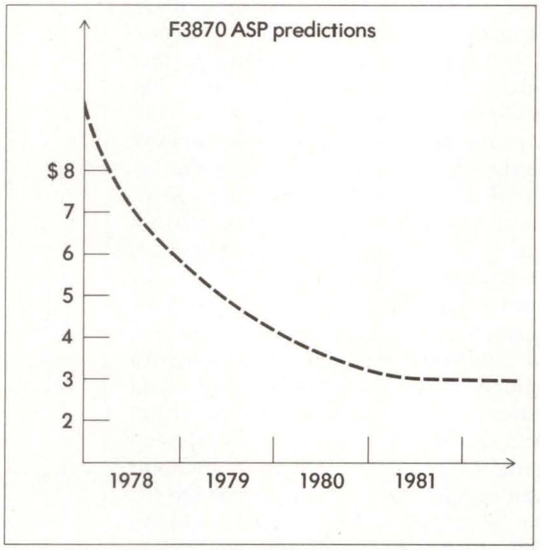
It's got a 40-pin plastic DIP that reduces device cost.

And F3870 pinouts are optimized to allow single-sided pc boards. This makes the connections easier and the pc boards cheaper.

All of which means economy for you with no sacrifice in performance.

Million dollar performer.

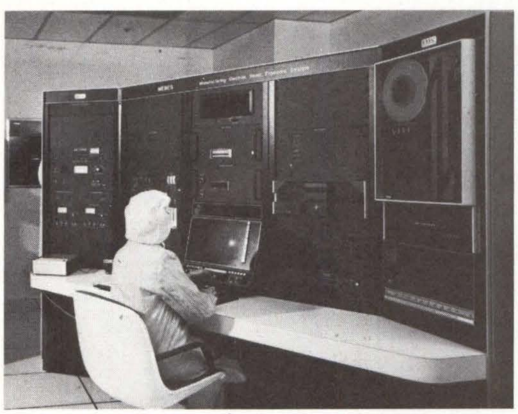
The F3870 delivers higher performance than other single chip microcomputers. It's organized 2K x 8 mask programmable ROM and 64 x 8 scratchpad RAM. With 32 bi-directional individually controllable I/O pins, a programmable binary timer and prioritized vectored interrupts.



Time vs. cost comparison graph.

It has an 8-bit processor, 72 instructions, output ready strobe, programmable internal and external vector interrupts and on-chip clock.

There's also on-chip regulated back bias generation and triple ion implanted n-channel technology. And the F3870 is fully software compatible with our entire F8 multi-chip family.



MEBES-Micro Electron Beam System.

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The F3870 family is expanding so you can take advantage of its cost savings now and still add intelligence and flexibility to your future designs.

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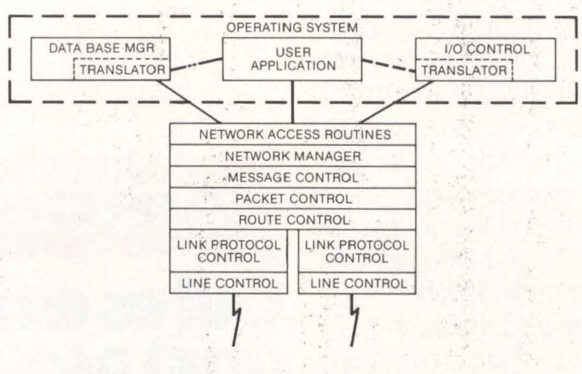
Distributed Networks Complemented by Packet-Based Architecture

A resource-sharing distributed data processing system called Network Data Series (NDS) and complementary AUTONET™ network architecture have been introduced by General Automation, 1055 South East St, Anaheim, CA 92803. They will be used to configure the company's Solution series compatible 220 and 460 computers into resource sharing distributed data processing networks in production automation functions. Data base sites and system resources are transparent to NDS applications programs; users have access from any network terminal.

Typical 460 NDS host systems can include 128k to 2048k bytes memory with error correction, and support up to four discs in 10M, 80M or 300M byte capacities, up to two 200-, 300-, or 600-line/min printers, 400- or 1000-card/min readers, up to four 800- or 1600-bit/in (315- or 630-/cm), 25/75-in/s (64/190-cm/s) mag tape units, and console serial printers. 220-based terminal clusters can accommodate up to four CRT display stations, and can be configured with 10M-byte disc or 200-line/min printer as required. In highly interactive environments with centralized data base, each 460 NDS host can support up to eight terminal clusters for a total of 32 terminals.

AUTONET is based on packet switching concepts from ADCCP (Advanced Data Communication Control Procedures) X.25 recommendations. It uses full duplex SDLC line protocols for message formatting and error correction at rates to over 2M bits/s. The framework can accommodate up to 255 individual network nodes, each with as many as 32 individual communications links. Standard capabilities include asynchronous program-to-program communication; remote control of any processor's operating system; total network management, unattended operation at any node; transparent access to remote peripherals, files, and data bases; memory image uploading; and maintenance troubleshooting on remote systems. Standard modems can be used for communication speeds to 2400 baud, high speed units to 56k baud, or local 460 host links to over 2.5M bits/s. A wide selection of emulators is available to connect the NDS to any other host, including packages for IBM 2780, 3780, and 3270.

First NDS installations will be made in the fall of 1978, with volume production of complete network configurations scheduled for March 1979.



AUTONET architecture

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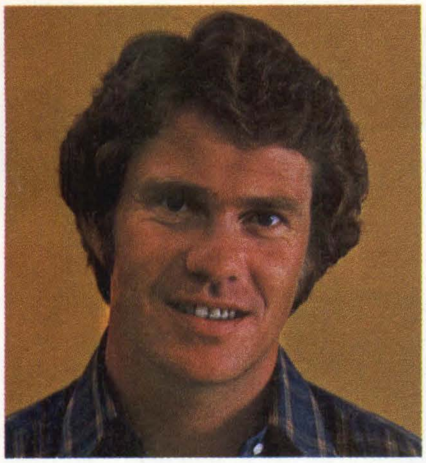

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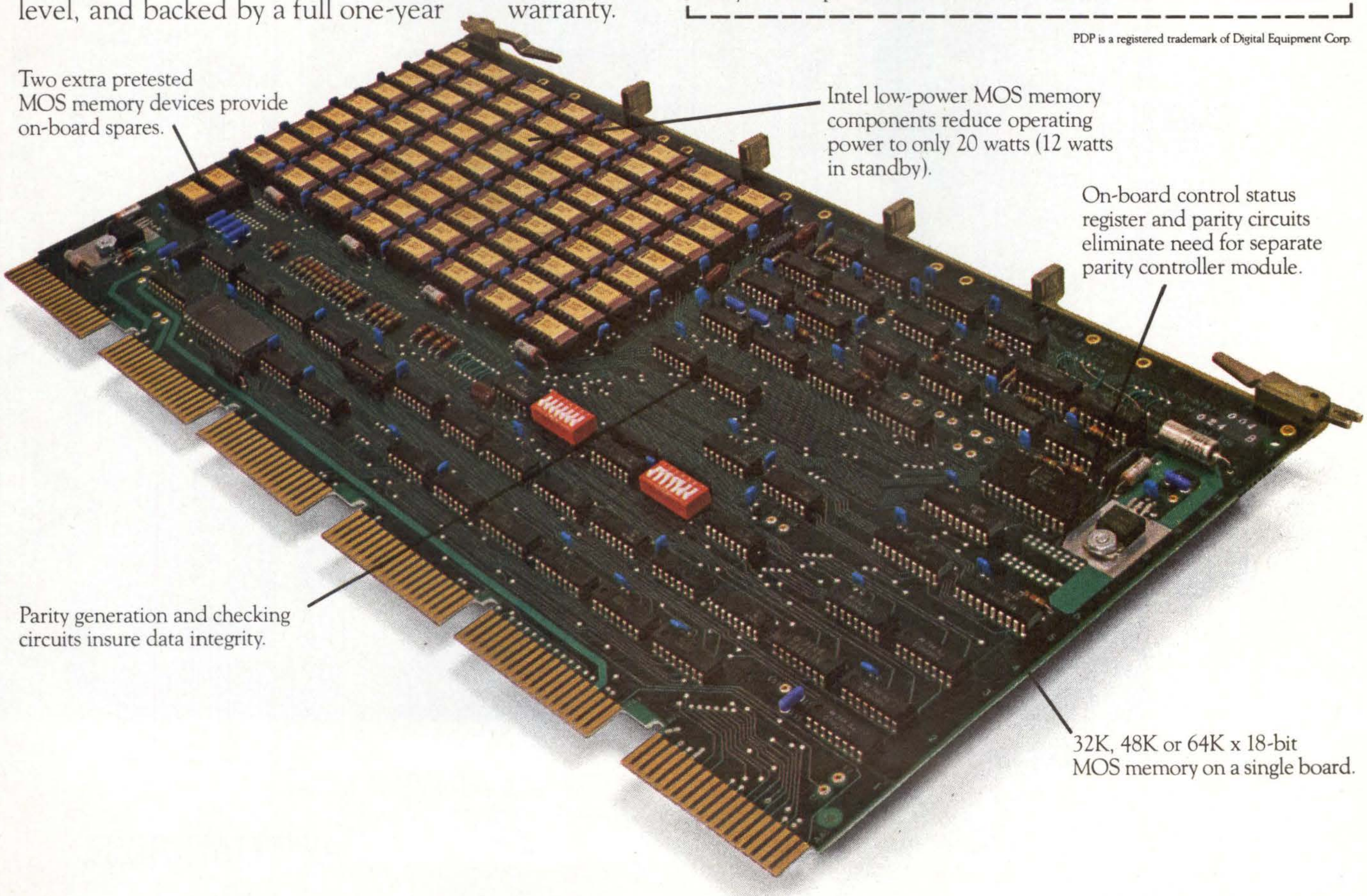

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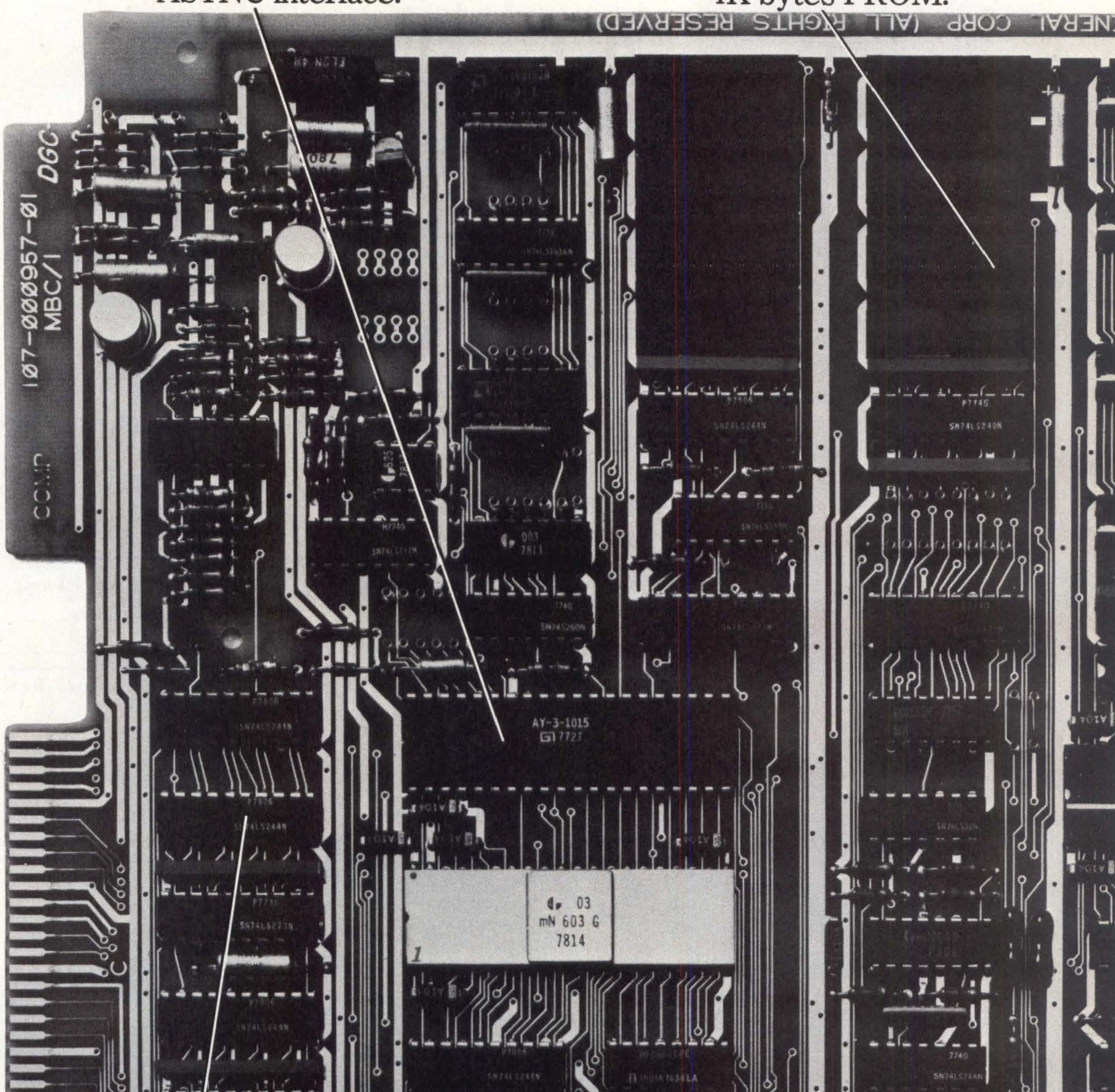

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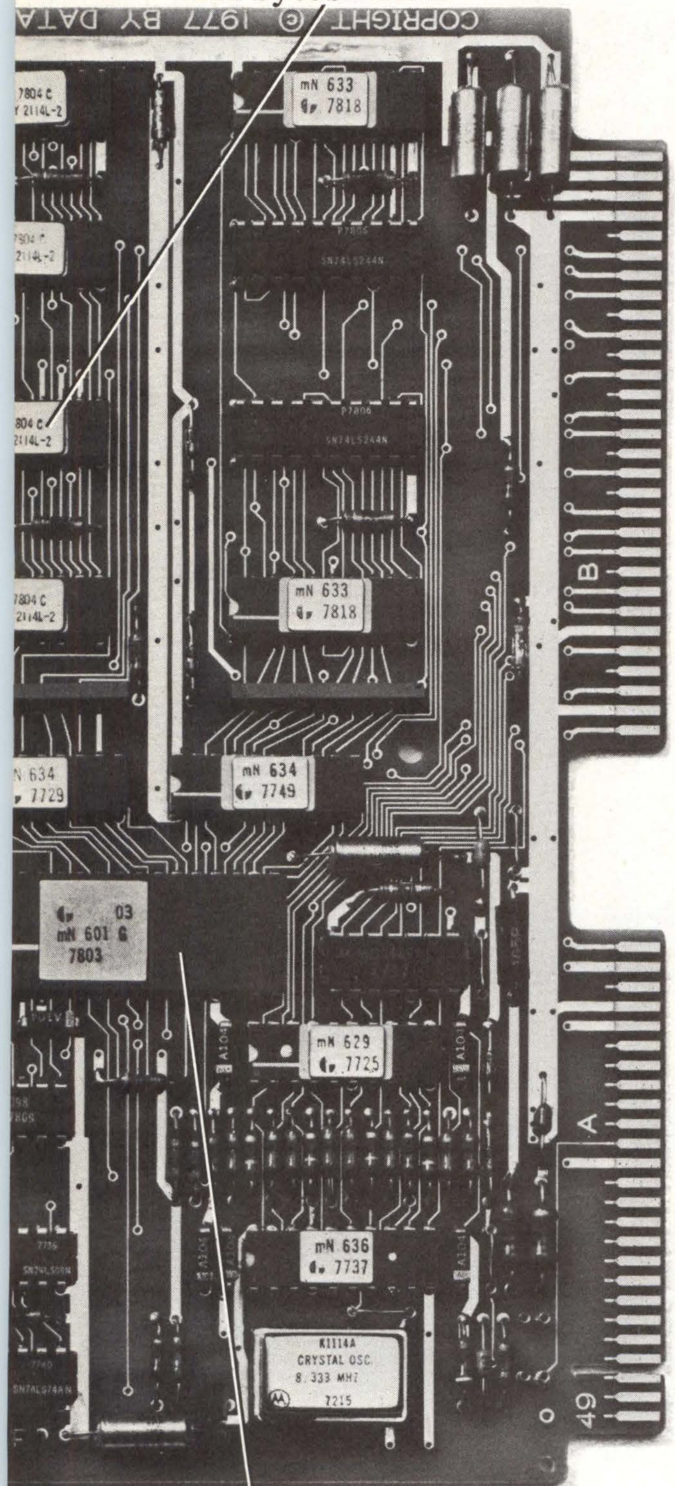
ACTUAL SIZE.

$725.*

2K bytes RAM.



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Introducing the Data General microNOVA Board Computer, MBC/1. The smallest, most functional 16-bit single board microcomputer you can buy. More power and capability in less space than any other. It's a full 16-bit processing unit. And it has multiply/divide, stack architecture, data channel (DMA) and 16-level priority interrupt, 2K bytes static RAM, sockets for up to 4K bytes of PROM. It also has async interface, 32-line digital I/O, optional console debug software and self-test diagnostics. All in a space of 7.5 x 9.5 inches.

It's all supported by our MBC/M real-time multi-tasking monitor and monitor emulator that lets you develop software under Data General's AOS, RDOS and DOS operating systems for execution on MBC/1.

To go along with all of this, there's a full array of compatible interfaces, design interface support, compatible software and excellent program development tools. If you want more board in less room, reserve a Data General MBC/1 microNOVA Board Computer. For more information, mail the coupon, call Data General or your nearest full service industrial distributor: Schweber or Wyle (Elmar/ Liberty). Or call your local dealer.

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Data General

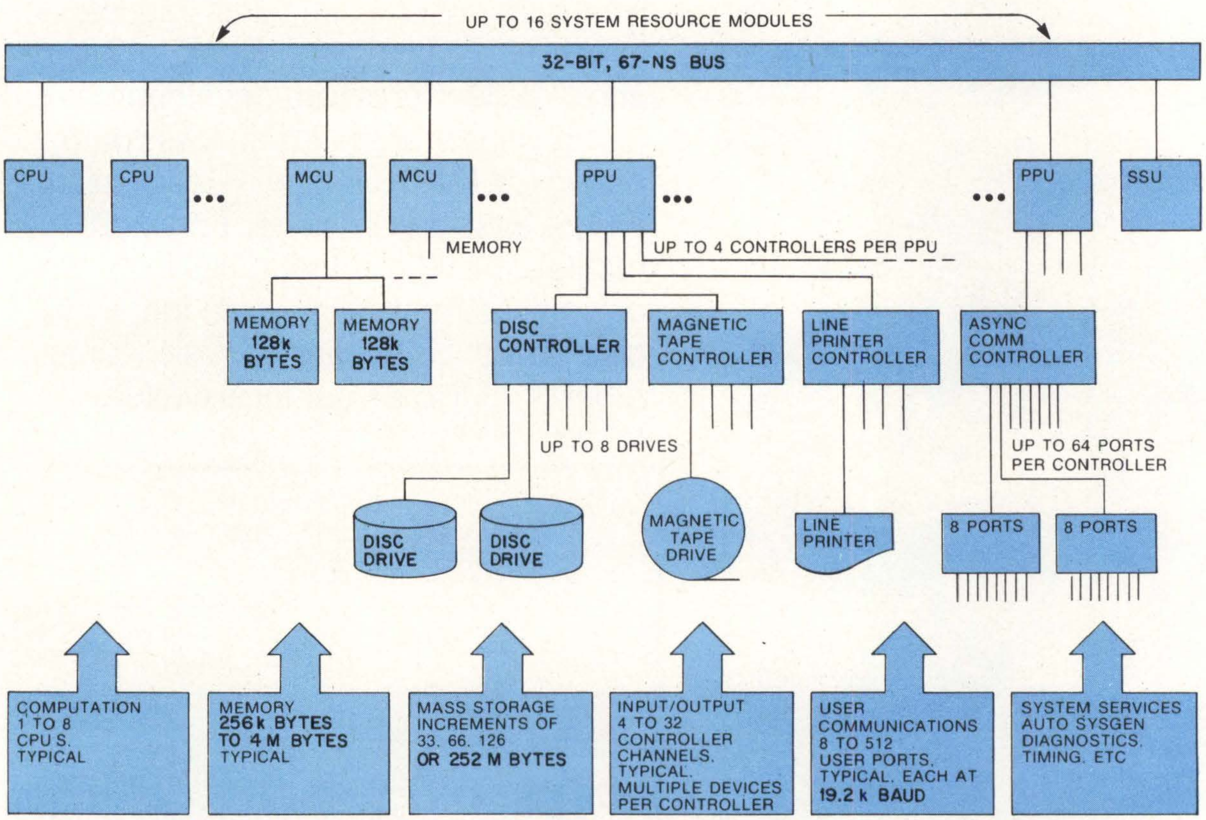
We make computers that make sense.

32-Bit Multiprocessor System Based on Variable Resource Architecture

Model 8000, a 32-bit modular multiprocessor system designed to simultaneously support hundreds of interactive terminals and multistream batch tasks, uses variable resource architecture. This design concept, developed by BTI Computer Systems, 870 W Maude Ave, Sunnyvale, CA 94086, involves multiple modules, all operating in parallel, which provide computational power, memory, and I/O channels in the specific mix needed for a range of configurations, system expansion, and fail-soft capability.

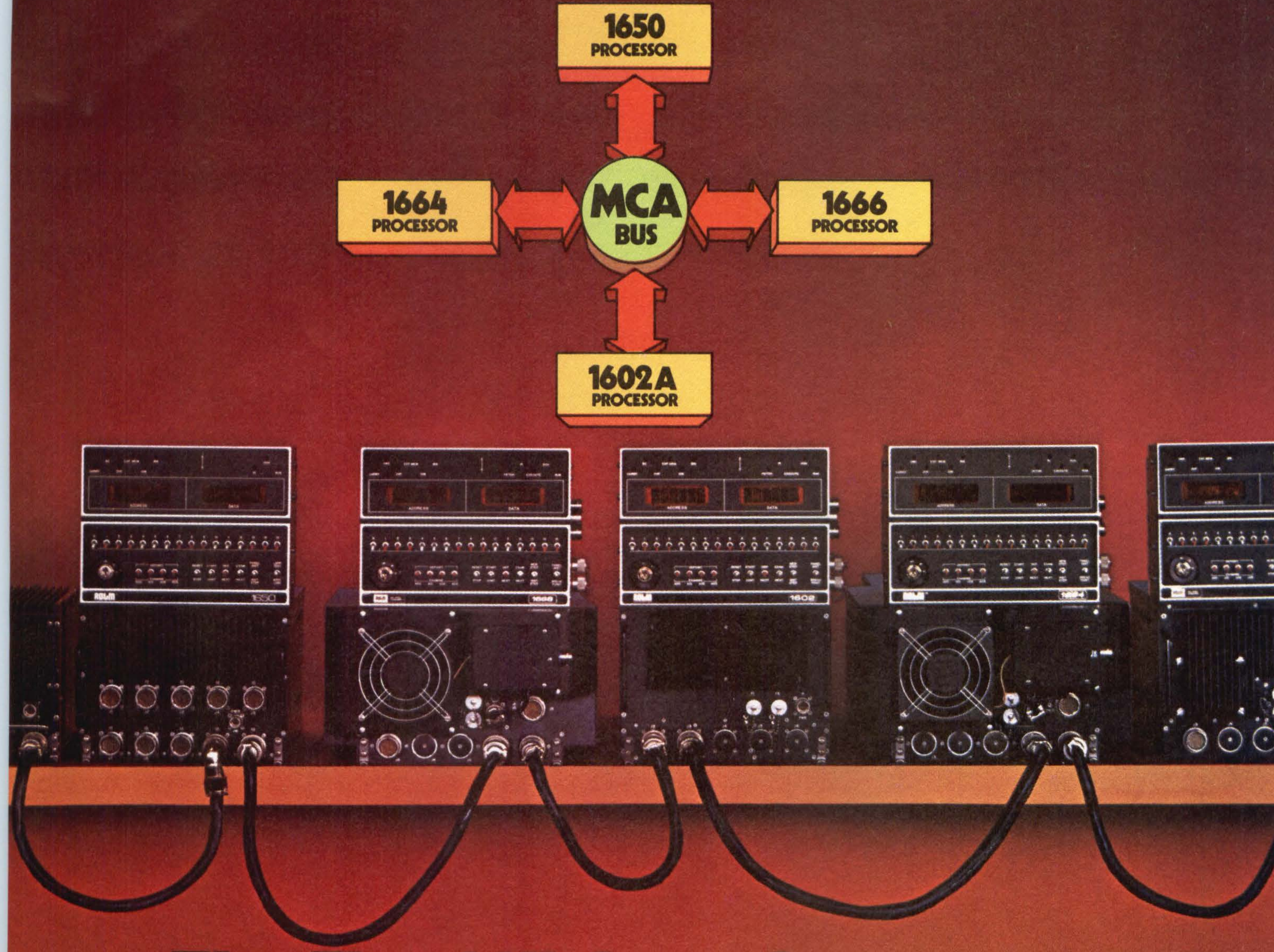
Engineering basis for the design is the high speed, distributed logic master bus, which provides 32-bit communication among up to 16 resource modules at a rate of 60M bytes/s. There are four types of resource modules: computational processing unit (CPU), memory control unit (MCU), peripheral processing unit (PPU), and system services unit (SSU). System configurations can include up to 8 processors operating in parallel, up to 8 parallel paths into a total core memory capacity of 100M bytes, up to 32 I/O channels, up to 512 high speed asynchronous terminal ports, and up to 128 disc spindles with 33M to 252M bytes/spindle.

Key to the system's operation is the virtual machine multiprocessing monitor which creates a standard virtual machine environment for each running program, or process, independent of the mix of hardware modules present in the system. It dynamically supports its varying workload by treating all hardware including the processors as a resource pool. The specific mix of peripherals



SYSTEM RESOURCE MODULES—FOR COMPUTATION, MEMORY, AND I/O—ARE AUTOMATICALLY POOLED FOR EFFICIENT SUPPORT OF INTERACTIVE USERS AND MULTISTREAM BATCH

A modular 32-bit multiprocessor, BTI 8000 uses variable resource architecture. Computational power, memory, and I/O resources are automatically pooled by system monitor software to process overall system workload



The First Mil-Spec Computers with Strong Family Ties

ROLM's new Multiprocessor Communications Adapter (MCA) provides complete multiprocessor capability for ROLM's family of AN/UYK-19 processors including the half million word 1666. As many as 15 of these processors may be tied to a single MCA bus, providing redundant processing capability in large or critical systems, or for DMA-speed parallel communications in a multiprocessor environment. The MCA is an economical way to increase systems capability by easily connecting additional processors to the current system.

ROLM's MCA is now available for off-the-shelf delivery. It is fully supported by ROLM real time software systems. Processors sharing an MCA bus may operate under RMX/RDOS, RDOS, RTOS or a combination of all three. If you have system requirements for ROLM's MCA family plan, write or call for more technical information.

ROLM—innovation, performance, reliability and value engineering.

That's Why We're #1 in Mil-Spec Computer Systems

ROLM MIL-SPEC Computers

4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350.

In Europe: 645 Hanau, Muehlstrasse 19, Germany, 06181 15011, TWX 418-4170.

CIRCLE 17 ON INQUIRY CARD

With Zilog, it's all in the family.

If you're an OEM interested in micros, take a look at the Zilog MCZ-1 family. It's ready today to start working for you.

We've got the goods for OEM's. There are rack-mountable units, as well as table-top model units with integrated CRT's, all sizes of disks and some new low-cost configurations. Plus, four full programming languages. Flexible configurations ready to fit almost any product development strategy.

- **Want a low cost disk computer?** Our MCZ-1/05 is a table-top unit with two floppies, RS232 terminal interface, parallel printer interface, up to 60K memory and lots of room for I/O expansion. It's under $5,000.
- **Need a cartridge disk computer?** Our moving head MCZ-1/35 disk system sports two Z-80's. The file management system is right in the disk control unit, and up to four cartridge disk drives are supported.
- **Need smarts to drive a display unit?** Our MCZ-1/60 gives you two CPU's to work with. Programs for the CRT can be down-loaded from the system's floppy disk. Terminal memory can go to 52K.
- **Go ahead and pull out the stops.** The MCZ-1/90 is a totally integrated computer package with three CPU's: the central computer, cartridge disk controller, and a programmable CRT.

Our micros speak your language. Zilog's MCZ-1 family gives you your choice of four software families. ■ COBOL ■ Extended BASIC ■ FORTRAN ■ PLZ (Zilog's powerful systems programming language)

We'll show you how to put it together. A whole family of I/O expansion boards are directly compatible with every mircoprocessor in the MCZ-1 series. There's a parallel interface, a serial interface, an analog interface, a RAM memory, a PROM memory—even PROM programmer boards.

Compatible all the way. Zilog's RIO operating system lets you start with a text editor, macroassembler, linker, file management system or any one of a variety of other I/O drivers and system commands. Then add any of our language processors: COBOL, Extended BASIC (decimal or binary), FORTRAN or the powerful PLZ family of system programming languages. Move your programs in any language at will up and down the whole MCZ-1 hardware family.

Tested. Then, tested again. Quality is monitored at every step of the way. Plus, every board and sub-assembly is burned in at elevated temperatures. And, after the system is assembled, it is burned in again at the same elevated temperatures.

Why wait? The Zilog MCZ-1 family delivers dramatic price/performance ratios unmatched by most minis. Every product is backed by Zilog's commitment to technological superiority, quality and service.

Name your volume. Name your deadline. Zilog is prepared to ship in OEM quantities with 30-day deliveries.

Write. Better yet, call. Let us know your needs. There's a Zilog small computer system that's just the right size for your application. You wouldn't expect less from the company that's pledged to stay a generation ahead.

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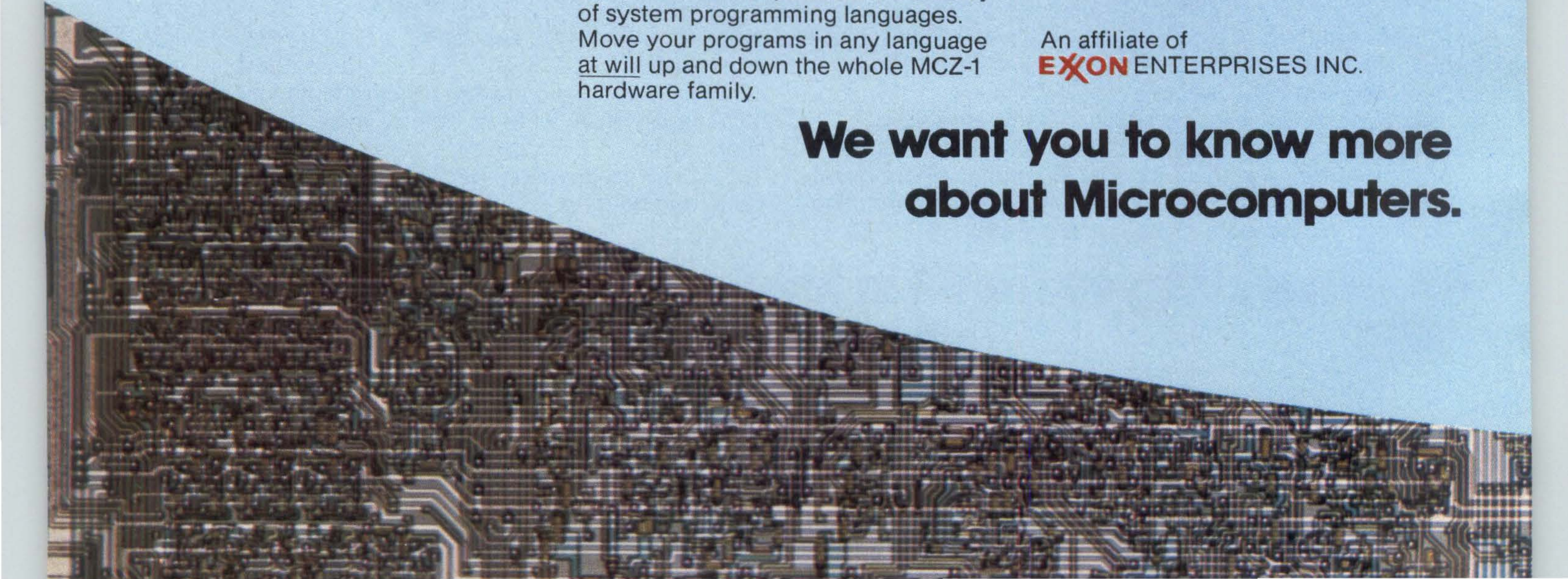
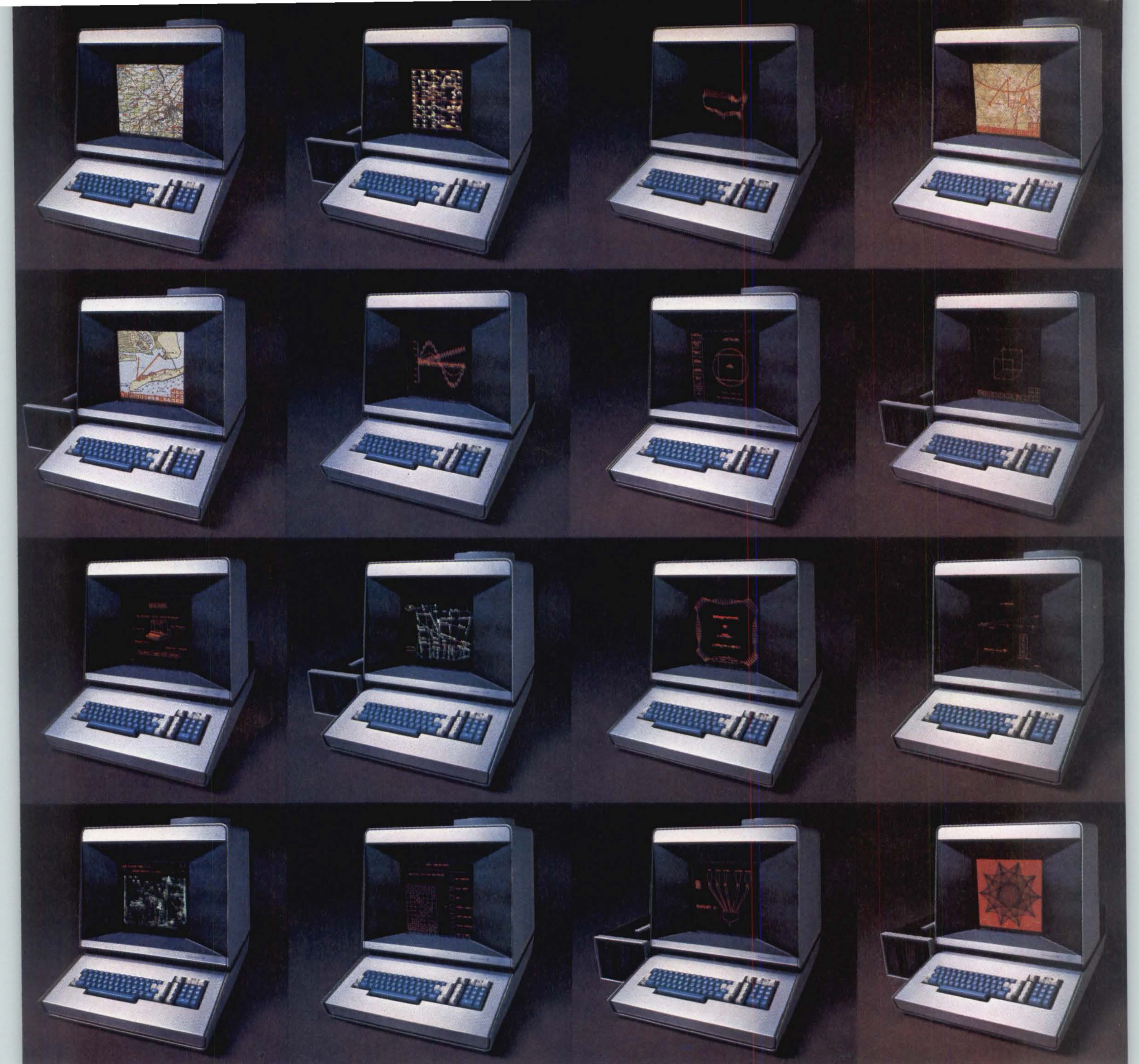



Zilog
CIRCLE 18 ON INQUIRY CARD



WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60 STANDS ALONE.

A display terminal that won't stand alone can't be as versatile or as adaptable as the Orion-60, the modular plasma display system that stands by itself or interfaces with existing hardware to let you create your own programs.

To begin with, the Orion-60 is an easy touch: besides offering full alphanumeric, floppy disc and rear-projection capabilities, it lets you create displays and enter data simply by touching the screen with your finger.

That means you can project a slide onto the screen coordinates and plot your own course over it. You can program your own character sets. You can generate vectors of any length to absolute screen coordinates. In short, you'll have a flexible terminal that will keep up with your needs today—and grow with your operations tomorrow.

Of course, since Magnavox was a leader in the development of plasma terminals, you can be sure your Orion-60 will have a bright, high-contrast display free from jitter and distortion.

There's a lot more you should know about the ways this remarkable terminal can help you get more out of graphic displays. For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 S. Coliseum Blvd., Ft. Wayne, IN 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

CIRCLE 19 ON INQUIRY CARD

is transparent to a program since all device and file I/O is performed by standard record writes and reads through logical I/O units assigned external to the program.

Software offered with the system includes ANSI standard COBOL, FORTRAN IV, a CODASYL compliant data base management system, RPG II, extended BASIC, an assembler, and an extended version of PASCAL. The system's control mode command language for both interactive and batch processes has a simple verb-noun structure. It supervises user access to the system, ensuring legal entry and accountability when the user logs on.

Circle 170 on Inquiry Card

Commercial Computers Speed Transactions In Online Applications

A low cost computer for small companies and a system offering online transaction processing capability extend the business computer line offered by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304. Both provide full data base management capability. In addition MFG/3000 materials planning and control system offers three products that enable manufacturers to improve inventory management, control costs, and obtain timely and accurate information on which to base purchasing and manufacturing decisions.

The HP 250 has a built-in IMAGE data base manager, software modules for generating printed reports and forms, 32k bytes of built-in user memory, 128k bytes of system memory, two 1.2M-byte flexible disc drives, 180-char/s printer, and full typewriter keyboard and CRT terminal. Providing four times the capacity of Series II models, the HP 3000 series III expands to 2M bytes of main memory. It uses the MPE-III operating system to speed online transaction processing and adds a number of data management capabilities.

Programming language used with the 250 is a business version of HP's BASIC, featuring subprograms, multiple character variable names, and flexible output formatting. A standard system includes the IMAGE/250 data base manager, a subset of the 3000 series IMAGE package. To make programming and operating as simple as possible, three software modules are provided. Query/250 allows unprogrammed access to information, permitting data to be retrieved, updated, or modified without additional programs. FORMS/250 consists of utilities for creating and modifying forms, and provides a programmable means of displaying/erasing forms and entering/retrieving data. Report Writer/250 aids in production of reports by providing automatic paging controls and built-in restart and pause capability for the CRT or single sheet printout.

In addition to larger main memory the series III uses the HP 7925 120M-byte disc drive. As many as eight drives can be supported for a maximum of 960M bytes. The enhanced MPE-III operating system for 3000 series III computer systems speeds operations such as entry and updating of data base without compromising the system's effectiveness in timesharing uses such as program development and problem solving. The system enables as many as 32 local terminals, operating synchronously or asynchronously, to be connected via a single hardwired line to a single input port. Using asynchronous repeaters the multiport option on multiport CRT terminals allows a single input port to accommodate a line up to 64,000′ (19.5 km) long while operating at 9600 bits/s.

The operating system's serial disc interface structure allows any disc pack to be treated as a private file and improves backup procedure speed as much as 2.5 to 1, by allowing backup to disc to be substituted for backup to tape.

Circle 171 on Inquiry Card

Semiconductor Memories Expand 3031/3032 Capacity to 12M Bytes

Semiconductor memories for IBM 3031 and 3032 processors added to the 6300 family offer users up to 10M bytes of external main memory in a single cabinet. Providing double the capacity currently available from IBM, models 6331 and 6332 are supplied by Memorex Corp, San Tomas at Central Expy, Santa Clara, CA 95052 in 1M- or 2M-byte increments up to a total of 12M bytes when combined with the minimum 2M bytes required on the CPUs. Performance improvement is attained through increased throughput, reduced paging frequencies, and extended data base/data communications applications.

Using 8k-bit MOS RAM technology the memories provide 128k-bytes of storage on a single board. Storage devices can be replaced individually, eliminating the need to replace entire boards when an error is detected. A microprocessor controlled maintenance panel further enhances maintainability by monitoring online memory status; sensing, collecting, and logging error conditions; isolating memory interface problems; and identifying failing memory components as they occur. The panel also provides a complete history of machine status and facilitates chip fault isolation and replacement.

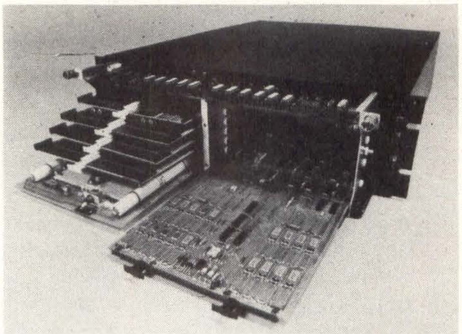
Full compatibility is maintained with 3031 and 3032 processor address relocation for up to 6M bytes. Address relocation is extended beyond IBM's 6M byte maximum so that the entire CPU address range may be reconfigured when memory in excess of 6M bytes is present.

Circle 172 on Inquiry Card

Minicomputer Family Expanded at Upper And Lower Levels

Low end model 23 and high performance model 57 have been added to the Level 6 family of minicomputers by Honeywell Information Systems, Inc, 200 Smith St, Waltham, MA 02154 to offer true mix or match capability without affecting a user's application. Priced at under $14,000, the model 23 operates in the 200k instructions/s range, while model 57 CPUs are capable of performing over 700k instructions/s, support direct addressing of 2M bytes of memory, and include a scientific instruction processor for efficient execution of FORTRAN.

A diskette based, communications oriented system the model 23 is best suited to dedicated application where it will remain installed over a long period performing one or more specific functions. Offered in rackmount or prepackaged versions, the unit has maximum memory of 64k words and supports diskettes, serial printers, line printers, and communication to



In the entry level model 23 minicomputer, Honeywell has packed up to 128k bytes of memory on half-size board by using 16k-bit memory chips (right foreground). Chassis holds processor and 12 half-size modules for memory, and peripheral and communications controllers

9600 baud. System cost was kept low by modifying the physical packaging structure.

The central processor features the same internal register organization and instruction set as the larger model 33, but uses a low cost synchronous bus that can accommodate a 64k-word system with up to 18 peripheral devices and/or communication lines. The processor is implemented on a single PC module that includes CPU logic, control, and timing circuits for the synchronous bus.

A high performance, commercially oriented minicomputer, model 57 has two processors—one that executes the standard Level 6 instruction set and one that executes an additional set of COBOL instructions—as well as a 4k cache memory and a memory management unit. Megabus architecture accommodates all system elements.

Directly addressable main memory can range in size up to 2M bytes. It is accessed only if the desired word is not in cache. Whenever a word already in cache is to be written, it will be modified both in main memory and in cache.

The model 57 processor requires three slots on the Megabus—one for the primary central processor board, on which a secondary board for memory management is mounted; one for the commercial instruction processor; and one for cache memory. The central processor (CP) and the commercial instruction processor (CIP) normally operate in parallel. The CP extracts operation codes and sends them on to the CIP, which then begins autonomous operation, leaving the CP free to execute the next instruction.

Supporting a multiuser transaction processing environment, GCOS/6 MOD 200 entry level transaction processing system is capable of operating as a standalone system or as a multifunctional intelligent terminal in a communication network. Transaction control is memory efficient and can result in decreased development time and effort. General features include higher level language support for entry level and intermediate COBOL and automatic self-generation during bootstrap loading.

Circle 173 on Inquiry Card

Modular Keyboard Based Interactive I/O Terminals Operate at 9600 Bits/s

Made up of a number of office environment modules, the 4500 data terminal family provides efficient, economical, and reliable data communications in computer based systems. Components form a variety of terminal configurations to provide a range of system solutions to user needs in sophisticated computer based communication systems. Teletype Corp, 5555 Touhy Ave, Skokie, IL 60076 is offering the terminal in configurations for interactive, batch, and data entry requirements. It has protocol features and host compatibility for easy application.

Modules in the initial offering include data entry and typewriter style keyboard modules with optional numeric pad, magnetic stripe operator badge reader, and keyboard lock for terminal security; display module with capacity for display of 24 or 32 lines of 80 char each; serial matrix printer module operating at speeds to 47.5 char/s and printing 132 char at 10 char/in (3.9/cm); and a 132-col line printer module that provides full font character printing at 300 lines/min. A microprocessor based controller module interconnects individual components and defines operating characteristics of each configuration.

The controller incorporates up to 64k bytes of addressable memory and three direct memory access circuits for efficient data manipulation within the terminal. It provides up to 32 SSI ports for device connection and two EIA RS-232 ports to interface to transmission facilities and auxiliary devices.

First members of the family, the 4540 series are keyboard display based interactive terminals designed for inquiry/response, data entry, and data retrieval. With operating speeds ranging from 2400 to 9600 bits/s, the units provide a choice of ASCII or EBCDIC code, and error checking and correcting scheme.

Single display and clustered versions are available; a cluster may contain up to 32 devices, 8 of which may be printers. All terminals can be coupled to multipoint or point to point private line communication facilities.

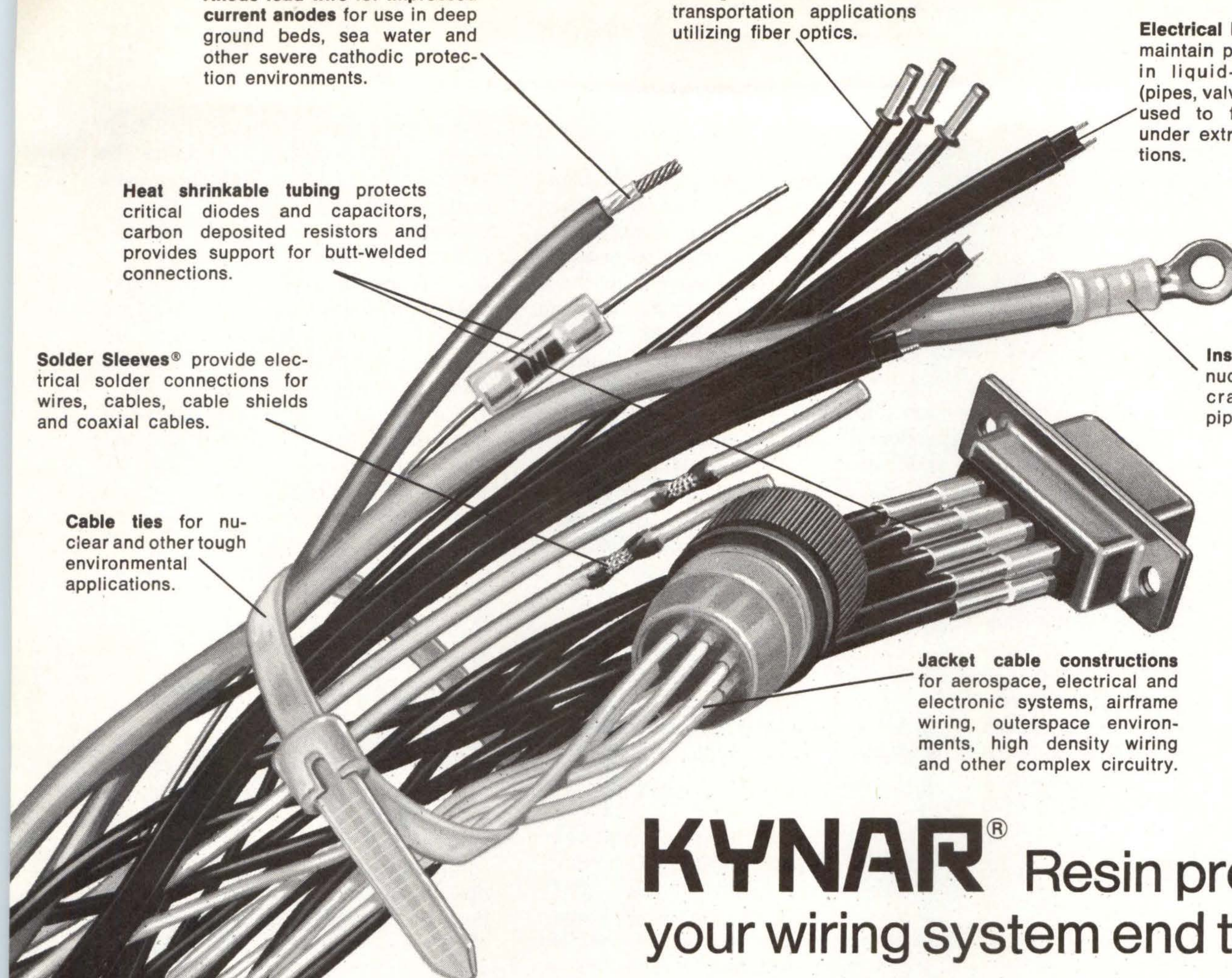
Circle 174 on Inquiry Card

Five Models Added To Intelligent Terminal Systems Family

To provide a complete family of distributed processing systems, Texas Instruments Inc, PO Box 14444, Houston, TX 77001 has added five members to its series 700. Models 771/1 and /2, and 774/2, /3, and /4 offer low cost solutions to requirements such as source data entry, local file inquiry/response, local printing and data preprocessing, as well as batch and remote data entry communication with a host computer or other family member.

A single-station intelligent terminal with 1920-char video display, two diskette drives, a 16-bit TMS 9900 microprocessor, and data entry keyboard, the 771/1 has a 64k-byte memory (24k bytes are user accessible). A built-in thermal printer is included with the 771/2. Both can be equipped with 150-char/s model 810 receive-only printer.

The model 774/2 is a multistation intelligent terminal system with dual diskette storage. Standard configuration includes a 96k-byte processor, 1920-char model 911 video



KYNAR® Resin protects your wiring system end to end.

It's the unique balance of these properties that enables KYNAR to perform in many tough applications:

Kynar can be marked, printed, striped, or hot stamped for identification. It can also be pigmented for color coding.

Kynar has high dielectric strength and good insulation resistance.

Kynar has a temperature range from −80° to +300°F.

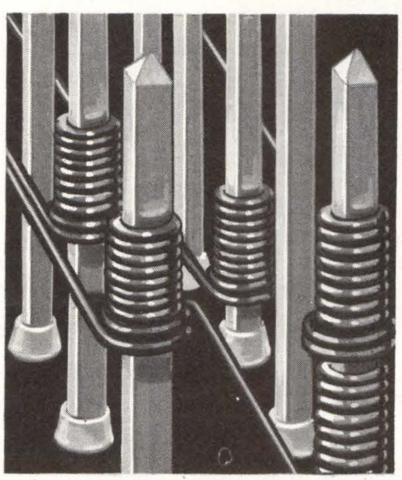
Kynar is nondripping, self-extinguishing (UL STD 94 V-0) and has an LOI (Limiting Oxygen Index) of 45.

Kynar has good chemical resistance, low permeability.

Kynar has a tensile strength of 7000 psi. It is mechanically strong and has good abrasion and cut-through resistance.

Kynar has low-moisture absorption (0.04%), excellent radiation and UV resistance.

For list of fabricators, more technical data, specifications (UL and military), write or call Joe Michaud. Plastics Department, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. (215) 587-7520.



Kynar insulated wire is ideal for automatic wire wrapping operations for computer back panels.

*KYNAR is Pennwalt's registered trademark for its polyvinylidene fluoride resin.
®Solder Sleeves is a registered trademark of Raychem Corporation.

PENNWALT
CHEMICALS ■ EQUIPMENT
HEALTH PRODUCTS

display terminal, dual 256k-byte diskettes, and two communication ports. The system supports up to four diskette drives, two model 810 printers, or one 810 and one 300-line/min model 2230 line printer. Memory expands in increments of 64k, 128k, and 192k to a maximum of 352k bytes.

A standard configuration 774/3 adds 5M-bytes of fixed disc capacity and 5M-bytes of removable cartridge to the /2. The 774/4 substitutes a 160k-byte processor and adds an expansion cabinet to support eight display stations and five printers.

All models use TPL 700 data entry language which combines a fill-in-the-blanks forms package with a high level English like procedure language for data processing applications. System operation on the 774 is supported by a multitasking memory resident system executive, which serves as interface between operator and task to be executed, providing operator communication, data file management, task scheduling, and data input/output.

Circle 175 on Inquiry Card

Standards Team Will Meet To Consider Standard Nomenclature for FORTH

A team formed to encourage conformity in use of the FORTH™ programming language and operating system will hold its fifth meeting in Los Angeles during September. Composed of members volunteered by major research institutions located in several European countries, Chile, Canada, and the U.S., the FORTH International Standards Team is attempting to formulate a standard model of nomenclature, formatting, and documentation.

Working since 1976, the group has provided a preliminary version of international standards which, when coupled with parallel CAMAC standards for computer and instrument hardware, has permitted faster verification and sharing of results and has alleviated duplication of experiments and programming. At the fourth session the team agreed to divide commands into several levels of subsets. The most fundamental, Level 0, subset was considered, and a set of basic standards of nomenclature, called FORTH 77, was adopted.

The upcoming meeting will focus on the more difficult questions posed by the Level 1 vocabulary, which arise because the application oriented language provides a choice of methods for solving problems that arise in particular technical fields. In conjunction with the meeting, suggestions and comments from users interested in standardization are being solicited. Such material should be addressed to the FORTH International Standards Team, c/o FORTH, Inc, 815 Manhattan Ave, Manhattan Beach, CA 90266 before August 1.

Circle 176 on Inquiry Card

Color Graphics Terminals Offer Affordable Raster Scan Systems

Claimed to make raster scan color graphics display techniques economically viable, Colorgraphics 6110 and 6310 computer terminals feature modular microprocessor controlled architecture and TTY compatible interfacing. Ramtek Corp, 585 N Mary Ave, Sunnyvale, CA 94086 introduced the family to provide the ability to easily convert from black and white to raster color graphics without heavy software development costs later on.

Compatible in software, options, and peripherals the terminals use resident control software which supports the communication interface, keyboard, and joystick, and includes a TTY emulator and graphic language interpreter. Basic software is extended with options that provide graphic subroutines and patterned vectors. Resident firmware provides an easy to use interpreter that allows the user to develop software offline without costly host computer overhead.

Terminals are initialized as TTY emulators, but convert to the graphics state on command. All communication with the host computer is serial asynchronous and in the form of printable ASCII text strings that are generated by high level applications programs. Dual architecture gives the user separate memories for graphics and alphanumerics. Text and graphics may be viewed separately or together, for user flexibility.

A low priced terminal, the 6110 features 320 x 240 x 3 graphics display matrix, 72 x 24 alphanumerics format, and 13" (33-cm) medium resolution color monitor. Offering eight graphics colors, the system has a TV-compatible format. A high resolution terminal, the 6310 provides an 800 x 600 x 3 graphics display matrix and 72 x 24 alphanumeric format. The system has a 19" (48-cm) monitor and offers programmable colors, as well as color zoom and pan over the standard 1024 x 1024 x 3 memory.

Circle 177 on Inquiry Card

Distributed Processing System Serves Four Input/Inquiry Terminals

XL20 distributed processing system is a multimicroprocessor unit that provides processing intelligence and data storage for data capture, report generation, file inquiry, and data communications. The system serves up to four video display input/inquiry terminals and accommodates up to four diskette drives totaling 4.8M bytes for program/file storage and I/O media.

Input/inquiry terminals for the system, offered by Pertec Computer Corp, CMC Div, 12910 Culver Blvd, Los Angeles, CA 90066, have either 480- or 2000-char video displays. Hardcopy output is handled by system printers capable of from 170 to 900 lines/min.

Diskettes are available with single-sided, single-density IBM format or double-sided, double-density XL extended format. Memory expands in 16k-byte increments from 80k to 128k bytes.

XL/OS operating system provides 2770, 2780, 3780, and HASP communications protocols as well as checkbox/COBOL for programming and indexed direct access method (IDAM) for local indexed file inquiry. Network communications is provided for SL40, CMC 1800, and CMC 3/5 and for certain mainframes.

When operated as remote online subsystems to an XL40, the terminals can share the system data bases and processing power, including 3270 mode capability. Using this feature, they can interactively access data bases in a remote host mainframe through the XL40.

Circle 178 on Inquiry Card

INTRODUCING THE BENDIX PORTABLE MODULE TESTER

Now automatic, on-the-spot module testing is on the way.

Here's a new way to test anything from a printed circuit board to a complex logic system. And you can do it on the job.

Our new portable unit weighs just 30 pounds and has no moving parts. Yet it does everything that stationary digital cabinet-type units can. It eliminates downtime while modules are tested away from the job site. Does away with trial-and-error testing and unwarranted returns, too.

You can take it on board planes or ships, to hospitals, to labs, to computers or communications equipment, and to sophisticated quality-control operations in mass production plants.

Highly trained operators are not needed. Programming procedures are so easy to pick up. And an interactive display system makes operation easier still. Test systems are stored on solid-state cards, providing reusable data memory.

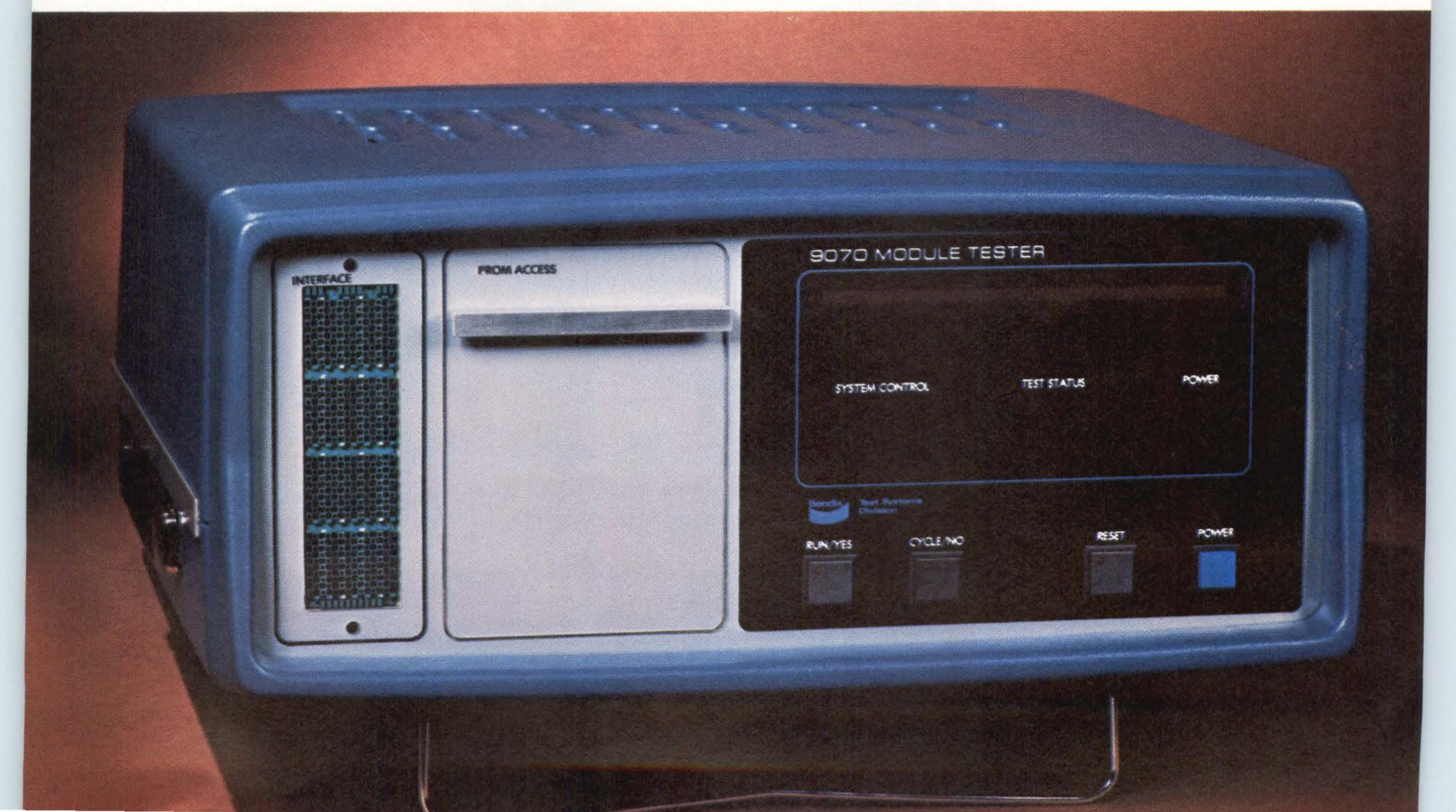
The Basic Bendix unit is capable of testing cards to 64 pins and has the capacity to expand to 256. Additional options are available including:

- Fault Isolation Testing
- Digital Voltmeter/Frequency Counter
- Teletype Interface and Advanced Software Aids.

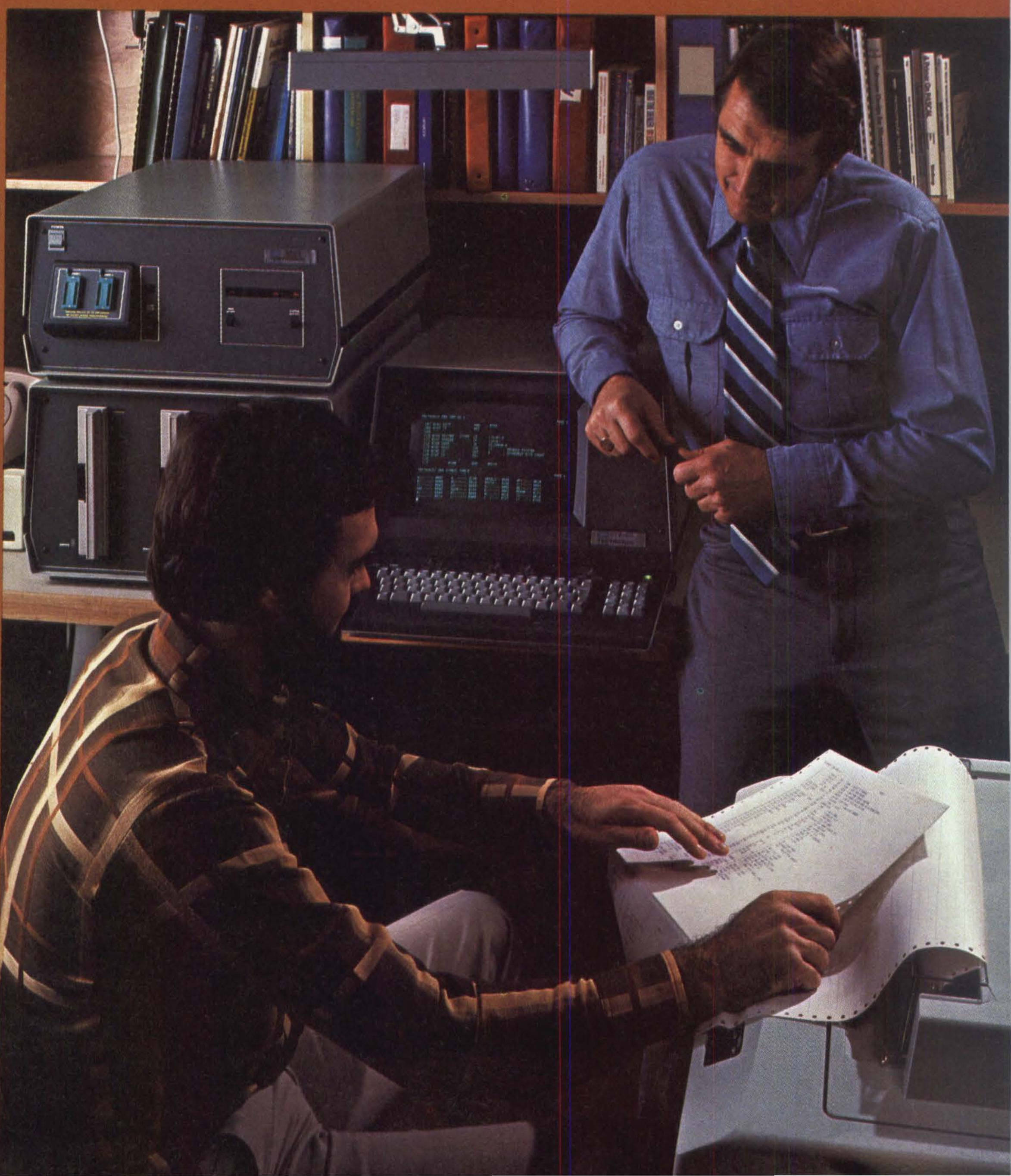
For more information, contact: Bendix Corporation, Test Systems Division, Teterboro, N.J. 07608. Or call (201) 288-2000, extension 1789.

Bendix

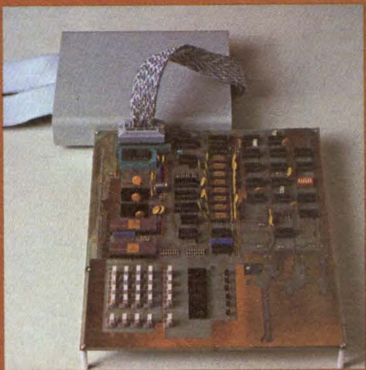
CIRCLE 21 ON INQUIRY CARD



Our system emulates the 8080 and the 8085. The Z80. The 6800. The TMS 9900. And that's just for openers.



Because who has time to learn a new system when a better chip comes along?



Prototype control probe runs prototype hardware and software under control of the microprocessor lab while you maintain access to program activity.

JOB AFTER JOB, OUR SYSTEM STAYS WITH YOU.

We know time spent learning equipment is best spent on equipment that's going to stay around.

That's why we engineered the first development lab for designers like us who work with major microprocessors.

Now you can work with two or more chips. Without depending upon a single chip vendor. Without buying and learning an entirely new system.

THE BEST IDEAS

Our features are the kind of ideas you'd probably engineer for yourself. . . the kind of system you get from a chip user, not a chip vendor.

DISC BASED SYSTEM

Includes text editor, macro relocatable assembler, debugging software and file management utilities, to help simplify software preparation and debugging.

REAL TIME PROTOTYPE ANALYZER

This invaluable option lets you easily track down timing or program logic problems by dynamically monitoring the microprocessor bus in real time.

UNCRASHABLE ARCHITECTURE

Separate system and emulator processors and memory protect the operating system software should your program fail while emulating the target microprocessor.

PARALLEL DEVELOPMENT INTEGRATED TESTING

Hardware and software engineers can test, trace, and debug independently up to the point of integration. Then they can work together, productively.

If you're concerned about how you spend your time, take a close look at a design lab you can use time and again . . . even when a better chip comes along.

Contact your local Tektronix Sales Office, or write or call Tektronix, Inc., P.O. Box 500, Beaverton, OR, (503) 644-0161. In Europe, Tektronix, Ltd., P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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COMMITTED TO EXCELLENCE

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Circle 23 for a demonstration.

Tektronix microprocessor development labs.

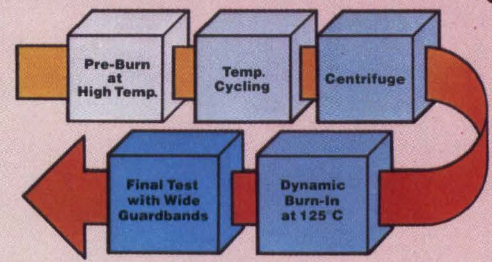
Designed by people on your side of the bench.

What the learning curve has done for Mostek memories.

Industry's most advanced memory products are now available for high reliability applications. Only Mostek offers high reliability processing of 16K dynamic RAMs, 4K static RAMs and 64K ROMs. High performance and high reliability. Mostek's learning curve experience made it possible.

For years, Mostek has been the recognized leader in memory circuit reliability. Every hi-rel memory circuit we ship is subjected to complete temperature cycling, centrifuge (constant acceleration) pre-burn test, dynamic burn-in and final test, all per MIL-STD 883/Class B processing.

Hi-Rel Processing



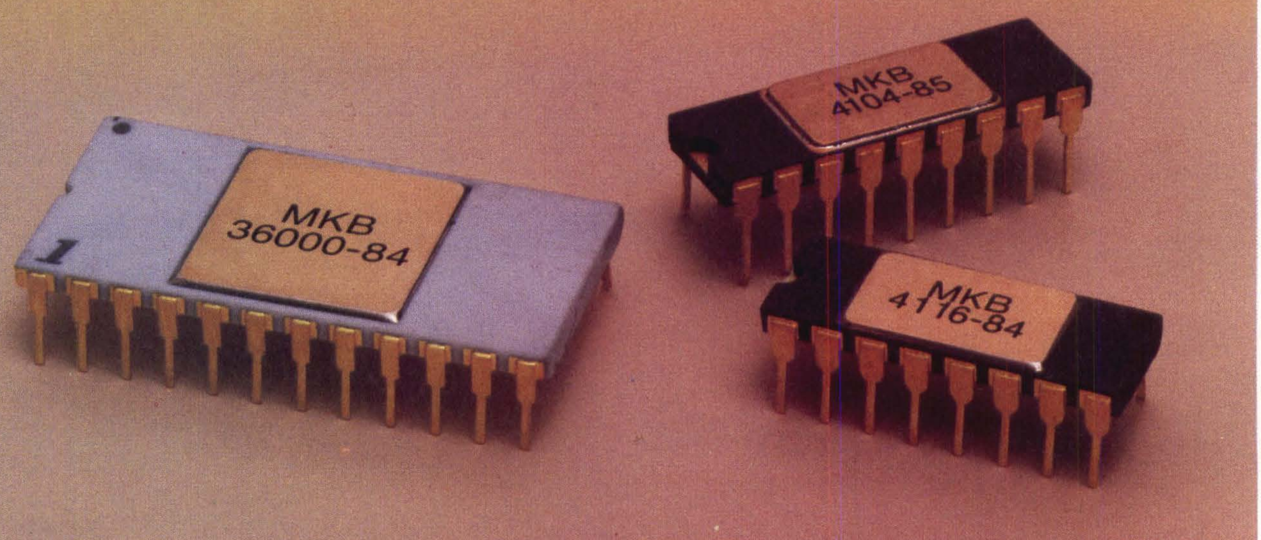
	Access Time	Cycle Time	Temperature Range (Ambient)
MKB4116-83/84	200/250ns	375/410ns	-55°C to +85°C
MKB4027-83/84	200/250ns	375ns	-55°C to +85°C
MKB4104-85/86	300/350ns	510/610ns	-55°C to +125°C
MKB34000-84	450ns	450ns	-55°C to +125°C
MKB36000-84	250ns	375ns	-55°C to +125°C

For military applications, Mostek offers the 4027, 4116, 4104 and 36000. And Mostek's 4096 4K RAMs have recently received DESC line certification for MIL-M-38510 Class B and C.

Mostek's Hi-Rel memories are available now. Both dynamic and static RAMs can be shipped from stock. And ROM programming receives the fast turnaround required for your application.

For more information on Mostek Hi-Rel memories, contact Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; Telephone 214/242-0444. In Europe, contact Mostek Brussels; Telephone (49) (0711) 701045.

MOSTEK.



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MKB—Devices processed 100% to meet requirements of Mil Std. 883 Class B including 100% final electrical tests at high and low rated temperatures.

Add-On Memories Offer IBM Compatibility Plus Added Capacity

Three models of IBM compatible 303X add-on memory from Electronic Memories and Magnetics Corp's Computer Products Div, 2311 W El Segundo Blvd, Hawthorne, CA 90250 are designed with small size as a criterion. Based on 4k MOS RAMS, all models feature a power controller that provides added capability during brownouts. Use of the same basic memory board throughout the series provides flexibility in expansion and upgrades.

Plug compatible with IBM's 3032 processor complex, the 7/3032 has capacity for up to 8M bytes. Users can expand to the maximum in 1M-byte increments. Units are designed for conversion to other 303X, 370/158, or /168 memories. Fetch and store time is 320 ns. Power supply is 208 V, 3 ϕ, and operating temperature is 59 to 95 °F (15 to 35 °C). Power consumption is 1.25 kVA at 208 V for the first megabyte and 0.80 kVA for each additional 1M-byte increment.

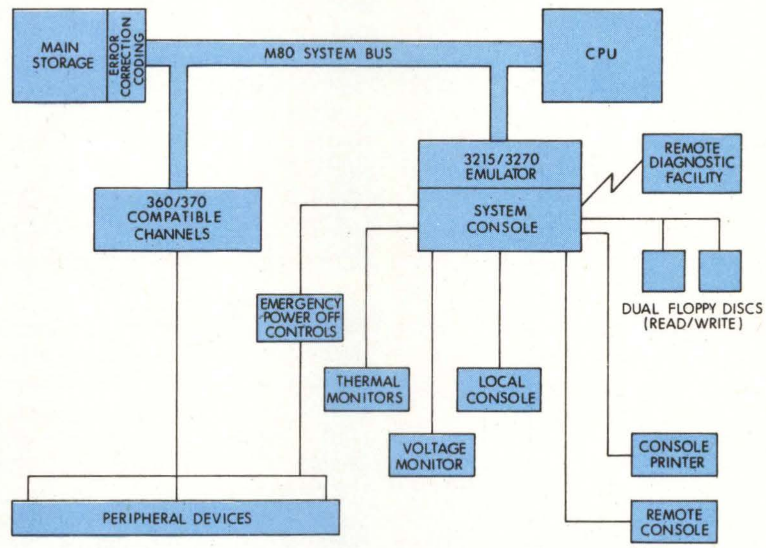
Fetch and store times for 7/3031 and /3033 are specified as 345 and 290 ns, respectively. The /3033 has a standby memory feature that can take over in the event of double bit errors. Power supply and operating temperatures are the same as for the /3032.

The models share enhancements, mechanics, power, and deferred maintenance. Deferred maintenance allows any 1024k-byte section of memory to be taken offline by simply flipping a switch on the front panel. The external operator's panel visually alerts the operator to status and existing malfunctions.

Circle 179 on Inquiry Card

Strategic Architecture Allows Plug-In Upgrade Of IBM Compatible CPUs

Two models of the M80 series IBM compatible central processors, the M80/3 and M80/4, introduced by Magnuson Systems, 2500 Augustine Dr, Santa Clara, CA 95051, are said to operate significantly above the performance level of the 370/138 and the 370/148, respectively. M80/5, with a performance range claimed to surpass that of the 3031, will be announced later this year. Systems are 100% software and hardware compatible with IBM Systems /360, /370, and 303X.



Magnuson's M80 series uses strategic architecture design concept to eliminate traditional constraints on system expansion, performance range, and software compatibility. Basic system contains CPU, resident firmware, data channels, main storage, and system console

While called a series, M80 is actually one basic configuration that can be user upgraded with plug-in card modules, due to a design concept called strategic architecture. System organization is structurally as well as functionally modular; logic and memory boards are essentially independent subsystems. Bus-structured CPU design minimizes possibility of failures caused by complex cabling and backplane wiring.

Memory uses currently available MOS devices; but the architecture permits any desired mix of memory, including charge-coupled device (CCD) and bubble. Schottky TTL MSI logic is used in the CPU and other logic subsystems; modularity allows use of higher performance circuits if required, or when economically feasible. The basic system can expand from 562k- to 16M-bytes memory, and from 3 to 16 data channels. Control store is expandable from 8k to 256k bytes.

Strategic architecture PCB modules include central processor (up to eight CPUs may be used in a multiprocessor); storage control board, including memory error correction, RAM, and all required address encoders; two console boards with independently programmed microprocessor systems to provide a variety of console functions; IBM compatible data channel; peripheral controllers; and system bus. An M80/4 system with 4M-bytes main storage, 8 data channels, and CPU, requires 27 memory and logic cards plus 3 console cards.

System console, functionally similar to that of a 370/158, fully controls CPU as well as access to memory and channels. An alter display mode permits display and alteration of system memories. In diagnostic mode, memory faults are traced to the chip, and channel faults to the board level. Channels may be reconfigured to match either byte or block multiplexing. Console processor also contains floppy disc, light pen, printer, and communications modem.

Systems are packaged in a compact desk-high unit and do not require special air conditioning. Power consumption is claimed to be 75% less than comparable /370 models. The unit can accommodate up to 4M-bytes memory and 8 data channels in addition to CPU and console. Add-on units expand this capacity to 16M bytes and 16 channels.

Basic system is not limited to IBM compatibility but can be modified to emulate Burroughs, Honeywell, and Univac computers, and be reconfigured at the console to run either IBM or non-IBM software. System may also be organized as a central processor, multiprocessor, distributed processing system (either central data base or remote), or as front- or back-end processor.

Circle 180 on Inquiry Card

Solid-State Keyboards Use Ferrite Core Switches For Reliability

A solid-state keyboard using linear ferrite core technology, Series III is being offered at a price competitive with reed and mechanical designs. Introduced by Cortron, a div of Illinois Tool Works Inc, 6601 W Irving Pk Rd, Chicago, IL 60634, the keyboards use a scanning technique for keyswitch array interrogation and code generation. Keyboards may be address encoded or encoded with any code set.

Ferrite core technology is not susceptible to failure through dust, moisture, or other environmental hazards. Insensitive to static discharge noise and emi, the switches maintain switch to switch consistency and essentially constant performance across a broad temperature/humidity range.

ss3 keyswitches are contactless, with a low profile—0.5" (1.27 cm) from mounting plate to keyboard bottom. Switch travel is a full 0.150" (3.81 cm). Life test rating is 100M cycles.

Standard keytops are 2- or 3-shot molded. Keytops and legend are available in standard colors as well as gloss, semimatte, and matte finishes.

Circle 181 on Inquiry Card

Multiuser Virtual Memory Minicomputer System for Sophisticated Applications

PROTOS™, a terminal oriented, multiuser virtual memory computer system, includes a high speed cache memory, overlapped instruction execution, memory mapping and protection logic, and expandability to 2M-bytes of semiconductor memory. Developed by the Naked Mini® Div of Computer Automation, Inc, 18651 Von Karman, Irvine, CA 92713, the system combines advanced software with minicomputer based hardware designed specifically to support it, and is capable of sustained mixed instruction processing rates above 1M instructions/s.

A small configuration includes 256k-byte processor with eight asynchronous I/O ports, hardcopy terminal, 300-line/min printer, 80M-byte disc unit, and two flexible drive units, and will sell for approximately $100,000. A larger system consists of 512k-bytes memory, 16 I/O ports, hardcopy terminal, 600-line/min printer, two 200M-byte disc drives, dual flexible disc drives, and three video display terminals.

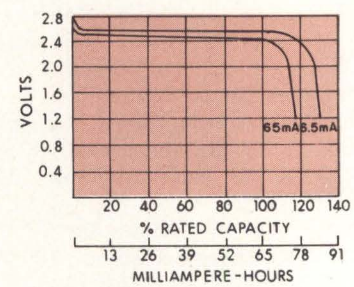
Principle features of the operating system are AUTOMAP™, a virtual file mechanism; a hierarchical multivolume file system incorporating removable private subfile systems; intertask communication, synchronization, and control; and independence of command language and operating system. Additional software support includes ALAMO™, a block structured system implementation language; macroassembler; interactive command language; and a metacommand language that permits users to write routines in which executable statements are commands.

Circle 182 on Inquiry Card

DIP-Type Battery Serves As Standby Power For Electronic Components

A standardized DIP-type nickel-cadmium battery, Data Sentry™ serves as an auxiliary power source in direct circuit board mounting applications. Developed by the General Electric Co, Battery Business Dept, PO Box 861, Gainesville, FL 32602, the batteries are rated at 70 mAh at 15 mA. They are offered in voltage modules of 2.4 or 3.6 Vdc to permit the designer to build the proper voltage for his system.

Battery design uses the μP-80 battery cell and is provided in a



Typical discharge curve for 2.4-V Data Sentry, General Electric's PC board mountable NiCd battery. Housed in 4-pin DIP-type package, device provides backup power for semiconductor RAMs

board mountable 4-pin DIP for PC board mounting. It is rated for a capacity of 65 mAh at a 1-h discharge rate and is designed for a continuous overcharge rate of 7 mA. Storage temperature range is from −40 to 50 °C. The batteries provide standard pin locations on polarity keyed modules, multiple pins for mechanical integrity, and are contained in a rugged plastic case. As an electronic component, they can be constant current overcharged continuously to keep them in ready to serve mode.

Circle 183 on Inquiry Card

Amplitude Measurement System Has Removable Calibration Module

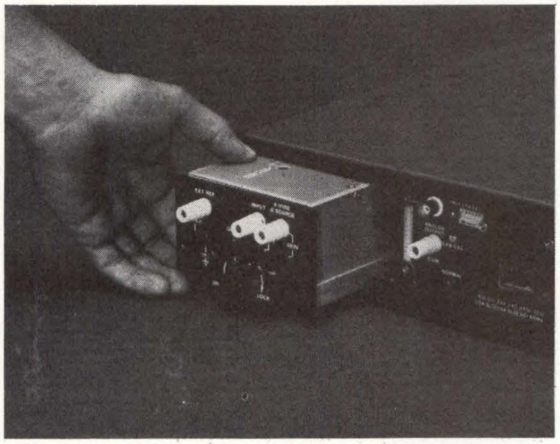
Based on a precision digital multimeter, the series 6000 amplitude measurement system also includes a completely removable National Bureau of Standards traceable cal-module, high speed digitizer, direct dB measurement conversion, 7-segment sorting, full math, and diagnostics. It was designed by Racal-Dana Instruments, Inc, 18912 Von Karman Ave, Irvine, CA 92715 to save user time while improving measurement and systems capability.

To reduce calibration costs, the unit is calibrated for most functions and ranges by simply flipping the switch on the rear panel, applying standard voltages and resistances to the front and rear panel inputs, and a simple sequence of front panel keyboarding. The removable calibration module contains both front and rear input terminals; all relays, dividers, and other components affecting calibration accuracy; as well as ac and ohm converters. Once calibrated the module automatically calibrates all other circuits when inserted into the instrument. Circuit cards outside the module may be changed without affecting its validity.

To eliminate most of the time-consuming routines traditionally required to accomplish resistor sorting, the instrument is equipped with a hi/lo limit function. It stores up to three low limits and three high limits to provide 7-bin sort capability. By entering one high and one low limit go/no-go testing can be attained.

Hardware costs can be reduced through selection of appropriate ac or dc reference and signal functions, with the instrument reading directly in ratio of the gain or attenuation. The calculator or lookup tables normally needed to convert to gain or attenuation in dB are eliminated, only the shift dB key need be pressed.

To reduce downtime and maintenance expense, a built-in diagnostic routine generates error messages. These messages allow a failure to be isolated to a single plug-in board.



Basic accuracy determining elements of Racal-Dana's series 6000 amplitude measurement system are contained in removable calibration module. All other circuits are automatically calibrated when module is inserted into instrument

Circle 184 on Inquiry Card

32-Bit Minicomputer Line Expanded With MOS Memory Units

One of eight computer systems announced by Systems Engineering Laboratories, Inc, 6901 W Sunrise Blvd, Ft Lauderdale FL 33313, the SEL 32/30 MaxiBox consists of processor with floating point arithmetic in firmware, memory bus controller, 256k bytes of ECC MOS memory, and a turnkey panel. Selling for a basic price of $27,300, the unit expands to 1M byte of 900-ns memory in 256k-byte increments.

Four models make up the 32/57 packaged systems series. Based on architecture of the 32 series processors, the units include single-cabinet packaging, ECC MOS memory, 26M-byte/s throughput, floating point instructions, and physical expansion to 1.8M bytes of memory. All include the RTM (realtime monitor) operating system.

Priced from $70,500 to $43,300, systems in the /57 line provide from 256k to 128k bytes of memory and 10M-byte capacity cartridge disc. The /5750 also provides a 300-card/min reader, 9-track magnetic tape unit, 300-line/min printer, and console CRT. Options include interfacing capability for up to eight local or four remote terminals. /5740 incorporates a 200-card/min reader and 340-char/s matrix printer. With 200-card/min reader and combination 30-char/s printer/console, the /5730 has either 256k- or 128k-byte memory. Aimed at dedicated realtime applications, the /5720 consists of 128k- or 256k-byte memory, 10M-byte disc, and 20-char/s combination printer/console.

In the higher performance 32/77 packaged series, systems offer realtime multiprogramming executive and macroassembler. Options include high speed floating point arithmetic and memory expansion to 16M bytes. Consisting of 512k-byte memory, 80M-byte disc, 9-track magnetic tape unit, 300-card/min reader, 600-line/min printer, and console CRT, the /7760 fills large storage needs, the /7750 replaces the /7760's disc with an 24M-byte capacity fixed media disc to meet reduced storage and performance needs. A starter system, the /7720 contains 256k-byte memory, 10M-byte cartridge disc, and 30 char/s combination printer/console. □

Circle 185 on Inquiry Card

The Computer in Machine Tool Control Today, and Its Future

Is direct numerical control finally a viable process for machine tools? Can its inherent values overcome the problem of its initial high cost sufficiently to permit recovery of investment within a reasonable time? Will it eventually replace standalone numerical control?

Those three questions introduced a summary of Westinghouse Electric Corp's 39th Annual Machine Tool Forum held in Pittsburgh, Pa on June 2 to 4, 1975 (*Computer Design*, Aug 1975, pp 42-44). Now, exactly three years later, speakers at the 42nd Annual Forum (June 12 to 14) in essence repeated the same questions.

Relative technologies have advanced drastically. The minicomputer has replaced the mainframe computer in nearly all applications except those requiring tremendous number crunching capacities. Even more important, perhaps, the microcomputer has progressed from a "toy" on the engineer's bench to an accepted device that has proven itself in thousands of control applications. Yet direct numerical control (DNC) still has not been universally accepted as viable, economical, and practical.

Choices Available in DNC

One of this year's speakers, C. A. Hudson of Westinghouse's Industry Systems Div, defended DNC and attempted to clear up some of the unknowns that have made prospective users shy away from its application ("Direct Numerical Control: Which Way is Best"). Mr Hudson claimed that although "thousands of small- and medium-size firms, as well as many manufacturing giants, are still put off by DNC" and "others (who) tried to justify it in the past . . . found it too expensive—requiring a big front-end cost," the technology has changed and "it's worth taking another look at DNC."

Although DNC has been too expensive for some firms in the past, it's now worth taking another look.

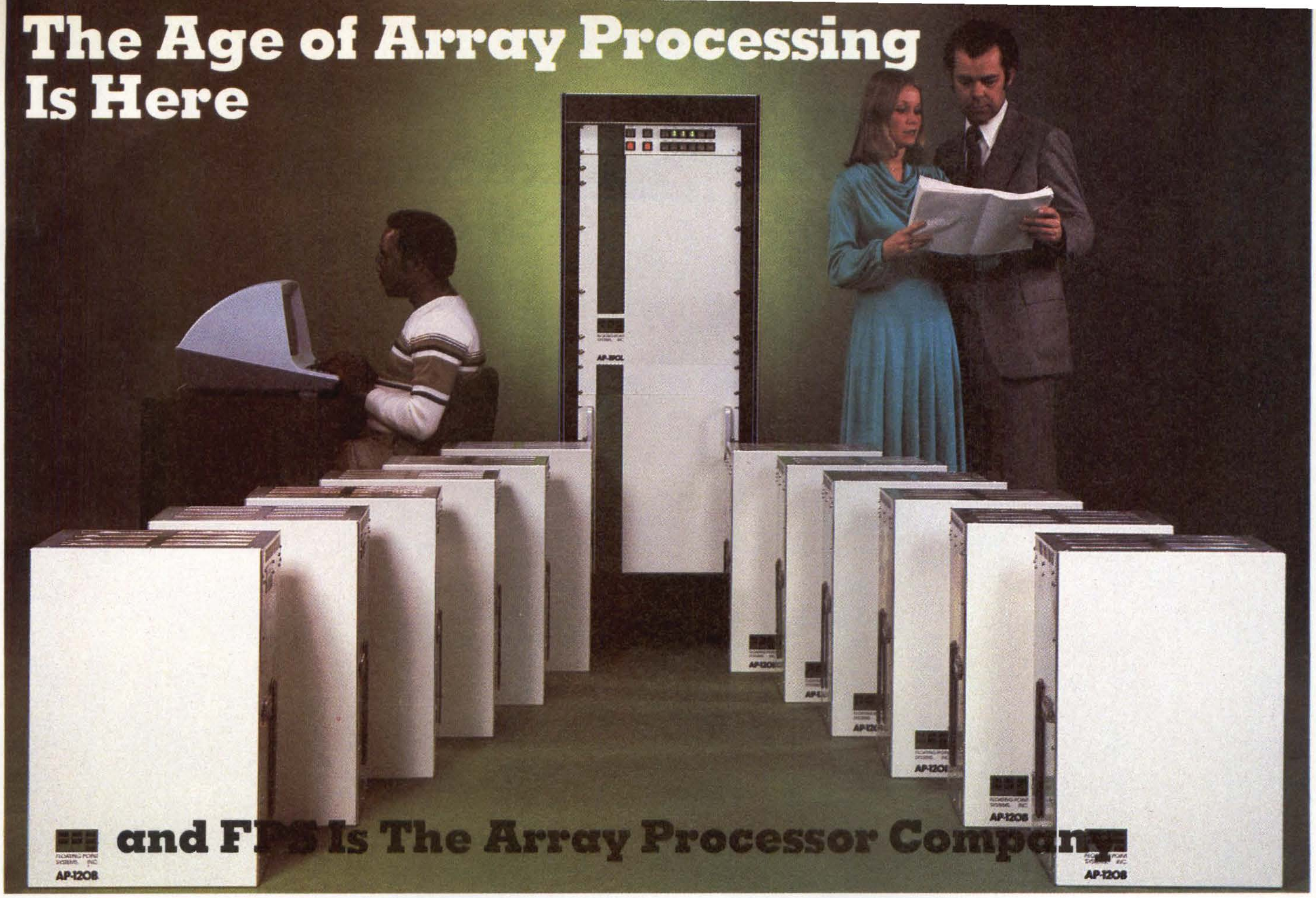
DNC can be implemented either as a modification to an existing NC system or by a complete retrofit. The first involves use of a behind-the-tape-reader (BTR) approach and can be implemented if the existing NC system is adequate. However, if the NC system is old and obsolete, the user may redesign his system around computer numerical control (CNC). Both are valid approaches. In some cases, the two can be combined.

As his first step in "taking another look," Mr Hudson reviewed the benefits of a DNC system consisting of a supervisory computer tied to an individual NC at each machine tool. This setup—which might additionally be linked with a mainframe data processing computer at a central facility—can be a complete control and feedback system that not only manages shop operations but also provides necessary manufacturing information.

Benefits of DNC include elimination of paper tape handling and the ability to make immediate program changes—even from the shop floor—as well as provision of realtime management information and access to remote computers from the shop floor. In addition there now are features available that were not practicable even a year or two ago. For example, on a typical system now in use, as many as 50 machine tools can be linked to a single control computer via serial full duplex communications, online machine control data storage can be almost unlimited, and data fed into the machine can be of practically unrestricted length, there is no need for costly multiconductor cables, large buffers can store the total library of machine tool information locally, and up to 8000 ft (2400 m) of data can be fed in—as opposed to a 300-ft (90-m) previous limit.

Additionally, recently provided capabilities enable blocking of machine control by logical operations through buffering, high level diagnostics that predict machine and tool wear, performance threshold monitoring and alarming, and reliability of control through use of dual computers. These identical DNC computers enable the data base management system to maintain data in nonredundant fashion while still providing control redundancy that allows one computer to assume full control if the other fails. [Mean time between failures (MTBF) is said to now be 100,000 h instead of 2000 h for a single computer system.] Also, parts programs are now stored and compiled at the DNC computer and many other factory operations are under computer control—affecting virtually every aspect of the manufacturing process.

When revamping existing NC systems, a BTR provides the necessary DNC connection by electrically interfacing with the controller of the NC paper tape reader. Not only is this technique the quickest and least expensive method of providing DNC, it works with all types of existing NC—no matter how old—and even with a wide mix of tools made by different manufacturers. It provides benefits of DNC without the cost of new controls and drives, retains investments in proven parts programs, minimizes machine downtime, and is cheaper overall—particularly



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COMPUTER DESIGN 8/78

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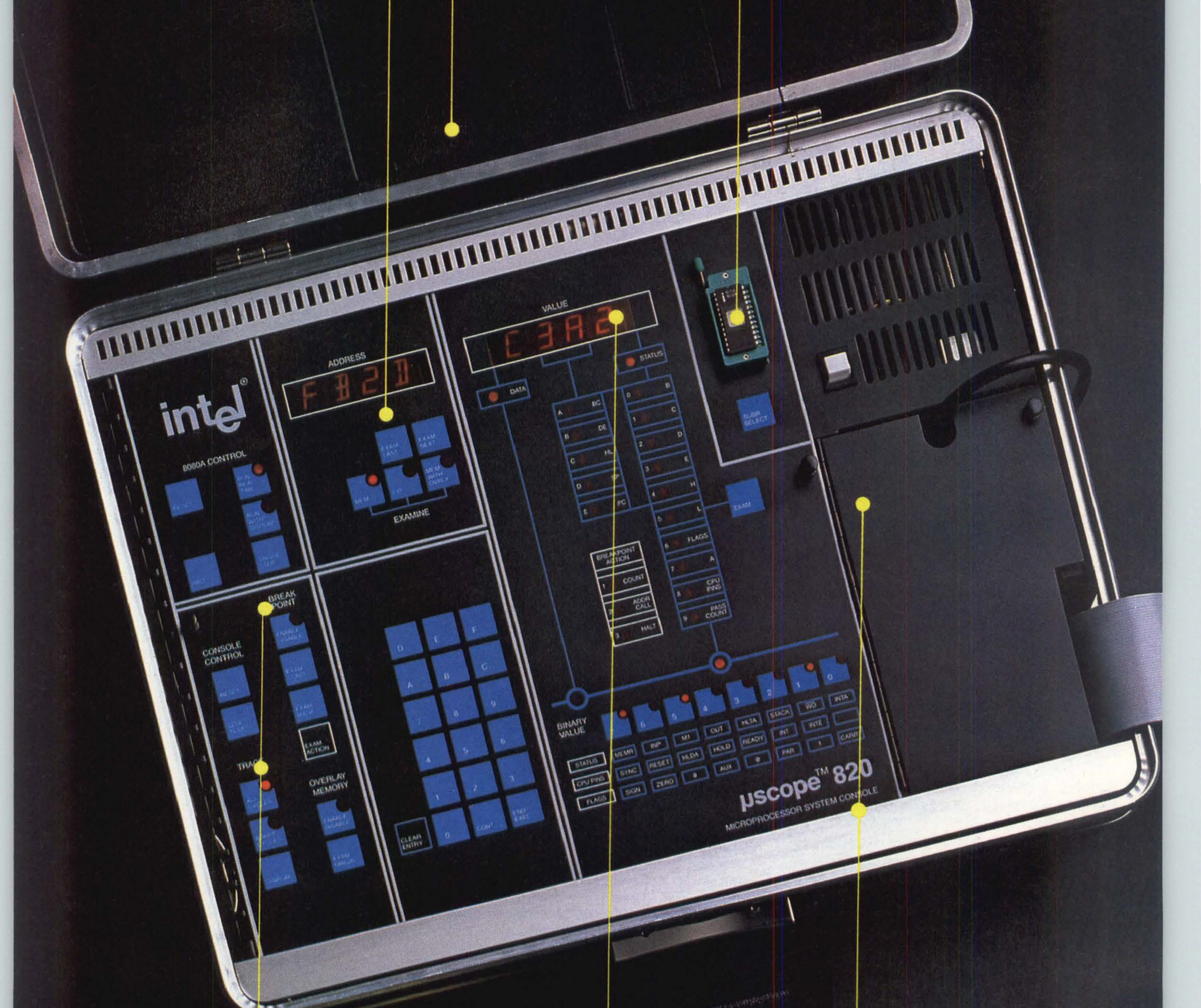

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CIRCLE 28 ON INQUIRY CARD

now that the necessary intelligence at the machine tool can be provided by a microprocessor.

Microprocessor based stored program buffers (SPBS) provide full duplex communications with the DNC or alternately with a remote timeshare computer via data link, memory to store the equivalent of up to 500 ft (150 m) of tape, and operator selection of program and/or block. Cassette tape or floppy disc memory can be added for local offline storage and part program entry and a plotter can be included for plot verification. This configuration retains the paper tape reader so that it can be used if the DNC fails or even while the DNC interface is being installed.

Computer numerical control (CNC) should be considered as an alternative to NC if controls are old or obsolete or if a new factory is to be designed. Mr Hudson pointed out that CNC "offers many advantages and improvements over NC." A CNC system, which replaces punched tape with a data cartridge or floppy disc, permits modification and recording of machine control data and provides both on- and offline diagnostic capabilities—all *at the CNC.* In addition machining data and operator instructions can be displayed on a CRT for easy viewing. All manual handling of data can be eliminated, response time or part programming cycle time can be improved, and machine data can be retrieved in real time via 2-way communications.

Mr Hudson stressed that each technique—revision, retrofit, or combination—has advantages. The potential user must review his present installation, his requirements, and the pros and cons of DNC and CNC—and then make his own decision.

Symbolic Control

Numerical control, whether direct numerical control (DNC) or computer numerical control (CNC), is based on techniques that are 30 years old, and according to Mr Donald C. Cumming of Symbolic Systems "it is time to rethink our concepts of machine tool control and develop new directions that will reap even greater gains in machine tool productivity." Mr Cumming believes that NC inherently places restrictions on the machine process. Adding a computer in a net of NC machine tools (DNC) or placing a computer on each machine tool (CNC) does not remove the restrictions ("The Coming Age of Symbolic Control").

According to Mr Cumming there are several of these restrictions. For example, control information is input from a *single source,* whether tape or an electronic device. Also, data presented to the tool are *sequential.* The machine tool's steps are performed in a set order predetermined by the commands; they cannot be modified unless a new set of commands is prepared. Next, the process is *numerical,* with each command reduced to a series of numbers that alone mean nothing to the operator. Finally, the NC process does *not* obtain data *in real time.* Data are based on conditions that existed at the time the part was programmed.

"Symbolic control," on the other hand, "is the control of the machining process through the use of multiple sources of data executing symbolically defined realtime machining procedures." Information needs are obtained from multiple sources. Although tape is still used, the operator can become an active part of the process to improve productivity in real time. In addition, data presented to the machine do not have to be sequential. The machine procedure is flexible and allows the computer to change the order of steps in real time as the part is being machined. Also, information input is based symbolically at both part description and machining procedure levels and the control operates in real time. "The key difference between the symbolically controlled machine and the numerically controlled machine is the ability of the symbolically controlled machine to integrate in real time data inputs from multiple sources and to operate from symbolically based machining procedures."

Mr Cumming claims that symbolic control allows return of the learning curve to the machining process.* Whereas NC makes it difficult or even impossible to tie in experience, symbolic control allows man to observe the machining process and to use the knowledge gained to improve the machining process.

Adaptive control methods, too, can be developed. NC does have the capacity for limited process adaptive control. However, it cannot be geometrically or operationally adaptive; it cannot change metal removal strategies or reorder sequences. Symbolic control has capability for all three.

The potential user must review his present installation, his requirements, and the pros and cons of DNC and CNC—and then make his own decision.

"It is time to rethink our concepts of machine tool control and develop new directions that will reap even greater gains in machine tool productivity."

Symbolic control allows return of the learning curve to the machining process.

*See "Learning Networks Improve Computer-Aided Prediction and Control," R. L. Barron, *Computer Design,* Aug 1975, pp 65-70

To illustrate the relation of symbolic control to NC, Mr Cumming defined 10 levels of machine control. The lowest four levels are for NC: 1—simple multiaxis NC machine with fixed sequential numeric input; 2—CNC without accessible memory (today's level); 3—CNC with extensive online memory; and 4—CNC with built-in postprocessor.

Next are basic symbolic control levels: 5—without decision making capability (similar to level 3); 6—with logical decision making capability (true definition of a symbolically controlled machine); and 7—with computer programmed control (level 6 but with user added programmed memory). Three further symbolic control levels exist: 8—integrates process, geometric, and operational adaptive controller; 9—returns learning curve to adaptive control, remembers optimization from one part to the next, and generates new tape; and 10—the "intelligent machine" (level 9 with the capability for long term optimization).

The Microprocessor

No one device seems to have influenced advances in machine tool control more than the microprocessor. Mainframe computers were impractical for such control functions; and even the minicomputer, although far less expensive, has been too costly for effective use in machine tool control. The microprocessor (and the resultant microcomputer), however, can now meet the basic requirements. It is capable of standalone control of individual machine tools or can function as local controller under direction of a central computer—and is cheap enough to be economically practicable.

At the Machine Tool Forum, Mr J. W. Froggatt of Westinghouse's Computer & Instrumentation Div discussed in detail the effect that this would have on the machine tool industry ("Impact of New Microprocessor/Microcomputer Technology on the Future of Machine Control"). A key point was that the control engineer has been able to take advantage of advanced technology and design capability in fields outside of his own. Although "he must learn about the product to apply it . . . (he) does not need in-depth knowledge of the inner workings." He can buy a vendor's product, such as a floppy disc controller, that contains a microprocessor and the necessary software to perform the function. He also can buy the microprocessor and all peripheral chips such as I/O and memory to comprise a microcomputer.

No one device influenced advances in machine tool control more than the microprocessor.

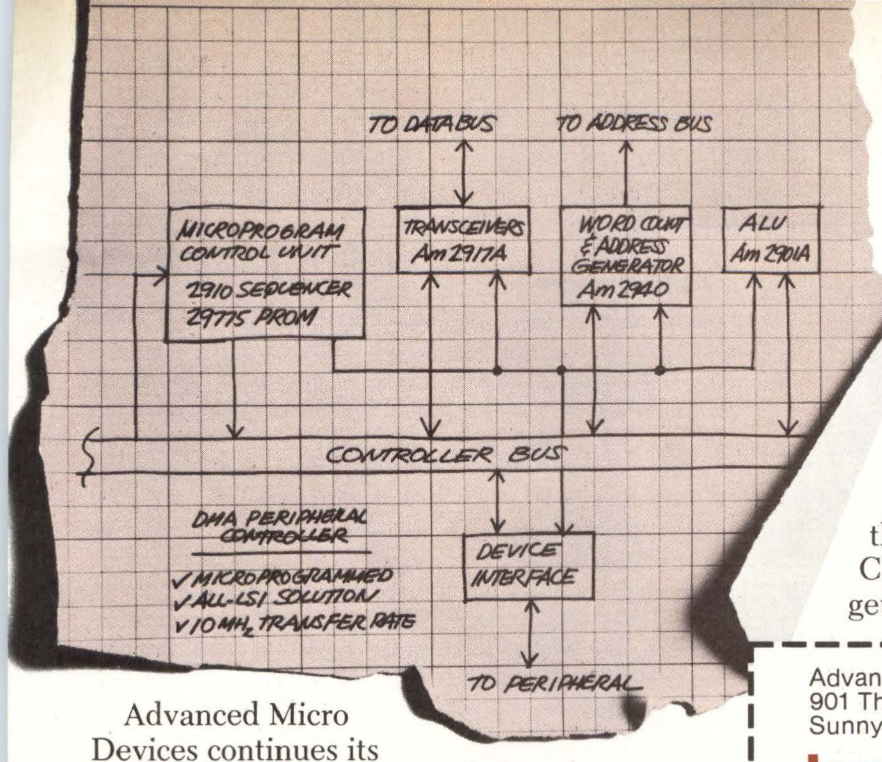
Mr Froggatt said that predicting the impact of microprocessor/microcomputer technology on the future of machine control has two aspects: the continuation of the trend of evolving improvements in existing products and methods, and the quantum jumps in control technology and productivity due to new ideas that emerge as designers discover what the new components can do for them. Initially, the trend toward distributed intelligence and remote intelligence will continue. As control components get smaller, more powerful, and cheaper, they will be feasible for use in smaller machine tools, will provide more sophisticated control, and will offer better diagnostic capability.

"Better design tools and more powerful, comprehensive components will allow the control design engineer to expand his imagination and scope of design capability. He will have a wider choice of modules and controls to purchase and at the same time have more capability to design and build on his own. He will be able to concentrate more on the needs of the manufacturing processes.

"Better standardization in programming languages and in input/output interfaces will allow better interchange of ideas, designs, and application technology."

"Better standardization in programming languages and in input/output interfaces will allow better interchange of ideas, designs, and application technology, enabling more effort to be spent in new areas. This standardization will also permit machine controls to be augmented with intelligent control products and more easily retrofitable with new control features."

Mr Froggatt also said that with "the arrival of big jumps in raw computational capability, many of the ideas now being tried in the laboratories and universities with minicomputers and larger computers will become practical realities for applications in the factory. Many of the ideas used now in large graphic CAD systems will become economically feasible for application to smaller users, who actually have the greater need for better, more machine shop oriented methods of inputting instructions to machine controls. At MIT recently, an experimental control system for machine tools was demonstrated which allows the skilled machinist to display a drawing of a part on the screen of a video display and to move a simulated tool as he would to remove metal to form the desired part. An attached computer automatically generates the numerical part program for later producing the parts. The machinists, who had no past programming background, were able to program with this method in a relatively short time. The new trends in microcomputers will enable ideas such as this to be an affordable, practical product." Still other research areas related to machine tool control in which the microprocessor may be useful are artificial intelligence, voice recognition, and robotics.



Advanced Micro Devices continues its course in advanced microprogrammable microprocessing.

This week, we'll look at the latest addition to the Am2900 family.

Chapter Seven, DMA.

In every computer system you'll find peripherals: discs, line printers, modems. In high-performance systems, data transfer between peripherals and memory is generally handled through a direct-memory access, or DMA, channel. And with today's high-speed peripherals, it has to be fast.

That's where the Am2940 comes in.

The Am2940.

It's a word count and address generator for DMA channels, an expandable 8-bit slice that generates an address and keeps track of the number of words transferred. (Just three parts give you a full 24-bit address.) And it's fast enough to keep up with a 10MHz transfer rate.

On each and every transfer you can increment or decrement the address and word count. Then, when it's all over, the Am2940 signals "done."

Are you looking for high speed in your DMA? Or low parts count? Would you settle for both? Ask about the Am2940.

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Each of these monthly messages is backed by a ton of theory and applications information. Send in this coupon and we'll send you Chapter Seven and tell you how to get the whole book.

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BUILDING A MICROCOMPUTER, CONTINUED.

DC&AS BRIEFS

Microprocessors Control Energy Management Systems

Microprocessors are the key elements in each of three different energy control and management systems introduced recently. One is intended for residential and commercial applications, a second is designed for small and medium size commercial and industrial customers, while the third is for use in large complexes. However, the promise inherent to all is energy savings.

Home Systems

Ecotroller™, a system announced by Ecotronics Inc, 8502 E Cactus Wren Rd, Scottsdale, AZ 85253, provides 16 individually programmable channels for residential and commercial uses. Its 24-V outputs drive relays and solenoid valves for control of setback thermostats or interior/exterior lighting as well as time control of appliances and sprinkler or drip irrigation systems. Control is maintained by a Motorola M6800 microprocessor. Pushbutton keyswitches allow new times to be entered, stored times to be examined, or previously programmed intervals to be overridden.

Timing is based on a repeating cycle of 14 24-h periods (cycle days) and is accurate to within 1 min/yr under normal operating conditions. A channel may be programmed with one or two control intervals during which time that channel provides 24 V at its rated output. Intervals may range from 1 min to 24 h in duration. Each channel may be programmed with its own intervals and may be set to operate on any day or days within the 14-day cycle.

Circle 160 on Inquiry Card

Commercial Installations

Energy management system model 50 for small and medium size commercial and industrial installations uses microprocessor control to monitor up to four different metered inputs on energy consumption. One to 64 loads can be controlled by peak demand limiting, total consumption limiting, and independent control function limiting such as time-of-day scheduling.

A human-engineered control panel allows an operator without knowledge of computer language to effectively modify all system parameters that are programmed into P/ROMs. All new program entries are automatically checked for validity and errors are indicated for correction. The system continuously checks its own internal hardware for proper operation and has a built-in system checking procedure for locating hardware failures quickly. Available from Franklin Electric Energy Conservation Products, 995 Benicia Ave, Sunnyvale, CA 94086, the system can be expanded in the field to meet changes in customers' requirements.

Circle 161 on Inquiry Card

Large Complexes

Delta distributed computer control system (Delta DCC), a system introduced by Honeywell Commercial Div, 10800 Lyndale Ave South, Minneapolis, MN 55420 for monitoring building functions and managing energy in large complexes, is said to offer payback of investment in one to three years, based on energy savings of 20 to 30% that are typical with such systems. (An earlier model installed at Camp Pendleton Marine Corps Base reduced energy consumption by nearly 50% in 83 buildings audited by the U.S. General Accounting Office, avoided over $900,000 in fuel and electrical costs in the first two years of operation, and assumed the monitoring duties of 29 men.)

Basic element of Delta DCC is a Delta 1000 microprocessor-based control and monitoring system including sensors, data-gathering panels, and peripherals. Each Delta 1000 can be dedicated to a particular function within a building, such as energy management, fire protection, security, or monitoring of electrical and mechanical systems; but it also communicates to the master control center over a data bus.

Circle 162 on Inquiry Card

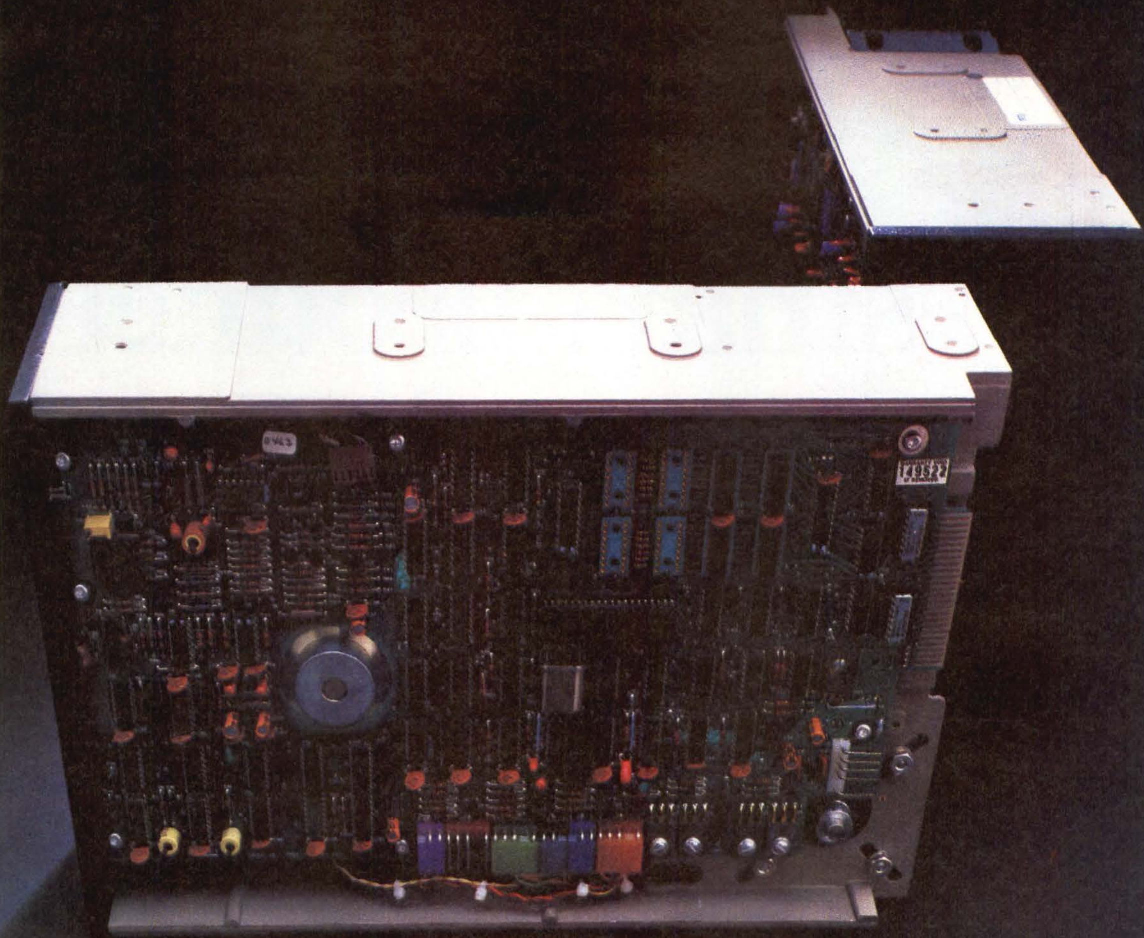
Calculator-Based System Reduces NC Programming Time and Errors

An interactive computer program that reportedly simplifies the programming of numerical controlled equipment has been made available in North America by Centech, Inc, 10835 N Dearlove Rd, Glenview, IL 60025, a subsidiary of CECN Industrie SA of Lyon, France. Called ELAN, the system is said to reduce the time required to prepare a program in some cases by 70% over standard methods for a machining operation, and to provide virtually an error-free program.

Programmer and Hewlett-Packard calculator-processor interface in conversational mode; the calculator asks questions on its display concerning the geometrical definition and machining operation of the part to be produced, and the programmer responds with simple answers or relevant data. Typically the system defines all machining functions into a series of points, lines, and circles. Then the programmer reduces the part to be machined into geometrical elements and feeds the information into the calculator through a series of answers to the calculator's questions. As the data are entered, the calculator provides a continuous printout of each step and a high speed plotter monitors the program by plotting the profile of each step.

Syntax and logic errors are noted in the calculator printer or display. All geometries are substantiated by an X-Y plotter which shows the scaled dimensions of the element as defined (inches or metric), and plots the geometry sequence for the total profile and the tool path. A high speed punch produces the final tape through a fast postprocessor. □

Circle 163 on Inquiry Card



Disk drives or subsystems?
Remex announces two low-cost controller/formatter/drives.

The RFS 1100 and micro-based 1200 are part of the Remex family of disk drive subsystems, complete with built-in controller/formatters.

Now time and money you might otherwise spend developing your own controller/formatter can be concentrated on application software and total systems — where you can make the greatest contribution.

The savings are sizable, even if the subsystems are not — many man-months of development time and dollars. And that's not considering getting your system to market months sooner.

Whether your system is based on a popular minicomputer or microprocessor, we've got the application notes and assistance capability to help make interfacing a breeze.

Both units are media compatible with the IBM 3740, 3540 and System 32. In fact, they'll read sectors of any length, provided standard IBM header information is used.

And both feature the Remex high quality disk drive hardware, with head geometry identical to IBM, assuring precise media interchangeability now and later on.

The RFS 1100 is available in 3 models, including 2 with buffers that permit greater CPU efficiency in your system.

The RFS 1200 has its own integral microprocessor for maximizing system speed and minimizing software overhead. It's available in a master/slave configuration for reducing costs in multiple drive applications.

Only Remex offers so much for so little in such neat, integrated packages — with nearly 20 years of electro-mechanical experience and nationwide field service to back it up.

Call or write today for complete information on complete subsystems. Ex-Cell-O Corporation, Remex Division, 1733 East Alton St., P.O. Box C19533, Irvine, CA 92713.
Phone: (714) 557-6860. TWX: (910) 595-1715.

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REMEX DIVISION

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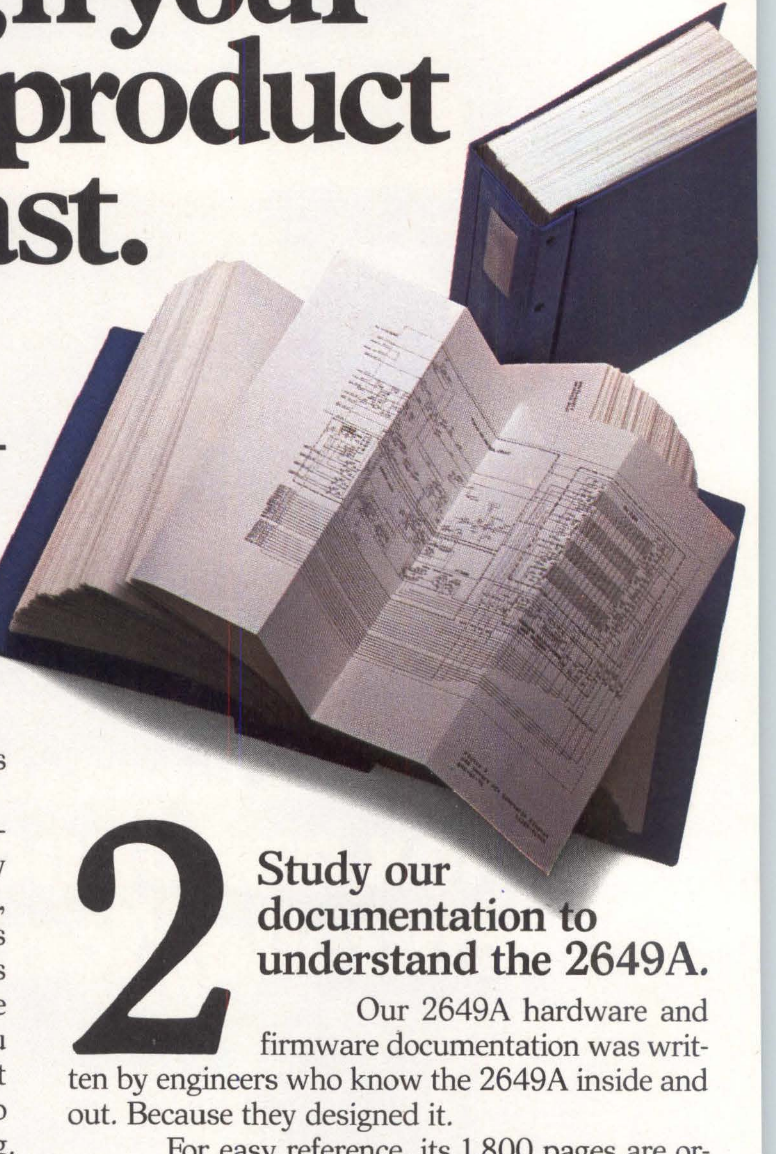
CIRCLE 29 ON INQUIRY CARD

Design your smart product fast.



1 Start your microprocessor-based product with HP's 2649A.

It's an 8080 MPU, CRT, display subsystem, power supply and 15-slot backplane, all in a good-looking case.

You choose the RAM, PROM, ROM, serial or parallel I/O, dual cartridge tape drives or keyboard you need for your product.

Then take advantage of our standard firmware, including utility subroutines for data display manipulation, keyboard switch translation, data transfer and communcations protocol. It's software you don't have to write and debug.

2 Study our documentation to understand the 2649A.

Our 2649A hardware and firmware documentation was written by engineers who know the 2649A inside and out. Because they designed it.

For easy reference, its 1,800 pages are organized in two volumes like an encyclopedia. So, for example, if you need the pin assignments for our keyboard interface module, it's easy to look up. And you'll find the details in the words of the engineer who designed it.

The more you know about our product, the less time you'll spend on yours.

3 Write, assemble and debug your software on the 13290B Development Terminal.

The 13290B has a source program editor so you can quickly write 8080 assembly language programs. A resident assembler to convert source programs into 8080 object code. 64K bytes of RAM as a test bed for your software. And a friendly, interactive debug program that lets you watch your program run step by step, in mnemonics, not ones and zeroes.

And because the 13290B *is* a 2649A, your program runs in your product's environment, which is a big help if timing or execution speeds are important.

It's probably the only development tool you'll need.

4 Get hands-on experience at our 2649A workshop.

Monday morning we'll ask you about your product. Then we'll spend five days showing you how to use the 2649A, 13290B and documentation to make it.

Of course, in just five days you probably won't be able to design your product completely. But by Friday night you'll have a good head start.

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5 Send us this coupon.

We'll tell you more about how HP's 2649A OEM Support Program will help you design your smart product fast.

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Company ____________

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My smart product is ____________

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Mail to: Hewlett-Packard, Attn: Ed Hayes, Marketing Manager, Data Terminals Division, Dept. 1226, 19400 Homestead Road, Cupertino CA 95014.

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CIRCLE 30 ON INQUIRY CARD

An E-sized drawing in 13.5 seconds.

Gould's 5400 printer/plotter will produce an E-sized drawing in 13.5 seconds. That's faster than any competing electrostatic printer/plotter. With a paper width of 36" and a speed of 3.25"/second, the 5400 generates over 48 square feet of hardcopy per minute.

Designed for applications where fast turn-around and high throughput rates are important, the 5400 is ideal for computer-aided-design, seismic data plotting, and business graphic applications such as PERT/CPM, Gantt, and others.

Gould's patented negative-pressure, closed loop toning system ensures high contrast dry hardcopy even at the maximum plotting speed of the 5400.

Print resolution is 100 dots per inch, horizontal and vertical. In addition, a staggered image head produces overlapping dots for high contrast images. A user-oriented control panel features a unique LED system for continuously monitoring paper supply.

For additional information on Gould 5400 printer/plotter capabilities, software, interfaces and special application packages contact your Gould representative. Or write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, Ohio 44114 (216) 361-3315. For brochure call toll free: (800) 325-6400, ext 77. In Missouri: (800) 324-6600.

GOULD

CIRCLE 31 ON INQUIRY CARD

Wescon/78

Dr C. Lester Hogan
Keynote Speaker

Western Electronic Show and Convention / September 12-14
Los Angeles Convention Center / New Bonaventure Hotel

Joseph Statsinger
Program Chairman

Accenting the theme Micro/Evolution, Wescon/78, the 27th annual Western electronics show and convention, will be previewed on Monday, September 11 and will run for three consecutive days thereafter. The Los Angeles Convention Center and the Bonaventure Hotel are the sites for the keynote luncheon, marketing conference, exhibits, film theater, professional program sessions, and awards programs.

On Monday, September 11 the keynote luncheon will be held at the Bonaventure Hotel, and will be augmented by the second annual presentation of the Don Larson Award, which honors outstanding contributions to Wescon. Keynote speaker for the luncheon will be Vice Chairman of the Board of Fairchild Camera and Instrument Corp, Dr C. Lester Hogan. Electronics marketing awards will also be presented at this time, the purpose being to encourage college students to pursue careers in electronics marketing and sales.

Moving into Wescon/78 itself, Tuesday through Thursday will feature exhibits, sessions, and awards programs. The All-Industry Reception will take place on Tuesday evening from 6:30-8:30 pm in the Bonaventure's California Ballroom, with "Auld Lang Sine" setting the mood for this $9.50/person event. 423 exhibitors will display products and systems from 9:30 am to 6:30 pm on Tuesday, 9:30 am-7 pm on Wednesday, and 9:30 am-5 pm on Thursday. A special theme exhibit displaying the winners of "Microprocessor Applications Center and Awards Program," which encompasses eight categories of microprocessor use, will highlight the Convention Center floor.

Thirty-six professional program sessions will cover technical topics such as the future of single chip microcomputers, design and installation considerations for fiber optic links, control systems, and legal rights and security developments. Program sessions will be held each day from 10 am-12:30 pm and from 2-4:30 pm. Chairman for the program this year is Joseph Statsinger, Aerospace Corp, El Segundo, Calif.

Wescon Flyer commuter bus lines will operate every 20 min to and from major suburban areas and the Convention Center for a roundtrip fare of $2. Two downtown shuttle lines will also provide transportation in 15-min intervals for attendees traveling in that section of town.

Wescon/78 is sponsored by the Los Angeles and San Francisco Bay Area Councils of IEEE and the Northern and Southern California Chapters of ERA. Advanced registration fee is $5, with an August 25 deadline. After this date, fees will increase to $6 for IEEE members and $9 for nonmembers. For further information, write to William C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245, or call (213) 772-2965.

Only sessions of interest to *Computer Design* readers will be covered in the following pages.

Professional Program Excerpts

Tuesday Morning

Session 1 — 10 am-12:30 pm

Industrial Control Systems Using Mini/Micro Computers

Organizer: Dr George W. Zobrist

This session will present ideas on the trend of using mini/micro computers as the controlling element in industrial applications. The trend will be discussed in papers on computer control, turbine blade temperature acquisition using an optical pyrometer and microcomputer, dc servo control, and an adaptation of BASIC for realtime applications.

Session 2 — 10 am-12:30 pm

Advances in Applied Computer Imagery Generation

Organizer: Dr Ted Zavodny

Recent advances in computer imagery generation (CIG) techniques have enhanced the realism of simulated images. State-of-the-art systems generate realistic, high resolution images by incorporating models which include effects of curved surfaces, variable shading, environmental conditions, illumination, highlighting, texture, and other special effects. This session will involve disciplines such as flight simulators, pilot training, animation, architectural design, multispectral sensor imagery simulation, and automatic student instruction, which all utilize these systems.

Session 3 — **10 am-12:30 pm**

Programmable Bipolar Logic for High Performance Application

Organizers: T. A. Longo and J. M. Early

Nanosecond and subnanosecond gate arrays and other programmable bipolar logic arrays bring LSI savings to digital system design. Product and technology advances and applications will be presented—particularly LSI gate fuse link and ECL gate arrays, and the use of high speed P/ROMs in Boolean function generation.

Session 6 — **10 am-12:30 pm**

Personal Programmable Calculators Come of Age

Organizer: Richard J. Nelson

Applications and daily usage of personal programmable calculators have increased in 1977 and 1978. Wide range of topics including design considerations, applications studies, usage in education, and advanced applications will be presented here to demonstrate the present state of programmable calculators.

Tuesday Afternoon

Session 7 — **2-4:30 pm**

Single-Chip Microcomputers—Distributed and Multiprocessing Techniques

Organizer: Jim Vittera

This session will attempt to determine the architectural evolution of 8-bit single-chip microcomputers and to investigate the implementation of large computer concepts such as multiprocessing and distributed processing as they apply to single chip microcomputers. Topics to be covered include architectural features of each machine that allow multiprocessing and distributed processing and techniques of using these features to implement multiple CPU systems.

Session 8 — **2-4:30 pm**

Computer Based Energy Management Systems

Organizer: D. Genovese

This session will cover several areas of the Energy Management System marketplace from the points of view of owners, engineers, and suppliers. The highlights of an ongoing survey of major universities and colleges will be presented. Department of Energy will give an overview from the Federal viewpoint.

Session 9 — **2-4:30 pm**

Advances in Bipolar Memory

Organizer: Thomas A. Longo

The variety, size, and complexity of bipolar memories are increasing. Advances in static, programmable read-only memories, including fast accessing and power down arrangements together with progress on large static bipolar memories and design limitations will be discussed. Future developments in bipolar dynamic memories will be predicted during this session.

Wednesday Morning

Session 14 — **10 am-12:30 pm**

Evolution of the 16-Bit Microprocessor

Organizer: James M. Early

Implications and possibilities for users of bipolar, n-channel, and CMOS 16-bit microprocessors are brought out in this session along with a discussion of compatibility in microprocessors. Special emphasis is placed on software origins and implications of various approaches.

Session 15 — **10 am-12:30 pm**

Modern Communications Techniques and Applications: Part I

Organizer: Bernard Sklar

Consisting of tutorial papers on digital communication technology including detection of digital waveforms, coding scenarios, and synchronization techniques for digital communication systems, session will attempt to blend theoretical basics and present day applications.

Session 16 — **10 am-12:30 pm**

The Impact of New Memory Technologies on Computer Design

Organizer: Andy Santoni

Hardware for computer data storage including large semiconductor RAMs, charge-coupled devices, bubble memories, and compact magnetic media are replacing core and other traditional memory equipment. This session will explore computer memory devices and their applications and how computer design can be changed to take advantage of this new storage media.

Session 19 — **10 am-12:30 pm**

Process and Device Modeling for VLSI Design

Organizer: C. D. Maldonado

The field of very large-scale integration (VLSI) is important because of its potential economic impact on the microelectronics industry during the next decade. In this session process and device modeling for integrated circuit design will be discussed with special emphasis on VLSI.

Wednesday Afternoon

Session 20 — **2-4:30 pm**

A Close Look at the 16-Bit Microcomputer: Past, Present, and Future

Organizer: Rudolf Panholzer

This session will look at new 16-bit microcomputers including the Intel 8086, Motorola MACS, and Zilog Z8000, alongside the minicomputer oriented micros, DEC LSI-11, TI 9900, and Fairchild 9440. The main goal of this session is to compare these two categories and to speculate the future.

Session 21 — **2-4:30 pm**

Modern Communications Techniques and Applications: Part II

Organizer: Bernard Sklar

This session will provide tutorial papers on digital communication technology including papers on satellite channels, communications systems, and digital techniques. As in Part I, the scope is a blend of theoretical basics plus present day applications.

Session 22 — **2-4:30 pm**

Memory Technologies: Systems Considerations and Applications

Organizer: Richard H. Lee

This session will present a tutorial paper on memory system architecture, focusing on speed, density, and cost considerations for various parts of the system. MOS, bipolar, CCD, and bubble memories will be examined from a technology and applications viewpoint as they relate to system architecture.

Session 25 — **2-4:30 pm**

Designing with Single-Chip Multipliers

Organizer: Alan J. Weissberger

Concentrating on application aspects of single-chip multipliers and high performance arithmetic units, this session will be comprised of paper presentations and a panel discussion. Topics to be considered include significance of the units' application to the practicing engineer, device characteristics and functional organization, system design examples, and applications in digital filtering, FFT, matrix operations, microprogrammed minicomputers, and 16-bit microprocessors.

If logic board testing problems have you feeling like this...

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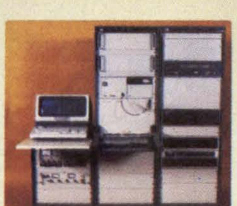

Testing may be your most frustrating and costly production bottleneck. But now, HP can help you make the right move in logic-board testing. Here's how the DTS-70 can help you increase throughput while cutting production and warranty costs.

HP's simulator-based system, at a cost roughly equivalent to comparison testers, increases testing efficiency. It gives known fault-detection effectiveness. And it provides design feedback by analyzing circuits for failure modes and testability before they're even built.

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Independent test-program generation, using a separate station and the DTS-70's minicomputer, eliminates a big bottleneck by allowing test-program generation while testing is in progress on the same system.

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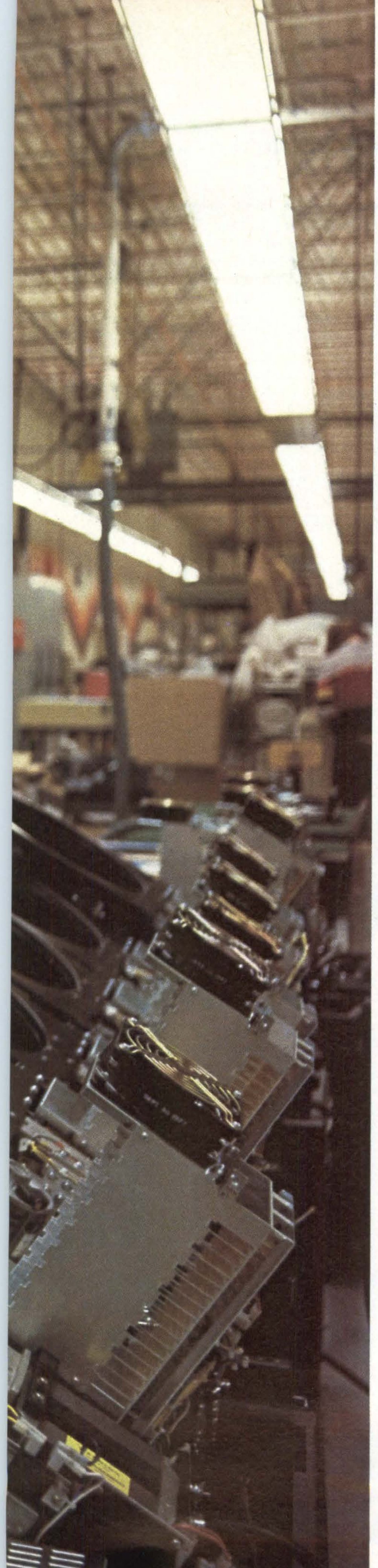
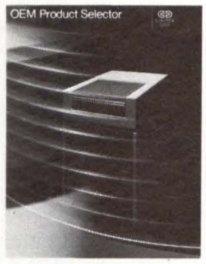


"We can help you put quality behind your nameplate."



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"As one of the world's largest suppliers of OEM equipment, Control Data knows what your customer is looking for.

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Dale C. Showers
Vice President O.E.M. Marketing

CIRCLE 33 ON INQUIRY CARD

Thursday Morning

Session 27 — 10 am-12:30 pm

Single Component Microcomputers: A Better Solution for Processor Type Design

Organizer: Rudolf Panholzer

Single component microcomputers present a cost-effective solution to design problems. Controller oriented microcomputers, which now incorporate more peripherals on the chip itself, will be introduced in this session. Specifically, the TMS1000 series family and the Zilog 28 will be discussed along with in-socket expandability and onchip A-D.

Session 28 — 10 am-12:30 pm

Speech Recognition and Processing

Organizer: William T. Bisignani

Research in improving man to man and man to machine communications via voice has been rapidly increasing. Factors contributing to this growth include improved speech signal processing techniques and advances in computing hardware. This session will present recent work in several speech processing areas including word and speech recognition, speech synthesis, speaker verification, and speech intelligibility enhancement, as well as provide an estimation of the relevance of automated speech techniques in the military.

Session 29 — 10 am-12:30 pm

Solutions for Microprocessor Product Testing

Organizer: Martin J. Weisberg

Digital fault isolation in microprocessor based products is a problem confronting general management, engineering management, production test managers, and field service personnel. This session will scrutinize various approaches for fault isolation, including circuit waveform display, signature analysis, and in-circuit emulation. Their effectiveness in design debugging, production testing, and field servicing will be assessed. Participants will discuss techniques in regard to speed of fault isolation, effectiveness in identifying defective components and circuit board defects, and cost effectiveness as compared with alternative techniques.

Session 30 — 10 am-12:30 pm

Reducing the Cost of Microcomputer Software Development

Organizer: Andrew A. Allison

This session will illustrate the needs of the microcomputer software designer by describing the evolution of software development within a major terminal manufacturer, then will discuss three approaches to improving efficiency, and hence reducing cost of software development. Two leading microprocessor manufacturers and an independent software house will be represented.

Session 32 — 10 am-12:30 pm

Alternative Procurement Approaches for Low to Intermediate Volumes of Custom LSI

Organizer: Jim Meyer

Six companies offering different approaches for custom LSI, including array or masterslice, the subcontractor route, or the full-service route, will each present a case stressing their individual choices. These choices will cover custom LSI design with IIL gate arrays, along with advantages of array or masterslices, and advantages/disadvantages of other custom LSI approaches.

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← "L" →	AWG 30 (0.25MM) KYNAR® WIRE INSULATION DIAMETER .0195 INCH (0.50MM) STRIP-OFF LENGTH BOTH ENDS 1 INCH (25MM) 500 WIRES PER PACKAGE				AWG 28 (0.32MM) KYNAR® WIRE INSULATION DIAMETER .023 INCH (0.59MM) STRIP-OFF LENGTH BOTH ENDS 1 INCH (25MM) 500 WIRES PER PACKAGE				AWG 26 (0.40MM) KYNAR® WIRE INSULATION DIAMETER .027 INCH (0.69MM) STRIP-OFF LENGTH BOTH ENDS 1 INCH (25MM) 500 WIRES PER PACKAGE			
LENGTH "L" INCH	BLUE PART NO.	WHITE PART NO.	YELLOW PART NO.	PRICE PER 500	BLUE PART NO.	WHITE PART NO.	YELLOW PART NO.	PRICE PER 500	BLUE PART NO.	WHITE PART NO.	YELLOW PART NO.	PRICE PER 500
1	30B-010	30W-010	30Y-010	$4.88	28B-010	28W-010	28Y-010	$5.25	26B-010	26W-010	26Y-010	$5.75
1.5	30B-015	30W-015	30Y-015	5.19	28B-015	28W-015	28Y-015	5.63	26B-015	26W-015	26Y-015	6.23
2	30B-020	30W-020	30Y-020	5.50	28B-020	28W-020	28Y-020	6.00	26B-020	26W-020	26Y-020	6.68
2.5	30B-025	30W-025	30Y-025	5.82	28B-025	28W-025	28Y-025	6.38	26B-025	26W-025	26Y-025	7.13
3	30B-030	30W-030	30Y-030	6.13	28B-030	28W-030	28Y-030	6.75	26B-030	26W-030	26Y-030	7.60
3.5	30B-035	30W-035	30Y-035	6.44	28B-035	28W-035	28Y-035	7.13	26B-035	26W-035	26Y-035	8.05
4	30B-040	30W-040	30Y-040	6.75	28B-040	28W-040	28Y-040	7.50	26B-040	26W-040	26Y-040	8.50
4.5	30B-045	30W-045	30Y-045	7.07	28B-045	28W-045	28Y-045	7.87	26B-045	26W-045	26Y-045	8.98
5	30B-050	30W-050	30Y-050	7.38	28B-050	28W-050	28Y-050	8.25	26B-050	26W-050	26Y-050	9.43
6	30B-060	30W-060	30Y-060	8.00	28B-060	28W-060	28Y-060	9.00	26B-060	26W-060	26Y-060	10.35
7	30B-070	30W-070	30Y-070	8.63	28B-070	28W-070	28Y-070	9.75	26B-070	26W-070	26Y-070	11.25
8	30B-080	30W-080	30Y-080	9.25	28B-080	28W-080	28Y-080	10.50	26B-080	26W-080	26Y-080	12.18
9	30B-090	30W-090	30Y-090	9.88	28B-090	28W-090	28Y-090	11.25	26B-090	26W-090	26Y-090	13.55
10	30B-100	30W-100	30Y-100	10.50	28B-100	28W-100	28Y-100	12.00	26B-100	26W-100	26Y-100	14.00

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100 ft. roll	R30B-0100	R30W-0100	R30Y-0100	$3.65	R28B-0100	R28W-0100	R28Y-0100	$4.05	R26B-0100	R26W-0100	R26Y-0100	$4.35
500 ft. roll	R30B-0500	R30W-0500	R30Y-0500	10.40	R28B-0500	R28W-0500	R28Y-0500	12.85	R26B-0500	R26W-0500	R26Y-0500	13.80
1000 ft. roll	R30B-1000	R30W-1000	R30Y-1000	16.82	R28B-1000	R28W-1000	R28Y-1000	21.10	R26B-1000	R26W-1000	R26Y-1000	23.15

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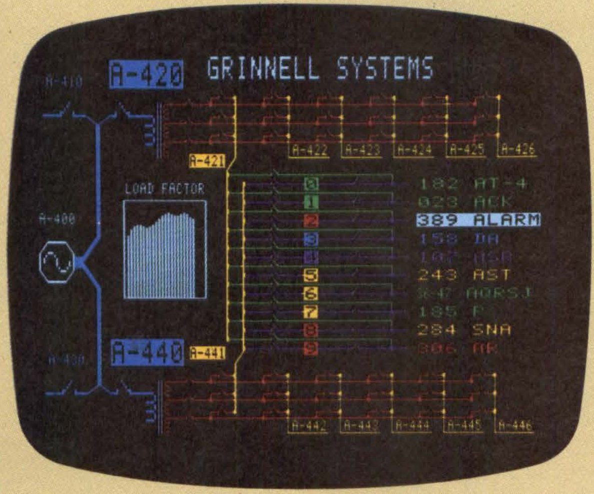

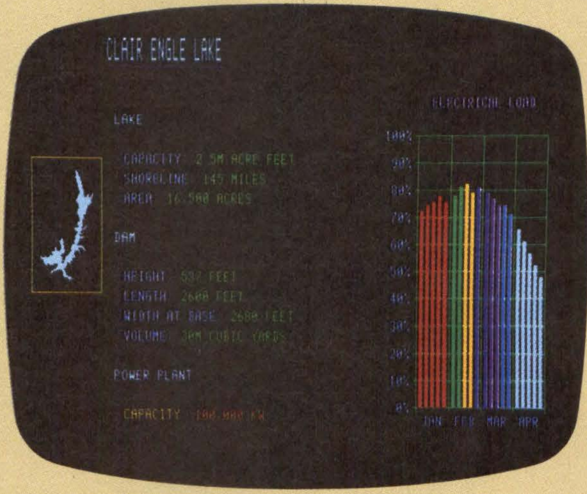

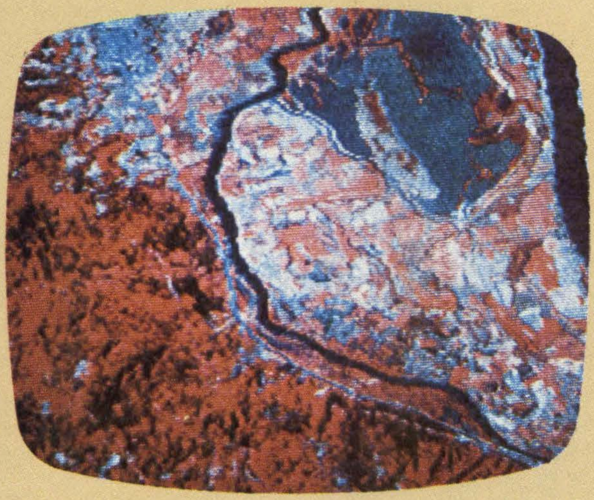

Full color image processing . . . greyscale and pseudo-color . . . basic B/W graphics . . . and everything in between: our 100% solid state, modular graphic television display systems can be matched to your computer display requirement, easily and economically.

And, they're intelligent. Powerful instruction sets minimize software overhead, simplify programming and eliminate the need for complex macro-instructions and high order programming languages.

Further, every Grinnell system includes a standard computer interface, full alphanumerics and graphics, 4K MOS random access refresh memories and your choice of standard resolutions: 256 x 256, 256 x 512 or 512 x 512. Plug-compatible interfaces for most minicomputers are available, along with a large number of operating options. All systems drive standard TV monitors.

Grinnell displays are already at work in tomography, ERTS imaging, process control, data plotting and many more applications.

So, before you decide on a display system, talk to our experts. Complete operating systems start at $5,450, and quantity discounts are available. For detailed specs and/or a quotation, call or write.

GRINNELL SYSTEMS

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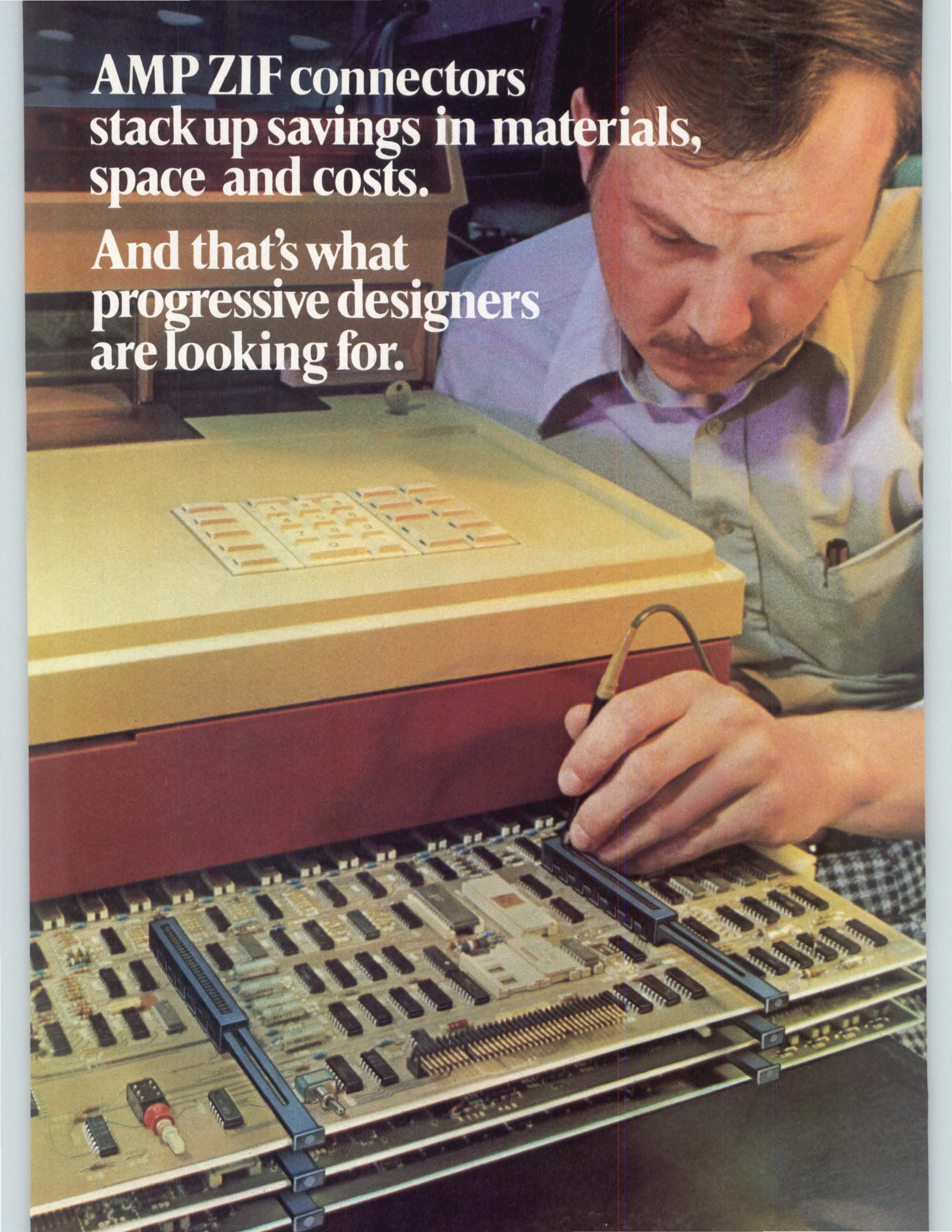
CIRCLE 35 ON INQUIRY CARD


AMP ZIF connectors
stack up savings in materials,
space and costs.
And that's what
progressive designers
are looking for.

Take our stacking zero insertion force connectors, for example. They effectively reduce costs, not only because they prevent board insertion damage but also because they eliminate board routing, beveling, and gold card edge fingers.

Their stacking design permits high density, bus organized packaging, eliminating backplanes and allowing shorter electrical paths from board to board. And card cages are no longer necessary. Add all these advantages and you can see why AMP stacking ZIF connectors are ideal for the new generation of microprocessors, intelligent terminals, and distributed processing systems.

There's another important advantage, too. AMP technical support. And it's available even when your product is in early development. In fact, that's when we urge you to get us involved. So you can take full advantage of the capabilities and willingness of our people to help you find a better way to increase your product's effectiveness.

There are more benefits in AMP ZIF stacking connectors: Maintenance is simplified because every board is accessible without the need for extender boards. Contacts are on .100″ grid spacing and feature the AMP Action Pin to reduce board hole damage.

Why not get the complete story on our Zero Insertion Force Stacking Connectors, as well as card edge types with side-entry capability. Just call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.

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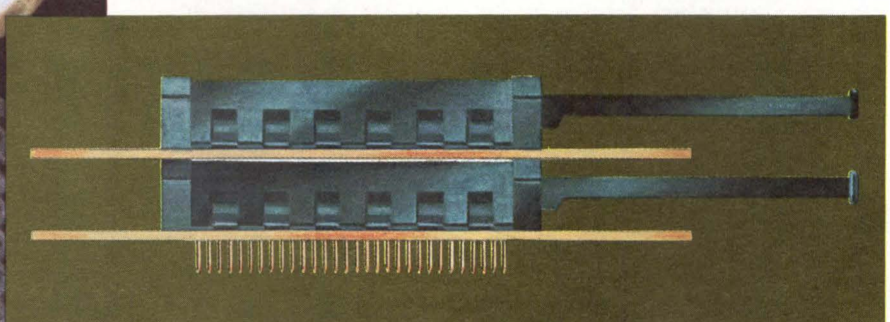

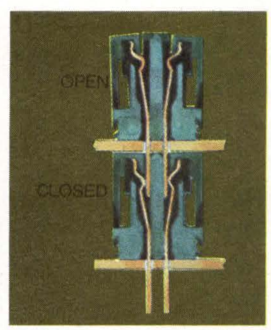

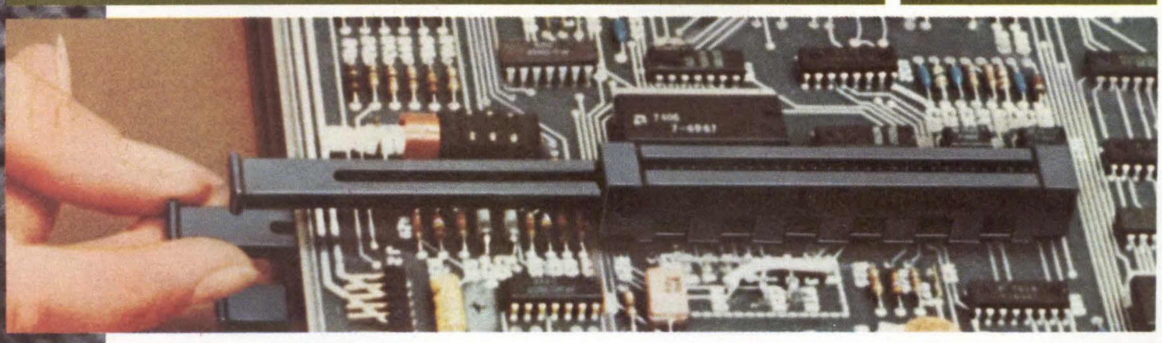

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CIRCLE 36 ON INQUIRY CARD

Thursday Afternoon

Session 33 2-4:30 pm

Structured Logic Design Using Fuse Programmable Logic

Organizer: John Birkner

Fuse programmable logic including the P/ROM, FPLA, FPGA, PMUX, and PAL allows the top down structure design of microprocessor systems architecture. This session will address the design methodology used to implement these fuseable devices as generalized Boolean transfer functions, synchronous state machines, and bus oriented microprocessor systems. Emphasis will be placed on a systematic approach to synthesis of optimal hardware functions.

Session 34 2-4:30 pm

Fiberoptic Links: Design and Installation Considerations

Organizer: David R. Weller

New approaches to fiberoptic links including specifications, terminations, field installation, and interconnections will be presented in this session. The objective is to offer ideas on design and field experience in developing and installing fiberoptic systems; for example, the handling of fibers in the field which includes splicing and termination of cables; and the design and miniaturization problems with drivers and receivers to insure reliable operations.

Session 35 2-4:30 pm

Automated Test and Control Systems— The Building Block Approach

Organizer: Robert L. Morrison

Recent advances in small computers and associated components required for automated test and control have necessitated improvements in the interconnection of these systems. The method that most facilitates interconnection of a large variety of different systems functions comes from the development of the IEEE 488 bus. This session will discuss the bus' operation and will present numerous application examples. Hardware necessary for bus interfacing will be explained, as well as techniques for troubleshooting. Finally, application of the bus to complete, automated systems will be discussed for both instrument and component based systems.

Session 37 2-4:30 pm

Problems and Solutions of Standardizing Design Methodology in Microprocessor Application Engineering

Organizer: Howard I. Cohen

This session will address the problem of establishing and applying standardization to the use of microprocessors in system design work. Levels of standardization that will be discussed encompass component selection, architectural characteristics, hardware design practices, programming language, busing methodology, unit and system level testing, and test equipment.

Session 38 2-4:30 pm

A New Breed of Integrated Circuits Invades Telecommunications Systems

Organizer: Rudolf Panholzer

Integrated circuits for telecommunication systems available for the design engineer will be discussed. Devices to be presented include tone and pulse dialers, dual-tone multifrequency detectors, variable slope delta modulators/demodulators, pulse code modulators/demodulators, and active filters. The session will be semitutorial and will emphasize both traditional and unorthodox applications. □

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Will be involved in the design and development of computer systems logic utilizing ECL and TTL logic families. Experience should include overall memory systems interface knowledge and general knowledge of computer systems architecture. Familiarity with IBM 370 architecture preferred. Minimum requirements are a BSEE plus engineering experience. We also have additional openings for individuals to assume project engineering responsibility for design and development of OEM memory for small add-on memory systems and/or storage board design

INTERSIL, the leading independent supplier of add-on main memory systems, offers exceptional advancement opportunities, a generous benefit package including profit sharing, and relocation. If you are interested in a move up, please send us your resume or call us collect to arrange an interview. INTERSIL MEMORY SYSTEMS, 1275 Hammerwood Ave., Sunnyvale, CA 94086. (408) 743-4300.

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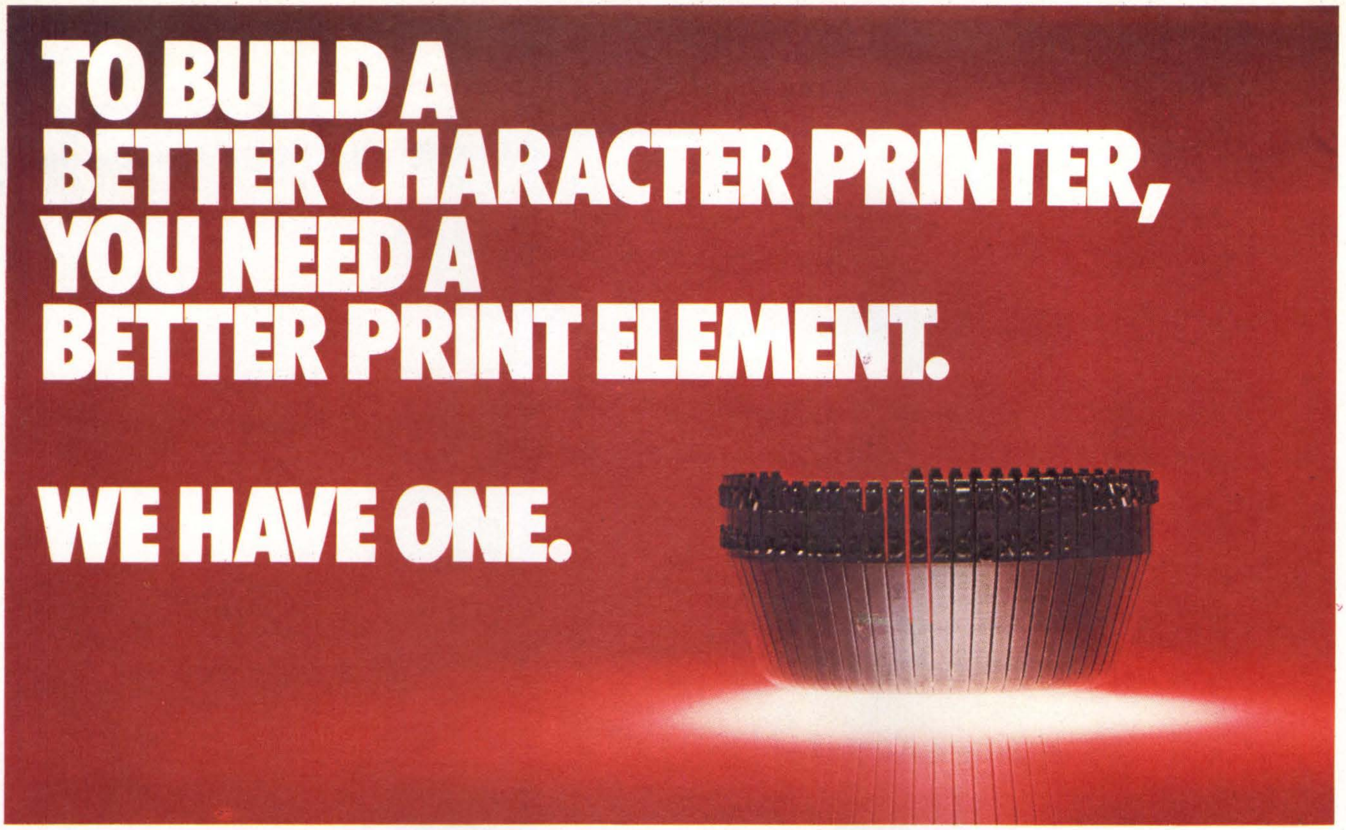
CIRCLE 37 ON INQUIRY CARD



THE NEC SPINWRITER "THIMBLE"

NEC built the Spinwriter family of bidirectional character printers to be better than today's best. That required a high quality print element able to outperform "daisy wheels," and we have one.

Our unique "thimble" print element lasts up to three times longer, prints faster, offers greater applications flexibility, and costs less than daisy wheel elements.

Spinwriter thimbles are made from plastic specially reinforced with fiberglass – and specially molded – to provide normal element life of more than 30 million impressions. Thimbles are smaller in diameter and lighter in weight than daisy wheels. They have less mass, which means they can reach the next character faster and, therefore, print at a faster effective rate.

Spinwriter thimble elements can print up to 128 characters compared with 94 printable on daisy wheels. One thimble can hold two type fonts, and output those fonts with OCR quality. That means a Spinwriter can be used even in those applications normally requiring metal wheels or other modifications which slow printers down.

Spinwriter thimbles are available in a wide variety of type fonts, and are priced approximately 30 percent less than daisy wheel elements. Like Spinwriter ribbons, thimble elements are easily accessible, and can be replaced in seconds by operators using one hand.

Spinwriter thimbles are noticeably quieter than either plastic or metal daisy wheels, which means that Spinwriter printers fit well in office environments. A Diablo-compatible interface is available for Spinwriters, making direct replacement easy for original equipment manufacturers (OEMs) and end users.

The thimble is only part of what makes Spinwriters better than today's best character printers. Consider our much longer lasting print hammer assembly: it has fewer moving parts than those on competing printers, and the voice coil actuated print hammer is strengthened with special alloys.

And consider the way highly reliable Spinwriters meet your printer needs: the Spinwriter family includes microprocessor-controlled receive-only and keyboard send/receive models, and basic mechanisms for those wishing to add their own power supply and housings.

Spinwriters feature Mean-Time-Between-Failure rates of better than 2,000 hours, and are serviced by one of the largest, most competent organizations serving the computer industry. Spinwriters are priced approximately 10 percent below competition, and we can deliver in OEM quantities in 60 days or less.

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MC6860 300/600 bps MODEM
MC6862 2400 bps MODULATOR
MC6850 ACIA (Async)
MC6852 SSDA (Sync)
MC6854 ADLC (Sync)
Available 1st half, 1979
MC6851 UCIA (Synch and Async)
Motorola peripherals-doing more
so your processor can do more!
MOTOROLA INTEGRATED CIRCUITS
·SYSTEMS ON SILICON·

communicates...

Cost effective communications capability has been a primary M6800 consideration from the start.

When the M6800 Family's design concept was finalized, one of the features that raised it above the ordinary new microprocessors of the day, that made it unique, was its orientation toward data communications.

The MC6850 Asynchronous Communications Interface Adapter and the MC6852 Synchronous Serial Data Adapter were part of the original M6800 Family. A MODEM, the MC6860, was the first addition to the basic family. Later, the MC6862 2400 bps MODULATOR was added.

Data communications is now, more than ever, one of the special provinces of the M6800 Family. Powerful new family LSI functions keep expanding its capabilities. Functions like the Advanced Data Link Controller, MC6854, which is available now, and the MC6851 Universal Communications Interface Adapter scheduled for availability in the first half of 1979.

Advanced Data Link Controller implements all major bit-oriented protocols - on chip.

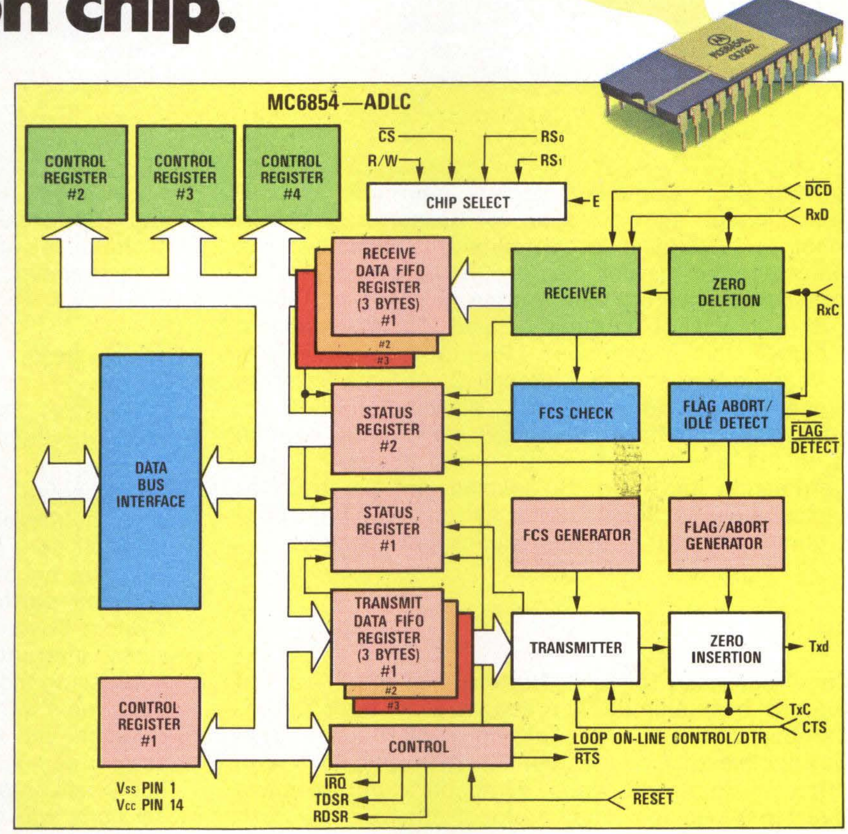
The MC6854 ADLC is Motorola's new 28-pin MPU/data communications link dedicated to doing its bit-sync job better than any 40-pin general purpose device can, and doing it less expensively.

It's available off-the-shelf now for $16.95 (plastic) in 100-up quantities. Because the MC6854 maximizes effectiveness of its specific function, software overhead and associated costs are minimized.

In addition to SDLC, the bit-oriented protocol implemented by most devices, the MC6854 also handles ADCCP and HDLC on chip, without any sacrifice of its complete MODEM controls (RTS, DCD, CTS, DTR), DMA capability, or loopback self-test. The ADLC implements NRZ and NRZI, and also provides complete on-chip loop control. Quad buffers, instead of the usual pair, allow two-byte transfers.

Three speed variations, 1 MHz, 1.5 MHz, and 2.0 MHz, are now available, and the 1.0 MHz MC6854 is offered in your choice of 0 to +70, −40 to +85, or −55 to +125 degrees C.

We have a reference sheet for all of our M6800 Family communications data sheets and wide range of applications notes. For a copy of the MC6854 data sheet, and the reference sheet with request reply card, write to Motorola Semiconductor Group, P.O. Box 20912, Phoenix, AZ 85036, or circle the reader service number.



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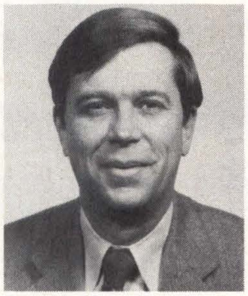
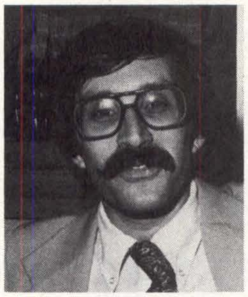
COMPCON Fall 78

September 6-8
Capitol Hilton Hotel, Washington, DC



Kenneth H. Crandall, Jr
General Chairman

Marshall D. Abrams
Program Chairman



David C. Hartmann
Tutorial Chairman

The 17th IEEE Computer Society International Conference under the direction of General Chairman Kenneth H. Crandall, Jr, Satellite Business Systems, McLean, Va will be composed of three preconference tutorials and a variety of program sessions surrounding the theme of computers and communications: interfaces and interactions. Program Chairman for this year's conference is Marshall D. Abrams from the National Bureau of Standards, Washington, DC. On Wednesday, September 6, a 9:30 am plenary session and an 11 am keynote session will focus on both governmental and carrier's policies and perspectives on telecommunications as well as ideas on the evolving computing and communications environment.

Tutorials

Tutorial chairman David C. Hartmann of the Library of Congress has initiated a preconference tutorial program consisting of three sessions all beginning at 9 am on Tuesday, September 5. "A Practical View of Computer Communications Protocols" will examine fundamental design and protocol choices in computer communications systems and discuss existing offerings.

Explaining recent developments in system and program testing techniques, "A Survey of Software Validation Methods" discusses developments including methods for analyzing program structure, techniques for quantifying test coverage and analyzing test results, systematic methodologies for planning and controlling the testing process, and automated tools and software aids for testing.

"Computer Networks: A Tutorial, 1978 Revision and Update" will cover network topology and communications media, network technology and its effect on network performance, resource sharing requirements and techniques, and approaches to network performance measurement, access, and management.

Networks

COMPCON Fall 78 will incorporate several sessions concerned with various aspects of computer networks. Wednesday sessions will cover flow control analysis by touching upon numerical analysis of networks with multilevel flow control, error detection and retransmission, and radio network analysis. One session will give an overview of information retrieval services and will particularly cover the Lockheed dialog, the System Development Corp (SDC), orbit, and BRS services. Internetwork routing and addressing, message addressing modes, and response routing in large computer nets will comprise another session. Other discussions will revolve around the areas of packet bus structures, analyses of network performance, and micronetworks. The paper presentations for these sessions will confront such topics as high bandwidth local computer networks, nodes, the vans system, interface processor for a recirculating data network, and design of a microsubnetwork. Still more sessions concerned with networks will encompass architectures, specifically of a modular network and a distributed data network. Interface standards for public data networks and network control protocols will be covered. Network management, particularly operational control and computer security along with various network operating systems will also be confronted. Final sessions on networks will involve discussions of performance evaluation trends and approaches to network design.

(*Continued on p 80*)

A phone jack.

That's all it takes to connect the Extel R.O. teleprinter to the switched telephone network.

Because we've replaced conventional external interface equipment with an integral modem that includes FCC registered line access circuitry all the way to the telephone line.

This means that with no more external signal hardware than a telephone connecting jack, the Extel R.O. printer can receive a call, answer the call, and send its own answer back (up to 63 characters), all without human intervention—automatically.

And you don't have to deal with several companies to complete the installation. One technician can do it during one call.

Internal integrated DAA/DLC. It's another example of technological leadership by Extel, a pioneer in solid state

teleprinters, expandable dot matrix printing, internal memories, automatic dialing and integral selective calling systems.

Learn more about Extel's complete line of modular, programmable teleprinters. Contact Sales Dept.: Phone (800) 323-5470; Telex 72-4398; TWX 910-686-4782; or use the coupon.

You'll get the best connection in teleprinters.

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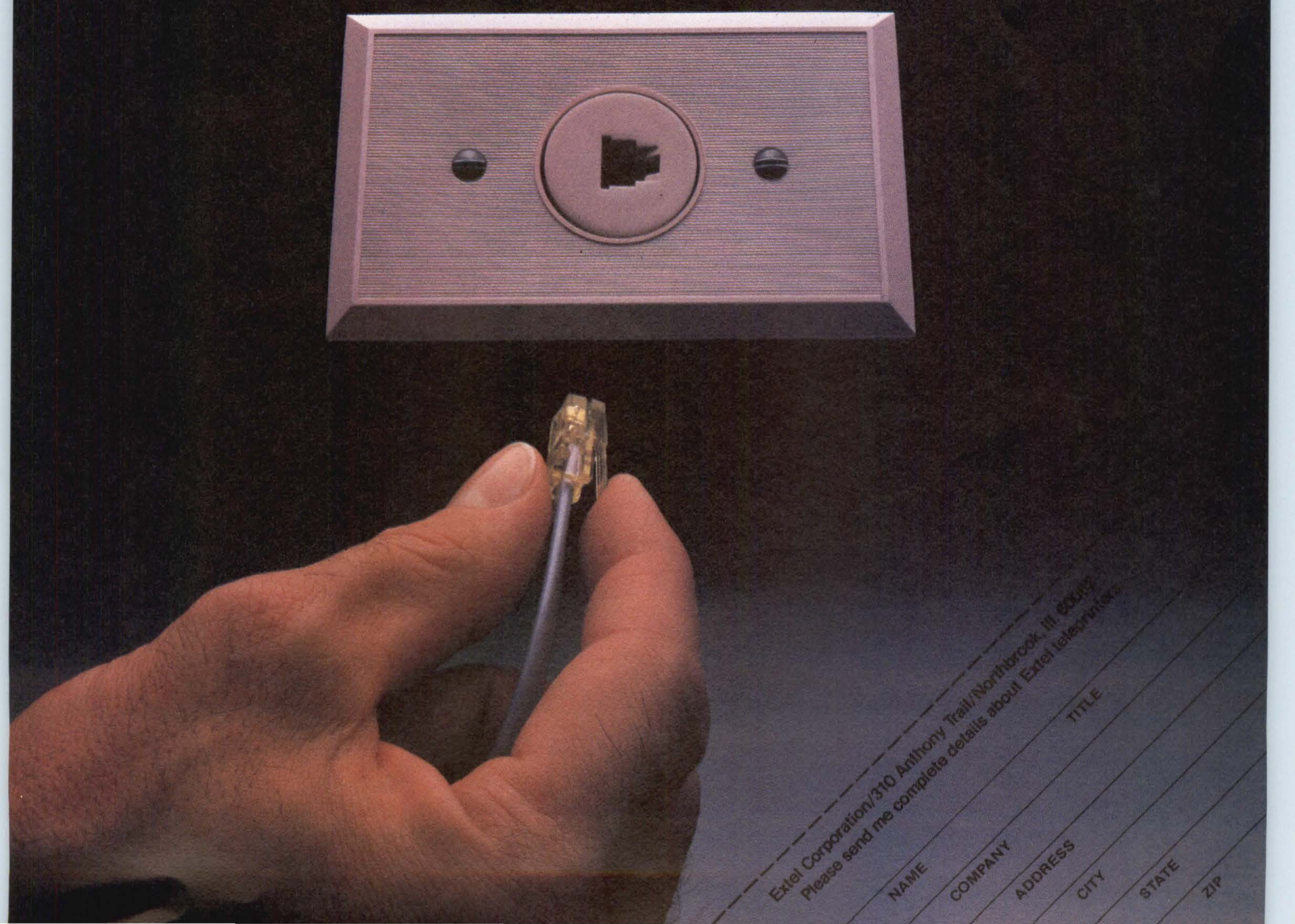
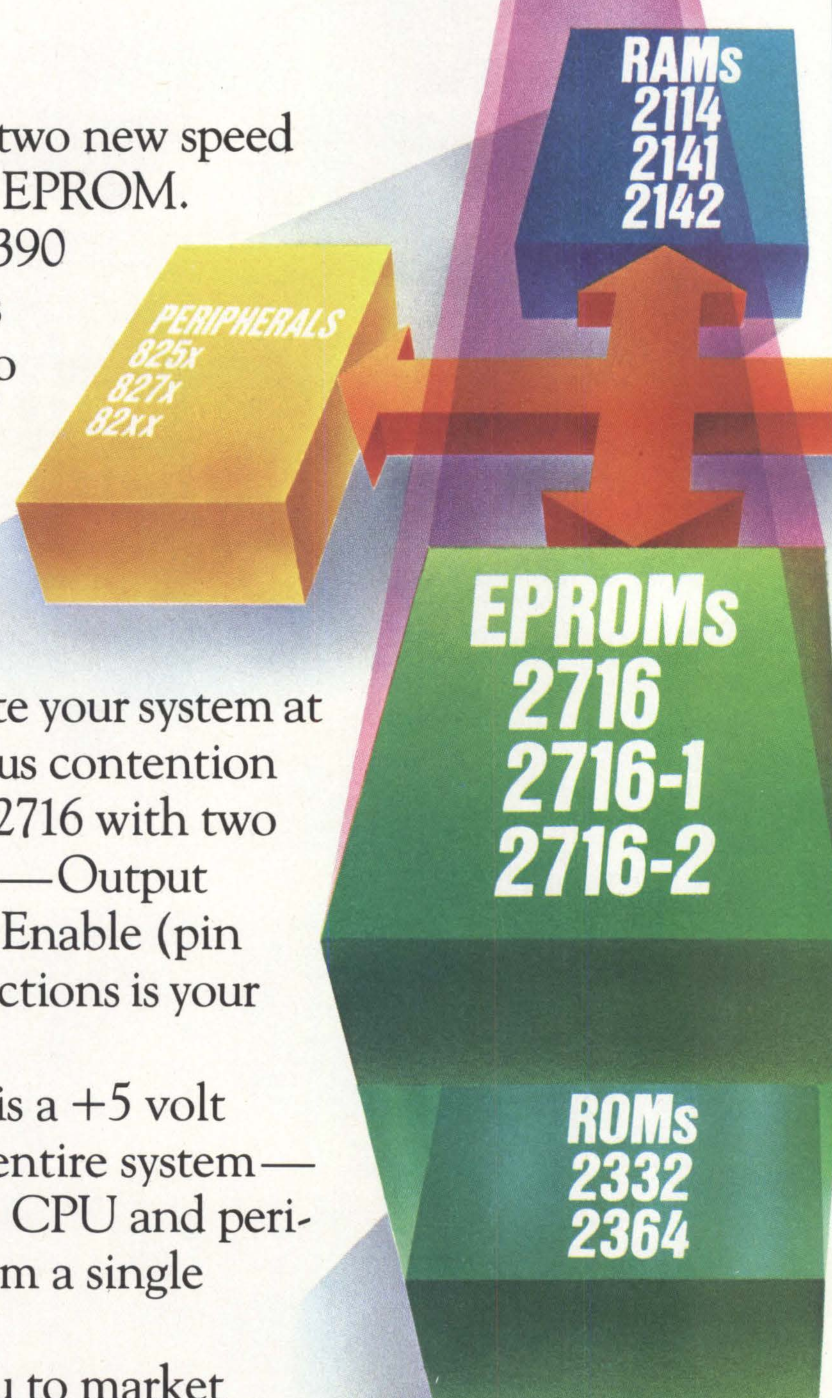
CIRCLE 40 ON INQUIRY CARD

Extel introduces the most advanced hookup system in the teleprinter industry.



Why microcomputer with our 2716



We've just introduced two new speed selections of our 2716 16K EPROM. The 2716-2 access time is 390 nanoseconds, the 2716-1 is just 350 ns—fast enough to take full advantage of the new multiplexed microprocessors, such as the 5MHz 8085A-2 and the HMOS, 16-bit 8086.

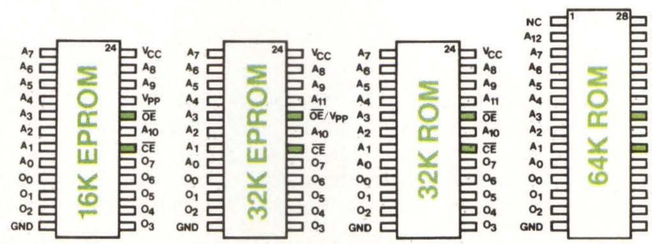
To enable you to operate your system at high clock rates without bus contention problems, we've built the 2716 with two separate control functions—Output Enable (pin 20) and Chip Enable (pin 18). Using both control functions is your key to high performance.

And because the 2716 is a +5 volt part, you can design your entire system—EPROMs, ROMs, RAMs, CPU and peripherals—all operating from a single +5 volt supply.

Using the 2716 gets you to market sooner, too, with fast, easy reprogrammability and no "turnaround time" for

system design starts 16K EPROM.

program changes. Then, when you're ready for volume production, there's the economy and upgrade capability of pin-for-pin interchangeable ROMs— the 2316E (16K), 2332 (32K) and 2364 (64K).



	2716	2332	2364
Organization	2K x 8	4K x 8	8K x 8
Active Icc (max)	100 mA	40 mA	40 mA
Standby Icc (max)	25 mA	15 mA	15 mA
Access Time (max)	350-450 ns	300 ns	300 ns

Just as important, designing with the 2716 today assures you of easy mobility to the higher density memories needed for the system upgrades you'll be implementing tomorrow. Utilizing the 2716's pinout, for example, not only gives you compatibility with our 32K and 64K ROMs, but gives you the design flexibility to move to our 32K EPROM when it's introduced.

Design flexibility is such an important consideration for maximizing your product's life cycle that we've devoted an entire application note to it. For a copy of AP30, with the complete story on the ROM/EPROM upgrade path, along with an updated 2716 data sheet, write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

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US and Canadian distributors: Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty, or L.A. Varah, Zentronics.

CIRCLE 41 ON INQUIRY CARD

Data Communications

Four sessions, two which are panel discussions, will focus on data communications. One panel will explore communications services and systems, user applications, and political problems—all related to international data flow. The second panel will discuss the FCC's impact on industry, market, and regulatory structures. Satellite communications, circuit switching technology, and distributed routing in hybrid packet and circuit data networks will comprise the remaining sessions.

Data Security

On Thursday afternoon panel members will discuss the effect computer networks have on privacy. The efficacy of the data encryption standard (DES) in data processing together with communication standards for using the DES will comprise a session on computer cryptography.

General Technology

Voice memory systems, services, and storage systems, along with issues in digitized voice will be included in Wednesday afternoon sessions. Validation tools will also be discussed. On Thursday, papers concerning standard interfaces and protocols for distributed systems will be presented. Virtual systems will be covered in another session. General sessions on Friday will contain papers on the use of an incomplete gamma function for improving measures of response time and measurement of an X.25 service. Outlooks on hardware to be explored include optimizing microcomputer development systems, minimizing risks in hardware/software partitioning, and random errors in digital systems due to flip-flops. Prospects and theories in information accessing will be dealt with in a Friday afternoon session.

Registration

Advanced registration for COMPCON Fall 78 must be completed before August 26. Tutorial registration fee includes luncheon and bound text. COMPCON fee includes one copy of the Proceedings and two complimentary drink tickets. Advanced registration fees are $60 and $75 (member and nonmember) for attending either one tutorial or COMPCON only. Advanced fees for one tutorial in addition to COMPCON are $120 and $135, respectively. Late registration fees (after the August 26 deadline) show an increase of $10 throughout. During COMPCON week, attendees may register for tutorials on September 5 and for COMPCON on September 6-8. □

CIRCLE 42 ON INQUIRY CARD

CIRCLE 43 ON INQUIRY CARD →

Looking For Price/Performance Balance In Data Acquisition Systems?

Weigh These Facts:

Model	Nonlinearity	Throughput	Internal Amp	Price (100's)
SDM856JG	±0.024%	38kHz	No	$ 99.00
SDM856KG	±0.012%	27kHz	No	$125.00
SDM857JG	±0.024%	38kHz	Yes	$125.00
SDM857KG	±0.012%	27kHz	Yes	$138.00

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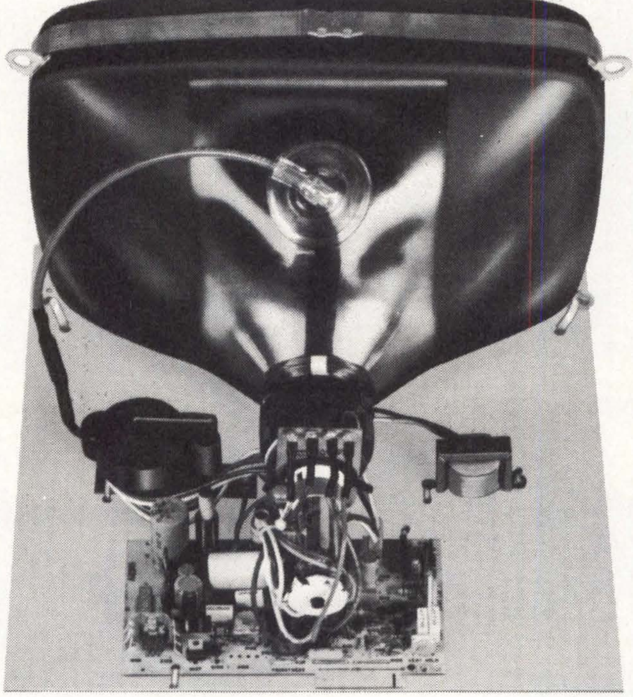

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HARDWARE APPROACHES TO MICROPROGRAMMING WITH BIPOLAR MICROPROCESSORS

Design advantages, limitations, and alternatives of bit-slice and fixed-instruction bipolar microprocessors are explored and compared to aid designers in implementing effective microprogrammable hardware for complex data processing applications

Joseph C. Conway Signetics Corporation, Sunnyvale, California

Design engineers are presently confronted with two important alternative technologies when developing functionally complex devices for use in computer systems, such as central processing units, memory controllers, floppy disc controllers, and high speed fixed- or moving-head disc controllers. The first approach, designing the system using small-scale and medium-scale integration logic elements, results in a device that is highly inflexible to modification. If a design error is discovered or a functional parameter is changed, circuits must be physically added or deleted, and printed circuit boards must be modified. Both result in increased costs and design delays.

The second system design approach, microprogramming with bipolar microprocessors, minimizes supplementary hardware and places functional control in microprogram memory. Additional hardware is limited to the circuits required to supply test-operating parameters for the microprocessor, and to the output circuits that the microprocessor sets and resets for controlling external events. If an operating parameter must be changed, modification will probably be limited to microprogramming without any hardware alteration.

In controller applications where small size and hardware flexibility are primary design factors the advantages of microprogramming are evident. An intelligent microprogrammed controller can carry out complex multiple function operations without host system intervention. A microprocessor also has inherent self-diagnostic ability. With simple built-in test routines, it can test itself and its associated logic, and pinpoint faulty memory locations and internal registers. Maintenance and repair times are minimal and data integrity improves because the processor can be programmed to verify its own ability to function. Because fewer components are required, the system design realizes increased reliability and overall cost effectiveness, with considerable savings in circuit board size and assembly costs.

Bipolar Microprocessors

Two basic types of bipolar microprocessor architecture—bit slice and fixed instruction—can be organized as a computer, or can be used to control external input/output (I/O) devices. Each configuration has self-contained control, processing, and source/destination logic. In addition, each configuration receives operational commands from microinstruction memory, called a "control store." This memory controls the functional characteristics of the microprocessor—in other words, its individuality. For the microprocessor to perform complex functions,

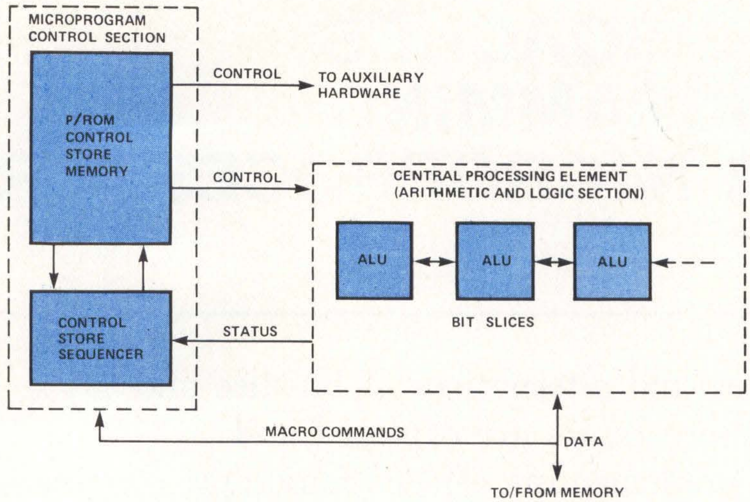

Fig 1 Bit-slice microprocessor. Architecture is organized in two major sections: microprogram control and central processing element (CPE). Since bit slices are only 2 to 4 bits wide, they are organized to allow cascading to wider words. Slices pass status to microsequencer for use in determining order of microinstruction execution

strings of microcommands are executed sequentially at rates of more than 4M instructions/s.

Bit-slice and fixed-instruction microprocessors differ in that a fixed-instruction microprocessor has fixed-format instructions and is completely self-contained. Bit slices are only a portion of the arithmetic and register section of a microprocessor and require a control store sequencer to address the microprogram. In these devices the microword is not fixed as in a fixed-instruction microprocessor; each field can be separately assigned to control the slices, I/O, microsequencer, and any other required logic to complete the design.

Microprocessors are often used to execute exactly (emulate) the instruction set of a standard minicomputer. This is accomplished by organizing the microprocessor so that memory addressing, system control, data I/O buses, and bus control signals match those of the central processing unit (CPU) being emulated. However, internal operation of the emulator can be organized so that an efficient string of microinstructions will accomplish each required CPU instruction. As each instruction is received, it is decoded by the microprocessor, which executes a specific string of microinstructions to accomplish the required function.

Extra capability may be added to the emulator by defining an expanded instruction set. Commands, such as multiply, divide, and binary-coded decimal (BCD) add, can be accomplished within microcode while retaining downward compatibility with the original instruction set for execution of existing systems software.

Bit-Slice Architecture

Bit-slice microprocessors come in 2- and 4-bit wide versions and contain a register stack, an arithmetic logic unit (ALU), shift logic, and data bus drivers (Fig 1). These circuits are organized as modular building blocks and can be linked together to form a microprocessor that meets design objectives efficiently. Although bit slices are functionally complex, no provisions are inherently available to address a control memory or to determine the order of microprogram execution. To accomplish these functions in a bit-slice design, a microsequencer is used to delegate the order in which microinstructions are executed and to control all decisions the microprocessor makes on incoming information.

From an external source, a series of related microinstructions, or macrocommands, and data are routed to the microsequencer and bit slices, respectively. The microsequencer decodes the command and executes a string of microinstructions from control store memory. These microinstructions determine what functions the bit slices will perform on the data and what type of decision the microsequencer will make to determine the next microinstruction address. This address may be dependent on status information from the bit slices, from external hardware, or from the program stack within the microsequencer. Basically, bit slices perform all arithmetic operations, and the microsequencer makes all decisions and sets the order of microprogram execution.

The complete design of a bit-slice microprocessor entails considerably more than connecting a microsequencer to some bit slices and adding programmable read-only memory (P/ROM) to control them. Other support circuitry also must be managed from the microprogram. In addition to the microword bits required for the central processing element (CPE) bit slices and microsequencer, other bits are necessary for dedicated functions, such as bus control, test input selection for branching, and write enables for registers or random-access memories (RAMs). In other words, extra microword bits must be assigned to control the auxiliary circuitry around the bit slices. Since the bit-slice design is totally modular in nature, the designer can tailor the power and function of the microinstructions to best support the design requirements.

Fixed-Instruction Architecture

The fixed-instruction bipolar microprocessor (Fig 2) is based on an entirely different organization than the bit

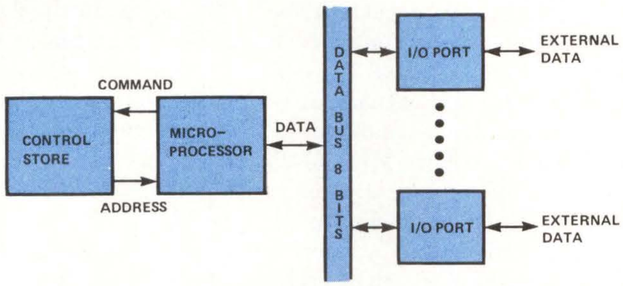

Fig 2 Fixed-instruction microprocessor. Architecture is organized with three separate buses, each dedicated to particular task. Address (ADR) bus is used to address control store and is 13 bits wide (8192-word addressability). Command (CMD) bus is 16 bits wide and carries fixed-instruction commands to microprocessor. All data to and from processor are carried on bidirectional data bus. I/O ports interface this bus to external data sources

slice. The instruction set is predetermined, and microword functions and fields are preassigned, unlike the bit slice which allows use of a customized microword. This microprocessor also contains a program counter and does not require an external bipolar microsequencer. The data bus has a fixed width (eight bits), and control signals have fixed organization and timing. Almost everything necessary for a complete microprocessor is self-contained, including a system clock/oscillator circuit that needs only an external crystal. With the addition of control store

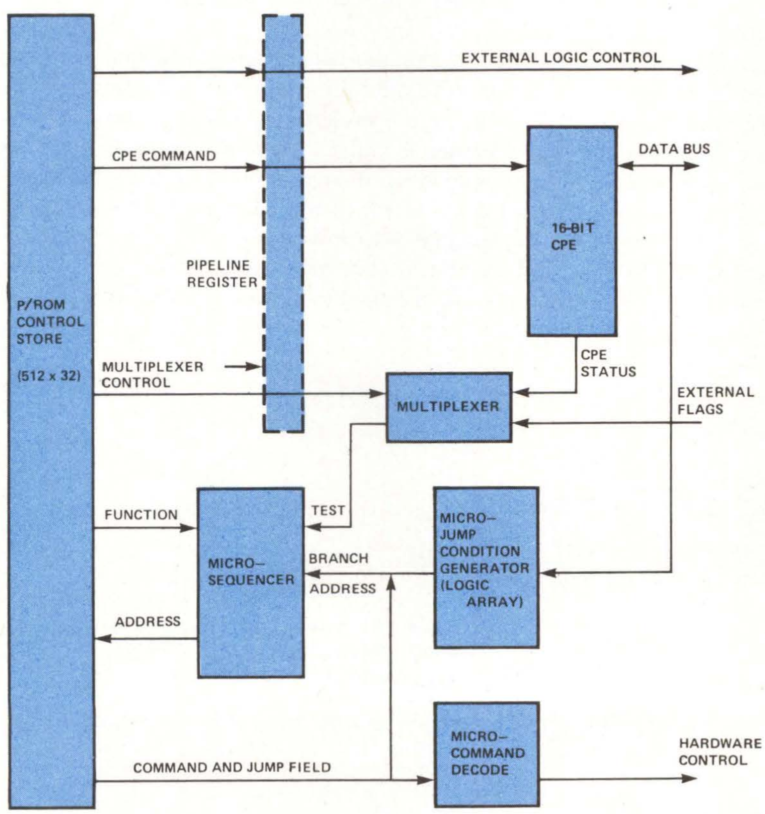

Fig 3 General-purpose bit-slice processor. Microprogram control and CPE are entirely separate, with microsequencer controlling microprogram next address and bit-slices performing ALU functions. By adding a pipeline register (dotted lines), operating speed can be increased by allowing new instruction to be fetched as previous one is being executed in CPE

memory (ROM-P/ROM) and some I/O interface circuitry, the fixed-instruction bipolar microprocessor becomes a complete computer system.

All data going to or from the microprocessor are transferred via the bidirectional 8-bit data bus. The microprocessor receives data, performs an arithmetic or logic operation, and places processed data in an internal register or routes it to an I/O port on the data bus. Microinstructions are fixed at 16 bits (2 bytes) wide, and a microinstruction address is generated entirely within the microprocessor.

Bit-Slice Application

Bit-slice microprocessors are well suited for general-purpose data processing applications. A simplified block diagram of a CPU organized with bit slices and a microsequencer is given in Fig 3. Purpose of the microprogrammed CPU is to perform macro-level instructions required by a minicomputer by executing a definitive series of microinstructions. An example of a macrocommand (complex instruction) would be a multiply instruction that requires a string of shifts and adds. This is accomplished in microcode by setting up a string of microinstructions (microprocessor one-cycle instructions), each of which does part of the macrocommand. As an example, the first micro shifts, the second adds, the third decrements a register and checks for zero, etc, until the macrocommand is complete.

In this CPU design, the sequence in which microinstructions are executed is controlled by the microsequencer, and arithmetic and logic functions performed on the data are accomplished in the CPE (bit slices). Functional parameters of the design are contained in the microword, which simultaneously commands the CPE, controls all sources and destinations of data buses, and selects the type of operation the microsequencer will perform. The microword also steers the proper external flag information into the microsequencer for use in conditional branching, test and skip, interrupt handling, and subroutine operations.

A control word for this application might have the field assignments shown in Fig 4, with each group of bits individually controlling a function that the microprocessor performs. Since a bit-slice design uses this type of microword organization, the microprocessor can have as many different commands as the total number of combinations of bits in the microword. In addition, the structure of the microprocessor can be altered by the organization of microword fields, allowing the design to closely match the function it must perform. This functional control is the greatest asset of a bit-slice design. Separate control of each distinct part of the microprocessor by the microword allows the design to be directly adaptable to system requirements. Microwords are often very wide—40 to 64 bits of code are common—with each bit dedicated to a particular task. By using a bit or group of bits to directly control a function (ie, bus steering), overlapping of operation can be achieved by allowing different sections of the microprocessor to simultaneously perform small tasks. Depending on the organization and assignment of the microword, the following three items could be accomplished in one microcycle (less than 200 ns): an arithmetic or register instruction in the CPE, a command to external hardware, and the testing of an external parameter with the microsequencer.

To obtain the fastest cycle times possible, a pipelined architecture can be used. Addition of a pipeline register between control store memory and CPE, as shown by the dotted lines in Fig 3, allows the microsequencer to address the next microinstruction while the previous one is being executed by the CPE. Pipelining refers to the multifunction effect that the pipeline register has on the sequence of microinstructions. In a microprocessor without a pipeline register, each instruction must be completed before a new instruction can be started. The microsequencer must address control store and control store outputs must become stable before the CPE can execute its function and the microsequencer can operate on the results of the CPE operation. In other words, the CPE, control store, and microsequencer are in series, each contributing to the cycle time of the machine. When a pipeline register is added, a new microinstruction is retrieved from control store memory as the one previously retrieved is being executed. In this manner, the microprocessor acts as a pipeline with instructions starting in one microcycle and ending in the next. This effectively eliminates the microstore access time from the microcycle, allowing a

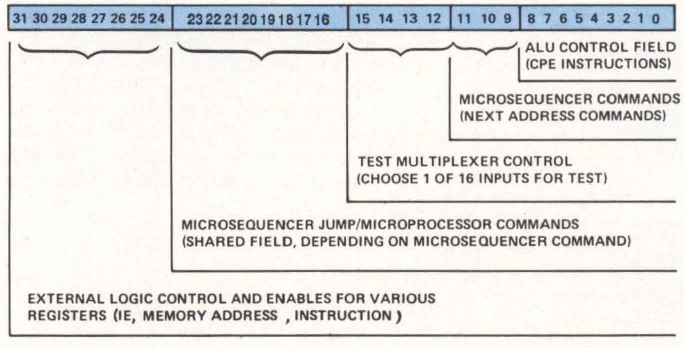

Fig 4 Microword for bit-slice processor. Each group of bits has definite purpose and controls separate part of microprocessor. Independent command fields allow each section to operate independently, making microprocessor highly flexible

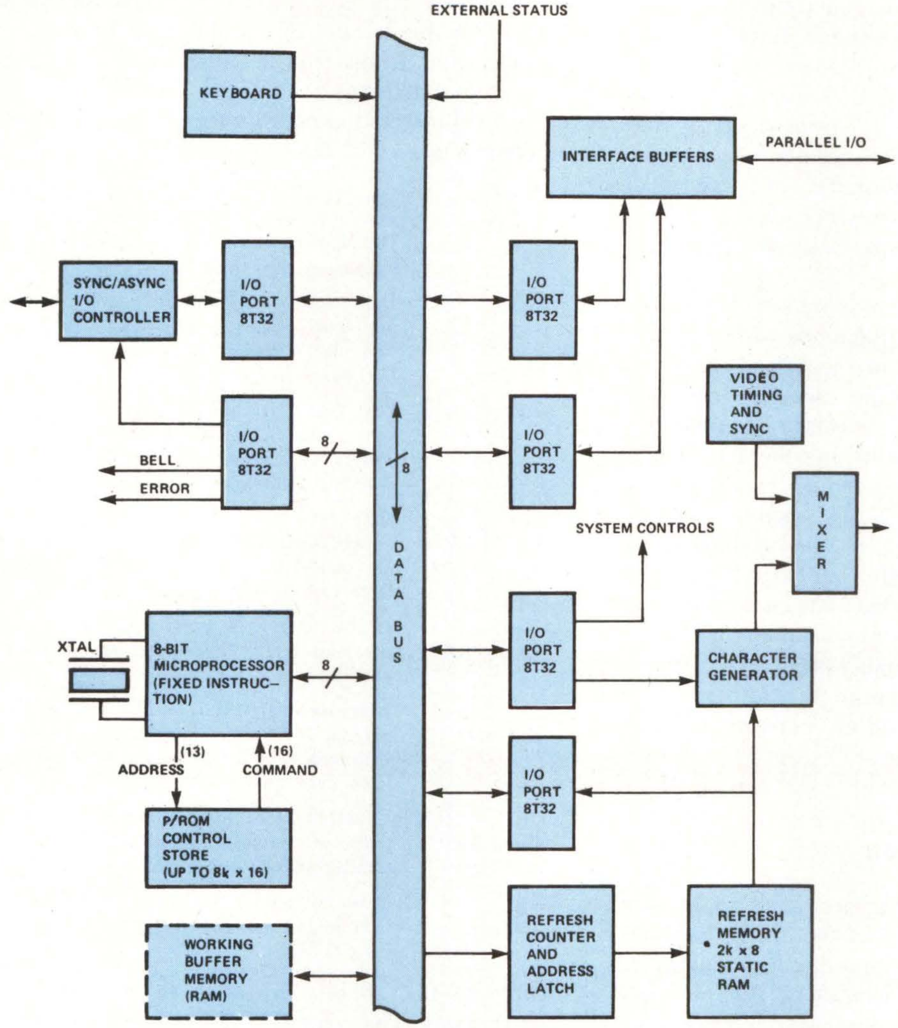

Fig 5 CRT controller. System illustrates single data bus and separate microprogram address and command buses of fixed instruction bipolar microprocessor. Data from any source on bus or internal microprocessor register can have an arithmetic operation performed on them and can be returned to same or different destination, all within one 250-ns instruction cycle

faster overall throughput. Pipelining, however, will actually waste a microcycle when a conditional branch in the program is required. The next instruction automatically fetched by the microcontroller must be abandoned and a new instruction fetched, requiring an extra microcycle.

Fixed-Instruction Application

A microprogrammed cathode-ray tube (CRT) display terminal (block diagram, Fig 5) contains a synchronous/asynchronous interface for connection to a modem or host computer through an RS-232-C interface. The interface also supports a keyboard and a bidirectional, parallel, high speed data port. Refresh memory and cursor control logic are directly controlled by a fixed-instruction bipolar microprocessor. The complete programmability of this design approach allows an intelligent terminal to be customized to almost any specialized application by simply changing the microcode.

Within the CRT display controller, the 8-bit microprocessor receives data from all sources and redistributes it via a single 8-bit bidirectional data bus. For each 250-ns instruction cycle (4M cycles/s), data can be retrieved from a source on the bus, a logic or arithmetic operation can be performed by the microprocessor, and the result can be placed in an internal register or returned to the same or different port on the data bus. The design is simplified by the 8-bit microprocessor's separate instruction and data buses. The P/ROM control store is individually addressed by the microprocessor, and 16-bit instructions are received via the command (CMD) bus, allowing the data bus to be dedicated completely to carrying data and status required to fully control the operations of the display terminal.

The extremely fast cycle time and full 8-bit architecture make possible the data processing or formatting functions required for complex operations of an intelligent terminal, including data manipulation and I/O protocols. In turn, realtime processing of incoming or outgoing data can occur while the microprocessor continues to perform basic housekeeping required for the display and I/O.

Since the fixed-instruction bipolar microprocessor can directly address 8192 words of program memory and since many programs require significantly less storage (1k to 4k typically), additional memory can be added to the design and addressed by the microprocessor without using extra hardware. This allows program expansion without hardware modification.

External hardware required for a basic system is minimal because the ALU and register file along with program counters and sequencing logic are contained within a single integrated circuit. The design uses only one data bus, which is expandable. Extra interface requirements can be incorporated by simply attaching more I/O ports to the bus since the microprocessor can address up to 512 ports. Furthermore, a working buffer memory (RAM) can be added to allow expansion of microprocessor capabilities. This buffer can be used as an extra scratchpad register for programs or for extra data storage. Since fixed-instruction microprocessors are modular in nature, a designer can begin with a small system and add capability later. The result is a design that can grow to meet future needs, thereby avoiding imposed obsolescence by new system requirements.

Microprocessor Selection

To choose the microprocessor that best suits application requirements, the designer first must thoroughly evaluate functional parameters, operating speed, cost, and future expandability. Second, the system must be programmed, and design bugs resolved. The microprogramming stage of design will require development aids such as writable control store, microprogram compilers, and perhaps a microprocessor emulator. Prototyping kits may also be employed as learning aids to gain a comfortable level of understanding before the actual development project is undertaken.

Although there are many parameters to be considered, the different organizations of the bit-slice and fixed-instruction types of microprocessor make certain choices more suitable for particular applications than others. Each type has an unique organization and can effectively fulfill a variety of specialized applications.

The 8X300 single-chip, fixed-instruction microprocessor (Fig 6), with completely self-contained program sequencing and microstore addressing, lends itself to low cost microprocessor based systems for medium to high speed control and data handling applications. The 8-bit wide, single bus architecture is ideal for situations where bytes of data must be processed and redistributed to other parts of the system.

Using entirely separate instruction and data buses, this microprocessor includes full instruction decoding, which interprets each instruction; decides the type of arithmetic or logic operation to be performed; and controls the source, destination, and number of bits to be operated on. Organization of the data paths and ALU allows the microprocessor to bring in data from the data bus, rotate, mask, perform an ALU operation, and place it in an internal register; or shift, merge, and place it back on the data bus in one 250-ns instruction cycle. Data source for the A input of the ALU is an internal auxiliary register; the B input can be either an internal register or the external data bus.

A fixed-instruction microprocessor performs the following eight classes of instructions.

MOVE	Data from data bus or internal register can be moved to data bus or another internal register. Data can be shifted any number of places and/or masked to any length.
ADD	Data from data bus or internal register are added to contents of internal auxiliary register and placed either in internal register or on data bus. Data may be shifted and/or masked.
AND	Data from data bus or internal register are ANDed with contents of internal auxiliary register, and results are placed on data bus or into internal register. Data may be shifted and/or masked.
XOR (Exclusive-OR)	Data from data bus or internal register are exclusive-ORed with auxiliary register and results are placed on data bus or into internal register. Data can be shifted and/or masked.
XMIT (Transmit)	Literal data field (part of instruction word) replaces data in internal register or is output on data bus.
XEC (Execute)	Executes instruction at address formed by replacing least significant bits of program address with sum of a literal field in instruction and data from data bus.
NZT (Non-Zero Transfer)	Literal field of instruction replaces current contents of program counter if selected internal register or data bus is non-zero.
JMP (Jump)	Program counter contents are replaced by a literal field in the instruction (unconditional jump from 0 to 17777_8).

Three of the 16 bits are used to choose the class of instructions. The other 13 bits are used for source, destination, and number of bits to be operated on or, in the case of an unconditional jump, become the address of the next microinstruction. The microprocessor is organized to handle bit-through-byte manipulation efficiently, making it ideal for high speed controller applications.

Bit-slice microprocessors, on the other hand, are best suited for central processing applications and for high speed peripheral controllers such as fixed-head disc control. Of the two types of bit slices described—3002 and 2901-1—the 3002 2-bit-slice microprocessor has the most effective organization for controllers because of its multiple data and memory input buses and self-contained memory address register (Fig 7). Both types fulfill requirements for CPE applications with certain individual advantages.

The 3002 has the fastest cycle time, a multiple bus architecture, and a built-in memory address register. The 2901-1 (Fig 8) has the advantage of being 4-bits wide instead of 2-bits wide, and is organized around a 16 x 4-bit, 2-port RAM. This 2-port scheme is effective for execution of complex arithmetic operations, making it an effective building block for central processing.

The 3002 2-bit wide bit-slice microprocessor (Fig 7) contains three separate data input buses, an accumulator

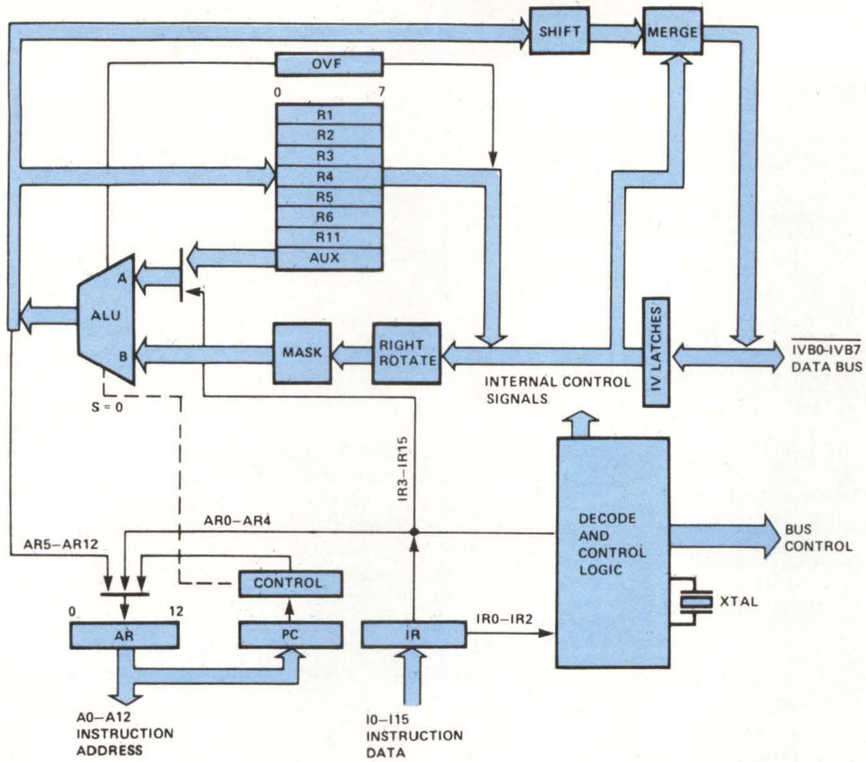

Fig 6 8X300 architecture. Microprocessor is organized to allow data from external source to be fetched, operated on by ALU, and passed back to data bus or deposited internally, all within one processor cycle (250 ns). Additionally, microprogram address register (AR) is used to address control memory, and 16-bit instruction data bus (IØ-I15) provides commands

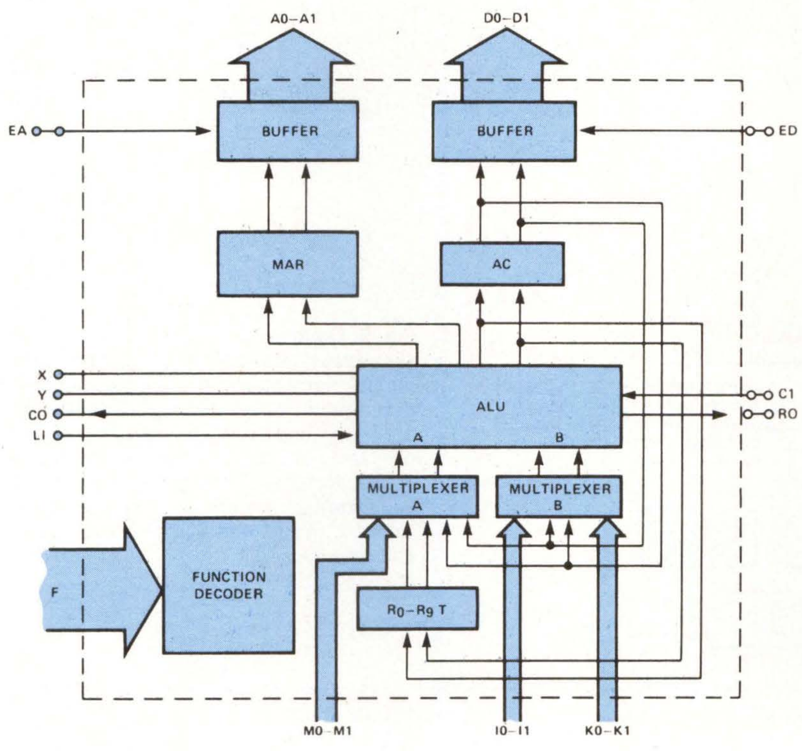

Fig 7 3002 2-bit-slice microprocessor. Bit slice has three separate data paths into ALU and two separate output paths. Additionally, there are 11 internal registers, and accumulator-shift in (LI), shift out (RO), carry in (CI), and carry out (CO) which are provided to allow cascading. Built-in memory address register (MAR) provides inherent buffer storage capabilities by simply connecting RAM addressing to A0 and A1 outputs and RAM data to two M inputs

(AC) on the output of the ALU, and 11 internal registers. A and B multiplexers (MUX) are separately controlled by the microword, allowing data from two different sources to be routed to the ALU at the same time. Also, the two K inputs (K0-K1) allow masking of multiplexer B data (also simultaneously). The 3002's built-in memory address register (MAR), which can be loaded and incremented via the microword, offers additional capability. Extra working registers or data storage can be implemented by simply connecting external RAM between A0 and A1 outputs for addressing, and M0 and M1 inputs for data.

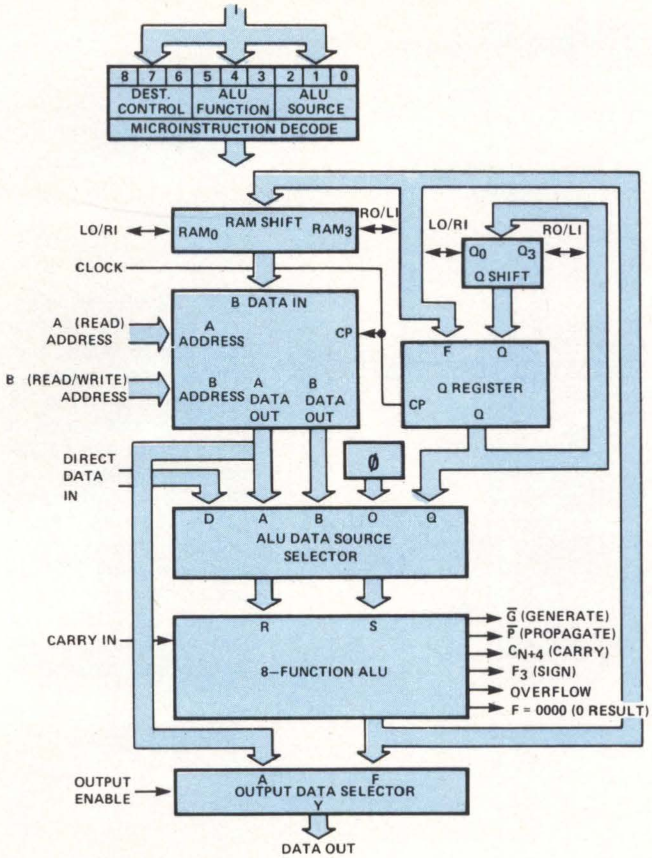

Fig 8 2901-1 microprocessor. This bit-slice microprocessor is organized around 16 x 4 dual-port register. Data from dual-port register file, external data, logic 0, or Q register data can be operated on with 8-function ALU. Subsequently, data can be shifted and stored back in register file and are available via Data Out bus. Each command is broken into three separate fields as defined: ALU source, destination control, and ALU function

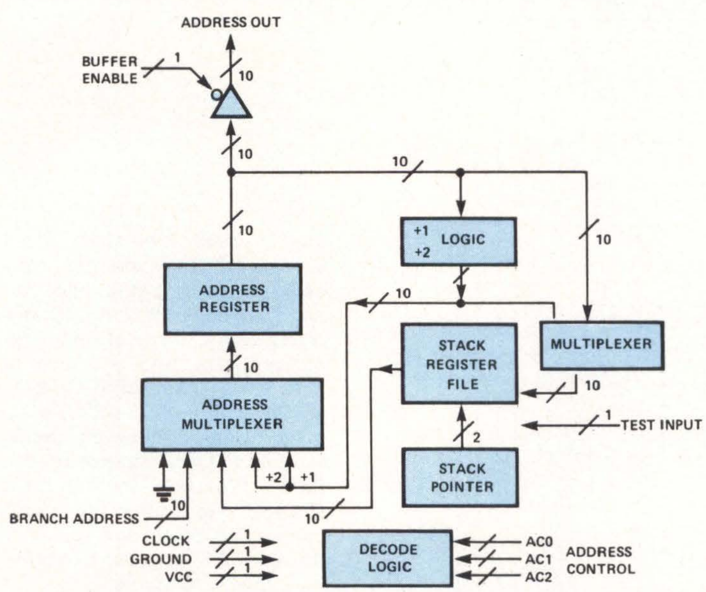

Fig 9 Control store sequencer. Microsequencer contains all necessary elements for microprogram control. It directly addresses 1024 words of microprogram and contains 4-level (LIFO) program stack for subroutining purposes. Next microprogram address can be external branch address, program stack, current address +1 or +2, or all-zeros (reset)

A 4-bit wide microprocessor CPE slice, the 2901-1 is organized around a 16 x 4 dual-port RAM and an 8-function ALU. The microword is divided into three separate control fields: ALU source, ALU function, and destination control. A Q shifter and Q register are included to allow left/right shifting independent of the ALU, which allows add and shift operations to be accomplished in one microcycle. The ALU has four output status flags available: F = Ø, overflow, F3 (sign), and CN + 4 (ripple carry). It also has an output data selector that allows output directly from internal RAM or ALU.

Each bit slice has definite performance advantages; however, a bit-slice CPE does not have the ability to control its own microprogram. This must be done by a microsequencer, whose function is to control the order in which microcommands will be executed. A typical microsequencer, or control store sequencer (Fig 9), contains all logic necessary to address control store memory;

Next Address Control Function Summary

Mnemonic	Description	Function AC_{2-0}	Test	Next Address	Stack	Stack Pointer
TSK	Test and skip	000	False True	Current +1 Current +2	No change No change	No change No change
INC	Increment	001	X	Current +1	No change	No change
BLT	Branch to loop if test input true	010	False True	Current +1 Stack register file	POP POP (read)	Decrement Decrement
POP	POP Stack	011	X	Stack register file	POP (read)	Decrement
BSR	Branch to subroutine if test input true	100	False True	Current +1 Branch address	No change PUSH (curr +1)	No change Increment
PLP	PUSH for looping	101	X	Current +1	PUSH (current address)	Increment
BRT	Branch if test input true	110	False True	Current +1 Branch address	No change No change	No change No change
RST	Set microprogram address output to zero	111	X	All 0s	No change	No change

manage a program stack for use in subroutining or looping; and conditionally increment, skip, or branch to a new microprogram address. It also contains a 10-bit address register, which is used to address a control store memory; and is loadable from an external source, internal 4-level stack, or increment +1 or +2 logic. Control of the next address multiplexer is independent of the type of instruction executed and the state of the external test input.

This microsequencer executes the commands listed in the Next Address Control Function Summary. The TSK and BRT instructions allow instruction skipping and conditional branching, respectively, according to the polarity of the test input. Two other instructions, PLP and BLT, are used to set up a program loop and conditionally return to it, respectively, allowing conditional looping within a microprogram dependent on external test parameters. Mnemonics BSR and POP are used to establish a branch to subroutine and return to the original program address +1, respectively. Finally, RST is used to unconditionally return to all Øs in the address register (reset program address), and INC is used to simply advance the program counter to fetch the next instruction.

Some types of bit-slice microsequencers are 4-bits wide and are cascadable to form longer word lengths. There are also 10-bit (or wider) single chip sequencers. These microsequencer circuits vary in architecture, speed, function, and ease of use from one manufacturer to another, but the primary function of microprogram control remains the same. Choosing a microsequencer basically requires as much consideration as the choice of CPE circuits. The designer must weigh the different characteristics—simplicity of the instruction set and its usefulness (power), number of control bits required for operation, and number of parts needed to address the required control storage to support the design.

Summary

Fixed-instruction and bit-slice bipolar microprocessors each have distinct advantages. The fixed-instruction bipolar microprocessor (8X300) is easy to use, is almost completely self-contained, and is efficient for bit manipulation in medium to high speed control applications. The 3002 and 2901-1 bit slices are more powerful for high speed controller and CPE applications requiring a large amount of arithmetic capability, or any design needing tailored microprocessor functions. A microprocessor designer must fully understand these differences to effectively choose the bipolar microprocessor approach that best fulfills specific requirements.

Although the effort necessary to develop an effective microprogrammed design approach initially seems significant, the benefits far outweigh the investment. After microprogramming techniques are developed, new applications become much easier to accomplish. Although a designer may have to learn a new method of structuring logic functions, once mastered, a powerful design tool can be applied to solving complex data processing or control systems.

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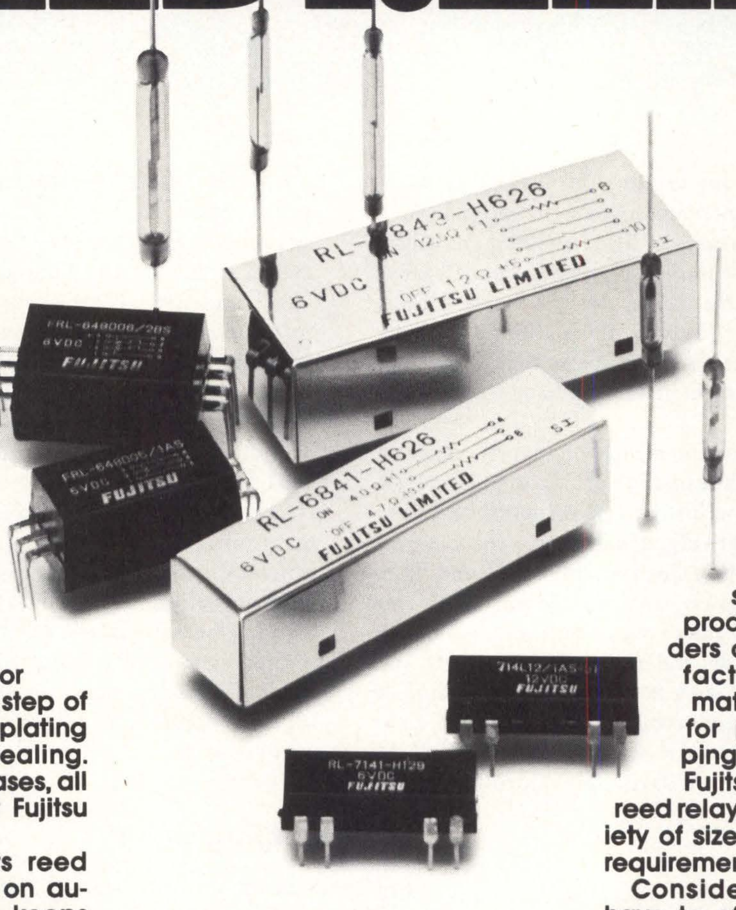

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AND CAPACITORS AND CONNECTORS AN

PREDICTING QUEUE PERFORMANCE ON A PROGRAMMABLE HANDHELD CALCULATOR

Coded for a portable reprogrammable calculator, a multiserver queuing model estimates CPU, channel, and peripheral utilizations, and determines queue sizes and response times for rapid and accurate data processing analyses. Attaching a hardcopy printer results in a complete interactive and convenient queuing investigative system

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Queues are waiting lines encountered in almost all data processing disciplines. Whenever several requestors compete for the service of a limited resource, queues form. Some diverse fields to which queuing theory can be applied include product line assemblies, hospital admissions, aircraft arrivals and departures, computer timesharing, communication networks, and processor job scheduling. The number of queues, and all too frequently the lengths of the queues themselves, evolve rapidly.

By recording the presented program code on two small magnetic cards, designers can turn the Texas Instruments' TI-59[1] calculator into a highly accurate and economical queuing analysis design tool. The calculator is handheld and interactive, essential features for engineers needing quick and effective evaluations of alternative computer configurations. Designers can solve queuing problems, isolate congestion bottlenecks, and iterate solutions for immediate and optimum decisions. Even more computing power develops when the companion PC-100A thermal printer is attached to the calculator, resulting in a completely interactive self-contained device that rivals a data entry terminal tied to a large timesharing computer in terms of performance, and exceeds it in terms of convenience.

Queuing Model

A simple 3-part shorthand notation—arrival distribution/service distribution/number of servers—has been adopted in technical literature for classifying the large number of different types of queuing situations that exist. Letters are used in the three fields to indicate either the type of distribution or the number of servers.

- M = exponential interarrival or service times
- GI = general (arbitrary) independent interarrival
- G = general (arbitrary) service time
- D = constant (deterministic) interarrival or service times
- E_k = Erlang-k interarrivals or service times
- m = number of servers

Typically, queue specifications are written as M/G/1, M/M/m, GI/M/m, M/D/m, GI/G/1, and so forth. To completely define the queue, the other parameters that also must be considered are queue discipline (first in, first out; last in, first out; or random), maximum number of queue waiting positions, and the number of items that can reside in the system.

To obtain the Multiserver Queuing Equations that could be programmed to fit within the 960-step capacity

Multiserver Queuing Equations

Input Parameters

Average arrival rate	λ
Average service rate	u
Number of servers	s

Performance Attributes

Facility utilization: $U = \lambda/us$

Probability of finding no—or zero—items* in the system:

$$P(0) = 1/((\sum_{N=0}^{s-1} (\lambda/u)^N/N!) + (\lambda/u)^s/(s!(1-U)))$$

Probability of finding N items* in the system:

$$P(N) = P(0)(\lambda/u)^N(1/N!) \quad , N < s$$

$$P(N) = P(0)(\lambda/u)^N(1/(s!s^{N-s})) \quad , N \geq s$$

Probability of finding all servers busy and having to wait on the queue (ie, that $\geq$ s items are in the system):

$$B = \sum_{N=s}^{\infty} P(N) = (\lambda/u)^s P(0)/(s!(1-U))$$

Average waiting time in the queue:

$$TW = B/(su(1-U))$$

Average system response time (ie, total time that an item spends in the system):

$$TR = TW + 1/u$$

Standard deviation of system response time:

$$SDTR = \sqrt{B(2-B) + s^2(1-U)^2} \quad TW/B$$

Probability of waiting time in the queue exceeding T:

$$P(TW>T) = Be^{-su(1-U)T}$$

Probability of response time exceeding T:

$$P(TR>T) = e^{-uT}(1+(B/s))((1-e^{-usT(1-U-(1/s))})/(1-U-(1/s)))$$

Average number of items in the queue:

$$Q = \lambda(TW)$$

Average number of items in the system:

$$N = \lambda(TR)$$

*Items in the system either reside in the queue or are being processed by one of the servers.

of the TI-59 calculator, assumptions have been made that there is a first in, first out (FIFO) queue discipline and that both the arrival of inputs and the service times are completely random. Fortunately, such randomness is frequently encountered in the real world and, in any event, always results in a conservative worst-case analysis. Mathematically, this is the classic M/M/m queue which, because of its memoryless Markov property, reduces the complexity of the queuing formulas. The model assumes an infinite queue capacity where items wait until they are serviced; there is no limitation to the number of possible items residing in the system. Although FIFO processing is assumed, preemptive priority queue disciplines can be modeled via techniques previously discussed.[2]

Designers with TI-59 calculators* can run the multiserver queuing model merely by referencing the user instructions in Tables 1 or 2 and the Program for Multiserver Queuing Model listing; further knowledge of either queuing theory or programming is not required.

All TI calculators use the same Algebraic Operating System (AOS**) hierarchy, and all HP calculators use reverse-Polish notation (RPN). Therefore, by eliminating printing of prompting messages and labeling of results and by breaking up the model's programming into independent parts that can fit into calculators with less memory capacity, the queuing model can be made to run on such calculators as the TI-57, TI-58, HP-19, HP-25, HP-29, and Sharp PC-1201. If each equation in the listing is coded and executed separately, the model can be made to fit into calculators with even fewer steps and registers. The applicable owner's manual should be consulted for specific programming details.

Calculator Programming Procedure

Partition TI-59 calculator memory into 720 instruction steps (numbered 000 through 719) and 30 data registers (numbered 00 through 29) by keying in "3 Op 17"; the "3" instructs the calculator to reserve 30 data registers. Then, reset (RST) the instruction address pointer to address 000, press the learn key (LRN), and begin entering the keystrokes for the Multiserver Queuing Model Program (see Listing). Press the Label (Lbl) key, and the instruction address count advances from 000 to 001; press X (multiplication) and the count goes to 002; continue with STO, 8, and so on. Any keystroke errors made during entry can be corrected with the calculator edit keys: single step (SST), backstep (BST), delete (Del), and insert (Ins). The leftmost column of the Program Listing gives the address of the first keystroke on its respective line and is provided to help make certain that entries are placed at their correct addresses; for example, Lbl is found at address 000, RCL at address 022, and If flg at address 040.

After the entire program listing is input, the display will read "712 00," indicating that the next instruction will be placed at address 712. Since the program has already been completely entered, LRN is pressed to get out of learn mode.

Data registers 10 through 29 need to be loaded with the numeric representations of the alphanumeric symbols to be printed on the PC-100A for prompting messages and headings. Store (STO) the integer number 3041273724 in data register 10, the number 3617354217 in register 11, . . . 1617270000 in register 16, etc. The 10 digits stored in each register represent 5 symbols. For example, dissecting the number 3617354217: 36 = S, 17 = E, 35 = R, 42 = V, and 17 = E. The program will print the letters "SERVE."

Next, make a final validation check of the program listing by resetting (RST) the program counter to address 000 and printing a listing (List) of the instructions

*Designers who have SR-52 calculators should consult Ref 2 for an applicable model. Those with Hewlett-Packard HP-67 and HP-97 programmable calculators can request copies of translations coded by B. Treppa from *Computer Design* (see "Letters to the Editor," Feb 1978, p 11), or those coded by H. Gowen from the Hewlett-Packard Users' Library, 1000 NE Circle Blvd, Corvallis, OR 97330.

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TABLE 1

Instructions for Multiserver Queuing Program Using TI-59 Without PC-100A Printer

Step	Procedure	Enter	Press	Display
0	Load two program cards			
1		λ	STO 01	
2		u	STO 02	
3		s	STO 03	
4			A	P(0)
Steps 5 through 13 may be executed in any order:				
5			A′	U
6		N	B	P(N)
7			B′	B
8			C	TW
9		T	C′	P(TW>T)
10			D, RUN	TR, SDTR
11		T	D′	P(TR>T)
12			E	Q
13			E′	N

TABLE 2

Instructions for Multiserver Queuing Program Using TI-59 With Attached PC-100A Printer

Step	Procedure	Enter	Press	Print
0	Load two program cards			
1			A	
				ARRIVAL RATE?
		λ	R/S	
				SERVICE RATE?
		u	R/S	
				NUMBER SERVERS?
		s	R/S	
				U
				P(0)
				B
				Q
				N
				TW
				TR
				SDTR
Steps 2 through 4 may be executed in any order:				
2		N	B	P(N)
3		T	C′	P(TW>T)
4		T	D′	P(TR>T)

on the printer. Similarly, list the contents of the data registers with the two keystrokes "INV List." If no printer is available, check accuracy by manually single-stepping (SST) through all 712 instructions and recalling (RCL) the contents of the data registers. Correct any wrong instruction entry by reentering that keystroke and, if necessary, using the calculator editing keys. Data register errors are corrected by re-storing (STO) the right number over the wrong one.

Finally, repartition the calculator into 480 instructions and 60 data registers with the keystroke sequence "6 Op 17," and record the entire calculator memory on 2 magnetic cards for future use. Each card [2.9375″ (7.46 cm) in length and 0.625″ (1.59 cm) in width] is recorded twice, once in each direction. There are four banks of calculator memory; two are recorded on each card. Press "1" and then "Write" to record the first memory bank on the top side of card 1; "2"

Program for Multiserver Queuing Model

Partition: 719.29

Program Listing:

```
000: Lbl X STO 8 ( x=t 15 RCL 8 X Dsz 8 005 1 ) INV SBR STO 9 Op 00
022: RCL Ind 9 Op 1 Op 29 RCL Ind 9 Op 2 Op 29 RCL Ind 9 Op 3 Op 29
040: If flg 3 50 RCL Ind 9 Op 4 Op 29 Op 5 CLR INV St flg 3 INV SBR
057: Lbl A' CLR 1 STO 05 41372427 Op 4 RCL 1 ÷ RCL 2 ÷ STO 4 RCL 3 =
084: INV SUM 5 Op 6 INV SBR Lbl A CLR INV St flg 1 CP Adv 3 Op 17 INV
102: St flg 7 20 Op 7 Op 18 CE If flg 7 158 10 SBR 18 SBR 20 Adv St flg 3
126: SBR 20 R/S STO 1 Prt St flg 3 SBR 20 R/S STO 2 Prt St flg 3 SBR 020
147: R/S Int STO 3 Prt Adv St flg 3 SBR 20 SBR 59 RCL 3 − 1 STO 7 =
168: x=t 190 STO 0 RCL 4 y^x RCL 0 ÷ RCL 0 SBR X = SUM 7 Dsz 0 173 RCL 04
192: y^x RCL 3 ÷ STO 6 RCL 5 ÷ RCL 3 SBR X + 2033550156 Op 4 RCL 7 = 1/x
222: STO 7 Op 6 If flg 7 17 SBR 316 SBR 377 SBR 390 SBR 329 GTO 353
245: Lbl B STO 0 − Adv St flg 1 SBR 610 31 Op 4 RCL 0 Op 6 RCL 3 = x≥t
268: 277 RCL 0 SBR X GTO 287 Exc 3 y^x Exc 3 X RCL 3 SBR X ÷ RCL 7 ÷
291: RCL 4 y^x 2033553156 Op 4 RCL 0 = 1/x Op 6 R/S Lbl B' CLR 14 Op 04
320: SBR 442 Op 6 INV SBR Lbl C CLR 3743 Op 4 SBR 506 Op 6 INV SBR
341: Lbl C' Adv SBR 400 Op 6 INV SBR Lbl D CLR 3735 Op 4 SBR 502 Op 06
364: If flg 7 456 SBR 458 Op 6 INV SBR Lbl E CLR 34 Op 4 SBR 519 Op 06
386: INV SBR Lbl E' CLR 31 Op 4 SBR 498 Op 6 INV SBR X STO 0 INV St flg 0
406: SBR 610 37 Op 4 RCL 0 Op 6 RCL 3 X RCL 2 X RCL 5 +/− = INV lnx X
430: 2037436037 Op 4 RCL 6 X RCL 7 ÷ RCL 3 SBR X ÷ RCL 5 = INV SBR CLR
458: 2 − 2036163735 Op 4 SBR 442 X SBR 442 + RCL 3 x² X RCL 5 x² = √x
489: ÷ ( SBR 442 X GTO 506 RCL 1 X ( RCL 2 1/x + RCL 2 1/x ÷ RCL 3 ÷
513: RCL 5 X GTO 442 RCL 1 X GTO 506 Lbl D' Adv STO 0 St flg 0 SBR 610
535: 37 Op 4 RCL 3 1/x − RCL 5 = X RCL 0 Op 6 X RCL 2 X RCL 3 = INV lnx
560: +/− + 1 = ÷ ( RCL 5 − RCL 3 1/x = ÷ RCL 3 X SBR 442 + 1 = X ( RCL 02
587: X 2037356037 Op 4 RCL 0 +/− ) INV lnx = Op 6 R/S 3335321455 Op 01
622: If flg 1 682 If flg 0 643 3743002713 GTO 653 3735002713 Op 02 35221735
663: 00 Op 03 3756000000 Op 4 Op 5 INV SBR 3100243717 Op 02 3036560000 Op 03
706: INV St flg 1 GTO 675
```

Prestored Data Registers:

```
10: 3041273724 3617354217 3500003441 1741243122 4040404040 4000003032
16: 1617270000 4040404040 1335352442 1327003513 3717710000 3617354224
22: 1517003513 3717710000 3141301417 3500361735 4217353671 3637133724
28: 3637241536 2000000000
```

and "Write" to record the second bank of memory on the bottom side of card 1; "3" and "Write" to record the third memory bank on the top side of card 2; and "4" and "Write" to record the fourth memory bank on the bottom side of card 2.

The next time a queuing analysis is needed, it is not necessary to reenter instructions or prestore data registers; merely feed the two magnetic cards into the calculator, one side at a time. Press either "0" or the number of the next memory bank before each feed. All 712 instructions and 30 data registers will be read from the 2 magnetic cards and loaded into the calculator memory. The first program execution reallocates memory from its initial 479.59 partition to the required 719.29 partition.

User Instructions

Two sets of user instructions are included, Table 1 for a calculator operating alone and Table 2 for a calculator with a printer attached. The calculator has been programmed to automatically sense when a printer is connected and to respond accordingly. The three necessary input parameters are arrival rate (λ), service rate (u), and number of servers (s). Units of time for λ and u should correspond. If both λ and u are in units of items/second, then waiting time and response time also will be in seconds. If λ and u are in items/hour, then waiting and response times similarly will be in hours. The term item is used here to convey the general nature of the model and can be interpreted as representing almost any entity seeking service. Depending upon the application, items can represent patients, visitors, automobiles, airplanes, messages, jobs, transactions, or disc accesses.

To initiate a simulation with the TI-59 calculator connected to a printer, follow the user instructions in Table 2. Pressing the "A" key at the top of the calculator starts the program by printing the heading

"MULTISERVER QUEUING MODEL," followed by an inquiry requesting the arrival rate.

The calculator waits until an arrival rate is entered and the run/stop (R/S) key is pressed. Entries are displayed immediately on the calculator light emitting diode readout. Mistakes can be cleared (CE) and corrected by reentry. Pressing R/S prints the arrival rate and continues calculator processing by printing a second prompting message requesting the service rate. When this input is followed by an R/S, the calculator prints the service rate and then requests the number of servers.

After this third parameter is input and the R/S key is pressed again, the calculator prints the number of servers, does the simulation, and ends by printing eight queue performance attributes with appropriate mnemonics at their right. Additional probability statistics can be obtained, via steps 2 through 4 in Table 2, by entering appropriate values corresponding to either integers or times, and then depressing whichever calculator key (B, C′, or D′) is desired.

Utilization (U) of each server (s) is the same because work is distributed equally. The probability of finding N items—those queued and those being serviced—in the system is P(N), which can be computed for any N value. P(0) is the probability of finding a completely empty system with no items queued and none being serviced.

As long as no more than s items are simultaneously in the system, items are immediately serviced without waiting, and the queue remains empty. As soon as a system has more items than servers, a queue forms. B is the probability of finding s or more items in the system or, in other words, having to wait on a queue. The average time an item spends waiting in the queue is TW; P(TW>T) can be computed for any time T and represents the probability of having to wait for

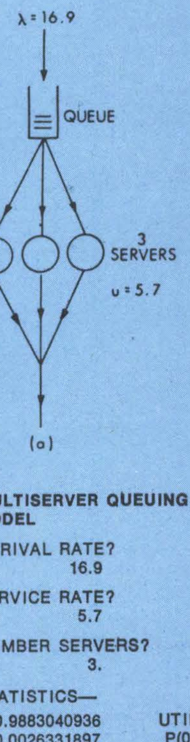
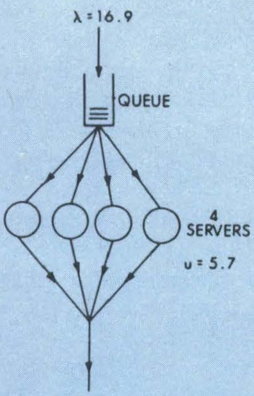


Fig 1 3-server queuing model. Assume that three IBM 1403 line printers (a) are servicing one large batch computer system, where an average of 16.9 jobs/h needs to be printed. If, according to specifications, each printer is only capable of outputting 5.7 jobs/h, then operation with three printers will be inadequate according to queuing model (b). High 98.83% printer utilization (UTIL) causes queue to back up with processed, but as yet unprinted, jobs. Mean queue length is 82.64 jobs (Q), and average time to get a job printed, once its processing has been completed, is slightly more than 5 h (TR). There is a 13.24% probability of processed jobs having to wait more than 10 h for printing (TW ↑ 10)

```
MULTISERVER QUEUING
MODEL

ARRIVAL RATE?
        16.9
SERVICE RATE?
         5.7
NUMBER SERVERS?
          3.

STATISTICS—
0.9883040936      UTIL
0.0026331897      P(0)
0.9779858368         B
 82.63980321         Q
 85.60471549         N
 4.889929184        TW
  5.06536778        TR
 5.001865963      SDTR

PROB(N ITEMS)
          1.         N
0.0078071766      P(N)
PROB(N ITEMS)
          2.         N
0.0115737969      P(N)
PROB(N ITEMS)
          3.         N
0.0114384308      P(N)

PROB(N ITEMS)
          4.         N
 0.011304648      P(N)
PROB(N ITEMS)
         20.         N
0.0093649735      P(N)
PROB(N ITEMS)
        100.         N
0.0036538784      P(N)
PROB(N ITEMS)
        140.         N
 0.002282327      P(N)
PROB(TW LARGER T)
          0.         T
0.9779858368    TW ↑ T
PROB(TW LARGER T)
          2.         T
0.6555635111    TW ↑ T
PROB(TW LARGER T)
          4.         T
 0.439437363    TW ↑ T
PROB(TW LARGER T)
          6.         T
0.2945636734    TW ↑ T

PROB(TW LARGER T)
          8.         T
0.1974519351    TW ↑ T
PROB(TW LARGER T)
         10.         T
0.1323559902    TW ↑ T
PROB(TR LARGER T)
          0.         T
          1.    TR ↑ T
PROB(TR LARGER T)
          2.         T
0.6794020326    TR ↑ T
PROB(TR LARGER T)
          4.         T
0.4554169034    TR ↑ T
PROB(TR LARGER T)
          6.         T
0.3052750797    TR ↑ T
PROB(TR LARGER T)
          8.         T
0.2046320054    TR ↑ T
PROB(TR LARGER T)
         10.         T
0.1371689353    TR ↑ T
```

(b)



(a)

Fig 2 4-server queuing model. According to this model, installing additional printer (a) alleviates queuing problem of Fig 1 by lowering utilization of each printer to 74.12% (UTIL), which is below critical 80% level (b). Response time (TR) drops to 0.26 h (15 min, 36 s), and queue contains only average of 1.42 jobs (Q). Probability of response time ever exceeding 1 h is only 1.19% (TR ↑ 1)

```
MULTISERVER QUEUING
MODEL

ARRIVAL RATE?
        16.9

SERVICE RATE?
        5.7

NUMBER SERVERS?
        4.

STATISTICS—
0.7412280702        UTIL
0.0397661205        P(0)
0.4948028745        B
 1.417316708        Q
 4.382228989        N
 0.083864894        TW
0.2593034905        TR
0.2284166332        SDTR

PROB(N ITEMS)
        1.          N
0.1179030591        P(N)

PROB(N ITEMS)
        2.          N
0.174786114         P(N)

PROB(N ITEMS)
        3.          N
0.1727418319        P(N)

PROB(N ITEMS)
        4.          N
0.1280410947        P(N)

PROB(N ITEMS)
        5.          N
0.0949076535        P(N)

PROB(N ITEMS)
        10.         N
0.0212354038        P(N)

PROB(N ITEMS)
        14.         N
0.0064101465        P(N)

PROB(TW LARGER T)
        0.02        T
0.4397293614        TW ↑ T

PROB(TW LARGER T)
        0.06        T
0.3472897514        TW ↑ T

PROB(TW LARGER T)
        0.08        T
0.3086350312        TW ↑ T

PROB(TW LARGER T)
        0.1         T
0.2742827339        TW ↑ T

PROB(TW LARGER T)
        0.5         T
0.025897837         TW ↑ T

PROB(TW LARGER T)
        1.          T
0.0013554852        TW ↑ T

PROB(TR LARGER T)
        0.1         T
0.7234404837        TR ↑ T

PROB(TR LARGER T)
        0.2         T
0.496660615         TR ↑ T

PROB(TR LARGER T)
        0.3         T
0.329398148         TR ↑ T

PROB(TR LARGER T)
        0.5         T
0.1354697506        TR ↑ T

PROB(TR LARGER T)
        1.          T
0.0118990479        TR ↑ T

PROB(TR LARGER T)
        10.         T
2.3204449-24        TR ↑ T
```

(b)

a time longer than T. Response time TR is the sum of waiting and service times; it is the total time an item spends in the system from input to output. SDTR is the standard deviation of response time; P(TR>T) can be computed for any T and is the probability that response time is greater than time T. The average number of items in the queue and in the entire system are Q and N, respectively.

Applications

Fig 1 shows three servers, each capable of processing 5.7 items/s, subjected to a 16.9-item/s arrival rate. Input parameters are, therefore, $\lambda = 16.9$, $u = 5.7$, and $s = 3$. Running the model for this M/M/3 queuing system predicts that each server will be 98.83% utilized (UTIL); that is, 9.883 s of activity will occur for each 10-s time period. High utilization increases the probability of items residing in the system, either in the queue or at the servers. P(0) reveals that there is only a 0.26% probability of finding the system without any items in it. Conversely, there is a 99.74% probability of finding items somewhere in the system.

When utilizations go above 80%, queues build and waiting times on queues increase significantly. In Fig 1, the probability (B) of having to wait for service on the queue is 97.80%, an almost absolute certainty. There is an average of 85.60 items (N) in the system, 82.64 (Q) of which are in the queue. Items are delayed in the queue for an average of 4.89 s (TW), and it takes 5.07 s (TR) for an item to go through the entire system, from input to output. The response time distribution is approximately exponential because standard deviation (SDTR = 5.00) is very close to the mean (TR = 5.07).

According to Fig 1, the likelihood of exactly 20 items (N) residing in the system [P(20)] is 0.94%. Summing P(N) from N = 0 through N = 20 results in a probability of

$$P(0) + P(1) + P(2) + P(3) + P(4) + \ldots + P(20) = \sum_{N=0}^{20} P(N)$$

0.26% + 0.78% + 1.16% + 1.14% + 1.13% + . . .
+ 0.94% = 20.61%

Adding together values of P(N) for N = 0 through 100 gives 69.12%. Summing P(N) from N = 0 through 140 gives 80.71%, or a 19.29% (100% − 80.71%) probability of having more than 140 items in the system at any time.

An upward arrow (↑) in printer outputs replaces the conventional greater than (>) symbol, which is not included in the 64-character capability of the printer. These two symbols are used interchangeably in this article.

Since both B and P(TW>0) represent the likelihood of having to wait for service, they give an identical result in Fig 1 of 97.80%. The probability of having to wait longer than T seconds, P(TW>T), is determined by inputting T and then pressing the C′ key. In Fig 1, for example, there is a 65.56% probability (TW ↑ T) of having to wait on line for longer than 2 s (T), or conversely, a 34.44% (100% − 65.56%) probability of having to wait for 2 s or less. Even though the average waiting time TW is 4.89 s, P(TW>10) means that there is still a 13.24% probability of an item having to wait more than 10 s before receiving service. P(TR>0) is always 1.0 (or 100%), because even if the waiting time is zero, servicing an item still takes some time. Given any T, P(TR>T) will be greater than P(TW>T) due to service time. Although the average system response time (TR) computes to 5.07 s in Fig 1, there is still a 13.72% probability of response time (TR ↑ T) exceeding 10 s (T).

Designers must consider the maximum response times of all items and not be content only with average response time. If a certain response time is intolerable, queue input parameters should be modified until the probability of ever exceeding that response time is sufficiently small. Suppose the occurrence of response times in excess of 10 s needs to be minimized. Then the configuration in Fig 1 may not meet specifications because of the 13.72% probability (TR ↑ T) of response time exceeding 10 s (T). However, as the model in Fig 2 illustrates, adding a fourth server reduces the likelihood of a 10-s (T) response time to only 2.32 x 10^{-22}% (TR ↑ T), which is a negligible amount.

Iterative Design

Having this multiserver queuing model preprogrammed on a handheld calculator enables designers to interactively change input parameters and to experiment with prospective alternatives. In Fig 2, an additional—or fourth—server is provided, but λ and u are not changed. For this M/M/4 queuing system, note that server utilization (UTIL) reduces from 98.83% to 74.12%, queue size (Q) decreases from 82.64 to 1.42 items, and waiting time (TW) shortens from 4.89 to 0.08 s. Summing P(N) from N = 0 through N = 14 gives 98.16% as the probability of finding 14 or fewer items in the system at any one time. Conversely, this leaves only a 1.84% (100% − 98.16%) probability of there ever simultaneously being more than 14 items in the system.

When P(TW>1) is computed, there is only a 0.14% probability of waiting time (TW ↑ T) exceeding 1 s (T). According to P(TR>1), there is only a 1.19% likelihood of response time (TR ↑ T) exceeding 1 s (T). The addition of the fourth server (Fig 2) to the configuration of Fig 1 has resulted in significantly improved system performance. Without the queuing model, designers would be unable to quantitatively compare the performance of these two configurations in a fast and easy manner. By using the model, designers can predict and evaluate system performance conveniently in just a few minutes.

Fig 3 lists modeling results when the arrival rate is increased by 25%, the service rate is doubled, and the number of servers is reduced to two. Due to the high 92.65% utilization (UTIL) at each server of this M/M/2 system, most arriving items find both servers busy; the probability of their having to wait for service in the queue is 89.12% (B). Mean queue length at equilibrium is 11.24 items (Q), and there is an average of 13.09 items (N) in the entire system at any time. Items are queued for an average of 0.53 s (TW), and their total system response time, from input to output, is 0.62 s (TR). SDTR is 0.60, quite large and almost equivalent to response time itself, indicative of an exponential distribution. Summing P(N) from N = 0 through N = 5 gives 34.33%, which translates to a 65.67% (100% − 34.33%) probability of the system containing more than five items. Since a maximum of one item can reside at each of the two servers, this also predicts a probability greater than 65.67% of queue size exceeding three. There is a 16.69% (TW ↑ T) probability of waiting time exceeding 1 s, and the possibility of response time exceeding 1 s is 19.57% (TR ↑ T). Only a very small likelihood exists of either finding waiting or response times longer than 10 s.

Modeling of queues is accomplished accurately and quickly. Reading the two magnetic cards that program the calculator takes less than 30 s, and the printer can print its prompting messages for λ, u, and s in less than 15 s. After these input parameters have been entered, execution of the Multiserver Queuing Equations begins. Running time for the examples in Figs 1 and 3, including the printing of "STATISTICS," takes 50 and 30 s, respectively. Even the more complicated 4-server configuration in Fig 2 computes in less than 1 min.

Summary

The Multiserver Queuing Equations can rapidly be implemented on both programmable calculators and microcomputers with relative ease; programming is comparable because firmware in the calculator read-only memory replaces the microcomputer's high level application language instruction set. Microcomputers would not be much faster than calculators since the equations would probably be programmed in BASIC, an interpretive language whose floating point arithmetic operations are not noted for their speed. Three advantages of using the programmable calculator/printer package over a video display terminal type of microcomputer are portability, hardcopy printout, and cost.

Discrete detailed models programmed on large computer systems in powerful simulation languages, such as GPSS (General Purpose Simulation System) and SIMSCRIPT, require a great deal of preparatory effort on the part of the analyst/programmer and many minutes, or even hours, of computer run time before results reach

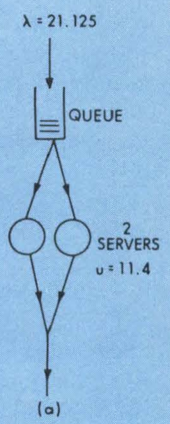


Fig 3 2-server queuing model. Level of performance is predicted for configuration requiring average of 21.125 jobs/h (λ) to be printed, with four printers of Fig 2 replaced by two high speed printers (a) that operate twice as fast, at 11.4 jobs/h (u). Poorer performance than in Fig 2 can be expected because printer utilization rises above 80%; in this case, up to 92.65% (UTIL). In (b), an average of 11.24 jobs is queued (Q), each for an average of TW = 0.53 h (31 min, 48 s). Although probability (TR ↑ 1) of response time exceeding 1 h is 19.57%, probability of response time ever exceeding 10 h (TR ↑ 10) is infinitesimal

```
MULTISERVER QUEUING
MODEL

ARRIVAL RATE?
        21.125
SERVICE RATE?
          11.4
NUMBER SERVERS?
            2.
STATISTICS—
  0.9265350877     UTIL
  0.0381331816     P(0)
   0.891203357        B
   11.23980353        Q
   13.09287371        N
  0.5320617057       TW
  0.6197810039       TR
  0.5999188075     SDTR
PROB(N ITEMS)
            1.        N
  0.0706634614     P(N)
PROB(N ITEMS)
            2.        N
  0.0654721764     P(N)
PROB(N ITEMS)
            3.        N
  0.0606622687     P(N)

PROB(N ITEMS)
            4.        N
  0.0562057205     P(N)
PROB(N ITEMS)
            5.        N
  0.0520765722     P(N)
PROB(N ITEMS)
           10.        N
  0.0355591805     P(N)
PROB(N ITEMS)
           14.        N
  0.0262059088     P(N)
PROB(TW LARGER T)
           0.2        T
  0.6375117039   TW ↑ T
PROB(TW LARGER T)
           0.4        T
  0.4560364023   TW ↑ T
PROB(TW LARGER T)
           0.6        T
  0.3262202073   TW ↑ T
PROB(TW LARGER T)
           0.8        T
  0.2333577389   TW ↑ T

PROB(TW LARGER T)
            1.        T
  0.1669296783   TW ↑ T
PROB(TW LARGER T)
           10.        T
  0.0000000474   TW ↑ T
PROB(TR LARGER T)
           0.2        T
  0.7427422737   TR ↑ T
PROB(TR LARGER T)
           0.4        T
  0.5341148523   TR ↑ T
PROB(TR LARGER T)
           0.6        T
  0.3823594005   TR ↑ T
PROB(TR LARGER T)
           0.8        T
  0.2735455672   TR ↑ T
PROB(TR LARGER T)
            1.        T
  0.1956805621   TR ↑ T
PROB(TR LARGER T)
           10.        T
  0.0000000555   TR ↑ T
```

(b)

steady state and are valid. Although the described multiserver queuing model is meant to supplement these more detailed simulations and is not intended to replace them, a queuing analysis performed on a programmable calculator is a fast and economical approach, and a useful and powerful computer system design tool for pinpointing inherent weaknesses, determining critical paths, and finetuning system performance.

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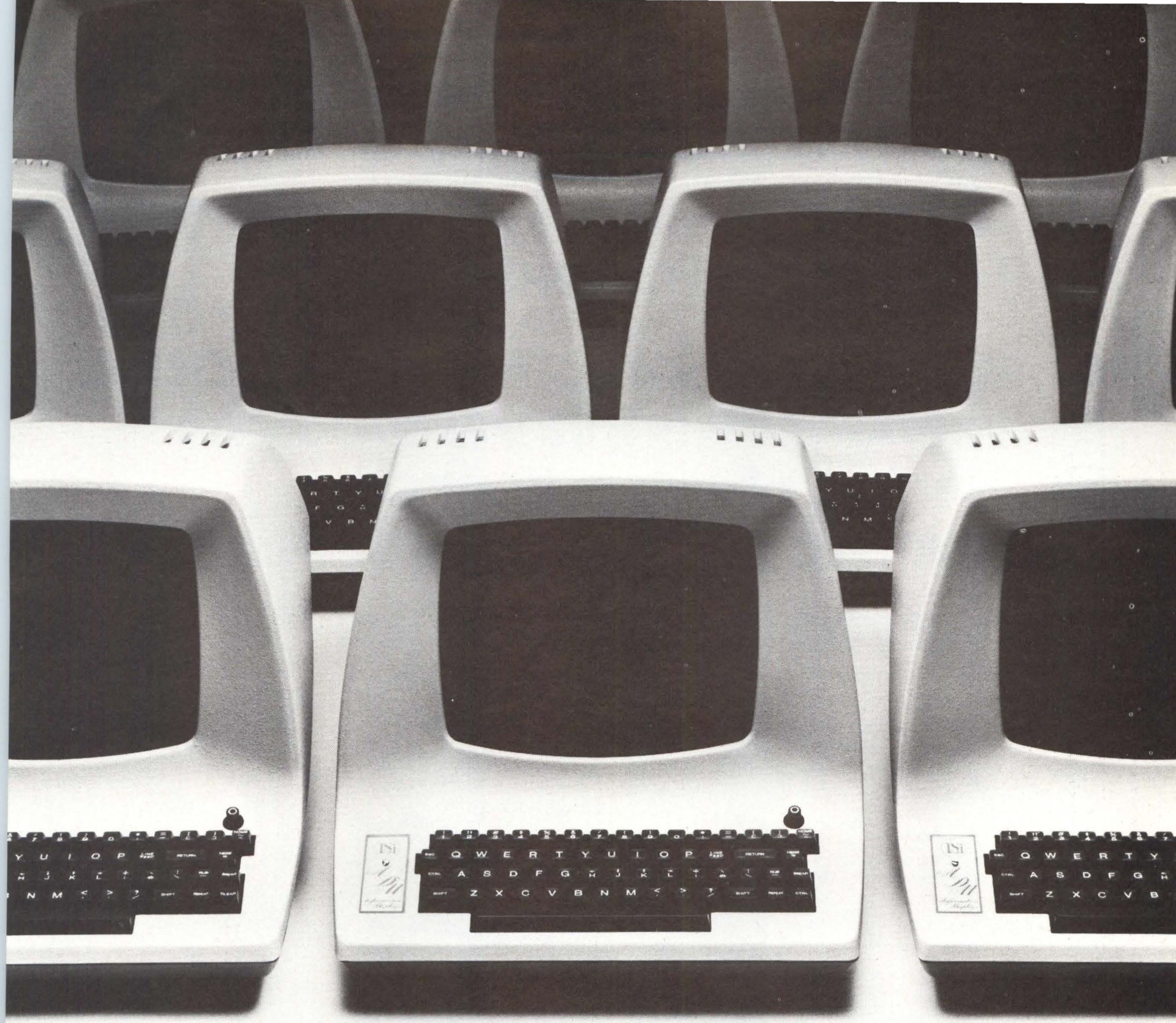

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CODE CONVERSION TECHNIQUES FOR DIGITAL TRANSMISSION

Systems using delta modulation techniques are becoming popular. Two design approaches for converting delta modulation to pulse code modulation, standard format for digital transmission networks, can be implemented with currently available digital technology

S. Ghosh TRW Vidar, Mountain View, California

Technical and economic advantages of coding audio and video signals into digital formats are well established. Digital representations permit simpler data transmission methods, processing of complex signals, and convenient storage and retrieval. Common techniques for converting audio and video signals into digital formats include pulse code modulation, differential pulse code modulation, and delta modulation.[1] Historically, pulse code modulation has been extensively used for speech digitizing and is the standard format for transmission over digital networks in the U.S. and abroad. Additionally the pulse code modulation format is convenient for complex digital signal processing, such as filtering or level adjustments. However, the other two schemes are becoming increasingly popular. Compared with pulse code modulation, differential pulse code modulation generally requires a slower bit rate for the same fidelity. Delta modulation is the simplest and most economical of the three coding techniques.

Increasing implementation of delta modulation (DM) for speech digitization has been discernible at local levels.[2, 3, 4] Concurrently, suitable techniques have evolved for converting DM into pulse code modulation (PCM) when necessary. For example, DM should be converted to PCM format for transmission over national networks, since digital transmission systems using cable or radio terminate at PCM channel banks, or at digital switches like No 4 ESS, which are based on PCM format. One conversion technique decodes DM to analog signals and then reconverts these signals to PCM. A more efficient method is conversion by digital signal processing. Another important application of DM-to-PCM conversion is to design PCM encoders (analog-to-digital converters for coding audio signals into PCM) based on DM-to-PCM conversion techniques.[5, 6, 7, 8] Speech is digitized by using a relatively simple delta modulator, followed by digital signal processing to produce PCM. LSI technology enables an increasing complexity of digital hardware on a single chip, and digital signal processing for DM-to-PCM conversion offers an efficient and attractive alternative for realizing a PCM encoder.

PCM Format

Speech encoding into PCM involves the following process (Fig 1):

(1) An analog input signal is bandlimited by a low pass filter to W Hz (about 3400 Hz for speech).

(2) The bandlimited signal is sampled at a rate (f_r) that must equal or exceed the Nyquist frequency ($f_r \geq 2W$). (The commonly used value for f_r is 8k bits/s for speech.)

(3) The sampled signal, which ideally represents an instantaneous signal value, is held in a sample-and-hold

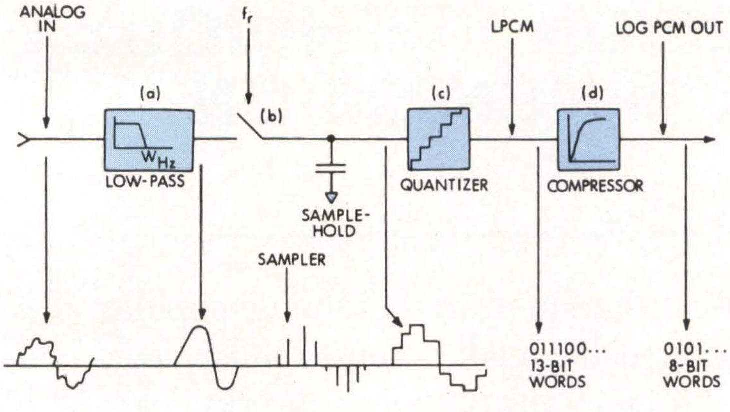

Fig 1A PCM encoding. This type of modulation converts speech signals into 8-bit words at 8k words/s. Encoding process involves: (a) input filtering, (b) sampling at 8k words/s, (c) quantizing, and (d) compression

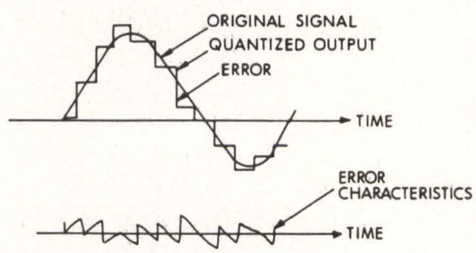

Fig 1B Quantizing noise. PCM encoding quantizes continuously variable input signal into one of 2^m discrete levels. Difference between input and quantized output is error voltage. This voltage produces noise-like effect on reconstructed output, known as quantizing noise

capacitor during the period between two sampling instants. During this interval, the sample is quantized into one of 2^m levels, if the coder is designed to produce m-bit words per sample. For example, a 4-bit coder with a quantizing step size of 1 will encode an input sample of amplitude 13.2 as 13 $(1\ 1\ 0\ 1)_2$. The larger the number of bits per word, the more accurate is representation of input samples by the coder.

(4) A coder with uniform quantizing step sizes is called a linear coder, and it produces linear PCM (LPCM) words. An m-bit coder will require f_r x m bits/s. A 13-bit coder (North American telephone quality standards require 13 bits to encode low level signals) will, therefore, need 104k bits/s per speech channel. To reduce this excessive bandwidth requirement, the linear PCM words are compressed according to a well-defined algorithm (μ-law in North America, A-law in Europe, μ and A being the compression parameters)[9] to produce 8-bit compressed PCM words (referred to as CPCM or Log PCM because of the near logarithmic characteristics of compression laws). This compression involves increasing step sizes when input signal is large; thus, the fine structure required for encoding an extremely low level signal is no longer required. In conventional PCM encoders, the two functions of quantization and compression are often combined. However, the configuration in Fig 1 is pertinent, since digital processes described are concerned with DM-to-LPCM conversion and LPCM-to-DM reconversion. Compression from, and expansion to, LPCM may be done digitally[9].

(5) For decoding, the 8-bit compressed words are mapped back into amplitude levels, and the amplitude pulse samples are low-pass filtered by a filter having bandwidth W Hz.

To facilitate later discussions, it is convenient to summarize the characteristics of the m-bit PCM coder described above. The nth input sample (y_n) is represented at the coder output by an m-bit word, such that

$$Y_n = k \sum_{1}^{m-1} a_i 2^i \qquad (1)$$

where

k = quantizer step size
a_i = 1 or 0
a_m = 0 for positive signal or 1 for negative signal

The PCM coder is, therefore, an analog-to-digital converter of bandlimited input signals with sign-magnitude representation.

The process of quantization, (rounding off a sample to one of 2^m discrete levels), produces errors. These errors as they occur from sample to sample are random in nature, and have noise-type effects on the reconstructed signals. This is called quantization noise, and its nearly uniform spectrum extends approximately to $f_r/2$.

Total quantizing noise power (n_1) is given by

$$n_1 = k^2/12 \qquad (2)$$

Minimum amplitude that the coder can represent is k, and maximum level it can encode without overloading is given by

$$S_{max} = 2^m \text{ x } k \qquad (3)$$

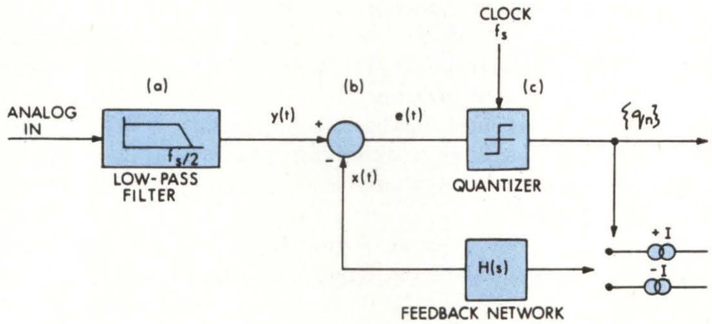

Fig 2A Delta modulation. This type of modulation converts analog signal into 1-bit digital words every clock interval. Encoding process involves: (a) input filtering, (b) subtracting estimate of output from input, and (c) quantizing error voltage into one-bit words

Delta Modulator Format

In PCM, an instantaneous sample of the input signal is converted into an m-bit word. The principles of DM encoding are quite different (Fig 2). Bandlimited input signal y(t) is always being compared with x(t), which is an approximation (or prediction) of the input derived from the encoder's digital output. At intervals controlled by clock (f_s), the output of the comparator, which is the error signal $e(t) = y(t) - x(t)$, is quantized into one-bit words (q_n). If e(t) is positive, the quantizer outputs a 1, otherwise a 0. Output sequence (q_n) controls injection of two current pulses ($\pm$ I) into a linear feedback network H(s); a 1 switches + I, and a 0 switches − I. Design of the feedback network enables its output to be an estimate of the input at the next clock pulse.

The following characteristics of DM (also known as 1-bit predictive encoding) should be noted:

(1) Coder structure is inherently simpler than that of the PCM coder. There is no sample-and-hold operation, and the quantizer produces one-bit words compared with m-bit words for PCM. The quantizer can be implemented by a limiting amplifier with zero threshold.

(2) Clock rate (corresponding to the sampling rate in PCM) is generally much higher than the PCM sampling rate $f_s >> f_r$), which permits use of a much simpler (and therefore less expensive) bandlimiting input filter. To illustrate this point, consider a PCM coder and a DM coder both operating at 64k bits/s. Sampling rate for PCM is 8k bits/s. PCM input filter must pass 3400 Hz (upper edge of speech band), but must cut off at 4000 Hz, requiring a relatively steep-sloped filter. For DM, however, the input filter must also pass 3400 Hz, but must cut off at 32 kHz (half of the clock rate of 64k bits/s), which can be realized with a gradually sloped filter.

(3) Feedback network H(s) is optimized to produce as close an approximation to the input signal as possible; therefore, its design depends on the statistics of the input signal. In its simplest form, H(s) is an integrator for speech-type inputs, but double integrators can be shown to yield better performance.[10]

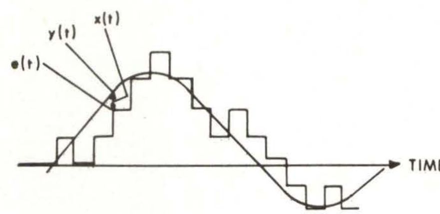

Fig 2B Quantizing noise. Waveforms show input voltage, y(t), its estimate, x(t), and quantizing errors, e(t), at clock intervals. If error is positive (input greater than estimate), output is 1; otherwise, output is 0

(4) Step size of the delta modulator is determined by impulse response of H(s) to input current pulses ($\pm$I). Each time this current pulse is switched in, the output of H(s) changes by + (or −) ∂. If injected current pulses are always equal, step sizes are uniform and the delta modulator is called a linear DM (LDM). As in the case of PCM, step sizes may be adapted to follow the input to reduce the bit rate required for operation. Coders that employ variable step sizes are referred to as adaptive DM (ADM).

(5) For an LDM, the maximum slope at the output of H(s) occurs when coder output is successive 1s (or 0s), and is given by

$$\text{Maximum slope} = \partial f_s \qquad (4)$$

If the input slope is greater than that indicated by Eq 4, slope overload will occur. This should be contrasted with the amplitude-overload condition of a PCM coder [Eq (3)]. To avoid slope overload, the design criterion for ∂ is taken as

$$\partial f_s = 8\pi\sigma f_e \quad (5)$$

where

σ = rms amplitude of input signal
f_e = rms input frequency

(6) Total quantizing noise power, (n_2), of a linear coder is given by

$$n_2 = \partial^2/3 \quad (6)$$

As in the case of PCM, the noise spectrum is nearly uniform and extends to $f_s/2$.

(7) Note that when H(s) is an integrator, analog input y(t) to the coder approximates the integral of digital output (q_n). This is different from PCM, where output words tend to equal sampled values of input.

DM-To-PCM Conversion

Referring to Fig 2, x(t), which is an approximation of input y(t), is obtained by passing digital output sequence (q_n) through linear feedback network H(s). It follows, therefore, that if coder output (q_n) is applied to a digital processor, H(z), having the same transfer function in the frequency domain as H(s), output of H(z) is an approximation of the digital representation of y(t), and LPCM samples may be obtained by interrogating H(z) at the Nyquist rate (f_r). Fig 3 illustrates this basic concept. Note that in this simple approach, since sampling rate is f_r (PCM sampling rate), input filter should cut off at $f_r/2$ (as in the PCM input filter).

Fig 4 shows a practical implementation of a DM-to-PCM converter based on principles of Fig 3. It is assumed that H(s) is an integrator and therefore H(z) is either an up-down counter or an accumulator. The delta modulator is an LDM operating at clock rate f_s, as in Fig 2, except that the input filter is similar to a PCM input filter of bandwidth W ($=f_r/2$). Digital output of the LDM controls the count of an m-bit up-down counter; a 1 causes a count-up, and a 0, a count down. The counter is organized to count in 2's complement mode.

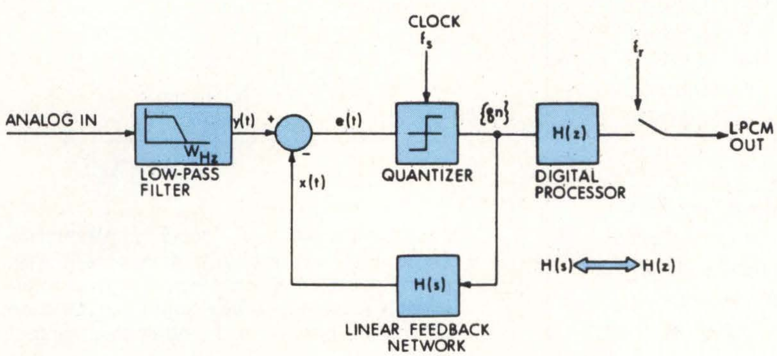

Fig 3 DM-to-PCM conversion. This type of conversion is obtained by applying DM output to digital processor H(z), which is equivalent to feedback network H(s). Output of H(z) is digital equivalent of x(t), and is therefore PCM representation of y(t)

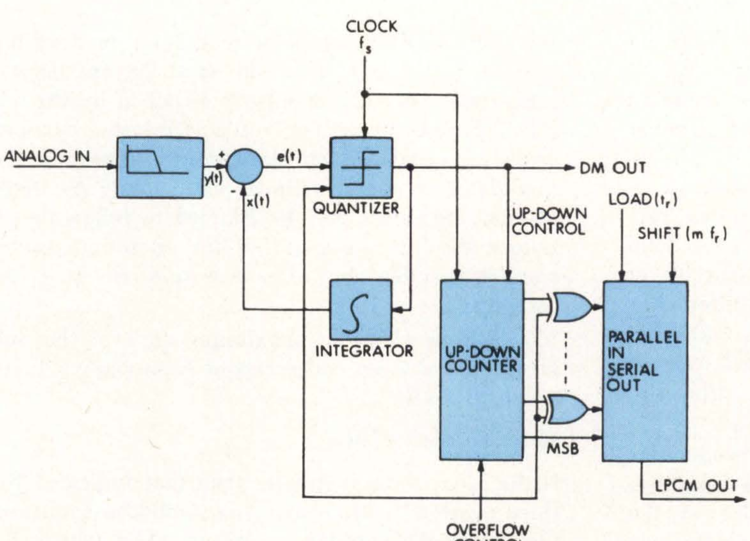

Fig 4 Practical DM-to-PCM converter. This conversion is realized by accumulating DM output in up-down counter, then interrogating contents of counter at sampling rate f_r. Note that up-down converter is digital equivalent of integrator

Assume that at time t_0, the input $y(t_0)$ is 0, and the counter is also in a 0 state (positive 0 = 00000..., or negative 0 = 11111...). Given these conditions, the counter output can be shown to be the PCM representation of the analog input. Let the input after n clock pulses be $y(t_n)$. From DM principles of operation,

$$y(t_n) = \partial(M_1 - M_2) \quad (7)$$

where M_1 = number of 1s in output (q_n) during n clock pulses and M_2 = number of 0s during same interval

However, the up-down counter at $t = t_n$ also represents $M_1 - M_2$. If the binary states of the m-bit counter are designated a_1 (LSB), a_1, . . ., a_m (MSB),

$$M_1 - M_2 = \sum_{1}^{m-1} a_i 2^i \quad (8)$$

and

$a_m = 0$ if $y(t_n)$ is positive, or 1 if $y(t_n)$ is negative

Comparison of Eq (1) and (8) shows that the counter output is the LPCM representation of input signal $y(t_n)$.

The MSB(a_m) of the counter represents the sign of the input signal. It is used to balance quantizer threshold so that average number of 1s and 0s over a period of time is equal (assuming that the input signal has no dc content, a correct assumption for speech). Balancing the quantizer this way ensures that the counter sign bit changes with the input signal sign bit, or that counter contents are 0 when input signal is 0. The MSB also controls a set of Exclusive-OR gates that convert the 2s complement output of the counter into the sign magnitude representation required for PCM. Outputs of these gates are parallel-loaded into an m-bit register at sampling intervals (f_r), and the register may be serially read out at a clock rate of mf_r.

A practical detail concerns overflow control of the counter. When the counter has reached its maximum count, one more 1 or 0 should not be allowed to cause overflow or underflow. The counter should then be maintained in a saturation state, indicating an overload of PCM output.

The simple approach outlined above, while basic in demonstrating principles involved, has two serious drawbacks. First, clock rate to produce m-bit PCM words is extremely high:

$$f_s \simeq 2^m \times f_r \quad (9)$$

For 13-bit words and a sampling rate of 8k words/s, $f_s \simeq$ 64M bits/s. Second, since the spectrum of the quantization noise produced by the DM extends to $f_s/2$, which is much wider than the Nyquist bandwidth, sampling this noise at f_r results in folding over the entire noise power into the signal passband. Total noise at coder output is, therefore, the sum of quantization noise n_1 [Eq (2)] and foldover noise n_2 [Eq (6)]:

$$n_t = n_1 + n_2 \quad (10)$$

In all practical realizations of DM-to-PCM converters, the clock rate is much lower than that given by Eq (9), and a digital filter is introduced before the PCM sampler to eliminate foldover noise. However, some of the circuit details described, such as balancing the quantizer or overflow control, are applicable to any practical design.

Practical Designs

Adaptive Delta Modulators

An effective method to reduce speed of operation is to use adaptive delta modulation (ADM) rather than linear delta modulation (LDM). As mentioned, step sizes in ADM are made to vary with the slope of the input signal, resulting in a corresponding reduction in clock rate. There are two types of ADM, syllabic and instantaneous. In syllabic ADM, step sizes change with syllables of

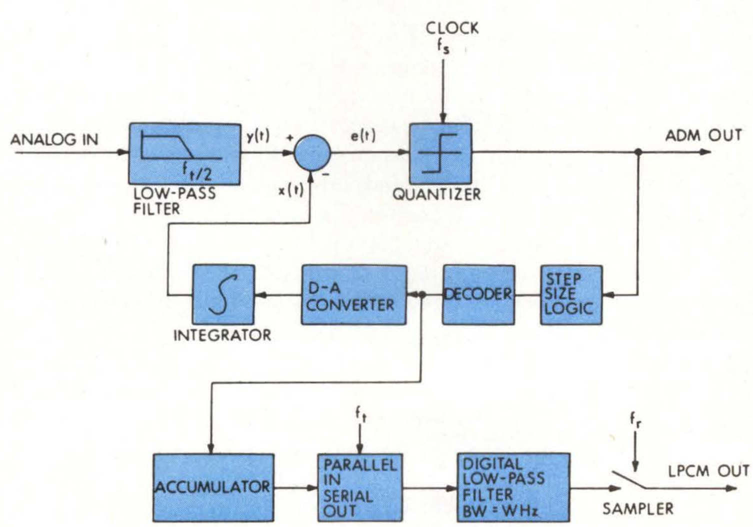

Fig 5 ADM-to-PCM conversion. Instantaneous step sizes are decoded and accumulated to produce PCM. Step sizes are varied depending upon magnitude of input signal, resulting in reduced speed of operation for delta modulator

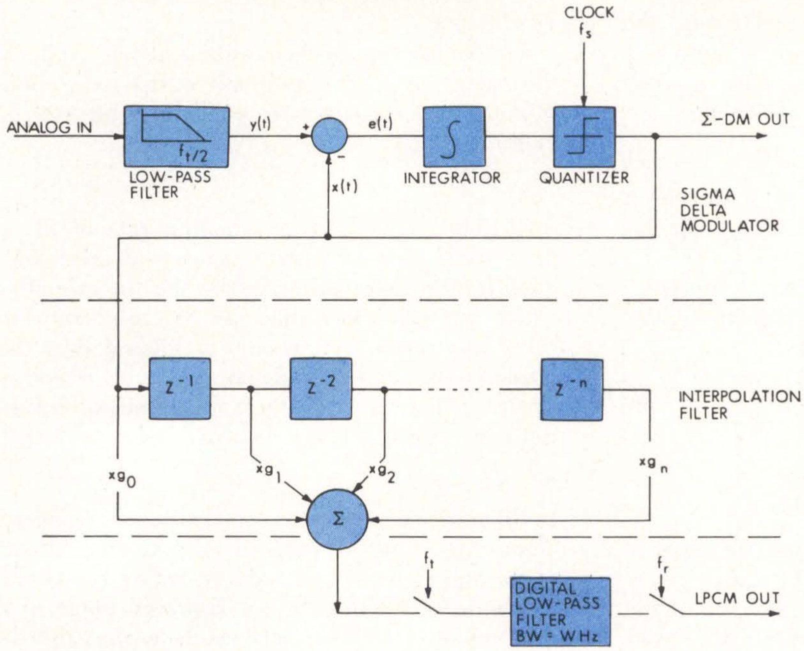

Fig 6 DM-to-PCM converter. Output of sigma delta modulator is processed by interpolation filter to produce PCM. Except for delta modulator, hardware is entirely digital

input speech relatively slowly. For instantaneous ADM, step sizes vary according to defined algorithms, depending on latter transmitted bits. For example, if the latter four transmitted bits are 1s, step size is doubled, or if the latter four transmitted bits are 0s, step size is halved. Instantaneous ADM is more suitable for conversion to PCM because step size information, contained in the bit stream, can be expanded easily into linear binary words for subsequent digital signal processing.

Fig 5 shows an ADM-to-PCM converter based on this principle.[5,6,8] The step-size logic monitors the number of successive 1s and 0s in the coder output, and produces binary words representing instantaneous step size. These binary words are translated into a series of binary-weighted current pulses by a digital-to-analog converter for injection into the integrator. The accumulator maintains a running sum of the binary words, and contents of the accumulator are transferred to a parallel register at a rate f_t, which is much higher than the Nyquist rate (f_t is generally 32k bits/s). Note that because of the much higher sampling rate, input filtering requirements are again considerably eased. Contents of the parallel register, representing LPCM words at a high sampling rate, are processed in a digital low-pass filter to restrict bandwidth to W Hz before being resampled at PCM sampling rate (f_r). PCM filtering of Fig 1 is, therefore, done digitally in this approach. The ADM bit rate required for generating PCM words of 13-bit accuracy is about 256k bits/s, considerably less than the clock rate indicated in Eq (9).

Digital Interpolation

Clock rate in ADM is reduced by varying step sizes, but this entails extra complexity in the analog circuitry, such as a digital-to-analog converter in the feedback loop. However, it is also possible to reduce the clock rate entirely by digital interpolation techniques.[7,11,12]

Fig 6 shows a DM-to-PCM converter using interpolation techniques. The linear delta modulator differs from that shown in Fig 2 in that the integrator is now in the forward path of the loop and not in the feedback path. This type of delta modulator is referred to as sigma-delta modulator (Σ-DM).[13] Characteristics of Σ-DM differ significantly from those of the DM shown in Fig 2. For Σ-DM, input y(t) is the average of coder output (q_n), and not its integral as in Fig 2. This important difference is illustrated in Fig 7. Another difference is that the Σ-DM does not suffer slope overload, unlike the DM in Fig 2, but limits when input amplitude is high.

The reason for using this type of modulator is that the digital network used as an interpolator after the modulator (Fig 6) has a nonrecursive low-pass filter structure, which has an output that is the average of its input in the passband. Filter coefficients (g_o, g_i, . . . , g_n) are chosen to define frequency response in the passband and for maximum out-of-band noise rejection.

To understand how use of digital interpolation permits a reduction in speed of operation of the Σ-DM, consider the DM of Fig 2. Assume that input changes from minimum to maximum during one PCM sampling interval ($1/f_r$). The output must produce 2^{13} 1s during this interval; this dictates the speed of operation to be 64M bits/s, Eq (9). Now, assume that the Σ-DM is operating at 8M bits/s; for the same input condition, it will produce 2^{10} 1s. Let the output be processed in a digital interpolation circuit (Fig 8) (this circuit can be realized, as shown in Fig 6, by suitable choice of filter coefficients). Notice that even though the Σ-DM is producing 2^{10} 1s, the digital interpolator is averaging 2^{13} 1s during one clock interval, thereby increasing accuracy of the coding process.

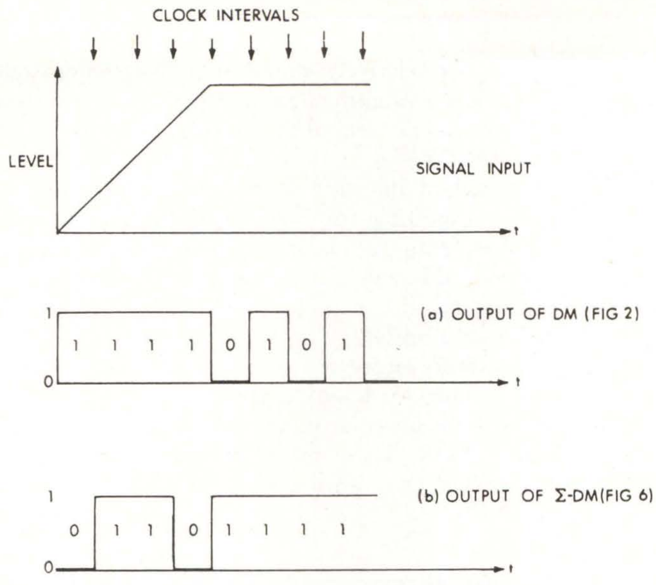

Fig 7 Difference between DM and Σ-DM. Sigma delta modulator (Σ-DM) used with interpolation filter differs from delta modulator shown in Fig 2. In Fig 7(a) for DM, input is integral of output. In Fig 7(b), for Σ-DM, input is average of output

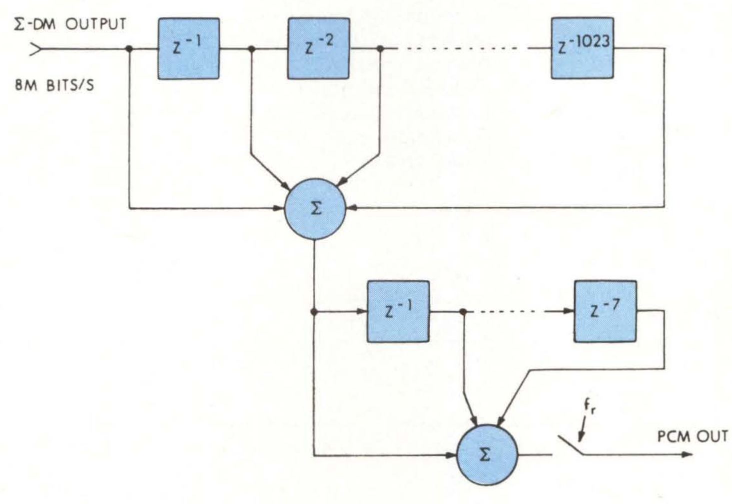

Fig 8 Digital interpolation. By reducing speed of operation of DM, digital interpolation improves resolution of output samples. During sampling interval, Σ-DM produces 2^{10} bits, but digital interpolator averages 2^{18} bits to produce output

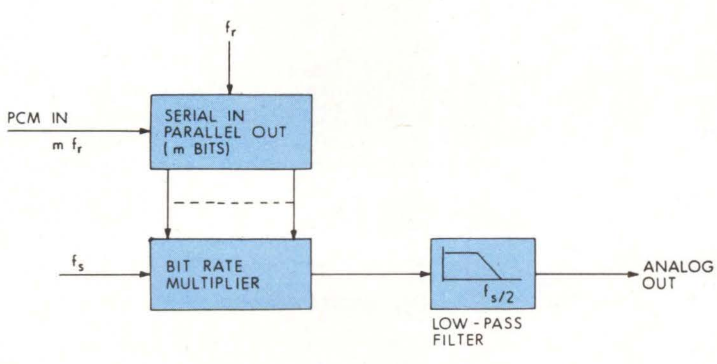

Fig 9 Simple PCM-to-DM converter. This converter uses bit-rate multiplier (BRM), in which low-pass filter converts BRM output into analog form. Clock rate is $2^m f_r$, and is usually high value

This explanation is an oversimplification of principles involved, but gives an insight into the digital interpolation process. Interpolator output is actually sampled at a rate f_t (32k words/s), and is further processed in a digital filter to restrict the bandwidth to W Hz before being resampled at a PCM rate of f_r. Clock rate required for this type of modulator is about 4M bits/s.

LPCM-To-DM Conversion

In a digital transmission system based on DM-to-PCM conversion at the transmitter, it is desirable to perform the reverse process at the receiver and to convert PCM to DM, for relatively simple digital-to-analog conversion. The most straightforward method for converting LPCM to DM is the use of a bit-rate multiplier (BRM), as shown in Fig 9.

Output of the BRM at bit rate f_s (operating speed of the transmitting DM) is passed through a simple low-pass filter to recover the original analog signal. This method, although simple, requires an extremely high operating speed, as given in Eq (9), and is, therefore, not always useful.

However, processes used for reducing speed of operation for DM-to-PCM conversion may be used in reverse to achieve a slower speed in PCM-to-DM conversion as well. These methods involve an initial stepping up of the PCM word rate from the Nyquist rate (f_r)

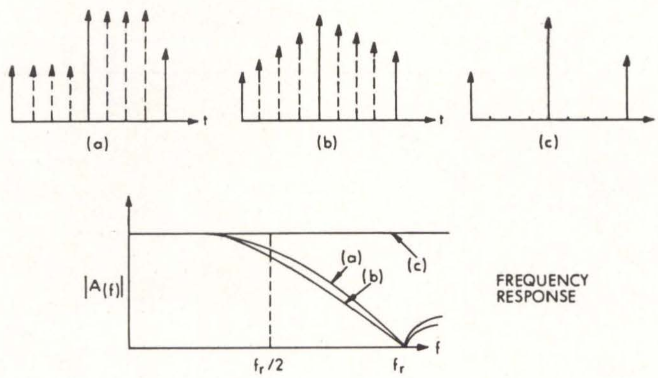

Fig 10 Increasing the sampling rate. Three methods for increasing sampling rate (f_r) to nf_r are: (a) repeat each sample (n-1) times, (b) use linear interpolation between samples, and (c) introduce n-1 zero-valued samples between successive samples. Methods (a) and (b) exhibit frequency distortion at the output, while method (c) does not

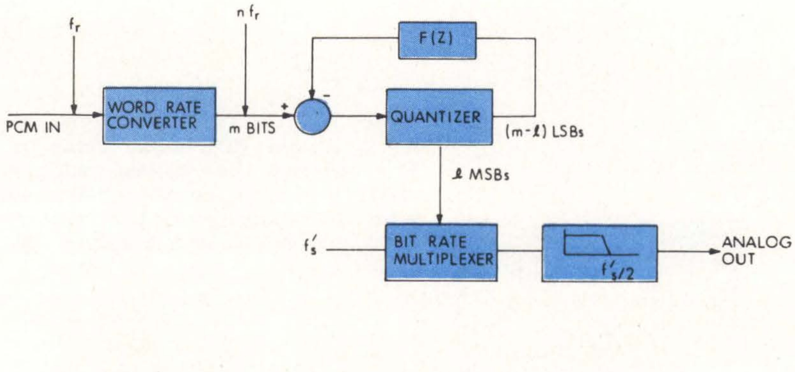

Fig 11 PCM-to-DM noise feedback. Using noise feedback in PCM-to-DM converter reduces required speed of operation of bit-rate multiplier. For example, *l* MSBs of m-bit PCM words are used in the BRM, and m-*l* LSBs are fed back to input through feedback network

to a higher sampling rate (nf_r). Fig 10 shows three different methods of achieving the higher sampling rate.

Repeating each original sample n times [Fig 10(a)] results in an output frequency response given by

$$\left| H(f) \right| = \left| \frac{\sin \pi f/f_r}{\pi f/f_r} \right| \tag{11}$$

Straight-line interpolation between successive samples [Fig 10(b)] shows a response of

$$\left| H(f) \right| = \left| \frac{\sin \pi f/f_r}{\pi f/f_r} \right|^2 \tag{12}$$

These responses may sometimes be unsatisfactory, and to obtain distortionless increases in sampling rate, it is necessary to insert (n − 1) zero-valued samples between the original samples, and to process the sequence in a suitably designed digital filter operating at a word rate of nf_r [Fig 10(c)].[14]

A useful technique for PCM-to-DM conversion is shown in Fig 11. The LPCM, with word rate stepped up to nf_r, is quantized to l bits, which is less than the PCM word length of m bits. Without the feedback arrangement, spectral density of quantization noise at the quantizer output is given by

$$q(f) = \left[\frac{V}{2^l}\right]^2 \times \frac{2}{3nf_r},\ f \leq nf_r/2 \tag{13}$$

where V = peak analog signal amplitude.
With the feedback shown, however, noise spectrum is modified to[15]

$$n(f) = (1 - F^{(j2\pi f/nf_r)})^2\, q(f) \tag{14}$$

By suitable choice of feedback network F(z), it is possible to have an acceptable passband noise performance even though input to the BRM is only l bits (less than the LPCM word length). This allows the BRM to operate at a bit rate much less than that indicated in Fig 9. Bit rate required for 13-bit PCM quality is about 4M bits/s.

Summary

Two alternative designs for converting a delta modulation bit stream to PCM format have been discussed. Both are aimed at reducing the rather excessive speed requirement for the straightforward conversion method. One approach is based on instantaneous adaptive delta modulation and uses an analog digital-to-analog converter. The other method uses digital interpolation, and employs entirely digital techniques. Both methods are equally suitable for integration onto a large-scale integration chip. Digital techniques for the reverse process of DM-to-PCM conversion have also been presented.

Speed of operation of these DM-to-PCM coders has been dictated by the requirement that their performance should match that of 13-bit linear PCM. The rather exacting specifications for 13-bit PCM quality originated from the needs of long haul, tandem transmission systems, where each link might involve several analog-to-digital and digital-to-analog conversions of the same analog signal. As both national and international networks become more digitally oriented, the number of such conversions per link should decrease. Also, several independent sources have reported experimental results that DM, operating at much less speed than indicated herein, gives adequate subjective performance.[1, 16] It may therefore be possible to reduce, in the not too distant future, hardware complexity for delta modulator and DM-to-PCM conversion by considerably reducing speed of operation.

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A graduate of Calcutta University, India, and London University, UK, S. Ghosh is presently employed with TRW Vidar as a project engineer. He has been involved primarily with design and development of digital communication systems: PCM channel banks, line repeaters, digital switching, and asynchronous multiplexers.

DESIGN NOTE

Interval Timer Serves As a Baud Rate Generator

With onchip, independent, multimode counters, a programmable interval timer can be configured to supply software selectable baud rates for peripherals or to overcome microcomputer timing problems

John Beaston Intel Corporation, Santa Clara, California

Many microcomputer systems utilize some form of serial communication to provide an inexpensive interface to peripherals such as cathode-ray tubes, printers, and keyboards. The interface is generally implemented using universal synchronous/asynchronous receiver/transmitters. Since different peripherals require different serial data or baud rates, these units are provided with receiver and transmitter clock inputs. Until recently, generating baud rate clocks involved the use of either a dedicated, fixed frequency oscillator if only a single baud rate was needed, or the use of programmable divide-by-N transistor-transistor logic counters to count down the processor clock if multiple speed selection was required.

Speed selection inflexibility and high parts count disadvantages usually associated with these methods have been overcome with large-scale integration (LSI). Special purpose, dedicated function baud rate generators (BRGs), such as the Fairchild F4702, SMC COM5016/5017, or Motorola MC14411, are now available. These BRGs provide either multiple, simultaneous outputs (MC14411) or a single output that is programmed via rate select inputs. Another more flexible option available is the programmable interval timer; the Motorola MC6840, Zilog CTC, and Intel 8253 are members of this group. These interval timers usually provide one to three independent, multimode counters onchip to solve a common microcomputer system problem—the generation of accurate time intervals under software control. In addition to implementing BRGs, these counters offer flexibility for use as complex motor controllers, realtime clocks, function generators, or event counters.

Functional Principles

Intel's 8253 contains three independent 16-bit counters—C0, C1, and C2 [Fig 1(a)]. Each counter operates as a presettable downcounter capable of either binary or binary coded decimal (BCD) counting. Six programmable modes are available: (a) output on terminal count (mode 0); (b) programmable one-shot (mode 1); (c) rate generator, divide-by-N (mode 2); (d) square wave generator (mode 3); (e) software triggered strobe (mode 4); and (f) hardware triggered strobe (mode 5). Since the counters are independent, any combination of modes may be used with each counter. Additionally,

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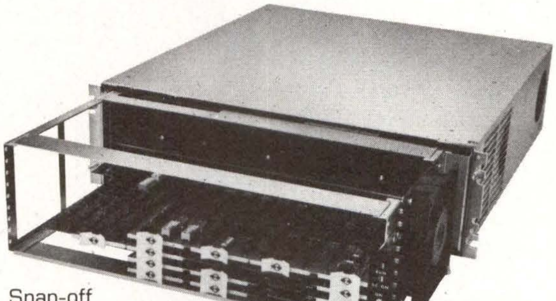

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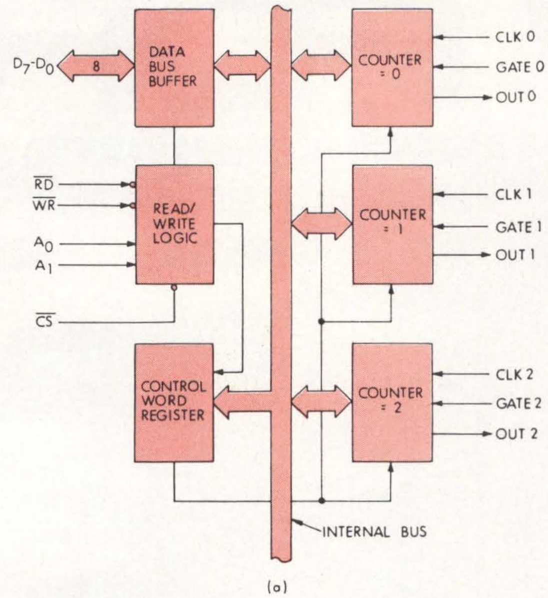


$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	LOAD COUNTER 0
0	1	0	0	1	LOAD COUNTER 1
0	1	0	1	0	LOAD COUNTER 2
0	1	0	1	1	WRITE CONTROL WORD
0	0	1	0	0	READ COUNTER 0
0	0	1	0	1	READ COUNTER 1
0	0	1	1	0	READ COUNTER 2
0	0	1	1	1	NO-OPERATION 3-STATE
1	X	X	X	X	DISABLE 3-STATE
0	1	1	X	X	NO-OPERATION 3-STATE

(b)

Fig 1(b) Control word and counter decoding formats. Each 8253 counter contains Load/Read register for count values. Common Control register is used to define each counter's mode and counting format

Fig 1(a) Block diagram of programmable interval timer. 8253 contains three independent, presettable, downcounters. Each counter has own input (CLK), gate (GATE), and output (OUT) controls. Remaining pins form traditional microprocessor bus structure

the current residual value of each counter may be read repeatedly by reading the count register.

In Fig 1(a), the clock, gate, and output lines provide a separate control for each counter. Their functions vary depending on the mode. However, in general, CLK supplies the events to be counted or serves as the basic time unit; GATE either inhibits or enables counting; and OUT indicates terminal count or supplies the divided CLK output. The remaining pins serve the standard microprocessor system bus. Each counter is addressed by decoding the A0 and A1 pins. Fig 1(b) lists pin conditions required to select various internal registers, depending on the operation desired.

Operation of each counter is controlled by programming a control word followed by loading the count register of the desired counter. The control word specifies the counter number, the reading or loading of the internal count register, mode selection, and counting format (binary or BCD), as shown in Table 1. Using a common control register saves valuable chip area plus reduces the I/O space required by the device.

TABLE 1

Control Word

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC Field

SC1	SC0	Functions
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL Field

RL1	RL0	Functions
0	0	Latch counter value
1	0	Read/load MSB only
0	1	Read/load LSB only
1	1	Read/load LSB first, then MSB

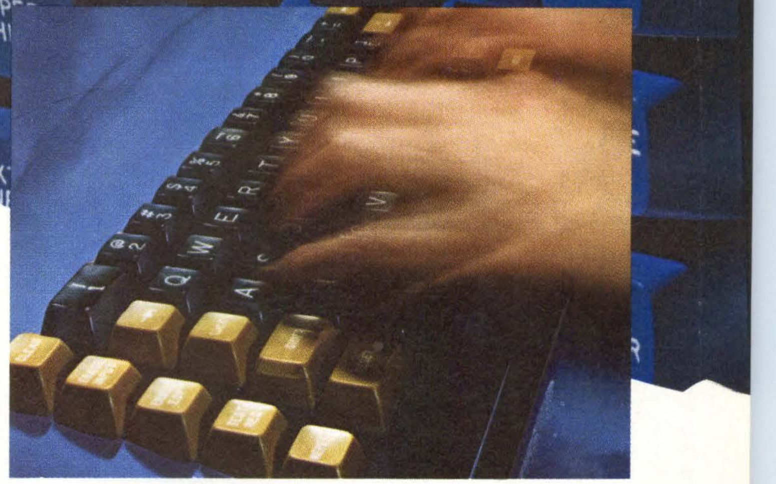
M Field

M2	M1	M0	Functions
0	0	0	Mode 0
0	0	1	Mode 1
X*	1	0	Mode 2
X*	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD Bit

BCD	Functions
0	Binary 16-bit counting
1	BCD counting (4 decades)

*X: "don't care"



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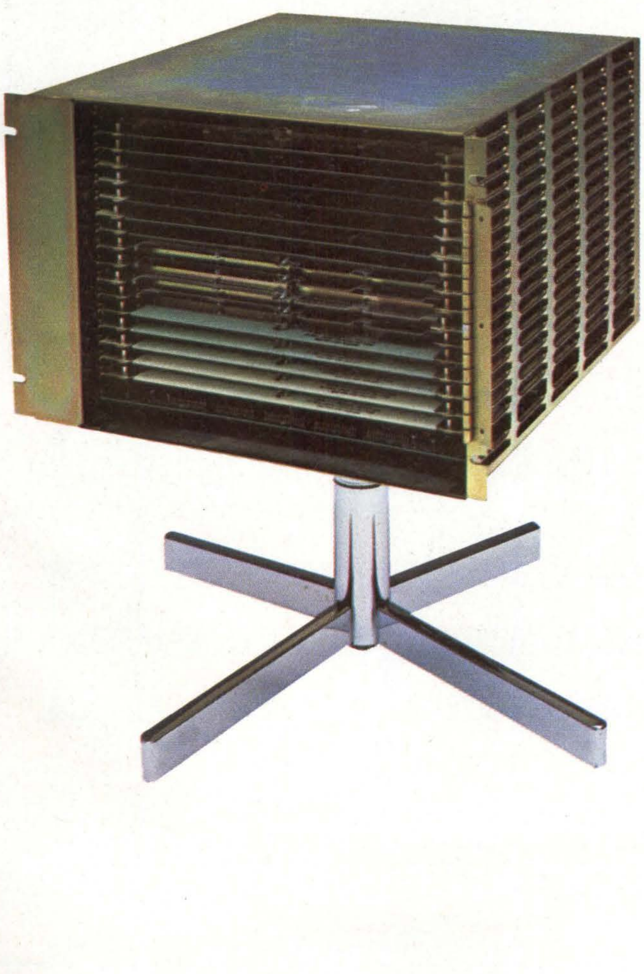

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For the BRG application, consider the system shown in Fig 2. This typical configuration comprises an 8085 processor, an 8251A universal synchronous/asynchronous receiver/transmitter (USART), and an 8253 interval timer implementing a serial communications channel. The USART baud rate clocks are supplied by counter 0 of the 8253. (Choice of counter 0 is arbitrary; any counter could be used.) To obtain accurate baud rate clocks, the CLK 0 input of the 8253 is driven with a 1.536-MHz source. This signal may be derived by several methods. However, one convenient method is to use a 6.144-MHz crystal for the 8085 and to divide the CLK output (3.072 MHz) of the 8085 by two with a 7473 flip-flop (Fig 2); the maximum 8253 CLK input frequency is approximately 2.6 MHz. The GATE 0 input (8253) is held high (5 V) since baud rate generation requires no gating, and OUT 0 (8253) directly drives the receiver and transmitter clock inputs, RXC and TXC respectively, to the 8251A. The remaining two counters (C1 and C2) of the 8253 are available to the system designer for implementing other timing or counting functions.

Software Principles

The software required to implement counter 0 as a baud rate generator is listed below. First, the control word is written to the 8253. Bits SC1 (D7) and SC0 (D6) of the control word (Table 1) select counter 0 (SC0 and SC1 = 0). Bits RL1 (D5) and RL0 (D4) specify that the count register is loaded first with the least significant byte, followed by the most significant byte (RL0 and RL1 = 1). Bits M2 (D3), M1 (D2), and M0 (D1) denote that Mode 3 is used; M1 and M0 = 1 and M2 = "don't care" (X). USARTs normally require square waves for data clocks. Bit BCD (D0) is set to zero to indicate that the count register data are binary. The input/output (I/O) port address is such that CS = 0, A0 = 1, and A1 = 1 [Fig 1(a)], to obtain write control word as follows:

TABLE 2

Baud Rate Divisors at 1.536 MHz

USART Mode	Baud Rate	TXC RXC (Hz)	Divisor at 1.536 MHz Decimal	MSB_{16}	LSB_{16}
	50	800	1920	07	80
	110	1760	873	03	69
	150	2400	640	02	80
X16	300	4800	320	01	40
Async	600	9600	160	00	A0
	1200	19.2k	80	00	50
	2400	38.4k	40	00	28
	4800	76.8k	20	00	14
	9600	153.6k	10	00	0A
	50	3200	480	01	E0
	110	7040	218	00	DA
X64	150	9600	160	00	A0
Async	300	19.2k	80	00	50
	600	38.4k	40	00	28
	1200	76.8k	20	00	14
	2400	153.6k	10	00	0A
	300	300	5120	14	00
	600	600	2560	0A	00
	1200	1200	1280	05	00
X1	2400	2400	640	02	80
Sync	4800	4800	320	01	40
	9600	9600	160	00	A0
	19.2k	19.2k	80	00	50
	38.4k	38.4k	40	00	28
	56k	56k	27	00	1B

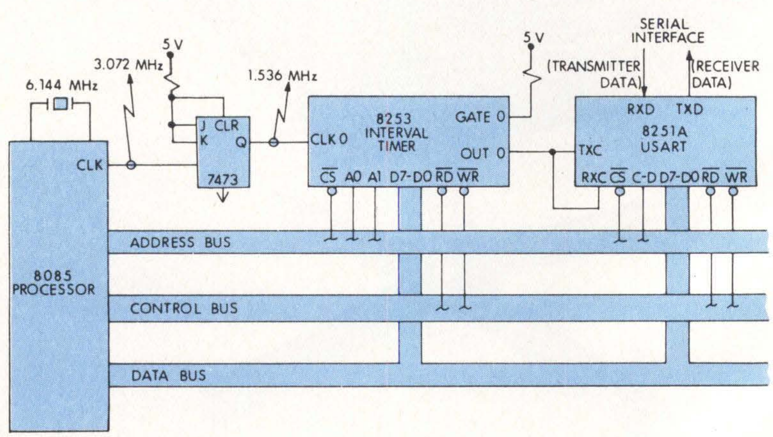

Fig 2 System block diagram. 8253 allows this serial communications channel to operate at any of common baud rates under software control

```
MVI  A, 36H   ;move control word
              to A register
OUT  83H      ;output control word
              to control register
```

After the control word is entered, the count register needs both bytes of the divisor, the least significant bit (LSB) and the most significant bit (MSB). Therefore, $\overline{CS}$, A1, and A0 are selected to load counter 0 [Fig 1(b)] as follows:

```
MVI  A, LSB   ;move divisor LSB to
              A register
OUT  80H      ;output LSB to coun-
              ter 0 count register
MVI  A, MSB   ;move divisor MSB to
              A register
OUT  80H      ;output MSB to coun-
              ter 0 count register
```

Table 2 shows the divisor (LSB and MSB) for various baud rates and USART modes, assuming the 1.536-MHz clock input. After both bytes of the count register are loaded, counter 0 starts generating the selected baud rate. The baud rate may be changed at any time during the main program by simply repeating the above procedure with a different divisor.

Summary

Baud rate generators can be implemented using either fixed frequency or programmable transistor-transistor logic (TTL) oscillators; however, their flexibility and versatility are limited due to their dedicated function. As a better solution, programmable interval timers offer software selectable baud rates and multiple simultaneous outputs if more than one counter is used. If only one counter is needed, the remaining counters are free to solve other system timing or counting problems. While the maximum frequency of the timers may not be sufficient for some counting applications, such as frequency counting above 3 to 4 MHz, they make up for this disadvantage in flexibility and convenience.

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(12-20). Being Organized

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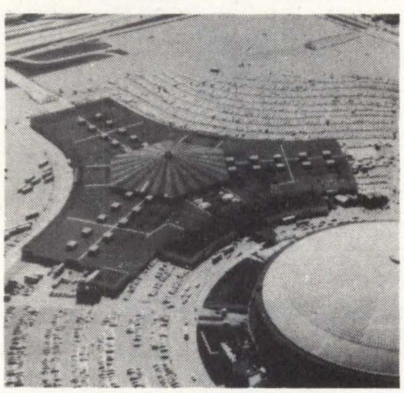

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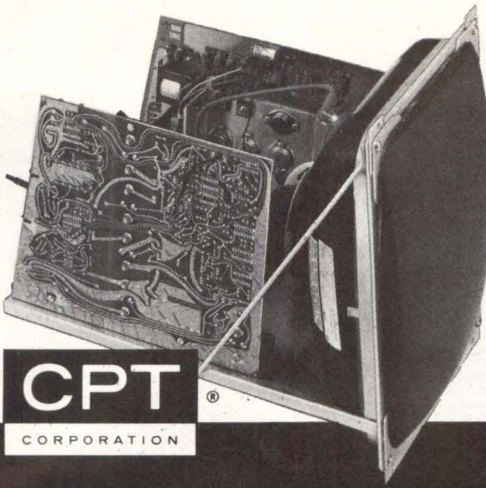
CIRCLE 52 ON INQUIRY CARD →



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This is an un-retouched photo of the new CPT HRD-15 Model S, black-on-white high resolution, high density raster display. As a result of faster scanning speeds and faster rise/fall rates, it gives you this unique clarity and high density. The "smear" at the edge of the dot is eliminated. The dot has more edge contrast, better definition. Developed to look as much as possible like the typewritten page, the CPT HRD-15 is human engineered for daily use without eyestrain.

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INTERFACING FUNDAMENTALS: THE 8085 FAMILY OF MEMORY DEVICES

Christopher Titus and Jonathan A. Titus
Tychon, Inc

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University

One advantage obtained from using the Intel 8085 microprocessor chip, an upgraded 8080-type device described last month (*Computer Design,* July 1978, p 114), is the availability of "family" devices that may be used with little or no additional external logic. Thus, the 8085 microprocessor and its family of devices are suitable for small controllers, instruments, and games, where expansion and the ability to run large programs such as BASIC may not be required.

Two of the 8085 family devices are the 8155 read/write (R/W) memory chip and the 8355/8755 read-only memory (ROM) device. Pin configurations and block diagrams for each are shown in Figs 1 and 2. The 8355 and 8755 ROM devices are equivalent, as far as the user is

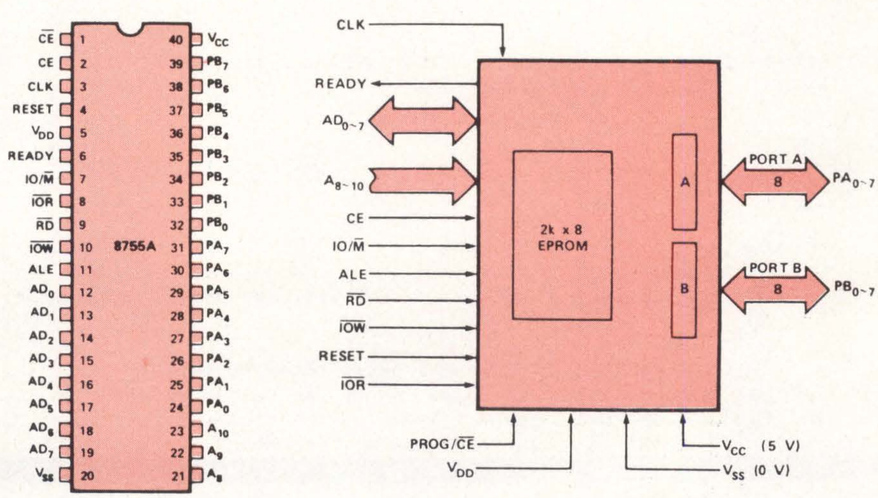

Fig 1 Block diagram and pin configuration for 8755 ROM used in 8085 based system

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CIRCLE 53 ON INQUIRY CARD

Whose whose in LSI-11 memories?

Strand Century, Inc.
Los Angeles, California

The company:
The leading manufacturer of memory light control systems for theatrical productions and TV shows.

Notable application:
Lighting controls for the Broadway hit "Annie." (Photo 1, courtesy Martha Swope.)

Whose CPU:
Digital Equipment Corporation LSI-11

Whose memory:
Monolithic Systems Corporation MSC 4601 Dual Height

Whose decision:
David Cunningham, Director Research and Development

Comment:
"We've been buying both quad and dual height memories from Monolithic Systems for several years. The outstanding cooperation of their people and their on-time deliveries were major factors in selecting them."

American Sign & Indicator Corporation
Spokane, Washington

The company:
The world's largest supplier of computer directed lighted signs, scoreboards and color displays.

Notable application:
Mark 400 Spectacolor Display on Times Square (Photo 2, courtesy American Sign & Indicator Corporation.)

Whose CPU:
Digital Equipment Corporation LSI-11

2.


3.

Whose memory:
Monolithic Systems Corporation MSC 4601 Dual Height

Whose decision:
David Cole, Director of Materials

Comment:
"Our displays have used Monolithic Systems' LSI-11 memories exclusively since 1976. Cost and delivery were the primary reasons for changing vendors and Monolithic's new dual height version has kept us convinced we made the right choice."

EG & G Princeton Applied Research Corporation
Princeton, New Jersey

The company:
The leading manufacturer of signal recovery instrumentation and pioneer in multichannel electro-optical detection techniques.

Notable application:
The OMA-2 Optical Multichannel Analyzer (Photo 3) permits real-time spectral analysis from below 200 nanometers to nearly 2.0 micrometers. RAM memory is used for storage of the scan format.

Whose CPU:
Digital Equipment Corporation LSI-11

Whose memory:
Monolithic Systems Corporation MSC 4501 Quad Board

Whose decision:
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Comment:
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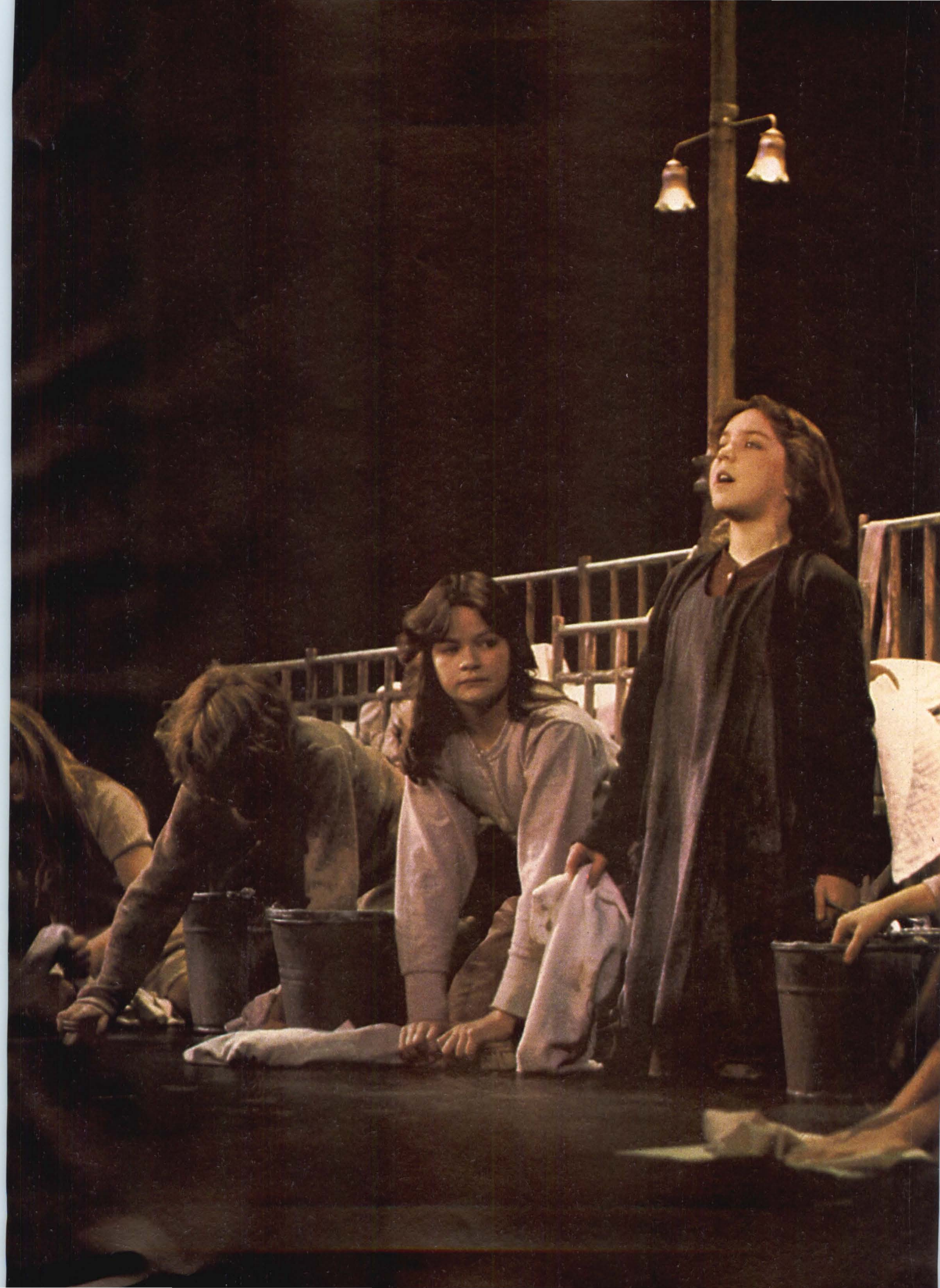
CIRCLE 54 ON INQUIRY CARD

1. (Right) A scene from "Annie." Presented by Mike Nichols. Winner of 7 Tony Awards–1977 –including Best Musical. Best Musical Award 1976-77, N.Y. Drama Critics' Circle. Produced by Irwin Meyer, Stephen R. Friedman and Lewis Allen.

2. (Left top) World's largest computer controlled Spectacolor display at the nation's number one sign location, Times Square in New York City. Eighty-two hundred lamps enable the extraordinary system to perform cartoon like animation in up to 17 different colors.

3. (Left bottom) Just as the human eye detects the variations in the visible light spectrum, the OMA-2 provides a real-time readout of wavelengths and intensities of this spectrum. Suitable detectors allow OMA-2 to "see" into the ultraviolet and infrared regions as well.



concerned: the 8355 is mask-programmed, while the 8755 may be erased and reprogrammed much like the 1702A and 2708 EPROMs. The 8755 contains 2048 (2k) bytes of ROM that may be accessed by using 11 address bits and 2 chip enable inputs, CE and $\overline{CE}$. These two control inputs must be at logic 1 and 0, respectively, for the memory to be accessed. Since the 8755 belongs to the 8085 family, the low address and data bus signals are multiplexed on the bidirectional address/data bus lines, AD7 to AD0. As such, the 8755 is not very exciting. However, it does contain two 8-bit input/output (I/O) ports, allowing a great deal of flexibility.

I/O ports on both ROMs may be programmed on a bit by bit basis so that individual bits may be for either input or output. This allows the user to select any combination of I/O bits, from 16 inputs to 16 outputs. Each of the two I/O ports on the ROM chip has a control register to facilitate bit programming. To make our system simpler to understand, we have chosen to use the accumulator I/O technique to interface the two I/O ports on the ROM chip to the 8085. The necessary microprocessor control signals are gated together to generate the $\overline{IN}$ and $\overline{OUT}$ required for I/O control. These signals are applied to the ROM chip's $\overline{IOR}$ and $\overline{IOW}$ pins. Device addresses for the I/O ports and their control registers are

Port A	XXXXXX00
Port B	XXXXXX01
Port A Control Register	XXXXXX10
Port B Control Register	XXXXXX11

The X represents "don't care" bits, since their states do not have to be known to select one of the four functions. This flexibility is possible since the chip is also controlled with the CE and $\overline{CE}$ inputs; these two inputs must be in their proper states before the chip can operate on the ports or port control registers. The contents of neither control register can be read; they can only be updated, not checked.

In this small 8085 system, the chips have been configured so that the ROM in the 8355 or 8755 starts at address 000 000 and continues through address 007 377. The I/O ports have addresses 001 and 002, with the control registers having addresses 002 and 003. The final system does not have absolute addressing, since some of the unused address bits are ignored. More decoding is necessary in order to expand the system.

The 8155 chip contains 256 bytes of R/W memory, which is probably more than enough for a small system. In most cases, it is used for temporary storage of data or results, as well as register and address information. The 8155 is bus compatible with the 8085 system through the use of the bidirectional address data bus and stan-

Bit Designations and Functions For Programming 8155 Control Register

Bit	Function	
D0	Defines Port A	Logic 1 = Input, Logic 0 = Output
D1	Defines Port B	
D2	Defines Port C	Four modes possible
D3	Defines Port C	
D4	Port A Interrupt Enable	
D5	Port B Interrupt Enable	
D6	Timer Control	
D7	Timer Control	

D7	D6	— Timer Control Bits
0	0	No effect upon counter
0	1	Stop counting
1	0	Stop after this count has been completed
1	1	Load counter and start counting. If counter is running, load and restart after current count has finished

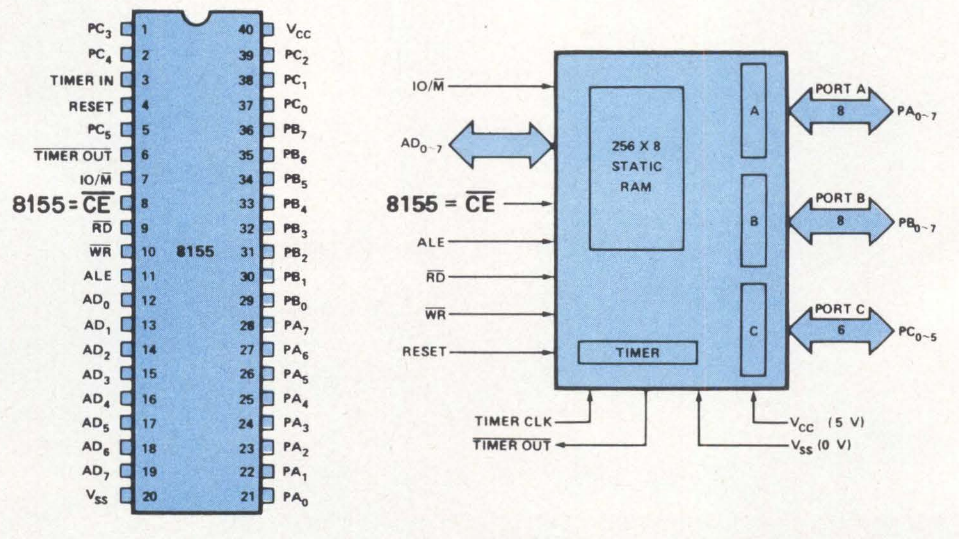


Fig 2 Block diagram and pin configuration of 8155 R/W memory for use in 8085 based system

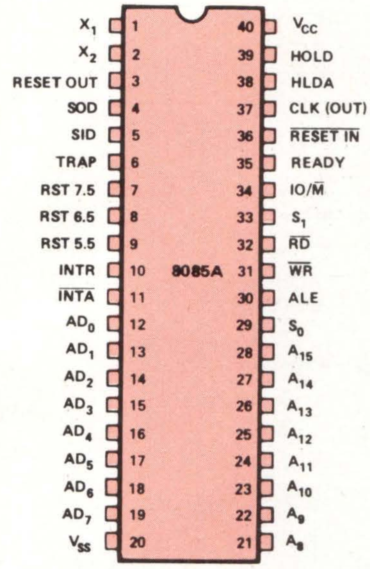


Fig 3 Pin configuration of 8085 CPU or microprocessor chip

dard control signals. In this case, only the IO/$\overline{\text{M}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ signals are needed for memory control. ALE, CLOCK, and RESET signals from the microprocessor are provided for internal control of the chip. Fig 3 gives the pin configuration for the 8085 microprocessor chip.

Like the ROM chips, the R/W chip has some I/O lines. In fact, there are two 8-bit I/O ports, A and B, and one 6-bit I/O port, C. Ports A and B may be operated in input or output mode; however, individual bits cannot be selected, as was the case with the 8355/8755. Port C may be operated in a number of ways, but these are beyond our present discussion. Let it suffice to say that they allow the I/O ports to operate in a manner that is similar to that encountered in mode 1 and mode 2 operation of the 8255 programmable peripheral interface chip.

The R/W memory chip also contains a 14-bit programmable counter, referred to as a timer, which may use either the microprocessor's clock output or an externally applied clock signal. The timer's output is available as a pin on the memory chip, and may be used in a number of ways, depending upon the situation. It could be connected to the serial input data pin (SID pin 5), so that it could be sensed by the RIM instruction; or it could be connected to one of the microprocessor's interrupt pins, RST 7.5, for example, so that the end of the timer's period could be detected through an interrupt action. The timer's output is fairly flexible, being programmed to operate in one of four ways.

CIRCLE 55 ON INQUIRY CARD

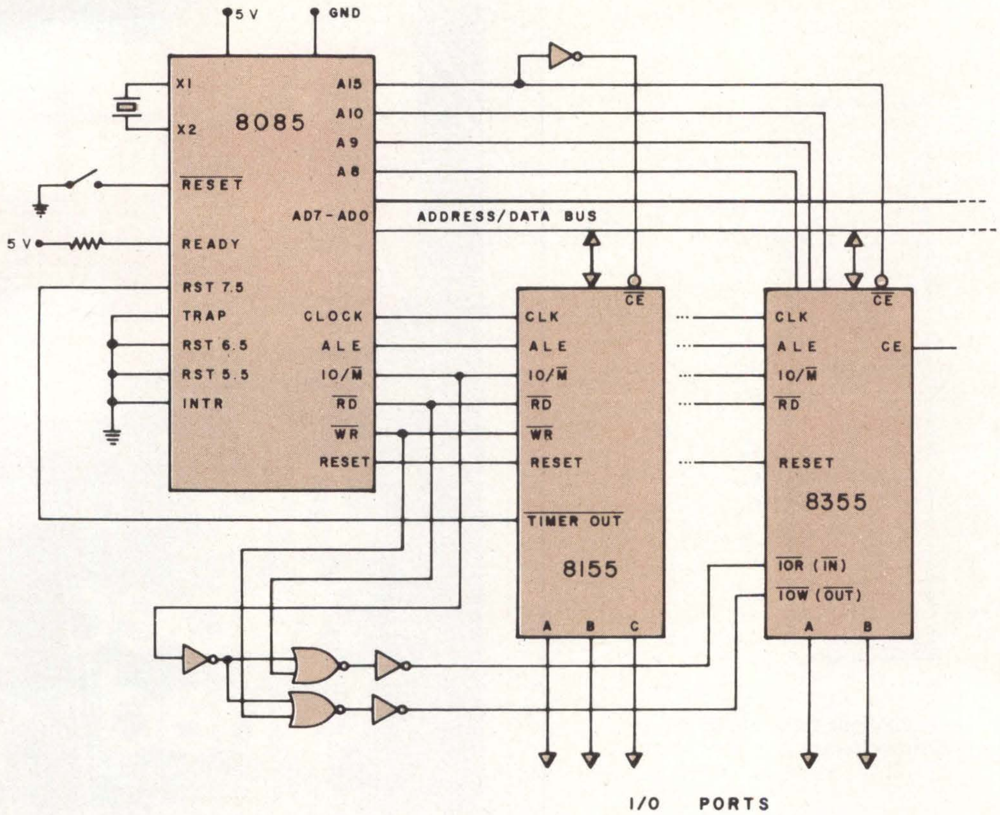


Fig 4 Minimum configuration using 8085 CPU, 8155 RAM, and 8355 ROM chips to perform control and memory functions

M2	M1	Mode of Operation
0	0	Output a logic 0 during second half of count
0	1	Output a square wave, same as 00 above, but reload and restart count at end of each count sequence
1	0	Output a single, short pulse at end of count sequence
1	1	Output a single pulse at end of count, but reload and restart count at end of each count sequence

Control bits M2 and M1 are the most significant bits in the 16-bit count value programmed into the counter. Since the counter is only 14 bits long, the control bits are not included in the count itself; instead, they are used by the counter's control logic to determine the state of the counter's output when the count has been finally decremented to 0. Whenever a new 14-bit count value is reprogrammed into the counter, these two control bits must also be included in the new 16-bit word.

An internal control register in the R/W memory chip is loaded with an 8-bit byte that is used to determine the operation of the I/O ports and 14-bit counter. The various control register bits and their function are shown in the Listing of Bit Designations and Functions.

Six device addresses are associated with the 8155 in an 8085 based system. They control the I/O ports, timer, and control register. The control register's address may be used in a read operation to read various conditions or status bits. Individual addresses and their functions are:

Command/Status Register	XXXXX000
Port A	XXXXX001
Port B	XXXXX010
Port C	XXXXX011
Counter Bits D7 to D0	XXXXX100
Counter Bits D13 to D8 and Counter	XXXXX101

In this 8085 based system, these devices have addresses 200 through 205. The 8155's $\overline{CE}$ input must be at logic 0 for the memory or I/O devices to operate properly. The configuration of our final, minimum system is shown in Fig 4. Two additional integrated circuits—an SN7404 hex inverter and SN7402 quad NOR—are needed to provide gating and inverting functions. Note the use of address bit A15 to select between the 8155 and 8355 chips; the latter has been chosen as the system's ROM. Use of this system and development of some software examples that may be used in small control systems will be explored next month.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

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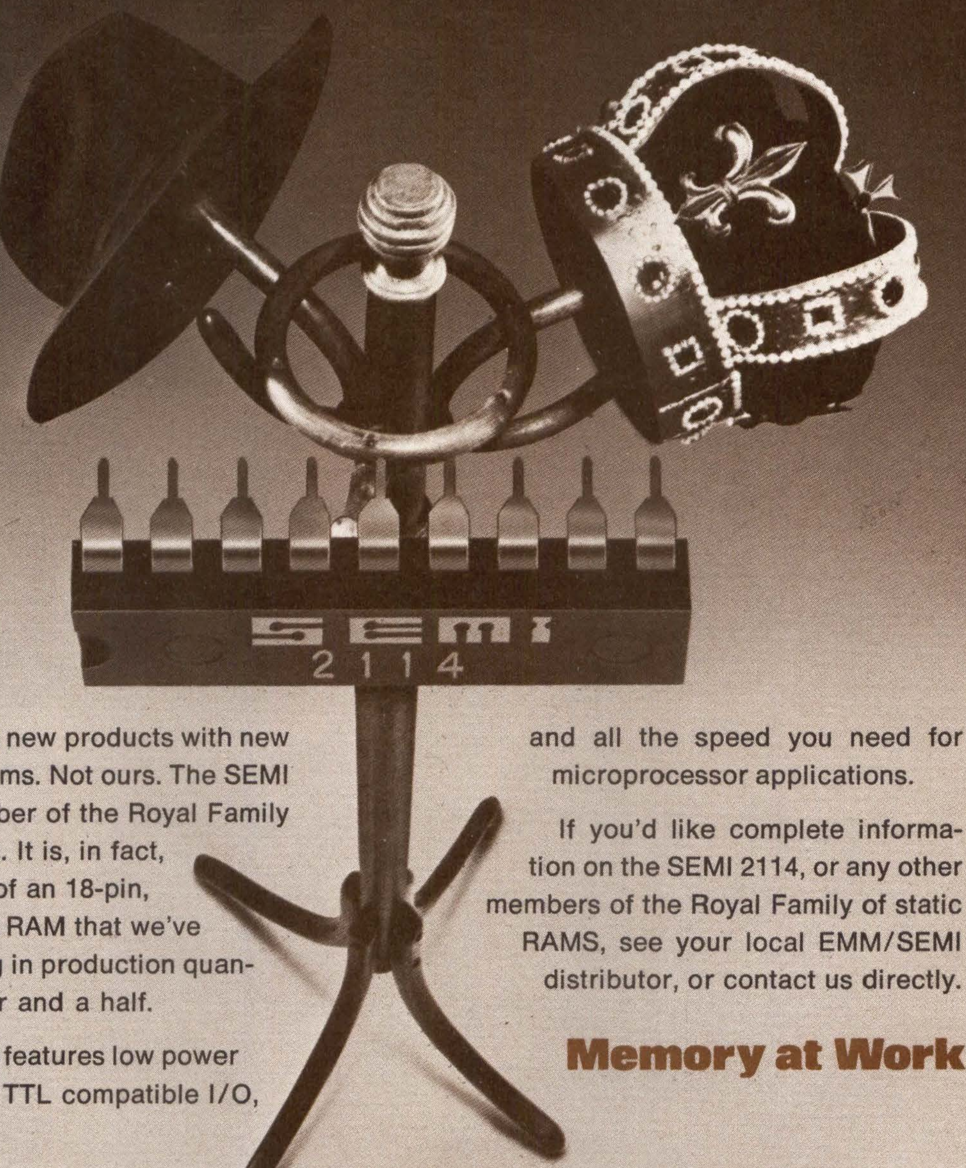

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CIRCLE 56 ON INQUIRY CARD

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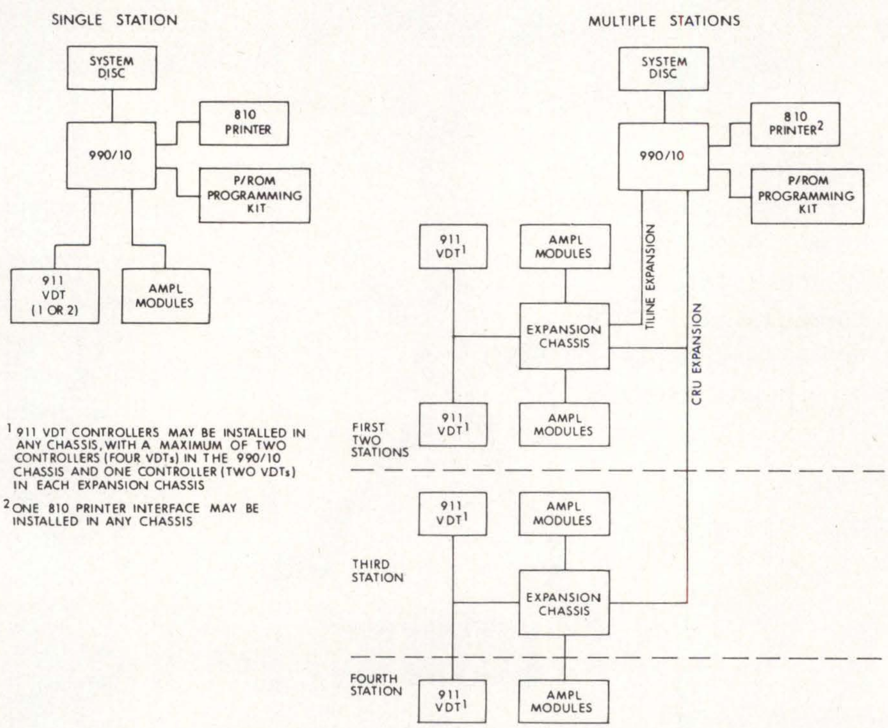

DS990-AMPL™ prototyping lab systems for Texas Instruments' 9900 family of microprocessors are based on DS990 model 4, 6, and 8 computer systems, together with one 810 printer, one expansion 911 VDT, and one AMPL station. Expansion chassis is required for two or more AMPL stations. System shown would support eight terminals, with any four of them controlling AMPL modules

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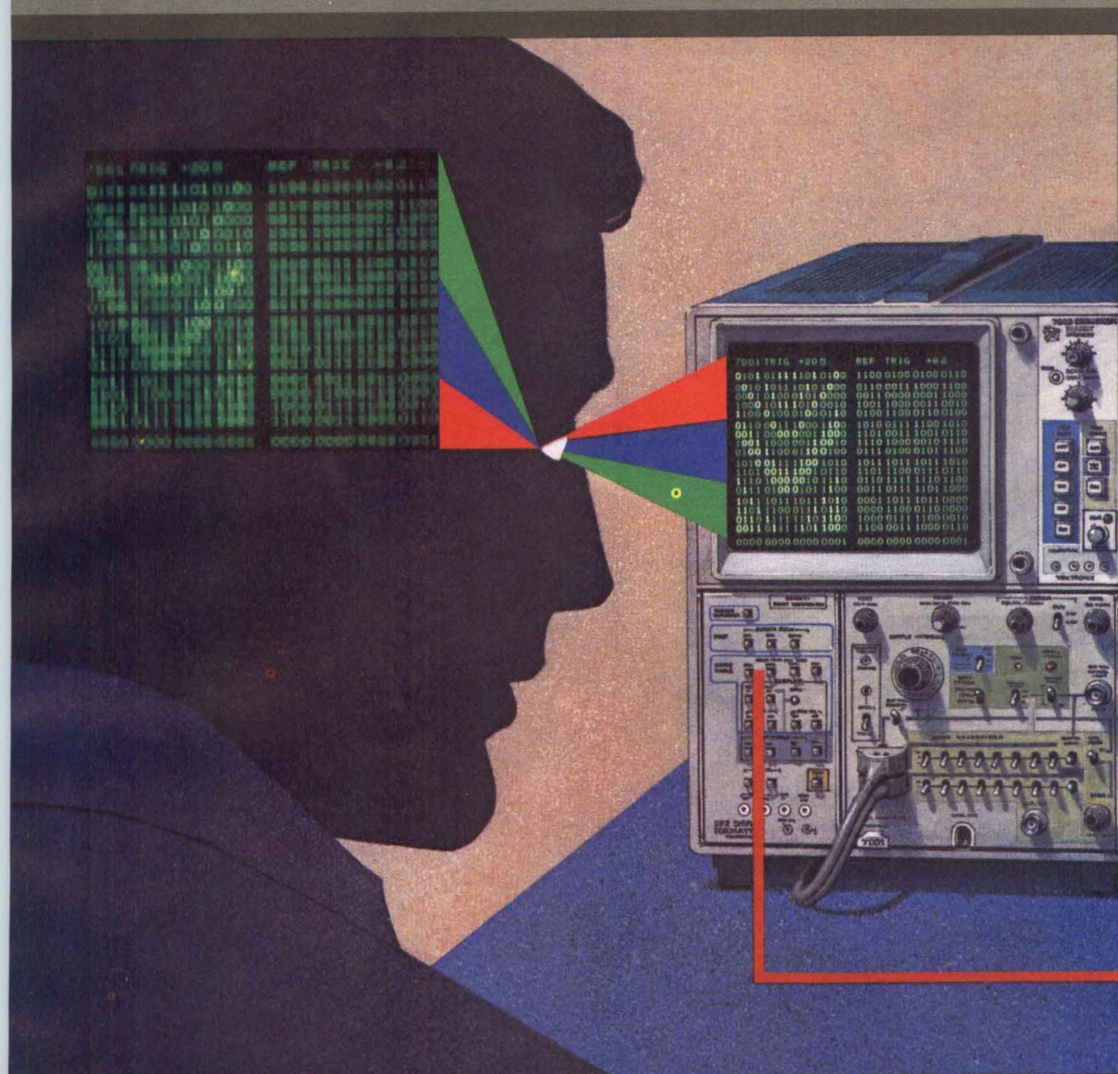

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And another nice thing is all the parts we support the 2901A with.

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Our family:

IDM2901A	4 Bit Microprocessor Slice
IDM2901A-1	Super 4 Bit Microprocessor Slice
IDM2902	Carry Look-Ahead Generator
IDM2909A	Microprogram
IDM2911A	Microprogram Sequencer
IDM29702	16 x 4 Bit RAM (Open Collector)
IDM29703	16 x 4 Bit RAM (Tri-State)
*IDM29704A	Fast 16 x 4 Bit RAM, 2-Port (Open Collector)
*IDM29705A	Fast 16 x 4 Bit RAM, 2-Port (Tri-State)
IDM29750	32 x 8 Bit PROM (Open Collector)
IDM29751	32 x 8 Bit PROM (Tri-state)
IDM29760	256 x 4 Bit PROM (Open Collector)
IDM29761	256 x 4 Bit PROM (Tri-state)
IDM29803	16 Way Branch Controller
IDM29811	Next Address Controller
IDM29901	Octal D-Type Flip Flop (Tri-State)
IDM29902	Priority Encoder
IDM29903	16 x 4 Edge-Triggered Register (Tri-State)
IDM29908	Quad Gated Flip Flop (Flag Control)

*Available soon.

Also, we supply a complete line of low-power Schottky MSI, MOS static and dynamic RAM's, as well as all the other parts you need to build a complete, high-performance processor.

So if you need to know who to go to for everything you need, now you know.

National Semiconductor
2900 Semiconductor Drive
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Gentlemen:

☐ Please send more information on your 2901A and its support products.

Name__________ Title__________

Company__________

Address__________

City__________ State__________ Zip__________

CD-8

National Semiconductor

and addition of peripherals is possible.

Texas Instruments, Inc, Digital Systems Group, PO Box 1444, Houston, TX 77001 has developed AMPL software as a high level prototyping language that controls debug functions and executes under the DX10 operating system. A 1-yr software update service is included with the system. A FORTRAN compiler is available as a DX10 option for more effective coding and program development. Other languages such as COBOL, BASIC, and Business BASIC allow applications of the DS990 systems to be extended beyond microprocessor development.

An emulator kit includes the TMS9900 emulator, TMS9900 or 9980 buffer, and the target system connector. Emulation support is available for the TMS990 and TMS9980A microprocessors; TMS9940, SBP9900, and TMS9981 are soon to be added. Expanding the emulator module's trace function which is dedicated to the microprocessor address bus, the logic state trace module is a general purpose logic analyzer on a single logic board. It is controlled by AMPL commands. A P/ROM programming kit permits the target system memory to be implemented in P/ROM or EPROM.

Circle 420 on Inquiry Card

Service Rents µProcessor Development Facilities To Small Businesses

Micro Development Lab is a short term, around the clock time rental service of microprocessor development and test equipment. W & B Instruments, Inc, Suite 103, 2483 Old Middlefield Way, Mountain View, CA 94043 has aimed the service at consultants and small businesses who may have equipment failures or temporary overloads.

For software development, the lab has disc operating systems with editors, resident assemblers, compilers, linkers, and loaders. Emulators, oscilloscopes, power supplies, and digital voltmeters perform hardware development and debugging. The 8080, 8085, 6800, and Z80 CPUs are currently handled by the service; support of others is planned.

When required, programs already started on floppy disc or paper tape may be converted to the appropriate system. In addition, microprocessor development training for both beginners and experienced users is being planned, as is software and hardware consulting.

Circle 421 on Inquiry Card

6802 Emulator Expands Support of Microprocessor Line

To support the Motorola 6800 series of microprocessors, Tektronix, PO Box 500, Beaverton, OR 97077 has begun development of a 6802 microprocessor emulator for the 8001 and 8002 microprocessor development labs. Users will then be able to take advantage of such capabilities as software development and debugging support, hardware and software integration, and realtime in-circuit emulation of a 6802 based prototype system (see *Computer Design*, Apr 1977, p 120). Inherent in the 6802 emulator system is support for the companion 6846, which together form a 2-chip microcomputer.

The development labs now support the Motorola 6800, Intel 8080A and 8085A, Texas Instruments TMS9900, and Zilog Z80 microprocessors. Also under development are emulators for the Mostek 3870/3872 microcomputers and Fairchild F8 microprocessors.

Circle 422 on Inquiry Card

Microprocessors Can Communicate Via Input/Output Modules

Four optically isolated modules protect sensitive microprocessor terminals while allowing them to receive inputs and control ac and dc power loads. Introduced by Motorola Semiconductor Products, Inc, PO Box 20912, Phoenix, AZ 85036, the units are color-coded and plug vertically into one of the company's I/O boards which interface with any system having CMOS, TTL, LS, NMOS, or PMOS logic.

Dc input module IDC5 translates 10- to 32-V input signals to MPU logic levels, while ac input module IAC5 does the same to 95- to 130-Vac stimuli. Both have a status indicator terminal for driving an LED in visual troubleshooting applications.

Dc output module ODC5 drives 3 A into a load, while withstanding up to 60 V across its output terminals. Ac output module OAC5 switches 3 A into a line load at voltages from 12 to 140 V rms with zero crossing, low noise internal triggering. All four modules withstand 1500-V transients between isolated terminals, and meet UL isolation requirements.

Circle 423 on Inquiry Card

PC Board Transformers Simplify Microprocessor DC Power Supply Design

The MP family of PC board transformers, specified in terms of dc output, allow users to design triple output regulated power supplies required in conjunction with microprocessor based devices and other logic/op amp circuits. The series includes single or dual primaries, with outputs for 5 and ±12 Vdc or 5 and ±15 Vdc from 5 to 25 VA. Signal Transformer Co, Inc, 500 Bayview Ave, Inwood, NY 11696 has also compiled data sheets listing auxiliary components for each rating. Both standard PC board types and low profile Flat Head™ models are available.

Circle 424 on Inquiry Card

Higher Speed Parts Are Introduced for S6800 µProcessor Family

The S6800 microprocessor family has been upgraded with devices that operate at up to twice the speeds of earlier versions, thus specifically suiting them to high speed microcomputer/controller applications. The additions include A and B versions of the S6800 microprocessor itself, the S6810 RAM, S6821 peripheral interface adapter (PIA), and S6850 asynchronous communications interface adapter (ACIA).

B versions of the microprocessor, PIA, and ACIA from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 operate at 2.0 MHz, while A versions operate at 1.5 MHz. The static RAM B version has a maximum access time of 250 ns; for the A version, it is 360 ns.

Circle 425 on Inquiry Card

Don't settle for a 'half' printer. A whole Printronix costs no more!

Both "halfs" that make a whole lot of difference!

Today, you can choose from several alphanumeric impact printers. Compare ours with the others. You'll find that Printronix impact matrix line printers offer print quality and reliability that no other matrix, drum, chain or belt line printer can match. We think you'll agree: it's the better printer . . . it's your best buy!

But we believe that alphanumeric printing meets only half of the distributed data processing needs of today . . . and especially tomorrow.

The other half has to do with printing graphics that can compact pages of printed data into simple, easy-to-understand forms. Printronix printers can plot almost anything. Graphs. Charts. Large Characters. Labels. Bar Codes. In fact, they offer a full plotting capability that no other impact drum, chain or belt line printer can provide!

Printronix Printer/Plotters give you both "halfs" of full printer capability for about the same price, or less, than you would pay for an alphanumeric printer alone.

Contact us for complete information on our 150, 300 and 600 line-per-minute printers. Get the whole answer to printer problems ... for the price of a "half" printer!

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(714) 549-8272. TWX:(910) 595-2535

PRINTRONIX

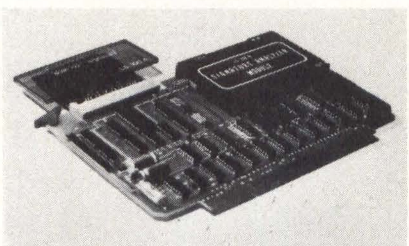
The "whole" printers.

CIRCLE 59 ON INQUIRY CARD

Low Cost Digital Logic Service System Locates Component Failures

Discrete, LSI, and microprocessor circuit troubleshooting and repair can be accomplished with minimal cost and technical knowledge. The LS-100 series logic signature system is S-100 bus compatible. It identifies hardware failures and verifies correct digital patterns providing go/no-go testing and diagnostics. Applications include commercial, industrial, and personal microcomputer equipment.

The device generates a 4-character signature from any repetitive logic state sequence—whether simple or complex. Board exercising sequences are developed with available utilities and instructions. Using the system, most computer system component failures can be isolated without an oscilloscope by those who do not understand hardware operation.



The system consists of a monitor board, display module, data probe with built-in logic state readout, 32-line multiplexer, accessories, test development utilities, and operating manual. A number of software and firmware support packages for other microcomputer systems are also offered by Phoenix Digital Corp, PO Box 11628, Phoenix, AZ 85017.

Features include 99.99% error detection accuracy; TTL compatible logic levels; separate control of enables, clock, and data inputs; signature clock rates up to 10 MHz; and 32-line multiple input selection. Other bus structures such as the EXORciser, Unibus, Multibus, SWTP, Altair, and Imsai may also be supported by plug-ins to the expandable system. Options are LED signature display, logic probes, and standalone test ability.

Circle 426 on Inquiry Card

Standalone Unit Expands Development System Line

The ZDS-1/25 supports software and hardware development of Z80 and Z80A based systems, functioning as an emulator of a prototype system, as a logic analyzer for monitoring and storing CPU bus activity and terminating program activity, and as a ROM/RAM simulator with memory mapping in blocks of 256 bytes. Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014 has introduced the 1/25 for prototype development systems with clock rates not exceeding 2.5 MHz. It is a low cost version of the ZDS-1/40.

The system is a single chassis, 19 x 9 x 15" (48 x 23 x 38-cm) standalone microcomputer with dual floppy disc drives for up to 60k bytes of memory storage as well as optional peripherals and interfaces. The 1/25A has 48k bytes of dynamic memory for $7740, the 1/25B has 60k bytes of dynamic memory for $8340, and the 1/25C has a 60k-byte memory with the company's PLZ programming language for $9340.

There are two modes of operation. In monitor mode, the system enables the user to utilize the Relocatable I/O (RIO) operating system to develop, edit, and modify software. In user mode, system memory and peripheral devices may be allocated partially or totally to the prototype system (with the exception of a few I/O ports), enabling program execution in a realtime environment.

Standard features include a Z80 CPU; 32k bytes of RAM expandable to 60k bytes; 3k P/ROM monitor program with 1k of dedicated monitor scratchpad area; in-circuit emulation via 3-ft (0.9-m) cable connection, and user clock verification. The programmable hardware breakpoint module enables suspension of instruction execution at a given address or activity, and programmable realtime storage module holds CPU or I/O port activity or monitors memory. The RIO operating system provides the OS executive, text editor, assembler, linker, P/ROM monitor and ZDOS file management system.

Circle 427 on Inquiry Card

For off-the-shelf delivery, contact your nearest Standard Distributor:

ARIZONA Phoenix—Liberty Elec. (602) 249-2232
Weatherford Co. (602) 272-7144

CALIFORNIA Anaheim—Weatherford Co. (714) 547-0891, 633-9633
Burlingame—Rose Elec. (415) 348-2740
El Segundo—Liberty Elec. (213) 322-8100
Glendale—Weatherford Co. (213) 849-3451
Mt. View—Elmar Elec. (415) 961-3611
Palo Alto—Weatherford Co. (415) 493-5373
Pomona—Weatherford Co. (714) 623-1261
San Diego—Liberty Elec. (714) 565-9171 or Weatherford Co. (714) 278-7400

COLORADO Commerce City-Elmar Elec. (303) 287-9611
Englewood—Weatherford Co. (303) 770-9762

CONNECTICUT Hamden—Arrow Elec. (203) 248-3801

FLORIDA Ft. Lauderdale—Arrow Elec. (305) 776-7790
Miami—Lykes Elec. (305) 633-8538
Orlando—Hammond Elec. (305) 849-6060
Tampa—Lykes Elec. (813) 886-6621

GEORGIA Doraville—Arrow Elec. (404) 455-4054
Norcross—Lykes Elec. (404) 449-9400

ILLINOIS Schaumburg—Arrow Elec. (312) 893-9420
Broadview—LCOMP Chicago (312) 865-7600
Westmont—RM/Bobelle Co. (312) 323-9670

INDIANA East Chicago—Acro Elec. (219) 397-8681
Ft. Wayne—Ft. Wayne Elec. (219) 423-4322
Indianapolis—Graham Elec. (317) 634-8202 or Sheridan Sales Co. (317) 297-3146

KANSAS Wichita—Radio Supply Co. (316) 267-5216

LOUISIANA Metairie—Trionics (504) 837-9025
New Orleans—Lykes Elec. (504) 733-3400 or Radio Parts, Inc. (504) 581-5959

MARYLAND Baltimore—Arrow Elec. (301) 247-5200
Beltsville—Treeko Sales (301) 937-8260

MASSACHUSETTS Cambridge—Apollo Elec. (617) 868-3120
Hingham—Sager Elec. (617) 749-6700
Woburn—Arrow Elec. (617) 933-8130

MICHIGAN Ann Arbor—Arrow Elec. (313) 971-8220
Farmington—Sheridan Sales Co. (313) 477-3800
Grand Rapids—RS Elec. (616) 241-3483
Kentwood—RM Elec. (616) 531-9300
Livonia—RS Elec. (313) 525-1155

MINNESOTA Bloomington—Arrow Elec. (612) 888-5522
Minneapolis—Arneson Sales Co. (612) 835-2177 or Northern Elec. Specialists (612) 835-2247

MISSOURI Florissant—Sheridan Sales Co. (314) 837-5200
Kansas City—LCOMP - Kansas City, Inc. (816) 221-2400
St. Louis—LCOMP - St. Louis, Inc. (314) 291-6200 or VanSickle Radio Elec. (314) 291-5000

NEBRASKA Lincoln—Scott Elec. Supply Co. (402) 464-8308

NEW JERSEY Bellbawr—Mid Atlantic (215) 923-6868
Moorestown—Arrow Elec. (609) 235-1900
Saddlebrook—Arrow Elec. (201) 797-5800

NEW MEXICO Albuquerque—Era Elec. (505) 266-5548

NEW YORK Buffalo—Summit Distributors Inc. (716) 884-3450
Corning—Corning Elec. (607) 962-0555
Farmingdale—Arrow Elec. (516) 694-6800 or Harrison Elec. (516) 293-7990
Mt. Vernon—Qar Industrial Sales (914) 699-2224
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Cleveland—Arrow Elec. (216) 464-2000 or Sheridan Sales Co. (216) 831-0130
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Dayton—Arrow Elec. (513) 253-9176, Esco, Inc. (513) 226-1133 or Sheridan Sales Co. (513) 223-3332
Toledo—RS Elec. (419) 531-5544

OKLAHOMA Oklahoma City—Radio, Inc. (405) 235-1551
Tulsa—Radio, Inc. (918) 587-9123

PENNSYLVANIA Pittsburgh—CAM/RPC Industrial Elec. (412) 782-3770 or Sheridan Sales Co. (412) 244-1640

SOUTH CAROLINA Greenville—Hammond Elec. (803) 233-4121

TENNESSEE Knoxville—Sheridan Sales Co. (615) 588-5386
Memphis—Bluff City Elec. (901) 345-9550

TEXAS Austin—Quality Components, Inc. (512) 458-4181
Corpus Christi—Douglas Elec. (512) 883-5103
Dallas—Quality Components, Inc. (214) 387-4949 or Weatherford Co. (214) 243-1571
El Paso—Era Elec. (505) 266-5548
Houston—Quality Components, Inc. (713) 772-7100 or Weatherford Co. (713) 688-7406

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WASHINGTON Bellevue—Liberty Elec. (206) 453-8300
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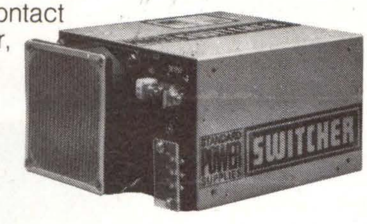
For detailed specs and prices on the switcher that beats the others cold, or to place a direct order, call your nearest distributor, or contact Standard Power, Incorporated, 1400 South Village Way, Santa Ana, CA 92705, 714/558-8512.



MODEL	VOLTS	AMPS	SIZE	WT. (LB)
SWS 750-5	5	150	10.10 x 7.75 x 4.94	15
SWS 750-12	12	60	10.10 x 7.75 x 4.94	15
SWS 750-15	15	50	10.10 x 7.75 x 4.94	15
SWS 750-24	24	33	10.10 x 7.75 x 4.94	15
SWS 750-28	28	28	10.10 x 7.75 x 4.94	15

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The Spec Meeter

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STANDARD POWER

SOFTWARE

8080/8085 Assembler Transfers Programs To Development System

The ASMB-80/85 mnemonic assembler for 8080 and 8085 microprocessors permits users with previously written assembler programs to transfer easily to the company's multiuser disc development system. The object code which is output is 100% compatible with the company's block structured assembler BSAL-80/85 object code (*Computer Design*, Feb 1977, p 134). The use of old programs is retained, with the added gain of mnemonic or block structure assembler language for future work.

Developed by Mupro Systems Div, 424 Oakmead Pkwy, Sunnyvale, CA 94086, the assembler provides relocatable code, parametric macros, 36 error diagnostics, and conditional assembly capability. Mnemonics are compatible with Intel's 8080 and 8085 instructions. Also, identifiers may contain up to 15 characters and may optionally be listed in a cross reference table.
Circle 428 on Inquiry Card

6800 Disc Operating System Aids Development And Applications

SDOS disc operating system for 6800 microprocessors handles from 32k to 64k of RAM and any combination or number of disc drives (with storage capacities of up to 2.14G bytes) online for application software or development tasks. Random and sequential disc files, device independent I/O, user customizable command interpreter, and tailoring of disc drivers are supported. Disc files, created automatically, increase or decrease in size because the operating system does all space management on a dynamic basis.

Command files allow prepackaged sequences of keyboard commands to be executed automatically. Errors are reported by English messages. The command interpreter supports list, copy, delete, file, rename, and help commands. Turnkey systems and enhancements can be built by replacing the interpreter with the desired application program. The system's utility programs allow the user to initialize a new disc, check the validity of disc files, and repair damaged disc file structures.

Versions of the operating system operate on Midwest Scientific Instruments, Cincinatti Milacron model 20, Electronic Product Associates Micro-68, and Wavemate 6800 systems; versions for several other 6800 systems will also be offered by Software Dynamics, 17914 S Laurelbrook Pl, Cerritos, CA 90701. The company's I/O package interfaces SDOS to the assembly language, allowing all available company software to be run under the operating system without change. Application programs compiled by the BASIC compiler on other systems will run on SDOS with little or no change.
Circle 429 on Inquiry Card

Meta Assembler Supports 2900 Bit-Slice Microprocessor

Meta Assembler language, compatible with Advanced Micro Devices' AMDASM language, is written in ANSI standard FORTRAN IV and will run on any computer with a word length greater than or equal to 16 bits. The instruction set of the microprogrammable bit-slice microprocessor can be defined by the user; programs are then assembled utilizing that instruction set. The program features conditional assembly, complex expression evaluation, and a cross reference table listing.

A separate program included by Microtec, PO Box 60337, Sunnyvale, CA 94088 in the package is used to break up the assembled object code into organizations that are compatible with the target P/ROM or ROM array. Additionally, the object module format is translated into either BNPF or Data I/O's ASCII hexadecimal format.
Circle 430 on Inquiry Card

Resident 8080 Assembler Gains Speed Through Hashing Technique

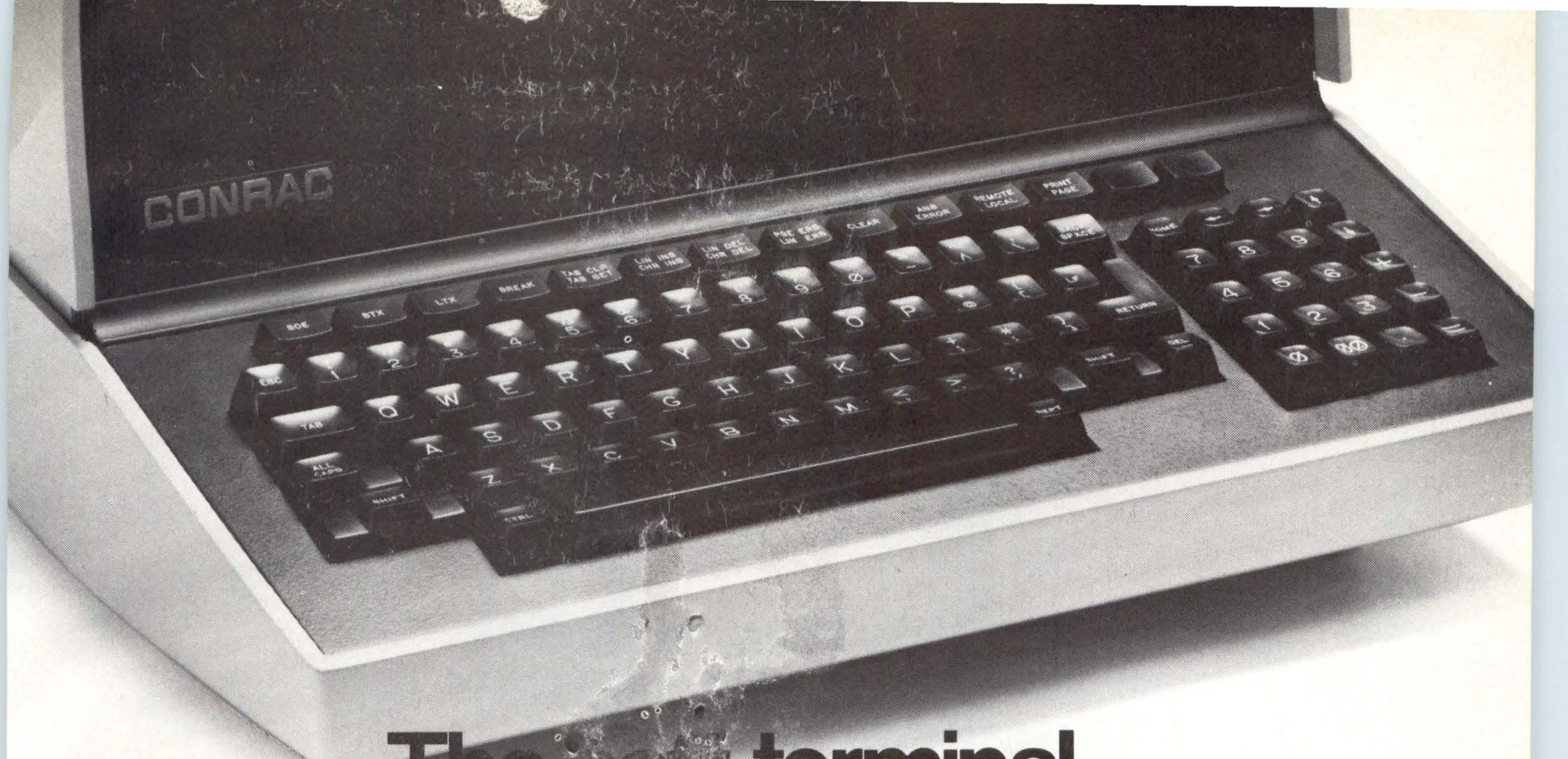
A 2-pass resident assembler for the 8080 microprocessor is Intel compatible except for macros, conditional assembly, and logical expression operators. Free format source is also accepted. Due to the hashing technique used by the label handler, the assembler is reported by Technical Systems Consultants, Inc, Box 2574, West LaFayette, IN 47906 to be very fast. Labels may be any length with six characters significant. Both passes and the initialization required for each are written as subroutines.

The assembler supports all standard pseudo-ops, as well as such options as pagination; titling; spacing; listing suppression; hexadecimal or octal output; decimal line numbers; hexadecimal, decimal, octal, or binary constants; and alphanumerically sorted symbol table. Object code may be output in Intel ASCII tape format or directly into RAM. Break and escape keys, and auto field formatting are also included. Source and symbol table space and 5.5k bytes of RAM are required.
Circle 431 on Inquiry Card

Cross Assembler Speeds Microprocessor Software Development

A cross assembler package, available on printed tape, translates instructions and data for the company's INS 8060 (SC/MP) microprocessor programs on Intel MDS-800, 210, 220, 230, or other host microprocessor development systems capable of running the ASM80 macroassembler. With a set of macros loaded into macro tables of the host system assembler, the MDSMAC allows fast applications software development. Assembly object code output is in the host's format, permitting direct programming of P/ROMS or ROMS.

Most directives, pseudoinstructions, expressions, constant definitions, and memory reference instructions are in the host computer dialect. National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has also devised two macros for high and low address orders. Conflicting INS8060/8080 instructions are slightly modified by appending an "S" to the 8080 mnemonic. □



The soft terminal. Designed to be redesigned.

Chances are, the intelligent terminal you really need doesn't exist yet.

That's why we build the Conrac 480, The Soft Terminal. It's designed to be redesigned by your software to fit your system like a glove.

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Most CRT terminals are built around one large circuit board, which doesn't leave you much flexibility.

The Conrac 480, on the other hand, offers you the benefits of a *clean bus architecture.* Plug in four cards, and get a basic working terminal. Plug in up to twelve additional cards, and get some real power. Cards like RAM up to 48K bytes, PROM up to 16K bytes, and interfaces to floppy disk drives, printers and other peripherals.

Software to make it happen.

Do you need a special keyboard, character set, or set of terminal attributes? No problem. Just plug in a special PROM.

With the proper MPU software, the Conrac 480 can be configured as a polling terminal or as a powerful microcomputer. Or as anything in between. This software can reside in PROM, or can be downloaded into RAM from a host computer or from disk.

Many software modules are available off-the-shelf, like a basic editing package, and protocol handlers for IBM, Burroughs, and Univac. More are on the way.

To make microprogramming easy, you can use the AMI 6800 Microcomputer Development Center software, which runs perfectly on our terminal. That's power!

Attractive outside as well as inside.

Any way you look at it, the Conrac 480 is attractive. The basic version is only 20" deep and fits where space is limited. Its understated modern styling blends into virtually any decor. And you can have your own color and texture.

Operators love the feel of our long-life capacitive keyboard with sculptured keys. And our sharp and stable CRT display. As a matter of fact, we're known worldwide as *the* manufacturer of professional video monitors.

Write to us or give us a call for more facts. We'll send you a comprehensive 12-page brochure on The Soft Terminal. And we promise not to use "hard sell."

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Telephone (07934) 675, Telex 74250

CIRCLE 61 ON INQUIRY CARD

AN ADD-IN RECOGNITION MEMORY FOR S-100 BUS MICROCOMPUTERS— PART 1: AN INTRODUCTION

Sydney Lamb
Semionics Associates, Berkeley, California

Content addressable or associative computer memory is available for the first time at a price that makes it practical for use with microcomputers. Called recognition memory, it differs from conventional memory by eliminating serial searching. An item may be accessed simply by being named. If it is present, those locations which have it recognize it and respond instantly, greatly reducing search time (compared to conventional memories) as well as reducing the amount of money and memory space invested in conventional software.

Recognition memory (REM) can be written into and read from like ordinary memory, but it also has parallel processing functions, including six types of recognize and multiwrite. Recognition operations replace serial searching, while multiwrite allows the central processing unit (CPU) to write into multiple locations with a single instruction. Moreover, individual bit masking may be applied to all operations, including ordinary (location accessed) read and write. A data processing system with these functions is known as a content addressable parallel processor. Suiting pattern recognition and information retrieval applications, it is also capable of performing parallel arithmetic operations. REM S-100, priced at $325, operates with Z80 or 8080 microprocessors or with any other microprocessor connected to the S-100 bus.

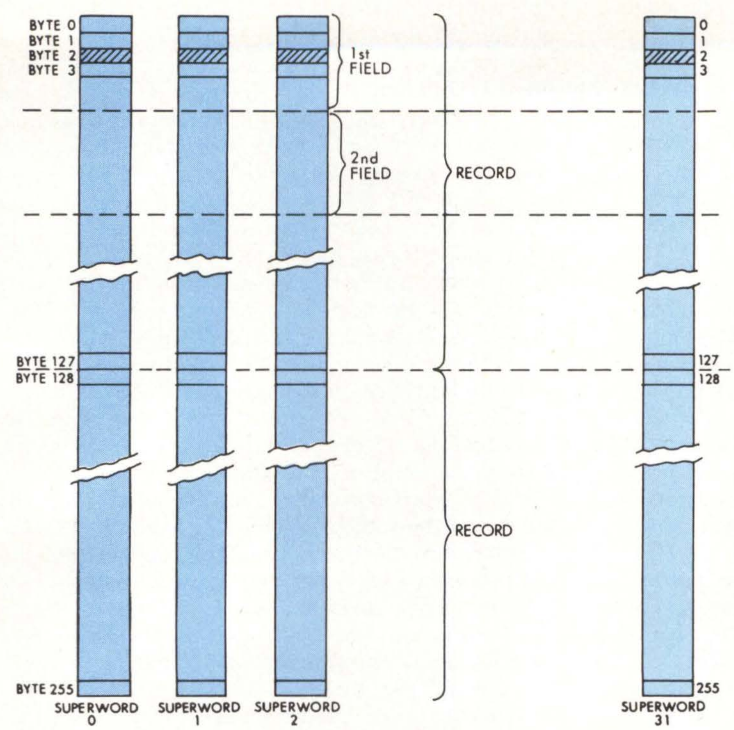
Multiwrite

Besides the basic recognition capability, or content addressability, REM has the multiwrite function: the ability to write data into multiple locations with a single instruction. Thus, the user can perform a recognize operation to find all records with certain properties, followed by a multiwrite into all those records (the responders). Multiwrite data might be a flag for use in some later recognize operation, or might be a rewriting of the recognized data to correct or update it.

There are three varieties of multiwrite. The user can write data into all records, into all responders to a preceding recognize operation or sequence of recognize operations, or into all nonresponders.

Ordinary RAM Functions and Bit Masking

In theory, a content addressable memory (CAM) need be addressable only by its contents, and some CAMs have been designed that way. However, REM has been designed as a CAM that can also be used as ordinary random-access memory (RAM) whenever the user desires—that is, a CAM whose contents can also be accessed by location. Thus, the capabilities of REM subsume those of RAM, just as those of RAM subsume those of read-only memory (ROM). A comparison of ROM, RAM, and REM is contained in the following table.



Layout shows 8k of REM (two 4k boards) with two equal length records/superword, and records divided into fields. Shaded bytes are accessed in parallel in REM operation if byte position 2 is specified by low order address bits

Modes of Operation

	Single Location		Parallel Operations	
	Read	Write	Recognize	Multiwrite
ROM	+	−	−	−
RAM	+	+	−	−
REM	+	+	+	+

REM also has a bit masking capability. The mask is a combination of 1s and 0s, written by the user to mask out certain bits. Those bits in positions where the mask has 0 are ignored. The mask can be used not only with recognize and multiwrite operations, but also with ordinary location accessed read and write. With the read operation, the data received by the central processing unit (CPU) are the logical AND of the mask and the data stored in the addressed location.

Nonmatch Recognition Functions

The recognize function has been described only in its simplest and most direct variety—that in which a memory location recognizes that its contents exactly match the presented data. REM also has five additional recognition functions: greater than or equal to, greater than, less than or equal to, less than, and not equal to. These varieties of recognition are built into the REM hardware. Besides being directly usable, they provide the basis for various additional functions that are software specifiable, such as between (ie, greater than lower limit, but less than upper limit). Different recognize functions can be performed on different fields. For example, it is possible to ask for the records from a stored data file of all individuals living in Kansas, with annual income greater than or equal to $25,000, age less than 30, and last name beginning with A, B, C, or D (ie, less than or equal to D).

Complex Functions

Systems with all of these capabilities are called content addressable parallel processors (CAPPS) by Foster.* Such machines are quite powerful. By interweaving recognition and multiwrite operations with appropriate use of bit masking, a CAPP is able to achieve speeds, flexibility, and programming ease well beyond the range of even very large and expensive conventional computers.

Thus, as previously mentioned, a recognition operation can be followed by a multiwrite operation, using a mask, to flag all records meeting the particular set of recognition criteria. These flags may now be included in the criteria for subsequent recognition operations.

It is easy to include "either-or" conditions in the recognition criteria. Instead of asking in the above example for the records of all persons living in Kansas, one could specify Kansas, New Mexico, or Colorado. The appropriate REM system subroutine can multiwrite a flag in all records with Kansas, then try New Mexico and multiwrite a flag in the same position of these responding records, and likewise for Colorado; the resulting records with the flag are the ones that satisfy the disjunctive criterion.

Some complex operations, among others, that are made possible by the abilities of REM include:

(1) incrementing the count field of all records meeting specified recognition criteria,

(2) bit by bit comparison of an input pattern with stored patterns,

(3) locating the record having the maximum value for a specified byte position or field (eg, the count field),

(4) similar to (3) for minimum value (useful in alpha-

*Caxton C. Foster, *Content Addressable Parallel Processors,* Van Nostrand Reinhold, 1976 betic sorting, since alphabetic order corresponds to numeric in standard binary codes for alphabetic characters),

(5) finding best fit in pattern recognition situations in which there is not likely to be a perfect match, by combining (1), (2), and (3),

(6) printing out an ordered list (based on alphabetic or numeric order of the specified field) of all records meeting the specified recognition criteria,

(7) moving information from one field to another within all records, or all records meeting specified recognition criteria, and

(8) various logical operations upon flags.

2-Word Sizes: Easy Interface With CPU

As the above examples illustrate, an associative memory is most useful if it has a very large word size—much larger than that of ordinary computers. However, a very large word size could lead to two problems: a large bus is expensive, and the associative memory could be difficult to interface with an ordinary CPU. The effects of these problems can in fact be seen by looking at prior associative memory designs. Associative memories have generally been built with their own tailor-made CPUS, capable of operating with very large word sizes.

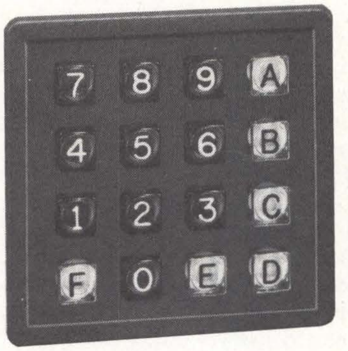
A simple solution, however, to the problem of interfacing with ordinary CPUS is the use of two word sizes. The smaller word is that of the CPU, simply called the word, as usual. In the case of most microcomputers, this is of course eight bits (one byte). The larger unit may be called the superword or REM record. Different varieties of REM may be built with different sizes of superwords. In the current version, the superword is 256 bytes long. This length is sufficient for most data records that would be put into REM, and since 256 = 2^8, 1 byte (8 bits) can serve to locate byte position within superwords. Of course, the user can put shorter records into the superwords—two, three, or more. The Figure illustrates a layout with two records per superword. (The terms entry and record are used interchangeably, although the term REM record is sometimes used for the full 256-byte superword.) Different types of records, of different sizes, may also be stored in REM. For example, a language processing system could have 7 lexical entries of 30 bytes each (for lexical rules) and 3 syntactic rule entries of 15 bytes each (for a total of 255 bytes) per superword.

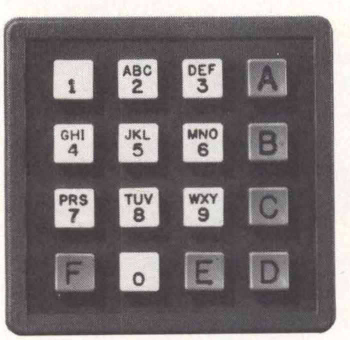
Since the smaller word—eight bits in the current design—makes it easy to interface REM with a microprocessor, the memory needs no CPU of its own. REM can therefore be built as an add-in associative memory. The current version is designed for the S-100 bus, which means that an S-100 microcomputer can be converted into a CAPP just by plugging a REM board into the S-100 bus.

The CPU can only operate upon one word at a time (one byte in the case of most microprocessors), but when it is performing a REM function, it operates upon the specified word position within all superwords in parallel, no matter how many there are. Multiple boards can be plugged into the same computer, subject only to power requirements (1.5 A per S-100 board) and the availability of slots. Since multiple boards are accessed in parallel, they can occupy the same address space if desired. However for use with ordinary RAM functions, they must then be assigned to different banks.

This discussion of associative memory, part one of a 3-part series, will be continued in next month's column with the presentation of specifications and a description of the memory structure. The final part will detail various applications in which the REM may be utilized.

Low Profile LED Keyboards

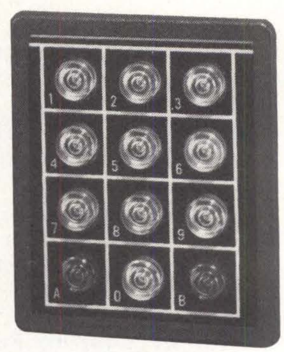


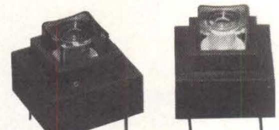


High performance LEDs mounted inside keybutton give visual indication of function status. 10, 12, or 16 station keyboards easily mounted from front of panel. Square or round keys, keytop or overlay decal marking. Universal circuit and pin-outs interface with most logic. Unlighted keyboards offer same design advantages but without LED lighting. Low cost, dependable, attractive. Wide selection of colors offer custom design at off-the-shelf prices.

Single station keyswitch modules, LED or unlighted, round or square, provide inexpensive method of assembling custom layouts or short-run prototype keyboards. Mount on PC or prepunched boards with holes on .100″ centers. Optional BCD or hexadecimal encoder "Adder-Boards" can be added to the Low Profile Keyboards. Compact packaging minimizes required space behind the panel.

Get the complete story now. Write for colorful descriptive catalog covering complete keyboard line.





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DUAL ONE SHOTS

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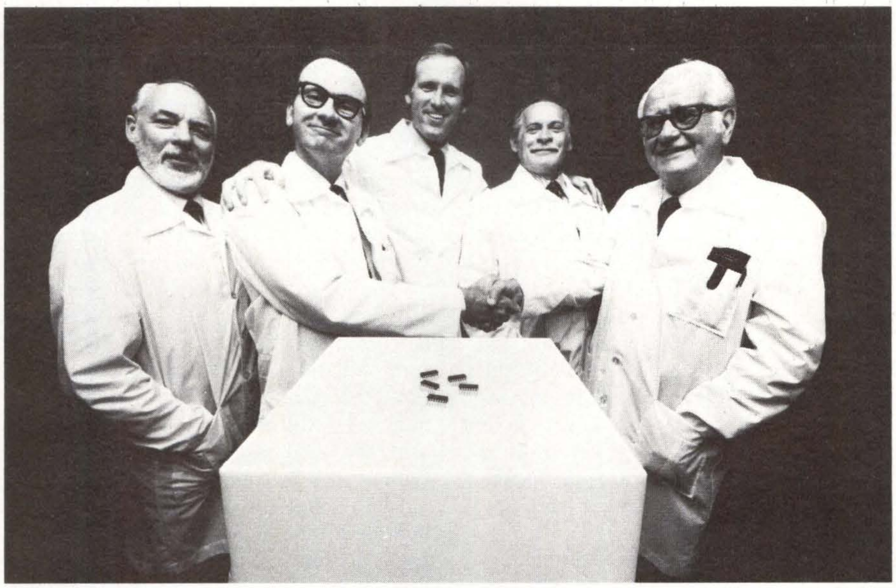

Our 96S02 Schottky TTL dual retriggerable resettable monostable multivibrator has been the industry standard ever since we invented it. But now it's getting some competition from Fairchild's brand new 96LS02 Low Power Schottky TTL dual one shot. A lower power version of a proven, time-tested part.

If you have delay or high-speed timing needs, one of our one shots is right for you.

Hot shot performance.

Our one shots feature very short propagation delays to output. 12 ns for the 96S02. 35 ns for the 96LS02.

Variable output pulse width between 35 ns and infinity over a 1300:1 range by use of the timing resistor alone.

0-100% duty cycles allowed without jitter.

Complete compatibility with all TTL families.

All of which provides a wide delay range. Stability. Predictable accuracy. And excellent noise immunity.

Our one shots hit the bull's-eye.

Our 96LS02 provides hysteresis on both trigger inputs and can utilize timing resistors up to 1 MΩ.

Our 96S02 provides hysteresis on the positive trigger input and can use timing resistors up to 2 MΩ.

And both require less power and less expensive timing components for long pulse widths.

If you'd like to take a shot at using our one shots in your next design, or if you're just interested in more details, contact your Fairchild sales office, distributor or representative today. Or use the direct line at the bottom of this ad to reach our Digital Products Division. Fairchild Camera and Instrument Corporation, P.O. Box 880A, Mountain View, CA 94042. Telephone: (415) 962-3716. TWX: 910-379-6435.

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CIRCLE 63 ON INQUIRY CARD

Single Board Holds 12-Bit Resolution Analog Input/Output System Compatible With Zilog Microcomputers

MP2216 provides 12-bit, 32-channel analog input and 2-channel analog output on the same board. Mechanically, electrically, and logically compatible with Zilog Z80-MCB® and Z80-MCS systems, the board is powered from the computer's 5-V logic supply. Logic levels and drive capacity are matched to the system bus.

The input section accepts 16 differential or 32 single-ended channels. Inputs ranging from millivolts to volts can be digitized because of the analog system's variable gain instrumentation amplifier. Input range is set for ±10 V and amplifier gain is 1. Throughput accuracy is ±0.025% FSR and throughput time is 40 μs/channel.

The 2-channel output section accepts 12-bit inputs from the data bus and converts them to analog outputs. Input data for each DAC are double buffered to minimize output glitches during data updates. Output ranges of ±10, 0 to 10, ±5, 0 to 5, and ±2.5 V at 5 mA are strap selectable; output settling time is 10 μs on all ranges. Bipolar and unipolar operation are jumper selectable.

Interfacing is accomplished primarily through a Z80 PIO that is contained within the system. The card is plugged into any I/O slots in the MCS chassis. For the MCB system, any slot that is first connected with the proper bus signals can be used.

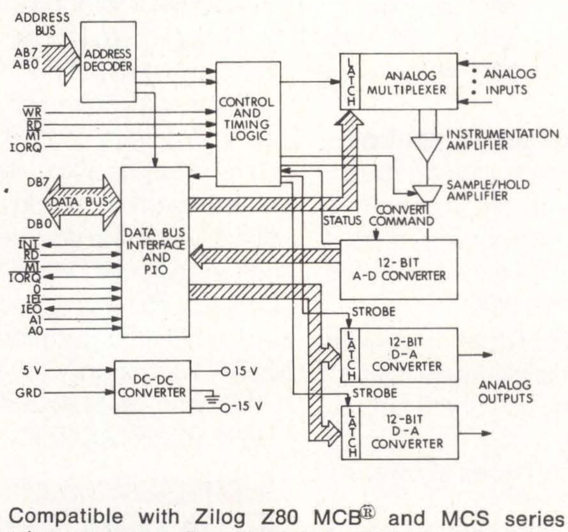
The board interfaces with the Z80 I/O bus, occupying 10 locations for the complete I/O system. The first four locations are required for the PIO, the next two to transfer input channel address and board status, and the remaining locations to pass data to the two DACs.

Data can be acquired from the analog inputs in either polling or interrupt mode. Programming is simplified as all are treated as I/O locations. The board's analog input system must be initialized to operate in either mode; the analog output system does not require initialization.

Although factory set by Burr-Brown, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734, the onboard PIO and registers may be moved independently throughout the I/O address space. The only address selection limitations are that the PIO and board registers cannot occupy the same locations and that the three most significant address bits of both must be the same.

The microperipheral board is available in two versions. The MP2216-AO configuration includes all features of the MP2216 system. The MP2216 includes all features except the two DACs. Prices in one to nine quantities are $745 and $595, respectively.

Circle 432 on Inquiry Card



Compatible with Zilog Z80 MCB® and MCS series microcomputers, Burr-Brown's MP2216 microperipheral is a 12-bit, 32-channel analog input/2-channel analog output system. Operating from computer power supply, board has high level or low level inputs

16-Bit Microcomputer On Single Board Has Advanced Capability

Minicomputer performance and systems capability have been combined with microcomputer board technology and economy to produce a 16-bit single-board computer. The MCB/1 microNOVA board computer from Data General, Route 9, Westboro, MA 01581 includes a 16-bit microNOVA CPU, 2k bytes of static RAM, sockets for up to 4k bytes of P/ROM, an asynchronous communications interface, and a 32-line digital I/O port on a 7.5 x 9.5" (19 x 24-cm) board.

The CPU provides NOVA® architecture, hardware stack and frame pointer, 16-bit hardware multiply and divide, realtime clock, hidden memory refresh, data channel (DMA) control, and 16-level priority interrupt. The memory bus extends off the board, allowing addition of more memory.

The digital I/O interface provides 16 input lines, external interrupt line, 16 output lines, data strobe, and system reset line. It provides full-duplex communication with an asynchronous terminal or modem via a 20-mA current loop or EIA RS-232-C lines with speeds of 110 to 9600 baud. Line speed, data bits, parity, and stop bits are jumper selectable. The I/O bus also extends off the board for expandability. The com-

INTRODUCING THE NEW COMPUTER THAT ISN'T.

The biggest problem with buying a new computer is that you have to buy a *new* computer. An untried, unproven computer.

The new Classic 7870, the newest member of the MODCOMP Classic family, solves that problem. Because it has all the performance features of the Classic 7860, which we introduced earlier this year. Except for one thing. It has four times the memory capacity.

With its large solid state memory (up to 2 million bytes) and an effective memory cycle time as low as 125 nanoseconds, it gives you the speed and capacity you need for demanding scientific, engineering and large process control applications.

And because the 7860 has already been tried and proven, the 7870 gives you something that no other new computer can offer you — a track record.

Classic beats DEC, Interdata, Prime and SEL.

In benchmark tests by computer users measuring both computational and I/O performance, the Classic 7860 has outperformed DEC's 11/70 and VAX. Interdata's 8/32. Prime's 400. And SEL's 32/75.

Hard to believe? Not really. Not when you consider some of the features we've built into the Classic.

Both the 7860 and 7870 have our unique multi-word (16-64 bit) architecture. Pipelined instruction processing. Our super fast floating point processor. And hardware instructions that are specifically designed for fast Fortran execution.

You don't have to trade reliability to get Classic's performance.

The best thing about the Classic isn't its performance. It's the fact that its state-of-the-art performance isn't achieved at the expense of reliability.

Since its introduction, the 7860 has been tested exhaustively by computer users in both scientific and process control applications.

They report that the Classic is as reliable as any computer MODCOMP has ever introduced. And that's saying something. Because independent surveys have consistently rated MODCOMP computers as the most reliable real-time systems on the market.

Why buy a new computer when you can buy our new computer?

The Classic is supported by a comprehensive set of operating systems and network extensions that have been used successfully by some of the most demanding computer users in the world. We also provide all the documentation you need to implement it quickly and easily. Plus a worldwide network of service specialists.

In fact, the only thing the new Classic 7870 doesn't give you is something you don't want anyway.

The problems associated with new computers.

For more information, send for our "MODCOMP Classic Family" brochure.

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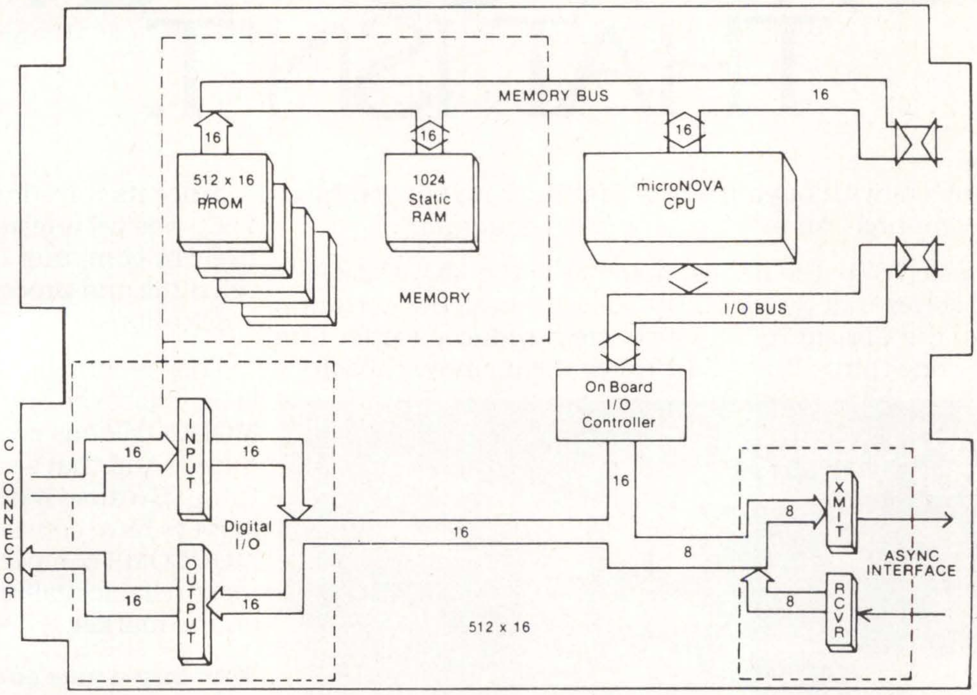


Eliminating packaging constraints, Data General's MBC/1 is complete 16-bit computer on single board. It contains 16-bit microNOVA CPU with full NOVA architecture, hardware stack and frame pointers, realtime clock, DMA, priority interrupt, 2k bytes of RAM, 4k bytes of P/ROM, and 32-line I/O interface. System is supported by MBC/M multitasking software package

puter is compatible with the microNOVA and NOVA 3 computer lines.

Software includes a multitasking support package (MBC/M) with an emulator for program development under the company's operating systems (DOS, AOS, and RDOS) and with a monitor for program execution. Optional onboard ROM console debug and self-test diagnostics permit software development on larger minicomputer systems.

With the software, users can write and debug applications programs on a development computer. A library of routines minimize the programming effort necessary to implement applications. Utility programs generate tapes for P/ROM burners; an optional console debug/diagnostics program provides two 512 x 8 P/ROMs that plug into the board's sockets.

Circle 433 on Inquiry Card

SBC Compatible 64k RAM Implements Error Correcting Logic

The necessity for higher data reliability and easier maintenance in MOS dynamic RAM storage for Intel SBC-80 systems is provided by a family of RAM boards containing error correcting circuitry. Mupro's Computer Products Div, 424 Oakmead Pkwy, Sunnyvale, CA 94086 offers a complete line that includes seven memory sizes: 4k, 8k, 12k, 16k (two versions), 32k, 48k, and 64k bytes. The 4k to 16k boards are available with 4k dynamic RAM; 16k and larger are available with 16k RAMS.

Three configurations are available for each of the 8 board sizes—without error detection, with single-bit parity, or with single-bit error correction and double-bit error detection—for a total of 24 boards. All error correcting configurations have diagnostic indicators to pinpoint the precise memory chip in which any correctable error occurred.

Error condition information is stored in an onboard register, and displayed by the onboard status LED indicators, which differentiate a single- or double-bit error, as well as the chip row and column in which a single-bit error occurred. Single-bit errors are automatically corrected in either case, and the system continues to operate. Failed parts may be replaced as part of regular maintenance.

Each board is provided with onboard refresh of the dynamic RAM.

Our new MegaFloppy family of disk drives zeroes in on the needs of both large and small quantity OEMs. These 5¼-inch floppies offer the capacity you'd expect only from 8-inch diskette drives, at 5¼-inch prices.

Our 1015 MegaFloppy lets large OEMs incorporate it right into their system. Select from the 1015 MegaFloppy Mod I and Mod III 35-track models. Or the Mod II and Mod IV 77-track models. They're double density single drives available with single or dual heads and capacities up to 946K bytes of formatted storage per drive, when used with the Micropolis Intelligent Controller.™ You can also daisy-chain up to four 1015 MegaFloppy drives—for a staggering total capacity of approximately four megabytes on-line.

Or you can choose from our 1055 MegaFloppy, complete system packages for small quantity OEMs. The 1055 MegaFloppy Mod II and Mod IV are 77-track, dual drive models—featuring the integrated Micropolis Intelligent Controller.

The Controller uses a simple, bi-directional interface, so an 8-10 chip personality card is all you need for attachment to a variety of 8 or 16-bit hosts.

It performs data formatting, encoding and decoding. Sector buffering. Error detection and recovery. Provides versatile user commands. And interfaces easily with the host system.

So, if your size and price needs call for a 5¼-inch disk drive system, write to us about our million-byte MegaFloppy family.

Just one more first from the citizens of Micropolis.

MICROPOLIS™
More bytes in store for you.

For a descriptive brochure, in the U.S. call or write Micropolis Corporation, 7959 Deering Avenue, Canoga Park, California 91304. Phone (213) 703-1121. Or, better yet, see your local distributor.

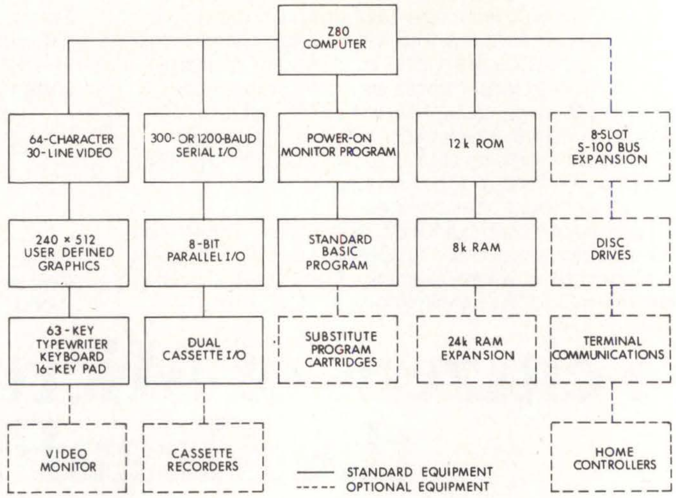
The citizens of Micropolis introduce the MegaFloppy.™

The first 5¼-inch floppy that gives you 1 million bytes.

Provision for external refresh synchronization, such as the Z80 provides, is also included. Battery backup is included. Refresh logic and essential circuitry to power the RAMS are connected to a separate battery backup power distribution bus to minimize backup power requirements. An input line for externally generated memory R/W protect insures against spurious R/W cycles during power fail switching periods.

Single quantity prices range from $455 (4k without error correction) to $2750 (64k with error detection and correction), with quantity discounts available. Delivery is 30 days ARO.

Circle 434 on Inquiry Card



Sorcerer computer from Exidy features keyboard enclosure housing complete electronics of system, based on Zilog's Z80 microprocessor. Standard and optional components are detailed. User programmability is expanded with availability of plug-in Rom Pac™ cartridges

Users Alter μComputer's Operational Functions With Plug-in Cartridges

Expandability of user programmable languages and simplicity of prepackaged programs on magnetic tape cassette are featured in the Sorcerer™ computer, introduced by the Data Products Div of Exidy Inc, 969 W Maude Ave, Sunnyvale, CA 94086. The self-contained computer need only be plugged into a video display and cassette tape recorder to be a fully functioning system. It can operate one or two audio cassette tape recorders for playing applications programs on cassettes, serving both communications and timesharing applications.

Rom Pac™ cartridges that plug into the side of the computer contain high level programming languages, operating systems, or special proprietary software. Standard BASIC comes with the computer; also available or under development are a user programmable EPROM Rom Pac, an assembler, editor, disc operating system, and word processing package.

System components are an 128 ASCII set, 79-key keyboard with upper/lower case alphanumeric characters and graphic symbols; 16-key numeric pad; Z80 microprocessor; 12k ROM with power-on monitor program; and 8k RAM for user program space, expandable internally to 32k. Addition of the company's 8-slot S-100 bus module and S-100 boards allow expansion. Dual cassette interface permits data rates of 300 or 1200 baud.

With 256 graphic expressions, the keyboard has 64 characters designated, with 64 others that are user definable. Graphic resolution of 122,880 points on the video screen is produced in a 512 x 240 format. A total of 1920 characters can be displayed at once in 30 lines x 64 characters, in an 8 x 8 format. A printer may be attached to the parallel interface to provide hardcopy output.

Circle 435 on Inquiry Card

OEMs Achieve Maximum Flexibility From Compact, Expandable System

As the initial member of the L Systems™ family, the PDP-11T03-L incorporates the RL01 high density disc storage units with a 5.2M-byte capacity in each of its two discs, a PDP-11/03-L microcomputer with 64k bytes of memory, and a choice of hardcopy or video terminals in compact cabinetry. A universal power supply permits quick conversion between 115 and 230 Vac, at 47 to 63 Hz.

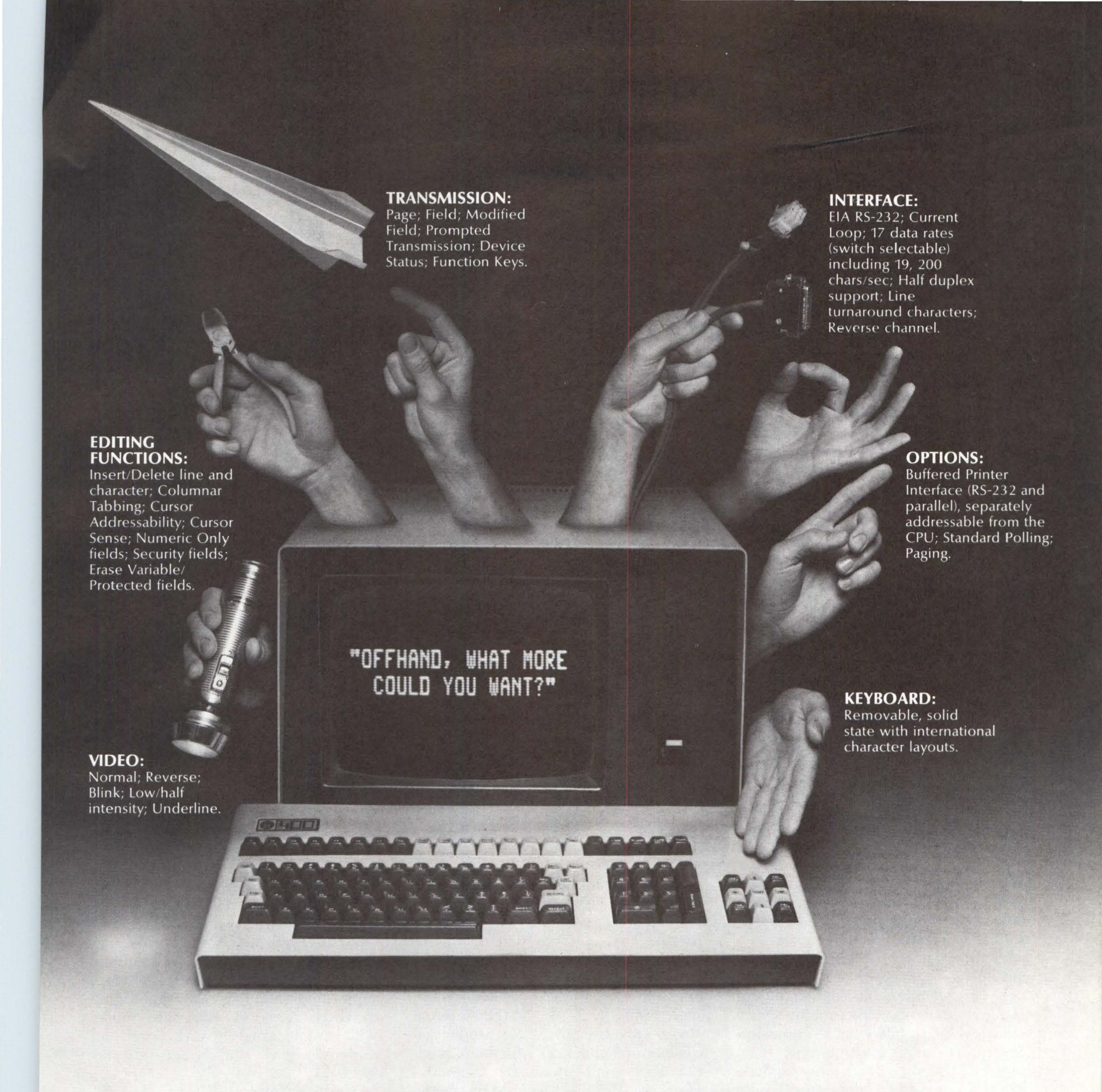
Digital Equipment Corp, Maynard, MA 01754 has supplied the system package with the latest version of the RT-11 operating system, version 3-B permitting development of extensive and sophisticated application programs, particularly suiting it to OEM needs. Standard software includes an editor, macro assembler, and utilities. High level languages such as BASIC, FORTRAN IV, and APL are available as options. An extended floating point instruction set is also included. The system is priced at $18,000.

Circle 436 on Inquiry Card

Fast 1-Chip μComputer Uses Emulator For Developing Prototypes

The 40-pin NMOS single-chip microcomputer, R6500/1 operates at 2 MHz with a 1-μs minimum instruction execution time. The device has an R6502 CPU instruction set, and is fully software compatible with the 6500 family. The advanced system architecture which enables multiple addressing enhances its performance speeds.

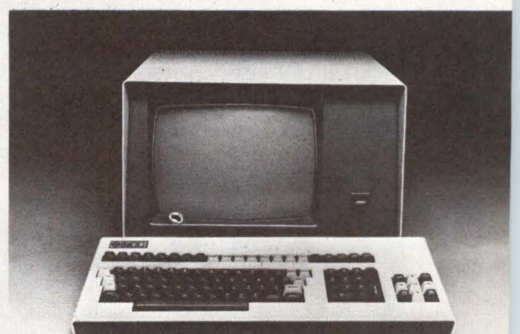
Onchip features include 2k x 8 ROM, 64 x 8 RAM, 16-bit interval timer/event counter, 32 bidirection-



When it comes to flexibility, the Infoton 400 Data Display terminal can hand you all you need.

Designed around the Z-80 microprocessor, it offers complete control of all Blocking and Editing functions through software settable modes. One thing that's especially easy to handle about the I-400 is its cost; at $1,095 in quantities of 100 or more, it's the most versatile terminal for the price you can get your hands on.

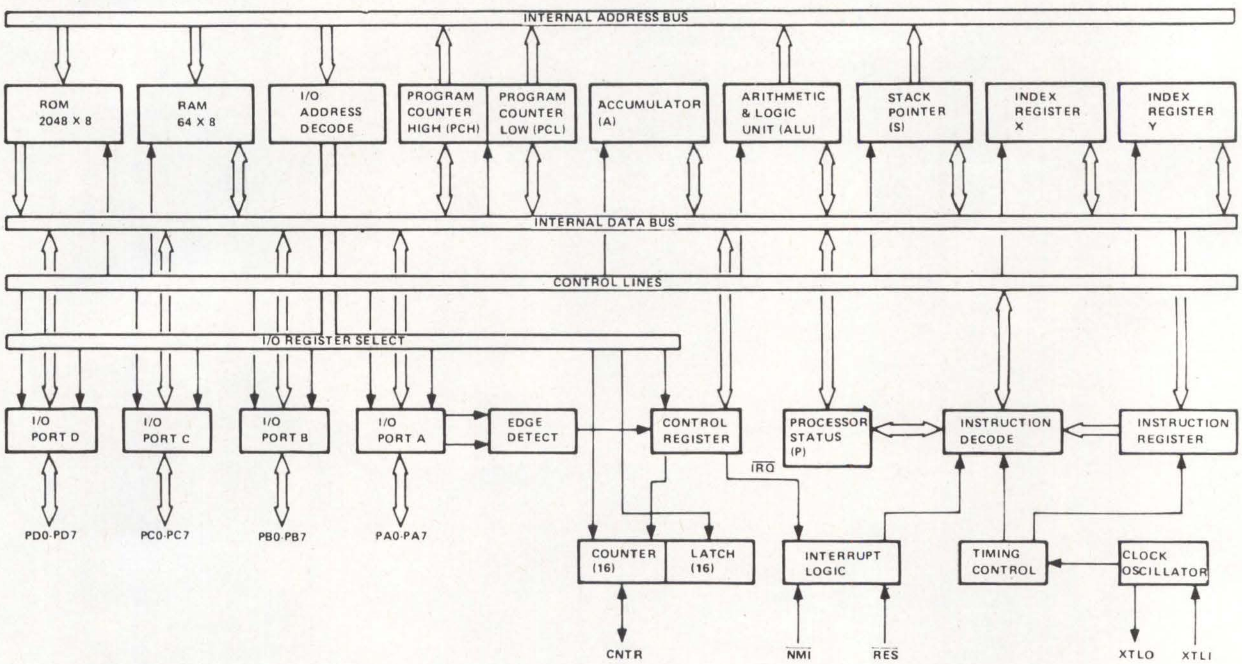
More information on the I-400 is quickly within your grasp. Call Infoton toll-free at (800) 225-3337 or 225-3338. Ask for Barbara Worth. Or write Barbara Worth at Infoton, Second Avenue, Burlington, MA 01803.



Infoton 400

Prepared by Chickering/Howell, Los Angeles.

CIRCLE 66 ON INQUIRY CARD



I/O ports, registers, and commands of Rockwell's R6500/1 single-chip microcomputer are treated as memory and are assigned specific addresses. This I/O technique allows full set of 6502 CPU instructions to be used in generation and sampling of I/O commands and data. When instruction is executed with I/O address and appropriate R/$\overline{W}$ state, corresponding I/O function is performed

al I/O lines, and internal clock oscillator. The 32 I/O lines are divided into 4 8-bit ports. Additionally, it has maskable and nonmaskable interrupts and an event-in/timer-out line.

Four programmable counter modes of operation are freerunning with clock cycles counted for realtime reference, freerunning with output signal toggled by each counter overflow, external event counter, and pulse width measurement mode. A 16-bit latch automatically reinitializes the counter to a preset value. Interrupt on overflow is software maskable to allow prototype circuit development.

Rockwell International Corp, Electronic Device Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803 provides a 64-pin emulator, of which 40 pins are electrically identical to the standard R6500/1 part. The device provides all R6500/1 interface lines plus routing the address bus, data bus, and associated control lines off the chip to be connected to external memory. An R6500/1 personality module for software and hardware development and in-circuit emulation is available as an option for the company's System 65 microcomputer development system.

Synertek is second sourcing the 1-chip microcomputer, which comes with either a 2- or 1-MHz internal clock. Quantity prices for production devices are under $10 for both models. Single-unit prices for the emulator are $75 for the 1-MHz model and $95 for the 2-MHz version.

Circle 437 on Inquiry Card

Small Business µComputer Systems Operate in Timesharing Mode

MicroStar 55 small business desktop systems consisting of a 12" (30.5-cm) video display, dual double-sided floppy disc drives (1.2M bytes), MicroStar 10 single-board computer, 48k-byte RAM, and detached typewriter keyboard with numeric pad can be configured as a data communications terminal or work station. The microcomputer board contains an Intel 8085A microprocessor, floppy disc controller, RAM, realtime clock, DMA, and priority interrupt supporting circuitry. It supports up to three users in timeshare mode, with two external RS-232 ports and a serial port for video display terminal.

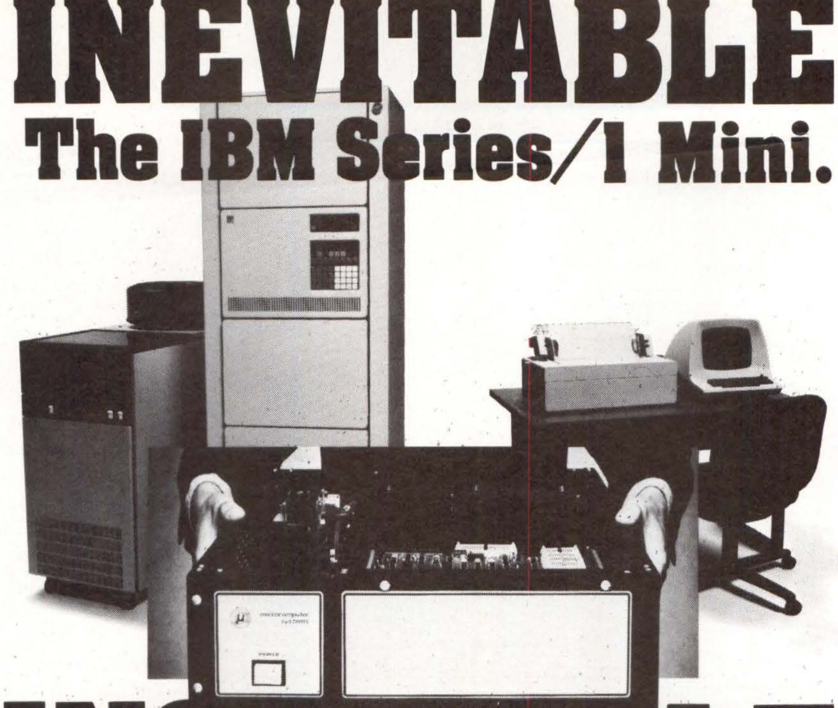
Micro V Corp, 17777 SE Main St, Irvine, CA 92714 has developed the $11,895 system to be programmed in ENGLISH II, which enables special reports to be generated. STARDOS and CP/M operating systems are supported.

Circle 438 on Inquiry Card

Imaging System Has Video I/O for Display Of Graphics and Text

Consisting of two standard size S-100 boards, the CAT-100 is a general

INEVITABLE
The IBM Series/1 Mini.



INCREDIBLE
The MSC-1200 Controller.

It seems that, every day somewhere in the computer industry, somebody does something that catches a lot of folks off balance.

Except for one. IBM.

No one is ever surprised by anything IBM decides to do. One anticipates as best as possible. Accepts. And adjusts.

So it was when IBM announced its Series/1 minicomputer last year. So too will it be, almost certainly, when Series/1 comes to dominate the marketplace it has entered.

IBM. Inevitable Business Machines.

An incredible controller for the inevitable mini.

We call it the MSC-1200. It could be called "the great go-between." Whatever you call it, the MSC-1200 is *the solution* to harnessing big capacity disk drives to the IBM Series/1.

For many reasons. *First, the 1200 is totally transparent to IBM's operating systems.* That means no expensive, time-consuming, error-prone corruptions of IBM's operating software. Simply plug in the MSC-1200 host adapter on one side and up to four high density drives on the other. And that's it.

Second is flexibility. Microcomputer Systems doesn't lock you into one manufacturer's drives or one particular drive technology. Be it removable or Winchester fixed media, using Ampex, Memorex, CalComp, CDC, Microdata, Okidata or Kennedy, no matter. The 1200 solution from MSC can accommodate them all.

A proven performer. Loaded with features.

The 1200 is the latest of Microcomputer Systems' Series 1000 controllers. In the last three years, Series 1000 has proven itself—in a wide range of minicomputer operating systems and with an installed base of over 1000—to be the most maintainable and reliable in the industry. The reason is simple. Because the reason is simplicity. Modular, single board construction. Low parts count. On-board microdiagnostics. Low stress design on all quality components. These features account for both enhanced MTBF and the negligible Series 1000 downtimes that have been experienced.

And yet, for all of its simplicity of design, the list of operational features is as impressive as its performance record. Error correction. Sophisticated channel techniques. Automatic self-test. Logical to physical drive correlation.

In the minicomputer marketplace, Series/1 is the comer. It's inevitable. And the MSC-1200—thanks to its transparency, data integrity, reliability, maintainability and price—is the controller. It's incredible.

Microcomputer Systems

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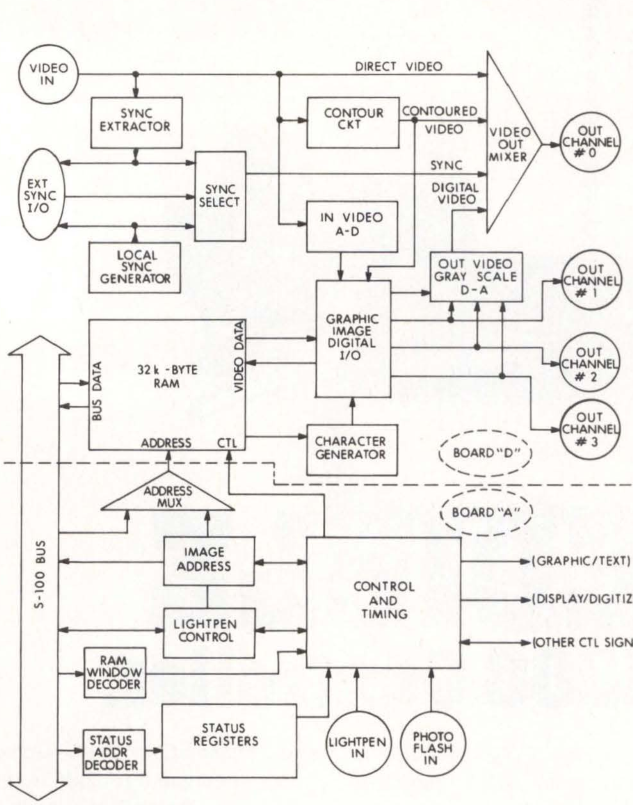

Digital Graphic Systems' CAT-100 video interface system on two boards allows any S-100 bus microcomputer to input and output standard video signals at maximum video rate. Basic system configuration has 32k bytes of RAM. Also featured are lightpen input, eight status registers, resolutions to 512 x 512, and variety of modes including graphics, text, and photo

purpose video imaging system for the S-100 bus. It features resolution to 512 x 512, multimode graphic and text display with video I/O mapping functions, and built-in frame buffer capability. Any standard NTSC video input up to 6-MHz bandwidth is accepted and digitized. Output data rate is 50M baud. The digitized image is mapped into the built-in 32k-byte RAM buffer.

Also featured are gray scale to 16 levels, realtime contouring operation, 4 video output channels, 6 text formats, and lightpen input. Digital Graphic Systems, 595 Matadero Ave, Palo Alto, CA 94306 offers extension capabilities of enhanced gray scale, color output, realtime analog video operations, and software in ROM.

Circle 439 on Inquiry Card

Flexible Disc Drive System Doubles Online Storage Capacity

The icOM® FD3812 dual-density, flexible disc system features a built-in formatter and controller, two disc drives, a power supply, and cabinet, providing increased storage capacity. Full sector R/W buffers allow asynchronous data transfer. DMA data transfer is optional. Diskette write protect and operation of up to four drives by one controller are also included. Disc formats are IBM Diskette 1 single density or IBM Diskette 2D dual density.

Pertec Computer Corp's Microsystems Div, 20630 Nordhoff St, Chatsworth, CA 91314 is aiming the system at OEM and development laboratory markets. Price will be approximately $2300 in OEM quantities of 100.

The controller responds to 8-bit command words to transfer data, initiate DMA data transfer, or transfer buffer contents. Commands are also used to seek data tracks and format the diskette.

MTBF exceeds 2300 h. Disc speed is 360 r/min with 10-ms track to track access time, 40-ms head load time, 5-ms sector R/W time, 83-ms average latency time, 700-ms automatic head unload time, and 1-ms interrecord time. Power requirements are 100/125 Vac, 60 Hz, 200 W maximum. Interfacing uses icOM plug-in interface and software, with up to 1.2M-byte online storage packages for most microcomputers.

Circle 440 on Inquiry Card

Faster Floppy Disc System Interfaces With S-100 Bus Microcomputers

The S-100 disc system from Info 2000 Corp, 20630 S Leapwood Ave, Carson, CA 90746 combines the PerSci model 277 dual diskette drives with the company's DISCOMEM disc controller board and Digital Research CP/M to provide all hardware and software needed for operation with any S-100 bus computer. Two spindles accept standard soft-sectored 8" (20-cm) flexible diskettes. The system is compatible with IBM 3740 format. Voice coil positioning is used in the drives to provide faster seek times.

The DISCOMEM board also contains I/O interfaces: two RS-232 serial interfaces with software selected baud rates from 50 to 19.2k bits/s, three 8-bit TTL level parallel interfaces, and provision for 8k of EPROM or for 7k of EPROM and 1k of scratchpad RAM. These I/O facilities allow the board to be combined with two other S-100 logic boards (CPU and 32k RAM) to create a complete disc based microcomputer system.

Circle 441 on Inquiry Card

You won't believe our Ballistic™ Printer until you see one in print.

And in person.

Unless you've been in hiding, you've probably heard about LSI's family of Ballistic Printers. Built with the same proven dependability of the Dumb Terminal and his Smarter Brothers.

Our latest matrix printer, the 200A, comes with standard features like a Space and Blank Character Compression Buffer. Tabbing over Blank Spaces ability. Half Duplex or Full Duplex Operation. And a fully buffered input, optionally expandable to 1024 characters. Not to mention its microprocessor versatility, and firmware flexibility.

To top it off, you can choose from options like Serial, RS232, Parallel, and Current Loop interfaces. Polling. X-ON, X-OFF. And elongated character capability with a choice of either 10, 12 or 16.5 Pitch.

The Printer's reliability lies in the simplicity of its patented Ballistic head. Which ballistically propels the matrix wires to assure longer head life. Eliminating tube clogging with inks, dust, and paper fibers. Even wire tip wear is substantially reduced.

The Ballistic Printer uses a five-start lead screw and servo to print bi-directionally at 180 cps. Direct, simple, positive. And very accurate.

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Ease of Operation Is Key to Business Computer System

The Tandy 10 business computer system, introduced by Radio Shack, a Tandy Corp Co, PO Box 2932, Fort Worth, TX 76101, consists of a workstation with diskette drives integrated into a metal desk, and separate 60-char/s matrix printer. The workstation includes a video display, standard typewriter keyboard, 10-key calculator pad for numeric entry, and 15 keys for data editing.

Each diskette holds up to 256k characters; internal memory capacity is 40k characters. Screen formatting language allows user prompting for data input. Extended BASIC comes with the system. FORTRAN IV and assembly level program languages, as well as other peripherals, are optional.

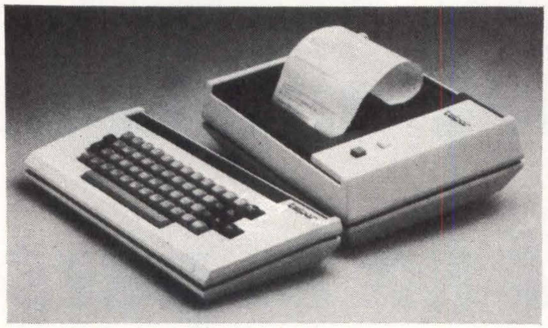
Circle 442 on Inquiry Card

Industrial Memory Module Provides High Density/Low Power

The CM4505 EPROM module serves a variety of industrial applications due to the fact that it provides for up to 65k bytes allowing reallocation of slots from memory to I/O—doubling the I/O capability—while dissipating less than 10 W of power. To supplement the MicroPac 80A line of microcomputers, Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176 has made the module TTL compatible, with oncard voltage regulation, switch selectable base starting address, switch selectable socket enable/disable, 16-bit address decoding logic, and provisions for choice of three EPROMS (2758, 2716, or 2732) with 16 sockets to be used as needed.

Circle 443 on Inquiry Card

Full-Duplex, Bit Serial I/O Terminal Provides Thermal Printing



Telpar's PS-48C interactive thermal printer also serves as full-duplex, bit serial I/O terminal with addition of optional keyboard

The PS-48C printer is a 48-column, self-contained ASCII coded device utilizing an F8/3870 single-chip microprocessor as system interface and controller. Modes of operation are TTL parallel or serial, RS-232-C serial, and 20-mA loop serial. Signaling rates are 110 or 300 baud in serial mode and up to 960 char/s in parallel mode. It operates interactively, printing one character at a time as they are received. Print format is a 5 x 7 dot matrix; throughput rate is 24 char/s.

Formatted for teletypewriter and typewriter capability, the KB-59C keyboard interfaces to the printer, resulting in a full-duplex, I/O terminal with bit serial I/O. Keyboard, printer subassemblies, printing mechanism, interface board, and power supply are offered separately by Telpar, Inc, 4132 Billy Mitchell Rd, PO Box 796, Addison, TX 75001 for OEMS.

Circle 444 on Inquiry Card

Integrated Microcomputer Features Display, Keyboard, and Software

An 8085 microprocessor, 32k or 64k RAM, two 5.25" (13-cm) floppy discs,

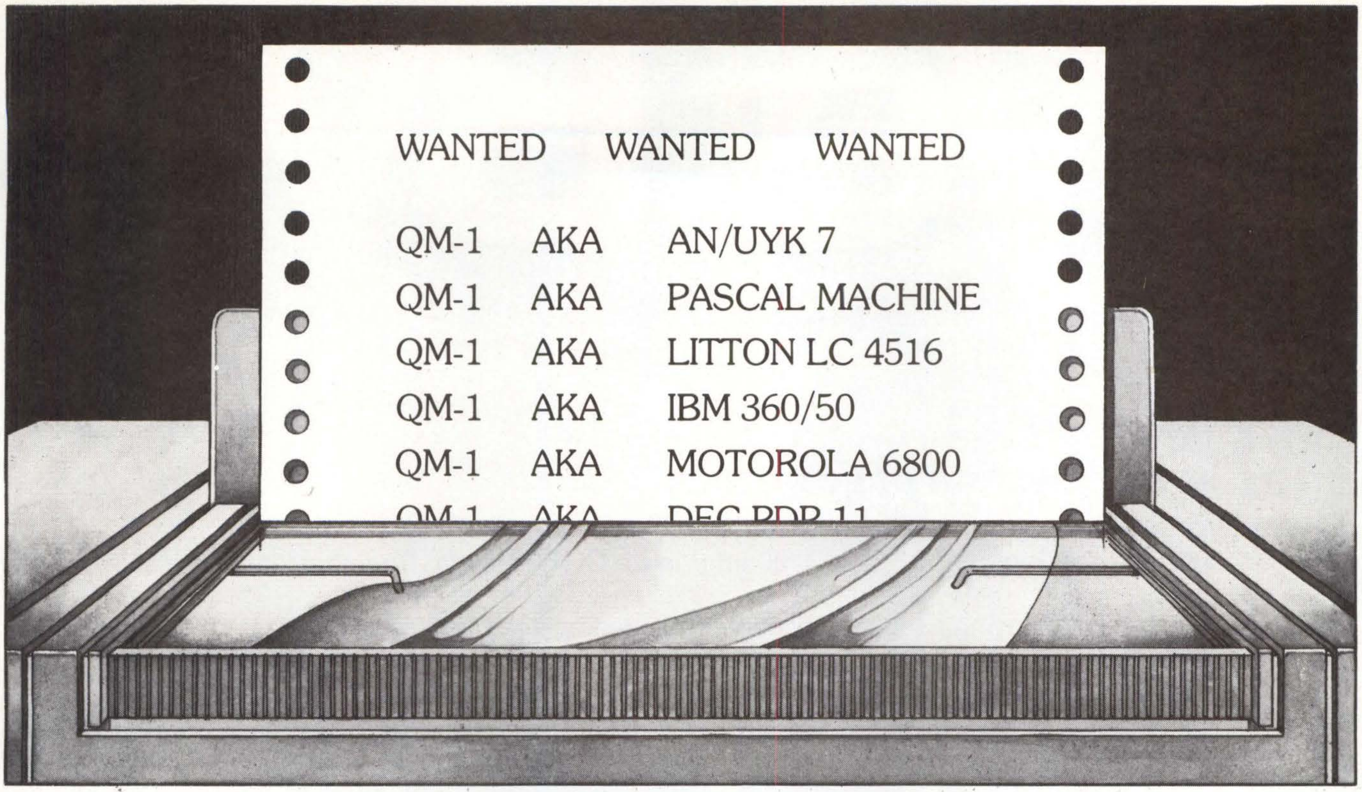
IMSAI's VDP-40 microcomputer in single cabinet for small business uses and development is based on Intel's 8085 CPU. Other components of expandable unit are video display, floppy disc drives, and keyboard

a 24-line x 80-char 9" (22.9-cm) CRT, heavy duty power supply, programmable keyboard, motherboard, and serial and parallel I/O ports have been incorporated by IMSAI Manufacturing Corp, 14860 Wicks Blvd, San Leandro, CA 94577 into the video data processor. VDP-40, priced at $4500, is designed for small business functions, systems development, and use as a terminal in a data communications network.

Software includes a disc operating system text editor, Extended and Commercial BASIC, relocatable assembler, linkage editor, and ANSI Level 2 FORTRAN IV. IMDOS, the company's floppy disc operating system, contains the 8080 assembler, text editor, debugging program, and floppy disc system diagnostic program.

Two optional double-density disc controllers can be supported, expanding the disc capacity to 5M bytes. Up to two miniature floppy drives and four floppy drives can be handled. Features of the CRT display include insert/delete, user programmable character set, protected fields, inverse video variable fields, and a 14-MHz bandwidth. The microprocessor controlled keyboard has N-key rollover, user defined special characters, and linedrawing characters.

Circle 445 on Inquiry Card



The QM-1 Also Known As The Emulator

The "computerhunt" for a single machine that can service a wide range of needs in a development laboratory ends with Nanodata's QM-1, The Emulator. The QM-1 can assume the identity of any computer, becoming exactly like the emulated machine down to the most minute detail.

Software developed on the QM-1 will run unchanged on the emulated machine and vice versa. What is more, the QM-1 can change identities as often as the user chooses.

Challenges that the QM-1 has met include digital design verification, critical software validation and hardware/software trade-off analysis. Whatever the specific computer requirements — general purpose, avionic, military, minis, imbedded micros or HOL machines — the QM-1 can satisfy them.

A typical QM-1 configuration costs approximately $300K. A cost-effective investment considering that emulators on the QM-1 have been benchmarked at speeds 35 to 100 times faster than simulators on multi-million dollar systems.

Talk to Mike Senft, Marketing Director, about specifics.

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Bye, Bye I

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If you buy a DECwriter after reading this ad, you deserve it.

Our popular Pussycat Printer and Model 1100 Interactive CRT Terminal. Together, they do a lot more than a DECwriter III and cost less.

In fact, at $1795, it's like buying a top-quality printer and getting a terrific little CRT free.

And what a CRT! The Model 1100 displays 80 characters per line in an easy-to-read 9 x 12 matrix and communicates at up to 9600 baud. Compare that to DECwriter III's puny 1200 baud.

Then when your results are ready, touch the PRINT key and the Pussycat printer lays down a whole screenful of characters in only 20 seconds. But, best of all, the CRT is ready for use again in 2 seconds or less. So the operator can go right back to work.

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Clean. Quiet. Inexpensive. The Pussycat Printer and the Model 1100 CRT from Perkin-Elmer. Compared to a DECwriter III, they do more and cost less.

*U.S. domestic price, quantity 75. See distributor (listed on the following page) for smaller quantities. Model 1100 and Pussycat Printer: $2795, quantity 1. Owl-1200 and Pussycat Printer: $3695, quantity 1.

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$2395*

A Perkin-Elmer editing CRT with line drawing and a 100 cps thermal page printer.

You can also plug the Pussycat Printer into our Owl-1200 Terminal and have a powerful editing terminal with forms drawing capabilities and hard copy, too.

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Or contact any of the Perkin-Elmer Data Systems sales and service centers or Full Service Perkin-Elmer Distributors listed on the following page. For more information, write Terminals Division, Route 10 and Emery Avenue, Randolph, New Jersey 07734 or telephone toll free.

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IEEE-488 Bus Interface Adds Flexibility at Low Cost to μComputers

The MEE-888 GPIB, which meets the requirements of IEEE Standard 488, has been added by Control Logic, Inc, 9 Tech Circle, Natick, MA 01760, to its M-Series line of modular microcomputers. Functions of talker, listener, and controller are accomplished using this $495 interface with the appropriate controlling software. It may be added to any existing M-Series system, either Intel 8080 or Zilog Z80 based, having up to 64k of memory in any combination of RAM (1k and 4k boards) and EPROM (2k, 2708 or 8k, 2716).

Circle 446 on Inquiry Card

Three μComputers Range From OEM to Intelligent, General Purpose Systems

A family of MCZ microcomputer systems—presently consisting of three models—has been introduced by Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014. A desktop, OEM oriented system, MCZ-1/05 uses the Z80 CPU and 16k dynamic RAM chips. It also includes two dual floppy disc drives with 600k bytes of online data and program storage, the Z80-MCB microcomputer board, and Z80-MDC memory disc controller board. Two open slots allow additional I/O expansion.

Main memory capacity is 64k bytes of RAM, with 3k bytes of P/ROM and 32k bytes of RAM. Also featured is a serial I/O port with RS-232-C or strappable current loop interface. The computer sells for $4750 in single quantities. A serial matrix printer interface and four serial I/O channels are optional.

An intelligent terminal with 4k bytes of RAM expandable to 52k bytes, a general purpose computer with 32k bytes of RAM expandable to 64k bytes, a 9" (23-cm) CRT, and rackmounted floppy disc drives providing 600k bytes of online program and data storage have been added to the basic system to form the MCZ-1/60 desktop system. Selling for $6990 in single quantities, the system is available in a version with desktop disc drives (MCZ-1/62). It provides the OEM with a high performance, low cost microcomputer system for general business applications.

MCZ-1/60 microcomputer implements an intelligent terminal and general-purpose computer in single enclosure. Two other members of Zilog family are MCZ-1/90 system offering intelligent terminal with keyboard and video monitor, general-purpose computer, and 10M-byte drive; and MCZ-1/05 OEM microcomputer containing Z80 CPU and 16k dynamic RAM chips

User interaction is via the CRT monitor with 24 lines x 80 char and a graphic mode, and a detached keyboard with 128 ASCII u/lc char, 10-key numeric pad, and 13 user definable function keys. Other features are dual Z80-MCB boards, Z80-MDC board, Z80-VDB video board, and six open slots for I/O expansion. Both of the systems are supported by COBOL, PLZ, BASIC, and FORTRAN IV, all of which run on the company's RIO operating system.

The final system MCZ-1/90 further expands the line by including 10M bytes of moving head disc storage for main file management run by a separate Z80 microprocessor. Additional storage is obtained from two single-sided removable minifloppy discs. Using three Z80 CPUs, the computer sells for $16,800. It supplies OEMs with expanded storage for use in medium-scale business data processing applications.

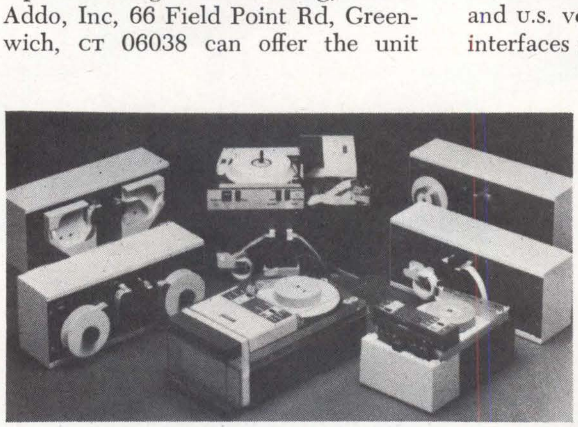
The major variation between the 1/90 and 1/60 is the file management performance increase of the former system. This is enabled because part of the operating system is downloaded to 16k of high speed static memory in the disc controller. Data transfer to and from the moving head disc and static memory in the disc controller is handled by the Z80-DMA circuit, producing high speed DMA.

Circle 447 on Inquiry Card

Compact Paper Tape Reader Operates At Low Speed

Reading up to 120 char/s with a compact mechanism containing only one moving part, the 4030 is an optical, bidirectional reader for 5-, 6/7-, and 8-track tapes with up to 60% transmissivity. By separating tape handling from reading, Facit-Addo, Inc, 66 Field Point Rd, Greenwich, CT 06038 can offer the unit with four interchangeable tape handlers: 4008 lock pin unit for tapes shorter than 65 ft (19.8 m), 4009 supply wheel for 65 to 165 ft (19.8 to 50 m), 4013 servo spooler for up to 330 ft (100.6 m), and 4019 tape bin for fanfolded tapes.

Combined with the 4070 tape punch, the reader forms the 4040 Combi with control panel, but separate interfaces. Six standard European and U.S. versions of serial and parallel interfaces are available.



Low speed 4030 tape reader from Facit-Addo can be equipped with tape handling mechanisms for four tape lengths or fanfold. Clockwise from left are two 4030 units, 4040 high speed punch and reader combination unit, two other 4030 units, 4020 high speed reader, and 4070 high speed punch

Circle 448 on Inquiry Card

COBOL Extends Facilities to Meet Microcomputer Needs

Designed for microcomputer, small business system, and terminal user markets, especially for those who wish to develop programs on their own machines, Intel 8080 CIS (Compact Interactive Standard) COBOL includes such extensions as advanced data entry facilities, runtime input of file names, line sequential files, hexadecimal literals, rapid development facilities, lower case, and interactive debugging. During the program development cycle, the programmer uses his editor to provide a source file.

A command loads the single-pass compiler to convert the source program to a compact intermediate (object) code. Another command loads the Runtime System, which in turn automatically loads the application program. Compilation errors can be corrected on the list file, and then resubmitted to the compiler as a source file. In addition, Micro Focus Ltd, 18 Vernon Yard, Portobello Rd, London 11 2DX, England is offering an ANSI 74 compatibility option.

Circle 449 on Inquiry Card

Multilevel System Offers Concurrent Operation and Disc Operating System

Providing both edit and realtime program areas that run concurrently, BASIC & DOS of Heurikon Corp, 700 W Badger Rd, Madison, WI 53713 also incorporates a disc operating system with efficient file management. Running independently from the keyboard and program editing functions, realtime programs are given highest operating priority and may be started automatically in response to external stimuli. Edit area programs will be interrupted to service realtime operations. When the realtime program finishes, control returns to the edit program.

File management architecture allows variable length files to be cataloged on the diskette. For maximum utilization of the diskette area, sectors are attached to the end of a file as they are created or modified, and returned to the available space pool when available.

The system runs the company's MLZ-80 microcomputer system (see *Computer Design*, Feb 1978, p 158) and is Intel SBC Multibus compatible. It comes on diskette or in EPROM.

Circle 450 on Inquiry Card

Three Software Packages Facilitate Use of Z80 Microcomputers

A software Disc BASIC interpreter XDB™, a dynamic software debugging utility Z BUG, and a LINKER utility program for binding individually compiled modules into a single program have been announced by Xitan, Inc, 1101-H State Rd, Research Pk, Princeton, NJ 08540 for use with Zilog Z80 microcomputers using a Digital Research CP/M™ disc operating system in at least 32k of memory. Using only 18k, XDB supports a console, reader, punch printer, and multiple disc files. Capabilities provided include LOAD GO commands, TRACE function, privacy statement, intercepting error conditions, and global editing. With faster execution, the software supports additional mathematical and string functions as well.

Z BUG extends techniques for developing assembly language programs with the addition of user controlled data formatting, flexible trap capabilities with tracing, and powerful expression evaluation of user entered data. Requiring 13.25k bytes, the utility provides for specifying the RADIX for three types of data and displaying the next instruction before execution; it also has six commands for memory data manipulation.

Operating faster than recompiling, LINKER features assigning of absolute memory address to each module segment, relocatable code in each segment, and use of a SUBMIT file. Each compiled module may access code and data defined in other modules. □

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TECHNOLOGY STATUS REPORT ON RECENT NMOS PROCESSES

Scott Smith and Eric R. Garen
Integrated Computer Systems, Inc, Santa Monica, California

Metal-oxide semiconductor technology has long been the mainstay in fabricating complex semiconductor circuits such as high density memories and microprocessors. Its appeal is based on easy fabrication processes in generating transistors plus the simplicity, low power dissipation, and small size of its logic circuits.

Several semiconductor manufacturers are continuing intensive research and development efforts to obtain even greater performance from metal-oxide semiconductor (MOS) technology, maintaining a general evolution toward ever smaller MOS devices. Two of the promising developments evolving from these efforts are the HMOS and VMOS processes being developed by Intel Corp and American Microsystems, Inc, respectively. HMOS is an acronym for high performance MOS, while VMOS stands for V-groove (or V-shaped groove) MOS. Both are n-channel processes.

Scaling Down MOS Devices

Prior to the development of HMOS, the size of the transistor itself was not reduced; instead, the width of the interconnecting conductors was narrowed to increase circuit density. Beginning two years ago, Intel engineered the technique necessary to reduce the transistor size itself while maintaining, or even improving, performance and reliability. HMOS is the technique of increasing performance in digital chips by scaling down the size and pa-

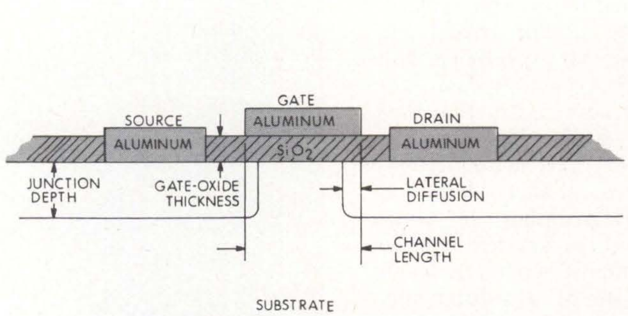

Fig 1 MOS transistor. By scaling down each physical dimension and by increasing substrate doping level, HMOS offers substantial improvements. First, increasing doping of substrate increases channel resistivity. This results in lower junction capacitance and reduced substrate effects, while increasing effective carrier mobility. Reducing gate-oxide thickness increases gain and punch-through voltage, and reduces body and short channel effects. Reducing channel length results in reduced gate capacitance and improved speed and density

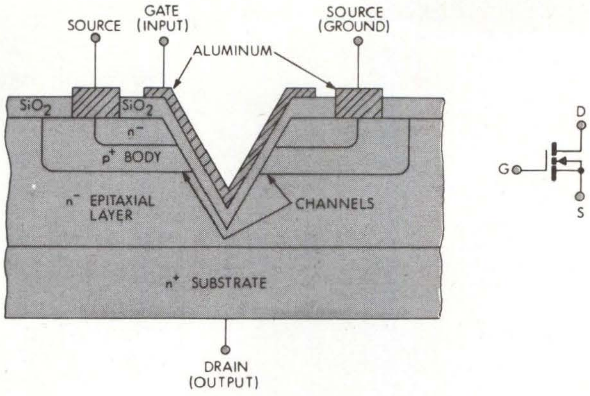

Fig 2 Cross-section of VMOS channel. Device is manufactured by depositing layers of differently doped semiconductor material on n^+ substrate. Channels are formed by etching V-groove into n^- epitaxial layer such that p^+ material adjacent to groove becomes channel. Gate is formed by depositing insulating layer of silicon dioxide followed by layer of aluminum

rameters of the individual MOS devices (transistors, diodes, resistors, and capacitors).

Furthermore, with smaller devices, the manufacturer has the choice of making the chip die smaller (and lowering the cost by getting more dice per wafer), or of putting more devices on a given die size. Intel and several other NMOS suppliers are concentrating on this evolutionary approach because (in addition to providing higher yields from smaller die sizes) it evolves directly out of standard silicon processing, requiring neither new device structures nor new circuit schemes.

Scaling down of MOS transistors involves several linear dimensions, as illustrated in Fig 1. The HMOS technique reduces each of the following parameters by a scaling factor, S: channel length, gate-oxide thickness, junction depth, and lateral diffusion. Original gain of the device is restored by multiplying the substrate doping level by S. These changes reduce the device size, providing greater density.

Increased speed is obtained by also reducing the supply voltage by a factor of S. Together with the previous parameter scalings, this reduces the supply current, parasitic capacitance, and gate delay by the same factor. Further benefits are that the power dissipation is reduced by a factor of S^2 and the power-delay product is improved by a factor of S^3. Table 1 illustrates these benefits with a side-by-side comparison of NMOS and HMOS versions of the 2115 RAM.

Although faster speeds, better densities, and lower power levels are benefits of scaling down, some disadvantages are incurred. Improved semiconductor fabricating facilities are required, including the ability to build more finely patterned geometries, produce thinner and purer oxides, improve isolation methods, and increase control of metalization and alignment. As the devices shrink and become more dense, care must be taken to design against nonideal device laws and second-order effects. Also, the benefit of a reduced power requirement carries with it the problem of necessary reductions in power supply voltages. With 5 V widely accepted as a primary supply voltage, users may be unwilling or unable to switch to the 2 to 3 V that HMOS will demand by 1980.

VMOS Technology

Unlike HMOS, VMOS is an altogether new technique combined with conventional MOS processes. Formally, VMOS is defined as "an anisotropically-etched, double-diffused MOS process." In simpler terms, this means that a special solution is used to etch grooves having a V-shaped cross-section through several epitaxial layers to fabricate transistors (Fig 2).

The substrate consists of n-doped silicon, which is connected as the common drain to all of the transistors in the wafer. Then, the following layers are deposited in succession: (a) a less heavily doped n-layer, (b) a p-type layer, and (c) a layer of n-material. The gate structure is created as follows. First mask is applied so that a small rectangular area is exposed to a special etching solution. This etching solution has the special (anisotropical) property of attacking the silicon as a crystal; ie, it dissolves the silicon along the crystal structure. The crystal structure is such that the etching causes a "V" pattern to be formed. When the bottom of the V has been formed, the etching automatically stops. Then an insulating layer of SiO_2 is deposited across the surface of the chip except for the junction of the n and p wells, which will form the source. Finally, aluminum is deposited to form the gate (as shown) and to provide the source connections.

This VMOS structure behaves as an n-channel enhancement mode MOS field-effect transistor (MOSFET). When the device is off, the drain is positive with respect to the source, resulting in a reverse-biased junction through which no appreciable current flows. If, however, a

TABLE 1

Comparison of Equivalent NMOS and HMOS Versions of Intel's 2115 High Speed 1k Static RAM

Parameter	1976 (NMOS)	1977 (HMOS)
Channel length (μm)	5	3.3
Gate oxide thickness (Å)	1100	700
Die size (mil^2)	18,500	10,200
Typical access time (ns)	45	22

TABLE 2

Comparison of 4k Static RAM Fabrication Technologies

Technology	Classification	Mfr	Model	Config	Speed (ns)	Power Dissipation (mW)
HMOS	MOS	Intel	2147	4k x 1	55/70*	900(150)/800(100)*
VMOS	MOS	AMI	2114	1k x 4	120	250
I^3L	Bipolar	Fairchild	93481	4k x 1	100	450
NMOS	MOS	National	8255	1k x 4	250	462
Bipolar	Bipolar	TI	74500/01	4k x 1	75	500

*HMOS device has two speeds and two power dissipations; standby power when chip deselects is shown in parentheses

positive voltage is placed on the gate with respect to the source, electron carriers are induced from the source into the P+ body (the channel) through their attraction to the gate. Once in the channel, the electrons are attracted to the positive drain, and current flows.

The advantages of VMOS over conventional MOS technologies derive from the vertical alignment of the MOS transistor. Because it is easier to control the depth of a deposited material than to maintain the lateral dimensions of the masking process, the length of the channel is closely controllable. Shorter channel lengths are possible, resulting in reduced capacitance and higher speed. Futhermore, arranging the transistor in a more vertical orientation results in a more compact transistor, which, in turn, allows greater device density without scaling. Indeed, scaling may be applied to already dense VMOS devices to achieve even greater density.

A primary disadvantage is that, being a new transistor fabrication process, VMOS requires extensive mask redesign to fabricate existing chips. Thus, it is primarily interesting for new chip design, rather than size (and cost) reduction of existing chips. Furthermore, the VMOS structure somewhat increases the processing complexity and requires new or adapted fabrication equipment to handle both diffusion and the V-groove etching.

Impact of Technologies

It is the general practice of semiconductor manufacturers to use memory circuits as the initial proving grounds for new fabrication methods. Both Intel and AMI have introduced 4k static RAMS using HMOS and VMOS, respectively. Intel's HMOS 2147 (a 4k x 1 device) is available in two speeds. The faster version has a 55-ns access time and draws 180 mA (30 mA in standby); the slower version runs at 70 ns and draws 160 mA (20 mA standby). Each has a special feature that causes it to go into standby mode whenever it is deselected, thereby saving significant power. Intel is also using this technology for the 8086 16-bit microprocessor. Not only does HMOS enable the 16-bit processor to be built on a single chip, the processor will be significantly faster than conventional NMOS circuits. It will execute a (16-bit) register-to-register addition in 600 ns, compared with the typical 1300 to 2500 ns of present 8-bit NMOS microprocessors.

AMI's 2114 is a 1k x 4 VMOS device. It features a typical delay of 120 ns at 50 mA. In addition, AMI is building 1k static RAMS to compete with bipolar devices; the VMOS 4015 and 4025 operate at 60 and 45 ns, respectively. Supply current for both devices is a respectably low 125 mA.

The values for 4k RAM speeds and power are interesting to compare with other semiconductor technologies. Fairchild is pursuing higher performance RAMS utilizing isoplanar integrated injection logic (I^3L) while RCA and Hewlett-Packard are using CMOS on sapphire (SOS). Table 2 presents the characteristics of some 4k static RAMS that use the various new technologies. Based on these first commercial devices, it appears that both VMOS and HMOS technologies compete very strongly with I^3L, SOS, and other non-NMOS technologies. It remains to be seen if a single dominant technology will emerge, but first indications are that all can result in significant cost and performance improvements.

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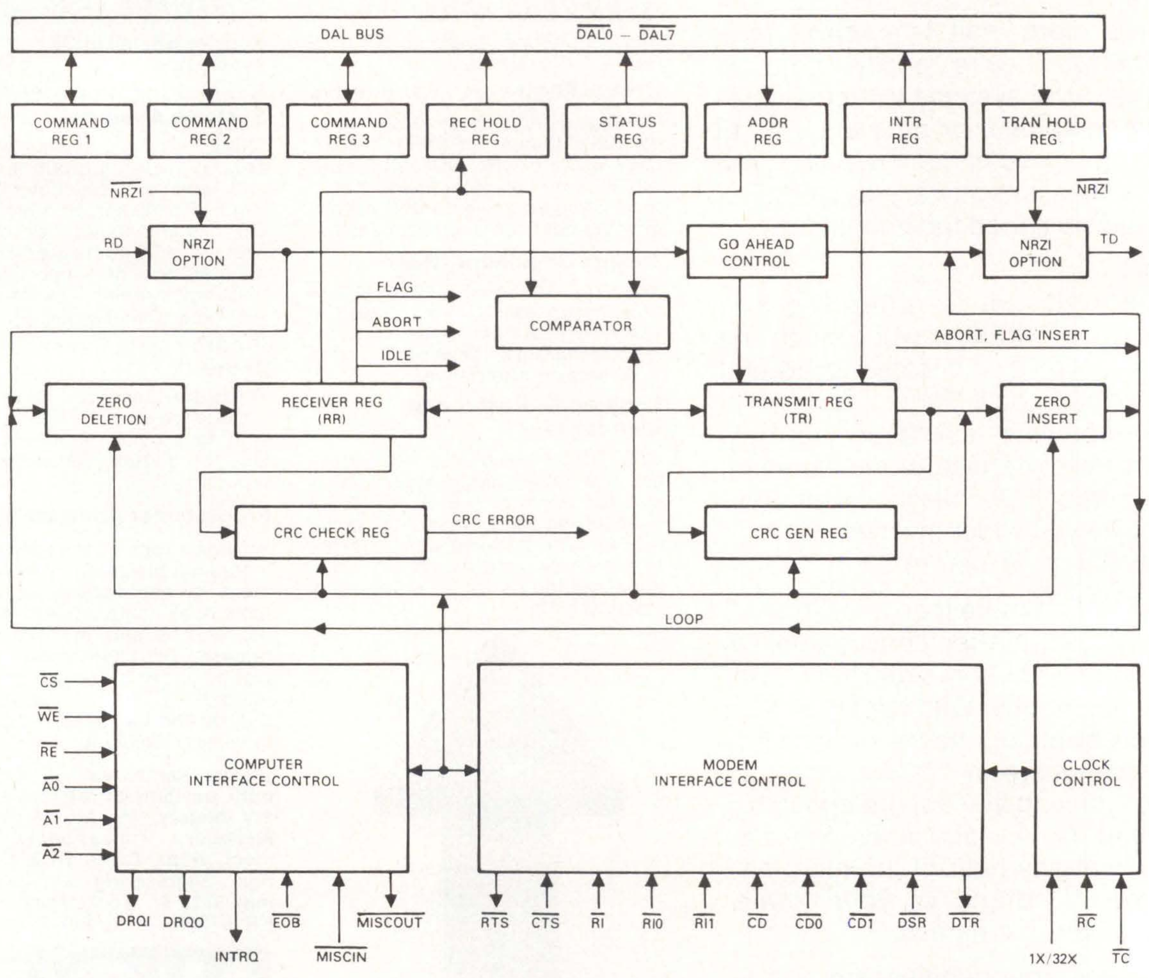
Fully TTL Compatible SDLC Chip Replaces 70 Logic ICs in Data Communications Applications

An NRZI encode/decode option, a digital phase lock loop when in 32X mode (an option), and a baud rate claimed to be three times faster than previously achieved (dc to 1.5M bits/s) are unique features of an MOS LSI programmable synchronous data link controller recently introduced. The SD 1933, from Western Digital Corp, 3128 Red Hill Ave, Newport Beach, CA 92663, uses SDLC line protocol to interface parallel digital systems to synchronous serial data communications channels. It is fully compatible with IBM, HDLC, and ADCCP specifications and the manufacturer claims that in some data bus applications the device will replace nearly 70 currently used logic ICs.

SDLC protocol includes zero insertion and deletion, CRC generation and checking, and automatic detection and generation of special control characters (eg, FLAG, ABORT, INVALID, and IDLE). A direct memory access mode is available, and the device is directly compatible with the company's DMA controller, the 1833. Double buffering of data enables the receiver buffer to hold data and status information while the transmitter buffer holds data and control information.

With NRZI option, the transmitter encodes transmitted data to NRZI format; since the receiver expects NRZI data, it decodes the NRZI encoding. In NRZI encoding the output remains in the same state to send a binary 1 and changes state to send a binary 0.



Block diagram of Western Digital SDLC organization. Chip is TTL compatible on all inputs and outputs. Only a single 5-V power supply is required. Options include end-of-block facility for transmitting blocks of data during a frame, 1X/32X transmission, NRZI, and go ahead control which allows chip to operate as data repeater

(Continued on p 166)

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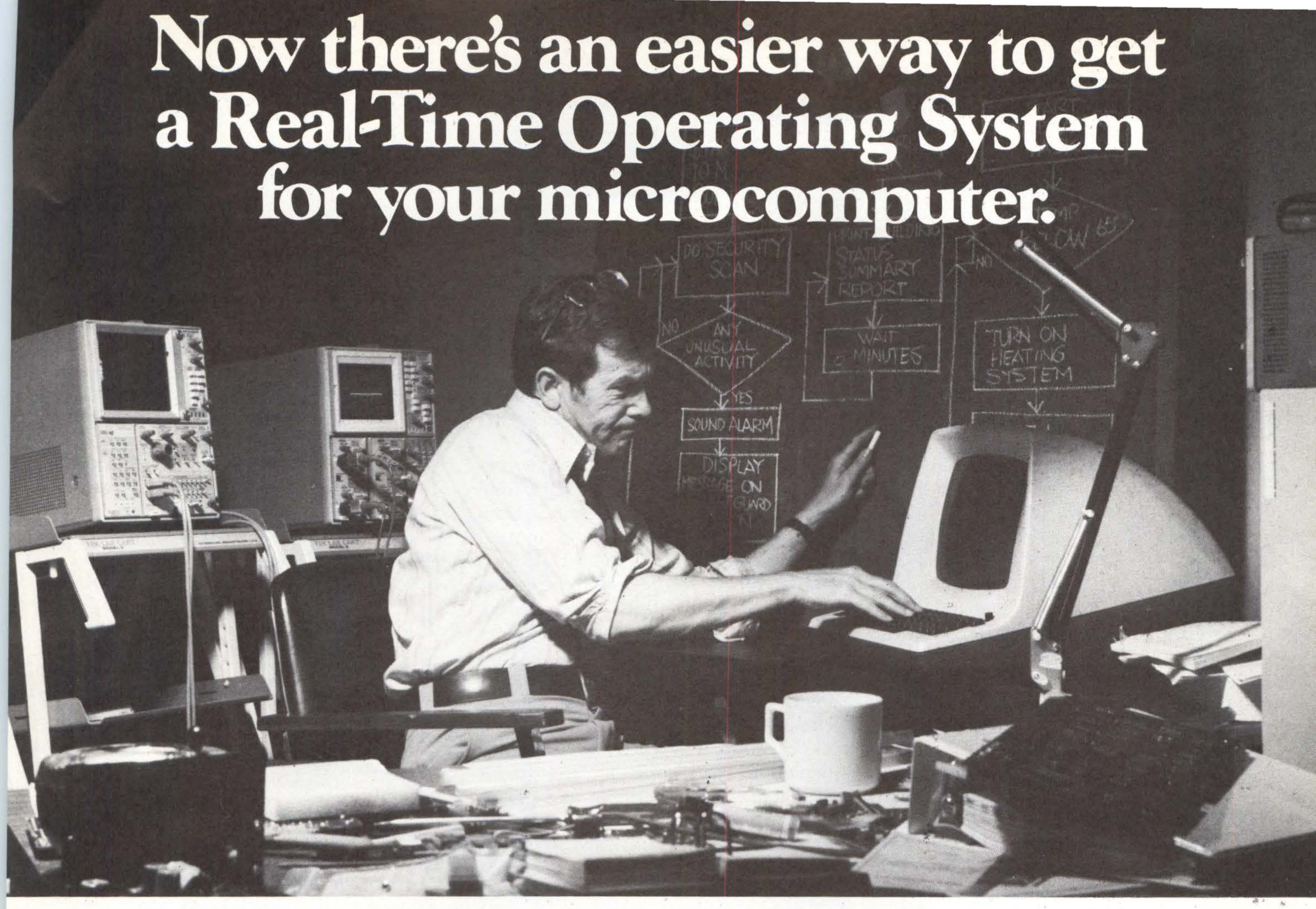

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CIRCLE 73 ON INQUIRY CARD

Using the 1X/32X option, when high the chip expects 1X clocks (both receiver and transmitter) and will send data accordingly. When low, the chip expects 32X clocks and will generate 1X clocks. The receiver synchronizes its 1X clock to each data transition. Transmitted data change on the rising edge of TC (transmit clock) and received data are sampled on the falling edges of RC (receive clock).

Other capabilities include an end-of-block facility, and a go-ahead option. End-of-block, used when blocks of data are transmitted during a frame, causes the frame check sequence to be executed upon completion of the present command. The go-ahead option allows the chip to operate as a data repeater with a 1-bit delay between receiver and transmitter, permitting the device to be used as a secondary station in a loop configuration.

An 8-bit receiver register (diagram) inputs received data at a clock rate determined by the receiver clock. Incoming data are assembled to a 5-, 6-, 7-, or 8-bit character length and then transferred to the receiver holding register (RHR). At this time, data request input (DRQI) is made active, informing the computer that the RHR contains data.

The 8-bit parallel receiver holding register presents assembled receiver characters to the bidirectional data access lines (DAL) bus when activated via a read operation. When the RHR is read by the computer, DRQI is made inactive.

An 8-bit comparator compares contents of the address register with the address field of the incoming frame. This is enabled by a bit in the command register. If enabled and there is a match, the received frame is input and DRQIS are generated. If enabled and there is not a match, the received frame is discarded. If not enabled, all received frames are input to the computer.

The 8-bit transmitter holding register (THR) is loaded with data from the DAL by a write operation. Data request output (DRQO) is also reset by the write operation. Data are transferred to the transmitter register when the transmitter section is enabled and the transmitter register is ready for new data. During this transfer, DRQO is made active, informing the computer that the THR is again empty.

This chip, fabricated in n-channel depletion load MOS technology, is available in both ceramic and plastic packages. Its 8-bit architecture enables the device to provide a full set of modem controls, with programmable modem control interrupts. It can be used with all types of mainframe, minicomputer, and microcomputer data buses. Unit prices for the 40-pin package begin at $25 in 100 quantities.

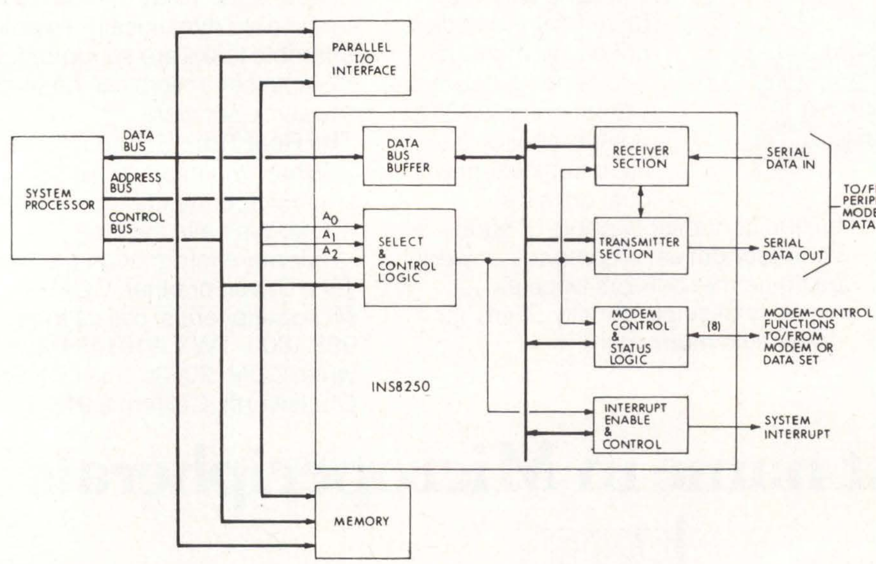
Circle 350 on Inquiry Card

Communications Chip Reduces Overhead in Microprocessor Systems

Many software programmable and hardware control features that reduce system complexity and microprocessor overhead during serial data transfers are implemented on the single chip INS8250 asynchronous communications element (ACE). The device operates as an UART in performing serial-to-parallel and parallel-to-serial conversions, and provides programmable baud rate generation, programmable serial message formatting, status reporting, and complete modem control. It readily interfaces to microprocessors such as the 8-bit SC/MP, 16-bit PACE, 8-bit Z80, and 1-chip 8085. To reduce software overhead during data character transfers, the device prioritizes interrupts from receiver line status, receive data ready, transmitter holding-register empty, and modem status.

The device's functional configuration is programmed by system software via a Tri-State® 8-bit bidirectional data bus. Its CPU can read the complete status of the device at any time during the functional operation. Status information reported includes type and condition of transfer operations being performed, as well as any error conditions (parity, overrun, framing, or break interrupt).

A programmable baud rate generator on the chip accepts any clock input from dc to 3.1 MHz, dividing it to select baud rates from 50 to 56,000. Divisors, loaded during initialization, are stored in two 8-bit latches using a 16-bit binary format. Double buffers on both the transmit and receive sections compensate for any asynchronous anomalies. The timing reference clock input can be divided by 1 to $(2^{16}-1)$, producing a 16X clock for driving the internal



General system configuration for application of INS8250 programmable asynchronous communications element. Produced by National Semiconductor Corp, chip functions as serial data I/O interface in microcomputer systems. Interfacing capability covers wide range of microprocessors

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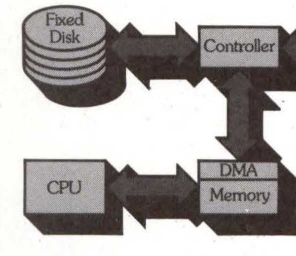

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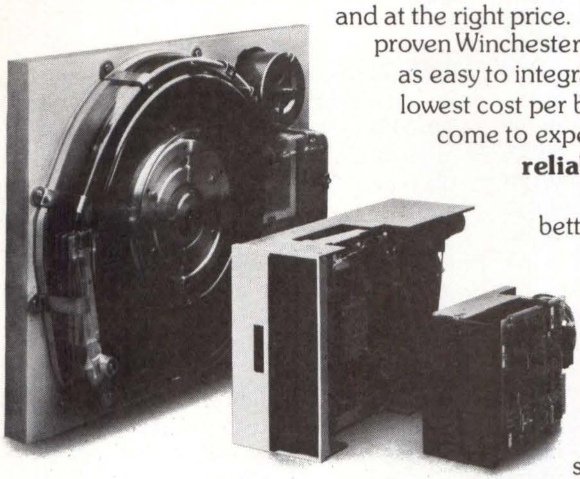

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transmitter logic. Provisions are included to use this clock to drive the receiver logic. Also included are a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

Asynchronous data format characters may have 5, 6, 7, or 8 bits; even, odd, or no parity bits; and 1, 1½, or 2 stop bits. The unit deletes start/stop and parity bits from the serial data stream prior to converting to parallel for the system data bus. It also adds standard asynchronous communication bits to output serial data stream. Contents of the line control register can be retrieved for inspection, eliminating the need for separate storage in system memory.

Status registers inform the CPU of line and modem conditions at any time. Data ready, transmitter register conditions, overrun parity, and framing error are signaled by the line status register. The modem status register indicates various clear, set, ready, and other conventional data signals from the modem.

Other features include a single 5-V power supply, line break generation and detection, false start bit detection, and the capability to add or delete standard asynchronous communication bits (start, stop, parity) to or from a serial data stream. Absolute maximum ratings require temperature under bias to stay between 0 and 70 °C and storage temperature to stay between −65 and 150 °C. All input and output voltages relative to the source supply must be between −0.5 and 7.0 V, and power dissipation is limited to 400 mW. Typical average power supply current is 65 mA with a maximum of 80 mA. Maximum input and clock leakages are ±10 mA. The device, housed in a 40-pin DIP, is produced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051.

High Reliability Hybrid Deglitchers Suppress DAC Transients

Output transients or "glitches" are produced when a digital-to-analog converter changes levels. A hybrid deglitcher is used to suppress these transients.

Transient spikes occur at the output of any DAC whenever its input code is changed. These glitches are caused by switch imperfections such as stored charge or gate-to-drain capacity, causing switches to turn off faster than they turn on, or vice versa. This time skew of analog switches and digital drive signals is most pronounced upon MSB reversals, when all logic inputs are changing.

A deglitching circuit isolates a DAC glitch from the output, but substitutes its own smaller glitch. This glitch comes from charge-dumping on the deglitcher hold capacitor during transitions from sample to hold, and hold to sample. Because it is independent of the DAC, glitch size will not vary with changes in the digital input codes. Therefore the glitch is small and constant.

Two hybrid deglitchers, the 4902 and 4902-83, are produced by Teledyne Philbrick, Allied Dr at Rt 128, Dedham, MA 02026. The -83, when used with the 4058-83 hybrid DAC and 1430-83 op amp, provides a 12-bit DAC system with an update rate of 1.66 MHz, deglitched to a 0.01% level. Sample to hold (and hold to sample) transient for the deglitchers is guaranteed at 12 mV peak to peak. Operation is guaranteed from −55 to 125°C.

All units are constructed, inspected, and processed to MIL-STD-883 including internal visual, stabilization bake, acceleration, and fine and gross leak. In addition, the 4902-83 is burned in at 125 °C for 160 hours and subjected to ten temperature cycles from −55 to 125 °C. Further guaranteed specifications on the 4902-83 include hold jump voltage of ±5 mV, decay rate of 25 μV/μs, and output current of 50 mA.

Circle 351 on Inquiry Card

Low Cost Universal Counter Performs Wide Range of Functions

A single-chip counter containing the functions of a frequency counter, period counter, unit event counter, frequency ratio counter, and time interval counter, the 28-pin ICM7216 is priced as low as $16.65 in 100-up quantities. According to its manufacturer, it will replace discretely implemented universal counters costing from $800 to $1000. It also has the capability of replacing about 100 separate components, including from two to ten SSI or MSI circuits and several driver transistors.

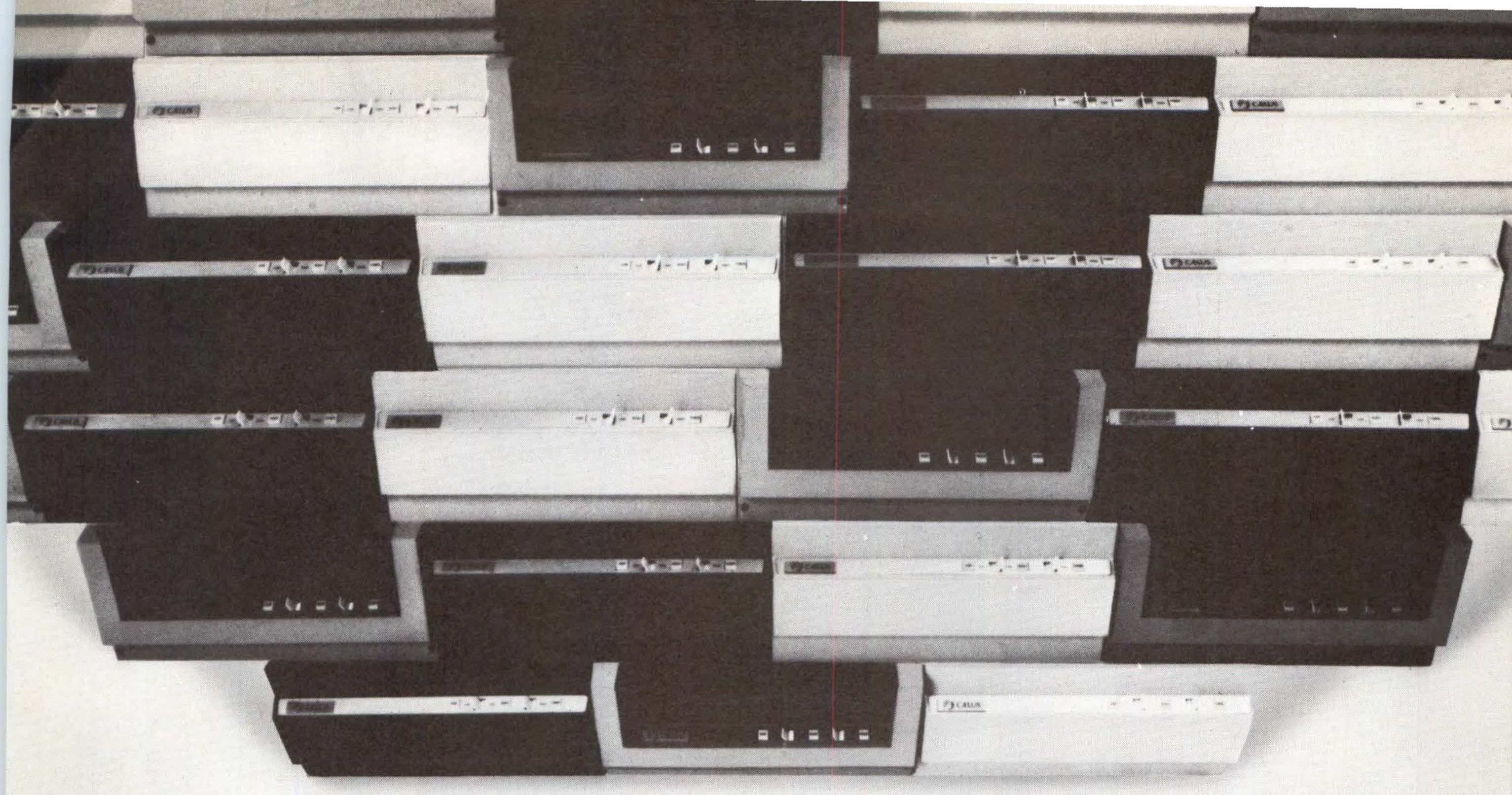
Use of a proprietary process designated as MAXCMOS™ is claimed by Intersil, Inc (1070 N Tantau Ave, Cupertino, CA 95014) to have integrated the equivalent of 3000 to 4000 transistors onto a single 159- by 150-mil chip. The result is a CMOS device capable of both high speed and high current drive operation. Its microprocessor compatibility is seen as a significant feature, initiating the development of "intelligent counter" systems that have mode-switching capabilities.

As a frequency counter, the device offers four internal gate times: 0.01, 0.1, 1, and 10 s. In its period, frequency, ratio, and time interval modes, it operates in 1, 10, 100, or 1000 cycles. It measures frequencies from dc to 10 MHz and time periods from 0.5 μs to 10 s.

Other features include a stable onchip frequency oscillator capable of operating with either a 1- or 10-MHz crystal; internally-generated multiplex timing with interdigit blanking, leading zero blanking, and overflow indication; and selectable controls for decimal point and leading zero blanking, either onchip or external. There is a standby mode that turns off the LED display, putting the chip into a low power (10-mW) status. Hold and reset inputs provide additional flexibility. Furthermore, the counter has a built-in test speed-up function capability.

The device has 8-digit multiplexed LED display outputs, each capable of switching up to 250 mA per digit. The output devices will directly drive both digits and segments of large LED displays. In addition to serving as a single-chip counter solution in many applications below 10 MHz, the device can also operate as part of a minimum chip solution in counter applications in the 100-MHz to 1-GHz range.

There are four versions of the counter, the ICM7216A/B/C/D, with the C and D versions functioning as frequency counters only. All versions incorporate leading zero blanking with frequency displayed in kilohertz. In the A and B versions, time is displayed in microseconds. The display is multiplexed at 500 Hz with a 12.5% duty cycle for each digit. A and C versions are designed



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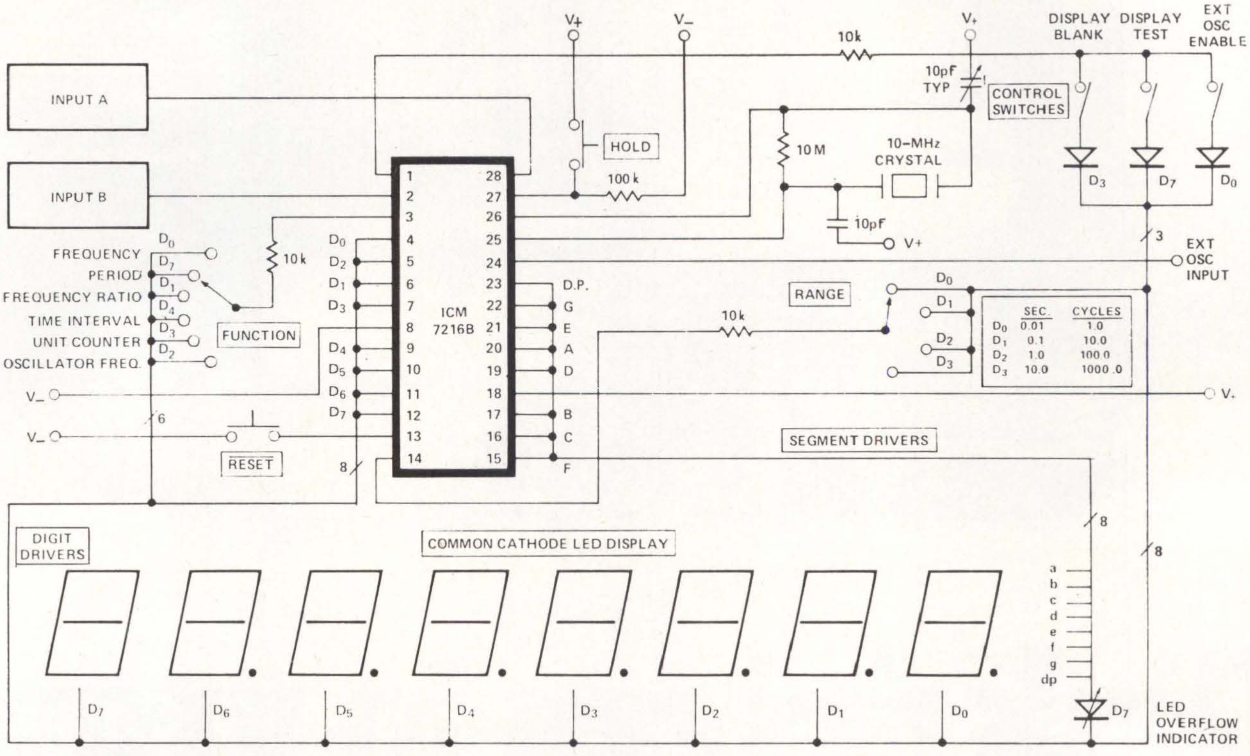

Intersil 10-MHz fully integrated universal counter. Also a LED display driver, the device combines high frequency oscillator, decade timebase counter, 8-decade data counter and latches, 7-segment decoder, digit multiplexers, and 8-segment/8-digit drivers that can directly drive large LED displays

for common anode display with typical peak segment currents of 25 mA; B and D versions are designed for common cathode displays with typical peak segment currents of 12 mA. In display off mode, both digit drivers and segment drivers are turned off, enabling the display to be used for other functions. Operation is off a single 5-V supply.

Absolute maximum ratings include a 6-V maximum supply voltage (V+ to V−), maximum digit output current of 400 mA, maximum segment output current of 60 mA, and voltage on any input or output terminal not to exceed V+ to V− by more than ±0.3 V. Furthermore, maximum power dissipation at 50 °C must not exceed 1.2 W for the 7216A/C and 0.6 W for the 7216B/D. Maximum operating temperature range is −20 to 70 °C for all versions.

Circle 352 on Inquiry Card

Single-Chip Codecs Reduce Digital Communications Cost

Available in two single-chip versions, a monolithic pulse code modulation (PCM) coder/decoder (codec) offers cost and size reductions in all major classes of digital telephone systems. The 2910 is compatible with North American telephone network standards, including Bell System standards; a 2911 version is compatible with European and international standards.

Each of the NMOS LSI devices is produced as a metal-mask option of the same essential chip design. Different interconnection patterns are applied to the chip to provide the two models. The patterns change the companding laws to conform to those preferred in two applications areas (μ Law and A Law).

A codec converts voice signals to digital words for transmission via a PCM link and reconverts the digital words to voice following transmission. The codecs produced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 perform both functions on a single semiconductor device. High density integration allows sample-and-hold circuits, digital-to-analog converter, comparator, and successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link and provide inband signaling.

Properties of these codecs include TTL compatibility for all digital inputs and outputs, precision onchip voltage reference, and the same power supply voltages as microcomputer

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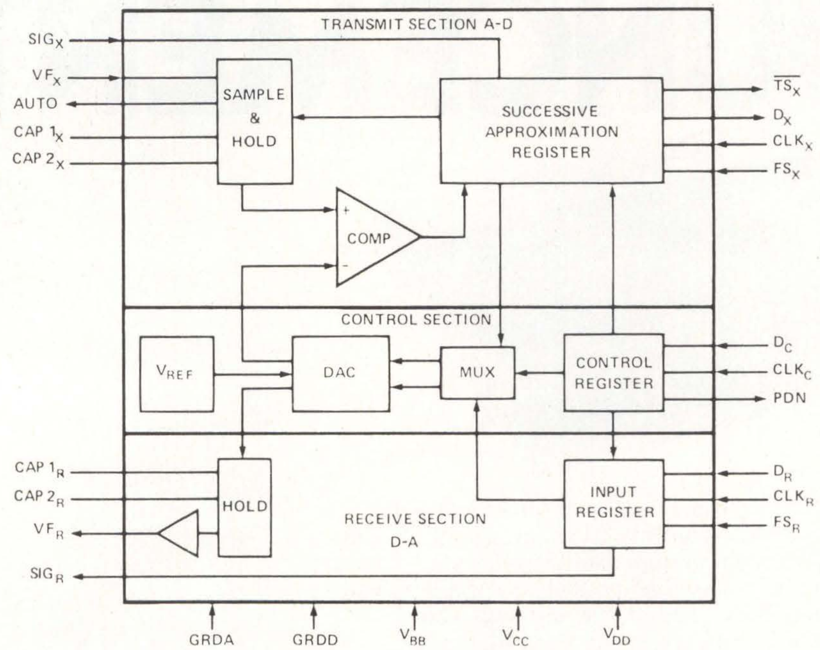


Block diagram of Intel's single-chip 2910 PCM codec for North American use. (2911 version meets European and international standards.) Ability to perform both coding and decoding on same chip is expected to reduce system complexity. Chip interfaces full duplex circuit with pulse code modulation highways of time division multiplex system

and memory components generally used in digital systems (12, 5, and −5 V). Power consumption is typically 230 mW, with typical standby power of 110 mW. The devices have a 78-dB dynamic range, with resolution equivalent to 12-bit linear conversion around zero. Also featured is a microcomputer interface with onchip computation of transmit and receive time slots.

Primary applications are in telephone systems, for transmission (T1 carrier), switching (digital PBXs and central office switching systems), and concentration (subscriber carrier/concentrators). However, the wide dynamic range and minimal conversion time (80 μs minimum) enable their application in data acquisition, telemetry, secure communications systems, and signal processing systems.

The transmit section encodes the incoming analog voice signal at the system frame rate and transmits it at the proper time. On the receive link, the codec fetches an 8-bit PCM word from the receive highway, decodes the analog value, and holds it until the next receive frame.

Transmit and receive frames are independent. They can be synchronous or asynchronous with each other. Common equipment is minimized by the onchip time-slot computation. The feature can be bypassed and discrete time slots sent to each codec in a system. In the power down mode, the codec disables most of its internal circuitry.

Absolute maximum ratings include a temperature under bias of between −10 and 80 °C; storage temperature between −65 and 150 °C; and power dissipation not to exceed 1.35 W. All input or output voltages must stay between −0.3 and 20 V with respect to the base supply voltage.

Both versions of the codec are now in volume production. The 2910 is supplied in a standard 24-pin DIP and the 2911 in a standard 22-pin DIP.

Circle 353 on Inquiry Card

8-Bit Monolithic DAC Includes Input Register

A common requirement for input into a digital-to-analog converter is that data must be stored in a latch before being transferred to the converter. In contrast to this, the DAC-UP8B is a monolithic 8-bit digital-to-analog converter that contains its own level-controlled input storage register. It also contains a stable voltage reference and a high speed output amplifier.

The device was designed by Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 to be used with microprocessor 8-bit data buses. Eight fast current switches operate into a diffused R-2R ladder network. The eight switched currents are summed by the output amplifier, which has a voltage settling time of 2 μs for a full-scale change. Linearity error is ±½ LSB max.

An enable line ($\overline{\text{LOAD}}$) controls the input register (see diagram). When this function is low, the registers are transparent and any change on the digital input pins is reflected on the analog output. A high state level will latch this digital information, and data are retained until this enable line goes low. Data and latch enable input lines have low input load currents.

Output voltage range is 0 to 10 V for unipolar mode and ±5 V for bipolar. Typical settling time is 2 μs for a full scale change. Either the internal reference or an external reference can be used to bias the current switching network. The device can function as a multiplying DAC by varying the reference input

The first Four-Headed Diskette Drive. PerSci stays a generation ahead.

PerSci has done it. Now the industry's only diskette drive with voice coil positioning comes equipped with four heads reading and writing both sides of two eight inch diskettes to provide superior random access capabilities in microcomputer and minicomputer applications. The new PerSci Model 299 dual-head, dual diskette drive offers the highest data capacity, reliability and the fastest access speeds available among small storage peripherals. It is the first drive to advance diskette capability to the level of hard discs.

8 Times More Capacity...

Employing double density encoding on both sides of two diskettes, the PerSci 299 records up to 3.2 Mbytes of unformatted data—eight times the capacity of a standard, single density drive. This unmatched single drive capacity provides the basis for an independent low cost data management system. For maximum media interchangeability with other drives, the 299 will also read and/or write one or two single sided diskettes. Up to eight 299 drives (32 read/write heads) can be daisy chained to achieve a total formatted system capacity as high as 16 Mbytes. Data can be handled in a single density IBM 3740 type format, in IBM 2D compatible double density or in other expanded soft and hard sectored formats.

And Voice Coil Positioning For 6 Times More Speed...

Only PerSci, Inc., has engineered voice coil head positioning for diskette drives. This design innovation gives the PerSci 299 drive the lowest average seek time of any floppy—33 ms including settle. The full 76 track access speed of the Model 299 is under 100 ms.

In A Single Small Size Drive...

While the 299 provides the data capacity and access speed of a hard disc drive, it is the size of a standard floppy—only 4.38" x 8.72" x 15.4." Up to four 299 drives can be mounted vertically or two horizontally in a 19" rack.

With Superior Reliability And Ease Of Operation.

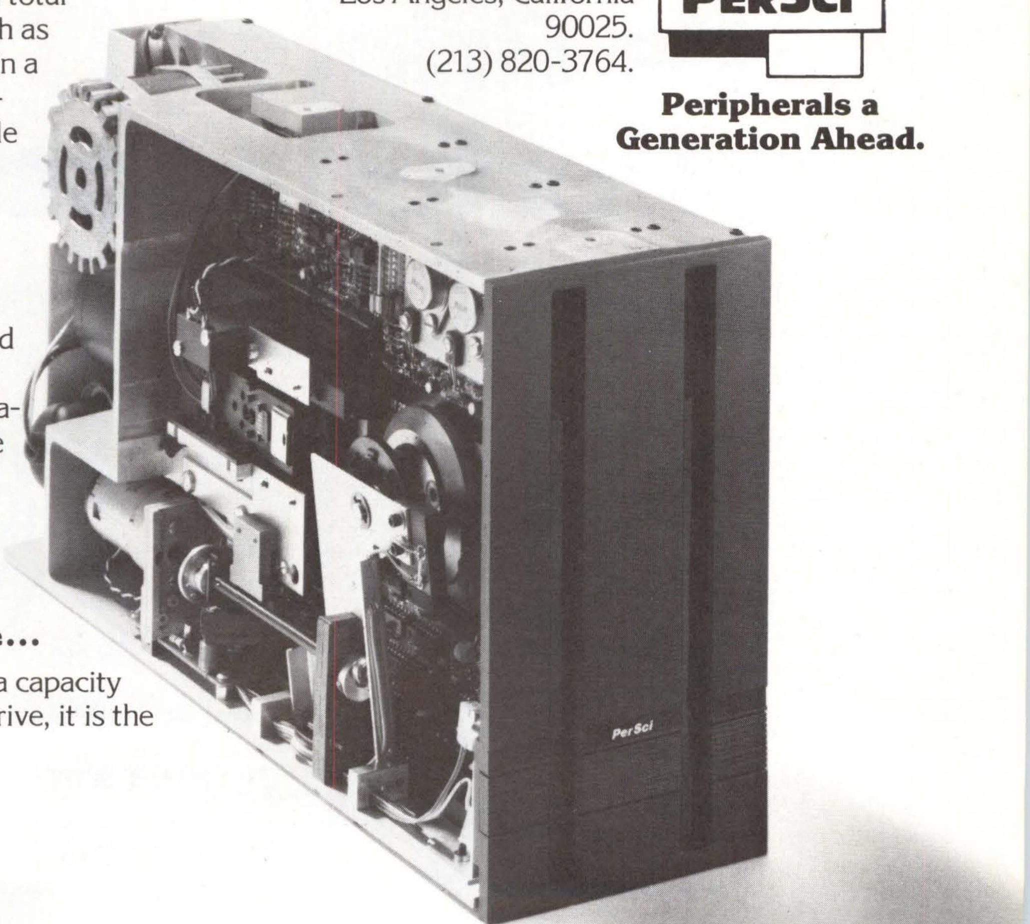
Mechanical and data reliability equal or superior to single headed drives—6000 hour MTBF and a soft error rate of 1 in 10^9—are made possible by PerSci's advanced drive design. A write protect feature guards against operator error, while front panel lights indicate the diskette selected. Electric diskette autoload protects diskettes from damage and allows drive unload by remote control.

Join The Next Generation...Now.

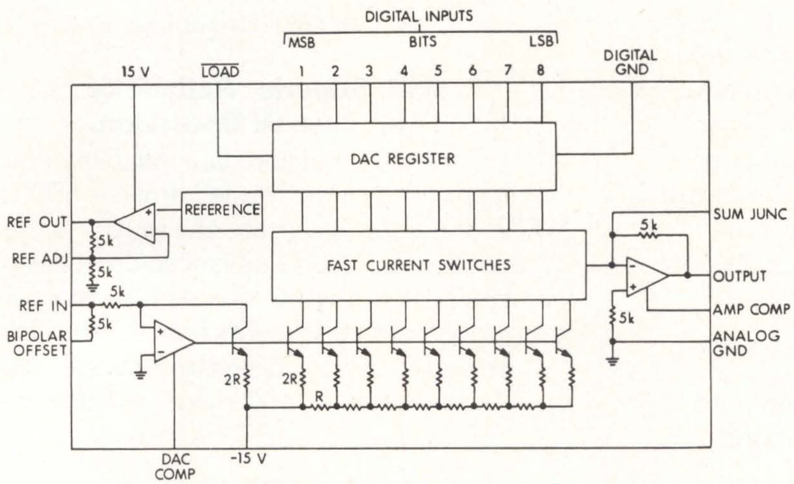
Get PerSci's four-headed diskette drive and get the speed, capacity and reliability of hard disc drives at a fraction of the size...and cost. Call or write for full information from PerSci, Inc., 12210 Nebraska Avenue, West Los Angeles, California 90025. (213) 820-3764.

PERSCI

Peripherals a Generation Ahead.



CIRCLE 77 ON INQUIRY CARD



DAC-UP8BC, 8-bit monolithic digital-to-analog converter from Datel Systems. $\overline{\text{LOAD}}$ latches data in DAC register. When $\overline{\text{LOAD}}$ goes low, register becomes transparent, and input data convert into immediate analog output voltage. Reference and output amplifier are short-circuit protected.

The device is monotonic (no missing codes) over the entire operating temperature range. Power supply requirement is ±15 Vdc over a ±12- to ±18-V range. Absolute maximum ratings include a −18-V negative power supply, 18 V for the positive supply and digital input voltages, and 12 V for reference input and summing junction. Power supply rejection is ±1 mV/V. Quiescent supply currents are 7 and −10 mA.

There are two versions of this 22-pin DIP device: the -UP8BC for operation over 0 to 70 °C, and the -UP8BM for operation over a −55 to 125 °C temperature range. Gain tempco is 20 ppm/°C (not counting the ±60 ppm/°C reference).

Coding is straight binary for unipolar output, offset binary for bipolar. Input logic level is 2 to 5.5 V at 10 μA for a 1 bit, 0 to 0.8 V at −50 μA for a 0. Load pulse width is 200 ns min. Reference input voltage is 5 V ±10%, resistance is 5 kΩ, and slew rate is 25 V/μs.

Output voltage range is 0 to 10 V unipolar, ±5 V bipolar, output current is 5 mA, and output resistance is 5 Ω. Reference output voltage is 5 V ±10%, current is 5 mA.

Circle 354 on Inquiry Card

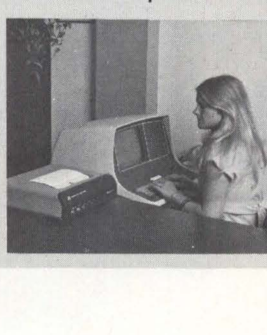
Little Printer, Big Performance.

In your next mini/micro system, you can have the same quiet, compact, reliable printer that has made the CDI Miniterm series a proven winner.

CDI's compact OEM thermal printer is lightweight (Q3 weighs only four pounds) and stepper-motor driven. All solid state circuitry insures maximum performance . . . such as the more than 1,000,000 hours of operation already logged all over the world!

The *new* Q3 is completely microprocessor controlled and is over 70% faster, with printing speeds in excess of 50 characters per second.

Find out more about CDI's quiet, compact thermal printers — available as a mechanism or as a complete terminal package — especially for the OEM. The kind of engineering excellence you expect from CDI, a leader in compact terminal manufacturing.



NOW 70% FASTER!

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- 50 characters per second
- upper/lowercase printing
- Dual fonts (APL available)
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The **Miniterm 1201 RECEIVE/ONLY TERMINAL** . . . Ideal for CRT hardcopy output.

- Compact, super quiet for desk-top use
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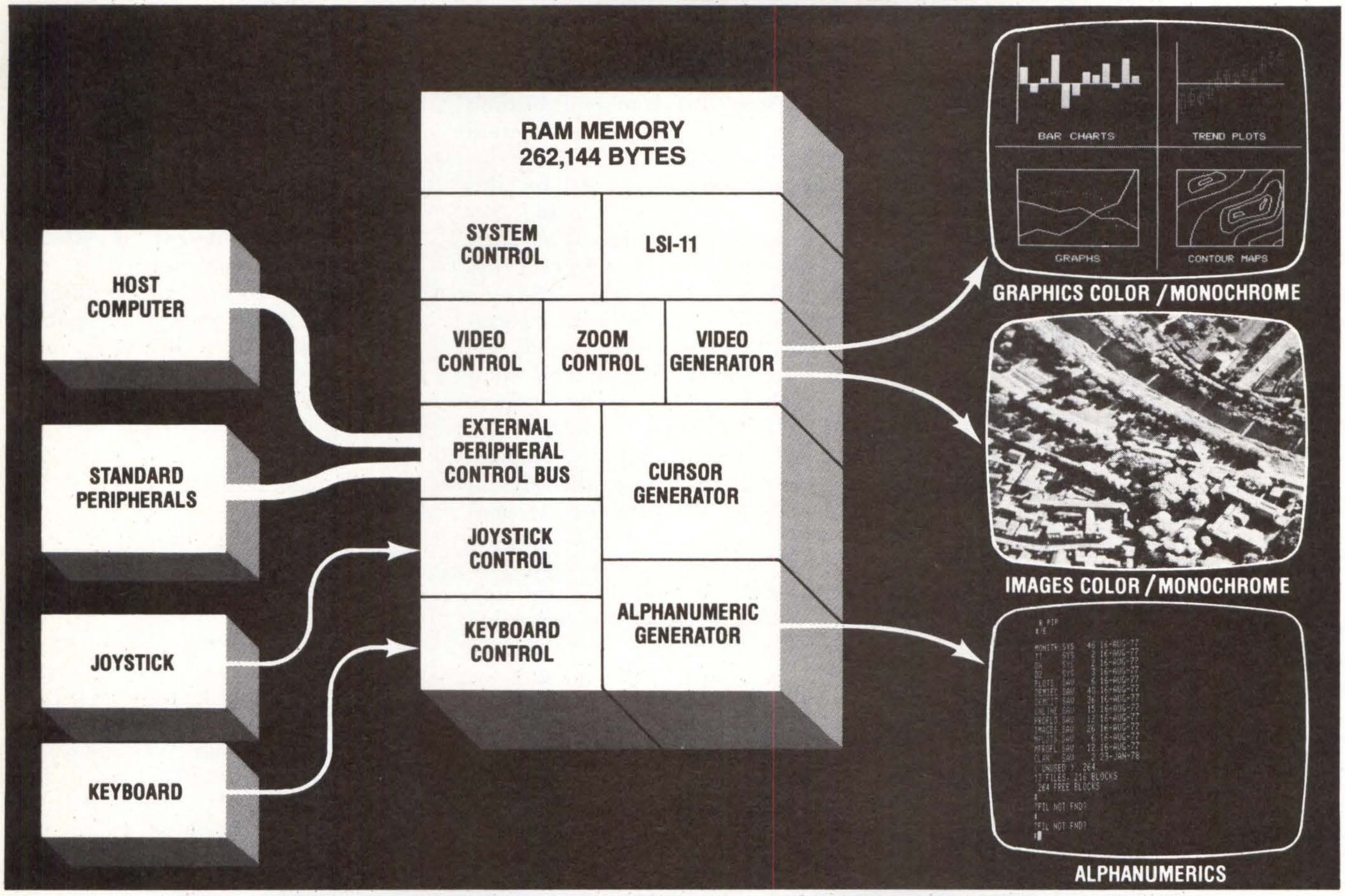

A BETTER IMAGE *Computer*

The VISACOM Visual Image and Computer System is a totally integrated Microcomputer and Display System... another in a series of innovative products from De Anza Systems, designed to enhance your image.

FEATURES

Microcomputer Digital Equipment Corporation LSI-11 microcomputer provides high speed capability and has an instruction set compatible with the PDP-11 series. The system provides a powerful stand-alone computer capability.

System Control Provides the LSI-11 with virtual addressing capability. The entire 256K byte memory can be addressed.

RAM Memory 256 K bytes of RAM memory are organized to provide processing and image refresh. This organization greatly reduces transfer times and increases interaction between the CPU and display image.

Zoom Allows a 64x64x16, 128x128x16 or 256x256x16 bit portion of the memory to fill the entire image window under hardware control.

Video Generator Provides four or eight bit digital to analog conversion and intensity transformation tables.

Dual Cursor Provides two individual cursors controlled by an external Joystick with multifunctions.

Alphanumeric Generator Provides up to four separate 80 character by 25 line overlays.

Software An operating system is provided to handle memory management, and also provides facilities to interface I/O and user subroutines. Subroutines for high speed generation of vectors, conics and rectangles are also available.

De Anza Systems Incorporated

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Santa Clara, CA 95050 (408) 988-2656

CIRCLE 79 ON INQUIRY CARD

Fast Processor Performs Full Range Of Math Functions

Contained on a single chip, a high speed processor that enhances the arithmetic capability of processor-oriented systems performs fixed-point single- and double-precision (16/32-bit) and 32-bit floating-point operation in a binary format. Available functions include basic arithmetic, trigonometric, exponential, and logarithmic operations. This device provides capabilities previously requiring hundreds of individual TTL packages.

The Am9511 arithmetic processing unit is produced by Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. It contains a general-purpose 8-bit bidirectional data bus and interface control and was designed to be compatible with any generally used 8-bit processor.

Circuit speed approaches that of minicomputer floating-point processors. With a clock rate of 2 MHz, this circuit can perform a single-precision add in 16 μs. Operating at a clock frequency of 4 MHz, it reduces the add operation to 4 μs.

Transfers taking place over the 8-bit bus include operand, result, status, and command information. Operands are pushed into an internal stack and a command is issued to perform operations on data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Power supplies are 12 V (V_{DD}) and 5 V (V_{CC}). Absolute maximum ratings include storage temperature from −65 to 150 °C and power dissipation of 2 W. The device is available in a 24-pin hermetic DIP.

Circle 355 on Inquiry Card

Computer Programs Govern Automated Design of Hybrids

Programs have been developed that specify preliminary placement of chips on hybrids as well as complete routing of interconnections. This process, developed by Automated Systems, Inc, 888 N Sepulveda Blvd, El Segundo, CA 90245, also provides precision art, a variety of diagnostic logic checks, and front-end loading analysis, all computer-generated from a common data base.

Programs were developed for this technology to accommodate the special design requirements associated with placement and routing of hybrids. These requirements include such factors as the need to avoid congruent vias through all layers and the need to determine the optimal rotation of chips as well as their placement on the substrate.

Enabling the computer to evaluate and select from among the myriad interconnection possibilities created by the chip placements is said to result in substantial time and cost savings over manual or computer-aided design in laying out dense hybrids. The process is offered on a service bureau basis throughout the U.S. and Canada. Customer input is comparable to that required for design automation of printed circuits: logic diagram or coded wire list, board geometry requirements, and special ground rules.

Circle 356 on Inquiry Card

Op Amp Offers Ultra-Low Bias Current

High input impedance (10^{13} to 10^{15} Ω) and a maximum input bias current of 75 fA characterize the 3528 FET operational amplifier family. The devices also provide offset voltages in the 250- to 500-μV range, and typical maximum offset voltage drifts of 5 μV/°C. Laser trimmed offset voltage virtually eliminates external nulling. Unity gain bandwidth is 0.7 MHz and slew rate is 0.3 V/μs.

These op amps are designed for use in various situations requiring ultra-low input bias current. Specific applications include photodiode amplifiers, photomultiplier tube amplifiers, low drift integrators, or current-to-voltage converters.

Performance characteristics are guaranteed over a −25 to 85 °C temperature range after warm up and without a heat sink. The specification of bias current under these conditions is significant in ultra-low applications because normal self-heating during warm up can change the bias current of conventional devices by factors as large as four.

Output is protected from damage due to short circuits to ground or to either supply. The manufacturer (Burr-Brown, International Airport Industrial Pk, Tucson, AZ 85734) states absolute maximum ratings that include a ±20-Vdc power supply, 500-mW internal power dissipation, and a ±40-Vdc differential input voltage. Storage temperature range is from −65 to 150 °C.

Circle 357 on Inquiry Card

DESC Issues Approval For 2k Bipolar P/ROMs

The Defense Electronics Supply Center (DESC), Dayton, Ohio, has provided QPL-II (Qualified Products List) approval to Monolithic Memories, Inc (1165 E Arques Ave, Sunnyvale, CA 94086) for its 2048-bit Schottky bipolar P/ROM. Two versions of the device are qualified to APL-II: the /20401 (open collector) and the /20402 (3-state). The new military "slash number" for the 512 x 4 device is MIL-M-38510/204 (USAF).

Both P/ROMS are available in military flatpack or DIP. For those ordering the circuits, the company's Federal Supply Code (FSC) number is 50364, and its manufacturer's designated symbol is "CECD." Standard part numbers for the devices are 5305-1 (open collector) and 5306-1 (3-state). The Air Force will use the P/ROMS in the new standard avionics computer (ANAYK-14) installed in the F-16 and F-18 aircraft.

Circle 358 on Inquiry Card

Low Cost Op Amp Claims Lowest Offset Voltage and Drift

Offset voltages of less than 25 μV and drifts of less than 0.5 μV/°C unnulled are characteristic of the AD517 monolithic operational amplifier. The device is laser trimmed at the wafer level to meet these levels of precision. Superbeta input transistors provide offset currents as low as 0.25 nA max and input bias currents as low as 1 nA max.

The manufacturer (Analog Devices, Route 1 Industrial Park, PO Box 280, Norwood, MA 02062) claims that the offset voltage is the lowest offered in the industry without external nulling pots. Input bias current is also claimed to be the lowest for any precision bipolar op amp. This current shows the characteristic drop with increasing temperature to less than 0.5 nA at temperatures above 70 °C.

The input stage is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short circuit protected and is capable of driving a load capacitance of up to 1000 pF.

Device layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances. Common mode rejection is 110 dB min; input bias current drift is ±4 pA/°C, T_{min} to T_{max}, input offset current is as low as 250 pA, and output current is 10 mA min.

The devices are available in three performance versions for operation over the 0 to 70 °C temperature range (AD517J, K, and L) plus one version for the −55 to 125 °C range (AD517S). The AD517S is also available fully processed and screened to MIL-STD-883A, Level B. Devices are priced as low as $3.50 in 1000 quantities.

Circle 359 on Inquiry Card

IC Provides Protection From Overvoltages

A sensing circuit that protects sensitive electronic circuitry from voltage transients and loss of regulation has been announced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 as a second source for the Motorola Semiconductor MC3423. It triggers a protective external crowbar SCR when it senses an overvoltage condition or if a TTL high level is applied to a remote active terminal. Separate outputs are available to trigger the crowbar circuit and to provide a logic pulse to indicator or power supply control circuitry.

The device features a current source that can be connected to an external time-delay capacitor to prevent false triggering caused by noise. Other characteristics include a 2.6-V internal voltage reference, with tempco typically 0.08%/°C, and operation specified over a 0 to 70 °C range. A more durable version, the MC3523, is characterized for operation over the full −55 to 150 °C military temperature range. Both versions are available in 8-pin DIPs.

Circle 360 on Inquiry Card

Custom LSI Process Utilizes Cell Library

Programmable logic arrays and full custom design represent two alternatives in the development and production of custom LSI chips. The former of these provides a very rapid turnaround, but does not optimize use of chip area, in terms of the user's specific requirements. On the other hand, the latter approach does provide optimization for the user, but involves a very long turnaround.

Holt Inc (3303 Harbor Blvd, Costa Mesa, CA 92626) provides a compromise approach to custom design, called custom celled CMOS. This compromise is based on the maintenance of a "cell library" consisting of logic elements stored on tape. These cells are drawn from the library to implement a custom arrangement of logic elements on a chip—in much the way that metal connections are employed in programmable logic arrays. The rapid turnaround characteristic of those arrays is maintained, but chip optimization is also possible in this technology, since the custom design relates to logic element placement, not just interconnection.

Circle 361 on Inquiry Card

MNOS Transistors Allow Quad Latch to Retain Data on Inputs

Use of MNOS transistors as memory elements enables a quad latch to retain data on its inputs when power is terminated. With the return of power, the stored data are automatically restored to the outputs. A 1-year data retention time over a 0 to 70 °C temperature range and a minimum of 1M write cycles are guaranteed.

The manufacturer, Plessey Semiconductor, 1641 Kaiser Ave, Irvine, CA 92714, states that the 4-bit data latch differs from other currently available MNOS products in being TTL MOS compatible, requiring only standard operating voltages of 5 and −12 V. An internal circuit generates all other required voltages.

These devices are intended for use in systems with small but critical memory requirements. They can be used, for example, as latching relay replacements, nonvolatile add-ons to counters, or storage elements for security codes. The MN9102, the first in a forthcoming family of nonvolatile MNOS products by this manufacturer, is available in a 14-lead ceramic DIL package.

Circle 362 on Inquiry Card

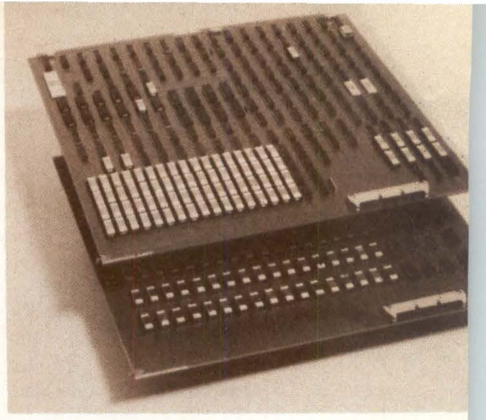
High Performance Operational Amplifier Is Housed In Mini-DIP

An op amp that is pin-for-pin compatible with the 741 series has been provided in a different model. The OP-02, produced by Precision Monolithics, Inc, 1500 Space Park Dr, Santa Clara, CA 95050, is now mounted in a mini-DIP and is designated as the OP-02CP.

This epoxy-B packaged device features an untrimmed input offset voltage at 3 mV maximum over a 0 to 70 °C ambient temperature and an input offset current of 10 nA maximum. Input voltage drift is 10 μV/°C maximum over the ambient range, and noise is typically 0.65 μV, peak to peak. The manufacturer claims that the device delivers better performance than both industry standard and premium type 741s. □

Circle 363 on Inquiry Card

PRODUCT FEATURE



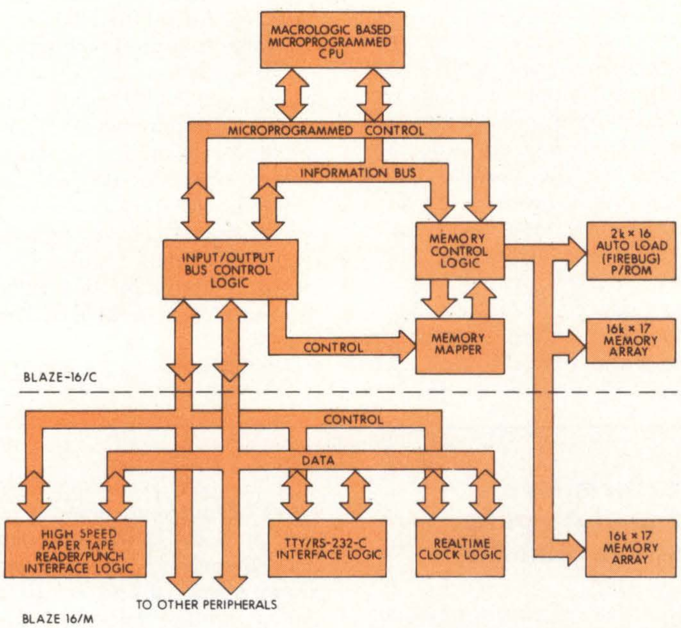
2-Board, All-LSI Minicomputer Features I^3L Technology and Bit-Slice CPU

Low power consumption and high speed are attained on the Blaze-16™ minicomputer through use of isoplanar integrated injection logic (I^3L®) technology and a Macrologic bit-slice microprocessor set. Introduced by Fairchild Camera and Instrument Corp, the 16-bit microprogrammed minicomputer is compatible with and executes the same instruction set as the company's Microflame™ microprocessor. It is compatible also with the Data General Nova 3™ minicomputer although it requires only two slots in a chassis while the latter requires five or six.

By using all LSI devices, rather than some MSI and some LSI, system reliability has been increased while system size, power consumption, and cost have been reduced. I^3L, employed in the design of the microprogram sequencer and main memory, also achieves high packing density.

Design Features

The Blaze-16 minicomputer is fabricated on two 15 x 15" (38 x 38-cm) printed circuit boards. One board—the -16/C (see diagram)—contains Macrologic microprogrammed CPU, memory control logic, 16k-word memory array, memory parity logic, memory mapping logic, autoload logic and P/ROMs, and input/output bus converter. Provisions are included for quadrupling the memory array size by plugging pin compatible 16k x 1 RAMs in place of standard 4k x 1 devices. Memory mapping logic can address up to 256k words.



Block diagram of Blaze-16 minicomputer. Memory array capacity can be quadrupled by replacing 4k x 1 RAMs with 16k x 1 devices having identical pinouts. Components are separated on two PC boards, designated as -16/C and -16/M

The second board—designated as the -16/M—contains a 16k-word memory array, TTY/RS-232-C interface logic, high speed paper tape reader/punch interface logic, and realtime clock. Memory on this card also consists of 4k x 1 RAMs.

There are essentially two major parts to the CPU: a 16-bit wide data path and a microprogram control. The data path consists of four arithmetic logic register stacks, each with eight registers/accumulators, and four data path switches. An I^3L microprogram sequencer controls the 1k-word by 48-bit microprogram, which resides in twelve 1k x 4 ROMs.

In addition to a basic FIRE instruction set, the microprogram handles multiply and divide instructions and stack handling operations. It includes a self-test routine and 15 operator-console routines. About 70% of the microprogram memory is free for user microprogramming and future instruction set expansion.

The minicomputer operates in a pipeline mode with a 200-ns microcycle. A 16-bit wide bidirectional bus, common to all peripheral devices, transfers both addresses and data between the CPU and main memory.

Typical memory array access time is 100 ns, and active power dissipation is 400 mW with 70-mW standby power. Other features include 240-ns cycle time, two chip selects, controllable data latching, and 65-ns access and cycle times when using the paging mode. Memory inputs have standard TTL threshold and temperature properties and the output is a 3-state totem pole with a conventional unit load of 10.

Instruction mapping P/ROMs provide up to 256 starting locations in the microprogram memory for macroinstruction execution (many instructions will share a common starting location). They continuously monitor the eight most significant bits of the bus to eliminate the delay required to load the instruction register. Instruction execution can be started merely by doing a memory read at the address in the incremented program counter and issuing an instruction to the microprogram sequencer. The instruction register is then used for the dedicated hardware portion of the control logic.

The microprogram sequencer contains a 10-bit microprogram-address register. Of seven test inputs, four participate in conditional branches and three in multiway branches. Conditional test lines are flip-flop buffered and these flip-flops can be tested individually by appropriate branch instructions. Three test inputs are used to form the least significant three bits of the branch address for an 8-way branch, depending on the bit pattern present on these three inputs.

With this sequencer the user can select pipeline or non-pipeline mode of operation. A pair of outputs allow the sequencer to control an external multiplexer when choosing the source of a branch address. An inhibit output facilitates sharing the microprocessor control fields with the next address field, thereby reducing the width of the associated control store.

Price and Delivery

Deliveries of the Blaze-16 minicomputer will begin in the fourth quarter of this year. Single unit price will be $4000, including FIRE 1 software package. Volume discounts will be available. Fairchild Camera and Instrument Corp, 464 Ellis St, Mountain View, CA 94042. Tel: 415/962-5011.

For additional information circle 199 on inquiry card.

BARRIER BLOCKS À LA CARTE

The "menu" of BUCHANAN® Single-Screw Barrier Blocks offers a recipe for every taste. In automated or manual installation, mounted on PC board, panel, or chassis, BUCHANAN SSB's are the most cost-efficient blocks on the market. And you can order them cooked up in almost every style and combination. Here are a few choice selections . . .

SSB's come *without* bottom terminals (A), for surface-mounting anywhere . . . *with* terminal pins for PC Board soldering: straight (B), or bent for perpendicular mounting (C) . . . with wire-wrap pins, for use with automated or manual wire-wrapping tools (D); also compatible with AMP® Crimp-Clip Termi-Point connectors (E) . . . with standard quick-connect terminals (F), excellent for interfacing machine wiring harnesses with field-installed wiring . . . and with solder-tail terminals (G), too.

THEN . . . SSB's also come with turret bases (H) for bottom-side circuit isolation, with *all* of the above terminals.

NOW WE COME TO TOP HARDWARE: SSB's come with binding-head screws , screws with captive clamp, phillips-head screws, or with a choice of 7 different quick-connects, or two styles of solder tabs.

WAIT . . . THERE'S MORE: You can select either 3/8" or 7/16" contact spacings . . . 1 to 32 terminals per block . . . choose from five different colors . . . six variations of hot-stamped circuit identification numbers . . . AND, you can get the exact combination you need — standard or special — at any Authorized BUCHANAN Distributor with a PDQ (Precise Designs Quickly) Center.

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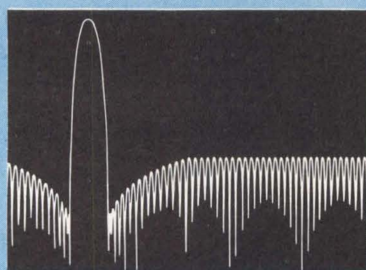
ADVANCED TECHNICAL

Course 412 — Four days

Digital Signal Processing



SAN DIEGO
Sept. 26-29

WASHINGTON D.C.
Oct. 10-13

PHILADELPHIA
Oct. 31-Nov. 3

BOSTON
Dec. 5-8

LOS ANGELES
Dec. 12-15

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensible manner, to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

- **An Overview of Applications**
- **Digital vs. Analog Signals**
- **Operations on Digital Signals**
- **Recursive Filters**
- **Nonrecursive Filters**
- **Design Techniques**
- **Computer Aided Design**
- **Statistical Approaches**
- **Spectral Estimation**
- **Application Case Study**

Course 350 — Four days

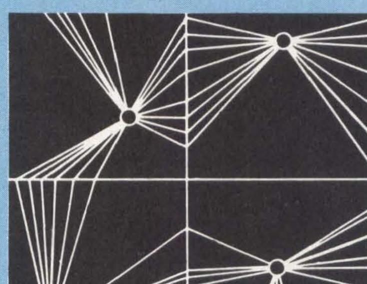
Distributed Processing and Computer Networks

WASHINGTON D.C.
Sept. 26-29

SAN DIEGO
Oct. 17-20

PHILADELPHIA
Nov. 7-10

BOSTON
Dec. 5-8



This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of the concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

- **What is to be Distributed?**
- **Data Communication Concepts**
- **The Computation Continuum**
- **Computer Networks**
- **Network Protocols**
- **Database Structures**
- **Database Requirements**
- **Security Considerations**
- **Evaluation and Selection**
- **Management and Control**

MICROPROCESSORS & MICROCOMPUTERS
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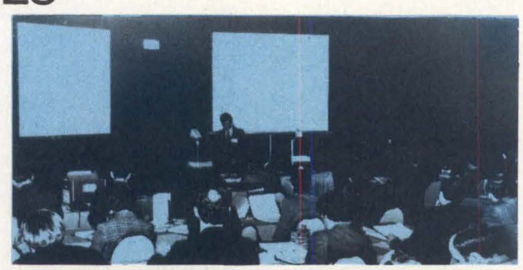


LOS ANGELES
Sept. 18-22

NEW YORK
Sept. 25-29

SAN DIEGO
Oct. 30-Nov. 3

CHICAGO
Nov. 6-10

WASHINGTON D.C.
Dec. 4-8

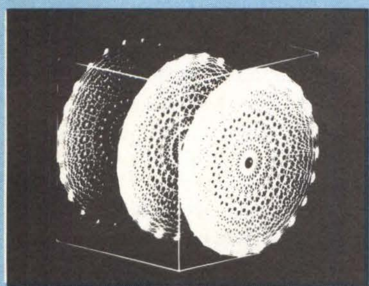
EDUCATION

INTEGRATED COMPUTER SYSTEMS, INC.

Course 365 — Four days

Computer Graphics

State of the Art Techniques and Applications



HOUSTON
Sept. 12-15

WASHINGTON D.C.
Oct. 10-13

LOS ANGELES
Oct. 17-20

CHICAGO
Nov. 7-10

BOSTON
Dec. 12-15

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

- **Display Hardware**
- **Color Display Techniques**
- **Two Dimensional Graphics**
- **Three Dimensional Graphics**
- **Transformations**
- **Software Structures**
- **The Hidden Line Problem**
- **The Hidden Surface Problem**
- **Software 'Build or Buy'**
- **Selection Methodology**

Course 440 — Four days

Fiber Optic Communication Systems

HOUSTON
Sept. 19-22

SAN DIEGO
Oct. 3-6

This course is designed for engineers, scientists and managers involved in the planning, design and implementation of all types of communication systems. The course covers the fundamental principles of fiber optic based systems, and the state of the art in system components including light sources, optical fibers, single and multifiber cabling, fiber coupling, photodetectors, receiver and repeater technology, and fiber optic networks. Commercially available components will be surveyed to illustrate design techniques for the cost effective, practical application of this important new technology.

- **Advantages of Fiber Optics**
- **Optical Fiber Transmission**
- **Cabling Technology**
- **Light Sources**
- **Detection Technology**
- **Receiver/Transmitter Technology**
- **Modulation Techniques**
- **Digital Communications**
- **Data Bus Design**
- **System Design and Analysis**

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- ☐ FIBER OPTIC COMMUNICATION SYSTEMS
- ☐ MICROPROCESSORS & MICROCOMPUTERS

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MAIL TO: **Course Manager**
INTEGRATED COMPUTER SYSTEMS, INC.
3304 Pico Blvd., P.O. Box 5339
Santa Monica, CA 90405

OR CALL: (213) 450-2060

Name__________ Job Title__________

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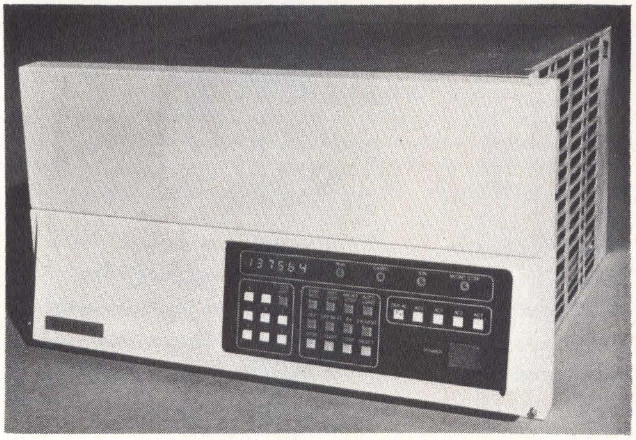
PRODUCTS

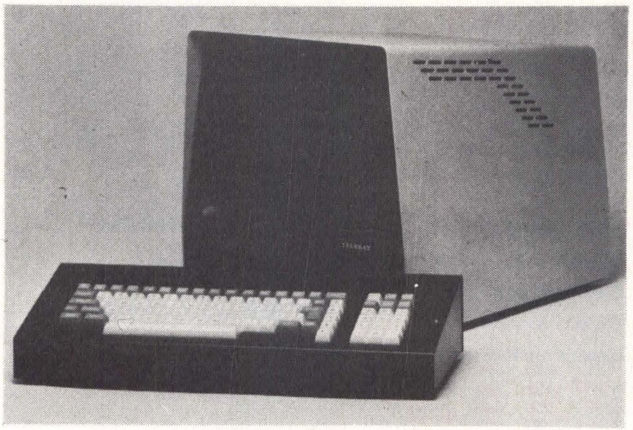
Nova Compatible Minicomputers Offer Direct Addressing of 64k Words



Single-board CPUs which operate with up to 64k words of directly addressable MOS or core memory, models 8 and 12 have operating speeds of 800 and 1200 ns, respectively. Basic versions accommodate 64k of core or MOS memory on separate boards; a special MS version has up to 64k of MOS on the CPU board. Compatibility with Nova computers is provided by four 16-bit accumulators, instruction set, program interrupt, and pin compatibility with peripheral controllers. Three chassis configurations have 5-, 12-, or 21-slot capacities. The 21-slot version accepts 17 boards plus 2M bytes of Megastore memory. 5-slot versions have four slots available for core (C) or MOS (M) memory in a 5.25" (13.34-cm) chassis, and 13-slot models make 12 slots available in a 10.5" (26.7-cm) chassis. All models provide complete front access to all boards, modules, components, and power supplies via the hinged front panel. Programmer console in the front panel allows entry of words and addresses. Pushbuttons allow control of the program and an octal pad indicator displays word or address entered or contents of a location. LED indicators display internal conditions for program debugging. **Ampex Corp,** 200 N Nash St, El Segundo, CA 90245.

Circle 200 on Inquiry Card

Modular CRT Display Terminal Provides Chip-Level Serviceability

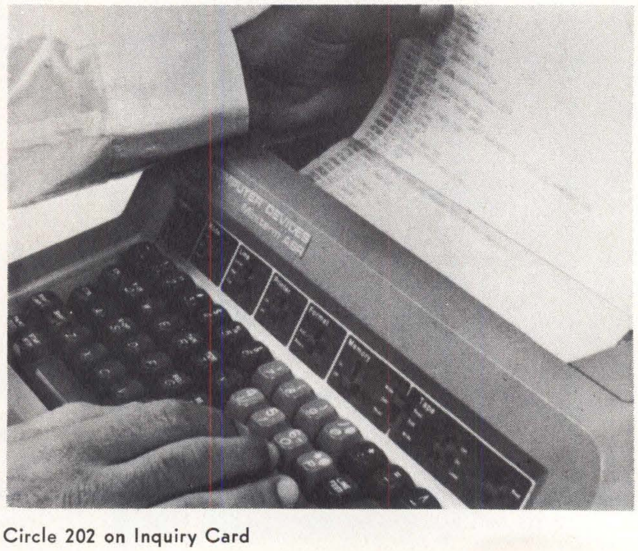


Completely serviceable without hand tools, the series 10 model 1061 is built of plug-in modules; no screws or tools are needed for replacement. Plug-in ICs provide chip-level serviceability. The microprocessor controlled CRT terminal has programmable I/O speeds from 50 to 9600 baud, also programmable are peripheral speeds and enable and disable. The 12" (30.48-cm) diagonal screen displays the 128-char ASCII set on 24 lines x 80 char (or 24 x 40 char changeable with ESC sequence). The typewriter styled keyboard has cursor pad, numeric pad, and 24 special keys for programming, editing, discrete functions, and mode selection. Text handling features include insert and delete line and character; transmit line, message, and page; highlight in dim, blink, reverse video, and underline in any combination; and a transparent mode for display of control codes. Communications are RS-232-C serial asynchronous in block or character mode, half or full duplex. **Teleray, Div of Research Inc,** Box 24064, Minneapolis, MN 55424.

Circle 201 on Inquiry Card

Portable Microprocessor-Controlled Computer/ Terminal Includes Hardcopy Printer

The compact 17-lb (7.65-kg) Miniterm PRO (programmable remote operation) model 1206 is a microprocessor-controlled terminal that features 32k main memory and integral magnetic tape cassette drive. An integral BASIC interpreter coupled with 32k RAM editor utility allows users to program applications software to requirements. Users can create local program library of minicassettes, load programs directly into terminal, and compute and print out required solutions and report formats. Unit includes ability to program, load, and store in Motorola 6800^{R} assembly language. In addition to being a programmable portable computer, the device can be operated as an ASR offline terminal. The user-oriented, full alphanumeric keyboard is switch selectable to standard typewriter, alternate (TTY), or numeric cluster operation. Std features include 50-char/s printing speed, 1k-char line buffer, 1200-bit/s transmission rates, and EIA std RS-232 interface. **Computer Devices Inc,** 25 North Ave, Burlington, MA 01803.



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SEMICONDUCTOR OR CORE. EMM is the only memory company that can assess your needs impartially and recommend the solution best for your application. Either technology - semiconductor or core - is available in our industry standard MICROMEMORY 3000 family or in a custom design. **JUST THE RIGHT SIZE.** Proven EMM memories are available in capacities from 8K bytes to 128K x 22 bits on a single board. Or we can package them in a chassis with self-contained power supply. **ANY SPEED YOU NEED.** Why pay for speed you can't use? Or settle for less than you need? With our wide range of systems and choice of technologies, we can give you just what you should have.

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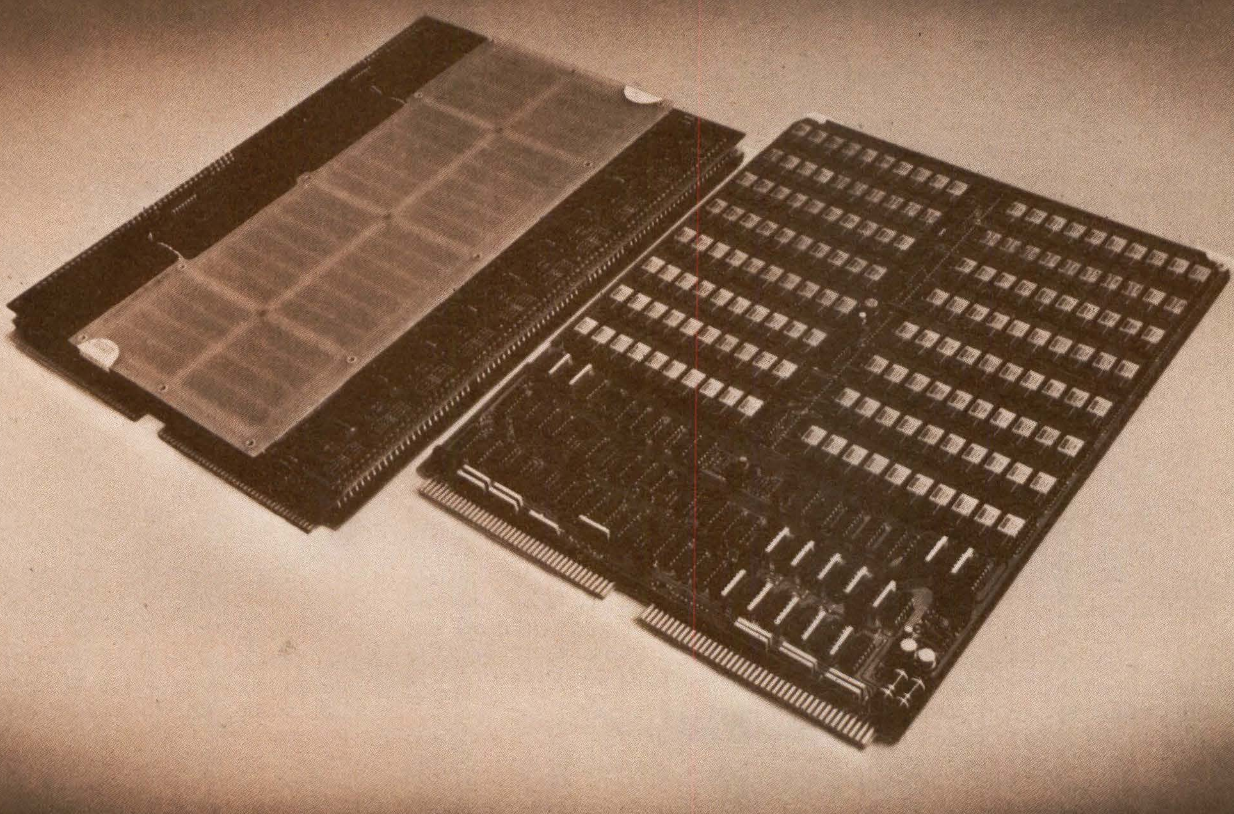
Just the right size

Any speed you need



Commercial Memory Products, a Division of Electronic Memories & Magnetics Corporation
12621 Chadron Avenue • Hawthorne, California 90250 • Phone (213) 644-9881

PRODUCTS

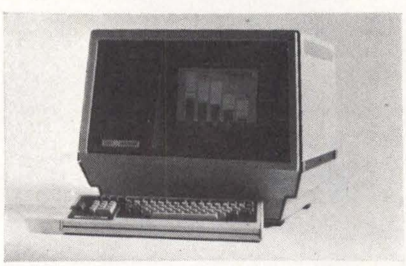
VOICE SYNTHESIS SYSTEM

VS-6.4, an improved model of the VS-6, produces electronically synthesized human speech from digital output. Digital information is converted to speech through a patented electronic design. 2 circuit boards of the VS-6 were changed to obtain improved voice quality. Converting existing VS-6 equipment is possible with the company's retrofit boards; software is unaffected by the change. **Votrax, a div of Federal Screw Works,** 500 Stephenson Hwy, Troy, MI 48084.
Circle 203 on Inquiry Card

OPTICAL ISOLATOR SYSTEM

TTL compatible system utilizes LED transmitters and PIN photodiode receivers coupled by a miniature optical fiber transmission line, operating on a 5-V power supply. Immunity from static and radiated fields, security of transferred data from external sensing, and high speed data transfer are offered. I/O operates at TTL level with repetition rates to 20 MHz and pulse widths as narrow as 15 ns. **Olektron Corp,** 6 Chase Ave, Dudley, MA 01570.
Circle 204 on Inquiry Card

COLOR GRAPHICS TERMINAL

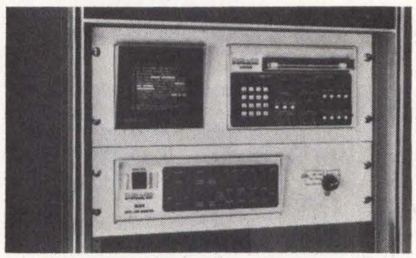


Capabilities of scrolling graphics and alphanumerics, and multipaged graphing with the added feature of color are incorporated in the 4027 computer terminal with raster scan display. Colors can be selected from a 64-color palette with up to 8 colors simultaneously on the screen. Plot 10 Easy Graphing host software and an Interactive Graphics Library are offered. Std video signal outputs are included. Interface options are available. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.
Circle 205 on Inquiry Card

COMPUTER ACCESS BADGE READER

Standalone, microprocessor controlled BD-1 reader can be configured to read type-5 punched or mag strip plastic badges to provide the host computer with operator identity. Communication is by std 110- to 9600-baud asynchronous RS-232 protocol in series with an installed CRT terminal or on a separate dedicated communications line. Automatic clamping upon badge insertion, remote or pushbutton badge ejection, and error signaling are incorporated. **General Digital Corp,** 700 Burnside Ave, East Hartford, CT 06108.
Circle 206 on Inquiry Card

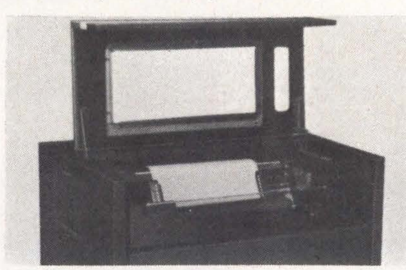
CONTROL CENTER DATA MONITOR



Rackmounted version of DLM II/Tapetrap data line monitor makes special code and hex switch accessible from front panel for easy code selection and hex display. Unit fits a std 19" (48.3 cm) equipment rack. A 1M-byte storage companion to DLM II, Tapetrap provides programmable, unattended monitoring techniques for fast fault isolation. Monitor is operator settable to record 1 track (250k char) and stop, record whole tape (1M char) and stop, or record continuously in an endless loop format. **Digi-Log Systems, Inc,** Babylon Rd, Horsham, PA 19044.
Circle 207 on Inquiry Card

900-LINE/MIN PRINTER

Model 1290, added to the ChainTrain[R] line printer series, has an 8080A microprocessor controller and single line memory data buffer. There are 132 print positions at 10/in (4/cm), with 6 lines/in (2.4/cm). Single line advance is 20 ms, and paper slew rate is 20/s. The printer automatically single or double line spaces, skipping over perforations. Line feed is 0 to 63 lines. Vacuum cleaner and paper puller systems are optional. **Data Printer Corp,** 99 Middlesex St, Malden, MA 02148.



Circle 208 on Inquiry Card

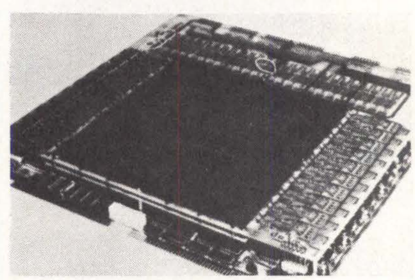
LARGE MEMORY LOGIC ANALYZER

Containing 3 separate memories, each capable of handling data as 16 channels of 1024 bits or as 16,384 bits in serial, microprocessor controlled logic analyzer can trigger on 16 parallel bits or on 16 bits embedded in a serial data stream. Memory depth and 20-MHz max clock rate allow diagnosis of propagation delay problems, such as those found in RAM. Built-in CRT and keyboard allow data to be entered, edited, and displayed in hex, octal, or binary, or as a parallel or serial timing diagram. **Moxon, Inc,** 2222 Michelson Dr, Irvine, CA 92715.
Circle 209 on Inquiry Card

MICROPROCESSOR BASED SYNCHRONOUS MODEM

Design of the standalone or rackmount 208B/A extends the modem's capability to a high level of performance at 4800 bits/s, full or half duplex over the switched network. Features include digital filters, digital automatic adaptive equalization, and diagnostic capability. The unit serves as a direct replacement for Western Electric 208B modems and incorporates front panel pushbutton controls and LED indicators. **General DataComm Industries, Inc,** One Kennedy Ave, Danbury, CT 06810.
Circle 210 on Inquiry Card

SINGLE-CARD, HIGH SPEED 128k-WORD CORE MEMORY



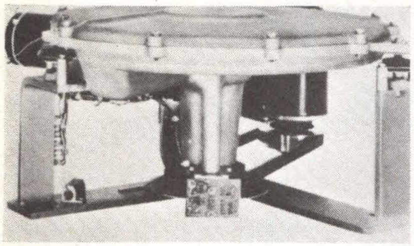
The 128k-word x 18-bit MAXI-STORE module combines mass storage with high speed for mini- and midscale computer uses. Cycle time is 750 ns and access time is 325 ns. It is expandable to 1024k words x 18 bits in a 19" (48-cm) rackmountable chassis with enclosed power supply. Planar card with address and data registers, and timing and control logic uses a 3-wire, 3D organization. It requires 5 and 15 Vdc. **Dataproducts Corp,** 6219 DeSoto Ave, Woodland Hills, CA 91364.
Circle 211 on Inquiry Card

MASS STORAGE DISC CONTROLLER FOR PDP-11

PM-DC11/300C consists of -DC11/300 disc controller, offline diagnostic logic, power supply, and fans for cooling in a 5.25" (13.33-cm) expansion chassis with front diagnostic control panel. Controller interfaces directly with the Unibus and uses CDC storage module disc drives. It replaces the DEC RH11-based disc systems and is software compatible with std DEC operating systems. Available for single or multidrive configurations, it has an unformatted capacity of 2G bytes/system when extended to full capability of 8 disc drives. **Plessey Peripheral Systems,** 17466 Daimler, Irvine, CA 92714.

Circle 212 on Inquiry Card

SEVERE ENVIRONMENT DISC DRIVE



Model 301D operates reliably in hostile environments under such conditions as 131 °F (55 °C), 10G shock, dust and dirt, humidity, vibration, and up to 45° tilt. Storage capacities of from 0.5M to 4M bytes are available with bit transfer rates of 1.1 and 2.5 MHz. Moving head type unit has a conversion wear coated fixed-disc rotating in a sealed chamber. Unit is provided with read/write and data separator electronics compatible with the 23.5/5440 type drives. **Digimetrix, Inc,** 20954 Corsair Blvd, Hayward, CA 94545.

Circle 213 on Inquiry Card

MILITARIZED THERMAL PRINTER

Nonimpact printer features 2 thermal printheads with no moving parts, each spanning 2" (5 cm) of paper width. Basic TP2000 is a 10-char/in (4/cm), 40-col unit that operates at a 240-line/min print speed. A 66-col, 17-char/in (7/cm) version is optional. Weighing <7 lb (3 kg), the device provides internal storage for 100 ft (30.5 m) of 4.25" (10.8-cm) wide roll paper. It measures 5.75 x 6.25 x 7.50" (14.61 x 15.88 x 19.05 cm). **Miltope Corp,** 9 Fairchild Ave, Plainview, NY 11803.

Circle 214 on Inquiry Card

LINE PRINTER SYSTEM FOR DECSYSTEM 20

LP-20 compatible interfaced line printer system can drive 2 printers simultaneously at speeds from 300 to 1500 lines/min. S-20 controller measures 5.25" high and 19" wide (13.34 and 48.3 cm) and can be installed in unused space in DECsystem 20. System includes controller, electronics, and all necessary cabling. **Southern Systems Inc,** 3000 NE 30th Pl, Ft Lauderdale, FL 33306.

Circle 215 on Inquiry Card

27-W SWITCHING POWER SUPPLY

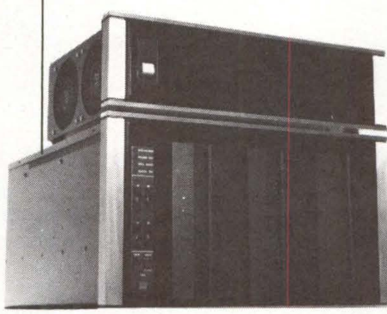
Low power series 2000, offering a 27-W, 4-output supply, has virtually noise-free operation. With a 60% efficiency, it operates on either 115 or 230 V. The reliable supply has been developed for data processing and communications applications to improve upon linear designs, while remaining cost competitive. It has received UL approval. **Conver Corp,** 10631 Bandley Dr, Cupertino, CA 95014.

Circle 216 on Inquiry Card

2 HIGH PERFORMANCE LSI-11* OEM SYSTEMS

THE FD/X3

☐ 3.75 Mbytes Floppy Disk on-line ☐ Three Drives ☐ Double Density ☐ Double Sided ☐ DMA Interface ☐ Switch Selectable Drives

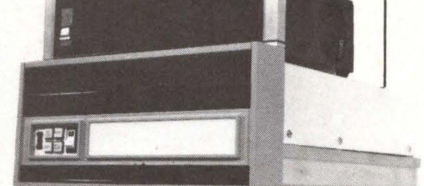


$11,000
Single Quantity Price

$7,500
Quantity 20 Price

THE CD/X3

☐ 20 Mbytes Cartridge Disk ☐ 3 Fixed and 1 Removable Platters ☐ 100% RK05 Compatible



$18,000
Single Quantity Price

$12,750
Quantity 20 Price

*Trademark of the Digital Equipment Corp.

Both Systems include: ☐ DEC LSI-11* CPU ☐ 61440 bytes RAM ☐ Serial I/O port (RS232 and 20 MA) ☐ Hardware Bootstrap ☐ Real Time Clock ☐ 16 QBus Slots ☐ Extended Instruction Set ☐ Floating Point Arithmetic ☐ RT-11 Operating System

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PRODUCTS

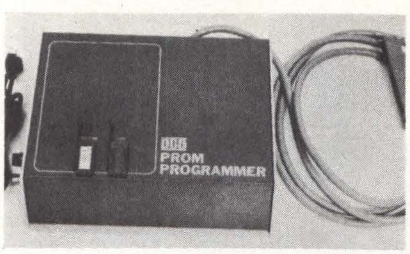
GAS DISCHARGE DISPLAY POWER SUPPLY

Power for 240- and 256-char matrix gas discharge displays can be obtained from low dc voltage with the E 1200 series power supply. Single-output unit converts 12- or 15-Vdc input to high voltage dc output. It may also be applied to any end use where battery or other low voltage dc input is available. I/O isolation is rated at 600 V rms (60 Hz, 1 min). Encased in aluminum, the supply weighs approx 185 g and measures 2 x 2.5 x 1.19" (50.8 x 63.5 x 30.2 mm). **Endicott Coil Co, Inc,** 24 Charlotte St, Binghamton, NY 13905.
Circle 217 on Inquiry Card

IBM COMPATIBLE GRAPHICS SUBSYSTEM

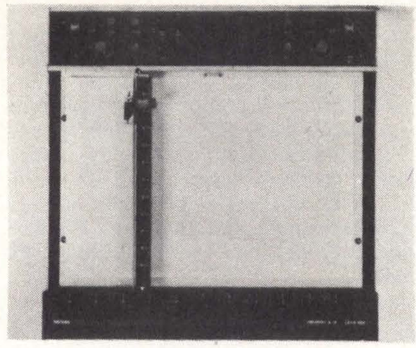
A 2- or 3-dimensional interactive graphics peripheral, plug compatible with IBM 360/370 channels, uses hardware and firmware to process channel protocol, error checking, and data/command buffering. Model 4370 reduces the burden on the host computer by performing all image manipulation and interrupt handling; software packages simplify development of applications programming on the host. Basic subsystem consists of a channel control unit, display control unit, and display station. **Adage, Inc,** 1079 Commonwealth Ave, Boston, MA 02215.
Circle 218 on Inquiry Card

HIGH DENSITY EPROM PROGRAMMER



Providing programming or copying capabilty for EPROMs, PB1002 programmer interfaces with MicroPac and SuperPac development systems; users select EPROM to be programmed by plugging in an adapter module. A control program provides all necessary functions. In addition to supporting 2708, 2758, 2716, and 2732 high density chips, instrument can read and verify object tapes, program an EPROM from RAM or copy socket, compare EPROM with RAM or copy socket, and transfer EPROM information into RAM. **Process Computer Systems, Inc,** 750 N Maple Rd, Saline, MI 48176.
Circle 219 on Inquiry Card

X-Y RECORDER



A high resolution instrument, the PM8131 plots up to the DIN A-3 format of 15 x 10" or 38 x 25 cm. Recorder is stable with minimal temp drift. Dynamic performance gives slewing speed of 95 cm/s and peak acceleration is up to 3800 cm/s^2 for Y axis and 2100 cm/s^2 for the X axis. Its high resolving power is attributable to its input sensitivity from 50 μV to 1 V/cm in 14 calibrated ranges for both X and Y axes. Cast in a sturdy aluminum frame, its construction and design are essential to its high degree of accuracy. Independent and fully variable zero offset facilities are provided on both axes. **Philips Test & Measurements, Inc,** 85 McKee Dr, Mahwah, NJ 07430.
Circle 220 on Inquiry Card

MOMENTARY CONTACT SWITCH

Disc switch features a flat momentary contact module requiring a shorter stroke, and can be covered by a Mylar overlay with graphics, or by std or rocker pushbuttons in individual, multiple, or tableau arrangements for designing keyboards on PC boards. Built around 2 contact diaphragms separated by insulating material, switch makes 3-point contact when upper diaphragm is pressed. Disc is totally sealed against moisture through insert molding and ultrasonic welding, allowing flow soldering through a freon bath without contact contamination. Other features include a self-cleaning principle and a broad range of switching power. **ITT Schadow Inc,** 8081 Wallace Rd, Eden Prairie, MN 55344.
Circle 221 on Inquiry Card

HIGH EFFICIENCY LED LAMPS

With externally attached current limiting resistors, 0.75" (1.91-cm) lamps operate at 5, 6, 12, 15, 24, and 48 V. Recommended operating currents range from 10 to 20 mA and typ luminous intensities range from 1 mcd to 10 mcd depending on model. Wide angle and high intensity lens configurations are available. All units can be panel mounted with the company's OC-4 mounting clip and are encapsulated in rugged epoxy lenses. **Opcoa Div of IDS Inc,** 330 Talmadge Rd, Edison, NJ 08817.
Circle 222 on Inquiry Card

SUBMINIATURE HALOGEN-CYCLE LAMPS

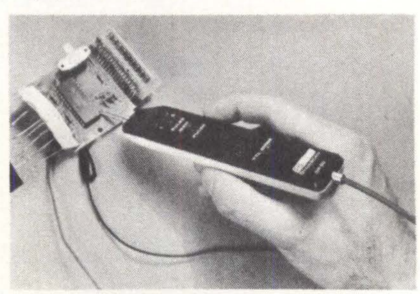
Lamps with single contact midget flange bases, which permit their use in std subminiature lamp holders, provide good electrical contact. Halogen-cycle lamp measures 0.188 x 0.625" (0.478 x 1.588 cm) and features a whiter light due to higher color temp. Lamps do not blacken with use as severely as comparable std incandescent lamps and maintain a higher percent of initial light output at 70% life expectancy. **General Electric Co, Lighting Business Group,** Nela Park, Cleveland, OH 44112.
Circle 223 on Inquiry Card

CRT/PRINTER SUBSYSTEMS

Package includes model 1100 interactive CRT which can operate up to 9600 baud, plus the 100-char/s model 650 page printer. CRT allows operator to carry out dialogue with a host computer at data rates almost 10 times higher than most teleprinters. When printing is requested, printer sets CRT free to resume dialogue with the host after 2 s. Package allows operator to print only summary results thus reducing paper waste. **Perkin-Elmer Corp, Terminals Div,** Randolph Park West, Rt 10 & Emery Ave, Randolph, NJ 07801.
Circle 224 on Inquiry Card

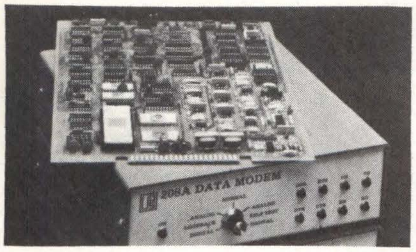
50-MHz LOGIC PROBE

Model DP-50 clearly displays in-circuit logic activity to simplify troubleshooting and analysis of digital circuits. Logic probe is compatible with TTL, DTL, RTL, HTL, CMOS, MOS, and high noise immunity logic. 3 bright LED indicators display pulse presence and high and low logic states. Unit continues to indicate pulse presence through max frequency of 50 MHz. Device is fully overload protected and will withstand $\pm$50 Vdc at the input. Min detectable input pulse width is 20 ns (10 ns typ). **Dynascan Corp,** 6460 W Cortland St, Chicago, IL 60635.



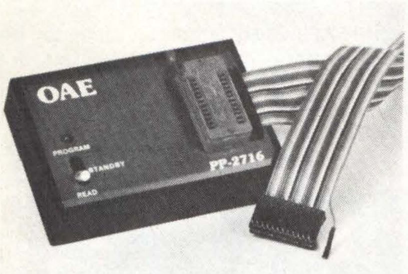
Circle 225 on Inquiry Card

4800-BIT/s DATA MODEM



Available for either 4- or 2-wire networks and as a freestanding unit or rackmountable enclosure, model 208 is Bell compatible. Enclosure accommodates up to 8 complete channels of 4800-bit/s communications and requires only 7" (17.8 cm) of space in a std 19" (48-cm) rack. Single card configuration is available which occupies <100 in^2 (650 cm^2) of PC board space. Applying a high speed microprocessor has resulted in a diminished component count and size reduction, with concurrent increases in modem reliability. **Universal Data Systems, Inc,** 4900 Bradford Dr, Huntsville, AL 35805.
Circle 226 on Inquiry Card

P/ROM PROGRAMMER



Designed for the single supply Intel 2716 EPROM, the PP-2716 connects to any read-only P/ROM socket via a 24-pin plug and 5-ft (1.5 m) of flat ribbon cable. Using the P/ROM socket interface (patent pending) data are sent over the 8 lower address lines to the programmer. No additional power supplies are required, and all timing and control sequences are handled by the programmer. Each instrument is supplied with an internal dc to dc switching regulator and zero insertion force socket. **Oliver Advanced Engineering, Inc,** 676 W Wilson Ave, Glendale, CA 91203.
Circle 227 on Inquiry Card

LIMITED-DISTANCE DATA MODEM

LDS 140 asynchronous modem transmits at speeds of up to 4800 bits/s over loaded or unloaded metallic circuits within a 12-mi (19.3-km) range. At 9600 bits/s, modem will transmit up to 6 mi (9.6 km) over unloaded metallic circuits. Modulation scheme does not require dc continuity. Modem includes controlled or constant carrier operation, local digital loopback, LED indicators, and signal quality monitors for easy installation. **Gandalf Data Inc,** 1019 S Noel St, Wheeling, IL 60090.
Circle 228 on Inquiry Card

3M/H-P COMPATIBLE SMALL DATA CARTRIDGE

Model TC-150 plastic cartridges can be used on drives manufactured by H-P, TI, Qantex, 3M, Instrumentation Technology Corp, and Candex Pacific. Compatible with 3M DC-100A and Hewlett-Packard 9162-0061 mini cartridges, the unit contains 140 ft (43 m) of 0.150" (0.381-cm) wide mag tape. Data storage capacity depends on the user's data format. Recording formats range from single-track 800 bits/in (314/cm) up to dual-track 1600 bits/in (629/cm). **Information Terminals Corp,** 323 Soquel Way, Sunnyvale, CA 94086.
Circle 229 on Inquiry Card

RP06 EQUIVALENT DISC SYSTEM

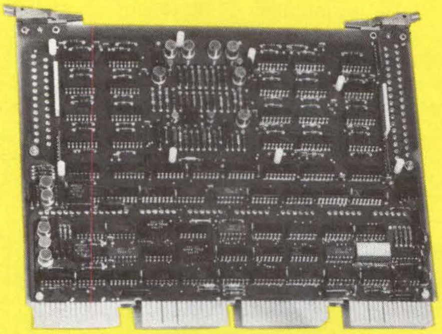
Compatible with DEC software, model CIT-200 is a low cost 200M- to 1600M-byte system containing up to 8 200M-byte drives and a DEC compatible controller/interface unit with cabling. Memorex model 677 disc drive supports overlapped seek and interleaved fetch and store, rotating at speeds of 3600 r/min, with 19 heads for 815 tracks. Advanced Electronic Design's controller and interface unit optionally supports up to 4 CPUs. **Computer Interface Technology,** 2080 S Grand Ave, Santa Ana, CA 92705.
Circle 230 on Inquiry Card

MICROPROCESSOR CORE MEMORIES

FOR THE LSI-11, 8080, 6800, IMP-16P, S100

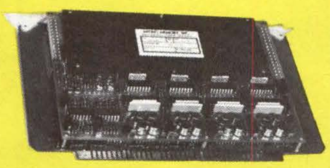
THE MM-1103 OFFERS 2 OR 4 TIMES THE MEMORY CAPACITY! FOR THE SAME SIZE AND POWER AS THE DEC MMV-11A!

MM-1103
8K X 16



MM-1103/16
16K X 16

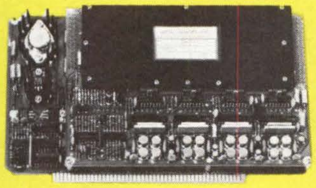
PLUGS DIRECTLY TO DEC LSI-11 AND PDP 11-03 COMPUTER



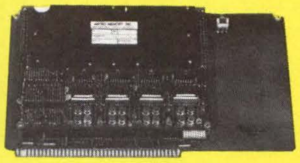
MM-6800 8K X 8
USED ON MOTOROLA'S EXORCISER AND MICRO MODULES

FEATURES:

- NON-VOLATILE.
- PIN-TO-PIN COMPATIBILITY.
- POWER MONITORING FOR DATA PROTECTION.
- DELIVERY FROM STOCK.
- ONE YEAR WARRANTY ON PARTS AND LABOR.
- ALL UNITS TEMPERATURE CYCLED AND BURNED IN.



MM-S100 8K X 8
USED ON IMSAI 8080, ALTAIR, AND SOL MICROCOMPUTER



MM-8080AL 8K X 8
USED ON INTEL'S MDS 800 AND SBC 80/10 MICROCOMPUTER

Micro Memory Inc

9438 Irondale Ave.
Chatsworth, California 91311
Telephone: (213) 998-0070

CIRCLE 84 ON INQUIRY CARD

MICROPROCESSOR BASED CRT TERMINAL

Designed around Z80 microprocessor, Video 200 offers computer control of formatting and editing capabilities, enabling host computer to guide terminal operators through data entry and retrieval. Full duplex keyboard allows nondisplay keys to be monitored by computer. Complete formats consisting of 16 different types of display attributes can be flashed onto the terminal's screen by the computer to aid operators in data entry. Unit features 12" (30.5-cm) screen with a 128-char ASCII display set with u/lc and control codes. **Western Union Data Services Co,** 70 McKee Dr, Mahwah, NJ 07430.
Circle 231 on Inquiry Card

COMMUNICATIONS SOFTWARE EMULATOR

Compatible with Univac's full-duplex Nine Thousand Remote (NTR) protocol, the software package enables a 1600 system with COS memory system to communicate with a Univac 1100 series host computer supporting NTR. Communications are in both ASCII and FIELDATA, at line speeds from 2k to 56k bytes/s. Std features include support of multiple data streams, and card reading and punching in column-binary format. Various options are available. **Harris Corp, Data Communications Div,** 11262 Indian Trail, PO Box 44076, Dallas, TX 75234.
Circle 232 on Inquiry Card

DOUBLE DENSITY FLOPPY STORAGE SYSTEM

An IBM compatible single- and double-density floppy disc storage system and controller, FT series features HIP (host interface processor) controllers for DEC and Data General microcomputers. HIP is an intelligent DMA controller which increases system throughput by offloading the CPU from disc I/O processing. Each system can provide 2.5M bytes of storage. 2-drive expansion enclosures are available. **Scientific Micro Systems,** 777 E Middlefield Rd, Mountain View, CA 94043.
Circle 233 on Inquiry Card

INTERACTIVE, REFRESHED GRAPHICS TERMINALS

Up to 4 DYNAGRAPHIC™ display terminals (models 3205, 6210, and 6220), with 19" (48-cm) CRTs, 92-key alphanumeric keyboard, and choice of lightpen or joystick, can be supported by 1 Dynagraphic minicomputer. Host/terminal software-hardware package lets users interactively develop and manipulate pictures and picture elements with FORTRAN calls. Terminal control program gives local control over functions; refreshed graphics allow manipulation and selective erase. **IMLAC Corp,** 150 A St, Needham Heights, MA 02194.
Circle 234 on Inquiry Card

9-V RECHARGEABLE NiCd BATTERY

This high capacity battery is suitable for replacing primary 9-V batteries, for use as a backup power source, and for use as standby power for semiconductor RAMs. Manufacturing technique for the mass electrode design results in a battery capacity of 110 mAh. Coupled with a discharge voltage of a nom 8.4 V, the device delivers as much as 924 mWh for each discharge cycle. A battery charger unit to be plugged into ordinary house current is also available. **Varta Batteries Inc,** 85 Executive Blvd, Elmsford, NY 10523.
Circle 235 on Inquiry Card

FOR AUTOMATIC INSERTION...

Switch to KEMET T322 precision molded axial leaded capacitors. The excellent lead concentricity of the T322 molded part is far superior to epoxy back-filled parts, and eliminates high-speed automatic insertion problems. The high-quality T322 gives you same size, same function, with more CV values. 0.1 to 68.0μF; −55°C to +125°C temperature range, 2 to 50 volts. For more information, write: Electronics Division, Union Carbide Corporation, P.O. Box 5928, Greenville, SC 29606. Phone: (803) 963-6300. Or see your local KEMET Representative.

KEMET— precision molded. Competition— epoxy back-filled.

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In Europe: Union Carbide Europe, S.A. 5, Rue Pedro-Meylan, Geneva 17, Switzerland. Phone: 022/47 4411. Telex: 845-22253.

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The original 'hands on' people

Hands on microprocessor short course with **FREE** take home microcomputer included in the $499 tuition.

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Oct. 23, 24, 25, 26, 27	Philadelphia, PA
Nov. 13, 14, 15, 16, 17	Palo Alto, CA
Dec. 11, 12, 13, 14, 15	Albuquerque, NM
Jan. 15, 16, 17, 18, 19	St. Petersburg, FL

Advanced Programming Course:
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Learn microprocessors first hand from the original hands on people.

For more information call Jerilyn Williams, (317) 742-6802 or write Wintek Corp., 902 North 9th Street, Lafayette, Indiana 47904.

WINTEK

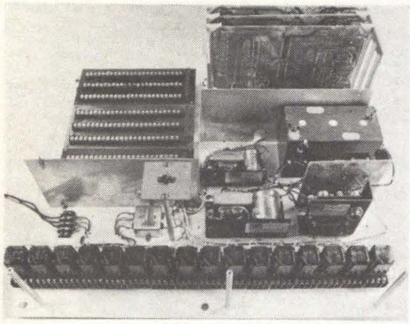
- **6800 Hardware/Software**
- **Custom Hardware/Software**
- **In-house short courses**

 CIRCLE 92 ON INQUIRY CARD CIRCLE 93 ON INQUIRY CARD

INDUSTRIAL MONITORING AND SUPERVISORY SYSTEM

Outpost 7/1 is a master station capable of handling up to 600 data points from up to 30 remote terminal units. System incorporates CRT, poller task, and operator interface via keyboard in English. Essential supervisory functions of monitoring, alarming, and reporting by exception, and using up to 20 custom CRT pages for data display are all performed by system. Operating features include Midget executive systems manager program and Microvisory applications program designed to lead an operator through the entry of data points into system. **Tano Corp,** 4521 W Napolean Ave, Metairie, LA 70001.
Circle 236 on Inquiry Card

MICROPROCESSOR BASED I/O MULTIPLEXER

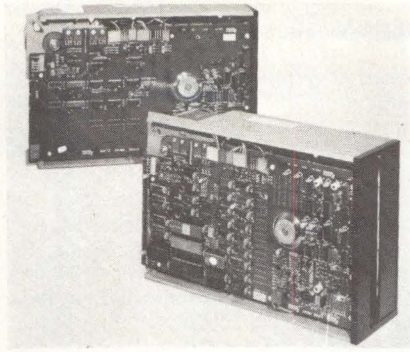


Mini-Terminal Unit (MTU) D4800, which may be located in close proximity to sensors/control units, is a complete intelligent multiplexer, functioning under control of the internal microprocessor. Modular in design, MTU accommodates various D-A requirements including up to 48 digital I/Os, 32 analog inputs, and 16 analog outputs. Unit communicates with a central processor by means of serial data on twisted pair cables. Entire unit mounts in a NEMA 1 enclosure measuring 24 x 30 x 10.5" (60.9 x 76.2 x 26.7 cm). **Electronic Modules Corp,** PO Box 141, Timonium, MD 21093.
Circle 237 on Inquiry Card

SHIELDED-PAIR DATA CABLE

Insulated with the expanded copolymer polyolefin Datalene™, which features low dielectric constant and dissipation factor for high speed, low distortion data handling, cable includes properties of crush resistance, light weight, and temp range of −40 to 80 °C. For applications requiring an impedance value of 150 Ω, a UL-listed 22-gauge stranded single pair with nom capacitance between conductors of 8.8 pF/ft (2.7/m) and nom dc resistance of 14 Ω/1000 ft (4.3 Ω/km), and a 2-pair 22-gauge solid conductor design with nom capacitance of 8.8 pF/ft (2.7/m) and nom dc resistance of 16.1 Ω/1000 ft (5 Ω/km) are available. **Belden Corp,** 2000 S Batavia Ave, Geneva, IL 60134.
Circle 238 on Inquiry Card

FLEXIBLE DISC DRIVES WITH CONTROLLER/FORMATTERS



Controller/formatter circuitry mounted on a single card within the diskette drive enclosure provides media compatibility with IBM 3740 and 3540 and System 32. Single-density subsystems are available as IBM compatible 26-sector format (1101), 128-byte full sector buffer (1102), or 16-sector format with 256-byte full sector buffer. Transfer rates are 31k bytes/s, or 250k bytes/s with buffering. 1200 series store 256k bytes in 26 sector, 295k bytes in 15 sector, and 315k bytes in 8-sector format. RFS2400 series add double-density encoding. **Remex Div, Ex-Cell-O Corp,** 1733 E Alton St, Irvine, CA 92713.
Circle 239 on Inquiry Card

If you're designing hard-copy OEM systems, here's the laser breakthrough you've been waiting for:

The OEM CR-135 WriteLite™ Modulated Laser from Coherent.

At last, a laser-writing system that is easy to design with, has a graphics capability, and a price that is easy to live with.

Coherent's WriteLite Modulated Laser is the first complete laser-writing subsystem. All the writing components are put together for you: the laser, the modulator, and the electronics. Just add your own scanning system or ask Coherent about that too.

Now you don't have to be a laser expert to be a laser user. The laser and modulator are integrated and pre-aligned in one small package. The 1.6mW minimum output power in the first diffracted order and 150 ns rise time are guaranteed.

All you have to do is plug in your TTL input. And the WriteLite is ready to write at six pages per minute or faster on standardly available photoconductors.

You might think that having the whole package systems-engineered and pre-aligned beforehand would run up the price. Quite the contrary. In OEM quantities, the WriteLite is priced to meet your strict design goals budget. So now laser writing capabilities are well within your reach.

And what capabilities!

WriteLites are now being used for:

Technology	Equipment
Xerographic	Copiers/non-impact printers
Photographic	Computer output micro-film/fascimile systems
Thermo/electro static	Oscillographic recorders

The WriteLite package is the very heart of non-impact printers, facsimile systems, CRT hardcopy recorders, direct writing, oscillographic recorders, COM systems and telecopiers. Just tell us what your system is and we'll show you how the WriteLite will save you time and money.

The breakthrough you've been waiting for. The CR-135 WriteLite Modulated Laser from Coherent. For complete information, write or call Coherent, 3210 Porter Drive, Palo Alto, CA 94304, 415-493-2111.

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Laser Division
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415-493-2111

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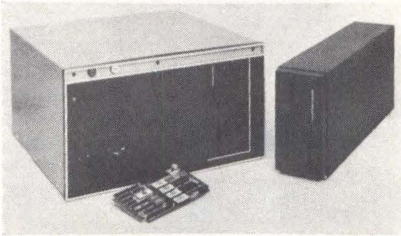
CIRCLE 85 ON INQUIRY CARD

PRODUCTS

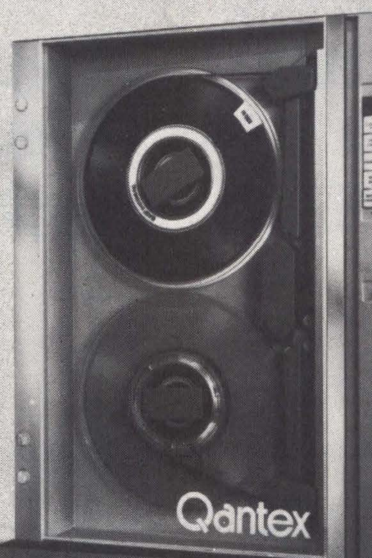
DISKETTE BASED INTELLIGENT MASS STORAGE SYSTEMS



With data capacities in 1M byte formatted, IBM compatible systems incorporate model 277 dual diskette drives and are available in 1- or 2-drive (2 or 4 spindle) with microprocessor based controller, power supply, and cabling in 19" (48-cm) rackmountable chassis, 1- or 2-drive without controller in cabinet, or slimline 4.5" (11.4-cm) wide vertical mounted system that incorporates 1 dual drive (2 spindles and power supply) in tabletop chassis. Avg seek time including settle is 33 ms; full 76-track seek is done in <100 ms. **PerSci, Inc,** 12210 Nebraska Ave, West Los Angeles, CA 90025.
Circle 240 on Inquiry Card

The difference is operational reliability

PDP-11
NOVA
ROLM
INTER DATA

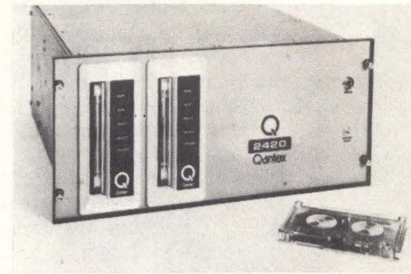


- *75 IPS Industry Compatible*
- *Controllers for Minicomputers*
- NRZ-800 BPI/PE-1600 BPI
- FLOATING SHUTTLE™ RESULTS:
  No tension arms/vacuum columns
  No down time/noise
- 300 IPS REWIND
- LOW POWER
- SOFTWARE COMPATIBILITY
- LOW COST

For more information on the Model TDX, call Leon Malmed, Sales Manager

Qantex DIVISION
NORTH ATLANTIC INDUSTRIES, INC.
200 TERMINAL DR., PLAINVIEW, NEW YORK 11803 • 516-681-8350 • TWX 510-221-1879

CARTRIDGE STORAGE UNIT WITH MILITARY INTERFACE

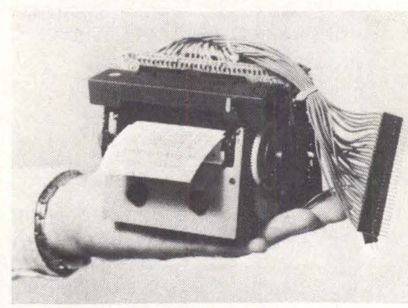


Commercial grade model 2420, a 5.7M-byte cartridge tape storage system, is compatible with all U.S. Navy computers, and is also a plug compatible alternative to the company's AN/USH-26, a Navy std MIL SPEC cartridge memory. For design, software development, and evaluation of military systems, the unit includes tape drive, ANSI compatible formatter, NTDS interface, power supply, and enclosure. **Qantex Div, North Atlantic Industries, Inc,** 200 Terminal Dr, Plainview, NY 11803.
Circle 241 on Inquiry Card

WORD PROCESSING SYSTEM PRINTER MULTIPLEXER

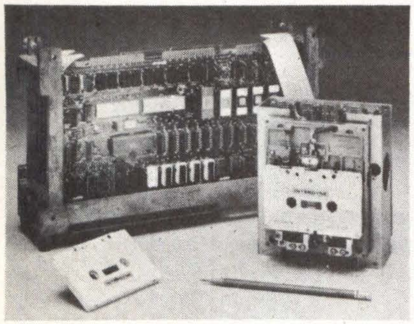
Three standalone Wordplex 1 word processing systems can share a common 45-char/s printer through the use of a multiplexer, to aid small print volume users generating large amounts of original, rather than repetitive, typing. The printer multiplexer is housed in a freestanding cabinet measuring 14.2 x 4.5 x 11.7" (38 x 13 x 30 cm). It weighs 5.5 lb (2.5 kg). Wordplex 1 systems can easily be upgraded to Wordplex 7 shared logic systems. **Dennison Office Systems Div,** 300 Howard St, Framingham, MA 01701.
Circle 242 on Inquiry Card

21-COL INSTRUMENTATION PRINTER



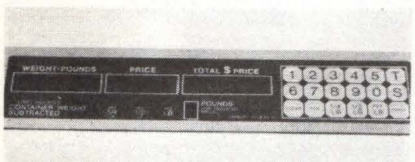
Model 388-21 impact printer can be operated with a 100% duty cycle at a print rate of 3 lines/s. Life is 5M printed lines. Large, fully formed char are printed in 2 colors using a replaceable ink ribbon cassette. The 3.5 x 5 x 4.1" (8.9 x 12.7 x 10.4-cm) printer uses std 2.75" (7-cm) wide paper rolls. Low noise is achieved through a printing principle that pinches paper and ink ribbon between char wheels and rubber platen. **Datacq Corp,** PO Box 3223, Monterey, CA 93940.
Circle 243 on Inquiry Card

SBC COMPATIBLE CASSETTE INTERFACE



IB 4100 plugs directly into the SBC 80 chassis and has I/O connectors for two IC 2500 series cassette drives. Driver software, provided in ROM which plugs directly into the SBC 80 board, performs data block formatting, error detection, and reads and writes to and from memory at 12 in (30 cm)/s, searches at 40 in (101 cm)/s, and rewinds at 120 in (305 cm)/s. Card and cassette drive add capacity of 0.5M bytes, data transfer rate of 1k bytes/s, and fast memory access. **Interdyne Co,** 14761 Califa St, Van Nuys, CA 91411.
Circle 244 on Inquiry Card

TACTILE RESPONSE CUSTOM KEYBOARDS



Tactile feedback keyboards provide quick and accurate contact, and have flat, spill resistant surfaces. Units are designed for a wide variety of configurations and insure high reliability through sealed mounting. Graphic possibilities available include legends, colors, sizes, shapes, and nomenclatures to meet functional and visual demands. **Bowmar Instrument Corp, Commercial Products Div,** 8000 Bluffton Rd, Fort Wayne, IN 46809.
Circle 245 on Inquiry Card

ANALOG-DIGITAL MULTIPLEXING SYSTEM

T-Wire system replaces wiring or reduces wiring costs with large installations. Handling up to 256 digital points (128 max each direction) plus 32 analog points (16 max each direction), microprocessor based system also communicates via 3-wire cable up to a max distance of 10,000 ft (3050 m). Basic system consists of 2 units which operate in a master-slave relationship. Hardware consists of 2 card file/terminal block panels. Prewired slots and terminals are provided for 14 digital I/O cards, 1 A-D card, and 2 D-A cards. **Tenor Co, Inc,** 17020 W Rogers Dr, New Berlin, WI 53151.
Circle 246 on Inquiry Card

2-DRIVE FLOPPY DISC CONTROLLER

A complete interface for Multibus compatible computer systems, the 8101 controller offers read throughput of 12,288 bytes/s and a write rate of 768 bytes/s. Fully compatible with Shugart SA 400 and 450 minidrives, and with SA 800 and 850 std drives, the single card can control 2 disc drives in single density operation. A FIFO full sector buffer is used for timing independence. Communication with the host computer is completely asynchronous. **Monolithic Systems Corp,** 14 Inverness Dr E, Englewood, CO 80110.
Circle 247 on Inquiry Card

UNINTERRUPTIBLE POWER SYSTEM

UPS design features controlled ferroresonant transformers in both inverter and battery charger. This closed loop method provides output voltage that is potentiometer adjustable and has regulation of <±1% under any condition of line or load. Transient response is 2 to 3 cycles for any load change with max overshoot of 15 to 20%. Overall efficiency is 70 to 80%. Units are available from 500 VA to 10 kVA with 120 or 240 Vac, 50 or 60 Hz, single-phase output. **Retelco, Inc,** 1260 Mercer St, Seattle, WA 98109.
Circle 248 on Inquiry Card

Give your PDP-11 a Calendar.

When you equip your computer with a TCU-100, you'll automatically have the date and time available when you power up.

It's an easy way to keep track of downtime, too. Furthermore, you can use the unit like an alarm clock. Set it to interrupt at preset times—or at intervals as short as 1/2048 second.

TCUs are shipped preset to your local time, but can be set to any time you want by a simple software routine. The built-in battery back-up is good for months with out computer power.

For the *LSI-11 user,* we offer the TCU-50 — the same reliable timekeeper without the interrupt capability. With either unit, time is cheap. The TCU-100 is just $495. And the TCU-50 is only $325.

Time is only one way we can help you upgrade your PDP-11 or LSI-11 system. We'd also like to tell you about the others.

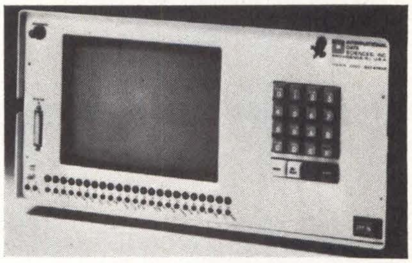
So contact Digital Pathways if you're into -11's. *We are too.*

DIGITAL PATHWAYS INC.
4151 Middlefield Road • Palo Alto, California 94306 • Telephone (415) 493-5544

CIRCLE 87 ON INQUIRY CARD

DATA NETWORK TEST SET

Expanded interactive and monitoring capabilities of the Hawk 4000 Datatrap are accessible through 2 menu pages that display instrument configuration status and guide the user through fault analysis procedures. The microprocessor controlled unit monitors, transmits, and receives data between a modem



and terminal, displaying them on a 9" (23-cm), 512-char screen; 4096 char can be trapped and stored. Various protocols and formats are std. **International Data Sciences, Inc,** 100 Nashua St, Providence, RI 02904.
Circle 249 on Inquiry Card

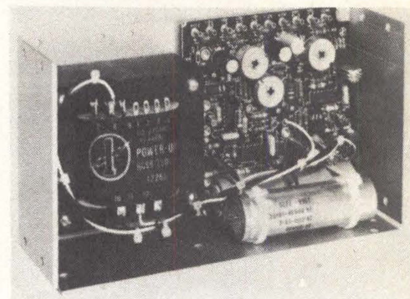
POWER CONDITIONER

Protection against short and longterm voltage fluctuations—a major source of computer error, program loss, and system damage—can be obtained with the 10- to 100-kVA power conditioner models. When utility power goes above or below rated voltage by 20%, it is instantly corrected to within 5% of rated voltage. Dual filtering system virtually eliminates faults and transients. Specs include efficiency of 96% and response time of 1 cycle. **Topaz Electronics,** 3855 Ruffin Rd, San Diego, CA 92123.
Circle 250 on Inquiry Card

OPTICAL SWITCHES

Epoxy backfilled switches are hermetically sealed in Valox[R] housings, and use glass-lensed IREDs for max environmental protection. CLI 200 and 210 have phototransistor outputs with switching speeds of 5 to 15 μs; 220 and 230 have darlington phototransistor outputs with 2- to 10-mA sensor current levels. The 305 provides an emitter follower output and 0.005" (0.127-mm) slit over the sensor aperture. The 325 and 355 have photodarlington outputs for 3- to 12-mA sensor current levels; 375 and 395 have phototransistor outputs and typ 5-μs switching speeds. **Clairex Electronics,** 560 S Third Ave, Mount Vernon, NY 10550.
Circle 251 on Inquiry Card

TRIPLE OUTPUT DC POWER SUPPLY



HCAA-60W, built in industry-std package size for 60-W, 3-output openframe power supply, outputs 5 V at 6 A with overvoltage protection, 12 to 15 V at 1.0 A, and −12 to −15 V at 1.0 A. −12 to −15-V output may be changed to −5 V at 0.4 A by jumpering two PC board terminals. Total isolation between 5 and ±12 V to ±15 V outputs allows user to arrange polarities to suit the application. Std features include 115/230 Vac ±10% input capability, ±0.05% line and load regulation, and full protection against short circuit and overload. Max output ripple is 3 mV pk-pk. **Power-One, Inc,** Power-One Dr, Camarillo, CA 93010.
Circle 252 on Inquiry Card

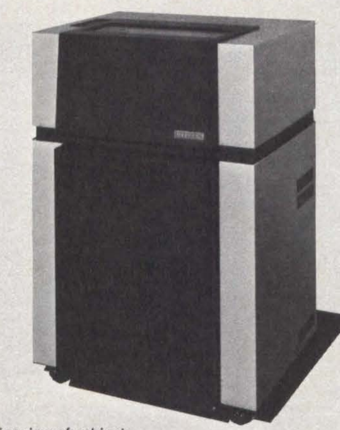
HYBRID CHARGE SENSITIVE PREAMPLIFIER-DISCRIMINATOR

The PAD preamplifier, discriminator, and pulse shaper in a TO-8 package can be mounted next to the anode of a charge producing detector to simplify complex multidetector systems. Model A-101 can detect a fast rising (<20 ns) charge pulse exceeding a charge of approx 0.16 pC. Interfacing with CMOS and low power TTL, the unit requires 15 mW of power. Input sensitivity and output pulse width are externally adjustable. The device also has an output pulse width that is variable with external trim capacitor. **Amptek,** 6 De Angelo Dr, Bedford, MA 01730.
Circle 253 on Inquiry Card

CITIZEN SERIES 8000 PRINTERS

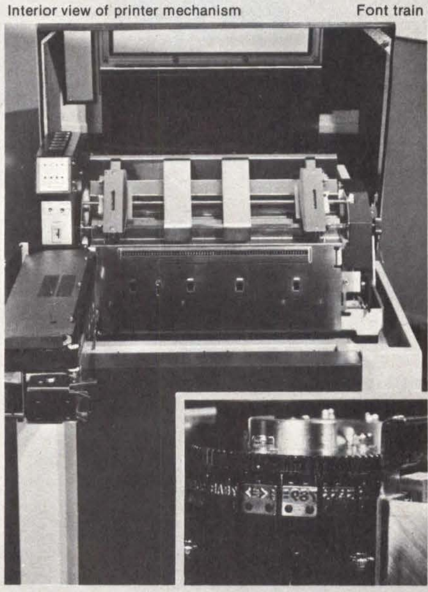
heavy-duty
132 Columns
250-720 LPM
Chain Printer
Excellent Quality and Price

Manufactured by
CITIZEN WATCH CO.
Tokyo, Japan



Exterior view of cabinet

Interior view of printer mechanism — Font train



If you are an OEM in the computer industry, you know the crucial importance of gaining a competitive edge. We know it, too.

CITIZEN is the largest independent line printer manufacturer in Japan. We are new in the U.S. market. A very tough market. And we are growing fast because we offer our clients a very advantageous price/performance mix. The competitive edge.

The Citizen Series 8000 Line Printers are available in two basic models, with the following minimum speeds:

Model 8201		Model 8601
298 LPM	— 48 characters —	720 LPM
250 LPM	— 64 characters —	600 LPM
188 LPM	— 96 characters —	444 LPM

Full details on the competitive edge offered by the Citizen Series 8000 printers are yours for the asking. Call or write to:

Mike M. Fujiwara
Marketing Manager, Line Printers
C. ITOH ELECTRONICS, INC.
5301 Beethoven Street
Los Angeles, California 90066
Telephone: 213/390-7778

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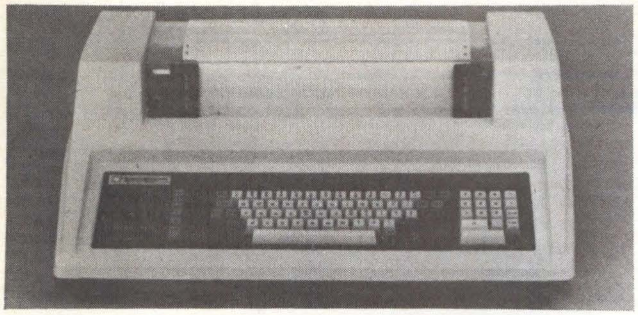
 CIRCLE 88 ON INQUIRY CARD

KEYBOARD SEND/RECEIVE TERMINAL



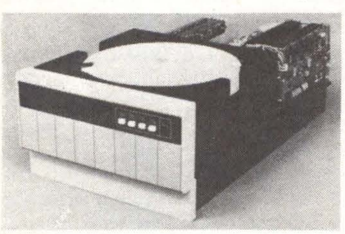
The OMNI 800™ model 820 features quiet operation, 150-char/s printing of an original and 5 copies with a 9 x 7 dot matrix format, a full 128 alphanumeric char ASCII keyboard, a 640-char FIFO buffer, and answerback memory. Other std features include keyboard selectable baud rates, a preprogrammed self-testing capability, and serial asynchronous data communication at rates from 110 to 9600 baud. Noise level is below 60 dBa. Microprocessor design technology provides control of printing functions, programmable forms control, and a buffered communications interface. Options include a compressed character font, numeric cluster, full ASCII/APL keyboard, international character sets, and device/forms control. **Texas Instruments, Inc, Digital Systems Div,** PO Box 144, Houston, TX 77001.
Circle 254 on Inquiry Card

INTELLIGENT CLUSTERED TERMINAL SYSTEM

System 4000 is completely programmable and is able to emulate a variety of communications protocols as well as perform onsite processing within a cluster using local disc storage. Built-in emulators allow the system to function in IBM 3270 and 2260, Univac UTS 400, and Honeywell 7700 terminal modes, cutting line costs by concentrating data. Each cluster may consist of a cluster controller/processor; communications controller, floppy disc storage for up to 1M byte, keyboard/display stations, and high and low speed line and character printers. System can support 8 keystations and 4 printers simultaneously. Cluster controller includes a microprocessor, up to 32k bytes of RAM, and function and task oriented microprocessor modules. **Racal-Milgo, Inc,** 8600 NW 41st St, Miami, FL 33166.
Circle 255 on Inquiry Card

CARTRIDGE MODULE DISC DRIVE FAMILY

Offering removable and fixed disc storage with capacities ranging from 32M to 96M bytes, the Hunter family provides backup and copy capabilities in single drive systems. Storage is divided between 16M bytes of top loading 5440-type cartridge and 16M, 48M, or 80M bytes of fixed storage. All data are contained on 1, 2, or 3 fixed discs and the removable cartridge. Using existing 3330-type technology, the drives transfer data at a rate of 1209k bytes/s with an avg access time of 30 ms. They have a rotational speed of 3600 r/min, track density of 370 tracks/in (145/cm), and recording density of 6060 bits/in (2385/cm). Compatibility with Trident and storage module drives allows users to intermix types on a single controller. **California Computer Products, Inc,** 2411 W LaPalma Ave, Anaheim, CA 92801.



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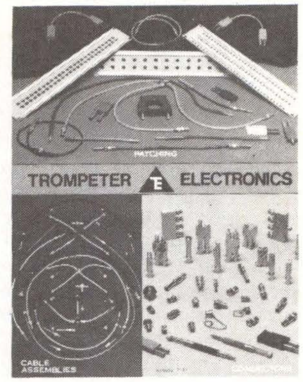
NEW FREE CATALOG



TROMPETER ELECTRONICS has just published a new 40 page catalog T11, illustrating a complete line of coax, twinax, triax and quadrax connectors, patch panels, plugs, jacks, patch cords, cable assemblies, networks and accessories. The catalog includes an eight page technical discussion of noise in cable systems.

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PRODUCTS

300/600-LINE/MIN BAND PRINTER

High reliability for heavy-duty uses and low operating noise levels—62 dBA with optional cabinet and 65 dBA on pedestal stand or desktop—are features of printer series. Included are the L300, which prints a std 64-char ASCII set at 300 lines/min; the L600, rated at 600 lines/min; and the L250G, offering a 15-char/in (6/cm) compressed printing capability and 720-point/in^2 (112/cm^2) graphics printing capability, in addition to normal 10 pitch printing and 300-line/min operation. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173.
Circle 257 on Inquiry Card

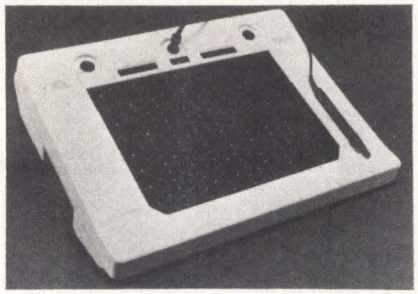
HARDCOPY DATA COMMUNICATIONS TERMINAL

PERT (printing economy remote terminal) provides 48-char/line capability on a continuous roll of ribbonless thermal paper. Modular design allows a choice of options including rechargeable battery or 110-Vac power, line level or acoustic telephone line connect, or direct computer connect with 20-mA loop or RS-232. Data transfer rates are selectable between 110 and 9600 baud. Std ASCII uc keyboard provides status indicator lights. The unit is compatible with all std computer formats. **Micon Industries,** 252 Oak St, Oakland, CA 94607.
Circle 258 on Inquiry Card

SERIES/1 COMPATIBLE 600-LINE/MIN PRINTER

Operating at twice the speed of the IBM 300-line/min band printer, the DAC/1-600 features 132 col/line, self-test, 8-channel vertical format unit, 6-part forms capability, and line printer attachment. Other features are single line memory buffer, EBCDIC or ASCII 64-char set and coding, Data Printer Corp's ChainTrain^R design, and open Gothic char style. Spacing is 10 char/in (4/cm) and 6 lines/in (2.4/cm), with paper slew rate of 20 in (51 cm)/s. **Digital Associates Corp,** 1039 E Main St, Stamford, CT 06902.
Circle 259 on Inquiry Card

LED BASED COMPUTER TERMINAL



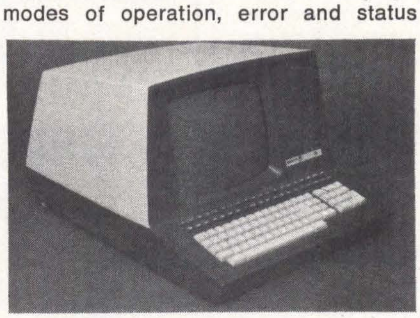
An interactive terminal consists of a panel of 128 LEDs (or 256) which, when a fiber optic pen is pointed at them, responds by lighting or extinguishing LEDs and/or by illuminating a numeric display on the panel. TRUEDATA serves the functions of a data input keyboard, visual display unit, and printer. LEDs required for an application are annotated and printed on an overlay of metal, paper, film, or plastic covering the panel. **Grundy & Partners Ltd,** Bond's Mill, Stonehouse, Gloucestershire GL10 3RG, England.
Circle 260 on Inquiry Card

MILITARY BOARD-TO-BOARD CONNECTOR

Digi-Klip^R tandem connector bus is rugged and provides rapid access for analysis and repair, requiring no motherboards, cables, or wirewrap. After formation BeCu connector is heat treated to guarantee low contact resistance. MC-18 and MC-19 tandem connectors will accommodate 0.062" (0.157-cm) thick PC boards. -18 is available in 2- to 22-board positions on 0.400" (1.016-cm) centers between boards; -19 has 0.500" (1.27-cm) centers between boards. **Components Corp,** 6 Kinsey Pl, Denville, NJ 07834.
Circle 261 on Inquiry Card

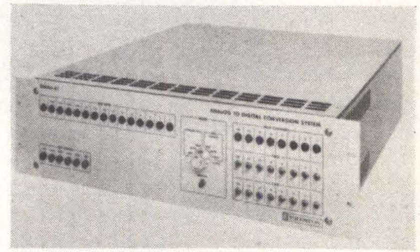
BUFFERED VIDEO DISPLAY TERMINAL

Micro Bee 2 is an 8085A microprocessor controlled terminal with 24-line x 96-char display format and keyboard for interactive and batch mode uses. Features include memory lock; normal, reverse, blink, underline, and half-intensity video levels; and protected data fields, numeric only fields, and modified data field transmission. Firmware displays modes of operation, error and status



messages, and communication protocol. **Beehive International,** 4910 Amelia Earhart Dr, Box 25668, Salt Lake City, UT 84125.
Circle 262 on Inquiry Card

ADC FOR DIRECT MINICOMPUTER INTERFACING



GMAD-4A includes an analog signal amplifier whose gain can be controlled over the range from unity to 16 by a 3-bit digitally coded signal supplied by minicomputer or controller. Range of control permits the data conversion system to be optimized for resolution on a channel by channel basis. When equipped with 15-bit ADC, range of amplifier gain permits digital resolution of input signal changes as small as 38 mV. Modular construction permits addition of cardmounted multiplexers. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.
Circle 263 on Inquiry Card

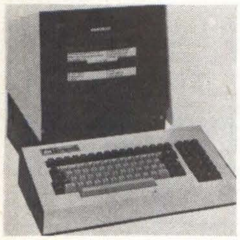
BUSINESS APPLICATION CRT TERMINAL

Model 531 has a memory size of 1920 uc ASCII char displayed in a 24-line x 80-char format. It includes 3 char accents, formatted data entry, buffered RS-232 printer output, and char and line edit functions. Terminal's 82-key detachable keyboard includes a TTY pad, numeric pad, and function key pad which contains 12 keys used for editing and related terminal functions. Up to 10 remote monitors can be daisychained through its auxiliary video output. **Ann Arbor Terminals, Inc,** 6107 Jackson Rd, Ann Arbor, MI 48103.
Circle 264 on Inquiry Card

SCALABLE ABSOLUTE ENCODER FOR SEVERE ENVIRONMENTS

Encoders convert any shaft input to BCD or binary information corresponding directly to the shaft angle with an accuracy of ± 1 part in 3600. In addition, 3-, 4-, or 5-digit, 0.5" (1.27-cm) high LED displays of that angle are available. DIGI-SHAFT system uses a shaft transducer that is a reliable resolver. The zero point can be reset to any value via an available offset adjustment; any output scale factor can be provided. Multiple shafts can be encoded simultaneously. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.
Circle 265 on Inquiry Card

BUFFERED APL/ASCII VIDEO TERMINAL



A buffered APL/ASCII terminal with transaction processing capability, the Elite 3045A offers protected formats, video enhancements, and APL overstrike/ASCII underscore. The microprocessor based terminal features character interactive, line, or page mode communications to meet a variety of applications needs; asynchronous and optional isochronous communications interfaces; 102 and 202 modem compatibility; and switch selectable EIA and optional 20-mA current loop interfaces. It also provides 10 user function keys, multiple level video display capability with no memory address space required to support screen enhancements, detached keyboard for expanded applications flexibility, and 15 baud rates up to 9600, selectable from the keyboard. **Datamedia Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.
Circle 266 on Inquiry Card

MINICOMPUTER WITH HIGH DENSITY MEMORY

Providing reduced cost, size, and power consumption with increased processing power, memory size, and throughput, the -16/460 minicomputer uses HYPAK, a high density memory technology based on hybrid circuit packaging which packs 256k bytes of memory with full 6-bit error correction facilities on a single 13 x 15" (33 x 38-cm) board. Memory modules contain eight 4k MOS dice in a std DIP. A computer with 1M-byte memory requires 8.75" (22.22 cm) of std rack space. 6-bit error correction facility detects and corrects all single bit errors and detects all 2-bit errors, providing uninterrupted operation for extended periods. **General Automation, Inc,** 1055 S East St, Anaheim, CA 92803.
Circle 267 on Inquiry Card

MICROPROCESSOR BASED PROGRAMMABLE CONTROLLER

MPC-8/01 is programmed for logic diagram language, but can be modified by changing the firmware to accept ladder diagram or Boolean statements. A system can have a single I/O rack with as few as 8 inputs and 8 outputs, or as many I/O racks as needed up to 2048 digital inputs and outputs. Input modules may be selected from 240- or 120-Vac; 225-, 24-, or 5-Vdc modules. Output modules may be chosen from 120 or 240 Vac at 5 A, 120 Vac at 1 A, 30 Vdc at 1 A, or 53 Vdc at 0.5 A, reed relay, mercury-wetted relay, or 5-V logic outputs. System has capacity for 6k (8-bit) scratchpad memory and up to 24k (16-bit) user program memory, which may be EPROM or RAM in any combination. Internal timing to 999.9 hours, minutes, seconds, or tenths of seconds, and counting to 9999 is available. **Dynage, Inc,** 1331 Blue Hills Ave, Bloomfield, CT 06002.
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GRAPHICS DISPLAY PROCESSOR

GDP/2A vector graphics display has the ability to draw 3M 0.1" (0.254 cm) vectors/s. Electrostatic deflection in the 19" (48.3-cm) CRT and completely digital vector drawing circuitry ensure perfect end-point closure between vectors and uniform intensity. Display processor has a complete instruction set which fully exploits the power of a totally refreshed display. Control instructions affect vector intensity, XY positioning, scaling, and program flow. Single byte vector format provides compact storage while 4-byte format gives full screen size capability. **Three Rivers Computer Corp,** Box 235, Schenley Pk, Pittsburgh, PA 15213.
Circle 269 on Inquiry Card

NEEDLE GUIDES FOR IMPACT DOT MATRIX PRINTERS

Needle guides can be supplied in regular 7- or 9-hole inline types, or 10, 11, 12, 13, and 14, as well as to customer requirements; for OCR applications, holes can be provided in multiple numbers of rows. Guides are available with flat or curved surfaces facing the printing ribbon, assembled or unassembled. They are offered in single crystal alumina, Al_2O_3, or multicrystal alumina with grain size below 1 micron, both with zero porosity. **Imetra, Inc,** 200 Clearbrook Rd, Elmsford, NY 10523.
Circle 270 on Inquiry Card

120M-BYTE MOVING HEAD DISC MEMORY

Compatible with HP 3000 computer systems, the 7925 with 120M bytes of H-P formatted data storage in a removable disc pack is readily adapted to the equipment of other manufacturers. Average random seek time is 25 ms; data transfer rate is 7.5M bits/s, or 937.5k bytes/s. The controller can handle up to 8 drives. One surface of the pack carries servo information for the track follower, head actuating mechanism. Error correction code hardware is std. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.
Circle 271 on Inquiry Card

125-IN/s TAPE DRIVE

Mod 14 is format selectable, reading and recording 1600 char/in (629/cm) in PE format and 800 char/in (314/cm) in NRZI. Both formats can be implemented in the same unit for dual density recording. It accepts either IBM Easy-Load I and II type cartridges as well as ANSI compatible open reels up to 10.5" (26.7 cm) in dia. Built-in daisy chain capability permits up to 4 units to operate from the same formatter. Extra long vacuum columns reduce moving parts and provide better performance. **Wangco Div of Perkin-Elmer Corp,** 5404 Jandy Pl, Los Angeles, CA 90066.
Circle 272 on Inquiry Card

12-V, 120-mA MODULAR SUPPLY

Miniature 21-12 power supply measures 1.75 x 2.25 x 1" (4.45 x 5.72 x 2.54 cm), and weighs 5.3 oz (150 g) The transformer is vacuum impregnated. Output voltage is 12 V ±1% at 120 mA, line and load regulation are ±0.1%, and noise and ripple are <2 mV rms. Short-circuit protection includes foldback current limiting. Input power is 115 Vac ±10% at 50 to 400 Hz. Inputs of 100 and 220 Vac at 50 Hz are also available. **Calex Mfg Co, Inc,** 3355 Vincent Rd, Pleasant Hill, CA 94523.
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ROM Boards
for bootstrap programs and other types of fixed data and program data

- Model 20-101 with 128-Word ROM—$295*
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- Model 20-102 with 256-Word ROM—$345*

*Price includes detailed Operation & Maintenance Manual. Programming services available. Quantity discounts given.

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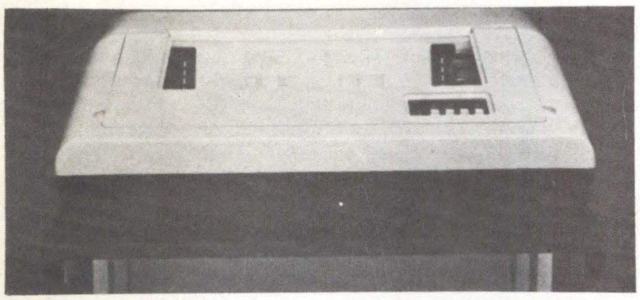
COMMUNICATIONS FLOPPY DISC SYSTEM

Comm-Stor II uses IBM 3740 compatible diskettes and interfaces with RS-232 communications devices. Its internal microprocessor enables the user to store and retrieve files by file source. Variable length files increase file storage capacity and maximize usage of the diskette regardless of mix of file sizes. Merging files capability increases editing capability and gives more flexibility in text editing applications. The system provides buffering at terminal and/or modem port allowing commands and data to be stacked, minimizing handshaking and system delays, and providing protection from data overruns. Individual file protection allows selected files to be specified as protected, while retaining the ability to create or alter others. **Sykes Datatronics, Inc,** 375 Orchard St, Rochester, NY 14606.
Circle 274 on Inquiry Card

180-CHAR/s BIDIRECTIONAL MATRIX PRINTER



300 series Ballistic™ printer features a built-in microprocessor that provides control of all print functions, 15 switch-selectable form lengths, 15 perforation skipover formats, and complete vertical and horizontal tabulation control. Processor also enables the printer's 128 printables to be expanded to 2 sets of 128 for alternating character sets on a line by line basis. A space and blank character compression buffer looks ahead as data are received, automatically compressing all space and blank character counts into 1-, 2-, or 3-byte strings allowing slew rates of 50 in (127 cm)/s for increased throughput. Serial interface (310) comes std with a 512-char buffer; parallel (301) version has a 256-char buffer. Both expand to 2048 char as an option. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst, Anaheim, CA 92803.
Circle 275 on Inquiry Card

FLEXIBLE DISC STORAGE TERMINAL

TermiNet® diskette storage terminal (DST) requires no coded commands; instead, a set of English language commands like write, read, and erase actuate the unit. All operator switches and LED indicators are on the front control panel. Measuring 17.82 x 12.62 x 16.62" (45.26 x 32.05 x 42.21 cm), the single unit drive weighs 30 lb (13.5 kg), while the dual unit weighs 45 lb (20 kg). Terminal is configured as an independent unit with two RS-232 ports; one for computer peripherals, the other for a data set. It is compatible with Bell 212A data sets. Storage media is an IBM compatible soft sectored, single-sided flexible, magnetic diskette which has usable storage capacity of 231,800 char in a single unit with average access time of 463 ms. ASCII coded data are transmitted and received in serial asynchronous form at various baud rates. **General Electric Co, Data Communication Product Business Dept,** Waynesboro, VA 22980.
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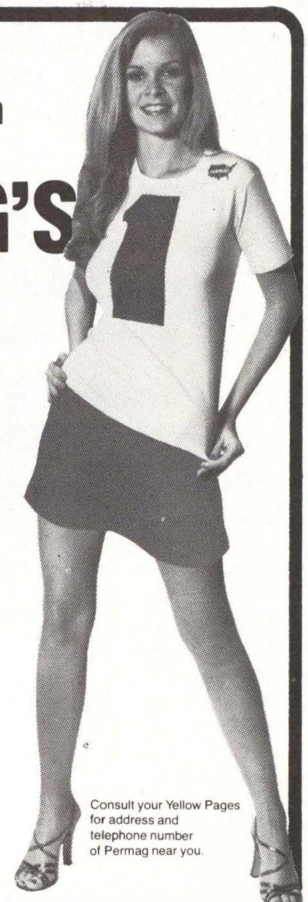

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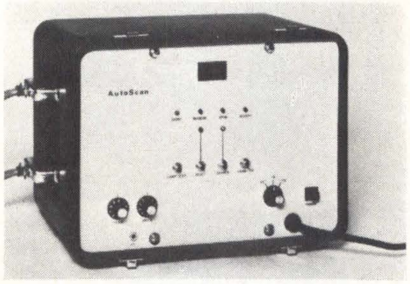
PRODUCTS

WIRE/CABLE ASSEMBLY FAULT TEST INSTRUMENT



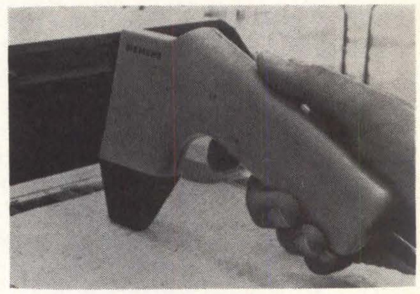
In either production testing or field troubleshooting, portable Autoscan will indicate nature of each fault (short, open, or miswire) and display its pin number. A from-to button permits display of pin number at destination end of a short or miswire defect. 2 std models, one with 99-wire capacity and the other with 49-wire capacity, are self-contained, solid-state, and use LED displays. Units measure 9 x 11 x 12" (22.9 x 27.9 x 30.5 cm) and weigh 12 lb (5.4 kg). An optional 5-col printer unit automatically prints out identity and nature of fault on paper tape. **Muirhead Inc, Addison Div,** 1101 Bristol Rd, Mountainside, NJ 07092.
Circle 277 on Inquiry Card

IBM COMPATIBLE DISPLAY TERMINAL

Multifunction C-760 includes a microprocessor controlled keyboard and visual display, ROM, 49,152-char RAM, flexible disc storage and controller, and simple forms programming language. Display is compatible with IBM 2770, 3770, and 3780 terminals and provides data communication with a host computer at speeds of 1200 to 9600 bits/s. Up to 2000 char of data can be displayed in a format of 25 lines with 80 char/line. A simple forms language and an optional business version of the BASIC compiler support user programmability. **Control Data Corp,** Box O, Minneapolis, MN 55440.
Circle 278 on Inquiry Card

HANDHELD OCR SCANNER

Device consists of a pistol grip scanner and a logic controller connected by a flexible cable allowing user ample room for manipulating scanner in a working environment. Information read is transferred at 140 char/s to a data terminal. In operation, read head is passed over a line of type set in OCR font; optics in read head create an image of information on a photodiode matrix. Brightness levels of the scanned area are converted to electrical signals. Information is transferred to interfacing data terminal in bit-parallel and char-



acter-serial fashion. **Siemens Corp, OEM Div,** 1440 Allec St, Anaheim, CA 92805.
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DISC BASED MULTIFUNCTION TERMINAL SYSTEM

Serving as word, distributed, or business data processing system, the 64k J500 Videocomputer displays 1920-char on 24 x 80 CRT screen and has a movable keyboard with 20 programmable function keys, and 4 cursor control keys. 2 floppy disc drives accommodate up to 2M char of storage; 2 additional units may be connected. The unit also supports up to 4 cartridge disc drives, 45- or 55-char/s or 300 line/min printer, as well as different communications protocols on 2 communication lines at std baud rates to 9600 baud. **Jacquard Systems,** 1639 11th St, Santa Monica, CA 90404.
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The INTERDATA interface solution

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Forecasts are also furnished by custom vs. standard, by product type — AC to DC, DC to DC, AC to AC and DC to AC, and for power supply components — inductors, capacitors and semiconductors. The industry structure is analyzed, and company profiles are supplied on the leaders with market volume and share information presented. Pricing trends, technological trends and product characteristics are discussed. Special emphasis is made to distinguish the captive and available non-captive markets.

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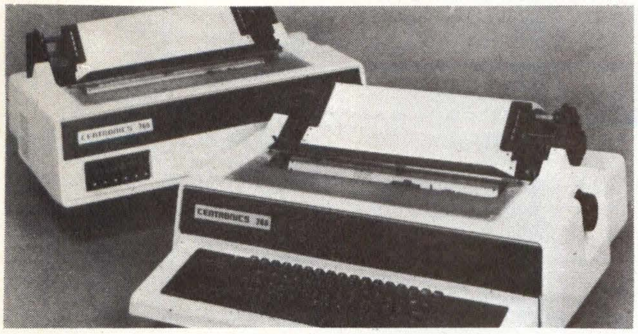
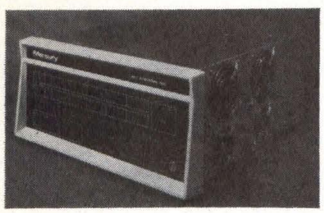
1200-BIT/s DOT MATRIX IMPACT TELEPRINTER



Capable of sustaining 1200 baud and printing at a min of 200 char/s, microprocessor controlled model 765 combines high speed features to generate characters at 1200 bits/s without loss of data. Features include a min 200-char/s print speed from a high speed printhead, bidirectional printing to eliminate time consuming carriage returns, a logic seeking printhead that enables the printer to seek the nearest character of the next printline, a 15-in (38-cm)/s slew rate, 1k-char buffer, and a servo carriage drive for simple, reliable operation. 10-, 12-, 15-, or 17-char/in (3.9, 4.7, 5.9, or 6.7/cm) printing density selectable under host or keyboard program control allows users to generate printed output up to 224 col. Switch selectable baud rates are 300, 1200, 2400, and 9600. **Centronics Data Computer Corp,** Hudson, NH 03051.
Circle 281 on Inquiry Card

GENERAL PURPOSE 16-BIT MINICOMPUTER

Compatible with the Nova™ series, Mercury 3 accepts any I/O controller which meets data channel requirements of the Nova series. CPU combines three 160-ns microprogrammable processors; concurrent handling of memory, I/O device, and ALU functions provides high throughput. 4 general purpose registers are provided along with hardware stack and frame pointers. Hardware multiply/divide, real-time clock, power fail, and auto restart are std features.



Both semiconductor and core memories are available and may be directly addressed up to 128k bytes. Larger capacity memories use unique mapping to avoid speed deterioration. High current capacity (40 A at 5 V) along with 93 I/O pins allow complex I/O interface arrangements. **SCI Systems, Inc,** 8600 S Memorial Pkwy, Huntsville, AL 35802.
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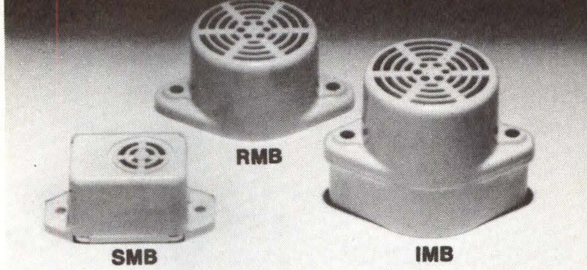
PHOTODETECTORS/EMITTERS FOR FIBER OPTICS

Infrared emitting diodes and spectrally matched detectors with sensitivities suited for short, medium, and long length fiber cables are offered in selected glass lensed metal packages compatible with AMP fiber optic connectors. Devices are suited to low frequency transmission of digital pulse signals through the insulating fiber media. Emitters offer power outputs at 50-mA drive current of 550 and 1600 μW, radiant intensities of 4.0 and 11.6 mW/steradian, and response times of 50 and 250 ns for the -100 and -200, respectively. Detector MFOD100 has sensitivity of 18 μA/mW/cm^2 with rise and fall times of 1.0 ns. -200, a 1-transistor silicon sensor, has sensitivity of 5.6 mA/mW/cm^2 with rise time of 2.5 μs and fall time of 4 μs. A Darlington photodetector, the -300 offers sensitivity of 75 mA/mW/cm^2 with 40- and 60-μs rise and fall times, respectively. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.
Circle 283 on Inquiry Card

Buzzzz.
(Write for new catalog.)



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CIRCLE 99 ON INQUIRY CARD

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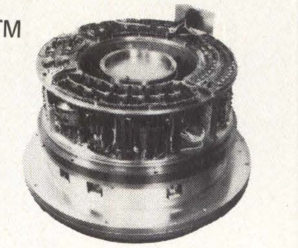

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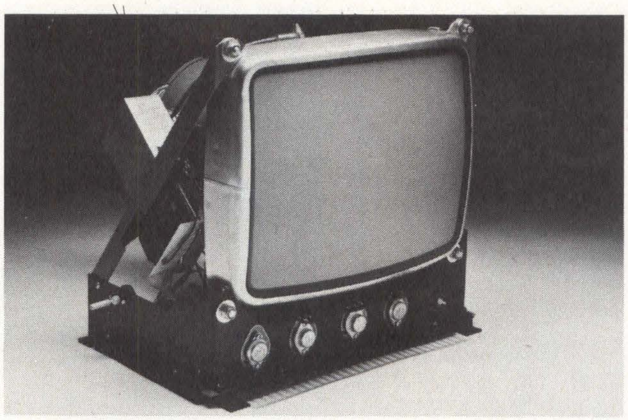

No Frills Color. Just the basics. If you're a black and white terminal manufacturer, the Intecolor 813 is all you need to upgrade your terminals to color.

It consists of an 8-color, 13" CRT, plus a special Analog Module System with all the circuitry necessary to perform deflection and video drive functions for the CRT. The completely self-contained circuitry is on a single printed wiring board which also generates the low voltage, high voltage and CRT bias, mounted on a sturdy aluminum frame for heat sinking the power transistors needed for the circuitry.

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PRODUCTS

INTELLIGENT PROGRAMMER FOR UV ERASABLE CMOS P/ROMs

Designed specifically for programming 6603 and 6604 devices, the 660 contains its own microprocessor and 4096-bit RAM buffer and can be operated standalone from its front panel or interactively with an ordinary CRT or TTY terminal through built-in RS-232 or 20-mA current loop interfaces. Programmer can communicate with computer and/or automatic IC test equipment for automated online P/ROM programming. Built-in features include editing capabilities for loading and checking the RAM buffer and/or 660X EPROM, ability to accept most paper tape formats, firmware for P/ROM copying and verifying, and a front panel erase-check capability. Programming time is typically half that required for similar n-channel device programmers. **Pacific Cyber/Metrix, Inc,** 3120 Crow Canyon Rd, San Ramon, CA 94583.

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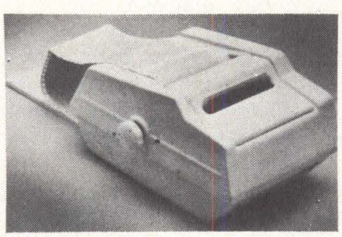
CASSETTE BASED PAPER TAPE EMULATOR

Model 6801 operates with either single or dual cassette transport and is directly compatible with conventional paper tape systems. Cassettes increase data transfer rates and provide reliable on- or offline data storage in a compact package. A self-contained power supply provides all internal power requirements from a single 115/230-Vac input power source. Data communication is achieved via a serial asynchronous interface, in accordance with EIA Std RS-232-C; speed is selected in 8 steps between 110 and 9600 baud. Manual controls and indicators enable user to select basic unit functions and operate the equipment. EPROM software provides flexibility to implement additional options. **Raymond Engineering Inc, Raycorder Products Div,** 217 Smith St, Middletown, CT 06457.

Circle 285 on Inquiry Card

40-COL LINE PRINTER

Kyodo model RO-101P, a 40-col drum type printer with microprocessor controlled electronics, incorporates paper sprocket-feed for vertical forms control, single board electronics with a choice of 5 interfaces, and MPU-controlled (TMS 9980) selection of top of form increments from 4 to 11" (10 to 28 cm), 8 baud rates, 5 to 8 data bits, stop bits, and parity with ACK and NACK signals. 8-bit parallel data (ASCII) is std interface; RS-232-C, 20-mA current loop, or IEEE-488B are optional. Modem interface is provided by use of TMS 9902 (asynchronous communication controller) and ICs are used for level conversion. Communication signals are converted from RS-232-C level to TTL level and written into RAM. **Computers International, Inc,** 3780 Wilshire Blvd, Los Angeles, CA 90010.



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LITERATURE

Liquid Crystal Displays

Brochure points out custom design and production capability of the company's watch and clock industry LCDs along with line of displays available for multiplexing applications. **Ladcor,** Mountain View, Calif.
Circle 300 on Inquiry Card

Image Processing

"Application Note Using the Comtal Series 200" gives insight into the use of digital exploitation systems with features such as interaction, roaming, overview, and freezing, as well as dynamic image presentation or displayed image readback. **Comtal Corp,** Pasadena, Calif.
Circle 301 on Inquiry Card

Electronic Components

Encompassing eight sections, 224-p catalog covers resistor networks, hybrid microcircuits, planar gas discharge displays, LCDs, trimming and precision potentiometers, and turns-counting dials. **Beckman Instruments, Inc,** Fullerton, Calif.
Circle 302 on Inquiry Card

Data Processing Software

With architectural, operational, and configuration diagrams, 16-p brochure discusses ITEMS™ transaction energy management system for distributed data processing. **Incoterm Corp,** Wellesley Hills, Mass.
Circle 303 on Inquiry Card

Voice Data Entry Terminals

Literature describes model 600 teletype compatible voice data entry terminal which enables individual at source level to communicate directly with a computer by voice and serves as a video or teleprinter terminal. **Threshold Technology Inc,** Delran, NJ.
Circle 304 on Inquiry Card

Computer Oriented Books

Containing over 1000 books from 207 publishers, *Annual Bibliography of Computer Oriented Books* lists books covering hardware design, data communications, computer applications, program design, and advanced programming. Price for bibliography is $4. **Computing Newsletter,** Box 7345, Colorado Springs, CO 80933.

Disc Packs/Cartridges

Brochure lists media characteristics and selection criteria for disc packs, cartridges, and diskettes. **Nashua Corp,** Nashua, NH.
Circle 305 on Inquiry Card

Signal Processing Applications Programming

Divided into four sections representing various levels of programming, illustrated booklet demonstrates programming of sophisticated applications when using the SPS-21 system. **Signal Processing Systems, Inc,** Waltham, Mass.
Circle 306 on Inquiry Card

Linear/Interface Circuits

BIFET and bipolar op amps, voltage regulators and comparators, line circuits, peripheral, MOS, memory and display drivers, and sense amps are covered in 128-p catalog with schematics and key features. **Texas Instruments Inc,** Dallas, Tex.
Circle 307 on Inquiry Card

Display Devices

Guide provides tabulated data, outline configurations, definitions, and phosphor screen characteristics for std line of display devices including instrument and information display CRTs. **RCA/Electro-Optics and Devices,** Somerville, NJ.
Circle 308 on Inquiry Card

Optical Fibers

Giving dimensions, transmission characteristics, coupling properties, and graphs, folder includes product summaries and covers lacquer-coated optical fibers which combine low attenuation and high bandwidth characteristics. **Telecommunication Products Dept, Corning Glass Works,** Corning, NY.
Circle 309 on Inquiry Card

Control Systems

"Computer Science & Technology: An Architecture for a Robot Hierachical Control System," a 227-p report, describes development, implementation, and control programs for computer based control systems for utilization of complex automation systems such as industrial robots. Price of report (SD No. 003-003-01874-1) is $4.25. **Superintendent of Documents, U.S. Government Printing Office,** Washington, DC 20402.

Submodular Power Supplies

Block diagrams, performance specs, outline drawings, and emi and holdover storage data comprise 12-p brochure on submodular series of 50- to 300-W single- and triple-output switching power supplies. **ACDC Electronics,** Oceanside, Calif.
Circle 310 on Inquiry Card

Test and Measuring Instruments

Catalog includes photos, descriptions, and technical specs for oscilloscopes, counters and counter/timers, pulse generators, recorders, multimeters and voltmeters, and signal generators. **Philips Test & Measuring Instruments, Inc,** Mahwah, NJ.
Circle 311 on Inquiry Card

μProcessor Fault Testing/Diagnosing

Paper discusses testing capability of signature analysis and in-circuit emulation in a single instrument as an effective technique for fault diagnosis in microprocessor based products. **Millennium Systems, Inc,** Cupertino, Calif.
Circle 312 on Inquiry Card

Debugging with Logic Analyzer

Problems encountered when using a logic analyzer to debug a microprocessor based process control system are presented in 4-p application note which also points out advantages of implementing microprocessor control. **Tektronix Inc,** Beaverton, Ore.
Circle 313 on Inquiry Card

CMOS Phase-Locked Loops

Describing high performance loops for small size and low cost applications, application note presents fundamentals and design considerations of phase-locked loops, particularly SCL 4046B and SCL 4446B. **Solid State Scientific Inc,** Montgomeryville, Pa.
Circle 314 on Inquiry Card

Solid-State Time Delays

Alternative techniques in solid-state time delay technology are presented in handbook illustrated with schematics, block diagrams, line drawings, tables, and curves. Free copy may be obtained for limited time by writing on company letterhead. **Amerace Corp, Control Products Div,** 2330 Vauxhall Rd, Union, NJ 07083.

Optoelectronics

Catalog includes data, photos, and dimensional diagrams of lamps, phototransistors, photodiodes, photovoltaic cells, optoisolators, and the 4-digit, 16-segment alphanumeric display, DL-1416. **Litronix, Inc,** Cupertino, Calif.
Circle 315 on Inquiry Card

Remote Access System

Spec sheet describes 6100 remote access system, which provides access and control of voice grade circuits for testing and trouble analysis from a centralized location. **ADC Telecommunications,** Minneapolis, Minn.
Circle 316 on Inquiry Card

Connectors

Describing rectangular, rack/panel, circular, microminiature, PC, I/O, and filters, connector selection guide also includes wire and contact requirements and environmental options. **ITT, Cannon Electric Div,** Santa Ana, Calif.
Circle 317 on Inquiry Card

16-Bit Computers

Brochure indicates advantages of 16-bit and limitations of 8-bit computers and introduces the H11 computer, a 10-bit machine that utilizes DEC's LSI-11 CPU. **Heath Co,** Dept 350-650, Benton Harbor, Mich.
Circle 318 on Inquiry Card

Data Communications

Catalog provides details and illustrates full line of modems from 300 to 19.2k bits/s, time and frequency division multiplexers, and data line concentrators. **General Data Comm Industries, Inc,** Danbury, Conn.
Circle 319 on Inquiry Card

Switching Power Supplies

Catalog lists complete specs on 94 std switching power supply models including DC-DC converters, multiple output supplies, PC board units, and modular supplies. **Etatech, Inc,** Placentia, Calif.
Circle 320 on Inquiry Card

Voice Couplers

One brochure includes table of equipment and diagrams of registered and grandfathered voice couplers; another lists specs, features, supporting equipment, and connector pin assignments of Pulsecom[R] 1695 high density single-frequency signaling systems. **Harvey Hubbell, Inc, Pulsecom Div,** Falls Church, Va.
Circle 321 on Inquiry Card

Synchro Converters/ Displays/Encoders

Catalog provides features, spec tables, applications information, and diagrams of multispeed D-S and S-D converters, and programmable solid-state limit switches, all having TTL compatible I/Os. **Computer Conversions Corp,** East Northport, NY.
Circle 322 on Inquiry Card

Memory Board Tester

Design and operation of MD-207 system for testing memory boards and systems are explained in brochure along with engineering and production applications and sequential photos. **Macrodata Corp,** Woodland Hills, Calif.
Circle 323 on Inquiry Card

Acoustic Couplers/Modems

Presenting data on proper compatibility, terminal interface, line coupling, data rate, and transmission modes of various types of modems, brochure also introduces cross references for communications needs. **Omnitec Data,** Phoenix, Ariz.
Circle 324 on Inquiry Card

Database Management Systems

Brochure on data base management system 2000 discusses its applications in production use and includes photos, block diagrams, operating environments, and features. **MRI Systems Corp,** Austin, Tex.
Circle 325 on Inquiry Card

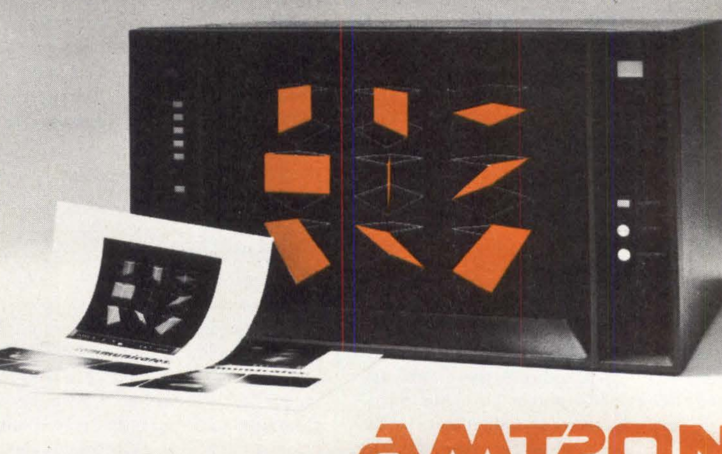
Measurement and Control Devices

Detailed spec tables make up 32-p short form guide on measurement and control products including converters, various amps, multiplexers, digital panel instruments, and power supplies. **Analog Devices,** Norwood, Mass.
Circle 326 on Inquiry Card

Thank you.

Thank you for your enthusiastic response to our DG-13 and DG-19 high-resolution color CRT monitors. While the '78 NCC was our first showing in the field of data graphics, we're no stranger to quality picture display — as anyone in broadcast television can attest.

At NCC, you confirmed the validity of the Amtron approach to design philosophy and manufacturing technology — and for that, we thank you.



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GUIDE TO PRODUCT INFORMATION

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GUIDE TO PRODUCT INFORMATION

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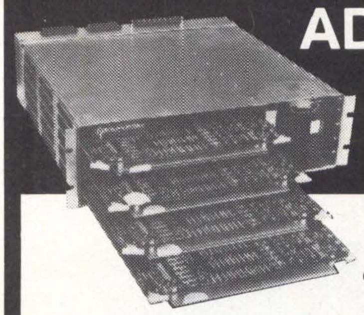
MEMORY ADD-ON SYSTEMS
ADD-IN BOARDS
MASS CORE



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Desktop combination reader/punch with serial asynchronous RS-232C compatible interface. Designed to operate with a terminal device on the same serial data lines or alone on a dedicated serial line. Reader will generate data at all standard baud rates up to 2400 baud.

Punch accepts data at all standard baud rates up to 600 baud continuous or 4800 baud batch, utilizing a 32 character buffer.

Two modes of operation are provided: *Auto Mode* — Simulates Model ASR 33 Teletype using ASCII defined data codes (DC 1, 2, 3 and 4) to activate/deactivate the reader or punch; *Manual Mode* — Code transparent mode. Panel switches control activation/deactivation of reader or punch and associated terminal device.

Tape duplication feature is provided by setting unit to LOCAL mode.

MODEL 1560-AS

High-speed, compact, with self-contained electronics and power supply. Complete in attractive noise dampening housing.

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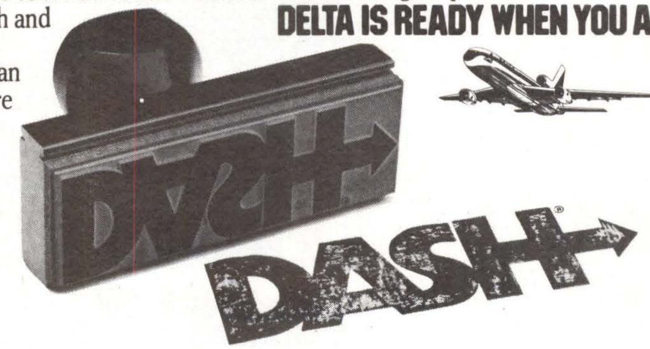

CIRCLE 109 ON INQUIRY CARD

ADVERTISERS' INDEX

*Appearing in selected geographic areas

Color quality and intelligence— two reasons our H-7000 looks like a winner

Specifications

COLOR MONITOR:
- 19 inch
- High resolution tube

CHARACTER/SYMBOL SET:
- 64 ASCII characters
- 64 programmable symbols (PROM)
- 256 dynamically writable symbols (RAM)

CHARACTER/SYMBOL CONTROL:
- 7 colors
- Blink
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- Double size character/symbol
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DUAL MEMORY FEATURE

BAR GRAPH DISPLAY

TREND GRAPH DISPLAY

DISPLAY EDITOR OPTIONS:
- Standard keyboard
- Function keyboard
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Versatile features include trend and bar graphing, superimposing of two pictures using dual refresh memory, two level intensity and other visual functions designed to present complex information in an easy to assimilate form.

Our patented "Dynamically Writable" Symbol Conversion Memory offers the process engineer the most flexible graphic character set in the industry and enables him to freely define symbols at any time.

To suit all customer requirements, we offer three basic models with 960, 1,920 or 4,032 characters/symbols per display.

Another unique feature of the H-7000 is a software tool called Display Generating Software (DGS). Using DGS, the process engineer can construct or modify a display picture by interactive English language "conversation" through the CRT terminal.

Take a look at the H-7000. You'll see it's a winner at a glance.

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...systems flexible enough to use in a wide variety of applications. Systems easy to build, easy to service. Systems in which every part—the microprocessor, every semiconductor, every connector, every miscellaneous component—is or soon will be a second-sourced industry standard.

Card	PLS 881	PLS 888	PLS 858	PLS 868	PLS 898
Processor	8080A	8080A	8085	6800	Z-80
PROM* Capacity	4K (2708)	8K (TMS2716)	8K (2716)	8K (2716)	8K (2716)
RAM** Capacity	1K	2K	2K	2K	2K
Input Ports (8 lines)	2	2	2	2	2
Output Ports (8 lines)	3	3	3	3	3
100 Piece Price	$165	$185	$185	$185	$185

*PROM not included. **1K of RAM included.

Pro-Log builds 8080A, 8085, Z-80, and 6800 microprocessors into one-card systems.

We use standard 4½-inch by 6½-inch 56-pin edge-connected cards. We've refined each system to fewer than 100 parts. To make sure our systems work when you get them, we test each system before and after power-on burn-in. We supply complete documentation with every card. Buy 250 of any one card and we give you free the plans for that card and non-exclusive manufacturing rights. You can build cards yourself and use us as a second-source. Need more capability later? Upgrade to one of our equally well-designed multiple card systems.

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