

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

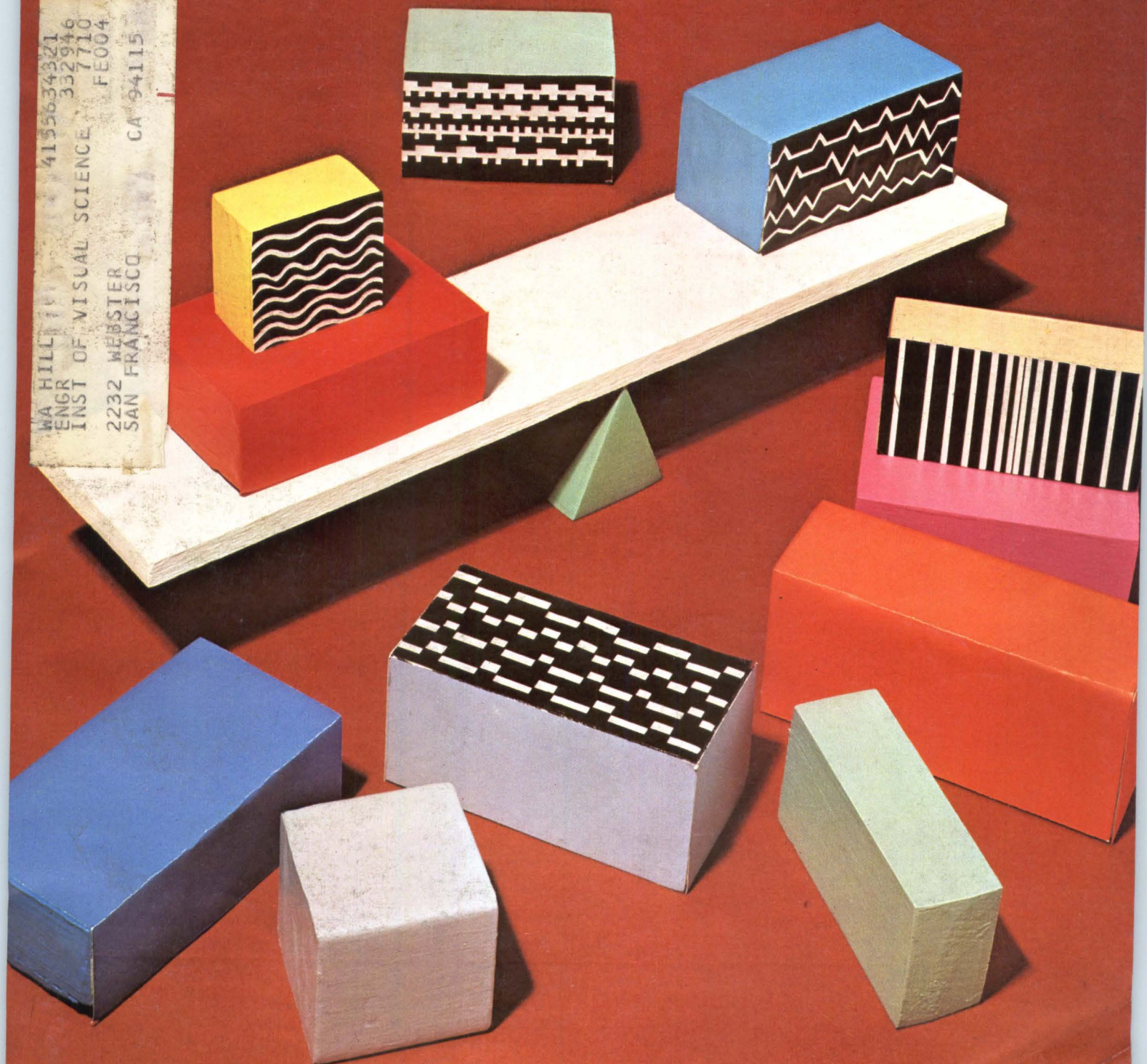
FEBRUARY 1979

COMPARING MICROCOMPUTER DEVELOPMENT SYSTEM CAPABILITIES

HARDWARE LINK DIRECTS MULTICOMPUTER INTERACTIONS IN PROCESS CONTROL

PARALLEL PROCESSOR ARCHITECTURES
PART 2: SPECIAL PURPOSE SYSTEMS

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THE MAGAZINE OF DIGITAL ELECTRONICS

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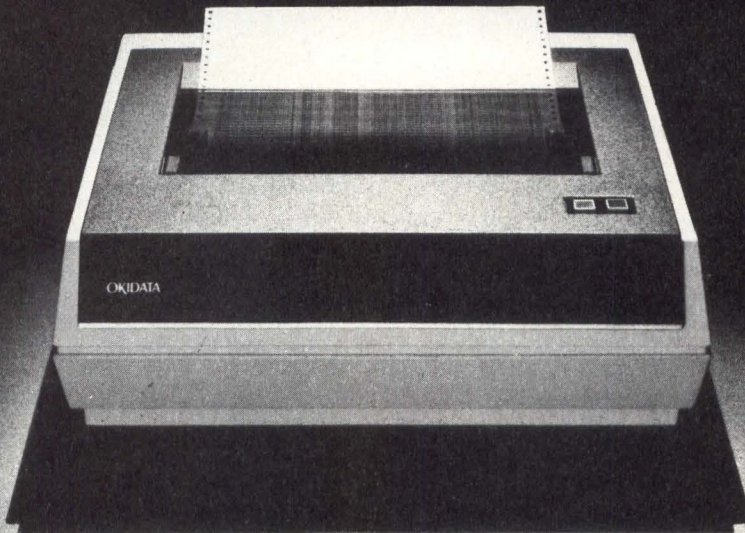
IECI '79 60

At this IEEE Industrial Electronic and Control Instrumentation Society Conference, speakers from worldwide will discuss diverse applications for microprocessors in control

INTELCOM 79 74

Examining technological developments, regulatory issues, and key aspects of communications, this year's conference consists of technical program sessions, executive forums, and a mini-university

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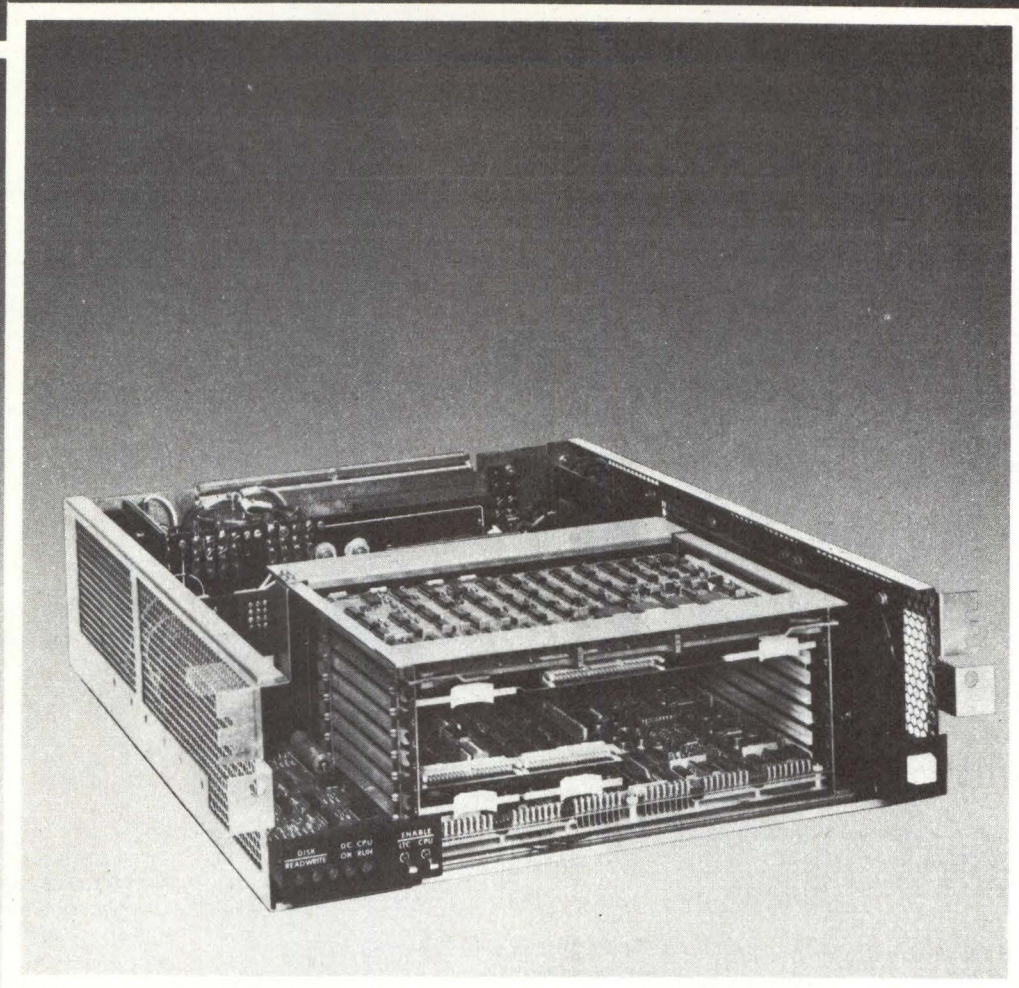
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CALENDAR

CONFERENCES

FEB 26-MAR 1—COMPCON Spring, San Francisco, Calif. INFORMATION: COMPCON Spring 79, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

FEB 26-MAR 2—INTELCOM, Dallas Convention Ctr, Dallas, Tex. INFORMATION: M. Raftery, Mgr of Promotion, Horizon House Internat'l, 610 Washington St, Dedham, MA 02026. Tel: (617) 326-8200

MAR 6-8—Optical Fiber Communication, Shoreham Americana Hotel, Washington, DC. INFORMATION: Optical Society of America, 2000 L St, NW, Suite 620, Washington, DC 20036. Tel: (202) 293-1420

MAR 11-15—Internat'l Conf on Magnetic Bubbles, Palm Springs, Calif. INFORMATION: Dr Paul J. Besser, Rockwell International, 3370 Miraloma Ave, PO Box 3105, Anaheim, CA 92803

MAR 14-16—Simulation Sym, Causeway Inn, Tampa, Fla. INFORMATION: Sudesh Kumar, NCR Corp, 4045 Sorrento Valley Blvd, San Diego, CA 92121

MAR 19-21—Federal DP Expo, Sheraton Park Hotel, Washington, DC. INFORMATION: Dick Rusch, Interface Show Group, 160 Speen St, Framingham, MA 01701. Tel: (617) 879-4502

MAR 19-21—IECI Conf and Exhibit on Industrial and Control Applications of Microprocessors, Philadelphia Sheraton, Philadelphia, Pa. INFORMATION: S. J. Vahaviolos, Physical Acoustics Corp, PO Box 3135, Princeton, NJ 08540. Tel: (609) 452-2511

MAR 25-28—Numerical and Control Society Annual Meeting and Technical Conf, Marriott Hotel, Los Angeles, Calif. INFORMATION: Elaine Skott, Numerical Control Society Headquarters, 1800 Pickwick Ave, Glenview, IL 60025

MAR 27-29—Trends in Online Computer Control Systems, University of Sheffield, U.K. INFORMATION: IEE Conference Dept, Savoy Pl, London WC2R 0BL, England

MAR 29, APR 17, and APR 19—Invitational Computer Conf, Dallas, Tex; Dayton, Ohio; and Chicago, Ill. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

APR 3-5—Very Large-Scale Integrated Circuits, Technologies, Systems, Applications, Baden-Baden, Federal Republic of Germany. INFORMATION: Dr Ing F. Coers, Stresemannallee 21, VDE-Haus, D-6000 Frankfurt 70, West Germany

APR 3-5—Specifications of Reliable Software Conf, Hyatt Regency Hotel, Cambridge, Mass. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

APR 9-12—INTERFACE, McCormick Pl, Chicago, Ill. INFORMATION: Sheldon G. Adelson, President, Datacomm Interface, Inc, 160 Speen St, Framingham, MA 01701. Tel: (617) 879-4502

APR 23-25—Relay Conf, Stillwater, Okla. INFORMATION: Engineering Extension, Oklahoma State U, Stillwater, OK 74074. Tel: (405) 624-5146

APR 23-25—Sym on Computer Architecture, Marriott Hotel, Philadelphia, Pa. INFORMATION: Dr Barry Borgerson, Sperry Univac, PO Box 500, Blue Bell, PA 19422. Tel: (215) 542-2013

APR 24-26—Electro, New York Coliseum and Americana Hotel, New York, NY. INFORMATION: William C. Weber, Jr, General Mgr, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

MAY 1-3—DATA Computer Show and Data Communications Conf, Toronto, Canada. INFORMATION: Kimberly Coffman, 2 Bloor St W, Suite 2504, Toronto, Ontario M4W 3E2, Canada

MAY 8-10—Society for Information Display Internat'l Sym, Chicago Marriott Hotel, Chicago, Ill. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: (305) 446-8193

MAY 17—Trends and Applications: Advances in Systems Technology Sym, National Bureau of Standards, Gaithersburg, MD. INFORMATION: Trends and Applications, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAY 18-20—Mid-Atlantic Personal and Business Computer Show, National Guard Armory, Washington, DC. INFORMATION: Mid-Atlantic Expositions, Inc, PO Box 3315, Annapolis, MD 21403. Tel: (301) 263-8044

MAY 21-23—European Hybrid Microelectronics Conf and Exhibition, Internat'l Congress Centre, Ghent, Belgium. INFORMATION: Prof R. Govaerts, Katholieke Universiteit Leuven, Afdeling E.S.A.T., Kardinaal Mercierlaan 94, B-3030 Heverlee, Belgium

MAY 21-24—Sym on Incremental Motion Control Systems and Devices, Ramada Inn, Urbana, Ill. INFORMATION: Dr B. C. Kuo, PO Box 2772, Sta A, Champaign, IL 61820. Tel: (217) 333-4341

JUNE 4-7—National Computer Conference, New York Coliseum, and Hilton and Americana Hotels, New York, NY. INFORMATION: Marjorie Greimel, American Federation of Information Processing Societies, 210 Summit Ave, Montvale, NJ 07645. Tel: (201) 391-9810

JUNE 5-8—Business Equipment and Systems Internat'l Marketing Event, Paris, France. INFORMATION: Peter Ryan, U.S. Dept of Commerce, Industry and Trade Administration, Washington, DC 20230. Tel: (202) 377-2849

JUNE 25-27—Design Automation Conf, Town and Country Hotel, San Diego, Calif. INFORMATION: Robert J. Smith, III, Electrical Engineering Dept, U of Texas, PO Box 7728, Austin, TX 78712. Tel: (512) 471-4540

SEMINARS

MAR 5-8—16-Bit Microcomputer Design and Mini/Microcomputer Comparison Sem, Ramada Inn, Woburn, Mass. INFORMATION: Prof Donald D. French, Institute for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: (617) 964-1412

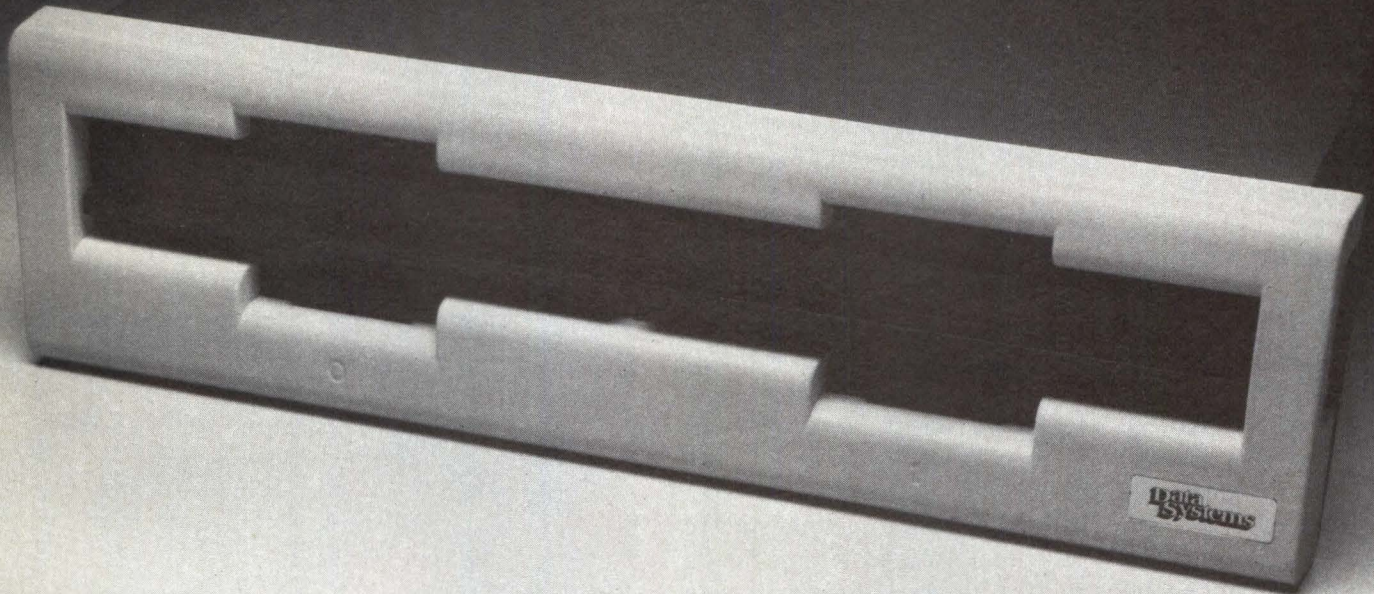
APR 5-6—Workshop on Computer Analysis of Time-Varying Imagery, Philadelphia, Pa. INFORMATION: Dr N. I. Badler, Computer and Information Science, Moore School of Electrical Engineering/D2, U of Pennsylvania, Philadelphia, PA 19104. Tel: (215) 243-5862

SHORT COURSES

MAR 22-24—Microprocessor Programming, Portland, Ore. INFORMATION: Vincent J. Giardina, IEEE Mgr of Continuing Education, 445 Hoes Ln, Piscataway, NJ 08854. Tel: (201) 981-0060, X174/175

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We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

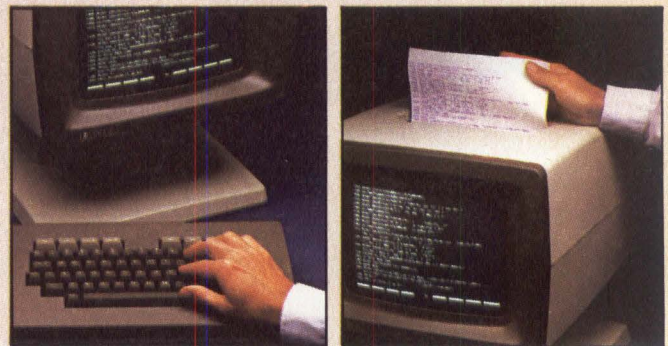
Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

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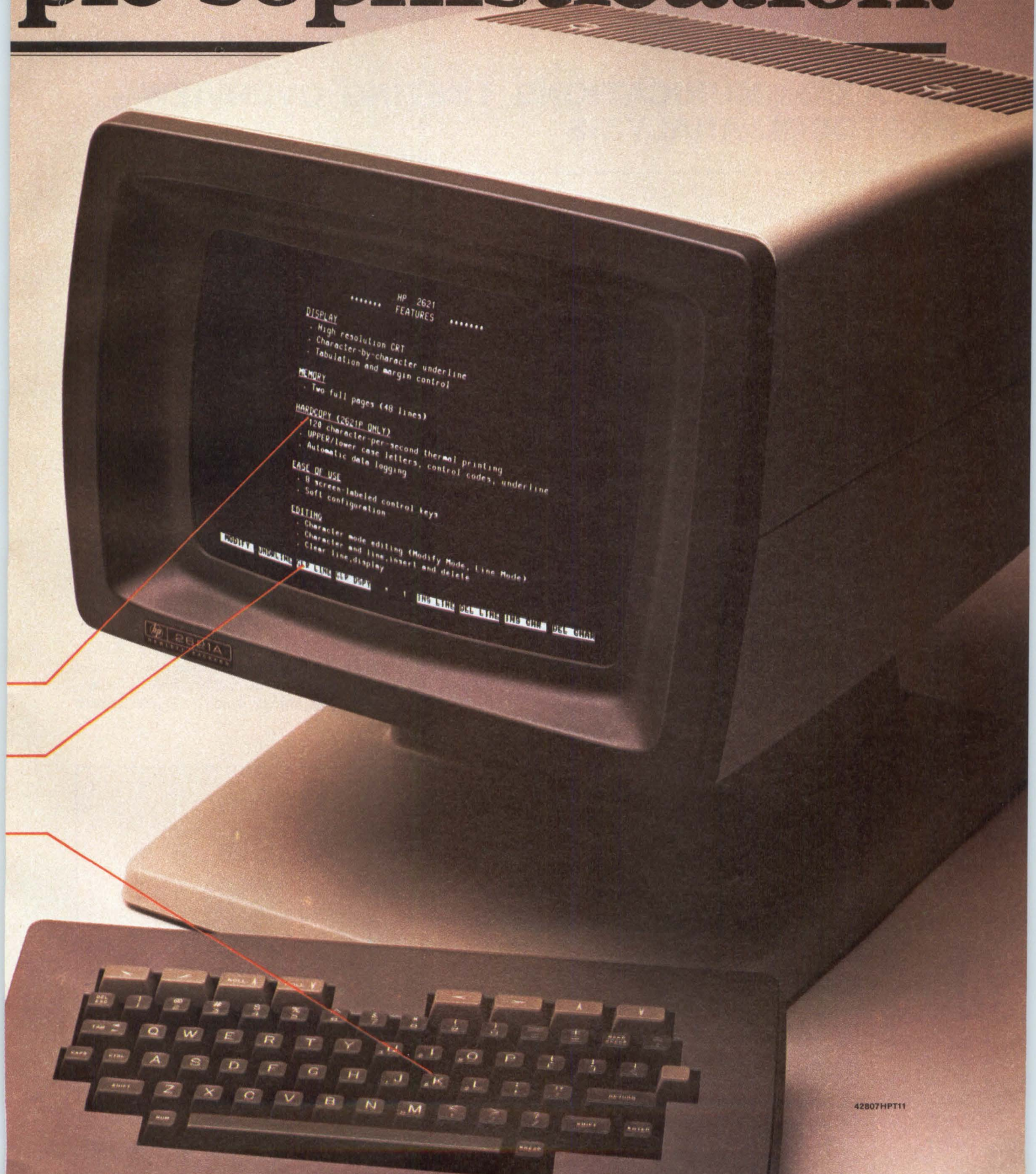
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DATA COMMUNICATIONS TESTING OVERVIEW— PROTOCOL ANALYSIS

Jeffrey R. Duerr

Hewlett-Packard Company, Delcon Division
Mountain View, California

The original concept of the computer as a basic calculator and number cruncher has undergone a profound change in the past two decades because of the development of vast data processing networks. As these computing systems have become more sophisticated, their ability to process and distribute data has been greatly extended by connection to remote terminals, and linkage to other geographically dispersed processing centers. A major factor in this dynamic growth has been the development of means by which these data centers can communicate through existing voice channels. The significance of this feat is even more impressive when one realizes the contrast in requirements between data and voice transmission.

The telephone system was designed for adequate communication from the human voice to the ear by relaying

a reproduction of a waveform in the normal voice band, 300 Hz to 4 kHz. Although signal-to-noise (s/N) ratios need be maintained at a reasonably high level, the ear, aided by its mental processor, is very forgiving of distortions in phase and frequency. For faithful data transmission, however, s/N ratios are less important; phase and frequency distortion, on the other hand, cause intersymbol interference and consequently higher error rates.

Data Communications System

A block diagram of a basic point-to-point data communications system is shown in Fig 1. Facility A communicates with facility B through an established voice channel supplied by one of the common carriers such as AT&T. Facility equipment may range from a simple remote

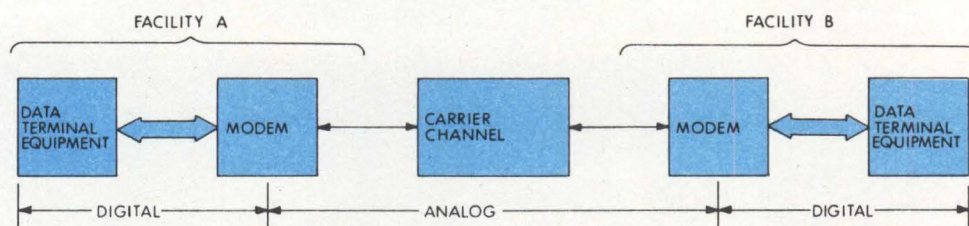


Fig 1 Simplified point-to-point system using common carrier channel. Since equipment and services are often from disparate sources, trouble spots are not easy to pinpoint

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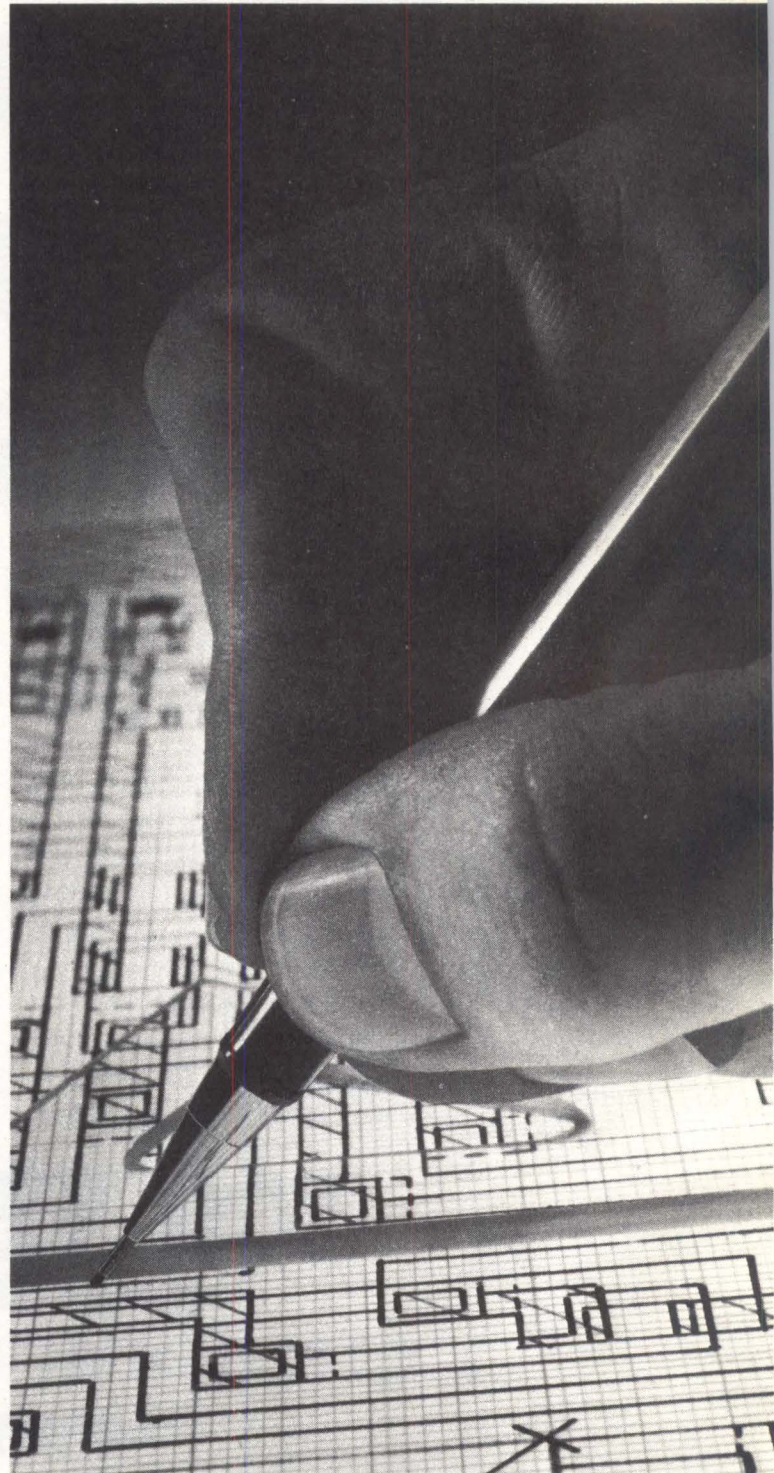
Still, the questions are asked. And, as the leader and chief innovator in this complex field, we'd like to answer them.

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to custom LSI is like nine months."

In a technology this complicated, all MOS companies sometimes run into design or production problems. But keep in mind that AMI has far more experience than anyone else. With more than 1200 different circuits under our belt, we know what will work and what won't. That's one reason we average less than seven months from firm specification to fully-tested LSI circuits—the fastest turnaround in the industry. As we work in 25 variations of four major processes, we don't have to bend your application to fit any production limitations. And we have plants in California, Idaho and Korea to build you all the product you need. (Some of our custom clients use more than a million circuits a year.)

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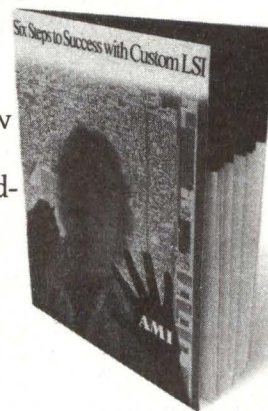
It also touches on some of AMI's applications' history, showing how far we've come in the past decade. We've made anti-skid and miles-to-empty circuits for the auto world. Sewing machine, kitchen range, washer/dryer and microwave oven controls for the appliance industry. Chips for phones, video games, televisions and electronic organs. And a broad spectrum of EDP applications, from keyboards and displays to memory management systems.

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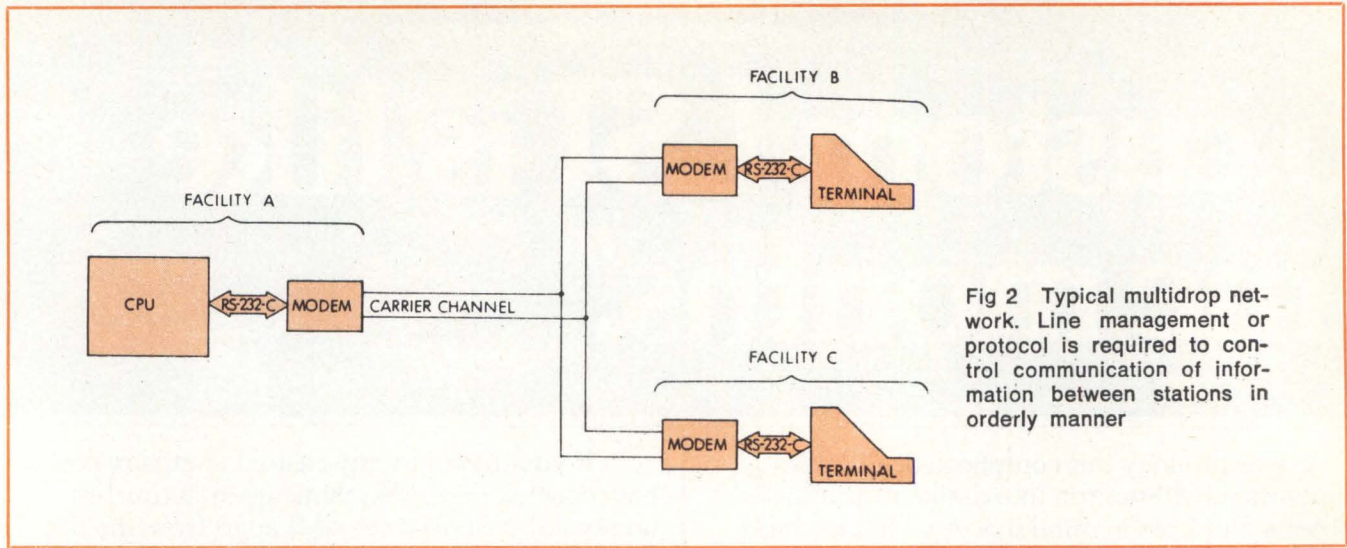


Fig 2 Typical multidrop network. Line management or protocol is required to control communication of information between stations in orderly manner

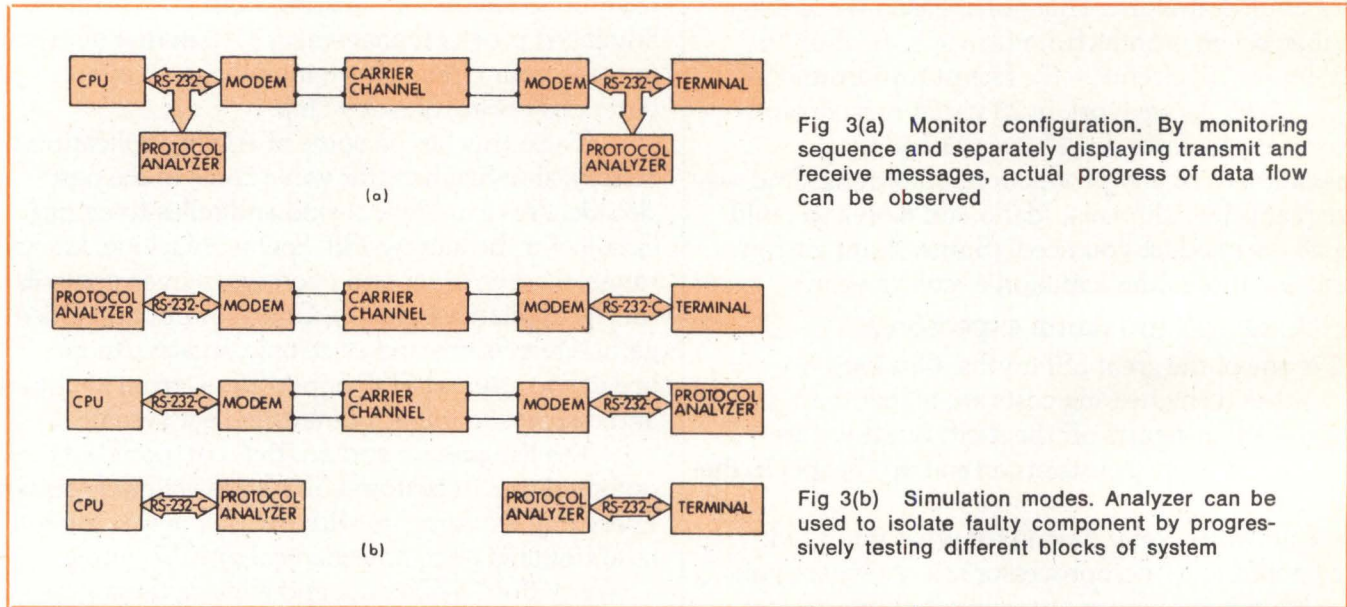


Fig 3(a) Monitor configuration. By monitoring sequence and separately displaying transmit and receive messages, actual progress of data flow can be observed

Fig 3(b) Simulation modes. Analyzer can be used to isolate faulty component by progressively testing different blocks of system

terminal-modem combination to a more complex configuration of processing equipment including CPU, several terminals, and a variety of peripherals. The classic dilemma faced by the communications manager at facility A is commonly referred to as the "finger-pointing" problem. He often has terminal equipment supplied by one manufacturer, modems by another, and a communication channel leased from the local telephone company. If he lacks adequate technical expertise in each of these three areas, it will sometimes be difficult to pin down the actual source of the trouble when a problem arises.

Tools to resolve this situation do exist, and are typically applied at three different levels: (1) protocol testing, (2) digital data testing, and (3) analog channel testing. Because each of these levels represents a unique measurement set, they will be discussed as separate elements in the overall measurement solution.

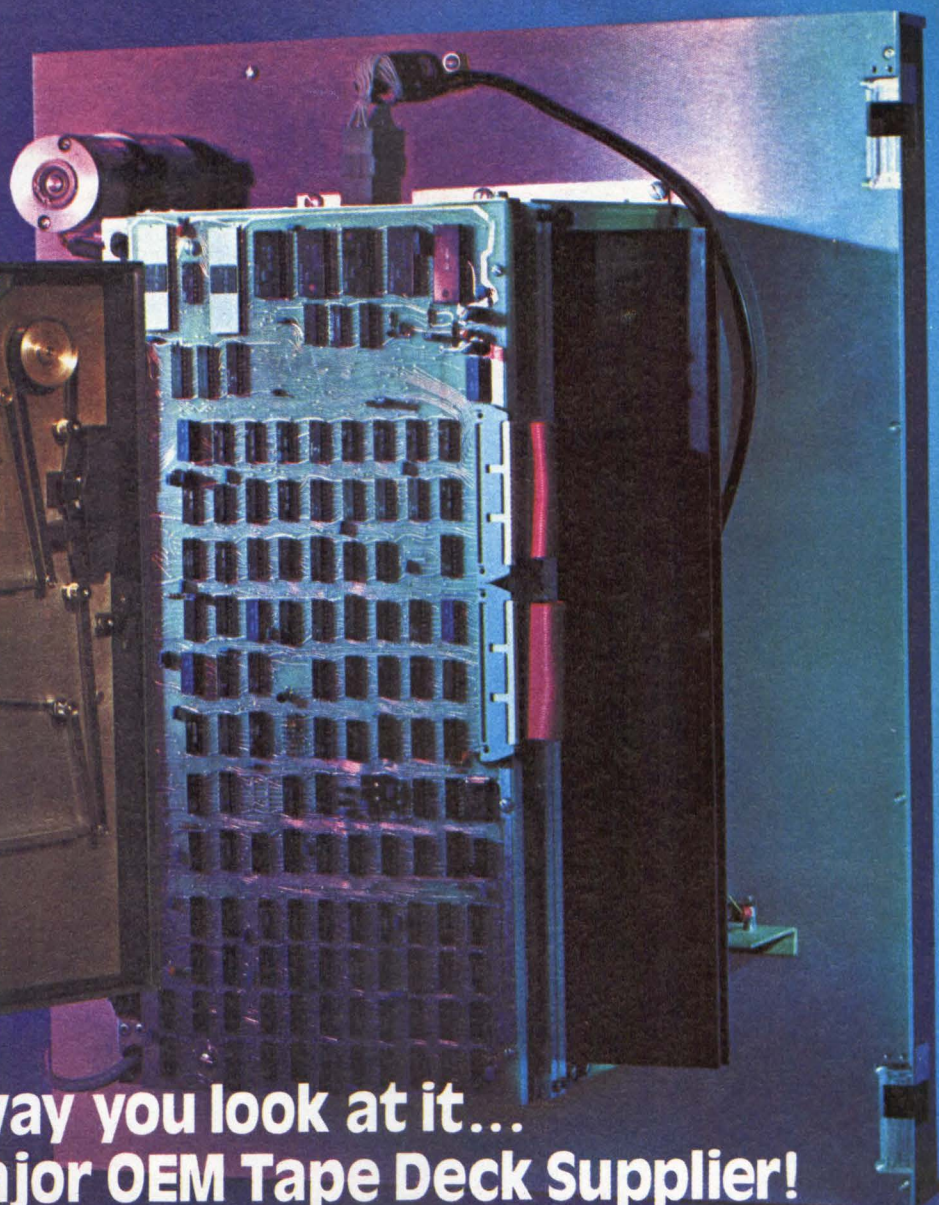
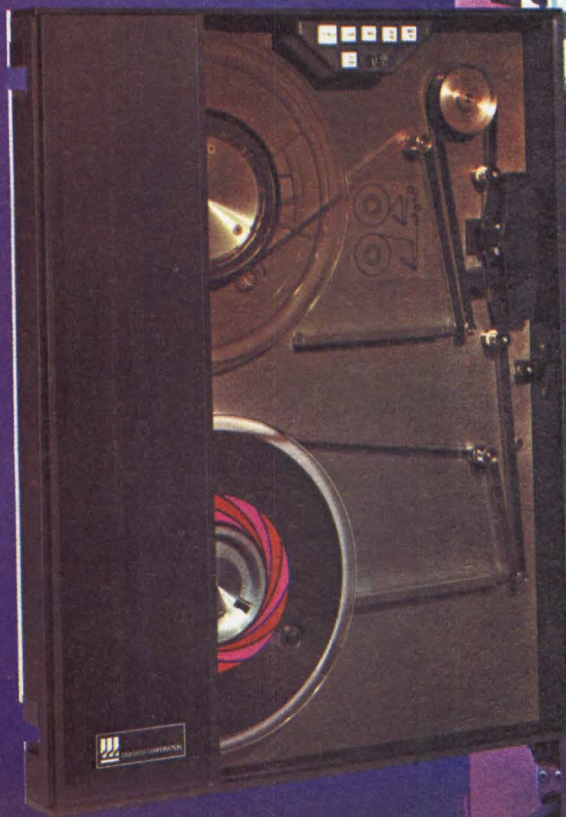
Protocol Testing

A distributed network (Fig 2) has special requirements for data flow management along the communication paths.

Because communication can extend from a simple point-to-point path to several points on a multipoint network, a need arose for this type of management, or line protocol. This provides the grammar by which machines can converse with each other in an orderly and controlled manner.

Binary synchronous communications (BSC), first introduced in 1966, became the industry standard for medium and high speed data communications. As new digital networks, satellite communications, and other advanced transmission techniques came on the scene, they created a need for a full duplex line protocol that was more efficient than BSC. This need is being met by newer standards, such as high level data link control (HDLC). HDLC allows a greater volume of information to be transmitted in a given time period, effectively reducing cost per unit volume of data transmission. In addition to transmission of standard text, other functions performed by protocol include acknowledgment or rejection of the text, detection of errors, retransmission after error detection, and other polling and command sequences.

In order to properly test communications operation at this level, a different type of test equipment is required.



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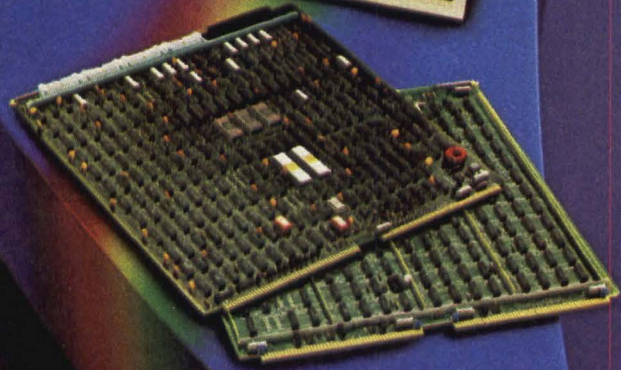
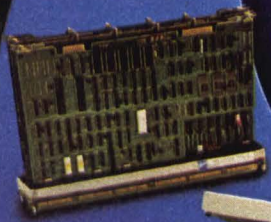


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Protocol testers developed for this purpose can interact with the communications system under test through a system language level, and can function in two modes, monitor and simulate.

Monitor mode is a passive, non-intrusive function for evaluating status and recording data information at the terminal-modem interface. This capability makes it possible to locate common network problems without costly interruption of the data communication channel. The fact that approximately 80% of system problems can be diagnosed by protocol analysis in monitor mode while the data link being checked remains in service is one of the more valuable features of this test method. In monitor mode, the analyzer should have the capability of triggering (trapping) on specific sequences and commands. This allows pinpointing of common network faults while passively monitoring data and handshake leads at the digital interface. The monitor configuration is shown in Fig 3(a), where a protocol analyzer is observing the CPU-modem interface at each end of a communication path.

Simulation modes for a protocol analyzer are shown in Fig 3(b). The analyzer can simulate a CPU to the modem, generate a message for the distant CPU, and interact with CPU or terminal.

Typical Problem and Solution

Assume that the CPU in the simple multidrop network of Fig 2 polls terminals B and C in an alternating sequence.

A typical symptom of a problem might be that the terminal at facility B does not respond to a poll request. By using protocol analysis at the terminal-modem interface at point B, it is possible to determine whether or not B is actually receiving the polling request. A non-intrusive monitor mode, triggering on the polling sequence for C, accomplishes this. Since C does respond, this trigger will produce a display where any follow-on sequence which was intended to poll terminal B can be observed. If there is a proper polling sequence to B, the response of B to that poll request can be observed.

If the response from B is correct, two other areas need examination. First of these is the handshake signal timing between terminal and modem at B. Control signals at the interface between modem and terminal must occur at prescribed intervals and for prescribed periods of time. Using the analyzer, the elapsed time for data terminal turnaround, time between request to send and clear to send signals, and other timing functions of the interface can be determined.

Second, assuming that these timing signals are within specification, point A should be investigated for proper response to the poll command at the modem-terminal interface. Choosing the appropriate trigger point allows the operator to observe the returned sequence from terminal B. An improper sequence indicates modem and line problems. A correct sequence implies that data input to the CPU is not accepted properly, a CPU problem. As before, further investigation could reveal discrepancies in the timing interchanges between modem and terminal or CPU.

When the problem has been isolated to a system component, the analyzer can be directly connected to either CPU or terminal and simulate one or the other. In this way the required protocol message can be generated and the response observed. In addition to diagnosing the overall protocol format, the analyzer should be able to make basic character parity error checks in the data message, giving a further dimension to testing the CPU-terminal network.

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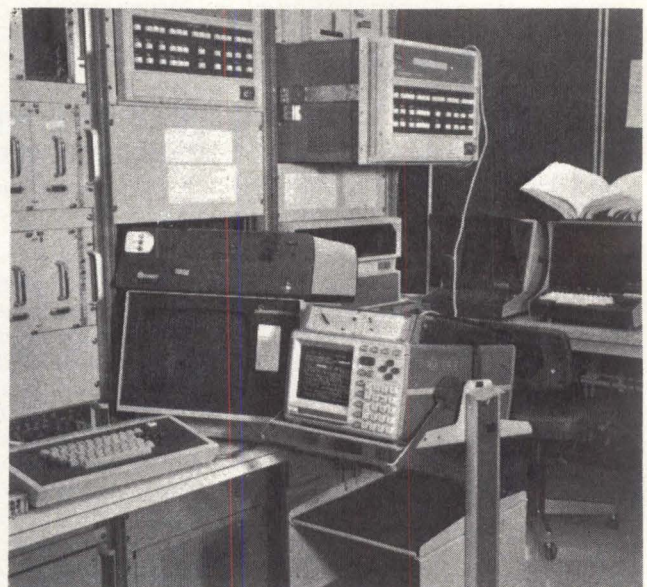


Fig 4 Typical test setup for protocol analysis. Here instrument (HP1640A) is monitoring interchange between terminal and minicomputer

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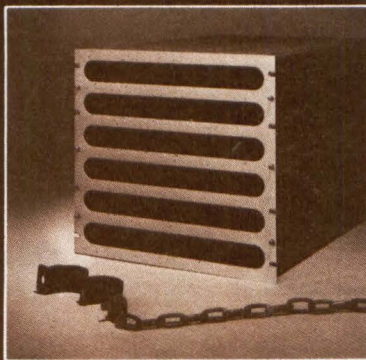
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Fig 4 shows a protocol analyzer in a typical test configuration.

Display output for a synchronous test is shown in Fig 5. Transmission of the standard "Fox" message is followed by an end of text (Ex) character and an idle. The received response includes two sync characters (Sy), an acknowledgement of proper receipt (Ak), and an idle.

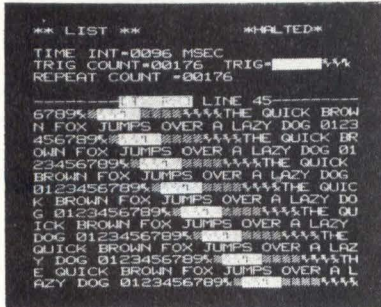


Fig 5 Display output for synchronous test. Display has been initiated well into message flow and shows transmit (normal video) and receive (reverse video) sequences

In addition, information on message time interval, trigger sequence, and number of repeats is available in the header.

Protocol Analyzer Selection Criteria

Ease of use is one of the most important parameters to be considered in choosing a protocol analyzer. Because the instrument must interact on a high level with a sophisticated network, the operator should not be bogged down with complexities in its operation.

Another important feature is the ability of the instrument to recognize and trigger on specific sequences. This is the real key to indexing into problem areas that may be experienced in the network.

There should be sufficient memory with enough characters to display problem symptoms on the network. Actual amount of memory required is lessened by increased capability of the analyzer to do more sophisticated triggering.

The ability to monitor the modem-terminal interface not only for data but also for timing functions is very important. Approximately 80% of system problems can be solved by non-intrusive monitoring. This saves network operating time, as well as resulting in considerable cost savings.

Simulation of either CPU or terminal is another important asset in detailed troubleshooting of specific blocks of the entire network.

The analyzer should be adaptable to a number of code sets, at least two or three, and preferably five or six, depending on the type of network. The most common of these codes are ASCII, EBCDIC, and hexadecimal.

Finally, capability of making basic parity error checks, or more elaborate longitudinal redundancy checks (LRC) and cyclic redundancy checks (CRC) on received messages will add to the overall utility of the analyzer.

Protocol analysis represents the highest level of a complete data communications test procedure. While digital and analog testing, to be covered in ensuing columns of this series, appeal to the hardware test engineer, it is protocol analysis that is the equivalent for the software troubleshooter.

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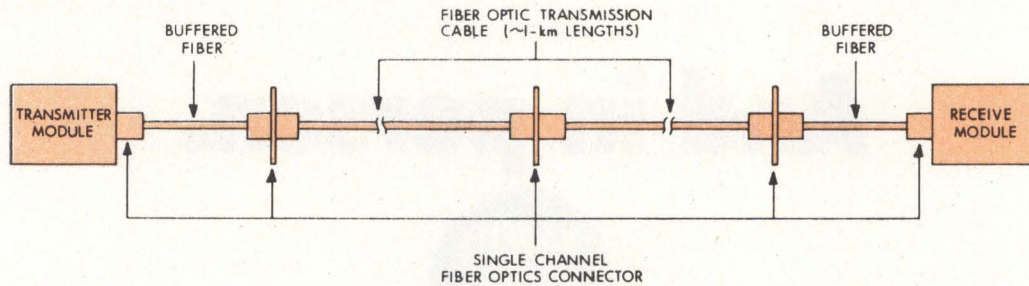
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Transmission system configuration. Two 1.07-km cables are coupled at midpoint by connector arrays. 1-m buffered fibers at the transmitter and receiver ends serve as patch cords to couple optical energy to and from cable ends

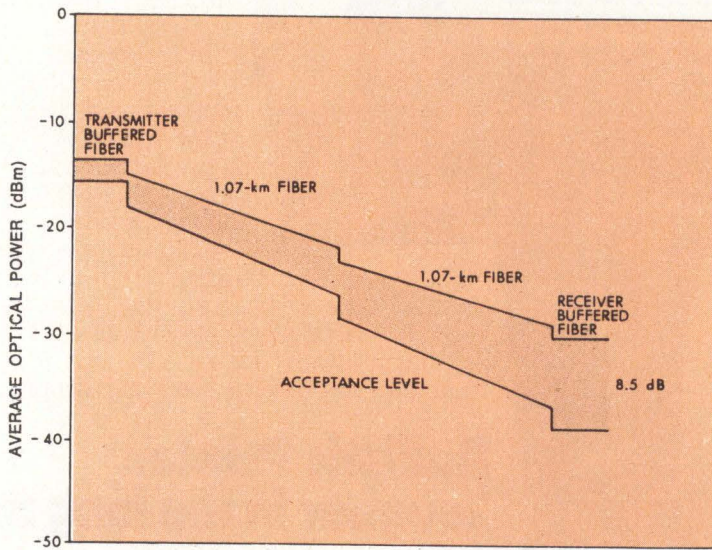
A fully operational fiber optic data transmission system has been installed by the U. S. Navy for use in the Defense Satellite Communications Sys-

tem (DSCS) at the Naval Communications Station in Agana, Guam. Hardware and installation assistance was provided by IRT Electro-Optical Pro-

ducts Div, 7635 Plantation Rd, Roanoke, VA 24019.

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Data channel power budget. Lower line shows acceptance level. Upper line, plotted from actual data link used in configuration audit, shows 8.5-dB optical power margin above acceptance level

References

1. *Computer Design*, Aug 1978, pp 18, 20
2. G. C. Wilhelmi, T. A. Eppes and J. R. Campbell, "An Operational Thirty-Channel Fiber Optic Data Transmission System in the DSCS Network," *ICC'78 Conference Record*, Vol I, pp 6.2.1-6.2.5

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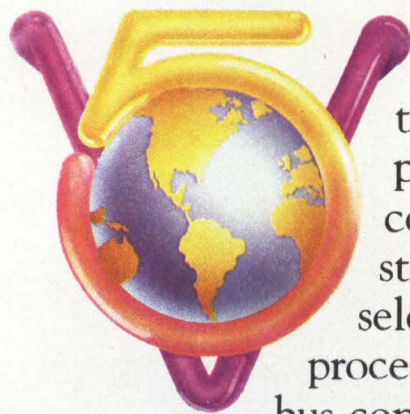
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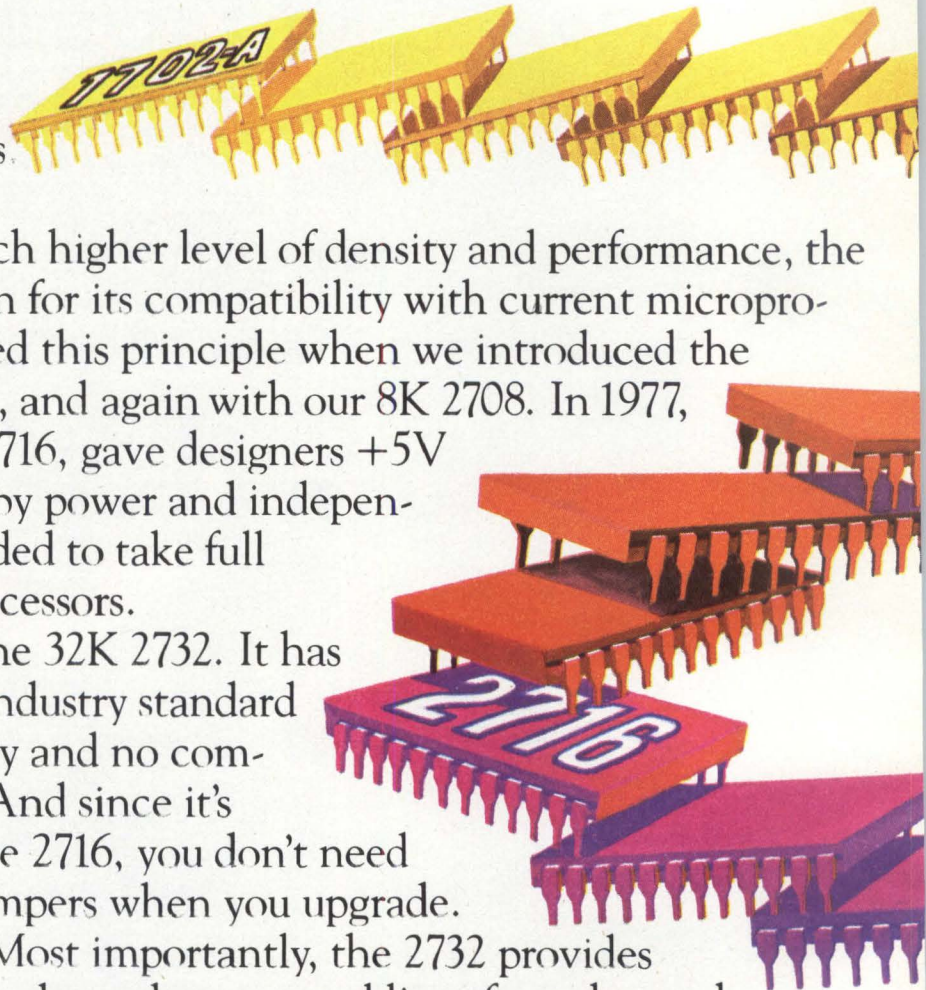
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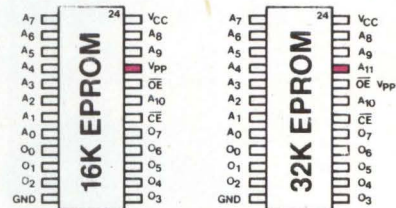


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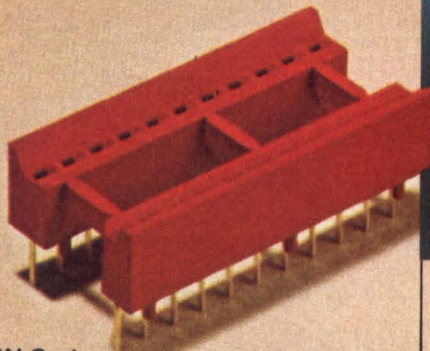
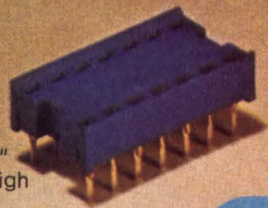
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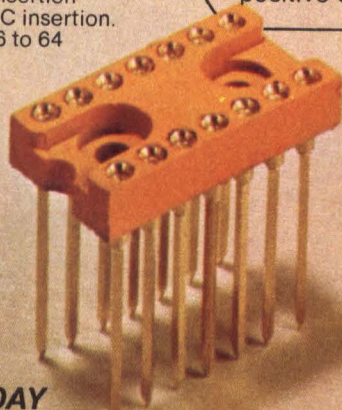
26% lower profile— .150" Ideal for high density, high volume configurations, provides maximum vibration resistance. Solder type, single leaf “side-wipe” contacts. 8 to 40 contacts.



ICN Series high reliability general-purpose sockets. Low insertion force allows automatic IC insertion. In solder or wire-wrap. 6 to 64 contacts. Dual leaf “side-wipe” contacts.

ICA Series

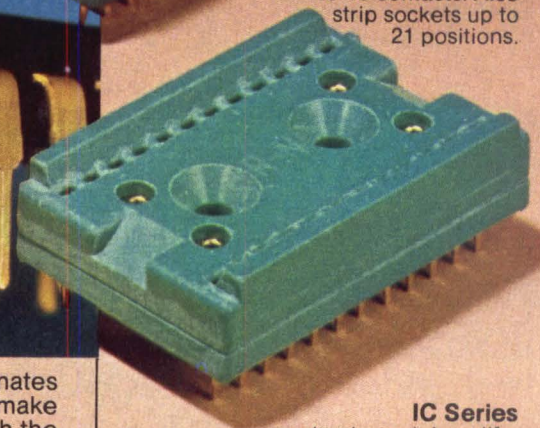
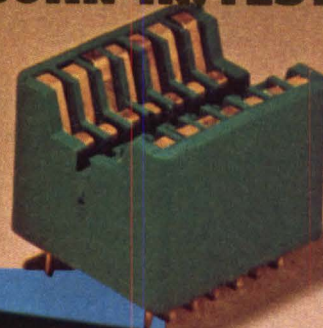
high reliability pin socket contacts. Low profile in solder or wire-wrap. 8 to 40 contacts.



BURN-IN, TEST SOCKETS

TS Series

very long contact life. Very low insertion force. Ideal for incoming inspection. With 14 to 40 contacts. Also strip sockets up to 21 positions.

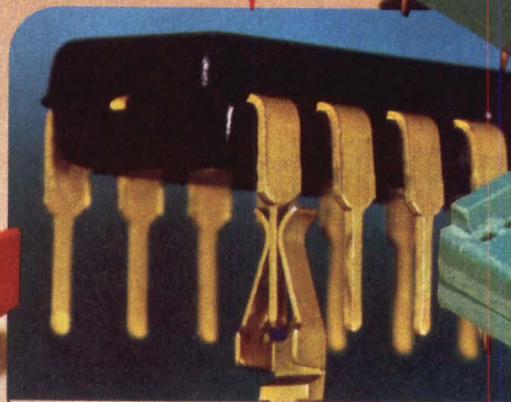
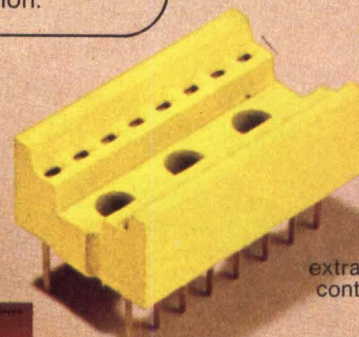


IC Series

moderate cost, long life. Designed for general test and burn-in up to 350°C. With 14 to 40 contacts.

ICN/S2 Series

lowest cost burn-in socket available. Designed to accept IC extraction tool. With 8 to 40 contacts, with strip sockets up to 25 positions.



RN HIGH RELIABILITY eliminates trouble. “Side-wipe” contacts make 100% greater surface contact with the wide, flat sides of your IC leads for positive electrical connection.

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CIRCLE 18 ON INQUIRY CARD

Interface Improves Printer System Capabilities

Full duplex serial data communications interface DAC-11/SDI for medium to high speed line printer subsystems is designed especially for asynchronous and bisynchronous data communications systems. The microprocessor-based unit has a minimum 1k resident memory, and is compatible with the DEC DL-11 and DH-11 single/multiple line asynchronous interfaces, as well as other minicomputer serial controllers, multiplexers, and intelligent terminals. Current loop and EIA RS-232-C versions are available. The interface is furnished by Digital Associates Corp, 1039 E Main St, Stamford, CT 06902.

The device is designed to operate under all popular communication protocols. A self-test feature with local loopback simplifies pinpointing trouble spots. Unit is available self-contained, including power supply, for use with existing printers, or in a single-board version integrated into a new data communications printer. Circle 400 on Inquiry Card

System Option Tests IPARS/PARS Protocol

A special option for INTERSHAKE[®] data communications diagnostic test system is designed for testing the IBM IPARS/PARS (international programmed airlines reservation system) protocol. IPARS/PARS is common to most such systems, but there are minor variations within each. Atlantic Research Corp, 5390 Cherokee Ave, Alexandria, VA 22314, says that the Intershake system is the only commercially available interactive tester programmed to handle these variations. Compatible with virtually any terminal type used in the network,



the unit can be connected as an on-line passive monitor without disturbing the system. Basic programmability enables network monitoring, or selective emulation of either CPU or terminal.

Unit can be programmed in IPARS language or IPARS HEX, rather than reverse line HEX, using the system's keyboard and program development editor. Data and/or control characters are displayed on a 9" (23-cm) 1024-char CRT in either normal language, IPARS HEX, or reverse line HEX. Unit incorporates 62-char quick brown fox message, plus line control and SMI (state of manual input) characters. In addition to IPARS the system will also handle as standard ASCII, EBCDIC, EBCD, Selectric, and BAUDOT codes at rates from 45 to 256k bits/s. It also accommodates as standard BSC, SDLC, and DDCMP protocols. Optional data recorder can selectively record 500k chars for later analysis.

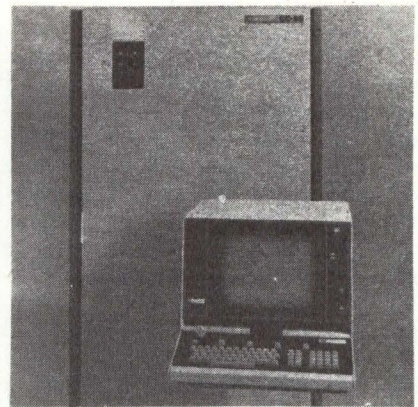
Among the system's capabilities in the IPARS/PARS environment are measurement of error rate/throughput using live CRC (cyclic redundancy check), and measurement and display of system response time with thresholds for alarm conditions.

Circle 401 on Inquiry Card

Communications Processor Provides High Throughput

cc-85, with microcontrol architecture and an instruction lookahead cache memory, has an internal cycle time of less than 90 ns for the highest throughput available, according to Computer Communications, Inc, 2610 Columbia St, Torrance, CA 90503. The processor can be used with all models of Systems 360/370/303X and compatible mainframes, and provides complex communications network processing with over 400k-char/s capability, approaching 1M char/s at peak load times.

A microprocessor-controlled CRT console can be used in system supervisor, system monitor, or engineering console modes. System supervisor mode allows dynamic system reconfiguration and control including real-time assignment of lines and terminals. System monitor provides individual line trace and 4-color readout of system line status, alarms, and statistics. Engineering mode permits di-



agnostics, information displays, and performance analysis via a direct port into the CPU. The cc-85 emulates an IBM 270X protocol and can also be used as a front-end processor or message switcher.

Other features include automatic rate detection, automatic polling on multipoint lines, disc-based operations, memory expandable to 512k bytes, direct memory access for BSC and SDLC, 8 groups of 16 registers, and 32 hardware interrupt levels.

Circle 402 on Inquiry Card

Architecture Supports Minicomputer Series in Distributed DP Systems

DCA (distributed communications architecture) is now supported on V77-600 and V77-800* minicomputers in distributed data processing systems, according to Sperry Univac, P. O. Box 500, Blue Bell, PA 19422. The system provides an interface to an advanced DCA network which uses DCP communications processors.

Available to the user at an application level is PRONTO, a transaction processing module which enables all necessary queuing, buffering, screen management, and control for UNISCOPE, TTY, or IBM 3270-type terminals. Programs written to interface with PRONTO can be developed in COBOL, FORTRAN IV, or macroassembler and can access either sequential, indexed, or TOTAL files.

DCA-compatible RBT/RJE supports the V77 as a remote batch/remote job entry station. Paper peripherals are supported with standard print,

*See Digital Technology Review, p 34.

punch, and card read capabilities. GRAM, (global resource access module) provides a basic level access method with interface routines such as OPEN, CLOSE, GET, and PUT. The user may choose to employ his own self contained application interfacing to network resources via the capabilities of GRAM.

Application management service modules manage local network resources such as lines and terminals, provide network console support, and allow error logging/recovery and other features. Termination system and sub-architectural interface modules pass data between application level subsystems and the communications data link. Functions performed

include message segmentation, sequencing and acknowledgement, pacing, port presentation services, and UDLC data link control.

A device attach facility supplies one or more terminal access modules (TAM) and associated line protocol handlers, and supports UNISCOPE 100-compatible terminals. By including 3270 master and slave handlers, a multi-vendor network may be accommodated in which 3270 terminals are linked to an IBM host, while U100-compatible terminals are connected to a Sperry Univac host. Application programs can be written to allow host systems to communicate with non-native terminals.

Circle 403 on Inquiry Card

Digital Facsimile Service Inaugurated Between U. S. and Switzerland

The first commercial digital facsimile service between the U.S. and Europe has been introduced by RCA Global Communications, Inc (RCA Globcom), 60 Broad St, New York, NY 10004, and Radio-Suisse Ltd, Berne, Switzerland. Users of the service, called Q-Fax, may send and receive messages, documents, graphics, engineering drawings, and other forms between the two countries in less than a minute. Cost of sending a standard 8.5" x 11" (22 x 28-cm) document to Switzerland is \$7.

Q-Fax service was introduced in Mar 1978 between RCA Globcom and Kokusai Denshin Denwa (KDD) Ltd international communications center in Tokyo. Subsequently the service

was extended to Hong Kong and Manila. Cost of sending a standard size document to the Far East is \$10. The service operates at 2400, 4800, or 9600 bits/s.

In the U. S., customers of Southern Pacific Communications' Speedfax service or of other specialized common carriers interconnecting with the Q-Fax network may use the same procedures for Switzerland as they use to send or receive documents to or from other Q-Fax locations.

Guide Provides Data for Interstate Network Planners

Rate digests, planning suggestions, and a telecommunications reference

manual are available in a one-volume guide prepared for those involved in the planning and maintenance of large or small interstate data communications networks. The 350+ page loose-leaf "Executive Telecommunications Planning Guide" is published by Center for Communications Management, Box 324, Ramsey, NJ 07446. Annual subscription price of \$250 (\$295 overseas) includes monthly update service.

The volume presents a digest of rates and descriptions of all services from AT&T Long Lines, Western Union, the specialized common carriers, international record carriers, and value-added networks.

Also provided are charts and tables showing patterns of average load and call distribution, Erlang and Poisson theories of trunk capacity, interface and interconnect standards for voice and data systems, including modem circuits and pin assignments, and other data of interest to network planners and designers.

Among entries in the reference section are listings of all U. S. rate centers, mileages between major metropolitan areas, and names, addresses, and telephone numbers of the common carriers. A tariff directory, glossary of telecommunications terms, and a pending section which presents filed but not yet effective tariff revisions are also included.

Circle 404 on Inquiry Card

International Electronic Message Service Set for Demonstration

A demonstration of INTELPOST (international electronic post) service is scheduled for early this year. The system will ultimately provide for high speed transmission and reception of facsimile copies of original letters, documents, and other data. Channels will be established to transmit data via satellites between the U. S. and Argentina, Belgium, Federal Republic of Germany, France, Iran, The Netherlands, and the U. K.

INTELPOST is an operation of the U. S. Postal Service. Installation and initial maintenance of the communication circuits will be performed by ITT World Communications Inc, 67 Broad St, New York, NY 10004. Data rates on the circuits will vary from 9.6k to 50k bits/s. Dedicated circuits provided by ITT Worldcom will be used to reach the satellite, while high speed digital facsimile equipment will perform the scanning and printing. □

All's well that ends well.

See page 81

How can a company that makes so many interfaces, and delivers them so fast, make them so good?



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The finest components. Hand assembled. Each skilled MDB craftsperson working alone to produce a product and submit it for testing. *That's* what makes MDB computer interfaces the best available, bar none.

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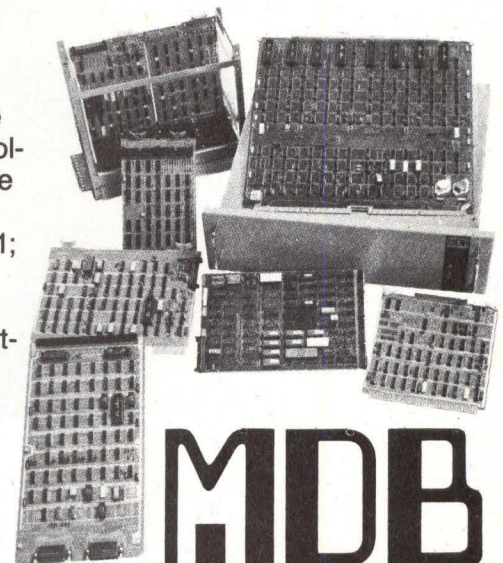
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Included in our line are line printer and card reader controllers and other plug-compatible modules for most computers including DEC PDP-11, LSI-11; and PDP-8; IBM Series/1; Data General Nova and Eclipse; Interdata and Hewlett-Packard computers. All MDB products are software compatible or transparent. No special diagnostic or operating software is needed.

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Computer Models Designed to Improve Performance, Function, and Economy

Additions to the Nova computer family—models 4/C, 4/S, and 4/X—provide performance, function, and price improvements over other members of the family. In the 4/C designers at Data General Corp, Rt 9, Westboro, MA 01581 have put the speed of a Nova 3 on a single board; the 2-board 4/S and 4/X feature 50% higher speed than the Nova 3. All models were designed to provide a broad set of reliability, self-diagnostic and maintainability features, allowing units to indicate when and where a problem develops to simplify maintenance.

The CPU board in all three contains an asynchronous terminal interface, automatic program load, power fail/auto restart, virtual console, and optional hardware multiply/divide. The microprogrammed bit-slice processor incorporates architectural features of 3 series units, including hardware stack and frame pointer, high speed direct memory access (DMA) channel, and 16-level priority interrupt structure.

Processor architecture provides four accumulators, stack capabilities, and Nova instruction set, extended with

byte manipulation instructions for commercial and communications applications, and optional signed multiply/divide for increased computational efficiency. Horizontally micro-coded CPU implementation allows extensive overlap of operations. In the /S and /X an instruction prefetch processor increases performance by looking ahead of currently executing instructions to store further instructions in a high speed FIFO, thus eliminating the fetch cycle in many cases.

Processors are formed using 2901A-type bit-slice elements. The /C uses a 48-bit long microword while /S and /X units use a 56-bit microword, devoting the extra eight bits to control of the prefetch processor. This processor, implemented with a FIFO stack, stores 13 instructions. For efficient operation, the stack reload instruction is incorporated in the CPU's JMP instruction, assuring that instructions are loaded in execution sequence.

Accelerated with 4-way interleaving, the 400-ns memories allow the prefetch processor to load instructions at 20M bytes/s, and reduce memory

conflict on memory modification instructions. The result is typical instruction execution times such as 400 ns for a store and 200 ns for an add. Memory boards are available in 32k- and 64k-byte increments for the 4/S, and 32k-, 64k-, 128k-, and 256k-byte increments for the 4/X. The 4/C carries 16k, 32k, or 64k bytes on the CPU board.

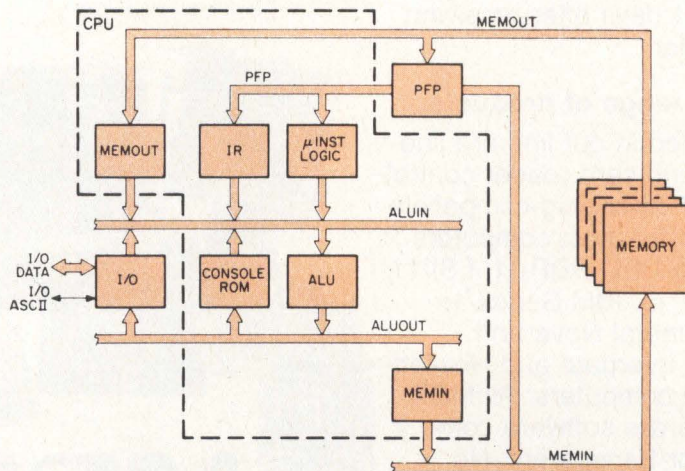
Resident on the CPU board of the /X, the memory management and protection unit performs logical to physical address translation giving user programs access to 256k bytes of main memory through four address extension tables: two program maps and two data channel maps. The unit also permits privileged instructions, protection for I/O devices, and both write and validity protection for main memory. With RDOS software, the MMPU makes dual operations possible. The protection feature prevents addressing areas outside user space; any memory references outside user space are trapped before they can interfere with another ground or the operating system.

Internal diagnostics run automatically when power is turned on, or is restored after a failure, testing CPU, memory, and the prefetch processor. Built-in memory test diagnostics can exercise main memory at a stress level substantially beyond that encountered in normal operation, allowing fast isolation of soft failures.

System and application software is executed under RDOS, RTOS, or DOS. Language support includes FORTRAN IV with ISA realtime extensions, globally/locally optimizing FORTRAN 5, Business BASIC, single and multiuser extended BASIC, and ALGOL. Communications support includes the communications access manager, sensor access manager, RJE80, and HASP II remote batch terminal emulations.

Typical configuration prices include \$3500 for a NOVA 4/C with 64k bytes of memory, asynchronous interface, automatic program load, power fail/auto restart, and 5-slot chassis. A 4/S with the same complement plus realtime clock and 16-slot chassis has a tag of \$7600; and a 4/X with 256k memory, floating point processor, MMPU, battery backup, 20M-byte disc, magnetic tape subsystem, 180-char/s printer, and four displays is priced at \$56,886. All prices are single quantity. Deliveries will begin by March for /S and /X, by June for /C.

Circle 140 on Inquiry Card



Block diagram of Data General Nova 4. Minicomputer family incorporates prefetch processor and advanced memory architecture for enhanced performance. Memory features include separate data in and data out buses. Console ROM runs self-diagnostics at power up and allows user to access and modify all registers and memory locations

NEC Spinwriter. The fluent printer.

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Users of word processing, computer output or terminal character printers expect fine print quality from their character printers.

But with NEC Spinwriter™ printers, you get even more. Our unique "thimble" – with up to 128 characters – gives you many extra features no other printer offers.

Like bi-lingual fonts, so you can print in any two languages at once. Or multi-lingual fonts – with up to five languages on the same print element: English, French, German, Spanish and Italian. Or technical/math thimbles with full alphanumerics, plus super- and subscripting and many arithmetic and scientific symbols.

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and PS pitches, and our low-cost custom thimble design capabilities.

That's six extras so far. Seven: speed. Spinwriter printers use lightweight thimbles, so they print at a full 55 cps. Eight: durability. Our fiberglass-reinforced elements last up to 30 million impressions. And finally: quietness. Spinwriter thimbles are so much quieter than other character printers that you can hear the difference.

Now add those features to Spinwriter's acclaimed reliability, serviceability and ease of use, and see if you can find a reason for not including them in your systems.

And don't forget our Trimliner™ band printers. The ideal line printer for products that need 300-to-600 LPM output that you can always rely on.

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CIRCLE 24 ON INQUIRY CARD

FOR RENT...NOW...

Beehive's versatile and easy-to-use B100 and Mini Bee 2 terminals, both available for immediate short-term, low cost rentals today.

If you need a self-contained, feature-filled video display terminal fast, the B100 will fill the bill . . . and it's available today. Beehive International's B100 features both RS232C or current loop interface, has switch selectable transmission rates from 75 to 19,200 bps, and includes cursor control. You'll also like the addressable cursor. The terminal has an easy-to-read 12-inch non-glare screen which is formatted to display 24 lines with 80 characters per line. You can choose upper and lower case characters, too. The B100 has a total page memory of 1920 characters, and the 82-key, ANSI compatible keyboard features auto repeat, 2-key rollover and alpha lock. The addressable cursor lets you directly position by line and column, and an erase mode allows you to erase from cursor to end of line, from cursor to end of memory, and clear. You'll also find operation more efficient because of B100's 11-key numeric pad with decimal and additional function keys. Communications mode is Full Duplex (Echoplex), Half Duplex, and Block (asynchronous 10 or 11-bit word). It's ready for you now.

The low-rental rates on Mini Bee 2 will make you happy if you need a TTY-compatible terminal with cursor control and a detachable keyboard. Beehive's Mini Bee 2 is a stand-alone, operator/computer accessible remote display terminal with a detachable keyboard. You use Mini Bee 2 to transmit and receive data serially through an RS232C interface at any of several preselected transmission rates to a maximum of 9600 baud. Mini Bee 2 has a 12" rectangular monitor which displays 25 lines with 80 characters per line. It has a total page memory of 2000 characters, and each character is generated from a 5x7 dot matrix with two dot spacing between adjoining characters. Communications mode can be full duplex, half duplex, 10 or 11-bit asynchronous word. Mini Bee 2 also features character-by-character transmission, an escape sequence mode for unique CRT functions, and an erase mode. It's also available off-the-shelf from REI immediately.

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- Rexdale, Ontario (416) 675-7513
- Montreal, Quebec (514) 681-9246; Vancouver BC (604) 684-6623

Plug Compatible Add-On Memory Increases 303X Capacity to 16M Bytes

To provide IBM 303X users with up to 16M bytes of memory, Ampex Corp, 200 N Nash St, El Segundo, CA 90245 has developed the ARM-303X plug-compatible add-on memory. Modularly designed, the memory system is self-contained in a compact package that installs on a hinge in place of a computer cabinet door. It is also available as a freestanding unit.

ARM-3031 and -3032 units have 4-way interleaving and are expandable in 1M-byte increments; the -3033 has 8-way interleaving and is expandable in 1M-byte increments. All three allow up to 16M bytes in one cabinet, and do not require IBM memory to be installed. In the field, expansion is accomplished with plug-in memory boards and add-on card cage. Each board has capacity for 256k bytes.

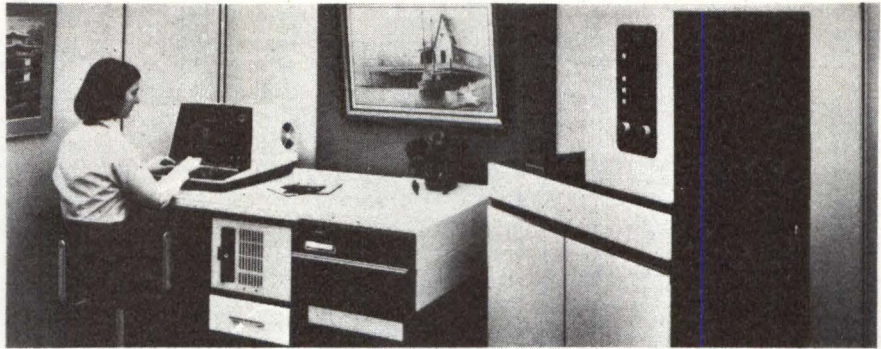
The memory system consists of frame interface logic, memory timing, control logic, memory boards, power supply, error detection panel, and cooling units. A special fault indicator panel at the operator console shows whether a fault lies in the add-on memory or elsewhere. A probable cause is indicated if the fault is located within the memory.

Power consumption is rated at 0.9 kVA at 208 V for the first 2M bytes; and 0.4 kVA at 208 for each additional 2M-bytes. Heat dissipation is 2100 BTU/h for the initial 2M bytes and 950/h for each 2M-byte addition.

Circle 141 on Inquiry Card

Distributed Intelligence Key to Word Processors And Image Printer

OIS/100 office information systems—/130 and /140—multiply the word processing power of present systems and add information processing potential. In designing the systems, Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851 has added distributed intelligence hierarchies, allowing a single system to expand to 924k bytes of memory, with 33 microprocessors distributed throughout major components. Providing high speed, high quality output for the series is an intelligent image printer that uses fiber optics



Providing typewriter quality output at 18 pages/min using fiber optics and CRT technology, Wang's intelligent image printer is designed for use with OIS/100 series word processing systems

and CRT technology to produce documents 50 times faster than conventional typewriters.

Modularity allows the systems to be upgraded to meet growing requirements. Capacity starts with the single disc /130 with 10M-byte capacity and up to 14 peripheral devices and grows to the /140 with three discs storing 170M bytes and attaching 32 devices. A major factor in the expanded capacity and performance is the increase in memory which is available within each system component. In the distributed intelligence architecture, logic, memory, and operational functions reside in each major component, rather than just in the CPU. As an example, each workstation contains a 32k-byte memory and circuitry that allows it to perform operator prompting and editing tasks; each printer has 16k bytes plus processing circuitry. In addition, both units have microprocessors.

Capable of producing 18 pages/min, the intelligent image printer combines fiber optic and CRT technology with a plain paper, dry toner copying process to provide typewriter quality copy. It allows type styles and sizes to be mixed and vertical and horizontal printing functions to be combined in a print run. It can be operated either as a printer or as a copier.

In use, a computer originated document stored on the system disc is transferred through a data channel to the microprocessor control unit of the printer, which assigns print commands and selects font and type sizes. The digitized document is converted by a character generator into precise visual images that are displayed a line at a time on the surface of a CRT

located inside the printer. As each line is displayed, it is scanned by electronics and converted into a light pulse read by a fiber optic subsystem. Each pulse is transmitted through a fiber to twin photoreceptors positioned directly above the paper to be printed. The light pulse is reconstituted into character images that are painted onto the paper. Resolution can be as great as 90,000 dots/in² (13,949/cm²). A dry toner is then electronically bonded to the paper, forming each character.

Selective paper handling capability of the machine allows several types of paper to be used in sequence without operator intervention. Since sets of documents are printed in sequence, there is no need for a collating mechanism. The speed of the unit allows it to be used as an output device shared by as many as 24 operators.

Among the other peripherals supported by the word processing systems are printers, photocomposers, telecommunications interfaces, and OCR devices. Software provides capability to perform sort routines and to handle many accounting functions. Password security assures confidentiality of records.

Circle 142 on Inquiry Card

64k-Bit RAMs, ECL 100k Circuitry Add Power to Large Computer Systems

Technological and design features in the V-8600 family provide the performance and reliability required by large system users. Among these are extensive use of ECL 100k circuitry, 64k RAM chips, internal transfer bus

architecture, and multiple virtual machine capabilities. According to NCR Corp, Dayton, OH 45479 the V-8650 and -8670 processors initially forming the family are suited to the large volume transaction processing environment that will characterize the 1980s.

Extending the flexible architecture of the 8500 systems (see *Computer Design*, July 1976, pp 30, 34) to the large systems environment, the 8600 family is based on an internal transfer bus, a data highway to which all other system components are linked. Each data path on the transfer bus is 32 bits wide and can transfer messages between subsystems at a rate of 72M bytes/s.

The processor subsystem uses ECL 100k, an integrated circuit family with picosecond gate speeds. The processor cycles at 28 ns and uses a pipelining technique for executing instructions. Each instruction is broken into segments; multiple segments can be processed simultaneously.

A high speed instruction storage unit in the processor stores firmware or microcoded instructions which are loaded into the system via flexible diskette. This firmware interacts between the hardware and software to give the machine its processing personality. The machine can be conditioned to process statements written in a specific programming language, providing faster compilation and execution than processors that are not language oriented. Processing power is further increased by use of a fast access buffer or cache memory which reduces memory access time by a factor of six.

Two medium scale processors in the system control unit monitor system

elements on a millisecond basis. The unit controls two visual displays and functions as operator control center as well as system diagnostics unit. Diagnostics can be performed concurrently with normal operations.

From two to four channel control processors in the I/O subsystem can attach to the system bus. These can control up to 32 channels, each with a 2M-byte/s transfer rate. Channels feed directly into a dynamic channel exchange switching center that automatically routes the data flow to one of the channel control processors for transmission to other system elements. This distributed processor design provides high reliability and speed.

Both systems operate with the virtual resource executive (VRX) which provides batch processing, telecommunications, transaction processing, data base, and interactive application development capabilities. They also conform to distributed network architecture and can be conditioned to operate as FORTRAN virtual machines.

With 28-ns main processor, 32k bytes of cache memory, and main memory that extends from 4M to 8M bytes, the V-8650 with 4M bytes of memory sells for \$1,776,500. This price includes operator console and two I/O channel control processors serving up to 16 I/O channels. The dual processor V-8670 provides 128k bytes of cache memory and from 4M to 16M bytes of main memory. Priced at \$2,555,000 with 4M-byte memory, this system includes twin station console and 2 channel control processors with 16 I/O channels. Customer deliveries are planned to begin in fourth quarter 1980.

Circle 143 on Inquiry Card

which works in conjunction with cache. A 4-byte (32-bit) memory access yields a worst case (cache miss) memory access time of 750 ns for four consecutive bytes.

Among the system options are a 64-bit floating point processor which performs both single and double precision arithmetic functions. This processor works in conjunction with optimized ANSI 77 FORTRAN to provide speed and accuracy in scientific applications. A writable control store option offers up to 12k bytes of 150-ns writable control store and 2048 bytes of P-ROM.

MEGAMAP memory management system, standard on the system, allows addressing of up to 2048k bytes of memory by dividing the area into 1024-byte pages which are allocated as needed. Operating systems include the VORTEX II as well as the SUMMIT system.

Among the key options of the SUMMIT software package are support for PASCAL as a component of the structured programming system and for QL/77, an inquiry/update language used in conjunction with the TOTAL database management system. Another option is the distributed processing modules that allow terminals to access series 90 or 1100 mainframes, remote V77 series computers, and IBM System/370s.

Terminal operation is supported in asynchronous block or character mode, binary synchronous block mode (3270 emulation), or synchronous block mode with Uniscope or intelligent UTS-400 terminals. Terminal management and control capabilities include timesharing, transaction processing, online program development, remote job entry, remote processor access from any terminal, online database inquiry and update, and a comprehensive security system that allows access to data and applications programs based on IDs and passwords.

System PASCAL is a high level general purpose language that is applicable to both numeric and nonnumeric problems; it has the data structuring capabilities of COBOL, block structured organization of ALGOL, and compact arithmetic expressions of PL/1. Its control structures are conducive to topdown design and structured programming techniques. With the language, arrays may be multidimensional and may include arrays of arrays. Different data types may be combined into a single entity and stored as one logical component.

High Speed Minicomputer, Support for PASCAL Added to Line

Extending the existing V77 line, the V77-800 minicomputer represents a major performance increase over other members of the family. With a 150-ns CPU cycle time, the system processor performs arithmetic and logic operations on 16-bit instructions and data, and uses a 1024-byte 150-ns cache memory to speed execution. For use on this system and on the -600, Sperry-Univac Minicomputer Operations, PO Box 500, Blue Bell, PA 19422 also introduced a multitask-

ing terminal oriented operating system that supports the PASCAL language.

Designed both for commercial and scientific use, the system operates as a standalone unit, frontend processor, or as part of a distributed network with Sperry Univac and IBM mainframes. The CPU has 6k-byte onboard control store for sequencing processor operations, hardware multiply/divide, realtime clock, and power fail/restart logic.

Built-in cache memory is twice as fast as the cache that was optional on the -600. Support is provided for 128k to 2048k bytes of 600-ns memory



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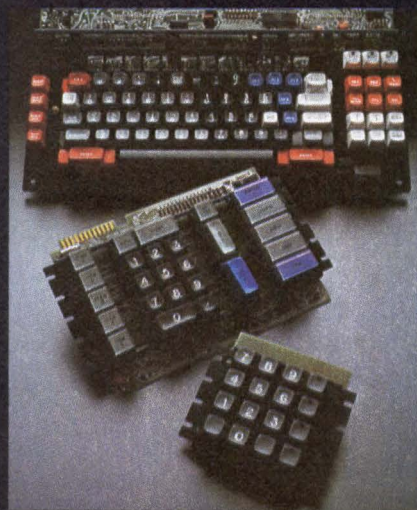
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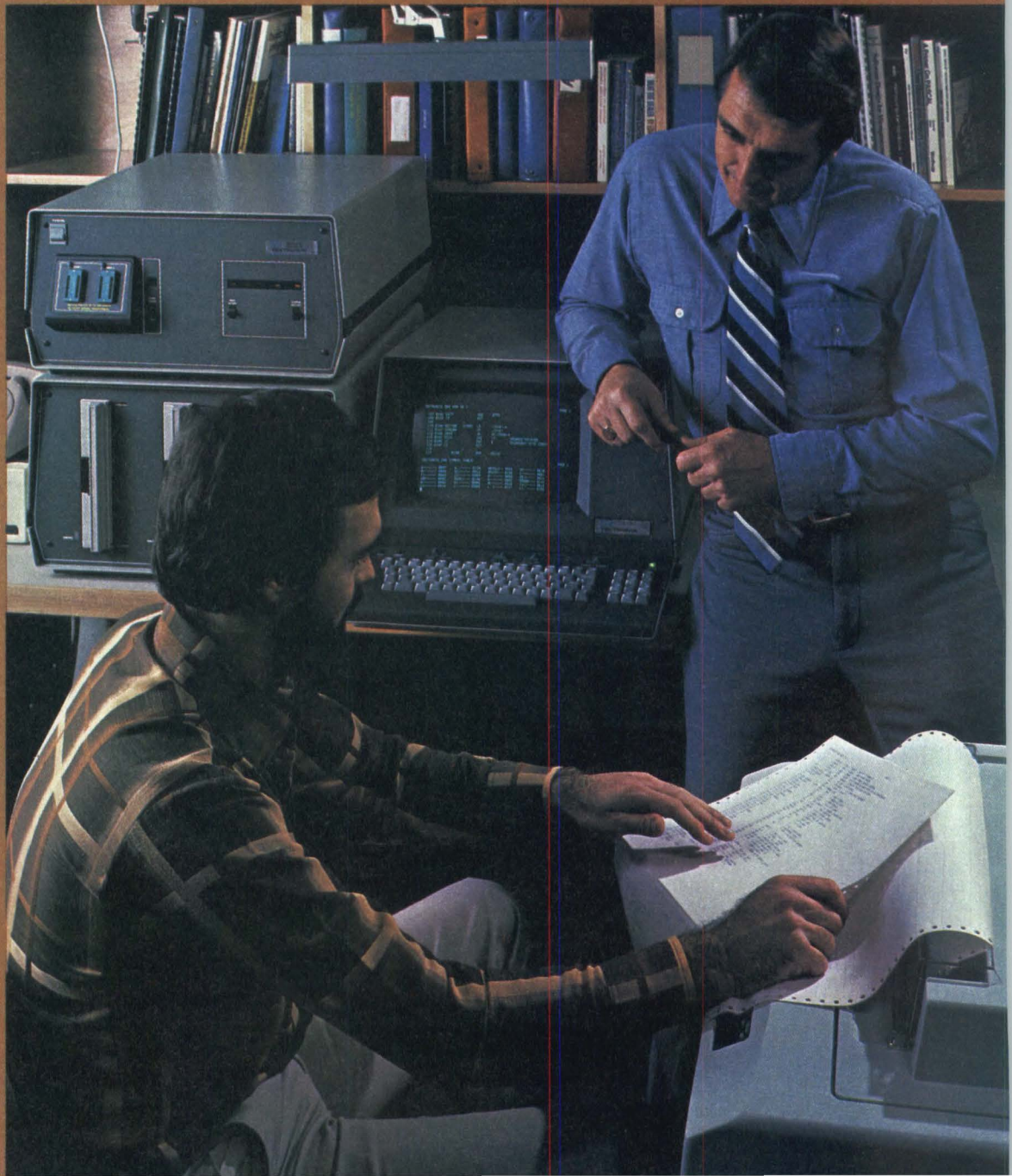
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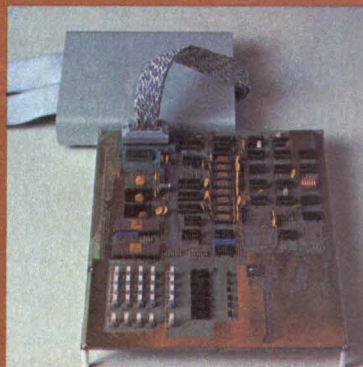
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logic problems by dynamically monitoring the microprocessor bus.

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This specially enhanced, compiler version of BASIC is compatible with the 8080 and 8085, and includes a subset of Z80 instructions. Extensions include comprehensive interrupt handling and optimization features to produce compact code.

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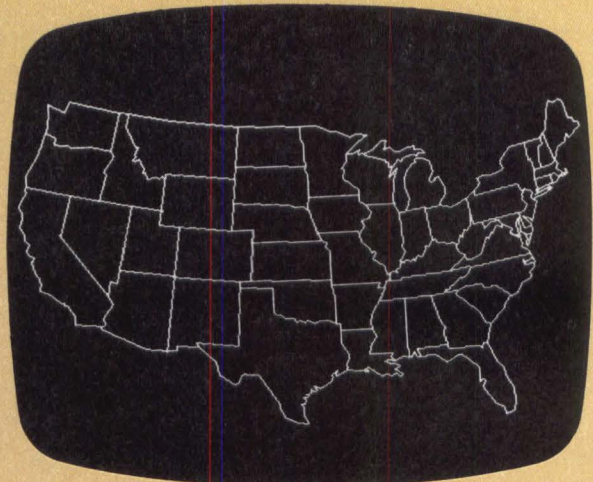
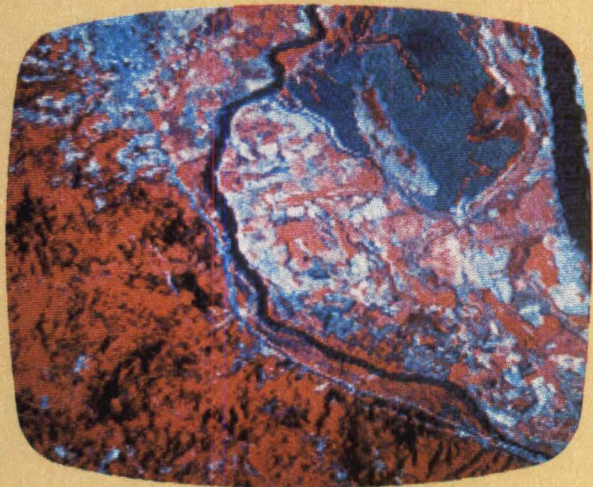
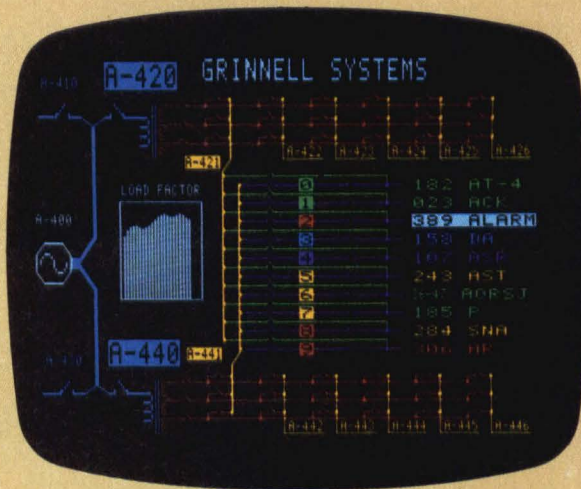
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CIRCLE 30 ON INQUIRY CARD

The structured programming system allows users to enter, edit, and compile PASCAL programs for execution under the SUMMIT operating system. It also includes a diagnostic scheme that allows programs to be executed a line, a paragraph, or an entire program at a time, with diagnostic aids to indicate both error conditions and performance information.

By supporting COBOL, FORTRAN IV, FORTRAN 77, RPG II, and assembly languages, the software allows the user to choose the most appropriate language for his particular requirement. Microprogramming support enhances software and hardware performance. Circle 144 on Inquiry Card

a laser source that scribes a track by melting the surface and leaves pits to record data. Unique to the system is the proprietary trilayer disc that uses a laser sensitive material for recording and playback.

The trilayer structure (see Fig 1) of the optical disc is formulated to provide wideband high SNR response at low laser recording levels. Fabricated to operate in an antireflective mode, the trilayer section consists of a thin metal layer and a reflector layer separated by a transparent dielectric layer. Thickness of the metal and dielectric layers are adjusted to allow a component of incident light

to pass through the metal layer and reflect back so that it is out of phase and equal in amplitude with the reflected component of the incident beam. This results in near complete cancellation, while the trilayer structure absorbs essentially all of the incident laser radiation. Efficiency is further enhanced by SiO₂ thermal barrier layers around the trilayer section which insulate it, allowing absorbed energy to rapidly elevate the temperature of the metal layer to the melting point.

To record, the laser source is focused on one side of a blank optical disc. The disc, which is normally ab-

Optical Video Disc May Meet Future Needs for High Volume Data Storage

Capable of storing 10¹¹ bits of data on a 12" (30.5-cm) disc, an optical disc system under development at RCA Corp, Commercial Communications Systems, Cherry Hill Offices, 206-1, Camden, NJ 08101, is expected to meet future needs for archival mass storage of data. The system, as described by G. J. Ammon of The Advanced Technical Laboratories, in a paper entitled "Wideband Optical Disc Archival Data Storage," records information as the disc rotates under

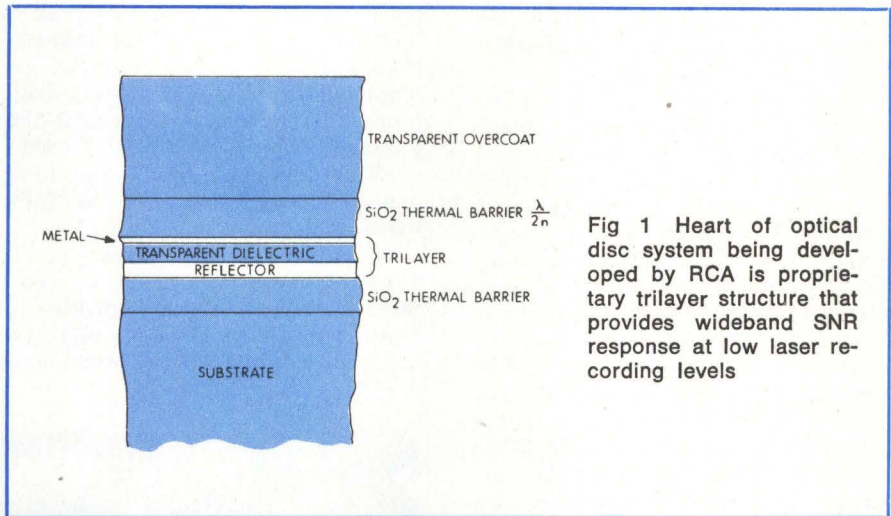


Fig 1 Heart of optical disc system being developed by RCA is proprietary trilayer structure that provides wideband SNR response at low laser recording levels

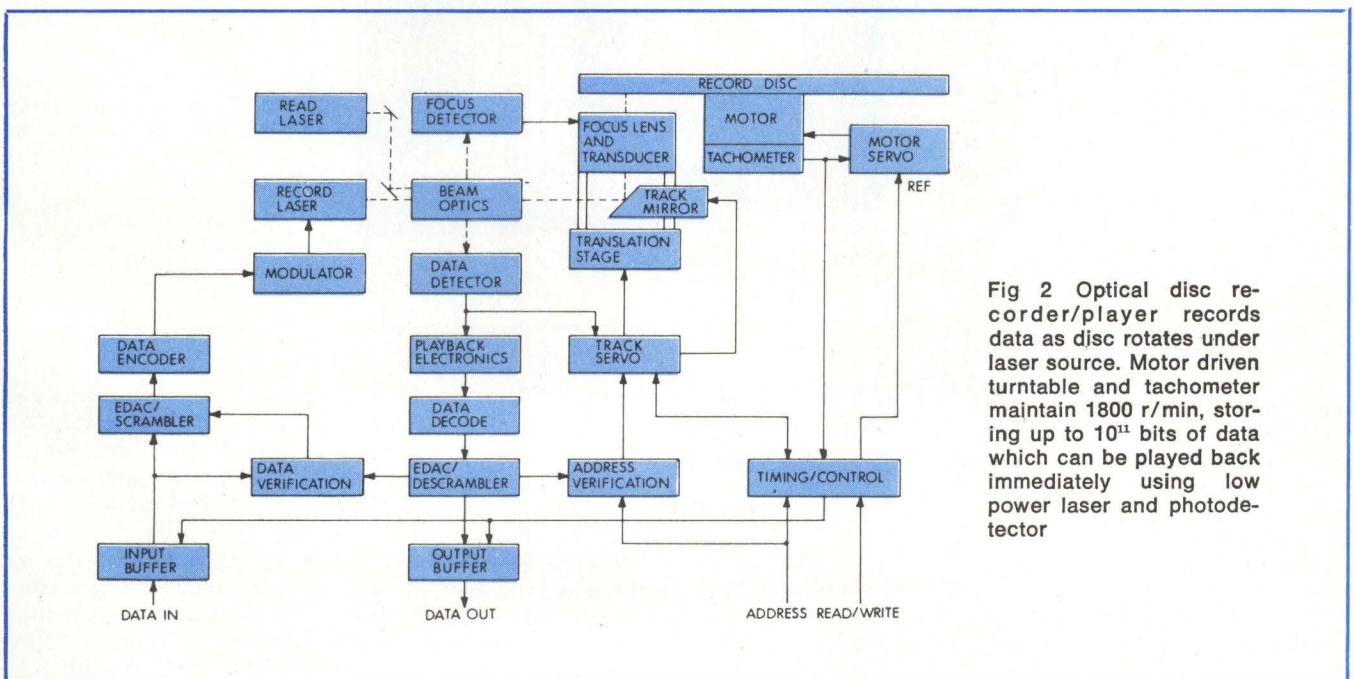


Fig 2 Optical disc recorder/player records data as disc rotates under laser source. Motor driven turntable and tachometer maintain 1800 r/min, storing up to 10¹¹ bits of data which can be played back immediately using low power laser and photodetector

sorptive and appears black, is rotated so that a laser spot scribes a circular track on its surface. Raising the laser's power above the disc's record threshold causes the absorptive layer on the disc to be melted away, thus exposing the second reflective layer. By modulating the laser, the process can be used to record a series of reflective pits whose lengths vary with the time of exposure. Playback is accomplished by operating the laser at a constant level below the disc's record threshold and detecting the reflected optical signal with a photodiode.

Data to be recorded are loaded into the input buffer (see Fig 2). This buffer provides expandable storage to handle asynchronous data at different rates and serves to block and add address and header information necessary for data access and synchronization during readout.

EDAC/scrambler circuitry mixes data to disperse long burst errors encountered in the record/playback process and adds error detection and correction check bits for subsequent error control. The encoder converts the incoming NRZ data stream into a modulation format which matches channel characteristics of the optical disc and allows maximum storage density.

Data verification is accomplished by reading data with the second laser after recording. This laser's output is coupled into the optical path of the record system to illuminate the data track just after the point of recording. Detected data are decoded, descrambled, and corrected in the EDAC/decoder, and the resultant NRZ data stream is compared to the original stream (delayed in the input buffer). Blocks having uncorrected errors are rerecorded.

During data readout, only the read laser is activated and the detected signal is processed as in the read after write function. Data are checked by comparing read address information to that on the address input, with data from the proper track being held in the output buffer until transfer is requested.

This recording method has obvious advantages over magnetic storage media—cost of the media is low and density is high. With proper modulation coding and error processing, the system can store 10^{11} bits of data on a 12" (30.5-cm) disc with single channel data rate of 50M bits/s and error rate of 10^{-10} . Efforts are continuing on development of an archival digital data storage system.

Circle 145 on Inquiry Card

Packaged Systems Meet Varied Configuration Requirements

In the System 1, 04, and 34 families of packaged systems Plessey Peripheral Systems, 17466 Daimler, Irvine, CA 92714 offers a variety of configurations to provide users with substantial savings. Based on PDP-11 processors and available with DEC operating systems, the packages are designed to meet specific configuration needs.

System 34, for high volume data processing users, is based on the PDP-11/34A central processor with 64k-byte MOS memory, programmer console, asynchronous serial interface with realtime clock, disc controller, bootstrap loader, and bus termination. Providing such features as extended instruction set, self-test diagnostics, and memory management, the packages include 5M-, 10M-, 62.4M-, or 256M-byte disc drives and have main memory expandable to 256k bytes of MOS or core.

Running under DEC's RT-11, RSX-11M, and RSTS/E, or Plessey's PCS-001, each system can provide all features of an RT-11 single user system plus a timesharing monitor. PCS-

001 enables BASIC, FORTRAN, and DIBOL programs to run concurrently on different terminals. With the appropriate operating system the machines can run under FORTRAN IV, FORTRAN IV-Plus, DIBOL, BASIC-Plus-2, and COBOL-11.

Designed for users requiring increased speed, the 04 family uses the PDP-11/04 processor with programmer console, is equipped with 5.25" (13.34-cm) chassis and 64k bytes of addressable MOS or core memory, and offers the choice of floppy or cartridge disc unit. Running under the RSX-11M multiuser, multitask operating system, the unit can operate on FORTRAN, BASIC, BASIC-Plus-2, and COBOL-11 programs.

Complete general purpose mini-computer systems, the System 1 family is constructed for use in demanding environments. Built around the LSI-11 based MICRO-1/03 with up to 64k memory, the system is available with dual floppy drives or 5M- or 10M-byte disc drives, and is packaged in a 29" (73.66-cm) high cabinet. The processor features an extensive instruction set and operates under RT-11 for single user access, or TSX, an executive program that permits time sharing under RT-11. Languages include FORTRAN, BASIC, and DBL.



Circle 146 on Inquiry Card

Economical System 1, designed around Micro-1/03 by Plessey, is constructed to withstand demands of factory and warehouse environments

Entry Level System Adapts to RJE or Standalone Use

The META 4/5010, in addition to being suited to use for remote job entry as well as a standalone processor, provides a price/performance ratio and comprehensive instruction set that are attractive to system integrators. An entry level system, the 4/

5010, announced by Digital Scientific Corp, 11425 Sorrento Valley Rd, San Diego, CA 92121, also incorporates the SENTRY power and environmental monitoring system that contributes to system reliability.

Standard system accommodates up to 64k bytes of main storage using n-channel RAMS. Memory cycle time is 500 ns with each memory word including two data words plus one par-

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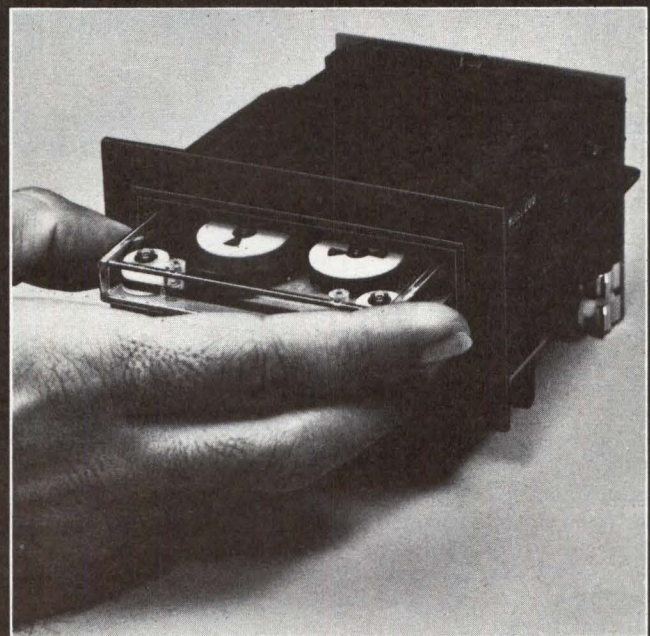
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ity and one protect bit. Expansion beyond 64k is achieved using an optional similarity package.

The 5010 is a 16-bit word length system that can directly address all storage. The machine's mnemonic instruction set includes a subset of commands for emulating IBM 1130 or 1130 type systems. Software packages for simulating IBM 2780, 3780, and

some 3740 model terminals operating with /370 series, Amdahl, and Intel systems are available. In addition, the unit can perform RJE functions to Univac 1100 series systems operating under Exec 2 and 8 operating systems and to Control Data systems operating on UT200 terminals. Communication with any system supporting bi-synchronous communications at rates

to 9600 baud is possible. The DM-2 operating system includes an assembler and FORTRAN compiler; an expanded FORTRAN compiler is available as an option.

In a minimum configuration, made up of CPU, realtime clock, I/O facility to accommodate four I/O controllers, 16k bytes of memory, 600-card/min reader, 300-line/min printer, and 1M-byte cartridge disc, price is \$43,300. A communication oriented system expanded to 32k bytes of memory and providing a binary synchronous communications adapter and IBM 3780 support is priced at \$48,900.

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SOFTWARE

Cross Assembler Cuts Time Needed to Program Graphics Display Systems

Cross assembler software written in FORTRAN IV reduces the time and effort needed to translate and develop programs for graphic display systems. Genisco Computers Div of Genisco Technology Corp, 17805 Sky Park Dr, Irvine, CA 92714 used FORTRAN IV in preparing the package because of its compatibility with most commonly used existing data banks. Provided in 9-track 800-bit/in (314/cm) magnetic tape format, routines can be auto-loaded from host CPU to the company's programmable graphics processor. The package assembles the processor's set of 55 mnemonic instructions.

The package's basic syntax defines allowable source input characters—alphabetic, mnemonic, and special—and gives instructions for symbol names that may be assigned values by an equate pseudoinstruction. Numbers may be written in octal, decimal, or hexadecimal. Operators and operands within an expression are evaluated from left to right. Source statements may consist of comments, pseudoinstructions, or graphics processing assembly instructions, and may be in free format. Each statement is a record in the source input file.

Pseudoinstructions are directives to the assembler that control the assembly translation process. Assembly routines are usually stored in an auxiliary memory space and loaded into the graphics processor's buffer for execution as overlays. □

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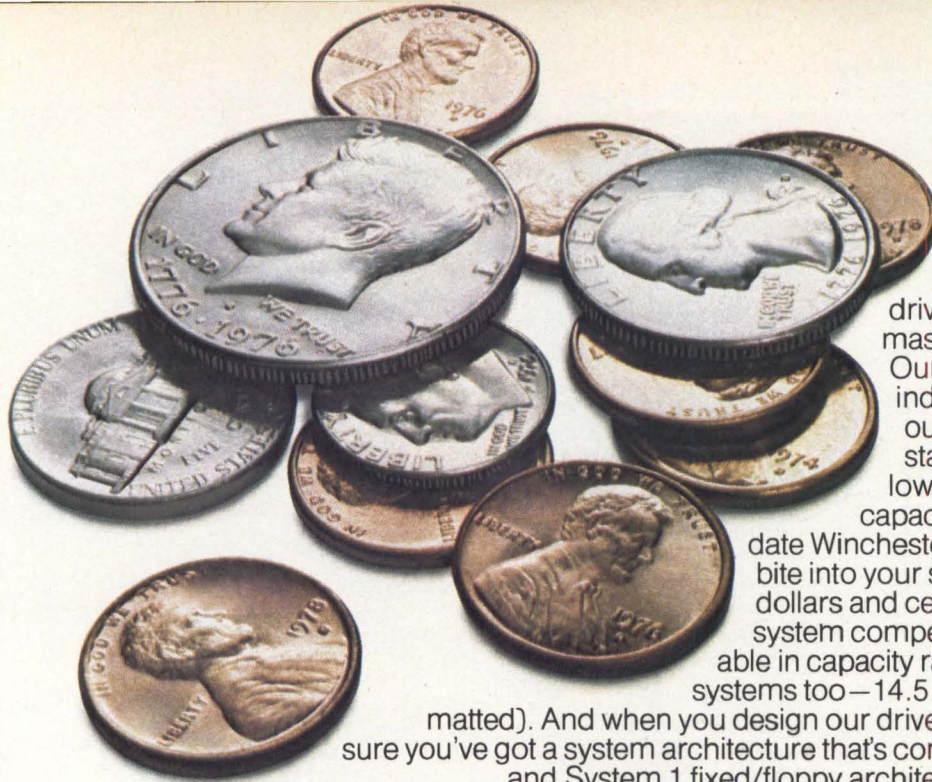
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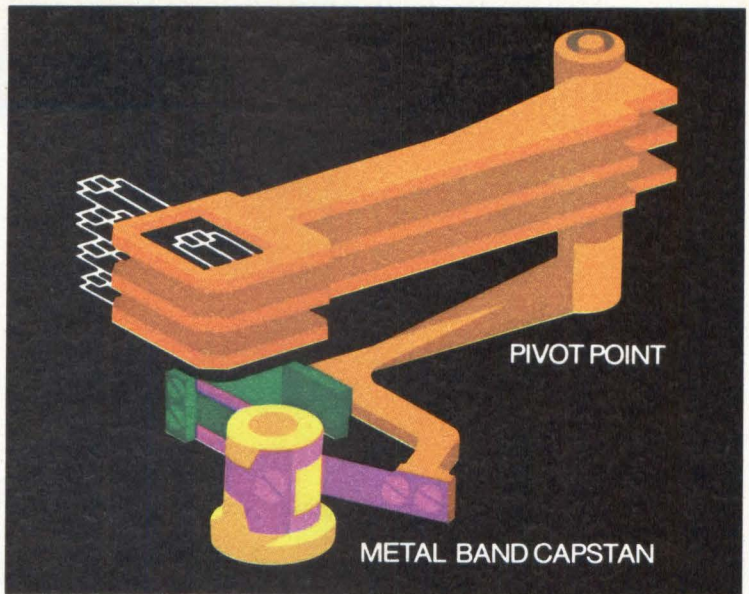
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The SA4000 Series of rigid disk drives are the newest line of low cost mass storage products from Shugart. Our floppy disk drives have been the industry standard for years, and now our fixed disk drives are setting new standards of their own. Like the lowest cost per megabyte in their capacity range so you can have up-to-date Winchester storage at a price that won't bite into your system profits. That means real dollars and cents savings to help keep your system competitive. SA4000 drives are available in capacity ranges that are just right for most systems too—14.5 and 29 megabytes (unformatted). And when you design our drives into your system, you can be sure you've got a system architecture that's compatible with IBM S/32, S/34 and System 1 fixed/floppy architecture.

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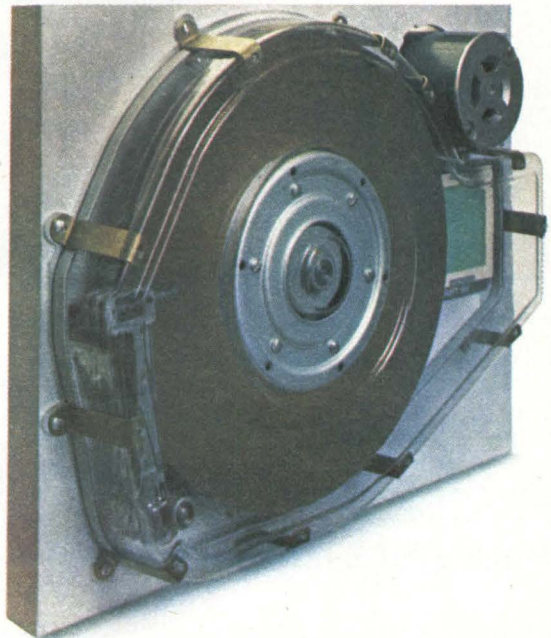
Winchester Technology and Two Configurations.
Shugart fixed disk drives use industry-proven Winchester head and media technology to preserve your data in its own safe, sealed environment. The model SA4004, with 14.5 megabyte capacity, utilizes one disk and four heads. The SA4008, 29 mbyte version, has two disks and eight heads. Eight optional fixed heads are available to give you an additional 144 kbytes (unformatted) of head-per-track storage for applications such as indexed files or table look-up. The SA4000 Series offers an easy upgrade too. Keep your floppys for I/O and system back-up. Add our rigid disk drives for the additional capacity and throughput you need to upgrade your operating systems and mass storage.

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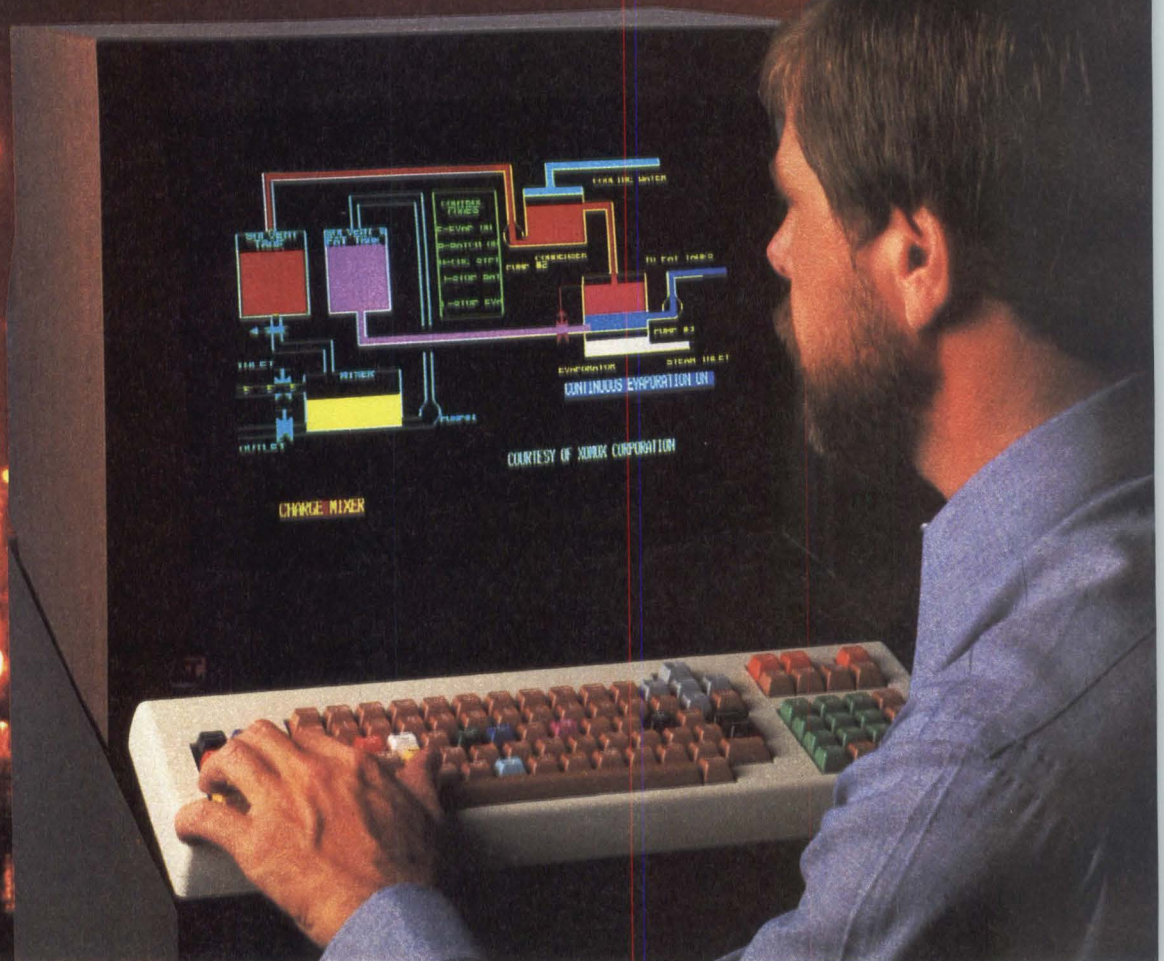
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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Compact Controller Manages Industrial Systems in Real Time

Applications of realtime measurement and control are almost universal in scope. Relatively small samplings within a laboratory environment would include monitoring of experiments, medical and biomedical research, analytical instrumentation, and product development. Industrial areas might include product testing and quality control; sensor based monitoring and alarm; logging, plotting, and display; process simulation; and pilot plant process control.

One system that has met the fundamental measurement and control requirements but that was never widely distributed has served as the prototype for a next generation system that is to be marketed. MACSYM I, used in a number of measurement and control applications under evaluation conditions, has now been superseded by MACSYM II (see *Computer Design*, Dec 1978, pp 164-165); both systems were developed and manufactured by Analog Devices Inc, 365 University Ave, Westwood, MA 02090.

Some of the applications of the MACSYM I controller include testing of battery cells to determine expected life, controlling the temperature of the water in jacketed tanks, and controlling the temperature of autoclaves. Information gained from these systems was used in the development of MACSYM II.

Battery Research

Three primary functions are performed during the life testing of storage cells: providing alternate cycles of

constant current charge and discharge of the cells; removing fully charged or discharged cells from the circuit to prevent damage while others are still in operation; and acquiring voltage vs time data for each cell, manipulating the data, and presenting the final data in tabular and graphic forms. The basic system configuration for performing long term life tests of experimental cells is shown in Fig 1.

In this case, the controller furnishes constant current to the cells under test in either direction by switching load resistors and controlling the direction and magnitude of a programmable power supply. A shunt resistor provides feedback information for precise current setting. During the charge cycle, the controller periodically checks the voltage across each cell, and when the voltage reaches a preset level, disconnects that cell from the circuit to prevent overcharging. The same process disconnects discharged cells from the circuit during the discharge cycle. Cell voltages are periodically sampled and the readings stored on a floppy disc in each cycle.

Because all test functions are performed in a continuous operation, software completes all control functions and performs necessary data reduction concurrently. It also presents a hard copy of the data when requested. The entire program is written as a series of independent tasks for each of the three functions.

MACBASIC, the multitasking programming language used, also provides a full set of graphic commands. That enables researchers to obtain fully annotated plots of

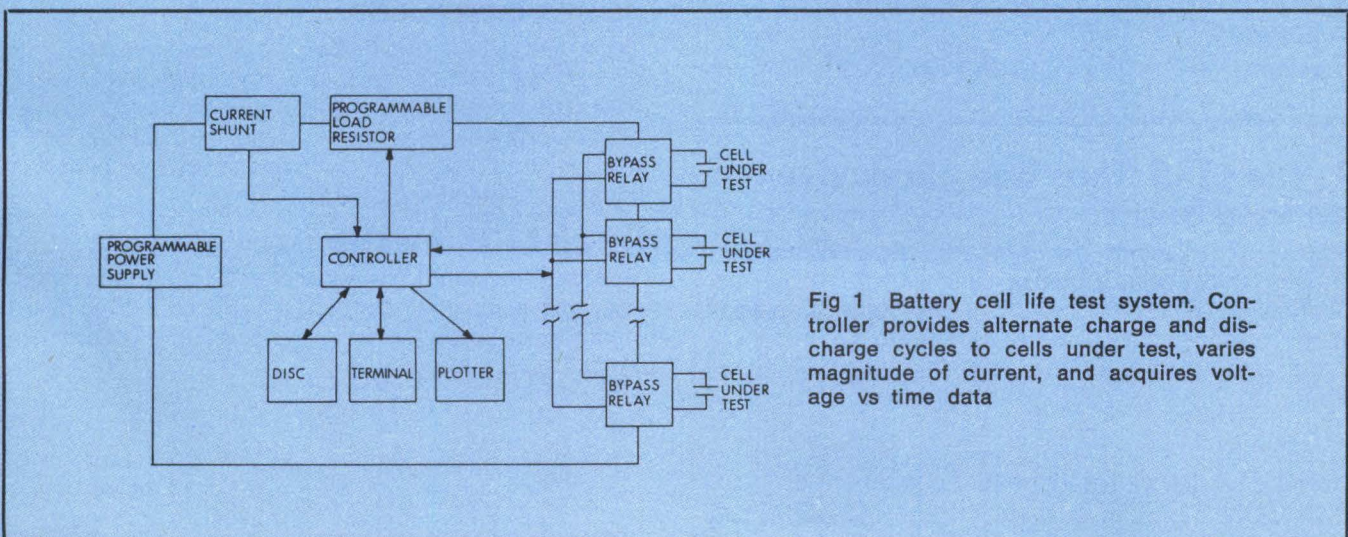


Fig 1 Battery cell life test system. Controller provides alternate charge and discharge cycles to cells under test, varies magnitude of current, and acquires voltage vs time data



TWELVE REASONS WHY THE L135 IS THE MOST PRODUCTIVE LSI BOARD TEST SYSTEM YOU CAN OWN.

To compare productivity in LSI board testers, take their three common operations: diagnosing, testing, and programming. Now, to each operation apply the basic measures of productivity: cost, throughput, and quality of testing.

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1. The L135 finds bad LSI devices on long buses.

The Electronic Knife does it. It takes just a few more probes after regular guided probing finds the failing bus. Without the Electronic Knife, you're faced with trial and error replacement of LSI chips. Or skilled technicians tying up the system for an hour or more per bad IC.

2. The L135 makes fewer diagnostic probes – by an order of magnitude.

State-sensitive trace does it. Most LSI boards are loaded with multi-input LSI chips linked through “wired-and” bidirectional buses. These often require hundreds of diagnostic probes per fault. State-sensitive trace cuts the number dramatically.

3. The L135 produces immediate probe commands.

The on-line circuit model with a large random-access memory does it. With circuit structure immediately accessible, the operator does not wait for commands between probes. Other test systems that use fault dictionaries often delay each command several seconds, adding minutes to each diagnosis.

4. The L135 mechanizes probing.

The M150 Automatic Prober does it. Seven to ten times faster than a human operator, the M150 speeds up board diagnosis even more because its operation is both error-free and fatigue-free.

See the full line of Teradyne test equipment at NEPCON WEST in Anaheim (Booth 449-450).

The L135 delivers the highest quality of testing, thereby slashing costs for diagnosis later at systems test and service out in the field.

5. The L135 emulates LSI-board operating environments.

5-MHz clock-rate testing does it. To ensure adequate board quality, you usually have to run LSI boards at clock rates as the last step in testing. Only the L135 provides test rates of up to 5-MHz, the speed of many microprocessors seen in today's products.

6. The L135 emulates and tests CPU sets.

Multiple drive/compare phase control does it. During clock-rate testing, the test system must first replace the CPU set and then test it at speed. The associated microprocessors usually receive multi-phase inputs and generate multi-phase outputs. The L135 provides the necessary, easy-to-program, precise phase controls over driver inputs and comparator strobing.

7. The L135 tests and diagnoses analog circuits.

Integrated ac-dc-parametric capability does it. The L135 offers many analog force-and-measure functions through matrix connections, all completely integrated into system hardware and software. If these capabilities aren't integrated into the test system, they must often be added to accommodate the increasing analog content of LSI boards. That prolongs test time and slows diagnosis considerably.

8. The L135 tests at dc and clock-rate on the same channel.

All-speed pin compatibility does it. In clock-rate testing, high-speed tests are usually applied on the same pins tested earlier with dc. The L135 allows you to apply both types of tests at the same system channel, eliminating the need for awkward switching or extra channel capacity.

9. The L135 has enough clock-rate channel capacity for the big jobs.

432 I/O pins does it. Big LSI boards have upwards of 250 edge-connector pins, all active. In addition, you need simultaneous access to dozens of internal test points and devices invisible to the edge connector. The L135 offers the highest clock-rate channel capacity, enough for all foreseeable LSI boards.

10. The L135 cuts total programming time.

The P400 Automatic Programming System does it.

The P400 automatically generates all the dc patterns and diagnostic data for the toughest part of most LSI boards: the jungle of random digital logic, as well as those portions containing modeled LSI devices. Total programming time is shorter. The best of the so-called "automated test generation" techniques offered by other systems still require manual pattern-writing. That takes longer and costs much more.

The L135 cuts the time needed to get products into the production line and out to the market place.

11. The L135 cuts system time for debugging.

Immediate-response debug software does it. During test-plan debugging, the L135 responds to the test engineer's commands and displays results immediately. Total debugging time is cut to a fraction because the test engineer is not distracted by system delays; he can concentrate on his circuit and his test plan.

12. The L135 readily assembles the many parts of LSI test plans.

Structure-merge programming does it. Test plans originate in many places: manual patterns and circuit models, learned data from known good boards, circuit and device simulators, automatic pattern generators, etc. The L135's structure-merge software and its straightforward protocol assembles them all into a coherent package, saving your engineers hours of tedious and costly work.

For more information on these and other L135 features, contact your local Teradyne Sales Office or call any of the numbers listed below.

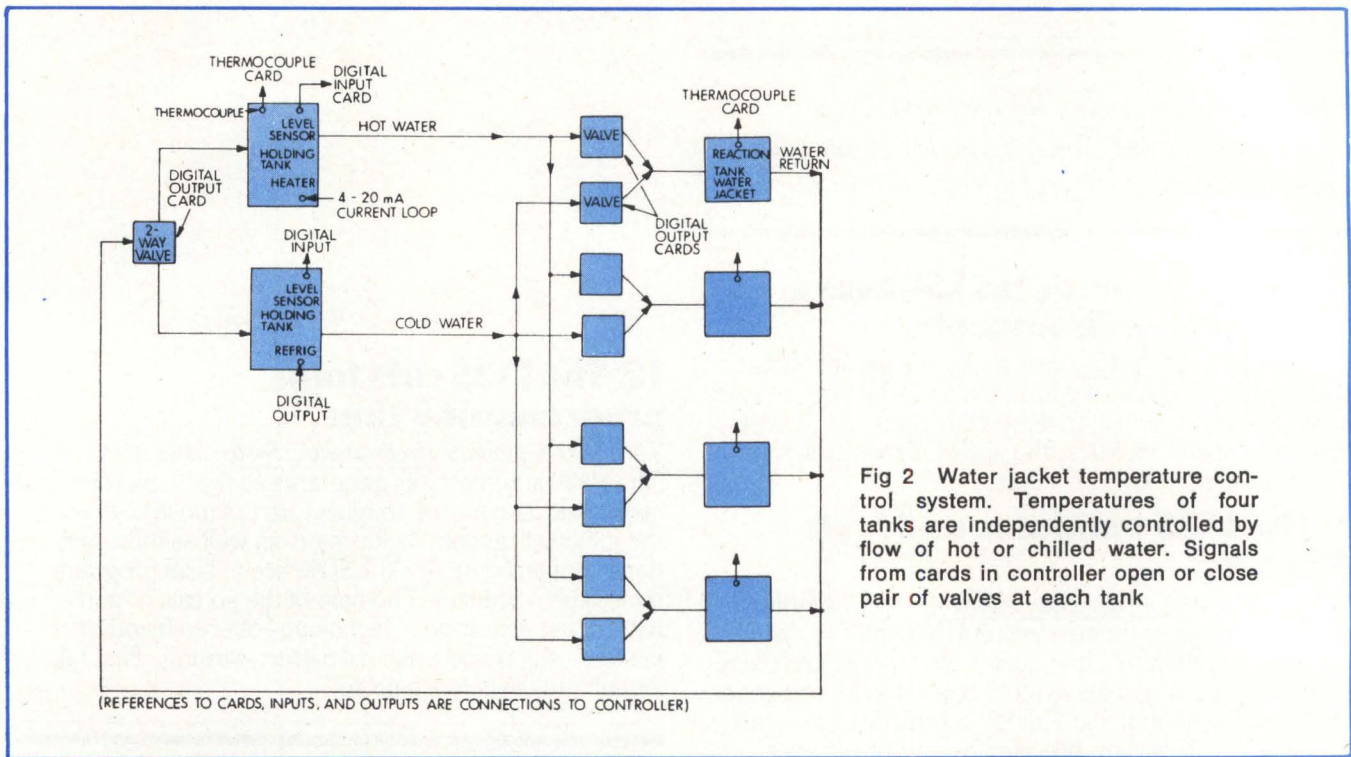


Fig 2 Water jacket temperature control system. Temperatures of four tanks are independently controlled by flow of hot or chilled water. Signals from cards in controller open or close pair of valves at each tank

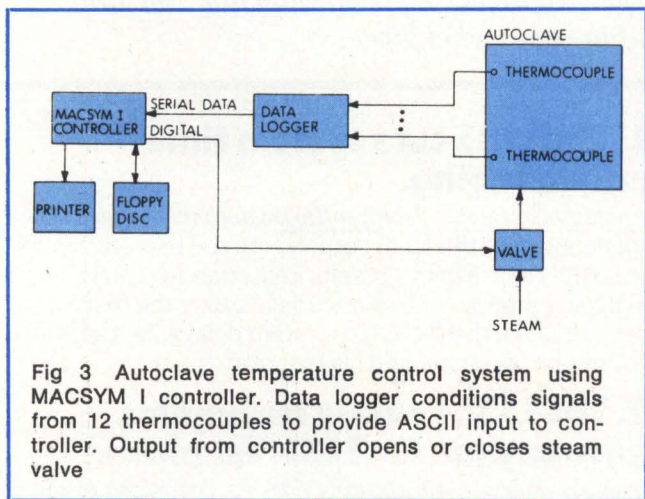


Fig 3 Autoclave temperature control system using MACSYM I controller. Data logger conditions signals from 12 thermocouples to provide ASCII input to controller. Output from controller opens or closes steam valve

such information as charge and discharge curves and capacity vs charge cycle plots for each cell.

Water Jacket Temperature Control

Fig 2 illustrates an application in which four water jacketed tanks are independently temperature controlled by introducing either hot or chilled water. A thermocouple on each tank senses the temperature variations and individual pairs of solenoid valves control the flow of water.

A temperature profile is predetermined for each tank. Whenever the temperature as measured by the thermo-

couple is outside that profile either the hot or the chilled water valve is activated. If the temperature remains within the setpoints of the profile, both water valves are shut off.

Hot water is provided from a holding tank containing a thermocouple temperature sensor and a proportional heater with a 4- to 20-mA current loop input. Chilled water is supplied by a similar tank that contains a refrigeration unit. Level sensors in both holding tanks control the position of the 2-way valve on the single line for water return.

All sensors and actuators interface directly with signal conditioning cards in the controller chassis. This eliminates the need for separate signal conditioners and their additional wiring.

Capabilities of MACBASIC enable each of the control functions to be implemented in realtime tasks. All control loop algorithms as well as full facilities for online troubleshooting are handled easily by the general purpose language.

Control of Autoclave Temperature

Drug manufacturers have a basic problem in controlling autoclave temperatures so as to provide proper sterilization of contents without damage to contents caused by excessive temperatures. Also, federal regulations force them to maintain accurate logs for each batch processed.

To meet all these requirements, a major drug manufacturing firm uses the system shown in Fig 3. Twelve thermocouples are distributed throughout the batch being sterilized. Signal conditioning is provided by a data logger that supplies a serial ASCII input to the controller. To

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CIRCLE 38 ON INQUIRY CARD

maintain a temperature within proper limits, the controller opens or closes a valve that allows steam to enter the autoclave.

At the beginning of each sterilization run, the operator is prompted to enter basic information such as drug type and batch number. When this has been completed, the controller opens the steam valve and begins monitoring the thermocouples. At each temperature scan, the controller sorts out the highest and lowest reading. When the temperature reaches 112 °C, sterilization begins and the time is noted. If the reading exceeds 114 °C, the steam valve is shut off. Monitoring continues as before, along with logging of the data and exception reporting, and steam is turned on or off as necessary to maintain the proper temperature range.

The highest temperature is used for control and the lowest temperature is integrated until a preset value or quality factor is reached. At that point steam is shut off to terminate the sterilization process. A full log of the run is printed out in conformance to federal standards. The log is also stored on floppy disc for a backup record.

Instrumentation engineers using this system were able to design and implement the applications software without having to bring in computer specialists. The software's multitasking feature enabled them to control four completely independent autoclave systems utilizing a single terminal as a shared resource.

Controller Description

MACSYM I, the controller in each of the three preceding applications, is not a fully integrated system and contains no signal conditioning. As mentioned, it was basically a prototype version for the MACSYM II, which is a fully integrated system with signal conditioning, and is faster, smaller, and less expensive both in initial cost and in implementation (Fig 4).

In MACSYM II, conventional computer bus architecture is used for communication among processor, memory, and peripherals (Fig 5). A secondary bus, called the analog/digital input/output (ADIO) bus, interfaces to as many as 16 ADIO cards. Both buses are managed by an intelligent ADIO controller.

By splitting the system bus architecture in this manner, the ADIO controller is the only element in the measurement and control group connected to the processor bus, and is the only card which must carry the hardware overhead associated with interfacing to a processor. As a result, the ADIO cards carry little or no overhead for the ADIO bus. In addition, the ADIO controller contains all elements necessary to perform A-D data conversion, sharing this resource among the various ADIO cards in the system. Also, because the ADIO bus is isolated from the high speed, noisy processor bus, greater accuracy with low level analog signals are obtained.

The manufacturer says that these three advantages result in reduced size, complexity, and cost of ADIO cards and optimize architecture with respect to speed and signal conditioning requirements of measurement and control systems.

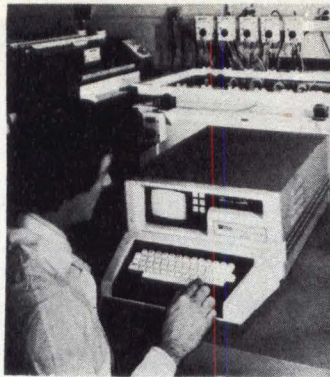


Fig 4 MACSYM II controller in simulated control system

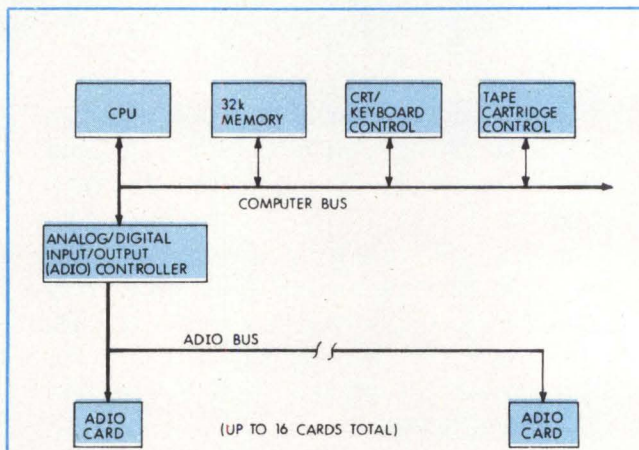


Fig 5 Diagram of MACSYM II split bus architecture. Computer bus interfaces to processor, memory, and peripherals; ADIO bus communicates with individual sensors via I/O cards

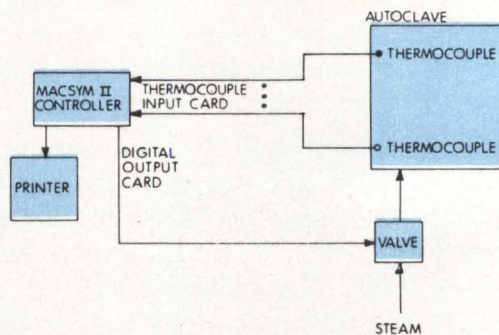


Fig 6 Configuration of MACSYM II controller system as possible replacement for system in Fig 3. Signal conditioning is accomplished in controller, eliminating need for data logger, and integral data cartridge negates need for floppy disc subsystem

As an example of the improvements inherent to the MACSYM II controller, if it were used in the previously discussed autoclave application, the data logger could be eliminated and the floppy disc subsystem could be replaced by an integral data cartridge subsystem. In this case, the thermocouples could be connected directly to thermocouple input cards (Fig 6).

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Now, for the first time, you don't need an expansion box or special back planes. DMAX/16 consists of two hex boards which install easily into standard SPC slots and connect to the current loop or EIA/RS-232 panel by separate flat-ribbon cable. As many as 16 units can be placed on a single PDP-11 for a total of up to 256 lines. A DMUX/16™ option allows modem control for 16 channels.

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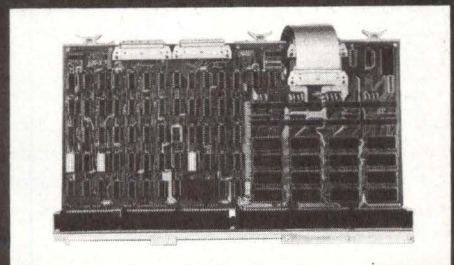
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CIRCLE 28 ON INQUIRY CARD

Control Computer System Dedicated to Petroleum/Chemical Processing

Designed specifically for control and management functions in the petroleum, petrochemical, and chemical industries, the Optrol 7000 process computer system is described as an online process engineering tool. Both hardware and software are configured for ease of initial operation according to Applied Automation, Inc, Pawhuska Rd, Bartlesville, OK 74004.

Basic hardware consists of a 32-bit word length digital computer with from 256k up to 1M bytes of directly addressable core memory, a 10M-byte disc, a microprocessor controlled process operator's console (CRT display system), a system console, and process I/O equipment. As many as 248 local I/O units can be connected to the control system in any combination and remote process I/O units are also available. Each local unit can control as many as 15 channels of up to 16 analog, 16 pulse, and 256 digital inputs or outputs plus one remote unit party line.

PROFORM realtime operating software supports as many as 16 process operator's consoles. Engineering functions supported include system generation, data base building, process calculations, report building, control implementation, system modifications, system documentation, and data collection.

Circle 161 on Inquiry Card

I/O System Saves Main Computer Time By Collecting and Preprocessing Data

MODACS III, made up of a Classic 7810 computer, communications link, direct memory processor, I/O controller, and connectors for digital and analog I/O interfaces, is said to expand the data acquisition function beyond ordinary I/O capabilities and save CPU time. Rather than merely collecting and transmitting signals, it collects and manipulates the data, and then transmits the results, thereby relieving the main computer of some duties.

Basic configuration of the system from Modular Computer Systems Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33309 is a standard 19" (48-cm) rack-mountable card file with power supplies. Four card positions are provided for CPU, controller, and communications link. User-specified process I/O modules fit into another 16 positions.

Each controller can drive up to 4 card files, each with 16 option cards, providing a grand total of 2048 control points. I/O variables are transferred to and from the CPU memory via the direct memory processor at rates up to 100,000 words/s. Since, in operation, the only time software intervention is required is to start

and stop the block transfer of data, a memory resident data base can be set up and maintained with minimum software. However tasks can access the process I/O through the data base.

Almost any combination of digital and contact inputs and outputs can be handled, including level analog input needs at rates of up to 30,000 samples/s within ± 10 -, ± 5 -, ± 2 -, or ± 1 -V signal ranges. A converter decides which gain is best suited for the input and automatically scales the converted value in the data word.

Circle 162 on Inquiry Card

Microcomputer Meets Needs for Small Process Control Applications

Superkim, a single-board microcomputer control system from Microproducts, 1024 17th St, Hermosa Beach, CA 90254, meets the requirements for applications such as manufacturing or production line automation, automatic machine tool operation, or realtime data collection. It is compatible with all KIM-1 software and most KIM-1 and Apple II hardware interfaces. TTY, RS-232, and cassette interfaces are included. Eight latched priority interrupts are individually resettable under software control.

Other features include 1k bytes of RAM with sockets for additional 3k bytes, 2k-byte ROM monitor, sockets for 8k or 16k bytes of EPROM, power-on reset, 5-V regulator, and eight counter timers. The I/O structure can handle eight 8-bit ADCs and nine 8-bit I/O ports.

Circle 163 on Inquiry Card

Interface Board Couples Image Sensor Cameras to Microcomputer Systems

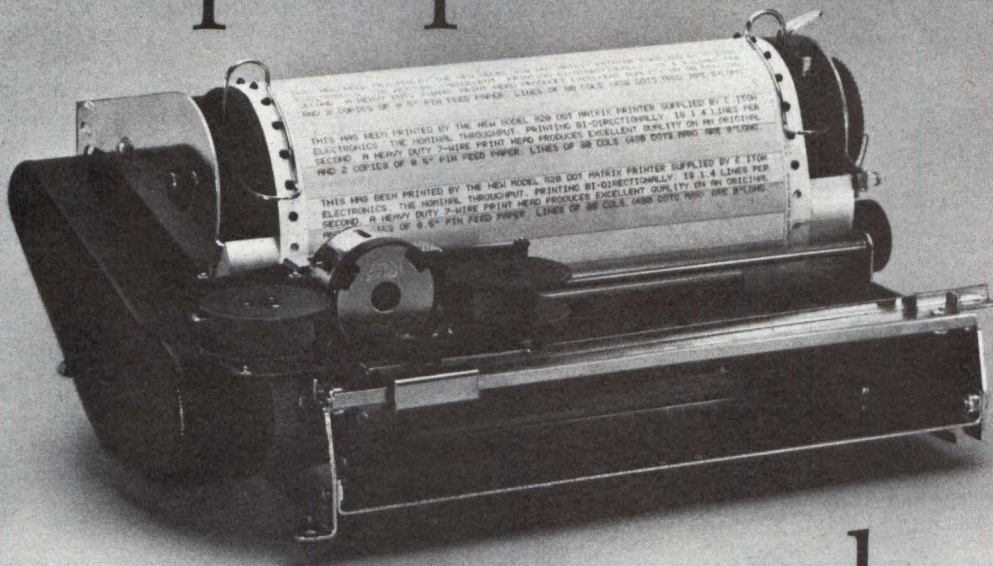
Multibus compatible circuit board model RSB-6020 inputs serial digital data from one or two photodiode array cameras and preprocesses the data for use with Intel SBC80 microcomputer systems. The single board camera interfaces, introduced by Reticon Corp, 910 Benicia Ave, Sunnyvale, CA 94086 for use with its cameras, plugs directly into the microcomputer system. It allows a full range of microcomputer control power to be applied to sensor signals in real time.

One preprocessing mode permits storing the address of each optical transition for one complete line scan; a second mode stores the number of diodes in each transition group. Preprocessed data are then stored in two 512-byte onboard RAMs. While data from a camera scan are being loaded in real time into one memory, the data in the alternate memory from the previous scan can be accessed by the system CPU. A toggling scheme is used to process all camera scans, without interruptions, at pixel rates of up to 2 MHz.

Data, written into the memories in 16-bit format, are available to the microprocessor system in 8-bit format for ease of processing. The board also furnishes interrupt signals at the end of each camera scan as well as complete handshaking protocol for asynchronous operation with the microcomputer system. Software listing is provided for operation of the interface with SBC80/05, /10A, and /20 single-board computers.

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CIRCLE 40 ON INQUIRY CARD

Measurement/Control Processor Gains Extended Data Acquisition Capabilities

Three optional capabilities for the HP 2240A measurement and control processor manufactured by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304 extend performance of the microprocessor based analog/digital subsystem. This option consists of a ROM set that replaces the processor's standard measurement and control firmware. Seven added programming commands provide the added capabilities plus other programming conveniences.

Now the processor can transmit acquired analog and digital data continuously to an associated computer at a rate of 10,000 readings/s at the same time that the computer is performing other work. Processor intelligence effectively decouples measurement tasks from the computer's computational tasks and minimizes the communications overhead when continuously repeating a measurement task to acquire large amounts of data from sensors.

History data acquisition enables the processor to acquire data and then discard them if an unpredictable but critical event does not occur. However, whenever the event does occur data leading up to the event, and possibly after it, can be recovered. The data, which can

be any mix of analog, digital, or counter inputs, can be used for analysis and correlation and may detail why the critical event occurred. Only the latest data are retained.

An If-Then programming format eliminates the need for computer intervention to alter task execution when a change is sensed in the state of the process, machinery, or apparatus under test. The processor can close a process or machine control loop independently of the computer when quick response is required to realtime changes in the application.

Circle 165 on Inquiry Card

Industrial Processor/Console Board Is User Oriented

Key components of the INMOD-885 processor/console circuit board include 3-MHz 8085A microprocessor, 2k-byte EPROM monitor, 20-digit keyboard, and 8-digit prompting hexadecimal display. The S-100 compatible board, from Industrial Modules, Inc, PO Box 2985, Santa Clara, CA 95051, also includes 256 bytes of RAM and can accommodate another 4k bytes of EPROM.

In addition to the usual I/O functions, the conversational monitor provides memory protect and debugging aids. The number of instructions to be executed before control is returned to the monitor can be defined by a Multi-Step hardware implemented function, while Multi-Break allows a breakpoint for any address combination to be defined. □

Circle 166 on Inquiry Card

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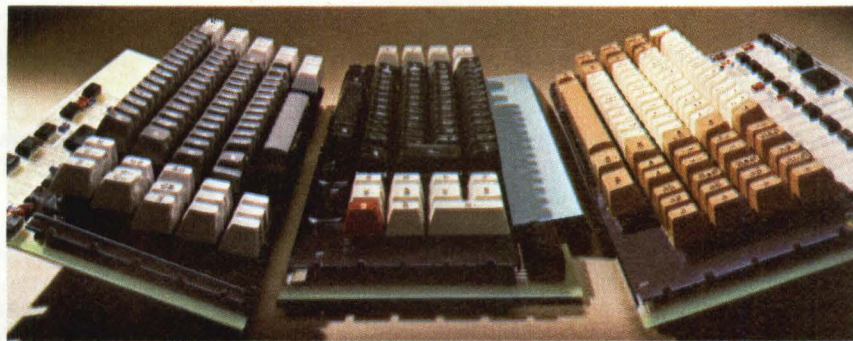
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Introducing Series III SOLID STATE KEYBOARDS

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operational and environmental conditions. This means cost efficiency for you—reduced downtime, lower repair cost, fewer service calls, satisfied customers, and lower prices. That's total value!

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IECI '79

Philadelphia Sheraton Hotel
Philadelphia, Pennsylvania

March 19-20



Harry W. Mergler
General Chairman



Paul M. Russo
Technical Program



William C. Hittinger
Keynote Speaker

The fifth annual IECI conference and exhibit will be a forum for the dissemination of recent industrial and control applications of microprocessors. Sponsored by the IEEE Industrial Electronic and Control Instrumentation Society, the conference will feature 80 papers from industry and university in 16 program sessions. Authors from Japan, Canada, England, France, India, Mexico, and The Netherlands, as well as the U.S., will discuss topics including microprocessor controls for industrial steelmaking, turbine steam reheat, sun-following mount for solar photovoltaic energy planning, constant current, thyristor converters, and industrial positioning.

The first of three panel sessions is scheduled for Monday evening. Chaired by V. Huang of Bell Laboratories, this session will focus on the impacts new developments in microprocessors will have on the ongoing 8- vs 16-bit debate. A second evening panel on software development and high level language,

chaired by W. Bennett of Virginia Polytechnic Institute and State University, will be held Tuesday evening. The ongoing international developments of VIEW-DATA-like systems is the subject of a special panel session tentatively scheduled for 9-11:30 Tuesday morning.

A keynote address by William C. Hittinger, Executive Vice President, Research and Development, RCA Corp, will highlight the Awards Luncheon on Tuesday. This year's General Chairman is Harry W. Mergler, Case Western Reserve University; responsible for the technical program is Paul M. Russo, RCA Laboratories.

Preconference registration is \$75 members, \$85 non-members, and \$20 students for the full conference, and \$40 for one day only. Registration at the conference is \$85, \$95, \$20, and \$50, respectively.

Details on the technical program that follows are limited to information available at press time.

Technical Program

Monday Morning

Session I

9-11:30 am

Power Systems

Chairman: V. F. Rajagaopalan, Universite du Quebec a Trois-Rivieres, Canada

"A Direct Digital Control of a Three-Phase Six-Pulse Cycloconverter Using a Microprocessor," T. Fukao and H. Akagi, Tokyo Institute of Technology; and S. Miyairi, Tokyo Denki University, Japan

"Direct Digital Control by Microprocessor of a Dual ac-dc Thyristor Converter," G. Rooy and A. Ouamar, L'Ecole Nationale Supérieure d'Electricite et de Mechanique, France

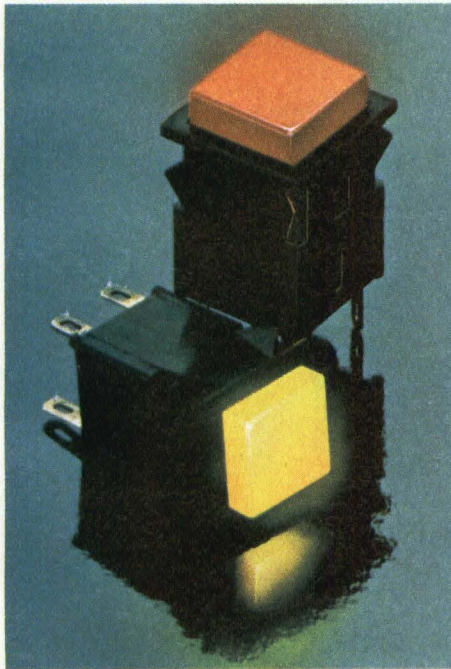
"Application for Measurements and Analysis of Quenching Phenomena of Power Circuit Breakers," Y. Miyazaki, Toshiba Corp, Japan

"A 'Lookup' Table Based Microprocessor Controller for a Three Phase PWM Inverter," E. Dwyer and B. T. Ooi, McGill University, Canada

"A Microprocessor Based, Waveform-Insensitive, Linear-Output Thyristor Controller," M. B. Broughton and J. D. Wilson, Royal Military College of Canada

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05 Series LPB's fit .625 square panel hole size; accept low cost T 1 $\frac{3}{4}$ wedge base lamp. Relamp from front panel. 1 Amp., 125 VAC rating. Compatible L.E.D. version complete with L.E.D. display lens.

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No wonder the K100-D is our fastest selling new logic analyzer ever. It gives you 16 channels, 1024 word memory, clock rates up to 100 MHz, signal timing resolution to 10ns-plus a built-in display and keyboard control.

Biomation's K100-D puts it all right at your fingertips — more performance and features than any logic analyzer ever.

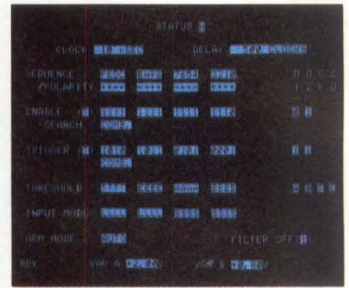


It starts with the micro-processor-controlled keyboard and interactive video display. To give you fast, precise control, the display serves as a comprehensive control status menu, with all selectable parameters in reverse video. There's a single, labelled key for each function, corresponding directly to status display choices. So guesswork is eliminated.

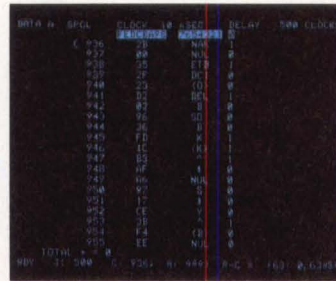
For example, in the data domain, you can direct the display to read in hexadecimal, octal, binary or ASCII, or any combination, by selecting one of four control buttons. There's also a unique "sequence" key that enables you to rearrange the order in which channels are displayed, to aid in data decoding, to simplify side-by-side comparison of timing signals and to enable you to cancel any channels you're not interested in seeing. A separate key controls horizontal expansion.

That gives you an idea of the K100-D's display versatility. Here's a picture of its astounding capture capability.

By providing timing analysis of signals as fast as 100 MHz, you can capture logic signals with resolution to 10ns. And the 100 MHz clock rate protects against obsolescence as the speed of your systems gets faster and faster. The K100-D also has a latch mode that can capture glitches as narrow as 5ns.



With the 32-channel input adapter, the K100-D is ideal for exploring the new world of 16-bit microprocessors. To give you unprecedented analysis capability, there's a built-in Auto Stop capability you can use to detect, record and display any match (or mismatch) between incoming data and previously recorded data held in a reference mem-



ory. Or using Search Mode you can key in a specific word and the K100-D will find it in memory.

To get the full impact of the K100-D, you really do need to have it at your fingertips. That's why we would like to arrange a demonstration. Call us at (408) 988-6800. Or, for

more information, write: Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050.



CIRCLE 45 FOR INFORMATION



Session 2

9-11:30 am

Process Control

Chairman: G. Cook, University of Virginia

"Microprocessor Control for Industrial Steelmaking *Hot Shop*," D. L. Browne, Kaiser Engineers, Inc

"Microprocessor Controls for Turbine Reheat Steam Temperature," J. M. Bukowski and F. Behringer, Westinghouse Electric Co

"A Microprocessor Torque Computer for Gas Turbines," C. J. Rubis, Propulsion Dynamics; and C. R. Westgate and K.-L. Li, Johns Hopkins University

"Automated Liquid Phase Epitaxy Growth System," T. Sakata, *et al*, Nippon Electric Co, Japan"Microprocessor Application in System Identification," S. S. Sengupta, *et al*, Indian Institute of Technology, India**Session 3**

9-11:30 am

Data Acquisition

Chairman: J. King, Digital Equipment Corp

"A Microprocessor Based Data Acquisition System," D. A. Townzen, Kaye Instruments, Inc

"Remote Collection of Analytical Instrument Data," L. Grim, Oxford, Pa

"Microprocessor Based Conversion Unit," P. J. Griffin, Honeywell, Inc

"A Microprocessor Based SCADA Communications Controller," D. E. Woods, Pennsylvania Power & Light Co

"A Microprocessor Based, Low Power, Data Acquisition System," M. S. P. Lucas and G. L. Johnson, Kansas State University

Monday Afternoon**Session 4**

2-4:30 pm

Energy Systems

Chairman: F. Harishima, University of Tokyo

"Multi-Microprocessor Applied SCADA System for Electric Power Systems," S. Ryusawa, *et al*, Toshiba Corp, Japan"A Microprocessor-Controlled Autonomous Sun-Following Mount for Solar Photovoltaic Energy Planning," C. H. Much, *et al*, MIT, Lincoln Laboratory

"A Multiple Input Residential Power Consumption Monitor," I. H. Thomae and W. Taylor, Thayer School of Engineering

"Microprocessor Assisted Check Synchronizing," A. K. Ghai, *et al*, University of Roorkee, India

"A Microcomputer Controlled Residential Energy Conservation System," S. K. Kavuru and H. W. Mergler, Case Western Reserve University

Session 5

2-4:30 pm

Control Applications

Chairman: P. Fasang, University of Portland

"Cogeneration with Utility Demand Control Employing Error Adaptive Techniques," C. W. Ross, Leeds & Northrup Co

"A New Approach to the Constant Current Control by a Microprocessor," N. Matsui and Y. Tsunehiro, Nagoya Institute of Technology; and A. Nagai, Nagoya Dengen-shan Ltd, Japan

"A Microprocessor Based Resistance Welder," K. Hyodo, Toshiba Corp, Japan

"Unloader Control System Using Microcontroller," M. Araki, Toshiba Corp, Japan

"Microprocessor Energy Controllers for Navy Buildings," R. I. Staab and D. Shiroma, Navy Civil Engineering Laboratory

Session 6

2-4:30 pm

Intelligent Instruments

Chairmen: E. Ohno, Mitsubishi Electric Co, Japan; and P. C. Sen, Queens University, Canada

"A Microprocessor Based Instrument for Particle Size Measurement," G. J. Pfisterer, Leeds & Northrup Co

"A General Purpose IEEE-488 Bus Interface," S. M. Babb, *et al*, Kansas State University

"Wind Instrumentation with Microprocessors," S. M. Babb, and G. Johnson, Kansas State University

"Performance Enhancement of a Heat Stress Monitor Using a Microprocessor," D. J. McCormick, Reuter Stokes

"A Programmable Waveform Controller," H. T. Yeh, Oak Ridge National Laboratory

Monday Evening**Panel Session 1**

7-8:30 pm

8- and 16-Bit Microprocessors

Chairman: V. Huang, Bell Laboratories

Tuesday Morning**Session 7**

9-11:30 am

Distributed Systems

Chairman: C. Westgate, The Johns Hopkins University

"A Distributed Microprocessor Control System for a Continuous Fabrication Process," D. F. Baker, *et al*, McDonnell Douglas Astronautics Co

"HelioStat Controller," D. B. Wecker, Carnegie Mellon Institute of Research; and G. Mutone, Westinghouse Electric Corp

"Processor for the Cinematics of Various Machines," T. Bennani, Ecole Supérieure d'Electricité, France

"A Hierarchically Distributed Energy Management System," C. J. Tavora, University of Houston

"The Cotton-Picking Approach to Computer Systems Development: Parallelization of System Development by the Isolation of System Function with Autonomous Microcomputers," B. Astle, *et al*, RCA Laboratories**Session 8**

9-11:30 am

Industrial Control Products and Applications

Chairman: R. Born, Cutler-Hammer Corp

"A Microprocessor Based Compressed Air Supply System," N. Iwama and Y. Inaguma, Toyota Central Research & Development Labs, Inc; and S. Kuroiwa and M. Watanabe, Toyota Motor Co, Ltd, Japan

"A High Performance Rugged Microcomputer for Industrial and Process Control," M. Kausch, *et al*, Cromemco, Inc

"Microprocessor Controls for Power Plant Feed Pump Turbines," M. Norman, Westinghouse Electric Co

"Punched Tape-to-Diskette Transcriber: A Case Study in Microprocessor System Development," I.H. Thomae and B. C. Nourse II, Thayer School of Engineering

"Servo Application of a Microprocessor Based Stepper Motor Controller," R. E. Boucher, Stanford University

"Front Panel Programmable Multitask Sequential Controller," L. Reiss, Poland

Special Panel Session

9-11:30 am

VIEWDATA-Like Systems

Chairman: W. J. Ginn, University of Essex, England

Tuesday Afternoon**Session 9**

2-4:30 pm

Consumer and Automotive Systems

Chairman: R. Sherman, Ford Motor Co

"A Small Viewdata Centre," W. J. Ginn and F. P. Coakley, University of Essex, England

"An Universal CMOS Controller for Washing Machines," B. Kete-laars and P. Tharma, N. V. Philips, Holland

"A Modern Day Wine Dispensing System," R. W. Baker, Silverman Associates

"Application of Microprocessors to Converting a Manual Automotive Transmission to Automatic Transmission," S.-H. Chung, General Electric Co

"Microprocessor Based Engine Dynamometer Data Acquisition System," W. Diehl and W. Reynolds, Bendix

Session 10

2-4:30 pm

Automated Manufacturing and Numerical Control

Chairmen: T. Hasegawa, Toshiba Corp, Japan; and P. C. Sen, Queens University, Canada

"A μ C-Less Servo System Using a Microprocessor," H. Maruyama, *et al*, Mitsubishi Electric Corp, Japan

"A Microprocessor Based Control System for On-Line Color-Intensity Measurement," K. Yamaguchi and F. Harashima, Institute of Industrial Science; and H. Naruto and T. Kishii, Kyoritsu-Dengyo Co, Japan

"IBM Series/1 Numeric Control by Positioning System (NCRY)," S. P. Casto, IBM Corp

"Microprocessor Based Control for Cigarette Makers," P. Vlahutin, Industrial Nucleonics Corp

"Wafer Slicing with a Microprocessor Based Controller," D. Van Le, *et al*, RCA Laboratories

"General Purpose μ P Controlled Industrial Positioning System," K. R. D. Tracton, Concordia University, Canada

Tuesday Evening

Panel Session 2

7-8:30 pm

Software Development and High Level Languages

Chairman: W. Bennett, Virginia Polytechnic Institute and State University

Wednesday Morning

Session 11

9-11:30 am

Signal Processing

Chairman: T. Nagle, Auburn University

"A Minimal Z-80 Based Adaptive Digital Filter for Intruder Detection," D. Nickel and M. S. P. Lucas, Kansas State University

"Summary of New Industrial Application of a Microprocessor to Transmission Systems," M. Bernard, Ecole Supérieure d'Electricite, France

"Correlation Flow Measurement of a Cryogenic Fluid by Use of a Microprocessor," O. Tsukamoto, *et al*, Yokohama National University, Japan

"A Fixed Point FFT for a 16-Bit Microcomputer," E. E. Wallingford, Royal Military College, Canada; and A. A. Sarkady and H. M. Neustadt, USNA

"A Versatile Low-Cost On-Line Signal Processor Based on a 16-Bit Microcomputer," E. E. Wallingford, Royal Military College, Canada; and A. A. Sarkady and H. M. Neustadt, USNA

Session 12

9-11:30 am

Motor Control

Chairman: V. Stefanovic, Concordia University, Canada


"A Microcomputer Based Solid-State Direct-Current Controller," F. E. Acker, *et al*, U.S. Steel Corp

"A Microprocessor Based PLL Speed Control System of Converter-Fed Synchronous Motor," H. Taoka, *et al*, University of Tokyo, Japan

"Harmonic Elimination of Microprocessor Controlled PWM Inverter for Electric Traction," S. Sone and Y. Hori, University of Tokyo, Japan

"A Microprocessor Based Control System of Thyristor Converter Fed DC Motor Drives," T. Izumi, Fuji Electric Co, Ltd, Japan

"Digitally Controlled Thyristor Current Source," G. Olivier, *et al*, Concordia University, Canada

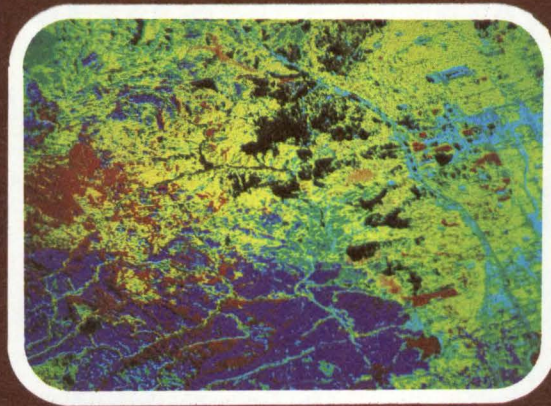


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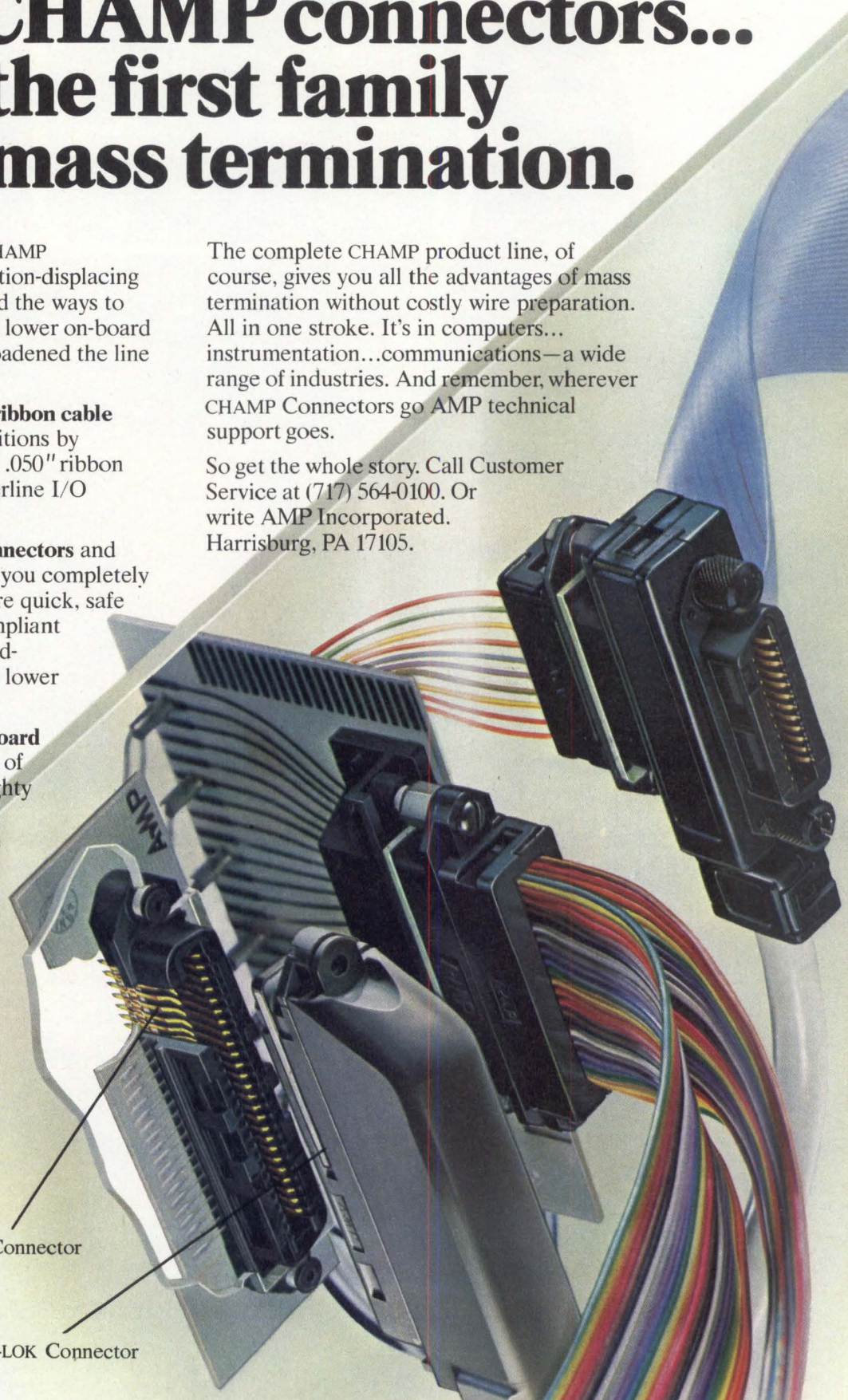
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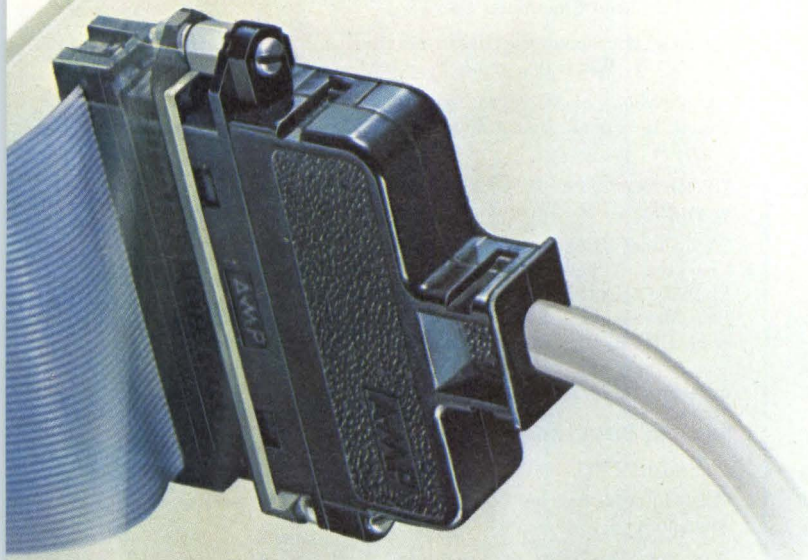
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CIRCLE 48 ON INQUIRY CARD

Automated Diagnosis and Testing

Chairman: S. Korin, IRM Corp

"The Development of Automatic Diagnostic System for Industrial Motors Using a Microprocessor," T. Usami, *et al*, Mitsubishi Electric Corp, Japan

"EC-1030 System Performance Evaluation by a Microprocessor Based Monitor," S. Rao, *et al*, Indian Institute of Technology, India

"Automation of Environmental Testing," G. A. Mathes, EMA, Inc; and D. R. Bloemke, Rosemount, Inc

"On-Line Statistical Analyzer for Production Testing and Quality Control," G. Minns and K. Kindberg

"Microcomputer-Controlled Potentiometer Test System," A. R. Marcantonio, RCA Laboratories

Wednesday Afternoon**Biomedical Applications**

Chairman: C. Einolf, Westinghouse Electric

"Recreational Boat Operator Performance Measurement Using Microprocessors," L. Kendrick, B & K Dynamics

"A Miniature Recording Cardiograph," P. J. Zsombor-Murray and L. J. Broomen, McGill University, Canada; and N. T. Hendricksen, Anher Engeliendsvej, Denmark

"Application of Microprocessors to Continuous Heart Rate Monitoring of High Risk Infants," S. Chung, General Electric Co; and P. W. Houck, Virginia Baptist Hospital

"Microprocessor Control of the Blood Flow Plethysmograph," W. E. Seiberling, *et al*, The University of Akron

"Medical Applications: Microprocessor Based EEG Biofeedback Training Unit for Epileptics," B. Keane and J. Henke, Clemson University

Monitoring and Control

Chairman: K. Goksel, Bell Telephone Laboratories

"Microprocessor Based Servo Control for Gunfire Control," B. P. Eng, Lockheed Electronics Co

"A New Microprocessor Based Monitoring System of Multi-Motor Drives," Y. Watanabe, *et al*, Toshiba Corp, Japan

"Applications of Microprocessor Based Programmable Logic Controller to Flying Shear Control," T. Funahashi, Toshiba Corp, Japan

"A Microcomputer Based Supervisory System for a Sewage Treatment Plant," M. Machida, *et al*, Toshiba Corp, Japan

"Acoustical Diagnostic Methods Using Histogram Analysis for Checking Nuclear Power Plant Components," Y. Hashimoto, Chugoku Electric Power Co; K. Kawai, Tokyo Electrical Power Co; M. Suzuki, Chubu Electric Power Co; and Y. Michiguchi, *et al*, Hitachi Ltd, Japan

System Development

Chairman: I. Thomae, Thayer School of Engineering

"List Interpreters for Microcontrollers," M. D. Maples, M & E Associates

"On the Simulation of Processes; A Hardwired Approach," E. Cristo Alvarez and L. M. Hernandez Ortega, Facultad de Ingenieria, UNAM, Mexico

"Adaptive Techniques; The Intelligent Approach on EPROM Programming" C. Chavez, Facultad de Ingenieria, UNAM, Mexico

"Problem Solving with the TMS 9940," K. S. Padda, Texas Instruments

"A Microprocessor Based Debugging Tool for an 8080 Microcomputer," R. S. Gottlieb, General Electric Co □

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Monday Afternoon

Defense Telecommunications

Organizer/Chairman: D. L. Solomon, Office of the Secretary of Defense

"AN/TRC-170—The Future in Tactical Tropospheric Scatter Communications," W. J. Connor, Communications Systems Directorate, Raytheon Corp

"Growth of Packet Switching Services in the U.S. Dept of Defense," D. O'Rourke, U.S. Civil Service Commission and M. Green, Information Spectrum, Inc

"Defense Satellite Communications: Lessons Learned and Future Directions," J. H. Babcock, Office of the Secretary of Defense

"Analog Digital Transition in Defense Networks," J. A. Kinahan, Page Communications Engineers, Inc

"Field Telephones/Field Terminals—A Generation Gap?" K. Johnsen and A. Bratlie, AS Elektrisk Bureau

International Network: Transnational Data Flow

Organizer/Chairman: G. R. Pipe, Transnational Data Report

"International Data Regulation Issues from the Perspective of the European Economic Community," E. F. M. Hogrebe, GDM Research Center

Panel Members: J. Freese, Swedish Data Inspection Board; D. Hebditch, Telecommunications Consultant; H. Donahue, Control Data Corp; W. Fisherman, NTIA; and E. F. M. Hogrebe, GDM Research Center

Tuesday Morning

Data Communications: Distributed Processing

Organizer: D. Doll, DMW Telecommunications Corp

Chairman: M. Dortch, The Yankee Group

"Considerations When Implementing a Distributed System," A. Lubitz, Raytheon Data Systems, Inc

"DP-100 Connected Speech Recognition System," S. Tsuruta, *et al*, Central Research Laboratory, Nippon Electric Co, Ltd

"Advent of the Electronic Office," D. Hosage, Datapoint Corp

"Distributed Processing and the Automated Office," D. Kutnick, The Yankee Group

"Definitions of Communications and Data Processing on an Entropy Basis," N. Seitz, NTIA

Wednesday Morning

Data Communications: Data Networks

Organizer/Chairman: D. Doll, DMW Telecommunications Corp

"Network Cost and Performance Optimization," F. E. Ferrante and M. M. Balagangadhar, Page Communications Engineers, Inc

"International Applications of TYMNET Technology," R. A. Bamberg, TYMNET, Inc

"A User's Perspective Toward Network Implementation," R. Techo, Georgia State University

"Development of Telecommunications—A Company Asset?" W. Brasuell, Fairchild Electronics, Inc

"XTEN—Ending the Information Float," W. Combs, Xerox Telecommunications Network Services, Inc

Data Communications: Peripherals and Interfacing

Organizer: D. Doll, DMW Telecommunications Corp

Chairman: B. F. Baldwin, ECI Div, E-Systems, Inc

"Current Developments in Teleprinter Technology," B. Baldwin, ECI Div, E-Systems, Inc

"Radio Data Terminal System," T. Miyawaki, VHF-UHF Communications Div, Nippon Electric Co, Ltd

"Application of Microprocessor Technology in Improving Vessel Traffic Systems," R. A. Pickens and A. G. Hamlin, Page Communications Engineers, Inc

"Linear Integrated Circuits Bring Telephones Up to Date," S. D'Arrigo, SGS-ATES, Agrate

INTELCOM 79, to be held in the Dallas Convention Center, is an international telecommunications exposition intended to present educational, business, and financial activities in the field. Included in the 5-day convention are exhibits and more than 200 application papers to be presented during 30 technical program sessions, 2 executive forums, and 10 mini-university seminars.

Telecommunications Mini-University

Ten intensive, 2-day seminars will comprise a telecommunications mini-university. Experts in the field will discuss the latest in telecommunications development, planning, marketing, and technology. Seminar topics include Computer Communications Concepts, Fiber Optics and Electro-Optics in Telecommunications, Hands-On Software and Interfacing Experiments with Microprocessors, Intelligent Terminals in Distributed Systems, and Distributed Processing and Data Communications. Seminars will be held from 8:30 to 11 am and from 2 to 5:30 pm.

Executive Forums

These forums are designed to offer a broad and upper-level appraisal of telecommunications issues, trends, and opportunities to communications customers, suppliers, technologists, and government, industry, and financial administrators. Each forum features a panel of telecommunications authorities.

Executive Forum A, held Tuesday through Friday, 9-11 am, will address topical issues challenging the industrialized world. Panel subjects are to include the Global Frequency Spectrum rewrite, the rewrite of the Communications Act of 1934, and changes made by specialized common carriers and reaction of the International Record Carriers.

Executive Forum B will profile telecommunications activities—past, present, and future—of the developing world in panel sessions to be held at 2 pm Monday through Thursday. Latin American, Africa, the Middle East, and Asia will each be addressed on separate days.

Pre-Conference Registration

Registration for exhibits only is \$15; for 1-day attendance of the technical sessions it is \$50. The \$120 fee for the full 5-day program includes exhibits, executive forums, and a copy of the published proceedings. \$295 Mini-University seminar fees include two complete days of instruction per course, detailed course notes, and admission to the exhibition and technical sessions.

Details on the technical program that follows are limited to information available at press time.

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Thursday Morning

Communications Privacy and Security: Computer and Facsimile Communications Security

Organizer/Chairman: D. K. Branstad, National Bureau of Standards

"Data Security Applications of the NBS Data Encryption Standard," R. Thorpe, Collins Telecommunications Products Div, Rockwell International

"Cryptography Application of The Data Encryption Standard," R. Lennon, Kingston Development Laboratories, IBM Corp

"Advanced Techniques in Network Security," D. Hillis, Secure Communications Electronics Div, Motorola, Inc

"Some System Implications of Data Communications Security," D. Abmayr, Datotek, Inc

Fiber Optics (1)

Organizer/Chairman: H. Elion, Arthur D. Little, Inc

"A Worldwide Survey of Operational Fiber Optical Systems," L. Bloom and R. Gallawa, National Telecommunications and Information Administration

"Optical Fiber Cable Transmission Equipment and Optical Device," Y. Ohashi, *et al*, Transmission Div, Nippon Electric Co, Ltd

"Fiber Optics—A Panacea for Telecommunications?" F. E. Ferrante, Page Communications Engineers, Inc

"Fiber Optic Trunk System for Analog Video Transmission," O. I. Szentesi, Siecor Optical Cables, Inc; E. Kuegler, Siemens AG; and W. D. Petty, Cablecom-General, Inc

Thursday Afternoon

Testing and Measurement: Datacomm (1)

Organizers/Chairmen: R. L. Allen and R. Coackley, Hewlett-Packard Co

"Remote Testing of Telephone Networks Used for Voice and Data Transmission," J. L. Kelly, Hekimian Laboratories, Inc

"Advances in the Centralized Testing of Remote, Unmanned Central Offices," R. E. Pospisil, Telecommunications Technology, Inc

"Centralized Diagnostics for Data Communications Systems," N. Kumar, Dynatech Data Systems

"Automated Signal Quality Monitoring vs Automatic Channel Quality Monitoring," N. W. Feldman, U.S. Army Communications Research and Development Command

Fiber Optics (2)

Organizer/Chairman: H. Elion, Arthur D. Little, Inc

"A T-3 Rate Fiber Optic System," C. A. Ebhardt, IRT Telecommunications

"Digital All Dielectric Links in the Telephone Plant," D. F. Hemmings and R. Jones, Harris Corp

"Optical Components and Application to an Optical Transmission System," S. Takeuchi, *et al*, Sumitomo Electric Industries, Ltd

Friday Morning

Fiber Optics (3)

Organizer/Chairman: H. Elion, Arthur D. Little, Inc

"Fiber Optical Cables for Telecommunications," R. L. Ohlhaber, *et al*, Technical Research Center, Belden Corp.

"Proof Testing of Optical Fibers—An Asset or a Liability?" S. T. Gulati, Corning Glass Works

"An Optical Fiber Digital Link Using a High Efficiency LED," M. Kawashima, *et al*, Transmission Div, Fujitsu, Ltd

"Avoiding Common Pitfalls in Optical Waveguide Measurements," P. R. Reitz and D. Charlton, Corning Glass Works

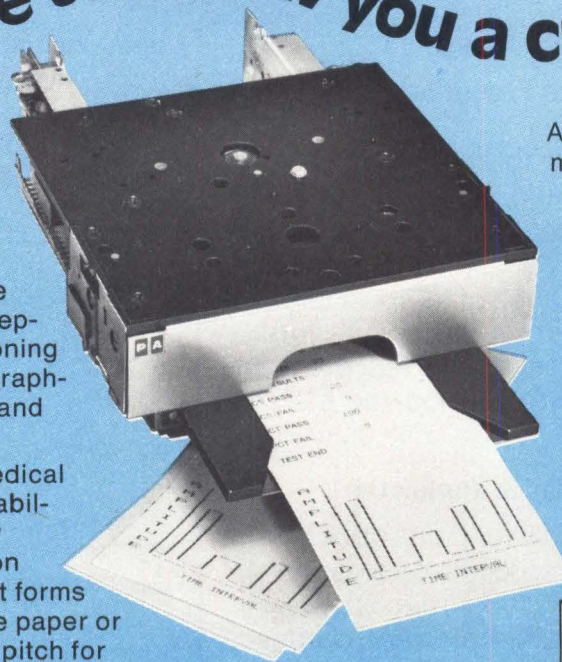
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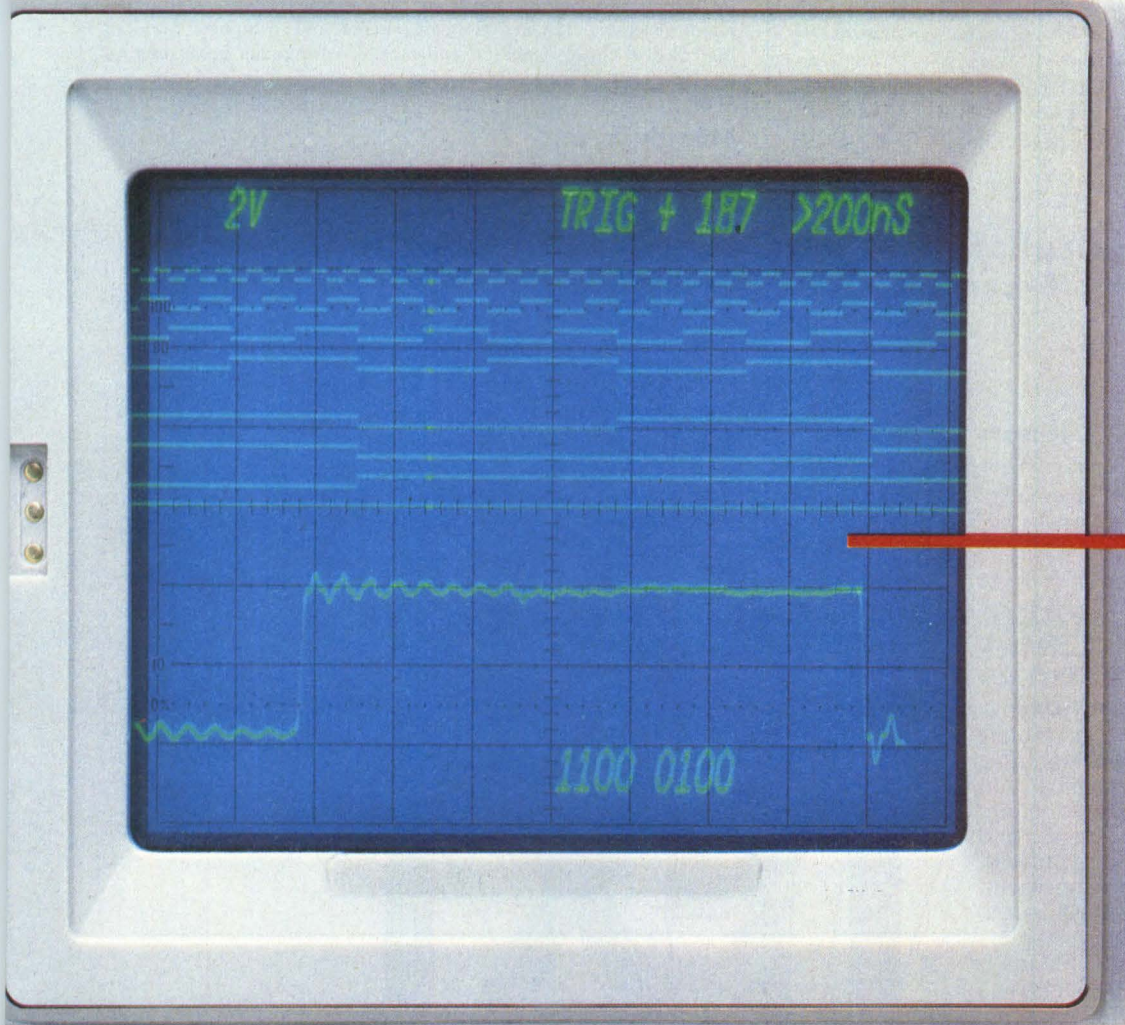


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Testing and Measurement: Datacomm (2)

Organizers/Chairmen: R. L. Allen and R. Coackley, Hewlett-Packard Co

"Data Communications Systems Users and Their Maintenance Requirements," J. L. Wallace, Atlantic Research Corp

"Maintenance of the United Airlines PARS System," M. Teflian, United Airlines

"Protocol Simulation—A New Side in Data Diagnostics," K. L. Damanda, Digitech Data Industries, Inc

Friday Afternoon

Fiber Optics (4)

Organizer/Chairman: H. Elion, Arthur D. Little, Inc

"Optical Fiber Communications for Broadcasting Applications," Y. Ueno, *et al*, Nippon Electric Co, Ltd

"T-3 Rate Fiber Optic Terminal Equipment," L. Campbell and D. Matthews, Digital Communications Corp

"Asynchronous Process Control Data and Links," C. H. Podlesny, Galileo Electro-Optics Corp

Telecommunications Mini-University Excerpts

February 27 and 28

Seminar 02

Computer Communications Concepts

Instructor: Carlos Laredo, Bell Canada International, Inc

Course covers types, functions and characteristics of all elements in data communications system; function and rationale for controls and protocol; and network appraisal and design evaluation

Seminar 04

Fiber Optics and Electro-Optics in Telecommunications

Instructors: Dr Herbert Elion, Arthur D. Little, Inc and Dr Glenn Elion, International Communications and Energy, Inc

Course designed for private, military, and educational communications personnel covers optical fibers and cables, couplers, connectors, and splices, modulation methods and light sources, and new devices and developments

Seminar 05

Hands-On Software Interfacing Experiments with Microprocessors

Instructor: Howard Boyet, Pratt Institute

Designed for telecommunications professionals, course starts with microprocessor digital logic components and computer architecture basics, covers machine and assembly language programming, and proceeds to hands-on storage and retrieval experiments

March 1 and 2

Seminar 06

Intelligent Terminals in Distributed Systems

Instructor: Arnold Kashar, Technogenics Group, Inc

Course details functions, parameters, and applications of intelligent terminals, and explores their role in distributed information processing

Seminar 12

Distributed Processing and Data Communications

Instructor: Daniel R. McGlynn, McGlynn Associates

Advantages, disadvantages and selection criteria for data communications/distributed network are outlined in course for computer analysts, data communications managers, and electrical engineers □

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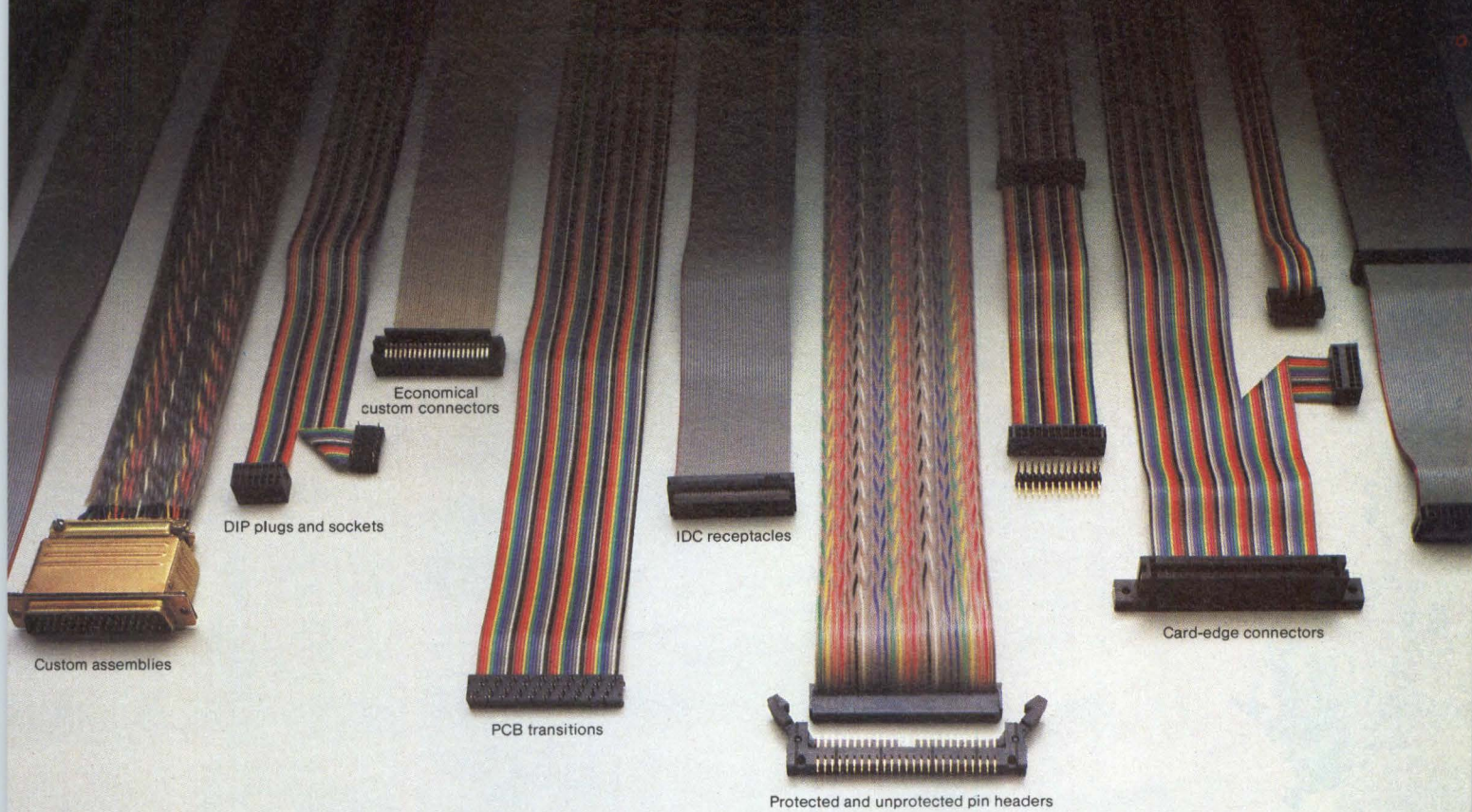
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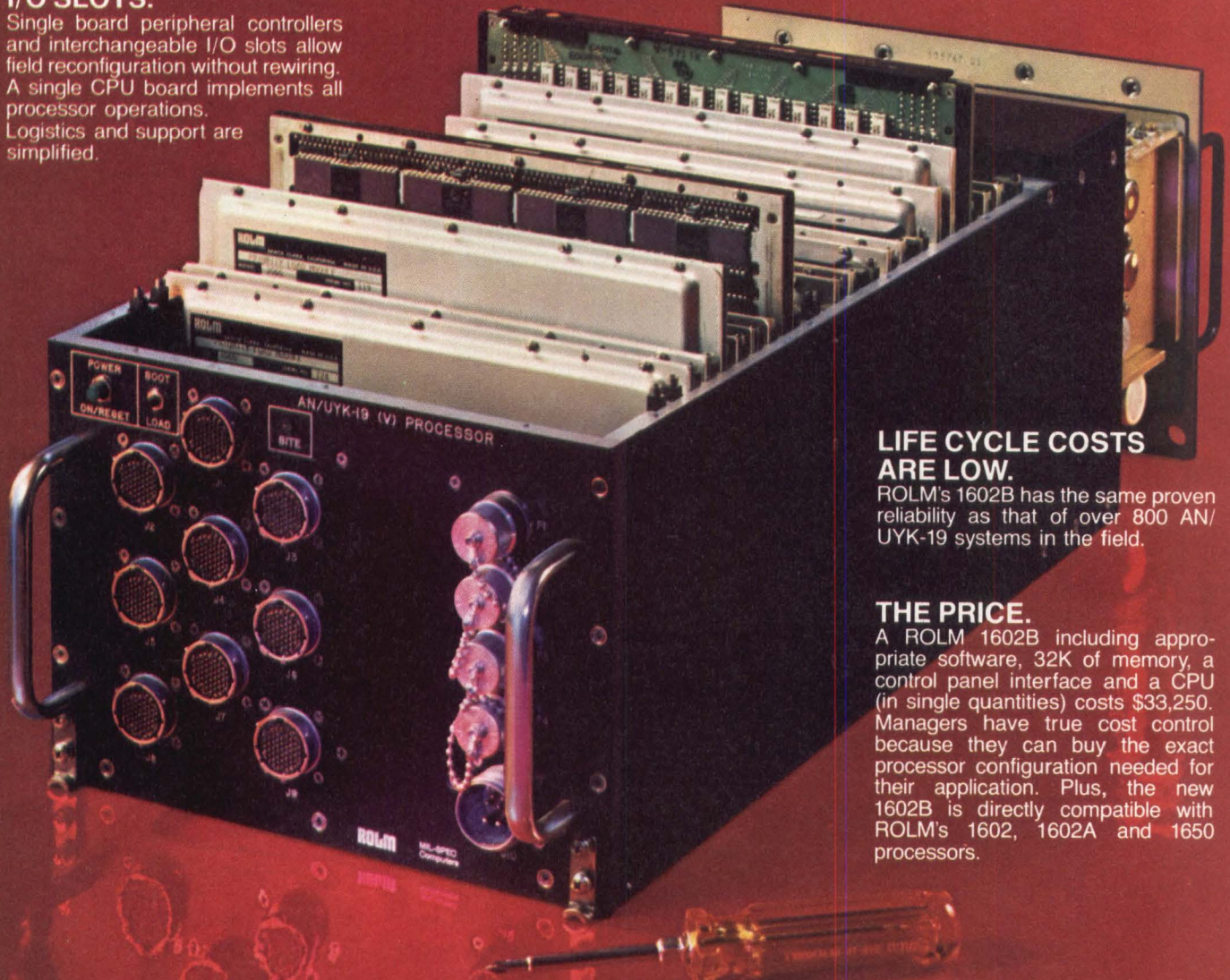
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CIRCLE 58 ON INQUIRY CARD

COMPARING MICROCOMPUTER DEVELOPMENT SYSTEM CAPABILITIES

Hardware and software integration difficulties during microprocessor based system design mandate use of microcomputer development systems with comparative processor support capabilities and software, and differing control consoles, memories, and in-circuit emulation architectures

Bruce E. Gladstone

Futuredata Computer Corporation, Los Angeles, California

Proliferation of microprocessor based products necessitated the design of microcomputer development systems. These tools represent either general purpose or universal investigative aids that support several microprocessor types, or dedicated aids restricted specifically to a single microprocessor type or family. A system assists the designer in evaluating alternative microcomputer hardware or software prototypes because it incorporates all standard computer development tools, such as the central processor, mass storage memory, control console, editor, assembler, and compiler. Also, simultaneously testing hardware and software produces powerful debugging capabilities (Fig 1).

Specialized in-circuit emulator types of microcomputer development systems evolved to handle problems inherent in separating hardware and software defects. These include the Futuredata Microemulator and Tektronix In-Prototype Emulator that support microprocessors from a variety of manufacturers, the Intel ICE and Motorola USE that support a family of microprocessors, and single-microprocessor systems from RCA, Rockwell, and Zilog. The in-circuit emulator provides the most accurate method for testing and checking microcomputer system hardware and software. It replaces the central processing unit (CPU) chip in the system under test, duplicates the chip functionally, and furnishes indications of system operation and control at a

console or terminal. The ability to examine, change, or modify CPU registers, storage memory, and program execution permits rapid and easy hardware and software testing.

Hardware Elements

A microcomputer development system consists of a series of hardware and software elements. Major hardware elements are the central processor, memory, mass storage, and control console (Fig 2). The central processor executes the various algorithms involved in the development task and, at times, executes an editor, an assembler, a debugger, and the designer's program. Thus, it performs two major functions: host and designer program execution.

Memory stores both program and data. These programs can be host programs, such as the editor or compiler, or designer programs. Data involve editor workspace, assembler symbol table, input and output (I/O) buffers, and/or data generated by the designer's program.

Mass storage stores operating programs, designer's programs, and either temporary or permanent data. It is sometimes used as an extension of main memory. For example, when editing a large program, the editor workspace may not be large enough to contain the entire

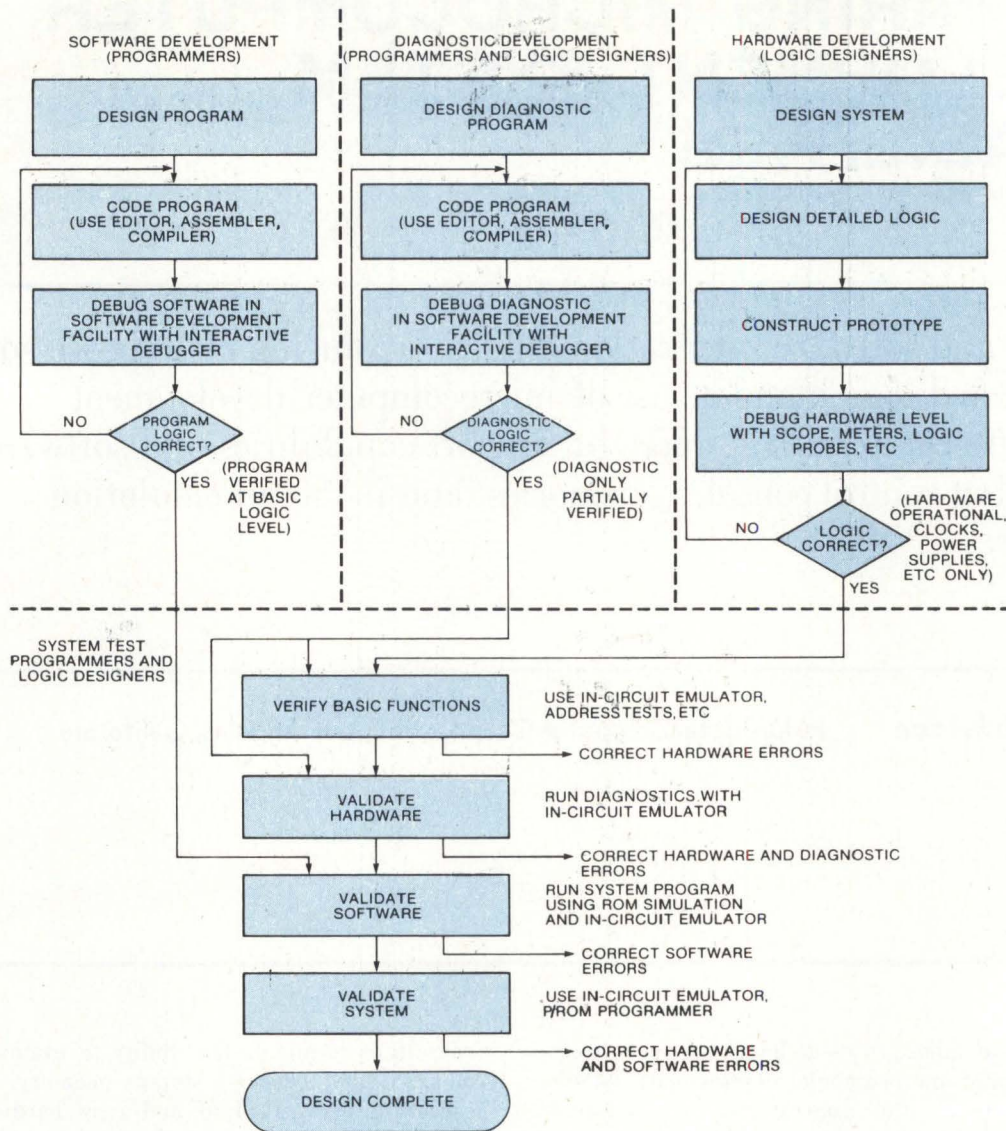


Fig 1 Microprocessor based system design with development system. Development of micro-computer based design involves preparation of application program, hardware design, diagnostic programming, and system test phase. Capability of development system is especially critical in latter, when it is necessary to sort out hardware versus software problems

program during edit. Moving the source program from one file in mass storage through the edit buffer to another file in mass storage accomplishes an edit. In this case, the two files and the editor work area comprise a very large memory space.

The control console provides an interface between the designer and the microcomputer development system. Systems differ greatly in the type of console used. Two primary functions of the console are to accept operator input (source programs, debugging commands, operating system commands, data) and to provide feedback and output to the operator (assembly listings, memory dumps, register displays).

Essentially, these four hardware elements also constitute a software development system, of which the Intellec 8 and Intellec 80 are examples. The next three hardware elements, however, relate to the hardware development aspect of microcomputer design and apply specifically to microcomputer development systems.

An in-circuit emulator provides a direct connection between the microcomputer development system and the prototype system. Read/write memory within the microcomputer development system simulates read-only memory (ROM) or programmable read-only memory (P/ROM) in the prototype system. This greatly reduces the time needed to change and correct designer programs. Some

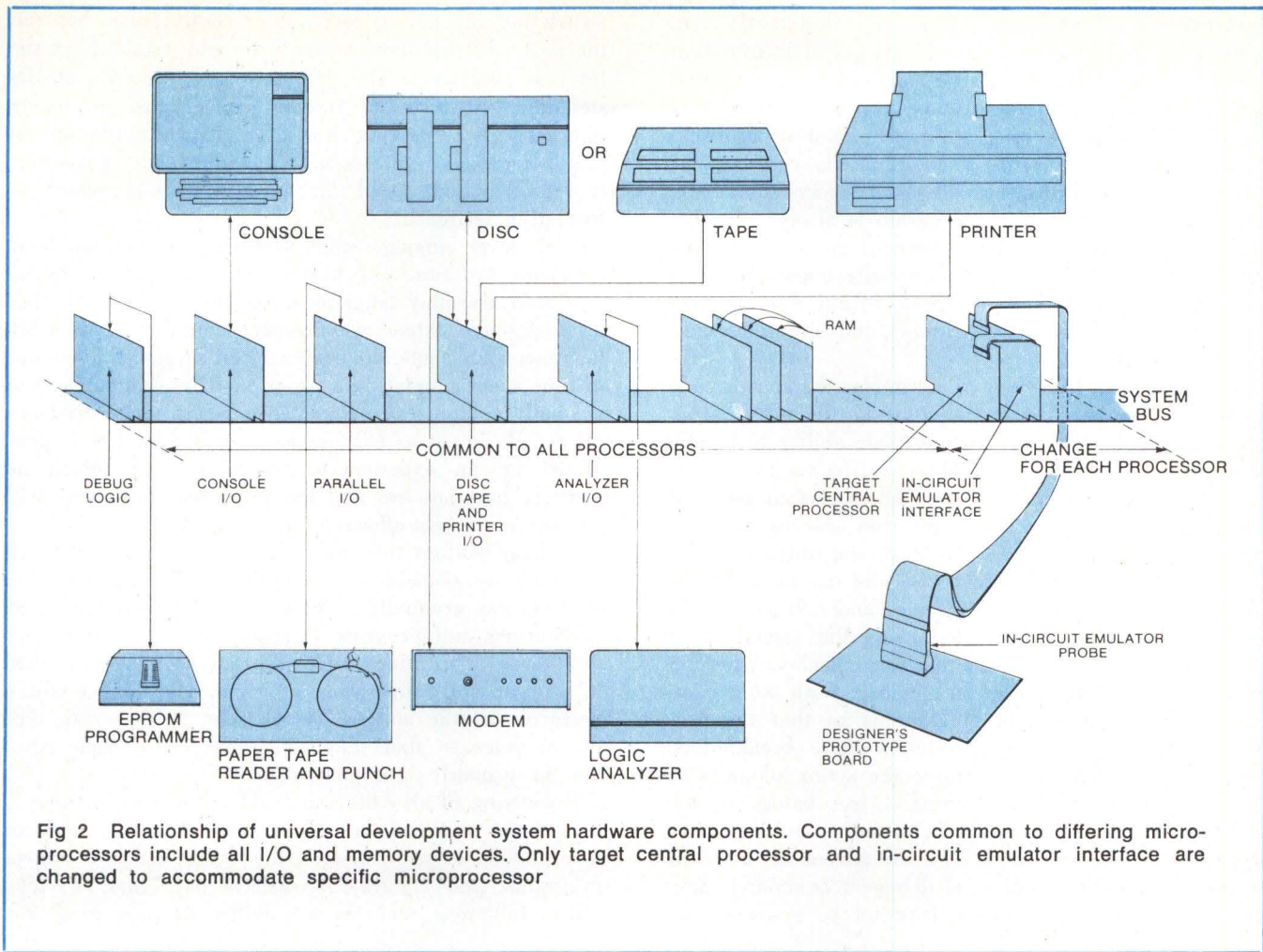


Fig 2 Relationship of universal development system hardware components. Components common to differing microprocessors include all I/O and memory devices. Only target central processor and in-circuit emulator interface are changed to accommodate specific microprocessor

in-circuit emulators allow the designer to gradually switch functions into the prototype system. Thus, the designer separately tests the clock circuits, input control lines, and direct memory access (DMA) control system to evolve the final design in discrete increments.

Final software can be stored in P/ROM using the P/ROM programmer. Programs debugged and running in simulator ROM are permanently burned into an electrically programmable ROM (EPROM) or P/ROM.

Hardware debug aids, used in the debugging process, separate hardware and software problems. These aids include a single-stepping facility, a hardware breakpoint facility, and a logic analyzer. With a single-step facility, the designer steps through the program one instruction at a time. A hardware breakpoint facility sets up a logical condition, usually an address, that halts the program whenever it encounters that address. Then, the designer can examine interim results, determine whether they are correct, and either continue executing the program or go back and modify it. In addition to providing hardware breakpoints, a logic analyzer captures data on the fly and displays it. Thus, the designer views the system's operation as a series of bus transactions. The logic analyzer has a fixed amount of storage that is continually updated by the last bus cycle, while the earliest bus cycle is erased. Therefore, when a hardware breakpoint is encountered, the logic analyzer memory shows events leading up to the breakpoint.

The microcomputer development system contains other I/O hardware elements. The printer provides hardcopy listings of the program, while other I/O devices, such as a paper tape reader, a punch, or a modem, provide a standardized interface into other systems for data interchange. Thus, with a paper tape reader and punch, a designer may write a program on one development system and communicate it to another development system. Likewise, with a modem, a designer connects a microcomputer development system by telephone lines to a large computer which may have other processing facilities available (cross-compilers, cross-assemblers, etc).

Software Elements

Integrated into a development system are an editor, assembler, debugger, high level language compilers, linkage editors, and operating system—all software components. The editor creates and modifies source programs, written in assembly language or in higher level languages, depending on the task. The editor must, of course, have editing commands to change, delete, and insert lines of code; positioning commands to target on a particular location in the program where changes are to be made; and utility commands to read and write edited data.

Editors differ in their capabilities and in their interactions with the control console. Most are written for

teletypewriter compatibility. To meet this design criterion, editors are designed with a small amount of information feedback. More recent designs use ultra high speed cathode-ray tube (CRT) displays to provide context based editing and to offer a large amount of information feedback. A context based editor is very similar to the editors used in CRT word processor systems; here, a significant amount of the program is always "on display." A cursor within the display or context performs the editing; all changes instantaneously update the program as displayed. This feedback within the program context substantially reduces errors and simplifies editing commands.

The assembler translates or assembles the source code (assembly language), generated using the editor, into object code. Assemblers differ in their ability to handle macros, to generate relocatable code, to support a variety of operand formats, and to allow certain types of pseudo-instructions. The designer uses macros to name commonly used sequences of instructions, which then are "called" with a single instruction—the macro name.

A debugger interactively executes and debugs the object program that is generated using the assembler or compiler. Commands handle memory display, program execution, and data storage in memory. With other commands, the designer sets breakpoints so that the program will halt when it encounters these breakpoints. Thus, the designer can determine the action of parts of the program. Additional commands set values in the processor registers, find data in memory, and read and write object program files. With the advent of in-circuit emulator capability, additional debugger commands map memory between the host and prototype systems, and

switch the various microcomputer control lines between the host and prototype systems, thereby establishing the level of emulation. The debugger also provides single-stepping and program tracing. Since most debuggers interact with a teletypewriter, they provide minimum operator feedback. New debugger designs take advantage of the ultra high speed CRT displays with increased information feedback.

High level language compilers translate a high level language program (in BASIC, FORTRAN, COBOL, PL/M, etc) into assembly language programs. Since each high level language statement represents a number of assembly language statements, the designer can shorten the amount of time spent generating a program. This time advantage normally contains an associated expense, since the compiled code is not as efficient as assembly level code generated by an experienced programmer; however, as memory becomes less and less expensive, compilers will become more cost-effective.

Linkage editors link individual program modules, all of which are assembled or compiled separately. Thus, the designer can gradually build a library of commonly used subroutines and program segments and, as a last step, link these subroutines and program segments together to form an entire operating program. The linkage editor performs all the address calculations necessary to link the modules so that they can interface to each other and fit properly into memory.

Consisting of an editor, assembler, monitor, debugger, compilers, and linkage editors, the operating system manipulates, stores, retrieves, loads, and executes system programs, and creates and deletes data files. Various utility functions, such as the ability to copy programs

TABLE 1
Operator Console Types and Major Function Times

<u>Operator Console</u>	<u>Application Example</u>	<u>Debug Function Time¹ (Overhead)</u>	<u>Edit Function Time²</u>
Binary lamps and switches	Front panel; Imsai and Altair computers; DEC PDP-11	10 min	Not practical
Hexadecimal keyboard and display	Intel SDK-85; KIM-1	180 s	Not practical
Printer terminal with P/ROM debug monitor	Motorola EXORciser with Exbug, and T1 Silent 700 terminal	120 s; includes time to write results; printing time is significant	480 s; must re-list to check edit
CRT terminal—120 to 960 char/s—and debug monitor	Intel MDS with Intel CRT terminal; Tektronix 8002 with CRT terminal	80 s	240 s; must re-list to check edit
Memory refreshed CRT display	Futuredata Microsystems 10, 15, 20, and 30	40 s; minimum operator entry	90 s; context editing

¹Standard debug example: set breakpoint, execute, examine register and 32 bytes of memory, make a 5-instruction patch, re-execute, examine registers, and continue execution.

²Standard edit example: change two lines, delete three lines, and insert five lines. Assume that all data are in memory.

either in source or object form from one media to another, also are offered.

The mass storage device attached to the system, such as paper tape, magnetic tape, and disc, principally differentiate the various levels of the overall operating systems.

Operator Console Levels

Microcomputer development systems differ primarily in two hardware areas: the operator control console, and the type and speed of mass storage devices. Table 1 shows five levels of operator control consoles. Early operator consoles contained binary lamps and switches. Even today, most minicomputers have a front panel containing a row of toggle switches and a row of lamps. Manual loading of an initial program is common practice with these front panel switches. A bootstrap program inputs a more sophisticated loader through a paper tape reader and, finally, that loader program loads in the designer or system program, again from the teletypewriter paper tape reader. Interaction with an operating program for debugging can also be done with panel lamps and switches. Obviously, this manual debugging method is tedious, evolving, as a result, many modifications to operator consoles.

The first improvement added a printer terminal with debugger. Debuggers written around this terminal type provided a minimal response to each command since printer terminals were relatively slow (data rates of 10 to 30 char/s). Each command deliberately limits information; otherwise, the designer continually would be waiting for the terminal to finish printing the results of the last command. This in turn led to two further improvements: one in the direction of less cost (hexadecimal keyboard and display) and the other in the direction of higher performance (CRT terminal).

The hexadecimal keyboard and display are inexpensive methods of implementing an operator console. Information previously entered with switches and displayed with binary lamps is now entered with a hexadecimal keypad and shown on 7-segment light emitting diode displays. The keypad approach reduces operator entries from 8 or 16 switches to 2 or 4 keystrokes. This technique clearly minimizes operator errors but still does not provide much additional information. High speed CRT terminals, as implemented on most microcomputer development systems, merely act as high speed versions of a printer terminal. System software has not been updated to take full advantage of the CRT terminal speed; only the process is accelerated by generating output data at a greater rate.

The microcomputer development system designer uses the highest level of operator console, a memory refreshed CRT display, to take into account the ultra high speed capability of the console at design time. Thus, a context based debugger and a context based editor can be provided. In this type of console, the designer sees a continually updated register display, large memory dumps, and whole segments of source code in context, greatly reducing the confusion as to exactly what is happening. This type of interactive software is designed around consoles that operate with data rates between 10k and 50k char/s. The present state-of-the-art and

direction of microcomputer development systems indicate that this level of operator console should become more prevalent in the future.

Mass Storage Levels

Small computers use four general levels of system mass storage. The first level is no mass storage facility. The designer keys in the program, usually in binary or hexadecimal, and then executes immediately. The next level is paper tape based systems available on many small computers. The mass storage medium is punched paper tape, and the combined operator console and mass storage device is usually a teletypewriter. This level of storage system was dominant for many years, largely because of excellent cost-performance characteristics. Only recently have CRT displays and magnetic tape or disc systems been able to compete effectively with paper tape systems. The third level of mass storage is low speed magnetic tape (generally, cassette). Data are read and written into cassette tapes somewhere between 30 and 400 char/s. This represents an improvement of 3 to 40 times over the teletypewriter and makes low cost microcomputer development systems practical. This level of storage system is perhaps a good choice for relatively small programs (500 to 1000 lines or less), a limited budget, or an initial implementation of a development system.

The fourth, generally accepted standard for mass storage on development systems is flexible disc, either a 5.25" (13.34-cm) or an 8" (20-cm) diameter version. Data transfer rates are greater than 1000 char/s. Access time and throughput for this mass storage device cease to be significant factors in development time. Comparisons of editing overhead times using teletypewriter, paper tape reader and punch, medium speed cassette tape, and fast flexible disc indicate that even for a 100-line program, a teletypewriter is slow. Likewise, for a 1000-line program, the medium speed cassette based system is probably too slow. However, with a flexible disc based system, the designer edits and assembles 10k-line programs in a relatively short time.

Development System Architectures

Architectural considerations involved in comparing microcomputer development systems relate to two basic implementations of in-circuit emulation—a master-slave approach, such as taken by Intel and Tektronix, and a single-processor approach, such as that of Motorola, Futuredata, and Zilog. Table 2 summarizes these architectures and implications.

Master-Slave System

In a typical master-slave system (Fig 3), the master (host) microprocessor runs all system software functions, including editing, assembling, disc file management, and "downline loading" of object programs to be tested in the prototype (target) microprocessor using in-circuit emulation. The target (slave) microprocessor is the designer's microprocessor under investigation. The development system manufacturer primarily accrues the

TABLE 2
Development System Emulator Architectures and
Associated Hardware/Software Devices

<u>Manufacturer</u>	<u>Emulator Architecture</u>	<u>Micro-processors</u>	<u>Memory and Peripherals</u>	<u>Software</u>	<u>CRT Display</u>
Futurdata (Microemulator)	Single processor and common memory; allows full speed emulation and complete control of emulation modes; universal	8080 8085 8086 6800 6802 Z80	Up to 64k Cassette Floppy disc EPROM programmer Logic analyzer Printer	Editor Assembler Debugger Macro Assembler Linker BASIC Interpreter BASIC Compiler	Memory refreshed
Intel (ICE)	Modified master-slave single memory; slows emulation with wait states. Allows control of emulation modes; nonuniversal	8048 8080 8085 8086	Up to 64k Paper tape Floppy disc EPROM programmer Logic analyzer Printer	Editor Assembler Debugger Macro Assembler Linker PL/M Compiler FORTRAN Compiler	RS-232-C Teletype-writer mode*
Motorola (USE)	Single processor with common memory; nonuniversal	6800 6802	Up to 64k Cassette Floppy disc Printer	Editor Assembler Debugger Macro Assembler Linker BASIC Interpreter FORTRAN Compiler	RS-232-C Teletype-writer mode
Tektronix (In-Prototype Emulator)	Master-slave architecture with split memory; permits full speed emulation and control of emulation modes; universal	8080 8085 6800 Z80 9900	16k Host, Up to 64k Target Floppy disc EPROM programmer Logic analyzer Printer	Editor Assembler Debugger Macro Assembler Linker	RS-232-C Teletype-writer mode
Zilog (In-Circuit Emulator)	Single processor with common memory; allows only minimal control of emulation modes; nonuniversal	Z80	Up to 64k Floppy disc Printer	Editor Assembler Debugger Macro Assembler Linker PL/Z Compiler	RS-232-C Teletype-writer mode

*Teletypewriter mode: CRT display is treated as a byte-serial device with data rates of 120 to 960 char/s.

advantages of such an approach. First, using a standardized host microprocessor minimizes software cost for implementing a new microprocessor. The second advantage is that less of the system resources need be reserved for the host system.

A disadvantage of the master-slave system is that it splits memory into two separate spaces. The system programmer encounters more difficulty in dealing with a split memory and its discontinuous address space than with a single large memory. A single memory space more effectively handles host functions that require large amounts of memory (editor work areas, and assembler and compiler symbol tables). Thus, 16k of host memory and 16k of prototype memory provide only a 150-line

edit buffer. The same 32k memory in a single large device supports over 1500 lines of editor code (some of this advantage is due to packing the editor data). A second disadvantage is the higher cost that additional memory and microprocessors add to the system.

A third and rather subtle disadvantage relates to modification of the system programs. Most designers of computer systems realize that over a long period of time the supplied operating software will be modified. This modification may add a new I/O peripheral device, for example, printer or paper tape reader or punch, 7-track or 9-track tape drive, hard disc drive, or a number of devices not included in the original system. With the master-slave approach, the designer must modify pro-

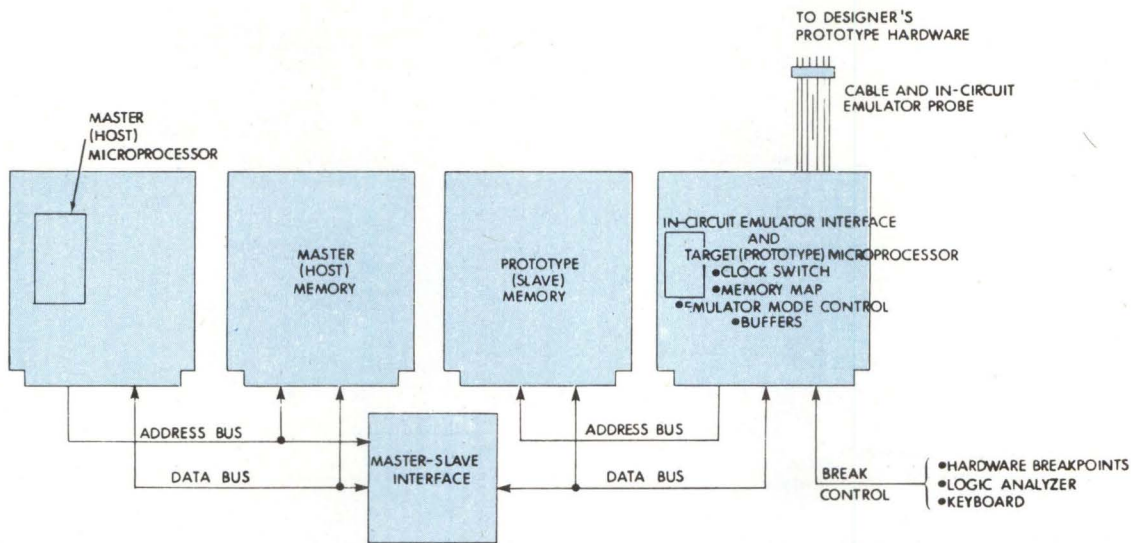


Fig 3 Master-slave in-circuit emulator architecture. System and prototype functions are divided between master (host) and slave (target) microprocessors, respectively. System development functions, such as file management, text editing, host I/O, and debugging, are performed by master microprocessor. Prototype related functions, such as prototype program execution, prototype I/O, and in-prototype testing, are done by slave microprocessor

grams written for an unfamiliar host microprocessor. Thus, an 8080 or 6800 designer might be confronted with the necessity of modifying code written for a 2650 microprocessor.

The Microemulator II systems permit both common and separated memories to be used, depending on designer requirements. A master-slave processor approach is used, but all memory is contiguous in the host system. The slave microprocessor is remote from the system (at the emulator plug), and none of its resources need to be reserved for the system. Software systems written in their native languages support the 8080, Z80, and 6800 families of microprocessors.

Single-Processor System

In a single-processor system (Fig 4), system software usually is written on the target microprocessor. Thus, a 6800 designer would modify 6800 code, an 8080 designer would modify 8080 code, and a Z80 designer would modify Z80 code. This type of development system can become a multipurpose device. After becoming familiar with the system hardware and software, many designers may use that same hardware in the development of test equipment that will follow the design through its production life.

The clear cut advantage of a single-processor system is low cost, since much less hardware is included. A second advantage is that one large memory is furnished; thus, a 32k memory space provides for 26k of object code in the prototype system, and an assembler symbol table with many thousands of symbols. The Intel ICE system, while a master-slave system, does provide for one large memory accessed by both microprocessors. To do this, the system delays the target microprocessor when it accesses development system memory. However, this compromises the ability to totally emulate prototype system operation. Another advantage of the single-processor system is the use of development system hardware and software as part of in-plant test equipment.

A disadvantage of a single-processor system is that the manufacturer must entirely rewrite software packages for each new microprocessor. Standardization trends in the industry make this less of a problem. A second disadvantage, depending on the application, is that emulation is not entirely separate. Thus, most single-processor systems reserve part of the memory space for system programs that must be resident during emulation. They generally have at least one privileged I/O address to switch the system in and out of emulation mode. Depending on the design of the single-processor system, it also may use some DMA capabilities and an interrupt

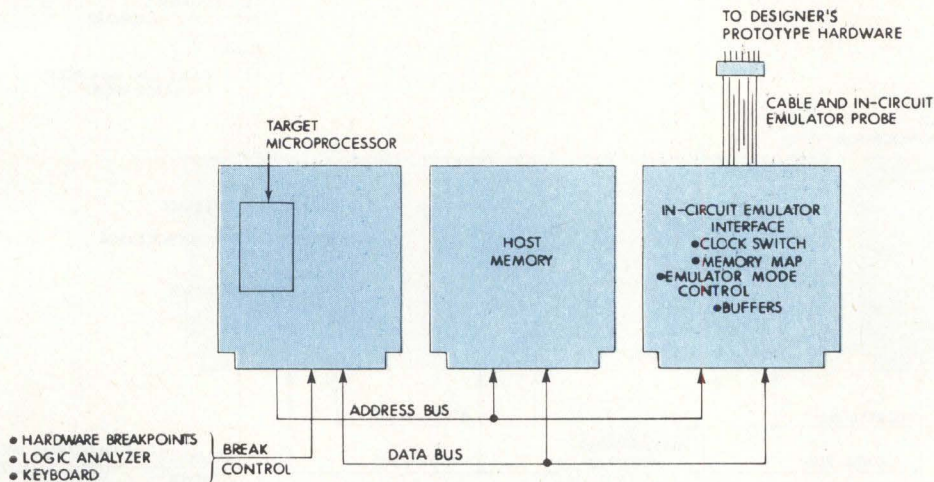


Fig 4 Single-processor in-circuit emulator architecture. Dedicated system development functions are programmed in related instructions for direct execution by target microprocessor. Differing target microprocessors require associated system software modifications

structure. The designer can upgrade the emulation capabilities of the system as needed to support development.

Summary

Microcomputer development systems have common capabilities of processor, memory, console, mass storage, in-circuit emulation, and system software. They differ in type of operator console, mass storage device, in-circuit emulation architecture, high level language support, and whether or not they are universal (support a wide range of microprocessors from a variety of manufacturers).

Development system support for the 8080 and 6800 and their successor microprocessors is necessary. These two microprocessors are standards to some extent, because of significant investment in 8080 and 6800 software. The 8080 standard includes as its successors the 8085, the 8086, and the Z80. The 6800 standard includes as its successors the 6802, 6809, and 6502. In general, these successor microprocessors, with the exception of the 6502, have attempted to remain program compatible with earlier versions. Both microprocessor manufacturers and designers who invested substantial amounts of money in programs to support these microprocessors require this compatibility.

With some 20 manufacturers, most of whom can introduce one or more microprocessors per year, a universal

development system becomes an essential tool for designers. Since the 8080 is 10 times more powerful than the 8008, the Z80 is 2 to 3 times more powerful than the 8080, and the Z8000 and 8086 are 5 to 10 times more powerful than the Z80, the pressure to adopt new microprocessors is intense. Thus, the designer must be able to switch the target microprocessor without starting from scratch.

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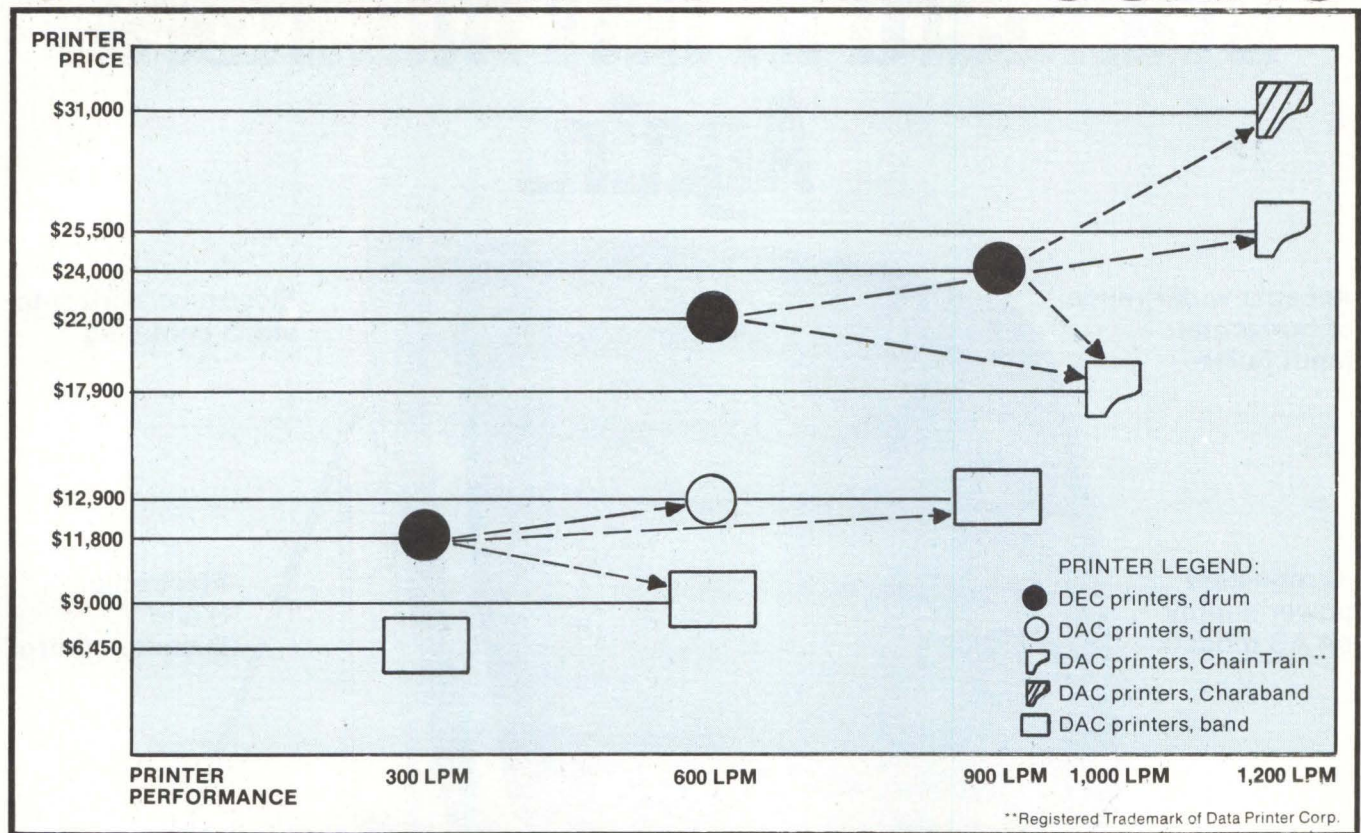
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Bruce Gladstone, vice president of Futuredata Computer Corp, has expertise in hardware and software aspects of microcomputer systems design, as well as electronic systems design. He has been responsible for Microemulators™, EPROM programmers, and Microanalyzer™ designs, and development system software and debuggers. He holds an MS in engineering from UCLA.

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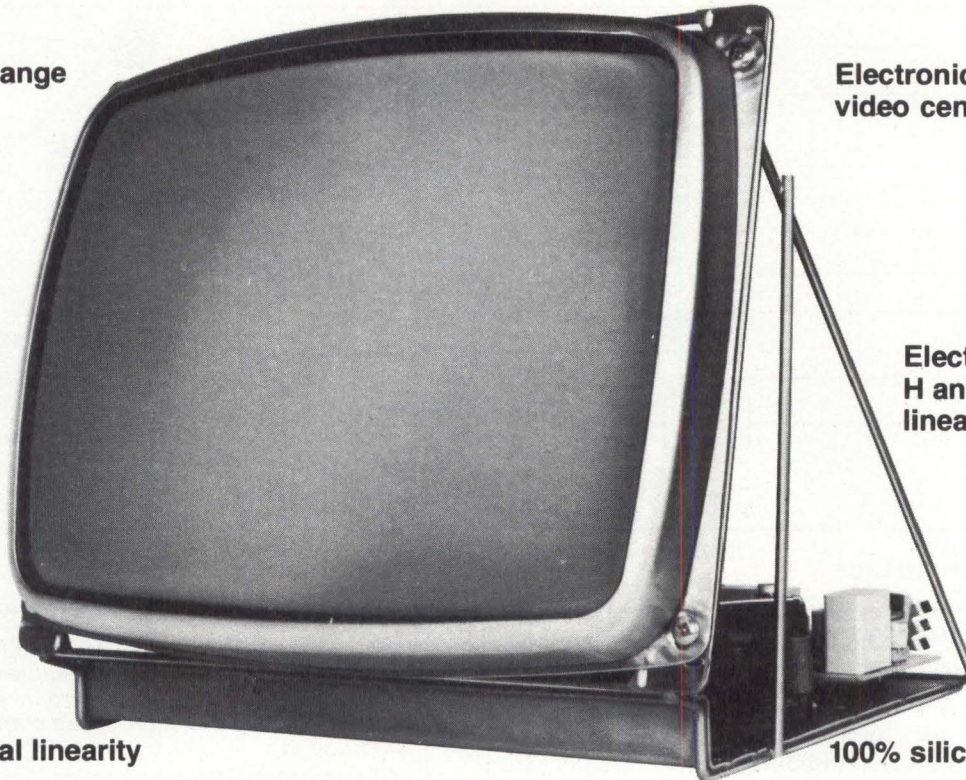
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HARDWARE LINK DIRECTS MULTICOMPUTER INTERACTIONS IN PROCESS CONTROL

Communications between central and satellite processors in a star-configured multicomputer industrial process control system are directed and controlled by an interprocessor hardware link embodying tradeoffs between speed and simplicity

Avinash D. Marathe and Anil K. Chandra

Bhabha Atomic Research Centre, Bombay, India

Traditionally, computerized industrial control processes have been under the direction of a single large computer. In such a centralized system, the entire process depends on the computer; if it fails, the process comes to a halt. While a backup computer may be provided, this tactic is usually expensive, and software required for a redundant centralized system becomes complex and inefficient because of the large and involved overhead.

Recent advances in technology have produced economical computing capabilities, resulting in a trend toward using multicomputer configurations for directing complex process control systems. Among the advantages to be realized in implementing these configurations are parallel processing for improved system response to realtime variations, greater software reliability, and built-in redundancy.^{1,2,3}

Multiprocessor, as distinguished from multicomputer, systems have integrated software working on a single input data stream. Main memory and most other hardware resources are accessible to all processors. In a multicomputer system, however, each computer has its own operating system working on a distinct data stream, memory is seldom shared, and little data transfer occurs between constituent computers.

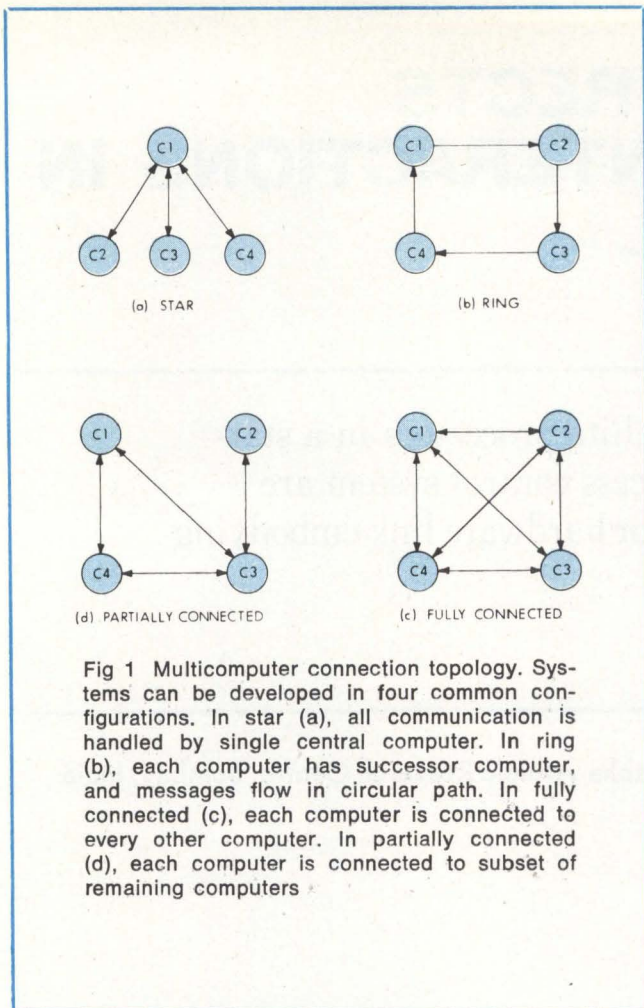
Multicomputer systems are distributed intelligence systems and are ideally suited to applications where it

is possible to segregate independent subsystems that require relatively little interaction. Dedication of a computer to each subsystem permits the software of each computer to be custom tailored to a specific task, resulting in improved system throughput. Each computer in a multicomputer system performs jobs that are specifically partitioned to minimize the extent of their interaction.

In many process control applications, however, a significant amount of information generated in a source computer must be transferred to a destination computer for further processing. The interprocessor communicator (IPC), a hardware link, has been developed to conduct and control data transfers in a multicomputer process control system. Data transmission rates between the various computers, and therefore system throughput, are constrained by the design aspects of the IPC.

Multicomputer System Configurations

A multicomputer system is usually characterized by topology (Fig 1), composition, control mechanism, type of communication channel, and mode of task allocation.⁴ Topology refers to the scheme of interconnecting different computers in a given system—star, ring, partially, or fully connected. A multicomputer system can have



all computers identical (homogeneous composition) or all computers mixed (heterogeneous composition). The control mechanism can be centralized, with only one computer making all decisions, or distributed, with decision-making scattered among all computers in the system. Data transfers may take place in serial mode over a single line communication channel or in parallel over a multiline channel. Allocation of tasks to each computer can be dynamic, during system operation, or static, during system design.

Different multicomputer configurations can be evaluated by such criteria as throughput, software overhead, and fail-safe capabilities. For example, a star organization generally permits the highest level of throughput.⁵ However, these attributes may not be directly applicable to a multicomputer system used in a process control environment, where a system is subject to several additional design constraints.

First, a system overview of the controlled process must be retained at all times. In a multicomputer system, this overview is best implemented by having centralized control in a star-connected configuration. The central computer can regularly obtain relevant information from peripheral computers and utilize the data to optimize various control parameters.

Second, the multicomputer system must respond efficiently and rapidly to quick changing process control parameters. To ensure fast response, the overhead associated with a multicomputer system, such as interprocessor communication, should be minimal. Therefore, except for geographically widespread control systems (eg, for oil fields), such communication should be over parallel lines. Also, jobs should not be distributed among the various computers in real time, but should be as-

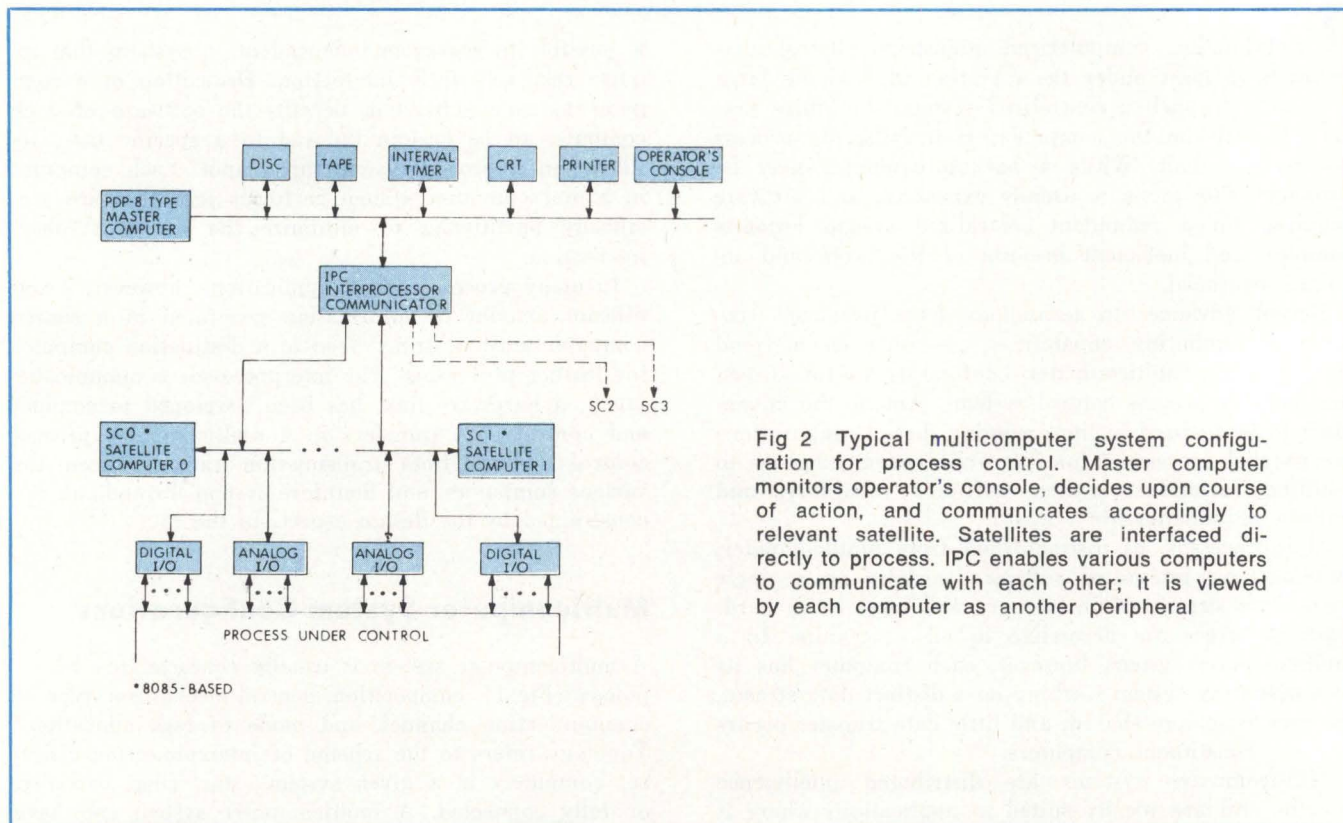


Fig 2 Typical multicomputer system configuration for process control. Master computer monitors operator's console, decides upon course of action, and communicates accordingly to relevant satellite. Satellites are interfaced directly to process. IPC enables various computers to communicate with each other; it is viewed by each computer as another peripheral

signed to each constituent computer during system design. This allotment is adaptable to process control, since the control problems are normally well defined.

Third, various peripherals, such as discs, tapes, operator consoles, terminals, and printers, should be subordinate to the centralized main computer, which obviously has to be more powerful than the peripheral computers.

Fourth, for speed, simplicity, and economy, hardware units should control the information flow between multi-computer system and process. Thus, a given set of signals would be routed to a specific computer, implying that all jobs associated with these signals should be handled only by the corresponding computer.

Consequently, based on evaluation of the described design factors, a heterogeneous star-organized multi-computer system with static allocation of tasks is well suited to complex process control applications. A typical system configuration (Fig 2) consists of a central master computer, several peripheral satellite computers, and an IPC, with each computer connected to several peripherals.

In operation, jobs assigned to all computers are synchronized to be performed in fixed periods of time marked by the interval timer. At the beginning of any such period, the master computer analyzes the operator's console commands, prepares command words, and conveys these commands to the relevant satellite computers. These computers operate according to the commands and, at the end of a particular time period, prepare status words that are conveyed to the master.

The IPC enables the constituent computers to interact with each other. Actual information transferred by the IPC may be of several types. If satellite programs are stored on disc, the master fetches these programs during initialization and transfers them through IPC to the relevant satellite(s). Most of the information to be displayed on the system CRT is actually generated in the satellites, since these computers are directly interfaced to the process. Process status information, as well as command and status words, are transferred by the satellites through the IPC to the master.

IPC Design Considerations

Several tradeoff factors must be evaluated in the design of an IPC for multiple computers connected in a star configuration. For example, transfer of data from one computer to another can be carried out either under control of each participant computer's program or in the DMA (direct memory access) mode under IPC control. In the program control mode, the source computer writes the required information in, as an example, a 128-byte RAM in IPC and sets a flag to indicate that data are available or that memory is full. The destination computer subsequently checks the flag and, on finding it set, accesses the IPC to retrieve the written information.

It is necessary to have such information blocks available at a dual-port memory for each pair of computers. Also, contention problems must be solved in the event that two computers simultaneously try to access the same memory block.

In the DMA mode, the source computer provides IPC with information regarding size and location of the relevant block of data, identity of the destination computer,

and direction of data transfer. Once the transfer is initiated, it is the responsibility of IPC to fetch the data from the source computer and convey it to the destination computer. Normally, data transfers in DMA mode are much faster than those in program control mode. Also, DMA mode is asynchronous with normal processing, demanding minimal CPU involvement. For handling process control systems, the overhead associated with IPC is minimized in the DMA mode.

In a general process control application, a particular computer should be able to communicate with any other system computer. This availability permits fast communication over the shortest path. However, hardware required for control and direction of this communication configuration is extensive and involves a complex flow of control paths. One alternative is to route all communications through the master. Thus, when data are transferred from one satellite to another, the first satellite transfers the data to the master, which then conveys the data to the second satellite. This path constraint is not severe, as the extent of communications required between satellites is already minimized by the established scheme of task partitioning.

Again, in a general application, communications between the master and a satellite should be independent of any other similar communication in progress. This setup results in high processing rates because no satellite needs to wait for any other, but dictates that the number of data channels must match the number of satellites. To save the considerable hardware and cost required for a multichannel communications system, albeit at the expense of speed, the number of data communication channels is restricted to one. The IPC can fetch data from the source computer, keep filling a multiword buffer at one end, retrieve data from the other end, and keep conveying data to the destination computer. This type of buffer increases the speed of data transfer but involves complex control. A simpler alternative is to have only a 1-word buffer.

In addition to cost considerations, each design factor involves a tradeoff between speed and simplicity. Higher speed operation requires additional hardware, increases complexity, and reduces reliability. Since the IPC is a critical system node, it is advisable to opt for simplicity and reliability at the expense of speed. In practice, the software structure can be organized to overcome some of the speed limitations.

Data transactions through the IPC can be initiated by any system computer. Because only a single communication channel has been established, logic must be provided to resolve the conflict of multiple requests. An economical alternative is to restrict this privilege to the master computer only. In this manner, the master retains the desired overview of the system, and controls the timing of each data transfer. The IPC link with the satellites can be a radial (parallel) or a serial bus configuration. A radial link is preferable since failure at any point in a serial bus link can bring down the entire system.

IPC Hardware Design and Operation

In a typical process control system, motion (speed and position), temperature, pressure, flow, and weight are

a few of the physical process variables that are measured by various transducers, such as potentiometers, thermocouples, pressure switches, and flow meters. These physical quantities are converted to electrical analog signals, which are then digitized by analog-to-digital converters. The digitized values are fed to a digital computer through an analog input unit (AIU), which samples the values at periodic intervals. The computer compares the sampled values with setpoint values stored in memory and decides the corrective action to be taken.

Digital variables representing the state of digital transducers, such as limit switches, are similarly fed to the computer through a digital input unit (DIU). The computer analyzes these logic variables and takes action by effecting the state of digital outputs through a digital output unit (DOU).

In the process control multicomputer system under discussion, a 12-bit minicomputer (PDP-8 type) serves as master and four 8-bit microcomputers (MIDGET type, using 8085 microprocessors) perform as satellites (Fig 2). In this system design, only the master initiates a transaction. All satellite-to-satellite communications are routed through the master, and the master can communicate with only one satellite at a time.

To effect a data transfer, the master first provides relevant information to the IPC. Information required includes size of the data block to be transferred, starting address of the block in the source computer, and starting address of the region where this block of data is to be deposited in the destination computer. Also, the identity of the satellite and the direction of transfer must be specified before finally instructing the IPC to commence operation. All data transfers between master and IPC are conducted as 8-bit (1-byte) operations for convenience, because of the obvious incompatibility between the 12-bit master and 8-bit satellite word lengths.

Upon completion of a data block transfer, a check is made to verify that the transfer has been carried out properly. To effect this check, the master reloads the IPC with the sizes and starting addresses of the data blocks for the source and destination computers. The IPC then initiates a transfer in read-check mode by fetching the first data items from each of the two blocks and comparing them. If they are not identical, the IPC informs the master that there is an error in the transfer. If the first items match, the IPC fetches and compares the next two items, and so on, until the entire block is completely checked. The IPC also carries out parity checks on the data items. Each computer supplies a parity bit along with the DMA data byte, and the IPC checks for validity. If necessary, these checks can be inhibited.

IPC Registers

There are three 16-bit registers and two 8-bit registers in the IPC, all accessible by the software program (Fig 3). The 16-bit satellite address counter (SAC) tracks the memory address of the relevant satellite during the course of a single master-to-satellite data transaction. This register is loaded initially by the master with the starting address of the data block in the relevant satellite memory. Since the master conducts 8-bit transactions only, it requires two instructions to load SAC completely (see "List of IPC Instructions"). Contents of SAC are incremented during a data transaction as each byte is loaded into or read from a satellite.

The 16-bit block counter (BC) similarly loads the 2's complement of the size of the data block to be transferred, thereby permitting a theoretical maximum of a 64k block length transfer. In practice, the size is limited

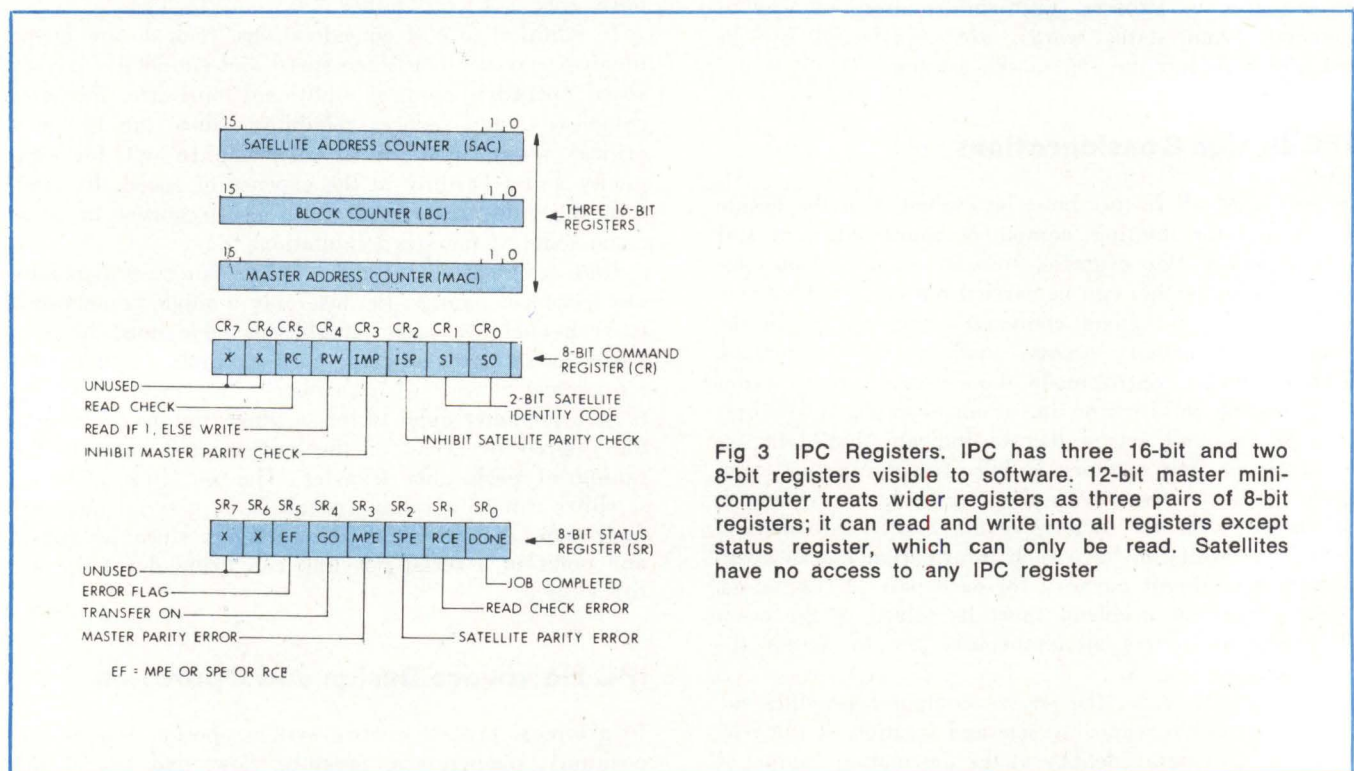


Fig 3 IPC Registers. IPC has three 16-bit and two 8-bit registers visible to software. 12-bit master minicomputer treats wider registers as three pairs of 8-bit registers; it can read and write into all registers except status register, which can only be read. Satellites have no access to any IPC register

List of IPC Instructions

Instruction	Function
Read or load SAC (High-order byte)	Transfer 8-bit data between PCT data bus and high/low significant half of relevant 16-bit counter
Read or load SAC (Low-order byte)	
Read or load BC (High-order byte)	
Read or load BC (Low-order byte)	
Read or load MAC (High-order byte)	
Read or load MAC (Low-order byte)	
Read or load CR	Transfer 8-bit data between PCT data bus and CR
Read SR	Transfer 8-bit data from SR to PCT data bus
Initiate transfer (GO)	Commence DMA data transfer operations under control of IPC
Check if IPC Interrupting	Skip next instruction in software program if condition is true
Check if Done	
Check if Error	Stop DMA data transfer operations
Abort Transfer	

because the master storage capacity is only 32k. The BC is incremented when one byte is completely transferred from the source computer to the destination computer. When BC overflows, it causes IPC operation to cease.

The 16-bit master address counter (MAC) stores the starting address of the data block in master memory. Since the minicomputer used has only a 15-bit address bus, the most significant bit of MAC is not utilized.

The command register (CR) is an 8-bit latch; however, only six bits are defined. Bits CR1 and CR0 define a 2-bit code (s1, s0), which is decoded to select one of the four satellites for participation in the data transaction. Bits CR3 and CR2 can be set to suppress the parity checks carried out normally on master data and satellite data, respectively. Bit CR4 defines the direction of data transfer relative to the master, while bit CR5 can be set to effect a read check. In the read-check mode, the state of bit CR4 is ignored, and IPC reads data from both the source and destination computers. Registers SAC, BC, MAC, and CR can be read back by the master, after loading, to check for errors.

The 8-bit status register (SR) also has only six defined bits. Bit SR0 is set if a data transaction (read-check or actual transfer) is completed successfully. Bit SR1 is set if an error is detected during a read-check operation. Bits SR3 and SR2 indicate detection of parity error in data received from master or satellite, respectively. The GO bit (SR4) stays set as long as any transaction is in operation. Bit SR5 is set if any one of bits SR3, SR2, or SR1 is set and indicates an error. The master can check the state of the error flag (SR5) directly without reading the status register. The status register is cleared by the load CR instruction. In addition, the IPC has two 9-bit (8-bit data + 1-bit parity) buffer registers—a read buffer (RB) and a write buffer (WB)—for receiving DMA data from the master and a

satellite, respectively. Both buffers are transparent to the software program.

Typically, the registers operate as follows. The master loads the SAC, BC, and MAC registers. Then it reads back the register contents to check if the loading operation has been performed correctly. Next, it loads CR with the satellite identity and, for example, a read command. Finally, it gives an initiate transfer (GO) instruction.

In turn, IPC takes control and begins to effect the transfer. The master can check when the transfer is over either by polling IPC (check if done) or by waiting for an interrupt. If the transfer is not completed within a certain time interval, the master aborts the operation and attempts again. If the transfer is completed and there is a parity error, the master repeats the entire process once more. If the transfer is completed successfully, the master reloads the various registers and then issues a read-check command. On a read-check error, the master repeats the loading once again. If there is an error repetition, the master computer informs the operator's console. A flow chart of operation within the IPC is shown in Fig 4.

IPC Design implementation

The master computer has four buses on which all peripherals are connected (Fig 5). During DMA operations, a peripheral presents the address of the desired memory location on the address bus, and data transfer can take place on the DMA data bus in either direction. Data transfers conducted under program control are carried out on the program control transfer (PCT) data bus. The fourth or control (CNTL) bus carries the control signals used during DMA and program control data transfers. There are three buses on the satellites—address, data, and control.

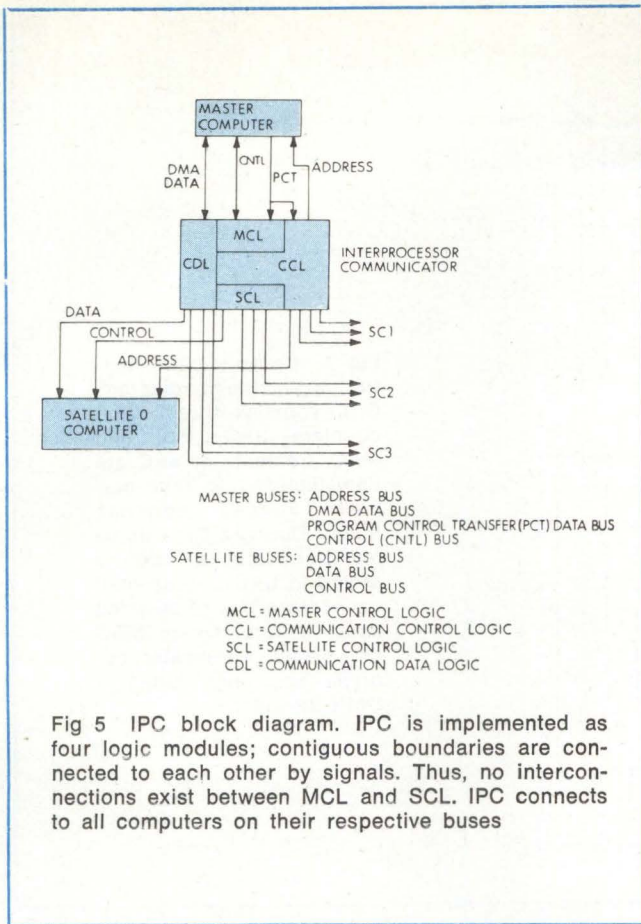


Fig 5 IPC block diagram. IPC is implemented as four logic modules; contiguous boundaries are connected to each other by signals. Thus, no interconnections exist between MCL and SCL. IPC connects to all computers on their respective buses

Four logic modules make up the IPC—MCL, CCL, SCL, and CDL. Master control logic (MCL) (Fig 6) contains all control circuits required for the master to communicate with IPC. Device identification logic detects the address code for IPC on the control lines and enables the remaining MCL logic blocks. Instruction decoding generates suitable control signals to execute the different instructions. DMA logic sends a DMA request to the master at the proper time and generates the control signals necessary to effect such a transfer. MCL also contains the command register (CR) and the status register (SR).

Communicator control logic (CCL) (Fig 7) contains the read/write SAC, BC, and MAC registers. SAC register output is demultiplexed into four normally 3-stated satellite address buses. During a DMA transaction involving a satellite, the relevant address bus is activated, and the contents of SAC are placed on this bus. Similarly, the 3-stated output of the MAC register is activated only during a DMA transfer involving the master. Logic to increment the SAC, BC, and MAC counters is distributed in the MCL and SCL modules.

Satellite control logic (SCL) (Fig 8) contains the logic required to generate and receive the various control signals during a DMA transaction involving a satellite. These signals effect a read or write operation on the relevant satellite memory, and are generated subject to the timing constraints imposed by the satellites. All outgoing control signals are normally 3-stated. CCL also contains logic to increment SAC.

All DMA data flow is carried out in the communicator data logic (CDL) module (Fig 9). DMA data from

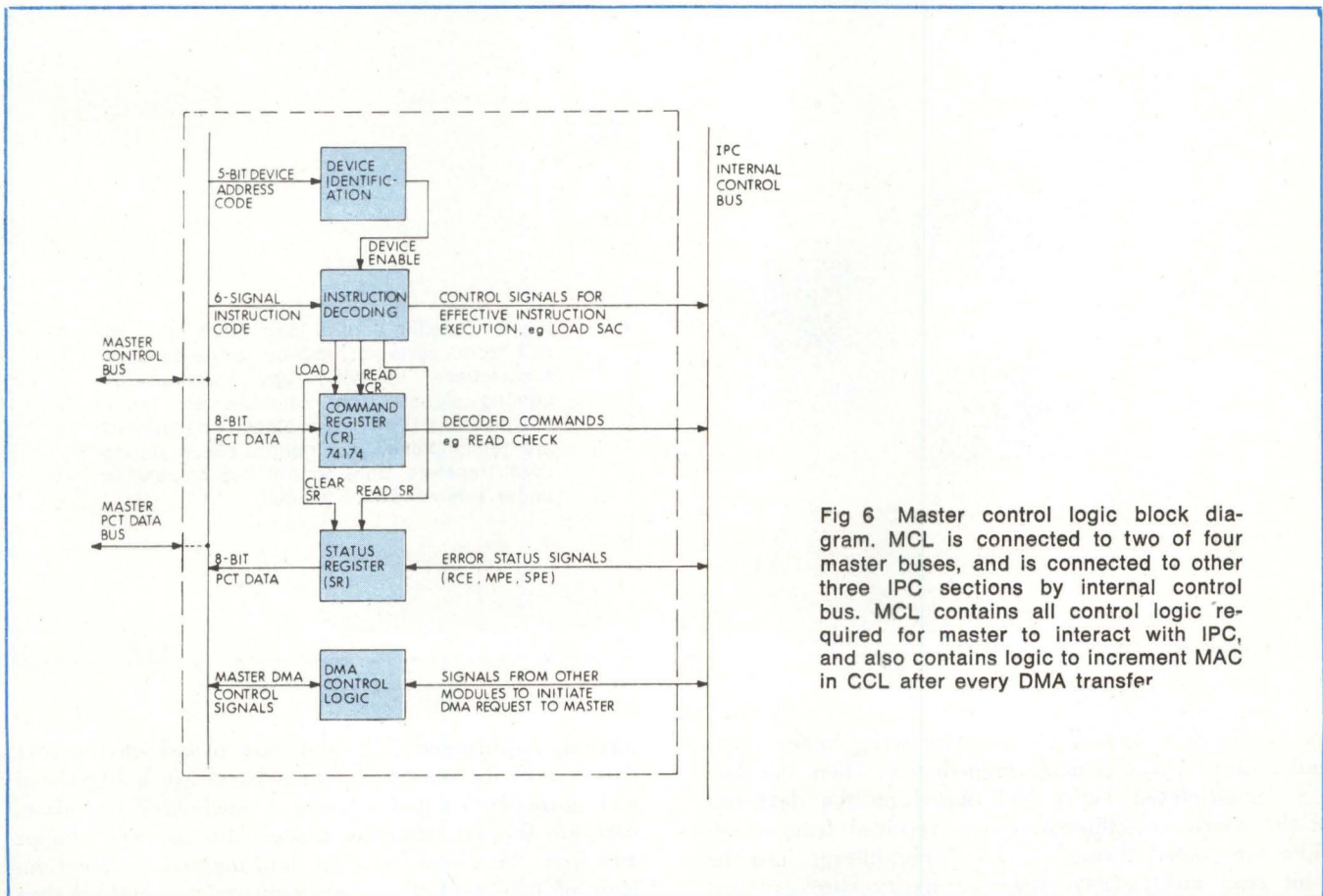


Fig 6 Master control logic block diagram. MCL is connected to two of four master buses, and is connected to other three IPC sections by internal control bus. MCL contains all control logic required for master to interact with IPC, and also contains logic to increment MAC in CCL after every DMA transfer

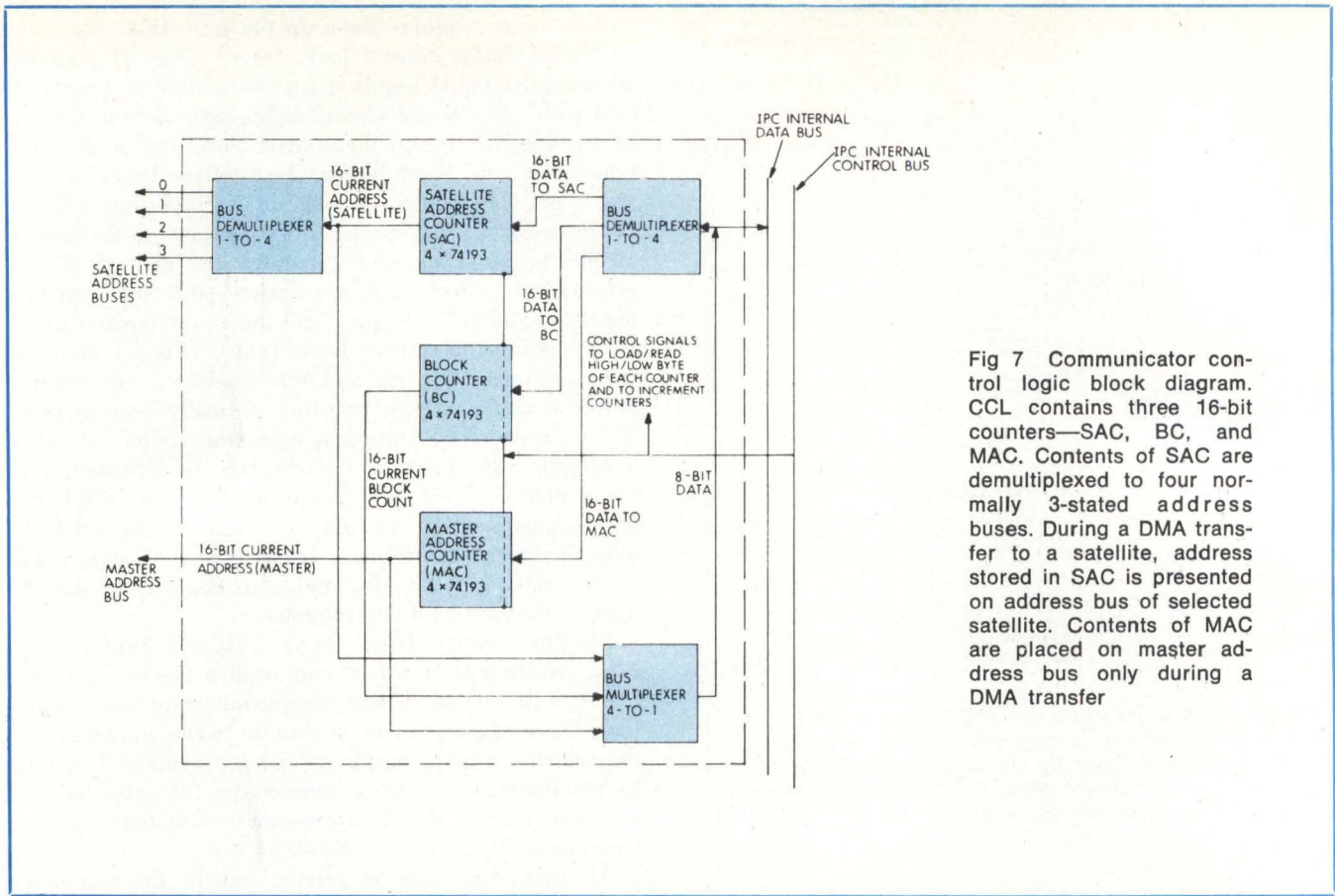


Fig 7 Communicator control logic block diagram. CCL contains three 16-bit counters—SAC, BC, and MAC. Contents of SAC are demultiplexed to four normally 3-stated address buses. During a DMA transfer to a satellite, address stored in SAC is presented on address bus of selected satellite. Contents of MAC are placed on master address bus only during a DMA transfer

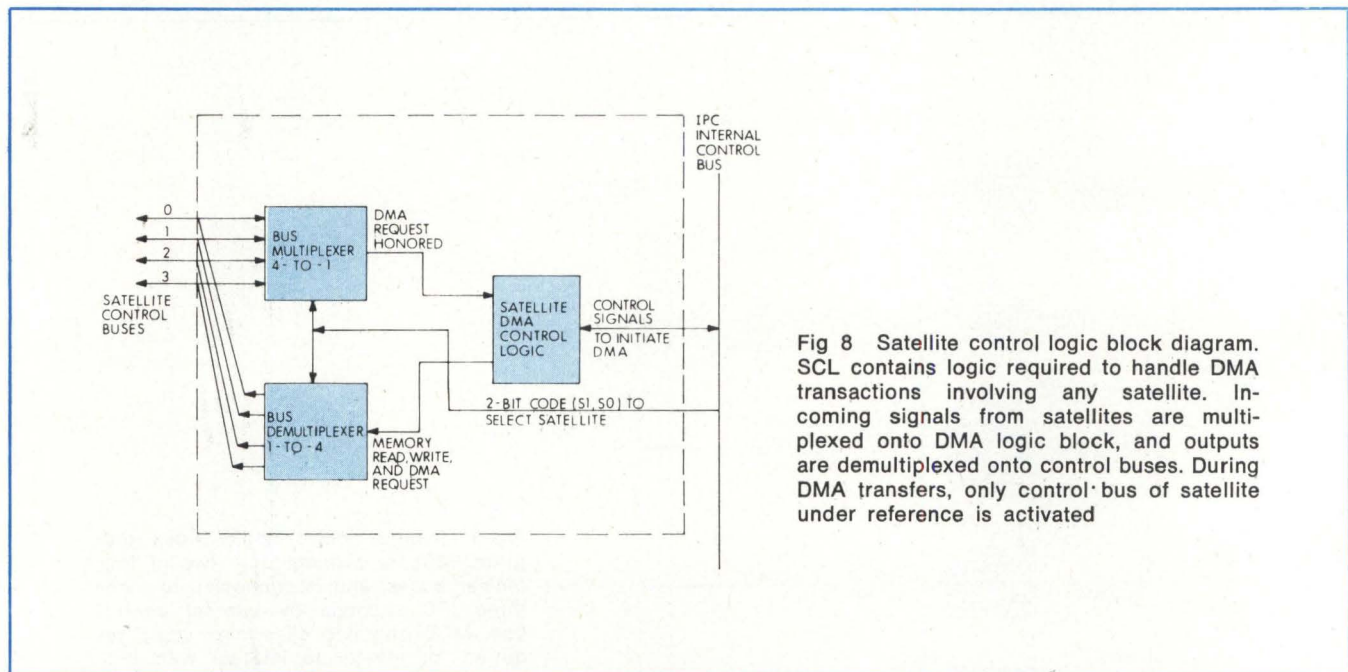


Fig 8 Satellite control logic block diagram. SCL contains logic required to handle DMA transactions involving any satellite. Incoming signals from satellites are multiplexed onto DMA logic block, and outputs are demultiplexed onto control buses. During DMA transfers, only control bus of satellite under reference is activated

the master are received by the 9-bit write buffer (WB) and a parity check is made immediately. Then, the data are demultiplexed 1-to-4 and placed on the data bus of the selected satellite. DMA data received from a satellite are passed through a 4-to-1 multiplexer into the 9-bit read buffer (RB), where a parity check is per-

formed. Subsequently, the data are placed on the DMA data bus of the master. All data buses are bidirectional and normally 3-stated. During a read-check operation, data are fetched from the master into the write buffer and from the selected satellite into the read buffer. Contents of the two buffers are compared to check if they

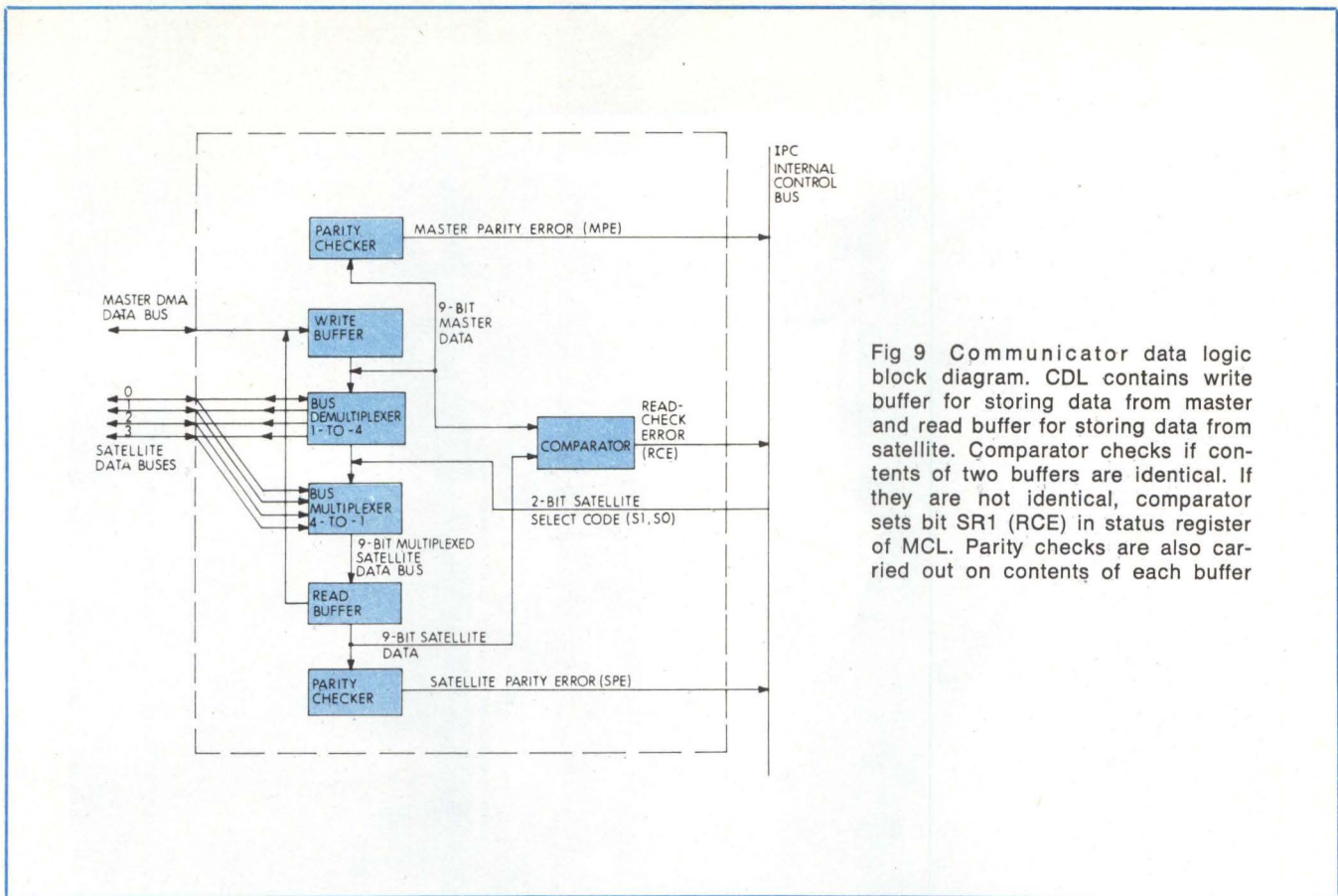


Fig 9 Communicator data logic block diagram. CDL contains write buffer for storing data from master and read buffer for storing data from satellite. Comparator checks if contents of two buffers are identical. If they are not identical, comparator sets bit SR1 (RCE) in status register of MCL. Parity checks are also carried out on contents of each buffer

are identical; meanwhile, parity checks are carried out on both data items.

Summary

Design of an IPC link for a star-connected multicomputer process control system discussed here consists of a PDP-8 type 12-bit minicomputer and four MIDGET microcomputers, built around an 8085 8-bit microprocessor. The multiple computer configuration is more powerful and flexible compared to a single centralized computer system.

Hardware and some of the software considerations involved in IPC design have been explained. The IPC design has been simplified to ensure reliability by imposing constraints on interprocessor communication requirements. Several design factors involved a tradeoff between data transfer speed and hardware complexity. In all cases, speed has been sacrificed to maintain hardware design simplicity. Several error check capabilities are provided to ensure integrity of all data transactions.

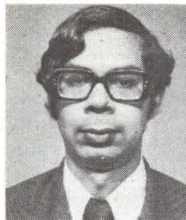
To ensure hardware simplicity, many IPC functions have been relegated to software, thereby increasing software complexity and slowing down IPC operations. Also, because of the incompatibility of minicomputer and microcomputer word lengths (12 bits vs 8 bits), some data bits of the master computer remain unused in data transactions. Accordingly, a multicomputer system using a 16-bit minicomputer as master would result in an improved communications solution, and should be considered for more powerful process control system designs.

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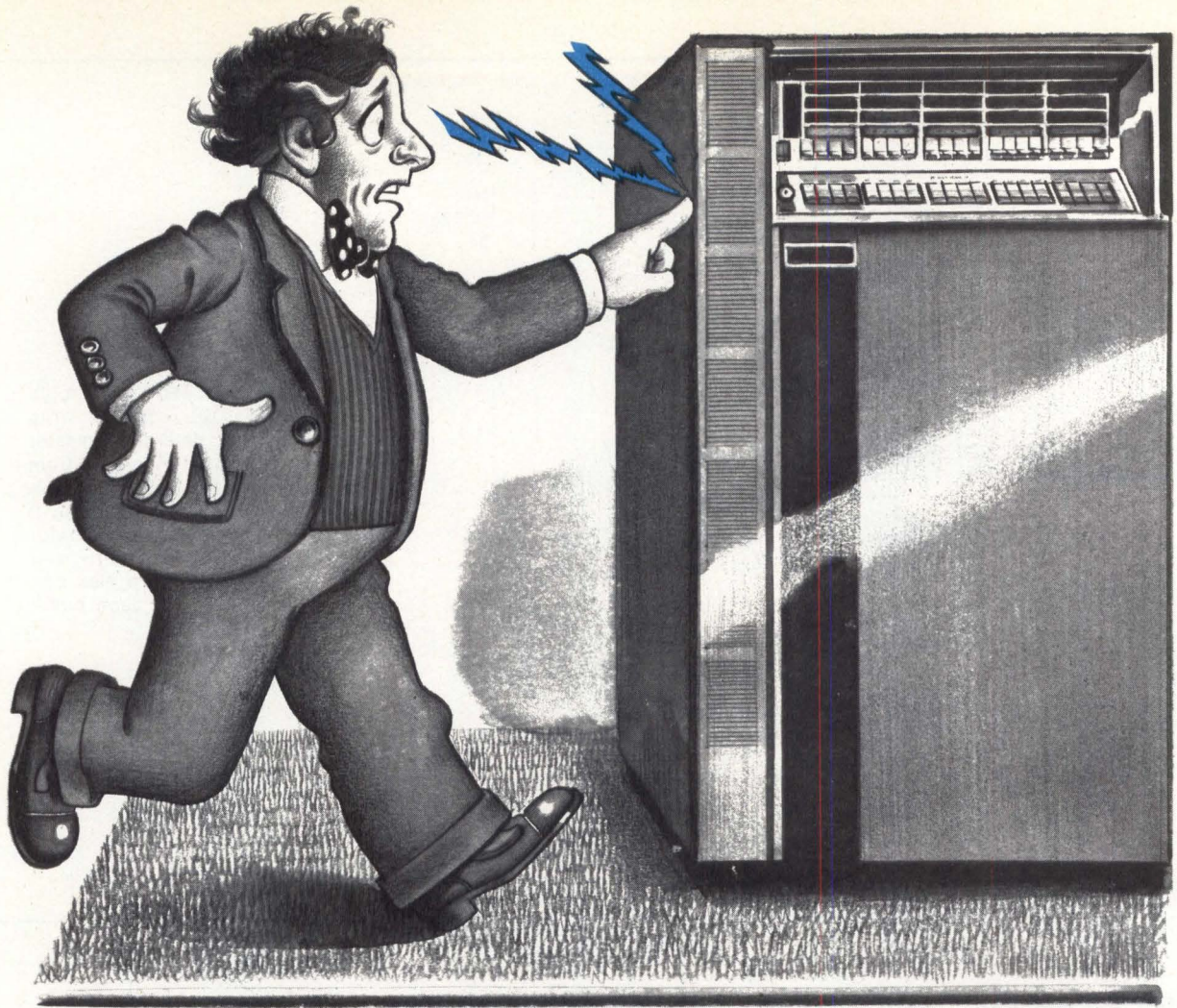
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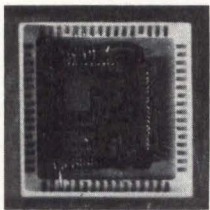
Avinash D. Marathe is a scientific officer in the Reactor Control Div, Bhabha Atomic Research Centre. He works in design and development of system software for nuclear power plant computer-based control systems. He has a Bachelor of Engineering in EE degree from the College of Engineering, Pune



Anil K. Chandra is also a scientific officer at B. A. R. C.'s Reactor Control Div. He is in system design and hardware development for nuclear power plant control systems. He has a Bachelor of Technology in EE degree from the Indian Institute of Technology, Delhi



DESTROYING A CIRCUIT IS AS EASY AS WALKING ACROSS A CARPET



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PARALLEL PROCESSOR ARCHITECTURES—

PART 2: SPECIAL PURPOSE SYSTEMS

High performance special purpose and scientific attached computing systems contain architectures that are custom tailored to solution of a certain problem. Grouping such systems by intent and capability allows general comparisons to be made within these limited classes

Kenneth J. Thurber Sperry Univac, St Paul, Minnesota

Focusing on special purpose systems, Part 2 considers systems that are specially tailored to perform well in only one or a very limited set of applications. These machines gain proficiency through associative memory or through the capability to provide associative addressing and to perform vector and matrix operations. Performance comparisons are made within two limited groups: special purpose parallel processing systems

(STARAN,¹ PEPE,² and ILLIAC IV³) and special purpose scientific attached processors (AP-120B,⁴ 3838,⁵ BSP,⁶ and MATP⁷). While this examination of individual architectures reveals limitations in application scope, a look at how they perform matrix operations reveals performance characteristics that may be expected from each.

Special Purpose Systems

Special purpose in the sense that their architectures are tailored to provide optimum performance in a certain type of application, this category of processors includes the Goodyear STARAN, PEPE, and ILLIAC IV.* Common to all of these is the use of an associative memory or the capability to provide associative addressing.

Part 1 of this 2-part article, published in January, discussed general purpose concepts of parallel processing, multiprocessor systems, and pipeline and functional systems. Architectural structures of STAR, ASC, and CRAY-1 computers were examined in relation to their potential performance in special problem areas. In contrasting these machines some of the differences between pipeline and functional machines have been pointed up, and areas of optimum performance for each have been identified.

*Portions of the descriptions of the STARAN, PEPE, and ILLIAC IV architectures were excerpted with permission from *Data Structures and Computer Architecture: Design Issues at the Hardware/Software Interface* by K. J. Thurber and P. C. Patton, published by D. C. Heath, Lexington, Mass, 1977.

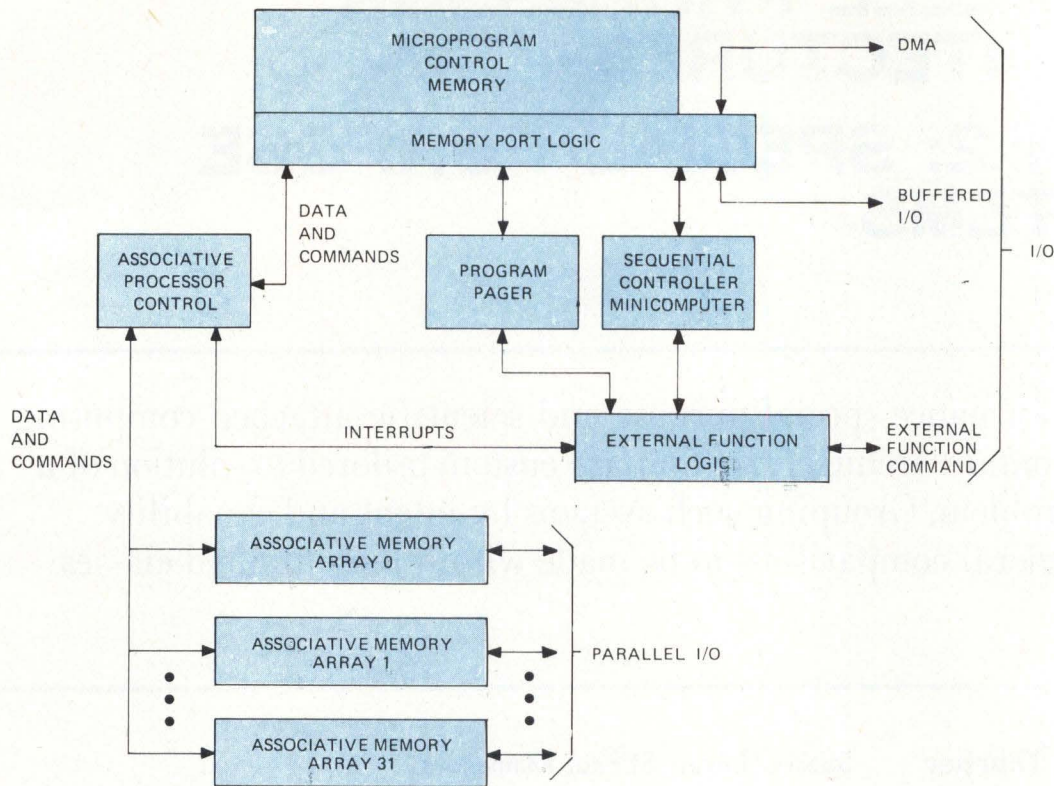


Fig 1 STARAN system. System may contain up to 32 memory arrays, controller for arrays, external function logic, paging device, sequential controller minicomputer, and memory along with associated porting hardware. STARAN E allows each basic memory array to have associated backup random access storage that can be paged onto associative memory arrays

STARAN System

The STARAN series of processors is based upon the concept of associative memory. Associative memories "address" their data via data characteristics (eg, greater than, less than, between limits, and equality), rather than by the address location of data as in a conventional random-access memory (RAM).

Plated wire was used as the storage medium in early Goodyear associative processors. These machines consisted of a basic bit-slice associative processor and, thus, were restricted to a bit-serial mode of input/output (I/O) access. STARAN B¹—a bit-slice semiconductor processor—was designed to correct this deficiency. STARAN E⁸—an advanced STARAN B—provides a RAM acting as a backing store to each associative memory array. These processors have parallel word I/O; they use an exclusive-OR (XOR) generated, skewed logic storage technique. In this technique, a RAM is oriented for bit-slice associative processing and essentially stores a bit slice (bit slice "i" consists of the *i*th bit of all words) in a single RAM word. Conceptually, the data may be viewed as stored and rotated 90 degrees from its normal storage orientation in the RAM.

To retrieve a word, a bit-serial operation sequence is required.⁹ A solution to this problem is to place an adder in front of each memory chip decoder in an adder skew technique.¹⁰ To retrieve bit slices, the adders are engaged and the memory chip number is added to the address before it is decoded. To retrieve words, the adders are ignored. The effect of this process is to "skew" the data in memory, thereby allowing both bit slices and words to be retrieved in a bit-parallel manner. Unfortunately, this procedure is not as modular as desired.

In a similar technique, XOR gates can be placed in front of the chip address decoders and the data skewed. In both cases, data may have to be shifted prior to storage or after retrieval to ensure that the programmer sees both bit slices and words. Furthermore, due to symmetry, it is not essential which mode of storage is designated for words or bits, as long as the convention is followed after it has been established.

To the programmer, the basic array appears to be addressable in either a bit-slice or a word-slice mode; that is, either all bits of a word (word slice) or the *i*th bit of all words (bit slice *i*) may be addressed. In addi-

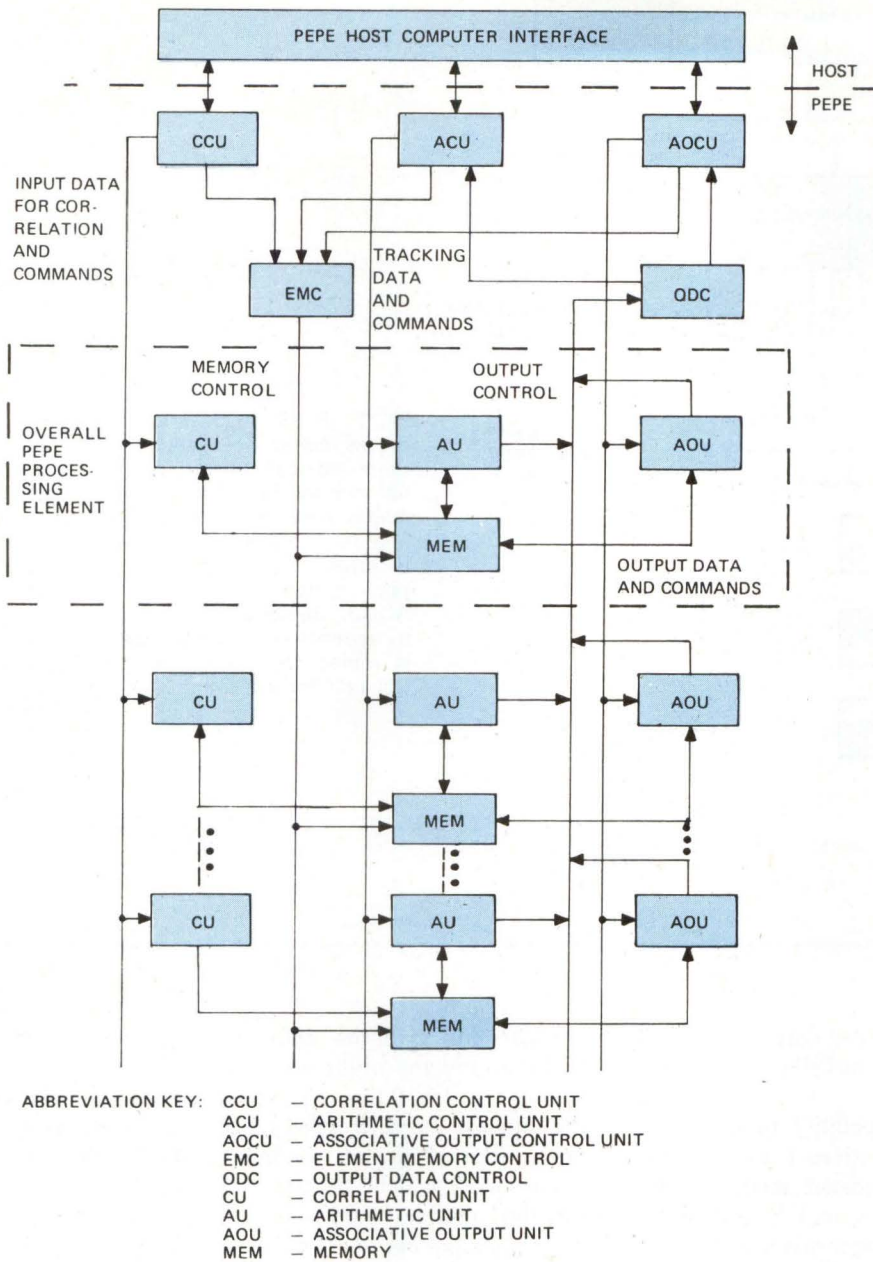


Fig 2 PEPE system. Complete system consists of three controllers—CCU, ACU, and AOCU. Each controller drives set of parallel processors—CU, AU, and AOU, respectively. CU, AU, and AOU share common memory and can be integrated to form complete processing element. Access control to memory resides primarily with ACU. Element memory control (EMC) and output data control (ODC) functions, in conjunction with ACU, establish memory exclusion capability during operation. All controllers have access paths to host processor

tion, STARAN can provide capability to address mixed modes; for example, it could be set to address two contiguous bits of every other word, four contiguous bits of every fourth word, etc.

A basic STARAN memory array contains a logic circuit called a flip network (FN). Internally, the machine addresses either bit slices (FN is essentially bypassed) or word slices (FN addresses "diagonals"). Data, when stored in a skewed manner, as described previously, can be viewed as stored along a diagonal, ie, a nonvertical or nonhorizontal memory map in the memory array. The number of word slices and bit slices is 256 for a STARAN B memory array, as this size is compatible

with many commercially available RAMs. Most of the FN logic can be implemented utilizing off-the-shelf selector decoder logic and XOR chips, specifically, MC10174L selector chips and MC10107L XOR chips. Cost of FN is about 80% of the cost of a memory array; the array (256 words x 256 bits) contains 65,536 bits, and FN is equivalent to about 50,000 bits.

The basic memory array also contains X, Y, and M registers in parallel, each consisting of 1 bit/associative-memory word. The X register stores temporary results; the Y register acts as a search-results register, that is, contains the results of search, arithmetic, and logic operations; and the M register specifies element activity.

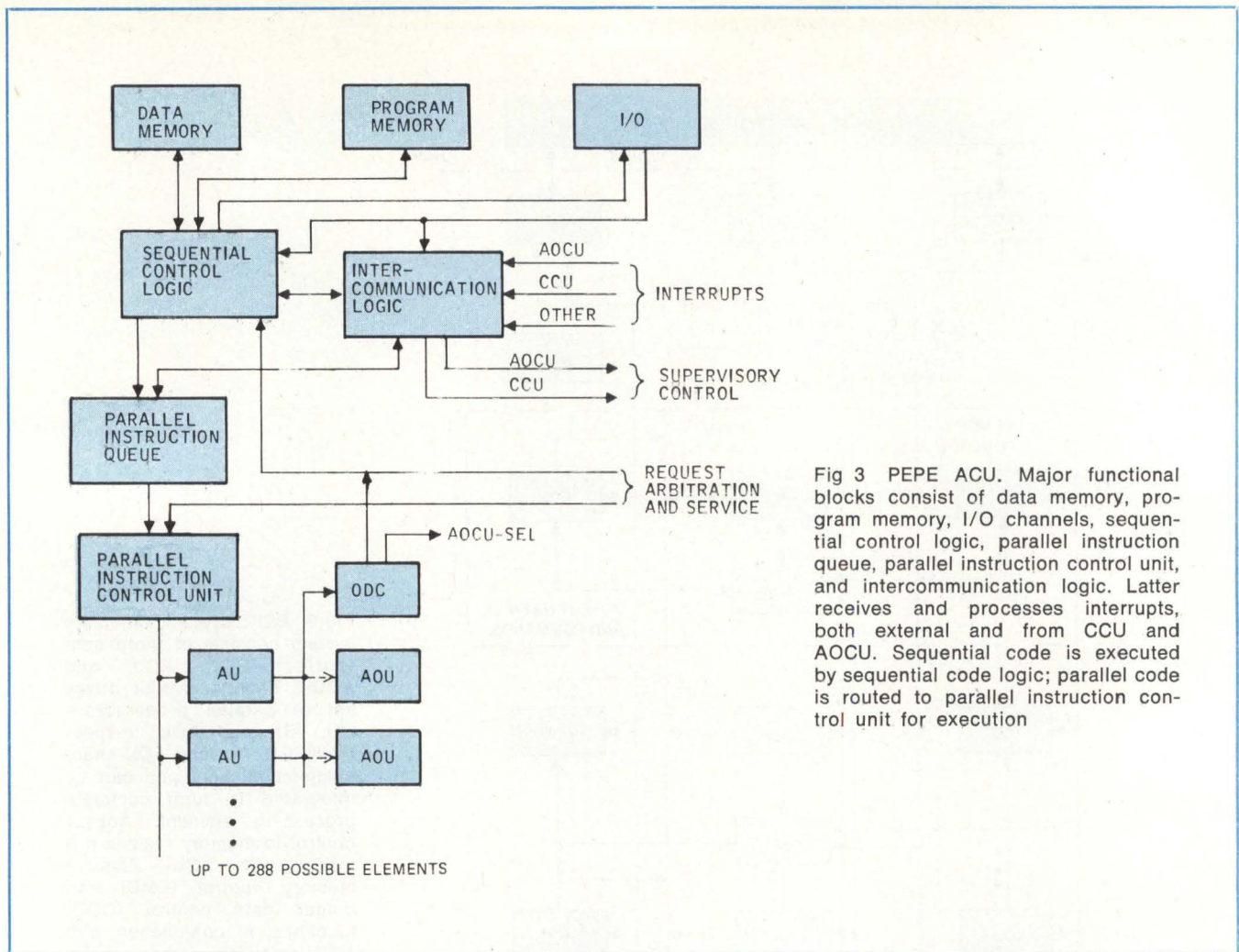


Fig 3 PEPE ACU. Major functional blocks consist of data memory, program memory, I/O channels, sequential control logic, parallel instruction queue, parallel instruction control unit, and intercommunication logic. Latter receives and processes interrupts, both external and from CCU and AOCU. Sequential code is executed by sequential code logic; parallel code is routed to parallel instruction control unit for execution

This last register, in the bit-slice mode, corresponds to a word-select register and, in the word-slice mode, to a data register.

Each processing array has the capability to perform either of the two variable logical functions between registers. STARAN does not have a dedicated serial adder on a per word basis. However, the X and Y registers, using logical functions, appear to have this capability. This cuts the cost of an array, but requires the facility for high speed operation within the X, Y, M register complex.

Each of the 256-word x 256-bit associative arrays includes a 256-bit resolution system. Since the associative processor does not have addresses in the conventional location sense, memory can be viewed as ordered from the top location to the bottom location. To manipulate a specific location, a device is provided that allows the programmer to address the topmost word, which has been identified by the search process as satisfying the specific search criteria. This device is called a multiple match resolution system or responder. Multiple matches can occur because many locations can satisfy the search criteria. Response resolution is a continual process that occurs after every search operation. This process is implemented via a special logic network. Resolution is always occurring in each array, and the system interface is a 9-bit response output.

Eight bits give the address of the first responding location, and the ninth bit is the inclusive-OR of the response register. Thus, eight bits specify the location of the topmost matched word of each 256-word associative array. The ninth bit specifies to the system that the array has a match. By using the ninth bit, the system can then resolve matches between the system's 32 memory arrays, giving STARAN the capability of presenting to the programmer an 8192-word contiguous associative memory system, even though no array is larger than 256 words. A complete STARAN may be composed of up to 32 basic memory arrays (Fig 1).

I/O is not definable for STARAN because each system is unique with regard to I/O requirements. Typical capabilities include direct memory access (DMA) to a host computer, buffered I/O for peripherals, communication through external function logic, and parallel I/O channels into any array. A minicomputer functions as a sequential controller and host for the associative processor controller and associative memory arrays.

Assembly language APPLE* (Associative Processor Procedural Language) has been developed for STARAN. Assemblers for APPLE are custom tailored for the individual machine installation. Few I/O instructions are included in the language, since I/O is also customized for each installation.

*APPLE is a registered trademark of Goodyear Aerospace Corp, Akron, Ohio.

TABLE 1

Comparison of Parallel Processor Capabilities

	PEPE	ILLIAC IV	STARAN
Data Word Size	32 bits	64 bits	256 to 1024 bits
Instruction Word Size	32 bits	32 bits	16 bits
Memory Size	1k bytes/PE	2k bytes/PE	Basic module 256 words of 256 bits; up to 32 modules
Backing Store	In host	Paged to PE	Available per module
Memory Cycle	100 ns	250 ns	100 ns read
Number of Processing Elements	Up to 288	64	1/word of associative memory
Processing Element	32-bit floating point accumulator oriented	64-bit floating point accumulator oriented	Serial adder oriented
Processing Element Complexity	8800 gates	10,000 gates	Serial adder
Microprogrammed	Yes	Yes	Yes
Processing Element Connections	Linear array	4 nearest neighbors	Not convenient (available by data shifting)
Parallel Operation Within Arithmetic Unit	Yes	Yes	No
Associative Addressing	Yes	Pseudo	Yes
High Order Language	PFOR	GLYPNIR	None available
Processing Speed			
Add	300 ns ¹	500 ns ¹	0.85 μ s/bit
Multiply	1.9 μ s ¹	700 ns ^{1,2}	— ³

1. Time for one PE; all PEs may operate in parallel

2. Two operations may complete in this time

3. May be computed as N^2 times 0.85 μ s, where each operand is assumed to consist of N bits.

PEPE System

A parallel element processing ensemble (PEPE) system (Fig 2) comprises processing elements (PEs) designed for ballistic missile radar defense data processing. The system can input data in the correlation control unit/correlation unit (CCU/CU) complex, update tracks in the arithmetic control unit/arithmetic unit (ACU/AU) complex, and output radar control commands through the associative output control unit/associative output unit (AOCU/AOU) complex, simultaneously. The CU and AOU portions of PEPE have facilities which correspond to an associative memory capability for track correlation and track output ordering, respectively.

Since the three complexes are similar in operation, only the ACU/AU complex is described. Execution sequencing consists of an instruction fetch and an instruction evaluation. The result of this process is a machine instruction, which is sent either to the sequential control section for execution on sequential (control unit) variables or to the parallel instruction queue (PIQ) for transmission to the parallel instruction control unit (PICU) for execution as a parallel instruction to operate on variables contained in the parallel operating PEs. The PIQ is invisible to the programmer, while the PICU is microprogrammable. The PEs are hardwired to execute as slaves to the PICU microinstructions.

The ACU sequential control logic section (Fig 3) consists of the following capabilities: accumulator and extension, index, condition, interrupt mode, and I/O buffer registers; the AU has accumulator and extension, arithmetic overflow, double precision carry, element activity, element fault, tag, and activity register capabilities. Processing elements in PEPE use the activity stack concept to support nested control structures from the extended version of Parallel FORTRAN (PFOR) programming that is available. Like STARAN and ILLIAC IV, PEPE operates with a concept of processing element (PE), activity; ie, a processing element is either active (participates in an operation) or is inactive (does not participate). PEPE, however, does not use a single flip-flop to control activity; instead a set of flip-flops in each PE is organized as an activity stack. In addition to normal operational concepts usually associated with activity, the activity flip-flops in a PEPE PE can operate in a last-in first-out (LIFO) stack mode. This idea is referred to as the activity stack in PEPE.

PFOR contains constructs that allow for both sequential (control unit) variable and parallel (PE) variable declarations. Parallel arithmetic and logic expression evaluations are also provided. The PFOR WHERE statement is the parallel analog of the FORTRAN IF. A counting function is available to tally the number of active elements, and to furnish the exact number of matches

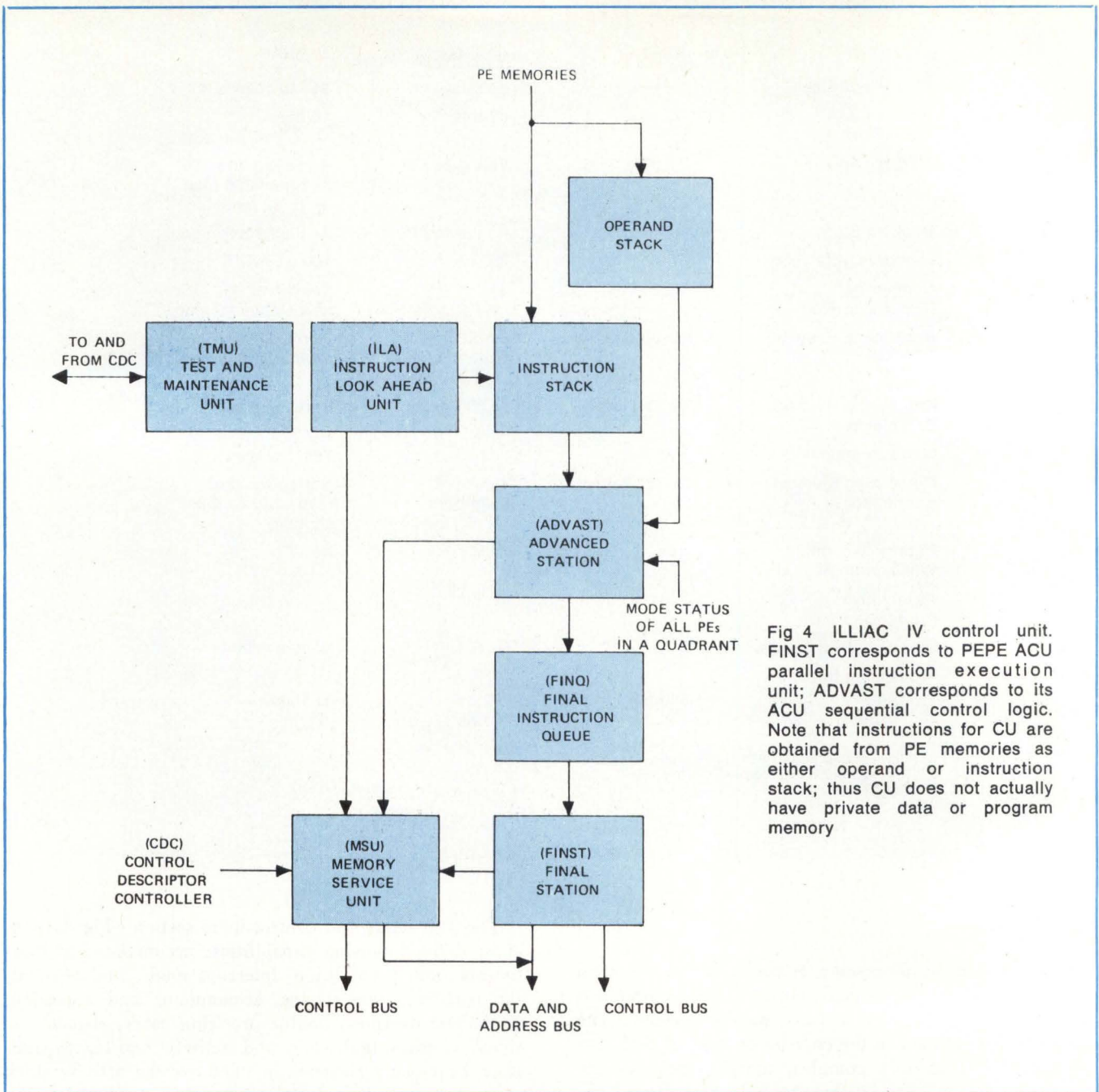


Fig 4 ILLIAC IV control unit. FINST corresponds to PEPE ACU parallel instruction execution unit; ADVAST corresponds to its ACU sequential control logic. Note that instructions for CU are obtained from PE memories as either operand or instruction stack; thus CU does not actually have private data or program memory

and indications of none, one, many, or all in the match indication subsystem. An analogy to the FORTRAN logical IF statement is also provided. Lastly, a parallel DO statement to control sequencing is available. An assembly language—parallel assembly language (PAL)—supports commonality. Each of the six units—ACU, CCU, AOCU, AU, CU, and AOU—is able to execute a subset of PAL, thereby simplifying software problems. To date, two versions of PEPE have been built and benchmarked (Table 1).

ILLIAC IV System

A functional block diagram of the ILLIAC IV control unit (CU) is given in Fig 4 and the processing element (PE) in Fig 5. The CU—composed of five major subsections:

instruction look ahead (ILA), advanced station (ADVAST), final station (FINST), memory service unit (MSU), and test and maintenance unit (TMU)—controls the sequencing of PE quadrants. PEs are interconnected to each of their four nearest neighbors. Originally, ILLIAC IV was conceived to consist of 256 PEs. These were subdivided into groups of 64 elements, four 8 x 8 arrays or quadrants. Only one 8 x 8 quadrant was built. A concept for multiquadrant operation was conceived but not implemented. CU instructions are fetched from PE memories and paged into ILA. Thus, functionally, CU has an instruction memory but, physically, memory is an integral part of the PE quadrant memories. This allows ILLIAC IV programs to be different in separate quadrants and to be fetched from backing storage at the same time that PE data are fetched. Each PE could be viewed as part of a processing unit (PU). A PU could be viewed

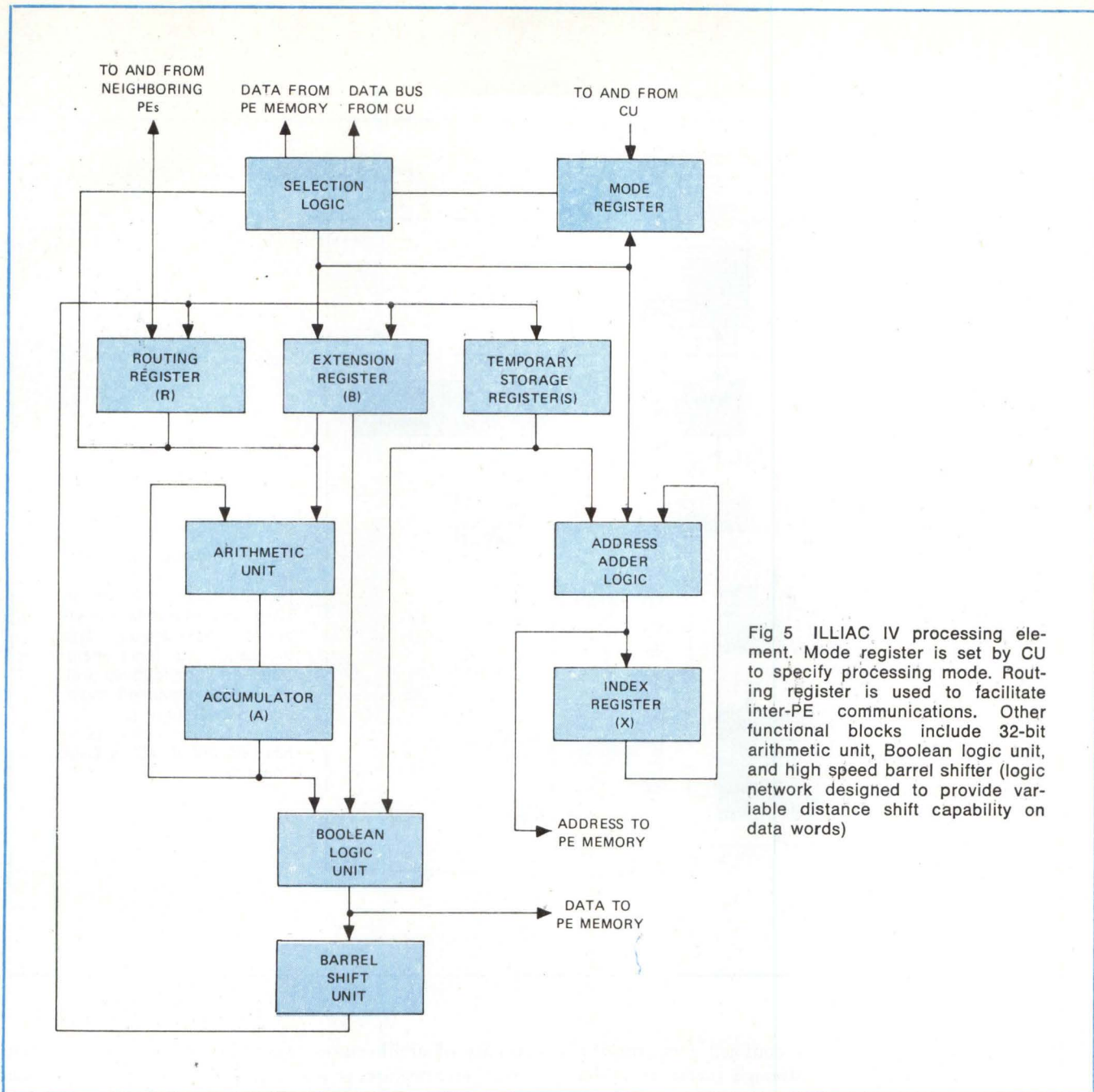


Fig 5 ILLIAC IV processing element. Mode register is set by CU to specify processing mode. Routing register is used to facilitate inter-PE communications. Other functional blocks include 32-bit arithmetic unit, Boolean logic unit, and high speed barrel shifter (logic network designed to provide variable distance shift capability on data words)

as containing memory to hold PE data. Large volumes of data are held on a set of discs used as backing storage for the memory associated with each PU. The CU contains four general purpose accumulators, several control registers, a 64-word scratchpad, and quadrant control registers. The ADVAST subsection examines each instruction and executes sequential instructions. Parallel instructions are decided by FINST and transmitted to PEs for execution.

The processing unit (PU) consists of the PE of Fig 5, its memory (PEM), and the memory logic unit (MLU); the PE contains no control logic. PE registers visible to the programmer are: results register A, activated by PE activity status; operand register B; intermediate storage register C, which is always enabled and used for communication; and intermediate storage register S, which is operable only if PE is active.

Double indexing is possible in ILLIAC IV. Double indexing consists of the ability to index a variable at two locations: once at the control logic level and then at the PE logic level. Importantly, the index value may be different in each PE. A number of higher order languages (TRANQUIL and IVTRAN) have been proposed for ILLIAC IV. The current *de facto* standard appears to be GLYPNIR, an extension of ALGOL. It is block-structured, and provides for both sequential and parallel variable data declarations. Parallel assignment statements are also available. Furthermore, arithmetic capabilities may be controlled with a routing index, which allows the computation to be performed remotely (in another PE) and routed to the currently active PE. GLYPNIR constructs are available to provide dynamic storage allocation, and data declarations allow static storage allocation. Pointers are supplied to support a record-processing capability. Point-

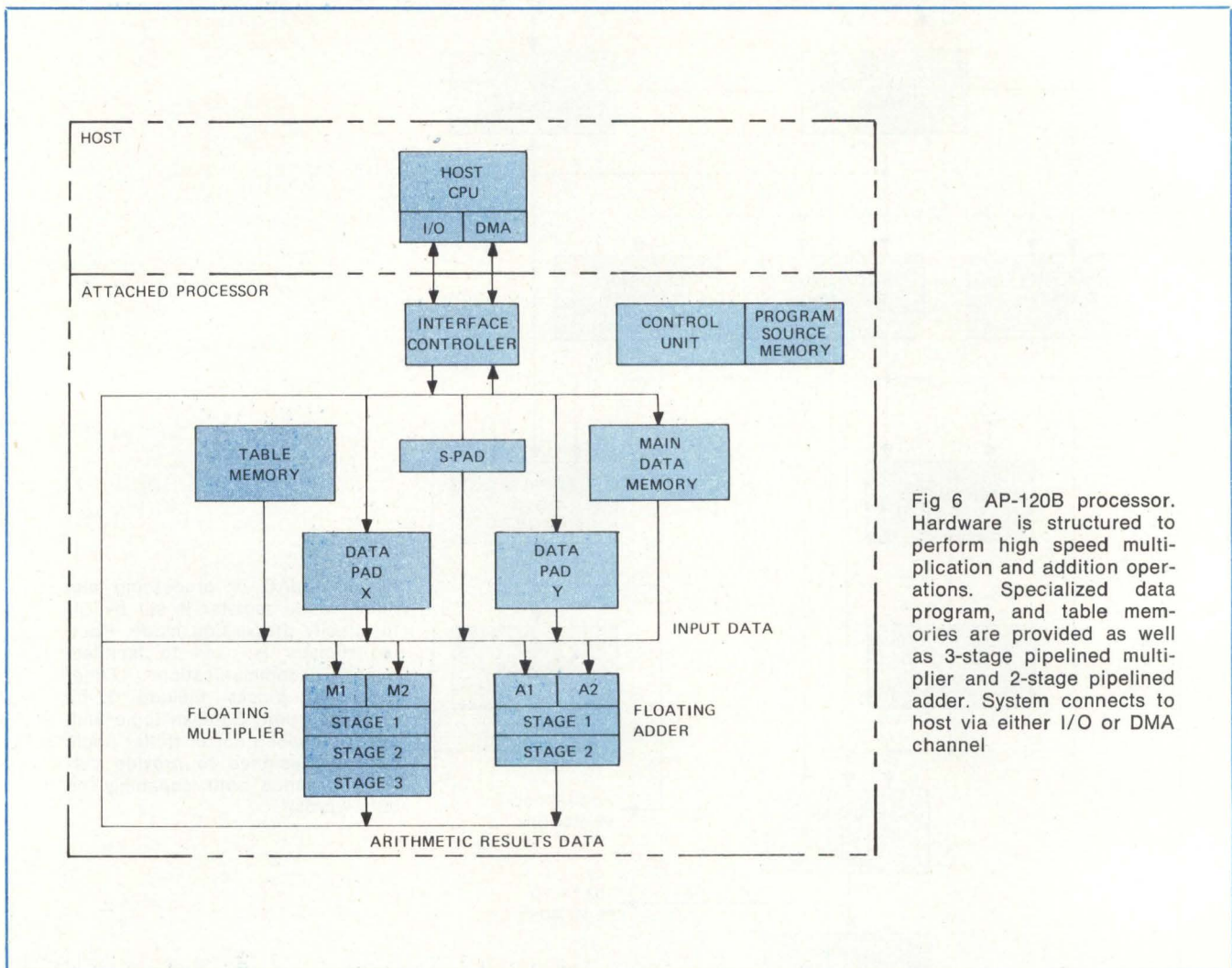


Fig 6 AP-120B processor. Hardware is structured to perform high speed multiplication and addition operations. Specialized data program, and table memories are provided as well as 3-stage pipelined multiplier and 2-stage pipelined adder. System connects to host via either I/O or DMA channel

ers may be vectors and may be confined (PE pointer) or nonconfined (CU pointer). Although ILLIAC IV is designed primarily for matrix processing, it can be programmed to look like a 64-element associative memory.

Special Purpose System Comparison

Architectures and capabilities of STARAN, PEPE, and ILLIAC IV differ substantially (Table 1). STARAN uses bit-serial arithmetic, PEPE uses 32-bit arithmetic, and ILLIAC IV uses 64-bit arithmetic. Both ILLIAC IV and PEPE have high order languages available, but STARAN has only an extensible assembly language. STARAN is designed to operate solely using associative addressing. PEPE uses associative addressing for input (in the CUU/CU complex) and for output (in the AOCU/AOC complex). ILLIAC IV is designed for use of random-access addressing, but can be used also in a pseudoassociative mode. Additionally, it has a high level of PE interconnectivity with PES being connected to their four nearest neighbors. PEPE is arranged in a linear array with limited nearest neighbor communications available. No convenient nearest neighbor connections are available in STARAN. This di-

versity of architectures makes for interesting study, but each architecture is severely limited in its application potential.

Scientific Attached Processors

Although many vendors manufacture scientific processors, the following scientific attached processors have been selected for discussion because of their architectural diversity. Floating Point Systems' AP-120B is a high performance pipeline system containing an addition pipe and a multiplication pipe designed for scientific signal processing applications. Comparable architecturally to AP-120B, the IBM 3838 is designed with a different overall system concept while the basic attached processor is similar. The Data West MATP consists of up to four pipelined processors and, thus, can be viewed as a multiprocessor based attached processor; ie, it is a hybrid multiple instruction multiple data stream/single instruction multiple data stream (MIMD/SIMD) system concept. Consisting of a single instruction multiple data stream (SIMD) oriented system the Burroughs BSP has 17 mem-

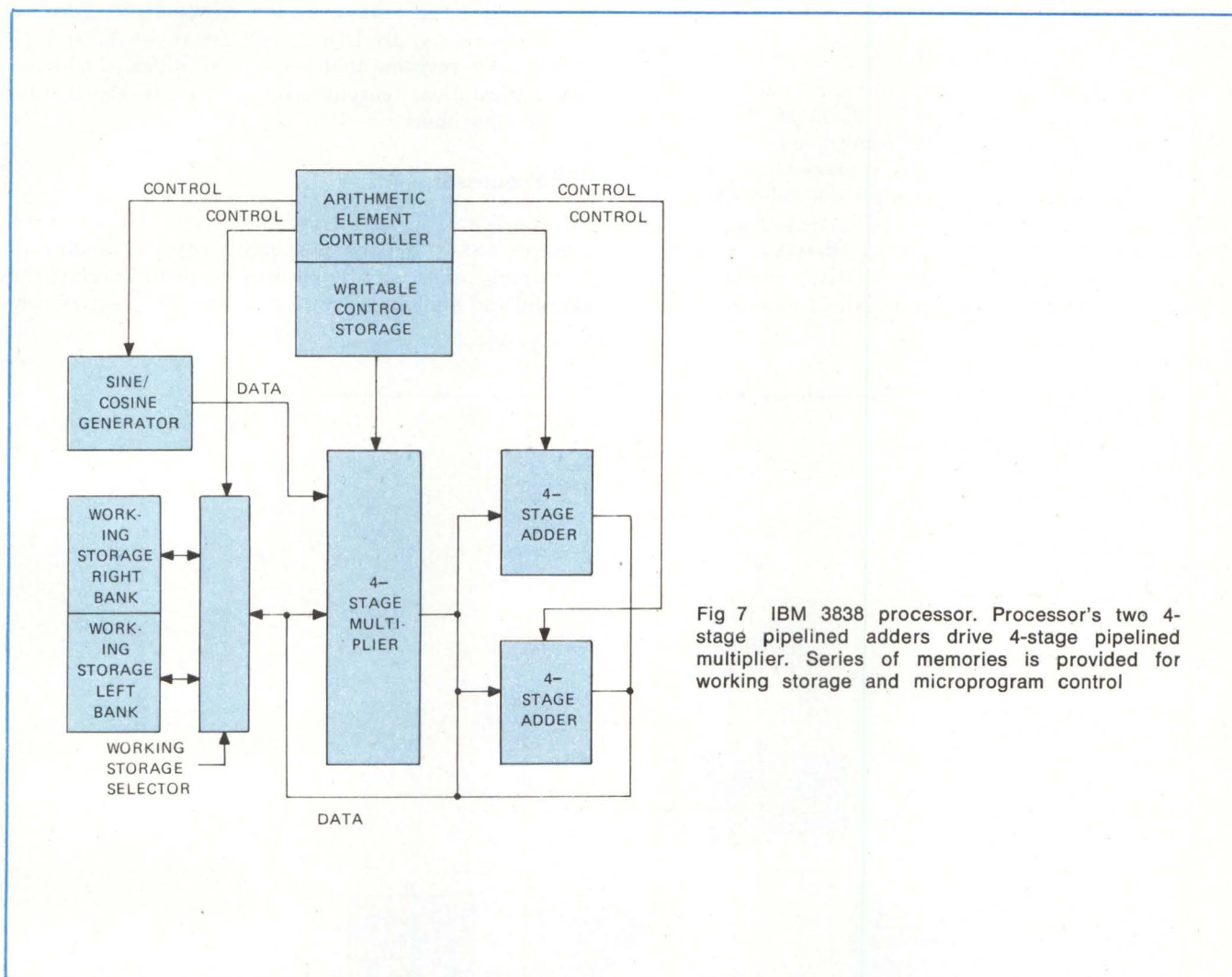


Fig 7 IBM 3838 processor. Processor's two 4-stage pipelined adders drive 4-stage pipelined multiplier. Series of memories is provided for working storage and microprogram control

ory modules with only 16 processors; this alleviates memory access problems for processed data.

AP-120B Processor

A fully parallel, microprogrammable, pipelined, floating point processor, the AP-120B (Fig 6) consists of a 3-stage pipelined adder and a series of scratchpad and data memories. It is interfaced to a host over either an I/O or DMA channel to provide a high performance system oriented toward signal processing. The system's functional hardware is typical of machines of this class. Major functional blocks are control unit containing microprocessor sequencing and data transfer control logic; program source memory made up of writable control store; data pad consisting of two register files totaling 64 registers; floating adder, a 2-stage pipeline capable of executing normalized, convergently rounded operations; floating multiplier, a 3-stage pipeline; S-pad unit consisting of 16 registers, arithmetic logic unit, shift controls, and decimate operator for use in address indexing, counting, and integer arithmetic operations; 64k

words of main data memory; table memory holding roots used to generate real and imaginary numbers needed for fast Fourier transforms; maintenance path; and interface controller. (A more detailed description of the processor's functions can be found in "Array Processor Provides High Throughput Rates," W. R. Wittmayer, *Computer Design*, Mar 1978, pp 93-100.)

3838 Processor

The 3838 is a pipeline scientific processor (Fig 7). It consists of two 4-stage adders and one 4-stage multiplier, as well as a microprogrammable controller and memory. Designed to attach to a System/370 via a block-multiplexer channel, it can transfer information at the rate of 1.5M bytes/s. With an optional 2-byte interface, maximum data rate is 3M bytes/s.

The 3838 appears to the host central processing unit (CPU) and block multiplexer channel as a shared control unit, encompassing a maximum of eight unshared ports. Ports (subchannels) 1 through 7 support separate programmer-defined tasks on a block multiplexing

basis. Subchannel 0 is reserved for the control processor (CP).

MATP Processor

In the MATP Real Time III are from one to four micro-programmable processors (Fig 8). Each of these processors comprises one writable control store and one control processor, which includes a processing unit, an index unit, and a memory map unit. Each index unit has up to 48 general index registers, 16 increment registers, 16 parameter registers, and a special bit-reverse register. Also included is a base register to displace the index values a fixed number of locations. All of these registers

and the processor loop-counter stack can be loaded from the writable control store or from the parameter stack. Each control processor has LIFO stacks of 16 program counter registers, 16 branch address registers, and 16 loop-counter registers that control the different addressing computations encountered in typical signal processing algorithms.

BSP Processor

BSP consists of a control processor (CP), 16 arithmetic elements (AES), a parallel memory (PM) consisting of 17 memory units, an alignment network to interface the AES and PM, a file memory (FM), and a file memory con-

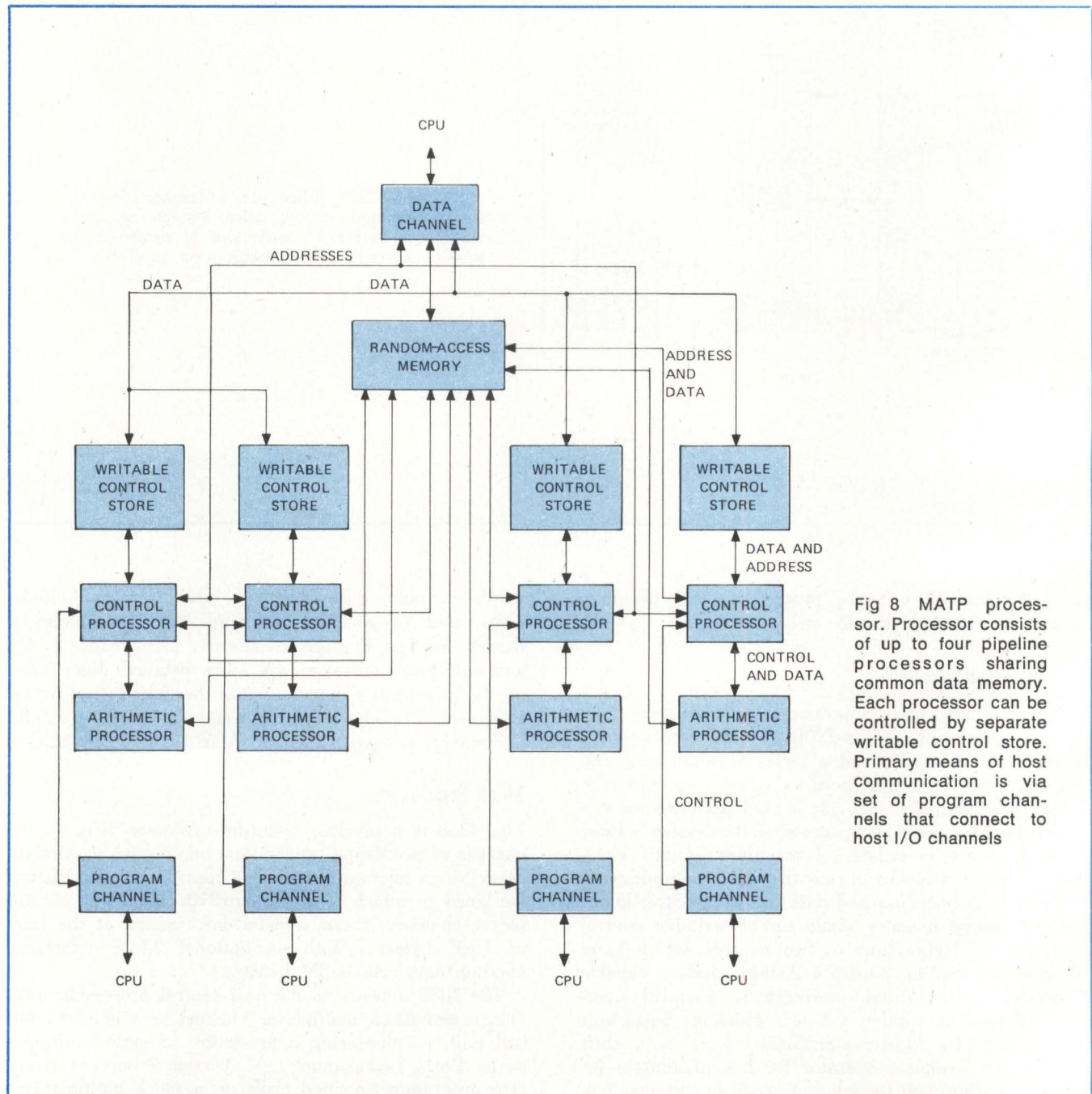


Fig 8 MATP processor. Processor consists of up to four pipeline processors sharing common data memory. Each processor can be controlled by separate writable control store. Primary means of host communication is via set of program channels that connect to host I/O channels

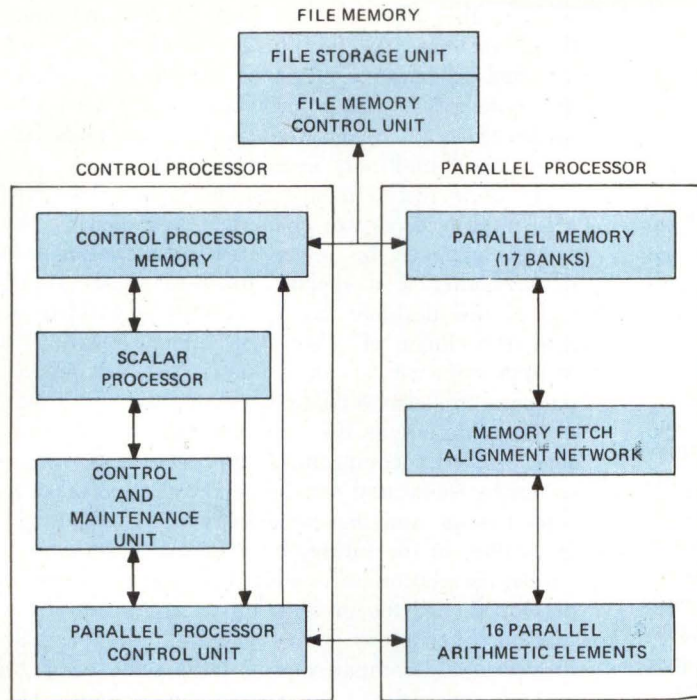


Fig 9 BSP processor. Architecture is unique for scientific attached array processor. One control unit drives 16 arithmetic elements that operate synchronously. These 16 arithmetic elements access subset of 17 memory banks through alignment network. This capability tends to minimize memory access conflicts

TABLE 2
Comparison of Attached Processor Capabilities

	<u>AP-120B</u>	<u>3838</u>	<u>MATP</u>	<u>BSP</u>
Data Word Size	38 bits	32 bits	32 bits	48 bits
Processor	Pipelined	Pipelined	Pipelined	Pipelined
Number of Controllers	1	1	1 to 4	1
Number of Processors	1	1	1 to 4	16
Memory Size	32k to 1M bytes	2 16k-byte sections	65k bytes	500k to 8M bytes
Clock Rate	167 ns	100 ns	100 ns	320 ns
Microprogrammed	Yes	Yes	Yes	Yes
Writable Control Store	Yes	Manufacturer only	Yes	Manufacturer only
Architecture	Pipeline	Pipeline	Pipeline MIMD/SIMD	Pipeline SIMD
Speed ¹	12	30	120 ²	1.5 Scalar ³ 50 Vector
Add	6	20	2 x 40	
Multiply	6	10	40	

1. Speed is theoretical. Peak operation rates are quoted in terms of millions of floating point operations per second
2. Assumes maximum configuration of four processors and controllers
3. BSP PEs do not multiply and add simultaneously; thus speed rating scheme used here does not reveal their best features; it was chosen because it illustrates peak performance from other systems being considered

trol unit (Fig 9). The CP provides for parallel processor control. It consists of a controller, a scalar processor, and a parallel processor control unit.

The parallel processor performs array oriented computations by executing 16 floating-point operations simultaneously in its 16 arithmetic elements. Thus, the architecture of BSP is a SIMD array rather than a pipeline (eg, in comparison to AP-120B or 3838). Data for array operations are stored in a parallel memory. Parallel memory is accessed by the AEs through an alignment network (AN). AEs operate at a clock frequency of 6.25 MHz; more common arithmetic operations are completed within two clock periods.

Scientific Attached Processor Comparisons

Interestingly, the AP-120B, BSP, MATP, and 3838 are all essentially designed as competitors (Table 2); yet, their architectures vary considerably. The BSP provides the most striking contrast. It is a SIMD processor with 16 slaved processors and a single controller. Furthermore, the processors do not have dedicated local memories but, instead, share 17 memories through an alignment network to avoid memory conflicts. The AP-120B, MATP, and 3838 processors are more conservative designs, since they are all basically pipeline processors. MATP uses four pipeline processors in a multiprocessor based configuration; AP-120B and 3838 are single pipeline processors, but each processor has more than one pipeline. The AP-120B has one adder pipe and one multiplier pipe. The 3838, however, has two adder pipes and one multiplier pipe.

Matrix Multiplication on Parallel Processors

A parallel processor's potential performance can be demonstrated by performing matrix type data manipulations. A major computation in many potential applications is matrix multiply. When applying high performance processors to such tasks, design of both hardware and software systems is extremely application dependent.* In many cases nonstandard algorithms must be developed to ensure adequate system performance.¹¹

Examples of these are the algorithm derived by Cannon¹² to multiply two $n \times n$ matrices together in n stages using a parallel processor with multiple PEs, each containing three registers and each interconnected to its four nearest neighbors. Analysis and simulation of matrix operations on a paged pipeline processor has been performed by Elshoff.¹³ His findings resulted in formulation of three rules that may be applied to properly set up matrices for processing in a least recently used paged environment on a pipelined processor.

Summary

Very high performance parallel processors provide a richness of architectural concepts that range in application suitability from general purpose computing to special purpose vector or associative oriented problems. This discussion of parallel processing concepts covers

several existing large scale systems, summarizing major architectures. The systems can be classified into four major categories: multiprocessors, pipeline and functional systems, special purpose systems, and scientific attached systems. Generic multiprocessor systems are distinguished by their processor interconnection technique and can be grouped as common bus, crossbar switch, and multiport memory system.

No clear distinctions exist as far as surveyed large scale architectures are concerned. Almost any available architecture can be interpreted as more advantageous than another if a specific problem subset is selected. Unless the designer has a definitive problem solving goal, the choice of relevant architecture will be an indistinct solution to an arduous task. Definitive comparisons are also difficult because computer capabilities are as different as the originally intended applications. The preferred compromise approach is to group machines by intent and capability and then to make specific comparisons and benchmarks within a limited class. Hopefully, in the future, investigative techniques for accurate correlation of widely varying machines will be developed. For the present, broad architectural and performance variations should constrain designers to carefully evaluate comparisons of large scale computers.

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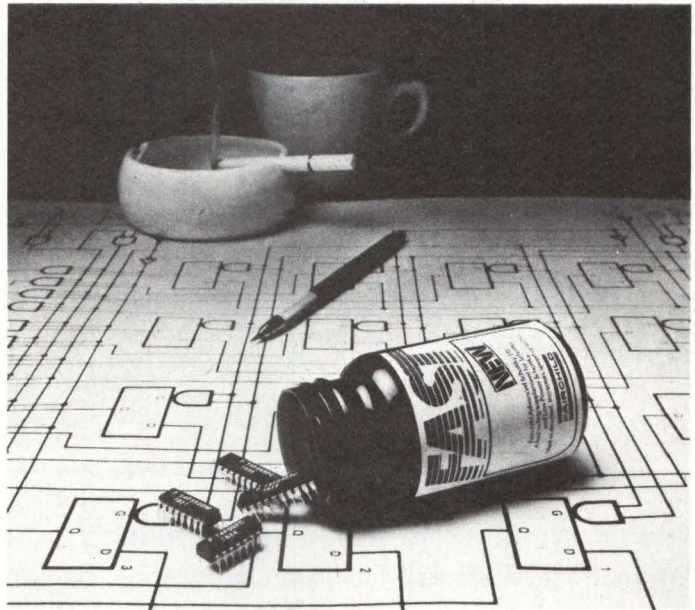
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74F04PC	2.5	2.7
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Disc File Actuator Design Permits Increased Track Density

A dual-structured disc file actuator design incorporating coarse and fine location positioners for precise long and short travel excursions, respectively, fulfills accuracy and reliability requirements imposed by narrow-track discs

Rudolf W. Lissner, David H. McMurtry, and Richard A. Wilkinson
International Business Machines Corporation, San Jose, California

A disc file actuator must position a magnetic head across the surface of a disc quickly, to minimize central processing unit wait time, and accurately, on a magnetic track that has a width approaching 0.001" (0.0254 mm). Since disc bearings have minute high frequency vibrations, the servo must drive the actuator to compensate for these vibrations. As track widths get increasingly narrow, the mass of a large actuator limits its ability to follow these vibrations. Actuator ball bearing inconsistencies, which were less noticeable in low track density machines, become problems in high track density machines.

To increase track density on magnetic discs, accurate servo operation of the linear actuator is needed. However, the ball bearings normally

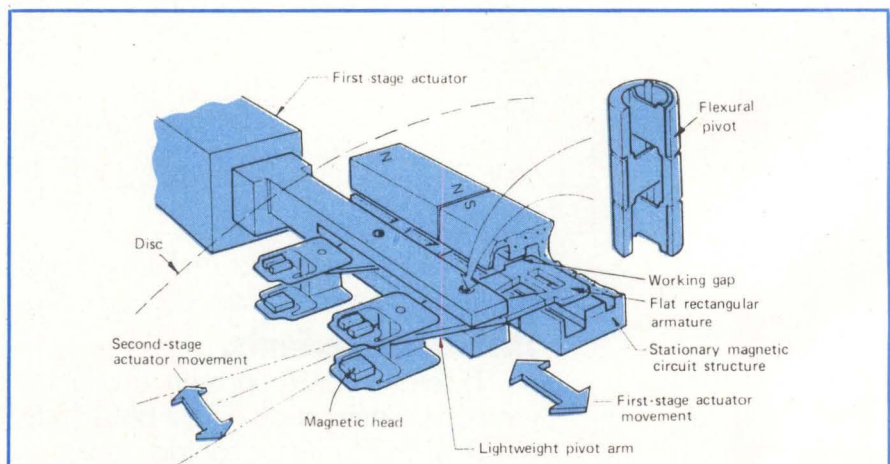
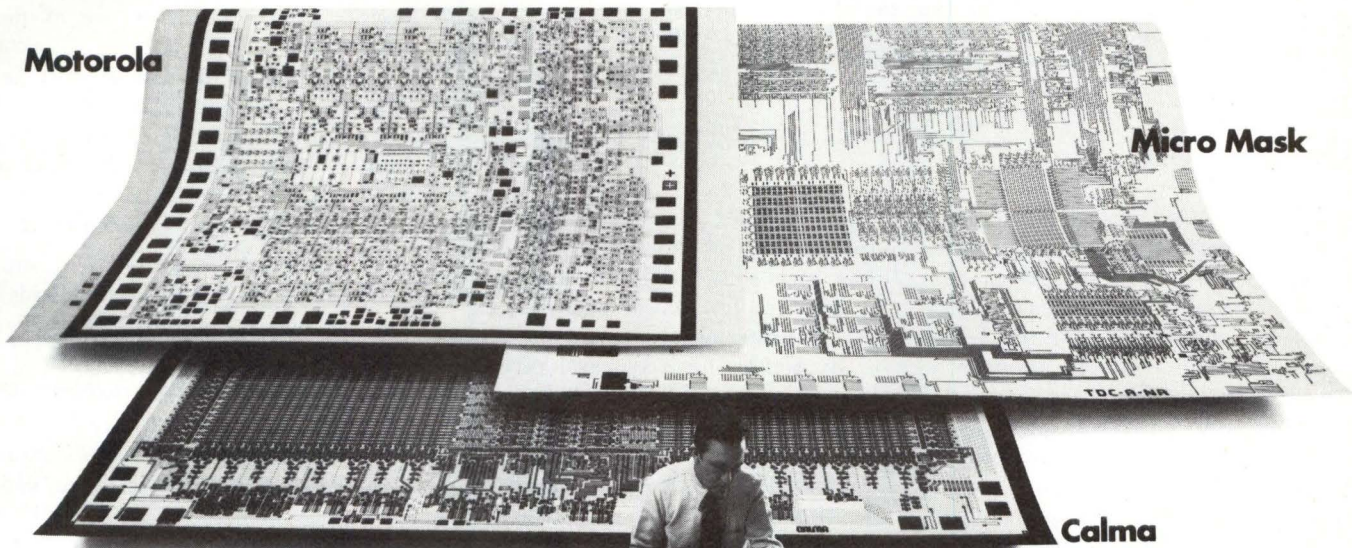


Fig 1 Two-stage disc file actuator design. While moving magnetic heads to specified track, first-stage actuator carries second-stage actuator linearly to coarse position. Then, second-stage actuator pivots to designated track

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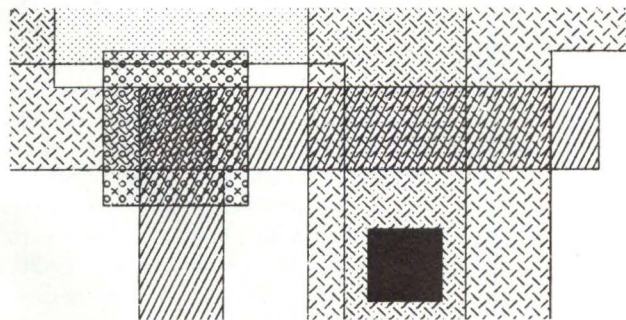


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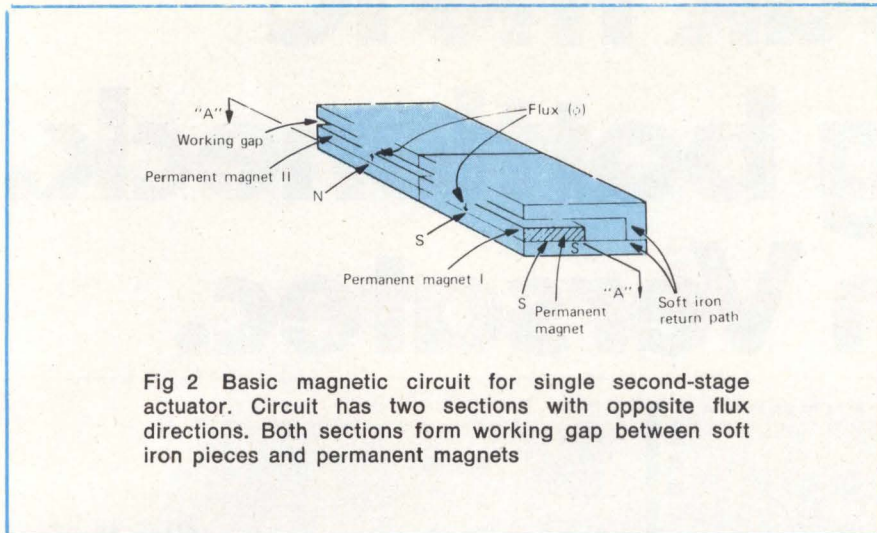


Fig 2 Basic magnetic circuit for single second-stage actuator. Circuit has two sections with opposite flux directions. Both sections form working gap between soft iron pieces and permanent magnets

used to support the actuator have marginal performance characteristics over the short linear excursion necessary to keep the magnetic head precisely positioned on the disc track. A solution to this problem is to support these linear excursions by a Bendix Flexural™ Pivot. Several technologies, such as piezoelectric and magnetoresistive, were considered for the second-stage actuator, but were rejected because they required high voltage or high current

and exhibited an undesirable hysteresis effect. A voice coil technology has been considered attractive since it requires low power and has negligible hysteresis.

By combining a Flexural pivot, a voice coil actuator for short excursions, and coarse mover for long excursions, a disc file actuator system can be designed that will minimize bearing static friction (stiction) and lighten the moving mass for small, precise, track-to-track motions.

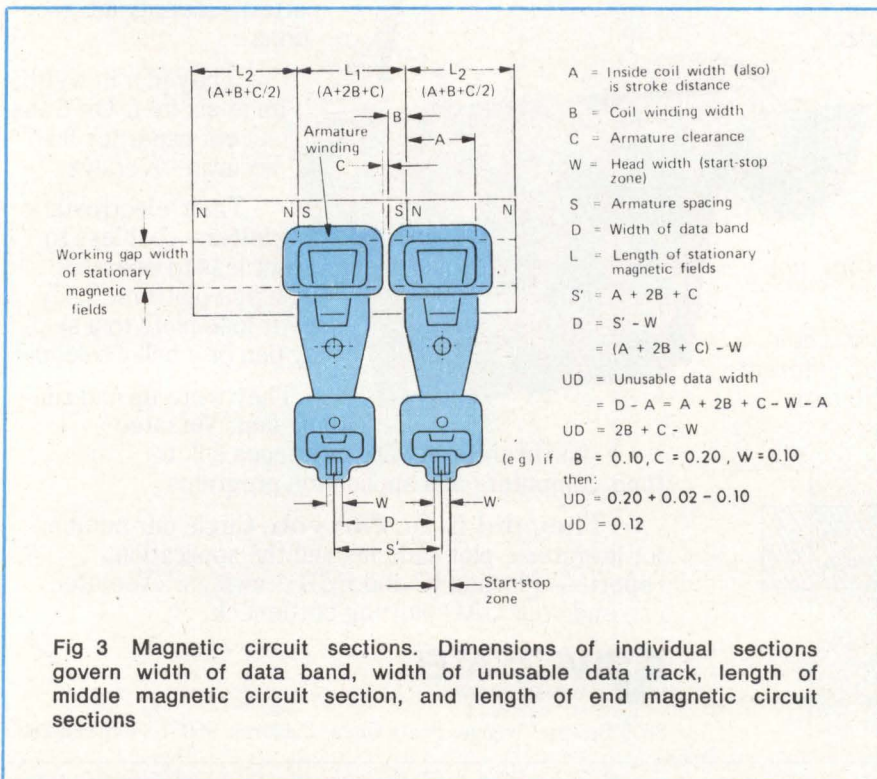


Fig 3 Magnetic circuit sections. Dimensions of individual sections govern width of data band, width of unusable data track, length of middle magnetic circuit section, and length of end magnetic circuit sections

Actuator Design

A 2-stage actuator design has been evolved in conjunction with a servo concept in which a 2-layer disc contains both servo and data information. The servo information is permanently written directly beneath the data. The servo head and the data head are mounted on a common slider that flies over the rigid disc surface. This actuator concept applies equally well for servo information alternated with data in discrete sectors on the same surface of the disc.

The coarse or first-stage (F-s) actuator can be a standard voice-coil actuator, a linear stepping motor, or another linear actuator. The fine or second-stage (s-s) actuator consists of the following components (Fig 1):

- (1) a lightweight pivot arm supporting a magnetic head (or heads) on one end and a flat rectangular coil on the other,
- (2) a Flexural pivot providing the rotation axis, and
- (3) a shielded magnetic structure mounted to the machine frame cantilevered between the discs. This core has a slit gap containing the flat rectangular coil. The magnetic structure is segmented into discrete magnets with alternating polarity. The two driving legs of the rectangular coil are within the gaps of the adjacent magnets.

The s-s actuator is unique in that the armature neither is attached nor has a fixed relationship to the magnetic circuit. The magnetic circuit that provides the working gap is fixed in place; hence, it is not part of the F-s actuator moving mass.

During a seek operation, the F-s carriage holding the s-s actuator is coarse positioned, causing the flat rectangular coil to move linearly like a generator in a magnetic field (a torsional unbalance force would be created). In this case, the coil is prevented from generating current by solid-state circuits or by opening the circuit (disc file logic control). After reaching the final coarse position, current is applied to the coil, causing the arm to pivot. The head can be positioned over approximately 20 tracks, and the track-following-disc runout is monitored by the servo position error signal.

The Flexural pivot is a commercial unit capable of limited rotation about one axis with high stiffness in other directions. Several sizes of pivots were tested to determine their stiffness about the two rotational axes and in the two translational directions lying in the plane of the armature. These values were used in a NASA Structural Analysis (NASTRAN) finite element structural model of the armature to determine natural frequencies and vibration mode shapes. Angular excursion of the 0.25" (0.635-cm) diameter pivot is $\pm 1^\circ$ for the configuration described. Published data indicate a fatigue life of $>0.94 \times 10^9$ cycles for a 0.25" (0.635-cm) pivot flexing $\pm 9^\circ$.* It is considered that this reliability criterion will be adequate for the life of the machine. Center shift caused by $\pm 1^\circ$ of rotation is only 0.25 μ in (63.5 μ m) in the access direction.

Magnetic Circuits And Structures

The basic magnetic circuit for an s-s actuator. (Fig 2) consists of two circuit sections with opposite flux directions. These two magnetic circuit sections form the working gap for one s-s actuator.

Fig 3 shows section A-A of Fig 2 in detail, with two s-s actuator armatures utilizing three magnetic circuit sections. The length of the magnetic circuit sections required is determined by the maximum stroke or travel of the F-S actuator, the width of the armature winding, and the amount of movement of the s-s actuator.

A shielded magnetic circuit section is shown in Fig 4. The secondary gap formed by the shielding is at essentially the same potential, and flux flow in this gap is negligible. Bandwidth limitations of the s-s actuator can be improved by customary techniques, such as shorted turns and specific magnetic circuit material. The torque (T) developed by a device using this magnetic circuit is approximated by

$$T \cong 0.1 N L_{eff} I_a r (Bg_1 + Bg_2) \text{ dyne-cm}$$

where

N = number of windings

Bg = working gap flux densities (gauss)

L_{eff} = length of each winding within each working gap flux (cm)

I_a = applied current (amperes)

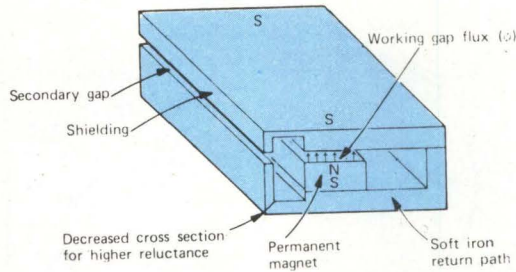
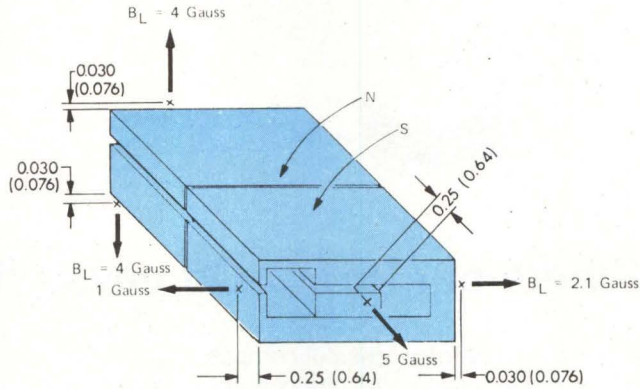


Fig 4 Shielded magnetic circuit section. Stray field shielding, which is important in magnetic recording, is provided by high-reluctance reduced-cross-section flux path, which also forms secondary gap



DIMENSIONS ARE IN INCHES (CM)

Fig 5 Leakage measurements. Typical dimensions for magnetic circuit section yield low stray flux densities (B_L). Therefore, second-stage actuator can be located close to magnetic media without erasure complications

r = distance from center of rotation to center line of working gap (cm)

(Bg_2) in an adjacent circuit section,

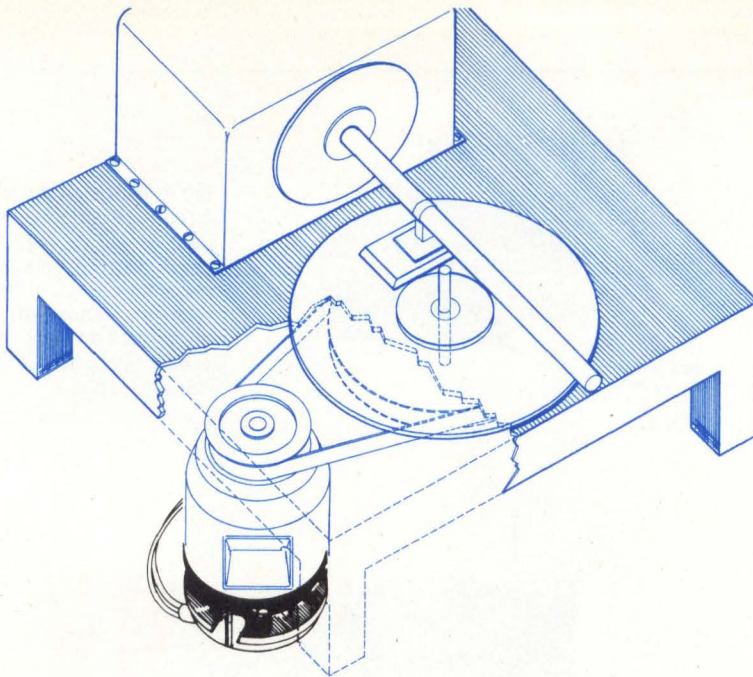
$$T \cong 0.2 N L_{eff} I_a Bg r \text{ dyne-cm}$$

If the working gap density (Bg_1) in a single magnetic circuit section equals the working gap flux density

*J. L. Olson, "The evaluation of flexural pivots to meet critical performance and life requirements," ASME 70-DE-76, 1976

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See page 81



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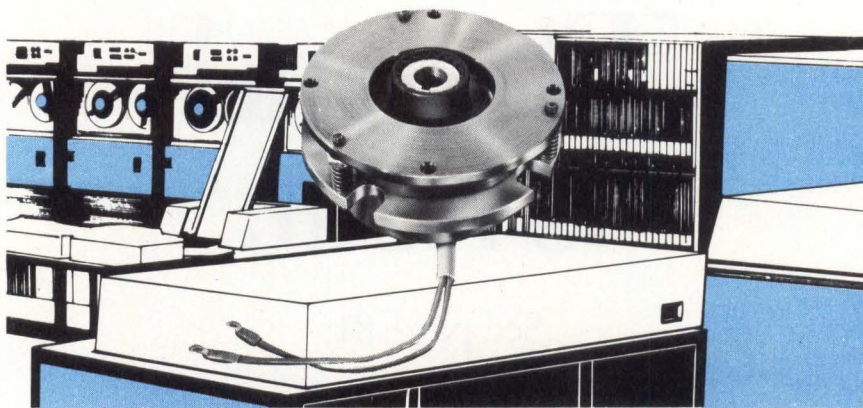
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Several variations on the basic magnetic structure are possible. Magnetic structures that include pole pieces to focus the flux in the working gap will reduce the effective winding required by an amount proportional to the increase in flux density and will still develop the same torque. The magnetic circuit can also use an electromagnetic field coil to furnish magnetic flux in the working gap.

Various permanent magnets, such as Alnico alloys, rare earth, platinum, and cobalt can be used to supply working gap flux. In general, the specific application with its space and bandwidth requirements will dictate which material is best suited. Permanent magnets with high intrinsic coercivity values will result in a flat magnetic structure, while the use of Alnico alloys, for example, would result in a higher structure because of the greater magnet length required.

The use of an s-s actuator close to magnetic media, such as magnetic discs and tape drivers, would not cause erasure problems. Fig 5 shows a magnetic circuit section with measured stray field magnitudes. As shown, the maximum stray flux is only about 2 gauss above the maximum ambient value of 3 gauss.

Summary

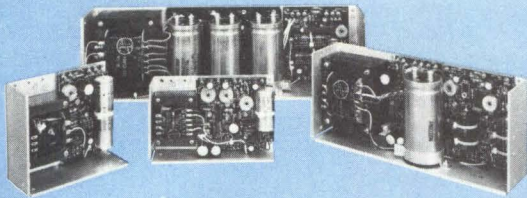
The 2-stage disc file actuator design concept has several outstanding capabilities: (a) the Flexural pivot has no stiction phenomenon to cause servo instabilities; (b) servo bandwidth is improved, thereby permitting the second-stage actuator to track-follow higher frequency runouts; (c) the first-stage actuator moving mass is not significantly increased over existing voice coil motor designs since the second-stage magnet structure is stationary; and (d) the linear motion of the coarse (first-stage) actuator will not excite rotational natural frequencies of the fine (second-stage) actuator, since the center of actuator mass is at the pivot point.

These capabilities combine to produce an actuator which, in concert with the dual-layer disc servo concept, could result in a high track density disc file. □

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5	3.0	B5-3	\$24.95	12	1.7	B15-1.5	\$24.95	18	1.3	B24-1.2	\$24.95	24	1.2	B24-1.2	\$24.95
	6.0	C5-6	44.95		3.4	C15-3	44.95		2.6	C24-2.4	44.95		2.4	C24-2.4	44.95
	12.0	D5-12	74.95		6.8	D15-6	74.95		5.2	D24-4.8	74.95		4.8	D24-4.8	74.95
	18.0	E5-18	104.95		10.2	E15-9	104.95		7.8	E24-7.2	104.95		7.2	E24-7.2	104.95
6	3.0	B5-3	\$24.95	15	1.5	B15-1.5	\$24.95	20	1.3	B24-1.2	\$24.95	—	—	—	—
	6.0	C5-6	44.95		3.0	C15-3	44.95		2.6	C24-2.4	44.95		—	—	—
	12.0	D5-12	74.95		6.0	D15-6	74.95		5.2	D24-4.8	74.95		—	—	—
	18.0	E5-18	104.95		9.0	E15-9	104.95		7.8	E24-7.2	104.95		—	—	—

SINGLE OUTPUT — HI-VOL

115/230 VAC INPUT • OVP ON 5V MODELS

VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9
2	3.0	HB2-3	\$29.95	12	0.5	HA15-0.5	\$22.95	24	1.2	HB24-1.2	\$24.95	48	0.5	HB48-0.5	\$29.95
	6.0	HC2-6	49.95		1.7	HB12-1.7	24.95		2.4	HC24-2.4	44.95		1.0	HC48-1	49.95
	12.0	HD2-12	79.95		3.4	HC12-3.4	44.95		3.6	HN24-3.6	64.95		3.0	HD48-3	79.95
	18.0	HE2-18	109.95		5.1	HN12-5.1	64.95		4.8	HD24-4.8	74.95		4.0	HE48-4	109.95
5	1.2	HA5-1.2/OVP*	\$22.95	15	0.5	HA15-0.5	\$22.95	28	1.0	HB24-1.2	\$24.95	180, 200	0.12	HB200-0.12	\$34.95
	3.0	HB5-3/OVP*	24.95		1.5	HB15-1.5	24.95		2.0	HC28-2	44.95				
	6.0	HC5-6/OVP*	49.95		3.0	HC15-3	44.95		3.0	HN28-3.0	64.95				
	9.0	HN5-9/OVP*	69.95		4.5	HN15-4.5	64.95		4.0	HD28-4	74.95				
	12.0	HD5-12/OVP*	79.95		6.0	HD15-6	74.95		6.0	HE28-6	104.95				
	18.0	HE5-18/OVP*	114.95		9.0	HE15-9	104.95		—	—	—				

SINGLE OUTPUT — HIGH POWER

115/230 VAC INPUT • OVP ON 5V MODELS

VOLTS	AMPS	MODEL	PRICE 1-9
5	25.0	F5-25/OVP*	\$149.00
	35.0	G5-35/OVP*	185.00
12	16.0	F15-15	\$149.00
15	15.0	F15-15	\$149.00
24	12.0	F24-12	\$149.00
28	10.0	F24-12	\$149.00

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	12	63%		
	15	60%		
5	14	63%	RE5-23/OVP*	\$130.00
	18	60%		
	23	57%		
5	25	63%	RG5-40/OVP*	\$220.00
	32	60%		
	40	57%		

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BB15-1.5	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A	\$53.95
CC15-3.0	12V @ 3.4A or 15V @ 3.0A	-12V @ 3.4A or -15V @ 3.0A	\$84.95

DUAL OUTPUT — HI-VOL

115/230 VAC INPUT • OVP ON 5V MODELS

MODEL	OUTPUT #1	OUTPUT #2	PRICE 1-9
±12 to 15V			
HAA15-0.8	12V @ 1.0A or 15V @ 0.8A	-12V @ 1.0A or -15V @ 0.8A or -5V @ 0.4A	\$39.95
HBB15-1.5	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A	49.95
HCC15-3.0	12V @ 3.4A or 15V @ 3.0A	-12V @ 3.4A or -15V @ 3.0A	79.95
±18 to 24V			
HAA24-0.6	18-20V @ 0.4A or 24V @ 0.6A	(-)18-20V @ 0.4A or -24V @ 0.6A	\$39.95
±5V			
HBB5-3/OVP	5V @ 3.0A*	-5V @ 3.0A*	\$61.95
HCC5-6/OVP	5V @ 6.0A*	-5V @ 6.0A*	92.95
5V and 9-15V (Isolated Outputs)			
HAA512	5V @ 2.0A*	9-15V @ 0.5A	\$44.95
HBB512	5V @ 3.0A*	9-15V @ 1.25A	54.95
HCC512	5V @ 6.0A*	9-15V @ 2.5A	86.95

TRIPLE OUTPUT — STANDARD

TRACKING REGULATORS • ±.02% REGULATION

MODEL	OUTPUT #1	OUTPUT #2	OUTPUT #3	PRICE 1-9
BAA-40W	5V @ 3.0A	12V @ 1.0A or 15V @ 0.8A	-12V @ 1.0A or -15V @ 0.8A	\$ 69.95
CBB-75W	5V @ 6.0A	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A	\$ 91.95
DBB-105W	5V @ 12.0A	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A	\$126.95

TRIPLE OUTPUT — HI-VOL

115/230 VAC INPUT • OVP ON 5V MODELS

MODEL	OUTPUT #1	OUTPUT #2	OUTPUT #3	PRICE 1-9
HTAA-16W	5V @ 2.0A*	9-15V @ 0.4A	(-)9-15V @ 0.4A or -5V @ 0.2A	\$ 49.95
HBAA-40W	5V @ 3.0A*	12V @ 1.0A or 15V @ 0.8A	-12V @ 1.0A or -15V @ 0.8A or -5V @ 0.4A	\$ 69.95
HCBB-75W	5V @ 6.0A*	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A	\$ 91.95
CP-131	5V @ 8.0A*	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A	\$110.00
HDBB-105W	5V @ 12A*	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A	\$126.95
HDCC-150W	5V @ 12A*	12V @ 3.4A or 15V @ 3.0A	-12V @ 3.4A or -15V @ 3.0A	\$149.00

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Software Error Checking Procedures For Data Communication Protocols

Digital data integrity of two IBM communications protocols is assured by software generation of cyclic redundancy check bits in a micro-processor based communications controller

J. Wong, W. Kolofa, and J. Krause

Motorola Display Systems, West Chicago, Illinois

Cyclic redundancy check bits are employed for error detection in nearly all synchronous data communications. The bits are often generated through hardware in host computers, and their calculations are often protocol-dependent. With a software approach, a general purpose hardware interface can handle all synchronous mode data communications; modifications will accommodate protocol-dependent characteristics dictated by host computers.

Mathematical techniques and hardware circuits show how microprocessor software emulates hardware calculations. This software method for generating and calculating cyclic redundancy check (CRC) bits was developed for a M6800 based controller that is part of a multidrop network. Remote stations in the network communicate with the mainframe accord-

ing to IBM's binary synchronous communications (BSC) protocol.¹ This method also can be applied to CRC calculations for synchronous data link control (SDLC) protocol.²

Hardware Method

An n-bit data block to be transmitted is treated as a binary polynomial of the following form:

$$M(X) = b_n + b_{n-1}X + b_{n-2}X^2 + \dots + b_1X^{n-1} + b_0X^n \quad (1)$$

where b_n represents the nth bit position in the outgoing data block, b_0 being the least significant bit (LSB). Prior to transmission, data polynomial $M(X)$ is divided by constant generator polynomial $G(X)$ of degree k , resulting in quotient polynomial $Q(X)$ and remainder polynomial $R(X)$:

$$\frac{X^k M(X)}{G(X)} = Q(X) + \frac{R(X)}{G(X)} \quad (2)$$

Remainder polynomial $R(X)$, known as the CRC bits, is appended to the data block for transmission to or from the remote station. Upon arrival of the data block and associated CRC bits, the receiver regenerates the CRC bits and compares them with those received. If the comparison is not equal, the received data block is assumed to be in error, and retransmission is requested. Note that the CRC bits do not provide enough information for forward error correction at the receiver, so that retransmission is always required.

Hardware CRC bit generation uses special purpose integrated circuits (ICs), such as the MC8503 16-bit universal polynomial generator. This bipolar LSI circuit is capable of generat-

ing CRC bits based on one of the following generator polynomials:

$$X^{16} + X^{15} + X^2 + 1 \text{—BSC protocol}$$

$$X^{16} + X^{14} + X + 1$$

$$X^{16} + X^{12} + X^5 + 1 \text{—SDLC protocol}$$

$$X^{16} + X^{11} + X^4 + 1$$

A divider circuit (Fig 1)—consisting of a k-stage shift register with feedback connections and Exclusive-OR gates—generates a k-bit CRC corresponding to the polynomial

$$G(X) = 1 + G_1X + G_2X^2 + \dots + G_{k-1}X^{k-1} + X^k \quad (3)$$

Main advantage of the hardware approach to CRC calculations is that it does not require processor time. Unburdened of these calculations, the microprocessor is free to handle higher data rates or more synchronous ports. This approach also provides a small saving in memory, approximately 50 bytes. Major limitation of the hardware approach is that it is not flexible enough to satisfy all the rules imposed on CRC calculations by different host computers. Furthermore, it requires separate ICs to perform the CRC calculations for each synchronous port. Therefore, the increase in hardware cost is proportional to the number of synchronous ports required by the system.

Software Method

Main advantage of the software approach to CRC bit generation is flexibility; programs can be easily modified to satisfy different protocols. Unlike the hardware approach, only one CRC software routine is required for all synchronous ports. However, processor time must be allocated to handle the maximum data rate for CRC calculations performed by software.

For 8-bit Extended Binary Coded Decimal Interchange Code (EBCDIC) transmission using BSC protocol, CRC bits are generated by the polynomial $G(X) = X^{16} + X^{15} + X^2 + 1$ (4) referred to as CRC-16.

The divider circuit for Eq (4) is shown in Fig 2. Assume that the data block consists of two hexadecimal bytes: F0 (first byte) and 26 (second byte).

$$\begin{array}{cccc} \frac{2}{0010} & \frac{6}{0110} & \frac{F}{1111} & \frac{0}{0000} \\ \text{MSB (X}^9\text{)} & & & \text{LSB (X}^{15}\text{)} \end{array}$$

The data polynomial, constructed using Eq (1), is

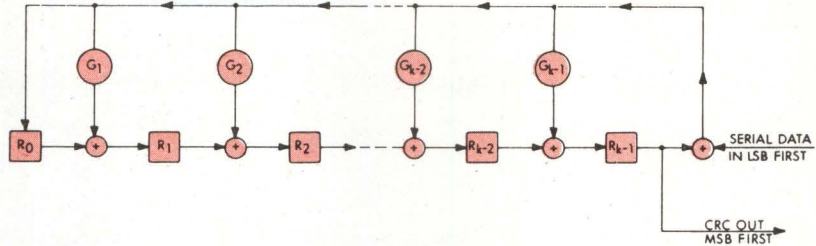


Fig 1 Divider circuit for CRC accumulation based on generator polynomial of Eq (3). Exclusive-OR is performed between incoming data bit and R_{k+1} of CRC accumulator. Result T is shifted into R_0 position, causing every $R+$ to be replaced by R_i , where i is any number between 1 and $k-1$. If G_i is nonzero, Exclusive-OR between T and R_{i-1} is performed before CRC accumulator is shifted

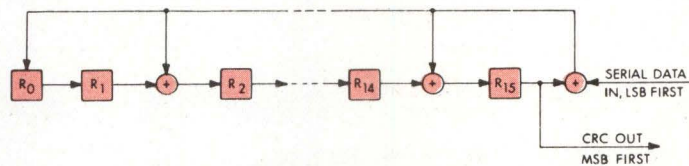


Fig 2 Divider circuit for generating CRC-16 [Eq (4)] for BSC protocol. Exclusive-OR is performed between incoming data bit and R_{15} of CRC accumulator. Result T is shifted into R_0 position. Exclusive-ORs between T and R_1 and between T and R_{14} are also performed before CRC accumulator is shifted

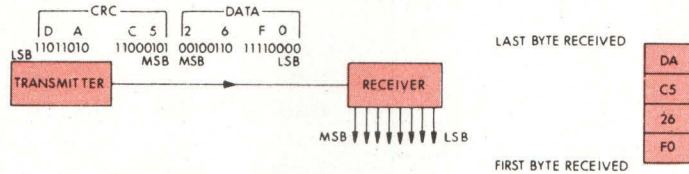


Fig 3 Data and CRC bit transmission/reception. Diagram depicts how message bytes 26F0₁₆ and associated CRC bytes DAC5₁₆ are transmitted and received. Note that calculated CRC bits at transmitter are (MSB) 1010 0011 0101 1011 (LSB), with MSB transmitted first

$$M(X) = X^2 + X^5 + X^6 + X^8 + X^9 + X^{10} + X^{11} \quad (5)$$

To calculate CRC-16, the data polynomial is multiplied by X^{16} , arranged in descending exponential order, and then divided by generator polynomial $G(X)$:

$$\begin{aligned} \frac{X^{16}M(X)}{G(X)} &= \frac{X^{27} + X^{26} + X^{25} + X^{24} + X^{23} + X^{22} + X^{21} + X^{20}}{X^{16} + X^{15} + X^2 + 1} \\ &= (X^{11} + X^9 + X^6 + X^2 + X + 1) + \\ &\quad \frac{X^{15} + X^{14} + X^9 + X^8 + X^6 + X^4 + X^3 + X + 1}{X^{16} + X^{15} + X^2 + 1} \quad (6) \end{aligned}$$

The remainder polynomial $(X^{15} + X^{13} + X^9 + X^8 + X^6 + X^4 + X^3 + X + 1)$ yields the CRC bits (MSB) 1010 0011 0101 1011 (LSB). After the CRC bits are generated, the transmitter appends it to the data block (Fig 3). However, note that the most significant bit (MSB) of the CRC is transmitted first. If there are no transmission errors, the received CRC bits are equal to those generated at the receiver. With the MSB of the received CRC arriving first, Fig 2 reveals that the generated CRC bits at the receiver will be all zeros, provided

that the arriving CRC bits are included as data in the overall CRC accumulation.

To generate CRC-16, software is written for the M6800 microprocessor in accordance with the divider circuit of Fig 2. Synchronous communication is handled by the xc6852 serial synchronous data adapter, which is a programmable n-channel metal-oxide semiconductor IC. This IC is programmed to accept 8-bit EBCDIC with the LSB arriving first. Synchronization is achieved by detecting two consecutive SYNC code characters; these characters—embedded in a received message but not part of the arriving CRCs—are not included in CRC accumulation. To ensure proper CRC bit generation, the following rules must be observed.

(1) Initial value of CRC must be set to zero.

(2) CRC accumulation begins after detecting initial start of header (SOH) or start of text (STX) character. However, these control characters should only serve as triggers and should not be included in CRC accumulation.

(3) CRC accumulation is completed upon arrival of an intermediate transmission block (ITB), end of transmission block (ETB), or end of text (ETX) character. These control characters not only serve as ending signals but also are included in CRC accumulation.

(4) If two incoming CRC bytes following the ITB, ETB, or ETX characters are included in CRC accumulation, the final CRC should be zero. If not, a transmission error has occurred.

(5) Data bits are shifted serially, LSB first, into the CRC accumulator.

(6) Final CRC bits are shifted, MSB first, out of the CRC accumulator.

The CRC-16 accumulation subroutine is flowcharted in Fig 4 and listed in Subroutine 1. This subroutine is called, with the incoming character stored in register B of the M6800, each time a CRC accumulation is desired. RAM locations CRCHI and CRCLO correspond to the 16-bit shift register of Fig 2 with locations CRCHI (7) and CRCLO (0) corresponding to bit R₁₅ and bit R₀, respectively. Assuming a 1-MHz system clock, this subroutine requires 512 μs to execute, and processes baud rates up to 9600.

SUBROUTINE 1

CRC Subroutine for BSC Protocol

```

* M6800 SUBROUTINE FOR BSC CRC-16 ACCUMULATION
* GENERATOR POLYNOMIAL: X**16+X**15+X**2+1
* B REGISTER CONTAINS RECEIVED CHARACTER
* X REGISTER CONTAINS LOOP COUNTS
* CRCHI: HIGH ORDER BYTE OF CRC-16
* CRCLO: LOW ORDER BYTE OF CRC-16
* INITIAL VALUES OF CRCHI AND CRCLO MUST BE ZERO

CRC16  LDX  #$0008      LOAD LOOP COUNTS
LOOP   CLR  A          CLEAR A REGISTER
      LSR  B          SHIFT B(0) INTO CARRY BIT
      ROR  A          SHIFT CARRY BIT INTO A(7)
      EOR  A,CRCHI     EXCLUSIVE-OR AT CRC(15)
      STA  A,CRCHI
      AND  A,$80
      BEQ  ROTAC      KEEP RESULT IN A(7)
                        RESULT IS ZERO, ROTATE CRC
                        ACCUMULATOR
      LDA  A,$40      BSC MASK
      EOR  A,CRCHI     EXCLUSIVE-OR AT CRC(14)
      STA  A,CRCHI     SAVE RESULT FROM EXCLUSIVE-OR
      LDA  A,$02      BSC MASK
ROTAC  EOR  A,CRCLO    EXCLUSIVE-OR AT CRC(1)
      ASL  A          CIRCULAR ROTATION OF CRC
                        ACCUMULATOR
      ROL  CRCHI
      BCC  STORA
      ORA  A,$01
      STA  A,CRCLO
STORA  DEX
      BNE LOOP        PROCESS NEXT DATA BIT
      RTS

```

The major advantage of this CRC software approach is that it can be easily extended to handle the SDLC protocol. The generator polynomial for SDLC is given by

$$G(X) = X^{16} + X^{12} + X^5 + 1 \quad (7)$$

The divider circuit corresponding to this generator polynomial is shown in Fig 5. Notice the similarity between the SDLC circuit of Fig 5 and the BSC circuit of Fig 2. A software subprogram for generating CRC-16 for SDLC is listed in Subroutine 2. The difference between the SDLC and BSC routines is in the bit positions where Exclusive-OR functions are performed. Although there are only minor differences in the two CRC accumulation routines, the method by which the two protocols handle the initial and final values of the CRC bits differs greatly, as follows:

BSC Protocol

- Initial hexadecimal value of CRC is 0000.
- Final CRC is transmitted MSB first.
- At receiving station, final hexa-

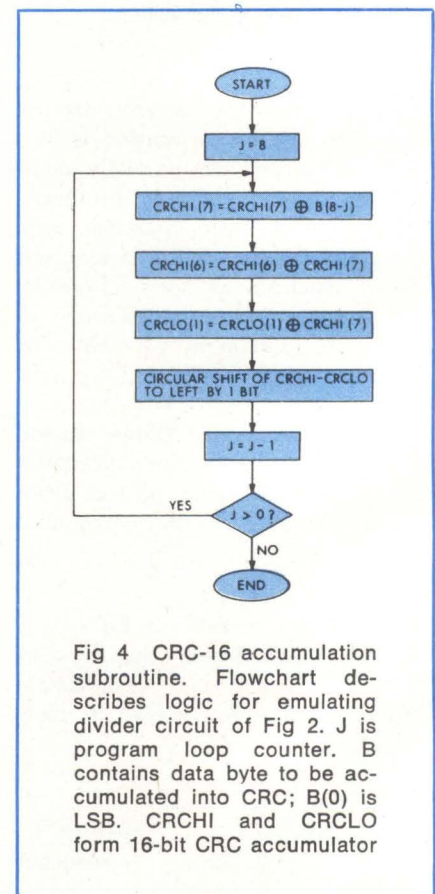


Fig 4 CRC-16 accumulation subroutine. Flowchart describes logic for emulating divider circuit of Fig 2. J is program loop counter. B contains data byte to be accumulated into CRC; B(0) is LSB. CRCHI and CRCLO form 16-bit CRC accumulator

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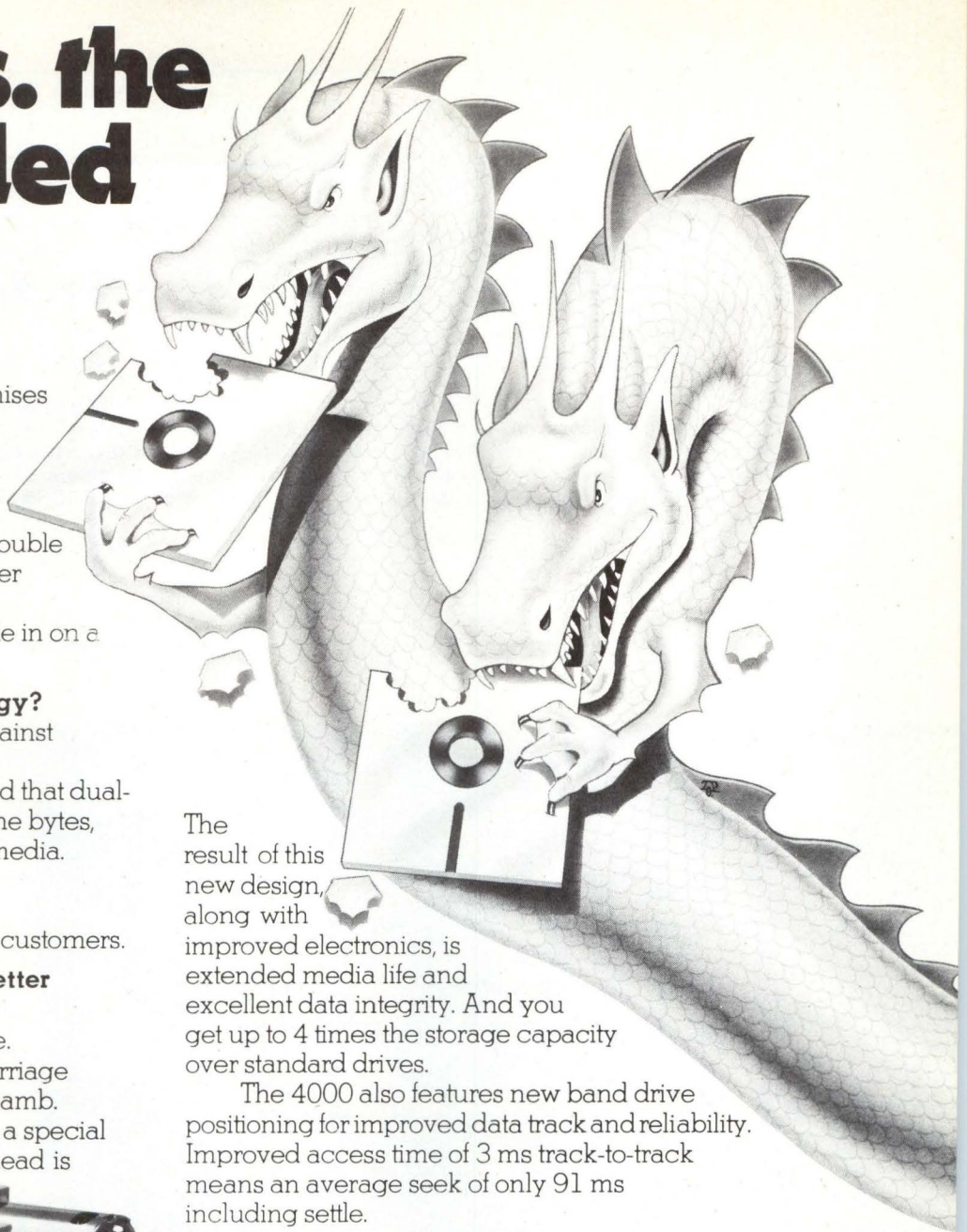
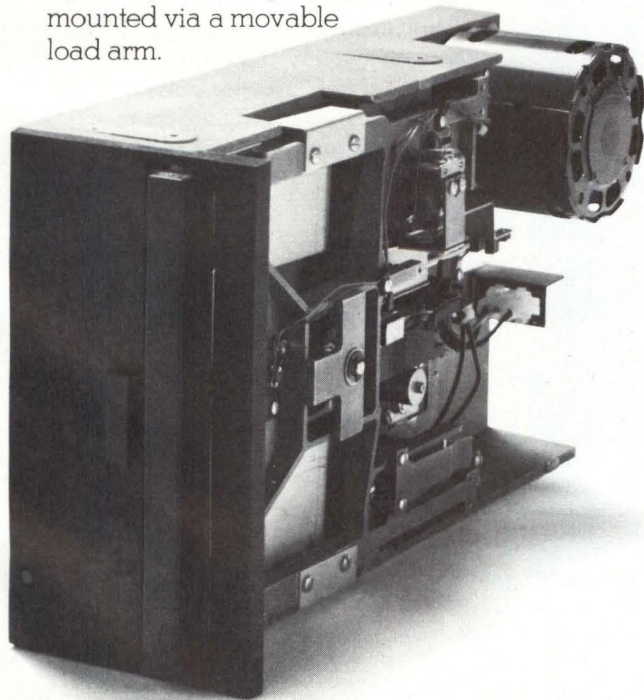
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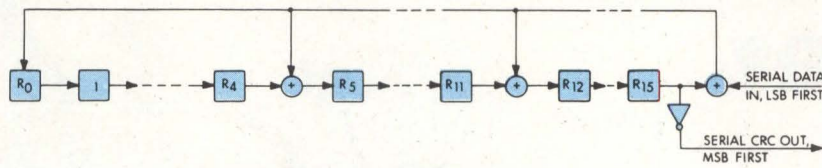


Fig 5 Divider circuit for accumulating CRC-16 [Eq (7)] for SDLC protocol. Exclusive-OR is performed between incoming data bit and R_{15} of CRC accumulator. Result T is shifted into R_0 position. Exclusive-ORs between T and R_4 and between T and R_{11} are also performed before CRC accumulator is shifted. Note that for SDLC, complement of final CRC is transmitted

SUBROUTINE 2

CRC Subroutine for SDLC Protocol

```

* M6800 SUBROUTINE FOR SDLC CRC-16 ACCUMULATION
* GENERATOR POLYNOMIAL:  $X^{16}+X^{12}+X^5+1$ 
* B REGISTER CONTAINS RECEIVED CHARACTER
* X REGISTER CONTAINS LOOP COUNTS
* CRCHI: HIGH ORDER BYTE OF CRC-16
* CRCLO: LOW ORDER BYTE OF CRC-16
* INITIAL VALUES OF CRCHI AND CRCLO MUST BE FF

CRC16  LDX  #$0008    LOAD LOOP COUNTS
LOOP   CLR  A         CLEAR A REGISTER
       LSR  B         SHIFT B(0) INTO CARRY BIT
       ROR  A         SHIFT CARRY BIT INTO A(7)
       EOR  A, CRCHI  EXCLUSIVE-OR AT CRC(15)
       STA  A, CRCHI
       AND  A, #$80   KEEP RESULT IN A(7)
       BEQ  ROTAC    RESULT IS ZERO, ROTATE CRC
                       ACCUMULATOR
       LDA  A, #$40   SDLC MASK
       EOR  A, CRCHI  EXCLUSIVE-OR AT CRC(11)
       STA  A, CRCHI  SAVE RESULT FROM EXCLUSIVE-OR
       LDA  A, #$10   SDLC MASK
ROTAC  EOR  A, CRCLO  EXCLUSIVE-OR AT CRC(4)
       ASL  A         CIRCULAR ROTATION OF CRC
                       ACCUMULATOR

       ROL  CRCHI
       BCC  STORA
       ORA  A, #$01
STORA  STA  A, CRCLO
       DEX
       BNE  LOOP     PROCESS NEXT DATA BIT
       RTS

```

decimal value of CRC is 0000 if two incoming CRC bytes are included in CRC accumulation.

SDLC Protocol

- (a) Initial hexadecimal value of CRC is FFFF.
- (b) Complement of final CRC is transmitted MSB first.
- (c) At receiving station, final hexadecimal value of CRC is F0B8 if two incoming CRC bytes are included in CRC accumulation.

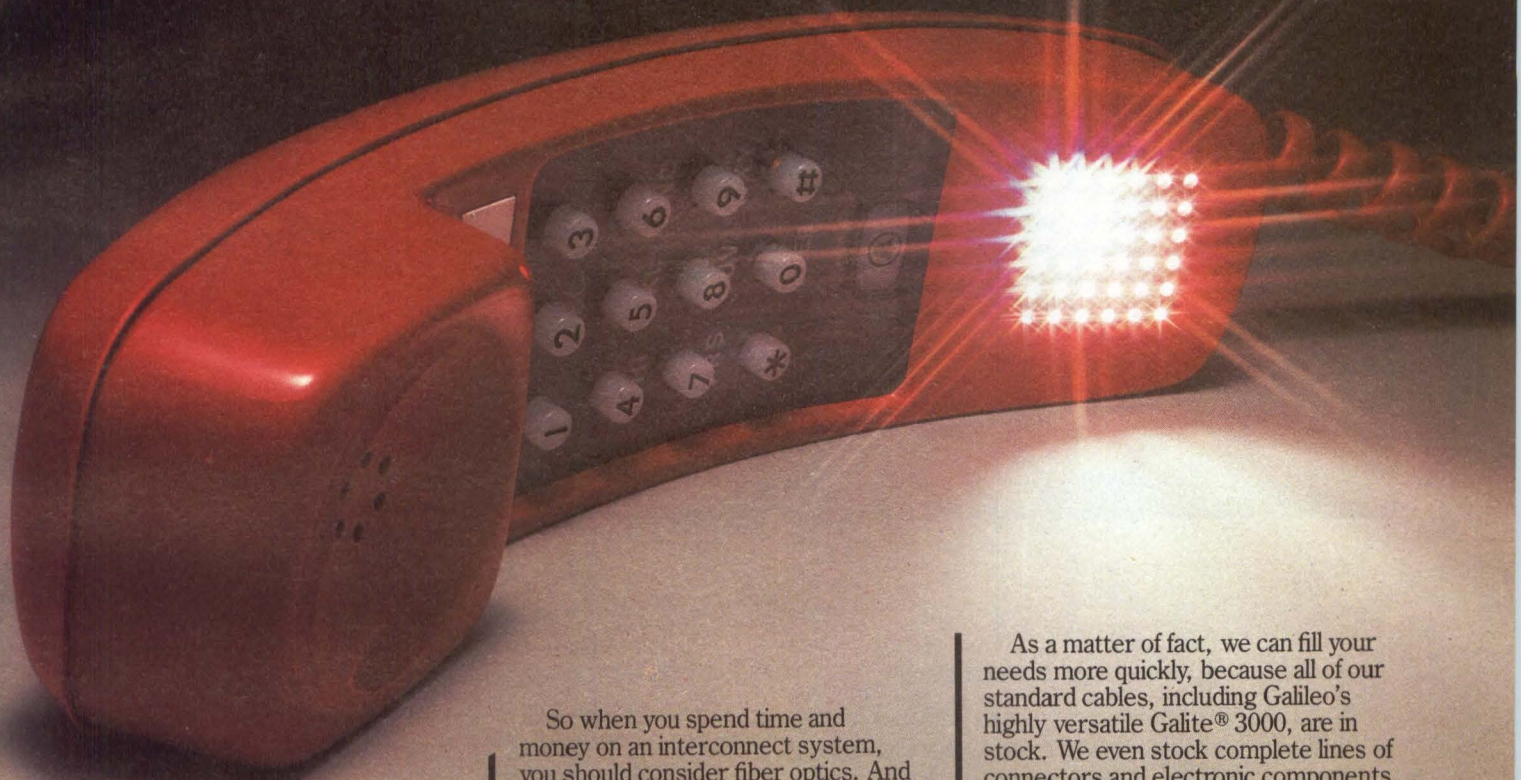
Summary

Software error checking procedures are defined for interfacing an M6800 based communications controller to an IBM mainframe computer, using BSC protocol. Background on mathematical techniques and hardware circuits for CRC calculations is provided. Software CRC generation and calculation allow a general purpose hardware interface to handle all synchronous data communications. Deviations in CRC calculations imposed by other mainframe computers are easily accommodated by software changes. Once software CRC generation for BSC protocol is established, modifying it for SDLC protocol is a simple exercise.

References

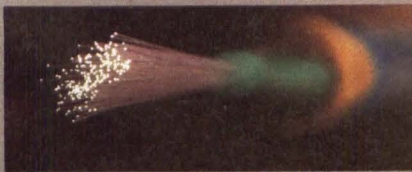
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2. R. A. Donnan and J. R. Kersey, "Synchronous Data Link Control," *IBM Systems Journal*, Vol 13, No 2, 1974

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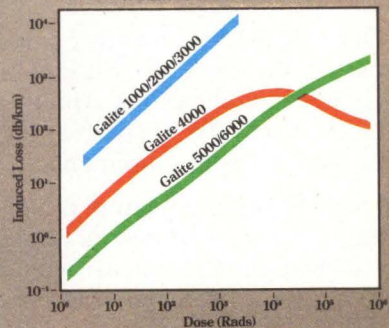


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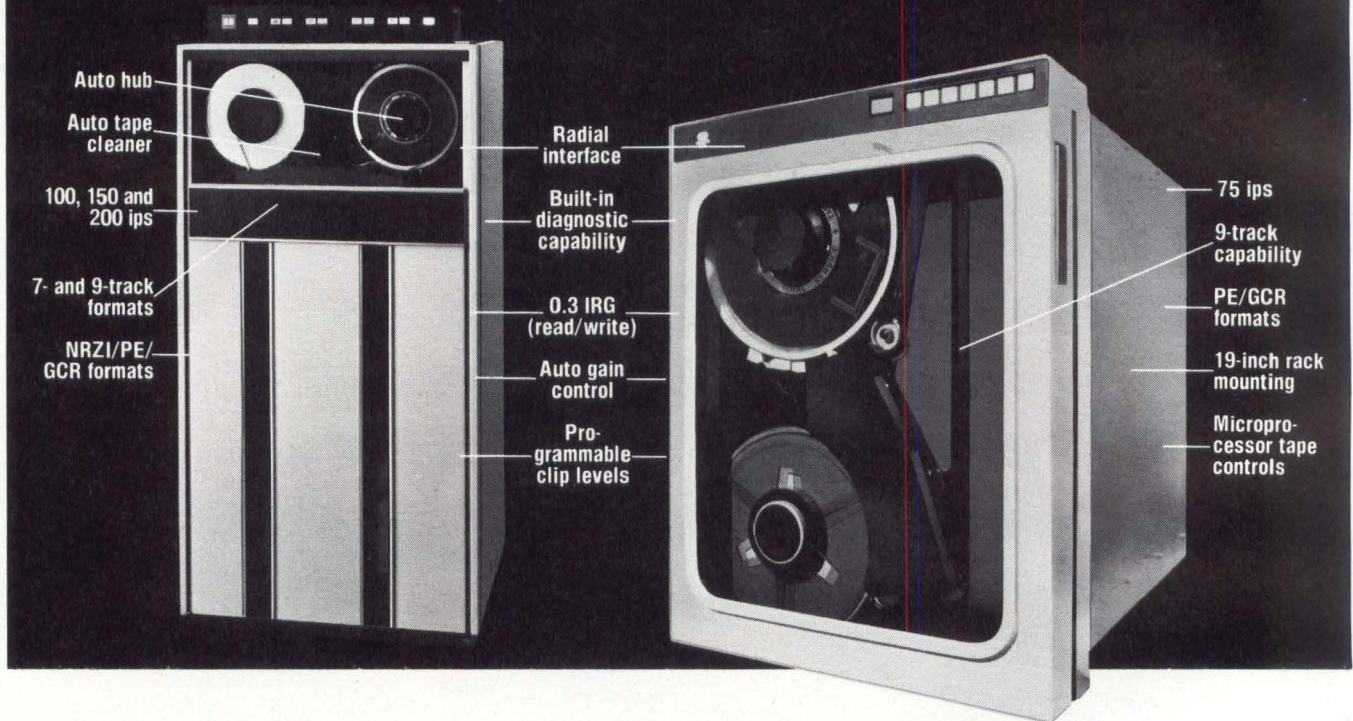
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INTERFACING FUNDAMENTALS: LOOKUP TABLES

Jonathan A. Titus and Christopher A. Titus
Tychon, Inc

Peter R. Rony and David G. Larsen
Virginia Polytechnic Institute and State University

In many applications, the microcomputer is used to convert data values from one data domain* to another. This might involve converting strings of ASCII characters to binary numbers, converting degrees centigrade to degrees fahrenheit, or converting a 4-bit binary number to a code suitable for use with a multiplexed light emitting

diode display (a 7-segment code). In some of these conversion problems, it is very easy to apply a mathematical function to a value in one data domain, the result being a datum value in another data domain. For instance, to convert strings of ASCII characters to binary numbers, the microcomputer simply has to perform a masking operation,¹ followed by rotation and addition. To convert °C to °F, the microcomputer has to perform a multiplication followed by addition ($^{\circ}\text{F} = \% \text{ } ^{\circ}\text{C} + 32$ or $^{\circ}\text{F} = 1.8 \text{ } ^{\circ}\text{C} + 32$). However, the relationship between a 4-bit binary number and a 7-segment code for use with a multiplexed light emitting diode display is very complex, as can be seen from the Table.

To convert binary 7-segment codes in the Table to octal or hexadecimal (hex), it is assumed that bit D6 represents the G segment and that bit D0, the A segment. The most significant bit of the 8-bit word, D7, is assumed to be 0. It also is supposed that within the 7-segment code, a logic 1 will turn the display's segment on and a logic 0 will turn the segment off. The lettered designation of the segments within the 7-segment display is shown in the Figure. Rather than try to determine a numerical relationship between the binary numbers and the 7-segment codes, a lookup table will be used to convert the numbers (one data domain) to codes (another data domain).

The lookup table will contain the sequence of ones and zeroes that are required to turn specific segments within the display on and off. For instance, to display a 1, segments B and C must be turned on and all the remaining

**Binary Numbers and Appropriate
7-Segment Codes**

Binary Number	7-Segment Codes							Octal	Hex
	Binary								
	G	F	E	D	C	B	A		
0000	0	1	1	1	1	1	1	077	3F
0001	0	0	0	0	1	1	0	006	06
0010	1	0	1	1	0	1	1	133	5B
0011	1	0	0	1	1	1	1	117	4F
0100	1	1	0	0	1	1	0	146	66
0101	1	1	0	1	1	0	1	155	6D
0110	1	1	1	1	1	0	0	174	7C
0111	0	0	0	0	1	1	1	007	07
1000	1	1	1	1	1	1	1	177	7F
1001	1	1	0	0	1	1	1	147	67
1010	0	0	0	0	0	0	0	000	00
1011	0	0	0	0	0	0	0	000	00
1100	0	0	0	0	0	0	0	000	00
1101	0	0	0	0	0	0	0	000	00
1110	0	0	0	0	0	0	0	000	00
1111	0	0	0	0	0	0	0	000	00

*Data domain is simply a "domain" where the units are all the same, ie, all temperatures in °C, all pressures in lb/in², all velocities in km/min.

SUBROUTINE 1

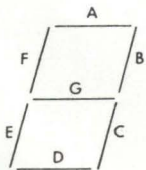
Binary to 7-Segment Conversion

/This subroutine must be called with a 4-bit number in register
/A. The 8080 will return with 7-segment code in register A.

```

*034 156
034 156 345 CONVRT,  PUSHH  /Save register pair H on stack
034 157 041          LXIH   /Load register pair H with
034 160 173          BINSS  /base address of binary to
034 161 034          0      /7-segment lookup table
034 162 205          ADDL   /Add low 8 bits of address to A
034 163 157          MOVLA  /Save result in L
034 164 322          JNC    /If there is no carry, do not
034 165 170          OKASIS /increment H register
034 166 034          0      /by one
034 167 044          INRH   /There is a carry, increment H
034 170 176 OKASIS,  MOVAM  /Get 7-segment code into A
034 171 341          POPH   /Pop register pair H off of stack
034 172 311          RET    /Return with code in register A
034 173 077 BINSS,  077    /7-segment code for 0
034 174 006          006    /7-segment code for 1
034 175 133          133    /7-segment code for 2
034 176 117          117    /7-segment code for 3
034 177 146          146    /7-segment code for 4
034 200 155          155    /7-segment code for 5
034 201 174          174    /7-segment code for 6
034 202 007          007    /7-segment code for 7
034 203 177          177    /7-segment code for 8
034 204 147          147    /7-segment code for 9
034 205 000          000    /7-segment code for 10
034 206 000          000    /7-segment code for 11
034 207 000          000    /7-segment code for 12
034 210 000          000    /7-segment code for 13
034 211 000          000    /7-segment code for 14
034 212 000          000    /7-segment code for 15
    
```

segments turned off. To display a 2, segments A, B, D, E, and G must be turned on and segments C and F turned off. To find the appropriate 7-segment code for a binary number, the binary value of the digit to be displayed is added to the base address or starting address of the lookup table. The result of this addition is the memory address at which the appropriate 7-segment code for the binary number is stored. Subroutine 1 contains a binary to 7-segment lookup table (BINSS) having a base address of 034 173₈ (1C7B₁₆). A subroutine, which the 8080



Letters designate individual segments of 7-segment LED display

microprocessor can call to find the appropriate 7-segment code, based on the binary number contained in the A register, is also listed in Subroutine 1.

When Subroutine 1 is called, the 4-bit binary number to be converted to a 7-segment code must be contained in the 8080's A register. The first instruction in this subroutine saves register pair H (registers H and L) on the stack. Register pair H is then loaded with the 16-bit base address of the BINSS lookup table. The low eight bits of this address are then added to the content of the A register (ADDL) and the 8-bit result is stored back in the L register. If the carry is a logic 1 as a result of this addition, a one must be added to the eight high bits of the address. Therefore, if the carry is a logic 0 as a result of the ADDL instruction, the microprocessor jumps to OKASIS. If the carry is a logic 1, the content of the H register (the eight high address bits) is incremented by one.

At OKASIS, the microprocessor loads the A register with the content of the memory location addressed by register pair H. The A register now contains the appropriate 7-segment code for the 4-bit binary number originally contained in the A register. The microprocessor then pops register pair H off of the stack and returns from the CONVRT subroutine. As is evident, the 4-bit binary number

was added to the base address of the lookup table. The result was used to address a memory location where the proper 7-segment code was stored.

What will happen if the lookup table entries (the 7-segment codes) are not placed in the lookup table in the proper order? If this occurs the 8080 microprocessor will not be able to determine the proper code for the number contained in the A register.

A lookup table can also be used to convert ASCII characters to Extended Binary Coded Decimal Interchange Code (EBCDIC), or to determine the sine or cosine of an angle or the logarithm of a number. If a lookup table is used to determine the sine of an angle, it might contain 90, 180, or 360 entries, depending on the sophistication of the subroutine that accesses the lookup table, the speed at which the conversion must take place, the amount of memory that can be used by the lookup table, and the desired accuracy of the result.

If the sine lookup table contains 90 entries, each entry could represent the sine of an angle between 0 and 90° or of an angle between 0 and 360°, with a difference of 4° between each entry in the table. Using a table that contains 90 entries, representing the sine of angles between 0 and 90°, the sine of any angle can be determined. However, this means that all angles must eventually be "reduced," by software, to angles between 0 and 90°. The sign of the sine would also have to be determined. By increasing the size of the table to 180 or 360 entries, in which each entry represents an angle change of 1°, fewer operations have to be performed on the angle before the sine can be found in the table. In fact, if the table contains 360 entries, the sign of the sine does not have to be determined with additional software steps, because one bit within each entry could be used as a sign bit. This means that an 8-bit table entry would contain a sign bit and a 7-bit sine.

In the "Microcomputer Interfacing: Command Decoders" column,² a thumbwheel switch was used to enter a number that represented a particular diagnostic program, 1 of 10 such programs, to be executed by the microcomputer. Since the diagnostic programs might be stored anywhere in memory, a 16-bit address specified the starting address of each diagnostic program. These addresses were stored in a lookup table using consecutive memory locations. For this reason, when the thumbwheel switch number was entered into the microcomputer, it was multiplied by two. The result of this multiplication was an even number between 0 and 18₁₀. The number then was added to the base address of the lookup table. Two 8-bit bytes, stored in consecutive memory locations, were then loaded into the D and E registers (register pair D). This 16-bit address was then moved to register pair H and written into the program counter.

Although the relationships between degrees centigrade and degrees Fahrenheit are well known, °C = 5/9 (°F - 32) and °F = 9/5 °C + 32, the time required for the microcomputer to convert one temperature to another using mathematical subroutines may be too long in some applications. If this is true, a lookup table might speed up the conversion process. Assuming that all temperatures will be within the range of 0 to 100 °C and that all temperatures are resolved to 1 °C differences, a lookup table with 100 entries can be used. The first entry in the table for 0 °C will be 00100000₂ (32₁₀), and the entry for 100 °C will be 11010100₂ (212₁₀). As expected, to determine the temperature in °F, the temperature in °C will be added to the base address of the lookup table. The resulting address is then used to address the memory location where the temperature in °F is stored (Subroutine 2).

SUBROUTINE 2

Conversion From Degrees Centigrade to Degrees Fahrenheit

```
CTOF,  PUSHH  /Save register pair H on stack
        LXIH  /Load register pair H with
        CFTAB /base address of centigrade
        0     /to Fahrenheit lookup table
        ADDL  /Add low address to degrees C
        MOVLA /Save result in register L
        JNC   /If there is no carry, do not
        COK   /increment register H
        0     /by one
        INRH  /There is a carry, increment H
COK,    MOVAM /Get temperature in degrees F
        POPH  /Pop register pair H off of stack
        RET   /Return with temperature in A

CFTAB, 040    /0 C = 32 F
        042    /1 C = 34 F
        045    /2 C = 37 F
        .      /Remainder of lookup table
        .      /is stored here (100 entries total)
        .
        322    /99 C = 210 F
        324    /100 C = 212 F
```

SUBROUTINE 3

Conversion From Degrees Fahrenheit to Degrees Centigrade

```
FTOC,  PUSHH  /Save register pair H on stack
        LXIH  /Load register pair H with
        FCTAB /base address of Fahrenheit
        0     /to centigrade lookup table
        SUI   /Subtract 32 (decimal, 040 octal) from
        040    /temperature in register A
        ADDL  /Add low address to (F - 32)
        MOVLA /Save result in register L
        JNC   /If there is no carry, do not
        FOK   /increment register H
        0     /by one
        INRH  /There is a carry, increment H
FOK,    MOVAM /Get temperature in degrees C
        POPH  /Pop register pair H off of stack
        RET   /Return with temperature in A

FCTAB, 000    /32 F = 0 C
        001    /33 F = 1 C
        001    /34 F = 1 C
        .      /Remainder of lookup table
        .      /is stored here (180 entries total)
        .
        143    /211 F = 99 C
        144    /212 F = 100 C
```

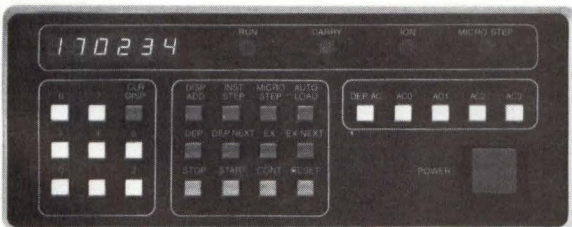
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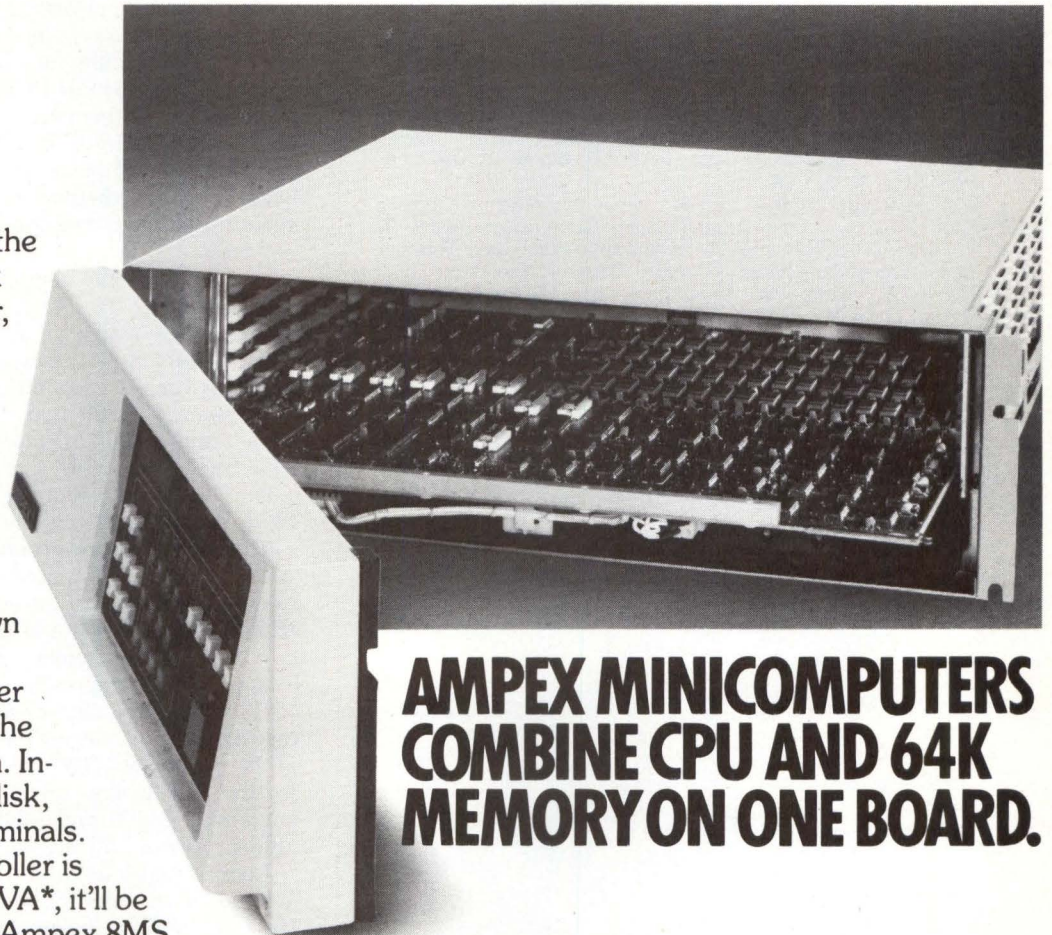
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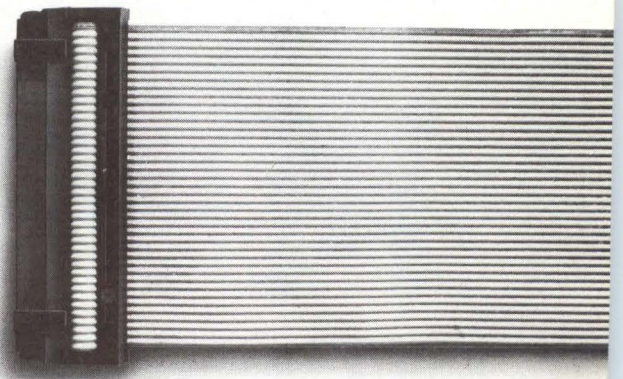


Charley Penrose has some suggestions about achieving big system capability in the little 8MS cabinet. Call him at 213/640-0150. Or write to him at Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245.

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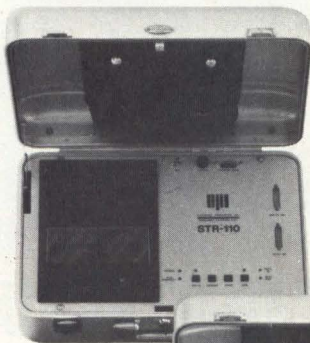
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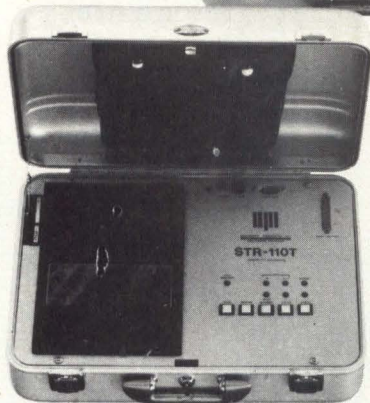
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To convert from °F to °C, a lookup table with 180 entries (212 - 32) is required for resolutions to 1 °F. However, in this conversion, the temperature in °F is not simply added to the base address of the lookup table. Remember, the first entry in the table, at the base address of the table, contains the temperature in °C for 32 °F. Therefore, 32 must be subtracted from all temperatures in °F; then the base address can be added to the result (Subroutine 3).

Lookup tables usually are implemented when a conversion must be performed as quickly as possible, or when there is no simple relationship between the two equivalent values in two different data domains. Using a lookup table generally avoids time consuming and perhaps complex-to-write mathematical calculations. Of course, if $A = 2B$ and the value of B is known, then the lookup table probably would not be used to determine the value of A . Regardless of whether B is in fixed or floating point numerical format, multiplication by two is relatively easy and fast.

To determine the sine of an angle, a lookup table that contains 360 1° (8-bit) entries could be used. Each entry would contain a sign bit and a 7-bit sine. With this lookup table, the microprocessor can determine the sine of any angle between 0 and 360°, to 0.78% accuracy, in only 29 μs (assuming a 500-ns cycle time). However, the lookup table requires 360 memory locations for storage. For a 90-entry lookup table that represents all angles between 0 and 90° in 1° increments, the microprocessor needs 100.5 μs to determine the sine of any angle between 0 and 360°. For more accurate sines of angles, the lookup table could be composed of 16-bit values, where each value contains a sign bit and a 15-bit sine. If the sine for all angles between 0 and 360° is stored in memory in 1° increments, 720 memory locations will be required for lookup table storage. The microprocessor also will need 53 μs to find the sine of the angle. For the lookup table that contains 90 entries for the angles between 0 and 90° in 1° increments, 180 memory locations will be required to store the lookup table. To determine the sine of any angle between 0 and 360° using this lookup table, the microprocessor will require only 109 μs.

Lookup tables do have disadvantages: they require large amounts of memory for storage and have limited accuracy. However, with a lookup table, a data domain conversion is performed very quickly. Lookup tables frequently are used when there is no simple mathematical relationship between the two equivalent values. By considering the accuracy, speed of conversion, memory storage requirements, and possible mathematical relationships, the user will be able to determine when and where to use lookup tables in programs.

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THE AMI/BERKELEY MATCH PROGRAM— AN INDUSTRY SPONSORED MICROCOMPUTER PROJECT LABORATORY, PART 2

Harold S. Stone

University of Massachusetts
Amherst, Massachusetts

Microcomputer projects of varying types evolved from the Match Program, conceived by American Microsystems, Inc (Santa Clara, Calif) and the University of California's (Berkeley) Electrical Engineering and Computer Science Department to provide students with the learning laboratory experience of designing a microcomputer system. Part 1, published last month, detailed the program itself and one student's EEG/EKG analyzer—the winning project. This final installment describes two other projects: a voice controlled wheelchair and an intelligent terminal.

Microprocessor Based Control System For Wheelchairs

This project by Eytan Ben-Meir intends to create a microcomputer controlled wheelchair that accepts and operates

from voice input. Handicapped people confined to wheelchairs frequently have disabilities that prevent them from operating wheelchairs either by hand or by a mechanical device that controls a drive motor. Voice input and speech recognition for a small vocabulary not only are feasible, but also are in commercial production, so that this aspect of the project in itself is not an advance in technology. The challenge consists of coupling voice input to a wheelchair drive system, while making a small system that consumes little power, so that it can be self-contained to fit the space available in a wheelchair. This would have been impossible prior to the advent of microprocessor technology.

The interesting aspect of the design concerns the speech recognizer. Basic external portions of the circuitry appear

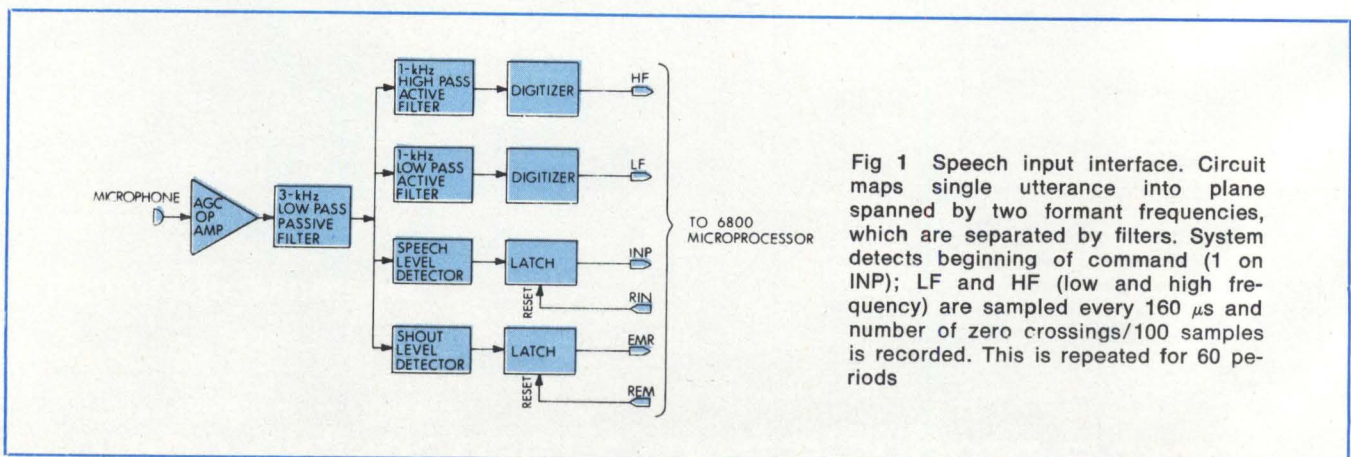


Fig 1 Speech input interface. Circuit maps single utterance into plane spanned by two formant frequencies, which are separated by filters. System detects beginning of command (1 on INP); LF and HF (low and high frequency) are sampled every 160 μ s and number of zero crossings/100 samples is recorded. This is repeated for 60 periods

in Fig 1. Here voice input from a microphone is filtered through a 3-kHz low pass filter, and then is analyzed separately through 1-kHz high pass and low pass filters, and by level detectors set to detect normal talking and shouting. The shout level detector shuts down the wheelchair in emergencies since the presence of shouting causes an emergency halt without requiring analysis of the speech content.

The speech level detector output triggers the analysis software in the microprocessor that voice data are present, and the microprocessor then samples the outputs of the low and high pass samples. Samples are taken every 160 μ s, and the number of zero crossings/100 samples is recorded for samples taken in a 16-ms period. The process of sampling and averaging over 16 ms is repeated 60 times, covering 960 ms of speech, sufficient time to catch most single utterances.

The zero crossing data collected for 60 low and high pass samples are basic data used by the speech recognizer to select the nearest word from its vocabulary. The project used a simple heuristic weighting scheme to detect one of seven commands: go, stop, slow, fast, back, left, and right. Fig 2 shows the idea behind the recognizer. This 2-dimensional matrix contains 30 cells arranged in a 5 x 6 array. Each cell is identified by its x-y coordinate, given in the number of zero crossings observed in one interval in the high and low frequency channels, respectively. Thus, each 16-ms sample of high and low frequency zero crossings produces a pair of numbers that becomes the coordinates of a cell in Fig 2. The 60 16-ms samples are entered into the table by recording in each cell the number of those samples whose coordinate pairs fall in the cell. To complete the recognition process, the resulting 5 x 6 matrix is compared with stored versions of matrices that indicate the most likely results when each of the seven oral commands is received, and the processor selects the best match.

To store the seven pattern matrices, the processor has a training mode during which the subject repeats several times the command to be uttered, with an average of the observed matrices computed in the pattern matrix. Project development was uncompleted at the close of the academic year so that exact details of the training and recognition algorithms were not settled. The successful application of this approach, while still uncertain, is a subject of much interest.

Design and Implementation of CRT Terminal With Graphics Capability

Design of a cathode-ray tube (CRT) terminal that performs both text editing and graphics is the objective of this project by Bruce Char and Michael Ubell. To give flexibility and computational power, a microprocessor drives the terminal, typical of other intelligent terminals currently available. To create enhanced capabilities, the system can accept a new character or graphics character set from the input keyboard, and use these characters to generate visual images. In addition, the system has a user definable subroutine area wherein the user can enter programs for the microprocessor to process data in the display memory. Presumably this terminal could be coupled to an existing system as an intelligent terminal. The ability to change the contents of the programs in the terminal's memory permits it to be downline loaded externally so as to alter its interactive and functional characteristics.

Fig 3 shows a block diagram of the system. The microcomputer is the AMI EVK-200 evaluation kit to which a keyboard and display processor are connected. The student

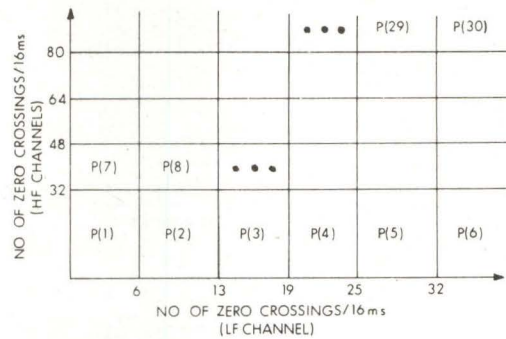


Fig 2 Zero crossings plane. Plane is divided into 30 elements. Array P(i), $i = 1, 2, \dots, 30$ is created and compared with seven arrays prepared during training mode for seven commands; statistical rule decides which command (if any) was given

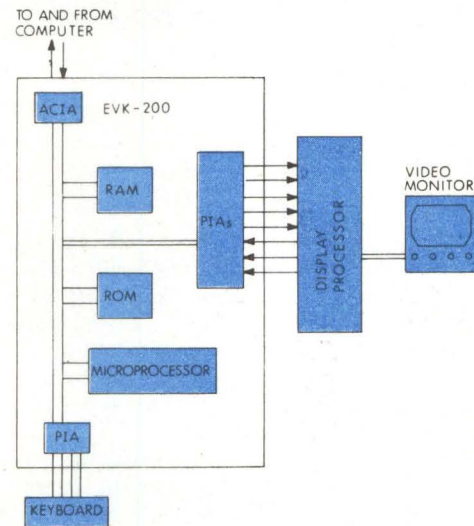


Fig 3 Microcomputer system for CRT terminal. Terminal's major components are video board and microcomputer board. Latter is AMI's EVK-200 prototyping system containing 6800 processor, I/O interfaces, RAM, ROM, and P/ROM. ROM contains development software for prototyping work—6800 assembler/disassembler and utility routines to load and develop application software. Use of EVK system hardware is not integral to design

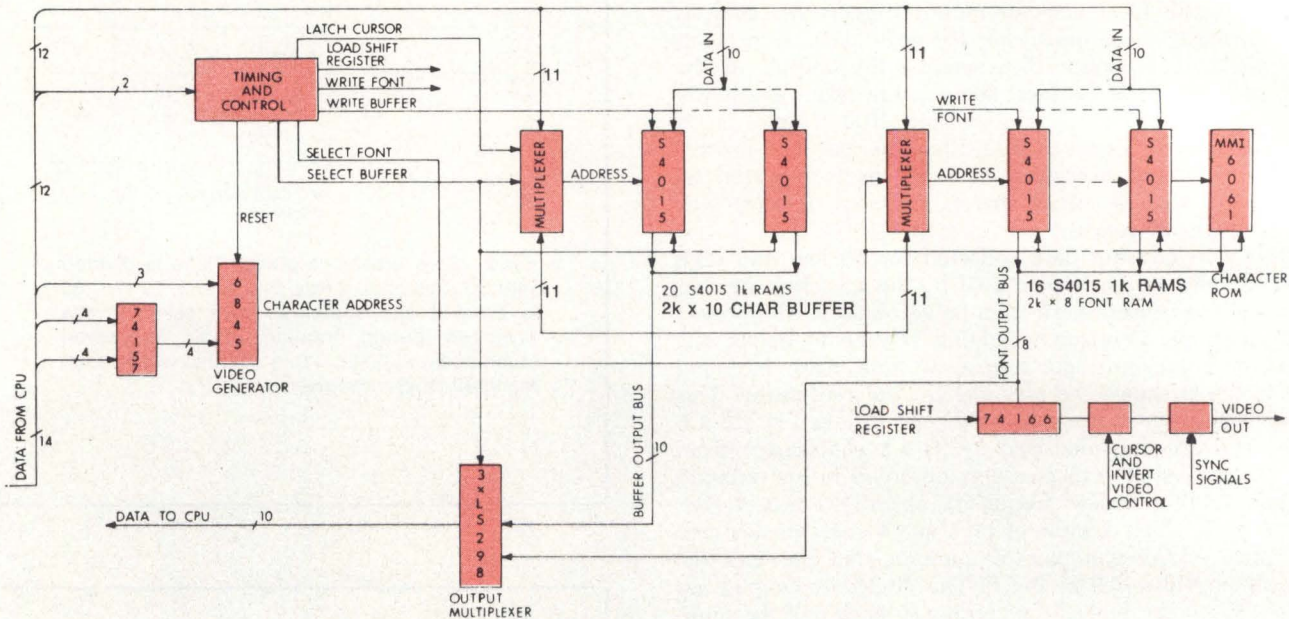


Fig 4 Video board memory. Schematic shows memory segmented into three parts. Buffer memory is map of 1920-char matrix locations, stored in 2048 x 10-bit RAM. Character generator ROM is used for ASCII character set (standard font). Alternative font is stored in 2048 x 8 bits of RAM, organized as 256 x 8 x 8 dot patterns

designed display processor drives a video monitor. The heart of the display processor is a 6845 video display chip, donated by Motorola, plus a collection of 16 8-bit control registers that define the characteristics of the display, such as height, width, cursor position, and blink rate. The processor can load these, so that the display controller can be altered by program to drive various types of monitors with different characteristics.

The design decision to go to a separate processor was forced upon the design team because the latency of the 6800 to direct memory access requests is too long to be useful for the high speed requirements of the display. Consequently, the microcomputer loads data into the display processor for viewing on the terminal, and the display processor responds to processor requests with an acknowledge signal when the operations are completed.

To perform various display functions, the display processor memory is organized into three separate parts—a character memory, and a random-access memory (RAM) and read only memory (ROM) to hold displayable patterns (Fig 4). A map of the displayable character positions is organized as a 2048 x 10 memory. The 10 bits encode character (8 bits), font (1 bit to select from two fonts), and inverse or direct video (1 bit). One of the selectable fonts is from a standard character generator ROM (a 6061 donated by Monolithic Memories, Inc) or from user pro-

grammed memory arranged as an array of 256 characters encoded as 8 x 8-bit matrices.

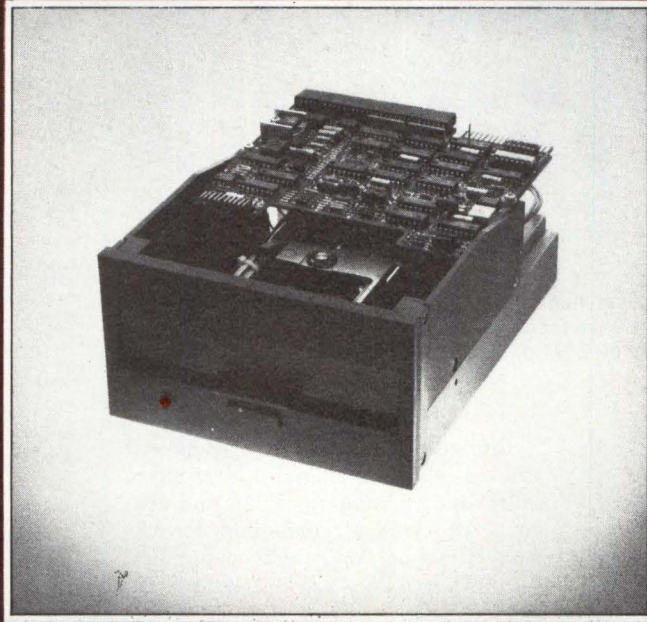
The project's challenging aspects concerned the high speed requirements for the video display unit which essentially precluded a heavily software oriented implementation based on the 6800 microcomputer. Fortunately, some of the hardware design problems were greatly eased by the use of the display controller chip. Dense, fast memory would also have been helpful in reducing construction time since the memory contains about 36 chips, yet does not contain a good deal of capacity.

Conclusions

These two projects and others not published in this article are far more ambitious lab projects than could have been attempted before the advent of the microprocessor. Students now have the opportunity to focus their energies and talents on total systems where they once had to be content with building pieces of systems. They can solve problems that range from electrical, hardware, and software design, to packaging and human interfacing.

Acknowledgement

We are grateful to AMI for making the projects possible, and to Tom Larkin, Sharon Long, and many others for their considerable efforts that contributed to the student projects.



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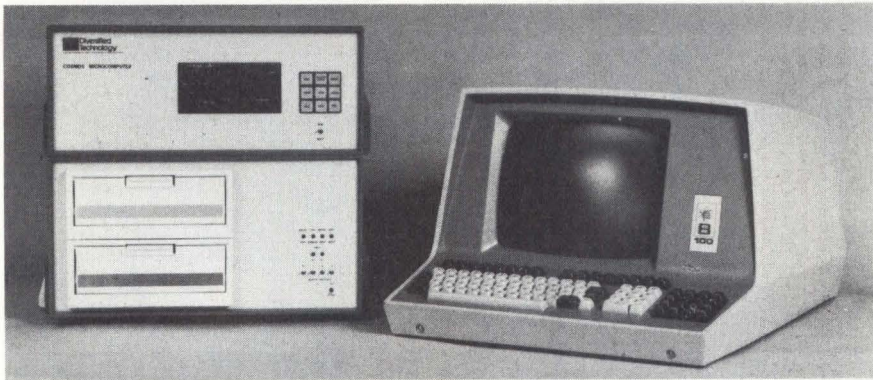
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Standalone Microcomputer Develops Resident, High Level Language Programs



DT/μMOS development system can stand alone for program development; it includes DT/μMOS microcomputer, dual floppy disc with controller, interactive CRT terminal, full high level development language, and in-circuit I/O emulation. Solid State Scientific has developed model DTM 145-DH to be enhanced with options, peripherals, and accessories

DT/μMOS model DTM 145-DH high level development system is a stand-alone microcomputer for resident, high level language program development. It is comprised of the DT/μMOS microcomputer, dual floppy disc with controller, interactive CRT terminal, high level development language, and in-circuit I/O emulation.

Based on the SCP 1802 microprocessor, the microcomputer utilizes CMOS technology for low power, high noise immunity, and wide temperature range. Specifications include an 8-bit word size, 3.2-MHz clock, instruction cycle time of 5 μs at 3.2 MHz or 3.2 μs at 5 MHz, and memory addressing of 65k bytes of RAM, ROM, or EPROM. Memory capacity consists of a 12k-byte RAM with expansion up to 65k bytes using optional RAM or EPROM. An optional hardware arithmetic logic chip handles high speed scientific computation. It provides 32-bit fixed and floating point notation of arithmetic and scientific functions. Interactive in-circuit I/O emulation eases development. In addition, each system component is individually available for OEM systems.

Dual floppy disc drives accommodate 250k bytes/drive (IBM format) for editing and program storage. The floppy disc controller supplied can control up to four drives for a total capacity of 1M bytes. It features individual write protect and disc based editing.

Interactive program development utilizes a CRT terminal for program entry and debugging. Type and features of terminal, including formatting, function keys, edit capability, and block mode, are optional. Standard features are a 24-line x 80-column display, upper case ASCII, addressable cursor, RS-232-C, 20-mA current loop, printer output, and display scrolling. Line printers are also available depending on the application.

The resident structured high level programming language used by the development system is MICROFORTH. Highly efficient in programming throughput, memory capacity, and processor speed, it is comprised of a compiler, a cross compiler to compress application programs for target systems, an assembler, a cross assembler, interpreters, an editor, and a floppy disc operating system. Multi-level programming allows the language to "learn" as applications programs are developed. Other features are interactive debugging and reverse Polish notation. The language, according to Solid State Scientific Inc, Montgomeryville, PA 18936, reduces program development time by up to 90% over assembler language.

The system is suited to microprocessor product development, engineering, and research. Documentation is supplied. System peripherals, accessories, and expansion modules are also available.

Circle 410 on Inquiry Card

Bus Adapter/Motherboard Expands Memory and Extends I/O Capabilities

The 8100, an adapter and 6-slot motherboard with card guides, interfaces the Radio Shack TRS-80 microcomputer to the S-100 bus. The adapter connects to the microcomputer via a ribbon cable. A second TRS-80 connector allows another microcomputer to be connected at the same time.

Also included are optional onboard support circuitry and sockets for 16k bytes of dynamic RAM. The RAM may be split into 4k blocks which are addressed to any 4k boundary; 4k dynamic RAMS may be used in place of 16k RAMS.

HUH Electronics, 1429 Maple St, San Mateo, CA 94402 has included optional onboard I/O interfaces to handle serial and parallel I/O. Serial interface features RS-232 or 20-mA current loop, software programmable baud rate from dc to 56k baud, programmable modem control lines, and onboard DB-25 connector. Jumper selection allows the microcomputer to function as either a computer or a terminal.

Latched 8-bit parallel input and 8-bit parallel output ports have positive and negative strobe inputs and outputs. A standard 22/44-pin edge connector joins them.

Circle 411 on Inquiry Card

Package Assembles and Expands Board-Level Computer System

The RMC 660 assembled, rackmounted system, developed by the Computer Products Group of National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, accepts up to eight Series/80 microcomputer, memory, and interface boards. It either assembles a Series/80 board-level computer system or expands existing systems as a chassis. Boards are inserted in slots; etched backplane circuits interconnect power, bus, and control lines.

Designed for the company's or Intel's board-level computers, the package consists of two system board chassis, heavy-duty regulated power supply, and front panel with control

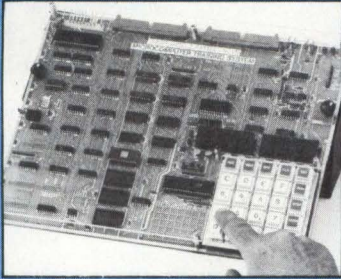
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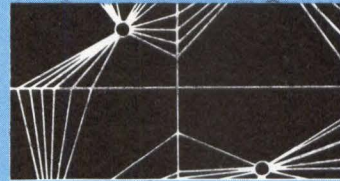
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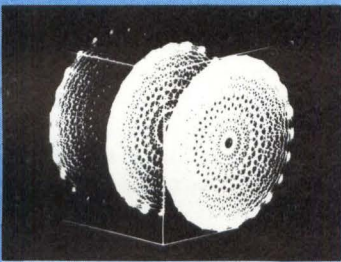
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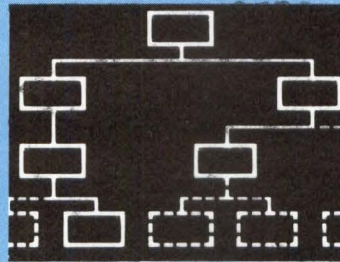
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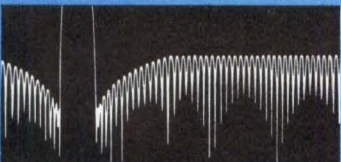
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switches mounted in a standard 7 x 19 x 20" (17.8 x 48.3 x 50.8-cm) RETMA enclosure. Price is \$1250 each. Supply provides -12 V at 1.5 A, 5 V at 30 A, -5 V at 1.75 A, and -12 V at 1.75 A. Output current is limited to 1.2 times rated value while overvoltage protection circuits operate at 1.16 to 1.32 times rated voltage. Line voltage input is through a transformer tapped for 100, 115, 200, and 230 V at 47 to 63 Hz.

Regulation is 0.1% for a 50% load change and 0.1% for a 10% line variation. Ripple is 10 mV peak to peak, from dc to 500 kHz, on all outputs. Stability is 0.05% for 8 h with constant line, load, and temperature. Remote sensing is provided for the 5-V level; all outputs may be trimmed $\pm 5\%$ from nominal values.

An ac power failure detection circuit supplies a TTL compatible high level signal when line voltage drops 10% below normal. The signal returns low when line voltage reaches 8% below normal. All dc levels remain within specification for 2 ms after low line conditions and 7.5 ms after total power loss to complete orderly shutdowns.

Four LSI Peripheral Devices Enhance Bit-Slice Based Systems

Additions to the 2900 family offer four peripheral devices for bit-slice based systems. Included are the Am2904 status and shift control unit, Am2930 program control unit, Am2940 direct memory access counter, and Am2942, a 22-pin version of the direct memory access counter. The LSI devices from Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086 replace up to 15 lower complexity circuits. They undergo 100% processing to MIL-STD-883 requirements. Prices range from \$16.95 to \$22.95 in 100-unit lots.

The 2904 contains three independent logic blocks to handle housekeeping functions associated with the ALU. The circuit selects the carry-in signal to the ALU from one of seven sources. It sets up 32 shift linkages, 16 left and 16 right, to handle shift techniques found in minicomputer instruction sets. Two edge triggered status registers function as foreground or background registers or as micro

or machine level status registers. Bit manipulating instructions are provided. The device also performs single-cycle tests for any of 16 conditions. Tests are performed on either of two status registers or directly on the ALU output.

The 2930 functions as a program counter which is updated at the end of each memory fetch and as an index register to store offset values. It handles subroutine linkage and relative address capability, while also providing a microprogram sequencer. Expansion accommodates long addresses.

Two independent 8-bit synchronous counters comprise the 2940. Either counter can be incremented or decremented on each clock. Each counter can be preset through a syn-

chronous parallel load feature. The DMA counter itself is cascadable to any length; its two internal counters can be cascaded to form a 16-bit programmable up/down counter in one package.

The 22-pin version 2942 functions as a high speed DMA address generator or programmable timer/counter. Multiplexed address and data lines can be used with a common bus. Of the 16 instructions, 8 are the same as those of the 2940. Eight additional ones facilitate the programmable timer/counter functions. As such, the device has two independent programmable 8-bit, up/down counters in one package. Cascading is possible with several devices or within one device to form a 16-bit single-chip counter.

Circle 412 on Inquiry Card

Training Aid Teaches Microprocessor Hardware, Software, Troubleshooting

The 5036A entry level microprocessor learning program covers three fundamental areas—hardware, software, and troubleshooting. Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304 has designed the briefcase-size microcomputer and 20-lesson textbook/lab manual to give hands-on experience, especially useful to industrial training, production, and service departments. The company's model 5004A Signature Analyzer and 5024A Troubleshooting Kit can be added for training in microcomputer fault location; jumpers intro-

duce faults and program failures into the system.

A PC board layout of the microprocessor lab's main circuit board uses color graphics to highlight components and buses. Data, address, and status lines have individual LED indicators. During single-step program execution, the user can observe each signal line during each machine cycle. Demonstrations cover operation of microcomputer systems with keyboards, speakers, switches, LEDs, and displays; interaction with I/O devices; and processor handling of inputs. The lab also shows how to differentiate between a microprocessor and its peripherals when a fault exists in a system.



Microprocessor lab from Hewlett-Packard trains user in areas of troubleshooting, hardware, and software. Block diagram layout of main circuit board uses color graphics to teach hardware concepts; Monitor program demonstrates programming aspects; and addition of signature analyzer supplements troubleshooting experiments

A Beautiful Way To Interface



IQ 140

SOROC's first and foremost concern, to design outstanding remote video displays, has resulted in the development of the IQ 140. This unit reflects exquisite appearance and performance capabilities unequaled by others on the market.

With the IQ 140, the operator is given full command over data being processed by means of a wide variety of edit, video, and mode control keys, etc.

The detachable keyboard, with its complement of 117 keys, is logically arranged into 6 sections plus main keyboard to aid in the overall convenience of operation. For example, a group of 8 keys for cursor control / 14 keys accommodate numeric entry / 16 special function keys allow access to 32 pre-programmed commands / 8 keys make up the extensive edit and clear section / 8 keys for video set up and mode control / and 8 keys control message and print.

Two Polling options available: 1) Polling compatible with Lear Siegler's ADM-2. 2) Polling discipline compatible with Burroughs.

IQ 120

The SOROC IQ 120 is the result of an industry-wide demand for a capable remote video display terminal which provides a multiple of features at a low affordable price.

The IQ 120 terminal is a simple self-contained, operator / computer unit.

The IQ 120 offers such features as: 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions and protect mode. Expansion options presently available are: block mode and hard copy capability with printer interface. The IQ 120 terminal incorporates a 12-inch, CRT formatted to display 24 lines with 80 characters per line.

CIRCLE 74 ON INQUIRY CARD

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The programming portion explains how programs work at hardware and software levels, and teaches simple programming. The ROM is programmed with the Monitor, comprised of a power-up, self-test program to check system operation, demonstration programs to illustrate microcomputer versatility, and signature analysis test program to exercise all the system's nodes for troubleshooting purposes. The Monitor determines processor reactions to keyboard commands, and performs programmed operations.

The final aspect of the system is troubleshooting and repair to the component level. The recommended accessory for the troubleshooting

experiments is the 5004A Signature Analyzer. The signature analysis data compression technique provides a 4-digit hexadecimal "fingerprint" unique to each node in a microcomputer system. Users compare signatures of circuits under repair to those documented by the manufacturer in order to verify that the signal on the node is correct.

The lab is priced at \$800. Troubleshooting accessories are the 5004A Signature Analyzer for \$990, and the 5024A Troubleshooting Kit for \$625, which includes the 545A Logic Probe, 546A Logic Pulser, and 547A Current Tracer.

Circle 413 on Inquiry Card

Analog Input and I/O Boards Bring Data Acquisition to μ Computers

Two solutions to data acquisition problems for users of the Intel SBC-80 single-board computers are available. These are a second gen-

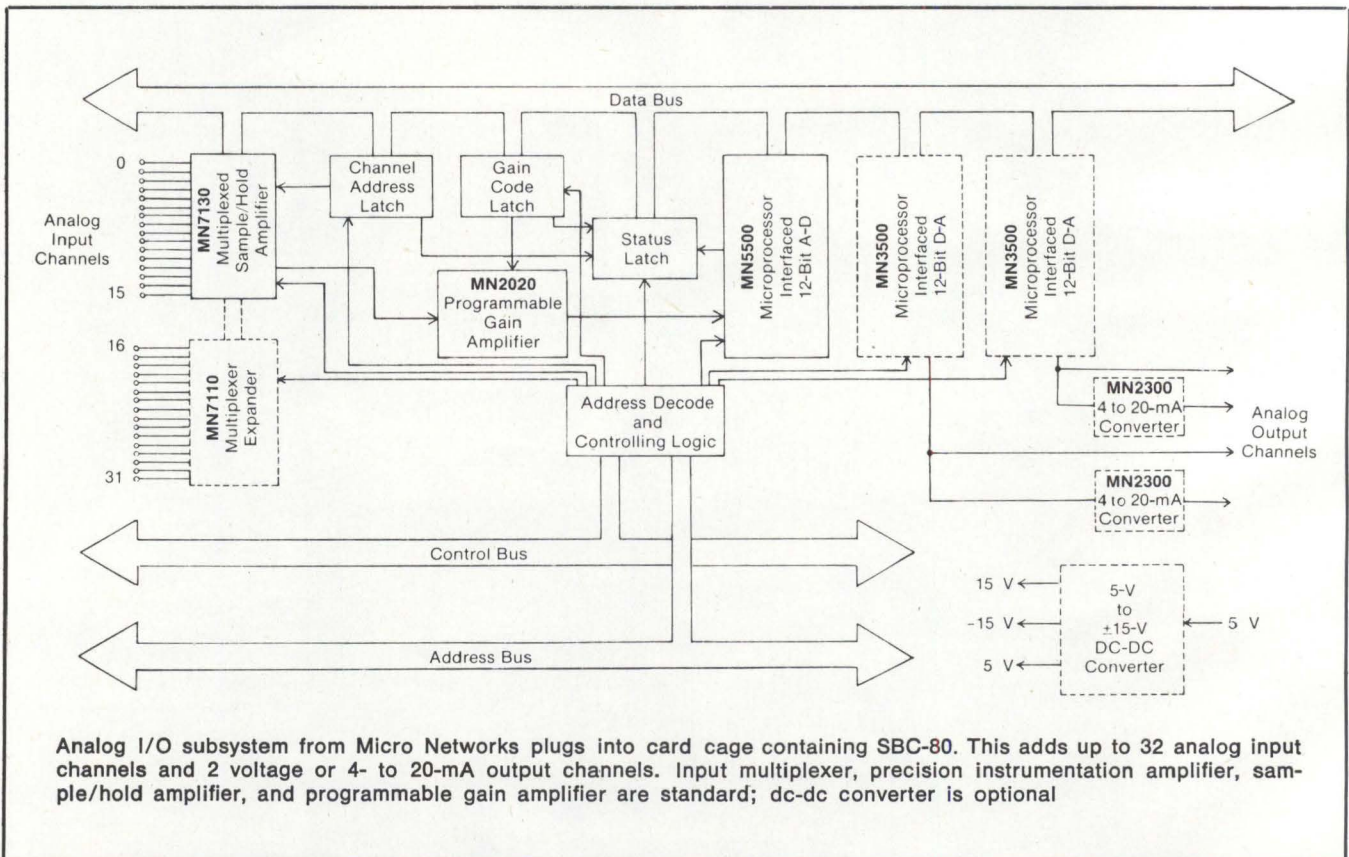
eration analog input board and an analog I/O subsystem, both of which are electrically and mechanically compatible with the SBC-80/10, /20, and MDS systems.

Analog Input Board

The first is the RTI-1202, available

with 8 or 12 bits of resolution and accuracy. It features a high speed sample and hold amplifier, instrumentation amplifier with resistor programmable gain, 16 single-ended or 8 differential input channels expandable onboard to 32 single-ended or 16 differential channels, and accepts 4- to 20-mA current loop inputs. The prewired board can be plugged into any Multibus card cage. Wirewrap jumpers change input range or operating mode.

Additional features of the interface are memory mapping, external trigger and EOC interrupts, and random or autoincrement modes of channel selection. A dc-dc converter is optional. Key specs are input overvoltage protection to $\pm(V_{CC} + 20 V)$, gain range of 1 to 1000 V/V, input full-scale range of 10 mV to $\pm 10 V$, 2- μ s max conversion time for 8-bit ADC and 25- μ s max for 12-bit ADC, and throughput of 125 kHz for 8 bits and 30 kHz for 12 bits. The Instruments and Systems Group of Analog Devices, Inc, PO Box 280, Rt 1 Industrial Park, Norwood, MA 02062 has introduced the

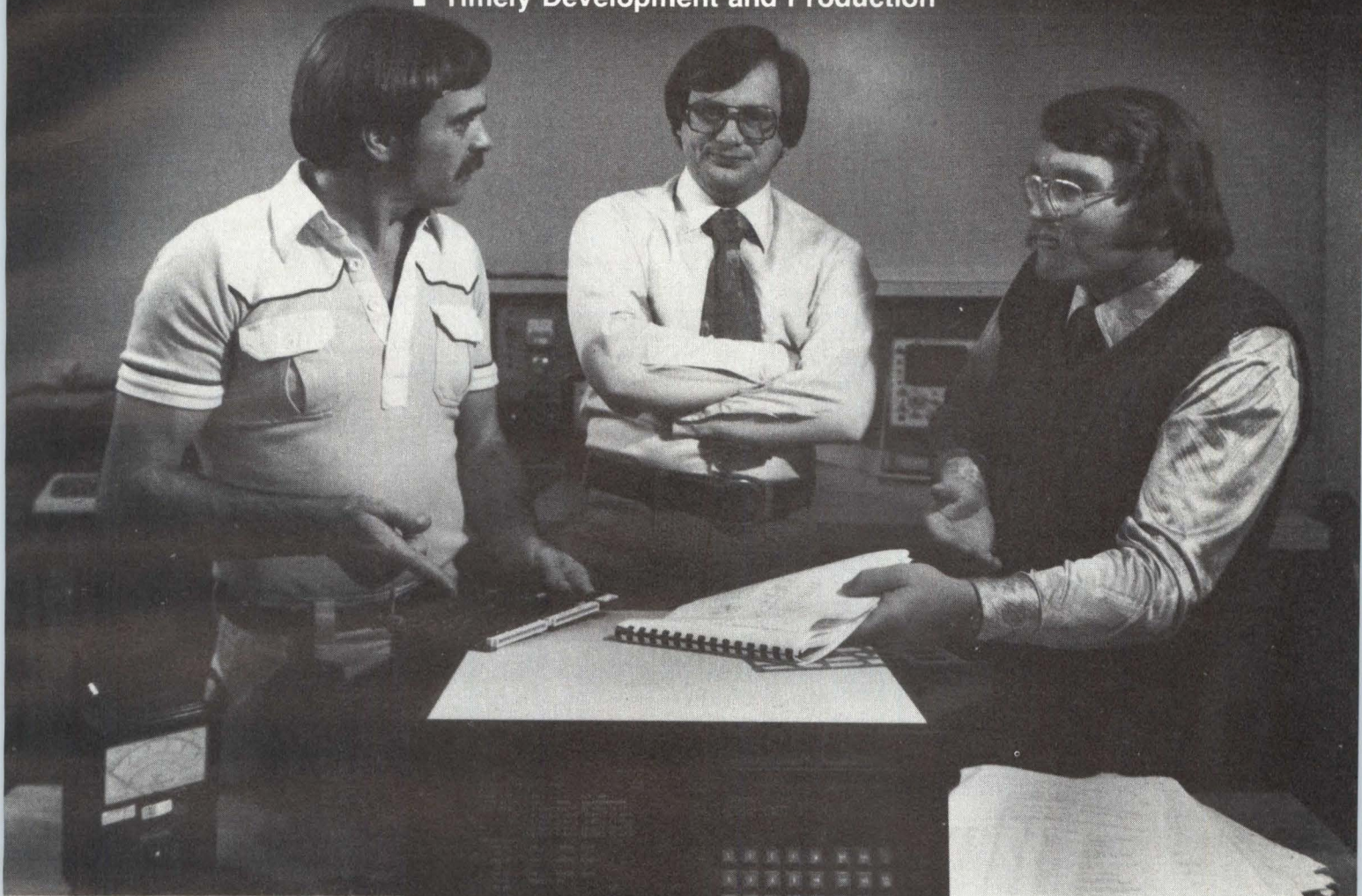


Analog I/O subsystem from Micro Networks plugs into card cage containing SBC-80. This adds up to 32 analog input channels and 2 voltage or 4- to 20-mA output channels. Input multiplexer, precision instrumentation amplifier, sample/hold amplifier, and programmable gain amplifier are standard; dc-dc converter is optional

When you integrate hardware and software . . .

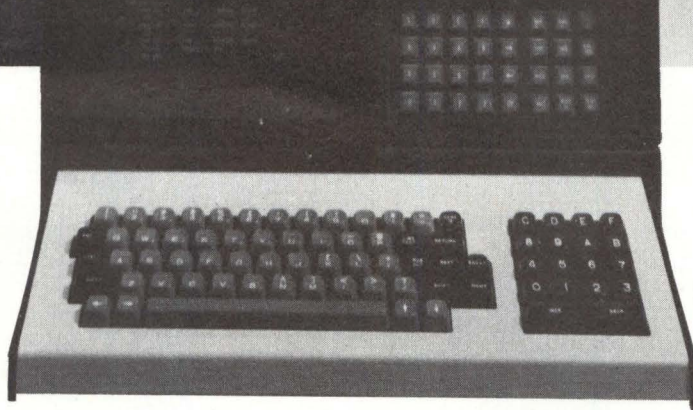
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Circle 414 on Inquiry Card

Analog I/O Board

Offering 19 bits of dynamic range, the standard MN7300 from Micro Networks Corp, 324 Clark St, Worcester, MA 01606, provides 16 input channels. The optional multiplexer expander increases the input channels to 32 single-ended or 16 differential. Two output channels offer either voltage or 4- to 20-mA outputs. Two optional output channels drive CRT displays, pen plotters, and analog control applications, as well as generating complex analog waveforms. Both channels can be configured for voltage outputs of 0 to 5, 0 to 10, ± 2.5 , ± 5 , and ± 10 V,

or for 4- to 20-mA current outputs.

Included are a 12-bit ADC and 8-level software programmable gain amplifier. Using this amplifier, the basic user selectable input ranges of 0 to 5, 0 to 10, ± 2.5 , ± 5 , and ± 10 V can be modified under software control by gains of 1, 2, 4, 8, 16, 32, 64, and 128. This allows full-scale input ranges from ± 19.5 mV to ± 10 V.

The memory mapped board occupies 10 consecutive locations positioned anywhere in user memory. All card activities are software controlled. Additional features are a low package count, hermetic sealing of critical components, and an optional dc-dc converter. Prices range from \$612 to \$1138, depending upon options.

Circle 415 on Inquiry Card

EPROM Module Holds Up to 16 Individually Addressable Devices

Byte Board, an EPROM module for the S-100 bus, accepts up to 16 2708 EPROMs, incorporates a power-on jump capability, and provides for wait state generation for slow memories. Each EPROM is individually addressable on any 1k boundary, and may be placed anywhere in the com-

puter's address space. Unused EPROM locations do not take up memory address space. The state of all user selectable options, silkscreened onto the board, can be read directly from the board.

Data Vector Corp, po Box 3141, Burbank, CA 91504 has solder masked the module to minimize solder bridges during assembly. It is fully socketed and has two spare IC pads for custom circuitry.

Circle 416 on Inquiry Card

Desktop Computer Packages Peripheral Devices Internally

The 625 Mark II desktop computer, based on a Z80 central processor, includes an extended BASIC operating system and up to 60k bytes of internal RAM, along with the display and hardcopy peripherals. A 1280-

character CRT displays 16 lines of 80 characters, with 64 graphic characters. A 40-column alphanumeric matrix printer provides multiple copies on plain paper, with variable character sizes. The full size typewriter style alphanumeric keyboard also has a 10-key numeric keypad. Twenty keys serve as 60 special functions.

Dual flexible disc drives store up to 630k bytes of data (both program and data storage). Compucorp, 1901 S Bundy Dr, Los Angeles, CA 90025 offers several software packages for both business and scientific applications, available on flexible discs.

Five board slots within the computer handle various interface options. These are the IEEE-488 bus option, A-D/D-A interface with internal multiplexer and 32-line parallel interface, dual serial communica-

tions controller, CMOS memory and realtime clock, and S-100 interface. A 19" (48-cm) rackmount version is also available. Prices start at \$8000.

Circle 417 on Inquiry Card

Buffered 16k RAM Board Uses Fully Static 4k Memory IC

An S-100 bus 16k x 8-bit RAM board uses a 4k memory IC similar to the 2102, but with four times the capacity/IC package and less power/bit. Typical power is 1.5 A at 8 V. Fully static memory is compatible with DMA and other devices. All signals to MOS devices are buffered by low power TTL to prevent static electricity damage and to minimize capacitive loading on the bus.

No wait states are required for 8080, Z80, or other CPU operation at 2 MHz (4 MHz optional). A DIP switch selects addresses in 16k blocks. Electronic Control Technology, 763 Ramsey Ave, Hillside, NJ 07205 provides low profile IC sockets; battery backup can be wired in.

Circle 418 on Inquiry Card

I/O Interface Module Expands Computer's Capabilities

Providing four channels of programmable ac power control, 600 W each channel or 1600 W total, the A828/AC-P I/O interface for the Radio Shack TRS-80 microcomputer can sense switch closures, photosensors, and 5-V logic levels, drive LED displays, and operate motors, solenoids, and alarms. The package consists of a self-contained 5-V power supply, interface cable, I/O port connector cable, metal enclosure, and sample programs. The power supply prevents loading of the TRS-80. The 5 V at 150 mA is present at the port connector for powering user circuits.

JC Enterprises, po Box 23445, San Diego, CA 92123 is selling the interface for \$165, with an optional expansion cable costing \$6. With the same functions, the A828 AC is also offered that includes 4-channel ac power control and 5-V power supply. Price is \$124.50.

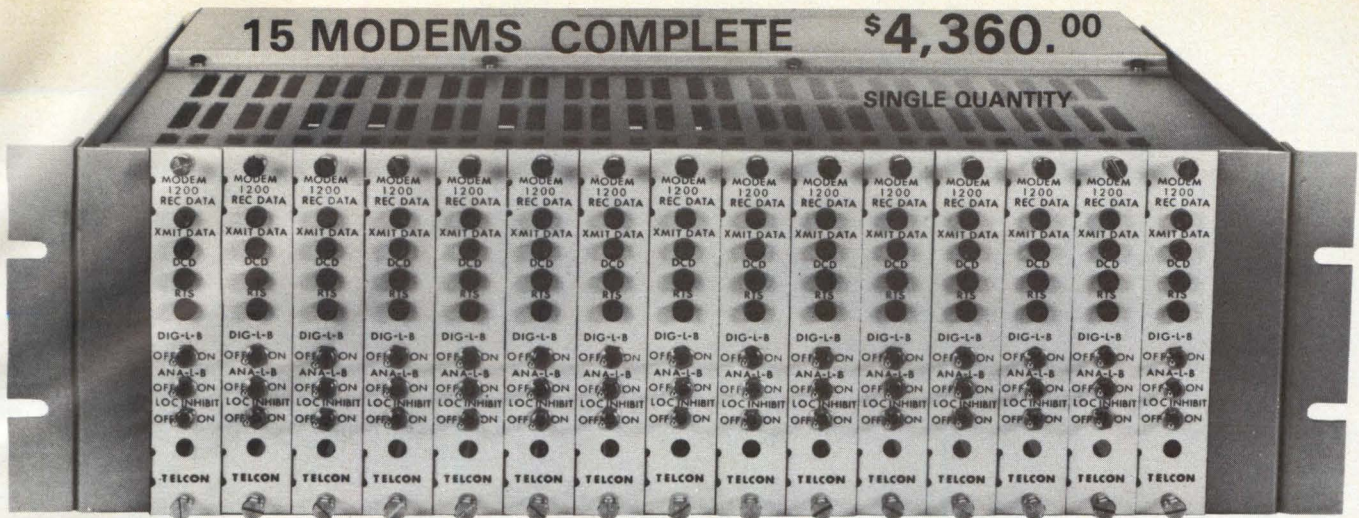
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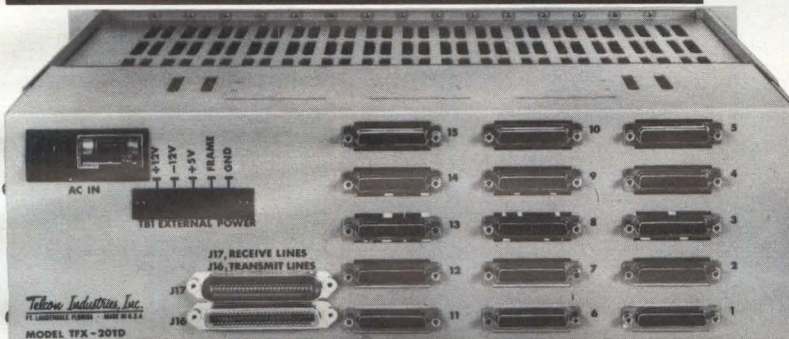
Telcon's quality FSK data modem TM-1200 is designed for asynchronous operation up to 1200 bps over a 3002 unconditioned line (up to 1800 bps with C2 conditioning) or over the public switched network using a CDT coupler.

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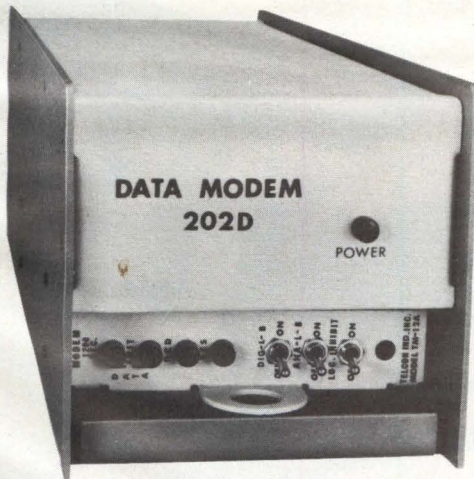
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Dept of Defense Must Protect μ Processors From Static Electricity

The pervasiveness of static electricity—a peril to microprocessors—necessitates that the Dept of Defense (DOD) catch up with industry in materials and equipment to prevent static electricity damage to microprocessors. This message was presented by Jess J. Kanarek, president of Wescorp, 1155 Terra Bella Ave, Mountain View, CA 94043, to the national convention of the American Defense Preparedness Association. Both microprocessor destruction and degradation occur in virtually every operating environment.

It was pointed out that increased functioning speeds of the chips make

them more vulnerable to static damage. Therefore, the static electricity must be dissipated in an even shorter time period if damage is to be prevented.

Current military specs permit anti-static shipping bags that require more than 0.001 s to dissipate a static charge; in addition, the material used is degraded by detergents and water, and protects only if humidity is 25% or more. Industry, on the other hand, is increasingly using conductive materials and equipment in assembly, handling, storage, and shipment of microcircuits, assemblies, and subassemblies. Kanarek urged that more attention be given to development of materials meeting specific DOD needs, and of methods of using these materials to prevent degradation at government facilities.

Floppy Disc Control Board Circuitry Uses Digital Logic Design

Single-board, double-density floppy disc controller with a DMA channel is compatible with IBM 3740 single-density and both IBM 2D and Intel SBC-202 double-density formats. It operates with Intel SBC-80 and MDS system software, or the CP/M operating system.

An 8085 processor directs diskette operation. A 1k-byte RAM buffer handles disc data. DMA data transfer

to or from the system occurs at a rate of over 1M bytes/s.

The board, which does not depend on LSI circuits, includes an all digital logic design of Micromation, Inc, 524 Union St, San Francisco, CA 94133 in the disc control circuitry. Included are a phase-lock oscillator and write precompensation circuitry, as well as CRC error detection logic. An onboard hardware UART with RS-232 interface facilitates communication with a system console device. Bus arbitration and master control logic coordinate the DMA transfer.

Circle 420 on Inquiry Card

Precision Analog Interface Board Offers 12-Bit D-A Conversion

The assembled PAIB, a peripheral analog interface board, consists of two analog output channels and output voltage ranges for operation in either monopolar or bipolar modes. A patch area allows user designed circuitry to be utilized.

Compatible with most S-100 bus microcomputers, the board functions as a successive approximation ADC for measurement and control of up to eight analog input channels. A separate 8-bit digital output port is contained onboard. Vector Graphic, Inc, 31364 Via Colinas, Westlake Village, CA 91361 has designed it to

use hermetically sealed, laser terminal DACs for true 12-bit (0.012%) accuracy.

Circle 421 on Inquiry Card

Hardware/Software Compatible I/O Board Gives 200-V Isolation

The dual height, DT2768-I digital I/O board is hardware and software compatible with Digital Equipment Corp's DRV11 general purpose, parallel line interface unit for the DEC LSI-11 and -11/2. Components are a 16-bit wide data input register, 16-bit wide data output register, and control/status register. Two 40-pin,

DRV11 compatible Berg connectors provide input, output, and power access; DIP switches assign a base, as well as two interrupt vector addresses. Available addresses and the control/status register protocol provide maximum software efficiency with the basic LSI-11 structure.

A 200-V bit-to-bit isolation feature for all 32 data lines, as well as control and status lines that interface with the external process, optimizes systems noise performance and provides reliability. Data Translation Inc, 4 Strathmore Rd, Natick, MA 01760 designed the board for rugged industrial environments.

Isolated signal lines assume a logic 1 state for inputs between -2.0 and 0.25 V, and a 0 state for inputs between 3.6 V at 15 mA and 7 V at 25 mA. Input response time is 50 μ s max and input frequency is typically 10 kHz. A compatible, non-isolated version, the DT2768, operates at significantly higher speeds.

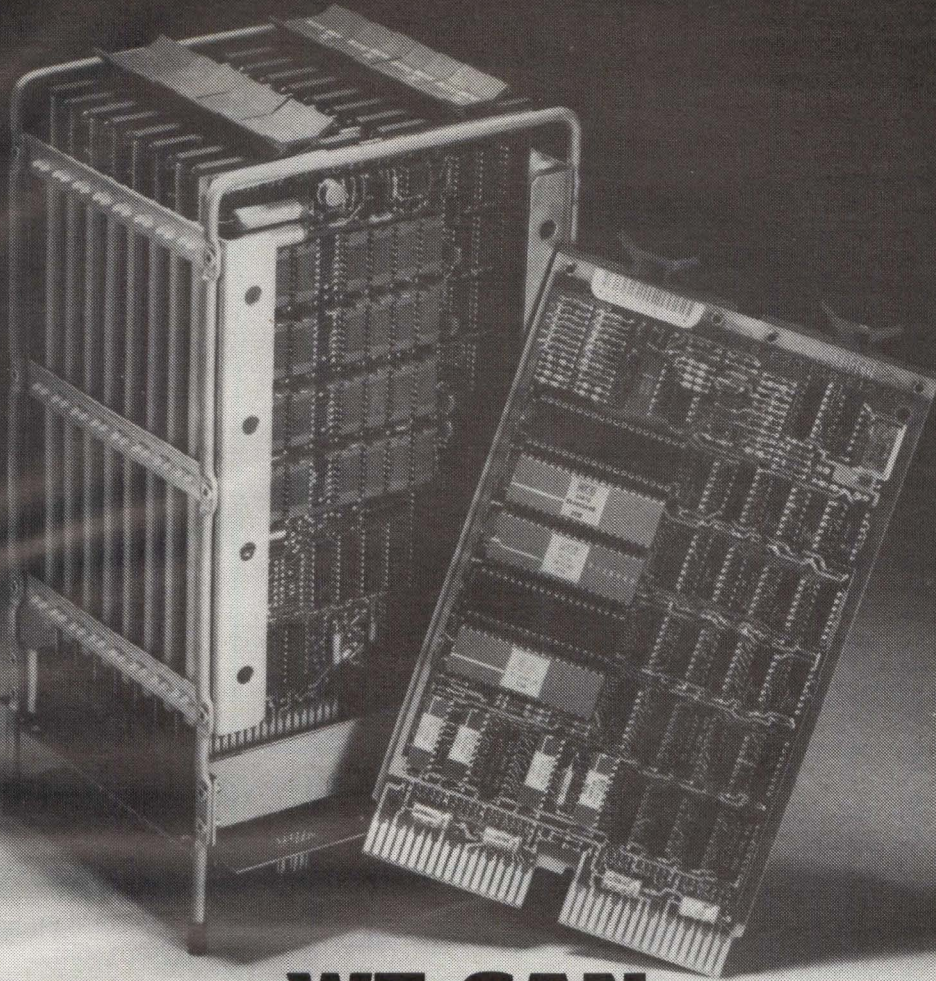
Circle 422 on Inquiry Card

Tape Controller Applies Cartridge Drives to Uses of Big Reel Tape Drive

All 3M type tape cartridge drives can be linked to Digital Equipment Corp's LSI-11 computers using a plug-in TC-160 data cartridge magnetic tape controller from Western Peripherals, div of Wescorp, 1100 Claudina Pl, Anaheim, CA 92805. The controller handles from one to eight 6400-bit/in (2520/cm) drives each having a 17M-byte capacity, or the same number of 1600-bit/in drives, each with a 4.2M-byte capacity.

The device emulates DEC's TM-11/TU-10 0.5" (1.27-cm) magnetic tape system, allowing cartridge drives to serve big reel tape drive applications. Requiring no special wiring, the unit occupies any two adjacent Q-bus quad slots in the computer. It is cable connected to a small adapter board that mounts on the rear of the drive. These adapter boards allow interfacing to DEC, Kennedy, Qantex, Tandberg, and 3M cartridge drives. The adapter daisy chains the drives, handles unit-select assignments, and provides signals to front panel indicators.

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Price Formula Configures 16k-Byte Development System

A development package for the 6800 includes a single-board computer, 16k bytes of RAM, RS-232 interface with switch selectable baud rates, 300- and 2400-baud cassette interfaces, FANTOM-II monitor/debug ROM, editor/assembler software, card rack, backplane, and power supply. Wintek Corp, 902 N 9th St, Lafayette, IN 47904 has priced the system at \$895, \$177 less than the regular price. Also available are an EPROM programmer module and 15 interface modules on 4.5 x 6.5" (11.4 x 16.5-cm) boards with standard 22/44-pin edge connectors.

Circle 424 on Inquiry Card

Reliable, High Speed Digital Tape Transport Employs Phase Encoding

Plugging directly into a standard 8-bit parallel port, BETA-1 is a universal tape storage device that interfaces to many microcomputers, including non S-100 bus systems. Serial port connection is optional. The unit uses the industry standard phase-encoding technique. An internal 8035 microprocessor has a 1k-byte program and high level tape operating system. The tape transport features random seek at more than 100 in (254 cm)/s, with average access time in 10 s or less, and loading time at 8000 bits/s. MECA, 7026 Old Woman's Spring Rd, Yucca Valley, CA 92284 also offers an option that permits loading speed of 16,000 bits/s. Single-quantity price is \$399.

Circle 425 on Inquiry Card

Hard Disc System Packs 10M Bytes of Formatted Online Storage Per Unit

The HD-10 hard disc system features the CDC Hawk model 9427H hard disc, which uses a single fixed disc for 5M bytes of storage. An industry standard 5440 type removable disc cartridge provides an added 5M bytes of storage for file backup capability and offline storage.

The system includes the IMDOS II operating system, compatible with other versions of IMDOS and CP/M[®] Version 1.33. Applications written under IMDOS require little or no changes to run under IMDOS II. All of the company's utilities and languages will also run.

Compatible with the company's 8080/85 based microcomputers, the disc system has an average random access time under 35 ms. A single S-100 bus I/O board interfaces with up to two external disc controllers, each of which supports up to four hard discs. This expands any system to 80M bytes of hard disc storage with only one I/O card. Two models—a 10M-byte drive system with controller and a 10M-byte expansion drive—are available from IMSAI Manufacturing Corp, 14860 Wicks Blvd, San Leandro, CA 94577 in both 50- and 60-Hz versions.

Circle 426 on Inquiry Card

Microcomputer System Adds Onboard Floppy Disc Controller

The single-board OEM 90F/MPS microcomputer is based on the Z80[™] family. Board resident facilities include multidensity DMA floppy disc controller with DMA based disc access, multitrack transfers, data scanning, and support of up to four 5.25 or 8" (13.34- or 20-cm) single/double-density drives. Quay Corp, PO Box 386, Freehold, NJ 07728 has also included up to 65k bytes of dynamic RAM, up to 14k bytes of UV erasable P-ROM with programmer, 1k bytes of static RAM, up to four 8-bit programmable I/O ports (two Z80 PIOS), four programmable counter/timer channels, an RS-232-C or 20-mA serial port with selectable baud rates, 2.5- or 4-MHz operation, and P-ROM resident system monitor with debug capabilities.

Circle 427 on Inquiry Card

Expandable DAC Boards Slide Directly Into μComputer's Card Guides

ST-MNOVA-DA series of three plug-in D-A converter boards, in 4- and 8-channel versions, interface to Data General's micronOVA microcomputer.

The -DA4A is a 4-channel unit with an optional ± 15 -V 150-mA dc-dc power converter onboard. The -DA4B is the same, without the dc-dc converter; it requires an external supply of ± 15 V at 160 mA. The third, -DA8B, is an 8-channel DAC; it does not have the onboard dc-dc converter, and requires an external supply of ± 15 V at 320 mA. Prices are \$630, \$550, and \$785, respectively. Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 includes a systems manual and paper tape diagnostic program as part of the purchase price.

Performance specs for all DAC cards include 4- μ s settling time to within $\pm \frac{1}{2}$ LSB of final value, max nonlinearity of $\pm \frac{1}{2}$ LSB, gain temperature drift of ± 30 ppm of full-scale range/ $^{\circ}$ C, zero temperature drift of ± 5 ppm of full-scale range/ $^{\circ}$ C (unipolar output), and offset temperature drift of ± 5 ppm of full-scale range/ $^{\circ}$ C (bipolar output). Slew rate is 20 V/ μ s.

Four jumper selected full-scale output voltage ranges are 0 to 5, 0 to 10, ± 5 , and ± 10 V. Output impedance is 50 Ω , capable of driving loads with ± 5 mA of short-circuit proof current. Digital input coding is either straight or offset binary, or 2's complement. Any DAC may be replaced by the 16-bit digital output port.

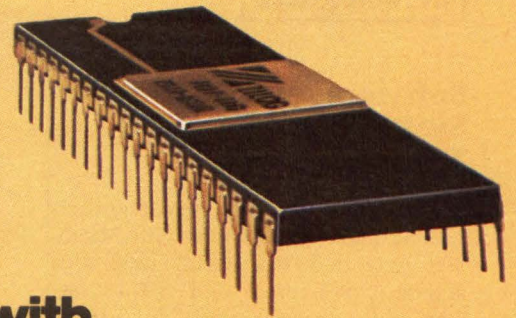
Circle 428 on Inquiry Card

Switch Programmable Ports of I/O Board Give Interface Flexibility

Four parallel ports and two RS-232/TTY serial ports plus strobe and attention ports of the S-100 I/O board are all switch programmable to interface various types of peripherals. Parallel ports can be switched for input or latched output; both serial ports can be switched to any of 16 baud rates from 110 to 19k. Each strobe and attention port flip-flop can be switched for positive or negative pulsing. The eight I/O addresses can be located on any boundary divisible by eight. Designed by George Morrow, the SWITCHBOARD[™] is available from Thinker Toys[™], 1201 10th St, Berkeley, CA 94710. There are options for 4k of RAM and 4k of EPROM.

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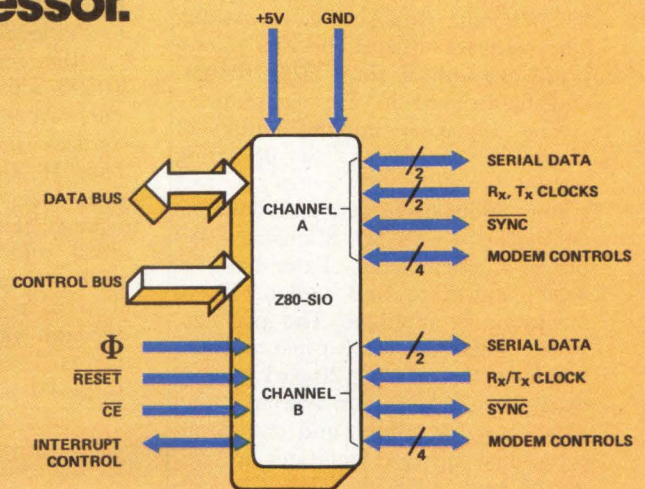
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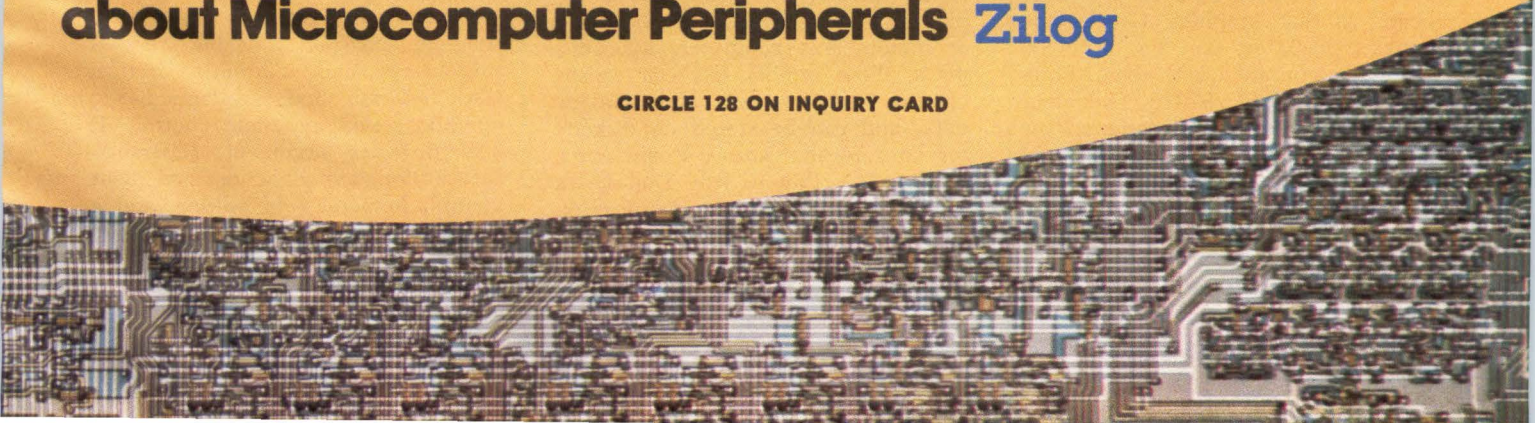
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SOFTWARE

Software Makes Computer Systems Compatible With Three Languages

Challenger III series microcomputers can be made compatible with Microsoft Extended-Disk BASIC, 1968 ANSI standard FORTRAN, and 1974 ANSI standard COBOL through the use of the OS-CP/M software package introduced by Ohio Scientific, Inc, 1333 S Chillicothe Rd, Aurora, OH 44202. The software utilizes the Z80 microprocessor, one of three—Z80, 6502A, and 6800—used in the computer.

The 48k RAM implementation of Digital Research's CP/M operating system consists of a CP/M text editor, 8080 assembler, and dynamic debugger, as well as a Microsoft 8080 macro assembler, Extended-Disk BASIC, FORTRAN, and COBOL. Documentation is supplied. The package, with a suggested retail price of \$600, includes three 8" (20-cm) floppy discs—one diskette for FORTRAN and BASIC, one for COBOL, and one duplicator. The software facilitates upgrading of models C3-S1, C3-A, C3-B, or C3-OEM systems.

Circle 430 on Inquiry Card

Software Support Manages Memory Mapped Video Board Functions

The 6502 Video Driver Routine (VDR) software supports memory mapped video boards, interfacing easily to applications programs, assemblers, and BASIC, among others. It manages cursor movement, line and page overflow, scrolling, and control of scrolling speed, printer, and partitioning of the screen into protected areas. Programmable mode control is maintained over the video board so that graphics, Greek, and reverse characters can be displayed on boards equipped with them. Forethought Products, 87070 Dukhobar Rd, Eugene, OR 97401 designed the package for S-100 video boards of 16 lines by 64 characters, adaptable to 32-character boards. The software is provided on a KIM compatible cassette tape.

Circle 431 on Inquiry Card

Enhanced Capabilities of Macro Assembler Retain Speed

MACRO-80, a 14k assembler for the 8080/Z80, comes in a package with a linking loader, library manager, and cross-reference facility. Single copies cost \$200. Assembling over 1000 lines/min, the assembler supports a complete Intel standard macro facility. Memory is the only limit on the nesting of macros.

Code is assembled in relocatable modules that the linking loader manipulates. An expanded set of conditional pseudo-operations, such as testing of assembly pass, symbol definition, and parameters to macros, enhances conditional assembly capability. Conditionals may be nested up to 255 levels.

Other features added by Microsoft, 10800 NE Eighth, Suite 819, Bellevue, WA 98004 are comment blocks, variable input radix from base 2 to base 16, titles and subtitles, variable page size, and octal or hexadecimal listings. The assembler accepts both 8080 and Z80 opcodes, selectable with a pseudo-op or command switch. The user controls assembler output through various listing control statements.

Circle 432 on Inquiry Card

Simplified Editor Creates Color Graphics Using Keyboard Commands

A color graphics editor software package is compatible with existing 48-line Intelligent Systems Corp's Intecolor™ series of intelligent graphic terminals containing 8-color displays. The package resides in firmware. With this PEDIT (picture editor) software, a user can create any color graphic display by using simple keyboard commands to draw vectors, horizontal and vertical lines, rectangles, and symbols, without having prior programming knowledge.

Symbols differ from displays in that sets of up to 100 symbols can reside in RAM for addition to a display on command from the keyboard or remote host computer. Like displays, these symbol sets can consist of any graphics or alphanumeric data, and can be stored on diskette for later recall. USDATA Engineering, Inc, 14241 Proton Rd, Dallas, TX 75234 also supplies a hardcopy print-out option on a Printronix printer/plotter.

Circle 433 on Inquiry Card

PASCAL Compiler's Object Code Executes on 8080/Z80 Microprocessors

Developed for the CommFile 130 microcomputer floppy disc system with 44k bytes of memory, this efficient compiler is a standardized implementation of Wirth's PASCAL as defined by the "PASCAL User Manual and Report." The compiler is a utility program under the operator oriented disc operating system of DMG, a div of Cetec Corp, 2300 Owen St, Santa Clara, CA 95051.

Source code for PASCAL programs is loaded onto the microcomputer's floppy disc using the standard editor. The compiler then produces object code which is executable on 8080 or Z80 microprocessors. Compiled programs can execute in systems with smaller memories. Proprietary applications compiled on a development system may be provided in binary form to fully protect the source. CommFile users may obtain the compiler for a license fee of \$500.

Circle 434 on Inquiry Card

Language Addition to CRT Forms Small Business System

MICROBOL is a high level language for developing and running business applications on floppy disc configurations. It operates with Digital Equipment Corp's VT-100 CRT, providing such screen attributes as split screen scrolling, dynamic cursor addressing, and full software control of all screen options. It operates within 16k words of processor memory, supporting application programs that are shared by multiple users. The language combines with the CRT and floppy disc processor to create a small business system.

The single software package from MICROBOL, Inc, 711 E Semoran Blvd, Suite 118, Altamonte Springs, FL 32701 contains the operating system, language processor, and disc facility. Data fields may be defined and re-defined. Language statements are compiled incrementally and executed interpretively. The software permits individual and vectored transfer of program control, indexing, nested subroutines and subroutine return stack control, and overlapped I/O operations via program control. It also provides argument (operand) substitution, automatic decimal point control, numeric field editing, and a simplified uniform indexed disc file facility for direct access of data records by key. Circle 435 on Inquiry Card □

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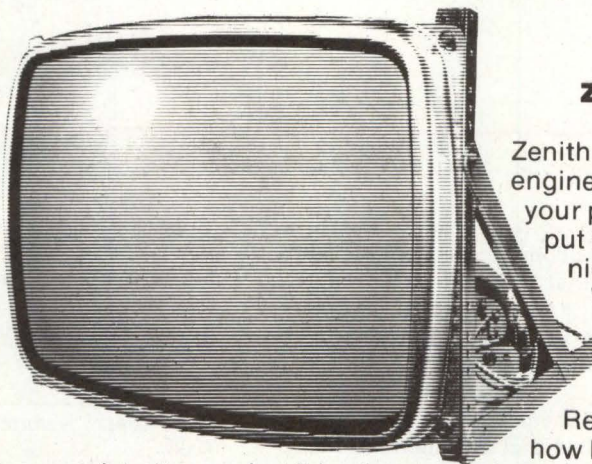
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RAM RELIABILITY IN LARGE MEMORY SYSTEMS—SIGNIFICANCE OF PREDICTING MTBF

Robert Koppel

Intersil Incorporated,* Memory Systems Division,
Cupertino, California

Reliability of large memory systems relates directly to the reliability of individual random-access memory semiconductor devices making up that system. System reliability can be predicted from a statistical study of failure modes in individual devices, and can be increased through use of low cost error correction techniques (to be covered in March).

There are two basic types of memory error, as indicated in Table 1. Both are drift-related and are highly sensitive

to temperature. First, there are the "hard errors"—permanent errors relating to power shorts, open leads, or other intrinsic flaws. These are permanent physical defects in the memory structure. In contrast are "soft errors"—random, nonrecurring single-bit errors, that are essentially

*Mr. Koppel is currently employed at Nitron Corp, Cupertino, Calif.

TABLE 1
Summary of Memory Errors in 16k RAMs

<u>Error Type</u>	<u>Source</u>	<u>Range of Failures/10⁶ h</u>	<u>Source of Data</u>	
Hard (permanent failure)	Catastrophic RAM failure	0.03 to 0.1	Field experience and accelerated temperature testing	
	Catastrophic IC failure	0.01 to 0.075	Field experience	
Soft (non-repeating)	Traditional	System noise Pattern sensitivity Temperature sensitivity	0.1 to 1.0 during infant mortality 0.04 to 0.3 after infant mortality	Manufacturing test and field experience
	Alpha-radiation	Trace of uranium and thorium in package material	0.001 to 0.1	Manufacturing test and field experience

noiselike, and not associated with any physical defect. In the present state of technology, hard errors are the less troublesome of the two. Hard failure rate experienced with several industry standard 16k RAMS appears to be approaching about 0.03 failures/10⁶ h (at 70 °C).

Referring to Table 1, it can be seen that soft errors come in two varieties. On the one hand are the traditional errors caused by system noise, pattern sensitivity, or temperature sensitivity. On the other, there are alpha-radiation errors—errors resulting from trace quantities of radioactive uranium or thorium in package materials. The ionizing alpha particles generate electron-hole pairs in the semiconductor material, leading to random shifts between 1 and 0 charge states in bit locations.

Soft Errors

“Traditional” soft error rates result from a combination of noise, data pattern, and temperature effects that push the RAM beyond its normal operating range. Reduction of these errors requires that substantial guard bands be provided during RAM testing on such key parameters as supply voltages, refresh timing, and operating temperature. In addition, PC boards must be designed to minimize noise. This includes the use of multilayer boards with internal power and ground planes, along with tight layout of the storage array and drivers to minimize the inductance of current carrying traces. It also includes proper decoupling of RAM supply voltages at the RAM components with high frequency capacitors.

Inevitably, a small number of marginal RAMS will pass component test and be mounted on the memory board. Resulting “infant mortality” defects are weeded out during manufacturing test by imposing wide guard bands at the card level. The subsequent soft error rate appears to approach 0.1 failures/10⁶ h, which is roughly three times the hard error rate.

As cell sizes have diminished to accommodate ever-increasing densities, another source of errors, the alpha-radiation mechanism, has been identified. Errors induced by alpha particles vary widely, and are highly dependent upon package material and storage cell design; ie, large storage nodes are less sensitive than small ones. From this it follows that many of the RAM chips that have recently undergone “shrink” redesigns will have an increased susceptibility to alpha-particle effects.

The industry has limited experience in dealing with errors induced by alpha particles, because chip designs up to now have been insensitive to this effect compared to the effects of traditional soft errors. However, experience indicates that, for conservatively designed 16k RAMS, alpha-particle failure rates are an order of magnitude lower than those of traditional soft errors. Therefore, traditional soft errors will predominate at roughly 3X the hard error rate and 10X the alpha-particle rate unless special care is taken to reduce them at the RAM and board test levels.

Memory Failure Data

Field reliability data on over 2G bytes of MOS memory devices, installed and operated over several years in add-on and add-in systems in mainframe applications, have been compiled. Through collection of fault data on cards returned for repair, component failure rates have been determined accurately, reflecting the actual environment in which those components are required to perform. These failure rates are in most cases similar to or lower than those listed in MIL-HDBK-217B for ground environment and screened parts.¹

Field data on 16k RAMS is limited, because of their relatively short history in operating systems. However, data that are available suggest that 16k RAM failure rates are rapidly decreasing (see Fig 1) indicating an industry trend. Of primary interest in the figure is the curve indicating that the rate of decrease for 16k RAMS has been consistently greater than that of 4k RAMS at corresponding points in time. This suggests a high probability that 0.2 failures/10⁶ h will be reached by mid-1979. To reflect present conditions, a value of 0.3 failures/10⁶ h will be used in making mean time between failure (MTBF) predictions for 16k RAMS. This reflects conservative application of Table 1 values, using the higher ends of the probability ranges.

Memory System Reliability

As previously stated, traditional soft errors will usually dominate in memory systems employing today's popular RAM sizes (4k, 8k, and 16k bits). For a well designed system, the overall RAM failure rate will lie in the 0.1- to 0.3-failures/10⁶-h range.

TABLE 2
MTBF of 64k x 16 Memory System

Component	λ_p Failures/10 ⁶ h	Device Quantity	Total Failures/10 ⁶ h
IC	0.050	50	2.50
Ceramic capacitor	0.01	64	0.640
Tantalum capacitor	0.02	10	0.20
Resistor	0.001	40	0.040
PC Board	0.50	1	0.50
Delay line	0.008	1	0.008
16k RAM	0.30	64	19.2
Total Nonstorage			4.248
Total Storage			19.2
Total λ_s			23.45 failures/10 ⁶ h
MTBF			42.600 h

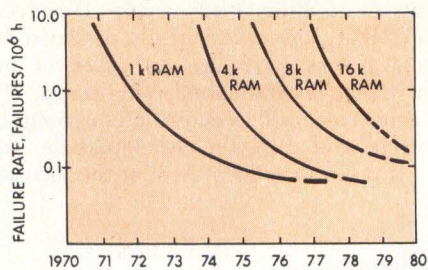


Fig 1 RAM failures vs time. RAMs of greater capacity, introduced at later dates, lag behind those of lower capacity in reliability. However, failure rate for larger RAMs drops more steeply, reflecting industry trend

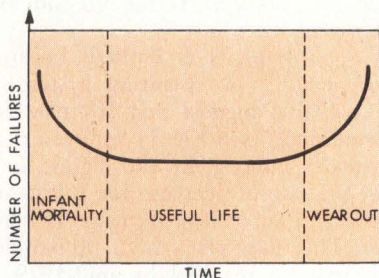


Fig 2 Failure rate as function of age. Infant mortality and wearout conditions involve greater failure rates. Probability calculations utilizing exponential reliability equation are based on steady state condition during "useful life"

Soft errors are due to a combination of the following effects: data pattern sensitivity, refresh margin (temperature sensitivity), aging due to thermal cycling, insufficient power supply margins, and insufficient system noise margins. Although these effects can be virtually eliminated through careful design, there is a hazard in going too far. An attempt to eliminate soft errors entirely may place such severe requirements on component, power supply, temperature, and layout density margins that the system may not be economically feasible. Rather than incurring these penalties of over-design, it is better to design a system with reasonable margins, which can tolerate occasional soft errors.

One technique that is commonly used to accommodate occasional soft errors is the use of an extra parity bit per word. Data are written into the parity bit to make the total number of ones in the word even (or odd). Thus a single bit error during a read access will be flagged by the parity detector. This signal will initiate a reaccess of the same word, one or more times, which will usually clear the problem. A few applications can permit large soft error rates, while many more systems can tolerate soft errors through the use of parity checking and reaccessing. When these methods prove inadequate, error checking and correction (ECC)—to be discussed in March issue—will usually solve the problem.

System MTBF Projections

Reliability requirements that are normally imposed on semiconductor memory systems necessitate a prediction of MTBF. MTBF is symbolized as M in the reliability equation:

$$R(t) = e^{-\lambda t} = e^{-t/M}$$

where

$R(t)$ = Reliability = Probability of successful operation over a time, t , throughout the useful life of the product.

λ = Chance failure rate of the system (assumed to be constant throughout useful life and usually expressed in failures per 10^6 h).

Then

$$M = 1/\lambda = \text{MTBF (usually expressed in hours)}$$

The term "useful life" is defined as the time after infant mortality failures have been weeded out and before wear-out mechanisms begin to come into play (see Fig 2).

As a direct consequence of the reliability equation, the cumulative probability of error-free operation is 63% after a time period equal to MTBF. Furthermore, a 90% probability of error-free operation occurs after a time period approximately equal to one-tenth of the MTBF. These values should be taken into account in estimating the predicted reliability of a given design.

Table 2 lists components utilized in a single card 64k x 16 memory system, including the quantity of each. Also listed is the failure rate, λ_p , for each component, based on field data. Since it is assumed (worst case) that a failure in any component will cause a system failure, the overall system failure rate, λ_s , is the sum of the component failure rates, each weighted by quantity used. The system failure rate of 23.45 failures/ 10^6 h, resulting in a system MTBF of 42,600 h for the single card 64k x 16 system is totally dominated by RAM failures. In this calculation, no distinction is made between the device failure modes; the only consideration is that device failures result in system failures that occur during the useful life period (after infant mortality) and are characterized by the component failure rates in Table 2.

If the MTBF prediction of 42,600 h meets the system requirement, all that remains is to build several systems and to demonstrate that, indeed, no more than 23 failures occur for each 10^6 h of operation at the maximum specified temperature. (A procedure for reliability demonstration is available; see Ref 2.)

If the requirement for memory capacity should increase so that additional identical memory boards are required in the system, the system failure rate will be the sum of the λ_s for each card. Hence a 4-card system (256k x 16) would have a failure rate of 93.8 failures/ 10^6 h or an MTBF of 10,650 h.

Summary

Reliability of a random-access memory is a function of several variables: number of elements in the memory, failure rate per element, density of the RAM, and operating parameters such as temperature and voltage. Statistical techniques enable us to predict these reliabilities as a function of the relevant variables. In the second part of this discussion, to be published in March, this descriptive approach to RAM reliability will be extended into error correction techniques and the consequent improvements that are practically attainable in memory reliability.

References

1. MIL-HDBK-217B, *Reliability Prediction of Electronic Equipment*, Sept 1974
2. MIL-STD-781B, "Reliability Testing," July 1969

**C-R-T, C-R-T, alpha-numeric,
ASCII-key, multi-key, programmability,
Blinkity, blankety video-bility,
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CIRCLE 77 ON INQUIRY CARD



Memory Family Expansion Adds 16k Military Version and 32k Low Power Dissipation EPROMs

Meeting the speed requirements of microprocessors now in production, a 32k-bit ultraviolet erasable and electrically programmable read-only memory has been added to an existing fourth generation family of high density devices. Organized as 4k x 8, the 2732 EPROM provides a 3-state output for direct bus interface. The manufacturer, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, has also introduced the M2716, a military version of the existing 16k-bit 2716 EPROM, capable of operating over an extended temperature range of -55 to 100 °C. Both of these fully static devices, each operating from a single 5-V power supply, are pin compatible with one another, as well as with 2332 and 2364 ROMs.

32k-Bit EPROM

Having a typical supply current of 85 mA (active operation) and 15 mA during standby, the 32k-bit memory is claimed to be the lowest power/bit EPROM on the market. (Maximum supply currents are specified at 150 mA in active operation and 30 mA in standby.) Chip enable control (\overline{CE}) serves as the primary device selecting function. When receiving a TTL high input signal it allows the deselected memory to enter the reduced-power standby mode.

With separate output-enable (\overline{OE}) control, bus contention in multiple microprocessor systems is eliminated. The microcomputer determines the time during which data must be presented on the bus and then releases the bus by way of the output-

enable line, for use by other devices such as memories or peripherals. In other words, with 2-line control, the microprocessor is always in control of the system, rather than passing this control to a particular memory device and waiting for data to become available. Because EPROMs are commonly used in larger memory arrays, this 2-line control ensures that system bus contention will not occur. Selection by \overline{CE} and common connection to all memory units in the array (and direct connection to the microprocessor) by way of \overline{OE} assures that each memory device is active only when data are desired from that particular device.

Other features of the 32k-bit memory include a 450-ns max access time, $\pm 5\%$ power supply tolerance, and erasure when exposed to light of wavelengths shorter than approximately 4000 Å. Permissible temperature range is from -10 to 80 °C under bias and from -65 to 125 °C in storage.

Single-pulse/single-location programming is possible, with TTL levels required for the address and data inputs. When address and data are stable, a single 50-ms active-low TTL program pulse is applied to the address location to be programmed. Users can program any location at any time, either individually, sequentially, or at random.

Circle 350 on Inquiry Card

Military Standard 16k-Bit EPROM

The 16k device has a static power-down mode that reduces active power dissipation by over 60% without in-

creasing access time. It also features single address location programming that allows all 16,384 bits to be programmed in only 100 s. Because TTL level control signals are used, all programming can be done onboard, in the system, in the field. Other features include a 450-ns max address time and a $\pm 10\%$ supply tolerance. Absolute maximum ratings for both EPROMs require that all input and output voltages with respect to ground lie between 6 and -0.3 V.

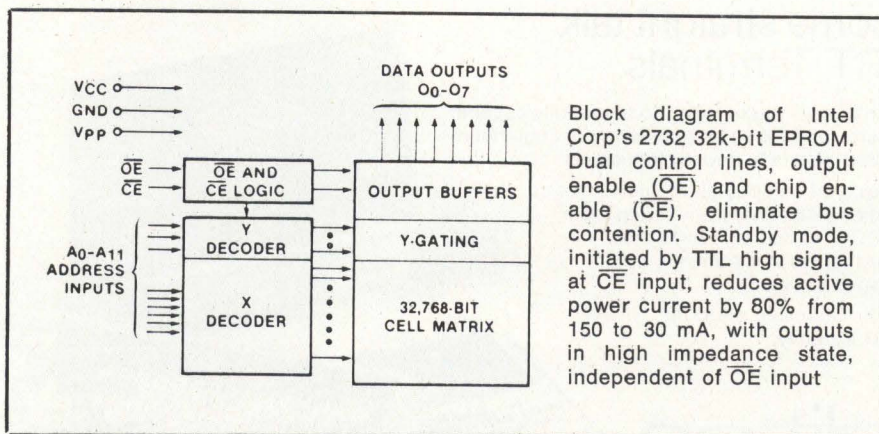
Circle 351 on Inquiry Card

Synchronous Serial Data Adapter Interfaces S6800 Bus Systems

S6852, a synchronous serial data adapter containing logic for simultaneous transmission and reception in bus organized systems, provides a bidirectional serial interface for communications between systems using the S6800-type data bus structure. Produced by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, the device finds its typical applications in floppy disc controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

The data adapter provides the logic for transmitting and receiving standard synchronous characters of 7- to 9-bit length. It includes capabilities for select, enable, read/write, and interrupt to allow data transfer using the S6800 or 6500 8-bit bidirectional data bus at rates as high as 600k bits/s. Parallel data are transmitted serially with automatic synchronization, fill-character insertion/deletion, and error checking.

Functional configuration of the device is programmed via the data bus during system initialization. At the bus interface, the adapter appears as two addressable memory locations. Internally there are seven registers: two read-only and five write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control 1, Control 2, Control 3, Sync Code, and Transmit Data. These programmable registers provide for variable word length, transmit, receive, synchronization, and interrupt control. The serial interface consists of serial I/O lines with independent clocks and four peripheral/modem control lines.



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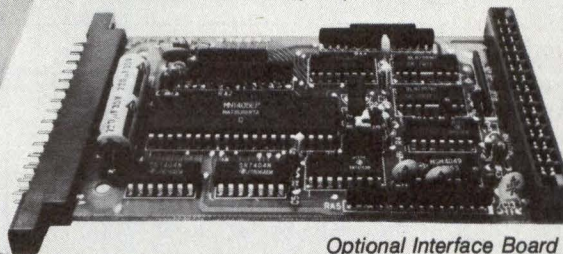
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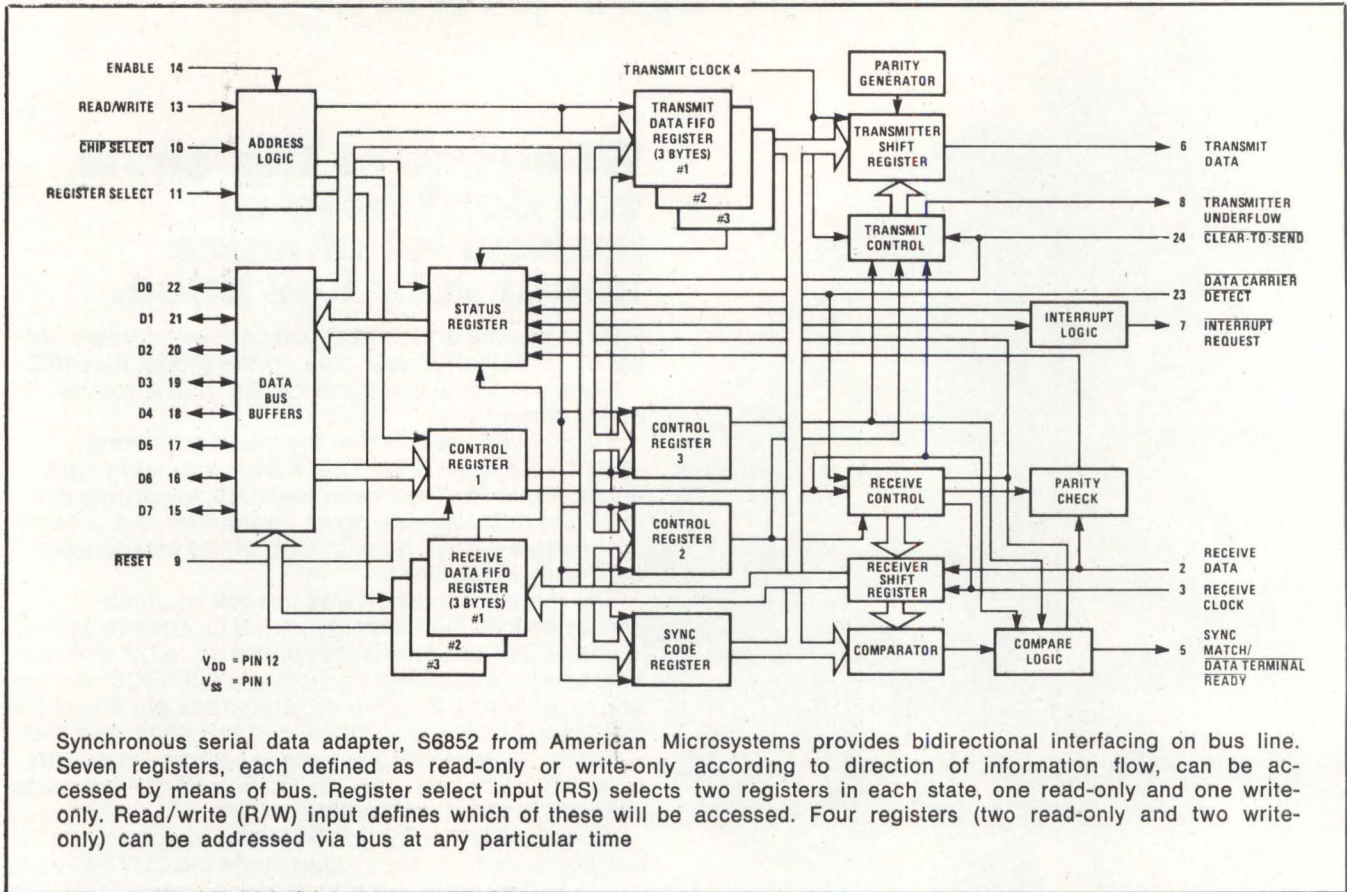


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Synchronous serial data adapter, S6852 from American Microsystems provides bidirectional interfacing on bus line. Seven registers, each defined as read-only or write-only according to direction of information flow, can be accessed by means of bus. Register select input (RS) selects two registers in each state, one read-only and one write-only. Read/write (R/W) input defines which of these will be accessed. Four registers (two read-only and two write-only) can be addressed via bus at any particular time

Additional features include three bytes of FIFO buffering on both transmit and receive; optional even and odd parity; and overrun, overflow,

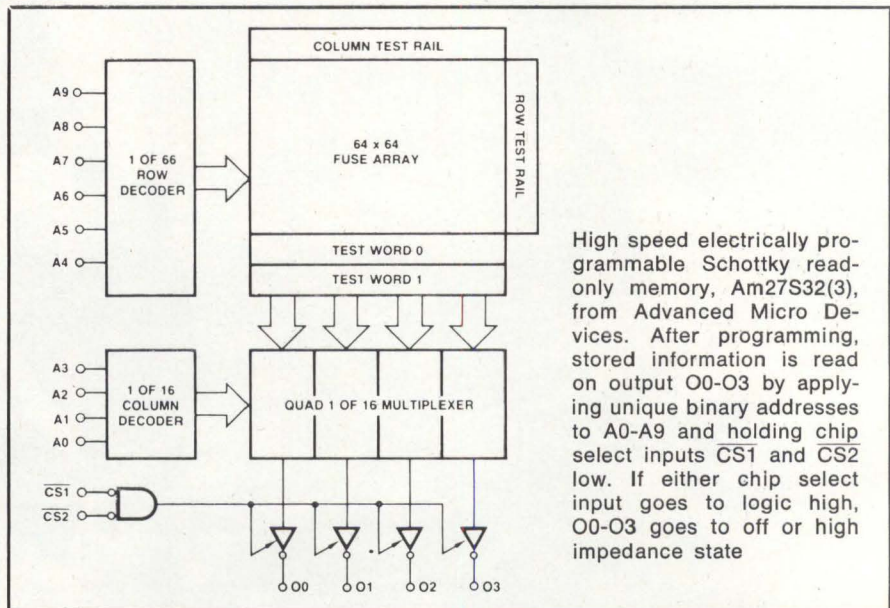
and parity status. Absolute maximum ratings require that supply and input voltages lie between -0.3 and 7.0 V. Temperature must stay between 0

and 70 °C for operation and between -55 and 150 °C for storage. The units are housed in either plastic or ceramic 24-pin DIPs.
Circle 352 on Inquiry Card

Fuse Technique Produces High Performance 4k-Bit P/ROMs

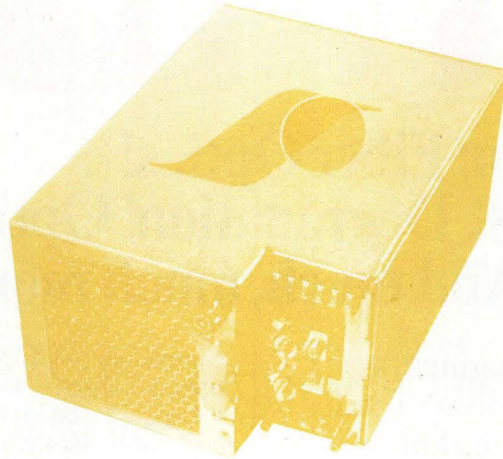
A 55-ns max commercial range access time is provided by a 4k-bit user programmable read-only memory, organized as 1024 x 4, and available in both open collector (Am27S32) and 3-state (Am27S33) output versions. For parts meeting military temperature extremes, max access time is 70 ns.

Fabricated by a proprietary platinum-silicide fuse technology, all of these devices from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086 are produced with a fusible link at each memory location storing a logic low and can be selectively programmed to a logic high by applying appropriate volt-



High speed electrically programmable Schottky read-only memory, Am27S32(3), from Advanced Micro Devices. After programming, stored information is read on output O0-O3 by applying unique binary addresses to A0-A9 and holding chip select inputs CS1 and CS2 low. If either chip select input goes to logic high, O0-O3 goes to off or high impedance state

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DC INPUT MODEL		PM2721	PM2722	---	---	
OUTPUT VOLTAGE	TYPE NUMBERS (Add Amps in Blanks)		OUTPUT CURRENT	OUTPUT CURRENT	OUTPUT CURRENT	OUTPUT CURRENT
	AC MODELS	DC MODELS				
2	20	2F	100	200	400	300
3	30	3F	60	100	200	200
5	50	5F	50	100	200	200
5	50	5F	60	120	---	---
5	50	5F	---	150	300	300
12	120	12F	25	90	120	120
15	150	15F	25	90	100	100
18	180	18F	22	45	90	90
21	210	21F	18	38	76	76
24	240	24F	16	33	66	66
28	280	28F	13	27	54	54
48	480	48F	8	16	32	32
SIZE (INCHES)			5x8x11	5x8x11	5x16x11	5x8x15
(CENTIMETERS)			12.7x20.3x27.9	12.7x20.3x27.9	12.7x40.6x27.9	12.7x20.3x38.1
WEIGHT (POUNDS)			16	18	35	25
(KILOGRAMS)			7.3	8.2	15.9	11.4

MULTIPLE OUTPUT SUPPLIES

AC INPUT MODEL		PM2675A	PM2676A	PM2677A	PM2678A			
DC INPUT MODEL		PM2775	PM2776	---	---			
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MAIN CHANNEL	OUTPUT VOLTAGES AVAILABLE	2, 3, 5, 12, 15, 18, 21, 24, 28, 48						
	MAX. POWER IN WATTS	250W	500W	600W	750W			
SECOND CHANNEL	OUTPUT VOLTAGE	5	12	15	18	21	24	28
	OUTPUT CURRENT MAX. (see note 1)	7	7	7	CHECK FACTORY			
THIRD CHANNEL	OUTPUT VOLTAGE	5	12	15	18	21	24	28
	OUTPUT CURRENT MAX. (see note 1)	10	10	10	CHECK FACTORY			
FOURTH CHANNEL	OUTPUT VOLTAGE	5	12	15	18	21	24	28
	OUTPUT CURRENT MAX.	4	4	4	4	4	3	3
SIZE (INCHES)		5 x 8 x 11 1/2						
(CENTIMETERS)		12.7 x 20.3 x 29.8 (see note 2)						
WEIGHT (POUNDS)		20						
(KILOGRAMS)		9						

Note 1: Higher currents available to 30 Amperes.

Note 2: Add 1 9/16" (4 cm.) for external fan on Models PM2677A, PM2678A.

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Fiber optics is one form of digital transmission. A detailed discussion on optocouplers for digital transmission will expand the designer's realm of possible choices in system implementations.

CTR Degradation

Of special interest to experienced designers is HP's treatment of CTR degradation, a controversial and frequently misunderstood subject among users of optocouplers. Intensive research has been undertaken by Hewlett-Packard in the past two years to compile a detailed report about CTR degradation. Hewlett-Packard will now share this same information with you in the seminar.

Optical Scanning

The discussion on optical scanning and encoding systems will cover theory and techniques. Applications of this technology are: computerized checkpoints, inventory control, computer and micro peripherals.

Contrast Enhancement

LED displays can now be viewed in direct incident sunlight. This technology has recently been refined,

complementing LED display products available in the marketplace. Learn the implementations of such a display based on designs incorporating the concepts of both luminance and chrominance contrast.

Backlighting

Solid state LED products are now available for use in backlighting applications. What are the illumination requirements for backlighting? How can light bar modules be used? What are some design considerations? These questions are answered in the discussion of backlighting. Applications of this technology include illuminating legends, indicators, bar graphs, and lighted switches.

Alphanumeric Display Systems

Over the past two years, the need for alphanumeric displays has grown rapidly due to the extensive use of microprocessors in new system designs. The presence of the microprocessor in such systems substantially simplifies the traditionally difficult task of designing an alphanumeric display into a system. Learn how an alphanumeric microprocessor-based display support unit may act as an interface between a keyboard, a display, and a host processor. Basic interface concepts as well as applications of smart interfaces will be discussed as the concluding seminar topic.

You will receive all of this valuable optoelectronic instruction by attending one of the scheduled seminars. You will also receive a hardbound copy of the McGraw-Hill published Hewlett-Packard Optoelectronics Applications Manual (retails at \$22.50), plus an additional 100 page addendum specifically prepared for this seminar. The Manual and Addendum will serve as reference material for your use after the seminar.

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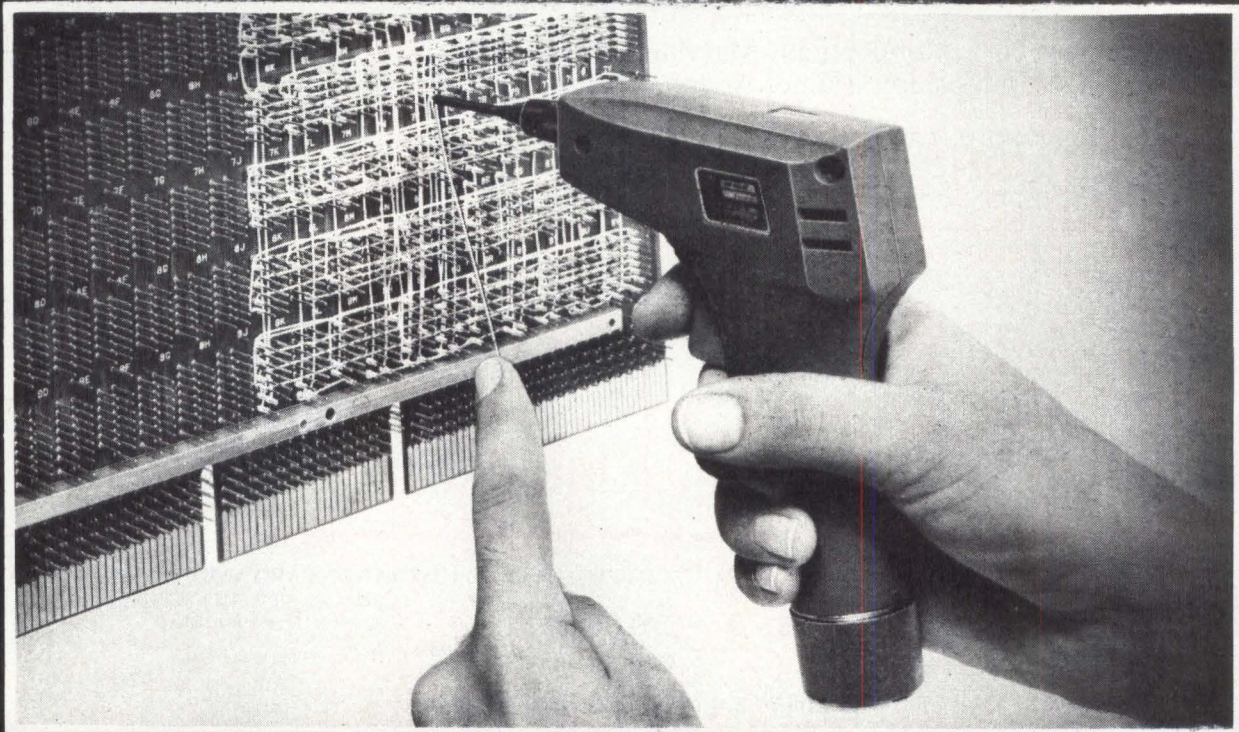
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AROUND THE IC LOOP

ages to the circuit. Utilizing easily implemented programming and common personality card sets), these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacture to insure extremely high field programming yields, and to produce excellent parametric correlation.

All devices in this family, which include 256-, 1024-, 2048-, and 4096-bit parts, use the same circuit design, creating a generic series that can be programmed with a single personality card set. Fully compensated for both voltage and temperature, these circuits provide flat ac performance over the military as well as the commercial temperature and supply voltage ranges. Additionally, selective feedback techniques have been incorpor-

ated in the design of the devices to minimize the propagation delay through critical paths, resulting in fast access times—claimed by the manufacturer to be the industry's fastest of its kind in a 1k x 4-bit configuration.

The P/ROMs are processed using the company's proprietary low power Schottky technology. Three-micron (3×10^{-6} -m) thick epitaxial layers are combined with washed emitters, composite masking, dual-layer metalization, and barrier metal Schottky diodes. Available in 18-pin packages, and thereby offering pin-for-pin replacement capability for industry standard products, these parts undergo 100% processing to the requirements of MIL-STD-883.

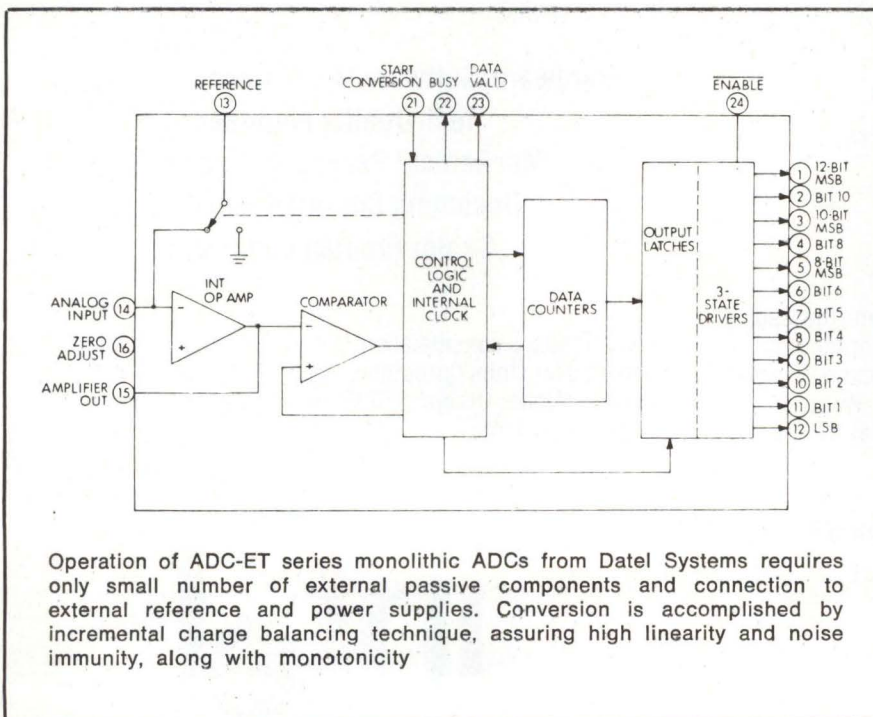
Circle 353 on Inquiry Card

CMOS A-D Converters Provide High Linearity With 3-State Outputs

Monolithic CMOS technology, 3-state outputs, and accuracy to 12 bits characterize the ADC-ET series of analog-to-digital converters, provided by Datal Systems, Inc (1020 Turnpike St, Canton, MA 02021). Operating from a ± 5 -Vdc supply with 5-mA max current drain, the devices fea-

ture a typical linearity of $\pm \frac{1}{4}$ LSB. Maximum conversion times are 1.8, 6.0, and 24 ms for the 8-, 10-, and 12-bit models, respectively.

An ADC of this series employs an operational integrator, comparator, CMOS switch, clock, two counters, latching output buffers, and digital control circuitry on the single silicon chip. Externally, the units require a voltage reference, two metal film resistors, and several compensation

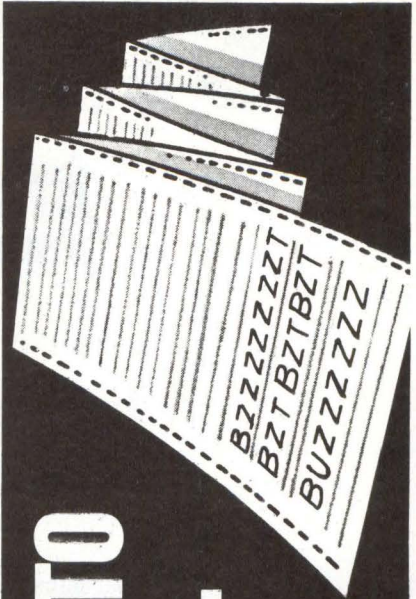


A POWER TOOL WAS CUTTING INTO CHARLIE SMITH'S DATA STREAM.

Charlie fixed it with a Belden Shielded Electronic Cord.

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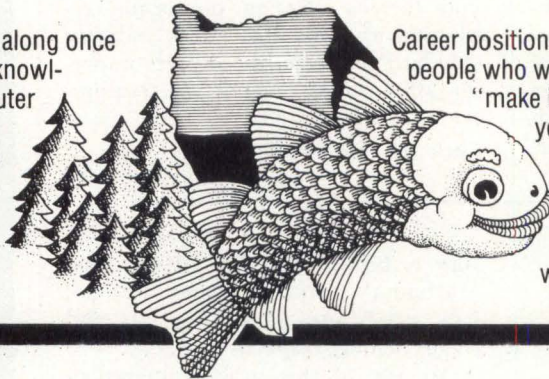
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AROUND THE IC LOOP

components for operation. Connection and application is simple and straightforward.

The quantized feedback integration technique provides noise immunity. Inherent monotonicity results in no missing codes over the full operating temperature range. At the completion of a conversion, the binary coded result appears in parallel form on discretely controlled latched outputs, which are CMOS, low power TTL, or low power Schottky TTL compatible. The controllable outputs may be switched to a high impedance or off state by holding the enable high.

Accurate, Stable Monolithic D-A Converters Run Fast

Settling times as fast as 85 ns (to $\pm\frac{1}{2}$ LSB), with $\pm\frac{1}{2}$ LSB nonlinearity, and a gain tempo of ± 5 ppm/ $^{\circ}$ C are provided by monolithic digital-to-analog converters. Both a 10-bit model (HI-5610) and a 12-bit model (HI-5612) are produced by Harris Semiconductor Products Div, PO Box 883, Melbourne, FL 32901 for high performance applications. The manufacturer states that the settling times are the fastest available of any commercially marketed units.

Since feedback and gain-setting resistors are included on the mono-

12-Bit A-D and D-A Converters Offer Speed at Low Power

High speed operation and low power consumption are featured in two 12-bit converters—one of these being an analog-to-digital type, the other digital-to-analog. Both devices provide low gain tempcos and models specified over either commercial or military temperature ranges.

Manufactured by Analog Devices Semiconductor, 829 Woburn St, Wilmington, MA 01887, the 12-bit ADC is implemented in a design incorporating only two IC chips. The AD574 features a fast successive approximation conversion to $\pm 0.01\%$ in 25 μ s, priced from \$34.50 in 100s. The ADC includes microprocessor interface control logic, clock, comparator, succes-

Other features include a typical gain tempo of 25 ppm/ $^{\circ}$ C (exclusive of external reference), a required 20- μ A input reference current, and 0- to 10- μ A analog input range. The devices can also be run in a standby mode with output data latched while drawing only 200 μ A.

Maximum ratings require that I_{in} and I_{REF} lie between ± 10 mA, that digital input voltage lie between -0.3 and V_{DD} 0.3 V, and that $V_{DD}-V_{SS}$ be limited to 18 V. Package dissipation must not exceed 500 mW. Devices are provided in 24-pin plastic packages for 0 to 70 $^{\circ}$ C versions and in 24-pin ceramic packages for the -55 to 125 $^{\circ}$ C military versions. There is also a -25 to 85 $^{\circ}$ C version of the 12-bit unit in a ceramic package.

Circle 354 on Inquiry Card

lithic chip, the number of components and their required board space is significantly reduced. Onchip resistors also afford better temperature tracking than offboard components, enabling better overall system accuracy to be achieved.

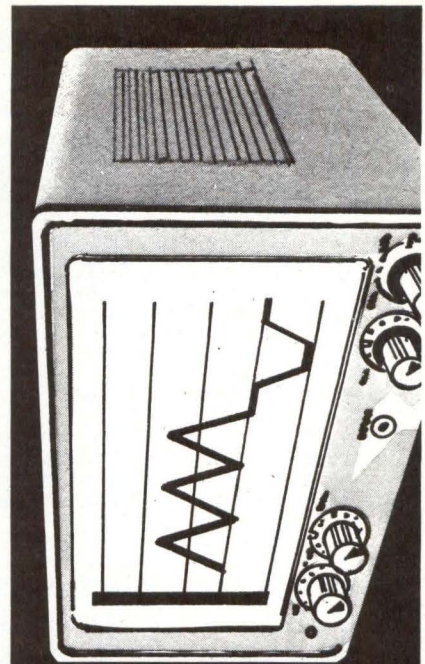
Typical applications include machine tool process controls, microprocessor based control systems, precision instrumentation, and automatic test equipment. The units are built to meet MIL-grade applications for missile guidance systems, avionics, and radar. Generally, the devices are compatible with the speed of any equipment interfaced to a microprocessor or a CRT system.

Circle 355 on Inquiry Card

sive approximation register, 3-state output buffers, and 12-bit DAC (AD565). It interfaces directly to an 8-, 12-, or 16-bit microprocessor bus. Gain tempo is as low as 10 ppm/ $^{\circ}$ C, max; power dissipation is typically 455 mW.

Model AD574J is guaranteed for ± 1 LSB and K and L grades for $\pm\frac{1}{2}$ LSB linearity over a 0 to 70 $^{\circ}$ C temperature range. Similarly, the AD574S is guaranteed for ± 1 LSB and the T and U grades for $\pm\frac{1}{2}$ LSB over -55 to 125 $^{\circ}$ C. Over the full temperature range, no more than one bit of missing code is guaranteed for the J and S grades, while all other models guarantee no missing codes.

Said to be the industry's first complete, monolithic 12-bit DAC to include a buried zener reference, the AD565 settles to $\pm 0.01\%$ in 200 ns,



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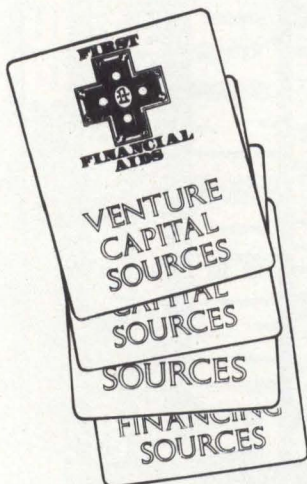
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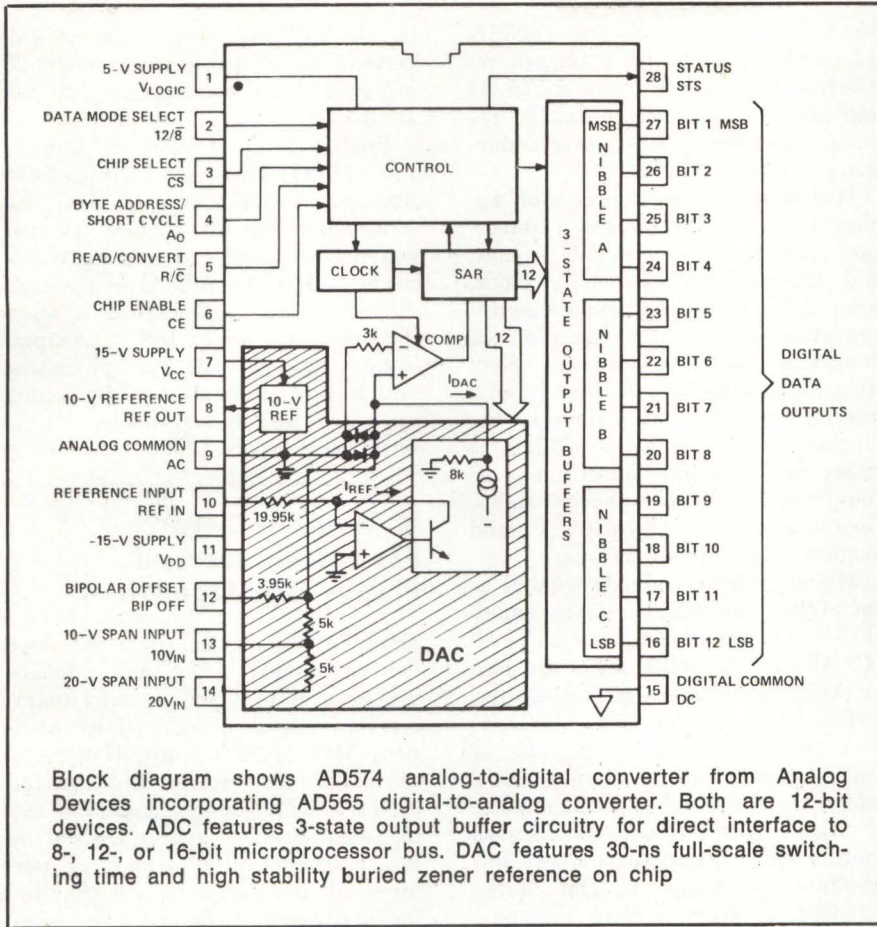
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typ, and is priced from \$16 in 100s. The reference and onchip application resistors are available for external use and are matched to the converter to provide the low gain tempcos and minimum full-scale and bipolar offset errors. Typical power consumption, including the zener reference, is 225 mW. Full-scale switching time is 30 ns (200-ns typical settling time to $\pm 0.01\%$). All grades are guaranteed monotonic over

temperature and are pin compatible with industry standard 563 sockets.

The DAC is available in four grades. Models AD565J and K are specified for use over the 0 to 70 °C range and are both available in either hermetic, size-brazed ceramic or plastic 24-pin DIPs. The AD565S and T are specified over the -55 to 125 °C range and are housed in the hermetic, size-brazed ceramic 24-pin DIP.

Circle 356 on Inquiry Card

Opto Couplers Are Second Sourced

The second sourcing of a series of industry standard opto couplers has been announced by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036. Isolation voltage for all couplers is specified at 7500 Vac peak (5 s), said to be in excess of the originator's specifications. A total of 34 models have been made available, including 25 phototransistors and 9 photodarlington out-

put couplers, in standard 6-pin plastic DIPs.

Phototransistor types include: General Electric H11A1, 2, 3, 4, 5, 10, 520, 550, and 5100; Litronix PL1, 12, 15, 16, and 74; Monsanto MCT2, 2E, 26, and 210; and Texas Instruments TL111, 112, 114, 115, 116, 117, and 118. Photodarlington types include General Electric H11B1, 2, 3, and 255; Monsanto MCA230, 231, and 255; and Texas Instruments TL113 and 119.

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Bipolar Digital Gate Array Totals 265 Cells

An array of 2120 uncommitted components arranged in a matrix of 225 logic cells and 40 peripheral interface cells with eight components each is contained on a chip 131 mils (3.33 mm) square. Designed to accommodate either digital or linear circuitry, the device is available in standard, low power, and high speed configurations.

Produced by Interdesign, Inc, 1255 Reamwood Ave, Sunnyvale, CA 94086, the ULA-225 (Uncommitted Logic Array) is supported by a software kit that enables users to design and lay out custom ICs. Priced at \$59, the kit includes guidelines for designing linear and digital circuits, component characteristics, IC layout sheets, adhesive functional overlays, and kit parts for breadboarding. Customer integrations, which include delivery of 20 prototype circuits, are priced at \$2800 with a 4- to 6-week turnaround time.

Additional features of the bipolar digital gate device include a single 5-V supply, TTL and CMOS compatibility, toggle rates to 10 MHz, and 40-mA output drive. For a 200-gate system, typical dissipation is 50 mW (low power array), 500 mW (standard array), or 650 mW (high speed array). The high speed array has been optimized for low power Schottky TTL compatibility, giving a typical performance of 10-ns gate delay and 10-MHz clock rate.

Circle 358 on Inquiry Card

Fast MIL-Spec ADCs Significantly Cut Power Consumption

Two series of analog-to-digital converters providing 8-bit and 12-bit conversions are specified from -55 to 125 °C by their manufacturer, Hybrid Systems Corp, Crosby Dr, Bedford Research Pk, Bedford, MA 01730. Both types of ADCs are available with either full MIL-STD-883B, Class B, or commercial/industrial processing. The 8-bit device, ADC542, designed to be a plug-in replacement for Burr-Brown's ADC82 devices, offers a 35% reduction in power consumption, drawing a total of 650 mW.

Similarly, the 12-bit device, ADC581-12, is designed to be a plug-in replacement for Burr-Brown's ADC85/84 and Datel's ADC-HX12B/HZ12B devices, providing a 70% power reduction to 570 mW.

Well-suited to microprocessor applications, the 8-bit ADC has a conversion time of 2.5 μ s typ, 2.8 μ s max, and includes precision DAC, clock, comparator, reference, and successive approximation register. Simple pin jumpering allows the user to select from three unipolar and three bipolar input ranges. Output coding in the bipolar mode is user selectable as either complementary offset binary or complementary 2's complement codes. Overall tempo is ± 45 ppm/°C, and longterm stability is 0.1%/year.

Military versions are designated as ADC542B-8; commercial versions (model C-8) are specified from -25 to 85 °C. All models in this series are hermetically sealed in 24-pin metal DIPs.

The 12-bit ADC provides a conversion time of 17 μ s (typ), 20 μ s (max), and includes internal clock, reference, and input buffer amplifier. It can be short cycled to obtain even shorter conversion periods where less resolution is required. The design provides an external clock rate control and the option to use an external clock for synchronization. Gain tempo is ± 30 ppm/°C max. The device takes a wide range of voltages (from ± 11 to ± 18 V) on the ± 15 -V supply inputs. Five input ranges can be selected and three output codes are available.

Commercial/industrial version C-12 operates over the same full temperature range as does the military B-12. Both versions are provided in 32-pin hermetically sealed, metal DIPs.

Circle 359 on Inquiry Card

Semicustom CMOS IC Family Provides From 60 to 600 Gates

A single semicustom complementary MOS IC typically replaces 10 to 40 standard TTL or CMOS SSI/MSI circuits. The basic family includes seven chips ranging from the CDI 50 (a 60-gate array utilizing up to 28 I/O pins) to the CDI 600 (a 600-gate device, containing over 2500 transistors and up to 74 I/O pins). These devices operate at relatively low power, with a wide operating voltage range (up

to 18 V). The output has a sink current capability greater than 20 mA at 5 V and greater than 300 mA at 15 V.

Produced by California Devices Inc (1333 Lawrence Expy, Suite 340, Santa Clara, CA 95051), the semicustom circuits require no special drivers, clocks, or critical waveforms, nor is any ratioed or dynamic circuitry needed. Operation is specified over a -55 to 125 °C temperature range, with MIL Spec processing and testing, and radiation hardening up to one megarad available.

Circle 360 on Inquiry Card

IC Handles Data For Hard-Sector Floppy Disc Operation

Simplification of the data interface between a flexible disc and a microprocessor is provided by an MOS integrated circuit introduced by Standard Microsystems Corp, Hauppauge, NY 11787. The device is designated as the FDC3400 floppy disc hard sector data handler (HSDH). Used in low cost controller systems, it performs all the data handling required for hard-sectored floppy disc operation.

For a write operation, the data handler receives the processor's parallel data and shifts them out bit-serially to the disc data encoding circuitry. During a read operation, it receives a bit-serial data stream from the disc data separator, establishes byte synchronization by detecting the programmable sync byte, and transfers data on a byte by byte basis to the processor.

Additional features include single- or double-density operation (recording code independent), minifloppy or standard floppy compatibility, and dual disc operation—writing on one disc drive while simultaneously reading from another. Inputs and outputs are TTL compatible, and a 3-state output bus provides processor compatibility.

The device detects data overrun and underrun and indicates these conditions on its status lines. A data underrun causes write data to be written onto the disc from a special programmable fill register, until new data are entered into the write data buffer or until the write operation is ended. □

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PRODUCT FEATURE

A family of high speed array processors "designed to function as peripheral computational subsystems in real world signal processing applications" has been introduced by Analogic Corp. The AP400 family is said to provide exceptionally powerful array processing and fully programmable computing capability at low cost.

Unique architecture and a sophisticated standard software package provide the processor's user with many of the program design options of a general purpose minicomputer. The fully programmable unit handles programs written solely or in a combination of FORTRAN, host computer assembly language, and array processor assembly language.

As one benchmark of the processor's performance capability, a 1024-point fast Fourier transform (FFT) is carried out in 3.6 ms. A typical 1024-point complex FFT operation is executed in 7.4 ms.

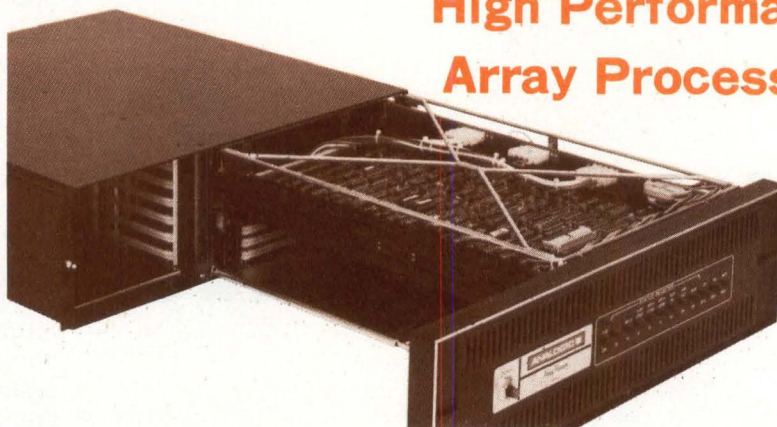
Data may be acquired either through a host interface or directly through a standard auxiliary input port. A multilevel interrupt structure and powerful executive provide realtime capability for applications requiring concurrent asynchronous data acquisition processing and output.

Hardware is available in three configurations: as a 4-card set for mounting directly within the host computer chassis; as a standalone unit in a rack mounting case, with integral power supply and space for additional memory and analog data acquisition cards; and assimilated with an AN5400 microprocessor controlled data acquisition system.

Design Features

A high speed microprocessor based multifunction command processor built into the array processor, in combination with dual pipeline architecture and innovative software, reduce hardware requirements, speed and simplify program generation, and permit efficient use of data memory. Most control, status, and data

Innovative Architectural and Software Techniques Result in Low Cost High Performance Array Processors



transfer between array processor and host computer is by direct memory access (DMA). Component count has been reduced drastically (from as many as 1000 ICs in other array processors to about 350 in this design).

A 3-stage arithmetic pipeline performs such functions as cross product, FFT butterfly step, and filter pole-pair step in response to machine language calls. Arithmetics and data memory are controlled by specifying three parameters: input data addresses, function to be performed, and output data addresses.

For full utilization of arithmetic logic, a buffered command and address pipeline parallels the arithmetic pipeline. Control signals for the adders, shifters, and multipliers in the arithmetic pipeline are created in, and transmitted along, this second pipeline as the pipeline arithmetic commands are decoded. Since control processor commands to the pipeline are buffer-stacked, the pipeline functions with very high efficiency.

Provision of two I/O ports permits direct input from high speed data acquisition front ends as well as direct output to peripherals. The control processor has its own operating system and is therefore largely autonomous. Most interaction with the host computer is by DMA only. The host is interrupted only on rare occasions such as when it instructs the array processor to begin a series

of computations or when the process ends.

Normally, array processor computations are carried out in block floating point format: 24-bit, 2's complement mantissa and 16-bit, 2's complement exponent. Such computations are performed at the rate of 10×10^6 arithmetic and logical operations/s. Data-dependent table lookup operations are performed at 1 MHz, while direct data input, via a standard auxiliary I/O port, may be made at up to 2.1 MHz.

Programs may be written at any of three different levels. At the highest, and easiest, level the user has a complete library of ANSI standard FORTRAN calls. These provide full access to the function repertoire with a minimum of user programming and a virtual disregard of the internal array processor operation.

At mid-level, host computer assembly language is available. The user sets up function control blocks stored in host memory for table-driven array processor operation. Sequences of functions may be chained together for fully independent concurrent operation of the host and array processor, with a minimum of host processor burden and a minimum of host memory taken up for array processor use.

Fine-level programming allows the user to exploit full resources of the array processor by employing the array processor's own assembly and

machine languages. A vertical architecture is employed, with registers, flags, the arithmetic pipeline, and all other internal structures available to the user via individual 1- or 4-word instructions ranging from simple 2-register operations to complex multi-operation pipeline arithmetic commands.

There are four distinct groups of standard software: system, for control of host and array processor activity; applications, for problem solution and realtime tasks; utility, for software preparation and use; and diagnostic, for hardware and software fault detection and isolation. The array processor is supplied with complete array processor and host resident systems software, applications software including an extensive library of FORTRAN and host callable functions, standard library of pipeline arithmetic commands in ROM, hardware diagnostics, and optional additional utility software and program debugging aids.

General Specifications

The 4-card array processor, ready to plug into a host processor, is available with edge connector patterns for most mainframes and minicomputers as well as many standard microcomputers. Power requirement with basic memory is 20 A nom at 5 Vdc. Standard memory is 4k words x 24 bits, expandable in 4k-word blocks to a maximum of 64k words/array processor; and standard program memory is 2k words, expandable to 4k (RAM or ROM).

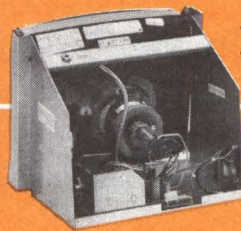
In standalone cabinet version the array processor measures 5.25 x 19 x 20" (13.3 x 48 x 50 cm). Power requirement is 130 W nom at 117 or 240 Vac, 50/60 Hz. Weight, with case, is 50 lb (22.7 kg). Operating temperature range is 0 to 50 °C.

Price and Delivery

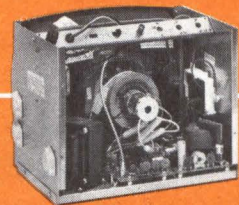
In the most economical configuration—the 4-card set with backplane and software—the AP400 array processor is priced at \$7500 each in 100 quantity. The standalone cabinet version in single quantity is \$12,500. Deliveries are scheduled to begin in the first quarter of this year. Analogic Corp, Audubon Rd, Wakefield, MA 01880. Tel: 617/246-0300.

For additional information circle 199 on inquiry card.

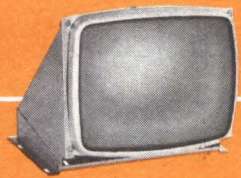
If you make top-quality data terminals, here are four reasons to use Setchell Carlson CRT data displays in your system.



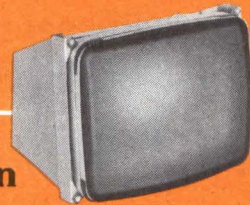
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Experience



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Our data displays are outstanding solid-state designs with critically matched magnetics to optimize the performance levels and dependability demanded by your customers. We use the most advanced engineering and production techniques to assure consistency of performance. No data display is built with more deliberate attention to quality and reliability.

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slight modifications. It would be less costly than starting from scratch. If you need a new, special package — we'll produce it for you, in the configuration you want, at minimal expense.

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Come to our Boston workshop and develop your skills in...

PASCAL is rapidly gaining acceptance in the computer world because of its:

- machine independence and
- accommodation of structured programming.

PASCAL is also the basis for DOD-1, the evolving standard Defense Department realtime language.

This unique workshop enables you to design and write PASCAL programs and evaluate high-level languages for your application. A fully-equipped laboratory will provide facilities to write and execute PASCAL programs during individual and group exercises.

George Poonen, Manager of Languages and Data Base Research at Digital Equipment Corp. will conduct the workshop.

WARNING:

Participants should expect to devote some evening hours to course preparation and group programming exercises.

Familiarity with mini or microcomputer architecture and experience with high-level language programming is assumed.

PASCAL FOR MINI AND

Program:

1. Introduction

- motivation behind the use of high-level languages
- overview of course

2. PASCAL

The goal of this part will be to introduce you to PASCAL through a series of case studies and examples. You will get an opportunity to write your own PASCAL programs and execute them. The emphasis throughout will be on:

- a. Mastery of the language, and
- b. Developing good programming style

A) PASCAL-I

- general form of PASCAL programs
- assignment statement
- basic I/O
- reading programs, syntax charts
- exercise 1

B) PASCAL-II

- constants, variables
- primitive data types
- precedence of operators
- lab (supervised sessions during which you will complete the given exercises)

C) PASCAL-III

- conditions
- loop structures
- selection
- exercise 2

D) PASCAL-IV

- introduction to procedures
- passing parameters by value and by reference
- functions
- nested procedures/functions and scope of names
- lab

PROGRAMMING

MICROCOMPUTERS / April 23-27, 1979

E) PASCAL-V

- general concepts of data types
- user-defined data types
- scalar data types
- arrays
- exercise 3

F) PASCAL-VI

- records
- sets
- pointers
- dynamic storage
- lab

G) PASCAL-VII

- sequential files
- text files
- formatting
- exercise 4
- list processing
- recursion
- advanced features — extensions
- survey of PASCAL implementation
- lab

3. High-level languages

Having learned one language, you will now be presented with a generic approach to programming languages. This approach will enable you to grasp the essential features of new languages in a matter of days.

- general approach to learning languages
- use of the above approach to learn PL/M and PL/Z
- additional features from other languages
- exercise 5

4. Compilers and optimization

A brief introduction to compiler design and organization to illustrate trade-offs in language design and use. This session's objective is to enable you to utilize high-level languages in the most effective way.

- design and organization of compilers
- what good compilers will do for you
- programming techniques to improve performance
- space/time trade-offs
- examples from LSI-11, INTEL 8080

5. Evaluation of languages

- checklist for languages
- when and when not to use high-level languages

6. Summary

- review
- new developments in languages and their use in small computers

In-house programs:

This workshop plus a variety of other customized technical and management courses are available for on-site presentation. Contact Donald French at (617) 964-1412 for details.

Tuition, schedule and continuing education credits

Tuition is \$600. This includes course notes and text, as well as Tuesday evening reception. The seminar is scheduled for 8:30 a.m. Monday, April 23, 1979, through 4:30 p.m. Friday, April 27, 1979.

Course certificate and 3 continuing education units will be offered by Polytechnic Institute of New York to participants completing the course.

Further information

For additional information on course content, objectives, and intended audience, you can call the course coordinator, Mr. Poonen, at 617/897-5111, ext. 3537. For administrative information, call the Institute for Advanced Professional Studies at 617/964-1412. Participants are urged to register early as enrollment is limited.

Additional courses:

16-BIT MICROCOMPUTERS: Design and Minicomputer Comparison — March 5 through 8, 1979, Boston.
 PROGRAMMING THE Z-80, 8080, and 8085 in Assembly Language — April 30 through May 4, 1979, Boston.
 MANAGING TECHNICAL PROGRAMS AND PROJECTS — May 14 through 16, 1979, Boston.

Course Registration Form

Please register me for the five-day course, PASCAL PROGRAMMING FOR MINI AND MICROCOMPUTERS co-sponsored by Polytechnic Institute of New York and Institute for Advanced Professional Studies to be held April 23-27 at the Ramada Inn, Woburn, Massachusetts 01801.

Sorry, I cannot attend — but please add my name to your mailing list.

Tuition is \$600. Make checks payable to Institute for Advanced Professional Studies. Please make room reservations early, directly with the hotel. Mention this conference to obtain special rates.

Name _____		Job title _____	
Employer _____		Business phone _____	
Business address _____			
City _____		State _____	Zip _____
Home address _____			

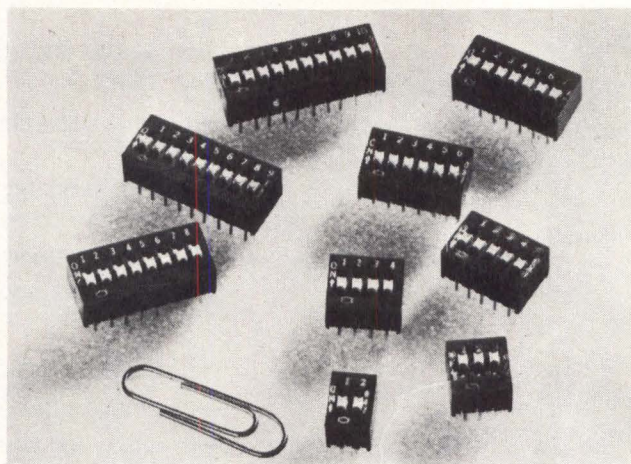
Return this segment to: Institute for Advanced Professional Studies
 Suite 306, One Gateway Center, Newton, MA 02158 Tel: (617) 964-1412

PRODUCTS

Slide Action DIP Switches Provide Nonslip Actuation, Easy Solder Flushout

Features of the SE2AV series spst switches are a concave button to insure self-centering and to prevent slippage during actuation, and drain holes for solvent flushout to eliminate contamination of contacts due to solder flux. Units have dust tight construction of slide operating mechanism and are available in 2- through 10-pole configurations. Also standard to the design are positive make and break; low contact bounce and resistance; visual position indicator; contact wipe $>0.005''$ (0.013 cm); high contact pressure of 50 g min; $0.3''$ (0.76-cm) profile; and gold plated contacts with flow soldering capability. Current carrying capacity is 100 mA max at 50 Vac; op temp range is 0 to 70 °C. Each circuit is rated at 10k mechanical operations min. **Cutler-Hammer, Inc, Aerospace Controls/Systems Div, 4201 N 27th St, Milwaukee, WI 53216.**

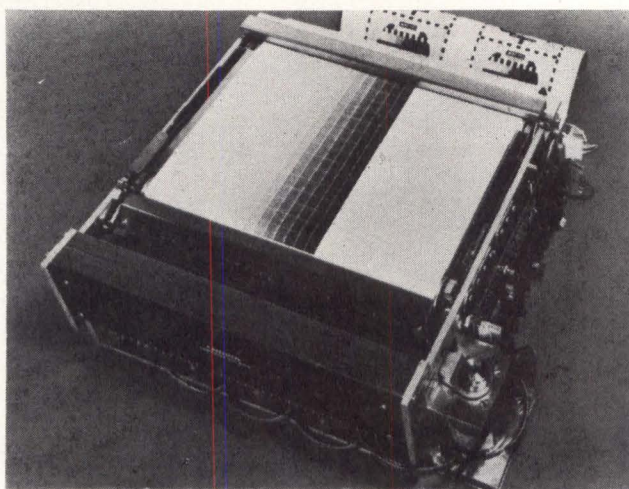
Circle 200 on Inquiry Card



Electrosensitive Digital Recording Device Prints Gray Scale Images and Alphanumerics

Archival gray scale imagery, line graphics, and alphanumeric printouts are produced on the CEC 912 gray scale printer using a dry electrosensitive recording process that requires no heating or toning. It prints 16 shades of gray scale with each step accurately defined by a 4-bit digital command. Horizontal and vertical resolution is 200 dots/in (79/cm). Specs include 2048 pixels/line, $0.005''$ (0.127-mm) pixel separation, and max picture width of $10.1''$ (25.6 cm). Data signals are input to the writing head assembly that consists of 128 electric styli; operation may be interrupted at any time. Max printout speed is 23.6 in/min (10 mm/s). Alphanumeric line printing may reach twice this speed, or 300 char lines/min in a 7 x 9 matrix for ASCII char. Rugged unit mounts in OEM equipment at any angle from horizontal to vertical for military and industrial applications and for mapping. **Bell & Howell, CEC Div, 360 Sierra Madre Villa, Pasadena, CA 91109.**

Circle 201 on Inquiry Card



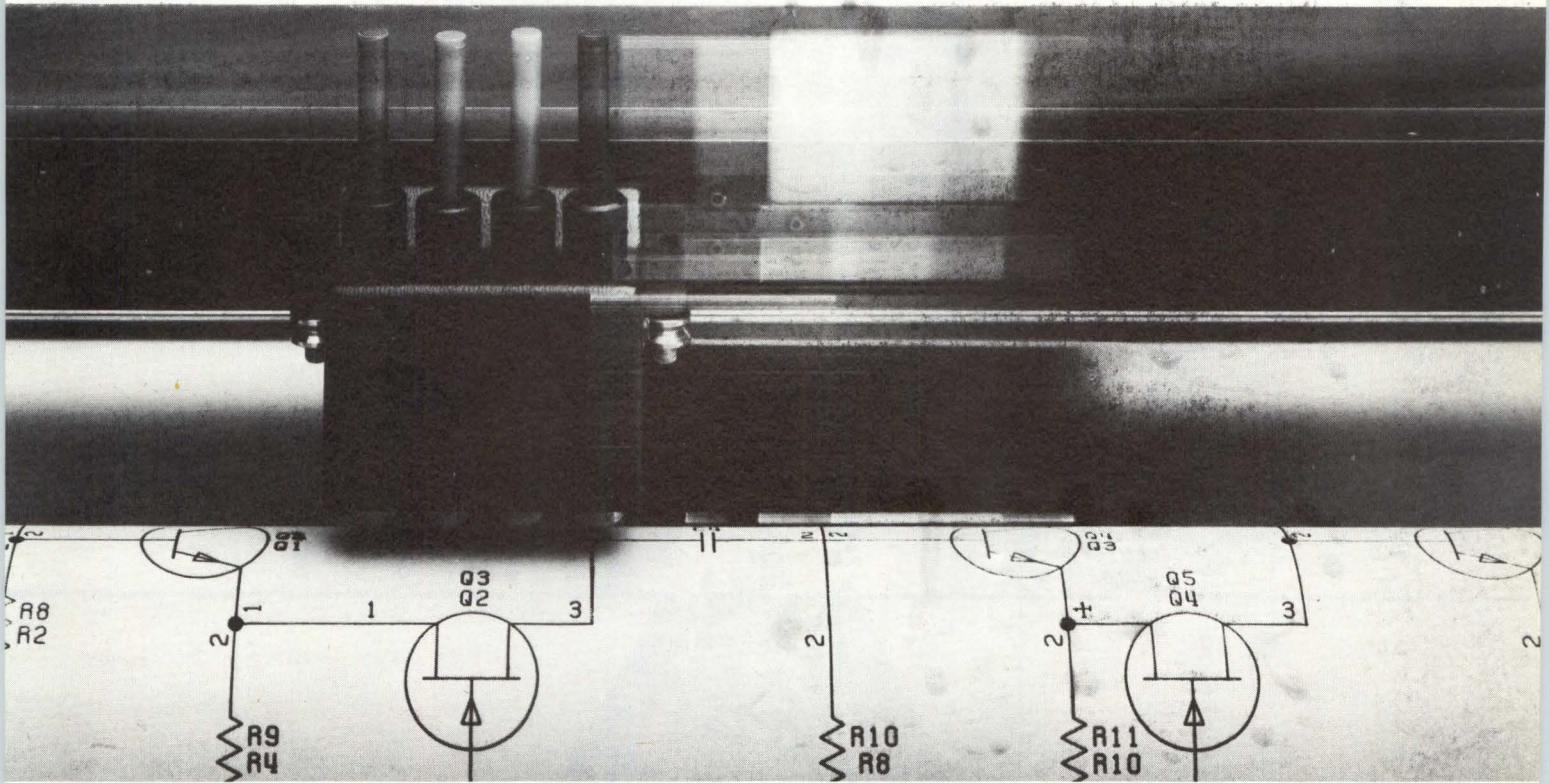
Computer Communicates Verbally Using Vocabulary Stored in Voice Response System



Plug and software compatible with DEC's PDP-8 and -11 computers, the BT-1 system uses compressed and prestored human speech for remote communications, laboratory and industrial automation, and software development systems. The computer can communicate messages, instructions, questions, answers, and alarms in natural human sentences or phrases—not computer synthesized—that transmit over telephone or rf links. Mag recordings of high quality speech are sampled at a 10-kHz rate with 6-bit resolution, resulting in 60k-bit/s digitized speech. These data are then compressed by a proprietary software method. Depending on the number of consonants in the word, the compression rate is as high as 5 to 1, minimizing bus time and storage requirements. Std vocabulary consists of numerics 0 to 9 and control words start, stop, and alarm; other vocabulary combinations are optional. **Perception Technology Corp, 95 Cross St, Winchester, MA 01890.**

Circle 202 on Inquiry Card

How to drum-up superior graphics in record time.



There's nothing to it.

Not when you start with the best. And that's exactly what the new CalComp 1055 high-performance drum plotter is – the best. In fact, it easily surpasses everything we – and our competitors – have created to date.

There's simply no other 36-inch, roll-fed drum plotter with specs like these. Plotting speed is an unprecedented 30 inches-per-second (762 mm-per-second) on axis. Complemented by a 4G acceleration ramp and 10MS pen-down time. The results are unbeatable quality and throughput.

What's more, you get the versatility that only four pens can provide and a practical, roll-fed design that keeps operator intervention to a minimum.

But that's not all. For increased accuracy, we made the 1055 completely d.c. servo-motor driven. And we gave it a special linear pen drive mechanism to help maintain consistently superior line quality. In every application.

The bottom line is this: Our new Model 1055 creates an entirely new set of standards

for all would-be, high-performance drum plotters. In terms of speed, accuracy and line quality. And in terms of good old-fashioned price/performance, too.

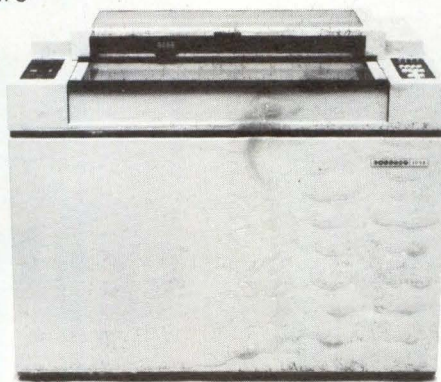
Of course, you may not need the sophistication of a 1055 right now. In that case, our new 1051 is the answer. You get 10-ips performance today, and the ability to field upgrade to a 1055 tomorrow – when your needs have expanded.

One thing hasn't changed, though.

CalComp service and support. It's still worldwide and second to none. For field service personnel. For in-place field systems analysts. And for the kind of help you expect from the world leader in digital plotters.

All of which proves, when it comes to high-performance drum plotters, CalComp's really drawing away from the competition. Again.

To arrange a special preview demonstration of the new 1055, please call your local CalComp sales representative in the following areas:



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2411 W. La Palma Avenue, Anaheim, California 92801

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CIRCLE 88 ON INQUIRY CARD

INTERFACE

79

↑ TO CHICAGO ↑

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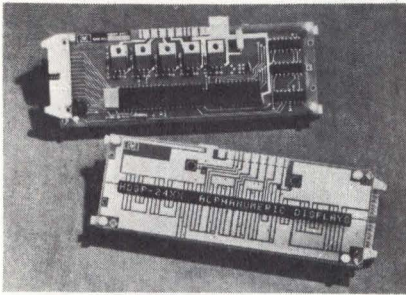
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PRODUCTS

STANDALONE DOT MATRIX DISPLAY SYSTEM



HDSP-24XX series couples dot matrix alphanumeric display with microprocessor based controller for easy-to-read 16-, 24-, 32-, or 40-char single line display. Controller incorporates preprogrammed routines to accept, decode, and display std ASCII data. 5.0-V operation plus std LSTTL compatible inputs and four separate display formatting modes allow for easy interface to keyboard or microprocessor based system. **Hewlett-Packard Co.**, 1507 Page Mill Rd, Palo Alto, CA 94304. Circle 203 on Inquiry Card

LAMPLESS PUSHBUTTON SWITCHES

Bright color indicators, with or without graphics, indicate changing functions mechanically in the series CA 110 switches that omit a lamp and socket assembly. Two methods of indication are legend and color change when the button is depressed, or legend remains the same but indicator color changes when the button is depressed. Indicators can be white, gray, black, yellow, green, orange, or metallic with white, gray, or black button shells. Tableau or stacked switches, 15 switches wide x 10 high/chassis, are available. **ITT Shadow, Inc.**, 8081 Wallace Rd, Eden Prairie, MN 55344.

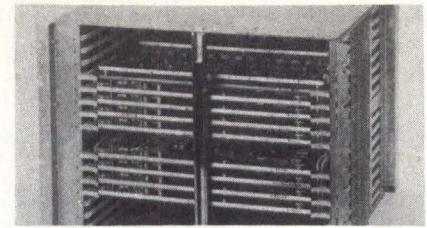
Circle 204 on Inquiry Card

OPTICALLY COUPLED INTERRUPTER MODULE

Featuring solid-state reliability and non-contact switching for applications requiring sensing of position or motion of an opaque object, CNY 36 consists of a high efficiency gallium arsenide LED coupled with a high gain silicon npn phototransistor across an air gap of 3 mm. It is encapsulated in a plastic package. Typ output current is 0.5 mA with an input of 20 mA; turn on/off time is 4.0 μ s. **Optron Inc.**, 1201 Tappan Cir, Carrollton, TX 75006.

Circle 205 on Inquiry Card

INTERDATA COMPATIBLE INTERFACE/MEMORY SYSTEM



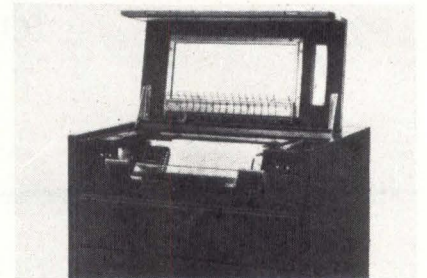
Memory bank interface (MBI), compatible with the Interdata local memory bank interface, has 16 slots for memory and assorted peripheral controller modules, of which 8 slots are reserved for memory. When populated with DR-717 64-bit core memory modules or other current Interdata core memory modules, max 512k-bit capacity is achieved. Parity and 750-ns operation are implemented by appropriate setting of on-board DIP switch. System comes in a 14" (35.6-cm) rack-mountable chassis. **Dataram Corp.**, Princeton-Hightstown Rd, Cranbury, NJ 08512. Circle 206 on Inquiry Card

SERIAL I/O MODULE

Each of the 8 RS-232-C asynchronous serial I/O ports on the 4.5 x 6.5" (11.4 x 16.5-cm) module supports all std baud rates from 150 to 9600. Baud rates are crystal controlled and individually switch selectable. Applications include data concentrators, key to disc systems, and communications switches. The module with 22/44-pin edge connector can be supplied with 2, 4, 6, or 8 ports. **Wintek Corp.**, 902 N 9th St, Lafayette, IN 47904.

Circle 207 on Inquiry Card

HORIZONTAL-MOVING FONT LINE PRINTER



Microprocessor-controlled Chaintrain[®] model 1260 prints at 600 lines/min and has motorized upper and lower tractor positioning. Carrier uses 8-char links riding on monorail track ensuring precise vertical alignment. Interchangeable links enable char set replacement. 64-char set is std with 48, 96, or 128 char optional. Print positions are 132 at 10/ in (3.9/cm). Printer has full line buffer, and will accept 6-part forms in sizes from 3.5 to 19.5" (8.9 to 49.5 cm). **Data Printer Corp.**, 99 Middlesex St, Malden, MA 02148.

Circle 208 on Inquiry Card

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CIRCLE 89 ON INQUIRY CARD

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DEC doesn't:

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Until you figure in the cost of converting all your media (to media that you can get from only a single source), and the cost of the new controller, new software and the entirely new support situation that you'll be facing.

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Supporting our customers with the right products, prices and deliveries has made us the largest independent supplier of DEC-compatible peripherals. Our product line presently includes add-in/add-on core and semiconductor memories, cartridge disc systems, floppy disc systems, mag tape systems, complete computer-based systems, and a wide variety of backplanes, expansion chassis and other accessories.

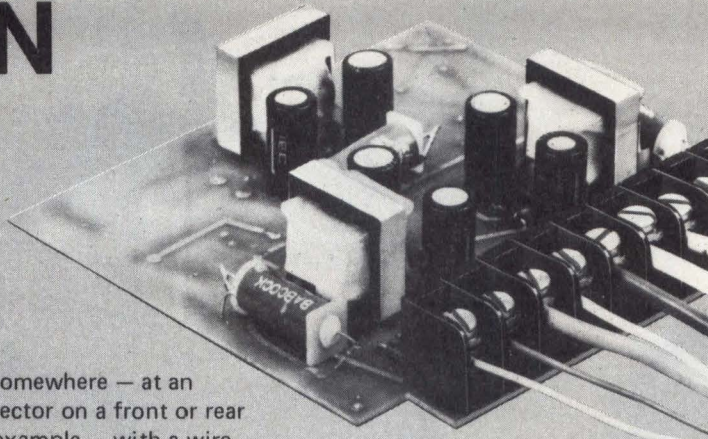
We're the only real alternative to DEC for all your miniperipherals, a complete single source. For all the details, please contact the nearest Plessey sales office today.



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GETTING THERE isn't HALF THE FUN



You start somewhere — at an input connector on a front or rear panel, for example — with a wire. Eventually, you arrive at a component somewhere on a PC board.

If your equipment is typical, you probably go through a half-dozen different connections in getting there. Solder eyes, terminal crimps, pins and sockets, terminal screws, etc., etc.

Every one costs money . . . eats away at profit. But that's not all. Every one is a *potential source of trouble*: unwanted resistance, leakage, crosstalk, breakdown; corroded, intermittent, or noisy connections. Every one can add to your debugging time, maintenance schedules, service calls. Any one could hurt your product's reputation.

BUCHANAN® RSB Single-Screw Barrier Blocks take your conductors *right to the board*, with no interruptions. They are engineered to give you a clean, solid, trouble-free, *permanent* connection. In flow-soldering, their stand-offs simplify flux cleanup. The "tri-barrier" design prevents shorts, isolates adjacent terminals, keeps screwdriver torque and pressure off the board. Ring or spade terminals cannot twist and short.

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Elk Grove Village, IL, (312) 437-8354; Manhasset, NY, (516) 627-8809;
Atlanta, GA, (404) 261-1224.

PRODUCTS

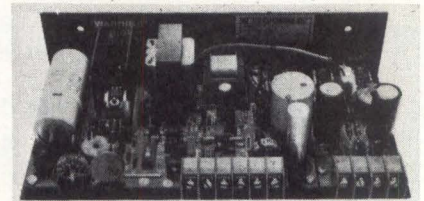
MINIFLOPPY DISC SYSTEM



The V80 system, which includes a minifloppy disc drive, power supply, regulator board, and case, increases usable storage capacity from 55k to 67.8k bytes on drive 1. Operating with a TRS-80 computer, the system also provides a faster drive, with a track-to-track access in 5 ms versus 40 ms for the computer's minidisc system. The self-contained unit is assembled and tested. **Vista Computer Co.**, 2909 Oregon Ct, Torrance, CA 90503.

Circle 209 on Inquiry Card

LINEAR REPLACEMENT SWITCHING POWER SUPPLIES



LR series 75-W single, triple, and quad output supplies have 115-Vac inputs and are regulated to 0.2%. Single output LR7500 models offer 5 V at 15 A, 12 V at 6.5 A, or 15 V at 5 A in a 4.87 x 2.1 x 7" (12.37 x 5.3 x 18-cm) package. Triple output LR7700 models contain 7500 series main output and two auxiliaries from 12 to 45 W each; LR7800 adds a fourth output of up to 12 W. **California DC**, 31117 Via Colinas, Bldg 402, Westlake Village, CA 91361.

Circle 210 on Inquiry Card

HIGH DENSITY LOGIC MODULES

The 760 modules contain from 8 to 10 functions/card. The series includes 8 kinds of logic gates, input interfacing cards with 10 functions/card, high density shift registers, and the ASCII transceiver module. The latter provides logic for a full-duplex asynchronous communication channel. It features automatic start and stop bit generation, and parity generation; and detects errors in framing, parity, and overrun. **Tenor Co, Inc.**, 17020 W Rogers Dr, New Berlin, WI 53151.

Circle 211 on Inquiry Card

OUR COMPETITIVE EDGE

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Mohawk Data Sciences is one of the leading suppliers of distributed data processing, key-to-disk and peripheral systems, with a customer base of over 7000 worldwide. Mark Stamp Steel has played a major role in the success of MDS products and their reputation for exceptional performance and reliability.

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I'd like to learn more about your products and services:

- Please send literature.
- Please send quotation (My specifications and requirements are attached).
- Please have a design specialist call.

Name _____ Title _____

Company _____

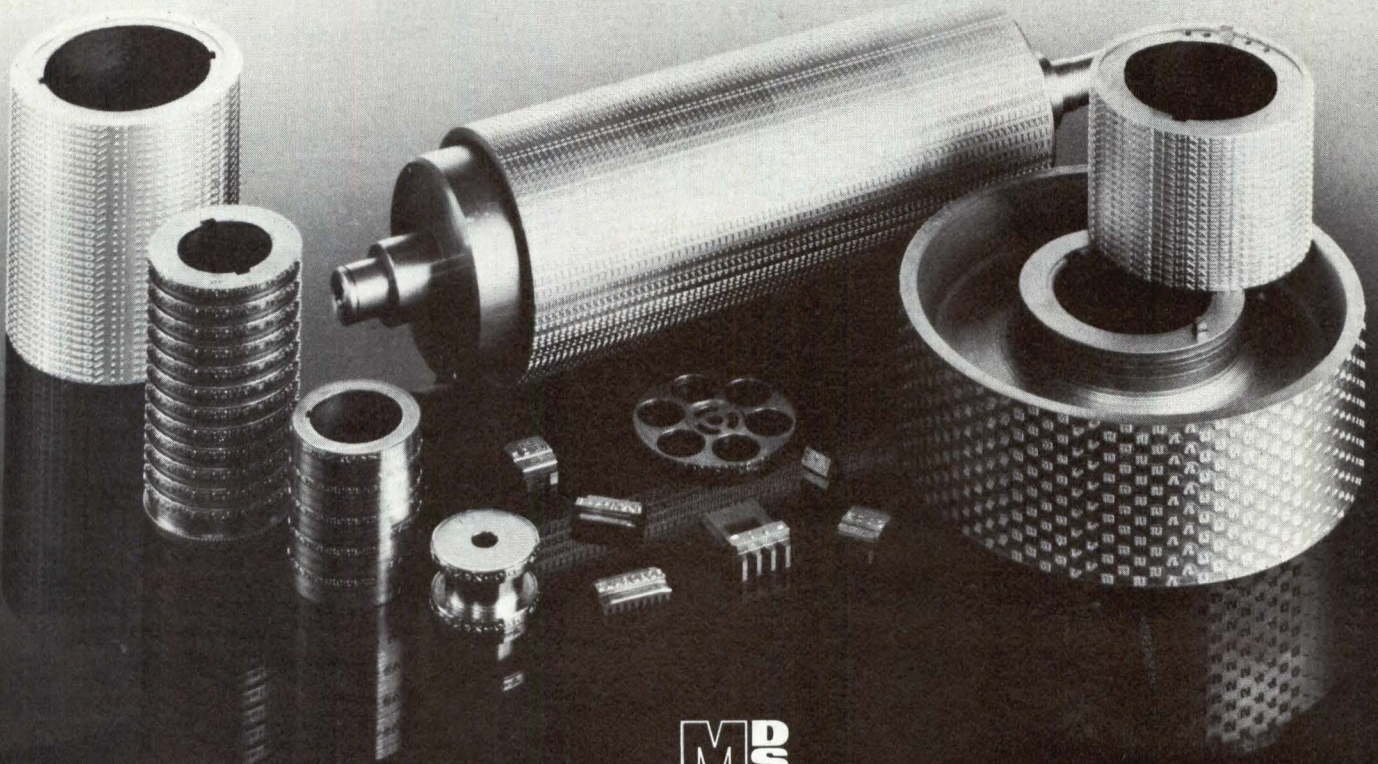
Street _____ City _____

State _____ Zip _____ Phone (____) _____

Mark Stamp Steel, a division of Mohawk Data Sciences Corp.,
Palisade Street, Herkimer, N.Y. 13350
Telephone: (315) 866-5300 (Ext. 5406).

CD 2-79

CIRCLE 92 ON INQUIRY CARD



MDS

Mohawk Data Sciences

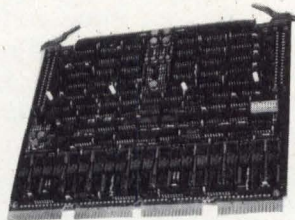
NOW AVAILABLE

LSI-11, SBC 80, 6800

16K CORE MEMORIES

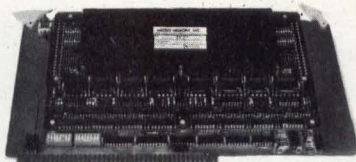
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- WRITE PROTECT.*
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MM - 1103/16



16K X 16

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16K X 8

MM - 1103/16

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MM - 8080/16

PLUGS DIRECTLY TO INTEL MDS 800 AND SBC 80/5, 10, 20 COMPUTER

MM - 6800/16

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* On models MM - 8080/16 and MM - 6800/16

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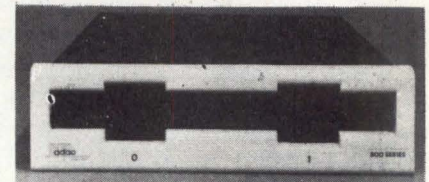
PRODUCTS

ZERO-SWITCHING SOLID-STATE RELAY

The 642 optically coupled ac relay features zero-crossover switching to minimize circuit noise. The model, packaged in a TO-116 DIP for convenient PC board insertion, uses hybrid micro-circuit techniques. It is rated to switch up to 1.5 A at 250 V rms, with peak transient ratings up to 600 V. **Teledyne Relays**, 12525 Daphne Ave, Hawthorne, CA 90250.

Circle 212 on Inquiry Card

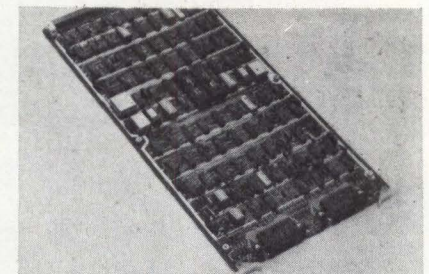
LSI-11 COMPATIBLE FLOPPY DISC SYSTEM



800 series, compatible with DEC LSI-11, LSI-11/2, and Adac System 1000 series, can be supplied with single- or dual-drive single density discs. 512k-bytes formatted storage is provided. Series is DEC RX01 software and media compatible. Controller hardware supports up to 4 drives. Formatting of diskettes can be in any standard IBM sector interleaving scheme. Self-testing micro-code and front panel indicators aid in error detection and correction. **Adac Corp**, 15 Cummings Pk, Woburn, MA 01801.

Circle 213 on Inquiry Card

DUAL PASLA FOR INTERDATA COMPUTERS



Dual programmable asynchronous single line adapter (PASLA) contains two PASLAs on a single 7 x 15" (18 x 38-cm) half-board. Each channel is compatible with Interdata operating system and diagnostic software and provides an interface between the Interdata multiplexer or selector channel I/O bus and any asynchronous data set or local terminal with an RS-232-C interface. **MDB Systems, Inc**, 1995 N Batavia St, Orange, CA 92665.

Circle 214 on Inquiry Card

The smart, reliable **TELERAY 1061:**



Highest Ever Features/Price* Ratio

*1090 list (desk stand optional)

NEW!

32 keyboard-

programmable functions

Call up forms, control sequences, etc...using up to 527 characters in any combination. PLUS these standard 1061 features:

- Independent I/O and peripheral speeds — *programmable*.
- Format and protect modes — dim, blink (or blank), underline and inverse video — *programmable* in any combination.
- *Programmable* tabs — up to 16 column positions.
- Monitor mode — 32 control codes displayable.
- Peripheral port, RS232C — *programmable* enable/disable.
- No-tools self-service in seconds, with snap-out, snap-in modules.
- Block mode transmission — page, part of page, line, part of line, and character by character.
- *Programmable* wide (40/line) or standard (80/line) character format with clear, readable 7x9 characters.
- Insert and delete — character or line at a time.
- Clear — page, to end of page, to end of line.
- SUPER SERVICE — replacement modules in reusable mailers ... it works!

And many more feature/benefits... hard to believe at the price.
Call your nearest TELERAY Sales Office for the complete, good-news story.

TELERAY Sales Offices:

(201) 652-7055, (201) 944-1600, (206) 641-6444, (212) 947-0379,
(213) 328-9770, (214) 661-0300, (216) 585-8421, (301) 589-2802,
(303) 279-7796, (312) 279-3290, (313) 354-6421, (405) 528-6071,
(408) 744-1930, (412) 243-8421, (416) 622-6752, (503) 292-3505,
(512) 451-5174, (512) 828-0937, (513) 223-8421, (518) 587-2313,
(602) 968-5962, (612) 535-5330, (613) 225-0411, (617) 459-2578,
(713) 780-2511, (714) 273-4771, (714) 552-7850, (716) 381-4120,
(801) 969-4034, (808) 523-1326.

TELERAY

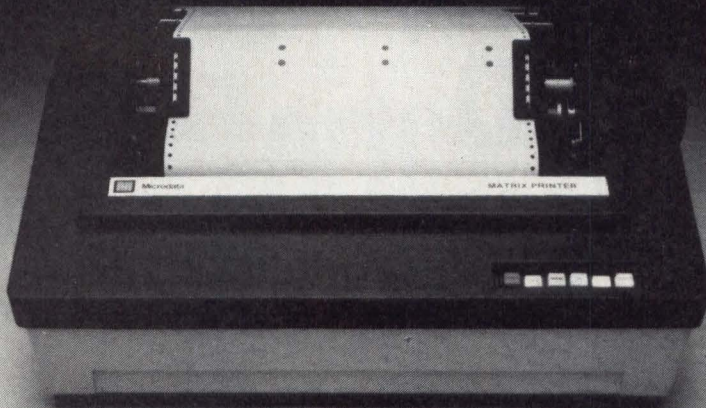
DIVISION OF



RESEARCH INC

BOX 24064 MINNEAPOLIS, MINNESOTA USA 55424
PHONE (612) 941-3300

**THIS IS
THE ONLY DECENT
LOW COST 165 CPS
MATRIX PRINTER
YOU CAN GET
IN VOLUME
RIGHT NOW.**



Other people make them, of course. But you can't get them in volume. Unless you're willing to wait a very long time. And in this business a printer you can't get is about as useful as all those wonderful products that haven't been invented yet.

Even if you did have a wide variety to choose from, you'd probably choose our Matrix printer anyway. Microprocessor control makes it efficient, fast and reliable. And it's programmable from your computer or optional keyboard.

Bidirectional printing and paper feed gives you true graphics capabilities. Special character sets, including foreign language alphabets, provide incredible flexibility. And when you add the optional keyboard, it becomes a remote communications terminal.

Matrix is compatible with all industry standard RS-232-C or parallel interfaces, so you can plug it in just about anywhere.

If you need a good matrix printer in volume and you can't wait forever, contact one of our local sales offices or the Director of OEM Sales, Microdata Corporation,
17481 Red Hill Avenue, P.O. Box
19501, Irvine, CA 92713.
Telephone: 714/540-6730.
TWX: 910-595-1764.

SALES OFFICES

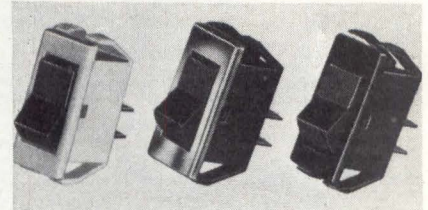
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Chicago 312/364-5820
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Microdata OEM Products
A significant difference.

Circle 95 for information only

PRODUCTS

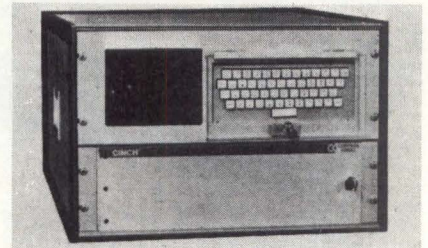
**SINGLE-POLE
ROCKER SWITCHES**



Single-pole rocker and paddle switches are UL listed and CSA certified. They are available with 3 separate ratings of 10, 12, and 16 A. Snap-in type panel mounting eases installation. Various color combinations, circuits, metal bezels, illuminated versions, hot stamping, and custom colors are available. Terminals are 0.25" (0.64-cm) slip-on type and can also be soldered. **Chicago Switch, Inc.**, 1714 N Damen Ave, Chicago, IL 60647.

Circle 215 on Inquiry Card

**INTELLIGENT DATA ACQUISITION
AND CONTROL SYSTEMS**



Cinch™ series Z80 based systems for industrial applications include 16 A-D channels, 16k EPROM (12k system BASIC, 4k user programmable), 4k RAM, and 2 serial ports, either 20 mA or RS-232-C. Options include additional memory, A-D and D-A channels, hardware, floating point processor, optically isolated high voltage I/Os, IEEE bus interface, keyboard CRT terminal, and P/ROM programmer. Programming is done in BASIC, enhanced with a real-time operating system and I/O subroutines. **Control Logic, Inc.**, 9 Tech Cir, Natick, MA 01760.

Circle 216 on Inquiry Card

**SPEED ENHANCEMENT FOR
MATRIX PRINTER**

RS-232-C and parallel interface compatible matrix printer now prints up to 165 char/s. Unit is controlled from a CPU or via an optional keyboard. Features include bidirectional printing and paper feed with optional char sets, including foreign language alphabets. **Microdata Corp.**, 17481 Red Hill Ave, Irvine, CA 92714.

Circle 217 on Inquiry Card

Our second product is another first.

We started CONVER because we felt it was time someone started applying imaginative thinking and high technology to power supplies; making them more responsive to your needs.

We did it with our first product: the industry's first 27-watt switcher at the price of linears.

And we've done it again with our second product:

The industry's first truly simple, modular, multi-output power supply.

Our CONVER 6000 Series is a sophisticated multi-output power supply utilizing a state-of-the-art packaging approach. And there's a second source to guarantee availability.

The CONVER 6000 Series offers advanced performance features, such as digital remote margin control, remote on/off and sequencing, faulty channel LED indicator, and signals for out of tolerance, input power failure, and current limit.

The CONVER 6000 Series offers more reliable performance, because of its modular p.c. board construction and conservative design. That means a longer operating life, with fewer repairs.

And if you ever need to make a repair, it'll take less time to do it—and less money, too—because you won't need a whole new unit—just a field-replaceable module.

Speaking of less money, that's another advantage the CONVER 6000 Series offers you—cost savings, because of its p.c. board construction and standardized modules.

It's available with three independent outputs, two at 600 watts and one at 350 watts. Total power is 1300 watts. Total size is 8" x 8" x 13½" UL listed. And it's guaranteed for six years.

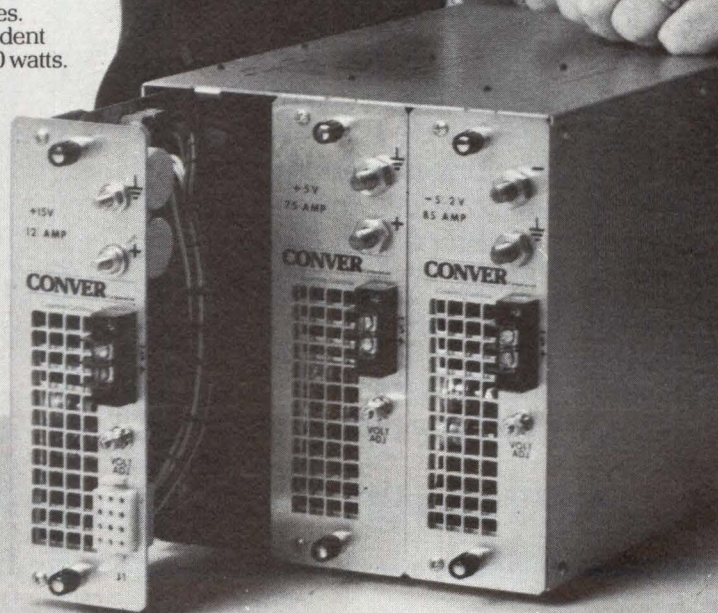
And it's available right now.

Just contact us at 10631

Bandle Drive, Cupertino, CA 95014.
Phone (408) 255-0151.

The CONVER 6000 Series Multi-Output Power Supply. More proof that we're going to change the way you think about power supply suppliers. Maybe you should think about changing to us.

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Director of Engineering
CONVER Corporation
WESTINGHOUSE
'67-'74 Switching Power
Supply Designer
KAISER ELECTRONICS
'74-'78 Manager, Switching
Power Supply Development

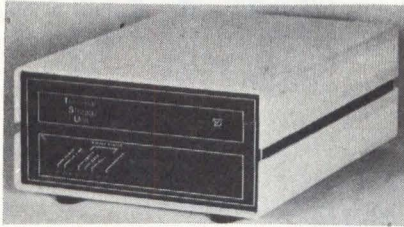


CONVER

CIRCLE 96 ON INQUIRY CARD

PRODUCTS

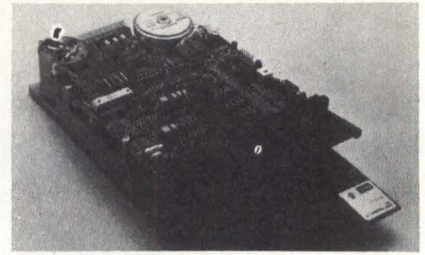
TERMINAL STORAGE UNITS



Variable top of form, programmable answerback, and editing capability for store and forward data communications applications are supplied in the TSU series. These capabilities are handled by TextEdit II software stored in P/ROM. Containing communications ability, the TSU-0 and -1 are single PC boards designed to replace an RS-232 interface on model 43 Teletype[®] printers. Models 4, 8, and 12, containing 4k, 8k, or 12k char of storage respectively, operate with any ASCII terminal having an RS-232 interface. **Tri-Data Corp.**, 505 E Middlefield Rd, Mountain View, CA 94043.

Circle 218 on Inquiry Card

5.25" FLOPPY DISC DRIVE

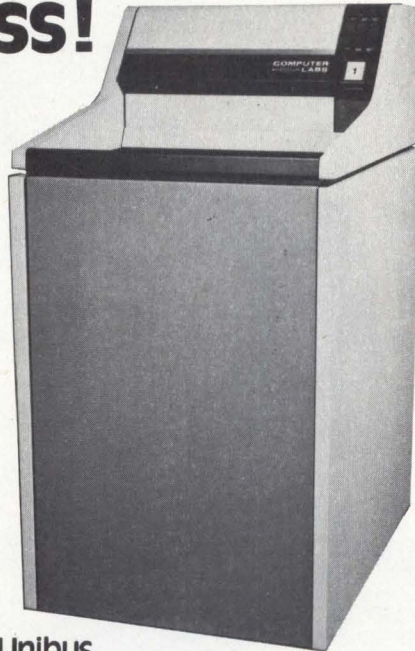


Said to use two-thirds less power than competitive models, 6106 has 40-track capacity and 12-ms track-to-track access time. It can operate in both FM and MFM recording modes and provides up to 250k-bytes unformatted capacity on one side of the disc. Non-frictional ball race is used for head positioning. Systems-oriented options include software-controlled door interlock, head-loaded activity LED, and head-load control that is separate from the select control. **Computer Products Dept., BASF Systems**, Crosby Dr, Bedford, MA 01730.

Circle 219 on Inquiry Card

176 MBytes of PDP-11 disk storage for \$1000's less!

You can have up to 176 MBytes of formatted storage in an all-new moving-head disk memory system from Computer Labs. The M7000 uses a single floor-standing drive which plugs into your DEC PDP-11 Mini-Computer without any hardware or software alterations. It looks just like a DEC RJP-05 or RJP-06 to the Unibus.



This system is completely compatible with DEC disk-pack media and software such as RT-11, RSX-11, RSTS, MUMPS, etc....but it costs thousands of dollars less. In fact, add-on drives for this system cost about 50% of the DEC equivalents.

Computer Labs also offers PDP-11 users a selection of disk memory systems equivalent to the RK-05 with storage capacities through 20 MBytes, and tape memory systems compatible to TM-11. Call or write now for all the details.

COMPUTER LABS

COMPUTER LABS, INCORPORATED

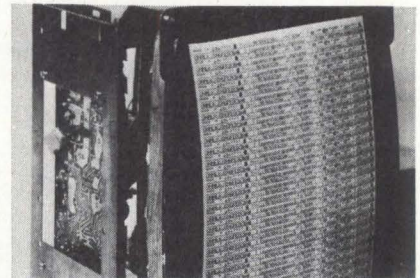
505 EDWARDIA DR. • GREENSBORO, N.C. 27409 • 919/292-6427 • TWX 510-922-7954

BISYNCHRONOUS COMMUNICATIONS CONTROLLER

Bisynchronous Intelligent Cable enables any Naked Mini computer to communicate with any terminal or device that uses industry std BSC protocol. The controller provides serial-to-parallel and parallel-to-serial conversion, manages a microprogrammed block check, controls the operation of the unit's multicharacter receive and transmit buffers, and features automatic character insert/delete capability. **Computer Automation Inc.**, 18651 Von Karman, Irvine, CA 92713.

Circle 220 on Inquiry Card

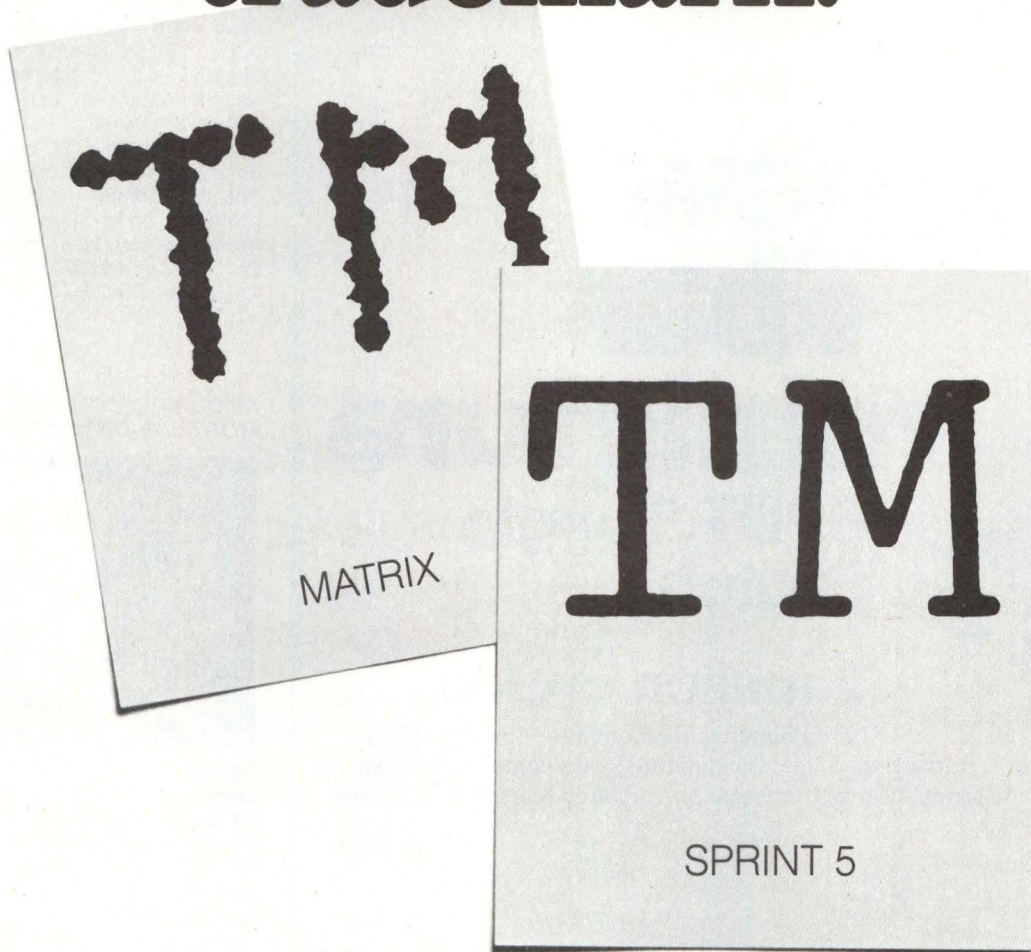
HIGH DENSITY, HIGH RESOLUTION CRT MONITOR



Noninterlaced VR-800 raster scan monitor has a horizontal scan rate of 50 kHz and a video bandwidth of 65 MHz. The full page CRT displays 800 visible scan lines and refreshes at 60 cycles/s. The display holds 66 lines of 7 x 9 char on black and white high speed phosphors. It is intended for use in word processing, graphics, and other high density, high resolution applications. **Moniterm Corp.**, Box 262, Long Lake, MN 55356.

Circle 221 on Inquiry Card

Quality print is Sprint 5's trademark.



For all those times when you wish your computer could print letter quality, you need a Sprint 5 Daisywheel Terminal from Qume.

Its fully-formed characters are always clear, distinct, eminently readable. (Even after they've been enlarged 1000%.)

Perfect for executive reports, financial statements, and any other application where neatness counts.

But the Sprint

5 does more than give you outstanding print quality. Much more.

Thanks to our dynamic positioning feature, it easily plots, creates

graphs, and justifies text. With switch selectable 10 or 12 character per inch spacing.

What's more, Sprint 5 comes with a wide selection of MultiColor™ ribbons including red/black. And over 60 different typefaces.

The Sprint 5 Daisywheel Terminal and RO Printer from Qume.

When it comes to dots versus daisies, our advantages are easy to see.

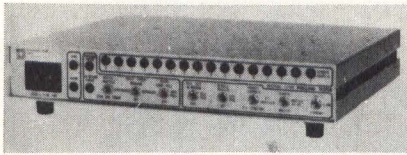
Qume[®]
the printed word



For more information, contact your nearest data terminal dealer or Qume, 2323 Industrial Parkway West, Hayward, California 94545.

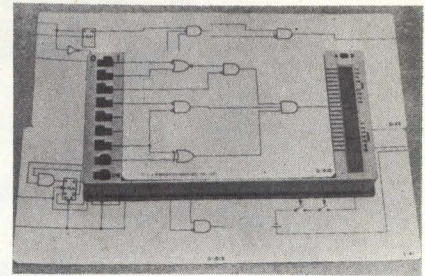
PRODUCTS

MODEM POLLING PERFORMANCE TESTER



Model 1700, a microprocessor based unit for testing polling performance of synchronous and asynchronous modems, can be used over either actual or simulated switched, private line point-to-point, or private line multidrop networks. It performs polling tests of on-line data communications equipment for fault isolation and system performance verification. Unit distinguishes between outbound and inbound polling message errors. Message errors can be deliberately introduced to verify network continuity. **International Data Sciences, Inc.**, 7 Wellington Rd, Lincoln, RI 02865. Circle 222 on Inquiry Card

LOGIC STUDENT TRAINING DEVICE



Self-Pace Logic Trainer™ model 100 trains students for digital electronic related assignments, by using physical logic state manipulation and visual display. It includes all gates, positive and negative edge triggered devices, master/slave clocking, and preset and clear functions. Switch circuit and Venn diagram problems as well as BCD and binary counting modes are supplied. The unit contains a manual, 40 digital problems, and a 9-V battery. **L. J. Broder Enterprises Inc.**, 3192 Darvany Dr, Dallas, TX 75220. Circle 223 on Inquiry Card

A new T-bar® miniature 6PDT Toggle Switch

Full Size.



2 million cycles
for computers, minicomputer and main frame forming, data communications equipment, medical, industrial instrumentation, and stop-start test switching

T-BAR Series 202 6PDT Mini-Paddle Lever Switches are designed for "must operate" applications. T-BAR Edge-to-Dome™ bifurcated contacts provide the SitStill™ reliability that protects the integrity and stability of millions of circuits during continuous use or even long periods of inoperation. The 202 retains its initial characteristics through 2-million operations. Call for application help.

T-bar INCORPORATED

SWITCHING COMPONENTS DIVISION

141 Danbury Road Wilton, CT 06897 Telephone: 203/762-8351 TWX: 710/479-3215

ACOUSTIC COUPLER FOR MODEL 43 DATA TERMINAL



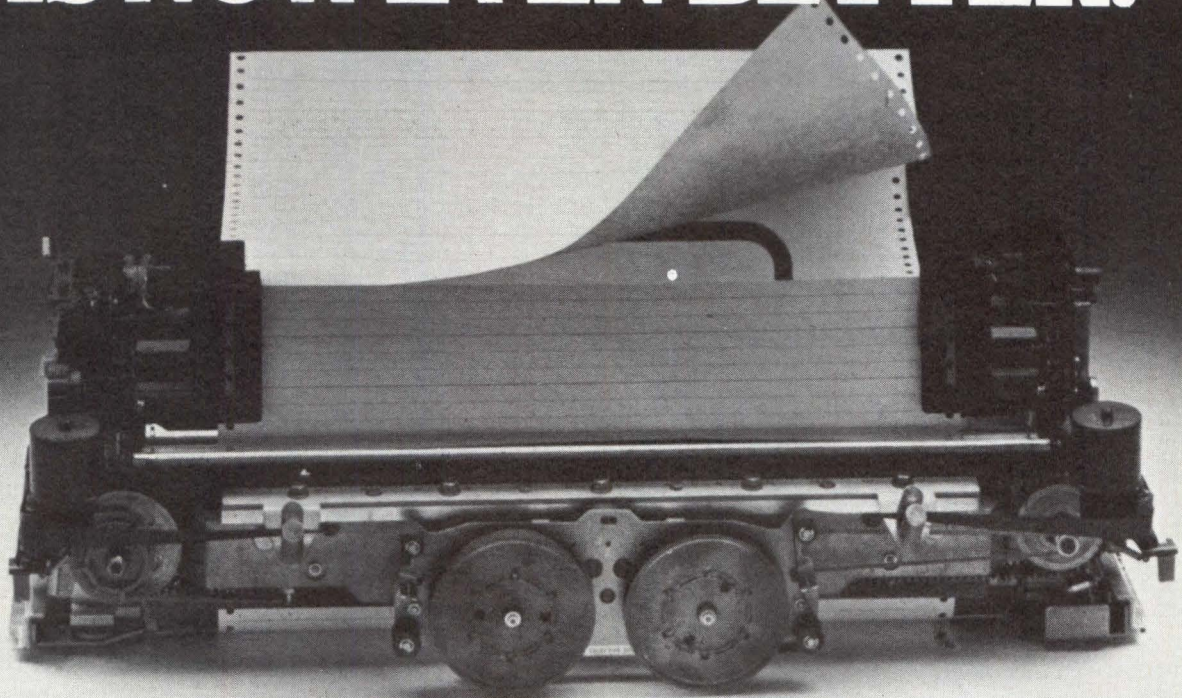
Designed to operate with Teletype Corp's model 43 data terminal, acoustic telephone coupler handles data at a rate of 0 to 450 baud, combines acoustic and hardware line coupling, and high sensitivity. The coupler interfaces to TTL of the terminal, eliminating the need for an EIA interface. **Om-nitec Data**, 2405 S 20th St, Phoenix, AZ 85034.

Circle 224 on Inquiry Card

CUSTOM-PROGRAMMED LOGIC CONTROLLER

Prepackaged solid-state model SK-1500 replaces individually wired control relay systems, and is said to eliminate 90% of the wiring time and space required for conventional systems. It can be used to actuate sequential steps in functions of such automated systems as machine tools, packaging equipment, and metal stamping production lines. Use of 100% CMOS ICs plus integral circuitry for input noise rejection eliminates noise. **Entertron Industries**, Elliott Sta Box 15, Buffalo, NY 14203. Circle 225 on Inquiry Card

THE BEST 300 LPM PRINTER ON THE MARKET IS NOW EVEN BETTER.



In order to build up a customer base of more than 40,000 units in three years, you have to have a superior printer. And no matter how you look at it, the Teletype* model 40 printer has a lot going for it.

Look at cost. Nowhere does anyone offer as much in a 300 LPM printer for as little as the model 40 costs. At the OEM price of under \$2000, it even compares favorably against low-speed printer costs.

Look at reliability. The model 40's unique design utilizes a minimum of moving parts for a maximum of on-line time. Plus proven LSI (Large Scale Integration) circuitry handles many functions formerly performed mechanically. This reduces hardware requirements and increases printer life.

Look at features. The unit is completely operational to give you everything necessary to go on-line. You also get 32 switch-selectable no-cost options to choose from, easily changeable character sets, and self-diagnostics.

Finally, look at product support. Not only do we offer nationwide service, we'll maintain your printer for as little as \$23 per month—and that includes labor and material.

With all that going for the model 40, how could we make it even better? Two ways.

First, we gave it a new, simplified OEM interface. Simply command the motor on, watch for the next character command, and send data.

Next, ribbon life has been significantly extended with our new re-inker mechanism that's available as a low-cost option.

No wonder we're getting a reputation as the OEM printer people.



THE OEM PRINTER PEOPLE

*Teletype is a trademark and service mark of the Teletype Corporation.

CIRCLE 100 ON INQUIRY CARD

PRODUCTS

PROGRAMMABLE ARRAY LOGIC DESIGN SYSTEM



Standalone system for designing, documenting, and programming PAL ICs translates Boolean equations directly into PAL fuse patterns, displays the resulting pattern on the terminal, and, upon command, blows the fuses in a new PAL device according to the pattern. CYMPL-1™ also reads the pattern from a previously programmed PAL and programs new devices accordingly, without the use of equations. Benchtop 47 x 14 x 48-cm cabinet unit offers two verification modes. **Cybernetic Programming Systems, Inc.**, 175 Jefferson Dr, Menlo Park, CA 94025.

Circle 226 on Inquiry Card

WIDE INPUT RANGE SWITCHING POWER SUPPLIES

Without jumpers, switches, or taps, the 15- to 75-W switching power supplies operate from 90 to 250 Vac. Brownout protection is offered since usable operation may be extended to any input voltage as low as 50 Vac. A single-transistor, single-transformer flyback design is used. Single, dual, and triple outputs are available in either open frame designs or rfi resistant enclosed packages. **Converter Concepts, Inc.**, 435 S Main St, Pardeeville, WI 53954. Circle 227 on Inquiry Card

DESK AND CPU CABINET

Workstation is available with 24 x 48 or 32 x 60" (61 x 122 or 81 x 152-cm) black laminant desk top and 23 x 26 x 23.5 or 23 x 26 x 32" (58 x 66 x 59.7 or 58 x 66 x 81-cm) simulated walnut grain finish cabinet with black laminant toe-kick. Cabinet has transparent bronze plexiglass door with chrome hardware and magnetic lock, removable back panel, RETMA std 19" (48-cm) rack, and optional adjustable shelves. **Group Two**, 4901 Morena Blvd, Suite 305, San Diego, CA 92117.

Circle 228 on Inquiry Card

RUGGEDIZED GRAPHIC DISPLAY SYSTEMS

Program compatibility between commercial and ruggedized hardware is achieved by microprogrammable graphics generators models 8295/8395. Both feature modular hardware to accommodate configurations depending on data load, data update, graphics complexity, and multiterminal needs. 8295 provides up to 12k of MOS RAM refresh memory and interfaces to Harris Slash 4, 5, and 6, Modcomp II, and SEL 32/55. Ruggedized 8395 features 16k mag core refresh memory, with internal memory save. **Aydin Controls**, 414 Commerce Dr, Fort Washington, PA 19034.

Circle 229 on Inquiry Card

MULTIPROCESSING DUAL PORT MEMORY SUBSYSTEM

Intel Multibus™ and National Semiconductor compatible RM-117 random access subsystem has virtual memory to support up to 1M bytes of storage and provides 2 logically independent paths to a common memory. 20-bit wide internal memory address can be generated from the Multibus or through virtual memory. 350-ns internal memory cycle time gives effective 700-ns speed if both ports are being accessed simultaneously. Basic board consists of dual Multibus interfaces, contention resolution, dynamic address translation and protection, and 16k bytes of memory. **Datacube SMK Inc.**, 670 Main St, Reading, MA 01867.

Circle 230 on Inquiry Card

Model 1200... The Heavyweight King of the ChainTrain® Printer Family.

The top of the line in DPC's patented family of ChainTrain line printers is the Model 1200. Its heavy-duty construction and rugged dependability, coupled with its blazing 1200 LPM speed, make it the prime choice for computer room applications where there is a continual flow of work on a wide variety of forms.

So, if you've got a heavy workload, the completely microprocessor controlled ChainTrain 1200 has the muscle to pull you through. For an impressive list of specs, including information about our free, 30-day, in-house trial, get in touch with us today. We'll tell you more about our Heavyweight Champ than Howard Cosell ever knew about Muhammad Ali.



DATA PRINTER CORP
99 Middlesex Street, Malden, MA 02148
Tel: (617) 321-2400 TWX: 710-348-0794
Regional Sales Offices: Clifton, NJ, Costa Mesa, CA

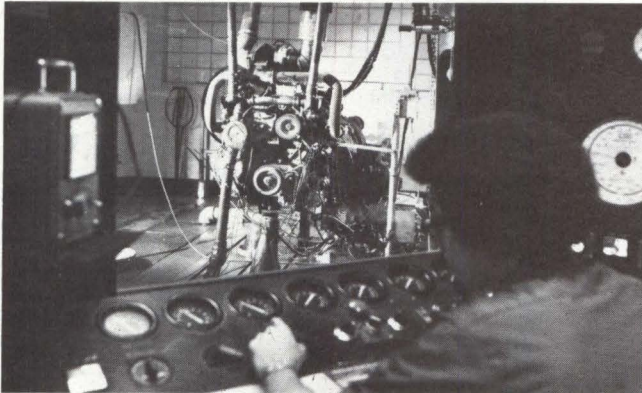




**"BEFORE WE COULD BUILD THE WORLD'S LARGEST INDUSTRIAL DATA ACQUISITION SYSTEM, WE NEEDED NETWORK AND SYSTEMS CAPABILITIES WE COULD DEPEND ON."
"ONLY MODCOMP HAD THEM."**

Jim Springer, Director of Data Systems,
AVCO Electronics, Huntsville, Ala.

Jim Springer is building what will be the largest industrial data acquisition system in the world. This system will be used on development and testing by one of the world's largest producers of diesel engines.



To implement the system, Jim chose MODCOMP's Classic[®] Computers, the MAX IV operating and communications system, and the MAXNET IV network extension.

"Network software capability is the key."

"The MAXNET IV network extension integrates all 120 computers in the system. This provides us with the performance characteristics of a stand-alone system, and the economic advantages of network resource sharing.

"In a real-time environment, that's essential."

"MODCOMP gives us the high speed and performance we need — at a cost we can afford."

"The MAX IV operating system is ideal for this type of real-time multi-programming because it provides 256 K-bytes of directly addressable memory. And with the Classic's extremely fast floating-point processor, we have more than enough speed.

"This is essentially the same system we specified for testing NASA's Space Shuttle. Ordinarily, that kind of superior quality and reliability would be out of reach for industry.

Sales offices: Atlanta, GA • Boston, MA • Chicago, IL • Cincinnati, OH • Dallas, TX • Denver, CO • Detroit, MI • Hartford, CT • Houston, TX • Los Angeles, CA • Clark, NJ • Orlando, FL • Pittsburgh, PA • San Jose, CA • Washington, DC

But because of their experience with the NASA system, only MODCOMP could meet the assigned high performance levels at a cost industry can afford."

"MODCOMP's tougher on their equipment than we are."

"Our customer was concerned about equipment reliability in their plant. And with good reason. The temperature can get as high as 120 degrees. But we've seen the Classic perform in worse places. MODCOMP's 'hot room' test facility, for instance. That's 132 degrees."

"Obviously we have a lot of faith in MODCOMP."

"We're just in the first phase of this system. But we have to know that, say, 3 years from now, the hardware will be available and that the software can be implemented or interchanged as needed.

"We recommend MODCOMP because we have a lot of faith in them. In their company, their equipment and their service.

"We know they can deliver. It's as simple as that."

At MODCOMP, we specialize in building real time computer systems and the network software capability to make them work.

Easily. Reliably. Affordably. And with the kind of performance you'd expect to find in the world's largest industrial data acquisition system.

If that's what you're looking for from a computer system supplier, do what Jim Springer did. Call MODCOMP.

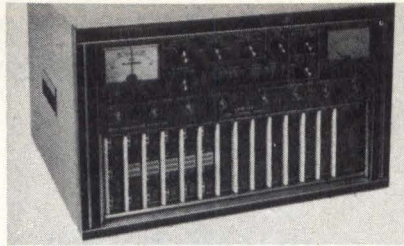
MODCOMP
Dedicated to your success

Modular Computer Systems, Inc.
1650 McNab Road, Ft. Lauderdale, FL 33309
(305) 974-1380

PRODUCTS

SPEECH PLUS MULTIPLEX TERMINALS

SPMT-7 series permits simultaneous transmission and reception of single audio channel plus a number of telegraph or data channels over a normal voice-grade telephone or radio circuit. Terminals are designed around frequency-programmable frequency shift transceiver. For alternate voice/data or data plus, delay equalized filters are



available to permit 4800/9600-bit/s data communication simultaneously with low speed TTY. **Coherent Communications Systems Corp**, 85D Hoffman Lane S, Central Islip, NY 11722. Circle 231 on Inquiry Card

PROGRAMMABLE FREQUENCY SYNTHESIZER SUBSYSTEM

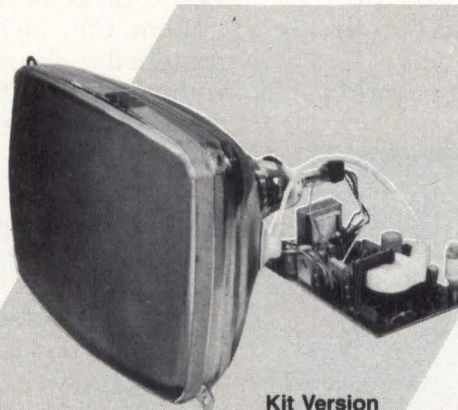
Model 5620A, designed as a direct build-in for OEM applications where required controls are normally provided by the host system, is a direct synthesizer with no phase-locked loops. Switching time is 20 μ s max. Spurious harmonic output is better than 35 dB below fundamental; close-in phase noise is 70 dB min below fundamental. Intended for use with 5- or 10-MHz external frequency standard, unit provides choice of 0.1-, 1-, 10-, 100-, 1k-, or 100k-Hz frequency resolution. Resolution is constant over 160-MHz operating range. **Rockland Systems Corp**, Rockleigh Industrial Pk, Rockleigh, NJ 07647.

Circle 233 on Inquiry Card

CIQ Series

9" and 12" CRT DISPLAY MONITORS with a Horizontal Rate of 15.72 KHz

Compatible with
TV120 or TV90
Priced Below the
Competition
Built-in Quality,
Performance,
Dependability



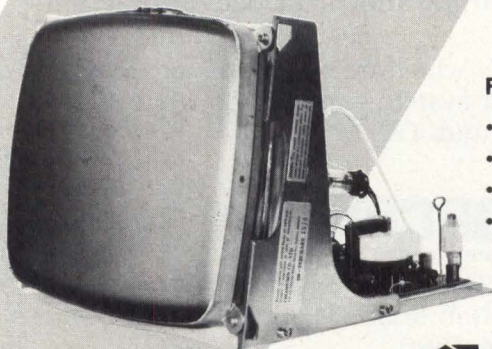
Kit Version

The low-cost CIQ-9 and CIQ-12 CRT Display Monitors with a horizontal rate of 15.72 KHz provide data equipment manufacturers with sharp, highly reliable image presentation.

Separate horizontal drive, vertical drive, and video signal inputs mean elimination of composite sync and video signal processing and simple output circuitry.

The completely new design of the compact integrated PCB utilizes the latest semiconductor and other components, providing a dependable performance level never before possible.

Delivered with P4 phosphor as standard. Available options are P31 and P39 phosphors, sturdy zinc chromate plated chassis and a power supply module which is compatible with practically any power supply standard in the world.



Chassis Version

FEATURES

- Uniform High Resolution
- Integrated PC Board
- Dependable Construction
- Squareness of Picture

C. ITOH ELECTRONICS, INC.

5301 Beethoven Street Los Angeles, Calif. 90066
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Telephone: (212) 682-0420 Telex (WU) 12-5059

DATA GENERATOR SYNCHRONIZING UNIT

Allowing parallel operation of very high frequency data generators and achieving up to 16 parallel data patterns at a 400M-bit/s data rate, SYN-400 synchronizer operates 2 to 4 DG-400YH data generators in parallel. The synchronizer/data generator system operates from 100 to 400M bits/s from an external clock source. It provides clock distribution to the data generators, and controls individual data generator reset and clock signals to achieve synchronous operation. **Tau-Tron, Inc**, 11 Esquire Rd, North Billerica, MA 01862.

Circle 234 on Inquiry Card

SUBMINIATURE LED PANEL LAMPS

Series 30 super-bright LEDs fit in 0.190" (4.826-mm) mounting holes and feature wirewrap terminals. Red, amber, and green lamp colors have respective luminous intensities of 50, 32, and 25 mcd at a drive current of 20 mA. Available with either regular or low profile Fresnel lenses, as well as clear or diffused std LED encapsulation, subminiature lamps are available with built-in resistors. **Data Display Products**, 303 N Oak St, Inglewood, CA 90301.

Circle 235 on Inquiry Card

VIDEO COMPUTER TERMINAL

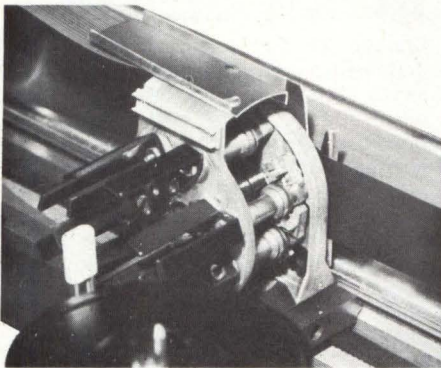
VT-4800 CRT terminal has IBM Selectric keyboard, 19 P-ROM programmable keys, 4k bytes of RAM and more than 11k-h MTBF. Other features include cursor addressing by keyboard or software, char read at cursor position (on 8-bit bus), scroll up and down through data (up to 16k bytes), page increment and decrement, and selectable baud rates from 110 to 9600. Addition of graphics board upgrades unit to vector graphics terminal. **SLM, Inc**, 2366 Walsh Ave, Santa Clara, CA 95050.

Circle 236 on Inquiry Card

Florida Data has the printer for the next 5 years

Are you worried about system throughput growing faster than your printer capability? Then talk to Florida Data Corporation about the printer for the next five years!

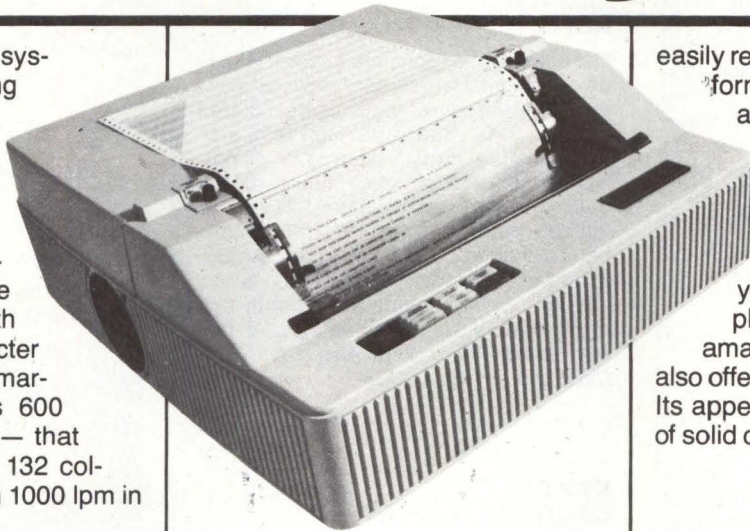
FDC's Model PB-600A can keep the pace with total system growth — it is the fastest character matrix printer on the market. Its print speed is 600 characters per second — that means 230 lpm at full 132 column width or more than 1000 lpm in shorter lines.



Print-heads for FDC printers are manufactured in-house with proprietary technology.

The secret of the PB-600A's outstanding performance is the proprietary print-head technology developed by FDC. We manufacture our own print heads. Print head life exceeds any other character matrix printer; FDC heads are warranted for one full year.

Our head technology was a long time coming — the engineers who developed it brought a total of more



Model PB-600A is the fastest character matrix printer on the market.

than 200 years' combined experience to the task. But it was worth waiting for. Now you can enjoy line printer output at serial printer prices, with the added benefits of exceptional reliability and outstanding customer support.

The PB-600A has all the other features you'd expect in a high-quality printer designed especially for OEM customers.

There are no duty cycle or page density restrictions on the print head; this means continuous printing, hour after hour. Standard PB-600A features include microprocessor controller, forward/reverse printing, an 894-character buffer, internal test capability and switch selection of four different type fonts. A two-channel paper tape reader provides vertical forms control. Paper tractors may be

easily repositioned to accommodate forms from 3" to 14 $\frac{7}{8}$ " in width, and a long-life ribbon provides 20 million characters before replacement.

Florida Data also offers the Model BNY, a new binary printer that brings you computer graphics and plotting capability at an amazingly low price. This printer also offers a two-pass character font. Its appearance is very close to that of solid character printing.



Volume production capability means economy, reliability for OEM customers.

Enjoy the economy and reliability that come from high-volume output. Enjoy the OEM customer support that comes from a dedicated, experienced technical staff.

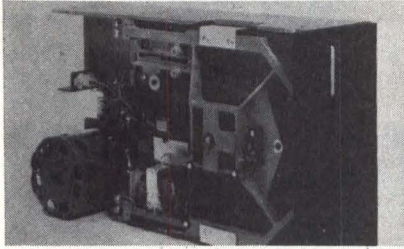
Get the details from:
Florida Data Corporation,
3308 New Haven Avenue,
West Melbourne, FL.
Telephone 305/724-6088.

Distributor inquiries invited.

FDC

PRODUCTS

DUAL-HEAD HIGH SPEED DISKETTE DRIVE



Compatible with single sided IBM 33FD and 2-sided 43FD drives, the RFD 4000 will store up to 1.6M bytes of unformatted data or 1M byte in IBM 128-byte sector format. Access time is 3 ms track to track with a 91-ms average seek time. One of the two ceramic read/write heads is fixed to the head carriage; the second is mounted on a movable head load arm attached to the carriage. **Ex-Cell-O Corp, Remex Div**, 17533 Alton St, Irvine, CA 92713. Circle 237 on Inquiry Card

DATA LINK FOR PLASTIC FIBER OPTIC CABLE

Separately packaged 3712T transmitter (TTL in/light out) and 3712R receiver (light in/TTL out) when used with fiber optic cable comprise a simplex data link providing 20k-bit operation. Receiver requires ± 15 Vdc at ± 20 mA, with 5-nW optical power input; transmitter needs 5 Vdc, 60 mA max, and launches 3.5 μ W of optical power into 40-mil 0.53 numerical aperture fiber. Units, housed in 41 x 77 x 16-mm metal packages operate with 10^{-9} bit error rate and 28.5-dB cable and connector loss. **Burr-Brown Research Corp**, International Airport Research Pk, Tucson, AZ 85734.

Circle 238 on Inquiry Card

LCD CONNECTOR

S420U series connectors clip onto std DIL LCDs, eliminating the need for epoxy or frames. Available for glass thicknesses of 0.036 to 0.062" (0.09 to 0.157 cm), the connectors are supplied with any number of contacts up to 40 on 0.1" (0.25-cm) centers. Tin plated brass alloy contacts are integral with their corresponding pins and cast into the connector body. Each contact terminates in the company's Cone Point[®]. **Teledyne Kinetics**, 410 S Cedros Ave, Solana Beach, CA 92075. Circle 239 on Inquiry Card

InGaAsP DOUBLE HETEROJUNCTION LEDs

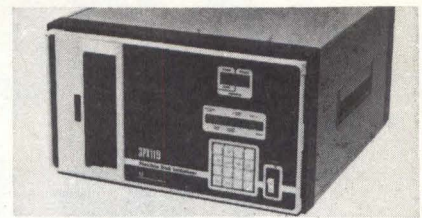
For fiber optic communications, these developmental quaternary devices allow the emission wavelength to be tailored between 1.05 and 1.35 μ m, to match the optimum transmission and dispersion properties of silica fibers at the optimum wavelengths near 1.27 μ m. A lattice matched InGaAsP/InP double heterojunction structure is used. Optical power output of the LED is 0.5 mW min with a modulation bandwidth of 50 MHz. **Varian Associates/LSE Div**, 611 Hansen Way, Palo Alto, CA 94303. Circle 240 on Inquiry Card

HYBRID SOLID-STATE RELAY

Capacities of 5, 10, 25, and 40 A comprise the 7800 series having a reed relay input and triac output. Life expectancy is 100M operations. Logic compatible units feature random switching, internal RC snubber, and diode clamped input. Electrical characteristics include an ac switching voltage range of 24 to 140, 24 to 280, and 24 to 280 V rms, 47 to 63 Hz. Op temp range is -30 to 80 °C and storage temp is -40 to 100 °C. **Hamlin, Inc**, Lake and Grove Sts, Lake Mills, WI 53551.

Circle 241 on Inquiry Card

FLEXIBLE DISC INITIALIZER



This self-contained, microprocessor controlled system offers fully automatic formatting of any single-sided 8" (20-cm) flexible mag disc. It is designed for disc initialization to any IBM compatible soft-sector format. The stand-alone or rackmount system is preprogrammed for 128-, 256-, and 512-byte sector formats, with other formats available. In operation, all 77 disc tracks are automatically formatted in <45 s with appropriate sector ID and data fields; the index track is recorded; and the entire disc format is verified. **Three Phoenix Co**, 10632 N 21st Ave, Phoenix, AZ 85029.

Circle 242 on Inquiry Card

CRT TERMINAL WITH 32 ADDED FUNCTIONS



Storage of up to 32 operator programmed or downloaded function messages, totaling up to 527 char, has been added to the model 1061. All functions (forms, control sequences, answerbacks, or any ASCII message) may be entered and called up by a simple escape sequence; 8 common functions may be initiated with dedicated keys on the keyboard. Another added feature is programmable secure fields (blank field modifier in lieu of blink). **Research Inc, Teleray Div**, PO Box 24064, Minneapolis, MN 55424. Circle 243 on Inquiry Card

10-ELEMENT LED DISPLAY

RBG-1000 offers ten 0.15 x 0.04" (3.81 x 1.02 mm) diodes arranged on 0.1" (2.54 mm) centers in a 20-pin, 300-mil (7.62-mm) DIP. Elements are individually addressable at both anode and cathode. Available in std red and additional colors, luminous intensity with all segments lighted is 2.8 mcd, typ. Power dissipation at 25 °C is 500 mW. Forward currents and voltages, respectively, are 20 mA and 2.5 V max (1.65 typ). **Li-tronix**, 19000 Homestead Rd, Cupertino, CA 95014.

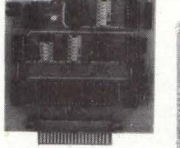
Circle 244 on Inquiry Card

For a happy ending,

See page 81

TRS-80^{E.S.} SERIAL I/O

● RS-232 compatible ● Can be used with or without the expansion bus ● On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line. Board only \$19.95 Part No. 8010, with parts \$59.95 Part No. 8010A, assembled \$79.95 Part No. 8010C. No connectors provided, see below.

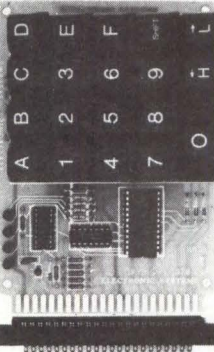


EIA/RS-232 connector Part No. DB25P \$6.00, with 9' 8 conductor cable \$10.95 Part No. DB25PS.

3' ribbon cable with attached connectors to fit TRS-80 and our serial board \$19.95 Part No. 3CAB40.

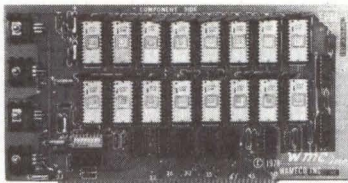
HEX ENCODED^{E.S.} KEYBOARD

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only \$15.00 Part No. HEX-3, with parts \$49.95 Part No. HEX-3A. 44 pin edge connector \$4.00 Part No. 44P.



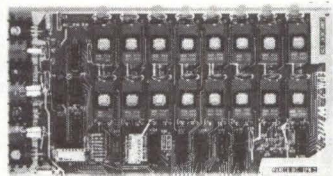
4K EPROM^{E.S.} WMC^{inc.}

This board is designed to operate with any speed or power 1702A. Addressable in 4K byte increments and can be configured to occupy either 2K or 4K segments. It can be populated one memory chip at a time. Bare board \$30, board with parts \$200, assembled \$230. Part No. EPM-1



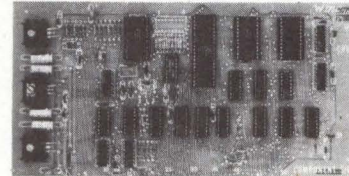
16K OR 32K EPROM^{E.S.} WMC^{inc.}

Designed to operate with any speed or power 2708 or single voltage (+5V) 2716. Addressable in 4K increments and can occupy multiples of 4K. It can be populated one memory chip at a time. Has bank addressing and Phantom Disable. The board comes with an exclusive software program that can be placed in a 2708 or 2716 that will, when used in conjunction with a RAM memory board, check out every line on the EPM-2. Bare board \$30, board with parts with 2708 \$455, assembled \$485. Board with parts with 2716 \$1,225, assembled \$1,255. Part No. EPM-2



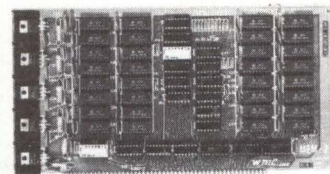
8080A CPU^{E.S.} (With Eight Level Victor Interrupt Capability) WMC^{inc.}

Uses the 8080A and the 8224 clock chip. The crystal frequency used is 18 MHz and the vector interrupt chip is the 8214. The board will function normally without the interrupt circuitry. When the interrupt circuitry is built up, the board will respond to eight levels of interrupts. Designed to be a plug-in replacement for the IMSAI CPU board and will work in other computers with the appropriate modifications made to the ribbon cable connector pin out from the front panel. The board will work in systems without a front panel if the system has a PROM board that simulates the functions of the front panel. Bare board \$30, with parts \$185, assembled \$220. Part No. CPU-1



16K STATIC RAM^{E.S.} WMC^{inc.}

Operates with any speed or power 2114. All input and output lines are fully buffered. Addressable in 4K byte increments. If the system has a front panel, the board will allow itself to be protected. If there is no front panel, the board will not allow itself to be protected. The board has Bank Address capability, Phantom Disable, MWRITE, and selectable wait states. Bare board \$30, board with parts \$665. Part No. MEM2



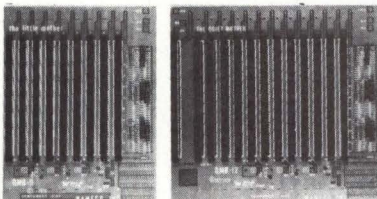
S-100 BUS ACTIVE TERMINATOR *

Board only \$14.95 Part No. 900, with parts \$24.95 Part No. 900A



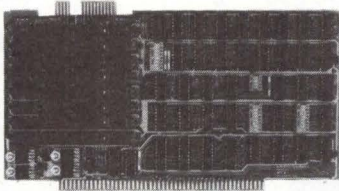
9 AND 13 SLOT^{E.S.} MOTHER BOARDS WMC^{inc.}

All traces are reflow solder covered and both sides are solder masked. The connectors used on these boards are the IMSAI™ type (.125" between pins, .250" between rows). Spacing between connectors is .750". All lines, except power and ground, have a passive RC network termination available. There is a kluge area available that will accept two 40 pin sockets and one 36 pin socket. The circuitry for supplying three separate regulated voltages to the kluge area is contained on the board. Part No. GMB-12 \$40 bare, \$105 kit, \$120 assembled. Part No. GMB-9 \$35 bare, \$90 kit, \$105 assembled.



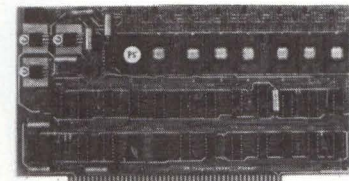
PIICEON 65K DYNAMIC RAM

Main memory for microcomputers, intelligent terminals, business systems, medical systems, and OEM systems. ● High density random access memory 48K bytes or 64K bytes ● Fully buffered ● S-100 bus compatible ● Low power (dynamic memory) ● Transparent refresh ● Digital delay line techniques for reliable operation ● Multiple boards allowed using hardware or software controlled bank select ● "Phantom" signal for RAM/ROM overlap ● All boards are fully tested prior to shipment. Operating System test and extensive bit pattern testing. ● Works directly in 8080A processors or Z-80 environment at 2MHz ● Currently used by industry ● 1 year warranty. Only available assembled and tested with 48K \$1,250 Part No. 48K, or with 65K \$1,475 Part No. 65K



8K EPROM^{E.S.} PIICEON

Saves programs on PROM permanently (until erased via UV light) up to 8K bytes. Programs may be directly run from the program saver such as fixed routines or assemblers. ● S-100 bus compatible ● Room for 8K bytes of EPROM non-volatile memory (2708's). ● On-board PROM programming ● Address relocation of each 4K or memory to any 4K boundary within 64K ● Power on jump and reset jump option for "turnkey" systems and computers without a front panel ● Program saver software available ● Solder mask both sides ● Full silkscreen for easy assembly. Program saver software in 1 2708 EPROM \$25. Bare board \$35 including custom coil, board with parts but no EPROMS \$139, with 4 EPROMS \$179, with 8 EPROMS \$219.



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ELECTRONIC SYSTEMS

Dept. CD, P.O. Box 21638, San Jose, CA, USA 95151

PRODUCTS

CRT TERMINAL WITH EXPANDED DISKETTE STORAGE



Automatic dynamic file allocation capability maximizes diskette storage capacity on Microterm II intelligent desktop CRT workstation. Storage space is assigned only as needed by system software. Terminal's 1.2M-byte file capacity packs multiple records into single sector, and supports indexed sequential, sequential, and direct access methods. File directory information for up to 11 files at one time may be retained in RAM, allowing any file or record to be retrieved in a single access. **Digi-Log Systems, Inc.**, Babylon Rd, Horsham, PA 19044.

Circle 245 on Inquiry Card

PLUG-IN MODULE TO CONVERT TYPEWRITER TO TERMINAL

Model 5061 telecommunications module permits an IBM model 50 or 60 electronic typewriter to operate as an ASCII computer terminal for use with microprocessors, CRTs, and other peripherals. The module installs inside the typewriter. It provides an RS-232 interface that operates at either 110 or 150 baud. The converted typewriter has Selectric quality printout, with added features not usually found in computer terminals. **Transaction Data Systems, Inc.**, 7015 Marcelle St, Paramount, CA 90723.

Circle 246 on Inquiry Card

WAVE SOLDERABLE SLIDE SWITCHES

The SL series of 6 types of enclosed detented and momentary/spring-return switches with low to medium current capacity contain no rivets, staking operations, or adhesives. Phosphor bronze and silver plated stationary contacts provide positive positioning and rigidity. Buttons, housing, and stators are fire retardant molded thermoplastic. Bifurcated, double wipe sliding contacts straddle both sides of the stationary contacts. **Standard Grigsby**, 920 Rathbone Ave, Aurora, IL 60507.

Circle 248 on Inquiry Card

0.5" MAG TAPE CONTROLLER

MTC-80, a single-board 6.75 x 12" (17.15 x 30.5-cm) formatter/controller, features IBM R/W compatibility for both NRZI and phase-encoded formats; 7 or 9 tracks at densities of 200, 556, 800, or 1600 bits/in (79, 219, 315, or 630/cm). Tape speeds of 25 and 37.5" (64 and 95 cm)/s are currently supported. It is compatible with Intel MDS and SBC-80 microcomputer boards, Multi-bus™, and National Semiconductor BLC series. **Zeta Research, Div of Nicolet Instrument Corp.**, 2300 Stanwell Dr, Concord, CA 94520.

Circle 247 on Inquiry Card

RECEIVE-ONLY TELEPRINTER

Available as a receive-only terminal or optioned with a keyboard, Datacom 1200 uses bidirectional printing capabilities at a max print speed of 180 char/s on line lengths of up to 132 char. It has a 7 x 7 dot matrix. Reducing printout time, the receive-only teleprinter serves as a hardcopy output device and peripheral printer. With the keyboard, it functions as an input device, for text retrieval, inquiry/response, and software program development. **The Computer Communications Group**, 12th Floor, 160 Elgin St, Ottawa, Ontario K1G 3J4, Canada.

Circle 249 on Inquiry Card

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PRODUCTS

HIGH SPEED LINE PRINTERS

Horizontal font printing mechanism on the 3300 series of commercial level medium to high speed printers can print up to 1500 lines/min. A double hinged print mechanism yoke assembly and a monorail print font guidance mechanism provide accurate print alignment. Character sets can be customized by individually removable slugs. Model 3300R is available for severe environments, the 3300N is both ruggedized and reduced in size, and the 3300T is "Tempest" qualified for secure applications. Print speeds are 600 lines/min with a 128-char set, 900 lines/min with 96 char, 1200 lines/min with 64 char, and 1500 lines/min with 48 char. 64-char ASCII and EBCDIC sets are std. Units have 5 speeds for forms advance, and 2 speeds each for backspacing of forms, moving forms right or left, and lateral tension adjustment. **Hetra**, 1151 S Eddie Allen Rd, Melbourne, FL 32901. Circle 250 on Inquiry Card

IEEE-488 DATA COUPLERS

Microprocessor based interface devices enable older, non-compatible instruments to be used in IEEE-488 bus based systems. A model 4885 controller can control the bus system through any RS-232 serial command source. It accepts high

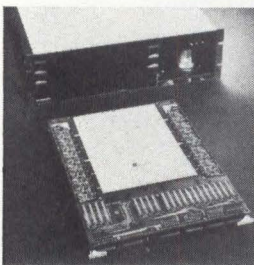


level commands and generates the signals and character codes needed to send commands through the bus. Data from devices connected to the bus are transmitted

back to the controlling source over the RS-232 data path. Model 4881 talker, 4882 listener, and 4883 talker/listener transmit data into or from the bus and allow a systems engineer or a programmer to connect existing instruments to the bus. The model 4884 coupler is a talker/listener interface for RC-232 compatible devices, to connect all RS-232 computer peripherals to the IEEE-488 std bus. **ICS Electronics Corp**, 1450 Koll Cir, Suite 105, San Jose, CA 95112.

Circle 251 on Inquiry Card

650-ns, 32k-WORD CORE MEMORY

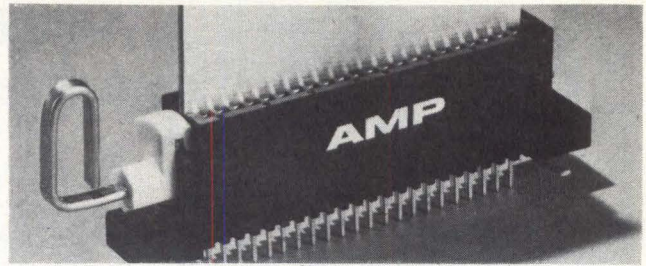


Store/3220, a 32k x 20-bit-word nonvolatile core memory intended for applications where data integrity and speed are primary concerns, is a self-sufficient planar unit fabricated on a single 11.75 x 15.4 x 1.0" (29.8 x 39.1 x 2.5-cm) card. Up to four cards can be linked in one chassis to give a maximum storage capacity of 128k 20-bit or 64k 40-bit words.

The memory is plug compatible with the Micro-memory-3000 interface. Worst-case power requirements are 5 V at 3.9 A, 15 V at 6.25 A, and -15 V at 0.55 A. Operating temperature range is 0 to 50 °C; an optional extended temperature model operates from 0 to 70 °C. Boards may be housed in an optional 19 x 22.4 x 5.25" (48.3 x 56.9 x 13.3-cm) chassis with a self-contained power supply. A self-test card option is also available. **Dataproductions Corp**, 6219 DeSoto Ave, Woodland Hills, CA 91364.

Circle 252 on Inquiry Card

SEQUENTIAL ZERO INSERTION FORCE CONNECTOR



A contact timing mechanism on this ZIF edgeboard connector ensures that signal, power, and ground circuits make and break in the proper sequence during PCB mating and unmating. Placement of the rotary-cam actuator, combined with an open board slot at one end of the connector housing, permits entry of the board for packaging versatility. Top-entry versions are also available. A safety lock prevents the contacts from closing unless the board is properly positioned and helps hold the board in place. Double-sided or multi-layer boards 0.054 to 0.070" (1.372 to 1.778 mm) thick with up to 130 contact pads (65 per side) on 0.100" (2.54-mm) centerline spacing, or up to 100 contact pads (50 per side) with 0.125" (3.175-mm) centerlines, or up to 86 contact pads (43 per side) with 0.156" (3.962-mm) centerline spacing can be used with this connector family. Tandem arrangements with up to 240 contacts (120 per side) are possible. **AMP Inc**, Harrisburg, PA 17105.

Circle 253 on Inquiry Card

LOW COST 24-PIN DIP FIBER OPTIC LINKS

DipLink-1, part of the Fibercom[®] family, is the first in a series of TTL or CMOS compatible, complete fiber optic links in 24-pin DIPs. The transmitter module has a pigtailed visible LED operating at 670 nm, while the receiver module contains a pigtail photodetector. Both modules are 0.4" (1 cm) high. Dupont PFX-P140 plastic core 0.5-m long fiber optic pigtailed are compatible with AMP's low cost Optimate connectors. Data rate, without the necessity of encoding, is from dc to 1M bytes/s over distances of 15 m. Rated performance allows for 2 splices of 2 dB each plus 3 dB for time and temperature variations. Longer pigtailed are offered as options. 12-V supplies can be used for CMOS operation, but the system requires 12 and 5 V for the receiver and 5 V for the transmitter for TTL compatibility. **Radiation Devices Co, Inc**, PO Box 8450, Baltimore, MD 21234.

Circle 254 on Inquiry Card

HANDHELD PORTABLE SIGNATURE ANALYZER LOGIC TESTER



LS-120, a low cost troubleshooting aid particularly applicable for use with hobby and small business computers and peripherals, enables analysis of bit streams of data at IC nodes and location of faulty components. Signature data from the device under test are gated into the analyzer and presented in hexadecimal format on LEDs. The unit is said to operate at system speeds of 10 MHz or greater and have 25-ns input signal setup, diode clamp over-voltage protection, and >99.9% error

detection capability with digital data compression for 16th order polynomial extraction of results. Options include an active probe with state LEDs for additional troubleshooting capability. **Phoenix Digital Corp**, 7745 E Redfield Rd, Scottsdale, AZ 85260.

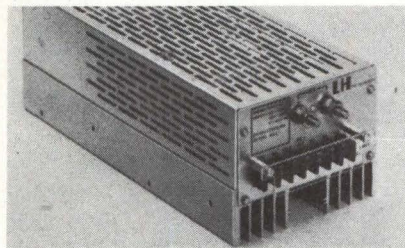
Circle 255 on Inquiry Card

WIDE INPUT RANGE DC-DC CONVERTERS

Line of 9 models powers ± 5 V at 4 A, ± 12 V at 1.7 A, or ± 15 V at 1.5 A analog circuits from 12-, 24-, or 48-Vdc buses or batteries. Low output noise and ripple and use of high attenuation filter reduces kickback spikes and reflected ripple caused by inverter switching. High I/O isolation separates output circuits from dc bus. Either output can be grounded to provide + or - voltages. Low thermal masses and gradients minimize delay in reaching equilibrium after any change in operating conditions from turn-on to full load swings. Shielded case minimizes radiated emi/rfi. **Intronics**, 57 Chapel St, Newton, MA 02158.

Circle 256 on Inquiry Card

MEDIUM POWER SWITCHING SUPPLIES

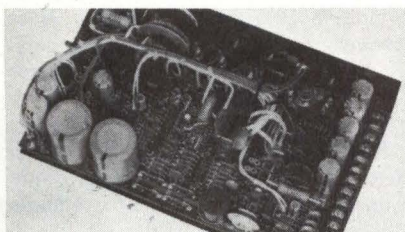


Little-MITE™ series of 250 to 600 W, convection cooled switching power supplies incorporates an IC control chip to reduce number of components and increase reliability. Series offers 92 to 130 or 184 to 260-Vac, 47- to 440-Hz input range for brownout protection. Power fail signal is triggered 16 ms after ac power loss; outputs remain in regulation for 20 ms after nominal power is removed. **LH Research, Inc.**, 1821 Langley Ave, Irvine, CA 92714.

Circle 257 on Inquiry Card

4- AND 5-OUTPUT OPEN FRAME SWITCHING SUPPLIES

SBC series power supplies have 0.2% max line regulation and load regulation of 0.3% max for 5-V output; 5% for ± 12 V, ± 15 V, and ± 24 V; and 6% for -5 V. Available outputs include 5 V at 10 A, ± 12 V at 4 A, and -5 V at 2 A or 24 V at 2 A; 5 V at 15 A, ± 12 V at 4 A or ± 15 V at 4 A, and 24 V at 4 A; and 5 V at 20 A, ± 12 V at 4 A, -5 V at 2 A, and 24 V at 4 A. **KEC Electronics, Inc.**, 21535 Hawthorne Blvd, Torrance, CA 90503.



Circle 258 on Inquiry Card

IEEE-488 DISKETTE SYSTEMS

With a microprocessor based controller performing all programming and formatting functions and ROM firmware offering file management capabilities of advanced disc operating systems, 8000 series systems provide the means for GPIB/IEEE-488 users to add IBM compatible diskettes. Features include IBM 3740 single density or IBM 2/2D dual density format, up to 600k bytes of storage/diskette side, up to 4 single or dual head drives, and data buffering up to 4096 bytes. **Dylon Corp.**, 3670 Ruffin Rd, San Diego, CA 92123.

Circle 259 on Inquiry Card

EXTENDED KEYBOARD OPTION FOR COMPUTER OR CRT

Option for either the ECD 7X computer system or the smart ASCII intelligent terminal includes 2 extra 24-key keypads which can be programmed by the user for special chars or control functions. Software allows user to assign operation of up to 72 keystrokes to 1 key. Any char or key can be reassigned or redefined, such as moving numbers and cursor movement commands to the extra keypads. All 128 key legends can be moved or redrawn to match newly assigned functions. **ECD Corp.**, 196 Broadway, Cambridge, MA 02139.

Circle 260 on Inquiry Card

RACKMOUNTED ASYNCHRONOUS DATA SET

Fitting into the 3000A cabinet and interfacing to EIA RS-232-C and CCITT V.24, RM 3120 is adapted to the implementation of multidrop networks as well as multiple point-to-point circuits. It is line compatible with the company's LDS 120 short-haul modem. Data are transmitted on private or telephone company lines out to 5.5 mi (8.9 km) at speeds up to 9600 bits/s, asynchronous on 26 AWG pairs. It conforms to Bell Publication 43401 at all speeds. **Gandalf Data, Inc.**, 1019 S Noel, Wheeling, IL 60090.

Circle 261 on Inquiry Card

COMPACT PM SERVOMOTOR

Model 33, a compact totally enclosed dc servomotor, incorporates shaft speed control electronics and encoder in motor assembly. Power source is only additional electronics needed. Torque capacity is 600 oz-in, (4.2 N*m). Life expectancy is 2000 continuous hours. Std shaft dia is 0.375" (0.95 cm) and length is 6.88" (17.5 cm). Custom lengths available. Options include pre-loaded ball or sleeve bearings, encoder outputs to 1000 pulses/r, and 12-, 24-, 36-, or 48-Vdc ratings. **K & D Magmotor Corp.**, 90 Prescott St, Worcester, MA 01613.

Circle 262 on Inquiry Card

DELTA DASH® GETS YOUR SMALL PACKAGE THERE IN A BIG HURRY.

Delta handles more over-the-counter shipments of 50 lbs. or less than any other certificated airline. And DASH (Delta Airlines Special Handling) serves 86 U.S. cities plus San Juan. Any package up to 90 inches, width+length+height, and up to 50 pounds is acceptable. DASH packages accepted at airport ticket counters up to 30 minutes before flight time, up to 60 minutes at cargo terminals.

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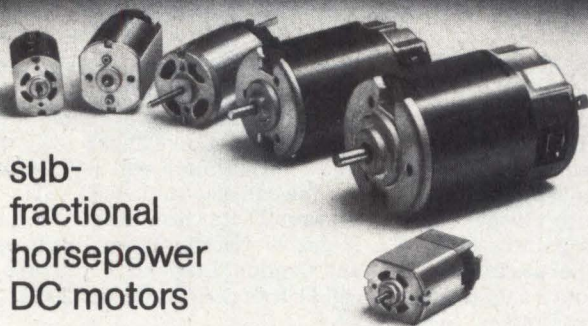


VIKRON

P.O. Box 737, 620 Blanking Woods Rd., St. Croix Falls, WI 54624 (715) 445-5230

CIRCLE 108 ON INQUIRY CARD

Customized



sub-
fractional
horsepower
DC motors

Buehler Products, Inc. offers a complete line of permanent magnet DC motors that are performance rated to your specific application for maximum cost effectiveness. These customized, long life Buehler motors are available with a wide variety of options in voltage, current, torque, speed, electrical connections, and frame size. They're used worldwide in office products, business machines, cameras, computer peripherals, tape recorders, marine and automotive applications. Write for full details on the Buehler FHP motor line.

**FHP permanent magnet DC motors
Miniature brushless DC fans
Miniature gear motors**

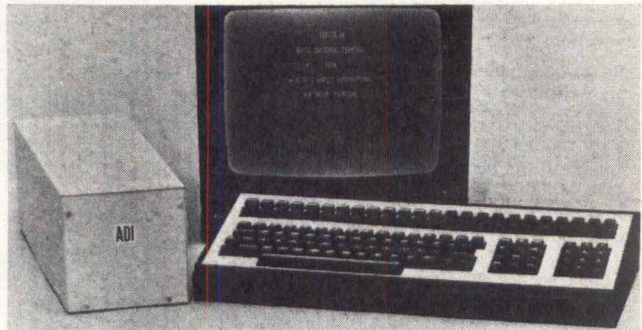
BUEHLER PRODUCTS INC., P. O. Box A, Highway 70 East,
Kinston, North Carolina 28501, (919) 522-3101



CIRCLE 109 ON INQUIRY CARD

PRODUCTS

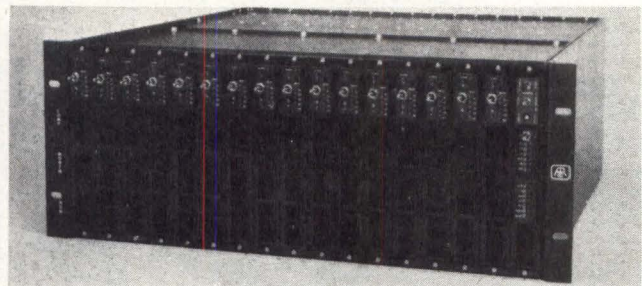
**UNIVERSAL P/ROM PROGRAMMABLE
CRT TERMINAL**



Series 60, a "basic universal terminal," simulates functions and operations of other terminals ranging from dumb to intelligent. A Z80 microprocessor handles communications I/O through a UART, while another special purpose microprocessor is dedicated to display refresh. DMA transfer can be obtained via the bus by locking out the Z80. Modular P/ROM software is both linking and relocatable. The terminal is available in RO, KSR, ASR, and multidrop configurations and in all screen formats from 8 x 16 to 40 x 80. Individual PCB hold program microprocessor, video and timing control, and power supply; three additional boards may be included for internal memory expansion to 8k, floppy disc controller, and other capabilities. ASCII, Baudot, EBCDIC, Hollerith, or other code conversion can be set in when the program is defined. **Applied Dynamics International**, 3800 Stone School Rd, Ann Arbor, MI 48104.

Circle 263 on Inquiry Card

**PATCHING SYSTEM WITH A/B
FALLBACK SWITCH**



DPS-4 Data Patch™ status/alarm and fallback switch system is available in 3 basic configurations: DPS-4-11, basic patching and A/B fallback switching; -1, patching and switching system with status display and A/B fallback switching; -2, same as -1 plus alarm. System is made up of 16 channel modules and a control module in a single assembly. User can choose a single assembly to match a specific application. Features include complete modularity, small size for minimum shelf space, easy maintenance, interface through standard 25-pin RS-232/V.24 connectors, positive locking patch cord, and long life contacts. A/B fallback switch selections can be made on an individual basis or an entire shelf can be switched with a master scan command. **Atlantic Research Corp**, 5390 Cherokee Ave, Alexandria, VA 22314.

Circle 264 on Inquiry Card

9600-BIT/s PRIVATE LINE MODEM

Internal switch setting in model 7296 modem allows transmission or reception of serial binary data at either 9600 or 4800 bits/s over leased voice-grade lines for full-duplex point-to-point operation. Operation over the public switched network is enabled by 7812 line adapter and by making 2 DDD calls. Unit features automatic equalization, integral system test capability, and switch-selectable analog loopback, digital loopback, training, or normal operating modes. **Tele-Dynamics D.v, Ambac Industries, Inc,** 525 Virginia Dr, Fort Washington, PA 19034. Circle 265 on Inquiry Card

HIGH RESOLUTION SHAFT ANGLE ENCODERS

MicroSeries model $\mu S_{-}/16$, 1.6" (4.1-cm) dia x 1.5 (3.8-cm) long, is available with natural binary and BCD mills (1 part in 6400) outputs; and model $\mu S_{-}/23$, 2.3" (5.8-cm) dia x 2.0" (5.1-cm) long has 14, 15-, and 16-bit resolution (0.4 to 0.1 mrad) and natural binary outputs. Features include typically 1024 to 8192 cycles on the fine track, parallel outputs std on natural binary units, and serial outputs std on BCD mills versions. Units are absolute encoders. **Itek Corp, Measurement Systems Div,** 27 Christina St, Newton, MA 02161. Circle 266 on Inquiry Card

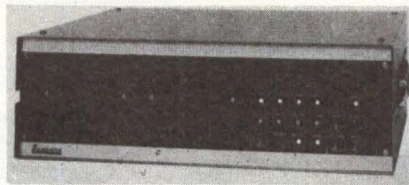
RPG II TEST PACKAGE

200 programs with 19,000 source statements and data records provide comprehensive listing of IBM System/3 compatible RPG II systems. 55 of the programs produce 300 error conditions for the compiler to detect, 125 test compiler and run time, and 20 test system performance with mailing list and label generation and production accounting applications. Package is available on 80 column cards with System/3 OCL directives, or on magnetic tape. **Panatec Inc,** 1527 Orangewood Ave, Orange, CA 92668. Circle 267 on Inquiry Card

4-QUADRANT MULTIPLYING DACs

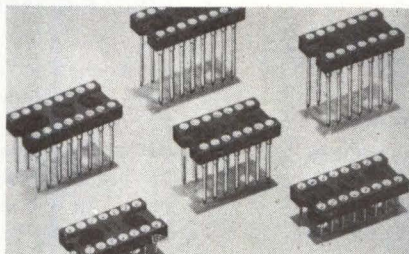
MDAC 1270-1570 series offer 12-, 13-, 14-, or 15-bit resolution and ± 10 -V at 10-mA max or ± 100 -V at 25-mA max output. Modular converters process binary and 2's complement inputs. Available with bipolar outputs, the units offer accuracy to $\pm 0.006\%$ FSR, settling time of 50 μs to 0.005%, and 15 ppm/ $^{\circ}C$ tempco. The 4.5 x 5.0 x 0.75" (11.4 x 12.7 x 1.9-cm) units have less than 0.5 LSB noise. **Phoenix Data, Inc,** 3384 W Osborn Rd, Phoenix, AZ 85017. Circle 268 on Inquiry Card

AUTOMATED CABLE AND BACKPLANE TESTER



Microprocessor controlled CBT/128 reduces testing of cables, backplanes, or wire wrapped circuit boards to a simple automated procedure. In auto-learn mode, the system memory records configuration of a known-good unit, which constitutes a master image against which all similar units to be tested are compared. Individual circuits are checked for open or shorted condition; errors are identified by both type of fault and exact pin location. Tester features basic 128-pin capability, but expands to 2048 pins in 128-pin increments. **Sensitek,** 127 Gaither Dr, Moorestown, NJ 08057. Circle 269 on Inquiry Card

SLIM BODY DIP SOCKETS



ICS series features socket bodies that are 0.400" (10.16 mm) wide and 0.125" (3.175 mm) high to allow max board area IC mounting. Contact is gold plated beryllium copper, and body is molded from glass filled polyester UL rated 95 V-0. All sockets feature pin 1 orientation and counter-bored mounting holes. Machined brass sleeve with wire-wrap or solder termination is available in bright tin or gold finish. **Samtec, Inc,** 810 Progress Blvd, New Albany, IN 47150. Circle 270 on Inquiry Card

LINE VOLTAGE REGULATOR

Static ac unit features $\pm 0.25\%$ line voltage regulation, 10 to -20% input voltage range, line noise filtering, voltage spike clipping, remote sensing with adjustable output, and shielded isolation transformer. It is available in 10 sizes from 10 to 500 kVA, and from 208 to 15k V, customer specified. Control elements are high quality thyristors, capable of handling all overloads up to complete short circuit. Gate control circuitry is solid state using ICs on interchangeable PCBs. **Rapid Electric Co, Inc,** Graysbridge Rd, Brookfield, CT 06804. Circle 271 on Inquiry Card

Quartz Crystals

for OEMs

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has them all

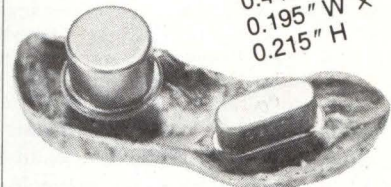
1kHz to 185 MHz
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New!

High Stability 10 MHz
in T0-5 Cans for synthesizers,
clocks, counters, etc.
Ratings from ± 3 to 30ppm
available to
OEMs from stock
at very low prices

0.7 to 1.3 MHz
in HC-18
Goldweld (modified)

0.445" L x
0.195" W x
0.215" H



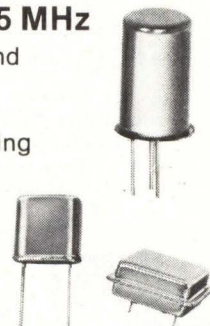
Excellent Stability, High Q
The smallest known package
for this frequency range.

1 kHz to 1 MHz JT • DT
DT Bar • NT • E (+5° Ext.)
H (+5° Flex.)

1 MHz to 185 MHz

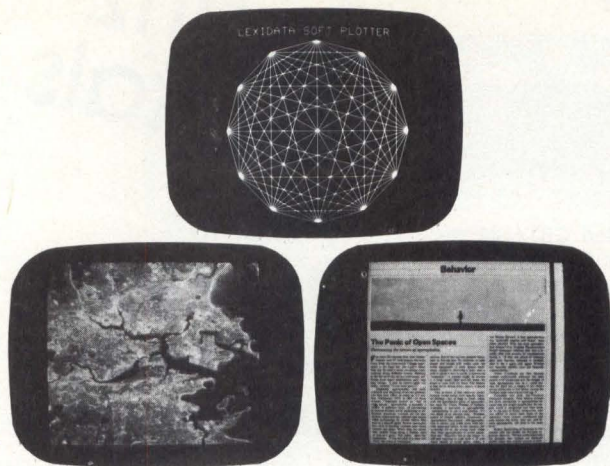
Fundamental and
Overtone
Excellent
Freq./Temp./Aging
Characteristics

for
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PRODUCTS

PM DC MOTORS WITH BUILT-IN TACHOMETERS

Built-in tachometer for controlling speed, low electrical and mechanical interference levels, lifetime self-lubricating bronze bearings, balanced armatures for smooth performance, and die-cast zinc end plates are features of series 13.45 and



13.65 permanent magnet dc motors designed for applications such as floppy disc drives and cartridge, cassette, and reel tape players. Voltage range is 10 to 16 V and nom operating speed is 3000 r/min. (Available motors without tachometers

have voltage range of 6 to 24 V and max operating speed of 10,000 r/min.) Torque range is 0.15 to 1 oz-in (0.1 to 0.7 N*cm). Speed deviations are $\pm 1\%$ to torque range, $\pm 0.5\%$ to voltage range. Tachometer data include output of 1.8 V rms per 1000 r/min, linear within 0.5% over $\pm 10\%$ speed deviation from 3000 r/min, and distortion within 8% at 400 cycles. **Buehler Products, Inc**, PO Box A, Hwy 70 E, Kingston, NC 28501.

Circle 272 on Inquiry Card

SINGLE-BOARD GRAPHICS IMAGING SYSTEM

RGB-256, a single PCB containing a complete color/gray scale imaging system, features 256 x 256-dot resolution with 4 bit planes. It includes built-in NTSC (American) or PAL (European) color and gray scale encoders that provide up to 16 shades or colors. The encoders permit the system to directly drive standard TV monitors on a single 75- Ω cable. An onboard phase lock loop permits the output to be synchronized to an external video source. Two cards can be combined to give 8 bit planes. This 2-card system, with no additional hardware, will give a total of 256 colors or gray levels. Standard 5-and ± 12 -V power supplies are used. An industry standard Intel MultibusTM makes the system plug compatible with all Intel and National single-board computers. **Matrox Electronic Systems Ltd**, 2795 Bates Rd, Montreal, Quebec H3S 1B5, Canada.

Circle 273 on Inquiry Card

UNIVERSAL P/ROM PROGRAMMERS WITH BUILT-IN CRT TERMINAL

The PPG ganged programmer accepts most EPROMs, programming up to 15 at a time. Before programming commences, the unit executes a number of test sequences to eliminate any possibility of error. If an error is discovered,

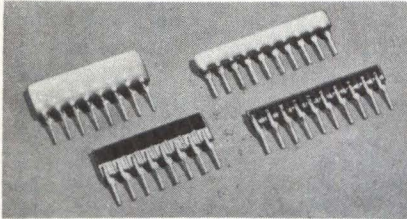


the operation is halted and the fault is displayed. EPROMs are tested for faults on power supply, data, and address pins. The RAM is sum-checked and the EPROMs checked to be empty before they are programmed according to the

manufacturer's specifications. When programming is complete, the EPROMs are individually checked against the RAM and the RAM is again sum-checked before an OK is displayed. Individual red LEDs light up near each EPROM socket to indicate faulty devices, while the alphanumeric display shows the type of fault. **Stag Systems**, 2465 E Bayshore, Rm 329, Palo Alto, CA 94303.

Circle 274 on Inquiry Card

STANDARD SIP RESISTOR NETWORKS



Series HC and HF resistor networks are high stability cermet resistors deposited on an alumina substrate in single-inline packages. Units are offered in 4-, 6-, 8-, 10-, and 14-pin packages, and 4 seated height configurations: 0.200, 0.250, 0.300, and 0.350" (0.500, 0.635, 0.762, and 0.889 cm). Resistance range is offered from 33 Ω to 470 k Ω with a std resistance tolerance of $\pm 2\%$. Std circuit configurations are 1 pin common and isolated resistors. **Centralab Electronics Div, Globe-Union, Inc.**, 5757 N Green Bay Ave, Milwaukee, WI 53201. Circle 275 on Inquiry Card

50-MHZ PULSE GENERATOR



Model 101D has repetition rates to 50 MHz and output capability to ± 20 V. A VMOS FET device stabilizes the 20-V output. Selectable output control modes are: upper/lower level, amplitude/base-line offset, and zero reference control. Transition times are variable from 6 ns to 500 ms and are independent of each other. **Systron-Donner Corp, Instrument Div**, 10 Systron Dr, Concord, CA 94518. Circle 276 on Inquiry Card

PCB MOUNTING RELAYS

For data processing, communications, measuring and control equipment, FRL 640 series epoxy molded low profile relays offer immersion cleaning safety and solid construction. They come in 1 Form A, 1 Form B, 2 Form A, and 2 Form B, with type 8 for switching under std conditions (50 VA max or 100 Vac, 0.5 A max) and type K for switching under heavy loads (10 W max or 100 Vdc, 0.5 A max); 5-, 6-, 12-, and 24-Vdc units are available. **Fujitsu America, Inc, Component Sales Div**, 910 Sherwood Dr—23, Lake Bluff, IL 60044.

Circle 277 on Inquiry Card

IEEE-488 INTERFACE BOARD FOR LOGIC STATE ANALYZER

Interface board permits model 532 intelligent logic state analyzer to function as a listener/talker on an IEEE-488 bus. Board plugs in to any slot in the 532's internal microprocessor bus and allows remote operation of all front panel functions from an IEEE-488 controller. RS-232-C capabilities also are available. **Paratronics, Inc.**, 800 Charcot Ave, San Jose, CA 95131. Circle 278 on Inquiry Card

DISC PACK FOR UNIVAC DRIVE

Mark XVIII pack, designed for use on Sperry Univac 8418 disc drive, stores 58M bytes of information. Special particle-oriented coating formulation provides maximum data reliability, reduced head wear, and longer life. Other features include a nonflammable Lexan[®] cover, temper-hardened steel locking assembly, and forged aluminum hubs. **Memorex Corp**, San Tomas at Central Expy, Santa Clara, CA 95052. Circle 279 on Inquiry Card

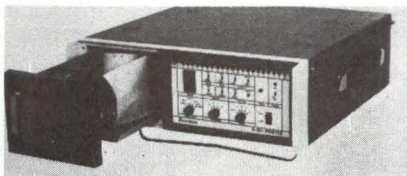
DIP SWITCH

12-position Bit[™] switch is a PCB mounted group of spst switching positions. 1.280 x 0.385 x 0.280" (32.512 x 9.779 x 7.112-mm) DIPs are designed for over 2000 switching operations for each position. Programmable in 5-s, 5-min, 12-h intervals, plus combinations of these, the device has a barrier strip that prevents unintentional programming. **Stanford Applied Engineering, Inc.**, 340 Martin Ave, Santa Clara, CA 95050.

Circle 280 on Inquiry Card

DATA TRANSMISSION MONITOR AND PRINTER

D-201 can be used as a peripheral to the company's D-500 and -600 series Datascope monitors to monitor asynchronous lines at any transmission rate from 50 to 9600 bits/s, and provide hardcopy of data originally sent at up to 100 bits/s using virtually any line discipline. Hex, ASCII, EBCDIC, and other codes are printed at up to 900 char/s. As a standalone hardcopy line monitor, the unit provides simplex and half-duplex operation. **Spectron Corp**, PO Box 620, Moorestown, NJ 08057.



Circle 281 on Inquiry Card

MFM floppy, 1 head or 2

AED's field-proven 6200 Series floppy disk system has recently been expanded to provide the minicomputer user with a wider choice of disk drive capability. The AED6200 Series now offers double density (MFM) systems in four configurations: 2 drives with single head (5 $\frac{1}{4}$ " and 7" cabinets), 4 drives with single head (10" cabinet), 2 drives with dual head (7" cabinet) and 4 drives with dual head (two 7" cabinets). All systems come complete with formatter, power supply, drive electronics and CPU interface. Interfaces for LSI-11, PDP-8 and 11, Nova/Eclipse, Varian, Interdata and CAI are all available from AED.

Here is a checklist of the AED6200's outstanding user benefits:

- low cost, fast access storage
- 1.2 megabytes/diskette
- industry standard 8" media
- programmable formatter for ideal record size
- multiple source drives
- 8 computer interfaces available
- expandable to 4 drives
- CRC and IPL for easier loading
- delivery from stock on all popular models

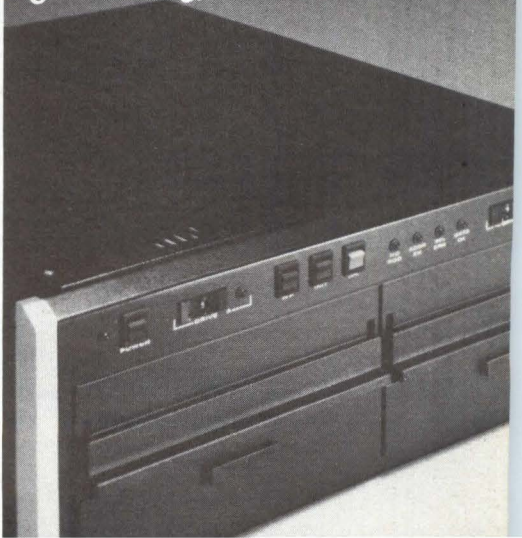
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440 Potrero Ave., Sunnyvale, CA 94086
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AED 6200

gives you more for your mini
CIRCLE 82 ON INQUIRY CARD



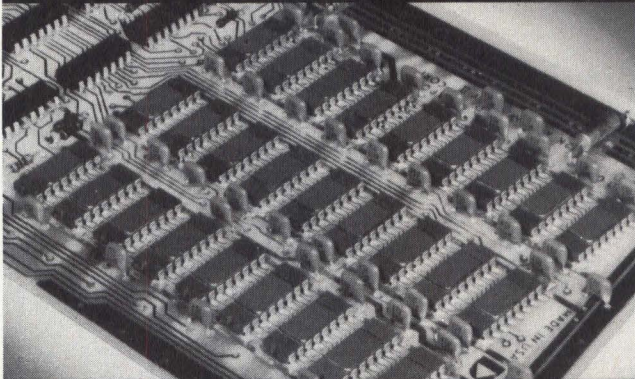
"BLUE MAX" DID IT!

Datapoint Corp. of San Antonio, Tex. needed a capacitor of miniature size, with maximum CV ratings, of consistent quality, and at a competitive price. They chose the KEMET "Blue Max" dipped monolithic ceramic capacitor. It comes in three dielectrics, six case sizes, with more than 350 CV ratings, in capacitance values from 2.2 pF to 4.7 μ F, in 50, 100 and 200V ranges. For more information, write: Components Dept., Union Carbide Corporation, P.O. Box 5928, Greenville, SC 29606. Phone: (803) 963-6300. Or see your local KEMET Capacitors Distributor.

KEMET[®] OFFERS YOU MORE.



Datapoint 5500
Advanced Business Processor

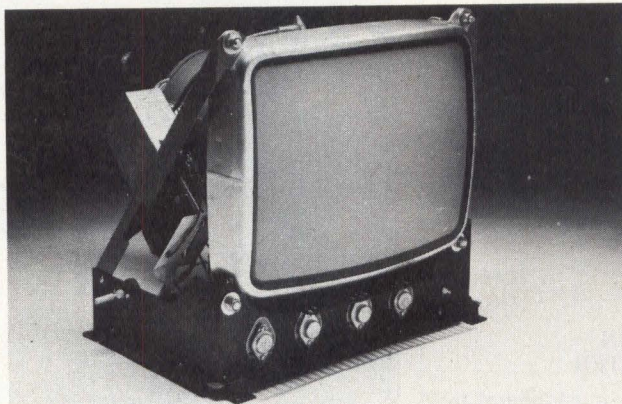


ELECTRONICS DIVISION
COMPONENTS DEPARTMENT

In Europe: Union Carbide Europe, S.A. 5, Rue Pedro Meylan,
Geneva 17, Switzerland Phone: 022/47 4411 Telex: 845-22253

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CIRCLE 112 ON INQUIRY CARD



No Frills Color. Just the basics. If you're a black and white terminal manufacturer, the Intecolor 813 is all you need to upgrade your terminals to color.

It consists of an 8-color, 13" CRT, plus a special Analog Module System with all the circuitry necessary to perform deflection and video drive functions for the CRT. The completely self-contained circuitry is on a single printed wiring board which also generates the low voltage, high voltage and CRT bias, mounted on a sturdy aluminum frame for heat sinking the power transistors needed for the circuitry.

With our Nine Sector Convergence System, perfect color registration takes only three to five minutes. And this convenient control panel can be located anywhere for easy access.

Available in standard 262 Raster line or 400 Raster line high scan versions. If you're ready to upgrade to a color line, call 404/449-5961 for a demonstration.

Color Communicates Better

Intelligent Systems Corp.



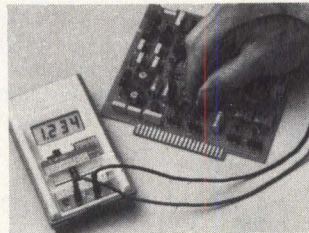
5965 Peachtree Corners East/Norcross, Georgia 30071
Telephone 404/449-5961 TWX: 810-766-1581

CIRCLE 113 ON INQUIRY CARD

PRODUCTS

3½-DIGIT POCKET SIZED DIGITAL MULTIMETER

A personal size DVOM for test and measurement applications, the LX 303 includes "large unit" features such as autozero, automatic polarity and overrange indication, and 200-mVdc full scale sensitivity. A snap on cover holds test leads and



protects the panel when not in use. Both function and range switches are configured for easy selection with the same hand that holds the unit. Angle mounted 0.5" (1.27-cm) liquid crystal display provides wide viewing angle. Measurements can be made on 5 dc ranges

from 0.1 mV to 1000 V (accuracy of $\pm 0.5\%$ per reading and full scale); ac ranges from 40 Hz to 5 kHz of 0.1 to 600 V (accuracy $\pm 1.0\%$ per reading, $\pm 0.5\%$ FS); 6 low power resistance ranges from 0.1 Ω to 20 M Ω ; and 6 dc current ranges from 0.1 nA to 100 mA. Size is 5.875" x 3.375" (14.9 x 8.57 cm). Weight is 8 oz (0.227 kg). **The Hickok Electrical Instrument Co.**, 10514 Dupont Ave, Cleveland, OH 44108.

Circle 282 on Inquiry Card

HIGH END BUDGET LABORATORY COMPUTER SYSTEM

DEClab-11/MNC, containing greater online storage capacity than the entry-level MINC system and increased programming flexibility, employs twin RL01 disc storage units for a standard 10M-byte capacity. Its fundamental programming is done in ANSI-standard FORTRAN IV, supplemented with company supplied subroutine packages. The user can customize the system's configuration through use of as many as 8 plug-in modules for both interfacing and control. Central element of the system is a 41" (104-cm) high central sub-assembly that incorporates a PDP-11/03 microcomputer with 64k bytes of semiconductor memory. Other system elements include twin removable storage discs, 4-port terminal interface, ROM diagnostic bootstrap, and either an LA36 DEC-writer II or a VT105 video terminal, which can display both alphanumeric and point-plot or histogram waveform data. **Digital Equipment Corp.**, Maynard, MA 01754.

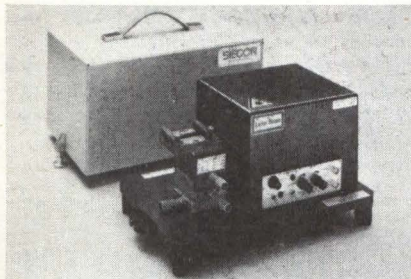
Circle 283 on Inquiry Card

KEYBOARD SWITCH MODULES

Any desired keyboard format can be set up for prototype, short run, or high volume production with System 87 switch modules. Available are single rows of 1 through 6 switches, with circuitry in single pole/common bus configurations, which can be arranged into row and column switching when switches are stacked; also offered are 3 x 4 and 4 x 4 keyboard pads with matrix coding plus single pole/common bus circuitry. When modules are stacked side by side, buttons are on 0.5" (1.27-cm) centers. Snap-on cap design allows legends to be added on cards for prototypes, or hot stamped or molded for long runs. Switching is accomplished by a snap-dome contact system that provides tactile and audio feedback to the operator. Life cycle is estimated at 3 x 10⁶ operations. Modules measure only 0.350" (0.889 cm) off the PC board. **Grayhill, Inc.**, 561 Hillgrove Ave, La Grange, IL 60525.

Circle 284 on Inquiry Card

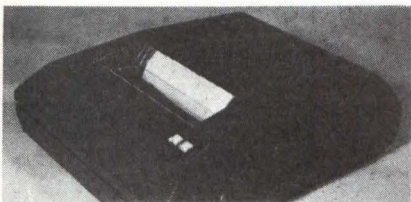
FIBER OPTIC CABLE MONITOR AND TESTER



Optical time domain reflectometer model 38 simplifies testing by making measurements when only one end of the fiber optic cable is accessible. Used with an oscilloscope the instrument can evaluate cable during and after installation, monitor field splicing and terminal connection operations, and perform quality control tests during cable manufacturing. Short light pulses and back-scattering and reflection characteristics of the fibers are used to determine length of fiber, evaluate splice or connector continuity, measure cable attenuation, assess fiber homogeneity, and locate fracture. **Siecor Optical Cables, Inc.**, 631 Miracle Mile, Horseheads, NY 14845.

Circle 285 on Inquiry Card

120-CHAR/S BIDIRECTIONAL PRINTER



Micro/Mini model 879 prints 120 char/s or 75 lines/min, using a 9 x 7 or 9 x 9 matrix to form the 96-char ASCII set (upper, lower, and triple wide). 80- or 32-col format is switch selectable. Available with roll paper feed, combination pin form and roll feed, or tractor feed, printer uses RS-232 and parallel interface. **Printer Terminals Corp.**, 124 10th St, Ramona, CA 92065.

Circle 286 on Inquiry Card

6-DIGIT, 0.5" LED DISPLAY

GaAsP display NSB5931 is a second source for Litronix DL6500 display. The device, built on a std PCB with plastic reflector and lens cap attached, contains six digits, each composed of 7 segments with right hand decimal point. Average current per segment is rated at 20 mA; peak current per segment is rated at 150 mA for 1 ms. **National Semiconductor Corp.**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

NUMERICAL THERMAL PRINTER MECHANISM

Essentially noiseless, the ANP-9M provides 7 col of 7-segment numbers (or 6 col with a \pm sign in the first, second, or third col), and 2 col of data identification either before or after the numbers. Data identification columns contain a dot print head which can print 5 x 7 letters, numbers, and engineering symbols. Units are available as a basic mechanism which mounts behind the user's panel or with an hinged bezel that permits the mechanism to be swung forward for paper loading from the front panel. **Gulton Industries, Inc., Measurement & Control Systems Div.**, East Greenwich, RI 02818.

Circle 287 on Inquiry Card

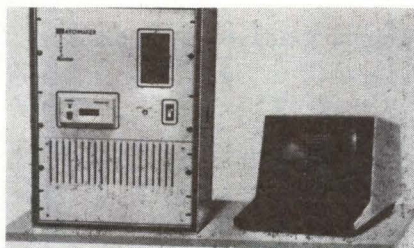
REVERSIBLE PM GEARMOTOR

Continuous torque of 100 lb-in (11.25 N*m) and speeds from 0.48 to 3100 r/min are features of the type EMR/EML motor which measures 1.5" (3.8 cm) dia with a max length of 6" (15.24 cm). Weights, depending on options and specific gear ratios desired, range from 11 to 80 oz (312 to 2268 g); 17 speed reduction ratios range from 3.67:1 to 6564:1. Options include special shaft extensions, shaft pinions, rfi filters, brakes, tachometers, and rated voltages from 6 to 115 Vdc. **Powertron Corp.**, 3821 Barringer Dr, Charlotte, NC 28210.

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PRINTED CIRCUIT BOARD AND BACKPLANE TESTER

Matchmaker high speed automatic continuity test system is available in 2 configurations—one completely self-contained incorporating keypad and 40-char alphanumeric display and the other with 24-line CRT and direct access for program editing. System performs variety of tests on PCBs, backplanes, wire and cable harnesses, and switch and relay assemblies at a test time of about 1 s per 1k points. Both versions operate on 115/230 Vac at 47 to 63 Hz and are available with 4k-, 8k-, and 16k-point capacity in 100-point increments. **Add'son Div, Muirhead Inc.**, 1101 Bristol Rd, Mountainside, NJ 07092.



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EMULATOR CONTROLLER

The AED8000 emulator/microcontroller provides cost effective data control and intermediate data buffering between your CPUs and Mass Storage disks. A total of 8 disk drives in any combination, including Winchester, can be utilized at one time; and up to 4 CPUs can be interfaced through the AED8000 Microcontroller interface electronics. The AED8000 emulates the OEM disk controller through generational changes, saving you money by not requiring you to write the software driver over and over again. And the controller not only runs the software for the emulated disk, but runs the mainframe manufacturer's disk diagnostics as well!

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- 256 x 16-bit data buffer

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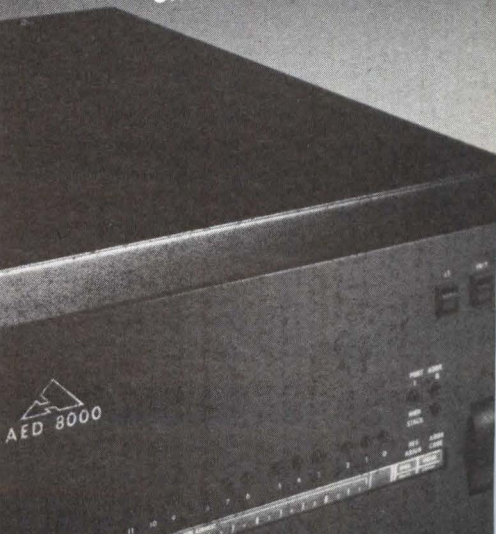
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Microcomputers

Catalog describes TRS-80 system—microcomputers, Level-I, and -II BASIC, interfaces, memories, disc systems, and printers—in plain language. **Radio Shack, A Div of Tandy Corp**, Fort Worth, Tex. Circle 300 on Inquiry Card

Communications Components

Catalog includes specs and applications for microprocessor controllable tone encoders, Touch Tone[®] detectors, CCITT std channel bandpass filters, C-message and C-notch weighting filters, and PCM pre-filters. **Frequency Devices, Inc**, Haverhill, Mass. Circle 301 on Inquiry Card

A-D/D-A Peripheral Boards

Slide-in SineTrac boards for micro- and minicomputers and for microprocessor based computers are described in brochure which also provides selection guides and block diagrams. **Datel Systems, Inc**, Canton, Mass. Circle 302 on Inquiry Card

Switches

Photos, line drawings, specs, and ordering information on more than 300 switches, including 16-A rocker switch and custom switches, are covered in catalog. **Chicago Switch, Inc**, Chicago, Ill. Circle 303 on Inquiry Card

EMI Filters

Circuit diagrams, performance graphs, specs, and dimension drawings of case styles are supplied in 16-p catalog. **Stanford Applied Engineering**, Santa Clara, Calif. Circle 304 on Inquiry Card

μComputer Analog I/O Systems

Technical specs in 74-p catalog cover analog I/O systems for DEC, Computer Automation, Intel, Zilog, and National families, as well as busable data acquisition modules, DACs, and dc-dc converters. **Data Translation, Inc**, Natick, Mass. Circle 305 on Inquiry Card

Data Communications Test Equipment

Intershake[®] line of monitors and programmable testers for data communications network diagnostics and maintenance is described in brochure. **Atlantic Research Corp**, Alexandria, Va. Circle 306 on Inquiry Card

Electrical Connectors for Hostile Environments

Photos, dimension drawings, and spec charts supply technical details for 10 lines of equipment, engineered for temps from absolute zero to 677 °C, for resistance to nuclear radiation, and operation under watertight conditions. **ITT Cannon Electric Canada**, Whitby, Ontario, Canada. Circle 307 on Inquiry Card

Microcomputer Applications

"The micronOVA Cookbook, A Taste of Success" discusses applications for the family in industrial automation, communications, data acquisition and control, commercial data systems, and instrumentation. **Data General Corp**, Westboro, Mass. Circle 308 on Inquiry Card

Optical Data Link

Specs, dimension drawings, and block diagram are presented in brochure that describes solid-state link using IR focused sources and detectors to provide bidirectional, wireless, noise-free digital data transmission. **AMREX Corp**, Redmond, Wash. Circle 309 on Inquiry Card

CMOS Multiplying D-A Converters

Guide provides section on theory and cites more than 25 applications using DACs including digitally programmable control circuits, programmable active filters and oscillator circuits, and audio and synchro applications. **Analog Devices**, Norwood, Mass. Circle 310 on Inquiry Card

Wirewound Resistors

Engineering handbook covering precision and power devices includes military style cross-reference chart, temp coefficients, multiplying factors for resistance wire diameters, and heat distribution curves. **RCL Electronics Div, AMF Inc**, Manchester, NH. Circle 311 on Inquiry Card

Personal Computer Components

Block diagrams and specs for microprocessors; memories; CRT controllers; LED displays; floppy disc, analog, printer, serial, and parallel interfaces; and sound synthesizers are featured in brochure. Free copy available from **National Semiconductor Corp**, MS/770, 2900 Semiconductor Dr, Santa Clara, CA 95051.

Data Communications Monitor

Function descriptions accompany full front panel photo of D-502B; brochure also furnishes program flowchart and instruction summary table for monitor/analyzer/interactive simulator and tester. **Spectron Corp**, Moorestown, NJ. Circle 312 on Inquiry Card

Modular Power Supplies

Operating specs and dimensions are provided for switching and linear supplies with single, dual, or wide range adjustable outputs, open frame construction, and encapsulated PC board mounting supplies. **Sorensen Co**, Manchester, NH. Circle 313 on Inquiry Card

Realtime Analyzers

Guide compares characteristics of the company's 660A dual-channel FFT analyzer to the Hewlett-Packard 5420A digital signal analyzer. **Nicolet Scientific Corp**, Northvale, NJ. Circle 314 on Inquiry Card

Tape Reader Products

Technical data, specs, and key characteristics for more than 14 hardware configurations including interface accessories and ruggedized military units are presented. **EECO**, Santa Ana, Calif. Circle 315 on Inquiry Card

Distributed Systems

Two brochures define distributed processing; provide diagrams of hierarchical, horizontal, and hybrid system structures; and cite compatibility between host and satellite processors. **Honeywell Information Systems**, Waltham, Mass. Circle 316 on Inquiry Card

Disc/Tape Supplies

Digital cassettes, diskettes, microfiche accessories, mini-cassettes, quick release splicing patches, perforated tape, magnetic splicers, encoders, and std and laminated control tapes are presented in catalog. **Robins Industries Corp, Data Products Div**, Commack, NY. Circle 317 on Inquiry Card

μProcessor Support Equipment

Descriptions, photos, and specs for P/ROM programmers, system analyzers, microprocessor cards, courses, and literature are included in 64-p catalog. **Pro-Log Corp**, Monterey, Calif. Circle 318 on Inquiry Card

5-V Switchers

Application note supplies circuit diagrams and parts lists for 100-, 500-, and 1-kW 5-V switching power supplies. **TRW Power Semiconductors**, Los Angeles, Calif.
Circle 319 on Inquiry Card

Data Acquisition System

Expanded Series 2000 line offering specialized equipment and SSI, MSI, and LSI systems is described in brochure. **FX Systems Corp.**, Kingston, NY.
Circle 320 on Inquiry Card

Digital Synthesizer Analyzer

Processor based instrument uses state-linear format to capture, program, display, and generate up to eight digital signals or pulse trains simultaneously. **Gould Inc., Instruments Div.**, Cleveland, Ohio.
Circle 321 on Inquiry Card

Breadboarding and Packaging Products

Short-form catalog includes photos, specs, and dimensions for microprocessor boards, Plugboards™, prepunched boards, prototype, and production hardware. **Vector Electronic Co.**, Sylmar, Calif.
Circle 322 on Inquiry Card

Miniature Potentiometer

Series 100 potentiometers, designed for use in laboratory instruments, telecommunication equipment, and computers, are described with design specs and dimension diagrams in 6-p brochure. **Centralab Electronics Div., Globe-Union Inc.**, Milwaukee, Wis.
Circle 323 on Inquiry Card

Electronic Hardware

Illustrations and descriptions of shoulder screws, retainers, panel screws, male and female swage type standoffs, pusher screws, washers, and handles are featured in 208-p catalog. **Promptus Electronic Hardware, Inc.**, White Plains, NY.
Circle 324 on Inquiry Card

DC Motors, Speed Controls, and Servo Systems

Engineering handbook contains updated technical information and covers optical encoders in technical detail. To obtain a copy send \$1.00 (to cover postage) with business card or company letterhead to **Electro-Craft Corp.**, Box 664, Hopkins, MN 55343.

Disc Packs

Flyer contains criteria for matching disc packs to drives based on drive's error correcting circuitry. **Nashua Corp., Computer Products Div.**, Nashua, NH.
Circle 325 on Inquiry Card

Programmable-Gain Amplifiers

Application note lists schematics, specs, and sample programs for both program controlled and autoranging units for use in data acquisition systems. **Micro Networks Corp.**, Worcester, Mass.
Circle 326 on Inquiry Card

DIP Switches

Electrical and mechanical specs, photos, and dimension drawings comprise information on line of switches. **CTS Corp.**, Elkhart, Ind.
Circle 327 on Inquiry Card

Transformers/Solenoids

Complete specs including dimensions and ratings, plus application hints for transformers, solenoids, converter/chargers, and coils, are given in condensed catalog. **Dor-meyer Industries**, Chicago, Ill.
Circle 328 on Inquiry Card

2400-Bit/s Data Modem

Brochure first outlines then details features and options of modem, and includes technical data and a section of advanced applications. **Codex Corp.**, Mansfield, Mass.
Circle 329 on Inquiry Card

Cable Shield Terminations

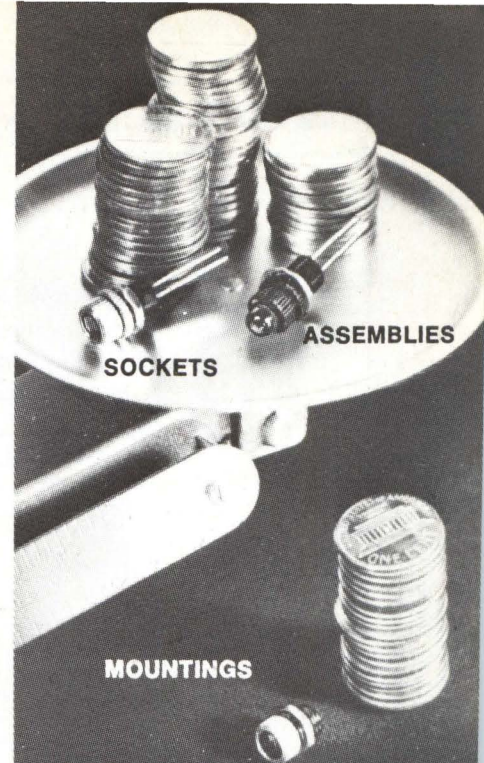
Series of 1-p data sheets presents the features and specs of various Solder Sleeve™ cable shield terminations. **Electronics Div., Raychem Corp.**, Menlo Park, Calif.
Circle 330 on Inquiry Card

Data Converters

Selection guide summarizes specs for 80 models of DACs and ADCs and includes table of pin-for-pin equivalents. **Hybrid Systems Corp.**, Bedford, Mass.
Circle 331 on Inquiry Card

Add-On Memory

Brochure lists specs for and describes line of add-on semiconductor memory systems and add-on automatic maintenance panel. **Storage Technology Corp.**, Louisville, Colo.
Circle 332 on Inquiry Card



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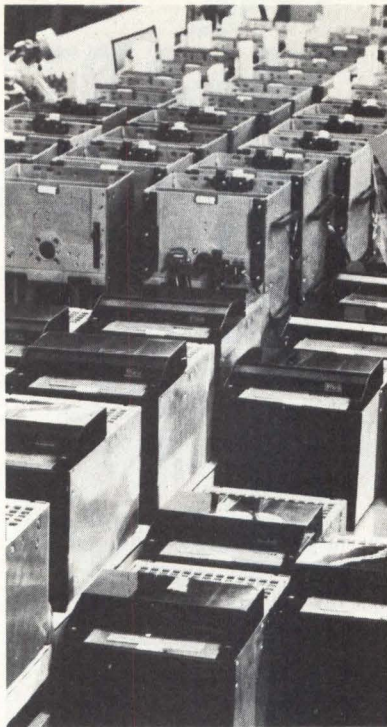
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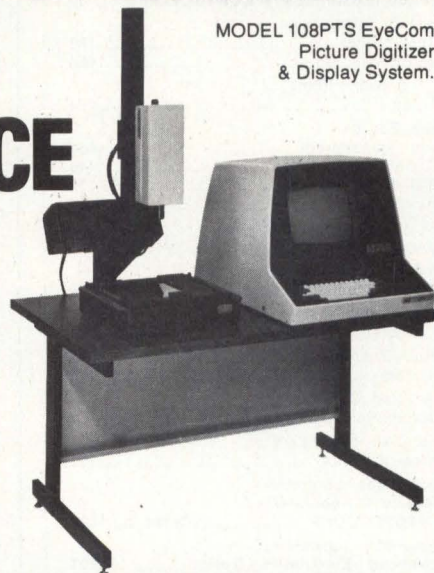
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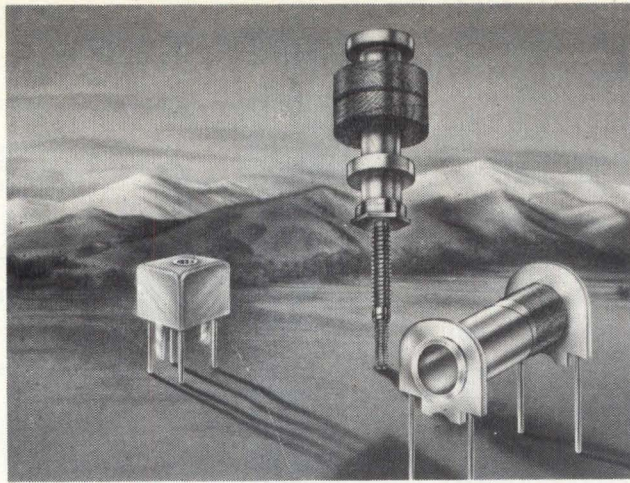
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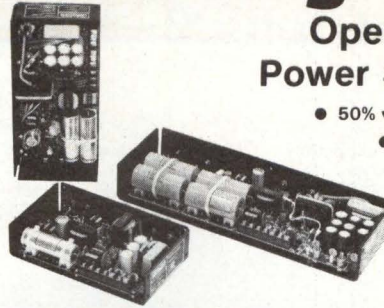
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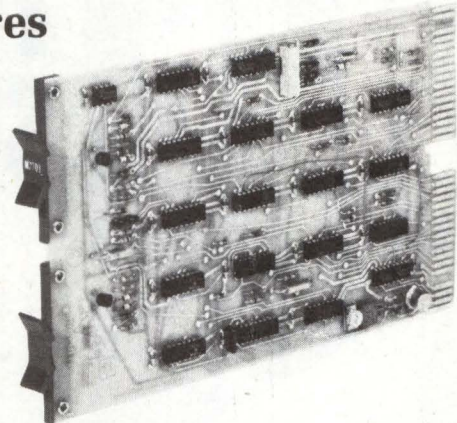
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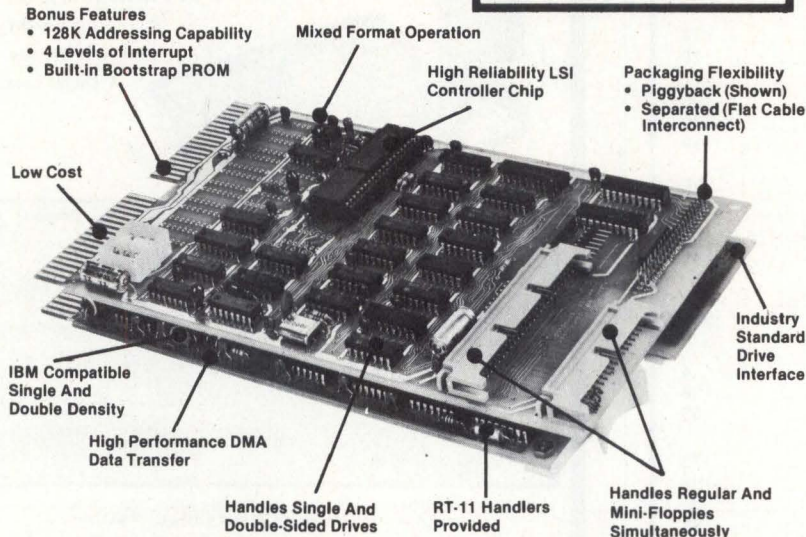
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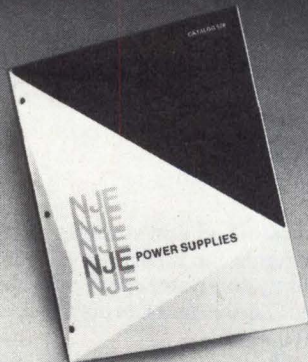
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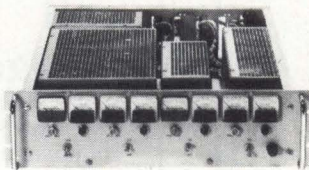
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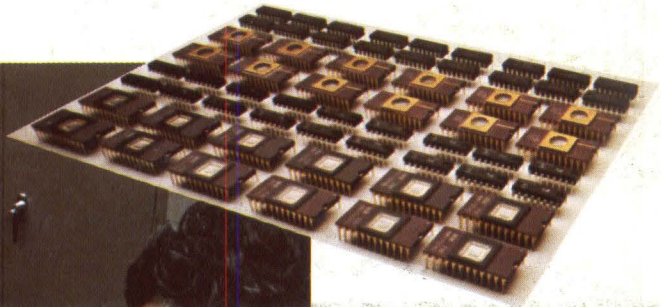
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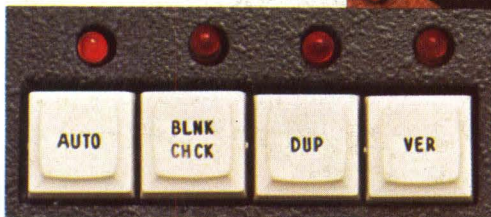


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