A PENNWELL PUBLICATION

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

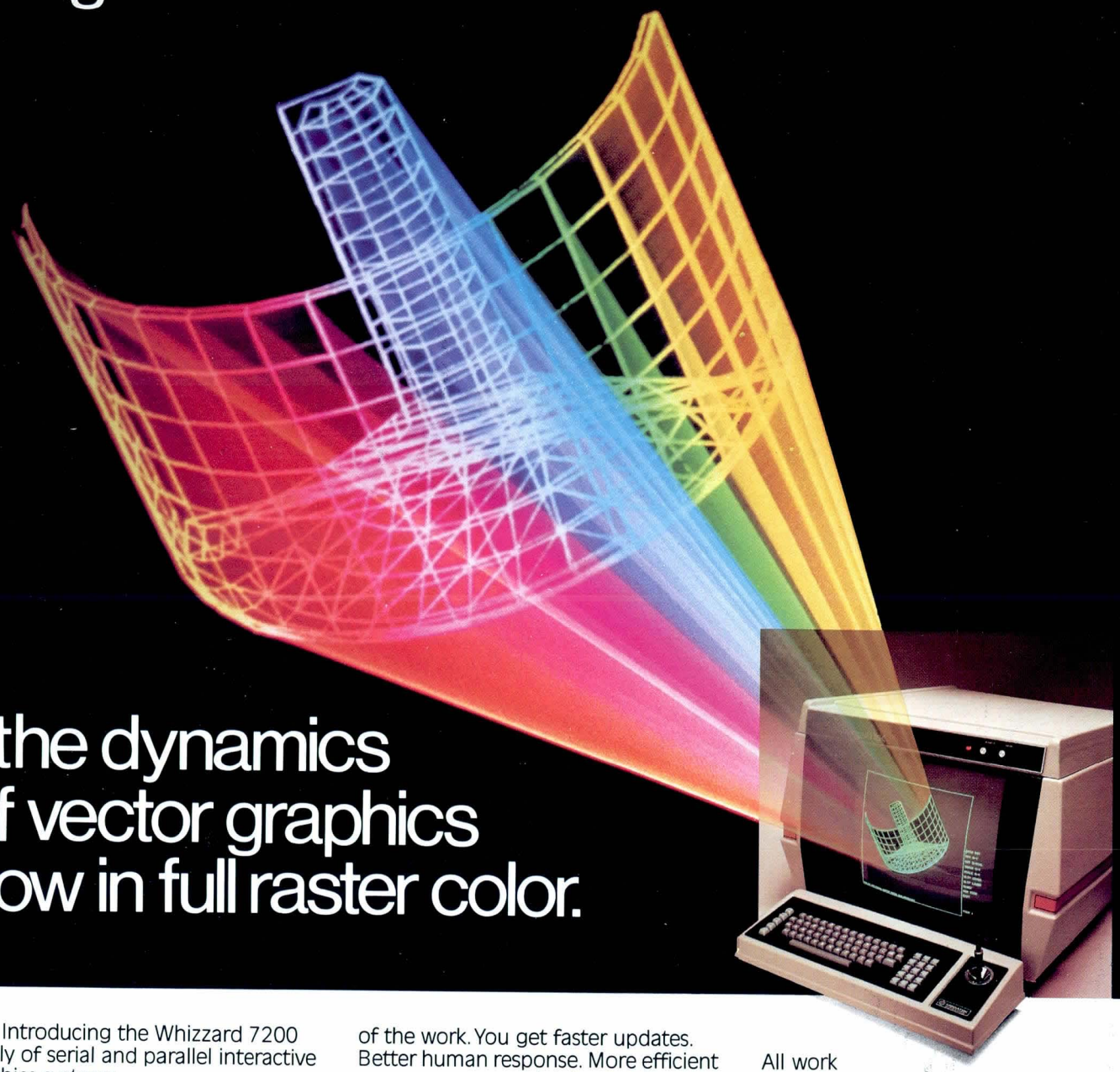
MAY 1981

LOW COST POWER TRANSIENT PROTECTION

MULTIPROCESSOR DESIGNS OUTPERFORM SUPERMINI ALTERNATIVES FOR CONTINUOUS SYSTEM SIMULATION

A DESIGNER'S REVIEW OF DATA COMMUNICATIONS

Imagine...



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Included are two new high-performance color raster Whizzards so fast they can modify complex engineering displays at a remarkably high frame rate — speed that rivals the powerful refresh vector output Megatek is known for.

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For details, call or write Megatek Corporation, 3931 Sorrento Valley Blvd., San Diego, CA 92121. (714) 455-5590.

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COMPUTER GRAPHICS SYSTEMS

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THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

MAY 1981

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BPA

ABP

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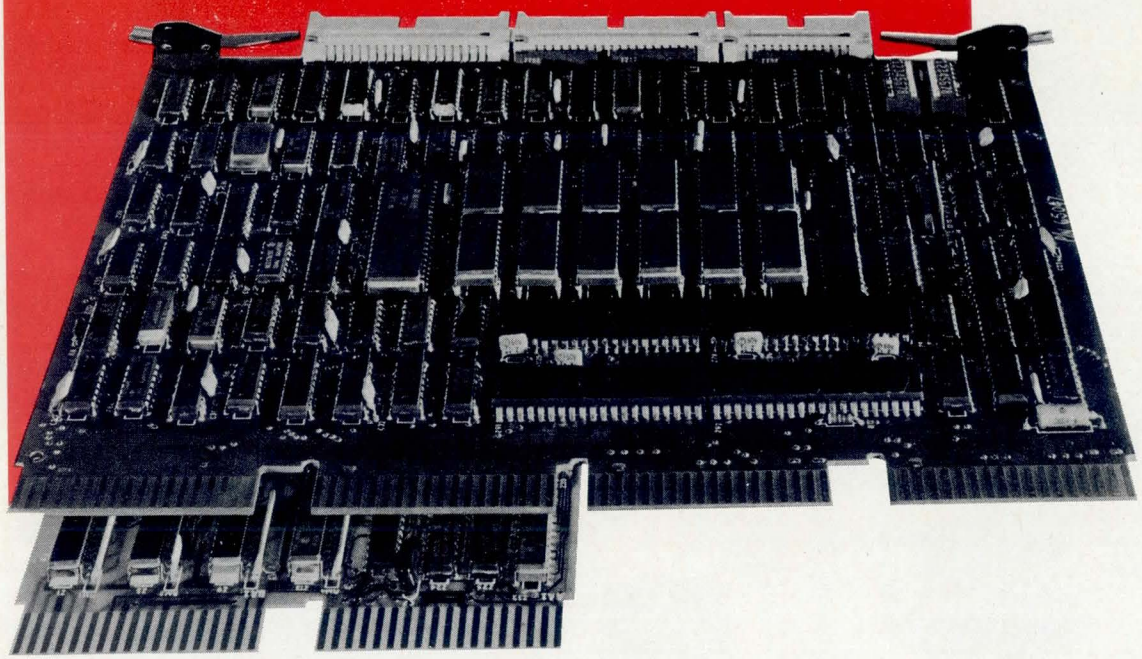

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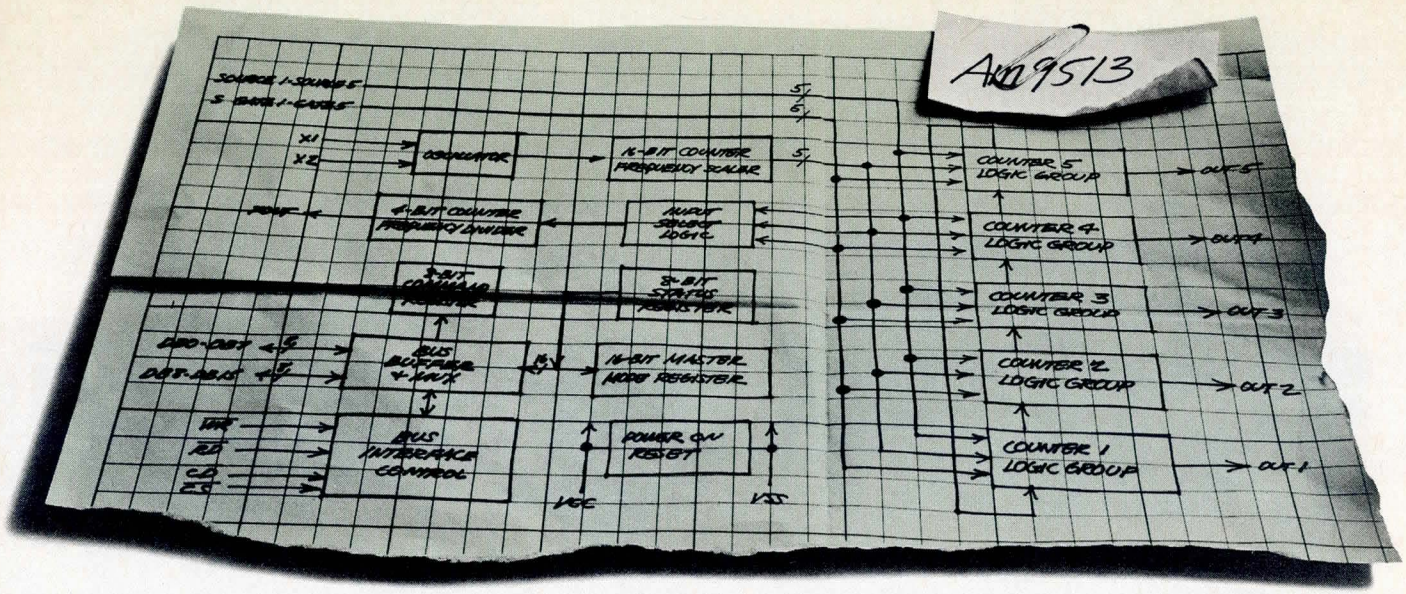

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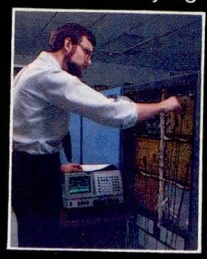

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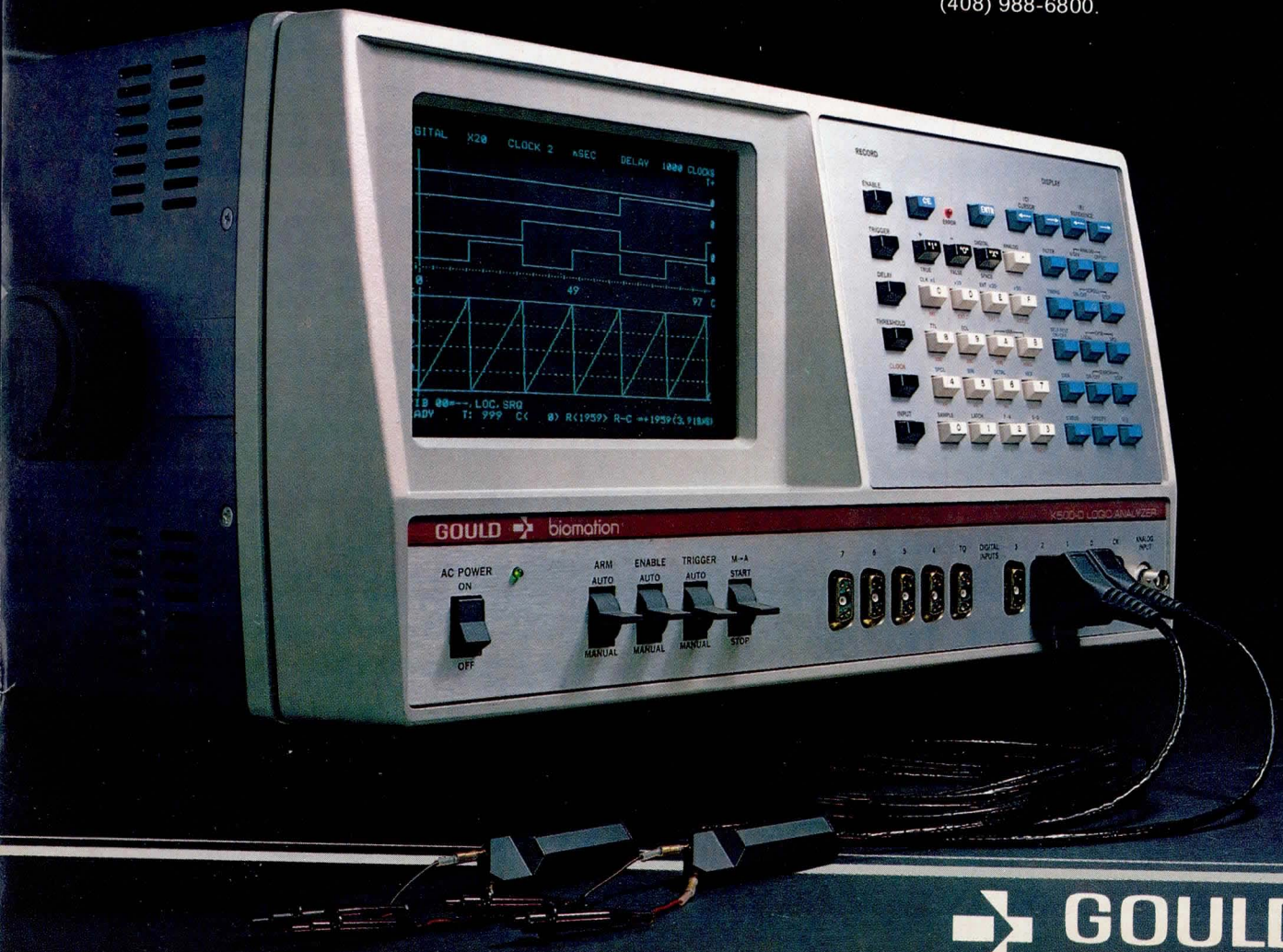

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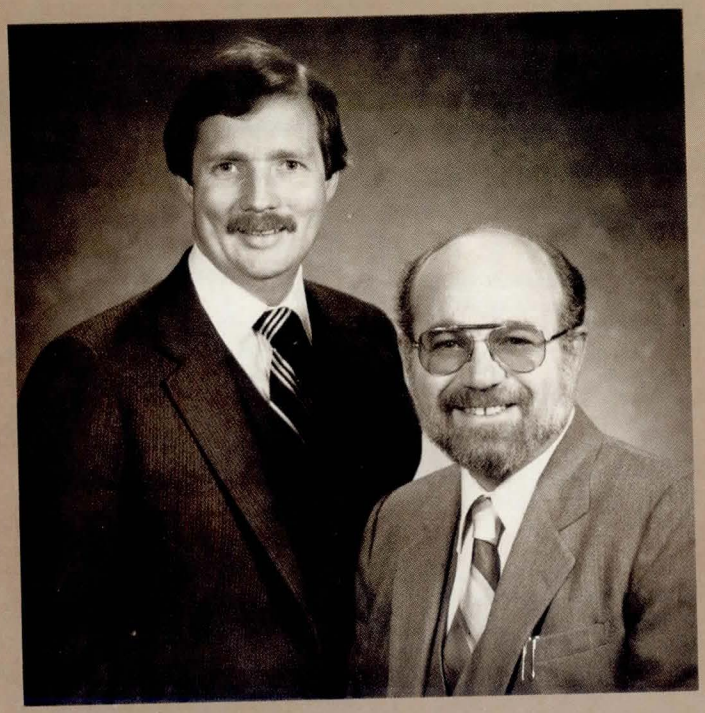

For many years there has been much discussion about the role of the systems designer and the directions being taken by the computer industry. At this time Computer Design *is renewing its commitment both to its readers and to the industry in a manner that counts: publication management and editorial direction from "real-time" industry managers. As newly appointed Publisher and Editor of* Computer Design, *we welcome your joining us in our commitment to the "real" computer industry.*

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CALENDAR

CONFERENCES

JUNE 1-4—Sym on Incremental Motion Control Systems and Devices, Hyatt Regency Hotel O'Hare, Rosemont, Ill. INFORMATION: Dr B. C. Kuo, PO Box 2772, Station A, Champaign, IL 61820. Tel: 217/356-1523 or 217/333-4341

JUNE 1-5—SNA But Not All IBM, New York, NY. INFORMATION: TCT Internat'l, 599 N Mathilda Ave, Sunnyvale, CA 94086. Tel: 408/735-9990

JUNE 8-10—CIPS (Canadian Information Processing Society) Conf, Waterloo, Ontario, Canada. INFORMATION: CIPS, 243 College St, Toronto, Ontario M5T 2Y1, Canada

JUNE 9-11—Data '81 Datacomm Conf and Exhibition, Winnipeg, Manitoba, Canada. INFORMATION: Laurie Whitsed, 55 Bloor St West, Toronto, Ontario M4W 3K2, Canada

JUNE 10-12—CONPAR '81 (Conf on Analyzing Problem-Classes and Programming for Parallel Computing), Nurnberg, West Germany. INFORMATION: Wolfgang Handler, Immd, Universitat Erlangen-Nurnberg, Martensstrasse 3, D-8520 Erlangen, West Germany

JUNE 14-18—Second Annual NCGA Conf, Baltimore Convention Ctr, Baltimore, Md. INFORMATION: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-1500

JUNE 23-25—COMDEX/Spring '81, Madison Square Garden and New York Statler Hilton, New York, NY. INFORMATION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

JUNE 29-July 1—Design Automation Conf, Opryland Hotel, Nashville, Tenn. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

JULY 21-22—Sym on Reliability in Distributed Software and Database Systems, Pittsburgh, Pa. INFORMATION: Marie S. Hreha, LRDC Bldg, U of Pittsburgh, Pittsburgh, PA 15260. Tel: 412/624-4908

AUG 3-7—ACM (Assoc for Computing Machinery) Siggraph '81, Dallas, Tex. INFORMATION: Dr Anthony Lucido, Intercomp, 1201 Dairy Ashford, Houston, TX 77079. Tel: 713/497-8400

AUG 11-14—Electronics '81, Mexico City, Mexico. INFORMATION: Franc D. Manzolillo, Proj Mgr, Rm 6015, U.S. Department of Commerce, Washington, DC 20230. Tel: 202/377-2991

AUG 18-21—VLSI (Very Large Scale Integration) '81 Internat'l Conf, University of Edinburgh, Edinburgh, Scotland. INFORMATION: Secretariat, VLSI '81 Internat'l Conf, 26 Albany St, Edinburgh EH1 3QH, Scotland

AUG 24-28—IFAC (Internat'l Federation for Automatic Control) World Congress, Kyoto, Japan. INFORMATION: IFAC '81 Secretariat, Kinki Hatsumei Ctr, 14 Kawahara-cho, Yoshida, Sakyo-ku, Kyoto 606, Japan

AUG 24-28—Internat'l Joint Conf on Artificial Intelligence, Vancouver, British Columbia, Canada. INFORMATION: Richard Rosenberg, Computer Science Dept, U of British Columbia, Vancouver, BC V6T 1W5, Canada. Tel: 604/228-3061

SEPT 14-18—COMPCON FALL '81, Capital Hilton Hotel, Washington, DC. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

SEPT 15-17—WESCON '81, Brooks Hall and Civic Auditorium, San Francisco, Calif. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

OCT 19-23—JEMIMA (Japan Electric Measuring Instruments Manufacturers' Assoc) Internat'l Exhibition, Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: 19th JEMIMA Internat'l Exhibition, Secretariat of the Administration Committee, 1-9-10, Toranomon, Minato-ku, Tokyo 105, Japan. Tel:03/502-0601, X4

SEMINARS

JUNE-JULY—Software Engineering, various cities and dates. INFORMATION: Renate Lammermann, Battelle Seminars and Studies Program, 4000 NE 41st St, Seattle, WA 98105. Tel: 206/525-3130

JUNE 1-2—Microprocessors: Hardware, Software, and Applications, Worcester Polytechnic Inst, Worcester, Mass. INFORMATION: Ginny Bazarian, Office of Continuing Education, Worcester Polytechnic Inst, Worcester, MA 01609. Tel: 617/753-1411, X517

JUNE 1-4—Pascal Programming Workshop; AND Ada: The Defense Department's New Standard Programming Language, various cities and dates. INFORMATION: Prof Donald D. French, Inst for Advanced Professional Studies, 1 Gateway Ctr, Newton, MA 02158. Tel: 617/964-1412

JUNE 8-11—ATE Seminar/Exhibit, Hynes Auditorium, Boston, Mass. INFORMATION: Test Conferences Registrar, Benwill Publishing Corp, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JUNE 9-11—Understanding and Using Computer Graphics, Chicago, Ill. INFORMATION: Bob Sanzo, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038. Tel: 212/233-1080

JUNE 22-23—Digital Electronics for Automation and Instrumentation; AND JUNE 24-27—Microcomputer Design Interfacing, Programming, and Application Using the Z80/8085/8080, Blacksburg, Va. INFORMATION: Dr Linda Leffel, CEC Virginia Polytechnic Inst and U, Blacksburg, VA 24061. Tel: 703/961-5241

AUG 15-17—Distributed Computer Control Systems, Beijing (Peking), China. INFORMATION: Prof Liu-Shi-hua, Chinese Assoc of Automation, Research Inst of Electronic Technic Application, PO Box 927, Beijing, China

AUG 31-SEPT 1—Real Time Programming, Kyoto, Japan. INFORMATION: 1981 IFAC/IFIP Workshop on Real Time Programming Org Committee, c/o Prof T. Hasegawa, Dept of Applied Mathematics and Physics, Faculty of Engineering, Kyoto University, Kyoto 606, Japan

SHORT COURSES

JULY 13-15—Data Communications, Fiber Optics, and Spread Spectrum Techniques; JULY 20-24—Mini- & Microcomputers: Their Structures, Characteristics, and Applications; AND JULY 27-31—Microcomputer System Design and Applications, Ann Arbor, Mich. INFORMATION: Viola E. Miller, Engineering Summer Confs, 200 Chrysler Ctr, N Campus, U of Mich, Ann Arbor, MI 48109. Tel: 313/764-8490

AUG 10—GPIB (General Purpose Interface Bus) Workshop, Sunnyvale, Calif. INFORMATION: Ben Catanzaro, Instructor, Intel Corp, MCSD Customer Training SV3-1, 1350 Bordeaux Dr, Sunnyvale, CA 94086. Tel: 408/734-8102, X375

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance.

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CIRCLE 9 ON INQUIRY CARD

Some environments for bubbles.

Intel introduces the iSBC 254™ Bubble Memory Board. The non-volatile Multibus™ memory system that goes where disks and tapes can't go. All in time for today's designs.

Bubbles store data in environments that bewitch storage devices such as disk and tape drives. That's because as solid-state devices, bubbles are unaffected by the heat of a factory floor, the roll of a ship or the dust of the desert wind. Since all that moves is information, bubbles aren't plagued with the wear and tear and related maintenance problems of electro-mechanical devices.

They're non-volatile, so you don't have to worry about battery back-up.

And because bubbles pack 1 million bits of data in an area less than 100 square centimeters, they can boost the performance of a portable data logger, as well as an in-house numerical control system.

Kindle your product development

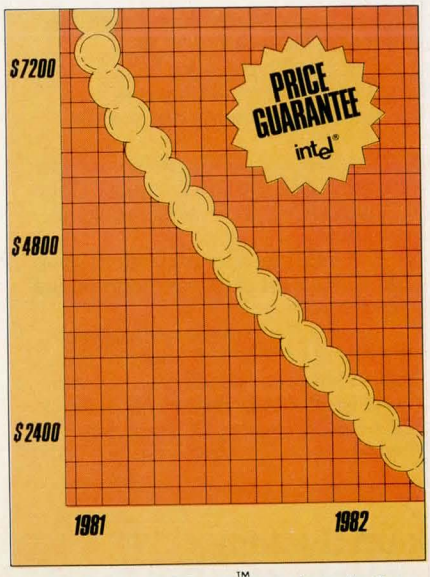
Now there's a fast, easy way for you to capture these advantages in your products: the iSBC 254 Bubble Memory Board. It puts from 128K to 512K bytes of Intel's 7110 bubble memory—complete with controller and support circuitry—on a 12 x 6.75-inch Multibus board. That's the same bubble memory and controller that's already storing data onboard ships and on factory floors. All pretested. And ready to run in your system today.

When you slip the iSBC 254 board into your Multibus-compatible chassis, it operates like any other microcomputer mass storage system. You choose from several I/O modes, including Direct Memory Access. You access data in a flash—several times faster than you can with a floppy. And move it at rates up to 50K bytes per second.

Add fuel to the fire

What's more, you can complement the performance of the iSBC 254 board in your system with any of a wide variety of Intel® Multibus boards

are a natural



Pricing for the iSBC 254™ board tracks the downward price curve of bubble memory components.

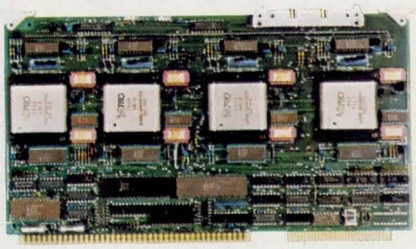
and software products available today. From 8- and 16-bit single-board computers, to analog and digital I/O, to real-time operating systems, complete with software drivers for bubble memory. Or if you want to configure your own board, you can start with Intel's Bubble Memory Prototype Kit (BPK72). It has everything you need to tailor Intel's 1-megabit bubble memory to your product.

Get the benefit of the continuous price reduction process

Like all of Intel's bubble memory products, the iSBC 254 board benefits from Intel's bubble memory price guarantee. By the end of 1981, the price of the 512K-byte board will be 34 percent lower than today's price on 100-quantity orders. After that, price reductions will continue tracking the downward spiral of bubble memory component pricing.

Put your competition on the back burner

The iSBC 254 bubble memory system is available off the shelf today. So you can start now to build the bubble's advantages into your systems. Reduced service and repair costs. Less preventive maintenance. Data integrity in hostile environments. And, as you do, you can open new frontiers. Ahead of your competition.



Find out more about how Intel bubble memory systems can help put you ahead. Contact your local Intel sales office/distributor. Or fill out the coupon below and send it to: Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call our toll-free hot line (800) 538-1876.

CD5

☐ I want to kindle my product development for bubbles. Have a sales representative call me with quantity price information on the iSBC 254 Bubble Memory Board.

☐ I want to find out more about bubble components and boards. Rush me a copy of the *Bubble Storage Data Catalog* by first class mail.

☐ I want to tailor bubble memory to my unique system configuration. Rush me information on the BPK72 Prototype Kit and the BPK70 Production Kit by first class mail.

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intel® delivers solutions

CIRCLE 11 ON INQUIRY CARD

Never Before Has A Back-up System Been As Intelligent As The System It's Backing Up.

This is 3M's HCD-75 High Capacity Data Cartridge Drive. And the reason it's as intelligent as a computer is because it thinks like one.

You see, unlike other back-up systems, the HCD-75 is interfaced directly with the primary system by means of sophisticated, microprocessor electronics. When the host computer has data to feed, the HCD-75 starts automatically. When the host computer stops, it does too. And since the HCD-75 also positions to any location, it not only saves tape cost, but retrieval time as well.

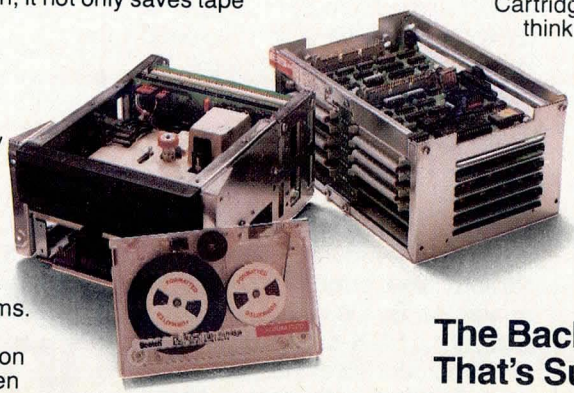
Of course, the use of microprocessors allows the HCD-75 to perform a number of other time-saving functions, too. Like block replacement, so you can easily correct errors or change files which need updating. And fast random access, which makes it useful both as an I-O device or as a storage unit for low-usage files. All of which relieves the host computer from difficult timing and formatting problems.

What's more, the HCD-75 features state-of-the-art error detection and correction capabilities. Even when the system is off-line, self-test diagnostic routines monitor its performance. And, combined with each of its $32.50 high-capacity cartridges, the HCD-75 provides a full 67 megabytes of formatted user information (144 mbytes unformatted). So costly operator interventions are sharply reduced.

If you're looking for a reliable, cost-effective solution to the problem of disk back-up, the HCD-75 High Capacity Data Cartridge Drive is the system you should be thinking about.

Not only has a lot of thinking gone into it. But a lot of thinking comes out of it, too.

For more information, check the listing on the next page for the representative nearest you. Or write: Data Products Division/3M, Bldg. 223-5E/3M Center, St. Paul, MN 55144.



The Back-up System That's Suddenly Way Out Front.

CIRCLE 12 ON INQUIRY CARD

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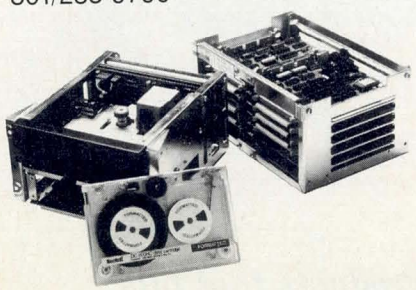


3M Hears You...

3M

LETTERS TO THE EDITOR

To the Editor:

Kalman Rozsa's Tech Note, "n-Dimensional Interrupt Handler Replaces Priority Encoder" (Feb 1981, pp 126-134), suggests building a special box to go between a microprocessor and the devices that may wish to generate interrupts, in order to resolve problems of concurrency and interrupt priority.... I suggest a simpler solution, which requires a small amount of synchronization logic on each device interface:

(1) Each device in the system has an "INT PENDING" latch, which is typically triggered by an event and cleared by the program.

(2) Each device has a "REQUEST INHIBIT" latch, which is set and cleared only under program control.

(3) Each device recognizes a "PRI IN" signal and generates a "PRI OUT" signal, which it passes to the next device on the bus.

(4) When INT PENDING is false, or REQUEST INHIBIT is true, PRI IN is passed unchanged to the next device as PRI OUT.

(5) When INT PENDING is true and REQUEST INHIBIT is false, PRI OUT is passed as false to the next device.

(6) The system generates REQUEST ENABLE when it can accept an interrupt. Any device (there will be at most one), which sees PRI IN as true, REQUEST INHIBIT as false, and whose INT PENDING latch is set, identifies itself to the processor and begins the interrupt sequence.

In this scheme, priority among un-INHIBITED devices is determined by physical location on the bus, but use of the INHIBIT masks allows software to reprioritize the system easily. Mr Rozsa's scheme allows a device to generate a second interrupt before the first is processed; in the proposed method, each device interface would be responsible for enqueuing multiple requests, should they occur.

Dennis Weeks
Data General
Bellevue, Wash

To the Editor:

After reading the correction in Ronny Horn's letter (Oct 1980, p 13) of the AOS program in "Integer Base Conversion on Handheld Programmable Calculators" (May 1980, pp 202-207), I edited it and found the same type of errors again.

When 12_{10} was converted to base 12, the answer was 9.999999996. For the correct answer, 10, one must reduce the proposed truncation of the three guard digits to one. The initial program is edited as follows: GTO 36, LRN, 13 times 2nd INS, X, 1, 0, 0, =, EE, INV, EE, ÷, 1, 0, 0, =, LRN. In spite of these changes, Ronny Horn's example remains correct too.

Andras Varga
Institute for Telecommunication Electronics
Technical University of Budapest
Budapest, Hungary

To the Editor:

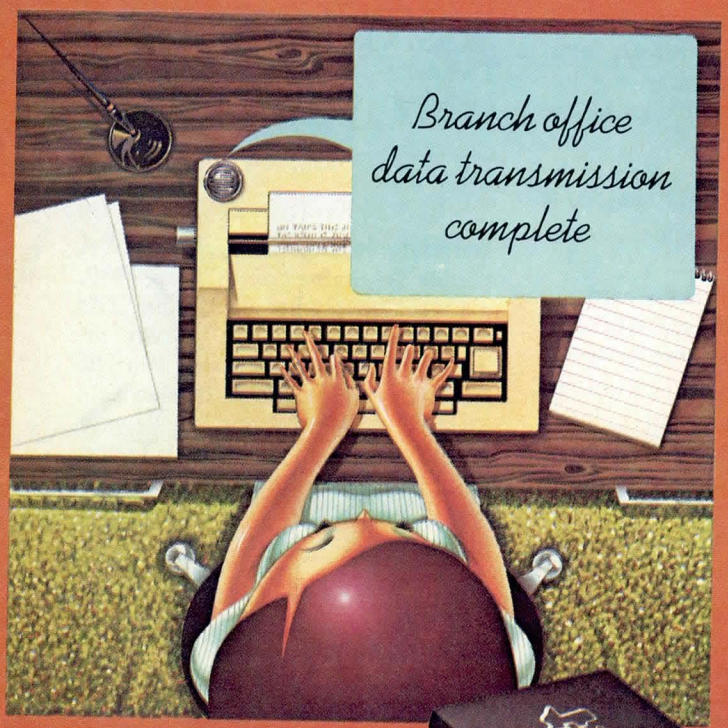
With reference to the Tech Brief "A Simple Tri-Stable Latch" (Aug 1980, p 134), I have a genuine doubt. The timing waveforms are drawn indicating that the circuit can be clocked at a 1-μs rate. The slew rate of the μ A741 is about 0.5 V/μs at $\pm$15-V supplies. Hence, the fastest input transition rate can in no case be less than about 2(2.4/0.5) μs, or 9.6 μs.

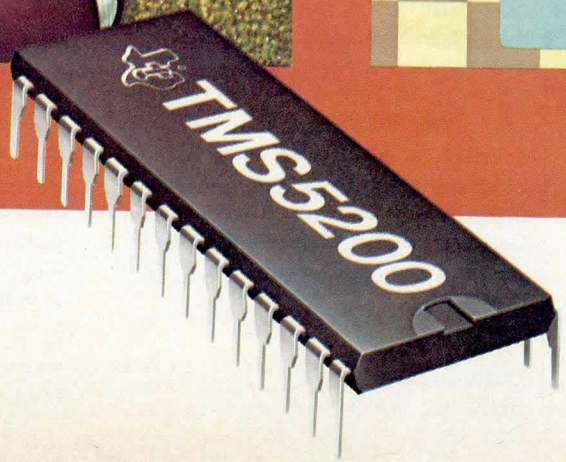
C. H. Sakharwade
TIFR
Bombay, India

The Author Replies:

The circuit can be clocked at a 10-μs rate, and not at a 1-μs rate as shown in the timing waveforms. For the clock rate of 1 μs, an FET input op amp 536 can be used in place of a 741. Also, by using a high slew rate op amp 531, the circuit can be clocked at a much higher rate than 1 MHz.

D. S. Jain
NRSA
Hyderabad, India





Products that talk.
The man-machine interface will never be the same.

Let's talk about speech capability. Voice synthesis products. From Texas Instruments.

The bright promise of products that think came closer to fulfillment in the 70s. The trend for the 80s is clear: Products that "talk."

Whether it's appliances, automotive consoles, transaction terminals, office systems, telecommunications, robotics or electronic toys and games, no other area of technology will have more impact during this decade.

Speech synthesis technology — pioneered by TI — portends a whole new generation of voice-prompting products. Products that will change the way you live and learn and work.

So, if you're designing new products with speech applications, talk to TI — the *only* total capability supplier with the experience and production-proven know-how to assure you of reliable speech products and services.

Let's talk technology

TI offers several methods of vocabulary analysis, dependent on your volume, versatility of application and voice quality desired. TI's Linear Predictive Coding (LPC) technique provides the highest quality speech reproduction because it's the only technique devised that models itself after the human vocal tract.

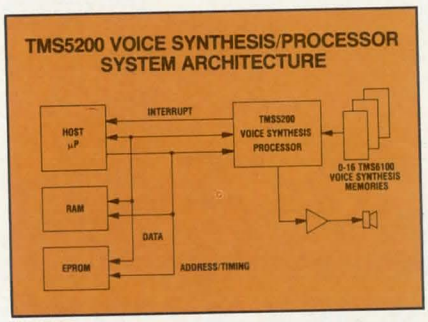
Define your vocabulary, consider your volume requirements, cost and development time, then talk to TI about your application.

Let's talk products

Choose from the industry's broadest, most cost-effective line of speech products. A growing line of integrated circuits, evaluation kits, OEM boards and a capability for the design and development of complete custom modules incorporating microprocessors, display and interface functions. A good example of our commitment to this technology: ROMs made especially for speech applications.

TI's LSI Voice Synthesis processors (VSP) and Voice Synthesis memories (VSM) are in volume production, now.

The TMS5200 single chip VSP produces high quality speech at a very low data rate (1200 bps), easily interfacing with 8 and 16-bit microprocessors. The on-chip FIFO buffer allows speech data to be stored in either the host microprocessor system, or off-line on bubble memory or floppy disk. Also, speech data may be stored in a custom ROM, such as the 128K-bit TMS6100. You can use TI VSPs with TMS6100 Series VSMs for storage of up to 3,000 words of speech.



The TMS5100 single chip VSP produces high-quality speech at data rates of 1200 bps and interfaces with 4-bit microprocessors. TMS5100 VSP directly addresses up to 16 TMS6100 VS memories for up to 30 minutes of speech.

For evaluation of TI's voice synthesis capabilities for 4, 8 and 16-bit microprocessors, complete speech evaluation kits are available for TMS5100 and TMS5200.

So, what are we talking about? We're talking about quality, flexibility, cost/performance effectiveness and right now delivery — only from the voice synthesis leader — only from Texas Instruments.

There's more. We're also talking about custom modules and boards. Like the TM990/306 speech module without standard vocabulary for applications using customer-specified words and shipped without EPROMs, allowing users to install Solid State Speech* vocabularies developed specifically for their own applications.

For high-volume applications, user-developed vocabularies can be implemented on mask-programmed ROMs.

The benefits of the custom module approach are both time and cost related. TI's experience in the design and production of electronic modules means quick cycle times, substantial savings, and, of course, getting your product to market faster.

Let's talk support

Like the development of production vocabularies at any of TI's Regional Technology Centers. Custom vocabularies can be synthesized at the RTCs at low cost with quick turnaround (so quick in some cases that you can walk out the door with your program) and delivered on EPROMs for use with either TI's TM990/306 speech board or TMS5000 Series VS processors.

And like tapping the resources of TI's word library where natural sounding speech is pre-recorded and readily available for specialized vocabularies.

And like an intensive one-day RTC seminar covering TI's Solid State Speech technology and its applications, including acoustics, phonetics, waveform analysis and LPC. Systems architectures as well as hardware and software design techniques and a demonstration of several speech products round out the day.

And like the Design Service assistance rendered by the RTCs for the application of cost-effective, state-of-the-art technologies to your specific product and program needs.

Let's talk now

About a total systems solution capability for voice synthesis technology. About low-cost, high-quality, quick turnaround Solid State Speech applications for your products.

Talk to your nearest TI field sales office, or write to Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265.

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TEXAS INSTRUMENTS
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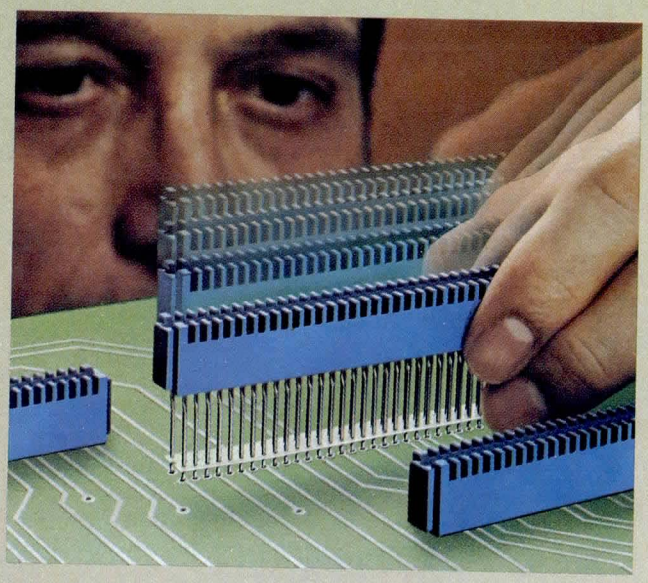
CIRCLE 13 ON INQUIRY CARD

Insert this preassembled card edge connector in one step, and forget it.



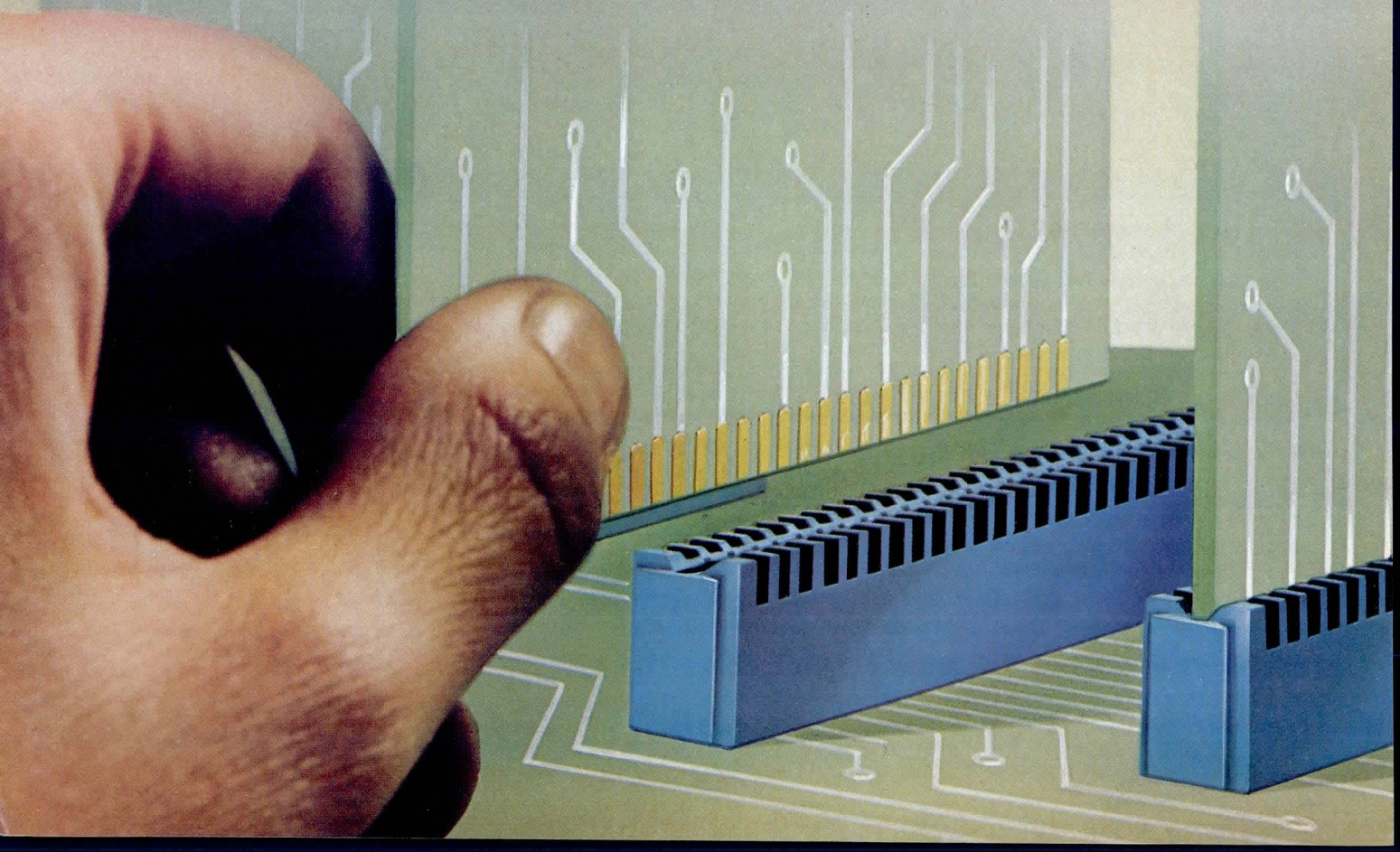
Preassembled to cut backplane production time. Designed for mother board insertion without damage to plated-through holes.

The one-step AMP PACE Connector does a lot to make your production simpler—and free from worry.

Using our unique ACTION PIN contact compliant design, just press the connector into place. Assembly is complete. There's no solder or costly, time-wasting rejects.

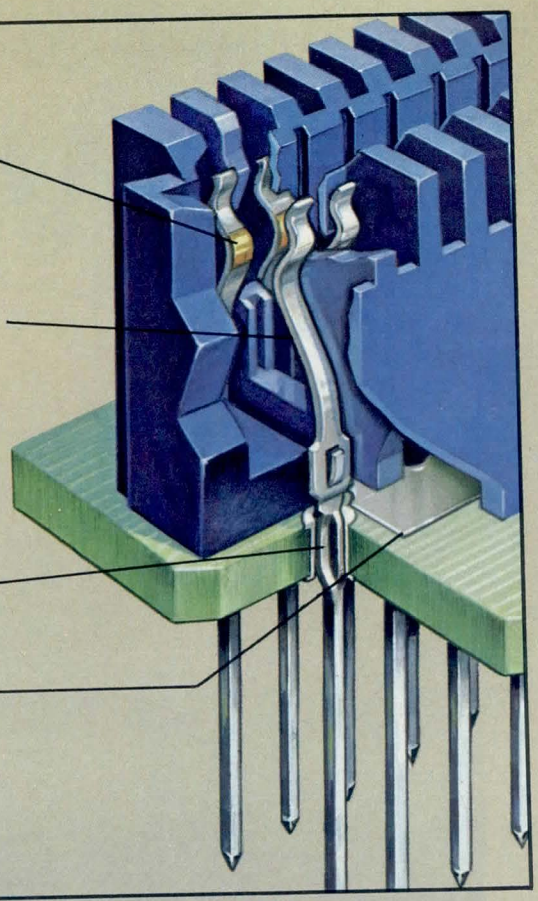
Even our Accu-plate precision plating avoids waste. By pinpointing gold only on the final contact area and using nickel and tin elsewhere, you don't pay for what you don't need.

The AMP PACE Connector. It's good enough to forget.



AMP Facts

Description: preassembled card edge connectors for .100" x .100," .100" x .200," and .125" x .250" centerlines; size 15 to 61, dual position.
Contact Rating: 3 Amp
Contact Resistance: Spring contact to test board—8 milliohms
Total circuit resistance—9 milliohms
Operating Temperature: —55°C to +85°C
Voltage Rating (Sea Level): .100" centerline spacing—1000 VAC
Insulation Resistance: 5,000 Megohms
Durability: 100 cycles
Salt Spray: MIL-STD-1344, Method 1001
Thermal Shock: MIL-STD-1344, Method 1003
Physical Shock: MIL-STD-1344, Method 2004
Humidity: MIL-STD-1344, Method 1002, Type II
Vibration: MIL-STD-1344, Method 2005



For more information, call the AMP PACE Connector Desk at (717) 780-8400.
AMP Incorporated, Harrisburg, PA 17105.
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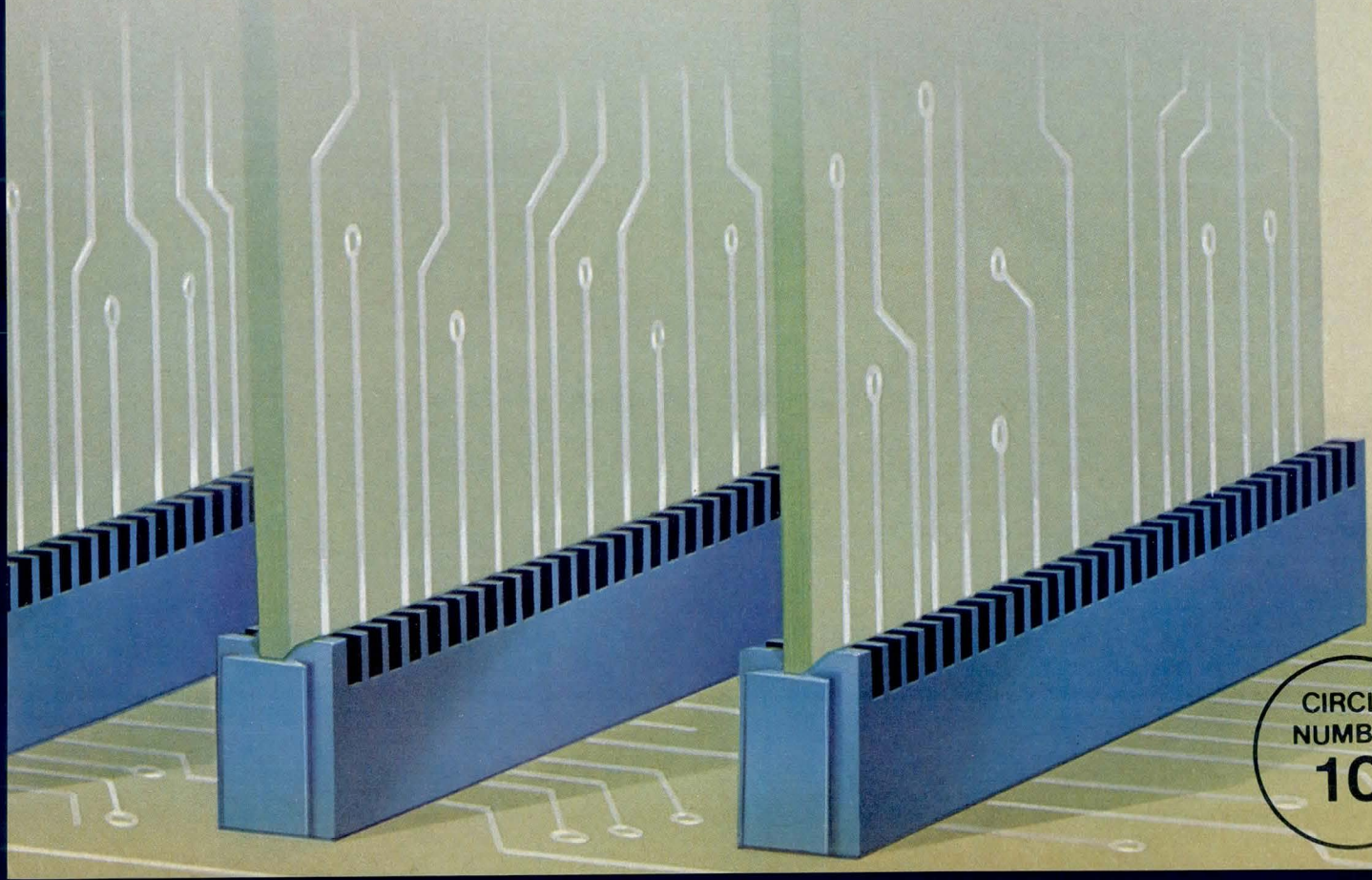
AMP means productivity.



CIRCLE NUMBER 10

Now: 45ns -

45ns

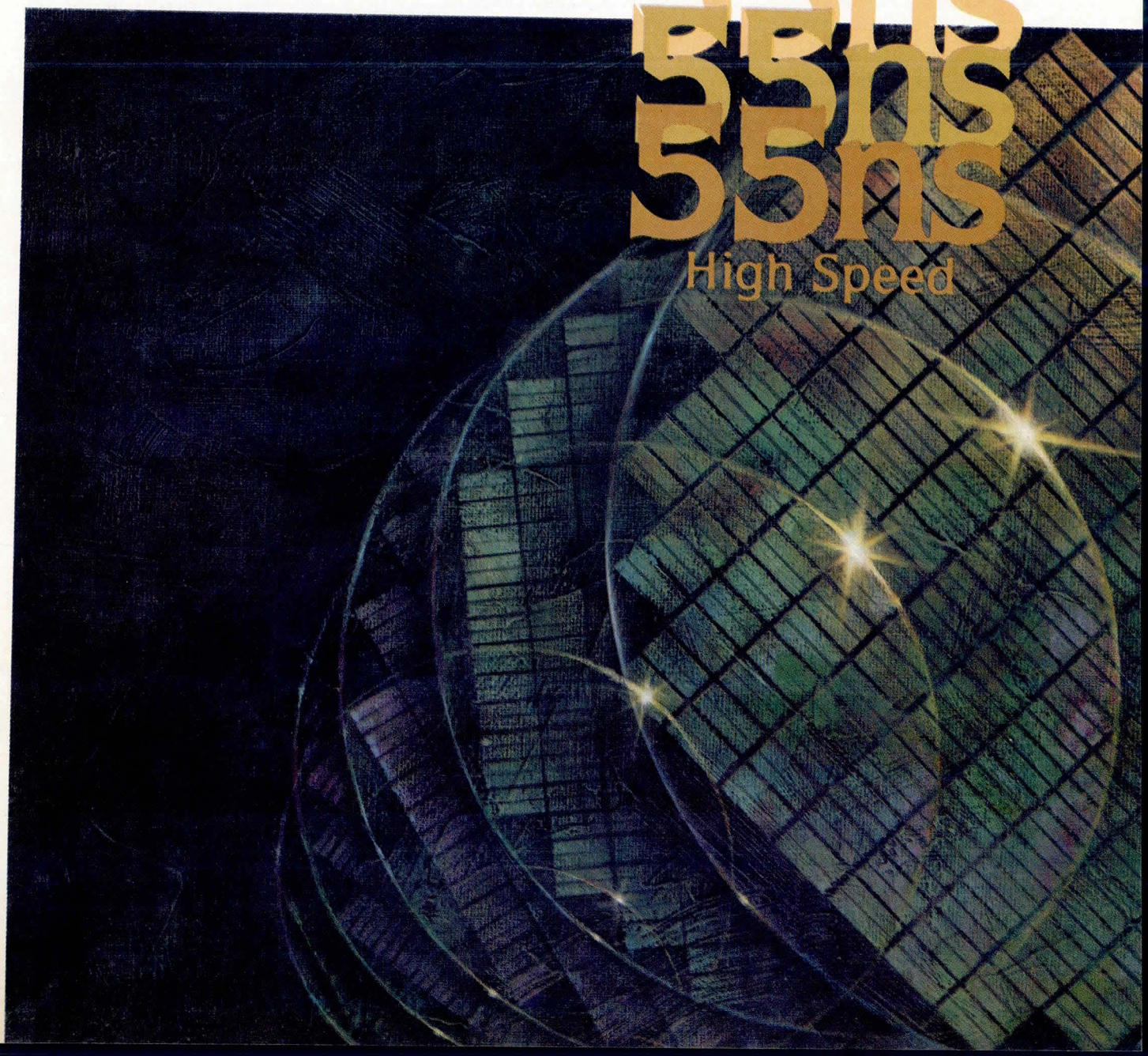
45ns

45ns

55ns

55ns

High Speed



-660mW

The INMOS IMS1400 16K static RAM sets another new standard.

Once again, the INMOS commitment to leadership in advanced VLSI technology has resulted in new performance levels for the IMS1400 16K x 1 static RAM.

The new IMS1400-45 offers the exceptionally fast chip enable access time of 45ns, with address access and cycle times of 40ns. Surprisingly enough, it consumes no more power than its 55ns companion. That's less than 660mW of active power and 120mW of standby power, using just a single 5V (±10%) power supply. And, like the IMS1400-55, it's TTL compatible and is packaged in a 20 pin, 300 mil ceramic DIP with industry standard pinout.

Both the IMS1400-45 and the IMS1400-55 deliver the performance you'd expect from a VLSI leader. And what's more, they're available now. For full information on the new standard of static RAMs, call or write INMOS today.

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1/2

CIRCLE 14 ON INQUIRY CARD

Contemporary Multiplexing Techniques—Part 1: Review and Characteristics

James F. Kearney

Timeplex, Incorporated
One Communications Plaza, Rochelle Park, NJ 07662

A multiplexer, primarily, puts several discrete channels of data onto a single high speed data link in order to substantially reduce the number, and thereby the cost, of data lines in a communications network. However, in the hands of the imaginative communication system designer, today's more sophisticated multiplexers can accomplish much more than that basic function. They can provide error free transmission. They afford considerably larger and more secure buffering power. They incorporate diagnostics that allow users to service their own systems and can also provide central control over the entire network. They can add flexibility to existing systems that will accommodate both planned and unforeseen future system changes.

An analysis of contemporary multiplexer design features will help the network designer to know what is available. However, his most important input will come from a thorough analysis of his own organizational requirements.

Basic Types of Multiplexers

All multiplexers allow simultaneous service of a number of terminals via a single high speed data communication line. Three basic types exist: frequency division, time division, and statistical. The frequency division multiplexer (FDM) divides the data link frequency band into several smaller bands, each of which carries a channel of data (Fig 1). FDM was the first technique to be used in multiplexing and took advantage of techniques and equipment used in radio, where frequency manipulation is common. However, FDM is quite inefficient when compared with the later technique of time division multiplexing, where the transmission path can be divided much more precisely.

The time division multiplexer (TDM) allocates time slots to channels on a dedicated basis (Fig 2). The overall time criterion is established by the speed of the high speed transmission line. Once that is determined, there is essentially a one to one translation, a matter of dividing up that aggregate transmission band into its component parts. Starting with a 2400-bit/s aggregate path, it can be divided into 48 50-bit/s channels, 32 75-bit/s channels, 24 100-bit/s channels, and so on.

As a practical matter, this straightforward approach must be modified somewhat by the need for synchronization, using unique bit patterns to lock the local multiplexers to the remote demultiplexers. Synchronizing information is very important, and will occupy certain portions of the bandwidth on the aggregate channel. Design of the multiplexer should accommodate synchronizing signals that cannot be easily simulated by the data patterns that are transmitted along with them. They should also be of such a nature that the amount of time stolen from pure data transmission is minimized.

TDM techniques are traditionally one of two types, bit- or character-interleaved, depending on whether each time slot within the transmission frame is devoted to a bit or to a character. Fast turnaround is the advantage of bit interleaving. It is not necessary to transmit and receive entire character sequences before the remote end can take action. Fast turnaround is most useful in public networks such as telex, where there is a certain amount of call setup signaling before actual data transmission, where quick give and take is desirable. On the other hand, character interleave techniques tend to be more flexible.

The statistical multiplexer (stat mux) is more efficient than a TDM because it allots time slots only for channels that are actively transmitting (Fig 3). It can support a number of terminals whose combined bit rates add up to more than the bit rate of the aggregate high speed line. Each frame of data carries a special header to identify the active channels. The stat mux is the most advanced type of multiplexer currently available and is the device of choice for most contemporary network designs. It will be the subject of most of this discussion.

(continued on page 26)

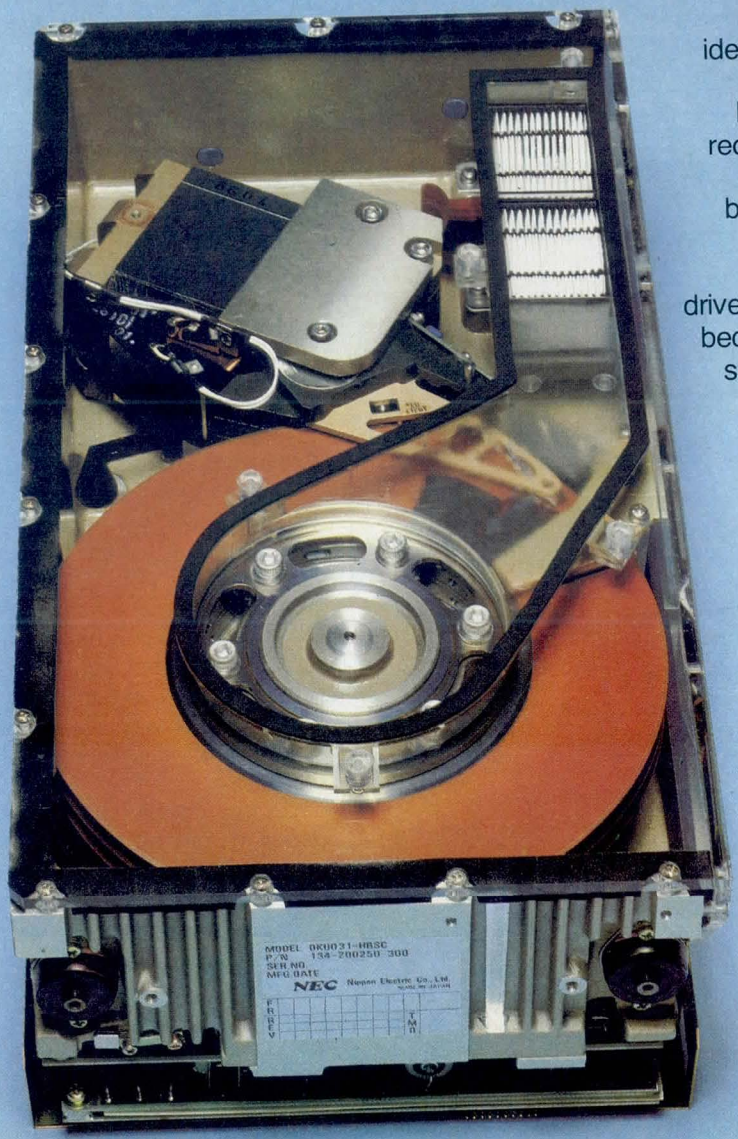
NEC introduces 8-Inch Winchesters.

With more capacity. Faster access. And the reliability you'd expect from NEC.

Once again, NEC leapfrogs conventional technology with its new D2200 family of eight-inch Winchester disk drives.

The first models in the series deliver 30-millisecond access time with capacities of 25.5 and 42.5 megabytes, respectively, and use conventional storage module device (SMD-type) controllers for convenient interfacing and formatting.

Sealed-disk Winchester technology is enhanced with voice-coil actuators, direct-coupled DC spindle motors and closed-loop air circulation which reduces parts count, eliminates periodic maintenance and gives the D2200 Series an MTBF in excess of 10,000 hours. When service is required, it's fast: the D2200s have a 30-minute MTTR.



The D2200 family is ideally suited to medium and heavy volume interactive business applications that require frequent disk access, as in virtual memory, database access and data communications operations.

Eight-inch Winchester drives are increasingly popular because they offer significant savings in installation, packaging, maintenance and cost-of-ownership.

And once again, NEC technology adds an extra dimension. Call your NEC Information Systems representative for more information.

NEC

NEC Information Systems, Inc.

Home Office: 5 Militia Drive, Lexington, MA 02173, (617) 862-3120
Eastern Office: 36 Washington Street, Wellesley, MA 02181, (617) 431-1140
Central Office: 551C Tollgate Road, Elgin, IL 60120, (312) 931-1850
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CIRCLE 15 ON INQUIRY CARD

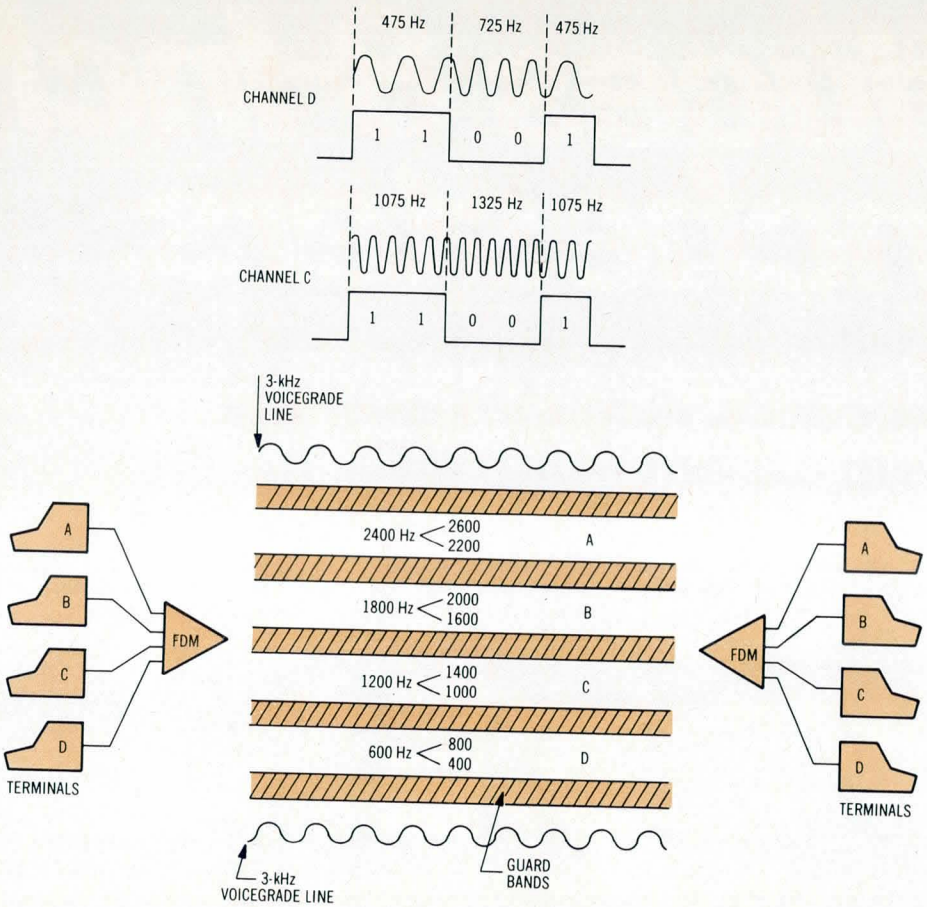

Fig 1 Frequency division multiplexing. On one channel, "1" bit may be transmitted at 475 Hz and "0" bit at 725 Hz. On next channel, "1" would be transmitted at 1075 Hz and "0" at 1325 Hz, and so on. Division depends on desired frequency of transmission, eg, 75-bit/s channel requires less spectrum space than 150-bit/s channel

Multiplexer Design Considerations

There are two main sections in the design of a multiplexer. The low speed section deals with the individual channel ends of the system where data rates are usually lower than that of the aggregate high speed link. This section must periodically scan the channels, sense and accumulate the data presented on each, and store the data in some digital storage medium. The high speed section assembles characters and presents them to the aggregate interface for transmission.

Traditional TDM design approaches use a variety of shift register techniques for memory and counting functions, maximizing the common control while minimizing the input/output (I/O) interface. By maximizing the common control, and sharing to a greater extent a common set of logic to respond to the stimuli of input and output, less hardware is needed for each channel to respond to these stimuli, and the less expensive the unit. "Expensive" in this context means both the dollar cost and the cost in loss of unit capability.

In today's marketplace, however, with the advent of microprocessors and statistical multiplexing, these old design techniques have been found to be more expensive than to apply more distributed processing techniques in the I/O channels. Using microprocessors, which have dropped considerably in cost, and distributing their processing power among a number of I/O units, the stat mux reduces hardware costs and increases capability and speed. As a result, the traditional combination of main common control and unintelligent interface modules is slowly being replaced by inexpensive microprocessors and distributed microprocessing techniques, gaining speed, flexibility of design, and flexibility of interfacing to the network.

Contemporary stat muxes, such as the Timeplex Series II MICROPLEXER, use universal synchronous/asynchronous receiver/transmitters (USARTs) on the low speed or channel side for serial to parallel and parallel to serial conversion. The microprocessor boards are controlled by CPU chips, enhancing their processing capabilities. Programmable read only memory (P/ROM) chips are used for storage of multiplexer control parameters, and random access memory (RAM) chips are used as data buffers. A chip that will promote an advanced data link controller (ADLC) X.25 is likely to be used as the interface circuit for the data link on the high speed side.

(continued on page 28)

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CIRCLE 16 ON INQUIRY CARD

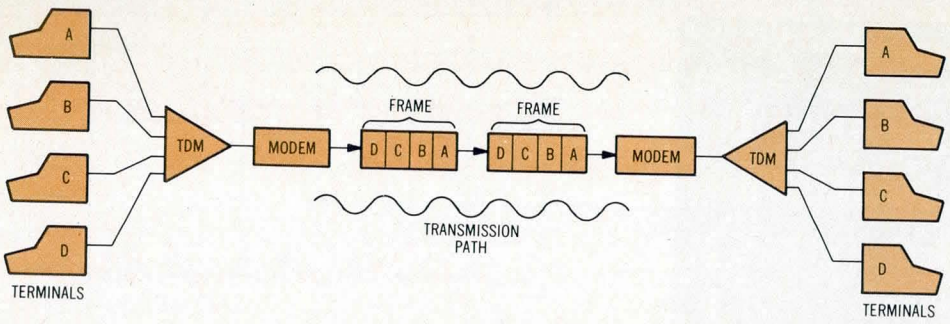

Fig 2 Time division multiplexing. Time slots are allotted to channels on dedicated basis whether or not "live" data are being carried. At any given time, majority of slots may not carry useful data but contain fill characters

Data enter this high speed link from the aggregate line and then go into the RAM buffers. The CPU handles transitions from the buffers out to the data channels, and the USART clocks the data out to the individual channels. In the reverse direction, with the data coming from the channels into the multiplexer on the way to the high speed data link, the USARTs accept the character as it comes in and pass it on through high speed buses into the buffer areas.

All stat muxes have a USART-type function handled on individual channels. All have one or more CPUs as master controllers to handle the data functions. The data are handled through the processors and sent to buffers where they are held until the high speed line indicates it needs the data. The master controller pulls the data out of the buffer and puts them on the high speed line. During this process a copy is made, has an identification number assigned to it, and is held in the buffer. When the system gets an acknowledgment (ACK) that the character was correctly received, the copy in the buffer is erased. A negative acknowledgment (NAK) causes the multiplexer to use the buffered copy to resend the data.

Where a TDM uses hardware for direct address on a one to one basis, the stat mux has no such firm relationship; all link assignments are dynamically allocated and are up for allotment on the basis of need. The information is transmitted as a data package that has been assembled by the multiplexer. The package, a data block, also carries extra information bits that involve control fields. The block must have a destination address or the address of the channel from which the data were accumulated, and it carries block check characters, most commonly cyclic redundancy checks (CRCs).

Using Multiplexers in Designing a Network

When the network designer understands the kinds of data communications inefficiencies that the multiplexer designer was trying to resolve, optimum use of stat muxes will be achieved. In bandwidth allocation in a TDM, a combination of terminals with baud rates of 150, 300, 1200, or greater can be put over a single high speed 9600-bit/s line, provided the aggregate sum of the speeds of the terminals is less than or equal to the speed of the aggregate line. In addition, some of the bandwidth must be reserved for control signals.

In the early stages of the asynchronous environment, data passed over the line in a character by character mode. The operator typed an "A" and it was passed on to the mainframe without buffering. Experience revealed that 1200-baud terminals,

(continued on page 30)

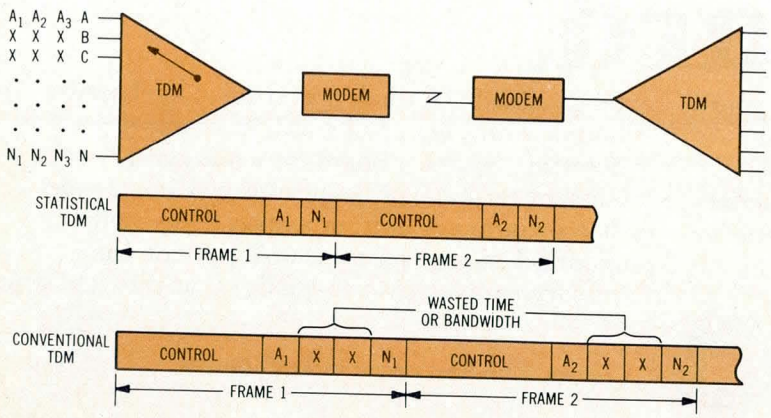

Fig 3 Statistical multiplexing vs conventional TDM. In TDM, efficiency suffers because dedicated time slots are not available to other terminals. In stat mux, which services only active terminals, more terminals may be attached. Buffer memory assembles data and is usually sufficient to store channel characters if traffic temporarily exceeds multiplexer's data link rate. Data may also be stored briefly for possible retransmission if errors are detected

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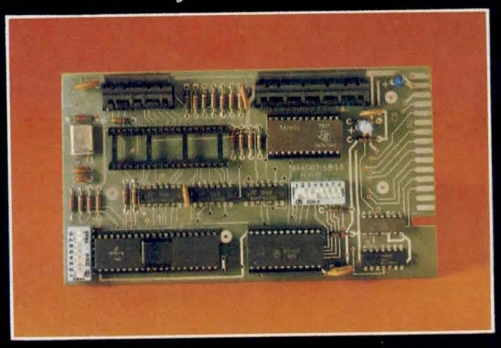

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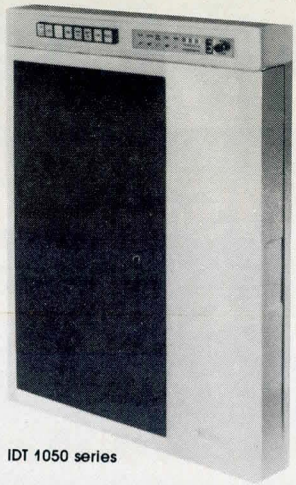

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INNOVATIVE DATA TECHNOLOGY

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capable of transmitting 120 char/s, were sending only 5 char/s because that was as much as the operator was typing. This left a lot of room for improvement.

The theory of the stat mux, then, is to scan associated data ports and assign bandwidth to channels only when they interrupt the system with data. Data primarily come in on a character mode basis and the standard USART interface receives the character. Upon receiving that character, an interrupt is raised; when the scanner comes by it sees the interrupt, picks up the character, and passes it on to a buffer and a processor. Data are then assembled and transmitted over the high speed link. With the main processor in the stat mux sampling and controlling the data it receives from the individual channels, it is possible to place more channels onto the system. Many terminals can be placed on a stat mux—for terminals operated in manual mode, probably twice as many over a 4800-bit/s line as was possible using a 9600-bit/s line—thus significantly reducing modem costs.

Adding block terminal modes into the system creates another dimension. These terminals have their own buffers; an operator keys in a given amount of data and hits a specified function key that sends the data as a block. Here, instead of sending 5 char/s, it is possible to send perhaps 500 char/s or even more, in full screen transmission mode. Inefficiencies are still built into the system because no two operators are going to key alike. Not all operators on all of the terminals feeding the line are going to enter all of their blocks at one time, so there is still room for the processor to get the data out over the high speed line in a reasonable amount of time—probably still with a response time that is acceptable to the end user.

When synchronous data are thrown into the stat mux a problem arises. This is because the system is constantly being polled, meaning that data are always going out on the lines. Whether the data consist of poll messages or live information, it is a condition that interrupts the processor and has to be handled.

A mistake is sometimes made in trying to compare the efficiencies that exist on a point to point arrangement, where there is no interference from other terminals, to a statistical multiplexing environment where four or five 4800-bit/s data channels come onto a composite 9600-bit/s data link. The responses are very fast on the point to point arrangement. However, in statistical multiplexing the response time will be reduced by the large amount of data that can be presented to the system at any one time, plus the overhead of stat muxing.

In a synchronous environment there is a more efficient way to present data to the system than the method generally used, where the user constantly

(continued on page 32)

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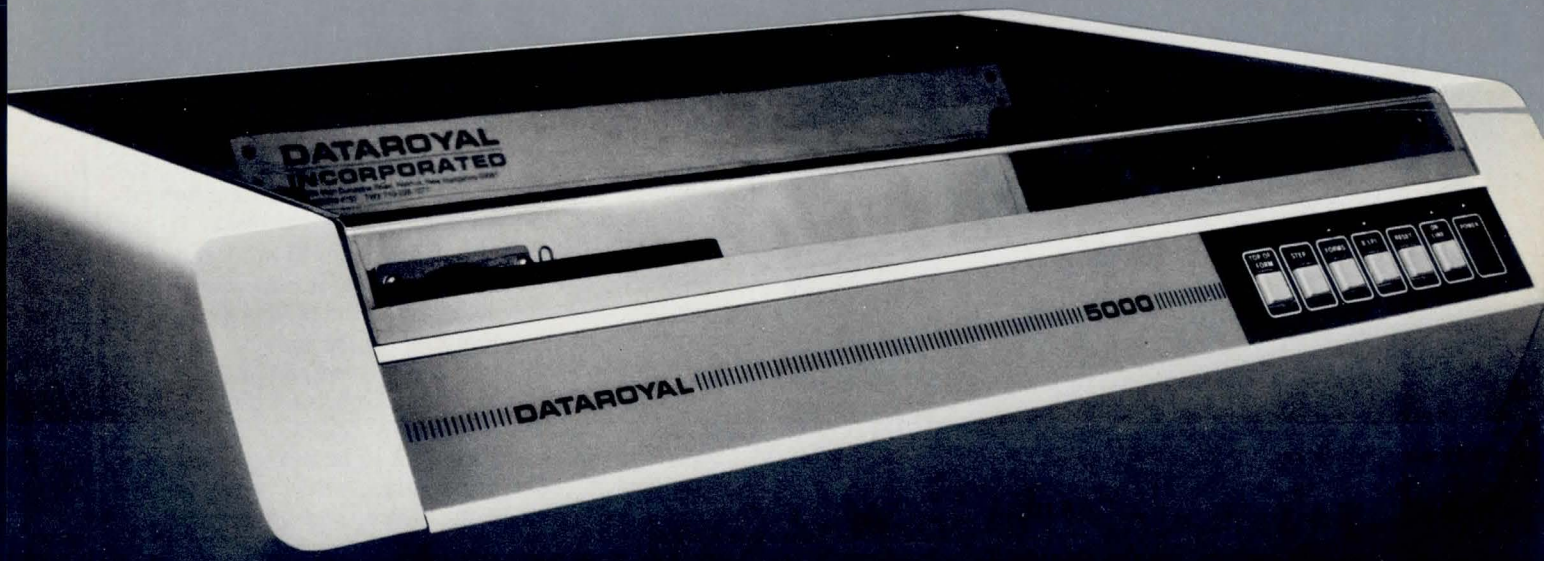

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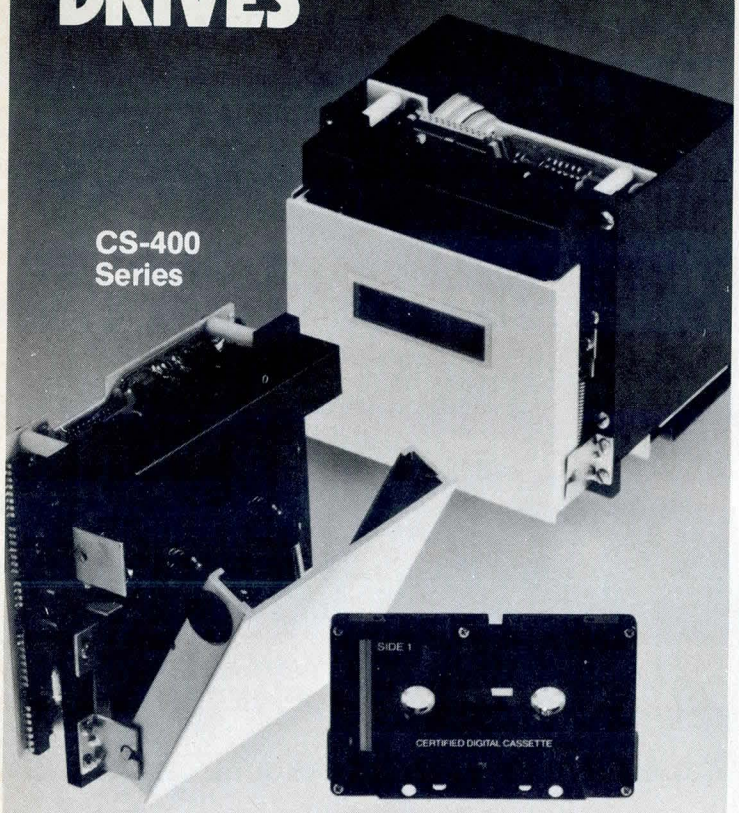

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transmits a full screen of 1920 characters, that in itself exceeds the 1-s capacity of a 9600-bit/s line. Consequently, on a one to one basis, there will be a delay. The more efficient way is to use preformatted screens. Here the original menu is presented to the CRT, and only the live or variable data are transmitted back to the host. This reduces the input dramatically to 150 or 300 characters. Both the multiplexer and the mainframe processor are now afforded more time to handle additional tasks.

As can be seen, stat muxing leads to more than setting up a point to point network. It puts intelligence into the system. It analytically interprets the traffic and the interrupts coming into the system, and proportionately and dynamically assigns them bandwidth on the high speed line. To be sure that it is efficient, the vendor and others designing the system must know how the data are to be introduced to the multiplexer, what takes place when the terminal enters the data to be processed, and how long those data are to be processed at the mainframe before being transmitted back to the terminal.

Overheads can be compounded within the mainframe unless proper procedures and implementation are worked out, the reason why stat muxing has recently tended toward enhancement packages. These features inform the user not only of internal buffer utilization but also of how much of the channel is being used. They help him plan not only the number of terminals to add to a particular controller on a given line, but also the number of additional lines to place on the front end. By knowing what are the current response times the user can determine what overhead is on the mainframe and communications. This provides a basis for establishing a threshold, a peak of utilization that can be used as a guideline before he must consider such operational changes as altering file structures, upgrading software, or acquiring additional communications facilities. It now becomes imperative to know the capabilities of the multiplexer for solving present and future problems.

The concluding column will discuss problems associated with emulation systems, buffering, clocking, traffic control, network configuration, and response time.

Please rate the value of this article by circling the appropriate number in the "Comments" box on the Inquiry Card.

High 719 **Average 720** **Low 721**

fiber optic modem for local data distribution

multiplexes control signals along with the data

Fiber optic modems are ideally suited for many local data distribution applications since they offer several inherent advantages over conventional hard-wired systems. These include immunity from rf and magnetic signals, increased bandwidth, and a significant improvement in the security of the data link.

Versitron's FOM-5 fiber optic modem (one of a family of fiber optic modems) not only provides the basic advantage of fiber optics, but also offers several unique system operating features that makes it ideal for local data distribution applications.

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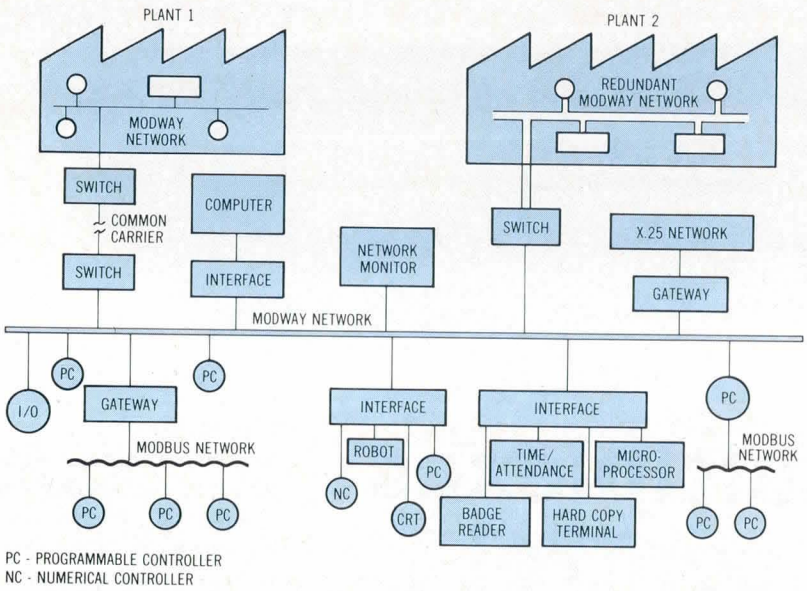

Typical Modway system configuration. Product family includes interfaces for current programmable controllers, computer interfaces, serial line interfaces, network monitors, network switches and gateways, and gateway services to public or private network facilities

Modway, a high speed communications system aimed at industrial local networking applications, can link a variety of computers, controllers, and terminal devices, and is designed for reliable operation in noisy factory environments. The system allows various elements to communicate with each other over a common shared bus and is configured to be compatible with the proposed IEEE standard (*Computer Design,* Mar 1981, pp 12-20). Modway was developed by Gould Modicon, Haverhill St, Andover, MA 01810, who say that it represents true distributed communciations from any site to any other with guaranteed realtime response and media independence in any data communication topology.

Unlike Ethernet-type systems Modway is speed and distance independent and operates at a 1.544M-bit/s rate at distances up to 5000 m. The data rate is compatible with T1 carrier for microwave and satellite communication over common carrier facilities.

The system supports both passive baseband and active CATV-type coaxial media. The company says that other cable technologies such as fiber optics will be available later. Network configurations range from star and daisy-chained connections to full multidrop using splitters and taps. The cable can use almost all commercially available media accessories. In addition, the company has designed special accessories for use in passive coaxial systems that increase the number of drops that can be accommodated. Cable installation is a customer responsibility, but documentation is provided to help determine the most flexible topology and media components.

The peer-to-peer system allows any device to communicate with any other, with no master or bus arbitration device required. Devices are connected on the common bus medium through "interface boxes." Time division multiple access (TDMA) with token (baton) passing is used to access and temporarily control the system and provide a totally deterministic communication service. Once a device has control of the system it is a master and can communicate with other devices by establishing logical links (virtual circuits) with them. These links are maintained during the baton-passing sequence, and the duration of time in which the device is a master is user programmable. The number of devices attached on the system depends on such criteria as media, distance, and cable topology. A single CATV-based network can handle 10,000 devices max.

The system supports three different types of devices. Those on the token-pass sequence and able to initiate communications are primary devices. Secondary devices are those that only respond when queried. The third type is a demander, a secondary device that can become a primary for short periods of time in response to the occurrence of some event in that device.

Included in the system is an option allowing full redundancy in media and Modway interfaces. A failsafe feature protects against failure of a single element bringing down the entire system. Failed or unplugged devices are automatically removed or new devices added by a self-repairing mechanism. The system will self-initialize on power-up and can configure itself without intervention from any other device. Highly secure protocols limit undetected errors to one error in the lifetime of a system, said to be one undetected error in 50 years.

The system falls under the umbrella of Modicon's network architecture for distributed systems (Monads) that provides for layered levels of communications protocol similar to the ISO/OSI model. The architecture also includes the Modbus communications system to provide a networking system capable of interconnecting Modway and Modbus networks over local and public facilities.

Circle 321 on Inquiry Card

System Encodes Data Stream into Standard Television Signal

Providing the user with an additional data communications capability within any standard 60/525 or 50/625 TV signal, the VIDAC communication system encodes digital data signals into the vertical

(continued on page 38)

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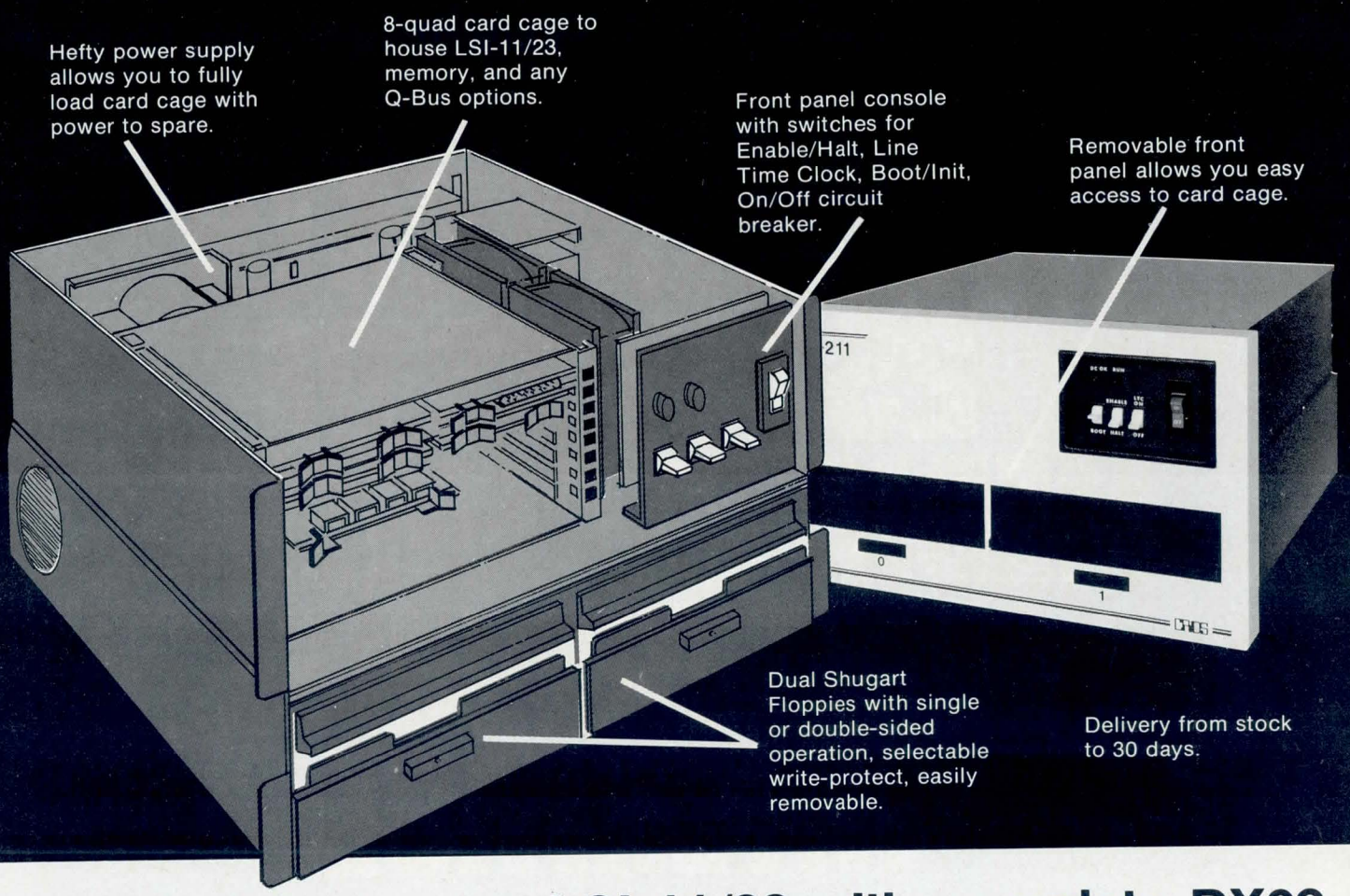

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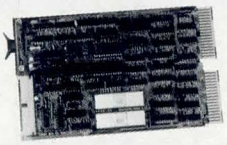

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The ANSI interface is microprocessor-based, and works efficiently at high data rates. The result: 3M drives are easy on customers' equipment overhead.

3 MIGRATION FROM 10 TO 60 MEGABYTES AND BEYOND.

The third benefit the 3M Compact Disk Drive family gives you is the migration needed to keep up with user demands. Migration that won't dead-end your customers, or cost them an arm and a leg to obtain.

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5 AND OTHER OUTSTANDING FEATURES.

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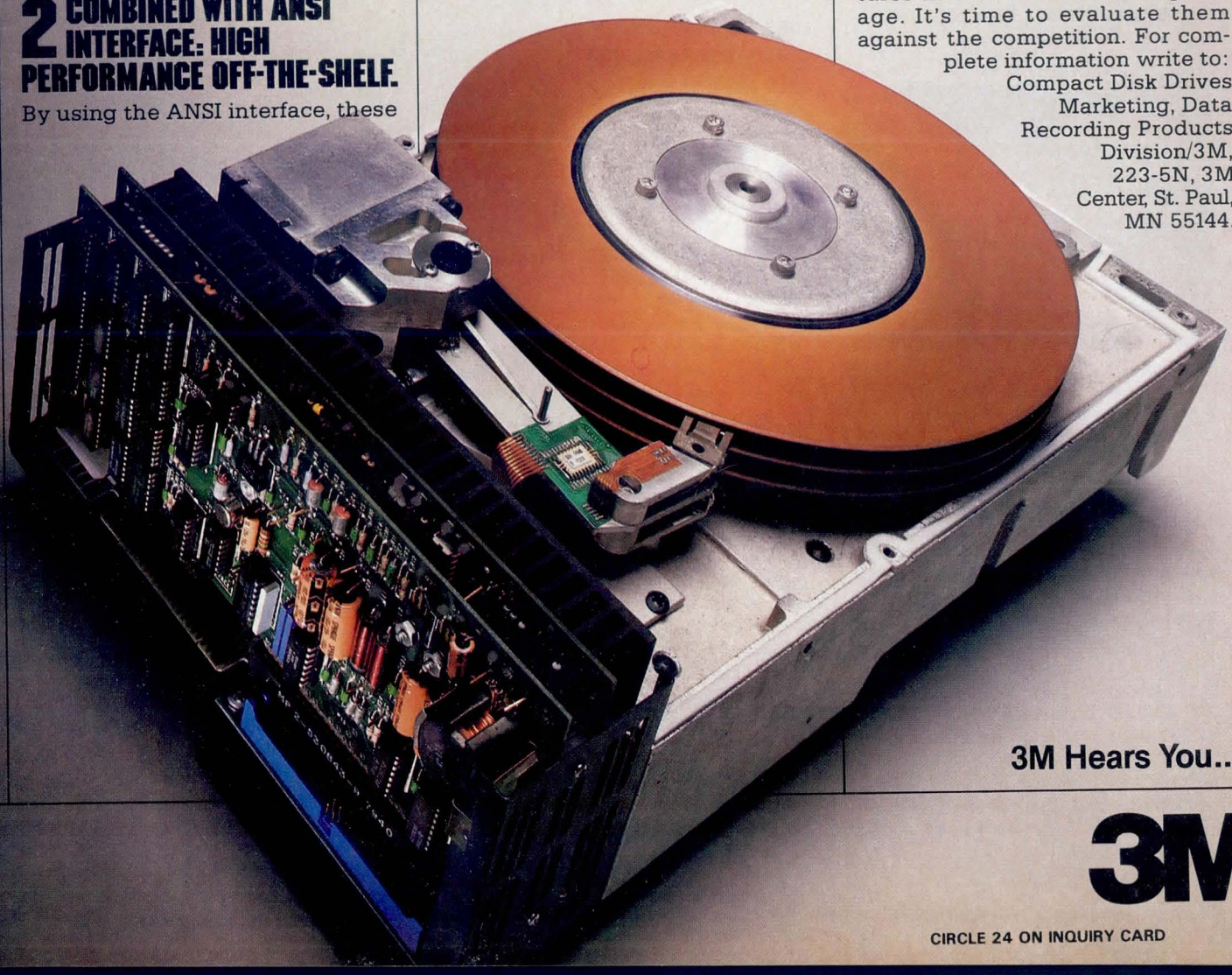

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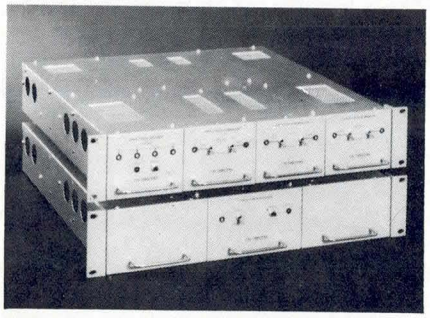
CIRCLE 24 ON INQUIRY CARD

blanking period at the transmission site and decodes them after reception from a satellite or any conventional TV transmission system. Developed by Caldatacom Inc, 1711B Little Orchard St, San Jose, CA 95125, the system provides the user with a secure data channel for interterminal communications without the need for separate data tielines.

The encoder input consists of a standard color video signal and an asynchronous RS-232-C data signal. Input data rate is selectable from 1200 to 9600 baud (optionally down to 75 baud). The encoder output provides a video signal containing data encoded on one line in the vertical interval. The data input contains one start and two stop bits, and at 9600 baud provides a data input rate of 872 char/s. A 1k-byte RAM managed by an 8085 microprocessor handles data formatting and input storage. If the video signal is disturbed for any reason the encoder continues to accept data into store, with available storage time of approximately 1 s. If data transmission is interrupted for more than this period, a marker is inserted into the data stream to indicate that data have been lost.



Vertical interval data communication encode (top) and decode terminals. Transmit and receive terminals are each 3.5″ (8.9 cm) high in standard rackmount chassis. All video connections are by 75-Ω BNC and data via DP-25 series connectors

Inserting 16 characters on the chosen data line in each field, the encoder provides a data transfer rate of 960 char/s, transmitting about 10% faster than the 872-char/s input rate. This allows the system to "catch up" from input store if the transmission path is interrupted or is not able to be used by the encoder. System accuracy for data transmission is related to video signal to noise ratio (SNR) of the transmission path. With a worst pattern bit sequence the maximum bit error is 10^{-5} and 10^{-6} at 43 and 52 dB SNR respectively.

The receive terminal contains at least one decoder and one dual-channel data eliminator. Up to six video channels can be handled, four of which can be scanned for data. Control logic causes the decoder to sequentially sample the four video inputs for 1 s each. When an incoming data stream is detected, the decoder locks to that video source until the stream ceases or is interrupted. The data-bearing signal is passed through a data eliminator that removes the data stream from the "data line" and inserts locally generated blanking before transferring the video signal to the local video system.

The data appear at the decoder output in RS-232-C format for distribution to local user terminals for selection and/or printing. A hardwired feedthrough mode, activated if power is lost at the receive terminal, protects video signal integrity.

Circle 322 on Inquiry Card

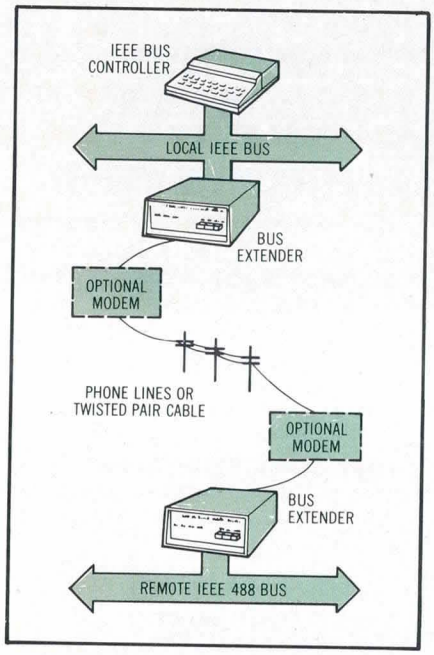
Bus Extender Provides Unlimited Range for IEEE-488 Systems

Virtually unlimited range for IEEE-488 bus systems is said to be available through use of the model 4886 bus extender from ICS Electronics Corp, 1620 Zanker Rd, San Jose, CA 95112. Implementing the extender overcomes the 66′ (20-m) limitation normally associated with 488 bus systems, and allows the user to interconnect any number of widely dispersed 488 systems into a single system directed by a master controller.

The device converts parallel bus data to serial form for high speed transmission up to 4000′ (1219 m) with twisted pair cable and over unlimited distances using modems and telephone lines. A second bus extender at the remote end reconverts the serial data to parallel bus data.

With twisted pair cabling, the transmission link is full duplex, allowing the controller to accept service requests or other inputs from the remote site while sending data or commands. In a multidrop configuration, up to 31 remote sites, identified by separate addresses, can communicate at one time with the controller.

With the device, master control is extended to an unlimited number of remote sites for unlimited distances over leased, private, or dial-up lines using synchronous or asynchronous modems. An optional autodialing feature (Bell 810A/C or equivalent) allows the extender to automatically call a remote site, verify the link, and notify the master controller of the completed call.



Limited only by the speed of the modems and the quality of the telephone lines, the extender can operate at up to 19.2k bits/s. It can be added to any IEEE bus system without the need to rewrite software programs or rewire control functions and can interface with all existing RS-232 compatible modems and future RS-449 systems.

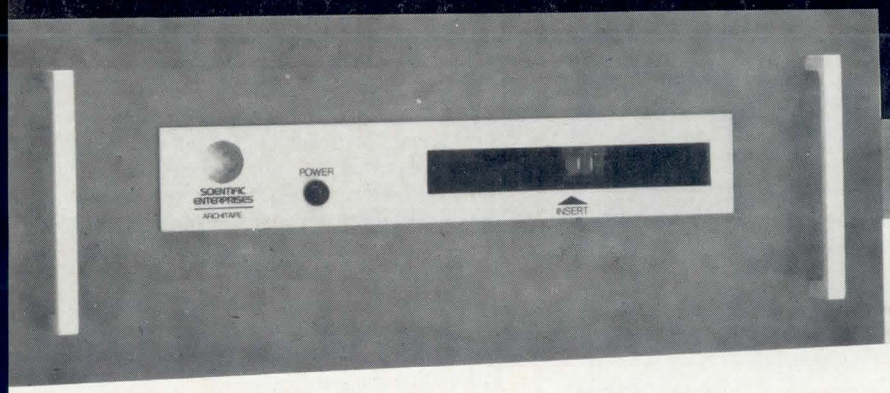
The extender can be configured to generate clock signals for synchronous operation or to accept clock signals from another extender or from a modem. As a transparent communications link, the unit supports all IEEE-488 bus commands, including a modified form of parallel poll. Timing restrictions on the response from the remote bus make the parallel poll answer valid after 20 ms plus the serial path turnaround time.

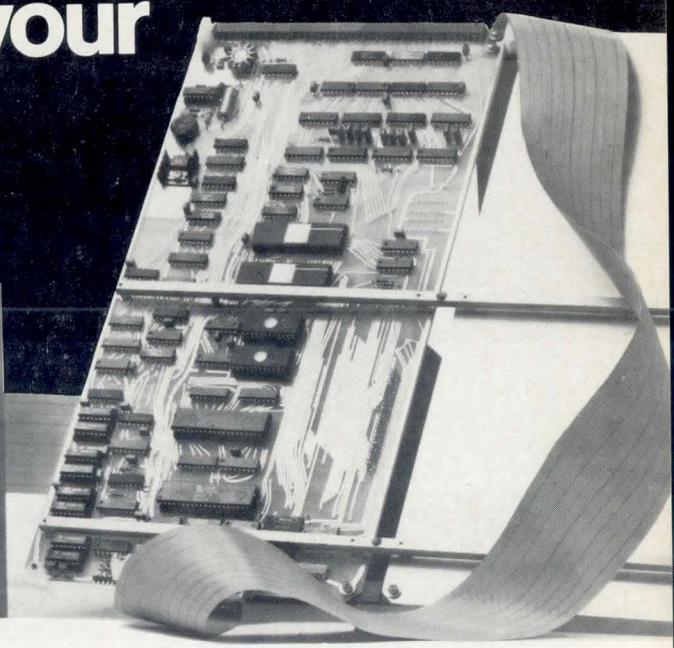
In addition, the extender can be programmed to perform an automatic self-check and determination of controller location at power turn-on. A remote extender's presence and open data link is continuously monitored during transmission idle time. Serial data integrity is ensured by error checking each transmission and retransmission of faulty messages via both parity and checksum error detection. The device measures 8.5 x 3.5 x 11.3″ (32.6 x 8.9 x 28.6 cm) and weighs 6 lb (2.7 kg).

Circle 323 on Inquiry Card

ARCHITAPE™

Now, 14 megabyte cartridge tape backup for your Perkin-Elmer or Tektronix 4081.





Cartridge tape archiving. The Architape 14 Megabyte (formatted) 4-track cartridge tape subsystem is compatible with all Perkin-Elmer (Interdata) 16 and 32-bit minicomputers, and the Tektronix 4081. The subsystem comes ready to install with all rack mount hardware, controller, cables, software, and full documentation.

Winchester backup. The Architape subsystem is designed to provide convenient, portable, ¼" ANSI tape cartridge backup for fixed disc systems. The drive itself provides maximum read/write protection against environmental contaminants. Your cartridge tapes can be read on any other Architape subsystem.

Complete Technical backup. Scientific Enterprises warrants each system for a full 90 days and provides complete documentation, a maintenance manual, plus prompt service and repair capabilities.

Software. Architape software is completely compatible with both the Perkin-Elmer OS16 and OS32 operating systems, and with the Tektronix 4081 GOS operating system. You get 9-track magtape performance for half the price... and compatible device drivers in half the memory. 4081 users get a complete stand-alone archive program that doesn't require changes to GOS at all!

Features

Drive: ANSI Std x 3.55—1977 cartridge • DEI Funnel Drive • Capacity is 14 Mbytes (formatted) • Transfers 192 Kbits/s, 30 ips • Density is 6400 bpi • Hard Error Rate is 1 in 10^{10} • 90 ips rewind (450 ft./60s) • Integral tape cleaner • Dual-gap head, read while write separate erase • Self-clocking MFM encoding.

Controller: Z-80 μP-based • Compatible with MUX and SELCH buses • Self-test on power up and initialize • Bus transfer rate is 35 Kbytes/s • Retries read/write functions a maximum of 10 times. • CRC error checking • Record size variable to 12 Kbytes • Record buffer on controller • Forward file search at 90 ips • Power requirement is +5V only at 2.5 Amps • Half-card (7 x 15:) ECB.

Now, networking. Architape's companion product, Archinet,™ provides add-on networking (up to 32 stations) for the Architape subsystem. Archinet provides an on-board microprocessor to handle protocol and retransmissions, and is completely supported with software. Configuring your network is easy because all stations communicate over a single shared cable.

Add-on and OEM information. Fast. If you're thinking of adding cartridge tape backup to your present system, adding networking, or OEMing new systems with archiving and networking capabilities, call Charles Vollum at SEI, fill out the coupon below, or, circle the reader service number. We'll be back to you with OEM or user add-on information. Fast.

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Company_____ ☐ OEM?_____

Computer Model_____

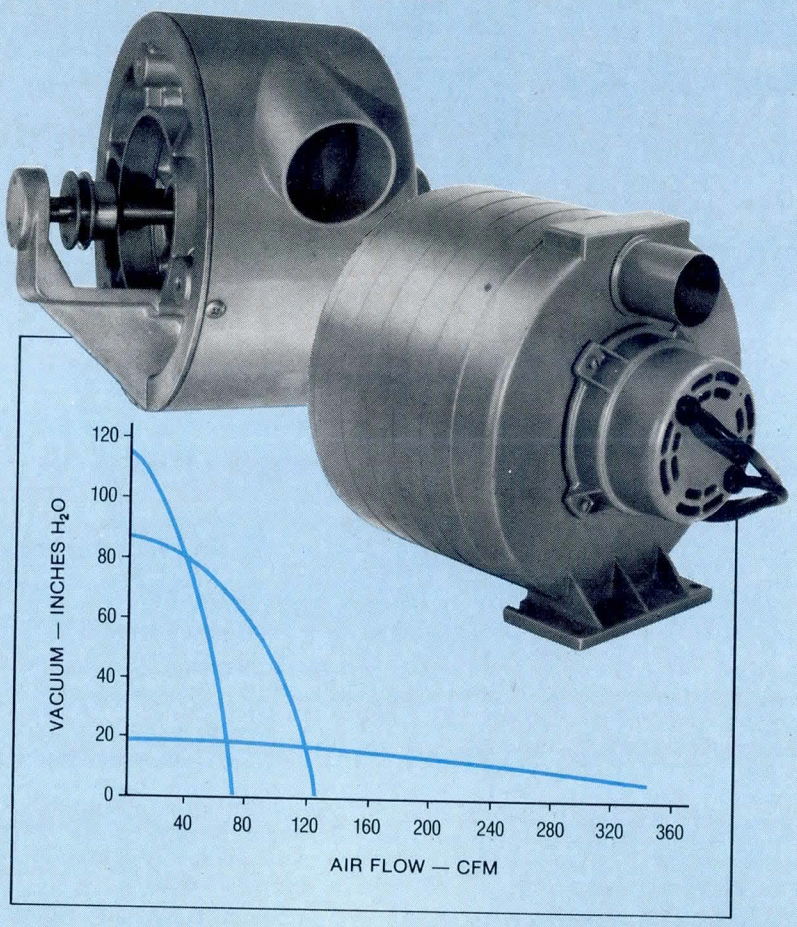
Address_____

City_____ State_____ Zip_____

Phone (_____)_____

CIRCLE 25 ON INQUIRY CARD

Windjammer® blowers provide multi-function working air



One air system for pressure, vacuum or both

Windjammer high-performance blowers supply vacuum and/or pressure for a wide variety of jobs. Typical applications include tape transports, card sorting, vacuum hold down, air sampling and cooling.

These blowers are designed specifically for environments where high noise levels would be objectionable and feature carefully balanced components. They can be supplied for belt drive or complete with motor.

Lamb Electric engineers can work with you to develop a Windjammer system tailored to your requirements. And, we can schedule quantity deliveries to meet your production requirements. Contact AMETEK, Lamb Electric Division, 627 Lake Street, Kent, Ohio 44240. (216) 673-3451.

AMETEK
LAMB ELECTRIC DIVISION

COMM CHANNEL

Standalone Communications Processor Supports Various Protocols

Standalone, self-powered, and microprocessor based, the MC-80 communications processor provides up to 16k ROM, 16k RAM, three serial communications ports, and one parallel printer port. Developed by Innovative Electronics Inc, 15200 NW 60 Ave, Miami Lakes, FL 33014, it supports numerous communications protocols and provides on- and offline diagnostics.

Available protocols permit the attachment of foreign devices to IBM, Burroughs, NCR, Honeywell, and Univac networks either by direct connection or through dedicated/multidrop modems. Modular software allows the configuration of systems that provides mainframe computer users with device independence and economies on RJE and interactive stations. End to end peripheral control and multidrop polling front ends for minicomputers are enabled, as well as communications between computers from different manufacturers. Device handlers allow attachment of letter quality printers, low cost dot matrix printers, keyboard CRT terminals, and medium speed line printers.

Extensive diagnostics increase the maintainability of the unit. Online diagnostics, shown on a 7-segment display, include poll or selection of a device, transmission errors, and modem status. Either power-on or operator-initiated actions execute offline diagnostics. CPU, ROM, RAM, and data paths are routinely tested. Operator-initiated tests include the exercise of attached peripheral devices, or canned messages to and from attached processors. Another level of testing completely checks every interface signal through test connectors that connect inputs to outputs.

Circle 324 on Inquiry Card

CIRCLE 26 ON INQUIRY CARD

Three Interconnecting modules, no hard wiring and you get the Switching Power Supply of the 80's

Customer: What's the significance of the 3 modules?

ACDC Salesman: In the past, everybody including ACDC produced specific switchers for given applications. You know, assemble the components in a box, wire them and then tweak and test and trim, etc. In our RS/RT switchers, we produce large quantities of three basic modules, and then test the daylights out of them, followed by full load, high temp burn-in.

Customer: What modules are you talking about and how do they work?

ACDC Salesman: O.K., we produce input modules, converter modules and output modules. We have 16 different board modules that make up 50 different power supplies. We take various combinations out of stock and assemble them in a chassis, interconnecting them through a mother board. It's fast, reliable, and it eliminates hard wiring.

Customer: I see, you can make up most any switcher I could want right out of stock. You say no hard wiring...what's wrong with wiring?

ACDC Salesman: Harnesses are a point of potential failure. There are possible cold solder joints vulnerable to everything including shipping vibration, not to mention noise considerations in how the harnesses are placed throughout. No one has ever successfully introduced a switching supply without hard wiring until our RS/RT Series.

Customer: When you say you test the daylights out of them, give me some details.

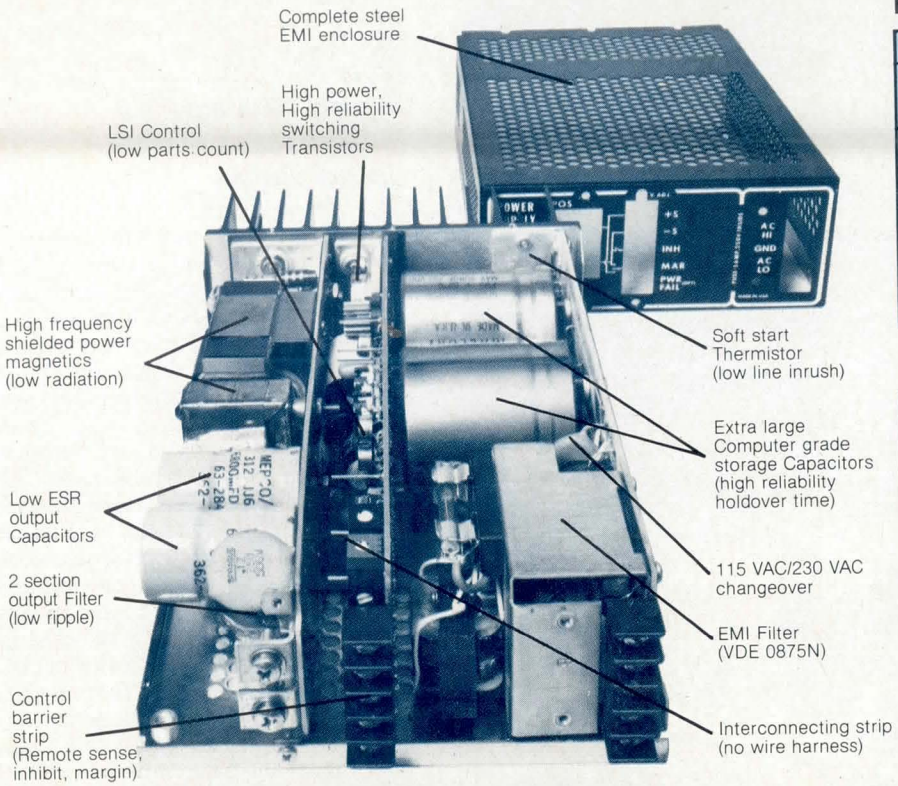
ACDC Salesman: O.K. First, all of our active devices are 100% screened. We stable bake, temperature cycle, and then 100% electrical test. All to MIL-STD-883B. The modules themselves are computer tested. When we assemble them into the final unit, we first Auto-Test, then burn-in for 48 hours at 50°C under full load, cycled, Auto-Test again with computer print out- serialized. You get one copy of the hard test data and we keep a copy. In other words we all know exactly what you're getting.

Customer: Everything sounds good, but what about the cost?

ACDC Salesman: Simple. We save you money because instead of building a hundred of these and fifty of those, etc., we continuously build thousands of the same modules each month. That saves us, and you, money. We test everything thoroughly and that eliminates warranty returns, reworks and all those costly problems. Believe me, if you've ever seen the production of power supplies, you'd know we have a uniquely superior product here...and, at a fantastically low price.

Customer: It sounds to me like you've brought power supply technology up to date.

ACDC Salesman: Thanks...we think our RS/RT Series are the switchers of the 80's.



RS Series/Single Output

SINGLE OUTPUT					
OUTPUT VOLTS	OUTPUT CURRENT				
	RS50	RS100	RS150	RS300	RSF375
2	10.0	20.0	30.0	60.0	—
5	10.0	20.0	30.0	60.0	75
6	8.0	9.0	25.0	50.0	—
12	4.5	9.0	13.5	27.0	31
15	3.6	7.2	10.8	21.0	25
18	3.0	6.0	9.0	18.0	—
24	2.5	4.5	7.0	13.0	15
28	2.0	4.0	6.0	11.5	—

RT Series/Triple Output

MULTIPLE OUTPUT				
	TRIPLE			QUAD
	RT100	RT150	RT300	RQ300
MAIN OUTPUT	5V 20A	5V 30A	5V 60A	5V 30A
AUXILIARY OUTPUTS	12V 2A 15V 2A	12V 5A 15V 4A 5V 5A	12V 5A 15V 4A 5V 5A 24V 2A	12V 5A 15V 4A 5V 5A 24V 4A
MAX. POWER	100W	150W	300W	300W

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CIRCLE 27 ON INQUIRY CARD

Processor Performs Communications Functions In Distributed Data Networks

A 2-way communications system designed for distributed networks, ICOT 253 is the latest model in the 25X family of modular processors from ICOT Corp, 830 Maude Ave, Mountain View, CA 94043. A variety of 253 configurations handles protocol/code conversion, line concentration, line multiplexing, and selective message routing. The processor can accommodate up to five full duplex 9600-baud synchronous or asynchronous lines, up to four of which handle customer-specified byte protocols and one a bit protocol such as 3271 SDLC or X.25/HDLC.

The processor uses a multiple microcomputer architecture: each line has its own computer, line interface, RAM, and program space. Each microcomputer can access a system RAM through an ICOBUS™ that handles interconnection, scheduling, and data transfer between the microcomputers.

Protocol/code conversion capability enables communications between incompatible terminals and host or network processors without requiring major software changes. The unit supports such standard protocols as Teletype 33/35, Bisync, PARS, P1024, 3271 SDLC, Uniscope, and X.25/HDLC.

Used in line concentration, each line can handle batch and interactive terminals, and both synchronous and asynchronous lines can be multidropped. In multidrop applications the unit handles polling of downline terminals. The user can also optionally apply the unit as a multiplexer instead of a concentrator.

The processor can route messages to different hosts, to other terminals attached to it, or to other network processors. This capability, combined with the ability to handle downline terminal polling, can measurably reduce host overhead.

Circle 325 on Inquiry Card

System 34/38 Interface Accommodates Non-IBM Output Devices

Output interface IF/1A provides plug compatibility between IBM systems 34, 38, and 5250 IDS, and non-IBM serial asynchronous RS-232-C output devices such as special or general purpose printers, paper tape punches, display-only monitors, and other similar output peripherals.

The device, a product of Technical Analysis Corp, 120 W Wieuca Rd NE, Atlanta, GA 30042, emulates an IBM 5256 printer and attaches to the 34/38 system via standard twinaxial cable. It is compatible with data lines that support 5256, 5225, 5252, models 1 or 11 5251 devices with cable through feature, and 5251 model 2 or 12 with cluster or dual cluster feature.

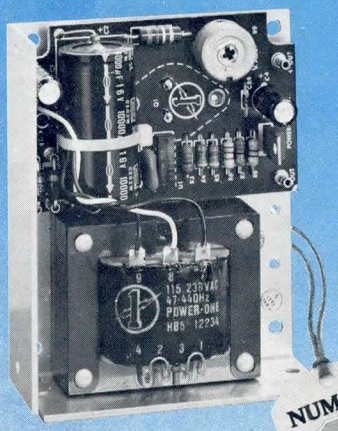
Interface provides XON/XOFF and CTS protocol support for output peripherals and converts all standard EBCDIC characters to ASCII. An internal self-test function verifies operation of the attached output device. Baud rate selection in standard units is from 110 to 19,200. The IF/1A is the first in a family of products intended for use by OEMs and systems houses in the integration of end user systems. □

Circle 326 on Inquiry Card

FOR ALMOST A DECADE...

$24.95

...AND STILL HOLDING



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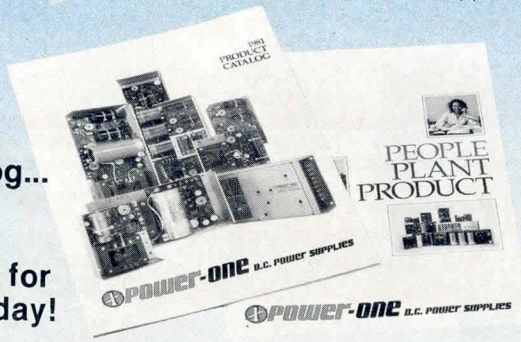

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COMPUSTAR™

INTERTEC'S INCREDIBLE 255 USER SMALL BUSINESS COMPUTER

At last, there's a multi-user microcomputer system designed and built the way it should be. The CompuStar™. Our new, low-cost "shared-disk" multi-user system with mainframe performance.

Unlike any other system, our new CompuStar offers what we believe to be the most practical approach to almost any multi-user application. Data entry. Distributed processing. Small business. Scientific. Whatever! And never before has such powerful performance been available at such modest cost. Here's how we did it . . .

The system architecture of the CompuStar is based on four types of video display terminals, each of which can be connected into an auxiliary hard disk storage system. Up to 255 terminals can be connected into a single network! Each terminal (called a Video Processing Unit) contains its own microprocessor and 64K of dynamic RAM. The result? Lightning fast program execution! Even when all users are on-line performing different tasks! A special "multiplexor" in the CompuStar Disk Storage System ties all external users together to "share" the system's disk resources. So, no single user ever need wait on another. An exciting concept . . . with some awesome application possibilities!

CompuStar™ user stations can be configured in almost as many ways as you can imagine. The wide variety of terminals offered gives you the flexibility and versatility you've always wanted (but never had) in a multi-user system. The CompuStar Model 10 is a programmable, intelligent terminal with 64K of RAM. It's a real workhorse if your requirement is a data entry or inquiry/response application. And if your terminal needs are more sophisticated, select either the CompuStar Model 20, 30 or 40. Each can be used as either a standalone workstation or tied into a multi-user network. The Model 20 incorporates all of the features of the Model 10 with the addition of two, double-density mini-floppies built right in. And it boasts over 350,000 bytes of local, off-line user storage. The Model 30 also features a dual drive system but offers over 700,000 bytes of disk storage. And, the Model 40 boasts nearly 1½ million bytes of dual disk storage. But no matter which model you select, you'll enjoy unparalleled versatility in configuring your multi-user network.

Add as many terminals as you like - at prices starting at less than $2500. Now that's truly incredible!

No matter what your application, the CompuStar can handle it! Three disk storage options are available. A tabletop 10 megabyte 8" winchester-type drive complete with power supply and our special controller and multiplexor costs just $4995. Or, if your disk storage needs are more demanding, select either a 32 or 96 megabyte Control Data CMD drive with a 16 megabyte removable, top loading cartridge. Plus, there's no fuss in getting a CompuStar system up and running. Just plug in a Video Processing Unit and you're ready to go . . . with up to 254 more terminals in the network by simply connecting them together in a "daisy-chain" fashion. CompuStar's special parallel interface allows for system cable lengths of up to one mile . . . with data transfer rates of 1.6 million BPS!

Software costs are low, too. CompuStar's disk operating system is the industry standard CP/M*. With an impressive array of application software already available and several communication packages offered, the CompuStar can tackle even your most difficult programming tasks.

Compare for yourself. Of all the microcomputer-based multi-user systems available today, we know of only one which offers exactly what you need and should expect. Exceptional value and upward growth capability. The CompuStar™. A true price and performance leader!

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CIRCLE 29 ON INQUIRY CARD

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8-inch Winchester Multi-User Systems. Now In Volume-$8,500.

Altos is delivering the cream of the crop with their new 8-inch multi-user Winchester disk systems. They're freshly packed with the quality features you expect from Altos, and at a price you expect from Altos, too—just $8,500.

Pick from two fully integrated systems, each packaged in our new compact, stylish cabinet suitable for either rack mount or table top applications. You get 10 MBytes of reliable on-line storage in our 8-inch Winchester drives. Then for system back-up storage, you can select from either 8-inch, single or double-sided floppy drives (ACS8000-10 and -10D) or a ¼-inch magnetic tape drive (ACS8000-10/MTU). And for powerful performance, all of these Z80A*based systems come complete with 208K of RAM and 6 programmable serial ports, ready to support four users.

Here's the most bountiful selection of systems and capacities in the field from the company that knows how to deliver quality systems in the volumes that OEMs need to stay competitive.

And Altos supports these systems with a broad software selection including the three industry standard operating systems—CP/M, multi-user MP/M** and OASIS†. These operating systems support seven high level programming languages: BASIC, FORTRAN, COBOL, PASCAL, APL, PL/1 and C. Also available are comprehensive communications packages: ASYNC—Altos-to-Altos, BISYNC—Altos-to-mainframe and full networking with CP/NET. All are designed to run on a high speed 800 Kilobaud networking channel—standard with every system.

The ACS8000-10 Winchester systems join our growing family of field-proven products. In just three years, more than 8,000 systems have been shipped to an OEM customer-base.

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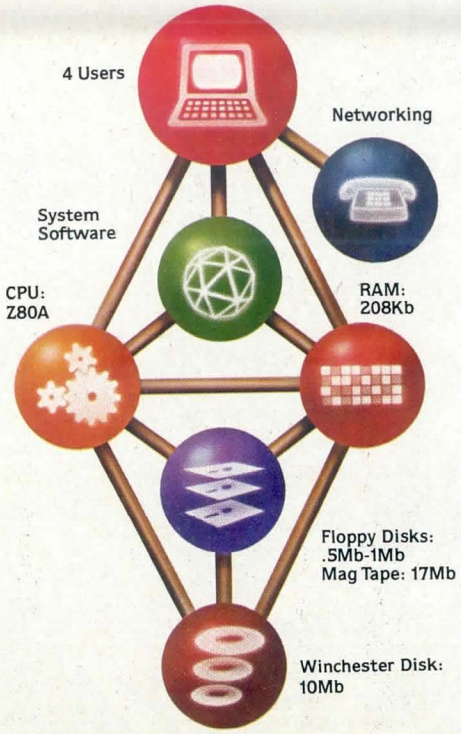

SYSTEMS PICTURED:

ACS8000-10 (10Mb HD + 1 floppy)	$ 8,500
ACS8000-10/MTU (10Mb HD + DEI Mag Tape)	$10,990

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DEC VT100® Compatible Plus

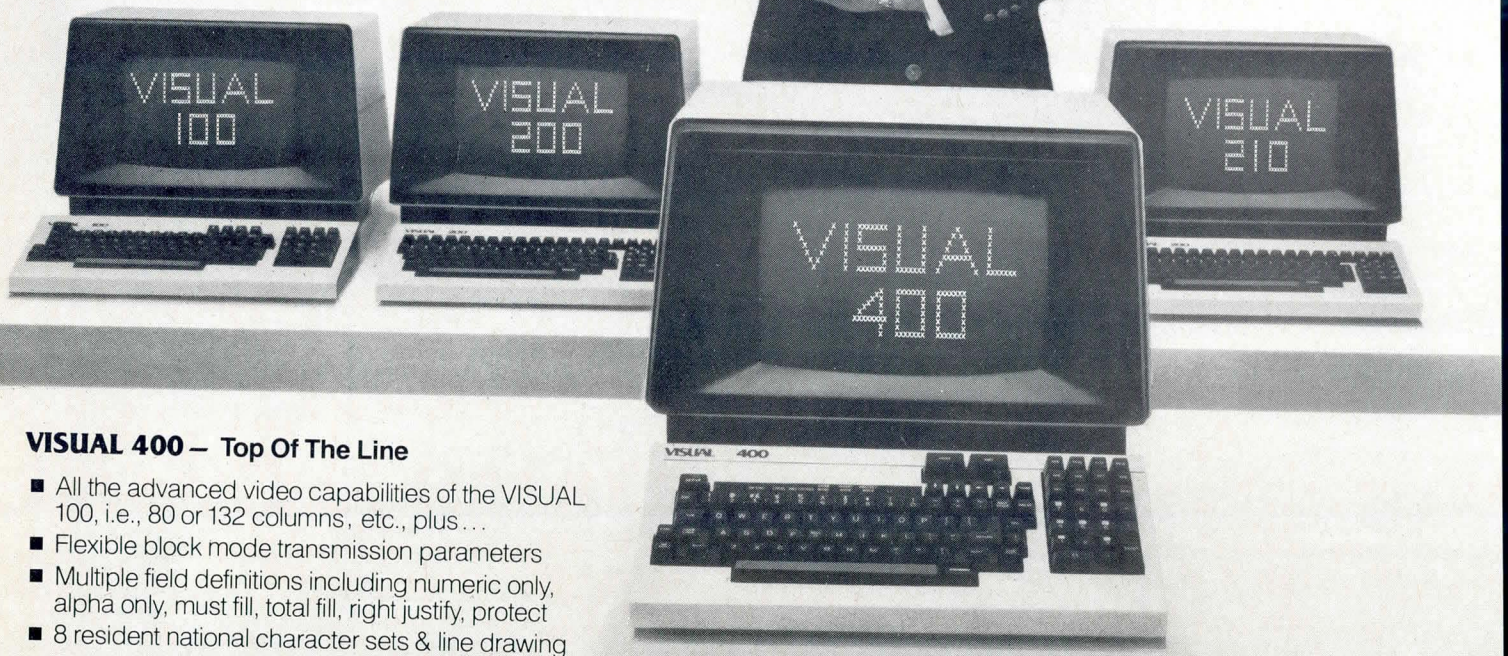
- Advanced video package is standard
- Non-glare, tiltable screen
- Detached solid state keyboard, n-key rollover
- CRT saver feature
- Serial buffered printer interface option
- Hewlett-Packard protocol compatibility option

VISUAL 200 – Switchable Emulations

- Switch selectable emulation of DEC VT52®, Hazeltine 1500, ADDS 580, LSI ADM-3A
- Non-glare tiltable screen
- Detached solid state key board
- Large 7 x 9 dot matrix characters with descenders for lower case
- Background/foreground, blink, security fields, editing
- EIA-RS232-C and 20 ma interfaces, serial printer port, smooth scroll, 14 function keys
- Numeric keypad and cursor positioning keys

VISUAL 210 – Block Mode

- All the features of VISUAL 200 plus...
- 14 user programmable function keys, up to 48 codes each may be down line loaded
- Transmit line, field, page
- User programmable message framing including start of message, end of line, field separator and end of message codes
- Remote transmit
- Suspend/resume transmit
- Transmit unprotect/all



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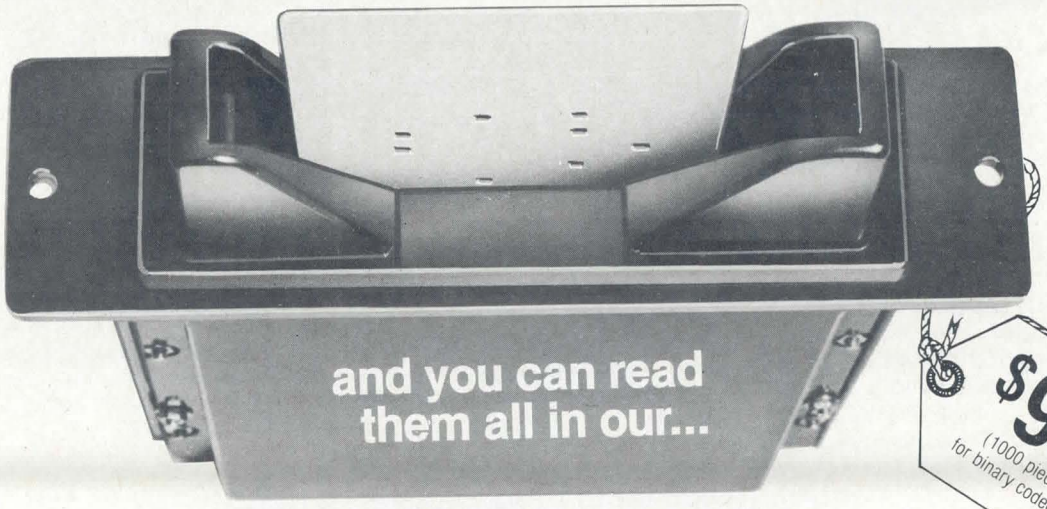
This badge can identify 999,999,999,999,999,999,999 **persons...**



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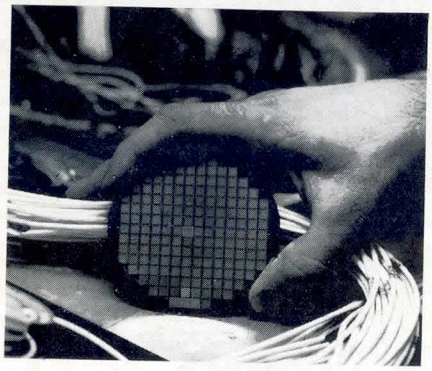
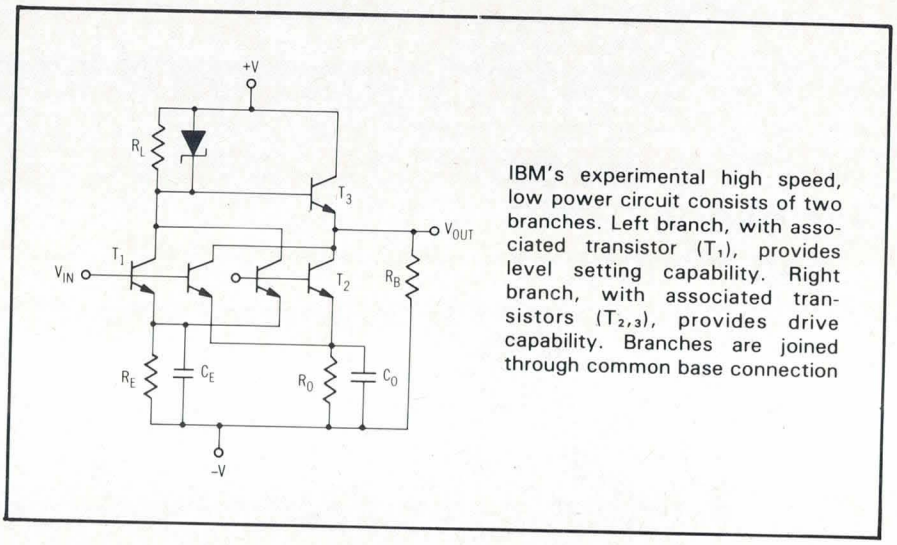
CIRCLE 33 ON INQUIRY CARD

Experimental Circuit Could Increase Computer Performance, Reduce Power Requirements



Wafer consisting of 159 chips made up of experimental Konian-Walsh circuits manufactured using normal 2.5-μ ground rules is framed by cables leading to LSI tester. Test results provided hardware verification of computer simulations



IBM's experimental high speed, low power circuit consists of two branches. Left branch, with associated transistor (T_1), provides level setting capability. Right branch, with associated transistors ($T_{2,3}$), provides drive capability. Branches are joined through common base connection

An experimental computer circuit technology that could yield high performance, low power chips was described by Richard R. Konian of IBM's General Technology Div, East Fishkill, NY facility, at Comcon '81 in San Francisco. The Konian-Walsh circuit, invented by Mr. Konian and James L. Walsh, has switching speeds faster than ECL, but with the low power level and cell size of TTL. Shorter electrical path and compact design reduce signal delay and power requirements.

The circuit consists of two independent branches: the input branch with logic elements that establish 0 and 1 levels; the output branch that provides high drive capability through active elements on both sides of the terminal that afford active pullup and pulldown. Transistors in the device are placed in parallel and the bases have a common connection. The signal is able to move from input to output in one collector time. This is done by combining, in one stage, both logic level capability and push/pull drive capability to drive line capacitance. Load characteristics include a fanout of 2 and 250-ps delay at about 2.5 mW of power.

Low output impedance is offered in both directions: emitter follower on the way up and capacitive overdrive on the way down. All switching transistors are switched by a low impedance source or driver. The two bottom transistors are switching devices and the third is an emitter follower.

Noise margin of the circuit depends on the resistor ratio of the dc gain to satisfy a particular application. It has a noise margin-performance trade-off. Independent current paths supply driver current and dc voltage. Line current passes through one branch and dc level current through the other. The dc level is set independently of the current discharge and charge capability of the driver. Therefore, functions of driving current and setting voltage are not in conflict.

Overdrive capacitors reduce dc power by helping to overcome the effect of the horizontal geometries of the transistors and providing a discharge pad for the line capacitors. Once capacitors are charged, a lower steady state capability is attained. Current flows only 50% of the time.

If research validates experimental results, the circuit may allow significant progress toward improving power, speed, and density factors now limiting computer size and performance. The circuit compares favorably as a potential alternative to widely used computer circuits. A typical ECL circuit has a 4.0- to 8.0-pJ rating and generates heat that necessitates advanced cooling techniques. A typical TTL circuit has a 1.2-pJ rating. The circuit may enable the use of VLSI in high performance computer systems, and its versatility may give it the potential for use in small low end systems as well. For example, in small systems fewer than 3000 of the devices might be configured on a chip using circuit power in the 2.5-mW range. In larger systems, the circuits might be packed at much higher densities using 0.5 to 0.7 mW.

Uninterruptible Power System Is Based on Variable Speed Constant Frequency Generator

PowerRotor overcomes power outage and erratic power supply problems affecting small/medium sized computers and sensitive electronic devices by isolating them from utility power. The low cost uninterruptible power supply, offered by Continental Power Systems, Inc, One Landmark Sq, Stamford, CT 06901, is based on a variable speed, constant frequency generator technology.

The unit supplies power to the computer during utility interruptions of 10 to 30 s duration. Except during interruptions, it is powered by a motor run on utility power. Since line power goes only to the drive motor, the computer is completely isolated from utility power and is supplied with well regulated power having frequency accuracy to 0.025% by the generator.

Through instantaneous and continuous remagnetization of the generator's rotor field poles, the UPS automatically adjusts itself to hold output power frequency constant. When an outage occurs, the system provides

(continued on page 52)

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*Actual photo from monitor.

CIRCLE 34 ON INQUIRY CARD

clean, accurate power; and in case of an extended outage, it provides enough time for orderly shutdown or start-up of standby power source.

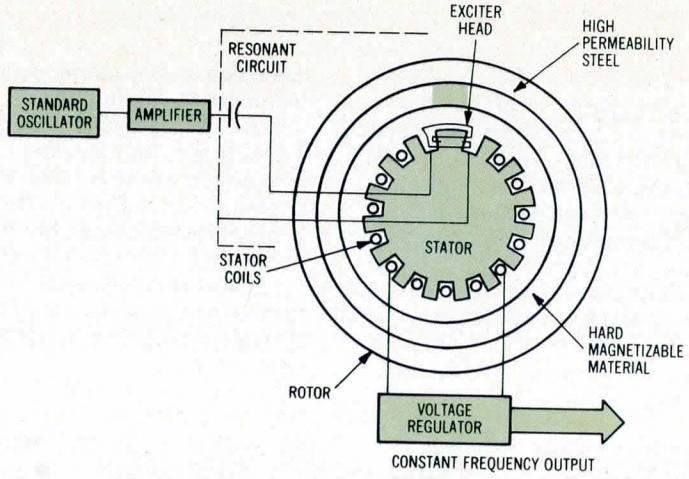
The inner periphery of the rotor contains a layer of magnetizable material. During operation, a pattern of magnetic field poles is written into this magnetic layer. The number and length of the written poles are determined by the speed of rotation of the rotor as well as the controlled frequency that drives the exciter coil which writes the field pattern.

As the exciter coil writes a controlled number of poles per second, the number of poles around the circumference of the rotor changes with the rate of the rotor. As rotor speed varies, the number of field poles compensates in inverse proportion, resulting in a continuously changing field pattern and in output frequency from the stator output windings that is under control of the coil.

The exciter coil is driven by a reliable low power solid state circuit. Frequency is determined by a crystal reference which achieves accuracy of 0.025%. Thus, frequency accuracies are available at power levels from a generator whose shaft speed may vary.

In addition to stable power, the system offers low maintenance and low emi to avoid interference with operation of the computer or other electronic equipment. Units can be paralleled for multi-unit installations. Model A7-603 is rated at 7.5 kVA. Output is 120/208 Vac, 3 phase, 60 Hz. Model A3-601, rated at 4.5 kVA, 120 Vac, 60 Hz single-phase will be available soon. Prices are $19,950 and $9975, respectively.

Circle 350 on Inquiry Card



UPS technology developed by Continental Power Systems is based on generator that instantaneously varies its field poles. Because rotor speed changes little during revolution, and same field pattern passes over output windings, output windings generate power output with frequency as accurate as that of exciter coil

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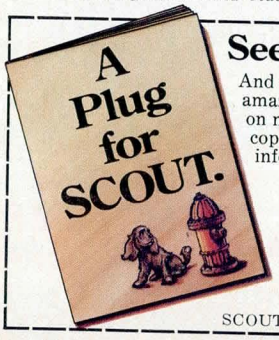

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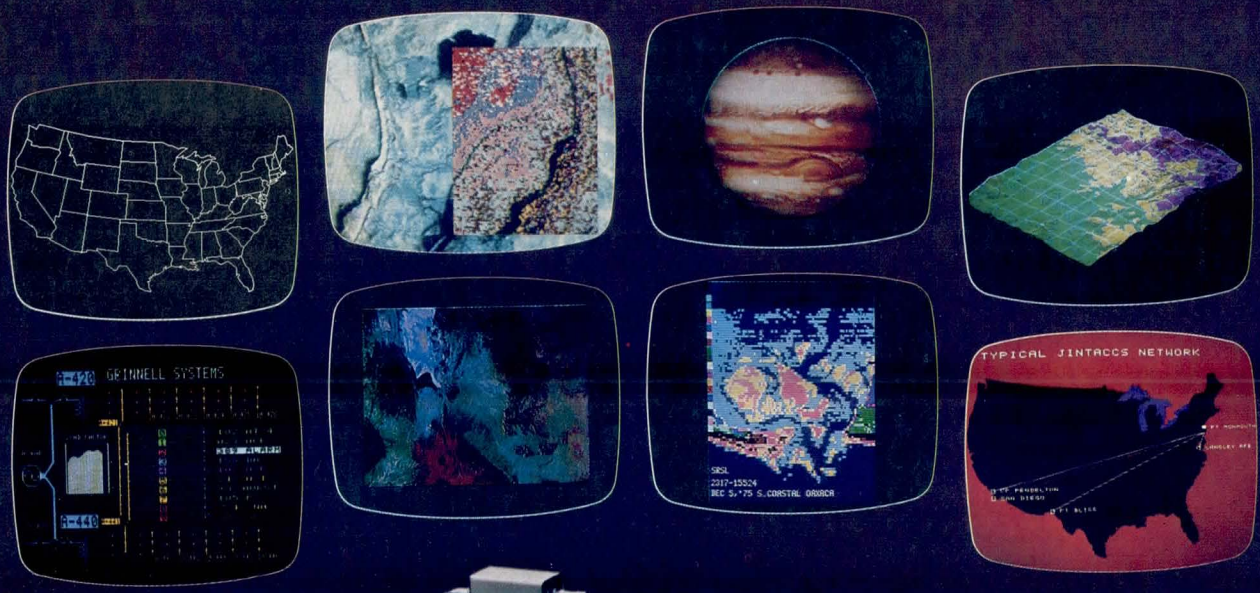

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CIRCLE 36 ON INQUIRY CARD

Peripheral Controller, Bulk Memory Expand DEC Compatible Line

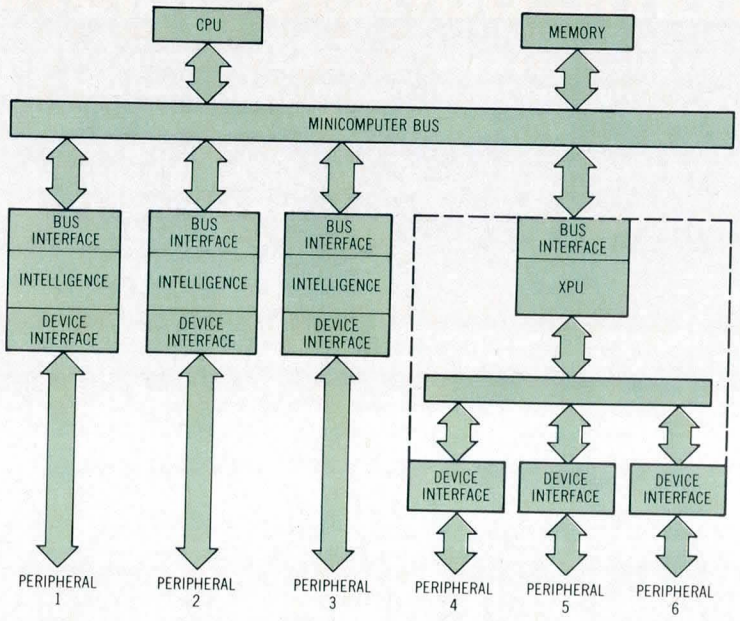
Peripheral controllers and bulk RAM memory augment the line of DEC add-in memory products available from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Hexacon is a single-board Unibus controller that is capable of simultaneously interfacing three peripheral device types: disc, tape, and bulk RAM. The controller achieves complete DEC software compatibility by emulating DEC I/O subsystems. NURAM, a bulk RAM system, offers from 2M to 8M bytes of high speed auxiliary memory and interfaces through Hexacon.

Designed to provide simultaneous I/O control of three peripheral device types, Hexacon is not three controllers on one board. It is a single microengine capable of controlling different devices simultaneously while providing software compatibility. Peripherals that can be attached to Unibus computers via the controller board include discs with SMD interface, 0.5″ (1.27-cm) tapes with Pertec interface, and the company's proprietary auxiliary RAM unit.

The controller is based on a microengine architecture called the transfer processing unit or XPU. The XPU is not an instruction processing unit; it is designed for high speed data moving applications. Featuring 2M-byte/s aggregate data transfer rate capability, the processing unit also incorporates a 4k-byte high speed RAM data buffer, achieving simultaneous multiple device type control with the same system performance as separate controllers.

The XPU's 40-bit microinstruction set, implemented with bit-slice components, is designed specifically to accommodate simultaneous control of multiple peripheral subsystems. It is much more powerful than needed, providing the ability to accommodate future high speed data rates anticipated with Winchester discs using thin film heads.

Designed for high speed data transfers, it has a 150-ns internal clock cycle and microword wide enough to simultaneously control instruction sequencing, ALU operations, and buffer transfers. Forty-eight internal registers are provided for computational tasks and buffer pointers. Large buffer areas for tape and disc are provided by 4k bytes of high speed RAM, virtually eliminating data late situations. An 8-bit internal bus allows a 6.66M-byte/s transfer rate.



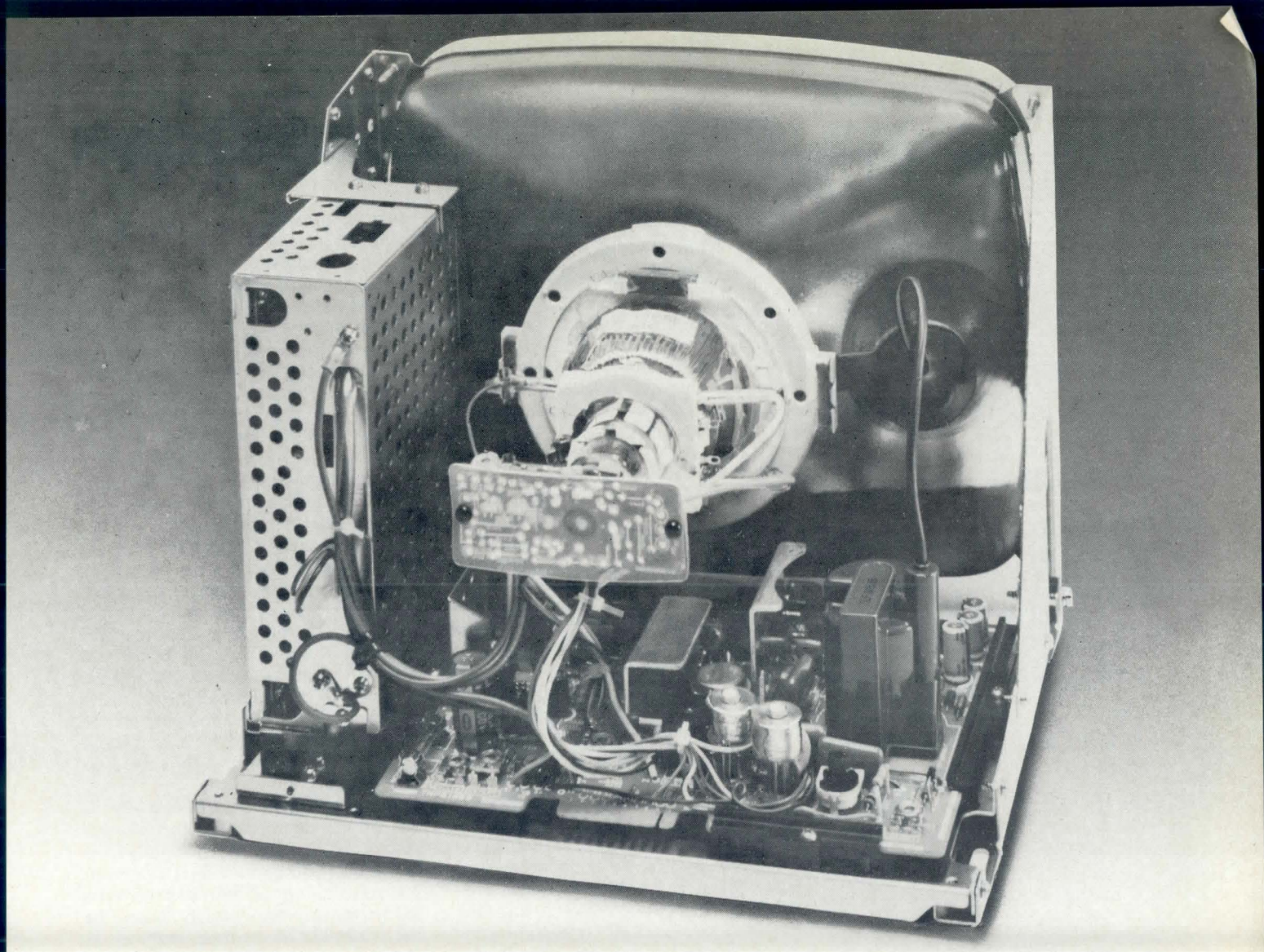
Hexacon Controller from National Semiconductor derives ability to simultaneously handle three peripheral device types from controller microengine. Bit-slice implementation with 40-bit wide microword, unit supplies 2M-byte/s aggregate device data transfer rate capability

Presenting only one Unibus load to the backplane, the controller can handle up to four 67M-byte disc drives, up to four tape drives operating at 25 in (64 cm)/s or 100 in (254 cm)/s, and up to 8M bytes of auxiliary memory. Using the controller board, a complete Unibus system can be configured in five backplane slots: two for CPU, one for 256k-byte memory, one for controller, and one for low speed I/O interface. Thus, the controller reduces total system cost in addition to simplifying spares logistics and reducing spare part inventory costs.

NURAM, a large RAM system for DEC Unibus, has built-in self diagnosis and self maintenance features. Offering from 2M- to 8M-bytes of rack mountable auxiliary memory emulating DEC's RS04 fixed head disc subsystem, the unit interfaces with systems through the Hexacon multidevice controller. Reliability and data integrity are achieved using the controller's intelligence, coupled with a data access scheme that optimizes the use of RAM as auxiliary memory. All write operations to the storage array are read back and compared automatically to verify correctness. A combination of retries and RAM substitution ensures that all data writes are completed successfully. Recovery of data employs automatic retries combined with ECC correction of soft errors to provide correct data reads. RAM substitution occurs on faulty data recovery as well as faulty writes.

When the number of spare RAMs on a memory board is reduced from ten to three, a service required light is lit, indicating that a replacement board should be ordered. If all spare RAMs on a board are used, a red light comes on, but the system continues operating without further device substitution.

Access time is specified as 2 μs; transfer rate at 500k bytes/s. All ICs in the system are per National's A+ conditioning program. Post manufacturing test includes 72-h dynamic burnin at 70 °C. A 24-h board level spare replacement program is available at $10/board/year.



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Midrange, High End Units Offer Wider Choice Within Minicomputer Family

Midrange systems models 7 and 9, and high end model 29 expand the DS990 minicomputer family, providing a wider choice of entry points and extending the hardware and software compatibility characteristics of the series. Introduced by Texas Instruments Inc, Digital Systems Group, PO Box 1444, Houston, TX 77001, model 7 uses a 990/10 central processor and a CD1400/32 cartridge disc system. Both CPU and disc mount in a pedestal that also provides additional space for optional expansion chassis or diskette drives. The cartridge disc features a total of 32M bytes of mass storage—16M in fixed disc and 16M in removable cartridge disc.

Model 9 uses the 990/10 central processor and the CD1400/96 version of the disc system—a 96M-byte cartridge disc with 80M of fixed and 16M of removable cartridge disc. This unit is also enclosed in a pedestal that provides additional space for expansion options.

The largest system, model 29 is equipped with a 990/12 minicomputer and cache memory. Mass storage is provided by the CD1400/96 disc system. This unit is housed in a 60″ (152-cm) equipment cabinet that provides space for expansion options.

In basic configurations, models 7 and 9 include error correcting disc controller, 128k bytes of memory, 13-slot chassis with programmer panel, and model 911 video display terminal. Single quantity price for the model 7 is $39,150; model 9 has a base price of $46,150. Included in a basic model 29 are error correcting disc controller, 256k bytes of memory with cache, two model 911 display terminals, and a 17-slot chassis with programmer panel. Basic price of this unit is quoted at $67,500.

Circle 351 on Inquiry Card

Software Feature Offers Low Cost Solution To Data Entry Errors

Entry Error Elimination (E^3) does away with high speed data entry errors while substantially reducing overall keyboard costs. Incorporated in the full travel membrane keyboard, developed by Oak Switch Systems, Inc, PO Box 517, Crystal Lake, IL 60014 (see *Computer Design,* Oct 1980, pp 82, 84), the method provides entry error control with a savings of 30% over most keyboards and with better reliability.

Consisting of a microprocessor based n-key rollover with phantom key lockout, the feature eliminates the possibility of entry error when an operator strikes more than one key simultaneously. The error rate resulting from rolling from one key to another is reduced by as much as 30% with n-key rollover. However, the heart of the entry error problem is the phantom key—the output of a key that hasn't even been struck. Caused when the mechanical switching that is commonly found in keyboard designs creates matrices having bidirectional current flow, phantom key results from the closing of three or more keys in a rectangular matrix, as shown in the diagram. The fourth key of the matrix is also falsely recognized and its symbol output. The mechanism that gives rise to the phantom key actually shorts out the square, and is caused by a conductive path that sneaks through the three keys that were actually struck.

This problem has been resolved by the use of an algorithm that detects and eliminates the phantom. The microprocessor reads the matrices every 3 to 5 ms (versus the 20- or 30-ms minimum interval between inputs), virtually eliminating the possibility of incorrect entry by its ability to scan and input four to six times faster than the key's closure rate.

Another technique that is used to reduce potential errors is putting all the commonly held down multiple keys, such as the shift key, on a separate matrix to reduce the likelihood of generating a phantom key. Changing the electrical layout to minimize the potential for a phantom key in neighboring keys also contributes to improved accuracy.

Circle 352 on Inquiry Card

Cache/Disc System Improves Response Time On Large Scale Systems

A cache/disc system for 1100/80 and /60 systems provides significant response time improvements. The system, announced by Sperry Univac, PO Box 500, Blue Bell, PA 19424, will enhance the productivity of current uniprocessor and multiprocessor systems.

Conceptually, the cache/disc system consists of a processor managing solid state memory interposed between the CPU and disc drives. Frequently accessed

(continued on page 58)

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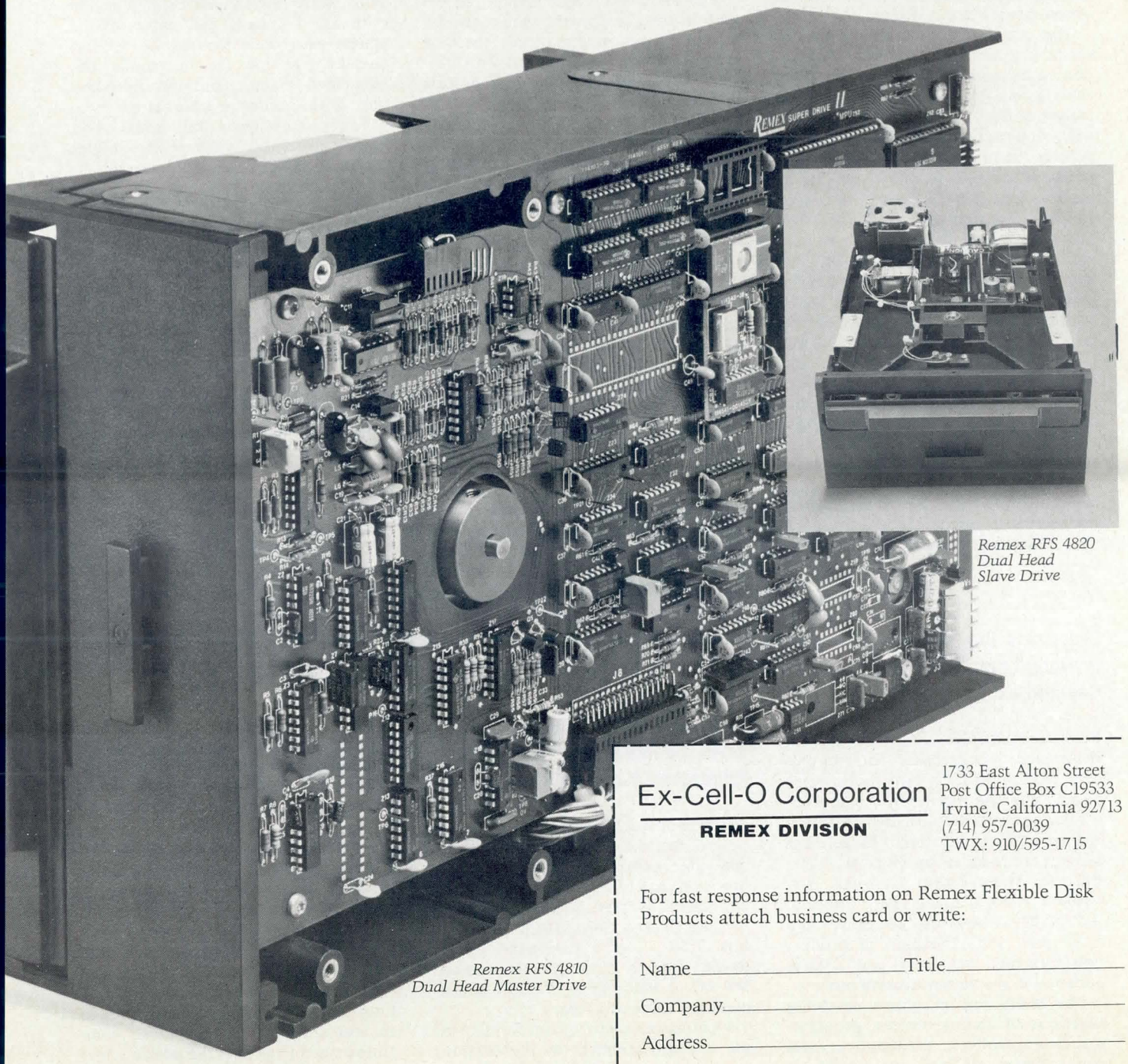

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CIRCLE 39 ON INQUIRY CARD

data are held (cached) in semiconductor memory and can be transferred to the host system without waiting for the long seek and latency time of disc drives. Although performance advantages are application dependent, simulation studies show a significant improvement over disc and drum subsystems. Mean service time (elapsed time from requesting a record on mass storage to the time that the CPU receives it) at a 75% hit rate can be two to three times faster than contemporary disc subsystems.

The intelligent 5057 cache/disc processor provides full control over operation of the cache/disc system that functions as an I/O peripheral system attached to the mainframe's word channels. Indexing, searching, buffering, storage management, staging, and destaging of data to and from disc to cache, along with extensive error recovery, are part of its functions. The 7053 storage unit uses 16k RAMs to provide capacity for 917,504 words. The storage unit can be configured as a cache memory used in conjunction with 8450 or 8470 disc units or as a solid state disc with response time of approximately 0.2 ms. Units performing these functions can also be intermixed.

Since actual data accesses are to and from the cache, it is possible to use a disc record size that is much larger than practical in a noncache disc system to obtain maximum utility from the storage device. Operation of the system is totally transparent to user level software.

Circle 353 on Inquiry Card

Batch and Continuous Process Control System Capabilities Extended

Batch and extended control systems for the microprocessor based TDC 2000 process management system boost efficiency, improve productivity and product quality, and enable better control of energy and raw material usage. The systems, introduced by Honeywell Inc, Process Management Systems Div, 16404 N Black Canyon Hwy, Phoenix, AZ 85023, provide computerized monitoring and regulation of production elements and track and control variables in the manufacturing process.

The batch control system combines functions of analog devices, programmable controllers, pneumatics, and digital computers into one system. It features sequence, logic, and modulating control, provides I/O monitoring, and has facilities that speed normal status checking and reactions to alarm situations and process interruptions.

Executing stored algorithms, the modulating control system continually measures the status of various events in a process against set points. The algorithms indicate, for example, process component changes, temperature variations, or process rate of change deviation.

The I/O monitoring function ensures that the data base used by the controller is kept current, automatically checking feedback signals and alarms. This provides improved controller and process reliability.

An enhanced alphanumeric tagging facility identifies process equipment, and an abnormal condition handling feature defines the precise action for the controller to take in correcting a process problem.

An enhanced local batch operator station improves communication between the batch controller operator and the process. The station includes a full keyboard, video screen for message display, and a tape cassette for efficient program loading and display entry.

The extended control system supplements the company's existing basic controller, managing industrial processes that require more complex control strategies. In a typical application, such as distillation column control, the system automatically coordinates the analog information (flow, temperature, level) as well as digital data (physical status of process devices, such as pumps and temperature switches).

Circle 354 on Inquiry Card

Floating Point Processor Gives Double-Precision Whetstone Value of 875k

A single-board floating point processor option for the 32-bit Eclipse MV/8000 computer increases its speed in double-precision calculations for engineering and scientific users. The FPP, developed by Data General Corp, Rte 9, Westboro, MA 01581, uses a data path that is 64-bits wide to give a double-precision Whetstone value of 875k and a single-precision value of 1150k.

Floating point instruction formats for the FPP are identical to the previous MV/8000 microcode formats, resulting in total user transparency to floating point implementations. Programs written earlier will run without modification when the option is added. Installed systems can be upgraded to include an FPP without reprogramming.

In case of a problem in the floating point unit, microcode instructions for the non-FPP instruction set can be booted into the system so that operations can continue in a slower mode, but with no downtime. This benefit derives from the system's RAM based microcode. Thus, with each system containing the optional FPP board, two copies of the system microcode instructions are included: one for the microcode implemented floating point operations and one for the hardware accelerator.

The FPP performs both single- and double-precision arithmetic. Single-precision (32-bit) calculations result in six to seven significant decimal digits; double-precision (64 bits) yields 14 to 15 significant digits. Both single- and double-precision calculations can use one or two guard digits to maintain maximum accuracy during truncation or unbiased rounding operations. Calculations over a decimal range of 5.4 to 10^{-79} are supported.

The floating point word format follows industry standard hexadecimal representation. It allocates the sign to bit 0 and the exponent to bits 1 through 7. The mantissa is contained in bits 8 to 31 (single-precision) or bits 8 to 63 (double-precision).

Circle 355 on Inquiry Card

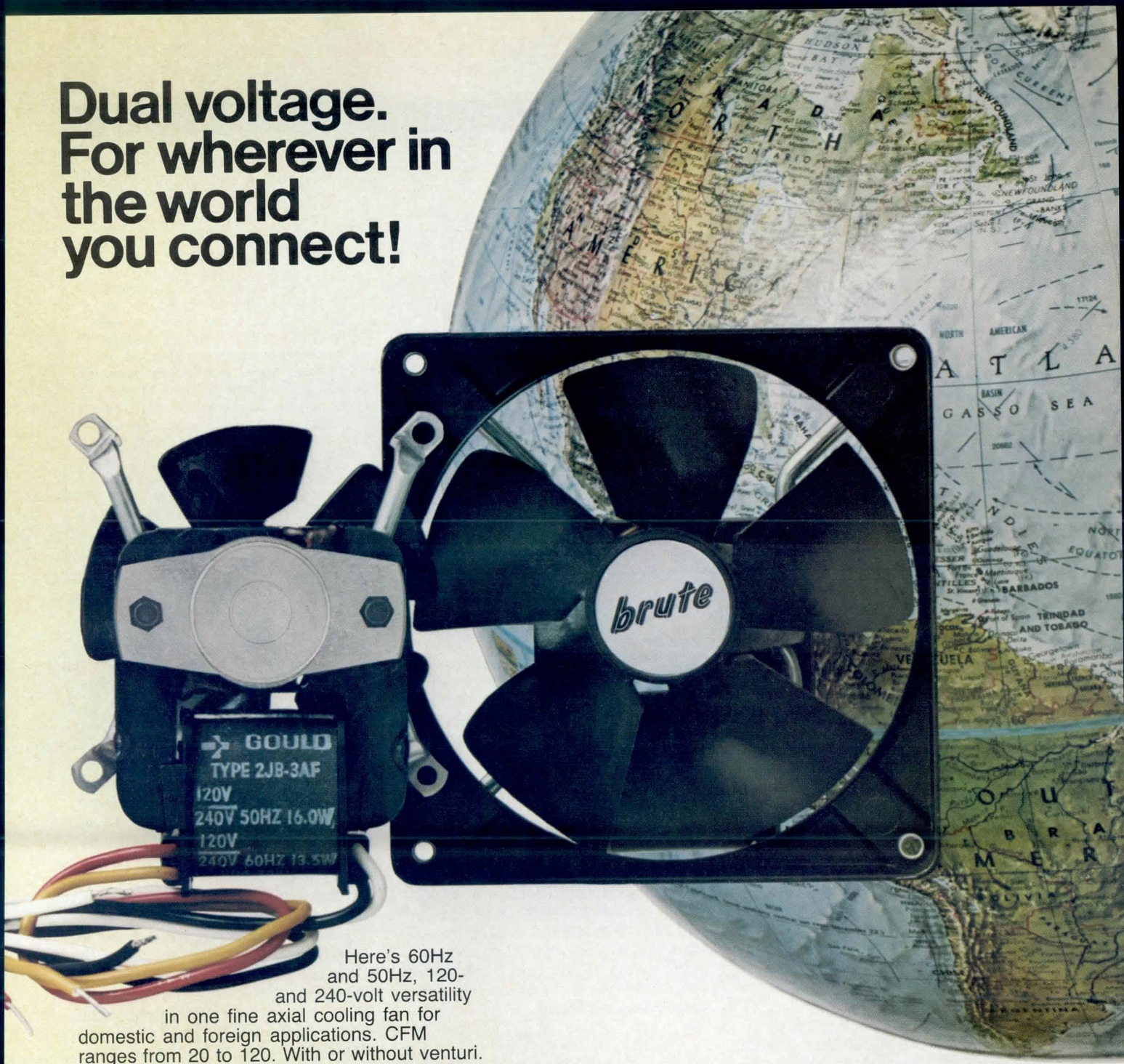
Graphics Display System Emulates IBM 3250 to Meet Needs of CAD/CAM Users

Display system model 8250 meets CAD and CAM needs by emulating IBM 2250 class graphics display equipment. In the system, Vector General, 21300 Oxnard St, Woodland Hills, CA 91367, has also incorporated features and functions of the IBM 3250 graphics display system and added features and functions that will be required by current and developing CAD/CAM programs.

Primarily, the system supports computer graphics augmented design and manufacturing (CADAM®), a CAD and CAM programming system developed by Lockheed Corp. This program resides in an IBM /370 type or compatible computing system and uses the IBM Graphics Access Method (GAM) driver designed to support 2250 class display systems.

(continued on page 60)

Dual voltage. For wherever in the world you connect!

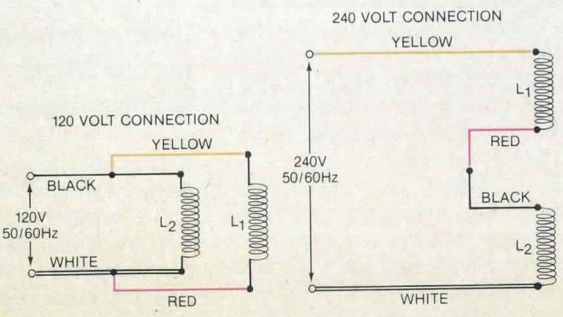


Here's 60Hz and 50Hz, 120- and 240-volt versatility in one fine axial cooling fan for domestic and foreign applications. CFM ranges from 20 to 120. With or without venturi. And a choice of three designs for mounting on $4\frac{1}{8}$" or $2\frac{13}{16}$" centers.

All from a top name in electric motors for just about everything—Gould. These Brutes feature Gould's open frame design and patented Recirk™ bearing lubrication system for extended life.

Metal parts are coated with a corrosion inhibitor and only flame-retardent plastics are used. U.L. recognized and CSA certified. Special modifications can be designed in.

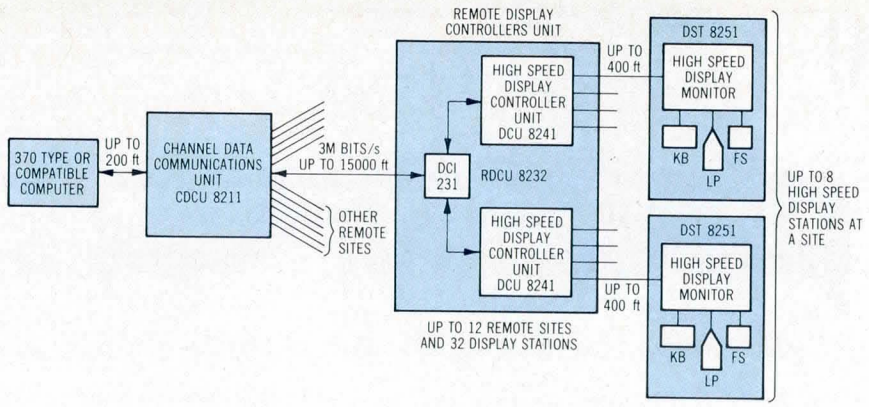
For more details or to order these inventory-reducing fans, call (315) 788-5530. Gould Inc., Electric Motor Division, 6393 Coffeen Street, Watertown, NY 13601.



GOULD

An Electrical/Electronics Company

CIRCLE 40 ON INQUIRY CARD



Enabling as many as 12 remote display stations to be located as far as 3 mi from host, Vector General's 8250 graphics display system provides channel speed of 1.2M bytes/s. System emulates IBM 3250 class graphics display equipment and provides features necessary to support future CAD/CAM software packages

However, it can be used in any environment where user application programs have been designed to run on those computers and software driver.

Channel speed of up to 1.2M bytes/s and operation of selector, block multiplexer, or byte multiplexer in real mode produce a system that can effectively support 32 terminals. Internal bus architecture enables more sites to be supported without sacrificing bandwidth. Furthermore, the 3M-bit/s communication line allows eight terminals at a site to be supported without degradation in display station response. Parallel microprocessors and buffering allow high speed data transfer across the system, and allow flexibility in adding features and enhancements as well as built-in diagnostics.

The architecture of the system is designed modularly to fulfill all criteria. It consists of a number of major components. The channel data communications unit (CDCU 8211) provides communication with the channel on one end and up to 12 communication lines on the other. Commands and data are processed by the unit and transmitted in a serial fashion down a low cost, user supplied coaxial cable, 3M-bit/s line, to as many as 12 remote sites.

The remote display controllers unit (RDCU 823X) is basic remote site hardware that supports the 3M-bit/s line at the site and issues commands and data to two display controllers plugged into its chassis. Two versions of the unit support either one or two controllers. Commands and data are acquired, processed, and output to a display station by the display controller unit (DCU 824X), which includes all necessary control hardware to support the standard display station configuration. One controller version supports four high speed stations; another supports two medium speed stations. The operator display station includes the monitor and function switch box, keyboard, and light pen. Both high speed and medium speed models are suitable for CAD/CAM applications.

The system is capable of linking sites more than 1 to 1.5 mi away without degradation in system response. Users can start with a small configuration consisting of CDCU 8211, RDCU 8232, DCU 8241, and 2 to 4 DST 8251s and build on by adding more DCU/DSTs and RDCU 8232 sites. A 32-station/12-site configuration can be spread across a radius of up to 3 mi.

Circle 356 on Inquiry Card

Desktop Computer Graphics System Offers Economical IC Mask Design

IC Designer is a 2-dimensional standalone system that is compatible with major computer graphics and analysis systems. The high quality desktop computer graphics system for IC mask design and schematic entry concentrates exclusively on the initial design process, relegating subsequent functions such as design rule checking, layout verification, and pattern generation to a service bureau or separate inhouse computer.

The system, developed by Avera Corp, 340 El Pueblo Dr, Scotts Valley, CA 95066, consists of video display, electronics and mass storage unit, and keyboard and mouse data entry units. Control of the system is accomplished by using either the input mouse or a keyboard. Assisting in rapid input are onscreen menus, symbol recognition (user definable), split screen with full text response, grids for freehand input, user written macro support, selective erase, master library of nested cells, natural units data structure, and function keys.

Primary graphic input is through the mouse—a device which the user rolls along any surface to move the cursor on the screen. The device can be used to indicate drawing items for graphic input, or to select various functions by positioning the cursor in any of the 24 onscreen boxes, select specific functions from the alphanumeric section, or draw a command symbol. In addition to its obvious use for entering and editing text, the keyboard has 14 user programmable function keys for command execution. It can also be used instead of the mouse for entering graphic information. In this case the user types numerical coordinates.

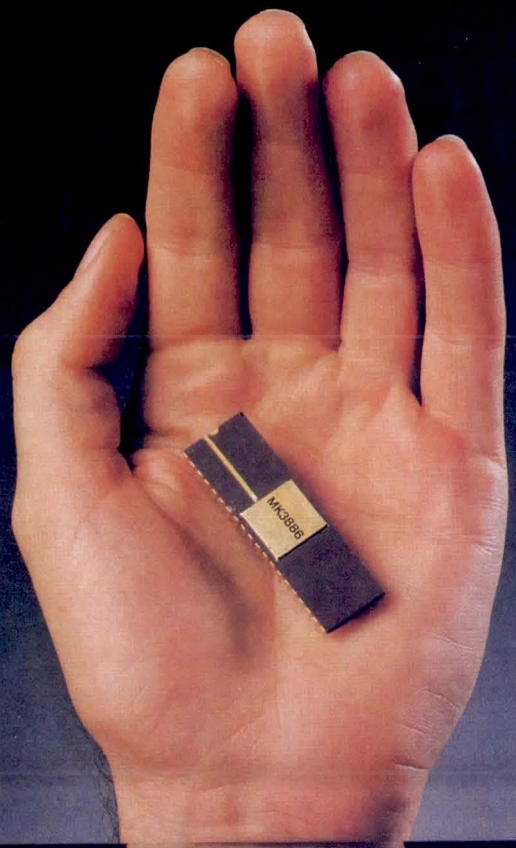
A high resolution raster display allows the designer to use one display for both alphanumeric and graphic functions and enables each area to be updated individually. The graphic area provides selective erase of any graphic input. The combination provides true interactive operation in a personal/desktop package.

(continued on page 63)

Z80 COMBO CHIP

Four functions in one reflects design simplicity at its best.

MOSTEK®



A serial I/O port. 256 bytes of RAM. Two programmable timers. Three external interrupt channels. Now you can get all of them in one integrated circuit: The MK3886 Combo Chip from Mostek.

This 5-volt only, 40-pin DIP is design simplicity at its best. The kind that means superior cost efficiency, fewer parts count, less board space, and higher reliability. With just three chips (Combo, Z80 CPU and Memory), you can configure a variety of highly versatile Z80 systems.

A sampling of application examples: As an intelligent remote data logger. Or an interrupt driven intelligent peripheral controller. Or an industrial security system with serial interface. Or as a building block in a "two-way" cable TV network. Or for a patient monitoring system. That's the versatility of the Combo Chip. In fact, no other chip simplifies Z80 design so efficiently. Find out why. Contact Mostek, 1215 West Crosby Road, Carrollton, TX 75006 (214) 323-1801. In Europe, contact Mostek Brussels 762.18.80.

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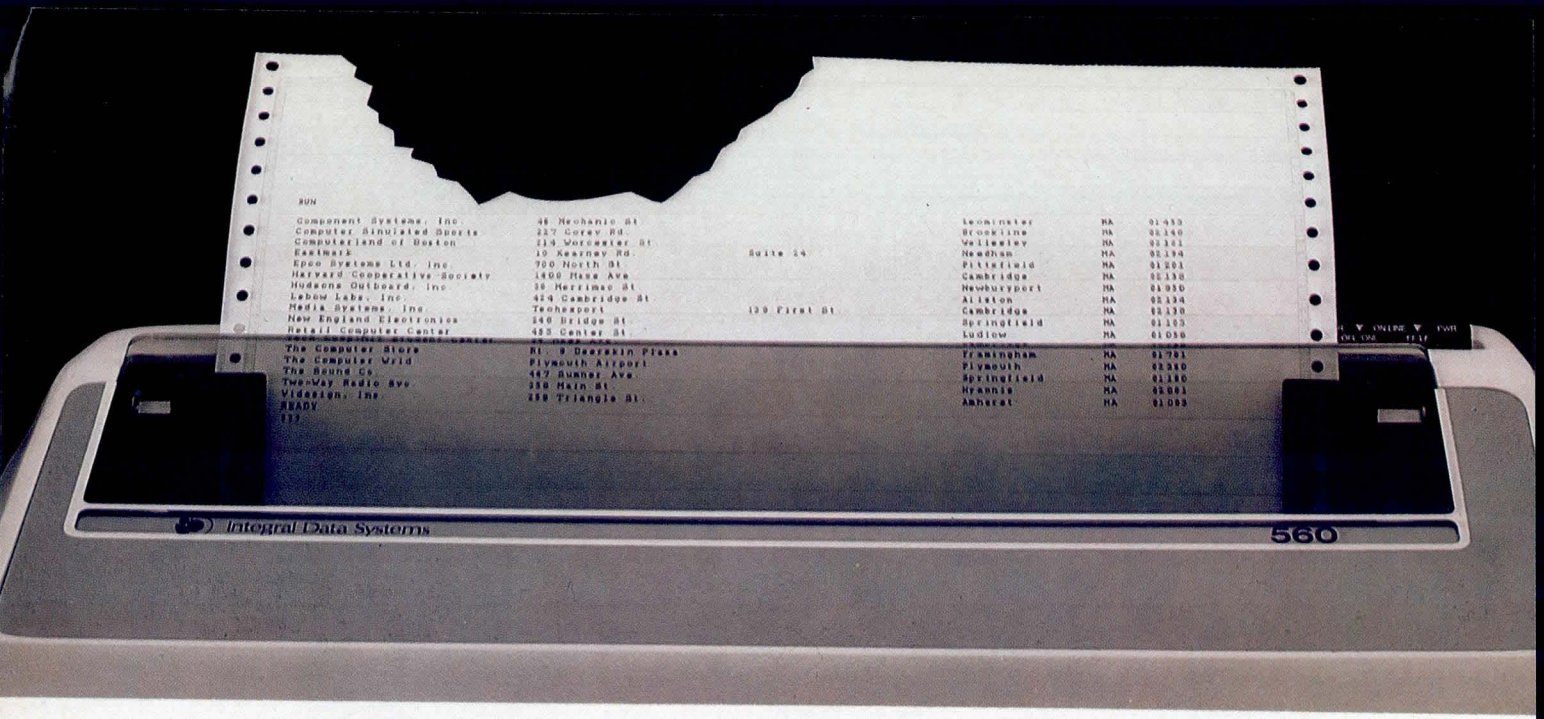

Meet the Tiger with a bigger bite.

Introducing the remarkable 132-column Paper Tiger™ 560. The first full-width matrix printer to give you fully formed characters for a low $1695.*

The new 560 features a staggered nine-wire ballistic type print head that overlaps dots in both horizontal and vertical planes. It bi-directionally prints up to 150 dense, text quality characters per second.

The 560 also features a reliable cartridge ribbon that lasts up to four times as long

presents a breakthrough in matrix printin
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creates high quality printouts by overla

Paper Tiger 560 Print Sample

as spool and cassette ribbons, separate heavy-duty stepper motors to drive the print head and advance the paper, plus true tractor feed.

And famous Paper Tiger performance comes with every new 560. Like fixed or proportionately spaced text, programmable tabbing and business forms control, automatic text justification, print formats to 220 columns, parallel and serial interfaces, self-diagnostics, and more. All inside the most compact printer of its kind.

Need more stripes? Dotplot,™ our high-resolution raster graphics package, is standard on every 560.

For data processing, word processing and small business applications, this is your Tiger. The business-sized Paper Tiger™ 560.

It's a Tiger you can count on.

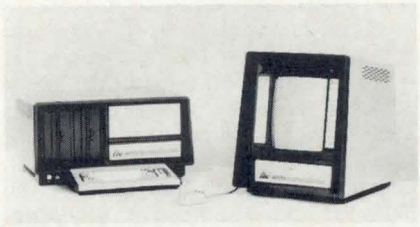
Call TOLL FREE 800-258-1386 (In New Hampshire, Alaska and Hawaii, call 603-673-9100.) Or write: Integral Data Systems, Inc., Milford, NH 03055.

Paper Tiger 560

Integral Data Systems, Inc.

*Suggested single-unit U.S. price. Very generous OEM discounts available.

CIRCLE 42 ON INQUIRY CARD



Standalone computer graphics system from Avera offers IC mask design and schematic input through "mouse" or keyboard, and provides high resolution raster display with grid structure of 64k resolvable points on each axis

The grid structure within which the user works has 64k resolvable points on each axis, and can handle designs with up to 64 layers. Area shading and outline patterns can be selected to help differentiate between layers. For repetitive design elements, graphic cells can be created and then nested in larger cells, with 16 levels of nesting available. All graphic elements can be manipulated (added, deleted, rotated, mirrored) with either the mouse or the keyboard. Software handles details of these manipulations.

A recursive data structure provides the ability to form "hard" associations. For example, a line can be associated with a symbol so that, if the line is later moved, the symbol cannot be inadvertently left behind. A powerful UNDO command withdraws the last command executed. Data can be formatted so that it is directly read by other graphics systems. Data can be transferred through communications links or by magnetic tape, allowing the designer to interface to existing systems.

A dual-density diskette storage system with 1M-byte capacity provides enough storage for approximately 1000 transistors in a drawing. Normally, a drawing and its backup are held on one diskette. In the case of a highly repetitive design, the drawing could contain information in cell form for the entire circuit.

Available as system options are an 11 x 11" (27 x 27-cm) tablet input device, a magnetic tape drive, compact hardcopy unit, and 10M-byte Winchester type drive unit for extended storage. Documentation and comprehensive training programs, along with technical and maintenance support, are supplied in the customer support package.

Circle 357 on Inquiry Card

ZIATECH'S GPIB controllers

With Ziatech's ZT85/38 general purpose interface bus, the possibilities are endless. Since our GPIB meets IEEE standard 488, you can interface more than 800 instruments and peripherals.

Ziatech gives you the freedom to build your own μP-based automatic test system. Get all of those GPIB instruments off the shelf—and onto the table.

THE COMPUTER-TO-COMPUTER COMMUNICATOR. Our ZT85/38 controller handles computer-to-computer communications at 250k bytes/sec. That kind of performance makes the RS 232C look like a slouch.

EASY TO DESIGN WITH. Everything you need is on a single board. That can end your spare parts' "float" forever. We'll help you cut design and documentation time, too. And you'll only need to learn a single protocol for system interface.

SELF CONTAINED AND LOW COST. The ZT85/38 is completely self-contained. Plus, you get 8k bytes of dual-ported RAM for buffering. Or for general use. You also get Ziatech reliability. We've put each board through 168 hours of grueling burn-in at 55°C.

CHECK OUT OUR ZT80 GPIB CONTROLLER, TOO. Our ZT80 gives you almost all the same features of the ZT85/38. Including MULTIBUS compatibility. It's the perfect board to specify for applications that call for 1k bytes RAM. And it costs even less than the ZT85/38. Whichever choice you make, *either board costs less than one engineering week of design time.*

LET US HELP TAKE THE GAMBLE OUT OF MULTIBUS CONTROLLERS TODAY. Contact Bert Forbes at Ziatech—(805) 541-0488 for full information.

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2410 Broad Street, San Luis Obispo, CA 93401 (805) 541-0488

CIRCLE 43 ON INQUIRY CARD

M-Series Expansions Include High Speed Processor, Operating System Software

Expansions of the M-series revealed by Hitachi, Ltd, No 5-1, 1-Chome, Marunouchi, Chiyoda-ku, Tokyo, Japan, include the M-280H processor, the largest in the series, and the compact high speed M-240H processor. Also announced were a variety of software programs mainly in connection with the VOS3 (virtual storage operating system 3).

A high speed processor that can be equipped with a maximum of 32M bytes of main storage capacity and 32 channels, the M-280H provides 3.5 to 4.0 times the internal processing speed of the M-180. Total system performance and time sharing system response performance have been improved through the larger main memory capacity and the throughput achieved using 32 channels.

High density packaging in the unit is achieved using ECL LSI circuits having 1500/550 gates/chip. Features include high speed arithmetic, pipeline control, and distributed microprogram control. With the optional integrated array processor, the speed for performing scientific calculations can be increased by a factor of 4, compared with a system without IAP.

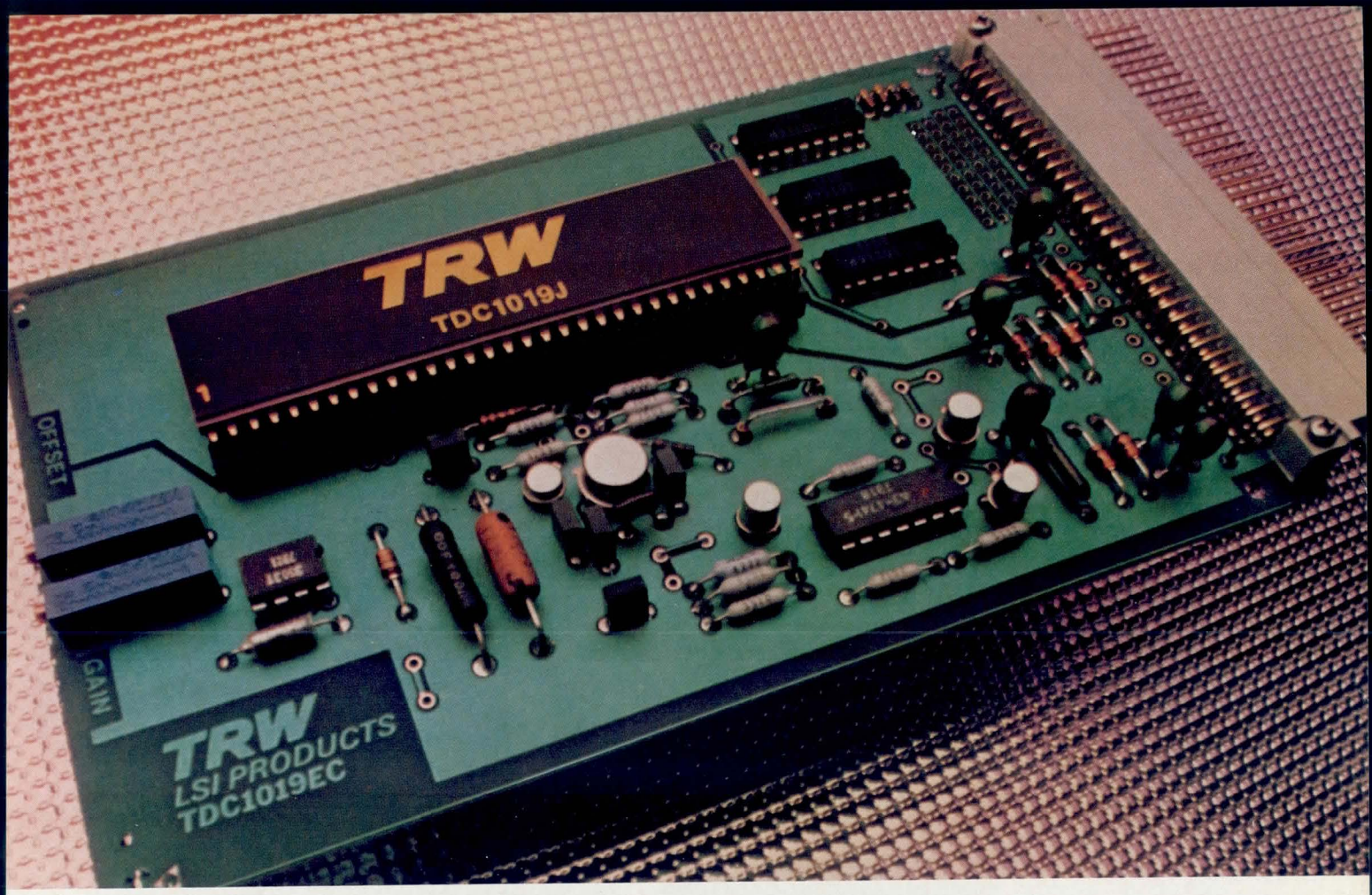
Main memory is formed of 16k-bit MOS RAMs and has a capacity in the range of 16M to 32M bytes. Buffer storage capacity of 64k bytes is provided. From 8 to 32 channels incorporated in the unit offer a total throughput of 90M bytes/s. Multiprocessor configurations having from 2 to 4 processors are possible.

The compact M-240H processor has internal processing speed three to four times greater than an M-16011 processor. A console service processor (separate from the central processor and incorporated within a console) is standard on this unit. Main memory with capacity for 2M to 8M bytes is formed using 64k-bit NMOS RAMs. Buffer storage capacity for 32k bytes is also provided. Total throughput of 16M bytes/s is obtained on the unit's 5 to 8 channels.

Operating systems for the units include VOS3/SP, VOS2/ESO (240H only), and VMS/ESO (240H only), in addition to the existing VOS3, VOS2, and VMS. The VOS3 is also available with data communication and control manager, high speed database manager, adapter for transaction management, practical data manager, and available command language for end users. Other programs include library management and editing system, Extended COBOL, COBOL debugging aids, FORT 77/source analyzing facility, compile and go FORTRAN 77, and APL/business graph feature. Distributed or network processing functions are supplied using extended communication support/virtual telecommunications access method/BASE, ECS/VTAM/multisystem networking facility, ECS/network control program, network terminal interface program, network job entry, distributed system manager/host, and host command control facility/host packages.

Circle 358 on Inquiry Card

CIRCLE 44 ON INQUIRY CARD



No Competition.

Now a monolithic 9-bit 40 nsec A/D converter. Just $585.

TRW presents the state of the art.

Now, there's a monolithic 9-bit 40 nsec A/D converter for only $585 in hundreds. TRW technology gives you the edge: Up to 10-1 power reduction over other video-speed A/D converters, and more than 2/3 size reduction; conversion up to 25 megasamples per second; highest reliability and stability; wide temperature range performance.

Using the TDC1019J is simplicity itself. A convert signal strobes 511 comparators, encodes all their binary outputs into a 9-bit word, and stores the word in an output latch. Unlike other types, our converter needs no sample-and-hold circuit. It works as a *flash converter,* and doesn't depend on tedious successive-approximation techniques. (And it's ECL compatible.)

Our new A/D converter is also available on its own standard 100 mm x 160 mm evaluation board (TDC1019EC). It's fully assembled and tested, equipped with a universal 64-pin edge connector. Using -5.2V and ± 15V power supplies,

the board accepts and digitizes a 1-volt peak-to-peak signal from a 75-ohm source . . . at up to 25 megasamples per second.

Price for converter and evaluation board is $885. In hundreds, just $685. (Converter only, $785. In hundreds, $585. If you order only the converter, we'll enclose the pertinent data sheet/application notes to help you evaluate it on your own.) Prices are U.S. prices only.

Any way you order, you can order with confidence and the knowledge that TRW has more experience than any other company in the design and production of high speed monolithic A/D and D/A products. (Remember our 8-bit converter? It was revolutionary then. It's now the industry standard.)

Give yourself and your company the TRW edge. Order the no-competition TDC1019J. On the board or by itself. Now in stock at Arrow Electronics and Hamilton/Avnet.

For immediate information, call 714-578-5990, or send in coupon, or just attach your business card to this ad and mail it to us.

TRW LSI Products P.O. Box 2472, La Jolla, CA 92038

Please send data sheets on the **TDC1019EC** and **TDC1019J** 9-bit A/D converter.

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TRW LSI PRODUCTS

An Electronic Components Division of TRW Inc.

TRW keeps you ahead in video speed data conversion.

CIRCLE 151 ON INQUIRY CARD

SIEMENS

Maxi-Mini™ 5¼" floppies score with immediate delivery.

Sports or business—winning demands quick reaction. That's what you get when you turn to Siemens for 5¼" Maxi-Mini drives, available for immediate delivery. You can count on Siemens drives for long-term reliability—and on the Siemens team for prompt service and total technical support.

Siemens 5¼" floppies feature anti-crunch diskette protection, precision metal lead screw for track-to-track head positioning, plus 20 ms step time. 125k byte capacity with 40 tracks; 500k byte capacity with 80 tracks. And industry compatibility.

When you turn to Siemens, you turn to the world's 5th largest electronic/electrical engineering company—which backs our team with more than $6 million in R&D each working day. In the U.S. alone, Siemens employs more than 12,000 people in 15 manufacturing plants, two R&D facilities, and sales/service offices covering all 50 states.

Siemens—high technology with highly competitive pricing. Just ask for a quote and see for yourself. Find out how Siemens responds to your floppy disk needs. Call Barrie Clark at (714) 991-9700.

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Siemens: Engineering Winning Drives.

CIRCLE 153 ON INQUIRY CARD

A Brilliant New Graphics Terminal from Genisco

Raster brilliance, contrast and erasability. Z-8001 intelligence plus programmability. All in a desk top, high resolution (1024 x 792), monochrome, graphics terminal ticketed at a low $10,000.*

Genisco's G-1000 is the low cost graphics terminal you've been holding your purchase order for. It is the first direct raster replacement for the Tektronix 4014-1** terminal—plug to plug and software compatible. But, at the same time, the on-board Z-8001 microprocessor plus 16K words each of RAM and PROM let you develop your own programs at your pace while your system is up and running on existing software (like PLOT-10).

Because the G-1000 is a bit map raster scan device it can do things a storage tube can't approach—like provide easy viewing in normal room light, and allow erasure of any portion of the screen without altering or redrawing the rest of the display. Genisco has equipped the G-1000 with all the quality features—60Hz noninterlaced refresh for flicker free viewing, a large 19 inch display, a detachable keyboard with cursor joystick. And, an optional alphanumeric overlay eliminates the need to use a second terminal. The unit supports a selection of I/O equipment including graph tablet and hard copy devices. With all that and the Z-8001 intelligence, the list of future capabilities is virtually open-ended.

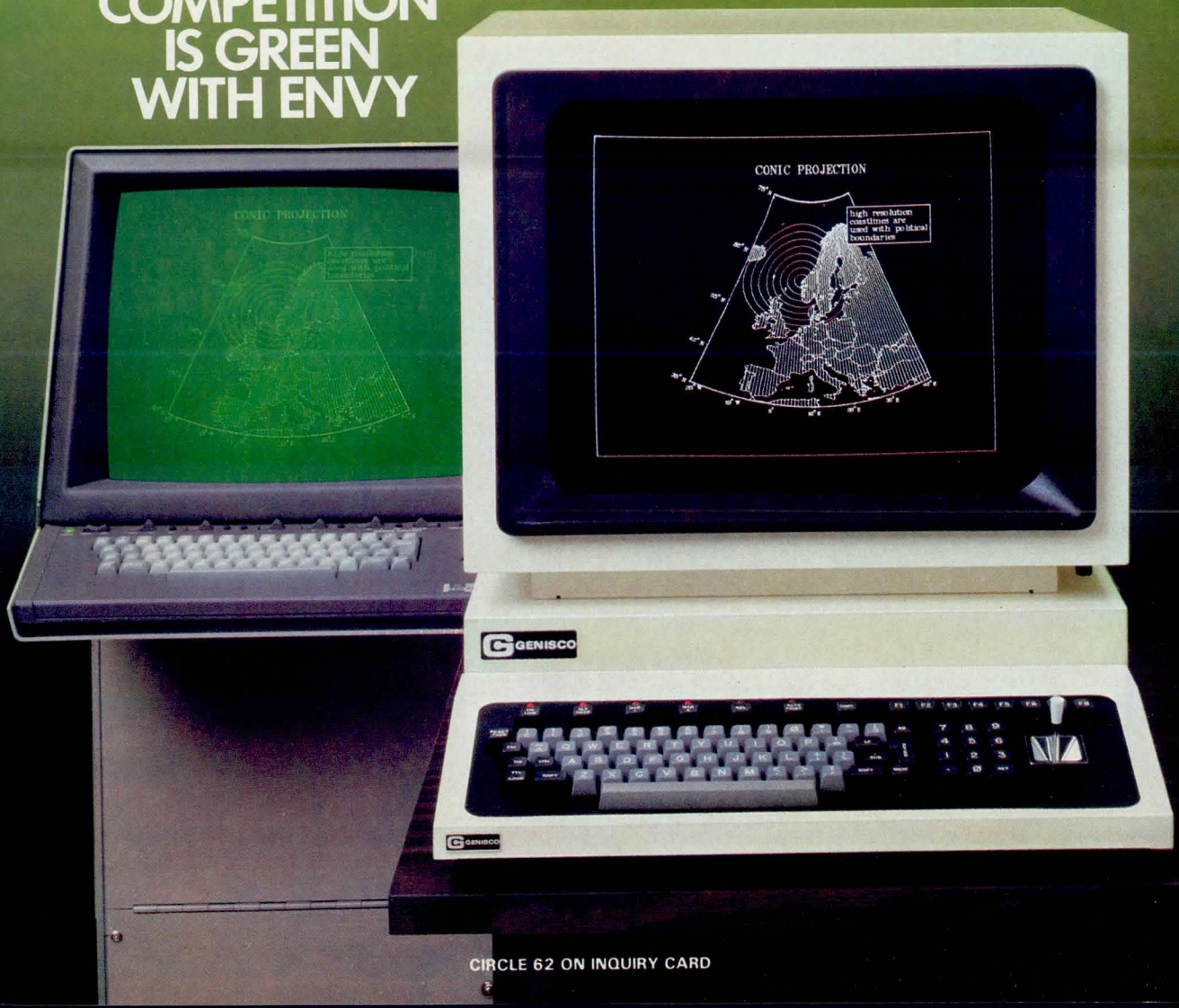
Take a look at Genisco's new G-1000—the 4014-1 replacement and a whole lot more.

Call or write for more information to Genisco Computers Corporation, 3545 Cadillac Avenue, Costa Mesa, California 92626. (714) 556-4916.

*Price varies according to quantity.
**Trademark of Tektronix
Graphics software from ISSCO Graphics.

Genisco

THE COMPETITION IS GREEN WITH ENVY



CIRCLE 62 ON INQUIRY CARD

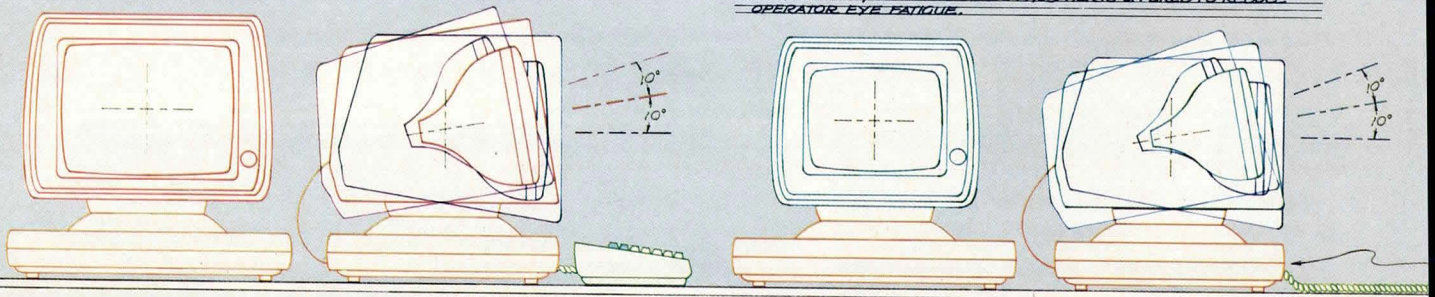
THE ZENTEC SERIES 8000 INTELLIGENT TERMINALS

The first Intelligent Terminal designed specifically for OEMs to configure and for people to use.

THE ZENTEC 8002 IS A COMPLETE INTELLIGENT TERMINAL COMPRISED OF THREE SEPARATE MODULES, THE 8201 LOGIC BOX, THE 8302 (15") VIDEO MODULE AND THE 8401 KEYBOARD.

WITH THE 8002, THE 15" CRT IS BALL-JOINT CONNECTED TO THE TOP OF THE LOGIC BOX AND PROVIDES A CONVENIENT 20° ANGLE OF TILT AND A 60° ANGLE OF SWIVEL.

THE ZENTEC 8001 IS SIMILAR TO THE 8002 WITH THE SUBSTITUTION OF A 12" VIDEO MODULE, THE NON-GLARE, HIGH RESOLUTION CRT SURFACE WITH A WHITE, GREEN OR AMBER PHOSPHOR IS OFFERED TO REDUCE OPERATOR EYE FATIGUE.



With the Series 8000, Zentec successfully re-defines the words Human Engineering. Never before has there been a more powerful, more flexible, more operator-oriented video display terminal designed expressly for OEMs and system integrators.

The first thing you see on the CRT is the almost completely glare-free surface for reduced operator eye fatigue. The single knob right up front is used to turn the system on or off and to control the level of brightness. While a P31 green phosphor is standard, white or amber phosphors may be optionally provided. Character resolution and contrast go easy on the eyes, too, and wait until you see the character size on our 15" screen!

Configurability AND Flexibility

With Zentec's unique multiple-module concept, the 8000 may be easily configured with either a 12- or 15-inch CRT with full swivel and tilt, up to three snap-in printed circuit boards in the logic box for fast MTTR, and a wide variety of detachable keyboard styles. A single PCB is standard with the 8000, and the OEM may add one or two of his own PCBs. The standard logic contains Zentec's unique mini-computer-like bus architecture under the control of a powerful microprocessor. Hardware for synchronous or asynchronous communications and printer I/O is standard. The Zentec 8000 may be configured with 16, 32, or 64KB of RAM and 4, 8, 12, or 16KB of ROM or PROM. That's flexibility!

The microprocessor-controlled detached keyboard of the 8000 is canted 11° for operator comfort and the keys may be stepped, or optionally, sculptured.

Through Zentec, all OEMs can now offer a unique private label product so finely tuned to their customers' needs that it achieves the highest level of man-machine interface. For the direct story on the Zentec 8000, call us at (408) 727-7662, or write for our brochure.

ZENTEC

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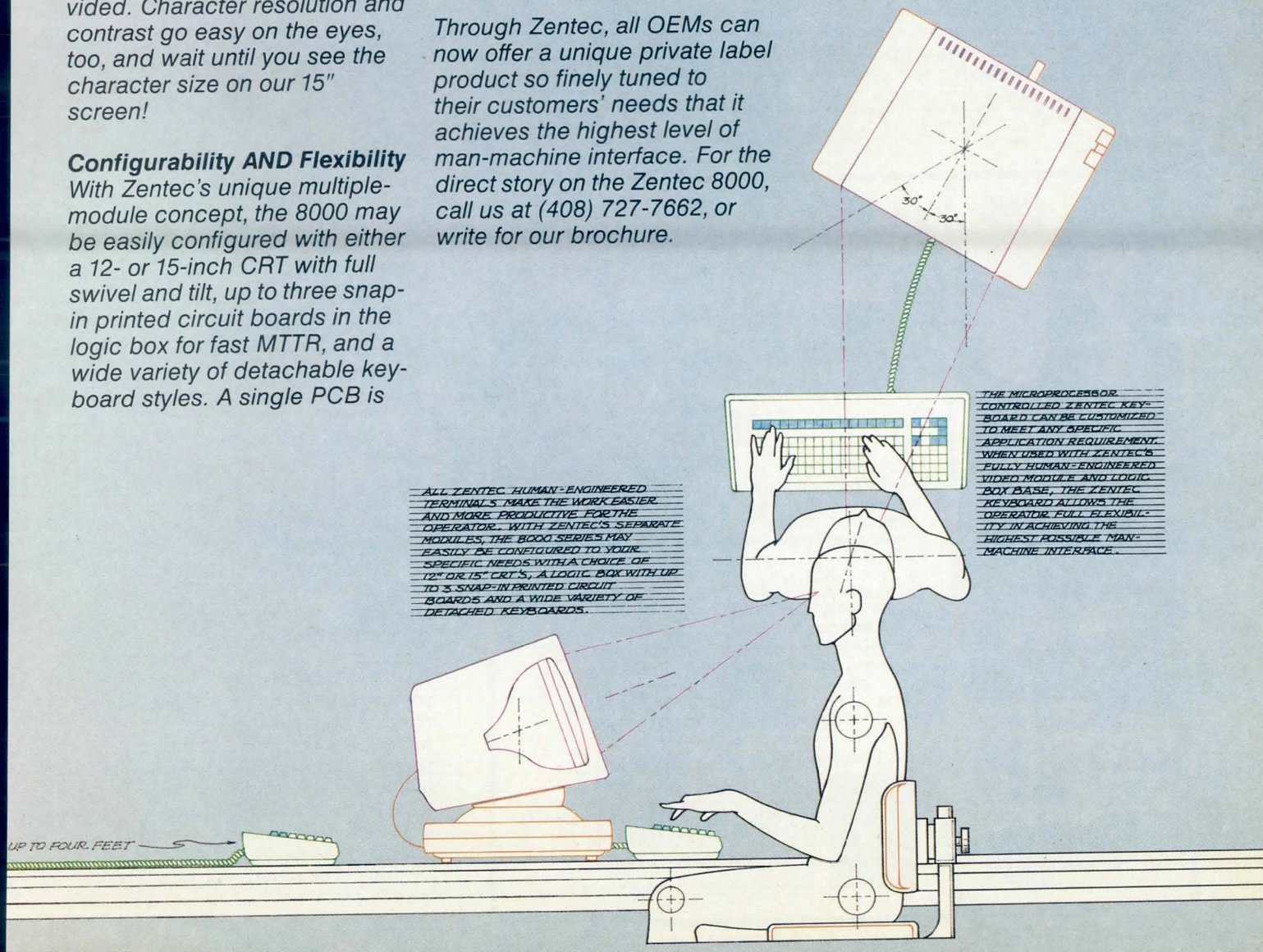

CIRCLE 157 ON INQUIRY CARD

Small Business System Offers Increased Speed, Wider Storage Capacity Range

The 1550, a small business computer that features increased processor speed and greater diskette storage capacity, can serve as a standalone computer or as a component of a telecommunications network. The low cost desktop processor, from Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, can perform both roles at the same time by using a concurrent operations feature.

Derived from the existing 1500 system, the 1550 is built around the higher speed Z80A micrprocessor chip; this gives it significantly greater processing speed than its predecessor, which used a Z80 chip. The processor includes 32k, 64k, or 96k of memory. Its concurrent job feature allows printing or communications tasks to be performed concurrently with processing. A built-in communications interface allows automatic call answering when attached to a user supplied modem.

The typewriter style keyboard includes special function keys, and the video display screen provides inverse (dark on light) characters. The system can be configured with double-density diskette drives, in either single- or double-sided versions, offering a choice between 1M- or 2M-byte drives. It supports up to three extension drives, providing up to 8M bytes of diskette storage on one processor. A processor with 64k of memory can support a 9310/9320 10M-byte cartridge drive, allowing still greater storage and faster accesss times. The 9310 consists of a disc drive and controller, while the 9320 includes disc drive, controller, and 4-terminal serial interface that allows the processor to serve as CPU in a 4-user DATASHARE timesharing business system. Addition of three extension drives means that one processor can support up to 40M bytes of online disc storage.

The system supports the DATABUS business programming language, as well as FORTRAN and BASICPLUS. Word processing and electronic message services can also be performed. The machine can be used for interactive IBM mainframe communications using the EM3270 software package. Software for IBM batch communications, 2780/3780, is also available.

Base price for a 1550 with 32k memory and a 0.5M-byte disc drive is $7075. The 1M-byte version costs $8075, while the 2M-byte unit is priced at $9075. With 64k memory and 9310 hard disc, the unit sells for $18,250; with a 9320 drive it has a tag of $18,750.

Circle 359 on Inquiry Card

MODULAR ELECTRONIC CABINETS – DESKS and CUSTOM INSTRUMENT PANELS

EQUIPTO ENCLOSURE SYSTEMS — first in choice for excellence! Hundreds of standard sizes available in both our top-of-the-line Heavy Duty Modular Cabinets and the value-engineered Challenger/Solid System line. We also offer a totally new Electronic Desk System in a variety of styles. And since every electronic equipment company is unique and has different enclosure needs, we'll modify our cabinets to meet those requirements.

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Entry Level System, Support Assist Features Extend Mainframe Family

AS/9000N is an entry level system with a 4M-byte, 6-channel minimum configuration that provides 2 to 2.4 times the processing power of the AS/7000 system. This addition to the AS/9000 series, from National Advanced Systems, 800 E Middlefield Rd, Mountain View, CA 94040, is field upgradable to the /9000, which provides 2.5 to 3 times the power of the /7000.

In addition, the system provides enhancements announced recently for the /9000 and /9000DPC. These include expansion of main memory to a maximum of 24M bytes in 4M-byte increments for greater performance when running IBM MVS operating systems. Extended channel capability allows all but one channel to operate as block multiplexer channels capable of supporting data streaming protocol. Data streaming will be available late this year without extended channel capability for a maximum of six channels and for all block multiplexers with extended channel capability. MVS/SP assist hardware and microcode provide improved performance when running MVS/SP release 3 and subsequent releases. This feature is similar in function to the 3033 extensions feature.

Minimum configuration is priced at $1,995,000. Additional main memory is priced at $140,000 in 4M-byte increments. The system will be available late this year.

Circle 360 on Inquiry Card

CIRCLE 152 ON INQUIRY CARD

The new Spectra-Strip 817 is the IDC D-Subminiature connector for those of you who have become disenchanted with D-Sub's.

With our D-Sub, you can now mass terminate your flat cables without separating each and every strand. Without stocking up on weird-pitched cable. Without a mechanical kluge tacked onto the back of the connector to go from .054-pitch pins to .050-pitch cable.

It terminates our Twist 'N' Flat,® 3C™ Color Coded and that great old standby Spectra-Zip™ cables with no fuss, no hassle.

And only the Spectra-Strip 817 D-Sub connector comes with a metal shell so that it's *fully* intermateable and intermountable with any of the other real D-Sub's.

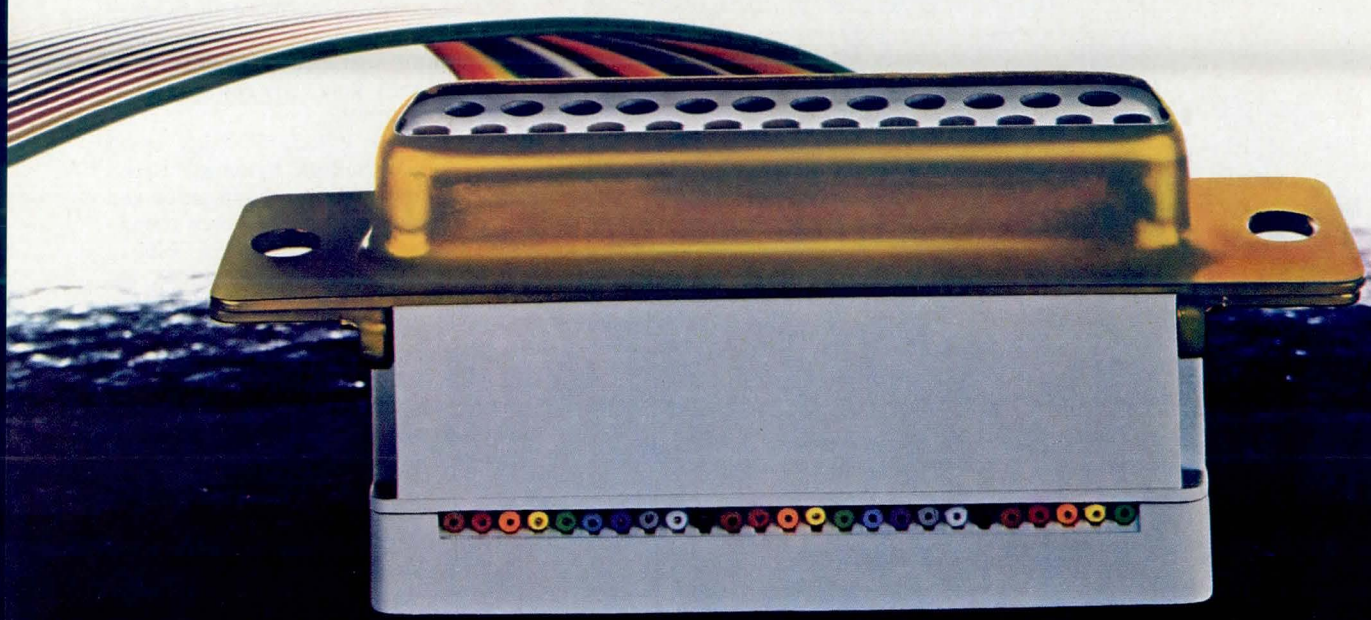
If that sounds like the way to build a D-Sub, call your nearest Spectra-Strip distributor for off-the-shelf delivery. He can also tell you about what we've got for you in our other IDC connectors, flat cable and assemblies.

They're simply superb.

Spectra-Strip, 7100 Lampson Ave., Garden Grove, CA 92642, telephone (714) 892-3361 and 720 Sherman Ave., Hamden, CT 06514, telephone (203) 281-3200.

In Europe, Spectra-Strip, Ltd., Romsey, Hampshire, England, telephone (0794) 517575.

D-Suberior.



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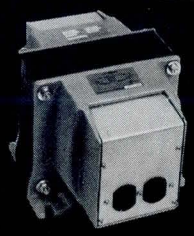
When you're down to the wire.

Allied Chemical

CIRCLE 128 ON INQUIRY CARD

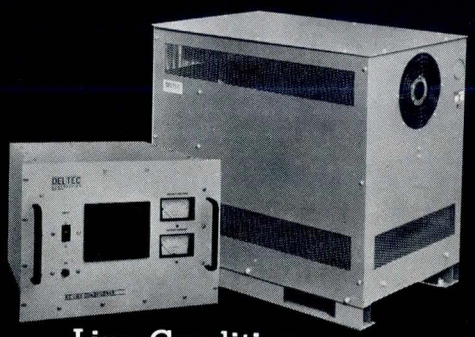
STOP TRANSIENT NOISE

Immunize Your System with Deltec.



Super Isolation Transformers Eliminate Transient Noise

The Deltec DT Series drastically reduces memory and transmission errors caused by transient noise on commercial power lines. Common Mode Rejection is 140dB and interwinding capacitance is less than 1 femtofarad (0.001 pf). Stock models are available from 250 VA to 5 KVA 1 Ø and 15 KVA 3 Ø, 50/60 Hz.



Line Conditioners for Noise & Stability Problems

Deltec's DLC Series computer power conditioners eliminate all power line noise problems which cause data and memory loss. Unique shielding provides 120 dB (1,000,000:1) reduction for: Transients - Voltage Spikes - Ground Loops - Line Noise caused by RFI or EMI (radiated noise). The DLC provides voltage regulation over 30% input voltage range with efficiencies greater than 93%. Ranges: 1200 VA - 20 KVA 1 Ø; 9 KVA - 60 KVA 3 Ø, 50 and 60 Hz.

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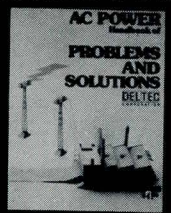
. . . gives you hard answers on how to solve AC Power problems. Now available at our cost of $4.00. Write or call for a copy.



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2727 Kurtz St., San Diego CA 92110. Telephone (714) 291-4211 TWX (910) 335-1241

CIRCLE 144 ON INQUIRY CARD

Solid State Touch Activated Keyboards Provide Full Function Capability

Model 55 Micro-Proximity keyboards are solid state, touch activated systems that combine cost advantages of simplicity with fully integrated single-chip circuitry. Built in sealed electronics of the ASCII keyboard provides full function capability in an encoded 8-bit parallel output that is completely verified, processed, and debounced, ready to connect directly to a system's data bus.

The microproximity technology, developed by TASA, Inc, 2346 Walsh Ave, Santa Clara, CA 95051, enables touching the designated sensor area to result immediately in a coded conditioned output signal. This signal and its accompanying strobe are continuous while the finger is on the key. The continuous strobe is convenient for timing (as in repeat operation on any key) and for triggering external audible or visual feedback mechanisms if desired.

When two or more keys are touched simultaneously no output code exists, a form of 2-key rollover, which minimizes error during high speed data entry. Control and shift keys, however, are valid 2-key operations.

Despite the keyboard's high speed operation, a built-in hysteresis circuit enhances the sensation of flip action and diminishes teasing of keys, even though the finger is as close as 0.001″ (0.025-mm). All other operations are similar to those on a conventional keyboard; eg, shift lock and shift functions.

Semicustom control panel designs provide flexibility in panel format, applied to an off the shelf key pattern. This includes selection of key size and number, nomenclature, product and corporate identity, and graphics. Full custom engineered control panel designs extend the options across parameters that include type, location, function, size, spacing, and number of keys; output codes; complete graphics; panel shape, size, and orientation; connector type and location; and integral mounting of displays, key locks, and other control devices. Normally designed with a smooth flat surface, the keyboards can be fabricated with formed key areas and home row locators. Gloved hand operation of a keyboard can also be accommodated.

Circle 361 on Inquiry Card

GET A CLEAR HONEST IMAGE THE HITACHI WAY!

Computer data and graphic displays never looked better, brighter, sharper.

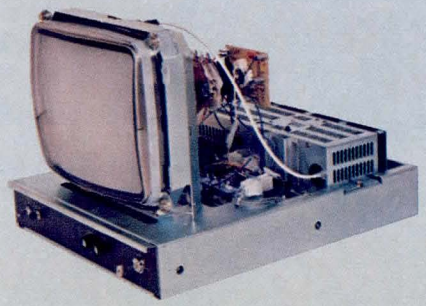
New Hitachi high resolution in-line RGB color monitors utilize wide video bandwidth and a 0.31 mm spacing between triad pairs. The result? A trio-dot density **twice that of conventional monitors!**

Look at these advanced features

Adjustment-free convergence, single PCB configuration, video amplifier bandwidth from 50 Hz to 25 MHz. Flexible frequencies range from 15 to 18 KHz horizontal and 50 to 60 Hz vertical. Monitors provide high contrast and brightness from black matrix and 85% light transmission tubes. Can any other maker match these advantages?

Variety of Screens

You can select from a wide choice of screens to meet your specific application needs: Normal phosphor; long persistence phosphor to virtually eliminate flickering, or medium resolution versions for most ambient light situations.



Unsurpassed performance

Long time convergence stability is assured due to self convergent in-line guns and **single PCB reliability.** Operator controls include power on/off, degauss, brightness, contrast.

Call or write for more information.

Hitachi America, Ltd.

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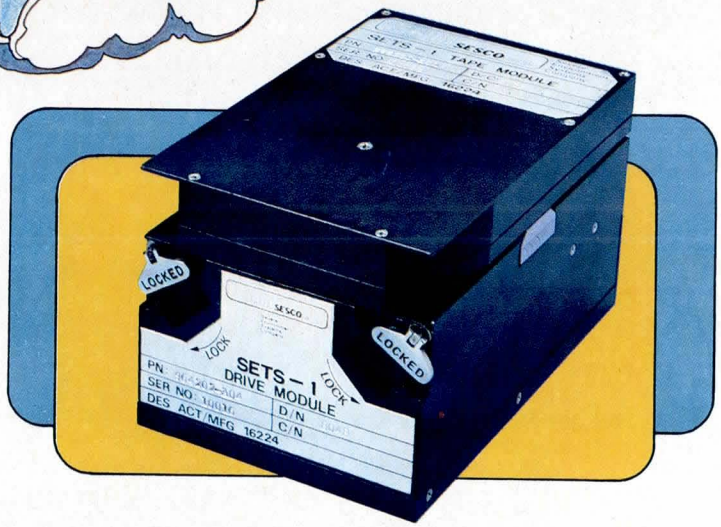
CIRCLE 158 ON INQUIRY CARD

TOUGHER!



SETS-1: A 23-megabit digital tape system for severe environments

The soaring eagle is tough. Our SETS-1 digital tape system is tougher... on the ground as well as in the air.

Built Tough for Tough Jobs

Whatever the application — industrial, military or aerospace — this rugged recorder is built to take on the most hostile environments. It meets MIL-E-5400, 4158, 16400... and more.

Right now SETS-1 is being used by the Army and Air Force for bulk storage and data gathering from tanks, aircraft and remote sites. Also for mission loaders, communications and fire control systems. Its wide operating temperature range of −55°C to +71°C makes it perfect for a growing number of industrial requirements, too.

A Top Performer

As for performance, there is none higher. A removable, hermetically sealed tape cartridge stores 23 megabits of data at 1600 bits-per-inch on 300 feet of 1/4-inch magnetic tape. Plus it offers bidirectional read/write on 4 tracks with a 192K bit-per-second transfer rate.

Small, Light, Dependable

Solid throughout, SETS-1 features an all-aluminum case that measures a compact 4" by 6" by 3.6". Quick, easy maintenance is assured by plug-in modularity. The drive module holds a reliable brushless D.C. motor and all electronics while the magnetic tape, head, sensors and capstan drive are contained in a separate tape module. All together, the entire package weighs in at under 5 pounds!

See What Tough Really Means

Phone or write for complete details today. You'll soon know why our SETS-1 tape system deserves to be called the "tough one"!

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A Subsidiary of Electronic Memories & Magnetics Corporation
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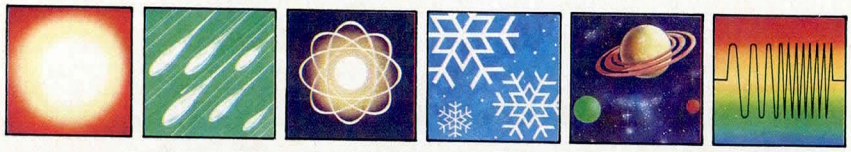

COMPUTER PRODUCTS FOR SEVERE ENVIRONMENTS

CIRCLE 155 ON INQUIRY CARD

OUR QUALITY COMES IN QUANTITY.

Many printers can give you good print quality on a first copy. The real challenge is to give you that same quality, copy after copy, on multi-part forms.

Obviously, most printers can't. The further they get from the first copy, the more their quality fades. But, as you can see here, the quality of Printronix' sixth copy continues sharp and clear.

This superior quality is achieved through a simple printing mechanism quite unlike any other. It forms characters by printing one dot row at a time, overlapping rows vertically and horizontally, while maintaining uniform hammer impact energy. The result is unequalled print quality and characters that appear solid.

This same design approach also requires fewer moving parts, eliminates most bearing surfaces, and employs simple hammer drive circuits. All of which means there's less to go wrong. And that's why Printronix can give you a full one-year warranty, not the 90-day warranty typical of most other printers.

For more information on the complete line of Printronix printers, call: (714) 549-7700. Or write:

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CIRCLE 83 ON INQUIRY CARD

32-Bit Eclipse Computer Designed to Meet Military Specs

A powerful Mil-Spec Eclipse computer, designed to meet MIL-E-5400, MIL-E-16400, and MIL-E-4158 standards, the MSE/800 incorporates an advanced 32-bit architecture with up to 2M bytes of main memory and provides over 4G bytes of virtual addressability. In the system, Rolm Corp, 4900 Old Ironsides Dr, Santa Clara, CA 95050, has incorporated an efficient demand paging technique and high speed I/O bandwidth that allow efficient use of logical space. Individual program user space can range up to 512M bytes, yielding the high capacity and performance needed for large scale computational and multiprogramming applications.

The machine uses a bit-slice architecture for high performance. A pipelined instruction processor lets the system make optimal use of its 200-ns microcycle speed. The system cache and instruction cache memory modules accelerate operations. Extensive diagnostic capabilities help ensure the availability, reliability, and easy maintenance of components.

Instruction processor operations are pipelined for optimum performance. This processor simultaneously executes one instruction while it decodes a second and fetches a third. The instruction processor is buffered by a 1k-byte instruction cache that is directly mapped to main memory. The processor transfers instructions from the instruction cache and data from the system cache to main memory simultaneously to achieve greater performance.

A 16k-byte system memory cache speeds access to main memory. The system cache is ported to both CPU and I/O system, and functions as a lookahead and lookback buffer for the system. Transfers between system cache and main memory occur at a rate of 16 bytes in 550 ns for write operations and 16 bytes in 440 ns for read operations.

A hardware accelerator for the demand paging system, the address translation unit effectively eliminates processor overhead for page translations by maintaining a table of recently referenced page addresses. The unit lets the system obtain page addresses at hardware speeds using the 36.4M-byte internal I/O bandwidth.

The system control processor is an independent diagnostic processor that provides extensive fail soft reliability. The unit consists of a console control board and a Nova architecture processor board with 4k-byte P/ROM and 32k-byte RAM. The 1.26M-byte model 8042 Mil-Spec flexible disc drive provides storage for error logs, diagnostic instruction sets, and a copy of the microcode. A terminal dedicated to this unit provides operators with soft system console facilities.

Software support is provided by the advanced operating system/virtual storage package, a multifunction, multilanguage software system that lets up to 128 users simultaneously develop and execute interactive and batch oriented operations in a secure environment. High level language support in the 512M-byte addressing range includes ANSI FORTRAN 77, ANSI general purpose subset PL/1, and ANSI BASIC. The SWAT native language debugger provides source and code level debugging facilities for AOS/VS FORTRAN 77 and PL/1 programs.

Circle 362 on Inquiry Card

Winchester/Floppy System Combines With Terminal To Form Desktop Computer

Winchester/floppy disc storage system 880 can be used with a DEC VT-103 intelligent terminal to configure a compact yet powerful desktop computer system. According to Data Systems Design, Inc, 2241 Lundy Ave, San Jose, CA 95131, the disc system is fully compatible with DEC hardware, software, and media, and can be used with any system based on the LSI-11 processor.

The half-quad LSI-11 interface board available with the disc allows users to benefit from the LSI-11 backplane in the VT-103. It occupies only one half-quad slot in the 4 x 4 backplane, leaving seven half-quad slots for the processor, memory, and other options. Bootstrap P/ROMs in the interface eliminate the need for a bootstrap card, further reducing the cost and freeing two slots.

The disc unit conserves tabletop space by combining 8″ (20-cm) Winchester and 8″ floppy in a 5.25″ (13.34-cm) high package. The unit can be placed directly on the tabletop or mounted in a lowboy rack.

Formatted capacity of the Winchester disc is 7.8M bytes. The floppy provides an additional 1M byte and accepts all combinations of single/double-sided and DEC single/double-density diskettes. In most applications, the Winchester serves as primary online storage because of its higher capacity and performance.

Compatibility with the DEC operating system is maintained by emulating the RL01 with the Winchester and the RX02 with the floppy. Users may switch from DEC systems with little or no change to their software. They can move from one operating system to another and can expect to remain compatible with future software releases.

Circle 363 on Inquiry Card

Dual-Floppy Disc in Computer System Offers 1.2M-Byte Storage

A small business computer system combining high capacity, high reliability floppy disc storage with a sophisticated error correction scheme and Z80 based processor, the 2600, introduced by Vector Graphic, Inc, 31364 Via Colinas, Westlake Village, CA 91362, uses dual double-sided quad-density 5.25″ (13.34-cm) floppy discs to store a total of 1.2M bytes. Central unit is a Vector 3 console with 12″ (30-cm) video display terminal and keyboard, a Z80 based single-board computer, and 64k memory. The unit uses the proprietary dual-mode controller board to interface drives to the central processor.

Based on IBM type technology, the controller automatically corrects up to five erroneous bits in every 256 bytes transferred from disc to CPU, eliminating errors due to disc contamination and other problems. Another controller feature is 256-byte sector buffering, enabling the computer to simultaneously handle interrupts and data transfers in and out of memory for communications tasks and other realtime functions.

In addition to high capacity and automatic error correction, the discs provide high speed—3-ms track to track, and 75-ms average access time. A rigid design adds to system reliability.

Software support system, includes the CP/M2 operating system, SCOPE screen oriented program editor, RAID debugger, ZSM assembler, and Microsoft Basic 80 Release 5. Optional are business accounting, word processing, and financial planning and modeling packages.

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Whatever your business or application, there's a TermiNet® 200 printer to fit it perfectly.

From mini/micro computer output to transaction processing, General Electric TermiNet 200 printers deliver the high performance you want. Like outstanding throughput, excellent print quality for up to nine-part forms, reliable operation, minimum downtime, and low operating costs. Choose the one to match your exact needs. A basic line printer with serial or parallel interfacing. A forms access printer with precise alignment and no paper waste. A split platen printer that does two different jobs at the same time. Plus a highly versatile KSR.

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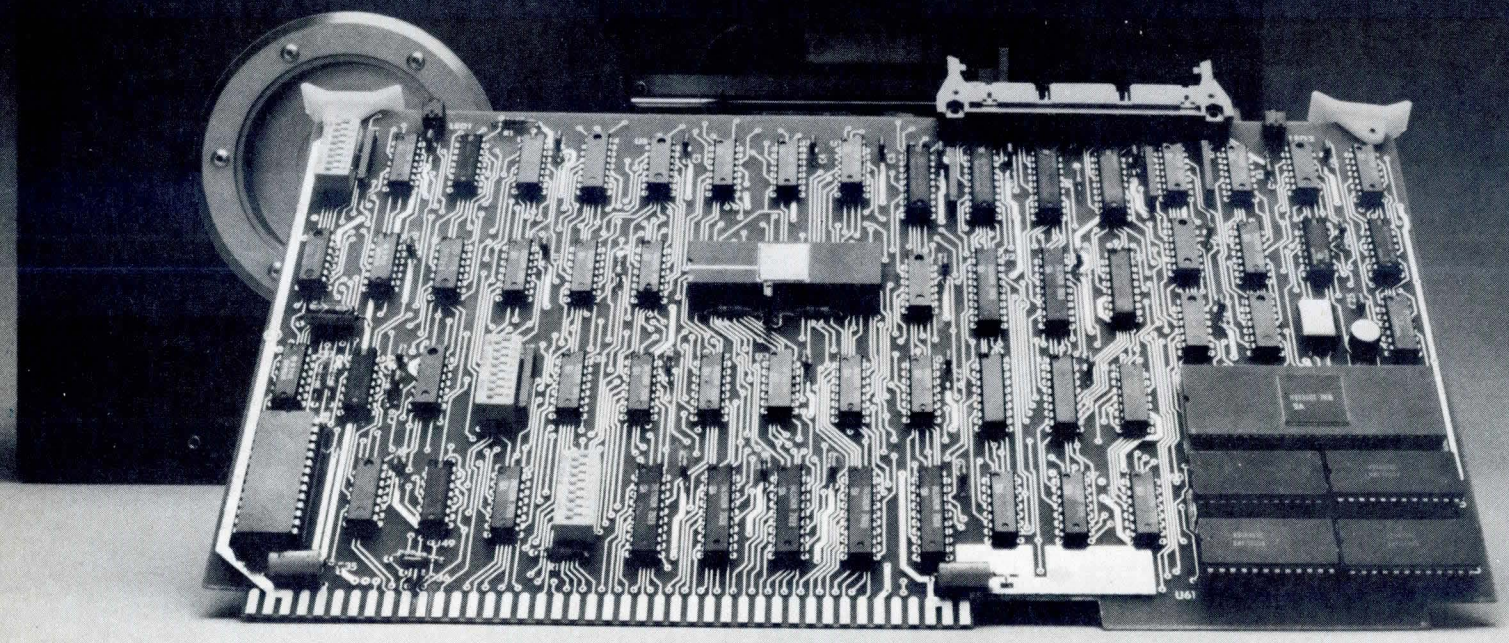

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CIRCLE 135 ON INQUIRY CARD

If You Use Back Planes...

You need the Innovation and Imagination of TRW Cinch Connectors' "Creative Technology"

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If your telecommunications, computer or military packaging applications require the following types of back planes, consider TRW Cinch Connectors as your primary source:

Printed Circuit Back Panels — new facilities, new equipment, mean even higher quality panels from double-sided to multi-layered and ten ounce copper laminated boards for your press fit requirements.

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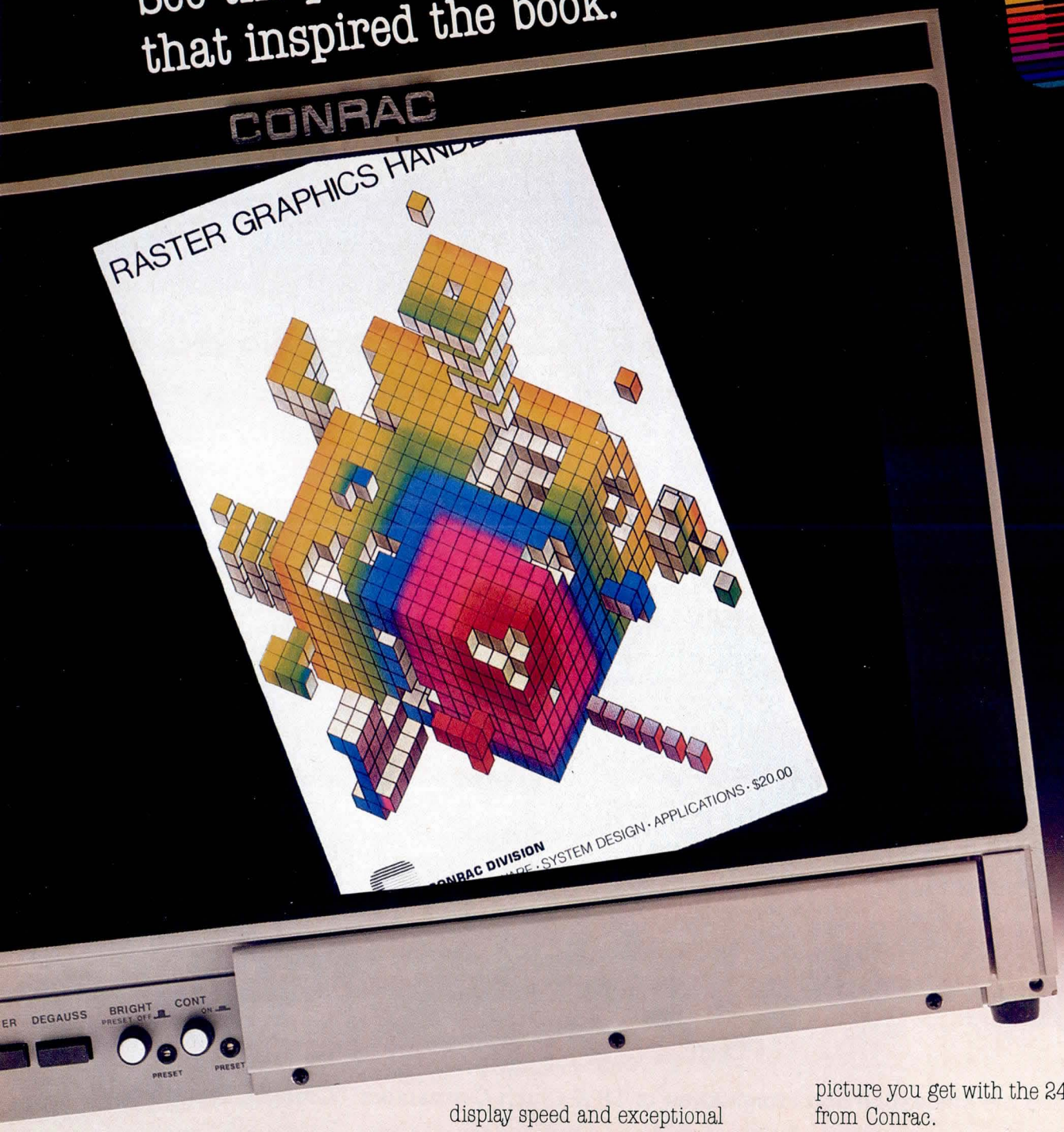
CIRCLE 122 ON INQUIRY CARD

TRW CINCH CONNECTORS

See the picture that inspired the book.



There are three must-see pictures this year. All from Conrac.

They are everything you would expect from the authors of the informative text on raster graphics. And then some.

See the 7100 series for high performance color, accelerated display speed and exceptional contrast that come with Conrac's precision in-line gun CRT, wide-band video amplifier and selectable horizontal scan frequencies.

See the 7200 series for all that—plus the extra resolution and sharpness that comes with the 7200's high density shadow-mask CRT.

And for the ultimate in high-resolution black and white, see the picture you get with the 2400 series from Conrac.

You may love the book—but wait till you see the picture.

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600 North Rimsdale Avenue
Covina, California 91722
Telephone (213) 966-3511 Telex: 67-0437

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CIRCLE 148 ON INQUIRY CARD

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CIRCLE 45 ON INQUIRY CARD

Direct Access Storage Units And Controller Are Compatible With IBM 3380 and 3880

Compatible with the IBM 3380 storage unit, direct access storage devices can store up to 2.52G chars of information, which is double the capacity of the company's current units. Also announced by Control Data Corp, Box O, Minneapolis, MN, 55440, was the 38800 storage controller, which directs storage and transfer of information between processors and storage devices. The disc storage units are designed for users of large IBM and compatible computer processors.

The units can read and write information at a rate of 3M chars/s, more than twice the speed of the 33502, through use of thin film head data recording technology. The units are designed with read/write heads, magnetic recording discs, and actuators contained in fixed sealed head/disc assemblies. Each storage control unit contains two independent control paths, or storage directors, that connect to data channels of a computer processor. One or two strings of up to four direct access storage devices can be attached to each storage director, thus providing users with a maximum of more than 20G chars of data/storage director.

Model A devices include four actuators and control logic to allow attachment to one storage director of a storage control unit. Model B units contain four actuators, and up to three units can be connected in a string to the A and AA models. The model AA also contains four actuators, but expands control logic to permit attachment to two storage directors located in the same or different controllers. A standard feature of these devices is dynamic path select.

An optional dual-access feature allows any of 16 actuators in a string to be addressed through two internal data paths. Thus, two concurrent data transfers can occur through the use of any two actuators in a string, and may be overlapped with seeking and rotational position sensing of all other actuators. Dual-access provides concurrent data transfers via each storage director, and continued data availability in the event of a malfunction in any channel, controller, or storage director.

The storage control unit provides program control of file organization and format to allow random or sequential processing of files. The two storage directors in a control unit can be connected to the same or different channels of a single processor. Each storage director can also connect to up to eight channels of the same or different processors, which allows greater subsystem throughput and availability of data.

Circle 365 on Inquiry Card

Laser Printing System Offers High Quality Output Direct From Computer

A computer controlled laser printing system that humanizes hardcopy computer output in terms of convenience and readability has been introduced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304. The HP 2680 prints 45 letter size pages/min, providing an added performance category for hardcopy output devices. It brings together in one system features and benefits of distributed database applications, word processing, offset printing, message distribution, and high speed reduction copying.

The system delivers reports directly from the computer in one pass. Printed on letter size paper and looking almost typeset, reports can be illustrated with symbols, logos, and special characters. Standard business forms can be stored electronically in the system.

The laser system is designed for use with HP 3000 Business Computer Systems—Series 30, 33, or Series 44. Because of its built-in intelligence and memory, it places little burden on the controlling computer; even the smallest HP 3000 can handle it using less than 20% of its resources.

Multiple printers at separate locations can produce localized or combined reports. Each system can incorporate online data from each computer in the network and produce tailored reports locally, avoiding cost and time for mailing or express delivery between locations.

Combining the HP 2680A intelligent page printer and interactive software, the system allows users to produce complex page layouts and forms, previously available only from offset printing processes. Up to eight separate information blocks can be designated on a single page of output. Character sizes range from 22/in (8/cm) to 1.38″ (3.51 cm) wide. With the system, forms can be created, stored in memory, and updated easily and conveniently. The blank form and fill-in data are produced simultaneously by the system, eliminating the need for stocking blanks.

Circle 366 on Inquiry Card

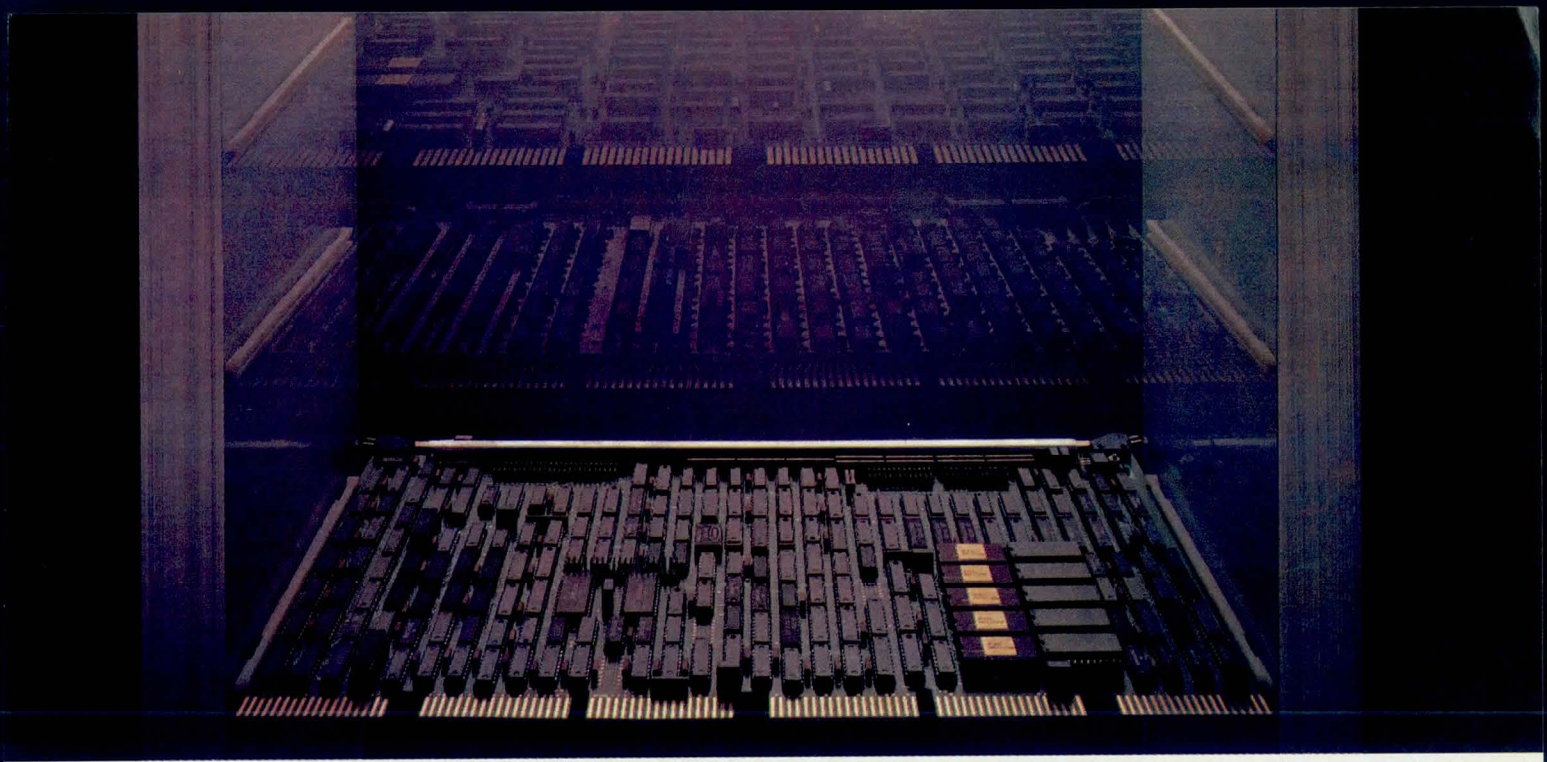
In-Circuit Test Systems Increase Memory Capacity To Double Data Storage

In-circuit test systems for prescreening PC boards before functional or performance testing, L529A and L527A assembly inspection systems include 96k of memory, and provide twice as much data storage capacity as the L529 and L527 systems. In addition to expanded memory, Teradyne Inc, 183 Essex St, Boston, MA 02111, provides the system with software features designed to increase throughput and fixturing efficiency. The added capabilities include testing of multiple boards of the same type, fixtured on the same test plate, in one contacting cycle; and testing boards of different types fixtured on the same test plate in separate test cycles.

L529A also offers a version of the company's board handler/fixturing system that operates without vacuums or air. A pressure rod matrix provides 60% more weight above the board under test for better probe compression on dense probe beds. The pressure rods themselves weigh 6.25 oz (175 g) each, compared with 5 oz (140 g) previously, and the number of rods has been increased by over 100. To accommodate the heavier weight, a 2-speed index lift action has been introduced in the board handler to enable the system to provide positive probe contact without an increase in access time.

Along with the board handler, the company is supplying socketed probes for use in building test fixtures, replacing the 1-piece probes previously supplied. The 2-piece probes are available with an assortment of probe contacts which plug into a universal probe receptacle. Probe contact styles include tulip head, spear point, and chisel head. All are offered in two contact forces, allowing selection of the contacts that will probe the best results for testing different boards.

Circle 367 on Inquiry Card



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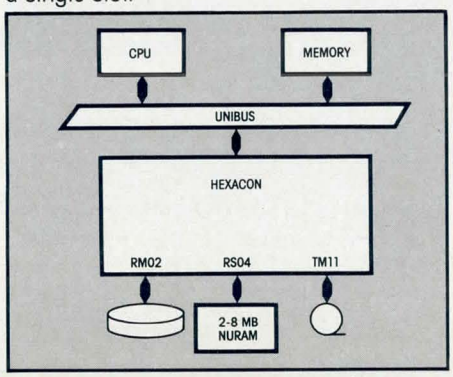

Cut costs in the factory and in the field. By using one board to do the work of three or more—with no degradation—you save a bundle in a number of ways.

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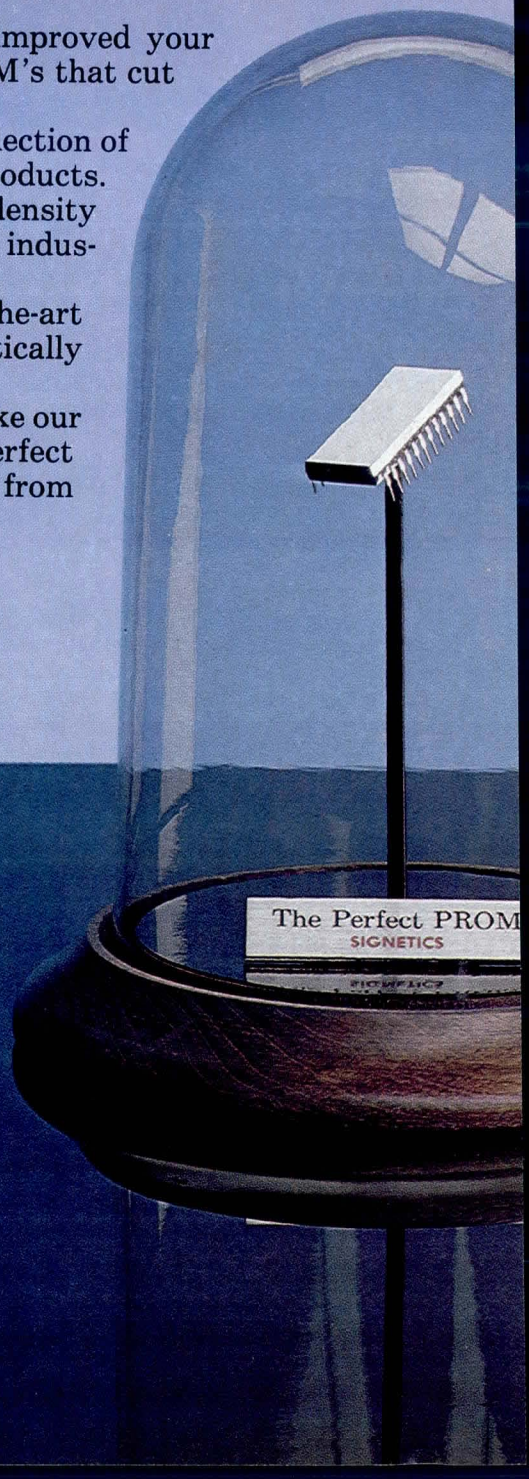

ct PROM.

BIPOLAR MEMORY SELECTION GUIDE

DENSITY	DEVICE TYPE	ORGANIZATION	OUTPUT CIRCUIT	ACCESS TIME (ns)	I_{CC}MAX. (mA)
256-Bit	82S23	32X8	OC	50	77
256-Bit	82S123	32X8	TS	50	77
256-Bit	10139	32X8	OC	20	145
1K	82S126	256X4	OC	50	120
1K	82S129	256X4	TS	50	120
1K	10149	256X4	OC	20	150
2K	82S130	512X4	OC	50	140
2K	82S131	512X4	TS	50	140
4K	82S115	512X8	TS	60	175
4K	82S141	512X8	TS	60	175
4K	82HS147	512X8	TS	45	155
4K	82S137	1024X4	TS	60	140
4K	82HS137	1024X4	TS	45	140
8K	82S180	1024X8	OC	70	175
8K	82S181	1024X8	TS	70	175
8K	82LS181	1024X8	TS	150	80
8K	82PS181	1024X8	TS	70	185
8K	82HS181	1024X8	TS	55	175
8K	82S2708	1024X8	TS	70	175
8K	82S183	1024X8	TS	60	175
8K	82S185	2048X4	TS	100	120
8K	82HS185	2048X4	TS	60	155
16K	82S191	2048X8	TS	80	175
16K	82HS191	2048X8	TS	60	175
16K	82S195	4096X4	TS	70	155
32K	82S321	4096X8	TS	90	175

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CD5/81

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SOFTWARE

Disc Optimization Utility Improves Performance for RSTS/E Users

Diskit, a utility for users of DEC's RSTS/E operating system, consists of four system management and disc optimization tools. A major component of the package provided by Software Techniques, Inc, 5242 Katella Ave, Suite 101, Los Alamitos, CA 90720, is DSU (disc structuring utility), an automatic disc optimization utility that rebuilds RSTS discs to improve system performance during directory and file operations. Requiring under 1 h to run, DSU improves overall system performance by as much as 35% by eliminating excessive accesses and reducing seek time.

DIR, a Macro-11 fast directory program, allows users to look up files by name, extension, and date (with wildcards) at the rate of 250 files/s. It supports all standard direct switches along with features such as password lookup, UFD placement, and UFD size.

The Macro-11 disc utility subroutine package, DUS, provides routine documentation for these management tools so that users can write their own disc handling programs. Included are routines (callable from Basic-Plus-2 or CSPCOM) that allow creation, placement, and full extension of UFDs under normal timesharing.

OPEN, a Macro-11 open files display program, displays open files by job, with complete job and file statistics. It has a sleep switch that allows information to be dynamically updated at any interval.

Circle 368 on Inquiry Card

Program Generator Cuts Screen Format Development Time

Version 3.0 enhancements of RIMS/MPG (requester oriented information management systems/mechanized program generator) source code program generator for DEC systems have been made available by Information and Systems Research, Inc, Bldg 1, 410 Rouser Rd, Coraopolis, PA 15108. Among the additions are capability to design reports and data entry screens online, create business graphics, and perform advanced technical functions.

Online screen design stems from a built-in onscreen data element move capability. By using cursor control keys, data elements can be arranged as desired on the CRT. In tests, development times for production of custom reports have shown reductions of approximately 95%.

Bar graphs, bar comparison graphs, deviation bar graphs, point graphs, and U.S. maps can be produced on a variety of output devices. This package also provides capability to custom write and install state maps, allowing users to produce sales graphs on a county or city basis.

Technical user features included in the package enable users to customize the system for a specific production environment. Some of these functions are white/black screen selection, variable compilation procedures, variable linkage procedures, user selectable program chaining sequence, and ability to preserve or delete program generation work files.

Another utility provides ability for a nonprogrammer, with no prior knowledge of system level commands, to delete dictionaries, work files, or other data and program files. In addition, basic packaging and ease of use have been improved.

RIMS/MPG is available for operating system/language versions that include RT-11, (CTS-300) DIBOL, DBL, and COBOL; and RSTS/E (CTS-500) DIBOL, CBL, COBOL, BASIC-PLUS, and BASIC-PLUS-2. Each version produces documented and consistent source level code for the programs it creates.

Circle 369 on Inquiry Card

Commercial Software Combines COBOL and DIBOL Languages With Timesharing Capability

PCS-200 and -100 commercial software packages accommodate the use of COBOL and DIBOL on the SYST-13V and DEC LSI-11/23 systems. The commercial software from Plessey Peripheral Systems, 17466 Daimler, Irvine, CA 92714, also features TSX-Plus, a multiterminal operating system suited for business data processing, that provides timesharing capabilities while maintaining the simplicity and easy use of the DEC RT-11 operating system.

In PCS-100, a DIBOL-11 compatible language processor (DBL) is combined with TSX-Plus and RTSORT capabilities. PCS-200 combines a COBOL language processor with TSX-Plus and RTSORT capabilities.

TSX-Plus allows user programs to be loaded into separate memory partitions so that they do not occupy the same virtual address space as the operating system. Each job can address up to 56k bytes of memory; if more jobs are running than will fit into memory, a priority and time-slice system controls which jobs remain in memory and which jobs are swapped to disc files. The packages do not use the RT-11 monitor but do require RT-11 device handlers and utility programs.

In addition to allowing RT-11 to be a timeshared operating system, the TSX-Plus feature provides automatic device spooling, log-on facility and usage accounting, program to program message communication, virtual lines, and detached jobs.

Circle 370 on Inquiry Card

Translator Converts System/3 RPG to COBOL Automatically

Interactive System/3 RPG CCP programs are automatically converted to corresponding CICS/VS Command Level COBOL programs by the IBM System/3 CCP to IBM CICS/VS COBOL translator package. The package, from DASD Corp, 9045 N Deerwood Dr, Milwaukee, WI 53223, also converts the System/3 display format facility (DFF) screen definitions to CICS/VS basic mapping support (BMS) screen definitions.

With automatic conversion of CCP to CICS as well as batch RPG programs to COBOL, System/3 users can migrate to different or larger equipment configurations with a minimum of effort. Using the output from the RPG/RPGII to COBOL translator, the CCP to CICS translator converts all screen and file references to CICS/VS command level COBOL techniques and performs realignment of all input and output screens used by the programs. The programs generate complete error handling and MAPFAIL routines.

A conversion listing that shows all changes and highlights several key areas is also produced by the translator. The DFF to BMS portion of the translator handles screen realignments of the COBOL field positions in the map, a picture of the screen, and the generated BMS code. □

Circle 371 on Inquiry Card

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CIRCLE 130 ON INQUIRY CARD

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Together, these products represent a continuum of capacity and compatibility matched only by the continuum of quality that has always distinguished Memorex offerings. A continuum that reaches back through six generations of disc drive manufacturing experience and seven in disc packs and cartridges. And a continuum secured by Memorex's edge in technology, the investment in research and development and the fact that we create and control the key elements of our drives—the media, heads, PCBs.

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CIRCLE 50 ON INQUIRY CARD

Production Control System Tracks Parts in Real Time

With advances in component performance and in system design concepts, older technologies—sometimes thought to be obsolescent—often resurface to be used effectively in new contexts. An example of this is the use of mark sense tab cards in a realtime production control system. This system, designated as FAMIS (Factory Management Information System), is being employed in the production of hybrid assemblies by Hughes Aircraft Co, Ground Systems Group, PO Box 3310, Fullerton, CA 92634.

Designed and installed by Digital Datacom Inc, 27721 La Paz Rd, Laguna Niguel, CA 92677, the system processes a single tab card as job traveler, to accompany a specific assembly through a series of workstations. Replacing all paperwork associated with the assembly, this card alone contains complete documentation of the operations and inspections performed on that assembly. Hand-fed optical readers scan the card to update the system's data files following each production event.

Use of a single tab card for a complete job history departs from the alphanumeric Hollerith code that is traditionally associated with this medium. Instead, the field elements of the card (printed by Moore Business Forms Inc, 1045 W Katella Ave, Orange, CA 92667) are configured as a 2-dimensional data matrix. (See Fig 1.) Each entry is made as a single pencil mark within a designated box. Advanced optical readers that can correctly distinguish marked from unmarked boxes under relatively noisy conditions make this system practical. Creased or smudged cards on which data are entered in correct locations, but without precision in the intensity or shape of the pencil mark, can be processed normally. During the 6-month interval of system operation from start-up in September 1980 through March 1981, with an average of 3000 cards in the system at any time, no error has occurred in the reading of any card bearing a correct entry.

The system that utilizes these cards is designed to provide a means of monitoring the complete realtime status of the entire production flow and quality test defects. Emphasis in the design has been on providing the capability for a simple, flexible human interface to the system.

System Configuration

A Data General MP-100 microNOVA computer with a 64k-byte memory and an 840-ns instruction execution time is the central processor for the system. Also from Data General is the 6095 disc drive that provides 5M bytes of fixed and 5M bytes of removable storage.

A display terminal, the 80-column x 24-line ADM-3A from Lear Siegler Inc, Data Products Div,

(continued on page 76)

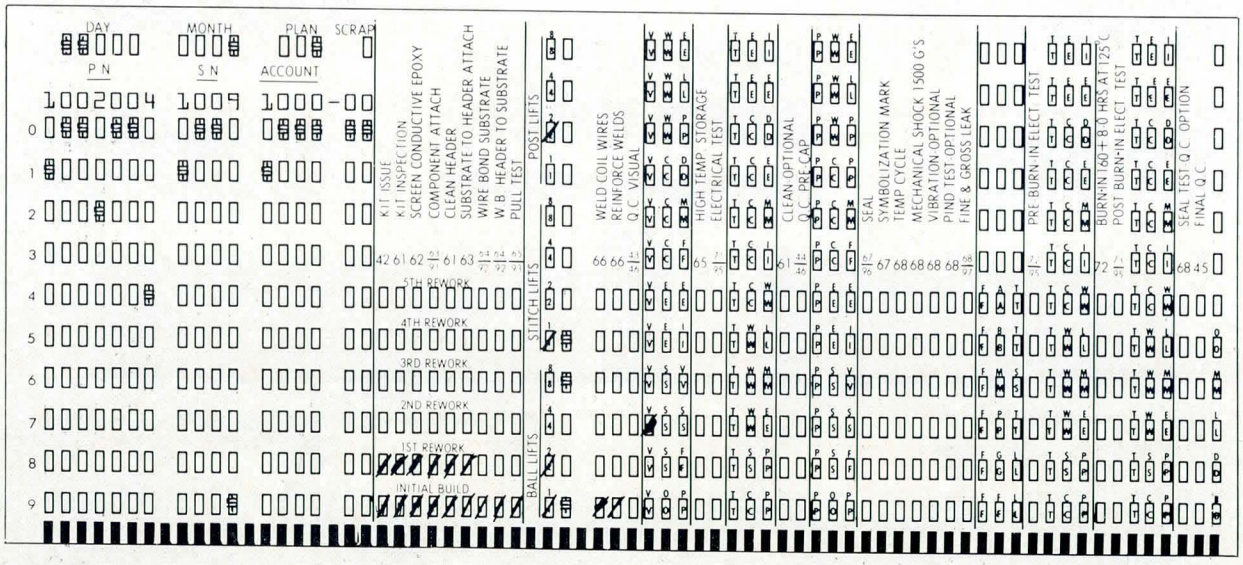

Fig 1 Mark sense tab card used in FAMIS system. Cards are initialized with generalized information relating to date, coding plan, account, and part and serial numbers. Subsequently, personnel mark squares to indicate completion of operations at workstations. Data fields following inspection steps [pull test, quality control (qc), visual, electrical test, etc] allow for entry of failure types

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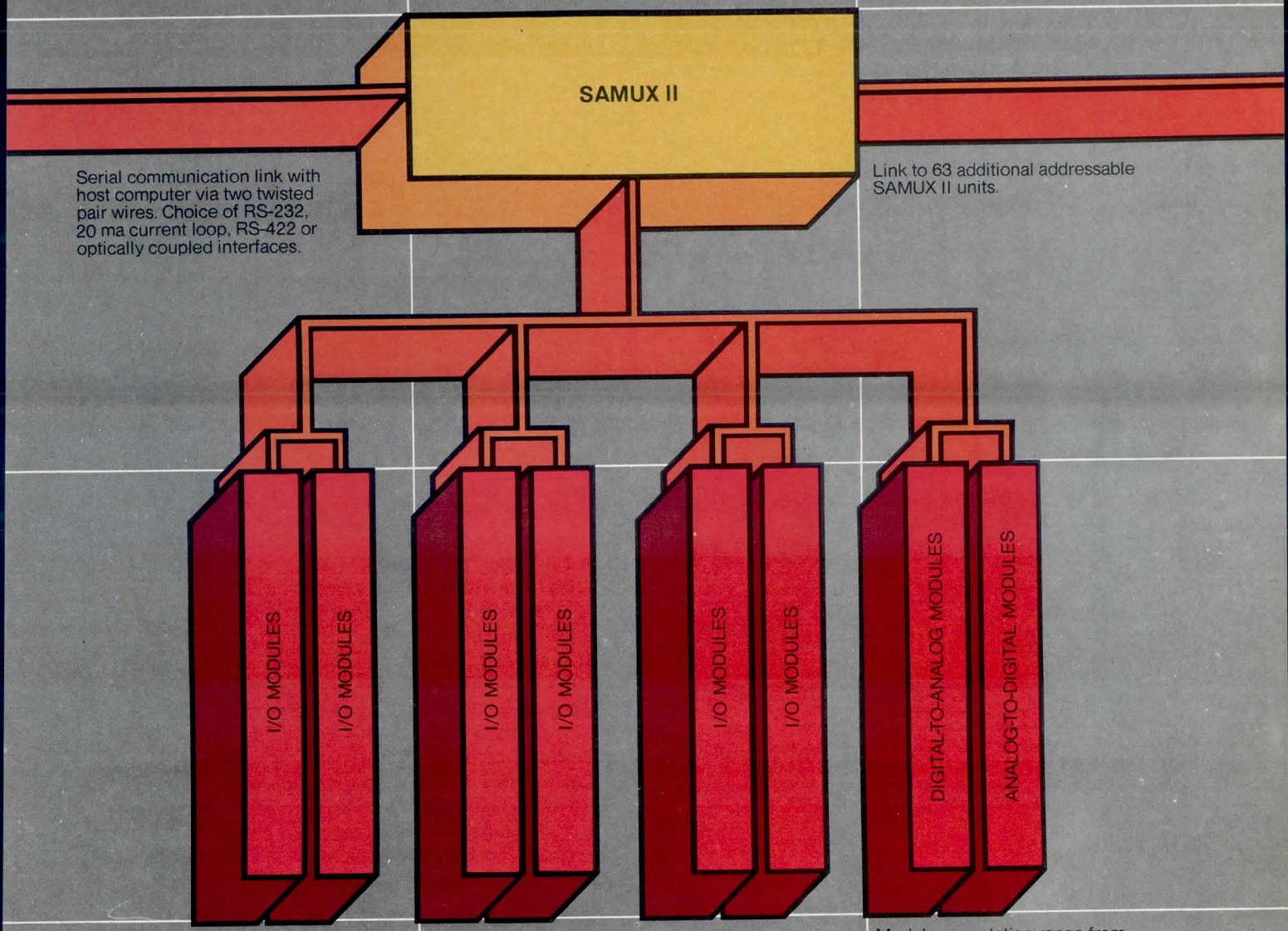

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CIRCLE 51 ON INQUIRY CARD

714 N Brookhurst St, Anaheim, CA 92803, provides a sequence of menus that allows a production control clerk to enter the configuration for a card series. This configuration includes printed fields for account number, generic part number, serial part number, date, and build plan number, as well as fields for subsequent data entry. Once the card series has been configured, the printed fields are produced by an 810 line printer from Texas Instruments, PO Box 1444, Houston, TX 77001.

Three card readers (soon to be increased to a total of five) are used in the facility. These readers include models 100 and 020 from True Data Corp, 17092 Pullman St, Irvine, CA 92714. Electronic modification of these readers, which is performed inhouse by the system manufacturer, includes the use of an 8-bit SCAMP microprocessor from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051. The microprocessor converts input data to serial format, and provides them to the CPU upon polling via an RS-232 interface.

One card reader, stationed near the display terminal and printer, acts as a verifier (Fig 2). A clerk can verify newly generated cards via this reader; an error light on the reader indicates a card entry that does not correspond to data in the disc file. This and

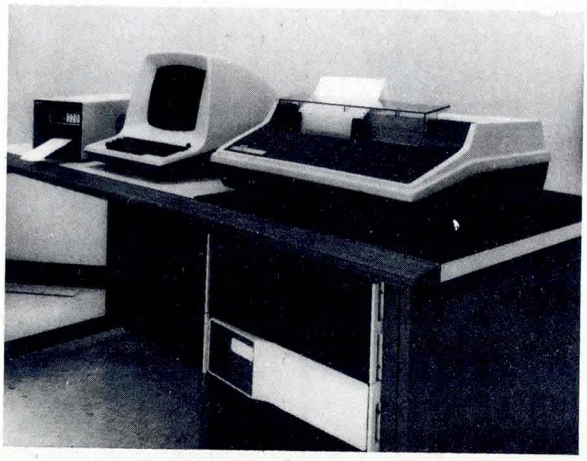

Fig 2 Card reader, display terminal, printer, central processor, and disc drive in hybrid assembly facility. Central processor in Hughes installation is Data General MP-100 microNOVA, but options ranging upward through NOVA and Eclipse lines allow for upgradability

other readers are located at various points in the production test facility to serve as input terminals for the system (Fig 3). As an employee completes an operation, he marks the appropriate box on his card. A defect may also be entered by checking an identifying box. The employee then inserts the card into any one of the readers in the facility, thereby entering the

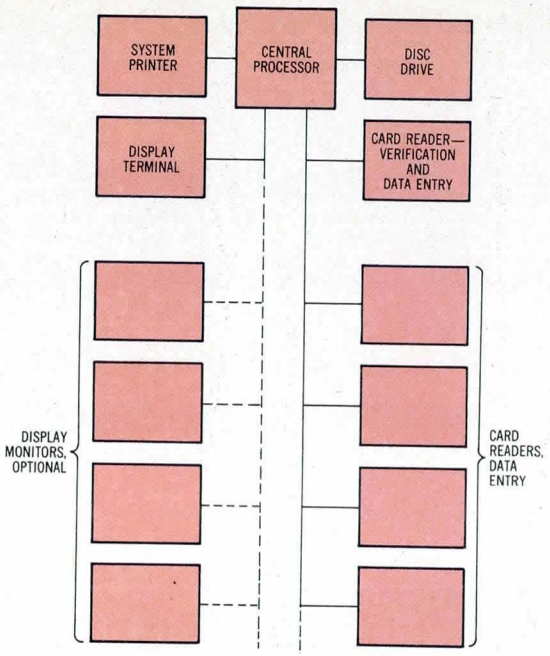

Fig 3 Configuration of production control system. Expandability allows optional display monitors and increases in number of card readers

data on disc. Then the card is returned to the hybrid assembly that it will accompany to the next workstation.

The employee enters pencil notations of faults on the back of the card, utilizing defect codes; subsequent to repair and inspection, a quality control stamp is added to the entry. Thus, between the data entries on the front of the card and the notations on the back, the full record of each specific assembly is maintained without additional documentation.

The system can be operated as a standalone production tool, or can be used as an extension of a central computer. Under consideration at the Hughes facility is linkage to an already installed central computer, the HP-3000 from Hewlett-Packard, 1501 Page Mill Rd, Palo Alto, CA 94304. Communication to the central computer, via either a synchronous or an asynchronous port, would provide such information as inventory and labor hours. Through PCB and software additions and use of an RJE-80 communication protocol, the production control system would, in this proposed plan, emulate an IBM 2780 remote batch terminal.

Software Modules

Application software for the system consists of five modules, totaling approximately 350k bytes. Coded in FORTRAN 4, the software is stored on disc. These

(continued on page 80)

INDUSTRIAL SOFTWARE

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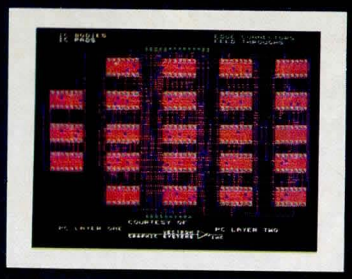

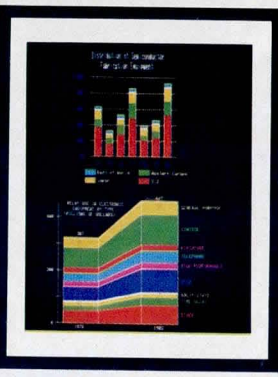

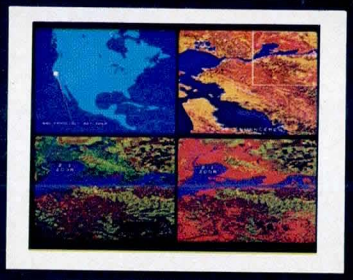

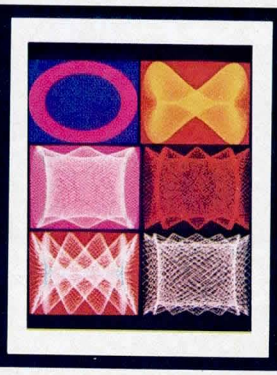

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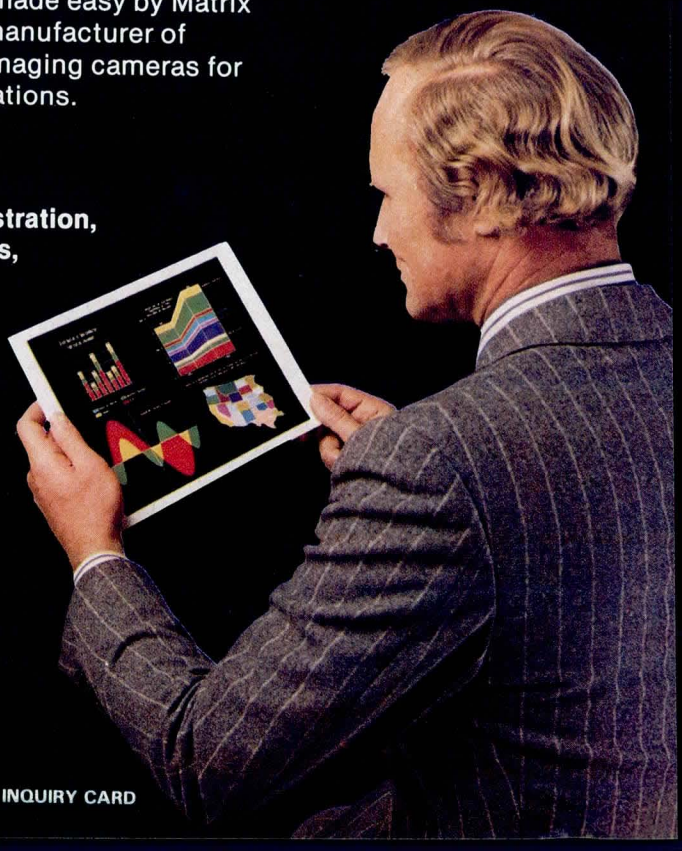

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CIRCLE 126 ON INQUIRY CARD

modules, called on a terminal from a master menu, provide the successive stages of system generation and operation.

The first module is the "build plan manager." Typically, a production engineer initiates the plan on a worksheet and passes this information to a production control clerk. Following a CRT-displayed menu, the clerk keys parameters into the system, defines the fields of the tab card, identifies those fields with production and inspection steps, and establishes the time duration for each step in order to maintain the production schedule. The control clerk then calls up the next module, "part build initiation," and responds to the next set of menu prompts to establish the hierarchy of account numbers, part numbers, and serial numbers. In addition to entering these parameters into the system, the part build initiation module provides a cumulative directory of all active numbers, reviews account data, builds disc data files, and prints the required job cards. Job cards are then issued to the floor, each accompanying the corresponding hybrid assembly.

Shop personnel monitor the status of parts with a third module, "work in progress." This module provides access to three directories (account numbers, part numbers, and build plans), a part status listing, and a database maintenance module. Part status listing allows personnel to ascertain part populations and subpopulations at various workstations in addition to the location of any specified part. The maintenance module provides a total work in progress listing and also allows selected personnel to enter the system via passwords so that various parts of the data base can be deleted or updated.

The fourth module, "hardcopy report," provides a printout of exception reports, parts status, and quality control reports, in each case including listings according to account and part numbers. (Utilization of this module requires the substitution of paper for tab cards in the system printer.) Finally, selection of the master menu's fifth module, "turn system off," performs disc housekeeping, closing all directories before shutting down the system.

A sixth module may be required if the production system is interfaced with the HP-3000 central computer. Three modes by which the system would report to the central computer are under consideration. The first of these, which would require an addition to the master menu, would allow the operator of the production system to select a callup request to initiate the data transfer. No menu addition would be needed for either of the other two modes, one of which would make use of a data request issued by the central computer, while the other would be an automatic file dump, initiated by the FAMIS system clock at programmed intervals.

Summary

In contrast to the traditional production control system in which data availability typically lags several days behind production, this system provides current realtime files that reflect the immediate status of all assemblies in production. Statistical reports of detected faults, sortable by account and/or part number, are furnished. Furthermore, the data entry method is designed for flexibility and ease of use by production personnel. The system also offers compactness and completeness in the maintenance of archival records. Finally, the manual mode of data entry allows data collection to continue even during computer system outage.

The expandability of the FAMIS system is demonstrated by the system manufacturer's plans for a customer in Los Angeles. In that version, 30 card readers will handle an average card population of 50,000, performing multiple concurrent programs. Required multitasking capability will involve a central processor with 256k bytes of memory that utilizes a current loop interface. Among the peripherals will be a 200 line/min printer, a 25M-byte Winchester disc drive with a 1.26M-byte floppy, and seven interactive CRT terminals, including the main station and six remote monitors. □

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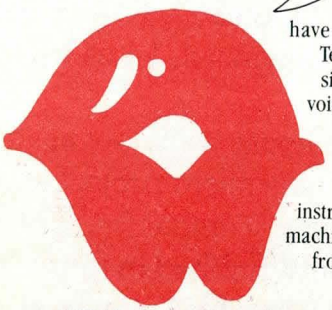

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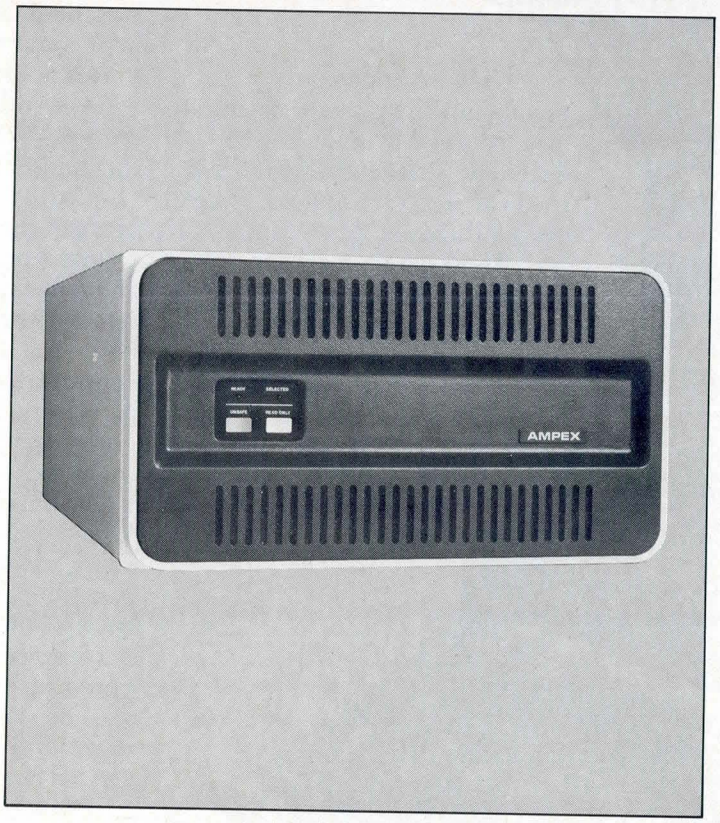

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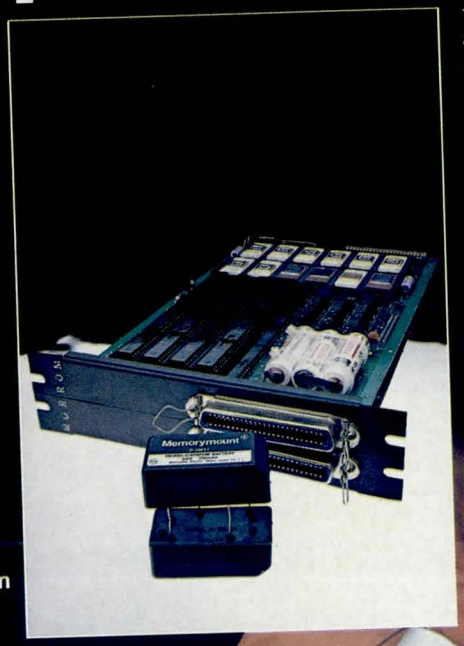

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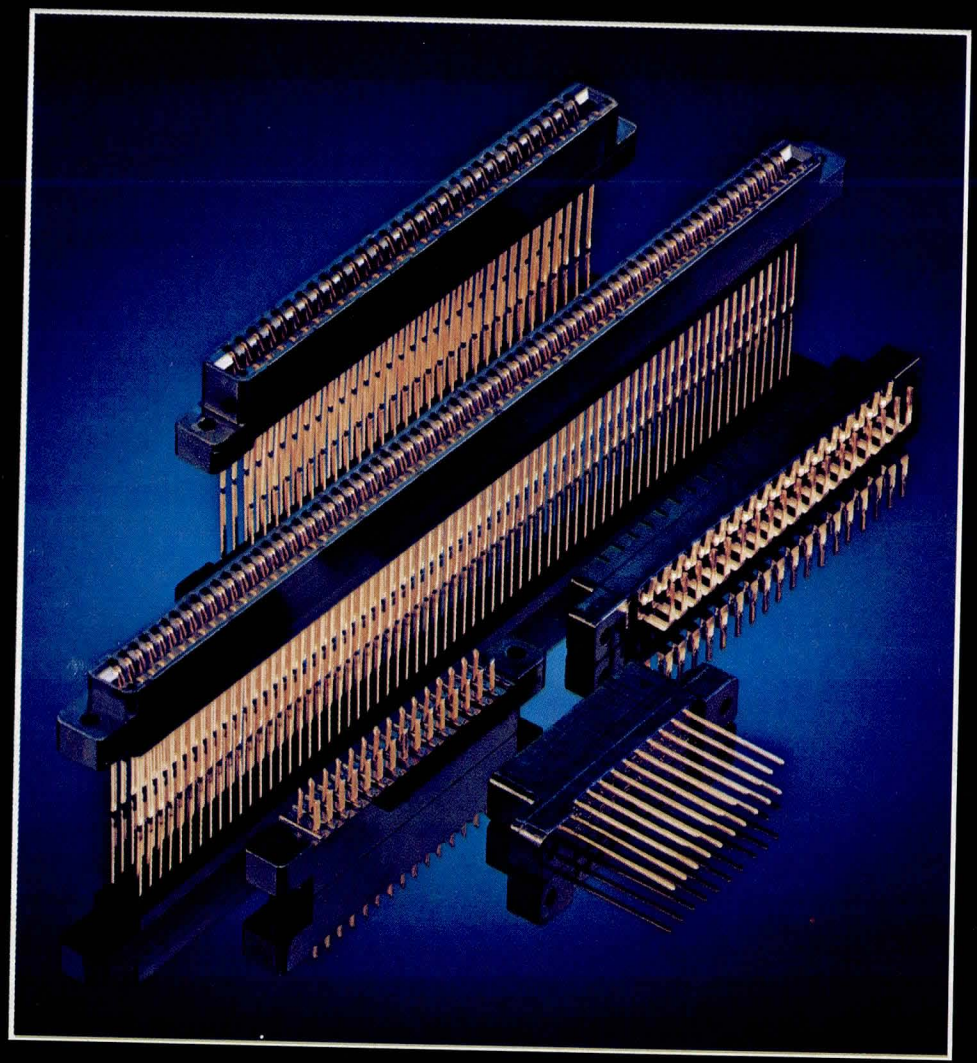

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LOW COST POWER TRANSIENT PROTECTION

Three line conditioning alternatives improve power quality where UPS blackout protection is not required

Frank Cathell

Deltec Operation, Gould, Incorporated
2727 Kurtz St, San Diego, CA 92110

With increasingly smaller and more powerful computers appearing on the scene, it would seem that ac power requirements might decrease. However, computer usage has increased as well, and developments in other electronic product areas have raised the demand for more and higher quality ac power. Simultaneously, the energy crisis has drastically limited construction of new power plants, placing a greater strain on existing plants. These factors combine to motivate a proliferation of uninterruptible power systems—auxiliary power sources that keep computers operating during blackouts or brownouts—and alternative devices that offer slightly more limited protection at significantly lower cost.

An uninterruptible power system (UPS) can offset many power problems such as marginal voltage level during unanticipated peaks in demand, fast fluctuations and sudden spikes or dips, and even high frequency transients. However, a UPS is overkill where blackouts are not a serious problem. Because it trades quantity for quality, a UPS actually increases power requirements. In addition, it is a relatively expensive solution in terms of initial investment, installation cost, nonproductive use of floor space, periodic battery maintenance, and inevitable battery replacement. Available at a fraction of the cost of a UPS, alternative solutions to power line problems require less floor space and far less maintenance.

Recognizing Power Line Problems

Computer power requirements fall well within commercial utility specifications that define limits for amplitude distortion, frequency variation, and harmonic distortion. However, utility specifications do not mention the fluctuations lasting from 3 to 30 ms that often occur during load switching or phase compensation. For example, a recorder installed at a residential site detected 2500-V transients generated by an oil burner. Surges exceeding 2500 V have been detected at hospital and department store sites. Industrial and manufacturing facilities have potentially greater problems created by

the presence of elevators, cranes, welding equipment, mercury arc lighting, and high voltage ignition systems. The typewriters, calculators, telephone switching stations, vending machines, and copiers that abound in every office contribute to the problem of power fluctuations and transients. Although these disturbances are obviously beyond power company control, they can cause utility load switching that aggravates the problem.

There are four basic categories of power line disturbance: total loss of power for extended periods, insufficient (or excessive) voltage for extended periods, short term voltage fluctuations at slow rates, and short term voltage fluctuations at fast rates. Any category of power line disturbance can be superimposed on the ac power and on any other category of disturbance. The first two categories can be detected by monitoring line voltage with a voltmeter and noting whether computer malfunctions coincide with periods of low (or high) voltage. The last two—short term variations and extremely fast fluctuations—can be detected only by particularly responsive power line monitoring equipment.

Detection and correlation of fast ac power fluctuations and transients is further complicated because these disturbances can enter a circuit as either common-mode noise or normal-mode noise. Since each enters by a different route, detection devices must be connected at different points in the circuit. A high performance power line monitor correctly coupled to a circuit can record transients with amplitudes varying from a fraction of a volt to several hundred volts, with durations as low as 50 ns. These sophisticated monitors can be leased for short periods at reasonable rates.

A Range of Solutions

Solutions to ac power problems run the gamut from basic power line filters installed just ahead of the critical load to a full UPS that totally isolates the critical load from the power line. Most computers include some type of power line filtering as well as a regulated dc power supply. However, the sheer magnitude of many power disturbances can simply overwhelm these circuits. A definite gap exists between the responsibility of the computer designer and that of the power utility. How far a designer can go to bridge that gap by allowing for the basic power disturbances depends on his budget. Three general types of devices can correct power line aberrations without resorting to the overkill of a full UPS: isolation transformers suppress line noise by attenuating the passage of transients from primary to secondary windings; voltage regulators compensate for line voltage fluctuations; and line conditioners provide both noise rejection and regulation, combining the characteristics of isolation transformers and voltage regulators.

Isolation Transformers

Ordinary power transformers with separate primary and secondary windings provide dc isolation but inductively couple fluctuations (normal-mode noise) to the secondary with an increase in coupling as frequency rises. Normal-mode noise coupled to the secondary winding can enter the critical load and trigger digital circuits falsely, causing apparent malfunctions. At the same time, radiated (common-mode) noise picked up on both sides of the ac line is coupled to the secondary through stray capacitance. Fig 1 shows both effects.

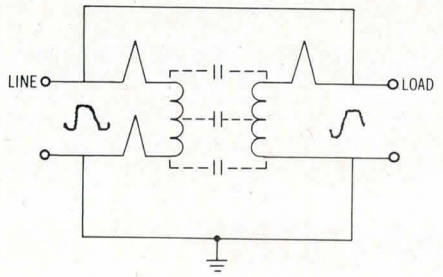

Fig 1 Ordinary power transformer. Inductive coupling passes normal-mode noise directly to secondary. Stray capacitance couples common-mode spike to secondary

To minimize confusion over terminology, manufacturers of isolation transformers have adopted such descriptive terms as *super-isolation* or *ultra-isolation*. Ultra-isolation transformers suppress common-mode noise by incorporating electrostatic shielding, minimizing the capacitance between primary and secondary windings, and shunting the noise to the ground as shown in Fig 2. More sophisticated and effective super-isolation transformers incorporate additional shielding, such as box shields on windings, to further reduce stray capacitance. Depending on the shield design, a super-isolation transformer can reduce common-mode noise coupling by as little as 50 dB (about 300:1 attenuation) or as much as 140 dB (10^7:1). Although 140-dB attenuation sounds impressive, burner igniter transients of 2500 V, automobile ignition transients of 20 kV, lightning strikes, and radio transmissions radiated into power lines acting as antennas can all seriously affect computer performance.

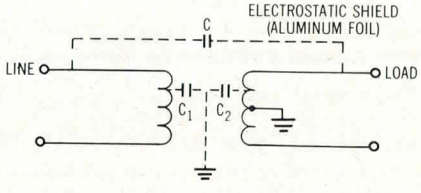

Fig 2 Ultra-isolation transformer. Electrostatic shielding reduces common-mode noise by making C very small. Series combination of C_1 and C_2 is also small, and path shunts common-mode noise from C_1 to ground

In general, selection of super-isolation transformers for use in computer systems should be based on the following considerations: common-mode rejection ratio (CMMR) of 120 to 140 dB up to 10 kHz; intercoupling rejection ratio (ICRR) 10 dB more than CMMR up to 10 kHz; interwinding capacitance of at least 0.001 pF with 0.0005 pF preferred; and, interwinding and winding to core leakage resistance exceeding 10 GΩ.

Isolation transformer connections are critical, and attempting to use a single transformer to isolate two or more devices can seriously degrade its performance. In general, separate transformers must be used whenever signal and common leads return to different grounds. To ensure effective isolation, it is mandatory to follow manufacturer's instructions for connecting the unit.

Isolation transformers can attenuate fast transients, spikes, and high frequency noise, provided that these disturbances are injected into the power circuit as common-mode voltage. No isolation transformer has the ability to compensate for loss of line voltage, slow line voltage fluctuations, normal-mode noise, or frequency variations. During power anomaly diagnosis, it is important to note that common-mode voltages never appear between the input leads of a transformer, but instead appear between one of the input leads and power ground. Therefore, a monitoring device connected between primary winding terminals will not detect common-mode voltage.

Voltage Regulators

When brownouts occur or line voltage fluctuates beyond allowable limits, most computer systems respond by shutting down in an orderly fashion, storing processed data and operating status to facilitate a fast and easy start-up when power returns to normal. However, for many applications, even orderly shutdowns can be prohibitively expensive, particularly if they occur often. A possible solution is a voltage regulator, a device that accepts input from the power line and supplies a relatively constant output voltage, regardless of input voltage variations within a specified range.

One common approach to voltage regulation, the tap changer, incorporates a tapped transformer and a control system that senses the transformer output, automatically changing the turns ratio to offset voltage fluctuations. In Fig 3, the output is sampled at the peak of each cycle and compared to limits derived from a dc reference. If the output peak voltage exceeds the high limit or falls below the low limit, the selected tap is changed to compensate; however, only one tap change can occur during each cycle. The phase sensing circuitry ensures that a tap change can occur only at a zero voltage crossing. Computers normally present a nonunity power factor; therefore, the current leads or lags the voltage by as much as 35°. Although the tap change takes place at 0-V crossings, the current is not at a zero crossing and circulating currents caused by two taps being on simultaneously can damage the tap switches. Tap switches must be greatly overrated in order to sustain this condition.

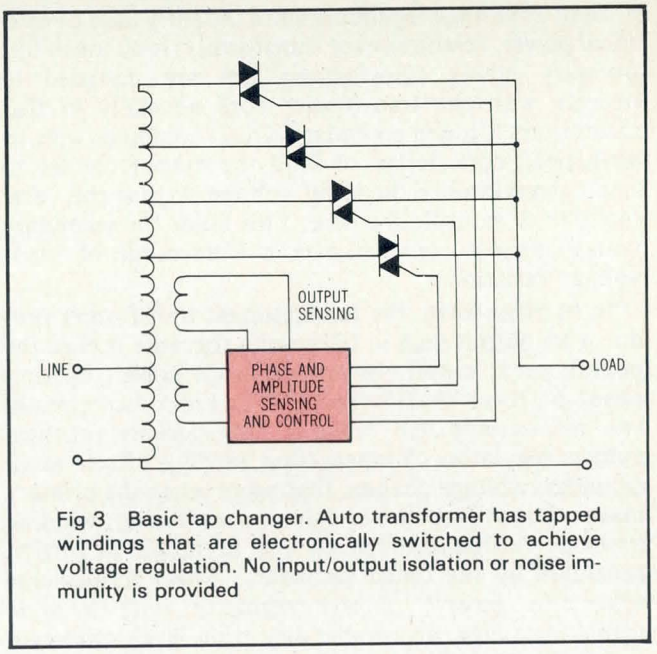

Fig 3 Basic tap changer. Auto transformer has tapped windings that are electronically switched to achieve voltage regulation. No input/output isolation or noise immunity is provided

Another version of the tap changer (Fig 4) combines some advantages of the Fig 3 design with the noise rejection characteristics of a super-isolation transformer. It uses a power transformer with isolated primary and secondary windings and incorporates additional electrostatic shielding. One advantage of the circuit in Fig 4 over the circuit in Fig 3 is that the isolated windings and electrostatic shields provide both dc isolation and 60 to 80 dB of common-mode rejection. On the other hand, this circuit exhibits a drawback shared by most tap changing regulators. The tap switching devices, usually triacs, generate internal noise that, if not properly filtered, can appear at the output.

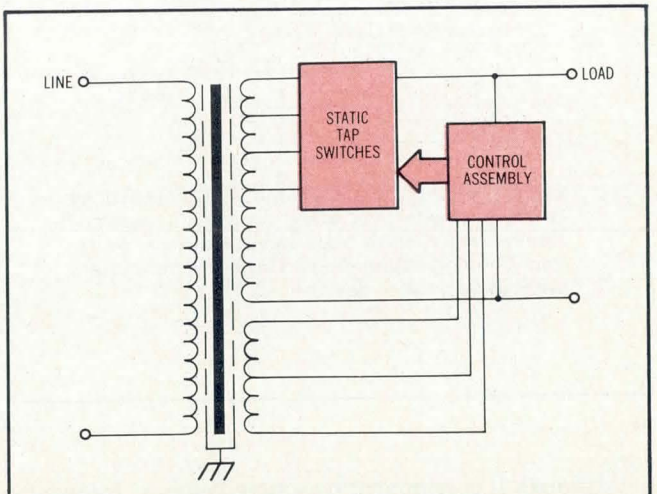

Fig 4 Improved tap changer. Isolated primary and secondary windings plus electrostatic shielding provide both dc isolation and common-mode noise rejection. However, switching devices can generate noise that must be filtered from output

Used as voltage regulators since the early days of electrical power, ferroresonant transformers look much like ordinary power transformers but are designed to operate with the transformer core normally in flux saturation. A tuned secondary circuit combines with an air-gapped core design to limit the output voltage to small changes once the input voltage exceeds the value required to saturate the core. This holds the secondary voltage almost constant over a wide range of input voltage variations.

In its basic form, the ferroresonant transformer produces an output high in harmonics (because it clips the peaks), yet it suppresses normal-mode noise (superimposed on these peaks). The unit in Fig 5 incorporates two refinements that make it an especially practical voltage regulator. Compensating winding offsets small secondary voltage changes that occur when the primary makes large excursions. Also, neutralizing winding develops feedback to cancel the harmonic distortion generated by the tuned secondary. These refinements achieve a passive voltage regulator with a wide regulating range, acceptable distortion level, moderate cost, and high reliability. Its overload characteristics present still another advantage. When the ferroresonant transformer is overloaded, its output voltage can drop to almost zero while output current actually increases. A direct short circuit drawing 150% of full rated current will not damage the design presented in Fig 5.

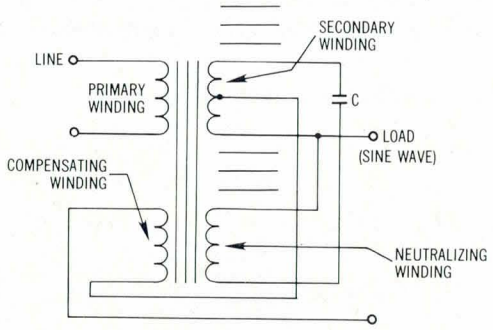

Fig 5 Ferroresonant transformer. Compensating winding offsets secondary voltage fluctuations. Neutralizing winding helps cancel harmonic distortion. Shorting output draws 150% of rated current without damage to device

Although it is regulated by a tuned circuit, frequency effects in the ferroresonant transformer are seldom significant because utilities typically regulate frequency to within 0.05%, and even as much as a 1% change will cause only about a 1.5% change at the transformer output. It shares its most serious shortcoming with most other types of voltage regulator: a complete inability to attenuate common-mode noise. Based on the preceding discussion, it might seem feasible to combine some form of voltage regulator with an isolation transformer to provide more complete protection. In fact, in some instances when a voltage regulator is already in use, an isolation transformer can be added at relatively low cost. However, overall line and load characteristics of two combined devices may differ considerably from those claimed for each unit. Therefore, it is important to evaluate specifications carefully before investing in a hybrid solution.

Line Conditioners

Combining characteristics of isolation transformers and voltage regulators, line conditioners regulate the ac line and provide noise rejection. The combination of voltage regulator and isolation transformer costs less and occupies less cabinet space. Line conditioners come in two basic configurations: one has a linear amplifier with a complex feedback network to cancel the effects of voltage fluctuations and normal-mode noise and electrostatic shielding in the transformer to attenuate common-mode noise; and the other uses a ferroresonant transformer with added electrostatic shielding. The linear amplifier conditioner compares the ac output from an amplifier to a reference derived from a 60-Hz sine wave generator, which is synchronized to the ac line. Any difference between line and reference voltage is applied as a correction voltage to cancel ac fluctuations and normal-mode noise. Primary shielding gives 80 to 100 dB of common-mode noise attenuation and regulation of typically 0.1%, but limited to an input variation band of about ±5 V. Beyond this range the unit passes unconditioned ac power directly to the load. Although it can provide exceptionally clean and stable power when used correctly, its limited range makes the linear amplifier conditioner a poor choice for computers driven by utility power lines.

The ferroresonant line conditioner is a more practical device for protecting computers from ac line fluctuations and noise (Fig 6). Like the ferroresonant transformer, it is a passive device with only a few components, making it extremely reliable. Its regulating characteristics are similar to those of the ferroresonant transformer, providing good line and load regulation over a wide range. Containing no switching devices to generate noise, it typically provides 60 dB of normal-mode noise rejection. In addition, it provides excellent common-mode rejection because it includes electrostatic shielding similar to the shielding in a super-isolation transformer.

A ferroresonant line conditioner selected for computer protection should have: ±3% voltage regulation, or better; less than 5% total harmonic distortion over 50% to 100% of rated load range at a 0.75 power factor; and, CMRR of 120 dB or more between 100 kHz and 1 MHz, with interwinding capacitance of less than 0.005 pF. As these characteristics indicate, a ferroresonant line conditioner is suitable for regulating the ac line and suppressing noise that can cause computation errors; unprogrammed branches, jumps, or halts; reduced throughput; and unreadable data records. Furthermore,

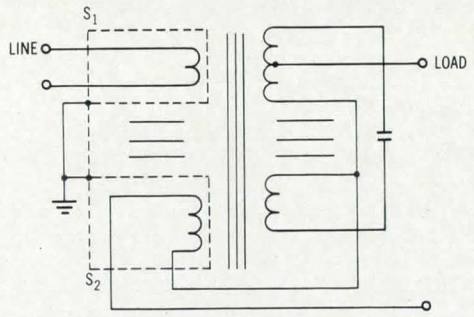

Fig 6 Ferroresonant line conditioner. Box shields S_1 and S_2 minimize common-mode noise coupling from primary to secondary. Combined with shielded primary, this gives ferroresonant voltage regulator many line conditioner characteristics

it costs far less and requires less space than a UPS, and needs no scheduled maintenance. In many installations, a ferroresonant line conditioner can protect a computer from virtually any power line condition except a blackout.

Summary

A UPS provides the ultimate in protection for a computer, but its high initial cost, large size, and stringent maintenance requirements can make it an unaffordable luxury for many of the small computers in use today. Furthermore, in most cases, the blackout protection provided by a UPS is not mandatory. Where transients or noise are disturbing a computer, a super-isolation transformer offers an inexpensive solution that requires no maintenance and negligible floor space. Where line fluctuations exceed the regulating range of the computer power supply, a voltage regulator can be added. The relatively low cost and small size of a voltage regulator make it an attractive alternative to a UPS. Finally, where the line voltage is unstable and noise is present, a line conditioner can correct both conditions, again at a much lower cost. For computer designers, each of these devices offers the opportunity to solve some of the problems over which they have had no control at a price that customers will find far more attractive.

About the Author:

Frank Cathell has worked in solid state failure mechanisms for the QA division of Sperry Rand at Goddard Space Center (NASA) and is now working in solid state power conversion design (mainly high frequency). He has a BS in physics from the University of Maryland and has done graduate work at Catholic University in Washington, DC.

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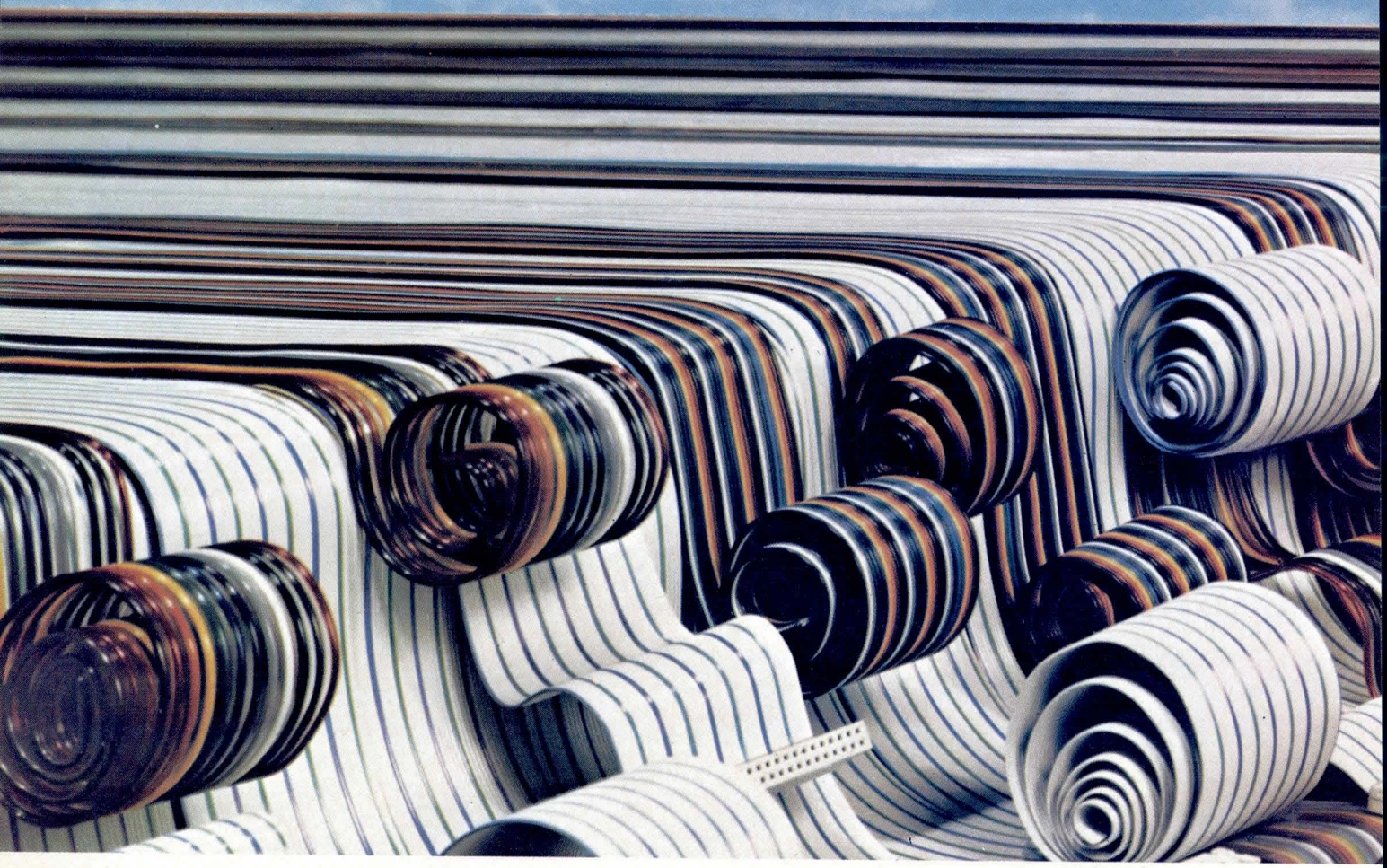

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FEATURE

MULTIPROCESSOR DESIGNS SURPASS SUPERMINI ALTERNATIVES FOR CONTINUOUS SYSTEM SIMULATION

State of the art report extrapolates from benchmark studies to compare cost and effectiveness of alternative hardware and software architectures assembled specifically to perform continuous system simulation

Granino A. Korn University of Arizona
Tucson, AZ 85721

Parallel operation of many computing elements accounts for the high speed of analog computer simulation. By itself, a 1-kHz analog multiplier is much slower than digital multiplication in a typical minicomputer. However, a large simulation can require hundreds of multiplications, which digital computers must perform in sequence. Attaining analog computer speed requires either parallel operation of multiple digital processors, extra fast digital computers, or possibly both. The choice is not clear cut. Since a general purpose simulator made from multiple, standard minicomputers was first proposed, the price/performance ratio of suitable small processors has improved by almost two orders of magnitude. However, the price/performance ratio of larger, faster computers has also improved, and these machines often have better software, fast auxiliary processors, or array processors. Although simulation is relatively well suited to parallel computation, waiting for intermediate results and delays during communication decreases throughput per processor as the number of processors grows. Therefore, it seems inadvisable to consider use of, say, several thousand inexpensive microprocessors for general purpose simulation. Nevertheless, the price/performance ratio of high volume microprocessors seems to improve faster than that of larger computers.

Price and Performance Comparisons

For technical, security, and personal reasons, most continuous system simulation users prefer a dedicated, medium size computer over large mainframe timesharing. The Table, "Computing Speed and System Cost for a Typical 3-Dimensional Flight Simulation," compares cost and performance estimates for various dedicated simulation computer system architectures. In order to investigate possible gains in efficiency from the use of assembly language and microprogramming, it compares systems based on FORTRAN (generated from the system differential equations by the DARE P simulation language translator), MICRODARE™ (a direct execution language using fixed point computation), and the DARE block diagram language. None of this software requires knowledge of assembly language, although the fixed point systems do require scaling. Two microprogrammed MICRODARE systems are also included in the table.

The Table shows that programming convenience outweighs system cost, if much programming and reprogramming must be done, and suggests eliminating the fixed point systems from consideration under these circumstances (parts B and C). Unfortunately, FORTRAN data were not available for the PDP-11/23; however, in

Computing Speed and System Cost for a Typical 3-Dimensional Flight Simulation*

	Relative Speed*	Estimated Cost (x $1000)	Relative Speed/Cost
A. DARE P (FORTRAN based CSSL)			
PDP-11/03, FIS (threaded FORTRAN)	1	11	1
PDP-11/40, FIS (threaded FORTRAN)	3	35	0.9
PDP-11/60, FPU (optimized FORTRAN)	97	60	18
VAX 11/780, FPA (optimized FORTRAN)	274	150	21
SEL 32, FPU (optimized FORTRAN)	174	60	32
PDP-11/34 with APS/120 array processor (FORTRAN subset)	800	180	50
VAX 11/750	164 (est)	90	20
B. MICRODARE [direct executing language (fixed point)]			
PDP-11/03	15	11	15
PDP-11/03, microprogrammed (WCS)	29 (est)	14	22
PDP-11/23	36 (est)	14	29
PDP-11/40	58 (est)	35	18
PDP-11/60	130 (est)	55	26
PDP-11/60, microprogrammed (WCS)	270 (est)	60	50
C. DARE block diagram language (fixed-point, est)			
PDP-11/03	28	11	28
PDP-11/23	69	14	55
PDP-11/40	112	35	35
PDP-11/60	250	55	50
PDP-11/60, microprogrammed (WCS)	400	60	73
D. 10-Processor systems (est, for 80% efficiency)			
PDP-11/03, threaded FORTRAN	8	31	3
PDP-11/03, MICRODARE	104	31	37
PDP-11/03, DARE block diagram language	200	31	71
PDP-11/23, MICRODARE	250	41	67
PDP-11/23, DARE block diagram language	490	41	131
E. 4-Processor systems (est, for 90% efficiency)			
PDP-11/03, threaded FORTRAN	3.6	16	2.5
PDP-11/70 (PDP-11/74), FORTRAN	349	200 (?)	19 (?)
VAX, FORTRAN	986	360 (?)	30 (?)
VAX, 11/750, FORTRAN	592	230 (?)	28 (?)
F. Projection for post-1985 hardware			
Micro-32, FORTRAN	80	20	44
MICRODARE	100	18	61
DARE block diagram language	200	18	122
10 Micro-32, common cache, 80% efficiency, FORTRAN	640	100	70
MICRODARE	750	92	90
DARE block diagram language	1400	92	167

*FORTRAN speeds are based on unpublished preliminary benchmark data by R. Hidinger, Naval Ocean Systems Center.

Estimated system costs include 2M- to 40M-byte disc system, console, and printer, depending on computer size; 11/03 and 11/23 systems have floppy discs.

any case, multiple microcomputers cannot yet compete against 32-bit minicomputers that offer much better floating point hardware, cache memory, greater word length, and generally superior compilers. Multiprocessors made up of four superminis communicating through a common, high speed cache can further upgrade system performance and also improve time-shared system availability (part E). These systems may be preferable to small mainframes in situations where a single 32-bit minicomputer is not adequate. Finally, systems combining a host minicomputer with a FORTRAN based array processor remain less convenient to program than 32-bit minicomputers. Nevertheless, the dramatic floating point computing speed of an array processor makes enhanced systems of this type worthy of consideration.

When some amount of programming convenience can be sacrificed to reduce cost, substitution of a fixed point, block diagram, simulation language dramatically upgrades the computing speeds of the low cost microprocessors (parts B and C). For example, a PDP-11/03 based simulation runs 25 times faster in the DARE

language than in FORTRAN. MICRODARE, about half as fast, compensates by offering direct execution; no compiler or linker is called, and repeated or iterative simulation runs are programmed very conveniently in interpretive BASIC. On microprogrammable computers, such as the PDP-11/03 or -11/60, MICRODARE is actually faster than assembly language.

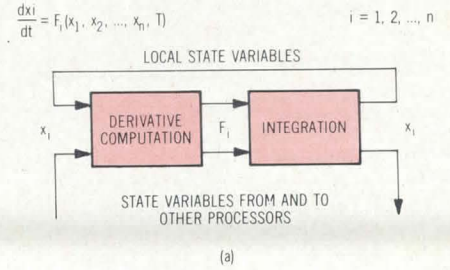
Fixed point languages also yield fast and relatively inexpensive multiprocessor systems (part C). The availability of new, faster, 16-bit microprocessors, which do not appear in the Table, makes these systems even more attractive. Their main disadvantage is the need for scaling. Apart from this, block diagram languages are high level languages that in no sense require knowledge of assembly language.

Hardware Trends Could Change The Outlook

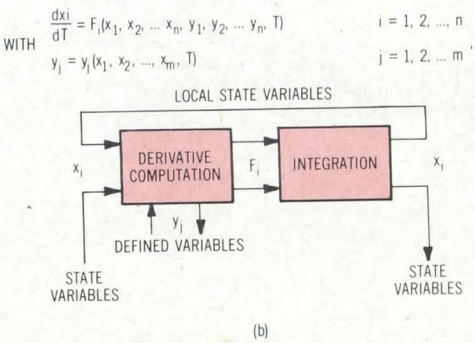
Although even PDP-11/23 class multiprocessors cannot compete with the 32-bit superminis under FORTRAN based simulation, future high end microprocessors will not only combine a 32-bit word length with efficient floating point hardware, but might also be fast enough to need common cache memories in multiprocessor configurations. Therefore, a post-1985 version of parts A to E of the Table might have entries similar to those of part F. These estimates are not farfetched; both floating point chips and microprocessors with 32-bit registers are on the market. These and other developments make microprocessor based simulation—including multiprocessing of FORTRAN based, floating point, equation languages—much more attractive because it is unlikely that supermini cost and speed will improve by more than a factor of two in the same short period.

Increasing Potential For Parallel Execution

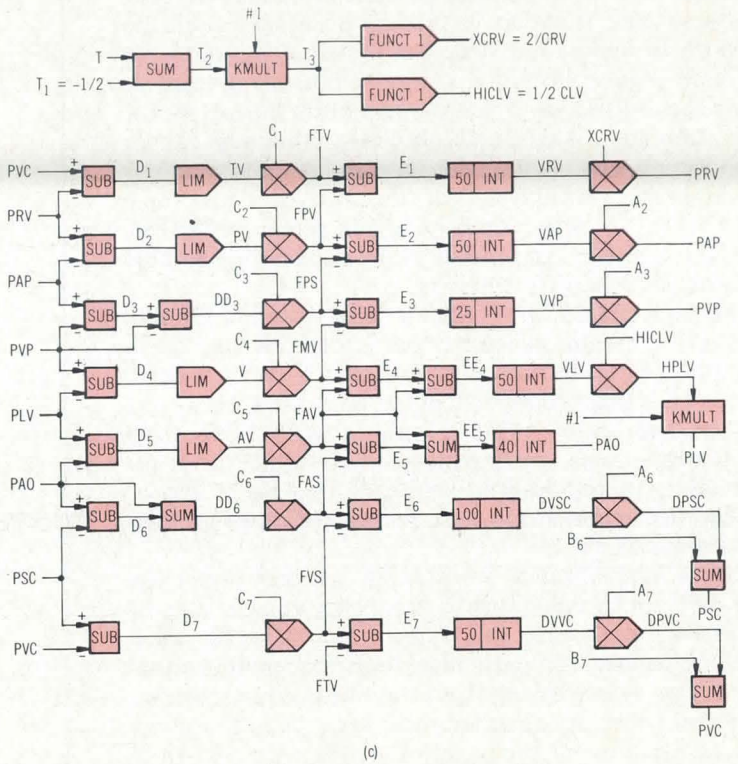
When a simulated system is described by differential state equations of the form shown in Fig 1(a), subsets of these equations can be assigned to different processors.



(a) Subsets of state equations are assigned to different processors. Each processor alternates derivative computation and integration steps. Updated state variables are sent to other processors after each step



(b) If defined variables also must be sent to other processors, transfers cannot wait until end of integration step. However, for systems with very regular equations, only defined variables need be transferred during integration step



(c) Block diagram of actual simulation breaks derivative computation into two phases. Variables FTV, FPV, etc, are transferred between phases. Then, variables PRV, PAP, etc, are transferred at end of second phase. Duplicate variable computation could avoid transfers here, but would be very inefficient

Fig 1 Parallel solution of system state equations

Each processor then alternates parallel computation of derivatives and parallel integration rule steps, updating the corresponding state variables and exchanging updated state variables with other processors. The independent variable, T, can be treated as an extra state variable. No derivative computation can end before all the state variables it needs are updated (although it could conceivably begin earlier). Therefore, although parallel computation is possible, there can be no extensive pipelining.

In order to reduce idle time, efficient multiprocessor programs must partition the set of state equations so that computing times per integration step differ as little as possible among processors. In addition, they must partition the equations so that processors need to exchange as little data as possible. These requirements may or may not conflict. To simplify data driven scheduling of computations that await transfer of updated state variables, all processors can postpone their state variable transfers until one integration rule step is complete. This scheme simplifies both hardware and software, but at some cost in speed.

It is often more efficient to represent a simulated system in the form shown in Fig 1(b), where the defined variables, Y_j, are convenient or useful intermediate results in derivative computations. If both the defined and the state variables must be transferred between processors, these transfers cannot be postponed until the end of an integration step. For system equations with suitably regular structure, it may be possible to transfer only the defined variables at some point during the integration step. Alternately, the integration step can be divided into two stages, with state and defined variables transferred, respectively, at the end of each stage [Fig 1(c)]. In other cases, though often inefficient, variable transfer can be avoided by duplicating variable computation in different processors.

Multiple passes of predictor/corrector and Runge-Kutta integration rules can be overlapped to run in parallel. When the computation load is partitioned in this way, equal processor loading is ensured. However, all of the state variables, along with their state derivatives, must be transferred—thus incurring appreciable communication overhead. This use of special integration methods may also restrict the range of practical applications.

More sophisticated partitioning schemes apportion the differential equations by frequency content and/or linearity, using different integration rules for each distinct segment. In particular, linear differential equations can be separated from nonlinear equations (eg, nominal trajectory equations and perturbed equations), or fast portions of the problem can be separated from slow portions. In this last instance, higher order integration rules or smaller integration steps can be applied to the fast equations or, if these equations are linear and time invariant, the efficient state transition matrix method of integration can be applied. The successful application of partitioned integration techniques to a variety of simulation problems on a single processor nearly doubled computation speed in favorable cases.

Four Alternative Architectures

Four types of multiprocessor systems can be used for simulation. In the first of these, the common memory multiprocessor systems, a local memory associated with each of N execution processors accounts for 80% to 90% of processor memory accesses. The shared data areas needed for simulation reside either in a common memory or in local memories made accessible to other processsors through an interprocessor communication system. The two simplest systems of each type use either a single, priority arbitrated bus to the common memory or a single bus transferring data between local memories. Systems of both types can be built from readily available hardware. Although the single bus presents a bottleneck, use of a common cache memory partially relieves this problem. (See Fig 2.)

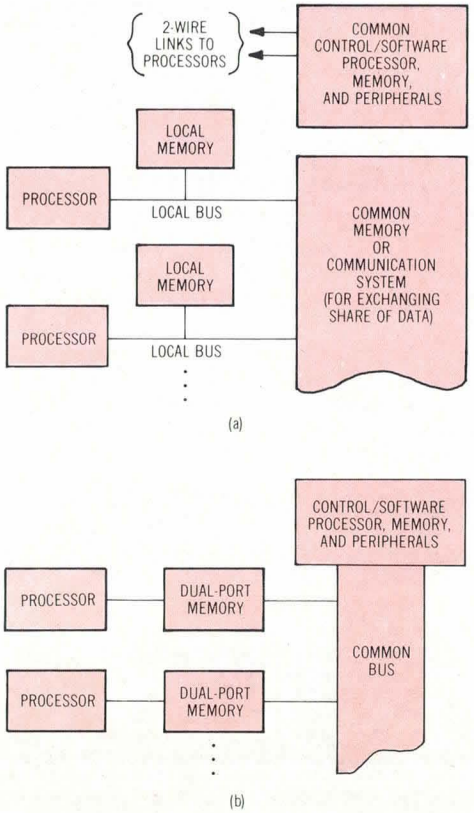


Fig 2 Parallel system architectures. Common memory architecture (a) combines local memories with either shared memory or communication facility. Under dual-port memory architecture (b), memory links processor to common bus. 2- or 3-dimensional processor arrays and data driven configurations are other alternatives

Two much more sophisticated systems, both developed at Carnegie-Mellon University, simulate a large common memory with software arbitrated connections between different processors and memories. C.mmp has a full crossbar switch connecting N processors and N memories, with on the order of 14,000 switch points for 16 PDP-11s. Cm* clusters four to ten processors on local common buses and uses additional buses to interconnect the clusters. In Cm*, an advanced, microprogrammed, communications processor computes effective memory addresses and schedules communications for each cluster. C.mmp was mainly a research vehicle; Cm*, in contrast, could be a very practical, general purpose system if its LSI-11 execution processors were replaced with faster hardware, and if its fast but complicated communications processors could be produced at less cost. A single Cm* cluster would serve nicely for many simulation problems.

In the second type of multiprocessor system, designed specifically for simulation, N dual-port memories connect N execution processors to a common bus controlled by a control/software processor. This processor translates and downloads simulation programs and transfers shared data between the dual-port memories after each integration step. Direct memory access (DMA) hardware on the common bus could serve as a low cost substitute for dual-port memory. Computation phases and data transfers are scheduled by interrupts or, more economically, through memory flag locations. These fast program changes through use of dual-port memories are especially attractive for direct execution systems.

Once again, the common bus becomes a bottleneck, particularly if more than about four processors are used. However, clever partitioning to minimize shared data transfers achieves idle periods proportional to N for N processors. The scheme of Fig 2(b) can be improved substantially by broadcasting a DMA transfer of each processor's shared data region into all other processor memories after each computing step. This economy is most significant in systems that use a large number of processors.

Many simulation problems, and especially network and field models, can be set up so that each processor in a multiprocessor system needs to communicate with only a few neighboring processors. This tantalizing possiblity has led to several proposals for large, 2- or 3-dimensional processor arrays organized along square, cubic, or tetrahedral lattices. In this third type of multiprocessor system, processors are joined by local multiport memories or through local communication processors and various buses. Unfortunately, although execution processors are relatively inexpensive, fast interconnection hardware is not. Programming is complicated as well; consequently, no viable system of this third type yet exists.

The fourth type of multiprocessor architecture, the data driven multiprocessor system, distributes computer operations to various execution processors as soon as the necessary data for each operation becomes available. True data driven systems and their special implementation languages are not yet ready for simulation applications. Fig 3, however, shows a simple, data driven, multiprocessor setup in which each processor is

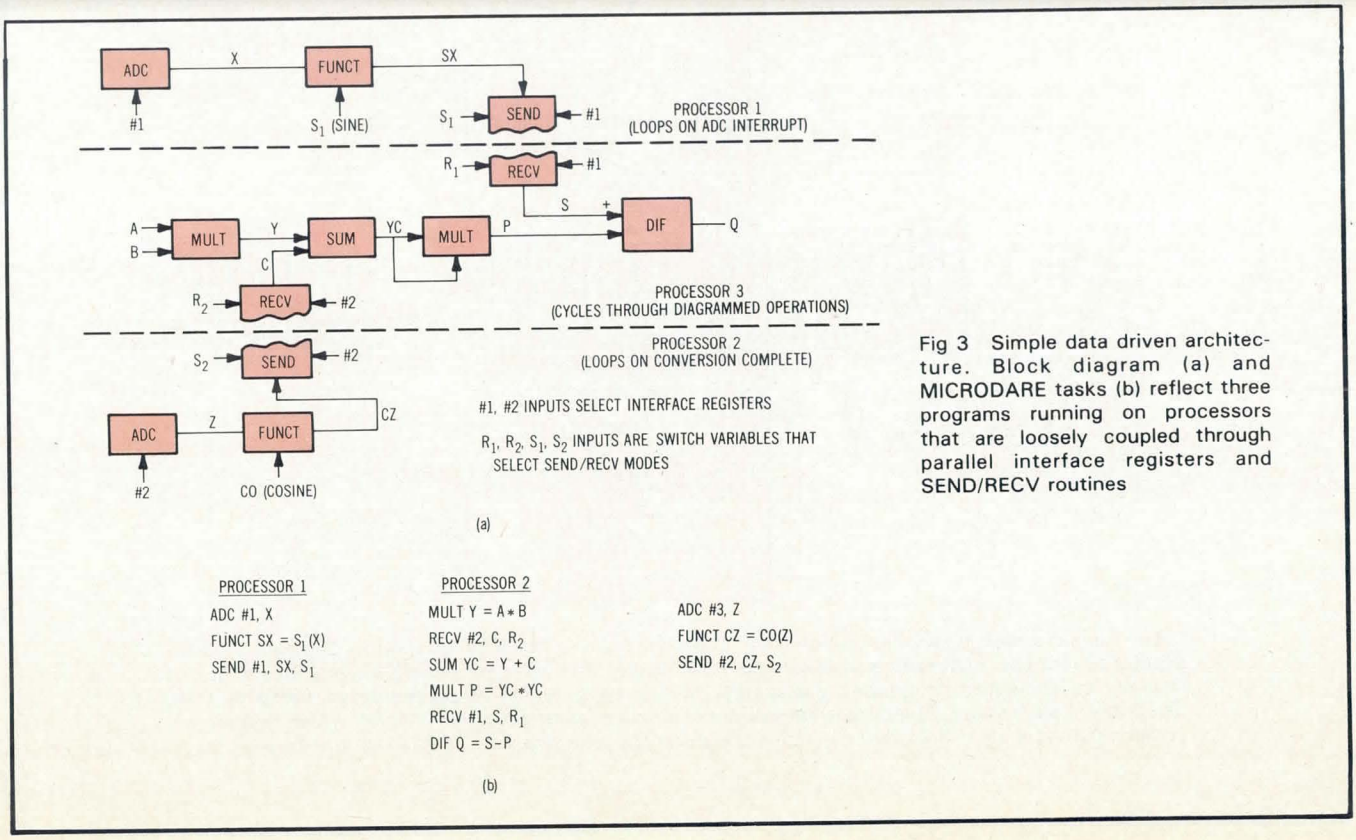


Fig 3 Simple data driven architecture. Block diagram (a) and MICRODARE tasks (b) reflect three programs running on processors that are loosely coupled through parallel interface registers and SEND/RECV routines

preprogrammed to execute part of a MICRODARE program as soon as wait loop (or interrupt driven) interface routines sense that the necessary data can be transferred between processors. The actual system diagrammed in Fig 3 serves a laboratory automation function and allows both pipelining and parallel operation. This scheme is also applicable to simulation, although it would seem to be more suitable for dedicated, special purpose simulators than for general purpose work.

Multiprocessor Software Considerations

In a typical simulation system, the run, integrate, and input/output (I/O) routines are system library components, and the logic control and derivative procedures are translated from the high level language simulation program. Fig 4 shows how a single processor simulation algorithm alternates derivative computations and integration rule passes. Using this approach, partitioned simulation systems are implemented by calling two or more integration routines which, in turn, call corresponding multiple derivative procedures. The high level language program defines system partitions, which are translated into several separate derivative procedures. In a single processor system, various integration and derivative routines are called one after another.

For the multiprocessor system of Fig 3, pairs of integration and derivative routines must be loaded into separate processors. They are invoked in parallel, using a "DO in parallel" call, by a RUN routine that executes in the control processor and starts each execution processor with either an interrupt or a shared memory flag. Multiprocessor language translators must also duplicate shared data areas (for shared state variables and defined variables) in each processor, and the RUN routine must schedule data exchanges between integration rule steps. In a typical RUN routine, language translation, control logic, and I/O execute on the control processor, which has direct access to all peripherals and displays.

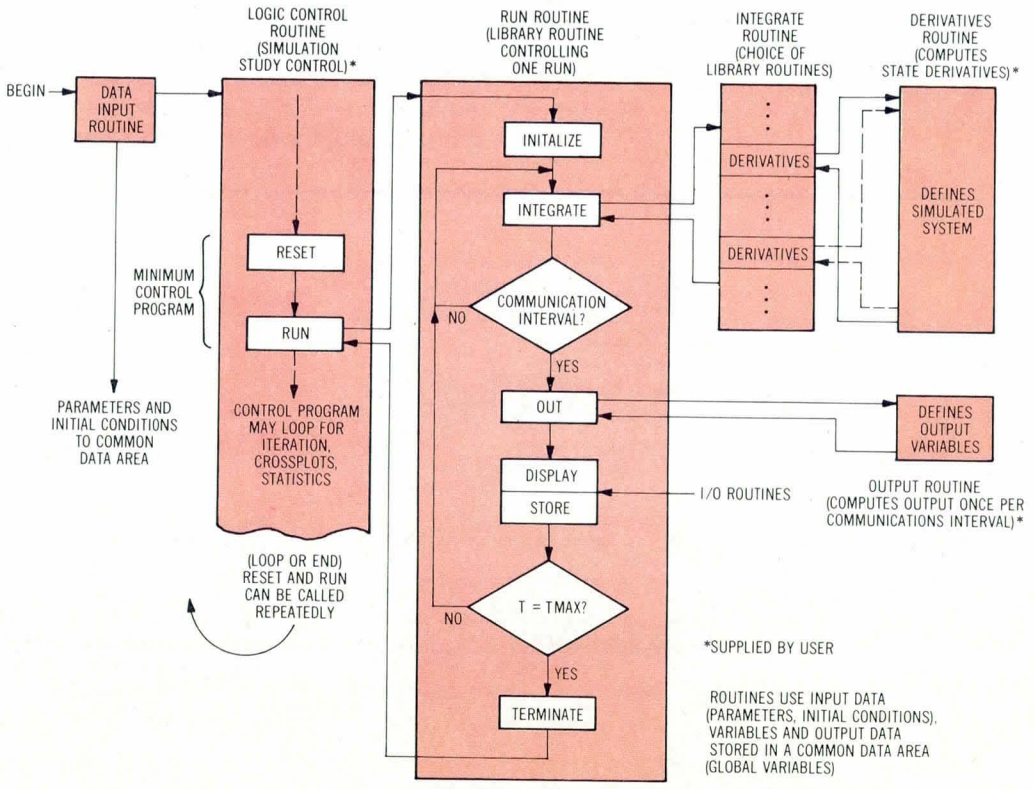


Fig 4 Single processor simulation algorithm. Logic control routine resets integrators and calls iterative simulation routines. RUN routine initializes time and display, then repeatedly calls integration and output routines as simulation progresses. Integration routine calls derivative procedure to compute state derivative at each stage. Output data are computed at end of communication interval, which typically exceeds integration step. Note that derivative computations alternate with integration rule passes

Summing Up Trends in Future Systems

Fast simulation of large dynamic systems is crucial for engineering design and partial system testing in many important applications. The Table's computer performance survey suggests that, for FORTRAN based, floating point, equation language simulation programs, 32-bit superminis are faster and more cost effective than any multiprocessor system built from currently available 16-bit microprocessors. For higher performance in FORTRAN based simulations (ie, faster and/or larger simulations), quadruple superminis and minicomputers teamed with array processors are currently available at the expense of some software development. However, where fixed point, block diagram, simulation languages can be tolerated, systems with multiple 16-bit microprocessors can be more than twice as fast as large, single processor superminis and substantially less expensive. These systems permit fast realtime digital simulation that might otherwise be impossible, as well as cost-effective simulation in training applications.

As fast 32-bit microprocessors with efficient microprogrammed or accessory floating point arithmetic become available, multiple microprocessor systems with up to 16 execution processors will become more cost effective than single processor superminis. In fact, it is likely that by 1985 some superminis will consist of multiple microprocessor systems. By comparison, fixed point simulation languages will offer only a marginal speed advantage. Because the hardware is now under development, it might be advantageous to begin planning multiprocessor simulation systems today, with special emphasis on suitable software and numerical algorithms for parallel computation.

Ideally, a cost effective simulation system should be built from standard, readily available microprocessor components, with essentially no hardware developed especially for simulation. Therefore, multiport memories must either be built by combining standard memory cards with commercially available bus arbitration chips, or be abandoned in favor of commercially available DMA controller circuits.

As to software, an ideal development program would be largely machine independent and would ensure efficient use of the new, 32-bit, floating point microprocessors as they become available. Much earlier, equivalent fixed point software could yield a substantial bonus of fast and inexpensive dedicated simulators and training simulators through the use of existing 16-bit chips.

Interactive simulation will benefit from research on direct execution language systems that return most programming errors as they occur and execute immediately on command without explicit translator, compiler, or linker calls. Direct execution system architectures can be much simpler for relatively restricted application languages (such as simulation languages) than, say, for full feature ALGOL. Primitive direct execution languages have proven enormously successful with early users precisely because of the direct execution feature.

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FEATURE

A DESIGNER'S REVIEW OF DATA COMMUNICATIONS

Efficient communication systems depend on knowledge of design concepts and principles for encoding and transmitting digital data

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Recent developments in information systems and computer and microcomputer hardware have highlighted the need for efficient data communications. Industrialists, educators, financial institutions, and government organizations are finding computer services essential to their operation, and the data communications link is an integral part of these services.

Data communication refers to the electronic transmission of encoded information or data from one point to another. As used here, the term encompasses all the physical elements, systems, devices, and procedures that are required for the transmission and reception of data between two or more points. Elements of a data communication system are communication channels, transmission modes, line conditioning, modems, serial communication interfaces, data link configurations, information codes, and protocols.

The data communication process generally requires at least five elements: a transmitter or source of information, a message, a binary serial interface, a communication channel or link, and a receiver of transmitted information (Fig 1). A data communications interface is often needed to make the binary serial data compatible with the communication channel.

Communication Channels and Facilities

A communications link or channel is a path for electrical transmission between two or more stations or terminals. It may be a single wire, a group of wires, a coaxial cable, or a special part of the radio frequency spectrum. The purpose of a channel is to carry information from one location to another. All channels have limitations on their information handling abilities, depending upon their electrical and physical characteristics.

There are three basic types of channels: simplex, half-duplex, and full-duplex. As an example of each, consider transmission between points A and B in Fig 1.

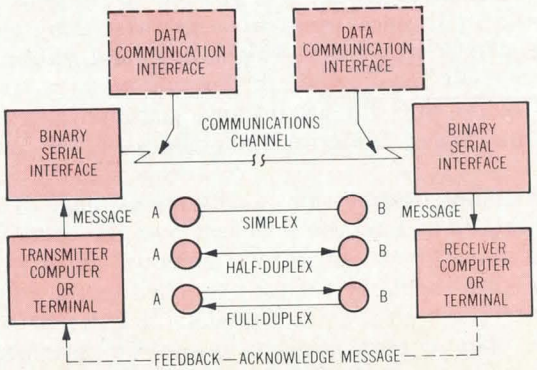

Fig 1 Elements of data communications process. Five major elements are source, message, interface channel, and receiver. Channel can be any of three basic types

Transmission from A to B only (and not from B to A) requires a *simplex* channel. Simplex channels are used in loop mode configurations such as supermarket checkout terminals. Transmission from A to B and then from B to A, but not simultaneously, requires a *half-duplex* channel. If a 2-wire circuit is used, the line must be turned around to reverse the direction of transmission. A 4-wire circuit eliminates line turnaround. Transmission from A to B and from B to A simultaneously describes a *full-duplex* channel. Although four wires are most often used, a 2-wire circuit can support full-duplex communications if the frequency spectrum is subdivided into receive and transmit channels.

In addition to the direction of transmission, a channel is characterized by its bandwidth. In general, the greater the bandwidth of the assigned channel, the higher the possible transmission speed. This speed is usually measured in terms of the number of line signal elements per second, the *baud rate*. If a signal element represents one of two binary states, the baud rate is equal to the bit rate. When more than two states are represented, as in multilevel modulation, the bit rate exceeds the baud rate. The range of channels includes private wire, wideband, Digital Data Service, limited distance, voice grade, subvoice grade, and telegraph (Table 1).

Digital vs Analog Transmission

Digital transmission can be applied to digital data or analog voice signals. In either case, information is sent over the communications channel as a stream of pulses. Pulses transmitted over a communication line are distorted by line capacitance, inductance, and leakage. The longer the line or the faster the pulse rate, the more difficult it is to interpret the received signal. This signal degradation is the reason for the closely spaced regenerative repeaters used in digital data transmission facilities. When noise and distortion threaten to destroy the integrity of the pulse stream, the pulses are detected and regenerated. If the regeneration process is repeated properly, the received signal will be an exact replica of the transmitted signal. It is possible to transmit pulses over short distances using privately owned cable or common carrier wire pairs. This is *baseband transmission* and usually requires line drivers and receivers on each end of the line. Longer distance communication must use the digital transmission facilities of the common carriers.

In analog transmission, a continuous range of signal amplitudes or frequencies is sent over the communications line. Linear amplifiers maintain signal quality. The voice telephone network supplied by the common carriers uses analog transmission facilities to service most data communications users. To interface the analog voice channels to digital terminals and computers, a modulator-demodulator (modem) is used. In a modem, digital information modulates a carrier signal, which passes through the telephone network just as does a voice signal. At the receiving end, the signal is demodulated back into digital form.

Voice Grade Lines

Voice grade telephone lines are available through the public switched network (Direct Distance Dialed or DDD); as private leased lines without conditioning; and as private, conditioned, leased lines. Although the bandwidth is the same for all three, the effective data rates vary because of different specifications for signal noise, amplitude attenuation, and envelope delay distortion.

Dial-up lines are the 2-wire pairs supplied by the common carriers on the public switched telephone network. Most often these lines are used for half-duplex operation, although frequency band splitting modems can facilitate full-duplex at 1200 bits/s. A major advantage of dial-up lines is that any point on a worldwide telephone network can be reached. Furthermore, communication costs are limited to the time the lines are actually in use.

Four major problems are associated with the switched telephone network. First, the lines may be noisy. The human brain can interpret what is being said despite the interference that plagues many calls, but computers and terminals can easily lose or misinterpret data because of noise. Second, delay distortion is caused by the various frequency components of a signal being transmitted at a nonuniform speed through the transmission medium. This may result in received data that are erroneous. Third, the switched network requires relatively long connect, disconnect, and turnaround times, which limit the system data throughput. Fourth, the reliability of telephone switching equipment is relatively low.

Although more costly than dial-up lines, private leased lines largely circumvent the problems that afflict the switched network. Their basic advantages are ready availability and freedom from busy signals, fixed monthly charges, and conditioning for better data quality, as well as higher transmission rates and throughput. Leased lines are generally 4-wire circuits usable for half- or full-duplex operation. Simultaneous transmission and reception is possible, and line turnaround is eliminated. The basic disadvantages of leased lines are higher cost and the line's connection to only one location. However, if telecommunication demands entail high volume, high quality, high speed traffic between two points, a leased line is the best choice.

Digital Data Services

The Bell System has developed a digital transmission network that provides higher data rates with fewer errors at a lower cost than conventional analog transmission facilities. Known as Dataphone Digital Service (DDS), the network is available in 32 U.S. cities and recently has been granted Federal Communications Commission (FCC) approval for 64 other cities. Two point, full-duplex, private line service is provided at synchronous data rates of up to 1.544M bits/s.

In June 1977, the FCC approved construction of American Telephone & Telegraph (AT&T)'s Dataphone Switched Digital Service (DSDS) for 27 cities at data rates

TABLE 1

Communication Channel Characteristics

Channel Type	Channel Interface	Data Rates (bits/s)	Applications
Fiber optics	Fiber optic connector	Up to 10M	Computer-computer, Computer-high speed peripheral
Private wire or cable	Line drivers and receivers Modem eliminators Limited distance modems	1M to 2M	In-plant data communications
Wideband analog	Wideband Bell 300-series modems, CCITT V-series wideband modems	19.2k to 230.4k	Telephone channel multiplexing
Dataphone Digital Service	Data Service Unit Digital Station Terminal	2.4k, 4.8k, 9.6k, 56k, 1.544M	Private terminal-computer geographically dispersed links
Switched telephone network (DDD)	2-wire modems	0 to 2k (async), 2k to 4.8k (sync)	Terminals, data collection stations, other interactive communications
	Acoustic couplers	300, 450, 600, 1.2k (async)	
Leased voice grade lines (with or without conditioning)	2/4 wire modems	0 to 2.4k (async) 2k to 9.6k (sync)	Remote batch, private communications networks
Subvoice grade	Narrowband modems	150 to 200	Teletypes, A-D converters, telemetry
Telegraph	dc signaling	45 to 75	TWX, TELEX

of 56k bits/s. Operations will not begin until AT&T files tariffs for DSDS and proposes an accounting system. Both of these measures must then be approved by the FCC. AT&T has also proposed that DDS and DSDS be included in its heralded Advanced Communications Service message switching network.

Specialized common carriers offer a variety of services in addition to those of the Bell System. These include shared private line services such as EXECUNET by MCI Communications and SPRINT by Southern Pacific; satellite services by the Radio Corporation of America, Western Union, and others; packet-switching carriers including Telenet by General Telephone and Electronics and Tymnet by Tymshare; and facsimile and electronic mail services such as Graphnet, TWX, TELENET, and SPEEDFAX.

Modems

Modems are devices that convert digital data from a computer or terminal to a modulated carrier waveform required by the communication channel. One modem is needed at each end of the channel, as shown in Fig 2. Modems are also known as data sets and are designed for specific kinds of service and for specific bandwidths or data rates. Those discussed here accept a binary serial input from the transmitter and provide a binary serial output to the receiver. Parallel input modems (used mostly for paper tape transmission) and analog input machines (used primarily for facsimile transmission) are not considered. The three types that are considered are short haul, wideband, and voice grade (Table 2).

Short haul modems operate over relatively short distances—generally less than 10 mi (16 km)—on solid conductor, non-band limited, non-loaded lines. In some cases, they are not true modems but are line drivers and line receivers that transmit and receive digital data. Although the communication line must be carefully chosen, the cost can often be one-tenth that of a voice grade modem rated at the speed. Other advantages are higher speed and reliability and easier maintenance.

Wideband modems operate over telephone transmission facilities at speeds of 19.2k bits/s to 230.4k bits/s. This class of data set is supplied almost exclusively by the common carrier and requires the bandwidth of 6 to 60 dedicated voice grade channels. Examples are the Bell 303B, -C, and -D for 19.2k-, 50k- and 230.4k-bit/s full-duplex operation.

Voice grade telephone lines with a bandwidth of 2700 Hz (300 to 3000 Hz) are by far the most common medium used for data communications. A voice grade modem, designed for use on these lines, should be selected on the basis of the type of service (dial-up or leased), the required data rate, and an acceptable level of error performance. The two broad categories of voice grade modems are asynchronous units and synchronous units. Asynchronous units operate at a maximum data rate of 1800 bits/s over dial-up facilities and 2000 bits/s

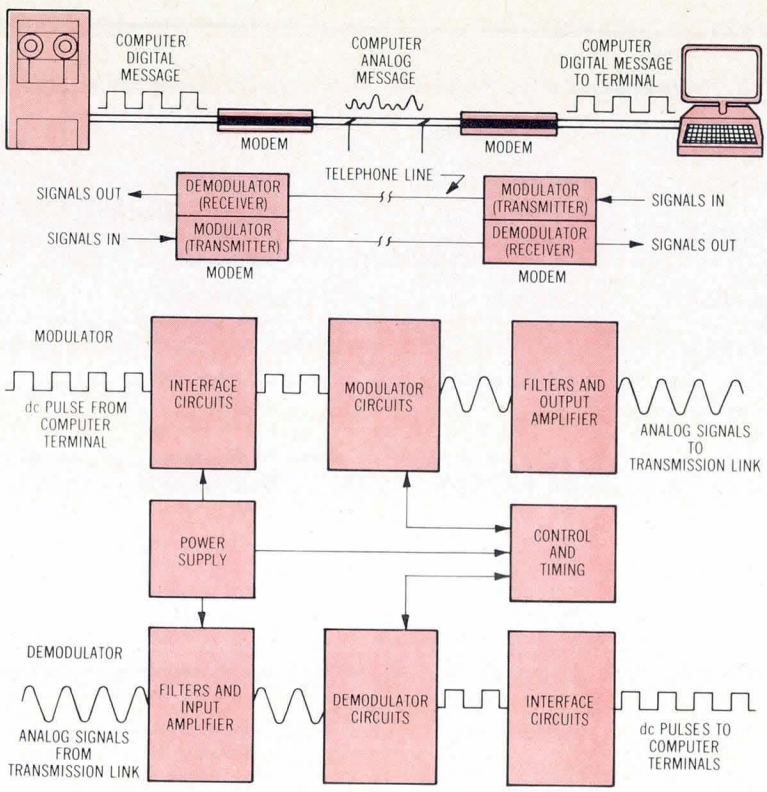

Fig 2 Analog transmission using modems. Modem is divided into two functional segments: modulator and demodulator. Modulator accepts digital input and converts squared dc pulse voltages to analog, audio signals, which are sent over transmission link. At end of link, demodulator of second modem reconverts analog signals to digital output

on conditioned leased lines. Acoustic couplers are asynchronous modems designed for dial-up use that are generally limited to speeds of 600 bits/s or less. Synchronous units operate at a maximum data rate of 4800 bits/s over dial-up and 9600 bits/s on conditioned leased lines.

Asynchronous and Synchronous Transmission

Asynchronous data are typically produced by low speed terminals with rates of less than 1200 bits/s. In asynchronous systems [Fig 3(a)], the transmission line is in a mark (binary 1) condition in its idle state. As each character is transmitted, it is preceded by a start bit, or transition from mark to space (binary 0), which indicates to the receiving terminal that a character is being transmitted. The receiving device detects the start bit and the data bits that make up the character. At the end of the character transmission, the line is returned to a mark condition by one or more stop bits, and is ready for the beginning of the next character. (An asynchronous character varies in length depending on the information code employed.) This process is repeated character by character until the entire message has been sent. The start and stop bits permit the receiving terminal to synchronize itself to the transmitter on a character by character basis.

Synchronous transmission [Fig (3b)] uses an internal clocking source within the modem to synchronize the transmitter and receiver. Once a synchronization character (SYN) has been sensed by the receiving terminal, data transmission proceeds character by character without the intervening start and stop bits. The incoming stream of data bits is interpreted on the basis of the receive clock supplied by the modem. This clock is usually derived from the received data through a phase locked loop. The receiving device accepts data from the modem until it detects a special ending character or a character terminal count at which time it knows that the message is over. The message block usually consists of one or two synchronization characters, a number of data and control characters (typically 100 to 10,000), a terminating character, and one or two error control characters. Between messages, the communication line may idle in SYN characters or be held to mark. Note that synchronous modems can be used to transmit asynchronous data, and, conversely, asynchronous modems can be used for synchronous data if the receiving terminal can derive the clock from the data.

Asynchronous transmission is advantageous when transmission is irregular (eg, when it is initiated by a keyboard operator's typing speed). It is also inexpensive because of the simple interface logic and circuitry required. Synchronous transmission, on the other hand, makes far better use of the transmission facility by eliminating the start and stop bits on each character. Furthermore, synchronous data are suitable for

TABLE 2

Modem Characteristics

Modem Type	Communications Channel	Data Rate (bits/s)	Use
1. Voice grade (vg)			
a. High speed synchronous	Leased line (3002) Dial-up	4.8k, 7.2k, 9.6k 4.8k	High volume machine to machine communications. 600 to 1200 bits/s
b. Medium speed synchronous Medium speed asynchronous Medium speed asynchronous	Leased line/dial-up Leased line Dial-up	2.4k, 3.6k 1.8k, 2k 1.2k	Interactive or low speed remote batch operations. 150 to 300 bits/s
c. Low speed asynchronous	Dial-up	300, 600	Interactive teleprinters and glass teletypewriters, data acquisition and collection. 30 to 60 bits/s
2. Wideband			
a. Super group (60 vg) b. Group (12 vg) c. Half group (6 vg) d. Lineplexer (2 vg)	5700, 5800 (TELPAK) 8801 8803 2 leased lines	230.4k 40.8k, 50k, 56k 19.2k 19.2k	Large volume telephone line multiplexing, dedicated computer to computer links
3. Short haul			
a. Limited distance [<10 mi (<16 km)]	Private wire/cable Nonloaded, non-conditioned, non-carrier line	2k to 1M 2k to 19.2k	Data communications in plant (private wire) or off premises where distance is <10 mi (<16 km) [(leased line)]
b. Medium distance [<50 mi (<80 km)]	Leased line	2k to 9.6k	Intermediate distance [10 to 50 mi (16 to 80 km)]
4. Modem eliminators and line drivers/receivers	Private wire/cable	2k to 1.544M	On-premises data communications. Typical distances are 500 ft (152 m) to 2 mi (3.2 km)

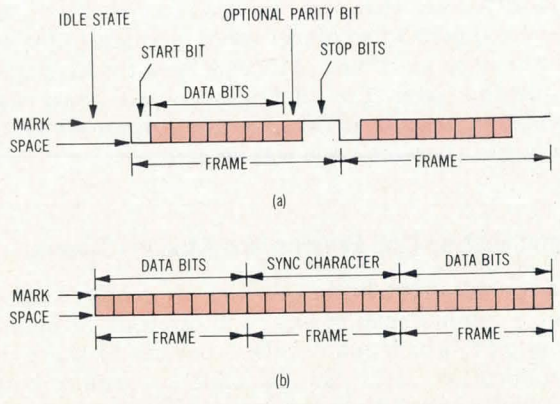

Fig 3 Asynchronous and synchronous transmission. Choice of proper timing mode depends directly on application. Asynchronous transmission (a) is used mostly with man-machine interfaces; synchronous transmission (b) offers high speed necessary for machine-machine communication

multilevel modulation, which combines two or four bits in one signal element (baud). This can facilitate data rates of 4.8k- or 9.6k bits/s over a bandwidth of 2.4 kHz. Synchronous modems offer higher transmission speeds, but are more expensive because they require precisely synchronized clock and data.

Modulation Techniques

Whether to use the dial-up network or leased lines depends on how the modem modulates data prior to sending them over the phone line. Certain modulation techniques permit higher transmission rates than others, and all modulation techniques directly affect the maximum data rate and the error performance. The three basic modulation techniques are frequency shift keying (FSK), amplitude modulation (AM), and phase modulation (PM) (Fig 4).

The most popular form of frequency modulation is FSK, in which the carrier frequency (operating at, say, 1700 Hz) is modulated ±500 Hz to present binary 1 or binary 0. Thus, a frequency of 1200 Hz represents a

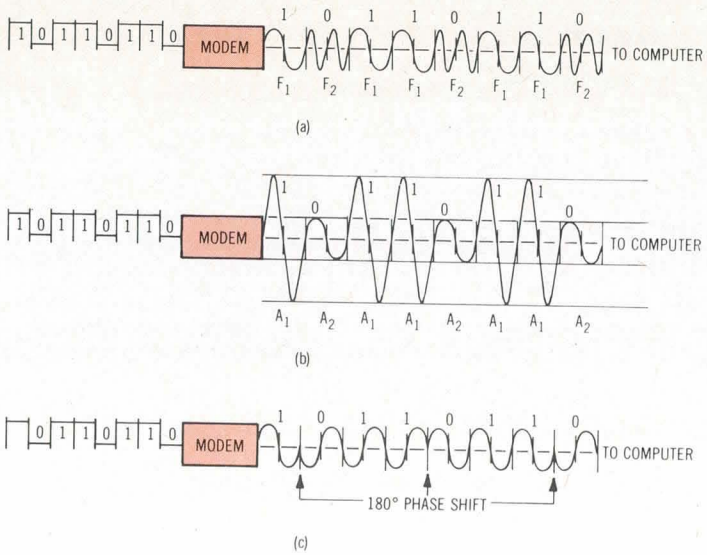

Fig 4 Modulation techniques. In frequency shift keying (a), digital signal (left) received by modem is shifted in frequency to represent binary 1 and binary 0. Because of the time needed to shift from one frequency to another, two is generally the maximum number used. In amplitude modulation (b), digital signals are amplitude modulated by modems using this technique. Here, one carrier signal amplitude (A_1) represents binary 1, and another (A_2), binary 0. In phase modulation (c), whenever 180° phase shift is encountered, receiving mode assigns value of binary 0; at all other times, value of binary 1 is assumed

zero, while a frequency of 2200 Hz represents a binary 1. FSK techniques are generally quite suitable for low speed devices like teleprinters and allow operation at speeds as high as 1800 bits/s.

AM enables a modem to transmit and receive the analog equivalents of binary 1s and 0s. This technique involves varying the amplitude of the line's carrier frequency. Several levels of amplitude modulation are possible, allowing twice as much data to be sent in the same time frame. Both AM and FSK are quite suitable for data transmission; however, FSK has a noise advantage over AM, and AM allows more efficient use of the available bandwidth.

PM modems are generally described in terms of the number of phase shifts generated, and operate at speeds of 2000 bits/s and above. In this technique, the transmitted signal is shifted a certain number of degrees in response to the pattern of bits coming from the terminal or computer. For example, in a 2-phase PM modem, if the analog signal generated by the transmitting modem is shifted 180°, a binary 1 (or 0 if desired) is indicated. If there is no shift, then the signal will be interpreted as a series of zeros (or ones) until such a shift is sensed. Generally, PM modems operate in four and eight phases, permitting up to two or three times the data to be sent over the line in the same bandwidth. Most 4800- and 9600-bits/s modems use PM.

Conditioning and Equalization

As data in the form of analog signals are sent down the line between modems, they suffer from the effects of envelope delay and amplitude distortion. Signals of different frequencies are delayed or attenuated by varying amounts as they are transmitted. To compensate for these effects, two techniques are employed: line conditioning and modem equalization.

Conditioning is the process by which the telephone company maintains the quality of a specific, privately leased line to a certain standard of permissible delay distortion and signal attenuation. AT&T has two types of conditioning referred to as C and D. There are five categories of C conditioning (C1 through C5) and two categories of D conditioning (D1 and D2). C conditioning atempts to equalize the drop in signal voltage and envelope delay for all frequencies transmitted; D conditioning controls the signal to noise ratio and harmonic distortion. Both may be used on the same communication channel.

Equalization refers to modem compensation for amplitude and envelope delay distortion of the line. Equalization is seldom required in lower-speed modems attached to a leased line, since minimum line conditioning is sufficient. However, conditioning and equalization are required when higher speed modems (4.8k- and 9.6k bits/s) are attached. Modems used for high speed transmission over the dial-up network must have equalization, since it is never certain exactly which unconditioned telephone line will be used.

Communication Line Sharing and Modem Sharing

When several input/output devices are required at one end of a communication link, a multiplexer or modem sharing unit, which enables these devices to share one communication line, can be used to reduce costs. Multiplexers take low speed inputs from a number of terminals and combine them into one high speed data stream for simultaneous transmission on a single channel. At the other end of the link, a second multiplexer (actually a demultiplexer) reconverts the high speed data stream into a series of low speed inputs to the host computer. The channel is split into time slots (time division

multiplexing) or frequency bands (frequency division multiplexing). Intelligent or statistical multiplexers increase line utilization by allocating time slots on the basis of a line activity algorithm.

Modem sharing units enable multiple terminals to share one modem. They are particularly valuable in networks that require clusters of terminals at remote sites because the number of modems and transmission lines are reduced. Operation is polled half-duplex. Multiport modems can split a high speed channel (eg, 9600 bits/s) into various medium speed channels (eg, two 2400 bits/s and one 4800 bits/s), thus permitting several medium speed terminals to share a 9600-bit/s line. A miniplexer is a device that performs channel splitting for DDS as well as for a single 3002 leased line. A lineplexer or biplexer splits 19.2k-bit/s data into two 9600-bit/s paths that can be transmitted over two conditioned full-duplex channels. This eliminates the need for a wideband channel to send and receive data at 19.2k bits/s. A port sharing unit connects to a communication controller or central processing unit port and transmits or receives data from two to six terminals or modems. Less costly than a multiplexer, it reduces the number of controller ports in a polled terminal data communications configuration and makes more efficient use of connected ports.

Standards and Protection

The electrical, functional, and physical interface to data terminal equipment provided by modems is compatible with Electronics Industries Association (EIA) or International Consultative Committee for Telephone and Telegraph (CCITT) standards. Most commercial models conform to EIA RS-232, and plug to plug compatibility via a 25-pin connector is ensured between modems and data terminal equipment that subscribe to this standard. CCITT V.26 is the electrical equivalent of RS-232-C, while V.24 is the U.S. standard's functional pin equivalent. CCITT V.35, a current-mode, 34-pin connector interface standard for serial data transmission up to 56k bits/s, is used by wideband European modems and in the Bell System DDS Data Service Unit at 56k bits/s. Military standard (MIL-STD) 188 is a U.S. government standard for military communications equipment. An improved EIA functional standard, RS-449, was approved in November 1977. Although not yet implemented in U.S. modems, it is being incorporated into modems used in Germany and in the CCITT V.36 modem.

Common carrier equipment on the switched telephone network must be protected. A device called a data access arrangement (DAA) limits the attached modem's signaling power to prevent it from exceeding the power level restrictions of the communication channel. In 1977, the FCC ruled that modem manufacturers can incorporate equivalent protective circuitry in their products, register them with the FCC, and connect them directly to the telephone network. DAAs are available from FCC-certified independent suppliers and can be leased from the Bell System. Modems rented from the Bell System or those used on leased lines do not require a DAA.

Protocols

Protocols provide the necessary ground rules to ensure the orderly and accurate transfer of data between digital devices. Data communications protocols are growing in importance as the terminal population increases, distributed processing becomes widespread, and new communications technologies, such as packet switching and satellite links, become commonplace.

Protocols associated with data communications have several major levels, or layers, that define various functions and operations. Each level is designed to be functionally independent of the others, but the function of each depends on the correct operation of the previous level. The protocols embodied in these levels range from those that define the physical and electrical links, eg, RS-232-C and CCITT V.35, to those that are responsible for functions such as message buffering, code conversion, recognition and reporting of faulty conditions in terminals or lines, communication with the host mainframe, and management of the communication network. They are implemented by software packages like International Business Machines (IBM)'s Systems Network Architecture (SNA), CCITT's X.25, and Digital Equipment Corporation (DEC)'s DECnet.

The remainder of this article concerns data link control protocols (DLCs), the sets of rules necessary for effective communication between terminals and computers over conventional communications channels. DLCs are involved in handling the communications link itself and moving information across it efficiently and accurately. Their basic functions are to establish and terminate a connection between two stations; to ensure message integrity through error detection, requests for retransmission, and positive or negative acknowledgments; to identify sender and receiver through polling or selection; and to handle special control functions such as requests for status, station reset, reset acknowledge, start, start acknowledge, and disconnect.

Structure of Data Link Controls

Data link controls can be classified into byte control protocols (BCPs) and bit oriented protocols (BOPs). In BCPs, a defined set of communication control characters effects the orderly operation of the data link. These control characters are part of a character code set. BCP messages are transmitted in blocks composed of a header or control field, a body or text field, and a trailer or error checking field with characters used as field or block delimiters. Examples of BCPs are IBM's Binary Synchronous Communications Protocol (BISYNC) and DEC's Digital Data Communications Message Protocol (DDCMP). Block formats for these are illustrated in Fig 5.

BOPs use only two or three specific control characters for operation of the data link. These characters are used to delimit the beginning (FLAG) and end (FLAG, ABORT, GA) of a message frame. Upon receipt of the opening FLAG, positional significance is used to delineate the bit sequence that follows into prescribed fields (Fig 5).

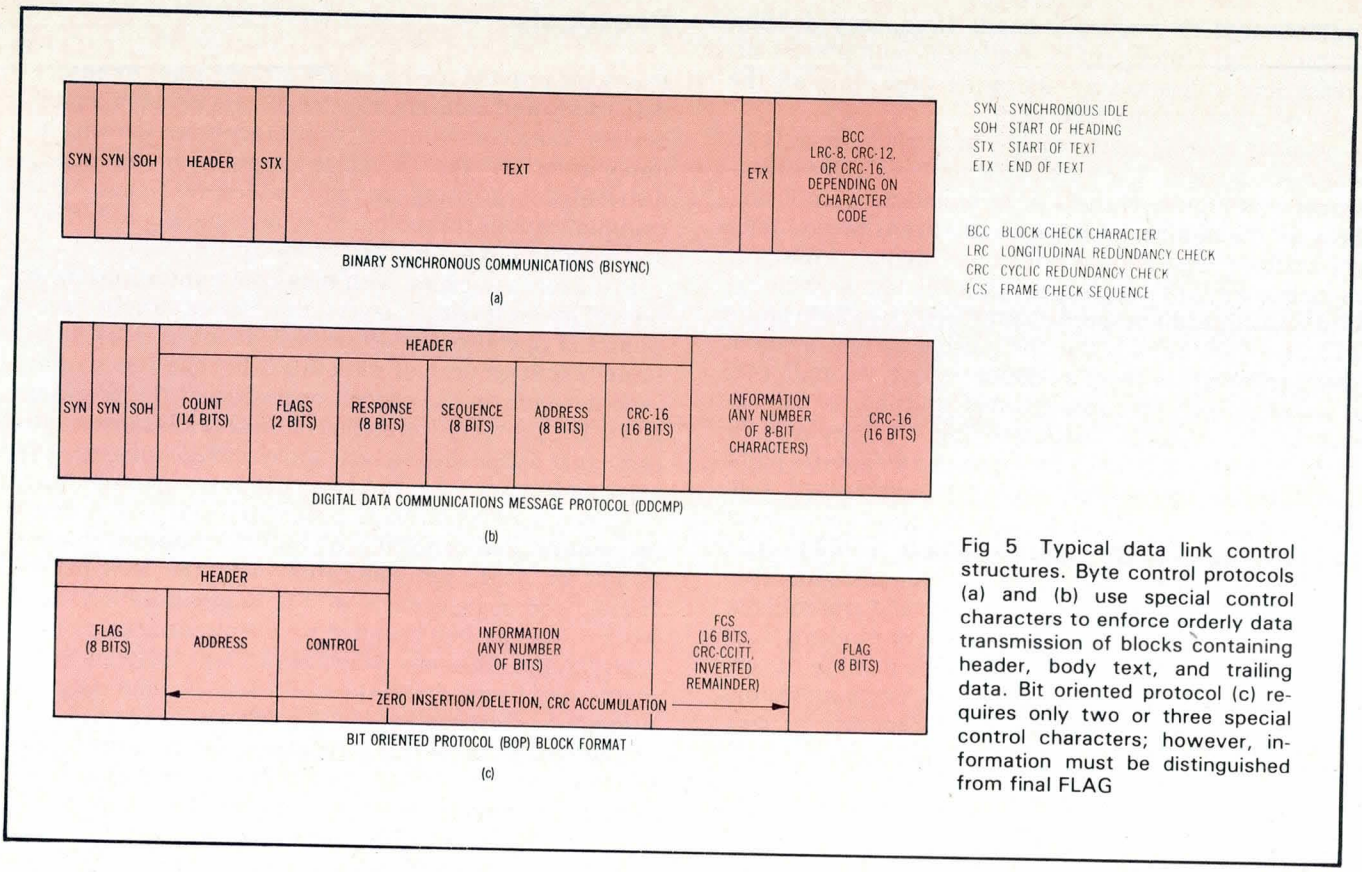

Fig 5 Typical data link control structures. Byte control protocols (a) and (b) use special control characters to enforce orderly data transmission of blocks containing header, body text, and trailing data. Bit oriented protocol (c) requires only two or three special control characters; however, information must be distinguished from final FLAG

These fields are address, control, information, and frame check sequence. The address, control, and frame check fields are of fixed length; the information field length is variable and may be zero.

BCP Messages

As already stated, BCP messages are transmitted in units called blocks. The header field contains auxiliary information that identifies the address of the message destination or source, the job number (if any), the type of message (data or control), the control action, and a positive or negative acknowledgment to ensure error-free reception of a previous message (or messages). Control actions are used to reset or initialize a secondary station, to acknowledge good or bad reception of blocks, to inquire why a response or acknowledgment has not occurred within a specific time period, or to abort a transfer sequence. The control information is conveyed via special characters or character sequences.

The text field contains any data being transmitted. The text may be characters of the information code set or may be transparent to that code set. In the latter case, pure data (binary, packed decimal, floating point), specialized codes, or machine language computer programs must be distinguished from characters in the code set being used. This is done by employing a transparent mode whose implementation depends on the specific DLC.

To ensure correct reception of information over communication facilities, a sequence of check bits, often called block check characters or BCCs, are generated and transmitted as an error check field. Each block of data transmitted is checked for errors at the receiving station in one of several ways, depending on the code and functions employed. These checking methods include vertical redundancy check (VRC), a parity check on each character, in conjunction with a longitudinal redundancy check (LRC), a horizontal parity; and cyclic redundancy check (CRC), which involves a polynomial division of the bit stream by a CRC polynomial.

BOP Messages

BOPs are more straightforward and universal than the BCPs just discussed. BOP messages are also transmitted in frames, and all messages adhere to one standard frame format. Common characteristics of BOPs are the independence of codes, line configurations, and peripherals; the use of positional significance instead of control characters or character counts; one standard frame format for all messages; the possibility of half- or full-duplex operation; the achievement of information transparency through zero insertion and deletion; and error checking on a complete frame.

A frame starts with the 8-bit FLAG sequence, followed in order by the sequences ADDRESS, CONTROL, INFORMATION (if present), and FRAME CHECK, and ends with another FLAG sequence. Each station attached to the data link continuously searches for the FLAG sequence and an ADDRESS sequence. In multipoint operation, for example, a secondary station must detect a FLAG immediately followed by its own ADDRESS to enable the receiver.

TABLE 3

Common Protocol Characteristics

Feature	BISYNC	DDCMP	SDLC	ADCCP
Full duplex	No	Yes	Yes	Yes
Half duplex	Yes	Yes	Yes	Yes
Message format	Variable	Fixed	Fixed	Fixed
Link control	Control character, character sequences, optional header	Header (fixed)	Control field (8 bits)	Control field (8/16 bits)
Station addressing	Header	Header	Address field (8 bits)	Address field (8 bits to 00)
Error checking	Information field only	Header, information field	Entire frame	Entire frame
Error detection	VRC/LRC-8 VRC/CRC-16	CRC-16	CRC-CCITT	CRC-CCITT
Request for retransmission	Stop and wait	Go back N	Go back N	Go back N, selected reject
Maximum frames outstanding	1	255	7	127
Framing—start —end	2 SYNs Terminating characters	2 SYNs Count	Flag Flag	Flag Flag
Gaps between characters allowed	Yes	No	No	No
Information transparency	Transparent mode	Inherent (count)	Inherent (zero insertion/ deletion)	Inherent (zero insertion/ deletion)
Control characters	Numerous	SOH, DLE, ENQ	None	None
Character codes	ASCII EBCDIC Transcode	ASCII (control character only)	Any	Any

When the primary station transmits, the station ADDRESS sequence, which is usually one 8-bit field, designates which secondary station is to receive the balance of the transmitted frame. When a secondary station transmits, the ADDRESS tells the primary station which secondary station originated the frame. A secondary station must recognize its valid address before it can accept a frame and take any action on the contents of that frame. Also, the primary station will accept a frame only when it contains the address of a secondary station that has been given permission to transmit. To ensure the integrity of the data being transmitted, the ADDRESS sequence appears within each frame. This enhances flexibility in that the primary station can interleave receptions from several secondary stations without intermixing individual station information transfers.

The CONTROL field follows the ADDRESS sequence and is composed of one or two 8-bit bytes, depending on the protocol implementation. It is the heart of the BOP message, for it determines the type of message, the send and receive frame sequence counts, and a poll command from the primary station or final response from the secondary station. The primary station uses CONTROL to tell (command) the addressed secondary station what operation to perform. The secondary station uses CONTROL to react (respond) to the primary station.

The INFORMATION field may vary in length; this includes different lengths in the sequential frames making up a complete transmission. The data may be configured in any code structure: straight binary, binary coded decimal, and packed decimal, among others. However, the content of the field must be self-defining by actual or implied means. For example, peripheral device control characters, such as carriage return, will actually be part of the INFORMATION field, while the code being used may be implied in the address of a specific terminal designed for a specific code. Furthermore, whether a frame contains an INFORMATION field at all depends on the particular CONTROL format transmitted. table 3 presents a comparison of common DLCs.

Synchronization Techniques

Four kinds of synchronization—bit, character, block and message—must be distinguished when using synchronous transmission. Bit synchronization is achieved through a received clock signal which is coincident with the received serial data stream. Most modems or "business machines" (ie, terminals) derive this clock by means of phased lock loops from the 0 to 1 and 1 to 0 transitions occurring in the received data. This technique, called self-clocking, overcomes the effect of propagation delay between distant stations and the tendency of electronic circuits within the modem to drift.

Character synchronization is accomplished by recognizing one or two "phasing" characters, often called SYN or sync characters. The receiver senses these SYN characters and phases its receive logic to recognize, by bit count, the beginning and end of each subsequent character. To ensure character synchronization throughout a message, SYN sequences are sometimes inserted in the transmitted data stream at 1- or 2-second intervals. This permits receiving stations to verify that they are in sync.

Request for Retransmission

As previously mentioned, DLCs include an error checking field to allow the receiving station to validate the message. When errors are detected, the receiving station issues a request for retransmission (ARQ). The two types of ARQs are *stop and wait* and *continuous*. Each provides defined methods for acknowledging correct (error free) reception of transmitted blocks of information.

When a connection is established in the stop and wait ARQ, the transmitter sends one block and then stops. Eventually, the receiver acquires that block, subjects the block to an error check, and then sends an ACK control character to the transmitter to indicate that the block is correct, or a NAK control character to indicate an error. If an ACK is returned, the transmitter sends the next block in sequence. If a NAK is returned, that block is retransmitted. Thus, the stop and wait mode involves periods of idleness, including propagation delays between each block, so that the line is not communicating nearly at its rated capacity.

In continuous ARQ, the transmitter keeps sending one block after another without stopping. The receiver and transmitter retain individual counts of the blocks outstanding and provide buffer storage to retain those blocks. Only when an erroneous block is detected does the receiver tell the transmitter to resend that block and all subsequent in-transit, but unacknowledged, blocks.

Summary

As the installed base of computers and the speed and volume of their output have increased, so has the need to transmit that output to more places over longer distances. Inherent in the data communications process—the electronic transmission of encoded information from one point to another—are various physical elements, devices, and systems, as well as standards and procedures. An understanding of these basic elements and concepts can help users of computer services to take advantage of the communication systems that are now available.

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About the Author:

As applications manager for the microprocessor division of Signetics Corporation, Alex Goldberger is responsible for product applications support, new product planning, and technical marketing support for microprocessors, microcomputers, and associated peripheral circuits. He has worked with integrated circuits since 1969 and was the design manager for the universal asynchronous receiver/transmitter (UART), the first large scale integration circuit for data communications. He holds a BSEE from the City College of New York and an MSEE from the Polytechnic Institute of Brooklyn, and is the author of several articles for technical publications.

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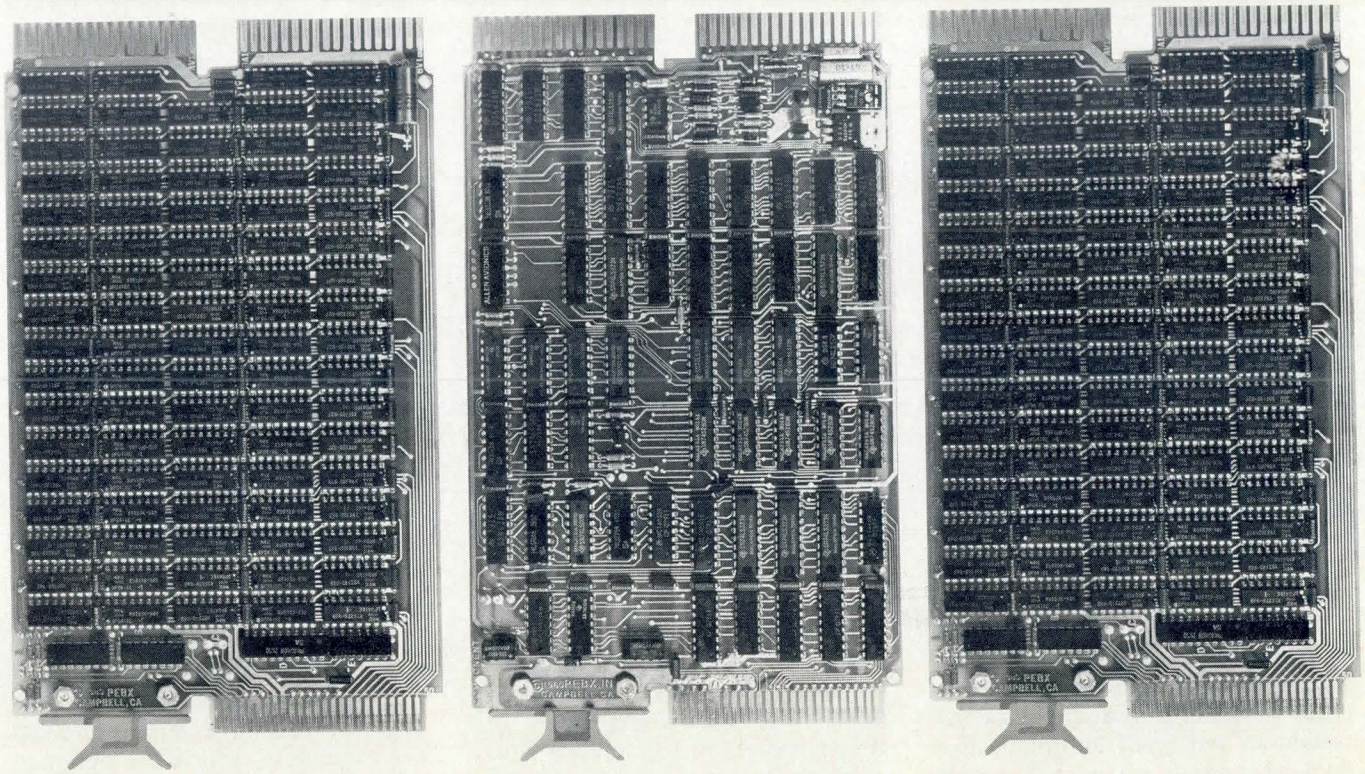

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CIRCLE 61 ON INQUIRY CARD

Embedded Diagnostics Utilize Excess ROM Capacity

Self-contained test routines make use of program memory to maintain 8048 based products in the field

Jim Handy

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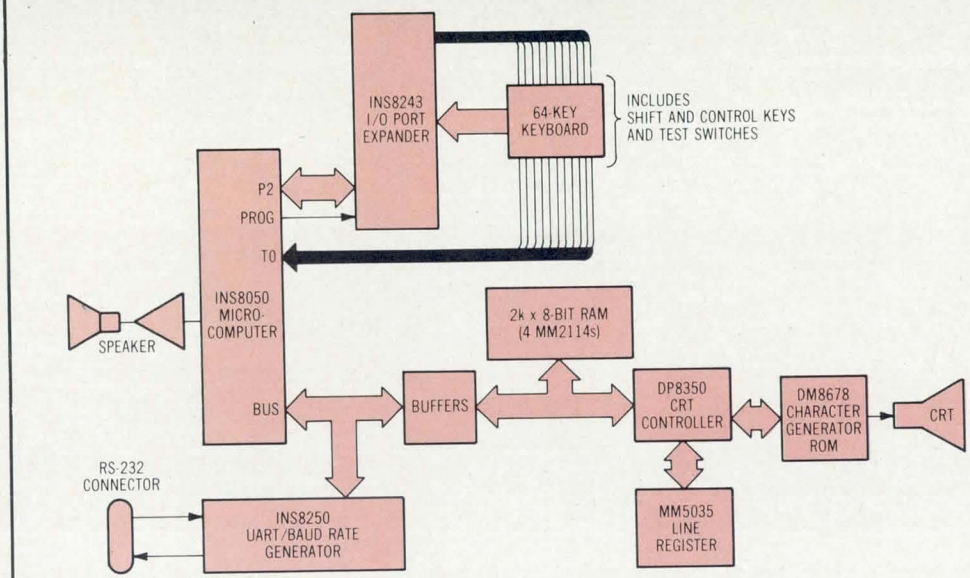
Diagnostic testing is one of the most troublesome and costly problems facing users of microcomputer based systems. Difficult throughout the production process, testing also takes its toll in the field. A variety of techniques can simplify testing procedures in a multiple-chip, microprocessor based design. One very successful approach has been advocated by microprocessor based systems designers, as well as large mainframe manufacturers and makers of telecommunications and consumer products. The technique is to embed diagnostic routines into the program memory of the system to be tested, allowing the device to test itself in its normal operational environment. Self-diagnostic commands are built into the microcomputer system's firmware to allow the system to test itself automatically. Such commands often are invoked by push button or switch.

The self-diagnostic approach has often been regarded as a luxury by those using currently available single-chip microcomputers. The 1k- or 2k-byte limitations imposed by the 8048 and 8049 have made it difficult to squeeze the necessary programs into the onboard read only memory (ROM) of these chips. To add ROM chips for the sole purpose of running diagnostic routines usually would be prohibitive in the kinds of minimum cost systems in which the 8048 family of chips is used most often. Additional ROM chips mean higher component count and higher system costs.

One solution to these problems uses National Semiconductor's INS8050, an upgraded member of the 8048/49 family with a 4k-byte onchip ROM. With this extra ROM, the system program and several diagnostic routines can fit into the chip with room to spare. Through the use of extensive prompts, the designer can use this storage to make the diagnostic routines easier to understand. System hardware requires only minor modifications to accommodate these tests, through the addition of test points and shorting pins to interface the various test loops.

For example, diagnostic self-testing could be incorporated into a cathode ray tube (CRT) terminal application using the 8050 microcomputer. Test routines might include random access memory (RAM) tests, input/output (I/O) device tests, communication tests, and CRT controller tests.

CRT terminal hardware consists of an INS8050 microcomputer chip with 4k bytes of internal ROM and 256 bytes of internal RAM; two INS8243 I/O expanders, which are designed to be used with any device in the 8048 family; an INS8250 universal



CRT terminal block diagram. Typical INS8050 application combines two INS8243 I/O port expanders and INS8250 UART with CRT controller chip, character generator ROM, and screen data RAM. Extra ROM in 8050 can be used to add diagnostic self-test capability without increasing terminal parts count

asynchronous receiver/transmitter (UART) and baud rate generator chip; a DP8350 CRT controller chip, and its associated DM8678 character output ROM; some RAM for the CRT screen data; an 80-character line buffer for the CRT controller; and assorted peripheral buffers. (See the Figure.)

I/O expanders are used to scan the keyboard and self-test switches. The UART serves to transport the data between the terminal and an associated data set. Screen data, which are output to the screen by the 8350 and the 8678, are held in RAM. This RAM can be modified by the 8050, which is used as a central controller to provide the terminal with several "smart" features implemented in its software.

The tests can be initiated by a set of auxiliary switches located within the terminal. Switches should be easily accessible to service personnel, but should not be in the CRT user's way. As part of the main program loop, the 8050 will scan all the keys on the terminal's keyboard as well as the test switches. If a switch is set to test mode, the appropriate test programs will be executed until the switch is returned to normal operation mode. There can be a separate switch for each test in the terminal.

RAM tests can be very simple. The address of the location under test is swapped (the lower 4 bits exchanged for the higher 4 bits), then loaded into that location. After all locations are accessed (for internal and external RAM), the program inverts each location and loads the result back into that location. During the third pass, each location is compared against what its contents should be. If the test fails, a signal can be generated on the same loudspeaker used to give a beep at the end of the line or during a "control-G."

I/O device tests are used to check the INS8243 I/O expander ports shown in the diagram. The keyboard is connected via these expanders, so the test should require keyboard inputs. Service technicians can be prompted by the CRT screen to input characters in a certain order. If the expected keyboard input is not received, the technicians are prompted again. Should the input still be wrong, a suitable error message is displayed on the screen.

Communications tests are initiated after a special EIA RS-232 connector is attached to the back of the terminal to make the INS8250 UART talk to itself. This is a simple go/no go test of all the appropriate RS-232 inputs and outputs. Each signal line is tested independently of the others to allow the detection of short circuits.

Finally, a CRT controller test helps to determine when and where the CRT controller chips are malfunctioning. The microcomputer fills the display RAM with characters suitable to make a display appear on the screen. For instance, diagonal rows of numbers, preceded by a few lines containing every printable ASCII code, might be chosen. Then the service technician simply has to compare the pattern on the screen with those in his service manual in order to pinpoint the trouble.

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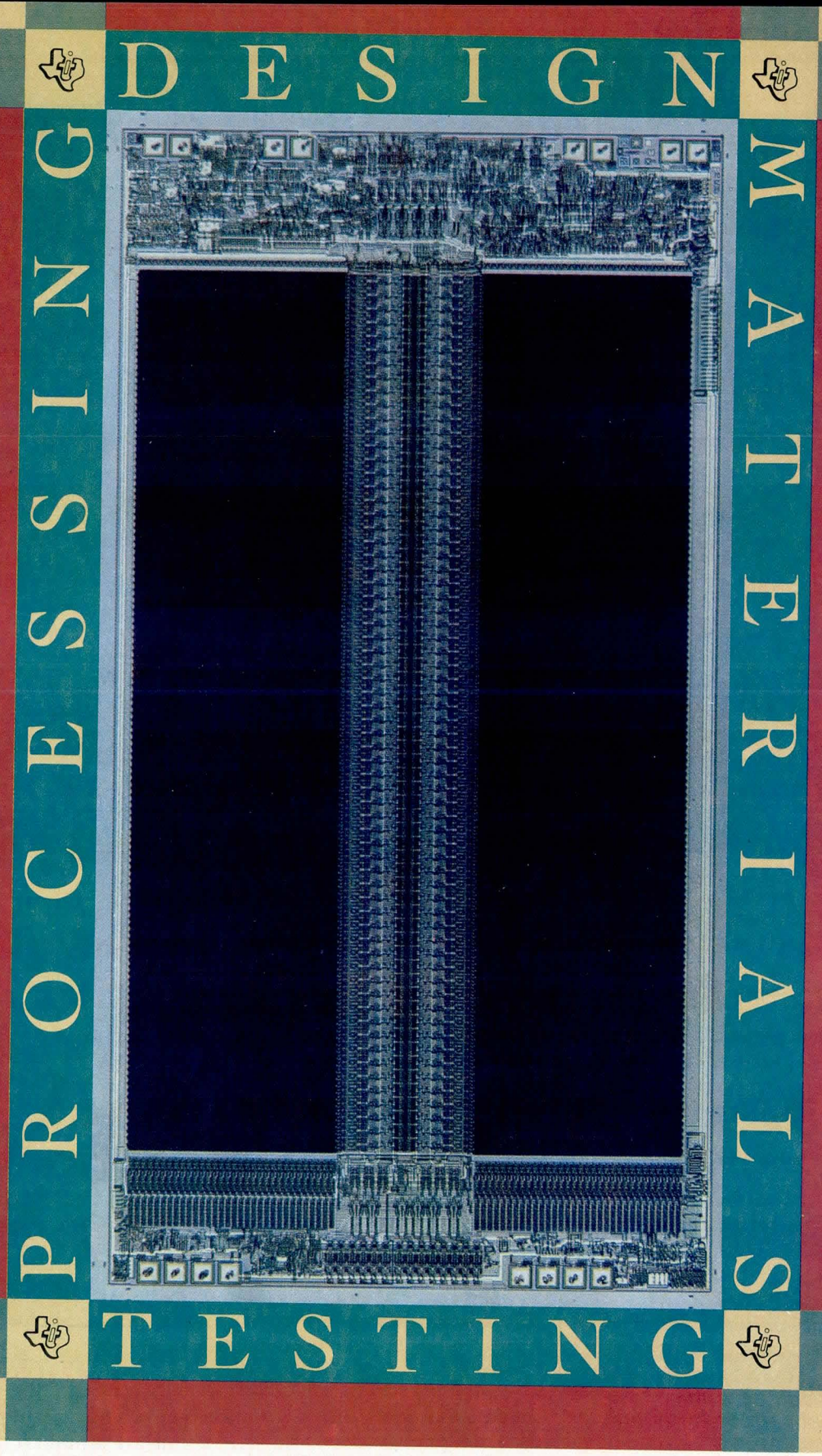

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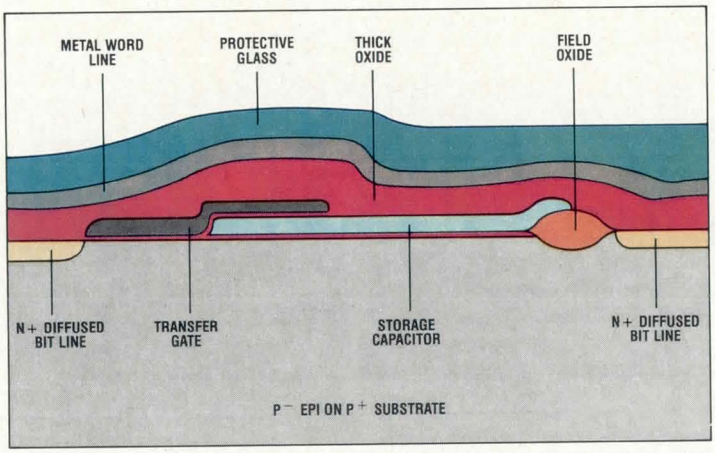

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CIRCLE 63 ON INQUIRY CARD

Envelope Mode Extends Digital Oscilloscope Accuracy and Usefulness

Dual sampling rates and peak detection capabilities give digital storage oscilloscope potential to capture very fast, low repetition rate pulses

Michael Turner
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Tektronix, Incorporated
PO Box 1700, Beaverton, OR 97077

One of the troublesome aspects of digital circuit design is observing fast pulses that occur at relatively low rep rates. Fast and infrequent pulses can reflect a difficulty in the circuit (eg, glitches) or an important aspect of the circuit design (eg, timing pulses). Glitches are difficult to capture because they are sporadic, narrow, and often caused by timing inaccuracies elsewhere in the system. A variable persistence oscilloscope can catch glitches, but only if an observer notices the display before it blooms or fades. A logic analyzer also can capture glitches, but it reveals only when a signal went high or low, and not the actual voltage levels. Moreover, some applications require higher accuracy than that provided by conventional oscilloscopes or logic analyzers. For example, to verify chip select timing in a memory system, the pulses that must be captured may be only 500 ns in duration and as much as 2 ms apart. The 0.5 ms/div sweep rate needed to capture these pulses would digitize the signal only once every 10 μs. Therefore, a digital oscilloscope could miss most of the 500-ns pulses.

Using a multiple sampling technique, the Tektronix 468 Digital Oscilloscope's envelope mode helps to capture fast, low frequency pulses. Envelope mode digitizes at a rate much faster than the memory recording rate and detects maximum and minimum values of a waveform envelope, either continuously or over a selectable number of sweeps. In its normal operating mode, a digital storage oscilloscope samples an input signal at a frequency determined by its TIME/DIV switch setting, storing one data word in memory for every sample taken. In envelope mode, the 468 samples at a much faster rate, but data are still recorded in memory at a rate the TIME/DIV switch specifies. Two words of data stored after every other sampling interval record the minimum and maximum of the many samples taken during the interval.

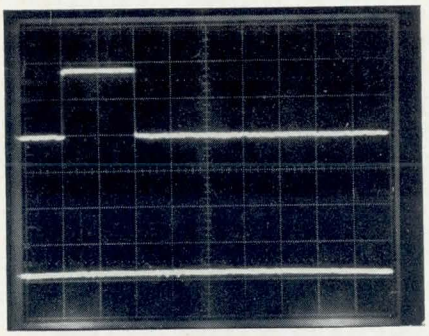
The acquisition system is based on a 25M-sample/s analog to digital converter (ADC). A flash conversion technique using 255 parallel strobed comparators defines the vertical position of the sample on the screen. In envelope mode, the memory rate varies in proportion to the TIME/DIV setting, but the ADC digitizes at a higher rate. Instead of recording just one data word for each sample, two are recorded: the maximum and

minimum of the many samples taken during two intervals. The 1024-word memory can store up to two 512-word waveforms—50 words per display division.

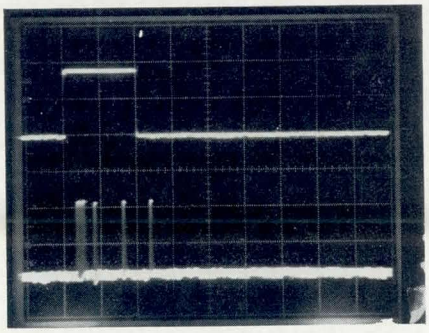
In a typical application, envelope mode helps monitor high speed pulses at low frequencies. Consider a circuit that is enabled by three 500-ns control pulses, all of which must coincide with a 2-ms gate pulse at 100 Hz. If the circuit intermittently fails to operate, one or more of the 500-ns control pulses might occasionally lead or lag the 2-ms gate pulse.

Checking the timing relationship between a 500-ns pulse and a 100-Hz waveform is difficult. A dual channel oscilloscope is needed to display the gate pulse on one channel and the fast control pulses on the other. Since incorrect results occur only intermittently, a storage oscilloscope is needed. Variable persistence storage could be used, but because of the high intensity required to display 500-ns pulses, the base line trace would experience extreme blooming. On the other hand, with digital storage, which can display the pulse without fading or blooming, the oscilloscope would have to sample at least once every 500 ns to guarantee capturing the control pulses. Then, to display both the control pulses and the gate signal, it would need a record length of 10 ms divided by 500 ns, or 20k data words—considerably more than typical equipment offers.

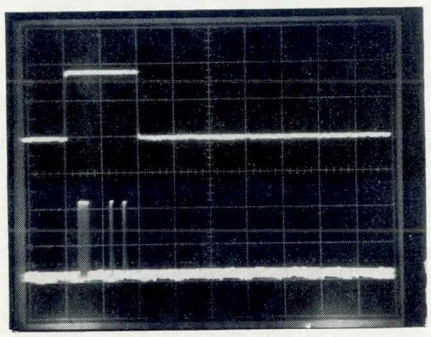
Using envelope mode, a sweep speed of 1 ms/div ensures that the 10-ms gate signal will be displayed. Dividing 1 ms/div by the 468's 50 data words/div gives 20 μs per sample—too slow to capture the 500-ns pulses in normal mode [(a) in the Figure]. But with envelope mode the signal is digitized every 200 ns, and only the maxima and minima occurring within two normal digitizing windows (40 μs in this case) are saved in memory. Multiple sweeps accumulate to record a picture of the waveform envelope over time.



(a)



(b)



(c)

Oscilloscope displays. Problem circuit uses 2-ms gate pulse every 10 ms (top channel) as window for three control pulses (bottom channel) that are all 500 ns wide. In (a), normal mode display that samples slowly enough to capture 100-Hz gate pulse will be too slow to capture 500-ns control pulses. In (b), envelope mode captures 500-ns pulses and shows that one is sometimes late. Problem is solved, in (c), and display shows that pulse timing is now correct

Parts (b) and (c) of the Figure show envelope mode displays that made the problem easy to diagnose. At the top of each screen, the gate signal was stored and displayed using the reference memory. Next, the fast control pulses were captured and their timing was compared with the gate signal timing. As shown in part (b) of the Figure, one of the control pulses sometimes lagged the falling edge of the gate signal, and then the circuit failed to operate.

Envelope mode overcomes several limitations of conventional digital storage oscilloscopes. By sampling at a rate much higher than the display rate, it permits narrow pulses on long pulse trains to be viewed. Also, using multiple sweeps, envelope mode can babysit—watching a circuit to detect an erroneous signal and only then displaying erroneous waveform for comparison with the correct waveform shape.

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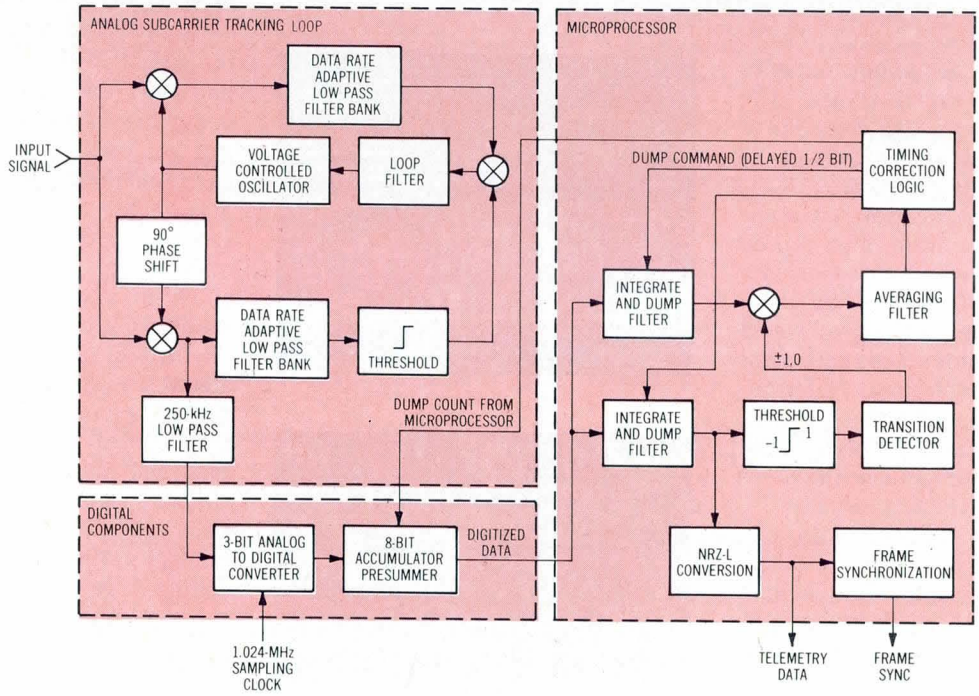
Microprocessor Controlled Data Synchronizer

A versatile receiver processes data at a variety of rates and code formats



Microprocessor accepts digital data from telemetry receiver. Signal loss is less than 1.5 dB for signal to noise levels ranging from 2 to 11 dB at minimum average bit transition density of 12.5% (64 transitions per 512 bit periods). Signal acquisition typically occurs within 2000 bit periods with 90% probability

Telemetry data in a variety of rates and formats are processed by a versatile receiver designed around a custom bit slice microprocessor. A prototype, built for 1.024-MHz communications between the Space Shuttle orbiter and a payload deployed up to 10 mi (16 km) away, handles phase shift keyed (PSK) signals in any of six codes at rates varying between 1 and 16k bits/s. The receiver can be reprogrammed to new rates and formats by changing the programs that control the processor.

As shown in the block diagram, the received signal is filtered and demodulated by analog circuitry, and the demodulated signal is digitized. Among the functions performed by the microprocessor on the digitized signal are bit detection, non-return to zero level (NRZ-L) conversion, frame synchronization (with programmable word length), bit sync acquisition and tracking, error curve normalization, lock detection, half-bit ambiguity resolution, and data rate tracking.

The receiver program, stored in read only memory on the microprocessor chip, is not written in standard assembly language. Instead, a language that is suited to parallel data transfers among the processor registers is used. (Much of the microprocessor operation is handled in parallel, allowing high speed processing at minimum power consumption.) The language is intermediate between a high level language and more conventional assembly languages. The mnemonics also simplify program revisions.

Note

This work was done by Sam W. Houston, Donald R. Martin, and Larry R. Stine of TRW, Inc, for Johnson Space Center.

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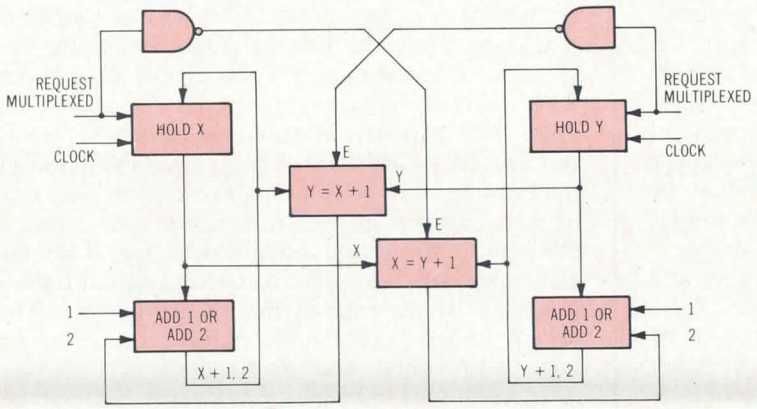
Multipath Star Switch Controller

A function control method is proposed for multiple-computer data processing systems



Star switch controller for two sequencers. Scheme would permit several parallel computers to scan common network stations at maximum rate. "Leapfrog" sequencing would allow bypass of port already being serviced by another computer

A star switch concept can allow a number of parallel computers to scan several common network connected data stations at a maximum rate. "Leapfrog" sequencing bypasses any port already being serviced by another computer. A combination of functional logic techniques increases the number of data paths possible in the system without installation of additional connective hardware.

The output address for each path is contained in individual hold registers. For internal switching of the timing control lines, their control logic is multiplexed so that only one path is being established at any one time. This avoids input port collision between data paths. Positions between address systems are asynchronous, but address systems are otherwise synchronized to the same internal service clock.

The figure shows the function control concept for two sequencers, X and Y. Each sequencer uses a 4-bit hold register and 4-bit adder connected end-around. The second vector connected to the adder during normal operation is a constant 1. When using this sequencer implementation, a "leapfrog" operation is simple. Two binary coincidence circuits are connected, one between X (the output of register X) and Y + 1 (the output from the adder in the end-around circuit) and one between Y and X + 1. The outputs from the coincidence circuits are cross-coupled to the (2^1) terms of the second vectors in each adder. When the (2^1) term is turned on, the (2^0) is turned off.

One sequencer leapfrogs only when the other sequencer is a step ahead and quiescent. All connections are cross-coupled so that whenever one of the two sequencers is ahead one step, the other sequencer will leapfrog. Since they are halted randomly, which of the two sequencers is ahead may alternate.

In a 3-sequencer system, any 2 out of 3 sequencers are first cross-coupled in the manner described for the 2-sequencer system. In addition, any two sequencers halted at adjacent positions must be detected. When this occurs and the third sequencer is also adjacent and operating, both the (2^0) and (2^1) terms of the adder's fixed vector are energized so that the adder will advance three positions—ie, leapfrog the two adjacent quiescent sequencers.

A 2-path system is only slightly more complex than a single-path system. Thus, a 2-path system for a 16-port star switch controller would be cost effective if added bandwidth or increased reliability were required. A multiple-path system, however, becomes more complex exponentially. The 3-path system is manageable, but may not be cost effective for a 16-port system. The design probably would be cost effective for a 32-port system, however.

Note

This work was done by Tage O. Anderson of Caltech for NASA's Jet Propulsion Laboratory.

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Interfacing Fundamentals: Double-Buffered Conditional I/O

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Virginia Polytechnic Institute and State University
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Previous columns in this series discussed the distinctions among various types of I/O techniques—input, output, unconditional, conditional, unidirectional, and bidirectional—as well as the basic difference between a flag and a semaphore. This and several subsequent columns will explore an additional concept, double-buffered conditional I/O, that facilitates the discussion of other I/O techniques known as the 2-wire and 3-wire handshake. Attention will be focused on a pair of 8-bit microcomputers: a master and a slave.

A *buffer*, in the context of data processing and computation, is "a device used to compensate for a difference in rate of flow of information or time of occurrence of events when transmitting information from one device to another."[1] The word "storage" is omitted from the original definition, thus permitting the inclusion of latches, which are storage devices, and 3-state buffers, which are not.

In double-buffered conditional I/O, which is so common that the existence of double buffering is rarely given special attention, there are two buffers in series in the data path between the data buses of the master and slave microcomputers. Typically, one of these buffers is associated with the master, and the other with the slave. One buffer is an output port (latch); the other is an input port (3-state buffer). The two buffers compensate for a difference in the time at which data transfer steps occur when data are transmitted between the master and the slave.

Examples of double-buffered conditional I/O were given in two previous columns.[2,3] In reference 2, a 74LS373 buffer/latch integrated circuit was used as the buffer between source and acceptor microcomputers; data flow was unidirectional. The 74LS373 contained an 8-bit latch, the output buffer for the source, and an 8-bit 3-state buffer, the input buffer for the acceptor. The source microcomputer clocked the latch, and the acceptor microcomputer enabled the 3-state buffer.

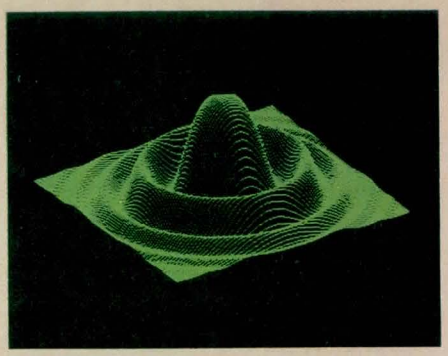
The bidirectional double-buffered characteristics of port A (mode 2) on the 8255 programmable peripheral interface chip in reference 3 are worth emphasizing. When the master outputs data to the slave, the output instruction OUT 80H clocks data into the 8-bit latch associated with port A. An acknowledge pulse, $\overline{ACK}_A$, from the slave enables the 3-state buffers associated with port A and permits data to be input into the slave. When the slave outputs data to the master, the two buffers in series are reversed. An $\overline{STB}_A$ pulse from the slave clocks the 8-bit latch associated with input port A, and the master input instruction IN 80H enables the 3-state buffers. Thus, port A (mode 2) on the 8255 chip contains four buffers: two for input and two for output.

The utility of the concept of double-buffered conditional I/O becomes evident when two microcomputers are interfaced together via a pair of programmable I/O ports such as those found on peripheral interface chips (6520, 6821, 8255) or on "combo" chips that provide various combinations of CPU, I/O, RAM, ROM, and timer functions (6530, 6532, 6534, 6801, 6803, 6805, 8048, 8155, 8741, 8755). Each of these chips has one or more unconditional or conditional I/O ports. The

(continued on page 124)

Characteristics of Programmable I/O Ports

Type of I/O Technique	Directional Characteristics	Number and Type of Buffers		Minimum Number of Flags or Semaphores
		Latches	3-State Buffers	
Unconditional input	Unidirectional	0	1	0
Unconditional output	Unidirectional	1	0	0
Conditional input	Unidirectional	1	1	1
Conditional output	Unidirectional	1	1	1
Conditional I/O	Bidirectional	2	2	2



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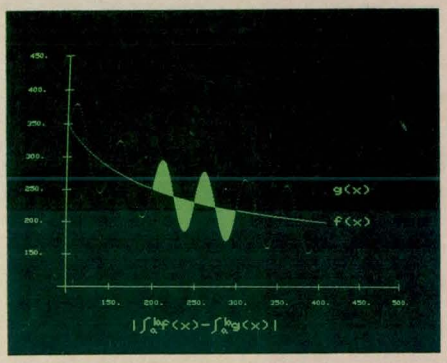

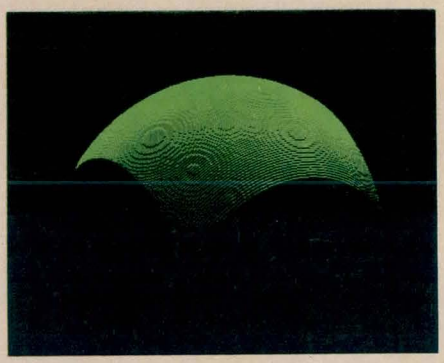

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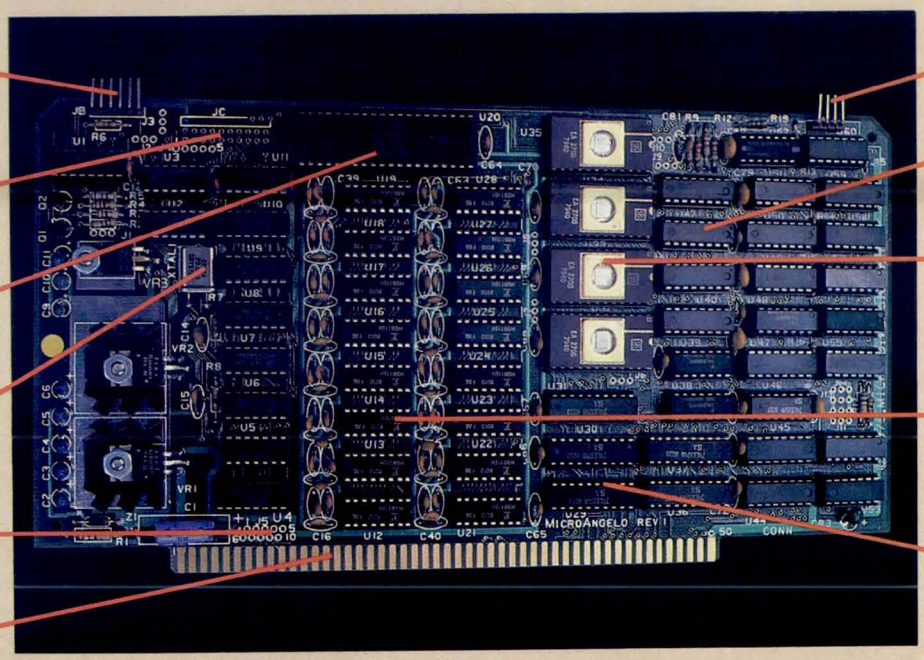

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use of the conditional I/O ports for microcomputer-microcomputer interfacing may be straightforward, but how are two microcomputers interfaced to each other when only unconditional ports exist?

The Table, which summarizes some of the characteristics of programmable I/O ports, provides some answers. With an unconditional port, only a single buffer—either a latch or a 3-state buffer— is present. Unconditional ports have neither a flag nor a semaphore directly associated with the port so that one or the other must be created from unconditional I/O bits available on other ports. To create a unidirectional conditional I/O port, there must be at least two buffers—one latch and one 3-state buffer—and at least one flag or semaphore. The creation of a bidirectional I/O port requires two latches, two buffers, and at least two flags or semaphores.

Fig 1 demonstrates a simple approach to the interfacing of two microcomputers using only unconditional I/O ports and bits. The master buffer is an 8-bit latch that is clocked by the $\overline{WR\ X}$ pulse from the master computer. The slave buffer is a 3-state buffer that is enabled by an $\overline{RD\ X}$ pulse from the slave computer. Communication between the master and slave buffers is continuous and is accomplished by a set of eight wire connections.

The interesting aspect of Fig 1 is the way in which the DAV (Data AVailable) and NDAC (Not Data ACcepted) flags are used to accomplish the conditional I/O. Observe that two flags are required, in contrast to the single semaphore shown in a previous article.[2] DAV is a single output bit on an unconditional output port located on the master buffer. NDAC is a single output bit located on the slave buffer. As shown in Fig 1, the master computer sets and resets the DAV flag, and the slave computer does the same with the NDAC flag. Since they communicate only with a single computer, they are clearly flags and not semaphores.

With two flags, there must be a total of four different logic conditions: two for DAV and two for NDAC. These conditions are summarized in Fig 2, which provides timing diagrams for the data transfer process between master and slave. The initial conditions—data not available from master and not accepted by slave—are chosen such that DAV is initially logic 1 and NDAC is initially logic 0. Data are first output to the master buffer (latch) by the master computer and given a short time to settle. As indicated by the timing diagrams, DAV is then reset, indicating that data are available from the master. The slave computer inputs the DAV flag bit, tests it, detects the logic 0 state, and inputs data from the slave buffer (3-state buffer). Once the data are input and stored, the slave sets the NDAC flag, thus indicating that data have been accepted. The master computer inputs the NDAC flag, tests it, and determines that data have been accepted. The DAV flag is then set once again, indicating that data are no longer available from the master. The slave computer inputs the DAV flag, tests it, detects the logic 1 condition, and consequently resets the NDAC flag in preparation for the next handshaking transaction.

The 2-flag handshaking process shown in Fig 2 is different from the use of a single semaphore.[2] Fig 3 depicts the difference, in the form of timing diagrams, for the same data transfer process shown in Fig 2, With a semaphore, only a single flipflop is present so that only two different logic conditions exist. When the master computer outputs data to the master buffer, the semaphore is set, indicating that data are available. The slave computer inputs the

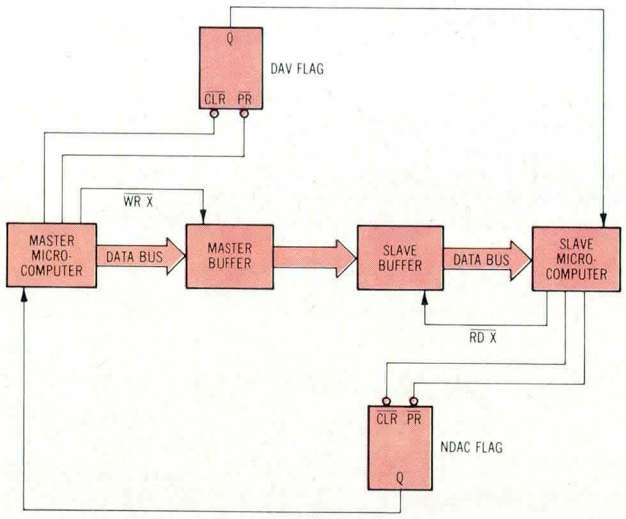

Fig 1 Double-buffered conditional output with two flags. Data available (DAV) flag informs slave when data are available from master. Not data accepted (NDAC) flag informs master when data have been accepted by slave

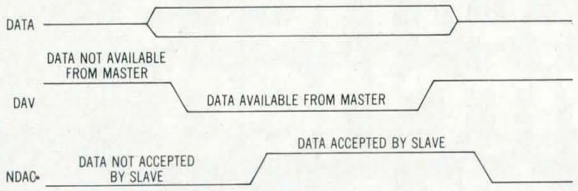

Fig 2 Timing diagrams for double-buffered conditional output with two flags. With two flags, there must be four different logic states: two for DAV flag and two for NDAC flag

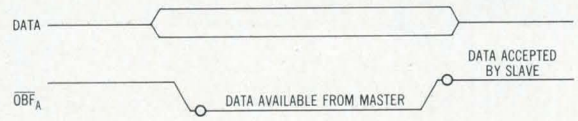

Fig 3 Timing diagrams for double-buffered conditional output with semaphore. With single flag, there are only two different logic states, "data available from master" and "data accepted by slave." $\overline{OBF}_A$ refers to output buffer full semaphore associated with port A on 8255 chip[3]

semaphore bit, tests it, detects the logic 0 state, inputs the data from the slave buffer, and, finally, sets the semaphore. The master computer inputs the semaphore bit, tests it, ultimately detects the logic 1 condition, and concludes that the data byte has been accepted by the slave. From a conceptual point of view, the use of a single semaphore is a simpler type of handshake than the 2-flag handshake shown in Figs 1 and 2.

References

1. *IEEE Standard Dictionary of Electrical and Electronics Terms,* John Wiley & Sons, Inc, New York, NY, 1972, p 64
2. P. R. Rony, "Interfacing Fundamentals: Conditional I/O Using Two Microcomputers," *Computer Design*, Aug 1980, pp 136-138
3. P. R. Rony, "Interfacing Fundamentals: Bidirectional I/O Using Two Semaphores," *Computer Design,* Apr 1981, pp 184-188

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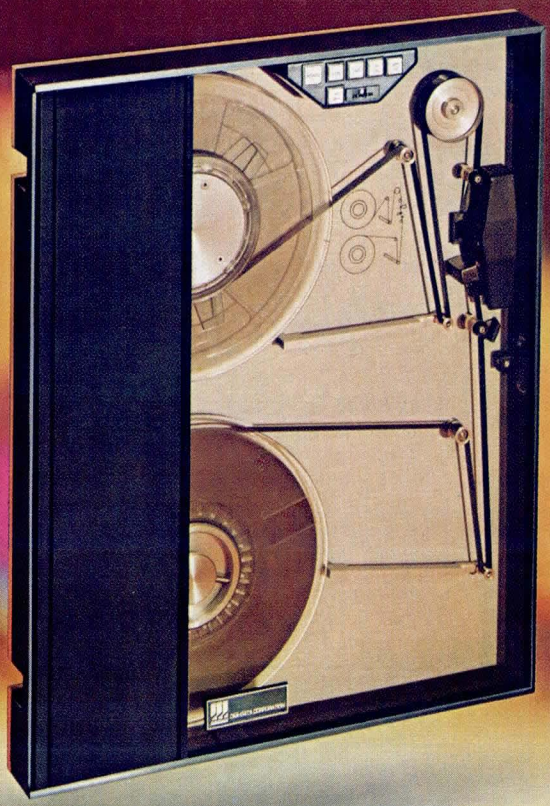
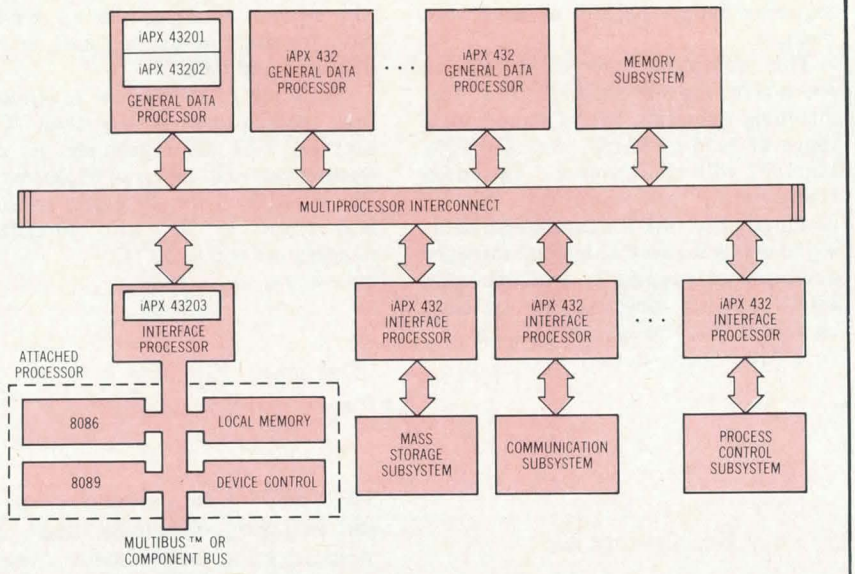


*LSI-11, PDP-11, Nova Eclipse, and HP 2100/21MX.

3-Chip 32-Bit Microprocessor Offers Computing Capability of Mid-Size Mainframe



Micromainframe architecture. Intel Corp's iAPX 432 32-bit microprocessor is implemented in 3-chip set composed of iAPX 43201 instruction decode chip, iAPX 43202 micro-execution chip, and iAPX 43203 interface processor chip. Architecture reduces software development and debug time and expense

A 32-bit microprocessor, iAPX 432 increases programmmer productivity through support of high level language concepts and object oriented programming, and offers capabilities extending from those of a mid-range minicomputer to those of a mid-range mainframe. The micromainframe's architecture, which Intel Corp, Special Systems Operation, 3585 SW 198th Ave, Aloha, OR 97005, has based on modular programs and data structures, reduces software development and debug time and expense, and includes hardware and software facilities for the design of fault tolerant systems.

System hardware recognizes and operates directly on objects, a higher level of data type than that manipulated by conventional computers. Together with modular programming discipline, objects form the basis of a programming methodology that allows large software applications to be broken down into smaller pieces. The pieces are then developed in parallel by programmers and are guaranteed to fit together when integrated into a total system.

The system is split into functionally specialized data processors and I/O subsystems that can be individually replicated in a software transparent fashion. Computing power is a function of the number of data processors in the system, and I/O capability can be increased by adding or configuring I/O subsystems. The multiple processor coordination facilities are built into the hardware, reducing configuration constraints and simplifying software requirements. Software transparent multiprocessing is expected to allow the design of systems having a one to ten times performance range.

In addition to 32-bit data words, the chip set operates on 32-, 64-, and 80-bit wide floating point values, and Boolean and character data types. The processor's instruction set supports from zero to three operand specifiers per instruction. It features symmetric operand addressing modes for scalar, vector, and recording elements, increasing high level language efficiency and eliminating the need for assembly language programming. Ada is the micromainframe's system programming language.

The processor is implemented in a 3-chip set; each chip is manufactured using a HMOS process and packaged in a 64-pin quad inline package carrier. The iAPX 43201 instruction decode chip and the iAPX 43202 micro-execution chip comprise the 32-bit general data processor (GDP). The chips act as a pipelined pair, one fetching and decoding instructions, the other executing them. The GDP supports a logical address space of more than 4G bytes and governs a 1T-byte virtual memory addressing space.

Single instructions replace entire operating system subroutines for storage allocation and interprogram communications; any data structure can be transmitted between programs with "send" and "receive" instructions. Buffering and synchronization are performed automatically by the hardware. The self-dispatching GDPs schedule and dispatch programs without software intervention; as more processors are added, the workload is automatically shared among them. To maintain flexibility, applications-specific policies that determine the type of scheduling to be used remain software parameters.

Communication with I/O devices is handled by the iAPX 43203 interface processor chip. It permits a satellite subsystem to act as an attached processor, independently handling all I/O activity. System I/O capability can be expanded by adding more such attached processor subsystems, or by reconfiguring an existing one. A single system can grow from a few CRT terminals, printers, and mass storage subsystems, to a much larger system, in a fully compatible manner. The interface processor also provides protected address windows between the attached processor and system memories, and a DMA-like buffering function to lower the micromainframe's memory access overhead.

Hardware failures can be detected by wiring any two identical 432 processors together into a self-checking configuration. This functional redundancy checking (FRC) pinpoints processor failure and confines it to a small portion of the system. Advanced data protection is provided by a "capability based" memory protection facility that immediately detects software errors and confines them to a specific program. FRC, together with advanced data protection, provides a basic element for the design of fault tolerant and "always available" computer based systems.

iAPX 432 will first be used in the Intellec 432/100, an iSBC compatible board level evaluation system designed to operate in conjunction with an Intellec development system. This system includes iSBC 432/100 board, object builder evaluation software, and introductory texts and references.

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16-Bit μComputer Is Suited for Severe Environment Applications

SECS 86/05 dual-board, ruggedized, 16-bit microcomputer from EMM Sesco, 20630 Plummer St, Chatsworth, CA 91311, consists of two 6 x 9″ (15 x 23-cm) ATR compatible boards connected by a Localbus interface. One board contains the processor and associated functions; the second contains the system's memory components. Both a Localbus interface, for communicating with local memory, and a Multibus system bus, for referencing additional memory and I/O devices, are included. The system is supported by the company's Real Time Multitasking Executive, for use in realtime militarized and severe industrial applications.

Standard features include an Intel iAPX 86/10 microprocessor with 5-MHz clock, three programmable 16-bit interval timers, 24 parallel I/O lines, a serial I/O port with programmable baud rates, and nine levels of vectored interrupt control, expandable to 65 levels. The system supports multimaster configurations with other of the company's 16-bit as well as 8-bit microcomputers. Full Multibus arbitration control logic allows up to three bus masters to share the Multibus system bus in a serial daisy chain fashion. With the addition of an external parallel decoder, the number of masters can be expanded to 16.

The system's memory module contains 16 sockets accommodating any mixture of EPROMs and byte-wide pseudo-static RAMs; total capacity is 64k bytes using Intel 2764 EPROMs or 32k bytes using 2k x 8-byte RAMs. The memory card interfaces to the computer via either the Multibus or Localbus; system memory expands to 1M byte with the Multibus, or 256k bytes with the Localbus, using additional Multibus or Localbus compatible memories. Addition of the TC-1 tape controller and SETS-1 tape system further enlarges mass storage capability.

Central processor architecture includes byte-addressable, memory-base pointer and index registers. The optional 8087 numeric data processor extends the processor's architecture and instruction set with over 60 numeric instructions, and supports math data types including 16-, 32-, and 64-bit integer; 32- and 64-bit floating point; 18-digit packed BCD, and 80-bit temporary.

Control logic is provided to accept a power-fail interrpt in conjunction with an ac-low signal, and to initiate an orderly system shutdown in the event of power failure. Read/write access to RAM is disabled during system power-down, and an auxiliary power bus allows separate power flow to RAM in systems requiring battery backup of read/write memory.

The computer meets MIL-E-5400, MIL-E-16400, and MIL-E-4158 specifications, including operation over a temperature range of −55 to 85 °C, and 0 to 95% humidity with condensation. All system components are mounted on an aluminum heatsink for conduction cooling to the card edges. Complete software development support is available with Intel's Intellec development systems, languages, and debugging facilities.

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655k-Byte Magnetic Bubble Memory System Is S-100 Bus Compatible

Bubbl-Machine, an S-100 bus compatible magnetic bubble memory system, provides up to 655k bytes of nonvolatile mass storage as an alternative to floppy or hard disc drives. The bubble memory system features small size, silent operation, long life, low power consumption, and fast operation, and is available from Bubbl-Tec, Div of PC/M, Inc, 6800 Sierra Ct, Dublin, CA 94566.

The system consists of one MBC-100 Bubbl-Board printed circuit controller module and from 1 to 16 MBB-100 Bubbl-Pac memory modules. The controller module connects to the memory modules via a daisychain, 26-conductor ribbon cable, or the memory modules can be housed in an external chassis and connected to the controller via a single 26-conductor cable. All modules have standard S-100 dimensions and plug directly into any S-100 system.

Providing the interface between CPU bus and memory modules, the Z80 based intelligent controller module performs essentially the same functions as a disc controller. It contains an 8-bit microprocessor and controls up to 16 memory modules for a total of 655k bytes of nonvolatile storage in 40k-byte increments. The controller module provides direct memory access to the host computer's RAM/ROM memory system and is fully compatible with the CP/M operating system. The microprocessor handles bubble device formatting and error checking and control.

Each memory module contains four Texas Instruments TIB0203 92k-bit magnetic bubble memory devices operating in parallel, for a total of 40k bytes of storage, equivalent after formatting to approximately 320 floppy disc sectors. Modules can be removed from the computer, or replaced, without loss of stored data.

Operation of the system is extremely fast: access time is less than 4 ms average, 7.27 ms maximum. Its data transfer rate is in excess of 88,000 bits/s. Power required for the entire system is less than 25 W, and operating temperature is 0 to 50 °C.

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μComputers Operate in Single or Multiprocessor Environments

Single-board 8-bit computers, PCU-6809 and PCU-68009, operate in single- and multiprocessor environments, respectively, and are designed for processing and control applications. The 6809 microprocessor based computers, available from Phoenix Digital Corp, 3027 N 33rd Dr, Phoenix, AZ 85017, can be used in standalone configuration or in the user's environment.

Both modules provide a CPU realtime clock and 4-yr calendar, power-on restart, system clock and timing, two parallel programmable I/O ports, a serial RS-232-C communications port, three 16-bit programmable timers, drivers and receivers for system expansion, moniter/debugger firmware, provisions for ROM/EPROM mounting, and the ability to work with slow memory. The multiprocessor version can interface with the NCM-6809 network control module operating on the same bus.

Available in 1- or 2-MHz versions, the board's 6809 microprocessor provides 59 instruction mnemonics in 10 addressing modes, 9 internal registers and accumulators, maskable and nonmaskable vectored interrupts, and vectored restart. Operating simultaneously with an NCM-6809 network subsystem on the same bus, two microprocessors can share a common bus by operating 180° out of phase with one another.

The onboard CMOS clock and calendar circuit incorporates an addressable

(continued on page 130)

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counter, an addressable latch for alarm-type functions, and two interrupt outputs. The realtime clock measures from thousandths of a second through months, and the calendar circuit functions as a 4-yr calendar.

Eight memory sockets, two on the private bus and six on the public bus, are capable of mounting up to 16k bytes of RAM, 64k bytes of ROM/EPROM, or a mixture of both. The private bus can be accessed only by the onboard microprocessor, while the public bus can be accessed by any microprocessor on the system bus. Slow external memories are handled by stretching the clock pulse.

Also included on the boards is the 6840 programmable timer module (PTM) with three 16-bit programmable timer/counters that can be connected to the external world through onboard jumpers. Two programmable I/O ports are incorporated via a 68B21 PIA; each port has eight independently programmable parallel I/O lines, one programmable input interrupt line, and one line that can be programmed to function as an interrupt input line or as a central output line. The RS-232 communications port, based on a 6850 ACIA, can be programmed to transfer seven or eight data bits; odd, even, or no parity; one or two stop bits; and -1, -4, or -16 clock mode.

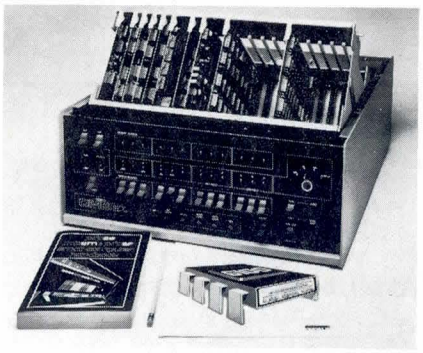
The board's system memory and I/O can be expanded through the addition of optional memory, I/O, and peripheral controller modules. Through their 3-state bus drivers and receivers, the boards are bus compatible with EXORciser bus compatible and R65 definition compatible boards. The commercial version has on operating temperature range of 0 to 70° °C, while the industrial version's range is -40 to 75 °C. The boards measure 9.75 x 6″ (24.76 x 15 cm), and weigh 0.75 lb (0.34 kg).

Circle 464 on Inquiry Card

μComputer System Runs PDP-8 Series Software Without Modification

Complete software compatibility with Digital Equipment Corp's entire PDP-8 family and VT-78 DECstation equipment is offered by the PCM-12 Omega microcomputer system from Pacific Cyber/Metrix, Inc, 6800 Sierra Ct, Dublin, CA 94566. The system employs a binary instruction set identical to that in the PDP-8/E and /A, allowing all DEC and user written software to be run without modification.

Features of the system include fully developed software, 12-bit word length, direct memory access, 5-μs fetch and execute time, and up to 65k memory words. Available in rackmount or tabletop configurations, the system provides a tilt-up card cage with 18-card capacity; heavy duty linear power supply; and a full function front panel with built-in, pushbutton activated bootstraps for RX01 and RX02 floppy discs, RK05 hard discs, TU-58 DECtape, and paper tape. A software type front panel without hardware switches is also available.



Microcomputer system. Pacific Cyber/Metrix's PCM-12 Omega runs DEC PDP-8 software without modification, and provides tilt-up card cage with 18-card capacity, heavy duty power supply, and full function front panel

Serving as the basis of the system is the 12510 CPU module. The double-sided, plated-through board contains the 6100 microprocessor, crystal controlled 4-MHz system clock, crystal controlled baud rate generator, interrupt-vector control logic, memory multi-plex logic, and all the line driver and interface logic necessary to define the system's 3-state, TTL level bus structure.

The system offers up to 32k words of main memory, plus 32k words of control panel memory. The basic main memory element for the system is the 12020 static memory module that employs 48 low power, 2102 family, 1k-byte static RAMs to provide 4k 12-bit words of memory. All the necessary logic to extend main memory to 32k words, a 256-word hardware push/pop stack, and a programmable realtime clock that generates interrupts at intervals from 10 μs to 40 s are contained in the 12540 memory extender module. Under control of the 12120 control panel memory expansion module, the 12020 static memory module can expand control panel memory space to 32k words, providing a total system memory of 65k words.

A complete line of plug-in option modules is also available, including seven memory options, four serial I/O modules, four parallel I/O modules, floppy and hard disc controller, paper tape and audio cassette interfaces, two printer interfaces, A-D and D-A converters, and a positive bus converter for PDP-8/I and /L peripherals. The ZODT monitor/debugger, a P/ROM resident ODT-like monitor, uses no main memory space, and provides a full complement of monitor and debugging functions to aid in initial testing of user software and to monitor system operation.

Circle 465 on Inquiry Card

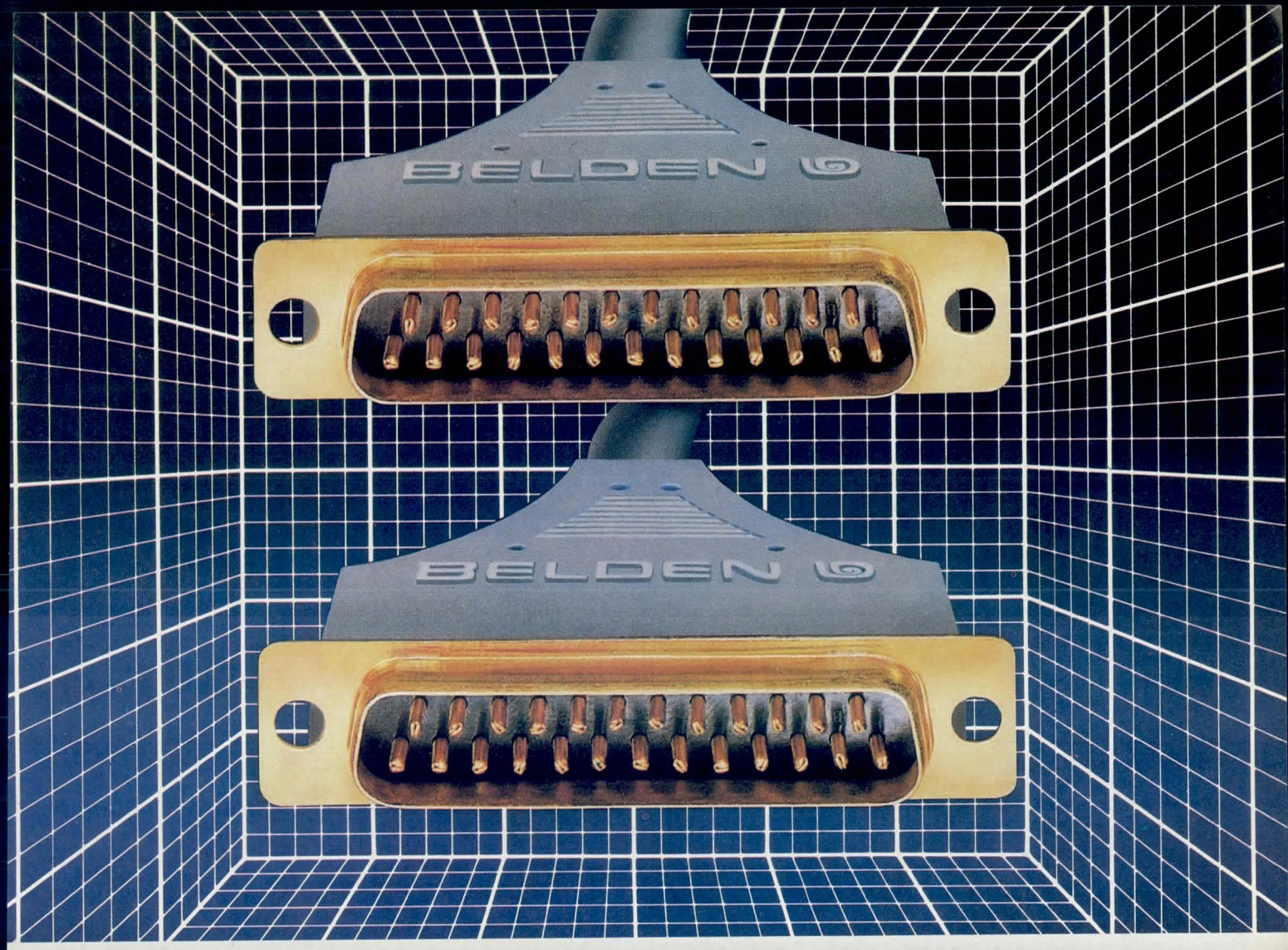
Breadboard System Eases Prototype and Custom Circuit Board Development

An expanded Scotchflex breadboard system, offered by 3M, Electronic Products Div, PO Box 33600, St Paul, MN 55133, facilitates the development of prototype or custom printed circuit boards, using the "U contact" system of solderless connections. The system provides the flexibility of accommodating several standard microprocessor boards plus the ability to tailor plugs and connectors to handle sockets sized from 8 to 40 conductors.

Plug and solder strips are supplied in 24-contact sizes; however, they are designed so that any number of contacts can be snapped off to suit a specific need. To maximize board density, the modular strips can be stacked end to end or side by side to fit the hole pattern in the printed circuit board.

Standard kits provide 24 24-contact plug strips, 16 24-contact solder strips, dual sockets ranging from 16- to 40-pin sizes, and a universal breadboarding tool. Optional kits add either an SBC-8010, S-100, Motorola M-6800, or Zilog Z80 equivalent microprocessor board, and a self-feeding wiring tool. Using the wiring tool, two wires can be inserted in any one "U contact."

Circle 466 on Inquiry Card



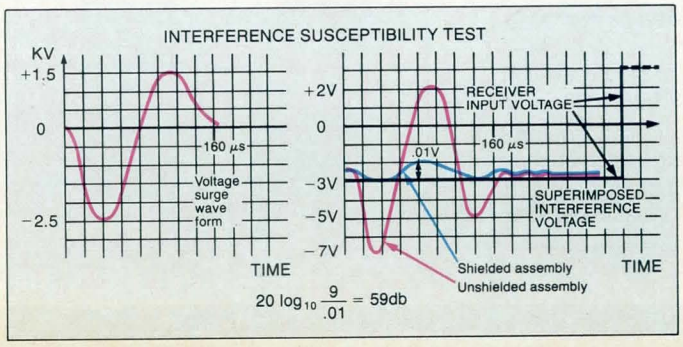
One of these cable assemblies can cut your interference levels 59 db.

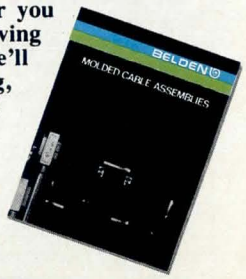
Both meet RS-232-C specifications. Both are made by Belden using rugged materials and proven designs.

But one is shielded. One is not. And that can make a big difference in critical data communications applications.

Although RS-232-C standards do not specifically call for shielded interconnect devices, our research indicates that cable *and* connector shielding is required to insure the signal integrity of the assembly. In fact, transfer impedance, leakage current power spectrum, electrostatic discharge and interference susceptibility tests at Belden all demonstrate the value of Belden totally shielded connector-cable assemblies over nonshielded assemblies.

With a complete line of rugged and highly reliable standard molded connector designs including GPIB, and complete custom design capabilities, we can make exactly what you need, when you need it. And show you ways to increase performance without increasing costs. Whenever you have a shielding need or a question involving interconnect devices, contact Belden. We'll share our experience. For a free catalog, write Belden Corporation, Interconnect Systems Operation, 105 Wolfpack Rd., Gastonia, NC 28052. Phone: (704) 865-4513.





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CIRCLE 69 ON INQUIRY CARD

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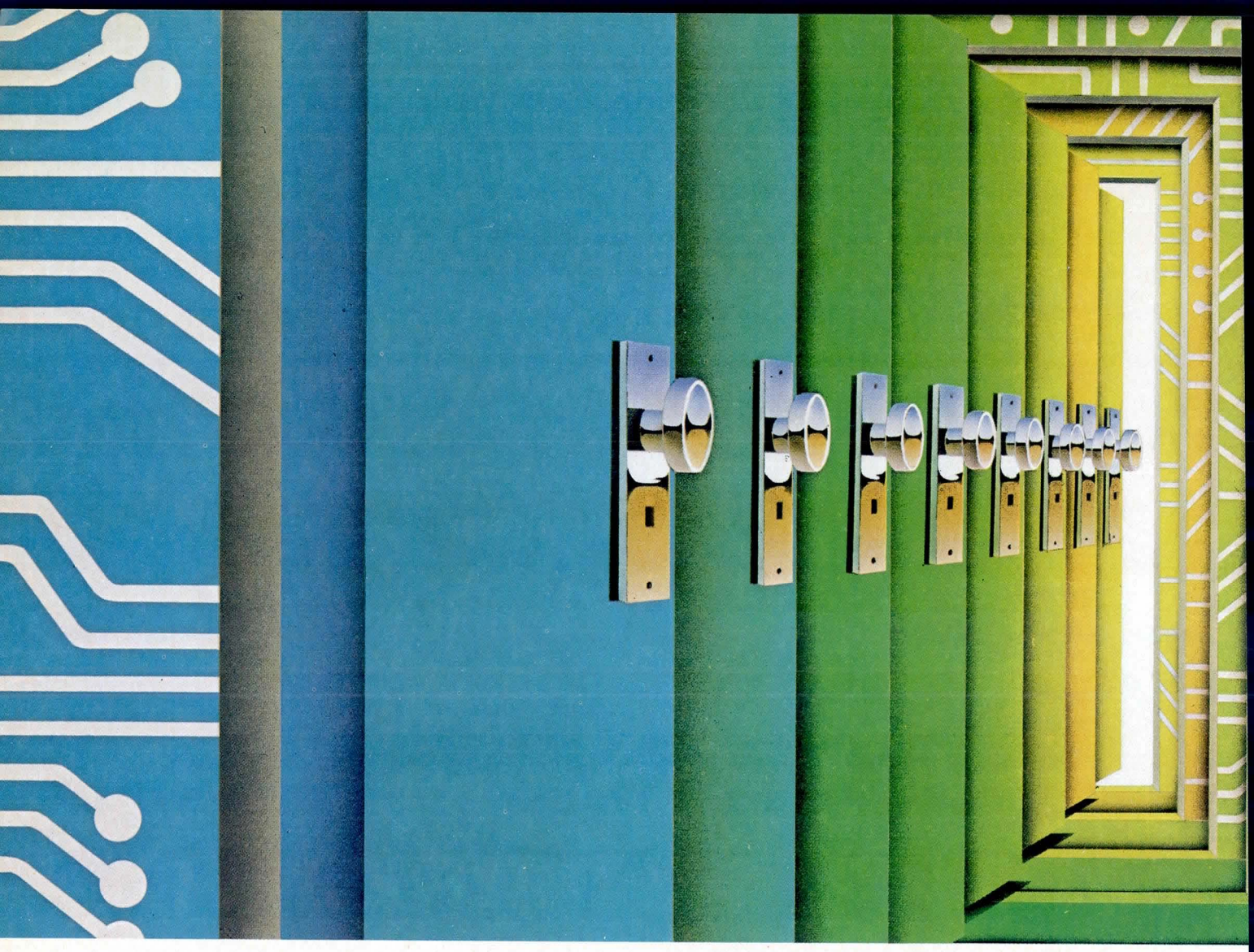


Intel's new E²PROM. We window, to open endless

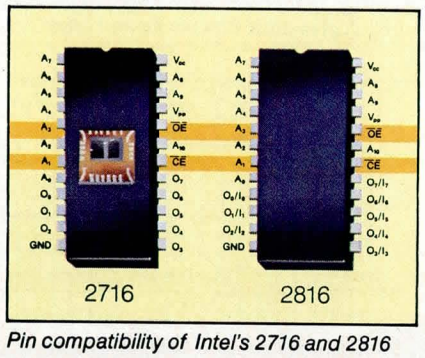
Intel introduces the 2816: the in-circuit Electrically Erasable 16K E²PROM that's both byte- and chip-erasable. Available in quantity today.

For years, system flexibility has been limited by both ROMs and EPROMs. But no more. Now, Intel's 2816 E²PROM combines in-circuit alterability and non-volatility, providing functionality that will advance today's high-performance microprocessor designs. This makes the 2816 a natural to replace conventional ROMs and EPROMs as the standard storage medium for programs. And opens the doors to a whole new generation of non-volatile memory applications.

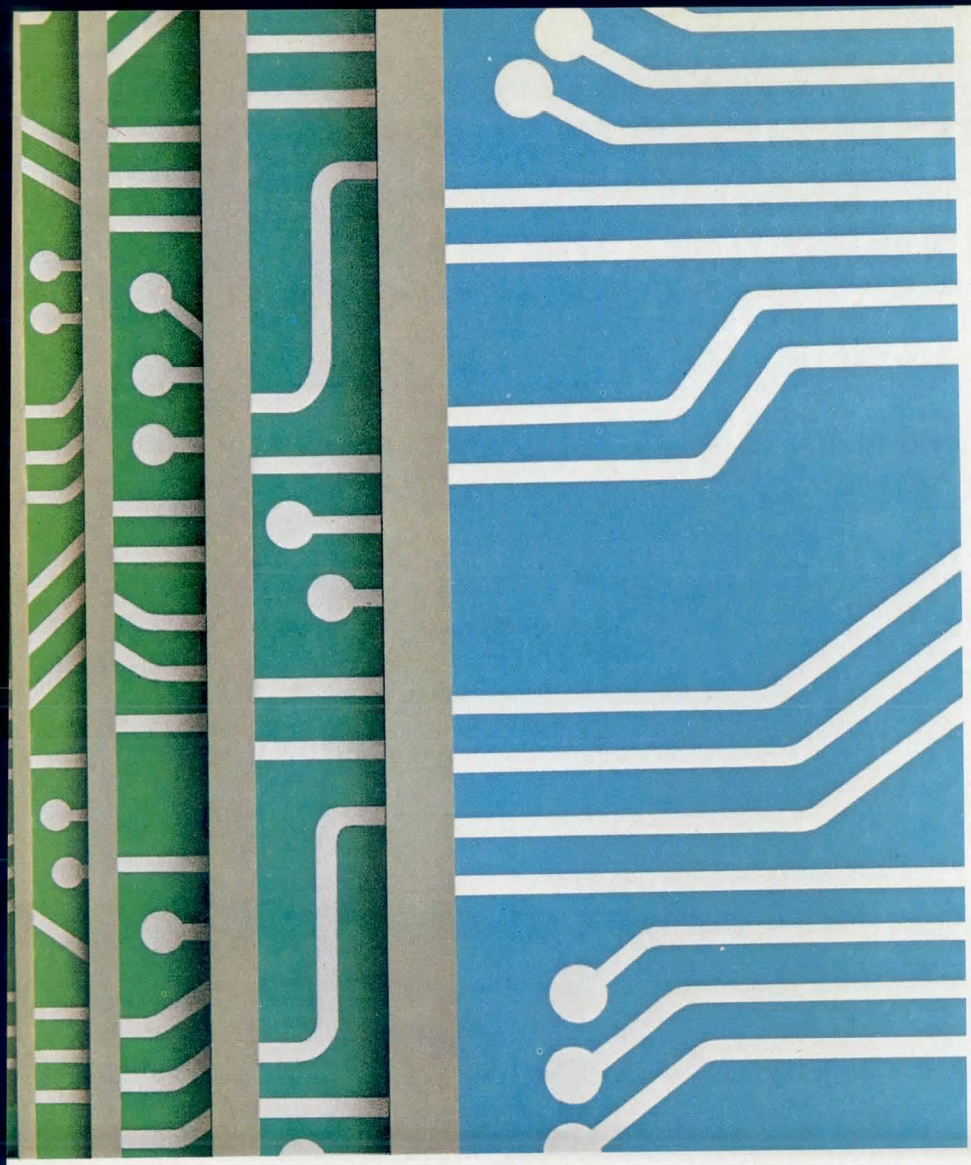
For systems smart enough to learn from experience

The 2816 E²PROM will revolutionize microprocessor system design. Now systems can be dynamically reconfigured—without human intervention. Consider the possibilities.

In industrial process control, equipment can be self-calibrating; machine tools, self-adjusting. In military and commercial aircraft, flight coordinates or radio frequencies can be changed remotely. In retail stores, point-of-sale terminals can have pricing tables updated instantly. In harsh industrial and manufacturing environments, programmable robots can make use of self-diagnosing/self-correcting feedback loops. The



Pin compatibility of Intel's 2716 and 2816



closed the design doors.

potential for convenient, low-cost system reconfiguration is enormous, for both OEM and end-user alike.

An exponential increase in design options

What are the E^2 advantages to designers? First, reprogramming flexibility. The 2816 can be reprogrammed electrically in the field, without interrupting in-service equipment operation. Or it can be reprogrammed remotely, via telecom or datacom links. Thus saving the labor and system downtime costs usually incurred with changing code in the field.

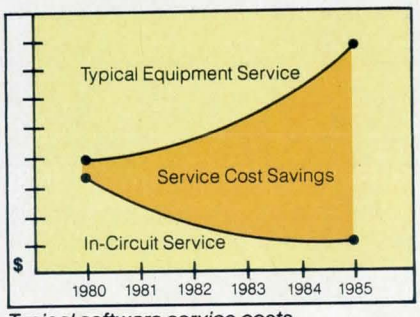
Second, the 2816 is both byte- and chip-erasable. Each byte can be rewritten up to 10,000 times, leading to simpler, more flexible systems. And reprogramming is fast: a single-byte program edit takes only 20 ms.

Third, the 2816 has the same reliability and data integrity as all non-volatile Intel memories. This reliability is a result of the 2816's floating-gate tunnel oxide (Flotox) cell structure and ten years of Intel experience in EPROM manufacturing. And unlike some other non-volatile ROMs, the 2816 does not require data rewrite to insure integrity. It will retain its data for at least 20 years—regardless of read frequency—without refreshing. And this kind of reliability—coupled with improved performance—will make the 2816 the industry standard for all program memories.

A match for today's micros

The 2816 is pin-compatible with the Intel® 2716. So it gives you all the microprocessor-oriented features that have made the 2716 the industry standard among EPROMs.

The 2816 also has the industry's fastest standard access time: 250 ns. And its two-line control eliminates bus contention between address and data lines. Plus it's low power. Thus changing existing concepts of memory storage and enabling designers to take full advantage of powerful new microprocessor capabilities, like those of the 8088 and 8086.



Typical software service costs

Remote reconfigurability in the here and now

Although the 2816 offers revolutionary capabilities, it's also the practical choice for microprocessor designs in the here and now. It's manufactured by Intel's proven HMOS*-E process. So you know it will follow the classical learning curve of a mainstream semiconductor technology.

To help you get started designing-in 2816s today, Intel provides full applications support and documentation. For instrumentation and control applications, we've already incorporated the E^2PROM on an iSBC 88/40™ single-board computer.

We've closed the window; now you can open totally new design doors, and watch the world beat a path to your products. The 2816 E^2PROM is available from stock through your local Intel distributor or Intel sales office. Or for further information, contact Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

*HMOS is a patented Intel process.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.

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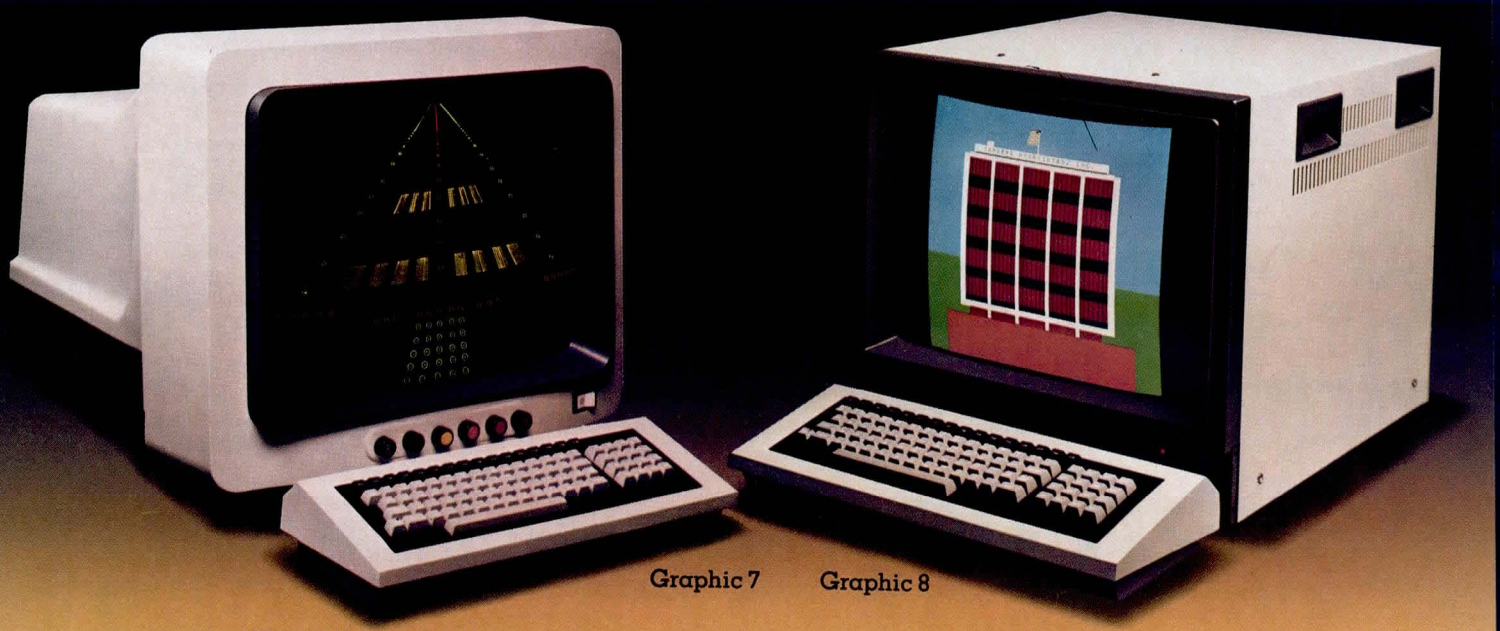
CIRCLE 70 ON INQUIRY CARD

THE BEST OF BOTH WORLDS: STROKE AND RASTER.



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Want high performance raster graphics?

Sanders Associates' new Graphic 8 offers you up to 256 simultaneous colors. High resolution. Dynamic operation with double-buffered refresh memory...

Plus upward-instruction compatibility with the Sanders stroke refresh Graphic 7 and its color and 3D options.

But there's more.

Both display systems – Graphic 7 and Graphic 8 – bring you built-in test, FORTRAN support, remote or local operation, interfaces to most computers, and other important user-oriented features.

Sanders' stroke refresh Graphic 7 and new raster Graphic 8 display systems: they put the best of both worlds at your fingertips. For more information, write or phone Sanders Associates, Inc., Information Products Division, Daniel Webster Highway South, Nashua, NH 03061. 603-885-5280.

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SANDERS

CIRCLE 71 ON INQUIRY CARD

512-k Byte Memory Board Incorporates Onboard Memory Management Unit

MEGA-4, a Multibus compatible memory board, contains up to 512k bytes of read/write memory, a memory management unit, and distributed refresh and full parity generating/checking circuitry. Available from Matrox Electronic Systems Ltd, 5800 Andover Ave, TMR, Quebec H4T 1H4, Canada, the board supports byte-wide and word-wide data transfers and satisfies the large memory requirements of 8-bit 8085 and Z80A, and 16-bit 8086 microcomputer systems.

A 8202 dynamic RAM controller serves as the basis of the board. It performs all distributed memory refresh functions and resolves conflicts between refresh cycle requests and read/write cycle requests. To the user, the card appears as static RAM with a 625-ns worst case access time and 725-ns cycle time.

The memory management unit (MMU) consists of two fast bipolar RAM lookup tables, containing 128 8-bit memory mangement registers each. These are loaded by the system CPU(s) to specify the mapping of the 64 physical memory segments on the board into the 128 logical memory segments in the 1M-byte Multibus address space. The unit facilitates multiprogramming; a supervisor program loads the MMU registers with the appropriate memory map as each user is run. It also permits instantaneous relocation of programs and unlimited system memory expansion. The MMU is disabled by onboard jumpers; it then operates as a conventional memory card with a base address that is strap selectable for any 32k-byte boundary.

Parity generation/checking is performed on each byte to enhance data transfer integrity. An interrupt signal is generated on parity error. During power loss, memory contents are maintained by a single 12-V battery supplying 1 A of current through backup supply terminals.

The board is available in 32k-, 64k-, 128k-, 256k-, and 512k-byte configurations and can be populated with 16k- or 64k-byte RAMs. It measures 30.48 x 17.15 x 1.27 cm, and has an operating temperature range of 0 to 55 °C.

Circle 467 on Inquiry Card

Floppy Disc Controller Reduces Software Overhead For S-100 Bus

LDP72 floppy disc controller reduces software overhead by assuming functions normally handled in software, and meets IEEE 696 specifications for the S-100 bus. Offered by Lomas Data Products, 11 Cross St, Westborough, MA 01581, the controller is IBM format compatible in software selectable, single- and double-density formats. Configured through software commands, it controls any combination of up to four single- or double-sided, 5.25″ or 8″ (13.34- or 20-cm) floppy disc drives.

Based on the Intel 8272 floppy disc controller IC, the controller is capable of performing parallel seeks on up to four drives. A multitrack transfer capability allows the high speed transfer of a complete track on both sides of a double-sided disc from disc to memory, in blocks of up to 16k bytes, with only one command sequence. Programmable data record lengths are available from 128 to 8192 bytes/sector, and an onboard data separator provides maximum data recovery reliability.

Circle 468 on Inquiry Card

Quad-Wide Memory Card Is Compatible with Variety of Systems

NS230, a 256k-byte, quad-wide memory card, is compatible with a wide range of systems. Available in a variety of configurations, from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, capacity of the card ranges from 16k x 16 bits without parity to 128k x 18 bits with parity.

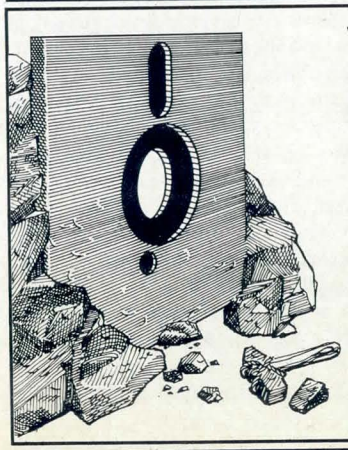
The card provides a read access time of 180 ns, a read cycle time of 490 ns, a write access time of 80 ns/byte, a write cycle time of 390 ns, and a read/modify/write (R/M/W) access time of 700 ns/byte with an R/M/W cycle time of 1000 ns. Features include internal or optional external refresh functions, battery backup provisions, and optional onboard parity generation and checking. An optional 22-bit addressing capability extends the card's use to anywhere within a 2M-word address range.

Mechanically and electrically compatible with the LSI-11, PDP-11/03, and LSI-11/23 systems, the card operates with, or in place of, the DEC MSV11-D and MSV11-E series semiconductor memory cards. It also installs in H9270, H9273-A, or DDV11-B backplanes, or any quad backplane wired for the LSI-11 Q-bus.

Floppy Disc Controller Automatically Determines Recording Density

A single-board floppy disc controller for Multibus systems, MM-SDC-80F interfaces up to four single- or double-sided, single- or double-density, 8″ (20-cm) drives, providing a total storage capacity

(continued on page 136)



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Attractive OEM licensing terms for state-of-the art system software:

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OTHER SOFTWARE: Word Processor, Interactive Assembler, Macro Text Editor, Interactive Debugger.

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MICROWARE SYSTEMS CORPORATION
5835 Grand Avenue, Des Moines, Ia 50312
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of over 4M bytes. The controller, from Mircomation Inc, 1620 Montgomery St, San Francisco, CA 94111, automatically determines recording density without console intervention or changes in switch settings, and allows users to transfer files from single- to double-density diskettes.

An 8257 DMA controller performs the data transfer to and from system memory. The device is interruptable and will complete a transfer when it regains bus control. Data for transfer is buffered in resident RAM, and the I/O parameter block from the system master is accepted and processed by a resident 8085 microprocessor.

The controller is compatible with Intel iSBC-201 and iSBC-202 controllers and is available with or without drives. Without drives, the board is ready for installation with a number of floppy disc drives; it is also available with a set of Shugart SA-801 single-sided or Qume Data Track 8 double-sided drives, mounted in a cabinet with power supply and cables. In addition to ISIS II compatibliity, the CP/M operating system and associated development and application software are available.

Circle 469 on Inquiry Card

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Notice that our linear voice coil actuator and many of our electronics are positioned *outside* the basic package. It makes a big difference in reducing circuit-damaging heat, and cuts your risk of magnetic field-induced data loss. Our linear actuator is a far more accurate and higher performance design than the competition's rotary or stepper motor systems, and more appropriate to tomorrow's high track densities.

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BASF

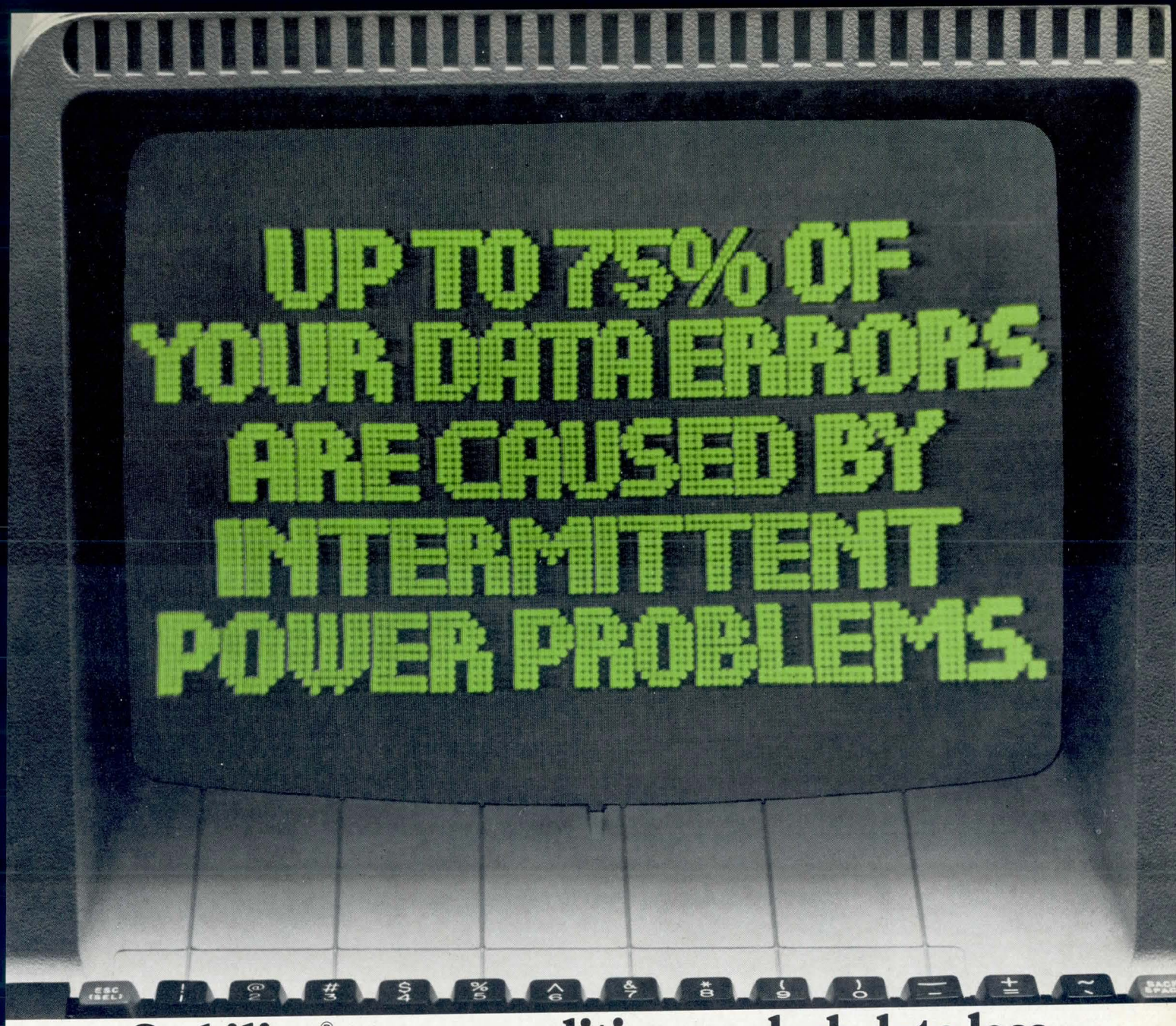
Emulation Terminal Option Expands Development System Capabilities

An emulation terminal system has been added to the model 64000 Logic Development System from Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304. The basic development system (see *Computer Design*, Nov 1979, p 168) facilitates the design, debugging, and troubleshooting of microprocessor based products. The model 64005S emulator terminal system provides users with the realtime functionally transparent emulation features of the logic development system, while retaining familiar in-house development procedures.

Additional Pascal compilers and realtime emulators are planned for the 64000 system. Available options will include Pascal compilers and emulators for Motorola 6802, 6809, and 68000; Zilog Z8001 and Z8002; and Intel 8086 and 8088 processors. A Pascal compiler for the Motorola 6800 processor and an emulator for the Intel 8048 processor will be available as well. The Pascal compilers, and the 8-bit and single-chip emulators, will be identical in function to existing system compilers and emulators. The 16-bit emulators are new to the system.

These 16-bit emulators will allow the user to replace the microprocessor in the system with an emulation probe that will provide debugging analysis and simulation features for system development as well as emulate the microprocessor. Each emulator is supported with an emulation mode that is fully transparent to the target system. DMA transfers and other bus request/grant activities, and normal and segmented addressing are supported; the user can configure the memory assigned to his system to meet particular requirements. Features will include realtime speed with no wait states inserted at up to a maximum clock rate of 8 MHz for the Motorola 68000 and Intel 8086, 5 MHz for the Intel 8088, and 6 MHz for the Zilog Z8001 and Z8002.

Circle 470 on Inquiry Card



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16-Bit μComputer Offers Minimum Chip-Count Solutions To System Designers

TMS9995 "ROM-less" single-chip microcomputer, first member of the 9900 family from Texas Instruments Inc, PO Box 225012, Dallas, TX 75265, supports low cost, minimum chip count applications and gives system designers a new level of minimum chip count solutions. It provides an advanced memory to memory architecture and compatible instruction set, maintaining software compatibility all the way to the object code level. A complete high performance system can be assembled using only a standard I/O peripheral, standard EPROM, ROM, or P/ROM, and the 9995 chip.

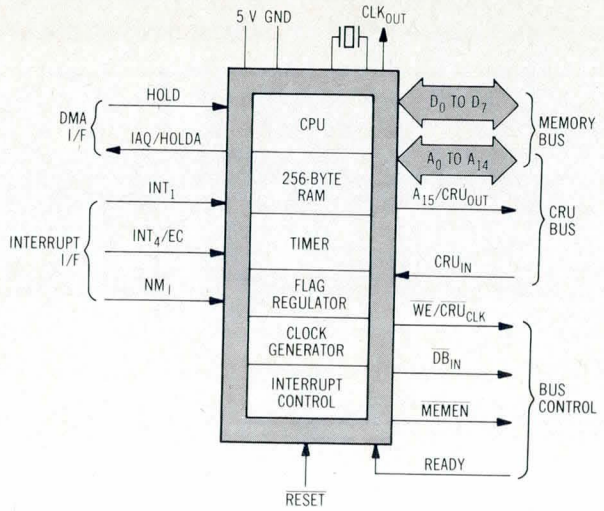
Features include 256 bytes of RAM; 64k bytes of memory expansion; 6-MHz crystal oscillator; a 16-unit timer/event counter; user-definable flag bits; automatic first wait-state generation; 8-bit data bus; separate memory, I/O, and interrupt bus structure; and five prioritized, vectored interrupts. Serial I/O is via a Communications Register Unit (CRU).

The instruction set is composed of the same 69 instructions as the TMS9990, plus four new commands: signed 16-bit multiply and divide, load workspace pointer from memory, and load status register from general memory. Architectural enhancements include two added system interrupts: arithmetic overflow and macro instruction detect. Arithmetic overflow speeds math operations, handling overflow conditions without extra software. Macro instruction detect provides instruction set expansion capability.

The chip is fabricated using silicon gate NMOS. It is offered in either a plastic or ceramic 40-pin dual-inline package and operates in free air at 0 to 70 °C. The chip can be clocked externally, or internally via onchip clock generation logic.

A standalone microcomputer board that supports evaluation of TMS9995 software and hardware features, as well as prototyping of TMS9995 interfaces, the TMAM6095 evaluation module contains a powerful monitor that enables programs to be assembled, edited, and executed. The symbolic assembler also provides reverse assembly capability.

Hardware features include two EIA data communication links that provide for interface to a local terminal and to a host system for upload/download



16-bit microcomputer. Texas Instruments' TMS9995 provides advanced memory to memory architecture and compatible instruction set. Features include 64k bytes of onchip RAM; separate memory, I/O and interrupt bus structure; and 6-MHz crystal oscillator

capability. In addition to the 256 bytes of onchip RAM provided by the microcomputer, 1k byte of external RAM is provided. 6k bytes of EPROM on the board contain the monitor and assembler; however, up to 24k bytes of EPROM may be used by populating the three 28-pin sockets with TMS2564 EPROMs. A large prototyping area provides ample room for breadboarding of the TMS9995 system.

Circle 471 on Inquiry Card

Single-Package System Meets Requirements for Industrial/Business Applications

Cykey model 9910, a Cyberbus based desktop computer from Cybersystems, Inc, 8300 Whitesburg Dr, Huntsville, AL 35802, can be configured to meet specific industrial and business application requirements. Over 60 plug-in cards are available for the computer, including CPU, memory, communications, and analog and digital I/O options.

System features include double-sided, double-density floppy disc drives and a 1k-byte RAM/2k-byte EPROM. Both an integral 80-column matrix impact printer with 133-char/s print speed and a 9″ (23-cm) green phosphor, nonglare CRT provide full point graphics capability (560 x 225 points). Also included are an 108-key detachable Hall effect keyboard with 10 user programmable keys, a light-pen for direct user interface, and a Z80 CPU with CP/M operating system available. A second disc drive, 48k or 64k bytes of RAM, and 6502, 6802, 6809, or 8085 CPUs are optional.

Peripherals offered for the computer include a processor, digitizer, word processing printer, bar code reader, and an integral P/ROM programmer. Mass storage options include an integral 5.25″ or 8″ (13.34- or 20-cm) standalone rigid disc drive.

Offered only to OEMs, the computer supports most high level languages such as BASIC, FORTRAN, COBOL, and Pascal, as well as CP/M compatible software packages. Other operating systems compatible with the computer include MPM for multitasking, multi-user requirements, CPNET for networked systems, Flex for the 6802 processor, and the company's DACSOS operating system for the 6502 processor.

Circle 472 on Inquiry Card

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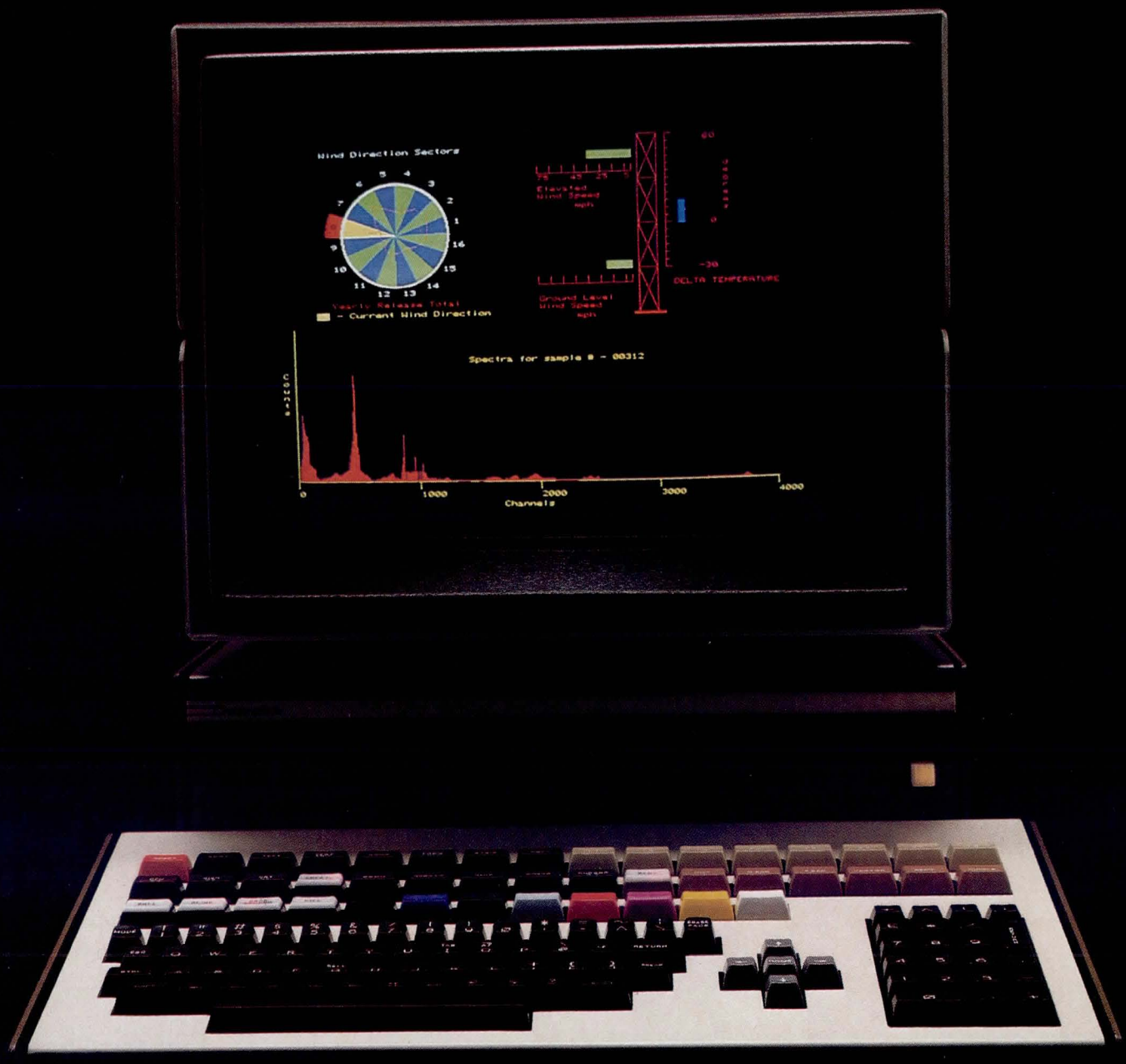

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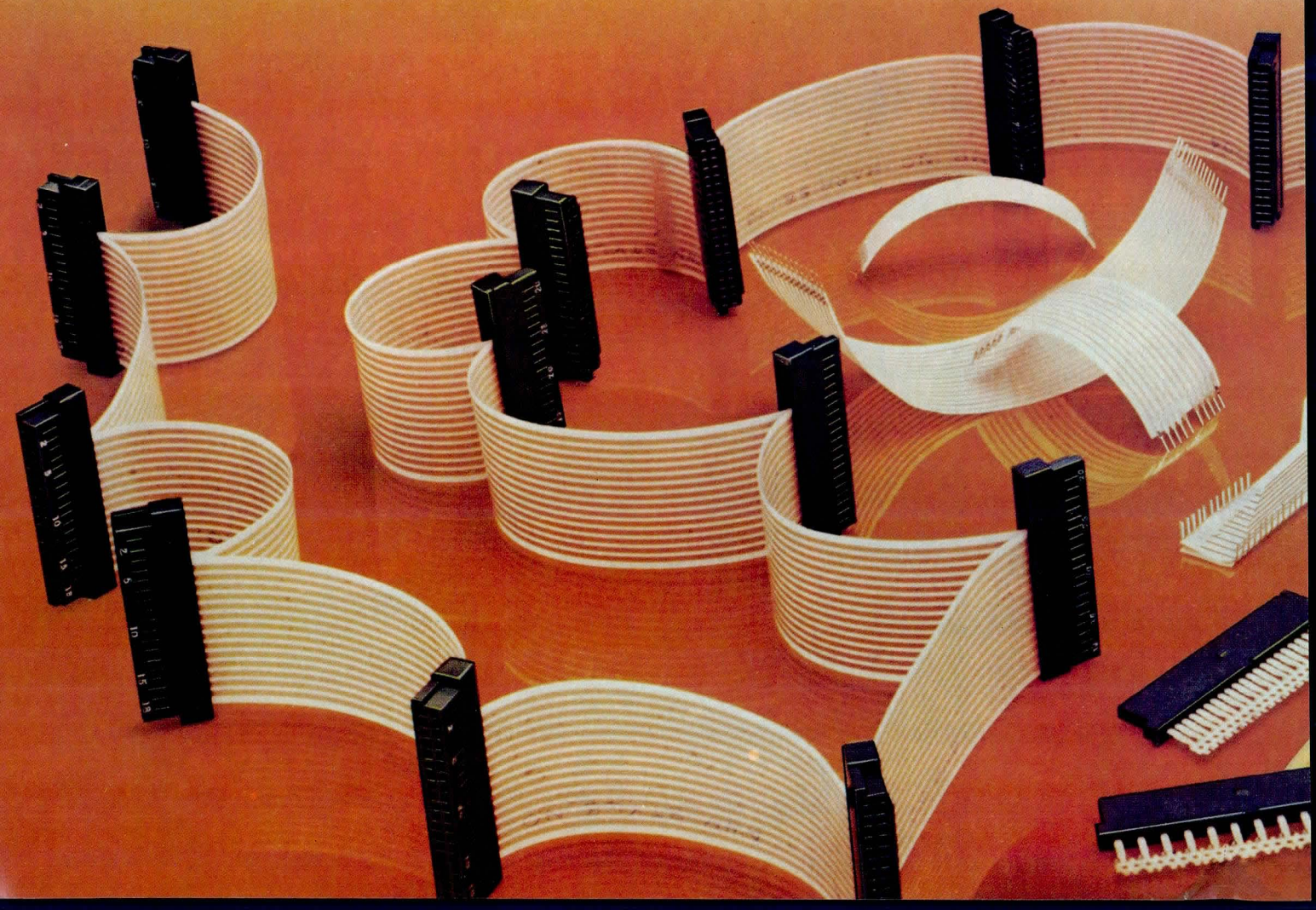
For an easy way to connect FFC or membrane switches to a pc board, our pressure connector clip is the most economical. For intermateability with a wide variety of AMP headers, nothing's more versatile than our insulation displacing connectors.

If you need customized assemblies, we can supply a full range, including flexible etched circuits on thin film base material. They're built to your specifications and 100% tested.

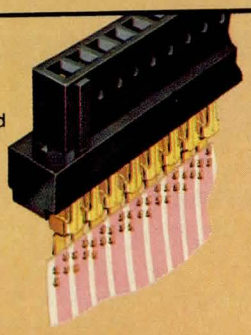


AMP Facts

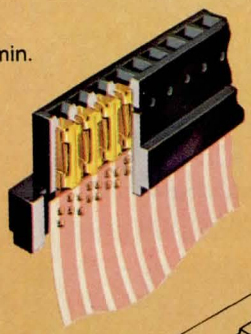
FFC specifications:
centerline: 100" system
current rating: 3 amp
rated temperature: 105°C
high potential: 1,200 VAC RMS
insulation resistance: 5,000 megohms min.
Underwriter Laboratories,
Component Recognized

FFC connector features:
- intermateability with AMP headers
- no cable preparation
- single or double row housings
- pin, receptacle, card edge and solder tab styles

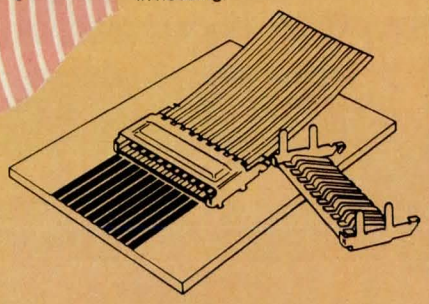
Connector clip features:
- direct conductor-to-board contact
- high contact force
- zero insertion force
- built-in strain relief



Preloaded contacts are mass terminated to cable.



Completed interconnect is seated in housing.



Connector clip simplifies mounting on pc board with a minimum contact force of 400 grams.

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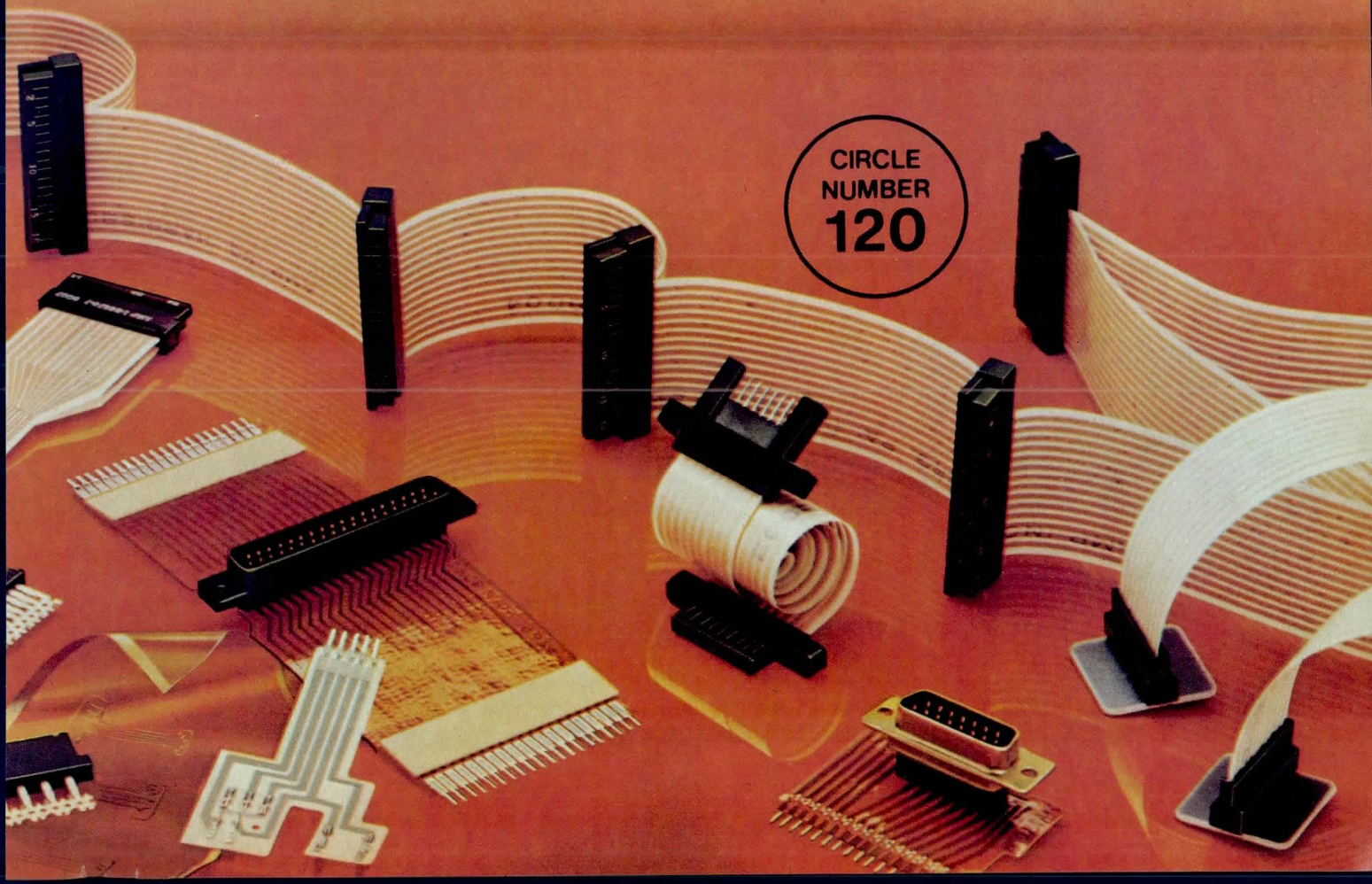

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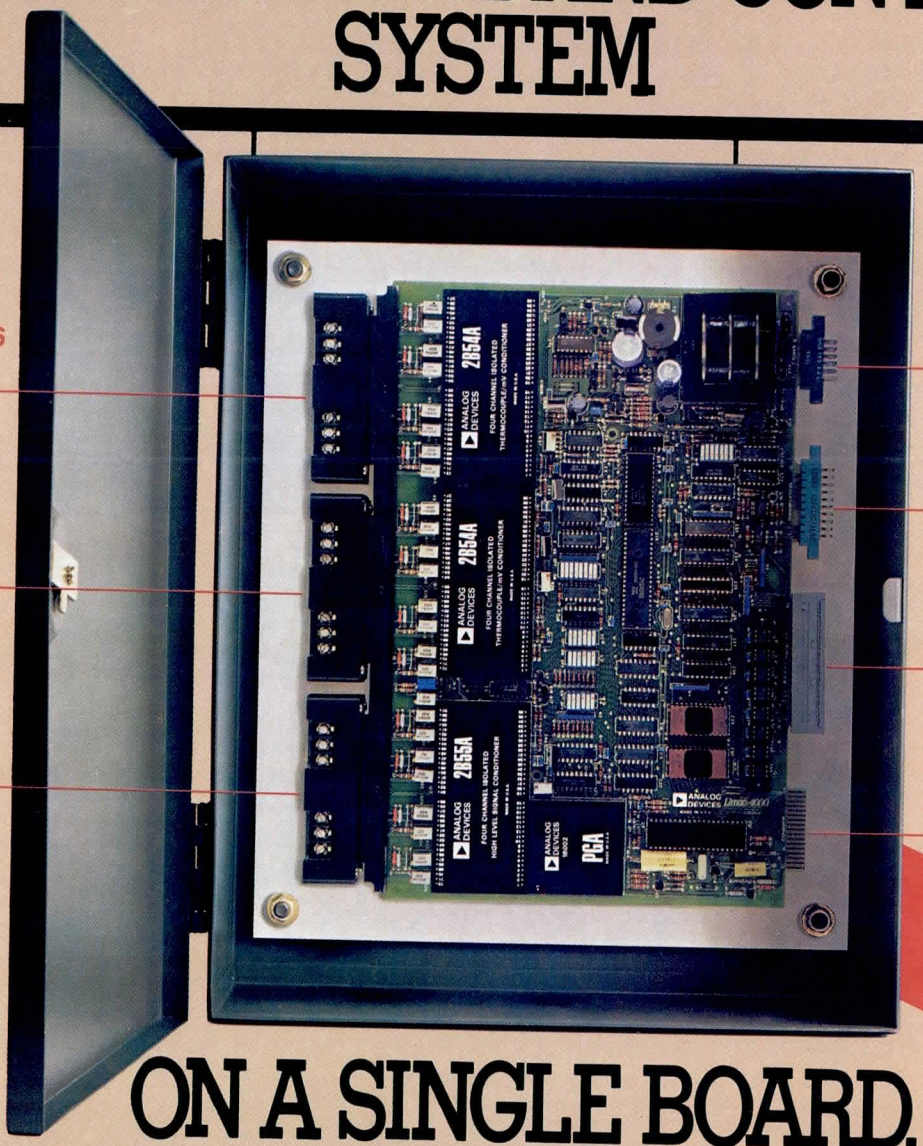

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μMAC-4000 is a fully integrated, precalibrated, intelligent system, complete with sensor signal conditioning, multiplexing, A/D conversion, digital I/O and serial communications to any host computer. Its on-board microcomputer unburdens the host CPU by performing sensor linearization, scaling and conversion to engineering units, and limit checking.

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CIRCLE 76 ON INQUIRY CARD

Add-On Unit Upgrades Personal Computer to Complete Development System

Developmate 81 offers both Z80 incircuit emulation and EPROM/EEROM programming capability to upgrade Radio Shack's TRS-80 personal computer into a complete development system. The unit, a product of Orion Instruments, 172 Otis Ave, Woodside, CA 94062, combines both the in-circuit emulator and the P/ROM programmer into a single box that plugs into the computer's expansion connector.

The computer bus is buffered and extended to a 40-pin connector that plugs into the Z80 socket of the target system, giving target system peripheral devices access to programs running in the TRS-80. With a debug program, reads and writes to the target system peripheral ports can execute to test interface hardware; small test routines can be run, or the complete target system program can be single-stepped or run with up to eight software breakpoints. All testing is done with the program in TRS-80 RAM; clock speed is 1.8 MHz during emulation.

A universal personality module provided by the built-in P/ROM programmer handles 2508 (8k), 2716, 2516 (16k), and 2532 (32k) EPROMS, plus 2816 and 48016 (16k) EEPROMS. Voltages and connections to the P/ROM are defined by a personality module, allowing future devices with up to 28 pins to be accommodated.

When target system hardware and software operate perfectly under emulation, the program is copied into P/ROM using the P/ROM programmer. The target system will run independently when this P/ROM is plugged in and the emulation cable is replaced by a Z80 processor.

The unit is supplied complete with EPROM and EEPROM programming software, power supply, emulation cable, TRS-80 cable, and universal personality module. It will operate with any model I TRS-80 computer, with or without expansion interface. Circle 473 on Inquiry Card

DEC® COMPUTER SYSTEMS COME IN SMALL PACKAGES!!

The SMS Disk System 11X is a powerful table top DEC computer system. Using the latest Winchester disk storage, DEC's RT-11 and RSX-11M operating systems run without the expense, inconvenience, and space requirements of DEC's RL01/RL02 disk cartridge peripherals. Weighing only 80 pounds and requiring only 10½" of table top or rack space, it also offers the following benefits:

MAXIMUM PERFORMANCE AND CAPACITY
- 8.9M bytes of formatted Winchester disk storage plus 1.2M bytes of usable floppy disk storage.
- Fast data transfer of **427K bytes/sec** for Winchester and 63K bytes/sec for floppy.

INDUSTRY COMPATIBILITY
- Automatic recognition of **DEC** RX01, RX02 and **IBM** diskette formats.
- Increases performance of DEC's RT-11 and RSX-11M operating systems.
- Emulates DEC RX02 floppy disk system.

CONVENIENT "MINUTE-PER-MEGABYTE" BACKUP
- Only **40 seconds** required for Winchester backup onto 1.2M byte floppy diskette.
- Standard RT-11, RSX-11M, and SMS utility software supports partial or selective file backup and load operations.

UNSURPASSED RELIABILITY
- Modular construction and minimal parts count ensure **long MTBF** and **short MTTR.**
- Offline system and drive test.
- On board **self test** verifies correct Flinchester controller and disk operation.
- CRT based **interactive diagnostics** ease system test and fault isolation.
- **Automatic bootstrap** tests CPU, memory and Q-bus operation before software loading.

EXCEPTIONAL DATA INTEGRITY
- Winchester disk **flaw management** deletes permanently flawed disk areas.
- Automatic **error retry** recovers soft or temporary errors.
- **ECC (Error Correction Code)** recovers corrupted data without system shut down.
- Patented PLL circuitry requires no field adjustments and provides maximum margins for worst case bit shifted data recovery.

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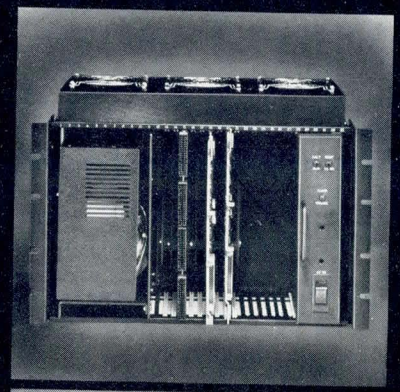

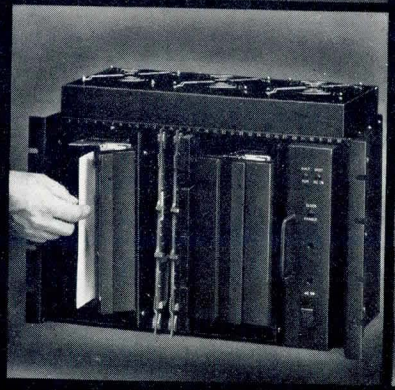

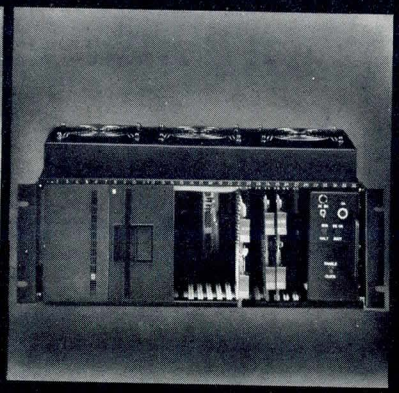

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DATA STACK

Golor Graphics and Sound Generator Offered for S-100 Bus Computers

Using this single-board color video processor and programmable sound generator, an S-100 bus computer can display text, graphics, and animation, with sound effects or music, on a color television set. The board, from Electronic Design Associates, PO Box 94055, Houston, TX 77018, provides 16k bytes of onboard I/O mapped video for storing multiple patterns, and two programmable I/O ports for interfacing to keyboards, joysticks, or other external devices.

A composite video signal that will drive a color monitor or color television through an rf monitor is provided by the Texas Instruments TMS9918A Video Display Processor (VDP). The VDP has four modes of operation: Graphics I mode (256 x 192 dots), Graphics II mode (extended 256 x 192 dots), Text mode (40 characters x 24 lines of user defined characters), and Multicolor mode (64 x 48 positions). It will display up to 32 user definable object oriented patterns, or sprites, that are X and Y positionable and reside in 32 separate display planes. Each plane is superimposed over the previous plane to form a composite picture. A composite video signal from an external source can be coupled into the VDP, superimposing VDP graphics or text over the external video signal.

The VDP chip uses 16k bytes of oncard display memory. Its internal addressing scheme synchronizes display memory requests, resulting in a flicker free picture with only one wait state at 4 MHz. An internal counter chain provides a realtime interrupt signal that can be jumpered to any of the bus vector interrupt inputs.

A 3-channel analog signal that is amplified and capable of driving a loudspeaker is provided by the General Instruments Programmable Sound Generator (PSG). All parameters controlling the output waveform are software programmable.

Three identical programmable square wave tone generators, one for each voice, have a clock rate of 1.8 MHz, and a range from 27 Hz to 111 kHz. The noise generator creates sound effects, producing a frequency modulated pseudo random pulse width square wave output with frequencies from 3 to 111 kHz. Its output can be mixed with any of the three tone generator outputs to provide a combination tone and noise.

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CIRCLE 79 ON INQUIRY CARD

Interactive Display/8k RAM Expand Capabilities of 8-Bit Emulator System

An interactive CRT terminal display capability and an optional 8k bytes of additional RAM memory space increase the versatility of the MicroSystem Emulator. The 8-bit emulator from Millennium Systems, Inc, 19050 Pruneridge Ave, Cupertino, CA 95014 (see *Computer Design*, Jan 1980, p 162), connects to a host computer, allowing it to act as a hardware and software development system for 6800, 6802, 8021, 8035, 8039, 8041, 8048, 8049, 8080, 8085A, 8748, and Z80A microprocessors and microcomputers.

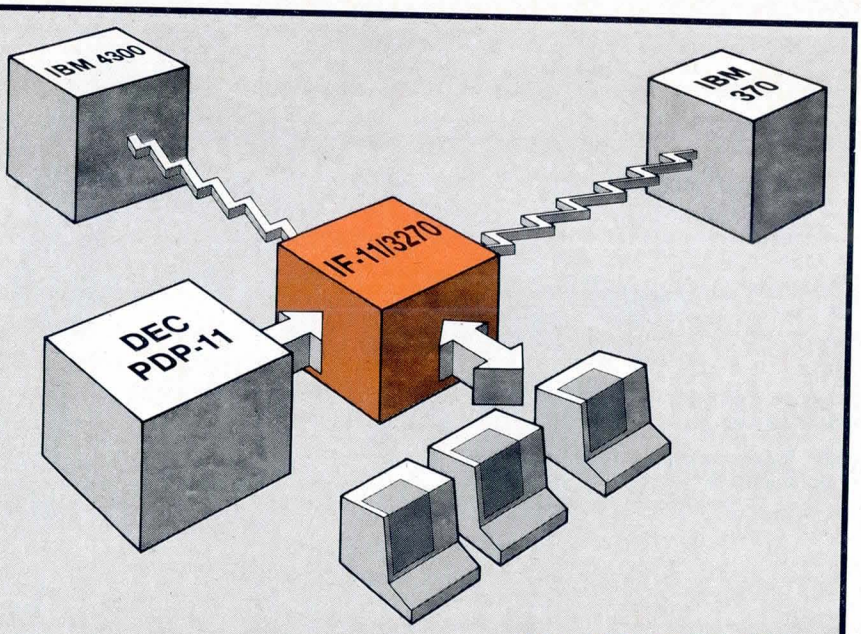
Connected to an auxiliary RS-232 port in the emulator, a CRT terminal will display up to 24 lines of information simultaneously. Users can view blocks of memory or display 23 lines of realtime trace memory at one time. All register contents of the target microprocessor can be displayed with a single keystroke.

Microsystem emulator enhancements. Offered by Millennium Systems, Inc, interactive CRT terminal display capability and additional 8k bytes of RAM increase versatility of Microsystem Emulator

In its "snapshot" mode, the system allows the user to define combinations of status information so that registers, memory locations, and I/O ports can be displayed automatically whenever execution is halted by a step, breakpoint, or run/display command. The CRT terminal and emulator share a single RS-232 port to the host computer, providing the capability of a complete hardware/software integration system implemented through a single port to the software development system.

The standard emulator provides complete debug facilities with 8k bytes of RAM. An optional 8k bytes of RAM extend the emulator mappable memory to 16k bytes. This onboard memory space allows designers to debug larger programs or program modules, and permits programs to be downloaded for execution in the emulator.

Circle 475 on Inquiry Card



3270
COMMUNICATION LINK

IBM mainframe users have an alternative 3270 information display system, the IF-11/3270. Up to 31 display terminals can be clustered with a PDP-11 or VAX system. Individual terminal users may access either of two IBM 370 type hosts, or the local DEC processor at will, or can initiate data transfers between the DEC processor and the hosts.

Displays can be DEC VT-100s or other ANSI-compatible terminals. Under user control, the IF-11/3270 can switch displays from emulation of standard intelligent IBM terminals to normal PDP-11 operation.

A typical installation entails a centralized IBM mainframe database with DEC minicomputers at remote field sites. Since the IF-11/3270 does all BSC protocol processing, the unencumbered DEC system is available for everyday tasks.

If you want more details on how the IF-11/3270 system can serve you better, contact us today.

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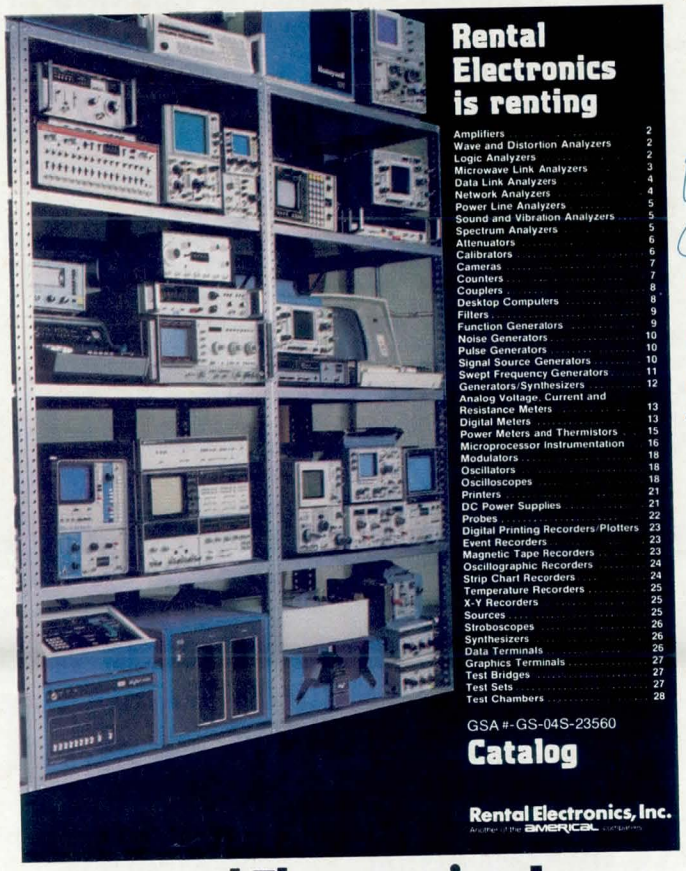

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CIRCLE 81 ON INQUIRY CARD

BRIEFS

Static RAM Module Has Onboard Batteries for Data Retention—A 16k-byte nonvolatile static RAM module designed for compatibility with the EXORciser-Micromodule microprocessor bus, model 9637 utilizes byte-wide CMOS static memory devices supported by onboard batteries for up to three years of data retention when system power is absent. From Creative Micro Systems, 11642-8 Knott St, Garden Grove, CA 92641, the module is organized in two independent 8k bytes that can be selected by onboard switches to operate in any 8k boundary. It can also decode four aditional address lines for use in memory management systems.
Circle 476 on Inquiry Card

Standalone μComputer Supports Network Operating System—Algo 2000, a standalone microcomputer system without a disc, is designed as a network member and supports the Network Operating System version of CP/NET from Digital Research. Offered by Algo, Inc, 10336 Nightmist Ct, Columbia, MD 21044, the unit contains a Z80 microprocessor, two RS-232-C serial interfaces, 32k bytes of RAM, and 2k bytes of ROM. Options include parallel interfacing, Z80 counter timer circuit, and up to 8k bytes of ROM.
Circle 477 on Inquiry Card

C Compiler Generates Object Code for Motorola 68000—C68 compiler system consists of preprocessor, compiler, relocatable assembler, linking loader, support library, and utilities. From Alcyon Corp, 8474 Commerce Ave, San Diego, CA 92121, the system executes on any PDP-11 processor running the UNIX operating system and generates programs that execute on the 68000, standalone or under operating system control.
Circle 478 on Inquiry Card

Power Supplies Deliver 25-W Output—Wall plug-in power supplies from Ault, Inc, 1600H Freeway Blvd, Minneapolis, MN 55430, weigh 11 oz (308 g), deliver 25 W of regulated dc power, and are available in single output (5-V at 5 A) and triple output (5-V at 5 A and ±12-V at 0.2 A) versions. Supplies operate on 105/129-V, 50/60-Hz ac, at 0 to 50 °C, and are available with output terminals or output cable.
Circle 479 on Inquiry Card

Program Features Allow Receipt and Transmission of Data Files—ASCOM microcomputer communications program interacts with remote timesharing services or local computers and is compatible with CP/M type operating systems. From Westico, Inc, 25 Van Zant St, Norwalk, CT 06855, the program receives and transmits data files, and includes communication protocols, conversational mode, batch mode for automatic processing with command files, and system level commands for displaying directories and typing files to a screen or printer.
Circle 480 on Inquiry Card

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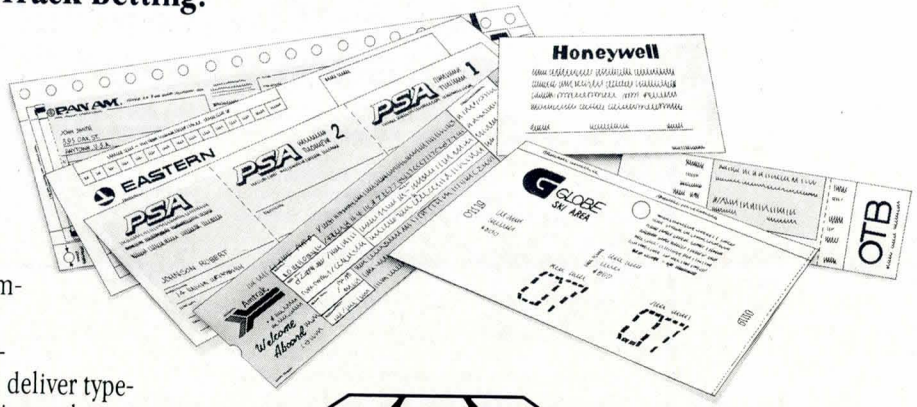

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BRIEFS

Cartridge Disc Drive Expands Storage Capacity of Microcomputer System—A random access cartridge disc drive from Infotecs Inc, One Perimeter Rd, Manchester, NH 03103, features a removable, front load disc cartridge with a 17M-char storage capacity plus a fixed disc cartridge storing 17M, 50M, or 84M characters. Up to eight drives can be interfaced to the company's Control Center 2 microcomputer, giving a maximum total system capacity of 808M characters.

Circle 481 on Inquiry Card

Interface Boards Accommodate Various Types of Disc Storage Systems—Three disc storage interface modules span a variety of disc storage capacities: module 750 interfaces to the 5.25″ (13.33-cm) Shugart 400 floppy disc drives; module 1350 interfaces to the Shugart 800 and equivalent 8″ (20-cm) floppy disc drives; and module 1360 interfaces to the Micropolis 1220 Winchester hard disc drive. The boards are available from Adaptive Science Corp, 4700 San Pablo Ave, Emeryville, CA 94608, and are fully compatible with the company's 6802 and 6809 based ModulasOne bus modules.

Circle 482 on Inquiry Card

Single-Board Computer Utilizes 6502 Microprocessor—From Systems Innovations, Inc, 505 Westford St, Lowell, MA 01851, the CPU 65/08 single-board computer for commercial and industrial applications uses the 6502 microprocessor, accommodates up to 24k bytes of ROM/EPROM and 8k bytes of RAM, and provides 40 I/O lines including four 16-bit timer/counters, two serial lines, and 14 levels of interrupt. The I/O bus supports DMA and is fully buffered with pinouts equivalent to the KIM 4 standard, allowing the CPU to drive expansion boards directly.

Circle 483 on Inquiry Card

Board Permits μComputer to Add Memory, Disc Drives, and Printer—Model EXP-100 expander provides 32k-byte memory expansion, a mini-floppy disc interface for four drives, a Centronics parallel printer interface, an RS-232 interface, and an S-100 bus for the PMC-80. Available from Personal Micro Computers, Inc, 475 Ellis St, Mountain View, CA 94043, the expander will run TRSDOS software as well as other operating systems designed for TRS-80 compatibility such as NEWDOS and VTOS.

Circle 484 on Inquiry Card

Intelligent Bus Slave Supports Cartridge Tape Drive—An 8085 based intelligent bus slave from Alloy Engineering Co, Inc, Computer Products Div, 85 Speen St, Framingham, MA 01701, the DMB-1 controller allows up to four DEI Funnel or equivalent 13.4M-byte tape cartridge drives to be interfaced to the Multibus for Winchester disc backup and file storage purposes. It provides up to 8k bytes of onboard buffer memory and runs under CP/M and MP/M when operated with an 8080, 8085, or Z80 bus master. Software is supplied on an 8″ (20-cm) single-sided, single-density floppy disc in CP/M format, and is also available for ISIS based systems.

Circle 485 on Inquiry Card

64k-Byte Dynamic Memory Module Is STD-BUS Compatible—From DY-4 Systems Inc, 1573 Laperriere Ave, Ottawa, Ontario K1Z 7T3, Canada, the DSTD-364 64k-byte dynamic memory card for STD-BUS applications features vertical and horizontal paging under software control, allowing the implementation of memory management and up to 512k bytes of memory on the STD BUS. For compatibility with existing systems, the paging register can be hardwired for contiguous addressing.

Circle 486 on Inquiry Card

Prototype System Contains Components Necessary to Implement Standalone Z80 STD BUS System—A Mostek MDX-CPU2 card, XTDTRS interface card, 6-slot STD card cage with wire wrap and extender cards, static RAM memories with custom address P/ROM and interface cable for Radio Shack's TRS-80, Mostek DDT-80 debug operating system in ROM, and 5.25″ (13.33-cm) floppy diskettes containing driver software for the TRS-80 are included in the TRS-PROTO packaged prototype system manufactured by Xitex Corp, 9861 Charwell Dr, Dallas, TX 75243. The complete package is available in both 2.5- and 4-MHz configurations and operates from a single 5-V supply.

Circle 487 on Inquiry Card

Fortran Added to 6800 Development System—FORTRAN compiler for the Sprint 68 development system operates in UCSD system software environment that includes an operating system, editor, assembler, and UCSD Pascal. Assembly language and Pascal programs can be linked with FORTRAN programs. The UCSD system package, including both Pascal and FORTRAN, is a product of Wintek Corp, 1801 South St, Lafayette, IN 47904.

Circle 488 on Inquiry Card

Programming Language Offers Assembly Language Features Plus High Level Language Techniques—C programming language combines assembly language features and power with the structured programming techniques of higher level languages, and is available from Cromemco, Inc, 280 Bernardo Ave, Mountain View, CA 94043, for their Z80 based, S-100 microcomputer systems. It runs under the company's multiuser, multitasking, CROMIX operating system, producing relocatable code that can be linked with the company's FORTRAN, COBOL, and assembly language, or called from BASIC. C is offered on 5″ (13-cm) or 8″ (20-cm) diskette.

Circle 489 on Inquiry Card

Magnetic Tape Peripheral Is HP-85 Compatible—A digital mass storage system that reads and writes ANSI, ECMA, and ISO compatible 0.25″ (0.63-cm) digital cartridges using intelligent and variable file structures, model GPIB-3000 recorder provides storage for approx 3.35M bytes of data per removable DC 300XL cartridge. Available from Innovative Data Technology, 4060 Morena Blvd, San Diego, CA 92117, in tabletop or rackmount configuration, the recorder supports three additional slave drives via a dual-buffer front end.

Circle 502 on Inquiry Card

Unit Translates 8085 Signals into 8080 Signals—ICE-85 signals are converted to ICE-80 signals by the 85/80 Emulator/Converter from NWW Micro Systems, PO Box 43013, St Paul, MN 55164, allowing users to emulate 8080 signals in their system. The unit consists of an electronic module with emulator cable, is transparent to the ICE-85 device, operates in real time, and receives its operating power from the user's base system.

Circle 503 on Inquiry Card

Microcomputer System Offers Data and Word Processing Capabilities—Packaged as a desktop unit or in OEM configurations, the MT500 provides both data and word processing capabilities for business or scientific applications. Available from Maatra Corp, 1835 W Shryer Ave, Roseville, MN 55113, the system features a full video display, Z80A microprocessor, CP/M operating system, 64k bytes of RAM, two 500k-byte 5.25″ (13.33-cm) floppy disc drives, and Selectric type keyboard. Options include printers, 103- or 212A-compatible modems, and business and scientific applications software.

Circle 504 on Inquiry Card

SOFTWARE

Disc Operating System Supports 16 User Tasks On TM990 Development System

A multi-user, multitasking development operating system for the 16-bit Texas Instruments TM990 microprocessor family, PDOS/EXPRES supports up to 16 concurrent user tasks with prioritized round robin clock swapping. Available from Eyring Research Institute, Inc, 1455 W 820 N, Provo, UT 84601, the system supports large or small floppy discs, hard discs, bubble memory, and extended memory capabilities of up to 256k bytes. Up to 32 contiguous or noncontiguous files can be open simultaneously in sequential, random, shared, and read only access modes.

Included in the system are an 8k-byte PDOS module, advanced EXPRES BASIC language interpreter, character and screen editors, assembler, complete floating point package, and user utility enrichments for program development. Also available are standalone run modules, and source listings for most utilities.

The EXPRES BASIC interpreter uses advanced interpreting techniques to approach execution speeds of common threaded code compilers while maintaining the interactive approach to program development. Features include multiline, recursive functions with local variables, variable names of unlimited length, context oriented string handling, disc interface primitives, hex number conversions, assembly language linkage, and color graphic command primitives.

Circle 505 on Inquiry Card

Cross Compiler Allows μProcessor Software Development On Timesharing Minicomputer

Pascal cross-compiler permits microprocessor software to be developed in high level languages and pretested on timesharing minicomputers, providing a far more efficient and less costly method than other means. Microprocessor development systems are used only for final software integration and testing in a hardware environment or for functions not available on the host. This approach, developed by Intermetrics, Inc, 733 Concord Ave, Cambridge, MA 02135, minimizes the number of programmers and microcomputer development systems needed for a project, maximizes programmer productivity, and increases the efficiency and predictability of software development cycles.

Designed for use with Digital Equipment Corp's PDP-11 minicomputers running under Bell Laboratories' UNIX or DEC's RSC-11M operating systems, the package is compatible with the 1980 ISO Pascal draft standard. Written in Pascal-Vu, it includes compiler front end, EM-1 interpretive language, host and target microprocessor development system (MDS) code generators, and host and target MDS interpreters.

The front end Pascal to EM-1 compiler program produces compact EM-1 assembly code. After compilation, there are two ways in which to run the compiled programs: interpretation or compilation to true PDP-11 code. Through interpretive program execution, EM-1 code is simulated by the EM-1 interpreter on the PDP-11, allowing the program to be pretested, and problems diagnosed, before it is transferred to the MDS.

The second method of running compiled programs translates the EM-1 instruction set to native code. The UNIX assembler and loader produce a program that is directly executable on the MDS. This method results in execution speeds about seven times faster.

Both methods can be intermixed, using the interpretive method to run programs that are not used frequently, and native code to run those that are performed frequently. On the MDS, code produced by either of these methods can be intermixed with assembly code produced by the MDS.

Two libraries are included in the software package, one containing often used external routines for Pascal programs, and one containing Pascal runtime routines. There are two versions of each library: one for the EM-1 interpreter resident in the PDP-11, and one used when programs are transferred into PDP-11 code.

Circle 506 on Inquiry Card

Programming Language/Operating System Speeds Software Development For Exorset μComputer

An operating system and programming language, polyFORTH for the Motorola Exorset 30 microcomputer speeds software development of high performance applications. From Forth, Inc, 2309 Pacific Coast Hwy, Hermosa Beach, CA 90254, it is a fully interactive development tool for instrumentation, process control, data acquisition, graphics, and similar applications.

The Exorset version of polyFORTH (pF6809/30) features a screen editor in addition to the standard multiprogrammed operating system, assembler, interpreters, and FORTH language compiler. Options include 2-D graphics, a math package based on fixed point fraction arithmetic, and file management.

Circle 507 on Inquiry Card

Cross Support Software For Development System Includes Macro Assemblers

Cross support software for the Intel MDS model 230 microprocessor development system allows programmers to develop products using the 6800 microprocessor family. American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, offers four macro assemblers supporting the 6800 family on the microprocessor development system: 6800, 6802, and 6808; 6801 and 6803; 6805; and 6809.

Each assembler supports local and global labels, and includes both arithmetic and logical operations. A screen oriented editor with menu select speeds editing; programmers can scan through 23 lines of code displayed on the screen and edit by overwriting the existing code or selecting commands from the menu.

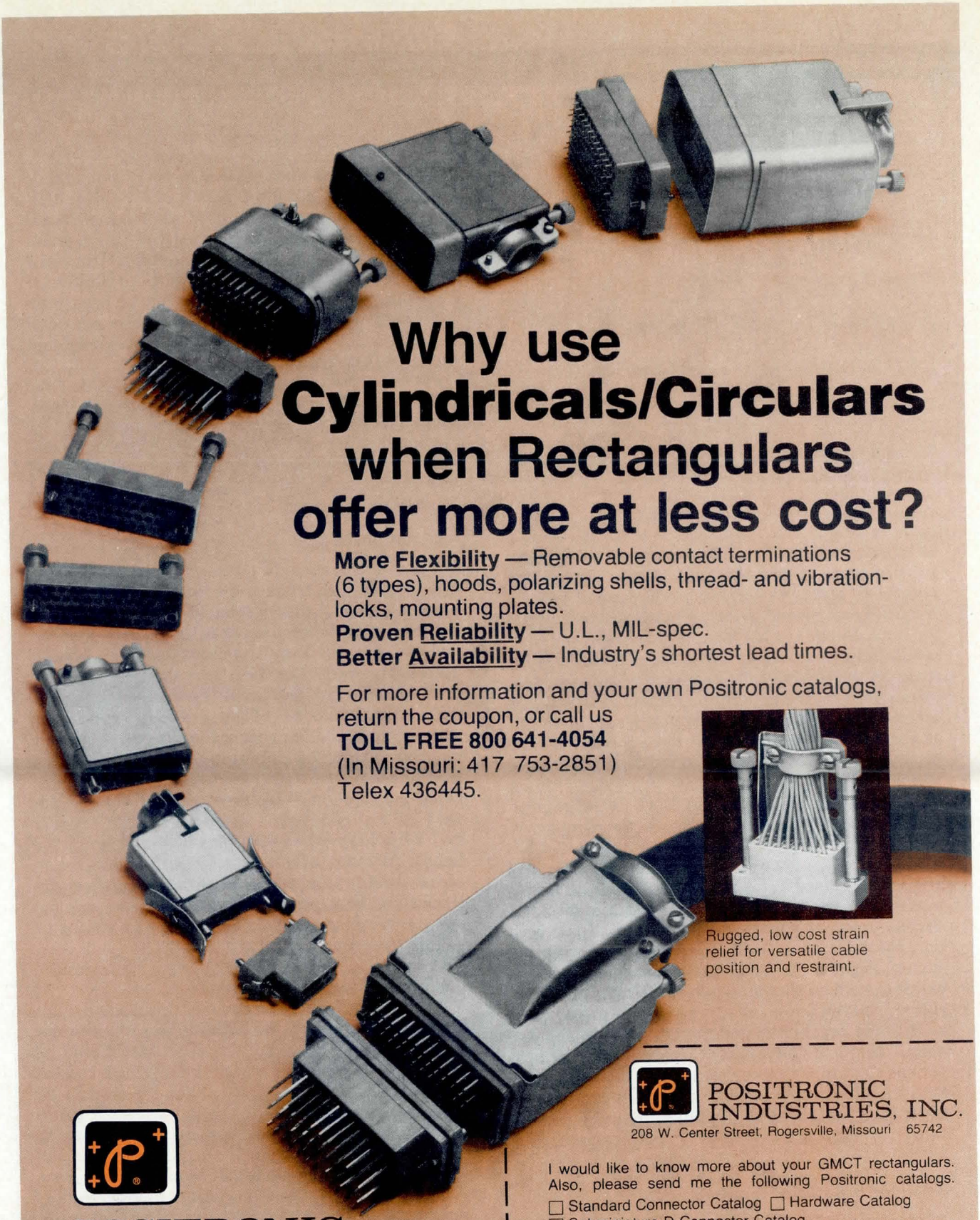
Circle 508 on Inquiry Card

Cross Assembler Uses IBM-370 Mainframe to Develop Z8000 Programs

A cross assembler for the Zilog Z8002 16-bit microprocessor is available from Alan Associates, 605 Locust Lane, State College, PA 16801. It allows the development of Z8000 programs with a minimum of microcomputer hardware and uses the IBM System/370 mainframe as a host.

Operated using paper cards on a batch system, or without any paper on a system with a text editor, the system offers macro capability, a hash addressed symbol table, and user defined mnemonics. Input is assembler source using Zilog mnemonics and conventions; output is hexadecimal Tektronics format with checksum on paper cards or images.

Circle 509 on Inquiry Card



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CIRCLE 84 ON INQUIRY CARD

Replacing 2111 RAMs with Contemporary Parts Ensures Availability and Improves Performance

Richard Nedinsky
GTE Microcircuits
2000 W 14th St
Tempe, AZ 85281

Designers of small microprocessor based systems are beginning to feel the pinch of the diminishing number of static RAM options. These small systems frequently use small RAMs as convenience buffers, but semiconductor RAM vendors are phasing out their small, easy to use static RAMs and are focusing instead on the needs of the high volume, high performance minicomputer and mainframe markets that utilize large, dense memory components. In addition, as the state of the art moves toward 64k dynamic RAMs and other dense parts, limited plant capacity requires manufacturers to phase out older product lines. Consequently, static parts such as the popular 2111, a 256- x 4-bit static RAM, are becoming difficult to find.

Introduced in 1973 as a state of the art part, the 2111 RAM enjoyed great popularity for some years, but is now being replaced by faster and denser RAMs. Because over the past two years, half of all 2111 vendors have abandoned the part, new product designers cannot depend on its continued availability, and existing products that incorporate 2111s must be redesigned. Nevertheless, 2111-type static RAMs have worthwhile capabilities and there is a continuing demand. They are simple, easy to use, and fast enough (250 ns t_{acc}) to interface directly with contemporary MOS microprocessors. Small static RAMs continue to track the state of the art, manifesting technical advances as improvements in price, performance, and reliability.

Selecting a Replacement RAM

Alternatives to 256 x 4 2111 static RAMs include the 1k x 4 2114, the 1k x 8 8114, the 2k x 8 8116, the 4k x 1 2141, the 1k x 4 2142, and the 256 x 8 3539. The 2111 has a sister part, the 2112, also organized as 256 x 4 and threatened with extinction. RAMs organized 512 x 8 are not commercially available.

Selection of an alternative chip initially should be based on bit organization. A pair of 4-bit wide 2111s provide a memory 256 words deep. Since additional memory is not needed, replacing 2111s with a memory deeper than 256 would be wasteful. If the host microprocessor system operates with an 8-bit wide data bus, the 2111's replacement should have 8-bit wide data words. This reduces the necessary RAM package count by 50%, thus cutting inventory and board stuffing costs.

Having selected a 2111-replacement RAM, the designer should contact the manufacturer to determine the part's long-term delivery potential, including the product life cycle and the vendor's commitment to manufacture in the future. Data sheets and sample parts should be acquired after continued availability is assured.

RAM Retrofitting

If a host microprocessor product has been in production long enough to have one of its component ICs become obsolete, most probably the original design engineer is no longer associated with that product, and the retrofit designer must familiarize himself thoroughly with the host circuitry. A recently manufactured printed circuit board containing the relic 2111s should be obtained and a scope or a variable threshold bus analyzer used to determine the input, output, and supply voltage levels and the chip select, read/write, and output-disable pulse widths. Direct substitution of the new RAMs for old may not yield the desired results because the original designer may have strapped various pins high or low, or the sample part may have been selected for too long an access time. The 2111's published specifications should not be depended upon because the original designer may have created some marginal timing or voltage situations, eg, the 2111 specification calls for a data setup (t_{DW}) of 150 ns yet there is no assurance that it is provided by the host circuit.

Existing 2111s should be powered down and cut out after the action of the host circuit on the RAMs has been thoroughly analyzed. The new RAM should be installed by temporarily wiring the conductive paths to an unmounted socket. Then the system can be powered up and activated.

When the new parts have been qualified for use as long-term replacements for the 2111s, the printed circuit board should be modified. Many companies do not switch abruptly from one part to another but instead build boards with both parts for an evaluation period, comparing the new part with the old part in the field. This interim period allows for control of the depletion of the inventory of old 2111s.

A working example of this phased replacement strategy is provided in the block diagram of a

(continued on page 154)

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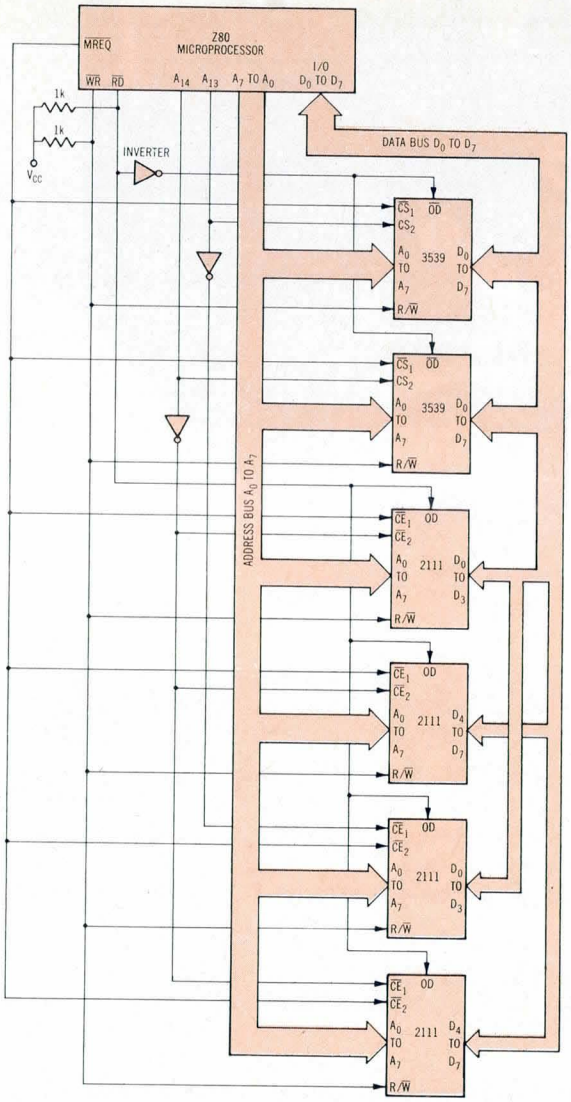

Block diagram of system that once required eight 2111 RAMs. Contemporary 3539 RAMs are being phased in. Four 2111s have been replaced by two 3539s

microprocessor based product requiring four 211S, organized as a 512 x 8 convenience buffer. Sockets have been provided to replace all the 211S with two 3539s. Therefore, the board can be built with 2111s or 3539s. The 3539s' chip select lines are temporarily wired into the system's address bus ahead of the inverters that drive the 2111s' chip enable inputs. These inverters will be available for other uses or can be removed from the system when the 2111 RAM population has been phased out. The memory access time improves because the propagation delay time introduced by the inverters is eliminated.

Designing New Products with 3539s

A convenience buffer using 3539 RAMs requires half as many address decoders as one implemented with 2111 RAMs. Consequently, aggregate input leakage is cut in half, and the controlling microprocessor often performs better, especially at higher temperatures. Memory systems with fewer components are quicker and easier to design. The reduction in parts count helps increase MTBF and reduce MTTR. Since 3539 RAMs are designed as constant current devices and do not cause erratic impedance changes on the 5-V bus, they do not require power supply decoupling capacitors.

A single 3539 RAM provides twice the buffer storage of a 2111 and features 2k-memory bits, organized 256 x 8. This allows a 2 to 1 RAM package count reduction, freeing a corresponding amount of printed circuit board real estate. The 3539 features both high and low chip enable inputs, reducing the number of hex inverter sections required to interface the chip (2111 RAMs do not provide true-high CE inputs). Maximum data access time for the standard 3539 is 300 ns and falloff selections provide t_{acc} of 400, 500, and 650 ns at correspondingly lower prices. Special application 3539 RAMs are also available. One provides a 48% power reduction, from 400 to 210 mW, for portable products. Another conforms to MIL-STD-883B and provides high reliability for use in harsh environments, such as automobiles and avionics.

Summary

Easy to design convenience buffers for use in small microprocessor based systems are being threatened by the disappearance of 1k static RAMs. The 1k parts are being replaced by dense dynamic RAMs. RAM vendors have divided into two groups, one servicing the mini- and mainframe markets, the other the recently developed, growing microprocessor based consumer products market. Manufacturers of microprocessor based consumer products and other small systems can phase out the once popular 2111 RAMs and replace them with more contemporary parts, such as the 3539 RAM.

Please rate the value of this article by circling the appropriate number in the "Comments" box on the Inquiry Card.

High 725 **Average 726** **Low 727**

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CIRCLE 86 ON INQUIRY CARD

16-Pin 64k N-Channel Dynamic RAM Employs PDP Capacitor in Memory Cell Structure

A recently announced 64k x 1 NMOS dynamic RAM utilizes a polysilicon dielectric polysilicon (PDP) capacitor in the memory cell structure.* This structure is claimed to offer performance and density advantages over conventional approaches. The 64k device, from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, also employs an unusual sense amplifier configuration that multiplexes two pairs of bit lines for each sense amplifier. This technique reduces the number of memory cells per bit line by one-half. The result is shorter bit lines and an increase in the signal voltage available to the sense amplifier. PDP memory cell and sense amplifier configurations provide signal voltages up to four times greater than are available with conventional designs.

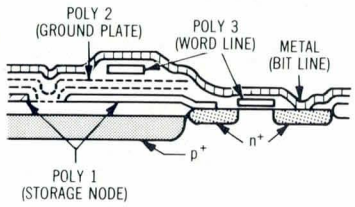

Fig 1 Cross-section of triple-poly memory cell with PDP capacitor. Structure is claimed to provide two times storage capacity of predecessors for a given memory cell size and dielectric thickness, as well as improved refresh characteristics

The cross-section of a PDP storage capacitor is shown in Fig 1. The capacitor is formed between the storage node (poly 1) and the ground plate (poly 2). A third layer of polysilicon is used for the word line (poly 3). The storage node is connected to the source of the switch transistor by a buried contact in each memory cell. A shared contact connects the drain to the metal bit line.

Efficient area utilization is the major asset claimed of the PDP capacitor. In this structure, the space separating the PDP capacitors accommodates the switch transistor. Also, the space between adjacent PDP capacitors is limited by photolithography and not by electrical isolation problems common to previous inversion capacitor structures. Thus, a larger capacitor is possible per memory cell area.

In previous double-poly memory cells, the channel length of the switch transistor was difficult to control because of the poly-to-poly alignment tolerance. With the PDP memory cell, the switch transistor is formed by poly 3 and is thus self-aligned to improve control of threshold voltage and subthreshold current leakage.

The PDP cell also provides an improved quality storage medium. In conventional inversion capacitor designs, the capacitor area is subject to junction leakage to the substrate. In the PDP cell, about 20% of the total memory capacitor area is formed by an n^+ area, which can leak to substrate. The major portion of the capacitor is formed by two polysilicon plates separated by a high quality dielectric. Thus, the refresh characteristics of the PDP memory cell are superior to those of inversion capacitor cells.

Except for the memory array, the 64k RAM, designated NMC4164, is implemented in standard N-channel silicon gate technology. (See Fig 2.) The device is a companion part to the company's other 5-V dynamic RAMs, which include the 16k NMC5295, and 32k NMC4132. Produced in 16-pin dual-inline packages, the parts are TTL compatible, feature Tri-State® outputs, and operate from a single power supply. Versions of the NMC4164 will be available with access times of 120, 150, 200, and possibly 250 ns. Active and standby currents are 40 and 4 mA, respectively. Refreshing is required every 4 ms. This can be accomplished by performing any cycle that brings the row address strobe ($\overline{RAS}$) active, including an $\overline{RAS}$ ($\overline{RE}$)-only cycle at each of the 256 row addresses.

Circle 441 on Inquiry Card

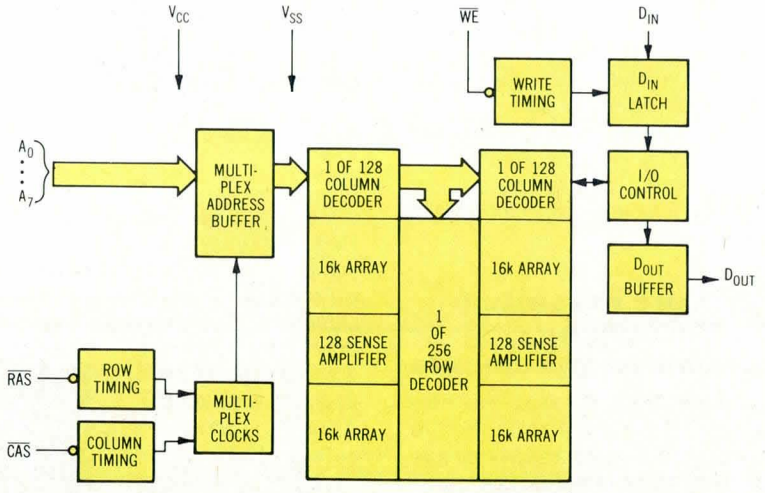

Fig 2 NMC4164 64k dynamic RAM with novel sense amplifier configuration. By multiplexing bit lines, number of memory cells attached to each bit line is halved, nearly doubling signal voltage available to sense amplifier. Device features multiplexed address input with separate row and column strobes

*F. J. Smith, R. T. Yu, I. Lee, S. S. Wong, and M. P. Embrathiry, "A 64k-Bit MOS Dynamic RAM with Novel Memory Capacitor," *IEEE Journal of Solid-State Circuits,* vol SC-15, no 2, Apr 1980, pp 184-189

CORRECTION

The company name and address for the IC Loop item "Two High Speed P/ROMs Available" (p 189) in the February issue should have read: Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94086.

Cortron announces a solid state keyboard at "bare bones" prices.

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CIRCLE 87 ON INQUIRY CARD

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6808	**8039-6**	**3874**
6802	**8035**	**3876**
Z80A	**8021**	**F8**
8080A	**8022**	**1802**
8085A	**8041A**	**6500/1**
8049		

Assembler support is available now for the 16-bit chips listed below. Emulation support for the 9900 is available now. Real-time emulation and Pascal support will be available in stages for the 68000, Z8001, Z8002 and 8086 beginning the third quarter of 1981.

68000	**Z8001**
8086	**Z8002**
SBP 9900	**TMS 9900**

```
LOC  INST      MNEM  OPER      EFADD A  B  X    Y    U    S    CC DP
1003 8E4000    LDX   #4000           00 05 4000 0005 0006 0002 50 00
1006 AB00      ADDA  X+             01 05 4001 0000 0000 0002 50 00
1008 5A        DECB                 01 04 4001 0000 0000 0002 50 00
1009 26FB      BNE   -05        1006 01 04 4001 0000 0000 0002 50 00
1006 AB00      ADDA  X+             03 04 4002 0000 0000 0002 50 00
1006  <BREAK     TRIG1>


> GO SYMBOL

LOC  INST      MNEM  OPER      EFADD A  B  X    Y    U    S    CC DP
1006 AB00      ADDA  X+             03 04 4002 0000 0000 0002 50 00
1006  <BREAK     BKPT1>


> TTA 3

ADDR DATA      MNEMONIC                    EXTERNAL          BUS
1009 26        BNE                         00000000          M R F
100A FB                                    00000000          M R
1006 AB        ADDA                        00000000          M R F
```

6809 Prototype Control Probe tip fits easily in hard to reach locations. Probe status lights monitor key processor signals.

(top) Trace All display gives disassembled prototype code plus the status of all key processor registers on a step-by-step basis.

(middle) Symbolic debugging allows all major address locations to be defined as easily read mnemonics. Breakpoint information includes full display of processor status.

(bottom) Trigger Trace display shows real-time bus activity on a cycle-by-cycle basis plus eight channels of hardware logic defined by the user.

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Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312.
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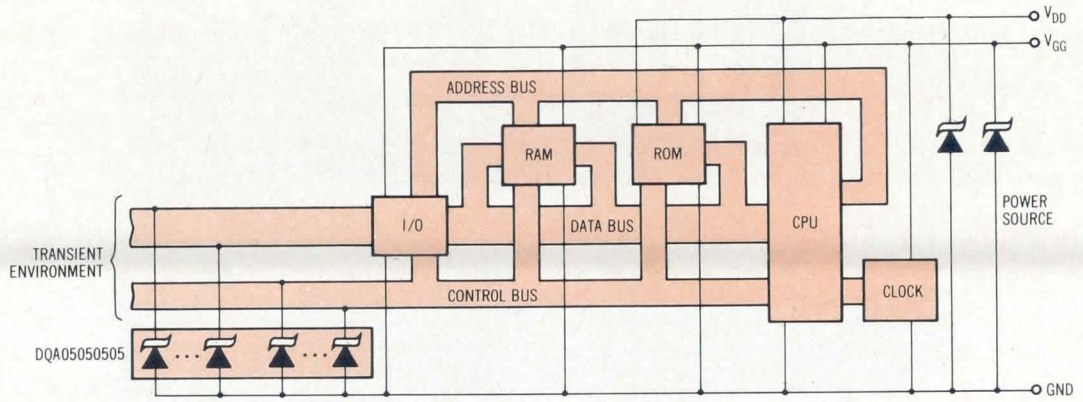
16-Pin Dual-Inline Transient Voltage Suppressor Offers Multiple-Circuit Protection

Designed as a single protector for multiple-power input applications, a 16-pin dual-inline transient voltage suppressor series accommodates automated insertion in boards adjacent to the circuit or components that require protection. Each device in the standard DQA and selected DQB series from General Semiconductor Industries, Inc, 2001 W Tenth Pl, Tempe, AZ 85281, provides four separate TransZorb^R arrays that allow the user to select single- or multiple-voltages from 5 to 50 V. The standard DQA05051212 provides a voltage combination of 5, 5, 12, and 12 V, common to many microcomputers and microprocessors. For digital input applications, pairs of devices can be connected from each line to ground for maximum protection.

Each device has a response time of less than 1 x 10^{-12} s, with adequate protection levels for the most sensitive MOS memories and microprocessors. Peak power dissipation is 600 W at a 10 x 1000 impulse. Static discharge can exceed 10,000 V for 10 ms with a 60-A current potential. Applied to typical TTL circuit for 30 ns, 10 V will cause destruction. Placing transient suppressors across the signal lines to ground will keep unwanted transients out of data and control buses. Transient suppressors that are shunted across the power lines maintain a continuous operating voltage during ac line surges and switching transients.

The DQA family of devices includes a 4-cell array characterized by the reverse standoff voltage, synonymous with the integrated or microcircuit power supply voltage. The breakdown voltage is that point at which the transient suppressor is in avalanche breakdown. This point is temperature dependent and has a positive temperature coefficient. Allowance has been made in establishing the minimum breakdown voltage at 25 °C to provide safe operation over the full temperature range of −65 to 150 °C.

Circle 442 on Inquiry Card



DQA transient suppressor application. Transient suppressor from General Semiconductor Industries prevents microprocessor system failures on signal and input power lines caused by transients (electrostatic charges), ac power surges, or switching of power supply to ON or OFF

GIMIX & MICROWARE present the 6809 PROFESSIONAL TOOLBOX

A **GIMIX** 56KB static RAM 2Mhz 6809 Dual Drive Mainframe System with **MICROWARE's** Multiuser OS9 Pro-Package --special combination price **$3968.09.** This system includes the **GIMIX** Mainframe with 30 amp C.V. ferro-resonant power supply, SS50/50C Motherboard, 2Mhz 6809 CPU with time of day clock and battery back-up, 6840 programmable timer, 2 serial ports, 56K Bytes of Static RAM, and two 5¼" disk drives and double density controller installed in the **GIMIX** Mainframe with the same brownout protection and power supply reliability that **GIMIX** is famous for.

MICROWARE's OS9 Pro-Package includes OS9 Level 1, the BASIC09 interactive compiler, Macro Text Editor, Interactive Assembler, and Interactive Debugger which gives you the necessary tools for efficient structured software development.

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And this system is expandable. You can add memory, I/Os, video or graphics cards, Arithmetic processors, additional drive capacity, and other hardware now or in the future to this SS50 bus structured system from **GIMIX** or other SS50 bus compatible manufacturers. **MICROWARE** has other OS9 software such as the Stylograph Screen-Oriented Word Processor available now, and in the future will be announcing other languages and utilities that run under OS9. And coming soon from **MICROWARE** will be OS9 Level 2 that lets you address up to 1 megabyte of memory.

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DAS Allows Mixing of Single-Ended and Differential Signals

AD364 is a 16-channel, 12-bit IC data acquisition system (DAS) that allows mixing single-ended and differential signals and selecting either without hardwiring. Recently introduced by Analog Devices, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062, the DAS is packaged in two hermetic DIPs and offers true 12-bit accuracy, guaranteeing no missing codes over temperature and 20-kHz throughput rate.

The two packages include two 8-channel multiplexers, a differential amplifier, a sample/hold circuit, a latched channel address register, an input mode control, control logic, and a 12-bit A-D converter. No external components are necessary in interfacing to standard microprocessor buses such as the 6800.

Inputs may be 16 single-ended, 8 differential, or a combination of the two—eg, 4 fully differential in addition to 8 single-ended inputs. Switching between single-ended and differential signal sources is accomplished via the input mode control which imposes no penalty on throughput. The input mode control also enables the user to select the difference betweeen two single-ended inputs.

Other features include 50-μs maximum total acquisition and conversion time per channel and input voltage ranges of ± 2.5 V, ± 5.0 V, $\pm$ 10 V, 0 to 5 V, and 0 to ± 10 V. Outputs can be in either 8-bit bytes or full 12-bit words. The AD364 J and K are available for a 0 to 70 °C temperature range, and the AD364 S and T are available for a -55 to 125 °C range.

Circle 443 on Inquiry Card

Military 12-Bit ADC Specified Over −55 to 125 °C

Pin compatible with ADC85 type 12-bit analog to digital converters (ADCs), MN-ADC87 offers guaranteed performance specifications over temperature range of -55 to 125 °C. Linearity of the successive approximation device is guaranteed to be better than $\pm$ ½ LSB. Performance specifications include a

(continued on page 163)

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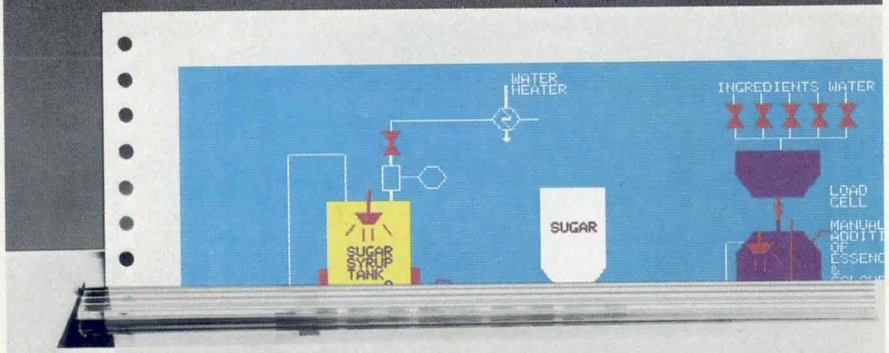

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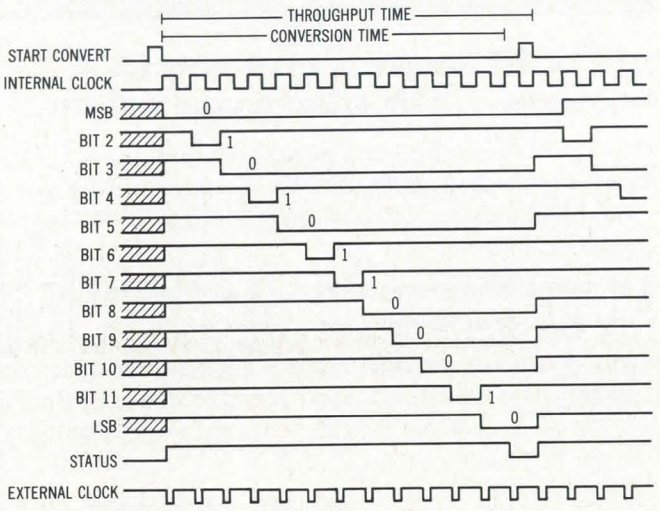

MN-ACD87 ADC timing diagram. Conversion time is width of STATUS pulse. START CONVERT command must be at least 50 ns and must remain low. Internal clock is enabled and conversion cycle begins on falling edge of START CONVERT signal. From falling edge of START CONVERT signal until STATUS rising to "1," delay may be 100 ns. Parallel data will be valid 120 ns after the STATUS output goes low

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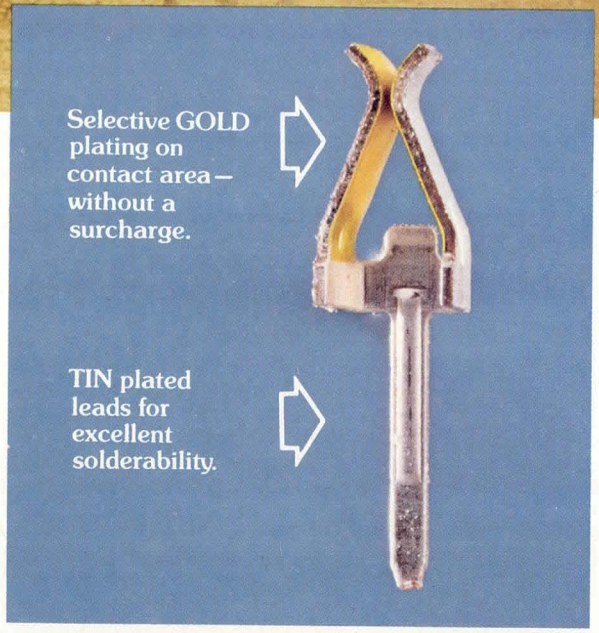

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CIRCLE 91 ON INQUIRY CARD

maximum gain drift of ±20 ppm/°C, a maximum offset drive of ±5 ppm of FSR/°C, and no missing codes over temperature.

Manufactured by Micro Networks Co, 324 Clark St, Worcester, MA 01606, the ADC has an internal clock with a guaranteed conversion time of 10 μs. There are five user selectable input ranges, serial and parallel outputs, a short cycle pin, a user optional high impedance input buffer, and pins for offset and gain adjustments.

The ADC is suited for fast data digitizing in military/aerospace applications. Its hermetically sealed ceramic 32-pin dual-inline package has favorable thermal characteristics and can withstand harsh environments. Thin film hybrid construction results in a low MTBF that is further reduced by optional MIL-STD screening.

This device is specified and tested for different applications. For the military/aerospace designer, overall unadjusted absolute accuracy specifications that apply from −55 to 125 °C are listed and tested. Gain and offset drift specifications are listed and tested for the industrial/commercial designer. The ADC is available with specifications guaranteed for either −25 to 85 °C or the military temperature range. For military/aerospace and demanding industrial applications, the device is available fully screened to the requirements of MIL-STD-883, method 5008.

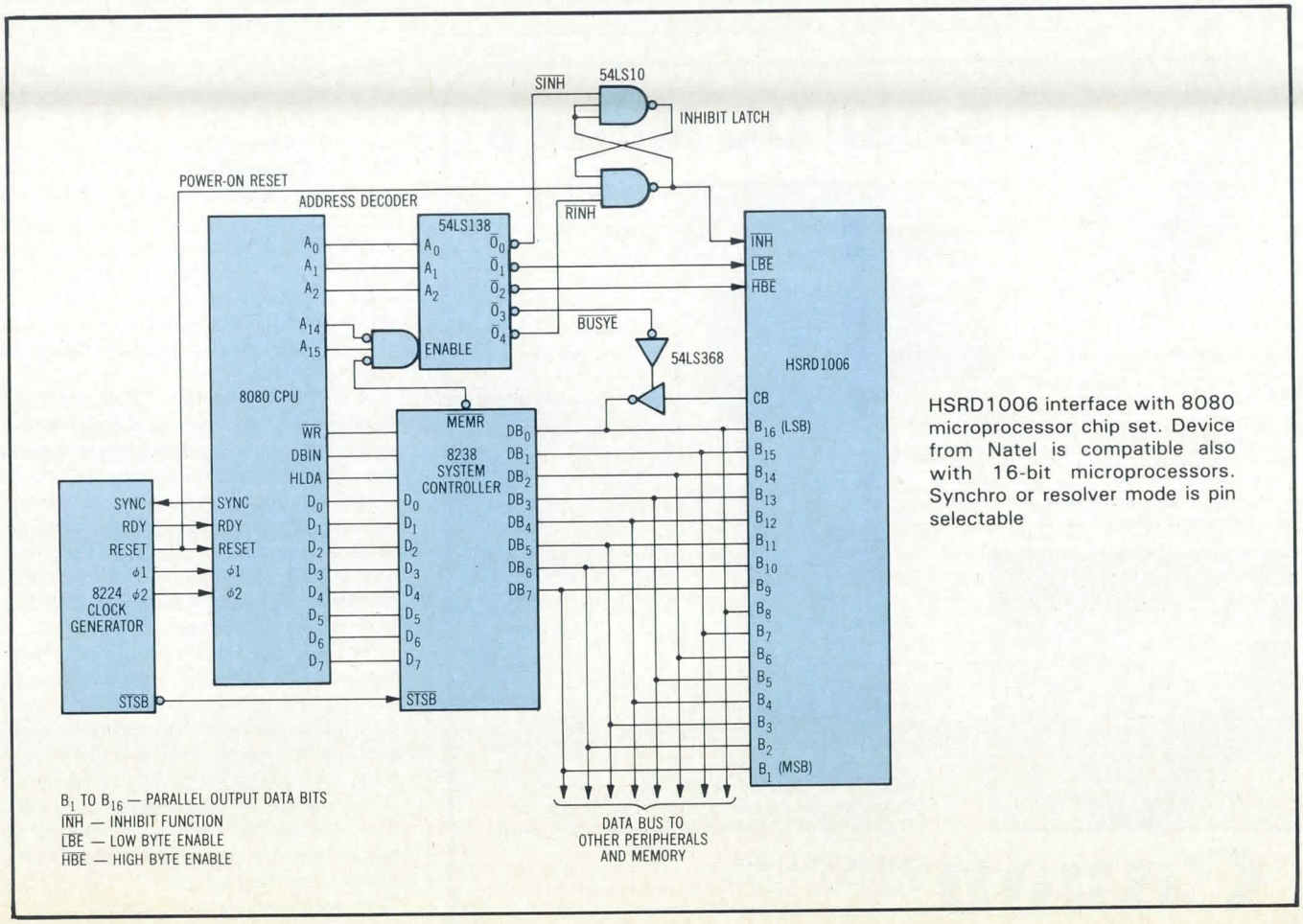
Circle 444 on Inquiry Card

16-Bit Synchro/Resolver to Digital Converter Is Microprocessor Compatible

A 16-bit synchro/resolver to digital converter, packaged in a standard 36-pin double-DIP hybrid, operates from a single 5-V power supply while consuming 20 mA. HSRD1006, from Natel Engineering Co, Inc, 8954 Mason Ave, Canoga Park, CA 91306, is compatible with 8- and 16-bit microprocessors. Selection of the synchro or resolver mode is accomplished by pin programming.

Basic accuracy is ±1.3 arc-min. A type II servo loop ensures tracking with no lag errors. To make the converter insensitive to a reference phase shift of up to ±45°, a reference synthesizer is used. Transferring data is eased through the use of a transparent latch with 3-state outputs configured as two independently enabled 8-bit bytes. This allows data to be read without interrupting converter tracking and permits memory-mapped data interface and control with 8- and 16-bit microprocessors and single-board computers. A typical interface configuration with an 8-bit microprocessor is shown in the Figure. In this example, the microprocessor applies inhibit set pulse ($\overline{SINH}$), which causes INHIBIT LATCH to set for the duration of data transfer. Test loop monitors converter busy (CB) output of converter. When CB line is detected in logic "0" condition, a 2-byte load is executed to transfer 16 bits of data into H and L registers. Since H and L registers must be used once more in order to execute the reset for INHIBIT

(continued on page 164)

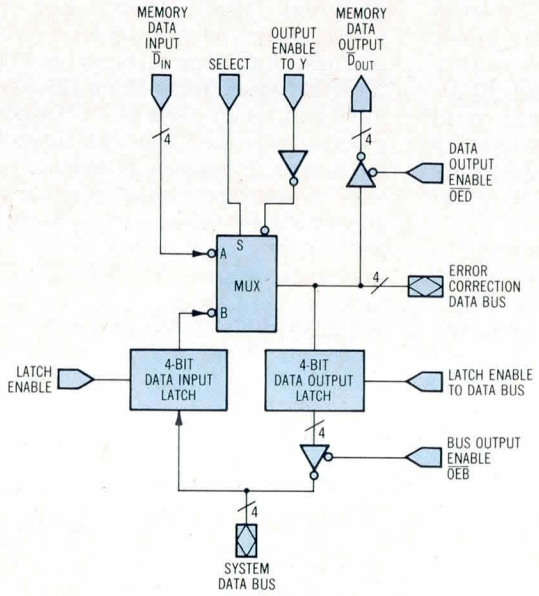


HSRD1006 interface with 8080 microprocessor chip set. Device from Natel is compatible also with 16-bit microprocessors. Synchro or resolver mode is pin selectable

LATCH ($\overline{RINH}$), XCHG instruction is executed to transfer 16 data bits of D and E registers. INHIBIT LATCH is then reset and a subroutine returns execution to the calling program. Logic inputs and outputs are TTL and CMOS compatible. Digital data outputs can drive one 54/74 gate load or four 54LS/74LS gate loads.

A built-in test feature provides a logic "1" when the tracking error exceeds ±1°. Analog signals that correspond to converter tracking velocity and instantaneous tracking error facilitate the monitoring of converter dynamics. An automatic gain compensation circuit is incorporated into the converter design to allow signal voltage variations of 30% without degradation in accuracy or change in converter hysteresis.

Circle 445 on Inquiry Card



Logic diagram of EDC multiple data bus buffer. Device features separate input and output buses for RAM, 3-state control on all buses, and bus input and output data latches with separate enables. Bus to EDC unit is bidirectional. 24 mA drive to system data bus is required

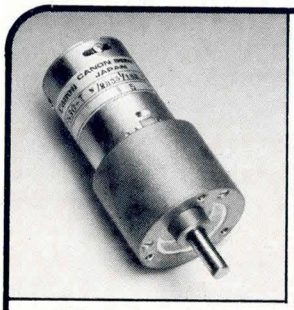
EDC Multiple Data Bus Buffers Offered

Am2961/2962 error detection and correction (EDC) multiple data bus buffers are the latest addition to the Am2960 family of memory support products from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. This family of parts also includes the Am2960 EDC, the Am2965/2966 dynamic RAM drivers, and the Am2964B dynamic memory controller. An AmZ8160 series is based on the same device designs, but with parameters characterized for AmZ8000 microcomputer systems. The Am2961/2962 will also be available as the AmZ8161/Z8162.

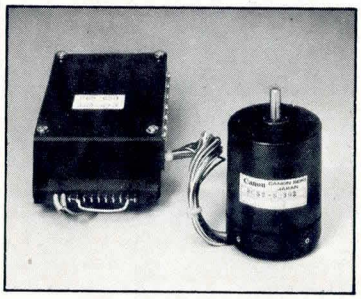
A single-chip solution to the interface between the EDC unit and the system bus and memory array, these devices exhibit the drive, bus organization, and 3-state control required by state of the art memory systems. The Am2961 provides an inverting data path between the data bus and the EDC bus. The Am2962 does not invert this path. The bus architecture is shown in the Figure.

To improve flexibility, the devices feature a 4-bit configuration in a 24-pin, 0.3″ (0.76-cm) wide package. This configuration provides an optimum compromise between byte level control capability and minimum package size. Speed is compatible with the Am2960 EDC unit. The Am2961/2962 allows expansion to match memory data widths up to 64 bits, as does the Am2960 EDC.

Circle 446 on Inquiry Card



Small DC Motors



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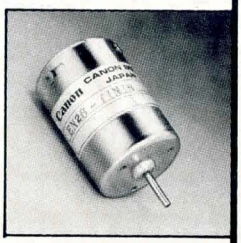

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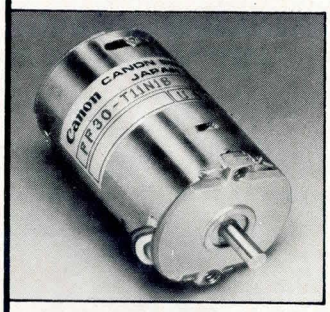

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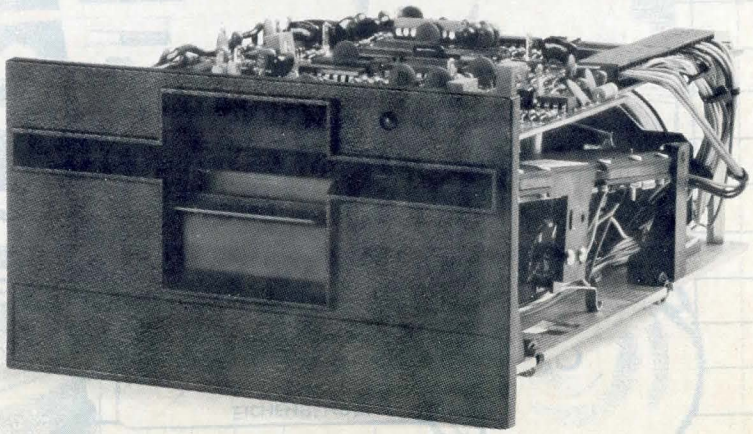
Our wide range of drives comes with a precision centering mechanism to insure accurate centering of a disk—every time (four times better than the competition). In addition, we include ceramic/ferrite double density recording heads, 10 msec track-to-track access time, stainless steel precision-ground positioning reference, and the highest quality electrical and mechanical components available. So you get high track storage capacity, fast access, lowest cost per K byte, significantly greater reliability and best of all, 3 years delivery experience of 85,000 high capacity drives.

	Maximum Capacity	# Delivered Through '79	Positioning Mechanism	Track Density	Av. Access Time (msec)
Shugart SA450	437.5K	<5,000	spiral cam	48	440
MPI B91	960K	Evaluation only	steel band and capstan	96/100	240
TEAC 50C	960K	<10,000 Mainly in Japan	steel lead screw	100	865
Micropolis 1016/1015	1,100K	60,000	steel lead screw	96/100	365

Our drive was designed from the ground up for its double density capacity, not merely redesigned from a single density unit. That's one reason we've shipped more high capacity 5¼" floppies by far than anyone else. Another is that no matter how many imitators there are, there's no substitute for the original.



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CIRCLE 93 ON INQUIRY CARD

32k Military EPROM Has Standard Power-Down Pinout

Developed for military microprocessor systems, the M2732 32k EPROM is processed to MIL-STD-883 level B. Produced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, the device operates at −55 to 100 °C with a maximum access time of 450 ns, a maximum active power of 150 mA, and a maximum standby power of 35 mA. The recently announced EPROM can replace the M2716 16k EPROM with only half its average power dissipation per kilobyte. It is claimed to be the first 32k military EPROM compatible with the new industry standard pinout for high density microprocessor memory devices. The pinout, which ensures upward compatibility with future 64k and higher density devices, conforms to the JEDEC byte-wide memory family standard.

M2732 is destined for applications in flight recorders, navigation, guidance, and weapons control systems and in program development prior to the fabrication of conventional ROMs. Application features include single 5-V power supply operation, automatic power-down, separate output enable to eliminate bus contentions, single-pulse programming, and onboard programmability. Automatic power-down reduces average power dissipation 60% to 80%. In active operation, the M2732 dissipates 750 mW. On standby, it dissipates 175 mW at 35 mA. A higher temperature version (−55 to 125 °C), the M2716M dissipates 575 mW active and 165 mW on standby. Automatic power-down control is built into the chip enable function. The chip powers down and goes on standby when deselected, and powers up when enabled.

Separate chip enable and output enable control pins are used to eliminate bus contention problems caused by differences in EPROM response times or by glitches on address lines. Two-line control is also incorporated in the JEDEC pinout standard. At chip enable time, the EPROM is selected. However, the outputs remain inactive until the output enable becomes inactive. The microprocessor controls both selection and timing of the EPROM. In M8085A, M8086 and other multiplexed bus systems, 2-line control ensures that readout cannot occur when the bus is in the address transmission mode.

Circle 447 on Inquiry Card

M2732/M2716 Military EPROM Family*

	M2732	M2732/S8416	M2716M	M2716
Temperature Range	−55 to 100 °C	−55 to 125 °C	−55 to 125 °C	−55 to 100 °C
Organization	4k x 8 bits	4k x 8 bits	2k x 8 bits	2k x 8 bits
Max Access Time	450 ns	550 ns	450 ns	450 ns
Max Standby Current	35 mA	35 mA	30 mA	30 mA
Max Active Current	150 mA	150 mA	115 mA	115 mA

*All devices conform to MIL-STD-883 level B, and operate from a 5-V (±10%) power source

64k Dynamic RAM In Double-Poly N-Channel Silicon Gate Technology

Organized as 65,536 words by 1 bit, a TTL compatible dynamic RAM has been implemented in double-poly N-channel silicon gate technology for low power consumption. Packaged in a 16-pin ceramic DIP by Toshiba America, Inc, Memory and Microcomputer Products Div, 2151 Michelson Dr, Suite 190, Irvine, CA 92715, TMM4164C is available in three versions. TMM4164C-2 has a 120-ns access time and 250-ns cycle time, -3 has a 150-ns access time and 320-ns cycle time, and -4 accesses in 200 ns and requires 330 ns per cycle.

All versions use a single 5-V power supply with a maximum standby of 27.5 mW. The device has common I/O capability using "early write" operation, and features read/modify/write, RAS-only refresh, pin 1 no-connect, and page mode capability. Two-dimensional chip selection is made possible by output unlatching at cycle end.

Circle 455 on Inquiry Card.

Monolithic Video Speed ADCs Fabricated Using Bipolar ECL Technology

SP 9752 2-bit and SP 9754 4-bit analog to digital converters (ADCs) are suitable for implementing high speed, 100-MHz or higher, wideband signal processing circuits. The ADCs, from Plessey Semiconductors, 1641 Kaiser Ave, Irvine, CA 92714, complement the company's signal conversion IC family that includes the recently announced 300-MHz SP 9768 DAC. Both devices are fabricated using high performance, bipolar ECL technology. Units provide "carry" nodes for driving larger systems of unlimited resolution.

Internally, the ADCs operate on a master/slave principle that eliminates the need for external sample/hold circuits. Following the alternating high and low levels of an external clock, onchip comparators first track and encode the input's analog level, then latch it onto a binary word of equivalent weight. Data output pins can be wire-ORed into an ordinary data bus. Bit expansion is accomplished by carry-in and carry-out pins.

Circle 448 on Inquiry Card

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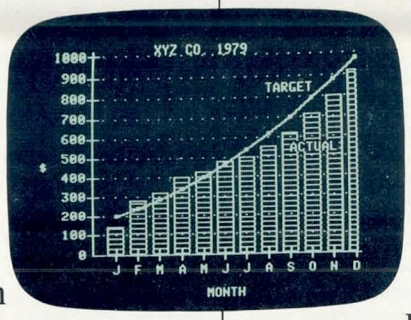

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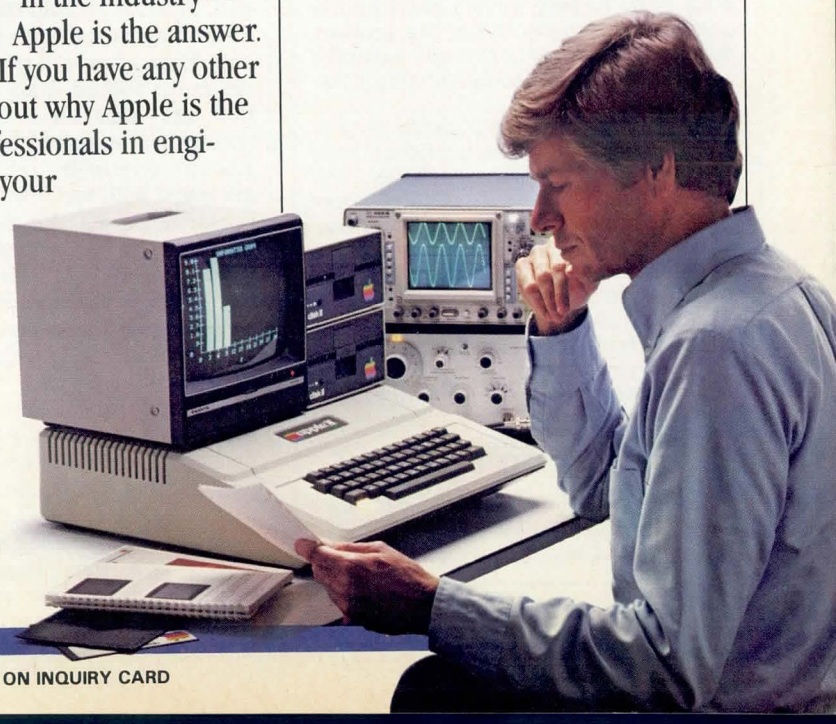
	Apple II	Apple III
Maximum Memory Size	64K bytes	128K bytes
Screen Display	40 column (80 column with peripheral card) 24 Lines Upper Case	80 column 24 Lines Upper Case/Lower Case
Screen Resolution (B&W)	280 x 192	560 x 192
Screen Resolution (Color)	140 x 192 (6 colors)	280 x 192 (16 colors)
Keyboard	Fixed	Programmable
Numeric Key Pad	Accessory	Built-in
Input/Output	8 expansion slots	4 expansion slots plus built-in: disk interface RS-232 interface Silentype™ printer interface
Disk Drives	Add-on one to six drives	One drive built-in, plus interface to support three more drives
Languages	BASIC Fortran 77 Pascal Assembly Pilot	Enhanced BASIC Fortran 77 Pascal Assembly
Typical Configuration Pricing	CPU, 48K RAM, single disk drive, B&W Monitor (9"), Silentype™ printer, and BASIC. **$3250.00***	CPU, 96K RAM, integrated disk drive, B&W Monitor (12"), Silentype™ printer, SOS, Enhanced BASIC. **$4865.00***

*Suggested retail price.

apple computer inc.



CIRCLE 94 ON INQUIRY CARD

NMOS and CMOS 128k-Bit ROMs Developed

Two 128k-bit ROMs, a NMOS and a CMOS, have been announced by NEC Microcomputers Inc, 173 Worcester St, Wellesley, MA 02181. Designated μPD23128, the NMOS ROM will be manufactured using 3-μm design rules and will have a 250-ns access time. The clocked device has a standby mode that enables the maximum power of 275 mW to be reduced to 82.5 mW. It is targeted for applications that require large memory storage, such as computer terminals, communication control equipment, electronic translators and voice synthesis. The μPD23128 NMOS device is packaged in a 28-pin package using JEDEC version B pinout.

In addition, the company announced a CMOS 128k-bit ROM, the μPD73128. This 5-V device will be packaged in a 52-pin flat package and is designed for low power consumption applications such as language translators. The μPD73128 will have a 4-ms access time and will require 30 mW maximum.

Circle 449 on Inquiry Card

FREE 48-Page Catalog

A new, free 48-page catalog is free from Creative Computing and Peripherals Plus. To help buyers make intelligent purchasing decisions, the product descriptions are exceptionally comprehensive and include screen photos in the software section.

The catalog describes 20 books on programming, games, and educational applications; 160 software packages for Apple, Atari, TRS-80, PET, CP/M, TI, Sorcerer and Sol computers; 3 magazines (*Creative Computing*, *Microsystems*, and *SYNC*); 5 graphics and music peripherals; an LP record; board game; 8 T-shirts and an eclectic assortment of other products for the personal computer user.

To get your free copy, simply drop a card or note to the address below.

creative computing

Attn: Adele
39 East Hanover Avenue
Morris Plains, NJ 07960

Power Monitor and Time of Day Clock Improve System Reliability

Recently announced power monitor and time of day clock micromodules from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, have been developed to improve system reliability. They include the M68MM10A (power monitor), the M68MM10B (power monitor plus battery backup realtime clock/calendar with RAM), the M68MM10C (time of day clock and RAM). The A and B versions provide the sequence of power-up and power-down signals required for systems that use nonvolatile memory, eg, battery backed up RAM. These micromodules monitor ac line voltage, and detect either an abrupt power loss or a low voltage brownout condition. The abrupt power loss is detected after 2.0 ms of no line voltage. The brownout condition is detected when the input line voltage drops below a user selected value.

Power-down begins with an NMI pulse as soon as a power-fail is detected. Through user written software, required data can be stored in nonvariable memory. After a variable jumper selectable save period, a PWRFAIL signal is generated to inhibit writes into the protected memory. The length of the save period depends upon the load on the power supply which affects its hold-up time. RESET is generated simultaneously with PWRFAIL to hold the processor and all resettable I/O devices in a reset condition. The system will remain in this condition for 500 ms. Upon power restoration and after the 500 ms wait, the power-up sequence begins. First a jumper selectable restore period is generated with NMI, PWRFAIL and RESET released. During this period, a subsequent power-fail sequence will not be initiated, allowing the software to restore the system to normal operation. Following this delay period, any power-fail condition will again reinitiate the power-down squence.

The optional C version with a CMOS time of day clock and RAM with battery backup provide a number of additional features that are required in many applications. The software settable/readable calendar and time of day clock allow time tagging data and events. Realtime tasks can be initiated by the hour-minute-second alarm conditions or by software selectable periodic interrupts from 30.52 μs to 500 ms. A 64-byte CMOS RAM is included in the chip. Fourteen bytes are used for the clock function, and 50 bytes are available for storing user data. This RAM is write protected by the PWRFAIL signal.

Circle 450 on Inquiry Card

N-Channel MNOS EAROM Meets Small Memory Needs

Aimed at microcomputer applications which require a small memory, ease of use and speed, the ER4201 EAROM is organized 128 x 8. The N-channel MNOS device features 5-V operation in the read mode and a maximum access time of 350 ns. From the Microelectronics Div of General Instrument Corp, 600 W John St, Hicksville, NY 11802, the EAROM includes incircuit electrical word alterability and onboard address, mode and data latching.

Single operation reprogramming via a Program command will place the chip in the Busy mode and initiate an automatic erase followed by a write. This capability, along with the onboard latching, allows the processor and system bus to be freed completely during the EAROM's 10-ms reprogramming operation. Nonvolatile data retention is estimated to be ten years.

Circle 451 on Inquiry Card

Read/Write IC Developed for 8″ and 5.25″ Winchesters

Silicon Systems Inc, 14351 Myford Rd, Tustin, CA 92680, recently introduced the SSI 115 5-channel read/write IC for use with 8″ and 5.25″ Winchester disc drive magnetic recording heads. The device is an extension of the company's product line for the 3350 Winchester plug compatible marketplace, and it offers improved performance and simplified interfacing with drive electronics.

The device operates with center tapped recording heads and provides five channels of read/write electronics, TTL compatible logic control, and data protection. Each channel contains a differential write current switch, a high gain low noise read amplifier, and write safety circuits. Typically the device replaces a discrete component implementation requiring 10 in² (64.5 cm²) or more of printed circuit board space.

Circle 452 on Inquiry Card

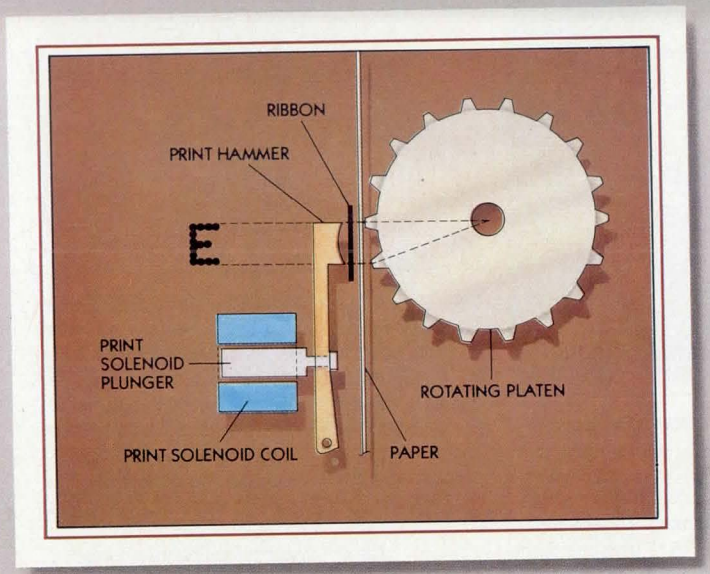
INTRODUCING A REVOLUTIONARY DOT MATRIX PRINTER WITH JUST ONE HAMMER. AT AN INCREDIBLE PRICE – JUST $399.

The Uni-Hammer Replaces Seven... or More.

Revolutionary? We don't know what else to call it. An impact printer with a single rugged hammer, rather than the seven or more individual solenoids and print wires found in conventional dot matrix printers.

At an incredible unit price of $399!

Because of the unique Uni-Hammer design, the GP-80M is smaller and simpler than other dot matrix printers yet costs considerably less. Which makes it a natural for OEMs needing compact, reliable, low cost printers for system use, and also for the personal or small business user who wants a quality impact printer at the lowest possible price.



How the Uni-Hammer Works

The GP-80M, which prints both graphics and alphanumerics, uses a rotating platen with protruding splines positioned behind the paper (see diagram). The character or graphics image is created by multiple hammer strikes in rapid succession as the print head advances across the paper. The precision gear train assures exact positioning of the print hammer relative to the splines on the platen, to provide excellent print quality.

A Complete Printer

The GP-80M has features comparable to printers selling for thousands of dollars. These include upper/lower ASCII character sets, ribbon cartridge, 80 columns at 12 characters per inch, adjustable tractor feed, original and 2 copies, 30 characters per second, and full graphics with a resolution of better than 60 dots per inch in both horizontal and vertical axes.

Plenty of Interfaces

Interfaces include Centronics parallel, RS232C, serial TTL, 20mA current loop, IEEE-488, Apple, TRS-80, PET, HP-85... and more.

See the GP-80M in action at your local computer store, or write for the distributor in your area.

A Product of the Seiko Group

The GP-80M is manufactured by Seikosha and exclusively distributed in the USA by Axiom. It took a company such as the Seiko group, world's largest watch manufacturer, with vast experience in the design of small, intricate, precision products, to come up with a totally new concept in dot matrix printing.

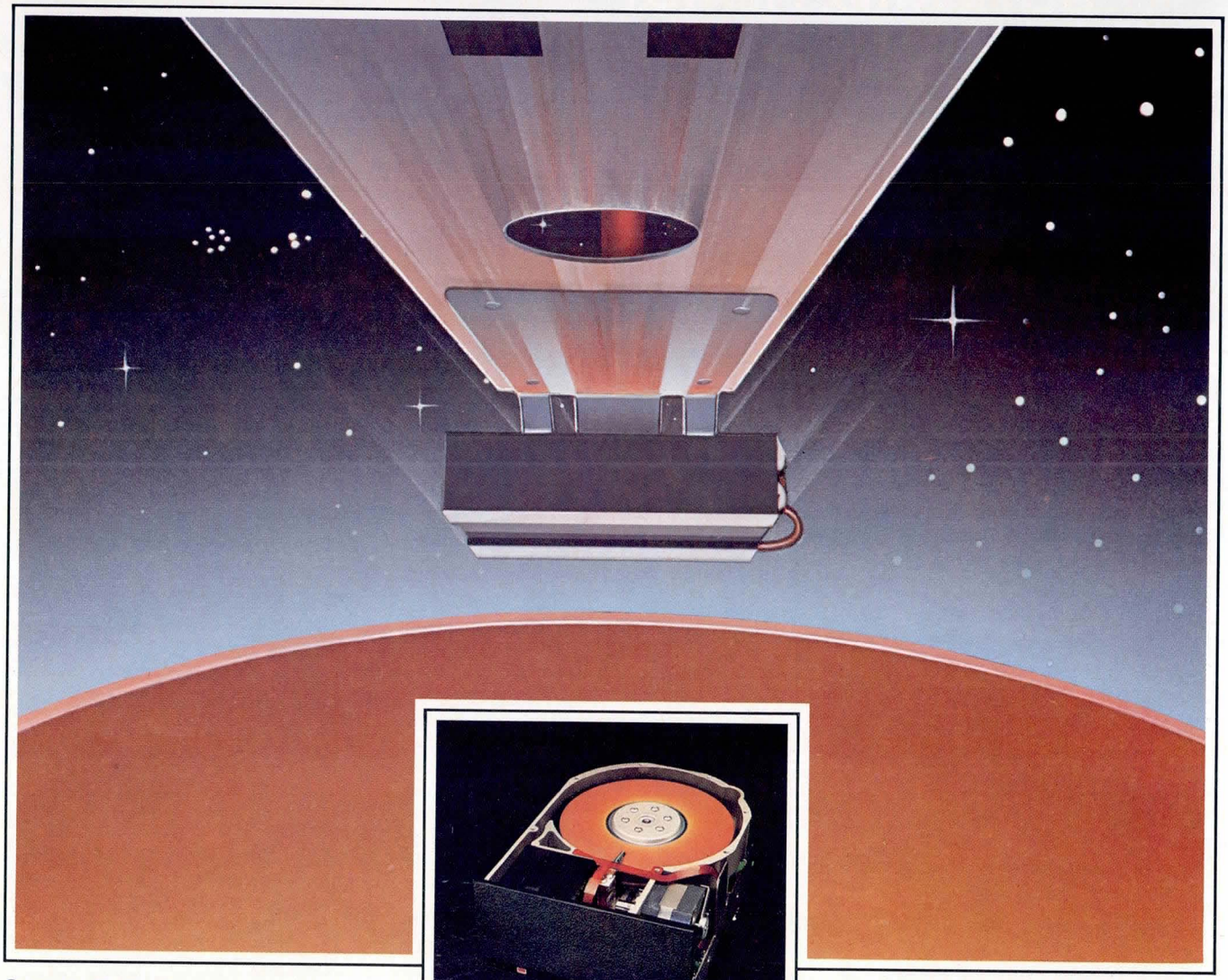
AXIOM

AXIOM CORPORATION

1014 Griswold Avenue • San Fernando, CA 91340
Telephone: (213) 365-9521 • TWX: 910-496-1746

CIRCLE 95 ON INQUIRY CARD

Thin is in!



Seagate Technology announces another first. The inventor of the 5¼-inch micro-Winchester™ now brings you thin film heads and 12.76 megabytes on just two platters—double the capacity of current ferrite head drives.

The new ST512 micro-Winchester with thin film heads stores 10202 bits per inch and doubles the number of tracks from 612 to 1224. Increased bit packing permits recording closer to the disc center and eliminates the need for write precompensation.

No change in form factor or interfacing. The ST512 doubles storage capacity without changing your system configuration. Size and shape exactly match Minifloppy and ST506 micro-Winchester. Just as important, the ST512 uses the same recording format, 5 MBits/sec. data transfer rate and DC voltages. You can use the same interface and power supply.

Think what ST512 could do for your system. Perform interactive, on-line jobs without being disc limited. Offer faster random access to inventories and other long listings. Run prompt-driven tutorials and other large disc-based programs. Share storage resources in local networks. Serve faster 16 and 32-bit machines. In short, provide faster access to more storage in less space.

For complete specifications, circle our readers' service number. To order an evaluation unit, write, telex or phone.

Seagate Technology

360 El Pueblo Road Scotts Valley, California 95066 (408) 438-6550 TELEX 172114 SCVL
East Coast Sales Office: P.O. Box 137 Allamuchy, New Jersey 07820 (201) 852-6184

"Turning the tide in fixed disc technology"

™micro-Winchester is a trademark of Seagate Technology

CIRCLE 96 ON INQUIRY CARD

IC LOOP

BRIEFS

4k x 8 Quasi-Static RAM Performs and Controls Its Own Refresh—A 4k x 8 quasi-static, self-refreshing RAM acts effectively as a static RAM. Available from Zilog Inc, 10340 Bubb Rd, Cupertino, CA 95014, the Z6132 NMOS device is organized into 4096 8-bit words. Combining static RAM convenience with the high density and low power consumption normally associated with a dynamic RAM, the device eliminates the need for external refresh circuitry through a transparent self-refreshing function that meets the refresh time requirement of dynamic memory cells.

Because of the extensive use of dynamic circuits, the RAM consumes one-sixteenth the power that a 2114 type static RAM requires for an equivalent function. Application flexibility is permitted by a choice of 250-, 300-, and 350-ns access times, with further speed enhancements planned for the future. Separate pins are used for addresses and bidirectional data input/output.

Z6132 is available in a 28-pin plastic, ceramic or cerDIP dual-inline package. It operates from a single 5-V supply with a ±5% tolerance, and conforms to the Z-BUS™ specification used by the Z8000™ microprocessor and Z8™ single-chip microcomputer families.

Circle 453 on Inquiry Card

Intelligent-Positioning Stepper Motor Controller Introduced—Serving as an intelligent interface between a keyboard or microprocessor system and a 4-phase stepper motor, the CY512 intelligent positioning stepper motor controller is user programmable and accepts either ASCII decimal high level language commands and data or binary commands and data. The NMOS device can either store a command sequence as a program for later execution or accept individual commands for immediate execution.

From Cybernetic Micro Systems, 445-203 S San Antonio Rd, Los Altos, CA 94022, the chip provides ramped step rate capability in both absolute and relative position modes and has direction finding capability in the absolute mode. The 40-pin LSI device has 21 high level, function oriented instructions that are easily called up by single-letter labels such as 'P' for position, 'S' for slope, and 'R' for rate.

Circle 454 on Inquiry Card

GOOD CRT'S COME IN SMALL PACKAGES

Who says a CRT terminal has to be big and bulky to do a good job? At Ann Arbor Terminals, we offer a full 15-inch screen *and* detached keyboard as standard on all our desktop terminals. And the case is only 14" wide by 15" high by 13.6" deep. We're known throughout the industry for our high quality and reliability. On top of this, we probably have the widest range of available options in the field. Display formats from 256 to 4800 characters. Foreign language character sets. Special command sets. Custom keyboards. Editing, protected fields and block transmit.

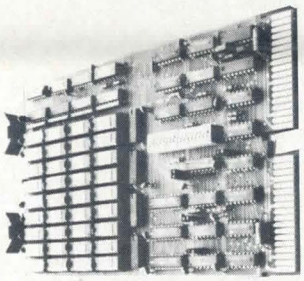
And if your application doesn't lend itself to a desktop terminal, we offer display controllers (especially good in industrial environments) for use with free-standing monitors. Or buy our terminal without the case and mount it in your own console.

So when the CRT is the focal point of your system, why settle for a large case and small screen? You can have excellent readability without taking up a lot of room. And get the features you need. Call us for more information at Ann Arbor Terminals, Inc., 6175 Jackson Road, Ann Arbor, Michigan 48103. Tel: (313)663-8000. TWX: 810-223-6033.

ANN ARBOR TERMINALS, INC

CIRCLE 97 ON INQUIRY CARD

STATE OF THE ART MEMORY SYSTEMS



256KB LSI 11/23® SINGLE DUAL WIDTH BOARD
The First and Only 256KB Memory on a Single Dual Board.

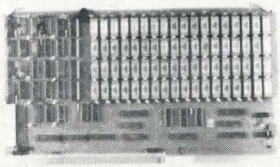
4 MEGABYTE ADDRESS FIELD — Most memories available for the DEC PDP 11/23 are only addressable to 256K bytes (18 address lines). The CI-1123 is addressable to 4 mega bytes (22 address lines) so there is no need to worry about obsolescence.

FAST ACCESS AND CYCLE TIME — With an access time of 270 NSEC and cycle time of 400 NSEC one is insured the best throughput on the PDP 11/23 system.

PARITY — The CI-1123 generates and checks parity for each byte of memory. Totally DEC compatible.

BATTERY BACKUP POWER CONSUMPTION — Power requirement for the module is only 1.2 AMP from the 5 volt supply. The CI-1123 is easily configured for battery back-up mode of operation requiring only 300MA from a single 5 V back-up supply for 256KB memory in the down state.

SINGLE QTY. PRICE: 32K x 18 **$575.** 128K x 18 **$1925**



512KB SINGLE BOARD MULTIBUS® MEMORY
State of the Art Multibus Memory Design.
First to Offer 512KB on One Board.

The CI-8086 module is compatible with both 8 or 16 bit Multibus Systems.

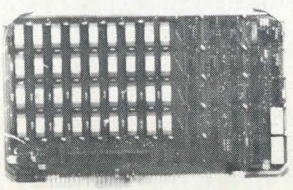
PARITY — The CI-8086 generates and checks even parity with selectable interrupt on parity error.

FAST ACCESS AND CYCLE TIME — Data access is 250 NSEC and cycle time is 375 NSEC.

16 MEGA BYTE ADDRESSING — The memory is addressable in 16K increments up to 16 mega bytes.

LOW POWER CONSUMPTION — Total power consumption is under 8 watts.

SINGLE QTY. PRICE: 128K x 9 **$1350.** 512K x 9 **$2995.**



64K x 9 EXORCISER® I SINGLE BOARD MEMORY
For Exorciser I, Exorciser II and Rockwell System 65.

FAST ACCESS AND CYCLE TIME — Data access time is 225 NSEC and cycle time is 400 NSEC, allowing the unit to work as a static RAM at clock rates in excess of 1.5 mega hertz. For 2 mega hertz operation the board can be easily configured to utilize a cycle stealing refresh operation.

ADDRESSING — On-board memory select is available in 4K increments up to 64K words of memory on either the VUA or VXA control inputs.

PARITY — On board even parity with output jumper select to the system bus as a parity error or non-maskable interrupt.

Complete board power consumption is under 7 watts.

SINGLE QTY. PRICE: 64K x 9 **$575.**

Tested and burned-in. Full year warranty.

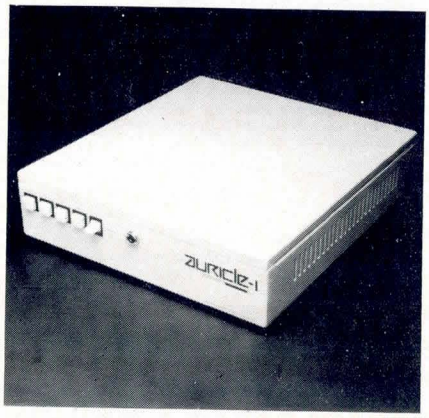
Chrislin Industries, Inc.

31312 Via Colinas · Westlake Village, CA 91361 · 213-991-2254

Multibus is a trademark of the Intel Corp. LSI 11 is a trademark of Digital Equipment Corp. EXORciser is a trademark of Motorola

CIRCLE 98 ON INQUIRY CARD

Low cost system familiarizes OEM designers with speech recognition capabilities



General structure of Auricle-I speech recognition system. Speech input is analyzed for energy content in each of 16 frequency bands, followed by data compression to reduce processing and memory requirements. Final step is utterance recognition, in which filtered and compressed data are matched against stored patterns called templates

Electronic speech recognition capability for such diverse applications as CAD/CAM, robotics, word processing, data entry, telecommunications, EDP, inventory management, security, and personal computers is being offered to OEMs by Auricle, Inc, a subsidiary of Threshold Technology, Inc. Auricle-I, an isolated-word, standalone development system, allows OEMs to familiarize themselves with speech recognition and develop interface hardware and software before designing the speech recognition capability into their products. A low cost, compatible PC board version containing proprietary LSI signal processing circuits will be available before the end of this year for incorporation into those products.

Principles of Operation

Because isolated-word speech recognition systems understand only single words or short phrases from a limited vocabulary, they are less expensive than continuous-speech systems. Auricle-I has a vocabulary of 40 words or short phrases, considered adequate for many OEM applications. However, if needed, that vocabulary can be expanded to 128 words.

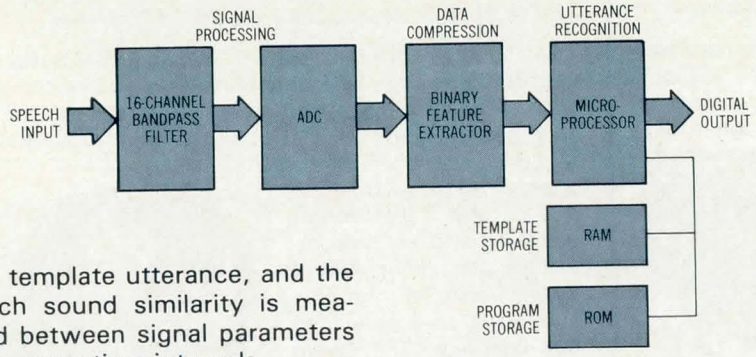
All speech recognition systems perform three basic functions: conversion of analog voice signals to digital format, compression of the digital signals in time and space to reduce processing and memory requirements, and comparison of the compressed signals to stored patterns of each word in the system's vocabulary. Signal processing removes phase from the input and analyzes and digitizes its energy content across the audio bandwidth, usually by 16- to 19-channel bandpass filtering or linear predictive coding.

Data compression in isolated-word systems is accomplished by quantizing the duration of the input word into 16 intervals, with each interval represented by 16 to 32 characteristic sounds called binary features. The input word, after compression, typically exists as a 512-bit matrix—32 bits for each of 16 time intervals. Utterance recognition consists of two sequential procedures: time alignment and comparison for speech sound similarity. Time alignment overlays both the matrices of the input word and each of the stored vocabulary/word matrices—called templates—in turn. When an input correlates well with a stored template, the system recognizes the word and outputs its code to the host system.

The Auricle-I development system (see block diagram) performs all of these actions; it receives individual spoken words or short phrases, analyzes their energy content, and compares them to patterns of vocabulary words entered by the user in a single training session. Close correlation between input and a vocabulary word determines recognition.

Signal processing is accomplished by a 16-channel bandpass filter and an analog to digital converter. In this operation, phase is removed from the speech signal but spectral power information is preserved. During the data compression stage, the data rate of digitized speech is reduced to less than approximately 2k bits/s in order to reduce the memory and processing requirements in the next stage.

For utterance recognition, beginnings and endings of utterances are detected and interior time segments are discarded. This results in contraction to a standardized length so that all utterances appear to have the same time duration. The unknown utterance is time aligned with



each template utterance, and the speech sound similarity is measured between signal parameters in the same time intervals.

To enter each vocabulary word, the user speaks it into the microphone three times. The system threshold can be defined by the user to a point that differentiates between words of similar sounds. Background noise is canceled automatically so that the system can function in noisy environments. Recognition accuracy is claimed to be better than 99%. An internal monitor program allows the user to evaluate different applications and vocabularies.

Specifications

The system is self-contained, with power supply, noise-canceling microphone, and all necessary connectors. Serial ASCII code to RS-232-C interfaces are made through a built-in DB25 connector. An IEEE-488 bus interface is optional.

Response time is 350 ms for input words of less than 1.2 s in duration. Data rate is selectable from 330 to 19.2k baud.

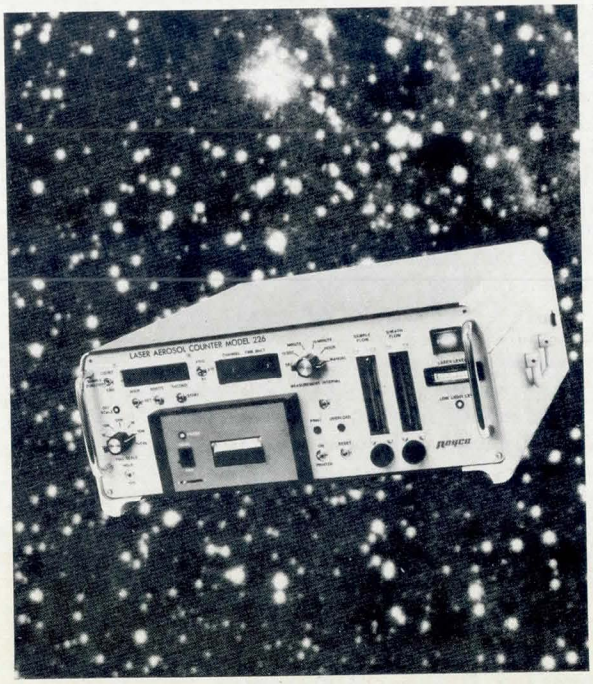
Electrical supply requirements are 115 Vac/60 Hz or 230 Vac/50 Hz. Power consumption is 9 W. The operating temperature range is 0 to 50 °C at 10% to 90% relative humidity, noncondensing. Cabinet dimensions are 3″ (7.6 cm) H x 12″ (30.5 cm) W x 13″ (33 cm) D. Weight is 4 lb (1.8 kg).

Price and Delivery

The Auricle-I development system with 40-word capability is priced at $2480. Quantity discounts are available. Delivery is 30 days ARO. Unit price for the present PC board used in the system is $695 in quantities of 1000. The LSI board, available in late 1981, will be priced at approximately $500 each, in quantities of 1000. Auricle, Inc, 20823 Stevens Creek Blvd, Cupertino, CA 95014. Tel: 408/257-9830.

For additional information circle 199 on Inquiry Card.

Monitor disk head environments for 0.1 μm particles.



The ability to monitor minute airborne particles in the sealed environment of low-flying disk drive heads is crucial to the successful development and testing of these delicate mechanisms.

Hiac/Royco comes to the rescue with individual particle counting at the 0.1 μm level, a level lower than you can get from any other manufacturer. And in our Model 226, you get it in a package that's compact and completely portable, yet highly versatile as well.

This unique laser-based instrument provides 16 accumulating memory channels with a dynamic size range from 0.1 μm up to 6 μm. Operating controls are front-panel mounted for ease of use. There's a selectable 6-digit display for channel particle counts and a built-in data printer with memory circuit.

We'd like to tell you more about our Model 226. Please call or write. 141 Jefferson Drive, Menlo Park, California 94025. Telephone (415) 325-7811.

HIAC/ROYCO
Where technology counts for excellence

INSTRUMENTS DIVISION OF PACIFIC SCIENTIFIC

Pacific Scientific Inc. Allmend Center—CH4460, Gelterkinden/Basel, Switzerland ■ 8 Cambridge Road—Brighton, Sussex BN3-1DF, England ■ Pacific Scientific GmbH Hertigstrasse 51, 7250 Leonberg -2, West Germany

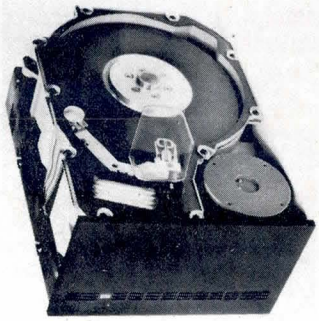
20-MHz Signature Analyzer Simplifies Troubleshooting of Microprocessor Based Units

Well suited for both field service and in plant applications, the SA-1010 allows semiskilled technicians to troubleshoot microprocessor based products down to the component level, by making simple comparisons of digital signatures. Instead of swapping boards in the field to locate a suspected problem, field engineers will use the instrument to localize the problem and replace only the board or components found defective. When the data probe is applied to a circuit node, the analyzer converts the lengthy bit stream into a 4-digit hexadecimal type display. To locate a problem, the field engineer traces through the circuit, comparing observed signatures to those identified on a schematic diagram or service manual of the product under test. When a node is reached that has a correct input signature and incorrect output signature, the problem has been isolated. For fast field check of board only, signatures can be observed at board interconnection points and compared with data using a simplified procedure. The multifamily instrument is usable with TTL, MOS, and CMOS logic circuits. For user convenience, a 1-MHz TTL clock synchronizing output is provided on the rear panel. The instrument is supplied with detachable probe assembly, control and data pods, and vinyl pouch for storage of probes and manual. **B&K Precision, Dynascan Corp,** 6460 W Cortland St, Chicago, IL 60635.

Circle 200 on Inquiry Card

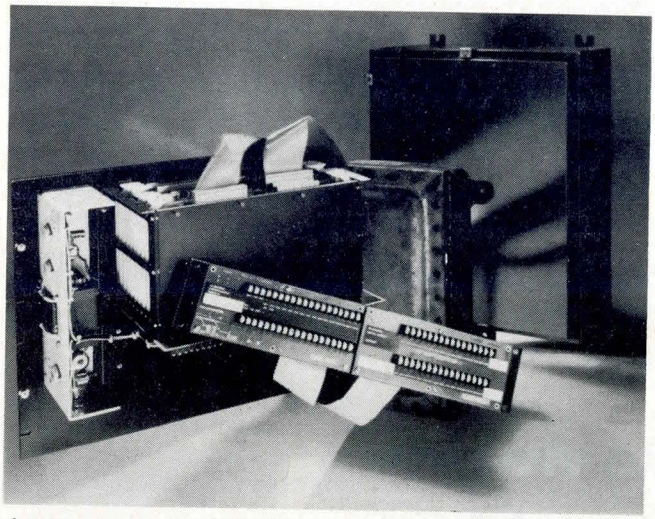
5.25″ Winchester Drives Offer Unformatted Storage for Up to 16M Bytes

CM 5000 family offers 5.3M, 10.7M, and 16M bytes of unformatted storage in a unit that is physically compatible with standard 5.25″ (13.34-cm) floppy drives. The interface has the same basic structure as that for a minifloppy and is compatible with the Seagate ST506. Offered in 1-, 2-, and 3-platter versions, the drive accomplishes positioning with a swing arm mechanism supported on 2 preloaded ball bearings. The swing arm is driven by a metal band/stepping motor actuator system. Relatively high track density (345 tracks/in or 135/cm) is achieved through the use of a high torque, high precision stepper motor coupled with an onboard microprocessor; 8650-bit/in (3405/cm) density is attributed to the use of manganese zinc heads. The electronics includes a step pulse buffer and velocity ramp profile for faster and more accurate positioning. The drive incorporates an integral spindle motor with dynamic braking. Offtrack positioning capability allows the positioner to be moved slightly off track for read margin testing, ensuring greater drive reliability. Another feature is an optional data free head landing zone. Average access time for each version is 105 ms, and average latency for the standard version is 8.3 ms. Error rates are no greater than 1 per 10^{10} bits for soft read errors, 1 per 10^{12} bits for hard read errors, and 1 per 10^{6} for seek errors. No preventive maintenance is required. **Computer Memories, Inc,** 9233 Eton Ave, Chatsworth, CA 91311.



Circle 201 on Inquiry Card

Multibus Based Data Acquisition System Provides Cost Effective Analog and Digital I/O

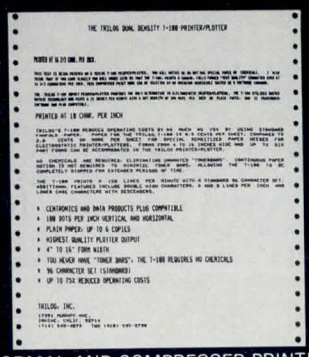


A microprocessor based data acquisition system, MCS100 provides 12-bit accuracy over industrial temperature ranges of 0 to 50 °C. The unit can be remotely located up to 1500 m using an ASCII communications path. Various analog and digital I/O cards can be used in any combination in 9 card slots. Multibus compatibility avoids a sole source situation by accommodating I/O cards from numerous manufacturers. I/O card options include 15-channel differential analog input with programmable gain, which can be extended to 63-channel input with addition of a single 48-channel expander card; 16-channel analog output card with either 4- to 20-mA or ± 10-Vdc outputs; 24-channel discrete input card optically isolated for either contact closures or voltage level inputs; and 32-channel discrete output cards with fully isolated relay contact outputs. Resident signal conditioning, in addition to programmable gain, includes thermocouple and RTD linearization, auto-zero, 0 to 100% scaling, and autoranging. Baud rates are variable in std increments from 110 to 19,200 baud. Speeds up to 300 channels/s for analog and up to 4000 channels/s for digital I/O are provided. Std ASCII communication is RS-232-C with options for adding redundant current loop, RS-422, and parallel access. Up to 15 systems can be multidropped on a single current loop highway; only CPU driver capabilities limit the number of parallel access multidropped units. Modular design allows expansion to a second card cage; 19″ (48-cm) relay rack, indoor wall mount, NEMA-4, and explosion proof packages are options. **Burr-Brown Industrial Systems Div,** PO Box 11400, Tucson, AZ 85734.

Circle 202 on Inquiry Card

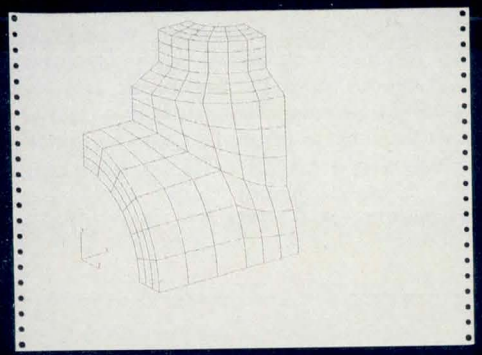
WITH TRILOG PRINTERS:

THE EXTRAS ARE FREE!

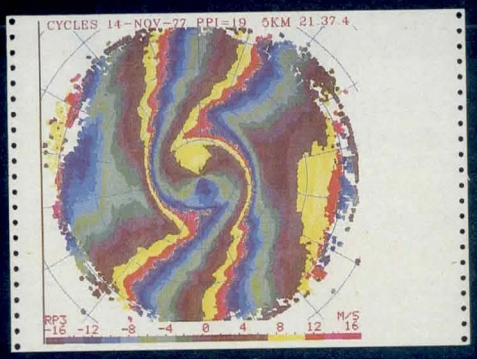


NORMAL AND COMPRESSED PRINTING

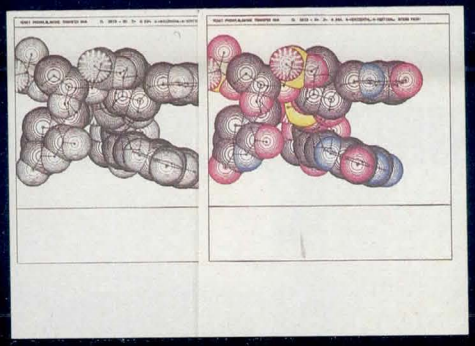
150 LPM AND 250 LPM



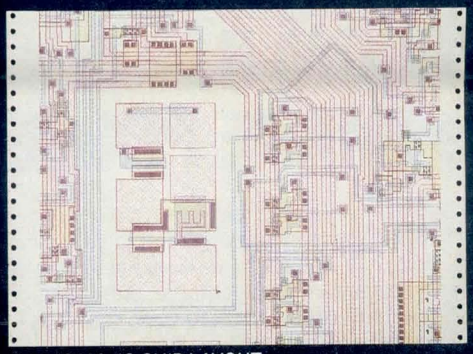
HI RES. STRESS ANALYSIS (PDA Eng.)



RADAR WEATHER MAPPING



SCIENTIFIC: MOLECULAR STRUCTURE (MIT)



CAD/CAM: IC CHIP LAYOUT (Silicon Systems Inc.)

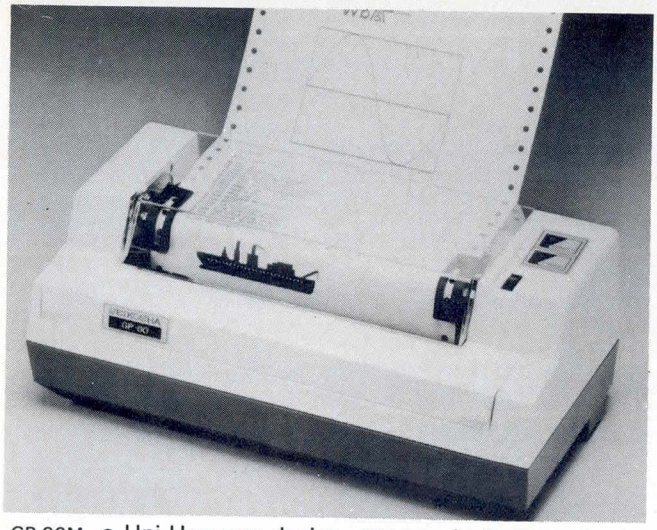
ONLY the TRILOG COLORPLOT™ line printer has all the EXTRAS — at no additional cost!!! EXTRAS such as near letter quality printing at 150 LPM, and either matrix quality printing at 250 LPM, or text quality 150 LPM compressed print at 16 2/3 CPI for printing full 132 character lines on 8 1/2 inch paper. PLUS, high resolution black and white graphics plotted on plain paper at only 1/2 cent per copy. But, that's not all...the most exciting and unique EXTRA of them all is the ability to plot high resolution FULL COLOR graphics for applications such as: CAD/CAM, Scientific, 3-d Cartography, Computer Art, and Business Charts.

COLORPLOT™ is sold and serviced through the worldwide network of TRILOG distributors. For futher information contact your local TRILOG distributor, or request the "COLORPLOT Packet" by writing or calling: TRILOG, Inc., 17391 Murphy Avenue, Irvine, CA 92714 -- (714)549-4079. TWX(910)595-2798.

TRILOG

CIRCLE 100 ON INQUIRY CARD

Reliable, Low Cost Impact Printer Uses Single Print Hammer



GP-80M, a Uni-Hammer design, uses a single rugged print hammer rather than the 7 or more individual solenoids and print wires found in conventional dot matrix printers. Printing both graphics and alphanumerics, the mechanism employs a rotating platen with protruding splines positioned behind the paper. The character or graphics image is created by multiple hammer strikes occurring in rapid succession as the printhead advances across the paper in front of the rotating platen. The precision gear train ensures exact positioning of the print hammer relative to the splines on the platen, providing excellent print quality and uniformity of the 5 x 7 dot matrix pattern. The unit's ribbon cartridge and ribbon handling mechanism eliminates the drive motors and linkages usually employed. A friction ratchet attached to the printhead advances the ribbon during the head motion return cycle. Standard features include ASCII upper- and lowercase character sets, up to 80 columns with 12 chars/in (4.7/cm), adjustable tractor feed, 3-copy reproduction, 12-W power consumption, and Centronics parallel interface. Optional interfaces include RS-232-C, serial TTL, 20-mA current loop, and IEEE 488, as well as interfaces for small computers including Apple, TRS-80, PET, HP-85, and Sharp. In addition, the std unit has full graphics capability with resolution of 60 dots/in (23.6/cm) in both horizontal and vertical axes. Dot graphics, normal characters, and double-width characters can be intermixed on a single line under software control. Measuring 5 x 12.9" (12.7 x 32.8 cm), the unit prints at 30 chars/s. **Axiom Corp,** 1014 Griswold Ave, San Fernando, CA 91340. Circle 203 on Inquiry Card

EYECOM II
the IMAGE PROCESSING PERIPHERAL

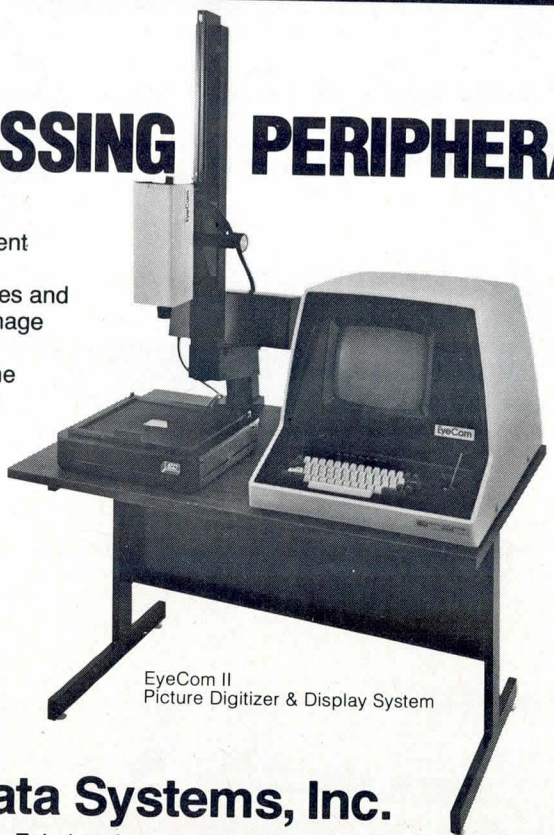
Add this image processing peripheral to your present PDP-11* or LSI-11* to measure variations in image brightness, separate image features, enhance edges and contrast, measure areas of interest, do real time image integration, and real time image differencing.

A basic software package is provided to apply the EyeCom System to your particular problem.

FEATURES:

- **Real Time Digitizing, 640x480x8-bits**
- **Add, Subtract and Convolution of images at video frame rates**
- **Joystick Cursor, 640x480 Resolution**
- **Graphic & Alphanumeric Overlay**
- **Color & Gray Scale Mapping Tables**
- **Terminal or Rack Mount Configuration**

Call or write for complete information:



EyeCom II
Picture Digitizer & Display System

Spatial Data Systems, Inc.

P.O. Box 978, 508 So. Fairview Ave., Goleta, CA 93117 • Tel: (805) 967-2383

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The Image Processing Company

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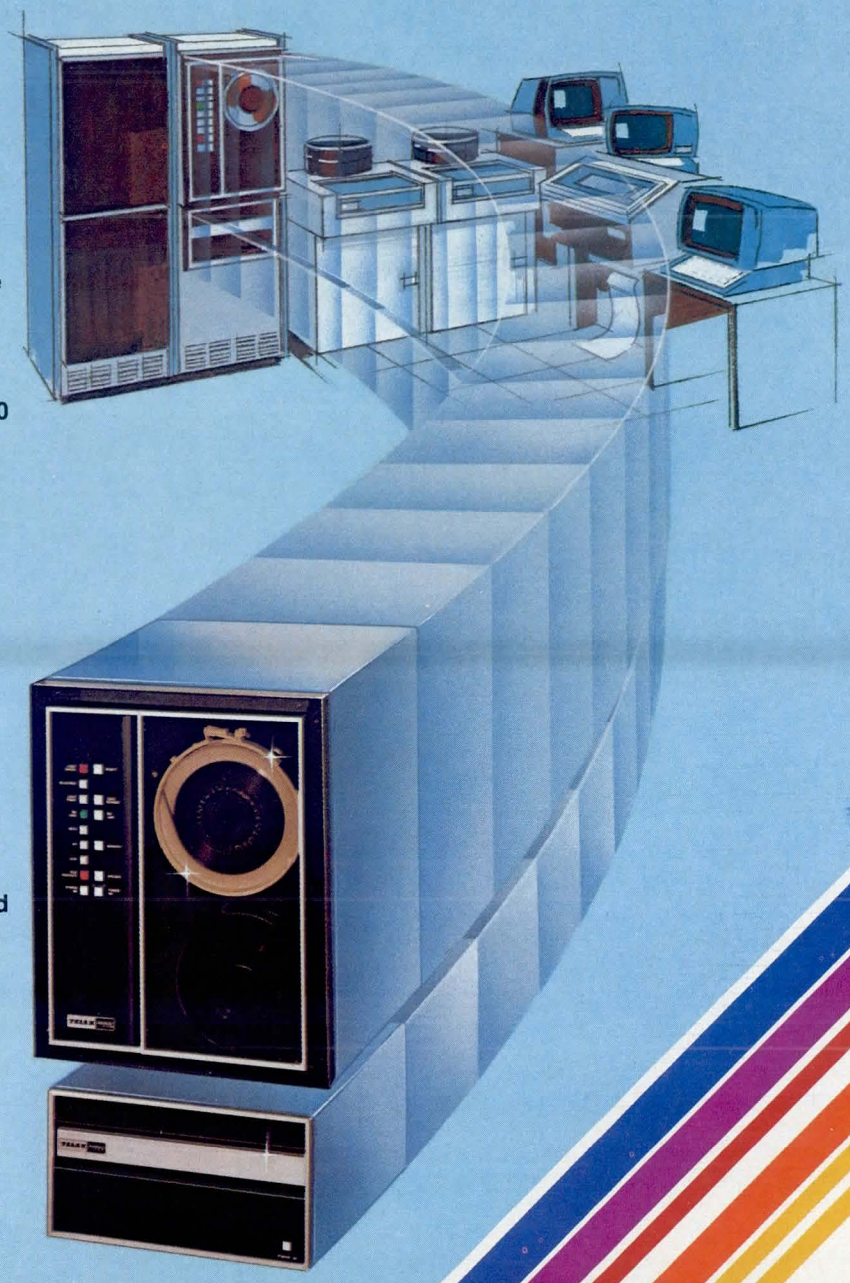
Outstanding field-proven subsystems to fit your high-performance needs.



TELEX GCR Tape Subsystems *stand out* as the most proven, high performance rack-mountable GCR units available today. Field proven in demanding seismic operation. Compatibility proven in IBM plug-compatible applications. Versatility proven in super-minicomputer environments.

Enhance your high performance computing system with high performance peripherals. Select the TELEX 6200 family. Available in 6253 (6250/1600/800 bpi), 6250 (6250/1600 bpi) and 6240 (1600/800 bpi) tape drives and tri-density 6850 formatters. Tape speeds of 50, 75 and 125-IPS available.

TELEX GCR subsystems *fit in* with your high performance computer system. Already interfaced to sixteen different CPU's. TELEX Engineering assisted with these interface developments to provide reliable operation and customized features. And we stand ready to assist you in making TELEX subsystems fit into your computer system.

With more than 2,000 units shipped — a majority for high-speed 125-IPS operation and a large number with tri-density capability — TELEX GCR offers field maturity, versatility, and integratability.

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The innovation continues... **TELEX®**

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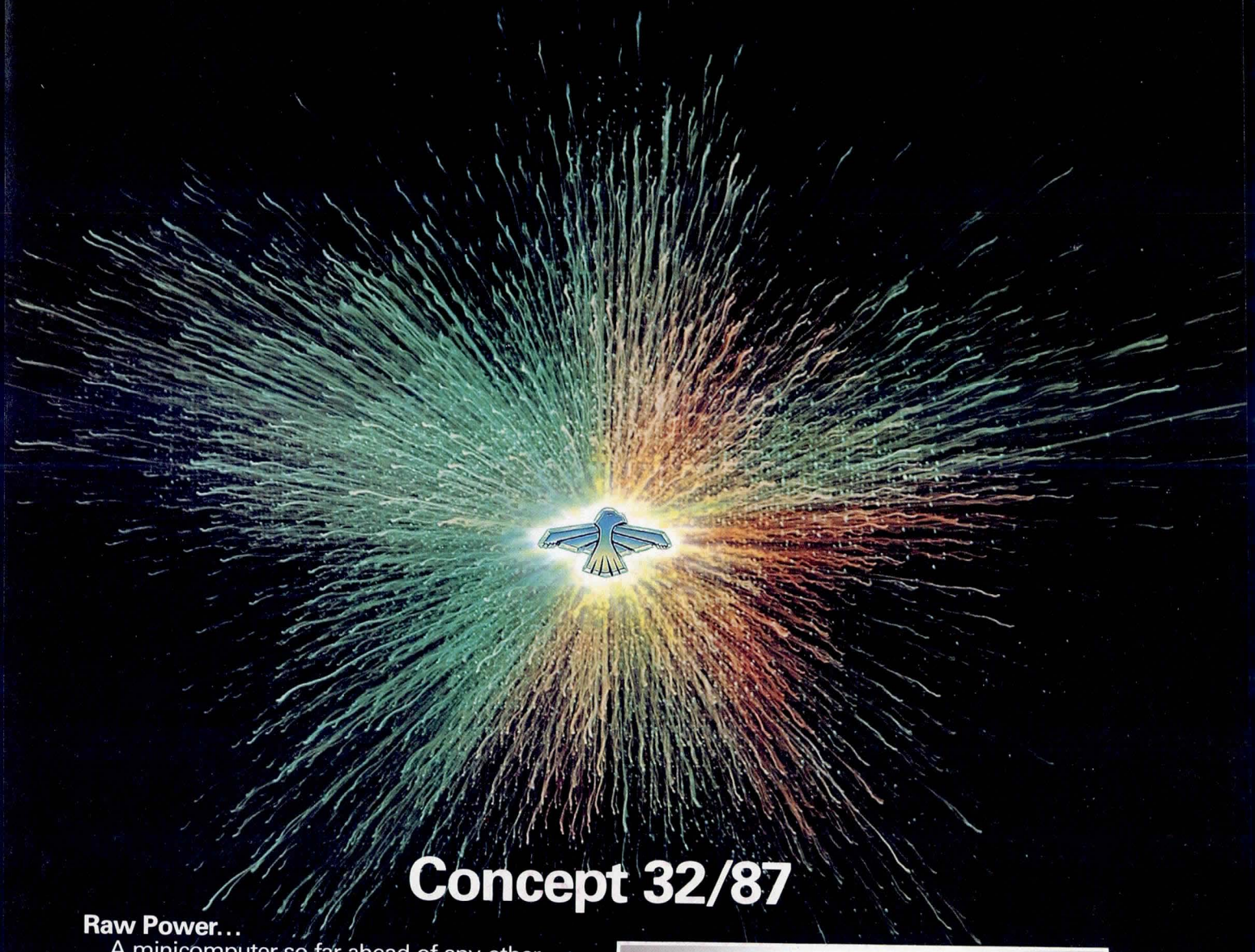
CIRCLE 102 ON INQUIRY CARD

Unleashing the most powerful minicomputer ever designed.

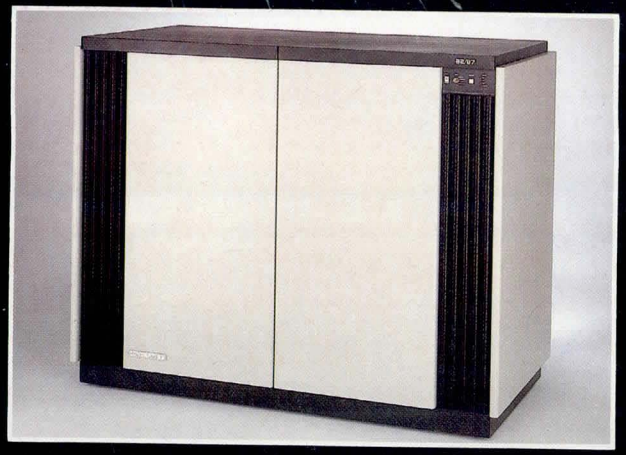


Concept 32/87

Raw Power...

A minicomputer so far ahead of any other that the numbers speak for themselves:

Whetstone 1	3604 Whets (x1000)
Whetstone 2	2249 Whets (x1000)
Real-Time Simulation	22.4 Seconds



Serious about wanting the most powerful minicomputer available? Call SYSTEMS. We'll match our numbers against anyone's.

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CIRCLE 103 ON INQUIRY CARD

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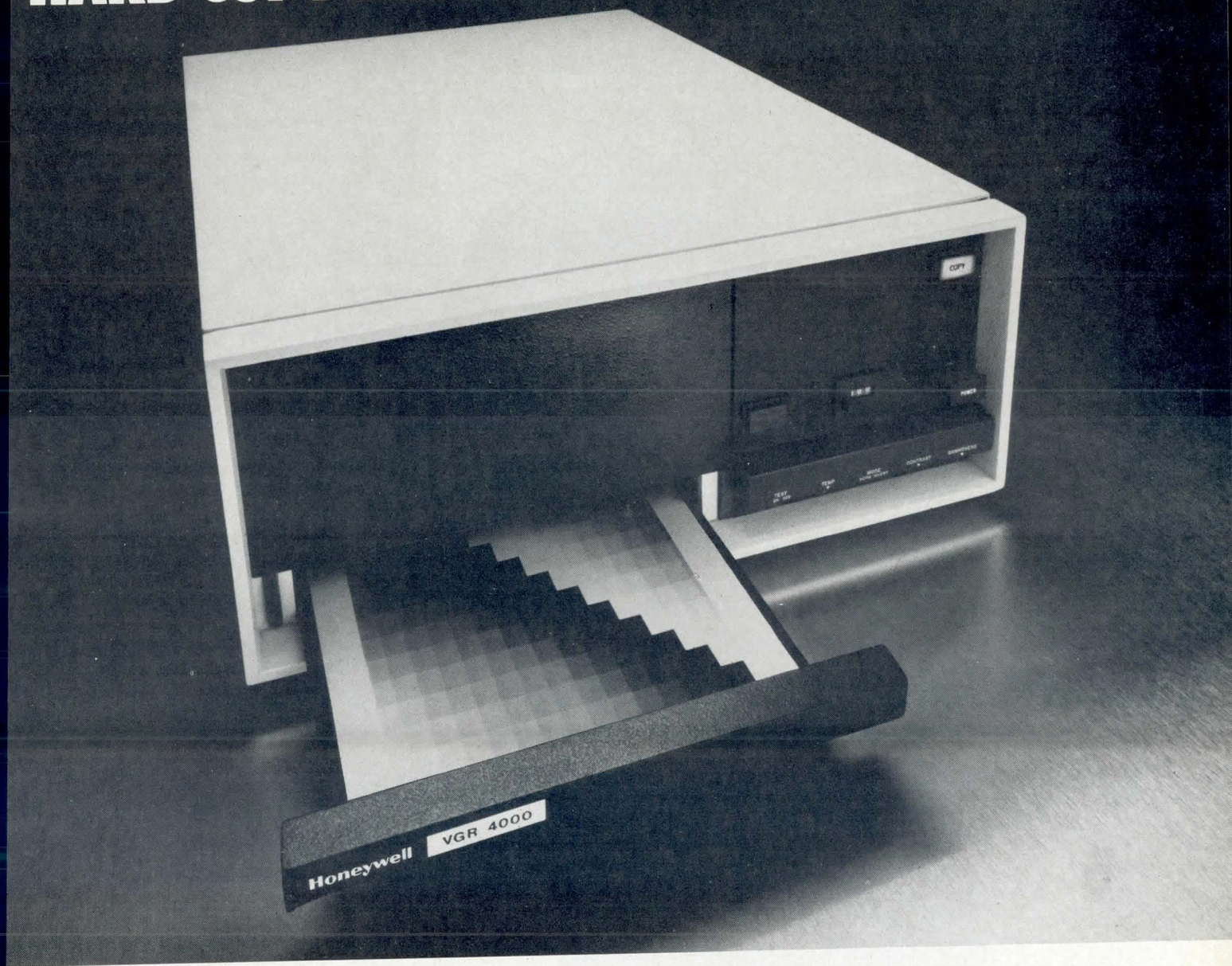
THE LATEST ADVANCE IN VIDEO GRAPHIC HARD COPY RECORDING FROM HONEYWELL



VGR 4000, Honeywell's new and advanced video graphic recorder, provides fast, crisp, 8½ x 11" hard copies on dry silver paper from most CRT's and other video sources.

White-on-black or black-on-white images are as simple as flipping a switch. With options, images can be produced having up to 16 shades of grey or even more.

An innovative processing technique eliminates the need for large heated platens. This allows the recorder to run cool, consuming very little energy.

The VGR 4000 is the only recorder on the market available with a self-contained test-pattern generator providing a choice of formats for proper copy verification.

Rugged, yet cleanly designed for easy operation, the compact VGR 4000 can be used on a desk top or rack-mounted, taking up only 7" of front panel space.

Honeywell's VGR 4000 is the latest advance in video-input hard-copy reproduction systems, built by the people with the most fiber-optic CRT recorder experience in the field.

To get the whole story on the VGR 4000 and how it can meet your needs, call Durke Johnson at 303/773-4700. Or write Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

WE'LL SHOW YOU A BETTER WAY.

Honeywell

HON-6-631

CIRCLE 104 ON INQUIRY CARD

DATA TERMINALS AND DISPLAYS

INTERACTIVE DISPLAY TERMINAL ENHANCEMENTS

Terminal status indicators, online and character set power-up, cursor key transmission, and tab improve performance of the series 510 terminal. Other added features include specified character repeat, short form cursor addressing, form feed recognition, line editing enhancements, printer port support, page data protection, display timeout and refresh, programmable page and field delimiters, editing enhancements for format mode, numeric field enhancements, APL overstrike control, added synonym valid APL overstrikes, and APL edit key. **Anderson Jacobson, Inc,** 521 Charcot Ave, San Jose, CA 95131.

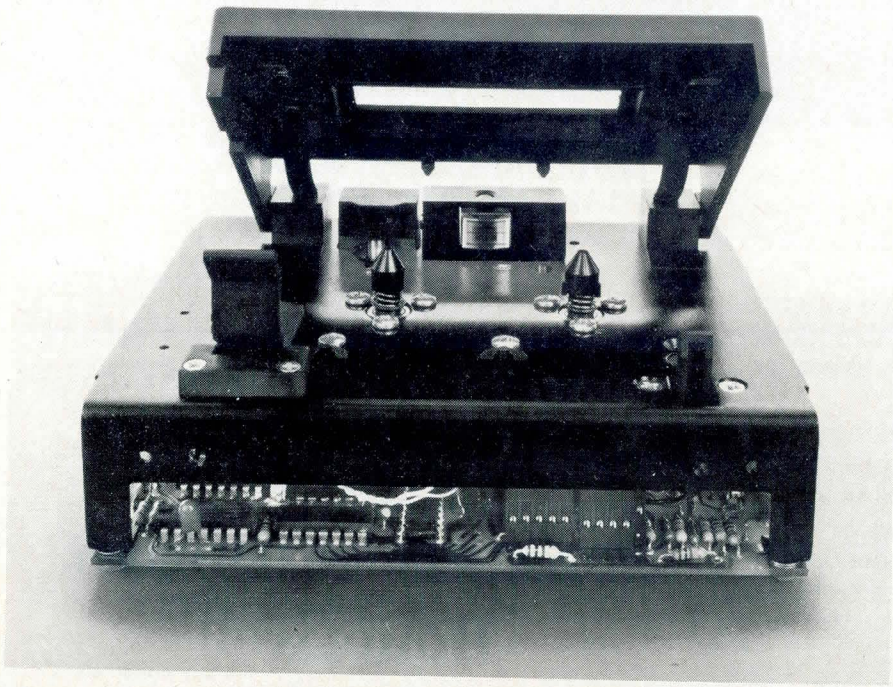
Circle 204 on Inquiry Card

132-COL DISPLAY TERMINALS

Two display terminal models, the concept 108 with 128-char u/lc ASCII and the concept APL8 with APL/ASCII and full true overstrike, offer 80/132-col display, nonvolatile storage memory, 4 to 8 pages of display memory, and a series of user-specified functional capabilities. The 132-col display uses a 5 x 9 dot matrix within a 7 x 10 dot array, while the 80-col display uses a separate character generator with a 7 x 11 dot matrix within a 10 x 12 dot array. Display memory relieves the interactive user of the burden of generating unnecessary hardcopy printouts and is allocatable between display memory and function key storage, allowing up to 28k characters for function key storage. A "create screen" function enables a user to create screen formats offline and transmit the complete format, including attributes and graphic characters, to a host computer or offline storage device. Other features include programmable function keys, multiple user-selectable character sets, I/O capability for networking between multiple communications lines, buffer overflow control for high speed operation, and self-test. **Human Designed Systems, Inc,** 3700 Market St, Philadelphia, PA 19104.

Circle 205 on Inquiry Card

WE THINK A TAPE TRANSPORT THAT ALWAYS NEEDS ADJUSTING DOESN'T HAVE ITS HEAD SCREWED ON RIGHT.



MFE's permanently aligned, one-megabyte, two-track cassette transport.

At MFE, we don't think you should have to spend time and money aligning your tape transports.

So we designed our 450 series transport so it never needs aligning. The tape head is actually bolted down to the baseplate. You can even replace our head in the field in just minutes. Without making any alignments.

You'll like MFE's new door design, too. It's extremely easy to load, and there are no linkages or complicated mechanical parts to go wrong.

And our tape handling system is so advanced it's virtually mistake-proof. Even if you accidentally eject the cassette while it's running at 120 ips, you won't damage the tape.

MFE's 450 series is available with or without a door. And it includes the 452, our one-megabyte, two-track transport that automatically reloads for the second track. We also offer the 250 series single-track transport.

If you've had enough of transports that always need adjusting, contact us.

Our head is screwed on right.

Call **800-258-3884.**

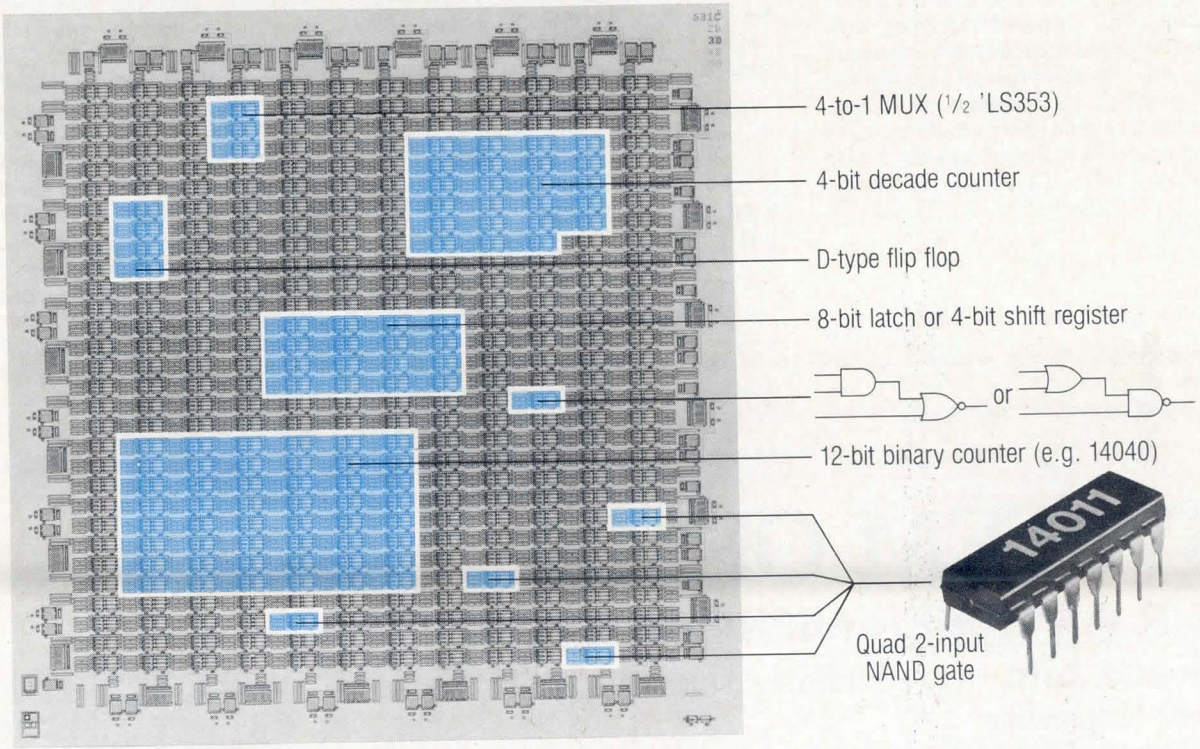
Or write MFE Corporation, Keewaydin Drive, Salem, NH 03079.

MFE

CIRCLE 105 ON INQUIRY CARD

The GarbageCollector

The little SystemChip™ for all the other stuff.



73% of the gates available left for your garbage logic.

Our small gate array chips let you compress all the miscellaneous logic garbage of your new system onto one circuit. We've got more than two dozen tried and true CMOS chips in our repertoire that give you high reliability, attractive pricing and your choice of packaging. And our in-house CAD gives you fast turnaround (how's five weeks sound?).

So if you've got the big system functions handled already with standard parts, you can leapfrog your competition with gate arrays as small as 50 gates or as big as 2240 or more. Put us to work. Send us your logic diagram for a quick confidential quote. We'll be happy to help you take out the garbage.

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Tel: (408)727-2280, TWX: 910-338-2032

DATA TERMINALS AND DISPLAYS

CRT DISPLAY TERMINALS

Terminal series 278 model 3 displays 2560 chars in 32-line x 80-col format, model 4 displays 3440 chars in 43-line x 80-col format; and model 5 displays 3564 chars in 27-line x 132-col format. Terminals attach to the company's 276 or IBM 3274/3276 control unit. Optional response time indicator measures system response from host to terminal display station and displays information on screen, outside data area. Port attachment for the model 281 message printer is also optional. **Telex Computer Products, Inc,** 6422 East 41st St, Tulsa, OK 74135.

Circle 206 on Inquiry Card

DASHER-EMULATING TERMINAL

Microprocessor based Visual 110 provides emulations of the Dasher 6052/6053 as well as 200/100 terminals and supports an ANSI mode of operation. Extensive use of nonvolatile RAM eliminates all exterior switches (except power ON/OFF); other features include smooth or jump scrolling of data on the screen, enable/disable audible keyclick for transmitted codes, selectable typamatic/nontypamatic keyboard, normal or reverse video on a screen basis, and block or underline cursor selection. **Visual Technology Inc,** Railroad Ave, Dundee Park, Andover, MA 01810.

Circle 207 on Inquiry Card

HIGH RESOLUTION CAD CRT DISPLAY

Flicker-free image resolution of substantially greater than 1000 x 1000 pixels on the RASTERGRAF™ display, offered as an option to the SIGMAGRAPHICS II CAD system, eliminates the common CAD/CAM problem of poor raster CRT resolution. Parallel processing with an onboard microprocessor for display management enables local generation of drawing details and frees the user from the time needed to reenter such data. DMA transfer rate to the display is up to 1M-bytes/s; vector drawing time is typically 3 μs/pixel. High pixel density results in circles and straight lines with no observable stair-stepping. Multiple high speed memories and multiple display storage permit storage of display parameters, selective area update, image rotation, isometric or perspective views, and zoom control up to 16x magnification. All models include an alphanumeric keyboard with 64 user-definable special function keys and a non-destructive overlay cursor controlled by an XY positioning joystick. Low persistence phosphors enable use under normal ambient room lighting. **Sigma Design West, Ltd, Graphics Products Group,** 7306 S Alton Way, Englewood, CO 80112.

Circle 208 on Inquiry Card

SYSTEM OEM'S

OUR IMPROVED MICRO MUTT . . .

takes a bite out of rising user support costs

Micro Mutt provides:

- Dial-up access to your customers' CPU's with full console privileges.
- Remote software debugging and updating.
- Remote exercising of hardware diagnostics.

This means less travel for your technical support staff. You service your customers from your own facility, at minimal cost and with immediate response to their demands.

Micro Mutt is easily installed between the CPU and console of most minicomputers, requires no modification to existing hardware or software and is loaded with performance features.

Call or write for the technical details.

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STR® technology for high data integrity. Three major tape formats for design flexibility.

We don't forget the OEM's needs.

The STR-810 digital recorder is designed for data logging, data acquisition and as a system loader. Using either the 3M DC-300A or DC-300XL cartridges, packing density is 1600 bpi, for respective data capacities of 2.3M bytes and 3.4M bytes per cartridge, using four tracks. Features include microprocessor-controlled tape movement and read/write electronics. For maximum versatility, interfaces include RS-232 and IEEE-488. Or, using control and status lines available, you can interface to specific microcomputers such as LSI-11 and 8080. EPI's optional ANSI X3.56 formatter, with NRZI or phase-encoded personality cards, turns the 810 into a plug-in component for industrial instrumentation and mini/microcomputer-interfaced peripheral markets. Price: $756 in quantities of 100. **STR-STREAM** is a high-speed, high-capacity version of the 810 designed for Winchester disc backup. Density is 6400 bpi for 17M bytes capacity per cartridge. Features include advanced head design, MFM formatting and compatibility with 8" or 14" discs.

CIRCLE 107 ON INQUIRY CARD

EPI's STR-610 is a compact, low cost digital recorder that's ideal for use with POS terminals, smart CRT terminals and as a general peripheral for mini/microcomputer-based systems. The 610's recording density is 800 bpi for a capacity of 168K bytes/track, using a two-track 3M DC-100 mini-cartridge. Formatting is ANSI Standard and interfacing is parallel, with a variety of options. Price: $280 in quantities of 1,000. **The STR-LINK III** is a high-speed (9600 baud), portable program loader that uses the STR-610's drive system and shares the same specifications. It is used as a field service tool for diagnostic work or as a peripheral in a mini/microcomputer system. STR-LINK III uses a serial RS-232 interface for data communications or data terminal applications, and it can be controlled through RS-232, ASCII control codes, or manually. Price: $1,615 in single quantity.

CIRCLE 108 ON INQUIRY CARD

STR-LINK II is EPI's proven medium-speed (1200 baud) universal portable program loader for programmable controllers and process control systems. Using a standard cassette, it features switch-selectable transmission modes for maximum flexibility. Price: $1,889 in single quantity.

For maximum design freedom, proven reliability and high data integrity through Speed Tolerant Recording technology, remember EPI—the company that doesn't forget the OEM's needs. For more information, contact Electronic Processors Inc., P.O. Box 569, Englewood, Colorado 80110. Phone (303) 761-8540.

CIRCLE 109 ON INQUIRY CARD EO/4

Let EPI remember for you.

ELECTRONIC PROCESSORS INCORPORATED

DATA TERMINALS AND DISPLAYS

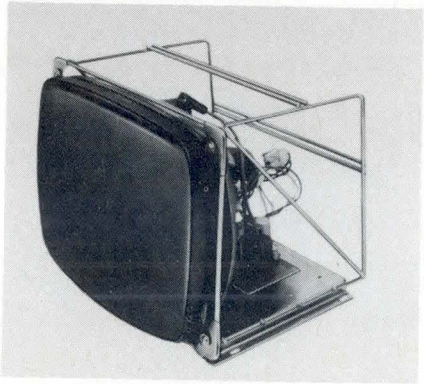
REPLACEMENT CRT TERMINAL

A replacement for Hazeltine 1500, AMD-3A, VT-52, ADDS, Soroc, Televideo, Visual Technology, and other terminals, ABM 80 features high resolution nonglare CRT screen, numeric and special function keypad, full video attributes, advanced editing, block mode, monitor mode, protected and unprotected fields, foreground and background operation, and programmable keyclick and margin bell. The 12″ (30-cm) P31 phosphor CRT has an 18-MHz bandwidth. Programmable video attribute and 128 displayable ASCII characters are provided. Characters are formed on a 7 x 9 dot matrix for upper case, 7 x 11 dot matrix for lower case. The unit permits switch selectable emulation of various terminals with block mode and advanced editing. Other functions include line insert and delete, character type over, character rubout, and format control. **Amtek Business Machines, Inc,** 2255H Martin Ave, Santa Clara, CA 95050.

Circle 209 on Inquiry Card

CRT DISPLAY MONITOR

NDC-120 provides 25-MHz video bandwidth, excellent linearity, uniform focus characteristics across the entire screen, horizontal retrace time that is typically less than 7 μs, and electronic and mechanical compatibility with Ball Brothers and Motorola monitors. Separate horizontal drive, vertical drive, and video signal inputs, as well as composite video, simplify interface circuitry. MTBF is 10,000 hours min with a 90% confidence level. The unit is delivered with P4 phosphor. **TSD Display Products, Inc,** 35 Orville Dr, Bohemia, NY 11716.



Circle 210 on Inquiry Card

SMS *FLOPPY* PLUS WINCHESTER DISK STORAGE FOR DEC® COMPUTERS

AVAILABLE SOON!! Look for 20M byte and 30M byte Flinchester systems in the near future.

MAXIMUM PERFORMANCE AND CAPACITY
- **8.9M bytes** of formatted Winchester disk storage plus 1.2M bytes of usable floppy disk storage.
- Fast data transfer of **427K bytes/sec** for Winchester and 63K bytes/sec for floppy.

UNSURPASSED RELIABILITY
- Modular construction and minimal parts count insure **long MTBF** and 15 minute MTTR.
- Off-line system and drive test.
- On-board **self test** verifies correct system operation.
- CRT initiated **super diagnostics** ease system test and fault isolation.
- **Automatic bootstrap** tests CPU, memory and DMA operation before software loading.

CONVENIENT "MINUTE-PER-MEGABYTE" BACKUP
- Only **40 seconds** required for Winchester backup onto 1.2M byte floppy diskette.
- Standard RT-11, RSX-11M and SMS utility software supports partial or selective file backup and load operations.

INDUSTRY COMPATIBLE
- Automatic recognition of DEC RX01, RX02 and **IBM** diskette formats.
- Plug compatible with DEC PDP-11 Unibus and LSI-11 Q-bus.
- Increases performance of DEC's RT-11 and RSX-11M operating systems.
- Emulates DEC's **RX02** floppy disk system.

EXCEPTIONAL DATA INTEGRITY
- Winchester disk **flaw management** deletes permanently flawed disk areas.
- Automatic **error retry** recovers soft or temporary errors.
- **ECC (Error Correction Code)** recovers corrupted data without system shut down.
- Patented PLL circuitry requires no field adjustments and provides maximum margin for worst case bit shifted data recovery.

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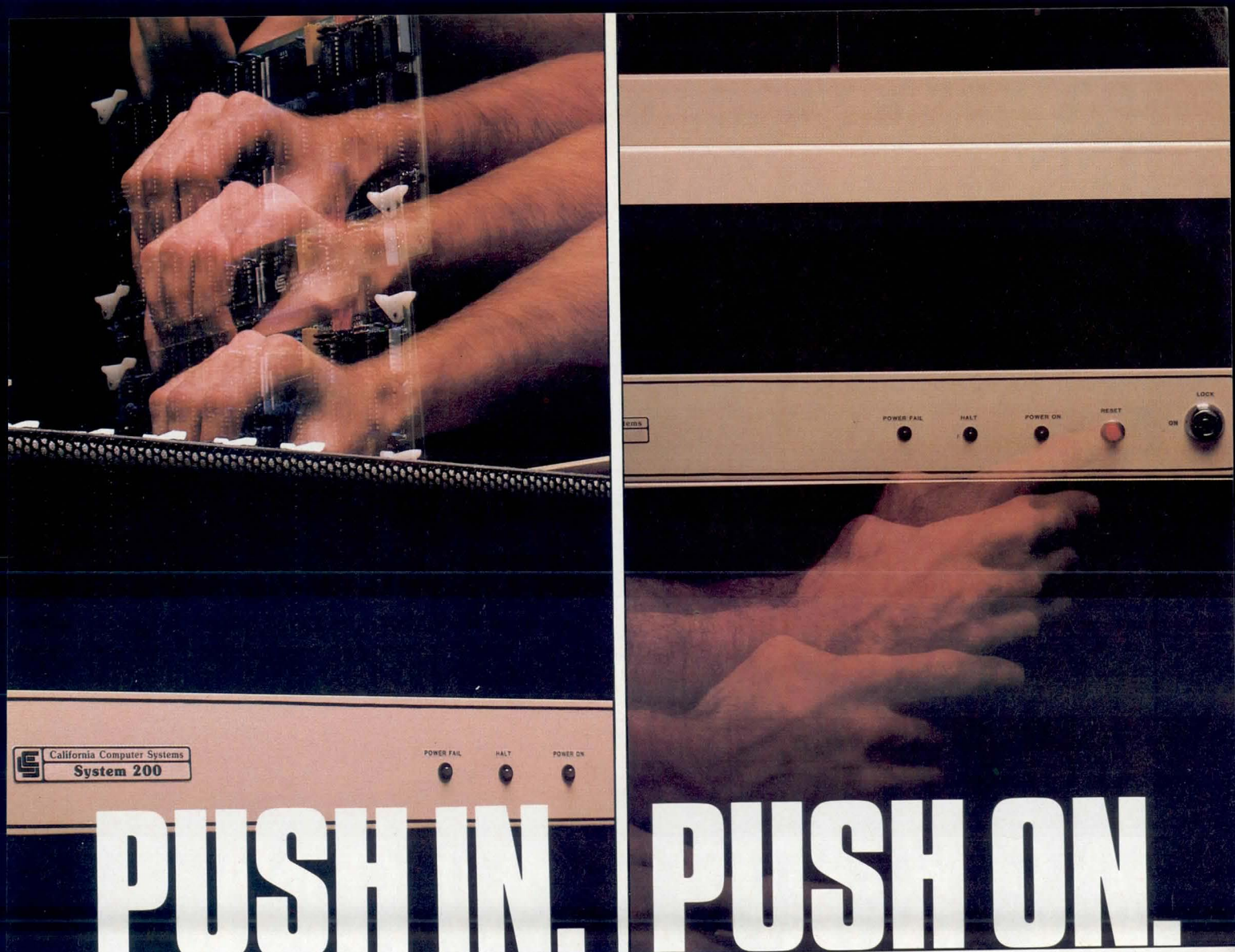
CIRCLE 110 ON INQUIRY CARD



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CCS. MAKING MINIS OUT OF MICROS.

Here's the CCS line of board-level computers for system builders on the move. **Push in** the CCS board. And **push on** with your application. CCS board-level systems go together easily, come up quickly, and run reliably, with a proven return rate of less than 1%.

CCS board-level computers offer systems builders the optimal combination of low development cost, low manufacturing cost, and high reliability from proven, tested modules.

A headstart on reliability. CCS modules are designed to industrial performance standards, manufactured to industrial quality standards, fully burned in and tested. You spend more time and energy on your application when you rely on CCS modules instead of reinventing (and rebuilding) standard computer functions.

A full selection of S-100 board-level computers. Whether you want to add capability to another S-100 based system, or build a system from scratch, chances are you'll find solutions for all your system needs in the CCS product line. CCS manufactures a comprehensive selection, so you can tailor a system to your needs with a minimum of components. You buy exactly what you need. But you can easily expand later.

- Z-80A CPU Modules.
- Static RAM Memory Modules.
- Dynamic RAM Memory Modules.
- Serial and Parallel I/O Modules.
- Floppy Disk Controller.
- Hard Disk Controller.*
- High Speed Arithmetic Module.*+

We'd like to tell you more about the CCS line of board-level computers, OEM systems, and computer systems. There's a lot more to tell. Send in the coupon for more information, contact your local computer dealer, or call.

- ○ Please have a sales representative call me.
- ○ Please send more information on CCS Board-Level Computer Modules.

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California Computer Systems
250 Caribbean Drive
Sunnyvale, California 94086
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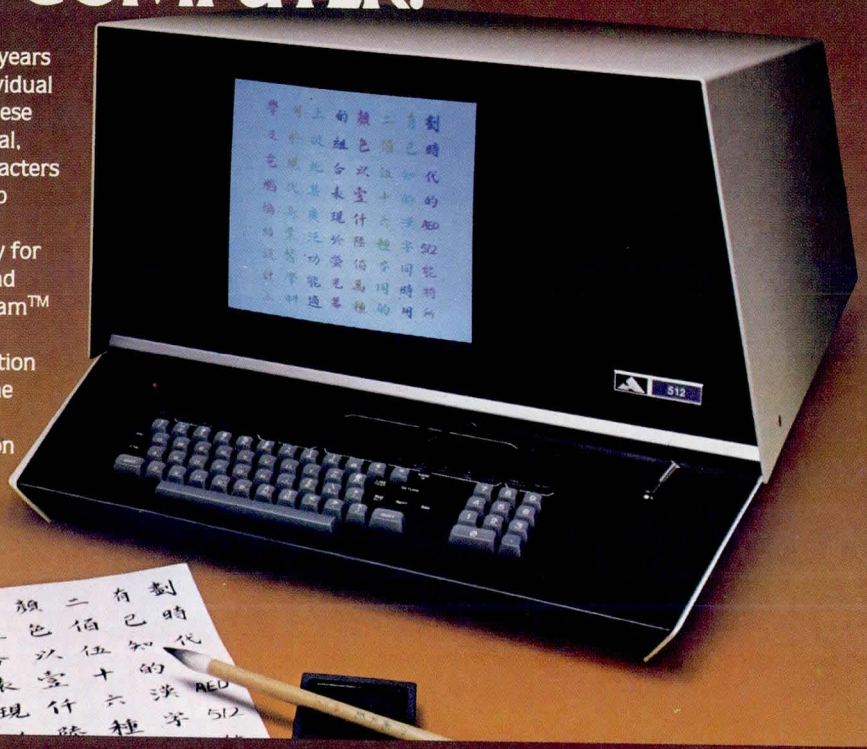
* Available Quarter 2, 1981.
\+ For use with CCS System Models 200, 300, 400.

CIRCLE 111 ON INQUIRY CARD

FROM MONOCHROME TO MULTICOLOR USING YOUR DEC COMPUTER.

美 Chinese brush calligraphy originated over 2,000 years ago, and familiarity with more than 10,000 individual characters is required to appreciate classical Chinese literature. With 256 simultaneous colors at your disposal, producing more than 16 million hues, each of these characters could be given a different shade on the AED512 desktop terminal. The AED512 offers programmable symbols, together with powerful imaging and graphics capability for use in business, medical applications, scientific study and CAD. Features like 512^2 (512 x 483 pixel screen), Superoam™ 1-16 integer zoom, continuous panning, down-loadable microcode, half-second image transfer and a wide selection of DMA interfaces (including LSI and PDP-11s), make the AED512 today's price/performance leader in intelligent graphics terminals. Call today to arrange a demonstration on your computer. We'll show you why 1981 is THE YEAR OF AED!



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TIN GOW. FASTEST GAME IN CHINA. WINC.™ FASTEST WAY TO WINCHESTER.

美 To play the ancient Chinese game of Tin Gow, you need a quick memory and a stack of money. But to complement your DEC computer with high-speed Winchester storage costs less than you think. In fact, our WINC controllers will give you up to 35 megabytes of data storage at the lowest cost per bit in their capacity range. DEC software transparent WINC controllers map all the data from three RL01/02s on a single Winchester (20/40 MBs unformatted)...plus running your RL diagnostics. That saves you space and money! A two-board set, the controller mounts directly in the chassis with the Winchester, while the compact Q-BUS/UNIBUS® interface plugs right into your PDP-or LSI-11. For transportable data, AED offers a cartridge tape drive that also mounts in the Winchester chassis. Call today for price and delivery information.

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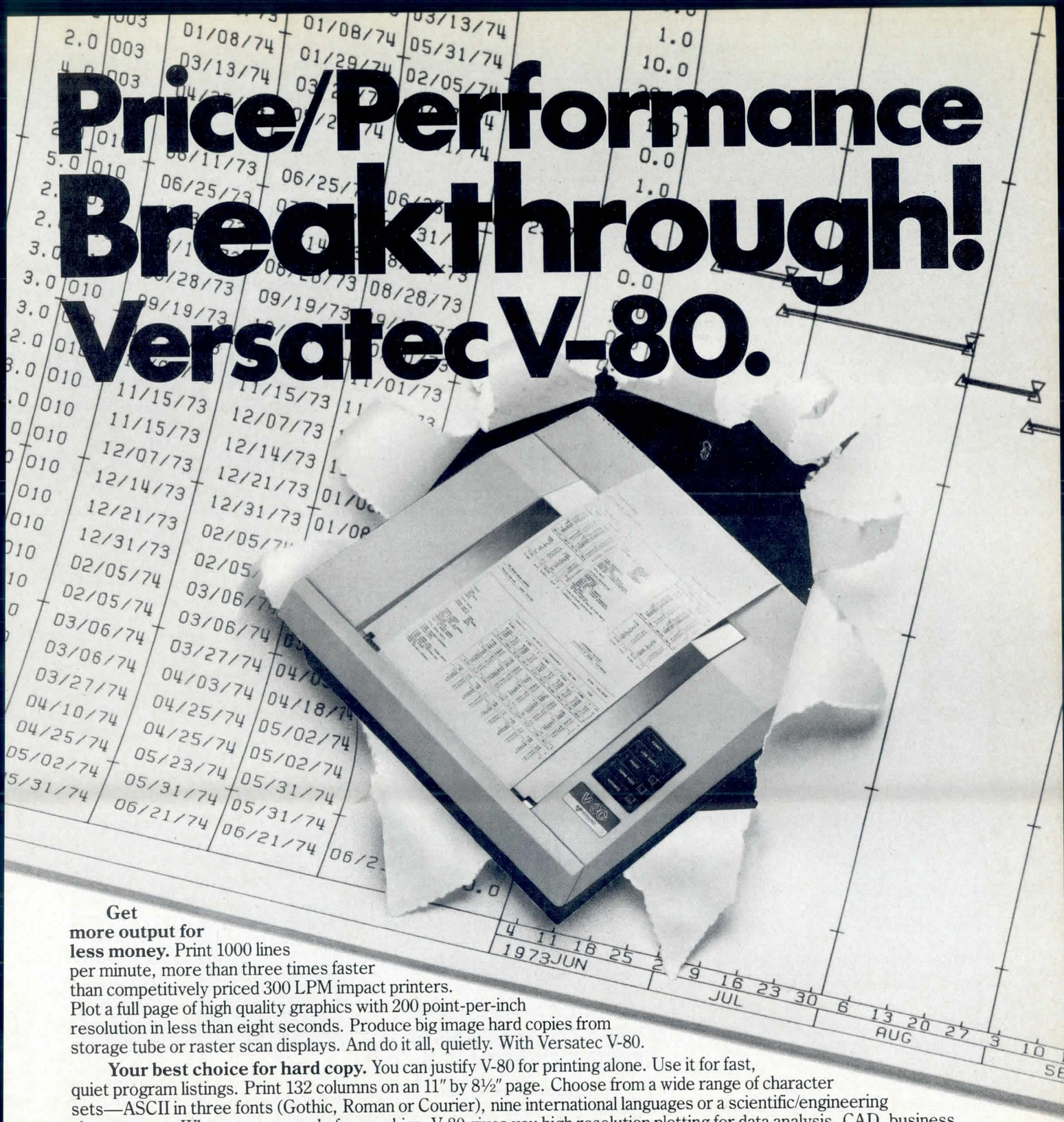
CIRCLE 113 ON INQUIRY CARD

Price/Performance Breakthrough! Versatec V-80.



Get more output for less money. Print 1000 lines per minute, more than three times faster than competitively priced 300 LPM impact printers. Plot a full page of high quality graphics with 200 point-per-inch resolution in less than eight seconds. Produce big image hard copies from storage tube or raster scan displays. And do it all, quietly. With Versatec V-80.

Your best choice for hard copy. You can justify V-80 for printing alone. Use it for fast, quiet program listings. Print 132 columns on an 11" by 8½" page. Choose from a wide range of character sets—ASCII in three fonts (Gothic, Roman or Courier), nine international languages or a scientific/engineering character set. When you are ready for graphics, V-80 gives you high resolution plotting for data analysis, CAD, business presentations, seismic sections, mapping, etc.

V-80 keeps delivering more performance for less money. V-80 non-impact electrostatic writing uses only seven moving parts. That means better reliability and easier maintenance. Modular design enables faster repairs.

And V-80 is nice to be around. Quiet electrostatic writing eliminates the irritating clatter of impact printers. Output is presented on a sloped platen for easy viewing. And changing toner is easier, and cleaner than changing a printer ribbon.

Get more output from your system. Versatec offers interfaces and intelligent controllers for all popular computers and display terminals, on-line and off-line systems, and support for local and remote operations. And V-80 is backed by the world's largest electrostatic printer/plotter sales and service network.

Break through to better price/performance. Circle our readers' service number for a free V-80 brochure.

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27/35 London Road Newbury, Berkshire, England Telephone: (0635) 42421 Telex: 847259

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CIRCLE 114 ON INQUIRY CARD

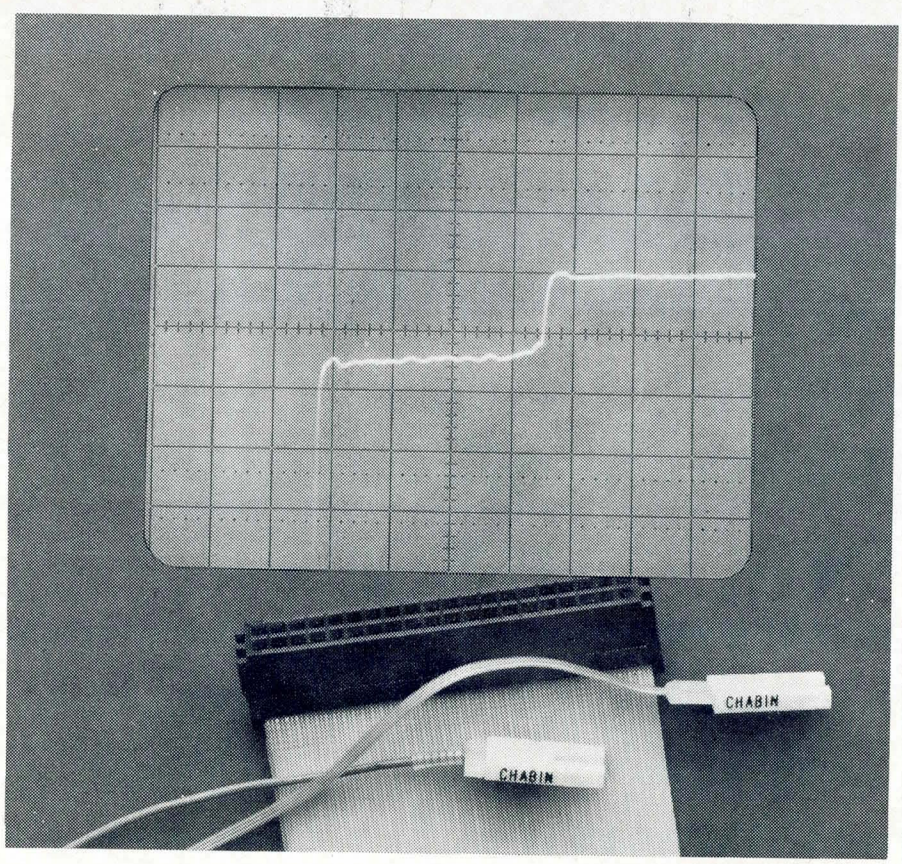
INPUT/OUTPUT DEVICES

OCR WORKSTATION

Scan + Plus workstation directly scans up to 6000 documents/h in continuous feed applications, or less when data are keyed from documents. Unit consists of document transport, single-line numeric OCR reader, document view stations, 2 program-selectable output stackers, and keystation. It can be located remotely or in data processing center. Data Capture operating system, a subset of ANSI '74 COBOL, handles up to 16 terminals. **Scan-Data Corp**, 800 E Main St, Norristown, PA 19401.
Circle 211 on Inquiry Card

GRAPHICS TABLET

An addition to the Personal Graphics System, HP 9111 Graphics Tablet is compatible with HP series 80 personal computers. It offers capabilities in 3 main areas to ease creation and manipulation of graphics on the display: tracing and digitizing existing designs or logos, creating new designs, and measuring areas and lengths of lines directly from maps or charts. **Hewlett-Packard Co**, 1507 Page Mill Rd, Palo Alto, CA 94304.
Circle 212 on Inquiry Card



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We focus all of our attention on high speed, controlled impedance transmission line interconnects.

When you need multiple or single-signal assemblies, Chabin Transmission Line Assemblies (TLA) are the answer . . . every time.

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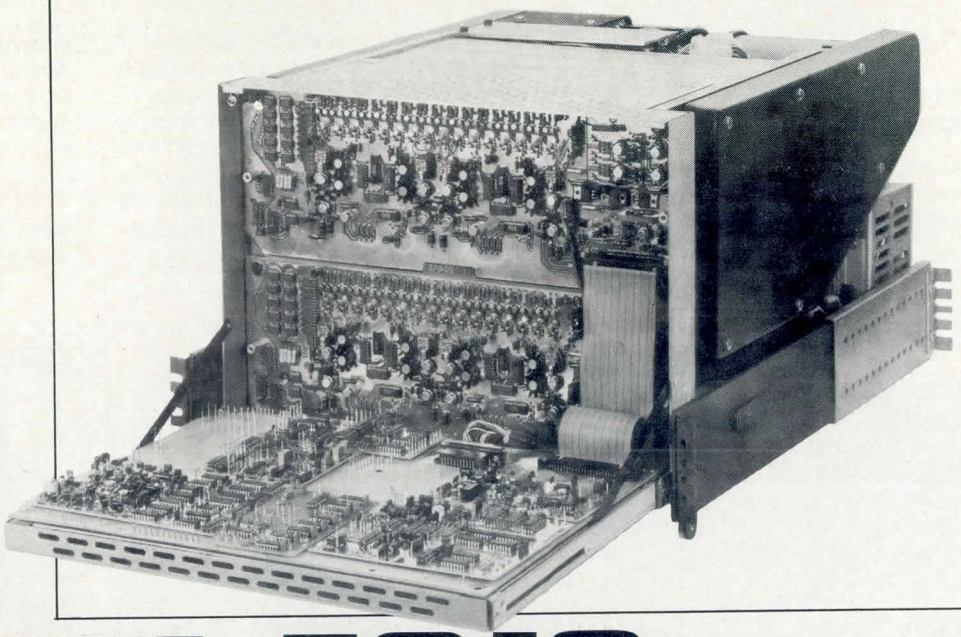
At Chabin we're large in capability yet small enough to be responsive.

DATA COMMUNICATIONS

DATA LINE MONITOR

Various data contained in HDLC or packet header can be translated into mnemonic format and displayed on high resolution 8" (20-cm) CRT according to CCITT X.25 protocol by model VP-3680A. Unit allows analysis of transmission procedures and aids in designing and diagnostic testing of data communications systems and peripherals. Features include selective trace, program trigger, and hard copy via video printer interface capabilities; std RS-232-C interface; and ease of operation. **Matsushita Communication Industrial Co, Ltd**, c/o MTC Div, 2446 Watson Ct, Palo Alto, CA 94303.
Circle 213 on Inquiry Card

RELIABILITY: 28,000 hr. MTBF.
ECONOMY: .035 cents per bit.



VRC MODEL 4016 MEMORY

CAPACITY . . .	37.9 million bits
BIT RATE	4.33 MHz
ACCESS TIME	8.5 m/sec.
DIMENSIONS	Height – 12¼" (31.2 cm.)
	Width – 17½" (44.5 cm.)
	Depth – 22" (55.9 cm.)
MEAN TIME TO REPAIR . .	Less than 1 hr.

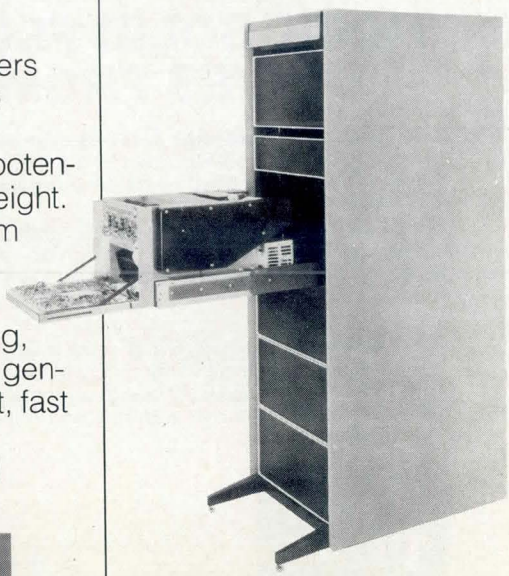
When it comes to speed, reliability and low cost, systems users in 25 countries in every continent of the world depend on the VRC 4016 head-per-track memory.

It features a fail-safe actuation system that eliminates the potential of media damage and data loss. It's compact and lightweight. All electronics, drive components and head retraction system are mounted outside the drum, making service simple and eliminating risk of contamination.

Applications are endless. Telecom and message switching, process control of all kinds, geophysical exploration, power generation, news editing, typesetting. Wherever low cost-per-bit, fast access and high data storage capacity are required.

For proven reliability, worldwide support, field service and predictable high quality, you can rely on VRC.

Write or call for complete details on the Model 4016 head-per-track memory...a simple, rugged, compact unit to improve the reliability of your system.



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CORPORATION

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Tel. (802) 886-2256, TWX: 710-363-6533
FAX (802) 886-2682

Vermont Research, Ltd.
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Tel. Leatherhead 76221
Telex: 23280
FAX Leatherhead 76834

CIRCLE 116 ON INQUIRY CARD

DATA COMMUNICATIONS

FIBER OPTIC DATA MULTIPLEXER

Lightwave Data Multiplexer LDM-9500 accepts up to 16 inputs from peripheral terminals, multiplexes them together, and transmits them over a fiber optic cable to a second multiplexer, which, after demultiplexing, interfaces the 16 ports to a host computer or other frontend device. The multiplexer operates full-duplex on a pair of optical fibers. Each of the 16 EIA data ports can be operated in asynchronous or synchronous mode. Asynchronous data rates can vary from dc to 19.2k bits/s. Synchronous operation is provided for any data rate from dc to 64k bits/s with external clock. **Digital Communications Corp,** 11717 Exploration Lane, Germantown, MD 20767.

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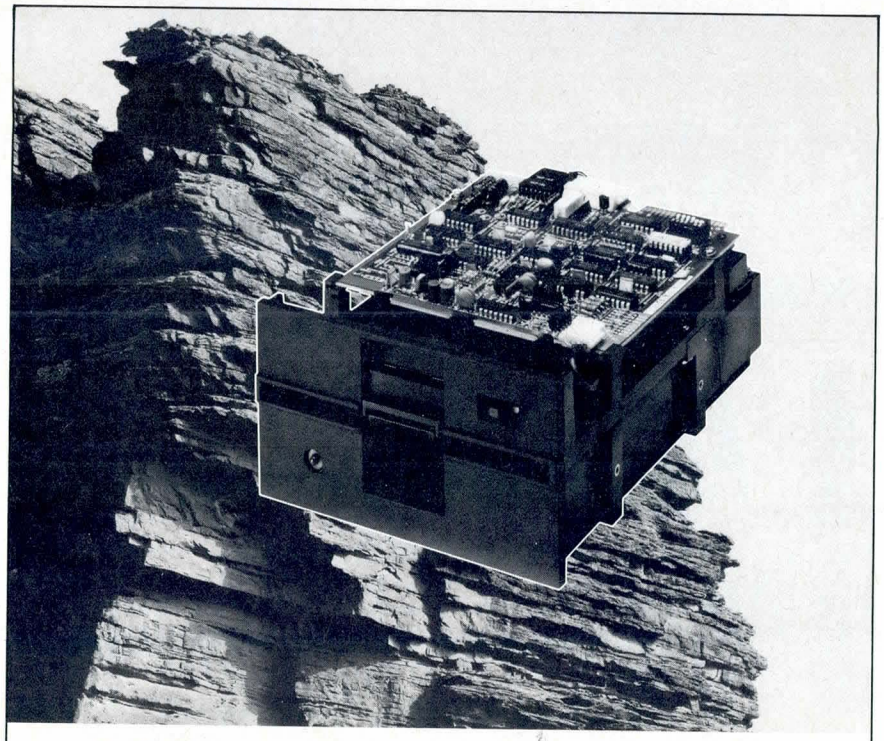

ROCK-SOLID FLOPPY DISK DRIVES FROM TEAC

Unique DC Spindle Drives feature our continuously-running brushless DC motor whose typical life expectancy is over 10,000 hours. Rock-stable, no electrical noise will interfere with the integrity of your data.

Superior Chassis features fiberglass reinforced polyester (FRP) which, unlike aluminum, won't stretch with heat. Extra-rugged and precision molded, the unit also has a shield to insulate the head from outside interference.

25 Years of Leadership in all magnetic recording technologies is your assurance of a quality product you can rely on. For complete information on all TEAC Rock-Solid Floppy Disk Drives (FD-50 Series) — including our one-year warranty and full technical support and service — just write:

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X.25/X.75 PROTOCOL TESTER

Software/hardware development tool NET-18 serves as an aid to developers of software and hardware for X.25/X.75 networks. The self-contained system simulates all levels of the X.25/X.75 protocol. The device can simulate both DTE/DCE, monitor X.25 lines, generate and display frames and packets, and report error conditions. As a fully implemented X.25 node, it can save from 30% to 50% of the time needed to develop and implement X.25 software and hardware. **Dynatech Packet Technology, Inc,** 7664-A Fullerton Rd, Springfield, VA 22153.

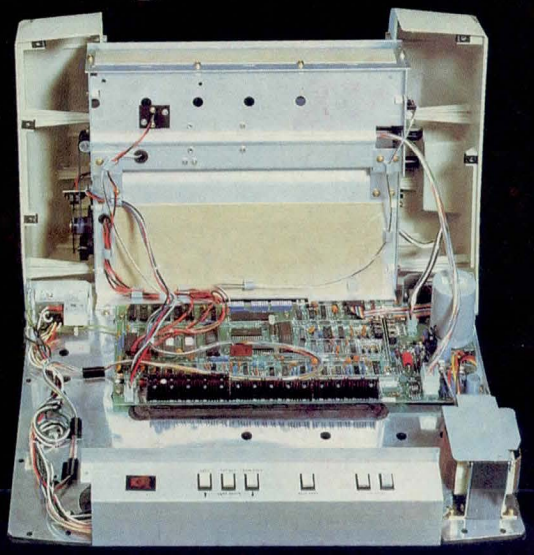
Circle 216 on Inquiry Card

ASYNCHRONOUS MULTIPLEXERS

A buffered, program controlled interface between PDP-11 and multiple local or remote asynchronous terminals, the compact SCD-DZ11 is available in 8- or 16-line EIA or 20-mA versions, as well as a version which provides 8 lines each of EIA and 20-mA operation on a single multiplexer. All are software compatible with DEC operating systems and diagnostics designed for the DZ11. Eight-line versions consist of a single hex-wide control board, cable assembly, and distribution panel. They expand to 16 lines by adding a second control board and cable assembly. **Sigma Sales, Inc,** 6505 Serrano, Anaheim Hills, CA 92807.

Circle 217 on Inquiry Card

Say Ahh...



Our New grafixPLUS™ 80-column printer opens wide for easy servicing.

Introducing the newest members of our grafixPLUS™ family—the DP-9000 Series 80/132 column printers—built on the same tradition of quality printout, solid design and low cost of ownership established by our 132/220 column DP-9500 Series.

A Case for Serviceability

Not that is comes up often, but want to get inside? Simple. Just remove a few screws and the clam-shell case swings open exposing all major components. This easy access plus built-in self-test and minimum component count yields an MTTR of one-half hour. The 9-wire print head replacement's even simpler . . . two screws and it's out. Without opening the case. And without a service call.

Performance Plus

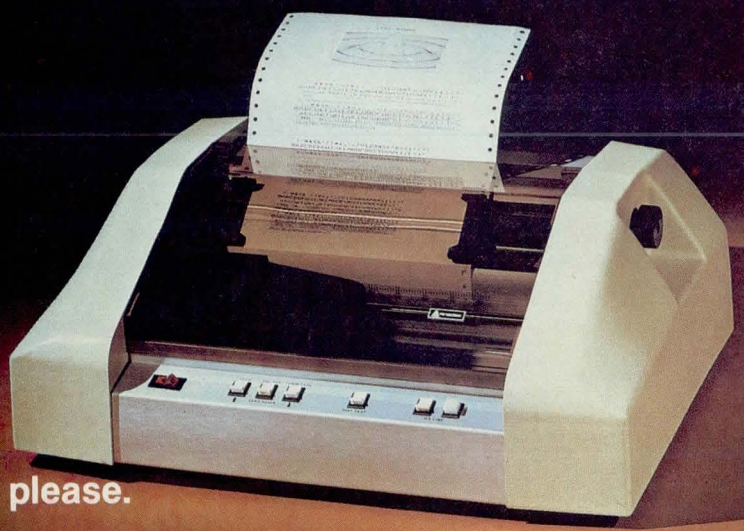
The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

Interface Flexibility

The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

When you're ready for a printer (or several thousand), look into the grafixPLUS DP-9000 Series from Anadex—you'll find an open and shut case for quality. Contact us today for details, discounts and demonstrations.

Anadex®
...the plus in printers



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The MIPROC-16AP offers super fast preprocessing, postprocessing and I/O handling power for your DEC® PDP-11® computer.

Adding a MIPROC-16AP to your PDP-11 adds processing power normally associated with much larger computers. . . 4 million instructions per second, 177 instructions, 256 directly addressable I/O channels with data I/O rates of 2.0 megabytes under program control and up to 20 megabytes DMA. . . Interrupt response in 750 nanoseconds, full context switching in less than 3 microseconds.

Optional floating point hardware offers 32 bit floating point operation in parallel with normal instructions.

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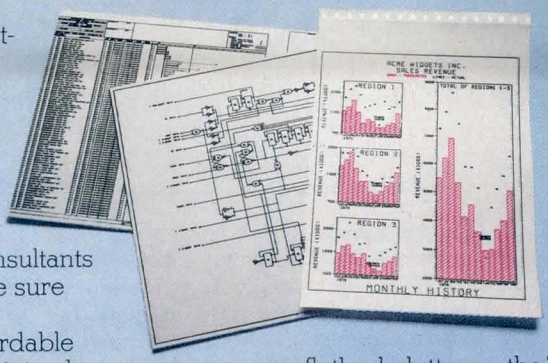
WE'VE ALWAYS OFFERED MORE GRAPHICS SOLUTIONS.

WITH ELECTROSTATICS, WE OFFER THEM ALL.

With the addition of electrostatics, CalComp has the broadest line of plotters available from any vendor. Whatever your application demands — flatbed, beltbed, continuous roll, computer output to microfilm or electrostatic — CalComp has a solution. And our sales representatives, graphics consultants with years of experience, will make sure it's the correct solution.



For plot previewing at an affordable price, our sales representative will introduce you to the new electrostatic printer/plotters. They're ideal for mapping, plot previewing, business charts and graphs and a host of other applications. And they function as a fast line printer as well.

Our representatives can help you select from a printer/plotter family that offers seven models, paper widths of 11" and 22" and plotting resolutions of 100 and 200 dots per inch. Plus, there's a wide range of operational and application software available.

When your plotter application requires a high degree of resolution or larger plots, our graphics professionals will still have the answer. Take our compact 1012 desk-top plotters for starters. You get crisp, clean 8½" x 11" or 11" x 17" size plots and the convenience of Z-fold paper.

For bigger jobs, there are six other precision drum plotters to choose from. Including the industry's largest, our new 1065, with an extra-wide 72" drum that plots at 30 ips.

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You also get a reliability guaranty you'd only expect from the graphics leader. All CalComp plotters are covered by our unique one year warranty on parts and labor. And our graphics consultants are backed by 22 systems analysts and over 100 service representatives in 35 cities — the most extensive service and support network in the plotter industry.

So, if you're looking for a solution to your graphic needs, call us today. We've got all the right answers.

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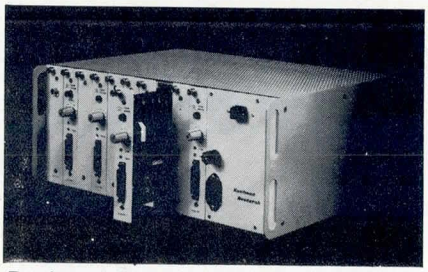
California Computer Products, Inc., 2411 W. La Palma Ave., Anaheim, CA 92801—Sales Offices: Tempe, AZ: (602) 894-9468, Orange, CA: (714) 978-7111, Santa Clara, CA: (408) 727 0936, Tarzana, CA: (213) 708-1093, Englewood, CO: (303) 770-1950, Altamonte Springs, FL: (305) 331-4615, Norcross, GA: (404) 448-4522, Schaumburg, IL: (312) 884-0300, Shawnee Mission, KS: (913) 362-0707, Metairie, LA: (504) 833-5155, Waltham, MA: (617) 890-0834, Southfield, MI: (313) 569-3123, Bloomington, MN: (612) 854-3448, St. Louis, MO: (314) 863-2711, Woodbridge, NJ. (201) 636-6500, Fairport, NY: (716) 223-3820, Cleveland, OH: (216) 362-7280, Dayton, OH: (513) 276-5247, Tulsa, OK: (918) 663-7392, Portland, OR: (503) 241-0974, Wayne, PA: (215) 688-3405, Pittsburgh, PA: (412) 922-3430, Dallas, TX: (214) 661-2326, Houston, TX: (713) 776-3276, McLean, VA: (703) 442-8404, Bellevue, WA: (206) 641-1925

CIRCLE 121 ON INQUIRY CARD

DATA COMMUNICATIONS

PORT CONCENTRATOR



Designed for IBM 3270 protocol, model 870 enables a single IBM system port to support 32 nodes of 8 terminals each; it supports any ASCII device, including special or nonstandard terminals. Unit provides necessary display and formatting control functions. Data rates of terminals can be from 110 to 19,200 bits/s; communication with IBM system is bisynchronous at up to 19.2k baud. Concentrator can operate in remote or local mode for computer port or terminal cluster, and performance is unaffected by expansion. **Kaufman Research Manufacturing, Inc,** 14100 Donelson Place, Los Altos Hills, CA 94022.

Circle 218 on Inquiry Card

UNIVERSAL RS-232/449 INTERFACE CONVERTER

Model 60 allows RS-232-C based equipment to be coupled with devices using the standard RS-449. Converter incorporates switching facility that allows user to select the RS-232 as either DTE or DCE. Support of reverse channel for the RS-449 is provided by separate 9-pin male connector. The RS-232 port has a 25-pin female connector while the RS-449 port has a 37-pin male connector. **Remark International,** 4 Sycamore Dr, Woodbury, NY 11797.

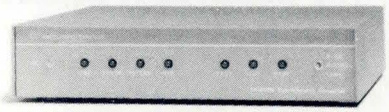
Circle 219 on Inquiry Card

SHORT RANGE MODEM ELIMINATOR/DRIVER

For synchronous or asynchronous operation at distances up to 400 ft (122 m), model 300 allows direct connection between terminals and computers. The driver provides digital regeneration of signals to achieve the increased operating distance and provides necessary EIA signal interchange between the terminals. An internal crystal controlled oscillator provides operating speeds of 2.4k, 4.8k, 9.6k, and 19.2k bits/s, all switch selectable. **Avanti Communications Corp,** Aquidneck Industrial Pk, Newport, RI 02840.

Circle 220 on Inquiry Card

SYNC-ASYNC CONVERTER



Allowing asynchronous data terminals to operate on synchronous data link, TP-200M accepts data in asynchronous format and converts it for operation with synchronous modem. It also matches terminal data rate to modem. Converter provides for error detection and retransmission, and offers remote test capability, remote reading of operating parameters, and front panel diagnostics. Unit is available in rack or desk models. **TeleProcessing Products, Inc,** 4565 E Industrial St, Bldg 7K, Simi Valley, CA 93063.

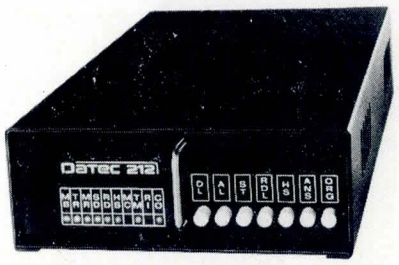
Circle 221 on Inquiry Card

300-BIT/s SWITCHED NETWORK MODEMS

Operating at 300 bits/s, Western Electric compatible models 103J, 113C, and 113D are compact, single-card modems designed to mount in a high density 16-card, 10.5" (26.7-cm) shelf or in a single convenient standalone enclosure, without modification. Units are end to end compatible with Bell 103 and 113 series data sets, and are full-feature equivalent to Bell 103J, 113C, and 113D data sets. 103J operates in originate and answer modes, 113C is originate only, and 113D is answer only. **General DataComm Industries, Inc,** 1 Kennedy Ave, Danbury, CT 06810.

Circle 222 on Inquiry Card

300/1200-BIT/s MODEM



Full- or half-duplex operation, manual and automatic answer/originate capabilities, lease line capability, and programmed or permissive transmission are features of the model 212 dual-speed modem. In low speed mode its data rate is 0 to 300 bits/s in binary, serial, asynchronous format; in high speed mode its data rate is 1200 bits/s in character- or bit-synchronous formats. Manufactured under a WECO license, this modem is compatible with Bell 103, 113, and 212A modems or acoustic couplers. It operates in a binary frequency shift key format at low speed and in differential phase shift keying format at high speed. In answer mode, the modem automatically adjusts to the speed of the originating modem. Character length is 9 or 10 bits including start/stop bits. Data interface is EIA RS-232-C. Contained in the modem are an internal optically isolated DAA, telephone line equalizer, linear phase-active receiver and transmit filters, test pattern generator-analyzer, and 2 custom Bell-designed MOS LSI chips. Receiver sensitivity is −48 dBm over worst case lines. **Datec Inc,** 300 E Main St, Carrboro, NC 27510.

Circle 223 on Inquiry Card

VT100 GRAPHICS IN 4.4 MINUTES!

From Selanar Of Course!

SIMPLY ADD A CARD

Adding the Graphics 100 PC card to your existing VT100 or VT103 gives you the most versatile CRT terminal on the market today. No other component or CRT changes are required.

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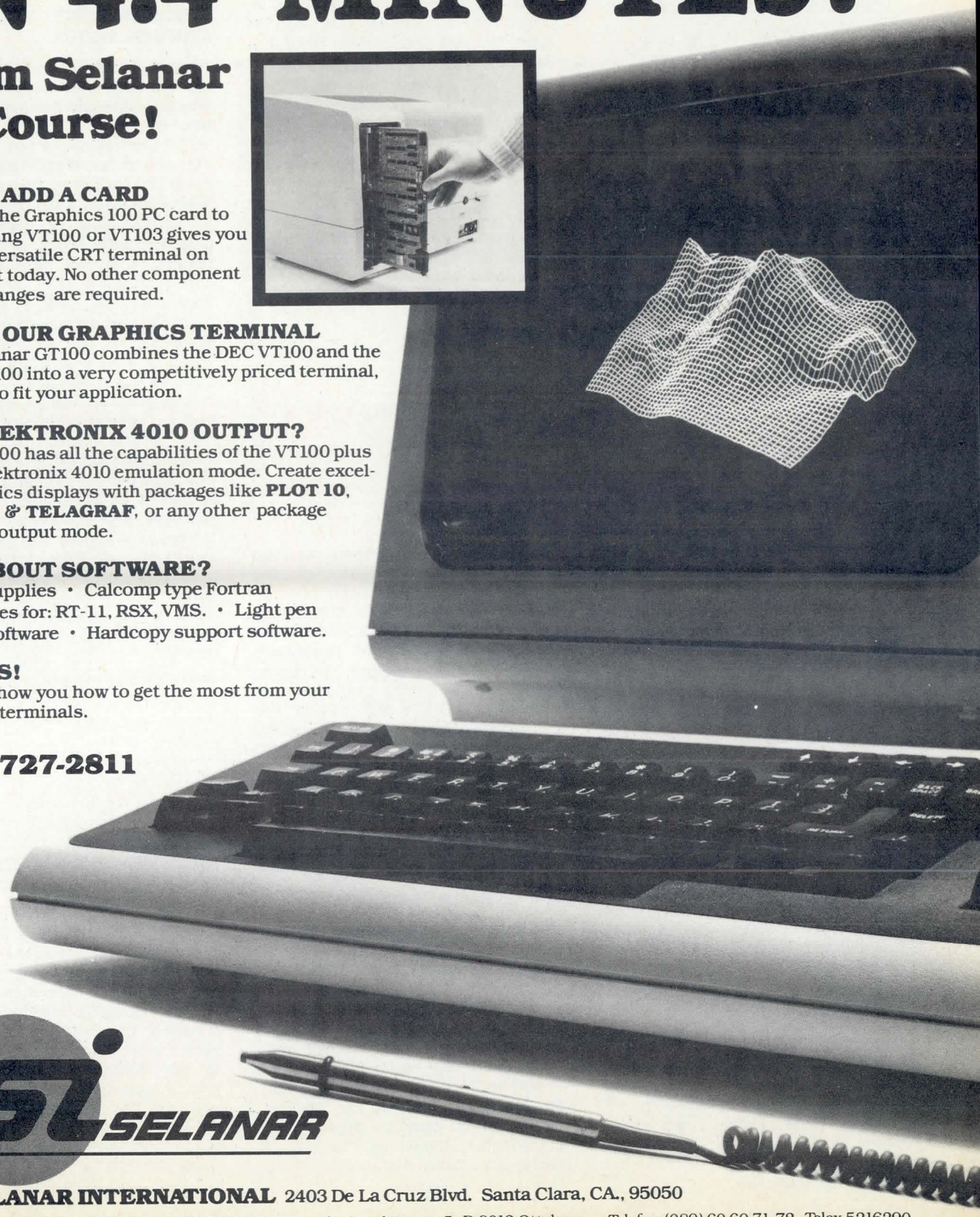

ISI SELANAR

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EUROPEAN HEADQUARTERS: ISI COMPUTER Alte Landstrasse 5 D 8012 Ottobrunn Telefon (089) 60 60 71-72 Telex 5216290

CIRCLE 123 ON INQUIRY CARD

TEST AND MEASUREMENT

BENCHTOP BACKPLANE TESTER

N123A, designed primarily for testing units in the 1000- to 8000-point size range, incorporates new memory and control cards, keyboard, and thermal printer in place of the strip printer. Maximum network length has been expanded from 450 to 1280 points. Print menu allows a choice of diagnostic printouts in user product nomenclature either on Pass and Fail, or on Fail only. An added command makes it possible to order printouts for hardcopy documentation of the equivalency tables which identify test points in product nomenclature. **Teradyne Inc,** 35 Morrissey Blvd, Boston, MA 02125.

Circle 225 on Inquiry Card

16-CHANNEL LOGIC ANALYZER

With memory depth of 2000 or 1000 words, and max recording speed of 50 or 24 MHz, LAM 1650 records in 8- or 16-channel mode, respectively. A timing diagram of each 8-channel input block is available in both modes. Triggering is done using a 4-level sequential trigger mode, up to 24 bits wide, and is backed by the trigger trace monitor. Up to 6 measurement setups may be stored in and recalled from nonvolatile menu memory. The unit allows choice of 4 threshold levels for its 2-variable, fixed TTL, and fixed ECL inputs. Two independent external clocks may be used in 16-channel mode. **Dolch Logic Instruments, Inc,** 230 Devcon Dr, San Jose, CA 95112.

Circle 226 on Inquiry Card

ROM/EPROM TEST SYSTEM

Q2/20 is based on microprogrammable pattern generator that controls address and DUT clock generation and incorporates advanced flow control logic for total test pattern flexibility. Six independently programmable DUT clocks can be used as chip selects, output enables, address latches, or EPROM programming inputs. Generator uses high level user oriented language to simplify pattern development. System features 128k-byte data buffer to store codes for ROMs and EPROMs up to 8k x 16 or 16k x 8 bytes. **Megatest Corp,** 2900 Patrick Henry Dr, Santa Clara, CA 95050.

Circle 227 on Inquiry Card

POWER SOURCES AND REGULATORS

SEVERE ENVIRONMENT POWER SUPPLIES

For a variety of high temperature, high shock, high humidity and high salt spray applications, SE assemblies include 4 single- and 2 dual-output power sources. A 44 x 8 x 8" (111 x 20 x 20-cm) case of ruggedized stainless steel packages the units. Power ratings for the modules in the assembly are 3.5, 5, 9.8, 12, 14, and 28 V, respectively. Source voltage range is either 105 to 125 V or 220 to 250 V. **Technipower, a Penril Co,** PO Box 222, Danbury, CT 06810.

Circle 228 on Inquiry Card

LITHIUM BACKUP BATTERIES

Designed for high volume PCB DIP assembly methods, hermetically sealed, leak proof, single-unit keeper batteries are available in 3-V/500-mAh, 3-V/1000-mAh, and 6-V/500-mAh configurations. Batteries meet military standards and have high abuse tolerance; op temp range is −100 to 250 °F (−73 to 121 °C). Pin location and type can be customized for specific applications. **Eagle-Picher Industries, Inc,** C & Porter Sts, Joplin, MO 64801.

Circle 229 on Inquiry Card

COMPUTERS AND COMPUTER SYSTEMS

CHINESE LANGUAGE COMPUTER SYSTEM

A compact small business computer, the Sigma-10 has complete Chinese character capability and a high resolution display capable of displaying 1520 Chinese characters (38 lines of 40 chars) or 4800 alphanumeric chars (60 lines of 80 chars), the maximum content of a std printed page. It is also capable of high resolution graphics with 512k pixels. A dictionary of approx 8k Chinese characters contains both simplified and traditional char sets. A specific dot matrix or font represents each char. A line or page of text is represented by a string of font characters. Display of Chinese text is handled by the refresh memory of the unit's general controller. The user simply sends Chinese data to the display by addressing system subroutines. Printing follows the same pattern except that the font is printed on hard copy. Compatible with the CP/M operating system, the Z80 based system offers user memory capacity of 64k bytes, BASIC language, online storage for 1024k bytes, and unlimited offline storage capacity. **Sigma Information Systems, Inc,** 556 Trapelo Rd, Belmont, MA 02178.

Circle 230 on Inquiry Card

STANDALONE COMMUNICATIONS PROCESSOR

MC-80 features modular software, allowing configuration of systems that provide mainframe users with device independence and lowered cost on RJE and interactive stations. End-to-end peripheral control and multidrop, polling front ends for minicomputers are provided. Communications protocols permit attachment of foreign devices to IBM, Burroughs, NCR, Honeywell, and Univac networks through direct hook-up or dedicated/multidrop modems. **Innovative Electronics Inc,** 15200 NW 60th Ave, Miami Lakes, FL 33014.

Circle 231 on Inquiry Card

The smallest 1/2 megabyte microcomputer has the biggest feature of all.

50 megabucks worth of software.

Sure, it's handy to get our HP 1000 L-Series microcomputer on just two boards—with a single board holding the full 1/2 megabyte of memory! But, before you consider buying any microcomputer, you should look beyond the hardware to the software.

After all, that's where most of the time and money is often spent in developing a microcomputer-based system. But you can eliminate almost all that effort by using an L-Series. With $50 million worth of software development behind it, you only have to worry about developing your applications programs.

The L-Series offers you the ideal combination of HP's big system software and economical microcomputer hardware. So you can build cost-effective solutions for data acquisition and control, communications, factory automation and a whole range of other products.

Designer software.

With the minicomputer software that HP has been perfecting for more than a decade, plus our Model 10 Development System, you'll find it's easy to create the system you need.

You can start with either RTE-L or RTE-XL, our powerful multi-programming, multi-user operating systems. Their modular construction lets you build the real-time computing environment your applications programs demand—programs you can develop in Assembler, FORTRAN 4X, BASIC and PASCAL. And our HP DSN networking software makes it simple to put low-cost computing wherever you need it.

Data base management on a board computer? With our IMAGE DBMS, you've got a powerful tool for simple and efficient data management. And you can easily picture the possibilities offered by our GRAPHICS/1000 software. Like our other software packages, these are all upwardly compatible throughout the entire HP 1000 line, giving you an easy growth path to even higher performance.

Efficiency across the board.

How to handle all this software power? Simple. We used an advanced distributed intelligence architecture that puts a separate LSI I/O processor on each interface board. This means each processor has its own direct channel to the entire 1/2 megabyte memory. (We used state-of-the-art 64K RAMS to put the 512K bytes of memory on just one board.) And with the CPU free to concentrate on computation, you get significantly increased throughput and exceptional microcomputer performance.

A range of solutions.

The L-Series comes in a variety of configurations to meet your needs best—from boards and boxes to entire systems. Prices start at only $1968 for a starter set that includes CPU, 64KB memory and one I/O board.

Like our other OEM products, the L-Series is backed by our full range of customer services—including worldwide software and hardware support.

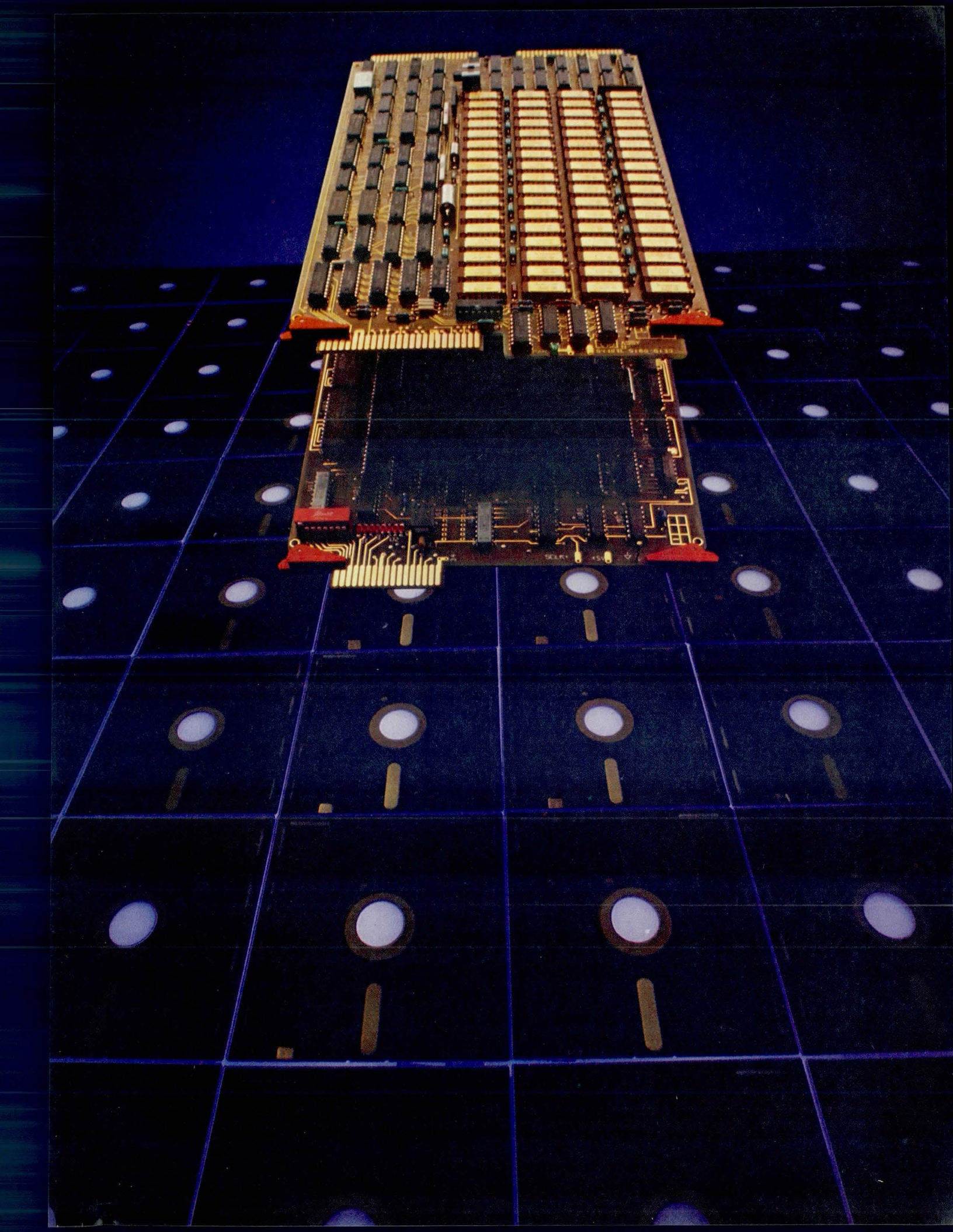
If you'd like a hands-on demonstration, just contact your local HP sales office listed in the White Pages. Or write for more information, and our new OEM catalog, to Hewlett-Packard, Attn: Joe Schoendorf, Dept. 1296, 11000 Wolfe Road, Cupertino, CA 95014.

HEWLETT PACKARD

U.S. OEM prices in quantities of 100.

Effective immediately: memory price reduced by 60%! CPU and 1/2 Mb memory for only $4500.

CIRCLE 127 ON INQUIRY CARD



SUBASSEMBLIES

PRINTER CONTROLLER

Fitting into 15" (38-cm) I/O card slot of Data General's NOVA and ECLIPSE computers, controller allows direct interface of computer to Mannesmann Tally serial and line printers with speeds ranging from 160 char/s to 300 lines/min. Controller is compatible with DG operating systems, including RDOS, AOS, and IRIS. For addressing, any of 64 device codes can be selected via DIP switch positioning. Self-test capability locates faults to printer, controller, or computer. Parallel data transfer rate is 100k bytes/s. **Mannesmann Tally,** 8301 S 180th, Kent, WA 98031.

Circle 232 on Inquiry Card

2-SPEED SYNCHRO PROCESSOR

TSL 1X36 accepts 2 binary word inputs from pair of synchro/resolver to digital converters that are mechanically or electrically geared in coarse/fine system and provides single, unambiguous 20-bit binary output that represents coarse synchro shaft angle. Inputs to processor are up to 14 bits from fine converter and 7 bits from coarse converter. With total conversion time of 250 ns typ, processor features 3-state output, available in 3 bytes for compatibility with 8- or 16-bit data bus systems. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.

Circle 233 on Inquiry Card

GAS DISCHARGE DISPLAY POWER CONVERTER

For 14-segment, 16- and 20-char, 1-line, screened image alphanumeric gas discharge display formats, E 1600 supplies 200 Vdc at 30 mA or ±100 Vdc at 30 mA from low dc line voltages, and up to 6-W power output. Encased in plastic and designed for PC board mounting, converter also accommodates 7-segment, 14-char, 2-line displays and certain matrix-type gas discharge displays. Weight is 40 g and dimensions are 1.88 x 1.30 x 0.82" (4.77 x 3.30 x 2.08 cm). **Endicott Research Group, Inc, Subsidiary of Endicott Coil Co, Inc,** 109 Main St, Johnson City, NY 13790.

Circle 234 on Inquiry Card

CIRCUIT COMPONENTS

LOW COST 14-BIT A-D CONVERTER

MP2734, a 14-bit modular ADC, combines 7-μs conversion time and ±0.5 LSB differential linearity. Suitable for application in precision data acquisition, the device has a differential nonlinearity tempco of ±1 ppm/°C, operates with uniform code widths, and maintains reliable high speed performance. With pin-programmable full-scale ranges of 0 to 5, 0 to 10, ±5, and ±10 V, the converter accepts all standard signal input ranges. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.

Circle 235 on Inquiry Card

14-BIT D-S CONVERTER

B1670 series synchro drivers accept 14 bits of digital data into internal registers and position up to 3 size 11 torque receivers within an accuracy of ±4 arc-min. Unit will switch the TRs through 180°, yet is fully protected against short circuits and synchro load malfunctions. Use of low power TTL input registers enables converters to be paralleled and multiplexed. An integral damping feature prevents current surges and ensures smooth and continuous rotation. **Transmagnetics, Inc,** 210 Adams Blvd, Farmingdale, NY 11735.

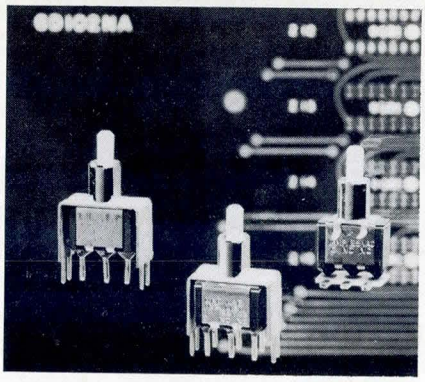
Circle 236 on Inquiry Card

MINIATURE 10-A POWER ROCKER SWITCH

Models C102 (spst) and C101 (spdt) have four positive locking legs for snap-in mounting and fit a 0.550 x 1.125 x 0.020 to 0.200" thick (1.397 x 2.857 x 0.051 to 0.508-cm) std panel cutout. Quick connect blade terminals accept 10 A at 125 Vac. Insulation resistance is greater than 1G Ω; contact rating is 10 A at 125 Vac or 28 Vdc, and 7.5 A at 250 Vac; and dielectric strength is 1500 V rms at sea level. **C & K Components, Inc,** 15 Riverdale Ave, Newton, MA 02158.

Circle 237 on Inquiry Card

PCB MINIATURE PUSHBUTTON SWITCHES

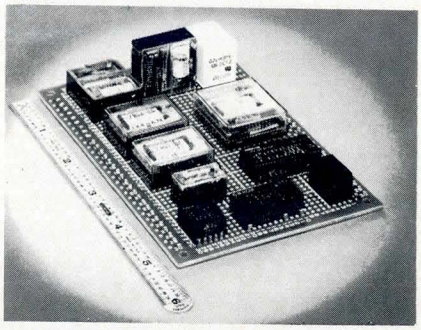


Series PS5 and PS6 single-pole, right angle, horizontal mount switches use epoxy board and bushing bracket and differ only in orientation of common terminal relative to bushing flat. PS7 and PS8 are available in single- or double-pole models and feature PC terminal and support bracket for mounting. PS7 has longer bushing and plunger than PS8. **Eaton Corp, Commercial Controls Div,** 4201 N 27th St, Milwaukee, WI 53216.

Circle 238 on Inquiry Card

PCB DIP RELAYS

G2N provides 80-mW sensitivity to permit direct drive by TTL, DTL, or IC circuits for interface devices. Units have independent 1A (SPST-NO) and 1B (SPST-NC) contacts and provide 10-W switching capacity with max switching current of 0.3 A. Available coil voltage ratings are 3, 5, 12, and 24 Vdc. G2P, an SPDT type for TTL direct power drive use, provides 3-A switching capacity at 120 Vac. Pick-up power is as low as 150 mW; dielectric strength is 2000 Vac; and coil voltage ratings are 5, 6, 12, and 24 Vdc. **Omron Electronics, Inc, Control Components Div,** 650 Woodfield, Schaumburg, IL 60195.



Circle 239 on Inquiry Card

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World's Leading Manufacturer of Miniature & Instrument Ball Bearings.

NMB offers a complete line of standard precision miniature and instrument ball bearings in ABEC 1 through ABEC 9 tolerances, as well as modified designs for special applications.

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CIRCLE 64 ON INQUIRY CARD

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Upper/lower case char.
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Non-glare screen
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Blinking cursor

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Typewriter/TTY keyboards
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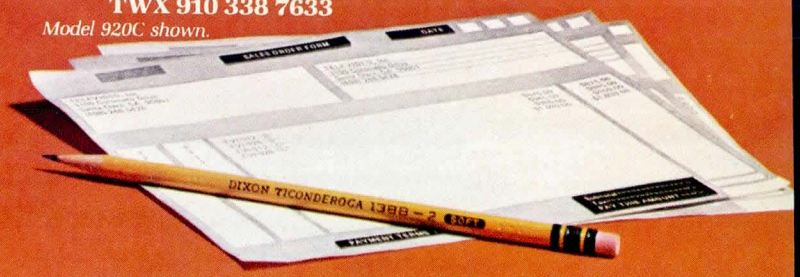
Model 920C shown.



COMPARE PRICE.

CALIFORNIA Santa Ana (714) 557-6095 • Sunnyvale (408) 745-7760 • MASSACHUSETTS Boston (617) 668-6891
NEW YORK/NEW JERSEY Morris Plains (201) 267-8805 • TEXAS Dallas (214) 980-9978

CIRCLE 129 ON INQUIRY CARD

CIRCUIT COMPONENTS

MINIATURE ILLUMINATED INDICATOR

Series 19 indicators offer round or square bezel; incandescent bi-pin lamp or red, yellow, or green LED; eight lens colors; and silver plated terminals for the lamp and for wire soldering of two #20 AWG wires. They mount in a 0.315" (0.800-cm) round hole as close as 0.354" (0.899 cm) on centers for multiple, limited space applications, and operate at temperatures from −25 to 45 °C. **EAO Switch Corp,** 255 Cherry St, Milford, CT 06460.

Circle 240 on Inquiry Card

AXIAL TANTALUM CAPACITORS

CA series solid tantalum capacitors are offered in a capacitance range from 1 to 47 mF. Tolerances of ±10% and ±20% are standard, with ±5% available as an option. Voltages range from 6.3 to 50 Vdc. Devices are encapsulated in a cylindrical metal case with epoxy end seal and inserted in an inert transparent plastic sleeve. Axial leads are tin-plated copper clad steel. Offered in 2 case sizes, capacitors can be supplied in bulk or on tape and reel for automatic insertion. **Thomson-CSF Components Corp, Passive Components Div,** 6660 Variel Ave, Canoga Park, CA 91303.

Circle 241 on Inquiry Card

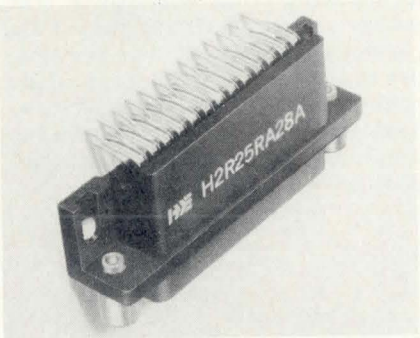
1% METAL FILM RESISTORS

Color coded CCF-55 resistors, available in 0.25-W, 125 °C and 0.12-W, 70 °C ratings, offer MIL-R-10509F type quality and performance. Std tempco is 100 ppm/°C. Physically protected by a conformal coating of flame retardant epoxy, resistors are produced in all EIA decade resistance values from 10 Ω to 1 MΩ, and are delivered in bulk or in tape and reel packaging for use with automatic insertion equipment. **Dale Electronics, Inc,** Dept 860, PO Box 609, Columbus, NE 68601.

Circle 242 on Inquiry Card

PACKAGING AND INSTRUMENTATION

SUBMINIATURE RIGHT ANGLE CONNECTORS



D subminiature right angle female connectors can be installed quickly on PC boards. Available with 1-piece, ultrasonically welded threaded inserts already attached, connectors are available with 9, 15, 25, or 37 positions for positive mating with all makes of D subminiature male plug connectors. **Holmberg Electronics Corp,** Asheville Hwy, Inman, SC 29349.

Circle 243 on Inquiry Card

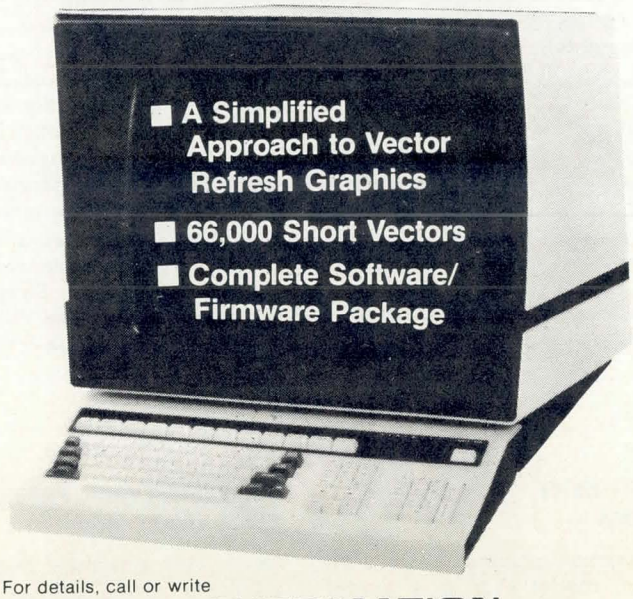
FLAT CABLE HEADERS AND SOCKETS

K series IDC flat cable headers and socket connectors are available with 10 to 60 contacts and meet MIL-C-83503 requirements; all MIL-SPEC socket connectors will mate, latch, lock, and key with series header. Series provides protection against mismating; a fourth side added to the header prevents socket connector from plugging into just one row of header pins. **Robinson Nugent, Inc,** PO Box 1208, 800 E Eighth St, New Albany, IN 47150.

Circle 244 on Inquiry Card

VECTOR AUTOMATION

GRAPHICUS-80

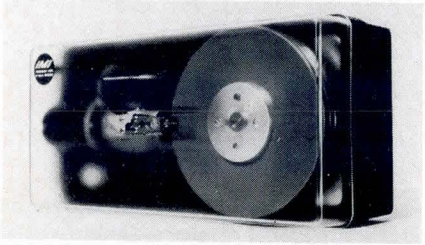


For details, call or write
VECTOR AUTOMATION, INC.
(301) 433-4202 Village of Cross Keys, Baltimore, MD 21210

CIRCLE 156 ON INQUIRY CARD

MEMORIES

40M-BYTE 8" WINCHESTER DRIVE



Model 7740 offers safety feature that protects against data loss or destruction and prevents head from being jarred or shocked during shipping. During normal shutdown or power failure, head assembly is automatically retracted so that heads touch down in nondata areas, and carriage assembly is locked in position. Other features include miniature voice coil actuator directed by closed loop servo system; brushless dc spindle motor; lightweight and high strength construction. **International Memories, Inc,** 10381 Bandley Dr, Cupertino, CA 95014.

Circle 245 on Inquiry Card

128k-BYTE RAM BOARD

Superstore is organized in blocks of 16k bytes that are divided into 2 64k memory blocks controlled by individual I/O ports. Used with 8-bit processors, memory is organized as 128k x 8 bytes, with 16-bit processors as 64k x 16 bytes. Board operates with any IEEE 696 S-100 system, and accepts extended 24-bit addressing or operates in bank select mode. Bank selection is made on 16k-byte boundaries. Access time is 330 ns; cycle time is 550 ns. **Piiceon, Inc,** 2350 Bering Dr, San Jose, CA 95112.

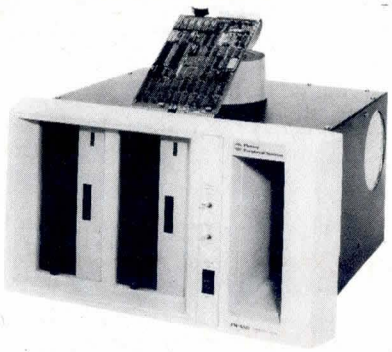
Circle 246 on Inquiry Card

MINI-FLOPPY DRIVE MECHANISMS

Mechanism-only versions of 6106/6108 disc drives, model 6107 is a single-head unit, the 6109, a double-head mechanical drive. With dimensions of 2.1 x 5.75 x 7.5" (5.3 x 14.6 x 19.0-cm), the drives occupy one-third less space than other units. For full compatibility, they are also offered with an optional 3.75" (9.5-cm) front panel. In existing dual-drive systems, use of three slim-design drives would permit a 50% increase in capacity to 1.5M bytes in the same packaging space. **BASF Systems Corp,** Crosby Dr, Bedford, MA 01730.

Circle 247 on Inquiry Card

DOUBLE-SIDED FLOPPY DISC SUBSYSTEMS



Double-sided, dual-density subsystem with 2 floppy disc drives, PM-XS31 is offered for use with PDP-11 computers. PM-XSV31 double-sided, dual-density system, consisting of dual-wide controller board and 1 or 2 floppy disc drives, is intended for use with the LSI-11. Standalone units include interface, formatting capability, power fail detection, write precompensation, and transparent firmware bootstrap circuitry. Disc capacity is 1M byte; max subsystem capacity is 2M bytes. **Plessey Peripheral Systems,** 1691 Browning Ave, Irvine, CA 92714.

Circle 248 on Inquiry Card

UNIVERSAL EPROM PROGRAMMING PERSONALITY MODULE

UN-3F can program most currently available NMOS EPROMs and future devices, including the 2716, 2758, 2732, 2732A, and 2764; TI's 2516, 2532, and 2564; and Motorola's 68764, without extra options. It can also program and erase Hitachi's 40816 EEPROM. The module's programming versatility combined with the portability of the PKW-7000 universal programmer makes field programming easier. Including the module, the programmer measures 11.4 x 7.5 x 2.5" (290 x 190 x 65 mm). **Intertek, Inc,** Naito Bldg, 7-2-8 Nishishinjuku, Shinjuku-ku, Tokyo, Japan 160.

Circle 249 on Inquiry Card

1M-BYTE ADD-IN MEMORY

PINCOMM 44S modules provide up to 1024k bytes on a single card and are hardware and software compatible with DEC PDP-11/44 minicomputers. Available in 512k-, 256k-, and 128k-byte increments, they are also compatible with regular or extended Unibus in systems other than PDP-11/44. Memory organization is 39 bits wide, consisting of two 16-bit data words plus 7 error correction check bits. Equivalent to DEC MS-11M (M7822), module occupies 1 slot in the computer. **Trendata Corp,** 3400 W Segerstrom Ave, Santa Ana, CA 92704.

Circle 250 on Inquiry Card

IBM COMPATIBLE TAPE DRIVE FOR HP-85

Model GPIB-1050 tape transport with board embedded formatter and IEEE 488 Std 1978 (HP-IB) microprocessor controller provides over 40M bytes of IBM compatible storage on a 10.5" (26.7-cm) reel with 2400' (720 m) of 0.5" (1.27-cm) tape. Data are recorded in IBM compatible 9-track (NRZI) 800 or 1600 char/in (315 or 630/cm) at 45" (114 cm)/s. Transport is software and hardware compatible with HP85 computers. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.

Circle 251 on Inquiry Card

New Holmberg D Subminiatures slash in-place costs!

New Holmberg D Subminiature Right-Angle Female Connectors install faster!

They're available with unique, one-piece, ultrasonically welded threaded inserts already attached. So there's no need to fumble with loose washers and nuts. And Holmberg's hardware doesn't encroach on mounting holes — so you have a clear path for bolting or riveting the connector to your PC board.

Look closely at the superior quality throughout. Like the high-dielectric, glass-filled polyester housing. Solder-plated contact tails are tough and rigid — no need for a supporting "barrier." Large, conical holes guide male pins for easy, sure mating. And the connectors can be delivered with your choice of selective gold in the contact area.

Take your choice of new Holmberg D Subminiature Connectors for fast delivery. In 9, 15, 25 or 37 positions for positive mating with *all* D Subminiature male plug connectors. With your choice of hardware and plating.

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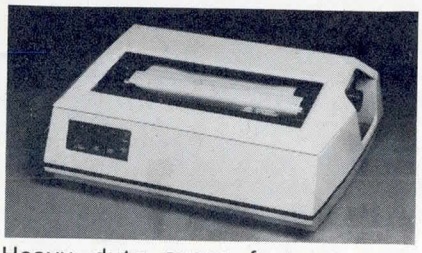
Irvine, California 92714
(714) 556-2930

CIRCLE 131 ON INQUIRY CARD

PRINTERS/PLOTTERS

160-CHAR/s SERIAL MATRIX PRINTER

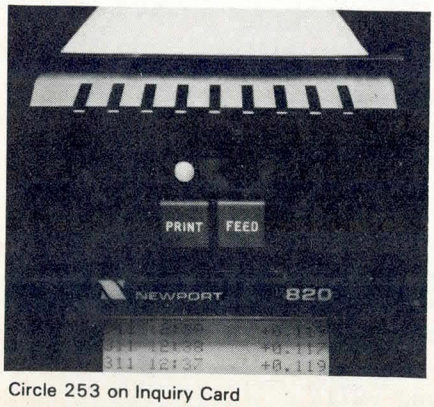


Heavy duty P1600 features compressed print mode, double-width characters, 7 x 7 dot matrix with upper- and lowercase characters, serial RS-232 communications interface, monitor mode, and escape code sequences. Operation can be controlled locally or by host processor. Unit is compatible with DM3270 control unit display station and completes the workstation when used with Micro 4400 data communication terminal. **Beehive International,** 4910 Amelia Earhart Dr, Salt Lake City, UT 84125.

Circle 252 on Inquiry Card

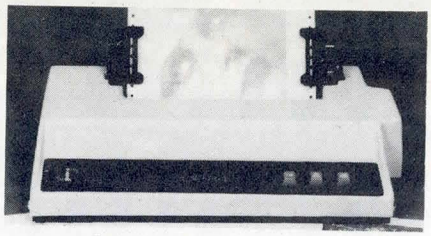
THERMAL DATA PRINTER

Designed for use with instruments having BCD outputs, model 820 prints 20-col lines in a 5 x 7-dot matrix at up to 1.5 lines/s. Unit has 4 basic switch-selectable operating modes: BCD character parallel and serial, system, and test. Std features include selection of 16 time delays between print cycles, out of paper indicator light and automatic print cycle interruption, symbols to annunciate overload and alarms, and 210 combinations of special characters for units of measure. **Newport Electronics, Inc,** 630 E Young St, Santa Ana, CA 92705.



Circle 253 on Inquiry Card

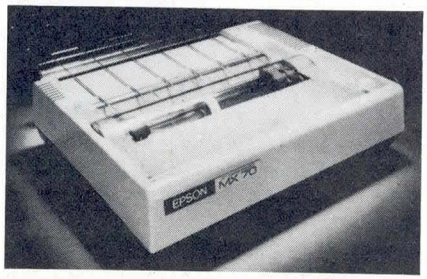
GRAPHIC PRINTER



DIP-84G features 7 x 7 or 14 x 7 dot matrix, 6 char sizes, 100-char/s bidirectional print speed, selectable tractor or friction paper feed, and long-life ribbon cartridge loading. It has variable line density and continuous form length controls, and can be operated at 100% duty cycle continuously without overheating. High resolution dot addressable graphic capability can plot, print CRT screen graphics, draw illustrations, and produce special effect symbols. With 96-char ASCII set, it provides both upper- and lowercase printing at 40, 48, 66, 80, 96, or 132 chars/line. **DIP, Inc,** 745 Atlantic Ave, Boston, MA 02111.

Circle 254 on Inquiry Card

LOW COST DOT MATRIX IMPACT PRINTER



MX-70 features Micro-Nine disposable printhead that can be snapped out and thrown away after it has reached its 50M- to 100M-char life expectancy; replacement requires less than 1 min. The printer outputs unidirectionally at 80 chars/s with a user defined choice of 40- (double-width char) or 80-col printing. It provides top of form recognition, programmable line feed and forms length, self-test mode, and an adjustable tractor feed. It prints on plain paper using an easy to read 5 x 7 matrix. Graftrax II, a high resolution (60 dots/in) function, is standard on the unit. Dot placement accuracy of this feature provides bit image graphics that are free of jitter, wander, and walk, and results in better definition. **Epson America, Inc,** 23844 Hawthorne Blvd, Torrance, CA 90505.

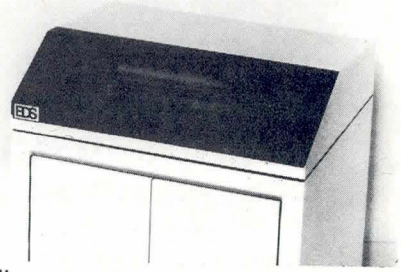
Circle 255 on Inquiry Card

RECEIVE-ONLY GRAPHICS PRINTER TERMINAL

LA34-VA, -WA, and -RA models of the DECwriter IV terminal provide graphics output and extension to conventional send/receive control logic. The 3 receive-only graphics output terminals reproduce the screen display from a raster scan video terminal. The XL extended logic option can be installed in model AA terminals in the field or ordered with the terminals. All 3 graphics terminals operate from printer ports of VT100, VT132, and VK100 video terminals or directly from a host computer. -RA is the basic version, -VA is intended for high resolution graphics and uses roll paper, and -WA provides both alphanumeric and graphics output on tractor feed paper. The extended logic options provide capabilities such as keyboard-selectable baud rates (which can be split baud rates), a range of 50 to 9.6k baud, auto-answerback, and a variety of character sets. The set-up feature is controlled from the keyboard, and is nonvolatile, so that turning off the terminal will not lose selected parameters. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 256 on Inquiry Card

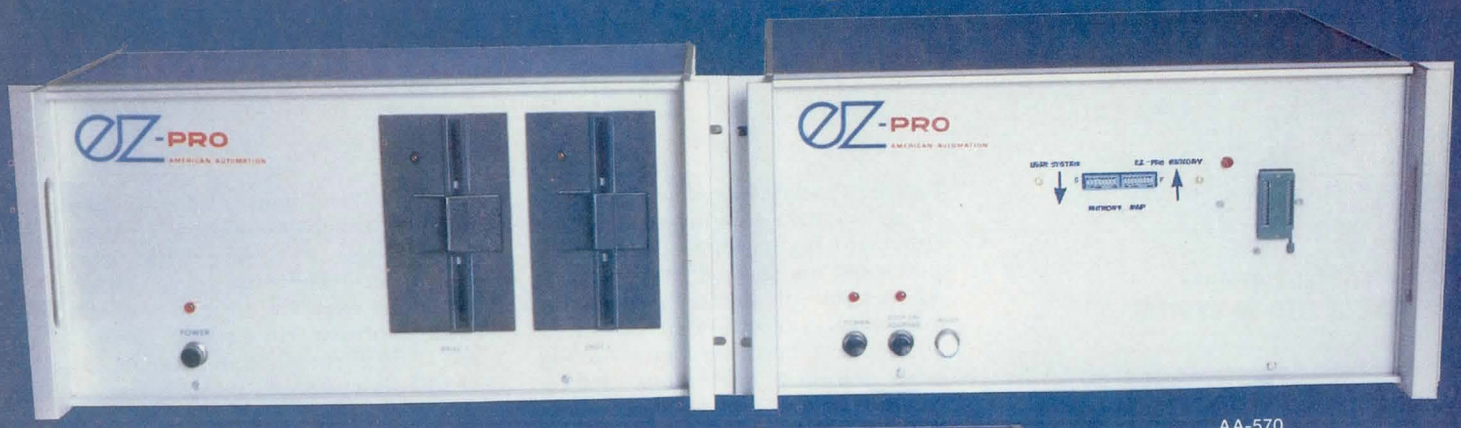
900-LINE/MIN BAND PRINTER



Microprocessor controlled model 900 operates at 1100 lines/min with 48-char set, 900 lines/min with 64-char set, and 672 lines/min with 96-char set printing 10 char/in (3.9/cm) horizontal and 6 or 8 lines/in (2.3 or 3.1/cm) vertical. Printer incorporates diagnostic routines and dual-digit status display that lets operators pinpoint and correct minor problems. Paper slew is 15″ (38 cm)/s with max single-line advance of 18 ms. Noise levels are less than 60 dB. Max power requirement is 600 W at 90 to 132 V, 60 Hz; 180 to 250 V, 50 or 60 Hz is optional. **BDS Computer Corp,** 1120 Crane St, Menlo Park, CA 94025.

Circle 257 on Inquiry Card

The EZ-PRO Development System



AA-591
Dual Disk

AA-570
Basic Development
Unit

AA-580 Interface Module equipped with eight AA-582 Memory Modules — used with bit slice systems.

THE EZ-PRO SYSTEM FEATURES:

Fixed Word Length Processors

- EZ-PRO supports a bunch and the bunch is getting bigger fast. Right now it's the Z80, 6800, 6802/8, 6805/146805, 6809, 6502/12, 6503-15 family, 3870/2/4/6, 8080, 8021, 8085, 8048 family. All are supported with real time in-circuit emulators.
- Emulators — Master/Slave type — Every resource in each slave is available to the user system including all interrupts and stack pointers.
- Trace and Logic Analyzer capabilities of course.
- EPROM Programmer, 2716 and 2732. Adaptor for 8748.
- Complete Software Support — Each emulator is provided with a Relocating Macroassembler, Linking Editor, Debugger and a DEMO program to show how the software is used. Higher level languages available include PASCAL and STRUBAL.

Bit Slice Processors

- EZ-PRO supports them all — You name it — 2, 4 or 8 bits wide — ECL or TTL.
- Microprogram word widths from 16 to 128 bits — Depths to 8K words.
- Bipolar PROM Programmers — ECL or TTL — 4 and 8 bit wide PROMs — intermixed if you like — Fast enough for production — Gang program 8 PROMS at a time with a single programmer.
- Complete Software Support — You'll have to experience it to believe the power and ease of use of AABASM, our Meta Assembler — And the rest of the software has the same standard of excellence.

The Basic EZ-PRO System

- 32 KB of static memory, expandable to 80 KB.
- Two RS-232 ports with selectable baud rates — one for a high speed printer and the other for a video terminal — Current loop port also provided.
- Choice of floppy disk capacities.
- Software provided for use on all systems includes a Resident Monitor, Disk Operating System, Disk Formatter and an Editor.

Prices

A complete EZ-PRO system equipped with one in-circuit emulator, dual disk unit, printer and video terminal sells for about $8,500. Bit Slice systems start at about $11,000.

What to do now that you're semi-sold . . .

Write or call us if you need more information. Then order a system at no risk. Advise us within 28 days of shipment from our plant that you don't want the system and return it to us in an undamaged condition within 35 days and we'll promptly return your money.

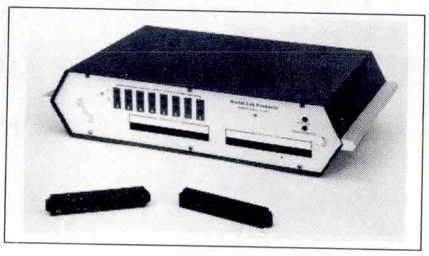
AMERICAN AUTOMATION

14731 Franklin Ave. • Tustin, California 92680 • (714) 731-1661 TWX 910-595-2670

CIRCLE 132 ON INQUIRY CARD

DATA ACQUISITION AND CONTROL

INTELLIGENT REMOTE DISTRIBUTED I/O SYSTEM



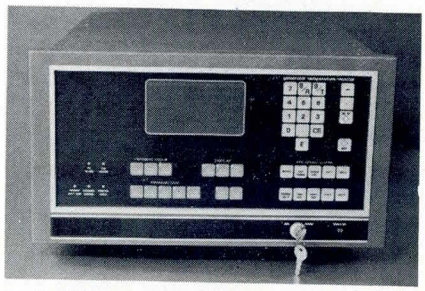
Compatible with any computer or terminal that has a supported RS-232-C port, devices provide both analog and digital I/O and meet RS-423 requirements for long distances. SL-800 series Intelligent Remote Serial I/O units can share the same line with a terminal or operate from a separate RS-232-C/RS-423 port. They are completely transparent when not executing commands. The self-contained standalone units with enclosure and power supply operate from the 120-Vac line, and provide 8 channels of digital output. **Serial Lab Products, Inc,** PO Box 766, 50 Brigham St, Marlboro, MA 01752.
Circle 258 on Inquiry Card

DATA ACQUISITION AND PROCESSING SYSTEM

A programmable transient data acquisition instrument for high speed laboratory or remote digital logging of data, the portable ALN 4000 offers an 8-bit A-D converter with software-selectable sampling, recording of up to 4k samples/transient at selectable rates between 156 kHz and 20 MHz, separate Z80A microprocessors for data acquisition control and data processing, and onboard processing architecture that eliminates recording of unneeded data and preserves significant events for later recall. Interaction between user and data logger is maintained via a handheld keyboard with alphanumeric display or other ASCII terminal. A built-in 20-col alphanumeric printer verifies instructions and provides local tabulation of portions of collected data. Data are stored on dual digital 3M tape cartridges at approximately 150k bytes/tape for transfer to a remote data logger or a computer on an RS-232-C communications link. Other std features include a 12-bit, 8-channel multiplexed A-D converter, 128k bytes of memory, high speed multiplier/accumulator units, 6 arithmetic processing units to augment the microprocessors, and an 8-channel D-A converter for data display. **Adaptronics, Inc,** 1750 Old Meadow Rd, McLean, VA 22102.
Circle 259 on Inquiry Card

TURNKEY INDUSTRIAL CONTROL SYSTEM

Low noise industrial Cyberbus serves as the basic element of RTC4000 modular microcomputer control system. Circuit modules, including CPU, digital and analog I/O, memory, communications, and power supply, plug directly into the bus. System features high noise resistance, low crosstalk, memory mapped I/O, DMA, and 16-bit data bus. Std control algorithms are supplied, and application specific software is added to tie modules together and obtain desired operation. **Electronic Management Systems, Inc,** 5439 Seward, Omaha, NE 68104.



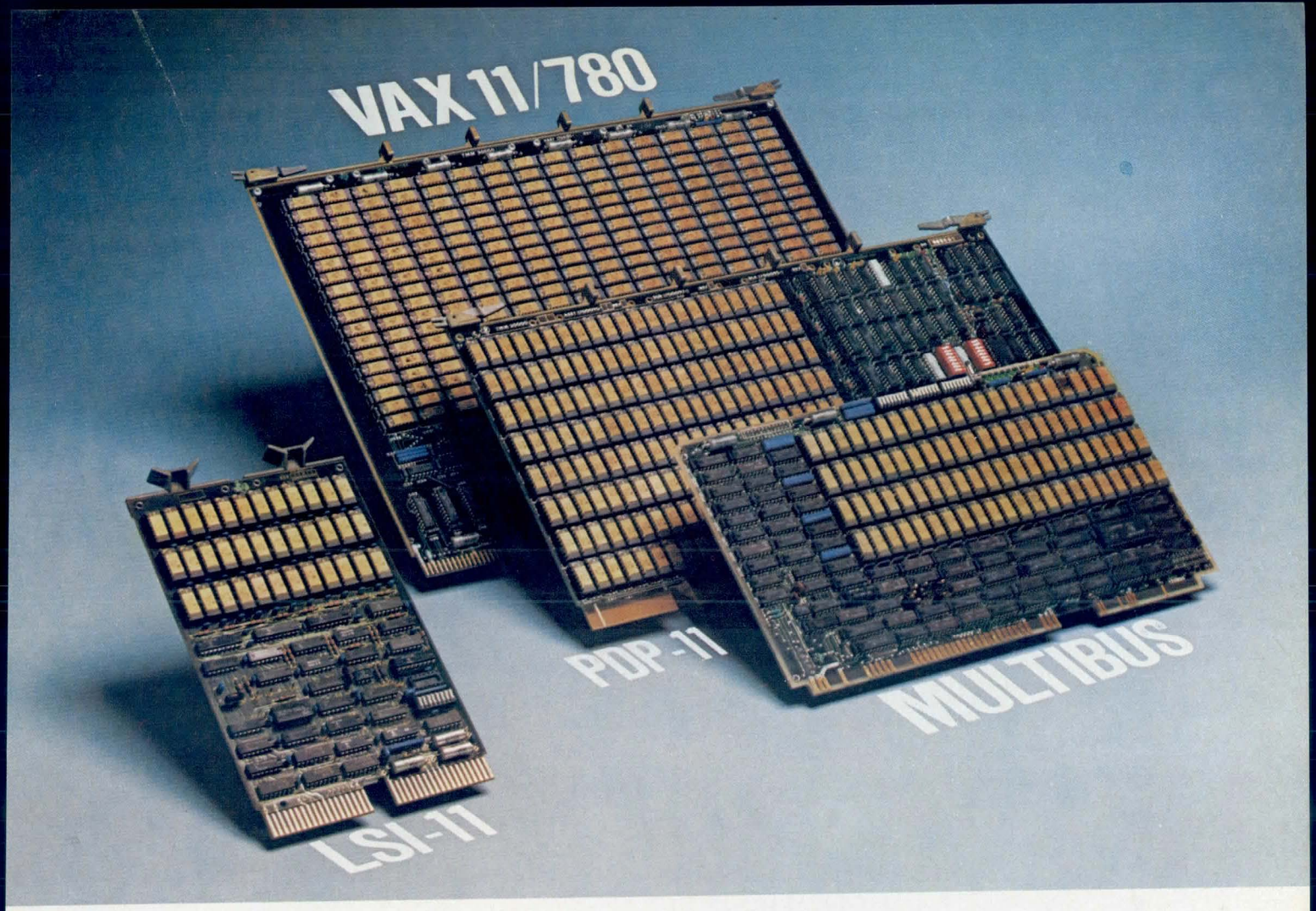
Circle 260 on Inquiry Card

ANALOG DATA ACQUISITION SYSTEM

Analogger I combines computational and control power of Apple II Plus computer with precision analog measurement system. Data logging is possible with printer, tape cassette, disc, or combinations; 48k-byte RAM allows development of process control functions and storage of data. Analog scanner interface is written in machine language and memory mapped. Complete system includes Apple II Plus, CRT display, floppy disc drive, clock/calendar, parallel interface, card cage for I/O modules, and Level 1 software on diskette. **Sanlab, Inc,** 7969 Engineer Rd, San Diego, CA 92111.
Circle 261 on Inquiry Card

CONTROL PROGRAMMER I/O ENHANCEMENTS

Mixed input and output capabilities for the company's DCP 7700 digital control programmer line have been added to models that feature single-variable setpoint vs time programmer with 2 or 3 controllers combined into a single digital instrument and to multiple-programmer/multiple-controller instruments. Inputs on multiple-setpoint programmer models can be from different type sensors; inputs for relative humidity are wet bulb and dry bulb temperature from platinum RTDs, and output on the multiple-controller instruments can be current, voltage, position, time, or duplex time proportional. Built-in low power relays for switching of remote start, hold, and reset functions eliminate the need for gold plated relay contacts at remote function terminals. On the setpoint programmer, 9 programs with more than 200 functions can be stored in a nonvolatile memory and accessed through a front keyboard. On multiple-setpoint program instruments, a program consists of a subprogram entered on each channel. The controller section of the front panel displays the controller output in percent, the value of the process variable in engineering units, and the number of the programmer/controller being monitored. **Honeywell Process Control Div,** 1100 Virginia Dr, Fort Washington, PA 19034.
Circle 262 on Inquiry Card



TI leadership. In 64K DRAM technology. In Memory Systems.

Whatever bus you're using — VAX†, PDP-11†, LSI-11†, or even Multibus‡ — TI can supply add-in memory system boards with dynamic RAMs from our own high-performance 64K series.

When you specify TI's high-density, low-power boards, you save rack space. So you have more room for I/O — or whatever else you need. And, the low-power consumption of TI 64K DRAMs, compared to the old-fashioned 16Ks, cuts temperature levels and increases reliability. The reduction in memory package count by as much as four boosts reliability even more.

System reliability will be higher, too. Thanks to error correction/detection available on many TI memory boards. Using our own bipolar EDAC chip helps cut component count and system temperature, as well as improving basic system reliability. The EDAC chip replaces about a quarter of a board of TTL circuitry.

All TI boards are 100% tested. 100% burned-in. All in TI's modern, high-capacity Houston facility. Delivery normally ranges from stock to four weeks.

Low cost

Representative pricing* for TI memory boards is as follows: $1600 for TMM10000-04 (192KB); $3800 for TMM20000-02 (256KB); $9000 for TMM30000-01 (1MB); $1845 for TMM40010-07 (64KB).

TI MEMORY BOARDS — CURRENT AVAILABILITY

System	TI Series	BYTES/BOARD						
		64K	128K	192K	256K	512K	768K	1M
LSI-11†	TMM10000[1]		X	X	X			
PDP-11†	TMM20000[2]		X	X	X	X		X
VAX†	TMM30000					X	X	X
Multibus‡	TMM40010[2]	X	X		X	X		

[1] Parity optional [2] EDAC standard

Custom capability

If you need custom memory systems in production quantities, be sure and talk to TI. We'll custom design boards for specific applications with the same meticulous attention to cost/performance effectiveness that our standard boards offer.

So for the latest DRAM technology, highest packing densities, lowest power consumptions, all at competitive prices, remember memory systems from Texas Instruments.

To find out more about TI boards call your local TI field sales office or authorized distributor. For details, call (713) 778-6549, or write to Texas Instruments Incorporated, Integrated Memory Systems, P.O. Box 1443, M/S 6404, Houston, Texas 77001.

†Trademark Digital Equipment Corp.
‡Trademark Intel Corp.
*U.S. Single-unit price, subject to change without notice.

TEXAS INSTRUMENTS
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CIRCLE 133 ON INQUIRY CARD

85215

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Dialight sells only used rockers and toggles.

That's because all are 100% tested. At Dialight we don't use hit-or-miss sampling to test our miniature rockers and toggles. All are 100% tested electrically and mechanically before you get them. And all are made in the U.S.A.

You can choose from thousands of different designs. Our rocker and toggle line contains countless combinations of standard colors, sizes, mountings and contact ratings. Included are dozens of front-panel and sub-panel types, plus many styles for snap-in and printed circuit board applications.

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Next time specify only used switches—100% tested rockers and toggles from Dialight, 203 Harrison Place, Brooklyn, N.Y. 11237 (212) 497-7600.

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CIRCLE 134 ON INQUIRY CARD

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A sleek graceful sailing vessel glides across the sometimes green, sometimes blue Caribbean. The cargo: you. And an intimate group of lively, fun-loving shipmates.

Uniform of the day: Shorts and tee shirts. Or your bikini if you want. And bare feet.

Mission: A leisurely cruise to remote islands with names like Martinique, Grenada, Antigua—those are the ones you've heard of. Before the cruise ends, you'll

know the names of many more. You'll know intimitely the enchanting different mood of each...and its own beauty and charm.

Life aboard your big sailing yacht is informal Relaxed. Romantic.

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Spend 6 days exploring paradise. Spend six nights watching the moon rise and getting to know interesting people. It could be the most meaningful experience of your life ...and it's easily the best vacation you've had.

A cruise is forming now. Your share from $400. Write Cap'n Mike for your free adventure booklet in full color.

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LITERATURE

Multibus Compatible Devices

OEM microcomputer board products, disc drives, MDS hardware and software, 8- and 16-bit development systems, and design aids are detailed in photos, diagrams, and charts of 56-p catalog. **Zendex Corp,** Dublin, Calif.

Circle 281 on Inquiry Card

Switching Power Supplies

Incorporating case, pin, and socket configurations, block diagrams, and photos, 54-p handbook details electrical and mechanical parameters of ac-dc and dc-dc power supplies. **Power General,** Canton, Mass.

Circle 282 on Inquiry Card

Converters

Hybrid and modular synchro devices are presented in 3-ring binder that includes specs, as well as design and applications information. **Natel Engineering Co, Inc,** Canoga Park, Calif.

Circle 283 on Inquiry Card

Silicon Power Semiconductors

Cross-reference guide lists over 10,000 rectifiers, transistors, and assemblies, and presents detailed dimensional drawings of package outlines. **Westinghouse Electric Corp,** Youngwood, Pa.

Circle 284 on Inquiry Card

Circuit Breakers

Using curves and tables on dimensions, delay curves, rating, decision tables, photos, and block diagrams, handbook/catalog covers spectrum and applications of industrial and military devices. Apply on letterhead to: Mr Robert Cox, **AIRPAX, Cambridge Div,** Woods Rd, Cambridge, MD 21613.

Power Plate Resistors

Technical bulletin tabulates specs for current sense and surge resistors, outlining typical applications. **Vishay Resistive Systems Group,** Malvern, Pa.

Circle 285 on Inquiry Card

Read/Write IC

Designed for 8" (20-cm) and 5.25" (13.34-cm) Winchester disc drive magnetic recording heads, 5-channel model 115 is described in spec sheet that includes block, pin configuration, and timing diagrams. **Silicon Systems Inc,** Tustin, Calif.

Circle 286 on Inquiry Card

Data Communication Devices

Photos, diagrams, and specs in 44-p catalog present 107 data communication products for use in 167 models. **Expandor Inc,** Pittsburgh, Pa.

Circle 287 on Inquiry Card

Fractional Horsepower Motors

Drip-proof and enclosed motors are described in bulletin that contains charts of torque curves, ratings, and dimensions, cooling system, and mounting information. **Gould Inc, Electric Motor Div,** St Louis, Mo.

Circle 288 on Inquiry Card

Switches

Engineering specs and drawings, and reference chart provide information on five types of thumbwheel, leverwheel, and pushwheel switches. **Cherry Electrical Products Corp,** Waukegan, Ill.

Circle 289 on Inquiry Card

Capacitors

Specs, configuration and dimensional drawings, performance curves, and values for each type are listed in 16-p catalog to describe range of capacitors. **International Components Corp,** Melville, NY.

Circle 290 on Inquiry Card

Cable Tap and Splitter/Combiner

Brochure uses diagrams, photos, and specs to describe coaxial cable tap and passive fiber optics splitter/combiner. **AMP, Inc,** Harrisburg, Pa.

Circle 291 on Inquiry Card

Terminals and Peripheral Devices

Full-color photos and spec charts detail terminal and hardcopy peripheral product line. **Hewlett-Packard Co,** Palo Alto, Calif.

Circle 292 on Inquiry Card

Modular Power Supplies And Converters

Catalog contains circuit characteristics, operational features, photos, and engineering drawings for line of dc-dc and ac-dc supplies. **Intronics, Inc,** Newton, Mass.

Circle 293 on Inquiry Card

Disc Drives

Multicolor brochure uses photos to depict product procedures and device characteristics of 5.25" micro-Winchester™ disc drives. **Seagate Technology,** Scotts Valley, Calif.

Circle 294 on Inquiry Card

Enclosures

Std and custom deep drawn enclosures, commercial, industrial, and military carrying cases, electronic cabinets, chassis, slides, and blowers, as well as modular containers, are included in product catalog. **Zero Corp,** Burbank, Calif.

Circle 295 on Inquiry Card

Voice Digitizing and Compression Techniques

Multicolored brochure uses charts and block diagrams to illustrate techniques that provide telephone security and high quality speech reproduction. **GTE, Sylvania Systems Group, Communication Systems Div,** Needham, Mass.

Circle 296 on Inquiry Card

Concepts and Terminology Guide

Switch, relay, connector, and circuit breaker information is presented in 36-p basic guide that includes glossaries, std and spec guides, conversion data, and resistance values. **Peerless Radio Corp,** Lynbrook, NY.

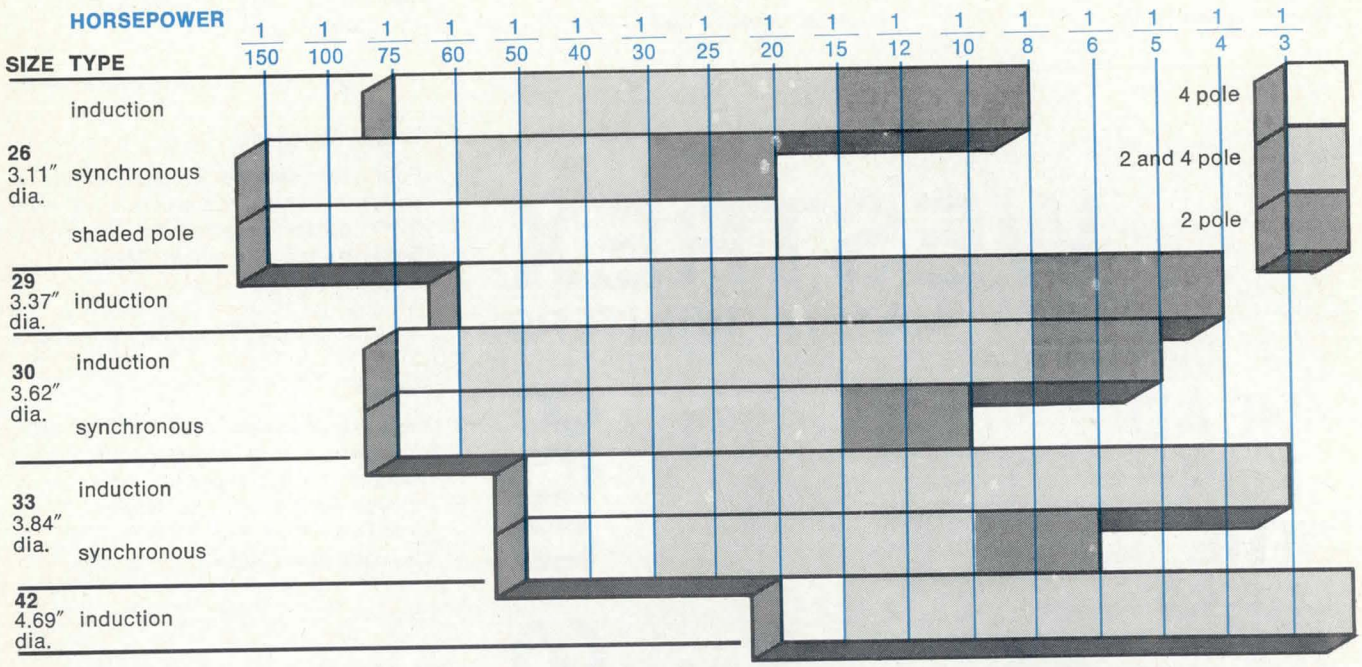
Circle 297 on Inquiry Card

Power Supplies

Catalog provides general specs and outline dimensions for open frame switching and linear power supplies, as well as custom, OEM linear, floppy disc, microprocessor, Micro-Reg low power, and S-100 bus supplies. **Sierracin/Power Systems,** Sylmar, Calif.

Circle 298 on Inquiry Card

The right motor for you



How can you design the right AC motor into your new equipment? Check the speed-HP envelopes above, then ask Robbins & Myers for exactly what you need. You will get precisely the speed, performance, features, and long life you require. Superior manufacturing technology then yields consistent motors from production lot to lot.

This approach differs from motor manufacturers who may force you into their standards rather than match your application needs. It's one reason Robbins & Myers motor customers return again and again; the motors help them build a trouble-free reputation. Request catalog D-1120 from Electric Motor Division, Robbins & Myers, Inc., 1345 Lagonda Ave., Springfield, OH 45501. Tel. 513-327-3329.

ROBBINS MYERS

CIRCLE 136 ON INQUIRY CARD

Software

Catalog details information about C and Pascal compilers, crosscompilers, and Iris operating system for mini- and microcomputers. **Whitesmiths, Ltd,** New York, NY.

Circle 299 on Inquiry Card

Backplanes

Brochure featuring spec tables and diagrams describes PDQ/DSC DEC compatible pressfit backplanes. **Stanford Applied Engineering, Inc,** Santa Clara, Calif.

Circle 300 on Inquiry Card

Digital Signal Processing

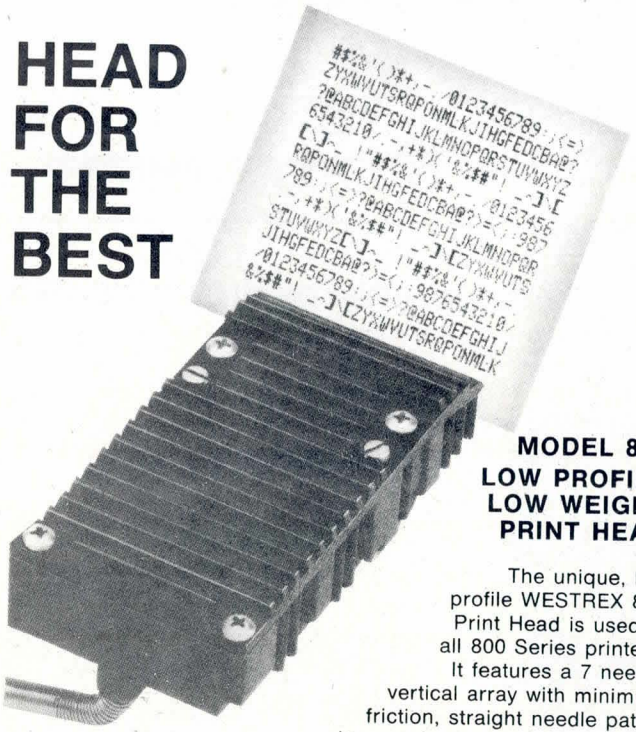
Application note explains use of TDC1023J all-digital correlator, as well as basic theory of correlation; systems and timing diagrams illustrate text. **TRW LSI Products,** La Jolla, Calif.

Circle 301 on Inquiry Card

WESTREX
DOT MATRIX PRINTERS

HEAD FOR THE BEST

800 SERIES



MODEL 801
LOW PROFILE
LOW WEIGHT
PRINT HEAD

The unique, low profile WESTREX 801 Print Head is used in all 800 Series printers. It features a 7 needle vertical array with minimum friction, straight needle paths, low power consumption, a 100% duty cycle and an average life of 100 million characters.

WESTREX 800 Series of 150 character per second, alphanumeric bi-directional printers include split platen, flat bed slip/document and 51 to 96 column journal printers in a variety of standard models to suit many OEM applications. All utilize the same simple, reliable drive system, head position sensors, ribbon transport mechanism and other quality tested components for maximum cost effectiveness.

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IN SWEDEN — WESTREX OEM PRODUCTS
Box 3503, S-17203 Sundbyberg, Sweden 46/8+981100

Power Supplies

Four-color handbook details electrical and mechanical parameters of over 200 power conversion products. **Datel-Intersil,** Mansfield, Mass.

Circle 302 on Inquiry Card

Relays

Catalog features drawings, charts, diagrams, and tables describing AGASTAT[R] pulse counting, timer delay relays. **Amerace Corp, Control Products Div,** Union, NJ.

Circle 305 on Inquiry Card

Heat Sinks

Design guide provides data and specs for custom, aluminum extruded heat sink shapes. **Aham Tor Inc,** Rancho California, Calif.

Circle 304 on Inquiry Card

Data Logger

Charts, photos, and diagrams present design information and application for Digitrend[R] 235 in 20-p, 2-color brochure. **Doric Scientific, Emerson Electric Co,** San Diego, Calif.

Circle 303 on Inquiry Card

Relays and Switches

Tables, diagrams, and photos describe line of dry reed and mercury wetted devices in 14-p catalog. **Socapex,** Canoga Park, Calif.

Circle 306 on Inquiry Card

Computer Repairs

Illustrated brochure describes how OEMs and end users can save money on computer repairs. **Digital Data Systems, Inc,** Plantation, Fla.

Circle 307 on Inquiry Card

COMPARE PRINTER TERMINALS AND BE CONVINCED

After you compare* features and performance...then look at price. With the Digi-Data Model 2516 KSR printer terminal, you get more value at 16 to 30% lower cost.**

For that Receive Only application, our 2511 RO provides similar advantages. And once your Series 2510 is installed, you have the reliability of fewer components with no cooling fan required... and the serviceability of a single board controller.

After you compare, we know you'll be convinced... the Digi-Data 2516 is "FIRST IN VALUE".

DIGI-DATA CORPORATION
8580 Dorsey Run Road, Jessup, MD 20794
(301) 498-0200
...First In Value

*Specifications and pricing obtained from vendor literature for comparably equipped units.
**Substantial OEM quantity discounts available.

Printing Terminal
VALUE COMPARISON

	DIGI-DATA 2516	TI 820	Tally T1612	HP 2635B
SPEED [Characters/sec]	150-200	150	160	180
SIZE Width	21.9"	26.0"	25.5"	25.2"
SIZE Depth	18.5"	21.0"	27.0"	23.0"
SIZE Height	8.5"	8.2"	8.5"	8.5"
WEIGHT [lbs]	39	40	69	56
Maximum BAUDRATE	19200	9600	9600	9600
EXTENDED BUFFER CAPABILITY	Yes	No	Yes	No
PRICE	$2150.	$2545.	$2605.	$3950.

DIGI-DATA CORPORATION
...First in Value!

CIRCLE 137 ON INQUIRY CARD

ACCORDING TO THE LATEST FIGURES, 37% OF ALL U.S. PATENTS WERE ISSUED TO FOREIGN CITIZENS.

In 1979, 37% of the newest ideas in this country didn't come from this country.

Many of them came from industrial rivals, eager to whittle down the technological lead that our country has held for so long. The largest share of U.S. patents went to Japan. The second largest share went to West Germany.

These and other countries seek U.S. patents in the hope of obtaining exclusive manufacturing rights to certain types of products here. This is especially worrisome in light of our determination to become less dependent on foreign goods.

Alarming as these patent figures are in themselves, they are even more alarming as symptoms of an overall decline in American technological innovation.

What can we do to reverse this decline? One of the most important things is to make sure that our colleges and universities continue to be strong. Our colleges and universities are vitally connected to every aspect of American science and engineering and business.

Most of the technology we have today is based on research generated by American colleges. Most of our great minds were educated there.

Unfortunately our colleges are being hurt by inflation.

So please make sure that your company is giving as much as it can, as much as it should, to the college or colleges of its choice.

America doesn't have a patent on ingenuity.

Send for our free booklet, "How to Develop an Effective Program of Corporate Support for Higher Education." Write CFAE, 680 Fifth Ave., New York, N.Y. 10019.

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GIVE TO THE COLLEGE OF YOUR CHOICE.

COMPUTER DESIGN ANNOUNCES...

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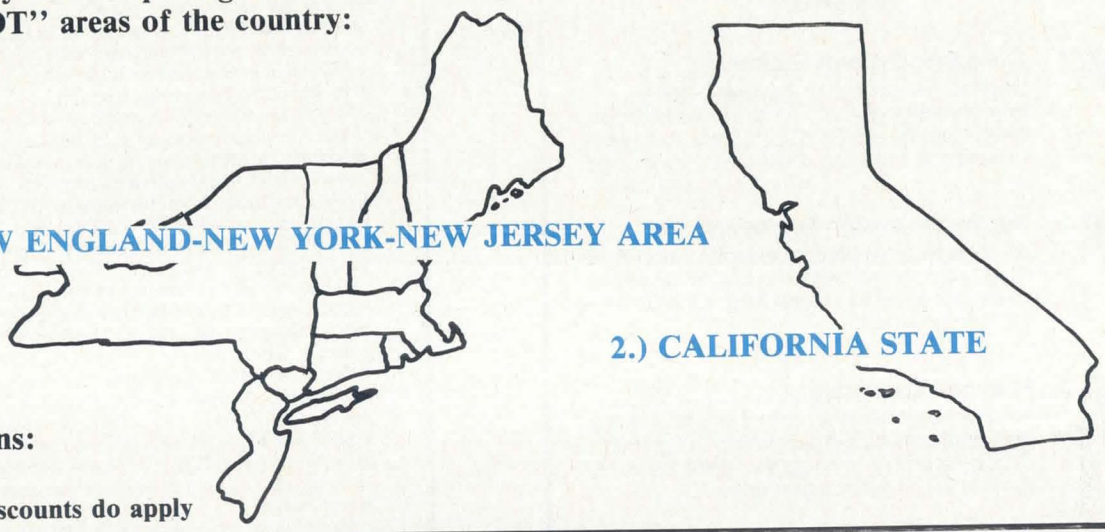

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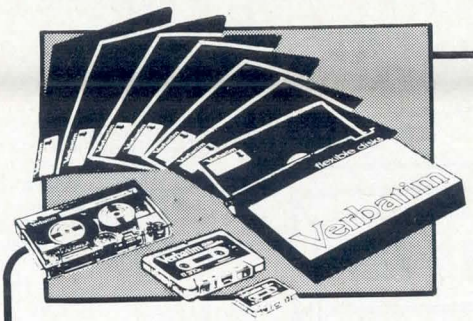

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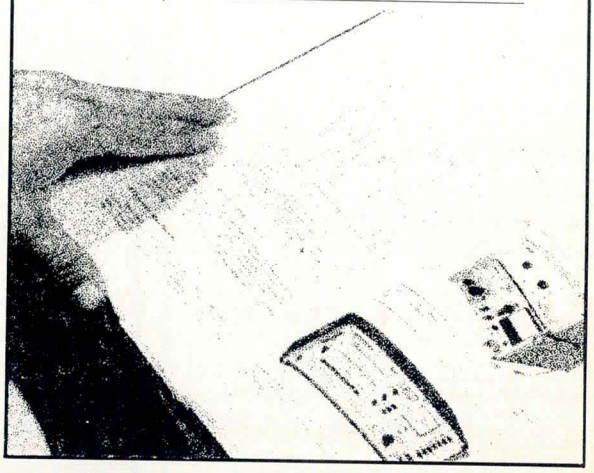

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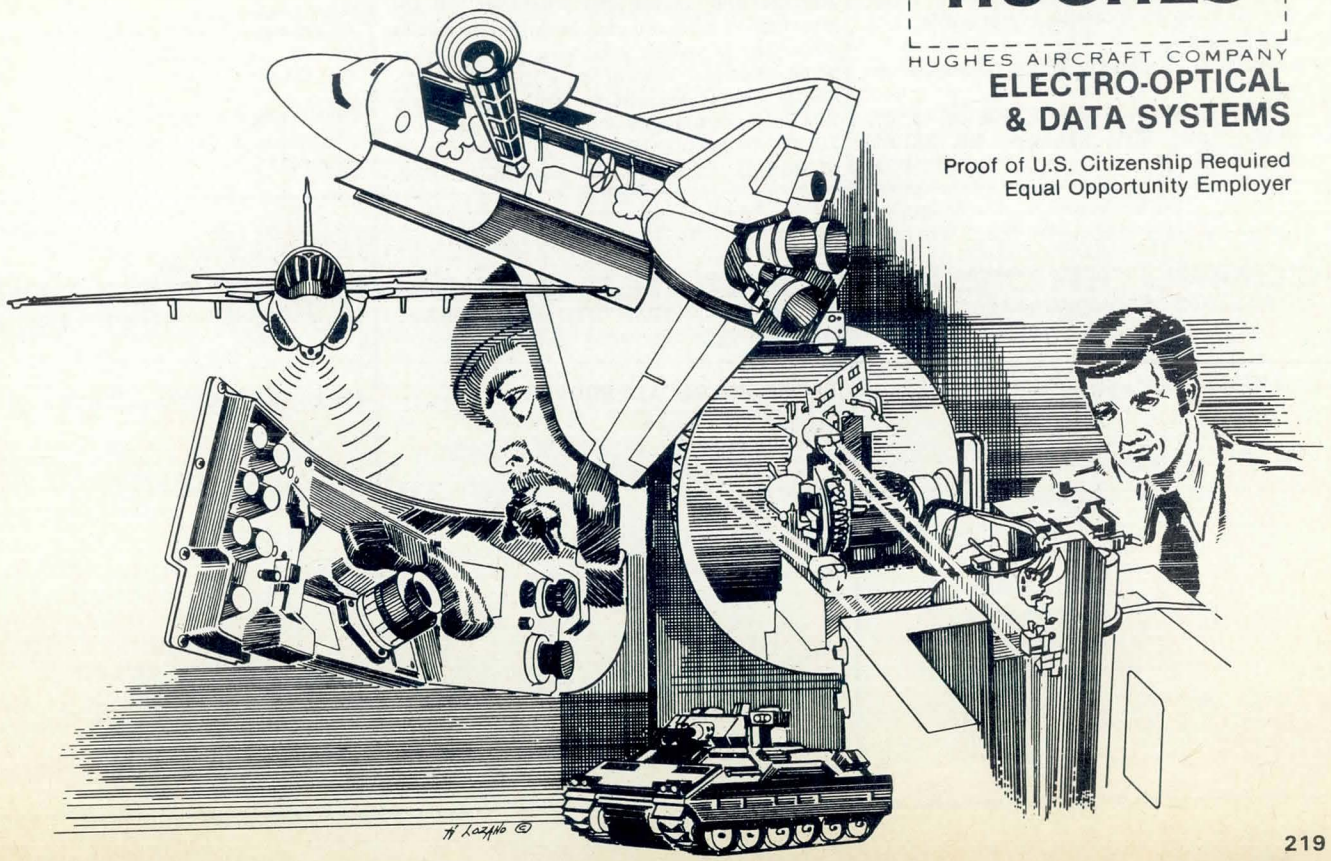

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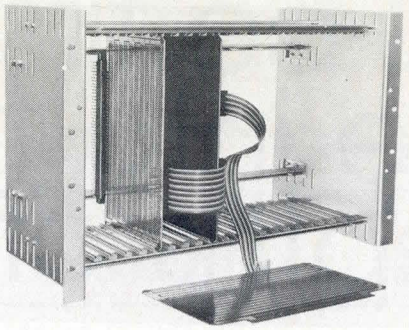

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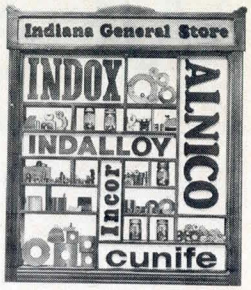

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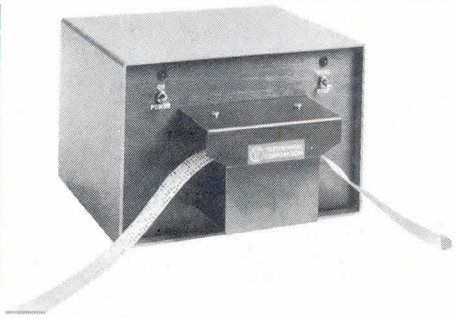

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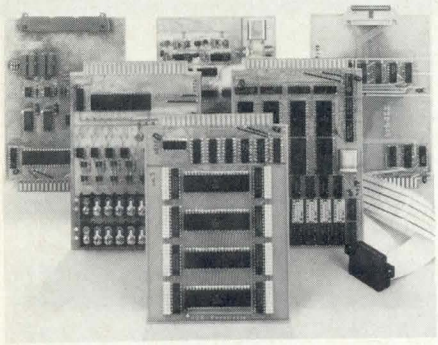

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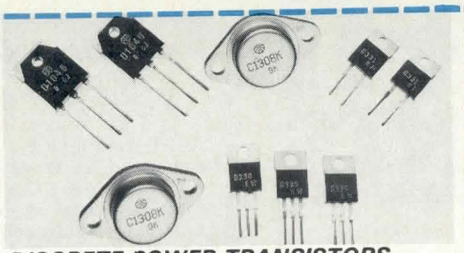

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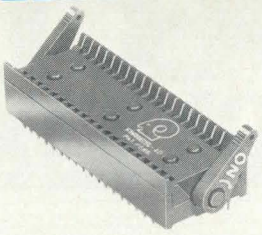

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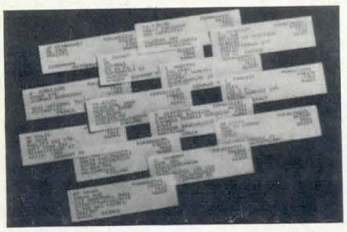

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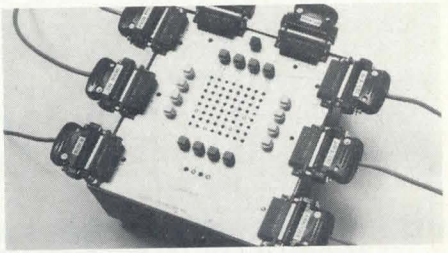

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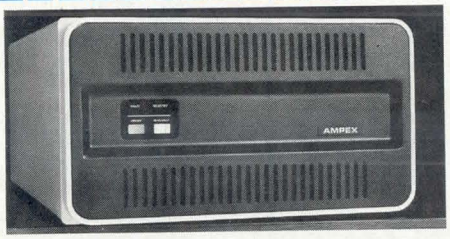

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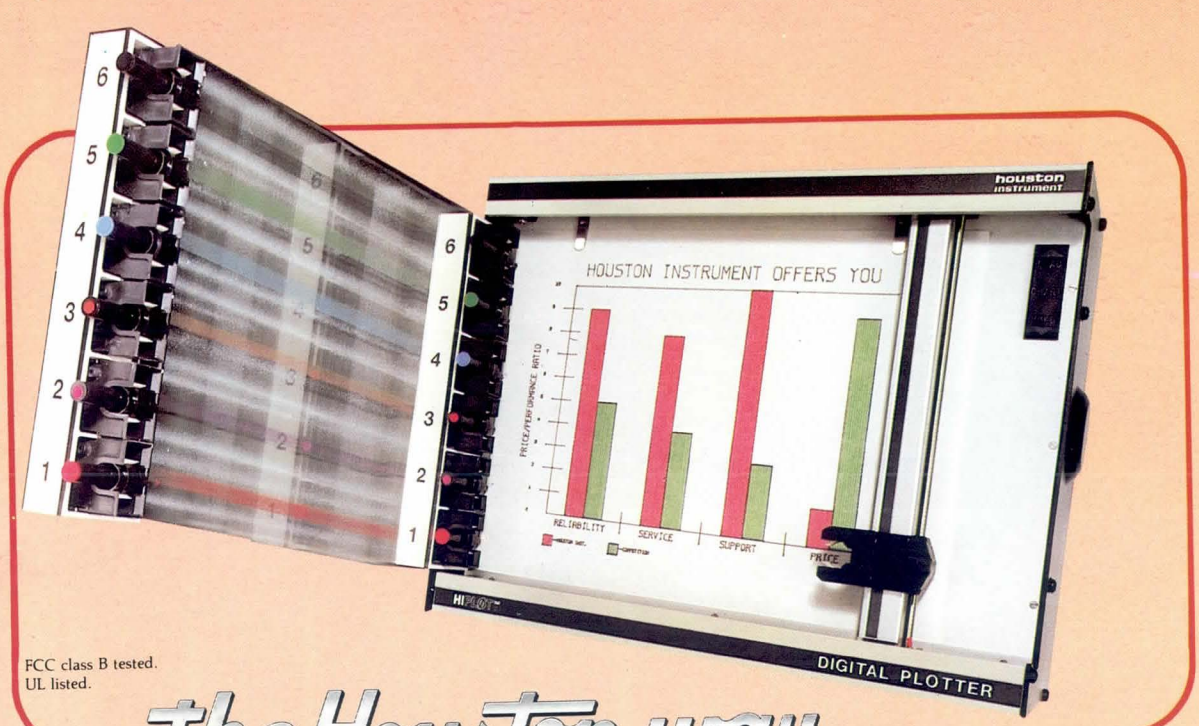

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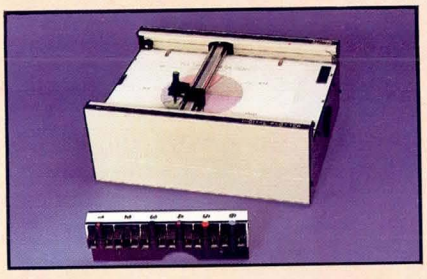

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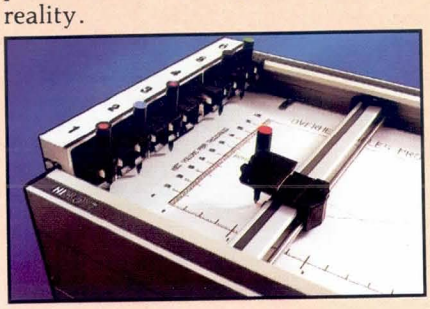

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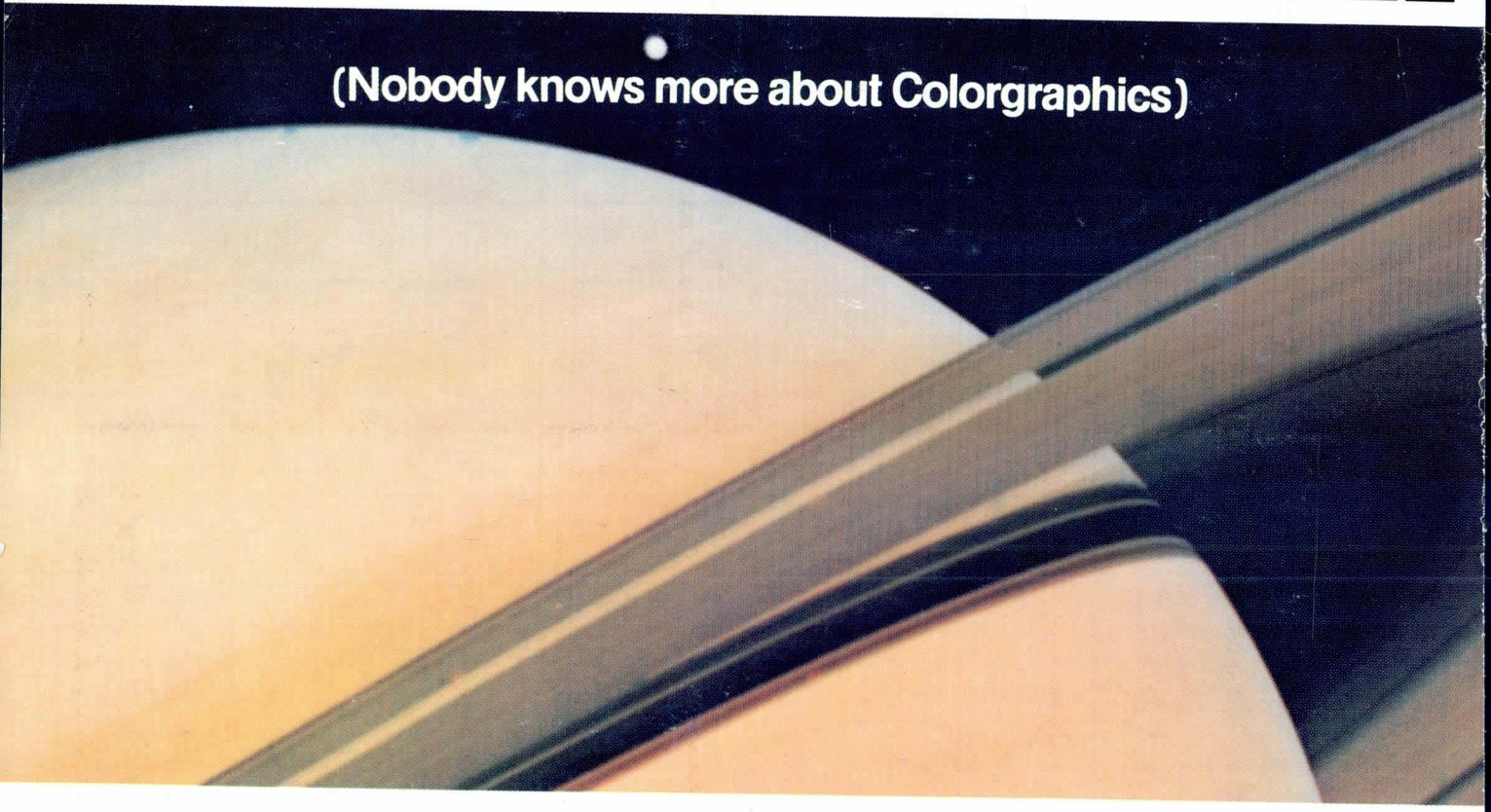

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