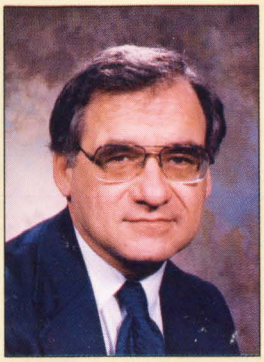
A PENNWELL PUBLICATION JULY 1992

COMPUTER DESIGN

Technology and Design Directions

$5 USA
$6 Canadian
®

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



ExperTest's Miczo on: Design for test

High-performance networks challenge Ethernet

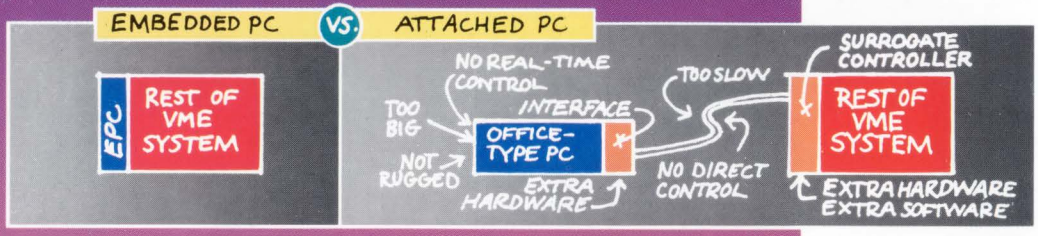
Separating hype from reality in benchmarking

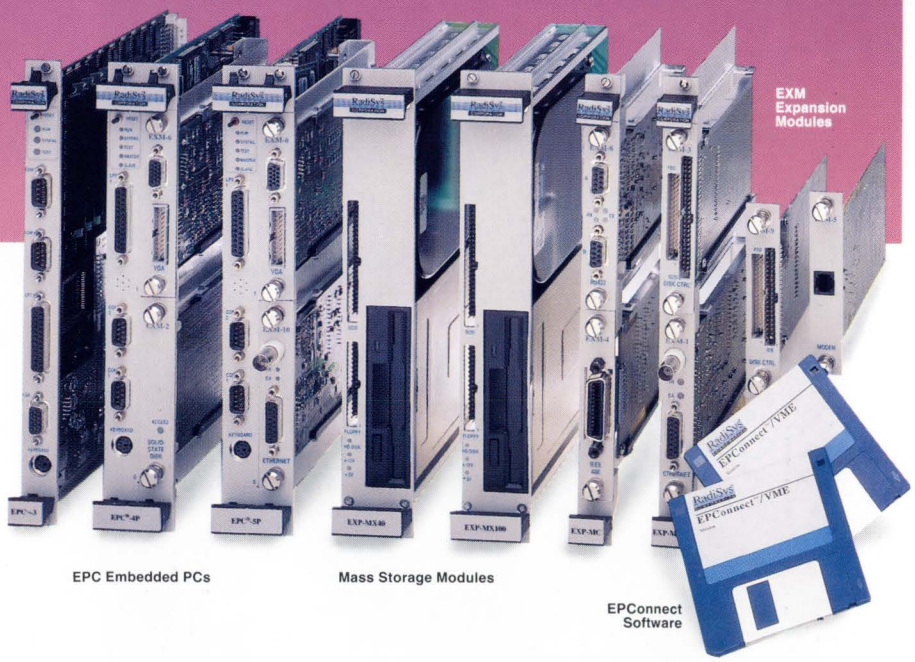
Automation improves speed and accuracy of software testing

LAND of LAN

07
0 74470 80522 9

RADISYS GIVES VME THE INSIDE ADVANTAGE





Integrating a PC with your VME system is a smart move. The "PC advantage" provides a superior human interface and access to the PC's huge base of system, application and development software.

The PC Advantage belongs inside your VME system. Not attached to it. By embedding a PC inside your VME card cage, instead of attaching it externally, you break through the inherent communications bottleneck that constricts system performance. You also eliminate the superfluous hardware and software needed to attach two system architectures.

Only RadiSys EPC® Embedded PCs completely integrate the strengths of PC and VME. An EPC, with its exclusive EPConnect™ Software, is the only 386- or 486-based, PC-compatible computer with software that integrates the VMEbus into the DOS, Windows, UNIX and OS/2 environments. EPCs give your VME systems:

- **Highest system performance** from the real-time responsiveness of the direct 32-bit interface between the 386 or 486 and the VMEbus.
- **Improved system packaging** in 1/10th the volume, with integral VME ruggedness, and no bus link baggage.

And EPCs cost you less. EPC-based systems avoid the costly pitfalls of attached PC systems. No extra interfaces, cables, surrogate controllers, or the software to make them work.

Give your VME systems the EPC advantage. Call (800) 950-0044. We'll send all the details. No strings attached.

EPC MODEL	EPC-1 (shipping since Aug '88)	EPC-3 (shipping since Aug '89)	EPC-4 (shipping since Mar '90)	EPC-5 (shipping since Oct '90)
Processor Modules:				
CPU	80386	80386SX	80386	80486
CPU Clock	16 or 20MHz	16MHz	25 MHz	25 or 33 MHz
DRAM	1 or 4 MBytes	1, 2 or 4 MBytes	4, 8 or 16MBytes	4, 8 or 16 MBytes
Graphics	EGA (640 x 350)	VGA (800 x 600)	VGA (800 x 600)	VGA (800 x 600)
Mass Storage Modules:				
Hard Disk Capacity	40 MBytes		40, 100 or 200 MBytes	
Floppy Drive Size/Cap.	3.5" / 1.44 MBytes		3.5" / 1.44 MBytes	
Expansion Capabilities:				
PC Add-in Cards	Yes		Yes	
EXMbus Expansion	N/A	EXM Expansion Modules:		
		EXM-1 Ethernet	EXM-5 Modem	EXM-9 IDE/Floppy Ctrl.
		EXM-2 Solid State Disk	EXM-6 VGA Graphics	EXM-10 Ethernet
		EXM-3 SCSI/Floppy Ctrl.	EXM-7 RS232 Serial I/O	EXM-11 Timer/Counter
		EXM-4 IEEE 488	EXM-8 RS422 Serial I/O	EXM-12 Prototyping Card
Software Support:	EPConnect development, run-time, and multiprocessing software package for DOS, Windows, UNIX and OS/2			

RadiSys®
CORPORATION

THE INSIDE ADVANTAGE

RadiSys Corporation
19545 NW Von Neumann Dr.
Beaverton, OR 97006 USA
(800) 950-0044
(503) 690-1229
Fax (503) 690-1228

CIRCLE NO. 1

One Thing Separates a Great System Enclosure from a Good One.

It's the innovative application of cutting-edge technology to your specific requirements. It's what we do at Electronic Solutions.

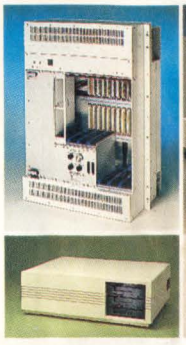
If you're the engineer responsible for the system packaging, you have your hands full dealing with power distribution, cooling, and safety concerns such as UL, CSA and VDE approvals. That's where Electronic Solutions can make your job easier! You can rely on our experience and expertise to quickly resolve the design issues you're facing – at a price that even your bean counters will be pleased with.

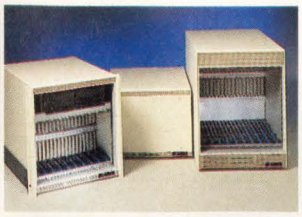
Airflow testing. Our *in-house* airflow/temperature testing facility allows us to carefully examine the environment *inside* a system enclosure, testing the effects of wire harness placement, fan size and location, and the characteristics of the airflow path itself. We can even test your complete system to fine tune air direction, cool hot spots, and reduce audible fan noise and power consumption.

Safety Agency Approvals. Bypass the costly maze of paperwork and testing! We can provide enclosures that are already UL listed, CSA certified, and GS approved through TUV certification. That big step allows you to install recognized boards and peripherals and win agency approval of your finished system with no additional effort or cost! As a self-testing facility for the agencies, we're equipped to handle every aspect of certification to reduce your costs and shorten your time to market.

EMI/RFI Testing. We subject our enclosures to *in-house* testing per MIL-STD-285, providing an attenuation profile of each unit. When it comes time for you to pursue FCC or VDE approval of your system, we can perform these tests for you and resolve any problems immediately.

Whether it's off-the-shelf or something special that's off-the-drawing board, there's only one way to get the enclosure that's just right for your system. That's to call Electronic Solutions and put our experience to work for you.





VMEbus
VXI bus
Sun bus
Mixed buses
Proprietary buses
Multibus I
Multibus II
Futurebus+

Tabletop,
Rackmount,
DeskMate,
Bellcore and
Custom
Designs

ZERO Electronic Solutions
UNIT OF ZERO CORPORATION

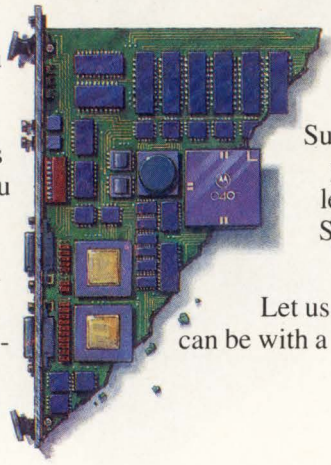
6790 Flanders Drive, San Diego, CA 92121
(619) 452-9333 FAX: 619-452-9464
Call Toll Free: (800) 854-7086
In Calif: **(800) 772-7086**

CIRCLE NO. 2

Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the

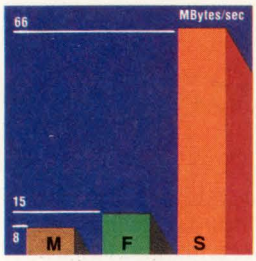


SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

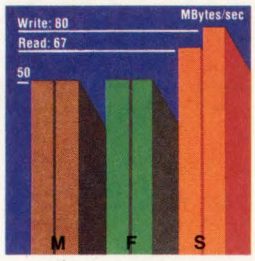
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



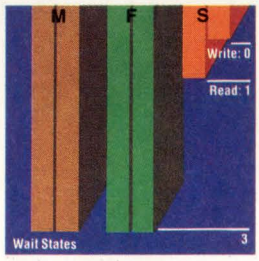
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



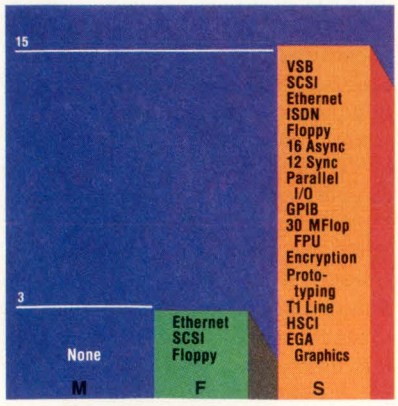
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



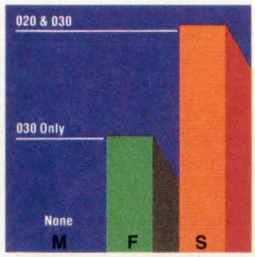
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



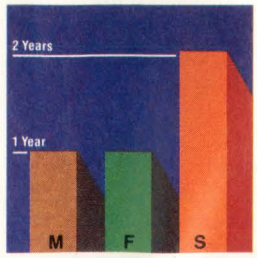
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



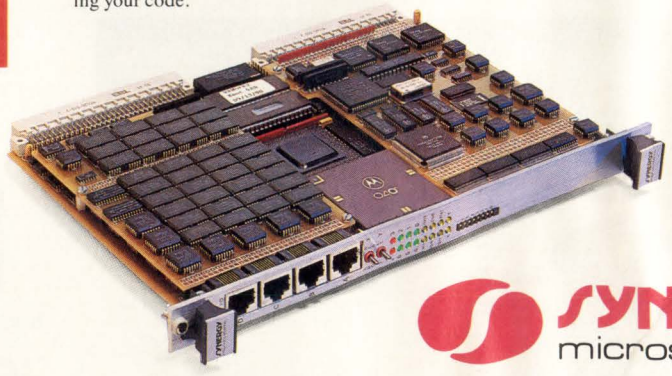
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 **(619) 753-2191** FAX: 619-753-0903

INSTANT DATA ACCESS (IDA) DIAL (617) 494-8338 DOCUMENT NO. 1042

IDA

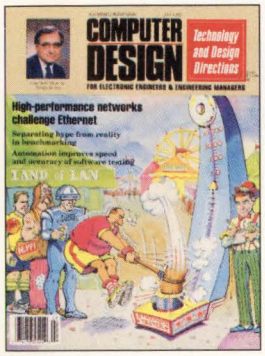
CIRCLE NO. 3

A PENNWELL PUBLICATION VOL 31, NO 7 / JULY 1992

COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



Because Ethernet can only hit a transfer rate of 10 Mbits/s, several contenders are lined up to displace the current network leader...**83**

Illustration by Bill Morrison

COMING NEXT MONTH

Designing high-speed digital systems

Bus-based DSP systems

Multichip modules

Op amps

NEWS BRIEFS

TECHNOLOGY DIRECTIONS

ASICs & ASIC Design Tools

Integrated Circuits

Software & Devlopment Tools

Computers & Subsystems

CAE/CAD Tools

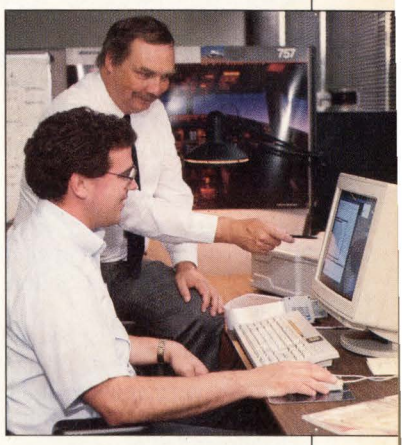
NEW PRODUCT DEVELOPMENTS

Computers & Subsystems

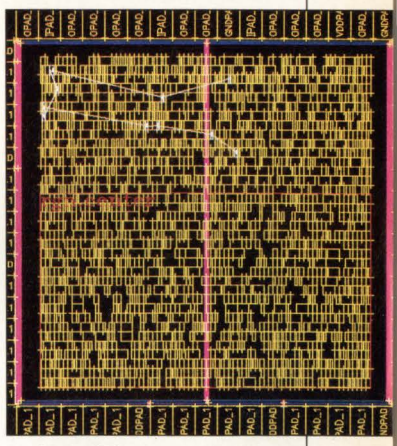
Integrated Circuits

CAE/CAD Tools

ASICs & ASIC Design Tools



Page 38



Page 50

Page 107

CONTINUED ON PAGE 5

SOURCEGATE™

integrating high level language debugging with in-circuit emulators.

SourceGate is a window driven high level language debugger designed to support the Huntsville Microsystems 200 series of in-circuit emulators.

- User configurable windows can be sized, moved and duplicated anywhere on the screen.
- Code can be viewed in all displays (trace, single step, etc.) in one of three modes: Source only, Assembly only or both Source and Assembly.
- Watch windows display and monitor code variables.
- Optional Performance Analysis Card for real-time software performance analysis and real-time software test coverage.
- Available for IBM PC family and UNIX systems including Apollo and SUN.

For more complete technical information, write to Huntsville Microsystems Inc., 3322 South Memorial Parkway, Huntsville, AL 35801 or call (205) 881-6005. Ask for *free* demo disk.

IBM is reg. T.M.
International Business Machines, Inc.
Unix is reg. T.M.,
Bell Laboratories, Inc.

Available Emulators

68000	68EC020
68008	68EC030
68010	68HC001
68020	68HC11 Family
68030	including FI&D3
68302	8051 Family
68301/303	DS5000
68330/333	8096/80196 Family
68331/332	8085
68340	64180/Z180
6809/6809E	Z80
	68HC16 Family

Now supporting 68040 Series

HMI

COMPUTER DESIGN
Technology and Design Directions

CONTINUED FROM PAGE 3

ExperTest's Dr. Alex Miczo on: Design for test

Test automation for ICs is finally taking its rightful place beside design automation in importance. **25**

TECHNOLOGY & DESIGN REPORTS

Automation improves speed and accuracy of software testing

Testing complex software applications is a tedious task best left to machines. New methods of automating the process promise payoffs in terms of shipping higher-quality products. *—Tom Williams* **57**

Separating hype from reality in benchmarking

Benchmarking simulators is a tough job that tests users and vendors alike. But with adequate cooperation between the two camps, meaningful results can be achieved. *—Mike Donlin* **69**

COVER STORY

High-performance networks challenge Ethernet

A half-dozen high-performance network interfaces—including three proposed standards—dominate the industry. Though each has advantages in its particular area, price/performance will undoubtedly push the market toward a single approach. *—Warren Andrews* **77**

DESIGN STRATEGIES

Video teleconferencing on British shores

Designing a video teleconferencing system involves building bidirectional equipment that can capture and compress video and audio images from one location and transmit them to another, where the signals must be received, decompressed and reconstructed. *—Dave Wilson* **95**

PRODUCT FOCUS

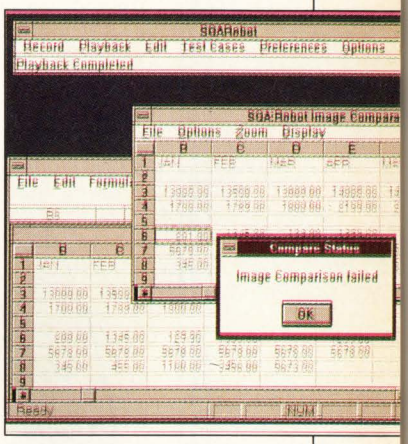
Logic analyzers tackle the "deeper" problem

Perhaps the greatest opportunity to shorten the design cycle comes from spending time more effectively in the lab. *—Jeffrey Child* **101**

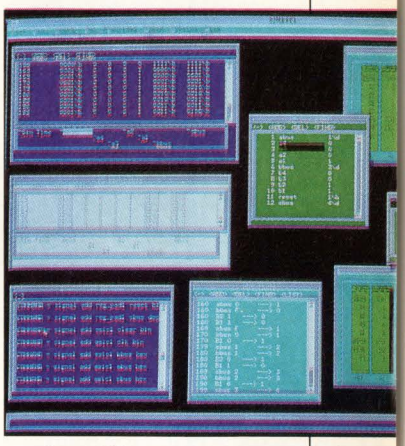
COLUMNS

MIXED-SIGNAL DESIGN *—Stephan Ohr*

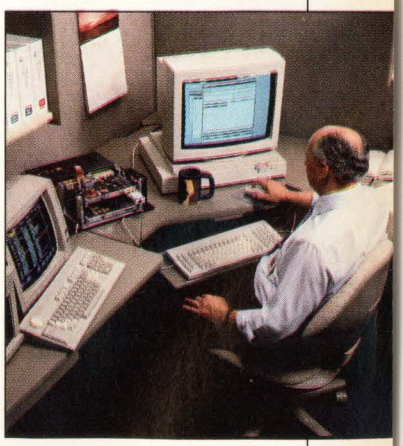
Standard linear parts from customizable arrays..... **114**



Page 57



Page 69



Page 101

If you're looking for realtime computing that's really open, there's only one place to really get it. Digital.

Our longtime leadership in realtime computing, combined with our total commitment to standards, makes it possible to offer you

DIGITAL. THE OP

the industry's most complete, product-rich, open realtime environment. And, best of all, it's available now.

Digital's adherence to standards provides you with a truly open advantage. Not only does it give you flexibility in your choice of realtime systems that afford you unmatched portability and interoperability, but it also fully protects your computing investments. Digital's support for a wide range of standards includes POSIX 1003.1, draft 1003.4, TCP/IP, DECnet™/OSI, Motif® and the VME, SCSI and TURBOchannel™ buses. Plus, we now offer realtime extensions to OSF/1.®

In addition to complying with open standards, Digital makes available a host of development tools that will boost your productivity.

Besides expanding the scope of our VAXELN™ Realtime toolkit for the VMS™ environment, we're introducing the same capabilities for UNIX® environments with our DECelx™ toolkit. Once again, our open approach leaves the choice up to you.

Digital's open realtime story continues with our Network Application Support (NAS) standards-based open computing products. You can share applications from different vendors across computing platforms. What that means is no matter what size computers you have in your realtime environment—from embedded processors to mainframes, no matter what operating system you're using, Digital can tie it all together. A better solution because it's an open solution.

Open standards. Open development tools. Open hardware and software. In short, an open environment. It's time you took advantage of Digital's open realtime computing. To find out how, just call 800-DEC-INFO (332-4636), ext. Realtime.

digital™

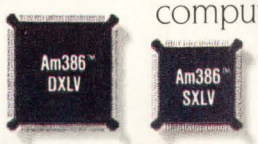
EN ADVANTAGE.

Soon, Eight Ho Computing Will

(actual size)

AMD Introduces The World's First 386 Microprocessor With 3-Volt Technology.

Two standard dry-cell batteries. There's really nothing special about them. Aside from the fact that they can run a powerful, portable 386 computer for a full eight hours. Provided, of course, that portable is built around a low-voltage Am386™ microprocessor.



The 25MHz DXLV and the 25MHz SXLV are available in PQFP packaging.

Thanks to the low-voltage Am386 microprocessors, laptop, palmtop and notebook computer designs will become smaller, lighter, and more powerful than ever before.

With battery life of up to eight hours or more. That's a full day's worth of 386 performance—the per-

urs Of Portable Look Like This.

formance you need to run sophisticated applications like Windows™ 3.0.

And rest assured, the low-voltage Am386 microprocessors are proven compatible and comply fully with JEDEC standards for low-power, 3-volt computing. We can even supply you with the 3-volt EPROMs your systems will need. Other 3-volt system logic is also readily available.

For more information on the low-voltage Am386 microprocessors call AMD today at **1-800-222-9323**. You'll never look at dry-cell batteries the same way again.

Advanced Micro Devices

"We're Not Your Competition."℠

CIRCLE NO. 5

Hitachi enlists systems design house to support its ASIC users

With its launching of a third-party ASIC design center program last month, Hitachi America (Brisbane, CA) has given its users access to a level of systems engineering expertise they themselves may not have. "As ASIC technologies become increasingly complex, the mix of customer requirements and expectations also becomes more sophisticated," explains ASIC marketing manager Joe Bunik. "Today's leading customers are not just looking for yesterday's training on patchwork tools and a grab bag of workstations. In addition to an industry-standard environment, they're looking for a support infrastructure which has the systems-level expertise and high-performance design techniques that will let them achieve a fundamentally superior ASIC solution."

Hitachi's appointment of Locus (Madison, WI) as an authorized design center is the first of several regional agreements it will be developing to support its users. Remarking that Locus is not just a CAD shop but is an experienced systems design and manufacturing operation in its own right, George Saul, director of marketing, says, "This depth of systems expertise at the ASIC level is critical to the effective implementation of customer solutions."

With ASIC designs involving hundreds of thousands of gates and system design requirements more demanding by the day, it's highly likely that we'll be seeing a proliferation of third-party ASIC design centers like the Hitachi-appointed Locus. *—Barbara Tuck*

Teradyne sells EDA tools

Teradyne EDA (Santa Clara, CA) has completed its departure from the front-end CAE business by selling its Aida test software to Crosscheck Technologies (San Jose, CA) and its line of Vanguard Schematic design systems to Sophia Systems (Tokyo, Japan). Though the deal is still pending, Crosscheck will immediately support present Aida users and will hire core engineering and marketing personnel from Teradyne.

The acquisition will give Crosscheck the ability to go beyond chip-level design to system-level testing and diagnostics. Crosscheck's present tools are applicable mainly to complex asynchronous circuits with multiple gated clocks. The Aida tool targets synchronous designs and is particularly useful in system-level debugging.

Sophia has been a Vanguard distributor for several years, and will obtain worldwide distribution rights with the acquisition. The vendor will sell, service and support Vanguard, and plans to enhance and expand the product line to stay competitive in the lucrative Japanese EDA marketplace.
—Mike Donlin

Neural net chip powers first commercial application

An analog neural network IC developed by Synaptics (San Jose, CA) is now powering an optical check reader built by Verifone (Redwood City, CA). The chip, called the I-1000, consists of two parts. The first is a neural network-based image-sensing array that imitates the early vision processes occurring in the retina before information is passed to the visual cortex of the brain. The second is a neural network trained by example to recognize the patterns of characters on a check being slid through a slot in the reader.

Neural networks are characterized by their ability to learn by example. In the case of the I-1000 in this application, the learning was done off-line via computer simulation and the results transferred to mask layers used in manufacturing the chip. One might think of it as an Electrically-Trainable PROM (ETPROM).

Synaptics was founded by Federico Faggin, coinventor of the microprocessor and cofounder of Zilog, and Carver Meade, of VLSI and Silicon Compiler fame. The design for the I-1000, of course, exists in a silicon compiler and can be expanded, reconfigured and retaught for other practical applications that may present themselves.
—Tom Williams

Bulletin board for fuzzy logic

A semipublic bulletin board for people interested in fuzzy logic has been established by Aptronix (San Jose, CA). Called FuzzyNet, the bulletin board has two levels. There is a level for the general public interested in news and developments in the industry. It will provide an electronic mail system and access to articles and news on applications tools and the like.

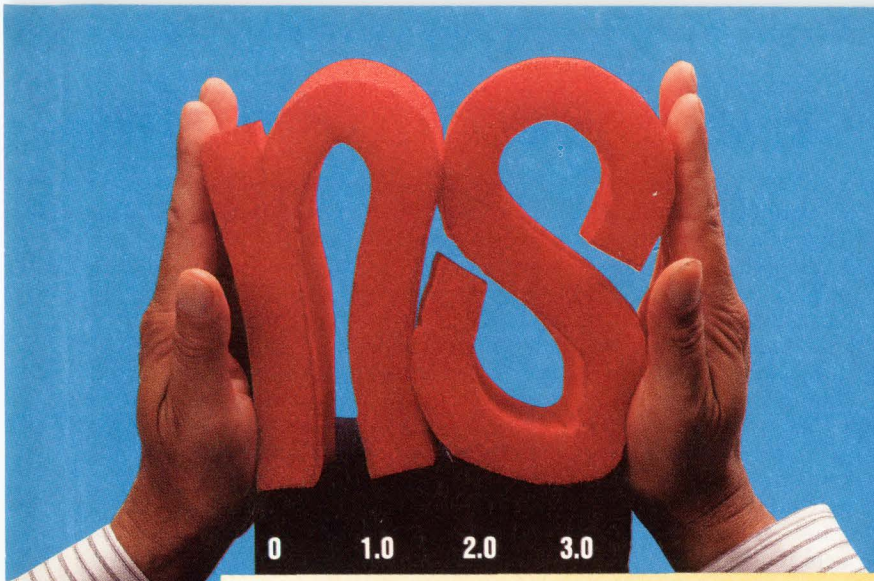
A second level will be for registered users of Aptronix's fuzzy logic development environment, called Fidé. At this level, users will be able to seek on-line help and exchange applications and experiences regarding the use of Fidé. FuzzyNet is up and running now, but is still building a base of users and information. The number is (408) 428-1883.
—Tom Williams

Cadence backed in push to extend Verilog methodology to VHDL

A dozen or so electronic systems companies and ASIC vendors are backing Cadence Design Systems (San Jose, CA) in an attempt to extend Verilog ASIC modeling practices to VHDL, which so far lacks any standard modeling methodology. The intent of the group is to submit a proposal to the appropriate standards organizations outlining how the adaptation of Verilog's predefined logic primitive set, standard interchange format for delays (Standard Delay File), timing model, and timing checks—all in VHDL source code—would accelerate the availability of ASIC libraries in VHDL.

The initiative has been endorsed by Alcatel NV, Bell Northern Research, Epson America, Ericsson Telecom AB, ExperTest, Harris Semiconductor, National Semiconductor, NEC Electronics, North Oaks EDA Consulting, Oki Semiconductor, S-MOS/Seiko, Sunrise Test Systems, Texas Instruments, Toshiba, the VHDL Technology Group, and Xilinx. I.M. Dodd, director of tools and technologies at Alcatel's Paris headquarters, says, "Let's move past the problems that have al-

Continued on page 12



COUNT ON IDT

When Every Nanosecond Counts

Squeeze critical nanoseconds from your high-speed logic interface with the fastest FCT logic available. IDT's FCT-CT family offers speeds that are 50% faster than standard FCT or FAST logic families — as fast as 3.4ns (typical)!

The Perfect System Solution

As a system designer, you need the perfect combination of:

1. ***Fastest speed***
2. ***Low ground bounce***
3. ***Low power consumption***

FCT-CT logic has true TTL compatibility for ease of design. The reduced output swings and controlled output edge rate circuitry ensure low system noise generation. No other technology offers higher speeds or lower power consumption.

The FCT-CT family is completely pin- and function-compatible with FCT logic, and is available today in all standard packaging.

FUNCTION	PROPAGATION DELAY (Max)	OUTPUT ENABLE (Max)	OUTPUT DISABLE (Max)
Buffers	4.1ns	5.8ns	5.2ns
Transceivers	4.1ns	5.8ns	4.8ns
Registers	5.2ns	5.5ns	5.0ns
Latches	4.2ns	5.5ns	5.0ns

Free Logic Design Kit

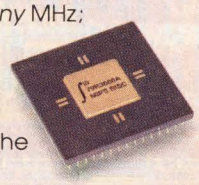
Call our toll-free hotline today and ask for Kit Code 3061 to get a *1991 High-Speed CMOS Logic Design Guide* and *free FCT-CT logic samples.*

12ns 256K SRAMS

Fastest cache solutions for RISC and CISC CPUs. 36+ ultra-high-speed sub-micron SRAMs for 33MHz processing & beyond are in the **SRAM Data Book**.

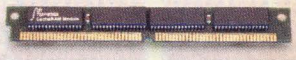
35mips RISC CHIPS AND MODULES

R3000A for the most mips at *any* MHz; R3051 for CPU, cache, & buffers on one chip. Modules, eval. boards & software complete the family. See them in the **RISC Data Book**.



HIGHEST-PERFORMANCE MEMORIES

Fast FIFOs, dense dual-ports, BiCEMOS ECL, & memory modules. 120+ FIFOs & multi-port memories, 5ns ECL, & multi-chip modules are in the **Specialized Memories Data Book**.



Call today for your new IDT data books with complete technical specifications and application information.

Integrated Device Technology, Inc.

(800) 345-7015 • FAX: 408-492-8674

CIRCLE NO. 6

Continued from page 10

ready been solved by the industry and focus on things that need our attention, like subsets for synthesis and acceleration."

EDA vendors of VHDL tools will most likely withhold endorsement until they receive some confirmation that the Cadence-backed initiative is about the advancement of technology, rather than the advancement of Cadence. A hands-off policy, once a strong technical proposal has been submitted to the appropriate forum— which would appear to be VHDL International— might be the confirmation they're waiting for.

—Barbara Tuck

PC multiprocessing bus waits for the 586

Whether you prefer to call it the 586 (or, as Intel prefers, the P5), samples of the latest 80X86 microprocessors reportedly will be delivered to beta customers sometime between now and November's Comdex. Companies that have seen advance technical specifications are apparently impressed with the device.

In fact, designers at Corollary (Irvine, CA) are impressed enough to refocus their strategy for C-bus II, a multiprocessing bus architecture for the PC, and orient it exclusively toward the P5. The original plan for C-bus II was to build a multiprocessing chip set targeted for a 50-MHz 486 and to follow that with MIPS R4000 support. "C-bus II is CPU-independent, so in the future we can support other processors, but at this point it's definitely focused on the P5," says Corollary president George White. "The goals of C-bus II are the same—to be an open bus that is available to use without any royalty or other kinds of attachment." C-bus II will be implemented in a two-chip set which includes a cache bus controller and a datapath exchange chip.

Using the chip set, designers can build the P5 multiprocessor from one-half of an AT form-factor card. The design goal of the C-bus II is to allow from six to eight P5 chips in a multiprocessing PC. If rumors are true that the P5 is twice as fast as a similar-speed 486, such a system based on six 66-MHz P5s would be capable of about 250 Transaction Benchmarking Council (Version A) transactions per second, speculates White.

Intel's aggressive strategy for the P5 and the fact that Intel was willing to share advance information were among the reasons why Corollary decide to alter its focus. This perhaps indicates Intel has changed its stance toward companies, such as Corollary, which build chips that go around Intel's microprocessors.

Concentrating on the P5, Corollary has shelved plans to make a C-bus II chip set for the R4000. Although his was the first company after the original 21 founders to join the ACE consortium, White has been disappointed with ACE's progress. "We still have a technical interest in supporting the R4000, but we really need to see strong customer interest in advance," says White. The needs of the R4000 processor have, however, had some influence on the C-bus II design. "When we had planned to build an R4000 version of the C-bus II chip set, the R4000 crowd wanted more memory to support the R4000's 64-bit virtual address space," says White. As a result, Corollary expanded the physical memory space of the C-bus II from 2 Gbytes to 32 Gbytes. "It's probably a good idea for P5s as well," he adds. The change in memory space is the only modification to C-bus II's feature set as announced last year.

Along with Microsoft (Redmond, WA), Corollary has also announced the development of an implementation of Windows NT that takes advantage of the C-bus II multiprocessing architecture. C-bus II also supports Unix System V Release 4.0 and Santa Cruz Operation (SCO) MPX.

—Jeffrey Child

New support policy for SBus

Sun Microsystems Computer Corporation (SMCC—Mountain View, CA) is updating its SBus support policies this month to provide a greater level of support to SBus developers and to focus its support in critical areas. Last quarter's *SBulletin* (see "Sun curtails support," *Computer Design*, June 1992, p 132) reported that Sun was curtailing its SBus support and would no longer accept inquiries from developers.

SMCC has apparently rethought its position and now says, "Market development engineering will continue to provide phone, fax and e-mail support on demand for hardware, firmware and software queries from the SBus developer community." The company reports the greatest number of questions received has concerned software. And as SMCC nears the introduction of Solaris 2.0, the staff is expected to be busy preparing for the transition. For that reason it states: "We will probably respond less quickly to your requests than we have in the past," but will acknowledge receipt and provide an estimate of when it can service the request.

In addition, SMCC stressed it will make a major effort to aid SBus developers in their transition to Solaris 2.0 DDI/DKI interface. The company will make available a migration kit with sample drivers, a *Device Drivers Manual*, manual pages for the DDI/DKI routines, and data structures and a white paper on porting to Solaris 2.0.

—Warren Andrews

Dazix joins the synthesis pack

Capitalizing on a partnership with AT&T Bell Laboratories (Murray Hill, NJ), Dazix (Huntsville, AL) has entered the competitive synthesis arena with a suite of tools called Dazix Synergy.

The tools, which support the synthesis of VHDL, Verilog and the C hardware description languages, face stiff competition from industry leader Synopsys (Mountain View, CA), as well as Cadence Design Systems (San Jose, CA), Mentor Graphics (Wilsonville, OR) and Viewlogic Systems (Marlborough, MA). Dazix director of marketing James Ulatowski promised that its solution would be more integrated than those of the competitors, but gave few specifics to support the claim.—*Mike Donlin*

FUTUREBUS+ BECOMES A REALITY.

FUTUREBUS+ PICKS UP WHERE VME LEAVES OFF.

CCT is proud to be the first to deliver a significant family of Futurebus+ products. A family that's built on industry standards!

With Futurebus+, OAS (open architecture systems), CCT has taken a giant step forward in computer technology. We can deliver OAS systems or boards based on industry standard micro-processors & operating systems, all in an environment that allows more speed, capacity and intelligent communications.

Our product line includes, standard CPU's, global memory, array processors and specialized interfaces that address the demands of many applications. Including:

- Telecommunications bridges and routers
- Tactical computers and displays
- Manufacturing process monitoring & control

Today's processing power is cramped on yesterday's bus. Release the power of your application with Futurebus+ data movement capacity.

Don't invest in yesterday's technology — Futurebus+ is here today!

FEATURES:

- Scaleable up to 256-bit
- 64-bit compatible
- Multi-processing and Cache coherent environment
- Standard software paradigm through CSR's
- Fault tolerant
- Distributed and Central arbitration
- 68030-33 CISC CPU
- 29000 RISC CPU
- i860 64-bit RISC CPU

Call or Fax CCT today for more information on our Futurebus+ product line!

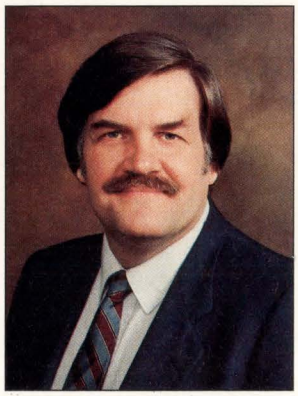
Phone 1-800-CCT-7902
Fax 1-714-937-1225

Cable & Computer Technology, Inc.
1555 S. Sinclair St.
Anaheim, CA 92806
(714) 937-1341

CIRCLE NO. 7

Barnum would be proud

While the drive for bigness may be irresistible, big isn't necessarily better.



John C. Miklosz
Associate Publisher/
Editor-in-Chief

The 29th staging of the Design Automation Circus—excuse me, Design Automation Conference—is over, and most of us on *Computer Design* have finally wound down enough to make some observations about DAC, and about trade shows in general.

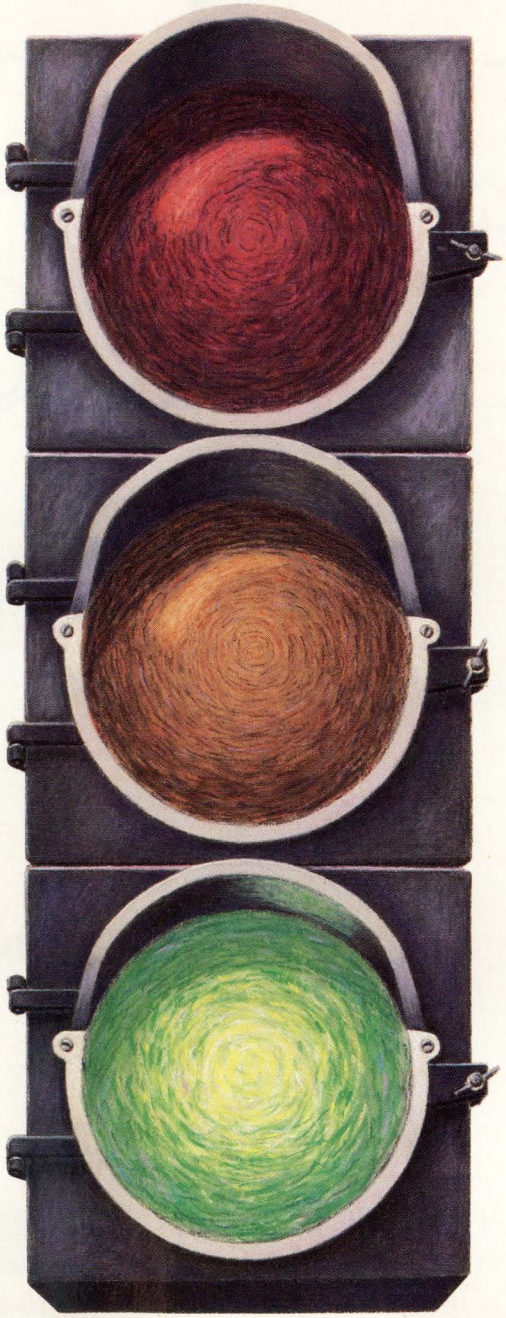
I've come to the conclusion that, while the drive for bigness may be irresistible, big isn't necessarily better. DAC has become a big show, not so much in terms of the number of exhibitors—there were only about 120 this year, although that's not small—or in terms of the number of attendees—attendance was reportedly down 30 to 40 percent compared to last year—but in terms of the staging. Gigantic booth areas, huge audiovisual presentations complete with barkers and a vast array of T-shirts and giveaways somehow seem more appropriate to a Comdex—basically a consumer/reseller/retailer-oriented show—than to a conference and exhibition where the exchange and acquisition of technical information, as well as taking the first steps toward an intelligent buying decision, should be the most important consideration. It's now become extremely difficult to separate the signals from the noise if you're an editor, much less an attendee, and to have your signals heard above the noise if you're an exhibitor, especially a small exhibitor.

Computer Design, for example, sent three technical editors to DAC and, well before the second week in June, they were all being bombarded with requests to attend one-on-one meetings, press conferences, breakfasts, lunches, dinners, hospitality suites, and entertainments. And, of course, they were all being bombarded by the same exhibitors. Some tough choices had to be made: visit with a large vendor, or a small one or an up-and-coming one; give someone an hour or only a half-hour; go to the Nixon library, see *The Phantom of the Opera*, or have dinner at The Cellar. The decisions about what vendors to see on the floor, what exhibitor presentations to attend or what audiovisual extravaganzas to mill about watching must have been just as difficult for the engineering attendees, although most of them probably didn't receive the same number of invitations for breakfasts, lunches, dinners, and entertainments—unless they were big customers or potential big customers, which is understandable.

And, finally, DAC had to be daunting for the small exhibitors, those with only one or two booths. How do they catch an attendee's attention when there's a barker giving a pitch in front of a 10-foot screen? (I can't figure out why anyone would listen to a barker in front of a 10-foot screen, but . . .) Just as an editor might miss something new or significant, so will a designer if a smaller vendor can't get the designer's attention or can't get his message across because of the noise.

Unfortunately, big shows can become victims of their bigness, especially when smaller conferences and exhibitions come along that provide a saner forum for the exchange of information and intelligent buying decisions. We hope that DAC doesn't suffer the tribulations of a couple of other big shows we know.

THE ONLY 5-VOLT MEGABIT FLASH. NO WAITING.



Atmel's 5-Volt-only, one-megabit Flash is available. Production quantities. No waiting.

That's 5 Volts to read and 5 Volts to write. No costly 12-Volt converter or regulator circuits to clutter your system. And, there's more:

PERFORMANCE:

- The AT29C010 is fast—90 nanoseconds commercial, 120 nanoseconds military.

HASSLE FREE:

- The AT29C010 has one thousand 128-byte sectors, and each can be individually written or erased.
- The AT29C010 has the easiest programming algorithm in town. It's self timed and has automatic erase, so you don't have to erase before writing.

So, if you like blazing access times, need sector write and want to save space, call, fax or write us about your application and we'll get you a sample of the Atmel 5-Volt-only Flash.

No Waiting.

INSTANT DATA ACCESS (IDA) DIAL (617) 494-8338 DOCUMENT NO. 1045

ATMEL®

The people who make the difference.

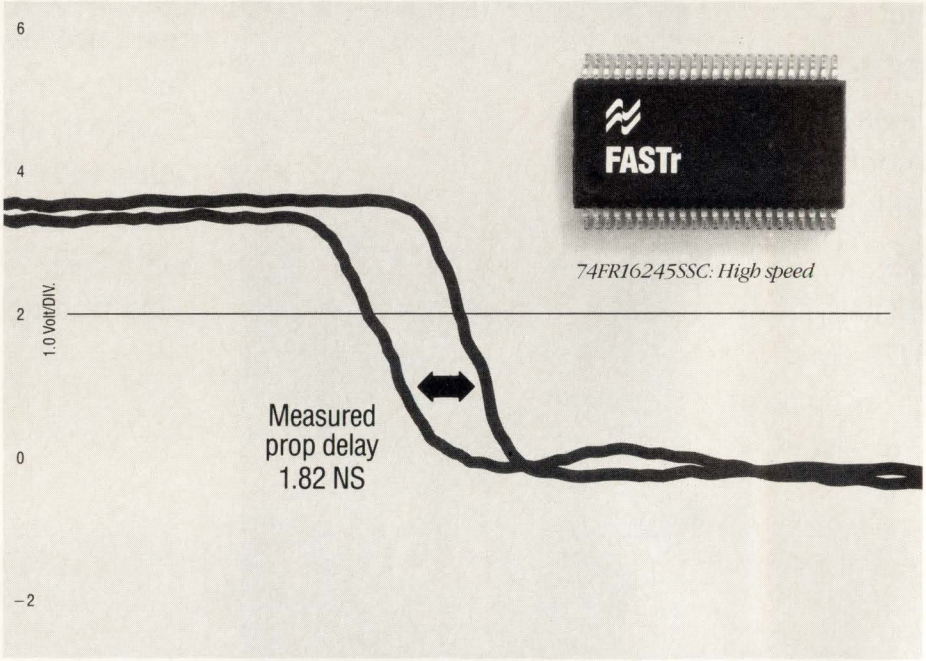
ATMEL CORPORATION
2125 O'Nel Drive
San Jose, CA 95131

Tel. 1-800-292-8635
Tel. (408) 441-0311
FAX (408) 436-4200

CIRCLE NO. 8

National Semiconductor

Introducing FASTr Widebus.



National's going to widen your perspective on Widebus™ with a new family of 16-, 18- and 32-bit bus interface logic devices.

In high-performance PCs, workstations, and medical equipment, our bipolar FASTr offers measured propagation delay of 1.82ns, and guarantees single output switching at 4.3ns max. That's pretty fast company.

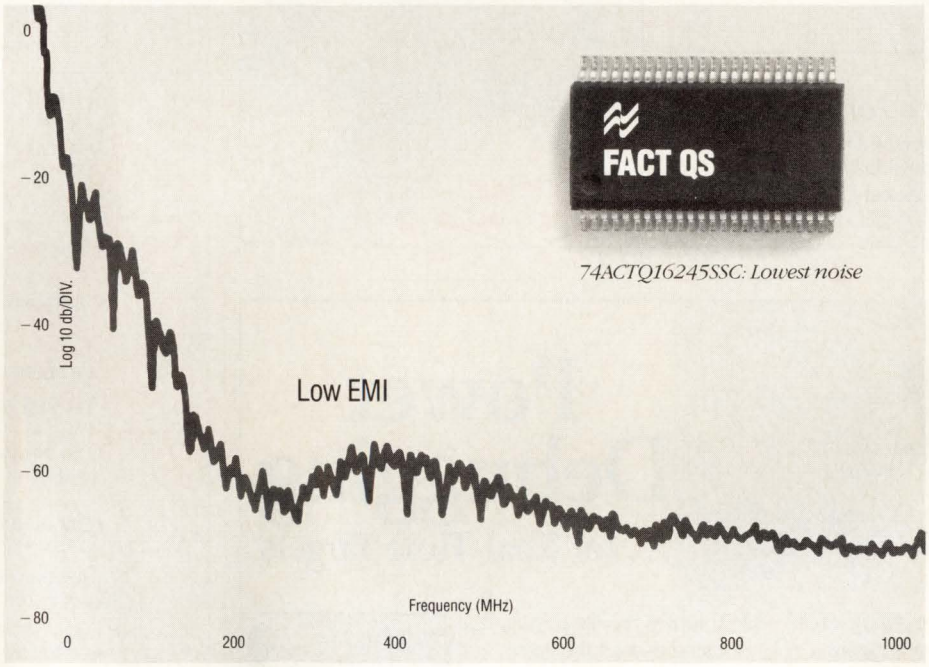
In PCs, laptop and notebook computers, as well as portable communications equipment, our ACMOS FACT QS features quiet output switching and proprietary noise-control circuitry. And that helps you reduce EMI, ground bounce and under-

National's Widebus Family

- Lowest noise (FACT QS: $V_{OLP} = 0.8$, $V_{OLV} = -0.8$)
- High speeds (FASTr: 1.82ns measured)
- Drop-in replacement capabilities
- Guaranteed specs:
  - pin-to-pin skew under MOS conditions
  - AC performance under MOS conditions
  - Ac performance with 250pf loads
- SSOP packaging
- 32-bit read/write buffer FACT QS (74ACT3283T) sampling now; 18-bit SCAN device available now

NORTH AMERICA: P.O. Box 7634, Mt. Prospect, IL 60056-7643 (Tel: 1 800 628 7364, ext. 195; Fax: 1 800 888 5113); **EUROPE**: Industriestraße 10, D-8080 Fürstenfeldbruck, Germany (Tel: 49 8141 103 0; Fax: 49 8141 103 515); **HONG KONG**: 15th Floor, Straight Block, Ocean Centre, 5 Canton Rd., Tsimshatsui, Hong Kong (Tel: 852 737 1654; Fax: 852 736 9921);

And its silent partner.



74ACTQ16245SSC: Lowest noise

shoot. Widebus just doesn't get any quieter.

And with both FASTr and FACT QS, National gives you the AC specs you need to maximize your system's potential: pin-to-pin skew under MOS conditions, AC performance under MOS conditions, and with 250pf loads. No other Widebus supplier guarantees that kind of performance.

Best of all, our Widebus is now widely available. We're already shipping 16-bit FASTr and 16- and 32-bit FACT QS devices. And we're planning the introduction of additional 18- and 32-bit Widebus products.

So if you're looking for the Widebus with wider appeal, look no further than National.

To make it fast and keep it quiet, call National today at 1-800-NAT-SEMI, Ext. 195.

National Semiconductor

JAPAN: Sanseido Building 5F, 4-15-3, Nishi-shinjuku, Shinjuku-ku, Tokyo, Japan 160 (Tel: 81 3 3299 7001; Fax: 81 3 3299 7000). Widebus is a trademark of Texas Instruments. Inc.

COMPUTER DESIGN
Technology and Design Directions

EDITOR-IN-CHIEF/ASSOCIATE PUBLISHER
John C. Miklosz, Ph.D., (508) 392-2114

SENIOR EDITORS
Warren Andrews, *Computers & Subsystems*
(508) 283-2102
Barbara Tuck, *ASICs & ASIC Design Tools*
(516) 473-1661
Michael G. Donlin, *CAE/CAD Tools*
(508) 392-2123
Tom Williams, *Software & Development Tools*
(408) 335-5514
Dave Wilson, *Integrated Circuits*
(508) 392-2176

SECTION EDITOR
Jeffrey Child, *New Product Highlights*
(508) 392-2126

CONTRIBUTING EDITOR
Stephan Ohr, *Analog & Miixed-Signal*
(908) 232-1380

MANAGING EDITOR:
Arlyn S. Powell, Jr.

CHIEF COPY EDITOR:
Annette M. Staron-Wilson

ASSISTANT EDITOR:
Lisa A. Coleman

PRESENTATION MANAGER:
Richard Sarno

EDITORIAL ASSISTANT:
Claire Ellis

ART DIRECTOR: Jan Horner

ILLUSTRATOR: Manuel King

AD TRAFFIC MANAGER:
Kelly Rice, (508) 392-2198

CIRCULATION DIRECTOR:
Robert P. Dromgoole, (918) 832-9213

CIRCULATION MANAGER:
Paul Westervelt, (918) 832-9287

REPRINTS:
June Bozarth, (918) 835-3161

PUBLISHER
David L. Allen, (508) 392-2111

ASSOCIATE PUBLISHER/ NATIONAL SALES MANAGER:
Tim L. Tobeck, (508) 392-2116

PennWell PUBLISHING COMPANY

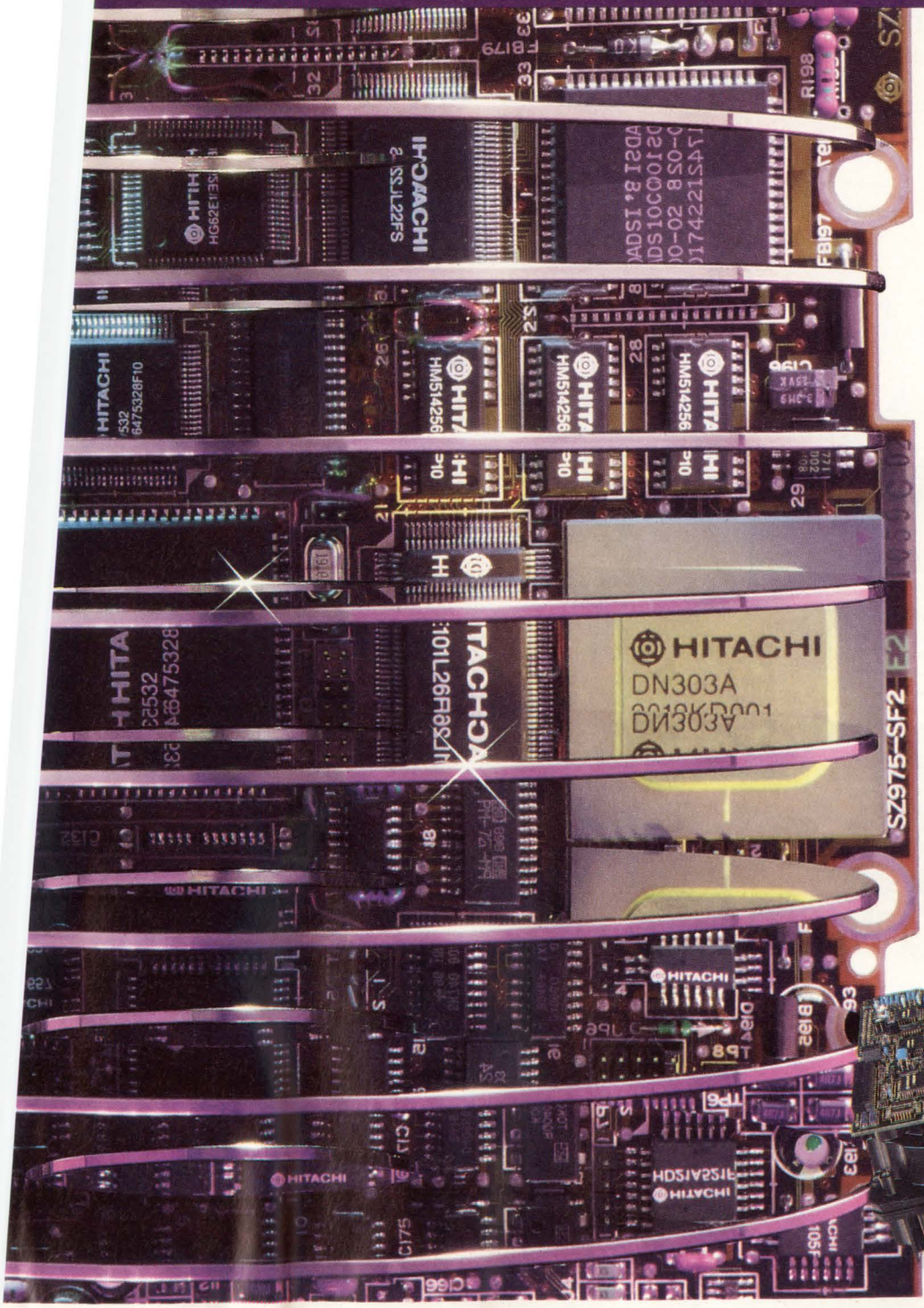
Advanced Technology Group
Dr. Morris R. Levitt, Senior Vice-President
Leslie P. Cypret, Vice-President, Administration
One Technology Park Drive
P.O. Box 990
Westford, MA 01886
Tel: (508) 692-0700
Fax: (508) 692-0525

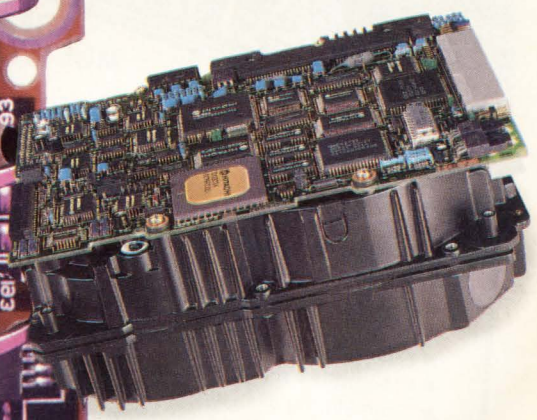
Postmaster: Send change of address form 3579 to COMPUTER DESIGN Circulation Department, Box 3466, Tulsa, OK 74101

BPA ABP

Pushing the Edge of Capacity...

1.65 GB in a 5.25-inch Form Factor.





Edge-to-Edge Performance

The DK516C-16 uses Hitachi's advanced proprietary technology to deliver 1.65 GB of capacity and a fast 13.5 ms average access time.

Its SCSI interface provides a maximum data transfer rate of 5.0 Mbytes/sec (synchronous), with a 256 Kbyte data buffer and read look-ahead cache.

Or, if you have an ESDI application, look into Hitachi's 1.54 GB DK516-15 with a 14 ms average seek time and a 2.75 MB/sec data transfer rate.

Edge-to-Edge Quality

Choose the DK516 and you get a drive backed by the quality and reliability of Hitachi—a $54 billion company. Unlike other drive manufacturers, we design, build, and test all key components in-house.

For more information about the DK516, or any Hitachi disk drive, call 1-800-HITACHI.

Hitachi America, Ltd.
Computer Division, MS500
Hitachi Plaza
2000 Sierra Point Parkway
Brisbane, CA 94005-1819

HITACHI®
Our Standards Set Standards

Authorized Distributors:

CONSAN 612-949-0053 (IA, IL, IN, KS, KY, MI, MN, MO, ND, NE, OH, Pittsburgh, PA, SD, WI)

GENTRY ASSOCIATES 800-877-2225 (AL, D.C., FL, GA, LA, MD, MS, NC, SC, TN, VA)

R SQUARED 800-777-3478 (AZ, CA, CO, NM, OR, UT, WA, WY)

SIGNAL 800-228-8781 (CT, MA, ME, NH, RI, VT)

SPECIALIZED SYSTEMS TECHNOLOGY 800-688-8993 (AR, LA, OK, TX)

HITACHI (CANADIAN), LTD. 416-826-4100 (Canada)

CIRCLE NO. 11

IDA INSTANT DATA ACCESS (IDA) DIAL (617) 494-8338 DOCUMENT NO. 1034

CALENDAR

CONFERENCES

July 26 - 31
SIGGRAPH '92
McCormick Place, Chicago, IL.

This year's conference theme is "Insight Through Images," a theme that will be portrayed through an extensive program of courses, panels and an exhibition. More than 25,000 people are expected to attend this leading forum for computer graphics hardware, software and systems. There will also be an electronic theater and art show. Contact: ACM SIGGRAPH '92, PO Box 95316, Chicago, IL 60694-5316, (312) 644-6610, Fax (312) 321-6876.

Circle 366

August 12 - 14
Windows & OS/2 Conference
World Trade Center & Hynes Convention Center, Boston, MA.

More than 20,000 attendees are expected at this conference which focuses on the two key personal computer graphical interfaces of Windows and OS/2. There will be technical sessions on programming in the Windows and OS/2 environments. The exhibit will include a test drive center where computers are set up for attendees to try the latest applications. Contact: CM Ventures, 5720 Hollis St, Emeryville, CA 94608, (415) 601-5075, Fax (415) 601-5075.

Circle 367

September 15 - 17
Buscon '92 East
Hynes Convention Center, Boston, MA.

Buscon '92 East is the event where the products, technologies and components related to bus- and board-level design can be seen. The technical conferences, designed and coordinated by *Computer Design* and *Military & Aerospace Electronics*, are highly focused, in-depth seminars that explore the hottest issues from SCI to Futurebus+, RISC and embedded PCs. There will be half-day and full-day tutorials and more than 200 exhibitor booths. Contact: Registration Department, Buscon '92 East, 200 Connecticut Ave, Norwalk, CT 06856-4990, (800) 243-3238, Fax (203) 857-4075.

Circle 368

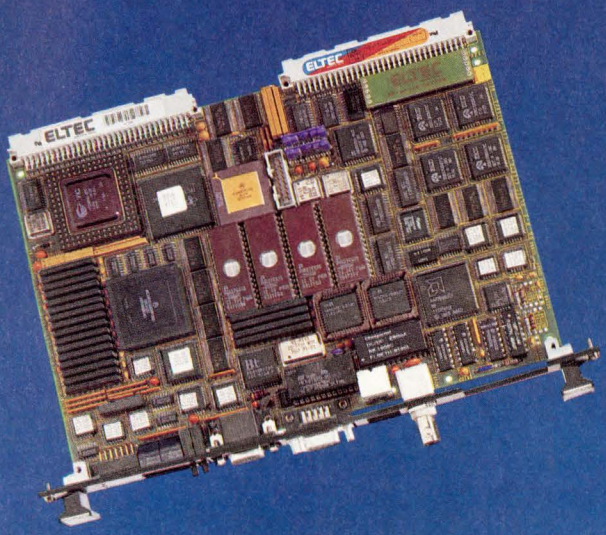
September 22 - 24
Unix Expo
Jacob K. Javits Convention Center, New York, NY.

The ninth annual Unix Expo will showcase Unix/Open Systems products, standards and services to an audience including corporate end users, resellers and systems integrators. The expo and conference will analyze current trends in the Unix community, including the move toward Open Systems computing, multimedia and the corporate world's increasing use of Unix as a platform for achieving open systems. Contact: Bruno Blenheim Inc, Fort Lee Executive Pk, One Executive Dr, Fort Lee, NJ 07024, (800) 829-3976 or (201) 346-1400, Fax (201) 346-1532.

Circle 369

EUROCOM®16

The low cost solution ...
... for any kind of CPU/Graphics application on VME



Multi-Functional Features

68(EC)030, 25 MHz CPU, optional FPU, SVGA-Graphics (800 x 600 pixels) with 16 colors, support for EL-displays, Ethernet or Cheapernet Interfaces, SCSI Interface, 4 or 8 MByte DRAM, 128 KByte SRAM, 2 MByte EPROM space, AT-Keyboard and mouse adaptor, 4 serial and 2 parallel ports.

Software-Flexibility

Realtime Operating support for OS-9 and LynxOS including X-Window and MGR plus TCP/IP network software.

Modular Design

Board design permits low cost specific configurations for quantity requirements by removing various features.

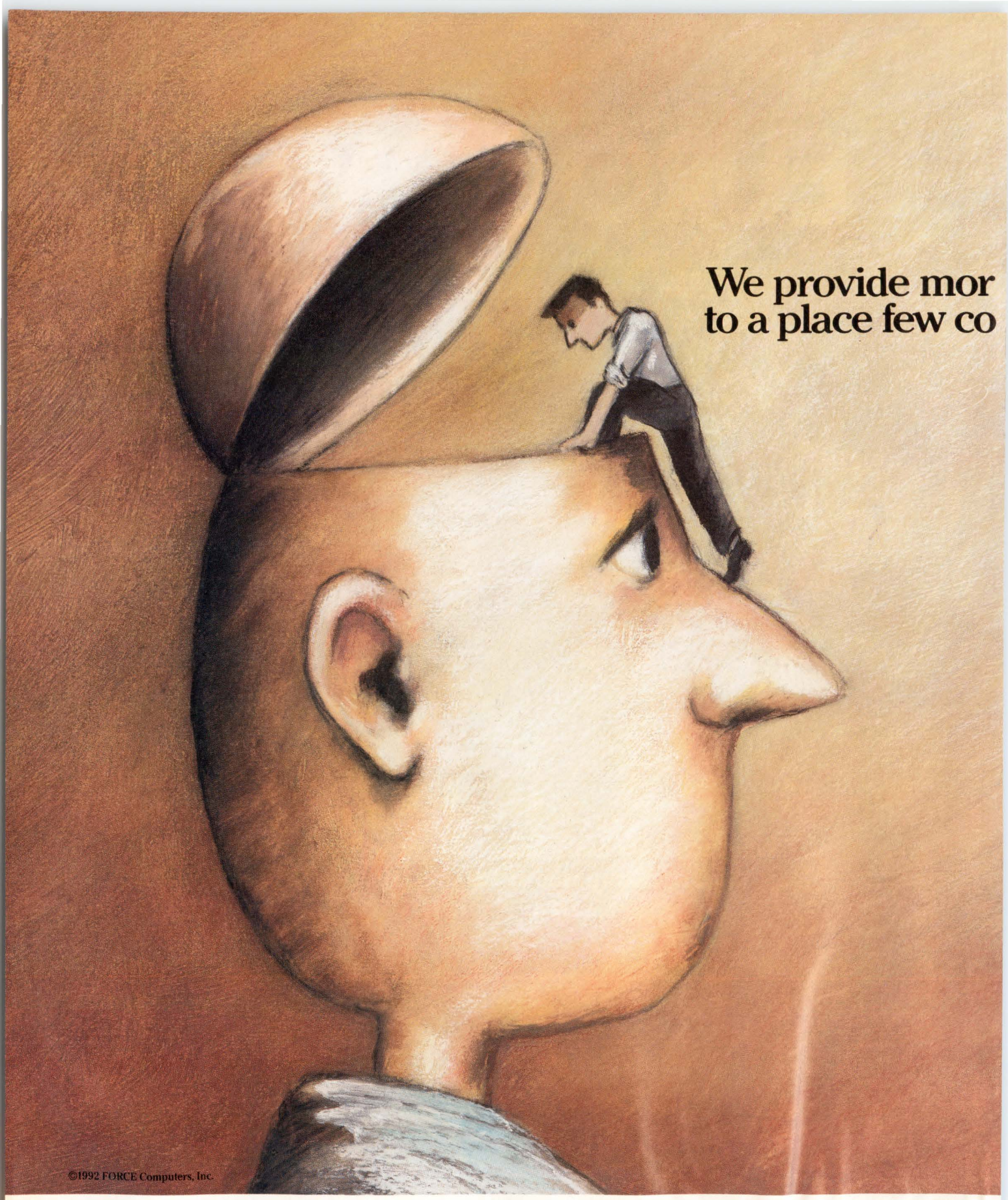
... Want to know more about this or any of ELTEC's other VME CPU, Graphics or Image Processing products then call or fax us now ...

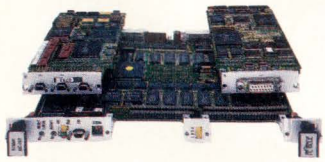
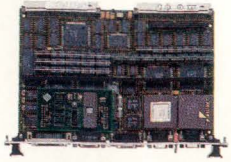
ELTEC - The complete VME solution.

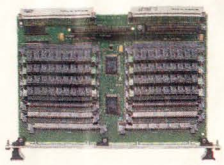
American ELTEC

USA: American ELTEC, Inc. • 4340 Stevens Creek Blvd. • Suite 204 • San Jose, CA 95129 • Tel (408) 244-4700 • Fax (408) 244-5544
U.K.: ELTEC International PLC • 45 Caldecotte Lake Drive • Caldecotte Business Park • Milton Keynes • MK7 8LF • Tel (0908) 366499 • Fax (0908) 274600
France: ELTEC International SARL • 1, Allée des Garays • 91120 Palaiseau • Tel (1) 64471877 • Fax (1) 64470933
Germany: ELTEC Elektronik GmbH • Galileo-Galilei-Straße 11 • 6500 Mainz 42 • Tel. (06131) 918-0 • Fax (06131) 918198

CIRCLE NO. 15





e solutions because we've been mpanies have dared to venture.

When it comes to embedded systems design, nobody offers better solutions than FORCE.

But, we have to admit, we had a little help. From you.

At FORCE, we get inside the heads of our customers to learn about their requirements.

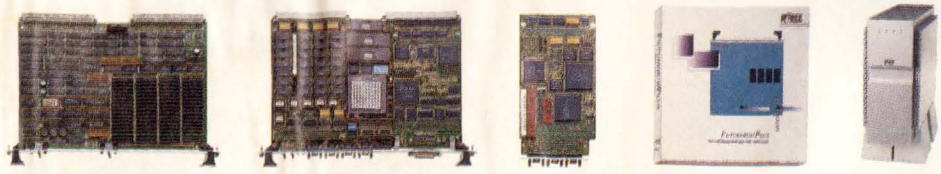
The result is the world's most advanced CISC and SPARC™ based VME single board computers, including the latest SPARC CPU-2E boards.

What else did you have in mind? How about bus extensions – like SBus and our own FLXibus.™ Plus SunOS™ and the widest variety of real-time operating systems and kernels.

And when your designs need to evolve to the next generation, count on FORCE for the best in VME64/Plus™ or Futurebus/Plus.™ Because better products come from better knowledge.

For a partner that can get your application up and running fast, call 800-237-8863, ext. 10. In Europe, call 49.89.608-14-0.

And thanks for keeping an open mind.



FORCE COMPUTERS®

3165 Winchester Blvd., Campbell, CA 95008-6557
Prof.-Messerschmitt-Str. 1 W-8014 Neubiberg/München

CIRCLE NO. 16

NEW & NOW

IRONICS SYSTEM 32™ OS-9™ Real-Time VMEbus Development/Target System

The *Complete* OS-9 System

SYSTEM 32 combines Ironics' proven hardware, Microware's tried and true OS-9™ Professional, with refinements that make SYSTEM 32 a *product – not a project!*

Power Tools — full ANSI C compiler and source debugger, UNIX "look-and-feel" libraries, and online tutorials get you up and running – *fast*!

ICEBOX™ System Case — the best VME enclosure in the world, optimized for accessibility, power, and cooling.

"Can Do" CPU— our 25MHz, 4MB 68030 host CPU gives you 4 Serial Ports, 1 Centronics/ Parallel Port, 68882 FPP support, and onboard SCSI and VSB interfaces – *standard!*

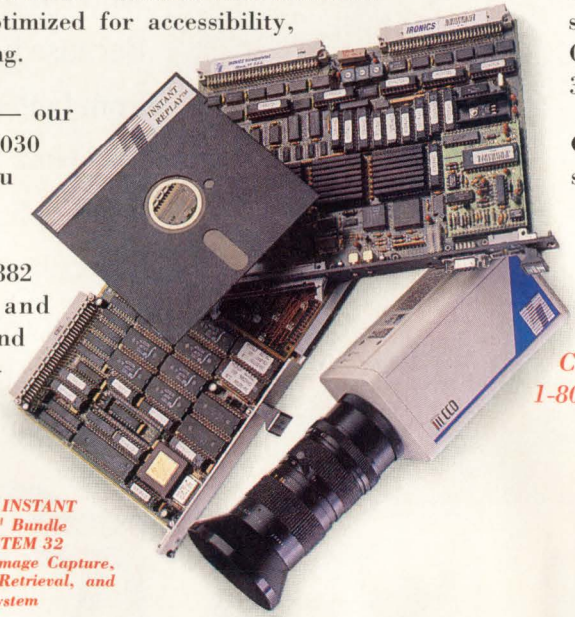
Add Ethernet, X-Windows, or Both — our industry standard networking and user-interface connections put the world at your fingertips.

Bolt-On Imaging and Graphics Capabilities — grab, transport, store, pre-process, retrieve, and display images with bundles like ***Instant Replay***.

MultiProcessing, Ready When You Are — no one knows MultiProcessing engines and software like Ironics. From a single CPU to a rack full of '040's, SYSTEM 32 answers your need for speed.

Custom Systems, To Go — if your system needs are out of the ordinary, you've come to the right place! Ironics' veteran System Integration Group can handle anything from mild to major customs.

Call our VME Product Hotline Today.
1-800-334-4812



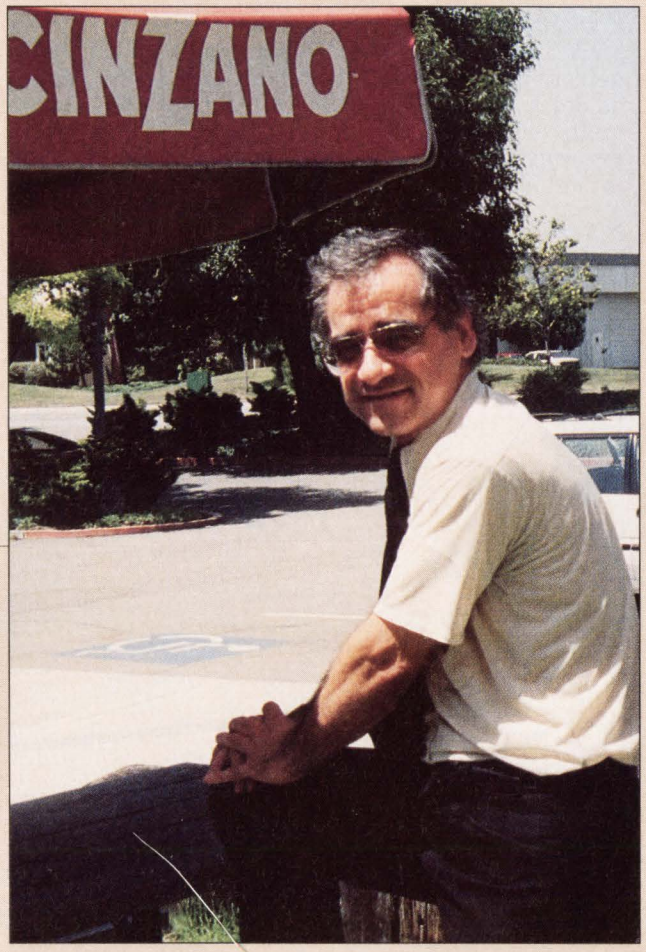
IRONICS INSTANT REPLAY™ Bundle Turns SYSTEM 32 Into An Image Capture, Storage, Retrieval, and Display System

IRONICS Incorporated

IRONICS INCORPORATED • 798 Cascadilla Street Ithaca, New York 14850 USA • 607-277-4060 Fax 607-272-5787

CIRCLE NO. 17

Dr. Alex Miczo on: Design for test



Test automation for ICs is finally taking its rightful place alongside design automation in importance. The problem of creating an efficient and exhaustive set of test vectors for an IC has always existed, but its enormous difficulty has consistently eluded automated solutions. Recently, some new approaches to automatic test design have matured to the point of commercial viability and are causing electronics designers to reevaluate their approaches to test. Fortunately, these tools come at a time when test generation has emerged as a bottleneck in getting new, high-quality electronics to market.

The goal of test automation is to accelerate test program development to achieve shorter time-to-market, higher-quality tests and reduced testing cost. Many test tool paradigms meet these objectives by trading off increases in silicon or design costs. It is important, therefore, to answer some end-product economic questions before evaluating any test automation solution: How much defect coverage does my product market require? What degradation in performance or chip cost can my end product accept? How many vectors can my foundry afford to support?

How much is good enough?

Recent studies by major electronics corporations and universities are helping to answer the question of how much coverage is good enough. The evidence clearly demonstrates the financial advantage of increasing defect coverage from less than 85 percent to more than 95 percent. This higher degree of testing reduces 'passed' defects by more than 15,000 parts per million of the total production run. Each company must translate for itself the savings that this provides in fewer service calls, reduction in bad inventory and elimination of expensive rework. These are typically large numbers, but perhaps of more importance is the company's improved quality image in the marketplace.

The task facing every test automation tool is basically the same: to find the minimal set of chip input that will push a possible error at any circuit node to the chip output for detection. Most solutions simulate electrical failures at each node, and then search forward through the logic for an unblocked path to the output (observability) and backward for a path from the input (controllability). The real difficulty comes in trying to navigate the heavily interdependent, clock-sensitive logic as the software looks for these pathways. For most designs, the search space approaches infinity, making unguided probes impossible. For example, an IC with 400 flip-flops and 100 I/Os has 10^{150} possible logic paths, which is orders of magnitude greater than the number of particles in the universe.

The original automatic test generation (ATG) programs required only a structural netlist of the circuit, and so imposed little if any change on the design. The netlist information proved insufficient, however, to guide ATG and the test coverage results were poor. Today's netlist-driven ATG products offer improved search algorithms and guidance file inputs, but the increasing complexity of designs continues to make the computer run-times unrealistic. As a result, users of these tools end up adding nearly total design-for-test structures to the sequential logic in their designs.

The name of the game is trade-offs

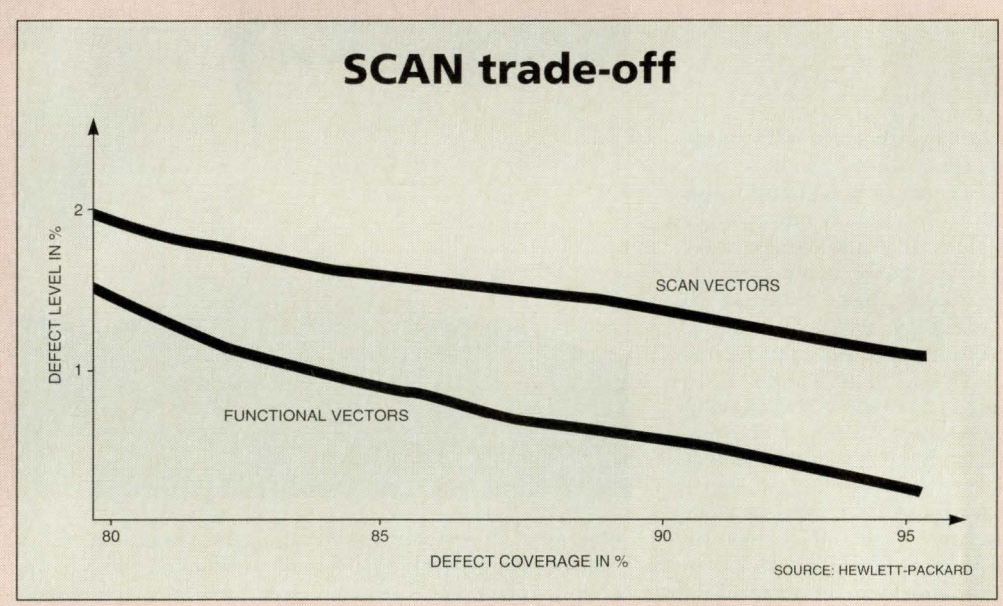
There are many factors which decide whether a company can accept a new design methodology for test development. The major trade-off occurs between the expected defect coverage of the test automation, and its impact on both the current design environment

Dr. Alex Miczo is the founder and chief technical officer of ExperTest, Mountain View, CA

and the silicon implementation. Defect coverage includes both static fault coverage at each node and detection of other common manufacturing flaws such as delay faults, transmission line effects and inadequate drive. Many of these latter errors can only be discovered by performing the tests under the IC's intended operating conditions.

Static vs. dynamic test

The ineffectiveness of netlist-driven ATG software has led some people to believe that the only solution to the IC test problem is to 'invade' the design with static test logic. This simplifies the task of creating high-static-fault-coverage tests by eliminating the sequential time sensitivity of the logic. The most mature of these methodologies is scan. It works by dedicating a minimum of three additional IC pins to a daisy-chained connection of all the storage elements in the design. During test mode, the storage chain is controlled by the scan pins, and can be set to known values for ATG. The result is typically high static fault coverage.



Scan design requires 10 to 30 percent more silicon, depending on acceptable levels of performance degradation, to implement the chain connection. Therefore, it can have significant penalties in die costs, speed and power consumption. In addition, scan mandates adherence to a set of design rules that may mean a change of style for designers; it can also constrain the use of many common design practices. One of the often unmentioned trade-offs with scan is that important manufacturing flaws in a die are not discovered because the chip is being tested statically rather than at the dynamic operating speed.

Another test insertion methodology which addresses the issue of testing at operating speed is offered by some ASIC foundries. This technology uses a grid of test structures laid over a gate array base wafer to provide a high level of circuit node observability in the ultimate design. The controllability issue for testability is still being addressed. As is the case with scan, designers have to consider the additional silicon costs and performance degradation of this new technology. Until it gains wider acceptance, foundry choice is limited to selected technology licensees and device families.

Next step—test synthesis technology

The newest of the emerging test automation solutions takes advantage of the trends toward logic synthesis and top-down design. This test synthesis technology, developed by ExperTest, uses the logic-synthesis register transfer level (RTL) model to guide ATG through the circuit. Knowing how the ASIC or custom IC works, the program can efficiently navigate even very complex control logic, such as coupled state machines. Typical benefits are much shorter computer runtimes, fewer vectors and coverage of between 95 and 100 percent, without the added overhead of scan.

In addition, this new ATG is ideally suited for optimizing the use of IDDQ testing. IDDQ can target CMOS-related faults not covered by the normal stuck-at model, but the tester measurements should be minimized because of their time duration.

The real benefit of using the design model to automatically create the test program is the linkage it provides between the two worlds. The designer can begin synthesizing test vectors at the beginning of the product cycle and can therefore evolve design and test concurrently. Like a smart test engineer, the model-driven ATG points out testability problem areas. The designer or test engineer can either let ATG automatically synthesize fully functional logic enhancements for test, or the change can be easily amended to the design model.

ExperTest ATG encourages functional testing, but it supports full scan, partial scan, built-in self-test, and boundary scan, to ensure compatibility with existing test methodologies. The flexibility, efficiency and quality that synthesis provides to design can now be applied to test.

For many technical markets in the 1990s, customer-measured quality will provide key product differentiation. From top to bottom of the electronic product manufacturing chain—including chip set vendors, board manufacturers, system integrators, and capital equipment providers—the supplier selection will be based on delivering 'known good' product. Incomplete tests on a $10 ASIC that causes an unexplained system crash on a $10,000 computer, a $500,000 communication switch or a $1 million medical imager won't be tolerated. Whether the ultimate test automation choice for a particular design is scan, test point insertion or design-driven ATG, the advantages provided by higher test coverage will be felt throughout the entire company and economy.

THE OEM POWER PLAY

The LBP-NX Laser Beam Printer Engine packs 17 page-per-minute printing power into a compact desktop unit. With its impressive throughput, high-volume paper capacity and acclaimed Canon reliability, the LBP-NX is the solid choice for OEMs who demand uncompromising, heavy-duty performance for their customers.

The LBP-NX features versatile two-tray paper handling, job offset for multiple users, and optional duplex capability to meet the demands of today's business. Plus Canon's ultra-fine toner has a smaller particle size than conventional toners, producing exceptionally sharp text and graphics. Canon includes this new technology in the patented, user-replaceable EP-N cartridge which houses virtually all consumables.

Canon is seeking OEM partners with value-engineering and marketing insight. To see how Canon can give you a powerful edge, call **1-800-323-0766** and ask for the Canon OEM Laser Beam Printer Design Guide.

SPECIFICATIONS	
Print Speed:	17 pages per minute
Paper Handling:	Letter, legal, A4, executive, envelope, OHP transparency, label stock
	Optional envelope feeder
	Optional duplex module
Paper Delivery:	Face up (50 sheets) Face down (500 sheets)
EP-N Cartridge Yield:	8,000 pages (at 5% coverage)
Dimensions:	17.9"W x 22.4"D x 19"H
Weight:	96.8 lbs.

The Engines that Drive the Industry™

Canon

CIRCLE NO. 18

Split decision on HDLs forces VHDL/Verilog coexistence

Barbara Tuck, Senior Editor

If you're fed up with arguments concerning the advantages of VHDL over Verilog or vice versa, and you simply want libraries and tools that help get your job done, you now have a good chance of getting your wish. VHDL and Verilog vendors are trying to figure out how the two hardware description languages can coexist, since designers are obviously not of one mind when it comes to an HDL of choice. VHDL vendors have accepted that those who made Verilog a de facto standard are not going to abandon it quickly. And Verilog vendors have only to look at the growth of VHDL use to accept that it has, indeed, established itself as a worldwide standard.

Where does that leave users?

If you're a VHDL user, you're left with IEEE on your side, a well-defined language that's being updated this year and a plethora of tools from which to choose, although most are immature and many don't conform fully to the 1076 specification. On top of that, you now have IEEE approval on the STD LOGIC 1164 nine-state multivalue logic system (MVL-9), and at least one ASIC vendor has begun delivering models. But you don't have a standard timing methodology. "VHDL has a long way to go before we would sign off on it," comments Laurin Ashby, manager of the Chandler Design Center for the ASIC Division of Motorola (Chandler, AZ), which today signs off on Verilog. Though VHDL is a very good high-level modeling tool, it can't match Verilog at the gate level, says Ashby. "If VHDL gets to the point where it can model to the detail of Verilog, we'd support it," she says.

If you're a Verilog user, you most likely have all the models and high-performance simulation you need, but IEEE acceptance is still ahead of you. You also have to wonder whether most of the newer tools with high-level system capability will be developed in VHDL, and if so, if you'll be pressured eventually to switch to VHDL anyway, particularly if you work for a multinational company.

If you use both VHDL and Verilog, you're left with a duplication of tools and models, none of which operate together, unless you happen to be a VHDL customer of Cadence Design Systems (San Jose, CA), using your Verilog models on VHDL-XL.

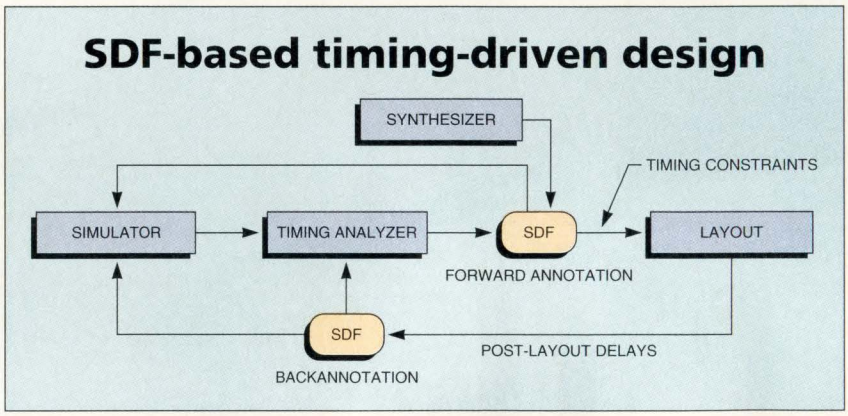
In short, whatever you're using, you're left with a design methodology full of holes, one that needs a lot of work before it will facilitate full-system designs. Though one language is the best answer over time, it's not impossible to have multiple languages, according to Cadence's president and CEO, Joe Costello. He adds, "The tragedy [would be] if there are two HDLs, [and] we don't make them workable for the system designer." Costello states that the semantics and syntax of VHDL and Verilog may not be the same, but that standard practices for the two could be.

Common ground

It's the standard practices and standard operating environment that make Verilog look better than VHDL on the implementation side, Costello explains, whereas VHDL, with its high-level constructs, is more robust at the system level. "Why not take everything you possibly can from the standard practices and operating environment of Verilog and incorporate them into VHDL to make it workable?" he asks. Cadence has decided to stay with its VHDL-XL, which shares simulation algorithms with Verilog-XL, instead of putting its support behind the Valid/Intermetrics VHDL simulator. VHDL-XL will have full language support by the fourth quarter, according to Costello.

He urges fellow vendors to stop hassling over languages and serve the user by putting energy into simulator performance, model availability, higher-level constructs, and methods of hiding the complexity of VHDL for ease-of-use. And he has a message to you, the user: "Take a leap of faith. Be part of the team that makes VHDL successful. VHDL is a long way from success at this point. There's too much vendor influence in VHDL and not enough input from users. Take control of both VHDL International (VI) and Open Verilog International (OVI) and combine the best of both worlds."

Andreas Hohl of Siemens (Munich, Germany) is chairman of



Cadence has proposed that its Standard Delay File (SDF) format, currently being used for Verilog, might be accepted as an industry standard, with modifications to make it appropriate for both VHDL and Verilog models. The proposal covers back-annotation of timing information appropriate for commonly used model characteristics such as pin-to-pin delays and wire delays. If the data used for back-annotation is in a neutral format, it can be used as a bridge between different tools in the design process, as well as between tools in different systems. In a timing-driven design flow, such as that illustrated here, the timing data forms the glue between the different aspects of the design process.

Now get four times the performance in our new logic analyzer.

At an even lower price per channel.

The new HP 16550A makes high-performance logic analysis affordable.

In 1987, HP set the price/performance standard for logic analyzers. Now, HP breaks through with a new price/performance standard. Introducing the HP 16550A logic analyzer module.

At 100 MHz state speed, the HP 16550A is fast enough for any processor you're likely to run into. Its 500 MHz timing speed makes measurements with 2 ns resolution. And it offers 102 or 204 (with 2 cards) state and timing channels with 4K samples each to capture the most elusive events.

Yet, all this performance costs less per channel than any other logic analyzer configuration in the HP 16500 family.

And since the HP 16550A is part of a modular system, you can create exactly the system you need now. Then add capability by adding a 1 GSa/s digitizing scope, 1 GHz high-speed timing, pattern generation, and the broadest list of microprocessor and bus support available.

Find out how to get breakthrough price/performance with the HP 16550A logic analyzer. For a brochure, **call 1-800-452-4844,** and ask for **Ext. 3045**. For a FAX data sheet, dial (208) 344-4809 from your FAX machine, access section 4 (Test and Measurement Instruments) and enter ID# 6503.

There is a better way.

HEWLETT PACKARD

Comparison of HP Logic Analyzers					
Configuration	**Max State (MHz)**	**Max Timing (MHz)**	**Memory Depth**	**# of Channels**	**Price***
HP 16510B	35	100	1K	80	$14K
HP 16550A	100	500	4K	102	$16.5K

*U.S. List Price includes HP16500 mainframe at $7.7K.

† In Canada call 1-800-387-3867, Dept. 445.

CIRCLE NO. 19

VHDL International

For more information about VHDL International (VI), or to get on the mailing list for *VHDL Times*, VI's quarterly newsletter, contact Michael P. Carroll, executive vice-president/chief operating officer, at:

VHDL International
407 Chester St
Menlo Park, CA 94025 USA
Tel: (800) 554-2550
(415) 329-0578
Fax: (415) 324-3150

VHDL International expects to hold its next Users' Forum this October in Washington, DC.

the VHDL Forum for CAD in Europe. He agrees that from a user's point of view, the coexistence of VHDL and Verilog makes sense. "There's no need to mix the languages," says Hohl, "but Verilog experience could be helpful with recommended practices." Much more effort is required, according to Hohl, to establish VHDL. "If VHDL claims to be a system language, we need to extend it to cover all system components, including analog and mechanical." Asked about the feasibility of merging VI and OVI, Hohl says the two groups might at least share common projects.

Discussions are indeed taking place between VI and OVI on the interoperability of VHDL and Verilog models. As chairperson of the VI Technical Advisory Committee, Dave Coelho, who's also executive vice-president at Vantage Analysis Systems (Fremont, CA), has entered into discussions with Hal Alles, corporate architect for Mentor Graphics (Wilsonville, OR), who chairs an OVI committee looking at model interoperability. "A special project committee sponsored by both groups is quite possible," reports Coelho. "We'll look at a whole range of solutions, including the possibility of VHDL and Verilog simulators talking to each other, as well as the possibility of translating models from one language to another."

Getting together on timing

The second area being considered as a possible common VI/OVI project is the review of the VHDL timing problem and establishment of a standard back-annotation file format for VHDL. VHDL designers going to silicon today have to use proprietary tools and ad hoc methods to settle timing issues. Though VHDL does contain configurations that can be used for this purpose, the methodology is reportedly clumsy, inefficient and not at all practical for large ASIC designs. Dr. Vassilios Gerousis, CAD system evaluation manager at Motorola (Chandler, AZ), chairs both an OVI committee on library modeling and a VI-sponsored IEEE working group evaluating a timing methodology for VHDL. Such a duplication of efforts has led to expectations that a special project group might be formed that would span both VI and OVI.

Open Verilog International

For more information about Open Verilog International (OVI), or to receive a subscription to *OpenExchange*, OVI's monthly publication, contact Deborah Kelley at the OVI office:

Open Verilog International
Suite 408
1016 East El Camino Real
Sunnyvale, CA 94087 USA
Tel: (408) 776-1684
Fax: (408) 776-0124
Email:OVI@netcom.com

The next OVI Users' Group meeting will be in Santa Clara, CA, March 23-24, 1993.

In the meantime, Cadence has proposed its Standard Delay File (SDF) to the IEEE working group as a neutral format for storing delay information. SDF is currently being widely adopted by ASIC vendors of Verilog libraries. VHDL purists might argue that SDF is external to VHDL, but Victor Berman, responsible for language strategy at Cadence, as well as being chairman of the North American Chapter of the VHDL Analysis and Standardization Group, says, "I don't deny it's outside the spec, but this is engineering, and the name of the game is to get the job done. Sometimes purity has to suffer for efficiency."

Mentor Graphics, which recently announced a multiphase program that will incorporate Verilog-XL into the Falcon Framework so that you can have access to Verilog as well as VHDL, had hoped that its Advanced Modeling Process (AMP) modeling specification would be adopted as the industry standard. Mentor is likely to insist that some of AMP's attributes are incorporated into SDF, or whatever timing methodology is finally adopted. SDF seems to have the edge since it has been adopted for Verilog.

If Verilog and VHDL are to be used together, it would make sense for the delay format of the two to be the same, independent of both languages and reflecting the physical hardware, according to Berman. Not only would the same timing semantic for simulation make sense if you were modeling in VHDL and Verilog together, but it also would if you were using the two HDLs separately, since it would let you compare what's happening with the expectation of similar results. For ASIC vendors, the same timing semantic for Verilog and VHDL would mean developing a single delay calculator, with a little difference perhaps in output formats for the two.

Cast your vote

Ultimately, it will be you, the user, who'll decide whether you want a single language over the long term. In the meantime, get in touch with VI and OVI and ask what you would get out of becoming a member. Since the IEEE is today the keeper of VHDL, it seems that a merger of VI and OVI is way more complicated than it might sound, as well as being highly unlikely from a political point of view, so you'll have to decide between VI and OVI, or you can join both. Watch, though, for special project groups that span the two. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Cadence Design Systems
(408) 943-1234 ..... **Circle 218**
Vantage Analysis Systems
(510) 659-0901 ..... **Circle 219**

Now You Can See True Colors Without Getting Soaked.

New full-featured RAMDACs from Brooktree deliver 24-bit true color for cost-conscious PC designers. Introducing four new RAMDACs that span the spectrum of PC applications, from 640x480 VGA systems to 1280x1024 workstation-quality graphics. They've got the right features, the right prices and are available right now.

True Color in a VGA Environment

Unplug Sierra. Plug in our totally compatible Bt481 or Bt482. You'll get 24-bit performance at 16-bit prices.

These new RAMDACs support 15-bit TARGA, 16-bit 5:6:5 and 24-bit true-color formats. They even allow you to switch between VGA and true color on a pixel-by-pixel basis.

Choose the Bt481 if you prefer an external hardware cursor. Or pick the Bt482 for its on-board 32x32x2 cursor — ideal for faster windowing environments.

Workstation Graphics at PC Prices

Introducing the Bt484 and Bt485, our newest mouth-watering RAMDACs. They combine true color with higher resolutions for higher performance graphics subsystems. And they're economical, too.

Bt485 operates at up to 135 MHz to drive pseudo color to 1280x1024 resolutions and gamma correct true color to 1024x768. It has a 64x64x2 cursor and all the serialization and timing to directly interface to a VRAM frame buffer.

Bt484 provides maximum flexibility with its programmable pixel port to provide 256 to 16.8 million colors, on-board 32x32x2 cursor and supports both interlaced and non-interlaced monitors.

Bt	Resolution			
Colors	640x480	800x600	1024x768	1280x1024
256	Bt481/Bt482			Bt485
64K				Workstation RAMDACs
16.8M			Bt484/Bt485	

Call Brooktree at **1-800-VIDEO-IC** for technical details and pricing today.

Brooktree Corp., 9950 Barnes Canyon Road, San Diego, CA 92121, (619) 452-7580, FAX (619) 597-0673.

Brooktree®

INTEGRATED CIRCUTS

Superscalar Sparc chips offer performance gains, compatibility

Tom Williams, Senior Editor

Superscalar design has now come to Sparc RISC architecture. In efforts to boost performance while avoiding many of the system design pitfalls caused by cranking up clock speeds to 100 MHz, Cypress Semiconductor (San Jose, CA) and Texas Instruments (Dallas, TX) have opted for parallel instruction launch and multiprocessing based on the widely popular Sparc architectural specification. Each has announced superscalar implementations of Sparc that will allow virtual drop-in performance upgrades for existing system designs and will run existing binary code—with significant performance gains.

The Texas Instruments TMS390Z50 SuperSparc CPU chip and the Cypress CYM6200 HyperSparc family of processor modules differ significantly in terms of design philosophy and moderately in terms of performance, although claims by the two companies are difficult to compare exactly. Cost differences are not yet certain, because Cypress has yet to set pricing on its modules, which it has scheduled for full production in the fourth quarter of 1992. The TI chip is now in production in its 40-MHz version, with the originally projected 50-MHz version to become available later this year. TI is quoting a quantity price of $400.

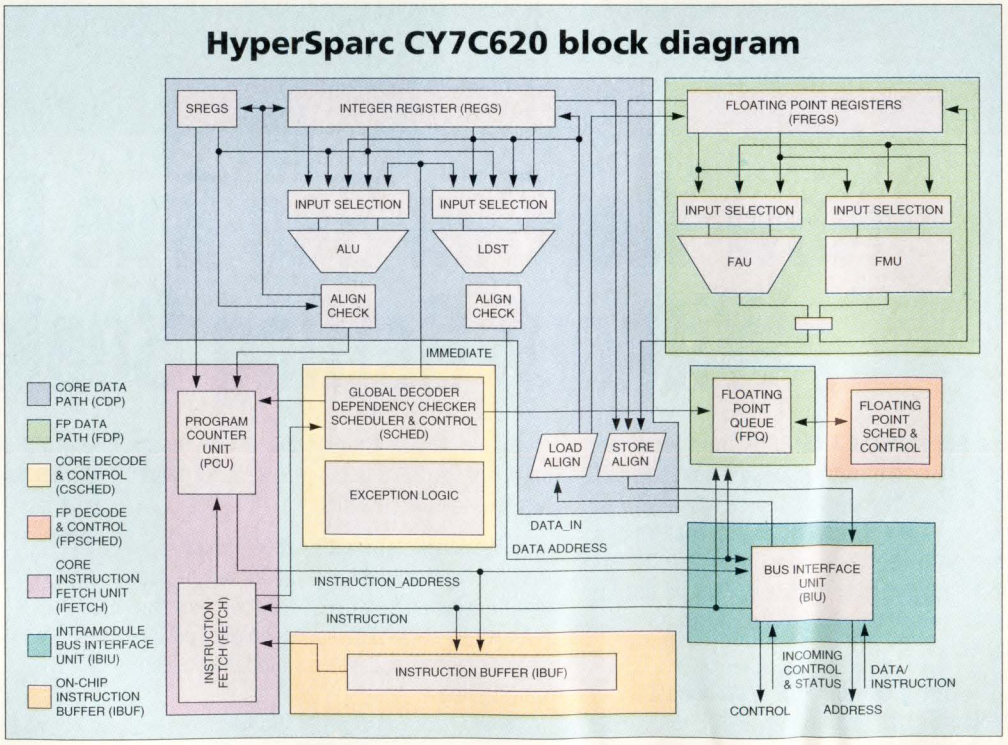
What's inside

The most striking difference between the two CPUs is that the TMS390Z50 is integrated on a single silicon chip that includes the superscalar engine (capable of up to three instructions per clock cycle), a 64-bit floating-point unit, memory management, bus interface, 20-kbyte instruction cache, and 16-kbyte data cache. TI's design uses 3.1 million transistors on a 15.8 mm^2 die; it's implemented in TI's 0.8-µm Epic IIB triple-metal BiCMOS process. The Cypress CYM6200 family, which initially will have three versions, is based on three ICs in its HyperSparc chip set integrated on an M bus module.

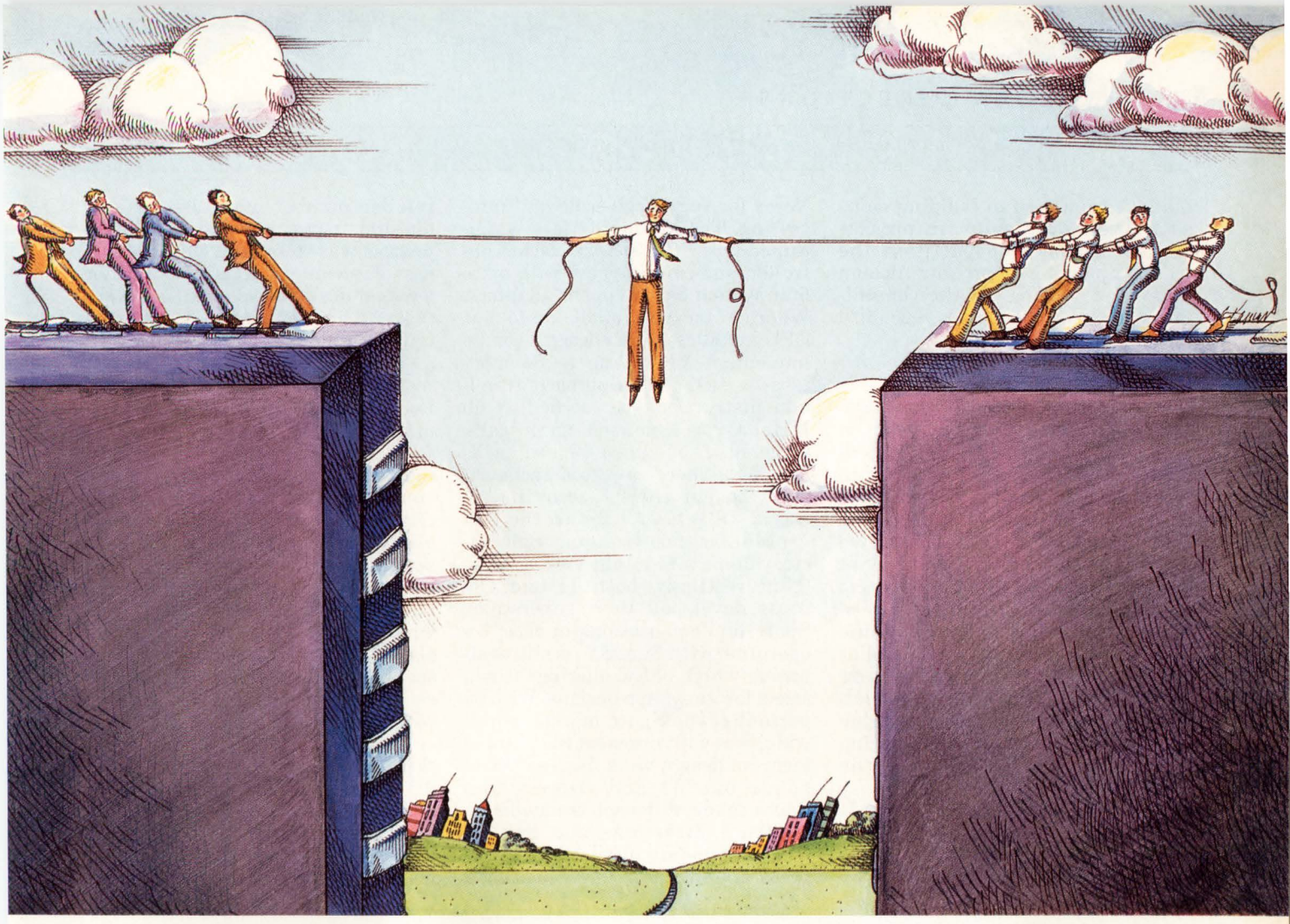
The CYM6200 family of modules consists of three elements: the CPU, the CY7C625 cache controller/MMU tag unit, and two or four CY7C627 cache data units. Modules in the family differ by having one or more CPUs and two or four cache units (128kbytes or 256kbytes respectively). The CY7C620 CPU includes integer and floating-point units and an 8-kbyte two-way set instruction cache; it's capable of launching two 32-bit instructions per cycle. It contains 1.2 million transistors. The cache controller/MMU unit controls the cache memory units that are not integrated on the CPU and also interfaces to the M bus at 40 MHz. The CPU modules communicate via a proprietary intramodule bus that can scale in speed as the internal CPU speed is scaled upward to 100 MHz, while maintaining a separate clock for interfacing with the M bus.

The TI SuperSparc chip also maintains separate clocks—not, as in the Intel 80486, a single clock with divided frequencies—so that the processor can run faster than the interface to the M bus for ease of upgrading system performance.

According to Roger Ross, president of Ross Technology (Austin, TX), the Cypress subsidiary that developed HyperSparc, cost played a major role in the decision to partition the design among IC modules. "When you double the size of a piece of silicon, you double its price," he says. Also, he noted that Ross Tech-



In the Cypress HyperSparc CY7C620 CPU, the two-way set associative instruction buffer can store 2,048 64-bit instructions. The core data path handles all integer instructions, plus load and store. It has eight overlapping register windows and eight global registers (136 total). The core instruction scheduler decodes, groups, schedules, and dispatches instructions. It can launch two instructions per clock cycle to any two of the four logic blocks (load/store, branch/call, integer, and floating-point).



TI's 7.5-ns '22V10. For those times you're torn between profit and performance.

Trying to get the best performance on a tight budget can create a few hang-ups. Texas Instruments has a simple solution. Introducing the TIBPAL22V10-7. TI's newest high-performance programmable logic device that's designed to fit the bottom line as easily as it meets your design specs.

High performance, low price

While competitive pricing is one of our '22V10's most outstanding features (less than $17 when you purchase 5,000 or more), you'll be even more impressed by its performance.

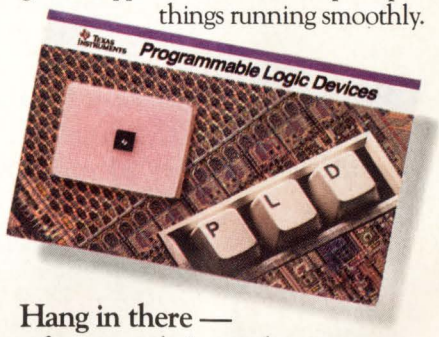
At an incredibly fast 7.5 ns, our '22V10 supports system speeds up to 50 MHz with a variable term distribution that gives you more design freedom with complex functions. It's an excellent choice for high-end systems using the latest microprocessors. And since all this is achieved using our proven bipolar process, the '22V10 provides a universal architecture that's easy to work with using familiar design tools.

Accurate, dependable and available today

Speed and ease of use mean nothing if difficult programming keeps your product from getting to market on time. That's why our '22V10 is designed for quick, dependable programming with your present tools. In fact, we're running at a 99.4% first-time programming success rate.

Best of all, our 7.5-ns '22V10 is available in volume *today* with just-in-time and ship-to-stock delivery programs tailored to meet your needs. You'll also have the backing of our global support network to help keep things running smoothly.

08-1287



Hang in there — a free sample is on the way

Simply return the attached reply card or **call 214-995-6611, ext. 3717**, for one free TIBPAL22V10-7.

TEXAS INSTRUMENTS

INTEGRATED CIRCUITS

nology's approach to building chips as if they were software projects makes it easier to partition the work, by using a smaller design team and putting off the commitment to actual physical layout until late in the design cycle.

Modules do even more

The major area of competition—and no doubt the largest market—for Cypress and TI will be in M bus modules, since TI will be offering a family of M bus designs as well. The SuperSparc M bus module consists of a single CPU chip on a standard M bus plug-in board. A module with more external cache memory is also available in the form of the Multicache module, which includes the SuperSparc multicache controller and 1 Mbyte of SRAM cache memory. In 1993, TI will introduce a dual-CPU Multicache module. All "glue logic" for multiprocessor interfacing is incorporated on-chip on the TMS390Z50.

In addition to running on the M bus, the TI Multicache modules can be selected to operate on the X-bus packet-switched mode developed by Xerox for very large-scale multiprocessing. The X-bus interface is contained in the SuperSparc cache controller, and can interface with up to four system buses via bus adapters. Where M bus can handle up to four CPU modules, X-bus designs can be implemented with up to 64 modules—which could approach 10 billion instructions per second at 50 MHz. Cypress hasn't specifically targeted its modules for use on X-bus, but "there are good technical ways to get there," according to David Ditzel, director of the Advanced Systems Group at Sun Microsystems (Mountain View, CA).

Interestingly, both TI and Cypress developed their superscalar Sparc implementations in close cooperation with Sun. Sun is still evaluating which of the offerings it will select for its system designs. With 63 percent of the Sparc market worldwide, Sun will represent the plum in terms of design wins. But, as Ditzel points out, TI and Cypress/Ross "have made different trade-offs in different directions and neither CPU will go into all platforms." Cypress' stated aim in implementing a smaller number of transistors per die and using a two-metal CMOS process was to build a CPU module for volume manufacturing suited for low-cost desktop systems. The eventual pricing announcements from Cypress should tell the story there.

Performance gains right away

Both TI and Cypress are claiming immediate performance gains of 2 to 3× over previous Sparc implementations using existing applications and compilers. Actual performance differences between RISC chips are always hard to quantify without exact measurements that deal with such questions as: how many Specmarks at what clock speed with what cache? The two companies' claims also quote different clock speeds and make the usual differing estimates of the other's performance when doing comparisons.

But Eric Schmidt, president of SunTech, Sun's software business development branch, says the real story is in the software compatibility that comes with the performance gains. "At least a doubling in performance at the same clock speed simply

Use our low power, low voltage memory and buy more time.

If you design battery operated systems such as laptop and notebook computers, Micron's low power, low voltage memory components can buy you more time.

Micron's extensive line of leading edge, low power, low voltage DRAMs and SRAMs are designed to give you optimum 3.3 volt operation in battery powered systems, extending battery life and system operating time. Since the parts run cooler, they also increase system reliability. And we offer the latest packaging technologies such as TSOP and PQFP.

So call Micron today at 208-368-3900. And find out how to buy more time.

Micron. Technology that works for you.

Part Number	Memory Configuration	Availability
3.3 Volt, Low Power, Extended Refresh DRAMs		
MT4C4001J VL	1 Meg x 4	3Q92
MT4LC4001 S*	1 Meg x 4	4Q92
MT4LC4001 L	1 Meg x 4	4Q92
MT4C4256 VL	256K x 4	Now
5 Volt, Low Power, Extended Refresh DRAMs		
MT4C1004J L	4 Meg x 1	Now
MT4C4001J L	1 Meg x 4	Now
MT4C8512 L	512K x 8	3Q92
MT4C16256 L	256K x 16 DW[1]	3Q92
MT4C16257 L	256K x 16 DC[2]	3Q92
MT4C1024 L	1 Meg x 1	Now
MT4C4256 L	256K x 4	Now
MT4C1664 L	64K x 16 FPM[3]	Now
MT4C1670 L	64K x 16 SC[4]	Now

Part Number		Memory Configuration	Availability
3.3 Volt, Low Power Specialty SRAMs			
MT5LC2818	Latched	16K x 18	Now
MT58LC1618	Synchronous	16K x 18	Now
MT5LC2516	Latched	16K x 16	Now
MT58LC1616	Synchronous	16K x 16	Now
5 Volt, Low Power, Low Voltage Data Retention SRAMs			
MT5C1001 LP		1 Meg x 1	Now
MT5C1005 LP		256K x 4	Now
MT5C1008 LP		128K x 8	Now
MT5C2561 LP		256K x 1	Now
MT5C2564 LP		64K x 4	Now
MT5C2565 LP		64K x 4 $\overline{OE}$[5]	Now
MT5C2568 LP		32K x 8	Now

*Self Refresh [1]DW– Dual Write Enable [2]DC– Dual $\overline{CAS}$ [3]FPM– Fast Page Mode [4]SC– Static Column [5]$\overline{OE}$– Output Enable

MICRON TECHNOLOGY, INC.

2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3900
Customer Comment Lines: U.S. 800-932-4992; Intl: 01-208-368-3410

CIRCLE NO. 22

INTEGRATED CIRCUITS

by plugging in a different M bus module is a virtual certainty in both cases, even if we wait until later to sort out the details." Add the multiprocessing capability offered by both vendors, and price/performance will go even higher. Schmidt notes that Sun's new Unix operating system, Solaris (Versions 1.0 and 2.0 are out), already has multiprocessor support. He predicts that future systems will be "multiprocessing multithreaded everywhere."

While these gains are available immediately on the hardware side, compiler technology will take some time to exploit the opportunities offered by the new implementations. Schmidt wouldn't speculate as to what increments of performance improvement could be expected from compilers that could take advantage of such things as scheduling instructions for parallel execution and making more efficient use of the pipeline. Wayne Rosing, president of SunLabs, Sun's R&D group, suggested, though, that users would be "pleasantly surprised."

Sun's Ditzel points out, however, that advances in compiler technology in the Sparc world usually benefit all Sparc hardware implementations. Furthermore, code generated by a compiler tuned for the Cypress or TI superscalars would still run on other Sparc implementations, even if not as efficiently.

As to development support, SunPro, Sun's development tools branch, has announced support for the TMS390Z50 with its Sparcworks suite of development tools. At the same time, SunPro announced that it was working on releases of its tools, especially compilers, that could further exploit the TI SuperSparc's superscalar features. Sun hasn't made any announcements regarding support of the HyperSparc, but existing Sparcworks tools will be binary-compatible as well.

For its part, Texas Instruments is supplying a $50,000 system design starter kit consisting of a SuperSparc simulator that includes additions for caches, MMU and store buffers, a Verilog model that allows behavior modeling of the CPU and the Multicache/bus controller, and a JTAG-based scan tool for boundary-scan testing of board- and system-level designs. The kit also includes documentation and an M bus designer's guide. ■

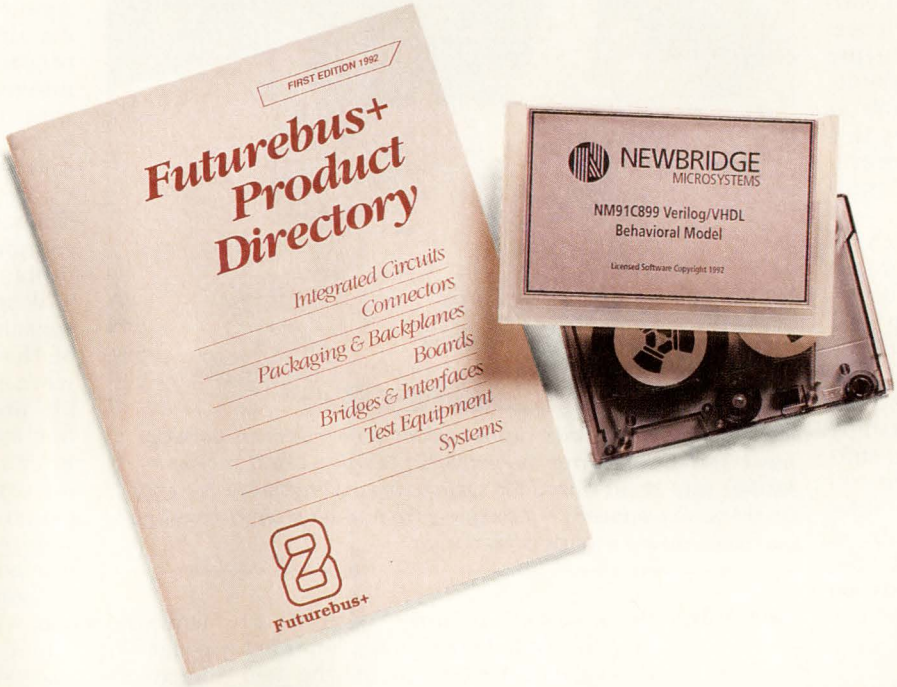
For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Cypress Semiconductor (408) 943-2600	Circle 200
Ross Technology (512) 892-7802	Circle 201
Sun Microsystems (800) 821-4643	Circle 202
Texas Instruments (800) 336-5236 ext.700	Circle 203

It's high performing...

When your Futurebus+ card needs to take control of the full 64 bit address data path our low power consumption Futurebus+ Arbiter and Compelled Interface can provide all the performance you'll need.

- High performance IEEE 896.1-1991 Futurebus+ Profile B Compliant Compelled Interface.
- Support for Futurebus+ compelled mode data transfer protocols as both master and slave.
- Internal DMAC and Futurebus+ programmable registers so the NM91C899 can be used in applications ranging from simple "non-intelligent " slave I/O boards to single board computers utilizing RISC or CISC microprocessors.
- Distributed arbitration or arbitrated message applications by using the NM91C899 in conjunction with the NM91C896.
- Direct connections can be made to the central arbitration handshake lines if distributed arbitration is not used.
- NM91C899 interface controller implements all the IEEE 1212 required CSRs.



see for yourself.

Verilog/VHDL behavioral models are available to evaluate our high performance interface devices for your design or for board and system performance simulations. Give us a call at 1-800-267-7231.

NEWBRIDGE
MICROSYSTEMS

The Futurebus+ Product Directory was provided courtesy of VITA, Scottsdale AZ. For a copy call (602) 951-8866.

CIRCLE NO. 24

SOFTWARE & DEVELOPMENT TOOLS

Tool suite targets 32-bit microcontrollers

Tom Williams, Senior Editor

The complexity and specialization of today's 32-bit designs are throwing new challenges at development tool vendors. Complexity translates as 32 bits, and specialization means microcontrollers with all their application-specific peripheral devices, such as timers, I/O, RAM, ROM, and DMA controllers. The upshot is that ever larger and more complex programs have to be created and maintained by an engineering community that's facing shortages of both people and experience. The task of producing tools that are affordable, adequate to the job at hand and usable by this overstressed community has become daunting.

According to Richard Jensen, vice-president of new business development for Applied Microsystems (Redmond, WA), 32-bit embedded systems are making increasingly heavy demands on software engineering resources—roughly double the demands of 16-bit projects. By contrast, the demands on hardware engineers have risen only moderately.

Richard Jensen, Applied's vice-president of new business development (seated on desktop, behind Brian Crowley, CPU32 project leader), says 32-bit embedded systems are making heavy demands on software engineers, but the jump from 16-bit projects hasn't impacted hardware engineers that much.

System know-how

The fragmentation of applications into specialized areas is driving two trends. One is, of course, that semiconductor vendors are addressing specialized application areas (automotive, military/aerospace and communications) with specialized microcontrollers. The second is a crisis in experience. There's a serious shortage of experienced software engineers, although software engineering is only part of the problem. A good programmer may not have adequate knowledge of the application being programmed, and a person with detailed knowledge and experience of the application may not be an experienced programmer.

"Application experience is a far more valuable thing to put on a team than programming experience. A company doing a sonar is better off getting a chief petty officer off a submarine, and they'll teach him how to program," says Jensen. But somebody has to know the insides of the processor or microcontroller to help him out, Jensen adds, "and that pressure is being put on the tool companies." So, on the one hand, an applications expert has to learn enough about general-purpose programming to apply his or her knowledge, and, on the other hand, tools have to shield this expert from the need to deal with the detailed innards of the specialized and very complex microcontrollers being worked with.

Estimates by Applied Microsystems show that a typical 32-bit embedded system project may have from three to five hardware engineers, but requires between 10 and 30 software engineers. With that many people being paid hefty salaries, a development organization faces the challenge of how to give them all useful tools without spending itself out of existence, how to keep them all productively busy and how to achieve the best time-to-market.

One caveat Jensen offers is this: "Doing your own real-time kernel is the worst business decision you can make." In this situation one or two engineers are doing what vendors who are experts in the field have already done very well, while the rest of the team is waiting to start the project. Beyond that, Applied Microsystems is pushing its concept of a proper mix of tools in an integrated environment that includes software simulation for binding code to the hardware environment and emulation for solving the most complex timing-related problems.

Where it was once acceptable to equip each of the one or two software engineers on an 8-bit project with his or her own $5,000 emulator, emulators for 32-bit microprocessors are too expensive for the larger teams of engineers needed for this work. But the generic activities remain the same: write and debug the code's logic, bind it to the target hardware's physical environment and check and debug timing-relatedissues.

Tackling 32-bit controllers

Applied Microsystems has made an aggressive thrust in one segment of the 32-bit microcontroller arena with suites of tools for three members of Motorola's CPU32 family. The supported processors are the 68330, 68340 and 68F333, each of which is based around the 68020 CPU core but with its own mix of on-chip peripheral devices. The company's strategy is to emulate the core processor and isolate the application-specific functions—to switch to a dif-

Optimize your 680x0 Application to its peak

...with Oasys Embedded/Cross Software Tools.

Reach the pinnacle of your development with Oasys Cross Tools

Oasys delivers full 680x0 Cross and Native development tool kits built around the industry standard Green Hills compilers.

The Green Hills 680x0 compiler's Dhrystone rating is 35% faster than Sun's native C compiler. Using the new procedural inlining optimization, the rating jumps to a staggering 80% improvement.

Advanced C, C++, FORTRAN and Pascal Language Support

- Full ANSI C XJ311 support with switch selectable K&R C support.
- A true *C++ Compiler* for cross development.
- FORTRAN 77 with VAX VMS and DoD MILSTD-1753 extensions.
- Pascal ISO Level 1 support.
- All compilers are inter-language callable.
- Native compilers are supported for 680x0, 88000, 386™ & i860™ microprocessor hosts.

Available Now!

Oasys tools are available on over 35 UNIX based workstations and systems including DEC (VMS/Ultrix), Sun, HP/Apollo, IBM (OS/2 and AIX), and DG. Call us for the complete list.

Other Cross Tool Kits include:

88000, 80386, i860 and Microsoft C.

Integrated 680x0 Cross Development Tool Kits

Green Hills 68000/10/20/30/40 Optimizing Cross Compilers (C, C++, Pascal, FORTRAN)

- Superior register allocation, inlining and loop unrolling techniques.
- Support for position independent code and data.
- 68881, 68882, 68332 support.
- ANSI C run-time source library included for cross development.

Oasys UDB Universal Debugger

- Source level remote debugger for embedded programming.
- Multi-targeted and multi-window (supports 680x0 and 88000 targets).
- Extensive macro language.
- Customize communications to your target.

Oasys 680x0 Assembler/Linker

- Macro Assembler, Linker, Librarian, Cross Reference and Symbol File Format Utilities.

Oasys 680x0 Simulator

- Invaluable for debugging software without target hardware.

Call Now for a FREE
MULTI Debugger Demo Disk!
(for SUN-4 SPARC only)
(617) 862-2002

Oasys

Worldwide Support: Australia—Forefront Computing Svcs 03-785-1122 **Benelux**—Computing & Systems Consultant 040-434-957 **France**—RTS 01-6986-1958 **Germany**—Stollman 040-890-880 **Israel**—Ankor Computers Ltd. 972-3-5483737 **Italy**—Instrumatic 02-353-8041 **Japan**—ERIC 03-668-8866, MCM 03-487-8477 **Norway**—OTE Komponent 02-30-6600 **Singapore**—Automated Systems Ltd 02-789-9566 **Spain**—Decisa 01-204-4500 **Sweden**—Traco AB 0893-0000 **Switzerland**—Zuhlke Engineering AG 01-730-7055 **UK**—Real Time Products 021-236-8070

One Cranberry Hill, Lexington, MA 02173

Single Source, Total Solutions

CIRCLE NO. 25

SOFTWARE & DEVELOPMENT TOOLS

ferent microcontroller, then, you need only change the probe head and software on the same emulator box.

The CPU32 family of development tools consists of an instruction set simulator, a CodeTap hardware debugging probe and a 32-bit emulator. All tools are tied together via Applied Microsystems' Validate/XEL interface, which is based on Hewlett-Packard's Softbench environment.

With the instruction set simulator, you can begin developing and debugging target-specific code on the host system before any target hardware is available. You can write high-level source code on a PC, Sun or DEC workstation, compile it to the target code and debug at either the source or assembler level. The simulator is aimed at solving problems of code logic that are not dependent on hardware but are usually the most numerous in any operation. With prices starting at $2,000, the simulator can be provided for almost everybody on a project.

For the majority of hardware-related integration problems—that is, fitting the code to the target environment in terms of I/O addresses, memory ranges for ROM and RAM, interrupt lines, and other factors—Applied Microsystems supplies a CodeTap tool for each of the three supported members of the CPU32 family. CodeTap's probe head carries a microcontroller plus a monitoring chip that lets you set hardware breakpoints and debug code in the hardware environment without actually using any of the target's memory or I/O resources. Debugging doesn't include the detailed timing-dependent problems which require a full emulator. But with the EL 3200 emulator selling for about $20,800, the $6,500 CodeTap provides a cost-effective solution for the hardware-binding class of problems.

"Application experience is a far more valuable thing to put on a team than programming experience."

—Richard Jensen
Applied Microsystems

Applied Microsystems will also be sourcing Motorola's single-board evaluation boards for the CPU32 family. Those who want to get started running code immediately on target hardware need only plug the CodeTap head into the evaluation board. Of course, the evaluation board may not have all the characteristics of whatever specialized system is under design, but it provides a means of making progress at the

Spend three days at the '92 Embedded Systems Conference.

Spend the year using what you learned.

Helpful. Inspiring. Top Notch. Excellent. These are just some of the words our past attendees use to describe the Embedded Systems Conference faculty. In just three days you'll find answers to the toughest questions you face presented by leaders in the embedded development community. Faculty who know your job is becoming more complex; who work everyday on real workable solutions to the toughest problems you face. People like Larry Constantine, Steve Mellor, Paul Ward, Derek Hatley, Imtiaz Pirbhai, P.J. Plauger, and Michael Slater.

Build Your Own Program.

Customize your own program by choosing from over 75 lectures and workshops that cover a wide range of issues in embedded development. You'll get top notch advice on real-time programming, CASE and object-oriented methodologies, embedded project management, programming languages, debugging and algorithms and much more.

Attendees can choose from over 75 technical sessions led by the leaders in embedded development.

Try Out The Latest Technology At The Embedded Systems Development Products Exhibition.

The Embedded Systems Conference will also be the site of the largest most highly targeted exhibition of embedded development products and services. Nowhere else will you find all the latest tools and utilities on display at one time.

The Santa Clara Convention Center is conveniently located in the heart of Silicon Valley.

You'll Come Away With New Ideas That Translate Directly Into Increased Productivity.

Most importantly, the Embedded Systems Conference is a peer environment that fosters dynamic exchange of vital information, ideas, and insights. You'll find professional excellence throughout the conference; in the lectures and workshops, on the floor of the exposition, in the tutorials, and in informal receptions and hospitality events. And you'll get it all in three days.

Over 120 exhibitors will be showcasing cutting edge tools and utilities.

Phone us, fax us or mail us today for more information.

TEL: (415) 905-2354
FAX: (415) 905-2220

THE FOURTH ANNUAL EMBEDDED SYSTEMS CONFERENCE

SEPTEMBER 21-24, 1992

SANTA CLARA CONVENTION CENTER
SANTA CLARA, CALIFORNIA

❒ **YES! Please send me more information about the Embedded Systems Conference.**

Name_____ **Title**_____

Company_____

Address_____

City_____ **State**_____ **Zip**_____

Phone (_____)_____ **FAX** (_____)_____

Send info on: ❒ attending ❒ exhibiting **Please also send info to:**_____

CDES

Mail or FAX to Embedded Systems Conference Miller Freeman Inc.
P.O. Box 7843, San Francisco, CA 94120-7843 — TEL (415) 905-2354; FAX (415) 905-2220

CIRCLE NO. 27

hardware/software integration stage before a final design prototype is ready.

Finally, Applied Microsystems has developed a version of its EL 3200 emulator for the CPU32 family. The EL 3200 comes with a probe head for one of the supported microcontrollers; the other heads and their associated software can be substituted. An optional 16-bit logic state analysis probe is available for monitoring points of interest in the target system.

Emulator's new features

Among the new features of the EL 3200 are the ability to set breakpoints in ROM or in shared or dual-port memory—especially useful for embedded systems—as well as its dynamic pin tracking. The 68330 and 68340 have pins that can be configured in software to serve different functions. For example, the upper eight address lines can be used first as address lines and then switched to act as a parallel port. What's more, this can be done dynamically as the program is running. The EL 3200 can keep track of such switchable pins by monitoring the instruction stream via the instruction pipeline and instruction fetch signals, looking for writes to the internal registers that configure the states of the external pins.

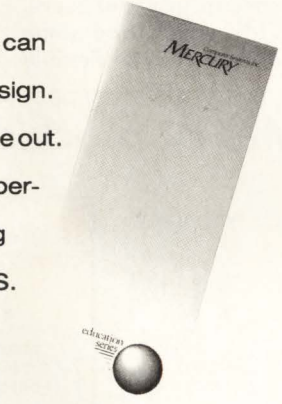
The proliferation of microcontrollers has presented a large challenge to tool vendors, because no single CPU can cover all the vertical markets. But as Jensen notes, "This is an expanding market because they [the semiconductor manufacturers] are doing this, they're getting greater application opportunities." Given the intricacies of the different controllers, the prospects for tool vendors to provide adequate tools for developing systems are also quite challenging. Meeting that challenge will require ever more effort from tool vendors, as well as cooperation from semiconductor vendors. ■

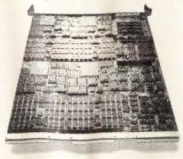
For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Applied Microsystems
(800) 426-3925 ..... Circle 217

FOR THOSE WHO THINK ALL ATTACHED PROCESSORS ARE ALIKE, PROCESS THIS.

Your choice of processors can make or break your system design. Performance in = performance out. So start with the leader in high performance real-time computing solutions. Mercury's MC860VS. The only attached processor that offers up to 32 Intel i860s in no more than 8 VME slots. So you get 80 Mflops to 2.5 Gflops to handle the most demanding applications in defense signal processing and medical imaging. And all Mercury products can be configured in workstations and chassis systems to deliver scalable performance at a scalable price. So if you're building or buying a high performance computing solution, take advantage of Mercury's unparalleled investment in standards, innovative hardware, and software development environment. And get the most complete, flexible, high performance computing solutions available. If you've been thinking about multiprocessing solutions, here's some important information to process:





☐ I want to learn more.
Send me your white paper "Multiprocessing for the 1990s."
☐ I want to subscribe to Mercury's ongoing Education Series.
☐ Please send me more information on the MC860VS right away.

Name _____
Title _____
Company _____
Address _____
City/State/Zip _____
Phone _____

Please send to
600 Suffolk Street
Dept. K.
Lowell, MA 01854
Fax (508) 458-9580
(508) 458-3100

Computer Systems, Inc.
MERCURY

CD 7/92

Mercury's MC860VS. The Ultimate Performance Machine.

IDA INSTANT DATA ACCESS (IDA) DIAL (617) 494-8338 DOCUMENT NO. 1020

CIRCLE NO. 29

COMPUTERS & SUBSYSTEMS

Major board vendors keep up with shift from traditional bus-based systems

Warren Andrews, Senior Editor

Although the standard-bus industry continues to leverage its way into proprietary-bus solutions in many application areas, the same standardized boards that are replacing proprietary solutions are being abandoned by designers who have traditionally relied on them to build systems around non-proprietary buses, primarily because of size and cost. In response, board vendors are beginning to offer alternatives which may be the first steps in a changing of the guard, fragmenting once-sacred VME application areas.

The processing power and I/O now available on a single board are making it possible in many cases to eliminate a backplane and interface circuitry, as well as software for multiple-board solutions. On the other hand, another set of applications is emerging that's so complex that new multiboard solutions are being sought.

There's been change for some time at the high end, what with multiprocessor boards, fault-tolerant hot-swap systems and fast crate-to-crate communications, but low-end systems are just starting to veer away from the traditional. The first to take advantage of the shift from traditional VME use has been Sun Microsystems (Mountain View, CA), which not only offers an alternative to VME, but announced it will soon get out of the VME business altogether in favor of its single-board solutions depending on SBus modules.

Force Computers (Campbell, CA) has followed Sun's lead by offering its 2S board, primarily a VME single-board computer without the VME interface. Unlike Sun, though, Force plans to remain a power in the VME business. In fact, it's part of Sun's strategy to transfer its technology to Force, so that the latter company can continue to support those of Sun's customers wishing to stay with VME solutions.

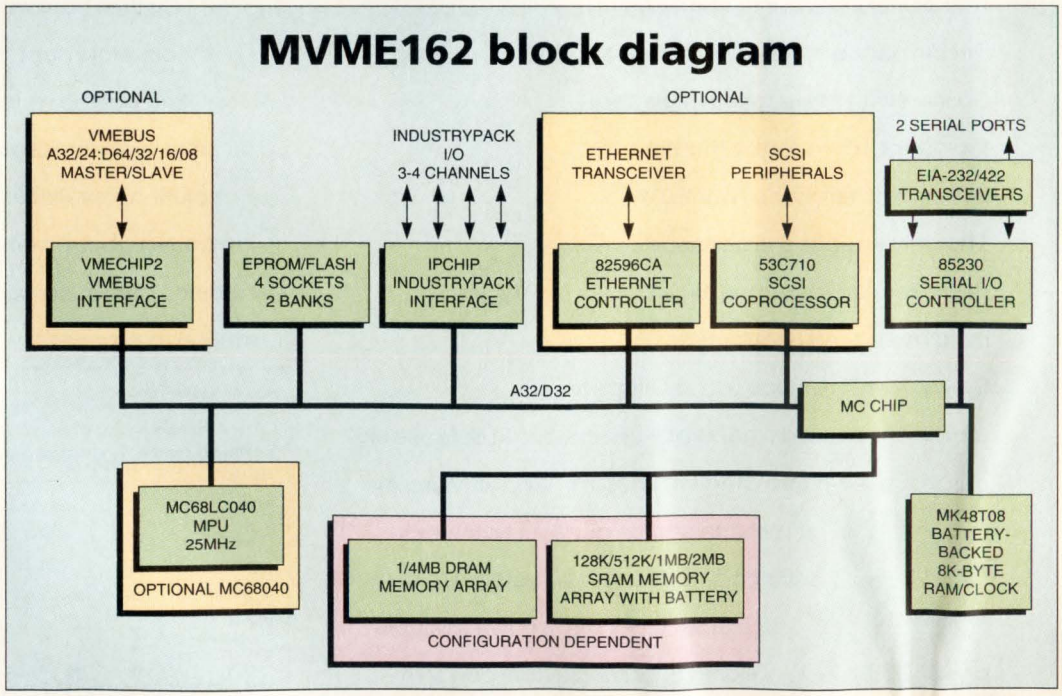
The most recent company to offer what is essentially a 'busless' solution is Motorola (Tempe, AZ), which will offer both a VMEbus and a busless version of its latest SBC, the MVME162. But Motorola's approach varies significantly from that of both Sun and Force.

First, of course, it's based on the Motorola processor, not on Sparc. But other differences are equally significant. "The MVME162," says Jerry Gipper, Motorola's director of VME components marketing, "is targeted at a specific group of users, both in the VME and stand-alone versions. It's designed to be flexible and easily configured to adapt to a wide variety of applications in the industrial control and automatic test equipment areas."

The MVME162 is also quite different from any of the company's earlier single-board efforts. For example, it offers no Unix support, being designed exclusively for real-time applications. And it offers a large number of different memory configurations, as well as Ethernet, SCSI and floating-point support. (The basic board is fitted with a Motorola MC68LC040 processor, a 68040 with the floating-point unit stripped off and low-power memory buffers added.)

First with IPs

But the most important difference between the MVME162 and any other Motorola offering—and any other mainstream 6U VME board, for that matter—is the inclusion of sockets for three or four IndustryPack modules for including special functionality. IndustryPacks, devel-



Motorola has broken with tradition and may be setting a major trend with its MVME162 single-board computer, which is offered with or without a VME interface, and with three or four IndustryPack sockets for I/O modules. This board is designed to sell with a 25-MHz Motorola 68LC040 (68040 without FPU) for under $1,000 in OEM quantities.

"Why can't I get a full Mil-Spec, conduction-cooled VME board with advanced commercial functionality?"

"You can! From Radstone."

Leave it to Radstone to combine the enormous processing power of the 68040 microprocessor with full Mil-Spec reliability on a single VME board. With the CPU-40, Radstone brings the high performance, functionality and flexibility previously available only in advanced commercial VME processor boards to high-rel NDI Mil-Spec applications.

Powerful, Flexible, Expandable

This high speed, single-board computer has features like a 25 MHz 68040 microprocessor, SCSI and Ethernet ports, up to 8 Mbytes of dual-ported RAM, up to 4 Mbytes of 32-bit wide Flash EPROM and much more. It also boasts the first Military Expansion Bus for other functions like MIL-STD-1553B, serial/parallel I/O, VSB or customer-specific functions.

And that's not all. The CPU-40 is available in conduction- and air-cooled full Mil-Spec or ruggedized models, and software development models. All five models are 100% software compatible to meet all your applications precisely.

Ultimate Boards/Total Systems

And there's even more in the Radstone arsenal. Full Mil-Spec, ruggedized and development boards for graphics, intelligent I/O, memory...plus ATR chassis, rugged enclosures and software support. A total embedded systems capability.

When you need the high performance and functionality of commercial boards...with full military reliability...at an off-the-shelf price...call Radstone. We invented Mil-Spec VME ...and we're continually perfecting it.

Radstone Technology Corporation
20 Craig Road, Montvale, NJ 07645-1737
Call Toll-Free: (800) 368-2738
Eastern Region: (201) 391-2700
Central Region: (708) 304-0202
Western Region: (408) 727-4795

RADSTONE TECHNOLOGY

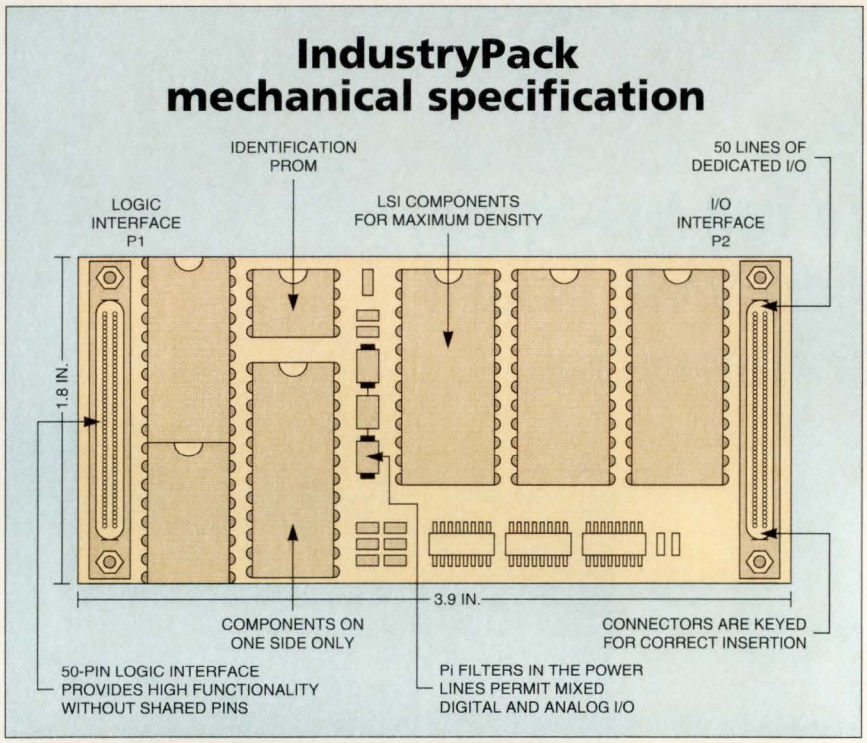
CIRCLE NO. 30

oped by GreenSpring Computers (Menlo Park, CA), are compact add-on mezzanine modules measuring only 1.8×3.9 in. for a single unit, and 3.6 × 3.9 in. for a double. GreenSpring developed the IndustryPack to be the ideal mezzanine for both 3U and 6U VME, and has released the specification to the public domain. Currently, more than a dozen companies support the pseudostandard, offering more than 25 different option modules.

Motorola has traditionally been timid about offering a mezzanine or daughterboard, and at one time even suggested that such an approach was unreliable. But over the past two years the company's changed its mind, offering memory expansion in the form of its 147 and 167 proprietary memory expansion cards. The inclusion of IndustryPacks, however, marks Motorola's first use of a NIH (Not Invented Here) expansion module.

"We selected the IndustryPack module instead of SBus or any of the more than 21 available VME mezzanine buses," says Gipper, "because it's an open standard, is bus-independent, has multivendor support, offers a double-size option, and modules available fit closely with the target application area of industrial automation." Gipper also points out some of the other features of IndustryPacks, including two clock speeds, all logic pins fully defined, CMOS interface levels for low power, 50 or 100 I/O lines per module, good interconnection with the carrier board, module identification PROM, and amenability to high-density surface-mount designs.

"The IndustryPack concept," says GreenSpring's executive vice-president, X. Kim Rubin, "was created to mate with the VME form factor, either 3U or 6U, to provide an efficient I/O flexibility not available with other technologies. Compared, for example, with SBus, IndustryPacks are very low-cost and provide just what's needed for industrial control applications."



Motorola has either three or four sites for IndustryPack modules to be included on its MVME162 single-board computer. IndustryPacks are compact boards (1.8 × 3.9 in.) with two 50-pin connectors, identification PROM and on-board Pi filters.

One up

Apart from providing a very flexible platform, 27.8-Mips performance with a 25-MHz 68040 or 68LC040, versions with and without VMEbus interface, and a variety of IndustryPack options, Motorola's coup de grace is price. According to Gipper, the board in a standard VME configuration is expected to sell for "well under $1,000 in OEM quantities." This makes it one of, if not the, lowest-priced, full-featured SBCs on the market.

Gipper claims that the combination of Motorola's manufacturing technology for its six-sigma quality line with the anticipated sales volume of the new board makes the low price possible. In comparison, Motorola's previous price leaders, its MVME147 and MVME167 products, have been at close to twice the MVME162's price. (There have been periodic reports, however, that prices have been substantially lowered on these parts to meet the demands of very large customers.)

Motorola's use of IndustryPacks marks the first time any of the top ten VME board makers have adopted a standard mezzanine bus. The exception has been Force, which has included SBus slots on its SBCs as part of its arrangement with Sun. Motorola's adoption of GreenSpring's IndustryPacks, however, is not part of any major technology-swapping arrangement, though Motorola will be reselling GreenSpring's modules.

More important, Motorola's move may mark the beginning of a shift for VMEbus-based systems. Traditionally, users of VME in industrial control applications have relied on multiple VME boards to implement a complete system. This necessarily included a backplane, as well as the software to make sure everything ran smoothly across the VMEbus—something of a problem in the past. Now, with the shrinkage of semiconductor geometries and the broad availability of ASICs, it's possible to condense the functionality of several boards onto a single one.

Users are anxious to take advantage of the resultant smaller space, lower cost and higher reliability inherent in such single-board, busless approaches. But developing suitable products has turned out to be more of a job than simply reconfiguring a standard board. In Sun's case, its approach was to deliver a full board-based Unix platform with the versa-

We wrote the books on real-time.

When it comes to real-time system software, Microware Systems Corporation leads the way. Now, we offer two books that provide you with complete real-time solutions — the OS-9 and *OS-9000 Catalogs*.

Microware offers the broadest range of real-time solutions in the industry. Data sheets and flyers just weren't enough to tell our story, so we wrote these books to tell you about our real-time operating systems. These catalogs are chock-full of more than 330 pages of useful information about our operating systems including networking, graphics, language compilers and productivity tools.

OS-9 is the world's leading real-time operating system for 680X0-based systems. OS-9 has been designed into thousands of embedded applications from industrial automation to consumer electronics.

OS-9000 is a portable real-time operating system written in C for advanced CISC and RISC processors. The ability to port OS-9000 to various hardware platforms "future-proofs" your real-time software investment through the 1990s.

Put the world's real-time leader to work for you today.

For Your Free Catalogs, Call

1-800-475-9000

In California, call (408) 980-0201

microware®

MICROWARE SYSTEMS CORPORATION

1900 N.W. 114th Street • Des Moines, Iowa 50322
Phone: (515) 224-1929 • Fax: (515) 224-1352

MORE CHOICES • MORE OPTIONS • TOTAL SUPPORT

CIRCLE NO. 31

tility of SBus modules. Motorola, on the other hand, is vying for a big chunk of the industrial control business by offering a variety of modular I/O approaches and flexibility, as well as a standard-bus option.

While Motorola is the first major VME maker to offer both a bused and busless version of its SBC, GreenSpring itself offers a single-board busless board utilizing Motorola's 68332 communications processor along with a number of IndustryPack sites. The board GreenSpring has dubbed the Platform 332 supports six IndustryPacks and, according to GreenSpring president Henry Lehmann, "offers VME performance and software compatibility without a backplane."

New technologies advanced

Bringing out a busless 680X0 board may not be a big shot in the arm for the VME industry, but it may well forward two technologies. First, PC platforms have enjoyed a relatively uncrowded field for small, embedded SBCs. Users with applications that called for more than a PC, yet who couldn't afford the space and cost of a backplane-based system, often elected proprietary approaches. Now they have an alternative.

Second, Motorola's move may well put IndustryPack on the map as a viable technology. Though IndustryPacks have been around for quite some time, their use hasn't exactly grown explosively. Motorola's approach has created an opportunity which may well attract followers. The approach provides a sensible alternative for relatively low-performance I/O without the need to go to a full VMEbus board, or to provide a custom solution.

It will probably be some time before the jury is in on the new Motorola offering—samples of the board won't be available for another month or so. But development alternatives are already available in terms of a standard MVME167 combined with a GreenSpring IndustryPack carrier board. In addition, IndustryPacks have apparently been used in a number of systems utilizing proprietary boards in the recently completed European Disney entertainment complex. And IndustryPacks are used by GreenSpring as well as some 20 other companies in a wide variety of applications. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Force Computers (408) 370-6300	Circle 204
GreenSpring Computers (415) 327-1200	Circle 205
Motorola (800) 234-4VME	Circle 206
Sun Microsystems (415) 336-3000	Circle 207

Pick up the number one real-time operating system.

And run with it.

In today's competitive market, it's important to run with the best. And when it comes to real time, the iRMX® operating system is the clear favorite.

You see, iRMX has a 13-year track record for proven reliability. In fact, only DOS runs on more X86 systems. Now, iRMX for Windows provides the first real-time operating system with guaranteed response time that runs DOS and standard-mode Windows on the i386™ and i486™ architecture. That's right, true real time on a PC.†

iRMX for Windows brings more than just affordable hardware to real time. It also gives you a head start on development with access to the huge installed base of DOS applications and tools. In fact, you even have the option to run Windows†† (including Windows 3.1).

So take the first step, call (800) GET-iRMX (800-438-4769)* and ask for Lit. Pack. #2B. And start running real time with your favorite DOS and Windows software.

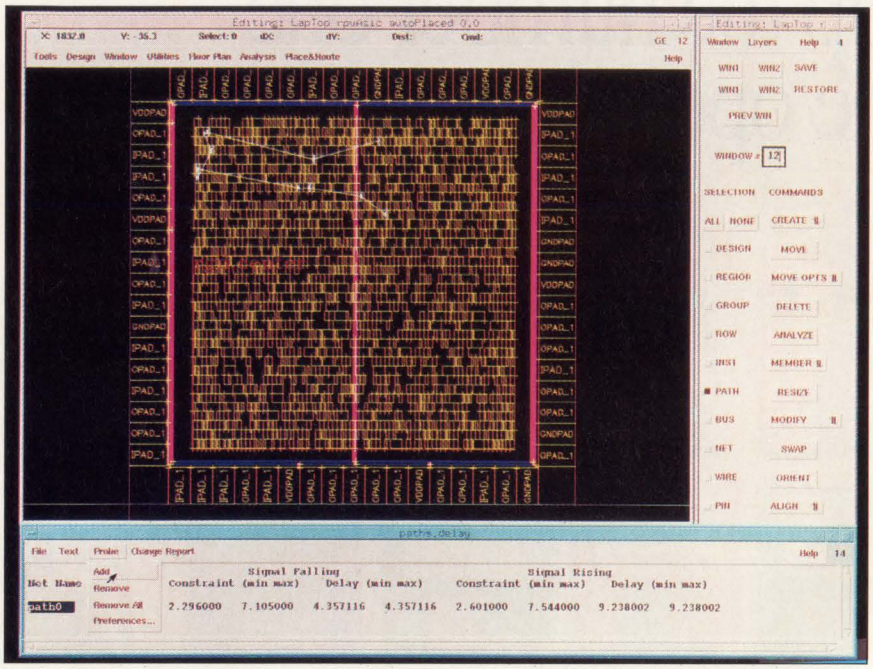
intel®

*Outside the U.S.A and Canada, FAX (503) 696-4633. © 1992 Intel Corporation. iRMX is a registered trademark and i386 and i486 are trademarks of Intel Corporation.
†iRMX runs on IBM and Compaq compatible i386 and i486 based PCs. ††All other products shown or mentioned are trademarks or registered trademarks of their respective owners.

CAE/CAD TOOLS

EDA vendors unveil tools for rules-driven layout

Mike Donlin, Senior Editor



In this photo of Cadence's Preview floorplanner, a critical path is displayed graphically and highlighted for analysis. In the lower part of the screen, a table compares the highlighted path's estimated delay versus the user-specified timing constraint.

Many IC companies are lining up behind the doctrine of concurrent engineering and embracing the end of the "over the wall" methodologies of the past. Traditionally, design engineers created and simulated the logical portion of an IC or ASIC and then passed the resulting netlist information to the layout specialist for component placement and routing. This method removed the design engineer from the physical implementation of his or her ideas, and often resulted in costly iterations

Bridging the gap

Bridging the gap between the two camps is difficult, however, because many designers don't want to get involved with the drudgery of physical layout, and layout specialists don't often cross over into the hallowed halls of the design engineer. EDA vendors are responding to this dilemma with tools that tie vital design information to the physical design of the silicon, in effect making rules-driven layout a reality.

"Some of the most essential data is in the critical timing paths," says Isadore Katz, vice-president of marketing for the IC design division at Cadence Design Systems (San Jose, CA). "Growing chip complexity and submicron geometries are making timing constraints tighter than ever, and it's important that they're dealt with early in the design phase. In yesterday's standard designs, for example, a typical 5-ns clock skew budget translated to about 1.5 m of wire. Today's budget is more on the order of 100 ps, which comes out to about 3 cm of wire. Obviously there's no room for error in the place-and-route domain."

To help designers and layout specialists meet these tight timing constraints, Cadence has recently released Preview, a foundry-independent automatic floorplanning and analysis environment for IC design. According to Cadence, Preview links logical and physical design by bringing floorplanning and analysis information to an early stage in the design cycle, which will give designers confidence that their designs will meet size and performance goals on the first pass through physical place-and-route. "Floorplanning is important because it gives the designer critical timing information, such as interconnect delay, while the design is in the flexible concept phase," says Donna Rigali, senior product manager at Cadence. "Floorplanning isn't the same as actual placement, because it's tied to the logic design portion of a product's development. It's high-level partitioning information as opposed to final cell or gate placement."

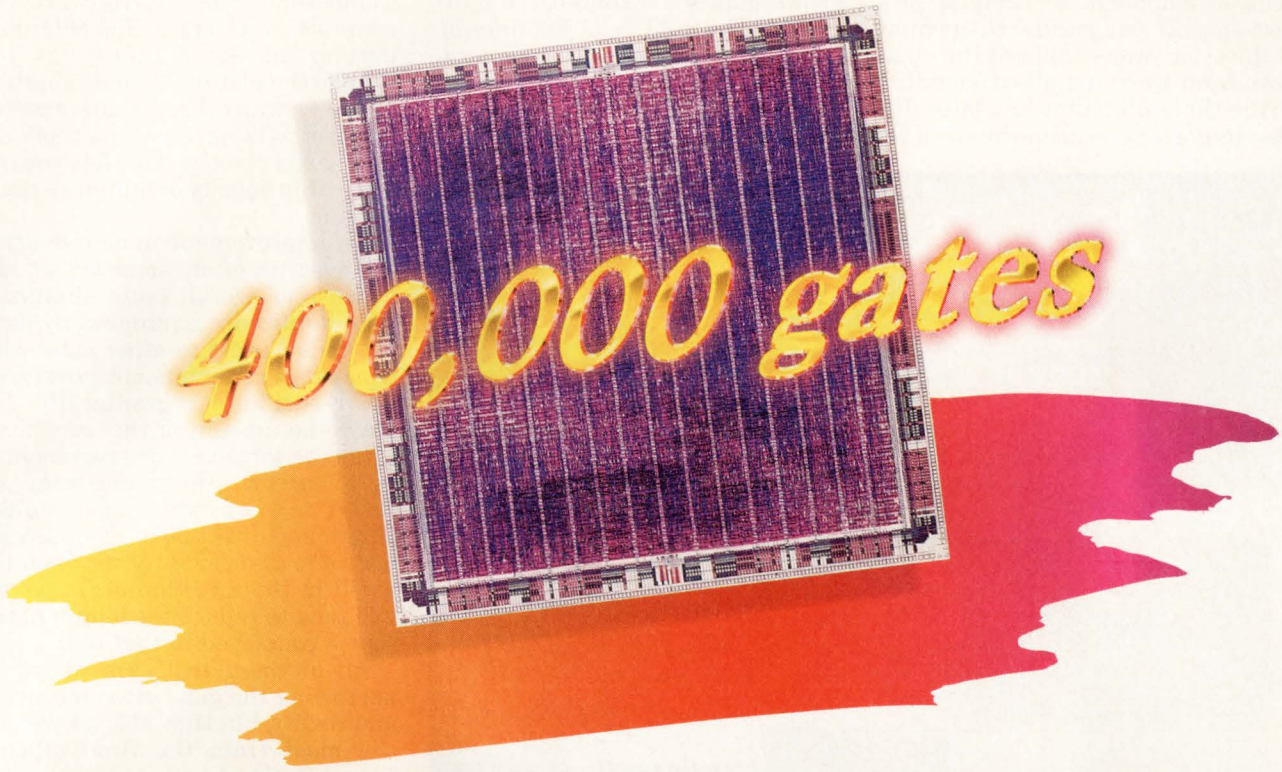
Preview contains tools for prediction of timing, size, congestion, and routability. Given a set of design constraints, the tool analyzes alternatives and creates a floorplan which the designer can optimize for performance.

"These types of tools are necessary for our leading-edge customers who are megahertz driven," says Fuad Musa, director of strategic CAD programs at the ASIC division of the Motorola Semiconductor Products Sector (Phoenix, AZ). "From a silicon point of view, things like parasitic and wire delays are becoming a bigger factor in terms of the percent of the total delay. The more that you know about these effects when you're conceptualizing a device, the more intelligence you'll build into your designs. This leads to better optimization of the design and more performance from the silicon. It also gives you more confidence that the device will work and keeps you from being too conservative with the resources that the technology offers."

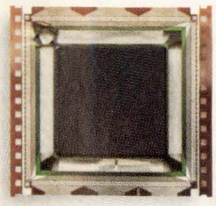
Winning designer confidence

If there's a flaw in all this, it's the assumption that designers will trust automatic design tools enough to actually use them. EDA vendors have to win converts to the concept that software can be a reliable guide for an experienced designer who may be directed by the tool to alter a design. "We believe that chip complexity will force the issue," says Bruce Yanagida, manager of software architecture and manufacturing operations at Cascade Design Auto-

Think Performance.



Think Mitsubishi Gate Arrays.



Before you design your next gate array, or even your first, you've got to think about performance. Your very next thought ought to be: **Mitsubishi Gate Arrays.**

Mitsubishi's triple-layer metal, 0.8µm gate arrays offer 400,000 gates with over 60% utilization, and a typical loaded delay as fast as 215 picoseconds. We also give you up to 512 I/Os and pin counts as high as 576 in our exclusive µ Pitch TAB™ packaging.

We also offer design kits for the industry's most popular workstations, from logic synthesis, to simulation, to automatic test pattern generation (ATPG). So you can design on your own workstation or ours.

VISION® ACTION REALITY

Mitsubishi offers both local design support and the global resources of a stable, well-capitalized company. As one of the world's top 10 semiconductor suppliers, we've been in the ASIC business over 15 years and we're continuing to invest in technologies for the next decade.

When you think gate arrays, think performance. Then think Mitsubishi. You'll be glad you did.

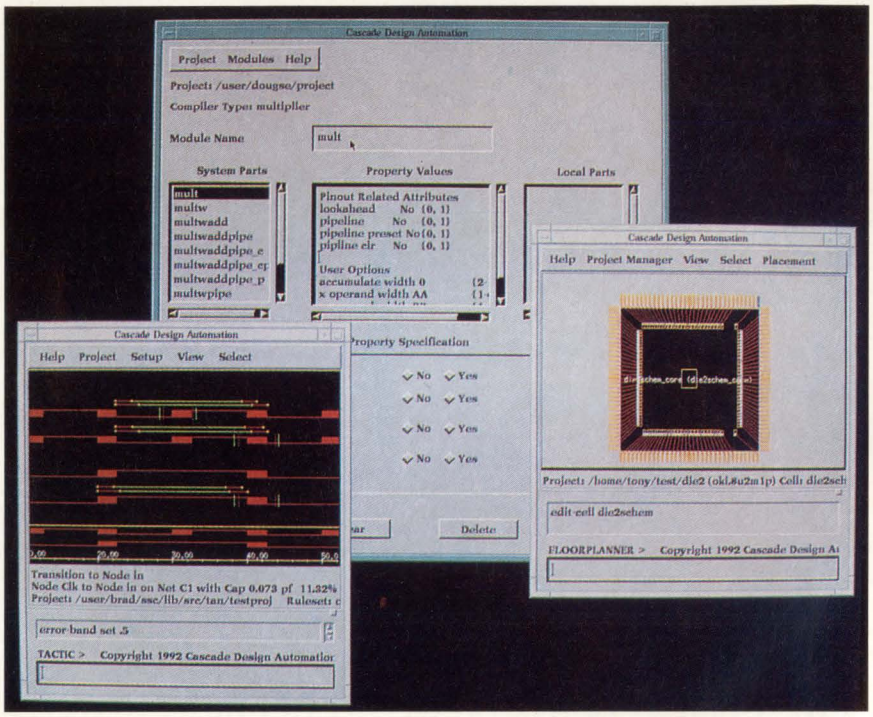
Phone (408) 730-5900 ext. 2106

MITSUBISHI
ELECTRONIC DEVICE GROUP

CIRCLE NO. 34

CAE/CAD TOOLS

mation (Bellevue, WA). "It's next to impossible for a designer to keep track of all the rules during a product's development. By bringing process-specific design rules to the front of the cycle, we've relieved the engineer from worrying about violating a rule that will haunt him later. It's also important to keep the tools interactive, so that a designer can go in and tweak the automatic tool's results for best performance."



Shown here is the package view of a chip (right window) that was generated by Cascade Design Automation's Epoch software. The packaging software lets you modify packaging selection, bonding rules, pinout, and placement. The Timing Analyzer (left window) is a static timing analysis tool that reports critical paths and timing violations. The background window shows Epoch's module browser, which lets you select from the parameterized module library by name or by functional specification.

At last month's Design Automation Conference in Anaheim, CA, Cascade unveiled its IC design suite, Epoch. The tools target performance-driven layout and feature a collection of module libraries, including standard cells, memories and datapath elements. An interactive timing analysis capability keeps the designer involved in the project. By incorporating IC-specific information into the tool set, Epoch accepts user constraints and uses timing and load analysis to drive placement, routing, buffer sizing, power and clock distribution, and packaging. Epoch's timing analyzer provides an error reporting scheme which graphically represents timing errors against a display of the active clocks. The tool lets you interactively modify design parameters to perform "what if" analysis on chip performance.

"The timing analysis information is critical to ensuring a design's accuracy," says Barry Roitblat, Cascade's director of marketing. "Particularly with submicron technology, you have to model the chip so that when it comes back as a device you have some degree of confidence that it will behave the way you think it's supposed to. This means accurately modeling the delays of components and interconnects so you can do a distributed analysis of the delays to avoid things like race conditions in the final design."

Keeping designers involved

Interactive floorplanners, like Cadence and Cascade's, are targeted at skeptics who might not trust a fully automated tool and are also aimed at seasoned designers who know more about their processes than could ever be built into software. For example, Cascade's FloorPlanner, part of the Epoch suite, lets you change the placement or orientation of a cell, swap cells, reshape a cell or group of cells, or regroup sets of cells into flexible blocks. This lets you improve chip density or minimize route lengths.

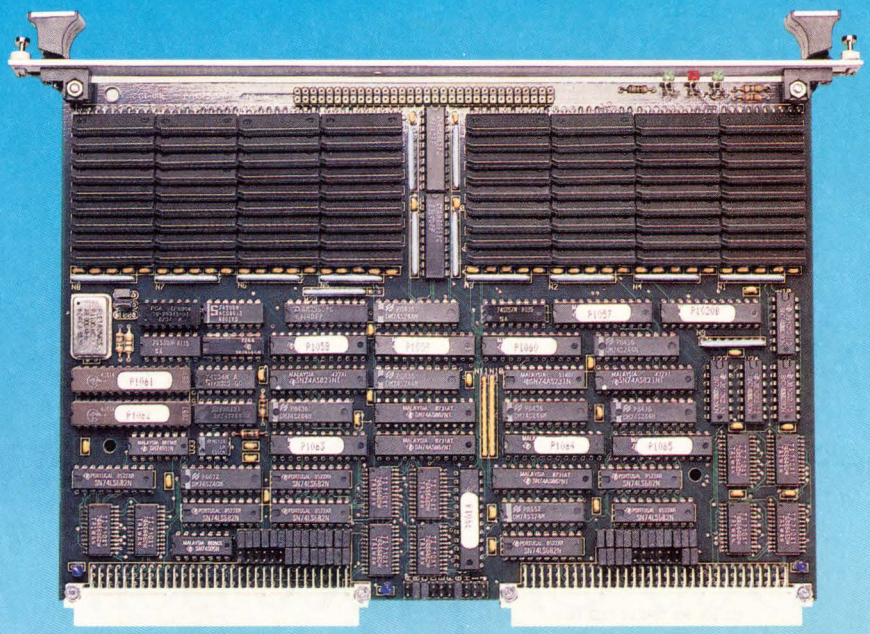
An improvement in chip density, however, is often achieved at the expense of overall route minimization. Routes are minimized by placing cells closest to other cells with which they communicate most heavily. FloorPlanner graphically displays the amount of this communication as force vectors, represented by an arrow originating from the center of a cell, which sums up the length and direction of the nets connected to that cell. Any movement of a cell in the direction of the arrow will tend to reduce the length of the routes connected to that cell.

All of these tools are aimed at narrowing the gap between concept and reality, but they also let you get the most from the final silicon. There's a fine line between squeezing as much performance from a device as possible and being too careful and not designing up to the technology's full potential. "Silicon vendors tell you that they have 40 or 50 or 60 percent utilization of actual gates," says Motorola's Musa. "That's quite a range, and just how much you're going to get from your final design depends on how well the design is thought out. It's not unusual for a customer who's pushing the maximum number of gates in a design to find out that the silicon vendor couldn't place and route it and had to take something out or change the design. No one needs that kind of aggravation. With the right tools, you know your limitations and capabilities early on, so you get what you designed." ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Cadence Design Systems
(408) 943-1234 ..... Circle 208
Cascade Design Automation
(206) 643-0200 ..... Circle 209
Motorola Semiconductor Products Sector
(800) 521-6274 ..... Circle 210

40 MB/SEC DUAL-PORT VME/VSB MEMORY



CI-VME40

The CI-VME40 is the ultimate high-speed, high-capacity DRAM memory board with a dual-port interface to the VME and VSB Busses. The CI-VME40 is optimized for Block Transfer Cycles yielding a bus transfer rate up to forty megabytes per second. Chrislin is the only memory supplier to offer such an advanced and versatile dual-ported VME/VSB memory!

THE CI-VME40 FEATURES:

- 20ns write/20ns read ACCESS TIMES in BLOCK CYCLE
- 90ns write/140ns read ACCESS TIMES in SINGLE CYCLE
- 63ns write/83ns read CYCLE TIMES in BLOCK CYCLE
- 195ns write/195ns read CYCLE TIMES in SINGLE CYCLE
- 4MB, 8MB, 16MB, 32MB, 64MB in one VMEbus/VSB slot
- Byte Parity Error Detection
- Memory start and end addresses selectable on 256KB boundaries
- VMEbus and VSB memory start and end addresses configured independently

ALSO AVAILABLE FOR THE VMEBUS ARE...

THE CI-VMEmory FEATURES:

- Low-cost high-power VME memory with 4, 8, or 16MB
- VME Revision C.1 compatibility
- Lower and upper memory addressses independently selectable in 64K byte increments
- Byte Parity Error Detection with selectable trap on Parity Error
- On-board Control Status Register

THE CI-VSB-EDC FEATURES:

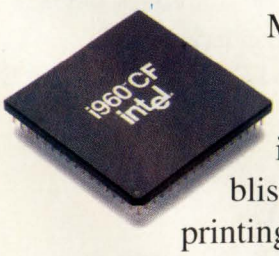
- Low-cost high-power dual-ported VMEbus/VSB EDC (Error Detection and Correction) memory
- 4, 8, 16, 32 or 64MB in one VMEbus/VSB slot
- VME Revision C.1 compatibility, VSB Revision C
- Lower and upper memory addressses independently selectable on 256K byte boundaries
- Single-Bit Error Detect and Correct, Double-Bit Detect

Chrislin Industries, Inc.
31312 Via Colinas, Suite #108, Westlake Village, CA 91362
TEL: (818) 991-2254 FAX: (818) 991-3490

Providing Top Quality Memory for Over 16 years!

CALL TOLL FREE: (800) 468-0736 (PST)

We've just tested the performance of our new i960 CF processor.



Make no mistake. This is no middle-of-the-road processor.

It's our new superscalar i960™ CF chip. And it delivers blistering speed to your high-end printing, imaging, communications and networking applications. Simply put, it outruns every 32-bit embedded processor on the market—and we have over 25 benchmarks to prove it.

You see, only our i960 RISC architecture brings superscalar processing with multiple operations per clock to embedded applications. Our new i960 CF processor is highly integrated with optimized data and instruction caches for throughput up to

twice that of our i960 CA chip. Which makes it the most advanced technology available for embedded applications.

If you're already using our i960 CA processor, you can quickly shift up to higher performance with full code and pin compatibility. And, of course, we offer a comprehensive array of Solutions960 development tools to further speed up your design process.

So step on it. Call 800-548-4725 and ask for literature packet A9A50 for complete benchmarks. And learn what your applications can do with a faster engine.

intel®

CIRCLE NO. 36

XRAY Gets You There on Time

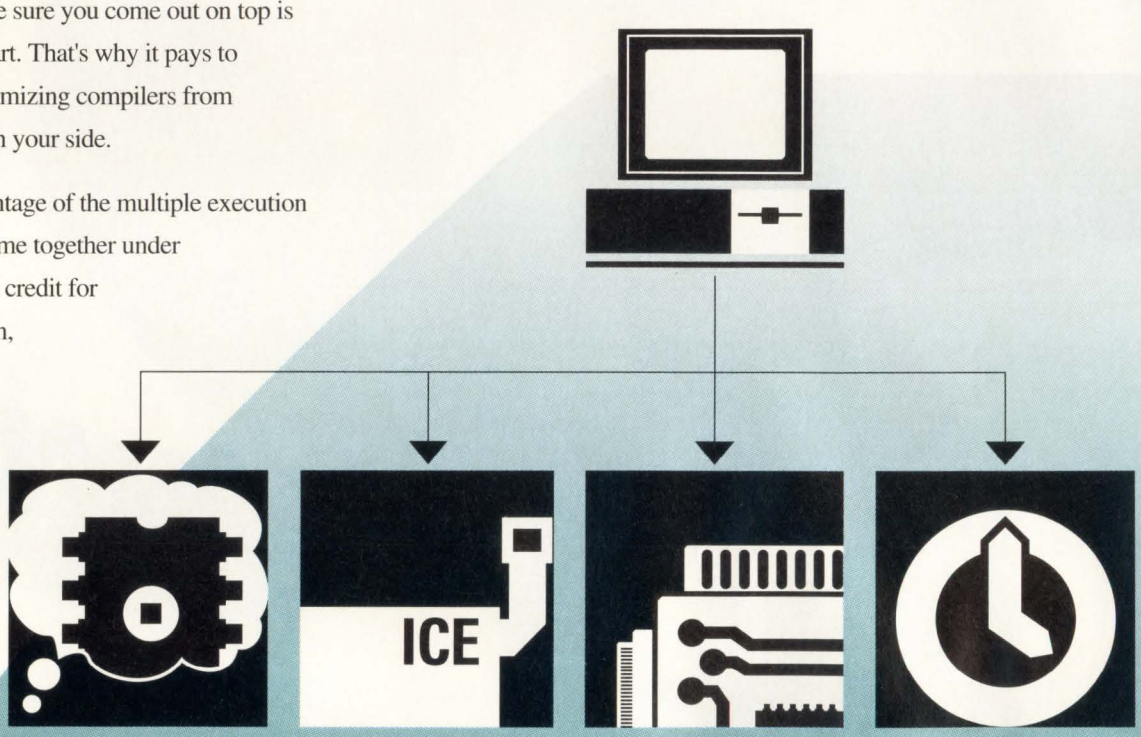
Getting your embedded system to market on time is never easy. There are always surprises during software development and hardware integration. And they expect you to keep it all on track, no matter how many curves they throw at you.

A Solid Head Start

The best way to make sure you come out on top is to get a solid head start. That's why it pays to have XRAY and optimizing compilers from Microtec Research on your side.

When you take advantage of the multiple execution environments that come together under XRAY, you'll get the credit for making things happen, instead of the heat for holding things up.

Here's why . . .



Instruction-Set Simulation

Debug with maximum control and visibility into actual program and data, even before your hardware is running. Features cycle-counting, performance analysis, code coverage, and peripheral simulation.

In-Circuit Emulation

Perform real-time, source-level debugging through emulators from industry-leading instrumentation suppliers.

Target ROM Monitor

Combine Microtec Research's host-based debugger and configurable target monitor for excellent price/performance. The small monitor offers high-speed communications options -- including Ethernet, high-speed serial, and parallel.

Real-Time Embedded OS

Get both source- and system-level debugging from a single tool for seamless development of multi-tasking applications.

No Explanations

With XRAY, you can go where you want to go, instead of being stuck in the lab fixing someone else's problems. And with the head start XRAY gives you, you won't have to explain why you're late. In fact, you won't have to explain anything at all.

Microtec Research

Setting the Standard

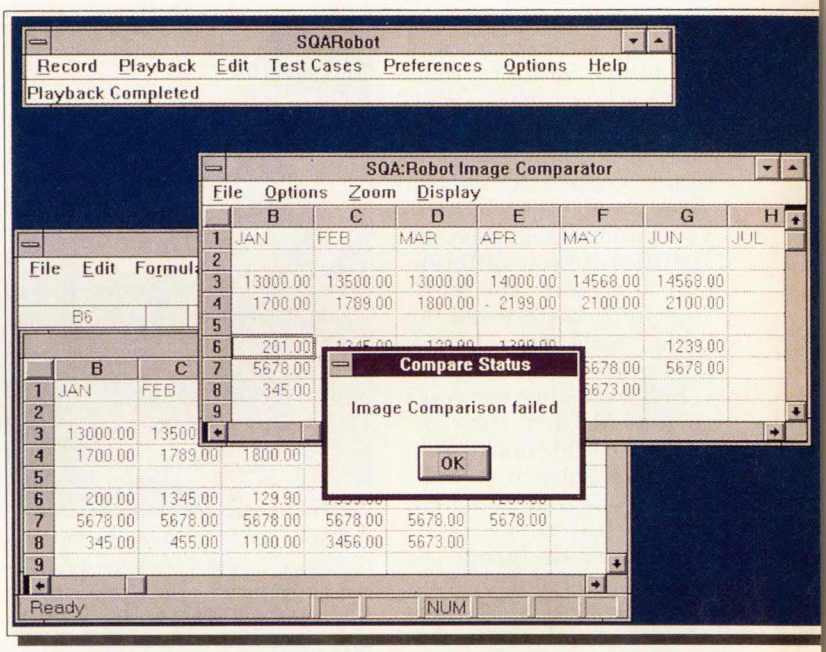
Microtec Research, Inc., 2350 Mission College Blvd., Santa Clara, CA 95054, 408-980-1300 **800-950-5554**
Boston 603-880-4484, Dallas 214-934-6555, London 0256-57-55-1, Los Angeles 714-727-0458, Munich 089-609-6020, Paris 33-1-30-57-19-09, Tokyo 03-5210-3050

CIRCLE NO. 37

Automation improves speed and accuracy of software testing

Testing complex software applications is a tedious task best left to machines. New methods of automating the process promise payoffs in terms of shipping higher-quality products.

Tom Williams
Senior Editor



SQA Robot from Software Quality Automation uses Microsoft's Visual Basic for creating a certain level of test scripts. It's also capable of working with Microsoft's MS-Test tool in the context of a project-management environment called SQA Manager.

There's an old cliché that says if you put enough monkeys in a room with enough typewriters for long enough, they'll produce all the great works of literature. For a long time there's been a similar myth about software testing. But locking a bunch of college students in a room with unlimited pizza and turning them loose on a software product can no longer be considered a credible form of software testing—if it ever was. Today's software products have become so large and so complex, and in many cases so critical to life and safety, that a more systematic and disciplined approach to software testing has become imperative.

But exhaustive software testing entails two elements that discourage human operators and make them prone to mistakes: repetition and tedium. Creative people such as programmers instinctively balk at the idea of long hours exercising every function of an enormous program over and over with the only variety being different input values to be compared with different expected outputs.

Now that an ever-growing number of applications, including a large number of embedded systems, are using window-based user interfaces, the problem is only getting worse. If anything cries out for automation, it's a way to thoroughly test software.

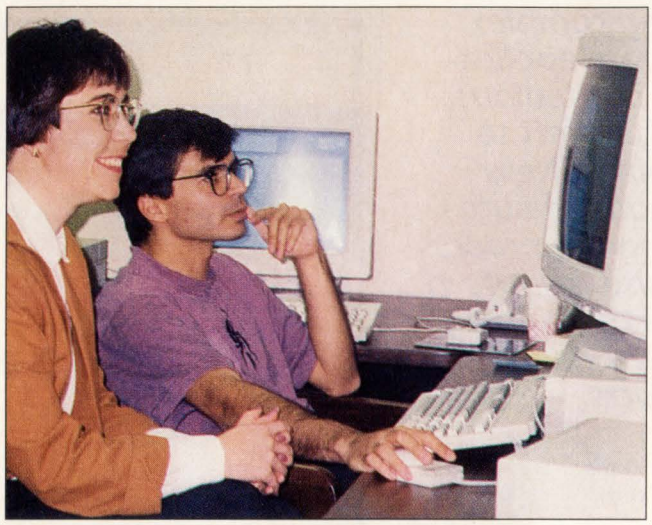
Help is on the way

Fortunately, a number of tools at a range of prices and offering a variety of capabilities are appearing to help developers automate the testing process at the user interface level. Basically, testing at this level entails supplying the system's various functions with inputs and comparing the system's reaction with expected outputs. It also includes deliberate attempts to crash the system so that the code that's finally shipped doesn't fail because of wrong inputs.

For embedded systems, there's also a need to exercise inputs and outputs that aren't addressed by the user interface but that, in the final product, are used by sensors and actuators. Still, even those tools that are limited to testing at the graphical user interface (GUI) level can greatly reduce the amount of testing tedium for embedded systems which require interaction with a user via a GUI.

GUI-oriented testing tools come in two basic flavors: software-only tools that reside on the same CPU with the application under test, and hardware-assisted tools that run on a separate platform and intercept the signals of the application system's keyboard, mouse, video, and other I/O. As you can imagine, there's a significant price differential between the software-only variety and the tools based on separate hardware.

Software-only test tools such as MS-Test from Microsoft (Redmond, WA) and SQA Robot from Software Quality Automation (SQA—Lawrence, MA) have become practical with the advent of window-based GUIs that have a solid application programming interface (API). Both MS-Test and SQA Robot reside in memory on the same machine that's running the application under test. They can achieve a high degree of nonintrusiveness to the application because they interact with it only via the Windows API, the same as a user would.



Tali Aben, director of marketing for Mercury Interactive, says hardware-based testers can test many embedded system functions by interacting with a window-based GUI "which actually drives the embedded software on the other end." In addition, says Aben, Mercury Interactive is working on serial, parallel and device I/O capabilities so the test system can monitor and stimulate I/O lines other than the user interface, such as might connect to sensors and activators. Here she watches her company's TestRunner software perform.

Staying out of the way

The issue of being nonintrusive is a hotly contested one among test tool vendors, with the hardware-based toolmakers claiming totally nonintrusive testing. When it comes to window environments such as Microsoft's or X Windows, David Snow, SQA's vice-president, points out, "Lots of things are supposed to coexist on the desktop. So guess what? If Robot is going to bring down your application, so is your word processor."

Hardware-based testing tools, such as TestRunner from Mercury Interactive (Santa Clara, CA) and Ferret from Tiburon Systems (San Jose, CA), do attempt to keep absolutely isolated, not only from the software application under test but also from the hardware platform and operating system the software's running on and under. Each system consists of a personal computer that runs the test software to control and monitor the system under test, along with a connector box that intercepts the keyboard, mouse and video signals of the target machine. The program running on the tester platform can then input keystrokes and mouse movements directly via the hardware lines of the application platform.

The hardware-based testers can also pull the video signal off the target and compare the screen produced by the application—pixel by pixel, if need be—with the expected resulting screen stored on the test platform's disk. Both TestRunner and Ferret include hardware accelerators for image processing. They can capture full-screen images from the target and quickly compare them with screens stored on their internal disks.

Standing somewhere in between is another GUI-oriented test tool, AutoTester Plus from AutoTester (Dallas, TX). AutoTester Plus comes in both a character-oriented and a Windows version, and can run either target-resident or on a separate platform. Another product from Mercury is a software-only test system called XRunner, which resides on X Windows systems and interacts via the X Windows window manager.

Tool differences

Along with their relatively high price tags, the hardware-based systems do offer some capabilities not available from the software-only tools. For one thing, if a test causes an application to completely hang up the system, the hardware-based tester can do several things. It can be programmed to halt and dial the test engineer at home in the middle of the night, or it can log the failure, reboot the application system, go to a known state, and continue testing. The hardware-based systems can also monitor I/O lines other than those accessed by the user, which is an advantage when testing those parts of an embedded system that aren't directly touched by the user interface. Such a system can even be used to control a simulator—perhaps running on yet another platform—which will send input data to nonuser I/O ports which can be correlated with the testing at the user interface level.

Both Ferret and TestRunner, since they interact with the target only via user interface lines and are independent of the target's operating system or window API, can be applicable to more than one target. TestRunner will work with IBM PCs, Macintoshes, Unix workstations, and others. Ferret has interface adapters for DEC, Sun, Silicon Graphics, X terminals, and many more. The result is that you have to learn only one set of testing tools to be applied to many different target systems.

According to Mercury's director of marketing, Tali Aben, another advantage of a hardware screen image processor/comparator is that it accurately reproduces varying delays in responses that might confuse a system that was simply playing back a script. "I could play back a window normally 99 times and have it pop right up," she says, "but what hap-

NOTICE

WE'VE BEEN ASKED TO MAKE IT VERY CLEAR THAT
THERE'S A WHALE OF A DIFFERENCE BETWEEN QNX® AND UNIX®

WE'RE GLAD TO OBLIGE.

EVEN THOUGH THE QNX REALTIME OPERATING SYSTEM IS *NOT* BASED ON UNIX SOURCE CODE, WE CAN UNDERSTAND HOW SOME DEVELOPERS MIGHT CONFUSE THE TWO. AFTER ALL, QNX FOLLOWS THE LATEST IEEE POSIX 1003.1 AND 1003.2 OPEN SYSTEMS STANDARDS, SO YOU GET THE SAME API AND UTILITY SET FOUND IN MANY UNIX SYSTEMS.

BUT LOOK BENEATH THE SURFACE AND YOU'LL SEE TWO FUNDAMENTALLY DISTINCT ARCHITECTURES. A MONOLITHIC OS ON THE ONE HAND, A MICROKERNEL OS ON THE OTHER. THEY'RE DIFFERENT SPECIES ALTOGETHER, AS DIFFERENT AS A WHALE AND A SCHOOL OF DOLPHINS.

ARCHITECTURE YOU CAN BUILD ON

QNX'S MODULAR, MICROKERNEL ARCHITECTURE GIVES YOU REMARKABLE FLEXIBILITY. OS SERVICES ARE PROVIDED BY A TEAM OF COOPERATING PROCESSES RATHER THAN BY A MASSIVE MONOLITHIC KERNEL. THE RESULT? YOU CAN STRIP QNX DOWN TO A ROM-ABLE EMBEDDED SYSTEM. OR BUILD IT UP TO A VAST NETWORK AND HARNESS THE POWER OF HUNDREDS OF CPUS.

OUR PRICING IS MODULAR TOO, SO YOU'RE NOT FORCED TO PAY FOR WHAT YOU DON'T NEED.

REALTIME PERFORMANCE YOU CAN COUNT ON

NEED THE SPEED OF A FAST, REALTIME EXECUTIVE? QNX CLOCKS IN AT 16 µSEC PER CONTEXT SWITCH ON A 33 MHZ 80486. BUT QNX DOESN'T STOP THERE. WITH ITS PRIORITY-DRIVEN, PREEMPTIVE SCHEDULING, YOU CAN BUILD *REAL* REALTIME SOLUTIONS.

DISTRIBUTED PROCESSING YOU CAN BET ON

QNX CAN TRANSFORM A BUNCH OF ISOLATED MACHINES INTO A SEAMLESS SUPERCOMPUTER, ORCHESTRATING HUNDREDS OF CPUS WITH ITS NETWORK-WIDE IPC. YOU'RE IN COMPLETE CONTROL OF ALL RESOURCES AT ANY POINT, FROM THE PLANT FLOOR RIGHT UP TO YOUR DESKTOP.

SUPPORT YOU CAN DEPEND ON

DURING THE LAST TEN YEARS, WE'VE EARNED A REPUTATION FOR OUTSTANDING TECHNICAL SUPPORT. WE OFFER EVERYTHING FROM 24-HOUR ONLINE CONFERENCING TO ONSITE CONSULTING, SO YOU CAN EASILY REACH THE PEOPLE WHO MAKE UP THE QNX DEVELOPMENT TEAM. THEIR EXPERTISE CAN HELP YOU KEEP YOUR DEVELOPMENT PROJECTS RIGHT ON COURSE.

TO FIND OUT HOW YOUR APPLICATIONS CAN THRIVE IN THE QNX ENVIRONMENT, CALL 1-800-363-9001, (EXT. 103).

QNX®

REALTIME OPERATING SYSTEM

QUANTUM SOFTWARE SYSTEMS LTD.
175 TERRENCE MATTHEWS CRESCENT
KANATA, ONTARIO, CANADA
K2M 1W8
TEL: 613-591-0931
FAX: 613-591-3579

CIRCLE NO. 38

ARCHITECTURE MAKES THE DIFFERENCE

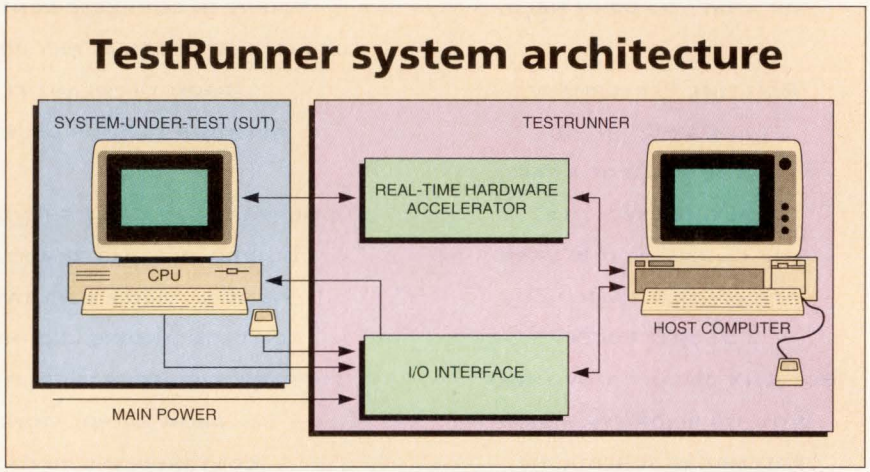
pens if one time the window manager is busy and pops the screen up a second late?" The results might be correct, but a noncritical variation in response time might cause the system to log an error. "That's the problem with record/playback that's merely based on time," she says.

Real testing vs. illusion

According to Gregory Pope, Tiburon's director of validation technology, there are two kinds of testing. "There's testing to prove to your customer that the system looks like it's working. Then there's real testing—testing to find the bugs." So one of the main ideas is to introduce conditions that can cause failures and see how the system reacts. "If a program calls for a value between 1 and 1,000," says Pope, "put in 'ABC' and it shouldn't blow up." It should return an error message or provide some kind of "soft landing" that won't cause a general failure or a possibly catastrophic action. One need only remember the story of the bug in a fighter plane's navigation software that caused the aircraft to flip upside down when it crossed the equator—a bad interpretation of the term "down under."

At the foundation of all GUI-oriented testing tools is the ability to emulate a user by capturing and playing back his or her interaction with the application—recording keystrokes and mouse activity. Whether a testing tool is a software-only tool or running on separate hardware, the capture/playback approach has the immediate ability to let you reconstruct exactly what led up to an unexpected result or failure. It also gives you the ability to save such test scripts and screen comparisons for repeated testing when changes are made to code.

But capture/playback by itself, according to AutoTester's regional vice-president, George Brown, "just creates another nightmare," because test code very quickly gets unmanageably long, and it's hard to have a systematic view of what it's doing. So testing tools have been provided with varying degrees of programmability in addition to their recording ability. For example, programmability lets you capture a series of keystrokes that exercise a feature and then embed those keystrokes in a loop. The exercise of the feature can then be repeated as often as desired while stepping through a series of input values or options, making it possible to extensively test the given feature automatically with a compact coded script. You could also run a series of operations in one mode, then switch to some other mode and replay the same operations many times without having to recapture or rewrite a script.



In the Mercury TestRunner architecture, an I/O interface module lets the test station intercept mouse, keyboard, video, and other I/O, record user activity, and play back test scripts without intruding on the application or the operating system.

First steps to automation

The ability to program test scripts bestows the capability to begin automating the tedious testing process. But test-scripting languages by themselves tend to require a closely detailed knowledge of the code to be tested—more so than is required for creating scripts from straight capture/playback. The advantage is that such language-based scripts can be more systematic and compact. The SQA Robot tool, for example, supports capture/playback as well as the creation of scripts using Microsoft's Visual Basic language. Visual Basic, as the name suggests, relies heavily on interaction with elements of the GUI and lets you build test cases without much detailed knowledge of the underlying code. But these test cases are more systematically programmed than mere capture/playback sessions.

For more detailed scripting, SQA has built-in hooks in SQA Robot to let it work with the MS-Test tool from Microsoft. Microsoft MS-Test includes, in addition to capture/playback capability, two levels of programmability for creating test scripts. FastTest works at about the level of Visual Basic working with SQA Robot. It lets you create test scripts for Windows applications that verify basic functions (such as the existence of an application's menu items), respond to dialog boxes and save and open files. The 'BListBoxExists' function, for example, checks to see that a list box with a specific name exists and logs an error if it doesn't.

At the next level, MS-Test provides a test programming language called TestBasic that provides familiar control structures such as FOR...NEXT loops and SELECT...CASE constructs to do things such as extensively embed captured keystroke sequences in loops to step them through sequences of data. MS-Test also comes with four dynamic link libraries (DLLs), from which it can call a wide range of functions to test applications. Many DLL procedures cover events, such as the ability to send keystroke and mouse movements to an active window. Others check the existence or status of controls such as menu items, check boxes and list boxes. Still others let the tool capture and compare windows.

The higher the level of programming power you select for creating test scenarios, the more efficiency and detail you can expect from your tests. That greater detail, however, requires a closer knowledge of the program code and more preparation before testing begins. In fact, the Microsoft manual admonishes the user that "although it takes time to develop the test software, this time

PC-based tools automate testing of embedded code

Recent advances in PC-based software test automation, coupled with an ever expanding array of PC-compatible boards and devices, have made it possible to automate the testing of embedded software systems by capitalizing on the PC's ability to emulate or communicate over a wide variety of protocols at a reasonably low cost.

Powerful and flexible PC-based memory-resident software-testing technology is now available which can execute coresident with other applications, communications or emulation programs and drive them as directed by a script. Scripting languages support input and output to and from the screen, disk and keyboard, and provide logic to evaluate and respond to results while documenting exceptions.

This combination of software and hardware makes it possible to develop an automated test operator that can test any software executable by, or accessible from, a PC. The result is a fully automated test operator which can be easily and quickly configured for various devices and applications.

Testing fire alarms

Simplex Time Recorder Company (Gardner, MA), a premier vendor of electronic fire alarm systems, offers a sophisticated monitoring and response panel for detecting and responding to fire conditions in buildings. The panel's embedded software constantly monitors and interprets electronic signals from throughout the building, discerns the presence of fire and then performs an amazing series of tasks, including calling the city and fire authorities, describing the location of the building and nature of the emergency, rerouting air flow, and recalling elevators to the ground floor.

The panel itself sports a keyboard and LCD for manual operations. Still, given the possible combinations of conditions which could arise and the number of potential response actions, the testing effort for this system was daunting. Although manual testing could be performed via the panel for portions of the system, the electronic signals which are monitored and the automated responses can't be tested in this way.

To ensure the quality and reliability of the system over the large volume of potential conditions and responses, Simplex developed both customized hardware and software tools which were installed in a PC in combination with off-the-shelf cards. This system was then controlled by a scripting language to create and evaluate the various events.

First, Simplex designed a card which received data from the system and converted it to RS-232 protocol for transmission over a serial communications link to a PC. Running on the PC was a software shell specifically developed to receive, decode and display the data. This enabled the PC to evaluate the responses of the system.

A low-cost digital I/O board in the PC was used to cause the specific stimuli which were needed to create the test events. The board converted TTL output to the electronic signals which would simulate the actual conditions on the system and transmitted them to the panel, letting the same PC cause the events and evaluate the responses.

With this step completed, a test script library was developed to automatically apply and evaluate test cases from the PC. Test conditions were created by parsing and transmitting command sequences entered at the keyboard into the electronic stimulus needed to simulate a particular condition, then reviewing and evaluating the response as it was received over the communications port. According to Simplex's software quality assurance engineer, David Despres, "Our automated test bed has substantially improved our test coverage with less time and fewer resources."

Testing postage scale systems

Many electronic devices depend on human input. Applications ranging from appliance controls to automated tellers use embedded software applications to interact with a human being. In theory, these systems should be manually testable, but in practice, the potential combinations often exceed human endurance and capacity for consistency.

A leading vendor of postage scales and meters faced exactly such a problem. While office personnel across the nation use this equipment everyday without undue difficulty, actually recreating and verifying the complex matrix of rate schedules as applied to varying weights and zones presented a testing problem which outstripped the resources available for manual testing.

The scale system offered a standard RS-232 port through which the embedded software was loaded. This interface also provided a test port which could receive command sequences from a PC front end via an asynchronous communications link. Sequences were translated into events on the meter, such as weighing a package and selecting the class of service. The meter's response, which was the postage calculation, could be returned over the same interface.

The final layer was an automated scripting language which operated the front end, permitting test cases to be applied in an unattended mode. The test cases consisted of both the inputs (package weight, postal zone, class of service) as well as the expected output (the amount of postage due). Discrepancies and test results were automatically logged for later review and analysis.

The result was an automated software-testing system which could be connected to one or one hundred postage meters over standard communications lines, and which was capable of exercising thousands of test cases, 24 hours a day, seven days a week, in a consistent and repeatable manner. Following new loads of the embedded software or changes to the devices themselves, these test cases could be repeated automatically at a marginal cost in time and resources.

Naturally, the equipment itself was still subjected to literal hands-on testing to verify its mechanical integrity and reliability, but the complex underlying calculations in the embedded software system could be easily and accurately verified in an unattended mode.

Linda G. Hayes, president, AutoTester, Dallas, TX

is more than made up during the middle or later stages of testing." According to Microsoft product manager Audrey Watson, "If you're doing what you're supposed to be doing and building the test cases as you develop the product, you're more likely to use TestBasic."

Microsoft advises organizing test scripts into a hierarchical set of scenarios, cases and suites. A scenario tests one instance of a given feature, while a case is a collection of scenarios testing different aspects of that feature. A suite is a grouping of test cases around an application's general function, such as all items in the file menu. If features of the code are changed, you then know which scenarios or cases you need to go in and change as well. But the entire test hierarchy should then be run against the new code to see if the changes introduce any errors elsewhere in the application.

```
**********CLIPTEST.MST**********
********

****This script tests the capability of the Windows
****Calculator to send data to the clipboard
correctly.
****Lines preceded by asterisks are comment lines.
****Commands beginning with an "X" are FastTest
****function names. The "F4" command closes
the
****Calculator window.

'$INCLUDE 'FTEST.INC'

****Set log options and start the Calculator:
XLogOn
XLogBanner "Starting Clipboard Test"
Viewport Clear
XStartApp "C:\WINDOWS\CALC.EXE"."

****Perform a subtraction:
XType "888"
XType "-"
XType "333"
XType "="

****Select the Edit/Copy menu items:
XAlt "e"
XKey "c"

****Verify that the expected result of the
subtraction
****(555) is the same as the value currently held in
the
****Clipboard:
XClipBoardCmp "555"
XAlt "{F4}"
END
```

This sample of a FastTest script from MS-Test exercises the calculator application and compares the result with an expected result stored in the Windows clipboard.

Making test programming easier

Everyone knows that a disciplined method of test development should go hand in hand with a disciplined process of application development. Test requirements should match those derived for the application in the front-end requirements analysis. There should be a link to the CASE tools used by the development team.

But of course, that's seldom the way it works in the real world. The Software Engineering Institute (SEI) of Carnegie-Mellon University (Cambridge, MA) estimates that about 85 percent of today's software development organizations are operating at the 'chaotic' level, which is the lowest of five grades for the methodical and orderly development of software.

It's not surprising, then, that people want ways to make the creation of test scripts easier for existing code—and for working in an organization where all the disciplines of a CASE environment aren't in place. The Mercury TestRunner system, for example, does more than just capture user input while recording. It records user activity directly into a C-like language. That makes it much easier to figure out what's going on than is the case when dealing with a raw recording of keystrokes and mouse coordinates, and it facilitates adding automation elements such as loops and data tables.

Multimedia capability

In the Tiburon Ferret system, in addition to tools that aid in test script programming, bug report generation and deriving tests from requirements, there has been added a multimedia capability. "Despite the fact that we've put these tools in, if no one writes requirements down, who's going to do it?" asks Tiburon's Pope. For existing code or code created without systematic written documentation, Ferret offers the ability to interview the inventor on videotape and play back the interview in a window. According to Pope, "I can go find the guru who invented something and say, 'Can you tell me how this works?' and he probably will. If I say, 'Write it down,' he'll probably say, 'I'm busy.' "

Ferret also includes a handheld scanner for inputting handwritten notes, such as the results of a conversation over drinks that only exist on a cocktail napkin. Tiburon is now working on a Hypercard-like method of indexing such stored multimedia information to relevant parts of the project. "When you want to design a test, call up the interview and find out what the thing is supposed to do," says Pope.

Automating test generation for existing code is also a big part of what AutoTester does. In its character-based version, AutoTester can automatically analyze a program's screens and create templates. In addition, the test engineer can write scripts that don't contain the actual data used in exercising the code. The test data, inputs and expected results can then be kept in separate files. In testing, the input data elements are applied to a given script or screen template and the output of that screen is compared with the expected results.

According to AutoTester's Brown, automating template generation and keeping test data in separate files has several advantages. For one thing, it makes test suites easier to maintain. When a function changes, you generally know which screen is affected and can go in and change that template. "Just as you wouldn't hard-code data for your programs, we don't hard-code data for our test cases," Brown says. This lets the test engineer spend more time on creating test data that will really exercise the system and, since

68000 Developers Do It FreeForm!

FreeForm sets you free! FreeForm is the *first* remote debugger that gives you the freedom to incorporate *all* the resources and tools of your host machine *directly into your target debugging environment!*

FreeForm does it right! Now you can view source with your favorite editor, redirect debugging output into a file, pipe the output to another program, or incorporate your programs *right into FreeForm.* You never have to *exit or escape* from FreeForm in order to compile, link, and re-download your code.

FreeForm does it real time! Your application runs in real time because FreeForm is a nonintrusive, monitor-based debugger. And it's not necessary to turn off the code optimizer, because FreeForm debugs fully optimized, production quality C code.

There's only one thing better than FreeForm-- and that's FreeForm and CrossCode C together! CrossCode C is an advanced optimizing ANSI C compiler package used in over 1,000 applications. It's so good that three out of four clients are referrals from other satisfied users.

FreeForm gives you power! Together with your host (UNIX or MS-DOS) and your target, FreeForm and CrossCode C give you the industry's most powerful 68000-series development system!

FreeForm does it all! It lets you debug all ROMable 68000-series applications, whether you're designing around the 68000, the 68300 family, the 68040, or the new 68ECXXX.

Do it FreeForm Today! Call us at: 1-800-448-7733, EXT. 520 to receive your **FreeForm Demo Kit** for a 30 day free trial.
Do it FreeForm just once--and you'll never go back!

SOFTWARE DEVELOPMENT SYSTEMS, INC.
4248 Belle Aire Lane
Downers Grove, IL 60515 USA
Phone: 1-708-971-8170
FAX: 1-708-971-8513

The Most Responsive Software Company

tests are generated from the program's own screens, less time on defining the templates and scenarios themselves.

Careful planning still needed

For all automated aids, however, the admonition to plan carefully and design systematically is still a wise one. As one user, Keith Davis, director of QA applications at Borland International (Scotts Valley, CA), puts it, "Automation is a separate component to the test process, and you need to really plan for it. You have to really think about what the process is and how it fits into your system." One of the payoffs of automatic testing, says Davis, is that you can run tests unattended and get feedback on the product while devoting creative human resources to things other than running manual tests.

As a vendor of one of the more expensive test systems, Tiburon's Pope comments about the cost of testing: "There are three costs associated with buying a test tool. The initial investment is the most obvious cost. The second is what it takes to set it up, learn to use it and use it the first time. The third cost is how much it costs to use the tool every other time you use it. You can buy a $400 tool that costs you $100,000 to use for a year."

Against the costs, you've got to weigh the benefits of shipping quality software. "You can't put a price on it," says Borland's Davis, "even if it cost $250,000 to do the installation. If we ship a product with bugs in it, we become an acquired company."

Tiburon's Pope points out that SEI estimates the costs of bugs that get out into the field to be between $4,000 and $16,000 per bug when you figure 800-line support, finding and fixing the bug, changing the documentation, and shipping repair disks—not to mention such intangibles as customer goodwill and the credibility of the company. "If you believe that," he says, "as soon as you find three or four bugs you've paid for the system."

Test scripts aren't enough

To be effective, software testing has to fit into the larger context of a software engineering operation. "You need more than a test-execution tool to get this job done," says SQA's Snow, "or all that will happen is you'll be doing the same things faster but no better." SQA Robot is designed to work within an environment provided by another SQA tool, SQA Manager. SQA Manager includes a database and project-management utilities so that various people working on a project can look at the data involved in specifying requirements, designing and executing tests and comparing the results of tests with the original requirements. It's also able to accommodate MS-Test through the hooks built into SQA Robot.

"You need more than a test-execution tool to get this job done, or all that will happen is you'll be doing the same things faster but no better."

—David Snow
Software Quality Automation

For those more sophisticated developers using CASE tools, Snow notes that the use of dataflow diagrams allows a better functional understanding of the code to be tested. Still, "it's possible to check function points and still leave a very large part of the code untested," Snow says. So other tools such as profilers and coverage-analysis tools are needed to provide a level of confidence that the tests that have been designed really exercise a known portion of the code.

"The industry average is that most code goes out with at best 50 percent coverage," says Richard Conley, vice-president of software management products for Veritas (Santa Clara, CA), which makes code-coverage analysis and simulation tools for the Unix environment. "We once found 90 test cases that seemed to be really doing something turned out to be hitting only one particular branch and [provided] only 10 percent coverage," says Conley. "So the organization thought it was doing something but had no good insight into how much of the code was being exercised."

Veritas' VistaTest system incorporates the ability to analyze code and predict how much effort will be involved in testing it; it also performs coverage analysis. VistaTest can then flag portions of the code that haven't been touched by the current suite of tests, so that the test engineer can use that information as feedback to design tests for more complete coverage. "But," warns Conley, "just having 90 percent coverage doesn't mean that the code is 90 percent perfect."

Not all code, such as calls to the operating system, is easily accessible from the user interface—in the sense that a user can say, "If I click this menu item, I will cause that OS call." The VistaSim simulator is able to go in and place error conditions into less accessible places, such as the interfaces between application OS calls and the kernel, so the tester can examine how the code reacts. VistaSim also uses random error seeding as a gauge of the thoroughness of testing.

In random error seeding, the simulator seeds the code with known errors and keeps track of their locations. The test engineer can then run his test suite and determine how many of the seeded errors are detected. This can in turn serve as a gauge for how effective the overall test suite is. Even if the developer decides that it's not cost effective to test 100 percent of his code, he or she needs tools that can give a confidence level.

Confidence in the quality of testing comes from three things: the fact that you're not turning up bugs; your knowledge of how much of the code you've covered; and the ability to predict how many bugs might be left, derived from error-seeding analysis. It would be ideal to know that you've covered every part of the code and found every bug. Lacking that, it's at least helpful to know where you haven't been. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

AutoTester, Inc
(214) 706-3312 ..... **Circle 211**
Mercury Interactive
(408) 987-0100 ..... **Circle 212**
Microsoft
(206) 936-7021 ..... **Circle 213**
Software Quality Automation (SQA)
(508) 689-0182 ..... **Circle 214**
Tiburon Systems
(408) 371-9400 ..... **Circle 215**
Veritas
(408) 626-1222 ..... **Circle 216**

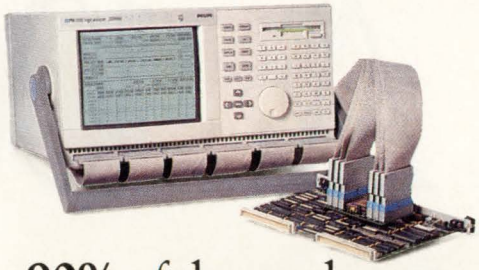
FLUKE AND PHILIPS – THE GLOBAL ALLIANCE IN TEST & MEASUREMENT

FLUKE®

PHILIPS

PHILIPS

Test results:



90% of those who try a Philips Logic Analyzer from Fluke buy one.

100% get a free DMM*.

Our logic analyzers sell themselves. All we have to do is get one in your hands. To make sure you do, we're giving you a Fluke DMM*, whether you buy our analyzer or the competition's. (See attached card for complete details).

Only the Philips PM 3580 family of logic analyzers give you *true* dual state and timing on up to 96 channels - simultaneously. All accessible with one probe and one keystroke. Which means no more dual probing or reconfiguration between state and timing. Or no probes at all if you use our boundary-scan test option!

*The top-of-the-line Fluke 12 in our newest DMM family. It combines a smart set of troubleshooting features in a new design that's exceptionally fast and simple to operate — with one hand. It's yours after our 30 minute demo, no matter whose logic analyzer you purchase.

All our analyzers feature 50 MHz state and up to 200 MHz timing speeds. As well as integrated state and timing triggering for fast debug of complex hardware and software problems. Plus broad µp support like Intel®'s i486; i386; 80286; 80186/88 families. The MCS-96, 8051, and i960 families. And the Motorola 68040 to 6800, 68HC11, 68332/1, 68302, 68340, 56001, AMD®'s AM 29030, and TI's 320Cxx family.

The PM 3580 family of logic analyzers is priced from $4495 to $11,450 - about half the cost of comparable analyzers. What's more you can have them up and running in only 30 minutes.

Find out why the PM 3580 family of logic analyzers were the only ones cited for excellence and innovation by *Electronic Design, EDN, Embedded Systems, Electronic Products*, and *R&D* magazines. Take the Fluke Challenge. The odds are 100% you'll be totally impressed.

For literature, our video or a demonstration, call **1-800-44-FLUKE**.

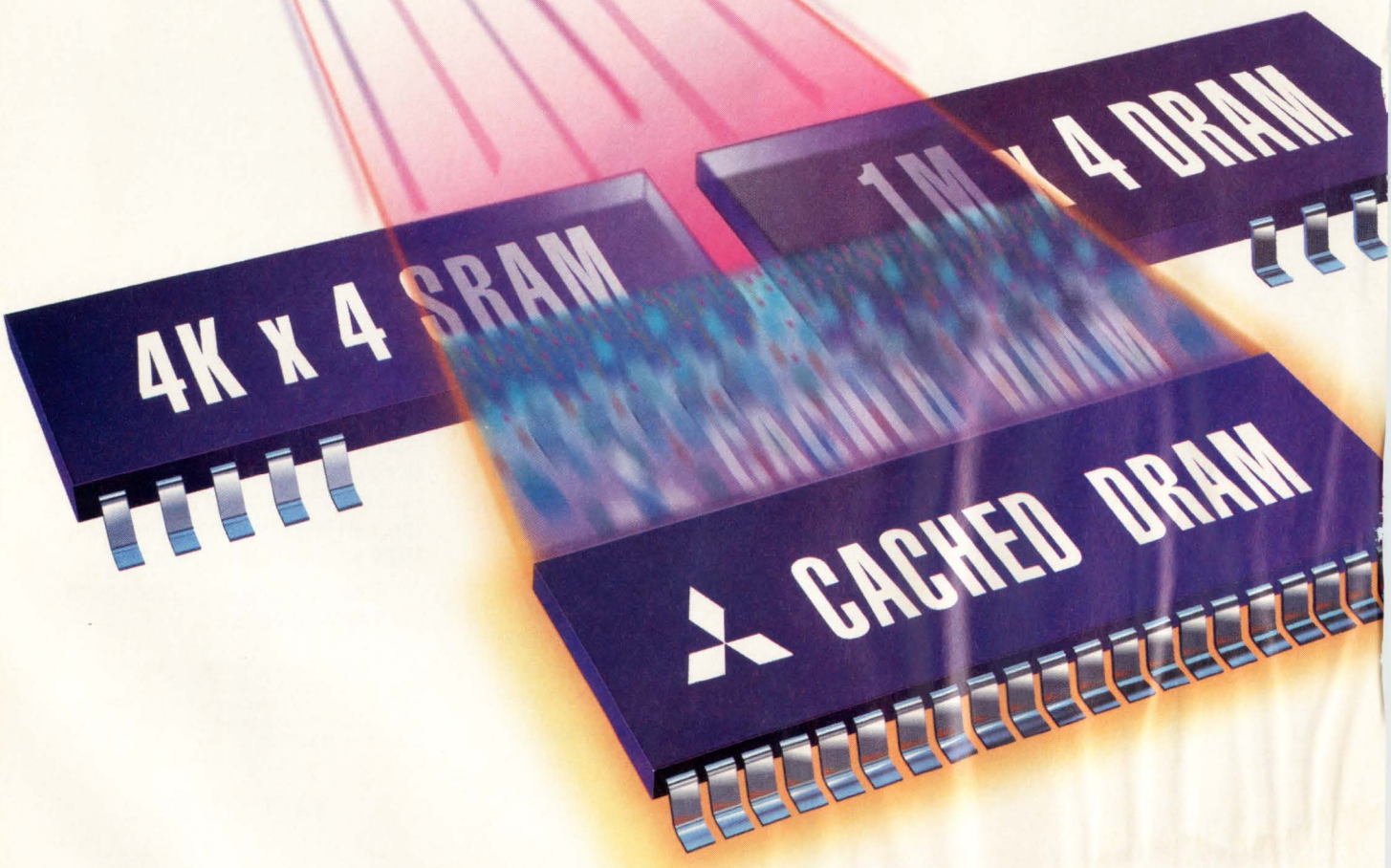
John Fluke Mfg. Co., Inc., P.O. Box 9090, M/S 250C,
Everett, WA 98206-9090. U.S. (206) 356-5400.
Canada (416) 890-7600. Other countries: (206) 356-5500.

FAST ANSWERS

FLUKE®

CIRCLE NO. 40

Synchronous 4Mb At 100MHz,



Cached DRAM. It Screams!

Matching low-cost DRAM technology with today's high-speed CPUs can be a design engineer's nightmare. Until now. **Introducing the 100MHz 4Mb Cached DRAM from Mitsubishi.**

FIRST SYNCHRONOUS DRAM

Mitsubishi combined a fast, 4K x 4 SRAM and a 1M x 4 DRAM with a wide, 16 x 4 bit internal bus and a synchronous clock design, all into one tiny TSOP IC. The result is the industry's first synchronous DRAM with on-board cache.

100MHz OPERATION

The Cached DRAM's large, 16 x 4 bit internal data path can transfer a 16-line data block in just one cycle, allowing the small on-chip cache to perform like a much larger external cache. The result is fast, 100MHz performance at a much lower cost than separate cache configurations. Plus, the Cached DRAM's fast copy-back scheme significantly reduces the miss cycle penalty time.

COST-EFFICIENT, SMALL SIZE

The Cached DRAM die and package are only 7% larger than those of a standard 1M x 4 DRAM. And, since they are manufactured with the same process and on the same production line as Mitsubishi's standard 4Mb DRAMs, Cached DRAMs are highly cost-efficient to manufacture.

LOW POWER OPERATION

With a clock that can be stopped to reduce power consumption to as low as 1mW, the Cached DRAM is ideal for portable and highly integrated applications where low power consumption, compact size and fast operation are essential.

MITSUBISHI'S CACHED DRAM PERFORMANCE

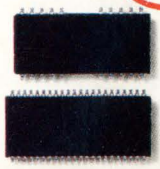
Part Number	Cache Hit Access/Cycle	Cache Miss Access/Cycle	Direct Array Access/Cycle	Package
M5M44409TP-10	10ns/10ns	70ns/280ns*	70ns/140ns	TSOP**
M5M44409TP-15	15ns/15ns	75ns/300ns*	75ns/150ns	TSOP**
M5M44409TP-20	20ns/20ns	80ns/320ns*	80ns/160ns	TSOP**

*Cache hit cycles can resume after one miss access time, while the copy-back completes in the background.

**TSOP Type II. Also available in reverse pin-out TSOP.

Samples Available June 1992

Not your ordinary next-generation DRAM, Mitsubishi's 4Mb synchronous Cached DRAM sets a totally new standard for cost-effective, high performance memory. For more information and technical specifications, please call **(408) 730-5900, ext. 2106 or 2226.**



Standard 4Mb DRAM.

Actual size.

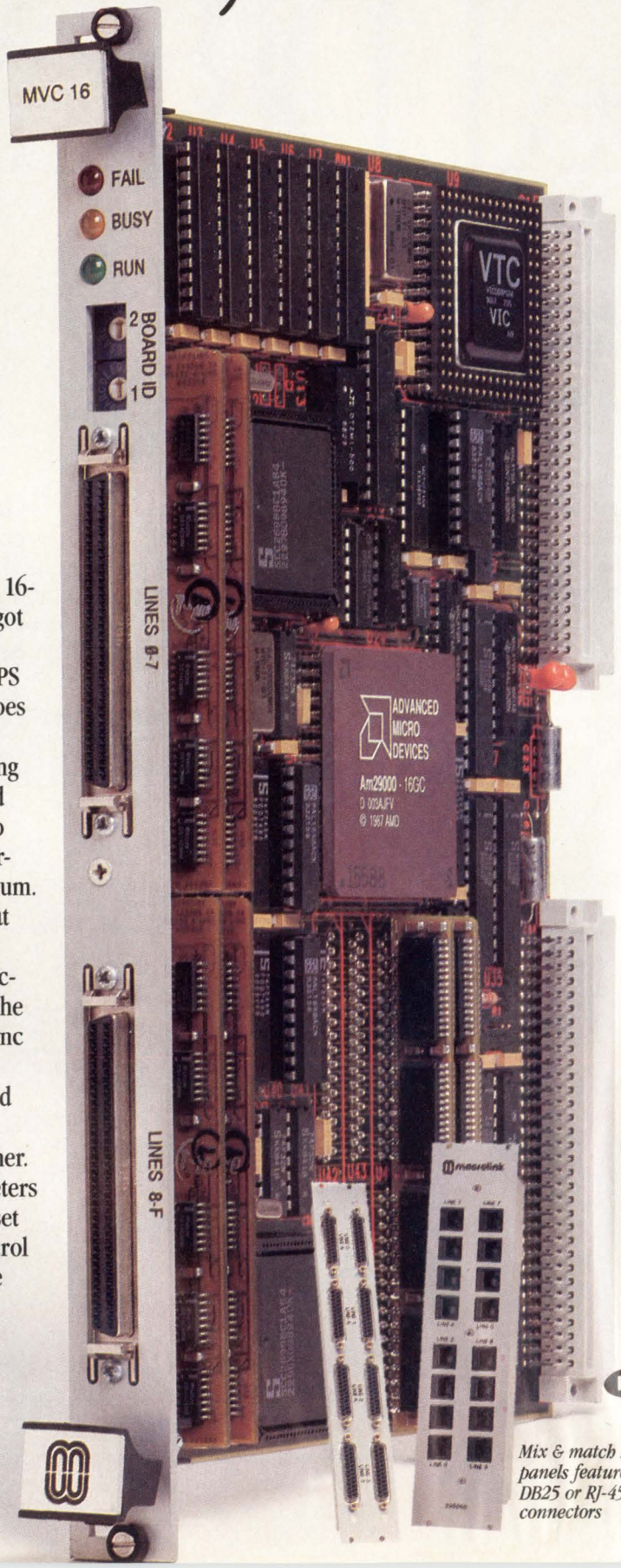
4Mb Cached DRAM is only 7% larger than a standard 4Mb DRAM.

VISION® ACTION REALITY

MITSUBISHI
ELECTRONIC DEVICE GROUP

CIRCLE NO. 41

16 lines, No waiting.



Mix & match I/O panels feature DB25 or RJ-45 connectors

Your application is first in line with the MVC 16-line Async Commux. It's got processing capacity to spare, thanks to a 16 MIPS RISC, so system power goes to your users—not I/O.

Character processing and buffering is managed on-board by our RISC, so driver calls and host overhead are kept to a minimum. All 16 lines can operate at 38.4 KBaud. That's over 61,000 characters per second throughput, double the rate of other VMEBus async controllers.

The MVC's advanced features benefit both the integrator and programmer. Port and VMEbus parameters are soft-configured and set line-by-line. Modem control is standard. Full software support is also included, along with diagnostics and a Streams driver.

Advanced memory architecture and high-speed buffering eliminate overruns and port domination. Memory is expandable from 128KB to 1MB, so the MVC handles today's requirements and future application needs.

With over 11 years experience producing advanced storage, communications and memory products, Macrolink delivers the powerful and flexible MVC in 8 and 16 line configurations. Call us today. We won't keep you waiting.

Macrolink Inc.,
1500 North Kellogg Drive,
Anaheim, California 92807.
Phone (714) 777-8800,
FAX (714) 777-8807.

macrolink® inc.

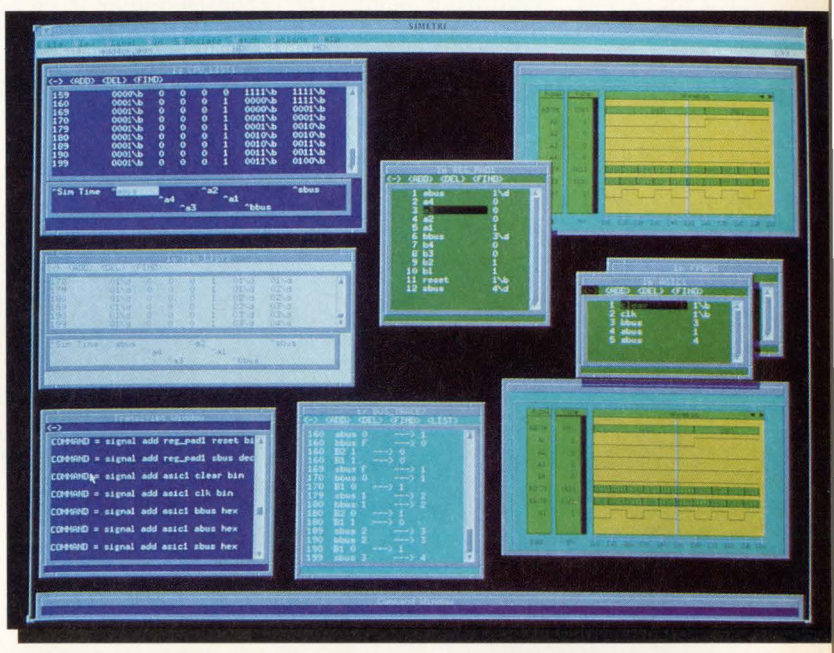
CIRCLE NO. 42

IDA INSTANT DATA ACCESS (IDA)
DIAL (617) 494-8338 DOCUMENT NO. 1037

Separating hype from reality in benchmarking

Benchmarking simulators is a tough job that tests users and vendors alike. But with adequate cooperation between the two camps, meaningful results can be achieved.

Mike Donlin, Senior Editor



In this shot of the Simetri simulator from Evaluations Per Second, user-defined windows let you view CPU activity with related time stamps (upper left windows), waveform information (upper and lower right), snapshot information on the simulator's current status (center window), and state changes (bottom center). The transcript window at the lower left stores commands issued to the simulator, while the windows at the center right show devices being evaluated.

Anyone who's participated in a simulation benchmark knows that it's a lot like test-driving a car, except that you're learning to drive while you're evaluating the product. Though the term benchmark conjures up a suite of tests that will ensure the simulator you purchase is the right one for your designs, a closer look reveals that finding the best simulator is a task fraught with difficulties.

Are your designs mostly digital? Are they mostly analog? Are you pushing silicon or circuit-board technology so that timing becomes critical? Do you have modeling expertise? The list is practically endless and the resulting confusion over just what makes a good benchmark has frustrated the EDA community, both vendors and users, for years.

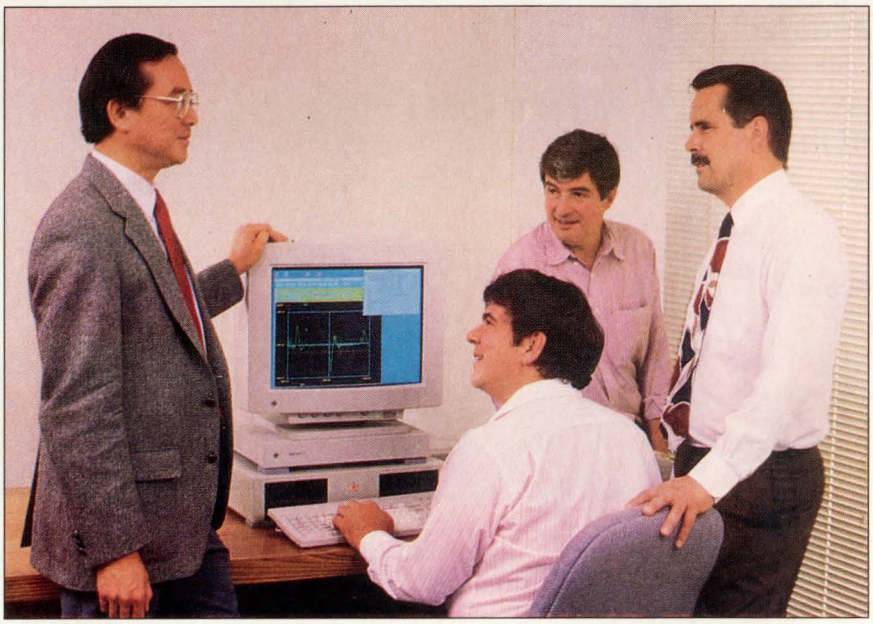
The stakes are high, too. Not only are simulators costly, but the very nature of analog simulation requires you to bank on its ability to make accurate predictions of your design's behavior. You'll be depending on it to help you debug your circuit. And you'll spend a staggering amount of money and time on model development to drive the simulator. A wrong decision can ruin a company's reputation, and making the right decision can still eat up dozens of man-hours of evaluation time.

"Generally, vendors don't like benchmarking," says Hal Alles, corporate architect at Mentor Graphics (Wilsonville, OR), "because it's like buying a lottery ticket—a lot is left to chance. If vendors do get involved, and we all do, it's best to take control of the situation as soon as possible. And that should serve as a caution to the user community. Right off the bat, every simulator has built-in limitations—that is, every simulator makes certain assumptions about how the real world is going to behave. If customers aren't really involved in the benchmark, if they don't understand these assumptions, they might end up with a simulator that isn't right for their designs. It's easy for any vendor to tune a benchmark to make his simulator look good. That's why it's foolish to let any one vendor run the show."

Though it would seem only logical for customers to get involved in a benchmarking operation, the task is so daunting and time-consuming that many users might be tempted to take the easy way out and just send some

representative circuits out for evaluation by the simulation vendors. This can be a costly mistake. First of all, as Alles points out, almost any savvy vendor can fudge benchmark results in his or her favor. Second, an uninvolved customer will be stuck with a simulator that he or she knows little about after the benchmarking is over. Even seasoned designers find the benchmarking process frustrating, mainly because the time spent evaluating competing products isn't necessarily time spent producing a design.

"We once performed benchmarks for a whole summer and never got any real satisfaction," says Terry Coston, director of design systems at Harris Semiconductor (Melbourne, FL). "We ended up putting together a simulator with Verilog and Spice and it's doing the job, but arriving at that solution wasn't easy. The most important thing is to get the simulator in-house and do it yourself. Remember, no vendor has ever lost a benchmark."



"Successful benchmarks occur when both the user and vendor commit resources to the task," says Paul Wang (left), vice-president of the CAE division at Contec Microelectronics. "Vendors can help develop accurate models of the circuit, but the customer should have accurate measurements from his design or it's hard to verify the results."

Should vendors run the show?

For obvious reasons, it would seem that vendors would want to run the benchmarking show, but this isn't always the case. Customer involvement will pay off after the purchasing decision is made, vendors contend, because the customer will have chosen a simulator that actually works with his or her designs. Vendors know that a sale made under false pretenses will only come back to haunt them.

"Just throwing a schematic at a vendor without a clear description of the conditions in which it's going to operate is a mistake," says Kevin Jorgensen, product marketing manager at Viewlogic Systems (Marlborough, MA). "It's in everyone's best interest to really look at what the customer is doing. That means working with the customer and coming up with a real engineering application after the benchmark is done. This gives the engineer doing the evaluations something he can show to his peers that will be used to develop a real circuit. Customer participation is crucial."

Many vendors also agree that customers should know whether the circuits they're benchmarking have problems. They might use older circuits that had bugs, or they might bring in circuits that are under development with unknown bugs. In either case, the resulting benchmarks can show real results because the simulator will prove its mettle by debugging actual design flaws.

"If I were the customer, I'd write my own benchmarks," says Paul Wang, vice-president of the CAE division at Contec Microelectronics (San Jose, CA). "It's a tough but worthwhile job. Surprisingly enough, many customers come to us with a circuit to simulate and don't know what the results should be. It's far better to design and measure a representative circuit and see which vendors can simulate it accurately."

Easier said than done

The problem lies in designing a circuit that will be global enough to ensure simulation success in future designs, while being specific enough to ensure an even playing field among the competing simulators. Even simulation benchmarks sponsored by unbiased third parties can breed confusion, as was demonstrated by the IEEE-sponsored Bipolar Circuit and Technology Meeting (BCTM) held in Minneapolis in September of 1990.

Each of the participants in the BCTM was given a design specification for a fictitious 12-bit successive approximation register (SAR) analog-to-digital converter. Process models for the converter were provided by the BCTM. The object of the benchmark was to simulate the entire converter through a complete conversion cycle (13 clock cycles) and report on maximum conversion time, time required for simulation and limiting factors of the design.

The converter was an excellent device for testing mixed-signal simulators because the circuit relied on both analog-to-analog and analog-to-digital feedback. Because many of the commercially available mixed-signal simulators either don't handle mixed-signal feedback or are hard to use with feedback loops, the circuit promised to be a challenge for the participating EDA vendors. The good news from the competition was that most of the vendors were successful in simulating the circuit. The bad news was that there was no clear winner, as each vendor could lay claim to some performance advantage over the others. Why the confusion?

"The BCTM benchmark had some undefined parameters," says Viewlogic's Jorgensen. "Though the circuit was well defined, we didn't have a clear idea of the conditions that it would operate under. There was no set clock rate, for instance, and that caused some problems. After all, no circuit operates in a vacuum."

Both vendors and users alike, therefore, must define how a circuit is going to be used in a design, or a benchmark can produce ambiguous results. "In the BCTM example, it

would have been very important to know what we were trying to accomplish," says Shawn Hailey, president of Meta-Software (Campbell, CA). "If the purpose of the overall design was speed, then it might be necessary to push some components to their limits. We found out, for instance, that in that design there were a couple of op amps that were marginally unstable. An abstract simulation wouldn't have caught that, but if the circuit wasn't going to be running at speed, it wouldn't have made a difference."

The upshot of BCTM, then, is that you have to know where you're headed before you start out, a condition that can't always be met in a benchmarking scenario. So where do you start? Most vendors agree that the best place is with your product—what are you designing?

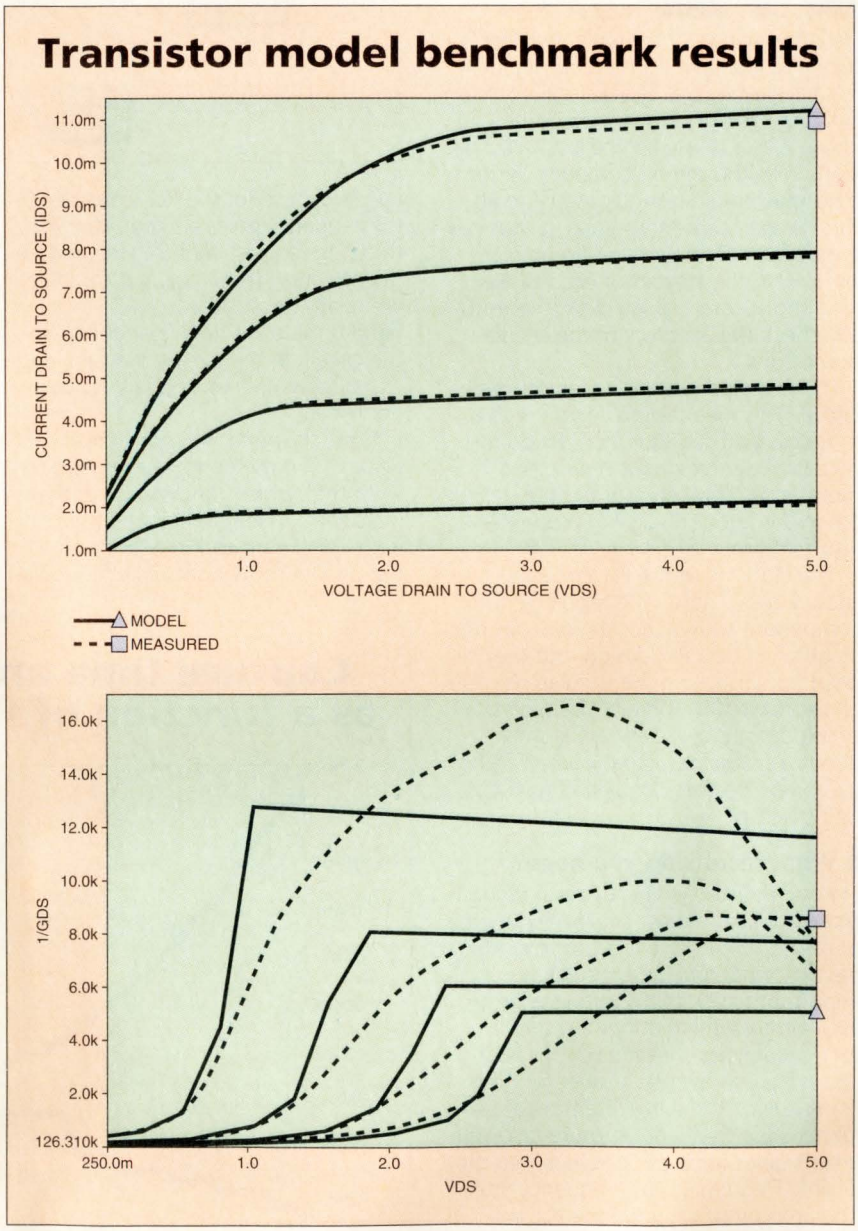
Printed circuit board (PCB) designers will need to run their simulation benchmarks differently than IC designers. "PCB or system engineers will probably be using a lot of standard parts in their designs," says Prasad Subramaniam, supervisor in the CAD/CAE product management group at AT&T Bell Laboratories (Murray Hill, NJ). "They may not need to write a lot of models and can depend on commercially available hardware and software models for simulation. In other words, they can assume that the components are good and concentrate on how they use them. Silicon designers, on the other hand, will be using A-D converters, phase-locked loops and op amps, which can be very vendor-specific regarding the fine points of their operating parameters. Good device models become critical to the operation of the circuit. In each case, the simulators are doing different things and therefore need to be benchmarked differently."

Simulation trade-offs

In addition to keeping your ultimate goal in mind, it's necessary to evaluate performance features that will be crucial to your final choice. Some simulators sacrifice accuracy for speed, a trade-off which seems fatal, but isn't necessarily a flaw if you're going to use the simulator continually during a design process. "You might get away with a fast behavioral simulator if you're going to use it primarily to search for design errors, " says Brian Miller, simulation product manager at Teradyne (Boston, MA). "In a scenario like that you'd be looking for a partial, rather than a full-bore, simulation. A less accurate behavioral evaluation might be alright under those circumstances."

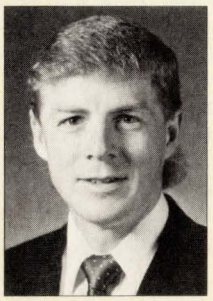
Even in design environments where there's leeway in the accuracy department, the speed-vs.-accuracy debate rages. Naturally, no simulator is worth anything if it's not somewhat accurate, but the level of accuracy can be leveraged for speed, a choice that demands that you know how much you can sacrifice and when. Analog circuits are notoriously slow to simulate, but demand a high degree of accuracy or the final design may not work at all. A purely behavioral approach to an analog circuit might produce good results for design verification, but might fall flat for debugging critical circuits.

"The problem with behavioral analog simulation is deciding which



Accurate modeling information is of paramount importance in benchmark results. In (A), this model of a transistor was quickly extracted and might be presented as "accurate to 3 percent." But a 3 percent accuracy in current tells you very little about the accuracy of the conductance G_{DS} (resistance of the transistor) in saturation. (B) takes a derivative fit of G_{DS} and shows that the output impedance is off by a factor of two, in spite of the 3 percent accuracy in I_{DS} (current drain to source). Both models were provided by Meta-Software's Meta-Labs Division.

Getting involved in the benchmarking process



An interactive method of benchmarking makes the user a participant in the evaluation process, yet still lets the vendor show the simulator's full capabilities. Such benchmarking, for example, was performed by an analog circuit designer who evaluated the Saber simulator from Analogy. The benchmark circuit he chose was a phase-locked loop (PLL) design. Even though his company designs a number of different types of circuits, the PLL was chosen because he was having trouble designing and accurately simulating these types of circuits. He also had substantial lab data to eventually check the accuracy of the simulation results.

The first step was to 'water down' the circuit. This meant simplifying it into a more general configuration. By doing this, the user created a circuit that more accurately represented the design process without disclosing proprietary information.

The diagram of the PLL circuit is shown above right. The topology and component values chosen were not necessarily the best PLL design, but they sufficed for illustrating the simulator's capabilities. (Actually, some of the worst circuit designs often show the most about a simulator's capabilities. If all circuits were perfect, simulators wouldn't be necessary.)

What results do you need?

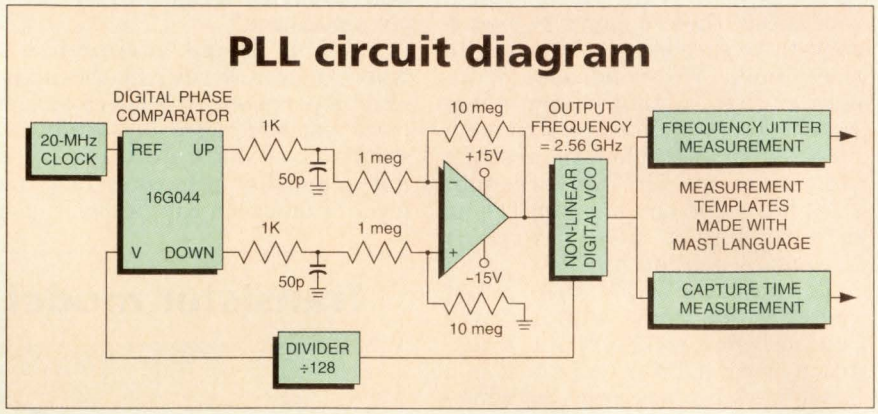
The second step of this benchmarking process was the most critical. What type of results would give the customer the best information about the circuit? It's important to ask this question without assuming anything about the simulator's capabilities—let the vendor worry about how to get the answer for now. For this circuit, the important measurements were frequency capture time (the time it takes for the PLL to lock into the desired frequency) and frequency jitter (the amount of variation the PLL will have once it's in lock).

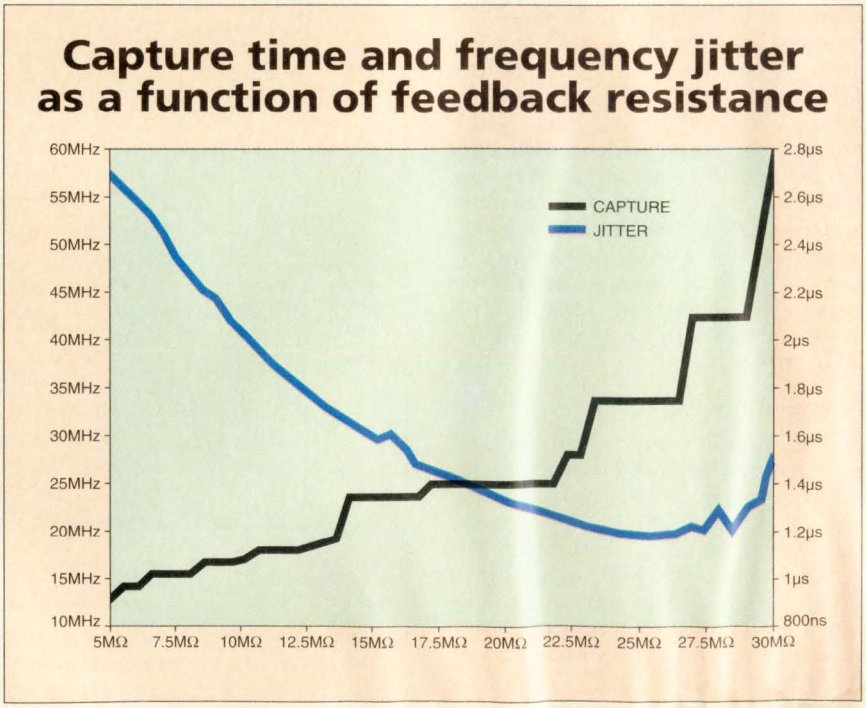
But this still wasn't all the user wanted. He needed to know what values to choose for the PLL's low-pass filter frequency poles and amplifier gain to get the lowest capture time and frequency jitter. These circuit parameters are nearly impossible to calculate by hand if there are nonlinear devices in the circuit. In this circuit, the frequency-vs.-voltage function of the VCO was nonlinear.

Now, the vendor began actively participating in the benchmarking process. With the vendor's knowledge of the simulator and a clear definition of the ultimate goal, a procedure was devised that would show how well the simulator could perform the desired task. To accomplish the particular tasks of the PLL benchmark, a four-step procedure was incorporated by the Analogy application engineer.

The benchmark begins

First, the engineer determined that two devices weren't available with the simulator's standard library—the phase detector and the VCO. Both were created with Saber's Mast modeling language. The VCO was particularly interesting because the frequency-vs.-voltage function was determined by a set of value





Mark Chadwick, product marketing manager, Analogy, Beaverton, OR

pairs originally measured with lab equipment. The VCO model was implemented in such a way that a look-up table of these value pairs was directly accessed. This model was especially beneficial to the user because he could easily change the look-up table.

To enable parameters to be varied, fast simulation times were a must. Single simulations with Spice took over three hours. By using mixed-mode simulation and some behavioral models for selected devices, that simulation time was cut to under two minutes.

To measure the capture time and frequency jitter, special measurement models were created with Mast. These models automatically measured these two parameters and displayed their values during the simulations. These models were eventually added to one of the standard Saber model libraries.

The last operation was a parameter sweep. This function let the user automatically sweep any of the circuit parameters while performing multiple simulations. The final results are the curves shown at left. The X-axis of the graph represents the resistance of the feedback resistor in the amplifier section. The Y-axis represents both the capture time and frequency jitter of the PLL. Here now was a single, concise graph that showed the engineer the nonlinear performance of the PLL. The engineer could easily determine the trade-offs in circuit performance with this information. In addition, the Analogy application engineer showed how statistical Monte Carlo analysis could be used for further analysis of the circuit.

The final step of the benchmark was to have the user take over the simulation of the circuit. He then modified the simulated circuit himselfvp

to the exact structure of the real circuit. By having the vendor perform the original simulation, the user skipped the beginning of the learning curve and could get hands-on experience using the simulator with a circuit he was familiar with. Comparisons between the final simulation results and lab measurements showed excellent correlation. The results of the benchmark showed the simulator's full capabilities to solve problems that were relevant to the user's particular needs.

behavior you're going to simulate," says Meta-Software's Hailey. "I've seen perfectly fine behavioral models that gave a good rendition of voltages but had nothing in the current domain. They were awful when it came to things like system-level ground bounce. The behavioral concept was all right for portions of the simulation, but the unspecified behavior of the circuit could have been disastrous for the final design."

Divide and conquer

To get around these hazards, vendors advise their customers to partition their designs into critical paths for detailed simulation and less critical paths for behavioral analysis. But in mixed-signal designs, circuit partitioning isn't as simple as it seems. Obviously, some components are purely digital and some are purely analog, but there are some hazy areas, such as the analog effects in digital circuits, where you must make partitioning decisions. As always, there are trade-offs involved.

In general, an analog model of a circuit will be more accurate than a digital one because the digital model is an approximation of a circuit's behavior. When the approximation is good, there's at least a factor of 10 difference in simulation speed, because a digital simulation is following an event cue whereas an analog program is integrating a set of coupled, nonlinear differential equations.

There are other advantages to the digital approach if the approximation is accurate. Digital simulation can apply worst-case timing analysis and fault simulation to portions of the circuit—a capability that's lacking in analog simulation. In addition, digital simulations can use hardware models, a capability that's particularly useful when there are complex devices such as microprocessors in your design.

When all is said and done, however, a lot of the decisions about partitioning a circuit come down to the expertise of the designer. The critical thing to remember when benchmarking an analog simulator is that you are working with models, not real devices. Understanding this limitation is critical when you're evaluating a simulator. You must understand the trade-offs when using a Spice model, a hardware model or a behavioral model. You can use a transistor as either a linear device or a switch, but you have to know the consequences of your decision.

Speed traps

All of these trade-offs are, of course, in the interest of speed. Unfortunately, speed is an area where vendors can play games with simulation results, so the buyer has to beware. "We believe that the best measure of a simulator's speed is events per second," says Michael Massa, president of Evaluations Per Second (Waltham, MA), "where an event happens when the output of a gate changes. Some vendors use evaluations per second, which measures inputs to a gate. In an event-driven simulator, the only real activity is when an output changes, not an input. Evaluating inputs can give high numbers to a simulator's benchmark figures, but doesn't really reflect what's going on in a circuit. Besides it's overkill."

Massa also cautions against arcane methods of evaluating a simulator using a 'gates per second' figure. "Older simulators looked at all the gates on every time tick," he says. "That produces an even higher number of evaluations with even more time wasted."

Even when you know the definition of the speed terms applied in a benchmark report, there are still subtle ways that the numbers can be presented. Timing information can be incorporated into the equation in such a way as to give skewed results. "My definition of events per second is to look at a bunch of two-input gates that have all the inputs wired together going to a clock that doesn't overlap the propagation delay through a device," says Rich Gogesch, engineer at OrCad (Hillsboro, OR). "Let's say you have a device with a 5-ns propagation delay. You use a clock that exceeds 5 ns on the low and high pulse and you use that to evaluate events per second. I've seen benchmarks from an accelerator company that boasted 100,000 events per second, and all I got with their product was 50,000. They used an inverter and matched the propagation delay to the clock input and effectively doubled their performance. You have to be careful of the games vendors play."

Easy does it

In addition to the speed/accuracy claims and counterclaims of vendors, there can also be gamesmanship in ease-of-use features. While

these features are important, they really aren't at the heart of what a simulator does. In other words, a colorful, multiwindowed environment is useless if you don't get accurate results. The user community has made it clear that it doesn't want to make confusing transitions as it moves around its design environments, and vendors have responded with easier-to-use graphi-

"Not every circuit requires the same simulation data," according to Brian Miller, simulation product manager at Teradyne. "Designs that push technology to the limit—marginal designs—require worst-case timing information, while nominal designs might get away without a close examination of timing parameters. The design should drive the simulator, not the other way around."

cal user interfaces. But caution is advised when putting too much emphasis on look and feel. "Don't get carried away with the niceties," warns Marsha Huff, applications engineer at Racal-Redac (Mahwah, NJ). "If customers limit themselves to demos and marketing hype, they might end up dazzled with a lot of smoke and mirrors and end up with a simulator that doesn't fit their needs. A good user interface is important, but not nearly as important as knowing what the simulator's doing."

A less obvious side of the ease-of-use portion of a benchmark is ease of integration. This benefit might not be as easy to quantify in a benchmarking scenario where evaluations per second and successful convergence are the buzzwords. But a simulator doesn't run in a vacuum—you must be able to backannotate results into the front end of the design or iterations can become tedious, time-consuming affairs.

"We've seen our share of simulators that were fine performers but which no one used because they were impossible to integrate," says George Edgar, applications engineer at Jet Propulsion Laboratories (Pasadena, CA). "If you have to pop up all kinds of schematics and input probes, it's easy to get lost. We had one large vendor in here, whose name I won't mention, who gave a good demo but whose product wouldn't work with anything else."

Ease of integration has always been a problem for simulators, mainly because of a lack of standards for models and design representation information. The efforts of the CAD Framework Initiative (CFI) are going a long way toward resolving these inconsistencies, but until standards are hammered out users must be wary of simulators that won't cooperate with the rest of a design environment.

"You should always be aware of the global engineering task," says Dundar Dumlugol, director of simulation modeling at Cadence Design Systems (San Jose, CA). "You have to look not just at the time spent in simulation, but at the time spent in the entire design process. This means a simulator must have features that let you analyze the data that the simulator has produced. You have to look at netlisting, how easy it is to access your results, waveform-analysis tools, and post-processing functions in general. A simulator that can't help you debug your design isn't very useful."

Service is key

All of these ease-of-use features indirectly point to one thing—vendor support after the sale. Unfortunately, this feature isn't obvious at benchmarking time. "We've been burned by vendors who became invisible after the sale," says Larry Hamilton, supervisor of test engineering at E-Systems (Dallas, TX), a defense contractor that makes computer systems. "When you're in the middle of a design problem, the last thing you need is the runaround from the vendor. If it takes several days to get a return call from the support people, you're in trouble."

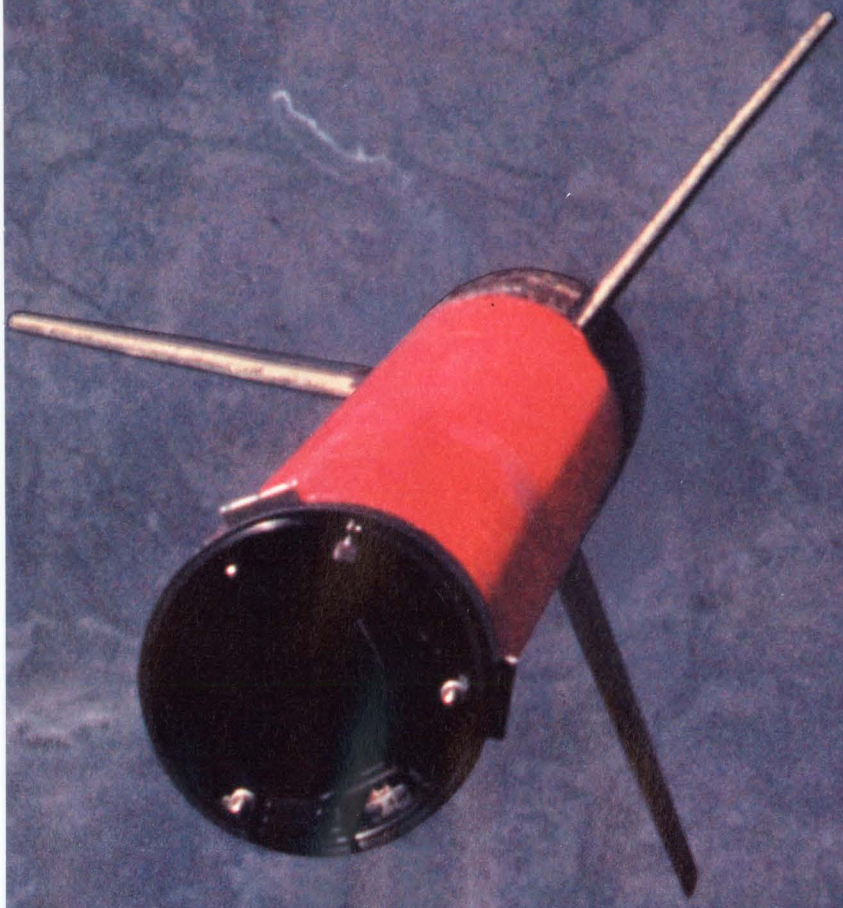
With all of the perils in benchmarking simulators, it's no wonder that users and vendors alike are put off by the task. A vendor that wins a benchmark under false pretenses is saddled with an unhappy customer and a potential for a bad reputation. A user that chooses the wrong simulator will face years of frustration or possible unemployment. But with all its pitfalls, benchmarking is still the only way to find out if a simulator will fill the bill. The best weapon, then, is being informed.

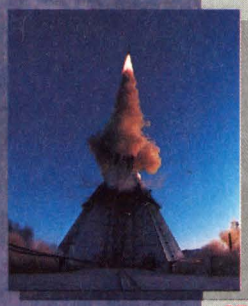
"An uninvolved customer is deadly," says Teradyne's Miller. "If you're a designer with a problem, you have to rely on your simulator to help you solve it. Now maybe that simulator will help you debug 90 percent of your circuit. Is that unknown 10 percent going to be irrelevant or is it going to shut down the fab? If you don't know the answer to that, you're asking for trouble." ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Analogy (503) 626-9700	Circle 220
Cadence Design Systems (408) 943-1234	Circle 221
Contec Microelectronics (408) 434-6767	Circle 222
Evaluations Per Second (617) 487-9959	Circle 223
Meta-Software (408) 371-5100	Circle 224
Mentor Graphics (503) 685-7000	Circle 225
OrCad (503) 690-9881	Circle 226
Racal-Redac (201) 848-8000	Circle 227
Teradyne (617) 482-2700	Circle 228
Viewlogic Systems (508) 480-0881	Circle 229

Only the best in outer space





In outer space, 700 kilometres over the earth's surface, conditions are at their harshest. Huge investments depend on the reliability of every single component. Failures can be fatal. That's why professional computer users rely on or products. You too should only have the best for your money.

or provides one of the largest selections of single height VMEbus boards, consequently designed in a CMOS technology. Our range contains 68000 family and IBM compatible CPU boards, signal processors, graphics, industrial I/O, mass storage and network controllers as well as OS-9, VRTX 32, VxWorks, PDOS, PSOS+, RTOS and MSDOS operating systems.

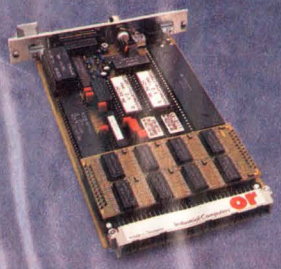
Our CPU family has only recently been extended to include the high performance VCPU-30 module. For a module with 12 MIPS the price is extremely cost efficient. Boards with the 68040 and 80486 will be available shortly.

or

oettle + reichler GmbH
Industrial Computers
Sieglindenstr. 19½, D-8900 Augsburg 1
Tel. (0821) 5034-0, Fax (0821) 5034-119

In the US and Canada contact:
DYNATEM
15795 Rockfield Boulevard
Suite G, Irvine, CA 92718
Tel. (714) 855-3235, Fax 770-3481

VMEbus boards able to meet the highest demands

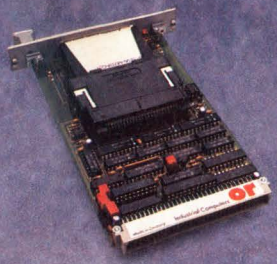


VLAN-10:
Intelligent Ethernet Controller

- Ethernet and cheapernet interface
- 256 Kbyte dual ported SRAM (opt. 1 Mbyte)
- Local 68HC000 CPU with 12.5 MHz offloads the host-CPU and the VMEbus dramatically
- Easy system-integration
- Operating-system-integration for OS-9, VRTX and VxWorks available

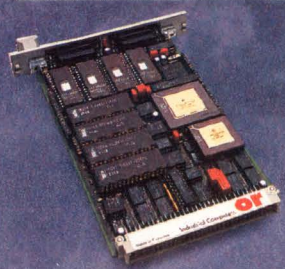
Network Software for VLAN-10

- TCP/IP ■ OS-9/NET ■ DECNET
- SO/OSI ■ SINEC AP 1.0



VMEM-10: Memory Card Interface

- Non-sensitive to dust, shocks and vibrations
- For memory cards up to 8 Mbyte capacity
- 8-bit and 16-bit wide databus
- CMOS RAM or ROM memory cards useable
- Data-transferrate max. 5 Mbyte/sec
- Battery backup and write-protection-switch
- Low battery voltage detector
- Compliant with VMEbus specifications ANSI/IEEE STD-1014 and IEC 821/297 also the high speed address-pipelining
- RAM-Floppy software-driver available
- Optional –40°C to +85°C operating temperature
- Low power +5V, 0.1 A



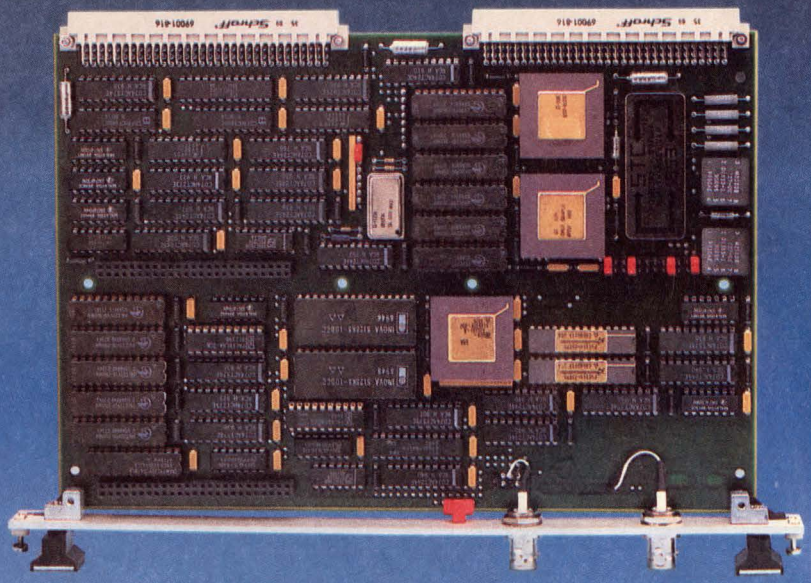
VCPU-30: High Performance CPU Board

- MC68030 50MHz HCMOS processor
- MC68881/2 floating point unit
- 2 Mbyte dual-ported SRAM max.
- 8 Mbyte dual-ported DRAM max. (burst mode)
- 2 Mbyte EPROM max.
- 2 async./sync. RS-232/422 channels
- Realtime clock, watchdog
- System controller, 4-level arbiter
- Multiprocessor-capability, mailbox-interrupt
- Optional SCSI and floppy interface
- Optional –40°C to +85°C operating temperature
- OS-9, PDOS, PSOS+, VRTX and VxWorks available
- Low power +5V, 0.9A

CIRCLE NO. 43

NEW FROM VMIC

MIL-STD-1553B COMMUNICATIONS CONTROLLER INTERFACE FOR VMEbus COMPUTERS



VMIC's New VMIVME-6000 Operates as Bus Controller, Bus Simulator, Multiple Remote Terminal/Monitor and Bus Analyzer.

The VMIVME-6000 also uses configuration register definitions implemented in the VXIbus specifications for a register based device. The unit provides 128K x 16 bits of dual port RAM for constructing control block information and storing transmitted and received 1553 bus data. This very flexible VMIVME-6000 unit is based upon a field-proven CMOS ASIC (Semi-Custom Application Specific Integrated Circuit) chip set, which provides on-board intelligence, superior functionality, and relatively low power consumption.

TWO YEAR WARRANTY

• **SOFTWARE-SELECTABLE PROTOCOL** - MIL-STD-1553A, MIL-STD-1553B, McAir A3818/A5232.A5690, General Dynamics 16PP303/690 • **PROGRAMMABLE CONFIGURATIONS** - Bus Controller, Bus Simulator, Multiple Remote Terminal/Monitor, Bus Analyzer, Diagnostic (Self-Test) • **POWERFUL CUSTOM ASIC-BASED DESIGN • 256 KBYTE OF DUAL PORT MEMORY • VXI CONTROL AND CONFIGURATION (REGISTER-BASED DEVICE) • ERROR GENERATION CAPABILITIES** - Parity, Bit Count (17 to 28 bit Times), Manchester Errors including both Bi-Phase and Transition Errors, Sync Errors in Both Command Words and Data Words, No Response and Late Responses (Programmable in µsec Increments), Incorrect TA Error (Status Word), Word Count (Plus and Minus), Gaps Between Data Words • **DOUBLE HEIGHT (6U) BOARD • FLEXIBLE PROGRAMMABLE INTERRUPTS**

1-800-322-3616

VMIC VME

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(205)880-0444 FAX (205)882-0859

CIRCLE NO. 44

High-performance networks challenge Ethernet

A half-dozen high-performance network interfaces—including three proposed standards—dominate the industry. Though each has advantages in its particular area, price/performance will undoubtedly push the market toward a single approach.

Warren Andrews, Senior Editor

Ethernet, the de facto computer industry network standard, is more than 10 years old and is starting to show its age. Though it enjoys by far the largest installed base of any approach, its maximum transfer rate of 10 Mbits/s—and real-world transfer rate of only about 2 to 3 Mbits/s—is far from satisfying current, not to mention future, needs. It's now many generations behind the succession of CISC and RISC processors that call for communications with a greater transmission bandwidth. That Ethernet has survived as long as it has is more a testimony to the vacuum in networking technology than it is to the inherent vitality of the standard.

But that vacuum is about to be filled with new approaches, most of which have promised to bring communications bandwidths to the Gbit/s range and beyond. These include FDDI (Fiber Distributed Data Interface), Fiber Channel and ATM (Asynchronous Transmission Mode) among the proposed standard approaches offered, as well as a small number of other, specialized, semiproprietary approaches—ScramNet from Systran Corporation (Dayton, OH), Universal Memory Network from Computer Sciences Corporation (Lompoc, CA), MCP from IronicsCorporation (Ithaca,

NY), and shared-memory approaches from vendors such as Lextel (Wakefield, MA), Bit-3 (Minneapolis, MN) and Augment Systems (Bedford, MA). While each approach was developed to meet some specialized communications need, there exist significant areas of overlap among them.

These approaches will undoubtedly coexist for some time, but it's likely that one will dominate the bulk of applications eventually—and this is true whether it's the best solution technologically or not. What will determine this winner isn't going to be raw bandwidth or flexibility, but some combination of features with the key element being price/performance. And, of course, what will drive price/performance won't be just the design approach and manufacturing technology; it will be sales volume.

Leading the way, therefore, will be those companies achieving both high volume and high performance—most notably, workstation manufacturers. The volume leaders at this point, Sun Microsystems (Mountain View, CA), IBM (Armonk, NY), Digital Equipment Corporation (Maynard, MA), and Hewlett-Packard (Palo Alto, CA), are all straddling the fence with regard to network interfaces.

Ironics vice-president of engineering Tom Rich stands next to his company's very high-speed data blaster as it transfers data from one computer to another. "Unlike traditional network and even reflective memory approaches," Rich says, "the Ironics approach looks almost like a DMA transfer, letting the receiving processor have immediate access to the data without having to find it in the address space."

Playing catchup

"We're hitting a bandwidth crisis now, driven by both increasing Mips and increasing I/O requirements," says Fred Sammartino, manager of high-speed networking and advanced development at Sun. "Processor performance has been doubling about every two years. And like anything experiencing that kind of exponential growth, it appears to start out slow then turns a corner and goes through the ceiling. We've been living in a period of blissful ignorance where we've lived with 10 Mbit/s Ethernet."

Sammartino explains that Ethernet has been helped along by partitioning systems into smaller segments, which in turn are boosted by high-performance routers and concentrators, but "all of a sudden," he adds, "you just run out of bandwidth. And because of the exponential growth of processor performance—and therefore network bandwidth requirements—once you run out of bandwidth, you're suddenly on a downward spiral which is very hard to get out of."

"Even going to a network like FDDI, with 10 times the bandwidth of Ethernet," contends Sammartino, "only gains you about three years at the most." Sammartino bases his estimate on processor and memory technology doubling every two years. "And when one looks at the type of costs it takes to restructure a network, a factor of 10 in bandwidth just isn't enough. What's really needed," he says, "is to go into a type of network structure that is scalable, so it not only solves today's problems but has a plan for the future—to scale up to faster rates as system requirements change."

There's little disagreement that greater network bandwidth is needed, and that future considerations should include some migration path for even greater bandwidths than are currently being considered. But there seems to be no consensus on what approach such an improved network should take.

Which way to go?

FDDI, as currently defined, only carries transfer rates to 100 Mbits/s, or about 12.5 Mbytes/s. But FDDI has a leg up because there are already a handful of chip sets on the market that support it, and a number of networks currently use it. Also, discussions are underway to scale FDDI up an order of magnitude—to a Gbit/s.

Alternatives to FDDI are few at present, and as yet none has been designated as a standard. The ATM approach is still undergoing solidification as a standard; it's expected it will be at least a year before things are settled out enough to start manufacturing chips and boards. And for Fiber Channel there are other considerations.

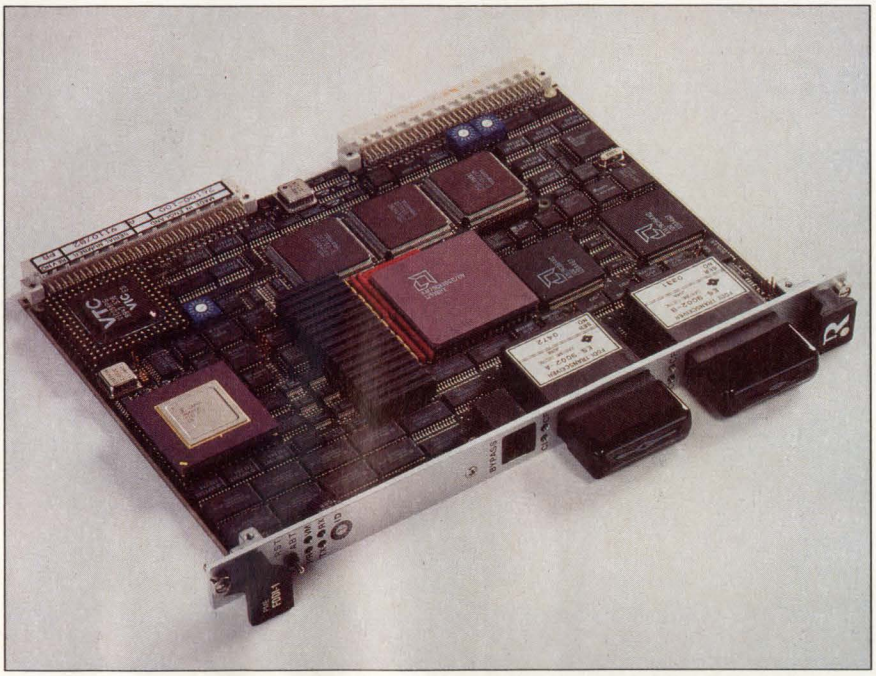
"Fiber Channel isn't really a network interface at all," says Steve Sibley, IBM's manager for the IBM/HP Fiber Channel alliance (Rochester, MN). "It's primarily designed to attach systems with a point-to-point link in a channel-type environment, and to map existing interfaces such as HiPPI and SCSI into a single standard." Although Fiber Channel was designed as a peripheral interface, some companies are already looking at manufacturing high-performance Fiber Channel switches, and others want to incorporate standard networking protocols into it, such as TCP/IP (Transmission Control Protocol/Internet Protocol) and OSI (Open Systems Interconnect). In addition, a study group is considering putting an ATM structure on Fiber Channel.

ATM is also undergoing specification, and a standards group is hard at work hammering out final details. In addition, there already exists an ATM chip consortium trying to design a chip set to implement the standard. The word from these groups is that the first practical ATM implementation won't take place until

well into 1993 or early 1994, and it will perhaps be 1995 before volume implementations arrive.

No need to wait

"FDDI is here now," says Joel Silverman, product manager for VME board maker Radstone Technology (Montvale, NJ), "and it satisfies customers' needs. There's little question that faster, more elaborate and even scalable interfaces are required, but people aren't going to wait until 1993, 1994 or beyond." Silverman adds that even though FDDI has been around for several years, it's only been in the last year or so that companies have been able to develop subsystems that make it practical.



Radstone Technology's FDDI-1 advanced architecture controller board for VMEbus, introduced this spring, is billed as the first 6U VME board to provide dual FDDI nodes in a single VME slot. Radstone claims the board is in full compliance with the FDDI PMD sublayer, thanks to its use of combined data link transceivers and integrated FDDI media interface connectors. It also employs the new SparcLite embedded processor.

"One of the keys to providing a practical FDDI interface," says Silverman, "has been to put as much of the network protocol intelligence onto a separate intelligent subsystem, to offload the protocol management from the host. Even a powerful host processor such as a Motorola 68030 or '040 can be brought to its knees if it gets involved doing protocol processing along with its other tasks."

But even with the benefits of an intelligent subsystem, FDDI has yet to live up to its rated performance. Few FDDI systems, if any, operate near the maximum bandwidth of 12.5 Mbytes/s (100 Mbits/s), and many systems achieve little better than 2- to 3-Mbyte/s rates. Even these rates, however, offer a major improvement over existing Ethernet connections.

FDDI is increasingly being used as a network backbone, rather than a desktop interface, primarily because of cost. Though there are now a handful of different FDDI chip sets, they're far from the point on the cost/volume curve where they make an inexpensive desktop interface. Furthermore, FDDI is currently defined as a fiberoptic interface, and it requires costly LED lasers and photodiode/phototransistor receivers, in addition to special connectors and splicing. Adding to the problems is the fact that most existing buildings are wired with copper, not optical fiber. The cost and time needed to replace copper wiring would make FDDI a costly solution if each node has to have a fiberoptic interface.

Copper stays alive

But help will soon be on the way. The FDDI committee is working out the final details for a low-cost, copper (twisted-pair) interface for the 100-Mbit/s standard. It's been reported that all of the technical hurdles have been cleared, and only some political issues remain. "Doing 100 Mbits/s over copper is not only eminently possible," says Sammartino, "but is very necessary."

Sammartino explains that the infrastructure isn't here to let networks immediately be changed over to fiber. He grants that new buildings will undoubtedly be wired with optical fiber, but replacing existing systems will be a slow process. That's why fiber and copper will have to coexist for some time.

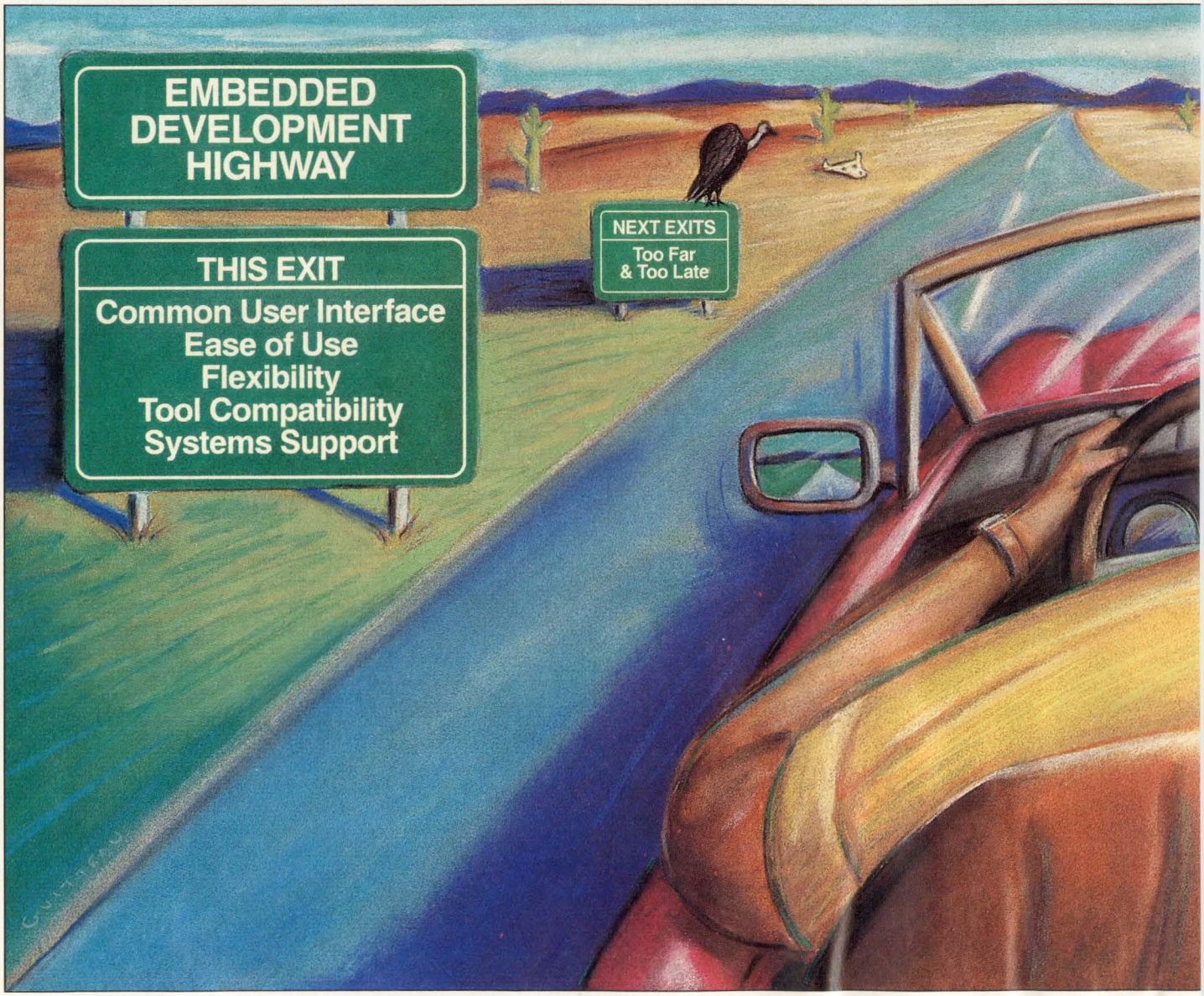
Even assuming optimum conditions—that the workforce of installers didn't need retraining to handle fiberoptic connectors and splices, that the entire base of installers was available to update older buildings rather than wire new ones and that the capital was available to perform the costly upgrades—only about three to five percent of existing systems could be retrofitted each year with existing manpower. That means that some intermediate step, such as using existing cabling, will be required.

It appears, then, that copper will be the fundamental transmission medium for all of the major approaches. FDDI, as mentioned, defines a 100-Mbit/s rate, which can be accommodated with today's copper technology. Fiber Channel also provides for lower rates, its lowest being 133 Mbits/s. The lowest of the ATM rates is a mere 51.840 Mbits/s.

Sammartino explains that, although FDDI transfers information at 100 Mbits/s, the line rate (baud) is about 125. "In comparison," he adds, "the line rate for ATM is 155, and, though somewhat higher than FDDI's 125, is close enough to allow the two to share the same technology. The technology exists today to run those signals over existing twisted-pair copper wire and stay within tolerable bit error and EMI."

Sammartino feels strongly that the availability of copper interfaces will be a compelling force in the implementation of next-generation networking technology. "Fiberoptic interfaces," he says, "will be too expensive for a real desktop LAN solution for quite some time." He explains that he's seen quotes of more than $50 per interface going out to the 1995 time frame. He believes this will make the price of a fiberoptic inter-

Before you get too far



Planning a large-scale embedded development project isn't exactly a Sunday drive. A wrong turn now could mean hazards further on.

There could be networking problems. Learning curve and team issues. Incompatibility between tools and systems from different vendors. And of course, the ever-present question of support.

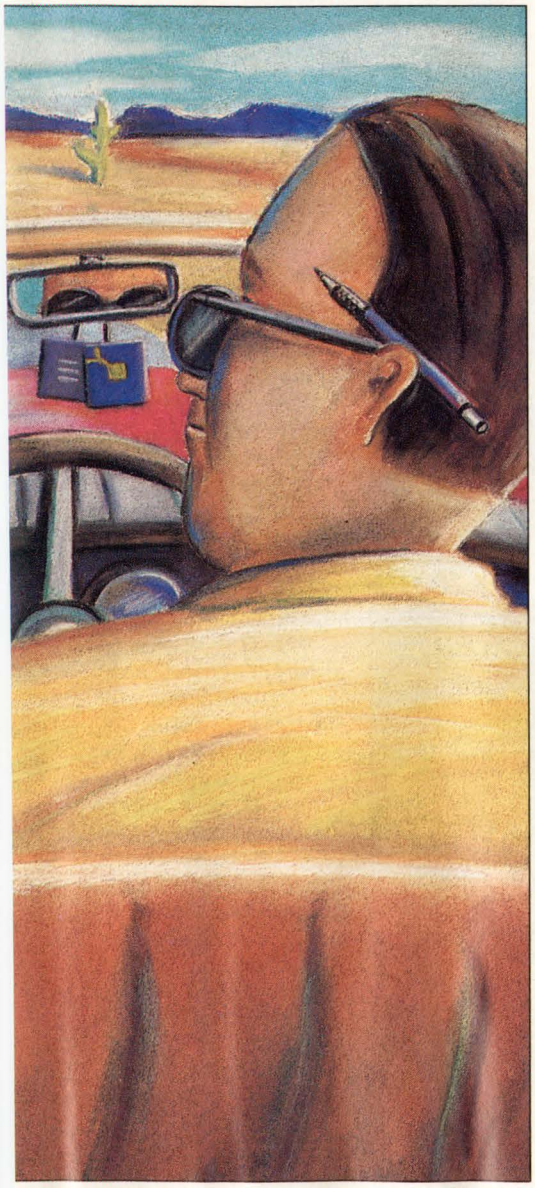
Major microprocessors supported by our development systems:

Intel	**Motorola**	
i960 CA	68030/EC030/020	
80386/286	68302	
80C186/188	68000/08/10	
80186/188		**Zilog**
80C86/88	**AMD**	Z8001
8086/88	Am386 DXL	Z8002

So here's a word to the wise: Talk to Applied before you've reached the point of no return. We can show you how to avoid costly detours.

In the U.S. and Canada, call 1-800-426-3925 (in WA, call 206-882-2000). Or contact Applied Microsystems Corporation, P.O. Box 97002, Redmond, WA 98073-9702 USA. **For the name of the nearest European distributor, call 44(0) 296-625462.** Europe Fax 011-44-296-623460. Or contact Applied Microsystems Corporation, Ltd., AMC House, South Street, Wendover, Aylesbury, Bucks, HP22 6EF, England.

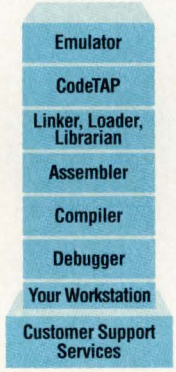
down the road, talk to us.



The right tools for the job.

We've designed our family of development solutions to be as flexible as they are powerful. Our emulators, simulators, CodeTAPs (Target Access Probe), debuggers, and compilers all work together seamlessly through a common interface. And our software lets you use many of your existing tools, so you can maximize the investments you've already made.

With our new CodeTAP family, you can afford to equip each software engineer with a powerful, in-circuit tool that puts emulation technology on their desktop. Which means that more engineers can be debugging more lines of code, earlier in the development process.



It all comes together through our integrated, systems approach.

We know the territory.

When it comes to large scale, high performance embedded development projects, we've been there. And not as a side business, but as our only business.

We've set up more than 12,000 embedded development systems worldwide. The majority of the world's top electronics companies use our solutions.

You couldn't hire somebody with that kind of experience. But when you put Applied to work for you, all this knowledge and understanding is at your disposal. It comes with the territory.

We're with you all the way.

If you've been stranded by vendors before, take note: We're with you for the long haul, providing you not only products and systems, but also planning, field engineering support, training, product upgrades, and complete documentation.

Sound good? Then call us at 1 800 343-3659 (in Washington call 206-882-2000) and let's talk about your specific development problems.

We'll help you find a solution that's right on track.

Applied Microsystems Corporation

Where it all comes together.

In Germany, call 06182/9203-0. Fax 06182/9203-15. Or contact Applied Microsystems GmbH, Dammstrasse 6, W-6453 Seligenstadt, Germany. Tel 06182/9203-0, Fax 06182/9203-15.
In Japan, call Applied Microsystems Japan, Ltd., Nihon Seimei Nishi-Gotanda Bldg., 7-24-5 Nishi-Gotanda, Shinagawa-Ku, Tokyo T141, Japan. Tel 03-4493-0770, Fax 03-493-7270.

CIRCLE NO. 45

face for the low-cost desktop prohibitive for some time to come.

Moving with Fiber Channel

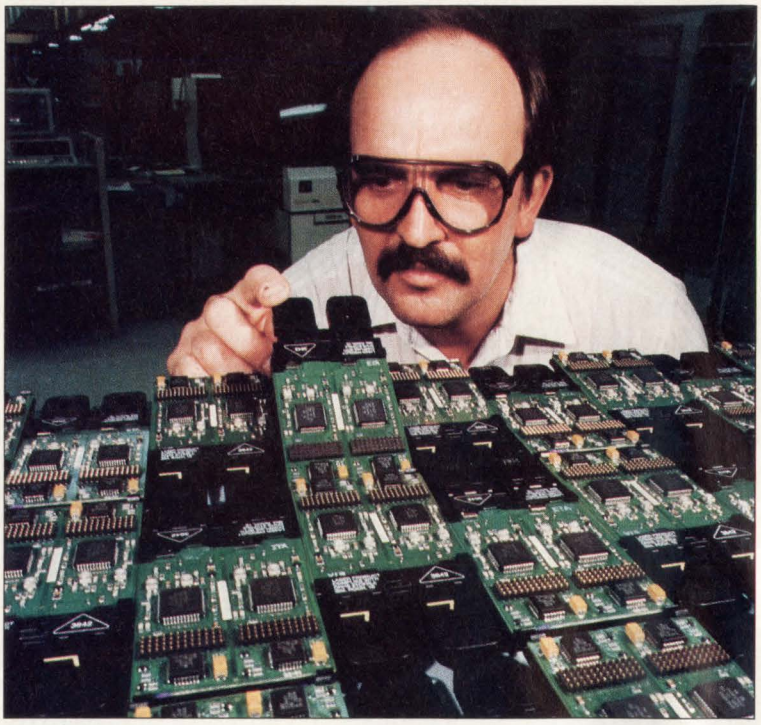
Fiber Channel has already been four years in the definition, "but we hope," says IBM's Sibley, "that the definition will be completed by year's end, with the emergence of products early next year." It doesn't look as if many will wait for the finalization of the specification to start developing products, however. IBM and Hewlett-Packard have already developed and are marketing an OEM Fiber Channel board, and it's been reported that both companies will be offering the board with a computer bus interface in the immediate future.

Robert Nunn, marketing director at Vitesse Semiconductor (Camarillo, CA), reports that his company, working with two partners (Interphase and Seagate), will soon announce a major Fiber Channel effort, including the definition of a Vitesse-developed GaAs chip set. Nunn, like Sibley, doesn't compare Fiber Channel to a telecom approach such as Sonet (Synchronous Optical Network), but he does rule out using its definition as a high-performance network interconnection scheme.

Douglas Felder, vice-president at Chi Systems (Pleasanton, CA), takes the same view. While Chi is currently working on HiPPI-based interfaces, Felder believes this will be a subset of Fiber Channel as soon as the technology reaches the level that chip sets are available. He says that Chi is presently working on interfacing Sun, Silicon Graphics and other workstation platforms, as well as high-performance storage systems, into what he calls a "HiPPI network."

Going HiPPI

The prototype of this network, according to Felder, is being developed at Lawrence Livermore Laboratories (Livermore, CA), with a number of companies participating. The consortium of companies, known as National Storage Labs, includes IBM Federal Systems, IBM Storage Systems and Network Systems, in addition to a number of workstation makers. The companies are providing materials and expertise to tie together a high-performance network test bed. The software tying the network together is being developed by General Atomics' Unitree division.



IBM and Hewlett-Packard have gotten together to develop a family of OEM Fiber Channel products designed to serve everything from desktop PCs to high-performance workstations. At the heart of the companies' approach is IBM's laser technology; IBM's been able to use relatively low-cost lasers such as those found in compact disc players in high-speed networks. Here an IBM researcher examines a Fiber Channel board.

The objective of the consortium is to demonstrate that it's possible to transfer data at HiPPI rates. "Until now," says Felder, "the only standard that's been available is FDDI, which limits transfer rates to 10 to 12 Mbytes/s. With HiPPI we've been able to demonstrate rates of 100 Mbytes/s." Existing systems are using conventional parallel HiPPI schemes with copper cables; however, fiber-based HiPPI is already in the wings.

"HiPPI," says Felder, "is here now, and we have many systems in the field and working. Fiber Channel started out as a relatively simple fiber option to the HiPPI hard-wire, but the option grew as those defining the specification kept adding feature after feature. It got to the point where it is now well defined, and a viable option, but it's still at least two years away."

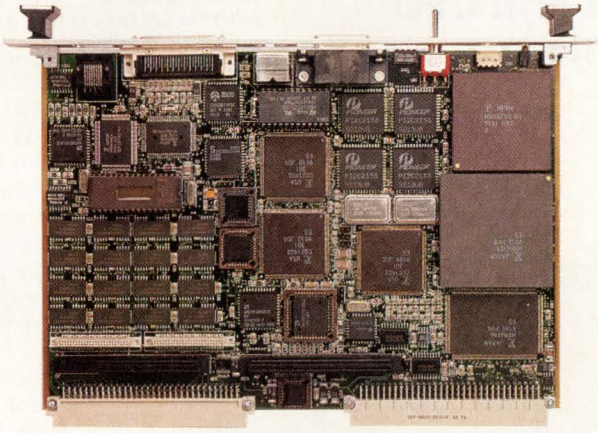
Fiber Channel, according to Sibley, has also been defined to include different rates, from the lowest of 133 Mbits/s, doubling through 266, 531 and on up to 1.062 Gbits/s, the fastest rate currently specified. "The decision to layer Fiber Channel into the four segments," Sibley adds, "lets users looking at different implementations adapt the standard to their specific needs." Those using SCSI, for example, may not need the higher data rate, and will not be forced into a more expensive solution than they need. If HiPPI has to be accommodated, the faster transfer speed will be needed.

In addition, the different rates let different technologies provide the most efficient operation, given some combination of data rates and distance. The Fiber Channel standard makes provision for lower-speed copper interconnection, as well as for multi- and single-mode fiber. The ideal solution is some "mix-and-match" combination of speed, medium and distance to provide the most economical result.

And it looks as if Fiber Channel is becoming very affordable. Prices for fiberoptic transducers have come down significantly, says Sibley, thanks to IBM's pioneering use of the same laser technology developed for commercial compact disc players in fiberoptic transducers. This has lowered the cost of a node from close to $1,000 to only a few hundred dollars. "And costs will continue to drop as volume picks up," says Sibley.

IBM's first OEM board-level product will sell in the $300 to $400 range in low quantities. The board

Seven Hot Reasons Why Your Next SBC Should Be a SPARC® 2SE



1 First

Our new SPARC® 2SE and 2LC are the first and only VME SBCs with SPARCstation 2™ performance. The SPARC® 2SE has complete Sun compatibilty on-board to put your workstation software to work in demanding real-world target applications like robotics and voice recognition systems.

2 040 x 2 =28.5

With 28.5 Mips of integer performance, the 40 MHz SPARC MPU is more than twice as fast as the 68040. A larger 64Kbyte cache and combined MPU/FPU put the SPARC® 2SE in a class of its own.

3 SPARC 100% Pure SunOS

We're partnered with SunSoft, a division of Sun Microsystems and developer of Solaris, Sun's newest operating system. So we guarantee full SunOS compatibility including: SunOS 4.1.1 Open Look, Open Windows, and ONC/NFS. All Sun application software and development tools run on a SPARC® SBC without modification.

4 64/32 64-Bit Architecture

Themis' SPARC® SBCs are the only SPARC VME SBCs built on the MBus, Sun's sophisticated 64-bit local bus. Used in the SPARCserver 600 MP Series, the MBus offers 64-bit paths to internal devices and memory for *fast* system throughput. Advanced ASICs designed specifically for the MBus guarantee performance and reliability.

5 Fully Loaded

The SPARC® SBC is a complete system on a card. Everything's on-board, including: 8-32 Mbytes DRAM, Ethernet, SCSI, VME interface, Open Boot PROM, Non-volatile SRAM and two Serial Channels. Its MBus/ VMEbus Controller has data FIFOs and hardware DMA for blazing VME performance.

6 Real Time Choices

Choose between LynxOS, VxWorks and VADSworks to cover any real-time requirement. Wind River's VxWorks is the standard for embedded real-time applications. VADSworks speaks ADA. Or use LynxOS for a POSIX or UNIX compliant kernel in the target system. Any way you choose, Themis has the software for your real-time environment.

7 The Future

The 2LC and 2SE are just the beginning. Themis is producing an entire family of SPARC 2-based products for every embedded application. Including high performance and low-cost SBCs. For more information contact Themis Computer, the sole source for VME SPARCstation 2 performance.

THEMIS COMPUTER

THEMIS COMPUTER-Americas and Pacific Rim
6681 Owens Drive, Pleasanton, CA 94588
Phone (510) 734-0870, Fax (510) 734-0873

THEMIS COMPUTER-Rest of World
1, Rue Des Essarts, Z.I. De Mayencin,
38610 Gieres, France
Phone 33 76 59 60 61, Fax 33 76 63 00 30

CIRCLE NO. 47

measures 1.5 × 4.5 in., and provides a full "byte-to-light" interface at transmission rates of 266 Mbits/s. It includes the optical link, encoder, clock recovery unit, and laser safety circuitry. "We expect these prices to drop to below the $100 mark by mid-decade [1995]," says Sibley. Of course, he adds, the price level will depend on distance and performance parameters. He expects to be offering a faster version of the unit soon, but he wouldn't commit to a firm timetable.

Sibley anticipates that even when the Fiber Channel rate reaches the Gbit/s range, interface circuitry will still be in silicon, as are IBM's existing chips. "We don't see the need for GaAs interface technology for at least the next generation or so," says Sibley. He claims that conventional silicon is more reliable and less expensive.

Sibley adds that IBM is also looking at copper approaches, but has not yet determined if they'd be practical. "We're looking at maintaining a very low bit error rate, in the range of 10^{-12} to 10^{-15}, and presently we don't see being able to maintain that level at the kind of data rates we're looking for."

At the higher transfer rates, factors other than simple interface IC fabrication can be strong considerations. One of these factors is receiver technology. As rates increase, the receiver becomes more difficult to build. "Hewlett-Packard has a lot of expertise in receiver technology, and that's one of the reasons we decided to team up with it in this Fiber Channel project," explains Sibley. Other factors in high-performance Fiber Channel systems are manufacturing technology and overall optical approach.

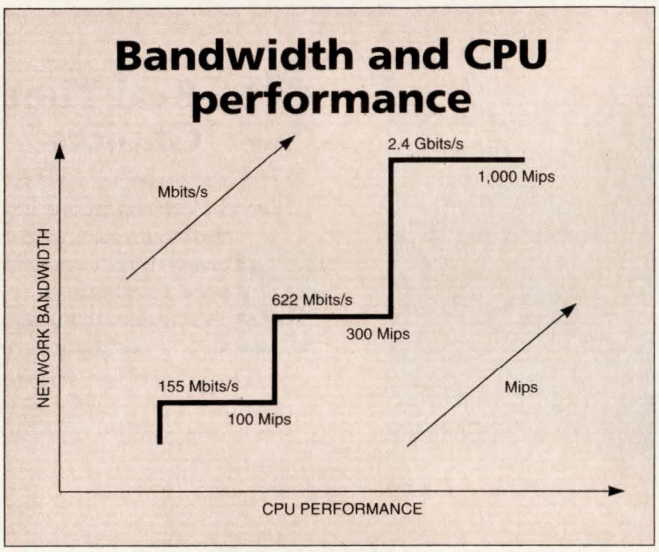
Not a network?

Though Sibley and some others are quite adamant that Fiber Channel isn't a network approach, others such as Felder aren't so sure. Felder even refers to some HiPPI implementations—as well as migrations to Fiber Channel—as networks. Although FDDI doesn't fit into the traditional topology of a network in terms of providing a ring or daisy-chain structure, network characteristics can easily be accommodated through high-speed switches and routers.

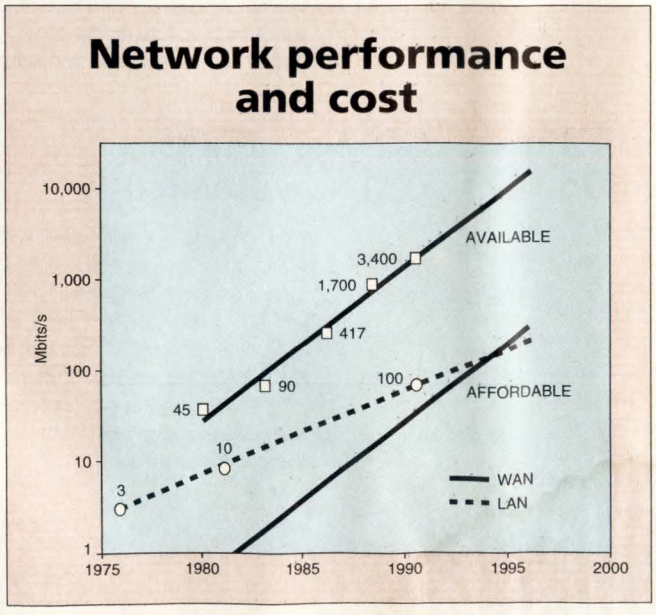
Sibley believes that the cost of various communications schemes will come down to a point where both a high-performance peripheral interface (such as Fiber Channel) and a high-performance network can coexist. Such a system could conceivably implement a Fiber Channel link to a high-performance disk array, and an FDDI or ATM connection to a LAN or WAN.

While this scenario may make some sense theoretically—just as a SCSI channel may coexist with Ethernet—it may not be practical to have a pair of Gbit/s channels going on and off the desktop. Such a system could require two special switches, one to network the disk array, the other to handle local area or global networks. Special bridges might also be required between the network and peripheral interfaces.

On the other hand, the scenario may not be so outrageous when one considers the type of work being done at National Storage Labs, where multiple computers—workstations as well as supercomputers—are tied into large, shared-storage subsystems such as disk arrays. A HiPPI or Fiber Channel interface could handle accesses to the storage facilities, a different network interface would handle interfaces within nodes in a system, and yet a third interface—to either individual machines or network concentrators—might handle the interface to wider area networks.



Higher-bandwidth communications schemes are required to handle increasingly fast processors. ATM offers scalable bandwidth for the faster approaches, with scalar jumps from 155 Mbits/s to 2.5 Gbits/s.



There's presently a gap between LAN and WAN performance and affordability. WAN capabilities such as those provided by Sonet are available, but not in a cost-per-node range to make them at all practical. LANs are not growing as rapidly in speed as are WANs, but they'll approach affordability in the near future. The ATM proposal would provide a middle ground to bring telecom-type technology into a reasonably economic range.

"It just makes a lot of sense to me," says Bill Kehret, president of Themis Computer (Pleasanton, CA), "if a single interface could be developed to handle all three situations." While it's not clear that a single interface can meet all the needs of a high-speed, point-to-point link such as Fiber Channel, as well as provide the flexibility of a WAN or LAN, at least the second two requirements can be satisfied.

Enter ATM

On one hand, those firmly behind FDDI are looking to increase the flexibility of the interface, adding a structure that will make it compatible with telecommunications systems. On the other, the ATM group is working to define a separate subset of the broadband ISDN (Integrated Services Digital Network) specification. "And, if it could also include a subset of the Bellcore-developed Sonet scheme, it would automatically provide a seamless connection between both local and wide area networks," says Sammartino.

Asynchronous Transfer Mode refers to the way packets are formatted and switched through a network, but it doesn't necessarily specify the physical layer or explain how the information is transmitted on the wire. In broadband ISDN, ATM and Sonet are coupled, but in LANs, they won't necessarily share the same transmission technology.

"But," adds Sammartino emphatically, "I'm a firm believer—and Sun is also—that if a solution could emerge that is a subset of Sonet for the local area, it would greatly simplify the entire issue." The trick, he says, is to find a subset that is fully compatible with, yet inexpensive enough for, a local area network. This will undoubtedly involve the development of a compatible chip set. Today, Sonet costs $1,000 a node, which wouldn't be a practical desktop solution.

"We're still in the early definition stages of ATM," says Sammartino, "so there really isn't any quantity of products available. Though there are a handful of parts available, we consider them generation zero." He believes real ATM devices, including both standard boards such as SBus boards and chips, will be available during 1993. At least one SBus ATM board is reportedly available from Fore Systems (Pittsburgh, PA), which is also readying an ATM switch for the market. Micro Pacific Research (Vancouver, British Columbia) also already offers an ATM switch. And a recent survey showed that several other firms plan to offer ATM hardware during 1993.

"The heart of this approach is the ATM packet specification, which defines 53-byte cells," says Kehret. "The size of the cell is small enough so there is virtually no latency in a packet transmission, yet large enough to allow it to be scaled up to and beyond the Gbit/s range."

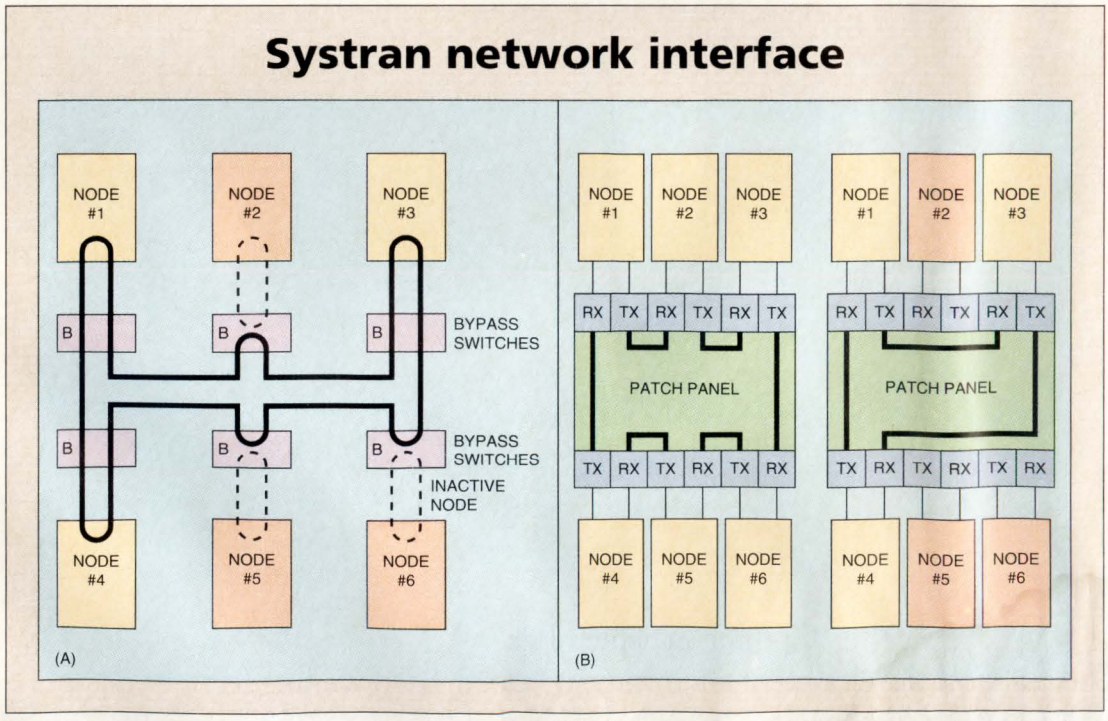
The ATM group is looking at the basic Sonet rates for incorporation into both a WAN and a LAN. These rates have thus far been defined as:

- OC-1 51.840 Mbits/s
- OC-3 155.520 Mbits/s
- OC-9 466.560 Mbits/s
- OC-12 622.080 Mbits/s
- OC-24 933.120 Mbits/s
- OC-36 1866.240 Mbits/s
- OC-48 2488.320 Mbits/s

**OC stands for Optical Carrier*

The hierarchy permits values going up to OC-240, which would top 12 Gbits/s, but that ceiling is still under consideration.

"Some of the first implementations we'll see," says Kehret, "will be based on the OC-3 and OC-12 rates, to take advantage of existing interface and cabling technology, as well as to be consistent with readily available telecom interfaces." What Kehret envisions is a totally transparent WAN/LAN, such that work-



One of the potential shortcomings of some ring network approaches, such as Systran's ScramNet, is the mishandling of a node failure. Systran adds flexibility to its network approach by providing two ways to handle such situations. In one (a), nodes can be eliminated with bypass switches; in the diagram, nodes 2, 5 and 6 are bypassed. In the other method (b), patch panels can handle the chore. On the left, nodes are operational; on the right, the same nodes—2, 5 and 6—are bypassed.

You Can Try Building Your Own Real-Time Operating System,

Building your own operating system for a real-time application can cost you up to a year in expensive programming time. And lost business opportunities. In a fast-moving market, it simply doesn't make sense to build. Not when VxWorks™ from Wind River Systems lets you move right in.

VxWorks gives you all the components and tools you need to start developing applications immediately. Which cuts your costs dramatically. And because VxWorks offers a more full-featured development platform than any other off-the-shelf operating system, it gets your product to market faster. It's the one true turn-key solution, fully compatible with industry standards right out of the box.

Hosts	Targets
Sun	68K
HP	SPARC
DEC	MIPS
IBM	i960

VxWorks supports multiple platforms.

Or You Can Feel Right At Home With VxWorks.

Wind River Systems pioneered off-the-shelf high-speed UNIX® networking for real-time applications. And VxWorks still leads with the most complete, robust networking available. The lean, efficient **wind**™ kernel gives it unsurpassed multitasking speed and functionality.

So before you invest the time and money trying to build your own real-time operating system from the ground up, find out more about VxWorks. And feel right at home from day one. 1-800-677-1586.

WIND RIVER SYSTEMS

Real-Time Solutions for The Real World

CIRCLE NO. 51

stations could plug right into a high-speed network and have a seamless connection to other machines in the same room or building, as well as with any on the same network, anywhere in the world.

The ATM approach has a strong following at Apple, Digital, Sun, and others, though much of the progress to date is kept tightly under wraps. Even the ATM chip consortium is very secretive about energing developments. But the group has apparently inked a timetable and plans to have products as early as 1993, while large-scale introductions won't be seen until 1995.

Sonet technology is currently in use by major telecommunications companies, but as a broadband interface it doesn't sell in enough volume to bring the price down. "And," says Sammartino, "the bulk of implementations for the first several years will undoubtedly be based on copper-wire transmission, at the OC-12 rate." He believes there will be no problem stretching the 125-Mbit/s line rate of FDDI to the 155-Mbit/s rate of ATM OC-12.

Hedging a bet

The need for more flexibility, particularly as multimedia becomes a reality, is becoming a major concern for network managers. This problem is being addressed aggressively by the FDDI group, which includes many of the same participant companies as the FDDI, HiPPI and ATM groups.

Second-generation FDDI provides upward compatibility from the first generation, but adds circuit-switched service to FDDI's existing packet-data service. The new service is intended to support isochronous data—data which must be delivered in regular amounts at uniform time intervals. A major advantage of an isochronous LAN is the ease with which it can be connected to WANs, making it attractive for such applications as desktop video conferencing. Isochronous data structure mates well with the cell-based approach of wide-area communications—essentially ATM.

But FDDI-2 uses the same 100-Mbit/s bandwidth as its predecessor, FDDI. The basic service also shares its ring-and-packet service with the isochronous service in the second-generation specification. At present, there's no FDDI transmission-rate hierarchy established, and many considering the approach feel that it may not provide the expandability needed for future generations of processors.

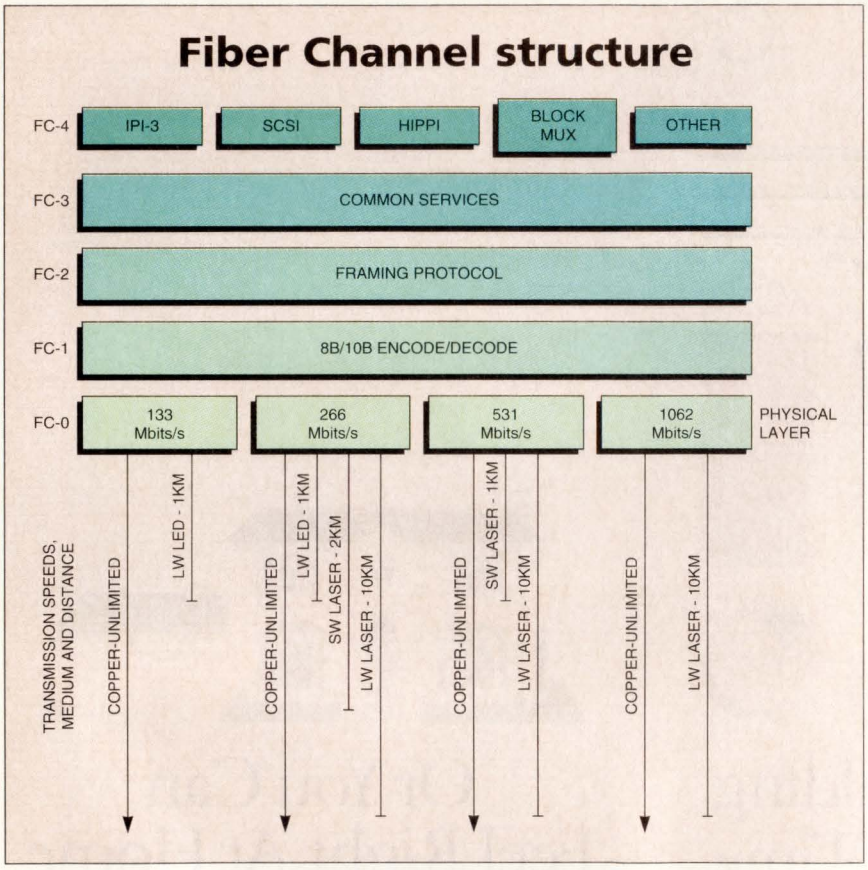
"There is always a bottleneck in network approaches," says Sammartino, "and the only way to solve the problem will be to add bandwidth." He explains that the useful life of a typical Ethernet system has been greatly expanded through clever organization of the network's topology. Using switched networks and hub concentrators, instead of conventional multiuser drop approaches, it's possible to increase the effective bandwidth of standard Ethernet. This approach in essence gives each user their own bandwidth through a direct connection to a hub rather than sharing the bandwidth with other users on a single line.

"But," Sammartino continues, "the problem is that when these are installed in a real environment, usually something like a client-server environment, the advantage erodes. It frequently happens that while the added per-user bandwidth lets users look essentially at an empty network, the server (or wide-area network or other facility) will be loaded up and unavailable. An escape—a higher-bandwidth connection—is always needed to go to a server or routers or wide area network."

With networks such as FDDI, there will always be a bottleneck of some kind or other. "Because of ATM's scalable approach," concludes Sammartino, there's always a next step up—a faster but seamless interface—to handle the higher-speed server or wide-area network requirements."

Networks for real time

The next generation of network interfaces is anything but "conventional," but it can't always handle the needs of some specialized, high-performance, real-time systems. Applications such as large simulators



Fiber Channel has been defined with five protocol layers, F0 through F4, the latter being the I/O channel analog to the ISO/OSI network layers. The physical layer (F0) has been defined in four speed ranges, from 133 Mbits/s to 1.062 Gbits/s. Transmission medium technologies appropriate to each, along with maximum transmission distances, are indicated below the physical layer.

If You Haven't Been To BUSCON Lately, Take A Look At What You're Missing.

BUSCON/92-EAST[SM]
SEPTEMBER 15-17,1992
HYNES CONVENTION CENTER
BOSTON, MASSACHUSETTS

Over the years, BUSCON has established itself as the industry's leading forum for boards, embedded software and other elements of systems architecture.

But BUSCON is more than boards. It's a comprehensive source of information for designers in the electronic OEM. If your applications require custom design or off the shelf technology, BUSCON is the one place to satisfy all your design needs.

Meet industry leading vendors who can help solve your design problems.

See the latest products and technology. Many important new developments are introduced at BUSCON

Learn from the experts who pioneered the technology at the industry's leading technical conference coordinated by Computer Design Magazine

Save time, save effort, save money– You can cover more ground at BUSCON in one day than any other source of industry information

Please Send Me Attendee Information for BUSCON '92 East

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

PHONE _____

Return to:
CMC,
200 Connecticut Avenue,
Norwalk, CT 06856
Phone: (800) 243-3238, in Connecticut (203) 852-0500
Fax: (203) 857-4075

BE3

It's all happening at **BUSCON '92 East, September 15-17, 1992 at Boston's Hynes Convention Center**. For more information call (800) 243-3238, (203) 852-0500 or fax (203) 857-4075, or return this coupon.

CIRCLE NO. 48

Proprietary solutions fill gaps left by standard networks

At least one major workstation manufacturer is fond of saying "The network is the computer," but today's users are apt to retort, "Yes, and the network is too slow!" In simple terms, both workstations and open-architecture real-time systems are evolving much faster than the standard network products intended to interconnect them.

For example, it's taken our industry about 10 years to progress from Ethernet to FDDI, a change representing about a twelvefold increase in speed. In the same 10-year period, system throughput demands have probably increased by a factor of 40 or more—since bus widths have quadrupled (from 16 to 64 bits) and CPU clock speeds have increased by a factor of 10 or more. The challenge is to provide connectivity solutions which can keep up with the systems they serve.

One response to this problem has been to replace or augment traditional peripheral buses (for example, SCSI), LANs (for instance, Ethernet) and serial-based connections with new, standardized, high-speed networks and network technologies. Some examples of this approach include FDDI, Fiber Channel, SCSI-2, and Sonet. These new networks and media systems offer the expected benefits of standardization, and provide significant performance gains over their predecessors. Even so, once you take into account the operating system overhead needed to manage network protocols, there remains a sizable gap between available network speeds as compared to present system connectivity needs.

Meeting the need for speed

A second response has been to create fast, low-overhead, proprietary data-transfer systems capable of exceptionally high data-transfer rates. Proprietary systems can do a good job of improving system-to-system data-transfer rates, subject to specific design trade-offs. Proprietary systems are differentiated in terms of the size of data transfer for which they are optimized, the data-delivery mechanisms they provide, the transmission media used, network configurations, and protocol structures (if any). Let's examine each of these differentiating factors:

•**Transfer size optimization**: Some systems perform well when transferring small messages, but tend to have lower absolute speeds when performing large transfers. Other systems are tuned to handle large block transfers with very high absolute speeds, but prove less efficient when handling smaller control-oriented messages.

•**Data-delivery mechanisms**: Some transfer systems (especially reflective memory systems) transfer data from the source to "bulletin boards" in the destination chassis. Typically, the data receiver either polls the bulletin board to look for incoming data, or is interrupted by the bulletin board when a message arrives. An advantage of the bulletin board approach is simplicity; in many cases, a simple data write is all that's needed to initiate a transfer. Other transfer systems follow a DMA transfer model, where the transfer initiator writes a small data structure which defines all aspects of the desired transfer. Once started, the transfer pulls a specific amount of data from a specific source, and delivers the data to a specific destination address in one or more remote chassis. An advantage of the DMA transfer approach is specificity and low overhead: once the transfer's described, data is moved to the precise destination address with no further intervention from the participating systems. Some, though not all, systems provide a synchronized broadcast mode which lets you transmit to multiple receivers at once.

•**Transmission media**: Although some wireless/cableless systems are available, most proprietary systems use either wire-based or fiber-based interconnects. Wire systems have the advantages of speed, ease of configuration and low cost, but they also have the limitation of relatively short interconnect runs. Fiber systems offer the advantages of very good speed and distance capabilities, but they come at relatively higher costs.

•**Configurations**: The simplest proprietary systems provide point-to-point system connections. Multisystem configurations include ring, star and linear multidrop topologies.

•**Protocols**: In some systems, data is transferred in a protocol "wrapper," with wrapper size varying from system to system. In evaluating systems using such wrappers, it's important to realize that the wrapper consumes some portion of the available transfer bandwidth. Typically, the fastest systems make every effort to minimize (or eliminate) this un-

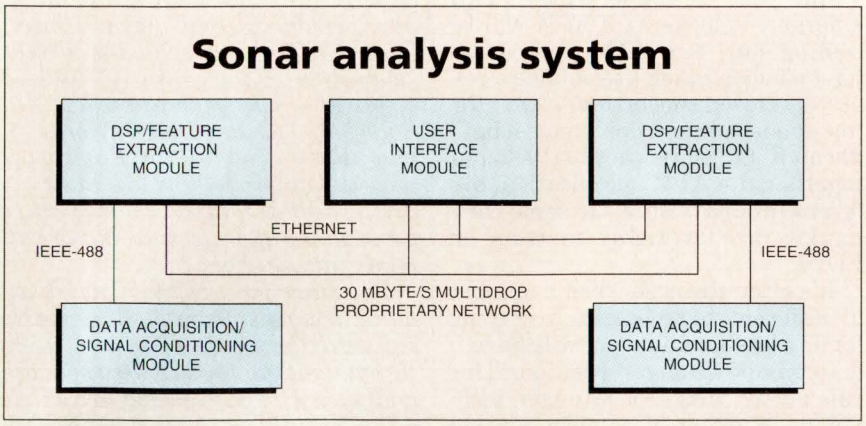
R. Chris Martens, director of marketing, Ironics, Ithaca, NY

with literally hundreds of different processors call for special communications systems. In response, a number of different approaches have emerged which bypass the traditional network and, in some way or other, let the memory of one computer talk directly to that of another.

This communication can be in the form of a common memory shared by two machines, such as Systran's ScramNet, or it can be a direct memory transfer—essentially a remote DMA—such as Ironics uses in its approach. Both approaches offer different advantages and are usually tailored to specialized applications.

Systran's ScramNet is a replicated, shared-memory network with a 150-Mbit/s data rate. The network communicates over a fiberoptic cable and is designed to update any system's ScramNet memory, from 128 kbytes to two Mbytes in size. "By providing a direct memory-to-memory transfer," says Tom Bohman, Systran's ScramNet product manager, "we're able to transfer information directly, without software protocols. Unlike FDDI or other approaches, ScramNet lets an application program in one computer communicate its data directly to an application in another computer in only a few microseconds. The network is designed for real-time systems where throughput isn't the only factor, but the age of the data is also a critical parameter."

The interface control document for ScramNet is a memory map, says Bohman. Since every computer is



wanted source of overhead.

Proprietary data-transfer systems can provide real speed advantages compared to traditional networks, especially when they're carefully matched to exact transfer requirements of the systems to be linked. Proprietary systems, however, are not a panacea and should not be regarded as outright replacements for traditional networks. For now, the cost of speed almost always entails a move away from the conventional seven-layer Open Systems Interconnect (OSI) network model.

Subdivide and conquer

Instead of viewing traditional networks and proprietary systems as an "either/or" proposition, one powerful approach is to distribute connectivity loads across both traditional networks and proprietary channels. A good strategy is to use traditional networks as a command and control channel, passing small messages at moderate speeds, while using proprietary systems as independent bulk data channels, blasting large blocks of data between systems at high speeds. In this way, proprietary channels augment, but do not replace, traditional networks, and each channel is used to service the types of transfers for which it is best suited. In typical applications, traditional network links serve as a common resource linking all chassis or nodes in the system, while nonstandard channels are used to link system elements which demand hard real-time data transfers.

The figure shows a block diagram of a sophisticated Sonar analysis system. The installation employs a combination of traditional and proprietary data channels. The system has five main elements: two separate data-acquisition/signal-conditioning modules (one for each main Sonar array), two separate DSP/feature-extraction modules (one serving each associated data-acquisition module) and one user interface module (synthesizing output from each of the two DSP feature-extraction systems).

Each data-acquisition module feeds preconditioned input data to its associated DSP/feature-extraction module via an IEEE-488 link. Both DSP/feature-extraction modules are linked to each other, and to the central user interface module, via two quite different kinds of networks. A conventional Ethernet link lets the user interface module pass command and control signals to either or both DSP/feature-extraction modules, and also lets messages pass between the DSP/feature-extraction modules. For fast bulk data transfers, such as are needed as Sonar array displays are updated or compared, a very high-speed (30+ Mbytes/s) proprietary multidrop network is provided. In this scheme, traditional and proprietary networks play mutually supportive roles and succeed, where a purely traditional or proprietary solution would not.

In an ideal world, traditional networks would be reasonably priced, easy to install and to use, and faster than the systems they connect. Until we reach that ideal, however, combinations of traditional data links and fast proprietary networks will provide the best blend of standardization, user-friendliness and high performance—at price points which make sense.

getting a local copy of the physical memory space, software engineers running the application simply need a map to describe where the data is located, where it's coming from and what format it's in.

"ScramNet is really the network alternative to a physical shared memory," continues Bohman. "It has the same data-link and immediate data-sharing characteristics as physical shared memory."

Computer Sciences Corporation's Universal Memory Network (UMN) takes an approach similar to Systran's. The company claims its technology provides near-simultaneous access by all devices on the network to data designated as common or shared. The reflective memory scheme is almost a subset of Systran's approach, but provides a semaphore capability to let devices exchange control information over the network. UMN operates at a rate of 40 Mbytes/s.

Even when such standard networking protocols as these are eliminated, data still may not get to a critical processing node and be acted on fast enough. "In these applications," says Tom Rich, vice-president of engineering for Ironics, "conventional LANs have to be augmented with a high-speed data-blasting channel."

Rich comments that some approaches have tried to use conventional networking technology but run into problems on two fronts: first, the bandwidth is too low, and second, host-processor intervention

is required to act on received data. "Even with specialized real-time networks, the processor still has to go out and look for the particular address location of transferred data," he adds.

To eliminate these problems, Rich says that Ironics uses a DMA model to eliminate latency—the receiving processor's memory itself is updated, so it doesn't have to go out and look for updated information. Ironics' MCPL approach uses a full 32-bit-wide datapath capable of saturating a VMEbus. Rich also hinted that a next-generation data pump utilizing a 64-bit architecture and providing full concurrent transmission and reception in an ASIC chip set will soon be in the offing.

What's really needed is to go into a type of network structure that is scalable, so it not only solves today's problems but has a plan for the future.

—Fred Sammartino, Sun Microsystems

■ ■ ■

The future beckons

Planning activity in the advanced network arena is reaching a fever pitch, yet solutions appear to be painfully slow in coming. FDDI, for example, has been under development for a decade—and it appears to be suffering from a bit of a backlash. Ethernet, though closing in on a 20-year tenure, has sold more in the past two years than in the previous 18. While no one has explained exactly why this is so, it has to be due in part to the fact that simple, twisted-pair solutions have come down into the mass-market price range. But certainly another factor is that customers have been waiting for a next generation that just hasn't emerged. For some, the wait may have been too long.

Although FDDI is here now, as Radstone's Silverman points out, it still has some hurdles to clear. Because the copper interface hasn't yet been defined, the only real solutions are fiberoptic. And the infrastructure for fiber just isn't here yet. In addition, it's an expensive solution—not just for the transducer components, but for the connectors, assembly and other factors involved in working in a new medium.

And just as copper-based FDDI emerges, it looks as if ATM will be coming out, too. ATM approaches haven't seen much use outside a relatively closed consortium—even the telephone carriers don't have a handle on it. So, while they battle to put together the ATM specification, different groups within the same companies are feverishly working on FDDI.

It's often the case when a number of different technologies are vying for leadership that one will have a discernibly stronger position. This can be by virtue of stronger technology, backing of a major market player to the exclusion of others, or acceptance by a major application area. None of these factors are in place and, in fact, trends are made even more confusing by companies heatedly pursuing multiple choices.

No clear winner will emerge in the next year or so, but what at one time appeared to be a clear field for FDDI may now be somewhat cluttered. The ATM approach espoused by the consortium makes a lot of sense, provided it can be practically implemented. And if it can also be tied in as a full subset of Sonet, it would clear the way for a network from desk to desk. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Chi Systems (510) 463-2513	Circle 230
Computer Sciences Corp (805) 736-1275	Circle 231
Fore Systems (412) 422-5944	Circle 232
IBM (507) 253-1517	Circle 233
Ironics Corp (607) 277-4060	Circle 234
Micro Pacific Research (604) 293-5403	Circle 235
Radstone Technology (201) 391-2700	Circle 236
Sun Microsystems (415) 960-1300	Circle 237
Systran Corp (513) 252-5601	Circle 238
Themis Computer (510) 734-0870	Circle 239
Vitesse Semiconductor (805) 388-3700	Circle 240

Postscript

Network interfaces are suffering from the same turmoil that's affecting other standards, including bus, peripheral and memory interfaces. The problem is that the current generation of interfaces is obsolete, before the next generation has hit. Solutions such as FDDI—an order of magnitude faster than Ethernet—were thought to be able to handle the anticipated traffic from future generations of processors, but are already falling short.

The other facet of the network dilemma comes from LANs. LANs satisfied the needs of system users throughout the 1980s where network nodes were largely located in a single office or building. Now though, with the expansion of services available and the global approach to business, it's critical to have access across the globe as fast as across the room. Current networking approaches are falling pitifully short.

There may well be a single solution to both the problem of a faster, scalable technology as well as one which will cope with the seamless integration of local and wide area networks. This sincle solution could be the approach taking advantage of a subset of the ISDN specification. ATM as a network interface is just beginning to emerge. If the specification settles out as expected, it will supply a full subset of both ISDN and Sonet.

Though there are no "ideal" solutions, ATM solves a lot of problems with a single approach. Fixes to FDDI such as FDDI2, are just that, fixes or Band-aids which only temporarily solve the problem.

Warren Andrews

COMPUTER DESIGN AND PENNWELL WELCOME A NEW PARTNER

Military&Aerospace ELECTRONICS

A PennWell Publication

Now, *Computer Design Magazine* and PennWell Publishing can help you meet your military/ aerospace requirements with one unique, dedicated, concentrated publication — *Military & Aerospace Electronics.*

Military & Aerospace Electronics is a colorful, tabloid size, monthly magazine serving the unique informational requirements of today's military/aerospace engineers and engineering managers.

In only two years, it has grown to a position of high visibility, strong identity and important readership with 46,000 BPA qualified subscribers at DoD/NASA/prime contractors, manufacturers of systems/subsystems and other OEMs — 96% of whom have Design/Buy/Specify authority.

Now, *Military & Aerospace Electronics* and *Computer Design* are partners within PennWell Publishing's Advanced Technology Group providing a strong editorial and circulation platform.

It takes this kind of organization to understand, cover and service the growing technology opportunities within the turbulent Military/Aerospace marketplace.

Come join us, the ever stronger *Military & Aerospace Electronics* in partnership with *Computer Design Magazine.*

PENNWELL PUBLISHING COMPANY ADVANCED TECHNOLOGY GROUP
ONE TECHNOLOGY PARK DRIVE, WESTFORD, MA 01886 508 692 0700 FAX 508 692 7780

Military&Aerospace ELECTRONICS

COLOR PUBLISHING • COMPUTER ARTIST • COMPUTER DESIGN • COMPUTER GRAPHICS WORLD • LASER FOCUS WORLD
• LIGHTWAVE • MICROLITHOGRAPHY WORLD • NETWORKING MANAGEMENT • SOLID STATE TECHNOLOGY • TYPEWORLD

CIRCLE NO. 49

NOW, IN THE TIME IT TAKES TO READ THIS AD, YOU CAN RECEIVE THE DATA SHEETS YOU NEED

COMPUTER DESIGN'S IDA 617 494 8338 INSTANT DATA ACCESS

INFORMATION YOU NEED ABOUT AN ADVERTISED PRODUCT CAN BE YOURS IN AN INSTANT BY FAX, ONLY FROM COMPUTER DESIGN!

LET "IDA" DO IT!

Just call IDA *Computer Design's* **"INSTANT DATA ACCESS."**

Get specs, pricing information, or the location of a local sales engineer or rep...by simply touching a few buttons.

If an ad in this issue of *Computer Design* includes an IDA **INSTANT DATA ACCESS** number, you don't have to wait to get the details you need to make critical design or purchasing decisions.

IT COULDN'T BE EASIER!

The next time you need product information in a hurry, just call IDA **(617) 494-8338** from a touch tone phone or a fax phone and follow the voice prompts.

IDA

JUST CALL:
(617) 494-8338
FROM EITHER A TOUCH TONE PHONE OR A FAX PHONE AND FOLLOW THE SIMPLE VOICE PROMPTS

IDA

This month, these participating advertisers have made information instantly available to you

advertiser	*document no.*
ATMEL	1045
Computer Design	1047
Hitachi	1034
KADAK	1036
Macrolink	1037
Mercury	1020
Synergy	1042

Still available from last month (through the end of next month):

advertiser	*document no.*
ATMEL	1050
Computer Design	1047
Force	1049
Hitachi	1034
Ironics	1046
KADAK	1036
SBE	1040

IT COULDN'T BE EASIER!

Using a fax phone...

1. Make note of the IDA document number you're interested in.
2. Pick up your fax phone and dial **(617) 494-8338.**
3. Follow the voice prompts.
4. Replace the handset in the cradle and the product data you requested will be faxed back to you without a break in your connection!

Using a touch tone phone...

1. Make note of the IDA document number you're interested in.
2. Pick up your phone and dial **(617) 494-8338.**
3. Follow the voice prompts.
4. Hang up the phone and the information you requested will be faxed back to you, right to the fax number you specify!

ONLY COMPUTER DESIGN GIVES YOU "IDA"—INSTANT DATA ACCESS — SO YOU CAN GET THE DETAILS YOU NEED INSTANTLY — BY FAX!

Delivering Today's Electronics OEM

COMPUTER DESIGN Technology and Design Directions

COMPUTER DESIGN• ONE TECHNOLOGY PARK DRIVE , WESTFORD, MA , 01886 • 508-692-0700 • FAX 508-692-7780

IDA INSTANT DATA ACCESS (IDA) DIAL (617) 494-8338 DOCUMENT NO. 1047

CIRCLE NO. 50

Video teleconferencing on British shores

The British Telecom design team: Front row, left to right: Steve Banthorpe, manager of aesthetics; Richard Gedge, overall manager; Shabir Azani, responsible for forward coding; Maurice Perini, responsible for parts of core coding loop in codec; Adam Guest, camera control system; Allister Kemp, microprocessor control system. Back row, left to right: John O'Donnell, video demultiplexer; David Norman, technical support; Peter Forty, head of codec development group; Stephen Jackson, channel interface; David Dolby, originator; Richard Whiting, technical support; Richard Incoll, technical support. Absent from the photo are: Tony Leaning, architectural design; Steve Barnes, audio system manager; Wesley Pretty, software development.

Designing a video teleconferencing system involves building bidirectional equipment that can capture and compress video and audio images from one location and transmit them to another, where the signals must be received, decompressed and reconstructed. This is no mean feat. A design team must have expertise in both video and audio technology, as well as in telecommunications equipment design.

In 1988, a team of engineers at British Telecom (Martelsham Heath, Ipswich, England) assembled to design the VC2100 video codec. Over the last two years, this equipment has been integrated into the VC5000 video teleconferencing system.

The electronics in a video teleconferencing system consist of a video and audio codec (coder/decoder unit) connected to an interface that links the codec to different telecommunications networks—this is the VC2100. In addition, a dedicated control system must be designed to provide the interface between the user and the VC2100 codec. This is the VC3200, or terminal management suite (TMS); it provides control for cameras, monitors, audio/picture switching, and user functions. Both these components make up the VC5000 videoconferencing system.

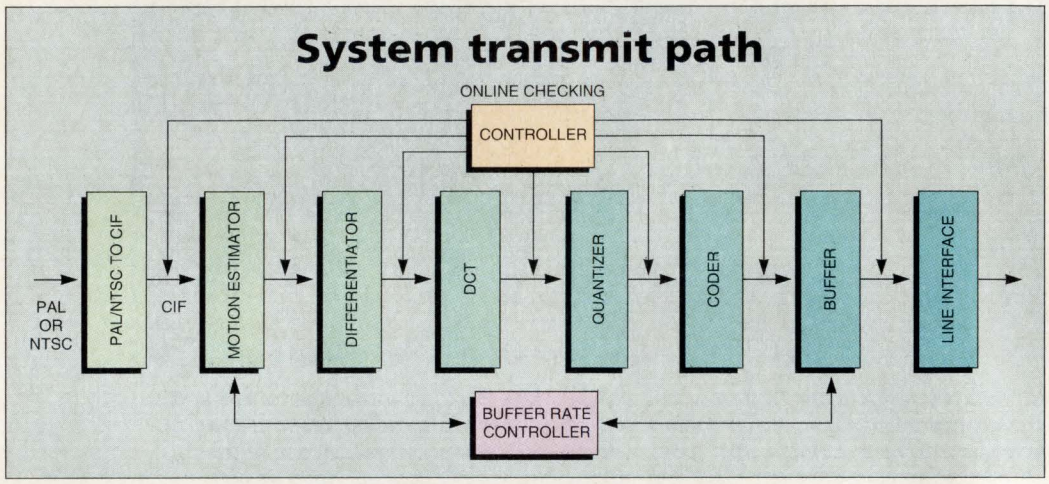
In operation, up to six video sources may be connected to the system. The TMS is used to provide the selected source for transmission to the VC2100. Up to three incoming, or previewed, pictures are shown to the user on the monitors.

The custom computer system in the VC5000 cabinet can be divided into two sections. In the bottom half of the cabinet is the TMS, which lets you control the teleconferencing environment—setting up the cabinet to match the dynamics of the room, selecting audio levels and switching video sources among the various monitors and cameras. In the top half of the cabinet, a second rack contains the video codec, audio codec and transmission-control electronics.

Dave Wilson, Senior Editor

According to Peter Forty, head of the codec development group, it was a conscious decision of the design team to separate the electronics control of the user's environment from the core video codec. That way, third-party codecs could be integrated into the unit if needed, while still providing the overall functionality that was required.

Both the video codec and the control section were designed around modular board components. The codec design is similar in dimension to triple-height VME cards that plug into a backplane bus, while the TMS resembles 3U VME. The British Telecom bus, however, is proprietary in nature. Many backplane bus signals are specifically used to route video signals around in real time; the speed of the bus is closely coupled to the coding algorithm used in the design. "In order not to compromise the reliability of the codec and get the throughput, it was necessary to design our own bus," says Forty.



This simplified diagram shows the key elements involved in the design of the British Telecom teleconferencing system transmit path. The hardest part of the design was the motion estimation processor that was built around eight custom Motorola ASICs.

Many standards, one system

According to Mike Carr, head of the video systems section, the company needed to bridge between two different line and picture rate standards—PAL (Phase Alternation Line) in England and NTSC (National Television System Committee) in the United States—before the codec could be developed. It's not cost-effective or practical to build custom PAL teleconferencing systems for the U.K. market that would be incompatible with custom NTSC solutions developed for the U.S.

The British Telecom solution was to develop yet another standard—CIF, or common intermediate format. Using it, any video teleconferencing system can capture video in either NTSC or PAL format, convert it to the CIF format, process the data in that format, and then output in either PAL or NTSC format.

To accommodate the CIF standard, the codec contains video input and output sections that convert the CIF format used for internal processing to the television standard of the country to which the equipment is being supplied. Because the system is modular in nature, individual units can be tailored to a specific country by adding or removing boards in a given format.

Motion compensation

By far the most complex part of any video teleconferencing system is the video codec, and the bulk of the codec is dedicated to video compression—the hardest task for any system to perform. In the British Telecom design, a group of seven cards is used for video compression, while an eighth converts the NTSC or PAL signals to the CIF format. The remaining five slots are used for two video inputs and up to three video outputs.

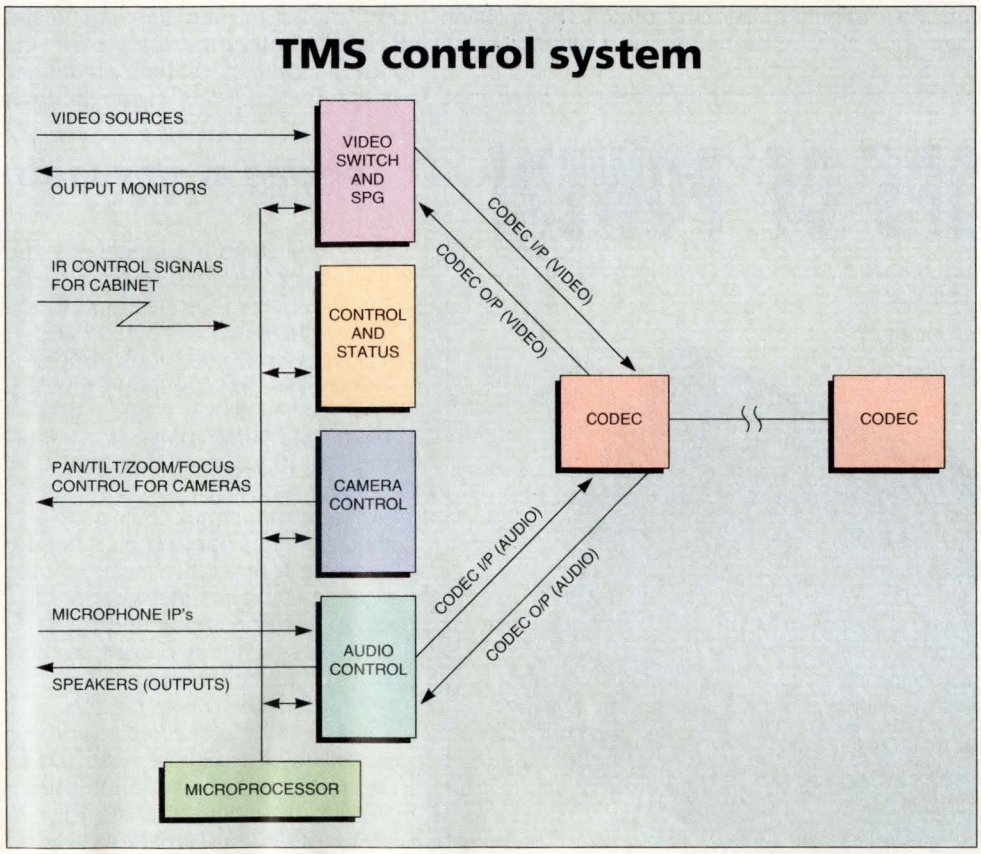
The central card of the video section is also the control card of the whole codec. It has two microprocessors on it: a Zilog Z80 and an Intel 80186. They supply the user and terminal interfaces. The central controller manages the data transmission rate from 2 Mbits/s to 64 kbits/s as well as controlling the video picture quality, at either full CIF or QCIF (quarter CIF) resolution. Also, the control card can change the audio/video mix—more compression can be applied to audio than video and vice versa. In addition, it can select a data port to which to send a fax or to bring terminal communication from one end of the system to the other.

The key component of the video compressor is the motion estimation board. Processing the data from the current and previous frames, then comparing the pictures and finding the best fit with a motion vector, is the most compute-intensive task of the whole Px64 compression algorithm, says Forty. "In the encoder, it is unnecessary to perform motion compensation, but in the decoder you must be able to accept motion-compensated data streams. You can trade off how you perform the motion estimation and compensation in the encoder," he adds.

Indeed, the H.261 standard lets you perform ±15 search windows and provide a vector to the line, but because it's so compute-intensive, different approaches can be used that are still compatible with the standard. "A lot of the proprietary chip sets that are becoming available now are based around ±7 search windows," says Forty. "That's not full search. We have implemented a full-search algorithm that compares every single one of the search positions of the previous data with the current data and arrives at the one position that gives the least energy for the search." On the British Telecom board, the motion estimation processor has been implemented in eight Motorola ASICs, with a ninth for memory control.

British Telecom decided on the Motorola parts when building the original demonstration vehicles for H.261. On the first demonstrator, each of the processors that computed one row of an 8 × 8 block of picture data was a single card of

TTL adders and multipliers. "To shrink that to a size that was cost-effective," says Forty, "each of those cards had to be one ASIC. We ended up with eight cards with eight ASICs on each card to perform motion compensation." For its part, the VC2100 represents the next level of integration: each of the eight-ASIC cards has become one ASIC. The ±15 frame search operation can be performed on a single board. In the next-generation design, the eight ASICs will be shrunk into two.



The complete BritishTelecom video teleconferencing system—the VC5000—comprises the VC2100 codec and the terminal management suite (TMS), or VC3200. The 3200 was developed separately from the 2100 and provides the user interface and control system for the cabinet, since a codec alone can't provide those functions. Shown here is a block diagram of the TMS.

FPGAs and ASICs

Throughout the design of the codec, British Telecom made heavy use of programmable devices, PROMs as well as PALs and Xilinx FPGAs. In that way, the design team was able to keep track of any changes in the H.261 compression standard, even while the hardware was being designed.

At the time the system was developed, the final H.261 specification hadn't been agreed upon. "The order in which the H.261 picture header information was sent to the line changed," according to Stephen Jackson, channel interface manager. "There were also changes to the DCT function." But using FPGAs helped. "Within an hour we could reconfigure those programmable devices to cater for every change we were called upon to make," he adds.

That, of course, necessitated partitioning the system architecture—deciding which functions were to be put into gate arrays and which were to go into FPGAs. "We were very conscious of which elements were constants, as well as which were variables," says Jackson. "In addition, we looked at which functions could provide us with a building block that could be used in other designs. We left those things that were subject to change in programmable form."

The Xilinx philosophy matched that of the British Telecom engineers. Forty says, "When developing hardware, we prefer to make a stab at what we want the function to be, and then debug that function in real time in the hardware rather than do a lot of simulation, attempting to get the thing right the first time. With video, the biggest aid to debugging is to see the video." Forty doubts whether a simulator that could simulate the operation of the design could have provided the turnaround time his team desired.

In addition to semicustom ICs and FPGAs, British Telecom worked with Inmos (Almondsbury, Bristol, England) to define the characteristics of a DCT chip. Although the DCT function itself is fixed, the final DCT specification isn't absolute. It lets you build DCTs with different internal rounding, truncation and accuracies, provided that they meet the overall accuracy required. The accuracy was specified so that, given the rate at which the video picture is updated, the two ends of a video teleconferencing system keep track of one another.

After motion compensation, a loop filter function is performed on the data. This is spatial filtering performed on each block to cut out noise. In addition to performing DCT and inverse DCT functions, the Inmos DCT chip was designed to perform this loop filter function as well.

After motion compensation and filtering, the data is passed to another board across the backplane bus, where a difference operation is performed on the new video in the current frame and the motion-compensated video in the previous frame. Then a DCT is performed, followed by quantization—a process that requires that the data be transformed from block to zig-zag format. Once quantized, the data is run-length encoded, then passed to another board that performs Huffman coding. Finally, data is passed to a buffer control and out to a line interface card.

British Telecom used a TMS320C15 from Texas Instruments (Dallas, TX) to perform the rate-control function inside the

codec. Deciding on the chip was easy. According to Forty, "The designer was familiar with the chip and it also had the amount of I/O that was required. It was fairly cheap, too."

In operation, the buffer containing the video and audio data provides status information to the TI rate-controller processor. It's obviously important to control the buffer, so that the rate at which the buffer is written into equals the rate at which data is taken out. Depending on the status of the buffer, the processor decides how to control the flow of data to it—whether or not to drop a frame, or whether to intercode or intracode the data.

The processor is also fed information from the motion compensation processor regarding the fit between the previous and current frames. The TI DSP chip makes the decision as to whether motion compensation is necessary or not. "If it's a really ropey fit," says Forty, "it probably isn't worth performing compensation." The chip also takes input from the user, making trade-offs regarding the characteristics of the preferred image. These include the preferred picture size, frame transmission rate and picture quality.

As far as test and diagnostic system maintenance are concerned, British Telecom designers also planned ahead. A dedicated board inside the codec is responsible for

Looking at standards

To understand the functions performed by the video codec, it's first necessary to understand the H.261 standard or Px64 compression algorithm commonly used in video-based telecommunications. Px64 codes a video frame that's been divided into blocks for transmission using discrete cosine transformation (DCT), quantization and run-length coding techniques. If interframe coding needs to be performed, the frame to be coded is stored in memory, in addition to being coded and transmitted as bitstream output. In this way the frame (or, more accurately, 8×8 blocks within the frame) can be compared to corresponding blocks in the next frame to be transmitted. A motion-estimation processor compares the image stored in memory to the next transmitted image. A vector is created that relates the values of the prior block to the current one. The differences between the two frames, as well as the motion vectors, are then fed to the DCT, quantizer and entropy coders before transmission.

"Fundamentally, you take differences between each frame, transform the differences and line code them. Part of that process is to perform run-length coding on the data to reduce the amount that needs to be transmitted," says Peter Forty, head of British Telecom's codec development group. Using difference information substantially reduces the amount of data that needs to be compressed, since most scenes in teleconferences contain only small regions of change while other areas remain constant.

online checking. It determines if the codec is working correctly, and in production testing it can be used to test each board in isolation. "It allows us to 'loop out' each board," says Forty, "and even in some cases to go to a finer resolution than that. We take all of the other boards, except the board that we are interested in, out of the loop and then apply a source from the test control card to the card under test and see if the data coming out of that card is what we expect to see. The card also provides a direct interface to the user. It has all the terminal drivers, as well as the code for interacting with a remote terminal to set up the call."

Networking it

In any videoconferencing system, designers can expect to work with a variety of data at different clock speeds; and all of it must be synchronized before the codec will operate correctly. Video, audio and the channel interfaces must be locked to a reference clock on the network. "One of the most difficult things in the design of a video/audio codec is ensuring that the devices that are supposed to be locked together are locked together and that you don't get interference from the different clocks that are floating around," says Forty.

"With the channel interface, you probably have ten or more clock sources," he adds. Forty was reluctant to reveal how such engineering challenges were solved by British Telecom. The solution appears to be part of the "secret sauce" involved in the design.

As to networking the system, British Telecom supplies a variety of different interfaces to accommodate different speed and transmission requirements. There is an interface to a 4-kbit/s channel which, with an external terminal adapter, allows connection to ISDN (Integrated Services Digital Network). The unit can also provide 56,000 channels for the US27 standard. Yet another standard, RS449, a clock and data interface, can be operated at any rate from 56 kbits/s up to 2 Mbits/s. In the main codec itself, the primary rate channel interface (PRI) is implemented on a single card, with four option slots provided for enhancements; one of those is normally taken up by the 2B access or connection to ISDN or to a terminal adapter.

British Telecom's latest video teleconferencing system is already in the works, and will be announced within a few months. We can expect that Peter Forty and his team have again reduced the size of the motion estimation processor through further levels of integration, and have integrated many of the functions previously handled by FPGAs into large, full-custom ASICs. The resulting system may simply house a single bay of electronics, perhaps in as few as three to four boards. As British Telecom continues its work with Motorola, the actual parts designed into next-generation British Telecom systems may eventually become standard parts offered by Motorola on the open market. They may embrace not only the Px64 standard, but also the MPEG multimedia compression and decompression standards as well. ■

Coming in August from COMPUTER DESIGN...

The Official BUSCON '92 EAST Show Guide

COMPUTER DESIGN and BUSCON team up to provide you with a complete Show Guide package before and during the show.

The Guide: The Guide will include the full exhibitor listing and descriptions, a dining and entertainment guide, a major value-added bus/board market overview and analysis and inquiry card.

Value-added Editorial: This summer's official Buscon Show Guide, mailed with the August issue of COMPUTER DESIGN and distributed to all show attendees, will feature the usual show information — technical session descriptions and schedule, exhibitor listing, dining and events in the Boston area — but will be enhanced by editorial of special interest to COMPUTER DESIGN readers, Buscon attendees and exhibitors:

- The Buscon East Show Guide will focus its value-added editorial on the trade-offs involved in choosing a standard-bus architecture for a board-level implementation of a product versus a non-bus implementation; on the trade-offs involved in choosing a microprocessor or microcontroller for building bus-based or non-bus implementations; and on the issues involved in choosing the optimum operating system or kernel for the particular microprocessor architecture that will be used in an embedded or real-time application.

- Included will be a general overview of the market for embedded and real-time systems written by Senior Editor Warren Andrews. Rounding out the report will be selected viewpoint articles from the leading experts in the development of architectures, operating systems and kernels, and real-time software development tools.

Distribution: The guide will be polybagged along with the Eastern portion of COMPUTER DESIGN's August issue for a total distribution of 50,000+. In addition, a special mailing will go to all of the pre-registrants...and it will be distributed to each attendee at the show.

Issue Date: August 1, 1992

Pricing: $2,200 Per Page — including color.

Savings Opportunity: Advertise in the September Show issue of COMPUTER DESIGN and save $500 per Show Guide page.

Closing: July 10

BUSCON '92 East
September 15—17, 1992 Hynes Convention Center • Boston, MA

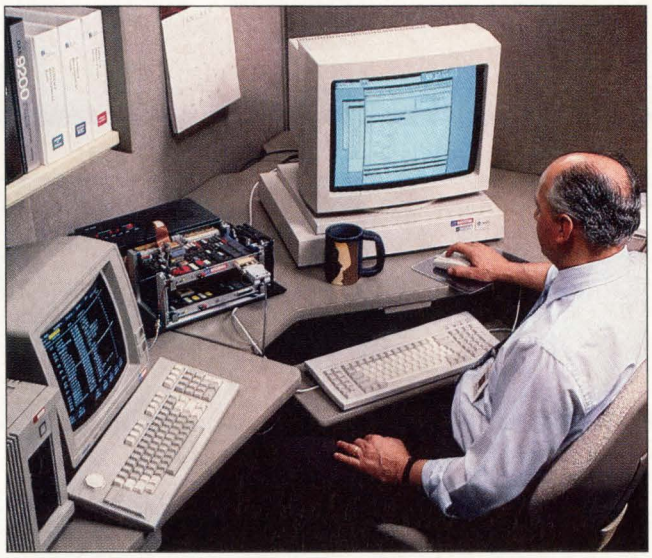
COMPUTER DESIGN• ONE TECHNOLOGY PARK DRIVE , WESTFORD, MA , 01886 • 508-692-0700 • FAX 508-692-7780
For more information, contact any of us ...
PUBLISHER: David L. Allen, 508-392-2111 • ASSOCIATE PUBLISHER Tim L. Tobeck, 508-392-2116• NATIONAL ACCOUNTS MANAGERS: • WESTFORD, MA, Tim Pritchard, 508-392-2217 • SPRING, TX, Eric Jeter, 713-353-0309 • SAN JOSE, CA, Diane Palermo, 408-371-7551 • STRATEGIC ACCOUNTS REPRESENTATIVES: • WESTFORD, MA, Sue Nawoichik, 508-392-2118 800-223-4259 • David Singer, 508-392-2109 800-223-4259 • INTERNATIONAL SALES OFFICES: • SURREY, ENGLAND, David Round, 81-686-7655 • PARIS, FRANCE, Daniel R.Bernard, 1-39-14-6780 • MUNICH, GERMANY, Johann Bylek,089-903-8806 • MILAN, ITALY, Luigi Rancati, 02-70-30-0088 • TOKYO, JAPAN, Toshio Equsa, 81-33-536-5404 • ASIA, AUSTRALIA, NEW ZEALAND, Tom Gorman, 852-833-2181

COMPUTER DESIGN
A PennWell Publication

CAE/CAD TOOLS

Logic analyzers tackle the "deeper" problem

Jeffrey Child, Associate Editor



LA-Connect, a program developed jointly by Tektronix and Microtec Research (MRI), combines a DAS9200 logic analyzer (left) and MRI's cross-compilers and X-Ray in-circuit source-level debugger. When object data is downloaded to the DAS, you can correlate the logic analyzer's real-time trace display with your high-level source code.

Perhaps the greatest opportunity to shorten the design cycle comes from spending time more effectively in the lab. While innovations in front-end tools have enabled designers to rapidly create designs on paper, and advances in manufacturing processes let you make up prototypes nearly overnight, most engineers still spend over half the design cycle in the lab, trying to sort out whether the design they created really works.

Logic analyzers, with their ability to passively observe circuit activity, play a key role in this process, helping designers discover logic system bugs and aiding them in refining their hardware/software integration process. And because emulators don't exist for many of the newest microprocessors, logic analyzers often provide the most sophisticated tool available for critical development work.

Faster, wider and deeper are still the demands that drive the development of logic analyzers. To meet the demands of today's faster and more complex microprocessors, these devices must be able to monitor signals at high rates, provide more channels to watch address and data buses and supply more memory to display larger segments of monitored waveforms.

Speed, channel count up

Responding to designers' demands, logic analyzer vendors have made steady advances in speed and channel counts over the past year. As the table shows, several analyzers offer synchronous clock speeds of over 100 MHz, while asynchronous clock rates above this figure have become routine. Likewise, channel counts of over 100 are now fairly common—even at maximum sampling rates. Less progress has been made in memory depth, although some vendors are making a concerted effort in this area.

Reflecting the opinion of several vendors, Jim Stager, vice-president of marketing at Biomation (Milpitas, CA), thinks that memory depth is important in today's design environment. "The industry seems to have caught up with the demand for faster and wider logic analyzers," says Stager. "We have logic analyzers available with hundreds of pins. And we're certainly keeping up with most of the microprocessors that are out there, and computers. But the depth game hasn't been played to the full extent." Biomation probably has the deepest logic analyzer available today, the K450M. A 100-MHz, 64-channel unit, the K450M currently offers 20 Mbytes of memory per channel. In addition, Biomation is sampling 80 and 320 Mbytes/channel in other versions.

While the price tag of $258,000 greatly limits the range of potential users for the K450M, Stager points out that there are applications where it can be essential. "If you want to perform cache tuning or see the probability of a particular instruction being executed during normal code operation, you can just record everything and do post-process analysis on it." Benchmark testing is another application for which the K450M is appropriate. "For example," Stager adds, "if you wanted to prove that a theoretical RISC processor will run faster than one that now exists, you could take a recording of the one that exists and code associated with it that it actually executed. Then you could match that up to a simulation model of your theoretical processor as it executes the same code."

The two extremes

As logic analyzer vendors continue to advance performance and integration, an interesting polarization has occurred. At the low end, led by Hewlett-Packard (Colorado Springs, CO), the traditional benchtop analyzer is now typically based on a logic-analyzer-on-a-chip solution. As a result, there's little room for differentiation among these products, except on the basis of price. As the table shows, a handful of such products are available for under $5,000.

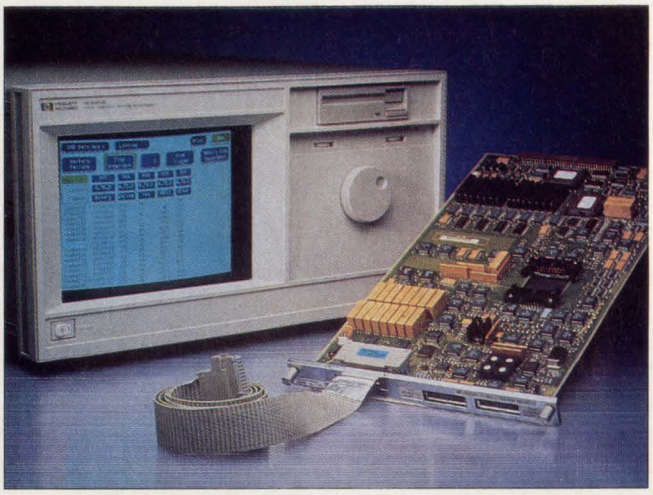
At the competitive high end of the logic analyzer market, activity is more diverse. For some time now, vendors have turned to modular solutions, helping both their customers and themselves preserve their investments by swapping in modules when it's time to upgrade or add new features.

The latest module designed for Hewlett-Packard's 16500-series logic analysis system is the 16542A, a 2-Mbyte data acquisition card.

Model	Max synch clock rate (MHz)	Max asynch clock rate (MHz)	Channels (state/timing)	Channels at max sample rate (state/timing)	Memory/channel (state/timing) (bits)	Triggering levels	Minimum glitch width (ns)	Price	Comments
American Arium 14281 Chambers Rd, Tustin, CA 92680 (214) 731-1661									**Circle 301**
ML4100L	25	100	32/32	32/8	2k	14	5	$2,695	Portable
ML4400P	200	200	100/100	50/50	32k	12	3.5	$17,495	Optional: 128k memory, timing to 500 MHz and 1 GHz. Supports all micros to 68040, R3051 and 80486. Modular design allows 360 channels.
ML4400I	50	100	80/80	80/40	4k	14	—	$11,495	Includes support for 50-MHz 80486. Optional 64k deep memory.
Biomation 1860 Barber Ln, Milpitas, CA 95035 (800) 934-2466									**Circle 302**
K450B	100	400	80/80	80/20	2k	16	3	$12,950	Portable, 8 - 16 bit disassemblers
K450M	100	200	64/64	32/16	20,000k	16	3	$258,000	80-Mbytes and 320-Mbytes samples available
K1000	—	1000	0/16	0/16	2k	2	3	$11,950	Portable low-cost timing analyzer
MLAS-132	500	500	32/32	16/16	2048k	2	2	$59,950	448 Channels maximum using separate chassis
CLAS4000	110	200	384/384	192/96	4k	15	5	$19,950	19-in. display, Macintosh host
K1600	—	20,000 equivalent	—/160	—/160	1k	1	1	$18,900	Analog display of all channels
Hewlett-Packard Company Inquiries 19310 Pruneridge Ave, Cupertino, CA 95014 (800) 452-4844									**Circle 303**
HP16542A/ 16500 System	100	100	80/80 (16 per card)	80/80	1M - 10M	1	10	$8,500/card	Memory is segmentable into multiple records; single card is 8 Channels x 2 M or 16 Channels x 1 M; multiple cards depth or width stackable
HP16550A/ 16500 System	100	500	204/204 (2 cards)	204/102	4k - 8k	12/10	3.5	$8,800/card	Transitional timing; time and state tagging; glitch trigger; compatible with all previous preprocessing
HP16515A/ 16500 System	—	1000	32 (2 cards)	32	8k	2	1	$8,300	—
HP1650 Series	35	100	80/80	80/80	1k	8	5	$3,500 - $8,000	32, 64 and 80 channel configurations; optional 100-MHz digital oscilloscope
John Fluke Mfg P.O. Box 9090, Everett, MA 98206 (800) 443-5853									**Circle 304**
PM 3585/30	50	200	32/32	32/32	2k	8	3	$5,450	Dual analyzer-per-pin architecture, MS-DOS utilities, IEEE 1149.1 support, offers 2,000 symbol names
PM 3580/60	50	100	64/64	64/64	1k	8	3	$6,695	Same as above
PM 3585/90	50	200	96/96	96/96	2k	8	3	$11,450	Same as above
Keithley Metrabyte 440 Myles Standish Blvd, Taunton, MA 02780 (508) 880-3000									**Circle 305**
PCIP-DLA	20	20	16	16	4k	2	2	$1,295	Stores and retrieves data trace sets in disk, overlays and compares two trace sets and does pass/fail comparisons on traces

Model	Max synch clock rate (MHz)	Max asynch clock rate (MHz)	Channels (state/timing)	Channels at max sample rate (state/timing)	Memory/channel (state/timing) (bits)	Triggering levels	Minimum glitch width (ns)	Price	Comments
Orion Instruments 180 Independence Dr, Menlo Park, CA 94025 (800) 729-7700									**Circle 306**
OmniLab 9360	34	204	96/96	16/16	128k - 512k	4	5	$12,550	Includes integrated 100-MHz, digital storage oscilloscope, 24-bit digital pattern generator, analog function generator
Promark Technology West 244 Sobrante Way, Sunnyvale, CA 94086 (408) 733-0272									**Circle 307**
PL 1000	200	1000	384/384	384/384	32k	15	4	$10,000 - $100,000	Operates under Windows 3.1. Optional pattern generator. Real-time comparator
KLA/2	350	2000	48	48	10k	2	0.8	$25,000 - $50,000	—
PL 100	50	100	32	32	8k/16k	4	5	$5,000	Operates under Windows 3.1. Fits inside any portable or benchtop AT-compatible computer
Rapid Systems 433 N 34th St, Seattle, WA 98103 (206) 547-8311									**Circle 308**
R3200	100	25	24	8	8k	4	10	—	—
R3600	200	50	32	8	8k	4	8	—	—
R3700	40	40	40	—	2k	2	25	—	—
R3800	100	50	32	—	8k	4	10	—	—
Tektronix, Test & Measurement PO Box 9864, Pittsfield, MA 01202 (800) 426-2200									**Circle 309**
Prism 3002CX 3001MPX	16	200	96/9	96/9	8k	7	—	$6,995 - $9,995	40-Mbyte hard disk, display, keyboard
Prism 3002CH	95	2,000	18/20	18/4	24k	4	2.5	$9,995	Same as above
1230	25	100	64	64/16	2k	13	5	$2,995	Digital oscilloscope module, user configurable
DAS9200	100	400	1536	1536/384	128k	16	2	$30,950	Pattern-generation performance analysis
Trace-Tek Instruments 1301 N Denton Dr, Carrollton, TX 75006 (214) 446-9906									**Circle 310**
16C50A logic box	35	50	16	16	1k	4	—	$1,295	Hand-held, battery-powered; PC software available
VMetro 16010 Barker's Point Ln, Ste 575, Houston, TX 77079 (713) 584-0228									**Circle 311**
VME-STA	16	100	96/99	96/99	2k/16k	4	4	$10,850	VMEbus analyzer system; 2 slots, simultaneous, state, timing, and anomaly analysis
FBT-625	50	200	177/105	177/105	32k	16	5	$25,000	Futurebus+ analyzer system; 1 slot, simultaneous state and timing
M2BT	10	—	56/—	56/—	8k or 32k	16	—	$9,500	Multibus II analyzer; 1 slot, 64 HW comparators

CAE/CAD TOOLS



The HP-16542A data acquisition card (front) from Hewlett-Packard offers 1 Mbit/channel, 16 channels and 100-MHz state/timing analysis. Up to five 16542A cards can be configured in an HP-16500A system mainframe (left), for a total depth of 8 channels by 10 Mbits/channel, or a maximum channel configuration of 80 channels by 1 Mbit/channel.

Each card provides 1 Mbyte/channel of memory with 100-MHz state/timing analysis across 16 channels. An HP-16500A mainframe may be configured with up to five 16542A cards.

The configuration of cards can be varied, depending on whether depth or width is more important to you. The choice is between a maximum memory depth of eight channels by 10 Mbits/channel, or a maximum channel width of 80 channels by 1 Mbit/channel. By attaching probe cables from multiple HP-16542A cards through a memory expansion interface, you can access up to 10 Mbytes of deep memory without any additional circuit loading.

Also recognizing the demand for deeper memory, Tektronix (Beaverton, OR) has beefed up the memory in its Centurion, a module of Tektronix's DAS9200 logic analyzer mainframe. Starting this month, the company intends to expand the Centurion's trace buffer to a 512-kbit depth behind each of the card's 1,536 channels.

A key factor behind the demand for deeper memory is the growing volume of software in modern embedded systems. With microprocessors racing at ever faster speeds, systems can crunch more code then ever in a shorter time. As a consequence, the software component of embedded systems has grown. While analyzers have traditionally been thought of as tools for debugging hardware, they're also finding a role in software debugging and hardware/software integration.

Software role

To address the needs of today's more software-intensive environment, Tektronix has teamed up with software development tool companies to create integrated tool environments. Last year, Tektronix and Microtec Research (MRI—Santa Clara, CA) teamed up to integrate a logic analyzer with software development tools. Called LA-Connect, the product combines C, C++ and Pascal cross-compilers and the X-Ray in-circuit source-level debugger with Tektronix's DAS9200 logic analyzer. Other tools (such as instruction set simulators and in-circuit debug monitors) are supported by LA-Connect as well. LA-Connect provides an application note that tells you how to use Tektronix's DAS9200 along with Microtec tools running on a workstation, so that the logic analyzer can provide the hardware breakpoints as you debug.

Microprocessors supported by MRI tools include the Intel i960, AMD 29000 and the Motorola 68000 and 88000 families. Expanding on LA-Connect to include 80X86 chips and tools, Tektronix recently an-

nounced a similar partnership with Concurrent Sciences (Moscow, ID). As a result, LA-Connect now integrates the Softscope source-level debugger and CSiMON debug monitor from that company. Support for several popular 80X86 compilers is provided.

At the heart of LA-Connect is a software linker that extracts symbolic information from object modules and converts the data to a format that's readable by the logic analyzer. By downloading this data to the logic analyzer via Ethernet, you can take advantage of the capabilities of the DAS9200, such as hardware breakpoints and real-time, state and timing analysis. Designers can correlate the logic analyzer's real-time trace display with their high-level source code.

A turning point

As design teams grow in size and faster 32-bit microprocessor designs become the norm, the demand for integrated tool sets is expected to increase. With this in mind, companies making high-end logic analyzers are planning their future products with a focus on interoperability.

"If you look at the spectrum of tools in the design environment that designers are working in, you see a lot of workstations," says Ken Panck, formerly a marketing manager at Tektronix. "The trend is to have these logic analyzers integrated at the workstation. That will start at the high end, because that's where the most powerful tools are."

The eventual goal is to let designers integrate hardware and software from within the same environment. "Maybe you could pull up and have a logic analyzer screen, then fill a trace buffer, and then link that back to your source code. These will make the logic analyzer more useful to software engineers by allowing them to stay in their host environment. Such solutions will require deeper memory. There is a trade-off between complex triggering (number of levels of triggering) and deep memory. But I think most users would vote for the deep memory and search for the problem, rather than have 14 levels of triggering," states Panck.

Michael Garber, product line manager for logic analyzers at Hewlett-Packard, agrees that integrated environments are the next step. "We're going to be seeing more connectivity with our customers' computers," says Garber. While the job of a logic analyzer is to capture data, interpreting that data can be a cumbersome task. Connecting a logic analyzer to a workstation and making use of software running on it may help that process. Adds Garber, "If you can just figure out how to hook it up and interpret what you see, its wonderful. That's how we're looking at the problem—trying to figure out how to help engineers do that." ■

Sponsored by the Rochester Section of the IEEE

THE FIFTH ANNUAL IEEE

ASIC CONFERENCE AND EXHIBIT

ASIC'92

September 21 - 25, 1992
ROCHESTER, NEW YORK

The 1992 ASIC Conference and Exhibit will provide ASIC and system level designers as well as R&D and manufacturing managers, and educators with knowledge of the tools and techniques required in all phases of ASIC design and implementation. The conference offers:

- ***A forum for the ASIC R&D community and vendors to share their experiences***
- ***An in-depth introduction to ASIC implementation for system designers***
- ***Executive overviews of ASIC trends, strategy, economics, and competitiveness***

HIGHLIGHTS

- Papers from Industry and Universities
- Educational Workshops
- Tutorial Sessions
- Panel Discussions
- Executive Keynote Speakers
- Conference Proceedings
- Exhibits
- Spouse Program
- Banquet/Luncheon Speaker
- Receptions

(Details in Advance Program)

Panel Discussions

Management --
Help or hindrance to ASIC technological competitiveness?
Top Level Synthesis --
Does performance meet expectations?

REGISTRATION

Lynne M. Engelbrecht, ASIC'92 Coordinator
170 Mt. Read Blvd.
Rochester, NY 14611, USA
Ph:(716)328-2310, Fax:(716)436-9370

Technical Paper Sessions

- Imaging and Communication ASICs
- Architecture and Physical Design
- Design and Test Methods
- Modeling, Synthesis, and Verification
- Designing Multichip Modules
- Cell Generators and FPGAs
- Analog and Mixed Signal Designs

Educational Workshops

Hands-on experience with:

- VHDL - Design and Simulation
- FPGA Design
- Designing Multichip Modules
- Mixed Analog/Digital Design
- Designing with ASIC Megacells
- Modeling Sub-Micron ASIC Macrocells

DISTINGUISHED SPEAKERS

Hal Alles	**Mentor Graphics Corporation**
Samuel Liu	**Silicon Integrated Systems Corporation**
Bruce R. Bourbon	**Vertex Semiconductor Corporation**
John Weldy	**Eastman Kodak Company**

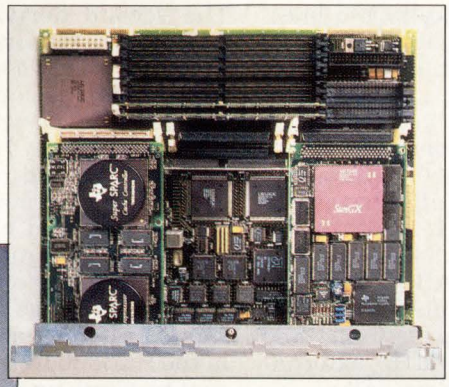
COMPUTERS & SUBSYSTEMS

Sparcstation 10 achieves new level of modularity

The recent announcement by Sun Microsystems (Mountain View, CA) about its latest Sparcstation ended speculation on which processor the next-generation workstation would use. In addition to announcing support for Texas Instruments' SuperSparc processor, Sun also took the wraps off one of the most modular and extendable workstations the industry has ever seen.

The new workstation, Sparcstation 10, ends the initial numbering sequence, as well as quieting speculation over what a Sparcstation 3 will look like—there won't be one. The jump in numbering, the company says, is to stress that the new workstation is not simply a next level, but that it represents a leap in performance.

While the key to the new workstation's performance lies in the 3,000,000+-transistor SuperSparc processor (see "Next-generation Sparc—can less be more?" *Computer Design*, June 1992, p 118), clever memory design, new peripheral interface circuitry and use of the new SBus 64-bit specification all contribute to the 2 to 4ö increase in performance over the previous generation. And if that's not enough, the Sparcstation 10 is the first commercial workstation offering built-in ISDN (Integrated Services Digital Network) capabilities.



Sun's latest workstation, the Sparcstation 10, brings a number of firsts to the desktop and single-board workstation business. It's the first to offer integral multiprocessing with plug-in M bus modules (inset), the first to provide on-board ISDN (Integrated Services Digital Network) capability and the first to make provision for up to four 64-bit SBus slots.

At the heart

At the heart of the Sparcstation 10 is Texas Instruments' (Dallas, TX) SuperSparc, mounted on a plug-in module. While the first release of the Sparcstation 10 will include a single 36-MHz processor (Model 30), at least three other upgrades were announced at the first release: the Model 41 (40-MHz single-processor version), the Model 52 (with two 45-MHz processors) and the Model 54 (comprising four 45-MHz CPUs). According to Sun, a 50-MHz version will be available by year-end.

In addition, the Model 40 will include a 1-Mbyte external cache, while the 52 will have two Mbytes and the 54, four Mbytes. The external cache makes possible dramatic increases in performance, particularly with applications that can take advantage of this larger memory.

Sun is the first workstation maker to bring multiprocessing to the desktop. The capability boosts performance in many applications that can take advantage of the SuperSparc's multiprocessors—either by using multiple processors with each working on one of several applications, or with each working on different parts of the same application.

On the M bus

The Sparcstation 10's modular design is aimed at letting you quickly and easily upgrade the CPU as well as I/O. Not unexpectedly, the new workstation has SBus expansion slots—four instead of the three provided by the earlier Sparcstations. And the SBus slots are designed to support the latest version of SBus (initially B.0), providing full 64-bit transfers.

But SBus is only one of the modular features of the Sparcstation 10. The included Sparc module, connected via the Sparc M bus, permits plug-in replacement of the processors. The module itself can contain one or two SuperSparc processors, along with some interface and cache logic. Units can accept up to two modules, each with two processors.

The M bus interconnect will also let you update processors as new generations come along. For example, a 50-MHz processor can replace the existing 40-MHz unit once the 50-MHz unit becomes available in quantity.

As promised by Sun's board-level group, the Sparcengine 10 (board-level implementation of the Sparcstation 10) will be available almost simultaneously with the desktop version. The single-processor version of the Sparcstation 10 will be available in the third quarter of the year, and multiprocessor versions are expected to be available in the fourth quarter. — *Warren Andrews*

Sparcstation 10 at a glance

- Up to 200 SPECint92, 228 SPECfp92 and 300 Mips
- One, two or four SuperSparc CPUs
- Two processor module sites
- Four SBus slots
- Built-in ISDN capability
- 36-, 40- and 45-MHz processors available; 50-MHz soon
- Runs Solaris 1.1, runs 2.0 with multiprocessing support

Sun Microsystems
2550 Garcia Ave
Mountain View, CA 94043
(800) 821-4643
Circle 353

INTEGRATED CIRCUTS

Siemens intros new generations of 40-MHz 8- and 16-bit MCUs

In what it's billing as the world's fastest 8- and 16-bit microcontrollers, Siemens AG (Munich, Germany) has added higher-performance generations to its two lines. The SAB80C52 and its derivatives are based on the Intel 8-bit 8051 instruction set, while the SAB80C166 family, developed jointly with SGS-Thompson (Milan, Italy), is a proprietary 16-bit architecture. To these families have been added the SABC501, which at 40 MHz is the fastest 8-bit controller around, and the SABC167, which features improvements in interrupt response and on-chip features while running at the 40-MHz external clock rate of the SAB80C166.

8-bit anchor

The anchors of the 8-bit line are the SABC501 and C501-R, which are completely software-compatible with the ROMless and ROMed versions of the 80C52. In re-engineering the core, Siemens optimized the critical paths, tightened the geometry and went to a denser process, but resisted the temptation to reduce the cycles per instruction associated with any given instruction. As a result, the relative execution time for all instructions in terms of cycles per instruction is the same as with the SAB80C52.

The SABC501 is aimed at speed upgrades of SAB80C52 designs and for low-power applications. It can operate over a voltage range of 3.0 to 5.5 V over the standard 0° to 70°C temperature range. The speed limit at the 3.0-V level is 12 MHz, ranging up to the full 40-MHz speed at 5 V. At 40 MHz, the part delivers a 300-ns instruction cycle time. The derivative versions based on the 501 core, which have added peripheral devices on the die, are rated to work at 5 V only.

Siemens is introducing two derivative parts along with the 501: the 502 and the 503. The SABC502 includes 256 bytes of XRAM, 16 kbytes of ROM, eight data pointers, and two watchdog timers. Among other things, it's aimed at users of high-level languages who need more RAM and pointers. The peripheral devices are taken from designs used in an earlier part, the SAB80C517A, which were then reworked under the design rules for the 501 core. The second derivative part, the SABC503, incorporates a 10-bit A-D converter and two watchdog timers, which also come from the SAB80C517A design.

With the SABC167, Siemens has greatly enhanced the interrupt response performance over the SAB80C166, and has increased the overall performance by increasing the performance of the peripherals. The SABC167 has a 50-ns interrupt sample rate as compared to 200 ns in the SAB80C166. Its overall interrupt response time (the time from an interrupt being received until the processor begins executing the interrupt routine) is now 250 ns, down from 400 ns with the SAB80C166. In addition, the SABC167 has 1 kbyte of on-chip RAM to hold up to 32 register contexts if desired.

Packaged in a 144-pin grid array, the SABC167 is probably the biggest 16-bit processor ever. It supports 110 I/O lines, 16 10-bit A-D channels, 32 capture/compare channels, and 52 interrupt sources. It also features on-the-fly ability to switch between five different bus configurations. For example, you can switch between 8- and 16-bit bus widths, select whether the bus is multiplexed or not, and choose the number of wait states.

Library, custom modules to come

Siemens plans to migrate its microcontroller technology through the use of standard library modules (such as RAM, ROM, A-D converters, and pulse width modulators), as well as custom modules developed by Siemens or in cooperation with customers, moving gradually in the direction of full ASICs. Improvements in process technology are expected to be leveraged off the 64-Mbit DRAM work being done in cooperation with IBM.

On the 8-bit side, the SABC501 and 503 are sampling now and the 502 will sample in the fourth quarter of 1992. Production quantities of each are expected the following quarter. Quantity 10,000 pricing for the 501, 502 and 503 respectively is $3.50, $5.50 and $4.00. The SABC167 will sample in the third quarter of 1992 and will be in production in the first quarter of 1993. Quantity 10,000 pricing will be $30.00. —*Tom Williams*

MCUs at a glance

- SABC501 (8-bit)

  40 MHz
  300-ns cycle time
  300-ns interrupt response
  1.2-µs 8 × 8-bit multiply

- SABC502 (8-bit)

  256 bytes XRAM
  16 kbytes ROM
  eight data pointers
  two watchdogs

- SABC503 (8-bit)

  10-bit analog-to-digital
  two watchdogs

- SABC167 (16-bit)

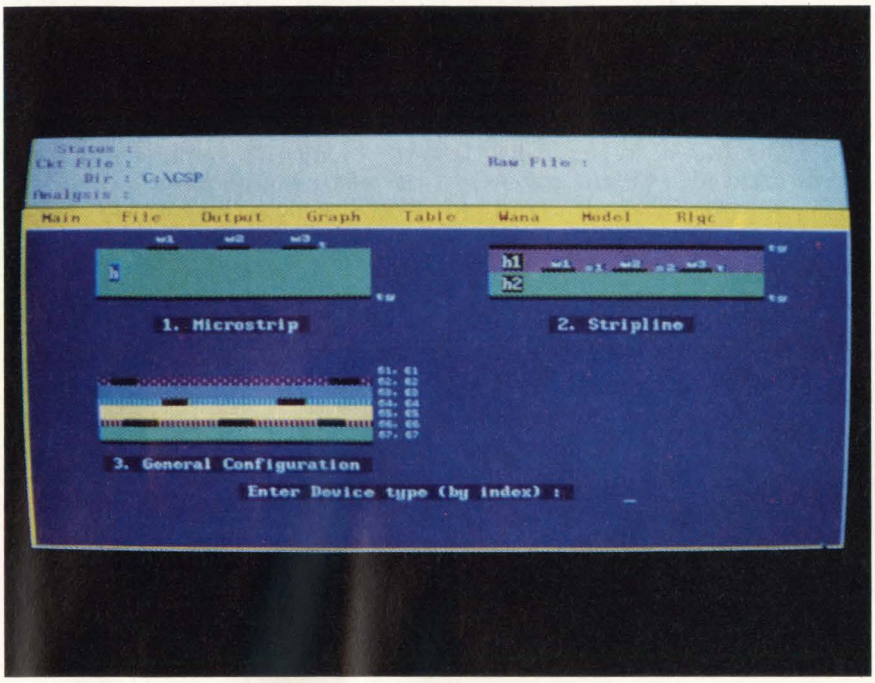
  40-MHz clock
  50-ns interrupt response
  50-ns counter resolution
  78-kHz pulse-width modulator with 8-bit resolution
  144-pin PGA

Siemens Components
Integrated Circuits Division
2191 Laurelwood Rd
Santa Clara, CA 95054
(408) 980-4583

Circle 356

CAE/CAD TOOLS

Tool targets transmission line effects in high-speed designs



Contec's RLGC two-dimensional field solver analyzes arbitrarily shaped conductors and multilayer dielectrics, including microstrip (top left) and stripline (top right). General shapes can be analyzed for connector and backplane modeling (bottom left).

Contec Microelectronics (San Jose, CA) has unveiled the RLGC Parameter Generator, a 2-D electromagnetic field solver that supports transmission line simulation for high-speed designs (R, L, G, and C stand for the per-unit resistance, inductance, conductance, and capacitance of transmission lines.)

The RLGC Parameter Generator uses a spectral domain analysis method to provide input to Contec's SI (Signal Integrity) simulator for analysis of nonlinear electronic circuits, including the electrical effects of the interconnects.

Simulation requires accuracy

"Faithful simulation of high-frequency designs demands accurate characterization of transmission lines," says Paul Wang, president of Contec's CAE division, "because signal degradation effects such as crosstalk, mismatch and loss greatly increase above 40 MHz. We believe that we have a more precise solution for determining transmission line RLGC parameters than other solvers, which are dependent on the boundary element method."

According to Wang, the spectral domain method eliminates the need to calculate the polarization charge at the dielectric interfaces, which lets the Parameter Generator accurately compute mode velocities and reduce the matrix sizes and number of unknown charges. "Our method doesn't have to rely on broad assumptions, limited configurations or other shortcuts that can reduce the accuracy of the outcome," Wang points out.

Other features of the solver include correct modeling of the edge condition, the ability to handle any number of dielectric layers and the capability to handle arbitrary conductor cross-sections.

The 2-D solver takes dielectric loss into account by calculating the G matrix at the specified frequency—a capability that Contec asserts is imperative for lossy substrates such as gallium arsenide. The tool also accurately computes the R matrix associated with resistive loss in the conductor as a function of frequency without making assumptions about the relative magnitudes of the depth of penetration and thickness of the conductor. This lets the SI simulator include skin effects. In addition to RLGC matrices, the tool calculates mode velocities, attenuation and characteristic impedances.

The RLGC Parameter Generator is available now. Licenses are priced at $4,500 for PC versions and $8,400 for versions that run on Sun and HP workstations. — *Mike Donlin*

RLGC Parameter Generator at a glance

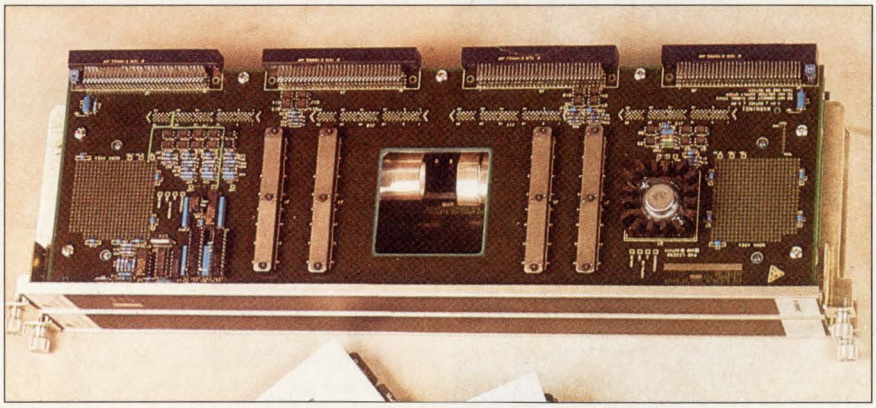
- Provides input to Contec's SI simulator for analysis of nonlinear electronic circuits
- Features accurate modeling of the edge condition, the ability to handle any number of dielectric layers and arbitrary conductor cross-sections
- Accounts for ground plane and ground conductor resistances to simulate crosstalk
- Available now for $4,500 on PCs and $8,400 for Sun and HP workstations

Contec Microelectronics
2188 Bering Dr
San Jose, CA 95131
(408) 434-6767
Circle 351

CAE/CAD TOOLS

Software keeps track of timing delays and constraints

As system clock speeds routinely climb to 50 MHz and beyond, the timing relationships between components in a system become critical. A stumbling block in tackling these timing problems is the lack of accurate timing information for VLSI devices and microprocessors. Logic Modeling (Milpitas, CA) promises to address these problems with its latest software, Release 2.0, for the LM family of hardware modelers.



Release 2.0 works with a Device Adapter Board (DAB) to model devices with up to 640 pins—twice the previous 320-signal-pin capability.

"Today's sophisticated devices have very different timing characteristics depending on their state or mode of operation," says Koorosh Nazifi, director of hardware modeling marketing at the company. "For example, the 486 has different setup and hold values for each of the 10 possible states that need to be tracked. Release 2.0 extends our timing capability to include this information, and makes it available on all supported simulators as a universal model."

Keep track of what's happening

The new software provides features for tracking timing constraints and delays. These include state-dependent and pin-dependent timing checks and delays, which require tracking of the internal registers and modes of the device during simulation to verify a device's proper timing. Setup, hold, cycle, pulse width, stability, and recovery times for a device can be specified in Logic Modeling's Shell Software. With this capability, a device's interaction with the rest of the system can be accurately checked, and errors and violations can be reported by the hardware modeler to the system.

The software's state tracking and mode dependency features combine behavioral-like Shell Software statements with the hardware modeler's ability to detect logic states, providing timing accuracy for full-function hardware models. To reduce pessimism and false errors caused by reconvergent fanout, Release 2.0 provides mechanisms for tracking input pin changes that cause changes on output pins of a hardware model. This capability provides common ambiguity elimination and makes min/max simulation more accurate by eliminating false errors.

Propagating the unknown

Unknown states generated during simulation typically represent design errors such as timing violations, state contention or an uninitialized condition. Release 2.0 features a proprietary unknown-propagation algorithm designed to accurately propagate the unknowns presented on a device's input pins, reducing pessimism and inaccuracies. The hardware modeler's unknown-propagation feature supports multisequence unknown propagation. The number of pseudorandom sequences is user-selectable and can be set within the Shell Software.

Release 2.0 is backward compatible with Release 1.3 and 1.2 software and will run with existing hardware models without any modification. Shell Software needs to be modified, however, to take advantage of the Release 2.0 timing features.

In addition to improving the quality of timing information for hardware models, Release 2.0 speeds overall simulation time, according to Logic Modeling. Generally, a hardware modeler offers better performance in simulation than gate-level or structural software models. On the other hand, the performance of long simulations for designs containing a large number of hardware models can be affected by hardware model evaluation time. Release 2.0 supports concurrent evaluation of hardware and software models. This lets the simulator parallel the evaluation of software and hardware models, eliminating any potential simulation idle time due to hardware model evaluations.

Release 2.0 is available now at no charge to users who are covered by software maintenance or standard system warranty. For nonmaintenance users, the upgrade will cost $10,800. *—Mike Donlin*

Release 2.0 at a glance

- Provides timing verification information to the LM family of hardware modelers
- Combines behavioral-like Shell Software statements with hardware modeler's logic state information for timing accuracy
- Features a proprietary algorithm to accurately propagate unknown states on a device's input pins
- Supports devices with up to 640 signal pins
- Backward compatible with previous releases

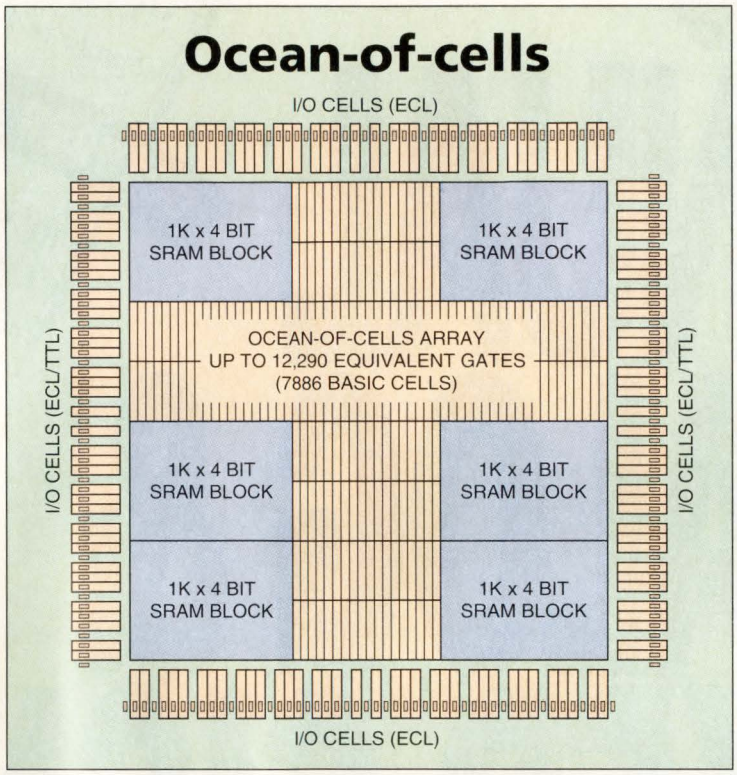
Logic Modeling
1520 McCandless Dr
Milpitas, CA 95035
(408) 957-5200
Circle 357

ASICs & ASIC DESIGN TOOLS

SRAM, logic and analog functions from ECL customizable arrays

Synergy Semiconductor's (Santa Clara, CA) System Elements family of bipolar ECL arrays offers embedded SRAM blocks with speeds to 3 ns and compiled metal-only SRAM. Based on Synergy's Asset (All Spacer-Separated Element Transistor) technology, the 1.2-µm System Elements achieve a unity gain frequency of 17 GHz and feature unloaded gate delays of 70 ps at just 200 µA.

The devices' Ocean-of-Cells architecture offers you the ability to craft individual Asset transistors and available resistors into simple analog functions. With system clock frequencies above 1 GHz, the System Elements are suitable for applications in speed-critical products. Synergy jointly developed the new parts with Toshiba America Electronic Components (Irvine, CA), which will act as a second source.



The SY9BP6R4 RAM-Intensive System Element (RISE) has six independent blocks of 3-ns embedded ECL SRAM plus an Ocean-of-Cells array with up to 12,290 equivalent two-input gates of 70-ps logic. I/Os located at the left and right sides of the die may be configured for TTL levels as well as ECL. A six-transistor cell is the basic "core tile" of the SY9BP6R4.

The transistor-level structure of System Elements devices allows implementation of logic gates, SRAM cells or analog functions via personalization of metal layers only.

By not prewiring individual transistors into conventional logic gates, Synergy has built into its System Elements the capability to connect cell components to produce analog functions. Designers can construct analog functions within analog zones, isolated from surrounding digital circuitry by separate power, ground and I/O pins, dedicated bias generators and metal guard rings. Using as few as five transistors and three resistors, you can implement a no-frills analog building block such as a simple voltage comparator in one basic cell. The Asset cell also lends itself to low to medium-resolution A-D and D-A converters.

Just the start

The initial four System Elements family members include one RAM-Intensive System Element (RISE) with embedded memory and three Universal System Elements (USEs) with nonembedded memory. The SY9BP6R4 RISE device has half a dozen blocks of 3-ns 1k × 4-bit SRAM combined with up to 12,290 equivalent two-input gates (7,886 core cells) of 70-ps logic. The SY21BP00, the densest of the introduced USE devices, has 33,555 equivalent two-input gates (21,120 core cells) of 70-ps logic and routinely achieves a logic density in excess of 450 gates/mm^2.

The SY9BP6R4 RISE and the SY21BP00 USE devices can be configured with all 144 pins ECL logic-level compatible (10k, 100k, or 101k), or with up to half the pins compatible with TTL levels, thereby eliminating the need for external ECL/TTL translators. Both devices are available in thermally-enhanced, low-capacitance molded packages (208-pin PQFP or 207-pin plastic pin grid array [PGA]), or a 240-pin high-density aluminum-nitride-surface PGA.

The lower density USEs available now are the SY4BP00, with up to 9,065 equivalent gates and 80 I/O, and the SY1BP00, with up to 1,665 equivalent gates and 32 I/O. Both come in PQFP and plastic leaded chip carriers.

Piece prices for Synergy's System Elements vary with device size, degree of complexity of circuitry implemented by the user, performance requirements, percentage of array utilized, RAM speeds, and packages. — *Barbara Tuck*

Systems Elements family at a glance

- Embedded and metal-only compiled ECL SRAM blocks
- Intermixture of ECL, TTL and analog I/Os
- Mixed-signal capability via analog zone
- Analog macro library

Synergy Semiconductor
3450 Central Expressway
Santa Clara, CA 95051
(408) 730-1313
Circle 354

2ND ANNUAL ANALOG & MIXED-SIGNAL DESIGN CONFERENCE.

HYATT REGENCY
San Francisco Airport
OCTOBER 28-30, 1992
BURLINGAME
CALIFORNIA

As a design engineer, higher speeds and greater complexity of electronics systems are making your job more challenging. And with clock speeds climbing to 50MHz and beyond, analog characteristics are becoming major considerations for digital design.

According to Technology Research Group, 40% of all ASICs will be mixed analog and digital by 1994. With this kind of demand, today's designer must be informed and prepared. Finally, there's a source of objective and up-to-date information on mixed signal design–The *Analog and Mixed-Signal Design Conference*. This technical conference, sponsored by *Computer Design* Magazine, features over 50 lectures and workshops 100% dedicated to your needs. Nowhere else will you find so much information, technology and expertise under one roof.

HIGH QUALITY WORKSHOPS

Respected engineers will offer high-quality information that you can immediately use to complete your design projects more quickly, creatively, and elegantly. You'll learn about analog and mixed-signal simulators, different design techniques, analog implications of high-speed systems, and much more in workshops such as:

- Analog Effects in High-Speed Design
- Mixed Analog/Digital Design Modeling, Simulation, and Test
- Selecting the Optimum Analog Devices
- Digitizing Analog Functions
- Solving Convergence Problems in SPICE
- Configuring Mixed-Signal with ASICs

And much, much more.

PRACTICAL HANDS-ON INSTRUCTION

For years you've been subjected to press releases from vendors under the guise of objective discussions or exposed to academic papers that had little bearing on your design problems. The *Analog & Mixed-Signal Design Conference* is different. You'll find in-depth, practical and real-world information from industry experts who have been there. They'll give you knowledge you can bring to the workstation tomorrow!

WHO SHOULD ATTEND?

The *Analog & Mixed-Signal Design Conference* is dedicated to the unique needs of mixed-signal design. If you're a digital designer addressing the problems of high-speed designs, a digital designer involved with analog, or an engineering manager making decisions about CAE/CAD tools you must attend this conference.

QUESTION AUTHORITY

The *Analog & Mixed-Signal Design Conference* Vendor Products Exhibition features booths crammed with the latest in analog and mixed-signal design tools. As questions arise during the workshops, you can go directly to the vendor authorities on the exhibit floor for answers. They will be on hand to let you try out and compare products, give you a clear grasp of the practical tools available, and tell you where to look for new avenues of information exchange.

As an attendee at the *Analog & Mixed-Signal Design Conference* you'll learn how to improve your design skills, how to increase productivity, and where to turn in order to ensure design success. All in three days under one roof.

Join your colleagues this October in Burlingame. The *Analog & Mixed-Signal Design Conference* promises to be one of the most significant industry events of the year!

For more information call Tom Loftus at (415) 905-2354 or Fax (415) 905-2220.
Sponsored by Miller Freeman Inc.
P.O. Box 7843
San Francisco, CA 94120-7843

ANALOG & MIXED SIGNAL
DESIGN CONFERENCE

Tell me more about the *Analog & Mixed-Signal Design Conference.*
I'm interested in: ❑ Attending ❑ Exhibiting

NAME _____ TITLE _____

COMPANY _____

STREET _____

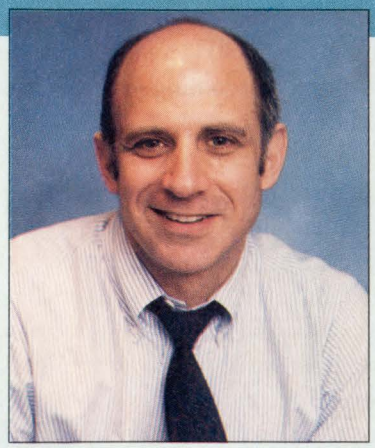
CITY _____ STATE _____ ZIP _____

PHONE _____ FAX _____

Mail or Fax to:
Analog & Mixed-Signal Design Conference
P.O. Box 7843, San Francisco, CA 94120-7843
Phone (415) 905-2354 / Fax (415) 905-2220

OCTOBER 28-30, 1992
Hyatt Regency
San Francisco Airport
Burlingame, California

CDAS1



Standard linear parts from customizable arrays

With analog and mixed-signal circuits, there's an almost endless need for customization, but what I'm hearing about repeatedly these days is ASSPs—application-specific standard products. These are standardized industry-specific products—such as disk drive read channels and telecommunications modems—that are built around an array of analog or mixed-signal cells. Like digital gate arrays, they are configured by their metallization layers, and represent a relatively quick way to tweak performance or add special features to an otherwise standard product.

Linear arrays, however, present some architectural and manufacturing challenges, and very few manufacturers have been able to offer them the same way that, say, digital ASIC vendors have offered gate arrays and standard cells. Manufacturers whose early business consisted of analog arrays—Exar (San Jose, CA), GEC Plessey Semiconductors (formerly Interdesign, Scotts Valley, CA) and Micro Linear (San Jose, CA)—have migrated, with their customers' help, toward standard product offerings. These manufacturers never hid the fact that many of their standard offerings were based on linear arrays. But expertise in disk drive electronics or communications was inevitably more visible than the array-based implementation.

Change is in the wind

That seems to be changing now. Not only are manufacturers such as Micro Linear touting their array technology by showing catalogs of customizable ICs, but the number of array vendors is also growing. An increasing number of IC vendors are *admitting*, if not *announcing*, that they too build standard products based on linear array technology. The names include those companies with strong bipolar manufacturing expertise: AT&T Microelectronics (Reading, PA), Harris Semiconductor (Melbourne, FL and Somerville, NJ) and SGS-Thomson (Carrollton, TX).

The reasons for this trend are twofold. First, array technology has changed. New CAE tools, combined with tighter geometries and double- or triple-layer metallization, make for better silicon utilization. The resulting linear and mixed-signal chips are no longer as costly to manufacture as they once were. Second, customization demands are tending toward high-frequency and high-performance areas where the user expects to pay a premium. These are areas where the bipolar expertise of array vendors shows up best.

It starts with a linear array

The foundation for ASSPs is a linear array—a series of commonly used analog devices, such as small-signal transistors, perhaps a beta-matched input pair, larger driver transistors (mostly NPNs), thin-film resistors and capacitors, as well as more complicated devices such as op amps, comparators and voltage references.

These arrays are prefabricated and are available in many different sizes and types, depending on the target application. Implementation and customization of a circuit are accomplished by means of metallization. In the old days, you took home a drawing of the array and drew a metal mask on tracing paper, almost the same way you'd draw the interconnects between components on a schematic diagram. These days, with digitized cell libraries depicting available components, the metallization layers are drawn on personal computers or Unix workstation screens using CAE tools.

Moreover, the architecture of many commercial arrays has been altered. Since linear CMOS and mixed BiCMOS processes allow higher densities, simple transistors and op amp arrays can be pushed to the outer edges of a chip, while the inner cells can include some fairly complicated logic and signal-processing blocks.

In principle, a linear array is a good solution to the problem of fast turnaround. The chips are already made and you simply need to metallize them for your application. In practice, it can be a very expensive way to go. You're actually paying to have the IC devices manufactured twice—once to build the array and certify that all the devices on it are working and accessible, and again to metallize selected devices and verify that they still work the way you want them to.

Perhaps the only way to avoid paying for silicon real estate and testing you don't need is to obtain 100

percent utilization of the devices on any chip. But because analog circuits are often pieced together by individual circuit designers, almost as a work of art, there's very little consistency between circuit implementations—even for the same application. And, inevitably, analog array chips have a very low utilization. An 80 percent utilization—a borderline proposition for a digital gate array—can be an economic disaster on an analog array. A user might select 80 percent of the devices, but, because there's no consistency between analog device sizes, the 20 percent not selected could be power transistor drivers, which take up half the chip.

Better utilization

But the linear array vendors have become very sophisticated about size and arrangement of devices, gearing them in many cases toward specific industry requirements. A disk drive read channel or communications modem, for example, either of which may have begun life as a metallized array, is repacked using ASIC standard-cell or handcrafting techniques to provide a tighter layout, smaller chip size and subsequently higher yields. Unused devices and circuit elements are typically eliminated in the process, but in certain areas of the chip the original array may be left intact. In this way an otherwise standard product—albeit, an industry-specific product—can be customized with minimal effort at a later date.

But the die-shrink that comes from knowing precisely what a customer wants also applies to the layout of the basic arrays. Devices that absorb large amounts of silicon area, such as power transistor drivers, are typically no longer included on most commercial arrays. Even the traditional real estate hogs such as thin-film resistors are optimized, in conjunction with laser trimming, to provide a range of resistor values in a very small area.

What Micro Linear calls its "application-focused arrays" include the FB3651 LAN transceiver, the FB3480 switch mode power supply controller and the FC3560 read channel array—arrays are specifically optimized for particular application requirements. The LAN transceiver array, for example, is geared toward 10Base-T applications. It includes nine timer cells, 12 analog function blocks, six high-frequency transmitter/receiver blocks, and 150 digital logic gates. This array has been the basis of standard products such as the ML4651/52 10Base-T transceivers and the ML4651 multiport repeaters.

The FB3480, similarly, includes an oscillator, voltage reference, error amplifier, 2-A output drivers, and is the basis for eight different catalog offerings.

The 10Base-T transceivers are based on Micro Linear's bipolar FB3600 family, a set of 12-V arrays with 1-GHz devices. The power supply controllers are built around the FB3400 bipolar family, a set of 36-V arrays with 300-MHz devices.

The FC3560 read channel array, however, is based on the company's FC3500 series of BiCMOS arrays. These arrays provide 5-V bipolar devices, including 4-GHz NPNs, 50-MHz PNPs and 50-mA power drivers, in addition to 1.5-μm linear CMOSs. Available analog circuit blocks include 8-bit A-D converters, 8-ns comparators and op amps with 100- and 350-MHz gain-bandwidth products.

Excited by speed

It's the fresh challenge of high-frequency applications—cellular telephones, wireless networks, fiber-optic links—that's encouraged manufacturers such as AT&T and Harris to show their capabilities in the linear array area. Both AT&T and Harris compete with complementary high-frequency bipolar processes. These are manufacturing processes that provide closely matched PNP and NPN transistors in terms of frequency response (f_t), current gain (β) and silicon area. New-generation current feedback amplifiers, low-voltage drivers and receivers (those that swing close to a +3-V power-supply rail) and push-pull amplifier outputs all depend on the use of matching PNP transistors.

Obtaining good PNP performance, however, depends on isolating transistors from interaction with other elements on the silicon substrate. There aren't too many ways of accomplishing this, and the ones that exist will raise the price of a high-frequency array. AT&T uses a junction-isolated process, in which a series of diffusions and implants converts an N region into a P for use by the PNP transistor. The process requires 18 to 20 masking steps. Harris uses a wafer-bonding technique, in which the isolation regions between transistors are formed by chemical etching through one wafer, which is actually glued through an oxide layer to another.

Products of the AT&T complementary bipolar IC (CBIC) processes include the ALA201/202 and the ALA210 UHF arrays. These arrays offer 12-V NPN transistors with a 4.5-GHz f_t and 11-V PNPs with a 3.75-GHz f_t. AT&T's newest complementary bipolar process, the 6-V CBIC-V, provides 10.2-GHz NPNs and 4.8-GHz PNPs, and provides the foundation for the ALA110 linear array.

In addition to its UHF-1 process, Harris trades on the experience of GE/RCA in linear arrays, suggests strategic planner Brian Mathews. The HTA3000 tile arrays offer 8-GHz NPNs and 4-GHz PNPs, and operate at up to 10 V. Devices built with the process include 850-MHz op amps and automatic test equipment pin drivers with better than 3,000-V/μs slew rates.

But don't expect any of this high-speed technology—even array-based technology—to come cheap. While this is the area where six-week turnaround is most plausible, NRE—the front-end engineering cost—for a Harris HTA3000 array is "ballparked" at around $97,000.

Stephan Ohr is president of Indian Forest Research and editor of the monthly newsletter, Mixed Signals.

SYSTEM SHOWCASE

SYSTEM SHOWCASE

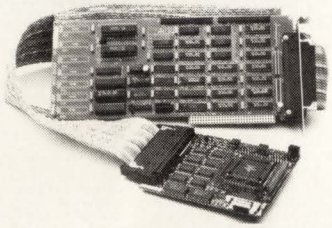
Reach over 100,000 qualified engineers and engineering managers with *SYSTEM SHOWCASE* advertising.

Rates start at $940

For more information call Sue Shorrock at 800-225-0556 or 508-392-2185

68HC16 68332

PC-based In-Circuit Emulator



- Supports 68HC16Z1, 68331, 68332, 68340 with more members of the HC16 and 300 families to follow.
- User interface under Microsoft Windows.
- Memory contents available in real-time (shadow RAM).
- Up to 17 MHz real time emulation.
- Full control of TCNT at breaks and single step.
- High-level C support. In-line assembler and disassembler.
- 10-day free trials available to qualified customers.

nohau CORPORATION
51 E. Campbell Avenue
Campbell, CA 95008
FAX (408) 378-7869
(408) 866-1820

CIRCLE NO. 167

OrCAD OFFERS DESIGN POWER FOR DOS AND UNIX USERS

Our DOS-based *Schematic Design Tools* are known for being the best price/performance value in the EDA industry. With the introduction of OrCAD's new line of UNIX® based products for the Sun SPARCstation™, OrCAD defines a new standard for ease-of-use, power, and value. **Call (503) 690-9881 for information.**

OrCAD®

CIRCLE NO. 168

OEM AIR PUMPS/ COMPRESSORS

- Only one moving part • Oilless
- Low power • Low vibration
- AC & DC models

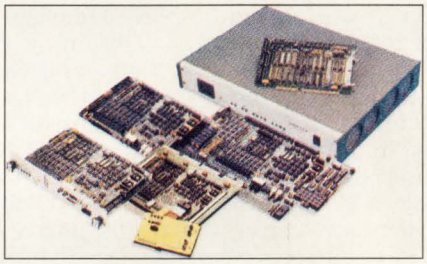
Call us to discuss your application
TEL: 708-860-0500
FAX: 708-860-9473

MEDICAL/SURGICAL • LEAK TESTING
BUSINESS MACHINES
AERATION SOURCES
VENDING MACHINES
ENVIRONMENTAL
GRAPHIC ARTS

Send for FREE catalog

MEDO USA, INC.
808-A No. Central Ave.
Wood Dale, IL 60191

CIRCLE NO. 169



REAL-TIME NETWORK

The SCRAMNet Network™ combines the real-time speed of replicated shared memory with the flexibility of a fiber optic LAN to get microsecond response from multi-vendor computers. It allows you to connect dissimilar computers at 150/Mbits/sec over fiber optics, with zero software overhead. This replicated shared memory network offers data filtering, programmable byte swapping, and a sophisticated interrupt structure.

SYSTRAN CORP.
4126 Linden Avenue, Dayton, OH 45432-3068 USA.
Phone (513) 252-5601 or 1-800-252-5601.

CIRCLE NO. 170

QUICK-TURN PC BOARDS

INSTANT QUOTES

1-800-234-1556
(After Hours (602) 377-7319)

Single/Double Sided/Multi-Layer
Gerber Input/Floppy or Modem

VISA MIL Approved U.L. Listed MasterCard

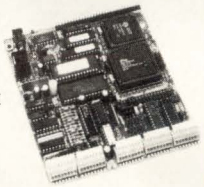
AVANTI CIRCUITS, INC.
17650 North 25th Avenue
Phoenix, Arizona 85023

(602) 863-7729 & 234-1556
Fax (602) 375-1909
BBS/Modem (602) 234-1737

CIRCLE NO. 171

MICROCONTROLLERS

- C Programmable
- Data Acquisition
- Control / Test
- Excellent Support
- From $159 Qty 1
- *New* Keyboard Display Modules



Use our **Little Giant**™ and **Tiny Giant**™ miniature controllers to computerize your product, plant or test department. Features built-in power supply, digital I/O to 48+ lines, serial I/O (RS232 / RS485), A/D converters to 20 bits, solenoid drivers, time of day clock, battery backed memory, watchdog, field wiring connectors, up to 8 X 40 LCD with graphics, and more! Our $195 interactive **Dynamic C**™ makes serious software development easy. You're only *one* phone call away from a total solution.

Z-World Engineering
1724 Picasso Ave., Davis, CA 95616
(916) 757-3737 Fax: (916) 753-5141
Automatic Fax: (916) 753-0618
(Call from **your fax**, request catalog #18)

CIRCLE NO. 172

GUI FOR INTEL 8051 EMULATOR

Franklin Software's GUI Emulator Interface brings windows-like power to Intel and Nohau 8051 emulators at a special price--

Special Offer: $49.

Emulator Interface Features:

- ❑ Fast graphical user interface with Drop Down Menus.
- ❑ Default windows for code, data, and status information.
- ❑ Symbolic debugging of "C" or PL/M-51 code.
- ❑ "Watch Windows" trace variables, structures, etc.
- ❑ Supports all emulator functions and Intel/Nohau tools.
- ❑ Point & Shoot (Mouse) control of emulator and target.

For Intel and Nohau Emulator Customers Only.

FRANKLIN SOFTWARE, INC

Call (408) 296-8056 Ext. 431 for details.
Please have your FAX number ready.

CIRCLE NO. 173

REMOVE HARDWARE LOCKS

Protect your investment!
Don't wait for your lock to get lost, stolen or fail and render your program useless.
Our **SAFEKEY'S** are guaranteed to unlock the following:

PADS 2000	MAXROUTE	TOPAZ
PADS PCB	MICROSTATION	RIO
SMARTCAM	3D STUDIO	& MORE

Limited Time Offer $399 plus S&H

(609) 390-2799
24 HR. FAX HOTLINE
(609) 390-3750

IMAGINE THAT
1 Evergreen Dr., Seaville, NJ 08230
TM-Trademarks property of respective owners.

CIRCLE NO. 174

SYSTEM SHOWCASE

USE OUR READY TO ORDER EXPERTISE IN:

ANALOG AND MIXED SIGNAL ANALOG-DIGITAL INTEGRATED CIRCUIT DESIGN, DEVELOPMENT TESTING AND MANUFACTURING.

TO:

● Reduce Costs ● Safeguard Your R&D Investment
● Increase Reliability ● Enhance Product Image
● Increase Manufacturability

TECHNOLOGIES	*VOLTAGE/CURRENT/FREQUENCY CAPABILITY*
CMOS Technology	Voltage : 1.5 to 500 Volts
BIPOLAR Technology	Current: 100nA to 5 Amps
BiCMOS Technology	Freqency: DC to 1 Ghz

APPLICATIONS SERVED
POWER ELECTRONICS TELECOMMUNICATIONS SIGNAL PROCESSING
CONTROL CIRCUITS FILTERS INSTRUMENTATION DATA ACQUISITION
COMPUTER PERIPHERALS DATA TRANSMISSION INTERFACE

FEATURES
STANDARD PRODUCTS BREADBOARD PARTS STANDARD CELL LIBRARIES
ANALOG ARRAYS ANALOG-DIGITAL ARRAYS LOW COST PROTOYPING
CONSULTATIVE ASSISTANCE ONE STOP SHOPPING SYSTEMS EXPERTISE

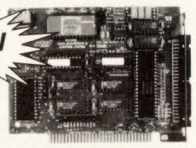
SPG SIGNAL PROCESSING GROUP
401 N. Alma School Rd., M.S.#9,
Chandler, AZ 85224
Ph: (602) 786-1197 Fax: (602) 821-2472

CIRCLE NO. 175

PC Bus Data Acquisition

...over 50 exciting hardware & software products!

NEW



AD1200 *only* **$359**

- 12-bit 125 kHz A/D Conversion
- 16 Analog Input Channels
- 3 Timers and 16 DIO Lines
- Supports DMA and Pacer Clock
- AT Bus Version Available!

A/D, D/A, Digital I/O and Timer/Counters for PC XT and AT computers • 12-bit A/D rates to 200 kHz! • Eight boards for AMPRO form factor CPUs • 110 VAC relay, optoisolation, multiplexer and thermocouple boards • DSP and data acquisition software • Request your ***FREE 80 page catalog today!***

rtd Real Time Devices, Inc.
State College, PA USA

Tel.:814/234-8087 • FAX:814/234-5218

CIRCLE NO. 176

SCSI-2

Low-cost, PC-Based Testers

For all SCSI Devices with solutions for every testing situation... design, manufacturing, field service

Transfer data at 10 MBytes/second. They feature:
- SCSI-2 Command Queuing
- SCSI-2 Message System Support
- High-level Multi-threading Support
- Initiator and Target Emulation

We offer complete development systems, low-cost manufacturing platforms and portable turn-key systems, all available with integrated bus analysis.

For information or prompt quotation, call, write or FAX us:

I-TECH CORP

6975 Washington Ave. So.,Suite 220 • Edina, MN 55439
612/941-5905 • FAX 612/941-2386

CIRCLE NO. 177

FINALLY

One tool to satisfy all your firmware development needs

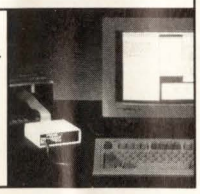
PROMICE is a universal system.
- Develops code for any microprocessor
- Complete, real time, source level debugging
- Host software for DOS, Unix, Mac, VMS
- Non intrusive on your target system
- Simply plugs into any ROM socket

PROMICE also supports Turbo Debugger, C_thru_ROM, FreeForm, GDB, and more.

PROMICE
...the affordable solution.

Grammar Engine Inc.

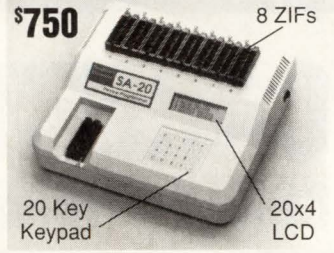
TEL: (614)471-1113
West: (415)750-0219
FAX: (614)475-6871



CIRCLE NO. 178

EPROM PROGRAMMER

$750



- **Quick pulse** pgms. eight 1 Mbit EPROMs in 40 sec.
- Stand-alone or PC-driven
- RS-232, **parallel** in & out ports
- Binary, Intel hex, & Motorola S formats
- 100 user-definable macros
- Information, call **(916) 924-8037**
- 1 Megabit of DRAM
- Made in U.S.A.
- A9 Identifier
- 2 year warranty
- Single pgmr. $550

NEEDHAM'S ELECTRONICS
4539 Orange Grove Ave. • Sacramento, CA 95841
(M-F, 8-5 PST)

MasterCard VISA

CIRCLE NO. 179

Z80 STD USERS!

Cost Effective Upgrade
Clock Speeds to 10 MHz
1 Mbyte On-board Memory

Increase your system performance and reliability while reducing your costs by replacing three of the existing cards in your system with one **Superintegrated** Z80 Card from Zwick Systems.

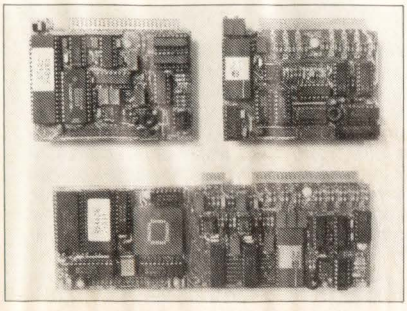
A **Superintegrated** Card in your system protects your software investment, requiring only minor changes to your mature Z80 code. You can increase your processing performance by up to 300 percent in a matter of days!

Approximatly 35 % of each **Superintegrated** Card has been reserved for custom I/O functions including A/D, D/A, Industrial I/O, Parallel Ports, Serial Ports, Fax and Data Modems or almost any other form of I/O that you are currently using.

Call or Fax today for complete information on this exciting new line of **Superintegrated** Cards and upgrade your system the easy way!

ZWICK SYSTEMS INC.
Tel 613-726-1377, Fax 613-726-1902

CIRCLE NO. 180



SBX ANALOG I/O GET A COMPETITIVE EDGE!

Density - up to 16 A/D inputs & 8 D/A outputs on one single width card. **Speed** - throughput rates up to 59 kHz. **Intelligence** - many preprogrammed modes. Input filters, prog. gain amps, sample-holds, FIFO I/O buffers & many other features too numerous to mention here.

ROBOTROL CORP
925 W. San Martin Ave, PO Box 990
San Martin, CA 95046
(408) 683-2000

CIRCLE NO. 181

Multibus II Parallel System Bus Analyzer

PSBA-100 ***A productivity enhancement tool for the system integrator, field service engineer, software, and hardware engineer.***

- Stand-alone, single board computer
- 6U form factor, installs in a single slot
- Built-in, terminal-based user interface
- Supports all four address spaces
- Data capture based on Multibus II protocol
- Fully programmable filter logic uses templates based on Multibus II protocol
- Filter logic supports 16 trigger levels

Multibus II is a trademark of Intel Corp.

PRC

PRC Inc.
1410 Wall Street
Bellevue, NE 68005

For more information and free Demo Disk, Call ....

New Features!

(402) 293-3900

CIRCLE NO. 182

CMOS 186

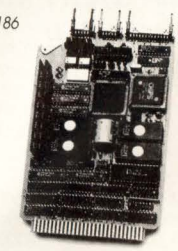
Single Board Computer

MULTI-TASKING

Runs C or QuickBASIC™ Programs

Powerful 16-bit computer directly executes EPROM's containing any C or BASIC .EXE file. NO LOCATORS! Software includes multi-tasking, multi-drop comm, PID control, OPTOMUX.™

- *10, 12, 16 MHz 80C186*
- *CMOS design*
- *512K RAM*
- *384K EPROM*
- *STD BUS Expansion*
- *COM1 RS232/485*
- *COM2, LPT1*
- *RTC Avail*
- *80C187 Avail*
- *OEM discounts*



MICRO/SYS
3447 Ocean View, Glendale, CA 91208
(818) 244-4600 FAX (818) 244-4246

CIRCLE NO. 183

SYSTEM SHOWCASE

EMPLOYMENT OPPORTUNITIES, OUTPLACEMENT AND POSITIONS WANTED

Recruitment Advertising
Sue Shorrock, (508) 392-2185

CAREER CONNECTIONS

Closing Dates for upcoming magazine issues

Issue	Closing
AUG	July 7
SEPT	Aug 4

POSITION WANTED ADS

Free 1" ad to subscribers seeking full-time employment. Just include 50 words of copy and your subscription label. We'll run your ad in 2 consecutive issues. Available to non-subscribers or consultants/companies at $125 per column inch. Mail your position wanted ad to : COMPUTER DESIGN , Positions Wanted, One Technology Park Drive, PO Box 990, Westford, MA 01886

HELP WANTED

COMPUTER PROGRAMMER

Duties: Design, code and debug business application software for the Chinese business community such as restaurants, wholesale/retail stores and import/export companies. Collect business and technical information in order to design software to meet the customers' requirements. Train and give instructions to customers to maintain quality service.

Requirements: Bachelor's Degree in Science majoring in Computer Science. Verbal and written fluency of the Chinese language.

Hours and Salary: 40 hours a week. Monday through Friday. 9:00 am - 5:00 pm. $500.00/week.

Send Resume Only to: Job Service of Florida, 2660 West Oakland Park Blvd., Fort Lauderdale, FL 33311-1347, ATTN: Job Order # FL 0621112.

PROGRAM MANAGER. Are you seeking a Program Manager who gets things done *on time* and *within cost* and *meets customer expectations?* Your search has ended. Track record for last four years: $47M New Business Secured, $2.5M of Extra Profit Generated, 100% On Time Delivery. Contact Joe @ P.O. Box 1413, Massapequa, New York 11758 or (516) 799-1229.

Over 30 years experience in Management of Manufacturing, Quality Assurance and Quality Control of electro-mechanical equipment. Have implemented TQM, SQC, SPC, FMEA, Reliability (MTBF), and ISO 9000 programs. Am immediately available for full-time or temporary employment. Resume on request. Richard Saggese, 37 Stonehenge Dr., Wayside, NJ 07712, (908) 922-0214.

Inside/Outside Plant Engineer (with Fiber Optic training), Manager Supervisor, Inspector. Over thirty years of experience throughout the U.S. Will relocate. Prefer the Carolinas and Southeast. Please call Ken at (518) 869-9728, leave message.

Realtime multitasking S/W specialist 20+ years experience. Languages: C, ADA Assembly, Pascal, Fortran; Operating Systems: VxWorks, VRTX-32, VRTX-32, VRTX-86, OS/2, VAX VMS, PCDOS, MSDOS, pSOS. Seek longterm S/W engineering position. Richard D. Dumas (214) 783-8455.

V.P./Director-level Marketing MAnagement: BSEE. 14+ years of hi-tech strategic/tactical marketing successes with board/system-level products: STDbus, Multibus, and VMEbus. Company associations: Hewlett-Packard, Intel, National, Force. Assertive/creative solution-finding style. Prefer S.F. South Bay, consider other. Steph (510) 659-8739 or P.O. Box 758, Newark, CA 94560-0758.

SENIOR LEVEL MARKETING MANAGEMENT: Expereience grounded in a solid progression of increasing responsibility for product design. My MBA allowed me to apply that experience to marketing assignments from microprocessor families to communications circuits. Expertise covers advertising to sales, and market segments from commodity products to specific market niches. Art Gruszynski (719) 576-3973.

SYSTEMS/PRODUCT DEVELOPMENT: Harware, Software. Firmware. BS Physics/Computer Engineering (GPA: 3.7). MS Manufacturing Engineering/Management (GPA: 3.7). 3 years Telecommunications experience. System Engineering: configuration, installation, orientation. Product Development: functional specification, architectural design, embedded OS development, schematic design, PCB layout, prototyping, troubleshooting. 4 Benmore Court, Plainview, NY 11803. (516) 939-0246. Reggie.

ADVERTISERS INDEX

ADVERTISER	PAGE NO.	CIRCLE NO.
A		
Advanced Micro Devices	8-9	5
Alacron, Inc.	98	52
American Eltec	21	15
Analog & Mixed Signal Conference	112-113	58
Applied Microsystems Corp.	80-81	45
ASIC Conference	106	57
ATMEL Corporation	15	8
Avanti Circuits	116	171
Avocet Systems	18	9
B		
Brooktree Corporation	31	–
BUSCON '92 EAST	89	48
C		
Cable and Computer Technology	13	7
Canon USA	27	18
Chrislin Industries	53	35
Computer Design	94	50
Cypress Semiconductor	CV4	–
† Computer Design	19	12
Computer Design	120	60
D		
Digital Equipment Corp.	6-7	–
Dynatem, Inc.	75	43
E		
Electronic Solutions	1	2
ELMA Electronics	105	56
Embedded Systems Conf.	41	27
F		
John Fluke Mfg. Co.	65	40
Force Computers, Inc.	22-23	16
Franklin Software	116	173
G		
Grammar Engine	117	178
H		
Hewlett Packard	29	19
* Hitachi America, Ltd.	19	11
Huntsville Microsystems	4	4
I		
I-TECH Corp.	117	177
Imagine That	116	174
Integrated Device Technology	11	6
† Intel Corporation	119	59
Intel Corporation	49	–
Intel Corporation	54-55	36
Ironics	24	17
K		
KADAK	20	14
L		
Lightwave	100	54
M		
Macrolink	68	42
MEDO USA	116	169
Mercury Computer Systems	43	29
Micro-Sys	117	183
Microboards, Inc.	104	55
Micron Technology	35	22
Microtec Research, Inc.	56	37
Microware Systems Inc.	47	31
Military & Aerospace Elect	93	49
† Military & Aerospace Elect.	33	20
Mitsubishi Electronics	34	21
Mitsubishi Electronics	51	34
Mitsubishi Electronics	66-67	41
MIZAR	48	32
N		
National Semiconductor	16-17	–
National Semiconductor	96A	–
Needham's Electronics	117	179
Newbridge Microsystems	37	24
Nohau Corporation	116	167
O		
Oasys, Inc.	39	25
OrCAD Systems	118	185
OrCAD Systems	116	168
P		
Pentek	99	53
PRC, Inc.	117	182
Q		
Quantum Software Systems	59	38
R		
RadiSys Corporation	CV2	1
Radstone Technology	45	30
Ready Systems	85	46
Real Time Devices	117	176
Robotrol Corporation	117	181
S		
Signal Processing Group	117	175
Software Development Systems	63	39
Sophia Systems	18	–
Sunrise Electornics	118	184
Synergy Microsystems	2	3
Systran Corporation	116	170
T		
* Texas Instruments	33	–
Themis Computer	83	47
V		
VenturCom	40	26
Vigra, Inc.	36	23
VME Microsystems	76	44
VMetro, Inc.	42	28
W		
Brian R. White Company	20	13
Wind River Systems	87	51
Z		
Z-World Engineering	116	172
Ziatech Corporation	CV3	61
Zwick Systems, Inc.	117	180

Computer Design's INSTANT DATA ACCESS ADVERTISERS

To receive data sheets instantly from these advertisers via FAX, **dial (617) 494-8338** and when prompted, enter the 4 digit document number shown here.

ADVERTISER	Page NO.	IDA NO
ATMEL	15	1045
Computer Design	94	1047
Hitachi	19	1034
KADAK	20	1036
Macrolink	68	1037
Mercury	43	1020
Synergy	2	1042

* Domestic only
† International only

The Advertisers Index is published as a service. The publisher does not assume liability for errors or omissions.

COMPUTER DESIGN Technology and Design Directions

Executive Office: One Technology Park Dr, PO Box 990, Westford, MA 01886
(508) 692-0700 Fax: (508) 692-7780 Telex: 883436
Publisher: David L. Allen (508) 392-2111
Associate Publisher/Editor-in-Chief: John C. Miklosz (508) 392-2114
Associate Publisher/National Sales Manager: Tim L. Tobeck (508) 392-2116
Administrative Assistant: Peg Alexander (508) 392-2112
Marketing Specialist: Betsy Anderson (508) 392-2209
Ad Traffic Manager: Kelly Rice (508) 392-2198
Recruitment Advertising, Postcards/System Showcase: Sue Shorrock (508) 392-2185
Circulation Director: Bob Dromgoole (918) 832-9213
Circulation Manager Paul Westervelt (918) 832-9287
List Rental: Deanna Rebro (918) 831-9551
Reprints: June Bozarth (918) 835-3161

SALES OFFICES

Associate Publisher
Tim L. Tobeck

National Accounts Managers

Eastern/Midwestern Region
Tim Pritchard
One Technology Park Dr
PO Box 990
Westford, MA 01886
Tel: (508) 392-2217
Fax: (508) 692-7780
Telex: 883436

Southwestern/ Northwestern Region
Eric Jeter
19627 I-45 N, Suite 220
Spring, TX 77388
Tel: (713) 353-0309
Fax: (713) 288-8350

Northern California
Diane Palermo
910 Campisi Way
Suite 1B
Campbell, CA, 95008
Tel: (408) 371-7551
Fax: (408) 371-6329

Strategic Accounts Representatives

Eastern U.S.
Sue Nawoichik
One Technology Park Dr
PO Box 990
Westford, MA 01886
Tel: (508) 392-2118
Fax: (508) 692-7780

Western U.S.
David Singer
One Technology Park Dr
PO Box 990
Westford, MA 01886
Tel: (508) 392-2109
Fax: (508) 692-7780

U.K./Scandinavia
David Round
Westmead House
123 Westmead Road
Sutton
Surrey SM1 4JH
Tel: (081) 770-1100
Fax: (081) 770-9779

France/Belgium/ Southern Switzerland/ Spain/Netherlands
Daniel R. Bernard
10, rue Michelet - B.P. 279
78502 Sartrouville Cedex, France
Tel: 01-39-14-67-80
Fax: 01-39-14-70-14

Germany/Austria/Northern Switzerland/Eastern Europe
Johann Bylek
Verlagsbuero Johann Bylek
Stockaeckerring 63
D-8011 Kirchheim/Muenchen
Federal Republic of Germany
Tel: 89-903-88-06
Fax: 89-904-35-26

Italy
Luigi Rancati
Rancati Advertising
Milano San Felice Torre 5
20090 Segrate, Italy
Tel: 02-70300088
Telex: 328601 RANCAD I
Fax: 02-7532354

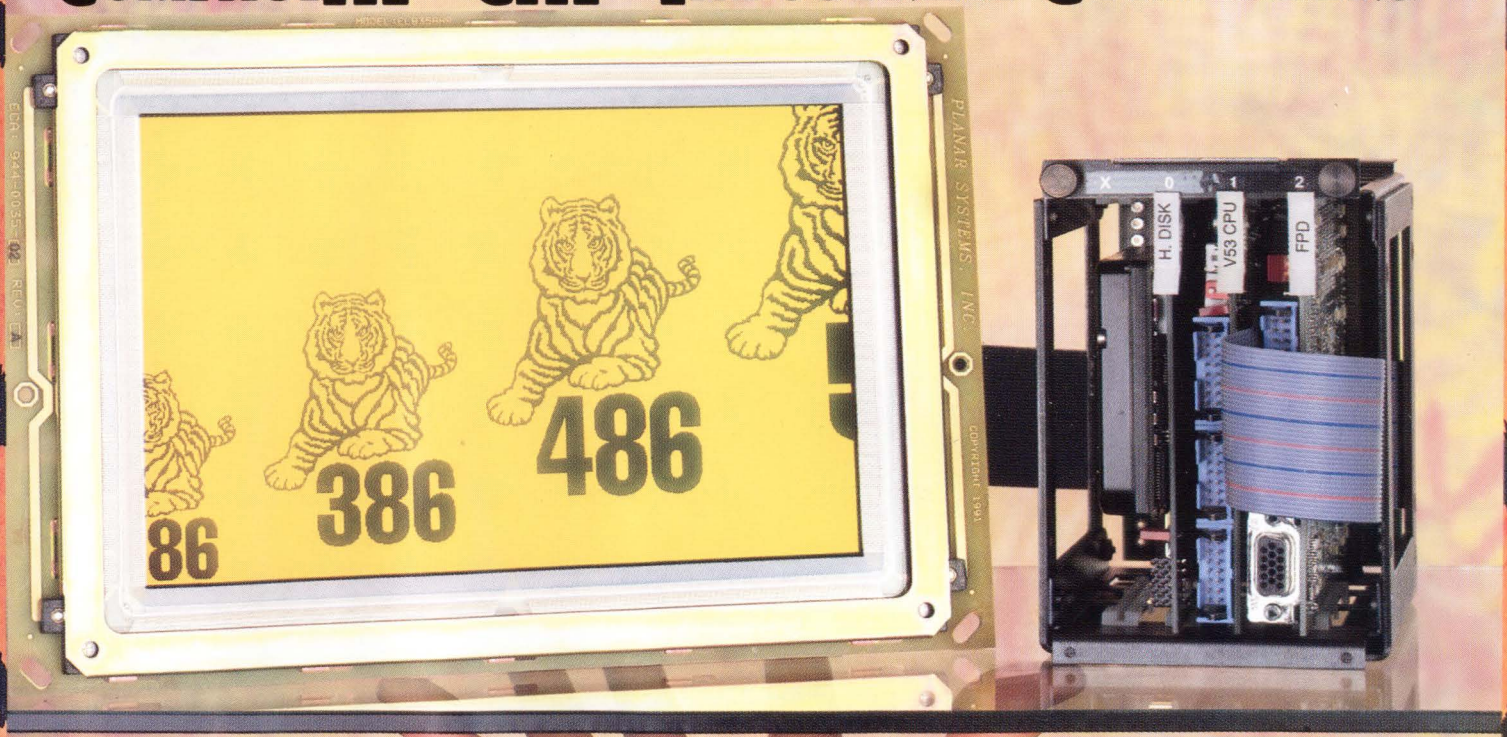
Japan
Toshio Egusa
PubliNetwork
C407, 2-22-6
Tsukuda Chuo-ku
Tokyo 104, Japan
Tel: 03-3536-5404
Fax: 03-3536-5490

Southeast Asia Taiwan/Hong Kong/Korea/ China/Thailand/Philippines/ India/Pakistan/Singapore/ Malaysia/Indonesia/Australia/ New Zealand
Tom Gorman
CCI Asia-Pacific, Ltd
Suite 905, Guardian House
32 Oi Kwan Rd, Happy Valley
Hong Kong
Tel: 833-2181
Fax: 834-5620

COMPUTER DESIGN (ISSN-0010-4566) is published monthly by PennWell Publishing Company, 1421 S Sheridan, Tulsa, OK 74112. Second-class postage paid at Tulsa, OK 74112 and additional mailing offices. Editorial offices are located at One Technology Park Dr, PO Box 990, Westford, MA 01886. Subscription Prices: Free to design and development qualified engineers and engineering managers in the U.S. and Canada. Paid to all others. Qualified engineers and engineering managers outside the U.S. and Canada - air shipped - $85 one year. For non-qualified recipients in the U.S. - $88 one year; in all other countries - air shipped - $154 one year. Call (918) 832-9263 for subscription information. Microfilm copies of COMPUTER DESIGN may be purchased from University Microfilms, a Xerox Company, 300 N Zeeb Rd, Ann Arbor, MI 48106. POSTMASTER: Send change of address form to COMPUTER DESIGN, Circulation Department, PO Box 3466, Tulsa, OK 74101. Officers of PennWell Publishing Company: Frank T. Lauinger, Chairman and Chief Executive; Joseph A. Wolking, President and Chief Executive Officer; John Ford, Senior Vice-President; Carl J. Lawrence, Senior Vice-President; John Maney, Vice-President/Finance; Steve Zimmerman, Vice-President/Corporate Services.

CATS

COMPACTAT "CAT" INDUSTRIAL COMPUTERS



SMALL CAGE, BIG PERFORMANCE

Ziatech's large selection of CAT computers lets you build embedded systems to your exact requirements. The CAT's STD 32® architecture delivers ferocious performance in a variety of compact packages.

ON THE PROWL?

Call or FAX today for a free CAT data sheet

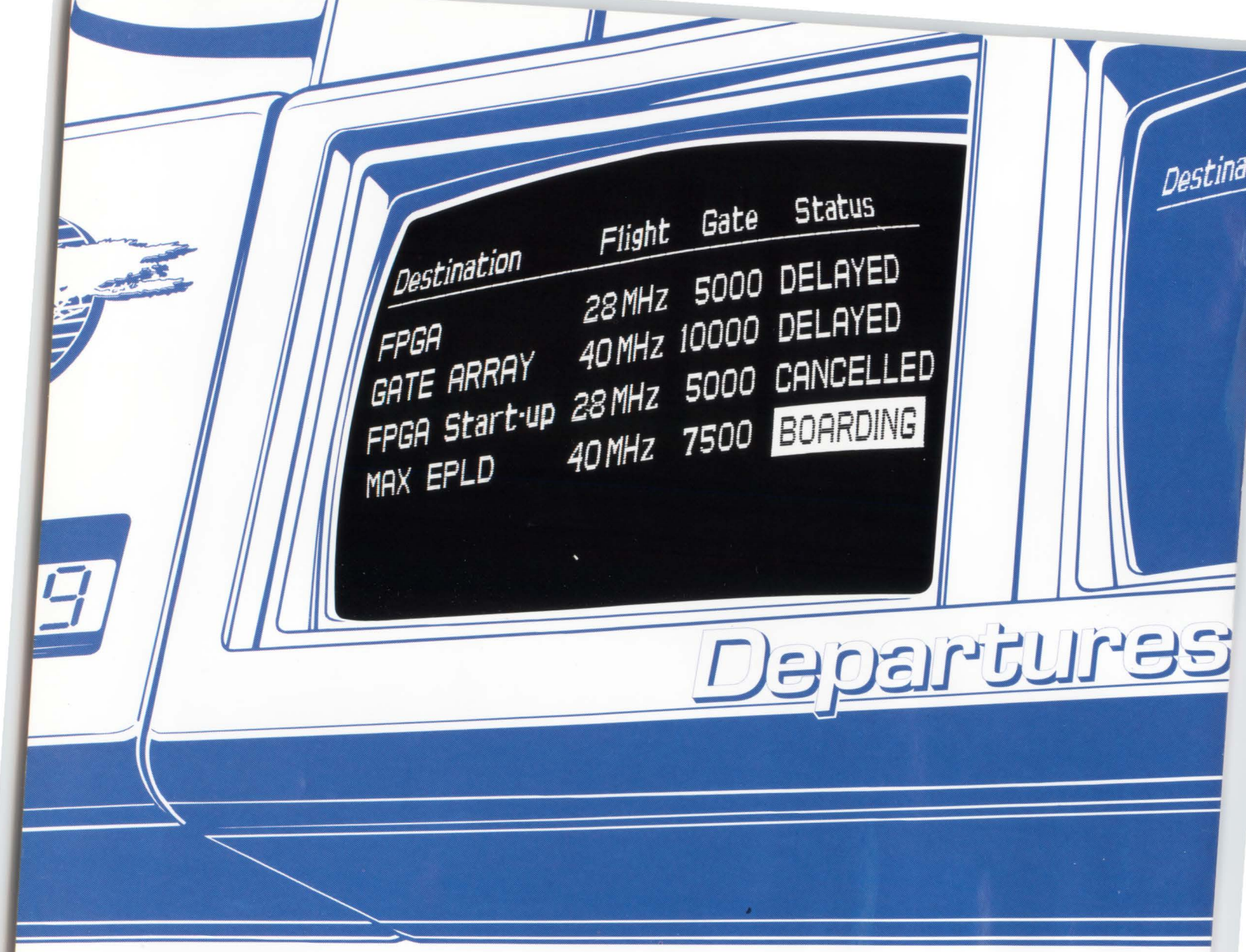
Phone 805·541·0488
FAX 805·541·5088

STD 32®

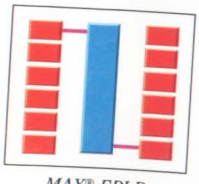
BIG CAT FEATURES

- 16- and 32-bit Industrial PC performance
- Industrial enclosures from 4 to 24 slots
- Multiprocessing, network and industrial I/O options
- Floppy, hard, solid state and PCMCIA storage
- DOS, Microsoft Windows®, OS/2 and UNIX compatibility
- STD 32 performance, STD-80 compatibility

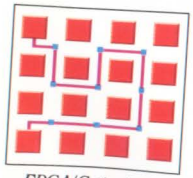
ZIATECH CORPORATION



NOW TAKING OFF—MAX EPLD.



MAX® EPLD Architecture allows full utilization of 7,500 gates.



FPGA/Gate Array Architecture: prepare for lots of delays (speed depends on routing).

The 40 MHz PLD with Gate Array Capacity

If you want PLD design convenience with the density of FPGAs or gate arrays, Cypress has the best way to get you there without delay: our new MAX CY7C341 EPLD.

MAX 341's exclusive Logic Array Block (LAB) architecture always affords you the shortest interconnect path. Data glides between the 12 LABs with a singular, predictable interconnect delay. Count on full, 7,500 gate utilization, with no drop-off from MAX's 40 MHz performance. And MAX 341's nonvolatility and built-in security bit give you extra safety and stability.

Since MAX 341 is a field-programmable EPLD, you cruise above the NREs that can cloud gate array solutions. You save even more in design-in time with MAX's PC-based development kit, which enables you to have a programmed solution in hours, not months.

Catch the entire MAX family of 28-, 44-, 68- and 84-pin devices in both (erasable) windowed ceramic or plastic packages. Call the Cypress hotline today for your free MAX information, including brochure and Data Book. Our Field Applications Engineers are ready to show you how MAX 341 can make your designs fly.

FREE MAX INFO HOTLINE:
1-800-858-1810*
Ask for Dept C111.

CYPRESS SEMICONDUCTOR

*In Europe, fax your request to the above dept. at (32) 2-652-1504 or call (32) 2-652-0270. In Asia, fax to the above dept. at 1 (415) 961-4201. © 1992 Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134. Phone 1 (408) 943-2600. TELEX: 821032 CYPRESS SNJ UD, TWX: 910-997-0753. MAX is a registered trademark of Altera Corporation.