

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

FEBRUARY 1969



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in this issue

POWER CONSIDERATIONS IN HIGH SPEED TTL LOGIC
SELF REPAIR IN A TMR COMPUTER
OPTICAL CHARACTER RECOGNITION

The new Varian Data dual-environment 520/i.



Tag this one to upset the present balance of power and price.

We've hung some other powerful attractions on this system-oriented computer besides that price tag. Two complete sets of hardware registers, including index registers.



They allow the 520/i to run dual programs. A single 1.5 μ s instruction transfers control between programs, or between processing and I/O programs. Data may be manipulated in multiple 8-bit bytes—it'll do arithmetic in 8, 16, 24 or 32-bit lengths within the same program. Program precision is changeable any time.

Hardware includes two 32-bit accumulators, two 16-bit index registers, two program counters, and two overflow registers. Eleven interrupt lines with four hardware priority levels. Expandable 4K to 32K 1.5 μ s memory. IC construction. 50 basic instructions. Interface modules for I/O devices. Proven software. Current delivery: 60 days.

If you're comparing price/performance ratios, 520/i is the new power to be reckoned with—write for your brochure.

varian data machines



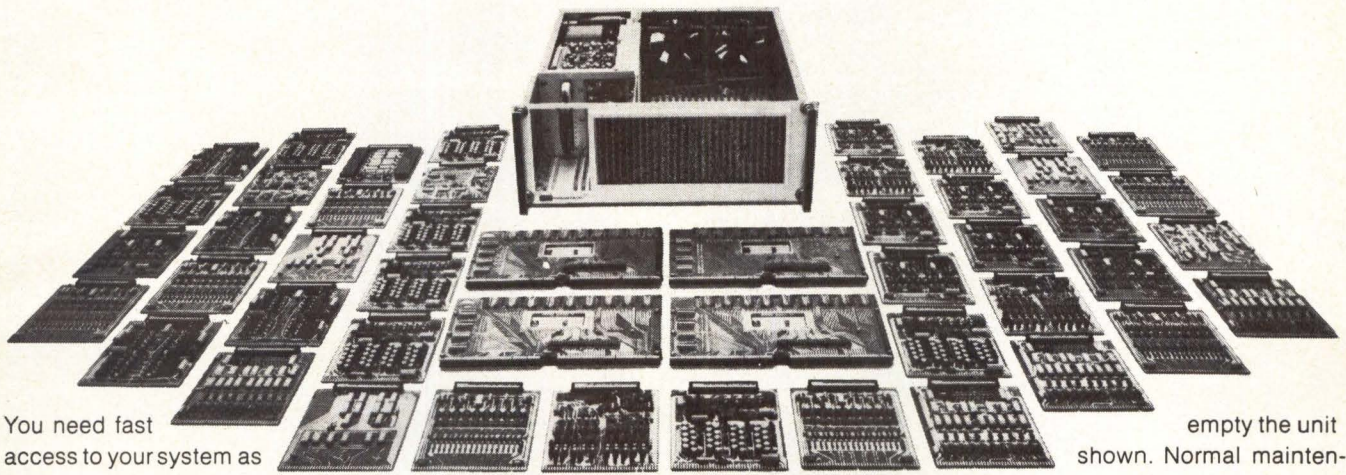
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CIRCLE NO. 1 ON INQUIRY CARD

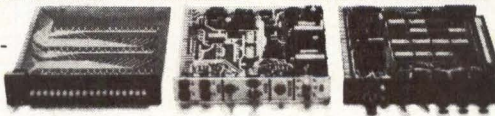
Access time: 6 minutes



You need fast access to your system as well as your information.

Our new medium capacity memory system delivers both. The NANOMEMORY™ 2000 Series has unequalled reliability

and operating margin. It packs up to 295,000 bits of information into a single 2½ cubic foot module (7" x 19" x 21.5"). Multiple units can be used for larger capacities. The basic package includes the power supply, 2½D-organized magnetics, IC electronics and an optional self tester. It does everything bulkier systems do—but does it in less space while delivering cycle times as fast as 650 nanoseconds and access times to 350 nanoseconds. □ Should you need it, physical accessibility is just as outstanding. It took six minutes to



empty the unit shown. Normal maintenance is even faster. All stacks and electronics are mounted on functionally-oriented plug-in cards.

One minute to open the case, then pull a card for easy access to any component. For added convenience, standard parts readily available from your local distributor are used throughout. □ For access to more information on our NANOMEMORY 2650 (650ns cycle time) and NANOMEMORY 2900 (900ns cycle time), please write us.

EM electronic memories

12621 Chadron Ave., Hawthorne, Calif. 90250 (213) 772-5201

CIRCLE NO. 2 ON INQUIRY CARD

You could build mountains out of our logic cards... if you had to

We've got that many. And you could build different kinds of mountains, too. We've got just that product line versatility. Build T²L SUHL I mountains, or T²L SUHL II mountains, or DTL mountains, or 7400 T²L mountains. We can supply enough for you to go as high as you want. And building mountains is a nice way to look at how our micrologic circuit cards are applied. But if you don't want to think in terms of mountains, you can build mole hills, too.

For more information, write or call:
 **CONTROL LOGIC, INC.** 3 Strathmore Road
Natick, Massachusetts 01760 / Tel: (617) 235-1865



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Prof. Bldg., Baker Ave.,

W. Concord, Mass. 01781

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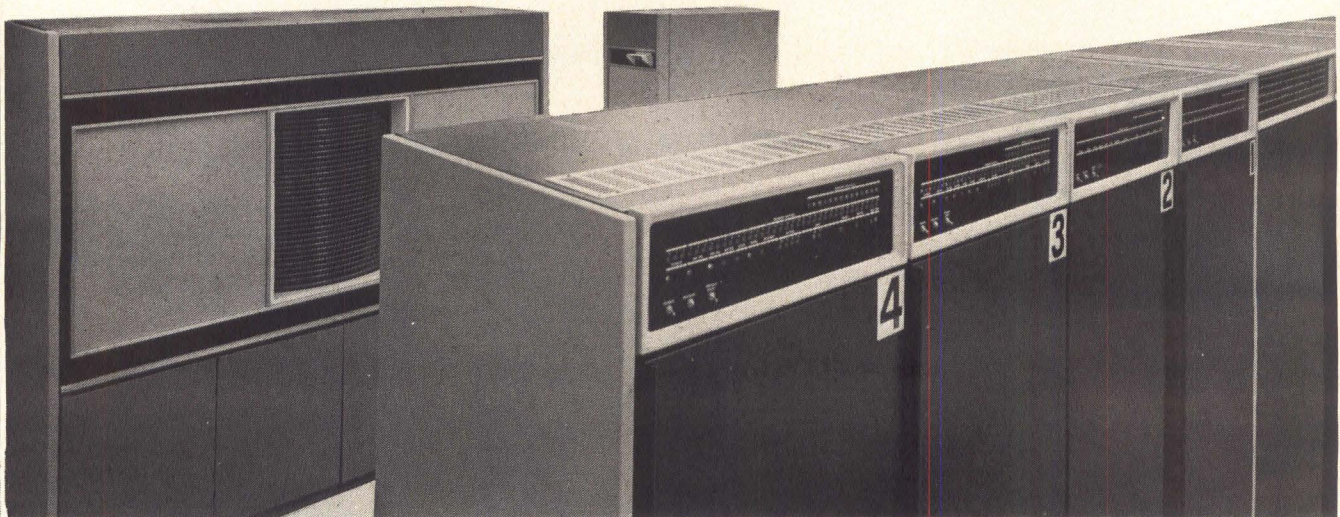
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**Why does
On-line Systems, Inc.
use our
DISCFILE® with their PDP-10?**



Why not...

with the DISCFILE's RELIABILITY and MAINTAINABILITY, the result of Data Product's time-tested, electromagnetic positioner (we've made over 6000 in the last 6 years), On-Line Systems can *stay on-line longer and get back on-line quicker . . .* and with a name like On-Line Systems, isn't that what it's all about?

Want to learn more about how you can plug our DISCFILE into your PDP-10 . . . write to Data Products Corporation, 6219 De Soto Avenue, Woodland Hills, California 91364.

*Data Products manufactures LINE/PRINTER™, DISCFILE®, Core Memories, Off-Line Printer Systems, Card Readers & Punches



"the peripheralists"

MAC is a good deal of computer.

72 instructions including: byte handling, 3-way nondestruct compare, test and skip up to 15 instructions, fast shifts, and optional multiply/divide.

1- μ sec memory cycle time. 16-bit parallel word, 2- μ sec add time. 4K words standard.

Three data channels: Programmed data channel, up to 90KHz. Optional multiplexed data channel up to 333KHz. Optional direct-memory-access up to 800 KHz.

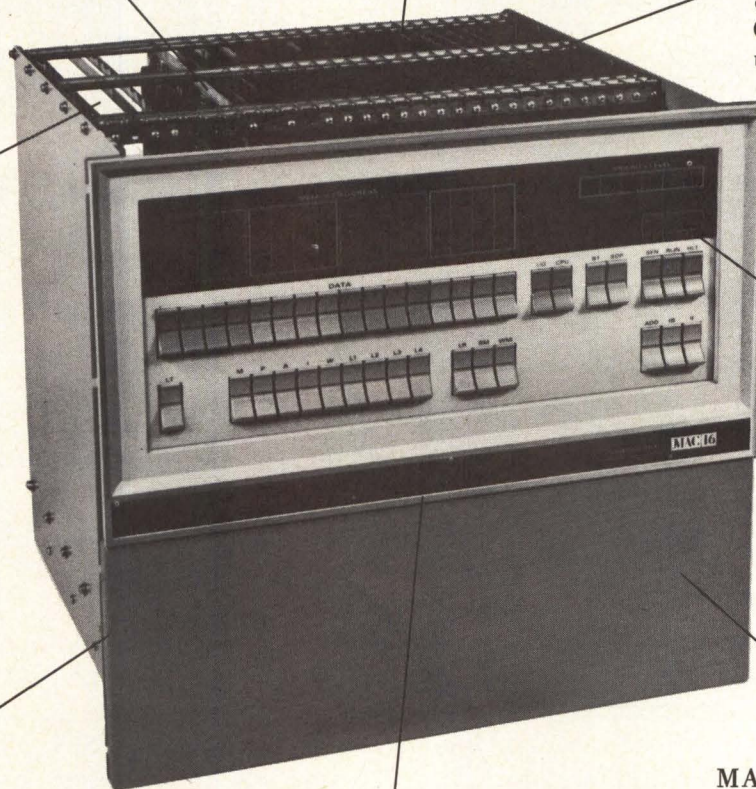
Expansion to 8K words in mainframe. Up to 65K available.

True-nested priority interrupts: 4 levels standard. Expansion to 64 levels. Automatic register save-and-restore, 6- μ sec response.

Third-generation software: LEAP, a two-pass, macro-handling assembler, linking relocatable loader with automatic depaging, debug and edit programs, utility routines, I/O drivers, and diagnostics. LEAP-FORT and MACSIM: Program assembly and simulation on big computers. USASA Standard FORTRAN IV with math library.

MAC 16, with 4K memory, ASR 33, 4 priority interrupts. Ready to operate.... \$11,950.

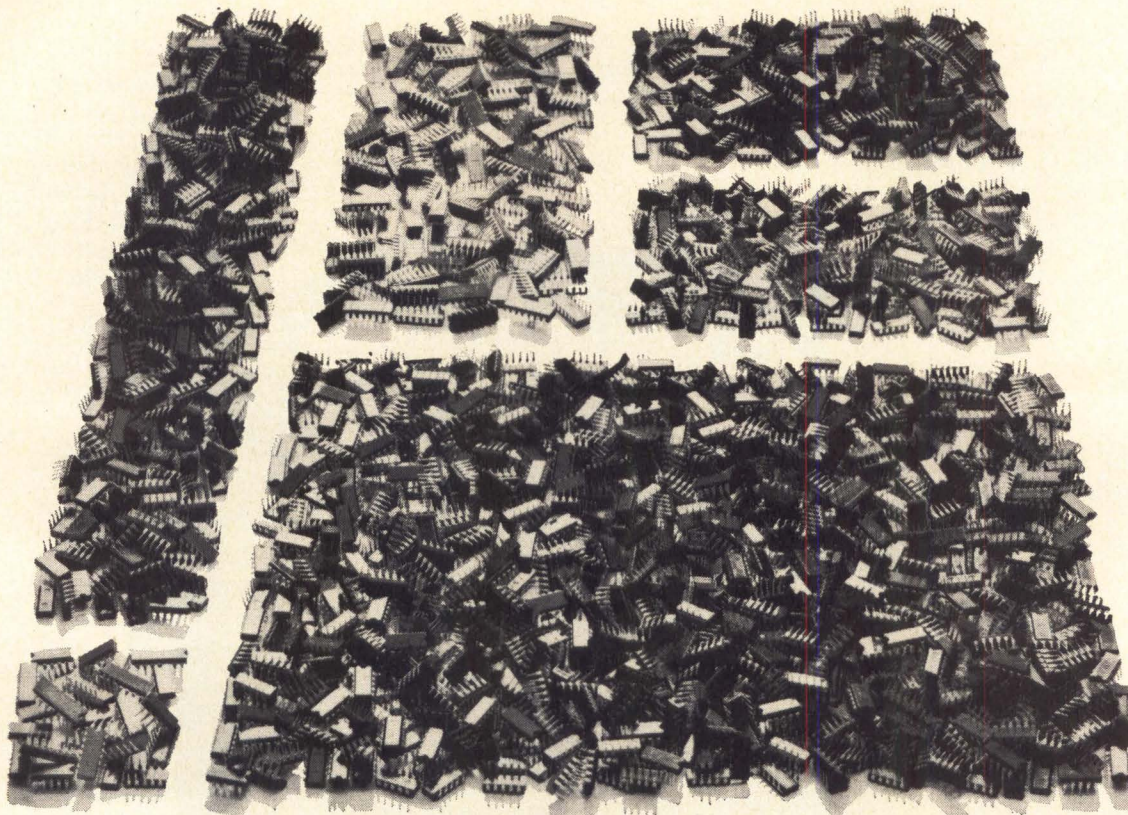
Mainframe space for options. Swing-out front panel, relocatable to remote position. Control-panel programmer aids.



Let MAC do it.

For technical data, write: MAC, Lockheed Electronics Company, Data Products Division, 6201 East Randolph Street, Los Angeles, California 90022.
CIRCLE NO. 5 ON INQUIRY CARD

Fairchild told everyone what MSI could do.

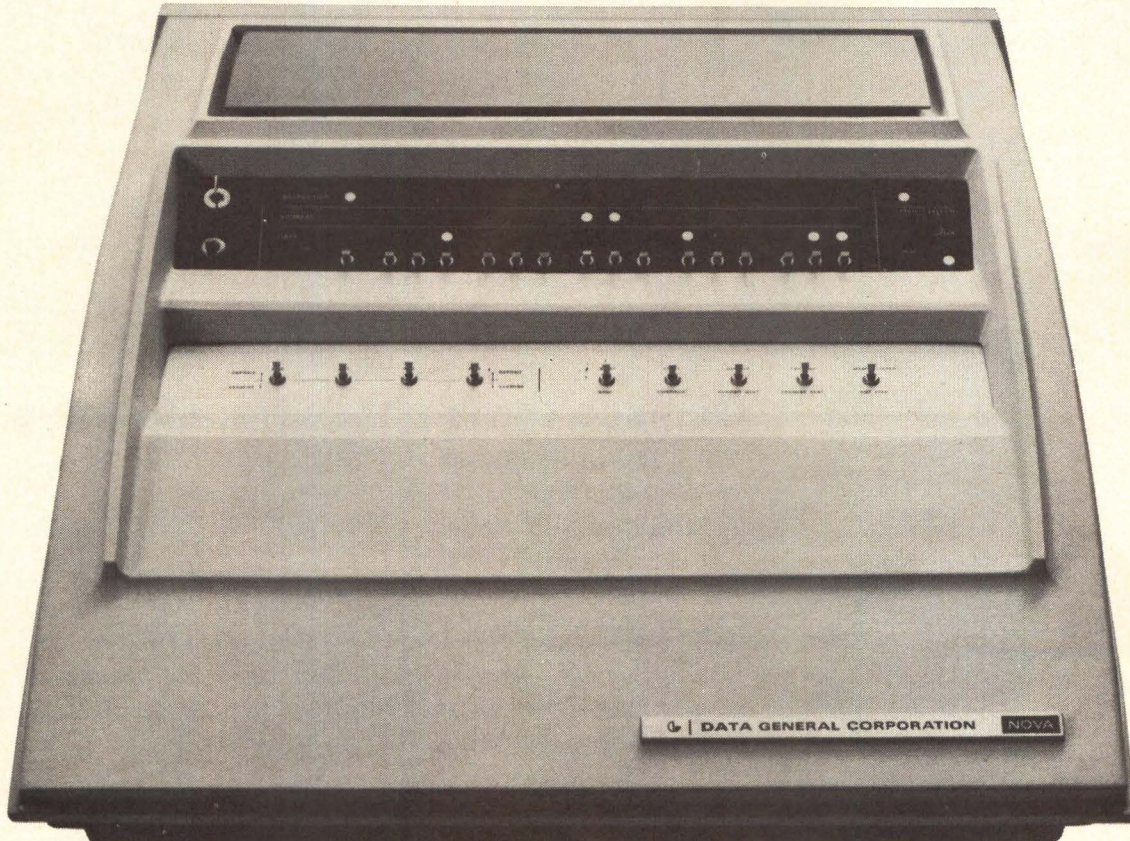


Ever since we introduced medium scale integration in 1967, we've been talking about the systems approach to computer design. Basic, compatible fundamental building blocks that do more jobs than a hundred Integrated Circuits.

Versatile circuits that function like shift

registers, counters, decoders, latching circuits, storage elements, comparators, function generators, etc. We said we had enough MSI device types to build more than half of any digital system you could design. An imaginative company in Boston took us up on it.

We're glad someone was listening.



Data General Corporation built a revolutionary computer with Fairchild MSI circuits. The building block approach allowed them to design and build the whole system in six months. And put it in either a desk top console (shown above) or a 5¼-inch high standard 19-inch rack mount package. The central processor fits on two 15-inch by 15-inch plug-in circuit boards.

Another board houses a 4,096-word core memory. A fourth board provides enough space for eight I/O devices. And there's still enough room left for boards that expand the memory capability up to 16K. Any circuit board can be changed in seconds, so the computer has zero down

time. The NOVA is the world's first computer built around medium scale integration. The first general-purpose computer with multi-accumulator/index register organization. The first with a read-only memory you can program like core. The first low-cost computer that allows you to expand memory or build interfaces within the basic configuration. And the first to prove the price/performance economy of MSI circuitry: The NOVA 16-bit, 4K word memory computer with Teletype interface costs less than \$8,000.

If you'd like more information on MSI, use the reader service number on the opposite page. For specs on the NOVA, use the reader service number below.

FAIRCHILD
SEMICONDUCTOR

FAIRCHILD SEMICONDUCTOR / A Division of Fairchild Camera and Instrument Corporation ■ 313 Fairchild Drive, Mountain View, California 94040, (415) 962-5011 ■ TWX: 910-379-6435

CIRCLE NO. 7 ON INQUIRY CARD

3 good reasons why you should build your own systems' power system:

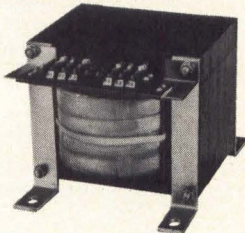
1.



Genisco three phase transformers.

Our three phase transformers are practically all you need to build your primary power system. They come in ranges from 3 to 37.5 KVA, either open or enclosed.

2.



Genisco Control Transformers.

These dry type transformers can do the secondary power system job. Three different groups to choose from. Ratings from 0.250 to 5.00 KVA.

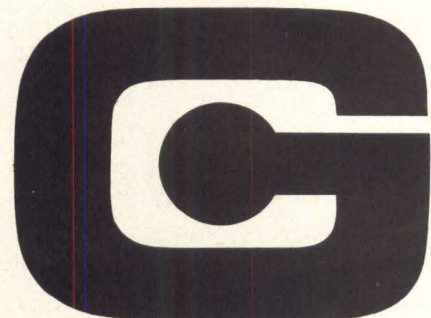
3.



Transient free switch/controller.

This handy device makes sure that all switching on or off occurs at zero crossovers. That way noise-generating discontinuities are eliminated.

Put these components together, add a few transistors and diodes, and you have your own, built in-house power supply. No need to pay someone else to do it. For more reasons why you should build your own consider economy, suitability, availability, and complete control over your product. For more information on our products, circle the reader service number shown below.



Now get IC Op Amp power...

with high gain and high voltage

RCA has these two monolithic OP AMP units for you—ready to meet your design requirements for high input impedance, high gain and high power output. Only the price isn't high! Ask your RCA Distributor for his price and delivery. Write RCA Electronic Components, Commercial Engineering, Section IC-ZB-2 Harrison, New Jersey 07029 for Data Sheet.

All characteristics below are typical

Power output (8% THD)
Output swing voltage (P-P)
Input impedance
Open-loop Gain
Input Offset Voltage
Input Offset Current
Input Bias Current
Slew Rate

RCA-CA3033
for $\pm 12V$ Supply

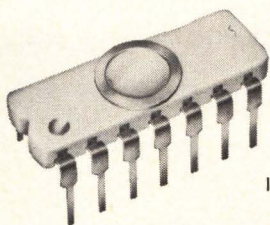
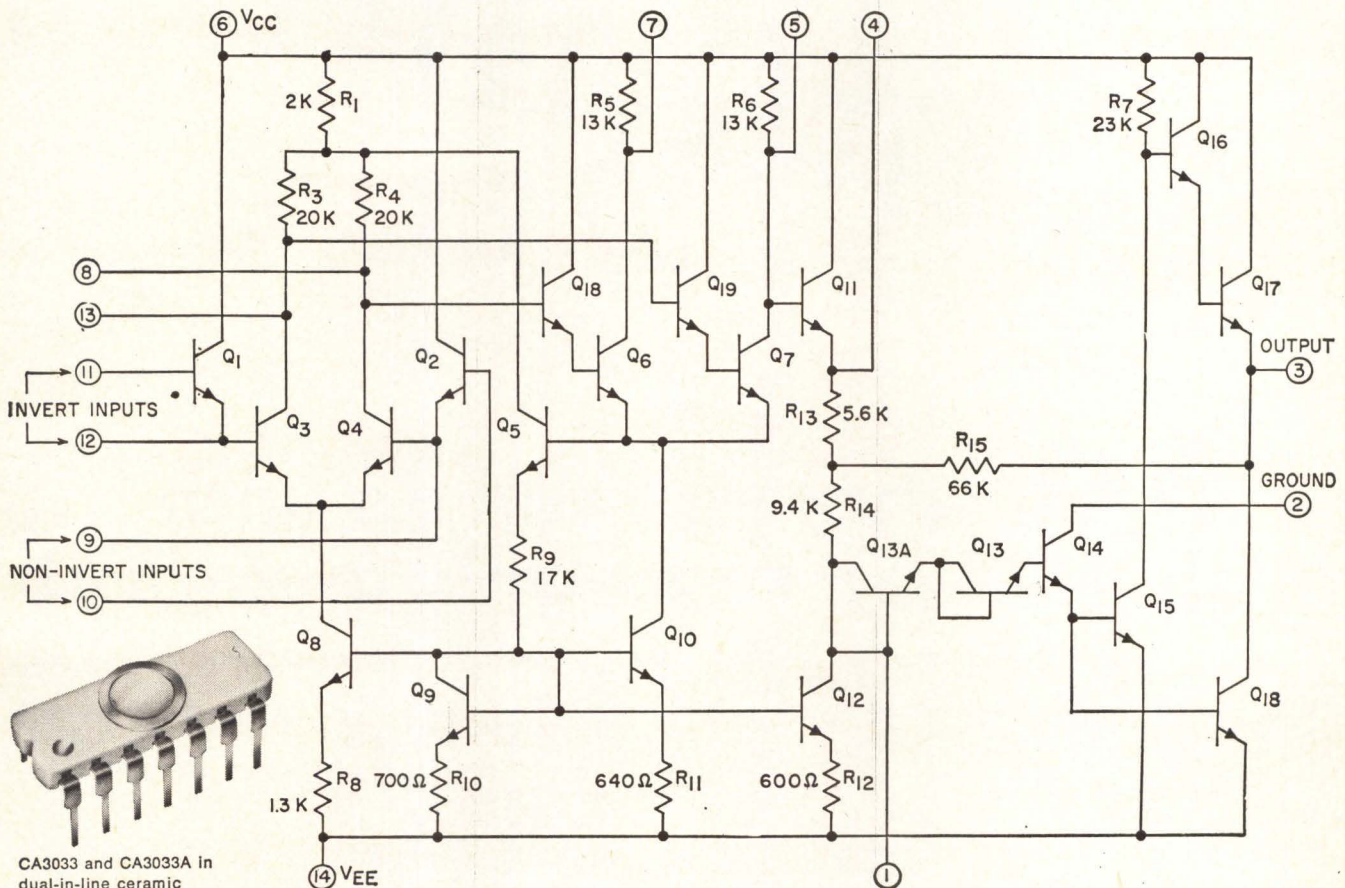
122 mW
21V
1.5 M Ω
90 dB
2.6 mV
5 nA
83 nA
1.2V/us

RCA-CA3033A
for $\pm 18V$ Supply

255 mW
32V
1 M Ω
96 dB
2.9 mV
9 nA
103 nA
2.5V/us

\$3.95 (1000 units)

\$4.95 (1000 units)



CA3033 and CA3033A in dual-in-line ceramic package (-55° to $+125^{\circ}C$ operating temperatures)

RCA
Integrated
Circuits

Now in plastic packages at economy prices.

CA3033 now available in dual-in-line plastic as CA3047 at \$1.95 (1000 units)
CA3033A now available in dual-in-line plastic as CA3047A at \$2.95 (1000 units)

CIRCLE NO. 9 ON INQUIRY CARD



Think what you can do with MOS 1024-bit read-only memory!

Start with the basic Philco-Ford pM1024 memory. Pattern organization can be 128 eight-bit words or 256 four-bit words. With built-in chip select, you can parallel chips to build up any desired bit capacity.

And what can you get?

Look-up tables, for instance. The off-the-shelf pM1024 is programmed with a sine table. By custom masking, the pM1024 can be programmed to read cosine, tangent, log, exponential or other commonly used functions.

Or you can have a synched 8-signal waveform generator. Or a character generator. Or microprogramming of subroutines.

Or you can solve recurrent equations having variables of known interaction.

Speed? Cycle times of 1 and 2 microseconds are available. Cost? Less than 5¢ per bit.

Turnaround? We transfer your custom bit pattern to the chip through the use of computerized software, with complete accuracy . . . and promptly.

Address decoding, memory and output buffers are all contained on the chip. Output drives DTL or T²L directly.

Get complete facts now, by writing to John Kitzrow, MOS Marketing, Philco-Ford Microelectronics Division, Blue Bell, Pa. 19422, or call 215-646-9100.

PHILCO 

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CIRCLE NO. 10 ON INQUIRY CARD

**MODULAR DESIGN MEANS
MAINTENANCE-FREE
SERVICE... WITH MDS
CARD PUNCH CONSOLES**



MDS 6011
CARD PUNCH COMPACT CONSOLE

MDS Card Punch Consoles are designed with interface and performance capabilities compatible with most computers and communication systems.

MDS Punched Card equipment features modular design... your assurance of simplified maintenance and long-term reliability. Card punch heads are sealed, oil-filled mechanisms insensitive to environmental conditions. Interface, control circuits and power supplies are included.

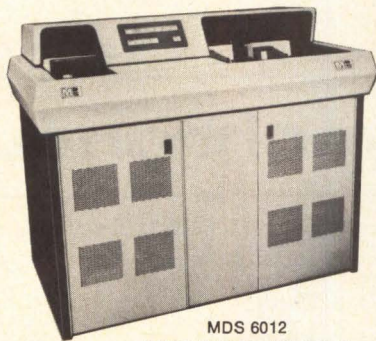
The MDS 6011 Card Punch Compact Console is a complete self-contained unit, ideal for mobile applications as well as typical fixed data handling installations. The card punch is matched to a complete card transport system with 1000 card capacity hopper and stacker. Throughput of 200 cards per minute. Cards are end-fed, column "1" first.

MDS 6012 Card Punch Console has interface and performance characteristics like those of the 6011. Modular deck assembly and electronics are designed to allow pre-read and/or post-read stations to be incorporated as options.

Ask for information on the MDS 6014... includes a card reader station incorporated ahead of the punch station.

Ask for: The MDS folder-file on MDS 6011, 6012, 6014.

FOR MORE — MEET YOUR MAN FROM MDS



MDS 6012
CARD PUNCH CONSOLE

MOHAWK^{MS}
DATA SCIENCES CORPORATION
OEM MARKETING

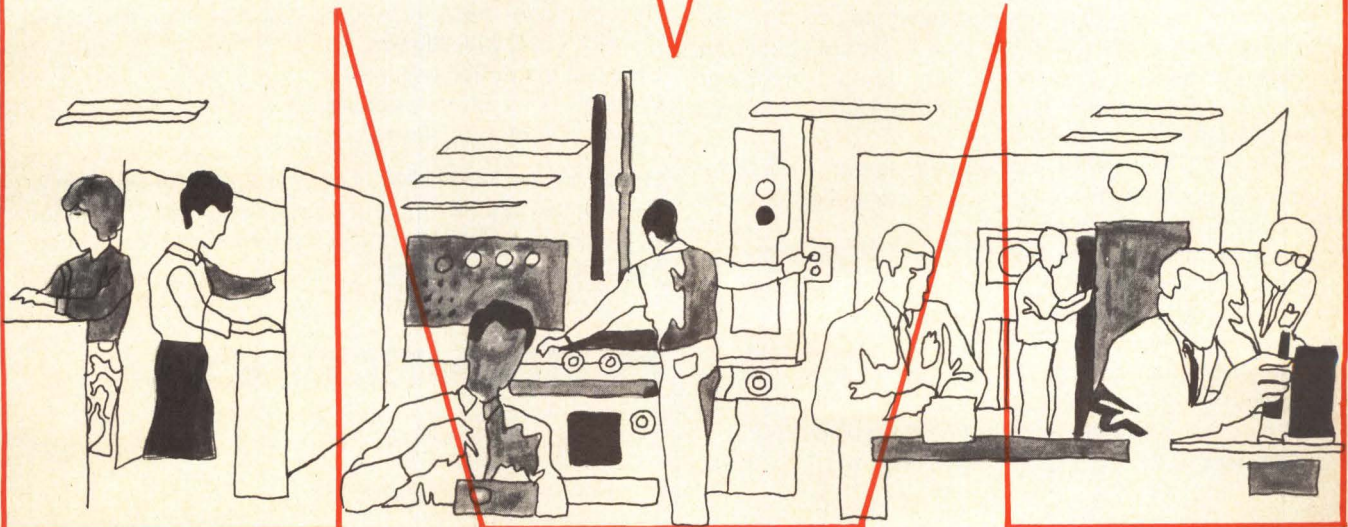
122 EAST RIDGEWOOD AVENUE • PARAMUS, N.J. 07652
Telephone 201/265-7333

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DIGITAL STRIP PRINTERS • BUFFERED TAPE UNITS
HIGH-SPEED AND LOW-SPEED LINE PRINTERS
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PAPER TAPE PUNCHES AND READERS

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CIRCLE NO. 11 ON INQUIRY CARD



now-Kennedy goes synchronous

Not content with being first in incremental recording, we've gone synchronous at Kennedy.

Our Model 3100 Continuous Magnetic Recorder offers the small computer user all the features of big, expensive transports, but at sensible low prices. Now it is possible to have full magnetic tape capability without spending several times the cost of your computer.

Operating at synchronous speeds up to 25 ips, the Model 3100 has a high performance single capstan drive matched to the reel servos for fast, accurate start/stop.

Read/write rates up to 20 Hz can be accommodated at 800 BPI. Tape motion is bidirectional with no program restrictions.

Forward and reverse high-speed search operations can be accommodated at 120 ips. Tape motion is under capstan control at all times.

Exceptionally easy to interface, the Model 3100 with write electronics provides write clock signals appropriate for the speed and density ratings as well as time delays for gap generation.

Model 3100 is available as transport only, or with any combination of Read and Write electronics. Seven track and nine track models are all fully IBM-compatible.

Reel size of the 3100 is 8½" (1200 feet) and 10½" (2400

feet) reels are available on Model 3110, which is essentially identical except for size.

Model 3100/3110 specifications:

Normal tape speed—up to 25 ips.

High tape speed—120 ips.

Drive direction—bidirectional.

Start/stop time—10 msec.

Record mode—NRZI-IBM compatible seven or nine track.

Density—200, 556, 800 BPI.

Program restrictions—none.

Write clock—internally generated.

Gap time—internally generated.

Prices for the Model 3100 begin at \$2600 for deck only. Electronics prices are correspondingly low. Write or phone for complete information and for the 36-page catalog of Kennedy products.

KENNEDY CO.

540 WEST WOODBURY ROAD, ALTADENA, CALIFORNIA

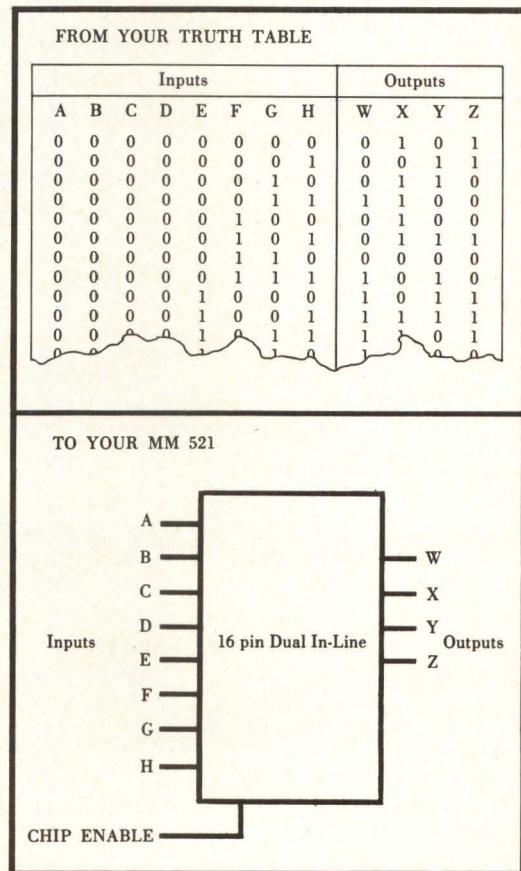
With a memory like this, you can forget the logic

Use the logic easily programmed into our ROM (Read Only Memory) elements. With a minimum of time (typically four weeks versus the twelve required for new custom logic elements), we can set up the simple interconnection metalization pattern your needs dictate and start shipments. Costs about a thousand dollars versus the forty thousand new logic elements run to. And there's every probability that your production run elements will cost less too.

ROM elements are far simpler to make than a new, untried logic design. They're highly repeatable and proven reliable. No logic race conditions; no logic circuit debugging. And our new MOS ROM elements are fast, 500 nanoseconds, the fastest available. They operate from +12 and -12 volt supplies. Easily compatible with conventional DTL and TTL.

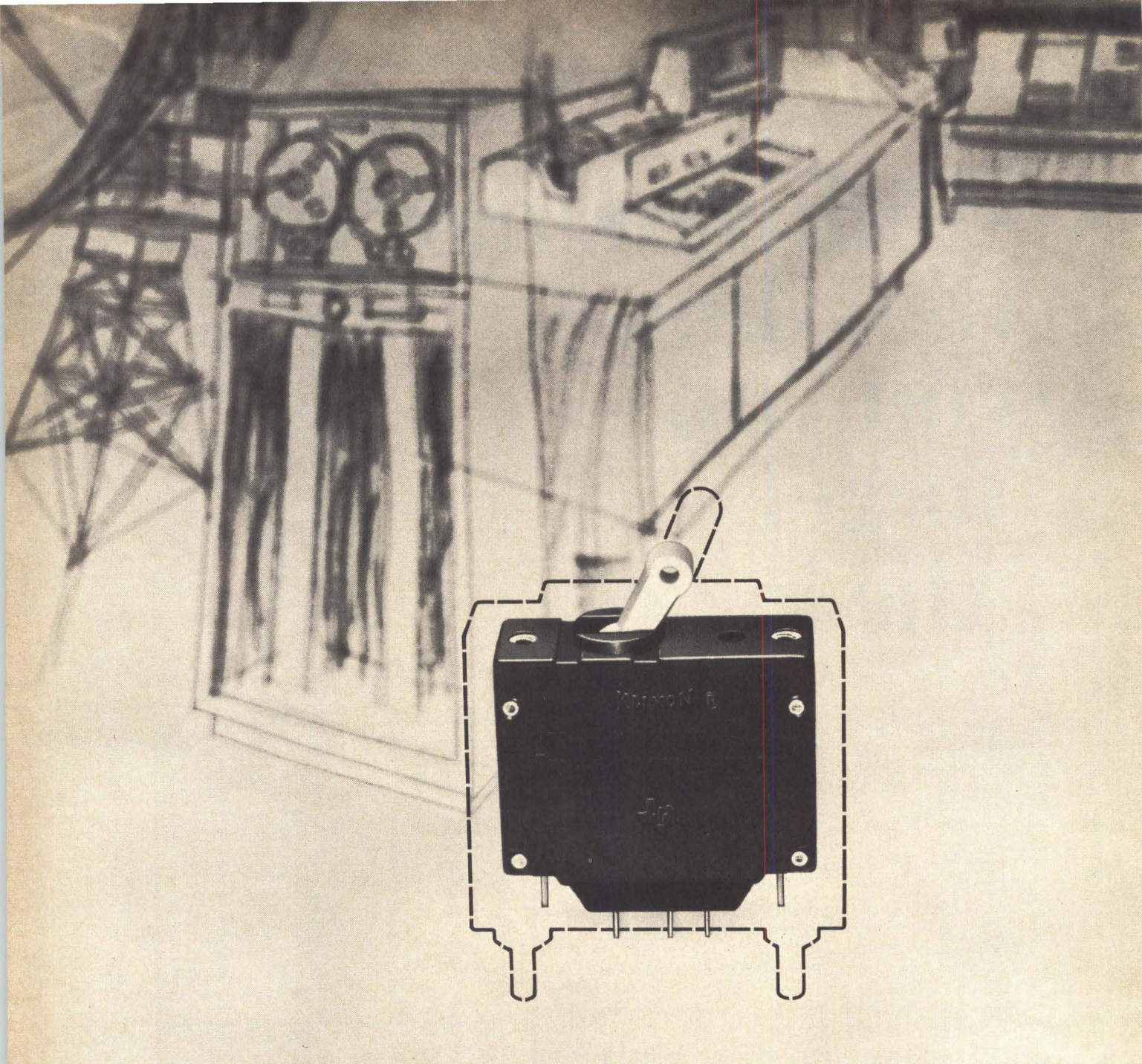
MM521 is a 1024 bit element (256 x 4) 16 pin Dual In-Line device selling for \$45.00 in 100 quantity. MM522 is a 1024 bit element (128 x 8) 24 pin Dual In-Line at \$60.00. Our 500 series MOS are specified at -25°C to +70°C. Full temperature range (-55°C to +125°C) is also available.

We're building a memorable packet of information for logic designers. For the complete set, write or call National Semiconductor, 2975 San Ysidro Way, Santa Clara, California 95051. (408) 245-4320. TWX: 910-339-9240. Cables: NATSEMICON.



National

MOS



The paradoxical circuit protector.

It's a brand new TI product. Yet, it offers you the benefits of a 5-year history of success. How come?

Very simple. Our new 51MC magnetic circuit breaker is the low-cost miniature version of our 4MC which advanced the state of the art five years ago with its smaller, lighter, simpler mechanism.

Our design engineers took that time-tested mechanism and

squeezed it into a 25% smaller package without affecting its superior operating characteristics. Faced with the same miniaturization problem, other manufacturers started from scratch.

Because of its predictable performance, we can guarantee that our new miniature 51MC . . . rated at 0.020 to 50 amps . . . will reliably perform in computers, power sup-

plies, business machines, communication equipment and allied electronic applications.

Bulletin CIRB 35 contains all the data on our new 51MC Series magnetic circuit breakers. Write for your copy today to TI Control Product Division, Attleboro, Massachusetts 02703, or phone (617) 222-2800.

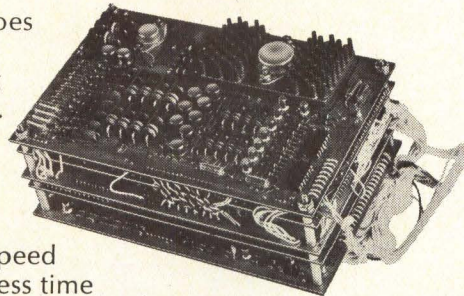


TEXAS INSTRUMENTS
INCORPORATED

CIRCLE NO. 14 ON INQUIRY CARD

Ugly is only skin deep.

Handsome is as handsome does . . . and our new 420 Buffer Memory does an outstanding job in spite of its appearance. We could have made it prettier, of course. But we wanted to keep the size down. And the price. So we concentrated on things like speed (4.0 usecs full cycle, with access time of 600 n.s.) . . . performance (20,000 hours MTBF) . . . capacity (1024 words x 8 bits per word) . . . and design (TTL integrated-circuit logic).



The really beautiful thing about the 420 is its versatility. It's ideal for just about any buffer operation where data comes in bursts that can't be absorbed by I/O equipment. Like data-conversion jobs in information terminals . . . numerical control devices on automated machine tools . . . unusual applications such as highway toll-collection systems . . . process control . . . medical electronics. *Ad infinitum*. Comes with or without address and data registers, too. (Either way, two 420's will just about fit into a shoebox.) Operating environment? 32 to 140° F., 0% to 90% R.H. without condensation.

For more facts on the 420, or for help with application problems, contact a Fabri-Tek man at one of our national or international offices. Or write or call us direct.

Fabri-Tek is a leader in advanced memory research, development and production. Our experienced Applications Engineers are ready to help you find solutions to problems in the following areas: Main Memories • Buffer Memories • Scratch Pad Memories • CRT Refresher Memories • Peripheral Mass Memories • Mil-Spec Memories • Extension of Main Memory • Numerical Control.



FABRI-TEK



Need a wild card to complete your logic system?

... gray code logic, arithmetic/logic, pulse synchronizers, excess 3 counters, multi-function cards ... all the wild ones are *standard* with CAMBION. Our constantly expanding deck currently contains over 300 different logic assemblies, enough to build complete systems without ever having to design that special card. Fast — money-saving.

The CAMBION pack won't go out-of-play either. It's designed with medium scale integration capabilities built right in. The exclusive 70-pin input/output edge connector gives you tighter packaging, more functions per card, and tomorrow's product today.

All CAMBION logic assemblies are functionally and physically compatible. Because we put more on a card, you use fewer cards, need

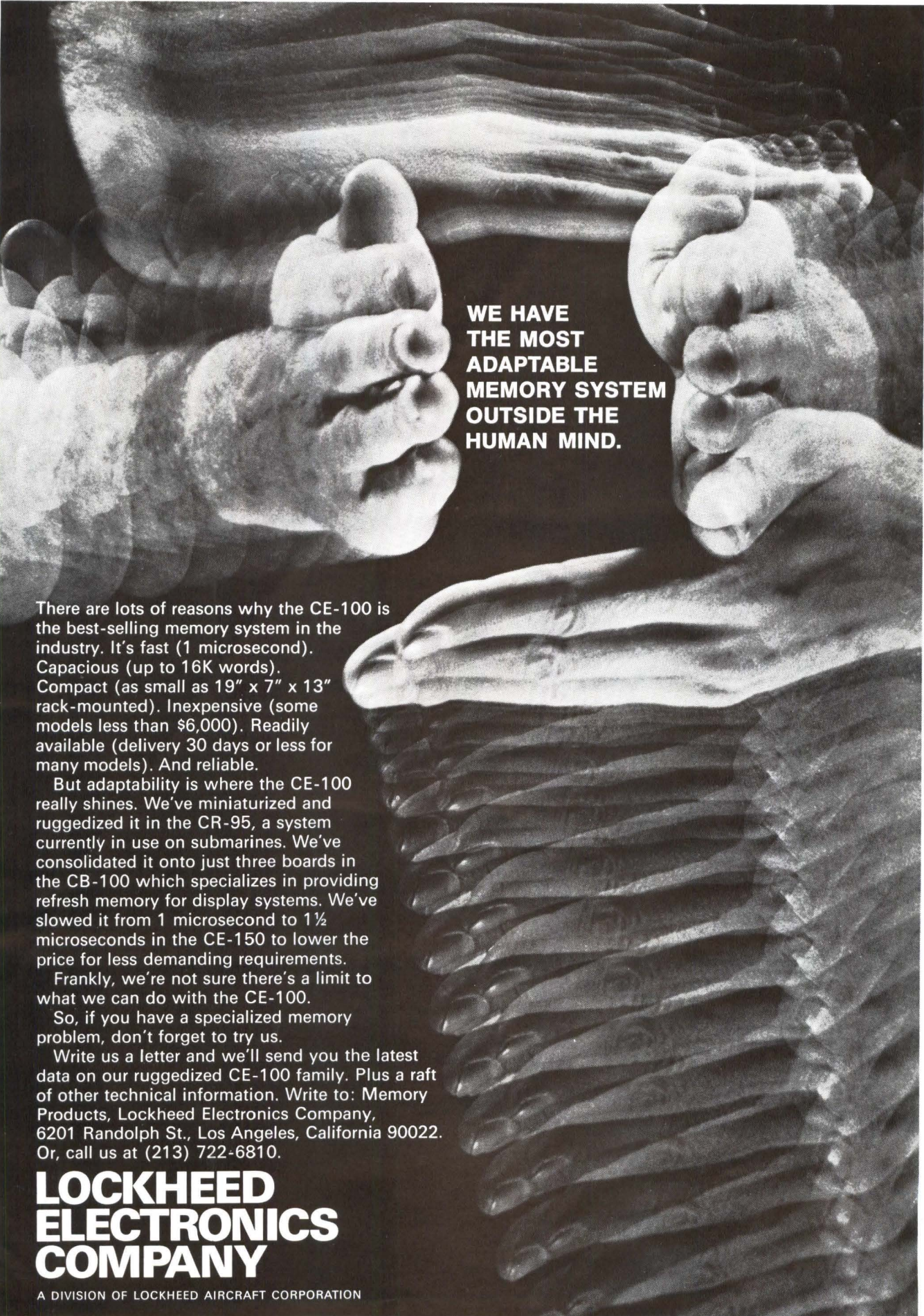
CIRCLE NO. 16 ON INQUIRY CARD

less racks, fewer panels, less cabinets, less space and fewer bucks in the total.

You'll want the right manual to learn the latest rules of the game. If hardware is your requirement, we've got still another book for that. Just circle the number below or write us direct. They're Free, of course. Cambridge Thermionic Corporation, 445 Concord Avenue, Cambridge, Massachusetts 02138. Phone: (617) 491-5400. In Los Angeles, 8703 La Tijera Boulevard, 90045. Phone: (213) 776-0472.

Standardize on

CAMBION[®]
the guaranteed logic assemblies



**WE HAVE
THE MOST
ADAPTABLE
MEMORY SYSTEM
OUTSIDE THE
HUMAN MIND.**

There are lots of reasons why the CE-100 is the best-selling memory system in the industry. It's fast (1 microsecond). Capacious (up to 16K words). Compact (as small as 19" x 7" x 13" rack-mounted). Inexpensive (some models less than \$6,000). Readily available (delivery 30 days or less for many models). And reliable.

But adaptability is where the CE-100 really shines. We've miniaturized and ruggedized it in the CR-95, a system currently in use on submarines. We've consolidated it onto just three boards in the CB-100 which specializes in providing refresh memory for display systems. We've slowed it from 1 microsecond to 1½ microseconds in the CE-150 to lower the price for less demanding requirements.

Frankly, we're not sure there's a limit to what we can do with the CE-100.

So, if you have a specialized memory problem, don't forget to try us.

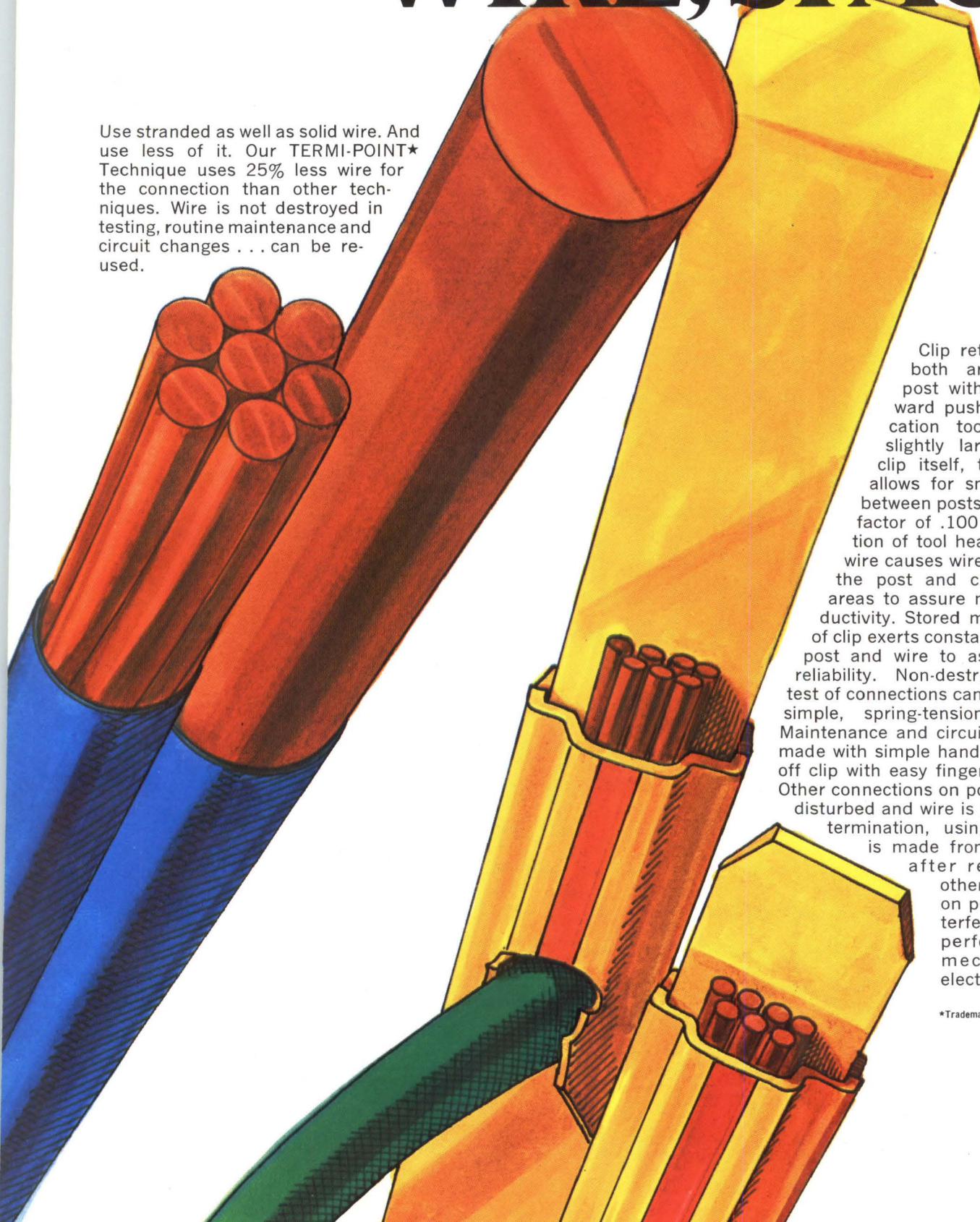
Write us a letter and we'll send you the latest data on our ruggedized CE-100 family. Plus a raft of other technical information. Write to: Memory Products, Lockheed Electronics Company, 6201 Randolph St., Los Angeles, California 90022. Or, call us at (213) 722-6810.

**LOCKHEED
ELECTRONICS
COMPANY**

A DIVISION OF LOCKHEED AIRCRAFT CORPORATION

The better point-to-point WIRE, SPACE,

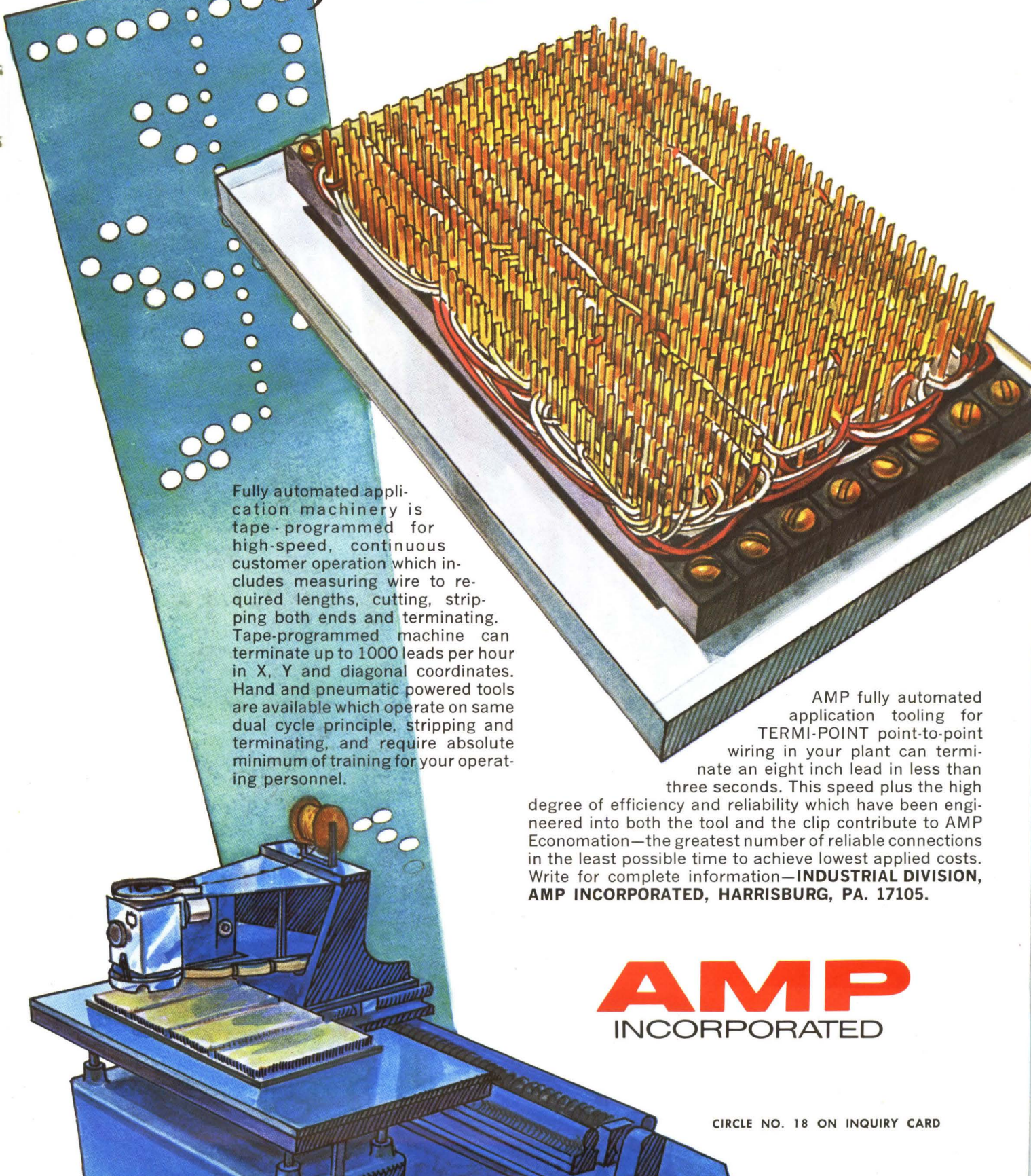
Use stranded as well as solid wire. And use less of it. Our TERMI-POINT★ Technique uses 25% less wire for the connection than other techniques. Wire is not destroyed in testing, routine maintenance and circuit changes . . . can be re-used.



Clip retains wire and both are affixed to post with straight, forward push of the application tool head. Only slightly larger than the clip itself, the tool head allows for smaller spacing between posts with a density factor of .100". Forward action of tool head on clip and wire causes wire to wipe along the post and create "clean" areas to assure maximum conductivity. Stored memory design of clip exerts constant pressure on post and wire to assure long-life reliability. Non-destructive tensile test of connections can be made with simple, spring-tension hand tool. Maintenance and circuit changes are made with simple hand tool that flips off clip with easy finger-twist motion. Other connections on post are left undisturbed and wire is reusable. New termination, using same wire, is made from top of post after repositioning other connections on post without interfering with their performance and mechanical and electrical stability.

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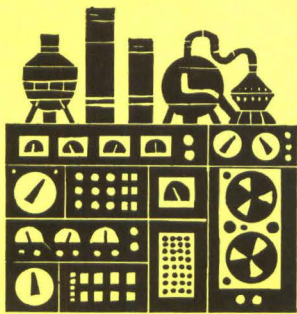


Fully automated application machinery is tape-programmed for high-speed, continuous customer operation which includes measuring wire to required lengths, cutting, stripping both ends and terminating. Tape-programmed machine can terminate up to 1000 leads per hour in X, Y and diagonal coordinates. Hand and pneumatic powered tools are available which operate on same dual cycle principle, stripping and terminating, and require absolute minimum of training for your operating personnel.

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CIRCLE NO. 18 ON INQUIRY CARD



INDUSTRY NEWS

COMPUTER INDUSTRY IN 1969—

The computer industry can expect a continuing lull in major hardware breakthroughs during 1969, according to Isaac L. Auerbach, President of the Auerbach Corporation, an international systems-design and computer consulting firm.

Commenting recently on the industry outlook for the coming year, Mr. Auerbach explained, "There is a growing realization that technology for technology's sake alone is not sufficient. In a high-cost, capital equipment-type industry such as this, the introduction of major change has impact only if such change has significant economic value."

As an example, Mr. Auerbach cited speculation of a dramatic reduction in the cost of transistorized circuitry within the computer.

"Even assuming that this could be accomplished," he said, "it would not have any real economic significance

since the central computer circuitry accounts for less than ten percent of the total cost of the computer installation to the customer. To spend hundreds of thousands of dollars, or even millions, for developing the technology and for tooling will not result in a dramatic economic saving. More effort should be channeled into the development of new applications utilizing existing equipment and know-how, and into improved means of communicating with the computer—that is, the man-machine interface."

In a positive vein, Mr. Auerbach listed two main areas in which he expects solid growth during the immediate future.

In the field of computer-assisted instruction, he said, "We shall see the continuing evolution of techniques that improve the ability to learn and the ability to provide instruction supplemental to that offered by the conventional teacher." He stressed as a challenge to the industry the develop-

ment of new material for use in computer-aided instruction, citing the fact that "the whole concept of this application is still subject to experiment. I feel, however, that in time the field of education will wholeheartedly accept and adapt to these new devices and techniques, thus opening a market that will burgeon in the future."

Another area of anticipated growth is the commercial process-control field.

"I believe," he said, "that we will see a rapid rise in applications that enable us to accomplish functions previously impossible in this field.

"In 1960," Mr. Auerbach continued, "I predicted that pneumatic control devices, known today as fluidics, would be a growing technology deserving careful observation and study. This has proven true, and today this technology continues to have an increasing impact because of the very significant decrease in cost and increase in reliability which such devices make possible."

HONEYWELL AGAIN EXPANDS KEYS TAPE—

The second major expansion in six months of Honeywell's family of Keytape computer data preparation units has been announced by the automation firm's Communications and Data Products Division.

The addition of 16 models rounds out the multi-purpose capabilities of these keyboard-to-magnetic tape data preparation units, said Thomas B. O'Heir, Keytape product manager. There are now 52 models in the Keytape family—26 for 7-channel tape and 26 for 9-channel tape.

Keytape units, designed to break through the punched card bottleneck of feeding information to computers, increase data preparation production an average of 25 to 35 per cent, reduce operator error and fatigue, and increase input of data to a computer from 300 to 1,000 per cent, O'Heir said.

Honeywell entered the off-line data preparation market in January 1968 when it introduced its first eight Keytape models—four each for transcribing data on 7-channel and 9-channel magnetic tape. The family was expanded in June with the addition of 28 models—14 for 7-channel tape and 14 for 9-channel tape.

New capabilities added with this expansion are a punched paper tape reader, a serial printer (typewriter) and a high-speed communicator that transmits data at 2,400 bits-per-second. Previously announced capabilities include punched card reading, a pooler, communication at 1200 bits-per-second, line printing, an adding machine, and check-digit verification.

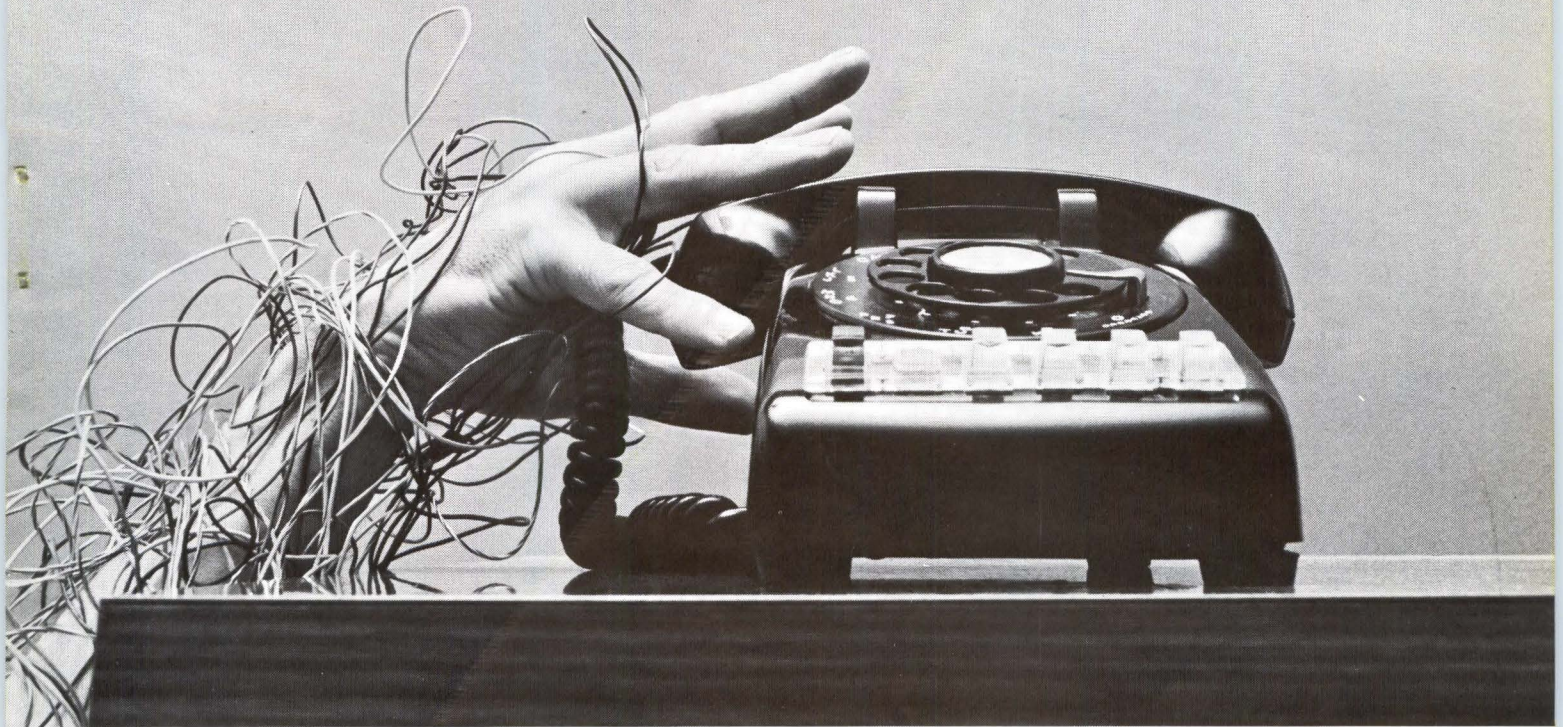
"Combination units—ones that perform up to three functions in addition to keyboard-to-magnetic tape transcription—allow a Keytape user to perform several operations on a single

machine and save the cost of buying additional single-purpose machines for specific tasks," O'Heir said.

With Honeywell's now extensive Keytape family, customers are provided data handling capabilities in three major areas—data preparation, media conversion and data communications.

In data preparation, basic Keytape units transcribe source data onto computer-ready magnetic tape. Check digit models are used to prepare data and verify data fields containing built-in check digits. Adding machine models accumulate data fields to provide off-line batch balancing while recording data on magnetic tape.

Media conversion capabilities include transcription of data onto magnetic tape from paper tape, punched cards and 51-column turn-around documents, and from magnetic tape to line or serial printers.



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CIRCLE NO. 20 ON INQUIRY CARD

INDUSTRY NEWS

A. D. LITTLE STUDYING OPPORTUNITIES IN ELECTRO-OPTICS

Arthur D. Little, Inc., is making a study of the effects that current and projected electro-optics technology will have on six major military and industrial markets over the next 10 years. The work is being undertaken for a group of companies chiefly in the electronics industry, and the results of the analysis will be issued to the sponsors in April, 1969.

The study will report on present and future electro-optics industry technology; component, materials, and systems applications; manufacturing costs and pricing; structure; and management problems. Markets being studied in the project are space and military broadcasting, navigation, and missile-guidance devices; military surveillance and reconnaissance instruments; computer, data-processing, and associated display equipment; commercial broadcasting, communications, and navigation systems; modulator and detector components; and laser materials.

ENGINEERING-SUPPORT FACILITY TO BE ESTABLISHED—Plans to establish an engineering and support facility to expand service to military activities at Fort Monmouth were recently announced by Sylvania Electric Products Inc.

Richard L. Shetler, a Senior Vice President of Sylvania, said the facility will permit optimum liaison between the company and such organizations as the Project Mallard Program Office, the Army Electronics Command, the Communications-Electronics Agency, and the Army Satellite Communications Agency.

The 20,000-square foot leased facility will be located in the Mid-Monmouth Industrial Park, less than one mile from the Electronics Command's headquarters. It will serve as a center for research, development, limited production, test, evaluation, operation, and maintenance of electronic equipment. The areas served will be primarily data processing, communications, surveillance, avionics, and electronic warfare, Mr. Shetler said.

Sylvania Electronic Systems, an operating group of the company with headquarters in Waltham, Mass., will occupy the new facility. The group has over-all responsibility for systems management of GT&E's major government projects.

COMPUTER DONATED TO SCHOOL—The University of Pittsburgh, School of Engineering, will be given a Model 4700 computer by Scientific Control Corp., as a result of a contest held at the 1968 FJCC.

Delegates to the conference were given the opportunity to win the newly announced computer and donate it to the university of their choice.

W. B. Jones, a member of Computer Science Corp. technical staff in El Segundo, Calif., won the computer and selected U. of Pittsburgh to receive it. The computer is valued at \$16,500.

Scientific Control's display at the conference featured a show on the performance and potential usages of the computer. Following the performance, the audience was asked to fill out a questionnaire on the computer's capabilities. The cards were graded, and the ones with all correct answers were eligible for the drawing which determined the winner.

"As far as we know, this is the first time a computer has been given away in this manner," said John Baird, President of SCC. "The computer will be delivered to the university in May of 1969."

INFORMATION RETRIEVAL UNITS INSTALLED—The Ultronic Systems subsidiary of Sylvania Electric Products Inc. has announced the first installation of Videomaster™, the desktop, information-retrieval unit that provides financial market information to brokerage firms on a video screen. A total of 275 VIDEOMASTER units were installed in 32 financial and brokerage offices during the last month.

Videomaster can summon 17 up-to-the-second details about any one of more than 8,000 securities, and display them simultaneously on its 12-inch video screen. It can monitor any of 18 selected securities and report their performance, and can alert its operator to special stock situations within price parameters he selects. Videomaster also provides optional capabilities for displaying market summaries, financial news, and economic background data from both internal and external computer sources, as well as from the worldwide Ultronic data network.

The keyboard of the Videomaster is detachable, allowing greater flexibility in desk or office arrangements. In addition, the keyboard can function with television monitors of any size as well as with the unit's own display screen.

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CIRCLE NO. 22 ON INQUIRY CARD

INDUSTRY NEWS

IEEE ELECTS BOARD OF DIRECTORS FOR 1969—Dr. F. Karl Wilenbrock, newly elected President of the IEEE announced that on January 7, 1969 the Institute's Annual Assembly elected the following to the IEEE Board of Directors:

Directors-at-Large: Mr. G. J. An-Aire, ITT Latin America, Buenos Aires, Argentina. Dr. Werner Buch-Poughke, Development Laboratory, Sinclair, Inc., New York. Dr. George engineering, Department of Electrical Engineering, University of Toronto, Toronto, Canada. Dr. J. G. Truxal, Polytechnic Institute of Brooklyn, Brooklyn, New York. Dr. D. G. Lampard, Electrical Engineering Department, Monash University, Clayton, Victoria, Australia.

A CALL FOR TECHNICAL SESSION PROPOSALS for the 1969 Western Electronics Show and Convention (WESCON) has been issued by Dalton W. Martin, program chairman.

WESCON will be held in San Francisco August 19-22, 1969. Mr. Martin indicated his committee is planning a program of 20 sessions in the four days.

The call is for "session" proposals, rather than individual papers. Prospective session organizers are invited to send letters of intent, describing suggested sessions, to the chairman by March 1. The committee will then direct successful proposers to prepare more detailed proposals.

Mr. Martin said that the 1969 program will emphasize sessions in areas of applied technology.

He noted the following subject and topic areas as typical of those in which the committee is particularly interested:

Instrumentation: Trends in programmed testing; applications of micrologic instrumentation, impact of computers on instrumentation design.

Components and Circuitry: Communications systems designed with integrated circuits; active filters employing IC's; beam-lead technology; microelectronic design trade-offs.

Computers and EDP: Impact of minicomputers on engineering design; Training engineers to use computers; The implications of MSI and LSI; Trends in peripheral equipment; New techniques in computer-aided engineering; New Data communications hardware; Modems.

Communications: Application of new devices (FET's, micrologic) to communication circuits; Trends in modulation and coding; Communications in remote computer systems.

Electro-Optics: New applications of lasers in industry and science; New work in holography; New optical scanning techniques; New display ideas.

The Engineer's Role in Management: How engineers prepare for management; New product planning; Engineer-management interfaces; Career goals for engineers.

Letters of intent should be addressed to Dalton W. Martin, WESCON Technical Program Committee, 3600 Wilshire Blvd., Los Angeles, Calif. 90005.

Mr. Martin is vice president of engineering, Vidar Corporation, Mountain View, Calif. Members of the committee include Richard W. Towle, Towlelectronics Laboratory, Los Altos Hills, (vice-chairman); Dr. Thomas M. Whitney, Hewlett-Packard Co.; Dr. David Kleitman, Signetics Corp.; and Dr. David K. Adams, Stanford Research Institute.

WESCON is co-sponsored by Region 6, IEEE (San Francisco Section and Los Angeles Council), and the Western Electronic Manufacturers Association.

CALL FOR PAPERS

A Workshop on Applied Magnetics will be held May 22 and 23, 1969 at the Sheraton-Park Hotel in Washington, D.C. under the sponsorship of the Magnetics Group of the IEEE. Papers are being solicited in all areas of applied magnetics. The topics listed in the following categories are suggestions and are not intended to limit the scope or subject matter of any proposed paper. Ferroresonant devices: transformers, frequency dividers and multipliers, core configurations, core materials, and frequency sensitive circuits; Computer design techniques (programs): transformer and/or inductor design, device characterization, parts and assembly layout, ferroresonant transformer design, power conversion circuits, and control of product testing by computer.

Space in the IEEE Transactions on Magnetics will be reserved for publication of accepted papers.

Abstracts of about 300 words, typed and double-spaced, should be submitted before January 24, 1969 to O. Kiltie, Ballastran Corporation, Executive Blvd., Fort Wayne, Indiana 46808, 219-484-4123.

CIRCLE NO. 23 ON INQUIRY CARD →

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**a report
on the**

OPERATIONS RESEARCH/ TIME SHARING SYMPOSIUM

The National Bureau of Standards was host on October 29-31, 1968 to over 500 persons attending an Operations Research/Time Sharing Symposium, which was sponsored jointly by the Bureau, the Office of Naval Research, and the Washington Operations Research Council. This, the first symposium sponsored jointly by these organizations, had as its theme operations research and computer innovation. The area is of special interest now because many innovations are coming about as a result of sharing computer time on-line and to make fuller use of the shared facilities. Emphasis was placed on time-sharing technology as a tool for decision making. Although specific hardware and software techniques were not emphasized in the Symposium sessions, provision was made for demonstrating current applications.

The Symposium opened Tuesday morning, October 29, with a keynote address by Major General W. E. Carter, Deputy Assistant Secretary of Defense. He discussed trends in information systems for decision making, including systems using time-sharing techniques. The Department of Defense not only uses on-line systems, but has to allocate for new and advanced information systems far into the future. General Carter noted in particular that it is difficult for a manager to foresee all his needs.

Later, at the Symposium banquet, Eugene Fubini of the IBM Corporation discussed several problem areas of large on-line systems. He asserted that the computer industry and operations researchers should cooperate in overcoming some of the major problems.

The keynote address was followed by a tutorial session on time sharing—its fundamental concepts, its use in education, and future system trends. This served as an introduction to the content of sessions to follow.

The second session dealt with present applications for time sharing, from the pedestrian to the venture-some. A down-to-earth aspect of flying was described in a paper on planning airline gate facilities, while another paper described procedures for projecting five years in the future the consumption of groceries. Specialized business applications presented were of insurance agency performance analysis and of credit rating communication. Management gaming was described as a no-longer esoteric management technique.

Planned and potential applications for systems in which computers are used on-line was the subject of the third session. It was opened with a talk by Nicholas E. Golovin, recently of the President's Office of Science and Technology, on the status of computers and the evaluative function in government. Other papers delivered in this session dealt with the emerging use of data management systems in the Defense Department, the use of on-line computing systems in planning strategic defense, time sharing in educational simulation and trends in displays for management.

Cost-benefit analyses of time sharing were presented in the second Wednesday session. Some of the analyses were nonspecific in application, such as those describing benefits to management and data managers from use of an on-line shared compu-

ter. Another cost/benefit analysis dealt with a specific application, on-line assistance in text editing and publishing.

The first Thursday session turned to potential solutions to special problems, some of them widespread: gaining acceptance of the shared computer as a new technological resource, and protecting privacy in the shared system. Another problem dealt with was the public policy issue resulting from the interdependence of the computing and communicating functions. Still others were the purely technical ones arising in developing resource-shared systems. The final session, which followed, consisted of a summary and panel discussion.

Among the demonstrations presented at the Symposium were those on time sharing as the retrieval system for multiply listed real estate, of an airline reservations system, and of a system for obtaining current stock quotations. In addition, the use of time-sharing systems for cost analysis and university/educational planning analysis was demonstrated.

Co-chairmen of the Symposium were Hugh V. O'Neill, of the GE TEMPO Center for Advanced Study, and Donald W. King, of Westat Survey, Inc.

Proceedings of this Symposium will be published by the Washington Operations Research Council and should be available by April of 1969. For further information contact:

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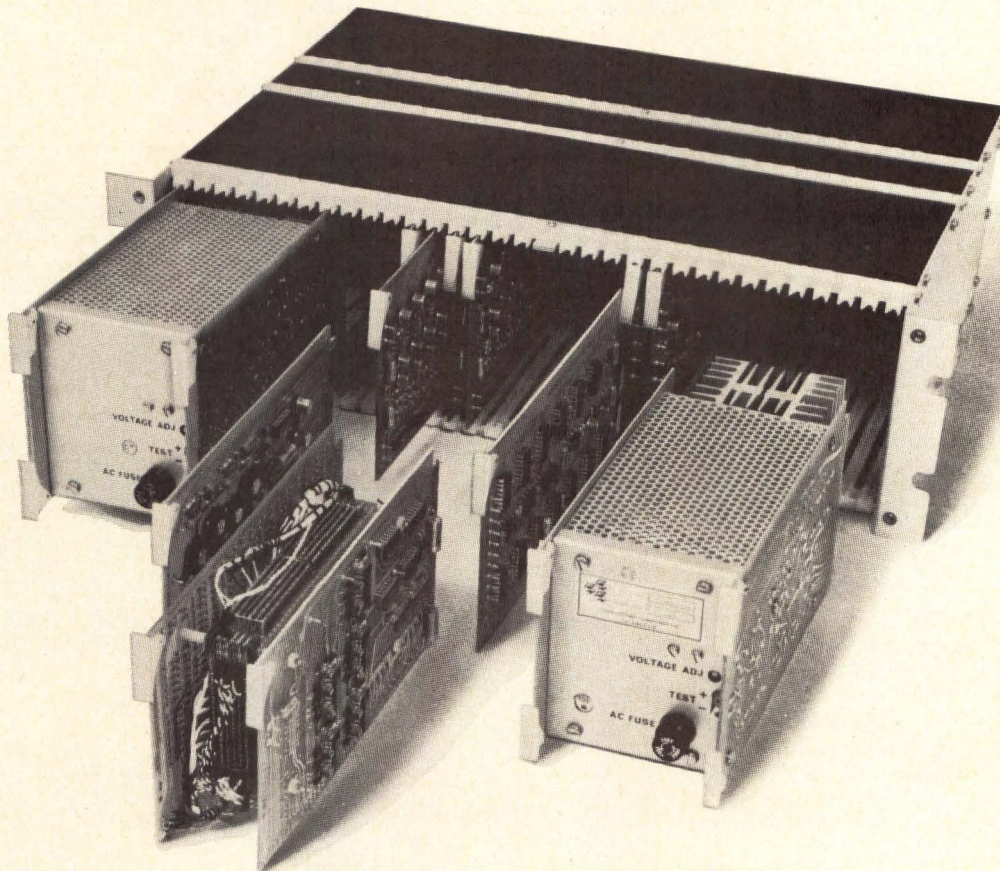
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CIRCLE NO. 24 ON INQUIRY CARD



DEVELOPMENTS

Automatic Reading Of Hand-Printed Data By Computer

Automatic reading of hand-printed messages by computer, long recognized as a promising means of speeding entry of data into information systems, is operationally feasible, according to an engineer of Sylvania Electric Products Inc., Waltham, Mass.

Dr. Donald B. Devoe of Sylvania's Applied Research Laboratory discounted two potential drawbacks to hand-printed entries. He concluded that a reliable recognition program does not require a prohibitive amount of computer storage, and that little difficulty is encountered in teaching persons to print clearly enough for accurate identification.

Dr. Devoe made his remarks in a paper presented at the 1968 Annual Convention of the Human Factors Society in Chicago. His findings were based in part on a study performed by the Laboratory under contract to the Rome Air Development Center, Griffiss Air Force Base, N. Y.

Any automatic recognition system must sense and categorize selected characteristics of the marks that are being interpreted, Dr. Devoe explained.

"To assure that the critical characteristics are present, rules for the formation of characters must be imposed on the persons doing the printing," he said. "These rules—or constraints—are thus determined by the computer's recognition logic, and if they depart greatly from habitual ways of forming characters, they introduce problems of learning, memory and motivation."

Numerous experiments using Sylvania employees were conducted to measure the speed and accuracy of printing and the amount of learning required for several levels of constraint difficulty.

"With a modest amount of train-

ing, a person can learn to follow a set of constraints that will permit a computer to interpret hand-printed data accurately. The requirements for computer capability are not excessive."

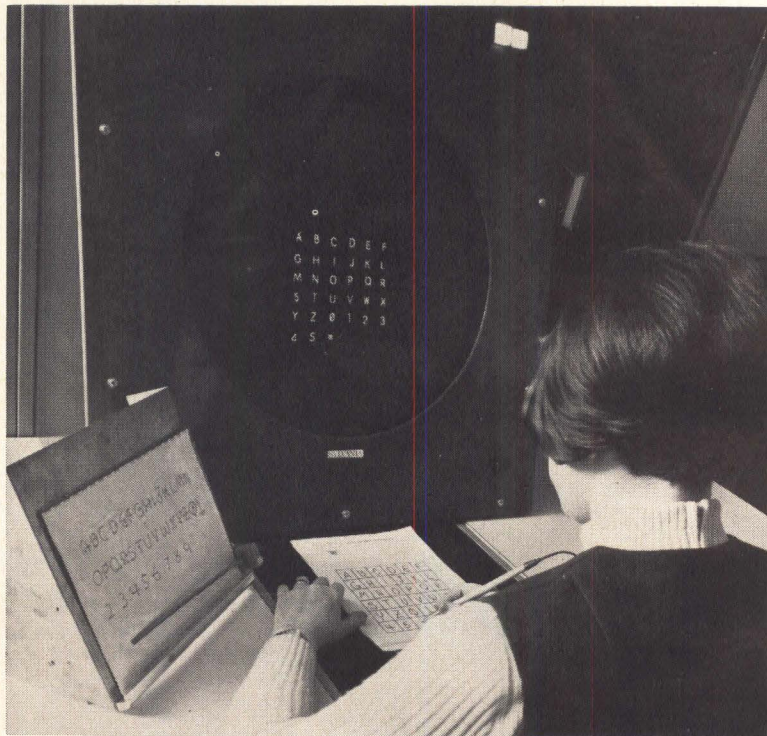
Sylvania has developed an electronic ballpoint pen which simultaneously transmits data to a computer for storage or analysis as it writes. The pen and its electronic "note pad" enable scientists to communicate with computers through written symbols and diagrams.

"Computers can recognize printed or typewritten material when each letter and number conforms to exact specifications," Dr. Devoe explained. "However, handprinted symbols have many individual

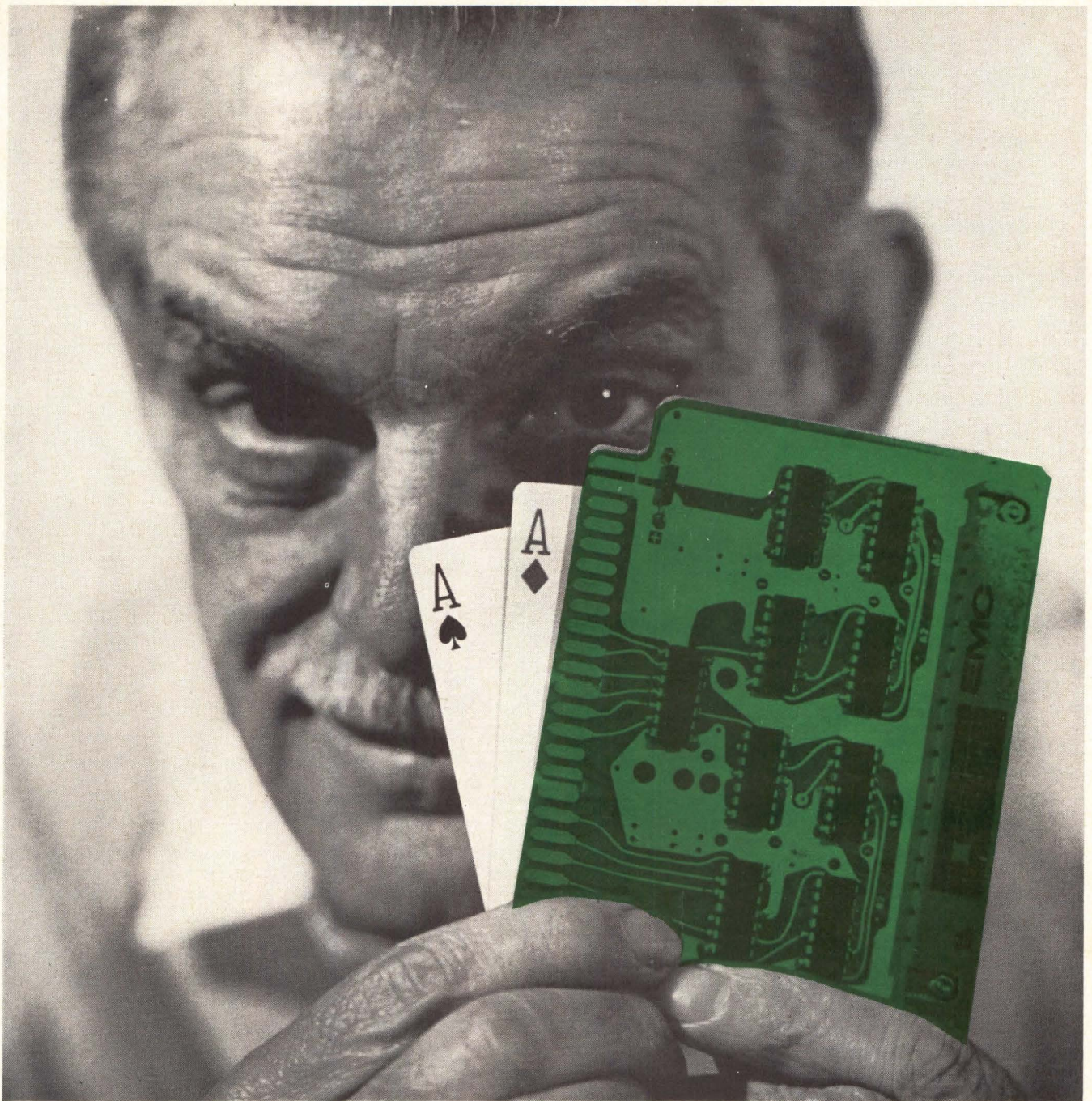
characteristics which can confuse a computer's recognition logic."

The ability to make immediate corrections is most important in order to provide essentially error-free messages, he continued. "Immediate visual feedback from the system promotes accuracy at the cost of speed, but this consideration is minor. The principal advantage of feedback is that it permits immediate correction," he noted.

Dr. Devoe cautioned against too permissive a set of rules. "In designing a system," he said, "the advantage of giving the user his personal set of constraints must be weighed against the nuisance of creating, storing, and reading into the computer the user's personal dictionary."



Sylvania has developed an electronic ballpoint pen which simultaneously transmits data to a computer for storage or analysis. The pen and its electronic "note pad" are used to communicate with a computer through written symbols and diagrams. Immediate visual feedback from the system via the visual display unit promotes accuracy by permitting the operator to make corrections immediately.



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inches wide by 3.5 inches high with an edge type connector of 44 rhodium-over-nickel tabs at the bottom. A 16-pin test point block at the top of the card accepts a standard 0.080 inch diameter test probe. Heavy power leads and large ground planes help to reduce the effects of noise. Additionally, each card incorporates a bypass capacitor between the power and ground leads. As a final protective measure, the cards are conformally coated on both sides.

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P.O. BOX 141 • TIMONIUM, MARYLAND 21093 • TWX 710-862-2638 • 301-666-3300

CIRCLE NO. 25 ON INQUIRY CARD



DEVELOPMENTS

Recording Head Part Measured To One Millionth Inch Accuracy

A surface profile measuring system is being used by IBM to insure accurate positioning of magnetic head assemblies for their disk storage products. Each assembly includes several stacked recording heads, each consisting of a .007 inch by .134 piece of ferrite placed inside a ceramic base about the size of a dime. An epoxy is used to attach the two parts.

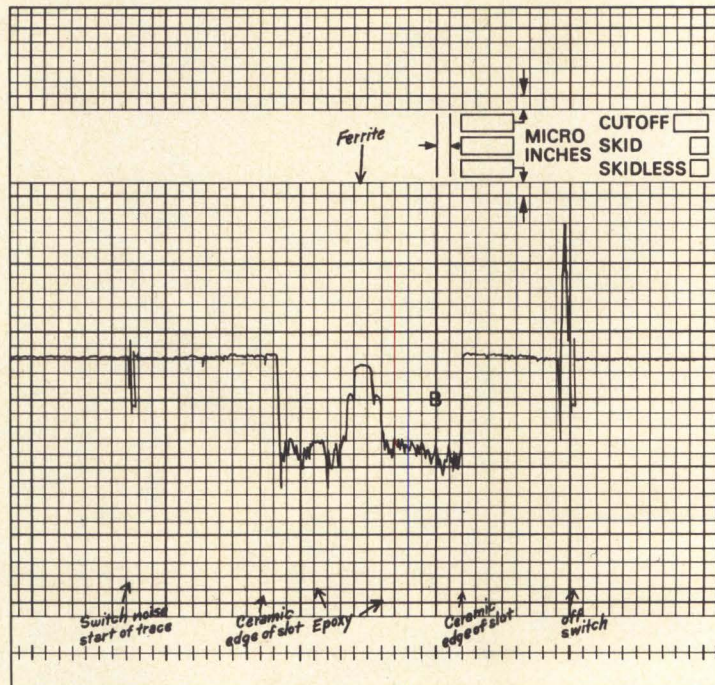
The micro-inch surface measurement system, developed by the Gaging and Control Division of the Clevite Corporation, checks the position of the ferrite, ceramic and epoxy, which must be maintained within 10 millionths of an inch. This precision tolerance is necessary because the completed heads, when stacked in an array, never come in direct contact with the disk surface; they instead are supported on a cushion of air above the disk surface. The system has a non-directionally oriented, diamond-tipped stylus that measures only .0001 inch across and weighs less than 200 milligrams.

IBM uses the analyzer to trace across three sections of the ferrite recording head. Three high contrast traces are obtained in this manner permitting simple profile analysis.

Engineers at IBM's manufacturing plant in San Jose, California, report the system exhibits two main advantages over previous methods of measurement: it is faster, and it is capable of much more precise measurement.

Photo-Optical Positioner System Developed

An automatic, tape controlled system for the generation of printed circuit board artwork has been developed by The Superior Electric Company, Bristol, Conn. The photo-optical positioning system is designed to eliminate the manual drafting and photo reduction of artwork. Working from a grid paper sketch, the tape can be programmed manually by a digitizer or by computer, and produces, on



Three high contrast traces provided by the analyzer permit easy profile analysis of magnetic head assemblies at IBM's San Jose, California plant.

film, an accurate circuit pattern to finished board size without the need for photographic reduction. Resolution to .0005" is provided. This film (positive or negative) then goes directly to the silk screening department for creating screens and to the blueprint machine for blueprint copies. The same equipment can be used for other graphic requirements, such as drawing schematics.

The system consists of a three-axis tape control unit driving an X-Y positioning table which holds the film on a vacuum frame, an optical head consisting of a controlled intensity collimated light source, a shutter and a programmed image disk. In operation the film is positioned by X-Y motion to location underneath the image disk which is in turn positioned to a programmed image under the shutter and light source. The shutter is opened automatically and an image is recorded on the film. When tracing a line, the shutter is kept open until the path is completed; in image flashing, the shutter is closed before movement to the next position. The shutter

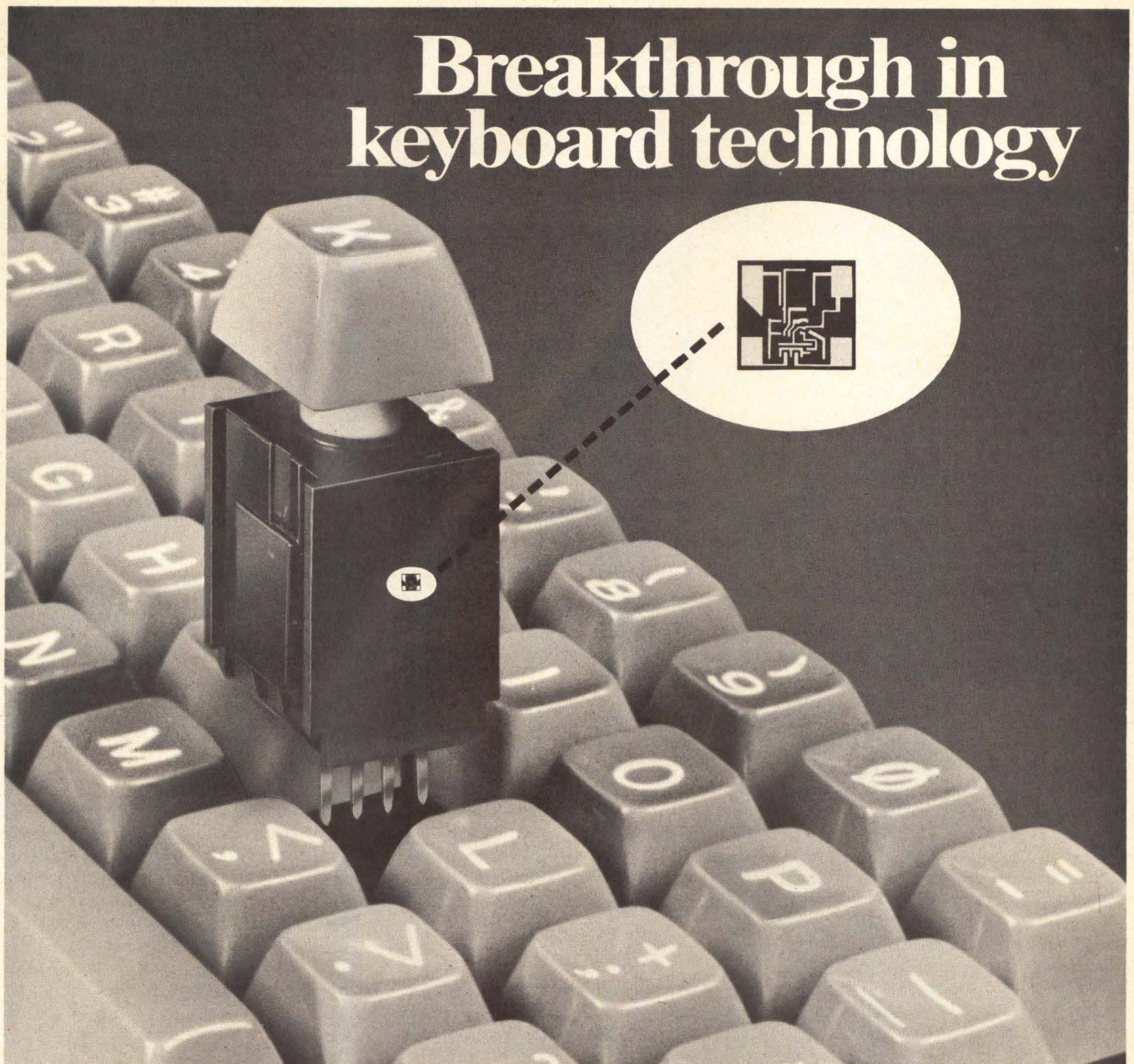
time is adjustable. The image can be a round or a square opening, a letter, a number, a schematic symbol, or virtually any character the customer selects. Normally there are 64 images on a disk, however this can vary on customer selection from 2 to 200 images.

The unit is also capable of step and repeat work within its travel range of 11" x 18", and at 100 times size can produce micro circuit artwork.

The initial tape program can also be used to produce compatible, proven tapes for tape controlled drilling, tape controlled eyelet insertion and tape controlled component insertion.

Users of such a system then have a fast, accurate method of producing artwork which can initially be used with manual programming and later adapted to computerized systems. It can operate as an independent unit for the production of artwork or as part of a complete system of tape controlled equipment for the fabrication of printed circuit boards, including assembly of components.

Breakthrough in keyboard technology



An all solid state keyboard...the first of its kind

The breakthrough: Using the Hall effect, MICRO SWITCH has developed the world's first practical application of an integrated circuit as a keyboard switching element. This tiny chip (inset above) is actuated with a magnet mounted on a plunger. Thus MICRO SWITCH for the first time combines integrated circuitry with manual actuation.

The result: SSK—an all solid state keyboard offering new reliability, new economy in a flexible package. It is

assembled, wired and encoded—ready to plug into your equipment.

Proven reliability: From key to connector, every unit of the new SSK keyboard is all solid state. The only moving mechanical part is the plunger. No mechanical linkages, no moving contacts to wear or fail.

Triple economy: *First*, initial cost is less, tailored to your high production commitments. *Second*, the bounce-free output of SSK requires no special interface circuitry to adapt it to your

equipment; just plug it in. *Finally*, being solid state, SSK is practically maintenance free.

Unmatched Flexibility: SSK adapts to your format and encoding needs. All standard key arrays and custom arrays, block or offset. Encoding of any 8-bit code (or less); hexadecimal; Baudot; BCD; USASCII mono-code, dual-mode and trifunction; plus EBCDIC and custom codes. Full selection of customized legends and colors. Write for complete details.

MICRO SWITCH

FREEPORT, ILLINOIS 61032

A DIVISION OF HONEYWELL

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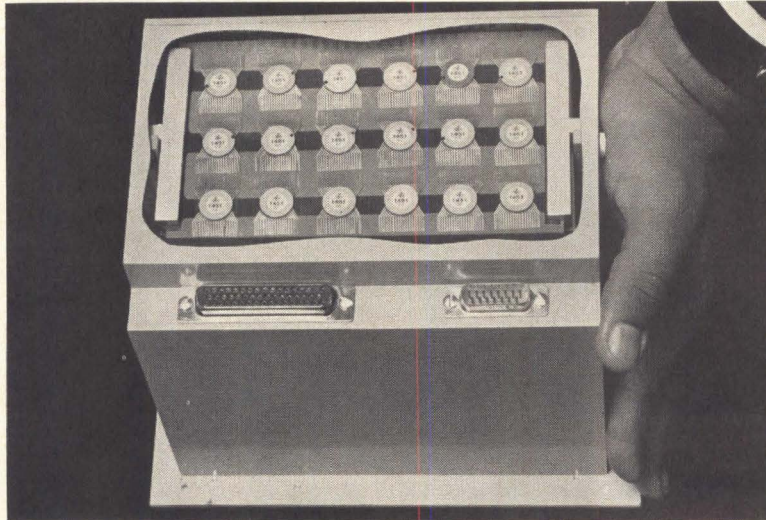
CIRCLE NO. 26 ON INQUIRY CARD



DEVELOPMENTS

General Purpose Computer Designed With MOS Circuits

A fully operational general purpose computer using highly advanced MOS circuitry has been developed by the Autonetics Division of North American Rockwell, to satisfy the general requirements of a navigation computer. The computer is a parallel, single address organization machine with a 24-bit word size for instructions and data. It is designed to address a 32K word memory, however, it currently uses a 4K word core memory and although the core memory has a 2 μ sec cycle time, the computer only requires a 4 μ sec memory to meet the stated instruction execution times. In the not too distant future, Autonetics expects to operate the MOS-LSA's at a 1 MHz clock rate (they're presently operating at a 250 kHz rate), at which time a 1 μ sec cycle time memory will be required. Thirty-five instructions are provided, including a 108 μ sec multiply, a 108 μ sec sum of products multiply, and a 112 μ sec divide. Most of the other instructions require 8 μ sec with the main exception being the shift type instructions which are of variable duration.



This fully operational general purpose computer is designed with MOS-LSA integrated circuits. Developed by North American Rockwell's Autonetics Div. for navigation applications, the computer weighs 9 pounds is 5" wide, 7" high and 6" deep and consumes only 10 watts of power.

The computer organization is fairly conventional, using an accumulator, a lower accumulator, an operand buffer register, a program counter, and three index registers. Four LSA's each are used to mechanize the 24-bit accumulator, the 24-bit lower accumulator, and the 24-bit buffer register. Four more LSA's are used to mechanize a 16-

bit program counter and three 16-bit index registers, and another three mechanize the mode control. These 19 LSA's constitute the arithmetic and control portion of the computer. In addition to these LSA's, the CPU card also has four LSA's to mechanize a core memory interface function and one hybrid LSA to mechanize the 4-phase clock.

Japanese Engineers Design High Speed Facsimile Transmission Machine

A high speed facsimile transmission machine has been designed by the Matsushita Research Institute of Tokyo, Japan as a result of five years of intensive research. The machine uses four printing tubes—two of which were developed by Matsushita for the machine—a thin film penetration printing tube and a prism fiber reading/printing tube. The two remaining elements are a thin glass window printing tube and an electrostatic charge printing tube.

When the thin film penetration printing tube is in use, an electronic beam is released directly onto the recording media. The


prism fiber reading/printing tube makes it possible for one tube to both read and print a manuscript at the same time. The thin glass window printing tube converts electronic beams into light for recording purposes, while the electrostatic charge printing tube changes electronic beams into electronic charges for recording.

Newspapers and news agencies, as well as banks, trading and manufacturing companies, have all been using some form of facsimile transmission equipment in their daily business transactions. They have found this essential piece of machinery to be a most reliable means of communication. However, in recent years, their volume of business has increased to the point where they have found it necessary to find a facsimile transmission de-

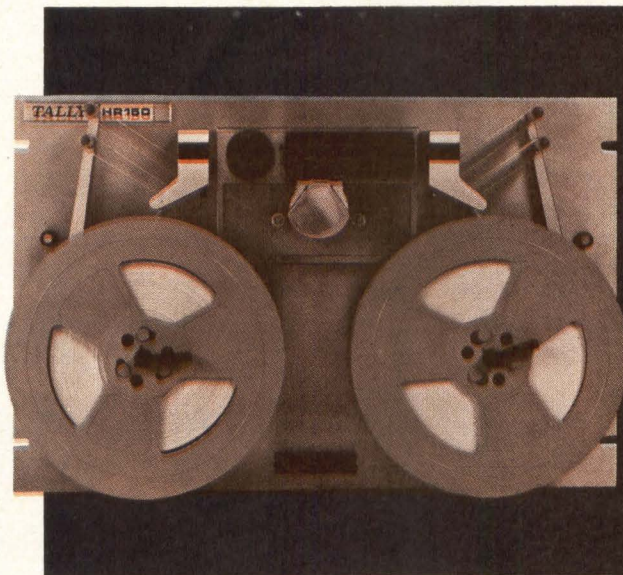
vice which could handle this increased work load efficiently at a much faster rate of speed.

Now, thanks to the engineers at the Matsushita Research Institute in Tokyo, such a machine is possible. For the first time, high speed transmission of a B5 size (18cm x 26cm) will take only eight to twenty-four seconds, because the electronic tubes in this machine will be scanning at the rate of 5 lines/mm. Previously, conventional mechanical scanning required thirty to one hundred and twenty seconds at 4 lines/mm. Before long, say Matsushita engineers, this new machine will be able to transmit and receive all types of information including the extremely high speed printing of an electronic computer output.

The Tally HR 150



**Day after day,
month after month,
year after year,
outstanding performance,
zero maintenance.**



New Tally HR 150 perforated tape readers have a first name: **High Reliability**. With essentially zero preventive maintenance, this tough reader is designed for a minimum life of 8,000 hours of actual reading time. In typical applications, minor failures would be experienced less than once a year.

Tally's remarkable new HR 150 readers are truly state of the art, operating asynchronously and bidirectionally at 150 characters per second. They feature a compact, self-contained design, and offer low noise level. Heart of this new reader is a stepping motor tape drive technique which permits true pulse operation and avoids the wear and tear caused by continuously moving parts.

You will find loading easy and fast. Reeling tension arms can be locked upright for convenient tape threading. Smooth rewind is bidirectional at 40 inches per second. All of this with a two year warranty.

If you are interested in **Day after day, month after month, year after year** of trouble free high performance, you can get all the information including full price and technical data, by writing Tom Tracy, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Or phone: (206) 624-0760. In Europe and the U.K., address Tally, Ltd., 6a George Street, Croydon, Surrey, England. Phone: (01) 686-6836.



TALLY

CIRCLE NO. 27 ON INQUIRY CARD



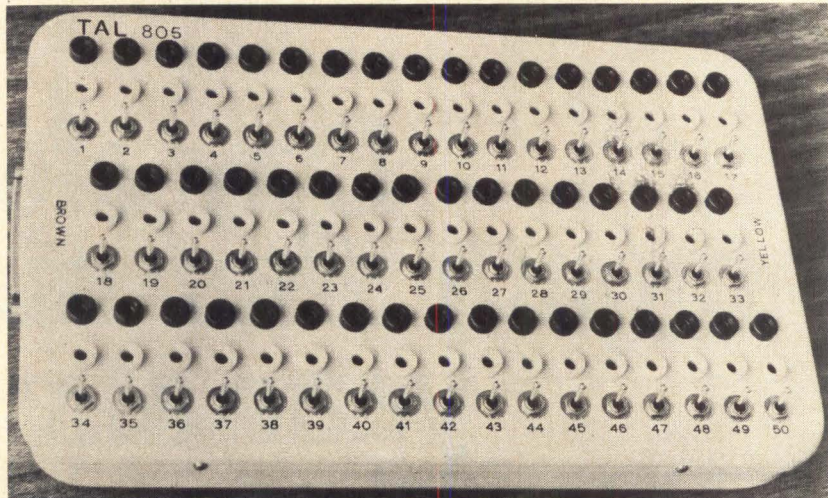
DEVELOPMENTS

Laboratory Break-Out Boxes Reduce Hookup Time

What is believed to be the first commercially-available break-out box, designed to reduce the hookup time required to test electronic/electrical equipment, has been developed by Technical Assistance Laboratories, Torrance, California.

The new testing device, when connected to a black box via a simple cable, breaks out all connections to standard banana jacks to ease terminations. The TAL break-out boxes can also be placed in series between any two pieces of equipment to allow the experimenter to measure or interrupt voltages, currents and waveforms traveling between the two units.

The new devices were created to eliminate the conventional, time-consuming practice of an electronic laboratory creating its own temporary break-out box for a particular job. These "jerry-rigged" boxes, designed only for one-time usage, would not be constructed with a lasting quality or universal design and, as a result, would be discarded after the completion of the job. The



The break-out box designed by Technical Assistance Laboratories permits all connections from a black box to be isolated to standard banana jacks. Designed for laboratory and production applications, the boxes reduce the hookup time normally required to test electronic/electrical equipment.

costly cycle would be repeated each time a new job reached the laboratory.

TAL break-out boxes, however, are designed and built in a manner that makes them ideal for the re-

peated performance of a wide variety of functions. Of universal design, they can be made to interface and mate with any type of connectors; any number of circuits may be included on a box.

New Techniques For Error Recovery In Computer Systems

Error recovery in computer systems can no longer be relegated to hardware or programming alone, according to Alan N. Higgins, an IBM programmer who recently reported a new approach to the problem.

"The cost of an error has increased dramatically with advanced programming techniques," Mr. Higgins said. "Merely rerunning the job can no longer be accepted as a prime means of recovery. Hardware and programming must form an effective partnership and attack the problem together."

Mr. Higgins discussed three general types of system interruptions at the 1968 Fall Joint Computer Conference:

- Hardware malfunction
- Design errors (both hardware and software)
- Operator or user-injected errors

Recovery management support (RMS) for the IBM System/360, Model 65, through various error recovery functions, aims to reduce the number of interruptions that the user is exposed to, or minimize their impact when they occur.

Among these functions, instruction retry has been a standard procedure whenever an error was encountered in reading or writing a tape. Now, through a detailed analysis of the computer's operating status, it is extended to not only I/O instructions, but to most of the instructions in the CPU.

The occurrence of a parity error in main storage makes instruction retry impossible, so another valuable function is the ability to "refresh" main storage by loading a new copy of the affected program module into main storage.

Another function, selective termination, enables the system to examine the failing environment, determine what problem program

was executing, and then proceed to terminate this program while continuing all other jobs that were running at the time of the malfunction.

A fourth function, I/O recovery, concerns basically I/O retry, which can provide the basis for a successful recovery from errors due to many varied I/O malfunctions.

These functions are contained in two programs that make up RMS/65. The first is a machine check handler (MCH) for CPU and memory malfunction; the second is a channel check handler (CCH) for I/O problems.

Recovery management support for the Model 65 is structured into a four-level hierarchy of: 1. Functional recovery; 2. System recovery; 3. System-supported restart, and 4. System repair. These stages cover the range from the successful retry of an instruction, to isolation and repair of program damage, to actual system repair.



SPC-12

the new automation computer

The SPC-12 is a new automation computer designed for economical use in dedicated automation and control functions.

The SPC-12 is powerful—with six programmable 12-bit registers, a 2-microsecond (4K to 16K) memory of 8-bit bytes, and a unique memory saving "shared command" concept. Fully IC'd for reliable 'round-the-clock' operation. \$6400, *including* a teletypewriter interface, control panel, and real time clock, console lock, optional power failure restart, and optional direct memory transfer.

That's just half the story. Most computers require expensive engineering and black boxes to work in a control system. Not the SPC-12. It comes with economical functional modules which adapt the SPC-12 easily to instrumentation, computer peripherals, keyboards and displays, sensors and communication networks. With these functional modules and its power, the SPC-12 achieves a new cost/performance ratio and makes computer control practical in your system today. Programming aids and application software of course. Call or write for more information about the SPC-12—the new automation computer.



GENERAL AUTOMATION, INC.
Automation Products Division

706 West Katella, Orange, Calif. (714) 633-1091

CIRCLE NO. 28 ON INQUIRY CARD

This article describes the effect of speed and load upon TTL microcircuits and provides numerical values useful to predict the additional power consumption required at high clock rates.

POWER CONSIDERATIONS IN HIGH SPEED TTL LOGIC

John C. Tirrell

Sprague Electric Co.*
Semiconductor Div.
North Adams, Mass.

The increase in power consumption of high speed TTL microcircuits resulting from high operating frequencies and various loads is seldom available in product specifications.

This article provides a frank discussion of the effect of speed and load upon TTL microcircuits and concludes with numerical values useful to predict the additional power consumption required at high clock rates.

The basic TTL NAND gate is analyzed in detail and is the vehicle by which these predictions are obtained. The effects of temperature upon circuit parameter changes are discussed along with a brief section explaining the heat-transfer mechanism in plastic dual in-line and flat-pack packages.

Most detailed circuit analysis is separated from the text and is located in the Appendix for readers who wish further explanation on how conclusions are obtained.

Microcircuit power considerations are basically of two types: power consumption and power dissipation. A proper understanding of these two terms will eliminate much of the present confusion and will also help to clarify their significance in the overall discussion.



John C. Tirrell received the BS degree from Wheaton College in 1955. Prior to joining Sprague Electric in 1965, he was associated with Teletype Corp., with responsibilities in the design and development of data communication systems and peripheral equipment. He is presently with Sanders Associates as manager of applications, data communication systems. He is a member of the I.E.E.E.

DEFINITION OF TERMS

Maximum power consumption represents the greatest amount of current at a particular bias voltage (V_{cc}) which the circuit can be expected to require for correct operation. On the other hand, maximum power dissipation of the microcircuit should be considered as the maximum stress in watts that can be tolerated before normal circuit operation is impaired or before damage occurs.

The power consumption of a microcircuit is also a measure of the amount of heat generated. Consequently, it indicates the power which must be dissipated from the package in order to maintain acceptable junction temperatures. This is why power consumption and power dissipation are often used as synonymous terms. However, power consumption is most important as an indication of the amount of power which must be available for proper operation.

The logic design engineer recognizes that there is a power speed trade-off in logic circuits. As the system speed requirements increase, so does the power consumption of the circuits required to perform the logic. The total power consumption of the circuits used is required to provide a guide for designing or selecting the proper power source.

The packaging engineer must also consider the circuit power consumption to determine the thermal dissipation requirements for the entire assembly. The proper ambient temperature must be maintained so that the junction temperature of the microcircuit chips are held within their specified operating temperature range.

In contrast, the power dissipation rating of a microcircuit is seldom a system design criteria. The *The author is now employed by Sanders Associates, Nashua, New Hampshire.

power dissipation limit is determined by the thermal resistance of the microcircuit package. If the rated power dissipation limit is exceeded, the internal temperature of the chip will rise to a destructive level. More appropriately, the rated power dissipation dictates the maximum limit which must never be exceeded and, in all practicality, never will be. However, the difference between the rated power dissipation and the maximum power consumption indicates the available power dissipation margin of a given microcircuit assembly.

Specified power ratings (both consumption and dissipation) are provided in microcircuit data sheets. They provide essential information for the proper use of the circuits. A better understanding of these values can be obtained by examining in detail the way these values are determined and used.

POWER CONSUMPTION OF TYPICAL GATE

Quiescent state—The power consumption of most gates is different for the 0 state than for the 1 state. This can be seen by using a typical NAND gate circuit and observing the current flow for both states.

Figure 1 shows the schematic of a NAND gate in the 0 state. This is the actual way the circuit is tested for power consumption. The values of components and parameters shown are nominal values for purposes of example, but remember that these values can vary considerably and so will the amount of current required.

The variations which affect power will be discussed later, but Fig. 1 shows that a major portion of the current flow contributes to the base drive for the output ON transistor. Since the emitter inputs are backed-biased and the output is open, all current flow is essentially from V_{CC} . The power consumption for the circuit shown is supply current times supply voltage, (I_{CC} (V_{CC}); or, (6.53 mA)(5V), which equals 32.65 mW.

A typical NAND gate in the 0 state can be expected to have close to 32.65 mW of power consumption.

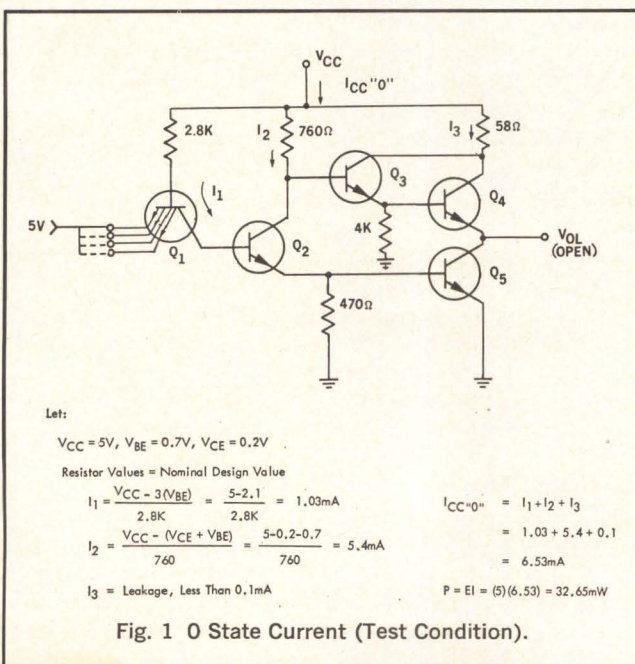
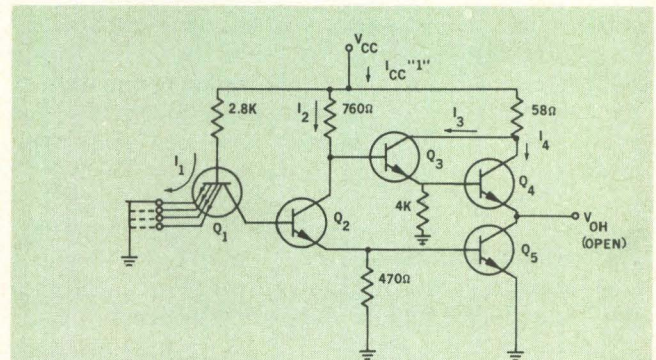


Fig. 1 0 State Current (Test Condition).

When the same gate is tested for 1 level power consumption, it is connected as shown in Fig. 2A. Here, the main current flow is out of the input. This keeps the input transistor ON and the output pull-down transistor in the OFF condition. The output is held high.

The total current flow in this example is 3.17 mA. The power consumption of this circuit is (2.72 mA) (5V) or 13.6 mW. Fig. 2B shows the method used to determine the current flow through transistor Q_3 . In the 1 state, with the output open, I_3 is greatly dependent upon the beta of transistor Q_3 .

Comparing the 0 and the 1 level current, note that there is almost a 3 to 1 ratio of power consumption between the 0 state and the 1 state of a typical gate.



Let:

$$V_{CC} = 5V, V_{BE} = 0.7V, V_{CE} = 0.2V$$

Resistor Values = Nominal Design Value

$$I_1 = \frac{V_{CC} - V_{BE}}{2.8K} = \frac{5 - 0.7}{2.8K} = \frac{4.3}{2.8K} = 1.54mA$$

$$I_2 = 0.02mA$$

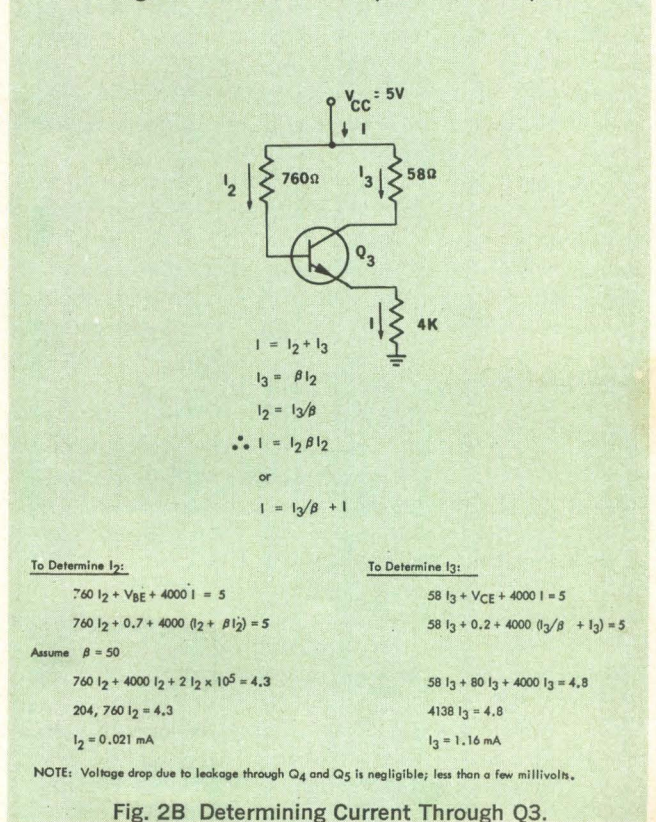
$$I_3 = 1.16mA$$

$$I_4 = \text{Leakage thru } Q_2 + Q_5 \approx 0.2mA$$

$$I_{CC} = I_1 + I_2 + I_3 + I_4 = 1.54 + 0.02 + 1.16 + 0.2 = 2.72mA$$

$$P = EI = (5)(2.72) = 13.6mW$$

Fig. 2A 1 State Current (Test Condition).



To Determine I_2 :

$$760 I_2 + V_{BE} + 4000 I = 5$$

$$760 I_2 + 0.7 + 4000 (I_2 + \beta I_2) = 5$$

Assume $\beta = 50$

$$760 I_2 + 4000 I_2 + 2 I_2 \times 10^5 = 4.3$$

$$204,760 I_2 = 4.3$$

$$I_2 = 0.021mA$$

To Determine I_3 :

$$58 I_3 + V_{CE} + 4000 I = 5$$

$$58 I_3 + 0.2 + 4000 (I_3 / \beta + I_3) = 5$$

$$58 I_3 + 80 I_3 + 4000 I_3 = 4.8$$

$$4138 I_3 = 4.8$$

$$I_3 = 1.16mA$$

NOTE: Voltage drop due to leakage through Q_4 and Q_5 is negligible; less than a few millivolts.

Fig. 2B Determining Current Through Q_3 .

USE OF 50% DUTY CYCLE POWER CONSUMPTION

Specified power consumption for individual micro-circuit gates is given in current or milliwatts for either a 50% duty cycle or for the 0 and the 1 states. In the latter case, the difference between the 1 and 0 state power levels can be determined, but when power at 50% duty cycle is listed only a general idea of the power for each state can be surmised without a detailed circuit analysis.

Of what use is the 50% duty cycle power consumption value when only this is given? For most applications, sufficient power supply margin can be provided by using the 50% duty cycle value so that a detailed tabulation of the most-power-consuming-combination of gates is not necessary. The 50% duty cycle values can be summed for a fairly good approximation of the maximum power required for a given logic system. However, caution must be exercised when using this approach as will be seen later.

In the examples of Figs. 1 and 2, the power consumption of a gate is essentially I_{cc} times V_{cc} . Often the question has been asked, "Doesn't the flow into and out of a gate contribute to the power consumption either of the gate or the gates connected to it?"

To answer this question in its entirety is futile. Where do you stop adding circuits in order to be able to consider all the current flows and consequently the actual power consumed (really dissipated) within a given gate? A brief example of two cross-coupled gates can be used to show that the total power consumed is equal to the sum of the individual 50% duty power consumption of each gate. Hence, current into and out of an input or output need not be considered.

Figure 3 shows the current flow into and out of two gates, one in the 1 state (Gate A), the other (Gate B) in the 0 state. Some of the I_{cc} current in Gate A flows out of the gate and contributes to the power dissipation of associated elements. Gate B dissipates power as the result of current from external elements flowing into its inputs and output.

Consequently, the actual power dissipation in Gate A is less than the $(I_{cc})(V_{cc})$ power of this circuit and, conversely, it is greater in Gate B. If the individual currents and corresponding power dissipation for every gate in a system had to be computed, the task would be enormous. The designer would just go ahead and design the logic assembly, put it together, and then measure the current required.

In many cases, the design of the power supply required is concurrent with the logic design and the designer needs a pretty good idea, ahead of time, as to the total power required.

In Fig. 4, gates A and B are combined and cross-coupled so that one is always in the 1 state when the other is in the 0 state. Notice now that the current flow from one gate output equals the input current of the other gate. By equating these currents, and considering the current times voltage power of both the I_{cc} and ground currents, it is apparent that the actual power consumed by both gates is the sum of their V_{cc} current times the V_{cc} potential.

Figure 5 also shows two gates. Assuming each to be

the same gate, but in a different state, 50% duty cycle power consumption for one gate is

$$\frac{(I_{cc 1} + I_{cc 0}) V_{cc}}{2}$$

Now, referring back to Fig. 4 for the power consumption of this circuit configuration, note that P equals $(I_{V_{cc} 1} + I_{V_{cc} 0}) V_{cc}$. In other words, the power equals twice the 50% power consumption of one gate. By totaling the 50% power consumption of the gates used, a value of the total power consumed for the particular circuit configuration is produced.

Obviously, not all circuits represent the ideal case. Unless a large number of circuit elements are to remain in only one state and the same state for long periods of time, totaling the 50% power consumption of each circuit works quite well.

PROVIDE SUITABLE POWER SOURCE

The typical power consumption stated in a specification provides a guide as to the average gate power expected from a large number of identical gates. However, a good design practice is to allow enough power capability to assure an adequate margin. For most applications the maximum values given should be used. At times, this additional power may be needed. Specifications describe a circuit insofar as is possible to fulfill the user's needs and at the same time hold internal testing to a reasonable level. Testing adds cost to the device and if reliable operation is expected without excessive testing, both the manufacturer and the user realize economic gains.

Because of this compromise, there is a possible 1 level condition for the NAND gate as defined by the output minimum high level, $V_{OH \text{ min}}$ level of 2.4 volts.

The maximum rated output load for the NAND gate is 10. This means it must sink 20 mA at 0.4 V maximum, and it must guarantee 2.4 V at 0.5 mA source. The input leakage of NAND gates at 2.4 V is below 50 mA, so 10 inputs would require 0.5 mA current source or, most likely, less. The NAND gate output design using a Darlington transistor pair can provide considerably more current and consequently the $V_{OH \text{ min}}$ level of 2.4 V is seldom attained.

Typically, the fully loaded output will be above 3 volts. But since $V_{OH \text{ min}} = 2.4 \text{ V}$ is a valid condition, the effect upon 1 level power consumption should be considered.

Refer to Fig. 6, which shows the NAND gate circuit connected in the 1 state with the output clamped at $V_{ol \text{ min}}$. At this specified level the total $I_{cc 1}$ current of the NAND gate can theoretically approach 5.87 mA and the gate can consume 29.35 mW.

The calculated power consumption values, the specification values, and the previously discussed 1 level value all differ. They are typical values and are tabulated below for comparison.

The difference between specification values and the computed values of Fig. 1 and 2 can be attributed to slight inaccuracies in the parameter values used. Notice, however, that considerable unexpected power consumption could occur. This can be seen when the

Table 1 Comparison of Specified & Computed Power Consumption.

Specification	I_{CC} (mA)	Power Consumption (mW)	50% Duty Cycle Power (mW)
0 Level	6.0	30.0	21.2
1 Level	2.5	12.5	
Computed			
Figure 1, 0 level	6.53	32.65	
Figure 2A, 1 level	2.72	13.60	23.1
Figure 6, 1 level	5.87	29.35	31.0

typical 1 level specification limit of 12.5 mW is contrasted with the V_{OH} min = 2.4 V condition of 29.35 mW.

It is necessary to re-emphasize the fact that the conditions of $V_{OH} = 2.4$ V are not usual. They are discussed here to point out the possibility of needing adequate power and the need for conservative design of power supplies; that is, to allow enough leeway to meet the maximum specified rating.

CONDITIONS AFFECTING POWER CONSUMPTION

Normal distribution curves provide a typical value of power consumption which becomes a good guide for determining the desirability of a circuit and the desirabilities of its associated family. As previously indicated, variations in the parameters of the elements within the microcircuit can affect its power consumption. An idea of what the maximum value can be is also needed to show what can happen under worst-case conditions. Now, consider the reason for parameter variations which effect worst case power consumption.

RESISTOR VALUES

The most obvious parameter affecting power consumption is the actual value of the circuit resistors. Since all resistors are made at the same time, they possess common characteristics and their values are all shifted in the same direction. If one is higher than the design value, they all will be higher and, similarly, they all will be on the low side if one is low.

Resistors in a circuit made by the epitaxial process will be within $\pm 20\%$ of their nominal values. Actually, closer tolerances are possible, but requiring less than $\pm 20\%$ would reduce yields and is not necessary. The circuits are designed for worst-case operation with $\pm 20\%$ tolerance resistors.

The actual resistance ratios of resistors within the same circuit is fairly constant. Although this is usually not essential for digital-type circuits, it is important for linear circuits. Because the ratios are fairly constant, linear circuits can be designed and made to operate satisfactorily.

If the actual resistance values in a logic circuit are at the -20% level, the circuit will correspondingly consume more power. This new power consumption will increase by more than 20% of the nominal power consumption.

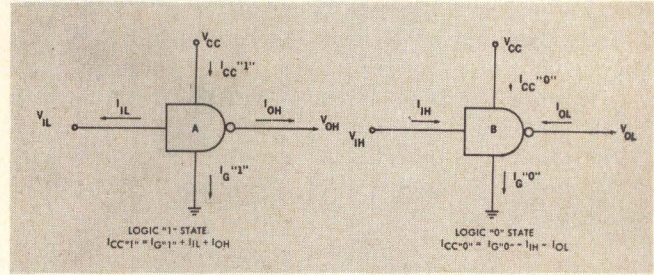


Fig. 3 Current Into And Out Of Gate.

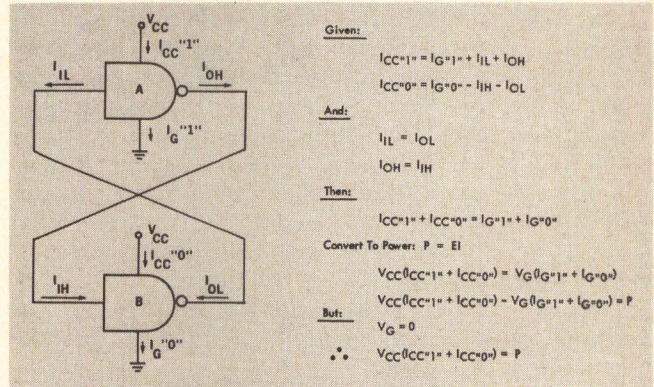


Fig. 4 Power Consumption Of Two Gates.

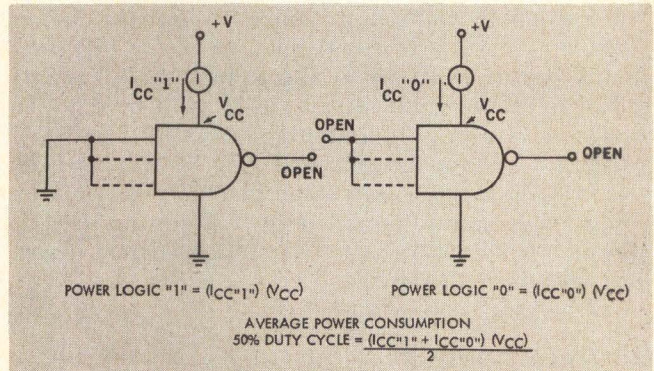


Fig. 5 Power Consumption Of One Gate.

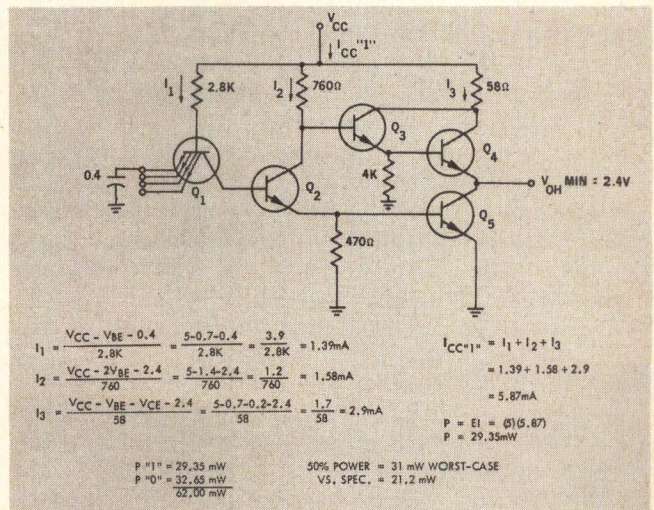


Fig. 6 1 State Current (Operating Condition).

Figure 7 shows that if the resistors are low by 20%, the 0 level power consumption is (8.13 mA) (5 V) or 40.65 mW. Comparing this with the 32.65 mW nominal value derived in Fig. 1, an increase of 24.5% in power consumption is apparent. The validity of this higher percentage increase is shown in Table 2.

Conversely, a 20% increase of resistor values will decrease power consumption by 16.7%. However, primary concern is with the effect lower resistor values have upon maximum power. This will be examined in detail later.

TEMPERATURE

Another parameter affecting resistor value is temperature. The temperature coefficient of resistance for diffused resistors in an epitaxial structure is a function of surface concentration and bulk concentration. Fortunately, the percent change vs. temperature plot for these resistors produces a dish-shaped curve. The minimum occurs near 25°C as seen in Fig. 8. Consequently, the worst-case temperature condition for power consumption, considering only resistors, is at or near room temperature when the resistors are most nearly at their lowest values. As the temperature increases or goes from 0°C to a lower temperature, the resistor values increase and the circuit consumes correspondingly less power.

VARIATION IN V_{CC}

An extremely important consideration for power consumption variations is the V_{cc} voltage. The power of the circuit increases as the square of the supply voltage and any small increase in V_{cc} will be reflected as an increase in power. Similarly, a reduction in V_{cc} will reduce power consumption. The latter, however, can be used to good advantage to reduce power consumption in certain applications by lowering the V_{cc} . Circuit speeds will decrease but proper system design will take this into account.

V_{BE} VARIATIONS

Another variation with temperature is the V_{BE} of the transistors within the circuit. The amount of V_{BE} change with temperature will directly affect the current flow through a resistor in series with the base of a transistor. The V_{BE} also will change as a function of base current and collector current. Figures 9 and 10 show the V_{BE} vs. temperature plot of the microcircuit transistors as a function of base and collector currents. These curves are taken from laboratory data (listed in the Appendix). All previous examples used $V_{BE} = 0.7$ V as a typical value at room temperature. As seen in Figs. 9 and 10, the 0.7 V value previously used is lower than the actual V_{BE} of a typical microcircuit transistor at room temperature. This is why the computed power consumption of Fig. 1 and 2 was slightly higher than the specified typical specification limits.

The rate of V_{BE} change with temperature for a forward-biased junction is inversely proportional to the forward current. Typically, from 1 to 1000 μ A the temperature coefficient (dV_{BE}/dT) is 2.2 to 2.3 mV/

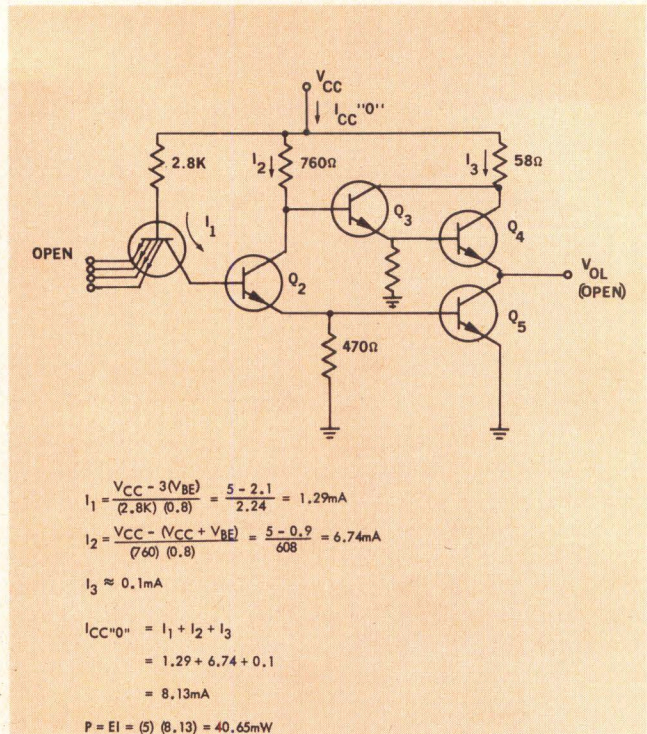


Fig. 7 0 State Current With -20% Resistors.

Table 2 % Change In Power Consumption For -20% In Resistor Value.

$$P = \frac{V^2}{R}$$

Assume R decreases by 20%

$$P' = \frac{V^2}{0.8R} \quad \Delta P = P' - P = \frac{V^2}{0.8R} - \frac{V^2}{R}$$

$$\% \text{ Change of } P = \frac{\Delta P}{P} \times 100$$

$$\% \text{ Change of } P = \frac{\frac{V^2}{0.8R} - \frac{V^2}{R}}{\frac{V^2}{R}} \times 100 = \left(\frac{1}{0.8} - 1 \right) 100$$

$$= 25\%$$

A decrease in R of 20% will increase P by 25%.

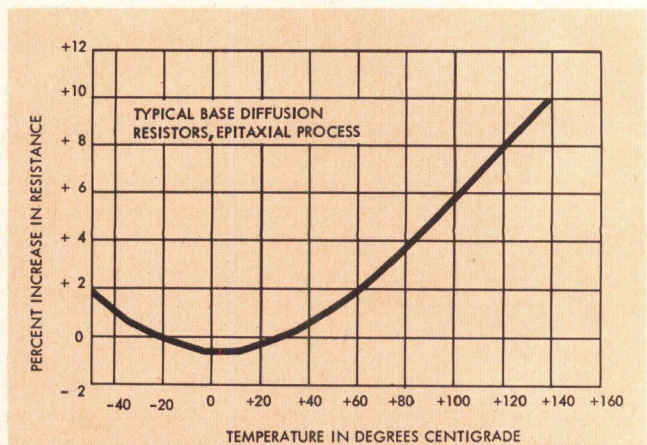


Fig. 8 Change In Resistance vs Temperature.

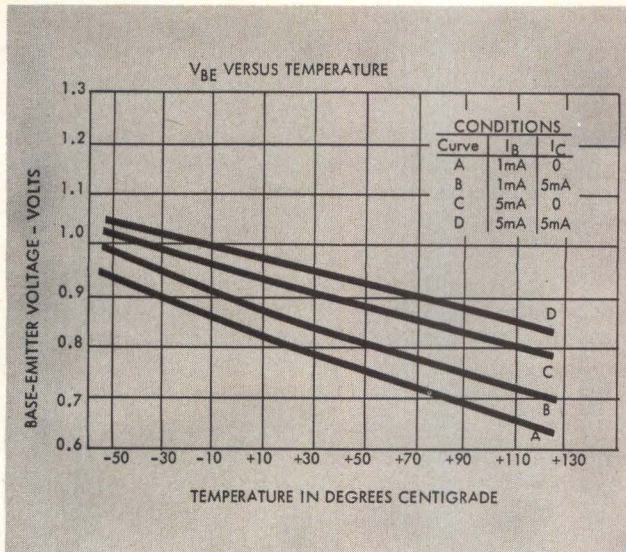


Fig. 9 V_{BE} Curve For Intermediate Size Microcircuit Transistor.

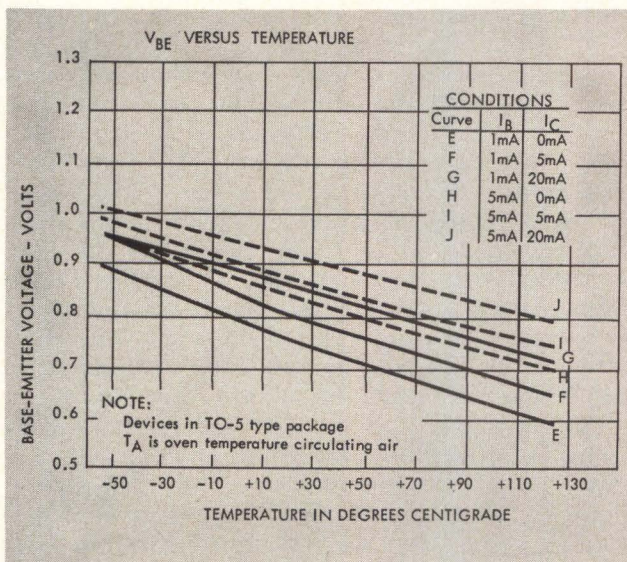


Fig. 10 V_{BE} Curve For Large Size Microcircuit Transistor.

Table 3 Calculated Worst-Case Power Consumption Over Temperature.

	-55 C	0 C	25 C	125 C
0 Level Current	5.80 mA	6.10	6.19	6.14
1 Level Current	2.64	2.78	2.78	2.74
Total	8.44	8.88	9.97	8.88
50% duty power consumption	21.10 mW	22.20	24.92	22.20

$^{\circ}\text{C}$. However, as the base current increases, the temperature coefficient decreases to approximately $1.5 \text{ mV}/^{\circ}\text{C}$ at 1 mA base current and to $1.3 \text{ mV}/^{\circ}\text{C}$ at 5 mA base current. Further information on V_{BE} characteristics is provided in the Appendix.

V_{CE} VARIATIONS

It was evident that variations in V_{CC} , V_{BE} , and resistor tolerances can affect the actual dc power consumption of a circuit. Another parameter which varies with temperature is $V_{CE(SAT)}$. For the current levels of the internal transistors used in the NAND gate of the example, this variation is small, ranging almost linearly from 0.13 V at -55°C to 0.23 V at $+125^{\circ}\text{C}$.

EXAMPLES

Two questions arise for which the answer can now be determined: (1) How much power is consumed under worst-case conditions and (2) is 25°C the proper ambient temperature for assuring worst case power consumption?

TEMPERATURE FOR WORST-CASE

By answering the second question first, the designer should be able to reduce the parameter of temperature to a single value for worst-case power consumption.

From the graphs in Figs. 9 and 10, determine the proper V_{BE} value to use as a function of temperature. Resistor percentage change is determined from Fig. 8. V_{CE} and leakage values also vary with temperature. The values used are listed in the Appendix along with the calculations of the results. Computing power consumption in the same manner used in Figs. 1 and 2 produces the values shown in Table 3.

The power consumption is maximum at 25°C for the four temperature values computed. Further determination of the exact temperature, where maximum power consumption occurs, could be performed but there is less than 0.6 mW between the lowest and highest 50% duty cycle power consumption for the temperature values shown. Consequently, the determination of maximum power consumption can be done at room temperatures. This eliminates the need for ovens to obtain this parameter.

DETERMINING WORST-CASE POWER CONSUMPTION

The worst-case quiescent power consumption for the NAND gate can now be computed. The parameter values at 25°C will provide this information. The values used and the computation is provided in the Appendix. The results indicate that I_{CC} maximum 0 level is 7.87 mA and I_{CC} maximum 1 level is 3.46 mA .

From this, note that as much as 39.35 mW for the 0 level and 17.30 mW for the 1 level could be measured in a good device. A 50% duty cycle power consumption of 28.32 mW is possible. However, the distribution curve for power consumption follows a normal bell-shaped curve and units at the upper extreme of power consumption would occur quite infrequently. Any units above these computed values would be rejected.

POWER DISSIPATION

For the packaging engineer, the amount of heat generated within the microcircuit package must be known, along with the thermal resistance of the package, in order to determine at what temperature the silicon chip is operating. Silicon transistor junction operating temperature is usually specified at a maximum of 175° C. Beyond this, thermal run-away can occur which would destroy the device. Similarly, microcircuit chips are rated at a maximum junction temperature (T_J) of 150° C. This lower value is lower since the overall complexity of a microcircuit is substantially more complex than a transistor and actual hot-spots are difficult to locate or predict. Overall average chip operating temperature should not exceed 150° C.

HEAT TRANSFER MECHANISM

The mechanism by which heat is transferred from the heat-generating area to the outside environment is threefold: conduction, convection, and radiation. Convection within a microcircuit package is slight and radiation is miniscule, since most packages are essentially opaque to electromagnetic radiation with wavelengths in the infra-red region. Essentially, the predominant method of heat transfer is by conduction from the chip to the microcircuit package. Heat conducted to the package is transferred to the ambient atmosphere by convection and radiation or by conduction through the package and leads to the mounting surface.

The entire transfer of heat from a chip to the final heat sink is a complex thermodynamic procedure. The

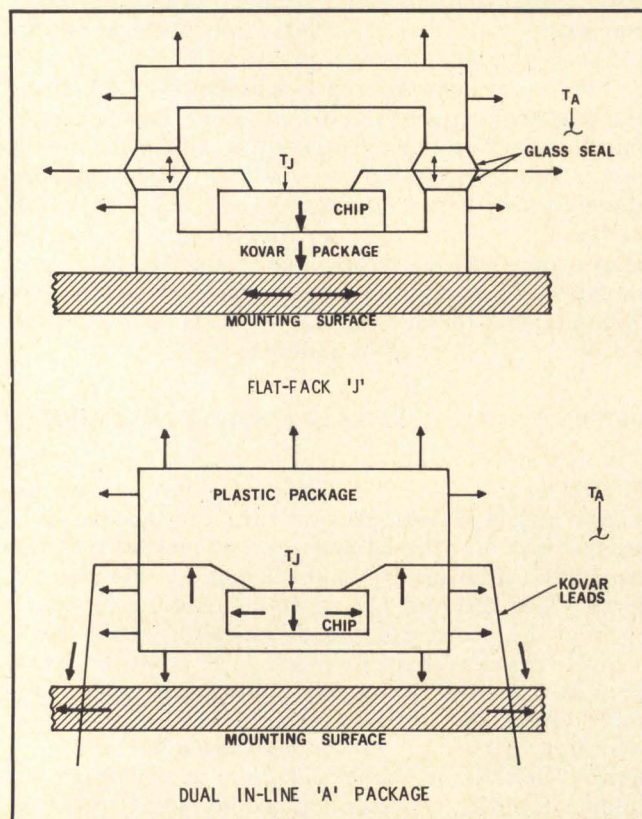


Fig. 11 Schematic Representation Of The Heat-Flow Paths For The 'J' And 'A' Packages.

heat is dissipated by the active and resistive elements on the top surface of the silicon die. Since silicon is a fairly good conductor of heat, the heat generated becomes distributed throughout the die and is transferred by conduction to the package. Calculations have shown that the heat transfer by the internal leads, the internal free convection and radiation heat transfer directly from the die to the case, and the conduction heat transfer through the glass sealing the leads in flat packs are all negligible. Consequently, the predominant heat transfer is by conduction through the die to its mounting surface then to the package surface.

Figure 11 shows the heat flow through both the flat-pack (J) and the dual-in-line (A) packages. The conduction paths through the leads of the DIP are more significant than in the flat package, since more homogeneous package material is in contact with these leads. However, convection is still a very important means of heat transfer from the DIP and this fact should be kept in mind when designing mounting assemblies for these devices.

PACKAGE THERMAL RESISTANCE

The thermal resistance of an integrated circuit package determines the relationship of the chip temperature to the external ambient temperature as a function of the wattage developed by the operating circuit.

How can the thermal resistance of a microcircuit package be determined? Fortunately, the forward voltage drop of a PN junction has a linear temperature coefficient which provides an accurate means to measure the actual junction temperature within a mechanically-sealed environment. The V_{BE} curve of a PN junction is first calibrated. That is, its change per degree C is determined. This diode, which is part of a circuit, is then used as a reference to determine actual chip temperature while the circuit is functioning.

The entire circuit is packaged and the finished assembly is operated in a controlled environment. The power dissipation (consumption) of the chip is determined by the IV operating characteristics. The temperature rise of the chip is obtained from the diode V_F characteristics over the full range of operating ambient temperatures.

The power dissipation vs. chip temperature (no heat sink) determines θ_{JA} (thermal resistance to air). This test evaluates the worst-case operating condition. Power dissipation vs. chip temperature (infinite heat sink) determines θ_{JC} (thermal resistance to case). This test evaluates an ideal case operating condition.

The standard J flat-pack was determined to have a θ_{JA} of 0.30°C/mW and the A case (DIP) to have a $\theta_{JA} = 0.23^\circ\text{C}/\text{mW}$. The θ_{JC} of the A case has been measured to be 0.119°C/mW to 0.132°C/mW, and the flat-pack $\theta_{JC} = 0.15^\circ\text{C}/\text{mW}$.

EXAMPLE

From the θ_{JA} of a DIP it is possible to determine the worst-case operating temperature of a junction within the chip of the NAND gate in Fig. 1. As determined, the worst-case 50 % duty cycle (low repetition rates)

of the NAND gate is 28.32 mW. With a thermal resistance from chip-to-ambient of $0.23^{\circ}\text{C}/\text{mW}$, the chip temperature above the ambient is $(0.23)(28.32) = 6.5^{\circ}\text{C}$. At $T_A = 125^{\circ}\text{C}$ (no heat sink), the chip temperature can be expected to be close to 132°C , well below the 150°C maximum stated previously.

POWER CONSUMPTION VS OPERATING FREQUENCY

The 50 % duty cycle power consumption of TTL circuits is equal to the average of the 0 state and 1 state power consumption levels for operating frequencies up to about 1 MHz. But as the clock rate increases further, the average power consumption also increases. System speed, therefore, becomes an important parameter when power consumption and power dissipation must be determined.

REASON POWER CONSUMPTION INCREASES

Power consumption increases with speed in high level TTL devices because the output is from the node of a pull-down transistor collector and an active pull-up transistor emitter. Inherent circuit delays and device switching characteristics cause both of these output transistors to be momentarily ON during the 1 to 0 transition (t_{THL}) and the 0 to 1 transition (t_{TLH}). Consequently, a momentary low impedance path between V_{cc} and ground occurs, resulting in current-spiking. This current-spiking increases the overall power consumption of the device.

The V_{cc} current-spiking for a given external load is constant in amplitude and duration. As the repetition rate of 0 and 1 conditions increase, the current-spiking time period becomes more and more a significant contributor to the overall power consumption requirements.

Figure 12 shows a plot of the average power consumption for 25 gates from zero to 50 MHz. This curve has been normalized to reflect the 21.2 mW power consumption of a typical gate. The power consumption increases at a rate of approximately $0.22 \text{ mW}/\text{MHz}$. At a clock rate of 50 MHz, the gate power consumption has increased to 32 mW.

Current-spiking is greatest when the output switches from the low to the high state. This becomes apparent when the operating states of each transistor are considered. When the output is low, the pull-down transistor is ON (fully saturated). The pull-up transistor is turned OFF and the phase-splitter transistor (operating as an emitter follower) is in a non-saturated condition.

When the ON bias is removed from the pull-down transistor, it begins to turn OFF. The base capacitance discharge path is through a 430 ohm resistor. This provides fast turn-off characteristics, but not as fast as the turn-on speed of the unsaturated pull-up transistor. Therefore, both output transistors are ON momentarily.

When the output is high, the pull-down transistor is OFF and the pull-up transistor may be ON depending upon the output voltage level.

If ON, it will be sourcing only a few milliamperes and consequently, is capable of fast turn-off. At the next change of state (1 level to 0 level) the pull-down transistor turns ON but not as fast as the pull-up

transistor turns OFF since the pull-down transistor must go into full saturation in order to sink the output load current. Current-spiking (if any) is minimal and is considerably less for the 1 to 0 transition. In most cases it is an insignificant contributor to overall power consumption.

EFFECT OF LOAD ON POWER CONSUMPTION

The t_{TLH} current-spiking is affected considerably more by the load at the output than by internal circuit delays. This is evident when considering the additional I_{cc} current required to charge external circuit capacitance at the output terminal. This additional current must come from the V_{cc} terminal of the driving gate during the 0 to 1 state transition. It is additive to the current-spiking already occurring due to the simultaneously ON condition of both output transistors.

Consequently, power consumption of the NAND gate increases as the capacitive load on the output increases. Measurements of the magnitude and duration of current-spiking have been taken as a function of load. This test procedure is shown in Fig. 13 and the results are listed in Table 4.

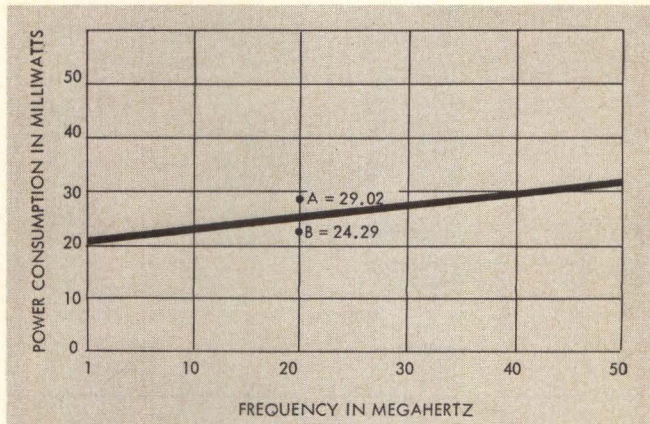


Fig. 12 Nand Gate Power Consumption vs Frequency—No Load.

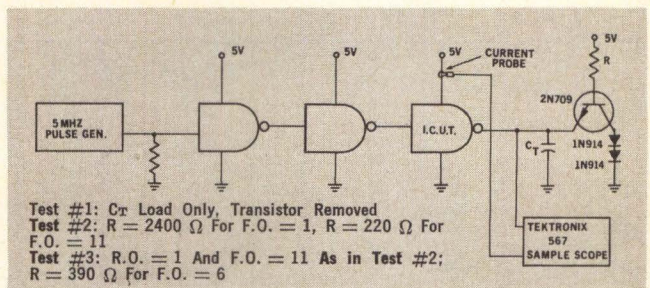


Fig. 13 Current Spiking Test.

Table 4 Current Spiking Measurements.

Test #1:	Load	Min. Amp. (mA)	Dura-tion (ns)	Max. Amp. (mA)	Dura-tion (ns)
	5 pF	14.2	3.2	22.8	4.2
	15 pF	19.2	3.8	25.4	4.7
	50 pF	27.0	6.5	31.4	7.2
	100 pF	42.4	9.3	43.0	10.3
Test #2:	F. O. = 1; 5 pF	25.4	3.5	37.4	4.3
	F. O. = 11; 30 pF	35.8	4.7	50.0	6.2
Test #3:	F. O. = 1; 15 pF	27.6	3.6	38.4	4.6
	F. O. = 6; 15 pF	27.8	3.6	42.2	4.9
	F. O. = 11; 15 pF	27.8	3.8	45.6	5.3

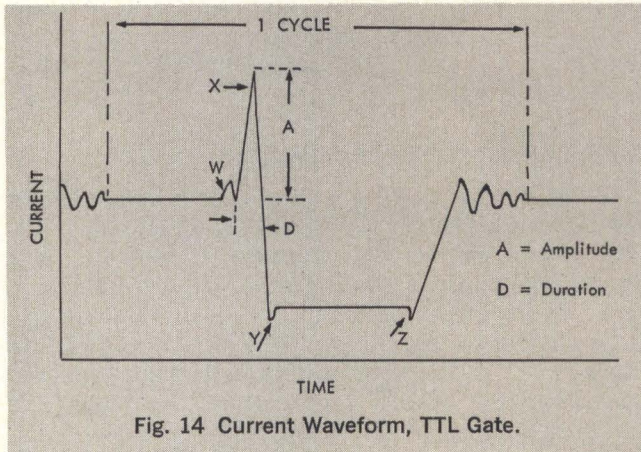


Fig. 14 Current Waveform, TTL Gate.

Table 5 Additional Power Consumption Caused By Current Spike.

Area of spike X in Figure 14 = Coulombs = Q
Units Equations
$Q = \frac{1}{2} (\text{spike duration}) (\text{spike amplitude})$
$Q = \frac{1}{2} DA$
$\Delta I, \text{ Due to spiking} = (Q) (\text{Frequency})$
$\Delta I = \frac{(D) (A) (\text{Frequency})}{2}$
$\Delta P, \text{ Due to spiking} = (\Delta I) (V_{cc})$
$\Delta P = \frac{(D) (A) (\text{Frequency}) (V_{cc})}{2}$
Dimensional Equations
$\frac{(\text{Time}) (\text{Current})}{(\text{Time}) (\text{Current})} = \text{Current}$
$\frac{(\text{Coulombs}) (\text{Hertz})}{(\text{Time}) (\text{Current})} = \text{Current}$
$\frac{(\text{Current}) (\text{Voltage})}{(\text{Watts})}$

Table 6 Additional Power Consumption At Fan Out = 1, 5pF; Frequency = 20MHz.

F. O. = 1,5 pF 0 level quiescent current = 6.0mA Frequency = 20MHz
Min. Additional Power
$\Delta P_{min} = \frac{(3.5) (10^{-9}) (25.4 - 6.0) (10^{-9}) (20) (10^6) (5)}{2}$
$= \frac{(3.5) (19.4) (20) (10^{-9}) (5)}{2}$
$= (679) (10^{-6}) (5)$
$\Delta P_{min} = 3.39 \text{ mW}$
Max. Additional Power
$\Delta P_{max} = \frac{(4.3) (42.4 - 6.0) (20) (5) (10^{-6})}{2}$
$= (1565) (10^{-6}) (5)$
$\Delta P_{max} = 7.82 \text{ mW}$

Table 7 Min. — Max. Power Consumption of Typical NAND Gate At 20 MHz.

Min. Power of NAND at 20MHz 21.2 + 3.39 = 24.59 mW
Max. Power of NAND gate at 20 MHz 21.2 + 7.82 = 29.02 mW

As stated before, the amplitude and duration of the current spike remains constant as the operating speed changes. The current spike becomes a proportionately larger contributor to overall average power consumption as the speed increases.

Figure 14 shows the V_{cc} current waveform of a TTL gate during the switching transitions. The current magnitude of a NAND gate is opposite to voltage output and the higher current level occurs during the 0 state.

Several current spikes are shown. The W spike has a positive direction and the Y and Z spikes are negative. Essentially, these current surges cancel each other when overall current is considered. The ringing pulses cancel similarly, although a small positive component remains. This amount is overshadowed by the large current spike indicated at X. This X spike is the one which contributes considerably to the overall power consumption and must be considered when determining the additional current required at a given frequency and load.

First determine the amount of charge required per spike and then determine the total amount of charges required for a given frequency. This states the additional current required.

The area under the pulse spike curve X provides the charge-per-spike. Since the curve shape is essentially a triangle, the area is one-half the pulse duration times the pulse amplitude.

This area has the units of current multiplied by time (coulombs). Multiplying coulombs times the number of times the spike occurs (frequency of operation) produces the total current requirement of all the spikes. Once the additional current required is known, the additional power requirement can be obtained by multiplying the current times the supply voltage. This is shown in Table 5.

The derivation of additional power for F.O. = 1 (5 pF load) is shown in Table 6. Minimum and maximum values are derived from the experimental results recorded in Table 4. The total current amplitude is shown in Table 4 and the quiescent 0 level current must be subtracted from this value to determine spike amplitude A.

To check the foregoing, determine the power consumption at 20 MHz of the standard NAND gate. Quiescent power consumption is 21.2 mW. Add the results from Table 6 to this value as shown in Table 7.

The NAND circuit will require 24.59 mW minimum and 29.02 mW maximum at 20 MHz, loaded with F.O. = 1, 5 pF. These values are plotted on the graph in Fig. 12 at points B and A, respectively. Points A and B fall above and below the average power consumption curve shown, but the curve does not fall exactly between these points. This is to be expected. The curve is for an unloaded gate and points A and B are for a lightly-loaded gate. The difference between the center point of A and B and the curve at 20 MHz is the additional power consumption required by the load. The difference between the curve of 20 MHz and the quiescent power consumption of 21.2 mW is the additional power consumption

caused by the two output transistors both being momentarily ON.

The foregoing procedure has been used to determine the additional power consumption of a typical NAND gate as a function of load and frequency. The unloaded current transient is included in these results since it is also included in the data recorded in Table 4. A chart showing the computed results is provided in the Appendix and plots to this information are shown in Figs. 15, 16, and 17.

The following graphs illustrate the effect which external load has upon power consumption as the frequency increases. A high capacitive load is by far the worst condition, since all of the charging current must come from the driving circuit. But even a lightly-loaded gate could almost double in power consumption at a 50 MHz operating rate.

SUMMARY

The power consumption of a high speed TTL circuit is affected by internal component parameter changes, temperature, bias voltage, speed of operation, and loading.

The specifications provide power consumption at $T_A = 25^\circ\text{C}$, a defined load (usually 0), and for a nominal V_{cc} . When various loads are used at speeds exceeding 1 MHz, the additional power consumed must be considered.

The dissipation of this power is an important consideration in the design of assemblies containing microcircuits. The thermal design of most circuits is conservative enough to allow operation at 125°C ambient, with chip temperatures remaining below 150°C at maximum frequency and worst-case power consumption. The worst-case NAND gate, previously described, consumed 28.32 mW at low speeds. At 50 MHz with a 100 pF load, it would possibly consume an additional 47.63 mW. This total of 75.95 mW would cause the chip temperature to raise 17.5°C above the ambient, if all heat transfer were by convection from the package. At $T_A = 125^\circ\text{C}$, the chip would be at 142.5°C . Even in this unlikely worst-case condition, the chip would remain below 150°C .

The important point to remember is that more power is required as the operating speed increases. As a consequence, circuits may exceed rated nominal power consumption. The designer must be aware of these variations and consider them when providing a power source and when designing the necessary thermal transfer mechanisms to remove heat from the microcircuit package assemblies.

APPENDIX

Temperature For Worst-Case

The curves plotted in Figs. 9 and 10 were obtained from data taken from a sample of several typical microcircuit transistors. The units were packaged in TO-5 type cans and were tested in an over-controlled ambient temperature of circulating air. This test condition is similar to actual microcircuit operating conditions. That is, the transistor junction temperature

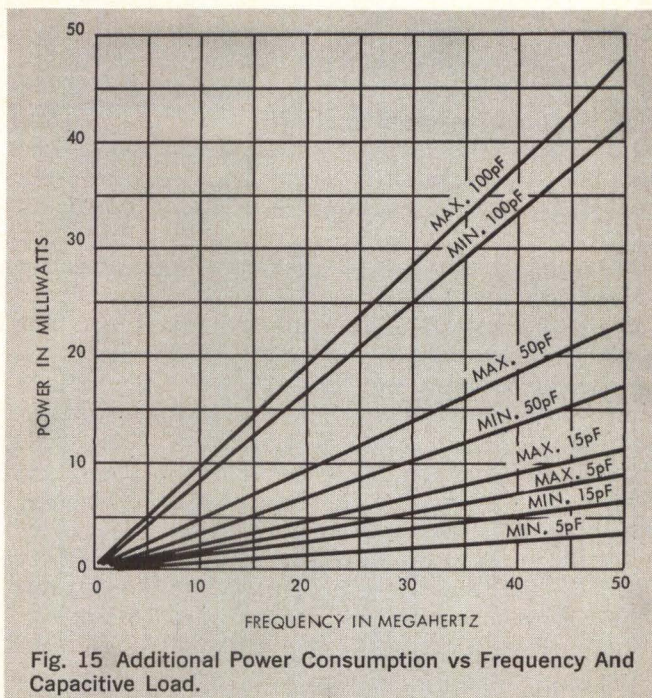


Fig. 15 Additional Power Consumption vs Frequency And Capacitive Load.

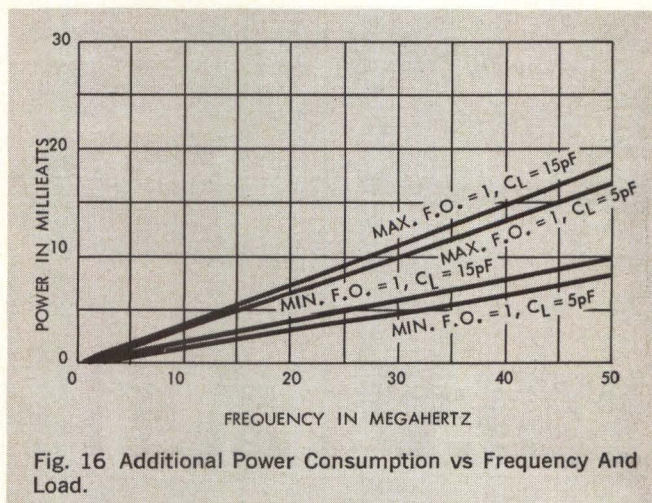


Fig. 16 Additional Power Consumption vs Frequency And Load.

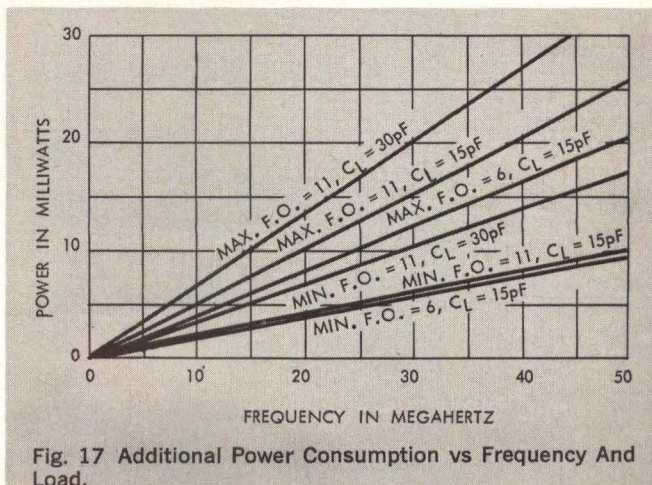


Fig. 17 Additional Power Consumption vs Frequency And Load.

was actually higher than the ambient and consequently the resulting curves do not represent the V_{BE} of the chips if they were at the recorded ambient temperature. In normal operating conditions, the ambient temperature is the controllable parameter and this data reflects the effect of the ambient temperature upon V_{BE} of the device which the user would encounter.

The chart below lists the measuring conditions and the measured values of V_{BE} .

Note that the size of the transistor affects V_{BE} . The larger output transistor has close to the same V_{BE} as the intermediate size transistor for low base currents. As the base drive increases, the output transistor V_{BE} becomes correspondingly lower. This effect can be attributed to the larger geometry of the output transistor providing less resistance in the current path, hence, there is less effect from IR drop.

The measured and extrapolated values which were used to determine at which temperature worst-case power consumption occurs are recorded below.

V _{BE} of Intermediate Size Geometry Transistors				
Temp.	V _{BE}			
	I _B = 1 mA		I _B = 5 mA	
	I _C = 0 mA	I _C = 5 mA	I _C = 0 mA	I _C = 5 mA
-55 C	0.95V	1.0V	1.04V	1.06V
+25 C	0.80V	0.85V	0.92V	0.96V
+125 C	0.63V	0.70V	0.78V	0.83V
Calculated Temp. Coefficient	1.85mV/°C	1.69mV/°C	1.39mV/°C	1.27mV/°C

V _{BE} of Large Size Geometry Output Transistor						
Temp.	V _{BE}					
	I _B = 0 mA			I _B = 5 mA		
	I _C = 0 mA	I _C = 5 mA	I _C = 20 mA	I _C = 0 mA	I _C = 5 mA	I _C = 20 mA
-55 C	0.90V	0.96V	0.96V	0.96V	0.98V	1.02V
+25 C	0.75V	0.80V	0.87V	0.84V	0.87V	0.92V
+125 C	0.58V	0.65V	0.72V	0.70V	0.74V	0.80V
Calculated Temp. Coefficient	1.79mV/°C	1.75mV/°C	1.31mV/°C	1.45mV/°C	1.34mV/°C	1.22mV/°C

Parameter Values For Determining Worst-Case Temperature.

	-55 C	0 C	25 C	125 C
V _{BEQ1} (Curve A, Fig. 9)	0.95V	0.84	0.80	0.63
V _{BEQ2} (Curve B, Fig. 9)	1.0	0.89	0.85	0.70
V _{BEQ3} (Curve B, Fig. 9)	1.0	0.89	0.85	0.70
V _{BEQ5} (Curve H, Fig. 10)	0.96	0.87	0.84	0.70
% Change from Fig. 8	(+2%)	(-.5%)	(+.3%)	(+8.5%)
4K	4080	3980	4012	4340
2.8K	2856	2786	2808	3138
760	775	756	762	825
58	59	57	58	63
V _{CE} (See Text)	0.13V	0.15	0.16	0.23
Leakage (See Text)	0.01mA	0.03	0.05	0.10

Computation for Worst-Case Temperature

Following is the method used for determining maximum power consumption over the full temperature range from -55° C to +125° C for both the 0 and the 1 state conditions.

Current for 0 Level State

-55 C

$$I_1 = \frac{V_{CC} - V_{BEQ1} - V_{BEQ2} - V_{BEQ5}}{2856} = \frac{5 - 0.95 - 1.0 - 0.96}{2856} = \frac{2.09}{2856} = 0.74 \text{ mA}$$

$$I_2 = \frac{V_{CC} - V_{CEQ2} - V_{BEQ5}}{775} = \frac{5 - 0.13 - 0.96}{775} = \frac{3.91}{775} = 5.05 \text{ mA}$$

$$I_3 = \text{Leakage} = 0.01 \text{ mA}$$

$$\text{Total } I = I_1 + I_2 + I_3 = 0.74 + 5.05 + 0.01 = 5.80 \text{ mA}$$

0 C

$$I_1 = \frac{5 - 0.84 - 0.89 - 0.87}{2786} = \frac{2.40}{2786} = 0.81 \text{ mA}$$

$$I_2 = \frac{5 - 0.15 - 0.87}{756} = \frac{3.98}{756} = 5.26 \text{ mA}$$

$$I_3 = \text{Leakage} = 0.03 \text{ mA}$$

$$\text{Total } I = I_1 + I_2 + I_3 = 0.81 + 5.26 + 0.03 = 6.10 \text{ mA}$$

+25 C

$$I_1 = \frac{5 - 0.80 - 0.85 - 0.84}{2808} = \frac{2.51}{2808} = 0.89 \text{ mA}$$

$$I_2 = \frac{5 - 0.16 - 0.84}{762} = \frac{4.00}{762} = 5.25 \text{ mA}$$

$$I_3 = \text{Leakage} = 0.05 \text{ mA}$$

$$\text{Total } I = I_1 + I_2 + I_3 = 0.89 + 5.25 + 0.05 = 6.19 \text{ mA}$$

+125 C

$$I_1 = \frac{5 - 0.63 - 0.70 - 0.70}{3138} = \frac{2.97}{3138} = 0.95 \text{ mA}$$

$$I_2 = \frac{5 - 0.10 - 0.70}{825} = \frac{4.2}{825} = 5.09 \text{ mA}$$

$$I_3 = \text{Leakage} = 0.10 \text{ mA}$$

$$\text{Total } I = I_1 + I_2 + I_3 = 0.95 + 5.09 + 0.10 = 6.14 \text{ mA}$$

Current for 1 Level State (Assume β of Q₃ = 50)

-55 C

$$I_1 = \frac{V_{CC} - V_{BEQ1}}{2856} = \frac{5 - 0.95}{2856} = \frac{4.05}{2856} = 1.42 \text{ mA}$$

$$I_2 = \frac{V_{CC} - V_{BEQ3}}{775 + 4080(\beta + 1)} = \frac{5 - 1.0}{775 + 204,000 + 4080} = \frac{4}{208,855} = 0.019 \text{ mA}$$

$$I_3 = \frac{V_{CC} - V_{CEQ3}}{59 + (4080/\beta) + 4080} = \frac{5 - 0.13}{59 + 81 + 4080} = \frac{4.87}{4220} = 1.18 \text{ mA}$$

$$I_4 = 2 \text{ times leakage of } Q_2 + Q_5 = 0.02 \text{ mA}$$

$$\text{Total } I = I_1 + I_2 + I_3 + I_4 = 1.42 + 0.019 + 1.18 + 0.02 = 2.64 \text{ mA}$$

0 C

$$I_1 = \frac{5 - 0.84}{2786} = \frac{4.16}{2786} = 1.49 \text{ mA}$$

$$I_2 = \frac{5 - 0.89}{756 + 3980(\beta + 1)} = \frac{4.11}{203,736} = 0.020\text{mA}$$

$$I_3 = \frac{5 - 15}{57 + (3980/\beta) + 3980} = \frac{4.85}{4017} = 1.21\text{mA}$$

$$I_4 = 2 \text{ times leakage of } Q_2 \text{ \& } Q_5 = 0.06$$

$$\text{Total } I = I_1 + I_2 + I_3 + I_4 = 1.49 + 0.02 + 1.21 + 0.06 = 2.78\text{mA}$$

+25 C

$$I_1 = \frac{5 - 0.80}{2808} = \frac{4.2}{2808} = 1.5\text{mA}$$

$$I_2 = \frac{5 - 0.85}{762 + 4012(\beta + 1)} = \frac{4.15}{205,374} = 0.02\text{mA}$$

$$I_3 = \frac{5 - 0.16}{58 + (4012/\beta) + 4012} = \frac{4.84}{4150} = 1.16\text{mA}$$

$$I_4 = \text{Leakage of } Q_2 \text{ \& } Q_5 = 0.1\text{mA}$$

$$\text{Total } I = I_1 + I_2 + I_3 + I_4 = 1.5 + 0.02 + 1.16 + 0.1 = 2.78\text{mA}$$

+125 C

$$I_1 = \frac{5 - 0.63}{3138} = \frac{4.37}{3138} = 1.39\text{mA}$$

$$I_2 = \frac{5 - 0.70}{825 + 4340(\beta + 1)} = \frac{4.3}{223,165} = 0.02\text{mA}$$

$$I_3 = \frac{5 - 0.23}{63 + (4380/\beta) + 4080} = \frac{4.77}{4230} = 1.13\text{mA}$$

$$I_4 = 2 \text{ times leakage of } Q_2 \text{ \& } Q_5 = 0.2\text{mA}$$

$$\text{Total } I = I_1 + I_2 + I_3 + I_4 = 1.39 + 0.02 + 1.13 + 0.2 = 2.74\text{mA}$$

A summary of the results obtained from the foregoing calculations is provided in the text.

Determining Worst-Case Power Consumption

The worst-case power consumption for the NAND gate would be computed for $T_A = 25^\circ\text{C}$ and all resistors are -20% of the nominal value. V_{cc} is held at 5 V dc.

Parameter Values for Worst-Case Power Consumption

$V_{BE}Q_1 = 0.80\text{V}$	4K resistor = 3.2K	$V_{CE} = 0.16\text{V}$
$V_{BE}Q_2 = 0.85\text{V}$	2.8K resistor = 2.24K	Leakage = 0.05mA
$V_{BE}Q_3 = 0.85\text{V}$	760 resistor = 607	$V_{CC} = 5.0\text{V}$
$V_{BE}Q_5 = 0.84\text{V}$	58 resistor = 46	$\beta = 70$

0 Level Power

$$I_1 = \frac{2.51}{2240} = 1.12\text{mA}$$

$$I_2 = \frac{4.00}{607} = 6.70\text{mA}$$

$$I_3 = \text{Leakage} = 0.05\text{mA}$$

$$\text{Total Current} = 7.87\text{mA}$$

$$\text{Power Consumption} = 39.35\text{mW}$$

1 Level Power

$$I_1 = \frac{4.2}{2240} = 1.875\text{mA}$$

$$I_2 = \frac{4.15}{607 + 3200(3 + 1) + 0.18\text{mA}} = \frac{4.15}{227,807}$$

$$I_3 = \frac{4.84}{46 + (3200/\beta) + 3200} = \frac{4.84}{3291} = 1.47$$

$$I_4 = \text{Leakage of } Q_2 \text{ \& } Q_5 = 0.1\text{mA}$$

$$\text{Total Current} = 3.46\text{mA}$$

$$\text{Power Consumption} = 17.30\text{mW}$$

50% Duty Cycle Power

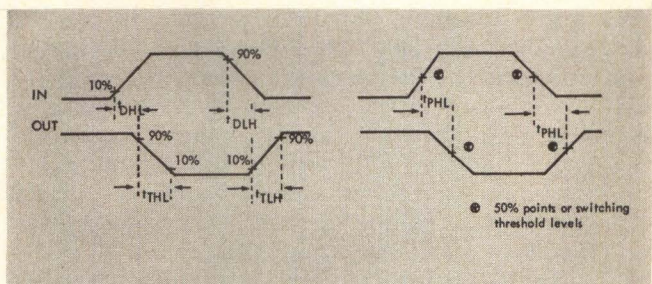
$$\begin{aligned} 50\% \text{ Power} &= \frac{0 \text{ level power} + 1 \text{ Level Power}}{2} \\ &= \frac{39.35 + 17.30}{2} \\ &= 28.32 \text{ mW} \end{aligned}$$

Letter Symbols

The following letter symbols are used in specifications for the Sprague high-speed TTL product line.

- H = HIGH state
- L = LOW state
- O = OUTPUT
- I = INPUT
- N = NODE
- Max. = maximum
- Min. = minimum
- $V_{OL \text{ max.}}$ = Low State Output Maximum Voltage
- $V_{OL \text{ min.}}$ = Low State Output Minimum Voltage
- $V_{OH \text{ max.}}$ = High State Output Maximum Voltage
- $V_{OH \text{ min.}}$ = High State Output Minimum Voltage
- $V_{IL \text{ max.}}$ = Low State Input Maximum Voltage
- $V_{IL \text{ min.}}$ = Low State Input Minimum Voltage
- $V_{IH \text{ max.}}$ = High State Input Maximum Voltage
- $V_{IH \text{ min.}}$ = High State Input Minimum Voltage
- $V_{INL \text{ max.}}$ = Low State Node Input Maximum Voltage
- $V_{INL \text{ min.}}$ = Low State Node Input Minimum Voltage
- $t_{PLH} (t_{pd})$ = Low to High State Output Propagation Delay Time
- $t_{PLH} (t_{pdo})$ = High to Low State Output Propagation Delay Time
- $t_{DLH} (t_{di})$ = Low to High State Output Delay Time
- $t_{DHL} (t_{do})$ = High to Low State Output Delay Time
- $t_{TLH} (t_i)$ = Low to High State Output Transition Time
- $t_{THL} (t_o)$ = High to Low State Output Transition Time

Note: $I_{OL \text{ max.}}$ would be used for Low State Output Maximum Current, etc. Symbols in parentheses are previously used terminology and are shown for reference only.



Additional Power Consumption Caused by Load and Frequency

The following records the computed additional power consumption as a function of load and frequency as described in the text.

Additional Power Consumption vs Frequency & Load.

Load	Power in Milliwatts					
	10 MHz		20 MHz		50 MHz	
	Min.	Max.	Min.	Max.	Min.	Max.
5pF	0.65	1.76	1.91	3.52	3.28	8.82
15pF	1.25	2.27	2.50	4.55	6.27	11.39
50pF	3.41	4.67	6.82	9.34	17.06	23.36
100pF	8.46	9.52	16.92	19.05	42.31	47.63
F.O. = 1,5pF	1.69	3.37	3.39	6.75	8.48	16.89
F.O. = 1,15pF	1.95	3.73	3.89	7.46	9.74	18.67
F.O. = 6,15pF	1.96	4.17	3.93	8.33	9.82	20.8
F.O. = 11,15pF	2.07	5.24	4.15	10.49	10.04	26.2
F.O. = 11,30pF	3.50	6.82	7.00	13.65	17.50	34.1

The application of optical character recognition systems is described in this article along with a discussion of the basic components that go into the make-up of a typical system. The economics of OCR systems are then compared to those of punched card systems.

OPTICAL CHARACTER RECOGNITION*

Derek Oram

Honeywell Inc.
EDP Division
Waltham, Mass.

Optical character recognition (OCR) systems are rapidly evolving as an economic means of inputting data into a computer. An OCR system converts the data printed on original paper documents into digital representations of the printed data and transfers this data into the computer. This is to be compared to alternative methods which involve manual keypunching of the characters onto a punched card and entering data via a card reader into the computer, or the more modern technique of using a keyboard-to-tape or keyboard-to-disc data entry system.

This article will describe how an optical character reader is used in a typical application in the utilities industry. It will show that the present trend toward low cost OCR devices lowers the monthly document volume at which the OCR total systems cost becomes less than the comparable punched card total systems cost.

The article will then describe the basic elements that make up an optical character recognition system; the paper transport, optical scanner and recognition systems.

HOW OCR IS USED

The use of OCR is best illustrated by comparing a punched card system with an OCR system in a common business application. Such an application is a return media or billing system used in the utility business.

Punched Card System (See Fig. 1)

The bill containing name and address and billed amount is printed on 80-column punched cards tied together in continuous form. The continuous form is separated in a bursting machine to form individual punched cards, then each punched card is inserted in an envelope and mailed to the customer. The customer returns the 51-column portion of the 80-column card back to the central office together with his payment; the card is then keypunched with the customer's account number and amount of payment and the data is fed back into the computer via a card reader to update the customer's record. This act of manually keypunching the 51-column card is slow and usually requires verification for accuracy.



Derek Oram received an EE degree from Kingston Technical College, Surrey, England in 1954, a Graduate Diploma in Electronics, at Southampton University, Hampshire, England and an MSEE from Southern Methodist University in 1965. Upon graduation from Southampton, Derek joined Vickers Armstrong (Aircraft) Ltd. He spent over three years at the Univac Div. of Sperry Rand, working primarily on an OCR punch that read credit card invoices. In 1965, he joined Honeywell and is now project manager of

OCR product development; he is also working in the area of MICR. Derek is a member of Computer Design's Editorial Review Board.

*This article is a reproduction from the Fall 1968 Honeywell Computer Journal.

There are many variations of this basic punched card billing system, but they all involve printing and punching the card. Even if the card is machine punched (printing performed on a bill feed printer), keypunching is required to handle the exceptions; i.e., those bills only partially paid, typically some 10 percent of the total bills returned.

OCR System (See Fig. 2)

The bills are printed on paper forms (less expensive than punched card stock, and more amenable to decorative printing) with an additional line of machine readable characters for OCR scanning containing the account number and the amount billed. The paper forms are burst into individual documents, and mailed to the customer who returns a portion (stub) of the paper bill with his payment. If the bill is only partially paid, the amount submitted is recorded on the bill (by the office) by means of "mark sense" pencil marks written into the appropriate mark indicators as shown in Fig. 3. Mark sense is a very simple and reliable way of hand recording characters on a document which are then capable of being machine read.

All the documents are then fed into the document reader to transfer the data on the OCR scan line and mark sense field into the computer, to update the customer's account.

An additional benefit may be gained from the use of an optical character reader in this application; utility meter readings may be inputted to the computer by mark sensing this information on paper documents.

Another factor in the OCR system is the problem of handling reject documents. Since the OCR device is reading printed information rather than binary punched holes, the document reject rate is a function of the quality of the printing. This reject rate may vary from 0.001 percent when reading lithographed printing, to 1-5 percent when reading high speed printer printing, to 25 percent when reading gasoline credit card invoices. The reject documents may be re-entered into the computer by retyping the documents, mark sensing the reject documents or alternatively using key-to-tape devices. The cost of handling rejects has to be considered when calculating the total cost of the OCR system. As seen above, in the OCR system the human operations have been reduced to handling the exception and reject documents and the number of machine operations to complete the billing cycle have been reduced.

PUNCHED CARD VS. OCR BILLING SYSTEM COSTS

To show the economics of OCR versus the common punched card billing systems the total systems cost has been analyzed, including computer and peripheral rental, labor, mailing, and paper costs. The results of this analysis are shown on the graph in Fig. 4.

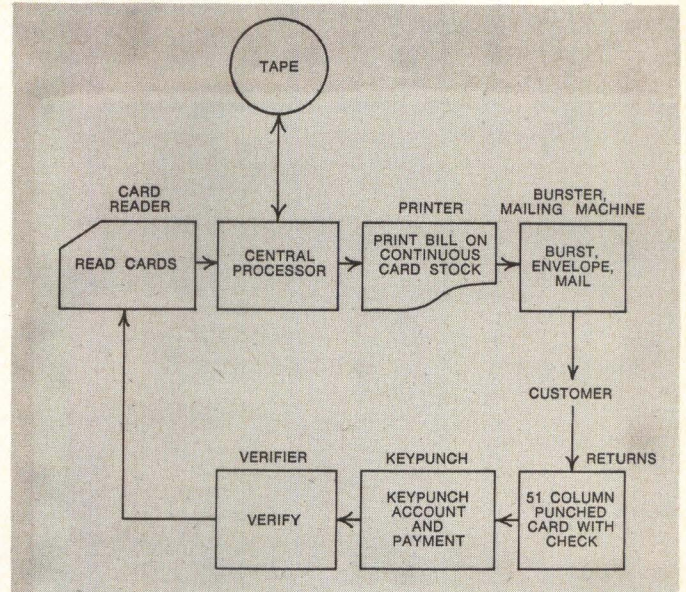


Fig. 1 Punched card billing system

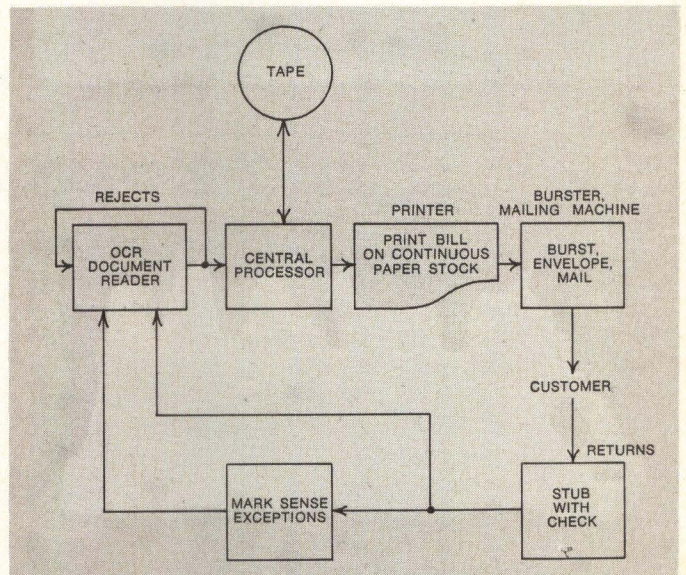


Fig. 2 OCR billing system

200 SMITH STREET
WALTHAM, MASS. 02154

Honeywell
ELECTRONIC DATA PROCESSING

DEKING ADDRESS
DEREK ORAM
45 JARMAN RD
SUDBURY MASS 01776

DISCOUNT DATE
NET AMOUNT PAYABLE
ON OR BEFORE
SEP 13 67
THEREAFTER
GROSS AMOUNT IS DUE
AMOUNT PAID

ACCOUNT NUMBER	TOTAL GROSS AMOUNT	TOTAL NET AMOUNT
141320 0116 06	436	417

WHEN PAYING AT OFFICE PLEASE BRING ENTIRE BILL
WHEN PAYING BY MAIL, PLEASE ENCLOSE THIS COUPON

MARK SENSE FIELD OCR SCAN LINE

NOTE: The mark sense characters shown correspond to 2.19c

Fig. 3 Typical OCR document

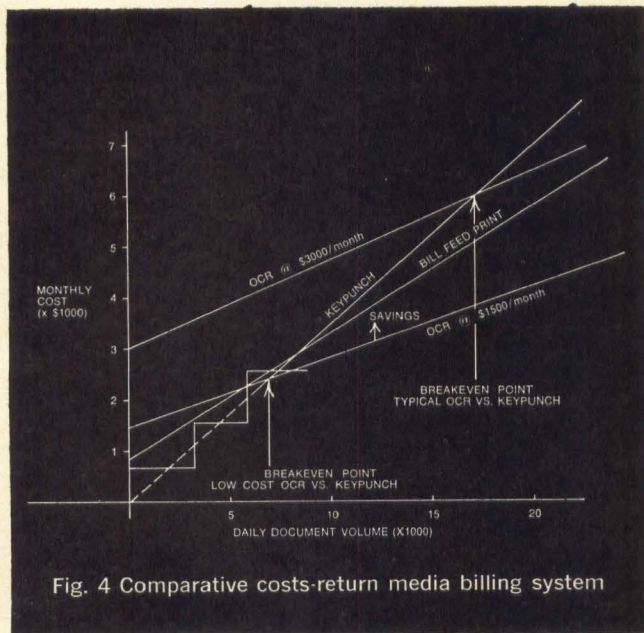


Fig. 4 Comparative costs-return media billing system

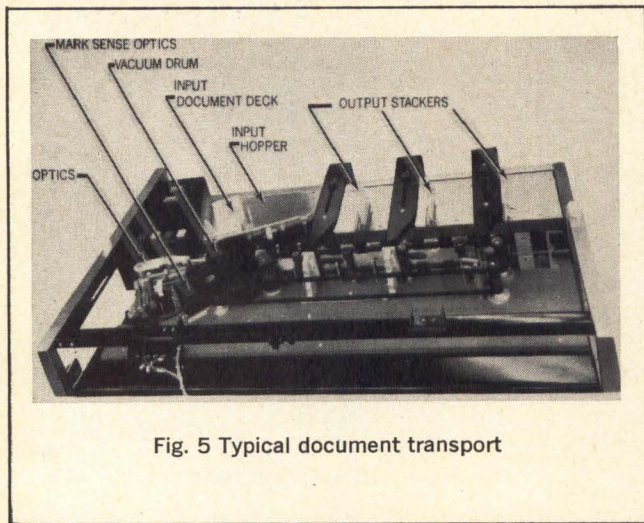


Fig. 5 Typical document transport

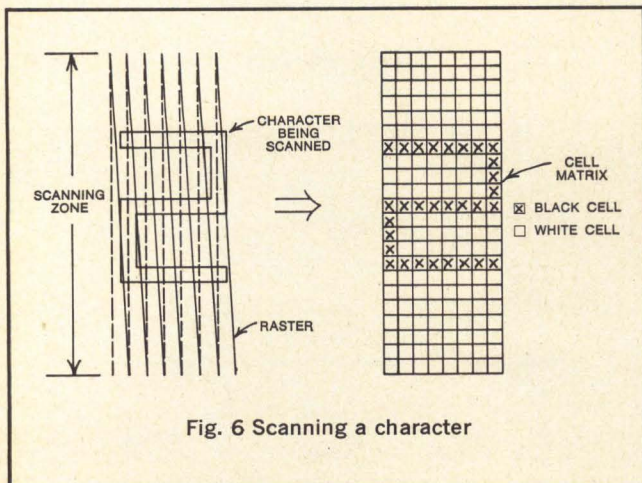


Fig. 6 Scanning a character

Typical document readers available today rent for between \$2,000-\$4,000 per month. It can be seen that the break-even point for a \$3,000 a month rental OCR document reader over the best punch card system is about 17,000 bills per day. For an OCR machine renting at \$1,500 per month the break-even point would be correspondingly lower, and the savings more dramatic—clearly, low cost OCR is very desirable. It is rapidly becoming a realizable goal.

OPTICAL CHARACTER READERS

Optical character readers may be classified into three types according to the type of documents that are read:

- Document readers which feed documents from 3 x 3 inches to 8 x 4 inches with a thickness ranging from 3 to 9 mils.
- Page readers which feed typically 8½ x 11 inch sheets of 3 to 4 mil thickness.
- Journal tape readers which read tapes in roll form such as those used in cash registers and adding machines.

All three types of optical character readers can also be broken down into three basic sub-systems: paper transport, optical scanner and recognition.

THE PAPER TRANSPORT

Paper transports come in many different sizes and shapes and are a subject unto themselves. One such document paper transport is shown in Fig. 5. To the right of the transport is the input hopper which contains the deck of documents to be read. The document separator transports one document at a time onto a vacuum drum which transports the document past the OCR optics and mark sense optics optical reading is done on the fly in this case. The document is then transported into one of three output stackers. Such a document transport (reader) is under the control of the computer, with each document being fed upon a feed command. The data on the document read by the optical character reader is then transferred to computer memory where it is manipulated and the decision made as to which pocket that document is to be stacked in. The use of the vacuum drum enables the optics to have an unrestricted view of the document so that the character line to be read may be located anywhere on the document.

A basic characteristic of this transport is its ability to transport documents from 3 x 3½ to 4 x 8 inches at a transport rate of 100 inches per second. This corresponds to a rate of 600 documents per minute for the 8-inch documents and up to 1100 documents per minute for the shortest ones.

OPTICAL SCANNING SYSTEM

The optical scanning system has the function of converting the printed information on the document into electrical signals that will enable the recognition system to recognize the printed characters. The typical scanning system slices the character many times vertically in a TV raster-like manner, and also divides each vertical scan into cells, so that the character is in effect characterized as a two-dimensional matrix of black and white cells (as shown in Fig. 6) for use by the recognition system. The scanning raster height is typically three times the height of the character to allow for vertical misregistration of the characters.

Early OCR systems used a rotating disk scanner invented by P. Nipkow in 1884 for television systems. This system is rapidly becoming obsolete, however, because of its mechanical complexity and speed limitations. A system largely used today is the flying spot scanner shown in Fig. 7.

The light output generated by the CRT electron beam is focused by a lens onto the document being read. The diffused reflected light from the document is focused by another lens onto a photomultiplier that converts the light energy into electrical energy which is amplified and sent to the recognition system. The CRT light beam is swept across the character in a raster-type scan by the CRT control logic. Since the light output from the CRT screen is non-uniform due to phosphor irregularities, an auxiliary feedback path is provided to dynamically adjust the beam current to achieve a more constant light output. The flying spot scanner thus has the advantage of extreme flexibility of scanning location on the document—with the document at a standstill, many lines of printing can be sequentially scanned. Furthermore, the resolution and scanning dimensions can be easily adjusted to accommodate varying font sizes.

A more simple, lower cost scanner is the solar cell scanner shown in Fig. 8. A high intensity light source illuminates the document which is in motion in the transport and the reflected image is focused onto a one-dimensional array of solar cells (a solar cell is a semiconductor photovoltaic device that converts light energy into electrical power). The output of each cell is amplified and quantized (the analog photo signal is converted into binary black-white signal). The output of each quantizer is connected to logic which converts the parallel signals into a sequential pulse train to create a raster-type scan output for the recognition system.

A variation of this scanner uses a two-dimensional array of solar cells so that the whole array of character cells is looked at in parallel. This of course radically increases the character reading rate, but is limited in application to very expensive recognition systems due to the large number of cells and amplifiers required (typically 800).

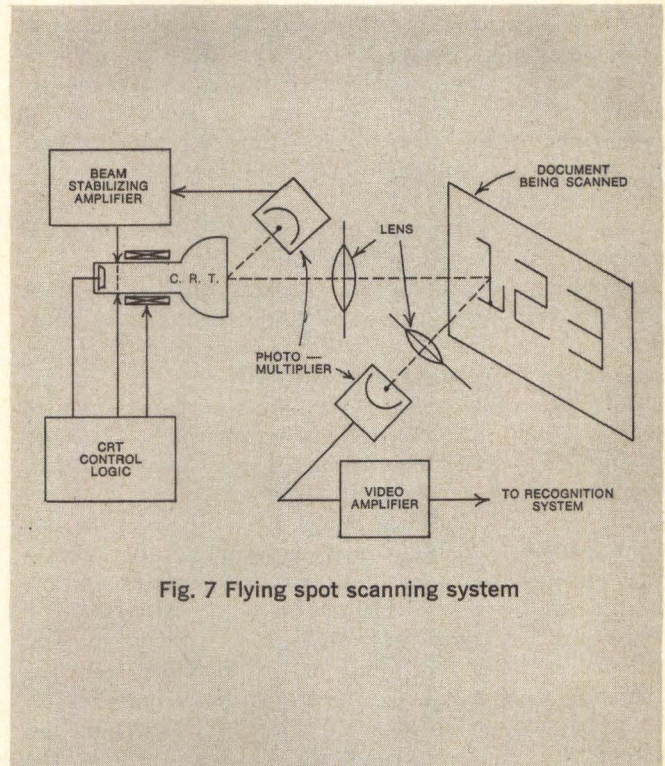


Fig. 7 Flying spot scanning system

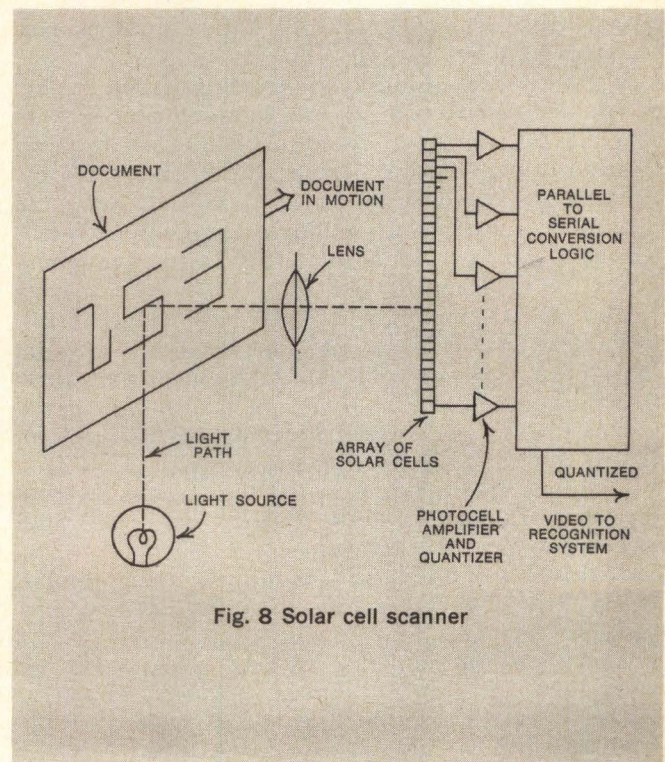


Fig. 8 Solar cell scanner

RECOGNITION SYSTEMS

There are many recognition schemes; therefore, it is only possible to review two of the more basic types in this article. The first is often called an area analysis recognition system—recognition is based on analyzing the whole area of the character rather than by features of the character. The block diagram is shown in Fig. 9.

The quantized video from the optical scanner is entered into a shift register of length equal to the number of vertical cells in the scanning array times the number of vertical scans taken through the character. A number of resistor matrices (one for each character) are connected to the shift register. The resistors are connected to those shift register flip-flops where, when the character is registered, a black or white cell is expected. Typically each character matrix consists of a hundred resistors, and the common point of each character matrix is connected to a current amplifier. As the character being scanned comes into registration with its matrix, the output voltage of the amplifier will rise, in this case positively. The most positive correlation voltage each character amplifier produces (occurring when the character bits coincide with resistor locations) is stored on the correlation voltage storage capacitor. The recognition circuitry then determines which capacitor has the highest voltage stored in order to decide which character is being read. For the recognition of that character to be validated, certain recognition requirements have to be satisfied, viz., the correlation voltage must have exceeded the minimum acceptable correlation voltage, and the difference between the character correlation voltage and all others must exceed a certain amount.

The second recognition approach is called stroke or feature analysis—during the scanning process, the character is classified by its features and their relative location to one another. To be readily analyzable by features, the type font has to be specifically designed for stroke analysis. Such a font is the US and International standard font for OCR, also commonly called the OCR-A font.

The OCR-A font was designed for maximum difference between characters for both area and feature recognition systems, while maintaining at the same time human readability. The font shown in Fig. 10 is therefore simple to read enabling the recognition system cost to be lowered considerably.

Analyzing the numerals in the font, it can be seen that each character can be defined by upper and lower vertical strokes located in five horizontal zones, and three horizontal strokes—upper, middle, and lower. The truth table for six of the characters is given in Fig. 11.

Analysis of the numerals truth table shows two or more stroke differences between any two characters, which accounts for the high reliability of recognition with this font.

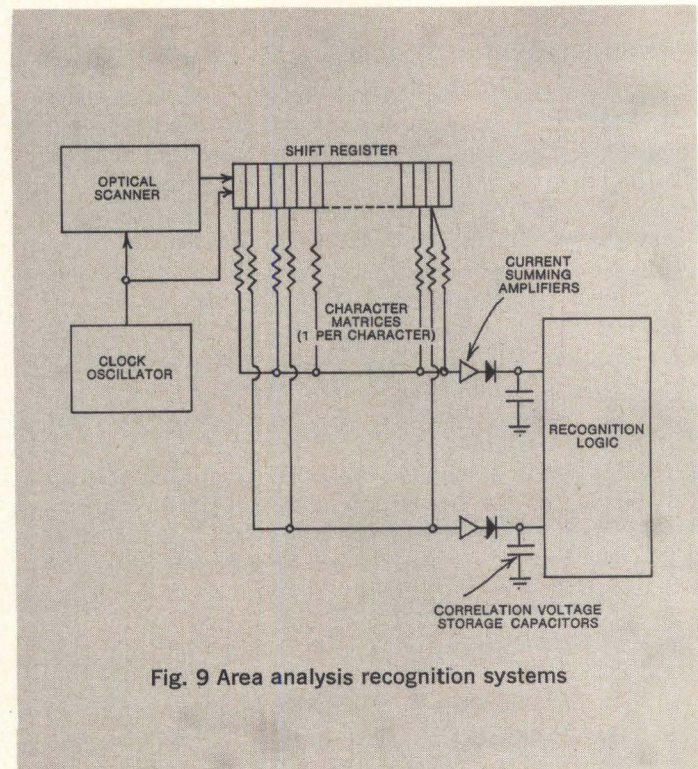


Fig. 9 Area analysis recognition systems



Fig. 10 USASI standard font for OCR

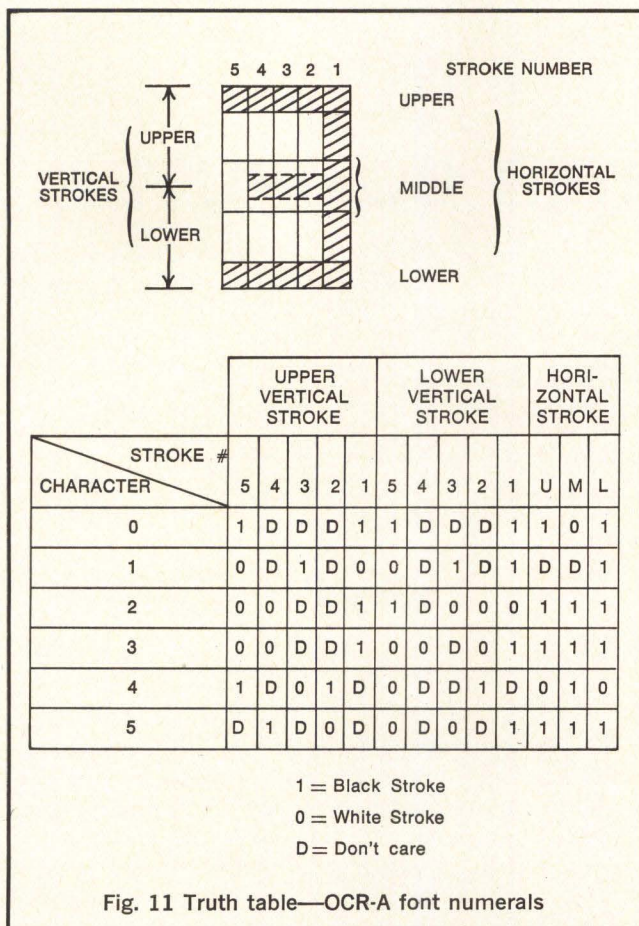


Fig. 11 Truth table—OCR-A font numerals

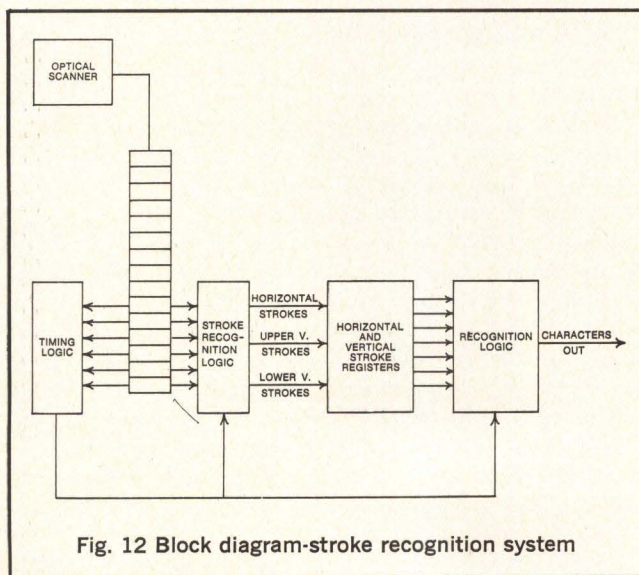


Fig. 12 Block diagram—stroke recognition system

The simplified block diagram for the stroke recognition system is shown in Fig. 12.

The output of the scanner (a serial pulse train representing the black and white cells of the character being read), is fed into the shift register which is capable of storing a complete vertical scan of black and white bits plus into another which is capable of storing one half vertical character stroke. Timing logic is connected to the shift registers to determine when to strobe for vertical strokes, and also to the stroke recognition logic which detects the strokes contained in the character and their relative position to one another. The stroke content of the character is stored in registers which are polled when the character has been completely scanned to determine which character was being read.

SUMMARY

This article has presented an overview of the large field of optical character recognition. By looking at a typical business problem, it has shown the necessity for OCR to become lower in cost to make it competitive with alternate systems. It has then reviewed the basic components that make up an OCR system: the document transport, the optical scanner and the recognition system.

Lower cost recognition systems are achievable through the use of stylized fonts such as the American Standard font that have been specially designed for OCR to maximize separation between characters.

The document transport shown in Fig. 5 is only one of a number of investigations Honeywell is conducting in the field of OCR among which include alphanumeric recognition capabilities, transport capability with greater size range and format flexibility and lastly, the most difficult problem of all, recognition of hand printed characters.

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This article discusses the use of a switchable voting element to effect a dynamic reconfiguration of a triple modular redundant computer organization upon occurrence of a logic failure.

SELF-REPAIR IN A TMR COMPUTER

**Michael Ball
Fred Hardie**

IBM Corp.
Owego, N.Y.

With the increase in complexity of digital computer systems, the training and experience required for efficient maintenance has already exceeded that of the skilled specialist. Even the computer designer, himself, experiences difficulty in analyzing the performance of a malfunctioning computer system. Self-repair has become a necessity. Self-repair, though, requires automatic error detection and self-diagnosis as a basic function of the computer.

The term "self-repair" has been used in the literature to mean anything from error masking to biological-style component regeneration. In this report self-repair means the automatic reconfiguration of the computer circuitry to bypass the failure either by a change of mode or by functional replacement of the failed part with a built-in spare.



Michael Ball received his BS in Physics from the University of Scranton in 1954. Upon joining IBM in 1954, he worked on determining the organizational requirements for an experimental full-value airborne/digital navigation-bombing computer system. Presently, he is an advisory engineer in the Integrated Test Systems and Interface Engineering department.



Fred H. Hardie received his BS and MS degrees in aeronautical engineering from New York University in 1944 and 1948. He joined the IBM Corp. in 1950 as a design engineer in the development of electromechanical computers. At present he is a senior engineer and manager of Integrated Test Systems and Interface Engineering.

The ever increasing reliability requirements of developing computer system applications has led to consideration of redundancy in computer organization. Of all the forms of redundancy being considered at present, triple modular redundancy shows, in the opinion of the authors, the most promise of "universal application." Like most redundant organizations, however, the very mechanisms which make a TMR organization failure tolerant also make it difficult to maintain.

TMR organizations operate on a two-out-of-three vote of input signals to produce proper output signals. If one of the input signals is "bad," its effects are cancelled by the votes of two "good" signals. The error is thereby masked by the voting process, and apparently more difficult to detect than it would be in a simplex-organized machine.

An approach to incorporating an automatic error detection and fault isolation capability into a TMR-organized computer system was investigated by the authors. In this approach, a switchable voting element is used to detect a difference between the three channel inputs to the voter and to identify the "bad" channel as well as to perform the basic voting function. Upon detection of a disagreement in input signals, the voter will initiate a switching action to reconfigure the machine organization to compensate for the failure.

TRIPLE MODULAR REDUNDANCY

TMR is a method of instrumenting a two-out-of-three voting function for electrical logic and control circuits. In the basic TMR configuration, the computer

is organized into three identical channels with each channel synchronized with the other two and all three channels performing simultaneous operations. A voting element placed at the outputs of the three channels compares the output signals and selects the signal on which at least two of the channels agree.

If a failure occurs in one channel, causing an error in its output, the failed channel will be "outvoted" by the other two channels and the effects of the failure are masked. Thus, a single failure in the computer will not cause an operational error, unless the failure occurs in the voting element. To prevent failures in the voting element from causing operational errors, the voting element itself can be triplicated, one element per channel.

For more effective voting, the channels can be subdivided into serial modules with voting elements placed at the outputs of each module. This is the organization of the specific computer examined by the authors and is shown in Fig. 1. A module failure, indicated by the dotted output lines, is shown in the figure.

The error resulting from a failure of Module 1/Channel 3 propagates only as far as Voter 1. Each section of the voter has a "good" input signal from Module 1/Channel 1 and Module 1/Channel 2 and the "bad" input from Module 1/Channel 3. The bad input is outvoted by two good inputs and the voter output to all three channels is good.

This error masking effect of majority voting is sometimes referred to as a self-repairing function. However, in this article, the term self-repair is used to identify the process in which the computer automatically detects an error in its operation, diagnoses the error to locate the fault, and then reorganizes its own configuration by means of some switching action to compensate for the failure. In this context, although the voting function makes the computer failure tolerant, the basic TMR organization is not self-repairing.

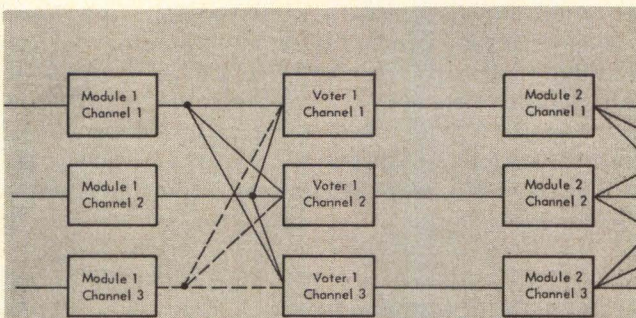


Fig. 1 TMR Organization.

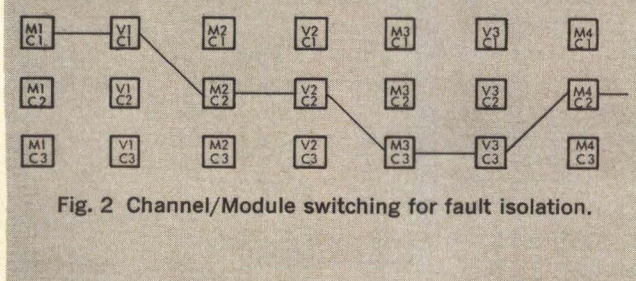


Fig. 2 Channel/Module switching for fault isolation.

SIMPLEX TEST MODES

At some point in time any accumulated failures in a TMR organization will have to be corrected. One method of detecting failures is to check each channel individually as a simplex computer. To reorganize the TMR computer into simplex channels, one of the following methods may be used:

- 1) Force the circuits of one channel to a "zero" logic state and the logic of a second channel to a "one" logic state. The "votes" of these two channels will then cancel and the third channel effectively operates as a simplex computer.
- 2) Turn off two channels and convert the voter to a simple circuit driver.

An alternate approach to computer checkout is to add error-detecting circuitry to the basic TMR organization.

Once an error is detected, the failure causing the error must be located if a repair is to be accomplished. The method of detecting errors by reorganizing the computer into a simplex configuration can be expanded to provide a fault isolation capability as well. In this approach the computer can construct an effective simplex channel by selecting a logic block from any channel and any module as shown in Fig. 2. Either of the above methods for forcing simplex operation may be used.

Assuming that seven modules are simply connected in a serial manner by voting elements, the following procedure can be used to construct a practical set of tests for error detection and fault isolation in a TMR configuration. The seven-module configuration represents an actual computer configuration examined by the authors.

In the assumed configuration, the TMR computer can be completely checked by a set of nine tests as indicated in Fig. 3. The numbers in the body of the table represent the channel selected in each module

Test	Module						
	1	2	3	4	5	6	7
1	1	2	3	2	1	2	3
2	1	3	1	3	1	3	1
3	2	1	2	3	2	1	2
4	2	3	2	1	2	3	2
5	3	2	1	2	3	2	1
6	3	1	3	1	3	1	3
7	1	1	1	1	1	1	1
8	2	2	2	2	2	2	2
9	3	3	3	3	3	3	3
10	1	1	1	1	1	1	2
11	1	1	1	1	1	1	3
12	1	1	1	1	1	2	1
41	2	3	3	3	3	3	3
42	1	3	3	3	3	3	3

Fig. 3 Test Set for error detection and fault isolation.

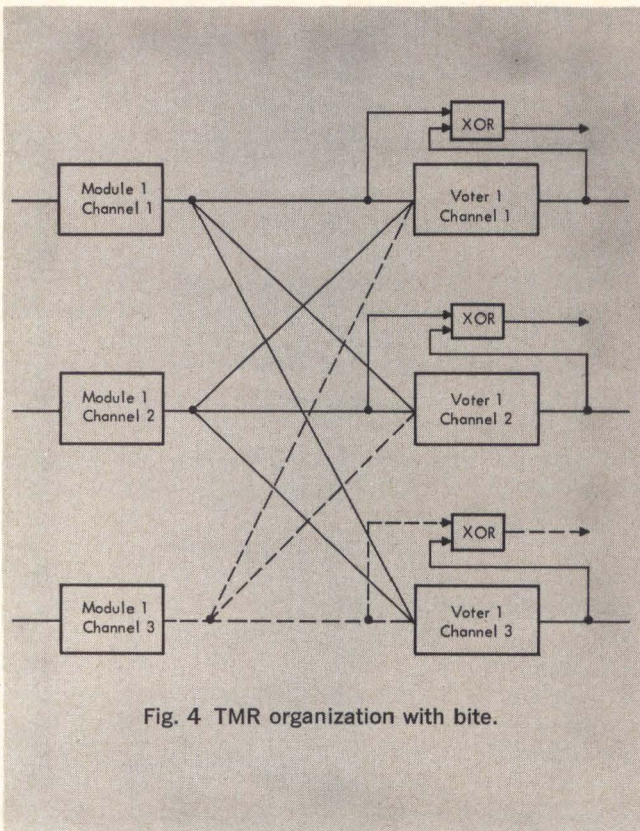


Fig. 4 TMR organization with bite.

by the test switching. Figure 2 shows the configuration for Test 1 of Fig. 3 for the first four modules.

The normal simplex channels are checked in Tests 7, 8, and 9. Since the cross-channel diodes which connect each logic block of the computer to the voting elements in the other two channels are not checked in the normal channel configuration, Tests 1 through 6 are required to complete the error detection check.

To provide the capability of isolating the source of a detected error in one of the 42 logic and voter blocks of the seven-module configuration, the set of required tests must be increased from 9 to 42, as indicated in Fig. 3. Tests 10 through 42, in effect, substitute alternate logic blocks for suspected logic blocks and rerun the simplex test with each substitution.

Even though the required tests have increased in number, the test time required to exercise all 42 tests will not exceed a few milliseconds. The number, 42 is, of course, an upper bound on the required number of tests since a fault will usually be isolated well before the 42 tests are exhausted. In the configuration described, the tests can be ordered in such a way that a large majority of probable failures can be isolated with only 12 tests.

Once the fault has been isolated to a logic block, corrective action must be taken. If built-in spares are available, the corrective action would be to replace the failed block by the spare through automatic switching. If built-in spares are not available, a partially corrective action would be to switch out the failed block plus one of the "good" blocks in the same module, effectively converting the module to

simplex operation while the remaining modules operate TMR. The effects of these corrective actions on computer reliability will be discussed in a later section.

ERROR DETECTING CIRCUITRY

The channel/module switching technique described in the previous section provides a maximal error detection capability with attainable fault isolation to a logic block level. The primary disadvantage of this technique is that it requires interruption of computer operation to perform the test. In real-time applications, periodic interruptions of even a few milliseconds duration may not be permissible. To provide error detecting and fault isolation capabilities to a TMR-organized computer system, special test circuitry must be added to the basic TMR configuration.

In providing its function of voting out the effects of a logic failure, majority voters mask the presence of these same failures. Additional circuits are needed in the TMR configuration to indicate the internal status of the redundant configuration. In the author's study, these additional circuits took the form of exclusive-ORs placed across each voter as shown in Fig. 4.

The exclusive-OR network will detect a logic difference between the primary input to the voter and output of the voter. For example, the logic block Module 1/Channel 3 is assumed failed, as indicated by the dashed output lines of the logic block. The exclusive-OR circuits will sense that the channel inputs and outputs of their respective voters in Channels 1 and 2 are logically identical and will produce no output signal. The exclusive-OR of Channel 3, however, will sense the difference between the incorrect (dotted) input signal to the Channel 3 voter and the corrected (solid) voter output.

The exclusive-OR network provides both error detection and fault isolation without interruption of system operation. In addition, the computer system may be made self-repairing by using the outputs of the exclusive-ORs to initiate a corrective action. Again the corrective action may consist of replacement of the failed logic block with a spare or automatic switching of the module containing the failed logic to simplex operation.

RELIABILITY CONSIDERATIONS

Expressions for the reliability of the basic TMR module and for the self-repairing versions can be derived by summing the possible failure states for each configuration. In the basic TMR configuration, if it is assumed that similar circuits always fail to the same logic level, then any module in the configuration cannot tolerate simultaneous failures in two channels. The operating states then consist of:

- 1) all three channels operating
- 2) channel 1 and 2 operating; channel 3 failed
- 3) channel 2 and 3 operating; channel 1 failed
- 4) channel 3 and 1 operating; channel 2 failed.

Summing the permissible states, the resulting expression for the reliability of the TMR module is

$$R_m = R^3 + 3(1 - R) R^2$$

where R is the reliability of the simplex logic blocks making up the triplex module. Collecting terms and assuming a constant failure rate (λ) for the individual logic blocks, this expression becomes

$$R_m = 3e^{-2\lambda t} - 2e^{-3\lambda t}$$

and is plotted as Curve 1 in Fig. 5.

If it is assumed that any circuit has equal probability of failing to either a zero or a one logic level, then the TMR module will, on the average, tolerate a simultaneous failure in two channels with a 0.5 probability of proper operation. The module reliability under this assumption becomes

$$\begin{aligned} R_m &= R^3 + 3(1-R)R^2 + \frac{3}{2}(1-R)^2R \\ &= \frac{3}{2}e^{-\lambda t} - \frac{1}{2}e^{-3\lambda t} \end{aligned}$$

and is plotted as Curve 2 in Fig. 5.

The reliability expression for the self-repairing case where the failed logic block is switched off along with a neighboring good block was derived in a rigorous manner, but can be induced by the following argument. As in the basic TMR case, the module can tolerate a failure in any one channel. When the failed logic block has been turned off, however, one of the remaining two logic blocks is also turned off. If, now, the second off logic block fails, the TMR module will still be operating since the good block is being used. Since there is a 0.5 probability that the second channel to fail in any module will be the one that is turned off, the expression for module reliability becomes

$$\begin{aligned} R_m &= R^3 + 3(1-R)R^2 + \frac{3}{2}(1-R)^2R \\ &= \frac{3}{2}e^{-\lambda t} - \frac{1}{2}e^{-3\lambda t} \end{aligned}$$

Since this expression is identical to the one above, it is seen that repair action of switching a module to simplex operation on detection of an error effectively forces compensating errors in different channels of the TMR module 50 % of the time. This case is also indicated by Curve 2 of Fig. 5.

The partitioning of a computer system into serial TMR modules provides a means for determining the internal status of the system during operation. In effect, it provides a means for detecting and compensating for logic failures before the resulting errors can be propagated to the output of the system. In combination with some additional buffering and some reasonableness tests on the system output, it would be possible to detect a failure in a TMR module that has already been switched to simplex mode. On detection of this failure in a second channel of a TMR module, the logic block of this

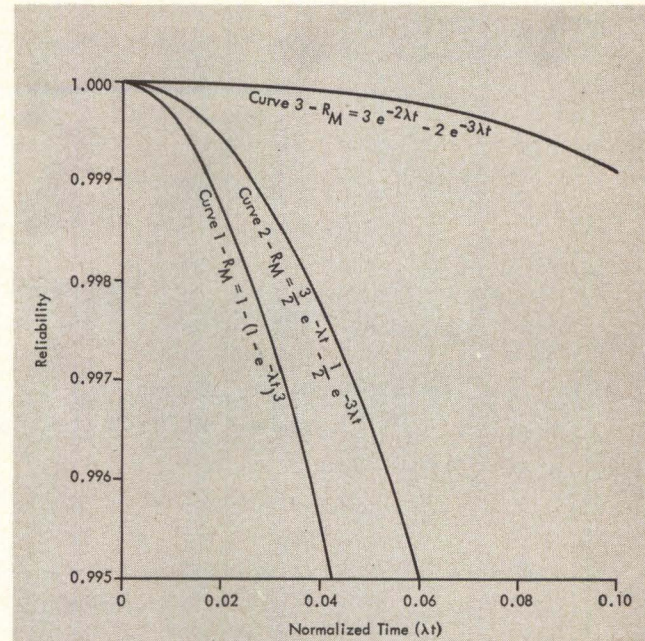


Fig. 5 Reliability of TMR versions.

channel could be switched off and replaced by the remaining good channel (the one that had been turned off with the logic block containing the first failure.)

Under these conditions the TMR module can tolerate any combination of channel failures except simultaneous failure of all three channels. The expression for the reliability of the TMR module becomes

$$\begin{aligned} R_m &= 1 - (1 - R)^3 \\ &= 1 - (1 - e^{-\lambda t})^3 \end{aligned}$$

and is plotted as Curve 3 in Fig. 5.

CONCLUSIONS

From the study which evolved the above results, the authors have concluded that self-repair in a TMR computer system is feasible and produces significant increase in system reliability over the basic TMR organization. The additional error detection, fault isolation, and automatic switching circuitry required to achieve the system reliability of Curve 3 in Fig. 5 cost less than twenty percent of the basic TMR circuitry.

The incremental reliability between Curves 2 and 3 of Fig. 5 reflects the reliability advantage of using up the available circuitry of a system during an extended mission. That is, rather than discarding a good logic block with every failed logic block, the good block is used as a spare.

The feasibility of extending the switching network to build in additional spares was considered in the study, but not examined in detail. It is the authors' opinion that such an organization will prove to be more desirable for extended missions such as manned and unmanned deep space probes than other approaches now being considered, including higher order and adaptive voting techniques.

HTI: AN ORDER TO IMPROVE MULTIPROCESSOR PERFORMANCE

Bernard Peters
National Security Agency

With the implementation of large scale multiprocessing configurations, it is necessary to devise hardware techniques to make it possible for the individual multiprocessors to optimize their utilization of the memory. Multiprocessing, as used here, is defined as several arithmetic units operating simultaneously using common memory. In a multiprocessing system the scarcest resource is assumed to be the memory accesses on the fast core. The pacing demand is against the fast core; I/O devices deliver their words to the core or get them from the core. The program order stream is read up from the core. The data or operand stream used by the program functions using the core.

Because of the use of core for these purposes by all of the processors, there is a certain amount of conflict. This conflict is resolved by race condition gates which select appropriate processors to receive the next available memory cycle.

Multiprocessing is a variant of multiprogramming. Multiprogramming depends upon the statistical utilization of the I/O channels to gain maximum employment of the central processor. The interrupt system is utilized by the executive to allocate the available machine time to the individual programs. These programs, for ease of programming, are written independent of consideration with whom they

may be run. Because of this characteristic it is not uncommon for a load of programs in a multiprogramming system to have all entered into a blocking state waiting for completion of I/O. It is not possible to program each processor so well that there is never unused time.

When one of the processors in this multiprogramming environment has entered a blocked state for all programs there is nothing for it to do. It is commonly programmed so that the executive searches all of the available flags and continues to entertain itself in what is described as the idle loop. While there must be in any proper multiprogram executive a lowest category of activities to be accomplished, these are not to be considered as part of the idle loop. However, even low priority tasks eventually are accomplished and there is literally no work to be done. This then requires the processor to use orders going around the idle loop.

It is to prevent this idle loop utilization performance of orders merely to keep the machine conscious that represents a loss on the memory to other processors of the multiprocessor configuration. The orders for the order stream which make up the idle loop cannot be obtained from the central processor free of charge. Every order of the idle loop which is read up from

memory uses a memory access. Because of this, it becomes desirable to install an order in each of the processors of a multiprocessor to permit it to eliminate the obligation to use this time.

This order could be named Halt Till Interrupt (HTI). The HTI instruction resembles an ordinary halt instruction which will put the machine into a run state upon the next interrupt. The order to be chosen after the HTI instruction is, of course, one dictated by the interrupt sequence. When it completes its action, control returns to the location directly after the HTI.

When the processor is halted for the HTI instruction, the processor must be free to cycle for input/output requests on the buffer channels. Automatic update of real-time clocks must continue. The cycle stealer must successfully steal cycles even though there is no order chain going. This permits the multiprocessor to have ongoing I/O activity. It can afford to stop for periods as small as a few microseconds. It is this collection of many periods of a few microseconds which represents the real savings in this system. The HTI instruction would not be effective for very long periods where the processor is unused because the operator was inattentive. These represent real losses in any case and although they may be administratively or economically exciting, from a systems design point of

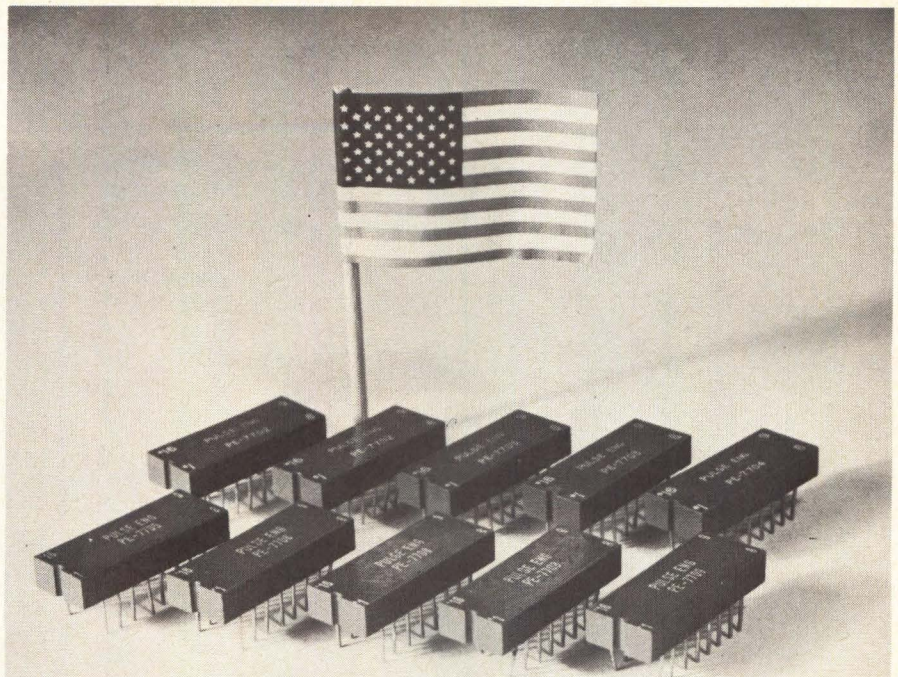
view, they are not amenable to amelioration.

Does the HTI instruction as proposed have any pertinence for a nonmultiprocessor or for a stand-alone computer? Many multiprocessors are designed to be both uniprocessors and multiprocessors. If possible, this order should be in the general class of equipment rather than the special multiprocessor capability.

The HTI instruction would be useful in a multiprogrammed unit processor. The unit processor does not know which of the tasks are engaged in I/O without extensive bookkeeping. Such bookkeeping would cost far more than it is worth. Therefore, when the multiprogrammer executive in a unit processor hits the idle loop, it would be desirable to stop utilizing memory accesses. The I/O mechanism buffer channels potentially need all the memory accesses which are available. Because of this, the multiprogrammer executive could afford to halt with the HTI instruction.

Could a multiprogrammer executive in a unit lose consciousness because of the HTI instruction? Probably not. For there would be real time clocks running which would be guaranteed to bring back the machine on an interrupt even if the multiprogrammed unit processor should go into an HTI instruction with no ongoing I/O activity. Thus the HTI instruction could be performed at any time there was a true idle condition present.

Is it necessary to reserve HTI for the executive system? Is it particularly harmful if a worker program executes the HTI instruction? It would seem that there could be no harm in the HTI instruction being executed by a worker. It does not interfere with the I/O of any program or the executive. Control reverts to the executive at the first opportunity. It would seem that the worker program is wasting its own time quantum. It is a suboptimal process to do this, but it does not look as though the HTI instruction would have to fall within the privileged set of executive instructions as is found in most multiprogrammed machines.



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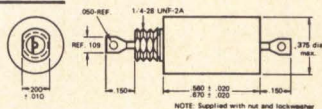
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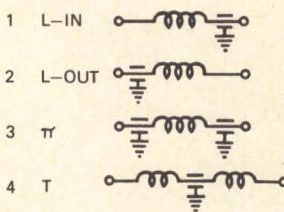
Ordering information

CF	4	A	PO6	- 1	G
TYPE	CIRCUIT	VOLTAGE	CURRENT	MOUNTING STYLE	TERMINAL STYLE

Voltage

A	50 VDC
B	100 VDC
C	200 VDC (115 VAC)

Circuit



Mounting Style

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2	.312	2 FLATS
3	.190	NO FLATS
4	.190	2 FLATS

Terminal Style

G	90° LUG
L	LEADS

Current in Amperes

PO6	.06 Amps.
P15	.15 Amps.
P25	.25 Amps.
P50	.50 Amps.
1PO	1.0 Amps.
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There does not seem to be any examples of the HTI instruction as specifically defined by the above paragraphs on any current equipment. However, there are some primitive forms of this instruction.

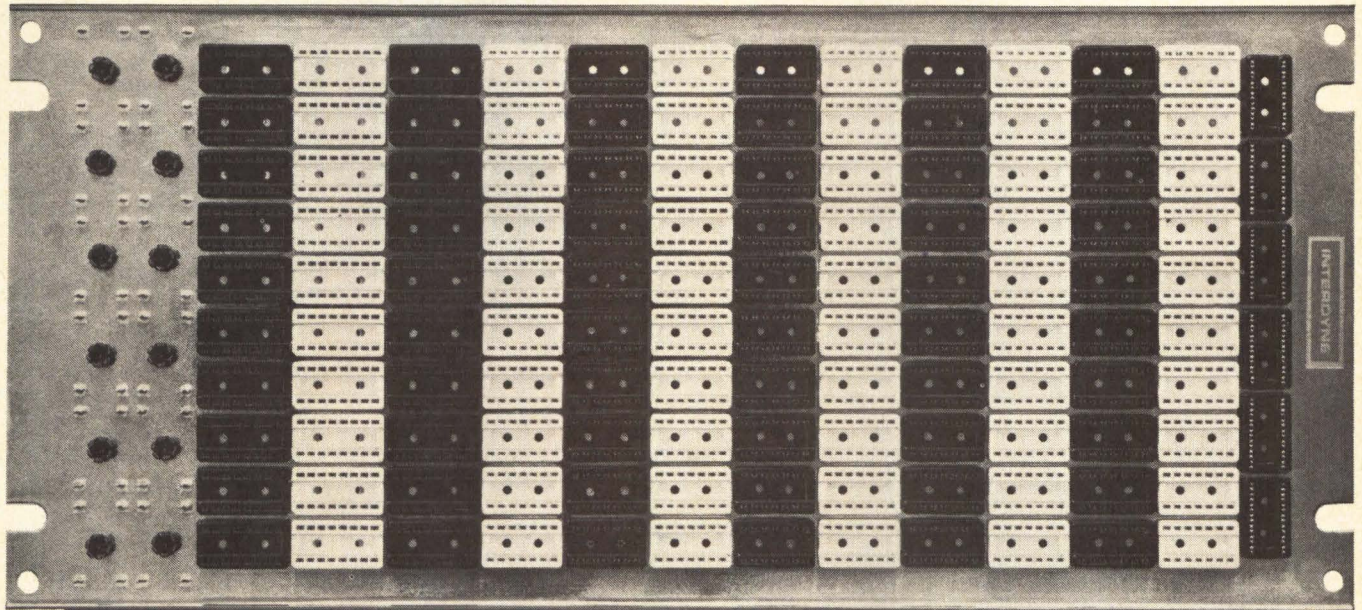
In the IBM/360 series there is a state word bit configuration which causes the machine to go into a pause until interrupt status. The modification of the state word is therefore a serious activity and this has an effect upon the utilization of the various registers of the equipment. It would be desirable to have the HTI instruction modify the state word solely for the purpose of going into a Halt Till Interrupt.

On large UNIVAC equipment there is no device similar to an HTI instruction although it is possible to construct an HTI instruction by doing a very long repeat of a no effective order. For instance, an Enter Index Register Zero or Add Zero to A under a very long repeat would have the advantage of freeing the machine of memory cycle demands while not disabling the consciousness of the equipment. But this is not a recommended practice because of the inclination of the interrupt routine to continue a repeat. Every repeat becomes a pure waste of time and the effect of freeing the machine cycles is counterbalanced by the wasted time while the repeat is run out. From a software point of view it would not be desirable to have to check the address on an interrupt to determine that an interrupt had occurred in the idle loop and could be aborted. There is the further disadvantage that the repeat register has to be modified by the idle routine.

It would seem that the capability for a HTI instruction is virtually existent in most current equipments and would require only the addition of a few gates to make it available to other equipments, assuming there is a logical position available in the expression of available orders.

It is therefore recommended that all computers which promise multiprogramming or multiprocessing and include real time clocks should also include the HTI instruction as described above.

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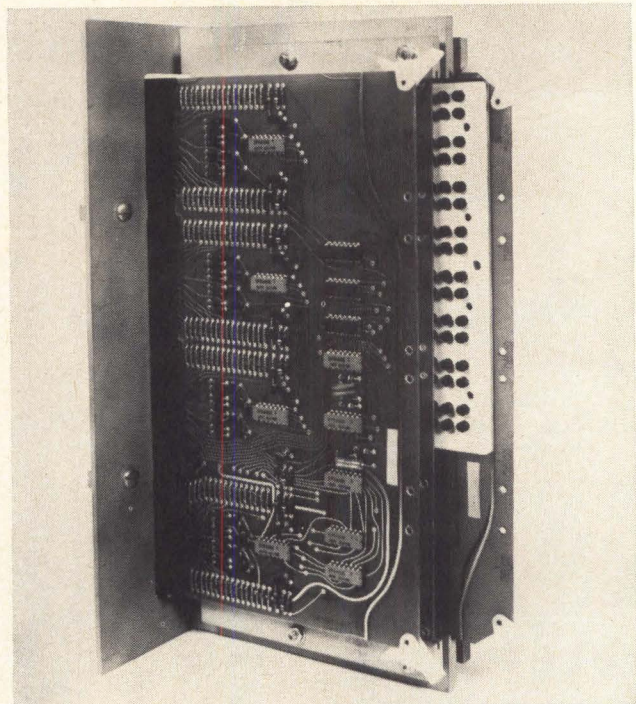
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The random access memory, developed by Memory Technology, Inc., Waltham, Mass., features a full cycle time of $1.2\mu\text{s}$ and an access time of 700 ns, and offers a memory capacity of up to 1024 words of 12 bits per word. It is packaged on four printed circuit boards which occupy a total volume of $10.5'' \times 6.0'' \times 2.0''$. All interboard connections are via card-edge connectors, thus allowing system disassembly by unplugging printed circuit boards.

The memory is DTL and TTL compatible and has the following approximate logic level ratings.

Standard fan-in is defined as:
Logical "0" (false) 0 to 1.0 Vdc at 1.6 mA source
Logical "1" (true) +2 to 5.0 Vdc at 40 μA sink.

Standard fan-out is defined as:
Logical "0" (false) 0 to +0.4 Vdc at 1.6 mA sink

Logical "1" (true) +2.5 to 5.0 Vdc at 40 μA source.

Other features include up to 10 address lines, up to 12 data outputs, an operating temperature range of 0 to 50° C, and a storage temperature range of -55° C to +125° C.

The heart of Memory Technology's ROM is a braid transformer matrix, consisting of a series of linear-ferrite U-shaped cores—each with its own winding—and a bundle of word wires. The wire braids are woven on a specially designed loom, assembled into the cores, and incorporated into modules. Basically, the memory contains one wire for each word to be stored and one core for each bit of the output word. The linear magnetic material of the core does not switch; the core acts like a transformer. Information is stored by the relative position of each word wire with respect to each core, making the memory electrically alterable or read only.

If a particular word wire passes through a particular core, a 1 is stored in the bit position represented by the core. When the wire is threaded around the core, a 0 is stored.

The pluggable-braid ROM is designed for microprogram control, character generation, stored tables, and program storage applications.

The use of a braid transformer matrix memory for a computer's control unit permits maximum flexibility of design at minimum cost. The control program may be tailored to fit the particular use to which the computer is put without costly redesign usually incurred when hard wired logic is utilized.

In a character generation system, the ROM is used to store and generate the binary description of each character being displayed.

Here the braid ROM exhibits the ability to change the character set without changing any electronics. By replacing the assembly of wire storing the binary pattern (the braid), any character set can be written with a given set of electronics. Further, individual characters may be quickly changed or added in the field.

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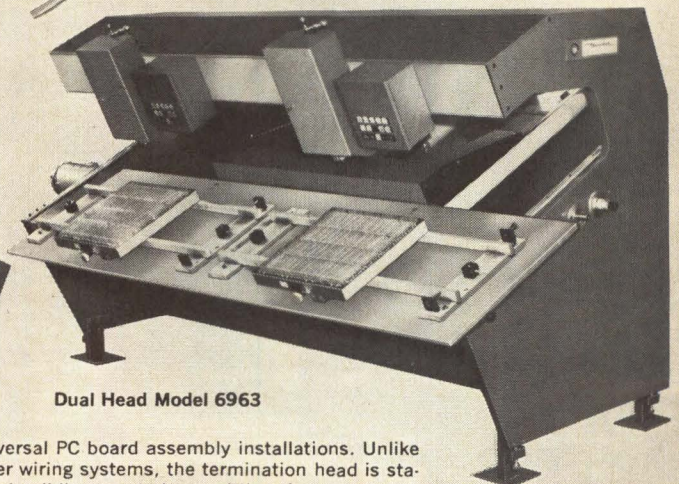
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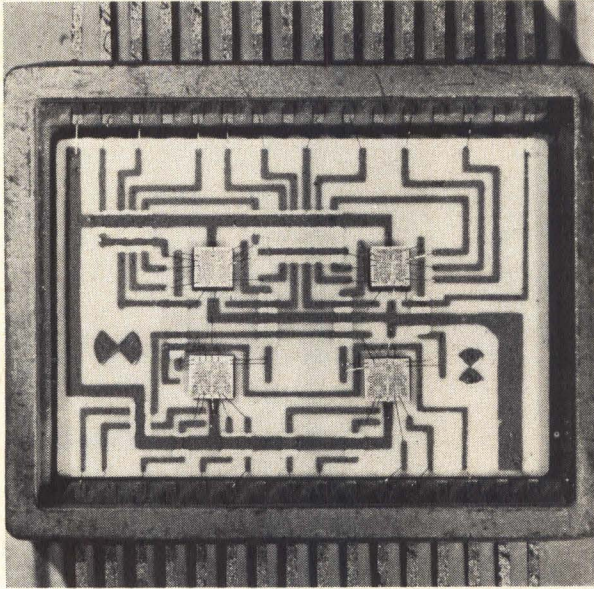
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FOUR-BIT ARITHMETIC CIRCUIT

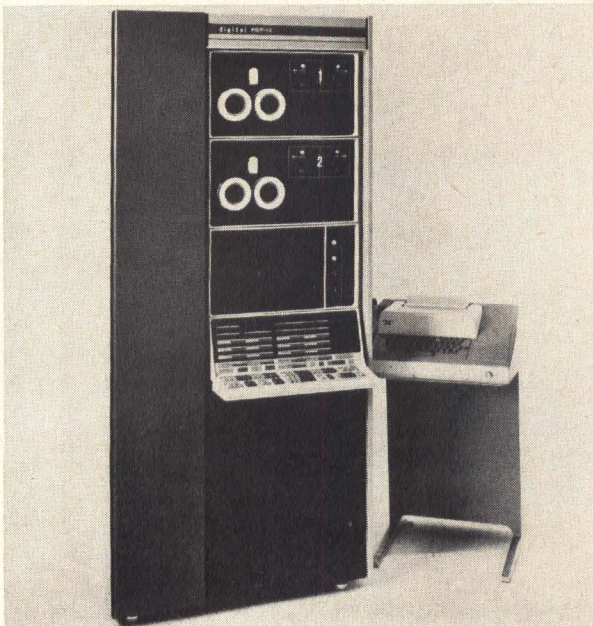
The SH8080 combines a ripple carry adder and a holding register to form a 4-bit arithmetic unit that incorporates four MSI chips. Two TT μ L 9020's and two TT μ L 9304's are interconnected by a multi-layer thick film substrate that provides high reliability not possible with customary wiring connections. The 9020, a dual JK \bar{K} flip-flop, and the 9304, a dual full adder, have been in widespread use for more than a year.

Compatible with current sinking logic, the SH8080 performs with a carry propagation time of 32 ns typically. The noise margin is 1 volt.

Chief applications for the circuit are in airborne computers, desk-top calculators, and high-speed data processing and ground support equipment.

The 4-bit arithmetic unit is available in a hermetically sealed, 32-lead flatpack. Industrial temperature range extends from 0° C to +70° C; military temperature range from -55° C to +125° C. Fairchild Semiconductor, Mt. View, Calif.

Circle No. 201 on Inquiry Card.



PDP-12 COMPUTER SYSTEM

A new computer system, the PDP-12, replaces the LINC-8 computer for laboratory applications. The PDP-12 in its laboratory instrument computer (LINC) configuration, includes a central processor with a 4,096-word memory expandable to 32,768 words, two magnetic tape storage units, a 7" x 9" CRT display, a 16-channel A/D converter and multiplexer, a data terminal, a teletypewriter and paper tape reader and punch.

Ease of operation is brought about by the system's console or control panel and the set of 43 basic instructions that are inherent to the system. A pushbutton on the panel loads the machine programs, controls the operation of the magnetic tape units and starts the system.

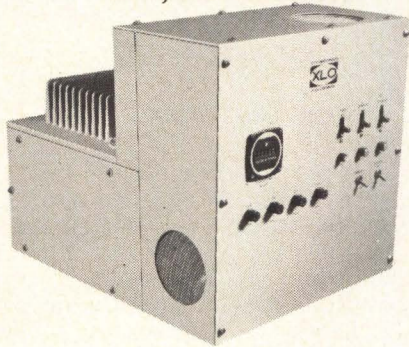
Other features of the system which add to simplicity include the ability to enter data manually through sense switches and the ability of the display to question the user as he operates the system. Several of the peripherals are built into the system, are fully buffered, and can be operated independent of the central processor.

The display shows the last 32 lines of any program being developed. To make a correction, it is only necessary to point the cursor at the error. Program file manipulation is held to a minimum; these programs appear as sub-routines to the master operating program. While assembly, editing and monitoring programs are separate in the system, they appear as one, using common commands. Digital Equipment Corp., Maynard, Mass.

Circle No. 200 on Inquiry Card.

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No kidding.
The new low-priced Bryant
CPhD packs 192 data tracks
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Write, and Select Elec-



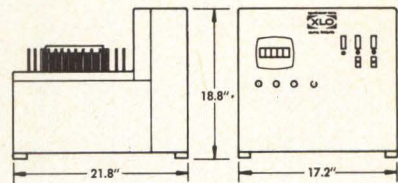
tronics. At an average
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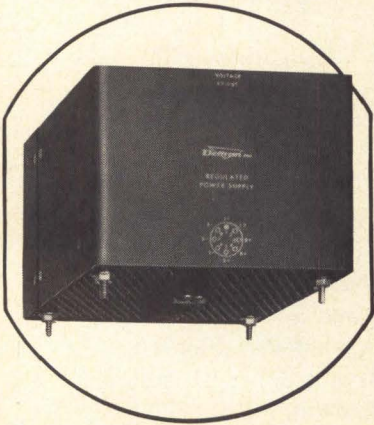
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CIRCLE NO 34 ON INQUIRY CARD

NEW PRODUCTS

PORTABLE TELETYPEWRITER

The DATANET 730 comes as a keyboard manual send/receive unit, or as an automatic send/receive unit/equipped with a punched paper tape option for transmission of messages.

The complete terminal comprises the portable teletypewriter; an acoustic coupler which serves the telephone handset; and a conventional telephone for immediate access to a time-sharing computer. It employs a standard Model 33 teletypewriter character set and keyboard layout.

Communication is initiated by plugging the DATANET 730 into any 115-volt ac outlet. The computer is then dialed by telephone. Then the receiver is cradled in the acoustic coupler, and tone signals feed data back through the teletypewriter at 100 words a minute. General Electric Co., Phoenix, Ariz.

Circle No. 208 on Inquiry Card.



MAG TAPE SYSTEM

The CartriFile, a single unit combining four cartridge-loaded magnetic tape files, can be used to sort, match, collate, and merge data. The tapes also provide program loading, off-line storage for memory dumps, and buffering for uninterrupted data accumulation.

The system is plug-compatible with PDP-8, PDP-8/S, PDP-8/I and PDP-8/L computers. Ten microinstructions are used for status checks and tape-action control, including simultaneous reading and writing. On-the-fly error detection and correction assure superior data reliability and replace program-controlled reread techniques. Data transfer rate is 462 12-bit words per second in variable-length records. Storage capacity is 320,000 words. Tri-Data, Mountain View, Calif.

Circle No. 226 on Inquiry Card.

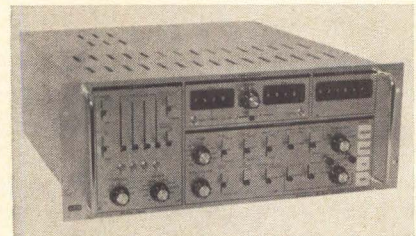
CHOPPER TRANSISTORS

PNP epitaxial base chopper transistors, 2N2944, 2N2945, 2N2946, feature breakdown voltage ranges up to 60 V, offset voltage as low as 200 μ V and typical h_{FE} of 50 to 250. Typical $r_{ec(on)}$ is 6 ohms.

The 2N2944-5-6 series of low level choppers are packaged in the TO-46 case. They may be ordered singularly or as matched pairs.

Typical applications include modulators, servos, telemetry systems and multiplexing. They are ideal in dc amplifier applications. Solitron Devices, Inc., Riviera Beach Fla.

Circle No. 252 on Inquiry Card.



DIGITAL PROCESSORS

Available in three models with 4096 channel memory; 1024 and 2048 channel memories. Used with Geoscience or any standard ADC models to collect and record high resolution data in nuclear research. Standard features include tag word generators, 3.5 μ sec memory, preset count and sweep, digital display expansion, selective readout, and modular input/output. Geoscience Nuclear, Div. of Geoscience Instruments Corp.; Hamden, Conn.

Circle No. 231 on Inquiry Card.

DRUM MEMORY SYSTEM

A compact, low-cost, ten-inch rotating drum memory system called the CLC-1, can store up to 1.2 million bits of data and has an average access time of 8.5 ms. The CLC-1 features four multiple pole-piece head assemblies, each containing eight write/read heads on 32 data tracks, operating at 3600 rpms.

The drum unit comes complete with a digital interface that makes it an ideal storage media for small accounting machines, general purpose business machines, and small and medium size computers. Bryant Computer Products, Walled Lake, Mich.

Circle No. 253 on Inquiry Card.

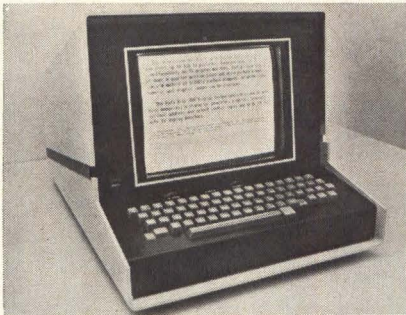
DIGITAL PRINTER

A high speed digital printer capable of printing 40 lines per second with a 16 column capacity, known as the Datalog MC 2400, is expected to be used in both military and commercial applications.

The design of the MC 2400 is such that it eliminates all belts, pulleys, clutches and ribbon motors. The print drum, attached to the shaft of a ball bearing motor, is the only continuously rotating part.

The unit is modular in design and is available with either a 12 or 15 character set. Datalog Div. Litton Industries, San Francisco Calif.

Circle No. 251 on Inquiry Card.



COMPUTER DISPLAY SYSTEM

A computer-driven television display system (TDS) incorporates multiple desk-top video terminals and has the capacity of storing and simultaneously displaying up to 128 different TV pictures. The terminals, which consist of monitors and keyboards, can be used for computer data entry and retrieval as well as for data display.

The TDS can be used for alphanumeric and/or graphic displays. Basically, the system consists of a disc memory, a time-shared control unit containing addressing logic and a character generator, a control terminal, and the display terminals.

Each TDS picture consists of over 1/4 million dark and bright picture elements (a 512 x 480 picture-element matrix) on which alphanumeric and graphic images can be written.

When writing on one channel, other displays are not disturbed. In writing alphanumeric images, individual characters can be changed. Similarly, when the display is used for graphics, single data bits can be altered. The displays may be written with dark images on a light background or with light images on a dark background. Data Disc, Inc., Palo Alto, Calif.


Circle No. 230 on Inquiry Card.

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Look into the numerical control systems of leading manufacturers and you'll find Remex reader/spoolers. For the same reason you'll find them in automatic test equipment and computer systems. Remex gives you predictable reliability. It isn't uncommon to run 200 million characters without a

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CIRCLE NO. 35 ON INQUIRY CARD

XL PVC IS TOUGHER BUT COSTS LESS



Irradiated crosslinked PVC-insulated wire with many of the advantages of TFE at half the cost is now being made into round conductor flat ribbon cable by Spectra-Strip.

Like TFE, crosslinked PVC won't melt, smoke or shrinkback if hit by a hot soldering iron. It's more solvent-resistant than ordinary PVC and several times tougher than TFE against cutting, crushing and abrasion.

Form stability and stable dielectric properties at higher temperatures and overloads may be XL PVC's most important benefits. Using this insulation, Spectra-Strip's unique bonded flat ribbon cable, harnesses and cable assemblies are rated at 115° for continuous operation, intermittent service at 150°C and momentary temperatures up to 350°C.

XL PVC meets all requirements of MIL-W-16878D, Types B, C and D and carries U.L. approval.

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CIRCLE NO. 36 ON INQUIRY CARD

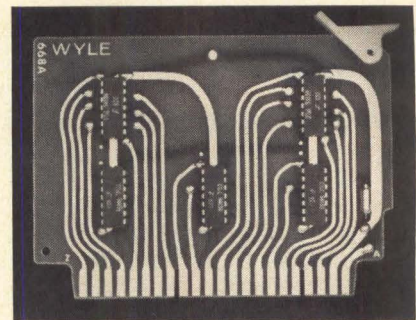
NEW PRODUCTS

MAG TAPE DEGAUSS OPTION

A magnetic tape degauss option with the purchase of a Mark II tape cleaner features a high level erase which removes magnetic flux (data and extraneous noise) from computer tape. Microswitch control sets the degauss feature for each reel of tape and automatically resets at the end of the cleaning and degaussing cycle.

This automatic feature enables an operator to degauss specific reels during cleaning while not affecting the magnetic information on others. The degauss option is designed for continuous operations with no possibility of excessive heating. As with previous models of the Mark II, complete safety to tape is guaranteed during cleaning. Data Devices, Inc., Culver City, Calif.

Circle No. 239 on Inquiry Card.



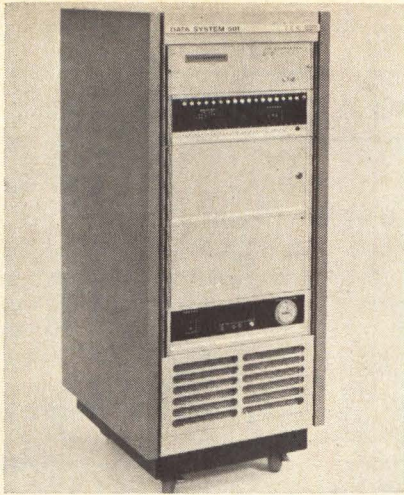
RS FLIP-FLOP

A ten set-reset, or storage capability is provided in the MSF-10, RS flip-flop IC logic module.

Using a basic circuit composed of cross-coupled NAND gates, the MSF-10 card has ten independent RS flip-flops, each with a single set and reset input, with all inputs and outputs brought out at the connector. The flip-flops are implemented by cross-coupled DTL 946 integrated circuit NAND gates.

The card provides for frequency, dc to 5 mc, and input loading of one unit load each input. Noise rejection is 750 mV, typical, at logic 0, and 1 V, typical, at logic 1, with input/output levels of +4 or -1 V at logic 1, and +0.2 plus or -0.2 V at logic 0. Output drive capability is 7 unit loads, and power requirements are +5 or -0.5 V at 75 mA, max. Systems Div., Wyle Laboratories, El Segundo, Calif.

Circle No. 222 on Inquiry Card.



DATA ACQUISITION TERMINAL

System 550 remote terminal monitors low level analog signals at remote facilities, with real time digital data transmission to a central computer or control station. Low level differential inputs from ± 5 to ± 500 mV are accepted with gain ranging accomplished in one of three modes: manual, programmed, or automatic. Up to 1000 low level analog signals are scanned at rates up to 50,000 samples per second while the remote terminal digitizes the data to 12 bit binary resolution and transmits it in PCM format over standard coax to a central processor located up to three miles away. The system includes a low-level multiplexer, A/D converter, PCM formater, and a line driver and line receiver Interstate Electronics Corp., Anaheim, Calif.

Circle No. 215 on Inquiry Card.

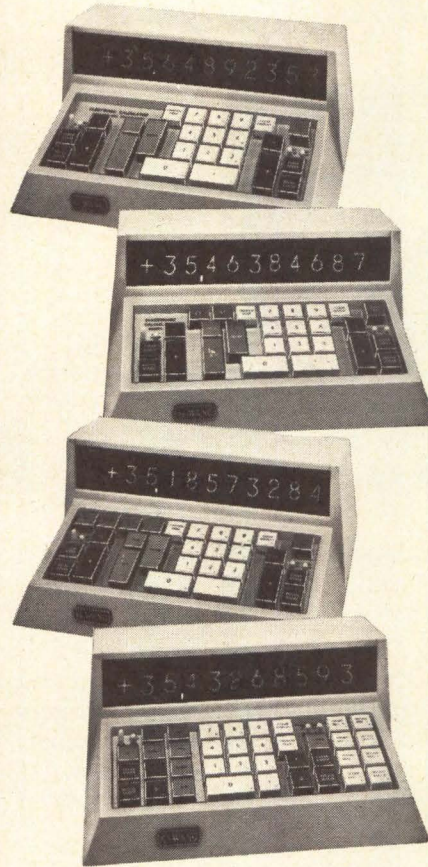
ULTRAMINIATURE COAX CABLE

A fully-shielded, flexible coaxial cable, only 0.01-inch in diameter, can function as either a compact coaxial or fully shielded line. Called miniplax coaxial cable, Type 7-50, the cable consists of a continuous outer sheath of copper, 0.001 inch thick, electro-deposited on FEP Teflon dielectric, 0.0084 inch OD, over a gold plated inner conductor of AWG #42 high-strength copper wire. The 125 micro-inch gold film assures maximum conductivity and oxidation resistance at the terminations.

It has a characteristic impedance of 50 ohms, and a capacitance of 29 picofarads/foot, a weight of 0.02 pounds/100 feet, and a minimum bend radius of $\frac{1}{8}$ inch. United Carr, Inc., Newton Highlands, Mass.

Circle No. 244 on Inquiry Card.

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Business Calculator

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Statistical Calculator

All the features and functions of the Model 300 plus \sqrt{x} and x^2 by single keystroke for $\sum x$, $\sum x^2$, $\sum y$, $\sum y^2$, $\sum (x+y)$, $\sum x \cdot y$, $\sum \sqrt{x}$, and $\sum \frac{1}{x}$

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Model 320

General Purpose Calculator

All the features and functions of the Model 310 plus Log_x and e^x by single keystroke for more advanced statistical, scientific and engineering calculations.

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All the features and functions of the Model 320 plus four extra data storage registers for complex calculations without re-entry of intermediate results.

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At the TI Industrial Products Group in Houston, we're building a new generation of optimized real-time data-acquisition and readout systems that communicate with workers and managers alike. We're also designing and building from scratch sophisticated central-station systems like our TIAC-870 shown below. It employs IC circuitry and logic techniques equal to anything in EDP today... anything!

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TEXAS INSTRUMENTS INCORPORATED



CIRCLE NO. 900 ON INQUIRY CARD

NEW PRODUCTS

LUMPED CONSTANT DELAY LINE

A 1000 ns. delay line designed for printed circuit board installation with taps available each 10 ns is 1.90 in. wide by 5.10 in. long by .30 in. high.

The series, at 200-ohm impedance, is designed with cut-off frequency at 65 MHz and displays low attenuation and minimum distortion. Operating temperature range is -55°C to $+125^{\circ}\text{C}$. The component is terminated with gold-plated pins and is encapsulated with epoxy in a diallyl phthalate housing. It incorporates stand-off feet to permit flush cleaning of solder flux residues after the soldering operation. Engineered Components Co., Gardena, Calif.

Circle No. 245 on Inquiry Card.



HIGH VOLTAGE POWER SUPPLY

CPS-1000 Series is available in two output voltage ranges: 10 to 20 kV, and 20 to 30 kV (exact voltage specified by the customer), with regulation to .001% for line or load variations, and a low drift of less than .005%/hr.

All high voltage circuitry is completely encased in three interlocking epoxy modules.

Other specifications include: Output, 10-20 kVdc @ 0-250 μA , 20-30 kVdc @ 0-100 μA ; Output voltage programming, fixed (with 5% vernier adjustment); Output polarity, positive or negative; Regulation, line or load, .001%; Drift, < .005%/hr; .01%/24 hr.; Resetability, .01% (after 30 min. warm-up); Temperature coefficient, .000025/ $^{\circ}\text{C}$ (ambient) after 30 min. warm-up. The unit measures $4\frac{1}{2} \times 4\frac{5}{8} \times 9$ inches, and weighs less than 14 pounds. Computer Power Systems, Inc., Sunnyvale, Calif.

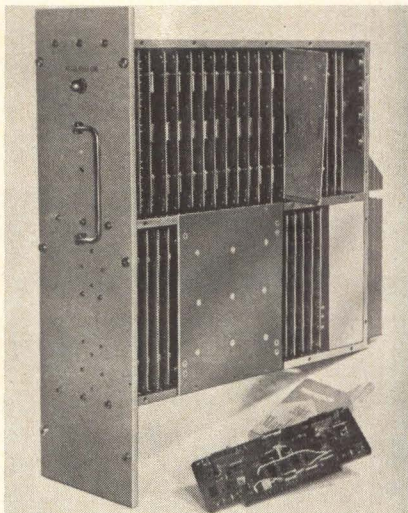
Circle No. 206 on Inquiry Card.

TAPPED DELAY LINES

A series of miniature, tapped delay lines constructed to be compatible with standard dual-in-line microcircuit packaging, D1511 Series, are .39" x .7" x .21".

The D1511 Series is offered with total delays of 100, 80, 60, 40, 20, and 10 ns. Each line has 10 tap delay points spaced at 1/10th of the total delay with delay accuracies of $\pm 5\%$. Output rise time is less than 30% of the total delay and distortion is held to less than 5%. Impedance for all units is 100 ohms $\pm 5\%$. Computer Devices Corp., Commack, N. Y.

Circle No. 247 on Inquiry Card.



RUGGEDIZED IC MEMORY

Model CR-95 is available in capacities of 4096 and 8192 words with word lengths variable in 4 bit increments from 8 to 36 bits. Full cycle time is 1 μ s with access time less than 500 ns.

Modular in design, the CR-95 employs field proven, highly reliable circuits used in the CE-100 repackaged onto smaller ruggedized logic boards. All circuits have been subjected to verifiable worst-case design analysis. Silicon semiconductors and high reliability components are used throughout.

Designed for application as a memory or buffer in small computers or data systems, the CR-95 meets the applicable requirements of MIL-E-16400 and similar specifications for mobile and shipboard equipment. Lockheed Electronics Co., Data Products Div., Los Angeles, Calif.

Circle No. 225 on Inquiry Card.



Have you noticed which disc memories your competitors use now?

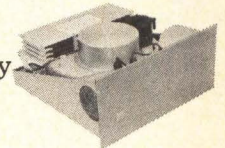
Five computer manufacturers and six data systems builders have adopted Data Disc memories as a standard rapid-access peripheral storage.

They've discovered that Data Disc memories cost about 35% less than any other head-per-track disc memory of equal storage capacity.

Perhaps you wonder how a top-quality machine can cost so little. Well, cost per disc, per track, per head or per drive is no less than any other reliable memory. But cost per bit stored is far less—simply because our “in-contact” recording technique stores twice as many bits per inch as older “floating head” techniques.

“In-contact” recording—in which heads ride in gentle contact with a highly polished disc—is five years old now. It has proven its long-

term reliability in hundreds of Data Disc memories now operating across the nation. We guarantee an error rate less than 1 part in 10^{10} , and tests by our customers show typical error rates 1000 times better.



An F-Series head-per-track system

Our F-Series head-per-track system comes with storage capacities of 0.8, 1.6, 3.2 and 6.4 million bits. It has an average access time of 16.7 ms, and stores 100,000 bits on each track—enough to fill the core memory of a small computer. And the whole system fits in $8\frac{3}{4}$ " of rack space.

For complete information contact Data Disc, Inc., 1275 California Avenue, Palo Alto, California 94304, Phone (415) 326-7602.



DATA DISC

CIRCLE NO. 38 ON INQUIRY CARD

Economy

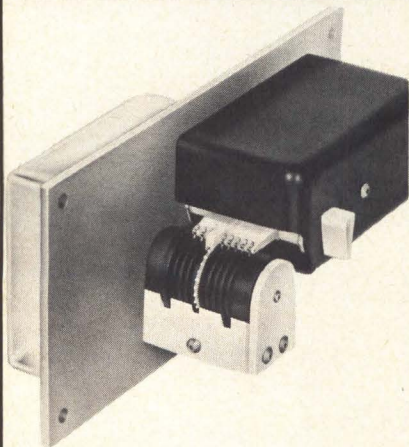
ONLY \$180

Simplicity

VALUE ENGINEERED

Reliability

EXCEEDS 100 MILLION CYCLES



CMC MODEL 18 Tape Reader

This simple unit reads tape uni-directionally . . . at 30 characters per second. **Starwheels sense holes; output is in the form of contact closures.**

Model 18 Tape Reader provides control equivalent to that of far more costly units **without complex circuitry or timing.** As easy to use as a relay.

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CIRCLE NO. 39 ON INQUIRY CARD

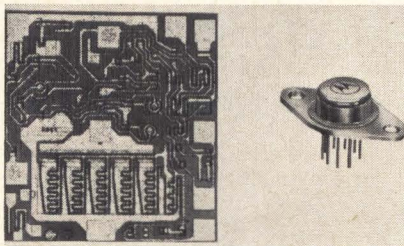
NEW PRODUCTS

HIGH SPEED FUSE

The Series 817 millisecond fuse is designed specifically to protect IC's and power transistors in digital micro-circuits. It is low in cost and available with ratings of 0.5, 0.75 and 1.5 A. All three units in the series will blow in one millisecond with small overloads. They will blow as fast as 50 μ s with 30 A overloads.

Packaged in a TO-46 can, this miniature fuse features 40 V at 50 A circuit interruption and insulation resistance of 10 megohms at 150 V. It has a -55°C to $+125^{\circ}\text{C}$ operating temperature range. Helipot Div. Beckman Instruments, Inc., Fullerton, Calif.

Circle No. 242 on Inquiry Card.



IC VOLTAGE REGULATOR

The MC 1560 has 0.002%/V typical regulation with changes in input voltage, and 20 milliohms output impedance with output current up to 500 mA.

A zero-temperature-coefficient voltage reference is provided by a resistive divider on the monolithic chip which balances the positive TC of a zener diode against the negative TC of forward-biased diodes.

A shut-down control allows both the load and the regulator bias current to be turned off, reducing system power consumption. The regulator has a typical recovery time for a drop in load current from 100 to 50 mA of 50 ns.

It is available in two packages: the MC-156-OR in a 9-pin variant of the TO-66 power transistor case. This device can dissipate 10 watts at a case temperature of 65°C and regulate a 500 mA load current. The MC 1560G, packaged in the 10-pin TO-5-type case, can dissipate 1.8 watts at a case temperature of 25°C and regulate a 200 mA load current. Motorola Semiconductor Products Inc., Phoenix, Ariz.

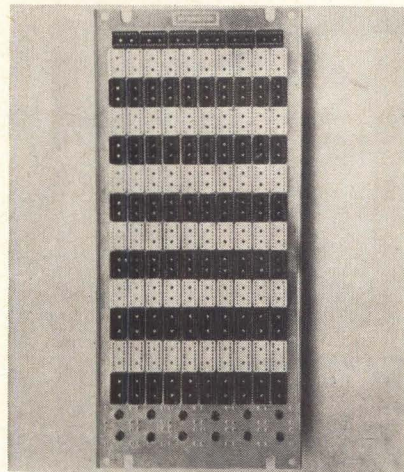
Circle No. 223 on Inquiry Card.

SET-POINT CONTROLLER

A digital set-point controller, Model 1050, when used with the Hickok DMS 3200 digital measuring system, can start and/or stop the operation of any peripheral function at pre-determined measurement values, as selected by the operator. Set-points are absolute, assuring start or stop functions at specific values with zero set-point error. Although the controller was designed primarily as a companion unit to the DMS 3200 System, it can be used with any device which provides ten-line decimal data outputs at the proper logic levels along with appropriate read commands.

Two controllers may be used in tandem for six-digit control. Front panel indicator lamps show operator when measurements reach set-point values and internal relays close when set-point values are reached. Closure contact connections terminate at terminal blocks for external connection to controlled devices. Hickok Electrical Instrument Co. Cleveland, Ohio.

Circle No. 235 on Inquiry Card.



MODULAR IC PACKAGING

Series 2900/5800 for direct entry dual-in-line packaging, allows use of current 14 and 16 pin ICs plus the new MOS circuits in standard product lines.

A module may contain any possible combination or any arrangement of 14, 16 or 24 pin sockets and transistor-discrete component receptacles. To achieve the specific optimal packaging configurations required by an application, several interchangeable modules may be used in multiple. Compromising the basic systems design to fit standard packaging is not required. Interdyne Inc., Los Angeles, Calif.

Circle No. 220 on Inquiry Card.



7/8 of a good engineer is not visible on the surface. But RCA knows that.

Speaking of visibility, there may be some things about RCA which are not too obvious. We are in a period of fast expansion; working on large-scale multipurpose computers with special emphasis on Information Systems.

And we are looking for high-level engineers who haven't begun to use all their potential. But want to.

They're engineers with a broad outlook. They don't home in on a narrow specialty. They can see pretty far ahead. They couple ingenuity and a fresh way of thinking with a detailed knowledge of the computer industry. They want to make their mark on that industry.

They are interested in Patents. Copyrights. Publishing. If that's what we'd find when we look into your other 7/8, you'll have a unique opportunity at RCA.

If your experience includes circuit designing, micro-circuits, systems communications or design automation, write us today.

Contact Mr. J. H. Nostrand, Dept. HW-7
RCA Information Systems Division,
Bldg. 13-2, Camden, New Jersey 08102.
We are an equal opportunity employer.

RCA

What weighs
135 pounds,
types 2400 lines
a minute
and costs
under \$10,000?

The
Shepard 880
Minityper.



Moving up in printer speed and number of columns generally means a move-up in price, size and weight.

Not so with the Shepard 880. It's fast (2400 L.P.M. numerics or 1200 L.P.M. alpha- numerics with up to 80 columns), yet weighs only 135 pounds and is designed to be rack-mounted with ease.

And now, because we've moved into full production on the 880, we are able to offer it at a price nearly half that of our prototype models.

If you are interested in saving space and saving money with a lightweight, compact, high speed printer, we suggest you write us.

FEATURES:

- Solid state electronics
- Size (2 drawers) each 8 $\frac{3}{4}$ "H x 19"W x 22"D
- Weight:
Mechanism Drawer (pictured above) 98 lbs.
Electronics Drawer 37 lbs.
- Speed up to 2400 L.P.M.
- Up to 80 columns available
- Character set 64 alpha- numerics
- Adjustable line spacing
- Self contained Power Supply
- Code Standard ASCII
- Interface:
Bit parallel, character serial
DTL or TTL compatible
Logic "0" = 0 volts
Logic "1" = +3.5 to 5.0 volts
- Single or 2-part forms
- Ink Roller System or impact paper

VOGUE

**Shepard
Division**

480 MORRIS AVE., SUMMIT, N.J. 07901
(201) 273-5255 • TWX 710-984-7989
CIRCLE NO. 40 ON INQUIRY CARD

NEW PRODUCTS

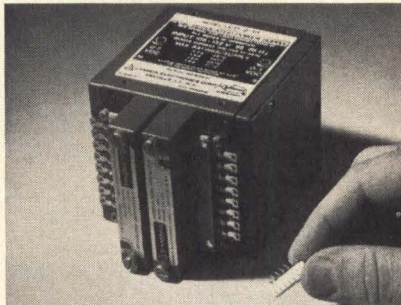
MAG TAPE SYSTEM

The 850 magnetic tape transmission system is a 800 bpi, 9-track system that operates at 6,000 characters per minute.

The 850 was designed primarily for use with Community's 100SR data communication system. As the 850 receives data from the 100SR units, it transforms the data instantly and automatically to computer code recorded on magnetic tape compatible with IBM-360 type computers using series 2400 9-track tape drives. The data is recorded at 800 bpi (bits per inch) density.

It can also transmit computer-prepared data to remotely-located 100SR units by reading the data block-by-block into a 160-character (or larger) MOSFET buffer memory unit. Community Corp., N.Y., N.Y.

Circle No. 212 on Inquiry Card.

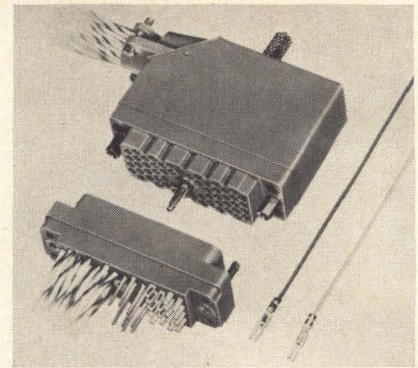


DUAL OUTPUT POWER SUPPLY

Features of the LCD-2 Series include independent operation, independent remote sensing, independent remote programming and series parallel (master/slave) operation. Each supply is electrically inserted and floating with respect to ground.

The LCD-2 Series is all-silicon and convection-cooled, with no external heat sinks. Eight models are available with voltage ranges (each side) to 120 Vdc. Regulation is 0.01% + 1 mV. Ripple and noise is 250 μ V RMS; 1 mV peak-to-peak. Temperature co-efficient: 0.01% + 300 μ V/ $^{\circ}$ C. The series is multi-current-rated for 40 $^{\circ}$, 50 $^{\circ}$, 60 $^{\circ}$ and 71 $^{\circ}$ C, with current ratings to 300 mA. Input voltage and frequency range is 105-132 Vac. 57-63 Hz. Weight of the supply is 2 $\frac{1}{4}$ lbs, and it measures 3 $\frac{5}{32}$ " x 3 $\frac{3}{32}$ " x 3 $\frac{5}{16}$ ". Lambda Electronics Corp., Melville, N. Y.

Circle No. 219 on Inquiry Card.



RECTANGULAR CONNECTORS

Series 8016 designed for rack and panel or in-line cable applications, is available in five insulator shell sizes (20, 38, 56, 90, and 120 contacts), and features the patented VARICONTM hermaphroditic fork type contact which can be customer inserted into the insulator. It is available with a variety of tail configurations; wire wrap, wire crimp, wire hole or tapered tab. The contacts are made of phosphor bronze with gold over nickel plating and are rated at 8.5 amps. Contact density is a .150" by .130" honey comb grid pattern.

The insulators (plug and receptacle) are made of glass-filled diallyl phthalate (per MIL-C-14F, type SDGF). Elco Corp., Willow Grove, Pa.

Circle No. 209 on Inquiry Card.

LABORATORY TAPE RECORDER

The AV-15000R laboratory recorder employs a unique tape handling principle allowing direct longitudinal recording to 15 MHz. The instrument operates bi-directionally to speeds of 960 ips, recording all frequencies longitudinally. It records 36 tracks on $\frac{1}{2}$ -inch tape and uses a simple indexing mechanism to step the heads.

Tape widths of $\frac{1}{4}$, $\frac{1}{2}$ and 1 inch, of any base thickness, can be handled, and speeds can be increased in decades from 15 to 960 ips with any two of them electrically switchable on a single recorder.

Employing either direct, FM or high-density digital recording, the AV-15000R is suited to many instrumentation uses ranging from acquisition of telemetered missile or radar data to the handling of vibration, strain, temperature measurement, to geophysical and other scientific measurement.

The complete transport unit weighs 220 lbs. and fits into a standard 19-inch rack. Newell Industries, Sunnyvale, Calif.

Circle No. 207 on Inquiry Card.



Collins' New Data Program Creating New Opportunities

Collins' C-8500 C-System gives users the first completely integrated system with virtually unlimited expansion capability.

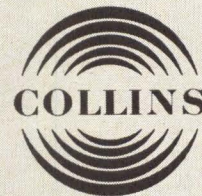
This new concept in computer applications is creating exceptional career opportunities for: Programmers, Hardware Diagnostic Programmers, Circuit Design Engineers, Memory Design Engineers, Digital System Engineers, Digital Systems Analysts, Logic Design Engineers, Mechanical Engineers, Data Systems Analysts and Applied-Systems Analysts/Programmers.

Engineers, Physicists, Mathematicians, and those with degrees in other physical sciences (1 to 5 years experience) will

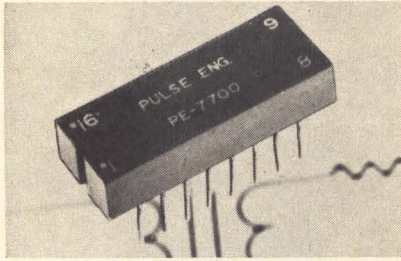
find an outstanding opportunity to learn and progress rapidly in the data field, even without previous data experience.

Please send your resume in confidence to Manager of Professional Employment, Dept. 100, Collins Radio Company, Dallas, Texas 75207; Cedar Rapids, Iowa 52406; Newport Beach, California 92660; or Toronto, Ontario.

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NEW PRODUCTS

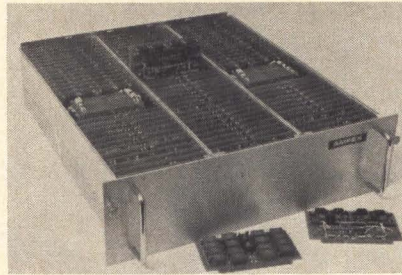


PULSE TRANSFORMERS

A Pulse Transformer Series designed specifically for computer floating switch applications includes four identical transformers in a high density package compatible with integrated circuits. The transformers feature controlled droop with primary inductance variation of less than 10% over the temperature range of 0° to 70°C.

A variety of 1:1 and 2:1 turns ratio transformer modules are now available from stock. Pulse Engineering Inc., Santa Clara, Calif.

Circle No. 232 on Inquiry Card.



CORE MEMORY

Model 3DM-650 has a cycle time of 650 ns and a data access time of 275 ns. Its modular expandability allows storage of up to five million bits.

The basic module can store 4,096, 8,192, 12,228 or 16,384 words of from 4 to 40 bits. Size adjustments within those capacity ranges are made through the addition or deletion of printed circuit card assemblies and core-planes. Capacities exceeding 16,384 words by 40 bits and ranging up to 65,536 words by 80 bits are obtained by adding memory modules. Ampex Corp., Redwood City, Calif.

Circle No. 229 on Inquiry Card.

MICROMINIATURE RELAYS

Designated Series MA and MS, the new TO-5 transistor sized, hermetically sealed DPDT relays are rated at 1 A and designed to withstand high environmental stresses. They meet all applicable requirements of MIL-R-5757.

The consistent contact performance of these relays is assured by strict environmental control throughout manufacture and 100 percent inspection of parts, assemblies, and of the completed products. HiG, Inc., Windsor Locks, Conn.

Circle No. 248 on Inquiry Card.



FOUR PHASE STEPPER MOTOR

The 18M34A1 variable reluctance stepper motor features a high torque/inertia ratio, and is suitable for bi-directional operation at stepping rates of up to 500 steps per second. The normal step angle is 15 degrees.

Typical applications are tape readers, incremental recorders and analog to digital converters. Muirhead Instruments Ltd., Stratford, Ontario, Canada.

Circle No. 211 on Inquiry Card.

CARD TRICK

Be the envy of your engineering section with a Flotron Model 30 Card Trick. This trick will enable you to extract pc cards from the rack quicker than the eye can see. □ To make the trick work, attach the Model 30 to the pc card and squeeze gently. At the same time, utter the magic word "Flotron"! Presto, you've performed the card trick... the pc card has been extracted *without damage* to costly connectors. □ The Flotron Model 30 Pin Type extractor accommodates cards with 3.87 center-to-center holes; .220 from chassis rail to the holes. Moulded from self-lubricating Delrin® plastic with all operating parts manufactured from stainless steel. □ Model 30's cost from \$15-35. It's no trick to buy one, either. FLOTRON INDUSTRIES, INC., 1201 E. Grand Avenue, El Segundo, Calif. 90245, phone (213) 678-8164.



PC CARDS BY CIRCUITRONICS, INC.

CIRCLE NO. 41 ON INQUIRY CARD

MEMORY STACK

A 500 ns core memory stack features 21½D organization with 18 mil ferrite memory cores. Capacity sizes range from 8K words by 9 bits/word to 16K by 18. Sizes to 16K by 36 are also available with a maximum speed of 600 ns.

With a 50 ns current rise time, half select drive current is 390 mA and full select drive current is less than 800 mA. Stack output is 25 mV after a worst case disturb pattern. The stacks can be operated over a temperature range from 0°C to 100°C. Ferroxcube Corp., Saugerties, N.Y.

Circle No. 249 on Inquiry Card.

THE HONEYWELL MAN:

a generation ahead

Conceiving today the computer techniques of tomorrow . . . the new ideas, the innovations that enable Honeywell to maintain its competitive edge . . . adding new impetus to Honeywell's growth in America's fastest growing industry.

The Honeywell Man is ahead of his contemporaries in other ways. Honeywell's unprecedented growth provides unlimited opportunities for personal advancement. And, today, opportunities are better than ever at Honeywell. New facilities have been added or started. The Technology Center in Waltham, Massachusetts, has been expanded. Requirements for Technical Specialists exist at all levels . . . with special emphasis on the following areas:

HARDWARE SPECIALISTS:

- Systems Design
- Communications Subsystems Design
- Peripheral Control Design
- Processor Design
- Logic Design
- Maintainability
- Circuit Design
- Diagnostic Programming
- Design Automation

Please forward your resume to
Mr. Jack Wermuth.

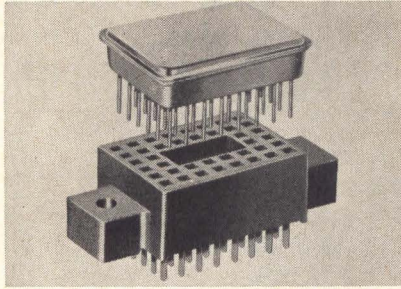
The Other Computer Company: **Honeywell**

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Waltham, Massachusetts 02154

Opportunities exist in other Honeywell Divisions. Send resumes to F. E. Laing, Honeywell, Minneapolis, Minnesota 55408. An Equal Opportunity Employer.



NEW PRODUCTS



MODULE SOCKET

This 40 pin molded module socket is designed to accept modules with round or flat leads. Wiping type beryllium copper gold plated contacts assure positive retention. Contacts are on a .100 in. grid pattern. Body material is Diallyl Phthllate. Chamfered entry holes provide easy insertion. .093 diameter mounting holes are provided for mounting to chassis. Socket comes with printed circuit termination.

Overall body dimensions: 1.375 Max l x .700 Max w x .360 Max h; Terminals protrude .120 ± .010 beolw socket body. Augat, Inc., Attleboro, Mass.

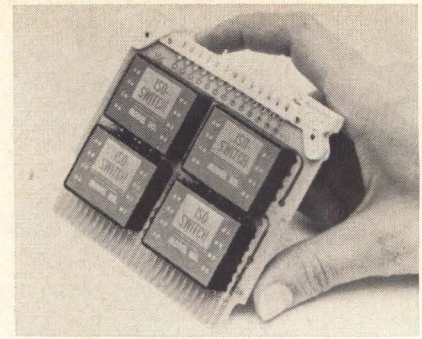
Circle No. 203 on Inquiry Card.



KEYBOARD-TO-TAPE UNIT

The KDR data recorder records in high densities on magnetic tape, in formats for direct use by EDP systems. Memory stores the operator's program (s.) holds 48 to 160 characters of data, and includes five different modes of operation to provide alternate uses of the machine: entry, verify, search, display and record/read. Extensive program control, including standard features such as unlimited left zero fill, aids maximum production. Accuracy of tape writing is automatically verified by a check-read operation to compare newly recorded data to data in memory. Potter Instrument Co., Inc., Plainview, N. Y.

Circle No. 214 on Inquiry Card.



ISOLATING DRIVER/RECEIVERS

Five isolating long-line driver/receivers are designed to drive digital data at high speeds over long lines. Typical applications include two-way communication between central processor and remote stations, hard-wired data links providing isolation and level shift, coupling "black boxes" and peripherals into computer main frames, and elimination of ground loops and noise in digital/analog systems.

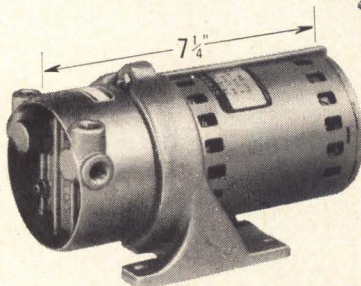
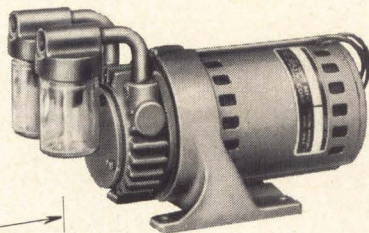
The new drivers can drive up to 10,000 feet of twisted pair line or coax cable at 100 kHz; up to 1000 feet at 500 kHz. Components Div., Electronic Engineering Co. of California, Santa Ana, Calif.

Circle No. 221 on Inquiry Card.

NEW for OEM

Two oil-less miniatures for vacuum or pressure

Model 1031 — 1 cfm
15" Hg continuous
20" Hg intermittent
10 psig continuous



Model 0531 — .6 cfm
20" Hg continuous
15 psig continuous
20 psig intermittent

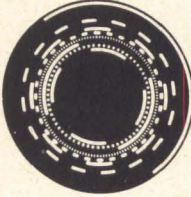
Check out the one that's best for you . . .

Two potent vacuum/pressure sources help make your product lighter, more compact. ■ No lubrication ever required. Deliver completely oil-free air. ■ Check one out on your equipment. Gast offers many other choices, too. ■ Write for Gast Catalog and Designers Handbook.

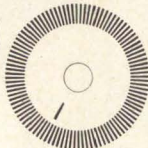
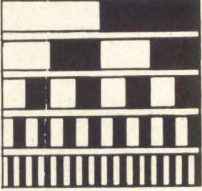
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CIRCLE NO. 42 ON INQUIRY CARD



DISCS

Encoders • Tachometers • Choppers
Photo Emulsion • Metalfilm • Metal



DYNAMICS RESEARCH CORPORATION
The Metrigraphics Div.
38 Montvale Avenue, Stoneham, Mass. 02180

Tel. (617)
438-3900

CIRCLE NO. 43 ON INQUIRY CARD

Logic Designers:

Help IBM develop large-scale data processing systems.

We need Logic Designers to develop the hardware for large-scale scientific systems, designed to solve complex problems having extremely large computational loads. Loads that are found in such areas as weather forecasting, radiation burst effects, or signal processing.

Imaginative new concepts.

Advanced concepts in system architecture are being explored to achieve exceptionally high data processing rates.

You would work on the design and development of systems hardware and its integration into the overall system.

If you qualify, you could get in on the ground floor of important advances in large-scale computation.

You should have an E.E. degree (or its equivalent) and two years' experience in large-scale scientific or commercial data processing systems, including logic design.

Grow with IBM.

This development program is just one of the many we have at IBM's Federal Systems Division, located near Washington, D.C.

For example, we are deeply involved with the manned space program. Working on systems to analyze delicate seismological disturbances. And designing many new real-time, on-line information systems.

It has been these kinds of advanced programs that have kept IBM a leader in the information processing industry.

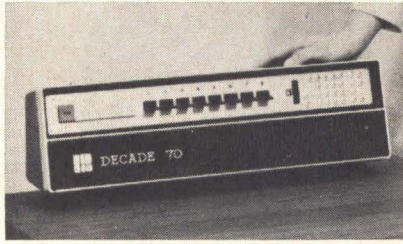
Call or write.

Learn more details. Call Jim Dunn at (301) 921-7724 collect any weekday between 9 and 4:30. Or, if you prefer, send a brief letter or resume to him at IBM Corporation, Federal Systems Division Headquarters, Dept. CB1029, 18100 Frederick Pike, Gaithersburg, Md. 20760.

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NEW PRODUCTS



HIGH-SPEED COMPUTER

The DECADE 70 is an 860 ns digital computer, rack-mounted and designed for applications in the OEM systems market. Features include a 16-bit memory word, a standard 4K memory field, expandable to 16K, memory parity, and a memory-protect function, as well as direct memory access.

Previously identified as the 70/2, the new computer will be marketed as the DECADE 70. Software is presently operational and includes a single-pass assembler, FORTRAN IV, CHAT, mathematical subroutines, and a utility package. Decade Computer Corp., Huntington Beach, Calif.

Circle No. 218 on Inquiry Card.



DIGITAL COMPARATOR

Model 5510 accepts parallel input of up to five digits plus over-range; compares the input to locally or remotely set limits; and outputs Hi-Lo-Go information via a rear connector. Each limit is controlled remotely, or manually set to issue an ADVANCE pulse to other equipment, it may be set to STOP other equipment or a system when an "out of limits" situation is encountered.

High speed operation is accomplished through "time-sharing" and a 1 μ sec compare time. Non Linear Systems, Inc., Del Mar, Calif.

Circle No. 213 on Inquiry Card.



PULSE GENERATOR

Model PG-11 provides single or double pulses, pulse pairs, pulse bursts or one-shot output. It will operate over a repetition rate range of from 10 Hz to 20 MHz in the double pulse mode and to 10 MHz in the single pulse mode. Rise and fall times are 5 ns max. at full ± 15 V output amplitude.

It may be triggered from dc to 20 MHz and/or may be synchronously or asynchronously gated. Output amplitude is switch selected plus or minus and is without measurable dc component. Repetition rate, output width (25 ns to 10 ms), delay (20 ns to 10 ms) and amplitude are continuously variable over wide dynamic ranges. Chronetics, Inc., Sparta, N. J.

Circle No. 228 on Inquiry Card.



Your Place in the SUN! (in Southern California)

The clear, sunny weather in Southern California is just one of many reasons for coming to Varian Data Machines, a Subsidiary of Varian Associates. You'll be joining a fast growing company. Orange County is noted for its excellent living and recreational facilities. You'll have 12 days vacation the first year, plus 8 paid holidays. Our stock purchase plan enables our employees to participate in our growth. There are many more reasons, including our new ultra-modern facilities!

DEVELOPMENT ENGINEERS: Computer processor and peripheral development. Perform main frame planning and development including specifications, logic design and integration with software and other hardware groups. We prefer three to five years related experience including some integrated circuit experience. BSEE or MSEE.

MEMORY ENGINEERS: Memory and Circuit Engineers with experience in the design of high speed core memories. Must be capable of working independently and doing original work. Good knowledge of both analog and digital circuit design is required. BSEE or MSEE degree with a minimum of three years professional experience.

PROGRAMMERS: Requires degree in Math or Physical Science and three to five years experience. Assignments include: designing and developing new model software systems and automated design programming; and real-time sharing programming for customers on our own machines.

Interested applicants should address their inquiries to: Personnel Manager

varian data machines

a varian subsidiary

2722 Michelson Drive
Irvine, California 92664

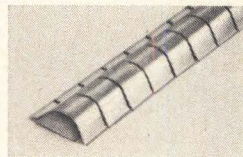
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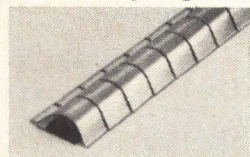
CIRCLE NO. 903 ON INQUIRY CARD

When RFI problems get sticky, try *sticky* fingers®

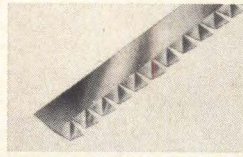
Attaches faster, shields better than anything else!



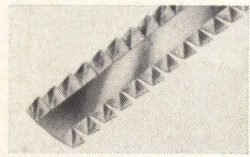
SERIES 97-500 The original Sticky Fingers with superior shielding effectiveness.



SERIES 97-510 Provides even better magnetic shielding with Magnefil® insert strips.



SERIES 97-555 New Single-Twist Series for use when space is at a premium. Measures a scant $\frac{3}{8}$ " wide.



SERIES 97-560 New $\frac{1}{2}$ " wide Double-Twist Series, ideal for panel divider bar cabinets.

Now you can specify the exact type beryllium copper gasket that solves just about every RFI/EMI problem. Perfect for quick, simple installation; ideal for retro-fitting. Self-adhesive eliminates need for special tools or fasteners. Write for free samples and catalog.



INSTRUMENT SPECIALTIES COMPANY, Dept. CD-57

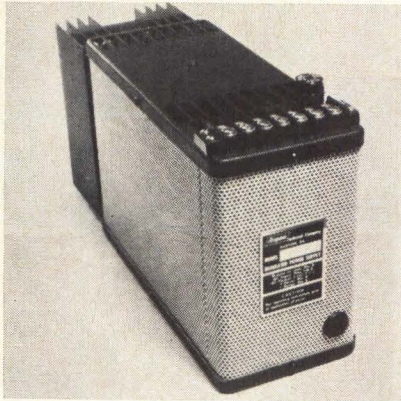
Little Falls, N. J. 07424

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CIRCLE NO. 44 ON INQUIRY CARD

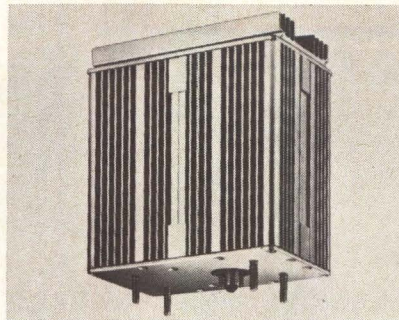
NEW PRODUCTS



AC TO DC POWER SUPPLIES

Fourteen ac to dc regulated power supplies have output current ranging from 7 to 10 A. The models can be supplied for operation at either 0 to 55°C or -21 to +71°C. Nominal voltages of these new units are from 3 to 15 V with adjustments of ± 0.25 to ± 0.5 V. Load regulation ranges from ± 0.4 to $\pm 0.5\%$; line regulation is $\pm 0.05\%$; ripple is 1 mV rms. They can be rack mounted to a 3 1/2 x 19-inch panel with four screws. Acopian Corp., Gaston, Pa.

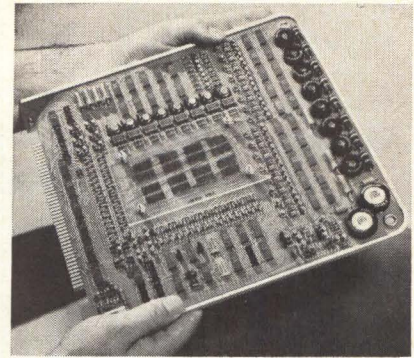
Circle No. 210 on Inquiry Card.



POWER SUPPLY MODULES

HT/HTA Series features regulation of 0.025% for $\pm 10\%$ line variation and an MTBF in excess of 60,000 hours in extreme environments. The supplies are completely enclosed and thus can operate in heavily contaminated atmospheres at ambients up to 60°C w/o heat-sinking, and higher if cooling is provided. Standard input voltage is 105-125 Vac, 57-63 Hz single phase; 105-125 Vac, 50-440 Hz or 220 Vac, 60 Hz are available options. The supplies are approximately 6 1/2" long, 4" wide, and 7" high; and are designed to be fully maintainable. Mid-Eastern Industries, Inc., Scotch Plains, N. J.

Circle No. 216 on Inquiry Card.



HIGH SPEED, LOW COST MEMORY

The MEMCARD™ system, contained entirely on a single, flat circuit board features a capacity of 1024 x 8 and a cycle time of 1.5 μ s. Address registers, power on/off, core memory and associated electronics are contained on one 12 by 12 inch board only 1/2 inch thick.

The 3-wire, 3-D memory, designed to operate in commercial environments of 0 to 50° C, also features temperature compensation within the memory itself. It is contained on a plane in the center of the printed circuit card and is comprised of eight mats, each containing 1,024 cores. Sanders Associates, Nashua, N. H.

Circle No. 202 on Inquiry Card.



SERIES 500 KEYBOARDS

- Choice of 3 standard alphanumeric models: 47, 56, 73 keys or any specified arrangement from 10 to 73 keys. Any or all keys illuminated.
- Seven data lines ASCII + parity + strobe.
- High reliability magnetic dry reed keys plus solid-state encoding. Solid-state keys available Jan. 1969. Will be completely interchangeable with present designs.
- Flexible design. Easily adapted to your requirements for prototype evaluation.



GRI Keyboard designed especially for data entry and retrieval on computer used in airline reservation system.



O.E.M.'s—Do you need a special keyboard to mount in your own cabinet? If you need only one or thousands, we will customize them for you at low cost. Fast service, too...

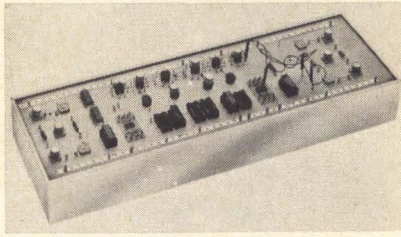
For complete information contact: **GEORGE RISK INDUSTRIES, INC.**

672 15th Ave., Columbus, Nebr. 68601 • Phone: 402-564-2777

CIRCLE NO. 45 ON INQUIRY CARD



NEW PRODUCTS



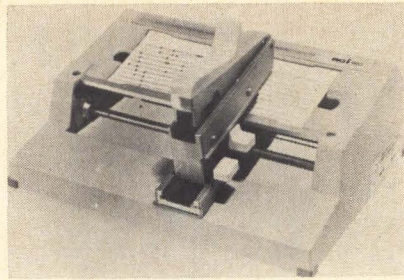
INTEGRATED CIRCUIT KIT

An IC kit provides a quick means of inter-connecting nearly all configurations of integrated circuits for experimentation.

Called the 29X Kit, its mounting surface is of pre-punched Micro-Vector-board. The .042" diameter holes on 1/10" grid spacing allow high or low density mounting of discrete components. The mounting surface is supported by 2" high aluminum frame-loc rails.

Included are a T42-1 push-in micro clip, K24C pins, 14 and 16-pin D.I.P. sockets with wire-wrap tabs that fit the holes. Vector Electronics Co., Inc., Glendale, Calif.

Circle No. 224 on Inquiry Card.

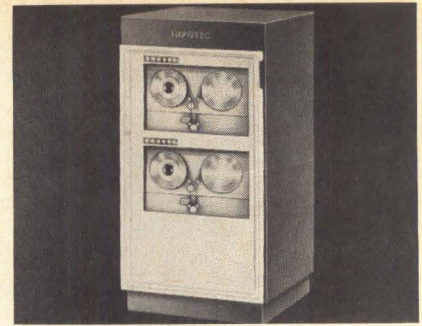


PRECISION MANUAL KEYPUNCH

The Model ACI-960 may be located in those areas requiring occasional keypunching, but not justifying a large equipment investment.

Programmers can use the ACI-960 for program changes, corrections or additions. Operations personnel can use the ACI-960 for replacing damaged cards, corrections or minor modifications to jobs without leaving the computer room. Data acquisition for inventory, production control, turn-around documents and shipping documents are among hundreds of applications often requiring some keypunching, but located far from the central keypunch area. Periphery, Inc., Framingham, Mass.

Circle No. 205 on Inquiry Card.



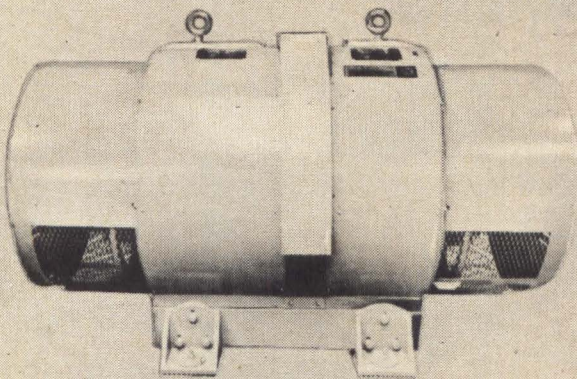
MAG TAPE SYSTEM

The TS-1130 is a complete magnetic tape system especially designed and engineered for the IBM-1130. Its compatible functions permit the efficient utilization of file data between the IBM-1130 and the IBM-360 or other medium-to-large scale computers. Some valuable applications resulting are in the areas of bulk data storage (historical files), data I/O storage media, and buffered communications data storage.

The TS-1130 is available in 7 and 9 track models and provides medium speed transfer rates for reading/writing IBM-compatible tapes. Tape transport mechanism and all electronics are self-contained in one compact cabinet. Infotec, Inc., Rye, N. Y.

Circle No. 217 on Inquiry Card.

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AC 500 KW 1 phase, 1500 KW 3 phase. DC to 50 KW.

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To 1000 KW, direct drive, belt drive, gear drive, totally enclosed, complete enclosure and common frame.

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Input 12/230 volts DC. Output 115/230 volts AC.

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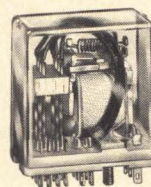
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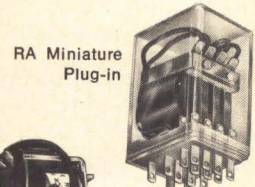
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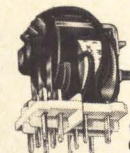
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CIRCLE NO. 47 ON INQUIRY CARD



DIGITAL MONITOR

The LOGICO digital monitor provides a simultaneous visual indication of the logic states of up to 20 digital or binary circuits. The LOGICO will not affect the circuit under test and can be used with any commonly used logic or voltage system in use today. With each logic system a reference potential is determined and is connected to the LOGICO's Reference terminal; the other inputs are connected to the particular circuit points to be observed.

Two models are offered, the Model BPL10 with 10 indicators and an internal supply and the Model BL10 with just 10 indicators. A single BPL10 can power a BL10; however, many BL10's can be paralleled using an external power supply or batteries. Industrial Inventions, Inc. Monmouth Junction, N.J.

Circle No. 234 on Inquiry Card.



DATA COMMUNICATIONS TERMINAL

The Inktronic® terminal prints at speeds up to 1,200 words per minute and can operate over voice-grade telephone lines. Characters are formed on ordinary paper by electronically deflecting spurts of ink—much as electrons are directed to the face of a cathode ray tube. The machines have solid state design and are virtually noiseless.

The ink costs less than a typewriter ribbon, with one print delivering 1,000 to 1,500 hours of printing at 1,200 words per minute, and no special paper is required.

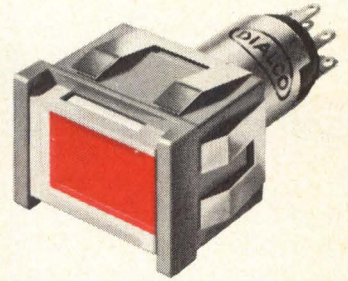
Two configurations of the Inktronic terminal are now offered by Teletype. They are the RO (receive only) and the KSR (Keyboard send-receive) sets. The RO is expected to find wide acceptance as a monitor of high speed data transmission or as a computer output terminal. The KSR uses the same printing method, but has a keyboard similar to that of a modern office typewriter.

The KSR can "talk" to a computer at a rate equal to the operator's typing speed and receive at the faster rate of up to 1,200 words per minute. Teletype Corp. Skokie, Ill.

Circle No. 233 on Inquiry Card.

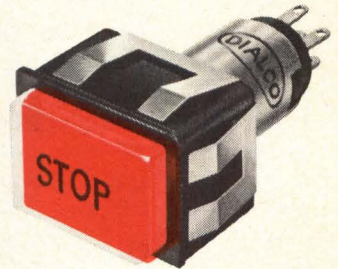
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low-profile snap-in-mounting push button switch or matching indicator that is interchangeable with most 4-lamp displays... available in a full range of cap colors... with a choice of bezels with or without barriers in black, gray, dark gray or white.



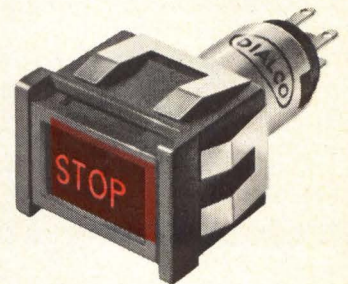
and a

legend presentation that's positive (like this one) or negative (like the one below) or just plain (like the one above)... one that's white when "off" and red, green, yellow (amber), blue or light yellow when "on"... or colored both "on" and "off."



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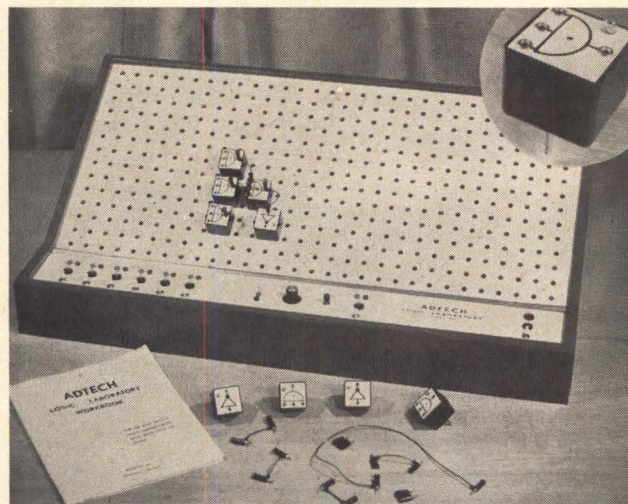
NEW PRODUCTS

ACCUMULATOR/REGISTER

The MM510 dual, dynamic 64-bit accumulator/register permits on chip recirculation of data into a serial register memory. The MM510 is a high frequency (4MHz), low power (0.8mW/bit/MHz) device designed for use in high speed "drum" type memory and high speed display system applications.

The construction of the device is such that recirculation of data is performed independent of the output drive circuit, thus making it insensitive to external loading. A push-pull-output stage is also incorporated into the design in order to increase the maximum frequency and significantly reduce output power dissipation. National Semiconductor Corp., Santa Clara, Calif.

Circle No. 227 on Inquiry Card.



LOGIC LABORATORY

A logic laboratory, the Model 401A, consists of a 32" x 18" logicboard and a set of sixty 1.5" x 1.5" x 1.25" logiccubes and 150 patchcords of various lengths. Power (5.5 v) and ground are applied to the logiccubes when they are placed anywhere on the logicboard with any one of four orientations. Signal connections between logiccubes and between logiccubes and the control panel of the logicboard are made by miniature stackable banana-plug patchcords. All signal connections are gold plated.

Each logiccube performs a single logic function. Available functions include not, and, or, nand, nor, exclusive-or, majority, RS flip-flop, JK flip-flop, half-adder, full-adder, one-shot, clock, toggle, pushbutton, relay, BCD counter, nixie display, serial parallel register, etc.

Features include: replaceable indicator lamp for each output, logic symbol on face of logiccube, TTL I.C.'s performing all logic functions, fanout of 10 (worst case), 1 V worst case noise margin, and circuits encapsulated in phenolic case.

The logicboard contains a 5.5 V, 4 A power supply which is fully protected against short circuit and overvoltage. Peak to peak ripple, load and line regulation are less than 50 mV. Adtech, Honolulu, Hawaii.

Circle No. 238 on Inquiry Card.

MAGNETIC DISC DRIVE

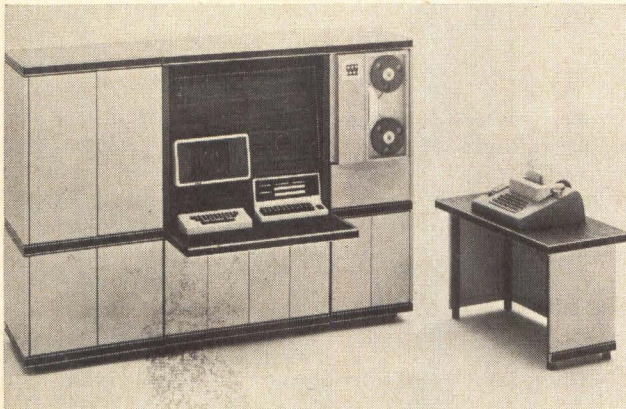
The Model 1100 Disc Drive, is intended specifically for System 360 users and has been designed to meet all their requirements—program, interface, styling, maintenance and reliability.

The chief feature of the Model 1100 is the extremely reliable hydraulic head actuator. This component, which is directly interchangeable with the 2311 hydraulic actuator, eliminates the thermal, magnetic and drift problems inherent in electronic actuators. It also minimizes periodic adjustment and maintenance requirements.

Specifications of Model 1100 include:

Disc pack; IBM 1316 or equivalent; Recording mode, double frequency; Storage capacity, 7.25 megabytes; Transfer rate, 156,000 8 bit bytes/sec; Disc speed, 2400 rpm; Access Times, Adjacent tracks—25ms, Average overall—75ms, Maximum overall—135ms; Latency Time, Maximum—25ms, Average—12.5ms; Written track width, .008"; After tunnel erase, .005"; Dimensions, 24"D x 30"W x 40"H. Linnell Electronics, Inc., Pennsauken, N.J.

Circle No. 236 on Inquiry Card.

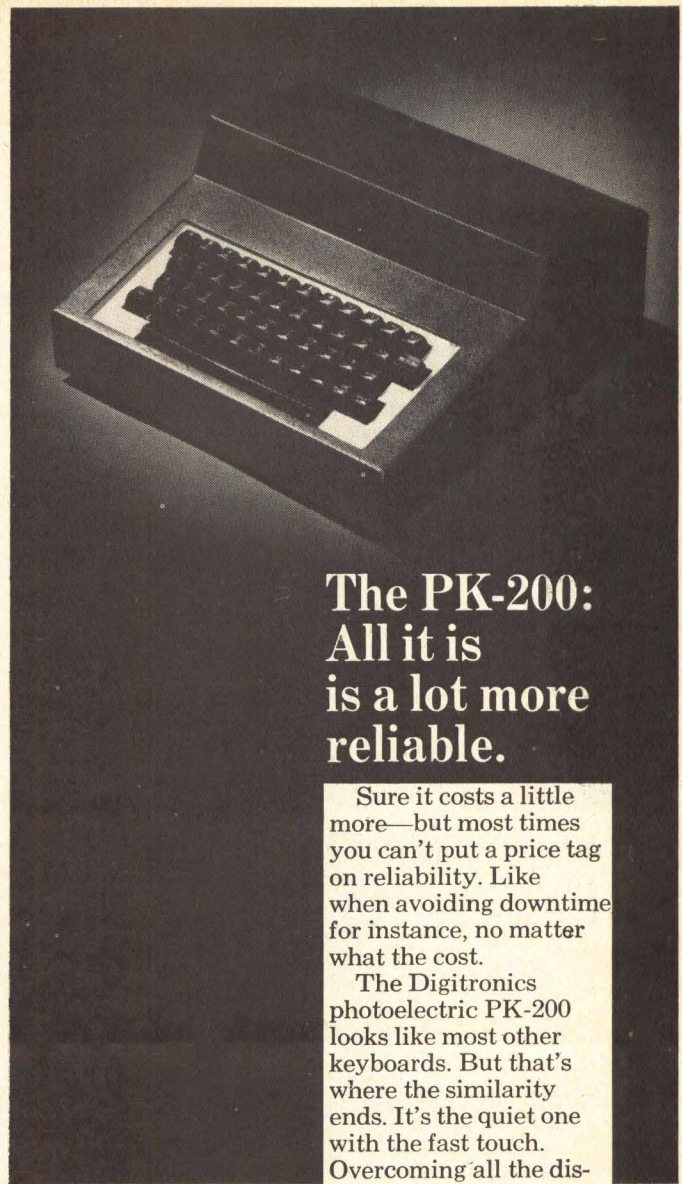


MICROFILM READER

The FR-80 recorder generates graphic information on microfilm directly from digital output. It has a resolution of 16,384 by 16,384 programmable points, and produces 20,000 lines per minute. The FR-80 accepts formatted tapes for the Stromberg Datagraphic 4020, 4060, and 4400, for California Computer Products plotters, and for IBM 360/1401 impact printers. The system will also be used for automatic typesetting, animated films, and data retrieval systems. In addition to over 300 million addressable points per film frame, the high resolution of the unit includes eight programmable line widths and eight programmable spot intensities.

The FR-80 has a comprehensive, system-oriented software package with on-line editing, debugging and paging. It has a variety of character styles, and a choice of 64 programmable character sizes, eight programmable intensity levels, five programmable character rotations, and eight programmable spot sizes. Speed is 10,000 characters per second, with an optional 100,000 characters per second. The system records on both 16 and 35 mm sprocketed and unsprocketed film, and an on-line monitor display provides complete operator interaction. Forms overlay is program selectable, and an optional graphics design package with a light pen and programmable controls provides on-line forms design, character design and extended graphics capability. Information International, Los Angeles, Calif.

Circle No. 237 on Inquiry Card.



The PK-200: All it is is a lot more reliable.

Sure it costs a little more—but most times you can't put a price tag on reliability. Like when avoiding downtime for instance, no matter what the cost.

The Digitronics photoelectric PK-200 looks like most other keyboards. But that's where the similarity ends. It's the quiet one with the fast touch. Overcoming all the disadvantages that go along with mechanical switch designs; completely eliminating switch contacts, minimizing RFI/EMI.

Its photoelectric encoding technique directly converts key operations into digitally-coded electrical signals. Positive interlocks combined with a strobe channel give you guaranteed accuracy.

Keyboard layouts are unrestricted and can contain from 10 to 75 keys. Output codes up to 14 bits are available.

Let us tell you what we don't have room to tell you here. Write Digitronics Corporation, Albertson Avenue, Albertson, N.Y. 11507.

 **DIGITRONICS**

CIRCLE NO. 50 ON INQUIRY CARD



Digital Display Head

This 12 page catalog fully describes the Midgi-Lite™, a direct viewing, seven segment digital display head. Pinlites Inc., Fairfield, N. J.

Circle No. 329 on Inquiry Card

AC Generators

Brochure 2030-PDL-1168 describes a line of revolving armature a.c. generators. Kato Engineering Co., Mankato, Minn.

Circle No. 319 on Inquiry Card

Miniature Relays

Technical data and prices on a line of miniature industrial relays are contained in a 4 page distributor catalog. Hi-G Industrial Products, A Subsidiary of Hi-G, Inc., Hauppauge, N. Y.

Circle No. 313 on Inquiry Card

Commercial P-C Connectors

This catalog gives detailed specifications and illustrations on "Vikom," commercial printed circuit edge card connectors with bellows contacts. Viking Industries, Inc., Chatsworth, Calif.

Circle No. 311 on Inquiry Card

Pushbutton Thumbwheel Switch

Two pushbutton thumbwheel switches series TIR-27000 and LRT 27000 are illustrated and technically described in a 2-color 2-page bulletin. Chicago Dynamic Industries, Inc., Precision Products Div., Chicago, Ill.

Circle No. 309 on Inquiry Card

Terminal Junctions & Connectors

Three separate, concise catalogs visually itemize lines of terminal junctions, miniature and subminiature connectors and hermetic connectors. The Deutsch Company, Electronic Components Div., Banning, Calif.

Circle No. 325 on Inquiry Card

Reed Switch

Detailed specifications for a full line of magnetic reed switches are given in this 8-page, 2-color catalog. Gordos Corp., Bloomfield, N. J.

Circle No. 321 on Inquiry Card

Graphics Terminal

A System Reference Manual describes the Graphics Terminal, a comprehensive, general-purpose CRT display system. Adage, Inc., Boston, Mass.

Circle No. 303 on Inquiry Card

Relays

This 12 page brochure covers the selection of relays, including information on trade-offs in selection, showing many cost saving practices. Cornell-Dubilier Electronics, Newark, N. J.

Circle No. 301 on Inquiry Card

Digital Tape Memory System

Description, performance characteristics and specifications of the Model TM-Z digital tape memory system, are contained in brochure C087. Ampex Corp., Redwood City, Calif.

Circle No. 314 on Inquiry Card

Logic Cards

A 64-page brochure contains complete technical information on a comprehensive line of thirty-four T²L logic cards, including schematics, specifications, and price list. Wyle Laboratories, Systems Div., El Segundo, Calif.

Circle No. 330 on Inquiry Card

Tape Recorder/Reproducer

A six-page illustrated brochure, Bulletin 1059, details features, specifications and applications for the Alpha 434 magnetic tape instrumentation recorder/reproducer. Midwestern Instruments/Telex, Tulsa, Okla.

Circle No. 307 on Inquiry Card

Pulse Transformers

Engineering bulletin, No. 40351, gives complete design information on Type 55Z DST pulse transformers. Sprague Electric Co., North Adams, Mass.

Circle No. 317 on Inquiry Card

Magnetic Tape Cleaning

This brochure "A Systems Approach to Tape Maintenance." describes an approach to magnetic tape cleaning. Data Devices, Inc., Tarzana, Calif.

Circle No. 310 on Inquiry Card

Computer Peripherals

A short form catalog features a complete line of computer peripherals offered to original equipment manufacturers and others. Burroughs Corp., Los Angeles, Calif.

Circle No. 306 on Inquiry Card

Switches and Indicator Lights

Catalog L-209 provides complete data, drawings and ordering information for 513 Series momentary and alternate action switches and matching indicator lights. Dialight Corp., Brooklyn, N. Y.

Circle No. 324 on Inquiry Card

Digital Indicators

This four page fully illustrated publication describes the CODEX range of digital indicators which present a versatile display concept. Muirhead Instruments Ltd., Stratford, Ontario, Canada.

Circle No. 308 on Inquiry Card

Tubeaxial Fan

The Dolphin, a 265 CFM Tubeaxial Fan which will provide continuous cooling for up to 5 years without maintenance, is the subject of Product Bulletin No. E-3002. Rotron Inc. Woodstock, N. Y.

Circle No. 320 on Inquiry Card

Printed Circuitry

A 12 page brochure on printed circuitry gives a complete review of the facilities and services available at the firm's new plant. Townsend Industries Inc., East Hartford, Conn.

Circle No. 300 on Inquiry Card

RFI Filters

A four-page catalog lists a wide range of filters designed for installation in data processing and related equipment. Hopkins Engineering Co., San Fernando, Calif.

Circle No. 302 on Inquiry Card

Multipurpose Keyboard Display

This brochure summarizes features, characteristics, and specifications of the multipurpose keyboard displays, Models 7550 and 7555. Scientific Data Systems, El Segundo, Calif.

Circle No. 304 on Inquiry Card

Push-Button Switches

A 4-color, 6-page catalog contains illustrations and specifications on five versatile lighted and unlighted pushbutton switches. Molex Products Co., Downers Grove, Ill.

Circle No. 322 on Inquiry Card

Wire-Wrap Connectors

These technical information bulletins feature four standard wire-wrap connectors used in computer, communication, and electronic applications. Sylvania Electric Products Inc., Warren, Pa.

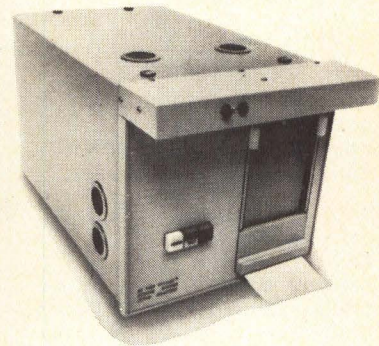
Circle No. 315 on Inquiry Card

Thick Film Photo Arrays

Bulletin HEI-100 describes the advantages, specifications, dimensions, packaging ideas and applications for LA-800 series standard light arrays. Hybrid Electronics, Inc., Chaska, Minn.

Circle No. 331 on Inquiry Card

The Ultra High Speed Printer you can slow down when you need to.



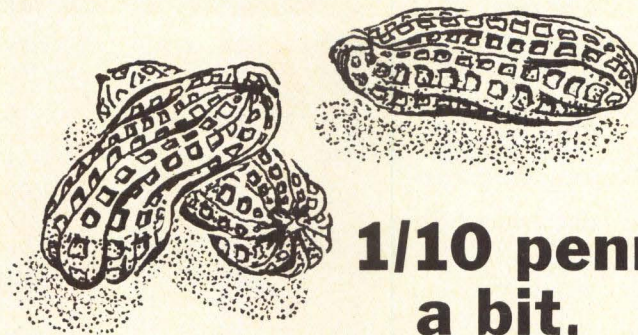
Litton Datalog's MC 4600 prints 6000 lines a minute — and everything in between.

Our MC 4600 offers flexibility as well as speed—anything from 1 to 6000 lines a minute capacity, 32 columns per line. Cathode ray tube with fiber optics achieves this flexibility and speed, as well as assuring reliability, silent operation and an MTBF in excess of 4000 hours.

The MC 4600 has a lot more to

offer: serial input, asynchronous operation, computer compatibility, operation from any digital source. To find out the whole story, call Datalog Division of Litton Industries, 343 Sansome Street, San Francisco, 94104. (415) 397-2813.

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1/10 penny a bit.

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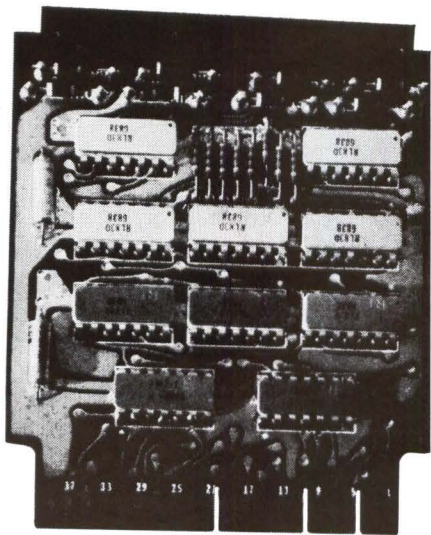
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The MMM10 is just one of a dozen new products in the great digital systems kit for 1969. To get MMM10 specs, price and delivery information, write or call today for Data File DK166. Raytheon Computer, 2700 So. Fairview St., Santa Ana, Calif., 92704. Phone: (714) 546-7160.

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Is your computer ready for memory expansion?

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RCA offers standard off-the-shelf memories with cycle time as fast as 750 nanoseconds and access time of 290 nanoseconds, capacities of 4K x 4 to 32K x 72. We'll quickly work out the "plug-in" compatibility for you, including voltage levels, timing and hardware. Simply let us know what your interfacing requirements are, and we'll take it from there. Or, we'll assist you, if you wish to do

the job yourself.

An RCA Field Representative will be glad to discuss your needs. Or, call or write Marketing Department (617-444-7200, Ext. 233) RCA Memory Products Div., 150 "A" St., Needham Hts., Mass. 02194.

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