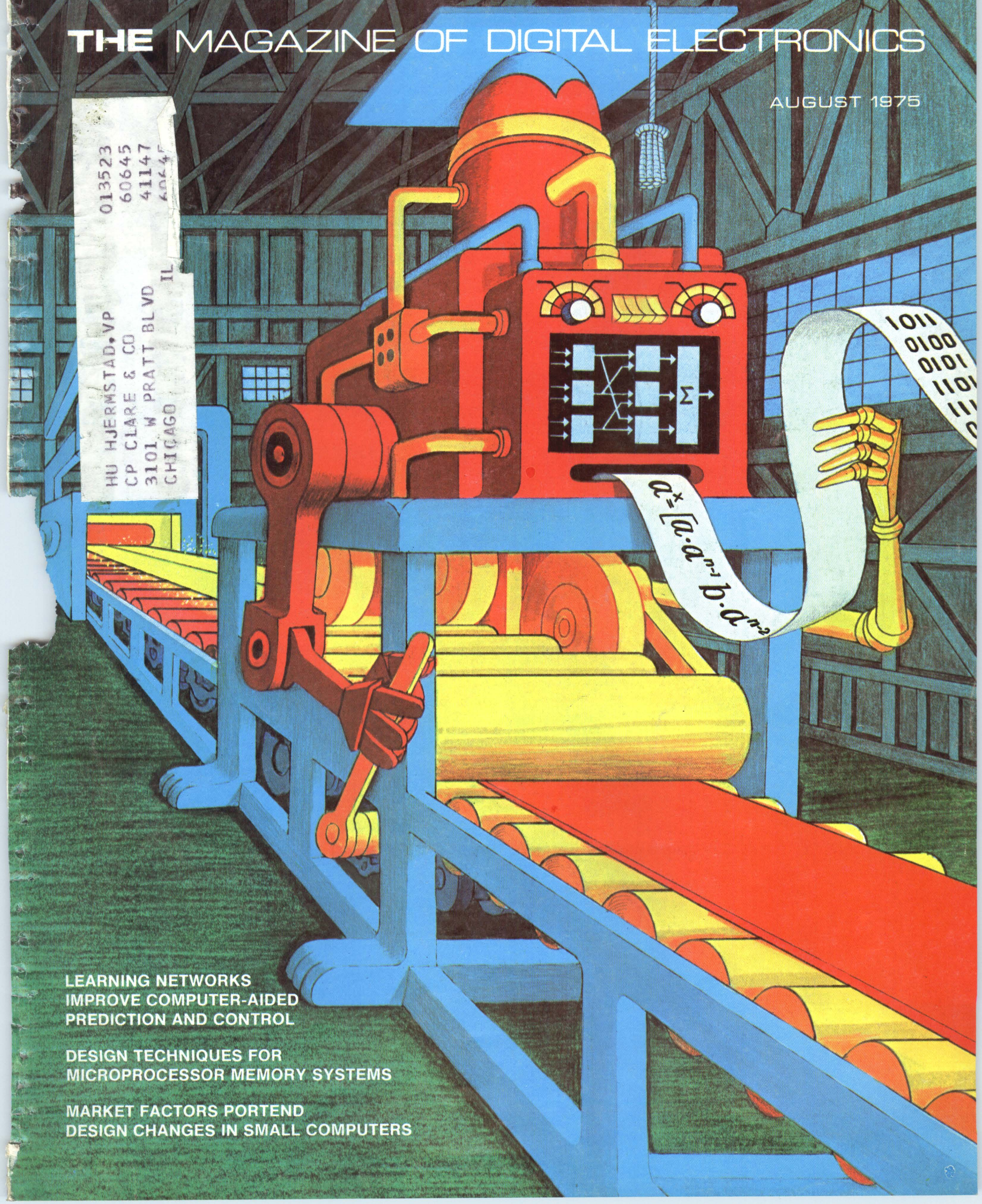
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

AUGUST 1975



LEARNING NETWORKS IMPROVE COMPUTER-AIDED PREDICTION AND CONTROL

DESIGN TECHNIQUES FOR MICROPROCESSOR MEMORY SYSTEMS

MARKET FACTORS PORTEND DESIGN CHANGES IN SMALL COMPUTERS

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Up to 8-channel VFU
Many parallel interfaces
1200 Baud communications

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Multi-part forms to 14⅞"
Up to 8-channel VFU
Printer emulating interfaces
Mini controllers

Model 1120
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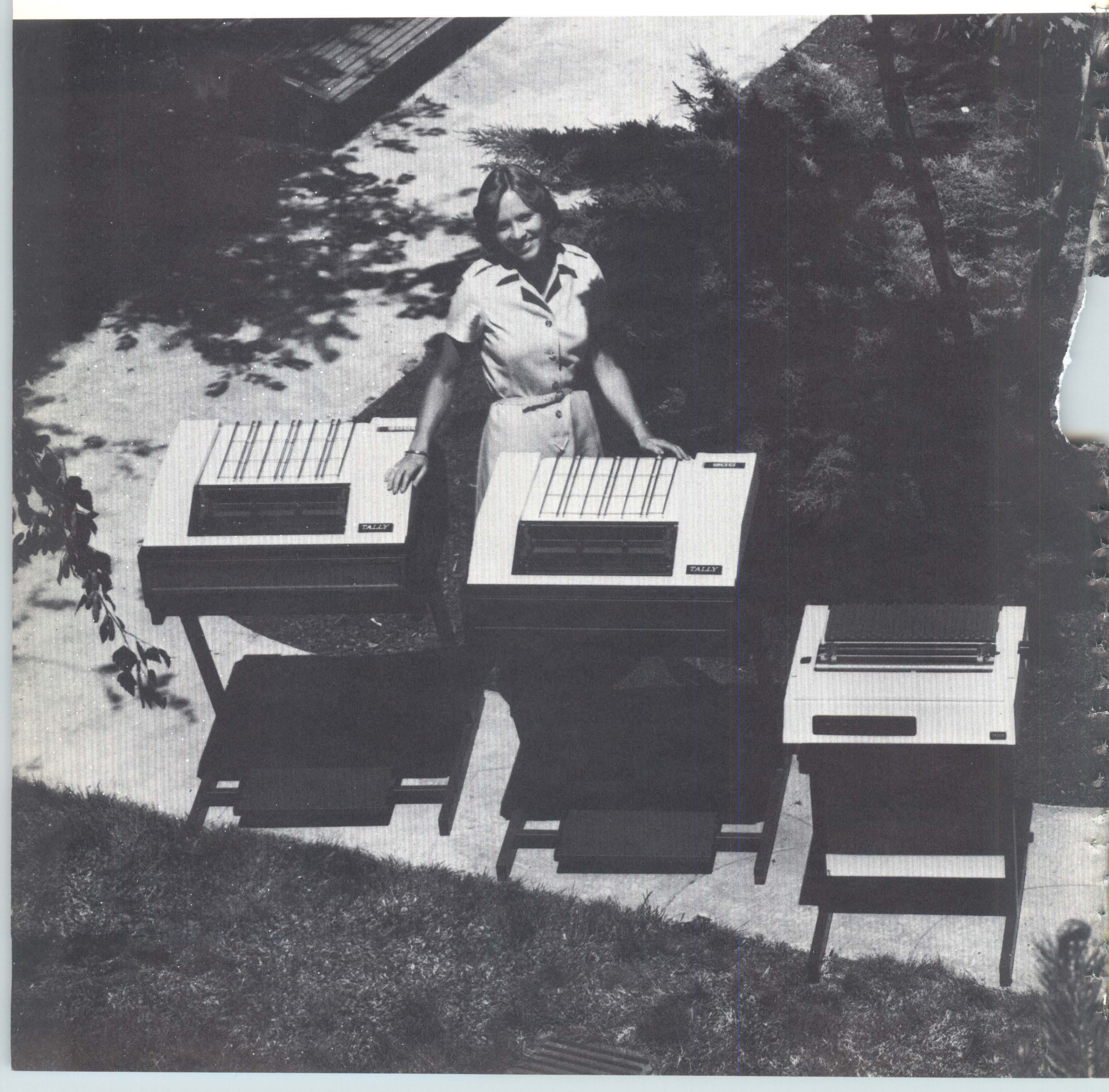
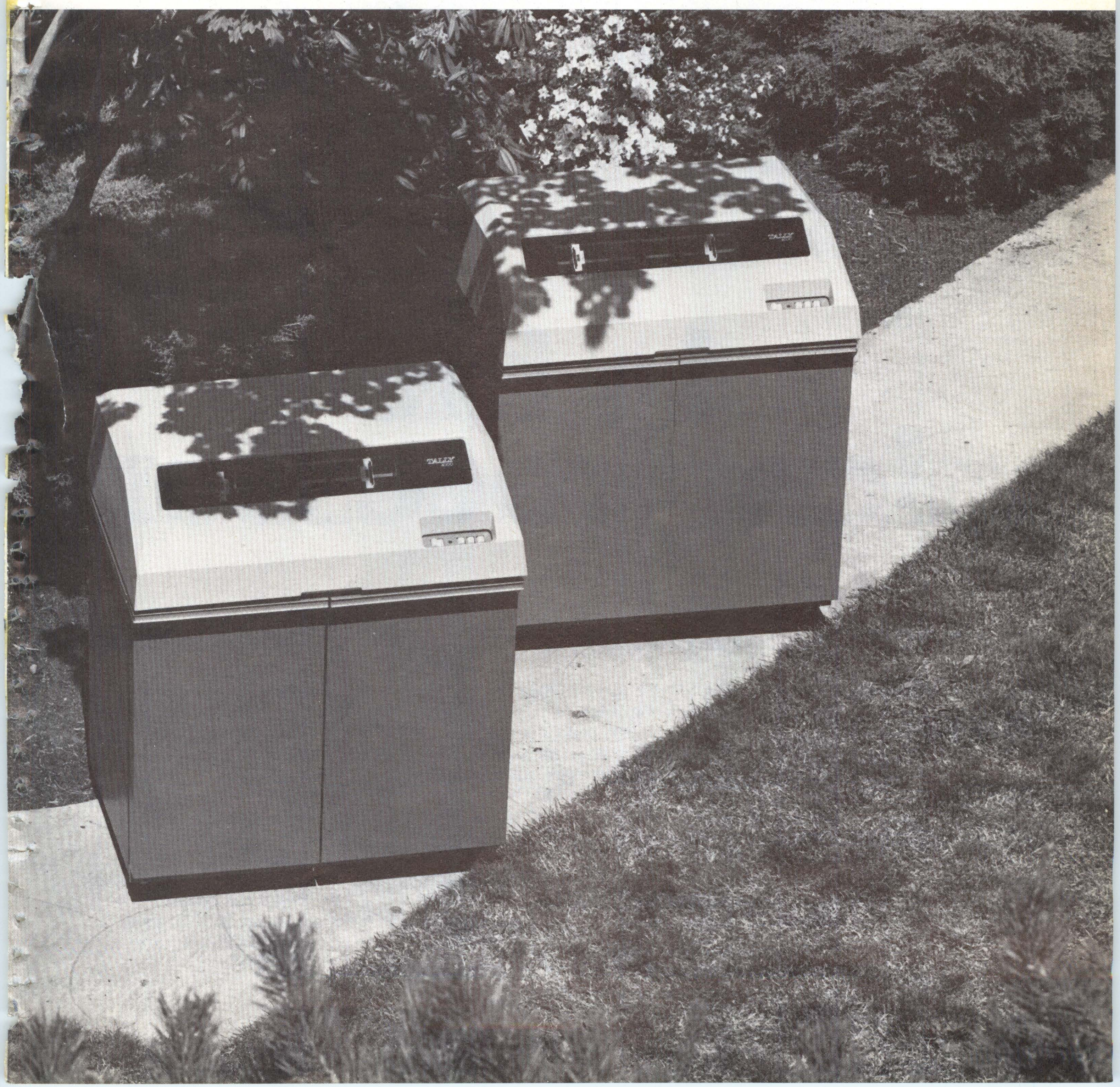
9 x 7 high fidelity print
Multi-part forms to 15"
2-channel VFU
Many parallel interfaces
Asynchronous communications





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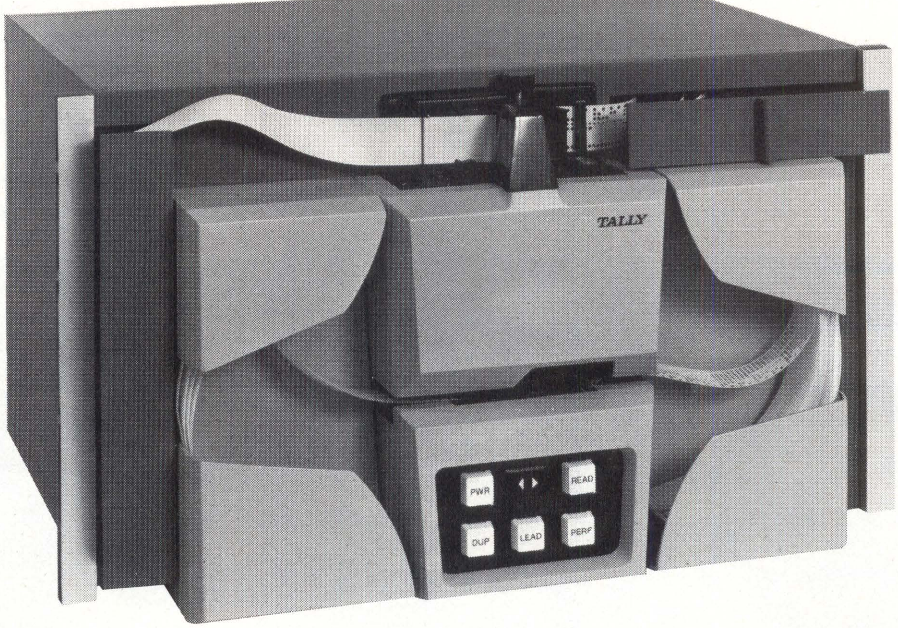

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THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

AUGUST 1975 • VOLUME 14 • NUMBER 8

FEATURES

54 WESTERN ELECTRONIC SHOW AND CONVENTION

Technical/professional presentations of WESCON's Professional Program address the needs, trends, and applications of electronic technology in semiconductor devices, microprocessors, automatic test equipment, and computer peripherals, and consider the effects of the times on capital raising, sales, energy policies, and promoting women

65 LEARNING NETWORKS IMPROVE COMPUTER-AIDED PREDICTION AND CONTROL

by Roger L. Barron

By identifying which variables play significant roles in the behavior of a process and showing how these variables interact with each other in determining what that process will do, the learning network—trainable in both its structure and parameter values—points the way toward improved theory for traditional modeling work

73 DESIGN TECHNIQUES FOR MICROPROCESSOR MEMORY SYSTEMS

by A. Thampy Thomas

Microprocessor system costs can be minimized by mixing memory types to reduce power and cooling requirements, and by using various design techniques to hold down the number of necessary support components

81 MARKET FACTORS PORTEND DESIGN CHANGES IN SMALL COMPUTERS

by Donald R. Wulfinghoff

General design approach of the small-computer industry is being reoriented by emerging factors which are more closely related to the market than to technology

88 RESTORED PROCESSOR FUNCTION SAVES LOGIC AND IMPROVES PERFORMANCE IN MICROCOMPUTER SYSTEM

by David R. Ahlgren

Flexibility of this low cost approach to microcomputer interface design allows a software formatter and controller to provide an incremental read/write capability for program loading or data recording applications

90 FLEXIBLE-CABLE/CONNECTOR SIMPLIFIES PCB WIRING

by John Knudson

Transition from flexible cables to rigid PC boards is eased by use of "U"-contact connectors which also eliminate wiring errors and simplify harness assembly

100 SUBSYSTEMS EASE INTERFACE BETWEEN PARALLEL DIGITAL DATA AND ASCII-COMPATIBLE EQUIPMENT

A family of subsystems-on-a-card simplifies communication between A-D or D-A converters and asynchronous serial teletypewriters and computers

DEPARTMENTS

8 CALENDAR

12 COMMUNICATION CHANNEL

18 DIGITAL TECHNOLOGY REVIEW

30 DEVELOPMENTS

42 DIGITAL CONTROL AND AUTOMATION SYSTEMS

94 MICROPROCESSOR/COMPUTER DATA STACK

102 PRODUCTS

125 LITERATURE

126 GUIDE TO PRODUCT INFORMATION

128 ADVERTISERS' INDEX

Reader Service and Subscription Cards pages 129-132

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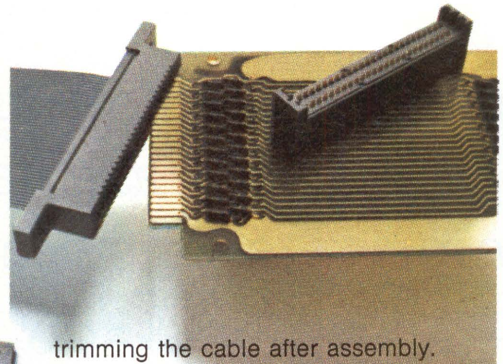
Design with the complete flat cable/connector system.



Assembly-cost savings are built in when you design a package with "Scotchflex" flat cable and connectors. But more important, 3M Company offers you the full reliability of a one-source system: cable *plus* connectors *plus* the inexpensive assembly aids that crimp the connections quickly and securely (with no special operator training required).

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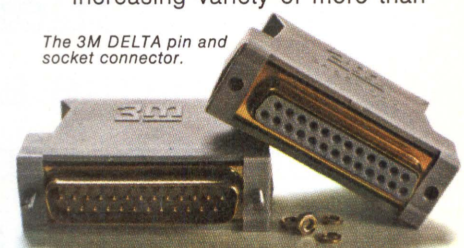
The 3M DELTA pin and socket connector.



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An open letter from electronics and

Mergers and acquisitions, like marriage proposals, fare best when pursued in private. The recent acquisition of Signetics by U.S. Philips Corporation wasn't talked about until it became a fact. Then the announcement naturally prompted a number of questions. We would like to reply to those which have been asked frequently enough to indicate that the answers are of general interest to our friends, customers and vendors.

Sincerely,

Charles C. Harwood

Charles C. Harwood, President
Signetics Corporation

Signetics to the business communities.

(Q) Where does Signetics fit into Philips, anyway?

(A) Signetics is now owned 100% by U.S. Philips Corporation, which is an American company owned by The United States Philips Trust. Consequently, Signetics remains a U.S. corporation. However, it will now benefit fully from the relationship existing between the United States Philips Trust and N.V. Philips Gloeilampenfabrieken, a large public company, active in the manufacture and sales of electronic equipment, electronic components, and other products.

(Q) Will Signetics now be a captive supplier to Philips Europe, Magnavox, or any other Philips interests?

(A) In a word, no. Where appropriate, Signetics will certainly be a normal, competitive supplier to Philips companies around the world. But not as a "captive" supplier, because Signetics' aim is to serve the world market as a component supplier.

(Q) Will Signetics be part of North American Philips and perhaps use the North American Philips sales force?

(A) No. Signetics is completely separate and will operate with its own selling organization.

(Q) Will Philips change top management?

(A) Philips does not plan to, and Signetics' management has committed to remain, and continue functioning in key positions.

(Q) What is Signetics' financial position?

(A) Despite the economic downturn which has affected its profit and loss, Signetics is in a positive cash flow position. Inventories are in solid shape, and we have unused credit lines. We are well-positioned financially, poised for the upturn in business.

(Q) Will Philips be infusing capital into Signetics?

(A) Capital will be invested as needed to meet our primary world-wide growth objectives from sources as will be available and required for a sound financial structure.

(Q) Will Signetics supply the international markets now?

(A) Yes, but keep in mind we are talking about a continuing operation — Signetics is already supplying the international markets. In fact, we intend to increase sales and services world-wide by also using the N.V. Philips sales and marketing organizations outside the United States.

(Q) Will Signetics customers see many changes now, due to Philips?

(A) Many changes, yes, but not due primarily to Philips. Signetics has been continually developing a variety of new products and technologies — many recent achievements will come on the market very soon: such as the #2650 microprocessor and the #2604, the 4096-bit Random Access Memory. Signetics' sales force is currently being strengthened, but this is in accordance with previously determined plans. Expanded marketing tools, advertising programs, internal changes to improve service to customers and prospects — all these are underway now. Of course, Signetics anticipates a significant plus through Philips' technological contributions and basic research.

(Q) Will there be changes in Signetics' price structure for products?

(A) Certainly not because of the acquisition. Signetics' growth, which has been quite substantial, has resulted from a combination of technology, quality, service, and competitive pricing. Neither Signetics nor Philips foresees any departure from the effort to keep improving in all four areas.

(Q) How will Philips help Signetics?

(A) Philips has a long and intimate understanding of the semiconductor business. They have done an immense amount of research and development in semiconductor devices. Signetics will benefit from this historical work, as well as all future inventions and technological breakthroughs — just as Philips will benefit from Signetics.

signetics

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CALENDAR

CONFERENCES

Sept 3-5—Computer Hardware Description Languages & Their Applications, City U of New York. **Information:** Prof Stephen Y. H. Su, Workshop Chrmn, Dept of EE, The City College, City U of New York, New York, NY 10031. Tel: (212) 690-5392

Sept 9-11—Hybrid Microelectronics Conf, Loughborough U of Technology. **Information:** Conf Dept, IERE, 9 Bedford Sq, London WCIB 3RG, England

Sept 9-11—COMPCON 75 Fall: IEEE Computer Soc Conf, Mayflower Hotel, Washington, DC. **Information:** Gen'l Chrmn, Dr Richard E. Merwin, Army BMD Prog Office, 1300 Wilson Blvd, Arlington, VA 22209. Tel: (202) 694-5282

Sept 11-12—Nat'l Bureau of Stds 1st Nat'l Conf on Software Engineering (immediately following COMPCON), Mayflower Hotel, Washington, DC. **Information:** Software Engineering, PO Box 639, Silver Spring, MD 20901

Sept 16-19—WESCON: Western Electronic Show & Conv, Brooks Hall/Civic Audit, San Francisco. **Information:** Don Larson, WESCON Gen'l Mgr, 3600 Wilshire Blvd, Los Angeles, CA 90010. Tel: (213) 381-2871

Sept 17-19—ASME Design Automation Conf, Statler-Hilton Hotel, Washington, DC. **Information:** Paul Drummond, Meetings Dept, Amer Soc of Mechanical Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Sept 22-23—MICRO 8: ACM SIGMICRO/IEEE Computer Soc 8th Annual Workshop on Microprogramming, Palmer House, Chicago. **Information:** Conf Chrmn, William Lidinsky, Argonne Nat'l Labs, Applied Math Div, 9700 S Cass Ave, Argonne, IL 60439

Sept 23-25—2nd EUROCOMP (European Computer Conf), Heathrow Hotel, London Airport. **Information:** Online, Brunel U, Uxbridge, Middlesex, England

Sept 23-25—IEEE Cybernetics & Society Internat'l Conf, Hyatt Regency Hotel, San Francisco. **Information:** L. S. Coles, Artificial Intelligence Ctr, Menlo Park, CA 94025

Sept 29-Oct 1—Electronic & Aerospace Systems Conv (EASCON), Stouffer's Nat'l Center Inn, Washington, DC. **Information:** IEEE, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Sept 29-Oct 2—IEEE Canadian Region Internat'l Electrical/Electronics Conf & Exhibition, Automotive Bldg, Exposition Park, Toronto. **Information:** T. W. Purdy, 237 Parkview Ave, Willowdale, Ontario, Canada

Oct 1-3—3rd Internat'l Industrial Electronics Congress, Torino. **Information:** Chrmn Exec Comm, Dr Ing Giovanni Villa, Corso Massimo d'Azeglio 15, 10126, Torino, Italy

Oct 6-8—NCF/NEC: Nat'l Communications Forum/Nat'l Electronics Conf, Hyatt Regency O'Hare, Chicago. **Information:** NEC, Suite 103, 1301 W 22nd St, Oak Brook, IL 60521. Tel: (312) 325-5700

Oct 6-9—ISA-75: Instrument Soc of America Conf & Exhibit, Mecca Hall, Milwaukee, Wis. **Information:** ISA, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

Oct 7-8—9th Annual Instrumentation & Computer Fair, Sheraton Inn/Washington-Northeast, Washington, DC. **Information:** Robert Harar, Exec Dir, Instrumentation Fair, Inc, 5012 Herzel Pl, Beltsville, MD 20705. Tel: (301) 937-7177

Oct 7-9—IEEE Computer Soc 4th Data Communications Sym, Hotel Le Concorde, Quebec City, Quebec. **Information:** Dr Tom B. Grandy, Bell-Northern Research, PO Box 3511, Station C, Ottawa, Ontario, Canada K1Y 4H7

Oct 7-9—IEEE Internat'l Sym on Electromagnetic Compatibility, El Tropicano Hotel, San Antonio. **Information:** EMC, PO Drawer 28510, San Antonio, TX 72284

Oct 13-14—Information Processing Assoc of Israel (IPA) 10th Nat'l Data Processing Conf, Binyanei, Ha'ooma, Jerusalem. **Information:** NDPC, c/o Kenes Ltd, PO Box 16271, Tel Aviv, Israel

Oct 13-15—16th Annual Sym on Foundations of Computer Science, Berkeley, Calif. **Information:** Sheldon B. Akers, General Electric Co, Bldg 3, Rm 223, Electronics Park, Syracuse, NY 13210. Tel: (315) 456-3067

Oct 14-16—IEEE Internat'l Conf on Advanced Signal Processing Technology, Lausanne. **Information:** Secretariat "Journées d'Electronique," Ch de Bellerive 16, 1007 Lausanne, Switzerland

Oct 20-22—Internat'l Security Conf, New York Hilton Hotel, New York City. **Information:** ISC, 2639 S La Cienega Blvd, Los Angeles, CA 90034. Tel: (213) 836-5000

Oct 22-23—8th Annual Connector Sym, Cherry Hill. **Information:** Electronic Connector Study Group, PO Box 1428, Camden, NJ 08101

Nov 11-14—12th Electrical/Electronics Insulation Conf, Sheraton Boston Hotel/Hynes Audit, Boston, Mass. **Information:** E/EIC, PO Box 159, 700 Peterson Rd, Libertyville, IL 60048

Nov 19-20—IEEE Computer Soc Sym on Computer Arithmetic, Dallas, Tex. **Information:** Prof D. E. Atkins, Dept of Elec & Comp Eng, U of Michigan, Ann Arbor, MI 48104. Tel: (313) 763-0038

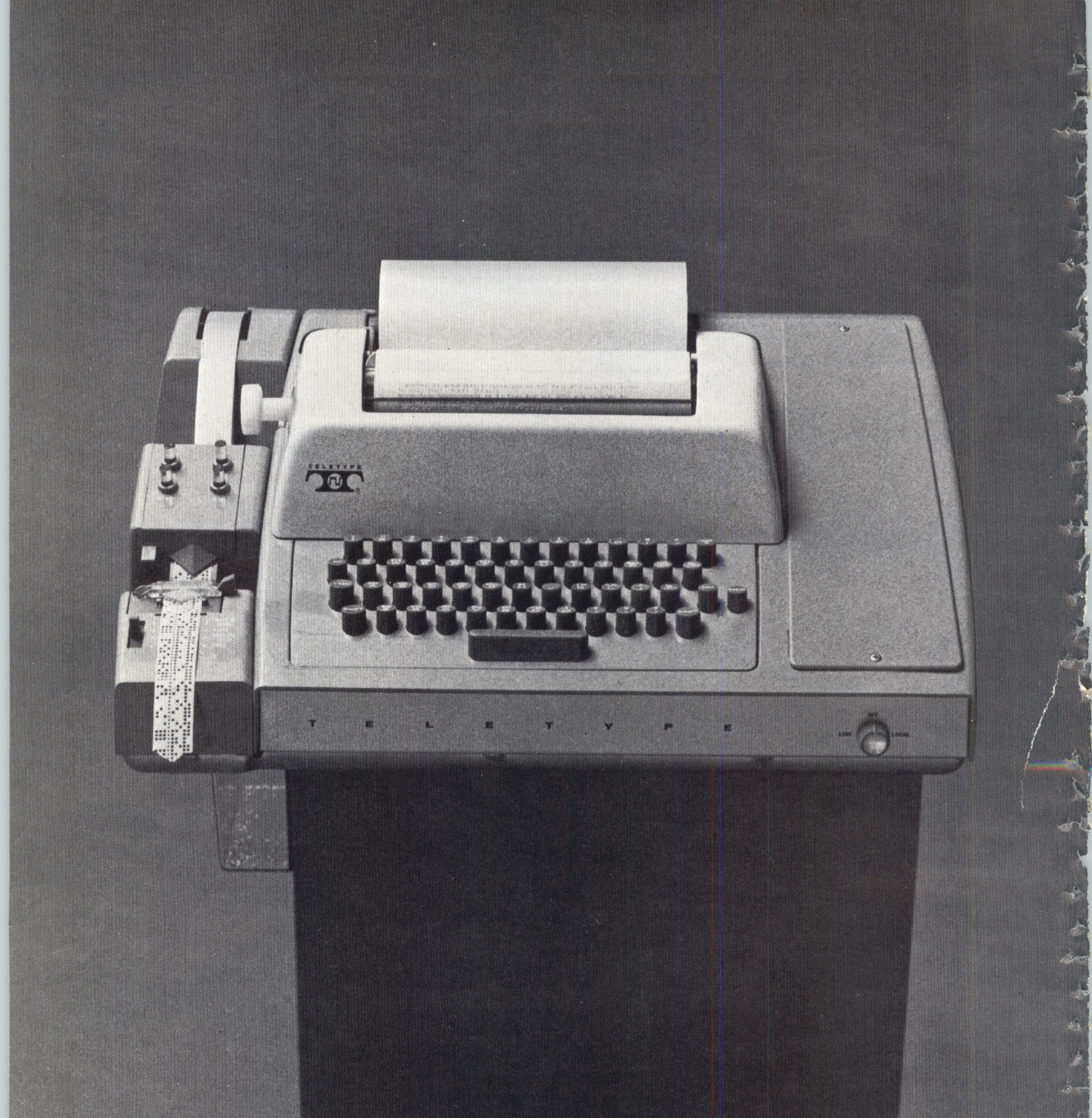
SEMINARS

Sept 8-10 (Los Angeles), **Sept 29-Oct 1** (Chicago), **Oct 6-8** (Boston), **Oct 14-16** (New York City)—Planning/Designing Distributed Data Processing Systems for (IBM Protocol) SDLC and (Systems Network Architecture Teleprocessing Package) SNA. **Information:** Saroj K. Kar, Telecom Computer Technology, 599 N Mathilda Ave, Sunnyvale, CA 94086. Tel: (408) 735-9990

SHORT COURSES

Sept 1-5, Dec 7-12—Digital Electronics for Automation & Instrumentation; **Sept 14-19, Dec 14-19**—Microprocessors & Minicomputers: Interfacing & Applications, Virginia Polytechnic Inst & State U, Blacksburg. **Information:** Amer Chemical Soc, Education Div, 1155 16th St, NW, Washington, DC 20036. Tel: (202) 872-4508

Sept 30-Oct 2—Microprocessors; **Oct 7-9**—Electronic Display: Technologies & Applications; **Oct 29-31**—Monte Carlo Simulation Methodology, George Washington U. **Information:** Director, Cont Eng Ed, George Washington U, Washington, DC 20052. Tel: (202) 676-6106


TELETYPE
T E L E T Y P E

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Leased Communications Services

The June 1975 column examined the recent changes made and alternatives offered with regard to switched communications facilities (toll, WATS, and so on). These tariff rate and policy alterations directly impact the information system designer whose objective is a low-cost yet maximum-throughput communications network. If a system's planning and design decisions today were based solely on the switched communications tariffs of one year ago, a high probability exists that that objective would not be achieved.

In examining similar concerns for presently available leased line services, the system designer will find an even greater degree and scope of changes undergone during the past year. Not only have the traditional services been drastically redefined, but entirely new leased communications services have been introduced. Also occurring in leased services is that the developing offerings of specialized common carriers are being marketed to compete with the traditional common carriers. This considerably more dynamic area, exhibiting more diversification as well as a greater choice of competing vendors, is also the more popular type of information system-related communications service; the leased network is more widely used with computer communications systems than is a switched or dial network.

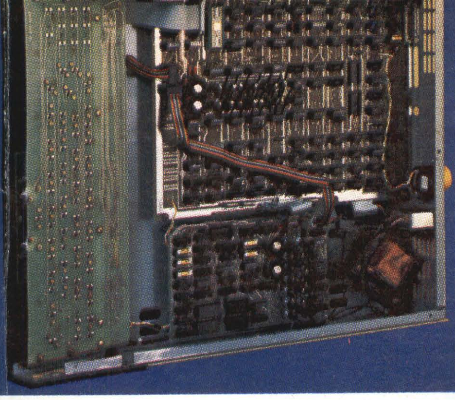
This month we explore the present status and relative application of the various leased line or leased communications facilities available to system designers. This should not be viewed as static or a final status, however; it is quite reasonable to assume that present offerings and suppliers will continue to undergo a greater frequency and scope of change, particularly as competitive factors continue to interact in a growing and more knowledgeable market.

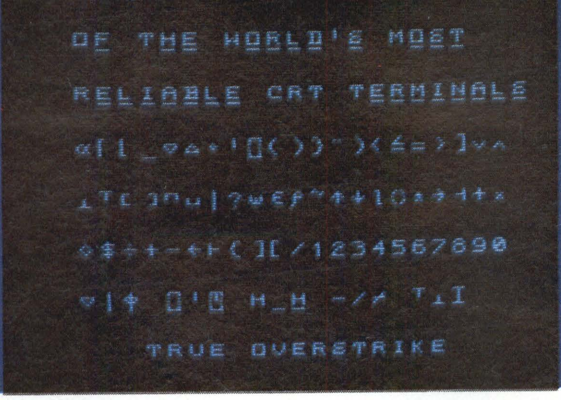
A leased communications service can be basically defined as a communications channel that is provided on essentially a full-time basis to interconnect specified geographical locations. Typically, the channel is priced on the basis of actual distance, and capacity as either a function of a bandwidth or digital sampling rate. Monthly charge is based on a provided capability—independent of actual usage, whereas a switched service is priced on a per-connection or -usage basis—not exclusively on potential usage.

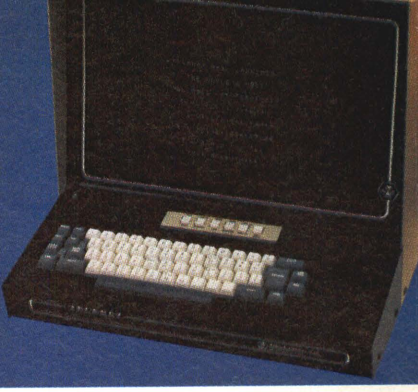
From an operational reliability aspect, there is a major distinction between leased and switched services. Equating operational reliability with computer center accessibility, switched services provide virtually infinite backup. If a switched channel should malfunction or degrade, operating personnel can easily disconnect and dial a new channel. Assuming that system data flow procedures and protocol permit such a recovery, accessibility to the center is easily re-established.

If a leased service should fail to operate properly, however, no easily implemented alternative exists which can be activated to maintain optimum accessibility. Normal practice requires that the user of such a channel suspend all data communications activity until common carrier personnel have tested for and hopefully found and corrected the problem. It is quite common to experience extensive periods of suspension, only to have the common carrier personnel declare that the channel in question meets their acceptance specification and that the source of the problem lies somewhere else in the system. If a second leased channel is continually available and paid for, computer center access could possibly be maintained during these prolonged periods; but unless such extraordinary steps to provide backup access are taken, a leased-channel network implies total dependency.

At present, a number of leased communications channel vendors are







The "Fewer Belly Aches" CRT Goes APL

Here's the newest addition to the growing TELERAY family of "gutless wonders" . . . the Series 3900 . . . following in the same tradition that produced the Series 3300 TTY replacement and the full-ASCII Series 3700 with single-logic-board, plug-in-chip simplicity.

The 3900 is really three terminals in one—APL, full ASCII, and upper-case TTY. Its display clarity is unusually sharp—the result of several interacting features: a high resolution monitor, 15-inch CRT, and TELERAY's switchable wide-character format (over ¼ inch high and wide).

The 3900 displays TRUE APL overstrike characters, with ASCII mode overstrike optional. It operates scroll-up, with bottom-line data entry and bottom-line cursor controls. And, except for the bell tone, it gives you totally quiet operation—no fan.

Best of all, it is priced lower by far than any APL terminal in the world . . . like under $2500—for one.

Standard Features:

- APL/ASCII Typewriter-Pairing Keyboard
- APL and Full-ASCII Character Sets—Computer Switchable
- True APL Overstrike and Underlining
- 15-Inch, High-Resolution CRT
- 1920 Characters (24 x 80)
- Wide Character Format (24 x 40), Switchable
- Asynchronous, Character-Oriented Transmission
- Dual Data Rates, to 9600 Baud
- All Standard Interfaces—RS-232, Current Loop and TTL

Optional Features:

- Printer Output—RS-232 Serial and Parallel TTL and Current Loop
- Composite Video Output
- Numeric Keypad
- Detachable Keyboard and Receive-Only Models
- ASCII Mode Overstrike
- 50 Hz Power Package

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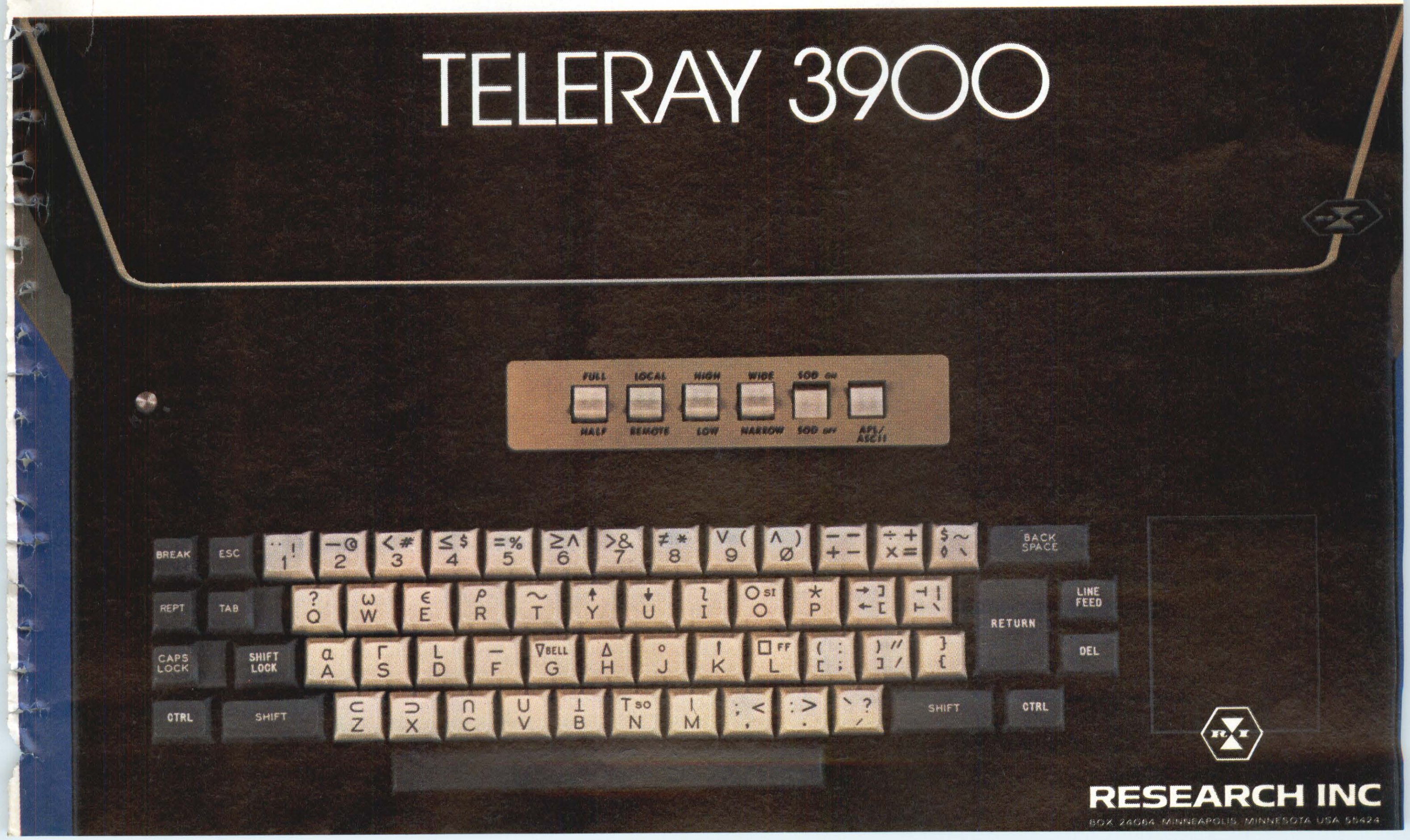


marketing facilities throughout the U. S. It is important to note that all of these vendors are basically capable of providing the defined services. All are regulated carriers and therefore subject to policies and rates they have written in their approved tariffs.

Occasionally, the traditional-common-carrier salesman, when critiquing his competition, might attempt to create the impression of their technical incompetence or minimal-resource capability; such statements are totally unfounded. All are capable of providing and maintaining their stated services; all have examples of others failing to always provide maximum service. The final decision point for leased-channel selection is primarily one of economics. It should be noted, however, that specialized common carriers are typically limited to defined geographical areas, while the traditional carriers have a considerably wider area of coverage.

With respect to interstate leased channels, the traditional common carriers are American Telephone & Telegraph (AT&T) and Western Union, while specialized common carriers are typically represented by MCI Telecommunications Corp, Southern Pacific Communications Co (SPCC), and Data Transmission Co (Datran). In addition, RCA Global Communications, Inc and American Satellite Corp market satellite-derived leased communications channels in selected geographical areas.

These channels are primarily analog facilities, so that for data communications, a modem must be used to convert digital signals to analog representations. Exceptions to this total analog environment are AT&T's Dataphone Digital Service and Datran's digital facilities.

Table 1 compares analog offerings currently available to the data communications system designer. MCI and SPCC have a uniform rate for the geographic areas they serve. AT&T and Western Union, however, divide their total service areas into high and low density cities or locations. If a leased channel runs between two high-density locations, high-density rates apply; if either or both cities are designated low, the low-density rates are used. AT&T has designated as high density 320 locations; Western Union, 70. Table 1 rates assume a type 3002, 2-wire equivalent channel; if a 4-wire channel were required, total AT&T and Western Union charges would increase by 10%, while with MCI and SPCC, only channel termination charges would increase (by 100%).

TABLE 1
Leased Analog Channels

Vendor	Channel Mileage Cost (per mile per month)	Channel Termination (per month)	Local Line (per month)
AT&T			
High density	$ .85	$35.00	$25.00
Low density	2.50	15.00	15.00
Western Union			
High density	.75	50.00	25.00
Low density	1.00	50.00	25.00
MCI	.75	77.40	12.50
SPCC	.69	65.00	32.00

TABLE 2
Leased Digital Channels

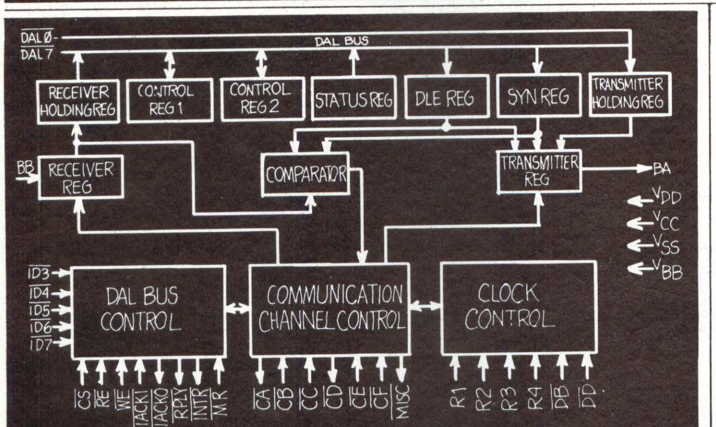
Vendor	Rate Bits/s	Channel Mileage Cost (per mile per month)	Channel Termination (per month)	Local Line (per month)
AT&T	2400	$.40	$10.00	$80.00
	4800	.60	20.00	100.00
	9600	.90	30.00	125.00
	56,000	4.00	62.50	220.00
Datran	2400	.75	80.00	70.00
	4800	.75	130.00	70.00
	9600	.90	180.00	70.00

Assuming a 200-mile, 2-wire, point-to-point channel between high-density locations, the following monthly costs would be incurred: AT&T, $310; MCI, $330; SPCC, $332; and Western Union, $300. If one point to be connected were designated low density, AT&T's monthly price would increase to $600, Western Union's to $350; those of MCI and SPCC would not change.

Even in a total high-density environment, ability of a data communications application to schedule its transmission times could permit use of leased channels on a part-time or metered basis. MCI and SPCC offer such services at discounted rates; AT&T and Western Union provide leased voice-grade channels on a full-time or full-period basis only. Depending on the points to be interconnected and flexibility of the application and associated terminal and central processor configurations, a part-time service might provide dramatic cost-savings.

The advent of digital transmission facilities offers unique cost and re-

Thanks to our bright engineers, we may have just cut our datacom chip sales in half.



THIS IS HOW ASTRO™ WORKS

They Made a Universal Interface Chip. Now We're Selling One Chip Instead of Two.

Everyone thought our MOS/LSI UART's were great. Then our engineers thought it would be nice if we also came out with two synchronous/asynchronous devices. One (SAT) was a transmitter; the other (SAR), a receiver.

But people kept telling them two chips were too much trouble. There had to be an easier, more flexible way. We said it couldn't be that difficult to get computers and terminals to talk to each other. They said it was.

So at great expense our brilliant crew produced an Asynchronous/Synchronous Transmitter/Receiver and cleverly named it ASTRO (UC1671).

Of course, while they were at it, they threw in a few more previously expensive goodies. They gave it full duplex capabilities so nothing had to wait.

After spending all this time to create it, they gave it IBM bisynch compatibility and transparent mode capability so you wouldn't see it anyway.

Details They Said You'd Like

ASTRO had to talk with computers. So they gave it a bus-oriented architecture. They fixed it so 32 ASTRO's could be addressed on bus and gave it a simplified interrupt and priority structure. So the processor wouldn't be slowed down, ASTRO was double buffered. And to top it off, ASTRO can operate at 1 Megahertz. Both modes have selectable 5-8 bit characters. Asynchronous mode allows 1, 1-1/2, or 2-stop bit selection. There are eight selectable clock rates, with up to 40% distortion allowance with 32X clock. Of course, all inputs and outputs are TTL compatible. It's all done using n-channel technology and comes in a 40-pin package.

Actually, It Was All Rather Cunning.

To tell the truth, we are well aware of the fact that not everyone will use an ASTRO to replace a UART, SAR, or SAT. Sometimes, they are all you'll need. And we recognize that ASTRO will take away business from the competition.

But that's how the high cost of technical leadership pays off. The denser the chip, the more problems you can help solve.

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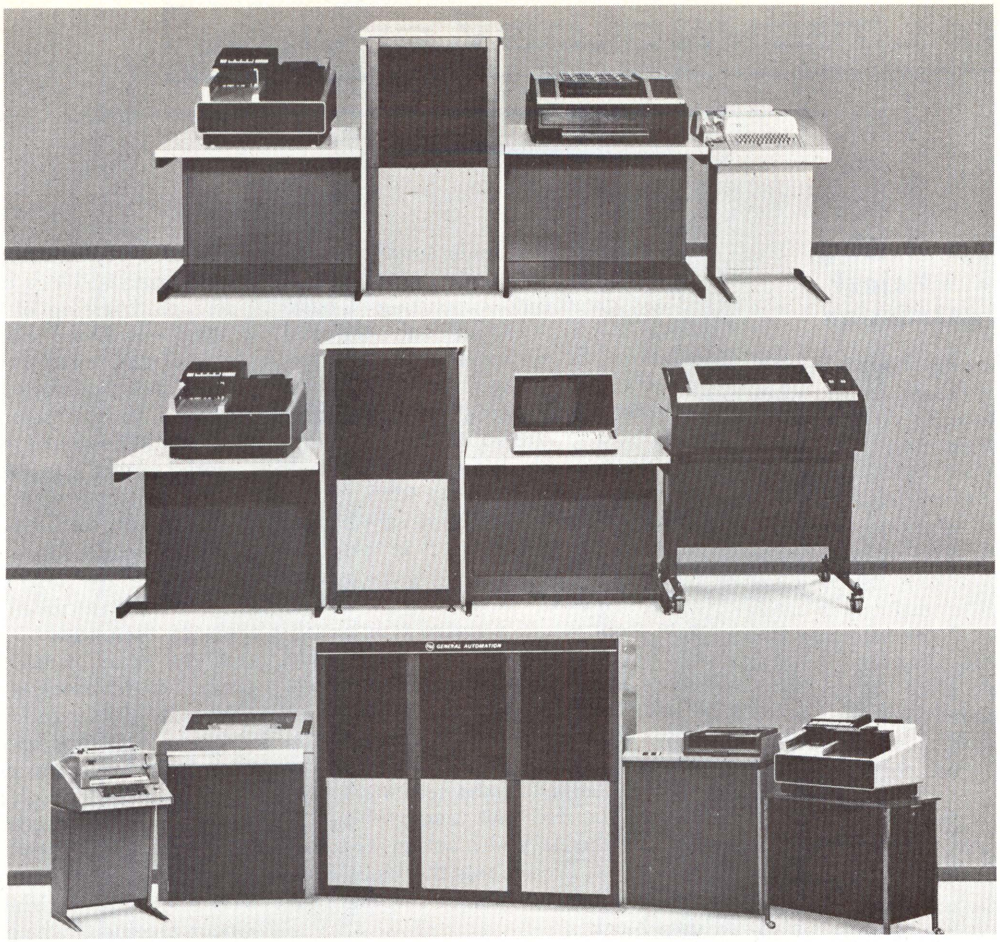
liability advantages to the data communications user. As shown in Table 2, both AT&T and Datran have announced such offerings. Considering the same 200-mile, point-to-point application for communication at 4800 bits/s, monthly costs would be $360 for AT&T, $550 for Datran.

Using digital transmission facilities, the user can avoid the additional monthly cost of renting a 4800-bit/s modem for each location. It should also be noted that the facilities are 4-wire, which can enhance data transmission throughput significantly.

Current availability of satellite-derived channels is typically for long-distance, continental networks. RCA presently provides only a domestic satellite-derived channel between New York City and either San Francisco or Los Angeles. American Satellite provides service among Chicago, Dallas, Los Angeles, San Francisco, New York City, and Washington, DC. Monthly rate for a leased continental channel from either RCA or American Satellite is $1000 (between New York City and San Francisco), plus $70 per each channel end for termination and local line. A similar analog channel from AT&T and Western Union HI-LO Tariffs would cost more than $2200 and $2000/month, respectively.

As cautioned earlier, a constant awareness of the continuing dynamics of this important area must be maintained. Due primarily to the competitiveness of the regulated vendors of leased channels, the data communications user must expect continual changes in both rates and policies, and, to assure maintenance of optimum network value, a system must be designed to accommodate such changes. Rigid network alignments, protocol, or operational disciplines can only lock a user into a less than optimum network. In the extreme, it is also quite possible that an inflexible system requirement for a fixed network configuration and operation may be rendered obsolete by a tariff or service alteration. Primary criterion in network design consideration is provision for maximum flexibility. In addition, system designers and, ultimately, users are obligated to monitor and track this rapidly changing environment. To fail to do so can result in system disaster. □



ONLY ALL OF THE ABOVE CAN OFFER ALL OF THE BELOW:

General Automation's new family of low-cost, expandable remote batch terminals offer more capabilities than any competitive systems produced by any terminal or minicomputer manufacturer anywhere.

Here's what we mean by *capabilities:*

Talk to any computer.

Our software emulator packages make our terminals multi-lingual. They can talk to IBM 360/370 HASP or 2780 work stations. They'll also emulate a Control Data User Terminal. Or a UNIVAC 1004 system.

Data spooling included.

Our disk-based emulator packages have data spooling. Which saves you transmission time. Which saves you money.

More operating systems.

Most RBTs have one or two operating systems. Ours have three. Including Free Standing (FSOS), Disk-Based (DBOS) and Real Time (RTOS) operating systems.

Name your configuration.

We can provide any hardware configuration, including any kind of peripheral equipment you could ask for. Our RBT family consists of three basic communications systems (base prices range from $19,500 to $30,000):

RBT-1 is an intelligent batch communications terminal used for entering, transmitting and receiving data between a remote location and a central computer.

RBT-2 combines communications terminal capabilities with a batch-oriented satellite data processing system.

RBT-3 is a complete communications system plus multi-programming-oriented stand-alone data processing system offering concurrent batch and real-time operations.

Communicate with an expert.

General Automation didn't get into the communications business yesterday. We are already the major supplier of minicomputer systems for front end processors, distributed data systems, Telex message switching systems and PABX control systems for the world's largest international communications companies. We're also the number one solver of tough communications problems in more than a dozen different industries.

We provide virtually everything you need to build or expand a data communications system. We can show you the best ways to get the most out of your communications dollar.

Give us a call at (714) 778-4800. Or write to one of the addresses below.

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CIRCLE 13 ON INQUIRY CARD

Selective-Repeat ARQ Allows 92% Efficient Satellite Transmission

Because the stop-and-wait error-checking protocols that are used when transmitting data over satellite channels currently offer only about 50% efficiency at speeds of 4800 bits/s and above, the lower circuit costs of satellite transmission have not yet outweighed the disadvantages of its lower throughput. Eliminating the long delays that reduce the efficiency of satellite channels, the 7400 Selective Repeat/Automatic Repeat Request (ARQ) transmits data blocks in a steady stream, increasing efficiency to 92%, and making the channels performance competitive with terrestrial systems.

Efficiency of satellite channels is degarded by the 600- to 800-ns round-trip delays that occur when the transmitter awaits individual response from the receiver to signify receipt of an error-free data block. These delays amount to only about 40 ms on terrestrial links.

The ARQ system technique, developed by Codex Corp, 15 Riverdale Ave, Newton, MA 02195, overcomes these delays by maintaining several blocks in the air on the outbound link at any given time. Consisting of basic error control system and terminal adapter, the system replaces the terminal's stop-and-wait technique with a system for transmitting data blocks in a steady stream, without waiting for an individual response on each block from the receiving terminal.

As each block in the stream arrives at the receive modem, it is taken by the ARQ's basic error control system (BECS) where it is checked for errors; if it is correct, it is stored temporarily in the receiving BECS's memory, and an ACK is sent back over the reverse channel to the BECS at the transmit end. The block is then given to the terminal adapter, which gives it to the terminal, utilizing the terminal's protocol. The transmit BECS, which is holding the ACKed block in its transmit queue, then erases the block from memory to make room for the next data block.

If a received block is incorrect, the receive BECS sends a NAK, but continues to accept and store subsequent correct blocks coming in from the transmit end. The transmit BECS then retrieves the NAKed block from memory and retransmits it, sandwiching the corrected block between the uninterrupted stream of new data blocks going out. Once the block is retransmitted and correctly ACKed, the correct block is ordered in its proper sequence in the remote BECS receive queue. When reconstructed, the set of stored blocks is released to the receiving data terminal in the same order in which they were transmitted.

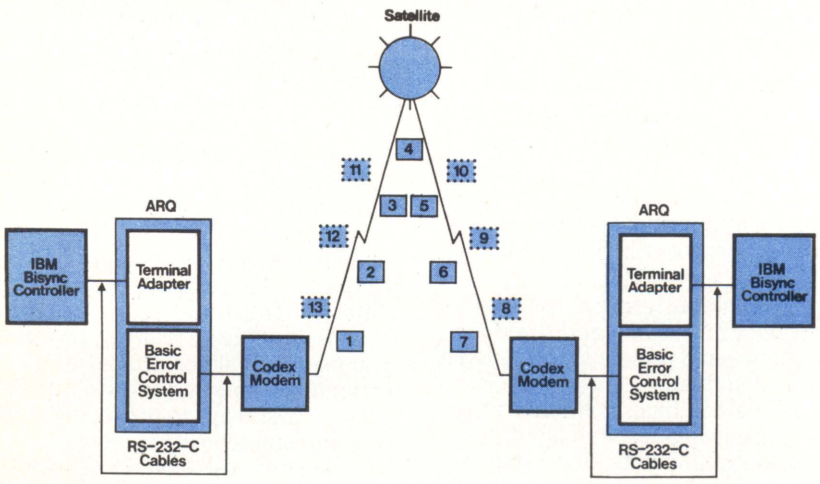
Completely transparent to user's block size, the ARQ clocks user blocks out of the terminal in 475-bit segments, then adds 37 bits of operational and error control data. The fixed-size, 512-bit block is then used as the internal block size in the error control system, allowing hardware to remain unaffected by the user's block size and to maintain high throughput when high error rates occur on a degrading channel. An effective throughput rate of 92% is obtainable on low error rate channels (10^{-6}), while throughput on poor channels, which have high error rates (10^{-4}), can be maintained 57% higher than with stop-and-wait techniques on an error-free channel.

Developed to use IBM binary synchronous protocols, full or half duplex, in its present configuration, the ARQ terminal adapter works only with that protocol. However, since the terminal adapter is the key element in implementing the selective repeat technology into a commercial system, provision is made to adapt the basic error control system to other terminal protocols by implementing the specific protocol on a plug-in module, which is interfaced to the terminal.

If no protocol is involved and the terminal is feeding a straight bit stream, such as facsimile or torn-tape systems, no adapter is needed; data can go directly to the transmit BECS. The ARQ is speed insensitive, accepting the modem's data clock at any speed up to 9600 bits/s, and supplying it to the terminal.

Indicators and counters incorporated on the enclosure allow users to monitor performance with online data without interrupting transmission. A bit error rate tester is manually activated at receive and transmit ends, putting out a known block pattern to permit the user to measure the bit error rate using a counter on the panel.

Circle 150 on Inquiry Card



Making satellite communications performance-competitive with terrestrial systems, Codex's 7400 Selective Repeat ARQ transmits data blocks in a steady stream, eliminating the normal stop-and-wait path delay of current error-checking protocols. Designed for use with IBM bisync techniques, the system, consisting of error control system and terminal adapter, is transparent to the circuit, requiring no hardware or software changes to transmit via satellite

Powerful and Friendly.

The Hewlett-Packard RTE-III operating system.

Check it out.

1. ✓ Up to 256K words of CPU RAM memory, providing lots of room for expansion.
2. ✓ Up to 64 mapped partitions, for real-time multiprogramming.
3. ✓ Multi-terminal, real-time BASIC, FORTRAN IV, ALGOL and assembly language, for easy program development.
4. ✓ Multi-stream batch, for increased efficiency.
5. ✓ RJE to IBM 360/370, for convenient access to large computers.
6. ✓ Fast response to real-time interrupts, for measurement and control applications.
7. ✓ I/O spooling, for increased throughput.
8. ✓ Network software, for remote file access, program communication and device-sharing with satellite computers.
9. ✓ 4K RAM semiconductor memory, for increased reliability.
10. ✓ Large-capacity discs with 25 millisecond average access time and 937 Kilobyte transfer rate, for increased performance.

The HP MX/65 DISComputer. Ideal partner for RTE-III.

RTE-III. The HP 21MX series does it again! Now, there's Real Time Executive-III. Just one more reason to choose HP's 21MX series for your real-time applications.

RTE-III gives you an operating system geared to the complex and varied needs of automated testing, research and production environments.

RTE-III is an ideal partner for HP's MX/65 or MX/55 DISComputers. Or use it with our 9600MX Measurement and Control systems.

Prices for complete systems start at a low $38,150* for a 32K word system.

There are no "maybes" about this operating system. It's the latest in HP's family of proven, upward-compatible, Real Time Executive systems. Systems that have been proven in hundreds of on-the-job applications.

To check out all the benefits of HP's RTE-III system for yourself, give your nearby HP field engineer a call.

*US Domestic Price only.

HP minicomputers. They work for a living.

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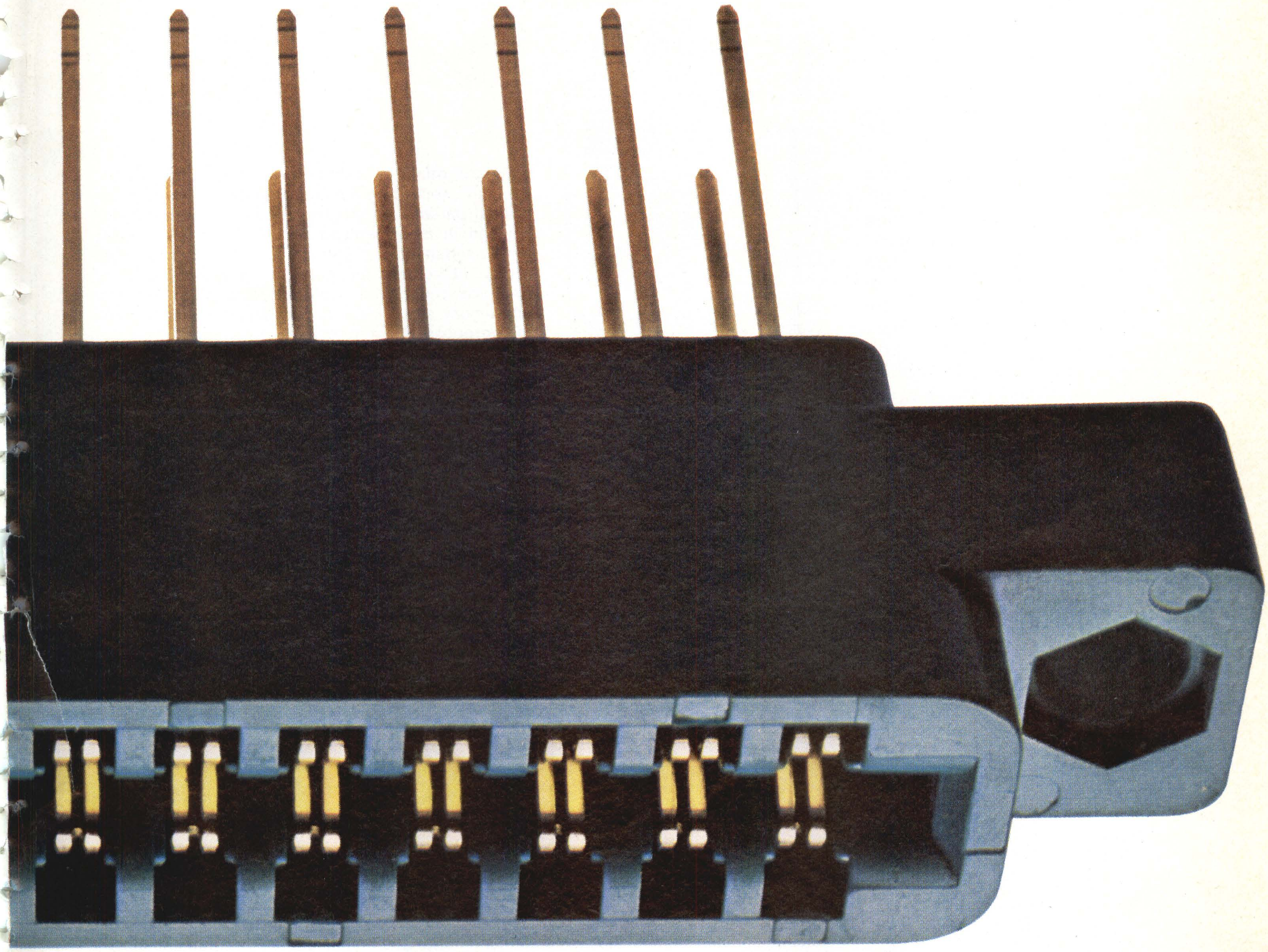
CIRCLE 14 ON INQUIRY CARD



with the outside world.

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We maintain this quality control and precision manufacture in high-volume production. We have to, since we supply the largest users of circuit connectors in the country.

What we've done for them, we can do for you.

When you need circuit board connectors that have to talk to the outside world, talk to somebody who's wise in the ways of the outside world —Sylvania.

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We're helping you make it.

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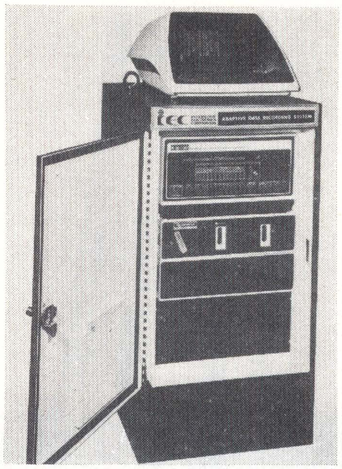
CIRCLE 15 ON INQUIRY CARD

Adaptive Reporting System Delivers Data for Critical Decisions



Onboard offshore drilling rigs, Interstate's adaptive data recording system measures and records critical parameters affecting platform performance. Housed in a ruggedized cabinet, with an integral heat exchanger (or optional air conditioner), that is sealed against the corrosive action of salt air and sea water, the system provides all sensing equipment and hardware for gathering, conditioning, processing, storing, and recording data

As platforms and drilling ships move out into deeper, rougher waters, the investment in rig construction increases considerably, with the price of a semisubmersible typically surpassing $30,000,000. Daily operating costs are going up accordingly: $45,000/day is not unusual for rough offshore areas. The fine line between environmental conditions which are dangerous to rig safety and those which are rough but still permit drilling becomes more and more critical as risk to rig is balanced against the costly loss of drilling time. Unfortunately, this kind of decision is often made on the basis of human observations and "seat-of-the-pants" assessments of environmental conditions. For more reasoned judgements, the timely, ongoing analysis of rig status and performance statistics is vital.

To provide the information which has become necessary for successful operations management, Interstate Electronics Corp, Environmental Engineering Div, 707 E Vermont Ave, Anaheim, CA 92803, developed its Adaptive Data Recording System. Monitoring and recording critical parameters that affect the performance of drill ships and platforms, the system collects data on drilling and shipboard operation as well as on the influence exerted on the structure by ocean and weather. Housed in ruggedized cabinetry, standard system hardware consists of processing computer, dual-cassette recorder, keyboard-controlled CRT display for presentation of real-time data and recall of statistical summaries, and a peripheral printer to provide shipboard logs.

System design and programming permit smooth operation by normal rig personnel. Compact tape cassettes are used to change software programs and record data. All data displays are provided in engineering terms and units to permit easy interpretation, and operating tasks consist merely of initial clock setting and biweekly cassette changes. Essential performance data are provided directly to the operator, while detailed statistical data are stored for further processing ashore. Regular maintenance employees can modify the system at the field installation. Software variations can be programmed on cassettes by Interstate, then transported to the rig for loading into the system tape deck.

Installed onboard an experimental tension-leg drilling platform design developed by Deep Oil Technology Corp, one system is collecting data on the rig's first sea trial. It will measure the amount of sway in relation to an acoustic beam installed on the sea floor; sense platform acceleration with three 2-component accelerometers on the platform deck; and compute dynamic values for surge, sway, yaw, pitch, roll, and heave from these data. Tension variations in the anchor cables will be measured with hydraulic load cells and measurements of the actual sea state acting on the platform will be made in conjunction with these recordings.

The system's data acquisition subsystem incorporates all input sensors and hardware for gathering and preparing sensor signals for processing: signal conditioners, low-pass filters, a multiplexer, and an analog-to-digital converter.

Signal conditioners provide sensor excitation and amplification, when necessary. Low-pass filters remove extraneous noise from each signal. The multiplexer scans sensor signals and feeds them to the analog-to-digital converter, which translates each signal into digital form so that it may be accepted and processed by the onboard computer.

The signal processor, together with peripheral recording equipment, analyzes and stores all processed information. This onboard computer permits great flexibility in control of data acquisition, recording, and display functions, and provides capability of expanding or modifying these functions at the operating site.

Use of a dual-cassette recorder permits approximately four days of continuous operation between cassette changes, and allows necessary changes to be accomplished without interrupting the recording cycle. This recorder is also used to load various software programs into the system. CRT display and keyboard provide the operator quick access and easy visibility of data. A peripheral printer furnishes hardcopy records of displayed information.

Addition of a magnetic tape recorder will provide a complete running raw data record (required by certain regulatory agencies and for experimental programs). Other equipment such as digital plotters for producing stripchart type recordings may be included if the application requires.

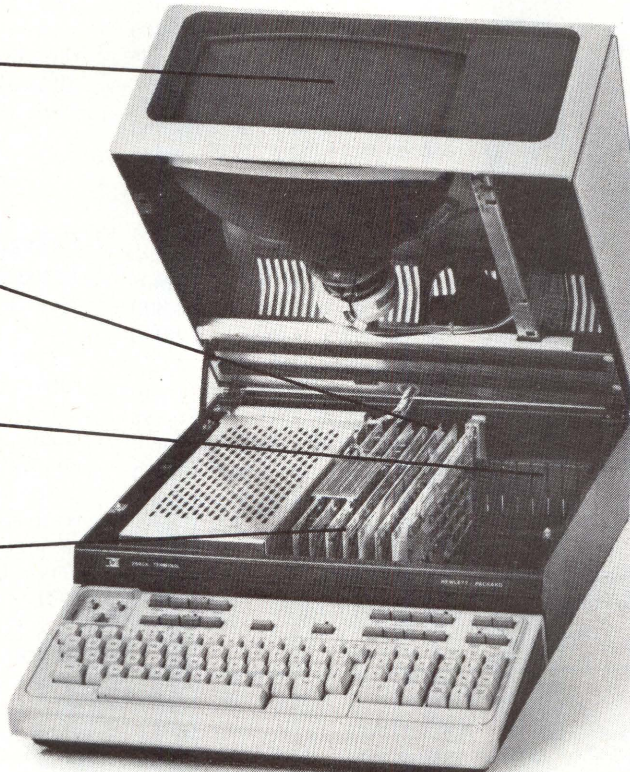
Circle 151 on Inquiry Card

Miniature Data Cartridge Records at 800 Bits/in., Transfers at 8000 Bits/s

Using exactly the same operating principles as the earlier 3M DC-300-A, but one-third its size, a miniature data cartridge, developed by 3M Co, Minneapolis, Minn, will be used for low cost, local mass storage in future products of Hewlett-Packard Co's Computer Systems Group in Cupertino, Calif.

Measuring 3 x 2½ x ½", the cartridge contains 140 ft of 0.15-in. wide tape, and records more than 100,000 bytes of data on one track. Tape control—better than is possible with a cassette—allows high density recording and fast transfer rates.

Now Hewlett-Packard makes selecting your next terminal an open and shut case.



Plug-in character sets.
The 2640A can store four 128 character sets concurrently: optional math, line drawing, and upper/lower case Roman.

Smart memory (with 4K RAM's).
Store as many as 50 short lines with the standard memory, or over 3 pages with the maximum 8K memory.

Pop-in, pop-out modularity.
Want to add features? Plug them in. Need a repair? Pop out the old. Plug in the new.

Computer-born technology controls the show.
Microprocessor controls memory, data communication, keyboard, and display.

Inspect its features. At $2640* you won't find another terminal that comes close. Inside or out. HP's 2640A. The terminal that grows with your system. It's from Hewlett-Packard. Come and get them.

A display that people like.
Precise. Crisp, with 9 x 15 dot character cell. All sorts of options, such as inverse video, underlining, half bright, blinking.

Why wait on us? Self-test.
Press the TEST key and the 2640A gives you a go/no-go indication.

Characters or blocks. You choose.
Transmit by field, line, or page at a time. Text can be composed locally allowing user verification before transmission. Character or line insert and delete, protected fields, and off-screen storage cut editing and CPU connect time. Plus, eight keys for user-defined function.

HP terminals. They work for a living.

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*Domestic USA price in quantities of six.

Providing reliability, long life, and interchangeability of the 3M DC-300-A, three times its size, this mini-cartridge measures 3 x 2½ x ½ in., contains 140 ft of 0.15-in. wide tape, and records more than 100,000 bytes on a single track

The minicartridge's reliability and long tape life qualify it not only to replace cassettes, but also to replace paper tape in many situations, according to Paul C. Ely, Jr, general manager of H-P's Computer Group. Drive requirements are much simpler than those of cassettes; the drive mechanism need have only one rotating part. Within the cartridge, an elastic belt, along the surfaces of the two tape reels, actually drives the tape, keeping both speed and tension constant. Tape control permits recording at a density of 800 bits/in., and transfer to occur at 8000 bits/s at a tape speed of 10 in./s.

The cartridge resulted from a cooperation whereby 3M engineers worked closely with H-P to meet specified requirements. Anticipated applications are data entry and acquisition and storage of both programs and data for minicomputers and terminals.

Circle 152 on Inquiry Card

Floppy Disc System Cuts Microcomputer Program Development Time

Plugging directly into Motorola's EXORciser (a system-prototyping minicomputer for the M6800 microprocessor family), the FD360-68 floppy disc system cuts hours from program development times. Eliminating the need for paper tape or cassette handling and storage, the system, supplied by iCom, Inc, 6741 Variel Ave, Canoga Park, CA 91303, utilizes reusable diskette cartridges, includes all necessary software on an IBM diskette, and contains all hardware necessary for immediate operation.

Consisting of from one to four floppy disc drives, IBM-compatible formatter/controller, and desktop cabinet with power supplies, cooling, and cabling, the system can be connected by plugging its interface into one EXORciser card slot; direct interface can be accomplished with latch I/O modules such as Motorola's MC6820 peripheral interface adapter (PIA) chip.

Disc system features include IBM 3540- and 3740-compatible data format and storage capacity for up to 256 kilobytes on each diskette. The disc head retracts from the media when not reading or writing to increase media life; the motor shuts down on load and unload to reduce media hub wear.

Each controller handles up to four drive units; each drive may be individually write-protected by a jumper on the controller-board connector. Asynchronous byte transfers to/from the CPU are enabled through provision of two separate 128-byte input and output buffers in the controller. The unit provides complete hardware track seek and seek verification as well as hardware CRC generation and verification.

Its Floppy Disc Operating System (FDOS) is a complete program development system, which, in addition to the EXORciser's EXBUG™, provides high speed software development tools that are usually available only on large minicomputer systems. Program storage and backup are provided on reusable diskette cartridges. Containing single command operations such as disc-to-disc program editing and assembling, disc-to-memory program loading, named files, and disc-to-disc file transfers, the system reduces time required for a typical edit-assembly sequence to approximately 5 min., compared to the 2 or 3 hr required using a teleprinter; and permits 10 times faster throughput than is gained using a paper tape reader or magnetic tape cassette.

Resident FDOS is contained in one p/ROM located on the system interface card. Its disc-resident assembler and editor are identical to the stand-alone editor and assembler for the EXORciser. EXBUG remains intact to retain all existing non-FDOS operations. The software is operational on any system containing from one to four of the disc drive units, and can utilize all available disc storage capacity.

Circle 153 on Inquiry Card

Private Branch Exchange Incorporates Computer for Extended Capability

Providing additional operating features and user conveniences plus price-competitiveness with other electronic private automatic branch exchange (PBX) equipment, the Computerized Branch Exchange (CBX) is claimed to provide substantial savings in both equipment costs and network usage charges. Available from ROLM Corp, 18922 Forge Dr, Cupertino, CA 95014, for business and institutional applications having between 80 and 800 telephone stations, the minicomputer-based system provides incoming traffic distribution, outgoing traffic management, user convenience and efficiency, and system reliability and service economy.

The CBX uses time-division multiplexing (TDM) instead of space-division multiplexing common to traditional PBX equipment. This technique provides a common bus that appears to be a continuous connection between calling and called parties. Transmissions are sampled frequently enough to assure good voice fidelity and no information loss, while permitting multiple stations to use the bus. Combined with computer control, the technique permits greatly simplified system wiring requirements. The system uses 3-pair wiring throughout instead of the 25- and 100-pair cables required for key telephones and call directors. This permits simple, inexpensive installation as well as efficient moves, changes, and additions.

Further savings are realized since the system uses standard telephones and provides user features that minimize the need for multibutton telephones. Multiline phone requirements are reduced with call pickup, group pickup, consultation hold, alternate answer, com line, and do-not disturb features. User convenience is pro-

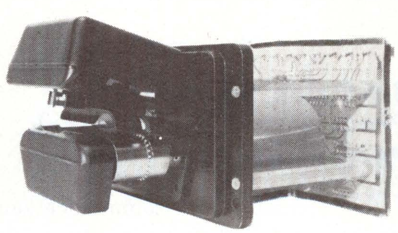
Most of these knowbodies will choose Step-Mate.

It takes a real knowbody to buy our Step-Mate tape reader. Those who don't know about Step-Mate usually buy that other company's device.

But of those who know about theirs and ours, and who give us a fair shot, three out of four choose ours: Step-Mate.

It's not our charm that does the trick. It's our product and our price.

Take the product. Step-Mate is a direct descendant of the first stepping motor drive tape reader ever built, which was ours, back in 1958.



Step-Mate reads 150 characters per second, interfaces easily with other equipment (24 volts), and is almost excessively reliable.

Step-Mate incorporates such costly features as a stepping motor, LEDs instead of lamp bulbs, phototransistor read sensors, full tape width barrel sprocket, and a self-cleaning readhead.

But it isn't costly. Only $360.

At this point you're practically a knowbody. Don't stop now, give us a call. And a chance.

EECO

FOR READERS

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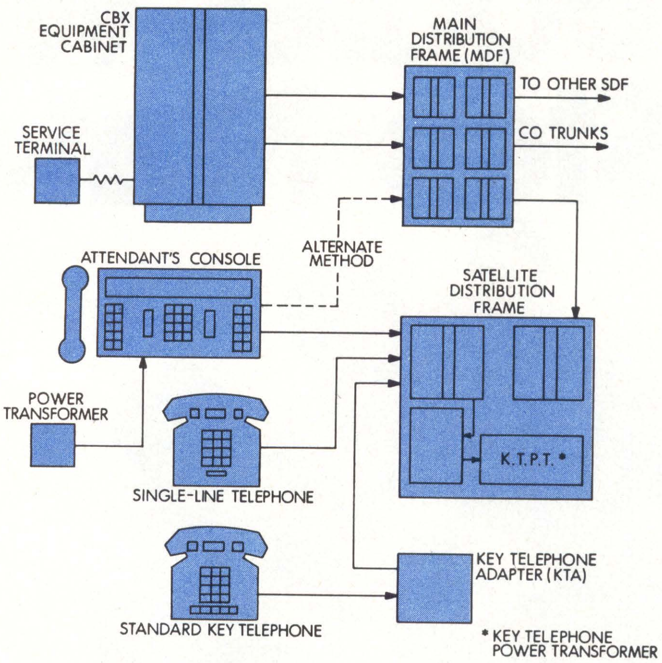
CIRCLE 17 ON INQUIRY CARD



Typical installation of "The Business Switch," ROLM Corp's Computerized Branch Exchange, which incorporates a minicomputer to provide extended operator features and user conveniences. Servicing between 80 and 800 telephone stations, the system cuts equipment and installation costs by using 3-pair wiring, and reduces usage charges through automatic route optimization and toll restriction features

vided through conferencing, speed calling, repeat number dialed, call forward, and automatic callback features.

The minicomputer at the heart of the system enables further cost reductions by providing toll and feature restrictions with up to 16 different classes of service on an individual telephone basis; automatic identification of outgoing dialing (AIOD) allows the user to establish accurate allocation of telephone expenses and to monitor the calling activity on all phones within the system. On outgoing calls the device automatically selects the most effective means, and eliminates special access codes for WATS and foreign exchange lines.

System reliability is enhanced by redundancy, built-in self-test, and remote error detection. Online system diagnostics constantly check the system for malfunctions; testing can be done at the installation site or remotely. Most wear-prone devices used in existing electromechanical and hybrid PBXs have been replaced with solid-state circuitry. Routine maintenance and repair service operations can be done without affecting normal system operations; moves and changes can be accomplished from a remote location at any time.

Circle 154 on Inquiry Card

Bit-Oriented Control Procedure Ups Network Performance/Response

A bit-oriented data communications control procedure designed to provide greater control flexibility, network integrity, system throughput performance, and response time in synchronous transmission of data within networks has been released by Burroughs Corp, Detroit, MI 48232. Called Burroughs Data Link Control (BDLC), the capability supplements standard basic mode data communications line control procedures, allowing terminal systems to serve different application needs while operating on the same communications line. This permits BDLC procedures to be used on existing networks that contain links operating with conventional procedures.

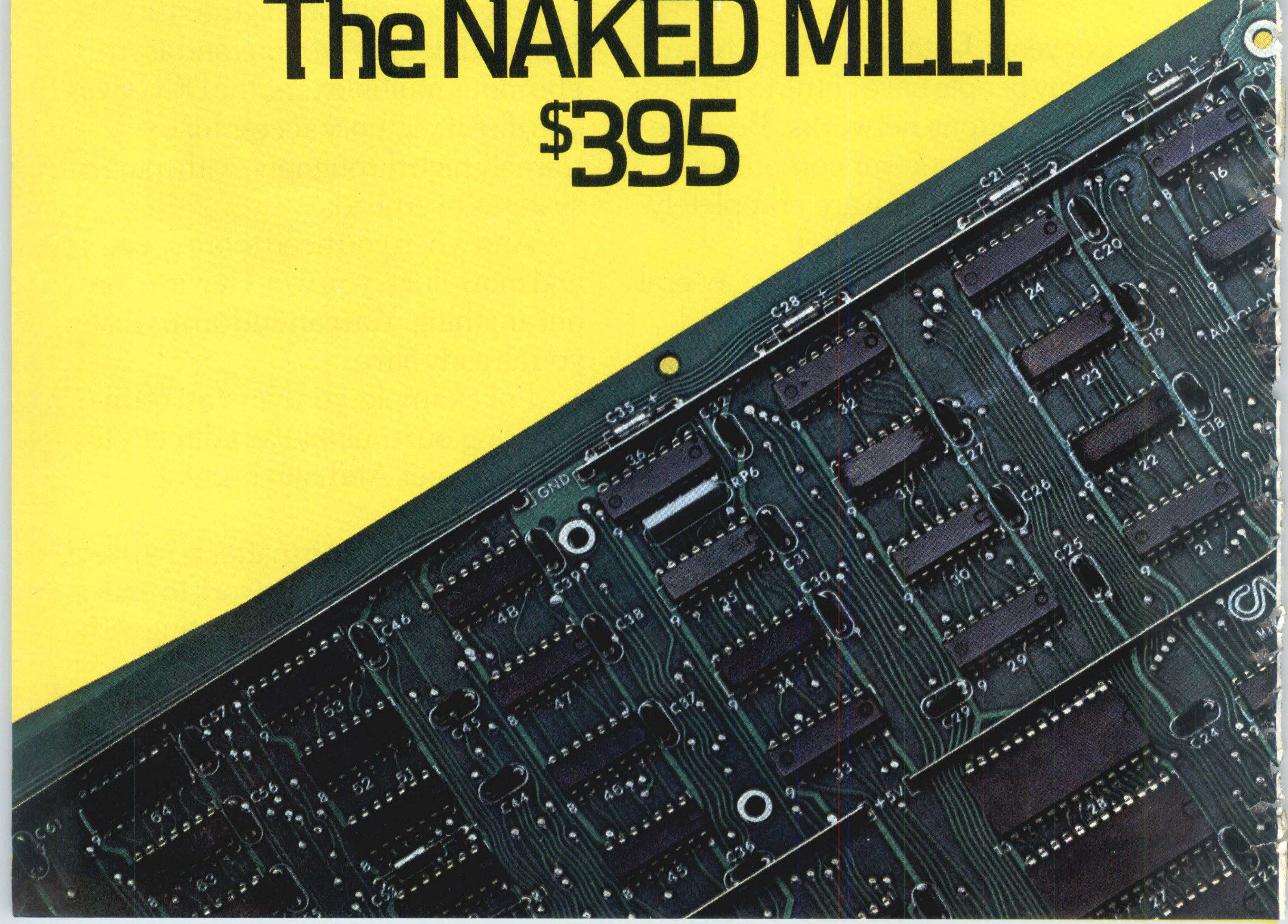
Providing an alternative to the method of transmitting message blocks of formalized character structures, BDLC provides efficient, high speed transmission of bit streams. With the method, information fields may be variable in length and may use any code or grouping of bits. Transmission control can be accomplished simultaneously with data transfer, and techniques for exception condition detection and error recovery are provided. In addition to telephone line communication, the method is applicable to microwave and satellite transmission systems as well as to digital data networks.

Essential elements of the technique are based on the principles of assigning primary and secondary relationships between stations on a data link for control purposes; standard frame structure, consisting of opening flag, address field, control field, variable length information field, frame check sequence for error detection, and a terminating flag for information exchange; independent numbering for frame sequencing; and modularity of procedure structuring and flexibility of the command/response repertoire.

Full utilization of network resources is permitted by the flexibility and adaptability of features, which take advantage of emerging technological developments such as packet switching and other computer-based data communications systems. Modularity of commands and responses permits selection of the specific combinations that are best suited to particular applications or operational environments, including interactive, batch, inquiry/response, conversational, or computer-to-computer data communications environments using 2-way simultaneous or alternating procedures.

The technique was developed through participation with national and international groups, including the American National Standards Institute, European Computer Manufacturers Association, and International Standards Organization (ISO). The Burroughs standard conforms to the draft ISO High-Level Data Link Control (HDLC) standard and is compatible with national draft standards. BDLC's modular structure allows modification to meet adopted standards, if necessary, and provides compatibility with other manufacturers' bit-oriented procedures. □

Circle 155 on Inquiry Card



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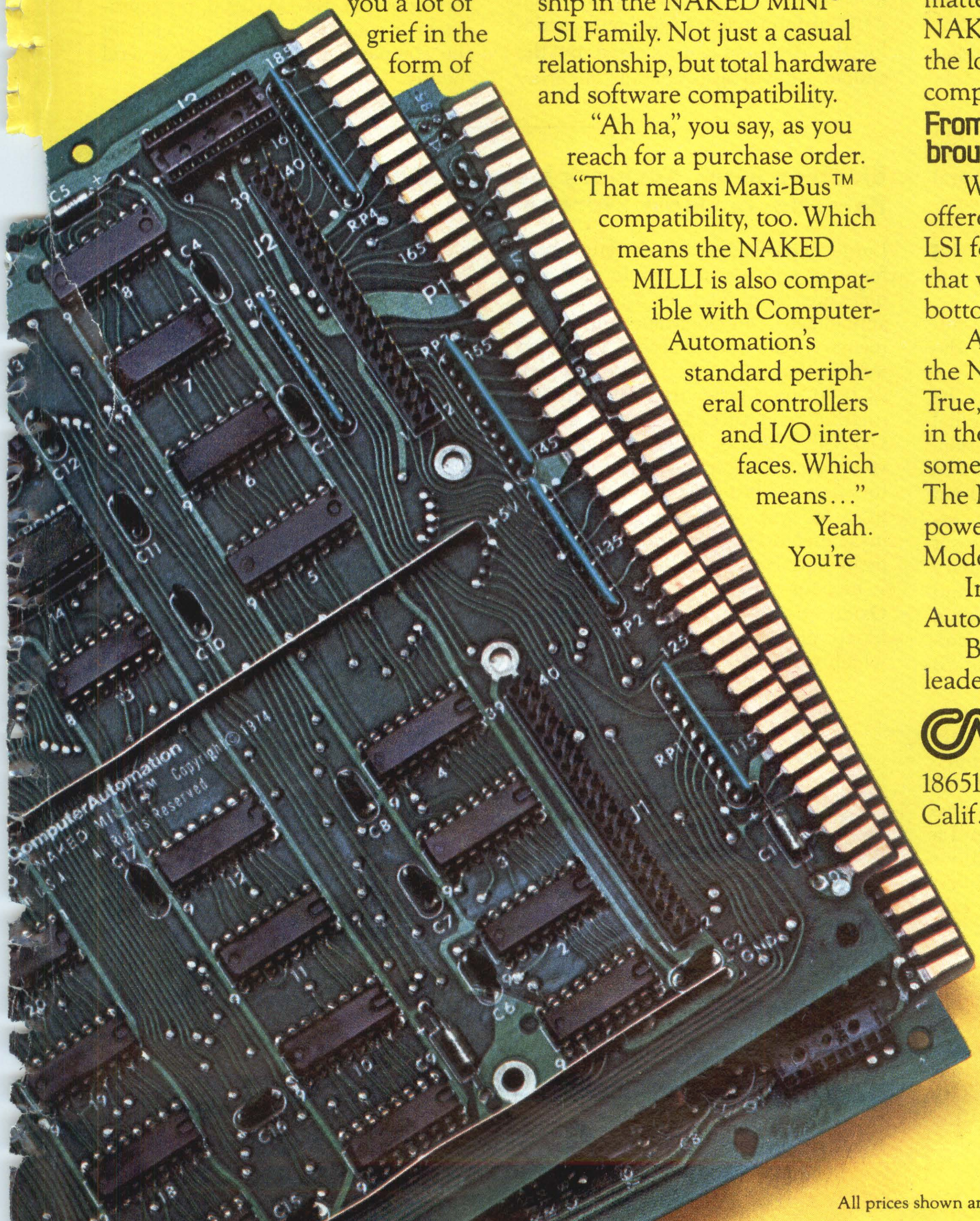

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DEVELOPMENTS

Microprocessor Family Will Offer High Speed Plus Versatility

A bit-slice-oriented series of microprocessors, consisting initially of five emitter-coupled logic (ECL) technology large-scale integration (LSI) circuits to be introduced in 1976, is claimed to offer system designers greater opportunities for both speed and variety in detailed architecture and software. A complete microprocessor is made up by interconnecting the five LSI blocks: 4-bit processor slice, control register, timing function, slice/memory interface, and slice lookahead circuit.

Applications for the M10800 microprocessors will include all systems that must process large amounts of data at high speeds. Typical would be the central processing unit, input/output (I/O) channels, communications controllers, and high speed peripheral controllers of large mainframe computers; minicomputers; high speed instruments and testers; real-time signal analyzers; and time-sharing systems.

The bipolar integrated circuit, microprogrammable processor set, developed by Motorola Semiconductor Products Inc, Phoenix, Ariz, may be used for byte-serial or byte-parallel bus organizations. Lateral expansion, in 4-bit increments, will be permitted to any width. High data throughput rates may be achieved by vertical expansion. A system using this processor will be able to process both binary and binary-coded decimal data and provide parity for error checking. Typical speed of operation, per microinstruction cycle, will be less than 75 ns.

The processor slice will contain arithmetic logic unit (ALU), data latch/mask and shift network units, accumulator, and I/O bus control sections. Data will flow through the slice via two bidirectional 4-bit ports and a 4-bit data input bus. Slice operations will be controlled by 16 select lines, and five additional output lines will signal ALU status. It will be possible to construct microprogramming steps from a set of over 70 ALU functions.

Logic for microprogram control will be contained in the control register, which will also accomplish control memory addressing, branching and interrupt operations, and system I/O interfacing. The timing function—the third block—will control phases of various clock signals throughout the system and will provide a means of interfacing the system to a manual test/control panel.

The slice/memory interface will be used to connect the processor slice (or slices) to a main memory system. It will contain data and address storage for complex addressing techniques. The fifth block—slice/lookahead circuit—will permit high speed arithmetic operations, in multiple-ALU organizations, by performing a lookahead carry function. This block will combine the group propagate, generate, and carry outputs of each ALU to form partial sums and carries for the data being processed by the system. It will also contain an array of logic elements that may be used for various ancillary functions.

All M10800 circuits will be logic level, power supply, and noise immunity compatible with the company's standard MECL 10,000 family of small-, medium-, and large-scale integration logic and memories as well as memories from competitive sources. Packaging of the processor slice and some of the other circuit blocks will be 48-pin quad-in-line, with the lead frame in a staggered-pin arrangement such that they can be housed in 24-pin packages.

Unique system software will not be offered. However, the processors will be adaptable to existing software. Full component documentation and support will be furnished.

Pricing has not yet been established, but the company expects that it will be competitive. Additional information on the M10800 microprocessor family will be announced by the company during the next several months.

Electron Beam Auxiliary Memory Offers Potential for Mass Storage Uses

Large data capacity, high data transfer rate, and a very flexible data format are combined in the recently announced all-electronic BEAMOS memory. Computer access to stored information is expected to be as much as 1000 times faster than with present rotating memories. Developed at the General Electric Research and Development Center, Schenectady, NY for use in fast auxiliary memories, BEAMOS will also be applicable to mass memories after further development and cost reduction.

BEAMOS (BEam Addressed Metal Oxide Semiconductor) memory is based on use of an electron beam which reads and writes data on a simple, unstructured MOS chip. Data can be stored for months (but not permanently) with or without power. Although designed primarily for military applications under adverse conditions of shock, vibration, rough handling, dirt, or dust, the memory eventually may also be marketed for commercial computer systems.

A complete BEAMOS memory is made up of one or more BEAMOS modules, address and interface logic, control circuits, and power supplies. Initial development was of a 32-megabit capacity memory because that size best fit the expected application. Lower capacity units are relatively easy to build but have a higher cost

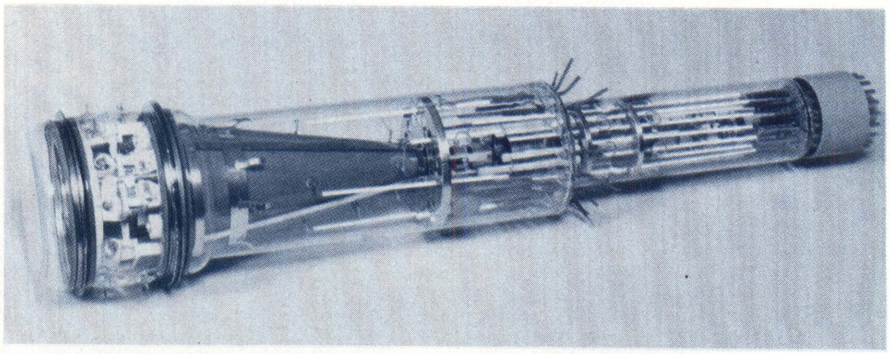

Fig. 1 BEAMOS memory module developed by General Electric contains a memory plane, made up of four MOS chips, and an electron-beam-accessing system, including matrix lens and 2-stage deflection system, all enclosed in a 17" long x 4" dia sealed, evacuated envelope. First module has 32-megabit capacity, 30-μs access time, and 10-megabit/s transfer rate

The next time you buy a microprocessor, you don't have to sign away your freedom of choice.

The AMI S6800 family is totally unbundled. You can order any part of it with no strings attached.

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For software support, you're free to use AMI's new relocating macroassembler, linking loader and simulator —all available on a major time-sharing service. You don't even have to buy the processor to get this support.

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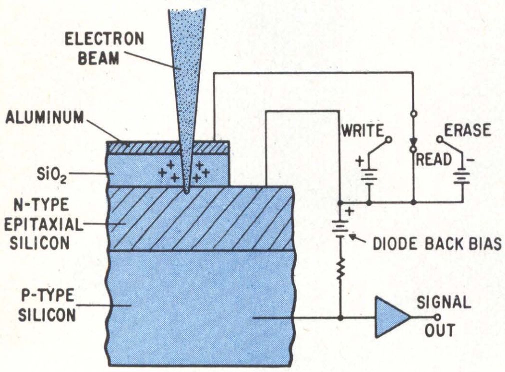


Fig. 2 Cross-section of MOS memory chip. Aluminum film is evaporated onto a thin insulating layer of silicon dioxide formed on n- and p-type silicon layers connected electrically as a back-biased diode. All layers are arranged in continuous, unstructured planes. A positive bias is applied to write and a negative to erase; zero volts allows read before rewrite

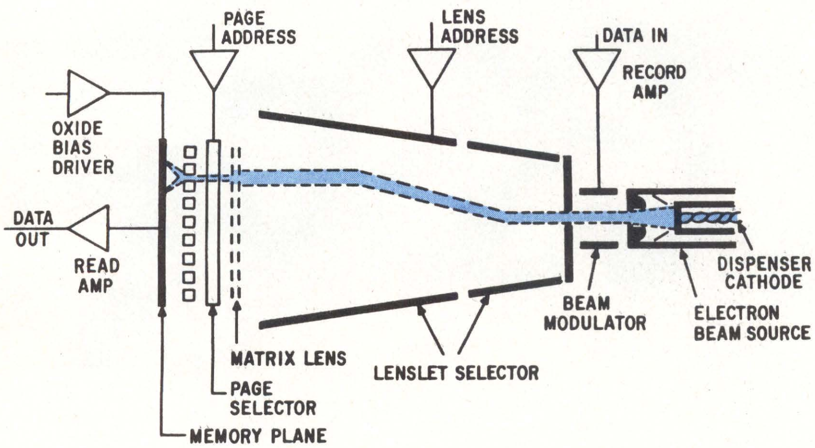


Fig. 3 BEAMOS electron optical system. First deflection occurs when applied voltage produces an electron lens which focuses the beam to an extremely fine spot. Page address voltage then deflects the beam into the proper memory site within the lenslet field

per bit; larger capacity provides lower per-bit cost but permits less modularity in systems design.

The present module has 30-μs access time and 10-megabit/s transfer rate. Spacing between bits is 4 μm. Modules of the same external physical size, but with 100-megabit capacity and 2.5-μm spacing between bits, are under development.

The memory module (4" dia, 17" long, and 2.8 lb) is a sealed, evacuated envelope (Fig. 1) containing an MOS memory plane and an electron beam matrix lens and deflection system. Data are stored as minute islands of positive charge on the memory plane, which consists of four 15-mm-sq chips mounted on a baseplate; the electron beam system is used for reading and writing the data. The plane is made up of a film of aluminum evaporated on a thin insulating layer formed on a silicon diode. The n- and p-type silicon layers are connected electrically to form a back-biased diode. Memory operating mode is controlled by applying a voltage across the oxide layer (Fig. 2).

Memory sites are addressed for reading, writing, or erasing by a 10-kV energy electron beam, controlled by 2-stage deflection and a matrix electron lens made up of 289 separate lenslets (Fig. 3). To write, a positive 40-V bias is applied between the aluminum and n-layer (Fig. 2), and the electron beam is deflected to the site where a "1" is to be stored. As the beam penetrates, it excites a large number of holes and electrons in the oxide, causing electrons to migrate to the aluminum, while the positively charged holes remain near the interface of the oxide and silicon.

To read, a slight negative or zero bias is used. The electron beam penetrates a short distance into the silicon where it generates a large number of hole-electron pairs. Some of the holes diffuse into the depletion region of the p-n junction, and are swept across, producing a signal pulse. Remaining holes approach the oxide-silicon interface where they are neutralized by recombining with electrons. Under oxide regions containing stored positive charges the holes are repelled away from the oxide to the junction, resulting in a large signal pulse, as they sweep across.

To erase, an appropriate reverse bias is applied to the aluminum, which causes the reading beam to neutralize the stored positive charge in the oxide, resulting in destructive readout. It is possible to prevent neutralizing of the positive charge by an intermediate bias setting. This permits from 10 to 20 read cycles without erasure (nondestructive readout).

MTBF of a BEAMOS memory system is predicted to be more than 8000 hr; the module itself has a life expectancy of at least 20,000 hr. The barium aluminate dispenser cathode (electron source) undergoes only 10% reduction in emission after 40,000 hr of continuous operation.

Dr Arthur M. Bueche, GE vice president for research and development, expects that the "impact (of BEAMOS) on the operation and architecture of computer systems will be far reaching, and is expected to result in substantial reductions in hardware and software costs." In a computer memory system, 16 or more modules could be linked to provide 500 megabits of memory, and could be accessed in parallel to provide data transfer rates of 160 megabits/s. Laboratory tests indicate that up to 1 billion bits could be stored in a single module.

The company estimates that BEAMOS will be competitive with magnetic disc and drum memories on a cost-performance basis. Price per bit —including supporting electronics—is estimated to be "about one-tenth of a cent, but could decline to one one-hundredth of a cent."

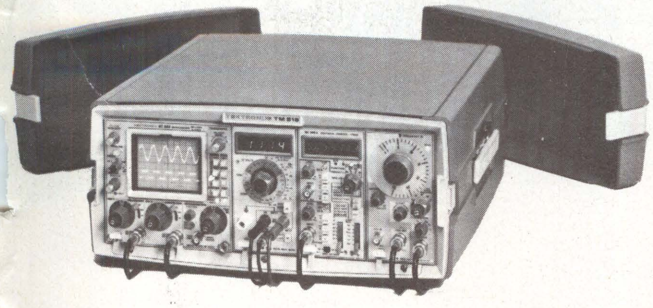
Further data on this development is contained in "BEAMOS—A New Electronic Digital Memory," W. C. Hughes et al, in the *Proceedings of the 1975 National Computer Conference,* pp 541-548.

TEKTRONIX ANNOUNCES

A new concept in portable instrumentation

The TEKTRONIX TM 515 Traveler Mainframe looks like fashionable flight luggage, compact and easy to carry, or slide under an aircraft seat. In reality, it's a five-compartment power module/mainframe that provides power and interface connections for TM 500 plug-in modular instrumentation. Plug in the new (two-wide) SC 502 15-MHz dual-channel oscilloscope, and you have the beginnings of a powerful take-along instrumentation system.

You can optimize a TM 500 system to your needs by selecting from more than 30 plug-in modular instruments. With the TM 515 Traveler Mainframe and SC 502 Oscilloscope as a nucleus, select from DMM's, counters, generators, power supplies, signal processors, and even blank plug-ins for your "home-built" circuits. Intended applications include areas from digital field service to medical, from audio/communicatons to on-site industrial controls maintenance.



The SC 502 is Tektronix quality, featuring clean triggering characteristics, delay line input, trigger view, trigger holdoff, 1 mV sensitivity, and the capability of working through the rear interface circuit board with other TM 500 instruments. It features a specially brilliant crt designed and built by Tektronix for use in areas of high ambient light. Include a DD 501 Digital Delay alongside the SC 502 and gain the capability of delay-by-events—you can then obtain stable digital displays from electromechanical sources like disc drives that would otherwise be too jittery for accurate viewing on any conventional oscilloscope. Include the DC 505A Universal Counter and DM 502 Digital Multimeter to complete your TM 515 package, and discover the benefits of simultaneous counter and DMM capability with trigger level readout at the touch of a push button.

The TM 500 concept lets you take along on field servicing trips the same instruments you use in the lab or for production testing, thereby enabling you to maintain the same standards on the "outside". The SC 502 Oscilloscope, for example, may be used as a bench instrument in any multiple-compartment TM 500 mainframe, and it offers unique systems capabilities, as well, when operated in a rack in the RTM 506.

Contact your local Tektronix Field Engineer or circle the appropriate reader service number for a demonstration of TM 500 instrumentation or additional technical information on the TM 515 Traveler Mainframe and SC 502 Oscilloscope. For an up-to-date TM 500 Catalog write to Tektronix, Inc., P. O. Box 500, Beaverton, Oregon 97077. In Europe write Tektronix Limited, P. O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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Cores made with Ampex temperature-independent material are so insensitive to temperature differences that you get better operating margins over the entire military qualification range, without current compensation (or any other kind of compensation). And only TIN cores permit reliable cross-temperature operation.

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DEVELOPMENTS

Plastic Modulators May Be Feasible for Control of Writing Laser Beams

Results of experiments conducted at Eastman Kodak Co's Research Laboratories in Rochester, NY indicate that injection-molded plastic modulators may help shrink both the cost and size of future laser recording and display equipment. In a paper presented at a Society for Information Display seminar in Washington, DC, Richard N. Blazey, senior research physicist at the Research Laboratories, said that although "today there are no commercial acousto-optic devices made from plastic . . . still, plastic is an attractive material to use since it can be molded, eliminating the expensive cutting and polishing required to fabricate crystal and glasses." In the experiments "we've eliminated the expensive cutting and polishing required to fabricate crystal and glass modulators by fabricating transmitting windows for the input laser beams directly into injection-molded plastic modulator blocks."

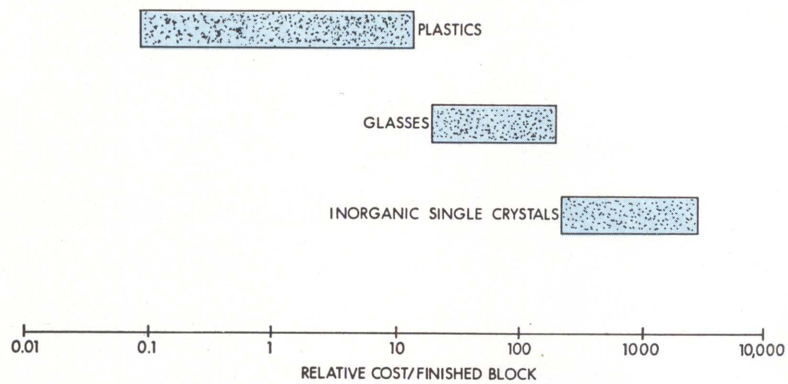
Acoustic impedances of plastics and organic adhesives are very similar. Bond thickness, therefore, is not critical and assembly can be performed without drastic precautions for cleanliness. In addition, the high acousto-optic figures of merit for many plastics reduce electrical power requirements. This permits shorter modulators that require fewer transducers.

High ultrasonic losses prevent the use of plastics in light deflectors. However, the experiments show that plastics may be used for modulators even when acoustic attenuation is quite high, since the sound wave will be attenuated only slightly in crossing the light beam because of the very small diameter of the beam. Heating by absorbed ultrasound, however, does cause some problems.

Two groups of experimental modulators were built at the Research Laboratories (see Table). One, called series B, was made from injection-molded blocks with laser beam-transmitting windows molded into the blocks. The second, series C, was machined from plastic lens blanks.

It was found that "in unfocused state the modulation bandwidth was limited by the diameter of the laser beam used. Focusing the laser through the cell reduced effective beam diameter, permitting shorter rise times. However, all the sound is effective in diffracting light only when the acoustic diffraction angle is smaller than the optical diffraction angle. Thus efficiency eventually falls as focusing makes the optical angle greater than the acoustic angle."

Several problems exist in the experimental devices. For instance, performance is limited by optical quality and thermal effects. Although the most severe optical problem—distortion of the laser beam by

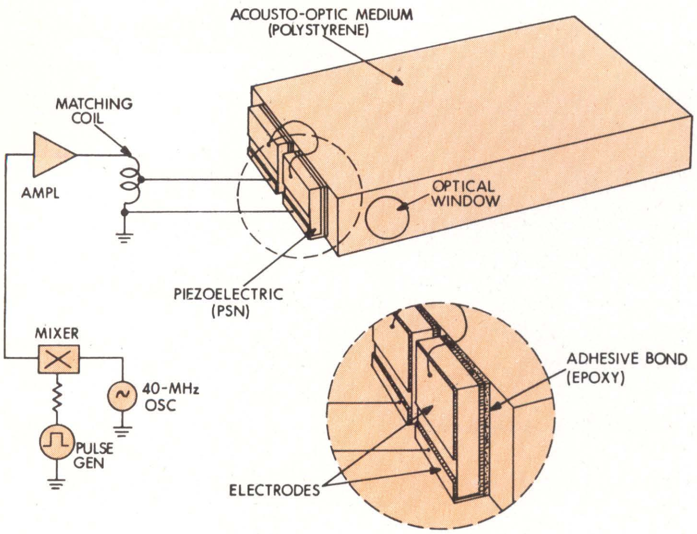


Comparison of estimated costs of fabricating acousto-optic modulators from various materials. Plastic blocks have been found to be far cheaper than either glasses or crystals

Plastic Modulator Characteristics

Series	Unfocused Beam B*	Unfocused Beam C**	Focused Beam B*	Focused Beam C**
Optical beam diameter (mm)	1	1		
Rise time (ns)	500	500		
f-number			150	133
Minimum rise time (ns)			40	100
Modulation bandwidth (MHz)	0.7	0.7	8.7	3.5
Maximum CW efficiency (%)	34	55	34	—
Maximum CW power (W)	1	0.56	1	0.56
Acoustic bandwidth (V = const)	24	16	24	16
Linear peak efficiency (%/W)	34	100	34	—
Optical contrast ratio	1400:1	—	100:1	—
Spectral range (μm)	0.4 to 5	0.4 to 5	0.4 to 5	0.4 to 5

*Made from injection-molded blocks which have laser beam-transmitting windows molded into the blocks
**Machined from plastic lens blanks



Experimental modulator made at Eastman Kodak's Research Laboratories from injection-molded plastic blocks. Thickness of adhesive bond is not critical because of similarity in acoustic impedances of plastic and adhesive. Oscillator and power amplifier are mounted in a single box with the modulator

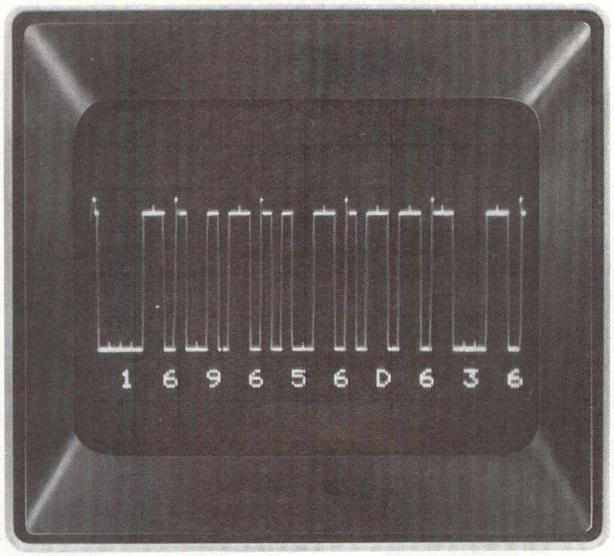
spatial refractive index gradients introduced in the molding—may be reduced by changing molding parameters, this results in a loss of flatness of the optical windows molded onto the block.

Also, heating of the acousto-optic medium by absorbed ultrasound can cause refractive-index gradients which distort the modulated beam and reduce diffraction efficiency. However, careful control of geometrical and thermal parameters and limiting CW electrical power applied to the modulator can eliminate these effects.

Mr Blazey suggested that plastic modulators could control the writing laser beams within facsimile receivers, laser data recorders, and character writing devices. However, in spite of advantages such as high efficiency, inexpensive fabrication, simple bonding, and low power requirements, no commercial plastic acousto-optic modulators are yet available, and Eastman Kodak does not plan to offer plastic modulators as a product. □

Illustrations and Table are reproduced from "Low Cost Acousto-Optic Modulators Molded from Plastic Materials" by Richard W. Blazey.

And now, for debugging serial data,



Biomation brings you the 110-D.

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The best way to tell you about the Biomation 110-D's dramatic new way of debugging serial data is to show you the memo from our own engineering staff that sold us on the concept.

Purpose

Designed to monitor, store, and display serial data, either synchronously or asynchronously. Major uses as follows:

1. High speed synchronous data (up to 10MHz)

- Rotating memories (drums, disks, floppy disks).
- Digital tape decks—up to and including high performance 3200 bpi reel-to-reel decks.

110-D will "snapshot" data and display it free of the jitter normally seen when using scope.

- Shift register and delay line memories (MOS shift registers, magnetostrictive delay lines, glass delay lines, etc. such as found in CRT-type data communications terminals and other video-refresh applications.

110-D will snapshot changing data patterns and allow stored analysis, otherwise impossible with scope.

2. Low speed synchronous data

110-D utilizes static RAMs to prevent data loss at low speeds.

- Synchronous modem channels—data between modem and terminal, between modem and computer front-end, etc. Includes Bell 201-type modems and other proprietary synchronous modems.

Using a scope has same problems as above: changing data patterns and channel jitter makes analysis difficult or impossible.

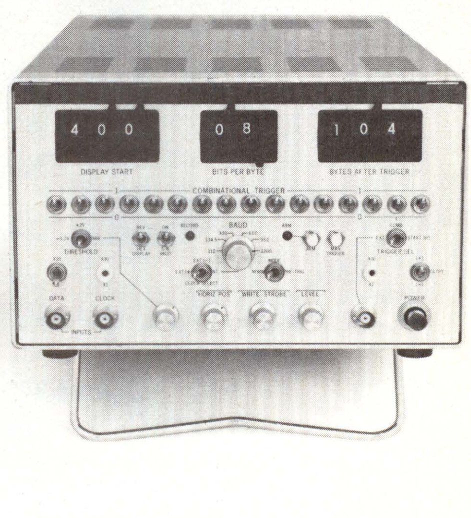
3. Low speed asynchronous data

- Asynchronous modem channels—Bell 103- and 202-type modems and equivalent units from independent suppliers. **110-D has switchable internal clock for sampling data at normal data baud rates.** Also has start-bit validation logic, for "framing" the data in start-stop data.
- RS232 data channels—includes nearly all computer terminals, both video and hard-copy. Teletype KSR-33 and Dataspeed 40 terminal are typical examples.

Asynchronous data is not only changing and jittering, but is coming in asynchronous bursts. The 110-D will time-compress the data to permit whole message groups to be easily observed.

Data from low speed computer peripherals—printers, card readers, card punches, paper-tape readers, etc. are often transmitted serially between them and the host main-frame. The 110-D is useful in developing and trouble-shooting these peripherals.

There isn't enough room on this page to give you the whole story. Please call or write us for all the technical data and for a "hands-on" demonstration of a whole new solution to serial data problems. Biomation, 10411 Bubb Road, Cupertino, CA 95014. (408) 255-9500. TWX 910 338 0226.



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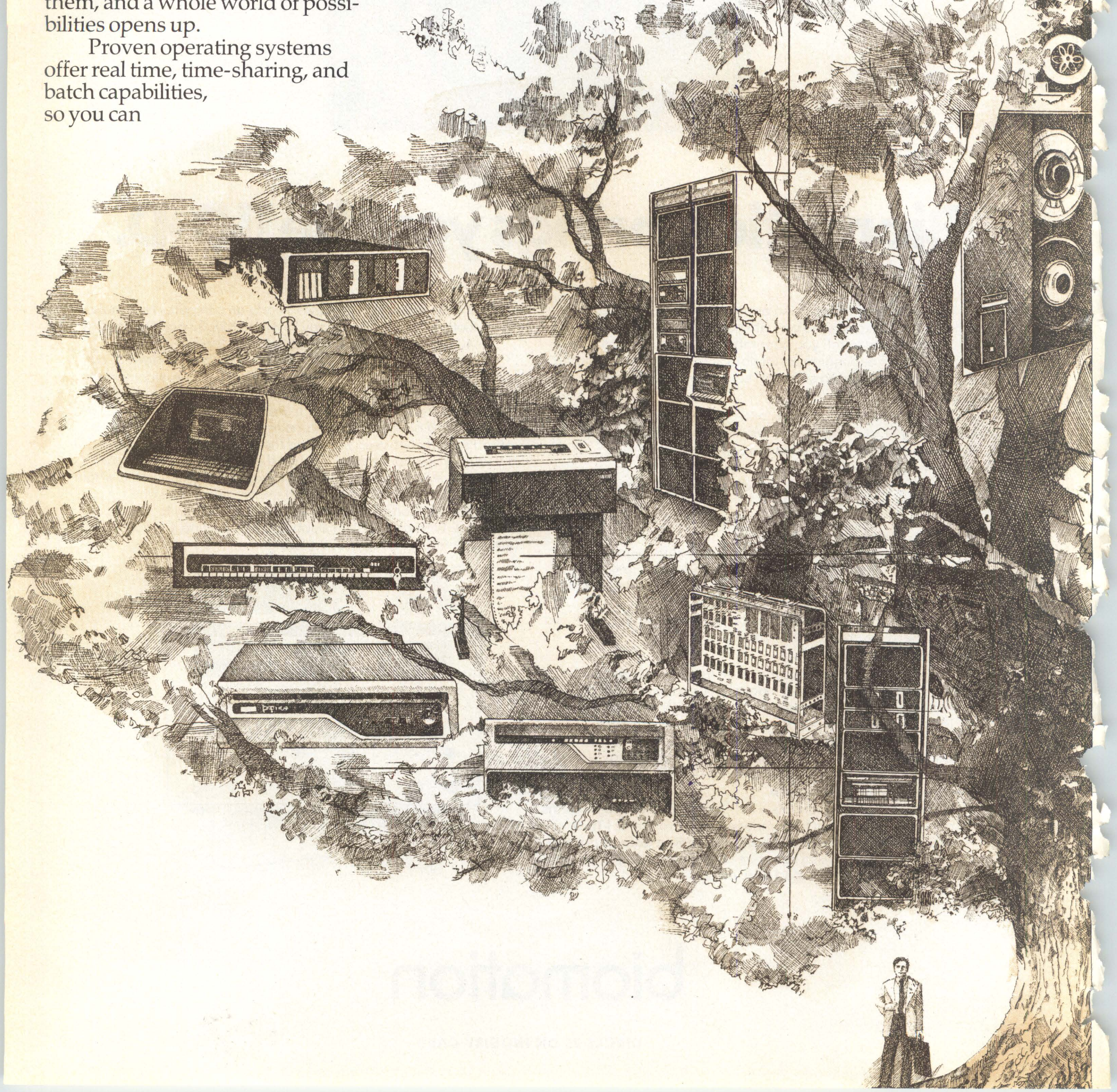

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CIRCLE 26 ON INQUIRY CARD

Direct Numerical Control: Will It Be in *Your* Future?

Is direct numerical control finally a viable process for machine tools? Can its inherent values overcome the problem of its initial high cost sufficiently to permit recovery of investment within a reasonable time? Will it eventually replace standalone numerical control? Panelists on the last day of Westinghouse Electric Corp's 39th Annual Machine Tool Forum, held in Pittsburgh on June 2 to 4, tried to answer these and many other related questions that were in the minds of the several hundred attendees. Whether or not they succeeded in satisfying each of the attendees—who, because of their diverse interests, had varied reasons for joining the Forum—can probably never be ascertained. Yet, the panelists supplied extensive hands-on information, based on actual case studies, and that alone made this session invaluable.

What is DNC?

If the panel discussion for machine tools brought out any one point, it was that the five panelists did not agree on a uniform definition of direct numerical control (DNC). Each had his own understanding of the term—prejudiced by personal experience in using DNC or standalone NC—and from that viewpoint, each was probably correct. As Mr Don Cumming, manager of operations planning, Westinghouse Steam Turbine Div, pointed out, "the definitions and distinctions are under constant change. So if you don't like my definition of DNC, wait five minutes and it'll change."

Mr Cumming's definition of DNC is: "the total feedback and control of information involved in the NC process. This implies that we're talking about a broader spectrum of information processing than just a tape. Operator instructions, production status, and machine status are all proper elements of the process. DNC started out to be the replacement of the tape communication links to the central computer which distributed the information it developed direct from the key control unit." As computing capabilities became better understood, the concept of DNC evolved toward a broader and more comprehensive information, distribution, and control system that aids and optimizes the production process.

An even more limiting definition—but of equal validity—was suggested by Mr Robert Chamberlain, vice president and general manager of Giddings & Lewis, Inc's Electronics Div: "a remote memory, serving a set of machine tools with on-demand distribution of programs and perhaps with feedback as on program sets." This definition was intended in the context of job-lot production. Although other panelists hinted at their individual definitions, in terms of a lowest common denominator, all five agreed that DNC involves control of machine tools from a central computer associated with mass memory.

(Basic distinctions among NC, CNC, and DNC for machine tool applications were provided aside from the panel discussion by Mr Bates Murphy, manager of marketing communications for Westinghouse's Industry Systems Div. They are included here to help clarify statements made in the following sections of this article.

NC—automatic control of a machine tool by instructions input from a punched tape

CNC—automatic control of a single machine by instructions input from a dedicated computer; ability to perform much more complex functions is a major advantage over NC

DNC—automatic control of many machine tools by a single computer; major advantage over CNC is the elimination of dedicated computers at each tool while retaining the ability to perform complex functions at all tools.)

Is DNC for Everyone?

There was little, if any, disagreement on the value of DNC and the likelihood that its use would increase rapidly. All concurred that DNC was a very efficient and effective tool—but that it was not a panacea. Some companies could put it to use in certain applications, but only after lengthy evaluations of its advantages and disadvantages—and reviews of the time required before recovery of their investment. Standalone NC is not in danger of being obsoleted in the foreseeable future.

The great push for DNC in the machine tool field began in this country in late 1970 when several manufacturers displayed their systems at the International Machine Tool Show. However, according to Mr James J. Childs, president of James J. Childs Associates, a consulting firm, DNC has not yet proven itself. Comparatively few firms put DNC to use during that 5-year span, "and even some people that have it are a little concerned about whether or not it's the right route, whether or not it's cost-effective; and that's a little hard to prove sometimes. But, it's getting better all the time; it's got to improve. It's going to evolve. As soon as we get the software going and get the people educated . . . to get the link

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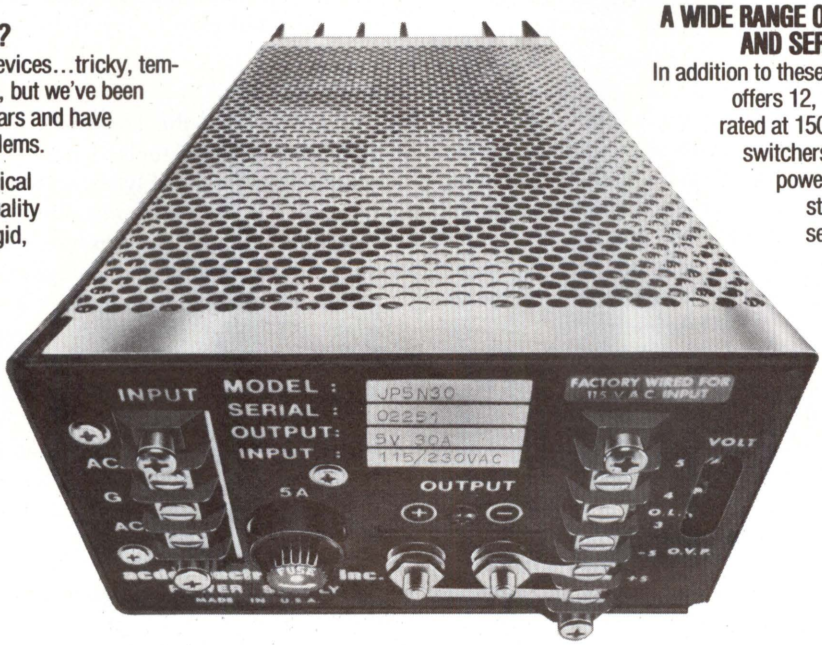

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CIRCLE 27 ON INQUIRY CARD

between the computer software and the manufacturing processes, I think then it's going to start."

As the panel moderator, Mr Robert Wilson, editor-in-chief of *Automotive Industries*, pointed out, just having NC eliminates most manufacturing operations. "If most of your manufacturing costs have to do with manual machines and machines with automatic cycles, DNC can't accomplish all that much for you. Even in an NC environment, parts may be simple, tapes may be quite short, and programming may be manual." In such cases DNC doesn't offer much advantage, certainly not enough to justify the costs involved. "Where DNC does look interesting though," Mr Wilson said, "is where there are complex parts to be programmed and machined, where there are engineering changes to be reckoned with, where there are quite a few part numbers, and where requirements for optimizing and editing tape calls for a powerful in-house APT-like processor." Another advantage is the automatic preparation of management information reports—but not all companies need or want such reports. Their value may not be equal to their cost.

DNC Case History

An example, presented by a representative of a company that recently placed a DNC system online, backed up Mr Wilson's statements. The trauma involved in justifying and selecting this system was described by Mr Richard Aggen, manager of tool and numeric design at Northrup Corp's Aircraft Div. Although the system was ordered in late March of this year, the company had been evaluating DNC since 1969. Because there won't be any hands-on experience to report until early in 1976, Mr Aggen could only discuss what criteria had to be evaluated, what preliminary decisions were made, how the system will be used, and what his company expects to gain from its use.

Based on results of an in-depth study started in 1969, it was decided that available systems did not have necessary capabilities and growth potential—and, in addition, were too expensive. However, in 1973, a new study team was formed to evaluate actual DNC installations in a variety of operations. This study showed that the technology had advanced to the point where DNC systems could be considered favorably for fabricating the complex parts used in the manufacture of aircraft.

Standalone NC—although relatively efficient—involved several major problem areas, with the editing of tapes probably one of the worst. The proving of tapes is quite involved and requires considerable man-hours of development, debugging, and testing. By the time a tape has been proven and used to make prototype and a few production parts meeting the required tolerances (typically within 10,000ths), a part modification order is received —and the whole process starts over again.

Mr Aggen says that "this is one of the areas where we expect to make substantial inroads by DNC. By editing the source program at the large computer directly on the shop floor, we hope to cut weeks and sometimes months out of this proving cycle." Since source programs are stored in the computer, it is not necessary to read the program in completely for every edit or update. Instead they load only the actual program lines that are to be changed. The computer accesses the job, updates it for the changes, and prepares a new tape.

This does not eliminate the problem of proving the new tape. However, Mr Aggen expects that procedures that have required several weeks in the past—because the machine tool was reassigned to a new job rather than being allowed to stand idle waiting for the edited tape—will soon be performed within minutes—before the job on the machine tool has been torn down.

Problem Areas

Another hands-on report of a DNC installation was made by Mr Jack Anderson, vice president, manufacturing, Shriber Div of Harris Corp. This organization had a DNC system installed and running even before the 1970 International Machine Tool Show. For the past four years the system has been operating successfully with 15 NC machine tools, and this has given management an opportunity to study "the good and bad" connected with DNC.

Mr Anderson believes there are two main problems inherent in DNC: high cost and lack of modularity. If the system includes a large computer, the cost must be spread over a large number of machine tools before it can be justified. Even if a minicomputer is used instead, a number of tools must be covered. Also, "DNC modularity, even though there are claims otherwise, has limited expandability without a sizable initial investment." Including a safeguard for "future planning" is not modularity; and it becomes very expensive if the user does not plan to use it for several years.

Summary

Unquestionably, the consensus of the panelists was that DNC for machine tools is here—and it can be used successfully and profitably. However, any company considering the possibility of installing DNC must allot a considerable amount of man-hours and funds to carry out thorough studies of advantages, disadvantages, and the likelihood of payback within a reasonable time. Even when otherwise successful, a system may not provide sufficient return on investment to warrant the initial outlay of funds.

In addition, if a DNC system is installed, at least one panelist, Mr Anderson, felt that it should be controlled by manufacturing personnel—not by data processing. The problems of DNC tend to be inherent in all manufacturing processes and can more readily be understood and solved by manufacturing personnel.

A major recommendation was that a mass storage control unit be developed. One solution would be to use economical and easily expandable random-access memory devices. Tying these to microprocessors would likely provide the relatively inexpensive and modular systems that are needed if DNC is to really become a standard in the machine tool industry.

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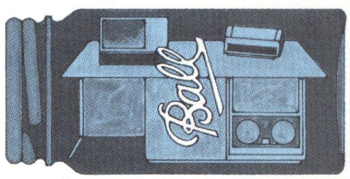
Answers to some tough questions on minicomputers—from systems to controllers to peripherals—published by Ball Computer Products, Inc., for pressured OEMs, hassled systems houses and puzzled end-users.

That's our name, all right. But probably not a fair question. Because Ball doesn't really make computers at all.

Minicomputer systems, yes. Peripherals, for sure. Controllers, indeed. In just 5 years, we've become the industry's largest independent supplier of controllers for Nova systems.



Mainly because we provide OEMs with strong technical support and service—things a lot of other companies figure you don't need.

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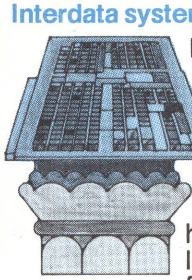

Ball has just announced a new line of disk controllers for Interdata Model 70, 74 and 7/16 mainframes. The new controllers have their own selector channel, and feature a built-in micro-programmable processor (designed and built by Ball, naturally) which permits us to program your controller to get more out of your hardware and software (answering the digital question, "Which costs less—smart programmers or smart controllers?").

These are probably the most sophisticated controllers ever designed—they support overlapped seeking, read-before-write, individual sector write protect an automatic data verification.

And yes, Va., they still fit in a single I/O slot inside the mainframe.

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The current craze for floppies is raising a lot of difficult questions. Like where's the cross-over point between hard and flexible disk systems? And are floppies better suited for recording computer data or destroying computer data?

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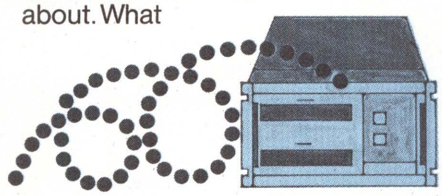

you do need to know about is that all those things give it performance and reliability previously available only on cartridge disk drives like the Ball 4300/4400.

Check it out . . . you'll flip.

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No failures. No downtime. No crashes. No sweat.

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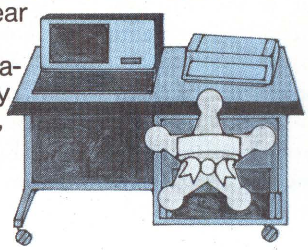

DMA Data Industries, the Paramus, N.J. OEM, reports that the system is being used to list outstanding warrants, retrieve arrest records, generate crime reports by type and location, and to retrieve microfiled mug shots and fingerprints.

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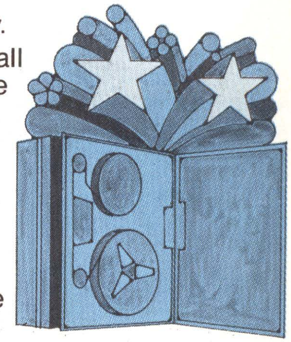

With the Ball 3180 phase encoded mag tape controller for Nova systems. Totally IBM compatible, the 3180 can interface up to 4 unformatted phase encoded Wangco, Pertec or other PE drives.

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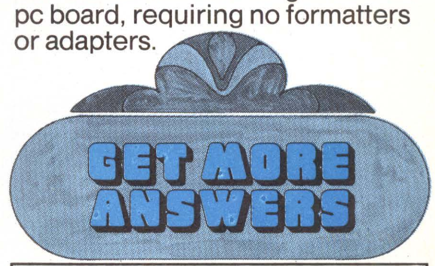

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Multiple-Chromatograph Systems Increase Capabilities by Computer Control

Chromatographic analysis of gas samples has been a standard in process industries for a number of years. Only relatively recently, however, have computers been sufficiently low in cost to warrant their use in controlling the analyzers. Once computerized chromatographs became practical they were used to both control the analyzer and manipulate the measurement data. As they became more sophisticated, computers were put to use as controllers for multiple-chromatograph systems—further justifying the cost of their inclusion.

An example of a current application is the Process Chromatograph Computer System supplied by Beckman Instruments, Inc, Process Instruments Div, Fullerton, Calif. This system uses a Digital Equipment Corp PDP-11/05 minicomputer to directly monitor and control up to 32 process chromatographs with associated single- or multiple-stream sample conditioning systems. All chromatographs are handled independently and simultaneously. Conventional chromatographic programmers are eliminated.

Various configurations of the chromatograph system are used by a number of petrochemical companies. However, not all use the full system. Many users supply their own computers, software, and other components (to the right of the dashed line in Fig. 1). In addition, earlier, less sophisticated systems with DEC PDP-8/I minicomputers and 16K words of memory could handle only a maximum of 20 analyzer units.

Process

Inputs from detectors (eg, thermal conductivity, hydrogen flame ionization, or helium ionization) are accepted by the system under software range control for operation at optimum gain for signal transmission level. High level signals from the chromatograph analyzers (Fig. 1) are directed, via the analyzer control and service panel, through a low pass filter to the multiplexer (MUX). There, each detector output is scanned at a rate of 10 samples/s. The analog-to-digital converter (ADC) changes each signal into digital form and sends it to the computer as a 14-bit word. Analyzer amplifier range is computer selectable with a range change decision made every 0.1 s (after each sample) so that the ADC is not affected by gain transition changes.

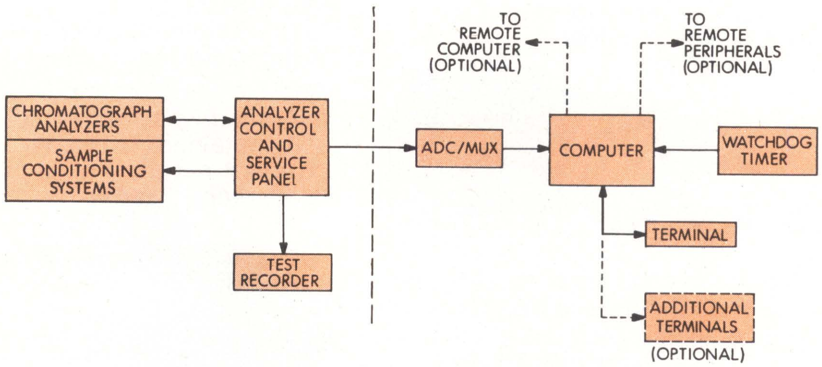
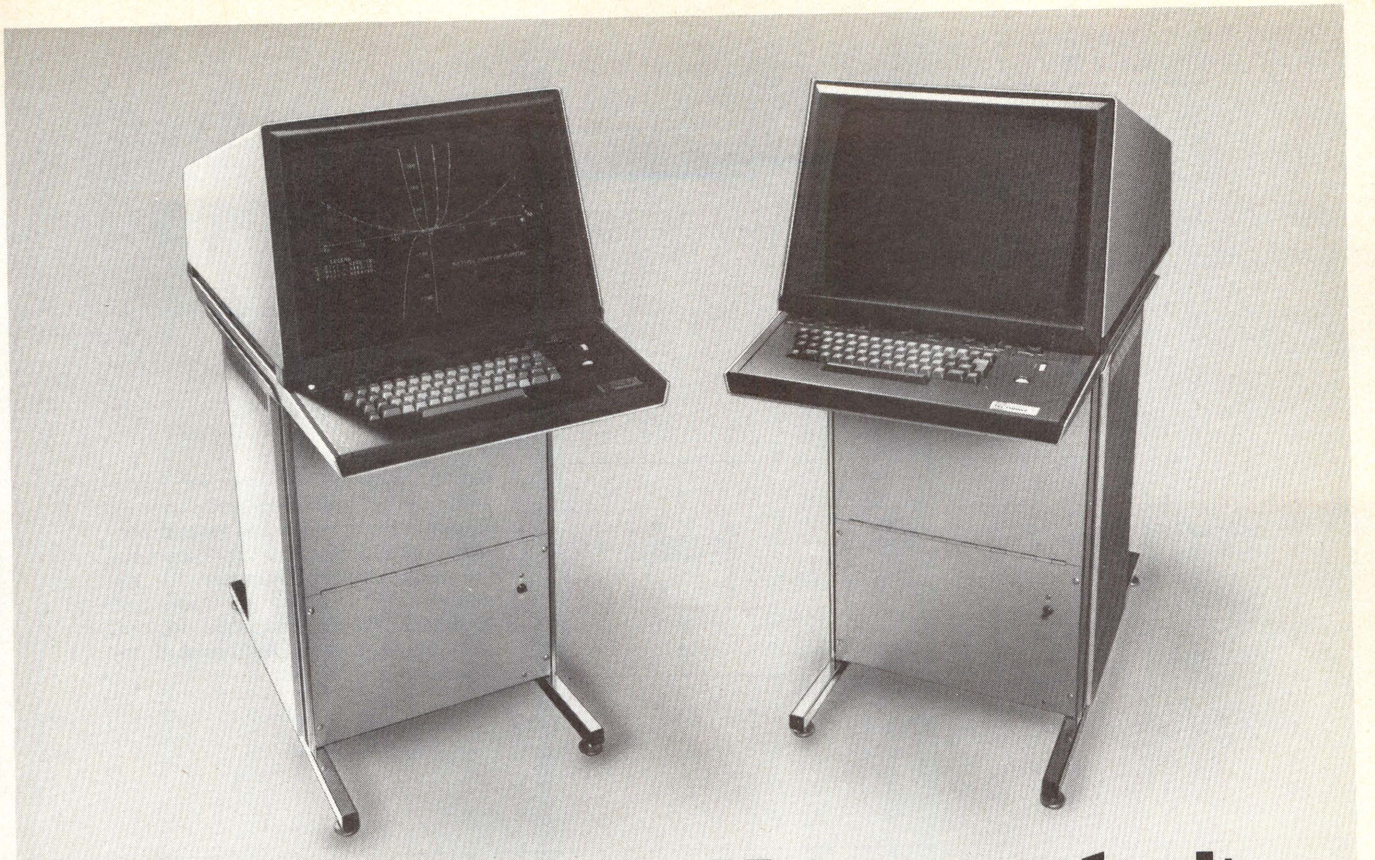


Fig. 1 Basic hardware component organization of Beckman Instruments' Process Chromatograph Computer System. As many as 32 analyzers can be controlled by a DEC PDP-11/05 minicomputer. Some users obtain only the components shown to the left of the dashed line and tie them into the other components within their own facilities. These users usually also provide their own software

The signal input system is a high speed, high accuracy data acquisition system. Multiplexer operation is at 20 kHz.

For startup, the analyzer control and service panel provides complete manual control over all analyzer and sample system sequential functions. This panel also serves as a termination point for field wiring and as a tool for isolating the analytical system from the computer during maintenance.

Basic functions of the computerized system are control of all sample inject and column switching valves as well as multiple stream and automatic calibration valves, monitoring of detector output and data reduction, automatic baseline correction for zero drift, and component identification and data presentation. However, the system's capabilities permit control functions



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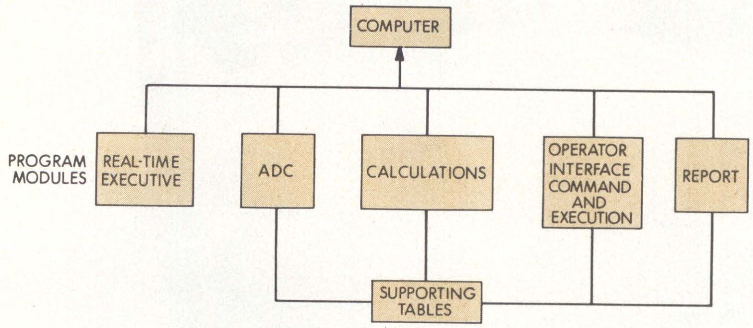


Fig. 2 System software for chromatograph monitoring and control. Five-module format of programs permits adaptation to the user's particular requirements. Support to the modules is provided by peak and sequence tables, response factors, component names, and related information

and computations which could not be achieved with conventional chromatograph programmers. These include material balance analytical calculations, simplified data presentation, auxiliary calculations, reduction of complete stream information for use by a host computer, automatic monitoring of the system for malfunctions, and dual status alarms on system performance for maintenance planning and fault isolation.

Computer System

Features of the PDP-11/05 include 12K words of 16-bit, 900-ns read/write core memory (expandable to 32K words for added system requirements); a set of over 400 standard instructions; real-time clock; direct memory access capability for multiple devices; hardware stacks that reduce programming time and save memory space; data communications interface; and terminal controller. Its 0 to 55°C operating temperature range at 10 to 95% relative humidity (non-condensing) fits conditions for process environments.

The computer uses microprogramming and Unibus® architecture for signal maneuvering to analyzer and peripherals. Standard peripherals that may be attached, dependent on individual system requirements, include teleprinters, paper-tape reader/punch, high speed line printer, card reader, magnetic tape units, rotating disc memories, plotters, and several types of displays.

Power failure protection is provided by a power fail and restart feature. If power to the computer fails, an interrupt occurs that causes the program to reset and save the registers before power is lost completely. Restart consists of setting all valves to "failsafe" mode and then allowing delay time for purge of the analytical system before starting a new analysis.

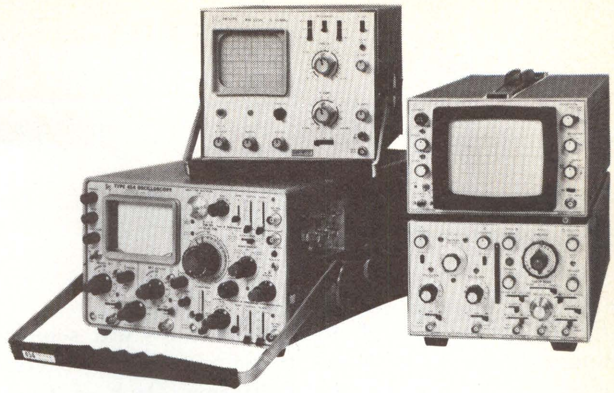
A watchdog timer is reset once each second by the computer. If a computer malfunction or interface failure prevents the computer from resetting the timer within 3 s, an alarm output is set. This causes all system solenoid valves to be reset to failsafe state, and an alarm message signals that the system is not operational. The failsafe condition prevents further samples from entering the analyzers.

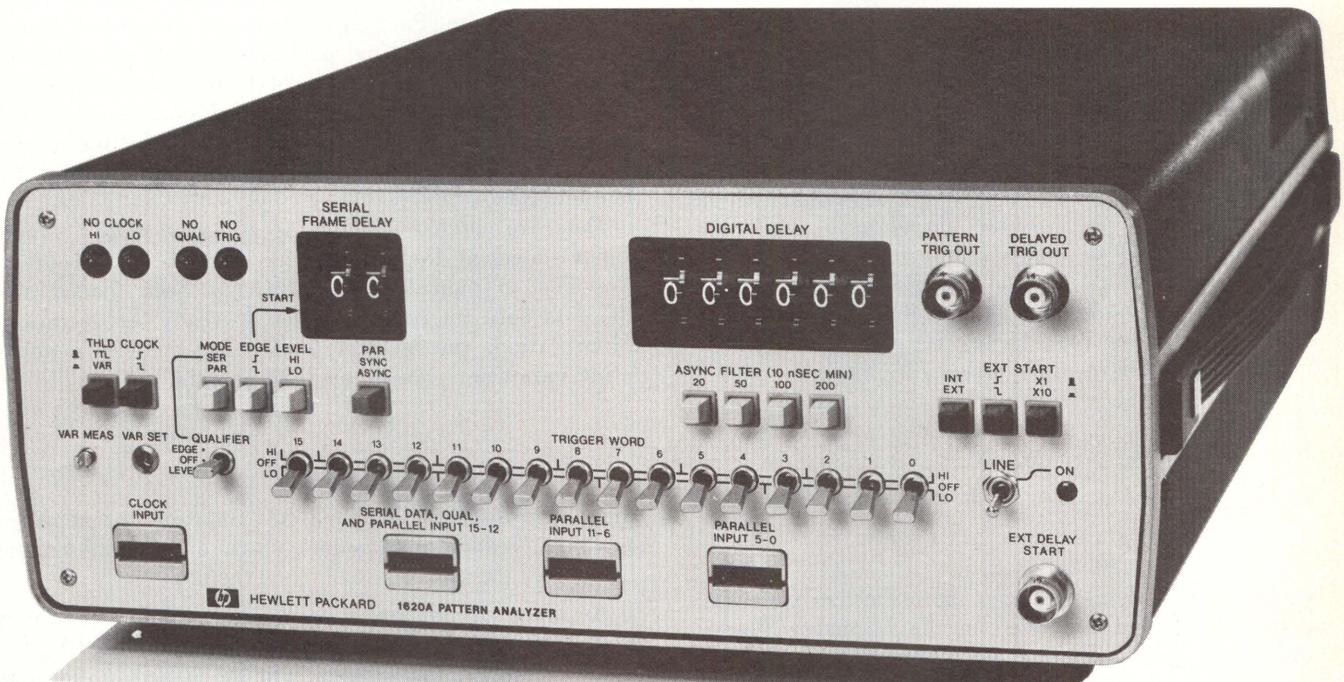
Software

Adaptation of system software to specific analytical requirements is eased by modular organization of the program. Five program modules (Fig. 2) consist of *real-time executive,* which controls all I/O functions, interrupts, updates time, and schedules job execution; *ADC,* which performs all data gathering, valve control, peak detection and resolution, baseline determination, and alarm checks; *calculation,* which performs peak area correction and all computations associated with the analyses; *OPCOM* (operator interface command and execution), which performs all operator communications functions and permits the operator to dynamically control system operation; and *reporting,* which performs all reports to printers, data output peripherals, trend recorders, and central computer.

Software sequence and peak tables provide identification and concentration for all components normally present in the process stream. Additional peaks resulting from process upsets are automatically measured and reported by the system. Monitoring and presentation of these "unknown" peaks provides information on the process operation and possible malfunctions.

Give your scope a word trigger





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With HP's new 1620A Pattern Analyzer and your present scope you can trigger on any digital word up to 16 bits. Whether your data is serial or parallel, synchronous or asynchronous. You simply preset the trigger word you want, and the pattern analyzer gives you a 2V, 25 nsec pulse when that word appears in the data stream.

The 1620A, with its pattern recognition ability, provides a dynamic window for viewing any digital circuit—at clock speeds up to 20 MHz. You can make real-time measurements on any part of your system... whether you're analyzing the data following the trigger word, another data stream, or some other event at that particular point in time.

You can also delay the trigger point up to 999,999 clock pulses after the word—in either serial or parallel mode. And if you have a long serial word to interrogate, the 1620A, with its qualifier input, lets you window on any portion of that word.

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For only $1,750* (including probes), you can turn your present scope into a digital troubleshooter and simplify your digital analysis problems. For more information about this newest member of HP's growing digital analyzer family, call your local HP field engineer. He can also give you information on HP's 4-bit AND-gate Trigger Probes for TTL, MOS, and ECL. Priced at just $95* each, they give you pattern recognition on four parallel events to trigger scopes, logic analyzers, or other digital test equipment.

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Microprocessors To Be Used in Traffic Signal Controllers

Ramps leading onto California freeways will soon contain microprocessor-based traffic signal controllers. A contract awarded by the California Dept of General Services to Honeywell Inc's Traffic Control Operation of Minneapolis, Minn calls for modems, communications terminals, control consoles, and programming systems in addition to the ramp controllers.

The microprocessors to be used are 8-bit devices —designed by the California State Highway Dept—that will operate in conjunction with 8000-word core memory. Instruction time for most operations will be about 2 μs.

Ramp signals will be actuated by either programs stored in memory or real-time measurement of traffic flow as determined by sensors imbedded in the traffic lanes. The company claims that advantages of the microprocessor-based system over those that use minicomputers include lower cost, higher reliability, and elimination of any requirement for air-conditioning.

Computer Programming System Eases Application Programming for Process Control

A "fill-in-the-forms" programming system, basically a set of standard routines that handle common process control functions without user programming, is claimed to virtually eliminate application programming for computerized process control. With ICAP (Industrial Control Application Package), users of Polstar computer systems enter operating parameters such as setpoints, limits, and alarms on standard forms, one column per loop. Then the data base is entered into the computer memory using a standard format written by the Taylor Instrument Process Control Div of Sybron Corp, Rochester, NY.

Data are entered serially for all loops with a simple input statement for each data type. Once the program, provided in punched-tape form, has been loaded and the data base entered, the system is ready for operation. Modifications can be made online and changes to operating parameters can be made at any time.

Data Acquisition System Expanded for Electrical Power Network

The amount of data that can be collected from its remote stations and processed at the Minnkota Power Cooperative's master station in North Dakota will be greatly expanded as the result of a contract recently awarded to Moore Systems, Inc, Sunnyvale, Calif. Present Digital Equipment Corp PDP-8 minicomputers with black and white CRT displays will be replaced by dual PDP-11/35 computers and color CRTs. Telemetering capabilities will be added at some existing remote sites and 23 remote stations will be added to the present network of 56 stations.

In the redundant system at the master station, one PDP-11/35 will operate online as the primary computer. The standby computer will automatically assume control if the primary computer fails.

System Automatically Diagnoses Gas Turbine Engine Maintenance Needs

A computer-controlled system delivered to the Public Service Electric and Gas Co of New Jersey by Hamilton Standard, Windsor Locks, Conn will be used to monitor performance and diagnose maintenance requirements of four gas turbine engines. Modular construction of the system, called Trends™, provides flexibility for handling additional engines if the need develops. The diagnostic tool is expected to improve maintenance practices, reduce maintenance costs, and extend engine life.

As many as 56 engine conditions will be monitored on a 24-hour basis; collected data will be analyzed by the system and printed reports will be issued to localize approaching maintenance needs and to warn of impending engine malfunctions—allowing corrective repairs to be made before possible catastrophic failure.

At a set time each day, or whenever the operator requests the information, the system will issue status reports on the performance of each engine—including measurements of each monitored condition, accumulated operating hours, and instructions for any required maintenance or repairs. Three types of messages will be issued: routine maintenance, to alert the operator that a scheduled preventive maintenance procedure is due; fault, when the system detects deterioration of engine performance and predicts the need for corrective action within 75 hr; and alarm, which is issued automatically whenever an engine operating limit is exceeded. This last message type will note the out-of-limit condition and provide a 5-min. history of events leading up to the problem.

Basic components of the system include a set of sensors for each engine to collect data and convert them into electrical signals, a data collection unit for each two engines which receives the electrical signals and converts them into digital form, and a central computer and data processing unit that can analyze information from as many as 50 engines. □

think General Instrument

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CIRCLE 32 ON INQUIRY CARD

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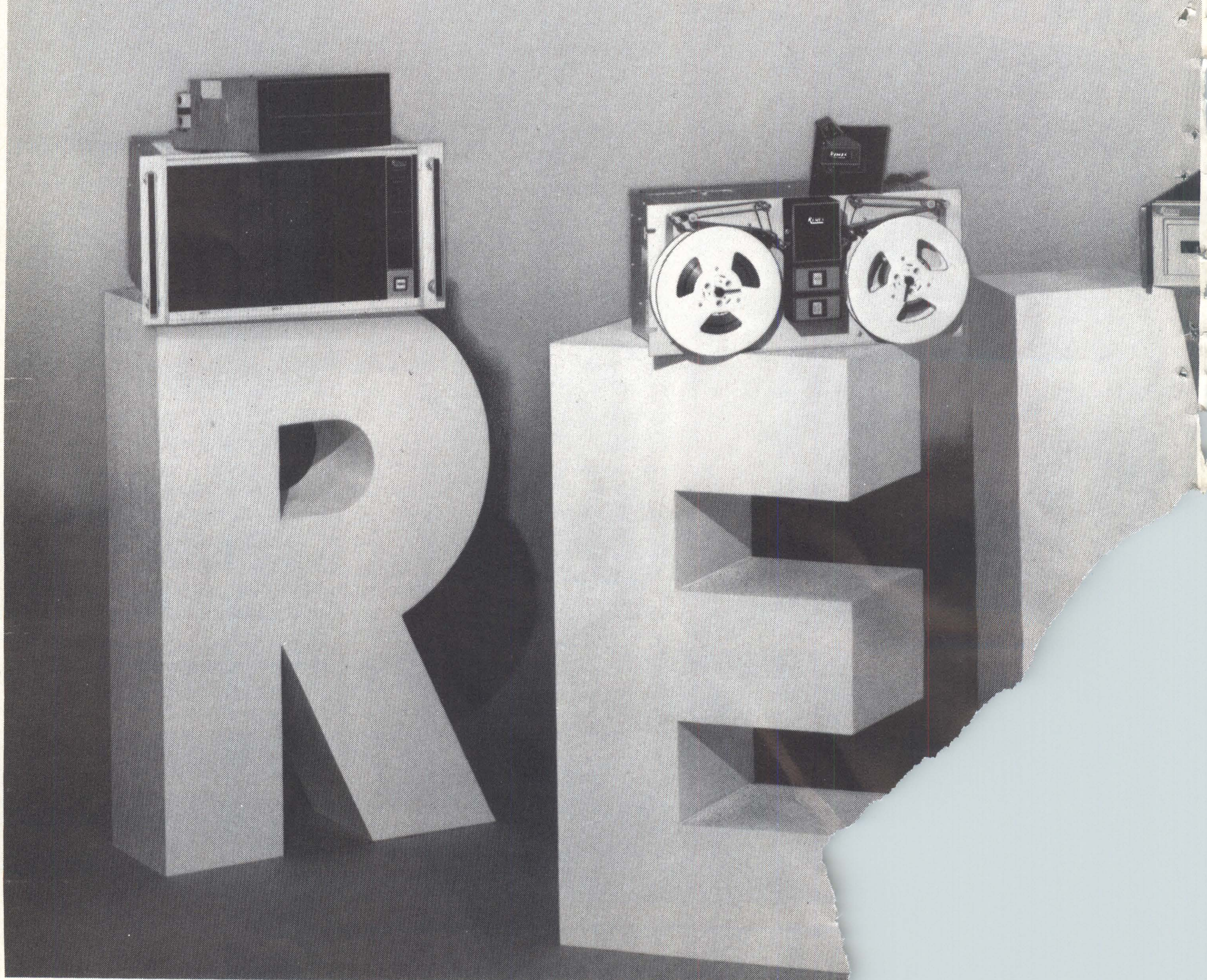

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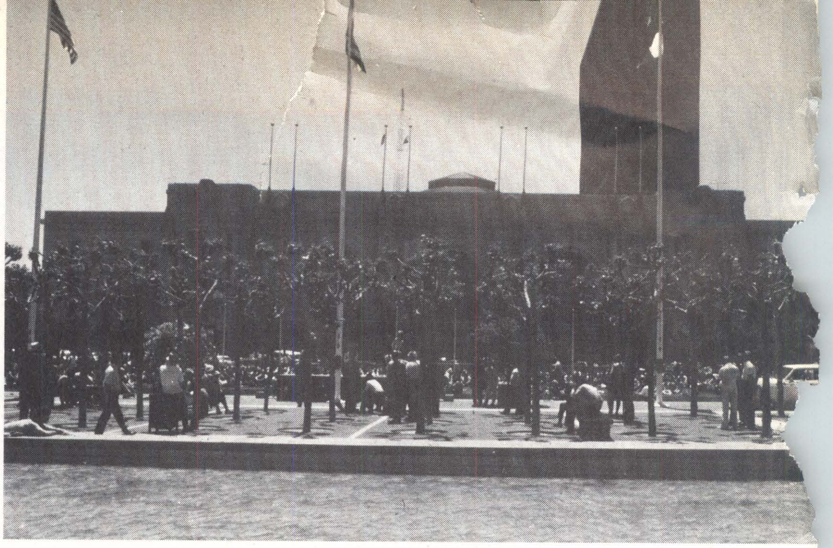
Electronics in the next thousand days



Brooks Hall/Civic Auditorium
San Francisco, California
September 16-19

Emphasizing needs, trends, and applications of electronics technology, the 24th Annual Western Electronic Show and Convention, co-sponsored by Northern and Southern California Chapters of the Electronic Representatives Association and by the Los Angeles Council and San Francisco Section of the Institute of Electrical and Electronics Engineers (IEEE), will consider "Electronics in the Next Thousand Days." Under the direction of co-chairmen Alan Mitchell, Hewlett-Packard Co, and Andrew Nalbandian, Lockheed Missile and Space Co, the Professional Program will consist of 32 half-day sessions running concurrently over the 4-day period in Civic Auditorium; approximately 275 exhibitors will occupy downstairs Brooks Hall.

Alan Mitchell
Co-Chairman
Professional Program

Andrew Nalbandian
Co-Chairman
Professional Program

Special Activities

Opening day, Tuesday September 16, the WESCON Luncheon will feature Daniel A. McMillan, publisher of *Electronics* magazine, who will give the keynote address. On Tuesday evening, WESCON will host the All-Industry Reception, and on Thursday, September 18, the all-day Distributor-Manufacturer-Representative Conference will be held. All events will take place at the St. Francis Hotel on Union Square.

On Wednesday evening, researchers, led by Dr Thelma Moss of the UCLA Neuropsychiatric Institute, will present their work in Kirlian photography, bioenergy phenomena, and unorthodox therapeutic techniques.

During all show hours, "Bayshore Flyer" bus commuter service will operate between Palo Alto and the Civic Center, with free parking at the Cabana Hyatt House. Within San Francisco, shuttle bus service will link the St. Francis Hotel and key BART stations to the Civic Center.

Exhibits

In Brooks Hall—one floor down from the Civic Auditorium—the display area will house approximately 275 exhibitors. Grouped into areas devoted to Components and Microelectronics; Computers, Peripherals, and Communications; Electronic Packaging and Production; and Instruments and Instrumentation, booths will be open from 9:30 am to 5 pm on Tuesday and Thursday, 9:30 am to 9 pm on Wednesday, and 9:30 am to 4 pm on Friday.

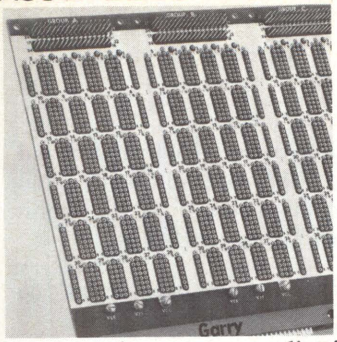
Registration

Registration will take place at Civic Auditorium during Convention hours. A $5 fee will cover Exhibits and the Professional Program. Each visitor will receive an embossed plastic Jacquard Inquiry Badge, which will serve both for admission and as an inquiry "credit card."

Professional Program

Aimed at the "next thousand days in electronics," sessions will address needs, trends, and applications of electronic technology in the next 30 months. Major emphasis is on computer-related components and semiconductor technology. Several sessions deal with automated test equipment; others with computer-aided design; and one focuses on SDLC data transmission. Only sessions of particular interest to *Computer Design* readers are covered here; information is necessarily limited to that available at press time.

NEW I.C. PLUGGABLE ECL PACKAGING ASSEMBLIES FROM GARRY MFG. CO.



A new product line designed specifically for pluggable wire-wrap packaging of high-speed ECL I, ECL II and ECL 10,000 logic series has been announced by Garry Manufacturing Company.

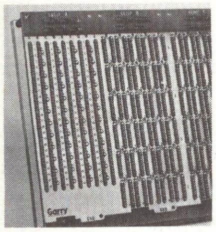
The packaging system incorporates a three layer low impedance power distribution system for both commercial and military applications. The commercial design utilizes a laminated third voltage plane, while the military design incorporates a true multilayer board fabricated to MIL-P-55640. Signal interconnections are completed with standard wire-wrap techniques.

The ECL Series Pluggable Packaging Assemblies are available in standard configurations or are supplied to custom requirements.

For complete information, call collect or write Garry Manufacturing Company, 1010 Jersey Avenue, New Brunswick, N.J. 08902. Phone: 201 545-2424

CIRCLE 72 ON INQUIRY CARD

DESIGN & ECONOMY ADVANTAGES IN NEW MIXED PATTERN BOARDS FROM GARRY

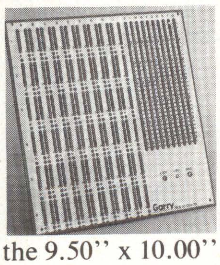


A new standard model Mixed Pattern Board from Garry Manufacturing Company permits the combination of designated 14-pin and 16-pin DIP's with a universal pattern for MSI and LSI DIP's — thus eliminating the need to buy universal patterns throughout. The boards are available with a universal section of 9 58-pin columns, and up to 210 positions in multiples of 30, for 14-pin and/or 16-pin DIP's.

For complete information, call collect or write Garry Manufacturing Company, 1010 Jersey Avenue, New Brunswick, N.J. 08902. Phone: 201 545-2424.

CIRCLE 73 ON INQUIRY CARD

NEW RAM PLUGGABLE PACKAGING ASSEMBLY FROM GARRY



Garry Manufacturing Company is now delivering a standard multilayer wire-wrappable I.C. pluggable packaging assembly for the 4K RAM solid state memory chip. Offering significant design and economy advantages when both RAM and standard chips are used, the 9.50'' x 10.00'' packaging assembly contains provisions for mounting 54 units of the 22-pin 4K RAM chip, plus a universal pattern capable of mounting 40 standard 14-pin or 16-pin DIP's. The voltage distribution plane on the component side of the assembly is designated as V_{CC}, the internal plane is V_{DD}, and the plane on the wrapping side is the V_{SS} plane. Delivery is off-the-shelf to 4 weeks.

For complete information, call collect or write Garry Manufacturing Company, 1010 Jersey Avenue, New Brunswick, N.J. 08902. Phone: 201 545-2424.

CIRCLE 74 ON INQUIRY CARD

TECHNICAL PROGRAM EXCERPTS

Tuesday Morning

Session 1 — 10 am-12:30 pm — Room 105

Microcomputers—How Do I Get Started?

Organizer/Chairman: Jonathan A. Titus, Tychon, Inc, Blacksburg, Va

To familiarize engineers with some approaches to using microcomputers, specific real experiences with commercially available and do-it-yourself systems are related. Eugene R. Fisher, Lawrence Livermore Laboratory, discusses microcomputers as systems elements and how high-level languages aid program preparation; David G. Larsen and Peter R. Rony, Virginia Polytechnic Institute and State U, present an approach to interfacing and breadboarding, using the Intel 8080 to teach microprocessor application; and Ed Lee, Pro-Log Corp, gives easy-to-use design steps for using logic processors in control applications. Specific approaches to multiple microprocessors in a system are detailed by Dr Robert L. Britton, California State University at Chico, along with practical considerations and design ideas and limitations.

Session 2 — 10 am-12:30 pm — Room 103

Sources of Capital in Difficult Times

Organizer/Chairman: Christian Hoebich, Hoebich Venture Management, Palo Alto, Calif

Commercial loans are difficult to obtain and venture capital is even scarcer, forcing emerging companies to look elsewhere for money to build their futures. Christian Hoebich, Hoebich Venture Management; David G. Arscott, Citicorp Venture Capital Ltd; Nolan Bushnell, ATARI, Inc; Clifford A. Morton, San Francisco District Small Business Administration; and William F. Plein, Commonwealth Financial Corp, make up the panel which will discuss alternate sources of capital and how to obtain them.

Session 3 — 10 am-12:30 pm — Room 104

Instrument Interfacing with the IEEE Standard Bus

Organizer/Chairman: Donald C. Loughry, Hewlett-Packard Co, Palo Alto, Calif

Providing a common method for interconnecting programmable instrumentation, IEEE Standard 488-1975 specifies mechanical, electrical, and functional elements of an interface system. Organization, relationship, and essential capabilities of the interface functions are discussed by Daryl E. Knoblock of Hewlett-Packard's Data Systems Div, with emphasis on options which give designers a second degree of freedom. Richard C. Lee applies a 4-bit microprocessor to an interface to provide internal processing and achieve a design satisfying requirements of instrumentation systems. Practical considerations beyond the scope of the standard are defined by Tom Coates, Hewlett-Packard's Santa Clara Div, along with guidelines for choosing control codes; John Fluke, Jr, John Fluke Manufacturing, focuses attention on software considerations of the interface scheme. C. Bruce Clark, Stanford Research Institute, and David J. Sager, University of California, will be on hand to critique the papers and make observations on technical implications, benefits, trends, and needs.

Session 4 — 10 am-12:30 pm — Room 106

Computer Aids for LSI Design and Tooling

Organizers: Donald E. Barnes and Thomas L. Davis, Topanga Data Systems, Chatsworth, Calif

Focusing on available concepts, procedures, software, and hardware to improve design and development time, reduce tooling costs, and provide increased documentation control, this session discusses all aspects of design and tooling, from layout to final mask and acquisition of circuit analysis data. Computer-aided design and pattern generation are covered by T. Grod, L. Woods, and G. Hendricksen of Electromask; Macrodata's Ivan Dobes and Ron Byrd describe a preprocessor program capable of recognizing si-gate transistor geometries; and graphics layout systems for faster tooling are the subject of Donald E. Barnes and Thomas L. Davis of Topanga Data Systems.

Session 5 — 10 am-12:30 pm — Room 321

Telephone Private Branch Exchanges (Electronic PBXs)

Organizer/Chairman: Albin R. Meier, *Telephony* Magazine, Chicago, Ill

Emphasizing capabilities of representative electronic PBXs and their effect on user and telephone company, this session highlights design philosophy as it affects engineering design decisions and market considerations. Jim Kasson of Rolm reviews design and application details of a recently announced computer-controlled PABX; Harry Lewenstein, Farinon Electric, illustrates how electronic PBX features can provide previously unavailable services. The systems' effects on the user are analyzed by O. R. Frederiksen of Bechtel Corp; Curtis Week, AT&T, Denver, speaks on "The Dimension System; and Thomas Patsign, Chestel Inc, concludes the session with details on how the systems fit into the PBX marketplace.

Tuesday Afternoon

Session 6 — 1:30-4 pm — Room 105

Microprocessor/Microcomputer Hardware and Software Support Systems

Organizer/Chairman: Ralph Martinez, Naval Electronics Laboratory Center, San Diego, Calif

In discussing advantages and disadvantages of current methods for generating and testing microprocessor software/firmware, attention is focused on those features that future support systems should have to minimize development time and costs. An historical overview of microprocessor/microcomputer hardware and software support systems, presented by Ralph Martinez, Naval Electronics Laboratory, provides background for the

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CIRCLE 35 ON INQUIRY CARD

views on advanced software expressed by Gerry Madea of National Semiconductor, who considers what software tools are required, what hardware is necessary for prototyping, and what additional hardware is necessary to support the software tools. According to Granino Korn, University of Arizona, applications-oriented nonprogrammers can generate efficient microcomputer programs without learning assembly language with a minicomputer-based programming system that permits interactive simulation of microcomputer program execution.

J. E. Bass, Rockwell International, considers the impact that distributing intelligence among multiple chips within a microcomputer system will have on system organization, software structure, and programming requirements, illustrating the concepts with an example of an intelligent CRT terminal. How wasted effort and delays can be eliminated by permitting the software designer to work with actual prototype hardware as it is being designed is described by Mike Maerz and Paul Rosenfield of Intel. Robert Van Naarden of Digital Equipment emphasizes the cost-effectiveness of microcomputers in application areas, centering on the "make or buy decision" and covering tradeoff decisions related to concepts of "overkill" for future growth versus compatibility.

Session 8 | 1:30-4 pm | Room 104

Packaging and Interconnection Considerations in the Use of State-of-the-Art Integrated Circuits

Organizer/Chairman: Allison C. Danzig, Photocircuits, Glen Cove, NY

Intended to inform engineers of major areas in packaging and interconnections which are affected by new IC designs and parameters, this session deals with four specific areas where the increased functions per chip and higher speed logic must be considered. Problems of pattern layout, manufacturing processes, and tolerances associated with complex, 2-sided circuit boards are discussed by Sam Smookler, Photocircuits, with respect to their effect on initial cost and final assembly reject rates. Implications of high speed logic on connectors, cabling, and hardware in equipment design are outlined by AMP's Richard Patrick and William Schumacher; heat dissipation requirements of current ICs are covered by Kenneth Garcia, AIL Div of Cutler-Hammer; and R. P. Burr and Joseph P. Hammond, Photocircuits, discuss electrical problems posed by high speed TTL and ECL circuits, and the advantages/disadvantages and performance characteristics of various interconnection techniques.

Wednesday Morning

Session 10 | 10 am-12:30 pm | Room 105

Microprocessor Applications

Organizer/Chairman: Roy Forsberg, *EDN* Magazine, Boston, Mass

Detailing the integration of microprocessors into finished products, session outlines key steps and decisions, and points out some detours. Histories are presented on an Intel 8080-based floppy disc system (Gary A. Kildall, Intel), a blood sample analyzer based on National Semiconductor's 16-bit chip set (Mike Cope, Interphase Associates), and a communications processor using the Motorola M6800 (Don Kavar, TRW Data Systems). Bob Cushman of *EDN* magazine will demonstrate how to get started with microprocessors for a few hundred dollars.

Session 11 | 10 am-12:30 pm | Room 103

Fielding a Winning Sales Team

Organizer/Chairman: Larry Courtney, Courtney/Wilson & Price Advertising, Calabasas, Calif

Every manufacturer of electronic equipment must, after deciding on a sales format, formulate a means of communicating, monitoring, and reviewing his approach, and making necessary changes. These points are discussed by a panel made up of Jerry S. Frank, Industrial Marketing Association; Larry Courtney, Courtney/Wilson & Price Advertising; Frank Burge, Regis McKenna Advertising; and Bob McColloch, Bourns Labs.

Session 13 | 10 am-12:30 pm | Room 106

Automating Test Generation—Answers to the Explosion in Digital Test Programming

Organizer/Chairman: Donald P. Allen, Fluke Trendar, Mountain View, Calif

Programming costs for bringing automatic test equipment online have long surpassed equipment costs, requiring that specific hardware and software changes be made to lower them. Robert E. Anderson, Omnicomp, surveys current test generation techniques, presenting advantages and disadvantages. Bruce Pomeroy, Digitest Corp, discusses steps that have been taken toward automatic stimulus generation as an alternate approach. The shared system approach is discussed by William C. Garrignes, Hughes Aircraft, while Noel P. Lyons, Fluke Trendar, considers a microcomputer approach.

Session 14 | 10 am-12:30 pm | Room 321

Energy Policy Decisions in the Next 1000 Days—Opportunities and Uncertainties for the Electronics Industry

Organizers/Chairmen: Ed Kyser, Systems Industries, Sunnyvale, Calif; and John Eidson, Hewlett-Packard Laboratories, Palo Alto

Local, state, and national level decisions on fundamental energy policies will have great impact on the industry, affecting design criteria of products from the perspective of efficiency and energy consumption. Offering a prediction of electric power's future is Richard L. Post, Lawrence Livermore Laboratories; Garry G. Williams of Stanford's Graduate School of Business attempts to access the effects of policy decisions on availability and consumption and on economic growth. Marketing considerations and other problems created by the legislation are topics for Donald F. Lundgren, an attorney, and Paul C. Valentine of Spaeth, Blase, Valentine & Klein. The case for conservation is presented by Gail Boyd, Woodward-Clyde Consultants, and R. Michael Evans of Acurex Corp; Glen Bacon of IBM's General Products Div and Malcolm McWhorter of Stanford University present "Electronics—An Alternative to Energy Consumption," and Willis W. Harman of Stanford Research Institute surveys probable futures.

Wednesday Afternoon

Session 15 — 1:30-4 pm — Room 105

New Developments in Microcomputer Design Aids and Logic Analyzers and Recorders

Organizer/Chairman: Frank Burge, Regis McKenna, Inc, Palo Alto, Calif

Test and design aids have become available to ease the transformation of logic designers into logic programmers. In his overview, Dr William Davidow, Intel Corp, briefly covers some equipment that will enable software development to be performed in high level English-like languages. The EXORciser, designed for use with the M6800 family of microcomputer devices, permits software development with actual system peripheral hardware under real-time conditions, as detailed by Van C. Lewing, Motorola Semiconductor. Jim Lally, Intel Corp, describes the Intellec[R], a processor-independent development system, which can be specialized to a particular microcomputer system with a plug-in chip-emulator module. System debugging can be greatly simplified through use of a logic state analyzer such as that detailed by Bruce Farley of Hewlett-Packard, and currently available logic recorders can provide timing diagrams with CMOS, TTL, and ECL signals (Roy Tottingham, Biomation).

Session 16 — 1:30-4 pm — Room 103

Engineering vs Purchasing: The Limits of Responsibility

Organizer: Glenn A. Ford, United Technologies, Sunnyvale, Calif

Moderator: David Steinberg, GTE/Lenkurt, San Carlos, Calif

Respective roles of engineering and purchasing will be debated by a panel composed of two engineers and two purchasing people, focusing on responsibility for economic objectives, quality adherence, meeting time-frame requirements, vendor contacts, and sourcing. Among panel members will be Edward P. Stone, Vidar, Div of TRW; Charles E. Totoritis, Varian; E. Karl Freytag, Lawrence Livermore Laboratories; and John Pullman, Applied Technology, Div of Itek.

Session 18 — 1:30-4 pm — Room 106

Synchronous Data Link Control (SDLC)—Teleprocessing Tyranny or Plug-Compatible Progress

Organizer/Chairman: Saroj K. Kar, Telecom Computer Technology, Sunnyvale, Calif

Indications show that SDLC will be the only serial-by-bit data transmission protocol that IBM will support. In his introduction, Saroj K. Kar, Telecom Computer Technology, presents sound technical reasons for adopting the transmission method and details on future teleprocessing requirements that may make other methods impractical. The panel, consisting of two users (to be announced, Bank of America, and Ronald Wheeler, Fireman's Fund Insurance) and two manufacturers (William H. Bridges, Memorex, and L. Barton Alexander, Four-Phase Systems), will present their views of the pros and cons of SDLC for their specific fields, and Robert F. Wicksham, Vantage Research Services, will forecast the marketing impact of the method on teleprocessing equipment and related components.

Thursday Morning

Session 19 — 10 am-12:30 pm — Room 105

I²L and CCD Applied

Organizer/Chairman: Jerry Metzger, IC Update Master, Sunnyvale, Calif

I²L logic and CCD memories will have a significant effect on system organization because of their speed and density. To explain the effect that these characteristics will have on designs, Stan Bruederle, Signetics Corp, describes an IBM-compatible SDLC universal synchronous transmitter/receiver. Bob Ruth, Motorola Semiconductor, considers additional applications made possible by density of I²L logic in bipolar LSI circuits. Practical information on the use of a 16-kilobit CCD memory in a 1-megabyte memory system is presented by Dave House, Intel Corp, who describes its operation, applications, and optimum system organization. Benefits to be gained from using a CCD line-addressable memory are covered by Kamal Gunsager, Fairchild Semiconductor.

Session 21 — 10 am-12:30 pm — Room 104

So You Want a Printer for Your Mini- or Microcomputer System?

Organizer/Chairman: David N. Kaye, *Electronic Design* Magazine, Los Angeles, Calif.

System designs using microcomputers require different selection criteria and interfacing methods for printers than those using minicomputers. Selection differences are enumerated by Ted L. Nichols of General Automation, who will evaluate units based on performance, reliability, and price in light of the rapidly changing technology. Various techniques of accomplishing the hardware/software interface are discussed by Paul Davies, Educational Data Systems, with emphasis on desirable characteristics for maximum throughput. The session concludes with description and demonstration of a microprocessor-controlled serial printer (David Ratcliffe, Interdata) and a medium-speed matrix line printer (David W. Mayne and Gordon B. Barrus, Printronix).

Session 23 — 10 am-12:30 pm — Room 321

Promoting Women? What's the Problem?

Organizer/Chairman: Esther H. Williams, Lockheed Missiles and Space Co, Sunnyvale, Calif

Giving the audience an opportunity to actively air their concerns and receive suggestions for solving their problems, the panel will discuss stereotyping, implementing training programs, and recruiting problems, as well as hidden concerns that hinder the promotion of women. Included on the panel are James Harper, Tektronix Inc; Carolyn Morris, Hewlett-Packard; Dr Stuart O. Parsons, Lockheed Missiles and Space Co; and Jean Wright, Dept of Defense.

Thursday Afternoon

Session 24 — 1:30-4 pm — Room 105

Organizer/Chairman: Fred J. Weibell, Veterans Administration Hospital, Sepulveda, Calif

Current interest in microprocessors and their possible applications includes the field of medical instrumentation. Special factors involved in interfacing a microprocessor to medical instruments are considered by Paul Mitzen, Beckman Instruments, while Randolph S. Carlson (Beckman) presents some design criteria for microprocessor-based instruments. Potential applications such as patient monitoring systems and diagnostic health care as well as other instruments are explored by Radha Ramaswami, Xerox Corp, and Erich A. Pfeiffer, Biomedical Engineering, VA Hospital.

Session 25 1:30-4 pm Room 103

Hybrid Microelectronics Clinic on Beam-Leaded Devices and Automated Assembly Technology

Organizers/Chairmen: Stanley M. Stuhlbarg, Hughes Aircraft, Fullerton, Calif; and Dr William B. Burford, Westinghouse Aerospace, Baltimore, Md

Examining the increasingly controversial questions related to device availability, mechanical dimensions, handling/testing techniques, reliability, producibility, and costs, the panel deals separately with in-situ beam leads and the emerging tape-mounted beam lead device technology as it relates to automated assembly of hybrid microcircuits. Members of the panel are Jack J. Degan, Bell Laboratories; John Kanz, General Dynamics; Gus W. Krause, Sandia Laboratories; Jerry J. Mazenko, Hughes Aircraft; and Bernard Reich, US Army Electronics Command.

Session 26 1:30-4 pm Room 104

Field Programmable Logic

Organizer/Chairman: Jack Kompan/J. A. Perri, Harris Semiconductor, Melbourne, Fla

Actual and projected uses of programmable-ROMs, PLAs, and microprocessors as logic replacements form the subject matter of this session. Economic, logistic, and testing advantages and disadvantages are highlighted by Chris Clare, Hewlett-Packard Co, who identifies design aids, simulation techniques, and software support for each participating technology. Insight on FPLA utilization limits is provided when Gene Miles, Intersil, discusses design system partitioning, breadboard simulation, and PLA expansion techniques. Selection of devices is influenced by architecture and system partitions; Mike Groff, Harris Semiconductor, considers these boundaries as well as the marriage of programmable-memory PLA and microprocessors to overlap those boundaries. To conclude the session, the speakers will be joined by Don Bryson of Intel Corp and Dr J. A. Perri of Harris Semiconductor for a panel discussion covering "Trends in Memory Logic Replacement."

Session 27 1:30-4 pm Room 106

Automatic Testing in the Manufacturing Process

Organizer/Chairman: George King, LeAnce & Reiser, Newport Beach, Calif

Difficult testing problems are presented to both maker and user by today's LSI IC devices—particularly microprocessors—and LSI circuit board assemblies. Three facets of the problem are covered from the standpoint of equipment, technology, and required tests. Dan Izumi of National Semiconductor describes manufacturers' problems in testing LSI before and after manufacture. James Campbell, Fairchild Systems Technology, details a real-time function-test generation system for testing complex

LSI; and Abraham Armoni, Computer Automation, outlines programming and fault isolation aids for automatically testing logic assemblies.

Session 28 1:30-4 pm Room 321

International Business Cookbook: Four Recipes for Success

Organizer/Chairman: Fred Glynn, Marketing Research, San Francisco, Calif

Providing manufacturers and marketers with up-to-date information on problems encountered when dealing with foreign firms, this "how to" session provides useful information on protecting patents and trademarks (Roger Borovoy, Intel), and methods for determining the size of a potential market (Fred Glynn, Marketing Research). Also covered are avoiding potential government red tape (Rauer Meyer, US Dept of Commerce) and selecting a foreign manufacturing plant for optimum financial advantage (Gunnar Hurtig, KTI Div of Baldwin Electronics).

Friday Morning

Session 29 10 am-12:30 pm Room 105

Present and Future of Sophisticated Pocket Calculators

Organizer/Chairman: Rudolf Panholzer, Naval Postgraduate School, Monterey, Calif

Exploring engineering design aspects, software questions, and market trends, this timely session attempts to clarify the situation created by the rapid developments and changes in the field. Discussion of the HP-65 (Roy Martin, Hewlett-Packard) serves as introduction to concepts of calculation and programmability and details firmware and card reader functions. Increased sophistication of calculators as spurred by discriminating selection is reviewed by Mike Cochran, Texas Instruments, who goes on to point out future trends, such as customized features, and upcoming innovations such as input/output. Cost reduction through tradeoff with sophistication has been the key to increased sales. Robert B. Johnson, National Semiconductor, describes what the future may bring; Richard J. Nelson, Statek Corp, attempts to define the user and predict what he will demand of future machines. Larry Wells, Creative Strategies, Inc, looks at the market, evaluating current applications, market penetrations, and trends toward calculators tailored to specific user categories.

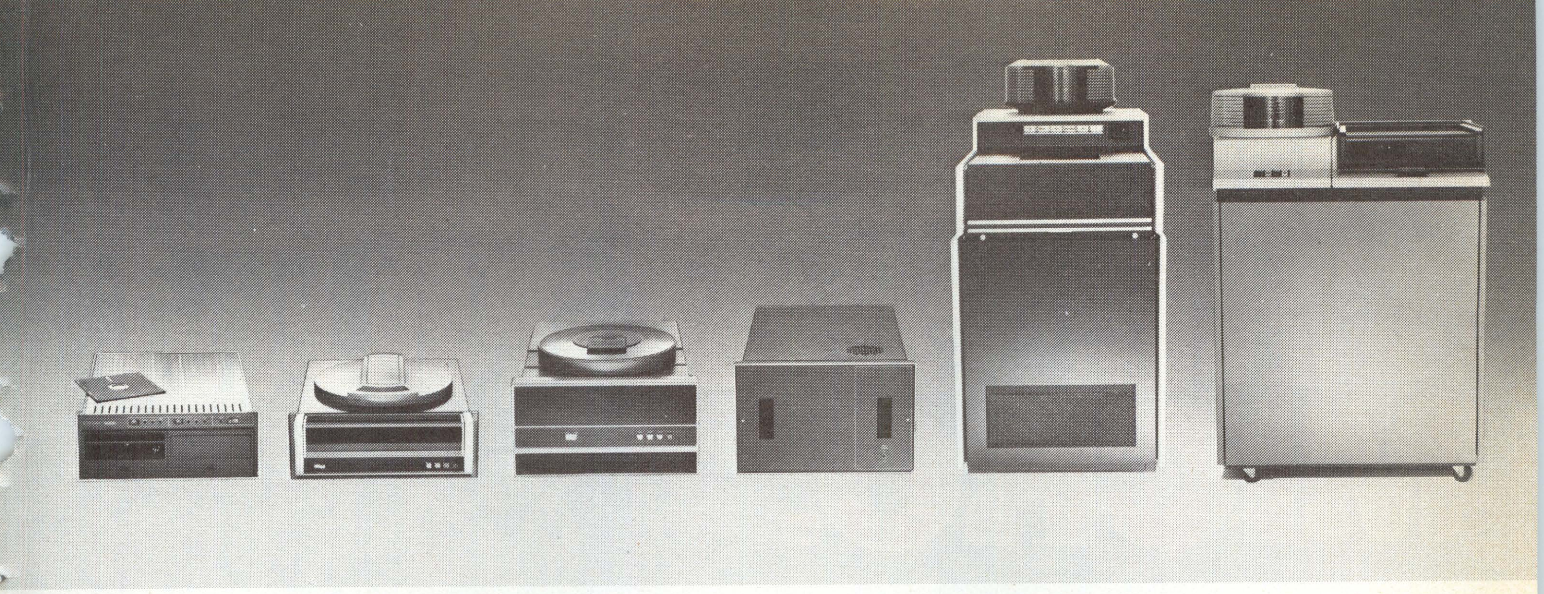
Session 30 10 am-12:30 pm Room 103

The Engineer and His Profession

Organizer: Roger Dorr, High Frequency Engineering Co, Portola Valley, Calif

Co-Chairmen: Roger Dorr, High Frequency Engineering; and Jack Nawrocki, Aeronutric Ford, Palo Alto, Calif

Update on the engineering profession covers the present status of electronics engineering (Roger Dorr, High Frequency Engineering), the current engineering supply and demand situation in general (Robert A. Rivers, Aircom Inc), and the changing picture regarding expanding engineering responsibilities (Dr Alan C. Nixon, Chemical Consultant). □



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CIRCLE 40 ON INQUIRY CARD

Networks that learn are useful in computer-aided design and manufacturing to improve process performance, reduce costs, and decrease the need for engineering analyses. Here's how they learn and how they are applied

Learning Networks Improve Computer-Aided Prediction and Control*

Roger L. Barron

Adaptronics, Incorporated
McLean, Virginia

A quiet revolution is spreading in the way that engineers think about manufacturing processes. In the past, these processes were designed and operated on the basis of either doctrinal or engineering concepts. Analysts and engineers have attempted to write instructions for control computers in the same way that they instruct human operators in how to perform appropriate manual control functions. Thus applications of computer-aided manufacturing during the first two decades of the computer era have consciously or unconsciously taken the form of one-for-one replacements of human operator functions by equivalent computer functions. This concept of replacement has maintained or even reinforced traditional reliance on analytically derived models of processes.

Now, however, speed, memory, and dependability of computers are leading to fresh approaches to modeling and control of manufacturing processes, and a number of exciting new methods are receiving attention, one of which is the "learning network" approach. Networks for computer-aided prediction and control, which may be implemented in computer software or peripheral hardware, can learn to predict trends in a process from the natural data it produces. The process is characterized entirely from its observable variables rather than by a set of theoretical equations; its true characteristics are embodied in the natural stream of data that flows from it. The problem is thus one of generating a process model *from data* rather than one of estimating what the data will be.

At the very least, this way of thinking can augment traditional approaches. The learning network identifies which variables play significant roles in the behavior of a process and shows how these variables interact with each other (usually nonlinearly) in determining just what the process will do. Thus the network points the way toward improved theory for traditional modeling work. Alternatively, the network can model the most uncertain aspects of a process, leaving other, already fairly well understood aspects to theoretical derivations.

Learning networks themselves can infer and predict process behavior very accurately. Unlike most predictive models, errors made by these networks do not necessarily increase cumulatively with increasingly longer forecast intervals. Also, they can adapt to changing process characteristics, keeping themselves up to date without requiring tuning or redesign by human specialists.

Perhaps most exciting, learning networks are able to predict from data that are produced "naturally" by processes—including records of sounds or vibrations, subjective evaluations of product quality, or whatever variables are readily accessible for economical measurement. It is only necessary that the natural variables, taken in concert, contain information for the inferences or predictions to be made.

In other words, computer-aided manufacturing (CAM) systems need not rely on instrumentation of state variables and other conveniences of older theories about control. Often there is no way to instrument such

*This article is based on a paper presented by Mr Barron at the 1975 CAD/CAM Conference of the Society of Manufacturing Engineers, held in Chicago, Ill.

variables, either because the transducers required do not exist or because the variables are physically inaccessible. For example, relationships pertaining to a batch reaction are hardly useful if measuring temperature and composition of material in the reactor is impractical. However, a learning network might control such a reaction by monitoring such variables as acoustic emissions or fluctuations in the temperature of off-gases. In doing so, the learning network more closely resembles human-like abilities for making associations between complex patterns of events—with the speed, accuracy, and attentiveness of a computer.

Learning Networks

Inference and prediction problems involve operations with sensor data obtained as a result of observing a physical process. The classical approach to designing the computer model has been to use all relevant deterministic or statistical characteristics of the process being observed, along with certain assumptions in design calculations. Very often the designer presumes the structure of the model and merely calculates values of certain parameters. Even if the nature of the observed process changes, the structure of the model often does not change; but the designer adjusts the parameter values in response to measured changes in inputs or outputs.

In many important applications, observable inputs are difficult to describe analytically. The best or even a good structure for the model cannot be determined in advance. In this case, a desirable model structure can adjust to representative inputs. That is, the model is *trainable* in both its structure and parameter values.

Trainability in structure implies the existence of interconnections of similar elementary building blocks in a network. This network is described by a general (usually nonlinear) function of certain input variables called observables. Since little may be known about the characteristics of the observables, network parameters are not known in advance, but are learned as the network is trained with representative inputs. This concept raises new questions about what the structure of the elements of the network should be, how the element parameters should be adjusted, how many elements are necessary, and how they should be interconnected.

Polynomial and Multinomial Approximations

Suppose that the input consists of N observables, x_1, x_2, . . . , x_N, and the output, y, is a scalar quantity whose value is the estimate of a particular property of the input process. In general, y will be a nonlinear function of the x's. Under fairly general conditions, this function of N variables can be expressed in an N-dimensional Maclaurin series:

$$y = a_o + \sum_{i=1} a_i x_i + \sum_{i=1} \sum_{j=1} a_{ij} x_i x_j + \sum_{i=1} \sum_{j=1} \sum_{k=1} a_{ijk} x_i x_j x_k + \ldots$$

Although in the most general case, the coefficients are functions of time, underlying characteristics of the x's often do not depend on time, so that the coefficients are constants.

To apply this Maclaurin series, identities of the observables or measurements, x_i, must be known, along with the number of terms in the series needed to provide an acceptable approximation to the desired function—even though this function is itself not known. To determine the observables, all those that are *thought* to have a bearing on the desired output are used at first, and the ones whose trial shows them to be of little use are later discarded. The number of terms is determined adaptively with a trainable nonlinear

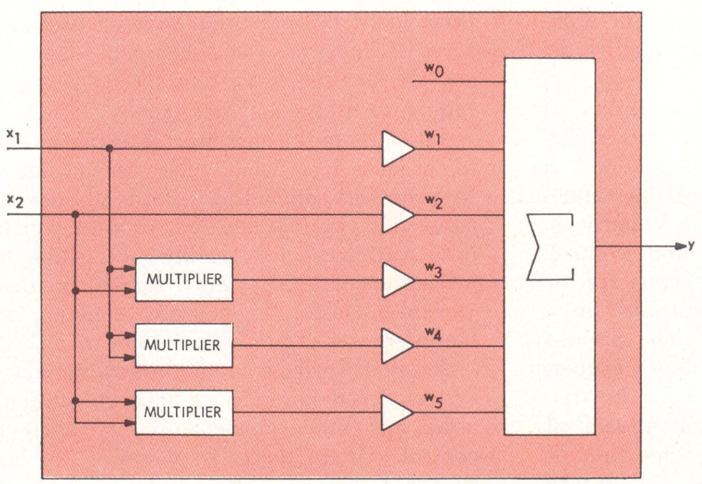

Fig. 1 Learning network element. A digital mechanization of the functions shown here is used to implement the first six terms of a Maclaurin series that expresses a property or characteristic of a process in terms of its inputs. It has only two inputs, but networks of elements such as this can combine all the inputs in pairs. Usually fewer than all possible pairs are necessary

network of interconnected elements, each of which implements a simple second-degree function of two inputs and one output, also including first-degree and constant terms (Fig. 1):

$$y = w_0 + w_1x_1 + w_2x_2 + w_3x_1x_2 + w_4x_1^2 + w_5x_2^2$$

This function is equivalent to the first six terms of the generalized Maclaurin series for two variables. Components of the element may be realized using digital devices. A network of these elements can be trained, by adjusting values of coefficients, to approximate the N-dimensional series.

Networks of the Basic Element

In a network of two layers of these simple elements (Fig. 2), each input, z_i, to the summation contains pairwise products of the network inputs, x_i, up to degree 4, while the first layer contains all possible pairs of three inputs. To implement a general multinomial expression (merely a polynomial in many variables), the number of elements in each layer would have to grow as one proceeds deeper into the network. However, it is found empirically that acceptable approximations are obtained without this growth; in fact, the number of elements in successive layers decreases—usually after only two or three layers—until only a few are left as inputs to the adder.

Known Data Set

Determining the coefficients of each network element and the number and interconnections of those elements requires a known data base—that is, a data base for which the values of the dependent variable are known. Steps involved are (1) optimizing the coefficients in each element of the first layer, (2) selecting those elements whose output is acceptable while rejecting the poor performers, (3) repeating steps (1) and (2) for the remaining layers, and (4) globally optimizing all coefficients in all layers based upon network output.

The known data base is divided into three independent but statistically similar subsets: a fitting subset, to determine coefficients of the elements; a selection subset, to reject the poor performers; and an evaluation subset, to evaluate overall performance. Fitting and selection subsets are also used for global optimization. Since the evaluation subset is *not* used for network synthesis, performance on it accurately estimates the network's ability to generalize to new, previously unseen data.

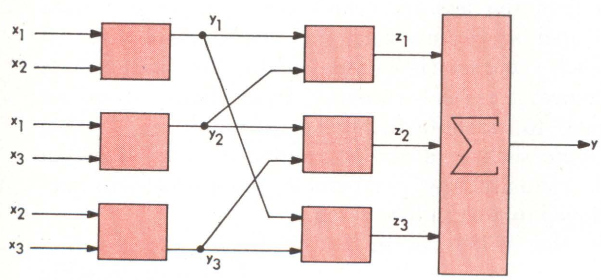

Fig. 2 Two-layer network. Three inputs combine into three pairs at the first level of elements such as that of Fig. 1. At the second level, outputs of the first level recombine in pairs to generate up to fourth-degree signals. Theoretically, later stages would snowball in number and complexity of interconnections, but in practice they do not

Training the Network

Element coefficient determinations are based, in part, upon a least-squares fit to a desired output, whereby the elements are first adjusted by a matrix algebraic procedure and then by a recursive search or optimization procedure. (Other criteria are of course possible, and are often used.)

Fitting and selection subsets are used alternately in training each layer. First, N specific observables that are the inputs to each element are chosen, more or less arbitrarily, and arranged into $N(N-1)/2$ pairs, feeding a like number of trainable elements, such as that shown in Fig. 1. Then the fitting subset of the known data base is applied to establish the coefficients, using a recursive search procedure with a least-squares criterion. The procedure is repeated for each of the $N(N-1)/2$ elements.

Not all pairwise combinations are significant in extracting the desired information. The selection process, using the selection subset, eliminates those elements whose performance is not acceptable, as measured by the square of the error magnitude. There are now, say, R elements that survive.

The process is repeated for the second layer, which initially contains $R(R-1)/2$ elements, involving all pairs of the surviving elements in the first layer—which now is again fed by the fitting subset. Coefficients of each element in the second layer are determined as in the first. Then the selection subset is fed a second time into the first layer and the unacceptable pairs eliminated from the second layer.

The process is repeated with succeeding layers until the error rate on the selection subset reaches a suitable low level. Although further reductions in error rate on the fitting subset could be made by incorporating additional layers, to do so would produce overfitting of the fitting data. Eventually, a single output results from each of several disjoint subnetworks; these outputs are added to produce a single output from the entire network.

A hypothetical example of the result of the training process to this point (Fig. 3) implies that at least 30 candidate parameters were initially inserted into the first layer, of which only a few survived. The figure shows that pair (x_1, x_{28}) interacts with pair (x_4, x_{30}), but pairs (x_5, x_8) and (x_{18}, x_{29}) do not interact with each other or with the other pairs. Thus the outputs of three disjoint subnetworks are added to produce a single output.

A final step in the training process is a vernier adjustment, or fine tuning, of the coefficients. This may arise because the coefficients of each element have been adjusted in the absence of interactions with other elements following them in the network; optimum coefficient values may be different when these interactions are present. Fitting and selection subsets are also used for this final adjustment process. The vernier adjustment—a global search—may use a random technique to obtain final values of the coefficients, as well as for subsequent network adaptation. After final adjustment of coefficients, the evaluation subset is used to estimate performance of the entire network.

Avoidance of overfitting is a key aspect in the training of learning networks. Good functional approximations to the fitting data subsets must be obtained that also closely approximate the data in the separate selection subsets—that is, the networks can be taught to generalize properly on their experience in fitting the points in the first subsets, so that error rates in later uses will be low. If overfitting is not avoided, the network produces deceptively small errors in approximating its first sets of data and then, in most cases, does poorly on subsequent new data. Often heard of are empirical models that appear to have much promise initially but that produce unacceptable errors when presented with new data; in most cases, such behavior is the result of overfitting. By using three independent subsets of the available data—taking care that each is statistically representative of the whole data base, the problem of overfitting is virtually eliminated and good advance estimates of operational error levels of the models can be obtained.

If a model realized by a learning network can be guaranteed not to be overfitted, it will be a smoothly fitted, functional approximation. Mathematically, this approximation is a continuous and differentiable function, derivatives of which closely approximate the quantitative derivative behavior of the real processes that are modeled. For this reason, numerical partial derivatives may be computed which reveal the quantitative sensitivity of the modeled variable (y)—and thus of the process that has been modeled—to small variations in specified values of the network input variables.

As will be seen, ability to interrogate learning networks at arbitrary points (within their regions of fit to prior data), thus finding predicted values and sensitivities of process responses, is the key to use of these networks in computer-aided design and manufacturing (CAD/CAM).

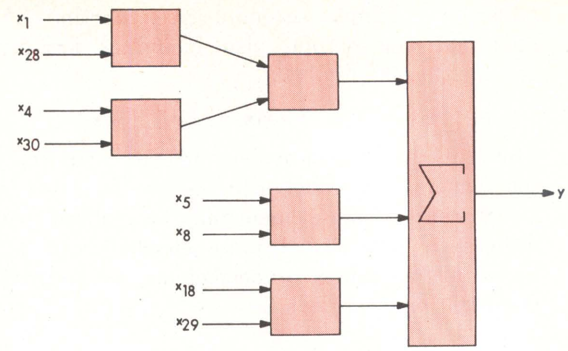

Fig. 3 Illustrative learning network. Although 30 or more inputs were hypothesized as contributing to the process controlled by this network, only eight survived the training process as contributing significantly to the output. Furthermore, only four of the eight required a subnetwork more than one level deep. Typically, learning networks have many more elements than shown here

Use of Learning Networks

A learning network in CAM implements a predictive model for the process being controlled (Fig. 4). A separate network is used for each predicted variable. Inputs to each network are measured process variables and trial control variables. When the switch is in search position, sequence search logic can rapidly interrogate the networks to discover predicted consequences of hypothetical control actions. When the switch is moved to control, the best sequence of control action found by interrogating the networks is transmitted through actuators to the process being controlled.

The sequence may be recomputed as often as desired—most often for a process that is subject to frequent disturbances. Conversely, the more accurate the predictive model, the less frequently the system must recalculate its control decisions.

Sequence search logic is a numerical optimization algorithm whose input is a predicted score computed by performance assessment logic. This score may consist simply of the magnitude of the arithmetic difference between the desired final value of a process variable and its predicted final value, in which instance the goal of the search logic is to find a sequence that drives the score to zero. When multiple variables are to be controlled to specified final values, the score function may be a weighted sum of predicted absolute final errors, in which the more important final variables are given greater numerical weights than the less important variables. Other, more sophisticated score functions may be computed to express such characteristics as quality of steady-state performance, transient recovery from disturbances, or adherence to manufacturing constraints. If flexible search logic such as a guided random search algorithm is used, virtually any computable score function may be employed to govern the search.

While the switch is in search mode, the learning networks are interrogated at a very high rate, making it possible to try many hypothetical sequences within a short period of time. Typically, for software networks having approximately 50 elements, at least 100 interrogations/s can be realized. Achieving a high interrogation rate requires that the networks be efficiently programmed. For the most demanding applications, peripheral computer hardware may also be employed to implement the networks. Depending on the amount of parallel circuitry used in the peripheral hardware, a tenfold-to-thousandfold increase in speed may be realized.

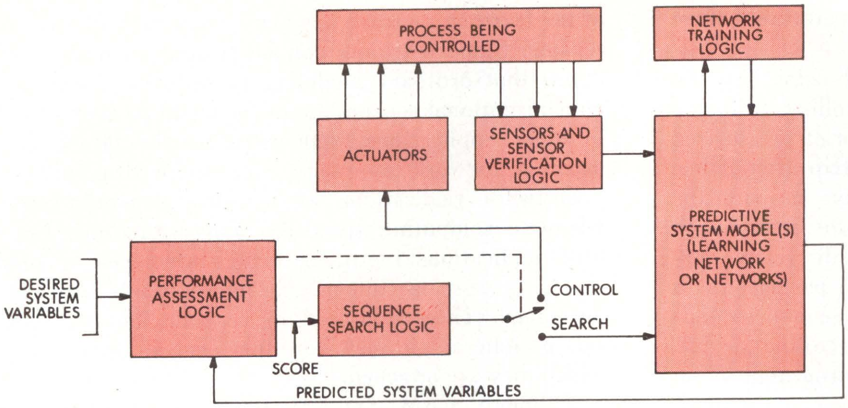

Fig. 4 An application in computer-aided manufacturing. Key elements, shown in color, set up an optimum sequence of control actions in search mode, then apply these actions to the process when the switch is thrown to control mode. If necessary, the system can return to training mode for minor retraining from time to time

When the predicted score is satisfactory, performance-assessment logic switches the control system from search to control mode (the system is in control mode most of the time), at which point adaptation or retraining of the predictive networks may be possible, using some of the system's computer resources. Adaptation is a fine tuning of network coefficient values, keeping the connectivity structure fixed, perhaps using a gradient or guided random search algorithm. Retraining completely restructures the networks and recalculates the coefficients to modify the ways in which network input variables interact within the networks themselves. Adaptation alone is usually sufficient, adjusting the coefficients in a background mode of control computer utilization—that is, with a lower priority than the control function, carried out only when the computer is briefly idle. Sometimes, adaptation is needed so infrequently that it can be performed entirely offline at, say, monthly intervals.

Sensor verification logic—an important part of the learning network system—establishes that each set of process measurements submitted to the networks is reasonably similar to the data patterns with which the networks were trained. If this similarity is not present, the process or sensor may be malfunctioning, or perhaps the system requires further training. Programs have been developed that perform the similarity test automatically and deal with each possibility that can arise; these programs use a data-clustering algorithm to synthesize the test.

Learning Network Example

Control of runout table cooling sprays in a hot-strip steel-finishing mill has been achieved, although this is a difficult industrial process for which to build a mathematical model—difficult because it has many process variables, strongly nonlinear interactions occur between some of these variables, and the response to a change in any input variable is delayed by a length of time related to the velocity of the steel strip moving through the mill and the physical length of the mill itself. Yet modeling such a process is extremely important, because it offers the best way to reduce or eliminate substantial economic losses suffered when either manual or conventional automatic controls are applied.

Learning networks provide a new method of modeling this process. They provide accurate, readily computable relationships with which—as the values of input and control variables are changed—outputs can be predicted. Because they take time delays into account, they are not sluggish as are linear controllers for transport delay plants, and they therefore avoid production of much off-specification material resulting from the large amount of time that such controllers require to reach their final states after input changes. Also, unlike some linear controllers that are too closely coupled, they do not become unstable.

Since it does not require that major nonlinear interactions be precisely known in advance, the learning network method is more successful than previously applied linear regression techniques. Also, unlike classical regression techniques, it is unlikely to go astray with real process data after having been made to work well with a different set of test data—because overfitting is avoided.

A typical hot-strip finishing mill consists of six roll stands, a runout table several hundred feet long with water sprays both above and below it, and a coiling device at its end. A steel bar about 1 in. thick and heated to approximately 1900°F enters the first roll stand, which squeezes it into a somewhat thinner and wider bar that is moving substantially faster than when it entered the stand (part of the steel displaced by squeezing goes sideways, part of it moves forward to contribute to the velocity of the bar). The other roll stands repeat the process in succession, so that the output strip is perhaps 0.1 in. thick, cooled to 1600°F (but still red-hot) and moving at up to 2000 ft/min. As it moves down the runout table, the strip must be cooled by the sprays to a specific temperature before it is coiled.

For illustrative purposes, rather than showing how the method may be applied to an entire rolling mill, we discuss here only its application to control of pressurized water sprays used to cool the hot steel strip after it has passed the last roll stand. (These sprays prepare the strip for coiling.) A typical mill contains many such sprays, typically arranged in about 15 discretely controllable spray banks; they affect several parameters in the strip being produced, which can take several seconds to pass from the last roll stand to the coiling device.

In this example, the model, which is programmed on an IBM 1800 process control computer, predicts the number of sprays required to achieve the desired coiling temperature. It has seven inputs: coiling and finishing temperatures; the strip's speed, thickness, width, and hardness; and spray pressure. (Finishing temperature is at the last roll stand; the difference between the two temperatures represents the heat that must be removed by the sprays.) Outputs are number and configuration of the sprays, chosen from eight above the table and seven underneath.

Reaction of the bar to the successive rolling steps is initially assumed and the sprays are preset when the bar enters the first roll stand, according to a prediction based on this assumption. As the partially rolled strip emerges from the fourth stand, the predicted sprays are actually turned on; they take a few seconds to build up to their full volume, while the strip traverses the last two stands. When the strip emerges from the sixth and last stand, the prediction is made again on the basis of actual measured temperature and speed of the strip. If the assumed behavior of the strip was valid, the original prediction would have been correct and the proper sprays would now be operating; but if the measured variables depart in any way from their assumed values, the number of sprays is modified accordingly.

The model also predicts the temperature of the cooled strip as it begins coiling. If the actual temperature at this point differs markedly from that predicted, the model may need modification or further training, or the process sensors or actuators may not be working properly. In practice, 98% of a sample run of 612 coils fell within an acceptable tolerance of ±50°F, corresponding to a prediction error within ±2 sprays. Furthermore, 93.5% of the coils were within ±1 spray of the ideal setting—substantially better than the performance of conventional controllers, especially when product specifications are frequently changed. (The learning network model that produced this performance was synthesized from building blocks according to the procedure outlined earlier).

Other areas where learning networks have been applied or are currently being developed for a variety of CAM processes include inference of surface-finish roughness in machining, ultrasonic nondestructive testing, fermentation process modeling, crystallization process modeling, and modeling of casting quality in aluminum diecasting.

Conclusion

Results for control of the cooling sprays on the runout table of a hot-strip steel-finishing mill verify the utility of the learning network approach, even with conventional sensors. Since networks can be trained to make associations that ordinary modeling procedures cannot make, nonconventional sensors might be useful or even essential in other applications, demonstrating the power of the learning network approach even more dramatically.

Software realizations of learning networks provide adequate computing speed in many situations. For future applications requiring faster inferences or predictions, large-scale integrated microcircuits are being developed. These will lead to very flexible and powerful peripheral devices for the central processors to which they are attached.

Although CAM applications of learning networks have been emphasized here, CAD applications are also receiving attention. Whereas in CAM the network is trained to a high degree of accuracy before being used online, in CAD it learns with each successive design experiment, and with search logic it performs as a designer in seeking out the best design.

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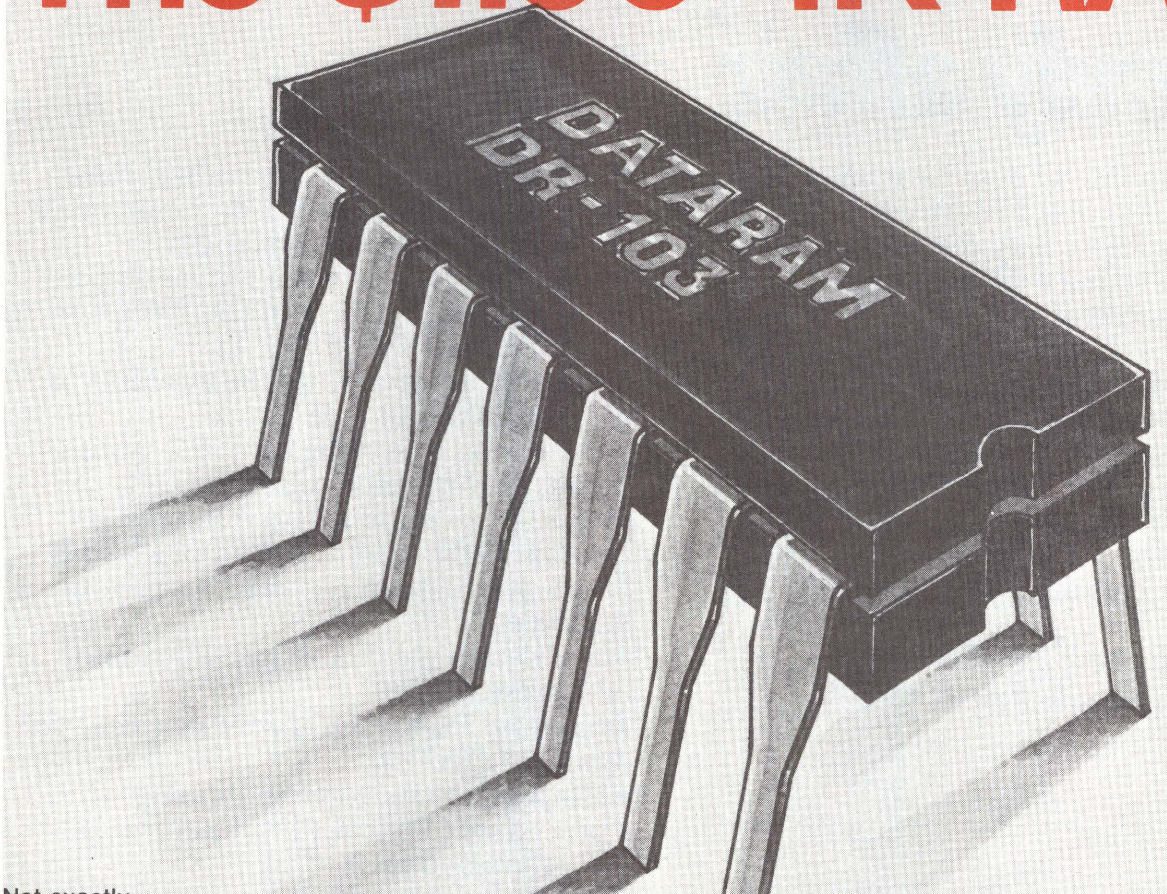

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Many factors affect the cost of a microprocessor-based system. A full-fledged evaluation requires a large investment of engineering time and talent, but a start can be made and an initial choice or elimination determined on the basis of a few specific features

Design Techniques for Microprocessor Memory Systems

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A microprocessor's cost is only a small percentage of the microcomputer system expense—typically less than 20%. Memory devices, peripheral circuits, clock drivers, power supplies, and cooling requirements account for the remaining 80%. Thus, minimizing the total system price requires special emphasis, particularly in the memory subsystem.

In 12- and 16-bit microprocessor systems, main memory utilization is only 20 to 30%—that is, on the average, memory access requires only 20 to 30% of central processing unit (CPU) active time.[1] There are two technological reasons for this sparse memory reference pattern of microprocessors. First, since microprogramming is the most effective implementation of the control structure of large-scale integration (LSI) processing units, most metal-oxide semiconductor (MOS) LSI microprocessors are internally "microprogrammed" using highly specialized programmable logic arrays (PLAs). This, of course, does not imply that all microprocessors are microprogrammable in the conventional sense; rather the PLA is optimized for a specific architecture and, in general, cannot be used efficiently for any other than the particular processor's macroinstruction set. However, the microprogrammed structure implies that the processor executes two to four nonmemory cycles for every memory cycle.

Second, since microprocessors and memory devices are implemented with the same technology (such as complementary, n-channel, or p-channel MOS) any technological improvements that result in reduced CPU cycle time should also reduce the memory cycle time. These two factors explain why the memory is utilized so ineffectively.

Multiple-CPU Systems with a Single Memory

This sparse memory reference pattern makes MOS LSI microprocessors suitable for multiple CPU-single memory systems.[2] Hardware simulations in a point-of-sale system, which used a 16-bit microprocessor to control eight terminals, showed that, on the average, memory was active only 32% of the CPU active time.[1] In this system, terminal transactions included typical cash register operations along with inventory control. However, the eight terminals exhausted the computational capability of the one CPU, while the memory bandwidth was still under-utilized. On a long-time average basis, three CPUs could share the single memory while only slightly degrading the individual CPU performance. A software simulation predicts the 3-processor throughput to degrade from 3 (the level when they run independently) to 2.65 (when they share a single memory), averaged over the entire simulation interval.

Memory-usage pattern of the CPU is highly application dependent and can be reduced even further for any given application. One way is to choose a CPU with an instruction set best suited for a specific application; another is to microprogram the most commonly used routines in a microprogrammable processor. There is also a definite correlation between the CPU word length and memory utilization. For example, an 8-bit CPU tends to refer to main memory more often than 12- and 16-bit machines, because most instructions in 8-bit machines are two or three bytes long.

Some CPUs repeatedly fetch from memory even when doing no useful work. This frequently happens

TABLE 1

Performance Degradation

	Slow down all cycles	Slow down memory reference cycles	WAIT 500-ns steps	WAIT 250-ns steps	WAIT 1-ns steps
New memory reference cycle	3.5 μs	3.5 μs	3 μs	2.75 μs	2.7 μs
New nonmemory reference cycle	3.5 μs	2.5 μs	2.5 μs	2.5 μs	2.5 μs
Effective memory access	700 ns	700 ns	1000 ns	750 ns	700 ns
Percent degradation in memory reference cycle	40%	40%	20%	10%	8%
Percent degradation in nonmemory reference cycle	40%	0%	0%	0%	0%
Percent degradation in CPU throughput with 40% "slower" memory device	40%	10%	5%	2.5%	2%

CPU cycle	2.5 μs
Memory access requirement of CPU	500 ns
Access time of memory device	700 ns
Percentage increase in access time	40%
Memory utilization of CPU	25%

in a "wait loop," which is a conditional branch that tests for occurrence of an external event, such as completion of an input or output (I/O) data transfer. In the absence of that occurrence, the branch repeats itself over and over, until the event happens. In dedicated applications, the CPU may have no alternative but to wait in this way, because it has no background processing to do. Every iteration of the loop requires that the CPU access memory to fetch the loop instructions. In a more efficient but more complex design, the CPU pauses—that is, it actually shuts itself down—until the external event restarts it through an interrupt procedure, avoiding unnecessary memory references.

System Performance with Slow Memories

Multiple-CPU systems are cost-effective only in applications that are computation-limited (as opposed to I/O limited). However, many microprocessor applications are not thus limited, placing the emphasis on reducing memory system cost. Since slow memory devices are less expensive than fast memory devices, cost can be kept low by using slower memory devices, if little or no system degradation results.

For illustrative purposes, assume a CPU cycle time of 2.5 μs. Assume also that for the CPU to run at full speed, memory access time should be 500 ns or less—a typical requirement for today's microprocessors. If a less expensive device with an access time of 700 ns is available, it can be used by slowing the entire system by 40%, extending the CPU cycle to 3.5 μs. However, this also degrades overall system performance by 40%. If one could "stretch" the CPU cycle only when it refers to memory, in perhaps one cycle out of four, the effective reduction in processor throughput would be only 10%.

A still better approach would be to "freeze" the CPU for 200 ns during the memory "window" of a normal cycle. This would extend the window from 500 to 700 ns, and the entire cycle from 2.5 to 2.7 μs. If memory references occur in only 25% of the cycles, system throughput degradation would be only 2% using a 40% slower memory.

Most currently available CPUs have a WAIT signal which stretches the CPU access window in the CPU cycle to accommodate slower memories and peripherals. When the WAIT signal is active, the CPU shifts from a synchronous mode of operation to a "handshake" mode. If the WAIT mechanism is not built in, it may be simulated by controlling the external clock generator, though this is difficult and cumbersome.

"Granularity" of the WAIT period—the minimum number of time units the CPU period can be stretched—varies among microprocessors. In practice, circuit design considerations constrain the WAIT period to be in

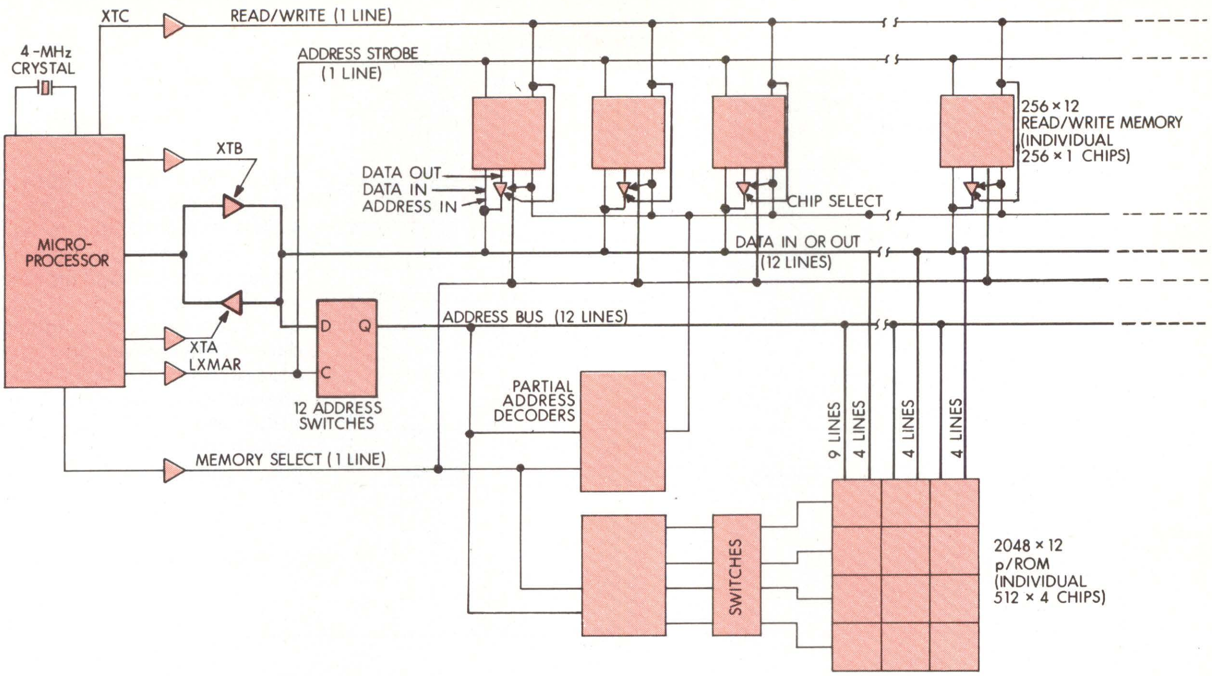

Fig. 1 Typical memory system. Although different applications require different configurations, this 2K x 12 p/ROM with a 256 x 12 read/write memory would be adequate for most, particularly if it includes provision for expansion to twice the size. The switches next to the p/ROM array apply power only to the particular chips being addressed at any one time, significantly reducing the system's total power dissipation. The whole system, including memory, dissipates less power than some multichip microprocessors alone

multiples of the basic CPU clock period. For example, if the WAIT duration must be an integral multiple of 500 ns, transfer time for a 700-ns memory will be the 500-ns memory window plus one WAIT period, or 1 μs. This reduces throughput by 5%, whereas, without granularity, the reduction would have been only 2%.

One way to abate this design constraint is to use a higher frequency clock and to divide the frequency for internal operation. For example, if the CPU has a 4-MHz timing source, divided by 2 for internal operation at 2 MHz, the WAIT can be in 250-ns steps—the length of one period at 4 MHz. Effective access time for a 700-ns memory would then be 750 ns, or the 500-ns access window plus one WAIT period, reducing throughput by only 2.5% (Table 1).

Power supplies and cooling requirements add considerably to both the cost and reliability of microprocessor systems. Even though the power dissipation of masked and programmable ROMs (p/ROMs) can be substantially reduced by power strobing—applying power to the devices only when they are selected for reading—this method won't work for read/write semiconductor memories, which lose stored data in the absence of power. Therefore, microprocessor-based systems usually contain a mixture of read-only and read/write memory—the former conserving power while storing fixed data, and the latter storing variable data while dissipating as little power as possible.

Microprocessor-Based Memory System

It is difficult to come up with a universally acceptable memory mix for such a system. A 2K x 12 p/ROM combined with a 256 x 12 read/write memory (Fig. 1) seems adequate for most applications, if the system includes provision to expand the total capacity up to 4096 words. For the majority of 12- to 16-bit microprocessor applications, memory requirements will be less than 4096 words. However, for any given application, an 8-bit machine must address more words of memory than a 12- or 16-bit machine, making its equivalent maximum memory-address space about 8000 words. Of course, the 8-bit machine must have a higher intrinsic speed to match the performance of the larger unit.

In a typical system based on the Intersil IM6100 (see "A Memorable Microprocessor," p 78), address, data-in, and data-out are multiplexed on 12 transistor-transistor logic (TTL) compatible lines, which may require buffering in general-purpose systems that require more capacitive or current driving capability than the microprocessor itself provides. When these lines carry a valid address, a CPU output called LXMAR indicates this condition; it may be used as the clock input to latches that store address information (Fig. 2). These latches may be external independent logic chips, or the internal address latches that are found in most CMOS

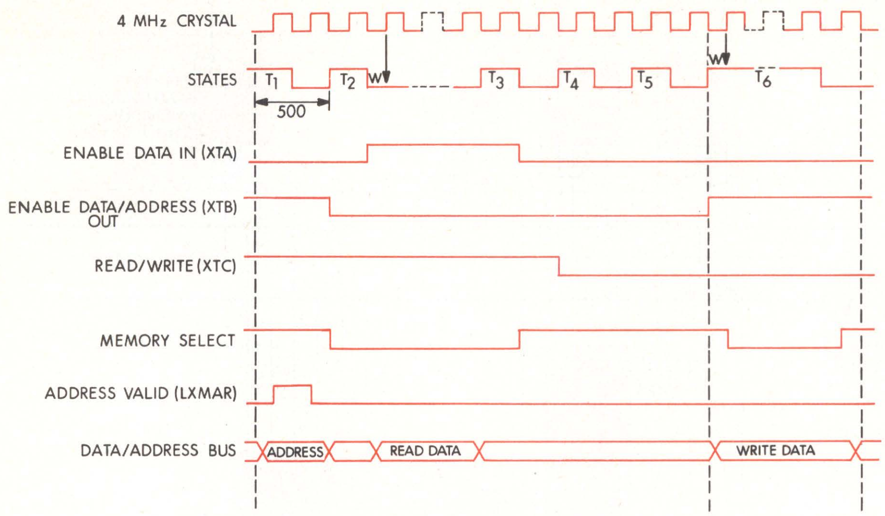

Fig. 2 Memory system timing. System clock runs at 4 MHz and is divided to half that frequency to permit closer control of waiting time for arrival of incoming data or acceptance of outgoing data. Data travel in both directions on bus, time-shared with address; ENABLE and ADDRESS VALID signals identify and clock the bus signals

and 4-kilobit n-MOS dynamic memories—for which this line becomes an address-strobe of chip-enable signal.

After the address has been latched, a memory-select line becomes active (low). It is one of four CPU outputs that address the memory, a switch register, an I/O device, or the control panel. When decoded with the high-order address bits, the memory-select line is the chip-select input for the memory devices. Another CPU output, called XTC, designates Read when it is high and Write when it is low.

Finally, two more signals, XTA and XTB, steer incoming and outgoing data through receiver and transmitter, respectively. Access windows represented by the active level of these lines may be extended indefinitely, in steps of 250 ns, with the WAIT signal, which is useful both for memory accesses and for I/O devices, particularly if long cable delays are involved.

A typical p/ROM is Intersil's IM5624, a 512 x 4 bipolar device with access time of about 50 ns and power dissipation of 500 mW. Its elements are programmed with avalanche-induced migration (AIM) technology,[3] instead of the conventional fused-link approach. Power for this memory can be switched on and off with a pnp transistor, such as 2N3467, in series with the V_{cc} line and controlled by the memory-select line.[4] The series power switches add less than 20 ns to the basic 50-ns access time; since memory system access time of less than 500 ns does not improve the performance of a typical microprocessor, the added delay does not affect system operation.

Intersil IM6523 and IM6524 CMOS read/write memories, both 256 x 1 silicon-gate devices, are typical microcomputer components.[5] Both are pin-to-pin replacements for the widely used SN74200 memory, a TTL device; however, the 6523 has three chip-select lines, while the 6524 has only two plus an address strobe that latches the memory address internally. These internal address latches, along with 3-state outputs, permit the address and data multiplexing mentioned previously without degrading performance of the system. With an address strobe, a static device can be inherently faster and dissipate less power than the fully asynchronous design; thus, the 6523 has typical access time of 400 ns at 5 V and power dissipation of about 10 mW at 1 MHz, compared to 250 ns and less than 5 mW for the 6524. Although the synchronous design causes a slight lengthening of cycle time, this is more than offset by improved access time, which is a more important parameter.

Extremely low standby power dissipation makes CMOS memories particularly suitable for nonvolatile memory systems, which have obvious advantages. In standby mode, they require only 1-μA or less leakage current. Thus, with addition of a standby rechargeable battery and a diode to keep the battery from discharging into the turned-off power line, these devices can be built into a nonvolatile memory system with ultra-low standby power requirements—only 600 mW at 5 V (Table 2). With these levels of power dissipation in memory, total power dissipation of the entire system is only 2 W average and 4 W peak—less than that of some multi-chip microprocessors alone. It makes a battery-operated portable microcomputer system (Fig. 3) feasible for the first time.

Some "quasi" CMOS p/ROMs may be available in the near future—for example, a laser-trimmed CMOS ROM. Even though a laser-trimmed ROM is not "field programmable," it offers easy design changes because of fast factory turnaround—less than a week—and very low setup charges. Another possibility is a hybrid design having classic p-MOS floating-gate transistors as programmable elements and CMOS peripheral circuits. However, until something like these comes along, power strobing of bipolar p/ROMs is probably the best solution for microprocessor systems.

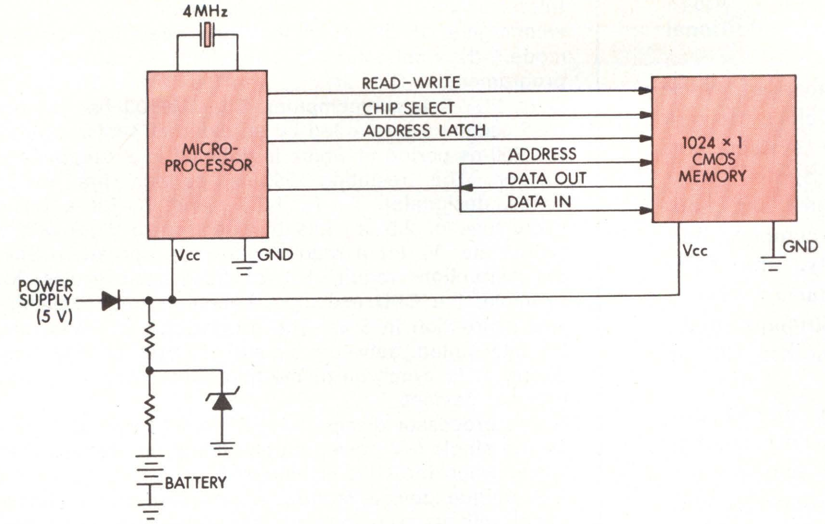

Fig. 3 Portable microcomputer. Low power dissipation of this CMOS-based system, powered from rechargeable batteries, make it truly portable.

Minimizing Overall System Cost

Certain auxiliary circuits are necessary to make a microprocessor memory system operational in a general-purpose environment. They include transceivers (transmitter/receiver pairs for buffering data lines), address latches, and additional buffering devices for control lines.

Address latches are essential only if address and data are multiplexed on the same lines, and if the memory devices do not have internal latches. In devices that do have internal latches, multiplexing is the rule, because dedicated address lines do not make much sense, especially in 12- and 16-bit machines. It would be better either to use those pins for more useful functions or to reduce the package size. However, for 8-bit machines, since eight bits address only 256 words, more address lines than data lines are needed. There are three possibilities: Fully dedicated address lines would require a package with a great many pins, perhaps more than are justified for a small device. Dedicating some lines to high-order address bits and multiplexing the other bits with data is more practical. Finally, address bits could be time-multiplexed themselves and brought in along the same lines that will later carry the data. Providing dedicated address lines doesn't necessarily save any external packages in a system. For example, buffering 12 address lines to provide drive capability for a general-purpose system would require two hex buffers; and latching them would require two hex latches.

A well-designed microprocessor provides all control signals for interacting with memories, I/O devices, and control panels, minimizing the total chip count in the system. Nevertheless, a microcomputer system will require from 10 to 50 support components, de-

TABLE 2

Power Dissipation

	Per chip	Total per system (peak)	Power strobing (peak)	Duty cycle	Avg per system
CMOS 256 x 1 Read/Write	5 mW	12 chips 60 mW	60 mW	40%	24 mW
TTL 512 x 4 p/ROM	500 mW	12 chips 6000 mW	3 chips 1500 mW	20%	300 mW
Decoders and buffers	—	840 mW	840 mW	30%	252 mW
Total	—	—	2400 mW	—	576 mW

pending on the microprocessor. These, in turn, can impose other complications.

However, since most standard ICs are available in TTL and operate at 5 V, a single 5-V power supply for the system would be beneficial. Each additional power supply adds about $20 to system cost.

High-voltage clocks and a large number of clock phases should be avoided. High-voltage clock drivers introduce large transient currents in the system, and these make system layout very difficult. Special pulse requirements, such as nonsymmetric shapes and non-overlapping sequences require a more complex and more expensive clock generator. Ideally, the CPU should operate directly from a high-frequency crystal or a single-phase, TTL-level clock. A complex high-voltage clock generator can easily add another $20 or more to the cost.

Almost any microprocessor can satisfy almost any application requirement, as long as one of the requirements is not real-time performance. Other major selection criteria are word size, memory requirements, chip count, power dissipation, number of power supplies, operating temperature range, clocking requirements, ease of understanding, ease of use, software support, and application support—all of which affect the total system cost. Since there is no standard instruction set or standard job to be done and the amount of work performed per instruction varies from machine to machine, the only way to fully evaluate competing microprocessors is to code specific benchmark applications and see how well a given microprocessor performs and at what cost. This will clearly show that some microprocessors offer more cost-effective solutions than others for a given problem. Many factors affect the system cost without getting into specific real-time performance features.

The true cost of realizing a specified real-time performance objective is not easy to evaluate. For example, assume that an 8-bit microprocessor specification includes executing a subroutine call in 8.5 μs, which implies five memory references—one for the operation code of the branch instruction, two to get the subroutine's location, and two to store the contents of the microprocessor's program counter, so that the main program can be resumed at the conclusion of the subroutine. (These last two are required only when the stack that stores the counter contents is implemented in main memory—but that is often the case.) If the microprocessor memory access requirement is 500 ns and if the CPU must wait an additional 1 μs for every memory reference—as it must if the system uses relatively slow, p-MOS erasable ROMs—true execution time for a call is then 13.5 μs, not 8.5 μs. If a specified microprocessor performance depends on a particular high-speed memory device, to realize that performance the incremental cost of the fast memories must be added to the cost of the microprocessor.

It is difficult to put dollar figures on certain other costs, such as the relative amount of both hardware and software engineering that is necessary to tailor various microprocessors for a specific application. For example, a microprocessor with a straightforward, easily understood symmetrical instruction set, adequate software support, and easy interface capability can reduce engineering time by as much as an order of magnitude.

A Memorable Microprocessor

Intersil's IM6100 is a single-chip, 12-bit CPU built with silicon-gate CMOS technology and operating in static mode.* Its architecture is compatible, in software and programmed I/O interface, with the Digital Equipment Corp PDP-8/E minicomputer. The IM6100 has an on-chip oscillator controlled by an external 4-MHz crystal, the 250-ns period of which is doubled in a single-stage divider. The resulting 500-ns periods are called states, designated T_1, T_2, T_3, T_4, and T_5, for a basic cycle time of 2.5 μs; this is extended to 3 μs with a sixth state, T_6, for a read-modify-write operation. Simple instructions require two of these basic cycles; for example, the CPU executes a memory-to-accumulator add instruction in 5 μs. The progression of states can be interrupted between T_2 and T_3 and at any time during T_6 to synchronize the microprocessor with slow external devices.

The processor dissipates less than 10 mW at 4 MHz from a single 5-V power supply; this drops to less than 1 mW when the CPU is halted.

A unique device feature is provision for a control panel with its own memory, separate from and transparent to the main memory.

*"IM6100 Users' Manual," Intersil, Inc, 10900 N Tantau Ave, Cupertino, CA 95014.

In general, all microprocessors with a given word length cost about the same and have roughly comparable instruction sets. Therefore, it is relatively safe to assume that, unless real-time performance is really critical, most currently available microprocessors will perform competitively in a given application. The question then is how cost-effective is the solution. Since full-fledged evaluation implies tremendous engineering investment, specific features such as those discussed should help the user at least in the initial evaluation.

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MC1667	Dual Clocked R-S Flip-Flop (Low Z)	SP1667
MC1668	Dual Clocked Latch (High Z)	SP1668
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Software in small computers may be totally abolished as a result of two market trends that warrant designers' attention: tendency to reflect what the nontechnical user wants, and departure from the use of new technology for its own sake

Market Factors Portend Design Changes in Small Computers

Donald R. Wulfinghoff

Booz · Allen & Hamilton, Incorporated
Bethesda, Maryland

The design approach used in the small-computer industry during the past decade is being reoriented by two emerging factors which are more closely related to the nature of the market than to technology. One is an increasing recognition of the market potential for computers that can be operated by nontechnical users, which prompts the designer of small computers to make his machines easier to operate; the other is reduction of computer prices to the point where a vast market consisting of nontechnical users is but one more cost reduction cycle away, which reorients the designer from technological sophistication toward lower cost.

Radical changes of the past were, for the most part, the result of technical virtuosity. Indeed, the history of the past decade is characterized largely by the emergence of small-computer companies headed by technical entrepreneurs. In some cases, these companies crystallized sufficient customer interest to grow and prosper; in others, their products could not find enough application to keep them in business. The market grew because it happened to need what the technical impresarios had to offer. Because this need eventually proved to be great enough to support volume production, the flow of new technology created not only technical advances, such as order-of-magnitude increases in speed and memory capacity, but also order-of-magnitude reductions in cost. However, expense has diminished nonuniformly in two major respects: relative price of the central processing unit (CPU) in an overall system has fallen much faster than that of other system elements, and hardware prices have dropped much faster than those of software. These changes in the balance of system cost should tempt the designer to consider new technological approaches for the purpose of reducing overall expense.

Hardware Cost Trends

Until a few years ago, the CPU dominated the price tag of a computer system, while memory, input/output (I/O), and peripherals were sized and priced to be CPU compatible. Most of the CPU's high cost resulted from the investment in discovery, invention, and engineering it represented. Once this phase had passed and the architecture of single-processor computers had stabilized, a drastic reduction in CPU cost became possible (Fig. 1), so that computers were able to reach—or create—a phenomenally broadened market base. This, rather than any significant change in capability, was the essence of the minicomputer revolution.

Today, the mainframe memory is typically the most expensive system component. With current architecture it will remain so, because memories are more highly standardized than any other computer element and thus their cost has less room in which to descend on the learning curve. Consequently, memory manufacturing costs will remain principally a function of array size, regardless of memory element type.

On the other hand, costs of processors, I/O, and many of the newer peripherals still contain a large factor of development and engineering. As pro-

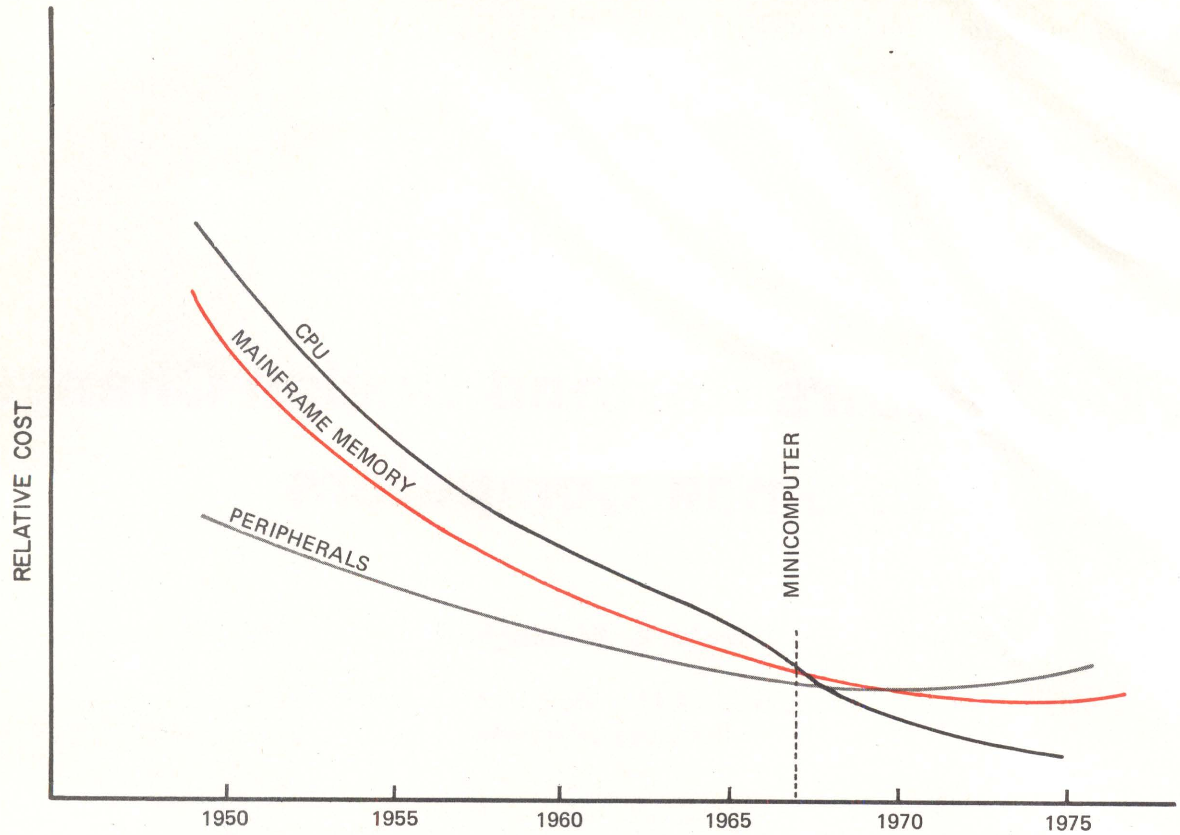


Fig. 1 Computer element cost trends. Large decline in relative CPU cost and leveling off of memory cost make memory an increasingly predominant factor in price. Expense of software, expense of memory to store it, and declining cost of hardware point to eventual disappearance of small-computer software

cessors become standardized, their prices will drop still further; this is, in fact, already happening, thanks to developments in large-scale integration (LSI), permitting a whole processor to fit on one or a few chips.

Standardization of I/O must await that of peripherals. This may take a long time, since new types of low cost peripherals will be required to service the yet evolving small computers of the future. Once standardization of all system components has taken place, mainframe memories will stand out even more obviously as the principal component of system cost. However, an architecture of inexpensive processors and expensive memories will be too provocative of change to endure unchallenged. If the cost of large, random-access main memories in small computers cannot be reduced, new architectures will almost certainly be developed to circumvent their expense.

Hardware/Software Cost Ratio

When hardware costs were much higher than they are today, the most economical approach was to program as cleverly as possible, in order to extract maximum benefit from the hardware. Today, software prices have risen, while those of hardware have plummeted, so that the cost of programming begins to exceed that of system hardware (Fig. 2). In addition, users have discovered from experience that the ability of software to extract performance from hardware has a practical limit, and that both costs and programming difficulties escalate rapidly as this limit is approached.

The result is a countertrend toward implementing functions in hardware instead of in software. In principle, any software function can be implemented in hardware; development of microprogramming has rendered it feasible as well as practical to execute repeated functions in this way. Housekeeping functions are particularly attractive targets for building in hardware because they are the most repetitive of all functions and because, if performed in software, they demand that the programmer have the most intimate knowledge of the machine's architecture. To some extent, housekeeping functions have been hardwired in the larger machines for many years, and this trend will undoubtedly soon encompass all machine designs.

Next in line for hardware implementation are standard high level language statements, usually executed by

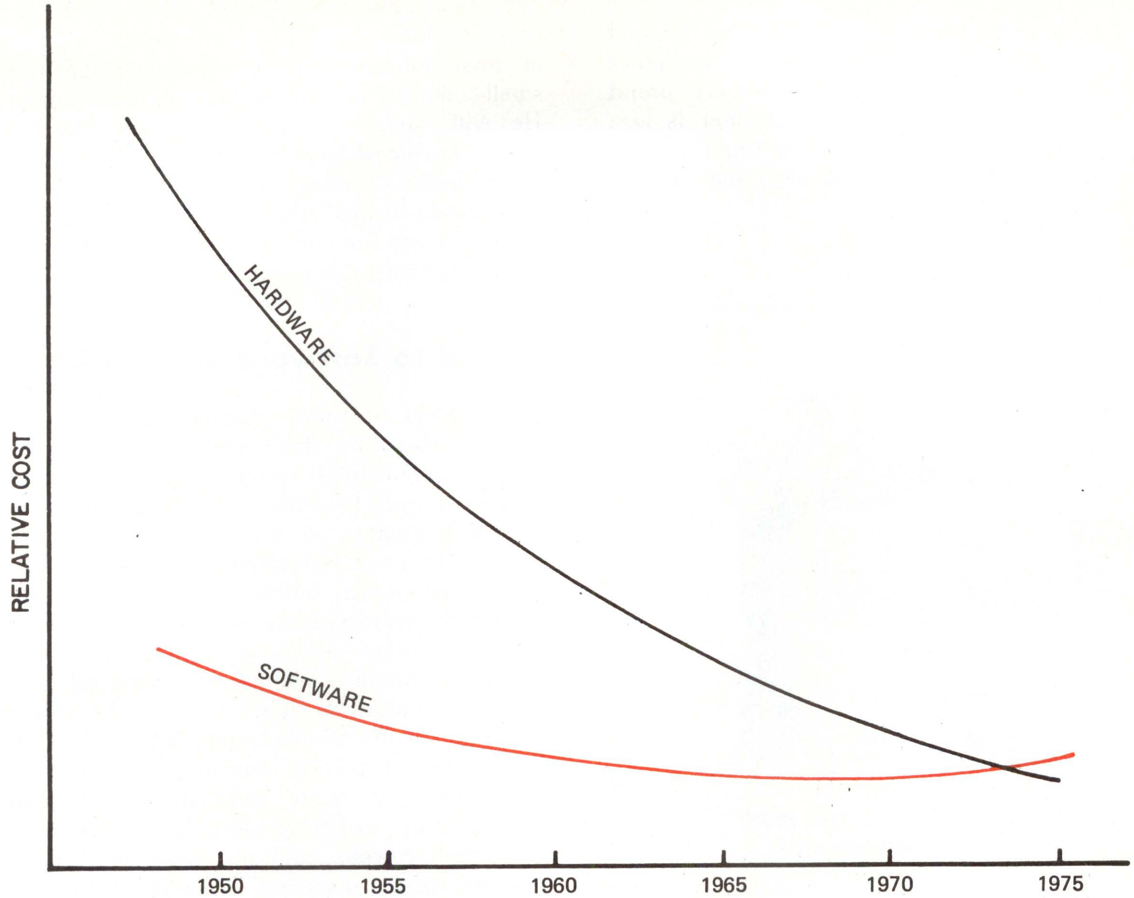


Fig. 2 Hardware/software cost trends. While relative costs of hardware are still dropping, relative cost of software has bottomed out. As a result, cost of software will henceforth determine minimum operating cost of conventional computers

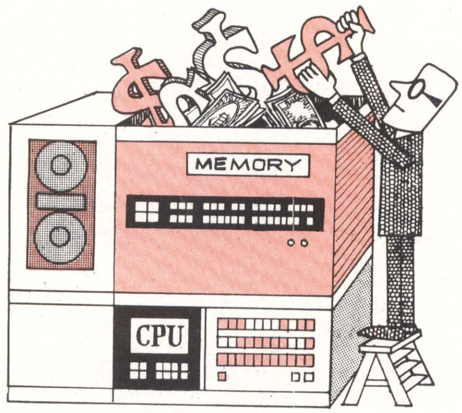
a large number of compiler steps. Progress toward hardware implementation can be seen, for example, in a plug-in module for the Hewlett-Packard 2100 computer series, which carries out 12 subroutines. At the present time, executing hardware functions that were previously performed in software is being marketed on the basis of offering higher throughput. In the future, however, hardware implementation will be used primarily to eliminate software and, possibly, to reduce overall system cost.

New Computer Market

Like other 20th-century technological marvels, such as the automobile and telephone, the computer has created widespread realization of the need for its capabilities—but unlike the automobile and telephone, it is still priced out of reach of a large majority of its potential users. However, advances in technology accompanied by increasing production volumes have succeeded in reducing the price of small computers to within an order of magnitude of what a majority of potential users can afford.

Explosive growth of the electronic calculator market in just the past few years illustrates what could happen in the vast untapped small-computer market. It shows that an attractive new product will sell in volume if it offers some prospect of repaying its cost in financial or psychological terms. This holds true even though the cost in absolute terms may be rather high (witness the engineer who spends several hundred dollars for an "electronic slide rule" when he could get by with his much less expensive bamboo model).

Immediate task of the designer is to reduce the initial cost of small computers to a level that is feasible for a substantial number of small users. Later, sales will result in large enough production runs to bring the price to within range of the remainder of the market. One particular characteristic lends hope that such a price break can be achieved: execution speed will be almost inconsequential to the new customer—much less so, for instance, than required for satisfactory operation of inexpensive electronic calculators. Predominantly, the small-computer user of the future will be a garage owner or haberdasher who wishes to calculate payrolls once each week, taxes once per quarter, and a financial statement once per year, or a scientist or engineer with a customized program to run a few times during the course of a year. For this class of customer, the machine must compute—not rapidly, but *autonomously*, eliminating a good bit of the user's drudgery and relieving him for other work. High processing speed is not especially useful to him, because his utilization of the computer is low, and program preparation and data entry times will always far exceed execution times of even the slowest-speed CPU.



MAIN FRAME MEMORY IS THE MOST EXPENSIVE COMPONENT

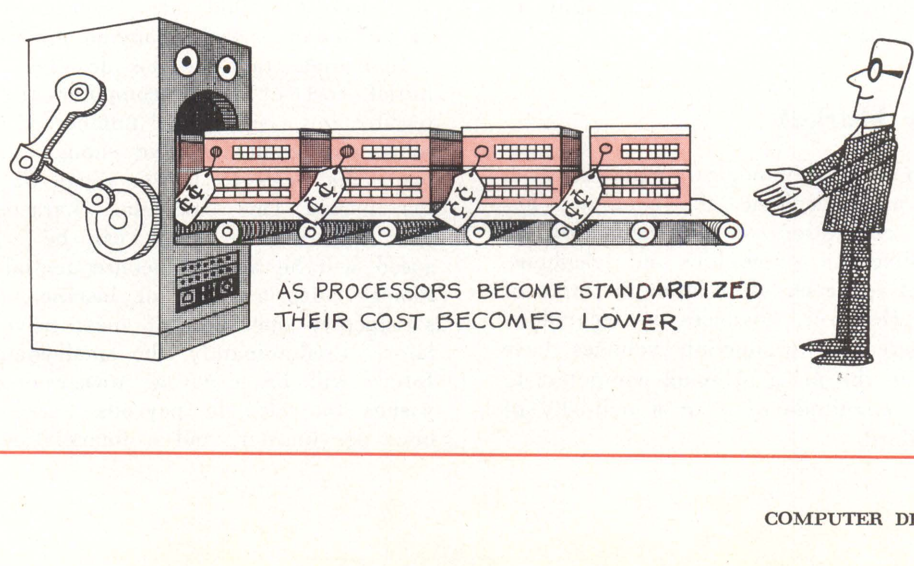
Another lesson of the calculator boom is that the typical new user will not buy a machine if he has to educate himself to operate it. Small calculators are so widely accepted in part because the user must learn virtually nothing in order to use one. The new computer user will have neither the time nor—probably more important—the confidence to learn a COBOL or a FORTRAN. The prospect of software, with its attendant coding sheets, assorted I/O devices, and other arcana, will frighten him away. Whereas the typical minicomputer user of today is either technically sophisticated or at least intrigued by a computer, the predominant small-computer user of the future will be neither of these. He will summon courage sufficient to face only a simple keyboard or some other equally unsophisticated input device—leaving to the designer the task of incorporating behind the keyboard the hardware which will carry out functions that with present minicomputers require considerable programming skill.

An End to Software in Small Computers?

Development of small computers is quite likely to be affected, then, by three factors: cost of software in proportion to total system price, reluctance of new computer users to generate, or even use, software, and the predominance of main memory—largely required to hold program execution software—as the most expensive subsystem. Indeed, these constitute three strikes against the very existence of software in small computers.

From another aspect, software may turn out to be a heel of Achilles leading to a reversal in the minicomputer industry's heretofore good fortunes. While the success of minicomputer applications has never been comprehensively surveyed, repeated allegations are made that many installations are failures—that they end up gathering dust in a corner of the lab after the professor and his graduate students learn—too late—of the machines' demands on time and pocketbook. As a result of disaffection stemming from variations of this experience, minicomputer sales may suffer a drastic decline, similar to those experienced by other technological marvels which failed to focus on the particular needs and limitations of the user.

This all adds up to the total absence of software as we presently know it in the predominant small computer of the future, and the substantial reduction of software in larger machines. The obvious alternative is hardware control (which may be called "firmware" or some other name).



AS PROCESSORS BECOME STANDARDIZED THEIR COST BECOMES LOWER

Software will be used in the future only with specialized machines run by computer professionals in order to perform functions which are needed so infrequently that hardware implementation is still not cost-effective. Aerospace and control applications, for example, may continue to depend on software indefinitely.

On the other hand, computers that actually compute will tend to abandon software. They will have simplified input devices and, consequently, limited instruction repertoires, which may increase the number of program instructions substantially. However, this will not necessarily increase either programming time or execution time, since single-keystroke, high-level instructions will be faster than today's usual computer inputs for both the user to specify and machine to perform. Most common input device will probably be a keyboard, because it is universally familiar. This pattern has already been set in some advanced programmable calculators, which have well laid out keyboards with separate sections for numerals, variables, and high-level instructions.

The range of functions that can be performed with relative ease in a software-directed minicomputer will probably never be economically implemented in a single hardware-directed small computer. Consequently, to shift from one category of problems to another, the user will interchange circuit boards or perhaps trade one computer for another. As with the present calculator market, one computer will perform business-oriented functions, another engineering functions, and so forth. Standardized operations such as trigonometric or statistical are already widely mechanized.

For other scientific problems, the designer may have to be more of a mathematician than he is now. One cannot mechanize an integral, for example, with the same certainty of avoiding mathematical pitfalls as one has in mechanizing a trigonometric function. However, despite the insistence of some numerical analysts that it cannot be done, the computer that evaluates integrals without an unacceptably high proportion of incorrect answers, and without requiring the operator to be knowledgeable in either programming or numerical analysis, will be a necessity in the scientific market.

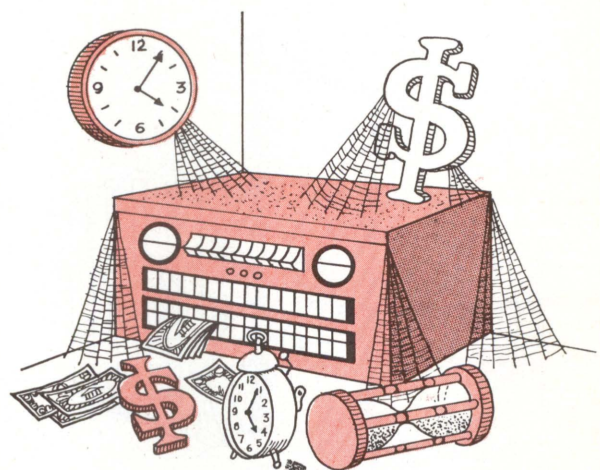
Eliminating Memory from Minis

Memory stores three types of information: data, manipulations of those data desired by the user, and ancillary instructions required by the machine for carrying out those manipulations. The first two are necessary in order to accomplish the user's objective, but the third is strictly for the benefit of the machine; the need to remove this "excess baggage" motivates the trend toward elimination of software.

Handling this third category of data also keeps the price of small computers at an unacceptably high level—high because the new user is demanding conversational languages, which, with software implementation, call for compilers. These typically require several thousand words of high speed storage, so that if current trends in memory prices can be extrapolated with any degree of certainty, the cost of memory will indefinitely keep the price of small computers well above $1000—too expensive for the new market.

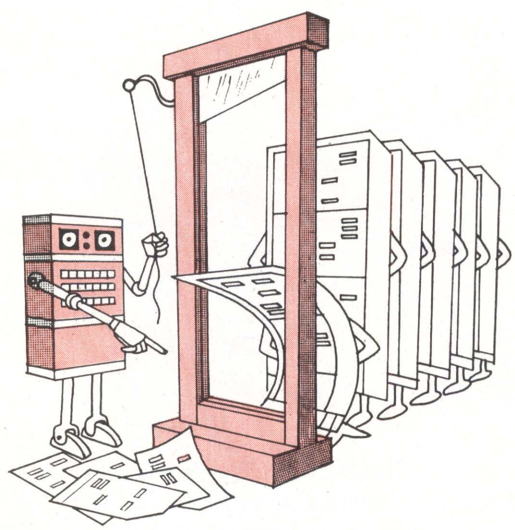
Programmable-calculator designers have made a very impressive contribution by mechanizing ancillary functions in hardware and thus eliminating storage of ancillary data in their machines. An intermediate approach to removing such data has been taken in heavily microprogrammed minicomputers, such as those developed by Microdata Corp; mechanization and microprogramming have reduced random-access storage requirements to several hundred words.

The much smaller memory required for necessary program instructions and data in the typical program of the new user should still be inexpensive. In the new market, where speed can be reduced by orders of magnitude, less expensive memory is feasible. Programmable calculators exploit the speed/cost tradeoff with a hybrid approach, storing a program on an inexpensive medium such as a magnetic card, and transferring it into an internal fast memory for execution. Memory size thus constrains program size, and attempts are being made to increase memory size in programmable calculators without substantially increasing cost. An alternative is to use paging—ie, transferring program segments into memory one at a time, as needed; pages are taken from a bulk medium such as magnetic or paper tape. At the other extreme, the expensive memory could conceivably be eliminated altogether and the program read directly from a less expensive and much slower medium.



SOME MINICOMPUTERS GATHER DUST IN THE CORNER AFTER WOULD-BE USERS DISCOVER THE MACHINE'S DEMAND ON TIME AND POCKETBOOK

A bulk medium is least expensive when read serially, eliminating the need for timing and addressing circuitry and requiring only a minimum number of transducers to sense the data. Serial reading has numerous disadvantages, however; it is slow, it cannot branch conditionally, and stored data are difficult to edit. Nevertheless, advances in technology, such as development of versatile, low cost tape transports, may make serial reading of a bulk medium once again at least potentially practical. If high level instructions, generated by a keystroke, are stored on tape and directly executed by hardware, the processor can operate at full speed on program segments with only moderate tape speeds. For branching or looping, the tape can be backed up. Alternatively, an endless reel of tape can be continuously run forward while the computer picks up one iteration of a program loop on each lap of the tape. Obviously, editing will still be difficult, and wear on the mechanism and on the medium becomes a limitation where programs include many branches. However, most instructions in any program are arranged serially and most data can be



SOFTWARE FOR SMALL COMPUTERS MAY BE APPROACHING THE END OF ITS EXISTENCE

reprocessed serially, so that although search time would far surpass processor time in an inexpensive bulk memory scheme, total running time still remains within limits acceptable to the new customer.

The salient point is that considerable sacrifice in performance may be acceptable in these machines if the base price can be lowered by a factor of several-fold, which is the reduction necessary to bring the price of a small computer below the threshold needed to achieve volume sales.

In the longer term, but still within a few years, new means of random access to bulk media can be expected. This is probable because, in general, a digital state can be sensed more readily than it can be changed, indicating far more numerous possibilities for new types of practical read-only memories or programmable read-only memories for bulk media than for fast read/write memories.

With random access, cost of the decoding matrix, rather than that of read/write memory elements, establishes the cost asymptote for memory, even though its elements may be much more numerous. Hence, if random access can be replaced by inexpensive serial data sensing, substantial cost reductions are possible. Clearly, development of suitable bulk media is a fertile area for innovation. Potential relative merits of these general approaches to the use of bulk media as main memory are summarized in the Table.

Despite the emerging possibilities of bulk memory media, the allure of large, fast random-access memories (RAMs) remains. Ultimate cost constraint of magnetic RAM elements is their discreteness, which introduces an unavoidable lower limit to cost per bit in the manufacturing process. In the case of nondiscrete media, such as LSI, and the more esoteric media, such as magnetic bubbles, the ultimate factor is a much less definable array size limitation, which is necessary to insure an acceptably low rejection rate in production. Production standards have been improved dramatically over the years, and it may be that limiting array sizes are still being substantially underestimated. Thus it is conceivable that large-size RAMs could yet drop enough in cost to reach the new market.

A Leaner, More Precarious Market

The computer market will not again achieve a steady state in either a marketing or technical sense until, first, everyone who has work for a computer can afford to buy one and, second, low cost device technology has stabilized. The first condition will probably be reached within a decade, as low cost memory and input components are developed. Technology can, in principle, improve indefinitely, but in practice, it will stabilize soon after the first condition has been reached. Stabilization will be forced by an industry weary of the current frenetic and economically dangerous pace of development. Until then, the small-computer market will belong to the innovator, since only he can survive in a quickly changing market of ever-falling prices.

In such an environment, the designer will have to change his outlook considerably. He will have to become more sophisticated in assessing characteristics of new devices; as recent history has shown, the key to lower cost is exploitation of novel physical devices. Also, the designer will have to become facile at developing new architectures to exploit these new devices. Indeed, architectural innovations that would have been considered major a few years ago will become commonplace.

Relative Merits of RAM Substitutes

	Size	Speed	Cost	Programming Flexibility
Paging from slow medium into RAM	Large	Intermediate to fast	High	Good
Serial reading of slow medium	Large	Very slow to intermediate	Low	Problematical
Random access reading of slow medium (developmental)	Small to medium	Fast	Low to intermediate	Fair to good

The minicomputer as we know it today will not disappear; rather, it will become part of a range of machines extending in capability from today's least expensive hand-held calculators to the most sophisticated large machines. Sophistication of the largest class of machine will undoubtedly grow, because computers are asked to perform increasingly esoteric functions with greater efficiency. Intermediate sizes for computing and controlling will become standardized and fewer in number, much as proliferating makes and models of automobiles became more standardized 40 years ago.

Meanwhile, present-day minicomputers will lose ground to both ends of this range. They will fall behind the smaller computers discussed here, as an increasing number of users who are not computer professionals realize that a minicomputer requires heavy investment in expertise. On the other hand, many who do not need greater capabilities—now achieved in minicomputers with software—will time-share larger machines, which are more economical than minicomputers as long as they can maintain a substantially higher level of utilization. This leaves the current minicomputer to those who can use it efficiently—meaning those who can use its sophistication and use it frequently.

Displacement of conventional minis by smaller computers is compensated for by one positive factor for the mini market: after a few years, as with any item of consumer technology, the inexpensive model serves to introduce the more sophisticated version, so that the new small computer will develop the market of the conventional mini to its full potential.

Summary

We have attempted to take a broad look at the future of the small-computer market as it affects the designer —stressing small-computer development, which will probably reach a stable state in the not too distant future. Three forces seem to be behind the current flux in the industry:

- Reduction in cost of the CPU relative to other subsystems, leaving the memory in particular as principal obstacle to cost reduction
- Increasing cost advantage of hardware with respect to software for machine control and increasing recognition of the shortcomings of software in the small-computer environment
- Reduction of computer prices to the point where a greatly expanded small-computer market is reachable just one step beyond the industry's current price position, so that cost becomes the principal aspect of design upon which the small-computer designer should focus

The main obstacle confronting the potential small-computer user is software, and the best way to circumvent this is to perform current software functions with hardware. This in turn will require reducing the scope of functions that any one machine can efficiently perform, a gambit allowed by the nature of the emerging small-computer market. The other major change in computer configuration will be replacing or eliminating the large RAMs of current minicomputers, an approach which elimination of software renders reasonable.

Today's closest approximation to tomorrow's small computer is the advanced programmable calculator, which, to some extent, comprises the elements necessary for a true computer—freedom from software, partial exploitation of low cost memory technology, and well advanced efforts to simplify the user's input.

Donald R. Wulfinghoff is a consultant with Booz · Allen & Hamilton, having a computer background in development of advanced computer architecture, device development, and computer marketing. He received an MS degree in physics from the University of Florida.

Restored Processor Function Saves Logic and Improves Performance in Microcomputer System

David R. Ahlgren

MicroMation
San Diego, California

Peripheral interface cost can be reduced by putting into the processor those interface functions that otherwise would leave the dedicated processor idle during their execution

For many years the trend in computer system design has been to remove functionality from the processor and put it into the peripheral equipment, in order to relieve the processor of burdensome and time-consuming chores and permit it to concentrate on its main task—computing. Today, the proliferation of microcomputers places increasing demands on designers to develop low cost peripheral interfaces. One often overlooked way to meet this demand is to restore some functionality to the processor. This can be particularly useful in certain dedicated applications, in which the processor has only one task to perform at a time and has nothing to do when not performing that task.

By utilizing the power of the central processing unit (CPU), the simplified interfaces offer low hardware cost and often improved performance and flexibility. This optimization is utilized extensively in the MM2000 dual cassette system (compatible with Intel's Intellec 80 and its 8080 microcomputer). MicroMation has trademarked the name Microware to refer to this design approach.

In a standard hardware asynchronous modem interface (Fig. 1) for recording binary data on audio cassettes, a universal asynchronous receiver/transmitter (UART) converts parallel CPU data into a serial bit stream with Teletype™ code format. The 1's and 0's are then converted to audio tones—ie, 1200 Hz for a 1, 2200 Hz for a 0—and recorded in that form on audio tape.

On input, this action is reversed: the UART supplies parallel data to the CPU, along with status information such as data output ready, data input available, parity error, and data overrun. It performs other control and signal processing functions as well.

The UART is a large-scale-integration circuit with complexity comparable to that of a typical 4-bit microcomputer. Its functions may be easily transformed to a program for execution by an 8-bit microcomputer. A system program would then pass parallel characters to the UART simulation program just as if it were a hardware UART. The

Component Cost Comparison

Conventional Hardware Design		Microware Design	
UART	$10	Flip-flop	$0.50
Control	3	Control	1
Drivers	3	Driver	0.50
UART Timing	6	UART Program	2
Generator	5	Generator	5
Detector	5	Detector	6
	$32		$15

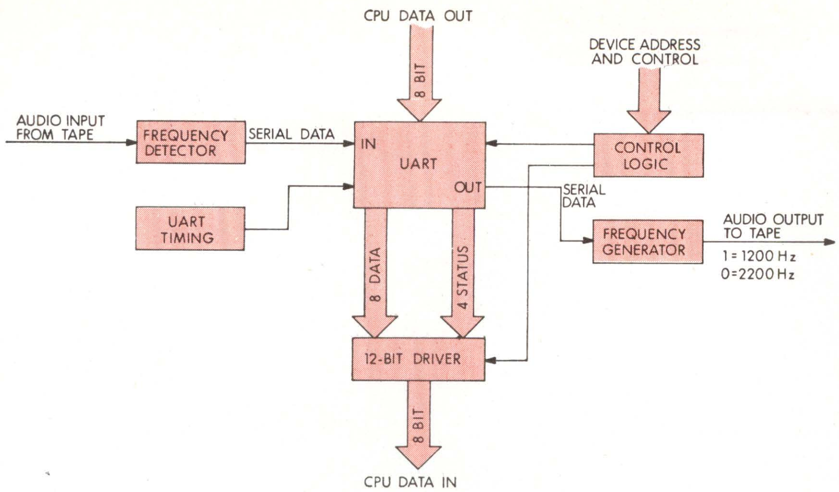


Fig. 1 Old UART-based controller. Integrated UART circuit converts data from parallel to serial, and vice versa, and generates various control and status signals. In conventional system it relieves central processor of much drudgery

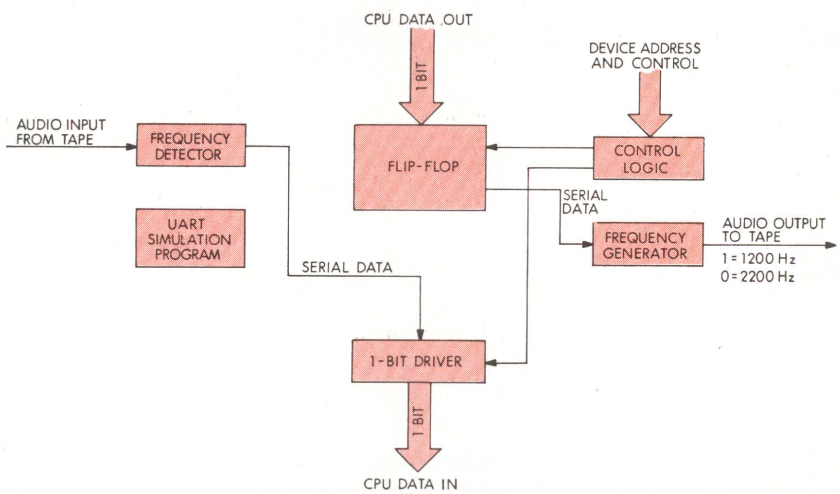


Fig. 2 New microcomputer-based controller. Restoring conversion function to processor simplifies the interface and reduces its cost while keeping the processor busy—even with drudgery—when it would otherwise be idle

UART simulator also processes the serial data stream between the computer and cassette interface.

The Microware audio tape interface (Fig. 2) utilizes this technique. It connects a CPU data output bit directly to the audio frequency generator; the UART program stored in the microcomputer's memory and the basic CPU cycle timing generate parity, serialize the data, and time bit durations.

On input, the procedure is again reversed; serial data from tape are forwarded to the CPU, which converts the serial bits to parallel characters and checks their parity. UART status information normally in hardware is maintained internally in the CPU memory.

Difference in system cost and complexity between hardware and Microware techniques is significant. While 50% savings in parts cost (see Table) are obvious, considerable savings also result from reduction in system complexity. The program that replaces this complexity need be checked out only once, with the same equipment that tests the entire system program. Field maintenance is also simplified. □

APPLICATION NOTE

Flexible-Cable/Connector Simplifies PCB Wiring

John Knudson

3M Company
Electronic Products Division
St. Paul, Minnesota

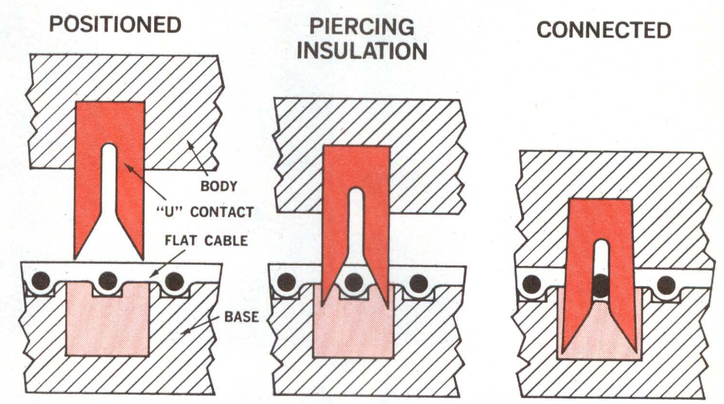
Advantages of mass termination are applicable to twisted-pair or parallel-lay individual wires using a connector system technique that accurately spaces conductors for termination in a U-contact connector that assures firm contacts between flexible cables and connectors on rigid printed circuit boards

A system for easing the transition from flexible cables to rigid printed-circuit boards provides a bonus by eliminating wiring errors and simplifying harness assembly. Flat-ribbon cable/connectors are now used in many areas of the computer industry: mainframes, minicomputers, peripherals, readout devices, machine tool digital controls, and some military applications. Key to the system is a method of termination that involves the use of "U" contacts in the connector. These contacts pierce the insulation without cutting the conductors, strip the insulation from them, and compress them to effect firm grips.

Assembly of Cable and Individual Wire Harnesses

During assembly, conductors of multiple-conductor cable harnesses must be accurately aligned with the U contacts in the connector. Conductors in flat cable are accurately spaced during cable manufacture, but those in a twisted-pair woven cable must be separated and accurately spaced before they can be terminated in a U-contact connector. Therefore, to apply advantages of insulation stripping and mass termination to twisted-pair or parallel-lay individual wires, a handling method was devised that allows mass termination of individual wires in connectors originally designed for flat cable.

Terminating flat cable in a U-contact connector requires four steps. First, a paper liner on the connector cover is removed, exposing a nonconductive transfer adhesive. Second, the cable is positioned on the connector cover, matching the cable's ridged contour to the cover's grooved contour. The adhesive holds cable to cover during handling. Third, this cable/cover subassembly is placed in a fixture plate, and the connector body, preloaded with U contacts, is located over the subassembly. Posts on the cover mate with holes in the body to align connec-



Key to the mass termination of individual wires and cables is the "U" contact, which pierces insulation, strips the insulation from the conductors, and clamps the conductors in a posltive, spring-like grip

tor parts during termination. Finally, the connector is pressed to terminate the cable. During termination, as shown in the Figure, the U contacts pierce the insulation and clamp onto the conductors.

A different fixture accurately positions individual twisted-pair or parallel-lay wires for connector termination. This fixture includes a guide and a holder to space and hold each wire. A pocket for the connector cover, located between guide and holder, registers the connector cover and wires; a clamp holds flat-woven or round-jacketed cable during wire preparation; and a bar removes the wires after termination.

During assembly, about 3 in. of each individual wire is exposed. In woven cable, the braid is pulled to free the desired wire length, then tied to secure the remaining woven section of the cable. The cable is clamped in the fixture, with the wires separated over the connector cover. All wires are placed in the guide slots and pulled into the wire holder, which cuts the insulation and firmly holds each wire. Proper wire location is then checked with a comb. With all wires positioned, the connector body is placed over the wires and cover, the fixture is moved to a parallel-action press, and the connector is pressed to terminate all individual wires in the cable. The connector/cable assembly is then removed from the fixture with the bar, and the wires are trimmed at the connector surface.

Parallel-lay, flat-woven cables can be daisy-chained; that is, connectors can be placed anywhere along the cable to give multiple interconnections. In daisy-chaining, the fixture wire holder is replaced by a guide that holds individual wires in place on each side of the connector cover. The previous steps are then followed for each cable/connector assembly. Daisy-chaining is not recommended for twisted-pair woven cables since the twists in the cable must be moved from the position of the connector to another section of the cable.

Applications

Development of a fixture to handle individual wires in cable assemblies has extended the connector/cable system to applications such as harnesses where grouped wiring is used on one end and random wiring on the other. The cable can be terminated with a U-contact connector at the grouped-wiring end and with terminals or direct soldering on the random-wired end.

A U-contact connector can also be used in applications requiring the electrical characteristics of twisted pairs. Suitability of the connector/flat-ribbon and woven-cable system depends upon a number of considerations, including electrical and environmental considerations, available connector and cable configurations, and compatibility with IC sockets and wrap post patterns.

U-Contact Connectors

Connectors of four different styles may be used to make the transition from individual wires or flat cable to a rigid circuit board: printed-circuit board (PCB) connectors, socket connectors, card-edge connectors, and dual-in-line (DIL) plugs. All have beryllium-copper contacts, located in glass-reinforced thermoplastic. PCB contacts are plated with bright tin; socket, card-edge, and DIL plugs are gold over nickel plating.

Permanent connection between cable and circuit board is made with a PCB connector. Disconnectable transitions are made with female-socket connectors, card-edge connectors, or DIL plugs.

PCB-type connectors are the simplest. Contact tails from the connector body are soldered directly into corresponding holes in the board. Female socket connectors make depluggable transitions from the cable to round or square male posts. Strain-relief covers, together with mating headers, are optional. Headers have right-angle or straight round contacts for soldering into holes on PCBs, or square contacts for wrapping.

Individual-wire or flat-ribbon cable can also be terminated in card-edge connectors. These connectors are dual readout, with bifurcated contacts which mate to pads on each side of the PCB.

DIL plug connectors also form a disconnectable transition to individual-wire or flat-ribbon cables. They have rectangular pins for mating to standard DIL sockets, or can be directly soldered to the boards. □

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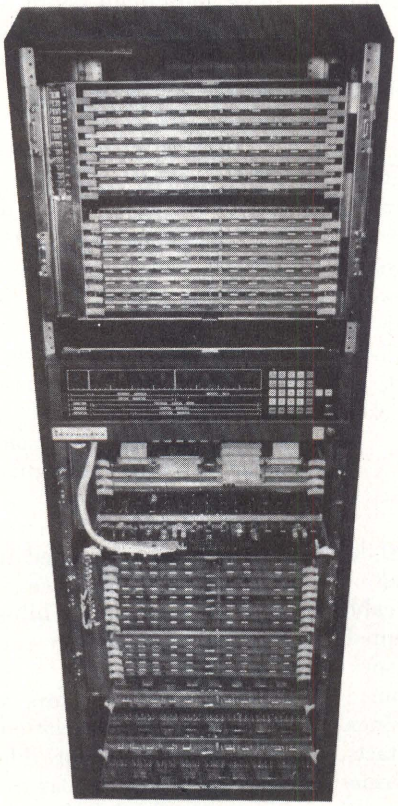


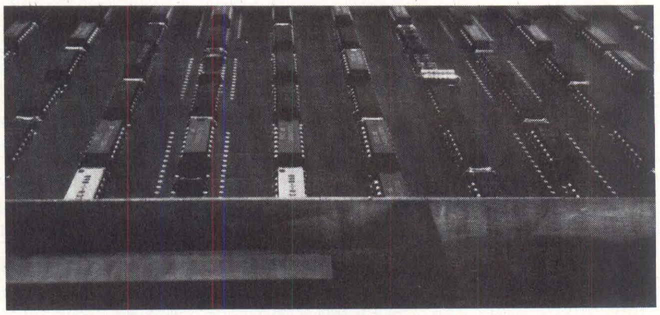
The 8/32 MEGAMINI – with a full Megabyte.

MEGAMINI SOFTWARE: POWERFUL, FLEXIBLE, EASY-TO-USE.

Today's hardware must be designed to ease your software effort. You shouldn't have to spend a lot of expensive programming time trying to figure out how to get around minicomputer hardware limitations. With the 8/32 Megamini you don't – because there are none.

For example. The direct addressing capability of the 8/32 Megamini allows you to build programs and data arrays in any size up to the amount of memory you have – no more 64K limits.

It also means we can give you versatile and powerful software to help lower the cost of building your system. Software with a multi-tasking operating system, OS/32MT, with unique multi-user



Multi-Wire Technology – a key to MEGAMINI performance.

Editor's Note: Beginning with this issue, *Computer Design* will include a monthly department on microprocessors and microcomputers that will make it easier for our readers to obtain useful information on these subjects in one section of the magazine. The department will cover basic and advanced information on current technical trends, design, and applications, including both hardware and software and any other pertinent material. (In addition, we will continue to publish full-length, in-depth feature articles.)

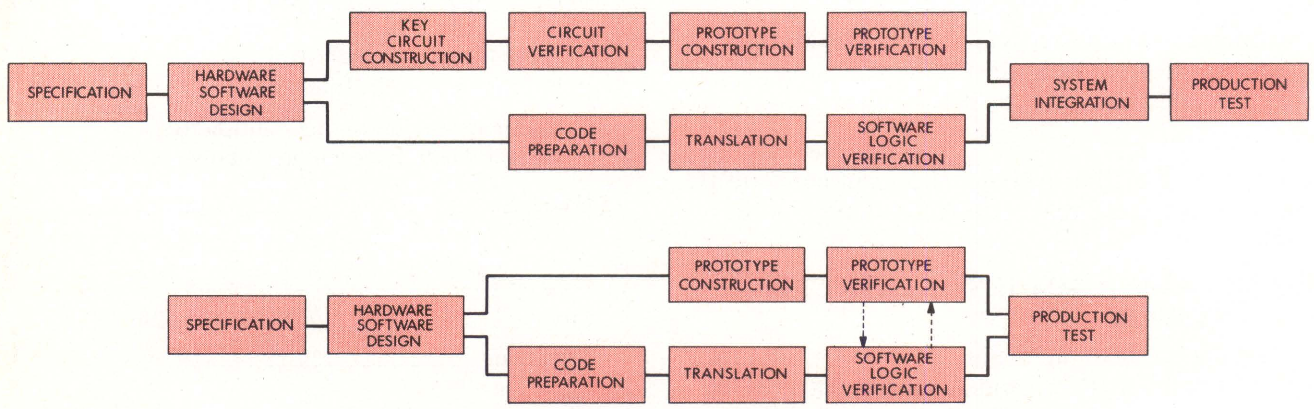
Please do not hesitate to send us your suggestions as well as criticisms on the content. Unless specifically requested to the contrary, all material submitted will be considered for publication, with credit to the contributor.

In-Circuit Development System Simplifies μComputer Design Cycle

Microcomputer engineers and programmers can now retire their traditional product development tools and work directly on prototypes having packaging identical to that of production models and operating in the environment of the actual product. Intellec MDS, available from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 at a basic price of $3950, is a complete microcomputer development system that can be tailored with numerous memory, input/output (I/O), and peripheral expansion options to meet the full spectrum of cost/performance requirements of equipment manufacturers. Extending the applications of automated development systems into production operations and field engineering, it can be used to prepare fault-isolation routines for production testing and field maintenance, automate production test and troubleshooting, and support in the field such activities as system installation checkout, operating analyses, development and checkout of field modifications, and customizing and loading equipment user programs.

In-circuit emulator (ICE) modules provide system emulation and diagnostic capabilities, and make the system processor-independent. Basically, ICEs allow the programmer to use system resources "transparently" as if they were physically a part of the prototype during emulation; they operate as the prototype's master circuitry, allowing software and hardware to be developed in the same environment, and provide a highly automated "window" through which the developer can control prototype operation and observe results in detail.

The company will initially supply two optional modules with the basic system: ICE/80 supports development of equipment based on MCS-80 microcomputers and other products utilizing the 8080 silicon-gate n-channel metal-oxide semiconductor 8-bit central processing unit. ICE/30 supports series 3000 Schottky bipolar large-scale integration computing elements; an optional bipolar read-only memory (ROM) simulator with max access time of 130 ns and capacity modularly expandable from 8 to 32 kilobits simplifies series 3000 micro-



Typical development cycle (above) using conventional design aid and (below) Intel Corp's Intellec MDS microcomputer development system program development. According to William Davidow, Microcomputer Systems Div manager, the company will support future microcomputer families with ICEs and software enhancements.

An ICE module connects the development system to the prototype microcomputer system's data and control bus (and to other points, if desired, via auxiliary connectors). This allows the ICE to take "snapshots" of any state transitions that may occur during prototype operation. The snapshots are translated into readable system images, which are shown on the display console, logged, or stored in bulk memory for further analysis.

The basic system includes an 8080-based central processor module, while subsystems consist of a universal bus with multiprocessor and direct memory access (DMA) capability; 8-level maskable priority interrupt structure; real-time clock plus a high speed clock system available through the bus; fully protected, >35-A power supply; 2-kilobyte ROM for the resident monitor; 16 (expandable to 65)-kilobyte random-access memory; numerous peripheral interfaces; and, optionally, an IBM-compatible diskette bulk memory system with supporting controls, interfaces, and software; DMA channel controllers; general-purpose I/O modules; universal prototype board; and a variety of accessories.

Currently available resident software includes a system monitor, 8080 macro-assembler, and text editors, enabling program generation, diagnostics, debugging, and documentation of either software or hardware data. For programming, only two or three passes are needed: symbol table, source listing and error diagnostics, and object code; the diskette or list output peripherals allow combination of the second and third. Hexadecimal object code generated can be converted by the monitor in programmable-ROM programming format.

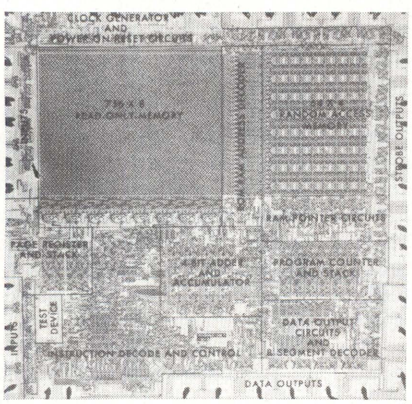
A resident text editor, written in the company's high-level PL/M™, manipulates on command either entire lines of text or selected characters. Text may be edited with string insertion or deletion, string search, or string substitution commands.

Microprograms for series 3000 systems are generated externally with CROMIS (Cross Microprogramming System), then entered into the Intellec MDS for further development and in-circuit prototyping with ICE/30 and its ROM simulator.

Circle 170 on Inquiry Card

'$9.98 Computer' Combines 6K ROM, 256-Bit RAM on Single MOS/ LSI Chip

A microprogrammable processor designed for low cost processor and controller applications contains all the essential elements of a "microcomputer-on-a-chip"—arithmetic and control sections, program storage, data storage, and input/output (I/O) facilities. Although originally intended for single-chip calculators, these elements, combined with a versatile instruction set, allow the S9209 from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 to be used in a wide variety of calculator and non-calculator, fixed-program applications.



American Microsystems, Inc microprogrammable processor for low cost processor and controller applications combines—on a single MOS/LSI chip—a 6K ROM organized as 756 8-bit words, and a 256-bit RAM implemented as four registers, each containing 16 4-bit words

It "provides users with the most cost-effective programmable computing element available, and can be adapted to perform specialized calculator functions as well in such seemingly remote areas as credit verification terminals and special-purpose industrial timers," states AMI applications manager Alex Goldberger. Other typical uses include portable data entry devices, low-cost cash registers, small terminals, and appliance controllers.

The mask-programmable p-channel, silicon-gate, metal-oxide semiconductor, large-scale integration chip contains permanent and temporary data storage capability, 4-bit arithmetic unit, accumulators, registers, program counter and stack, input and output data lines, and other associated circuitry. It can be used by itself, or, with a small amount of external hardware, several may be connected in tandem for increased-capability requirements. A 6K read-only memory (ROM), organized as 756 8-bit words, incorporates microinstructions to tailor the chip for performing the desired system functions; a 256-bit random-access memory, implemented as four registers each containing 16 4-bit words, is used for temporarily storing information in the processor.

A set of 33 basic instructions includes arithmetic, data manipulation, test, transfer, data addressing, and I/O types. Typical instruction cycle time is 15 μs.

A comprehensive software set—including a cross-assembler, simulator, and test program generator—supports development of custom programs. Also available is a hardware simulator to verify device design in actual operating conditions prior to release of the ROM pattern to manufacturing.

The circuit is supplied in either 28- or 40-pin dual-in-line plastic or ceramic packages, and has been preprogrammed into several standard, special-purpose devices. In quantities of 5000, unit price for a custom-programmed version is $9.98. Samples are available from stock.

Circle 171 on Inquiry Card

Software Supports Intel Microprocessors

A set of macro-assemblers for Intel 4004, 4040, and 8080 microprocessors is being offered by Microtec, PO Box 337, Sunnyvale, CA 94088. Written in FORTRAN IV, programs operate on any computer system having a word length greater than or equal to 16 bits as well as 16K words of main memory. Most programs can be assembled without modification.

Featured are symbolic addressing, relative addressing, and constant generation; a powerful macro facility and conditional assembly statements; and a set of listing and punch control pseudo-operations. Diagnostic error messages are also provided.

Programs are modular and commented and consequently can be modified for a user's individual requirements. Priced at $800, they will be delivered on computer-readable media along with a manual, source listing, and a test program (with its output listing) which allows assembler operation to be verified.

Circle 172 on Inquiry Card

Service Center Evaluates Present/Future Microprocessors, RAMs

Macrodata Evaluation Service Center for evaluating and characterizing microprocessor devices and 4K RAMs

An Evaluation Service Center, fully equipped with large-scale-integration, automatic test equipment for evaluating and characterizing microprocessor devices and 4K random-access memories (RAMs)—those commercially available now as well as those currently in development and entering the market—has been opened by Macrodata Corp, 6203 Variel Ave, Woodland Hills, CA 91364. The service is intended primarily to aid small to medium-size users who are presently evaluating or planning to evaluate microprocessors or RAMs for their new designs. Typically, these companies cannot afford the $200,000+ investment in automatic test equipment or properly characterize the devices while in the design/evaluation phase.

Using the concept of diagnostic emulation on MD-501 and -154 test systems, microprocessors or RAMs can be evaluated and data generated to define precise operating regions and confirm system operational capabilities before the user commits to large-quantity buys.

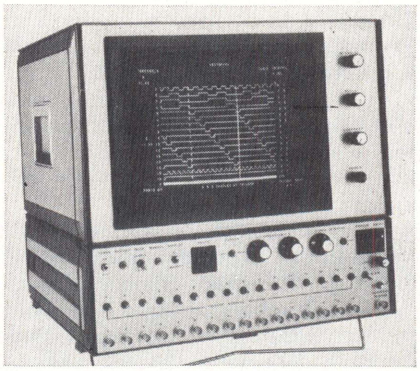
Circle 173 on Inquiry Card

Logic Recorder Debugs Microprocessors

Debugging "anyone's microprocessor" is the purpose of the V-16 logic recorder/analyzer from Vector Associates Inc, 685 Station Rd, Bellport, NY 11713. On its 12-in. raster scan display, 16 logic traces can be monitored and shown in a timing diagram presentation. Character generator readout of all front-panel switch positions is shown, and two logic families can be displayed simultaneously. Front panel provides 16 BNC-connector input channels, each capable of handling digital data from 50 ms through 50 ns (20 MHz) inclusive, with 10 switch-selected voltage thresholds from +10 through −10 V.

By means of a movable cursor, the display's Y-axis can be positioned anywhere within the X, of Δt, axis, permitting the user to look both forward and backward in time, at increments from 0 through 256.

A 16-bit trigger address register watches for a pattern set up on 16 "1," "0," or "don't care" toggles. When the pattern appears either at the front-panel BNCs or rear-panel microprocessor input/output, the re-



corder triggers. Final record following the trigger can be delayed by up to 1000 clock intervals from a thumbwheel-selectable trigger delay generator. All features mentioned are standard; optionally, a complete Polaroid photo package is available.

Circle 175 on Inquiry Card

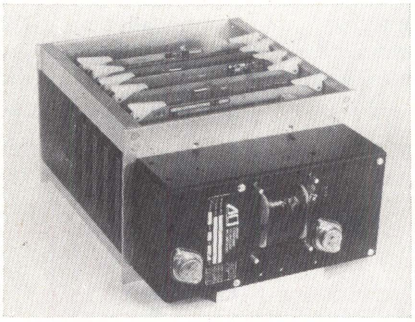
Microcomputer Workshops To Offer Hands-On Experience

A series of monthly workshops is being presented by PCS, Inc, 5467 Hill 23 Dr, Flint, MI 48507 to provide the hands-on experience necessary to handle its MicroPac 80 microcomputer. Each 5-day course will familiarize students with all hardware and software available as they configure and program their own systems. Classes are scheduled to begin Sept 8, Oct 6, Nov 3, and Dec 8.

Circle 174 on Inquiry Card

Protyping/Production System Is for Rockwell μP-Based Applications

To provide a convenient method of prototyping and/or production of Rockwell's PPS-4 microprocessor—after the PPS-4 program has been debugged in a development system



—is the purpose of the UMPS-4 universal microprocessor system from Applied Computing Technology Inc, 17961 Sky Park Cir, Irvine, CA 92707. An integral card guide/connector assembly is mounted in an aluminum frame with a prewired bus. A maximum of 14 cards may be used.

A typical system is configured by inserting standard UMPS-4 cards. In addition, component boards are available for custom wiring of special boards using standard dual-inline-package and/or PPS circuits. Custom board interconnect provisions and interface cables allow for system fabrication with minimum effort.

The basic system includes a prewired card cage with six connectors, central-processing-unit board, and universal programmable read-only memory board. Additional modules and power supply are available. All cards are dimensionally identical and operate with a standard 100-pin connector.

Circle 176 on Inquiry Card

Macro Cross-Assemblers for Intel μProcessors Are Cost-Effective

A combined macro cross-assembler for Intel 4004 and 4040 microprocessors operates on IBM Systems 360/370 and DEC PDP-10 computers. Written in assembly language in both cases, the assemblers, available from Zeno Systems, Inc, 2210 3rd St, Suite 110, Santa Monica, CA 90405, are claimed to be at least 50% more cost-effective than competing packages written in FORTRAN.

Although functionally equivalent to manufacturer-provided software, several enhancements have been added for user convenience: improved user interface and operating environment, clear and extensive error diagnostics within the assembly listing and summarized in a separate file or at the user's terminal, complete variable cross-reference listing, improved assembly listing format, and option control by additional, easy-to-use pseudo-operations.

The assemblers may be obtained under a one-time licensing agreement or utilized on a pay-as-you-go basis via time-sharing networks.

Circle 177 on Inquiry Card

Mostek Becomes Alternate Source for Fairchild Microprocessor

Termed "the industry's first true alternate-source arrangement for sophisticated large-scale integration (LSI) technology," Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 will manufacture the F8 microprocessor set of Fairchild Camera & Instrument Corp, Integrated Circuits Group, 464 Ellis St, Mountain View, CA 94042 as an alternate-source supplier of the family of 8-bit n-channel devices.

Mostek will supply the complete 5-circuit family, including central processing unit and read-only memory, dynamic and static memory interface, and direct memory access circuit. In addition, it will alternate-source the 3538, a 256 x 4-bit static random-access memory suitable for use with the F8 set.

The firms will also cooperate in expanding current F8 hardware, software, and support programs as well as in developing new F8 components. Mostek expects to have sample circuits available this month.

Circle 178 on Inquiry Card

Environment-Proof Microcomputer Enhances Traffic Control

On the basis of a microcomputer which is claimed to be totally insensitive to environmental effects, a line of traffic control equipment has been developed to provide economically attractive solutions for complicated intersections as well as coordinated traffic control systems. The computer and controllers are designed and manufactured by Philips Telecommunicatie Industrie B.V., Traffic Automation Group, PO Box 32, Hilversum 1301, The Netherlands, which states that no knowledge of software or computer techniques is required, so that traffic experts are able to concentrate entirely on traffic problems.

The microcomputer features 16K, 8-bit-word maximum address capacity and 6-μs average instruction processing time. Its 500-word/module memory consists of read-only, programmable read-only, and random-access and can be programmed manually; if desired, programs can be written in from a central point via interface units connected directly to a 6-m (max) common bus. Ambient temperature for the computer housed in a cabinet may range from −20 to 80°C.

Complex intersections with up to 32 signal groups can be controlled. In this capacity, the computer is an all-purpose traffic controller, equipped with lamp switches, conflicting-green monitoring units, detector interfaces, and local-operator aids such as a time-setting unit and a local-control panel.

In the function of a master controller, the microcomputer coordinates several intersection controllers and selects the most suitable coordination program on the basis of traffic flow and occupancy data, measured at strategic points; thus it is possible to control a whole sub-area. As an area controller, it supervises several master controllers; this includes coordinating the master controllers and the signalling from intersection and master controllers to a central controller, which may be equipped with a teleprinter for communication with the area control system and with a wall map displaying instantaneous traffic situations and operational conditions.

The system can be optimized by employing a general-purpose computer to provide such extra facilities as traffic statistics, new traffic program calculations, or transmission of new programs to the master controller.

Also in the equipment line is a computerless intersection controller for areas where two to six signal groups are sufficient.

Circle 179 on Inquiry Card

μComputer Bus Structure Provides Optimum Flexibility

Volume production and shipments of Mike 2 microcomputer modules have begun, according to their producer, Martin Research, 1825 S Halsted St, Chicago, IL 60608. Designed for maximum flexibility, system architecture features a bus structure which permits any board to be inserted in any position on the bus; the system is expanded by simply plugging additional boards onto the bus.

All critical control signals are decoded directly on the central processing unit (CPU) board and piped around the system on the bus. Hardware interfaces to the microprocessor generally need only two chips—a strobing decoder, and a latching device (for output ports) or 3-state driving device (for inputs).

The CPU board contains an Intel 8008 microprocessor, crystal-controlled oscillator, and all system timing; bidirectional bus drivers allow addition of many accessory boards. The console board has six 0.3-in., 7-segment display digits and a 20-key calculator-type keyboard; unlike with systems having banks of toggle switches and lights, programming is simple since codes are easily visualized.

Up to 1K of random-access memory (1024 8-bit bytes or 8192 bits) and 2048 bytes of programmable read-only memory (p/ROM) can be accommodated on the third board. The last—a breadboard—has a connector for interfacing to the system bus; all power and bus signals are accessible.

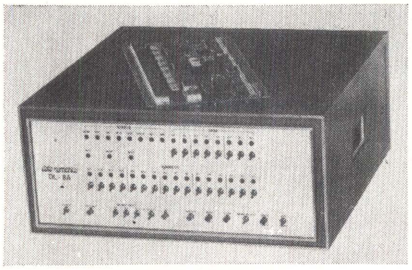
Also included is a monitor, consisting of 256 words in a single p/ROM, which permits writing instructions into memory at any location, and reading instructions, by simply punching keys on the keyboard.

The system comes complete except for a custom cabinet and a power supply. Boards each measure 5.5 x 7 in. and include a 50-pin connector at the rear which attaches to a 50-wire flexible cable (18 in. provided). The boards stack up, separated by rigid metal spacers. Power requirements are 5 V, 1.4 A; −9 V, 70 mA.

Circle 180 on Inquiry Card

μComputer System Assemblies Accept Any 14- to 40-Pin Component

Taking into account potential pin configuration changes that may occur as microcomputers become more widely used, Data Numerics Inc, 141-A Central Ave, Farmingdale, NY 11735 has designed model DL-8A with wirewrapped socket board



assemblies that will accept any component having from 14 to 40 pins. Problems inherent in printed circuit card and card file construction are said to be eliminated; and, since extender cards are not used, servicing is easier and system debugging is not burdened with the time-consuming task of reloading volatile solid-state random-access memory (RAM) each time an extender card is installed or removed.

Included with the wirewrapped socket system are a 4K RAM (expandable to 64K), mounting hardware for 2K programmable read-only memory (p/ROM), four input and four output ports, communications channel, interrupt system, and direct memory access, as well as a control panel, power supply, input/output interfaces, selected peripheral devices, and enclosure.

Software is systems oriented and includes cross-assemblers for DEC PDP-8 and -11 computers, p/ROM and paper-tape loaders, hardware diagnostics, and hardware debug routines. □

Circle 181 on Inquiry Card

Granted, our new ADM-3 is basic. Especially if you compare it with all the smart video terminals around (our ADM-1 or -2, for example). But the $995 unit price puts it into a different perspective.

As simple as it is, the ADM-3's one-card brain can help you move a lot of data. And it's compatible with most popular computers. That means, it fits all kinds of applications. Including yours.

Here's what you get for $995. 12" diagonal screen. Full or half duplex operation at 11 selectable data rates. Bright, easy-to-read characters — 960 or 1920, displayed in 12 or 24 rows of 80 letters. 59 data entry keys arranged like on a typewriter which keeps operator training short and basic, too. What's more, our ADM-3 is alert. It says "beep" when you come to the end of a line. The rest of the time, it just keeps cool and quiet.

Our DUMB TERMINAL also offers you room for improvements. Its RS 232C interface extension port lets you hook up hard copy printer, magnetic tape recorder or additional (smarter) data terminals. And with a few options, you can make our ADM-3 answer back. Increase its vocabulary by adding upper and lower case. Transmit and receive independently selectable rates. Even enter just numbers on a numeric key pad.

After counting all its limited blessings, you have to admit one thing: you simply couldn't ask for more for $995. At this low level, you can afford to order a dozen or more DUMB TERMINALS (and buy them at our even lower quantity discount price).

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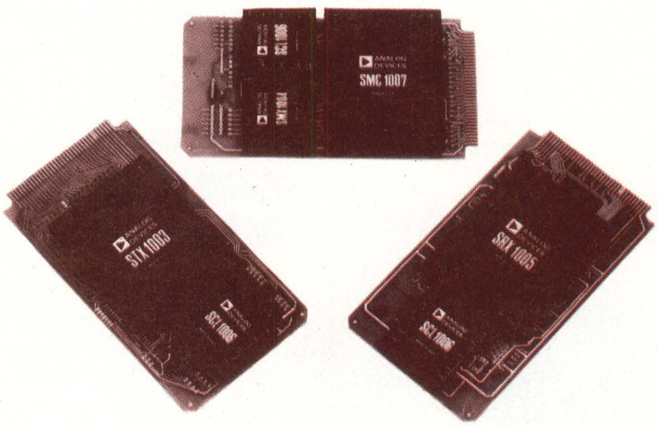
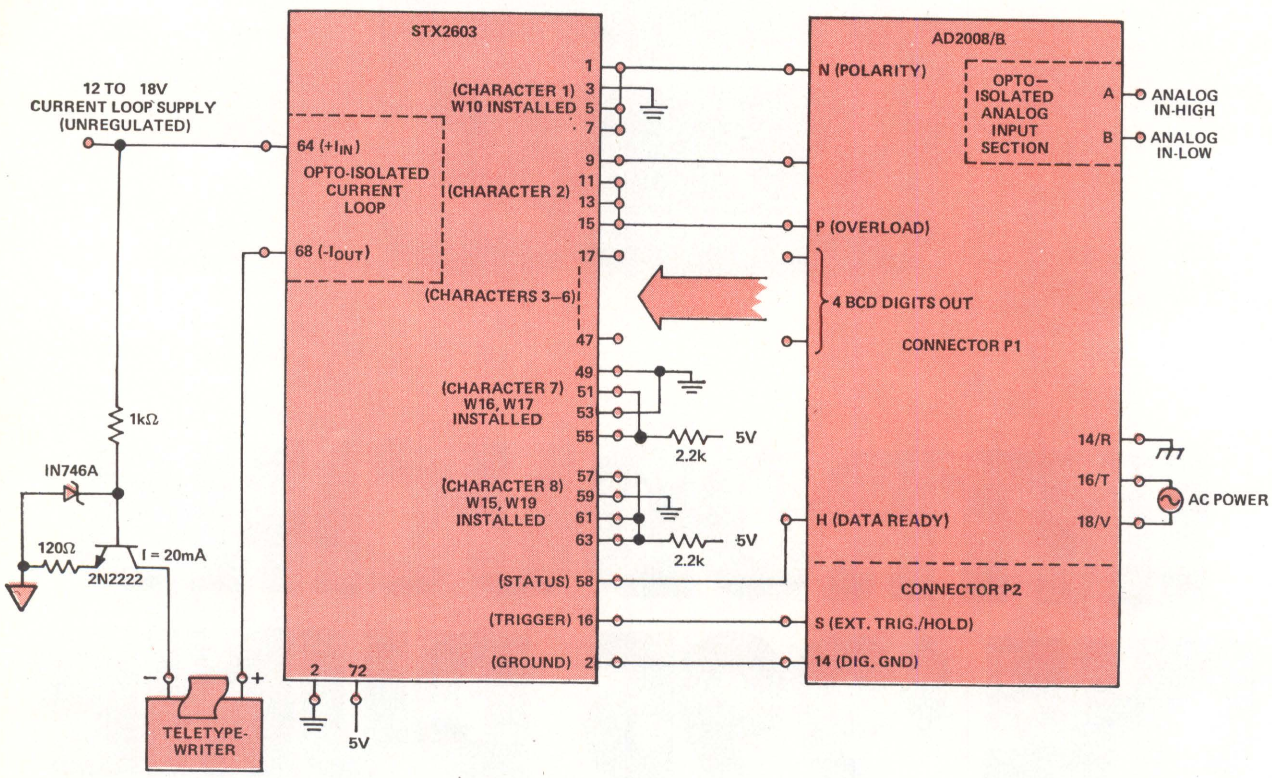
INTRODUCING THE $995 DUMB TERMINAL.

PRODUCT FEATURE

Subsystems Ease Between Parallel ASCII-Compatible



Communication between analog-to-digital or digital-to-analog converters, which function with parallel digital data, and asynchronous serial ASCII-compatible teletypewriters and computers is simplified by a family of card-mounted subsystems introduced by the Modular Instrumentation Div of Analog Devices, Inc. SERDEX (SERial Data EXchange) subsystems are based on the company's building-block SERDEX modules that are used in control and automation applications.



Interface hookup, illustrating the use of shift registers on a Serdex STX 2603 transmitter card, in an application where an AD 2008/B digital panel meter (DPM) is interfaced to a teletypewriter through the transmitter subsystem module. Using this arrangement, the DPM will convert upon receipt of a "?" typed in the teletypewriter, and transmit the data back after a conversion has been completed

Interface Digital Data and Equipment

The subsystems relieve system interconnection problems while maintaining the design flexibility of the modules. Three subsystem cards serve as transmitter, receiver, and multiplexer—in place of five units in the module family (serial data transmitter, serial data receiver, two modules which form a multiplexer, and a clock).

Configuration

A transmitter converts parallel output data from analog-to-digital converters into asynchronous serial ASCII data that can be handled by a teletypewriter or computer while a receiver reverses the procedure so that the output of the central control system can be used by digital input devices. The multiplexer subsystem allows up to eight transmitter or receiver subsystems to be interfaced in any combination to a control device through a single twisted-pair current loop.

All data transmission to and from SERDEX systems is by 2-wire data links using either optoisolated 20-mA current loops or direct TTL. The systems can be controlled either by keyboard commands from teletypewriters or by computers programmed in high level languages.

Each subsystem card uses the features built into the corresponding module; ie, a transmitter card includes a transmitter module, a receiver card includes a receiver module, and a multiplexer card includes a multiplexer module. Each card has a clock module with wire jumper programming for baud rate. Other jumpers on the cards control word length (5, 6, 7, or 8 bits/char for transmitter and multiplexer; 7- or 8-bit char for receiver), number of stop bits (either 1 or 2), and parity generation and verification, if desired. In addition, the transmitter and receiver cards include necessary pullup resistors, the transmitter card has two shift registers to expand the module's ability to send ASCII control characters, and the multiplexer card includes a multiplexer controller.

Only 5-V power, current loop driver (where needed), and appropriate data interconnections are required to implement a complete system. All cards are programmed for teletypewriter operation at 100 baud (1.76-kHz clock rate) when delivered but data transfer rates can be programmed for other applications at up to 19.2 kilobaud (307 kHz) by inserting jumpers. Spare pins are provided for applications where external logic or switches are needed for programming functions or where external shift registers are desired.

Because isolated current loop transmission is the most common application, all subsystem cards are jumper programmed for this mode. However, when the isolation or noise immunity inherent in the current loop is unnecessary or when high speed data transmission is desired at greater than 4800 baud, the current loop can be bypassed to permit direct TTL input and output interfacing to TTL or EIA RS-232 line drivers and receivers.

Normally, the transmitter card is programmed for half-duplex operation and the receiver card is wired for full-duplex. Each can be changed to the other type of operation by removing jumpers.

Specifications

Cards measure 4.5 x 8″ (114 x 203 mm), 4.5 x 8.375″ (114 x 213 mm) including card-edge connector fingers. Each card is supplied with card releases and connector.

Power requirements are 5 V at 625 mA for transmitter, 575 mA for receiver, and 725 mA for multiplexer. Operating temperature range is 0 to 70°C.

Price and Delivery

SERDEX STX2603 transmitter and SRX2605 receiver subsystem cards are priced at $395 each in 1- to 9-piece quantities; SMX2607 multiplexer cards are $450 each for 1 to 9. OEM quantity pricing is available. Delivery is from stock. Analog Devices, Inc, PO Box 280, Norwood, MA 02062. Tel: (617) 329-4700.

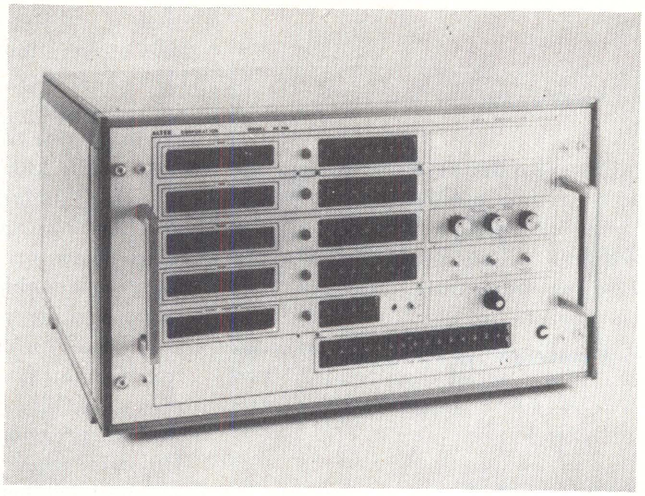
For additional information circle 199 on inquiry card.

PRODUCTS

Digitizer Data Acquisition System Records Positional Information in Digital Form

AC 74 provides a reliable means of digitizing measurements from all types of stereoplotters, comparators, coordinatographs, and film analyzers. Elimination of most complex circuitry simplifies operation. Using rotary or linear encoder input, the system displays up to four 6-digit values and transmits the information to any digital recording device or computer. Optical, magnetic, or brush contact encoder signals are conditioned to provide up/down pulses to counter display boards. Counts are presented on resettable 6-digit, 5 x 7 dot matrix LED displays. Features include encoder input conditioning, patch panel programming, event counter and fixed address identifiers, point and rate recording modes, selectable 1:2:4 count, pushbutton presets for all counters, and interfacing to any digital device. Optionally available are 16- and 54-char keyboards; incremental output, including vector increments from 001 to 999; scaler—variable multiplier from 0.0001 to 9.9999; and planimeter—direct readout of area or volume. **Altek Corp,** 2141 Industrial Pkwy, Silver Spring, MD 20904.

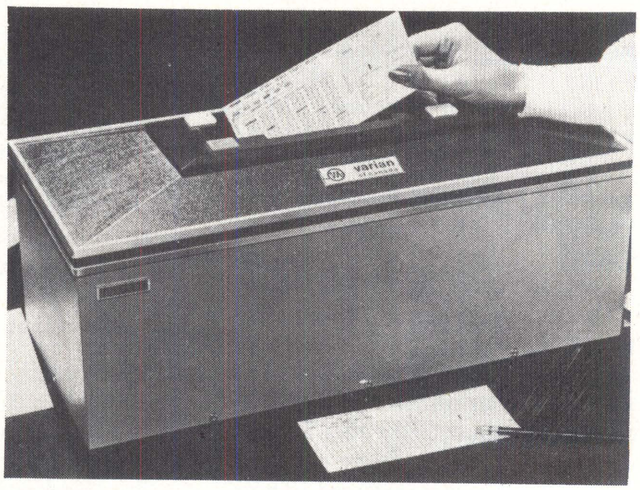
Circle 200 on Inquiry Card



Pollable, Interactive Transaction Terminal Provides Real-Time Replies

T-Scan accepts up to 340 bits of mark sense card message input and 64-char high speed printer outputs of up to 374 positions on the same card. A 24-bit binary field on the card called T-line, used for transaction audit and control, is optically scanned and may be preprinted on the card or post-printed by the integral high speed printer for later card re-use. Card size is that of an 80-col punched card. Up to 63 pollable addresses are available. Typ polling frequencies are 15 to 30 terminals/s. Asynchronous transmission of ASCII code is used at baud rates to 4800. Interfaces include RS-232-C, current loop, and differential voltage driver. Terminal operation is simple: the operator simply marks the card and inserts it in the terminal, and, in 4½ to 5 s the card is ejected with the output message. Entire unit, including the 22-col, 1100-line/min. printer, is packaged in an integral 21.5 x 9.75 x 11" housing. **Varian Data Machines, Peripheral Products Div,** 12062 Valley View St, Garden Grove, CA 92645.

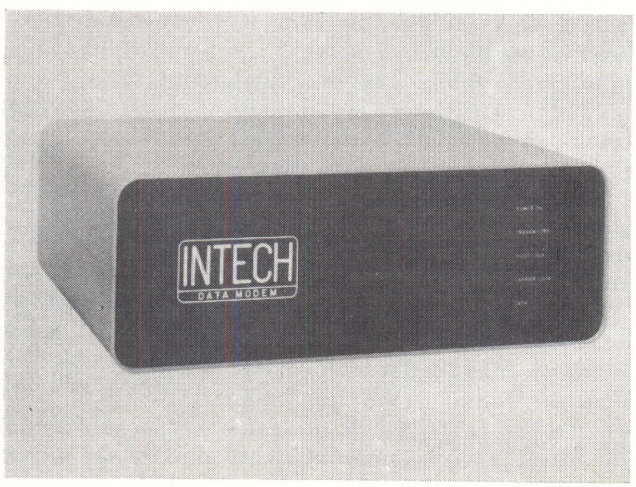
Circle 201 on Inquiry Card

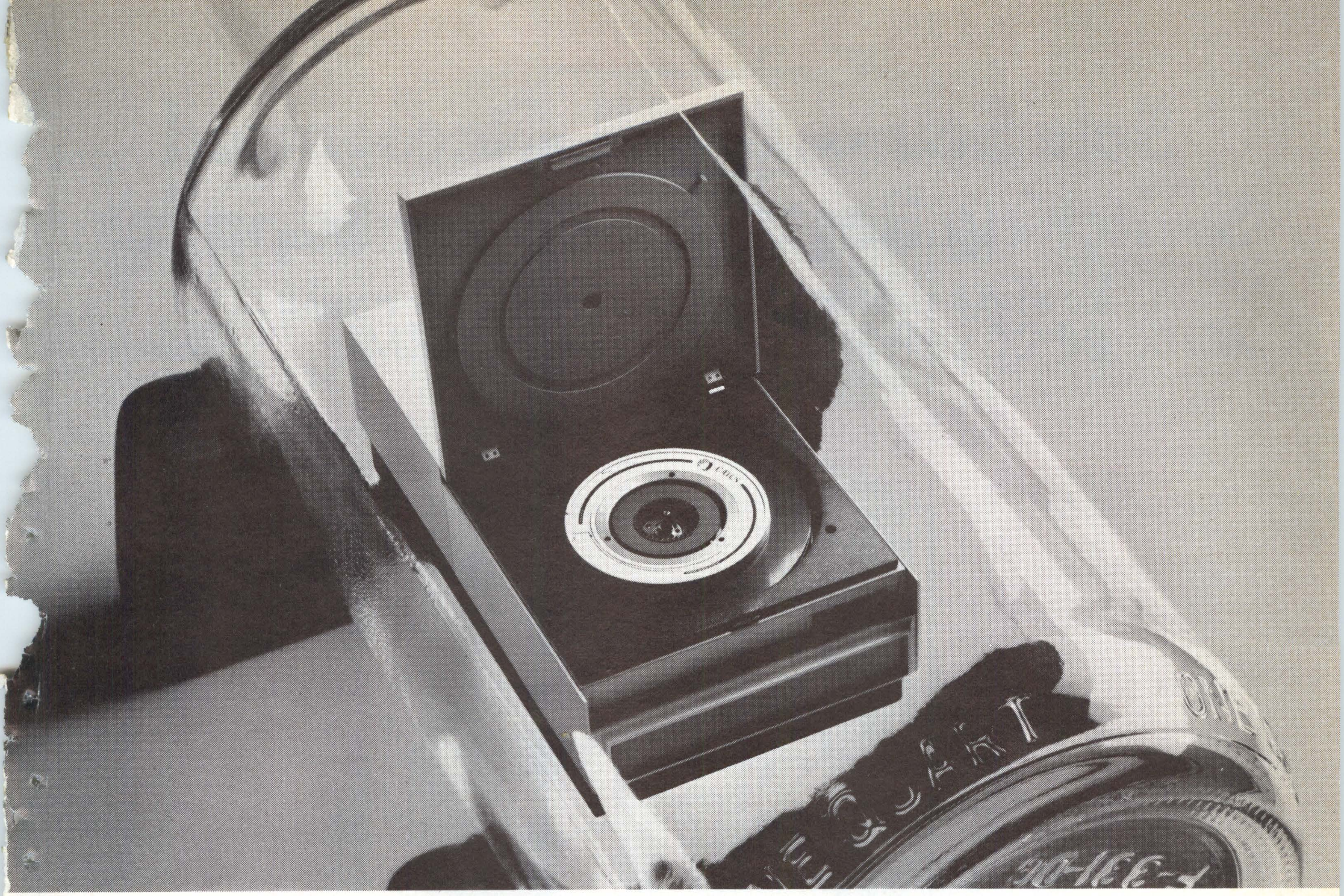


Data Modems Suited for Terrestrial Microwave Links, Satellite Communications Ground Stations

Designed for use on broadband coaxial transmission networks, terrestrial microwave links, or satellite links, particularly for data-under- or over-voice applications, low cost modems feature data rates of 1200, 2400, 4800, or 9600 bits/s and 19.2, 50, or 230.4 kilobits/s as std, with higher available. They are ideal for either multipoint polling or point-to-point dedicated service, are simple to install and maintain with no user adjustment required, have all solid-state ICs for max reliability and low power consumption, and offer quick and easy self-checking plus worldwide compatibility. Basic unit can be configured for 1-way, 2-way alternate, or 2-way simultaneous operation. Interchangeable interface options allow use of RS-232-C, Bell 303 current, or other special arrangement. There are no operating controls. LED status indicators provide visual monitoring of operational status and signal quality. **Intech Laboratories, Inc,** 4175 Veterans Hwy, Ronkonkoma, NY 11779.

Circle 202 on Inquiry Card





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The Trident Series has one of the lowest cost-per-byte ratios in the industry.

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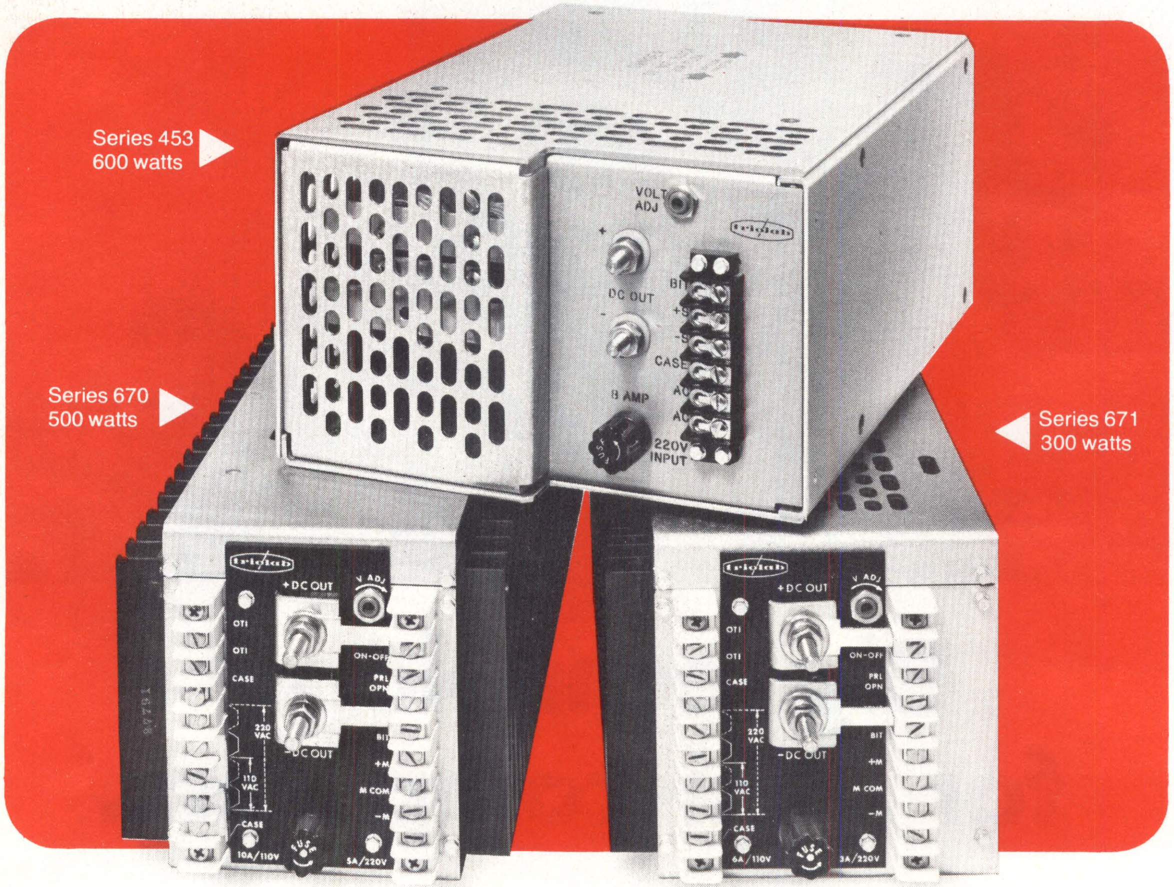

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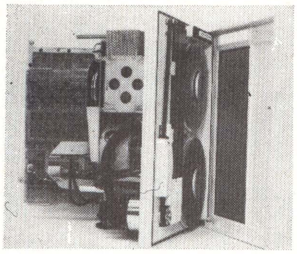
☐ **ARIZ.**—Cleveland Enterprises, (602) 996-6130 ☐ **CAL.**—Northern: H.K. Foraker, (415) 657-2213; Southern: Trio Labs, (213) 820-3254 ☐ **COL.**—Cleveland Enterprises, (303) 423-3707 ☐ **CONN.**—Zaslow Sales, (203) 242-7781 ☐ **FLA.**—Walker-Barkman, (305) 777-1551 ☐ **MD.**—R. L. Engineering, (301) 760-5533 ☐ **MASS.**—Burlington Sales, (617) 272-7655 ☐ **MICH.**—Luebbe Sales, (313) 357-0335 ☐ **MINN.**—Siedare Assocs., (612) 545-5663 ☐ **NEW MEX.**— Cleveland Enterprises, (505) 345-2481 ☐ **N.Y.**—Electro Rep, (516) 938-0540 ☐ **OHIO**—Luebbe Sales—Cinc: (513) 871-4211; Cleveland: (216) 333-0425; Dayton (513) 294-0426 ☐ **PENNA.**— Delmont: Luebbe Sales, (412) 468-4019; West Chester: January Marketing & Sales, (215) 793-2265 ☐ **TEXAS**—Oeler-Menelaides, (214) 234-6334 ☐ **CANADA**—Zaslow Sales, (416) 727-1211 ☐ **EUROPE**—Trio Laboratories Ltd., U.K., Hindhead 6060, Telex 858225 ☐ **JAPAN** —Rikei Corp.

125-IN./S TAPE DRIVE

Using capacitive tape sensors in a free-air-flow system that is self-purging of oxide and foreign particles to protect them from damage by external exposure, the 2760 incorporates a vacuum capstan, motors, electronic cards, vacuum tape cleaner, and other field-proven assemblies. Accessibility to all electronics and mechanical assemblies is from the front by simply swinging the tape deck on hinges furnished for rack mounting. Available in packing densities of 200-, 556-, and 800-bit/in. NRZI, or 1600-bit/in. phase-encoded formats, the 24.5" unit features three read threshold levels, skew window control for writing optimum tapes, no mechanical adjustments, two speed-selectable operations, wear-free tape path, ceramic guides in the head area, and IBM head and guide spacing. **Data Disc Inc,** 686 W Maude Ave, Sunnyvale, CA 94086.



Circle 203 on Inquiry Card

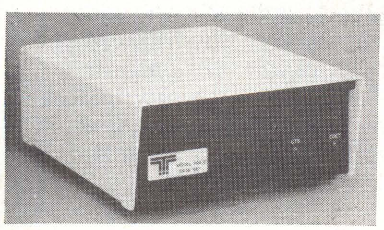
LED DISCRETE LINE

Line of 12 high intensity lamps in yellow, orange, green, and red offers choice of wide-angle or forward-view light patterns. Yellow, orange, and red models use composite chips of GaAsP on a GaP substrate; green are GaP on GaP. A clear lens, extra-high intensity unit provides a spot light pattern for backlighting; two diffused-lens units have either a 24-deg narrow-angle pattern for directional indicator applications or a 65-deg wide-angle pattern for general panel applications. Clear lens units have typ intensities of 45 (yellow, MC4-580B), 40 (orange/amber, -480B; and red, -280B), and 15 mcd (green, -380B); diffused-lens, narrow-angle units are rated 10 (yellow), 8 (orange/amber and red), and 3 mcd (green). Wide-angle diffused units provide 6, 4, and 1.5 mcd, respectively, for yellow, orange/amber and red, and green lenses. **Chicago Miniature/Drake,** 4433 N Ravenswood Ave, Chicago, IL 60640.

Circle 204 on Inquiry Card

MEDIUM SPEED MODEM

A basic asynchronous, frequency shift keying modem for direct replacement of 202D types, CW 904 units provide dial-up service at up to 1200 bits/s (half-duplex) with data access arrangement CDT and CBT and can be used in private-line application at up to 1800 bits/s, either 2-wire half-duplex, or 4-wire full-duplex. They also directly replace IBM lease line adapter and limited distance adapters (up to 600 bits/s). The series has a carrier detector circuit that is independent from the data receive circuit, switch-selectable transmit level adjustments, switch-selectable features, and receiver input sensitivity independent from carrier detector. It is available as plug-in PC card or standalone (single unit), or as a shelf/cabinet multiple mounting unit with redundant power supply. **Terminal Communications, Inc, sub of United Aircraft Corp,** 3301 Terminal Dr, Raleigh, NC 27611.



Circle 205 on Inquiry Card

MULTIPLEXED COMMUNICATIONS SYSTEM

Providing simultaneous remote control and status monitoring for as many as 7140 separate pieces of electrical equipment, System 1A remote units use IC multiplexer design and gates for detecting 28 input closures (floating), and relays for implementing 28 output closures (120 V, 10 A). Up to 255 remote units may be dispersed in a network, each connecting to another via a single pair of phone wires up to 1 mile long, and all operating under control of a master unit, which may contain its own control keys and display or may be interfaced directly to a computer at a TTL level. **Futronix, Inc,** 940 E Arques Ave, Sunnyvale, CA 94086.

Circle 206 on Inquiry Card

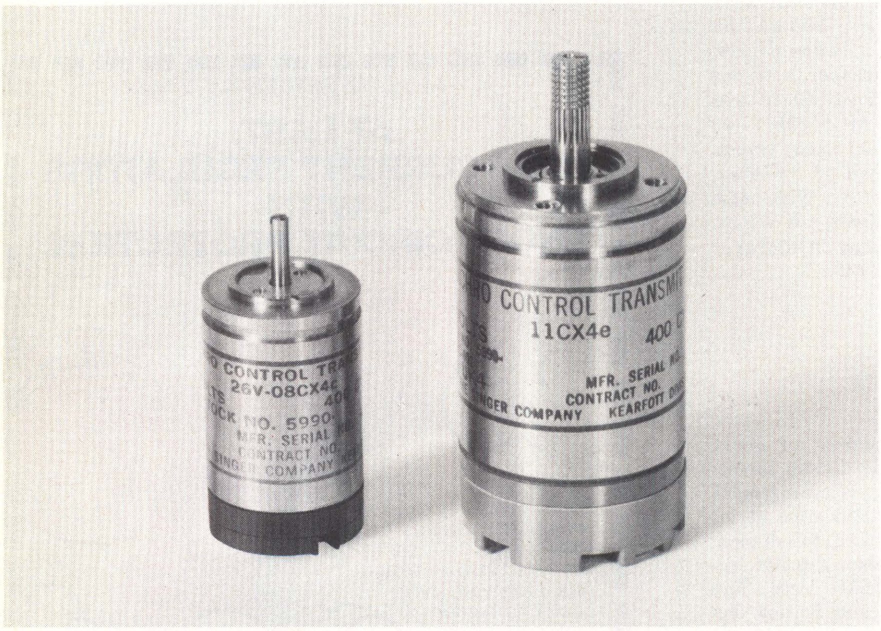
SCHOTTKY TTL BUS TRANSCEIVERS

Am26S10 and -11 offer 15-ns driver and receiver propagation delays and feature open-collector drivers with 100-mA current sinking capability, which permits ideal termination of 50-Ω transmission lines. Transceivers are designed for single-ended, 2-way communications in bus-oriented digital processing systems. The circuit pair operates from a single 5-V supply; each has a power-down feature limiting bus loading to 100 μA. Bus drivers have a common enable for all four units; receivers have narrow threshold regions specified at + or − 250 mV for noise immunity. **Advanced Micro Devices, Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.

Circle 207 on Inquiry Card

We made them first. To last.

Available now from Singer: Size 8 and 11 Bu/weps synchros designed to meet the latest requirements of MIL-S-20708C specifications.



Kearfott, the first to design Bu/weps size 5, 8 and 11 synchros, has over the years constantly made them better. These units are used in fire control systems, radar, navigation, missile functions and other applications requiring a high level of precision, endurance and reliability.

These Kearfott synchros operate over the entire temperature range of—55°C to + 125°C. They are DOD qualified and listed in the QPL.

(They can also meet reasonable cost requirements in computers, electronics and other types of business equipment.)

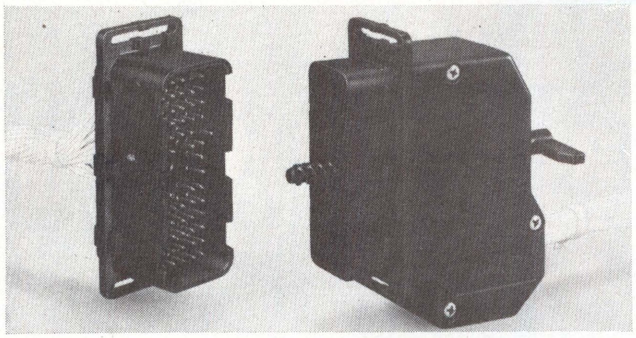
You can get these synchros in the following Bu/weps types:

Size 8	Size 11
26V 08CX4c	26V 11CX4c
26V 08CDX4c	11CX4e
26V 08CT4c	26V 11TX4c
	26V 11CDX4c
	11CDX4b
	26V 11CT4d
	11CT4E

We'll be happy to send you drawings and technical details on request. Also for Kearfott Size 5 Bu/weps CX, CDX and CT units, and Size 11 and 15 resolvers. Units with the same characteristics but different Bu/weps shaft variations are also available. Write for information to the Singer Company, Kearfott Division, 1150 McBride Avenue, Little Falls, N.J. 07424.

SINGER
AEROSPACE & MARINE SYSTEMS

FULLY METRIC CONNECTOR

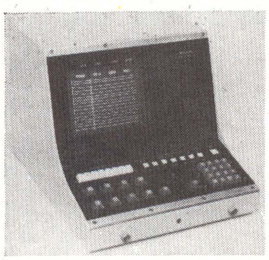


Claimed to be the first American connector manufactured to true metric dimensions, the rectangular rack and panel connector meets general requirements of national and international testing and approval groups such as UL, CSA, CEE, and VDE. All dimensions associated with its interface are in integral millimeters or 0.1-mm increments; contacts are located on 5-mm centers and accept wires from 0.08 through 2 mm² (or AWG #28 through #14). Stamped and formed brass contacts are available with either tin or selective gold plating; extra long first-make, last-break ground pins are gold-plated. The unit is molded entirely of UL rate 94 V-0 thermoplastic, except for strain-relief screws and electrical contacts. **AMP Inc,** Harrisburg, PA 17105.
Circle 208 on Inquiry Card

PRECISION TIMER

Utilizing the combined linear and digital technology of CDI (collector diffusion isolation) bipolar process, the TTL-compatible ZN1034E offers a repetitive timing accuracy of 0.01% with a temp stability of 0.01%/°C. Timing periods in excess of 300 hr can be accommodated with only four external components in most applications. Three on-chip regulators accept virtually any supply voltage with a total internal current draw of 5 mA; 25-mA complementary output drive capability is provided. The device is available in a 14-pin plastic DIP. **Ferranti Electric, Inc,** East Bethpage Rd, Plainview, NY 11803.
Circle 209 on Inquiry Card

DIGITAL WORD GENERATOR/RECEIVER



Featuring four separate memories and a CRT, which displays data "on command" for program generation and editing or functions as a digital scope, the 777 Digitester generates or receives up to 1024 serial bits or 16 parallel words of 64 bits each to assist in design/testing of digital logic products. In addition, the self-contained instrument incorporates a 10-key numeric pad and pushbuttons for selecting synchronization from an external source or from an internal precision crystal-controlled or infinitely variable clock. The four memories are used for (1) formulation and editing of the data pattern using integral keyboard and CRT, (2) storage of edited program for output to the DUT, (3) storage of response from the DUT and display of results on the CRT, and (4) nonvolatile storage of previously programmed patterns. **Moxon Inc,** 2222 Michelson Dr, Irvine, CA 92702.
Circle 210 on Inquiry Card

p-MOS, 1K RAM

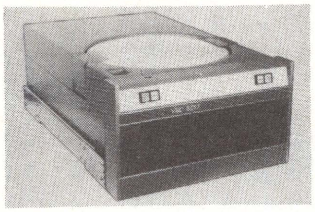
The 1103-F, a high speed version of the 1103 p-MOS 1024-bit dynamic RAM, features an access time of 120 ns. Measuring 103 mils/side, the circuit is totally free of pattern sensitivity and is supplied in a high reliability, 18-pin ceramic DIP. It is fully compatible with other 1103 designs. Aimed primarily at the mainframe computer market with other applications in add-on memory systems, the unit meets cost objectives because of its small die size and the high yield that result from Isoplanar process technology and special circuit design. The device is also supplied in std speed ranges, including 330-, 220-, 180-, 150-, and 120-ns specs. **Fairchild Camera & Instrument Corp, Integrated Circuits Group,** 464 Ellis St, Mountain View, CA 94042.
Circle 211 on Inquiry Card

VISUAL MEMORY SYSTEM

The D-8000 reproduces b/w visual material, through a video-to-digital conversion technique, for presentation on a std video monitor or TV set in black-on-white or white-on-black format, enabling video graphics to be transmitted over std telephone lines in digital form, or to be stored for later presentation. Input from any std b/w TV camera is converted to digital information for storage. System digital memory capacity of 8K 10-bit data words permits up to 7680 video transitions to be stored. **3M Co, Mincom Div, Datavision Video Products,** 15932 Shady Grove Rd, Gaithersburg, MD 20760.
Circle 212 on Inquiry Card

CARTRIDGE DISC DRIVE

Formatted storage capacity for 400 megabits on the model 5017 results from a patented method of recording 500 tracks/in. on the disc. The fast access unit servos on its own data track, permitting it to find and lock on the right track independent of temp variations. Avg head-positioning time is 35 ms. Its 50 to 100°F temp range makes it practical for use in non-air-conditioned environments. The unit measures 19" W, 28¼" D, and 10¾" H. **Vermont Research Corp,** Precision Pk, North Springfield, VT 05150.



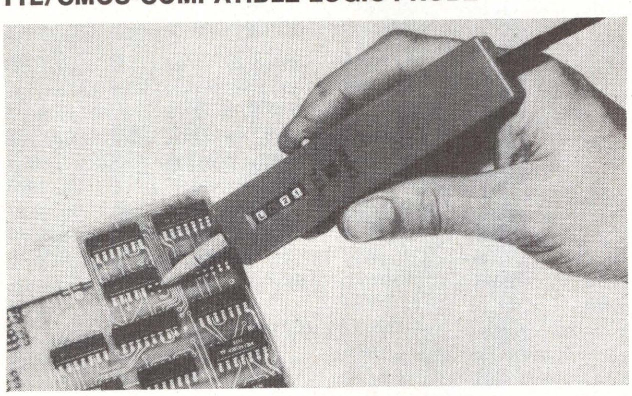
Circle 213 on Inquiry Card

DUAL OP AMP

Designated HA-2650, the internally compensated monolithic device features optimum tradeoff between ac and dc characteristics. Ac characteristics boast a slew rate of 5 V/μs and a bandwidth of 8 MHz; at $\pm$2 V, slew rate remains under 4 V/μs. Dc performance features a bias current of 35 nA with 75-mW power consumption and avg offset voltage drift of 8 μV/°C. Pinouts are identical to the Motorola 1558, permitting the device to be used as a pin-for-pin replacement where upgraded performance is desired. Both commercial and military temp range devices are available in either TO-116 DIP or TO-99 metal can packages. **Harris Semiconductor, a div of Harris Corp,** PO Box 883, Melbourne, FL 32901.

Circle 214 on Inquiry Card

TTL/CMOS-COMPATIBLE LOGIC PROBE



A versatile hand-held test instrument for TTL and CMOS ICs, the LP-7000 incorporates an accurate high/low discriminator and fast pulse counter. TTL and CMOS logic threshold levels and faulty or open-circuit conditions are precisely indicated by high and low displays. When switched to CMOS mode, 30/70% threshold levels are automatically adjusted from 4.5 to 18 V by the supply voltage applied to the probe. By pressing a push-button switch, pulses as narrow as 50 ns are detected without triggering or consideration of the pulse repetition frequency. Counting frequency is >10 MHz. Input impedance of 2 MΩ applies min load to circuits under test. Input overvoltages up to 250 V may be applied continuously without damaging the instrument. **Aikenwood Co, Zi-Tech Div,** 223 Forest Ave, Palo Alto, CA 94301.

Circle 215 on Inquiry Card

5" CRT DISPLAY

The "Tattletale," a data line monitor, provides portability with a companion CRT display; model 445 puts 640 char on the 5" screen; 485 displays up to 1280 char. Blinking control char allow easy recognition and fault isolation. Either model can sit transparently on any data communications line and monitor and display all data at rates up to 9600 baud, in both directions, including the normally invisible control characters. Framing and parity errors and line status characters are displayed on LEDs. Combination of status lights and alphanumeric char display reduces troubleshooting and fault-isolation time. Multiple CRT displays can be driven by one data line monitor. **Digi-Log Systems, Inc,** Babylon Rd, Horsham, PA 19044.

Circle 216 on Inquiry Card

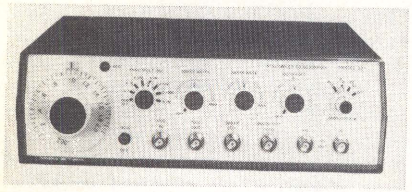
OPEN-FRAME POWER MODULES

Improved EPS series modules, available for 47- to 440-Hz operation, include a second frequency compensating network to provide better transient response and stability under varying load changes. With voltage ratings of 5 to 24 V and current ratings from 1 to 3 A, the supplies feature automatic-overload and short-circuit protection, and voltage and current limit trim control. Std options include overvoltage protector and regulation of 0.1% and ripple of 1 mV. **Deltron, Inc,** Wissahickon Ave, North Wales, PA 19454.

Circle 217 on Inquiry Card

PRODUCTS

FUNCTION GENERATORS



Xtal Control Accuracy makes the output of models 181 and 183 accurate to >0.01% of setting at XCG frequencies; there are 120 frequencies for 181, 150 for 183. 181 offers sine, square, triangle, and dc outputs with frequencies from 0.1 Hz to 2 MHz and internal 1000:1 sweep. High and low outputs are 30 dB variable for waveforms; up to 20 V pk-pk for high, to 1 V pk-pk for low. 183 provides 0.0001 Hz to 5 MHz plus triggered and gated modes, as well as variable symmetry control for pulse and ramp waveforms. **Wavetek,** PO Box 651, San Diego, CA 92112.

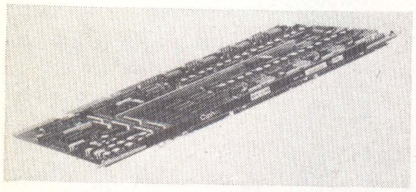
Circle 218 on Inquiry Card

MICROPROCESSOR-COMPATIBLE CORE MEMORY

LM-416-N, compatible with National's IMP-16P, IMP-16C, and PACE microprocessors, is nonvolatile with a data-safe feature that prevents data loss due to power swings or uncontrolled shutdown. Capacity is either 4K or 8K words by 16-bit word length; byte control is available. Cycle time is 1.4 μs; access time, 550 ns. Temp compensation is self-contained, and unit size is 11 x 8.5 x 1". **Litton Memory Products, div of Litton Industries,** Canoga Park, CA 91303.

Circle 219 on Inquiry Card

ADD-ON CORE MEMORY



MEM-11-16K, constructed with 16K of memory on a single board, is fully compatible with any DEC PDP-11 family program. Only two module positions are needed. The memory is plugged in directly for quick installation, and runs all DEC diagnostics without patching. Other features are TTL compatibility, 900-ns cycle time, 350-ns access time, full 8K sense inhibit windings, ±5-V margins, and multimode operation. **Cipher Data Products,** 7510 Clairemont Mesa Blvd, San Diego, CA 92111.

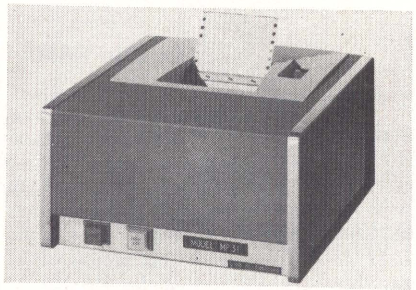
Circle 220 on Inquiry Card

TRIPLE-OUTPUT BENCHTOP POWER SUPPLY

Model KT7-20 provides 0- to 7-V output for digital logic and balanced plus/minus output voltages for op amps or other analog circuits. Output, rated at 2 A, has a constant-voltage/-current crossover characteristic with continuously adjustable current control. Adjustable overvoltage protection is included. Line/load regulation are ±0.01% each; ripple, 0.25 mV. Balanced outputs are adjustable from ±10 to ±20 V and are rated at 500 mA/output. Line/load regulation are ±0.05% each; ripple, 1 mV. Two meters may be switched to monitor all output voltages and currents. **Acopian Corp,** Easton, PA 18042.

Circle 221 on Inquiry Card

DOT MATRIX PRINTERS

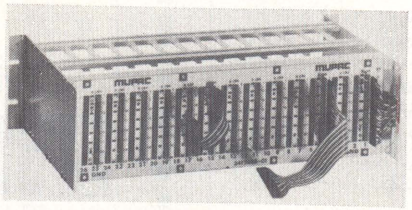


Model MP-30 series, suitable for OEM systems applications or as standalone printers, are available with three basic input configurations: RS-232-C, 20-mA current loop, and bit parallel/word serial. A total of 64 alphanumeric char and symbols are printed in 5 x 7 format or in expanded 10 x 7 format. Printers are capable of storing two lines of 32 col for the friction-feed model, 26 col for the sprocket-feed, and operate at 110 char/s. Size is 12.5 x 10 x 5.5". **TL Industries, Inc,** 6061 Telegraph Rd, Toledo, OH 43612.

Circle 222 on Inquiry Card

BOX CONNECTOR, CABLE ASSEMBLIES

Family of box-style connector and flat-ribbon cable assemblies is designed for mating with 0.025" sq pins on 0.1" centers. Various lengths and numbers of contact positions are available. Assemblies may be stacked end-to-end and/or side-by-side for 0.1" sq grid applications. Contacts are beryllium copper, and molded housings are glass-filled nylon. Wire is 26 AWG stranded and color coded for ease of troubleshooting. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.



Circle 223 on Inquiry Card

132-COLUMN PRINTER

Series 200/XL is capable of printing up to 132 char on std 8½" wide paper. Utilizing 16.5 char/in., the printer forms characters in a 7 x 9 dot matrix, and offers a 96-char font with u/l case. Unit is available as a KSR or R/O printer, with selectable speeds of 7.5, 10, 15, 30, 60, 120, or 240 char/s. SCOPEX plug-in module swapout program or maintenance by Sorbus, Inc are also offered. **Scope Data Inc,** 3728 Silver Star Rd, Orlando, FL 32808.

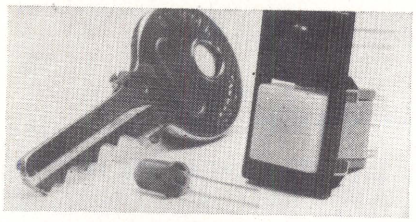
Circle 224 on Inquiry Card

CORE-RESIDENT OPERATING SYSTEM

SCORE (core resident executive system) is a software development tool designed for use in min configurations of model 32 computer systems. Featuring time-multiplexed CPU scheduling for multiple user tasks, it also includes I/O drivers for std peripheral devices and provides direct operator-level control for program assemblies and execution, in addition to load/dump and debugging capabilities. **Systems Engineering Laboratories, Inc,** 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313.

Circle 225 on Inquiry Card

SNAP-IN MOMENTARY PUSHBUTTON SWITCH BEZEL



A bezel designed to accommodate an LED indicator lamp has been added as an optional feature to 8100 series snap-in momentary pushbutton switches. The lamp can be snapped into the bezel either before or after the switch and bezel are installed in the panel. Bezel is available in nine colors. Switches accommodate lamp models of leading manufacturers. **C&K Components, Inc,** 103 Morse St, Watertown, MA 02172.

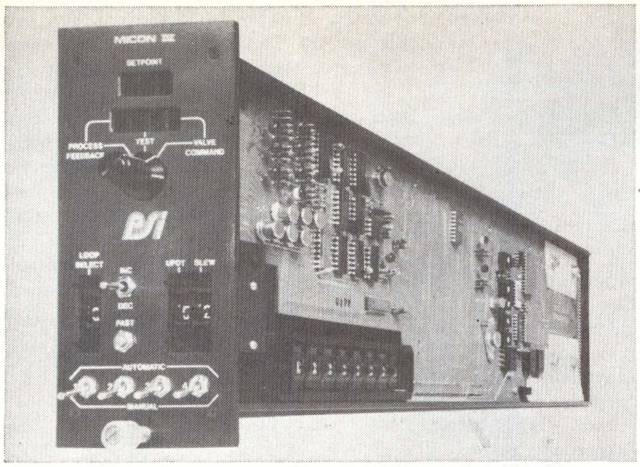
Circle 226 on Inquiry Card

SMALL LEDs

MICRO LED series is designed for applications where space is at a premium, including illumination of miniature dials, diagnostic lights, lamp arrays, and cockpit and battery status indicators. Featured are small size (0.02 x 0.018"); 1000 ft-L brightness at 10-mA; low cost; ruggedness (withstands 1-lb pull on wire); ±90-deg viewing angle; red, green, or yellow colors; axial leads; and variety of lens styles. **Digital Components Corp,** 1111 E Elizabeth Ave, Linden, NJ 07030.

Circle 227 on Inquiry Card

DIGITAL MICROCOMPUTER CONTROLLER



Preprogrammed to serve process control needs, the 4-loop Micon IV has a dedicated microcomputer as its front-end; its back is a controller. The unit is all digital with internal DACs and solid-state LSI-based design; it operates up to four modulating analog devices with 2-mode control plus up to 12 on/off logic devices. Accepting up to 16 process transmitter signals and up to 24 digital on/off signals, it outputs analog or digital signals that can be computed functions of any combination of analog or digital input signals. Memory is 2.5K of mixed ROM and p/ROM. Functions include multiply, divide, add, subtract, complement, extract square roots, and convert binary-to-BCD, analog-to-digital, and digital-to-analog. The controller measures 5⅞ x 2¾ x 20". **Process Systems, Inc**, 301 E Alton Ave, Santa Ana, CA 92797.
Circle 228 on Inquiry Card

REGULATED DC-DC POWER SOURCES

Designed to operate with 5-Vdc input, V5R V-PAC™ sources provide users with regulated positive or negative 3-, 5-, 9-, 12-, or 15-V output, depending upon device type, and afford isolation, built-in short circuit, and thermal overload protection. The units permit the use of a single power supply with MOS, linear, RAM, ROM, UART, and other devices having special voltage requirements. Output voltage tolerance is ±5%; output ripple is 100 mV pk-pk max; line regulation is ±0.2%; and load regulation is 150 mV, no load to full load. The devices mount on the same PC card as those being operated, and occupy less than 0.3 in.^{3} Pins are on std 0.1" centers, and fit regular 24-pin DIP sockets or may be soldered to cards using routine IC assembly techniques. **Reliability, Inc**, 5325 Glenmont, Houston, TX 77036.
Circle 229 on Inquiry Card

MINIATURE DIGITAL CONTROL

Using a single custom MOS LSI circuit and ¼"-high LED display, the series 7992 minicontroller predetermining counter assures long count and reset life by using no moving parts. The 4-figure, 2-level counter, housed in a 2 x 2 x 4½" case, is designed especially for instrument and industrial applications where existing electromechanical preset counters are inadequate to meet fast count rate, frequent reset, and long life requirements. The std unit operates on 24 Vdc at 5 W at speeds to 4200 counts/min. (An optional remote power supply module allows 115-Vac operation.) With a built-in bounce filter, the unit interfaces with existing switch-closure circuits and accepts TTL, DTL, and other logic-level pulses. **Veeder-Root,** 70 Sargeant St, Hartford, CT 06102.
Circle 230 on Inquiry Card

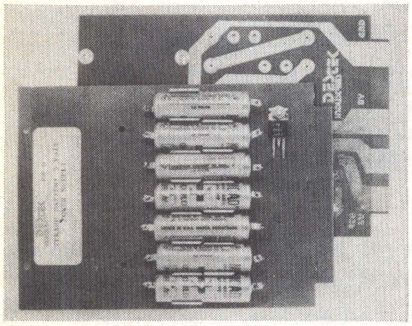
PRODUCTS

SUBMINIATURE TOGGLE SWITCH

Giga-Switch, designed for low energy applications at frequencies from dc to approx 1 GHz, features low internal resistance, low inductance, and low capacitance. Teflon fluorocarbon resins are used for the insulating components. Switch contacts are corrosion-resistant gold alloy, made to last through the unit's 100,000-cycle service life. Switch is used in attenuator pad switching with flat attenuation of up to 30-dB steps at 1 GHz and an insertion loss of <0.1 dB. It is also suitable for coax connector switching. **Instru-Mech, Inc,** 1275 Bloomfield Ave, Fairfield, NJ 07006.

Circle 231 on Inquiry Card

BATTERY POWER SUPPLY



5 ±0.25-V regulated, 8-V unregulated Tekard power supply, on a plug-in 4.5" wide PC card in both 4.5 and 6.5" lengths, has a capacity of ½ A-hr. It includes a charger plus a jack and insulating washers. Load regulation at 25°C is 15 mA typ, quiescent current is 4.2 mA typ, and op temp range is 0 to 60°C. Card is designed to fit a 0.156" spaced, 22-contact connector, or any other with finger spacing that accepts the 3.59" wide edgeboard plug. **Destek™ Industries,** PO Box 24163, Los Angeles, CA 90024.

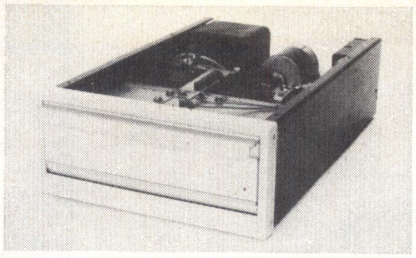
Circle 232 on Inquiry Card

TEMPERATURE SENSOR

TS3-57S Moxie thermal avalanche switch is a thin-film semiconductor that can be interfaced directly with triacs or other common power control devices. Operating as a combination sensor/discriminator/amp, it generates pulses directly proportional to temperature. It requires only a series resistor to operate from 110/220-Vac mains and eliminates complex ICs. Pulse output responds continuously to temp with nom sensitivity of 2 V/°C. Switching speed is 50 ns. **Multi-State Devices Ltd,** 1330 Trans-Canada Hwy, Dorval, Quebec H9P 1H8, Canada.

Circle 233 on Inquiry Card

FLEXIBLE DISC DRIVE



FD500, offering an ac motor, a locking door that cannot be opened when the drive is reading or writing data, and a ferrite head that is fully retractable from media under program control, is also available as a mechanics-only unit. The machine is fully compatible with data written on IBM 3540 or 3740 systems, and data recorded can be read by either system. Using an IBM diskette or equivalent medium, it stores up to 3.2 million bits of unformatted data, and transfers data at 250 kilobits/s. **Pertec Corp, Peripheral Equipment Div,** 9600 Irondale Ave, Chatsworth, CA 91311.

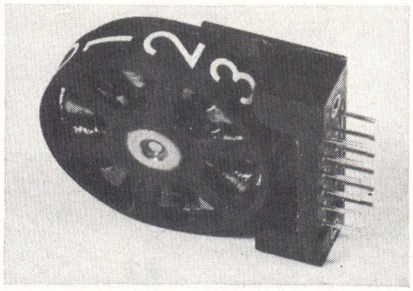
Circle 234 on Inquiry Card

MINIATURE RELAYS

Model PS 101 for 120-V and PS 201 for 240-V operation switch a 1-A inductive load, with a 1-cycle surge current rating to 20 A. Isolation, input-to-input, is 1500 V rms. PC board mounting eliminates discrete wiring of components. A single silicon-controlled rectifier is used; and optical elements are used for photoisolation, replacing reed or mechanical contact and hence eliminating moving parts. This, combined with zero-voltage switching, eliminates electrical noise and circuit transients. **International Rectifier Corp, Crydom Div,** 1521 Grand Ave, El Segundo, CA 90245.

Circle 235 on Inquiry Card

DIGITAL INDICATOR



Model H5220 is a TTL-compatible, magnetic-wheel, 12-V unit designed to be driven by a 5445/7445 BCD-to-decimal driver. It has an op temp range of −55 to 95°C, meets MIL-STD-202 environmental requirements, may be mounted on 0.295" centers, and is available with pins for direct PC board mounting or with lead wires for harnessing. **Novatronics of Canada Ltd,** PO Box 610, Stratford, Ontario, Canada.

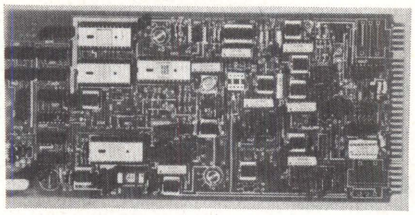
Circle 236 on Inquiry Card

KEYSWITCHES

Compact, low profile keyboards, for calculators, POS devices, and data entry equipment, may be designed with Lo-Pro 5 or wobble-free Lo-Pro 20 keyswitches. Both are available in a high-profile configuration as well. Lo-Pro 20 and its high-profile equivalent have integral elastomeric cushions to increase error-free operations to 20 million. Std coding, such as ASCII, is available, while variations can be ordered. Engineering assistance for designing custom logic can also be provided. **Stackpole Components Co,** PO Box 14466, Raleigh, NC 22610.

Circle 237 on Inquiry Card

LOW COST DATA MODEM CARD

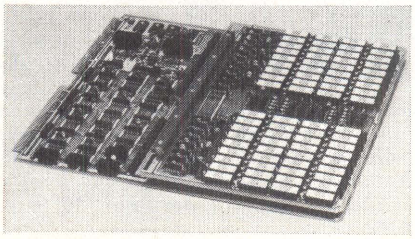


With TE-2400, designed for type 3002 unconditioned lines, all modulation, demodulation, and timing recovery functions are performed in four MOS/LSI chips. Predicted MTBF exceeds 40,000 hr. A strap option permits the modem equalizer to be inserted into transmitter or receiver circuits. Modulation is compatible with CCITT V.26; digital interface is in accordance with RS-232-C and CCITT V.24. Modem has fast synchronization, and request-to-send/clear-to-send time can be set to 1, 10, 20, or 150 ms. **Rockwell International, Collins Radio Group,** Dallas, TX 75207.

Circle 238 on Inquiry Card

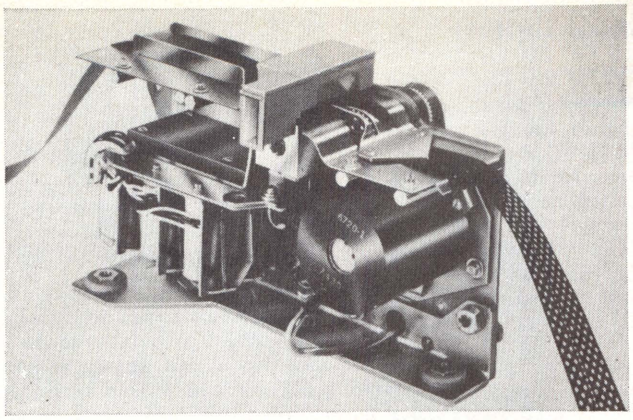
HIGH SPEED, STATIC n-MOS MEMORY CARD

TM-200, which uses a static n-MOS RAM, has a max access time of 130 ns and a min cycle time of 250 ns. Compact size and full TTL compatibility make it suitable for any high speed memory application. It consists of a 4K x 18-bit basic storage card including timing/control and/or a stackable memory card without timing/control. With the stacked assembly, a single card slot is capable of storing 16 kilobytes, organized as either 8K x 18 or 16K x 9. **Advanced Memory Systems, Inc,** 1276 Hammerwood Ave, Sunnyvale, CA 94086.



Circle 239 on Inquiry Card

PAPER-TAPE PUNCH

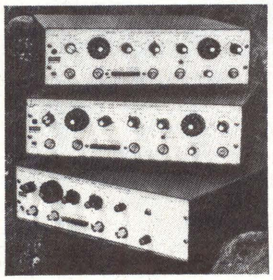


The Moduperf "75" offers field-replaceable modules which allow the operator to make adjustment-free replacements of die block and/or data selector in less than a minute, minimizing equipment downtime and simplifying service. Simple design provides reliability, long life, and compact size. By making the data selection directly on the punch pins and advancing the tape with a stepping motor, need for intermediate levers, links, clutches, ratchets, and pawls is eliminated as are problems normally associated with these complex mechanical elements. Built to precision standards from high-grade hardened tool steel, the die block will operate for a min of 120 million punch cycles or 1000 rolls of any type of tape. **Data Specialties, Inc,** 3455 Commercial Ave, Northbrook, IL 60062.
Circle 240 on Inquiry Card

16-BIT LSI POLYNOMIAL GENERATOR

The MC8506 addition to the MEGALOGIC™ family provides a means of error detection in serial data handling systems. The 160-gate LSI function divides the serial data stream by a std polynomial; the division remainder is transmitted at the end of the data stream as a cyclic redundancy check character. When the data stream is received, the same calculation is performed. If there are no transmission errors, an "all-0" indication is given in floppy-disc applications, a "pattern match" in SDLC applications. All data registers may be preset to logical 1; or the first two data registers to logical 0, and the balance to logical 1 in one clock cycle. The fully TTL-compatible device, with 380-mW power dissipation and 4-MHz typ data rate, is provided in a 16-pin DIL plastic or ceramic package. **Motorola Inc, Semiconductor Products Div,** PO Box 20294, Phoenix, AZ 85036.
Circle 241 on Inquiry Card

FUNCTION GENERATORS



Featuring 0.001-Hz to 5-MHz dynamic frequency range, 80-dB step attenuators, triggering, gating, and internal lin/log sweep generators, models 504, 506, and 507 offer VCF, sine, square, and triangle with variable symmetry for ramp and pulse operation; and 20-V pk-pk open circuit with 10 V pk-pk into 50-Ω output capability with up to ±10 V of variable dc offset. Trigger and gate modes provide single shot and burst operation when triggered from an external source or manual trigger. Start/stop points of triggered and gated waveforms can be varied through 360 deg. The 506 also has an internal ramp generator; the 507 adds logarithmic sweep mode to the linear sweep mode provided by the 506. **Dana Exact Electronics Inc,** 455 SE 2nd Ave, Hillsboro, OR 97123.
Circle 242 on Inquiry Card

PRODUCTS

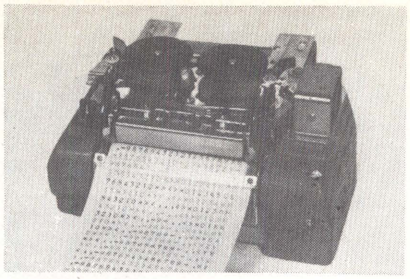
CMOS 4-BIT COMPARATOR

SCL 5485 4-bit magnitude comparator is an exact equivalent of the Motorola Mc 14585, in pin-out and electrical specs. It is available in ceramic flatpack, frit-sealed cerdip, or epoxy B DIL packaging, and in commercial and military grades. **Solid State Scientific Inc**, Montgomeryville, PA 18936.
Circle 243 on Inquiry Card

16K ROM

With 600-ns max access time, MK 28000 is a 16,384-bit MOS ROM which is pin-for-pin compatible with the EA 4900. No address lead time is required, so that both address and address-read can occur simultaneously. Power dissipation is 320 mW typ in active mode, 110 mW typ in standby. The mask-programmable p-channel device may be organized as either 2K x 8 or 4K x 4 and is suitable for use in minicomputers, POS terminals, CRT terminals, and mainframe applications. **Mostek Corp,** 13300 Branch View Lane, Dallas, TX 75234.
Circle 244 on Inquiry Card

COMPACT DIGITAL PRINTER

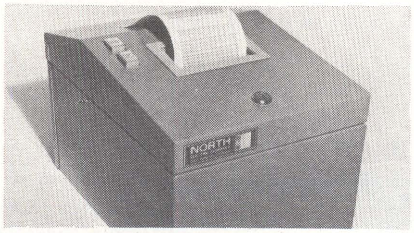


For applications in electronic calculators, cash registers, computers, and instrumentation, model EP-101 is an "on-the-fly" type, parallel-entry digital impact printer measuring 5½ x 6½ x 4" and weighing 5½ lb. Its cylindrical drum prints up to 21 col and up to 16 rows of char at 2.8 lines/s. Driven by a transistorized, brushless Hall-effect dc motor, the printer uses 3½" wide rolled paper which optionally may be pressure sensitive. **C. Itoh Electronics, Inc, Systems & Components Div,** 280 Park Ave, New York, NY 10017.
Circle 245 on Inquiry Card

RFI/EMI FILTERS

RNF type filters are UL recognized and meet CSA requirements. "L" series are for general usage to combat line-to-ground noise, "P" series are for suppression of line-to-line as well as line-to-ground interference, and "T" series are for low-impedance load applications. Capacitance line to ground is 0.01 mF nom; leakage current at 115 Vac/60 Hz is 0.5 mA max, at 250 Vac/60 Hz, 1 mA max; test voltage is 2100 Vdc, frequency range is 50 to 400 Hz, voltage is 115/250 Vac, and typ insertion loss meets MIL-STD-220. **RtroN Corp,** PO Box 743, Skokie, IL 60076.
Circle 246 on Inquiry Card

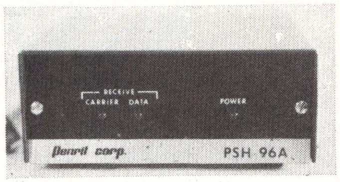
DOT MATRIX PRINTER



This 31-col, high speed dot matrix printer for numeric-only applications recognizes incoming data so that no strobe is required. Input may be decimal or BCD (char serial). Unit accommodates such interface requirements as TTL, CMOS, various voltages, and contact closure. An internal buffer collects data asynchronously and prints when commanded at 110 char/s. Also included are a printer-busy signal, paper wind-up motor, and packages which allow printed data to be kept under keylock but observed by the user. **North Electric Co, Electronetics Div,** PO Box 688, Galion, OH 44833.
Circle 247 on Inquiry Card

9600-BIT/S SHORT-HAUL MODEM

The asynchronous PSH 96A offers low cost, reliable data communications at distances up to 35 miles, depending on wire gauge and operating bit rate. Operation is full- or half-duplex over nonloaded cable pairs at any data rate from 0 to 19,200 bits/s. Features include visual diagnostics to ease installation and aid in system fault isolation, line equalization capability, and single-card construction. Diagnostics consist of LED status indicators on the front panel for power, carrier, and receive data. The modem can operate unattended continuously without need for periodic tests or checks. The standalone unit with built-in power supply measures 3 x 8 x 6", and weighs 2.5 lb. **Penril Corp,** 5520 Randolph Rd, Rockville, MD 20852.



Circle 248 on Inquiry Card

SOLID-STATE SENSOR

A solid-state proximity sensor that operates at speeds up to 100,000 times/s and weighs just ¼ oz, the magnetically operated Hall-effect 400 SR switch utilizes a 6- to 16-Vdc power supply, withstands temps ranging from −40 to 302°F (−40 to 150°C), offers solder/quick-connect terminals, and is packaged in a tough plastic enclosure. For linear or rotary motion detection in word processing and communications equipment, the device simplifies position or movement detection since there is no bounce in the no-touch sensor. Current sourcing or current sinking outputs are offered. The switch interfaces directly with nearly all electronic circuits, and requires no signal amplification in most applications. **Micro Switch, a div of Honeywell, Inc,** 11 W Spring St, Freeport, IL 61032.

Circle 249 on Inquiry Card

TERMINAL EXERCISER

A data generator and diagnostic tool for use in designing and testing computer peripheral equipment, the 578 aids field and design engineers by providing the capability of transmitting serial data and displaying received data and RS-232 interface control signals. A buffer permits equipment under test to be self-checking; up to 128 char of data may be received from equipment under test or manually loaded and then retransmitted to the input of the same equipment. Used as an exerciser, the device eliminates the need for a modem and computer when testing printers, teleprinters, plotters, CRT terminals, or other peripherals. Connection is made by interposing the unit between the terminal and its modem using RS-232 connectors. **Mission Data Products,** PO Box 2254, Westminster, CA 92683.

Circle 250 on Inquiry Card

12-BIT, 4-μS A-D CONVERTER

Model ADC-EH12B utilizes an MSI IC successive-approximation programmer/register, 12 fast-switching current sources, a low impedance R-2R resistor network, a precision voltage reference circuit, and a fast precision comparator to achieve fast conversion. Operating features include unipolar (0 to 10 V) or bipolar (±5 V) operation by external pin connection. Full scale tempco is 30 ppm/°C max; the converter is monotonic over its full op temp range of 0 to 70°C. The unit consumes 2 W of ±15-Vdc power. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.

Circle 251 on Inquiry Card

PRODUCTS

DATA SET

201C/LSI, a 2400-bit modem, is intended specifically for use by operating telephone companies in the U. S. and Canada. It is fully compatible with WECo data set 201C. Units are available for online evaluation. **International Communications Corp, a sub of Milgo Electronic Corp,** 8600 NW 41st St, Miami, FL 33166.
Circle 252 on Inquiry Card

OPTICAL INCREMENTAL ENCODERS

Rotosyn series, which includes complete internal squarewave electronics with TTL outputs—dual channel (A quad B), provides resolutions to 1000 cycles/turn, which can be increased via external logic to 4000 pulses/revolution. Encoders utilize advanced ICs and a single monolithic array of photosensors. Light source provides 90,000 hr continuous operation. ±5% noncritical voltage requirement and 175-mA drain permit use of a simple power supply. **Data Technology, Inc,** 4 Gill St, Woburn, MA 01801.
Circle 253 on Inquiry Card

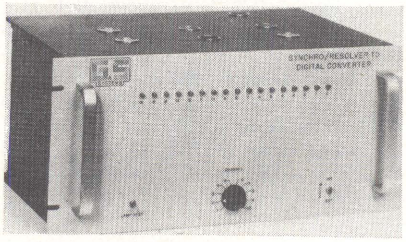
AUTOMATIC SCANNER

Model S260, a true random-access device with random busing capability, enables automatic point-to-point scanning of circuits under test, with low thermal contact resistance for precision measurements. Up to six mutually exclusive, individually addressable modules enable incremental or position-settable switching (from 2-pole/60 positions to 12-pole/10 positions) with BCD inputs for computer control of automatic testing. High-stability switches and low thermal pick-up will not degrade 1-ppm measurements. **Julie Research Laboratories, Inc,** 211 W 61st St, New York, NY 10023.
Circle 254 on Inquiry Card

MICROPROCESSOR SOCKET CARDS

3D3017 has four 40-pin, six 24-pin, five 18-pin, five 16-pin, and four 14-pin sockets. 24 ceramic and two tantalum capacitors are mounted on the card. Vcc and ground are prewired to the 14- and 16-pin sockets; power clips are furnished for custom power connections to the others. Power and ground planes provide for two additional voltages and mounting of four related bypass capacitors. 3D3018 is identical except for numbers of sockets and capacitors. **Electronic Engineering Company of California,** 1441 E Chestnut Ave, Santa Ana, CA 92701.
Circle 255 on Inquiry Card

SYNCHRO-TO-DIGITAL CONVERTER INTERFACE



A programmable interface for DEC PDP-8/E, /F, and /M systems, GS-SD-8 has a specially designed mode switch added to the converter that allows a wide range of synchro and resolver input voltages to be used. Line-to-line voltages range from 3 to 90 Vrms. Positions of programmable switches are determined by transducer type and input voltage range. Converter is used to digitize shaft angle information from synchros or resolvers that reach 1800 rpm. **G&S Systems, Inc,** 279 Cambridge St, Burlington, MA 01803.
Circle 256 on Inquiry Card

CIRCLE 60 ON INQUIRY CARD

VARIABLE SPEED DATA STORAGE DEVICE

With a max data transfer rate of >10 kilobits/s, the solid-state "Great Imposter" model 1000 module is plug-to-plug compatible with existing computer peripherals (paper-tape readers and punches, card readers), and can be used without hardware or software modifications. A selector switch allows the user to optionally use his original peripheral device. Std features include a tape search mode which enables the user to select data to be read from any section of the tape. Options provide read-only or read/write capability, read or read/write error correction, output data code conversion, and full RS-232-C interface capability. The basic read-only module comes complete with peripheral interconnection cable and a Redactron model 110 tape cassette. **Raymond Automation Labs, Inc,** 7 Bridge St, Glen Cove, NY 11542.

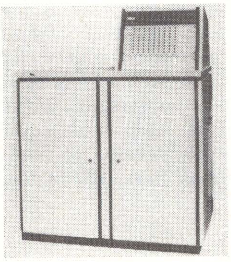
Circle 257 on Inquiry Card

DISPLAY CONNECTOR

Compatible with both gas discharge and liquid crystal displays, the ES series permits designers to vary connector card slot length, width, and contact placement without special tooling charges. Available with both 0.1" (ES1) and 0.05" (ES5) contact spacing, the connector is a single-side, single-readout, edgeboard style. A wide range of substrate lengths from 1 to 6" can be specified in 0.05" increments. The series can be provided to accommodate substrate thicknesses of 3/64, 1/16, and 1/8" nom. Dual-deflection contact design provides optimum individual contact pressure with min insertion force. Any number of contacts from 10 through 60 can be used on the ES1, 20 through 120 contacts are available on the ES5. **Dale Electronics, Inc,** E Highway 50, Yankton, SD 57078.

Circle 258 on Inquiry Card

COMPUTER SWITCH SYSTEM



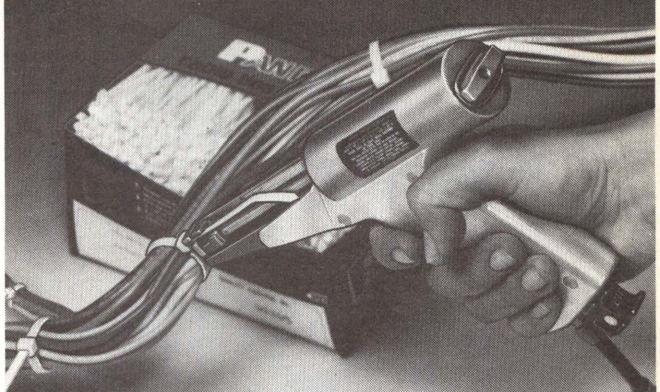
Designated 3915/3916, the IBM-compatible switch system provides increased functions and capacity over the currently available IBM 2914. The Mark II model provides up to 64 switch positions and offers 4 x 12, 8 x 8, and 4 x 16 configurations, as well as local or remote control. Local switch control and display are provided on the console of the 3915; the 3916 offers local display on the console with remote control and display at the CPU console. Features include capacity for a max number of machine configurations; reliability to assure no inadvertent configuration alterations due to power fluctuations; security to insure that configurations are not altered accidentally; expanded switching capacity to increase efficiency; and modular system architecture to permit field upgrading. **T-Bar Inc,** 141 Danbury Rd, Wilton, CT 06897.

Circle 259 on Inquiry Card

SHORTS DETECTION SYSTEM

For PC boards with 160 or fewer points, the L427 detects and identifies all common and internal shorts in semiconductors and passive components. The only programming necessary is assignment of stripe numbers. Electrical contact to stripe or pad is made through a spring-loaded bed-of-nails fixture. Continuity checks are made point to every other point at 2000/s. Measurements showing less than 10 Ω are considered shorts, and are printed out in a list on the front-panel strip printer. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.

Circle 260 on Inquiry Card

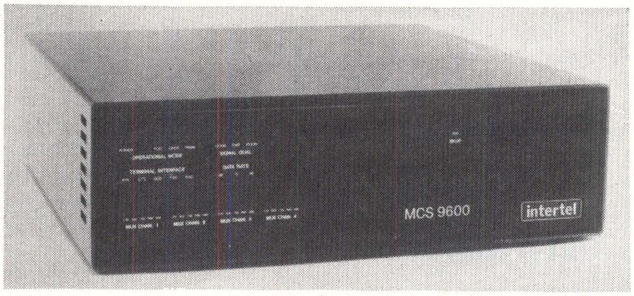


PRODUCTS

CIRCUIT CARD TESTER

A microprocessor-controlled, automatic test system, the firmware-driven, benchtop model 2160A is designed to test and diagnose complex logic arrays on a functional basis up to 200-IC complexity levels. Increased firmware capability is supplied as a prerecorded magnetic card which loads immediately into the tester, avoiding penalties of increased hardware costs. The control program provides conditional and unconditional branch instructions and subroutines. Firmware becomes operative at the press of a button, reducing time and effort necessary to generate complex automatic fault-isolation routines. An auto-programming feature captures all response data automatically from a known-good assembly. **Technology Marketing, Inc,** 3170 Red Hill Ave, Costa Mesa, CA 92626.
Circle 261 on Inquiry Card

9600-BIT/S MODEM WITH MUX OPTION

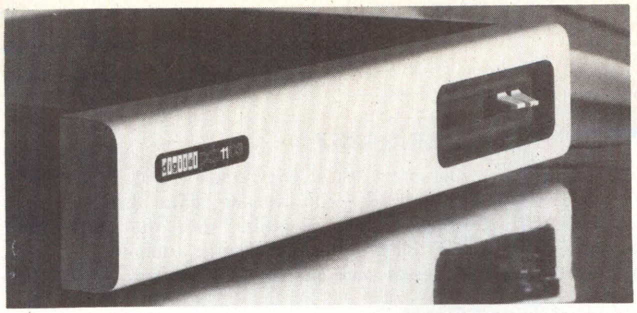


A time-division multiplexer (TDM) option for the company's 9600-bit/s modem consists of a single plug-in PC card that enables users to mix 2400-, 4800-, and 7200-bit/s data streams from terminals or co-located modems. Features include built-in self-test circuitry that automatically checks out the unit at the touch of a button, and status indictors that display important data terminal interface signals for each channel. Designed for use on the MC29600 modem, which operates on unconditioned type 3002 transmission lines and on the DDD network, the MUX option provides individual carrier control on each multiplexer channel for polled networks, and requires no software or hardware modification. **Intertel, Inc,** 6 Vine Brook Park, Burlington, MA 01803.
Circle 262 on Inquiry Card

COUNTER/CONTROLLER

Featuring solid-state reliability and accuracy combined with fingertip control, GARDIAN 4100 series have positive detent front-panel switches that are easily set and remain firmly in position. For applications requiring frequent changes in process control systems, the rugged 4.5 x 3 x 4" controller provides most popular control modes, programmable on rear-panel terminals. When the preset number is reached, an integral output relay performs a variety of functions. Manual reset, automatic reset for recycling, and adjustable output pulse and reset time delay are all std. The unit accurately totalizes passive contact closures and pulse voltage levels from 5 to 50 Vdc. Typ input pulse sources are switch closures, relays, and photoelectric and proximity sensors. **Durgin & Browne, Inc,** 80 Allen Rd, South Burlington, VT 05401.
Circle 263 on Inquiry Card

MICROCOMPUTER

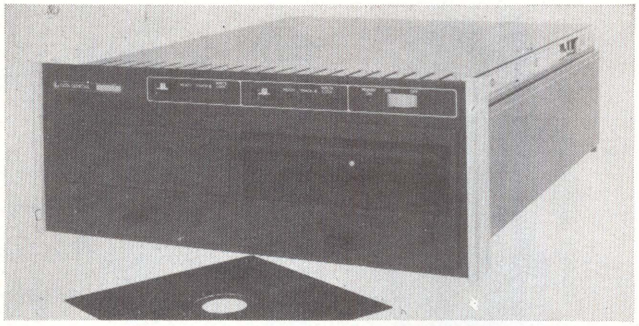


A boxed version of the LSI/11 microcomputer, the PDP-11/03 contains a 16-bit Si-gate n-channel, MOS LSI processor with memory, serial interface, power supply, rack-mountable enclosure, and operator's front panel. Available in 4K MOS RAM and 4K core configurations in both 115- and 230-Vac versions, the unit operates the -11/40's 400-plus instruction set at speeds comparable to the -11/05. The processor incorporates the Western Digital chip set, consisting of control, data, and two microcoded-ROM chips. An extended arithmetic option is contained in a fifth chip, which plugs into a socket on the microcomputer module. Other options include serial and parallel line-interface modules, and four expansion memory modules. **Digital Equipment Corp, Components Group,** One Iron Way, Marlboro, MA 01752.
Circle 264 on Inquiry Card

MULTIPLYING D-A CONVERTERS

The monoDAC-08 series of 8-bit monolithic converters features 85-ns settling time, complementary/differential high compliance current outputs, universal logic inputs, and low cost. Full scale and reference currents are matched to within 1 LSB, eliminating calibration in most applications. Direct interfacing with CMOS, TTL, DTL, ECL, and HTL is provided by an optional logic threshold adjustment, direct interface with n-MOS and p-MOS outputs of microprocessor RAMs is possible. **Precision Monolithics Inc,** 1500 Space Park Dr, Santa Clara, CA 95050.
Circle 265 on Inquiry Card

DISKETTE SUBSYSTEM

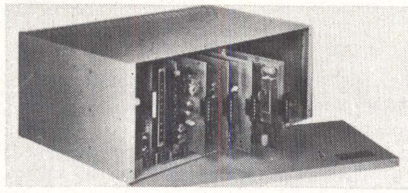


Providing mass-storage capability for Nova^{R} and Eclipse^{TM} computers, disc subsystem consists of a chassis containing power supply and drives, controller for up to four drives, and cable set. It is available in 2-drive (model 6030) and 1-drive (6031) versions; expansion to four drives provides a max 1.2-megabyte storage capacity. A thumbwheel switch lets users select any drive number as 0, 1, 2, or 3. The subsystem uses the computer's DMA channel for high speed data transfer. Each diskette has formatted data storage capacity of 512 bytes/sector, or 4096 bytes/track. Total surface capacity for a single diskette is 315,392 bytes. Features include data channel operation; sector transfer rate of 31 kilobytes/s; 260-ms avg access time; and 83-ms avg latency. **Data General Corp,** Southboro, MA 01772.
Circle 266 on Inquiry Card

PRODUCTS

AUTOMATIC CALLING UNIT

For mainframe computers that communicate via the public switched telephone network with remote data terminals, the series 907801 provides automatic dialing over the public telephone network under the direct control of the computer terminal, allows up to 15 addresses plus control functions to be stored in calling unit rather than in computer software, and permits address changes to be made by wire strapping. The units operate over std telephone lines, using positive dial-tone detection and loop signaling, and are compatible with all popular modems and mainframe computers. Rotary dial pulsing and Touch-Tone™ signaling are std. **Warren G-V Communications, div of Sola Basic Industries,** 101 Okner Pkwy, Livingston, NJ 07039.



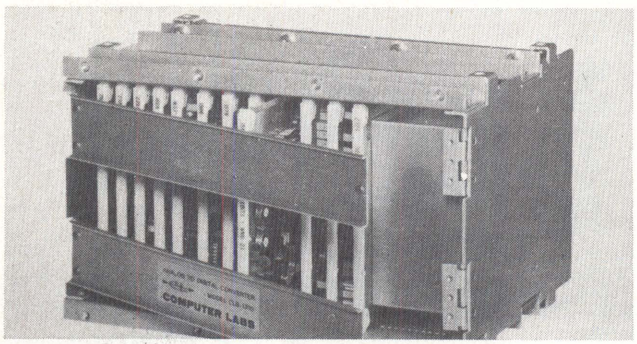
Circle 267 on Inquiry Card

COMPUTER TERMINAL

The 3010 communications terminal prints at 30 char/s, maintaining print quality and quiet operation even at sustained high printing speeds, and has special capabilities for drawing charts and graphs. Used with computer-aided text-processing systems, the microprocessor-driven terminal will automatically create, edit, and print documents according to instructions stored in the computer. It may be programmed to print both forward and backward, eliminating the need for carriage return. The typewriter-paired keyboard provides direct compatibility for APL applications. Offline diagnostics built into the unit can be initiated by the operator to verify correct machine operation or to isolate faults in keyboard, logic, or printer. **Xerox Corp,** 701 S Aviation Blvd, El Segundo, CA 90245.

Circle 268 on Inquiry Card

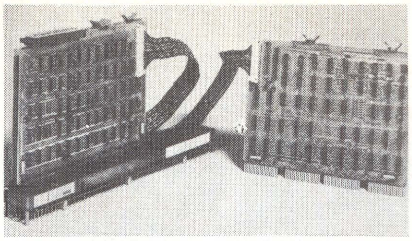
A-D CONVERTERS



CLB 9000 "Bare Bones" converters, with 11-, 12-, or 13-bit resolutions at word rates from dc through 10 MHz, operate as system ADCs utilizing dc power sources generally available in systems requiring A-D conversion. Internal track and hold circuits have an aperture of 10 ps to assure accuracy on fast-changing analog inputs; the units operate on system power, ±15, 5, and −5.2 V. Dc accuracy is specified as 0.025% ±½ LSB for 10-MHz models, and 0.025, 0.012, and 0.01% ±½ LSB for 11-, 12-, and 13-bit, 5-MHz models, respectively. Conversion times are 500 ±30 ns for 10-MHz units, and 600 ±30 ns for 5-MHz units. Analog input range is −2.048 to 2.048 V (bipolar signals). **Computer Labs Inc,** 1109 S Chapman St, Greensboro, NC 27403.

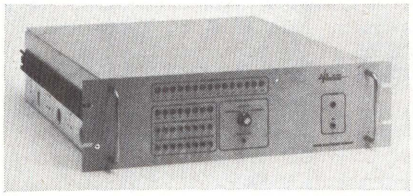
Circle 269 on Inquiry Card

INTERPROCESSOR COMMUNICATIONS INTERFACE



Designed for high speed data transfers between computers in multiprocessor or distributed systems applications, IPT-8 and -11 provide parallel memory-to-memory transfers at up to 500 kilobytes/s between two DEC PDP-8/E or -11 computers or between one -8/E and one -11, at distances to 50'. Up to 4096 12- or 16-bit words can be moved in one operation without program intervention. Other applications are in systems using PDP-8/A computers as front-end processors for large PDP-11 systems. **Computer Interface Systems, Inc,** PO Box 58, Piscataway, NJ 08854.
Circle 270 on Inquiry Card

DATA ACQUISITION SYSTEM



Series 2500 includes a fixed gain preamp and 2-pole active filters (Butterworth) per channel. Gain ranges and filter cutoff frequencies are determined by plug-in modules. Following the preamp/filter combination is a multiplexer, digital gain-controlled amp, S/H amp, and A-D converter. Featured are gains of X1 to X10,000, A-D converters with 10 to 15 binary bits, throughput rate of 50 kHz, common mode rejection ratio of 120 dB, S/H aperture time of 1 ns, and 64 channels in one 5¼" high cabinet. **Tustin Electronics Co,** 1431 E St. Andrews Pl, Santa Ana, CA 92705.
Circle 271 on Inquiry Card

REVERSIBLE STEPPER MOTOR

82900 series 5-Vdc bidirectional motor, providing 23-oz-in. max pull-in/out torque, has a frame size of 2¾ dia x 1 11/16". Std construction provides 2ϕ operation, 7-deg/30-min. step angle, and roller bearings. Optional design includes 4ϕ operation, 15-deg step angle, and sleeve bearings. Low heat rise and excellent heat dissipation result in lower op temp and more efficient power utilization. Applications include chart drives, small X-Y plotters, paper-feed drives for computer peripherals, and medical instrumentation. **North American Philips Controls Corp,** Cheshire, CT 06410.
Circle 272 on Inquiry Card

RAPID-ACCESS MEMORY

M300 disc memory system, storing up to 9 million bits on 128 tracks, with an avg access time of 12.5 ms, is a complete package including read/write electronics, track selection electronics, TTL interface, control electronics, and power supply—all contained in 10.5" of vertical rack space. A wide selection of interfaces and controllers is available, and electronics are packaged on a single PC board. Optimum gain select circuitry eliminates effects of the natural dynamic range of outputs from the head/disc surface. **Okidata Corp,** 111 Gaither Dr, Moorestown, NJ 08057.
Circle 273 on Inquiry Card

OPTICALLY COUPLED ISOLATORS

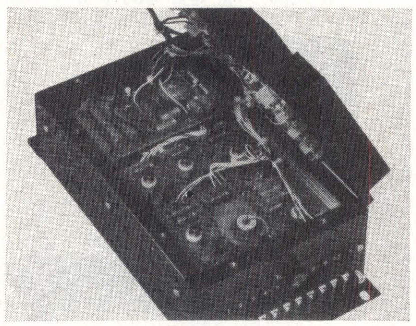
JEDEC-registered 4N22, -23, and -24 are designed to meet optical coupling requirements in high reliability applications. Comprised of a high-efficiency GaAs IR emitter coupled with a silicon phototransistor, devices are similar to the company's OPI 102 and 103 std isolators and are supplied in a hermetically sealed TO-5 package. Guaranteed min current transfer ratios are 25% for the -22, 60% for the -23, 100% for the -24. All feature 1-kV isolation. **Optron, Inc,** 1201 Tappan Cir, Carrollton, TX 75006.
Circle 274 on Inquiry Card

PRODUCTS

CHARACTER DISPLAYS

Three families of displays feature modular construction. Solid-state numeric devices, offering chars >2" tall, composed of LED segment arrays, require 5 V to operate. Solid-state alphanumeric offer char heights >3", either ASCII-II or Kata Kana format, and optional clock/driver and memory boards. Incandescent numeric offer char heights to 17", vertical/horizontal stacking, ac or dc lamp drivers, and front bulb replacement. All provide redundant coding of drive circuits and flexible interface configurations which allow simplex and multiplex addressing. **Electromedics,** 3295 Brookdale Dr, Santa Clara, CA 95051.
Circle 275 on Inquiry Card

MULTIPLE-OUTPUT POWER SUPPLY

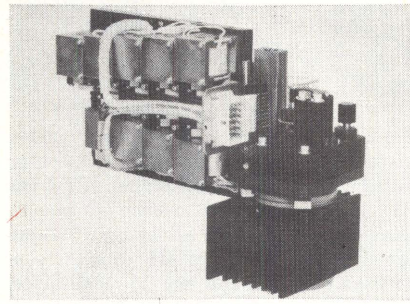


For high-reliability computer systems, model 2250, designed to deliver trouble-free power, is subjected to extensive burn-in testing. Available dc outputs are 5 V at 7 A, ±15 V at 0.5 A, 24 V at 1.5 A, and −20 V at 0.1 A. Inputs can be 24, 48, or 120 Vdc or 115 Vac, 60 Hz. Unit features high efficiency at full rated output, short circuit protection, reverse polarity protection, and switching preregulators. Dimensions are 12 x 6¼ x 4⅜". Custom-designed variations are available. **Autronics Corp,** 180 N Vinedo Ave, Pasadena, CA 91107.
Circle 276 on Inquiry Card

FLATBED PLOTTER

Model 430/101 Dataplotter[R] is designed for high speed plotting of digital graphic information. Lines do not exhibit step functions because plotting is performed in line segment rather than incremental mode. A digital servo (closed-loop) positive position system controls the pen, and velocity control optimizes plot speed. Included as std are 0.001" resolution which provides smooth curve plotting, "data verify" for absolute accuracy, control unit for easy interfacing to an online computer, and manual interrupt. **Broomall Industries, Inc,** 682 Parkway, Broomall, PA 19008.
Circle 277 on Inquiry Card

TAPE PERFORATOR MECHANISM



RPM 6120, for minicomputer, phototypesetting, and numerical controls applications, offers 120-char/s punch speed, bidirectional, and punches tape of five to eight levels, roll or fanfold, paper or mylar. Motor-driven tape feed and sprocket drive give positive control of longitudinal registration. Dimensions are 7.78 x 4.63 x 5.8", with weight <4 lb. Life expectancy is >8.4 x 10^7 char; punch life can be further extended by use of an optional carbide block. Also available is a 6-level advance-feed typesetter version. **Ex-Cell-O Corp, Remex,** 1733 Alton St, Santa Ana, CA 92705.
Circle 278 on Inquiry Card

PRINTER CONTROLLER

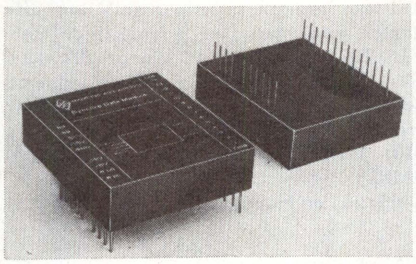
A switchable-model controller that permits the IBM 1403 printer to be used alternately with two different computers, G1403 series links the 1403 to non-IBM computers. A second computer interface can now be added to the system; the single printer controller can then be operated with either interface by actuating a front-panel switch. No program change to either computer is required. The controller is supplied in a standalone enclosure and includes all logic cards, memories, mating connectors, power supplies, and instructions. **Grumman Data Systems Corp,** 45 Crossways Park Dr, Woodbury, NY 11797.
Circle 279 on Inquiry Card

MINIATURE 400-Hz POWER TRANSFORMER

Encased in epoxy fiberglass, model 4A-7 provides 5 to 120 Vac with power rating of 7 W. Transformer has a wide variety of uses in airborne, space, missile, and military applications where small size and dependability are prime factors. Built to meet MIL-T-27C specs, encapsulated and hermetically sealed unit operates at 105°C amb. Regulation is <10% from no load to full load, efficiencies range from 90 to 93%, and dimensions are 1.37 x 1.25 x 1.31". **Abbott Transistor Laboratories, Inc, Transformer Div,** 5180 W Jefferson Blvd, Los Angeles, CA 90016.
Circle 280 on Inquiry Card

PRODUCTS

SYNCHRO-TO-DIGITAL CONVERTERS



Model LSI/85 S-D converter module, which uses an LSI chip, is TTL compatible and can also be used in MOS interfaces without modification. 14- and 10-bit resolution versions are available. Companion D-S module, series 785, provides 1.26-VA capability along with a high density package for operation between −55 and 105°C amb. Devices are pin-for-pin compatible with existing designs. Full mil temp range capability with ±3-min. accuracy at angular rates to 4000 deg/s are featured. **North Atlantic Industries, Inc,** Terminal Dr, Plainview, NY 11803.
Circle 281 on Inquiry Card

TRIPLE-OUTPUT DC-DC CONVERTER

Series C Iso-Pak modular, plug-in, dc-dc converter power supply delivers 9 W of regulated transformer-isolated dc voltages from inputs of 5, 6, 12, 15, 24, 28, or 48 Vdc. Output is 3-wire, regulated tracking, ±15 V, ±165 mA for analog/linear circuitry and 5 Vdc, 750 mA to power digital circuitry. Featured are separate transformer-isolated grounds, EMI/RFI shielding, and double-protection current limiting. Unit is housed in a 2.56 x 3 x 0.75" black metal case, shielded on all six sides. **Stevens-Arnold, Inc,** 7 Elkins St, South Boston, MA 02127.
Circle 282 on Inquiry Card

DIP SOCKETS

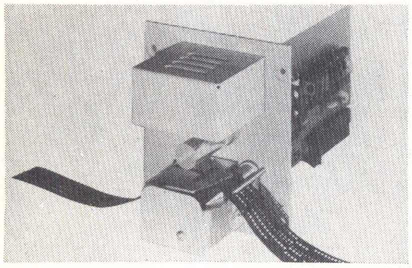
8204 series, for IC applications, allow 0.5" PC board spacing with an overall height of 0.19", and 0.1" contact spacing end-to-end or side-to-side. High-force phosphor bronze contacts insure electrical integrity. Contacts are pretinned, anti-wicking, and meet EIA specs. Wide-angle lead-ins accept a full range of pin sizes, and housing is visually marked for insertion accuracy. Contact springs grip the edge of the IC so that the sharp burr on stamped lead frames will not cut through the plating. **Thermalloy, Inc,** PO Box 34829, 2021 W Valley View Lane, Dallas, TX 75234.
Circle 283 on Inquiry Card

PRODUCTS

ASYNCHRONOUS CONTROLLER

A 4-channel asynchronous line adapter on a single board—for the SUE computer system—is capable of local or remote interfacing of up to four CRTs, modems, plotters, or printers. Each channel is individually controlled and programmed for data format, baud rate, status, and commands, and can operate in either full- or half-duplex mode. Interface is compatible with EIA RS-232-C and Bell 103 or 202 data sets. Up to 15 baud rates are jumper selected on each channel. **Lockheed Electronics Co, Inc, Data Products Div,** 6201 E Randolph St, Los Angeles, CA 90040.
Circle 285 on Inquiry Card

PHOTOELECTRIC TAPE READER

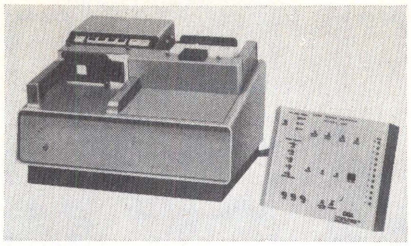


Econoread 150 reads any std 8-level 1" tape, including paper, mylar, aluminum, and aluminum mylar, without adjustments. Light source is a std long-line filament lamp, derated from 12 to 8 V, assuring >10,000 hr of life. A stepping motor drive stops on char at 150 char/s. One circuit card provides compatibility for DTL, TTL, or CMOS. Voltage regulators are mounted on the board, requiring only a single voltage of 24 to 28 V to drive the bidirectional reader. An out-of-tape switch is also std. **BAI, Data Products Div,** PO Box 681, Cherry Hill, NJ 08003.
Circle 284 on Inquiry Card

POLARIZED CONNECTORS

Featuring polarized or keyed insulator bodies, this line of DIP plugs, sockets, and interconnects incorporates offset guides and matching holes; thus they cannot be laterally misconnected or reverse connected (end to end). Selection includes 14-, 16-, and 24-pin plugs and interconnects with 26 combinations of pin dimensions for each length. To prevent intermixing 14- and 16-pin plugs of the same width, polarized guides are located in different positions on the insulator body. **Circuit Assembly Corp,** 3169 Red Hill Ave, Costa Mesa, CA 92626.
Circle 286 on Inquiry Card

IN-FIELD TESTER FOR CARD READERS

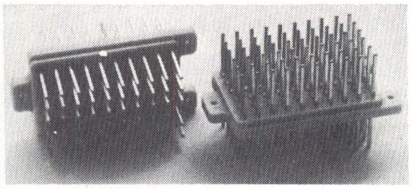


Model 100 card reader/analyzer, for use with Documation series M and D card readers, is plugged into the card reader interface connector. Using a prepunched deck of identical test cards, the user loads the first card and then, col by col, steps through memory to ensure that the card was correctly read. Simultaneously, the analyzer tests all 19 interface signals and pinpoints any malfunction. Once the first test card is read and stored in memory, the balance of the deck is read at the max operating speed of the reader. **Peripheral Sciences, Inc,** 203 E Main St, Norristown, PA 19401.
Circle 287 on Inquiry Card

MULTIPLE-OUTPUT LAB POWER SUPPLIES

Triple-output Pocket-Sized series of variable and preset voltage models contains, in a single package, voltages required for both digital and discrete circuits. One version includes variable dual ±9 to ±18 Vdc at 100 mA and 5 Vdc at 1 A output; the other two have preset ±15 Vdc at 100 and 200 mA outputs for discrete, and 5 Vdc at 500 mA and 1 A outputs, respectively, for digital circuitry. Other specs include 1% error preset voltage accuracy; regulation 0.05% line, 0.01% load; and ripple <1 mV rms. **Instant Instruments Inc,** 306 River St, Haverhill, MA 01830.
Circle 288 on Inquiry Card

60-PIN TERMINAL BLOCK



High-density terminal block for chassis mounting provides 60 terminations/terminal block and mounts in 1¾" of rack space. Interlocking feature permits mounting 6 blocks/rack space, for a total of 360 terminations. External dimensions are 1⅜ x 2⅝". Tin-plated brass terminals measure 0.045" sq. Molded, glass-filled nylon blocks are easily mounted with three screws. **ADC Products,** 4900 W 78th St, Minneapolis, MN 55435.
Circle 289 on Inquiry Card

LITERATURE

Computer/Management Science Courses

Catalog details data base technology, data communications, software technology, minicomputer technology, systems management, and computer auditing/security/privacy courses. **Control Data Corp, The Institute for Advanced Technology,** Rockville, Md.
Circle 300 on Inquiry Card

Electronic Components

Complete line of glass, glass-ceramic, ceramic, and microminiature solid-tantalum capacitors and metal-film resistors is described in catalog. **Corning Glass Works, Electronic Products Div,** Corning, NY.
Circle 301 on Inquiry Card

LED Lamps, Displays

Selection guide for GaP lamps gives lens description, power dissipation, and typ luminous intensity as well as optional designs for cathodes and anodes. **Opcoa, Inc,** Edison, NJ.
Circle 302 on Inquiry Card

EDP Minicomputers

Role of minicomputers in business data processing applications is explored in comprehensive technical report. **Formation, Inc,** Mount Laurel, NJ.
Circle 303 on Inquiry Card

Uninterruptible Power Systems

Ac power conversion systems for industrial and telecommunications markets are covered in illustrated brochure which provides complete features and specs. **Lorain Products Corp, a sub of Reliance Electric Co,** Lorain, Ohio.
Circle 304 on Inquiry Card

Stepping Motors

Catalog introduces 32 uni- and bidirectional stepping motors, designed to position inertia or friction loads remotely in 10-, 15-, 20-, or 30-deg increments. **Ledex Inc,** Dayton, Ohio.
Circle 305 on Inquiry Card

Microprocessor Conference

Microprocessors: Economics/Technology/Applications, which includes papers presented at First National Microprocessor Conference, held in 1974, is offered at $145 (volume discounts available). **Arthur D. Little, Inc,** Acorn Park, Cambridge, MA 02140; attn: Marjorie Maws.

Optoelectronics Products

Selection guide covering LED displays/lamps as well as isolators and photodetectors gives specs and application information. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 306 on Inquiry Card

Firing Circuit Noise Discrimination

Discrimination of signals from electrical noise caused by energization or de-energization of reactive loads in the vicinity of thyristors is the topic of illustrated article. **Westinghouse Electric Corp, Semiconductor Div,** Youngwood, Pa.
Circle 307 on Inquiry Card

Programmable Controller Systems

Reprint articles on proven applications and design considerations when using programmable controllers for online industrial use are presented in handbook. **I·T·E Datametrics,** Wilmington, Mass.
Circle 308 on Inquiry Card

Advanced Control Concepts

Three videotapes on "The Values of Process Control" are directed toward various levels of plant operation, including process and instrumentation engineers and manufacturing and management personnel. **The Foxboro Co, Educational Services,** Foxboro, Mass.
Circle 309 on Inquiry Card

Frequency Synthesizers

Catalog contains detailed descriptions and specs on frequency synthesizers and ancillary instrumentation for frequency analysis, monitoring, and control. **Adret Corp,** Lancaster, Pa.
Circle 310 on Inquiry Card

Uninterruptible Power Systems

Brochure describing user features plus details on reducing operating costs illustrates applications, system components, and controls. **Static Power, Inc,** Newport Beach, Calif.
Circle 311 on Inquiry Card

Microelectronics Seminar

92-page book containing papers presented at Interface '74 Microelectronics Seminar held in San Diego is available for $3.50 (applicable state/local taxes must be included). **Eastman Kodak Co,** Dept 454, 343 State St, Rochester, NY 14650.

Digital Line Scan Camera

Technical brochure on electronic line scan camera system, which makes possible rapid, accurate noncontact measurements of size, shape, and position for control of manufacturing processes, also covers illuminators and controllers. **Reticon Corp,** Sunnyvale, Calif.
Circle 312 on Inquiry Card

Logic-Circuit Testing

700-page, 4-volume illustrated handbook is intended to help companies improve utilization of their present testers and reduce time required to evaluate new test techniques. **Omnicomp,** Phoenix, Ariz.
Circle 313 on Inquiry Card

7-Segment Readout Assemblies

Technical bulletin describes Mini-Pak^R gas-discharge readout assemblies, designed for instruments or systems where packaging and panel limitations are of paramount importance. **Canyon Electronics,** Phoenix, Ariz.
Circle 314 on Inquiry Card

Solid-State Programmable Controller

Illustrated brochure details PC32X24, designed for automated electronic control/operation of machinery and manufacturing processes. **Intercontinental Dynamics Corp,** Bridgeview, Ill.
Circle 315 on Inquiry Card

Automatic Test Equipment

Systems and instruments for testing ICs, transistors and diodes, subassemblies, passive components, and laser trimming are detailed in catalog which also announces new products. **Teradyne, Inc,** Boston, Mass.
Circle 316 on Inquiry Card

Hand-Held Terminal

Brochure discusses some of the ways a hand-held terminal breaks restraints of location, utilization, size, and interface that presently restrict the use of conventional computer terminals. **Termiflex Corp,** Nashua, NH.
Circle 317 on Inquiry Card

Microcircuit Reliability

Comprehensive bibliography provides means for quickly locating latest government and industry reports, conference proceedings, and open literature on microcircuit reliability. Order 3-volume set ($50 delivered/$60 non-U.S.), 1975 edition ($40/$48), or 1974 ($15/$18) from **Reliability Analysis Center,** RADC (RBRAC), Griffiss AFB, NY 13441. Make checks payable to IIT Research Institute.
Circle 318 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

PAGE

HARDWARE

BREADBOARDS

Microprocessor Prototyping/Production System
Applied Computing Technology 96

CONNECTORS AND INTERCONNECTION SYSTEMS

PC Connectors
Viking Industries 9

PC Edgeboard Connectors
GTE Sylvania/Parts 20

Display Connector
Dale Electronics 117

Metric Connector
AMP 107

Polarized Connectors
Circuit Assembly 124

Flat Cable/Connector System
3M 5

Box Connector, Cable Assemblies
Mupac 110

FANS AND BLOWERS

Fans
IMC Magnetics/New Hampshire 16

INDICATORS; READOUTS: DIGITAL DISPLAYS; LAMPS

Digital Indicator
Novatronics of Canada 112

Character Displays
Electromedics 122

Small LEDs
Digital Components 110

LED Lamps
Chicago Miniature/Drake 105

PANELS AND BACKPLANES

Wire-Wrap Panels
Garry Mfg. 55

SOCKET BOARDS AND CARDS

Microprocessor Socket Cards
EECO 116

SOCKETS

DIP Sockets
Thermalloy 123

WIRING PINS & TERMINALS

Wiring Pins
Art Wire & Stamping 118

60-Pin Terminal Block
ADC Products 124

COMPONENTS AND ASSEMBLIES

FILTERS

RFI/EMI Filters
RtroN 114

MOTORS; ROTATIVE COMPONENTS

Micro Motors
Hitachi America 62

DC Motors
Motor Products Owosso 101

Reversible Stepper Motor
North American Philips Controls 121

Synchros & Resolvers
Singer/Kearfott 106

PHOTO DEVICE ASSEMBLIES

Optical Switches
Clairex Electronics 115

Optically Coupled Isolators
Optron 121

POWER SOURCES, REGULATORS, AND PROTECTORS

Power Supplies
Modular Power 111
Trio Laboratories 104

Switching Power Supplies
ACDC Electronics 43

PAGE

Multiple-Output Power Supply
Autronics 122

Triple-Output Benchtop Power Supply
Acopian 110

Multiple-Output Lab Power Supplies
Instant Instruments 124

Power Supply Card
Destek Industries 112

Power Supply Modules
Computer Products 97

Open Frame Power Modules
Deltron 109

Regulated DC-DC Power Sources
Reliability 111

Triple-Output DC-DC Converter
Stevens-Arnold 123

Voltage Regulators
Signetics 105

Miniature Power Transformer
Abbott Transistor Laboratories/Transformer 122

RELAYS

Miniature Relays
International Rectifier/Crydom 112

SEMICONDUCTOR COMPONENTS

DMOS FETS
Signetics 107

SENSORS

Solid-State Sensor
Micro Switch/Honeywell 115

Temperature Sensor
Multi-State Devices 112

SWITCHES

Thumbwheel Switches
C&K Components 119

Lighted Pushbutton Switches
Illuminated Products 97

Subminiature Toggle Switch
Instru-Mech 112

Snap-In Momentary Pushbutton Switch Bezel
C&K Components 110

Computer Switch System
T-Bar 117

CIRCUITS

CIRCUIT CARDS AND MODULES

Analog Function Modules
Data Translation 4

PC Board Shorts Detection System
Teradyne 117

DIGITAL & INTERFACE INTEGRATED CIRCUITS

ECL ICs
Plessey Semiconductors 79

Hi-Rel ICs
Signetics 109

RAMs, p/ROMs, Memory ICs
Signetics **111, 113, 115, 117, 118, 119**

PMOS 1K RAM
Fairchild Camera & Instrument/ Integrated Circuits 107

16K ROM
Mostek 114

p/ROMs
Harris Semiconductor 72

Interface ICs
Signetics 120

Microprocessors
American Microsystems **31,** 95
Mostek 97

Transmitter/Receiver ICs
Western Digital 15

Shottky TTL Bus Transceivers
Advanced Micro Devices 105

Multiplying D-A Converter
Precision Monolithics 119

PAGE

Timer ICs
Ferranti Electric 107

CMOS 4-Bit Comparator
Solid State Scientific 114

16-Bit LSI Polynomial Generator
Motorola/Semiconductor Products 113

LINEAR INTEGRATED CIRCUITS

Voltage Regulators
Signetics 105

Dual Op Amp
Harris Semiconductor 109

MEMORY/STORAGE EQUIPMENT

FLEXIBLE DISC STORAGE EQUIPMENT

Flexible Disc Drives & Systems
Ex-Cell-O/Remex 52

Flexible Disc Drive
Pertec/Peripheral Equipment 112

Flexible Disc Systems
Ball Computer Products 45

Flexible Disc Subsystem
Data General 119

MAGNETIC CORE STORAGE EQUIPMENT

Core Memory Systems
Ampex/Memory Products 34
Cipher Data Products 110
Dataram 71
Standard Memories 121

Microprocessor-Compatible Core Memory
Litton Memory Products/ Litton Industries 110

MAGNETIC DISC AND DRUM STORAGE EQUIPMENT

Disc Memories
General Instrument/Rotating Memory Products 51

Disc Memory System
Okidata 121

Disc Drives
California Computer Products 103
Diablo Systems ....**Cover IV**

Cartridge Disc Drive
Vermont Research 109

MAGNETIC TAPE STORAGE EQUIPMENT

Cassette Tape Subsystem
Kybe 113

Cassette Paper Tape Emulator
Ex-Cell-O/Remex 52

Tape Drive
Data Disc 105

Variable Speed Data Storage Device
Raymond Automation Labs 117

ROM & p/ROM PROGRAMMERS

p/ROM Programmer
Spectrum Dynamics/Adar Associates 114

SEMICONDUCTOR STORAGE EQUIPMENT

RAMS, p/ROMs, Memory ICs
Signetics **111, 113, 115, 117, 118, 119**

PMOS 1K RAM
Fairchild Camera & Instrument/ Integrated Circuits 107

16K ROM
Mostek 114

p/ROMs
Harris Semiconductor 72

High Speed, Static n-MOS Memory Card
Advanced Memory Systems 112

INPUT/OUTPUT AND RELATED EQUIPMENT

DATA TERMINALS

Data Terminals
Teletype 10

PAGE

CRT Display Terminals
Lear Siegler/Electronic Instrumentation 99
Princeton Electronic Products 123
Research 13

Intelligent CRT Display Terminals
Hewlett-Packard 23

Intelligent Printer Terminal
Xerox 120

Remote Batch Terminals
General Automation 17

Pollable Interactive Transaction Terminal
Varian Data Machines/ Peripheral Products 102

Terminal Exerciser
Mission Data Products 115

DISPLAY EQUIPMENT

Visual Memory System
Datavision Video Products/ Mincom/3M 107

GRAPHIC EQUIPMENT

Optical Digitizers
EMR Photoelectric 89

Sonic Digitizers
Science Accessories 121

Digitizer Data Acquisition System
Altek 102

INTERFACE EQUIPMENT; CONTROLLERS

Interprocessor Communications Interface
Computer Interface Systems 121

Disc & Tape Controllers
Ball Computer Products 45

Communications Controller Board
Data General 27

Asynchronous Controller Board
Lockheed Electronics/Data Products 124

Printer Controller
Grumman Data Systems 122

KEYBOARD EQUIPMENT

Keyswicthes
Stackpole Components 112

PAPER TAPE EQUIPMENT

Paper Tape Equipment
Ex-Cell-O/Remex 52, 116

Paper Tape Perforator/Reader
Tally 2

Paper Tape Reader
EECO 25

Photoelectric Tape Reader
BAI/Data Products 124

Paper Tape Punch
Data Specialties 113

PLOTTING EQUIPMENT

Digital Plotter
Zeta Research 61

Flatbed Plotter
Broomall Industries 122

PRINTER/PLOTTERS

Electrostatic Printer/Plotter
Versatec 47

PRINTING EQUIPMENT

Line Printer
Tally Cover II

132-Column Printer
Scope Data 110

Printer Controller
Grumman Data Systems 122

Digital Printers
C. Itoh Electronics/Systems & Components 4, 114
Practical Automation 60

Dot Matrix Printers
North Electric/Electronics 114
TL Industries 110

PUNCH CARD EQUIPMENT

In-Field Tester For Card Readers
Peripheral Sciences 124

COMPUTERS AND COMPUTER SYSTEMS

AUTOMATIC TEST SYSTEMS

Automatic Logic Card Tester
Technology Marketing 118

COMPUTER AUXILIARY UNITS

Program Loaders
Electronic Processors 59

PAGE

MICROCOMPUTERS AND MICROPROCESSORS

Microprocessors
American Microsystems 31, 95
Mostek 97

Microcomputers
Control Logic 80
Digital Equipment/Components 119
Martin Research 98
Microdata 64

Microcomputer System
Data Numerics 98

Microcomputer Development System
Intel 94

Microcomputer Controller
Process Systems 111

Traffic Control Microcomputer
Philips Telecommunicatie Industrie/ Traffic Automation 98

Microprocessor Logic Recorder/Analyzer
Vector Associates 96

Microprocessor Software
Microtec 95

Microprocessor Macro Cross-Assemblers
Zeno Systems 97

MINICOMPUTERS; SMALL- & MEDIUM-SCALE COMPUTERS

Computers
Data General 63
Digital Equipment 40

Minicomputers
Computer Automation 28
Hewlett-Packard 19
Interdata 92, 122
Systems Engineering Labs Cover III

Interprocessor Communications Interface
Computer Interface Systems 121

DATA COMMUNICATIONS EQUIPMENT

COMMUNICATIONS MONITOR

Data Line Monitor
Digi-Log Systems 109

COMMUNICATIONS MULTIPLEXERS

TDM Modules
Intertel 118

MODEMS; DATA SETS

Data Modems
Intech Laboratories 102
Rockwell International/Collins Radio 112
Terminal Communications/United Aircraft 105

9600-Bit/s Short Haul Modem
Penril 115

Data Set
International Communications/Milgo Electronic 116

OTHER DATA COMMUNICATIONS EQUIPMENT

Automatic Calling Unit
Warren G-V Communications/Sola Basic Industries 120

LSI Transmission Error Detector
Motorola/Semiconductor Products 113

DATA ACQUISITION AND CONTROL EQUIPMENT

A-D AND D-A CONVERTERS

A-D Converters
Computer Labs 120
Datel Systems 115

Multiplying D-A Converter
Precision Monolithics 119

ANGLE AND POSITION ENCODERS

Optical Incremental Encoders
Data Technology 116

DATA ACQUISITION SYSTEMS

Data Acquisition System
Tustin Electronics 121

DATA TRANSFER AND INTERFACE EQUIPMENT

Process-Computer I/O Interface
IPAC 38

Serial Data Exchange Subsystem Cards
Analog Devices/Modular Instrumentation 100

MONITORING AND CONTROL EQUIPMENT

Microcomputer Controller
Process Systems 111

PAGE

Counter/Controller
Durgin & Browne 118

Miniature Counter/Controller
Veeder-Root 111

Multiplexed Control System
Futronix 105

SCANNERS

Automatic Scanner
Julie Research Laboratories 116

SYNCHRO-DIGITAL & DIGITAL-SYNCHRO CONVERTERS

Synchro-To-Digital Converter Modules
North Atlantic Industries 123

Synchro-To-Digital Converter Interface
G&S Systems 116

TEST & MEASUREMENT EQUIPMENT; INSTRUMENTATION

Modular Instrumentation
Tektronix 33

COUNTERS

Counter/Controller
Durgin & Browne 118

Miniature Counter/Controller
Veeder-Root 111

DATA GENERATORS

Digital Word Generator/Receiver
Moxon 107

DIGITAL EQUIPMENT TESTERS

Digital Logic Recorders
Biomation 37, 39

Microprocessor Logic Recorder/Analyzer
Vector Associates 96

Automatic Logic Card Tester
Technology Marketing 118

TTL/CMOS-Compatible Logic Probe
Aikenwood/Zi-Tech 109

PC Board Shorts Detection System
Teradyne 117

In-Field Tester For Card Readers
Peripheral Sciences 124

Terminal Exerciser
Mission Data Products 115

INSTRUMENT GENERATORS

Function Generators
Dana Exact Electronics 113
Wavetek 110

METERS

Digital Multimeters
California Instrument 124
John Fluke Mfg. 16

OSCILLOSCOPES

Pattern Analyzer
Hewlett-Packard 49

SIGNAL AND CODE CONVERTERS

Serial Data Exchange Subsystem Cards
Analog Devices 100

OTHER PRODUCTS; SERVICES

EDUCATION

Microcomputer Workshops
PCS 96

EXHIBITIONS

Computer Conference & Exhibiiton
WESCON 108

MARKET REPORTS

Market Reports
Frost & Sullivan 120

SERVICES

Microprocessor/RAM Service Center
Macrodata 96

SOFTWARE

Core-Resident Operating System
Systems Engineering Labs 110

Microprocessor Software
Microtec 95

Microprocessor Macro Cross-Assemblies
Zeno Systems 97

OTHER NON-DIGITAL PRODUCTS

Cable Tie Tools
Panduit 117

Office Furniture
Systems Furniture 123

ADVERTISERS' INDEX

ACDC Electronics, Inc. 43
Adar/Spectrum Dynamics 114
American Microsystems, Inc. 31
Ampex Corp., Memory Products Div. 34, 35
Art Wire & Stamping Co. 118

Ball Computer Products, Inc. 45
Biomation 37, 39

C & K Components 119
California Computer Products 103
California Instruments 124
Centronics Data Computer Corp. 57
Clairex Electronics 115
Computer Automation, Inc. 28, 29
Computer Products, Inc. 97
Control Logic, Inc. 80

Data General Corp. 27, 63
Dataram Corp. 71
Data Translation, Inc. 4
Diablo Systems, Inc. .... Cover IV
Digital Equipment Corp. 40, 41

EECO 25
Electronic Processors, Inc. 59
EMR Photoelectric, Inc. 89
Ex-Cell-O Corp., Remex 52, 53

John Fluke Manufacturing Co., Inc. 16
Frost & Sullivan, Inc. 120

Garry Manufacturing Co. 55
General Automation 17
General Instrument Corp. 51
GTE Sylvania, Parts Div. 20, 21

Harris Corp., Semiconductor Div. 72
Hewlett-Packard Co. 19, 23, 49
Hitachi America, Ltd. 62

Illuminated Products, Inc. 97
IMC Magnetics Corp. 16
Interdata 92, 93, 122
The IPAC Group, Inc. 38
C. Itoh Electronics, Inc. 4

Kybe Corp. 113

Lear Siegler, Inc. 99

3M Co. 5
Microdata Corp. 64
Modular Power 111
Motor Products Owosso Corp. 101

Panduit Corp. 117
Plessey Semiconductors 79
Practical Automation, Inc. 60
Princeton Electronic Products, Inc. 123

Research, Inc. 13

Science Accessories Corp. 116
Signetics Corp. 6, 7, 105, 107, 109, 111, 113, 115, 117, 118, 119, 120
Singer Co., Kearfott Div. 106
Spectrum Dynamics, Div of Adar Assoc., Inc. 114
Standard Memories, Inc. 121
Systems Engineering Laboratories .... Cover III
Systems Furniture Co. 123

Tally Corp. .... Cover II, 1, 2
Tektronix, Inc. 33
Teletype Corp. 10, 11
Trio Laboratories, Inc. 104

Versatec, Inc. 47
Viking Industries, Inc. 9

WESCON 108
Western Digital Corp. 15

Zeta Research, Inc. 61

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