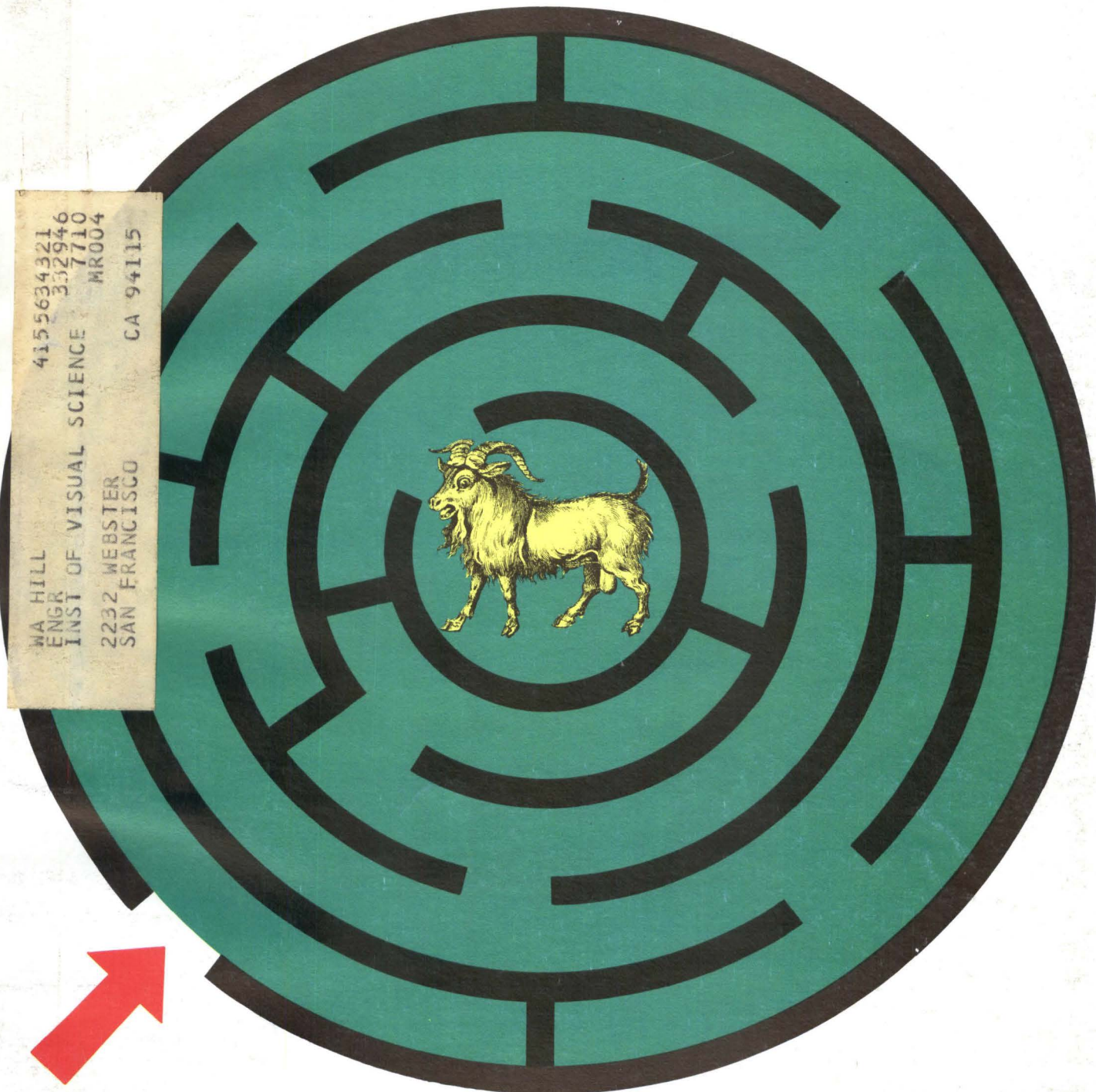


COMPUTER DESIGN

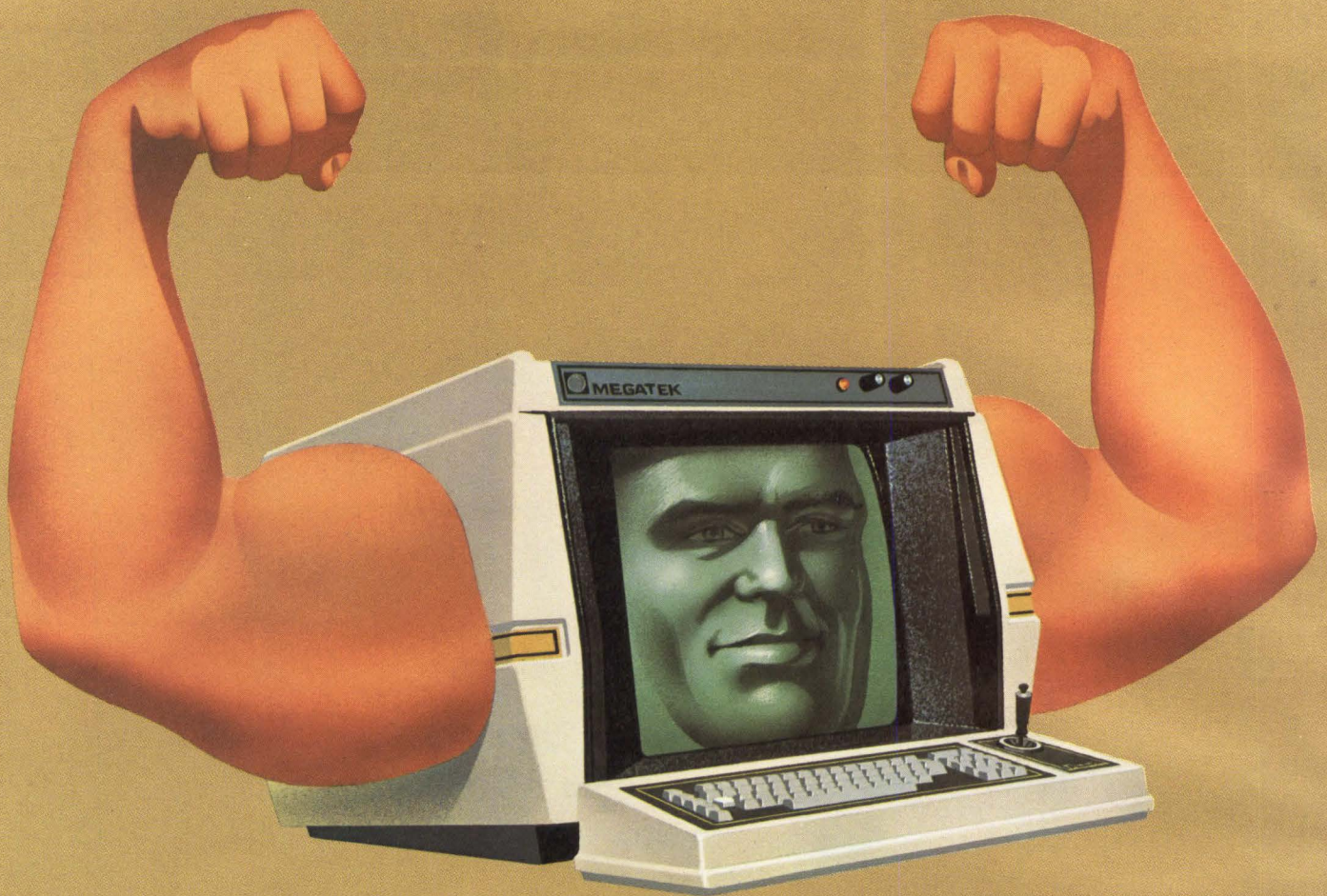
THE MAGAZINE OF DIGITAL ELECTRONICS

MARCH 1979



WA HILL
ENGR
INST OF VISUAL SCIENCE
2232 WEBSTER
SAN FRANCISCO
415 563 3432
332946
7710
MR004
CA 94115

DYNAMIC RAM CONTROLLER PERFORMANCE/COST TRADEOFFS
FORECASTING COMPUTER SYSTEM RELIABILITY WITH A HANDHELD PROGRAMMABLE CALCULATOR
COMPARISON OF SELECTED ARRAY PROCESSOR ARCHITECTURES



All muscle and no fat.

Most refresh graphic systems are flabby. With lots of features you don't need. Without a few you do.

The MEGATEK 7000 is built lean. You get fast graphics throughput. A high resolution, real-time, interactive display. Complete system modularity. An unmatched refresh graphics system. At a price that makes sense.

A built-in 32-bit microcomputer with a 64K byte, 32-bit wide refresh memory, expandable to 128K. Lets you process graphics data fast. And, saves you host computer time. Add MEGATEK's advanced vector generator and you get unbeatable graphics throughput.

Vectors and characters are displayed instantly. With precision end point matching. And constant intensity. 12-bit resolution is standard. Vector quality that outclasses every other refresh system.

Easy-to-use real-time interactive graphics. Outstanding display



dynamics. Hardware translation, blink, dashed lines. Absolute and relative jump. All standard. And, hardware clip, rotate, scale, and zoom are available as well.

Plus, the MEGATEK 7000 is easy to look at. 16 levels of image intensity. 8 programmable character sizes. The screen is clear and readable, even in a brightly lit room. And, with selective erase, you don't have to blank the screen to change a vector or symbol.

Add a universal computer interface that connects to any host computer. Field-proven software that cuts system development cost. A full line of

peripherals and accessories. Even color, if you need it. And, you have the most powerful refresh graphics terminal for your dollar on the market today.

But, don't take our word. Prove it to yourself. Call or write for a demonstration. And remember, the MEGATEK 7000 is backed by a national service network with fast, hot-line access.

For full details, write or call Peter J. Shaw, MEGATEK, 3931 Sorrento Valley Blvd., San Diego, CA 92121. (714) 455-5590. TWX: 910-337-1270. (European office: 14, rue de l'Ancien Port. 1201 Geneva, Switzerland. Phone: (022) 32.97.20 Telex: 23343.)

The Visible Difference



MEGATEK
CORPORATION

CIRCLE 1 ON INQUIRY CARD

Models 9100/9300 Vacuum Column Tape Transports . . . Proven. Period.

Kennedy's vacuum column digital tape transports weren't designed yesterday to grab a piece of a growing market. In fact, they virtually founded the vacuum column market. They were the first to have such features as a capacitive tape-location detector for improved tape life; air bearings and hardcoated read-after-write heads to reduce tape wear and improve data integrity.

Model 9100 (75 ips) and 9300 (125 ips) offer crystal controlled timing, read-after-write shortened skew gate, front-accessible test panel, quick release hubs and simplified tape loading.

Data densities are 200/556 cpi or 556/800 on 7-track units and 800 cpi, 1600 cpi or 800/1600 cpi on 9-track transports. The format is NRZ1/PE.

Models 9100/9300 offer more features, more performance, and most important, more time-in-the-field than any competitive units.

Why do we think so? Simple. Our figures show that we are about 3000 satisfied users ahead at this point.

KENNEDY CO.

540 W. WOODBURY RD., ALTADENA, CALIF. 91001
(213) 798-0953



KENNEDY-QUALITY-COUNT ON IT

CIRCLE 2 ON INQUIRY CARD

FOR OFFICES THAT WANT TO KEEP IT QUIET, THE NEW TALLY HUSH-TONE KEEPS THE LID ON NOISE.

If printer noise disturbs your office serenity, you'll appreciate the mel-low decibels of the whisper-quiet Tally Hush-Tone. Our special acoustically designed enclosure attenuates printing noise level down to an unheard of quiet level. When not printing, the Hush-Tone is totally quiescent.

TALLY[®] **PRINTERS** **WORLDWIDE**

OEM SALES OFFICES

Boston (617) 272-8070
New York (516) 694-8444
Chicago (312) 885-3678
Los Angeles (213) 378-0805
Miami (305) 665-5751
Philadelphia (215) 628-9998
San Jose (408) 247-0897
Seattle (206) 251-6730

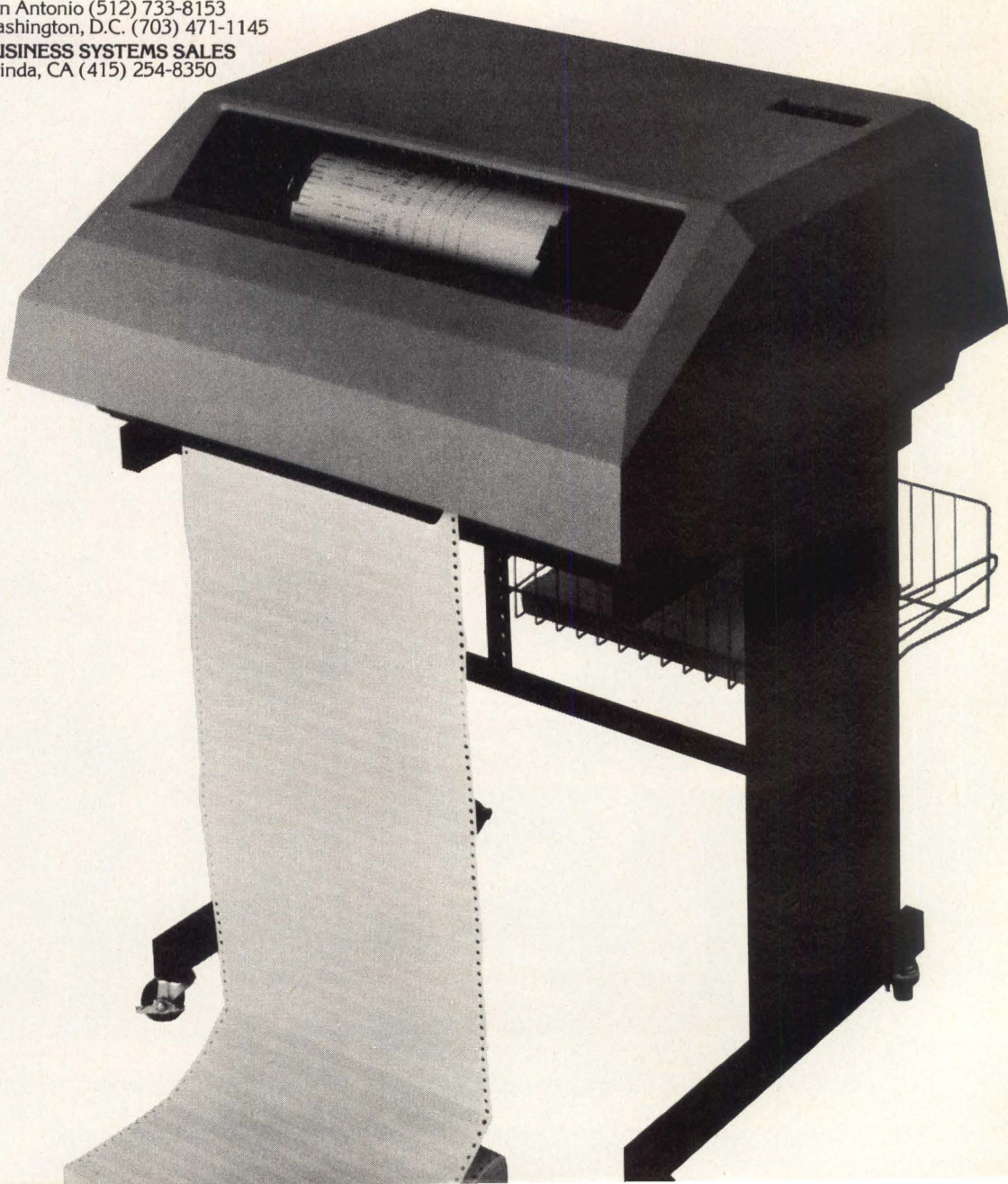
San Antonio (512) 733-8153
Washington, D.C. (703) 471-1145
BUSINESS SYSTEMS SALES
Orinda, CA (415) 254-8350

CIRCLE 3 ON INQUIRY CARD

Available at 125 and 200 lines per minute, the Tally Hush-Tone is easy to live with, easy to operate. And easy on the pocketbook. It's the newest member of the Tally T-2000 series—the most reliable (and lowest cost of ownership) line printers you can buy. Remember, Tally line printers never need adjustments, lubrication nor preventive maintenance. And you can always count on consistent print quality.

The Tally Hush-Tone. You get more than quiet performance. You get up-time performance.

Call or write today. Tally Corporation, 8301 South 180th Street, Kent, Washington 98031. Phone (206) 251-5500.



COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

MARCH 1979

VOLUME 18, NUMBER 3

DEPARTMENTS

- 6 LETTERS TO THE EDITOR**
- 10 CALENDAR**
- 12 COMMUNICATION CHANNEL**
Second in data communications testing series examines common sources of trouble on the digital side of the link, and presents clues on how to find them
- 38 DIGITAL TECHNOLOGY REVIEW**
Regular preventive maintenance can reduce both downtime and cost of maintaining peripheral equipment. Optimum service interval can be predicted using statistical data on failure rates and service time
- 80 DIGITAL CONTROL AND AUTOMATION SYSTEMS**
Computers of varied sizes automate a cold-rolling steel mill in Connecticut, control traffic in Georgia, and direct distribution of mail in Denmark
- 176 MICRO DATA STACK/COMPUTERS, ELEMENTS, AND SYSTEMS**
Full comprehension of DMA interfacing—accessing memory locations without using the CPU—allows its use in high speed data transfer applications
- 196 AROUND THE IC LOOP**
Error correction coding raises reliability of large memory systems by eliminating the effects of isolated single-bit failures, but results in increased system cost and decreased speed
- 210 PRODUCT FEATURE**
A single-board microcomputer features direct compatibility with industry standard bus structure and software plus 32-bit floating point arithmetic
- 246 LITERATURE**
- 248 GUIDE TO PRODUCT INFORMATION**
- 252 ADVERTISERS' INDEX**

Reader Service Cards
pages 255-258



CIRCULATION: 67,155
(JUNE 1978)

Copyright 1979, Computer Design Publishing Corp.
(USPS 127-340)

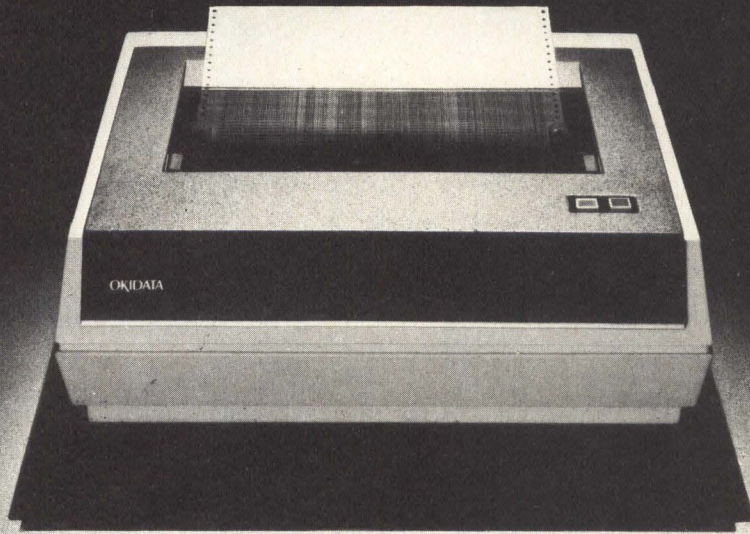
FEATURES

- DYNAMIC RAM CONTROLLER PERFORMANCE/COST TRADEOFFS 127**
by Andrew Volk
Proper memory access timing and refresh requirements for designing dynamic RAMs to interconnect to a microprocessor based system overcome common operational difficulties
- FORECASTING COMPUTER SYSTEM RELIABILITY WITH A HANDHELD PROGRAMMABLE CALCULATOR 141**
by Ronald Zussman
Reliability analysis program for handheld calculator is fast and easy to implement, estimates computer system dependability, identifies failure-prone subsystems, and delineates where redundant elements result in optimum reliability
- COMPARISON OF SELECTED ARRAY PROCESSOR ARCHITECTURES 151**
by Stephen P. Hufnagel
Study of two commercially available programmable array processors with emphasis on architectural differences reveals operating and performance characteristics that may be attributed to each
- TROUBLESHOOTING MICROPROCESSORS WITH A LOGIC ANALYZER SYSTEM 160**
by Robert Lorentzen
Multichannel digital logic analyzer systems are useful tools for studying, diagnosing, and correcting complex microprocessor hardware and software malfunctions
- HIGH SPEED LOW ERROR DATA TRANSMISSION WITH FIBER OPTICS 166**
by Hans O. Sorensen
Fundamentals of fiber optic data transmission system design and how they are applied are demonstrated by detailed description of an available system

CONFERENCES

- INTERFACE 104**
Session topics including terminal trends, software, networks, and digital communications technology will explore new directions in data communications and distributed data processing
- ELECTRO 110**
Program sessions and exhibits, focusing on electronics in the 80s, present state-of-the-art and career topics including microprocessors, fiber optics, LSI, and computer imaging

The New Slimline Series From Okidata



Line Printers That Sell Minisystems

The Okidata Slimline Series, a new family of microprocessor-controlled, 132 column line printers. A wide range of speeds, options and plug-compatible interfaces, all supported with common spares.

Common spares but uncommon price, performance and reliability. OEM prices that create new mini-system opportunities, print quality that helps sell the businessman and Okidata reliability and maintainability—unmatched in the industry. A 500,000,000 character head warranty and stored program machine history that replaces customer installation records.

The Slimline, available in 300, 250, 160 and 125 LPM models. Twelve program-selectable fonts, 5 x 7, 7 x 7 and 9 x 7 characters, and graphics capability. The Slimline, backed by a worldwide sales and service organization.

OKIDATA

Okidata Corporation
111 Gaither Drive
Mount Laurel, New Jersey 08054
Telephone: 609-235-2600

STAFF

Publisher and
Editorial Director
Robert Brotherston

Associate Publisher
Anthony Saltalamacchia

Editor
John A. Camuso

Managing Editor
Sydney F. Shapiro

Technical Editor
George V. Kotelly

West Coast Editor
Michael Chester
Arcadia, Calif.
(213) 574-7447

Associate Editors
Peggy Killmon
James W. Hughes

Assistant Editor
Joanne O'Donnell

Editorial Assistant
Winifred L. Helfrich

Editorial Advisory Board
Brian W. Pollard
Ralph J. Preiss
Rex Rice

Contributing Editors
Richard Ahrons
A. S. Buchman
H. S. Miller
Harold H. Seward

Production Manager
Judy Lober

Advertising Production
Linda M. Wright

Art Director
James Flora

Technical Illustrator
Charles Manchester

Circulation Manager
Alma Brotherston

Marketing Manager
Geoffrey Knight, Jr.

Marketing Production
Megan Kern

Research Associate
Sidney Davis

Business Manager
David C. Ciommo

Vice President-Sales
Lindsay H. Caldwell

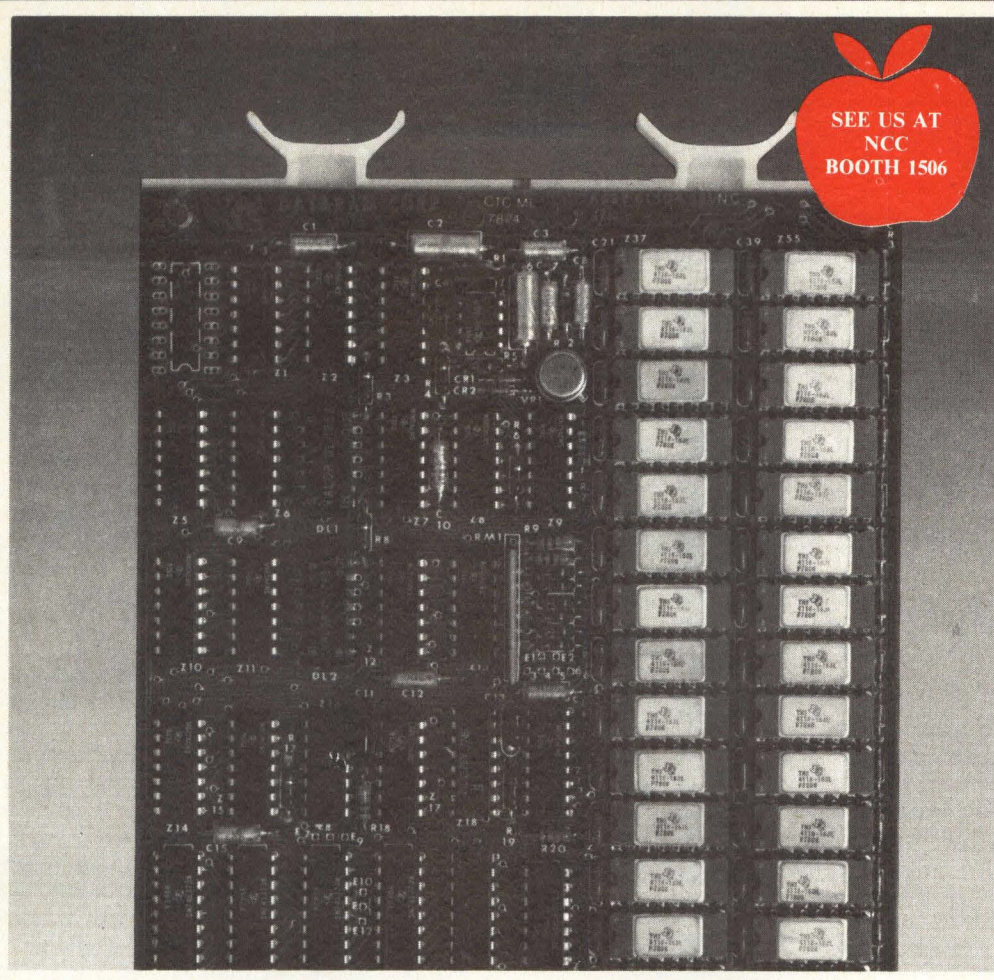
Editorial & Executive Offices
11 Goldsmith St
Littleton, MA 01460
Tel. (617) 486-8944
(617) 646-7872

Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

Computer Design is published monthly. Copyright 1979 by Computer Design Publishing Corporation. Controlled circulation postage paid at Pontiac, Ill. No material may be reprinted without permission. Postmaster: CHANGE OF ADDRESS—FORM 3579 to be sent to Computer Design, Circulation Dept., P.O. Box A, Winchester, MA 01890. Subscription rate is \$24.00 in U.S.A., Canada and Mexico, and \$40.00 elsewhere. Microfilm copies of Computer Design are available and may be purchased from University Microfilms, a Xerox Company, 300 N. Zeeb Rd, Ann Arbor, MI 48106.



SEE US AT
NCC
BOOTH 1506



32K x 18 LSI-11[®] ADD-IN

Dataram offers its newest idea in memory for LSI-11 microcomputers. 32K x 18 semiconductor ADD-IN memory that's right for your system. Right price. Right performance. Right now.

Using 4K or 16K semiconductor chips, Dataram's new LSI-11 ADD-IN covers the range from 8K x 16/18 to 32K x 16/18. And the system board outline conforms to DEC's standard dual-board size, enabling it to be used in either the LSI-11 or LSI-11/2.

Add to that such features as PDP[®]-11/03 compatibility, parity, on-board refresh, provision for battery back-up, Dataram's extensive burn-in and test, and full one-year warranty, and you'll see why this new semiconductor memory from Dataram is the right answer to your LSI-11 ADD-IN needs.

PLUS three more ways to enhance DEC's LSI-11

- 16K x 18 CORE ADD-IN
- 2.0 Megabyte BULK CORE Disk Emulation System
- 1.0 Megabyte BULK CORE MINI

DEC, PDP and LSI-11 are registered trademarks of Digital Equipment Corporation.

- Please send more information about Dataram memory for my LSI-11 microcomputer.
- Please send me information about your other LSI-11 compatible products.
- Please have a salesman contact me.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____ State _____ Zip _____



PRINCETON-HIGHTSTOWN ROAD CRANBURY, NEW JERSEY 08512
TEL:609-799-0071 TWX:510-685-2542

Canada: Ahern & Soper Ltd., Alberta, British Columbia, Ontario, Quebec • Finland: Systek OY, 90-737-233 • France: YREL, 956 81 42 • Italy: Mactronics Italia, 02/35 36 041 • Netherlands: Technitron b.v., 020-45 87 55 • Sweden: M. Stenhardt AB, (08) 739 00 50 • Switzerland: ADCOMP AG, 01/730 48 48 • United Kingdom/Ireland: Sintrom Ellinor Ltd., (0734) 85464 • West Germany/Austria: O.E.M.-Elektronik GmbH, 07 11-79 80 47 • Australia/New Zealand: Anderson Digital Equipment, (03) 543 2076 • India: Industrial Electronic Instruments, 79281 • Israel: K.D.M. Electronics, 921513 • Japan: Matsushita Electric Trading Co., Ltd., 03 (435) 4501 • Taiwan/Republic of China: Syscom Computer Engineering Co., (02) 7022156.

CIRCLE 5 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

I enjoyed the Nov 1978 article in *Computer Design* on "Breakpoint Design For Debugging Microprocessor Software" by T. P. Hughes and D. H. Sawin III (pp 99-107). Here at Weyerhaeuser headquarters, our main computer system is a Honeywell 66/60 which is a descendant of the GE 600 series.

On this Honeywell computer I use a software package which permits those features discussed in the article. The hardware has an instruction that transfers control to a fixed location which enables the debug monitor to assume control. The process is initiated via JCL control and the monitor allows dynamic breakpoints. Some associates and I have convinced ourselves that using breakpoint techniques is the best way to debug programs. Interestingly enough, we have not been able to convince others.

I am such a strong believer in this process that I have made extensive improvements to the standard vendor package. Specifically, I changed the module to suppress (on demand) the addition of an offset address (if one has been supplied) for any simple inquiry. This is very handy when debugging a module (the offset set to the load address of the module), but a reference must be made to a labeled common region. Normally in such circumstances the offset address would have to be set to zero,

display, then reset to the module load address.

The second major improvement allows displaying data via indirect reference capability. We find this very handy since our FORTRAN compiler is "pure procedure," eg, all references to arguments are via indirect pointers. In creating this capability, I was fortunate in that the hardware contains instructions for saving and restoring all user addressable registers at once, as well as instructions which develop addresses.

Shortly, I hope to begin using small computers such as those referred to in the article. Part of my selection criterion will be the availability of breakpoint processing. I have seen ads for circuit boards providing such capability. I would appreciate any thoughts on the subject.

David A. Young
Weyerhaeuser Co
Tacoma, Wash

The Author Replies:

We agree wholeheartedly with your assertion that using breakpoints is an extremely useful and powerful tool for debugging programs. In fact, we find it hard to consider debug of programs in the absence of such a capability. Likewise, it has been our experience that it is difficult to convince others of the value and convenience of this technique. We believe that one of the reasons for this

is the lack of general availability of debug monitors containing such a capability.

While there are many vendors who offer debug monitors, a large number of them have no breakpoint capability. Unfortunately, those that offer such capabilities often have implemented them in such a fashion that it is difficult, or unwieldy, to use. Many such "products" either do not run in real time or require the user to manage placement and removal of the breakpoints by manually inserting and removing code. Others rob the user of valuable processor resources, such as interrupt traps, or rely on the program under debug not to mess up critical resources, such as the stack pointer.

In summary, our feeling is that one must beware when purchasing a product with this capability. All may not be what it appears. There are monitors available which properly implement useful breakpoint facilities for most of the popular microprocessors. Unfortunately, some of these are available from rather obscure sources. We hesitate to recommend a particular one because the task of selection consists of making a large number of complex, inter-related tradeoffs.

T. P. Hughes
Consultant
South Orange, NJ

D. H. Sawin III
Foxboro Co
Foxboro, Mass

Interconnections driving you haywire?

See page 119

Letters to the Editor should be addressed:

Editor, Computer Design
11 Goldsmith St
Littleton, MA 01460

CORRECTION

On p 239 of the Nov 1978 issue, the "Cartridge Disc Controller" product item should state that the Xebec Systems Inc Quad™ "is a single 4-wide pc board."



When Joe Bruno heard we were famous for our custom work, he brought us his '57 Chevy.

Sorry Joe. It's custom MOS/LSI.

Chances are that in the fifties you were into custom cars too—who wasn't? But today you're designing systems, and custom means MOS/LSI.

If you're presently in production or breadboarding a system with discrete components and a batch of SSI and MSI integrated circuits, our high-density MOS processes will usually enable us to put your whole system on ONE CHIP at great cost savings. We've got high-voltage P-MOS technologies, as well as C-MOS capability. But, where we really shine is in our high-density n-channel silicon-gate COPLAMOS® technology, which virtually all our customers are now specifying for their high-performance, low-cost custom requirements. If you also need quick turn-around on mask-programmable options and

patterns, we can combine COPLAMOS® with our most recent technological breakthrough CLASP™ (which stands for COPLAMOS Last Stage Programmability) to provide the solution.

Standard Microsystems is a total-capability supplier—all design engineering, wafer processing, assembly, and test is performed in our modern, Hauppauge, New York facilities. Our processes are usually compatible with current state-of-the-art processes used throughout the industry. Not only can we start your design from scratch, but we can enter the custom cycle at any point. If you have masks, we can process wafers, generate test procedures, assemble devices and final test.

So, the next time you have a need in the custom area, just peel out to Standard Microsystems and tell 'em Joe sent ya.



STANDARD MICROSYSTEMS CORPORATION

35 Marcus Boulevard, Hauppauge, New York 11787 (516) 273-3100 TWX: 510-227-8898

The largest manufacturer of MOS/LSI data communication circuits

CIRCLE 6 ON INQUIRY CARD

INTRODUCING THE PERKIN-ELMER 3220

The Highest Performance Mini.

Full 32-bit architecture. DMA bandwidth of 8MBytes. MOS memory in 256KB modules with error correction as standard. Memory error logging down to the chip level, if you want. Memory expansion to 4MBytes. Cache memory, 128 32-bit registers, number-crunching features no 16-bit mini can match. And, all for less than a PDP-11/60.



The Lowest Cost Supermini.

Outstanding run-time speed and accuracy. Fast, responsive program development. Easy, cost-effective program conversion. Check the comparison chart.

Either Way, We've Got Them Beat.

	DEC 11/34	DEC 11/60	P-E 3220	SEL 32/57	PRIME 550
Architecture	16-bit	16-bit	32-bit	32-bit	32-bit
DMA Bandwidth	2MB	6MB	8MB	26MB	2.5MB
Maximum Memory	256KB	256KB	4MB	1.87MB	2MB
Number of Registers	8	16	128	8	128
Direct Addressing	56KB	56KB	4MB	.5MB	32MB (virtual)
Writable Control Store	No	Yes (opt.)	Yes (opt.)	Yes (opt.)	No
Shared Memory Support	No	No	Yes (opt.)	Yes (opt.)	No
Pricing - Processor 256KB, PF/AR, Systems Console, Chassis and Cabinet	\$29,700	\$41,900	\$33,500	\$41,600	\$70,000
256KB Expansion Memory	N/A	N/A	\$10,000	\$12,500	\$15,000

	Optimizer Technology	Average Compile Time	Whetstone Benchmark	Matrix Inversion Program	Binary Search	Price *
3220 FORTRAN VII	Global	2000 LPM	2.25 Sec.†	3300 Sec.†	39 Sec.†	\$ 88,600
VAX FORTRAN IV Plus	Block	1300 LPM	.85 Sec.	3700 Sec.	109 Sec.	\$167,200

*Both 3220 and VAX configured with: 512KB, Floating Point, 10MB Disk, Dual Density Tape, OS, FORTRAN.

†Without cache memory option.

Dynamic 32-Bit Software.

Perkin-Elmer 32-bit software is the best you can get. Tuned and proven where it counts. In the field. And not just for months. For years.

Powerful software like our FORTRAN VII, the only globally optimizing 32-bit FORTRAN compiler available on a supermini. It chops through tough, time-critical jobs with ease. And, it's targeted to ANSI FORTRAN-77 and IBM FORTRAN H compatibility to reduce conversion costs.

A flexible operating system for event-driven, real-time applications. Program development with up to 32 on-line, interactive terminals. The industry's most advanced transaction processing monitor, supporting commercial applications with up to 64 terminals, using COBOL and SORT/MERGE II.

Shareable software that allows our OS/32 MTM to make multi-terminal, multi-task program development a snap. And, increases memory efficiency as well.

From The People Who Invented The 32-Bit Supermini.

We introduced the first 32-bit supermini five years ago. Today, we have over 2,000 successful 32-bit installations worldwide. The Model 3220 is the first member of our new Series 3200 family, with more to come. Advanced systems and software that will keep Perkin-Elmer the undisputed leader in 32-bit performance and price.

Find out how we've got them beat any way you look at it. Call or write for a demonstration today. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757. (800) 631-2154. Or, in New Jersey (201) 229-6800.

PERKIN-ELMER

CIRCLE 7 ON INQUIRY CARD

CALENDAR

CONFERENCES

APR 1-4—Southeastcon, Hotel Roanoke, Roanoke, Va. INFORMATION: K. Reed Thompson, Rm 224, General Electric Co, 1501 Roanoke Blvd, Salem, VA 24153. Tel: (703) 387-7370

APR 3-5—Specifications of Reliable Software Conf, Hyatt Regency Hotel, Cambridge, Mass. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

APR 9-12—INTERFACE, McCormick Pl, Chicago, Ill. INFORMATION: Sheldon G. Adelson, President, Datacomm Interface, Inc, 160 Speen St, Framingham, MA 01701. Tel: (617) 879-4502

APR 17, 19, and MAY 8—Invitational Computer Conf, Dayton, Ohio; Chicago, Ill; and Denver, Colo. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

APR 23-25—Relay Conf, Stillwater, Okla. INFORMATION: Engineering Extension, Oklahoma State U, Stillwater, OK 74074. Tel: (405) 624-5146

APR 23-25—Sym on Computer Architecture, Marriott Hotel, Philadelphia, Pa. INFORMATION: Dr Barry Borgerson, Sperry Univac, PO Box 500, Blue Bell, PA 19422. Tel: (215) 542-1013

APR 24-26—Electro, New York Coliseum and Americana Hotel, New York, NY. INFORMATION: William C. Weber, Jr, General Mgr, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

APR 25-27—Modeling and Simulation Conf, Pittsburgh, Pa. INFORMATION: W. G. Vogt or M. H. Mickle, Modeling and Simulation Conf, 348 Benedum Engineering Hall, U of Pittsburgh, Pittsburgh, PA 15261

MAY 1-3—DATA Computer Show and Data Communications Conf, Toronto, Canada. INFORMATION: Kimberly Coffman, 2 Bloor St W, Suite 2504, Toronto, Ontario M4W 3E2, Canada

MAY 8-10—Society for Information Display Internat'l Sym, Chicago Marriott Hotel, Chicago, Ill. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: (305) 446-8193

MAY 15-17—Micro/Expo 79, Centre International de Paris, Paris, France. INFORMATION: Sybex, Inc, 2020 Milvia St, Berkeley, CA 94704. Tel: (415) 848-8233

MAY 15-17—National Aerospace and Electronics Conf, Dayton Convention Ctr, Dayton, Ohio. INFORMATION: NAECON, 140 E Monument Ave, Dayton, OH 45402. Tel: (513) 228-4121

MAY 15-18—Power Industry Computer Applications Conf, Bond Court Hotel, Cleveland, Ohio. INFORMATION: James R. Smercina, Cleveland Electric Illumination, PO Box 5000, Cleveland, OH 44101. Tel: (216) 623-1350, X3389

MAY 17—Trends and Applications: Advances in Systems Technology Sym, National Bureau of Standards, Gaithersburg, Md. INFORMATION: Trends and Applications, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAY 18-20—Mid-Atlantic Personal and Business Computer Show, National Guard Armory, Washington, DC. INFORMATION: Mid-Atlantic Expositions, Inc, PO Box 3315, Annapolis, MD 21403. Tel: (301) 263-8044

MAY 21-24—Sym on Incremental Motion Control Systems and Devices, Ramada Inn, Urbana, Ill. INFORMATION: Dr B. C. Kuo, PO Box 2772, Sta A, Champaign, IL 61820. Tel: (217) 333-4341

MAY 22-25—Internat'l Sym on Mini- and Microcomputers and their Applications, Zurich, Switzerland. INFORMATION: The Secretary, MIMI'79, PO Box 354, CH-8053 Zurich, Switzerland

JUNE 4-6—Machine Tool Forum, Pittsburgh Hilton, Pittsburgh, Pa. INFORMATION: J. Vincent Hanratty, Westinghouse Electric Corp, Westinghouse Bldg, Gateway Ctr, Pittsburgh, PA 15222. Tel: (412) 255-3693

JUNE 4-7—National Computer Conference, New York Coliseum, and Hilton and Americana Hotels, New York, NY. INFORMATION: Marjorie Greimel, American Federation of Information Processing Societies, 210 Summit Ave, Montvale, NJ 07645. Tel: (201) 391-9810

JUNE 11-13—Internat'l Conf on Communications, Sheraton Hotel, Boston, Mass. INFORMATION: Richard C. Stiles, Dir of Telecommunications Planning, GTE Labs Inc, 40 Sylvan Rd, Waltham, MA 02154. Tel: (617) 890-8460

JUNE 12-15—EDP USA '79: Computers and Peripheral Equipment, Milan, Italy. INFORMATION: Peter Ryan, U.S. Dept of Commerce, Industry and Trade Administration, Washington, DC 20230. Tel: (202) 377-2849

JUNE 17-20—Joint Automatic Control Conf, Hilton Hotel, Denver, Colo. INFORMATION: Prof T. F. Edgar, Program Chm, 1979 JACC, Dept of Chemical Engineering, U of Texas, Austin, TX 78712. Tel: (512) 471-3080

JUNE 20-22—Internat'l Sym on Fault-Tolerant Computing, Concourse Hotel, Madison, Wis. INFORMATION: Prof Charles R. Kime, Dept of Electrical and Computer Engineering, U of Wisconsin, Madison, WI 53706. Tel: (608) 262-0206

JUNE 25-27—Design Automation Conf, Town and Country Hotel, San Diego, Calif. INFORMATION: Robert J. Smith, III, Electrical Engineering Dept, U of Texas, PO Box 7728, Austin, TX 78712. Tel: (512) 471-4540

JUNE 25-29—Internat'l Sym on Information Theory, Grigano, Italy. INFORMATION: Prof M. Pursley, Dept of Electrical Engineering, U of Illinois, Urbana, IL 61801

SEMINARS

APR 10-12—Computer Aided Manufacturing Internat'l Robotics Sem, Royal Sonesta Hotel, New Orleans, La. INFORMATION: Gayle B. Clynch, Computer Aided Manufacturing-Internat'l, Inc, Suite 1107, 611 Ryan Plaza Dr, Arlington, TX 76011. Tel: (817) 265-5328

APR 23-27—PASCAL Programming for Mini- and Microcomputers, Ramada Inn, Woburn, Mass. INFORMATION: Prof Donald D. French, Institute for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: (617) 964-1412

MAY 23-25—IEEE Computer Society Afilomar Workshop on Microprocessors, Pacific Grove, Calif. INFORMATION: Ted Laliotis, Hewlett-Packard Labs, 3500 Deer Creek Rd, Palo Alto, CA 94304. Tel: (415) 494-1444

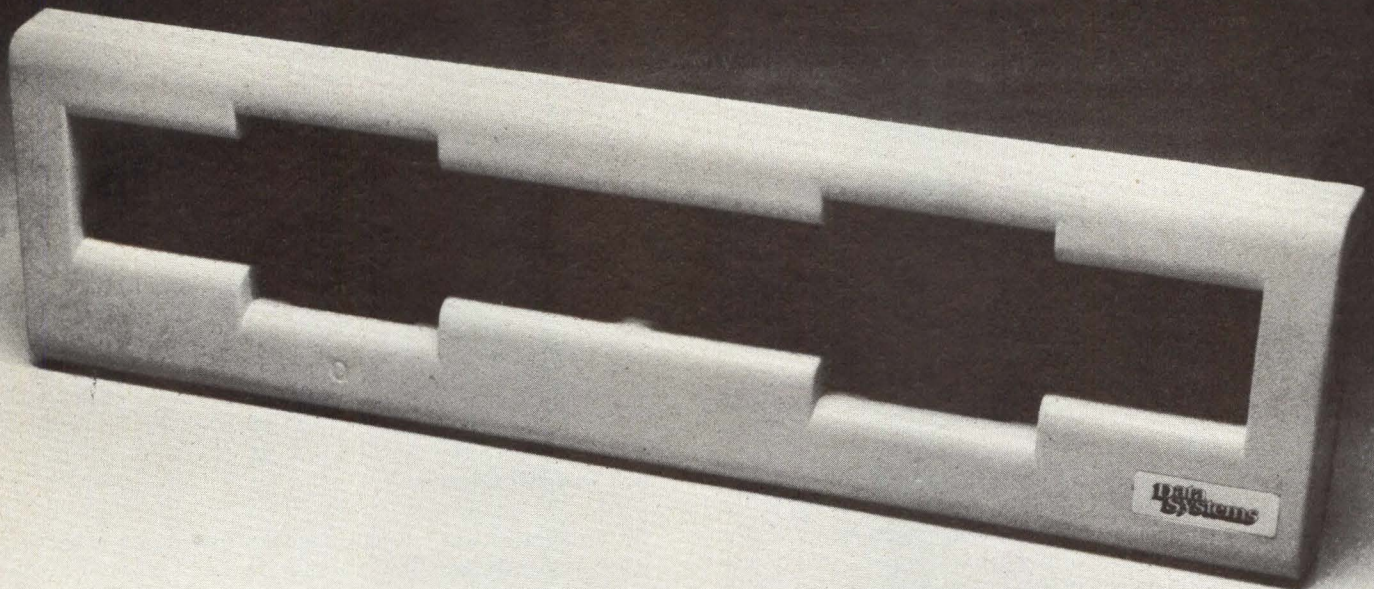
SHORT COURSES

APR 16-20—Data Communications Systems and Networks; and May 23-25—Microprocessors, Washington, DC; Washington, DC and Miami, Fla. INFORMATION: Continuing Engineering Education Program, The George Washington University, Washington, DC 20052. Tel: (202) 676-6106

JUNE 11-15—Machine Vision, Automatic Assembly, and Productivity Technology, Massachusetts Institute of Technology, Cambridge, Mass. INFORMATION: Dir of the Summer Session, Rm E19-356, MIT, Cambridge, MA 02139

Announcements intended for publication in this department of Computer Design must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.

INTRODUCING THE DSD 440. DOUBLE DENSITY, DELIVERED.



The DEC® RX02 – Compatible Flexible Disk System with 30 day delivery.

Our new DSD 440 records data in both DEC double density and IBM 3740 single density formats. It is 100% software, hardware and media compatible with DEC LSI-11, LSI-11/2, PDP-11 and PDP-8 computers including those equipped with extended memory. The DSD 440 can be set to emulate either the RX01 for downward compatibility or the RX02 for increased storage capacity and throughput.

Hardware Bootstrap

A 512-word hardware bootstrap is built into the interfaces for the PDP-11, LSI-11 and LSI-11/2 systems. In addition to bootstrapping both single and double density configurations, it also performs diagnostics on the CPU memory, and the disk interface and controller.

“Hyperdiagnostics”

Microprogrammed self-diagnostics are built into the drive and controller unit. User-selectable, stand-alone “Hyperdiagnostics” simplify maintenance and alignment procedures.

The DSD 440 data storage capabilities include write protection, power loss data protection, single track and complete diskette formatting. Diskettes can be formatted using sequential or user-selected sector interleaving. Special sector interleaving schemes can be implemented during formatting to improve system throughput.

Megabyte System

This powerful megabyte flexible disk system is packaged in a low profile 5¼-inch chassis.

The DSD 440 is being shipped in quantity now. Delivery is 30 days.

To find out more about it, contact Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

**Data
Systems**

3130 Coronado Drive, Santa Clara, CA 95051
(408) 249-9353 TWX: 910-338-0249

®Registered trademark of Digital Equipment Corporation

CIRCLE 8 ON INQUIRY CARD

DATA COMMUNICATIONS TESTING OVERVIEW— DIGITAL TESTING

Jeffrey R. Duerr

Hewlett-Packard Company, Delcon Division
Mountain View, California

The best way of determining how faithfully a system will transmit data is to feed data into it and evaluate the output. There are many cases where components of the system, modem, and carrier channel appear to be well within specification, yet the data transmission has a high error rate. On the other hand, sometimes a channel that appears to be hopelessly distorted will transmit perfectly good data. Because of these anomalies, bit error rate testing is needed to provide an overall indication of system performance.

BER Test Procedures

Bit error rate (BER) testing involves generating a known data sequence into the transmit modem, observing the receive sequence at the remote modem, and examining that sequence for errors. BER, expressed as the ratio of bits received in error to overall number of bits transmitted, will be an indication of end-to-end link performance. As an example, a typical voice-grade link might generate error rates in the order of 1 error in 10^5 bits.

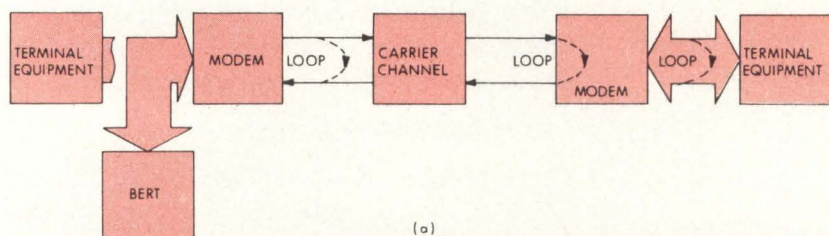


Fig 1(a) Looparound testing using one BERT

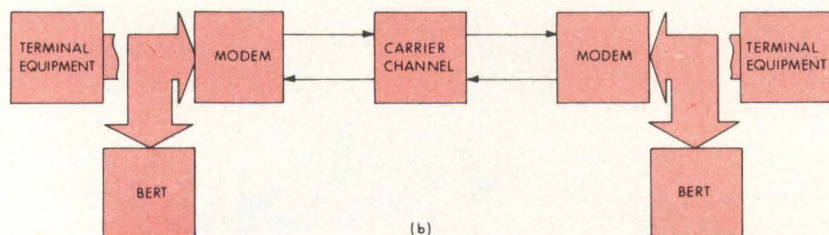


Fig 1(b) Application of two BERTs to full-duplex transmission system

Centronics. The Band Leader.



We're the leading OEM supplier of band printers. Over 100 OEM's have selected Centronics' 6000 Series Band Printers for use with their computer systems. That makes us the world's biggest supplier of band printers to the OEM market.

You can't beat the band for value. The reason we're the band leader is simple. In a word, it's value. Centronics' band printers cost up to 40% less than comparable printers. Yet they offer immediate availability, unsurpassed reliability, simple serviceability and over 85% spare parts commonality.

End users are hopping on our bandwagon. Another reason we're so big with OEM's is

customer choice. More and more end users select the Centronics' 6000 Series Band Printers for their systems. Small wonder, really. Centronics' 6000 Series Band Printers are unmatched for operational flexibility, print quality, upward compatibility, easy economical operation. And, Centronics offers more service capability worldwide than any other printer manufacturer.

Strike up the band. Price. Performance. Availability. And service. That's a combination that's hard to beat. Isn't it time you joined the bandwagon? For information, write or call: Centronics Data Computer Corp., Hudson, NH 03051, (603) 883-0111.

CENTRONICS®
The Band Leader

CIRCLE 9 ON INQUIRY CARD

Ideally, the actual transmitted test sequence should properly exercise the circuitry along the transmission path. While a simple alternating "1"- "0" pattern will provide error rate data, it is hardly representative of random data transmission. Pseudorandom bit sequences (PRBSS), although predictable, are of more practical value. They have all the appearance in the data domain of random digital data. These sequences, generated in repeating lengths of 2^n-1 bits, will generate all but one possible word combinations of bit length n . The most common sequences used in BER testing are 511 and 2047 bits long, representing $n = 9$ and $n = 11$, respectively.

Synchronous modems (generally those used above 1800 bits/s), typically employ clock recovery phase-locked loops at the receive end to regenerate a phase-coherent clock. Timing circuits such as this in the transmission path use the transition edges of the incoming data as a phase reference. This causes a slight frequency drift during long strings of 0 or 1 bits. To test for the resultant jitter in these timing circuits, some bit error rate testers (BERTs), such as the HP1645A, provide extremely long PRBSS of $2^{20}-1$ (over 1M bits) which provide in that data stream 20-bit word lengths. This long sequence, without transitions, is ideal for worst case testing of bit synchronization.

Beyond the BER Horizon

Modern BERTs do more than merely count errors. As data link requirements develop in sophistication, more measurements are needed to define problem areas adequately. Properly carried out, these additional measurements are all performed simultaneously, so that a total profile of system performance at any given time can be obtained. These measurements are block error rate (BKER), carrier loss, clock slip, skew, jitter, and total peak distortion.

BKER indicates first order statistical distribution of bit errors. It is obtained by dividing the received bit stream into block lengths, and determining the ratio of error-free blocks to blocks transmitted. This measurement is particularly effective in determining information throughput on a system containing block error recognition. Such systems ordinarily respond to the transmitter with a request to retransmit a block recognized as containing errors. BKER would, therefore, be an indication of the frequency with which these retransmissions would have to occur. A BER with errors grouped in bursts would affect fewer blocks, and consequently would give a lower BKER than an equivalent BER with errors in an even distribution across the data stream.

Carrier loss counting indicates how many times the signal was actually lost at the receiver. In a conventional switched telephone network, carrier loss can occur when data routing is changed during actual transmission. This phenomenon will be discussed in greater detail under "Analog Measurements" to be presented in the next issue.

Clock slips occurring at a high rate indicate that the receiver has experienced a jump forward or backward in the received data stream of one or more bits. This is a strong clue to look to the channel for problems when using an asynchronous modem. As switching occurs in order to create different routes for the carrier channel, more or less delay can be experienced in the new route, causing a time jump in the received message. With a synchronous system, the timing recovery circuitry in the modem, as well as disturbances in the channel, should be suspected.

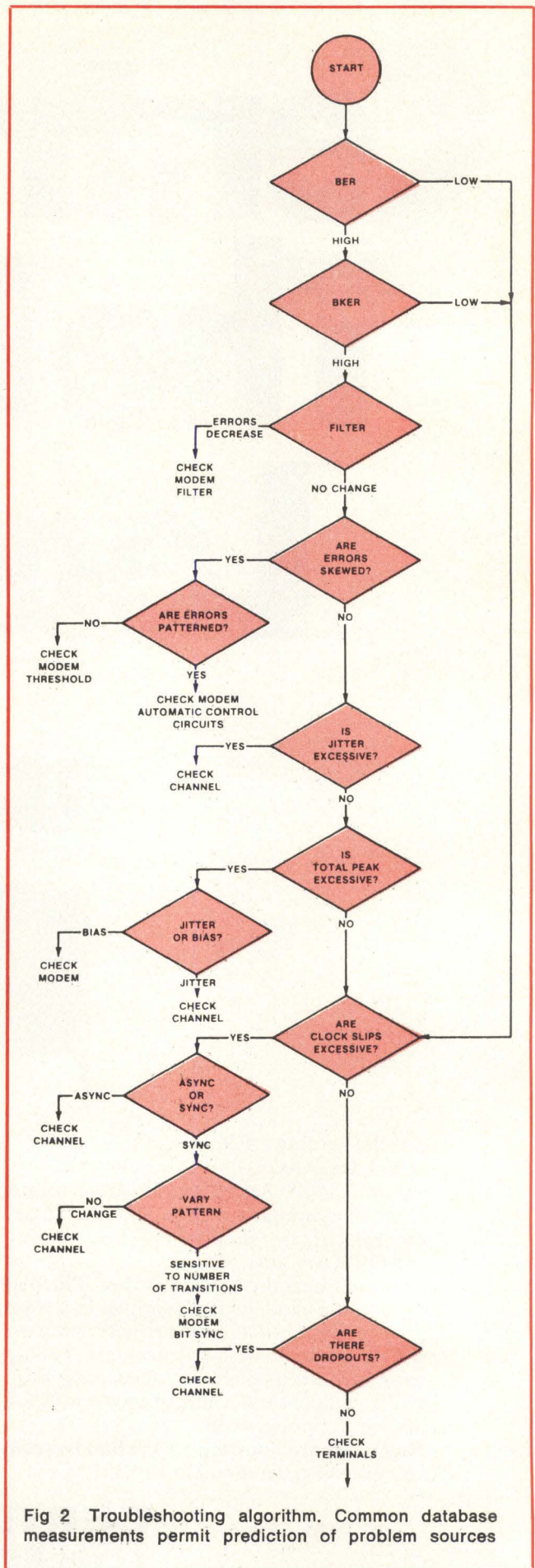


Fig 2 Troubleshooting algorithm. Common database measurements permit prediction of problem sources

By **SESCO**...
it works!



The Cook-able Computer

Introducing a ruggedized version of Intel's iSBC* 80/10A Single Board Computer

From Cryogenics to Hades

Our ruggedized SECS 80/10A likes it hot — or cold. It shrugs off shock, vibration, moisture. And thrives on dust, dirt and grime.

Meets MIL-E-5400, 16400, 4158 — and more. This makes our SECS 80/10A perfect for military systems and tough industrial applications — petroleum, steel, oceanography, communications.

In fact, anywhere a rugged microcomputer is needed.

Functional counterpart of Intel iSBC 80/10A

Exclusively licensed by Intel, our SECS (Severe Environment Computer System) is a functional counterpart of the standard iSBC 80/10A board. Even uses the same development system software.

*Trademark of Intel Corporation

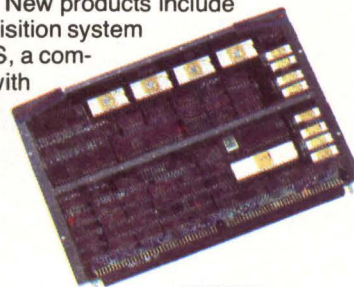
The difference is in the packaging

Our SECS 80/10A, which uses rugged Intel 883B chips, is mounted on a 9" by 6" shock and vibration resistant, full ATR compatible board. Conduction cooled, it operates from -55°C to +85°C. Add our numerous support modules and you end up with a versatile severe environment microcomputer system at a fraction of the development cost.

Other SESCO products

We also have a complete line of MIL SPEC core and semiconductor memories. New products include D-DAS, a digital data acquisition system for the 1553 bus, and SETS, a compact digital tape recorder with 23 megabit capacity.

When you're faced with a tough environment, "buy SESCO... it works!"



SECS 80/10A

EMM SESCO

Severe Environment Systems Company

A Subsidiary of Electronic Memories & Magnetics Corporation

20630 Plummer Street • P.O. Box 668 • Chatsworth California 91311
Telephone: (213) 998-9090 • Telex: 69-1404

CIRCLE 10 ON INQUIRY CARD

The intelligent disk architecture is available in STC

STC's new 2700 winchester disk family combines the intelligence of a microprocessor, 64k bytes of RAM, and a high-speed bus interface to offer you a versatile new disk architecture. An architecture that can help you achieve new dimensions in system speed and performance. Relieve CPU overhead burdens. Slash interfacing costs, and more.

Yet even without its advanced architecture, you'd still choose the 2700 disk family for its attractive price/performance and reliability values.

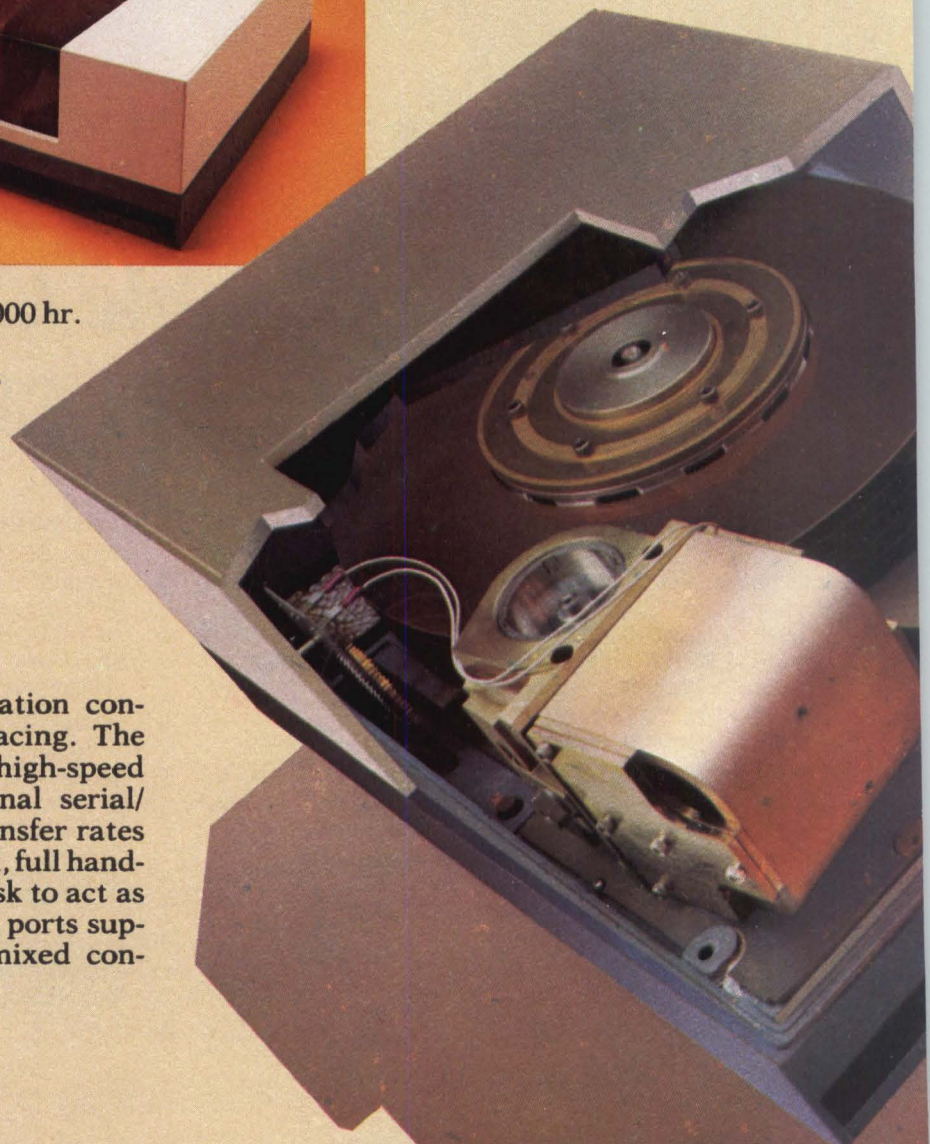
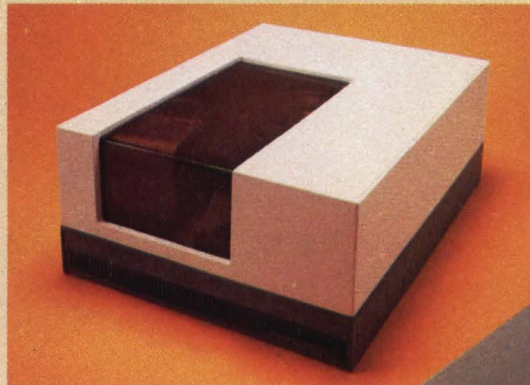
The 2700 family features formatted capacities of 39, 93, and 200 Mbytes, 25 msec average seek time, and OEM prices ranging from less than \$3,600* (39 Mbyte) to less than \$5,000* (200 Mbyte). With an 8000 hr. continuous operation MTBF, the 2700 will not just keep your customers happy, it'll keep your warranty expenses low.

*Domestic USA OEM prices in quantities of 100.

Powerful bus architecture for faster data rates and greater flexibility.

Gone are the speed and configuration constraints of serial, data-line interfacing. The 2700 disk family incorporates a high-speed byte-parallel interface, with internal serial/parallel conversion, to give you transfer rates up to 2 Mbytes/sec. The bidirectional, full handshake protocol permits any 2700 disk to act as master or slave, while built-in dual ports support radial, daisy chain or intermixed configurations.

Most important to you, the 2700 architecture offers maximum flexibility for applying these features. For instance, the architecture, coupled with the RAM buffer, permits continuous data transfer on both ports simultaneously. Thus your CPU can communicate with a 2700 on one port while disk-to-disk communication occurs on the other.



you'll need tomorrow Disks today.

The μ P can unlock your system's hidden resources.

One way to boost your CPU's performance is to get it out from under system overhead and back to productive computing. The on-board intelligence of the 2700 gives you that capability. Routines such as drivers, data management and utilities can be offloaded to the microprocessor, freeing the CPU and bus for other tasks. But that's just the beginning.

For example, you can use the microprocessor to optimize throughput by means of zero millisecond writes and caching algorithms to speed read access.

High-level software, including on-board editor and compiler, simplifies algorithm development for the above and other custom applications. And you can use the built-in RS-232 port to program right on the disk.

An intelligent controller in each drive. For free.

To help you get to the system level faster and easier, we placed 80% of the traditional controller functions within the 2700. Including all device dependent functions. Since you now only have to build a low-cost interface adapter—not a complete controller—your attachment costs are significantly reduced.

Low cost of ownership.

Fewer parts mean fewer failures. So the 2700 contains a minimum number of mechanical parts, only two of which move: spindle and actuator. The microprocessor contributes to this simplicity by replacing all sequencing and servo logic with firmware.

To eliminate scheduled maintenance, the 2700 dispenses with potentiometers. Dynamic adjustments are made internally under microprocessor control. And the 2700's closed loop air system means no filter changes.

If there's ever a failure, internal diagnostics isolate the problem to one of three sub-assemblies: logic board, head/disk assembly or power system. And these components uncouple quickly for fast repair.

All of this translates into high MTBF, low MTTR, to reduce your warranty and field service costs.

To learn more . . .

about tomorrow's disk architecture, today, contact Frank Gunn, Storage Technology Corporation, P.O. Box 6, Louisville, Colorado 80027. Or phone (303) 497-6037. In Canada: Ron Reardon, STC Ltd., 272 Galaxy Blvd., Rexdale/Toronto, Ontario M9W 5R8. Phone (416) 675-3350.

CIRCLE 11 ON INQUIRY CARD



STORAGE TECHNOLOGY CORPORATION

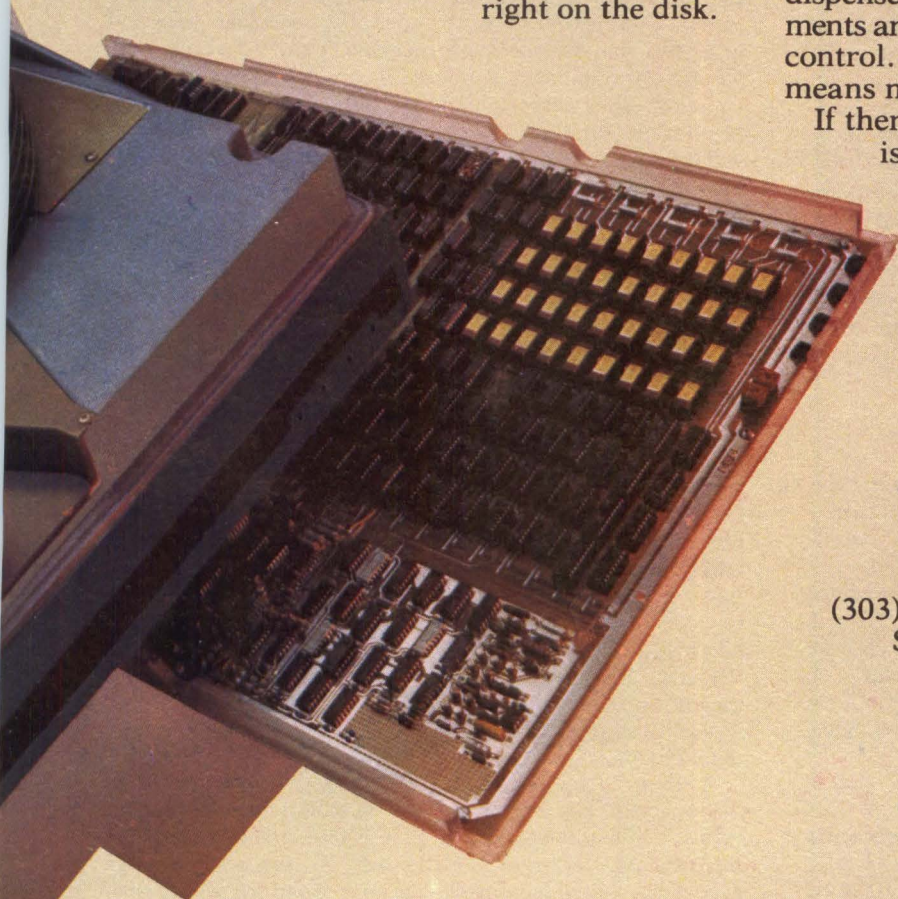




Fig 3 BER test setup. Test instrument HP1645A has been set to proper clock frequency and has completed proper handshake signals to accomplish transmission

Skew is a measure of the direction of received errors, ie, the percentage of total errors that were caused by 1s being mistaken for 0s. This should be approximately 50% in a fully random process. If the reading is consistently other than 50%, one would suspect either that the errors were somehow synchronous with the data and thereby caused by specific patterns, or that threshold circuits within the channel or modem were consistently favoring either 0s or 1s.

The remaining two measurements are related to the system's timing fidelity. Jitter, measured in asynchronous systems, is an indication of the short-term movement of data edges with respect to a stable clock reference. Total peak distortion combines jitter with any variation in the length of 1s vs length of 0s received, to give a total timing distortion measurement.

BERTs sometimes include a capability to easily insert filtering at the receive modem output. Any changes in error rate as a result of adding this filtering would point to less than optimum filtering in the asynchronous modem itself.

Testing Configurations

There are several test setups that can be used with the digital test instrument. Fig 1(a) shows the application of a BERT for evaluation in loop mode of the overall data communication system. By successively looping the transmitted test message at the output of the local modem, and, for full-duplex systems, at the input to the distant modem, and finally at the digital side of the distant modem, one can progressively test the performance of each element of the data transmission system. Implicit for completeness in this test is that the BERT itself have provision for a looparound in self-test.

While many channel disturbances are additive, and a good looparound test result is indicative of good one-way performance, one BERT cannot be used to isolate problems in a specific transmission direction in full duplex. For a complete analysis of half-duplex systems as well as more detailed analysis of full-duplex systems, BERTs should be placed at each end of the link to measure discrepancies in one direction at a time as shown in Fig 1(b).

Assuming that one can make all these measurements on a data transmission system, how are the results compared and how is the finger-pointing problem alleviated? The algorithm of Fig 2 delineates a process for combining these measurements into an effective diagnosis of system deficiencies. Although by no means exhaustive, the method demonstrates an orderly way to combine tested parameters so as to identify particular areas of weakness in overall performance. This approach will identify a significant number of problems directly, and in many other cases will define the next level of test to be carried out.

Two remaining sources of bad performance not yet mentioned are the terminal itself and the interface from terminal to modem. Under the error rate test method, terminal performance problems are isolated by first ensuring good performance in the modem/channel combination. More specific active tests on the terminal were described under Protocol Testing.*

The RS-232-C interface is the most widely used interface for terminal-to-modem data transmission. To be more flexible and to have the capacity to adapt to future needs, a BERT should be able to be easily adapted to other interface standards. The RS-232-C contains control signals between terminal and modem, as well as data timing signals. Operation of these control and status indicators is important for error-free data transfer. In addition to displaying the status of the modem indicator lines, a good error rate tester must send control signals to that modem. Also, more sophisticated testers will allow testing of turnaround times, such as the time between a "Request to Send" from terminal to modem and the return of a "Clear to Send" from modem to terminal. These turnaround times are a direct indication of the data channel availability.

A typical BER test setup is shown in Fig 3. Here the operator has connected the RS-232-C interface cable between the test set and a Bell 1200-bit/s asynchronous modem. At this point in the test, an error rate of 84×10^{-5} has been measured. This information, along with other measured parameters, leads to an analysis of overall transmission capability.

**Computer Design*, Feb 1979, p 10





A man in a dark suit and tie stands in a warehouse, leaning on a metal cart. He is looking towards the camera with a slight smile. The background shows stacks of boxes and a bright light source from a window or doorway.

A large, rectangular electronic device, possibly a VCR or stereo component, sits on a wooden pallet. The device has a control panel with several buttons and a small display. The brand name 'REMEX' is visible on the right side of the device.

Stacks of cardboard boxes are visible in the background. Some boxes have the 'REMEX' logo and the text 'FRAGILE - GLASS' and 'EXCELLO COMPANY' printed on them. A single light fixture hangs from the ceiling, illuminating the scene.

Introducing the Data Warehouse.

Winchester disk plus floppy copy.

Big for its size.

Calling it a "warehouse" may sound like an exaggeration.

But in spite of its mini/micro size, there's room inside for 20 megabytes of fixed Winchester-disk storage with reliability sealed in.

And there's room for one or two of Remex' flexible disk drives, as well. So you can quickly transfer up to 2.5 megabytes at a time from temporary storage to permanent.

High level protocol.

Like any warehouse, it has a front office — our highly intelligent, embedded formatter. This state-of-the-art, 6800-based unit features Channel Command Control, making the Data Warehouse one of the first mini/micro disk memory systems to incorporate a high-level protocol.

40% faster throughput.

Channel Command Control gives you direct memory access, reducing communications with the computer to the extent that throughput is increased 40

percent. It also permits transfer of up to 64,000 words by a single command. And there's a built-in 2K word buffer to provide a constant transfer rate under varying CPU conditions.

Off-line copying.

Data contained on the fixed disk can be copied onto the floppy(s) off-line, without slowing CPU activity at all.

We've packed a lot of unique capabilities, along with a power supply, into a single package that provides big, reliable mass memory performance for minis and micros at an unheard-of price.

Calling it a "warehouse" may be an understatement.

Call us today for full details.
Ex-Cell-O Corporation, Remex Division,
1733 E. Alton St., P.O. Box C19533,
Irvine, CA 92713. Phone: 714/557-6860.
TWX: 910/595-1715.

Ex-Cell-O Corporation

REMEX DIVISION

Paper isn't the only thing we look good on.

CIRCLE 12 ON INQUIRY CARD



Funds Transfer System Integrates Communications With Internal Bank Procedures

RFS (Rockwell Financial System) which automates a bank's commercial funds transfer internal operation and interfaces with wire services has been announced by Rockwell International, Commercial Telecommunications Group, PO Box 10462, Dallas, TX 75207. RFS is available in three standard versions, RFS-100 for banks with peak transaction rates of 300/h, RFS-200 with 3000/h, and RFS-400 for rates of 9000/h. Direct computer interfaces to Fedwire, Bank-Wire II, CHIPS (Clearing House Interbank Payment System), and SWIFT (Society for Worldwide Interbank Financial Transactions) financial wire services are offered. Interfaces for other switched networks such as Telex and TWX are also available.

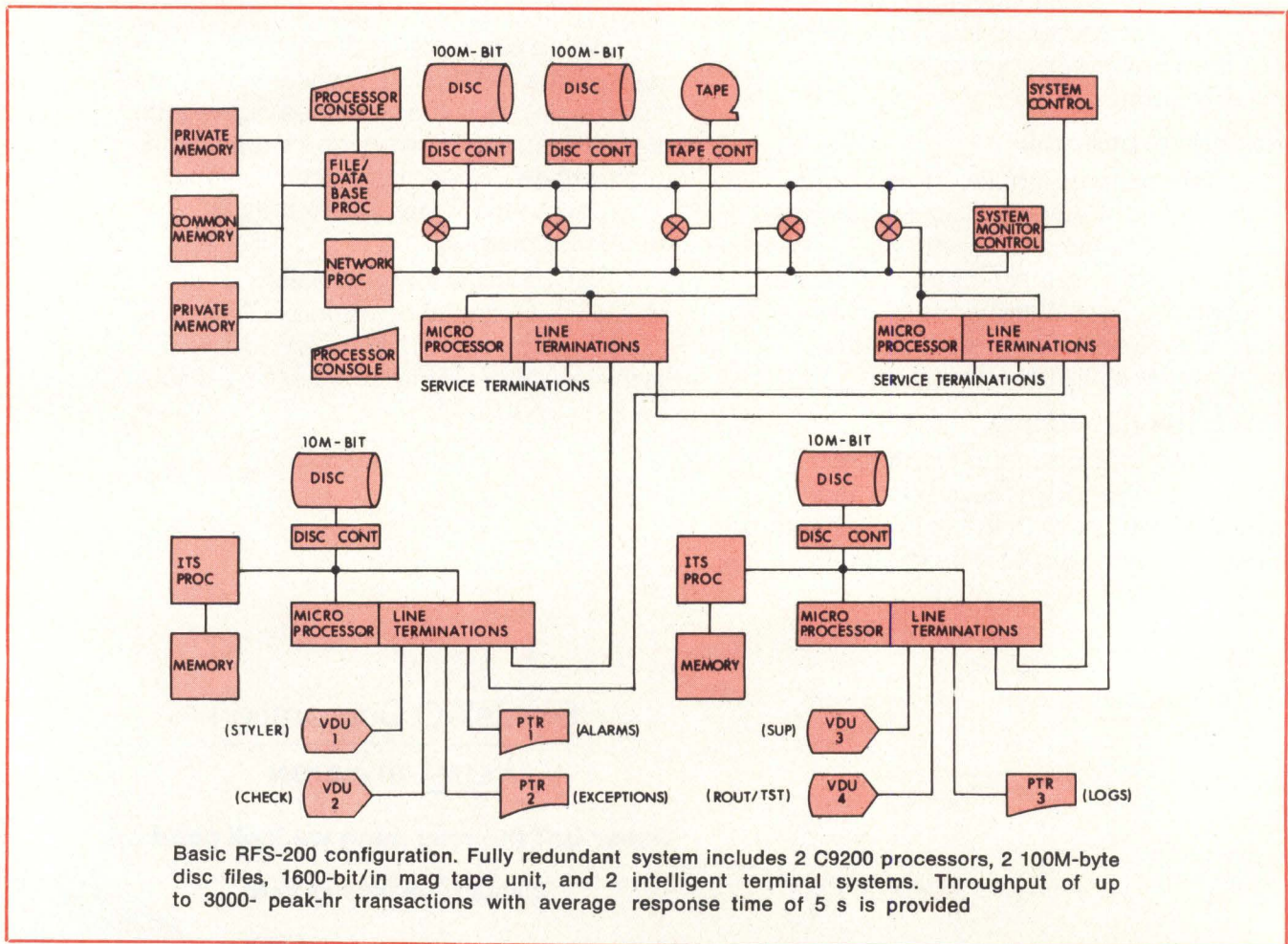
RFS equipment includes one or more C9200 processors and a com-

plement of disc files and mag tape units. Multiple video display terminals and printers are standard system equipment. RFS-400, the largest system, has two sets of dual processors with 1.5M bytes of memory and up to 10 intelligent terminal subsystems. Intermediate RFS-200 uses one set of dual processors and up to four intelligent terminal subsystems. The dual processors operate in a shared-load mode with mutual access to buffers and tables in common memory. In a recovery from failure situation, either processor assumes the entire traffic workload. The terminal subsystems control the video display units and handle display formats at the local level. RFS-100, smallest in the line, uses a single processor with hardcopy printouts on all traffic. Wire service

interfaces for Telex and TWX are hardware dial units. Line handlers for the other wire services are programmed in microprocessors.

The C9200 CPU is a 4-board processor mapped to allow addressing of up to 4M bytes of memory. Operating system software supports key features of the high level language compiler. The communications oriented language, similar to PL/I, supports a multiprocessor, multitask environment, and uniform calling sequences. Key database information and tables are afforded protection by the compiler, which exercises special controls with respect to data usage, allocation, and sharing.

Integrating the bank's communications over the various wire services with the bank's internal transaction and routing procedures, the company says, results in a high degree of automation and an orderly work flow for processing funds transfer functions.



Circle 400 on Inquiry Card

DEC PDP-11 TAPE USERS NO WAITING . . .

For the first embedded single board Magnetic Tape System Controller

Datum's new PDP-11 software compatible single board design, Model 1520 Embedded NRZI Tape Controller offers you more for less. And we're delivering them right now.

More versatility; occupies single HEX SPC slot or comes with its own chassis, 16 bit microprocessor controlled, word and or byte memory transfers with odd or even starting addresses and byte counts, TM-11 compatible, attaches to the Datum D450 tape drive or any industry standard tape drive (up to four can be attached). **More flexibility** of configuration-controls any

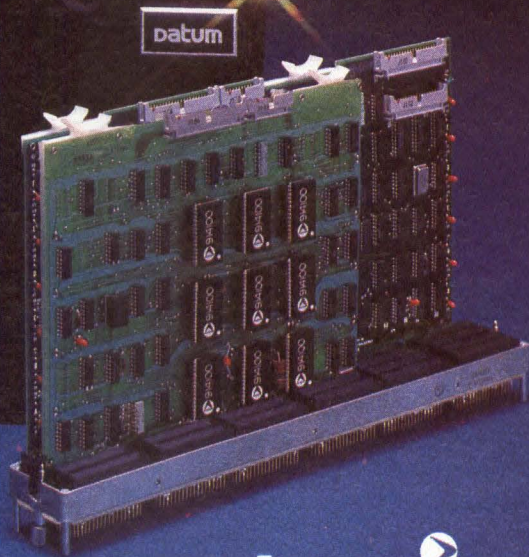
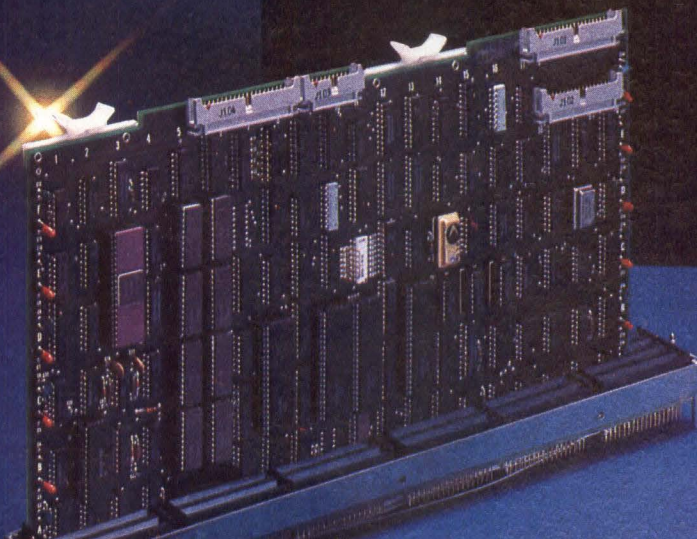
combination of speed and density. Dual Density is achieved simply by adding a second board to accommodate the Phase Encoded function.

And we offer you **less;** less initial cost*, less preventative maintenance. And you use less space thanks to Datum's advanced embedded controller design.

If you're a PDP-11 tape user and need delivery now, you owe it to yourself to learn more about Datum's more for less tape program. **For early delivery contact your local Datum representative today.**



**PDP-11
SOFTWARE
COMPATIBLE**

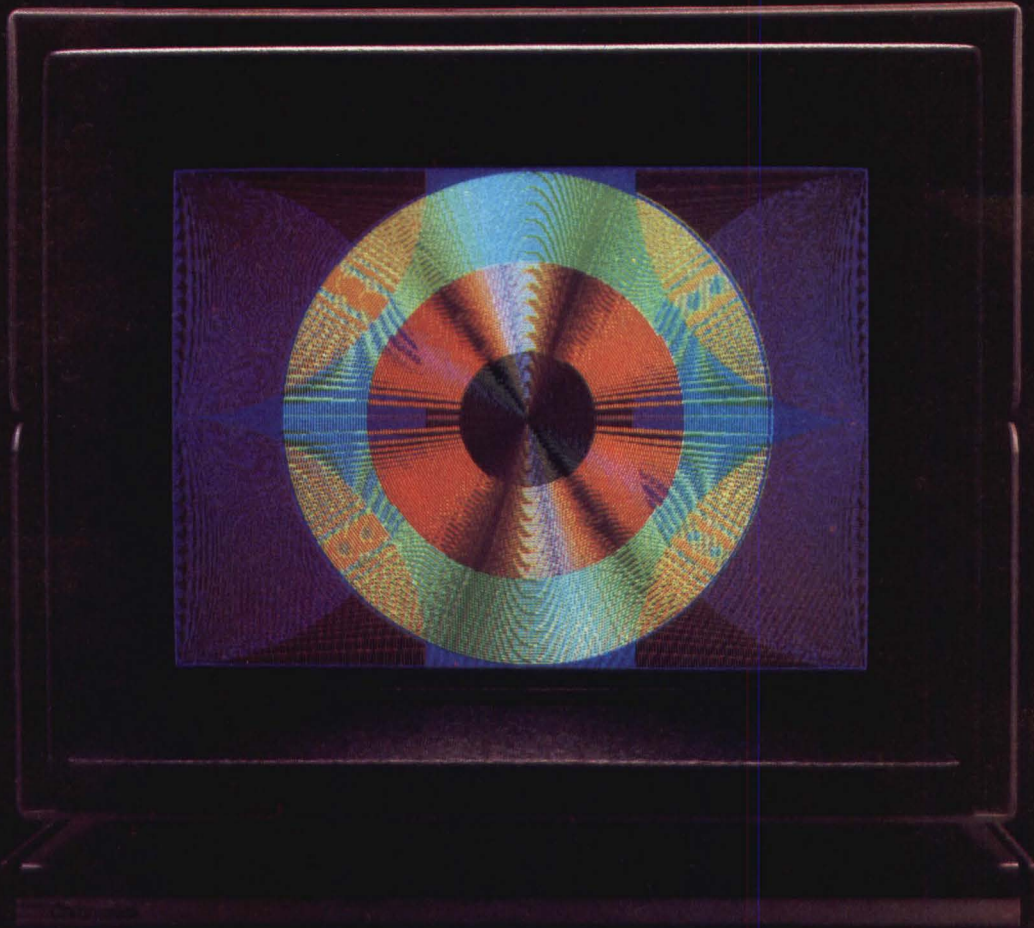


datum inc

CORPORATE HEADQUARTERS 1363 S. State College Blvd., Anaheim, CA 92806, Tel: 714/533-6333, TWX: 910/592-1289, Telex 68-5579 • **EUROPEAN HEADQUARTERS, DATUM (ELECTRONICS) LTD.,** DATUM House, Harlington, Middlesex, England, Tel: 01-897-0456, Telex: 935-398 • **DATUM SALES OFFICES, CANADA,** Willowdale, Ontario, Tel: 416/491-6960, Telex: 06-966857 **EOR TOR: MOUNTAIN STATES,** Denver Colorado 80232, Tel: 303/693-3414; **EAST COAST,** Mountainside, New Jersey 07092, Tel: 201/654-5590; **MIDWEST,** Des Plaines, Illinois 60018, Tel: 312/296-1064; **SAN JOSE,** San Jose, CA 95117, Tel: 408/249-5370; **NEW ENGLAND,** Framingham, MA 01701, Tel: 617/872-6911

*Single board NRZI design, \$3,000 Qty-1
PPD 103

Systems pricing begins at \$6,900 Qty-1



HERE'S AN INCREDIBLY BRIGHT IDEA FOR YOUR NEXT SYSTEM.

At Chromatics, one of our most important corporate goals is to stay ahead of our competition — with more innovations, more reliable products and more personalized service.

The result of our efforts is the CG SERIES of color graphic computers that start at \$5995 for a complete usable system with color monitor.

Enter your artwork and graphics quickly with our X-Y digitizer tablet and store them on our floppy disk peripherals. Analyze and operate on your results with our Microsoft[®] Z-80 BASIC soft-

ware and our graphics packages.

Viewability is enhanced with our multi-hue pattern fill routines, and the operator can Zoom in on the fine detail of a 512 by 512 high resolution color screen. And, for a permanent full-color record, you can even output the final results to a Xerox[®] 6500 color copier with our color hard copy interface.

In addition, our unified approach creates a powerful Z-80 development system with Assembler, Text Editor and Disk Operating System with operation in full color.

We're so confident of our color graphic computers that we back them with a full year's warranty instead of the usual ninety days or six months. If you should have a problem, we have a strict policy of giving customers the fastest possible turn-around time on repair service.

Watch out for us. We're determined to meet our corporate goal of staying out in front of everybody else. Way out in front.

Chromatics, Inc., 3923 Oakcliff Industrial Court, Atlanta, Georgia 30340; tel: 404/447-8797; TWX: 810/766-4516.

Chromatics
The World's Most Colorful Computer Company.

Sales Representatives USA

Alabama: Huntsville
Col-Ins-Co. 800/327-6600

Arizona: Phoenix
Thorson Co. 602/956-5300

California: Irvine
Thorson Co. 714/557-4460

California: Los Angeles
Thorson Co. 213/476-1241

California: Mountain View/S.F.
Thorson Co. 415/964-9300

California: San Diego
Thorson Co. 714/292-8525

California: Santa Barbara
Thorson Co. 805/964-8751

Colorado: Denver
Thorson Co. 303/759-0809

Connecticut
Bartlett Associates 914/949-6476

Delaware
Bartlett Associates 301/656-3061

District of Columbia
Bartlett Associates 301/656-3061

Florida: Ft. Lauderdale
Col-Ins-Co. 800/432-4480

Florida: Orlando
Col-Ins-Co. Inside Fla.
800/432-4480

Local 305/423-7615

Georgia: Atlanta
Col-Ins-Co. 800/327-6600

Hawaii: Honolulu
Thorson Co. 808/524-8634

Illinois
Resource Data Systems
312/564-5440

Indiana
Resource Data Systems
312/564-5440

Iowa (Eastern)
Resource Data Systems
312/564-5440

Iowa (Western)
Professional Marketing Services
612/474-5939

Louisiana: Baton Rouge
Col-Ins-Co. 800/327-6600

Maine
Bartlett Associates 617/879-7530

Maryland: Bethesda
Bartlett Associates 301/656-3061

Massachusetts: Framingham
Bartlett Associates 617/879-7530

Michigan: Detroit
WKM Associates 313/588-2300

Minnesota
Professional Marketing Services
612/474-5939

New Hampshire
Bartlett Associates 617/879-7530

New Jersey
Bartlett Associates 914/949-6476

New Mexico: Albuquerque
Thorson Co. 505/265-5655

New York: Holcomb
Bartlett Associates 716/657-6309

New York: White Plains
Bartlett Associates 914/949-6476

North Carolina: Winston-Salem
Col-Ins-Co. 800/327-6600

Ohio: Cleveland
WKM Associates 216/267-0445

Ohio: Dayton
WKM Associates 513/434-7500

Oregon: Portland
Thorson Co. 503/620-5800

Pennsylvania: Pittsburgh
WKM Associates 412/892-2953

Pennsylvania: Wayne
Bartlett Associates 215/688-7325

Rhode Island
Bartlett Associates 617/879-7530

South Carolina: Greenville
Col-Ins-Co. 800/327-6600

Texas: Austin
Thorson Co. 512/451-7527

Texas: Dallas
Thorson Co. 214/233-5744

Texas: Houston
Thorson Co. 713/771-3504

Utah: Salt Lake City
Thorson Co. 801/973-7969

Vermont
Bartlett Associates 617/879-7530

Virginia (Northern)
Bartlett Associates 301/656-3061

Virginia (Southern)
Col-Ins-Co. 800/327-6600

Washington: Seattle
Thorson Co. 206/455-9180

Wisconsin
Resource Data Systems
312/564-5440

Any other states
404/447-8797

Europe & Near East
Techexport, Inc. 617/661-9424

Far East
Computers International
213/382-1107

FOREIGN COUNTRIES
Australia: Crows Nest, NSW
TCG 439-6477

France
Techdata 749-40-37

Japan: Tokyo
Computers International Japan
03/402-8596

Scandinavia: Sweden
Teleinstrument AB 08-380-370

South Africa: Pretoria
Infodata Pty. Ltd. 01278-8141

Switzerland
W. Stolz AG 057-54655

United Kingdom: Bournemouth
Techex Ltd. 0202-293-115

Belgium: Brussels
Spesi
(02) 37491-12

Software Modules Lend Flexibility to Dispersed Data Processing Systems

Recent announcement of four mini-computer systems (see this issue, "Digital Technology Review," pp 63-64) by Prime Computer, Inc, 40 Walnut St, Wellesley Hills, MA 02181 was accompanied by the introduction of Primenet™ network communication capability for dispersed and local systems. In the former, the systems may communicate among themselves, with other vendors' systems, and with terminals over packet switched X.25 compatible networks. In local networks, users may connect physically adjacent computers via a high bandwidth multipoint loop configuration.

Software modules provide a distinct set of functions. Interprogram communication facility (IPCF) allows full duplex communication between programs residing on one or more computers at one or more locations. Users have the flexibility to share

with other systems or to divide the execution load among multiple processors. Interactive terminal support (ITS) facility permits a program under Primos[®] operating system to communicate with terminals attached to other company systems or to a packet switched network. In both cases, terminal messages enter the system through a single synchronous port which is multiplexed by ITS software in a manner transparent to the terminal user and application programmer. File access manager (FAM) facility permits network users to read and write files on other systems in the network without regard to physical location or structure. When a request to locate a file or directory cannot be handled locally, FAM is applied to find the data elsewhere in the network. The same level of security and access control is applied to files accessed through the network as is furnished for files accessed locally.

Remote job entry emulation packages support IBM 2780 and HASP,

Control Data 200UT, UNIVAC 1004, and ICL 7020. Distributed processing terminal executive (DPTX) conforms to protocols used by IBM 3271/3277 display systems.

Circle 401 on Inquiry Card

Fiber Optic Cables Get New Trademark

The data communications fiber optic cable line called PFX is now known as "Pifax" according to a recent announcement by the DuPont Co, Wilmington, DE 19898. Pifax cables are designed for short and medium runs of less than 1 km, are reinforced with Kevlar 49 aramid fibers in a protective jacket of Hytel polyester elastomer, and offer large diameter cores and numerical aperture, hard cladding, and easy connection.

The product line includes Pifax P-140 and P-240 single- and dual-channel polymethyl methacrylate core cables clad in a proprietary hard polymer; Pifax PIR-140 single-channel infrared transmitting all-plastic cable; and Pifax S-120 and S-220 single- and dual-channel plastic clad silica fiber optic cables, said to be the most rugged and easily connectable cable of this type now available.

DELTA DASH[®] GETS YOUR SMALL PACKAGE THERE IN A BIG HURRY.

Delta handles more over-the-counter shipments of 50 lbs. or less than any other certificated airline. And DASH (Delta Airlines Special Handling) serves 86 U.S. cities plus San Juan. Any package up to 90 inches, width + length + height, and up to 50 pounds is acceptable. DASH packages accepted at airport ticket counters up to 30 minutes before flight time, up to 60 minutes at cargo terminals.

Rate between any two of Delta's domestic cities is \$30. (\$25 between

Dallas/Ft.Worth and Los Angeles or San Diego or San Francisco). Pick-up and delivery available at extra charge. Call 800-638-7333, toll free. (In Baltimore, call 269-6393).

You can also ship via DASH between Delta cities in the U.S. and Montreal, Nassau, Bermuda, Freeport and London, England. For details, call Delta's cargo office. **DELTA**
The airline run by professionals

DELTA IS READY WHEN YOU ARE[®]

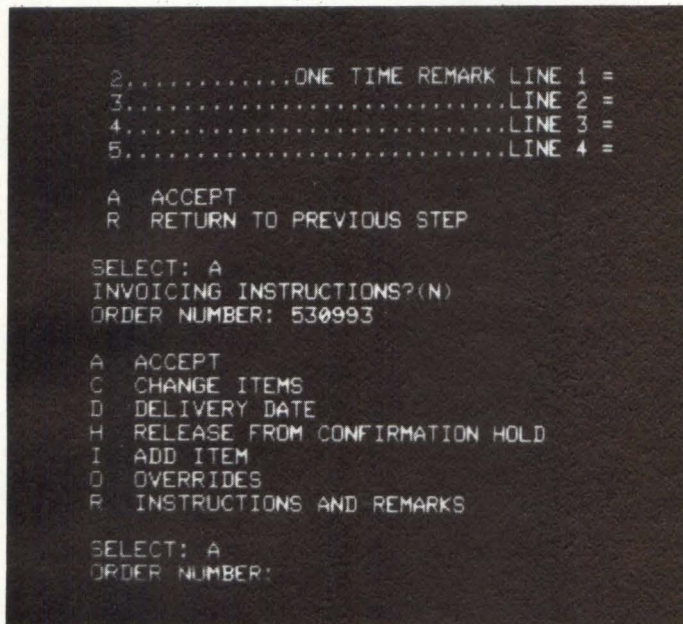


Communications Processor Interfaces to Packet Switching Networks

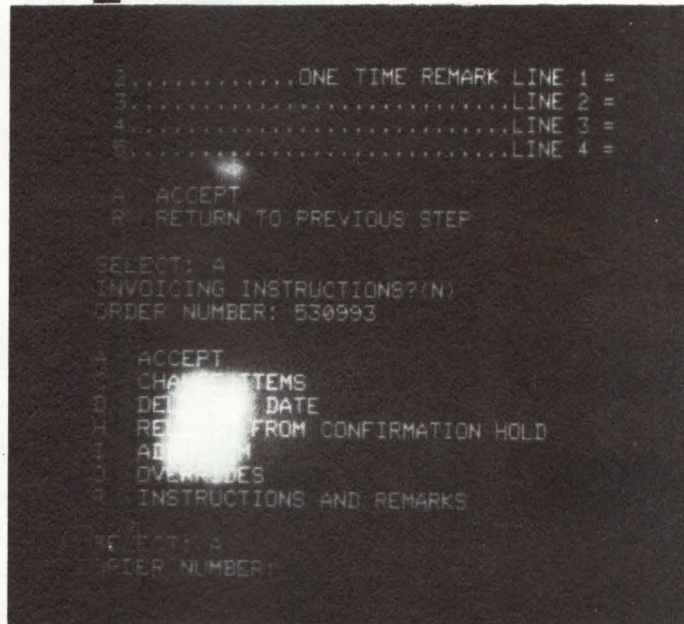
Basic function of MPAC 5000 is to interface any micro-, mini-, or main-frame computer, and asynchronous and synchronous terminals, to any X.25 compatible packet switching network. It supports up to 16 terminals at speeds to 9600 bits/s asynchronous and 56k bits/s synchronous. Each unit supports up to two HDLC (high level data link control) access lines at speeds of 1200 to 56k bits/s. Use of a second line affords hardware redundancy as well as providing for peak traffic distribution and minimizing queuing delays.

Furnished by Memotec Services Corp, 407 St-Laurent, Suite 300, Montreal, Quebec H2Y 2Y5, Canada, the unit fully implements the X.25 packet switching protocol with support from

To see or not to see? That is the question.



Display in ambient light with polarizer.



Display without polarizer.

And Polaroid has the answer: circular polarizer contrast-enhancement filters let you see your display under a variety of lighting conditions.

Circular polarizers kill reflections from CRT's by acting as a light trap. Ambient light can go through the circular polarizer, but after it is reflected from the tube face, it can't get out again. And circular polarizers can suppress up to 99% of reflected room light. They are far more effective than absorption-type filters for improving contrast.

Polaroid invented the circular polarizer and can satisfy your needs better than anybody else.

We offer the widest selection of *off-the-shelf* contrast-enhancement filters. Or—we'll make up precisely the filter you need: Choose glass or plastic filters with polished or non-glare surfaces. They can be flat or shaped to your specifications. They can have anti-reflective, RFI or abrasion-resistant coatings. Colors can be computer-matched to your display to provide maximum visibility.

We sell circular polarizers and offer technical assistance worldwide. For a free sample, just fill out and mail the coupon below. Or call Dick Adams *collect* at 617-864-6000, ext. 3315. He'll recommend the contrast-enhancing filter that best meets your needs.

And makes everything perfectly clear.

Polaroid Corporation, Technical Polarizer Division, Dept. A 415, 20 Ames St., Cambridge, Mass. 02139

Please send me a free sample circular polarizer and literature. Have your Application Specialist call me for an appointment.

Name _____

Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone Number _____

Application _____

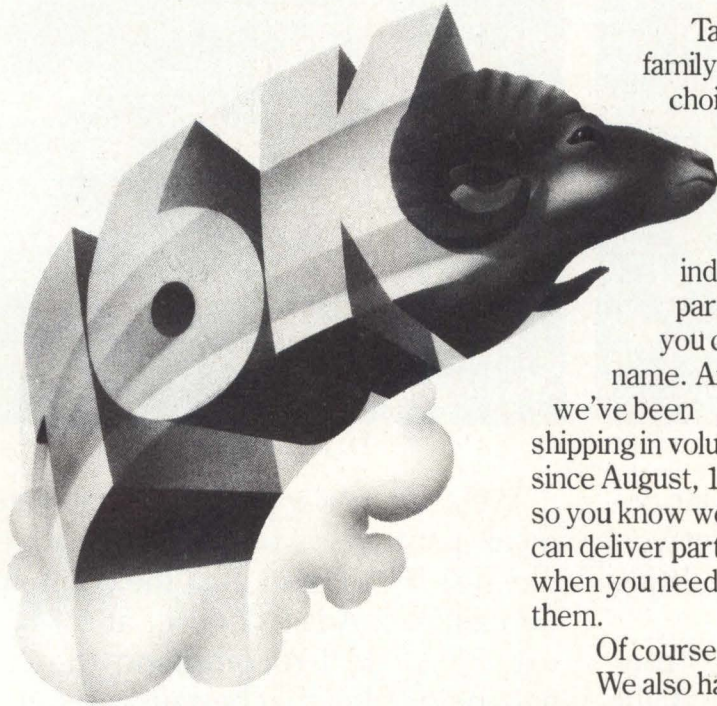
Polaroid®

Polarizing film. We made it first. We make it best.

©1979 Polaroid Corporation

Who do you think of
for high-performance 16K RAMs?

Next time,



Take your pick: our μ PD416 standard family offers a whole range of performance choices—extending to 120 ns access time and 320 ns cycle time. In either plastic or ceramic packages.

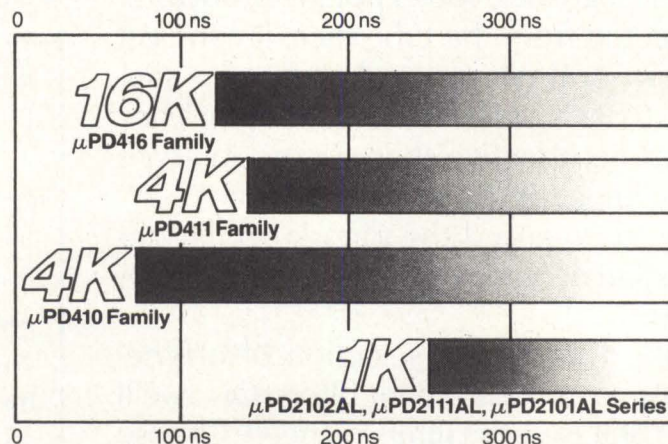
Every characteristic of our μ PD416 family meets or exceeds industry standards, which means our parts are suitable for any application

you can name. And we've been shipping in volume since August, 1977, so you know we can deliver parts when you need them.

P/N	t_{RAC}	t_{RC}	I_{DD1}	I_{DD2}
μ PD416-5	120 ns	320 ns	35 mA	1.5 mA
μ PD416-3	150 ns	375 ns	35 mA	1.5 mA
μ PD416-2	200 ns	375 ns	35 mA	1.5 mA
μ PD416-1	250 ns	430 ns	35 mA	1.5 mA
μ PD416	300 ns	510 ns	35 mA	1.5 mA

$t_a = 0^\circ\text{C to } +70^\circ\text{C}$

Of course, 16K RAMs are just part of our story. We also have a broad selection of other memory components, led by our industry standard



REPS: Action Unlimited, Arlington, TX; Spring, TX. Burton-Medley Associates, Grandview, MO. Cerco, San Diego, CA. Contact Sales, Inc. Burlington, MA. D/Z Associates, Inc., Denver, CO. Electronic Innovators, Inc., Minneapolis, MN. Eltron, Phoenix, AZ. HLM Assoc., Northport, NY. Parsippany, NJ. Imtech, Inc., Cleveland, OH; Dayton, OH. Kaytronics Limited, Ville St. Pierre, Quebec; Downsview, Ontario; Surrey, British Columbia. L & M Associates, Pikesville, MD; Montpelier, VA. Harry Nash Associates, Willow Grove, PA. R.C. Nordstrom & Company, Lathrup Village, MI. Perrott Associates, Inc., Fort Lauderdale, FL; Clearwater, FL; Orlando, FL. Santana Sales, Costa Mesa, CA. Stone Component Sales, Waltham, MA. Technology Sales, Inc., Palatine, IL. Trident Associates, Inc., Sunnyvale, CA. Tri-Tronix, Albuquerque, NM. Tri-Tronix, NW., Mercer Island, WA. 20th Century Marketing, Inc., Huntsville, AL; Greenville, TN. Wolff's Sales Service Company, Raleigh, NC.

DISTRIBUTORS: Almo Electronics Corp., Philadelphia, PA. Baltimore, MD. Bell Industries, Bellevue, WA. Century Electronics, Albuquerque, NM; Wheatridge, CO; Salt Lake City, UT. Norman Davis Electronics, South Euclid, OH. Diplomat/Westland, Inc., Sunnyvale, CA. Diplomat/Southland, Inc., Clearwater, FL. Diplomat/Lakeland, Inc., Elk Grove Village, IL. Diplomat/IPC of Mass., Chicopee Falls, MA. Diplomat, Holliston, MA. Diplomat/Northland, Inc., Farmington, MI. Diplomat/Electro-Com

think NEC.



4K Dynamic RAM (μ PD411), with access time down to 135 ns, and our highly successful high-speed 4K Static RAM (μ PD410), with access times down to 70 ns. Plus CMOS RAMs, Bipolar PROMs, 1K and 4K Static RAMs, and mask programmable ROMs up to 64K bits.

At NEC, we've built a reputation for advanced technology and volume delivery. We're also known for remarkable product reliability—thanks to experienced designers and meticulous manufacturing techniques, backed by 100% burn-in and testing with MIL-STD-883 methods. The result is an overall rejection rate of under 0.5%.

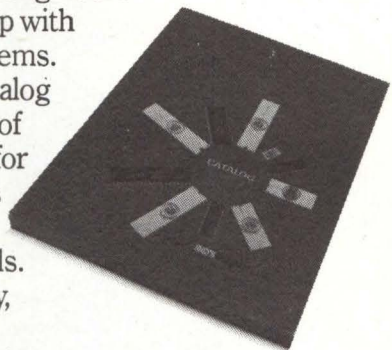
What's more, we offer thorough customer support, including documentation, testing, and special selection. And our engineers are always available to help with specific applications problems.

Our new product catalog will give you a better idea of just how much we can do for you, not only in memories but also in 8-bit and 4-bit processors and peripherals.

To get your free copy, clip your business card or letterhead stationery to this page and send to: NEC Microcomputers, Inc., 173 Worcester Street, Wellesley, MA 02181.

If you haven't thought of NEC before, you will. Next time.

NEC Microcomputers, Inc.



Corp., Minneapolis, MN. Diplomat/St. Louis, Inc., St. Louis, MO. Diplomat/IPC Corp., Totowa, NJ; Mt. Laurel, NJ. Diplomat Electronics Corp., Woodbury, NY. Diplomat/Alta-Land, Inc., Salt Lake City, UT. Future Electronics Corp., Montreal, Quebec; Rexdale, Ontario; Ottawa, Ontario. Hughes-Peters, Inc., Cincinnati, OH; Columbus, OH. Intermark Electronics, Sunnyvale, CA; Santa Ana, CA; San Diego, CA. Kent Electronics, Houston, TX. G.S. Marshall, Sunnyvale, CA; Irvine, CA; El Monte, CA; San Diego, CA; Phoenix, AZ. Milgray Electronics, Inc., Freeport, NY; Orange, CT. Reptron Electronics, Inc., Livonia, MI. Resco/Raleigh, Raleigh, NC. Semiconductor Specialists, Inc., Chicago, IL; Burlington, MA; Farmington, MI; Minneapolis, MN; Hazelwood, MO; Pittsburgh, PA; Dallas, TX; Milwaukee, WI. Sterling Electronics, Phoenix, AZ; Sun Valley, CA; San Diego, CA; Baton Rouge, LA; Waltham, MA; Albuquerque, NM; Dallas, TX; Houston, TX; Seattle, WA. Summit Distributors, Inc., Buffalo, NY. Summit Elec. of Roch., Inc., Rochester, NY. Technico, Inc., Columbia, MD; Roanoke, VA. Western Microtechnology Sales, Sunnyvale, CA.

REGIONAL SALES OFFICES: Western Region, NEC Microcomputers, Orange, CA (714) 633-2980. Eastern Region, NEC Microcomputers, Melville, NY (516) 293-5660.

CD-2-2

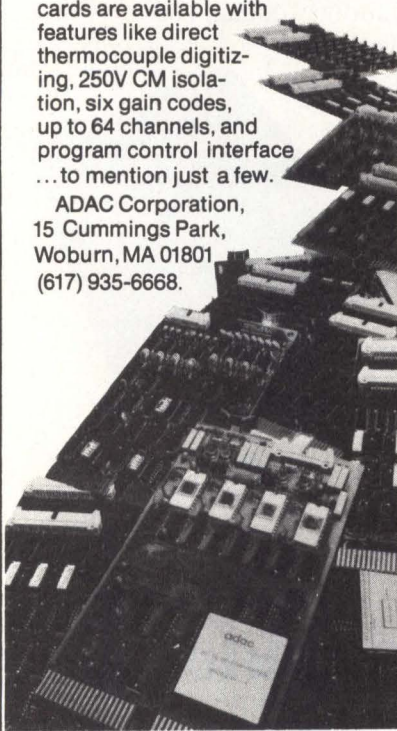
Nobody else has LSI-11 and LSI-11/2 cards like these.

Our digital cards are loaded with unique features such as the ability to use I/O lines as either inputs or outputs in increments of eight, up to 64 TTL inputs or outputs interfaced directly to the LSI-11 bus, the ability to detect contact closures on discrete input lines, and discrete latched outputs with the capability to drive high current incandescent lamps.

The Bus Repeater Card accommodates more devices than the basic bus can handle. The Bus Translator Card allows LSI-11 peripherals to operate with a Unibus CPU.

Both high level and low level analog cards are available with features like direct thermocouple digitizing, 250V CM isolation, six gain codes, up to 64 channels, and program control interface ... to mention just a few.

ADAC Corporation,
15 Cummings Park,
Woburn, MA 01801
(617) 935-6668.



COMMUNICATION CHANNEL

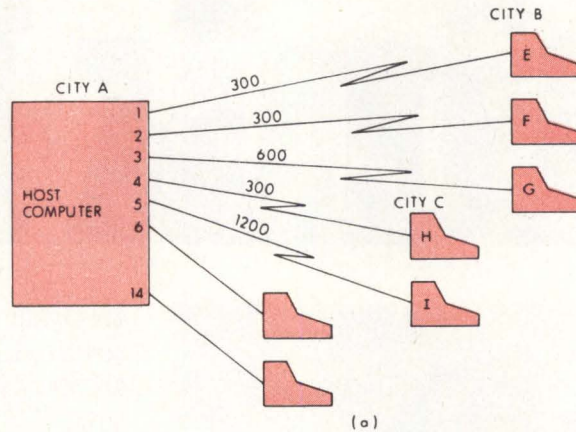


Fig 1(a) Host computer in city A has number of locally attached nonintelligent terminals to communication ports 6 through 14. Ports 1 through 5 have terminals E, F, and G from city B, and H and I from city C connected via dedicated facilities

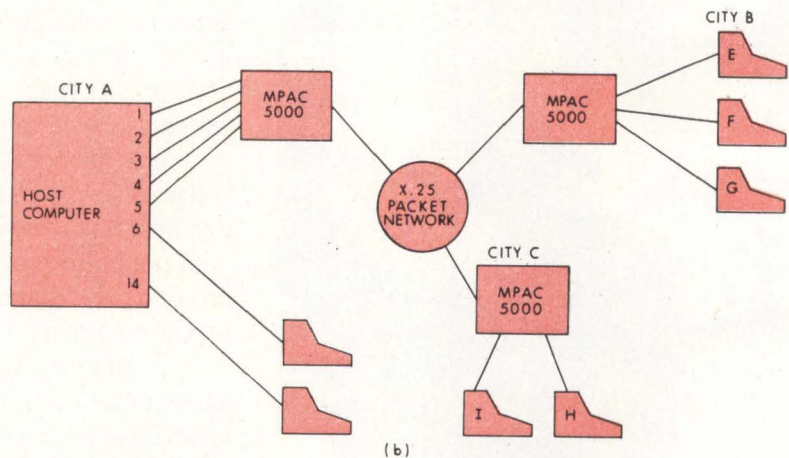


Fig 1(b) MPAC 5000 is connected to host using ports 1 through 5. Remote terminals at each location are connected to independent MPAC units reducing total number of lines required. Customer hardware and software remain unaltered. Unit in city A maintains protocol with units in cities B and C, so that all data from port 1 go to terminal E, from port 2 to terminal F, etc., and vice versa. Any asynchronous speed up to 9600 baud is supported

both permanent and switched virtual circuits. It is plug compatible with Bell 103, 213, and equivalent modems, and can be installed without any change to a user's hardware, oper-

ating system or application software. Options include data validation, encryption/decryption, and compression/expansion.

Circle 402 on Inquiry Card

Thinking Systems?

Think of the Possibilities – A Complete Computer for \$1275!*

**All You Do Is Add The Terminal, Printer,
And Applications Software —
And You've Got A Complete System!**

The Horizon is a complete computer — Z80, 16K RAM, Disk and I/O — priced so that the only limit to application in your system is your imagination! And, the Horizon is packaged in a natural wood cover, adding sales appeal to your system! Think of the possibilities if you're designing a system for education, small business, process control, word processing, engineering, or whatever is on your mind.

Over 10,000 North Star Systems In Use!

We offer you the maturity and reliability to meet the needs of demanding, high-volume applications. Horizon performance and reliability are assured through the use of the proven Z80A microprocessor and industry standard 5¼" 180K byte disk drives. Our professional approach to design (for example, a memory parity option) has been proven in thousands of installations.

North Star Horizon Specifications:

CPU: 4 mhz Z80A
RAM: 200ns (parity check optional)
Bus: 12 slot, S-100
Disk: 180K bytes per diskette
Controller: Up to 4 drives (720K bytes),
250 KB transfer rate
Cover: Natural Wood or
Blue Metal, no charge

**Complete Software Support:
DOS, BASIC, and MONITOR!**

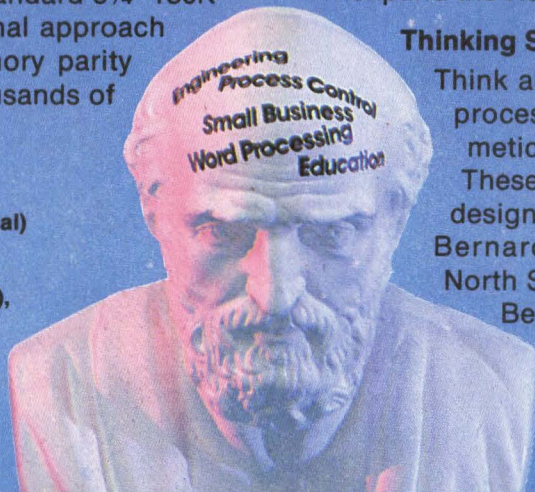
We provide you with the tools (system software) for writing the application programs that will make your system work! Our BASIC is a *full* extended disk BASIC! Hundreds of commercial software application packages have been developed using North Star BASIC. Additionally, a wide selection of application software for the Horizon is available from independent vendors.

Expand Your Horizon!

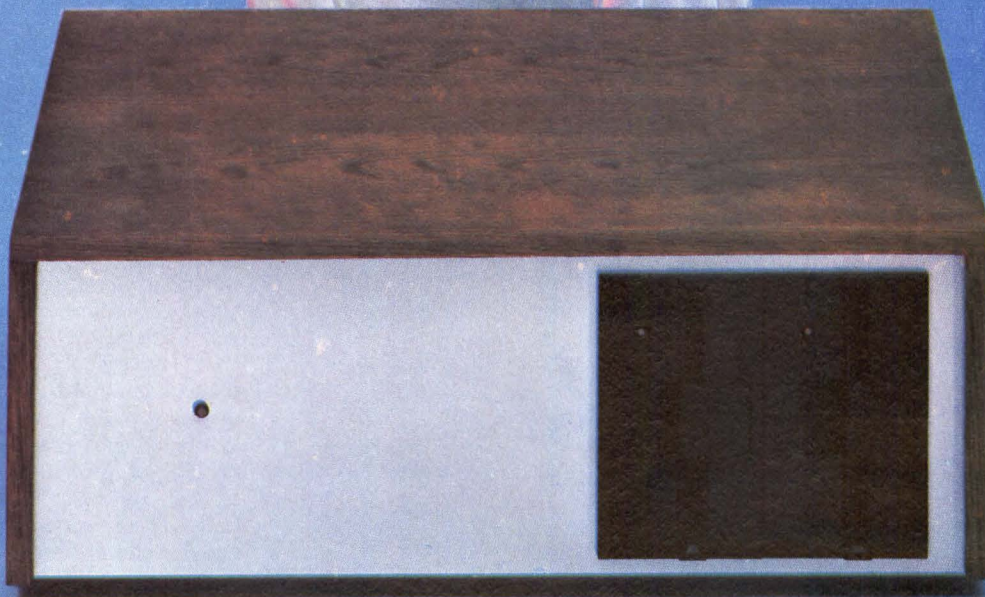
The Horizon can be expanded to 56K bytes or more of RAM, four disk drives (720K bytes), and three built-in I/O interfaces. Performance can be enhanced by the addition of the North Star hardware floating point board. Also, S-100 bus products from other manufacturers may be used to expand the Horizon.

Thinking Sub-Systems Only?

Think about North Star's memories, Z80A processor boards, floating point arithmetic boards, and disk drive systems. These are available for the OEM system designer. For complete information call Bernard Silverman at (415) 549-0858. North Star Computers, 2547 Ninth Street, Berkeley, California 94710.



NorthStar 



Report Analyzes Packet Switched Services

A recently released report's study of the charges for public packet switched networks, such as France's Transpac, shows that private circuits will be cheaper for large volume data traffic, while light usage will find the dial telephone network the cheaper way to go. Packet switching, however, offers savings for networks with medium traffic volumes, especially where fast response times and short transaction lengths are common. The "Logica Packet Switching Report" covers all aspects of the current packet switching scene, including the development of international standards. Problems of interfacing equipment to the new networks, case studies, and a survey of worldwide packet network developments are also included. The report is available from Logica, Inc, 801 Second Ave, New York, NY 10017, at \$250.

Packet switched services are already available in the U.S. and Canada, and are planned for Japan. Almost all Western European countries are planning to offer public packet switched services in the next few years. Therefore, according to the report, all makers and users of computer equipment should consider packet switching as a major influence in the data communications environment. Case studies show that major users are developing their own packet networks; for example, Citibank in the U.S. has set up a \$1.5M private network, while in the Netherlands, the Rijkswaterstaat (Water Authority) is spending \$2.5M on its own network.

Circle 403 on Inquiry Card

Instrument Setup Measures Bit Error Rate on T1 and T2 Systems

PF-1C digital error rate measuring setup is said to be the first dedicated instrument that can measure BER of standard T1 and T2 transmission systems without any modifications. Comprised of PFG-1 pattern generator and PFM-1 digital error rate meter, the 2-instrument combination is principally intended for testing standard digital radio systems and is also applicable in the production, installation, and maintenance of such systems. The instrument system is available from w&c Instruments, Inc, 119 Naylor Ave, Livingston, NJ 07039. It has front panel selectable 1.544M-bit/s (T1) and 6.132M-bit/s (T2) rates, selectable T1 and T2 line codes and direct system accessing capability.

PFG-1 generates two pseudorandom sequences and a number of frequently needed test patterns. It has been designed to allow testing of the effects of phase jitter and to make accurate error measurements despite its presence. An input for external phase modulation signals can be used to cause peak jitters in the range of 10 Hz to 200 kHz of up to $\pm 70^\circ$ and $\pm 40^\circ$ at 1.544M and 6.312M bits/s, respectively. The generator's intrinsic jitter at 1.544M bits/s is $\pm 0.8^\circ$ max. A bit-blanking (zero injection) feature allows testing of clock recovery circuits in regenerators. Internal clocks can be varied from front panel to test systems for tolerance to bit rate variance.

PFM-1, at the receiving end of link under test, has its own reference pattern generator and clock regenerator and can operate independently from the PFG-1. The display reads



PF-1C test setup. It has compatible 100/110- Ω balanced inputs and outputs and provides standard T1 (AMI-1/2) and T2 (B6ZS) line codes. There are additional 75- Ω inputs and outputs with RZ, NRZ, and AMI-1 codes

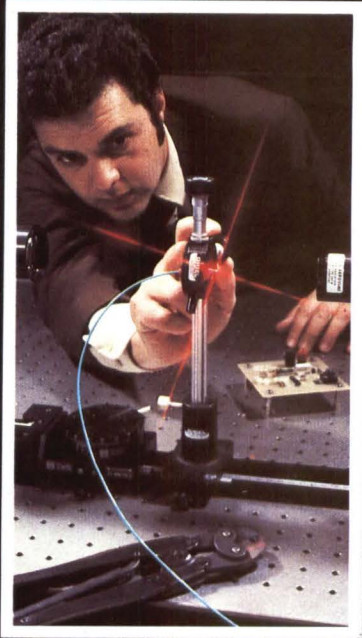
For a happy ending,

See page 51

from 1×10^{-2} to 9.99×10^{-3} with analysis over 10^7 clock bits, or 1×10^{-8} to 9.99×10^{-4} over 10^8 clock bits. Display is three digits plus an exponent. The instrument also has both pseudologarithmic analog and BCD outputs.

A convenient feature allows the pattern generator to be operated remotely by the error rate meter, for loopback measurements. The whole PF-1C setup can be remotely controlled for use in computer controlled test systems. The generator weighs about 18 lbs (8 kg) and the meter 20 lbs (9 kg). □

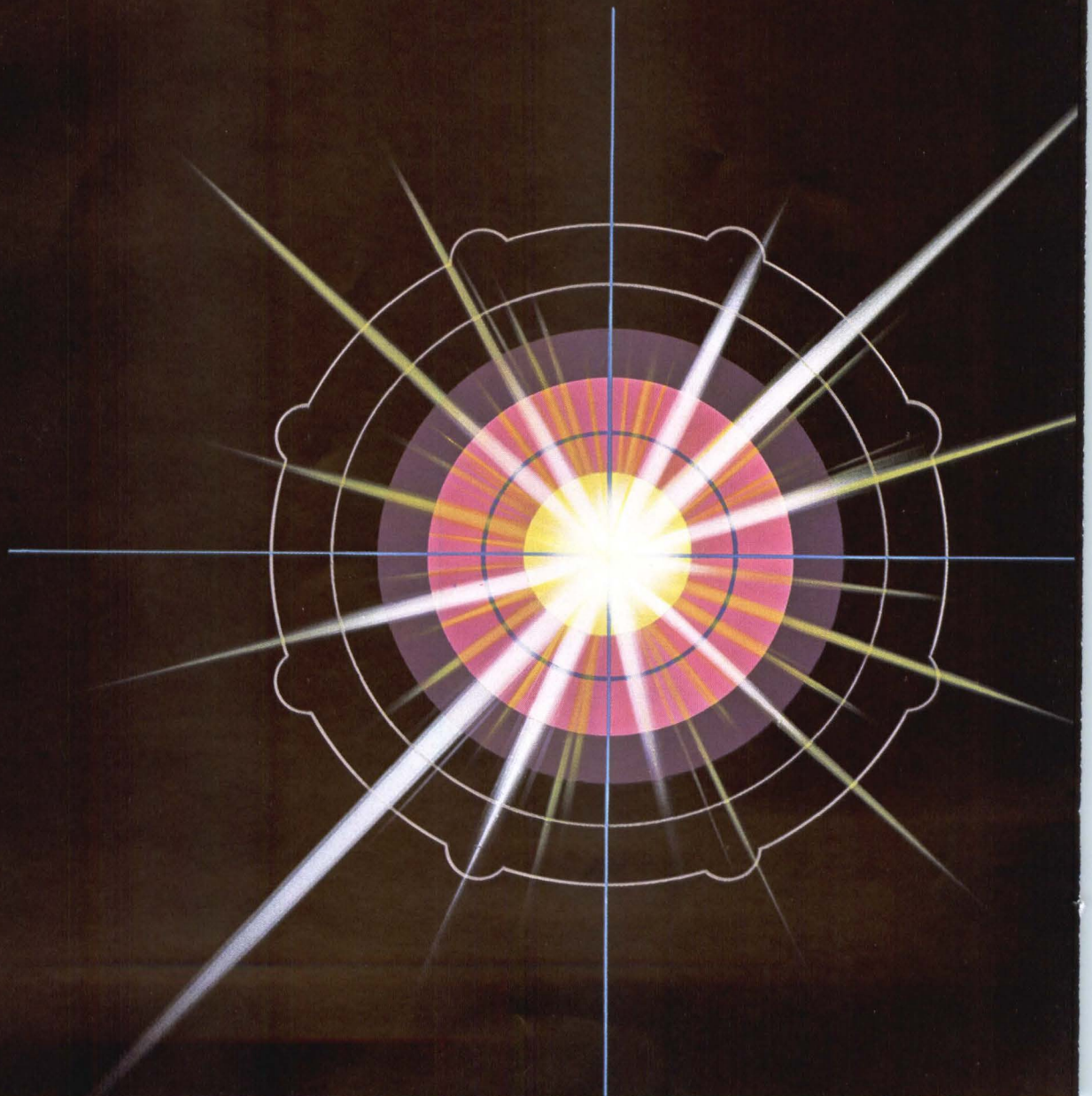
Circle 404 on Inquiry Card



**STARTING TODAY...
EVERYTHING YOU NEED
TO DESIGN TOMORROW'S
FIBER OPTIC DATA LINKS
COMES IN ONE KIT.**

“Brings an experimental fiber optic link to about 85% of the way toward a final commercial design...”

Design News Magazine



Just three steps to a precise fit

That's all it takes with the Optimate connectors in the kit:

1. Assemble with a few parts
2. A simple proven crimp
3. Then accurate polishing



Connectors for every problem

You will soon see that the AMP Optimate connector solves three basic problems quite neatly and precisely:

- Coupling of the light source to the fiber optic cable
- Splicing cables
- Coupling the fiber optic cable to the photodetector.

Innovative crimping tool

Every kit includes this unique tool which enables you to attach cable to connector accurately and permanently. The AMP crimping tool will not release until a certified, repeatable crimp is made.

Complete instructions

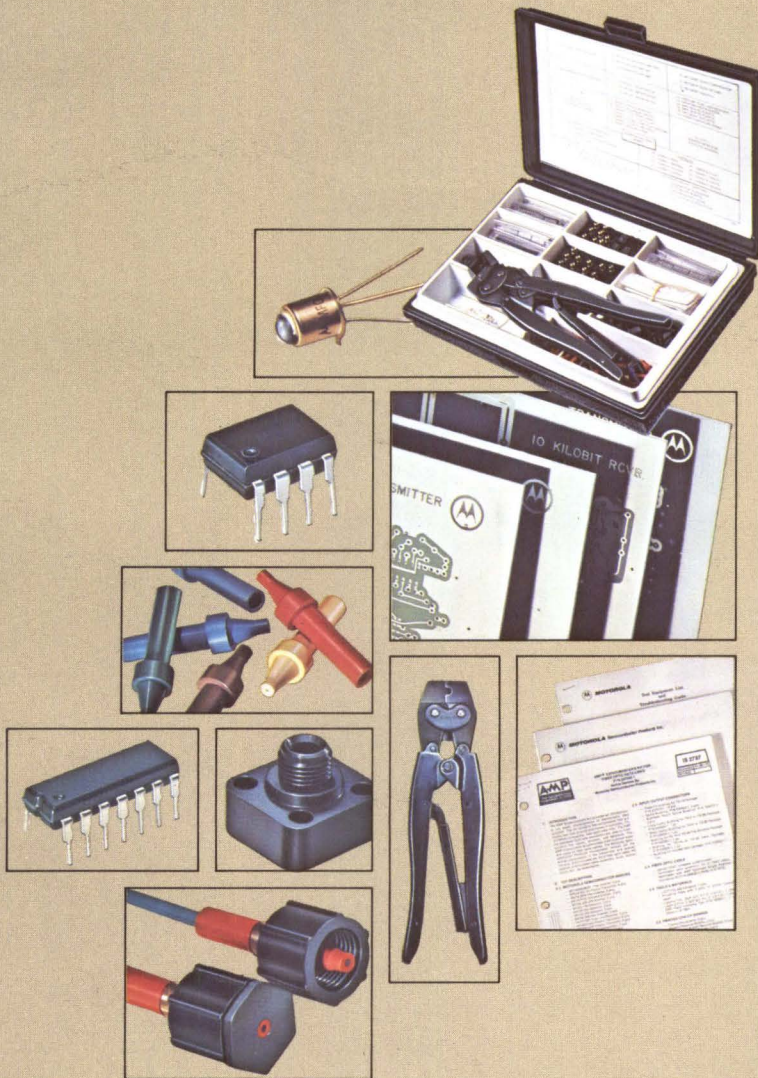
Nothing is left to chance. You get an experimenter's guide on system characteristics and complete instructions for constructing and experimenting with up to six fiber optic systems.

ORDER NOW. SEE BACK PAGE.



ANNOUNCING THE OPTIMATE EXPERIMENTER'S KIT FROM AMP.

With this one kit you can put your mind in high gear with all the elements necessary to design as many as six different workable data links ranging from 1 kilo-bit to 1 mega-bit—all TTL or CMOS compatible.



The AMP Optimate Experimenter's Kit gets you out of the parts procurement business and back into the design business. Cables...emitters...detectors...connectors...crimper...instructions—everything is in the kit. There's nothing extra to buy.

You actually design and experiment with active devices made by Motorola Semiconductor Products, Inc. as well as with a whole array of AMP fiber optic connectors, cable and p.c. boards. The kit includes instructions for making as many as six TTL- and CMOS-compatible low frequency data links operational to 45 meters or more. Components are also suitable for use with lower loss cables (not supplied.)

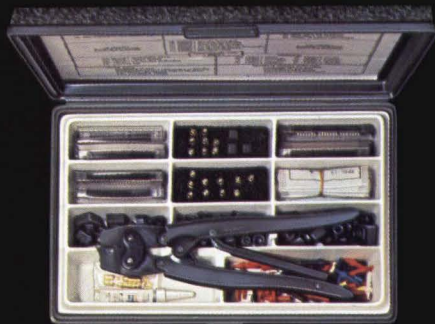
Active devices in the kit

These include pin photo diodes, phototransistors, photodarlington transistors and infrared emitting diodes. Components include numerous integrated circuits serving as amplifiers, buffers, inverters, receivers and comparators.

Six transmitter and six receiver PC boards are part of the package. Transmitter circuits range from one-kilobit to one-megabit capacity. Receivers can be one, two or four-channel, one kilobit to one-megabit capacity.

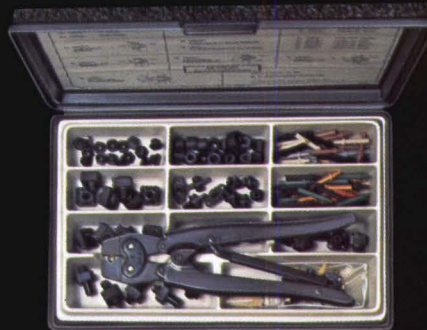
Complete set of AMP Optimate connectors

The heart of the kit—and the primary reason you can now design commercially feasible, repeatable fiber optic data links—is the AMP Optimate connector. It makes terminations simple, quick and accurate. Optimate connectors use a resilient material which insures centering to a degree previously unattainable. Precise, accurate polishing—once difficult—is fast, troublefree and easy, thanks to a simple polishing bushing that comes with the kit.



AMP OPTIMATE EXPERIMENTER'S KIT FOR FIBER OPTIC DATA LINKS

Included in this kit are all the components described, plus detailed instructions for constructing several fiber optic data communication links. Available only from AMP. P/N 227042-1



AMP OPTIMATE DESIGNER'S KIT

Contains assortment of fiber optic connectors, 1/0 bushings and tooling for use with your own cable, light sources and detectors—all housed in a sturdy box. An excellent low-cost introductory kit. Available only from AMP. P/N 530950-1

ORDER YOUR NEW OPTIMATE FIBER OPTICS KITS DIRECTLY FROM AMP. CHOOSE THE KIT YOU NEED. FILL OUT AND MAIL THE COUPON.

Remember, the Experimenter's Kit comes with active devices and boards. The Designer's Kit comes without them. Take your pick. Please include a company purchase order number, check or both. If you'd like more information, call us: Extension 8400, (717) 564-0100, AMP Incorporated, Harrisburg, PA 17105.

AMP has a better way.

AMP

INCORPORATED

Check Reader Service Number 101

AMP Customer Service, AMP Incorporated, Harrisburg, PA 17105

Please place my order for:

- OPTIMATE Experimenter's Kits for Fiber Optic Data Links at only **\$350** each. (P/N 227042-1)
- OPTIMATE Designer's Kits at only **\$181⁵⁰** each. (P/N 530950-1)
(Prices applicable to United States only.)

Please charge me as follows:

- CHARGE them to the following company order # _____.
- Enclosed is payment for the order.

My telephone number is (AC) _____

Name _____

Company _____

Address _____

City _____ State _____ ZIP _____

M508

AMP is a trademark of AMP Incorporated

 is a trademark of Motorola, Inc.

NEC Spinwriter. The fluent printer.

One printer. Many extra language features.

Users of word processing, computer output or terminal character printers expect fine print quality from their character printers.

But with NEC Spinwriter™ printers, you get even more. Our unique "thimble" — with up to 128 characters — gives you many extra features no other printer offers.

Like bi-lingual fonts, so you can print in any two languages at once. Or multi-lingual fonts — with up to five languages on the same print element: English, French, German, Spanish and Italian. Or technical/math thimbles with full alphanumerics, plus super- and subscripting and many arithmetic and scientific symbols.

Then add our unique 100-character-plus proportional space thimbles, numerous font styles in 10-, 12-

and PS pitches, and our low-cost custom thimble design capabilities.

That's six extras so far. Seven: speed. Spinwriter printers use lightweight thimbles, so they print at a full 55 cps. Eight: durability. Our fiberglass-reinforced elements last up to 30 million impressions. And finally: quietness. Spinwriter thimbles are so much quieter than other character printers that you can hear the difference.

Now add those features to Spinwriter's acclaimed reliability, serviceability and ease of use, and see if you can find a reason for not including them in your systems.

And don't forget our Trimliner™ band printers. The ideal line printer for products that need 300-to-600 LPM output that you can always rely on.

For more information on Spinwriter and Trimliner printers, contact NEC, where better printers are made.



NEC

NEC Information Systems, Inc.

Eastern Office: 5 Militia Drive, Lexington, MA. 02173, (617) 862-3120
Central Office: 3400 South Dixie Drive, Dayton, OH. 45439, (513) 294-6254
West Coast Office: 8939 S. Sepulveda Blvd., Los Angeles, CA. 90045, (213) 670-7346

CIRCLE 18 ON INQUIRY CARD



Montgomery Phister, Jr, writer, teacher, and consultant on subjects related to the economics of data processing, received BSEE and MSEE degrees from Stanford University, and holds a PhD from Cambridge University in England. His professional career includes positions at Hughes Aircraft, Thompson Ramo Wooldridge, Scantlin Electronics, and Xerox Data Systems.

TECHNOLOGY AND ECONOMICS: OPTIMUM PREVENTIVE MAINTENANCE STRATEGY

Montgomery Phister, Jr

Systems Consulting
Santa Monica, California

Preventive maintenance costs can amount to 45% of all maintenance expenses for a computer peripheral (see *Computer Design*, Oct 1978, p 111). This discussion centers on the factors that an organization must consider in establishing a preventive maintenance strategy.

Computer peripheral equipment can benefit from regular preventive maintenance, whose function is to reduce the incidence, and thus the cost, of preventable failures. A preventable failure is one whose probability of occur-

rence, following a repair or preventive maintenance action, can be described by a curve such as that of Fig 1. Peripheral units in particular are subject to such failures, which are normally caused by the accumulation of dirt at or near the read/write mechanism—magnetic oxide accumulations on a magnetic tape head, or paper fibers on punched card or line printer mechanisms.

With such equipment it makes sense to schedule regular preventive maintenance (PM). Maintenance strategy typically might obey the following rules. Subsequent to any maintenance action:

- (a) If no failure occurs prior to the PM interval, time t_p , carry out scheduled PM.
- (b) If the preventable type failure occurs before time t_p , repair it.
- (c) If another type of failure occurs before t_p , repair it, and, while the customer engineer (CE) is on the site, carry out PM.

Preventive Maintenance Interval

Clearly, PM is worthwhile only if the time spent on a PM call is less than the time which would be spent curing

An advocate of the premise that those involved in data processing at any level will benefit from a broad view of the economics of the industry, the author of this first in a series of columns contends that it is only through the study of the economics of technology that the best use and direction of science of technology can be determined. "A study of the science of technology defines what is possible; a study of the economics of technology establishes which of the possibilities is practical and useful."*

**Data Processing Technology and Economics*, M. Phister, Jr, Santa Monica Publishing, Santa Monica, Calif, 1976

Three OEM drives from Control Data with proven technology and reliability.



All three drives share a compatible interface. All have 35 ms. average access time, the same 2.5 MHz transfer rate and are daisy chainable from the same controller. They are among the most popular products in our line of OEM rotating memory.

Choose our Fixed Media Disk Drive for its 6000 MTBF reliability

The Model 9414 uses a non-removable 5440-type media disk, to store up to 12 Mbytes. Configured as stand-alone memory or with one of our low-cost flexible disk drives for backup, you get superior reliability.

Or our Cartridge Disk Drive that uses fixed/removable media

The Model 9427-H uses a removable disk cartridge and a single fixed disk to provide 12 Mbytes of storage capacity. One of the reasons for its wide acceptance (over 25,000 installed) is our flexible switch-controlled interface and four different connector options. This interface flexibility means our customers—and yours—can “plug and play” without costly hardware or software conversion.

Or a Voice Coil Drive for large-capacity storage

The Model 9747 gives you up to 60 Mbytes of storage using a CDC® 9873 or IBM 2316 disk pack. It's one of our most popular drives because of its proven reliability and exceptionally low cost... more than 30,000 delivered.

And all drives are ready for shipment

Control Data manufactures heads, media and

actuators for these drives, so you don't have to worry about delivery delays.

Put quality behind your nameplate. Call us at 612/853-3399 or if in Europe, contact one of our European representatives. Or return coupon to:

D. C. Steiner, General Manager, OEM Product Sales CD-39
 Control Data Corporation
 P.O. Box 0
 Minneapolis, MN 55440

Please send information on your

- 9414 Fixed Media Disk Drive 9747 Voice Coil Drive
- 9427-H Cartridge Disk Drive Entire OEM Product Line

Name _____ Title _____

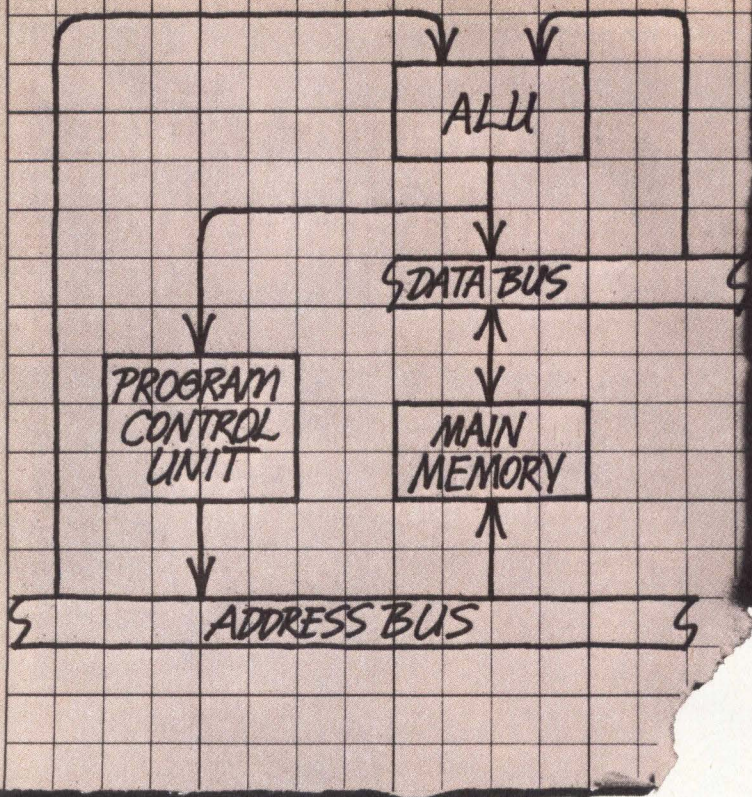
Company _____ Phone _____

Address _____

City _____ State _____ Zip _____



More than a computer company



THE AM2930
PROGRAM CONTROL UNIT

- COMPUTE NEXT ADDRESS IN PARALLEL WITH DATA OPERATION.
- 20-BIT ADDRESS LOGIC-- NOT CONSTRAINED BY 16-BIT ALU.
- 17 LEVEL HARDWARE SUBROUTINE STACK.

**CHAPTER FIVE:
THE PROGRAM CONTROL UNIT.**

Advanced Micro Devices continues its advanced course in microprogrammable microprocessing.

Step by step, function by function, we've been showing you how to build a fast, powerful microprogrammed machine.

When the course is over, you'll know what we know. As it turns out, that's quite a lot.

Every computer design contains logic for addressing the machine's memory.

The logic may be a simple address register driven from the ALU's output, or it can be a more complex Program Control Unit.

A PCU is a subsystem designed to handle address computation, indexing and various addressing modes. It relieves the need to squeeze data and address calculations through the same ALU.

BUILDING A MICROCOMPUTER, CONTINUED.

THE SQUEEZE IS OFF.

Advanced Micro Devices announces the Am2930 Program Control Unit. It increases throughput by computing addresses while your ALU processes data. Under micro-program control, the Am2930 can compute an effective address and update an on-chip program counter. No more addresses in the same place as the data. No more squeeze.

Two separate on-chip adders allow the program counter to be incremented while two operands are added together to create a memory address. The Am2930 also supports up to 17 levels of subroutines with the return stack right on chip.

THAT'S NOT ALL, FOLKS.

In addition to the Am2930, there's the Am2932. They're both expandable 4-bit slices. They both have the same powerful architecture. But the Am2932 comes in a space-saving 20-pin package.

So relax. You no longer have to process addresses in the same place as data.

With the Am2930 and Am2932, the squeeze is off.

BUILD YOUR LIBRARY. FREE.

Each of these monthly messages is backed by a ton of theory and applications information. Send in this coupon and we'll send you Chapter Five and tell you how to get the whole book.

Advanced Micro Devices
901 Thompson Place
Sunnyvale, California 94086

I want to build a microcomputer. Sign me up.

Name _____

Title _____

Mail Stop _____

Company _____

Address _____

City _____ State _____ Zip _____

3/79/CD

Advanced Micro Devices



Multiple technologies. One product: excellence.
901 Thompson Place, Sunnyvale, California 94086
Telephone (408) 732-2400

Next Chapter, The Data Path, Part II.

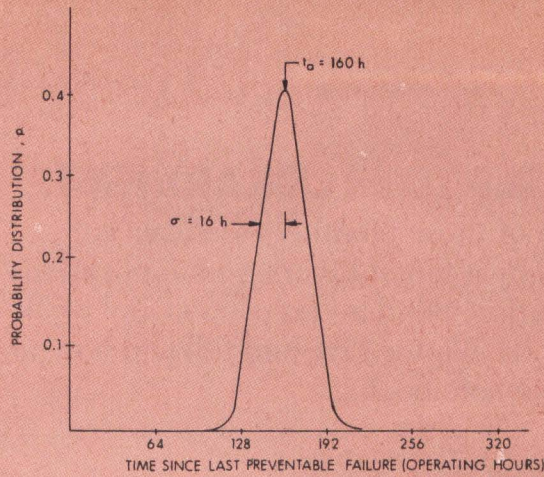


Fig 1 Probability distribution of typical preventable failure. Assume that failure occurrences follow normal distribution, with average time t_a and standard deviation σ . Thus, probability that preventable failure will occur between time t and time $(t + \Delta t)$ is $(p \times \Delta t)$

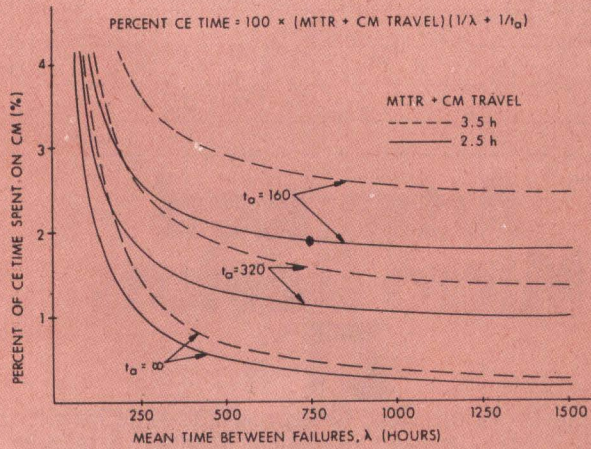


Fig 2 Percent CE time vs MTBF with no preventive maintenance. If $t_a = 160$ h, $\lambda = 750$ h, and MTR + travel time = 2.5 h as indicated by dot, the device will require 1.9% of CE's time without PM. Bottom two curves illustrate effect of eliminating preventable failures altogether

a preventable failure during a normal CE trouble call. PM calls are shorter than corrective maintenance (CM) calls for two reasons: they can be scheduled, so that travel time is less; and they require no diagnosis.

In choosing a value of t_p to implement this strategy, average time (t_a), and standard deviation (σ) must be taken into account, along with the time the CE spends in traveling to the customer's site, and performing PM and CM. It is evident there is an optimum value for the PM interval t_p . If this value is too small, the CE will spend too high a proportion of time on PM; if too large, too great a proportion of time will be spent dealing with preventable failures. Although the equations describing this situation cannot be solved analytically to determine the value of t_p which minimizes the CE's lost time, the approximate equations (see "Approximate Equations") are suitable for all practical purposes, and were used to calculate the curves of Figs 2 through 5.

Approximate Equations (for $t_p \leq t_a \leq 2.5 \sigma$)

Define

$$p_{10} = 0.5 \text{ EXP} \left[-1.21 \left[\frac{t_a - t_p}{\sigma} \right]^{1.42} \right]$$

$$p_{20} = \frac{t_p}{\lambda}$$

$$p_c = \frac{t_p - t_a + 2.5\sigma}{3 t_p}$$

Then

p_1 = Probability that a preventable failure will occur before time t_p

$$p_1 = p_{10} - p_{10}p_{20}(1 - p_c) \quad \text{if } t_p \geq (t_a - 2.5\sigma)$$

$$p_1 = 0 \quad \text{otherwise}$$

p_2 = Probability that a nonpreventable failure will occur before time t_p

$$p_2 = p_{20} - p_{10}p_{20}p_c \quad \text{if } t_p \geq (t_a - 2.5\sigma)$$

$$p_2 = p_{20} \quad \text{otherwise}$$

t_1 = Average time for occurrence of a preventable failure

$$t_1 = t_a - \frac{1}{p_{10}\sigma\sqrt{2\pi}} \left[e^{-\frac{(t_a - t_p)^2}{2\sigma^2}} - e^{-\frac{t_p^2}{2\sigma^2}} \right]$$

t_2 = Average time for occurrence of nonpreventable failure

$$t_2 = \frac{t_p}{2} - \frac{t_1}{2} p_{10}p_c \quad \text{if } t_p \geq t_a - 2.5\sigma$$

$$t_2 = \frac{t_p}{2} \quad \text{otherwise}$$

$$p_3 = 1^2 - p_1 - p_2$$

and percent CE time used for maintenance =

$$\frac{p_1 (\text{MTR} + \text{CM Travel})}{p_{11}t_1 + p_{21}t_2 + p_{31}t_p} + \frac{p_2 (\text{MTR} + \text{CM Travel} + \text{MTPM})}{p_{12}t_1 + p_{22}t_2 + p_{32}t_p} + \frac{p_3 (\text{MTPM} + \text{PM Travel})}{p_{13}t_1 + p_{23}t_2 + p_{33}t_p}$$

Using Corrective Maintenance Only

If no PM is elected, the equation and curves of Fig 2 show how the percentage of CE time spent on CM varies with mean time between failures (MTBF) for two different values of mean time to repair (MTR) plus travel time (dotted and solid curves) and for two different values of t_a .

The curves in Fig 3 show the percentage of a CE's time spent in PM and CM on a single device, as a function of the PM interval t_p . We assume the average time t_a between preventable failures is 160 h. For $\sigma = 16$ h (ie 68% of the preventable failures occur from $160 - 16 = 144$ to $160 + 16 = 176$ h after the last occurrence), the optimum PM time is about 120 h, for $\sigma = 32$ the optimum drops to about 100 h, and for $\sigma = 64$, to about 88 h, given the repair and travel times shown. Comparing Figs 2 and 3, it can be seen that the use of PM reduces the CE's percent time by 40 to 60%, depending on σ .

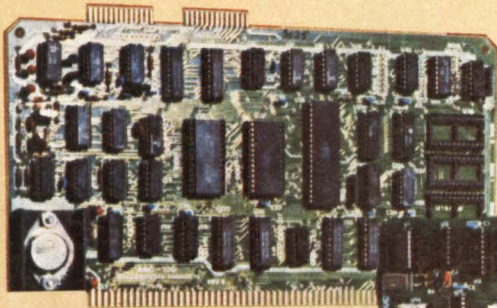
Travel time for PM actions has an important effect on the CE's time spent per device, and a noticeable effect on the optimum value of t_p (Fig 4). If PM travel time increases from 0.2 to 1.0 h, the CE percent time spent increases from 0.75 to 1.25%, and the optimum PM time from 100 to 135 h.

Percent "lost time" to the customer is nearly the same as percent CE time spent on CM and PM. While the CE is performing PM or CM at the site, and while he is traveling

Guaranteed Compatible!

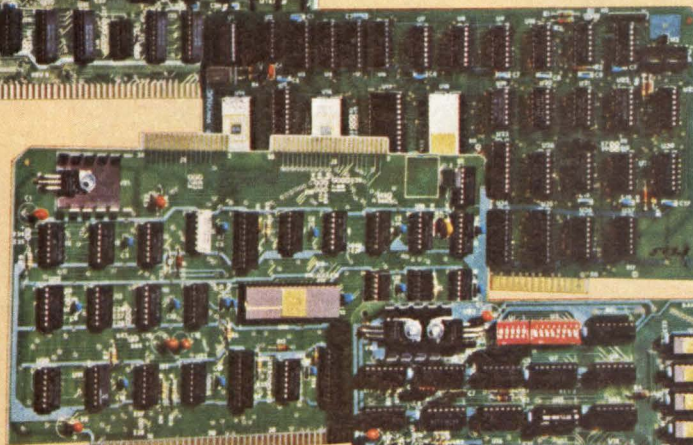
S-100 Bus OEM Boards

From SD Systems at reasonable prices

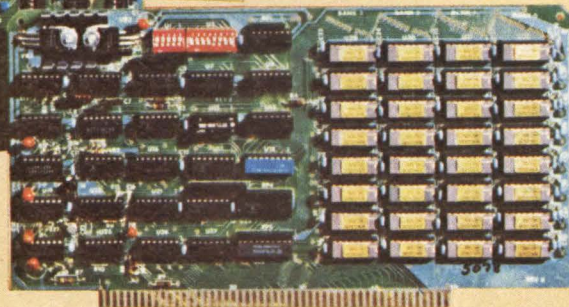


Single Board Computer (SBC-100)

Video Display Board (VDB-8024)



Flexible Disk Drive Controller (Versafloppy)



64K Random Access Memory (ExpandoRAM)

ASSEMBLED TESTED AND FULLY BURNED IN

The search is over for the convenience of S-100 Bus Computer boards that are really compatible and dependable. State-of-the-Art engineering, outstanding flexibility, rapid delivery, and low costs make the SD Systems computer boards the best OEM buy. The **SBC-100 Single Board Computer** is based on the Z80 microprocessor. Up to 8K of 2716 PROM, Serial RS-232 Port, Parallel Input/Output Ports, Software programmable baud rate generator, Four channel counter/timer, and 1K of RAM, all on-board. **VDB-8024 Video Display Board** features an on-board Z80 microprocessor for maximum flexibility in video control. 80 characters by 24 lines, displayed with high resolution on a 7x10 dot matrix. On-board Keyboard power and interface, 2K memory and a glitch-free display by use of I/O mapped interface make this board the most superior board on the market.



The **ExpandoRAM** is available in 16, 32, 48, or 64K versions using 4116 RAMs. The population can be increased in the field at a future point if requirements change. Featuring Switch selectable boundaries, Bank Selectable Write Protect and using less than 5 watts, the ExpandoRAM is more reliable memory for the money than any other OEM board. **Versafloppy, Flexible Disk**

Drive Controller with IBM 3740 soft sector-ed format compatibility controls up to four single or double sided disk drives either mini or standard size. **Full Line Software** includes Editor, Z80 Assembler, Linker, C-Basic, Complete Business Packages, System Diagnostic and Control Software and Disk Operating System. **PROM Programming Software and Hardware** also available. Circle the reader service number for full Technical Data... or call toll free to our Customer Service Department: 800-527-3460.

POST OFFICE BOX 28810 — DALLAS, TEXAS 75228

800-527-3460 — 214-271-4667 — TELEX 73-0151

CIRCLE 20 ON INQUIRY CARD

graphics software.

You just lost your last excuse for sticking with alphanumerics. Because with HP's new 2647A Intelligent Graphics Terminal, you get graphics without digging into your CPU's software.

A picture's worth a thousand numbers.

On an alphanumeric terminal, your data's just a screen full of numbers. But with the 2647A you can plot tabular data as a bar graph, or a pie chart, or a linear or logarithmic line graph. Quickly, with just a few keystrokes.

Now you can really see your data, not just look at it.

What's more, with the 2647A you can zoom in and out. Pan right, left, up, down. Selectively erase. Shade important areas to make them stand out. Use a rubber-band line to make a quick sketch.

Without any help from your programming department.

It's more than smart.

The 2647A's the smart way to get graphics from tabular data without software.

But what if your CPU's output isn't tabular? Or if you'd like to plot derived data, say a three-month moving average from monthly sales figures? Or if you need more than a bar graph, pie chart or line graph?

The 2647A's not just smart, it's intelligent.

You can program it to reformat data from your CPU, or to compute more data, in easy-to-write BASIC. And you can program it in AGL, our high-level graphics language extension of BASIC. Its powerful commands, such as FRAME, AXES, LABEL, LOCATE and PLOT, put sophisticated graphics at your fingertips.

Either way, your program runs on the 2647A without

any help from your CPU.

Hard copy's easy.

How do you get graphics into your briefcase?

The 2647A makes graphics as portable as alphanumerics. It interfaces easily with our 9872A Four-Color Plotter (which can even make overhead transparencies), and with our 7245A Thermal Plotter-Printer. All you need is an interface card, a cable and the peripheral itself.

And to keep costs down, more than one 2647A can share the same hard copy peripheral.

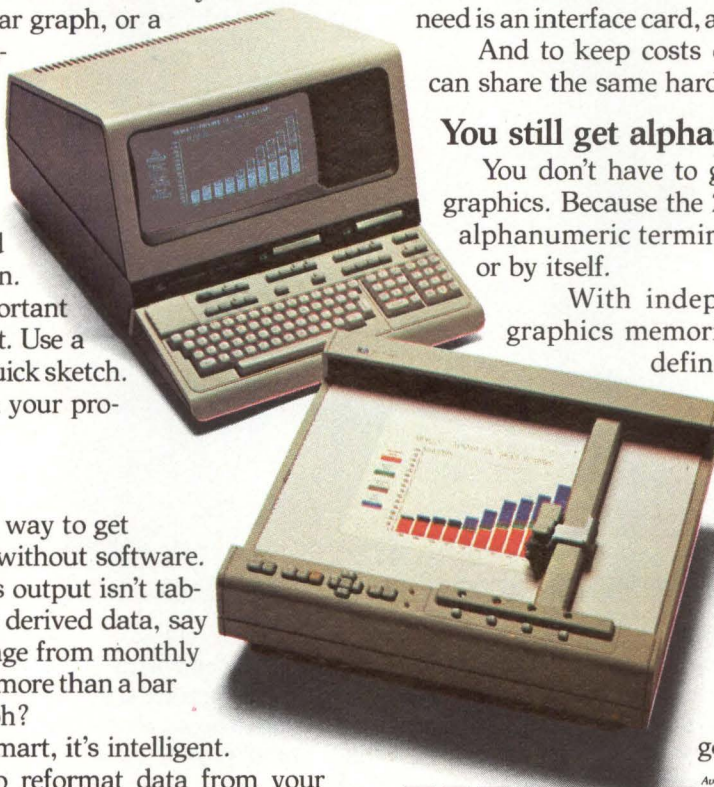
You still get alphanumerics.

You don't have to give up alphanumerics to get graphics. Because the 2647A's also a programmable alphanumeric terminal for interactive use on-line or by itself.

With independent alphanumeric and graphics memories. Eight soft keys you can define to do several steps with a single keystroke. A bright, easy-to-use, high resolution display. And built-in dual cartridge tape drives for 220K bytes of mass storage.

Best of all, the 2647A with full memory and data communications interface costs only \$8300*.

Which makes it easy to get the picture.



HEWLETT  PACKARD

42805HPT9

*U.S. domestic list price

CIRCLE 21 ON INQUIRY CARD

- Send me more information about graphics without graphics software.
- Show me graphics without graphics software.

Name _____ Title _____

Company _____

Address _____

City/State/Zip _____

Phone _____

Mail to Hewlett-Packard, Attn: Ed Hayes,
Marketing Manager, Data Terminals Division, Dept. 1227,
19400 Homestead Road, Cupertino CA 95014.

*U.S. domestic list price
Available on GSA Contract #GS-00C-01529 from 12/8/78 through 9/30/79

TEKTRONIX thinks your logic analyzer should be as versatile as you are

So ours let you sample *synchronously* and *asynchronously*.



Use the 7D01F
for hardware
and software
applications.

As a digital designer you must be versatile enough to do the *entire* design job. Logic and timing. Software and hardware analysis. Activity on and off the bus.

And so you need a logic analyzer that lets you synchronously verify logic and trace program flow on the bus; then asynchronously verify timing sequences and examine chip to chip transactions off the bus. A logic analyzer, in short, as versatile as you are.

Tektronix Logic Analyzers are versatile. In the synchronous mode, examine software flow using the clock of the system under test—up to 20 ns sampling rate. Switch to asynchronous and sample with the Logic Analyzer's own clock—up to 10 ns sampling rate. Pulse anomalies and timing problems are out in the open, where you can see them. With *one* logic analyzer.

Synchronous and asynchronous sampling: it helps

make our Logic Analyzers versatile. So you can do today's job and tomorrow's. So you can change applications without changing your logic analyzer.

Contact Tektronix Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix, Ltd. P.O. Box 36, St. Peter Port Guernsey, Channel Islands.

Tektronix
COMMITTED TO EXCELLENCE

For technical data,
circle 22 on Inquiry Card.
For a demonstration,
circle 23 on Inquiry Card.

TEKTRONIX LOGIC ANALYZERS THE VERSATILE ONES

For immediate action, dial our toll free automatic answering service: 1-800-547-1512

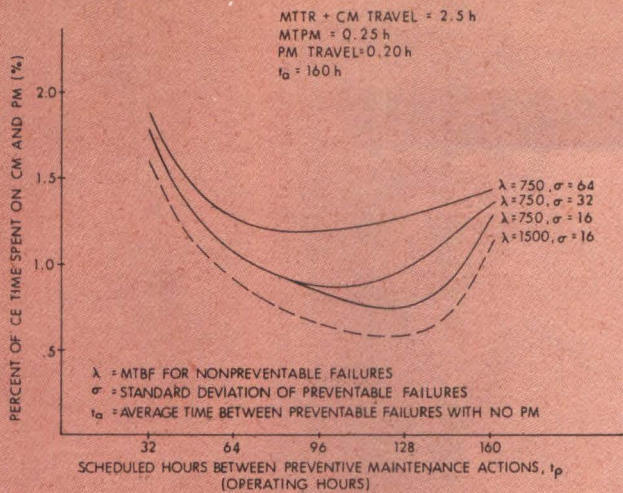


Fig 3 Percent CE time vs scheduled PM interval showing effect of differing values of σ and λ . Three solid lines describe device with MTBF λ of 750 h for nonpreventable failures; dashed line shows that change in MTBF for nonpreventable failures has no material effect on optimum PM interval

to the site after a failure has occurred, the device is out of service for the user. However, the device can of course be used during the time the CE is traveling to the site to perform PM. Therefore, percent downtime for the customer is equivalent to the percent CE time spent, if PM travel time is zero. The bottom curve in Fig 4 shows that the value of t_p which minimizes customer downtime is different from that which minimizes CE time and cost.

Fig 5 shows that an increase in MTR + CM travel time has the effect of reducing the optimum PM interval, for a given value of σ . Solid lines show percent CE time for

MTR + CM travel of 3.5 h, compared with 2.5 h for the dotted lines.

Conclusions

A manufacturer's first objective should be to design and manufacture reliable equipment (MTBF large) and to conduct maintenance efficiently (MTR + travel times small). If preventable failures cannot be eliminated, they should be infrequent (t_a large) and predictable (σ small).

To establish an optimum time interval for PM, a manufacturer must collect data on the distribution of prevent-

The
paper tiger
is coming.
In 30 days.

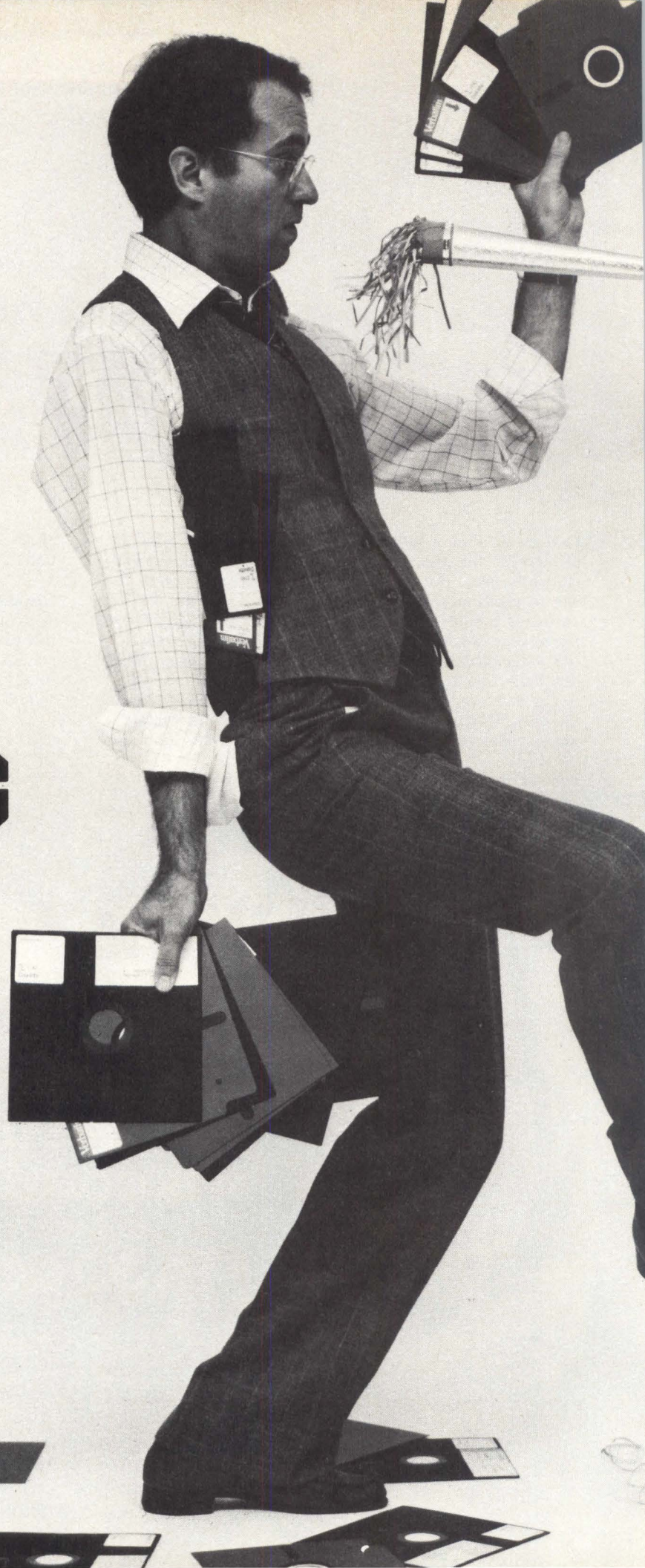
A smart new impact. With big-machine versatility no other compact printer can match. 80 to 132 columns. Variable width. Business forms. Selectable character sizes. Multiple copies. Tractor feed. Graphics. And much more.

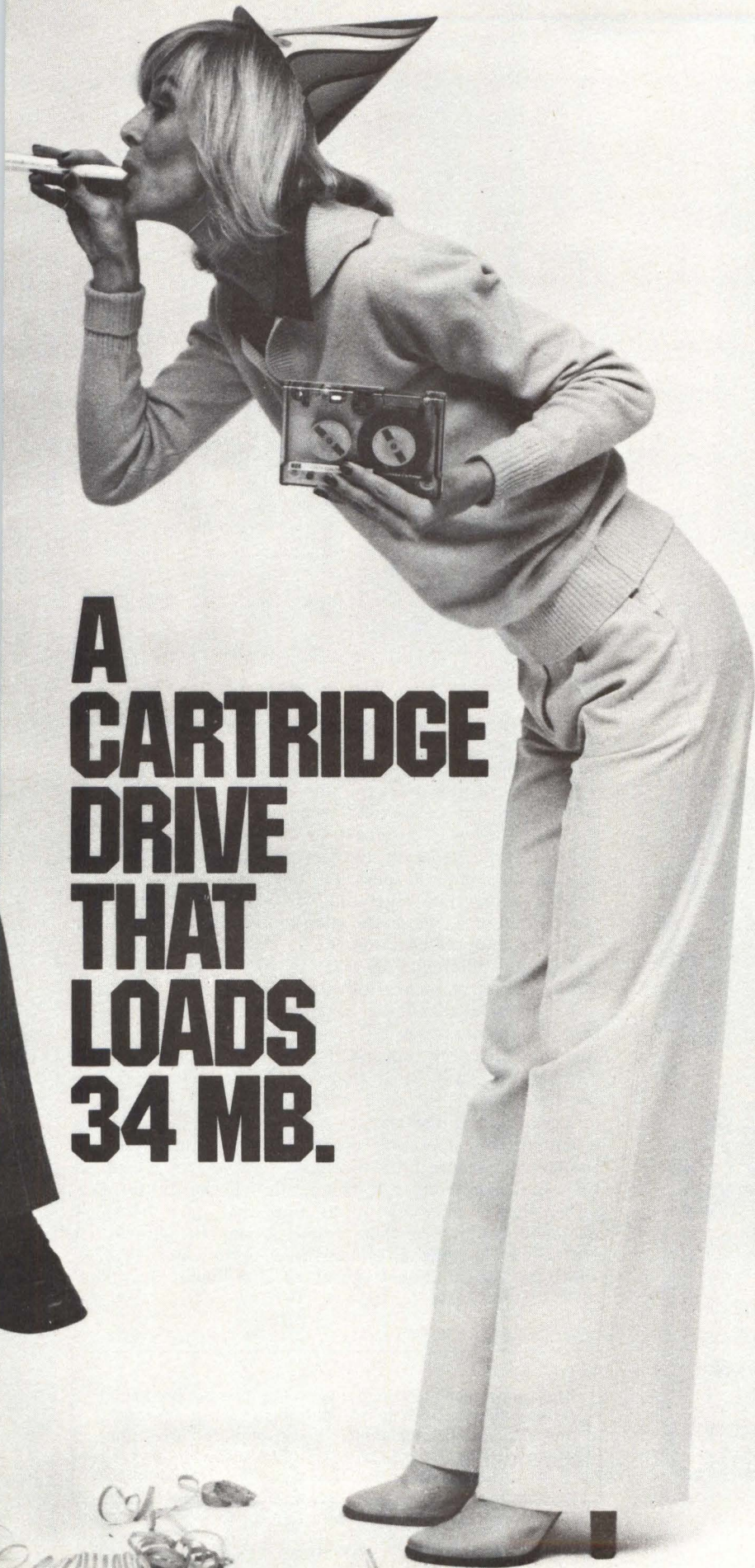
Take it from the leader in low-cost printers. This is one paper tiger that will deliver. Find out for yourself at Interface '79, April 9-12, (Booth #1033)



Integral Data Systems, Inc. 14 Tech Circle, Natick, MA 01760 (617) 237-7610

**HEY
DISK
JOCKEY,
WE'RE
CELEBRATING
SOMETHING
NEW TO
BACKUP
YOUR
WINCHESTER
DISKS.**





A CARTRIDGE DRIVE THAT LOADS 34 MB.

If you've been trying to backup Winchester disks with floppies and your file is beginning to look like this week's top 40, lend us your ears.

DEI's new 34 M Byte High Density Microtape™* Cartridge Drive is the latest development in the Funnel Series. It has as much capacity as 34 double density, double sided floppy disks, and 48% more capacity than an 800 bpi ½-inch reel-to-reel drive with 2,400 ft. of tape.

The 7,200 bpi, ¼-inch cartridge tape drive accomplishes this remarkable technical breakthrough by recording 7-tracks in GCR or MFM code at up to 10,000 FRPI and can transfer at the rate of 216 Kilobits/second.

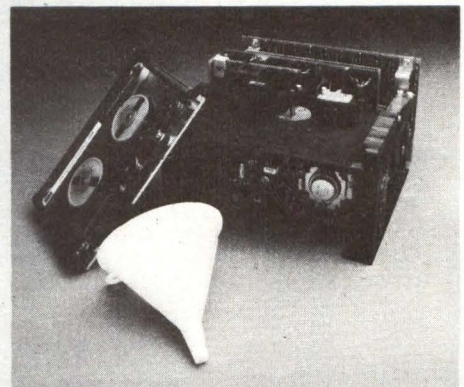
Put Microtape Drive performance together with small size (it's just 7-inches wide, 5¼-inches deep, 4¼-inches high and weighs 4 lbs.) and you'll have another reason to specify.

To top it all, there's DEI's experience with over 6,000 High Density cartridge tape drives in the field. In fact, our 17.28 MB Microtape drive has become an industry standard for Winchester disk save and restore.

So join the celebration and try our new High Density Microtape drive with your minicomputer system. Your customers will be tooting a tune that's music to your ears.

Write Data Electronics, Inc.
370 N. Halstead St., Pasadena
California 91107

Or call (213) 351-8991, Telex 67-5327.



DEI MICROTAP CARTRIDGE DRIVE

CIRCLE 24 ON INQUIRY CARD

*Microtape is the DEI name for its ¼-inch cartridge tape drives.

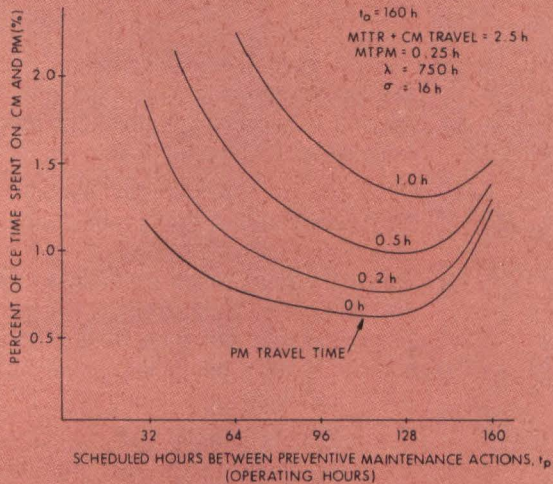


Fig 4 Percent CE time vs scheduled PM interval showing effect of PM travel time. Bottom curve shows downtime as seen by user

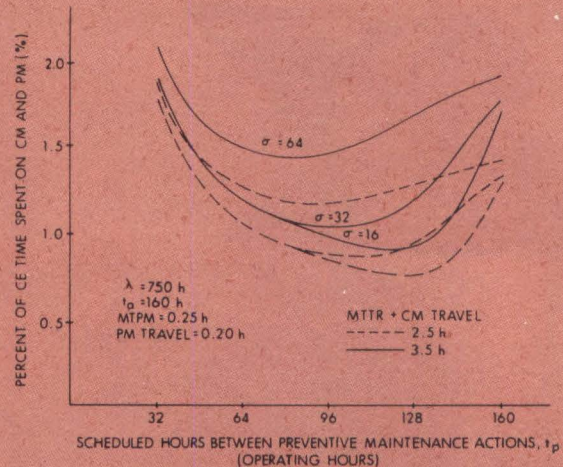


Fig 5 Percent CE time vs scheduled PM interval showing effect of MTRR (and travel time) for non-preventable failures. Optimum PM interval is reduced by increase in MTRR + CM travel time, for given value of σ




“THE FIRST KEYLESS LOCK IN CHIP FORM.

NOW YOU CAN MAKE A DIGITAL LOCK AS TINY AS THE DIGITAL KEYBOARD.

The new LS7220 Keyless Lock is in a 14-pin DIP. You'll slash production costs with reduced wiring, QC, stocking, handling, and boost reliability, marketability. 5,040 4-digit combinations, out-of-sequence detection logic, 25 μ A on standby. \$1.25 (1,000) quantity, from stock. Call me at 516/271-0400 and I'll tell you more goodies.

LSI COMPUTER SYSTEMS INC. 

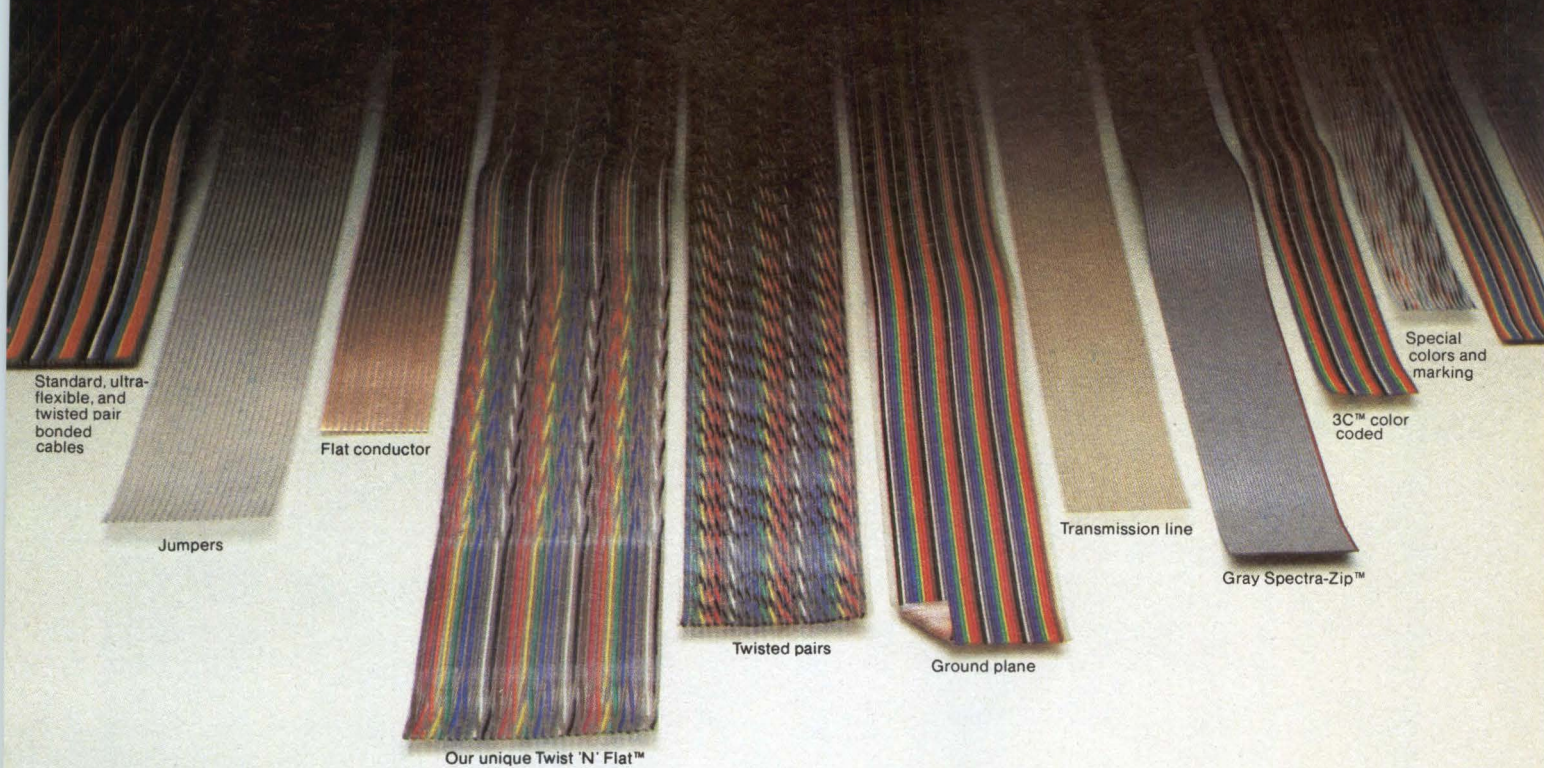
Manufacturers of Custom and Standard LSI circuits.

Ron Colino
VP/Marketing,
1235 Walt Whitman Rd., Melville, NY 11747
516/271-0400. TWX: 510-226-7833

able failures with time. Specifically, enough data must be available to estimate t_a and σ . Given statistical data on failures, the optimum PM interval can be determined as a function of the average time it takes a CE to repair failures, the time required to conduct PM (MTPM), and the time necessary to travel to the customer's site. The optimum time generally lies between 0.5 and 0.75 of t_a , the average interval between preventable failures. Increases in PM time (including travel) increase the optimum value of t_p ; increases in CM time (including travel) decrease the optimum value of t_p .

A small difference in percent CE time can have a significant effect on maintenance efficiency. If 70% of a CE's time is available for maintenance actions (PM and CM), 70 devices can be serviced, if 1% of his time is required for each, but only 64 devices if 1.1% of his time is required for each. It is therefore worthwhile to choose the optimum t_p for each device requiring PM. On the other hand, it is also wise to remember that the optimum is an unstable operating point; if the CE, through carelessness or because he is too busy, postpones a scheduled PM (thus increasing t_p), the result will be an increase rather than a decrease in the time that must be spent on maintenance. For that reason, it may be wise to set PM schedules with a t_p less than optimum—a strategy which has the additional advantage of reducing downtime.

The Author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in further articles.—Ed.



When it comes to flat, we've been around.

We make more different kinds of planar cables for more different kinds of interconnect systems than anyone on the planet Earth. And, in this world of planar-comelately's, Spectra-Strip has been around since the cable world turned flat.

For all your interconnect needs from planar cables to IDC connectors to complete custom assemblies, just check us out. We'll take total responsibility for solving your interconnect problems, and you won't need to call anyone else.

For the name and number of our nearest distributor or rep, write Spectra-Strip, an Eltra Company, 7100 Lampson Avenue, Garden Grove, CA 92642. Or call (714) 892-3361 today.



When you're down to the wire

CIRCLE 26 ON INQUIRY CARD

2,500,000 BYTES.



IBM COMPATIBLE { **ALL NEW**
DOUBLE SIDE
DOUBLE DENSITY } CONTROLLERS

STILL THE SMARTEST
NOW FOUR TIMES THE STORAGE

SMS MAKES FLOPPY STORAGE GROW.

MINIFLOPPY CONTROLLERS

Dual Head/ Double Density

Integrate the new dual head mini-floppy drives into your system with the new SMS FD0507-M double density controller:

- Provides up to 322K bytes of storage/diskette. (That's more than a single density, standard-size diskette!)
- Supports up to 3 dual head mini-floppy drives, including the Shugart SA 450. (Almost 1M bytes of storage!)
- Complete controller on compact 5¾" x 9½" PC board requires only +5 volts. (Mounts directly on disk drive!)
- Proprietary phase lock loop design provides industry's most reliable double density formats. (Fewer data recovery errors!)
- Easy interface to industry standard microprocessors, including INTEL 8080. (Both DMA and Programmed I/O can be accommodated.)

STORAGE SYSTEMS

IBM { Single + Double } Density

Our new storage systems feature:

- 2,500,000 bytes of IBM Diskette 2/2D double density compatible storage in a single low profile package. (Requires only 5¼" of standard rack space.)
- Both IBM 3740 single density and IBM Diskette 2/2D double density formats. (Guarantees diskettes are interchangeable with other systems.)
- Choice of single head or dual head disk drives. (Optimize storage capacity and cost to meet your needs.)

FLOPPY CONTROLLERS

IBM { Single + Double } Density

The new FD0500: now compatible with the IBM double density standard.

- Both IBM 3740 single density and IBM Diskette 2/2D double density formats. (Guarantees diskettes are interchangeable with other systems.)
- Supports up to 4 single or dual head floppy drives. (5,026,816 bytes of storage!)
- Complete controller on compact 8¾" x 14" PC board (Mounts directly on disk drive.)
- Proprietary phase lock loop provides industry's most reliable double density formats. (Fewer data recovery errors!)
- Simplified interfacing to industry standard microprocessors including INTEL 8080. (Both DMA and Programmed I/O can be accommodated.)



FEATURING THE HIP™

The HIP (Host Interface Processor) is an intelligent DMA controller which is plug compatible with LSI-11*, PDP-11* and Nova** minicomputers. It is available with a complete storage system or as a controller only.



SCIENTIFIC MICRO SYSTEMS
777 East Middlefield Road
Mountain View, CA 94043
(415) 964-5700
(TWX) 910-379-6577

* Trademark of Digital Equipment Corp.

** Trademark of Data General Corp.

CIRCLE 27 ON INQUIRY CARD

- I have an immediate requirement. Have an applications engineer call me.
- My new product requires a floppy system. Send me literature.
- My new product requires a controller. Send me literature.
- I'm a literature collector. Send me information for my files.

My host system is

- RS232C Microcomputer PDP-8 LSI-11 NOVA
- PDP-11

ESTIMATED YEARLY QUANTITY

- 1-14 15-49 50-100 100+

Name _____

Company _____

Address _____

City _____ State _____ Zip _____

We've Earned Our Stripes

With The Only Plug Compatible Microprocessor I/O System In The Industry

Opto 22 combines the latest and best in I/O modules with plug compatibility to single board computers. Opto 22 I/O Systems are available in plug compatible racks holding eight, sixteen or twenty-four modules. These highest quality Input/output modules are available for 5, 15, or 24-volt logic—all employing 2500 volts RMS photo-isolation.

Simplified installation and maintenance are important features of the systems. Barrier-type screw terminals, LED status lights, pull-up resistors and plug-in fuses are mounted on the racks. Changes and replacements are easily made without removing wires.

Because we concentrate solely on photo-isolated SSR's, you get quality, reliability and innovation at the best prices.

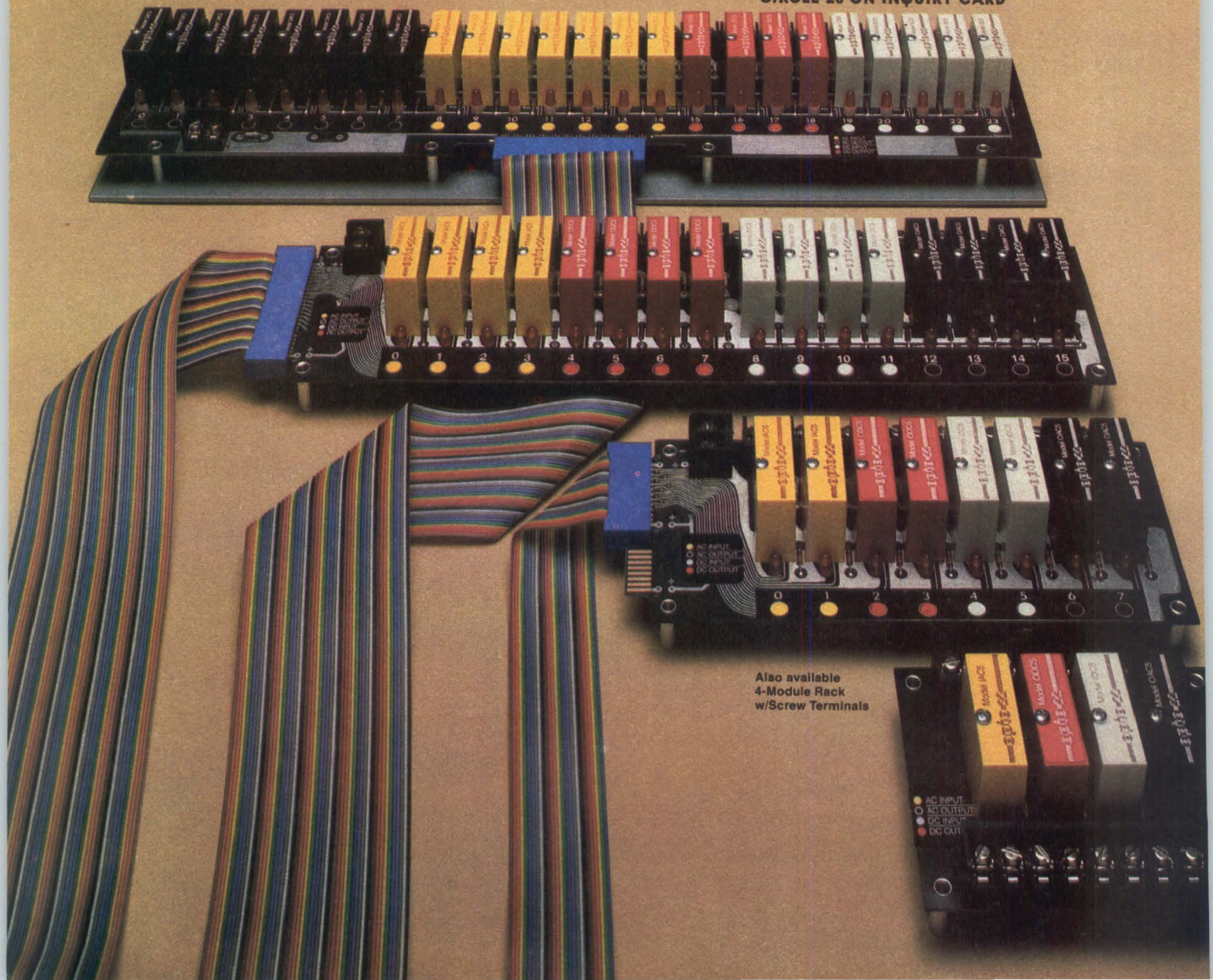
Plug compatibility with:

- | | |
|--|---|
| <input type="checkbox"/> Intel | <input type="checkbox"/> General Automation |
| <input type="checkbox"/> Motorola | <input type="checkbox"/> Iasis |
| <input type="checkbox"/> Burr-Brown | <input type="checkbox"/> Mostek |
| <input type="checkbox"/> Computer Automation | <input type="checkbox"/> National |
| <input type="checkbox"/> Control Logic | <input type="checkbox"/> Texas Instrument |
| <input type="checkbox"/> Data General | <input type="checkbox"/> Western Digital |
| <input type="checkbox"/> Digital Equipment Corporation | <input type="checkbox"/> Zilog |



5842 Research Drive, Huntington Beach, CA 92649, (714) 892-3313

CIRCLE 28 ON INQUIRY CARD



Also available
4-Module Rack
w/Screw Terminals

- AC INPUT
- AC OUTPUT
- DC INPUT
- DC OUT

Parallel Processor Will Be Capable Of Performing 6G Additions/s

An ultra-high speed data processing system being developed at NASA Goddard Space Flight Center will process images and 2-dimensional data, performing approximately 6G additions and subtractions or 2G multiplications/s. The Massively Parallel Processor (MPP) is being designed by Goodyear Aerospace Corp, 1210 Massillon Rd, Akron, OH 44315 under Phase I of a contract with the NASA Goddard Space Flight Center in Greenbe't, Md.

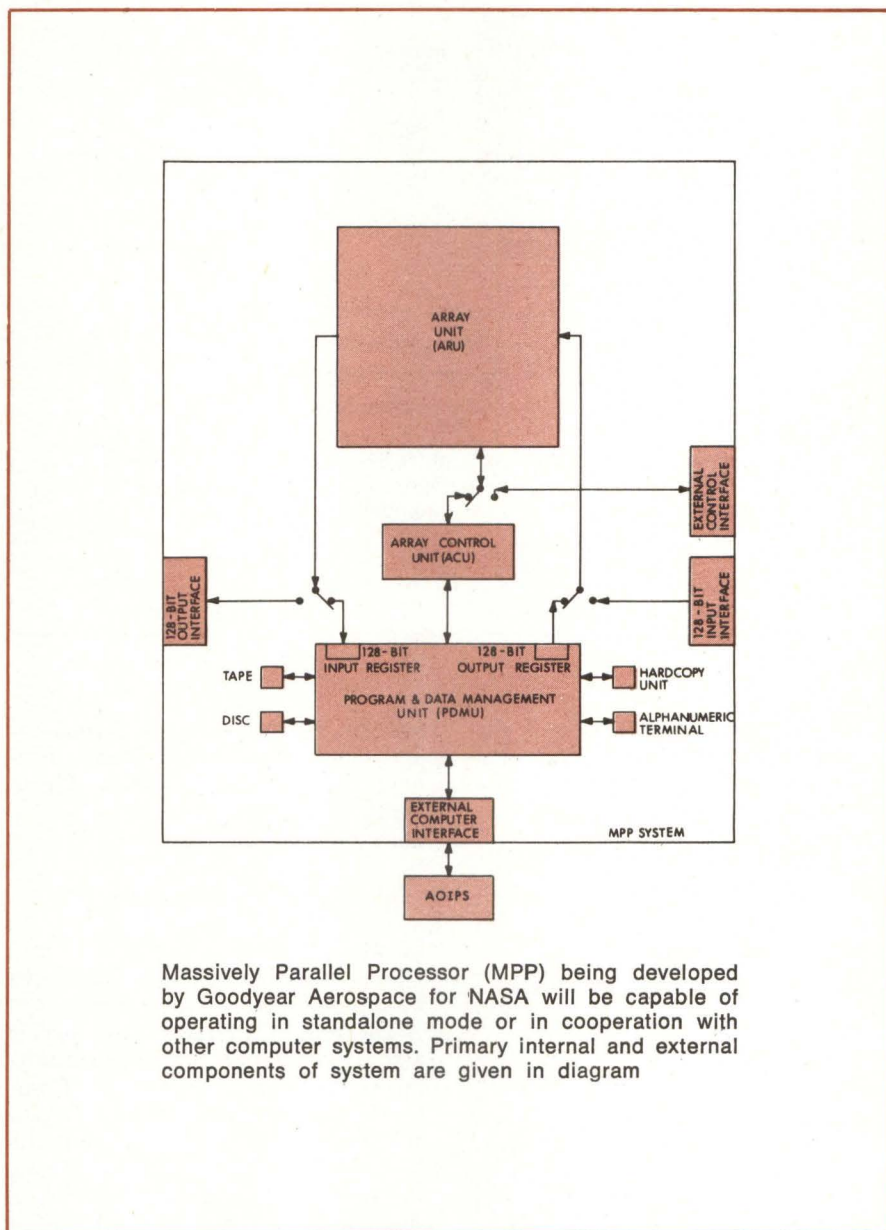
The MPP consists of an array unit, array control unit, and program and data management unit. A central control unit provides identical control signals and memory addresses to each processing element. One interface is provided to an external data processing computer; two interfaces allow direct access to the array unit.

Consisting of 16,384 processing elements (PEs) in an 128 x 128 array, the array unit functions as a single instruction multiple data stream computer and is the computational center of the system. An array control unit (ACU) supplies the array unit (ARU) with instructions for execution at a 10-MHz clock rate. To provide the maximum operation rate possible, the ACU design applies microprogramming techniques and allows as many overlapped operations as possible in one instruction cycle.

Managing data flow between ACU, ARU, and peripheral devices, the program and data management unit (PDMU) loads programs into the ACU, provides data to the ARU, displays results, executes system diagnostics, and manages all data flow and interfaces within the system. 128-bit I/O data registers allow data transfer at a rate of 128 bits/10 ns.

Packaged on LSI chips, every PE in the processing array has three basic constituents: arithmetic, logic, and routing unit, with a 4-neighborhood PE interconnection for routing data; memory unit composed of 256 bits of RAM; and I/O unit containing one bit of storage with connections for left-to-right 128-bit parallel I/O data transfer. Components within the PE communicate with each other through a bidirectional data bus.

Arithmetic is performed on variable word length integer or floating

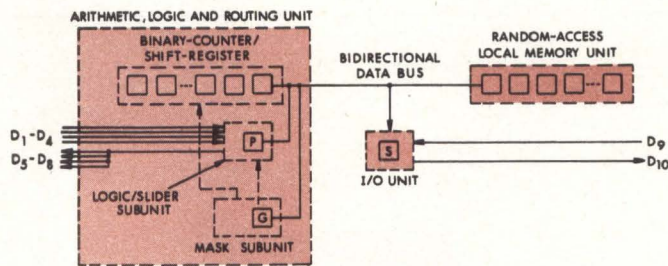


Massively Parallel Processor (MPP) being developed by Goodyear Aerospace for NASA will be capable of operating in standalone mode or in cooperation with other computer systems. Primary internal and external components of system are given in diagram

point operands. Operations are based on a design consisting of 16-stage binary counter (which downshifts the lowest bit to the data bus), logic processing component, and mask component. The counter downshift function changes weights of digits in sum, product, and cross-correlation function during computations. Sum of operands is formed by using the two lowest stages of the counter as a full adder. This bit-serial arithmetic unit is extremely efficient. Estimated performance in integer arithmetic op-

erations is 3.6G 8-bit add/subtract operations/s or 1.8G multiplies/s. In performing 32-bit floating point operations, the machine should be capable of 416M add/subtracts or 216 multiplies/s.

When installed at NASA-Goddard during Phase II of the contract, the machine will provide the speed necessary to process earth data received from satellites, performing the same operations simultaneously on all pixels (picture elements). Such data when processed become color images



DATA PATHS:
 D₁-D₄ FROM FOUR NEIGHBORHOOD PE'S
 D₅-D₈ TO FOUR NEIGHBORHOOD PE'S
 D₉ FROM LEFT NEIGHBORHOOD PE
 D₁₀ TO RIGHT NEIGHBORHOOD PE

Packaged on LSI chip, each of 16,384 processing elements in MPP consists of these components. Binary-counter/shift register serves as the primary computational unit within the system

of the earth with one pixel typically representing one acre of ground viewed by the satellite's image scanner. These data are becoming increasingly valuable to scientists for

use in analysis and prediction of agricultural crop yield, urban planning, pollution monitoring, and geological exploration.

Circle 370 on Inquiry Card

Data Bus Standard Contains Expanded Specs, Clarifications

Initially published in 1975, IEEE Std 488 provides a standardized interface that permits system components in close proximity to communicate over a contiguous party line bus. While the technical concepts defined in IEEE Std 488-1975 remain, the revised IEEE Std 488, Standard Digital Interface for Programmable Instrumentation, published by the Institute of Electrical and Electronics Engineers, Standards Office, supplies additional information and some changes for clarification.

Supplementary information is provided concerning system controller guidelines, devices powered on and off, serial poll, parallel poll configure, interface function capability identification, and data rate consideration for high speed operation. Some tables and figures have been modified, notes have been added to

further explain conditions and provisions, and some specifications have been broadened.

The revised standard is in concert with its international counterpart, International Electrotechnical Commission Publication 625-1. Copies are available at \$10 each from the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. Price of a single copy for the personal use of IEEE members is \$9. A \$2 shipping and handling charge must be included with each order.

Ink Jet Printing System Produces Range of Fonts at 50,000 Lines/Min

An ink jet printing system that forms images at the rate of 48,000 char/s, the **DIJET**® (direct imaging by jet ink transfer) system produces as many as 50,000 lines/min on a

moving web of paper, printing data from a computer tape. The system from Mead Digital Systems, Inc, 1771 Springfield St, Dayton, OH 45403 provides the speed and flexibility needed to print a range of font styles and graphics on various paper stocks at the speed of a printing press.

The system depends on two principles of physics. When any liquid is forced through a small opening, the exact size and interval of drops can be regulated precisely by ultrasonic stimulation. When this occurs, droplets can be given an electrical charge, or can be left uncharged. These droplets are then moved through a deflection field where uncharged droplets are allowed to print, and charged droplets are returned to an ink recirculation system. Each uncharged drop of ink forms part of a character or symbol.

The technique used relies on an imaging head or bar that has as many as 1280 individually controlled ink jets, each producing more than 50,000 uniform evenly spaced ink droplets/s. Each jet is linked through the system electronics and the minicomputer back to the magnetic tape which serves as the data source.

Key to the technique is a Foto-ceram glass-ceramic charge plate produced by Corning Glass Works, Corning, NY. Made of photosensitive glass, the plate has precisely positioned and shaped holes through which the ink jets are directed. The plate is nonconductive but carries a metal covering.

After the jet has been formed and broken up into droplets by ultrasonic energy, some of the droplets are charged electrically. These charged droplets are then deflected by the charge plate into a catcher for return to an ink reservoir. Uncharged droplets continue onstream until they strike the paper.

Measuring about 0.006" (0.152 mm) in diameter, the droplets pass through cylindrical tunnels 0.012" (0.305 mm) in diameter and 0.050" (1.27 mm) long that serve as charge electrodes. Electrical leads link each opening in the charge plate to the image head electronics and carry programmed commands to the image head.

Directly above the image bar, a command console panel provides a number of controls and indicator lights to facilitate system operations. The panel gives the operator control of the printing process and is located to allow the operator to see images as they are formed and thus

Double Density Floppies for your LSI-11/2

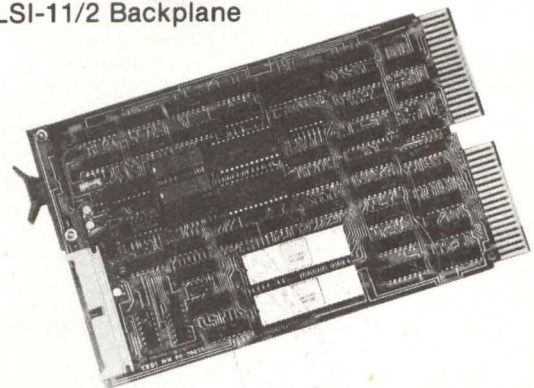
The FD-211 Dual Floppy System is the perfect plug replacement for your RX02 . . . In half the space . . . and at up to 30% savings.



- 5¼" Low Profile Chassis
- Dual Shugart Drives
- 512K Bytes Per Drive
- Front Panel Write Protect Switches
- Photocell Write Protect
- Complete Instruction Manual

CRDS continues its spectacular performance in the field of Peripheral Controller Design. Designing control/interface electronics onto a single Dual Height Card and with:

- Single and Double-Density Operation
- Complete Instruction Set
Compatibility with RX02
- Integral Bootstrap Loader
- Built-In Self Diagnostic, Formatter
- Dual Height Controller for LSI-11 or LSI-11/2 Backplane



Our MF-211 Dual Floppy/LSI-11 System does everything the PDP-11 V03-L will do . . . for a lot less.

Check These Features:

- Single and Double-Density Operation
- Complete RX02 Instruction Set Compatibility
- Over One Megabyte Storage Per System
- Functionally identical to the DEC PDP-11V03-L
- 10½" Rack Mountable Enclosure
- Available with DEC Software and Interface Cards
- 30K Addressable Memory
- Considerable Dollar Savings

Our MF-211 Dual Floppy/LSI-11/2 System, using the CRDS Double-Density Controller is functionally identical to the DEC PDP-11V03-L, however using only 10½" rack space. The MF-211 is the perfect low-cost answer to your PDP-11V03-L requirement.



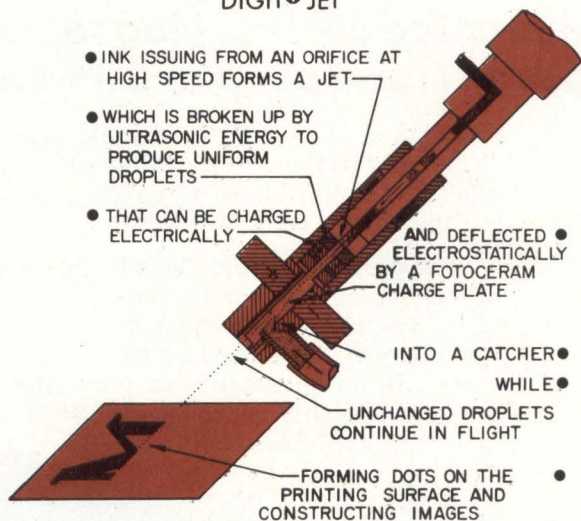
For more info on our FD-211 and MF-211 Double-Density Floppy Disk Systems, just call or write:

Charles River Data Systems, Inc.,

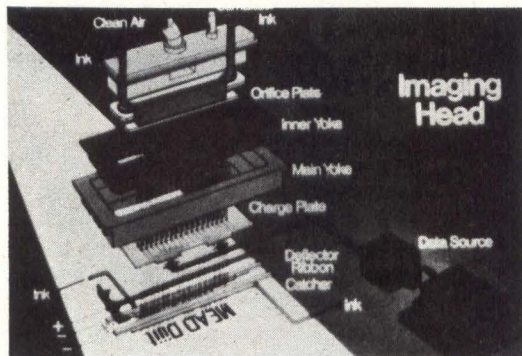
4 Tech Circle, Natick, Massachusetts 01760 Tel. 617 655-1800



DIGIT® JET



Components of Mead's ink jet printing system include Fotoceram glass ceramic charge plate containing 512 holes through which streams of ink are directed. Droplets in each stream can be deflected on command to ink reservoir or allowed to impact on printing surface



Flow of single ink jet is tracked through ink jet printing system. Electrical signals from computer to image head determine whether droplet travels to paper surface or is deflected back into system

to make fine adjustments for registration and print quality.

Other system components include a specially designed paper transport with dryer (the imaging system also has the flexibility to mount on a customized paper transport). A keyboard terminal allows communication with the data subsystem, permitting the operator to test fonts and obtain the status of data being printed. The terminal can also be used as a diagnostic tool.

Operating instructions and data are entered into memory through the tape unit. Dual tape drives are de-

signed to operate at high speeds and enable continuous printing on long production jobs.

Operator control panel and minicomputer are housed in the data station. The minicomputer stores fonts, takes data from the tape unit, and translates them into digital signals which are sent to the imaging bar. An ink cabinet houses a closed loop fluid system as well as power control and fluid control panel. The closed loop system cleans itself and gives maximum value by recycling ink for reuse.

Circle 372 on Inquiry Card

Large-Scale Computer Offers 128M-Bit Main Memory Capacity

Cyber 203, a supercomputer class machine, succeeds the STAR 100 and provides significant performance improvements over its predecessor. Contributing to these are a conventional—or scalar—processor that is six times faster, central memory with capacity for up to 2M words, memory bandwidth sufficient to transfer data at rates up to 100G bits/s, and substantial reduction in parts count through the use of LSI circuits.

Other major attributes of the machine, developed by Control Data Corp, Box O, Minneapolis, MN 55440, are its virtual memory mechanism and paging concept, and the 819-21 disc storage unit. Design features include vector stream processing (up to 100M results/s), separate scalar and array processing units, and functional units designed for sequential and parallel operations on single bits, 8-bit bytes, and 32- or 64-bit floating point operands and vectors. Vector addressing uses a high speed mapping technique for converting a logical address to an absolute storage address.

Based on vector architecture, the system's processing and I/O facilities are well suited to solving complex physical and mathematical problems. Complementing the architecture is a high speed scalar processing unit, wide bandwidth semiconductor memory, and broadband overlapped I/O system.

Scalar instructions are fully compatible with vector stream processing operations and complement the vector instructions. Independence of the functional units allows several operations to be performed in parallel. To reduce transfer delays, the scalar processing unit is located in a cabinet attached to the central memory. The processor is made up of 16 boards [each less than 1 ft (0.305 m) square]. Each board has 15 layers and accommodates 150 LSI chips, and operates with a 20-ns cycle time. An instruction stack and 256-register file allow rapid processing by minimizing accesses to memory.

Consisting of two vector pipelines—a stream unit and a string unit—the vector processor is capable of performing 100M floating point operations/s. The stream unit contains

A PART THAT SETS US APART

The Dual Density Databoard

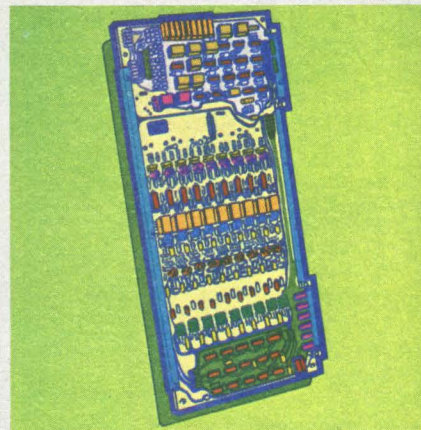
With the Series 900X vacuum column tape drives—both 75 ips and 125 ips models—Cipher Data Products introduces a state-of-the-art databoard that provides data electronics performance unmatched in the industry.

The databoard, on only one card, is 100% industry compatible, handling NRZI or PE formats selected through the interface or from the front control panel. This multi-function board features plug-in headers for speed selection and is usable on all other Cipher products, therefore, spares costs are significantly reduced for the user.

In comparison with competitive units this new databoard provides increased reliability—with a 40% reduction in total parts count, improved PE resolutions, low noise generation and pickup, a 50% lower power consumption, and the elimination of troublesome write deskew alignments. In addition, self test through special diagnostic and alignment modes can be accomplished without the use of external equipment.

Now look at all the other parts—like the Z-80 microprocessor, beltless direct drive, switched linear servo system, optical file protect and modulated tape sensor system. The Series 900X vacuum tape drive is far ahead of the market in design while still fully compatible with today's industry standards.

Do your part. Call for full information and OEM quantity price competitive quotes. Cipher Data Products, Inc., 5630 Kearny Mesa Road, San Diego, California 92111, (714) 279-6550.



Cipher
Data Products

CIRCLE 30 ON INQUIRY CARD

Who's first to put COBOL on a micro? Zilog, of course.

**Building computer systems for business?
Now you can use the latest Z-80[™]
microprocessor technology—without giving
up the benefits of COBOL.**

Now you can keep on programming in COBOL, just like you always have. Zilog's powerful new MCZ series of microprocessors let you compile and execute standard COBOL programs with performance and features that equal—even exceed—the COBOL capabilities of most minis.

Zilog's MCZ-1 series supports the 1974 ANSI X3.23 COBOL. It has been enhanced for use in the microprocessor environment with special display-oriented features.

Included are: a debug facility that provides interactive program development; sequential files; random files;

program segmentation; library; interprogram communication; 18-digit decimal and binary data types.

Zilog's MCZ-1 family also gives you the option of BASIC, FORTRAN and Zilog's dual-level PLZ. All are fully supported under Zilog's powerful RIO operating system.

The family an OEM can love.

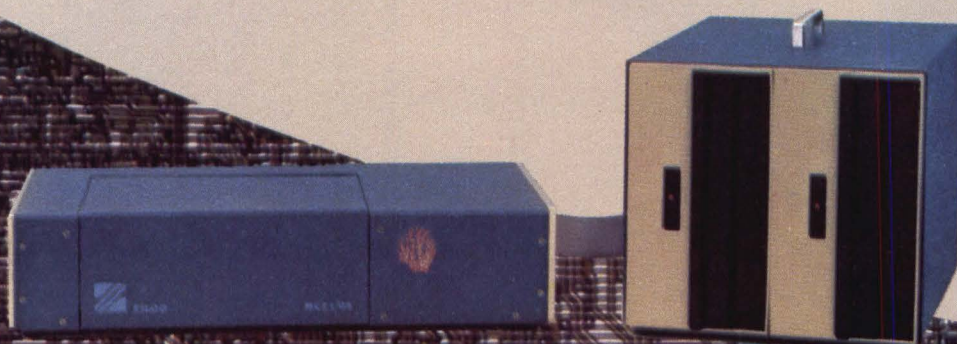
Zilog's MCZ-1 family has the compatible hardware options you need for almost any system configuration.

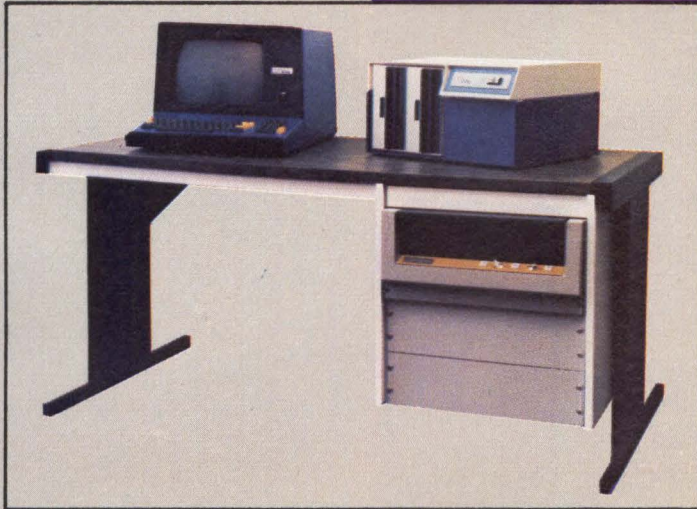
You can go for price with the exceptionally low-cost MCZ-1/05. This system features a table-top unit with

two floppies, RS232 terminal interface, 60K of memory—and lots of room for I/O expansion.

Move up in performance with a system like the MCZ-1/35, a moving-head disk system with two Z-80s, a file management system right in the control unit and the ability to support up to four cartridge disk drives.

Go any direction you need to with the general purpose MCZ-1/20. Or, select from rack-mountable units, table-top units, units with CRT's, units with a variety of disks—configurations to fit just about any product development strategy.





No waiting. Available now.

What else would you expect from Zilog—the company that's pledged to stay a generation ahead in micro-computer design? In OEM quantities, systems are available with only 30-day deliveries. We'd be glad to answer your letter asking for more information.

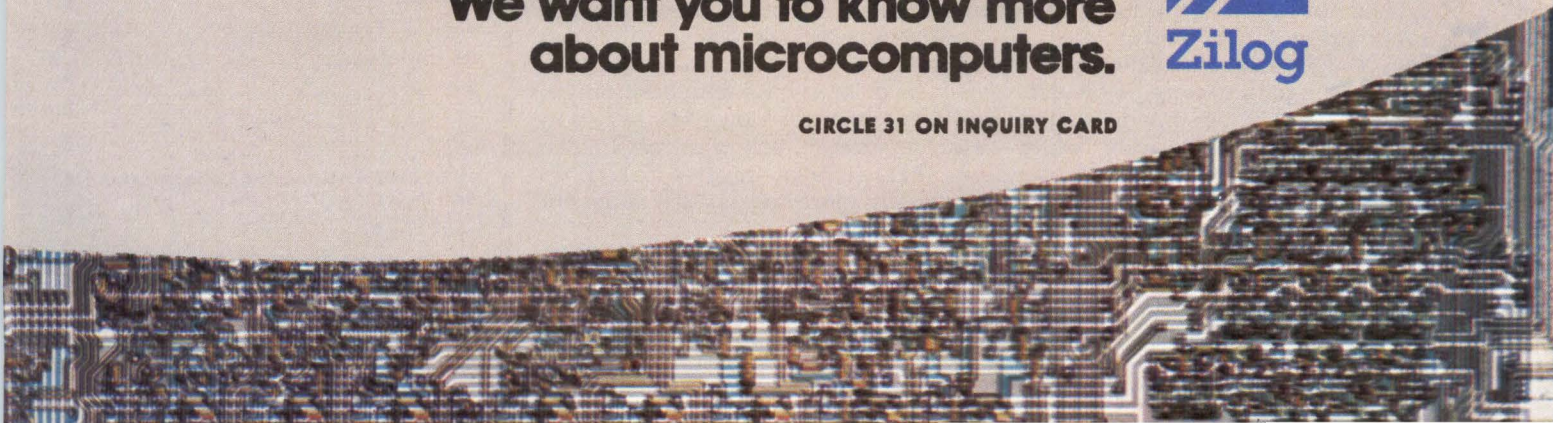
10460 Bubb Road, Cupertino, California 95014
(408) 446-4666 TWX 910-338-7621
EASTERN REGION: (617) 667-2179
MIDWESTERN REGION: (312) 885-8080
SO. WESTERN REGION: (714) 549-2891
NO. WESTERN REGION: (408) 446-4666
JAPAN: 03-476-3010
EUROPE (ENGLAND): (0628) 36131/2/3
WEST GERMANY, GMBH: (8106) 4035

An affiliate of
EXON ENTERPRISES, INC.

**We want you to know more
about microcomputers.**



CIRCLE 31 ON INQUIRY CARD





New Developments for Research Computing...

The New MOS Packaged Systems.

Until now, you've either had to forego 16-bit pricing to get 32-bit performance, or you've had to give up 32-bit performance just to keep the budget in line.

No longer. Now you can invest in a full-blown 32-bit computer system and pay no more than you would for a 16-bit computer. And not have to worry about insufficient power for future needs.

Here's why: value engineering. We've taken our high-performance 32-bit computers, and we've done some packaging that makes sense. We've added MOS memory. Expanded and fine-tuned our operationally-proven software. Made our systems more compact, more efficient.

And we put it all together for a third less money.

The result? A broad family of 32-bit computer systems, perfect for jobs that require high thruputs like telemetry, seismic exploration, or research. Or for jobs that need lots of I/O; process control, simulation, or laboratory automation.

All are upward-compatible, so you can still grow, but start with minimal investment.

If you'd like to have real performance, but can't overlook how effectively you use your budget, talk to us. We'll make sure that when you invest in SYSTEMS computers, more dollars will flow to your bottom line.

For more information about SYSTEMS, complete and return the coupon or call us toll free, at 1-800-327-9716.

SYSTEMS

Proven COMPUTER Performance

- Have a representative call me.
 Send me a detailed technical summary
 I plan to purchase in approximately _____ months.

Name _____ Title _____

Company _____

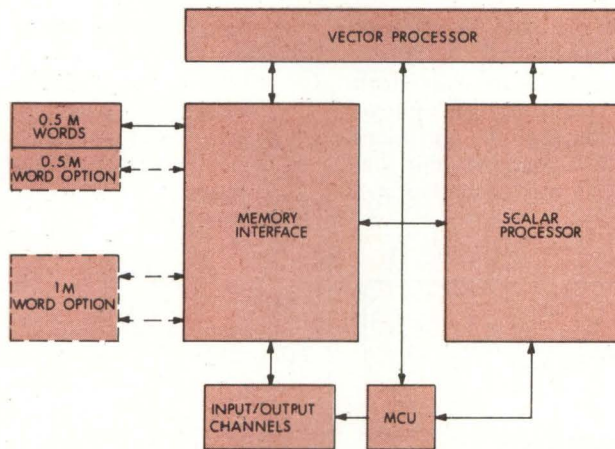
Address _____

City _____ State _____ Zip _____

Phone _____

SYSTEMS Engineering Laboratories
 6901 W. Sunrise Blvd.
 Ft. Lauderdale, FL 33313
 (305) 587-2900

71



Control Data's Cyber 203, incorporating LSI ECL logic circuits and 2M-word bipolar main memory, is capable of performing scalar computations six times faster than its predecessor and of completing 100G vector calculations/s. Complementary features are 100G-bit/s memory bandwidth and overlapped I/O system

vector instruction and streaming execution control. The unit manages data streams that connect directly between central memory and vector pipelines. The string unit processes strings of decimal and binary numbers and performs all bit string operations. It also serves as the processing unit for control vectors during floating point streaming operations. It contains the facility for BCD and binary arithmetic, zoned BCD processing, address arithmetic, and Boolean operations.

Input and output are handled primarily by peripheral stations, with the mainframe containing instructions to initiate I/O and process external interrupts. Central memory is a single-level unit made up of 1k bipolar ICs. Memory words are 78-

bits long to provide a 64-bit data word with seven bits for error detection and correction. Memory access time is 80 ns.

Twelve data channels provide 16-bit wide data paths between peripheral stations and storage access control and allow transfers to occur at 5M 8-bit bytes/s. Memory bandwidth allows all 12 channels to be active at this rate simultaneously, while supporting three vector streams at 100M operations/s.

Prices range from \$5.8M for a basic mainframe with 500k 64-bit words of memory to \$11.7M for a total system with mainframe, peripherals, Cyber 170 frontend, and software. All software available for the STAR 100 is usable on the system.

Circle 373 on Inquiry Card

Minicomputer Systems Gain Performance Through 32-Bit Architecture

Cache memory, high speed mos main memory, 32-bit architecture, and extensive microprogrammed logic are

common to the central processors of the 450, 550, 650, and 750 systems introduced by Prime Computer, Inc, 40 Walnut St, Wellesley Hills, MA 02181. All systems use these common features to provide increasing levels of performance, together with the

responsiveness of a minicomputer and capabilities of a mainframe.

Most powerful system and competitive with DEC's VAX-11/780, the 750 gains speed and flexibility from a 16k-byte cache memory, instruction prefetch buffer, burst mode I/O, interleaved memory, and floating point unit. The 16k-byte cache has a 95% hit rate on processor information requirements, dramatically reducing instruction execution times and processor overhead. An instruction prefetch unit further enhances performance by prefetching and decoding up to four instructions from cache memory. Accessing cache independently of the processor, the unit forms the effective address in parallel with instruction execution. Thus the next sequential instruction is always ready for the processor.

A 32-bit memory bandwidth speeds cache operation by allowing high volume data transfers to and from memory and cache. Interleaving of memory provides high speed data transfer between memory and CPU by allowing the processor to read or write four bytes at a time. Using burst mode I/O, this interleaving offers 64-bit data transfers, increasing throughput by providing an 8M-byte/s transfer rate between processor and peripheral controllers.

The floating point unit has a 32-bit path to the processor, fully utilizing the 32-bit architecture. An expanded hardware-implemented business instruction set offers fast decimal arithmetic, and a 32-bit arithmetic unit provides fast integer arithmetic.

An economical medium-scale system, the 650, designed for interactive data processing and computational timesharing, provides many of the 750's features. It performs engineering and business applications concurrently, supporting multiple languages and up to 63 simultaneous users. In distributed processing it can act as a program development tool. In addition, it can communicate with large mainframes and other systems over packet switched networks.

A 2k-byte cache memory provides an 85% hit rate on the next instruction to be executed. Execution times for single- and double-precision floating point arithmetic instructions on the 650 are said to be comparable to those of the IBM System/370 model 158.

(Continued on p 64)

Supporting up to 63 simultaneous users, the 550 runs programs up to 32M-bytes long and offers 2M-byte main memory capacity. A 2k-byte, 80-ns bipolar memory serves as a buffer between the CPU and main memory. The cache algorithm pro-

vides an 85% hit rate on the next instruction to be executed.

The processor's 32-bit wide arithmetic unit performs all integer arithmetic and logical operations. Design of the arithmetic unit permits complex address formation such

as base-plus displacement and indexing.

Features such as process exchange, segmented and paged memory management, and high data transfer rates give the system the power and speed for interactive data processing and computational timesharing, and for distributed processing applications that offload batch oriented mainframes.

Based on 550 system architecture, the 450 offers up to 1M bytes of main memory and supports 32 simultaneous users. The special CPU configuration, packaged in a cabinet with 32M-byte cartridge disc, is designed for the OEM. Included in the system are 2k-byte, 80-ns cache, floating point instructions, and virtual control panel.

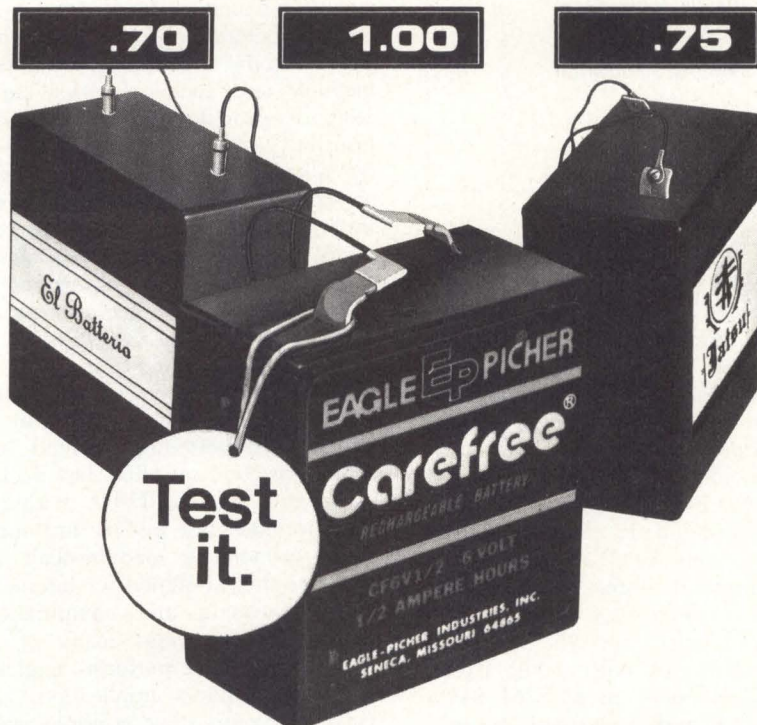
Standard on 450, 550, 650, and 750 systems, a virtual control panel allows a diagnostic specialist to remotely control any system, providing fast, effective troubleshooting. A pushbutton controls remote access to the system; a second button provides one of two modes of remote access: the remote terminal may monitor only or may be given the capability to operate the system. Two indicator lamps mounted on the panel's cabinet display the state of the remote communications link: one signifies that a remote user has permission to dial into the system, the other whether or not a remote access is in progress.

ANSI PL/I, ANSI '77 FORTRAN, and an interactive source level debugging tool have been added to the existing languages for the machines (ANSI '74 COBOL, BASIC, BASIC/VM compiler, IBM compatible RPG II, and macro assembler). PRIME/POWER is an interactive data management facility that simplifies data query, reporting, and maintenance tasks, allowing users to modify, compute, create, inquire, and report information from file systems.

Midrange systems 650 and 550 range from \$150,000 to \$250,000 and from \$95,000 to \$175,000, respectively, in price and are available now. Deliveries on the 750, which costs in the \$180,000 to \$300,000 range, are scheduled for midyear. The 450, with a price of \$35,000 in quantity, is scheduled for delivery in April.

Circle 374 on Inquiry Card

Test CAREFREE[®] against the gels.



We guarantee to deliver 100% capacity on the first cycle, unlike gels — with none of the memory problems of nickel cadmium. That's why the CAREFREE immobilized electrolyte technology is becoming the standard of the industry. Test one for yourself. Then choose from the world's largest line of maintenance-free rechargeables — 1/2 amp to 33 amp, 2 volt to 24 volt.

If you want to get technical, give us a call 417 776-2258



EAGLE-PICHER
SINCE 1947

Eagle-Picher Industries, Inc. • Commercial Products Department
P.O. Box 130, Seneca, Missouri 64865 • TWX 910 774-4533

AMPEX DELIVERS

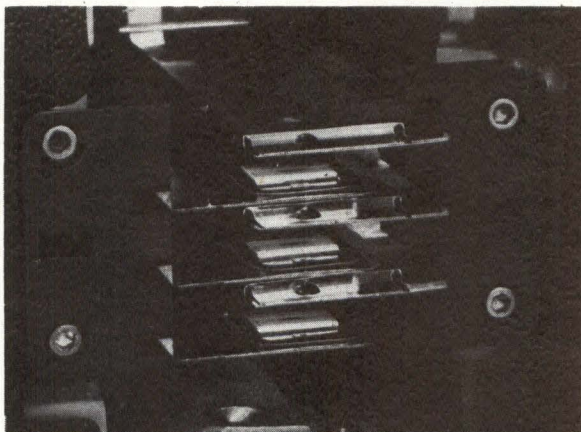
Ampex disk storage modules are both interface and *media* compatible with CDC's 9760 and 9762. And Ampex 40 and 80 megabyte SMDs offer a unique advantage over the CDC equivalents—they both can grow to a capacity of 160 megabytes with a simple field modification.

You'll find a lot more than CDC-compatibility when you look into the Ampex storage module family. Ampex can package your drive in rack, console or "Tempest" configuration, and can deliver such desirable features as variable sector format, address mark capability and on-track head servoing. The transfer rate is 1.209 megabytes per second, and access time average is 28 milliseconds.

Other Ampex disk storage modules provide capacities of 100, 200 and 300 megabytes, and within a given family, you can begin with the minimum storage and upgrade to a higher capacity right in your own facility. For those with super special data needs, Ampex even has a 300 megabyte module with a parallel transfer rate of 10.88 megabytes per second.

CDC-COMPATIBLE SMDs WITH BUILT-IN GROWTH.

Larry Russell has the information. Call him at 213/640-0150, and he'll prove that now there are twice as many ways to get the SMD capacity you need when you need it. Technical information and performance data is complete, and free. Write to Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Immediate delivery is only a P.O. away.



AMPEX MAKES IT EASY.

The Bantam.

The cocky new \$599* CRT that just changed the pecking order.

User Need	Feature	P-E BANTAM	LSI ADM-3A	Hazel- tine 1400	Hazel- tine 1500	Adds Regent 100
Easy to read display	7 x 10 matrix for highly legible characters	Yes	No	No	Yes	No
	Black on white or white on black display	Yes	No	No	Yes	Yes
	Display set deep in hood to reduce glare	Yes	No	No	No	No
	Full 24 x 80 display	Yes	Yes	Yes	Yes	Yes
	Full upper and lower case	Yes	Option	No	Yes	Yes
	Non-glare screen	Option	Yes	No	Yes	Yes
High operator throughput, low operator fatigue	Tab stops/tab key	Yes	No	No	Yes	Yes
	Backspace key	Yes	No	No	Yes	Yes
	Repeat key	Yes	Yes	No	No	Yes
	Shiftlock key	Yes	No	No	No	No
	Separate print key	Yes	No	No	No	Yes
Convenient switching Local/on-line	Local - remote key	Yes	No	Option	Option	Yes
International Character sets	French/German/Swedish/Danish/British/Spanish	Option	Option	No	Option	Option
High speed numeric	Integrated numeric pad	Yes	Option	No	Yes	Yes
Convenient system interfacing	RS-232/CCITT-V24	Yes	Yes	Yes	Yes	Yes
	Current loop	Option	Yes	No	Yes	Yes
Simplified program debugging	Transparent mode and displayable control characters	Yes	No	No	No	No
Faster maintenance	Self-test	Yes	No	Yes	No	Yes
Minimum desk space	Small size	15Wx 19Dx 14H	15.5Wx 20.2Dx 13.5H	15.5Wx 20.5Dx 13.5H	15.5Wx 20.5Dx 13.5H	21Wx 23Dx 14.5H
Printer port	Printer port	Option	Yes	No	Yes	Option
Cost effectiveness	Qty. 100 OEM price	\$599†	\$740	Less than \$550 in quantity 1000	\$860	\$895

*In quantities of 100.
†Qty. 1, End User Price \$966.

Nobody ever offered you a tough, high quality, compact CRT like the BANTAM before. At \$599 or any price. Designed for hectic office environments. And, human engineered to make an operator's life easier.

You get everything you need for cleaner input and faster throughput. An upper and lower case character set displayed on a sharp 7 x 10 dot matrix. A full 24-line by 80-character screen. A complete, sure-touch keyboard with shadow numeric pad.

You get complete tabbing. Full cursor addressing. Repeat, backspace and shiftlock keys. A transparent mode with displayable control characters to simplify host program debugging. And, a self-test mode for easy maintainability.

And, you get everything your operators need to make their jobs a joy. A hooded display that cuts glare. A wide bandwidth monitor for sharp images everywhere on the screen. Below-the-line character descenders' to make reading easier.

A switchable white-on-black or black-on-white display, whichever your operator prefers. An easy-to-find cursor that frames the entire character position in a transparent, inverted video block.

Plus plenty of options you can't get with CRTs costing much more. Like our low-cost Pussycat page printer. A full range of foreign language character sets. We even have a model you can switch from ASCII to full overstrike APL.

But that's not all. The BANTAM's compact good looks fit any decor. It's handsome enough for executive row and rugged enough for the stockroom. Silent? The BANTAM's fan-free design makes it quieter than an electric typewriter. And, the BANTAM only weighs 28 pounds.

Only an industry leader like Perkin-Elmer could do it. We designed a powerful, custom LSI controller chip that makes the BANTAM the one and only high quality CRT in its class.

But see for yourself. Use the comparison chart. Learn why we're so proud to add this \$599 CRT to the 250,000 peripherals that bear our good name.

And, remember our terminals come equipped with a No Hassle, 800 toll-free service phone number.

One call does it all. We give you service *where* you need it, when you need it. We're there. Not just "worldwide," but wherever you are.

For more information call or write Perkin-Elmer Terminals Division, Randolph Park West, Route 10 & Emery Avenue, Randolph, N.J. 07801 (201) 366-5550. Or contact any of our sales offices. Then watch the feathers fly.

The Bantam's available at all these places

PERKIN-ELMER SALES OFFICES

Santa Clara, CA (408) 249-5540.

Tustin, CA (714) 544-9093.

Atlanta, GA (404) 393-8440.

Arlington Heights, IL (312) 437-3547.

Waltham, MA (617) 890-1305.

Oceanport, NJ (201) 229-4471.

McLean, VA (703) 827-5900.

Singapore, Republic of
Singapore 2200949

Sydney (North Ryde), Australia
887-1000.

Toronto (Mississauga), Canada
(416) 677-8990.

Slough, England 753-34511.

Paris, France 664-1858.

Munich, Germany 089-753081.

Schiphol-Oost,

The Netherlands 020-458-269.

PERKIN-ELMER SERVICE CENTERS

Randolph, NJ; Oceanport,

NJ; West Long Branch, NJ;

Rochester, NY; Boston, MA;

Hartford, CT; Philadelphia,

PA; Pittsburgh, PA;

Washington, DC; Atlanta,

GA; Orlando, FL; Cleveland,

OH; Dayton, OH; Englewood

Cliffs, NJ; Detroit, MI;

Chicago, IL; Minneapolis,

MN; Kansas City, KS; Tulsa,

OK; Dallas, TX; Houston, TX;

Denver, CO; Phoenix, AZ;

Seattle, WA; San Francisco,

CA; Los Angeles, CA;

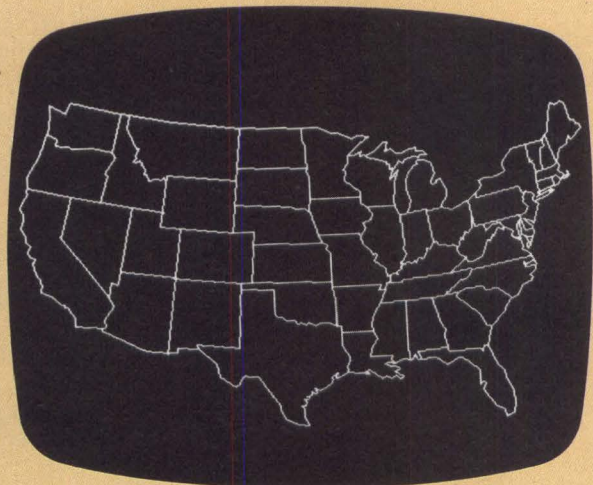
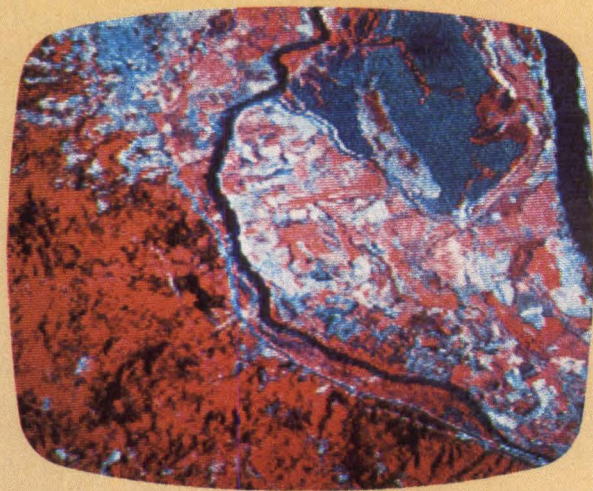
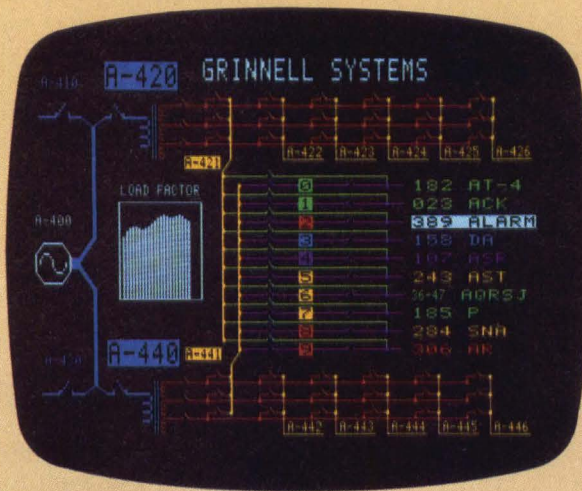
Orange County, CA; San

Diego, CA.



PERKIN-ELMER
Data Systems

Grinnell has your display...



from low cost imaging and graphics to full color image processing

Our modular, solid state systems can meet your computer display requirement, easily and economically.

And, they're intelligent. Every system has a complete alphanumeric and graphics package, and a powerful instruction set that simplifies programming—no need for complex macro-instructions and high order programming languages.

There's also a choice of standard resolutions: 256 x 256, 256 x 512, 512 x 512 (30 Hz or 60 Hz refresh) and 1024 x 1024. Plus plug compatible interfaces for most minis.

Options include overlays, function memories, pseudo-color tables, zoom and pan, independent cursors with trackball and joystick controls, split-screen, image toggling, and real time digitizers that grab and store images and sum consecutive frames.

Grinnell displays are already used for tomography, ERTS imaging, process control, image processing, animation and much more. All systems drive standard TV monitors.

So before you choose a display system, let our experts show you how to maximize performance and minimize cost. For details, and/or a quote, call or write.

GRINNELL SYSTEMS

2986 Scott Boulevard, Santa Clara, California 95050 (408) 988-2100

CIRCLE 36 ON INQUIRY CARD

System Enhancements Include Processor, Workstation Attachment

A Series/1 processor and an increase in the number of workstations attachable to the System/34 are among the enhancements announced by International Business Machines Corp, General Systems Div, PO Box C-1645, Atlanta, GA 30301. Other extensions to the Series/1 are 23M- and 29M-byte/drive disc subsystems and a FORTRAN IV Compiler and Object Support Library.

Using advances in storage and logic to reduce computing costs, the 4952 processor features main storage capacities of from 32k to 128k bytes and has an average instruction time of 9.4 μ s. The CPU, storage, clock comparator, and storage address relocation translation function are packaged on a single 9 x 7" (22.8 x 17.8 cm) processor card.

The storage address relocation translation function provides two 64k-byte address spaces and storage protection for the 2k-byte region controlled by each segmentation register.

128k bytes of storage sells for \$1800; a basic processor with 32k bytes of memory is expected to sell for \$4600, with 32k-byte memory increments pluggable on the processor card available at \$450.

Enhancing the 4963 disc subsystem are 23M- and 29M-byte models. The subsystem consists of primary disc drive and up to three expansion drives. Primary drive attaches to the Series/1 channel via the 3590 subsystem attachment feature. All models have 27-ms average seek time for movable heads, average rotational delay of 9.6 ms, and a 1.03M-byte/s instantaneous data rate.

Attachment features enable 5250 information display systems to attach to the Series/1, permitting a maximum of eight workstations to each attachment feature. A multiline attachment allows users to specify line speed, mode of operation, number of character bits, and parity on a per-line basis.

A licensed program for the event driven executive (EDX) basic supervisor and emulator, the FORTRAN IV compiler and object support library transforms source programs into machine instructions acceptable to the 4955 processor and the object library

provides I/O interfaces to the operating system, debug facilities, and bit manipulation routines to support the object execution environment.

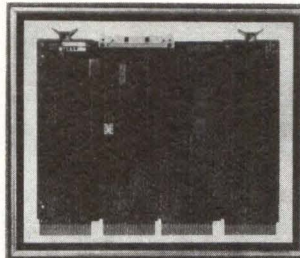
Workstation control expansion B feature for the System/34 enables eight additional 5250 display systems to attach directly to the system. Other enhancements expand the functions of interactive communications

between processors in a distributed systems network. Additions to the system support program interactive communications feature provide a high level interface for system to system communications using synchronous data link control and 3270 host system programs using binary synchronous communications.

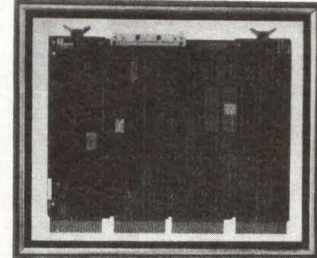
Circle 375 on Inquiry Card

PDP-11, LSI-11, LSI-11/2 COMPUTER USERS MEET THE DILOG STORAGE MASTERS

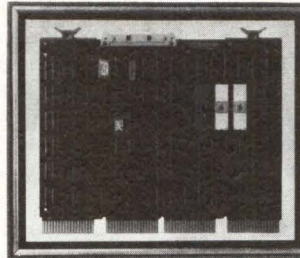
A COMPLETE FAMILY OF CARTRIDGE DISC AND MAGNETIC TAPE CONTROLLERS CONSTANTLY GROWING TO MEET YOUR BULK STORAGE NEEDS



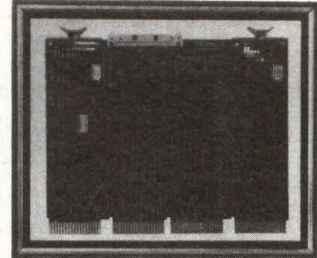
LSI-11 DISC CONTROLLER



LSI-11 TAPE CONTROLLER



PDP-11 DISC CONTROLLER



PDP-11 TAPE CONTROLLER

ALL MEMBERS OF THE DILOG FAMILY ARE COMPLETELY CONTAINED ON ONE QUAD-SIZE PRINTED CIRCUIT BOARD THAT OCCUPIES ONE LOCATION IN THE COMPUTER CHASSIS. THE MEMBERS OF THE FAMILY ARE ALL MICROPROCESSOR BASED PERMITTING THE FOLLOWING BENEFITS TO BE PROVIDED:

- To aid in isolating system malfunctions, an on-board AUTOMATIC SELF TEST feature monitors the controller for proper operation. A green DIAGNOSTIC indicator on the edge of the controller board remains lighted as long as the controller is functioning properly. If self-test fails, the controller has an AUTOMATIC DATA PROTECT feature that stops the CPU from interacting with the disc or tape, and thus prevents writing erroneous information into critical data base areas.
- All controllers are software compatible with DEC* operating systems.
- Various levels of system support are available — factory integration of customer-supplied peripherals, complete peripheral subsystems including a DILOG-selected peripheral, engineer/systems analyst consultation for special applications involving DILOG controllers.

DELIVERY ALL FAMILY MEMBERS IS STOCK TO 30 DAYS

OEM MIX AND MATCH DISCOUNTS FROM LOW UNIT QUANTITY PRICES ARE OFFERED

Come meet the current family members and let us introduce you to the newest arrival at NCC 79 in Booth 351 at the New York Hilton. But don't wait until then to let us hear from you; write or call SALES MANAGER, Distributed Logic, Inc., 12800G Garden Grove Blvd., Garden Grove, California 92643. TELEPHONE (714) 534-8950.

*DEC, PDP-11, LSI-11 are registered trademarks of Digital Equipment Corporation.

Realtime System Tests Boards Containing LSI/VLSI Components

In response to the trend toward greater board densities and increasing use of dynamic LSI devices, the CAPABLE 4900 system incorporates a 24-slot chassis, 512 high speed pins, and 10M-byte disc capacity to permit high density boards to be tested without sacrificing throughput. Computer Automation, Inc, Industrial Products Div, 2181 Dupont Dr, Irvine, CA 92713 has designed into the system the ability to functionally emulate logical operations of high density LSI components.

Interchangeable high speed pin interfaces, realtime controller, and realtime guided fault isolator controller are the three primary modules that make dynamic testing possible. A system integration and debugging aid uses the system's video display terminal CRT as an oscilloscope. Operating system instructions permit display of waveforms on the screen while timing signals between the test system, its test fixture, and the unit under test are being checked.

5- to 15-V adjustable or -15- to 15-V programmable pin interfaces provide high and low level changes, pulses in either direction, return-to-zero or return-to-one mode, clock signals, and complex waveforms during realtime operation. Available in 1k or 4k pattern depths, the pin module functions as a bidirectional pin for logic card's high speed data buses.

Programmable clock generator together with programmable local processing unit and realtime guided fault isolation receiver comprise the controller module. The multiphase clock generates eight phases. An internal phase lock loop circuit allows synchronization of the system to the onboard clock of the unit under test. The system references its oscillator if the board being tested has no clock onboard. Programmable to 20 MHz, the system reference clock permits multiple pulses to be generated in each test step.

Dedicated local processing unit operates from 10 kHz to 2 MHz. This unit has program memory and executes a high level instruction set that includes loop, branch, jump, and call subroutines.

Realtime guided fault isolation receiver generates and stores status information and controls clip and

probe accessories. Using current sensing probe and current injection techniques, an advanced fault resolution feature traces a fault to the exact pin or etch defect that is the cause of failure. Both 16- and 24-pin clips are standard.

The basic configuration, consisting of CPU, 32k main memory, 10M-byte moving head disc storage, realtime module, floppy disc drives, CRT terminal, and 16- and 24-pin high speed clips, is priced at \$110,000, with 90-day delivery. Options include analog and hybrid testing capability, programmable power supply, max of 512 pins (obtained in 16-pin increments), and memory storage expansion to 96k words of main memory and 80M bytes of mass storage.

Circle 376 on Inquiry Card

Timesharing System Allows Four Programs To Execute Concurrently

Using the DATASHARE® Business Timesharing System on the 1800 Dispersed Processor permits up to four local or remote users to enter data, execute programs, and complete other tasks from a common data base. The system, from Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, is claimed to provide an economical alternative for the business requiring multiple workstations.

1800 Datashare permits concurrent execution of up to four of the same or different programs, and maintains each program's data area in main memory for faster program execution. Data areas are independently configurable from 256 to 4096 bytes.

The system supports any teleprinter compatible device used as a workstation. Send and receive rates of each terminal device may be set independently, and range from 110 to 9600 baud. Terminals may be linked directly to the 1800 processor via a hardwired connection; remote terminals may use 103-type or 202-type modems over dialup or leased lines.

Prompting messages and menu-type screen displays make system configuration easy. The system's DSGEN package allows untrained operators to implement a complete data entry, validation, printing, and updating system. After a screen format has been designed, the operator can assign field checks, table lookups, and other editing criteria by

simply responding to prompting messages.

The systems may become participants in an attached resource computer (ARC™) system. While operating within this system, the 1800 uses disc storage managed by another processor instead of its own diskette module. The 1800 contains a processor and 60k bytes of user memory, keyboard, video display screen, and an integral auto answer communications interface. Capacity of the double-density diskette system may be expanded from 1M to 4M characters.

Single user data entry operations may be conducted in Interactive COBOL, DATAFORM™, DSGEN, and DATABUS. Batch-mode processing languages are BASIC PLUS, ANSI COBOL, RPG PLUS, DATABUS, and ASSEMBLER. 2780, 3780, RES, and HASP emulators allow single-user communications; MULTILINK™ permits realtime communication with host systems; DSNET™ allows remote files to be updated; and DATAPOLL® provides for network operations.

Circle 377 on Inquiry Card

Computer Terminal Produces Speech Output For Use By Blind

Free Scan Speech Terminal, model 1 (FSST-1), developed by Triformation Systems, Inc, 3132 SE Jay St, Stuart, FL 33494, permits visually impaired workers to perform a variety of data processing jobs. Using the unit, a blind operator is able to scan data stored in a computer memory and hear the information through a speaker or headphones. Sighted operators performing this task would read the information on a CRT display.

The operator enters instructions through a typewriter-like keyboard, using a set of function keys to access memory and enter the location of data by column and row. When the desired data stored in the computer's memory has been located, the electronic speech system "reads out" the data.

Electronic signals corresponding to each character are used to trigger a recording, playing back alphabetized speech, letter by letter, of data exactly as it would be displayed on a CRT. Speed of the response is switch controlled, allowing the operator to perform with high efficiency.

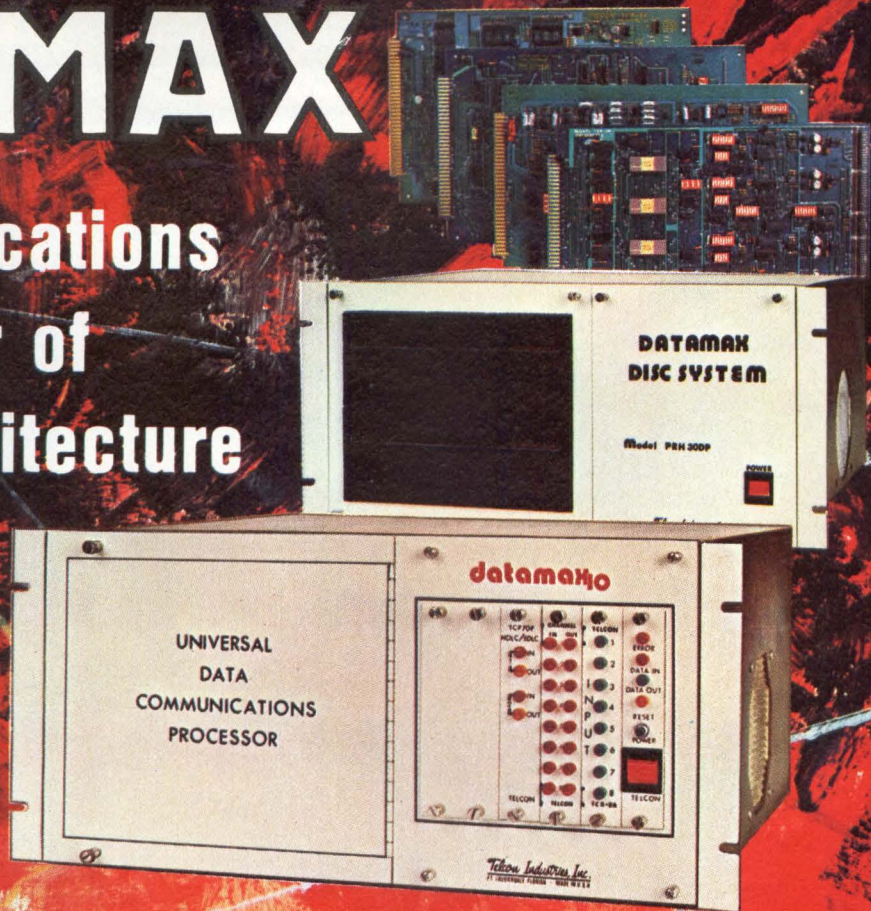
The device has an RS-232-C interface and uses standard ASCII input code. This enables it to be used with virtually any computer system.

Circle 378 on Inquiry Card

DATAMAX

The Communications
Processor of
Unlimited Architecture

Over 1,000
DATAMAX
Systems are
NOW IN USE



Datamax Systems handle a multitude of applications in both standard and custom environments.

Modular design effects cost savings by meeting exact needs in amount of hardware and application requirements. Expansion for existing systems entails addition of required modules only: an important cost factor.

Microprocessor-based, the DATAMAX offers total system design flexibility. Semi-conductor Read/Write RAM up to 32K Bytes. Optional Disc Storage up to 1 Mega Byte.

Telcon
INDUSTRIES, INC.

Leaders in Data Communications Since 1968

THE DATAMAX IS ...

THE ULTIMATE DATA CONCENTRATOR, 8 through 64 ports.

- Statistical TDM or TDM
- Intelligent Modem
- Message Switch
- Selective Caller
- Multi Port Store and Forward Unit
- Speed and Code Conversion
- Telex Switch
- Multi Protocol Interface
- Modem Concentrator, Mux with Modems Built-in

GENERAL SPECIFICATIONS

- 115/230 VAC-50/60 Hz Standard
- Sync, Async, Bisync, HDLC, SDLC
- Codes 5,6,7,8 or as required
- Ports 2 thru 64 with HI-Lvl (N) (P) and EIA
- Expandable RAM up to 32 K
- Built-in Modems 300,1200/1800,2400 Auto/Dial-Auto/Answer
- Programs Reside in E/PROM up to 16K
- Add on Disc Systems
- Complete Software Development System Available

Write for a complete Datamax library.

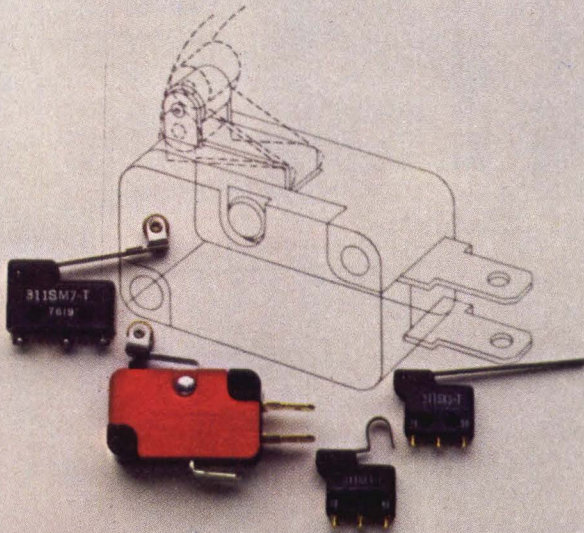
5701 N.W. 31st Ave., Fort Lauderdale, Florida U.S.A. 33309
Telephone: 305/971-2250 • TWX: 510/956-9412
• London: 01/353-6621 • Canada: 416/922-9191 •

Distributor Inquires Invited

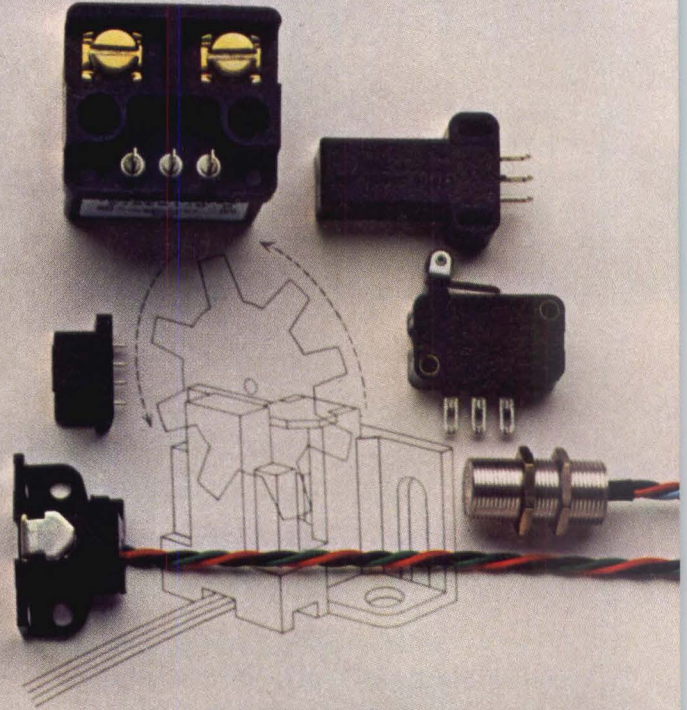
CIRCLE 38 ON INQUIRY CARD

Some of these components will probably never The others will just come close.

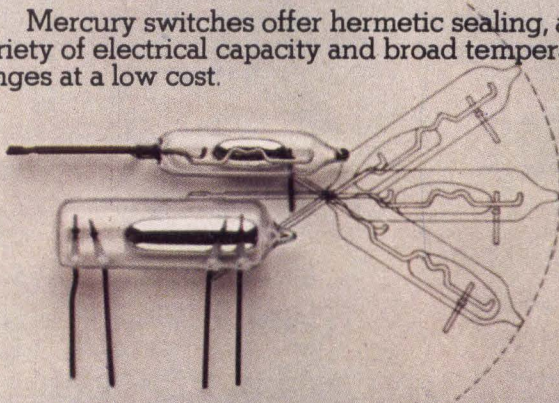
The SR, XL, XK and AV are solid state position sensors featuring almost infinite life. All offer zero speed operation with some up to 100 KHz. ES current sensor utilizes Hall-effect IC and protects against damage from short circuits or overcurrent conditions.



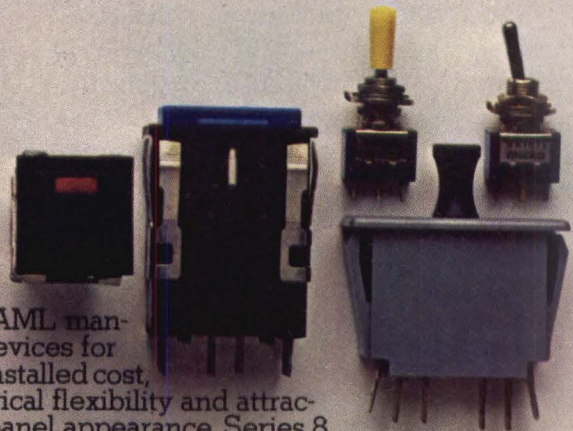
Snap-action V3, SM and SX switches offer wide variety of actuators, electrical capacity and termination.



Mercury switches offer hermetic sealing, a variety of electrical capacity and broad temperature ranges at a low cost.



AML manual devices for low installed cost, electrical flexibility and attractive panel appearance. Series 8 miniature manual switches provide small size and wide variety of operators. DM offers inexpensive snap-in panel mount design.



Solid state keyboards provide high reliability no mechanical keyboard can offer. Panel sealed versions also available.



wear out.

The solid state keyboard, AML lighted push-buttons and sensors you see here will probably never wear out. Because they're all solid state.

Each is based on a Hall-effect integrated circuit. A circuit that's been tested through billions of operations without failing. And proven by performance in thousands of applications.

The precision electro-mechanical components you see here come close. Simply because of the careful way they're designed and put together.

Like the long-life versions of our snap-action V3, SM and SX precision switches. Available in a wide variety of sizes, electrical ratings, terminals, actuators, contact forms and operating characteristics — some tested to a mechanical life of over 10,000,000 operations.

MICRO SWITCH will provide you with field engineers for application assistance and a network of authorized distributors for local availability. Write us for details or call 815/235-6600.

And find out how you can get a component that goes on forever. Or at least comes very, very close.

MICRO SWITCH

FREEPORT, ILLINOIS 61032

A DIVISION OF HONEYWELL

MICRO SWITCH products are available worldwide through Honeywell International.

DIGITAL TECHNOLOGY REVIEW

SOFTWARE

Added System Functions Increase Productivity and Reduce Operator Overhead

Enhancements to the System 5000 family contribute to productivity by giving operators more file processing control and by lessening operator involvement in routine processing. Introduced by Inforex, Inc, 21 N Ave, Burlington, MA 01803, the series includes five functions that facilitate file processing and packed decimal conversion, increased procedure library capacity for processing large applications; and remote operator command and letter quality printing features.

File table access, update, and insert commands allow operators to perform dynamic file table alterations; an OCA write feature permits

related file processing commands to be linked for automatic execution; and tape to tape file compatibility with mainframe packed decimal formats is facilitated by a packed decimal conversion feature.

Further software and hardware features are designed for use in remote applications. A remote batch print command allows system files to be printed remotely without operator intervention. A 150-char/s receive only printer fills medium volume remote requirements. The model 1410 uses a full 96 ASCII character set in a 9 x 7 dot matrix pattern. It features selectable baud rates from 110 to 9600, automatic parity error detection, and a self-test switch that initiates a rotating character test pattern.

Circle 379 on Inquiry Card

Software Strengthens 32-Bit Computer in Educational Administration

A high level COBOL language, a multikey ISAM file access capability, and a sorting utility take advantage of the 32-bit architecture of the VAX-11/780, allowing it to assume academic tasks. Announced by Digital Equipment Corp, Education Products Group, Maynard, MA 01754, the products complement current offerings that include FORTRAN IV-Plus and BLISS-32; as well as DATA-TRIEVE, a compatibility mode query language and report writing system.

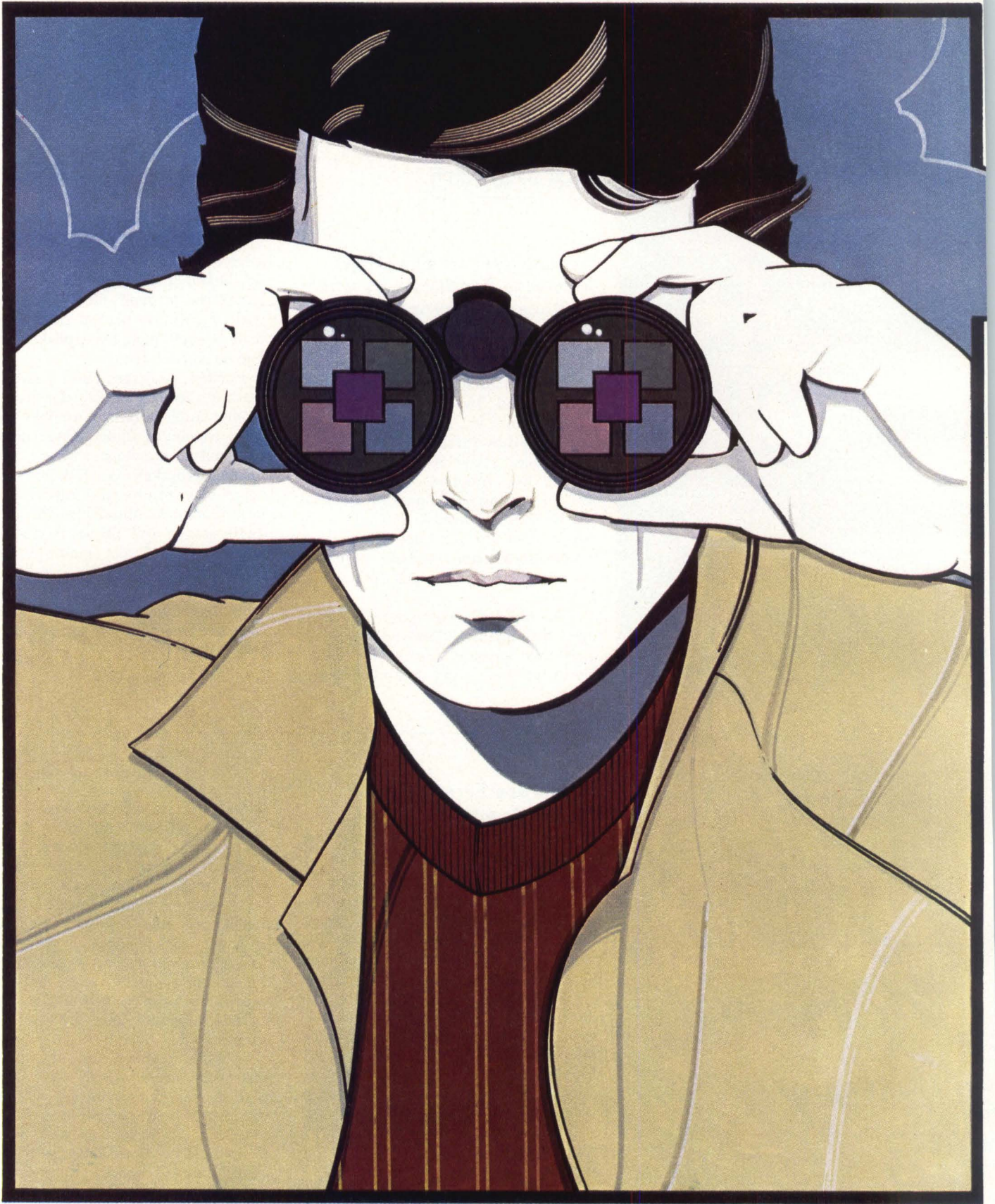
COBOL conforms to the 1974 ANSI standard with implementation of the nucleus, table handling, and I/O modules for sequential, relative, and indexed sequential file access as well as interprogram communication and a library facility. 32-bit object code allows direct calls to the operating system, subroutine calls to and from

other VAX-11 languages, transparent access to DECnet, and use of the system's virtual memory address space. The language accepts packed decimal data and uses the system's string manipulation instructions.

A native mode multikey ISAM facility extends the RMS file management system supplied with VAX/VMS operating systems. A design tool for creating data bases, the facility provides a primary key and as many as 254 alternate keys for access to each record.

A high performance utility that sorts data according to record, tag, address, and index sorting methods, the SORT package works with all RMS file organizations and record formats. It accommodates ASCII character, binary, decimal, packed decimal, and zoned data. The modular utility has a flexible memory requirement and can be used in standalone mode or as a subroutine to COBOL or other language programs. □

Circle 380 on Inquiry Card



The Future Has Arrived.

Intel delivers the 8086. Powerful. Practical. And the Architecture of the Future. Here today.

We have seen the Future and it is called 8086.

Even better, it's here today. Our new 16-bit microcomputer is an

architectural triumph, introducing designers to a new world of system expansion capability, high-level language programming and dramatically increased system thrupt.

Why we call it "The Future"

To deliver the Future, we designed the 8086 with a totally new architecture, super-efficient for implementing high-level, block-structured languages such as Pascal and PL/M-86.

The 8086 addresses up to a full megabyte of system memory with new addressing modes and efficient register utilization that totally support such minicomputer-like capabilities as relocatable and re-entrant code and instruction look ahead.

And the 8086's powerful new instruction set includes both 8-bit and 16-bit multiply and divide in hardware, with efficient byte string operations and improved bit manipulation.

We're committed to delivering the industry's highest performance, today and into the future. The 8086's architecture maximizes system thrupt today by delivering ten times the processing power of its 8-bit predecessors. Planned expansion promises another order of magnitude increase in performance through the addition of

I/O processors, special instruction set extension processors, memory management and distributed intelligence configurations.

System components for expanded multiprocessor applications are available right now, supporting the Multibus™ architecture in timing, control and drive levels. They include 8288 Bus Controller, 8282/8283 Octal Latches and 8286/8287 Octal Transceivers.

Get a jump on the future.

8086 is the most successful new microcomputer ever. The list of major market leaders who have evaluated 16-bit machines and chosen the 8086 is staggering.

One reason for the 8086's success is our commitment to *your* success. We've made the 8086 the industry's best-supported microcomputer. The cpu, interrupt controller and six additional support circuits are on distributors shelves, with more on the way. You can take advantage of the 28 existing Intel® peripheral interfaces. Our 2716 (16K) and 2732 (32K) EPROMS provide programming

flexibility and unique features for 8086 users, including protection against bus contention.

And we complete your system with a variety of off-the-shelf +5 volt MOS RAMs.

You can begin hardware/software development today, using the Intellec® Microcomputer Development system with ICE-86™ in-circuit emulation, PL/M-86 and ASM-86 for assembly language programming and 8080/8085 software conversion.

SDK-86, a complete system design kit including all essential components, makes it easy to begin prototyping without delay.

For an additional head start, iSBC 86/12™ single board computer brings the power of the 8086 to the Multibus with a fully assembled and tested 16-bit system.

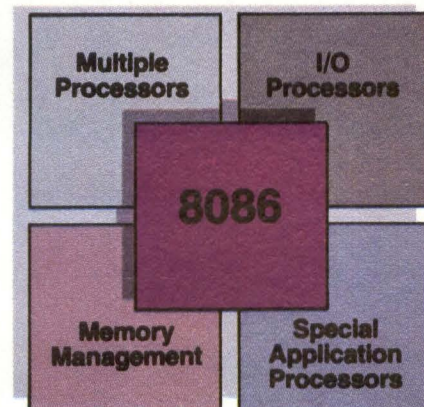
The Future belongs to you.

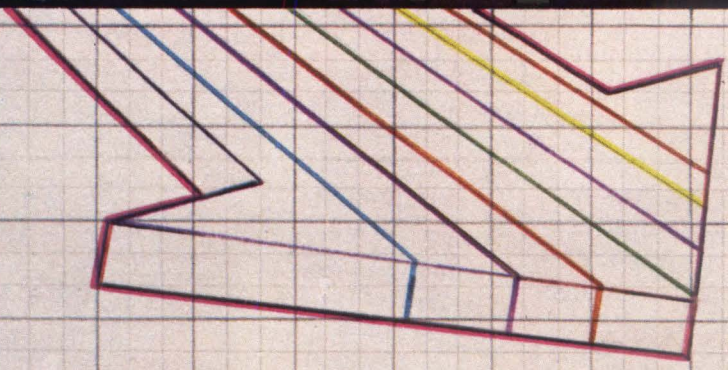
Get to market first and capture a piece of the future for your product. You can order the complete 8086 family from your distributor. Or, for more information, contact your local Intel sales office or write:

Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.

intel® delivers.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Strom, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.





Shortcut to Success.

Introducing iSBC 86/12™, the single board computer that brings the power of the 8086 to the Multibus™ standard.

There's no quicker way to implement designs with the new 8086 16-bit microprocessor than our new iSBC 86/12. It's dramatic evidence of the architectural capability of the 8086, with unprecedented computing power, memory and I/O capacity on a single board.

Multibus™ architecture ensures success.

The Multibus standard is your path to success with the iSBC 86/12 board. Since we introduced it in 1976 it has become the industry standard micro-computer bus. Even then we were looking forward to the 8086 and designed the Multibus architecture to support both 8- and 16-bit computers in single or multimaster systems, and a full megabyte of directly addressable memory.

That gives you unlimited design flexibility, with immediate access to the complete iSBC family of 8-bit computers, memory boards, analog and digital I/O, peripheral control and communications boards.

Plus over 100 additional expansion boards from more than 40 independent suppliers. And Multibus compatibility means you can preserve your design investment as your application requirements grow from 8 to 16 bits.

iSBC 86/12™ designed from experience.

We drew upon all our design experience to make the iSBC 86/12 board the most advanced 16-bit single board computer available.

At its heart is our 8086 CPU that gives the iSBC 86/12 board ten times the processing power of our 8-bit single board computers. We added 32K bytes of dual port RAM, fully accessible by all Multibus masters in shared memory designs. There are sockets for up to 16K bytes of EPROM. And the advanced architecture of the 8086 addresses up to a full megabyte of system memory.

The iSBC 86/12 board has a flexible I/O structure, with 24 programmable parallel I/O lines and a programmable synchronous/asynchronous communications channel with RS232C interface and programmable baud rate generator. In addition, the iSBC 86/12 architecture provides nine levels of vectored interrupt control and two programmable interval timers.



More than a shortcut.

The iSBC 86/12 board is a fully assembled and tested computer, dramatically reducing development time compared to component level design. More important, lower hardware costs enable you to incorporate the iSBC 86/12 board in hundreds of performance-dependent applications where the size and cost of larger computer systems would be prohibitive.

And, with Intel, there's no penalty for success. When volume makes it more economical for you to build instead of buy your boards, we'll provide manufacturing drawings, pc artwork and a volume source for all the essential LSI components.

The same Intel® Microcomputer Development System used with all Intel® microcomputers supports the iSBC 86/12 board with features such as ASM 86 assembler and PL/M 86 block-structured high level system programming language. You can debug your software right on your prototype system with ICE-86™ In Circuit Emulator or with the iSBC 957™ Interface and Execution package.

Attend an iSBC™ seminar in your area.

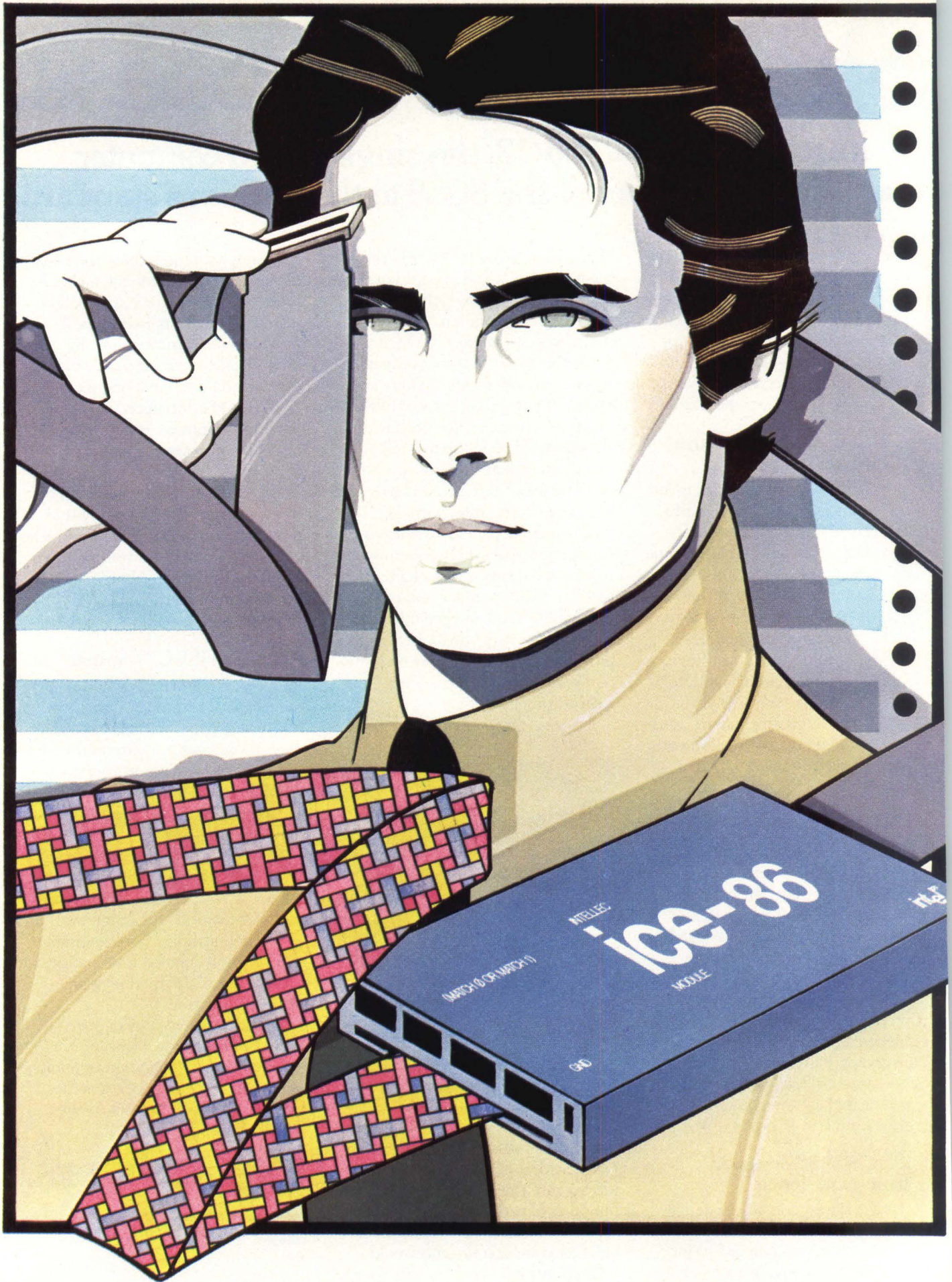
The best way to get started with this new-generation Single Board Computer is to attend the Intel iSBC seminar in your area.

You'll learn about the iSBC 86/12 board and the rest of the iSBC product line. And we'll take you through the configuration and design cycle for several applications. For a seminar schedule and detailed information contact one of the Intel regional offices listed below.

And, for a free copy of our iSBC Configuration Planning Kit, or for on-site configuration or pricing assistance, write: Intel Corporation, Dept. 4-903, 3065 Bowers Avenue, Santa Clara, CA 95051.

intel® delivers.

Intel Regional Offices
Santa Ana, CA: (714) 835-9642 Boston, MA: (617) 667-8126
Chicago, IL: (312) 325-9510 Dayton, OH: (513) 890-5350



Sixth Sense for 8086 Users.

Intel delivers ICE-86™ emulator, the designer's direct diagnostic connection to 8086 system development.

Intel's new 8086 sets the standard for 16-bit microcomputers. It delivers the Architecture of the Future today, high-level languages for programming and the Intellec® development system for unsurpassed support.

Now that support moves even further out in front. Introducing the ICE-86 module. Experienced microcomputer designers have learned that having a development system with in-circuit emulation — ICE — is like having a vital sixth sense. Only ICE emulation provides designers with the real insight in actual system operation absolutely necessary for cost effective, efficient product development. Now Intel delivers that sixth sense for 8086 users.

ICE-86™ puts the future in your hands

The 8086's early availability provides the opportunity to get your new products to market a year or more ahead of your competitors who wait for follow-on 16-bit microprocessors. Only Intel delivers the future today.

The Intellec development system with in-circuit emulation enables you to seize that opportunity. You can actually begin software development and debugging in an 8086 environment before any prototype hardware exists. Or you can use the ICE-86 module to begin simultaneous hardware and software development and integration while your system is little more than an 8086 cpu and system clock.

The ICE-86 cable plugs into your system cpu socket to provide emulation of system operation, up to the full megabyte of memory the 8086 can address.

Communicate in English, or symbolic references.

The ICE-86 emulator is actually a complex breakpoint and logic trace system supporting the most advanced symbolic debugging techniques. English-like statements or symbolic references entered at the Intellec keyboard eliminate the need to search memory maps, keep track of address changes or get bogged down in the details of system operation.

And the ICE-86 emulator's powerful logic analysis capability helps find the cause and correct the problem when bugs do appear.

PL/M-86 for the Architecture of the Future.

The most powerful microcomputer ever deserves the most powerful microcomputer programming language. That's PL/M-86, an extension of the world's most widely used development language.

PL/M-86 is an ideal example of the block-structured languages the 8086's futuristic architecture can support. It gives you 32-bit floating point arithmetic and 16-bit signed integer arithmetic. And it takes full advantage of the program-compacting features of the 8086, such as hardware multiply and divide and byte-string operations.

PL/M-86 is best for fast composition of large and complex programs. For those who prefer the efficiency of assembly language, there's ASM-86. And CONV-86 converts 8080/8085 code to the 8086.

The future is even brighter. Planned expansion of the Intellec system promises programming in Pascal and FORTRAN and the added flexibility of a macro assembler. It's true today and will be true long into the future — the 8086 is the best supported 16-bit microcomputer you can buy.

Modular programming is here.

The Intellec system gives you the flexibility of modular programming. You can develop routines in small, manageable modules, choosing the best language for each. Then using the Intellec system's powerful relocation and linkage capabilities, you can merge modules using symbolic references.

We optimized Intellec hardware for 8086 development, providing a dual diskette, expandable to four drives and 2.5 megabytes of memory. And we'll be expanding the Intellec system with a 7-megabyte hard disk, enough memory to extend the 8086's capabilities into the realm of large mainframe computers.

A manual for your success.

We've compiled an in-depth Success Manual for 8086 Users, detailing the Intellec Microcomputer Development System, ICE-86 and the full software package for 8086 program development. For your copy, contact your local Intel sales office. Or write: Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.



intel® delivers.

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Cold-Rolling Mill for High Carbon Steel Strip Automated by Minicomputer

Computer controlled operation of a "Z-mill," in which a coil of high carbon steel strip is rolled several times to reduce its thickness, is said to result in a more uniform product and to eliminate variations in performances of different operators. This mill rolls strip steel up to 13" (33-cm) wide at speeds up to 1200 ft (366 m)/min in coils up to 600 lb/in (107 kg/cm) of strip width.

A Digital Equipment Corp PDP-8/M minicomputer automates the reversing Sendzimir cold-rolling mill (Fig 1) installed at Wallace Barnes Steel's Bristol, Conn plant. The \$1.5M mill was designed and built by the Waterbury Farrel division of Textron Inc, Cheshire, Conn. Automation includes passing the coil of annealed strip through the mill, stopping the machine, and resetting the controls so that the strip passes back through the rolls in the opposite direction. The reversing mill rolls a 0.072/0.060" (1.829/1.524-mm) thick strip, reducing thickness in a series of passes down to a minimum thickness of 0.003" (0.076 mm).

All operating information for a particular job is stored permanently on a magnetic card. The automated rolling procedures are set up by inserting that card in an electronic reader. Typical information on the card includes number of required passes, reduction in thickness per pass, winding tension, and rolling speed. End product repeatability is always ensured, regardless of the operator.

Control Procedures

Functionally, the mill consists of two winders, one at each end, which alternate for feed and take up. The strip passes through a cluster of rolls driven by a 400-hp mill motor.

During computer controlled operation, gamma-ray gauges continually monitor entry and exit strip thickness/deviation. Digital pulse tachometers in contact with the strip on both sides of the mill measure the output length for a given unit of input length and feed the necessary information to the computer (Fig 2). The computer stores the data, computes the change in mill screwdown setting to correct for any deviation, and initiates the screwdown command when that particular increment of strip enters the roll bite. ("Screwdown" is essentially the pressure exerted on the work rolls by a hydraulic piston to effect the desired reduction in thickness of the strip. "Roll bite" is the point

where the strip enters the work rolls, the point where the reduction in thickness is effected.)

On an ordinary Z-mill, one that has not been computer automated, the operator must perform a number of actions prior to starting or stopping a mill sequence. Normally, he threads the strip through the mill onto the takeup winder, inserts work rolls, closes the door, and turns on the coolant. Then he lowers the upper work roll to put pressure on the strip. Once the proper pressure is attained, he puts the strip under tension by increasing current to the 300-hp drive motor on each winder. Although the tensions at winders are necessarily unequal, the roll pressure prevents movement of the strip at this time.

Now the operator increases roll pressure to the degree he thinks is required to reduce metal by the amount he wants in this pass through the mill, and again increases tension on the winders. Then he places the gauges and pulse generators on the strip—and finally pushes the button to start the mill.

In comparison, the operator of the Wallace Barnes computer automated Z-mill merely pushes a single button to start the mill. The automated rolling schedule performs many of the routine control desk settings, while the automatic setup sequences the mill through thread speed to a preprogrammed speed. There are pauses at logical transitions in the sequence for operator inspection of the settings and events that took place. When a pause occurs, the operator must give the signal to continue the sequence.

An AUTO PROGRAM CONTINUE button is used to give the signal to continue the rolling schedule and setup sequence after a pause; an AUTO PROGRAM READY light indicates the state of the sequence. When the mill stops, the number of the pass that was being rolled is displayed, and the READY light goes out, indicating that the mill is not ready. Pushing the CONTINUE button automatically sets up the control desk for the next pass, displays the pass number, and turns the READY light on. The operator may check the condition of the desk and is free to make any changes at this time.

The automatic rolling schedule sets up the desk with input and output gauge setpoints, composition for the gauges, roll bite pressure, input and output tension values, desired rolling speed, high or low tensions, and number of tension motors. When the mill is started, the automatic gauge control system corrects any pressure or "roll bite" error to bring the gauges to the

FPS Expands the Scientific Universe of PDP-11 Applications

200 x INCREASE
IN THROUGHPUT

SIMULATION

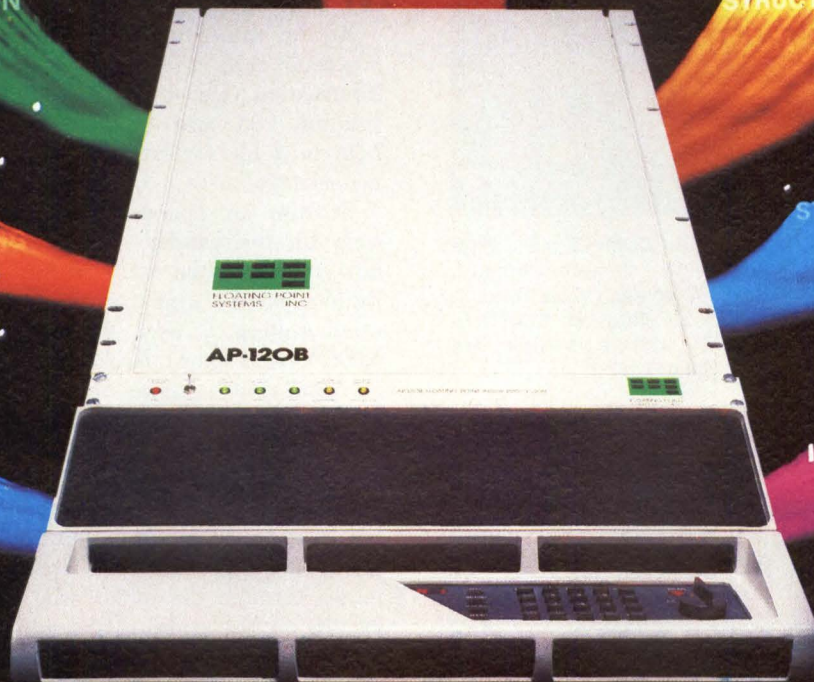
STRUCTURAL DESIGN

SIGNAL PROCESSING

STATISTICAL ANALYSIS

LOAD-FLOW ANALYSIS

IMAGE PROCESSING



FPS MAKES GREAT COMPUTERS BETTER

The FPS AP-120B Array Processor

A great contribution to technology, the DEC PDP-11*, but it can't give you the computational power required for many scientific applications. That's why FPS developed the AP-120B Array Processor.

The AP-120B Array Processor gives economical minicomputer systems the extraordinary computational power of large scientific computers. For example, an AP-120B has been used in a PDP-11 34 system to reconstruct and analyze complex digital images. Without the AP-120B, the task would take more than two hours. With the AP-120B, it takes less than thirty seconds — that's a 240X improvement!

A PDP-11 70 and AP-120B would offer

even greater data handling capabilities.

The FPS architecture is no secret. Internally synchronous operation and seven parallel data paths provide unequalled cost performance, reliability, and programmability. Programmable I/O units also enable exceptional features, such as direct control of disc storage and real time data flow.

Controlled by simple subroutine calls from a FORTRAN program in the PDP-11, or other host computer, FPS Array Processors can be programmed by selecting routines from the extensive FPS Math Library, by writing new routines in the relatively simple AP Assembly Language, or through use of the AP FORTRAN Compiler.

Hundreds of FPS Array Processors are in use today by people who want to retain the hands-on control and affordability of a minicomputer system, but require the exceptional throughput of a large mainframe for their application.

Find out how this new power in computing (typically under \$50K complete) can benefit your application. For more information and an FPS Array Processor brochure, use the reader response number or coupon below. For immediate consultation, contact Floating Point Systems directly.

*DEC and PDP-11 are registered trademarks of Digital Equipment Corporation.

The Age of Array Processing Is Here... and FPS Is The Array Processor Company.



CALL TOLL FREE 800-547-9677
P.O. Box 23489, Portland, OR 97223
TLX: 360470 FLOATPOINT PTL
In Europe & UK: Floating Point Systems, SA Ltd.
7 Rue du Marche, 1204 Geneve, Switzerland
022-280453, TLX: 28870 FPSE CH

Floating Point Systems, Inc.

FPS Sales and Service Worldwide: Boston, Chicago, Dallas, Denver, Detroit, Houston, Huntsville, Los Angeles, New York, Orlando, Ottawa, Philadelphia, Portland, San Francisco, Washington, D.C. International offices: Geneva, London, Munich, Paris, Tel Aviv (Eastronix, Ltd.), Tokyo (Hakuto Co. Ltd.)

CIRCLE 43 ON INQUIRY CARD

Please send me an FPS Array Processor brochure.

Name Title

Company Phone

Address

City State Zip

My Computer System is My Application is

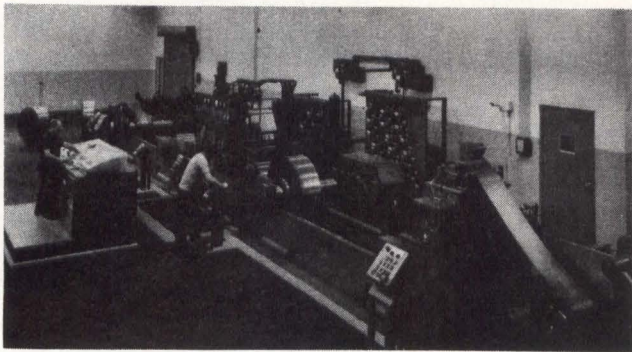


Fig 1 Wallace Barnes Steel Bristol, Conn Z-mill. High carbon strip steel is cold rolled under computer control, reducing strip thickness by 10 to 30% at each pass through reversing mill. Strip is reduced to as little as 0.003" in several passes. Coils of up to 13" wide strip steel are processed at speeds up to 1200 ft/min

proper setpoints. Measured deviations in the thickness of the input strip are used in a feedforward compensation to reduce deviations that might result on the output strip. A feedback control keeps the output gauge at its setpoint.

Initially, the operator sets tension, speed, pressure, material composition, and other variables. Once he is satisfied with them, he pushes a button to store the information. That information can be used on all subsequent passes through the mill—and the compilation of data available when the strip has been reduced to its desired thickness can be used to roll all other coils of the same product.

These data are transferred from the computer to a magnetic strip on a plastic card similar in size to a

credit card. (The card contains 256 bytes on a single strip. However, up to 1k bytes can be provided on a 4-strip card.) When the card is later inserted in a magnetic card reader, the computer has all data relevant to the coil of metal to be processed.

At the same time that data are transferred to the magnetic card, the operator receives printout of that information. He writes identifying notes on card and printout (eg, card, coil, and job numbers) and stores both in a file for later use in rolling coils of the same material.

Because an operator can see only the buildup of strip on the winder, it is very difficult to determine how much of the strip is left at the end of a coil. Buildup on the winder is visually deceptive, particularly when rolling a very thin strip. For example, three 0.005" (0.127-mm) thick wraps would have little buildup compared to three wraps of 0.020" (0.508 mm). The computer calculates precisely when to start decelerating the mill so that it can roll at maximum speed to practically the very end of the coil.

Computer calculations also are used to open or close strip wipers on the mill housing. The coil temperature is maintained with water soluble coolant as the strip passes through the mill. Twin double type strip wipers located on both sides of the mill keep the coolant inside the mill housing so that it does not come out onto the strip and wrap onto the coil. However, when speed of the strip is high enough to keep the coolant from leaking out on the input side, an automatic wiper function opens the wiper on that side. When strip speed drops below that value, the wiper is closed again.

By automatically adjusting speed and roll pressure in response to variations in the thickness of the incoming strip, the mill consistently provides strip well within

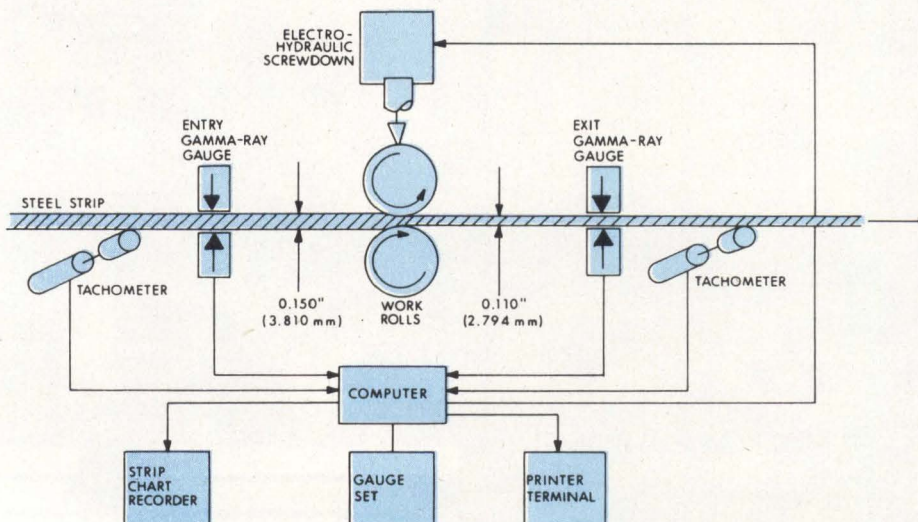
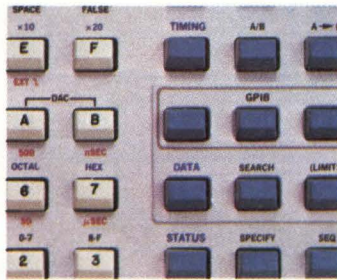


Fig 2 Schematic of Waterbury Farrel designed automatic gauge control system. During computerized operation, gamma-ray gauges continually monitor thickness of steel strip as it enters and leaves work rolls. Computer adjusts roll pressure in response to thickness variations of incoming strip. Tachometers (pulse generators) accurately measure length of strip entering and exiting mill

Biomation's K100-D -- no other logic analyzer even comes close.

No wonder the K100-D is our fastest selling new logic analyzer ever. It gives you 16 channels, 1024 word memory, clock rates up to 100 MHz, signal timing resolution to 10ns-plus a built-in display and keyboard control.

Biomation's K100-D puts it all right at your fingertips — more performance and features than any logic analyzer ever.



It starts with the micro-processor-controlled keyboard and interactive video display. To give you fast, precise control, the display serves as a comprehensive control status menu, with all selectable parameters in reverse video. There's a single, labelled key for each function, corresponding directly to status display choices. So guesswork is eliminated.

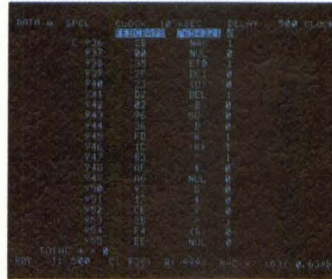
For example, in the data domain, you can direct the display to read in hexadecimal, octal, binary or ASCII, or any combination, by selecting one of four control buttons. There's also a unique "sequence" key that enables you to rearrange the order in which channels are displayed, to aid in data decoding, to simplify side-by-side comparison of timing signals and to enable you to cancel any channels you're not interested in seeing. A separate key controls horizontal expansion.

That gives you an idea of the K100-D's display versatility. Here's a picture of its astounding capture capability.

By providing timing analysis of signals as fast as 100 MHz, you can capture logic signals with resolution to 10ns. And the 100 MHz clock rate protects against obsolescence as the speed of your systems gets faster and faster. The K100-D also has a latch mode that can capture glitches as narrow as 5ns.



With the 32-channel input adapter, the K100-D is ideal for exploring the new world of 16-bit microprocessors. To give you unprecedented analysis capability, there's a built-in Auto Stop capability you can use to detect, record and display any match (or mismatch) between incoming data and previously recorded data held in a reference memory.



Or using Search Mode you can key in a specific word and the K100-D will find it in memory.

To get the full impact of the K100-D, you really do need to have it at your fingertips. That's why we would like to arrange a demonstration. Call us at (408) 988-6800. Or, for

more information, write: Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050.

GOULD
CIRCLE 44 FOR INFORMATION



PASS NO: 3
 OUTPUT GAUGE: 8.0 MILS 20.0% REDUCTION FROM 10.0 MILS
 TOTAL LENGTH: 15339 FT
 MATERIAL WITHIN +/-0.05 MIL: 15279 FT 99.6%

DISTRIBUTION OF OFF-GAUGE MATERIAL										
0.05 MILS DEV X	1	2	3	4	5	6	7	8	9	10
HEAVY (+)	9	3					1			9
LIGHT (-)	19	3	6	4						
CUMULATIVE PERCENTAGE:	99.8	99.8	99.9	99.9	99.9	99.9	99.9	99.9	99.9	100.0

Fig 3 Strip profile printout of pass 3 in management printout. Length of rolled steel within ±0.05 mil of 8.0-mil output is 15,279 ft, or 99.6% of 15,339-ft total length

ORDER: --- MATERIAL: .. 1075 ... DATE . 5/5/78 ... TIME 13:19:22
 GAUGE: 8.0 MILS LENGTH 15339 FT WIDTH 12.5 IN
 INITIAL GAUGE: 15.0 MILS STARTING TIME: 11:50:29
 TOTAL REDUCTION: 46.7% COIL TIME: 88.9 MIN
 TOTAL LENGTH ROLLED: 37864 FT ROLLING TIME: 55.3 MIN
 PRODUCTION: 3520 LB/HR DOWNTIME: 0.0 MIN

PASS	GAUGE (MIL)	REDUCTION (%)	TENSION		MAX MILL (LB)	MAX SPEED (FPM)	AVE SPEED (FPM)	ROLL TIME (MIN)	PASS LENGTH (FT)
			FRONT (LB)	BACK (LB)					
1	12.0	20.0	4335	4291	285	903/900	594	17.2	10230
2	10.0	16.7	3494	2486	180	734/1200	690	17.8	12295
3	8.0	20.0	3024	2587	235	915/1200	755	20.3	15339

Fig 4 Management printout of results during three passes through Z-mill. In this example, 12.5" wide coil of 1075 carbon steel was reduced in thickness by 46.7% from 15.0 mils down to 8.0 mils. Data for each pass show gauge in mils at end of pass, percentage gauge reduction during pass, tension on front and back winders (takeup or feed, depending on mill direction), maximum and average mill speeds, roll time, and pass length

minimum tolerances of ±0.0002" (0.0051 mm) on 0.045" (1.143-mm) thick strip up to ±0.00005" (0.00127 mm) on 0.005" (0.127-mm) thick strip. After each pass (upon request), the computer prints out (Fig 3) the nominal gauge, total feet in the coil, and number of feet within specified tolerances of ±0.00005" (0.00127 mm) up to ±0.001" (0.0254 mm). A management printout (Fig 4) provides a summary of all passes made by a particular coil of steel through the mill.

Multipoint Slowdown

Speed of the mill is automatically reduced for strip imperfections such as welds or edge cracks. Such cracks, if not compensated for, might propagate across the strip, causing the strip to break and stopping the mill.

Two 6-digit bidirectional wrap counters, driven by the tachometers connected to the winder shafts, measure total rotation of the winder shafts with a resolution of 0.01 wrap. The input wrap counter contains the number of wraps left and counts down toward zero; the output wrap counter starts at zero and accumulates the total number of wraps for the next pass.

Each time an imperfection or crack is noted, the mill operator pushes a button that causes the wrap

counters on the winders to record that spot and relay the information to the computer. The mill will be automatically slowed down by a multipoint function as the bad spot approaches the roll bite and will be automatically returned to normal speed when the bad strip clears the rolls. Information from the takeup wrap counter and printer (Fig 5) is entered into the computer so that automatic speed control can be used even during the first pass.

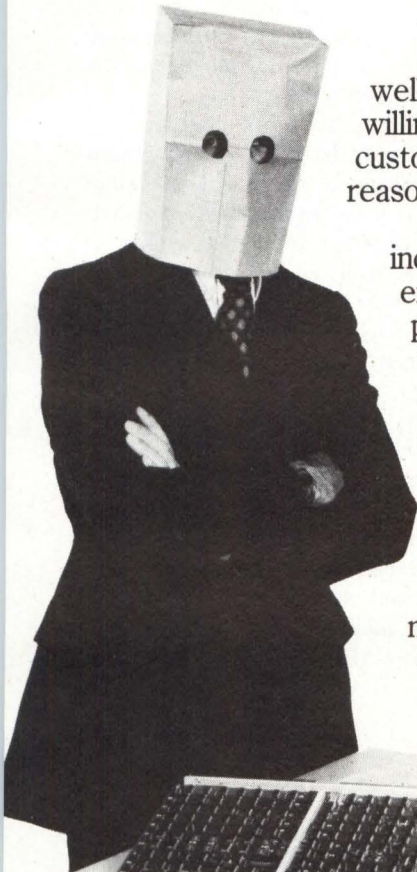
After the location of a bad spot is entered, the program keeps track of that location as the strip grows in length. Automatic slowdown will be continued for that spot until an erasure is ordered or a new coil is started.

As indicated on Fig 6, the actual slowdown path differs from that calculated. The mill is adaptively slowed from full speed (point A) to middle speed (point B) by a lead distance before the bad spot (point C) is reached.

Lag distance, that between the bad spot and when acceleration begins (point D), is at least as long as the lead distance so that the operator has time to erase the bad spot if desired. When full speed is again reached (point E), the mill maintains that speed until a slowdown point is reached for the next bad spot.

Four years ago, this man bet his job on our \$2400.00 single-board disk controller.

Both are still working.



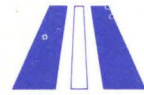
The man in the bag is product manager for a very well known company. Like all the rest of our customers, he's willing to give us a solid testimonial. However, like most of our customers, he happens to be an OEM. He has some pretty good reasons for wanting to remain anonymous.

But the point is, everyone who has ever paid our incredibly low price for one or a hundred disk controllers has ended up happy. We've given them as much or more performance than they could have bought for twice or even four times the money. Which is why we now have more than 2500 units installed.

Example: Our SMC11 for DEC PDP-11 computers will give you, among a lot of other things, contiguous sector data transfer and hardware error correction. Everything a big, expensive black box will do. For any storage module compatible disk drive. All on a single hex-wide board. All for \$3580. We have similar models to interface with Data General and Interdata. Floppy disk controllers, too.

Mail us the coupon now. It's an opportunity for you to find out how the least expensive disk controllers you can buy can also be the best. It's also a great chance for you to become unknown.

MiniComputer Technology



2470 Embarcadero Way • Palo Alto, California 94303 • (415) 321-7400

**The single-board disk controller company.
For DEC, Data General, and Interdata Computers.**

**Gentlemen:
Please send more information.**

Name _____

Title _____

Computer Type _____ Drive Type _____

Company _____

Address _____

City _____ State _____ Zip Code _____

Telephone () _____

CIRCLE 45 ON INQUIRY CARD

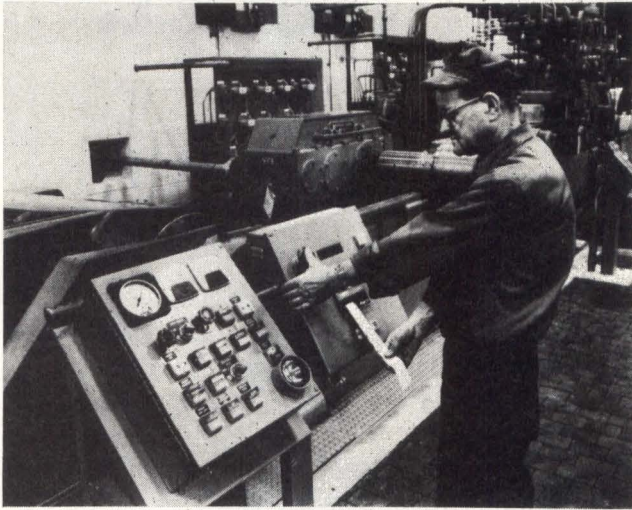


Fig 5 Closeup of takeup winder station control panel. Data from strip printer, entered into computer, are used for automatic control of mill speed

Automatic Stop

An autostop function is provided to accurately and quickly decelerate the mill to a stop at the end of each pass. This function continually monitors inputs from the mill and performs the necessary calculations. As represented in Fig 7, the mill is adaptively decelerated from full speed (point A) to slow (point B). Slow speed is maintained over a plateau distance (points B to C) for a specific period of time to allow

the operator to override the final stopping point if necessary. The mill is then stopped (point D), leaving the previous roll bite a precise distance in front of the work rolls.

As in multipoint slowdown, adaptive slowdown during the autostop sequence overcomes system inaccuracies and instabilities that prevent calculation of a 1-step slowdown distance from high to plateau speeds. Modulating the rate of deceleration allows the mill to reach plateau speed at the desired distance from the end of the coil in the minimum amount of time consistent with confidence that the mill will stop safely.

Calculated distance required to slow the mill is purposely larger than the actual distance (by an amount that increases with an increase in speed). This calculated slowdown distance error is periodically compensated for at the speed checkpoints indicated in Fig 7. Speed checkpoint spacing as well as deceleration speed are chosen to alternately slow the mill and hold it at set speeds for specific periods of time that allow mill drive inertia compensation and tension control circuits to function.

Control System Components

The controlling minicomputer is a Digital Equipment Corp PDP-8/M with 12k words of core memory and positive I/O bus, power fail/auto restart, and memory extension and timeshare. A 300-baud serial port allows interface to the data terminal and a 1200-baud serial port provides access to the magnetic card reader. Program loading is carried out through a PRS-01 paper tape reader.

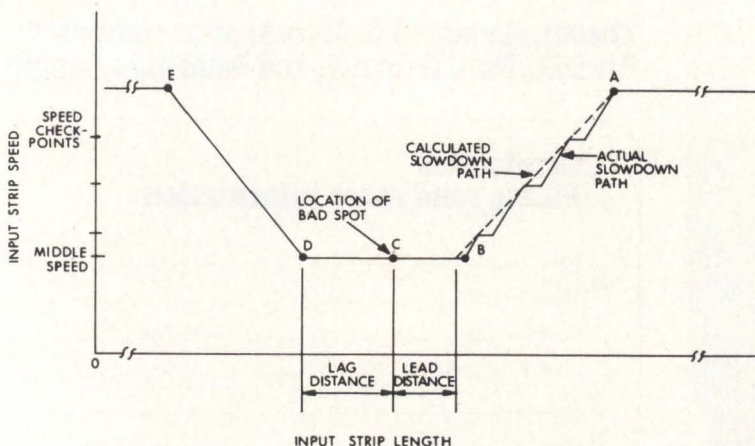


Fig 6 Linear representation of multi-point slowdown sequence for bad spot in strip. When input wrap counter is in coincidence with value at which mill must start to slow (point A), mill is adaptively slowed to middle speed (B) and actual location of bad spot is displayed. Distance that mill runs at middle speed before bad spot enters is lead distance (equal to distance between winder and work rolls). As bad spot passes through mill; value of output wrap counter is stored and slowdown point display starts to flash (C). Value in output wrap counter is new location of bad spot. Lag distance is length of strip between bad spot and location at which mill is accelerated back to normal speed (D). When accelerate point is reached, mill speeds up and slowdown point for next bad spot is displayed. Hold signal is sent when speed has returned to value at which slowdown began (E)



Custom color coded jumper



Many more of the same

We'll clone your jumper cables.

Call it cloning. Planned planar-hood. Or simply smart thinking. Just give us your jumper cable specs and we'll reproduce as many jumper cable duplicates as you need.

Fully tested, ready-to-install planar jumper assemblies that save you time, money and labor pains because we take total responsibility for them.

For all your interconnect needs from jumpers to planar cables and IDC connectors to complete custom assemblies,

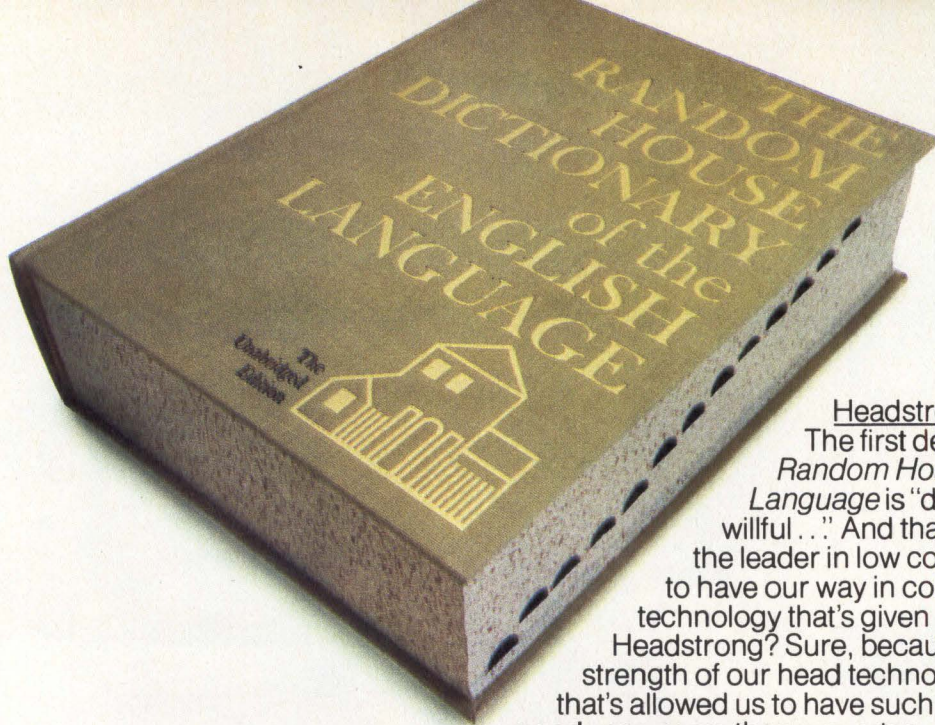
just check us out. You won't need to call anyone else.

For the name and number of our nearest distributor or rep, write Spectra-Strip, an Eltra Company, 7100 Lampson Avenue, Garden Grove, CA 92642. Or call (714) 892-3361 today.



When you're down to the wire

CIRCLE 46 ON INQUIRY CARD



Headstrong about leadership.

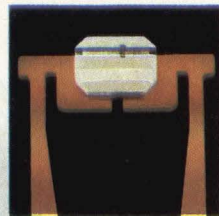
The first definition of headstrong in the *Random House Dictionary of the English Language* is "determined to have one's own way; willful..." And that's a fine explanation of why we're the leader in low cost disk storage. We're determined to have our way in controlling the read/write head technology that's given us our leadership position.

Headstrong? Sure, because it's the strength of our head technology that's allowed us to have such a good year: more than a quarter million floppy disk drives delivered. Proud of being headstrong? You bet. And proud of our heads-up OEM customers who specify Shugart products.

**We
headstrong
of**

Headstrong about technology.

The only sure way to control quality is to control the key technology responsible for that quality. You can do that only if you have depth in your R&D and manufacturing capabilities. At Shugart, we've got the strength and resources to develop and produce all our read/write heads. We've been doing it since day one. That's why Shugart read/write



head technology extends media life to over 3.5 million passes per track, and gives you a head life that exceeds 15,000 hours. And it's one of the big reasons why heads-up OEM's demand Shugart.

Because they know we're headstrong about controlling our technology.



Headstrong about R&D. We invest significantly more Research and Development dollars in floppy disk technology than any other manufacturer in the business. Shugart's commitment to R&D is responsible for our introduction of the first independently developed IBM-compatible floppy disk drive; the first, and now famous, Minifloppy™ and the first low cost fixed disk drive providing state-of-the-art Winchester technology. As your markets broaden, our product lines will grow to ensure your continued success.

We're committed to it. Shugart's

entire R&D effort is concentrated on

innovating and improving low cost disk storage products. It's our only business.

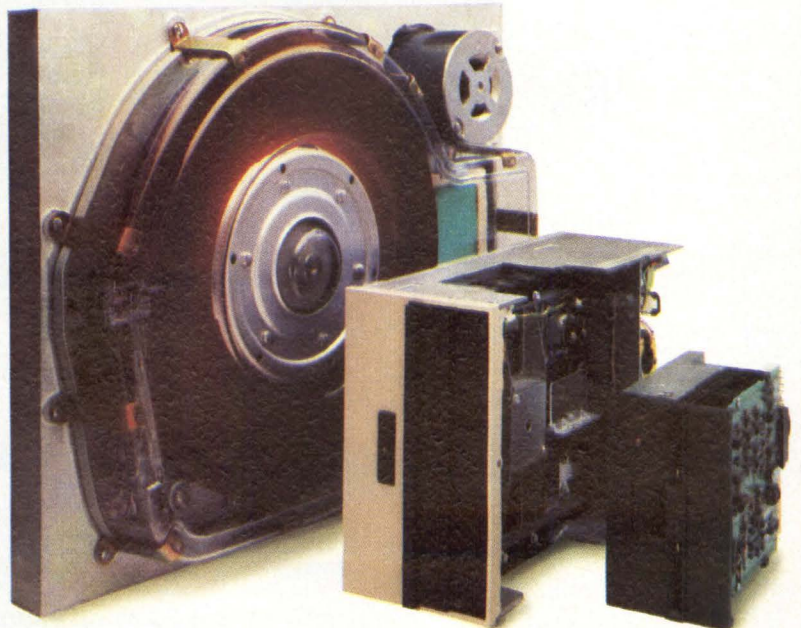
That's why we're so headstrong about R&D.



're and proud it.

Headstrong about delivery. In our business, innovation isn't enough. You've got to deliver high quality products in high volume. We're headstrong about our commitment to high volume delivery of low cost, rotating memory products. We fulfill that commitment by implementing production techniques developed by one of the best R&D and manufacturing engineering teams in the industry. Automated systems featuring high-speed conveyor and turret

assembly technology provide an unequalled manufacturing capability. And quality control at Shugart means testing 100% of the drives we manufacture. And these test procedures are tough — tougher, in fact, than any of the real applications where you'll be using our drives. Shugart Associates, Headquarters: 435 Oakmead Parkway, Sunnyvale, California 94086 (408) 733-0100; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 176006; Shugart products are also available from local Hamilton Avnet outlets.



 **Shugart**

The Headstrong Company

CIRCLE 47 ON INQUIRY CARD

FOR RENT...NOW...

Beehive's versatile and easy-to-use B100 and Mini Bee 2 terminals, both available for immediate short-term, low cost rentals today.

If you need a self-contained, feature-filled video display terminal fast, the B100 will fill the bill . . . and it's available today. Beehive International's B100 features both RS232C or current loop interface, has switch selectable transmission rates from 75 to 19,200 bps, and includes cursor control. You'll also like the addressable cursor. The terminal has an easy-to-read 12-inch non-glare screen which is formatted to display 24 lines with 80 characters per line. You can choose upper and lower case characters, too. The B100 has a total page memory of 1920 characters, and the 82-key, ANSI compatible keyboard features auto repeat, 2-key rollover and alpha lock. The addressable cursor lets you directly position by line and column, and an erase mode allows you to erase from cursor to end of line, from cursor to end of memory, and clear. You'll also find operation more efficient because of B100's 11-key numeric pad with decimal and additional function keys. Communications mode is Full Duplex (Echoplex), Half Duplex, and Block (asynchronous 10 or 11-bit word). It's ready for you now.

The low-rental rates on Mini Bee 2 will make you happy if you need a TTY-compatible terminal with cursor control and a detachable keyboard. Beehive's Mini Bee 2 is a stand-alone, operator/computer accessible remote display terminal with a detachable keyboard. You use Mini Bee 2 to transmit and receive data serially through an RS232C interface at any of several preselected transmission rates to a maximum of 9600 baud. Mini Bee 2 has a 12" rectangular monitor which displays 25 lines with 80 characters per line. It has a total page memory of 2000 characters, and each character is generated from a 5x7 dot matrix with two dot spacing between adjoining characters. Communications mode can be full duplex, half duplex, 10 or 11-bit asynchronous word. Mini Bee 2 also features character-by-character transmission, an escape sequence mode for unique CRT functions, and an erase mode. It's also available off-the-shelf from REI immediately.

Rental Electronics, Inc.
Another of the **AMERICAL** companies



More than 12,871 state-of-the-art instruments . . . off-the-shelf, throughout North America.

- Tell me more about B100 and Mini B2 now!
Call me at _____
- Send me a copy of your free illustrated Rental Catalog.
- I might be interested in buying—on a money-back guarantee basis—some of your late-model, well-maintained "previously owned" equipment. Please send me your Equipment Sales Catalog.
- I have a pressing need right now for the following: _____

Please phone me immediately at _____

NAME _____ TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

PHONE NUMBER _____ EXTENSION _____

Complete this coupon and return it today to
REI, 19347 Londelius St., Northridge, CA 91324.

GSA #GS-04S-21963 Neg © 1978 Rental Electronics, Inc.

Northridge, CA (213) 993-7368
Anaheim, CA (714) 879-0861
Mountain View, CA (415) 968-8845
Dallas, TX (214) 661-8082
Houston, TX (713) 780-7218
Burlington, MA (617) 273-2770
Oakland, NJ (201) 337-3757; Gaithersburg, MD (301) 948-0620
Des Plaines, IL (312) 827-6670; Ft. Lauderdale, FL (305) 771-3500
Cleveland, OH (216) 442-8080; Seattle, WA (206) 641-6444

Rexdale, Ontario (416) 675-7513
Montreal, Quebec (514) 681-9246; Vancouver BC (604) 684-6623

CIRCLE 48 ON INQUIRY CARD

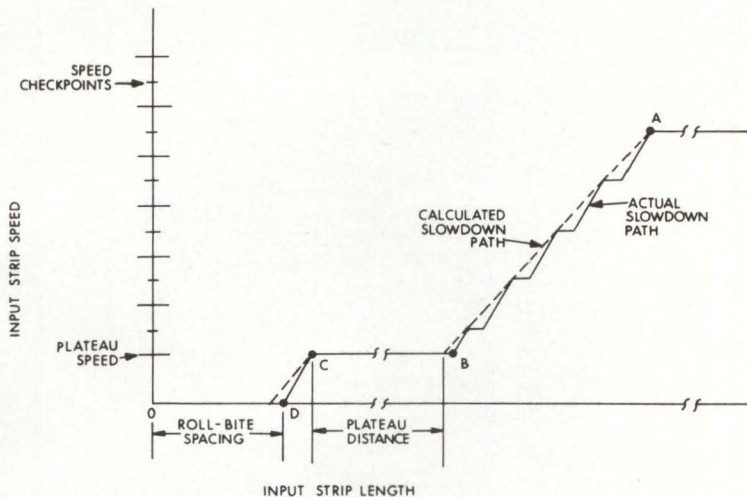


Fig 7 Linear representation of auto-stop sequence. When input wrap counter is less than or equal to value of point at which mill is required to start its descent from present speed to plateau speed, decelerate signal causes mill to begin to slow (point A). As mill speed changes, new slowdown point is calculated. At frequent speed checkpoints, input wrap counter is compared to new slowdown point and, if wrap counter is greater than new point, hold signal is sent and mill runs at constant speed until coincidence between wrap counter and new point is reached. At coincidence of two values, another decelerate signal is sent and mill continues its descent. Adaptive slowdown continues until plateau speed is reached and hold signal is issued (B). Mill now runs at constant speed until coincidence between input wrap counter and displayed value (C) slows mill to stop (D)

Continuous noncontact measurement of the strip is provided by a Laboratory for Electronics radiation (gamma-ray) gauge system. Thicknesses can be measured linearly to 3000 μm of steel using a single radiation source of Americium 241. Typical source specifications are $\pm 1.5\text{-}\mu\text{m}$ accuracy on a sheet thickness of 700 μm with a 25-ms response.

Locating gauges on the strip is automatic and repeatable. The operator actuates a pneumatic cylinder via desk-mounted switches to move gauges on or off the strip. Limit switches deactivate the cylinder at on-strip and off-strip positions. Gauges are standardized at least every eight hours to compensate for aging of the radioactive source.

Digital tachometers (pulse generators), located on either side of the work rolls and driven by measuring wheels in contact with the strip, convert shaft rotation into two channels of square wave outputs. Transitions give shaft position information while phase relationship between the channels indicates the direction of rotation. Information from the two tachometers is provided to corresponding digital counters for a visual indication of accurate and high resolution measurements of the length of strip entering and leaving the mill.

The magnetic card reader is a Vertel series KB-31 Microloader™ with RS-232 interface options. Read/write cycle time for a stripe of information on the plastic card is 5 s. Read speed is 3.1" (7.87 cm)/s. A typical data block is 2.81" (7.14 cm). For this applica-

tion, a 6-position DIP switch in the reader has been replaced by a 7-position one to provide convenient switching between ROMs in the printer terminal and those in the computer.

A Texas Instruments model 743 (Silent 700) data terminal with 20-mA current loop interface and mark parity option prints mill program information and communicates with both the Waterbury Farrel system diagnostic program and those used by the computer manufacturer. There is no interference with system operation and the next coil or pass can start while the printer is still providing data on the last one. Except to advance paper, the terminal's keyboard is not used in normal mill operation.

A dual channel strip chart recorder, running at a speed proportional to the strip, provides a permanent record of the input and output strip thickness deviations. The chart is driven by a stepping motor that receives signals from the tachometer on the output strip. Chart pens are driven by analog deviation signals. Tachometer information and deviation signals are switched automatically with a change in mill direction.

Digital panel meters convert analog thickness deviation signals to the digital format used by the automatic gauge control system. The meters are triggered when the mill is running by a digital pulse supplied by the control system each time a reading/conversion is made. Circle 190 on Inquiry Card

"With microprocessors why take chances on

We keep hearing that microprocessors are all things to all people. Yet, at AMI, orders for custom-designed circuits continue to grow. And, when you take a realistic look at standard microcomputer systems versus made-to-order circuits, it isn't hard to see why.

First, consider capabilities. While it's true that many products using custom circuits could be controlled by microprocessor systems, there are some that clearly couldn't.

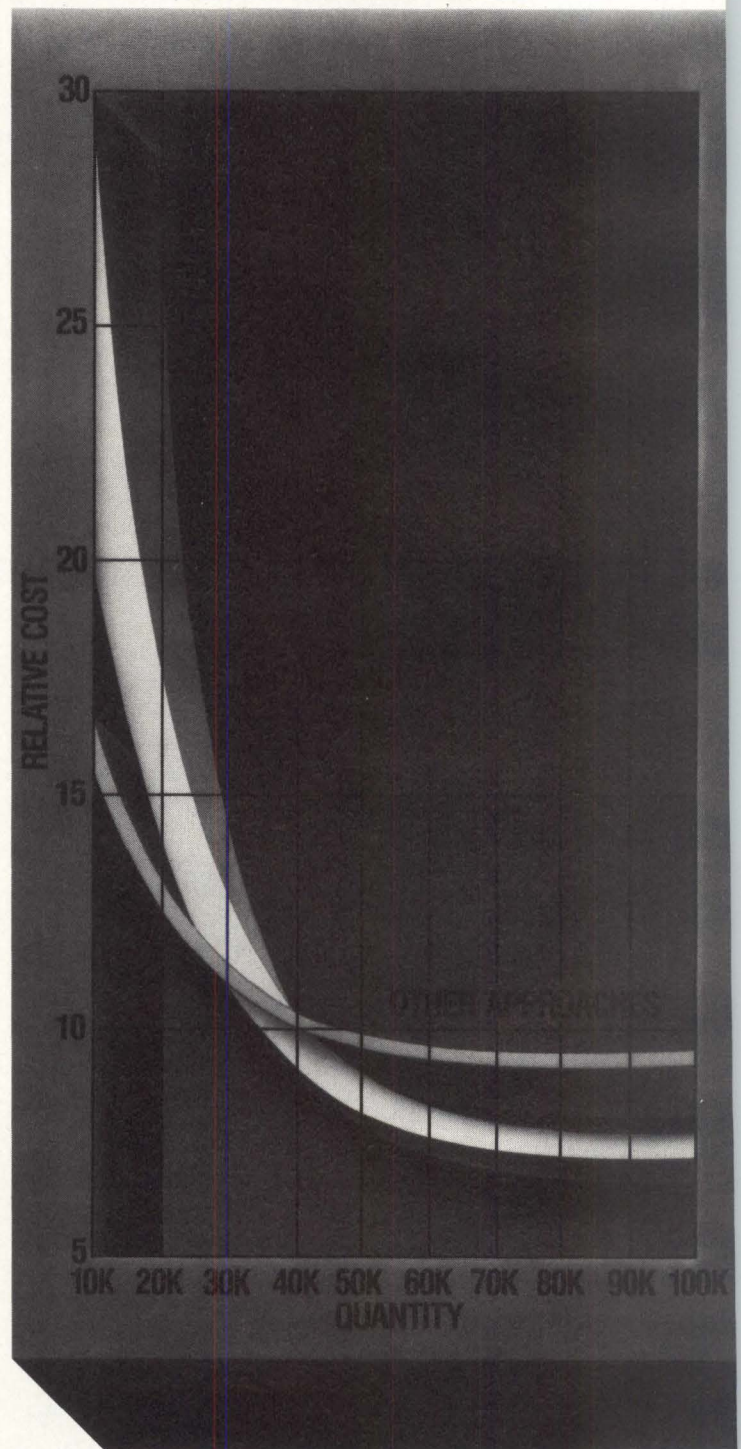
For instance, we just produced a custom MPU for a commercial avionics system. It required a series of interrupts that the architecture of a standard microprocessor wouldn't provide. Special display drives, A/D conversion on inputs and specialized high-speed calculations are other areas where off-the-shelf products are clearly out-classed in this application.

Second, look at the real costs of both systems. On the one hand, custom assures the minimum number of circuits. And, although there is some start-up expense, this is easily amortized over the life of the product. On the other hand, standard microcomputer configurations usually require a number of components, taking up more board space, assembly effort and testing time. These costs can run you at least 50% of each part's price. So a multi-circuit microprocessor system often represents as much in indirect costs as in the price of the circuits themselves. These factors alone can make a standard system less cost-effective than a custom job. And that doesn't even include the time and expense involved in programming. You can spend as long getting your software written as we would building the custom hardware.

Standard and custom should be partners, not competitors.

In many cases, a 'mixed solution' works

Is custom expensive? The chart shows that it can actually be more cost-effective than standard devices as the unit volume approaches 30,000 and when assembly, programming and test are taken into consideration.



...s a dime a dozen, custom LSI?"

best—a combination of standard microprocessor and custom peripherals. For instance, we designed a special circuit for a consumer entertainment company to expand the I/O capabilities of a standard 8048 MPU. And for a manufacturer of business equipment, we're working on plans to customize an S2400 (our 4-bit microcomputer) to provide ROM and RAM variations, adding a custom interface chip and clock. To help them get the product to market while we're developing this more cost-effective solution, we're providing them with our standard S6802 8-bit microprocessor.

An advanced home computer provides another example of standard and custom compatibility. A Z-80 microprocessor is supported by three AMI custom circuits—address, I/O and data chips. This trio contains the equivalent of 600 standard SSI and MSI integrated circuits. And, having a fast MPU to work with, our circuits were designed to run at seven MHz. Most important, they perform the intricate graphics functions, lowering the cost to the point where the computer does more for the money than competitive products.

It's apparent that microprocessors, far from shrinking the need for custom, have actually opened up vast new areas of application. In fact, you now have three ways to go—full custom, standard microprocessor or a mixture of both. Since we're the leading custom LSI company and a major supplier of microprocessors (the 4-bit S2000, 8-bit 6800 and 16-bit 9900) and memories, we're in the best position to supply your complete microprocessor system needs.

Want to know more? It's in the book.

Titled "Six Steps to Success with Custom LSI," our new brochure should answer many of your questions. Such topics as timing, options, processes, test and manufacturing are thoroughly covered, along with a variety of case histories.

It also explains the flexibility that AMI offers. Since we work in 25 variations of four MOS

processes, we don't have to reduce your product's capabilities to fit design or production limitations.

Unlike smaller companies, we're also organized to work with you in any of three different ways. We'll design and produce your circuit from scratch. Or you can handle the design in-house or through a third party, then we'll manufacture it. Or we can arrange a joint venture, where a team from your company and a team from ours work together to create a succession of new products.

Whichever way you decide to go, you'll have the satisfaction of working with the company

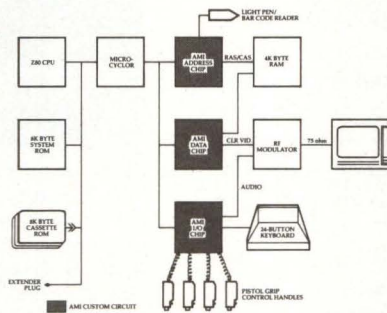
that wrote the book on custom MOS. Since 1966, we've created more than 1200 different circuits. We're continually finding new ways to get more onto a chip (up to 67,000 transistors at last count) in less time. As a result, we average seven months from firm specifications to fully tested circuits—the fastest turnaround in the industry.

Why don't you explore all these opportunities with us? To start with, ask for a copy of our book. Write or call AMI Custom

Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330. Or contact one of these AMI sales offices: California, (213) 595-4768; Florida, (305) 830-8889; Illinois, (312) 437-6496; Indiana, (317) 478-9339; New York, (914) 352-5333; Pennsylvania, (215) 643-0217; Texas, (214) 231-5721; Washington, (206) 687-3101.

And, if you'd like your questions answered in person, we'll make a half-hour presentation right in your office. We think it will help convince you that getting into custom isn't chancey at all.

AMI
AMERICAN MICROSYSTEMS, INC.



A triple option: this home computer uses a standard microprocessor, three AMI custom peripherals, plus standard ROMs and RAMs to achieve more performance for the money than any competitive system.

Traffic Control System Uses Laser Communication Link

Traffic around the North Georgia Regional Postal Center in Atlanta is being controlled by what is believed to be the first system of its kind to transmit data over laser beams. Built by the Sperry div of Sperry Rand Corp, the traffic control system uses low intensity lasers instead of traditional overhead wires or underground cables for communication. Because this is a relatively small system, all control is maintained by microcomputers—at both local intersections and the master station. There is no need for the central minicomputer that would be used in larger systems of the same type.

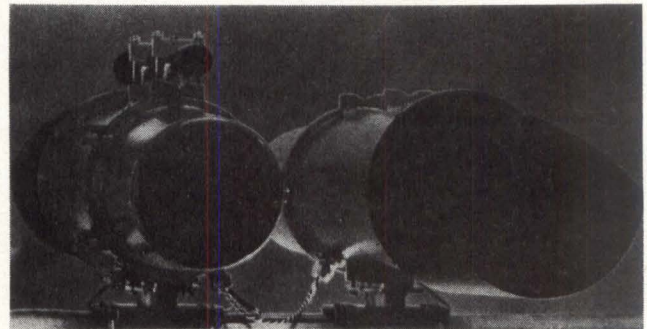
Vehicle detectors at controlled intersections interface to intersection controller microcomputers that in turn transmit traffic condition data over laser beams to a master subsystem. A microcomputer in the master subsystem sends commands back to the intersection controllers over laser beams to govern traffic signals.

Tests have shown that messages can be sent up to 10 mi (16 km) in clear visibility conditions and 2000 ft (610 m) in heavy fog. The communication subsystem functions in heavy rain, snow, lightning, and high winds, and has been certified as totally eye safe. In addition, since laser units are mounted on existing signal poles, their use reduces system installation time, cost, and traffic disruption and eliminates the need for telephone company service.

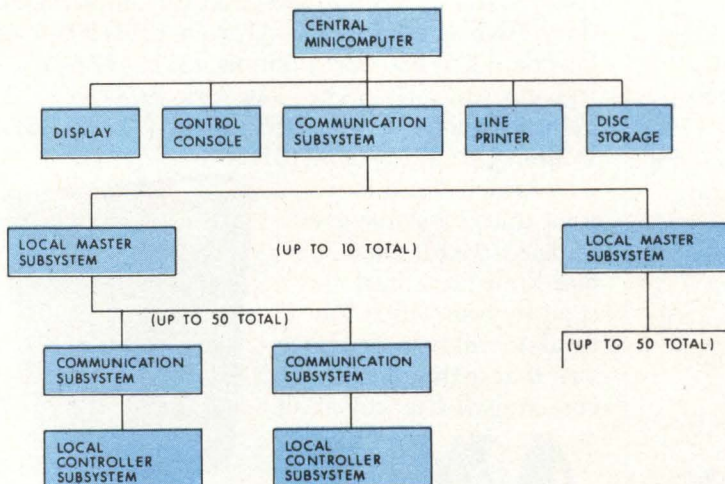
Although only a small number of intersections are controlled at the Atlanta application, laser communication systems can be used to control traffic on arterial

roads and in urban grids with up to 500 intersections. For such large systems, however, further communication subsystems, additional system components, and a central minicomputer would be required (see diagram).

Each local master subsystem in a Sperry SRT-5000 electro-optical traffic control system can handle up to 50 local controller subsystems, and each central minicomputer can maintain up to 10 local master subsystems. In addition to its control operations, the minicomputer also performs realtime data storage, reporting, and display functions, and provides operator command capabilities. Expansion of a small electro-

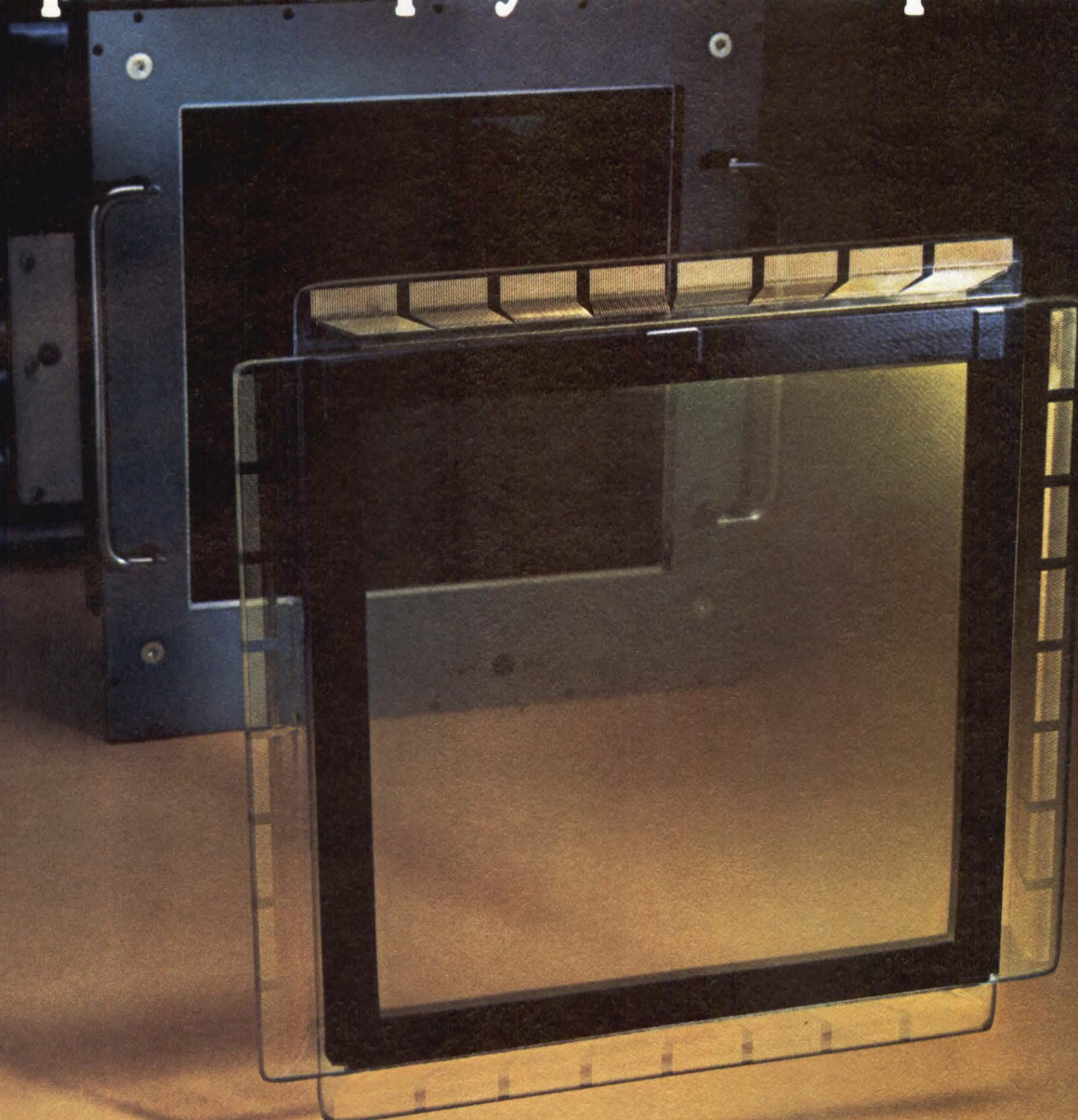


Laser beam communication subsystem for traffic control. Low intensity laser, comparable in power to normal flashlight beam, is certified to be totally eye safe. Transmission distance is 10 mi (16 km) under best conditions and 2000 ft (610 m) in heavy fog. By mounting laser units on existing signal poles, usual expense of leased telephone lines or buried cables is eliminated



Sperry SRT-5000 electro-optical traffic control system. Microprocessor-based local controller subsystems detect increases and decreases in traffic volume. That information is sent to a local master subsystem, which is also microprocessor based. Local master subsystem combines similar information from controllers at up to 50 intersections and transmits all information to central minicomputer, which determines what, if any, changes should be made in traffic light operation and relays those orders back through master subsystems to controller subsystems. Up to 500 controllers can be accommodated. Relatively small system installed in Atlanta, Georgia consists of only a local master subsystem and some local controller subsystems plus laser communication subsystems, without expensive central minicomputer

A new source for plasma display heads and panels.



Plasma technology has come into its own at Interstate Electronics!

To respond to new requirements and to meet increasing demand, we have rounded out our plasma product family by adding glass panel production. Our new panel manufacturing source is solidly in production to meet all of your program requirements.

This means immediate availability to you of "off the shelf" plasma display panels and heads, as well as all of the other products in our plasma display family.

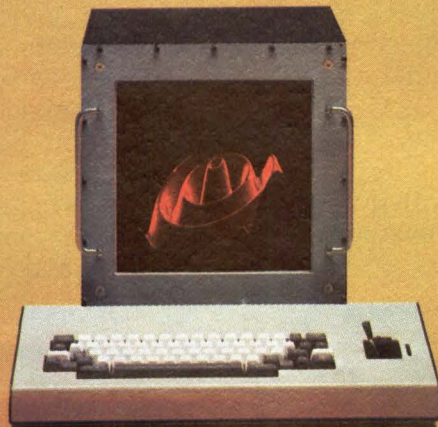
You now have a complete source for plasma products—Display heads, terminals, special-requirement

products, and panels.

Call today for complete details on availability, quantity, prices and special sizes. Write or call Don Poulos, Product Manager, Interstate Electronics

Corporation, 1001 East Ball Road, P.O. Box 3117, Anaheim, CA 92803. Telephone (714) 635-7210.

Remember, that's Interstate Electronics—specialists in information processing and display for more than 20 years.

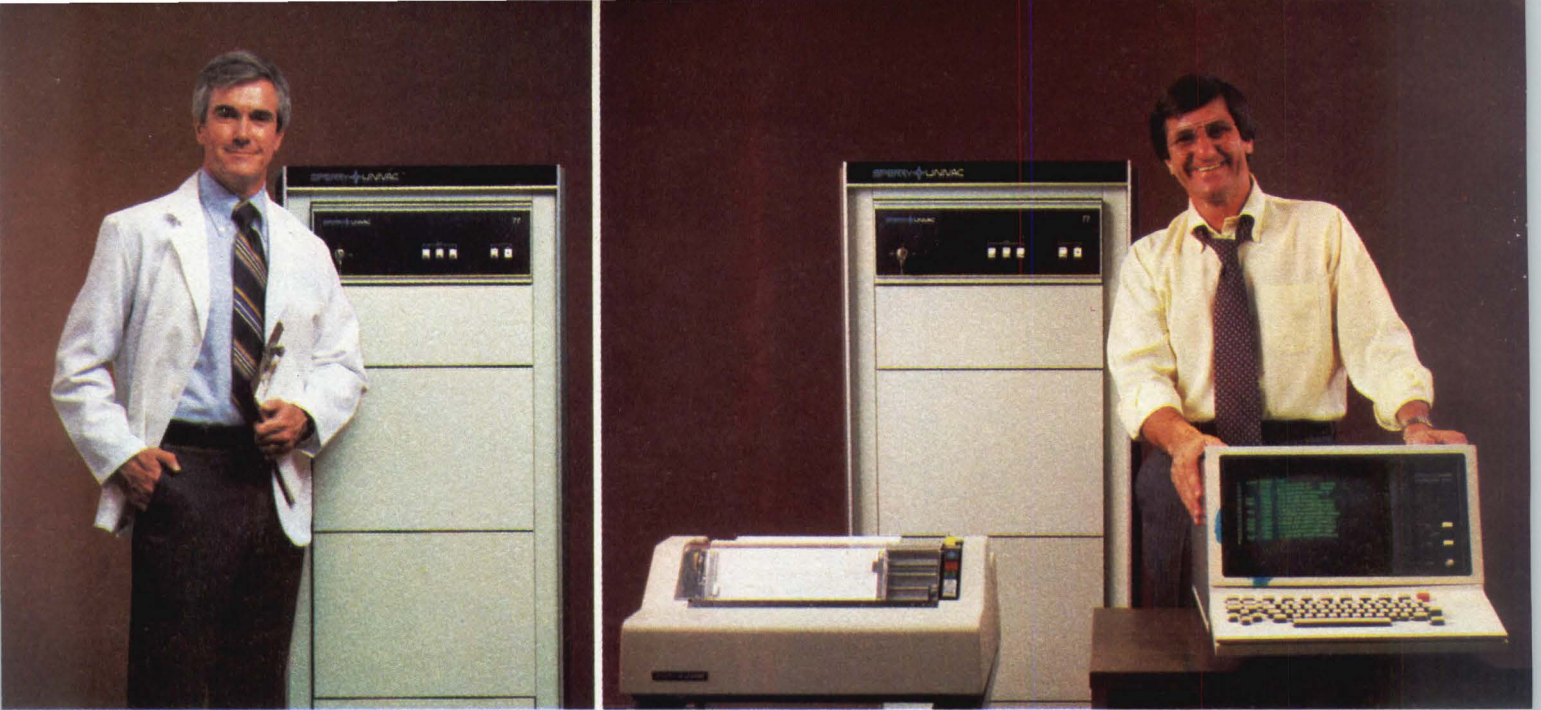


**INTERSTATE
ELECTRONICS
CORPORATION**

SUBSIDIARY OF **ATC**

Information Processing and Display.
Systems. Products. Services.

CIRCLE 49 ON INQUIRY CARD



Introducing the Sperry Designed exclusively for three

The Sperry Univac V77-800 Miniframe is the newest and most powerful mini we've ever built — a high performance, multi-use, general-purpose minicomputer system designed for both commercial and scientific data processing. It has a memory range from 128K bytes to 2 megabytes (with error correcting memory) and a 150 nanosecond CPU with integrated cache of 1024 bytes. Plus 12K bytes of user programmable writable control store.

There's an optional new high speed 64-bit floating point processor that works in conjunction with a new globally optimized ANS '77 FORTRAN.

No wonder our three most important customers think so highly of it.

OUR OEM CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

The Miniframe is customer microprogrammable. So an OEM can implement his own firmware packages. And with the many software packages we offer, the OEM can add all the bells and whistles he wants.

The Miniframe comes with our largest instruction set ever. So OEM's with their own software have much more flexibility in design.

The Miniframe speaks PASCAL, the powerful new language for scientific, commercial, and system programming that most competitive systems still can't speak. And of course, it also speaks COBOL, FORTRAN and RPGII.

More good news is that the Miniframe is compatible with the rest of the V77 product line.

OUR SYSTEM HOUSE CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Naturally, system houses want all the features OEM's do. And more.

So we gave them more.

More operating systems, for example. Choose from VORTEX or our new SUMMIT — an interactive, multi-terminal system with transaction processing and data base management. It gives you easy editing, screen formatting, and documentation aids. Plus speedy, comprehensive program development.

System houses also think PASCAL is important. Because it's more efficient, easier to maintain, expand, and modify.

The Miniframe brings systems builders a new query language called QL-77. It features inquire and report facilities. And interfaces



Univac V77-800 Miniframe. of our very best customers.

directly to TOTAL*, the data base management system. So preprocessing and intermediate handling are a thing of the past. Finally, TOTAL also gives you complete data base access and file access security.

OUR END USER CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Take all the features we designed in for OEM's and system houses and say ditto for the end user.

But we didn't stop there. We also pressed a few special hot buttons just for end users.

Consider QL-77, for example. End users will love our new query language because it reduces the amount of application programming. By storing query language procedures right in the data base file. Where they can be easily and quickly recalled and executed at any time.

Once again, SUMMIT, our new operating system, helps the end user handle transaction processing. Without any additional, expensive software. It's also the right answer for a multi-tasking, "fully-implemented" distributed processing system.

Finally, the Miniframe supports DCA and conventional protocols. So you can talk to both SPERRY UNIVAC and IBM hosts.

YOU'LL KNOW WE DESIGNED THE MINIFRAME JUST FOR YOU.

No matter what your application, no matter what your need, the Miniframe may just be the answer.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, ext. 536.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

We're Sperry Univac.

And our new Miniframe is going to solve some very big problems.

SPERRY UNIVAC
SPERRY UNIVAC IS A DIVISION OF
 SPERRY RAND CORPORATION

*TOTAL is a registered trademark of Cincom, Inc.

"At Lockheed-Georgia, we've found that color improves the flow of management information."

Robert B. Ormsby, President Lockheed-Georgia

Like so many other companies, Lockheed-Georgia is realizing the many advantages that color adds to desk-top computers. They're using our Intecolor 8053 for a variety of applications, including daily financial updates and on-line jobs status. And they're processing information faster and more accurately. Because color communicates better.

We should know. We have the largest selling color graphics terminal in the world. That's why we can offer the Intecolor 8053 desk-top computer for just \$3550.* No other system on the market — not even black-and-white models — can match it for value. It has an ample 19" diagonal screen, 8 foreground and background colors that speed comprehension and reduce operator fatigue, plus the power and flexibility to handle a wide range of daily operations. Extended DISK BASIC is a standard feature. And Intecolor's dual 8" floppy disk drive gives you up to 591K bytes of storage. All for \$3550.*

If you need help in a hurry, relax. Cash with order guarantees delivery of a single evaluation unit at the 100-unit price within 30 days, or your money back. Like all Intecolor units, it's covered by a six-month warranty.

For more information about how we can relieve your information burden, contact your representative today. Join the many companies who are finding out what a difference color can make.



Unretouched photo of screen

*100 unit price: USA domestic \$5075 single unit price

ISC SALES REPRESENTATIVES: AL: 205/883-8660, AK: (GA) 404/449-5961, AZ: 602/994-5400, AR: (TX) 214/840-2169, CA: Alhambra 213/281-2280, Goleta 805/964-8751, Irvine 714/557-4460, Los Angeles 213/476-1241, Mountain View 415/964-9300, San Diego 714/292-8525, CO: 303/759-0809, CT: (MA) 617/879-7530, DE: (PA) 215/688-7325, DC: (MD) 301/656-3061, FL: Orlando 305/425-5505, Ft. Lauderdale 305/776-4800, Melbourne 305/723-0766, Tallahassee 904/878-6642, GA: 404/455-1035, HI: 808/524-8633, ID: (UT) 801/973-7969, IL: (No.) 312/564-5440, (So.) (MO) 816/765-3337, IN: (IL) 312/564-5440, IA: (MO) 816/765-3337, KS: (MO) 816/765-3337, KY: (OH) 513/434-7500, LA: 504/626-9701, ME: (MA) 617/879-7530, MD: 301/656-3061, MA: 617/879-7530, MI: 313/588-2300, MN: 612/822-2119, MS: (AL) 205/883-8660, MO: 816/765-3337, MT: (CO) 303/759-0809, NB: (MO) 816/765-3337, NV: (AZ) 602/994-5400, NH: (MA) 617/879-7530, NJ: (PA) 215/688-7325, NM: 505/292-1212, NY: White Plains 914/949-6476, Holcomb 716/657-6309, NC: 919/682-2383, ND: (MN) 612/822-2119, OH: Cleveland 216/267-0445, Dayton 513/434-7500, OK: (TX) 214/840-2169, OR: 503/620-5800, PA: (East) 215/688-7325, (West) 412/892-2953, RI: (MA) 617/879-7530, SC: 803/798-8070, SD: (MN) 612/822-2119, TN: 615/482-5761, TX: 214/840-2169, El Paso Area (Las Cruces, NM) 505/523-0601, Houston Only 713/780-2511, UT: 801/973-7969, VT: (MA) 617/879-7530, VA: (MD) 301/656-3061, WA: 206/455-9180, WV: (PA) 412/892-2953, WI: (IL) 312/564-5440, WY: (CO) 303/759-0809, **EUROPEAN EXPORT SALES:** EUROPE: (MA) 617/661-9424, BELGIUM: Brussels 02-242 36-04, FRANCE: Rueil Malmaison 749-49-37, GREECE: Athens 642-1368, ITALY: Roma 805-647/872-457, THE NETHERLANDS: Poeldijk 01749-7640, SPAIN: Barcelona 204 17 43, SWEDEN: Vallingby 08-380-370, SWITZERLAND: Mutschellen 057-54655, **UNITED KINGDOM:** Bournemouth 0202-293-115, **WEST GERMANY:** München 089-31881, **AUSTRALIA & NEW ZEALAND:** Melbourne 543-2077, Meadowbank 808-1444, Chermside 59-6436, Wellington 64-4585, Auckland 876-570, **CANADA:** Datamex, Ltd. (Distributor) Dorval 514/636-9774, Ottawa 613/224-1391, Toronto 416/787-1208, Vancouver 604/684-8625, **CENTRAL & SOUTH AMERICA & CARIBBEAN:** (GA) 404/394-9603, **MEXICO:** Monterrey 564-876, **FAR EAST:** (CA) 213/382-1107, **HONG KONG:** 5-742211, **JAPAN:** Tokyo 402-8596, **TAIWAN:** Taipei 02-7026284, **MIDDLE EAST:** IRAN: Tehran 891148, **ISRAEL:** Tel Aviv 266-291, **KUWAIT:** Kuwait 438 180/1/2, **LEBANON:** Beirut 221731 260110, **SAUDI ARABIA:** Jeddah 27790, Riyadh 25083-39732, **UNITED ARAB EMIRATES:** Sharjah 24068. For sales and service in other countries contact ISC headquarters in Norcross, GA., U.S.A.



Intelligent Systems Corp. □ 5965 Peachtree Corners East □ Norcross, GA 30071 □ Telephone 404-449-5961 □ TWX 810-766-1581

CIRCLE 51 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

optic control system to include more intersections up to the 500 maximum is relatively easy and inexpensive compared to systems using telephone lines or buried cables, since only free air space is used for data transmission. No new lines or cables have to be added and little or no disruption of traffic is necessary.

Data transmission is accomplished using time division multiplexing (TDM) with a single voice bandwidth channel. A typical repeater network consists of a pair of optical transmitter/receivers (transceivers) operating in the near infrared spectrum region. Commands are transmitted from the master station to local stations, and data are returned to the master station through the network via these transceivers.

A local master subsystem has capabilities and flexi-

bility beyond mere transfer of data. It also logs and analyzes local equipment performance and telemetered traffic flow data and allows a portable test unit to be attached for manual operation of any local intersection. In a small installation, not requiring a wide range of peripheral online data storage and reporting functions, the master subsystem can be installed at a street side location.

Signal timing plans stored at each local controller, or transmitted periodically from the local master, can be selected at any or all of the intersections on the same local master. Plan selection may be a function of time of day and day of week, or as requested by an operator.

Circle 191 on Inquiry Card

Danish Computerized Mail Processing System Provides 1-Day Turnaround

From the time a letter enters the Central Sorting Office of the Post Telephone and Telegraph in Copenhagen, Denmark until it leaves enroute to its recipient it is directed by computers. Nearly 2.9 million pieces of first class mail from throughout Denmark are handled each day—and delivered within one day.

Ten Control Data System 17 computers configured in dual systems within five climate-controlled rooms sort, bag, and direct mail to specific trucks and railroad cars for final delivery. Each pair of computers handles a particular mail sorting and moving function. Operations handled by the computers include determining the drop point for incoming mail bags going to electronic sorting machines, directing trays of letters to certain areas of the building that represent geographic locations in Denmark, and then relaying bags of sorted mail to the proper loading areas. Capability built into the system allows both 1-day mail turnaround and capacity for many years of operations without increase in number of employees.

Although the computers stop and start the transporting and sorting equipment, a serial transmission loop has been incorporated for most of the system because of the thousands of required measuring and control signals. For instance, there are 1000 conveyors, each with six signals, in addition to many other controlled devices. Direct digital input/output is used on only a few configurations.

Special electronic control terminals throughout the 16-acre building are addressed individually by the computers. Control signals from the computers are first sent to the terminals and then used to activate 220/

380-V relays in switching circuits to control the equipment. These control terminals also accept status signals from sensors throughout the many circuits and transfer those data to the computers via the transmission loop.

Software was developed using structured methods for two main realtime functions: automatic control of the equipment and operator/system communication. Automatic control for the most part is performed on a cyclic basis, the fastest cycle being 0.2 s, where the terminals are polled for a new status and new control signals are issued. The operator communication subsystem handles all commands from the operator, such as start or stop groups of conveyors, open or close sorting departments, and change sorting tables. Reports on mail loss as well as statistics on the amount of mail and the availability of equipment are printed on request.

In software development a program-design language was used to describe and document modules. To back this up, a system was developed for automatic testing of programs and for quality assurance.

All software was specially designed and is unique to this project. Even though a total of 30 man-years was spent in the software development phase practically none of the software can be used directly anywhere else. The only exception would be if a terminal loop were reused. Then, depending on switching circuits, some software modules might be reusable.

Control systems contain dual 1784-1 computers via an inter-CPU-memory bus. Each computer is equipped with realtime clock, teletypewriter, paper tape reader, communications link to a central command computer, and the necessary terminal loop controllers. Micro-computer memory ranges from 46k to 96k bytes.

Circle 192 on Inquiry Card

DC&AS BRIEFS

**Automatic Controllers Position Tables
In Up to Four Axes**

A 12-V bus on the Anomatic™ controllers interconnect CMOS logic and controls with TTL microprocessor, P/ROM, and ROM. Because TTL portions are concentrated in a single section of the PC board, noise immunity of 4.8 V is realized throughout. The system can be programmed from internal memory, paper tape, cassettes, or magnetic cards. A built-in P/ROM programmer to provide nonvolatile memory and full editing capabilities for stored programs are included.

Programmed linear and circular interpolation up to four axes as well as several subroutines are provided. The automatic positioning table controllers are offered by Anorad Corp, 115 Plant Ave, Smithtown, NY 11787. Circle 193 on Inquiry Card

**Microprocessor Based Machine Tool Controller
Fits Into Closed Loop System**

Machine tool operation including 2-axis linear and circular interpolation and 3-axis point-to-point positioning can be controlled by the Micro-Hystep introduced by Hyper-Loop, Inc, 7459 W 79th St, Bridgeview, IL 60455. As many as 1000 blocks of random absolute and incremented program data, input through a panel mounted alphanumeric keyboard, can be stored.

A built-in online fault detector warns the operator if an operational problem occurs. Standard features of the microprocessor based unit include a 9" (22.9-cm) CRT display. The complete unit is a single compact console measuring 19 x 14 x 24" (48 x 36 x 61 cm). The controller, interfaced with a Hyamp II or III dc servo drive by the Commander I DAC module and combined with a motor, provides a complete closed loop digital control system.

Circle 194 on Inquiry Card

**DNC Offers Convenience of Programmable
Controller and Flexibility of Computer**

A general purpose microprocessor based computer and associated I/O options make up the System V direct numerical control offered by Unico, Inc, 3725 Nicholson Rd, Franksville, WI 53126. Modes of operation include entry for altering contents of memory locations; test for diagnosing hardware problems; program for entering application programs; step for testing operation of application programs; load for entering diagnostic programs, application programs, and system data; store for saving manually entered or altered program; and

run for normal system operation. All use the keyboard and display to select processor or memory location for alteration or observation.

A keyboard/display unit consists of a 48-button input keyboard and a 16-digit output display. Combined with the associated output display, the keyboard can be used to enter programs, load data, alter instructions, adjust settings, save data, and diagnose problems. The display module can be used for loading mass storage through paper tape or cassette. A power supply unit provides power for processor, memory, and interface modules. Standby voltage to maintain memory when system power is off is provided by a battery pack.

CPU (system controller) as well as RAM (for storing data and application variables) and ROM (permanent program) are on a single processor/memory PC board. Circle 195 on Inquiry Card

**Automatic Inspection System Locates
Surface Flaws on Circular Parts**

Model 620 circular laser scanner, for inspection of circular shaped manufactured parts, produces a flying laser spot scan which rotates at a rate of 3000 r/s. Position of the laser spot can be accurately defined through use of an optical encoder allowing for the specific location of a rejectable area to be identified. A He-Ne laser light source can be focused down to 0.001" (0.025 mm) or better to ensure high resolution for tight tolerance inspection.

The collimated laser beam is focused onto the rotating mirror face and then directed onto the part. By reflection or shadowing of the impinged light energy, surface characteristic or dimensional analysis of a part can be made. An internal clock count established over the entire 360 deg of laser sweep allows the system to provide inspection tolerances of $\pm 0.0005"$ (± 0.0127 mm) on most applications. The scanner is made by Automation Systems, Inc, 5 Del Mar Dr, Brookfield, CT 06804. Microprocessor based programmable logic functions are set by thumbwheel registers on the comparator cabinet to identify and reject various conditions of surface flaws.

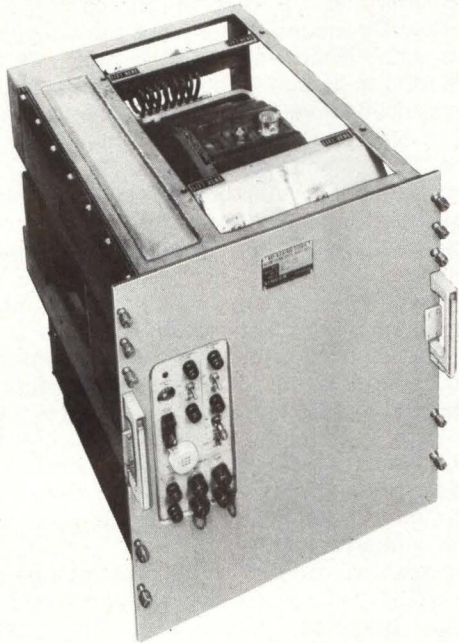
Circle 196 on Inquiry Card

**Microcomputers Monitor
Temperatures and Fuel Flow**

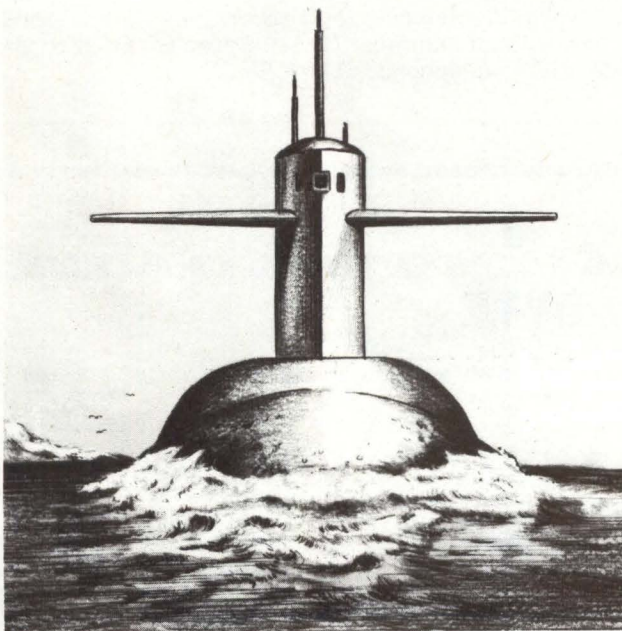
AMS series microcomputers are designed by Avicon Development Corp, 701 N Central Expy, Richardson, TX 75080 for both marine and industrial applications. The 101 temperature monitor can review functions of three zones, while the 201 monitor is used for fuel management. Each is finished with polyurethane enamel and housed in a watertight cabinet with sealed front panel. Several mounting options are available. □

Circle 197 on Inquiry Card

Librascope's RD-433 Militarized Disc Memory Can Go Anywhere The U.S. Navy Goes.



THE dependable memory subsystem for shipboard and submarine installations to interface the Navy's standard computers. This specially configured model for the Shipboard Tactical Intelligence (TACINTEL) program is listed in the Navy's inventory under the military designation RD-433 (XG-1)/SSH. TACINTEL is one of the newest systems in the Fleet Satellite Communications (FLTSATCOM).



Based on Librascope's production CL107MB memory system, the RD-433 is designed to fit in a standard 19" Retma open rack, meet MIL-E-16400, Class 4, operational requirements in free air ambient 0°C to 50°C, and withstand the MIL-S-901C drop hammer test. The system is also humidity and drip proof, and EMI/RFI secure as shown in the photograph.

Modularly designed for easy on-call maintenance, no preventative maintenance is required. The controller is made up of the low-cost SEMS (the Standard Electronic Modules developed by NAFI). Low power Schottky integrated circuits are used throughout the SEMS.

A different configuration employing Librascope's Model CL107MA, which also interfaces with the AN/UYK-20, is used in the Integrated Radio Room (IR²) of TRIDENT submarines. Librascope's mass memory subsystems are on board in many other U.S. Navy programs. For example, they are prominently successful on the BQR-24 program.

Call or write today for additional information on these rugged, reliable Militarized Mass Memory Systems.

The Singer Company, Librascope Division, Department N, 833 Sonora Avenue, Glendale, California 91201. Telephone (213) 244-6541, extension 1891.

Librascope

a division of The SINGER Company

INTERFACE Data Communications INTERFACE '79

April 9-12, 1979 • McCormick Place • Chicago, Illinois



McCormick Place, Chicago, Illinois

New directions in data communications and distributed data processing (DDP) will be the focus of the 70 conference sessions of Interface '79. The seventh annual data communications conference and exposition to be held at McCormick Place in Chicago will cover a variety of topics including terminal trends, software, networks, and digital communications technology. Participating in the exposition will be more than 225 companies exhibiting data communications and distributed processing hardware, software, and services.

The session map is provided on pages 108-109. Colored blocks denote sessions chosen for their interest to *Computer Design* readers. Gray blocks show sessions which, depending on participant's time constraints, may be of secondary interest.

Three Interface '79 session groups focus on networks. New Directions in Network Services (NDN 1-4) explores established value added networks and prospective ACS, XBS, and XTN extended network services. Problems of effective network implementation are discussed in Net Workshops (NET 1-4) sessions. Tech/Network Control and Performance (TCT 1-4) sessions detailing network planning, performance parameters, test equipment, and monitoring provide information on tools and methods to keep networks up and performing efficiently.

Two sessions in particular highlight the direction of data communications and distributed data processing for the 80s. Current and future applications of microprocessors, fiber optics, and satellites in data communications and distributed data processing will be postulated in the Technology Update (TEC 1-4) sessions. The Promise of All-Digital Communications (DIG 1-3) addresses potential benefits and problems inherent with all-digital systems, including one session on digitizing the human voice.

Other session groups of interest include Terminal Trends (TER 1-4) discussing "smart" and "dumb" terminals, graphics, teleprinters, and transaction-oriented systems; Productivity at the Interface (PRD 1-3) which instructs users on ways to enhance data-communications performance using ICs, modems, multiplexers, and terminal interface processors; and a Hard Look at Software (SOF 1-5) which investigates network operating systems, communications monitors, and database management systems.

Registration for the full four days is \$95; single-day registration is \$60. The pre-conference group rate of \$60 (full conference) or \$30 (single day) applies to the third and each additional attendee from the same company location, provided they register at the same time. For conference registration and hotel reservations, contact Interface '79, 160 Speen St, Framingham, MA 01701, telephone (617) 879-4502.

PUSHPA

8/32

INTERDATA®

ONE MEGABYTE

8/32C Processor with 128 KB PM9800 PUSHPA memory 896 KB PM9700 PUSHPA memory chassis Installation & Check-Out Two Years of Warranty Maintenance	\$51,900 44,800 1,000 N/C N/C	8/32D Processor with 1 MB Two Years of Maintenance on 896 KB	\$139,100 20,928 <hr style="width: 50%; margin: 0 auto;"/> \$160,028
---	---	---	--

SAVINGS

per system
in two years

\$62,328

per system
in two years

\$160,028

* Registered Trademark
 of Perkin-Elmer Corp.

PUSHPA memories

15261 Transistor Lane
 Huntington Beach, CA 92649, U.S.A.
 a division of

PUSHPA

INTERNATIONAL
 CORPORATION

PUSHPA

designs & manufactures only the most advanced core memory cards in the industry

Single or dual track, MFE is the driving force in cassette transports.

We revolutionized the digital cassette industry by making the first simple, reliable tape drive.

Now we offer that reliability in a full line of transports, both single and dual track.

The Single-Track 250B. With just two moving parts (no mechanical adjustment, ever) the 250B offers a record of performance no competitor can match: an MTBF of 15,000 hours. The 250B also has the widest ANSI/ECMA-compatible read/write speed range on the market (5-40 ips) and data transfer rates up to 32K bps.

The Dual-Track 450B. This new model gives you up to 720,000 formatted character storage, and features the exclusive TACHLOK™ servo speed control — for constant tape speed. Like the 250B, the 450B has data transfer rates up to 32K bps and needs no mechanical adjustment. Both models are available with a variety of interface options.

The Single-Track 250BH — for hostile environments. This incredibly rugged version of the 250B can handle just about any condition. Operating temperatures from -40°C to $+70^{\circ}\text{C}$, for example. And all kinds of shock and vibration. The 250BH has been field proven in some of the toughest applications you can name. Indoors and out. In a wide range of industries.

All three models are available in volume, ready to ship. And we can customize to meet your exact design requirements.

For details, contact MFE Corporation, Keewaydin Drive, Salem, NH 03079. Tel: 603-893-1921. TWX 710-366-1887/TELEX 94-7477. In Europe: MFE Products Sa, Vevey, Switzerland. Tel. 021 52, 80, 40/

TELEX 26238. (MFE has complete worldwide representation. Contact us for the rep nearest you.)

© MFE Corporation

**CIRCLE 54 ON INQUIRY CARD
Dual-track 450B**

MFE

Single-track 250B

**Single-track 250BH
Hostile
Environment**



HP's OEM-compatible the start of s

However big the system you're planning, make sure you start with a computer and disc combination from Hewlett-Packard. HP 1000 processors and disc memories were designed to work together. So whatever combination you choose, you're assured of complete compatibility. Then you can add off-the-shelf peripherals and instruments, as well as the equipment you build yourself, to

create extremely reliable, cost-effective OEM systems.

This compatibility extends to our RTE family of real time operating systems, data base management and networking software, too.

By offering computers in a range of speeds and main memory sizes, and discs from 5 to 50MB, we make it easy for you to find the performance you need at the price you can afford. And you have a choice of packaging in standard or low-profile racks, or as separate modules.

Three ways to mix and match

You can put together all kinds of disc and computer combinations. These three examples cover a range of prices and performance.

1. Our HP 1000 F-Series computer and 7920 top-loading disc give you a lot of speed and power for \$24,310. The computer has 128K bytes of 350 ns memory (expandable to 2MB), a Scientific Instruction Set, 14 I/O channels (expandable to 46), hardware floating point, and fast Fortran processor. The 50MB disc has a 25 ms seek time and a transfer rate of 937.5K bytes per second. You can also add storage to 400MB.

2. At \$17,428, our HP 1000 E-Series computer and 7906 disc is a great combination. The 64K byte memory (expandable to 2MB) has a 595 ns cycle time (350 ns optional). It has nine I/O channels, expandable to 46. The 7906 disc has half of its 20MB storage on removable cartridges and the other half on fixed platter. Seek time is 25 ms and the transfer rate is 937.5K bytes per second.

3. For economy, you can pair our HP 1000 M-Series computer with this same 7906 disc. You get the same ability to expand the 650 ns memory from 64K to 2MB, and similar I/O options. And the price starts at just \$16,187.

Quantity 50—U. S. domestic OEM prices with cabinetry as shown.



e computers and discs: omething big.

Another reassuring point: buying from one supplier means good service and support. Especially when that supplier is Hewlett-Packard.

We've been solving problems in the lab and factory for the past forty years, making thousands of instruments, computers and peripherals in that time. So we know exactly what an OEM needs

to make them all work smoothly together.

That's why so many successful OEMs start their systems with one of ours. So check out the full range of HP performance at your nearest HP sales office. You'll find it listed in the White Pages. Or write for complete information to Hewlett-Packard, Attn: Bob Puette, Dept. 1249, 11000 Wolfe Road, Cupertino CA 95014.

CIRCLE 55 ON INQUIRY CARD



HEWLETT  PACKARD

I'd like to know more about HP 1000 computers and discs for use in systems for my company for re-sale to others.

My application is (system function) _____

For (type of company/industry) _____

Name _____

Title _____

Company _____

Address _____

City/State/Zip _____

Phone _____

22806HPDS18

INTERFACE '79 Program Schedule

8:00 9:00 10:00 11:00 12:00 1:00

Monday		POL-1 Issues in Regulation and Competition: How They Affect Users	
		SCH-1 Fundamentals of Data Communications	

Tuesday		SCH-3 Basic Terminals and Terminal Systems		POL-3 Government Information Policy: Changing Needs and the Need for Changes	
		SCH-1 Fundamentals of Data Communications (R)		MGT-2 Datacomm Economics for Executives: Controlling Datacomm Costs	
		TER-2 Graphics: Displays and Plotters		PRD-2 Modems and Multiplexers: An Update	
		NDN-1 Extended Network Services: Background, Overview and Impact		INT-2 International Carrier Policies and Regulations	
		PRD-1 How New ICs Redefine Interface Functions		APP-1 DDP in Financial Services	
		NET-1 Achieving Network Transparency			

Wednesday		NDN-2 Prospective ENS Offerings: ACS, SBS and XTN		SCH-3 Basic Terminals and Terminal Systems (R)	
		TER-3 Teleprinter Technology in Transition		DIG-2 Digital Switching Systems	
		NET-2 Design Optimization		TCT-2 Measuring and Optimizing Response Time, Throughput and Reliability	
		OFF-2 Electronic Mail: Current and Future Implementations		WPD-3 Integrating Word and Data Processing Functions	
		TEC-2 Fiber Optics: Current and Future Applications			
		MGT-3 Evaluating User Pay-Back Schemes			
		SEC-3 The Constant Line: Equip. for Uninterruptable Power and Transient Suppression			

Thursday		NET-4 Vendor-Designed Network Architectures		NDN-3 Established Value-Added Network Services: New Challenges and Opportunities for the Packet Pioneers	
		TER-4 Trends in Transaction-Oriented Data Entry		APP-4 DDP in Government	
		MGT-5 Datacomm Organization: Who Manages What?		WPD-4 Shared-Logic Versus Stand-Alone Word Processing	
		SRV-3 Network Management Services: New Ways of Spelling Relief		SOF-4 Software for Evaluating and Diagnosing Performance	
		TCT-3 Real-Time Tech Control and Network Monitoring		APP-3 DDP in Retailing, Distribution and Transportation	
		DDP-4 To DDP or Not to DDP			

1:00 2:00 3:00 4:00 5:00 6:00

	POL-2 The Data Communications Market: Analysis, Projections, Scenarios		SCH-2 Understanding Communications Processors and Software	Monday
	DDP-1 DDP: Concepts and Approaches		TCT-1 Planning for Network Performance	
	SRV-1 Shared Services: Specialized Needs		INT-1 Design and Management of International User Networks	
	TER-1 More Intelligence in Terminals		SEC-1 Controlling File Access and Physical Security	
	MGT-1 Uncovering High-Payoff Datacomm Applications			
	SOF-1 Network Operating Systems			
	WPD-1 The Communicating Word Processor			

	DIG-1 All-Digital Communications: Background and Overview		SOF-2 Communications Monitors	Tuesday
	TEC-1 Micro Insights for Datacomm Planners		SCH-2 Understanding Communications Processors and Software (R)	
	SRV-2 Common Carrier Services: More Alternatives		DDP-2 DDP: Current Progress and Future Promise	
	SCH-4 Introduction to Networking and DDP		SEC-2 Seminar on High Reliability and Redundant (Backup) Systems	
	WPD-2 Text-Processing Networks			
	OFF-1 Message Communications: The Forms and Flow of Information			
	INT-3 Future Developments in International Telecommunications			

	SOF-3 Data Base Management Systems: A Datacomm Perspective		SCH-4 Introduction to Networking and DDP (R)	Wednesday
	PRD-3 Front Ends and Remote Communications Processors		DIG-3 Digitized Voice: Problems and Prospects	
	OFF-3 Telecommunications Tools for the Office		OFF-4 Facsimile Systems and Services	
	TEC-3 Satellites Come Down to Earth		MGT-4 Hiring, Training and Motivating Datacomm Personnel	
			DDP-3 DDP: Management Objectives and Considerations	
			NET-3 Network Simulation	
			APP-2 DDP in Manufacturing	

	NDN-4 Extended Network Services: Regulatory and Competitive Issues			Thursday
	TCT-4 Test and Diagnostic Equipment			
	SOF-5 Software Schemes to Optimize Data Flow			
	TEC-4 The Next Ten Years in Data Communications			
	MGT-6 Contract Considerations in a Multi-Vendor Environment			
	SEC-4 Getting Back Up: Audit Trails and the Recovery Process			

Electro79

Electronic Show and Convention / April 24-26
New York Coliseum / Americana Hotel

Electronics in the opening years of the 1980s will be the focus of the 3-day conference. Staged at the New York Coliseum and Americana Hotel,* respectively, exhibits and presentations on state-of-the-art and career topics are among Electro/79's attractions.

More professional program sessions are devoted to the microprocessor than any other topic—an indication of the microprocessor's impact on the industry. Other subjects to be covered are communications satellites, memories, fiber optics, energy management, LSI, and computer imaging. Sessions will be held at 10 am and 2 pm on Tuesday through Thursday.

The Electro special theme exhibit—Microprocessor Application Awards—featuring winners and finalists of a microprocessor applications contest will be displayed on the third floor of the Coliseum. Applications ranging from automotive use and production control to office equipment and energy conservation will be judged on the basis of effectiveness, popularity, state-of-the-art, originality, inventiveness, and cleverness. The special theme exhibit plus exhibits on the first two floors of the Coliseum will open each day at 9:30 am and close at 6:00 pm Tuesday, 7:00 pm Wednesday, and 5:00 pm Thursday.

The conference keynote address, delivered by Charles L. Brown, chairman of the board and chief executive officer of American Telephone and Telegraph, will be among the formalities of the preview luncheon. Also on the agenda is presentation of the Alan Ploss Award. The luncheon is included in the all-day Electro Marketing Conference, Monday April 23.

An International Visitors Center at the Coliseum will provide interpreter services, free registration, and a hospitality suite for foreign registrants. A reception scheduled for Wednesday will honor international exhibitors, attendees, commercial attaches, and counsels from foreign governments. Sales, marketing, purchasing, and technical electronic specialists will be available to answer questions for foreign companies entering the U.S. market, and for American firms expanding overseas.

The Electro Film Theater will again offer a selected series of scientific and engineering motion pictures produced by electronics companies. Screened from 10 am to 4 pm Tuesday through Thursday, the films cover electronics technology from space to microprocessors.

"Shuttle Into the Eighties" at the all-industry reception Tuesday April 24, 6:30 to 8:30 pm. Held in the Americana Hotel's Imperial Ballroom-turned-space-shuttle, the traditional party will feature aerospace equipment, space games, and a robot. Tickets are \$10 at the door.

The following excerpts from the Professional Program report sessions of interest to *Computer Design* readers. Although some session numbers and times may change, the information presented here reflects the schedule available at press time.

*The Americana Hotel is now known as the Sheraton Centre.

Professional Program Excerpts

Tuesday Morning

Session 1

10 am-12:30 pm

Keys to Successful Engineering Management

Session Organizer/Chairman: P. A. Peirce, USAF/Air Force Systems Command, Hanscom AFB

Prepared for Electro by the IEEE Engineering Management Society, this session focuses on four important topics to the engineer/manager: stress, motivating creativity, cost controls, and management of personnel.

"Stress and its Effect on Managers," M. Buckley, RCA

"Keeping Engineers Creative, Productive," I. Katz, Northeastern University

"Controlling Your Cost," Speaker to be announced

"Managing People Correctly at the First Level of Management," Speaker to be announced

Session 2

10 am-12:30 pm

Analog-to-Digital LSI

Session Organizer/Chairman: R. Walker, Intel Corp

Recently, we have seen the introduction of a new type of semiconductor device—one which combines complex linear and digital functions on the same chip. One-chip microcomputers with on-board analog-to-digital converters, microprocessor-compatible A-Ds, and codecs are representative of these new products. This session will cover processes (CMOS, NMOS, IIL, and laser trimming) and circuits (A-D, D-A converters, comparators, and amplifiers). Additionally, the speakers will discuss existing and future applications, economic considerations, accuracy and performance.

"Linear Compatible IIL," M. Timko, Analog Devices

"CMOS and Laser Trimming Provide Low Cost and High Performance," B. O'Neil, Intersil

"A-D LSI Optimized for Interface," P. Marcoux, Signetics

"N-Channel A-D LSI Offers Highest Density and Lowest Cost," E. K. Cheng, Intel

Session 3

10 am-12:30 pm

Marketing Personal Computers

Session Organizer/Chairman: F. Burge, Regis McKenna Inc

Last year's "hobby computers" are "personal computers" today, and "home computers" are already being sold. Identifying the potential market, designing the product to fit the need, and merchandising high-technology machines in retail stores represent the new challenges in personal computing. Financial, manufacturing, and retail experts offer their insights into a potential billion-dollar marketing puzzle.

"The Personal Computer Market," B. Rosen, Morgan-Stanley

"The Radio Shack Experience," L. Kornfeld, Radio Shack

"The Apple Experience," G. Carter, Apple Computer

"The Computerland Experience," E. Green, Computerland

Session 4

10 am-12:30 pm

Software Manufacturing in the Distributed Environment—Theory and Practice

Session Organizer/Chairman: J. Sternberg, Conversational Systems Corp

Reasons why "methods of software generation will have to change from 'customized' or 'packaged' approaches to manufactured items," and methods of manufacturing software will be discussed.

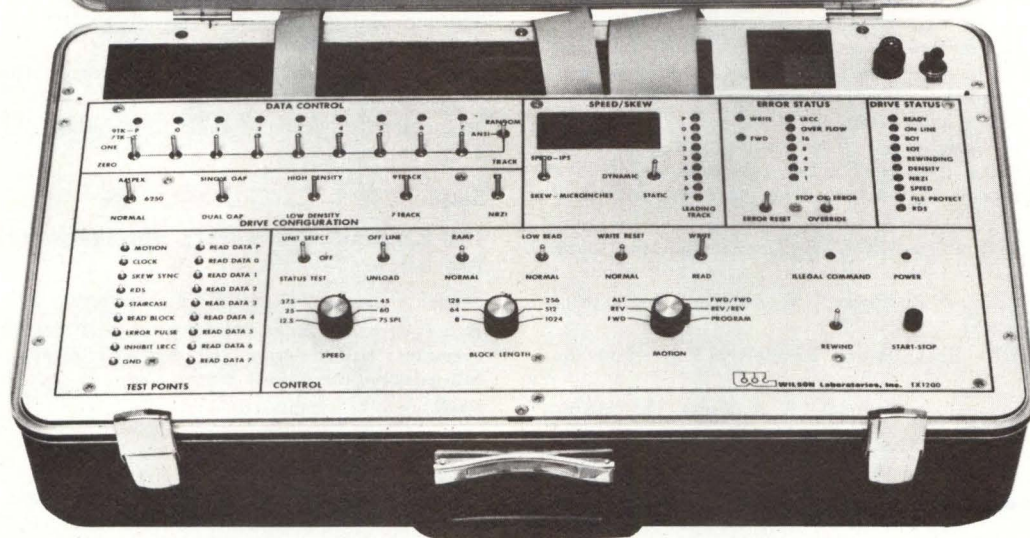
"Distributed Processing—Fact, Fallacy, and Future," J. Sternberg, Conversational Systems

"The Business Reasons for Decentralization," A. W. Kirsch, City Bank, New York City

"The Product Requirements of the Decentralized Environment," R. Moore, IBM Corp

WILSON EXERCISERS

THE ERRORS STOP HERE



**TX-1200
Tape Drive
Exerciser**

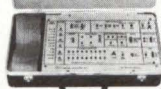
IDEAL FOR BOTH Q.A. AND SERVICE TESTING

FX-500



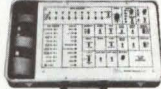
**Floppy Disk
Exerciser**

DX-500



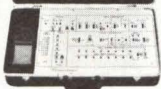
**Disk Drive
Exerciser**

TX-500



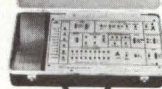
**Tape Drive
Exerciser**

CX-500



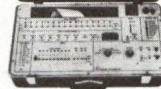
**Communications
Exerciser**

SX-500



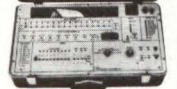
**Storage Module
Exerciser**

DX-1000



**Disk Drive
Exerciser**

DX-2314



**Disk Drive
Exerciser**

To completely test tape drives, disk drives, floppy disk drives and other equipment, you can't beat Wilson exercisers.

These universal Quality Assurance/Service testers are made to check out every operating function that can go wrong.

Wilson exercisers put each unit through its paces — continuously if necessary — to locate even intermittent errors.

Manufacturers, OEM's and Service Engineers rely on these heavy-duty exercisers to catch problems before they can go into a system — or to locate malfunctions that have occurred.

Each standard Wilson exerciser is fully engineered for the equipment it supports, and every exerciser is portable, rugged, reasonably priced and ready to go when you get it. Special needs? We also make custom testers.

Write or Call For Complete Information.

2237 N. Batavia Street
Orange, California 92665
Telephone (714) 998-1980
Telex 181 598



**WILSON
Laboratories, Inc.**

"Software Manufacturing—The Future Method of Software Generation," J. A. Goldfarb, Conversational Systems

Tuesday Afternoon

Special Session

1 pm

Electro International Leadership Panel

Major electronics executives from the United States, China, Germany, Holland, and Japan will participate in a panel session covering state-of-the-art electronic devices and systems development in their respective countries and regions

Session 7

2-4:30 pm

The Engineer and Public Policy: Servant, Guardian, or Gadfly?

Session Organizer: J. Casey, EAB/USAB Career Development Committee, IEEE

Session Chairman: J. F. Fairman, IEEE Member Conduct Committee

Most engineers are employees, and their professional responsibilities lie primarily in the realm of designing products or performing particular services. How can engineers, therefore, safeguard the health, safety, and welfare of the public? How can they influence policy in these areas? This session will attempt to clarify the interrelated requirements and principles underlying the dynamic components that influence the engineering environment.

"The Engineer—the Problem-Solver," S. Florman, Kreisler, Borg, and Florman

"The Right of Technical Challenge," V. Edgerton, Intelligence Technology Resources

"Informed Consent?" R. J. Baum, Rensselaer Polytechnic Institute

"Public Policy—Rational or Irrational," E. A. Weiss, The Sun Co

Session 8

2-4:30 pm

Advances in Digital Signal Processing: Hardware and Techniques

Session Organizer/Chairman: W. Koral, TRW LSI Products

In the course of the past three years a significant migration has begun from the classical analog techniques of signal processing to their digital counterparts. While the advantages of working in the digital domain have been well-known for many years, the scope of applications has been limited until very recently when LSI capability made the concepts physically and economically viable. This movement represents a revolution in many fields, especially telecommunications, radar, sonar, voice and video processing, and medicine.

"Dedicated Microcomputers Expand Digital Signal Processing Horizons," R. W. Blasco and H. Davis, American Microsystems

"Implementation of FIR Filters with RAMs," M. J. Narasimha, Granger Associates

"Monolithic Multiplier Supports Cost-Effective Speech Compression," S. Waser, Monolithic Memories

"Bit-Slice Microprocessor Applications for 4 kHz Channels," W. L. Betts, Paradyne

"Architecture Development for a Universal Digital Filter," R. Karwoski, TRW LSI Products

"Hardware Realization of Digital Processing," Z. Ali, Commercial Telecommunications

Session 9

2-4:30 pm

The Personal Computer: Hobby-Horse or Work-Horse?

Session Organizer/Chairman: F. Burge, Regis McKenna Inc

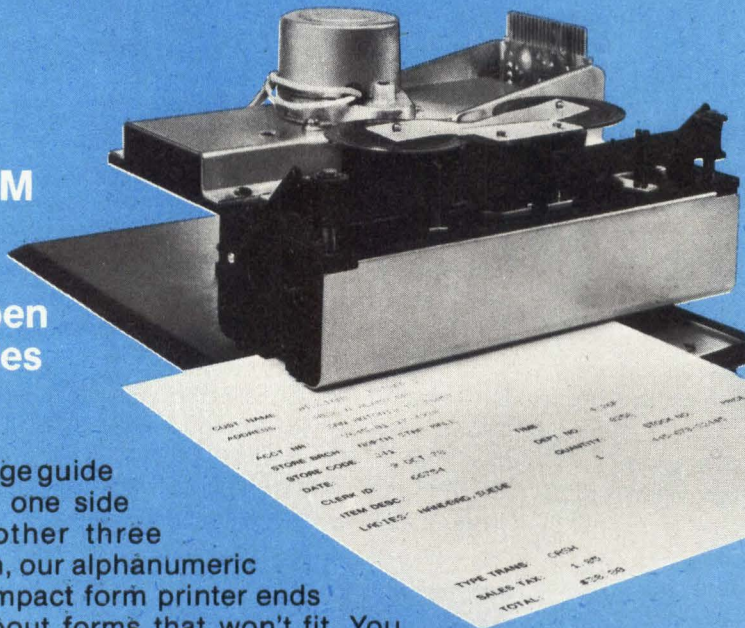
Is the personal computer a toy or a tool? Six owners of personal computers will describe and demonstrate what they are doing with personal computers.

Speakers to be announced

Feed all your forms to our wide-open printer

The OEM
impact
printer
wide open
on 3 sides

With an edge guide sensor on one side and the other three sides open, our alphanumeric DMTP-8 impact form printer ends worries about forms that won't fit. You can easily insert from bank checks to out-size pages, single sets to multipart reports... any forms where you need to print up to 50 characters per 4" line.



Consider the advantages! Programmable character pitch, heavy-duty construction and an extra long-life dot matrix printing head means real durability. Its exceptionally long needle stroke turns out crisp multiple-copy printings on thicknesses from .003" to .015" — without adjustment.

Its easily replaceable ink rollers and self-reversing ribbon gives you a 10 million character life.

ALL THAT,
YET STILL
ECONOMICAL—
ONLY \$269 IN 100's.



PRACTICAL
AUTOMATION, INC.

Trap Falls Road
Shelton, Conn. 06484
Tel: (203) 929-5381

CIRCLE 57 ON INQUIRY CARD



BUY PDP® FROM THE PDP® PEOPLE.

BUY MEMORY FROM THE MEMORY PEOPLE.

Apples and oranges. You wouldn't think of going to a memory house for minicomputers. So why go to computer houses for memory... at computer house prices?

Bank on experience. Digital Equipment Corporation, the maker of the PDP®11 Series, is an experienced minicomputer manufacturer. Intersil, with more than 2 billion bytes of memory systems delivered in the last 7 years, is an experienced add-on and add-in memory manufacturer. Put them together, you have the ideal combination. PDP®11 at DEC®'s price. Memory at Intersil's price.

We know what works. There's no such thing as a universal board. But, at Intersil, we know all the models in the PDP®11 Series. We can tell you what memory works with what. And why. That means you get off-the-shelf memory that fits your application. Available now.

Totally compatible. Intersil's IMC-11 memory cards are totally compatible with all PDP®11/04, 34 minis. Including standard software and hardware, memory management, parity control, core or semiconductor memory and standard or modified Unibus. **Name the configuration.** Whatever you need. Each card contains DIP switches which allow you to select the card starting address in 4K

increments up to 128K bytes. And, I/O page capacity is switch selectable to 1K, 2K or 4K words. **Warranted.** Intersil memory cards give you reliability...based on over 2 billion bytes delivered... not a bad record for the last 7 years. Experience. Experience you can depend on. And, each card is burned-in under worst case conditions before it leaves Intersil. That's why every card carries

full one-year warranty. Our warranty. **Experience tells.** Over the years, people have bought more minis from DEC® than from any other source. Over the last 7 years, people have bought more semiconductor computer add-on main memory systems from Intersil than from any other independent source. That's reason enough to talk to DEC® about minis... and Intersil about memories. **Apples. Oranges.**

®DEC and PDP are registered trademarks of the Digital Equipment Corporation.

INTERSIL

Microsystems
10710 No. Tantau Avenue,
Cupertino, CA 95014
Tel: (408) 743-4442 TWX: 910-339-9369



I'm interested, Apples and oranges? You're right. Tell me about Intersil's add-in memory for the DEC® PDP®-11/04, 34 Series minicomputer.
____ Please send me your Alexandre Dumas poster.

Name _____

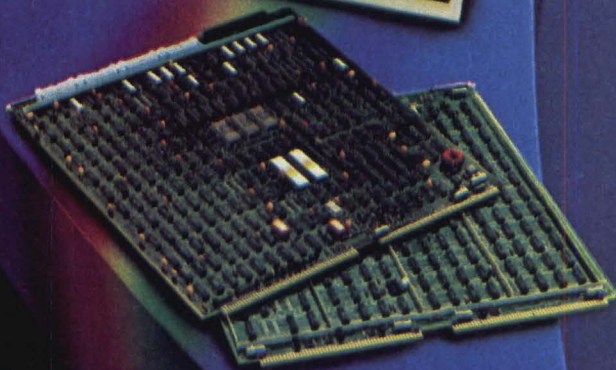
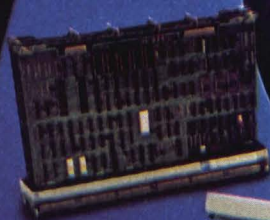
Company _____

Address _____

City _____ State _____ Zip _____

Country _____

Boose



The company whose glass jars became a legend is now making history in computer products.



Ball...where quality has been a tradition for 99 years.

In 1880, the Ball Mason Jar offered a simple solution to an age-old problem. Known for their consistent quality, these jars revolutionized an industry.

In 1979, after seven years of research and development, the Ball name is again making history with OEM computer peripheral products and the ReaDoc System for automatic processing of payments.

Ball Disk Drives

Products you'll be proud to label your own.

Ball Computer Products people understand the needs of the OEM. When you buy a disk drive, it must be fully operational when delivered. After that drive ships to your customer, it must exhibit high field reliability. And, if the drive does fail, it must be readily repairable. The BD-50 and BD-80 Disk Drives satisfy those needs . . .

- Because we insist on perfection through every step in the manufacturing process. (We ensure it through long, elevated temperature burn-in before shipment.)
- Because all BD-Series Drives employ modular construction and diagnostic features that simplify service.
- Because all BD-Series Drives are supported by the most complete field maintenance documentation in the industry.

Ball's total approach to product quality—That's what you'll like most about BD-Series Disk Drives.

Ball Disk and Tape Controllers

Powerful, yet easy to use.

Ball controllers for Nova and PDP-11 series computers are easy to incorporate into your system. Our **tape controllers** emulate similar products from the computer manufacturer. No software impact! And they are host-resident for lowest cost.

Our **disk controllers** include emulating controllers, which require no software modification, and non-emulating controllers, which come with complete software modification packages. Microprocessor-based, the Ball controllers incorporate all the latest features. Some even offer IBM format capability. All our controllers operate with any SMD interface drive—the Ball BD-50 and BD-80, or any other—even intermixed on the same controller.

Ball Disk and Tape Subsystems

Complete systems from a single source.

Ball Computer Products specializes in fully integrated disk and tape subsystems. Single source responsibility eases the headache of integrating components from several vendors. You decrease inventories and significantly improve factory throughput. Your shipments aren't held up for lack of a minor system component. And you have the comfort of knowing that before the system ever left Ball, it was tested on a system identical to yours.

Ball ReaDoc

Cash processing system.

The ReaDoc Remittance Processing System broke new ground in data processing for major companies processing mail and agency payments. This complete system, with terminal, memory, central processor and software, has already reduced cash processing expense for many firms and is building an enviable reliability record. While the system concept remains constant, each ReaDoc system is tailored for a specific customer application.

Ball Computer Products Legendary in their own time.

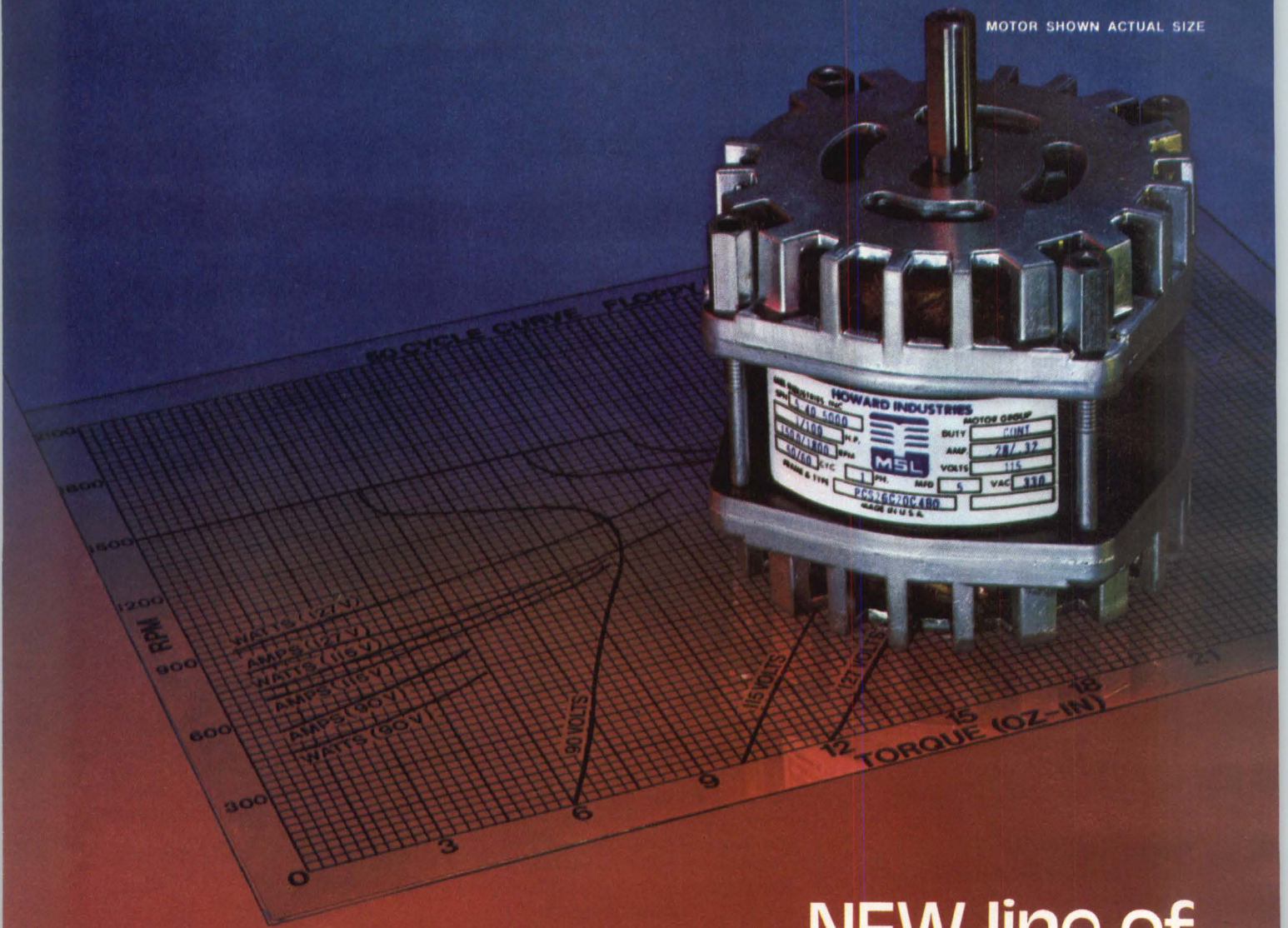
Ball Computer Products Division is a growing part of the Ball Corporation, a company with annual sales of more than half a billion dollars. Ball people personify the company philosophy of quality and performance leadership. Our products solve your problems by providing straightforward and reliable answers to complex requirements. We would like to be part of your company's success story. Call us for complete information.



**Computer
Products
Division**

Division Headquarters
860 East Arques Avenue
Sunnyvale, California 94086
(408) 733-6700

MOTOR SHOWN ACTUAL SIZE



NEW line of "high performance" induction drive motors

Same power in a
smaller package!

Completely
interchangeable!

HOWARD

Howard's new "high performance" line of FHP motors is perfectly suited for all types of business equipment drives. 16.7% shorter than motors of equal power — only 2¾" high.

WIDE RANGE OF DESIGN CONFIGURATIONS

Square wave 24VAC—48VAC, Frequency 50-60 cycles, Voltage 100 V thru 256 V, Speeds synchronous to 3600 RPM, non-synchronous to 3400 RPM, Power 1/100 HP to 1/10 HP.

UL and CSA approvable, available in PC, capacitor start or split phase models.

SEND FOR NEW 26-33 Frame Induction Motor Catalog with full specifications.



HOWARD INDUSTRIES One North Dixie Highway, Milford, Ill. 60953. Phone: (815) 889-4105

Session 10

2-4:30 pm

Database Management Systems on Microcomputers

Session Organizer/Chairman: S. B. Yao, New York University
The emergence of microcomputers has brought low cost dispersed application to data processing. This session reviews the impact of microcomputers on database management systems, research and commercially available database systems, and application of these systems to distributed processing, frontend/backend architectures, and office automation.

"Application of Microcomputers in Data Management," S. B. Yao, New York University

"Distributed Microcomputer Database Systems," D. Chai, Bell Laboratories

"Micro-SEED and Its Application," R. Gerritsen and R. Hackathorn, U of Pennsylvania, The Wharton School

"Microcomputer-Based Business Systems," R. Rustin, Algorithmics Inc

Wednesday Morning

Session 13

10 am-12:30 pm

Engineering and Purchasing: Chaos or Coexistence?

Session Organizer/Chairman: D. Singer, Electronic Buyers News, CMP Publications

The objective of this session is to develop suggestions for improving cooperation between the engineering function and the procurement function to enable firms to bring to market high quality products with the best price/delivery. Representatives from design engineering, manufacturing, and purchasing will participate.

Session 14

10 am-12:30 pm

Use of Logic Analyzer Tools in Development of Processor Systems

Session Organizer/Chairman: S. Lee, Hewlett-Packard Co
The role of logic analyzers in the development of processor systems (from minis to mainframes) will be presented in three case histories plus a projection of how logic analyzers will affect both software and hardware development in the future.

"The Use of CPE in the Design and Control of Computer Systems," S. Sensabugh, Testdata

"The Use of Logic Analyzer Techniques in the Development of the 21MX Series Minicomputers," J. Cates, Hewlett-Packard Data Systems

Session 15

10 am-12:30 pm

Desktop Computers

Session Organizer/Chairman: D. Cole, Hewlett-Packard Co

Demand for low cost, versatile desktop computers for small-business and engineering applications is growing almost faster than the industry can respond. The burgeoning market, the technology, and the wide range of applications are presented in this session.

"Market Overview: Growth and Applications of Desktop Computers," Speaker to be announced

"Desktop Computers in Business," S. Gagliano, Wang Laboratories

"Desktop Computers in Engineering," Speaker to be announced, Hewlett-Packard

Session 16

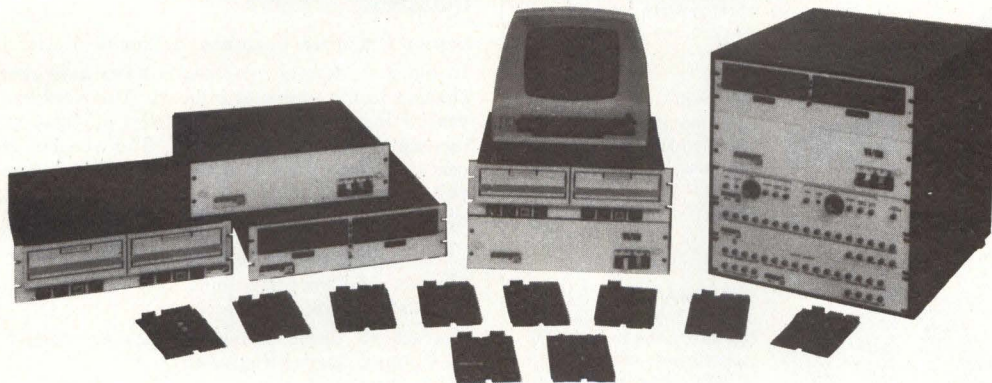
10 am-12:30 pm

Reducing Risks in Microcomputer Development

Session Organizer/Chairman: C. A. Ogdin, Consulting Editor, EDN Magazine

LSI-11™ FROM ANDROMEDA

THE BROADEST LINE OF LSI-11™ PRODUCTS FROM ANY SINGLE SOURCE



From SYSTEMS to SOFTWARE, from CARDS to CABLES, ANDROMEDA offers the broadest range of LSI-11™ components that can be purchased from any single supplier.

In addition to the items we manufacture internally, we also distribute the best products of other LSI-11™ equipment manufacturers including DEC™.

If you need any LSI-11™ product, from a 10mbyte cartridge disk based system to a DLV11 cable, fast and inexpensively, call ANDROMEDA, 213/781-6000. Andromeda Systems, Inc. 14701 Arminta Street #J, Panorama City, California 91402.

**ANDROMEDA
SYSTEMS
INC.**

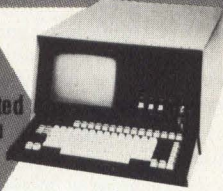
LSI-11 and DEC are trademarks of the Digital Equipment Corp.

CIRCLE 61 ON INQUIRY CARD

117

Comark THE MULTIBUS® MASTERS

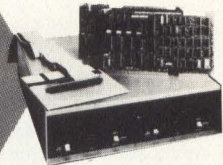
Multibus Integrated Terminal System



9-slot backplane, 9" CRT, 64 x 16 display, line time clock, key lock front panel, full ASCII keyboard, 40 function keys, 30 Amp +5V P/S, choice of CPU, LTC, 4 AC receptacles and documentation.

MB80 \$2580

Floppy Disk Subsystem



Dual floppy disk drives — single or double density, write protect switches, unit select switches, Multibus interface, cabling and documentation.

MF80 \$2850

1/2" Mag Tape Subsystem



Tape drive, formatter, interface card, dual 512 Byte tape buffers, cable and documentation. 7", 8-1/2" or 10-1/2" reel tape drives — 7 tr. NRZI, 9 tr. NRZI or 9 tr. NRZI/PE

MT80 \$4700

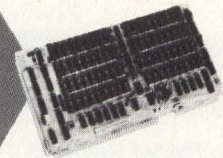
10 MB Cartridge Disk Subsystem



5440 top-load disk drive, 5 MB fixed — 5 MB removable, 512 bytes/sector, 12 sectors, Multibus interface, preformatted pack, 10' cable, slides and documentation.

MD80 \$7995

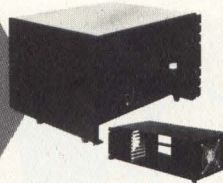
Static RAM Memory



16K or 32K bytes with parity. 20 bit address, 16K boundaries, 8 or 16/8 bit modes. Standard or CMOS. Battery charging — status and power fail circuits.

MR80 \$825

Powered Cage Card Cage



Powered Cage

9 slots, 30 Amp P/S, terminators, optional key lock control panel and documentation.

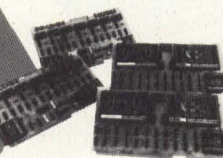
PC80 \$1195

Card Cage

Rack mounted 9 slot card cage, includes bus terminators, spade lugs for power and cooling fan.

CC80 \$350

Analog I/O Systems



High level A/D, 12 bit 0-10V, 8 dif./16 S.E. to 32 dif./64 S.E. Low level 12 bit 10 mV to 10V. Isolated wide range with 12 bit integrating A/D 250V com. mode rej., 4 or 12 chan.

Write or call, C.E. Guenther, for further information.

See us at INTERFACE '79, booth 1053.

* Multibus, registered trademark of Intel Corporation.

Comark Corp., The BusMasters

257 Crescent Street, Waltham, MA 02154 (617) 894-7000
TWX: 710 324 1503

The development of microcomputer applications incurs a surprising amount of risk. Worse, those risks are getting larger, not smaller. The problems being addressed are more difficult; the LSI devices are growing more complex; and the software complexities are rivaling those of larger minicomputer systems. However, there are ways to manage the risks. This session will address what some of the major risks are and offer practical suggestions for minimizing those risks (or, at least, their impact).

"Certainty, Productivity, Profits, and the Role of the Micro," C. A. Ogdin, *EDN Magazine*

"Risk Reduction Through Hardware/Software Tradeoff," W. J. Broderick, Tektronix

"Getting Software Right—The First Time," H. Hills, IBM Corp
Title to be announced, E. Michelman, Intel Corp

Wednesday Afternoon

Session 19

2-4:30 pm

Corporate Venture Capital

Session Organizer/Chairman: K. Rind, Xerox Development Corp
For a variety of reasons, an increasing number of U.S. companies have become active as risk/venture capitalists in new electronics enterprises. This session explores the differing motivations for these investment moves, both from the corporate manager's viewpoint and that of the employed engineer with entrepreneurial ambitions.

"Introduction to Corporate Venture Capital," K. Rind, Xerox Development

"Venturing as a Supplemental Window," G. Miller, Xerox Development

"Venturing as a Diversification/Acquisition Technique," R. Waserman, Gould

"Venturing as an Investment," C. Coulter, American Research & Development

"Venturing into Technology by a Non-Technology Company," Y. Wong, Time

"Venturing Through an Investment Group," G. A. Lodge, InnoVen Capital Corp

"Venturing as a Divestment Technique," P. Castillo, Business Development Services

Session 20

2-4:30 pm

Impact of the 64k Dynamic RAM on the Computer Industry

Session Organizer/Chairman: S. Young, Mostek Corp

In the past, density increases in RAMs have resulted in significant changes in the computer industry. The resultant cost decrease and density increase has broadened the products available as well as increasing the tasks performed. This session will discuss the impact of memory on the evolution of computer architecture as well as the impact the new generation RAM, the 64k, will have.

"The 64k RAM—The RAM of the 80s," S. Young, Mostek

"Testing Implications of the 64k," S. Orr, Univac

"Impact of Large Dynamic RAMs on Microcomputer Systems," W. Sanders, Apple Computer

"Impact of Large Dynamic RAMs on Minicomputer Systems," M. Gutman, Digital Equipment

"Impact of Large Dynamic RAMs on Mainframe Computers," P. Higatshi, NCR

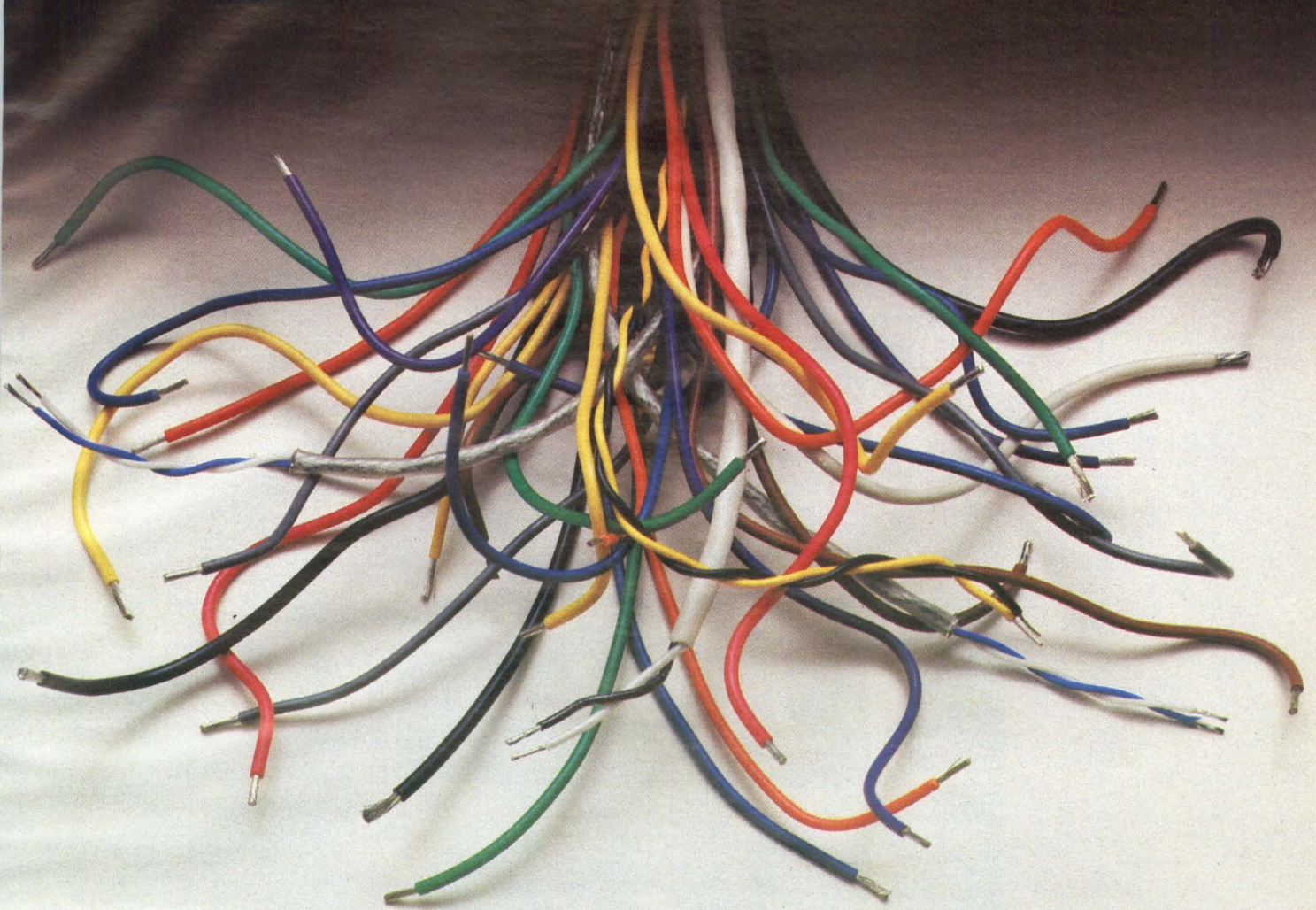
Thursday Morning

Session 25

10 am-12:30 pm

Women on the Steps of the Electronics Pyramid

Session Organizer/Chairman: E. H. Williams, Lockheed Missiles & Space Co



We'll take it from here.

Let's face it, interconnections can really leave you at loose ends.

So we're offering to take total responsibility for solving your mass termination problems.

We're Spectra-Strip, and what we make is exactly what you need to get your job done right, reliably and within reason.

For all your interconnect needs from jumpers and flat cables to IDC connectors and ready-to-go standard and custom planar assemblies, just check us

out. You won't need to call anyone else.

For the name and number of our nearest distributor or rep, write Spectra-Strip, an Eltra Company, 7100 Lampson Avenue, Garden Grove, CA 92642. Or call (714) 892-3361 today.



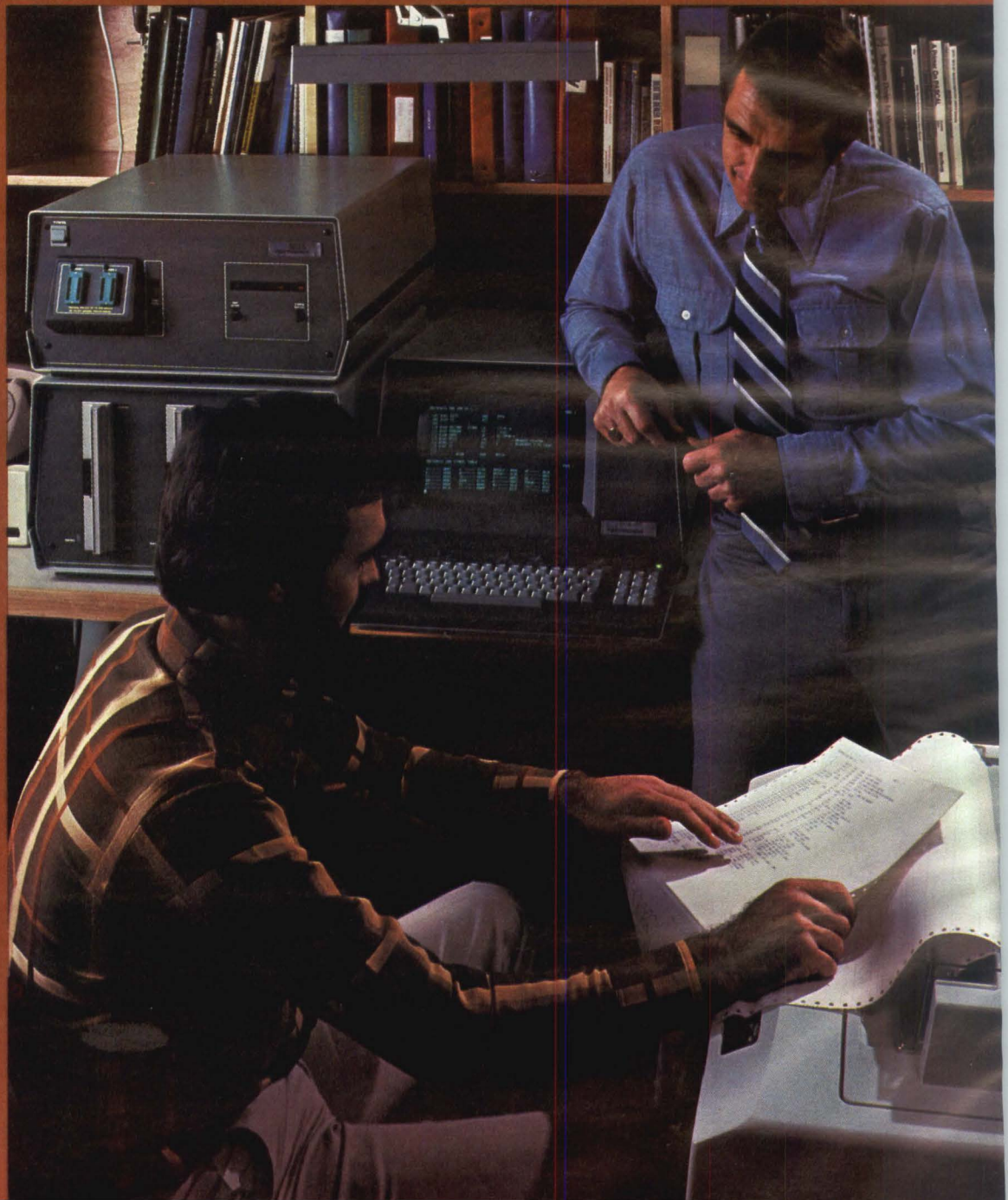
When you're down to the wire

CIRCLE 63 ON INQUIRY CARD

Now supports F8, 3870, 3872.

Our system
emulates the 8080 and
the 8085. The Z80.
The 6800. The TMS 9900.

And that's just
for openers.



Because who has time to learn a new system when a better chip comes along?

Both the Tektronix 8001 and 8002 microprocessor development labs now fully emulate the 3870, 3872 and F8. You can select the chip that best fits the job without repurchasing or relearning equipment.

JOB AFTER JOB, OUR SYSTEM STAYS WITH YOU.

We know time spent learning equipment is best spent on equipment that's going to stay around.

That's why we engineered the first development lab for designers like us who work with major microprocessors.

Now you needn't depend upon one chip vendor. Or buy and learn an entirely new system when you change chips.

THE BEST IDEAS

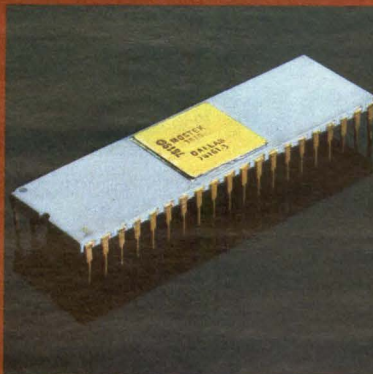
Our features are the kind of ideas you'd probably engineer for yourself... the kind of system you get from a chip user, not a chip vendor.

DISC BASED SYSTEM

Includes text editor, macro relocatable assembler, debugging software and file management utilities, to help simplify software preparation and debugging.

REAL TIME PROTOTYPE ANALYZER

This invaluable option lets you easily track down timing or program



logic problems by dynamically monitoring the microprocessor bus.

ENHANCED BASIC

This specially enhanced, compiler version of BASIC is compatible with the 8080 and 8085, and includes a subset of Z80 instructions. Extensions include comprehensive interrupt handling and optimization features to produce compact code.

PARALLEL DEVELOPMENT INTEGRATED TESTING

Hardware and software engineers can test, trace, and debug independently up to the point of integration. Then they can work together, productively.

If you're concerned about how you spend your time, take a close look at a design lab you can use time and again... even when a better chip comes along.

Contact your local Tektronix Sales Office, or write or call Tektronix, Inc., P.O. Box 500, Beaverton, OR, (503) 644-0161. In Europe, Tektronix, Ltd., P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

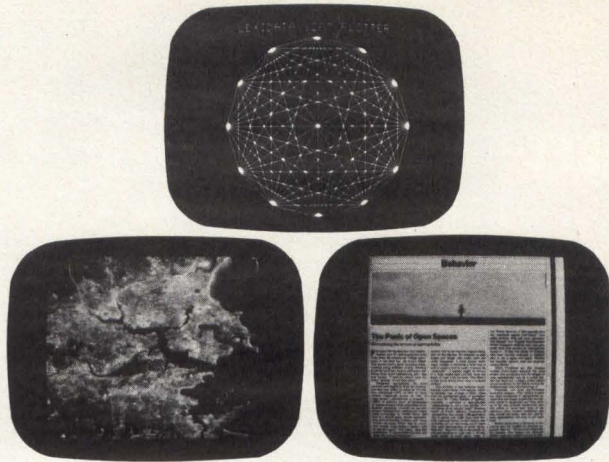
Tektronix
COMMITTED TO EXCELLENCE

For 3870 information circle 64,
For literature circle 65,
For a demonstration circle 66.

FOR FAST REPLY, CALL TOLL
FREE (800) 547-1512.
In Oregon, collect 694-9051.

Tektronix
microprocessor
development labs.

Designed by
people on your side
of the bench.



Raster scan high resolution refresh graphics

at a price you can't ignore

Now you can have a system
to meet your unique computer-graphics applications

System-sophistication made practical for the OEM and end-user

- Full refresh, flicker-free, raster scan display
 - up to 1280 x 1024 pixels in 16-levels of grayscale
 - display 1024 simultaneous colors from color look-up table
 - up to 16 bits of intensity or overlay data per pixel
- Interfaces for most minicomputers
- Gamma-corrected and composite video output
- High-speed, variable image processing
 - pixel update as fast as 45 nsec per pixel
 - random and sequential update
 - dynamic memory allocation
 - writeable control store
- User can program the alphanumeric generator and define the cursor
- Nondestructive functions to highlight image displayed
 - vector and alphanumeric overlays on image
 - zoom with continuous 4-directional scrolling
- Command I/O and DMA to host computer
- Peripheral options

A versatile graphics-system to meet your widely diverse needs that you'll want to know more about. Just write Lexidata Corporation, 215 Middlesex Turnpike, Burlington, MA 01803 or faster yet, call us at 617 273-2700, and ask for Martin Duhms.



Best in graphics, year after year

215 Middlesex Turnpike, Burlington, MA 01803
617 273-2700 • TWX 710-332-1381

Women in electronics have come a long way—or have they? Three accomplished professionals in electronics engineering, technical marketing, and product management will address the many problems and not-so-many opportunities in reaching higher levels on the pyramid. The session is planned for audience participation; short papers will be followed by a panel session.

"Outside Sales—An Upward Step on the Pyramid," T. Young, Electronic Products Div, 3M Co

"Women in Management—An Expansion of a Binary Issue," C. J. Morris, Hewlett-Packard Co

"Women in Electronic Professional Levels: The Engineer, The Business Trained, The Management Potential," E. H. Williams, Lockheed Missiles & Space Co

Session 26

10 am-12:30 pm

Nonvolatile Storage for Very Small Processors

Session Organizer/Chairman: E. W. Pugh, IBM Corp, T. J. Watson Research Lab

Covering EPROM, MNOS, battery backup of volatile semiconductors, bubbles, minicassettes, and minifloppies session deals with the problem of providing nonvolatile storage for low system cost micro- or small miniprocessors.

"Nonvolatile Semiconductor Storage," D. G. Craycraft, NCR Corp

"Bubbles vs Battery Powered Semiconductors," J. E. Juliussen, Texas Instruments

"Floppy Discs," G. H. Sollman

"Digital Cassettes," B. Minildi, Information Terminals, Verbatim

Wednesday Afternoon

Session 27

10 am-12:30 pm

Microcomputer Industrial Control Networks

Session Organizer/Chairman: J. E. Winegardner, Western Electric Problems systems architects face when designing an industrial control network now that microcomputer products are becoming relatively inexpensive to incorporate into a network will be brought to the forefront in this session. It is important that management-level executives be made cognizant of the wave of network application expected in the 1980's, the class of problems that might be encountered, and the increased productivity envisioned utilizing the network concepts.

"Distributed Processing Applications Using the mc6801 and the mc68488," D. Tietjen and R. Thompson, Motorola ICD

"Hardware Modularity: The Key to Success in a Control Network," R. Grant, Pro-Log Corp

"Master-Master Party-Line Bus in a Microprocessor Network," M. E. Stickle, *et al*, RCA David Sarnoff Research Center

"Communications Delays in Distributed Data Acquisition and Control Systems," J. D. Schoeffler, Cleveland State University

"Computer Network Standards for the Process Control Industrial Environment," D. T. Sze, IBM Zurich Research Lab

Session 28

10 am-12:30 pm

Batteries for Modern Applications

Session Organizer/Chairman: J. A. Wiseman, Gould Inc, Portable Battery Div

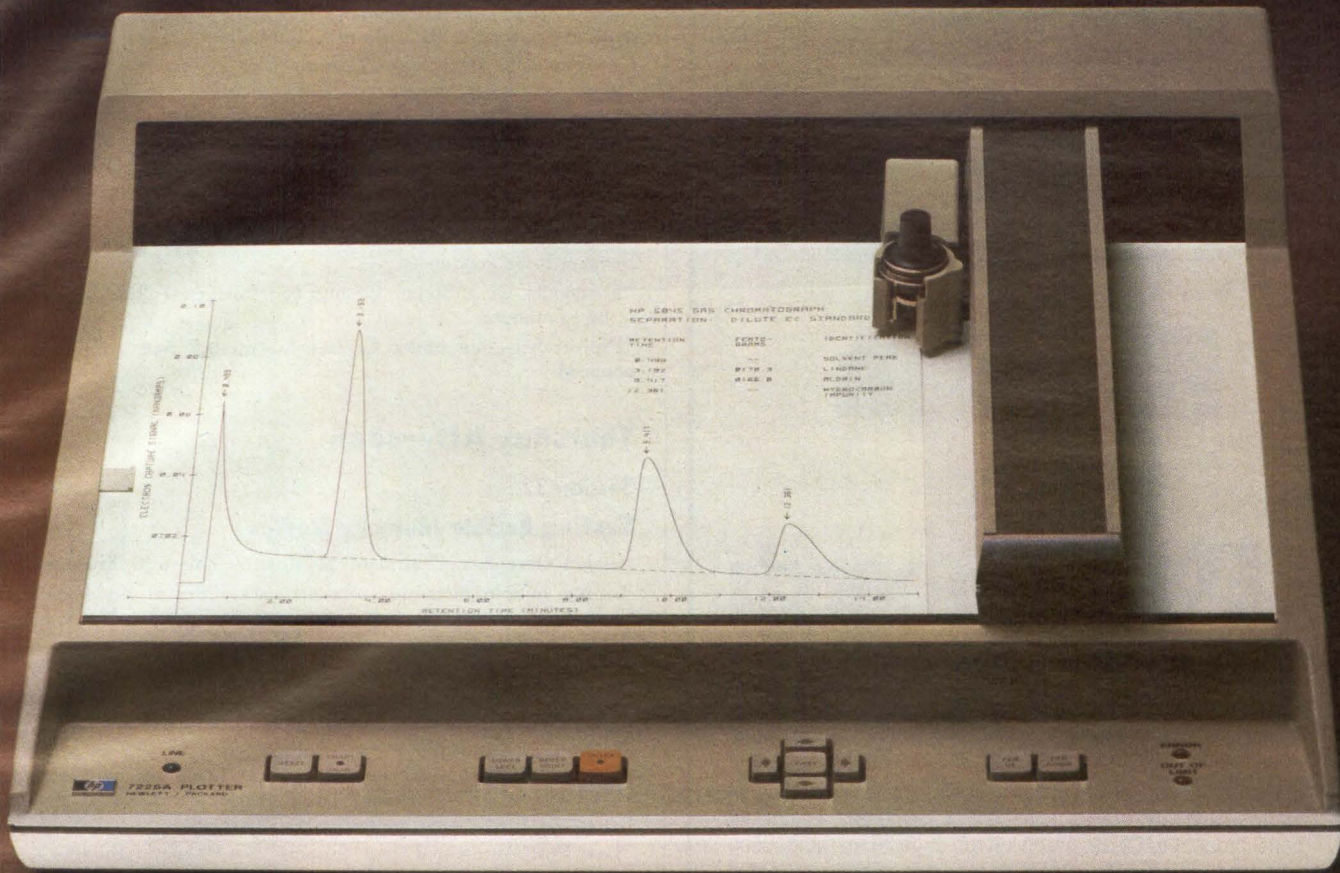
This session offers useful application information on portable battery power from the relatively mature, proven and well established technology of sealed-nickel-cadmium to a unique and innovative approach to lead-acid in the rechargeable battery field and to the very recently developed technologies of zinc-air and lithium batteries for practical applications.

"Lithium Batteries—An Emerging Technology," B. McDonald, Mallory Battery

"High Energy Density Zinc-Air Cells for Portable Electronics," S. Bender, Gould Inc

"Sealed Lead-Acid Batteries," R. Hammel, Gates Energy Products

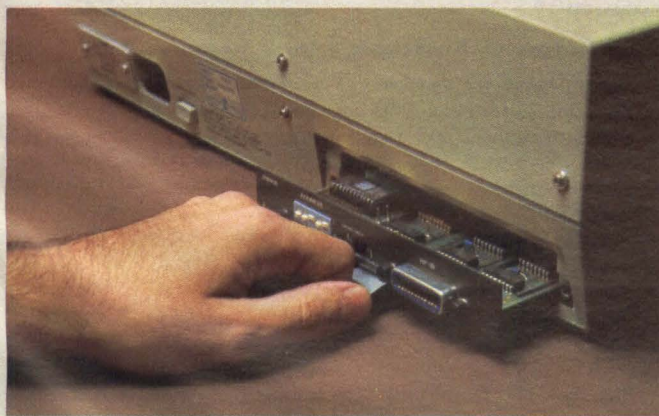
"Sealed Nickel-Cadmium—Backbone of the Portable Rechargeables," T. Wiseman, Gould Inc



Now OEM's can draw high quality graphics even when the bottom line is price.

Graphics gives you the best way to analyze and communicate data. But cost has been keeping it out of the picture for many OEM systems. That's why Hewlett-Packard is offering the new Model 7225A Graphics Plotter.

The price: \$1750 (domestic USA price with 17602A general purpose "personality" module), in quantities of five. With further OEM discounts from there.



Plug-in "personality modules" customize the plotter for you.

HP's versatile 7225A converts the output of processor based systems into high quality charts and graphs in any size up to 8½ x 11" (A4). A wide selection of plug-in "personality modules" lets you adapt the plotter to suit your needs. Different modules determine interface hardware, language, and capabilities such as internal character sets, axis generation, labeling and scaling.

Simple linear stepping motors eliminate many moving parts to assure reliability. Visually smooth, high resolution ink lines of any length and angle are generated, requiring only end point data.

And you give your customers the confidence of Hewlett-Packard's worldwide service network.

So if you want high quality graphics but you draw the line at price, look into the Model 7225A Graphics Plotter. For a detailed 24-page OEM brochure, contact Hal Phillips at Hewlett-Packard, 16399 West Bernardo Drive, San Diego, CA 92127; (714) 487-4100.

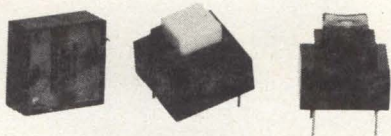
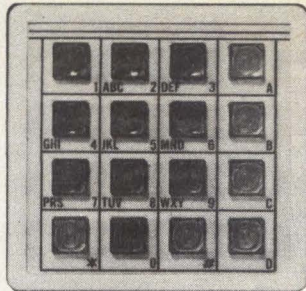
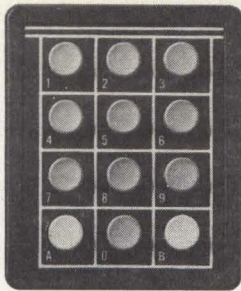
11901

HEWLETT  PACKARD

1501 Page Mill Road, Palo Alto, California 94304

For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

CIRCLE 68 ON INQUIRY CARD



LED Keyboards

L.E.D. Lighted—Mounted directly inside transparent colored keys, L.E.D.s provide visual status or function indication. 10, 12, or 16 station Low Profile Keyboards available with square or round keys in variety of color combinations. Universal circuit and pin-outs interface with most logic.

Unlighted—Low cost unlighted keyboards offer same design features and advantages as the L.E.D. keyboards. Easy front panel mounting. Clean, sharp keytop or decal marking. Long key life...5,000,000 plus cycles...and unique patented design assure reliable momentary contact.

Keyswitch Modules—Design your own keyboard. Single station keyswitch modules mount on PC or prepunched board with holes on .100" centers. Perfect for that odd keyboard layout or prototypes.

Distributor Stocked—Many standard keyboards stocked for off-the-shelf delivery. Contact your Stacoswitch Distributor today. He's got your keyboard.

STACOSWITCH DISTRIBUTUTORS—**ARIZONA:** Phoenix, R. V. Weatherford (602) 272-7144. **CALIFORNIA:** Anaheim, R. V. Weatherford (714) 634-9600; Glendale, R. V. Weatherford (213) 849-3451; Palo Alto, R. V. Weatherford (415) 493-5373; Pomona, R. V. Weatherford (714) 623-1261; San Diego, R. V. Weatherford (714) 278-7400; Santa Ana, Norstran, Inc. (714) 540-4165; Sunnyvale, Pyramid Electronics (408) 744-1900. **COLORADO:** Englewood, R. V. Weatherford (303) 761-5432. **ILLINOIS:** Chicago, LCOMP, (316) 628-1400; **MISSOURI:** Kansas City, LCOMP (816) 221-2400; St. Louis, LCOMP (314) 291-6200. **NEW YORK:** Lynbrook, Peerless Radio Corp. (516) 593-2121. **NORTH CAROLINA:** Winston-Salem, Kirkman Electronics (919) 722-9131. **TEXAS:** Dallas, R. V. Weatherford (214) 243-1571; Houston, R. V. Weatherford (713) 688-7406; Richardson, Southwest Electronics, Inc. (214) 234-3050; Stafford, Southwest Electronics, Inc. (713) 494-6021. **CANADA:** Vancouver, B.C., Intek Electronics (604) 324-6831.



1139 BAKER STREET, COSTA MESA, CALIF. 92626
(714) 549-3041 TWX: 910/595-1507

Other STACO Company products: Custom Transformers, STACO ENERGY PRODUCTS, Richmond, Indiana; Variable Transformers, STACO ENERGY PRODUCTS, Dayton, Ohio.

Session 30

10 am-12:30 pm

Engineering and Economics: You Can't Have One Without the Other

Session Organizer: Q. Gennaro, New Jersey Bell Telephone

Session Chairman: B. J. Blewitt, Public Service Gas and Electric

The economic viability of a product or system is often won or lost on the design engineering drawing board. Understanding the axioms and the tools of economics is an essential ingredient in career advancement, and how the engineering dollar is spent can make or break almost any project. This session focuses on the essential interfacing between engineering and economics—what every engineer needs to know and often doesn't.

"Engineering and Marketing in the Engineering Design Decision," Speaker to be announced

"Economics as a Stepping-Stone to Managerial Roles," Speaker to be announced

"Project Selection under Capital Restraints," Speaker to be announced

Thursday Afternoon

Session 32

2-4:30 pm

Testing Bubble Memory Devices

Session Organizer/Chairman: J. Mulady, Fairchild/Xincom

Testing bubble memories presents very different problems than those encountered in test procedures for present-day semiconductor memories. Six speakers define the problems and some solutions.

"Problems Unique to the Testing of Magnetic Bubble Memories at Both Wafer and Final Package," F. Quadri, National Semiconductor

"Testing of Bubble Memory Devices at Incoming Inspection by the Device User," J. Frank, Texas Instruments, Digital Systems Group

"Low Cost Automated Test Systems for Magnetic Bubble Memories," S. Bisset, Megatest Corp

"Distributed General Purpose Bubble Memory Test Systems," P. Burlison, Fairchild/Xincom

"Mechanical Probers and Handlers for Magnetic Bubble Memories," J. MacIntyre, Teledyne Tac

Session 33

2-4:30 pm

Advanced Automation

Session Co-Organizers: K. S. Fu and G. N. Saridis, Purdue University

Session Chairman: N. Caplan, National Science Foundation

"Robot Assembly Research and Future Applications," J. L. Nevins and D. E. Whitney, C. S. Draper Laboratory

"Manipulator-Control Automation Using Smart Sensors," A. Bejczy, Jet Propulsion Laboratory

"Syntactic Methods for Intelligent Control of a Manipulator," C. G. S. Lee and G. N. Saridis, Purdue University

"Programming and Data Structures for Sensor-Controlled Robots," R. L. Paul, Purdue University

Session 34

2-4:30 pm

The Future of Switching Power Supplies

Session Organizer/Chairman: W. J. Hirschberg, ACDC Electronics

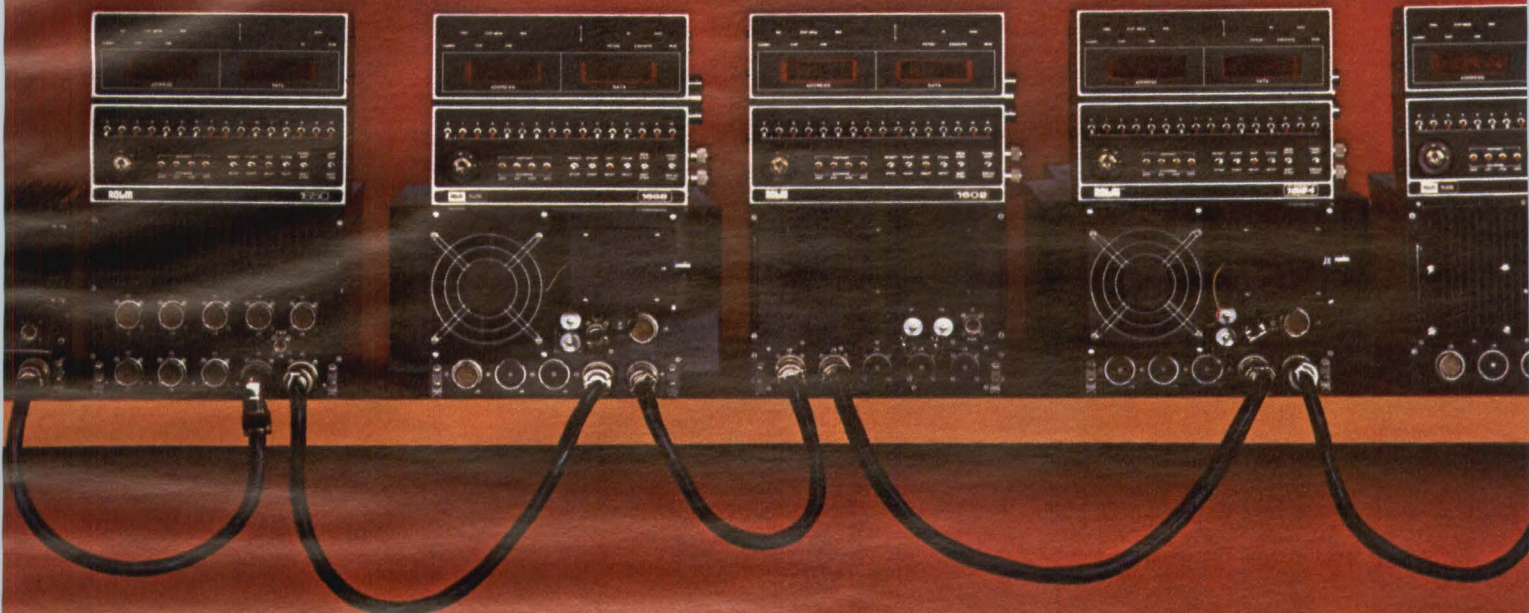
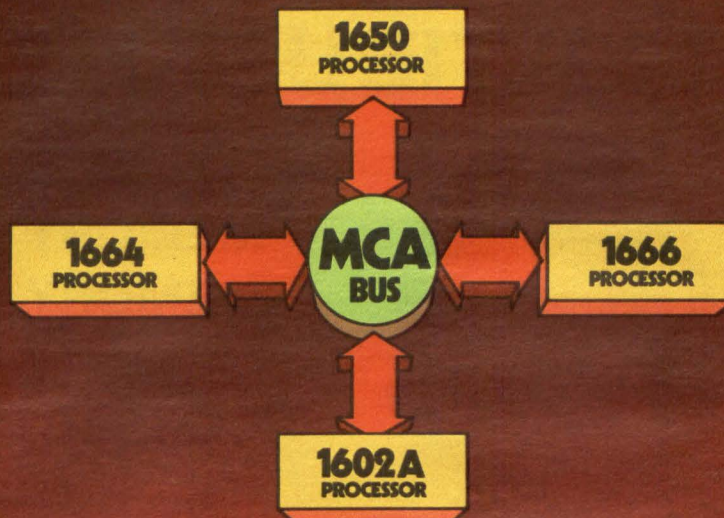
Opportunities for better performance, smaller size and less weight, greater reliability, and reduced cost are being challenged by tighter government regulations and society-written safety codes. This session reports on both great opportunities and the tough design problems.

"Applying Power FETs in Switching Power Supplies," B. Harvey, Siliconix

"Integration of Switching Power Supply Circuitry," S. Dendinger, Silicon General

"Novel, Unconventional Switching Power Supply Circuits," K. Check, Hewlett-Packard Data Systems

"Planning for Future EMI Constraints," J. Banasiak, R & B Enterprises □



The First Mil-Spec Computers with Strong Family Ties

ROLM's new Multiprocessor Communications Adapter (MCA) provides complete multiprocessor capability for ROLM's family of AN/UUK-19 processors including the half million word 1666. As many as 15 of these processors may be tied to a single MCA bus, providing redundant processing capability in large or critical systems, or for DMA-speed parallel communications in a multiprocessor environment. The MCA is an economical way to increase systems capability by easily connecting additional processors to the current system.

ROLM's MCA is now available for off-the-shelf delivery. It is fully supported by ROLM real time software systems. Processors sharing an MCA bus may operate under RMX/RDOS, RDOS, RTOS or a combination of all three. If you have system requirements for ROLM's MCA family plan, write or call for more technical information.

ROLM—innovation, performance, reliability and value engineering.

That's Why We're #1 in Mil-Spec Computer Systems

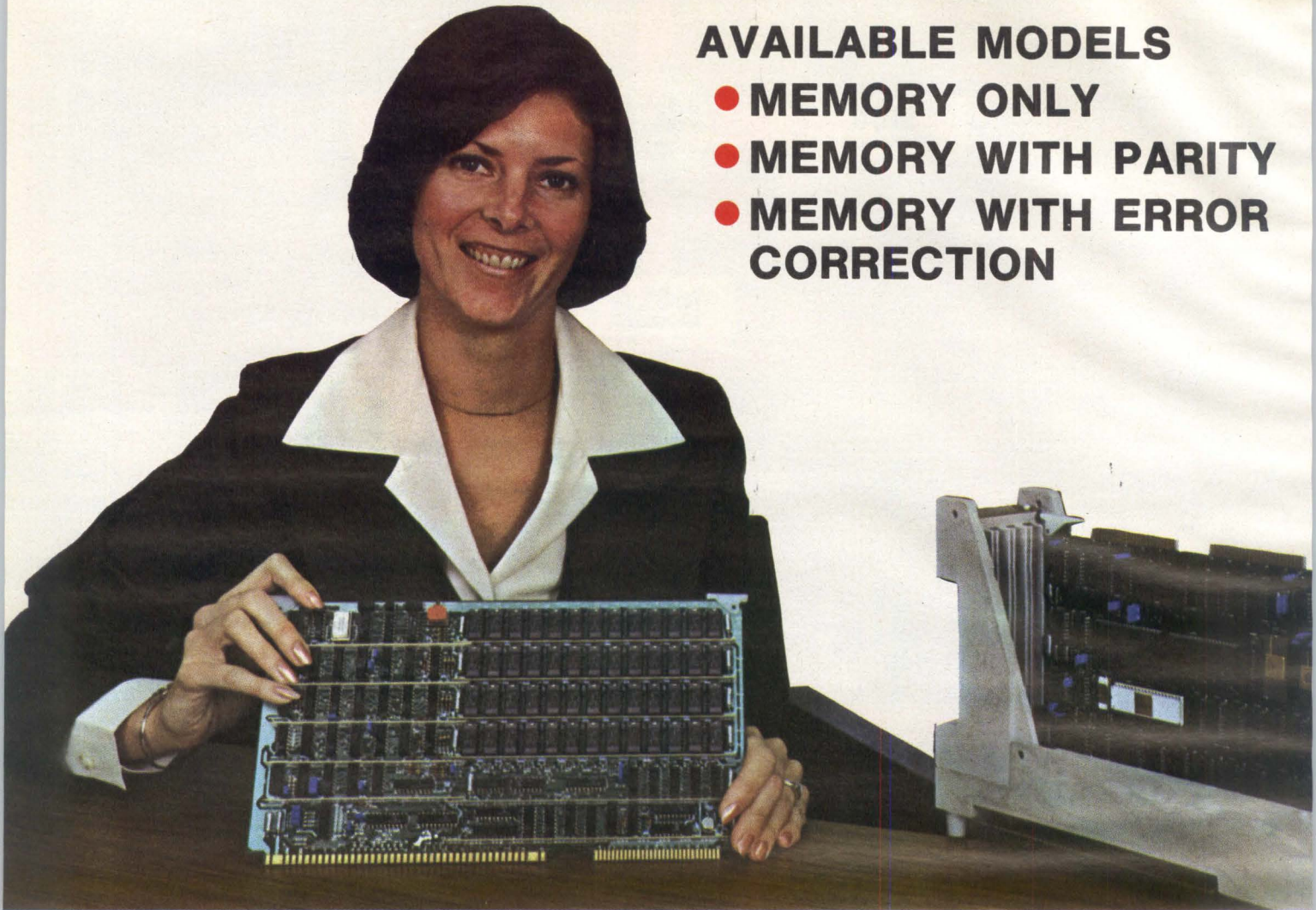
ROLM

MIL-SPEC
Computers

4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350.

In Europe: Muehlstrasse 19 D-6450, Hanau, Germany, 06181 15011, TWX 18-4170.

iSBC[®] MULTIBUS[®] MEMORY



AVAILABLE MODELS

- MEMORY ONLY
- MEMORY WITH PARITY
- MEMORY WITH ERROR CORRECTION

MUPRO's iSBC[®] Multibus[®] compatible memory is competitively priced and has been designed and specified to guarantee:

- Increased System Uptime**
- Reduced Power Consumption**
- Reduced Maintenance Expense**
- Reduced Overall System Cost**

The Memory is available in eight sizes from 4K bytes to 128K bytes/64K words.

MAJOR FEATURES

- Special backup power bus for minimum stand-by battery drain.
- Address space strapping options provide maximum user flexibility.

- The error correction option provides 85 times better reliability during the first 10,000 hours of operation.
- Compatible with iSBC[®] Extended Multibus[®] interface and Intellec MDS-800.
- Accommodates both 8-bit byte and 16-bit word transfers.
- Latching error indicator LEDs isolate single-bit errors to the individual memory chip and indicate double-bit errors.
- Strappable interrupt on non-correctable (double-bit) errors.
- $\pm 10\%$ margins on all supply voltages, plus battery backup mode.
- Provides power-fail capability.
- Provides on-card transparent refresh.
- 330 nsec access time, 450 nsec cycle time.



MUPRO

424 Oakmead Parkway
Sunnyvale, California 94086
(408) 737-0500
TWX 910-339-9251

See us at Electro '79 Booth 1635
And NCC '79 Booth 2700

iSBC[®], Multibus[®], and Intellec[®] are trademarks of Intel Corp.

Circle 71 for technical data Circle 187 for application assistance

Name _____ Title _____
Organization _____
Address _____
City _____ State _____ Zip _____
Telephone _____ Ext. _____
Application _____ Size K bytes _____
Delivery req'd (date) _____ Quantities _____

Model req'd: Memory only
Memory with Parity
Memory with Error Correction

ADD MY NAME TO MAILING LIST

DYNAMIC RAM CONTROLLER PERFORMANCE/COST TRADEOFFS

Designing a simple 16k dynamic RAM interface for a microprocessor based system involves critical decisions concerning address-row multiplexing, memory access timing control, and refresh counting

Andrew Volk Intel Corporation, Santa Clara, California

As microprocessor capabilities expand, the applications for larger amounts of system memory increase proportionally. For random-access memory, the designer can select either static or dynamic devices. Static random-access memories are probably the better choice when memory requirements are 8k bytes or less because of low cost, moderate system complexity, and straightforward memory interfacing. When storage requirements are 16k bytes or greater, dynamic random-access memories offer cost-effectiveness despite the need for additional control circuits to handle memory access, clock timing, and memory refreshing. Between these two densities, memory selection tradeoffs depend upon several interrelated parameters, including price, part types, microprocessor availability, logic gate interfacing, and designer experience.

Potential complexity of logic design should not deter designers from incorporating dynamic random-access memories (RAMs) into low to medium performance computing applications. Memory access timing and refresh requirements can be implemented easily and inexpensively for certain microprocessor based systems following basic dynamic RAM controller principles.

Controller Options

Several tradeoff options are available to the designer when developing a dynamic RAM controller. General RAM timing signals can be completely controlled by

logic gates and operated totally asynchronously from the microprocessor. This scheme achieves controller generality, permitting interfacing with any type of microprocessor. However, asynchronous timing is complex and expensive. If the RAM controller is dedicated to one type of microprocessor, then system design can be simplified by taking advantage of the microprocessor's inherent timing signals.

Refresh for dynamic RAMs can be handled by several techniques. Controllers that provide self-supporting refresh are highly general purpose oriented. This technique protects against long delays due to reset, wait states, direct memory access (DMA), or halt instructions, but it is expensive. Controller design can be simplified by refreshing either during machine cycles when the microprocessor is not accessing the RAMs (transparent refresh) or by software control. Software driven refresh does use a portion of the time the microprocessor would use for the main program's execution, but if properly designed, controller overhead can be held typically under 8%. This processing loss may not be a limitation, especially with low to medium performance systems.

Design Constraints

Basically, complexity of the dynamic RAM controller design is directly proportional to generality. To minimize complexity and expense, controller design is driven by certain system constraints.

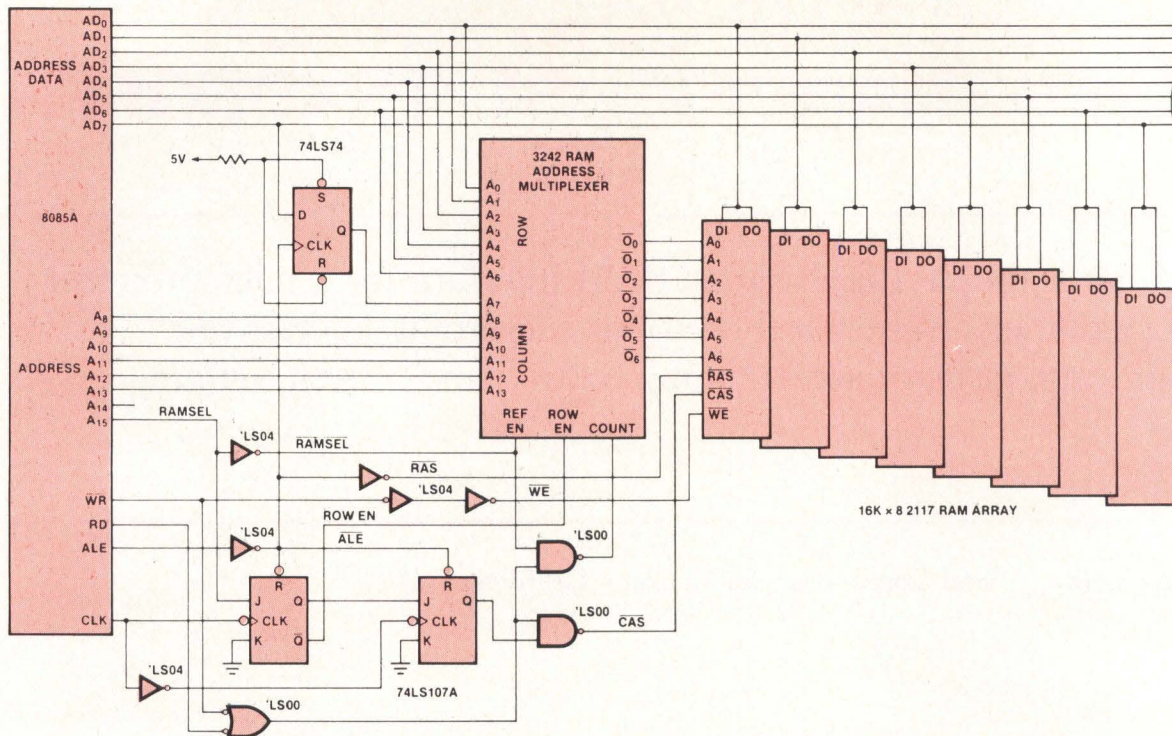


Fig 1 Dynamic RAM controller circuit. Microprocessor system uses clock and bus control signals plus four and one-half TTL packages to support timing and refresh requirements of 16k dynamic RAMs. 3242 multiplexes 8085A addresses and provides refresh addresses for 2117 type RAMs. RAS, CAS, and WE RAM control signals are generated by remaining TTL. Refresh can be provided during memory cycles when dynamic RAM is not accessed, or by software

(1) The system will not be subject to long reset, wait, DMA, or halt states. This consideration allows the design to depend on processor activity for refresh. (Note that this may make it more difficult to use certain debug aids that suspend processor activity or use single-stepping.)

(2) The RAM will be used for data storage only (no program execution) or some execution time can be designated. If the RAM is used for data storage only, transparent refresh can easily be provided; otherwise, software refresh can be provided inexpensively.

(3) Only one type of microprocessor will access the RAM. This dedication allows the system design to be optimized to that microprocessor's timing.

Governed by these boundaries, a dynamic RAM controller has been designed with an 8085A microprocessor and 2117-type 16k dynamic RAMs (Fig 1). System design divides into three basic functions: address multiplexing, timing logic, and refresh control (Tables 1 and 2).

Address Multiplexing

Dynamic RAMs of the 2117-type require their addresses to be presented in two 7-bit segments to access a memory cell array of 128 rows and 128 columns. Micro-

processor addresses A_0 through A_{13} provide these two segments which are time-multiplexed onto RAM pins A_0 to A_6 . The first segment—row address—selects one of the 128 rows. Since accessing any bit in the addressed row refreshes the entire row, the row address is also used for the refresh address. All 128 rows must be accessed within the refresh period, usually 2 ms. The row address is latched into the dynamic RAM by the row address strobe (\overline{RAS}), which is also used to start the memory access cycle. The second segment—column address—selects the proper bit along the previously selected row. The column address is latched into the RAM by the column address strobe (CAS). This strobe completes the memory access cycle and enables the RAM to either read or write. Both address strobes are generated by external timing logic.

The two segments are first delivered to the 3242-type RAM address multiplexer, a 7-bit 2 to 1 multiplexer (Fig 2). In addition to excellent output drive capability and ease of use, this address multiplexer contains an integral 7-bit refresh address counter. This counter provides completely transparent refreshing during memory cycles when the dynamic RAM is not otherwise being accessed. The 3242 has a row enable (ROW EN) input that selects row addresses when high and column addresses when low. The internal refresh counter is activated by the refresh enable (REF EN) input and

TABLE 1
Dynamic RAM Controller
System Signal Definitions

<u>Parameter</u>	<u>Description</u>
A. 2117 RAM	
$\overline{\text{RAS}}$	Row Address Strobe selects row and starts RAM cycle
$\overline{\text{CAS}}$	Column Address Strobe selects bit from row, completes RAM cycle
$\overline{\text{WE}}$	Write Enable allows selected bit to be written
DI	Data Input is data to be written
DO	Data Output is data from selected bit, enabled by $\overline{\text{CAS}}$
A ₀ to A ₆	Time multiplexed address bits, strobed by $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$
B. 8085A MPU	
ALE	Address Latch Enable strobes lower eight addresses on data bus
$\overline{\text{RD}}$	Read requests data to be presented to 8085A
$\overline{\text{WR}}$	Write indicates data on AD ₀ to AD ₇ to be written
AD ₀ to AD ₇	Time multiplexed address/data bus
A ₈ to A ₁₅	Upper eight address bits from 8085A
CLK	Clock output from 8085A (synchronous)
TRAP	Nonmaskable interrupt input
C. TTL	
ROW EN	Row Enable controls 3242 address multiplexer to select row address
REF EN	Refresh Enable selects 3242's internal refresh address counter
COUNT	Count increments 3242's internal refresh counter
RAMSEL	RAM Select enables TTL to access the RAM
BANKSEL	Bank Select selects RAMs to be accessed in 32k system (Fig 4)

TABLE 2
Performance Values of Timing Signals

<u>Parameter</u>	<u>Description</u>	<u>Time (ns)</u>	
		<u>Min</u>	<u>Max</u>
A. 2117-4 RAM			
t _{RAC}	Access Time from $\overline{\text{RAS}}$	—	250
t _{CAC}	Access Time from $\overline{\text{CAS}}$	—	165
t _{RCD}	$\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ Delay Time	—	85
t _{ASB}	Row Address Setup Time	0	—
t _{RAH}	Row Address Hold Time	35	—
t _{ASC}	Column Address Setup Time	-10	—
t _{CAH}	Column Address Hold Time	75	—
t _{WCS}	Write Column Setup Time	-20	—
B. 8085A MPU			
t _{AL}	Address Valid before ALE Falling	115	—
t _{LCK}	ALE Falling Edge to Next CLK Falling Edge	100	—
t _L	CLK Low Time	80	—
t _{CYC}	CLK Cycle Period	320	—
t _{DS}	Data Setup Time to CLK Rising in T _s	100	—
t _{CL}	CLK Falling to Control ($\overline{\text{RD}}$, $\overline{\text{WR}}$) Falling	—	60
C. TTL			
t _{DRAS}	TTL Delay from ALE to $\overline{\text{RAS}}$	0	30
t _{DCAS}	TTL Delay CLK to $\overline{\text{CAS}}$	0	40
t _{DWE}	TTL Delay from $\overline{\text{WR}}$ to $\overline{\text{WE}}$	—	30
t _{DROW1}	TTL Delay from ALE to ROW EN	—	40
t _{DROW2}	TTL Delay from CLK to ROW EN	—	20
t _{OO1}	Row Enable to Address Valid (3242 Multiplexer)	—	40

incremented by $\overline{\text{COUNT}}$; all three input signals are provided by external timing logic. The $\overline{\text{ZERO DETECT}}$ output detects when the lower six bits of the internal refresh counter are zero. This output is useful for a burst refresh counter in more complex designs, but is not used here.

During normal reads or writes, REF EN is kept low. At the beginning of the memory access cycle, ROW EN is high, selecting the row address—microprocessor addresses A_0 to A_6 —through to the output pins, \overline{O}_0 to \overline{O}_6 . Note that the input addresses are inverted on the outputs; this must be observed when checking out the circuit. After the row address is latched into the RAMs by $\overline{\text{RAS}}$, ROW EN is taken low and the column addresses—microprocessor addresses A_7 to A_{13} —are selected and held until after $\overline{\text{CAS}}$ has strobed them.

During memory refresh cycles, REF EN is taken high before $\overline{\text{RAS}}$ goes low. This selects the outputs of the internal 7-bit refresh counter. (When REF EN is high, the state of ROW EN is ignored.) $\overline{\text{RAS}}$ is then taken low to strobe in the refresh address. After the address is stored, COUNT is clocked to increment the refresh address.

In the 8085A, the lower eight addresses (AD_0 to AD_7) are multiplexed with the data bus lines and are available only during the first clock period of the machine cycle. For this reason, an external 8-bit address latch is normally required with a standard RAM to hold these address bits. However, the 2117-type dynamic RAMs have an internal 7-bit row address

latch, which eliminates the need for all but one bit of the external address latch. Address AD_7 is held in one-half of a 74LS74 flip-flop until $\overline{\text{CAS}}$ can strobe it into the RAMs as the least significant bit of the column address.

Timing Logic

Timing logic generates three RAM timing signals— $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and write enable ($\overline{\text{WE}}$)—and three address multiplexer control signals— ROW EN , REF EN , and COUNT . In this system design, the 8085A address latch enable (ALE) is used to generate $\overline{\text{RAS}}$, after buffering. The falling edge of ALE is specifically timed to provide sufficient setup and hold times to strobe the lower eight address bits into the dynamic RAM and 74LS74 external latch, thereby making an ideal row address strobe. Since ALE occurs every machine cycle, the RAMs are activated during all processor cycles. To prevent conflict on the data bus during reads or accidental writes, the RAM access cycles are qualified by $\overline{\text{CAS}}$, which acts as a delayed chip select in the 2117-type RAM and must be present to output or accept RAM data. The presence of $\overline{\text{RAS}}$ in every machine cycle increases power consumption, but simplifies the required timing logic and allows straightforward refreshing.

The ROW EN and $\overline{\text{CAS}}$ signals are generated using inverters, NAND gates, and two 74LS107A J-K type flip-flops. ALE is first inverted; it then clears the two

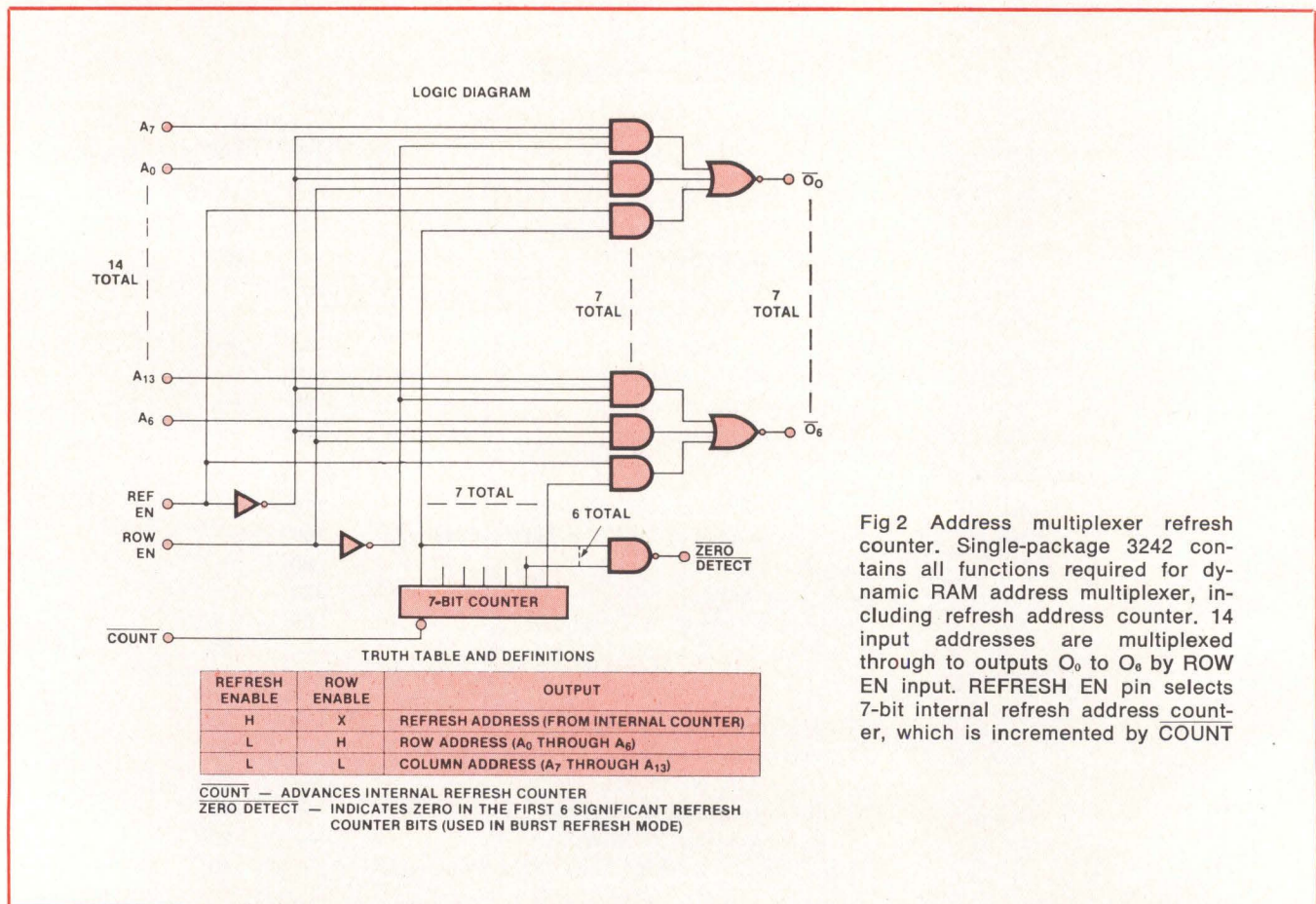


Fig 2 Address multiplexer refresh counter. Single-package 3242 contains all functions required for dynamic RAM address multiplexer, including refresh address counter. 14 input addresses are multiplexed through to outputs \overline{O}_0 to \overline{O}_6 by ROW EN input. REFRESH EN pin selects 7-bit internal refresh address counter, which is incremented by COUNT

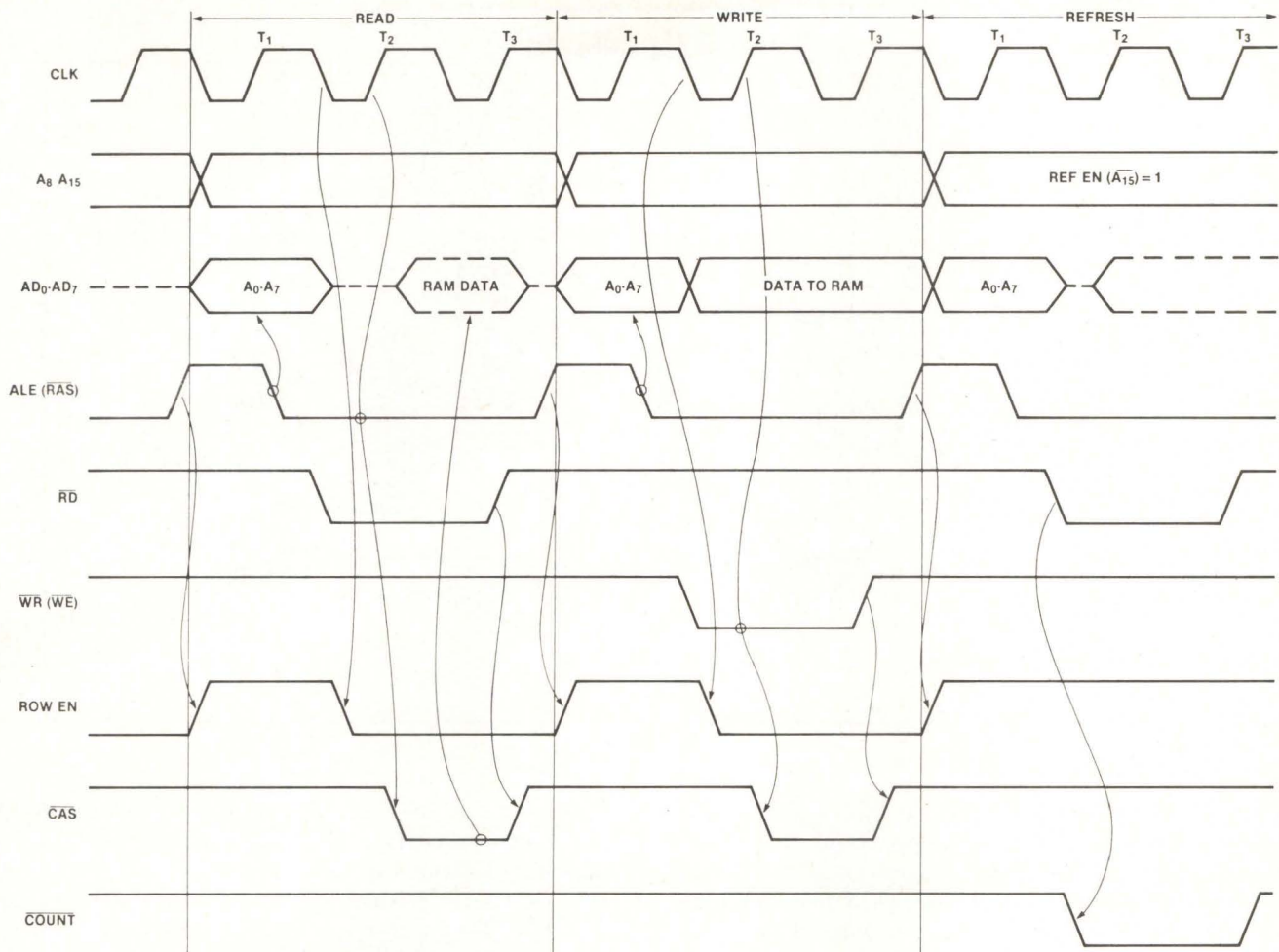


Fig 3 RAM read/write and refresh timing. All controller timing is generated from 8085A bus control and clock signals. ALE is buffered and used as RAS. It also triggers remaining read/write signals. ROW EN and CAS are generated off next two clock edges by two J-K flip-flops in Fig 1. RD or WR is used to terminate $\overline{\text{CAS}}$. WE to RAMs is buffered form of WR. Refresh is enabled through REF EN in any cycle that dynamic RAM is not accessed. During refresh cycles, RD or WR is used to increment refresh address counter

flip-flops at the beginning of each machine cycle (Fig 3). This drives both ROW EN and $\overline{\text{CAS}}$ to high. A RAM select (RAMSEL) signal is connected to the input of the first flip-flop. Only when the RAM is selected (RAMSEL high) will flip-flop outputs change on subsequent clocks and enable $\overline{\text{CAS}}$ to go low. For simplicity, address line A₁₅ is used as RAMSEL, which selects addresses 8000₁₆ to FFFF₁₆ as the RAM area.

ROW EN is held high until the next falling edge of the 8085A clock (CLK) output, furnishing the necessary row address hold time. $\overline{\text{CAS}}$ is enabled and goes low on the next rising edge of clock; this provides enough delay for the column address to be set up. Activation of $\overline{\text{CAS}}$ is also controlled by the 8085A read ($\overline{\text{RD}}$) and write ($\overline{\text{WR}}$) bus control signals. After $\overline{\text{RD}}$ or $\overline{\text{WR}}$ is active, $\overline{\text{CAS}}$ is enabled by the second flip-flop; thus, the two control signals have no effect on the leading edge

of $\overline{\text{CAS}}$. However, they ensure that the trailing edge of $\overline{\text{CAS}}$ is held long enough to guarantee the data-hold time during reading; yet, $\overline{\text{CAS}}$ is terminated in time to prevent conflict between the RAM data outputs and the 8085A lower eight addresses in the next machine cycle. RAMSEL can go high during unstable address periods, causing the two flip-flops to switch. However, $\overline{\text{CAS}}$ cannot be activated since neither $\overline{\text{RD}}$ nor $\overline{\text{WR}}$ is active during these periods. Write enable ($\overline{\text{WE}}$) to the RAMs is provided by buffering the 8085A $\overline{\text{WR}}$ signal. Proper $\overline{\text{WE}}$ and data setup times to $\overline{\text{CAS}}$ are guaranteed by clock (CLK) timing.

This system design provides 430 ns of access time from RAS and 180 ns of access time from $\overline{\text{CAS}}$, even at the full processor speed of 3.125 MHz. The $\overline{\text{CAS}}$ access time will be the limiting case in selecting the slowest dynamic RAM that will work in this system.

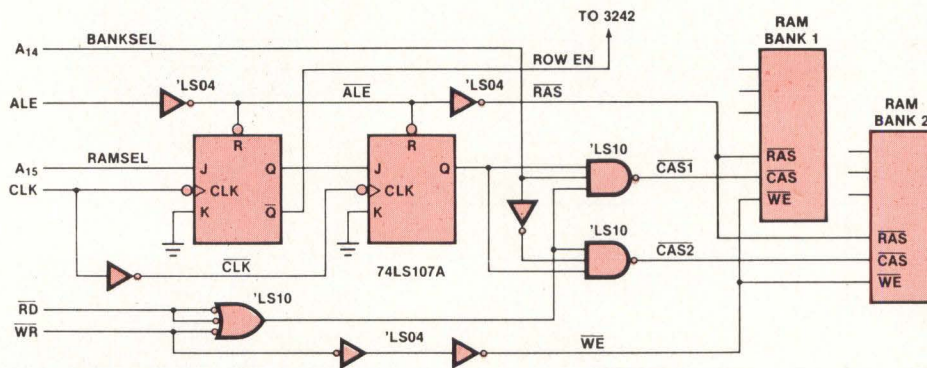


Fig 4 Expanding controller capacity to 32k bytes. Circuit of Fig 1 can be modified to support 32k bytes of dynamic RAM. This is accomplished using single package of three input NAND gates to decode two separate CAS control signals. In this circuit, A14 is used as BANKSEL to choose which array of 16k RAMs is selected. CAS1 and therefore RAM Bank 1, are enabled when A14 is high, and CAS2 when low

However, the designer will find that $\overline{\text{CAS}}$ access time is slow enough to enable a choice from among the least expensive speed selections.

A slight modification requiring just a few additional gates allows this same timing logic to support 32k bytes of dynamic memory (Fig 4). Address A14, which is bank select (BANKSEL), selects between two 16k RAM banks. Chip selection is still done through $\overline{\text{CAS}}$. Since $\overline{\text{RAS}}$ still activates the RAMs during every machine cycle, power consumption is slightly higher, but the provision for straightforward refreshing is the same as in the design described previously.

Refresh Control

The 2117-type 16k dynamic RAMs must be refreshed by accessing all 128 row addresses every 2 ms. Normal 8085A microprocessor read ($\overline{\text{RD}}$) or write ($\overline{\text{WR}}$) signals can be used for refreshing the RAMs. This technique allows a simple software routine to do the job. The RAMs can also be refreshed by a special $\overline{\text{RAS}}$ -only refresh cycle, in which the regular $\overline{\text{RAS}}$ signal strobes in the row (refresh) addresses, but the RAMs are not further accessed by $\overline{\text{CAS}}$. Because the RAMs are not "selected" by $\overline{\text{CAS}}$, this type of refresh can be hidden in memory cycles during which the dynamic RAM is not otherwise accessed.

$\overline{\text{RAS}}$ -only refresh can be completely transparent if the system design provides at least 128 processor machine cycles where the dynamic RAM is not accessed. In general applications where substantial programs can be executed from RAM, this requirement is difficult to guar-

antee. On the other hand, it is easy to accomplish if the dynamic RAM is used for data storage only. In this case, the fetching of instructions from the read-only memory (ROM) or static RAM, which stores the program, will provide the necessary nondynamic RAM refresh cycles. Although normal program execution provides several times the required refresh cycles, it is still necessary to prevent the processor from being held in long reset, wait, DMA, or halt states, since it is processor activity that basically provides the refresh times.

If programs stored in dynamic RAM must be executed and 128 refresh times cannot be absolutely guaranteed, software and an external refresh timing source must support refresh. Interrupts can force the processor to execute a refresh program every 2 ms. This program would only have to generate 128 non-RAM machine cycles before returning to the interrupted program to accomplish the refresh. The interrupt timing source can be borrowed from other realtime sources, such as baud rate generators, or can be generated separately by a one-shot or large-scale integration counter.

Table 3 lists an 8085A TRAP interrupt routine that provides the necessary 128 refresh cycles. This routine can be modified to fit the type of interrupt used, either maskable or nonmaskable. Main advantage and disadvantage of maskable interrupts are the designer's ability to disable them when the processor is executing a program in ROM, and the refresh is self-supporting. This saves interrupt overhead during these times. However, the designer must be sure to keep the interrupt enabled when needed, especially if there are other interrupts to be handled. The routine in Table 3

TABLE 3
Refresh Control Cycle Routine

Bytes	Refresh Cycles	Clock Cycles	Program	Comments
			REFRSH:	
1	1	10	PUSH PSW	; SAVE ACC AND FLAGS
2	1	7	MVI A,30	; LOAD ACC WITH LOOP COUNT
1	119	417	RFRSH1:	
3			DCR A	; COUNT LOOP
			JNZ RFRSH1	
			TRAP:	; (FOR TRAP INTERRUPT:)
1	1	4	RIM	; GET PREVIOUS IE STATUS
2	2	7	ANI 10H	; TEST IF PREVIOUSLY ENABLED
3	3	10	JZ RFRSH2	; IF NOT, DO NOT RE-ENABLE
1	1	4	EI	; ENABLE INTERRUPTS
			RFRSH2:	
1	1	10	POP PSW	; RESTORE ACC AND FLAGS
1	1	10	RET	; RETURN
<u>16</u>	<u>130</u>	<u>479</u>		

re-enables the interrupts at the end of the program to assure that no other interrupts are processed during refresh. Other interrupt routines should re-enable interrupts as soon as possible to avoid delaying refresh.

Using a nonmaskable interrupt request, such as the 8085A TRAP input, removes any concern that the state of the interrupt enable will prevent refresh. However, since it cannot be masked, TRAP will cause constant interrupt overhead unless the interrupt timing source can be separately disabled. Since the TRAP interrupt is accepted independent of the state of the interrupt enable status, keeping track of the enable status is only important if other interrupts are used. Table 3 also demonstrates how the 8085A can restore the previous enable status to avoid interference with the other interrupts. The interrupt enable status that existed prior to the TRAP is stored by the TRAP interrupt in the 8085A interrupt mask/status register. The contents of this register can be transferred to the accumulator by a read interrupt mask (RIM) instruction and the previous interrupt enable status can be tested (by ANI 10H—AND immediate with hexadecimal 10). This RIM instruction also ensures that previous interrupt enable status is cleared out, and that the current status and any future changes of interrupt enable status are reflected in the mask/status register until the next TRAP.

The routine in Table 3 requires only 16 bytes of memory and about 7.7% of available processor execution time. Overhead can be determined by calculating the number of clock cycles that the routine takes—479 cycles—and dividing by the total available in the 2-ms refresh period—6250 cycles at a 3.125-MHz processor

cycle rate. Note that the three instructions following the TRAP label are not to be used with nonTRAP interrupts, or may not be necessary in some applications. Without them, the routine is only 10 bytes. However, the loop count must be increased to 32 to keep the total number of refresh cycles correct. The total number of machine cycles is greater than 128 since the PUSH (data onto stack) and POP (data off stack) instructions may select a stack located in the dynamic RAM. Machine cycles that select the RAM do not generate refresh cycles in this design.

Instead of the 3242-type multiplexer, a pair of quad 2 to 1 data selectors can be used to multiplex the RAM addresses. In this case, ROW EN would be the data selection input. However, since the refresh counter is no longer available, the refresh addresses must be generated in software, as well as the count. Again, a hardware refresh timing source is required to enforce refresh. A nonmaskable interrupt request, such as the 8085A TRAP interrupt, is preferred because the interrupt must be recognized under all circumstances to guarantee that the RAM data are refreshed.

Table 4 delineates a sample software routine to generate 128 consecutive refresh addresses, if the internal counter of the 3242 multiplexer is not used for that purpose. This routine uses the POP instruction to generate most of the addresses, since the stack pointer is the only auto-incrementing register available in the 8085A. It restores previous interrupt enable status and takes about 7.8% of the microprocessor execution time. The routine is arranged so that the execution of the instructions provides 57 of the 128 addresses directly, and is written to minimize micro-

processor execution time. Other routines using iterative loops can be written in half the space, but take up to twice the CPU time.

Controller Performance

The challenge in designing a dynamic RAM controller is meeting the large number of often confusing timing specifications. The designer has to choose, from available timing sources, the correct signals that guarantee timing and that meet performance requirements.

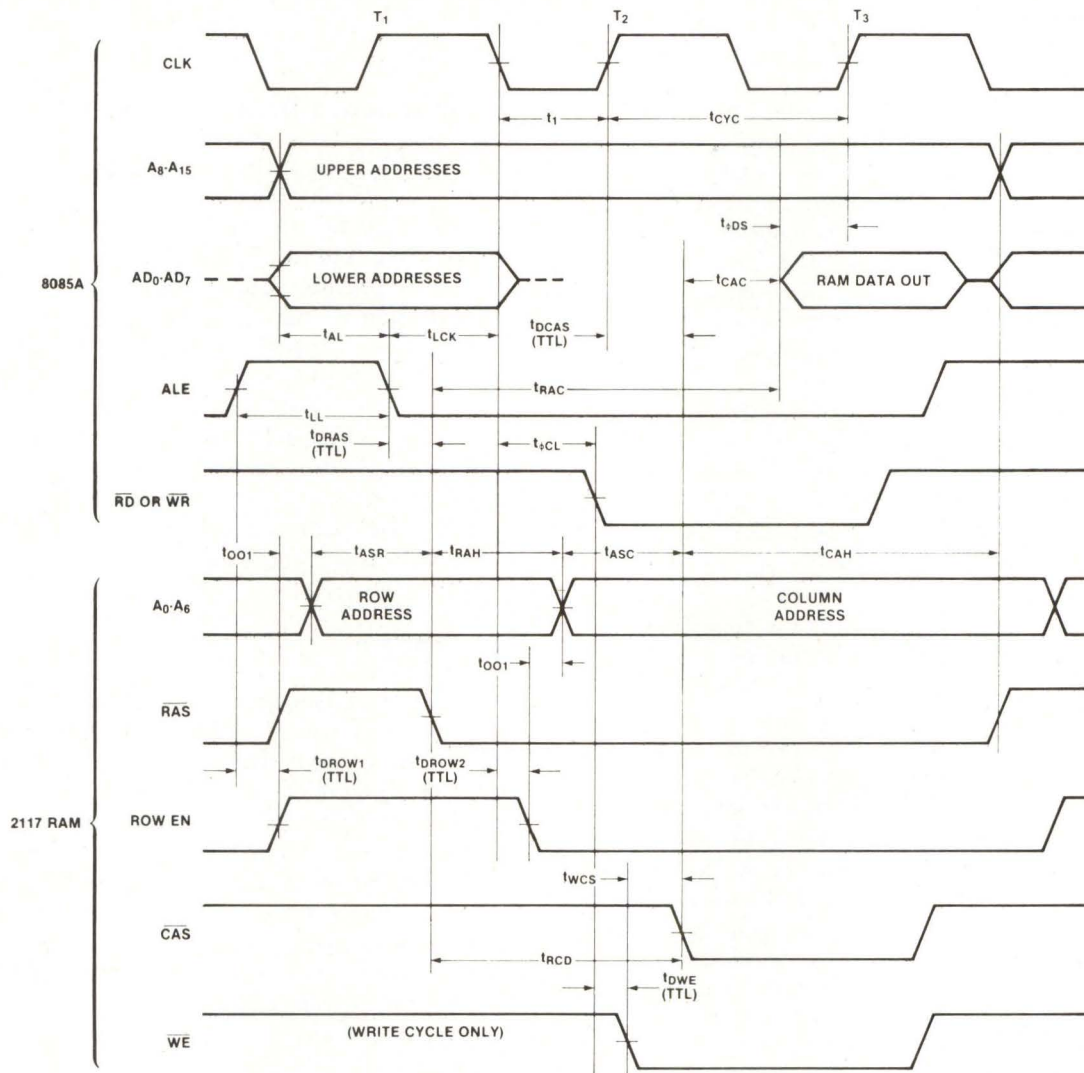
The controller functions properly if the timing provided by the microprocessor, less the applicable delays through the address multiplexer, flip-flop, and/or gates, is more than that required by the RAM input. Conversely, the RAM data output access time, less de-

lays, must be within microprocessor execution requirements. The designer's task involves correct evaluation of the available times and subtraction of the necessary delays.

For example, consider the row address setup time, t_{ASR} (Fig 5). The 8085A microprocessor provides a 115-ns address setup time to ALE (t_{AL}) and an ALE width (t_{LL}) of 140 ns. \overline{RAS} is formed from a double inversion of ALE, but for a worst-case analysis the benefit provided by the LS04 inverter propagation delays (2.5 ns minimum each) can be ignored. Two address delays are associated with the 3242-type multiplexer: the delay from an address input changing to a data output changing, and the delay to switch from row to column addresses (t_{OO1}). The first delay is applicable only if the ROW EN signal has been stable for some time before the address is stable, which is not the case

TABLE 4
Software Generated Refresh Addresses

Bytes	Refresh Cycles	Clock Cycles	Program	Comments
			REFRSH:	
1	1	12	PUSH PSW	; SAVE PROGRAM STATUS WORD (PSW)
1	1	12	PUSH H	; SAVE H AND L
3	3	10	LXI H,0	
1	1	10	DAD SP	; SAVE STACK POINTER IN HL
3	3	10	LXI SP,RFRSH1	
1	3	10	POP PSW	; DO 37 POP PSWs
1	3	10	POP PSW	} 37 POP PSWs
•	•	•	•	
•	•	•	•	
•	•	•	•	
•	•	•	•	
•	•	•	•	
•	•	•	•	
1	3	10	POP PSW	
1	3	10	POP PSW	
1	1	6	SPLH	; RESTORE SP
1	1	10	POP H	; RESTORE HL
			TRAP:	
1	1	4	RIM	; (TRAP INTERRUPT ONLY); ; GET PREVIOUS IE STATUS
2	2	7	ANI 10H	; TEST IF PREVIOUSLY ENABLED
3	3	10	JZ RFRSH1	; IF NOT, DO NOT RE-ENABLE
1	1	4	EI	; OTHERWISE ENABLE INTERRUPTS
			RFRSH1:	
1	1	10	POP PSW	; RESTORE PSW
1	1	12	RET	; RETURN
<u>57</u>	<u>131</u>	<u>487</u>		



	Available	Required (2117-4)
$t_{ASR} = t_{LL(min)} - t_{DROW1} - t_{O01(max)} + t_{DRAS(min)}$ $= 140 - 40 - 40 + 0^*$	= 60 ns	0 ns
$t_{RAH} = t_{LCK(min)} - t_{DRAS(max)} + t_{O01(min)} + t_{DROW2}$ $= 100 - 30 + 0^* + 0^*$	= 70	35
$t_{ASC} = t_1(min) - t_{DROW2(max)} - t_{O01(max)} = t_{DCAS(min)}$ $= 80 - 20 - 40 + 0^*$	= 20	-10
$t_{CAH} > t_{CYC}$	>320	75
$t_{CAC} = t_{CYC(min)} - t_{DCAS(max)} - t_{DS(max)}$ $= 320 - 40 - 100$	= 180	165
$t_{WCS} = t_1(min) - t_{CL(max)} - t_{DWE(max)} + t_{DCAS(min)}$ $= 80 - 60 - 30 + 0^*$	= -10	-20

*All minimum TTL delays are assumed to be 0 ns.

Fig 5 Controller performance evaluation. Evaluating performance of dynamic RAM system requires designer to identify appropriate signal relationships and time delays that make up each parameter. Some examples are shown with specifications of a slow speed 2117-4 type RAM. In every example, the controller provides at least a 10-ns margin even under worst-case combination of conditions. This performance allows designer to use slowest and least expensive RAM parts in this system

here. In this instance, the addresses and ROW EN both switch at about the beginning of ALE. However, the delay from the leading edge of ALE to ROW EN is greater than the delay to the addresses. Therefore, the worst-case t_{ASR} is equal to t_{LL} minus t_{001} , minus the time to generate ROW EN (t_{ROW1}), or about 60 ns, greatly exceeding the required time of 0 ns. Row address hold time (t_{RAH}) is equal to the time from ALE to the next clock edge (t_{LCK}), plus the delays through the two RAS buffer inverters (t_{DRAS}). Even ignoring the delays adding to the holding time, the time available is 70 ns, again sufficiently more than the required 35 ns. CAS address setup (t_{ASC}) and hold (t_{CAH}) times are determined by the 8085A clock low time (t_1) and by the time that the upper addresses are held stable (through state cycle T_3), respectively. There are two access time requirements for dynamic RAM: t_{RAC} , the access time from RAS, and t_{CAC} , the access time from CAS. The delay from RAS to CAS (t_{RCD}) will determine which of these access times is applicable. If t_{RCD} is less than the difference of t_{RAC} and t_{CAC} , the design is t_{RAS} limited. Conversely, if it is greater, the design is t_{CAS} limited. In this system, t_{RCD} is the time from ALE to the next clock edge (t_{LCK}), plus the clock low time (t_1) less the transistor-transistor logic (TTL) delays (t_{DRAS}), or about 160 ns minimum. This is twice the t_{RCD} required for even the slowest 2117-type RAM (85 ns); therefore, this design is definitely t_{CAC} limited.

Determining the access time from CAS requires using the 8085A clock related specifications; the data setup time to the rising edge of CLK in T_3 is 100 ns. CAS occurs one cycle ahead in T_2 ; therefore, access time is the CLK cycle time (t_{CYC}) minus the sum of the data setup time ($t_{\phi DS}$) and TTL delays in producing CAS (t_{DCAS}). If t_{DCAS} is about 40 ns, the access time (t_{CAS}) is 180 ns, adequate for 2117-4-type dynamic RAMs, which require 165 ns.

Other similarly subtle dynamic RAM requirements exist. Since the RAM data outputs are tied directly to the microprocessor bus, they must remain in the high impedance or floating 3-state mode during writes to avoid contention with the data being sent to the RAM. This is done in the 2117-type RAM by meeting the required \overline{WE} setup time to CAS (t_{WCS}). The 8085A clock related specifications define the maximum delay of \overline{WR} from CLK-falling ($t_{\phi CL}$) as 60 ns. \overline{WE} is delayed by two inverters from \overline{WR} , or about 90 ns from CLK-falling. CAS is delayed from CLK-falling by t_1 plus the TTL delay. \overline{WE} does not have to be low until 20 ns (t_{WCS}) after CAS. Even ignoring the TTL delay, there are 10 ns of margin. Also, 8085A CLK related specifications give parameters to evaluate data setup and hold times and other RAM specifications related to the timing of CAS.

Since all RAM address and control lines are TTL buffered, this system design can easily handle even 32k bytes. The extra capacitive loading on the data bus is no problem since 32k bytes represent only two RAMs per data bus line, and each RAM adds only 12 pF.

This leaves sufficient drive capability for adding ROMs or peripherals to the data bus without adding data bus buffering.

Miscellaneous Design Considerations

Dynamic RAM, in many ways an analog system, produces some harsh current spikes when accessed. This and any dynamic RAM design should follow proven printed circuit board layout practices that avoid crosstalk and provide acceptable power supply feeds. Gridded power busing—power lines running both parallel and perpendicular to the integrated circuit packages—is highly recommended to minimize inductive effects. A 0.1- μ F ceramic capacitor between every RAM device, alternately connecting V_{BB} and V_{DD} each to ground, is also proper practice to bypass current transients. Also, a large tantalum electrolytic bulk capacitor (at least 20 μ F) to prevent power supply droop on V_{DD} and V_{BB} is recommended.

Summary

Basic design principles of the low to medium performance system are adaptable to most inexpensive and easily implemented dynamic RAM controllers. Essentially, the key is the tradeoff between generality and expense. If it is determined that the design can be dedicated to a particular microprocessor, these concepts can be applied to reduce costs. In medium performance systems, simple software replaces considerable hardware without sacrificing undue processor execution time. The microprocessor clock and bus control outputs combined with a few TTL packages provide all the necessary RAM timing.

Bibliography

- G. Fielland, "Simplify Your Dynamic RAM/Microprocessor Interface," Intel Corp, Santa Clara, Calif, 1977
- G. Fielland and K. Oishi, "Keep the Memory Interface Simple," *Electronic Design*, Apr 26, 1978
- B. McCormick, "Application Techniques for the Intel 8085A Bus," Intel Corp, Santa Clara, Calif, May 1978



Andrew Volk is a senior design engineer in the custom circuits group of the Microcomputer Components Div at Intel Corp. His work has involved readying the 8080A for production, and then performing logic design for the 8085 and 8085A. He has acquired a BSEE and MSEE from the University of Wisconsin.

MULTIBUS[®] compatible memory systems

**NEW LOW PRICE
PLUS DELIVERY
FROM STOCK!**

4K to 64K RAM Up to 16K EPROM on one board.

Now you can have RAM and EPROM on the same board and buy as much or as little memory as you need. And because our memories use 16 pin memory element sockets you can change your memory when you change your mind.

Speaking of changing your mind, when you want to change address locations of either RAM or EPROM, it's done with two, on-board switches—providing 16 possible start locations for each memory.

Compare these features with our much improved read, write and refresh cycle times and you'll choose MSC first.

16K RAM Version

Up to 16K x 8 of RAM and up to 16K x 8 of EPROM on the same board.

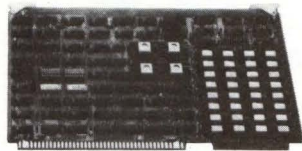
RAM expandable in 4K x 8 increments and EPROM expandable in 1K, 2K or 4K x 8 increments.

On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally MULTIBUS hardware and software compatible.

Limited one year warranty on parts and labor.



MSC 4502

CIRCLE 72 ON INQUIRY CARD

64K RAM Version

Up to 64K x 8 of RAM and up to 16K x 8 of EPROM on the same board.

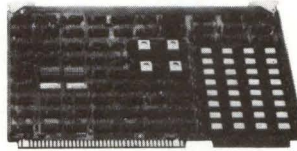
RAM expandable in 16K x 8 increments and EPROM expandable in 1K, 2K or 4K x 8 increments.

On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally MULTIBUS hardware and software compatible.

Limited one year warranty on parts and labor.



MSC 4602

CIRCLE 186 ON INQUIRY CARD

More MULTIBUS

Monolithic Systems has a full line of MULTIBUS compatible hardware and software products, including the MSC 8001, Z-80 based single board computer.

For more information call us today.

**MULTIBUS compatible
systems...from the
leader.**



Monolithic
Systems corp.

14 Inverness Drive East
Englewood CO 80112
303/770-7400

MULTIBUS is a registered trademark of
Intel Corporation.

©1978, Monolithic Systems Corp.

1. The inside story on the difference our full Data General **PRODUCT LINE** makes. *Reader Service #120*

3. Our **SMALL BUSINESS SYSTEMS** book explains the importance of having only as much computer capability as you need. *Reader Service #122*

5. Learn how our Real-Time Disc Operating System **SOFTWARE** gets you on-line fast, and keeps you there. *Reader Service #124*

7. How OEM's can solve potential problems by eliminating risks. *Reader Service #126*

9. The last word in microprocessor-based microNOVA systems with full 16-bit NOVA architecture. *Reader Service #128*

2. How **ECLIPSE** Data Systems' versatility answers the diverse business demands placed on a data system. *Reader Service #121*

4. Describes seven important Data General **SUPPORT SERVICES** that start and keep systems up and running. *Reader Service #123*

6. It's smart business to learn the benefits of our way of doing business. **WHY US** tells all. *Reader Service #125*

8. How the Data General **ECLIPSE M/600** gives more throughput, response and service than any other system in its class. *Reader Service #127*



GET ALL THE INFORMATION YOU NEED ABOUT COMPUTERS AT ONE STOP.

No other stop makes as much sense. You've got a choice of a whole family of reliable computers from \$100 computers-on-a-chip to \$1,000,000 multi-programming networks. The knowledge that there are 60,000 Data General computers installed in 33 countries. And our promise to keep a steady flow of quality, low-cost products coming. Mail the coupon for more information.

10. The unique story of our heuristic MULTI-PROGRAMMING operating system. Reader Service #129

12. How to customize a system to your application with Data General NOVA 4 systems, software and support. Reader Service #131

14. ECLIPSE S/230 sets the benchmark for big performance computer systems. Reader Service #133

16. ECLIPSE S/130, the standard setter. How to get the most from a mid-range mini. Reader Service #135

18. Fills you in on how our microNOVA has all the ingredients to handle complex problems requiring high-performance, real-time operations. Reader Service #137

11. The inside info on fast access to MASS STORAGE. Reader Service #130

13. How our computers are actually being used in APPLICATIONS. Reader Service #132

15. Explains how Data General DISTRIBUTED PROCESSING provides the ultimate in performance without disturbing your network. Reader Service #134

17. All the facts on our DASHER TERMINALS. Why they can work as you do. Reader Service #136

19. Get the whole story from our Data General ANNUAL REPORT. Reader Service #138



Mail to: Data General, Westboro, Mass. 01581

Your ad stopped me. Send the brochures I've circled.

Brochure numbers: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

Name _____ Title _____

Company _____

Address _____ Tel. _____

City _____ State _____ Zip _____



We make computers that make sense.

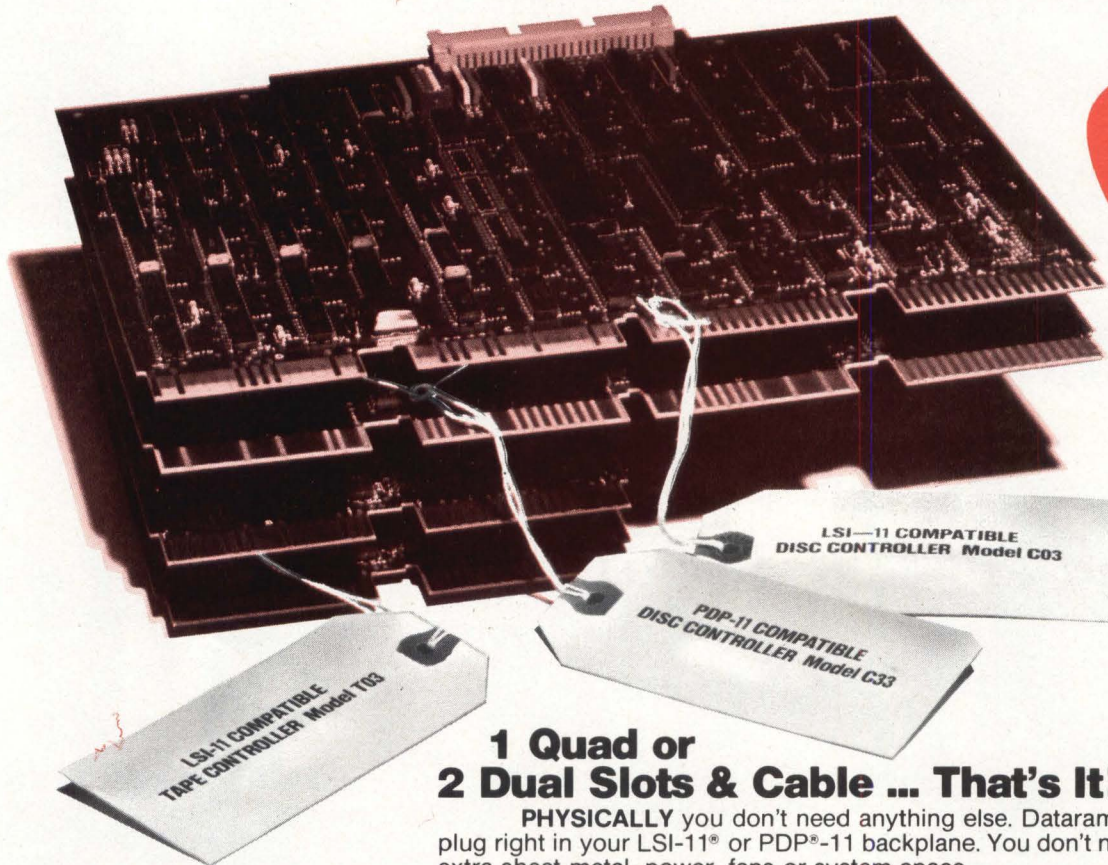
Data General Corporation, Westboro, MA 01581, (617) 366-8911. Data General (Canada) Ltd., Ontario. Data General Europe, 61 rue de Courcelles, Paris, France, 766.51.78. Data General Australia, (03) 89-0633. Data General Ltda., Sao Paulo, Brazil, 543-0138. Data General Middle East, Athens, Greece, 952-0557. © Data General Corporation, 1979.

CD 379

The Data General Computer Express – A live product presentation and demonstration – is coming to your area. Call your local Data General sales office. Or call direct (617) 366-8911, ext. 4722 for details.

Dataram

Dynus Disc/Tape Controllers Cost You Less To Use!



1 Quad or 2 Dual Slots & Cable ... That's It!

PHYSICALLY you don't need anything else. Dataram Controllers plug right in your LSI-11® or PDP®-11 backplane. You don't need, or pay for, extra sheet metal, power, fans or system space.

ELECTRICALLY you don't need anything else. Dataram Controllers simply become a part of your computer.

OPERATIONALLY you don't need anything else. Dataram Controllers are totally LSI-11 or PDP-11 software compatible — even diagnostics! They work with all independent RK05 or TU10 equivalents... there are no design subtleties that can *lock* you to one manufacturer's product. Dataram Controllers ensure that *you stay in control of your product.*

FINANCIALLY the cost to use Dataram Controllers is all up front. You won't get trapped by some single-source "bargain" unit with a non-standard format requiring additional software, limiting your operational flexibility or increasing your on-going costs for one-of-a-kind disc paks, etc., etc.

PHILOSOPHICALLY we make no promises, we just perform. Delivery is within 30 days . . . not "someday." Dataram LSI-11 or PDP-11 plug-in compatible Disc/Tape Controllers are real now ... not "soon to be" or "almost."

CONTACT Dataram and get the facts on the LSI-11 or PDP-11 Disc or Tape Controller that *Keeps You In Control . . . And Costs You Less To Use!*

**Dynus . . .
now part of Dataram**



**DATARAM
CORPORATION**

PRINCETON-HIGHTSTOWN ROAD
CRANBURY, NEW JERSEY 08512
TEL:609-799-0071 TWX:510-685-2542

LSI-11 and PDP are registered trademarks of Digital Equipment Corporation.

Dataram Corporation • Princeton-Hightstown Road • Cranbury, NJ 08512

- Please send complete details on Dataram Disc/Tape Controllers.
- Please have your sales representative call.

NAME _____ TITLE _____ PHONE/EXT. _____
COMPANY _____ DEPT./DIV. _____
ADDRESS _____
CITY _____ STATE _____ ZIP _____

FORECASTING COMPUTER SYSTEM RELIABILITY WITH A HANDHELD PROGRAMMABLE CALCULATOR

Equations, code, and user instructions for a calculator program which provides a fast, quantitative approach to understanding, evaluating, and improving computer hardware reliability

Ronald Zussman Securities Industry Automation Corporation, New York, New York

Contemporary computers made up of IC chip elements inherently provide better reliability than their predecessors, built with relays, vacuum tubes, or discrete transistors. Even today, however, non-redundant computer systems rarely enjoy mean-time-between-failures of over 2000 hours. Where there are stringent reliability specifications, essential computer components should be duplicated. Incorporating redundant hardware improves both reliability and maintainability—prerequisites for long, trouble free periods of continuous computer system operation.

Evaluating and enhancing computer system reliability are vitally important in nearly all processing applications. The equations and handheld calculator programs incorporated here provide computer designers with the tools necessary for making accurate reliability decisions. Redundancy must be introduced at the optimum level in the hierarchy of computer system organization in order to achieve maximum reliability at reasonable cost and complexity. The reliability models described ascertain the elements that need to be replicated, and determine the resulting total system reliability. It is assumed that the reader is familiar with handheld programmable calculators.

Programmable Calculators

The handheld programmable calculator offers convenience, portability, and a capability for powerful decision making. Texas Instruments' model TI-59 when used with a companion PC-100A thermal printer also produces alphanumeric messages and labels the results. The Reliability Analysis Program, using the instructions set forth in the Instructions, executes on the TI-59 in only a few seconds running time, with or without printer attached, and provides answers to intricate "what if" questions. It is easier and more revealing to determine computer system reliability interactively on a programmable calculator than to run a FORTRAN batch implementation of the program on a large computer.

Inputs to Reliability Model

To determine overall system reliability, element mean time between failures (MTBF), mean-time-to-repair (MTTR), the configuration, system failure modes, and minimum downtime that constitutes a failure must all be specified. MTBF and MTTR values for individual elements can be computed from trouble report statistics, estimated

TI-59 Reliability Analysis Program

Partition: 479.59

Program Listing:

```

000: Lbl B' STO 12 CP ( x=t 016 RCL 12 x Dsz B 06 1 ) INV SBR
019: Lbl List STO 00 Lbl Prt RCL Ind 00 Op 01 Op 20 RCL Ind 00 Op 02
035: Op 20 RCL Ind 00 Op 03 Op 20 RCL Ind 00 Op 04 Op 20 Op 05 INV SBR
052: Lbl ifflg Op 00 RCL 54 Op 01 Op 05 INV SBR Lbl D.MS Op 00 RCL 55
069: Op 01 RCL 56 Op 02 Op 05 INV SBR Lbl C x⇐t 2 2 STO 00 5 8 GTO Σ+
089: Lbl A x⇐t 5 7 Lbl Σ+ Fix 2 STO 13 ifflg 0 x Stflg 0 Adv SBR Prt
108: Lbl x Adv SBR ifflg RCL Ind 13 Op 04 x⇐t Op 06 STO 01 1/x SUM 02
125: RCL 02 1/x STO 03 SBR D.MS RCL Ind 13 Op 04 RCL 03 Op 06 INV SBR
141: Lbl B x⇐t SBR ifflg SBR x≥t + RCL 01 = ÷ RCL 01 = 1/x Prd 04 1 -
161: RCL 04 = ÷ RCL 04 x RCL 03 = x⇐t SBR D.MS Lbl x≥t RCL 58 Op 04
180: x⇐t Op 06 INV SBR Lbl D x⇐t SBR ifflg SBR π ÷ x⇐t ( x⇐t + RCL 01 )
199: +/- + 1 = Prd 05 RCL 05 - 1 = +/- STO 04 ÷ RCL 05 x RCL 03 = STO
221: 03 x⇐t SBR D.MS Lbl π RCL 57 Op 04 x⇐t Op 06 INV SBR Lbl A' Adv
238: 1 4 SBR List Pgm 01 SBR CLR 1 STO 04 STO 05 INV Stflg 0 Fix 0
256: INV SBR Lbl C' Adv 3 8 SBR List RCL 04 INV Fix Prt INV SBR Lbl E
272: Fix 0 STO 06 Adv 2 6 SBR List SBR Prt RCL 06 Prt R/S STO 07 SBR Prt
291: RCL 07 Prt R/S Fix 2 STO 02 ÷ ( RCL 07 - RCL 06 + STO 08 1 = STO
312: 01 SBR ifflg RCL 02 x⇐t SBR x≥t SBR D.MS RCL 01 x⇐t SBR x≥t R/S
328: x x⇐t SBR ifflg ( SBR π ÷ RCL 02 ) yx RCL 08 x RCL 08 B' x ( RCL 06
350: - 1 ) B' ÷ RCL 07 B' = STO 03 ÷ x⇐t ( x⇐t + RCL 01 = STO 04 SBR
372: D.MS RCL 03 x⇐t SBR π INV SBR Lbl D' Adv Stflg 1 STO 09 4 2 SBR List
390: 0 Lbl E' STO 11 ifflg 1 Dsz 4 6 Adv SBR List RCL 11 Fix 0 Prt SBR
409: Prt Lbl Dsz Fix 2 RCL 59 Op 04 RCL 09 Op 06 RCL 09 ÷ RCL 03 =
428: STO 10 +/- INV Inx x RCL 10 yx RCL 11 ÷ RCL 11 B' = INV Fix
446: INV Stflg 1 Prt Inv SBR

```

Prestored Data Registers:

14:	3517272413	1424272437	4500133113	2745362436	5100361735	2417360030
20:	3216172700	2000000000	5100003313	3513272717	2700303216	1727002000
26:	5100001331	4500262032	2120310030	3216172720	3132400041	3124373600
32:	3517344124	3517166400	3132400041	3124373600	1342132427	1314271764
38:	7500134213	2427131424	2724374500	6400000000	7500351727	2413142427
44:	2437450024	3100000000	7500333532	1413142427	2437450032	2100000000
50:	2113242741	3517360024	3100000000	0	4131243720	3641143645
56:	3637173020	2030371421	2030373735	2023353664		

Note: With calculator in learn mode, enter keystrokes found in program listing and store tabulated numbers into registers. Record calculator memory on two mag cards for future use. Reading these cards is a convenient way to reload entire program.

from reliability handbooks, or obtained from vendors. A failure must be defined in terms of equipment and downtime for the application being analyzed. For example, if the back-end computer of a large realtime switching network is not operational for a brief time span, such downtime can be masked by a frontend processor. With batch systems, brief soft failures may be tolerated even more readily.

The first step in determining the reliability of any computer installation is to draw a diagram showing the primary elements joined so as to indicate how their relationship affects system operation. This diagram does not usually represent actual physical connections. Thus, large and complicated configurations can be reduced to three basic reliability dependencies: series, parallel, and K of N (any K elements required to be operational

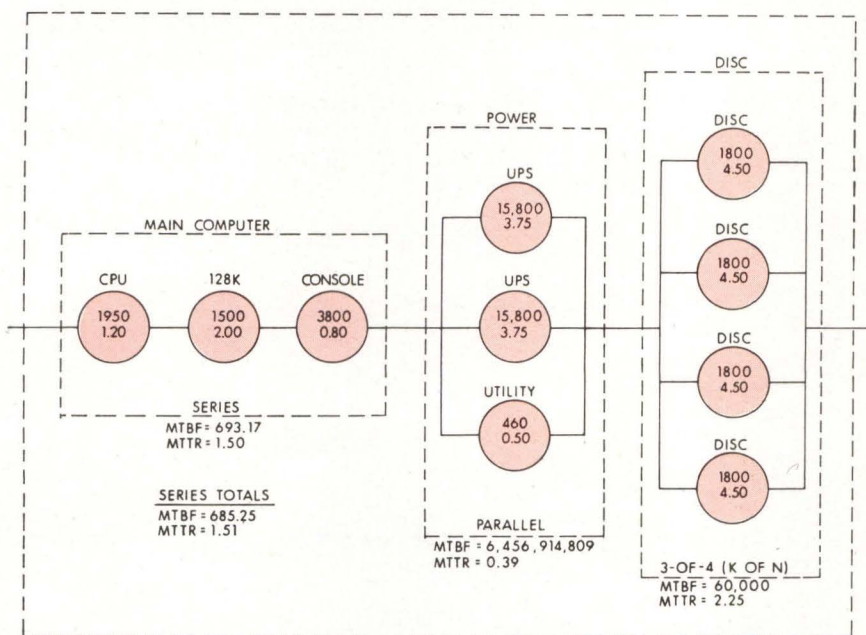


Fig 1 Reliability diagram for computer system configuration. Processor, memory, console, minimum of one power source, and at least three of four available discs are required for operational system. Top number within each circle is element MTBF, bottom number is MTRR

of N elements available). For example, in the reliability diagram shown in Fig 1, the processor (CPU), memory (128k), and operator's console are tied in series; if any one of these three elements fails, the entire computer system goes down. Next, two uninterruptible power supplies (UPS) and utility company lines are connected in parallel, indicating that only one of these three sources is necessary to energize the system. Finally, the disc subsystem is operational if any three of four available discs work. As indicated by the outermost dashed lines in Fig 1, the three subsystems are strung in series to calculate total computer system reliability.

To evaluate this total computer system, calculate dependability in successive stages (initially components, next first-level subsystems, then larger subsystems), building on each set of results until the entire installation is encompassed. Primary elements in Fig 1 are grouped by shorter dashed lines into three first-level subsystems: main computer, power, and disc. Intermediate MTBF and MTRR results for these three subsystems are used to compute the MTBF and MTRR for the total computer installation. Most computer configurations can be translated easily and directly into a hierarchy of series, parallel, and K of N network models.

Series Configurations

The statistical likelihood of series elements in a string being operational is calculated by multiplying together the probability of finding each element working. Thus, the overall long-term availability (A) of a series string of repairable components is the product of their individual availabilities:

$$A_s = A_1 \times A_2 \dots \times A_n \quad (1)$$

The reliability analysis calculator program multiplies availabilities and assumes that defective modules in a computer installation are either repairable or replaceable. This algorithm cannot be applied to nonrepairable subsystems because their long-term availabilities are zero.

The series formula for total subsystem MTBF is analogous to the equation for evaluating a circuit of parallel resistors; combined resistance is always less than the value of any one parallel resistor. Similarly, total MTBF in a series reliability diagram is always lower than the MTBF of its least reliable element. The inverse of series subsystem MTBF can be calculated by adding together the inverses of individual element MTBFs:

**Instructions for Running Reliability Analysis
Program on TI-59 Calculator**

Step	Procedure	Enter	Press	Display
S.0	Series Configuration		START (A')	1.
S.1	Enter MTBF and MTTR for each series element	Element MTBF	MTBF _s (A)	Cumulative subsystem MTBF
S.2	Repeat steps S.1 and S.2 for each series element. Cumulative result is displayed after each entry. After each element is added, you can interrupt loop and compute the following:	Element MTTR	MTTR _s (B)	Cumulative subsystem MTTR
S.3	Availability		A (C')	Availability
S.4	Reliability	Time period t	R(t) (D')	Reliability
S.5	Probability of n failures. Reliability must be calculated first.	n	P(n) (E')	Probability of n failures
SS.0	Series Configuration for calculation of MTBF only.		START (A')	1.
SS.1	Enter MTBF for each series element. Repeat step SS.1 for each element. Cumulative result is displayed after each entry. After each MTBF is entered, you can compute the following:	Element MTBF	MTBF _s (A)	Cumulative subsystem MTBF
SS.2	Reliability	Time period t	R(t) (D')	Reliability
SS.3	Probability of n failures. Reliability must be calculated first.	n	P(n) (E')	Probability of n failures
P.0	Parallel Configuration		START (A')	1.

$1/MTBF_s = 1/MTBF_1 + 1/MTBF_2 \dots + 1/MTBF_n$. (2)
This calculation holds for both repairable and non-repairable subsystems. The subscript s is used to denote subsystem values.

Another way of explaining Eq (2) is that the total failure rate ($1/MTBF_s$) is the sum of the failure rates of its series constituent elements. According to this concept, the MTBF of a series configuration, with two iden-

tical modules, has half the MTBF of one element. If a third identical component is added, series subsystem MTBF drops to one-third of the element MTBF; if more series modules are included, $MTBF_s$ falls proportionately.

For repairable subsystems, $MTBF_s$, $MTTR_s$, and A_s are mutually related by

$$A_s = MTBF_s / (MTBF_s + MTTR_s) \quad (3)$$

Step	Procedure	Enter	Press	Display
P.1	Enter MTTR and MTBF for each parallel element.	Element MTTR	MTTR _p (C)	Cumulative subsystem MTTR
P.2	Repeat steps P.1 and P.2 for each parallel element. Cumulative result is displayed after each entry. After each element is added, you can interrupt loop and compute the following:	Element MTBF	MTBF _p (D)	Cumulative subsystem MTBF
P.3	Availability		A (C')	Availability
P.4	Reliability	Time period t	R(t) (D')	Reliability
P.5	Probability of n failures. Reliability must be calculated first.	n	P(n) (E')	Probability of n failures
KN.0	K of N Configuration			
KN.1	Input number of elements required	K	K-of-N (E)	
KN.2	Input number of elements available	N	R/S	
KN.3	All elements are identical. Element MTTR and MTBF need to be input only once.	Element MTTR	R/S	Subsystem MTTR
KN.4		Element MTBF	R/S	Subsystem MTBF
KN.5	Availability		A (C')	Availability
KN.6	Reliability	Time period t	R(t) (D')	Reliability
KN.7	Probability of n failures. Reliability must be calculated first.	n	P(n) (E')	Probability of n failures

Note: "Press" column lists describing mnemonic, written on calculator mag program card. Actual calculator keystrokes shown in parentheses

After any two of these parameters have been determined, this equation can be used to solve for the remaining unknown; the equation, solving for $MTTR_s$ in terms of A_s and $MTBF_s$, is

$$MTTR_s = \frac{(1 - A_s)}{A_s} MTBF_s \quad (4)$$

For all series networks, repairable or not, total reli-

ability is the product of the reliabilities of each of the individual elements:

$$R_s = R_1 \times R_2 \dots \times R_n \quad (5)$$

The reliability analysis calculator program first solves for $MTBF_s$, and then uses the following equation:

$$R_s = e^{-t/MTBF_s} \quad (6)$$

RELIABILITY ANALYSIS

* SERIES MODEL -

UNIT- 1950.00 MTBF
 SUBSYSTEM- 1950.00 MTBF
 UNIT- 1.20 MTTR
 SUBSYSTEM- 1.20 MTTR

UNIT- 1500.00 MTBF
 SUBSYSTEM- 847.83 MTBF
 UNIT- 2.00 MTTR
 SUBSYSTEM- 1.65 MTTR

UNIT- 3800.00 MTBF
 SUBSYSTEM- 693.17 MTBF
 UNIT- 0.80 MTTR
 SUBSYSTEM- 1.50 MTTR

▲ AVAILABILITY = .9978441824

▲ RELIABILITY IN 2080.00 HRS= .0497521423

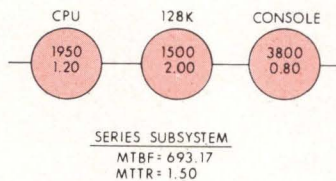


Fig 2 Three primary elements connected in series. Failure of only one element brings down entire subsystem. Series connection is always less reliable than its weakest link, in this case main storage (128k)

RELIABILITY ANALYSIS

* SERIES MODEL -

UNIT- 693.17 MTBF
 SUBSYSTEM- 693.17 MTBF
 UNIT- 1.50 MTTR
 SUBSYSTEM- 1.50 MTTR

UNIT- 6456914809. MTBF
 SUBSYSTEM- 693.17 MTBF
 UNIT- 0.39 MTTR
 SUBSYSTEM- 1.50 MTTR

UNIT- 60000.00 MTBF
 SUBSYSTEM- 685.25 MTBF
 UNIT- 2.25 MTTR
 SUBSYSTEM- 1.51 MTTR

▲ AVAILABILITY = .9978032837

▲ RELIABILITY IN 2080.00 HRS= .0480566918

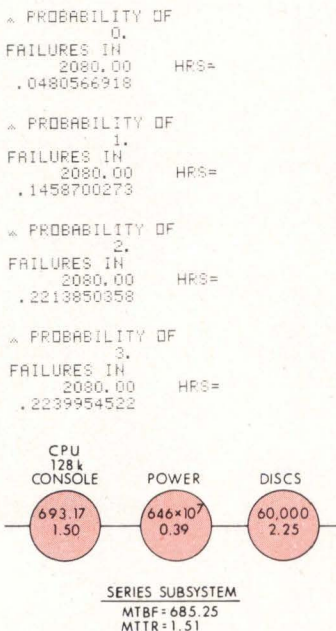


Fig 3 Series model for calculating dependability of entire computer system. Total system dependability is determined by joining first-level subsystems in series. MTBF and MTTR results from Figs 2, 4, and 5 are shown in reliability circles. MTBF for power and disc subsystems is already high, so further improvements in total system dependability would require adding backup processors, memories, and/or consoles

to determine series reliability; however, results are the same as if element reliabilities had been multiplied.

Series Calculations

To compute reliability or failure probability, the MTBF of at least one element needs to be input; however, both MTBF and MTTR are needed for availability. Pressing calculator key C' displays availability. Reliability, R(t), is the probability of successful uninterrupted operation without any failure(s) over a given time span (t). Calculate reliability by entering the time period, in the same units used for MTBF and MTTR (usually in hours); pressing key D' displays reliability. Multiply by 100 to convert to percent. The probability of any number of failures occurring during time interval t, P(n), is computed by entering the number of failures, n, and pressing key E'. This failure probability parameter is an expansion of reliability, the probability of zero failures; therefore, an alternate method of calculating reliability is to key in zero followed by E'. The time period over which failure probabilities are calculated is the same period used for reliability. Make certain to calculate, or recalculate, reliability over that desired time span first.

On the TI-59, press the A' key to initiate either series or parallel calculations. For the series model, enter the MTBF of the first element, then press key A. Enter its MTTR, and press key B. Repeat this sequence for every element in the series connection as follows: A', MTBF₁, A, MTTR₁, B, MTBF₂, A, MTTR₂, B, . . . , MTBF_n, A, MTTR_n, B. A cumulative MTBF is displayed each time key A is pressed, and a cumulative MTTR is displayed each time B is pressed, so that the effect of adding each series element is immediately apparent. This cyclic entry process can be interrupted after each element is entered to compute availability (key C'), reliability (key D'), or failure probability (key E') of the series components included thus far (see Instructions, Steps S.0 to S.5).

Sometimes, only failure rates are provided for the individual elements in a series connection. In such cases, the problem becomes one of determining the failure rate, or alternatively the MTBF of the whole series string. Initialize the model by pressing key A'. Since MTBF (h/failure) is the inverse of failure rate (failures/h), enter the failure rate for the first element; then press calculator keys 1/x and A. Repeat this process for each series element. Given element failure rates, the keystroke sequence is: A', failure rate₁, 1/x, A, failure rate₂, 1/x, A, . . . , failure rate_n, 1/x, A. Alternatively, if given element MTBFs, the keystroke sequence is: A', MTBF₁, A, MTBF₂, A, . . . , MTBF_n, A. The MTBF for the string of accumulated elements will be displayed each time key A is pressed; to convert this MTBF to its equivalent failure rate, press key 1/x. This entry process can also be interrupted to calculate both reliability and failure probability for the string of series elements thus far accumulated (see

Instructions, Steps SS.0 to SS.3). Availability calculations, however, require MTTR and therefore can only be accomplished as described in the preceding paragraph.

Figs 2 and 3 illustrate the use of the calculator program in computing dependability parameters for series configurations. In Fig 2, three primary elements (CPU, 128k memory, and console) are connected in series and their MTBF and MTTR values are entered consecutively. As each element value is entered, subsystem MTBF and MTTR values are immediately calculated. When the CPU is input, it is the first and only element included in the series subsystem; subsystem MTBF and MTTR are the same as that for the CPU. After the 128k memory is also incorporated, subsystem MTBF is reduced to only 847.83 h, and subsystem MTTR equals 1.65 h. MTBF_s falls even lower, to 693.17 h when the console value is added. Series elements can be configured and input in any order, but final results will always be the same. After each element is entered, the computer designer can temporarily suspend further input to solve for availability (key C'), reliability (key D'), and/or failure probabilities (key E') of the interim subsystem.

Fig 3 indicates the use of the series model in calculating the dependability of an entire computer installation. Three first-level subsystems, whose MTBFs and MTTRs have been calculated in Figs 2, 4, and 5, are the series elements. By studying MTBF values, the experienced computer designer can estimate the final overall MTBF. The first subsystem is the limiting resource because it has the lowest MTBF, 693.17 h; power and disc subsystems have MTBF values many times greater, 6,456,914,809 h and 60,000 h, respectively. The total MTBF of a series connection is less than the MTBF of any of its elements, and the reliability analysis program confirms this by predicting a total MTBF_s for the overall computer installation of 685.25 h.

Fig 3 also shows failure probability calculations. The arbitrarily chosen 2080-h time period could represent either 2080 nonstop hours, 260 8-h days, 130 online 16-h days, etc. The probability of zero failures produces the same result as reliability, 4.81%, because they both have the same definition. According to the printout, the probability of 1 failure occurring in 2080 h is 14.59%, the probability of 2 failures is 22.14%, the probability of 3 failures is 22.40%, etc.

Parallel Configurations

The inherent redundancy of a parallel configuration, where only one element needs to be working, enhances reliability. Parallel networks whose defective elements can be repaired or replaced are the most desirable, and are many times more reliable than a nonrepairable parallel configuration, which ceases to operate when each of its elements has experienced only one failure. Since most computer installations fall into the repairable

RELIABILITY ANALYSIS

* PARALLEL MODEL -

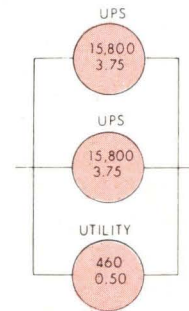
UNIT- 3.75 MTTR
SUBSYSTEM- 3.75 MTTR
UNIT- 15800.00 MTBF
SUBSYSTEM- 15800.00 MTBF

UNIT- 3.75 MTTR
SUBSYSTEM- 1.88 MTTR
UNIT- 15800.00 MTBF
SUBSYSTEM- 33301133.17 MTBF

UNIT- 0.50 MTTR
SUBSYSTEM- 0.39 MTTR
UNIT- 460.00 MTBF
SUBSYSTEM- 6456914809.00 MTBF

△ AVAILABILITY = .9999999999

△ RELIABILITY IN 2080.00 HRS = .9999996779



PARALLEL SUBSYSTEM
MTBF = 6,456,914,809
MTTR = 0.39

Fig 4 Paralleling elements increases reliability. Parallel subsystem works as long as any one of its constituent elements operates. This computer system is usually energized by one of its redundant uninterruptible power supplies. Should both these power sources fail, bypass transfer switch connects ac bus to normal utility company voltage

* ANY K-OF-N MODEL -
ND. UNITS REQUIRED = 3.
ND. UNITS AVAILABLE = 4.

UNIT- 4.50 MTTR
SUBSYSTEM- 2.25 MTTR
UNIT- 1800.00 MTBF
SUBSYSTEM- 60000.00 MTBF

△ AVAILABILITY = .9999625014

△ RELIABILITY IN 2080.00 HRS = .9659273384

△ PROBABILITY OF 1. FAILURES IN 2080.00 HRS = .0334854811



3 OF 4 SUBSYSTEM
MTBF = 60,000.
MTTR = 2.25

Fig 5 3-of-4 disc subsystem. Working combination of any three discs (K=3) suffices for this four-disc (N=4) subsystem to be operational. The K of N model, K elements required of N elements available, is restricted to situations where all elements have identical MTBF and MTTR values. Reliability diagrams of data storage peripherals should indicate any dependency on specific files as well as on raw hardware storage capacity. If different file is stored on each of four discs, and realtime system needs to access all of these files, proper representation would be either 4-of-4 or series model

category, paralleling key modules is a technique commonly used to significantly upgrade system reliability. The strategy for evaluating dependability parameters in repairable systems is to initially determine A_s and $MTTR_s$. Unavailability is defined as percent availability subtracted from 100%. The model calculates the unavailability of each parallel element by subtracting its availability from one:

$$U_1 = 1 - A_1, U_2 = 1 - A_2, \dots, U_n = 1 - A_n \quad (7)$$

Repairable subsystem unavailability (U_s) is the product of all element unavailabilities. The model multiplies the unavailabilities of the parallel elements together and determines unavailability for the entire parallel subsystem:

$$U_s = U_1 \times U_2 \dots \times U_n \quad (8)$$

Subtracting U_s from 1 reconverts back to parallel subsystem availability:

$$A_s = 1 - U_s \quad (9)$$

Parallel subsystem $MTTR_s$ is calculated with the same equation used in the series configuration for $MTBF_s$; just replace each $MTBF$ that appeared in the equation by its corresponding $MTTR$:

$$1/MTTR_s = 1/MTTR_1 + 1/MTTR_2 \dots + 1/MTTR_n \quad (10)$$

Consider two parallel elements, each with an $MTTR$ of one hour. If one of these elements fails, the parallel subsystem continues to operate. Total parallel outages are unlikely and will occur only if the second module simultaneously fails sometime during the 1-h downtime of the first element. The probability of the second element failing is approximately uniform over this 1-h downtime, and it will occur, on average, after 0.5 h has transpired. Repair of the first unit will, on average, be accomplished in another 0.5 h; therefore, overall parallel subsystem $MTTR_s$ is 0.5 h. Both the equation for $MTTR_s$ and this intuitive line of reasoning lead to the same result. If a third element, with the same $MTTR$ as the other two is added in parallel, only a simultaneous triple failure could bring down the parallel subsystem; in this case, $MTTR_s$ would be 0.333 h.

After solving for A_s and $MTTR_s$, the general equation for availability, with its terms rearranged, is used to determine parallel subsystem $MTBF_s$:

$$MTBF_s = (MTTR_s) (A_s) / (1 - A_s) \quad (11)$$

The above equations for repairable parallel networks have been implemented in the reliability analysis calculator program. They apply only to systems where repair or replacement of malfunctioning parts is feasible. These equations will not work for nonrepairable configurations because long-term availability is zero and $MTTR_s$ are not definable.

However, it is still possible to approximate $MTBF_s$ and R_s for nonrepairable parallel subsystems. Beginning with reliability, the approach is the same as that used

for availability. Define unreliability as reliability subtracted from 100%. Calculate the unreliability of each parallel element by subtracting its reliability from 1. Nonrepairable subsystem unreliability is the product of all element unreliabilities. Multiply the unreliabilities of the parallel elements together to compute the unreliability of the entire parallel subsystem. Subtract subsystem unreliability from 100% to reconvert it to parallel subsystem reliability, R_s . The equation for this process is

$$R_s = 1 - [(1 - e^{-t/MTBF_1}) \times (1 - e^{-t/MTBF_2}) \times \dots \times (1 - e^{-t/MTBF_n})] \quad (12)$$

After R_s is known, the second step is to find parallel subsystem $MTBF_s$. The relationship between $MTBF_s$ and R_s is expressed by Eq (6). Solving for $MTBF_s$ yields

$$MTBF_s = -t / (\ln R_s) \quad (13)$$

where \ln denotes the natural logarithm.

Parallel Calculations

These are handled similarly to the series procedure. The main modification is that an element's $MTTR$ value is entered before its corresponding $MTBF$. Key in the element $MTTR$, and then press key C. Next, enter the corresponding $MTBF$, and press key D. Continue this cycle until all parallel elements have been included, for example, A', $MTTR_1$, C, $MTBF_1$, D, $MTTR_2$, C, $MTBF_2$, D, . . . , $MTTR_n$, C, $MTBF_n$, D. Each time key C is pressed, the cumulative $MTTR$ for the elements included thus far is displayed. After pressing D, the cumulative $MTBF$ is displayed. As for series connections, the parallel entry process can also be interrupted after each element is input to calculate subsystem availability (key C'), reliability (key D'), or failure probability (key E'') (see Instructions, Steps P.0 to P.5).

For comparison, consider two parallel elements, each of which has an $MTBF$ of 100 h and an $MTTR$ of 1 h. If these elements are repairable, their parallel configuration has an $MTBF_s$ of 5100 h and an $R_s(2080)$ of 66.51%, according to the calculator program. If two nonrepairable elements, each with a 100-h $MTBF$, are connected in parallel, total subsystem $MTBF_s$ is no more than several hundred h, and reliability, $R(2080)$, is smaller than 1%. $MTBF_s$ can only be approximated for nonrepairable configurations because the precision of calculations is sensitive to the reliability time period chosen. Nevertheless, the difference in reliability levels is dramatic, going from 66.51% probability of no failures in 2080 h to almost certain failure.

Fig 4 shows three power sources in parallel. Running the model indicates the effect of increasing redundancy. Paralleling two UPS supplies, without a static bypass transfer switch, gives an $MTBF_s$ of 33,301,133.17 h, an $MTTR$ of 1.88 h (half the UPS $MTTR$ of 3.75 h), and a five-year reliability $R_s(43800)$ of 99.869%. Adding a static bypass transfer switch to connect the computer

to utility power in the event of UPS failures increases the MTBF_s by several orders of magnitude and the reliability R_s(43800) to 99.999%. Even this small 0.130% increase in reliability is significant for a critical application. If computer workload and turnaround time are paramount, the cost of replicated hardware may be justified by comparison to lost operation and revenue should potential downtime occur.

K of N Configurations

A K of N network connection frequently encountered in computer systems is a grouping of N elements, of which K elements must be working. When K is equal to 1, only one of the elements is needed to sustain subsystem operation, the equivalent of a parallel configuration. If all N elements are essential (K equals N), the group is actually a series network. Equations for calculating MTTR_s and MTBF_s for general K of N repairable configurations are

$$MTTR_s = \frac{MTTR_1}{N-K+1} \quad (14)$$

$$MTBF_s = MTBF_1 \left[\frac{MTBF_1}{MTTR_1} \right]^{(N-K)} \times \frac{(N-K)! (K-1)!}{N!} \quad (15)$$

These two equations have been coded into the reliability analysis calculator program. The K of N equations assume that all elements have the same MTBF and MTTR values. General availability Eq (3) is used to solve for A_s in terms of MTTR_s and MTBF_s.

K of N Calculations

The K of N model requires no initialization; follow the keystroke sequence given in the Table, Steps KN.0 to KN.7. Input an integer value for K and press key E; then, enter N and press the run/stop key, R/S. Input element MTTR, press R/S, and the MTTR of the total subsystem is displayed. Similarly, enter element MTBF, press R/S, and the display shows total subsystem MTBF. Subsystem MTBF and MTTR values are automatically stored in registers, so that they will not have to be reentered for further availability (key C'), reliability (key D'), and failure probability (key E') calculations.

A reliability diagram for a 3-required-of-4 available disc subsystem is depicted in Fig 5. The accompanying printout indicates the order in which input parameters are entered: K, N, element MTTR, and element MTBF. After element MTTR is keyed in, the program halts, displaying a subsystem MTTR_s of 2.25 h in this case. Similarly, when element MTBF is input, the program displays an MTBF_s of 60,000 h. Availability (key C') and reliability in 2080 h (key D') are also shown 99.99625014% and 96.59273384% respectively.

K of N dependability parameters, when elements are not alike, are complex and difficult to calculate. There are also configurations, especially in systems having

dual sets of data storage devices and redundant files, for which there is no method by which hardware interdependencies can be represented with absolute accuracy on a reliability diagram. In these situations, it is usually best to work up two sets of simple calculations, one optimistic and the other pessimistic. Such a sensitivity analysis provides reliability bounds and indicates whether a more detailed study would prove worthwhile. The bibliography listed in the Appendix explores this subject further. Reliability and MTBF can also be evaluated for K of N subsystems containing elements that cannot be repaired, as also described in the Appendix.*

Summary

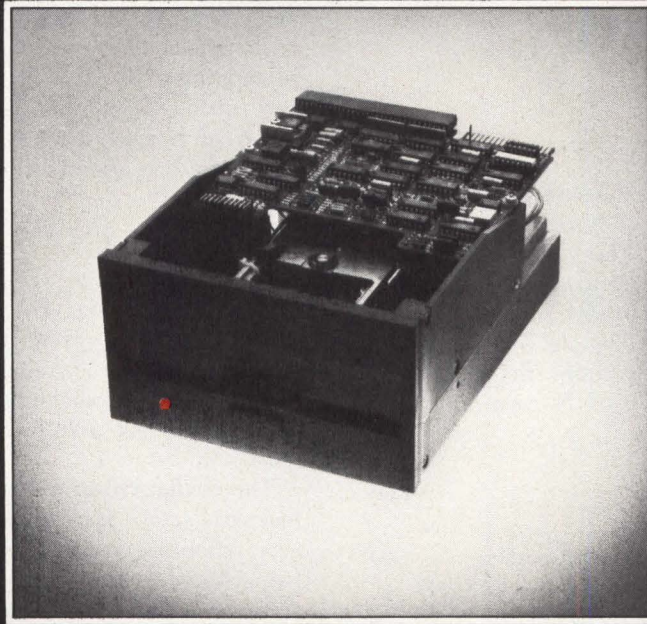
This article presents the equations, code, and user instructions for a TI-59 calculator program that can estimate the overall reliability of a computer installation, identify specific subsystems most prone to failure, and show where additional redundancy would help the most.

The configuration design objective is to reach a specified satisfactory level of reliability at minimum cost. Excess reliability wastes dollars while excessive downtime jeopardizes operation and results in costly failures. This software tool predicts computer installation reliability and determines the level and elements at which replication efforts should be directed. The reliability analysis calculator program is easy to use and it addresses issues at a level of detail that makes efficient use of the computer designer's time. It permits interactive analysis with a response time of seconds, which allows the investigation of many prospective reconfigurations. Reliability alternatives, along with their cost tradeoffs, can then be explored for factual appraisal and decision making based on quantitative results.



Ronald Zussman is a senior consultant and project leader of computer performance measurement and evaluation at SIAC. His past experience includes benchmarking, optimization, and modeling of Navy and Stock Exchange computer systems. He has earned a BSEE degree from Pratt Institute, an MSEE degree from New York University, and a professional EE degree from Columbia University.

*The appendix to this article contains a discussion of types of computer system failures, simplifying modeling assumptions made in deriving reliability equations, a list of pertinent equations, detailed instructions for programming the TI-59 calculator, code for the SR-52 calculator, an illustrative trouble report, and an extensive bibliography. Interested readers may obtain a copy of this appendix by writing to: The Editor, *Computer Design*, 11 Goldsmith St, Littleton, MA 01460.



Simply Better.

Our MPI 52 two-headed micro floppy drive has speed, accuracy, capacity, and simplicity. It's better than any other drive. Better because it's faster. Five times faster than the next best. Our exclusive band-positioning design ensures track to track access time of 5 milliseconds.

Better because it's bigger. 437.5K bytes per double density disk, unformatted.

And simply better because it's reliable. The MPI 52 has 1½% speed control, no mechanical switches, and comes fully burned in. There are only 10 moving parts, including our front door diskette ejector mechanism.

Order your industry-compatible MPI floppy disc drive. It's the drive for success.



MICRO PERIPHERALS INC.

21201 Oxnard Street
Woodland Hills, California 91367
(213) 999-1353

COMPARISON OF SELECTED ARRAY PROCESSOR ARCHITECTURES

Examination of synchronous parallel pipelined and asynchronous parallel array processor architectures points out differing hardware/software concepts, memory utilization, input/output flexibility, and processing capabilities

Stephen P. Hufnagel The University of Texas, Austin, Texas

Large general purpose mainframe computers, while capable of very high throughput rates, are too expensive for performing dedicated scientific computations. Although lower in cost, minicomputers have limiting processing speeds for handling repetitive numerically intensive calculations. Consequently, requirements for cost-effective solutions of iterative arithmetic on large arrays of data have led to the design and development of the add-on programmable array processor. In conjunction with a frontend host minicomputer, the array processor provides substantially increased throughput, precision, and dynamic range, under program control, for accommodating a wide range of digital signal processing applications. These applications, such as radar or sonar detection, speech analysis, data reduction, and image enhancement, usually involve exacting solutions of a defined set of problems, employing either fast Fourier transform, matrix operation, correlation, or convolution algorithms.

Combining an array processor with a host minicomputer allows each to perform individually and optimally. The host provides overall system control, directing the flow of data and instructions between input/output (I/O) peripherals and the array processor. High speed complex calculations are executed by the array processor, more than 100 times faster than the host could perform them.

For effective interface with a host minicomputer, an array processor should encompass (a) several specialized processors functioning in parallel, (b) floating point data format, (c) programmability, and (d) direct connections to external devices. The latter significantly reduces activity in host memory since only processed results are stored there. Software adaptability allows program deletions, changes, or modifications to existing algorithms, and enables new routines to meet altered application requirements. Rounding hardware in the floating point arithmetic units, compatible with fixed point formats, promotes improved accuracy. Multiple, parallel processors, under effective control, yield high speed operation.

Comparison of the architectural design of two programmable array processors reveals capabilities associated with each. Both processors perform high speed, floating point calculations as an attached peripheral device to a host minicomputer at an estimated processing rate exceeding 10M instructions/s. Unit A is the Floating Point Systems AP-120B; this unit is a synchronous, parallel pipelined, horizontally microprogrammable machine with a 167-ns cycle time, a 38-bit floating point format, a 64-bit program control word, 64 floating point accumulators, and 16 integer index registers. Unit B is the CSP MAP-300; this unit is an asynchronous, parallel, vertically microprogrammable

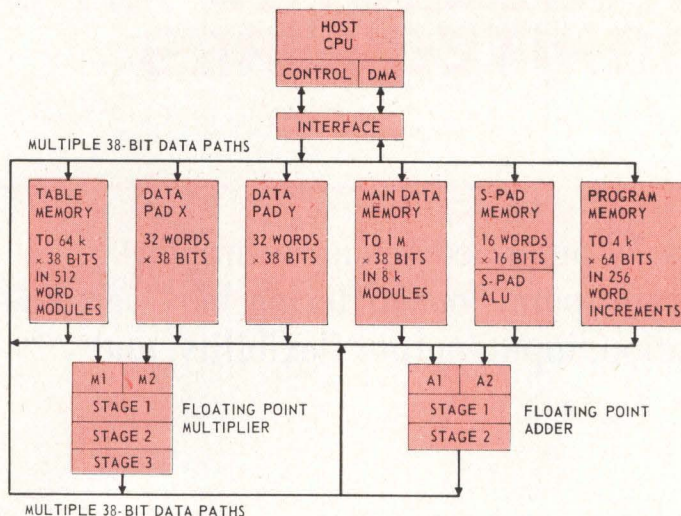


Fig 1 AP-120B array processor (unit A). Synchronous, parallel pipelined, horizontally microprogrammable machine has separate input bus and output bus for each floating point arithmetic element to any other element of system. Parallel multibus architecture allows flexibility in that multiple operands and resultants can be moved simultaneously from element to element

machine with a 70-ns cycle time, a 32-bit floating point format, a 16-bit program control word, 32 floating point accumulators, 8 integer index registers, and 3 parallel interprocessor memory buses.

Synchronous Parallel Pipelined Architecture

Significant design modules and the interconnecting data flow bus structure of unit A are shown in Fig 1. The host computer, which is typically a 16-bit minicomputer, serves the functions of program loading, I/O device setup and sequencing, possible data source, and possible pre- and/or post-data processor for unit A. This host is mandatory since unit A has only a primitive I/O capability to set up a direct memory access (DMA) transfer and to determine whether the transfer has been completed.

No interrupt handling hardware is available. An interface routes and directly ties the host computer to multiple 38-bit data paths. These paths transfer data between remaining blocks in the diagram. Any block is able to send data to, or receive data from, any other block with the exception of S-pad memory and S-pad arithmetic logic unit (ALU). S-pad memory performs integer address indexing and loop counting, and contains sixteen 16-bit directly addressable registers. The contents of these registers are modified to provide address routing registers for table memory, data pad X and data pad Y registers, and main data memory.

The floating point adder is a 2-stage pipeline adder with two buffer registers at the input. This pipeline design yields an effective floating point add rate that is equivalent to the 167-ns cycle time of the array processor, once the pipeline is full. Alternately, two cycles are required for the result of a particular add

to pass through the pipeline before the sum is usable in any further calculation.

A 3-stage pipeline, the floating point multiplier has two buffer input registers and must sequence through three stages before a particular result is available. Like the floating point adder, the effective floating point multiply time is one machine cycle time of 167 ns.

Two independently addressable banks of 32 floating point registers comprise data pad X and data pad Y. Each word is 38 bits long, and any register can be accessed in a single machine cycle. Additionally, a simultaneous read and write is possible within each data pad during the same machine cycle. This parallel register load and store operation allows storage of adder or multiplier results, or of data obtained from memory in the register, and fetching of new register data for input to adder, multiplier, or memory to occur simultaneously.

Control of unit A is achieved by 10 parallel opcode fields contained in the 64-bit program control word (Fig 2). All memory accesses, register transfers, and computations occur synchronously and in parallel. This sequencing allows for the simultaneous execution of the floating point adder, floating point multiplier, a fetch or store from data memory, two reads and two stores of accumulators, a conditional branch test, a fetch from table memory, and index register integer arithmetic to facilitate data memory, table memory, and register addressing.

Program memory has a 64-bit wide word and a 50-ns cycle time to support the processor. For any type of complex logical operations in memory, register address decoding, demultiplexing, or for any conditional logic based upon the data themselves, efficiency of this machine approaches that of a serial microencoded machine. The pipeline design of the adder and multiplier further diminishes the machine's efficiency when logical operations are based on the data themselves. Before a test

the tradeoffs required to provide bulk storage at a reduced cost.

Two types of data memory are available. They both have a 38-bit word size and are constructed of MOS integrated circuits. Data memory is addressable to 1M words with either 167- or 333-ns interleaved cycle time. An obvious tradeoff between processing requirements and cost can be made between the two memory speeds. In complex iterative algorithms, the two high speed 32-word data pad registers should prove adequate to prevent the slower memory cycle time from becoming a limiting factor in processing ability.

Table memory consists of 38-bit word, 167-ns cycle time bipolar ROM or RAM, in 512-word increments, addressable to 64k words. Table memory is used as constant storage and, for a fixed algorithm application, low cost ROM is adequate. Additional flexibility is obtained by using either a mixture of ROM and RAM table memory or high cost RAM table memory only.

The I/O system for unit A is a 3M, 38-bit word/s, direct memory access (DMA) common bus to either program or data memory. All inputs and outputs are on a memory cycle steal basis, and up to 256 devices are addressable.

Under program control, unit A is able to load program memory with an alternate program code pro-

vided by the host computer. This capability helps compensate for the limited size of this memory in applications where programs can be partitioned into independent sets of code and where the sequence of events allows sufficient time to replace code in program memory.

Data memory is also updated by DMA transfer. One limitation of this approach is the necessary cycle-steal sequence, which will stop all processing in the array processor for one memory cycle if a memory reference is being made simultaneously with the input or output transfer of a peripheral device or the host computer.

In summary, the architecture of unit A is designed to speed up data processing limitations of the traditional computer ALU by a synchronous parallelism of operations. This parallel multibus architecture provides high processing speed because multiple operations can be performed and resultants can be moved simultaneously between elements. The synchronous approach provides total predictability of data flow and timing considerations, which simplifies programming. However, the parallelism of operation and the pipeline multiplier and adder lose much of their speed advantage in an algorithm requiring logical decisions based upon data value. In addition, logical operations require inefficient use of expensive program memory.

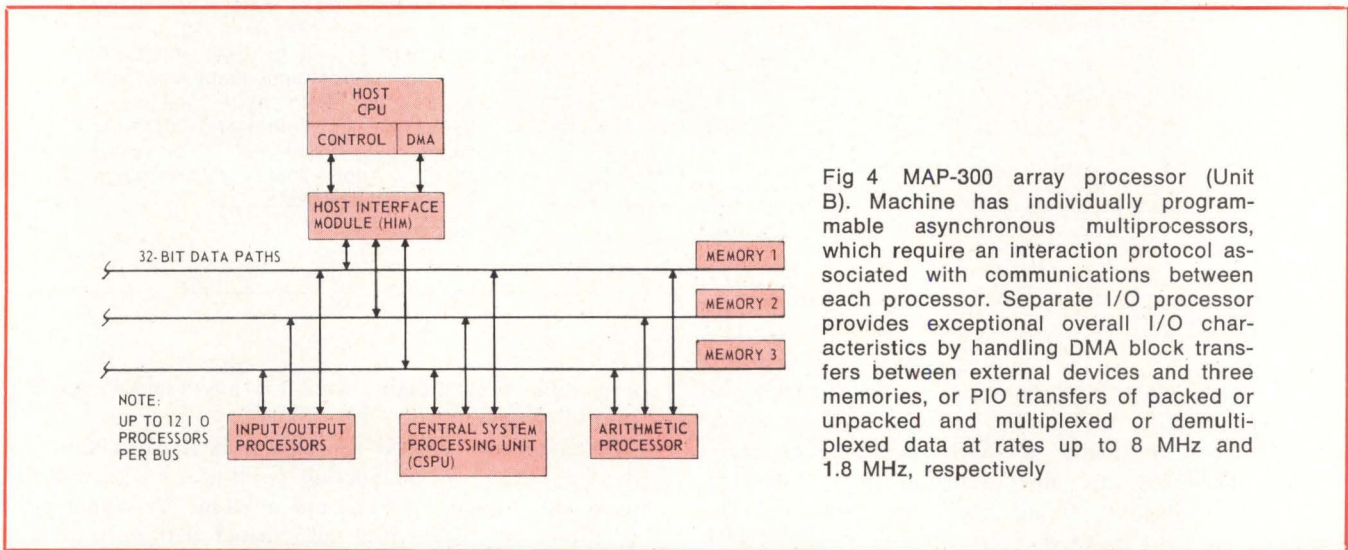


Fig 4 MAP-300 array processor (Unit B). Machine has individually programmable asynchronous multiprocessors, which require an interaction protocol associated with communications between each processor. Separate I/O processor provides exceptional overall I/O characteristics by handling DMA block transfers between external devices and three memories, or PIO transfers of packed or unpacked and multiplexed or demultiplexed data at rates up to 8 MHz and 1.8 MHz, respectively

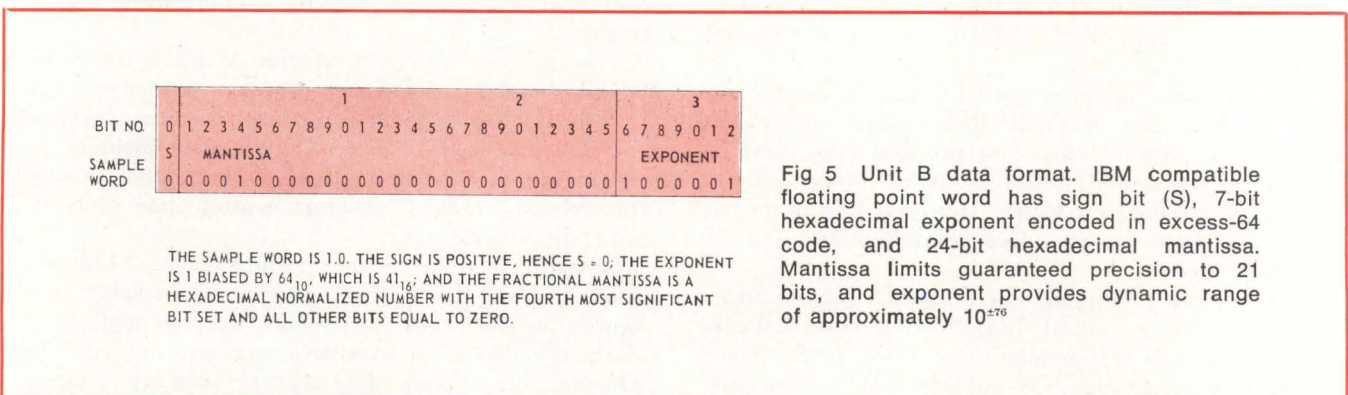


Fig 5 Unit B data format. IBM compatible floating point word has sign bit (S), 7-bit hexadecimal exponent encoded in excess-64 code, and 24-bit hexadecimal mantissa. Mantissa limits guaranteed precision to 21 bits, and exponent provides dynamic range of approximately $10^{\pm 70}$

Asynchronous Parallel Architecture

Control of unit B is achieved by an individually programmable asynchronous multiprocessor design requiring an interaction protocol (handshaking) associated with communications between each microprocessor. Unit B consists of the central system processor unit (CSPU), arithmetic processor, memories, host interface, and I/O processors (see Fig 4).

The data format selected for unit B (see Fig 5) is an IBM floating point format, which consists of a 7-bit hexadecimal exponent, a 24-bit hexadecimal mantissa, and a sign bit. However, a normalized hexadecimal positive number can still have as many as three leading zeros, which results in reduced precision of the data format over a binary format of equivalent size.

Serving as executive processor in the multiprocessor system, the CSPU communicates with each individual processor through three common memory buses and through a programmable priority interrupt system. The CSPU initiates processing sequences by entering needed programs into the arithmetic processor and the address controller of the arithmetic processor, and by starting operations as tasks become available from the host computer. It generally controls data flow in the system, including control of the I/O processors. The CSPU has

a 16-bit fixed point arithmetic unit with a 125-ns cycle time, an 8-register accumulator file, and a 192-level priority interrupt network.

The arithmetic processor can be divided into functional units whose operations are interdependent. A pair of arithmetic processing units is parallel programmed from 128 words by 32 bits of read/write memory. These two processors each have a floating point adder, a floating point multiplier, 16 floating point accumulators, and they share I/O first-in first-out (FIFO) queues (Fig 6).

These queues communicate to the three memory buses and are routed and addressed by the address queues provided by the independently programmable arithmetic address processor. The single operation field of the arithmetic control program word (Fig 7) allows for a sequential multiply, add, data transfer, conditional jump, or unconditional jump. Operations take from one to six subcycles, where a subcycle is defined as 70 ns, and the program sequencer allows parallel utilization of resources. A program step wait is generated if a resource is requested when the operation necessary to provide the resource is not completed.

The arithmetic address processor runs parallel to the arithmetic processor and has a repertoire of integer instructions to allow calculations of multiplex and

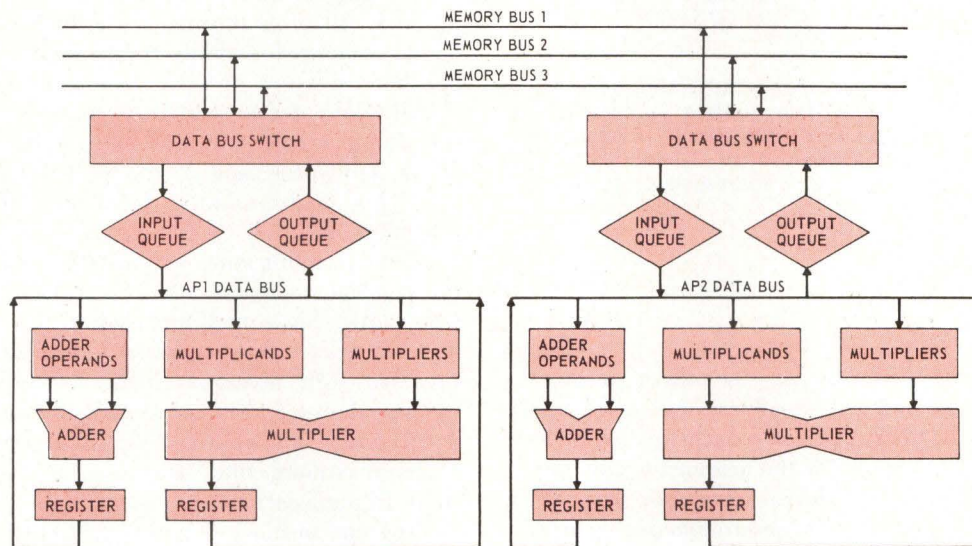
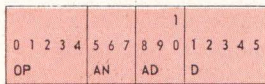
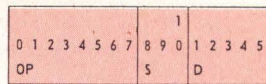


Fig 6 Dual arithmetic processor. Each processor has pair of independently programmed parallel adders and multipliers that feed through input and output queues to memory buses. Parallel asynchronous multiprocessor design increases overall speed, processing flexibility, and interprocessor control



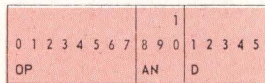
TWO ARGUMENT ADDER FORMAT

FIRST, THE CONTENTS OF THE RESULT (R) REGISTER IS MOVED TO THE DESTINATION REGISTER SPECIFIED BY D. THEN, AN ADD, SUB, MIN, MAX, MINABS, OR MAXABS BETWEEN THE CONTENTS OF THE REGISTERS SPECIFIED BY AN AND AD IS PERFORMED. THE RESULTS GO TO R.



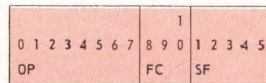
DATA TRANSFER FORMAT

THE CONTENT OF THE SOURCE REGISTER SPECIFIED BY THE S FIELD IS MOVED TO THE DESTINATION REGISTER SPECIFIED BY THE D FIELD. ALTERNATELY, A NO OPERATION (NOP) SPACE FILLER MAY BE DESIGNATED.



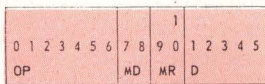
SINGLE ARGUMENT ADDER FORMAT

FIRST, THE CONTENT OF THE RESULT (R) REGISTER IS MOVED TO THE DESTINATION REGISTER SPECIFIED BY D. THEN, THE CONTENT OF THE REGISTER SPECIFIED BY AN IS LOADED, NEGATED, ABS VALUED, NORMALIZED, FIXED, ETC. THE RESULTS GO TO R.



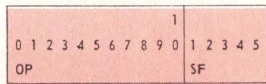
JUMP AND CALL FORMAT

FIRST, THE APU PROGRAM (CONDITIONALLY) JUMPS TO THE ADDRESS SPECIFIED BY THE NEXT 16-BIT WORD IN MEMORY; THEN, THE SPECIFIED SYSTEM FLAG (SF) IS SET ACCORDING TO A FLAG CHANGE CODE (FC). A CALL INSTRUCTION SAVES THE PROGRAM COUNTER



MULTIPLE FORMAT

FIRST, THE CONTENT OF THE PRODUCT (P) REGISTER IS MOVED TO THE DESTINATION REGISTER SPECIFIED BY D. THEN, THE ABS VALUE OR NEGATIVE OF THE CONTENTS OF THE REGISTER SPECIFIED BY MD IS MULTIPLIED BY THE CONTENTS OF THE REGISTER SPECIFIED BY MR. THE ABS VALUE OF THE PRODUCT GOES TO P.



CONTROL FORMAT

THE APU PROGRAM COUNTER IS RESET TO THE RETURN ADDRESS SAVED BY THE LAST CALL INSTRUCTION. THE SYSTEM FLAGS (SF) MAY BE OPTIONALLY SET OR CLEARED.

Fig 7 Arithmetic control program words. Two parallel 16-bit half-words comprise independent arithmetic units control in Unit B. Six possible half-word operation formats are possible

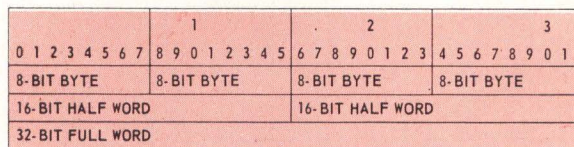


Fig 8 Versatile memory address ability. Unit B efficiently utilizes 32-bit main data storage supporting byte, half-word, and full-word addressing. Floating point numbers may be addressed as 32- or 16-bit words while integer numbers are addressed as 16- or 8-bit words

demultiplex address patterns for the three memory address buses. Input and output addresses are fed into separate FIFO queues that work in conjunction with the input and output data queues of the arithmetic processor sequencer. The arithmetic address processor has 128 words, each containing 25 bits of programmable memory that are writable by the CSPU.

Because of parallel arithmetic units, small program memory, and asynchronous address and processor I/O structures, complex logical decisions based upon data values would be inefficiently executed in this processor. Alternately, predetermined data multiplexing and demultiplexing are possible between the processor and memory as a result of the arithmetic address processor.

Unit B is capable of performing 4.75M multiplies/s plus 9.5M adds/s nested behind the multiplies. This

capability provides a maximum possible throughput of 14.25M floating point arithmetic calculations/s. Realistically, this criterion is not an attainable programming goal for normal applications.

The memory hierarchy of unit B entails use of 125-ns cycle time bipolar RAM and 500-ns cycle time MOS memory. All program memory is high speed RAM, while main memory for data storage and program storage can be a mixture of both RAM and MOS memory.

Main data storage and CSPU control program memory use 32-bit words that are addressable in 8-bit bytes, 16-bit half-words, and 32-bit full-word increments (Fig 8). This addressability facilitates efficient memory utilization.

Memory architecture is such that each of the three independent memory buses is capable of addressing 64k words. Since multiple memories may be employed and since each bus operates independently, each sub-processor can access a memory simultaneously on a cycle-steal basis, or can overlap input, output, and processing. This allows each subprocessor to perform at its maximum rate. Memories are multiported with up to 16 ports each.

Program memory for the arithmetic processor is a 128-word, 32-bit/word RAM. Each word is partitioned into half-words (Fig 9) to allow parallel control of the two multiplier and adder pairs that make up the arithmetic processor.

The arithmetic addresser section memory of the arithmetic processor has a 128-word, 25-bit/word RAM. Under direction of the CSPU, the arithmetic address section programs are loaded from main memory. The 32-bit words from main memory consist of a 7-bit address and a 25-bit instruction (Fig 10). The 7-bit

	1																2																3															
BIT NO.	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1																
INSTRUCTION																																																
INSTRUCTION TYPES																																																
	LOAD, ADDRESS INCREMENT, REGISTER ARITHMETIC AND CONTROL																																															
	ADDRESS																																															
	ABSOLUTE APS LOCATION																																															

LOAD INSTRUCTION: LOADS THE CONTENTS OF THE DESIGNATED OPERAND REGISTER WITH A SPECIFIED 17-BIT ABSOLUTE MAP MEMORY ADDRESS.

ADDRESS INCREMENT INSTRUCTION: ARITHMETICALLY COMBINES THE SPECIFIED INCREMENT WITH THE CONTENTS OF THE DESIGNATED OPERAND REGISTER.

REGISTER ARITHMETIC INSTRUCTION: ARITHMETICALLY COMBINES THE SPECIFIED INCREMENT WITH THE CONTENTS OF THE DESIGNATED OPERAND REGISTER.

CONTROL INSTRUCTIONS: A (CONDITIONAL) JUMP IS SPECIFIED.

Fig 9 Arithmetic processor program memory. Program memory of Unit B arithmetic processor is partitioned into half-words to allow parallel control of two multiplier and adder pairs

	1																2																3															
BIT NO.	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1																
INSTRUCTION	16-BIT HALF WORD																16-BIT HALF WORD																															
INSTRUCTION TYPES	SINGLE OR TWO ARGUMENT ADDER, MULTIPLY, DATA TRANSFER, JUMP AND CALL; AND CONTROL OF AP1.																																															
	SINGLE OR TWO ARGUMENT ADDER, MULTIPLY, DATA TRANSFER, JUMP AND CALL; AND CONTROL OF AP2.																																															

SINGLE ARGUMENT ADDER INSTRUCTION: PERFORMS ONE OF 13 ARITHMETIC OPERATIONS ON THE CONTENTS OF AN OPERAND REGISTER TO TAKE THE ABSOLUTE VALUE, APPROXIMATE RECIPROCAL, FLOATING POINT CONVERSION, ETC.

TWO ARGUMENT ADDER INSTRUCTION: PERFORMS ONE OF EIGHT OPERATIONS ON THE CONTENTS OF TWO OPERAND REGISTERS TO FORM THEIR SUM, DIFFERENCE, MAXIMUM, MINIMUM ABSOLUTE, ETC.

MULTIPLY INSTRUCTION: PERFORMS ONE OF FOUR VARIATIONS OF THE PRODUCT OF TWO OPERANDS.

DATA TRANSFER INSTRUCTION: MOVES THE CONTENTS OF ONE OF SIX SOURCE REGISTERS TO ONE OF 19 DESTINATION REGISTERS.

JUMP AND CALL INSTRUCTIONS: SPECIFY A (CONDITIONAL) JUMP WITHIN THE APU PROGRAM.

CONTROL OPERATIONS: INCLUDE RETURN JUMPS FROM SUBROUTINES AND INSTRUCTIONS TO CHANGE THE STATUS OF A SYSTEM FLAG.

Fig 10 Main memory addressing. Unit B control signal processing unit loads, from main memory, arithmetic addresser section (APS). Seven of 32 main memory bits designate memory location in APS, while remaining 25 bits are instruction bits

address specifies the location in arithmetic addresser memory where the instruction is to be loaded. The CSPU program resides in main memory. This program executes full-word (32-bit) and half-word (16-bit) instructions.

Host interface module (HIM) is the processor through which the unit B array processor and the host computer communicate. This module transfers blocks of data between the three memories and the host computer memory, converts data formats between the internal array processor format to or from that used by the host computer, and allows control information necessary to synchronize operations between the host computer and unit B. The HIM processor has a 32-word, 18-bit/word, programmable memory that is loaded by the CSPU.

The I/O processors are subprocessors that handle block transfers between external devices and the three memories in a programmed manner established by the CSPU. These I/O processors allow data transfers to occur without intervention of the host computer but under independently programmed control. A block transfer rate of 8 MHz is possible, while a programmed I/O (PIO) maximum rate of 1.8 MHz is feasible. All transfers are 8, 16, or 32 bits; parallel operation; and data may be packed or unpacked and multiplexed or demultiplexed on the fly in the PIO mode. Conversion

between integer and floating point formats is not possible in the I/O processor.

In summary, the architectural design of unit B uses an asynchronous parallel structure to speed up arithmetic operations. The parallel asynchronous microprocessor design increases speed by complex interprocessor control. This asynchronous approach eliminates predictability of data flow and state timing such that a complex protocol is required between processor elements. Programs are difficult to write and to debug. Complex logical decisions based upon data values are also difficult, although complex I/O multiplexing is handled efficiently. Program and data memories are used efficiently, which should reduce overall cost.

Conclusions

A simple deduction regarding the overall superiority of either of the described array processors is not practical. Both attempt to achieve the goal of being a high speed array processor, but each approaches this goal in a drastically different manner (see "Comparison of Major Array Processor Performance Characteristics").

A few descriptors are common between both array processors. Both require a host minicomputer to initially load programs and to perform any necessary setup

**Comparison of Major Array Processor
Performance Characteristics**

	FPS AP-120B	CSP MAP 300
Ideal Floating Point Operation, Maximum Rate	12.0M floating point calculations/s	14.25M floating point calculations/s
Maximum Block I/O Rate (DMA)	3M words/s	8M words/s
Maximum Programmed I/O Rate	Not Available	1.8M words/s
Capability to Perform PIO Data Manipulation	No	Yes
Internal Floating Point Word Size	38 bits (27-bit mantissa)	32 bits (24-bit mantissa)
Floating Point Mantissa Guaranteed Precision	21 bits	21 bits
Floating Point Format Dynamic Range	$10^{\pm 168}$	$10^{\pm 78}$
Number of Floating Point Accumulators	64	32
Fast Access Table Memory	Up to 64k words	Not Available

control of peripheral devices and overall sequencing of processing events. Both achieve significant numerical processing speed improvements over a typical mini-computer while performing repetitive numerical operations. Neither performs efficiently while performing complex logical operations based on data values. Beyond these general statements, the distinctions become more apparent.

Unit A (AP-120B) has a greater numerical dynamic range and carries greater numerical precision in its calculations. An overall reduced error from repetitive calculations upon data is a definite advantage that unit A holds over unit B (MAP-300).

The synchronous parallel operation of unit A versus the asynchronous parallel operation of unit B manifests itself in relative complexity of conceptualization and sequencing control. Unit A, although more difficult to program than a typical minicomputer, should be vastly easier to program than unit B. This simplicity is obtained by inefficient usage of the high speed (but high cost) program control memory in unit A.

On the other hand, unit B provides more flexibility in I/O control and more efficient utilization of both program and data memory. A definite disadvantage of unit B is the small program memories in all but the CSPU. This limitation necessitates that the CSPU reload the submicroprocessor control programs whenever a functional processing change is made, requiring suspension of numerical processing for the many microseconds needed to load the particular program memory with the necessary software code.

The 64 accumulators and the fast access table memory of unit A provide a potential processing advantage over the 32 accumulators and no table memory in unit B. Alternately, the parallel adders and multipliers of unit B provide a comparable arithmetic speed-up advantage over the pipeline adder and multiplier of unit A.

Finally, selection between unit A and unit B should be based primarily upon programming cost, I/O requirements, minimum acceptable memory configuration, and final cost for each application configuration. Although difficult and time consuming, benchmark programs of specific processing algorithms, which are typical of the machine's intended application, would best illustrate the advantage of one array processor over the other.

Bibliography

- R. A. Caspe, "Array Processors," *Mini-Micro Systems*, July 1978, pp 54-63
- CSP, Inc, "Macro Arithmetic Processor Systems (MAP-100/200/300) Programmers Reference Manual," Doc No. JB 6000-001-00, CSP Inc, 209 Middlesex Tpk, Burlington, MA 01803, May 1975
- Floating Point Systems, Inc, "AP-120B Array Transform Processor Handbook," Doc No. 725g-01, Floating Point Systems, Inc, Portland, Ore, 1976
- A. S. Margulies, "Array Processing Eases High Speed Vector Computation," *Digital Design*, June 1978, pp 52-56
- J. Meyn, "Processing Digitized Video In Realtime," *Computer Design*, Dec 1978, p 104
- C. N. Winningstad, "Scientific Computing On a Budget," *Data-mation*, Oct 1978, pp 159-164
- W. R. Wittmayer, "Array Processor Provides High Throughput Rates," *Computer Design*, Mar 1978, pp 93-100



Stephen Hufnagel is a research scientist at Applied Research Laboratories, The University of Texas at Austin, where he is involved in an exploratory development project entailing application of minicomputers to monitor, process, and control acoustic systems in a realtime environment. He holds a BS degree in mathematics from The University of Texas and has done graduate studies in electrical engineering and computer science there.

MICRO POWER

6500 performance, one-chip price. That's Rockwell Micropower.

The fastest selling microprocessor is now a one-chip microcomputer — Rockwell R6500/1.

The low-cost solution for high speed controllers, instrumentation and much more, the R6500/1 has 6502 CPU, 2K-byte ROM, 64-byte RAM, 16-bit programmable, 4-mode counter/timer, and 32 bidirectional ports. It operates on single 5V power.

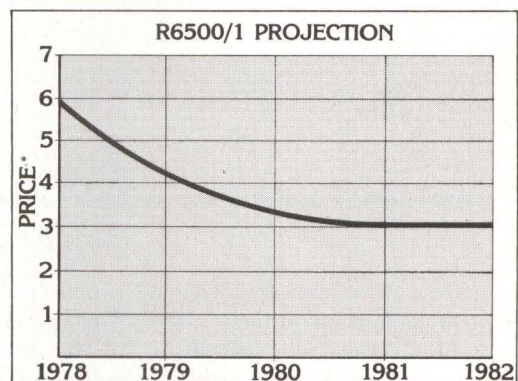
Proof is its performance. 6500 instruction power—13 addressing modes. $1\mu\text{s}$ minimum instruction execution at 2MHz. Benchmark it against any available one-chipper at any clock rate.

R6500/1 is totally upward/downward compatible with the entire 6500 family. It's fully supported with disk based SYSTEM 65 and high level PL/65 language. And Rockwell provides Emulator device for PROM prototyping.

R6500 on one chip—that's Rockwell Micropower!

For more information, contact Department 727-A2, Microelectronic Devices, Rockwell International; P.O. Box 3669; Anaheim, CA 92803, or phone (714) 632-3729.

*high volume



Rockwell International

...where science gets down to business

Troubleshooting Microprocessors With a Logic Analyzer System

Designed for flexibility, general purpose logic analyzer system performs realtime microprocessor investigation within the context of operational software by visually exhibiting map, data, and timing diagram displays

Robert Lorentzen

Gould Incorporated, Biomation Division, Santa Clara, California

A complete logic analyzer system performs an important problem solving role in locating microprocessor system software and hardware defects. This role begins at the final stages of software development and continues through production testing into field service repair. During the final stages of software development, the logic analyzer can help debug microprocessor software at maximum instruction rates. Problems that are transparent due to inherent speed restrictions of emulator instruction rates become defined and easily recorded using the logic analyzer. In production, the logic analyzer serves as a vital test tool by pinpointing hardware problems such as miswires, solder bridges, and defective integrated circuits. In field

service, the logic analyzer diagnoses operational difficulties onsite. A typical microprocessor problem helps demonstrate the problem solving capabilities of a general-purpose logic analyzer system.

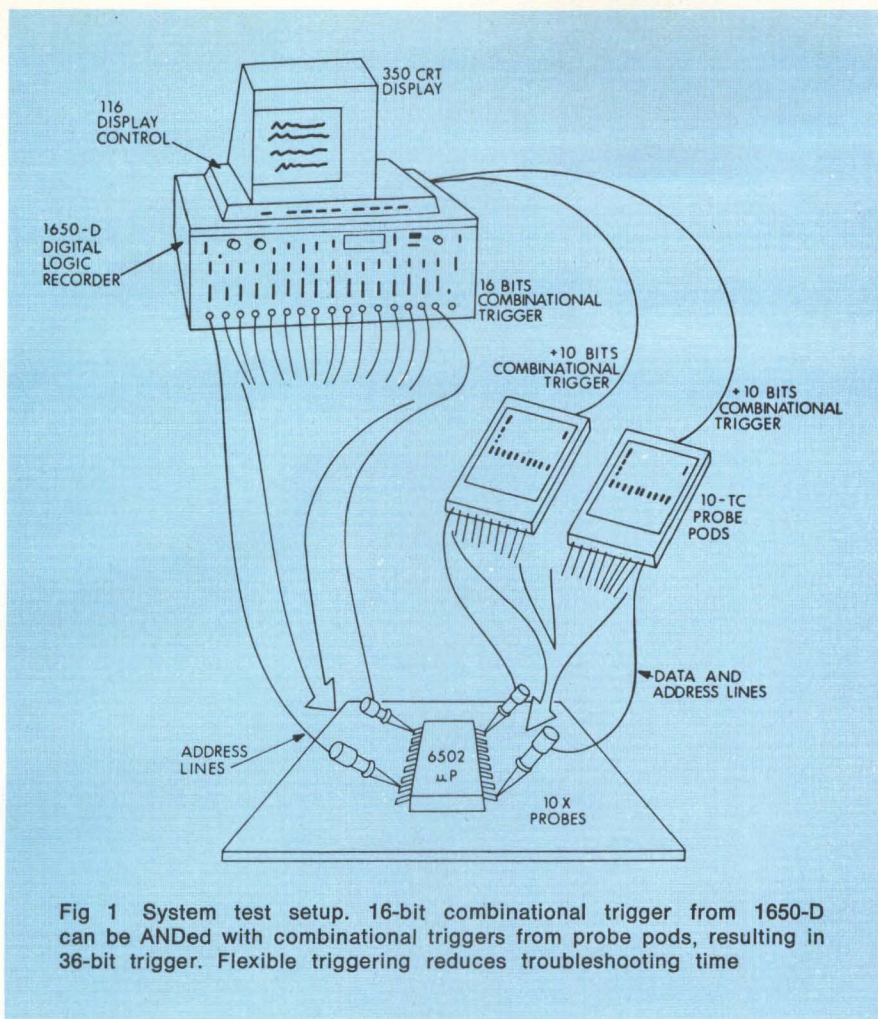
Equipment

In this application,* the microprocessor system consists of a 6502 microprocessor, a 6520 peripheral interface adapter, and a 6530 integral memory, I/O, and timer array. The 6502 is an 8-bit data, 16-bit address, four control line microprocessor with a minimum clock period of 1 μ s. The logic analyzer system comprises the 1650-D digital logic analyzer, the 116 display control, the 350 cathode-ray tube (CRT) display, two 10-TC probe pods, and 16 10X probes (Fig 1).

The logic analyzer records 16 inputs simultaneously at rates from dc to 50 MHz, storing 512 samples of the inputs in a 16 x 512-bit memory, and provides a 16-channel repetitive output.

In turn, the display control accesses the analyzer's memory to furnish any one of three selectable formats for CRT display including: (1) a standard timing diagram display format of all 16 channels, which is useful for hardware troubleshooting relative to time; (2) a data domain format that simultaneously shows memory address locations, a

*"Troubleshooting Microprocessor-Based Systems," Application Note 165AN-1, Gould Inc, Biomation Div, Santa Clara, Calif, Feb 1978



data truth table of 1s and 0s, and a selectable hexadecimal/octal data word translation, all of which are ideal for software analysis; or (3) a map mode that converts the analyzer's memory via digital-to-analog converters into a dot matrix pattern or signature that individually characterizes the system, assisting both software and hardware investigation.

The two probe pods have miniature probe clips that allow easy connection directly to the microprocessor unit (MPU) chip pins. Eight address bits pass through each pod and data ribbon cable to be recorded by the analyzer. In addition to the convenience of interconnection, the probe pod also has combinational trigger capabilities. This allows the expansion of the analyzer's combinational trigger to 36 bits wide, thereby allowing triggering from address and data (Fig 1).

System Problem and Solution

Program execution of the 6502 is recorded and examined easily and

rapidly with the logic analyzer system. In testing the microprocessor system under discussion, the logic analyzer indicates that, periodically, improper program execution occurs after start location address FFFC₁₆.

The first recording for the test setup is made with the analyzer in the pretrigger record mode to obtain a continuous tabulation of events (before and after the trigger is stored). The display control is set in the data domain mode and hexadecimal format, with the probe pods connected to the 6502 address bus. The analyzer's combinational trigger is set for the 6502 start location address (FFFC₁₆).

In Fig 2, the first recorded display shows the first 16 analyzer memory locations (1st column, decimal), the state table of the 6502 address bus (2nd, 3rd, 4th, and 5th columns, binary), and the hexadecimal conversion of the state data on the address bus (6th column). This display indicates that the microprocessor operated properly. This infor-

```

001 1111 1111 1111 1100 FFFC
002 1111 1111 1111 1101 FFFD
003 0111 0000 0000 0110 700E
004 0111 0000 0000 0111 700F

005 0111 0000 0000 1000 7008
006 0111 0000 0000 1001 7009
007 0111 0000 0000 1010 700A
008 0110 1110 0000 0011 5E0B

009 0111 0000 0000 1011 700B
010 0111 0000 0000 1100 700C
011 0111 0000 0000 1101 700D
012 0111 0000 0000 1110 700E

013 0111 0000 0000 1111 700F
014 0111 0011 1111 1111 73FF
015 0111 0000 0001 0000 7010
016 0111 0000 0001 0001 7011

```

Fig 2 Data domain display. First recording shows valid program execution; analyzer triggers on start location FFFC. Cursor is top line. Sixteen memory accesses are shown; cursor position determines which 16 addresses in memory are displayed



Fig 3 Map display for valid program execution. Analyzer triggers on start location FFFC. Cursor (boxed point) is placed at trigger and displayed at top of screen. 507 memory accesses after trigger are mapped

```

001 1111 1111 1111 1100 FFFC
002 1111 1111 1111 1110 FFFE
003 1111 1111 1111 1110 FFFE
004 0101 0010 1111 1110 52FE

005 1111 1111 0101 0001 FFS1
006 1000 1101 1111 1110 9DFE
007 1111 1111 1000 1100 FFFC
008 1011 0101 1111 1110 B5FE

009 1111 1111 1011 0100 FFB4
010 0100 1000 1111 1110 48FE
011 1111 1111 0100 0111 FF47
012 1010 1101 1111 1110 ADFE

013 1111 1111 1010 1100 FFA0
014 1011 0011 1111 1110 B3FE
015 1111 1111 1011 0010 FFB2
016 0110 0000 1111 1110 60FE

```

Fig 4 Data domain display for invalid program execution. Analyzer triggers on start address FFFC. Logic analyzer has captured faulty execution. Invalid program execution may contain clue to solution

mation is then loaded in the display control 16 x 16 hold memory for comparison against future recordings. Fig 3 shows the map mode output equivalent of the first recorded display.

An invalid program execution sequence is presented in Fig 4. Vir-

tually all addresses after start location address FFFC are incorrect. Differences between subsequent invalid program executions in the data domain are random and sometimes subtle. The display control compare mode (new recording compared with stored recording) helps to single out differences in the new recording. In this mode, all bit differences flash on the display; observe that the 15 addresses immediately following start address FFFC do not agree with those from Fig 2. The map mode is used extensively to highlight good and bad program executions. Fig 5 presents a signature for the invalid program execution shown in Fig 4. By comparing Figs 3 and 5, differences in the two recordings are easily discernible.

Because of the random addresses following start location FFFC in an invalid program execution, a recording that includes the microprocessor reset or start control line is made. The test setup is changed to include the start control line, and the trigger is derived externally via the probe pods (Fig 6). This configuration allows expanding the trigger word beyond FFFC and, in this case, to include the start control line. Pretrigger memory is set at 300 clock intervals. The 15 lower order address lines are recorded along with the start line, allowing observation of microprocessor op-

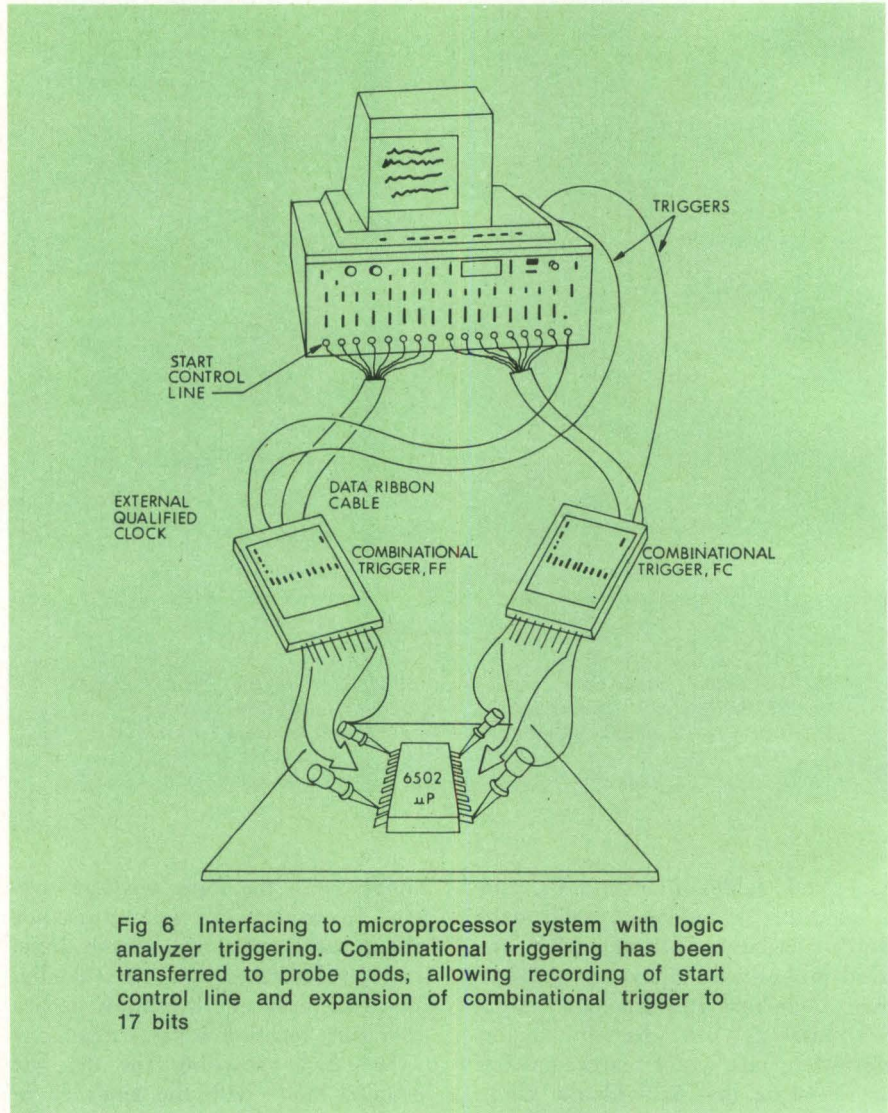


Fig 6 Interfacing to microprocessor system with logic analyzer triggering. Combinational triggering has been transferred to probe pods, allowing recording of start control line and expansion of combinational trigger to 17 bits

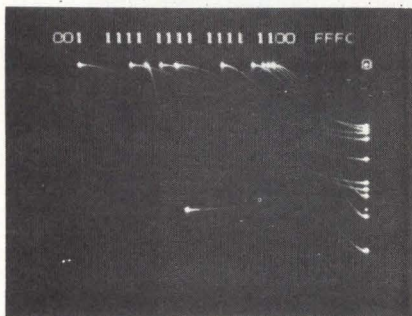


Fig 5 Map display for invalid program execution. Analyzer triggers on start location FFFC. All 508 program steps are conveniently displayed, allowing easy discernment between valid and invalid program executions. Compare with Fig 3

eration. Output data are reviewed in the data domain and timing modes. 300 clock intervals of pretrigger memory enable analysis of the activity on the address and start line before and after microprocessor start. Several recordings in this configuration will indicate the source of the problem.

In normal operation, the start control line is held low, inhibiting writing to or from the microprocessor; when a transition from low to high occurs, the microprocessor immediately begins the start sequence. The start control line is predominantly high when start location address

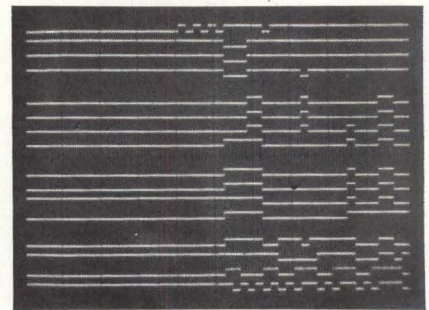
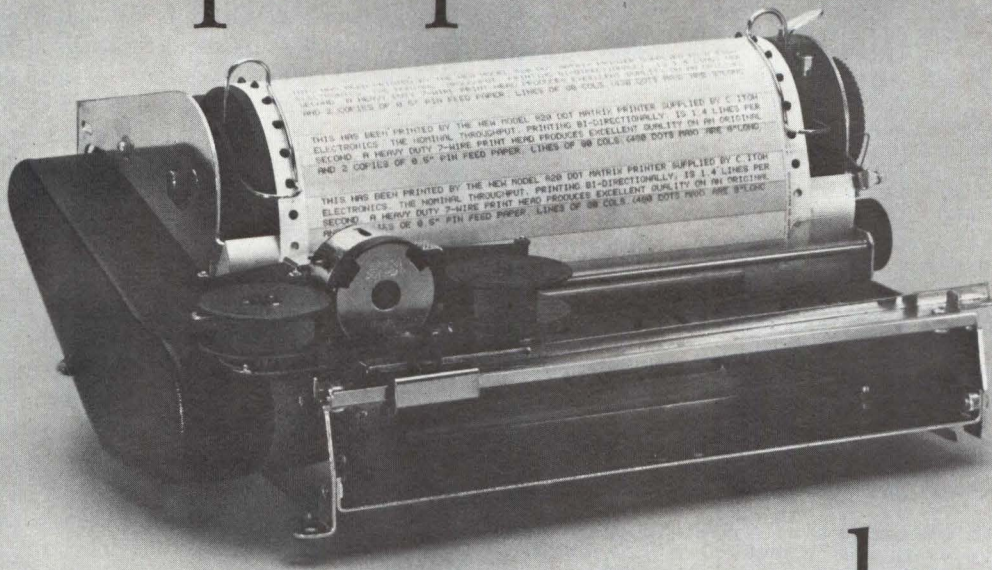


Fig 7 Time domain display of start control line (trace #1) 0-to-1 transition, and ringing. Analyzer's latch mode is used to capture glitches as narrow as 5 ns following 0-to-1 transition. Traces 2 through 16 are address lines A14 through A0, respectively

Model 820, 150 cps, 80-column, dot matrix impact print mechanism...



Here's the low cost bi-directional 150 cps print mechanism you've been waiting for. It's an 80-column dot-matrix impact print mechanism with a 7-wire heavy-duty, jeweled head that permits a life of 100-million characters! The mechanism utilizes an extremely simple design to achieve its cost performance and high reliability. It's the perfect OEM unit for computer output, communication terminals, data loggers, and general business applications. A sprocket paper-feed mechanism accepts standard 9.5" wide multi-**low cost** pin-feed paper. Print line position is adjustable vertically, and paper can be loaded from the bottom or from the rear. Price, in quantities of 500, is \$230.00* each. For detailed specifications, write or call today. **and too!**

**Domestic U.S.A. price only.*

C. Itoh Electronics, Inc.

5301 Beethoven Street, Los Angeles, CA 90066

Call: 213 390-7778 • Telex: WU 65-2451

East Coast

280 Park Avenue, New York, NY 10017

Call: 212 682-0420 • Telex: WU 12-5059

C. Itoh means excellence in printers

C. Itoh Electronics is part of the 118-year-old C. Itoh & Co. Ltd. world-wide trading organization.

CIRCLE 76 ON INQUIRY CARD

Engineering

challenge... research... discovery...

...it's the world of ECM.

It's our world here at Northrop Defense Systems Division. And it's a world to which you should aspire.

If you're intrigued and inspired by the new, the innovative, the state-of-the-art . . . you'll want to know that we at Northrop have committed ourselves to these ideals for the past twenty-five years. They've led us to our position as a renowned leader in the research, design and manufacture of sophisticated electronic countermeasure (ECM) systems.

By maintaining an environment that encourages creative freedom, coupled with our consistent procurement of long-term contracts and outstanding financial compensation — we've succeeded in building one of the finest engineering teams in the world.

But we need YOU. If you're trained and experienced in one of the following areas, investigate the potential at Northrop:

PRODUCT DESIGN

- *5-10 years experience in electronics and electromechanical high density packaging of military support equipment. Knowledge of investment casting and metal fabrication method processes.
- *RF design and analysis. Octave bandwidth MIC and strip-line components. ECM TWT and equipment experience, plus familiarity with MIL-STD-38510 and 5400E requirements.
- *Project Engineer with background in power supplies, modulators and high power TWT's required. Will be responsible for design and development of ECM transmitter.
- *Project Engineer with analog/digital circuits and microwave components experience.
- *Digital—Experience in design engineering for digital/analog controlled hardware necessary. Understanding of high voltage design and microwave circuitry desirable.

SYSTEMS

SENIOR ENGINEERS

MSEE and a minimum of 3 years experience in hardware or systems design and good written communications skills required. Microwave background necessary.

PROJECT ENGINEERS

A minimum of 5 years experience in EW hardware, software, systems design and analysis (active and/or passive), necessary. Microwave experience required.

ENGINEERS

Experience in active and passive electronic warfare systems and strong software and/or hardware background necessary.

We offer outstanding compensation packages including complete benefits, unlimited growth potential and the opportunity to combine the career of a lifetime with off-hours enjoyment in Chicago, one of the most exciting, culturally alive and highly liveable areas in the nation. For further information, please forward your resume stating salary history and requirements, in confidence, to:

Employment Manager, Dept CD379
NORTHROP CORPORATION
Defense Systems Division
600 Hicks Rd., Rolling Meadows, IL 60008
an equal opportunity employer m/f



FFFC is recorded. Periodically, however, the line is low when FFFC is recorded. This indicates that address FFFC occasionally appears twice during a 6502 start.

A timing mode recording is made to determine if the start signal 0 to 1 transition could be the cause of invalid program execution. Fig 7 shows the start signal transition recorded using the 6502's 1-MHz clock. The analyzer's latch is also employed to enhance this sample rate by flagging threshold transitions as small as 5 ns that occur between active clock edges. Negative pulses after the first 0 to 1 transition indicate ringing has occurred. This ringing is not the source of invalid program execution; proper program execution takes place despite this ringing.

By ANDing the start control line with the address (17-bit combinational trigger) bus, both occurrences of address FFFC are isolated. Address FFFC occurs once periodically when the start control line is 0 and once each time the start control line goes high, or to a 1 level. The address bus of the 6502 is undefined when the start control line is low. Address FFFC during this time is meaningless and does not represent a program execution. To record a valid 6502 program execution beginning with location FFFC, the analyzer must be triggered from a 17-bit combinational trigger. The combinational trigger includes the start control line at a 1 level, ANDed with the start location address of FFFC, as depicted in Fig 6.

The trigger expansion capability (from 16 to 36 bits), the analyzer latch input mode, and time resolution down to 20 ns allow rapid and precise microprocessor troubleshooting of software and hardware problems. The probe pods can be used to detect the address while data and control signals are recorded by the analyzer with the 10X probes or probe pods.

These are only a few of the features of the logic analyzer which analyzes a microprocessor system in real time, using operational software. It solves system problems starting with software development, continuing through production test, and on to in-service repairs. □

DEC Compatible Interconnect.

Get there 2 to 5 months sooner.

We equal DEC in form, fit, and function, but our delivery is better.

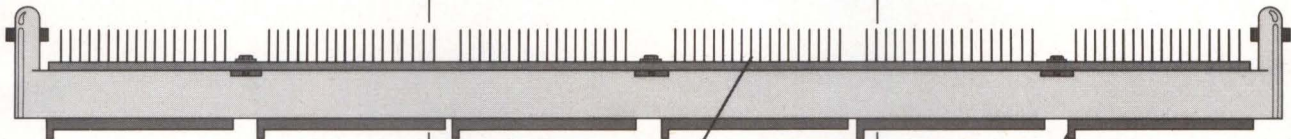
If you need standard replacements for your DEC backpanel interconnects but just can't wait months, call SAE. Ours are available in 4, 6, or 9 slot configurations. Or add more rows and/or slots and special order your own custom configuration.

Easy pin repair. Replace 1 pin, not 288.

You'll save valuable time and hardware dollars by replacing only the broken pins (not a whole section) on your PDP-11, LSI-11 or DEC peripheral interconnection.

Get the whole story on connectors/backplanes, hardware, and accessories.

For a copy of our data sheet with complete listings of mounting systems, units, logic modules, replacement parts, and simple hand tools for repair, write SAE, Stanford Applied Engineering, 340 Martin Avenue, Santa Clara, CA 95050. Or call (408) 243-9200.



Alloy CA 725 with selective 0.000030 μ in. gold plate contact over 0.000050 μ in. nickel plate.

Exclusive in-contact polarizing key is available for board plug-in safety.

SAE's DSC-H933-C four-slot mounting system shown. 4 x 6 backplane with frame, 18 dual pin, 24 module capacity.



SAE

Your quality source for
PC connectors • sockets
• switches • flat cable systems.

High Speed Low Error Data Transmission with Fiber Optics

A single channel design approach handles data rates up to 10M bits/s over distances to 100 meters while holding the maximum bit error rate to 10^{-9}

Hans O. Sorensen Hewlett-Packard Optoelectronics Division, Palo Alto, California

Losses in a point-to-point fiber optic system are insertion loss at the input and output, connector loss, and transmission loss proportional to cable length. Variations in these losses require a receiver with a dynamic range that can accommodate the variations and yet be able to provide adequate bandwidth (BW) and signal-to-noise (S/N) ratio at the lowest flux level. Fortunately, since no noise is picked up by a fiber optic cable, the receiver S/N ratio at any BW is limited only by the noise produced within the receiver. Receiver dynamic range must be large enough to accommodate all the loss variables that a system may present. For example, if the system flexibility requirement is for transmission distances ranging from 10 to 1000 m with 12.5-dB/km cable, and up to

two inline connectors, the dynamic range requirement is typically 20.5 dB.

Accommodating a 20-dB optical flux dynamic range plus maintaining high sensitivity requires the receiver to have two important capabilities: automatic level control (ALC), and ac coupling or its equivalent. The latter keeps the output of the receiver differential amplifier at a fixed quiescent level relative to logic thresholds, so that signal excursions as small as the specified minimum can cause the amplifier output to exceed the logic threshold. This function can also be called dc restoration.

ALC adjusts amplifier gain. Low amplitude excursions are amplified at full gain; for high amplitude excursions the gain is automatically reduced enough to prevent output

amplifier saturation. Saturation adversely affects propagation delay, so ALC is needed to allow high speed performance at high, as well as at low signal levels.

Fiber Optic System Design

In addition to ruggedness and reliability, several other objectives were established as targets for this development. Primary design objectives were convenience and simplicity of system installation and operation, along with a probability of error $P_e < 10^{-9}$ at 10M bits/s nonreturn to zero (NRZ) over moderate distances. Manufacturing costs also had to be low enough to make the system attractively priced relative to performance.

Electrical convenience is provided by several system capabilities. The

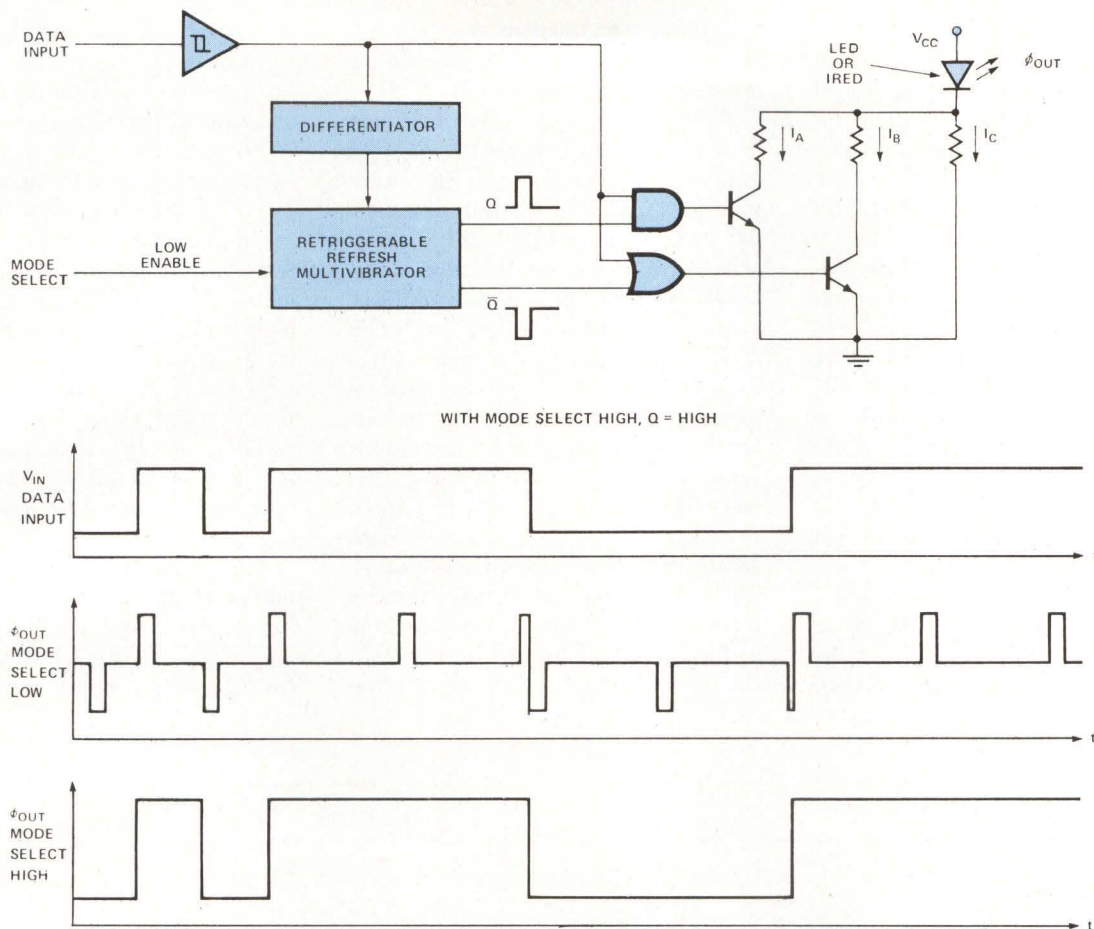


Fig 1 Simplified transmitter block diagram and waveforms. Entire transmitter is hybrid assembly in all-metal package. In addition to 5 V and ground, there are two TTL level inputs: data input and mode select. Making mode select high disables refresh multivibrator with Q high (\bar{Q} low), so that output flux (ϕ_{OUT}) is digital replica of data input signal. This mode requires external coding of data input signal for proper operation of receiver (Fig 2). With mode select low, refresh multivibrator is enabled, and output flux is internally pulse bipolar (PBP) coded. This makes system transparent with no restrictions on data format, allowing transmission of NRZ, RZ, or any arbitrarily timed digital signals, such as PWM

transmitter (Fig 1) and receiver (Fig 2) require only a single 5-V supply. All inputs and outputs function at TTL levels. No receiver adjustments are necessary because of the 21-dB or more receiver dynamic range that accommodates to fiber length variations as well as to age and thermal effects. When the system is operated in its internally coded mode, it has NRZ arbitrarily timed data capability, and is no more complicated to operate than a non-inverting logic element. Built-in performance indicators are available in the receiver. The link monitor indicates satisfactory

signal conditions, and the test point allows simple periodic maintenance checks on the system flux margin.

The internally coded mode of operation is the simplest way to use this system. This mode places no restriction on the data format as long as either positive or negative pulse duration is not less than the minimum specified. Simplicity is achieved by the use of a 3-level coding scheme called a pulse bipolar (PBP) code. This mode is selected simply by applying a logic low (or ground) to the mode select terminal on the transmitter — no conditioning signal or

adjustment is necessary in the receiver because it automatically responds to PBP code.

Transmitter Description

Fig 1 shows symbolically the logical arrangement of the transmitter, waveforms for signal currents I_A and I_B , and resulting waveforms for output flux. The arrangement is logically correct but circuit details are not actually realized as shown. For example, current sources actually have partial compensation for the negative temperature coefficient of the GaAsP

LED (or IRED). Fig 1 highlights five important technical design aspects.

First, the bias current (I_C) is never turned off — even when the transmitter is operated in the externally-coded mode (mode select high). This is done to enhance switching speed of the LED (or IRED) in either internally or externally coded mode. The bias current also stabilizes the flux excursion ratio (k) symmetry in the internally coded mode.

Second, ϕ_L (low level flux) is produced by I_C ; ϕ_M (mid level flux) requires $I_B + I_C$; and ϕ_H (high level flux) requires $I_A + I_B + I_C$. For the receiver, the excursion flux ($\Delta\phi$), produced by switching I_A and I_B , is the important parameter of the transmitter. Average flux is, of course, related to excursion flux, but is not as important in establishing the S/N ratio of the system.

Third, with mode select low and a typical 500-kHz signal at data input, there will be only one refresh pulse generated in each logic state. Excursions ($\phi_H - \phi_M$) and ($\phi_M - \phi_L$) are

nearly balanced; thus, an average-reading flux meter will indicate the mid level flux (ϕ_M) within $\pm 0.6\%$, depending on whether the flux excursion ratio is at its maximum or minimum limit, respectively.

Fourth, with mode select low, any data input transition (either hi-lo or lo-hi) retriggers the refresh multivibrator to start a new train of pulses. All refresh pulses for either logic state have the same duration. This keeps average flux near midlevel, even when the duration in either logic state of arbitrarily timed input data is short. Any refresh pulse is overridden (abbreviated) by the occurrence of a data input transition; thus, there is no additional jitter when the duration of the data input in either state is at or near the same length of time as the refresh interval. The refresh interval is long, relative to the refresh pulse duration, making a duty factor of approximately 2%; this also is done to keep the average

flux near mid level regardless of how long data input remains in either logic state. The only condition under which the average flux can deviate significantly from mid level occurs when data input remains in one state for a period of time less than the duration of the refresh pulse. If this is likely to occur, the format should be configured so that the numbers of 1s and 0s are balanced as they would be in Manchester code.* Observing this data format allows the use of the internally coded mode of this fiber optic system at data rates ranging from arbitrarily low to higher than 10M baud, the absolute limit being that at which signal intervals become as short as t_{PHL} (propagation delay for hi-to-lo transition) and/or t_{PLH} (propagation delay for lo-to-hi transition).

Fifth, with mode select high, the Q output of the refresh multivibrator is high (and \bar{Q} is low). In this condi-

*D. J. Morris, *Electronic Design*, No 22, Oct 25, 1978, pp 84-91

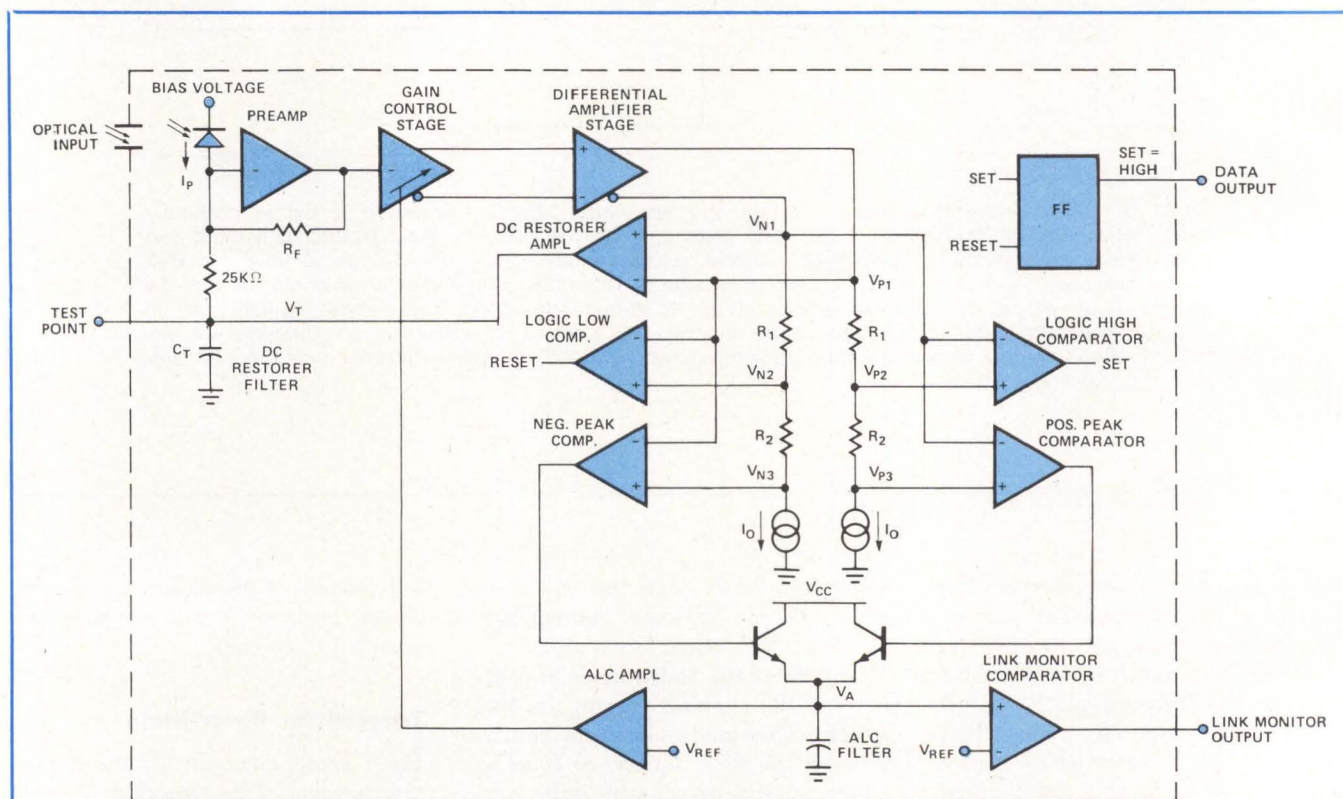
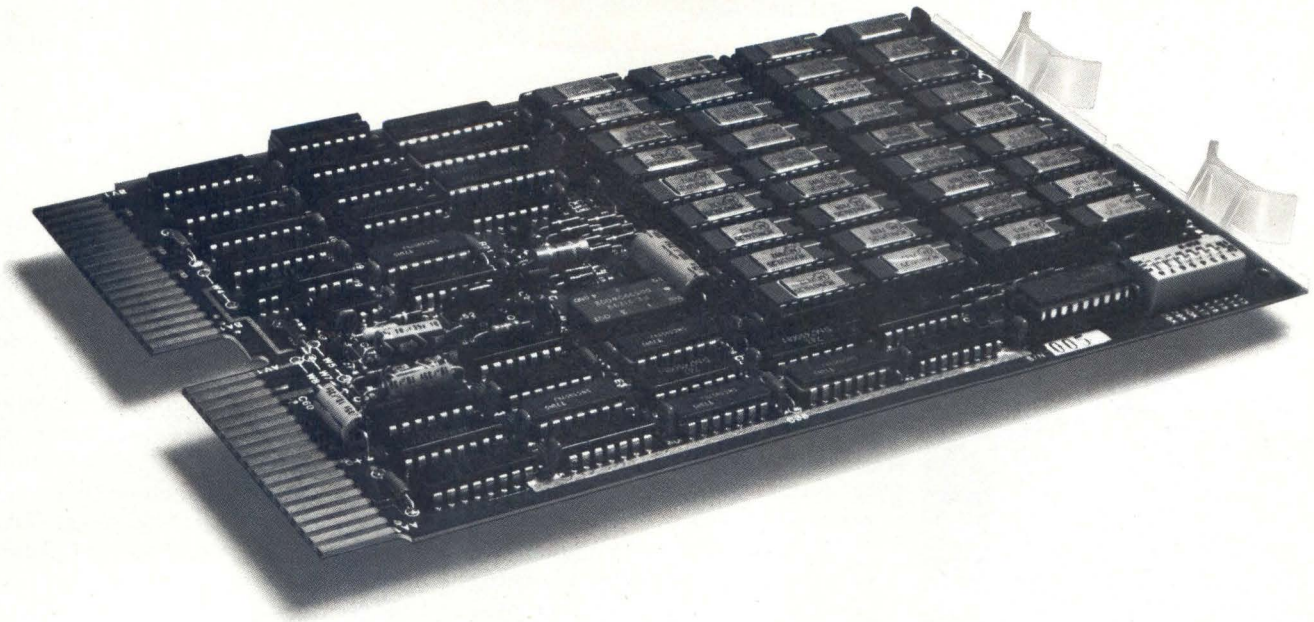


Fig 2 Simplified receiver block diagram. Hybrid-assembled in an all-metal package, receiver requires only 5 V and ground, and has three outputs: data output and link monitor are low power Schottky TTL level, while test point has high impedance. Test point voltage varies linearly as average input flux. High level at link monitor output indicates that amplifier output voltage excursions are large enough to activate automatic level control (ALC) and are, therefore, ample for operation of logic comparators. Positive flux excursion produces a positive voltage excursion that sets R-S flip-flop to make data output high until negative excursion resets flip-flop

Technological leadership.



LSI-11/2 add-in. Add the future to your memory. Now.

Decode 18-bit address. Recover 3K words of I/O page.

Motorola's MMS1102 add-in module covers your future LSI-11/2* memory management needs. It is address selectable on 4K boundaries in a 128-word address space (decodes a full 18-bit address), matching requirements of the future as well as today's 16-bit address.

Up to 3K words of I/O page can be selectively utilized as read/write memory. That unique feature is standard, switch selectable.

Extensive parity options.

Other features include optional on-board parity generation and checking logic, internally distributed refresh, plus total hardware and software compatibility with LSI-11/2 and LSI-11* systems. Low standby power complements the LSI-11 battery backup feature. The '1102 is built with industry standard MCM4116 dynamic RAMs, and with the high Motorola quality and reliability you expect.

Good for the budget.

Budget tight? Motorola's 32K x 18(16) MMS1102 is the inexpensive way to add the system storage you need now, with the future on board. Get off-the-shelf delivery for just \$950 (1-5 quantity), and OEM discounts are available.

Call (512) 928-6776

For immediate price and delivery information, call Motorola Memory Systems, (512) 928-6776, or your local Motorola sales office. To get an MMS1102 data sheet, write Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036, or circle the reader service number.

The MMS1102 is only one of the broad line of Motorola add-in, add-on memories available now for new and expanding systems everywhere. And, leading-edge storage capability is but one of the many technologies in which Motorola is providing service to the designers of

Innovative systems
through silicon.



MOTOROLA INC.

*Trademark of Digital Equipment Corp.

HOW DO YOU IMPROVE THE ACCURACY AND RELIABILITY OF A PERFORATED TAPE, FILM OR CHART DRIVE?



USE LAVEZZI HIGH PRECISION SPROCKETS, NATURALLY

Precision is more than just a word at La Vezzi. It has been the underlying concept for nearly 75 years of manufacturing sprockets, Geneva star-wheels and drivers, and other critical machine parts.

La Vezzi's record for achievement is testified by practically every motion picture projector used in the cinema today . . . in tape control systems, in medical analytical equipment, geophysical and astronomical recording systems, as well as data processing and business equipment.

The reason! La Vezzi has developed the technology to produce components with tight tolerances, and instituted quality control standards to verify the integrity of their parts.

Look to La Vezzi for an accurate way to drive your ideas. Our catalog tells all.

LaVezzi
machine works, inc.

900 N. Larch Ave.,
Elmhurst, Ill. 60126
(312) 832-8990



tion, I_A and I_B are both ON when data input is high, and both are OFF when it is low. This makes the output flux excursion a logical replica of the data input.

Receiver Description

The receiver block diagram (Fig 2) consists of four functional blocks: (1) a differential amplifier, including a gain-control stage and split-phase outputs, with a voltage divider for each; (2) a dc restorer with a long time constant; (3) logic comparators with an R-S latch; and (4) positive and negative peak comparators with single-ended output for the ALC and link monitor circuits.

The PIN photodiode converts optical flux at the input to a photocurrent (I_P), which is in turn converted to a voltage by the preamplifier. This voltage is amplified to a positive-going output (V_{P1}) and a negative-going output (V_{N1}). A rising input flux will cause V_{P1} to rise and V_{N1} to fall. These voltages are applied to the differential inputs of the dc restorer amplifier, whose output (V_T) falls until it is low enough to draw the average photocurrent away from the preamplifier via the $25k \Omega$ resistor. This makes $V_{P1} \approx V_{N1}$ when the input flux is at the average level. Output impedance of the dc restorer amplifier is high, making a long time constant with filter capacitor C_T . The long time constant is required for loop stability when input flux levels are so low that there is little or no ALC gain reduction, with consequently high loop gain. With no input flux, $V_T = V_{Tmax}$; as input flux rises, V_T falls proportionately, so that the voltage at the test point can be used as an indicator of average input flux. With respect to the receiver optical port, the responsivity of the PIN photodiode is approximately $0.4 A/W$.

As described above, when input flux is at the average level, the positive-going and negative-going output voltages, V_{P1} and V_{N1} , are approximately equal. Notice that this makes the outputs of both logic comparators low. A positive flux excursion, rising faster than the dc restorer (with its long time constant) can follow, will cause V_{P1} to rise and V_{N1} to fall. If the positive flux excursion is high enough, the logic high comparator input voltage ($V_{P2} - V_{N1}$) becomes positive, and a SET pulse is produced for the R-S flip-flop. Similarly, a negative flux excursion of such amplitude

would make the logic low comparator input voltage ($V_{N2} - V_{P1}$) become positive, and a RESET pulse would be produced.

A larger amplitude of positive flux excursion would make the positive peak detector input voltage ($V_{P3} - V_{N1}$) change from negative to positive and cause current to flow into the ALC filter capacitor. When voltage V_A starts to rise above V_{REF} , the ALC amplifier output will operate on the gain control amplifier to limit receiver forward gain. Notice that ALC action is the same for a negative flux excursion, so that the receiver gain limitation is determined either by a positive flux excursion or by a negative flux excursion — whichever is larger. For this reason, positive and negative excursions must be nearly balanced with respect to average flux. The allowable imbalance is determined by the values of the resistors in the negative and positive voltage dividers. ALC action limits the maximum excursion to a voltage of $[I_0 \times (R_1 + R_2)]$, whereas the logic threshold is only $I_0 \times R_1$. Actual limits are established by the tolerances on the resistors and the current sources. Notice that the ALC voltage (V_A) activates both the ALC comparator and the link monitor comparator. Therefore, a high link monitor output signifies two conditions: input flux excursions are high enough to cause ALC action (gain limitation), and excursions are more than adequate for operation of the logic comparator.

Notice that the link monitor output could be high, but k could be outside the specified limits such that P_e exceeds 10^{-9} . Conversely, because of safety margins in receiver design, it is also possible to have $P_e < 10^{-9}$ when the flux excursions are too small to make the Link Monitor output high.

The main concern in fiber optic link system design is the flux budget. Other areas of concern are data rate, data format, and the interface with other elements of a digital data transmission system. In this application, the fiber optic link is designed for logic-to-logic communications between computers, between computers and peripherals, and between computers and digital instruments.

This note was excerpted, with permission, from Application Note 1000, "Digital Data Transmission With the HP Fiber Optic System," Hewlett-Packard Optoelectronics Div, Palo Alto, Calif.

The first Four-Headed Diskette Drive. PerSci stays a generation ahead.

PerSci has done it. Now the industry's only diskette drive with voice coil positioning comes equipped with four heads reading and writing both sides of two eight inch diskettes to provide superior random access capabilities in microcomputer and minicomputer applications. The new PerSci Model 299 dual-head, dual diskette drive offers the highest data capacity, reliability and the fastest access speeds available among small storage peripherals. It is the first drive to advance diskette capability to the level of hard discs.

8 Times More Capacity...

Employing double density encoding on both sides of two diskettes, the PerSci 299 records up to 3.2 Mbytes of unformatted data—eight times the capacity of a standard, single density drive. This unmatched single drive capacity provides the basis for an independent low cost data management system. For maximum media interchangeability with other drives, the 299 will also read and/or write one or two single sided diskettes. Up to eight 299 drives (32 read/write heads) can be daisy chained to achieve a total formatted system capacity as high as 16 Mbytes. Data can be handled in a single density IBM 3740 type format, in IBM 2D compatible double density or in other expanded soft and hard sectored formats.

And Voice Coil Positioning For 6 Times More Speed...

Only PerSci, Inc., has engineered voice coil head positioning for diskette drives. This design innovation gives the PerSci 299 drive the lowest average seek time of any floppy—33 ms including settle. The full 76 track access speed of the Model 299 is under 100 ms.

In A Single Small Size Drive...

While the 299 provides the data capacity and access speed of a hard disc drive, it is the

size of a standard floppy—only 4.38" x 8.72" x 15.4!" Up to four 299 drives can be mounted vertically or two horizontally in a 19" rack.

With Superior Reliability And Ease Of Operation.

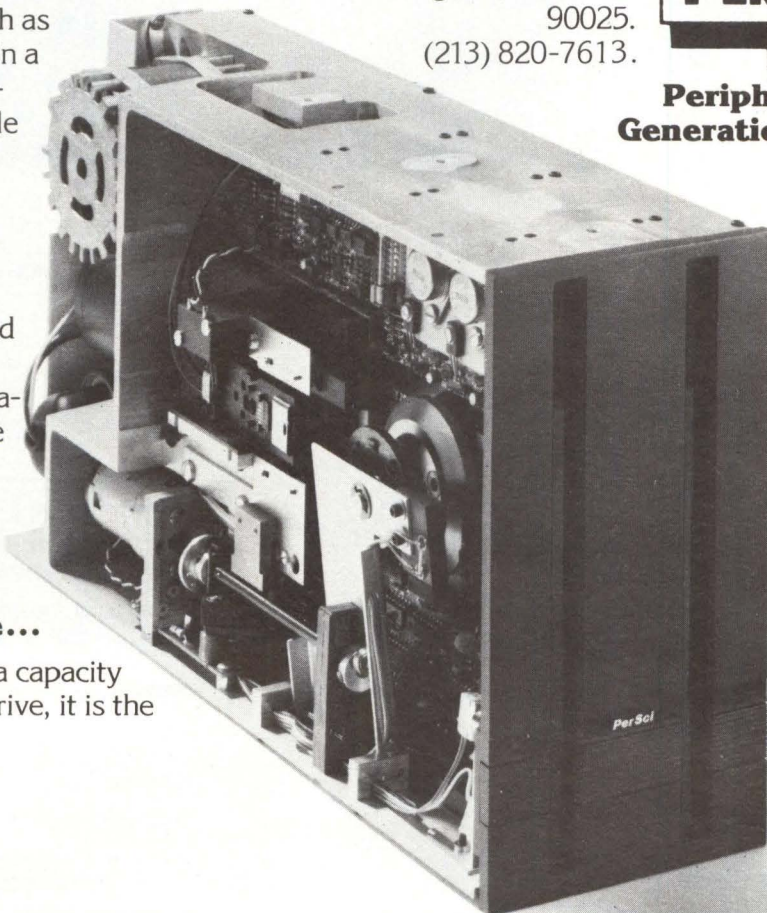
Mechanical and data reliability equal or superior to single headed drives—6000 hour MTBF and a soft error rate of 1 in 10^9 —are made possible by PerSci's advanced drive design. A write protect feature guards against operator error, while front panel lights indicate the diskette selected. Electric diskette autoloader protects diskettes from damage and allows drive unload by remote control.

Join The Next Generation... Now.

Get PerSci's four-headed diskette drive and get the speed, capacity and reliability of hard disc drives at a fraction of the size...and cost. Call or write for full information from PerSci, Inc., 12210 Nebraska Avenue, West Los Angeles, California 90025. (213) 820-7613.

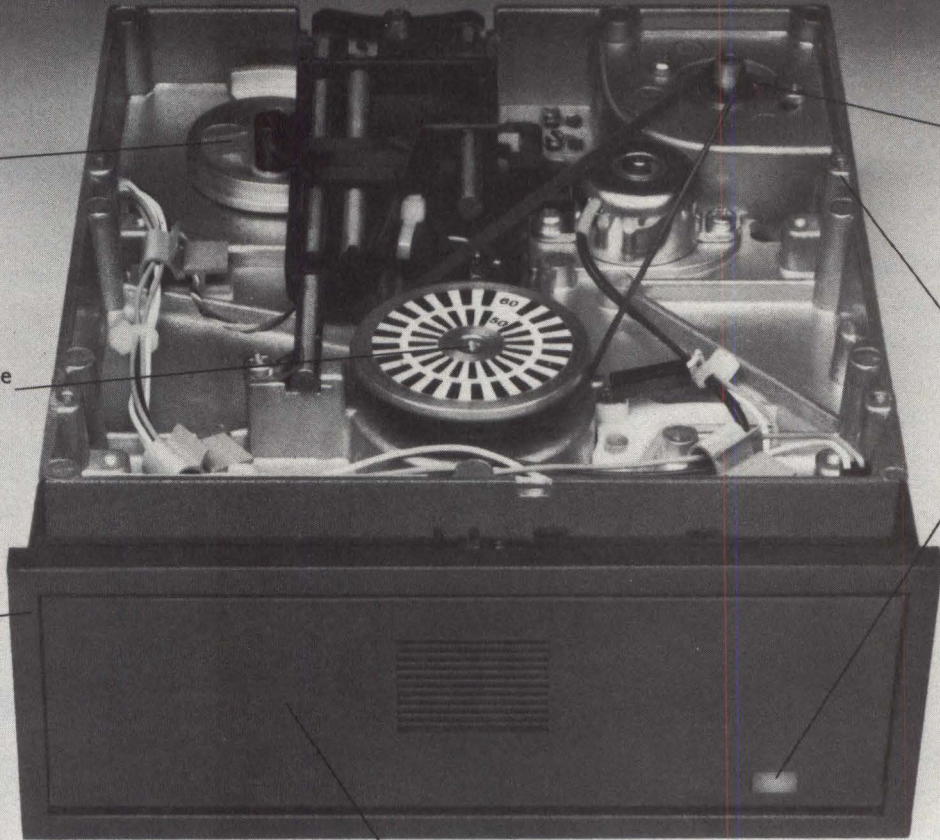


**Peripherals a
Generation Ahead.**



CIRCLE 80 ON INQUIRY CARD

Before you specify your next floppy disk drive, BASF has a small suggestion.



The 6106 uses a ball bearing, friction-free head positioner traveling in a spiral cam... resulting in less susceptibility to vibration or uneven wear.

Main capstan features a double ball race for more accurate and friction-free operation.

THE NEW BASF 6106 IS ONLY 2.1" HIGH. THREE 6106 DRIVES FIT IN THE SAME VERTICAL SPACE AS TWO OF OUR COMPETITION'S.

Consumes only 2/3 as much power as the competition, and generates less heat.

Industry-standard interface, power plugs and mounting points.

Activity light in door is standard.

Larger capacity than the competition: 40 tracks vs. 35 tracks at single or double recording density.

Track-to-track access time of 12 msec; more than three times faster than the competition.

Program-controllable door interlock option.

Built to tight production specs for improved reliability (10,000 hours MTBF) and less sensitivity to vibration.

Introducing the New BASF 5.25" Floppy Disk Drive.

The new BASF 6106 is not only the smallest 5.25" floppy disk drive available... it also offers many big advantages in terms of capacity, reliability, and accuracy. BASF is America's only producer of both 5.25" floppy disk drives and 5.25" floppy disk media. The 6106 is available right now at competitive prices. For complete information, send in the coupon now, or call Matt Connolly at 617-271-4035.

CIRCLE 140 ON INQUIRY CARD

BASF SYSTEMS

OEM Computer Products
Crosby Drive, Bedford, MA 01730

Please send me complete information and specifications on the new BASF 6106 5.25" Floppy Disk Drive.

Name/Title _____

Company _____

Address _____ Tel. _____

City _____ State _____ Zip _____



BASF

ELECTRO 79



In the Electronic Industry's No.1 Marketplace / New York

Electro takes a penetrating look at the technology, products and ideas that will dominate the industry in the approaching decade of the 80's. It begins Monday, April 23, with an all-day marketing seminar and a keynote address by Charles L. Brown, Chairman of the Board of the American Telephone and Telegraph Company.

Then, three days of exhibits and professional program sessions. There will be more than 700 exhibit booths and 120 technical presentations exploring topics like microprocessing, fiber optics, memory, minicomputers, testing, LSI, home computing and others.

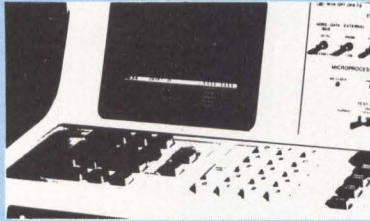


Electro / 79 in New York
April 24, 25 and 26, 1979
New York Coliseum / Exhibition
Americana Hotel / Professional Program

ADVANCED TECHNICAL

Course 142 — Five days

Troubleshooting Microprocessor-Based Systems



BOSTON
April 23-27

PHILADELPHIA
April 30-May 4

NEW YORK
May 14-18

TORONTO
June 25-29

SAN FRANCISCO
July 9-13

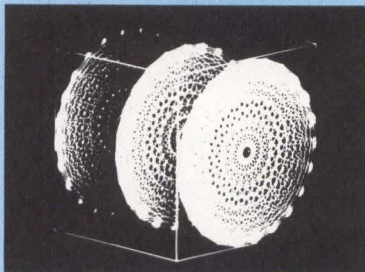
SAN DIEGO
July 23-27

Nearly all manufacturers, OEMs and end users are suffering from major production bottlenecks and customer service problems directly caused by the unavailability of trained personnel to test and troubleshoot microprocessor systems. This unique course is specifically designed for engineers and senior technicians involved in production testing, field service and design of microprocessor-based systems. The course provides these personnel with the practical knowledge they require, including an in-depth understanding of: a) microprocessor software and hardware; b) how to apply the most powerful microprocessor debugging technique; and c) how to use microprocessor troubleshooting equipment.

- Hardware Design Fundamentals
- Programming Fundamentals
- Overview of Microprocessor System Troubleshooting
- Writing Diagnostic Software
- Troubleshooting & Test Equipment
- Using Logic Analyzers
- In-Circuit Emulators
- Signature Analysis Techniques
- Microcomputer Development Systems
- Pre-Planning Requirements

Course 365 — Four days

Computer Graphics



BOSTON
April 24-27

PHILADELPHIA
May 1-4

SAN FRANCISCO
May 8-11

SEATTLE
May 15-18

ST. LOUIS
June 5-8

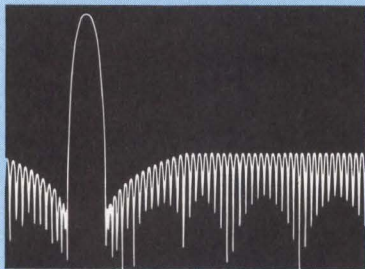
TORONTO
June 12-15

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

- Display Hardware
- Color Display Techniques
- Two Dimensional Graphics
- Three Dimensional Graphics
- Transformations
- Software Structures
- The Hidden Line Problem
- The Hidden Surface Problem
- Software 'Build or Buy'
- Selection Methodology

Course 412 — Five days

Digital Signal Processing



WASHINGTON D.C.
April 23-27

BOSTON
April 30-May 4

SAN DIEGO
May 7-11

SAN FRANCISCO
June 11-15

TORONTO
June 18-22

MINNEAPOLIS
July 9-13

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensible manner, to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

- An Overview of Applications
- Digital vs. Analog Signals
- Operations on Digital Signals
- Recursive Filters
- Nonrecursive Filters
- Design Techniques
- Computer Aided Design
- Statistical Approaches
- Spectral Estimation
- Application Case Study

COURSE ENROLLMENT INFORMATION

Course Hours:

Orientation (First Day): 8:15-9:00 A.M.
Lecture Sequence: 9:00 A.M.-4:30 P.M.
Informal Discussion Session with Instructor: 4:30-6:30 P.M.

Course Fees:

Four-Day Courses: 365, 350, 320 or 160 \$695.00 (U.S.)
Five-Day Courses: 142 or 412 \$795.00 (U.S.)

Course Fees Include: Lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.
Team/Group Discount: 10% reduction for three or more participants from the same organization, if invoiced at the same time.

CONFIRMATION:

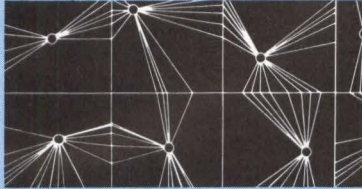
Upon receipt of your course Order Coupon or enrollment by telephone, a complete confirmation package will be forwarded, including course location details and an invoice.

DIPLOMA/CONTINUING EDUCATION UNITS

Each attendee receives a Course Completion Certificate awarding one Continuing Education Unit (CEU) for each ten hours of class participation. The CEU is a nationally recognized unit awarded by universities and educational organizations for participation in continuing educational programs.

Course 350 — Four days

Distributed Processing and Computer Networks



DETROIT
April 24-27

ST. LOUIS
May 1-4

SAN FRANCISCO
May 8-11

CHICAGO
May 15-18

TORONTO
June 5-8

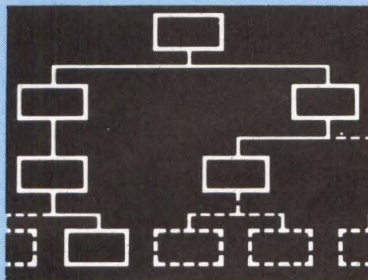
HARTFORD
June 12-15

This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of the concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

- What is to be Distributed?
- Database Structures
- Data Communication Concepts
- Database Requirements
- The Computation Continuum
- Security Considerations
- Computer Networks
- Evaluation and Selection
- Network Protocols
- Management and Control

Course 320 — Four days

Structured Programming



DETROIT
May 1-4

WASHINGTON D.C.
May 15-18

CHICAGO
June 5-8

TORONTO
June 12-15

HARTFORD
June 19-22

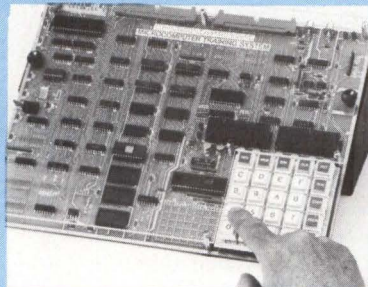
SAN FRANCISCO
July 10-13

This course is designed for programmers, software engineers, systems analysts and their managers who are charged with the responsibility of creating and maintaining reliable, complex program structures. Participants will develop a clear understanding of the concepts and applications of structured methodology, and will learn to evaluate various types of structured programming techniques. The course will provide in depth exposure to structured design and structured programming tools and procedures. The underlying theme of the course is the development of skills which will enable the production of structured programs at minimum cost, while planning for program changes, modifications and reducing maintenance costs.

- Analyzing the Programming Function
- Verification Using Structured Walk-Through
- Principles of Structured Program Design
- Developing Structured Systems
- Tools and Aids for Structured Program Design
- Productivity Management and Project Control
- Case Study Workshop
- Organizing the Programming Team
- Implementing Structured Coding

Course 160 — Four days

Microprocessor Hands-On Workshop



ANAHEIM
April 23-26

ST. LOUIS
May 1-4

NEW YORK
May 8-11

SEATTLE
May 15-18

TORONTO
May 29-June 1

WASHINGTON D.C.
June 4-7

This course is intended for engineers, programmers, systems analysts and their managers. It has been found extremely useful by attendees both with or without prior experience in either computers or electronics. In fact, managers who have attended report the course provides a level of familiarity, awareness, and confidence which enables them to better manage their staff in applying microprocessors.

EACH STUDENT RECEIVES A COMPLETE 8080 MICROCOMPUTER AND INTERFACING SYSTEM FOR HIS PERSONAL USE THROUGHOUT THE COURSE.

- Microprocessor Concepts and Terminology
- Development Equipment and Software
- Analysis of Potential Applications
- Selecting the Correct Microprocessor
- Microcomputer Hardware Design
- Managing a Microcomputer Project
- Hands-On Programming Exercises
- How to Get Started
- Hands-On Interfacing Exercises
- Future HW and SW Developments

PLEASE ENROLL ME IN COURSE: _____

CITY _____

DATE(s) _____

MAIL TO:

Integrated Computer Systems, Inc.
3304 Pico Blvd., P.O. Box 5339
Santa Monica, CA 90405

OR:

Integrated Computer Systems, Inc.
300 N. Washington St., Suite 103
Alexandria, VA 22314

OR CALL:

(213) 450-2060
LOS ANGELES

OR

(703) 548-1333
WASHINGTON, D.C.

Name _____ Job Title _____

Company _____ Mail Stop _____

Address _____

City _____ State/Province _____

Country _____ Postal Code/Zip _____ Telephone _____

- Please send FREE BROCHURES describing these courses.
- Please put me on your mail list to receive future course schedules.

A confirmation letter with complete details will be forwarded to you.

INTERFACING FUNDAMENTALS: DIRECT MEMORY ACCESS

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University

Christopher A. Titus and Jonathan A. Titus
Tychon, Inc

Direct memory access is a technique that allows a computer user to directly access individual memory locations without first having to go through the computer's central processing unit. This interfacing technique has numerous applications, but few microcomputer users fully understand them, and even fewer fully implement it for scientific data acquisition or control purposes.

Calculation of a very simple software routine that inputs an 8-bit data point and transfers it to a memory location shows that the routine takes many microseconds. Further, if more points are to be taken and stored in some sort of a sequential file, additional software steps are needed for "housekeeping" tasks that count the number of data points, increment the address pointer, etc. When these added software steps are introduced into the test program, an 8-bit data point may only be acquired every 30 to 40 μ s. Many cases, however, require higher data acquisition or data transfer rates. The idea of providing the computer user with direct access to the memory section of the computer is not new. Digital Equipment Corp provided a direct memory access (DMA) scheme in the PDP-8 series of minicomputers. It required additional hardware and the interfacing task was not particularly easy.

Most current microcomputers have a built-in DMA capability that few users ever consider. This allows small microcomputers to be used in high speed data acquisition systems where the data transfer rates are higher than those achieved under program control.

Microprocessor chips such as the 8080, Z80, and 8085 have data bus and address bus outputs that are 3-state. These 3-state devices can pass normal logic levels of 1 or 0, and they can also be forced into a third state, in which their outputs appear to be very high impedance loads on the bus. Thus, they no longer sink or source current; they are, in effect, "disconnected from the bus." The third state allows external devices to obtain the use of the address and data bus lines when the computer's operations are "suspended," and its outputs removed from the bus lines. The microcomputer's bus signals can be controlled easily to force them into this third state. On the 8080, there is a HOLD input. When this input is asserted at a logic 1, it forces the microprocessor to complete its current operation and then place its data bus and address bus outputs in their third state. The microprocessor outputs a handshaking hold-acknowledge (HLDA) signal to indicate that it has indeed placed these signals in the high impedance state.

External devices are synchronized so that they will not attempt to use the address and data bus lines until they receive the hold-acknowledge signal from the 8080. In general, these same devices have generated the bus-use request signal or hold signal that indicates to the microprocessor that they wish to use the buses.

In many microcomputer systems, additional buffers are used between external devices and the address bus and data bus connections to the microprocessor chip, itself. If this is the case, it is important that these buffers

FREE! SPEED READING COURSE.

DECITEK's free SPEED READING COURSE gives full details on new Model 262D9 desktop punched tape reader. (The model that reads 300 cps and recognizes XON and XOFF ASCII characters as well.)

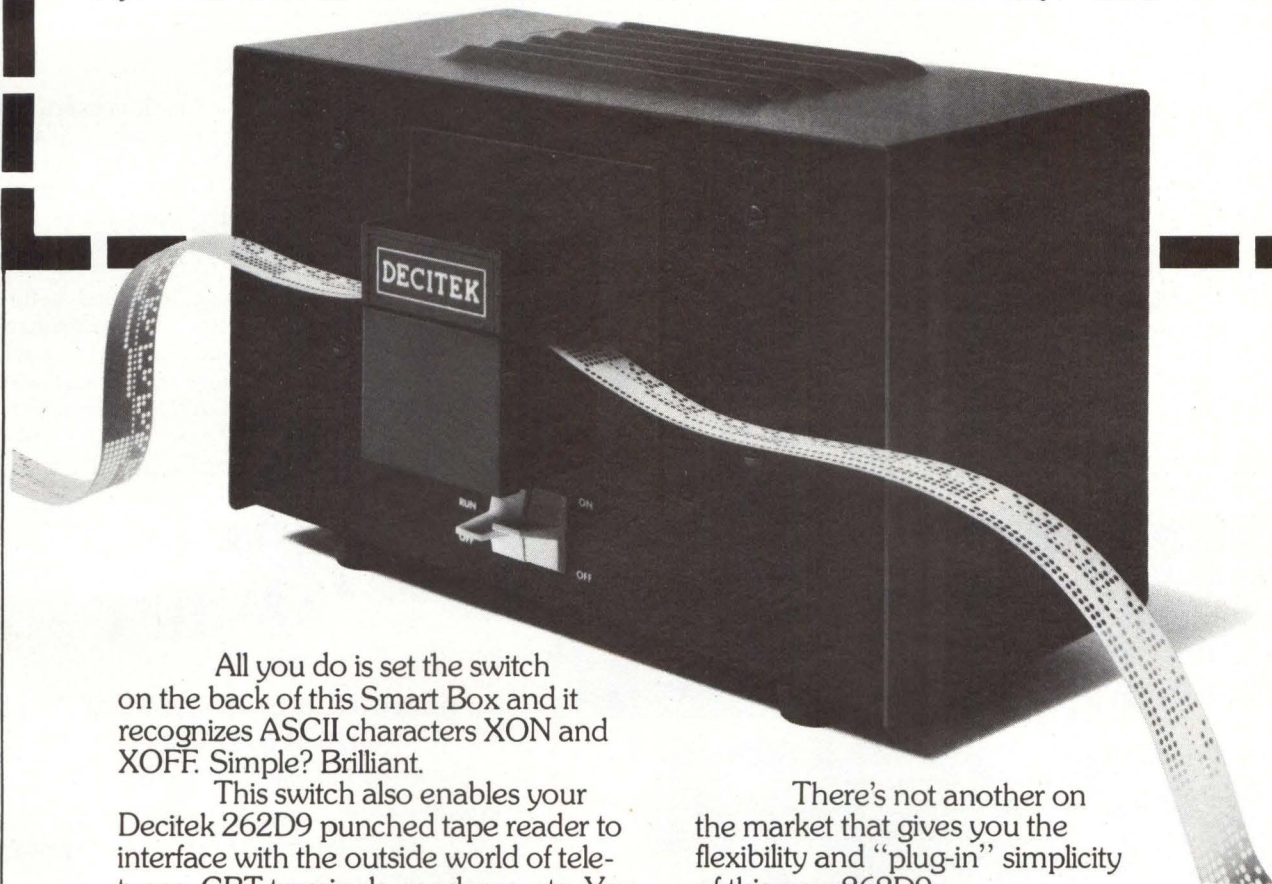
Please rush details. I understand this brush-up course on the latest in tape readers does not obligate me in any way.

Name _____ Position _____

Firm _____

Street _____

City _____ State _____ Zip _____



All you do is set the switch on the back of this Smart Box and it recognizes ASCII characters XON and XOFF. Simple? Brilliant.

This switch also enables your Decitek 262D9 punched tape reader to interface with the outside world of teletypes, CRT terminals, modems, etc. You select it, the Smart Box does it without internal programming by jumpers.

Then, using the second mode selector on the rear panel, you can program transmission rate (from 110 to 9600 baud), word length, parity and number of stop bits.

There's a lot more to this intelligent box. Dual-sprocket drive, 25,000 hour light source with fiber optics and stepper motor drive — that's a lot of tape reader. Add-on fan-fold boxes and 19" wing adapters provide installation versatility if you need it.

There's not another on the market that gives you the flexibility and "plug-in" simplicity of this new 262D9.

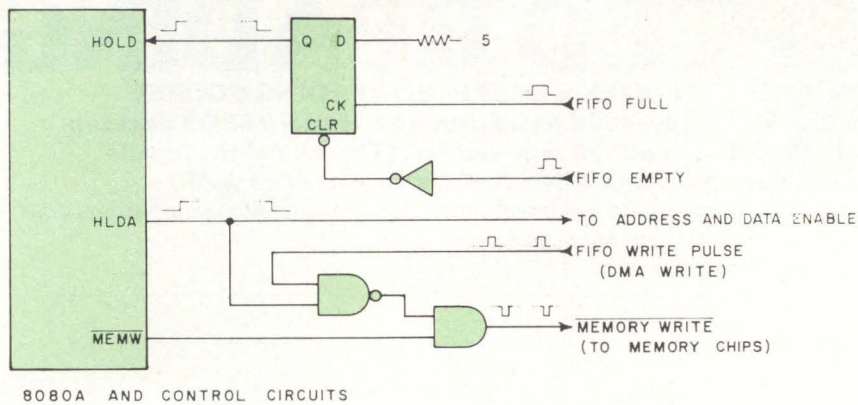
That's a fact. Another fact that will interest you is the reasonable cost of this improved Smart Box. So, do the smart thing. Mail the coupon for the FREE Speed Reading Course. Or, if you're in a hurry, call (617) 366-8334. Get the facts over the phone.

When reading matters

DECITEK

A Division of Jamesbury Corp.

129 Flanders Road, Westboro, Massachusetts 01581



DMA interface. Block diagram relates interaction of elements involved in application that uses programmable up/down counters for 16-bit address information during DMA transfer, along with FIFO buffer memory for data to microcomputer's memory

sense the hold-acknowledge signal and place their respective outputs in the third state, too. In the hold state, the central processor and its associated buffer circuitry must all be disconnected from the address and data buses.

External devices that are configured for DMA transfers generally have their own registers that provide address information, usually 16 bits. These address registers also have 3-state outputs that are normally disabled. They are only enabled, or turned on, when the microprocessor is in the HOLD state. They can then utilize the address bus to address the particular memory location to or from

which the data are transferred. The data path between the external device and the memory chips has also been placed in the third state, so it, too, can be used for the transfer of data, in this case the 8-bit value that is to be transferred between the external device and the location that is being addressed by the external 3-state address registers.

One other important detail must be discussed before the actual data transfer can take place. In most microcomputer systems, the reading-from and writing-to operations are controlled by two signals, memory read ($\overline{\text{MEMR}}$ or $\overline{\text{MR}}$) and memory write ($\overline{\text{MEMW}}$ or $\overline{\text{MW}}$). These signals



SUPER SMART

ALPHANUMERIC DISPLAY SUB-SYSTEMS

Completely Designed and Ready to Use

- 10, 20, 32 and 40 character/column models.
- All drive, interface and refresh circuitry included at no extra charge.
- Evaluation Kit containing full assortment of filter types and colors, bezels and mounting hardware available.
- Bright, sharp, highly readable characters, even in daylight, with proper filtering.
- Complete software manual, mounting diagrams and interface schematics. Technical advice from our systems engineers - who have already solved many of the problems you are facing.
- Vacuum fluorescent technology for low power consumption.

CALL NOW FOR A DEMONSTRATION

UNITED STATES
Digital Electronics Corp.
(415) 342-8333

CANADA
Talma Electronics Ltd.
(416) 883-4333

Local representation throughout the U.S.

ITALY
Auriema
02/430 602

FRANCE
Metrologie
791.44.44.

W. GERMANY/AUSTRIA
bitronic GmbH
(089) 470-2098

AUSTRALIA/N.Z.
Romtech Pty. Ltd.
(02) 601-4511

U.K./BENELUX
Dialogue Micro Systems
(06284) 73 716

SWITZERLAND
Memotec AG
(063) 2 61 81

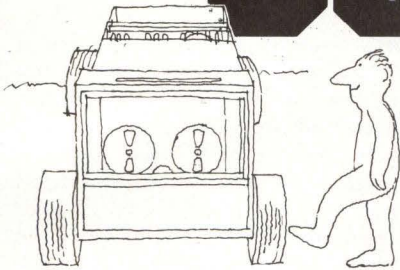


DIGITAL ELECTRONICS CORPORATION

A DIVISION OF CHEMETRICS CORPORATION
197 AIRPORT BLVD., BURLINGAME, CA 94010
(415) 342-8333 TELEX: 334422 CHEMETRIC BRGM

FOR READABILITY, STRIKING APPEARANCE & COST EFFECTIVE DESIGN

TEST DRIVE OUR DRIVE.

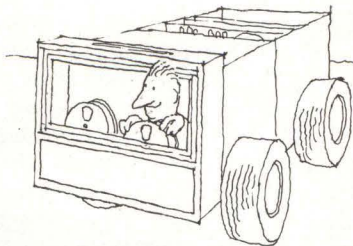
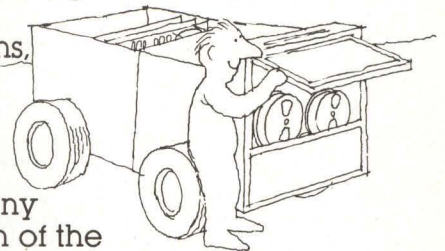


Not the tire-kicking, door-slamming kind, of course. But all the tests that quality cartridge drive should have to pass. Then you'll see why OEMs have been choosing our drives for their systems for more than five years now.

Go ahead. Run our DCD-3 through thousands of cycles. Even under changing environmental and load conditions,

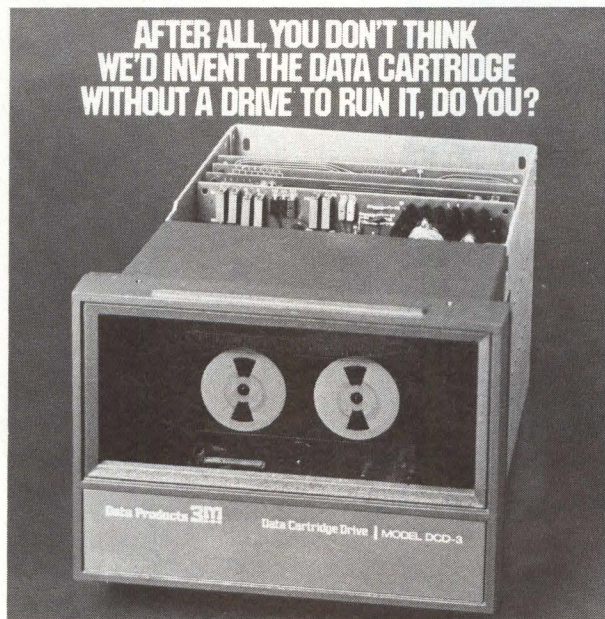
its long term speed accuracy will always stay the same. That's because we build it with a unique, motor-servo unit, complete with a tachometer, that can take punishment like that without any change in performance.

Or, put our DCD-1 through its paces. You'll never have any track location problems. Because it records over the total width of the tape. Which means the system is virtually immune to loss of signal from transient error.



For more good reasons why we think our drives out-perform any others, just take a look at the other products in our Data Products line.

If you have an OEM or systems requirement, why not take us up on our offer? To arrange a test drive of one of our drives, call (612) 733-8892, or write: Data Products, 3M Company, 223-5E, St. Paul, MN 55101.



3M

may or may not be available with 3-state outputs. In some systems where a control logic section has been constructed with discrete integrated circuits (ics), these two signals probably will not have 3-state outputs. When a system controller chip has been used, the outputs are probably 3-state in nature. In either case, it is easy to gate an 8080 generated read or write pulse with the corresponding one generated by the microprocessor chip. In this way, either the external hardware or the microprocessor can generate a read or write pulse. Since the 8080 processor is not operating or executing program steps while it is in the HOLD mode, it cannot generate a read or write signal. Using the HLDA signal to enable the read and write pulses generated by the external device causes the proper pulses to be generated by the 8080 in the normal mode and by the external device in the HOLD mode.

While the DMA interface thus far does not seem to be too useful (transferring only one 8-bit data word to a single location), it does illustrate the simplicity of constructing a DMA interface. In most situations, however, a block of data values are transferred between the memory and an external device. Note that the transfer may be in either direction, ie, from a high speed data acquisition device to the computer's memory, or from the computer's memory to a high speed data storage device, such as a floppy disc.

In one application, sn74193 programmable up/down counters provided the 16-bit address information during the DMA transfer and a first in, first out (FIFO) buffer memory provided a block of data to the microcomputer's memory. Some simple control logic generated a write pulse (MEMW) and then incremented the address (count)

present at the counters. The user preset the starting address, at which the block of data was to be stored, by using a series of switches. Once a complete block of data accumulated in the 256-byte long FIFO memory, external circuitry detected the "FIFO FULL" condition and initiated the request for use of the bus, asserting the HOLD line to the 8080. When the microprocessor acknowledged the hold condition with the HLDA signal, the data were transferred from the FIFO memory to the microcomputer's main read/write (R/W) memory at a rate of 500k bytes/s, or one byte every 2 μ s. This data transfer rate could have been increased at least four-fold, but it was unnecessary to do so in this particular situation. The Figure shows a block diagram of the interface that controlled the DMA data transfers.

Another use of the DMA interfacing technique is found in front panel control circuits. Control panels are often provided on microcomputers so that an operator can address memory locations and examine their content. The operator may elect to "deposit" new data in one or more memory locations, again through the use of a front panel. Such a control system is easily constructed through the use of the DMA technique, since a 16-bit 3-state buffer supplies the address and eight indicators show the state of each bit in the addressed memory location. Eight logic switches load new data into a location and two control switches, EXAMINE and DEPOSIT, are configured to generate the memory-read and memory-write control pulses, respectively. Additional embellishments to such a simple circuit can automatically increment or decrement the 16-bit memory address, among other functions.

There are, however, some notes of caution when contemplating the use of DMA. The 8080-type processors are locked out of performing any program steps while they are in the HOLD state; they cannot respond to interrupts while they are being controlled by an external DMA based device. The DMA based devices themselves stop the processor's operation, so that it is often difficult to predict when they will demand the use of the buses, thus halting complex, and perhaps time dependent, operations.

Some processors such as the mc6800 series devices require that the DMA based devices relinquish control of the bus on a regular basis. The 3-state control (TSC) line in 6800 based systems can only be asserted for periods of 5 μ s at a time. Likewise, in systems that use dynamic R/W memory devices, DMA based devices cannot continuously use the address and data buses for more than 1 ms or so, since the external control logic must be able to use the address and data buses to refresh the dynamic memory cells on a regular basis.

Because DMA interfacing is misunderstood, the technique is often overlooked by microcomputer users. When users do understand it, they often consider it difficult to implement. It is our conclusion that DMA devices provide a readily accessible alternative to other interfacing schemes when high speed data transfers are required. New DMA controller chips, such as Intel Corp's 8257, provide much of the needed control circuitry in a small ic package. While such devices often simplify the required circuitry, they need additional control software to perform initialization and other steps. Those who wish to design a DMA controller should start with a discrete ic approach to the interfacing task.

Pascal Compiler



for Data General Computers

- Written in Pascal.
- Generates Nova[®] Code.
- Over twice as fast as Fortran IV.
- Includes all Source Code.
- Available for RDOS, AOS, and DOS.
- \$975 for RDOS version on mag tape.

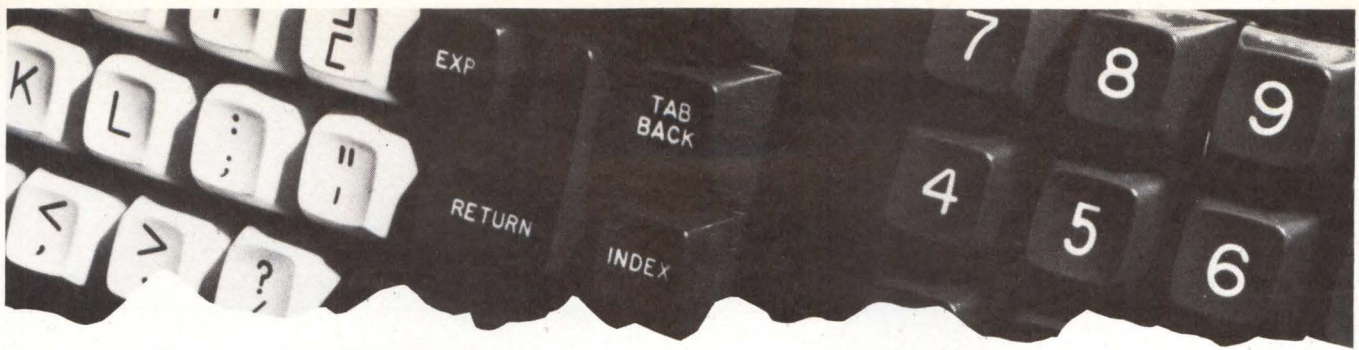
Rhintek, Inc. COMPUTER ENGINEERING

P.O. Box 220, Columbia, Maryland 21045, (301) 730-2575

[®] Nova is a trademark of Data General Corp.

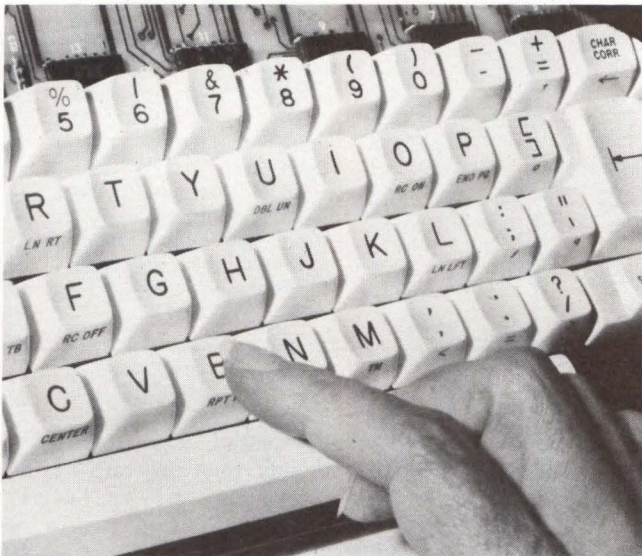


This article is based, with permission, on a column appearing in *American Laboratory* magazine.



the "Dumb Keyboard"

for smart designs



"Dumb" can be smarter than "intelligent"

In 1975 Cortron developed and released a new keyboard principle of design that has given many design engineers a very real competitive edge. It is so simple we call it the "ABC" principle (Address Binary Code). If you haven't heard of it we suggest you read on to find out what many of your competitors are already doing. There is an alternative to the expensive "intelligent" keyboard design. We manufacture both, but we feel dumb is generally smarter.

"ABC" principle An address encoded keyboard simply outputs a unique 8 bit binary code for each key station. This code directly enters the main system which, through various software routines, determines what each specific key switch is and does. This provides a keyboard that is both simple and versatile. Cortron has various subsets of this principle to give the designer "trade-offs" between system and keyboard such as PROM conversion, etc. Call us before you design, so these "trade-offs" can be discussed and your information bank complete before costly designs are finalized.

Upstroke/downstroke We also supply a unique "ABC" for both key depression and release. Thus, not only can you determine what character, function, etc. you want, you can also control which keys auto repeat — any or all—and also which keys are mode control.

Advantages Lower keyboard cost: Eliminates electronics on board with little or no added cost to system.

Versatile: One basic keyboard can be customized for virtually any customer configuration with only software or PROM conversion and key top change.

Inventory savings: Now you can satisfy all those special foreign language and function requirements with one keyboard and a stock of key tops.

Fast turnaround: No more 20 week wait for a new LSI mask for the special requirements. Virtually "off-the-shelf" availability.

Reliability: Less electronics on keyboard means improved reliability and long term cost savings to your system.

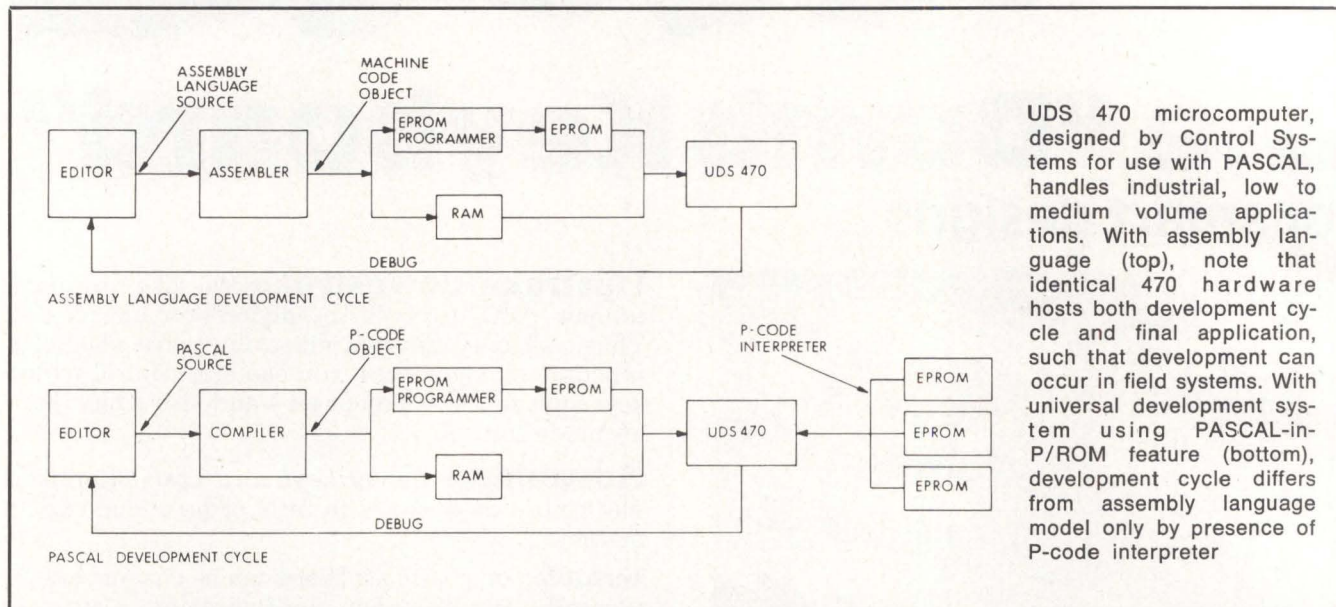
Call us today to find out why most new designs utilize the "ABC" principle. We will explain the various "trade-offs" and costs of keyboard design and even help with your software routines, if required.

Of course, if you feel intelligent is smarter for your system, we can also aid you in those design decisions. Cortron has developed and manufactured micro-processor based keyboards using the most popular single chip microprocessors. We have the modern system development aids and staff capability which has allowed us to write the highly flexible keyboard handling routines for the cases when "intelligent" is intelligent. For full details and literature, call or write: CORTRON, A Division of Illinois Tool Works Inc., 6601 West Irving Park Road, Chicago, Illinois 60634. Phone (312) 282-4040. TWX 910-221-0275. Toll free line: 800-621-2605.



THE KEYBOARD PROFESSIONALS

Microcomputer's Use of PASCAL in P/ROM for Dedicated Applications Speeds Development Cycle



UDS 470 microcomputer, designed by Control Systems for use with PASCAL, handles industrial, low to medium volume applications. With assembly language (top), note that identical 470 hardware hosts both development cycle and final application, such that development can occur in field systems. With universal development system using PASCAL-in-P/ROM feature (bottom), development cycle differs from assembly language model only by presence of P-code interpreter

A rugged, industrial quality microcomputer, UDS 470 offers PASCAL as an alternative to assembly language and BASIC for low and medium volume applications requiring power and fast development. This version of University of California at San Diego PASCAL is designed for ROM or P/ROM operation in dedicated applications.

The PASCAL-in-P/ROM feature makes high level programming as easy as assembly language programming. A PASCAL program is compiled, rather than assembled, and compiler output (P-code) is burned into P/ROM or EPROM (see Diagram). Once application software is de-

veloped, one or two cards of self-booting ROMs or EPROMs can hold the PASCAL runtime code plus application software at low cost. With faster execution due to the P-code interpreter, the general purpose language features user defined data types, multiple precision integer and floating point arithmetic, and optional transcendental functions; it also is block structured, self-documenting, and free-format.

The rackmountable system for OEMs uses a 6800 microprocessor, but can be upgraded to the 6809 or 68000 when they become available. Control Systems, Inc, Microsystems

Div, 1317 Central, Kansas City, ks 66102 intends the computer to be machine independent. A standard package for development work includes the CPU with 1k RAM and 2k EPROM, serial I/O port with automatic reset, and Vcc monitor; 32k RAM; 16k EPROM; double-density 5.25" (13.3-cm) floppy discs holding 204k bytes/side, with interface; power supply; and case. Software consists of UCSD PASCAL, 6800 monitor and DOS, and utility and test programs—linker, universal assembler, and editors. Integral CRT/keyboard, graphics (bit mapped), and various programs are optional.
Circle 410 on Inquiry Card

Board Set With 2-Byte Fetch and Store Doubles Capacity of S-100 Bus

An S-100 16-bit microcomputer system consists of the 8086 CPU with eight levels of vectored interrupt on one board; a combination of monitor ROM, serial I/O, and parallel I/O on a board; and an unpopulated 4k-byte static RAM board. They all conform to the proposed IEEE signal protocol and operate at 4 MHz. When

combined with a terminal and standard S-100 bus, the boards form a standalone computer.

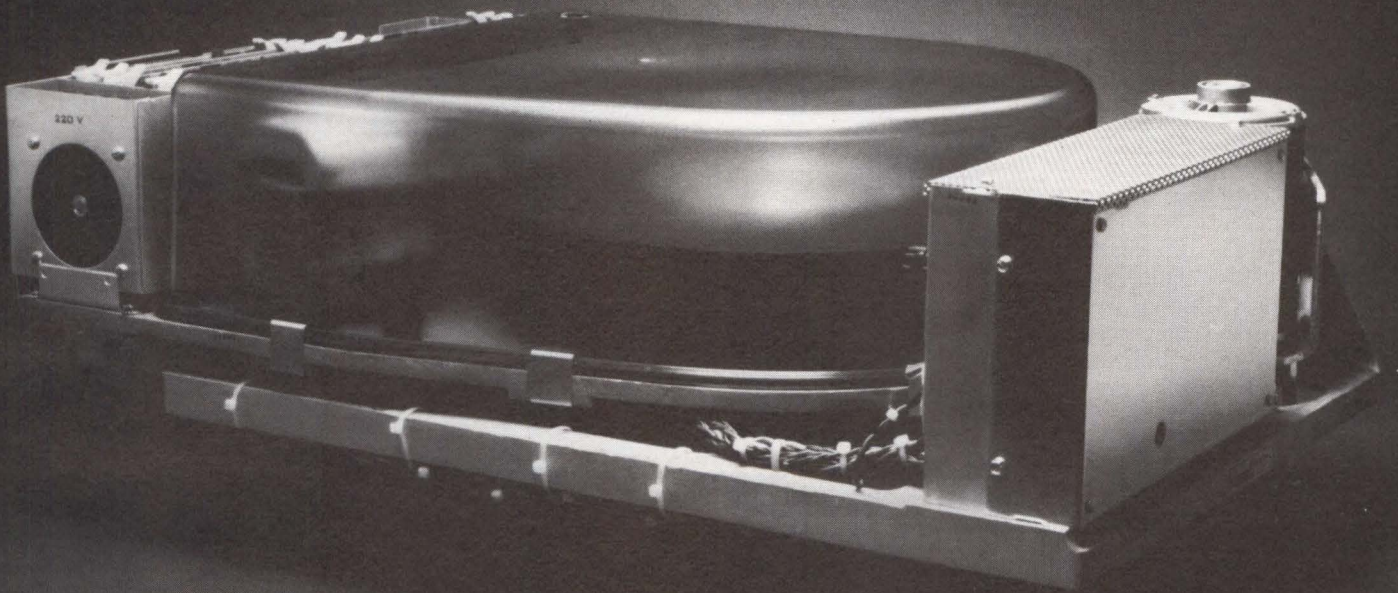
Developed by TecMar, Inc, 2314 Greenlawn Ave, Cleveland, OH 44122, the set complies with proposed IEEE 16-bit S-100 protocol providing fetch and store of two bytes at a time, doubling the previous capacity of the bus. Memory cards that fetch or store two bytes at a time must be used. Byte-at-a-time memory mapped I/O preserves compatibility

with previous devices. Word-at-a-time memory mapping may be used since I/O mapping is provided. Using a 20-bit address allows a 1M-byte address space. Use of address space beyond 64k bytes requires all memory to also conform to the proposed S-100 extended address protocol standard.

Monitor ROM is contained on two ICs with automatic power-on. A serial I/O port on the ROM-I/O board has a switch selectable baud rate from

Memorex OEM.

We deliver product not promises.



In the past 24 months we have delivered more Winchester type, OEM drives than all of our competitors put together. Here's why:

SUPERIOR DESIGN—The 601 is a superior design based on an investment of over \$25 million in Winchester technology.

HIGH RELIABILITY—The sealed environment of the 601 is expected to yield MTBF's in excess of 8,000 hours. Using an 801 tester, the MTTR is only one hour.

REDUCED INFANT MORTALITY—A special quality control program at Memorex is set up to screen out early failures that are expensive and embarrassing to OEMs.

LOW COST—Other manufacturers may quote lower initial prices, but, when it comes to cost of ownership over the life of the product, the Memorex® 601 disc drive is clearly the best value.

OEM SUPPORT—An extensive, world-wide service and support network assures you that help will be there when you need it.

IMMEDIATE AVAILABILITY—The 601 is in volume production and evaluation units are readily available.

For more information, or to get your hands on a 601, call or write.

MEMOREX

GENERAL SYSTEMS GROUP (OEM DIVISION), SAN TOMAS AT CENTRAL EXPRESSWAY, SANTA CLARA, CA 95052. BOSTON (617) 890-0700
NEW YORK (201) 325-0164; DETROIT (313) 354-4511; LOS ANGELES (714) 891-2541; DALLAS (214) 258-3510; SAN FRANCISCO (408) 987-1373

© 1979 MEMOREX CORPORATION. Memorex is a registered trademark of Memorex Corporation.

CIRCLE 87 ON INQUIRY CARD

183

110 to 4800 asynchronous or up to 50k synchronous. The interface operates in EIA RS-232 mode or 20-mA current loop. The board also has 24 lines of parallel I/O. The 3-board set can be purchased for \$995. Additional unpopulated memory cards are \$35 each.

Circle 411 on Inquiry Card

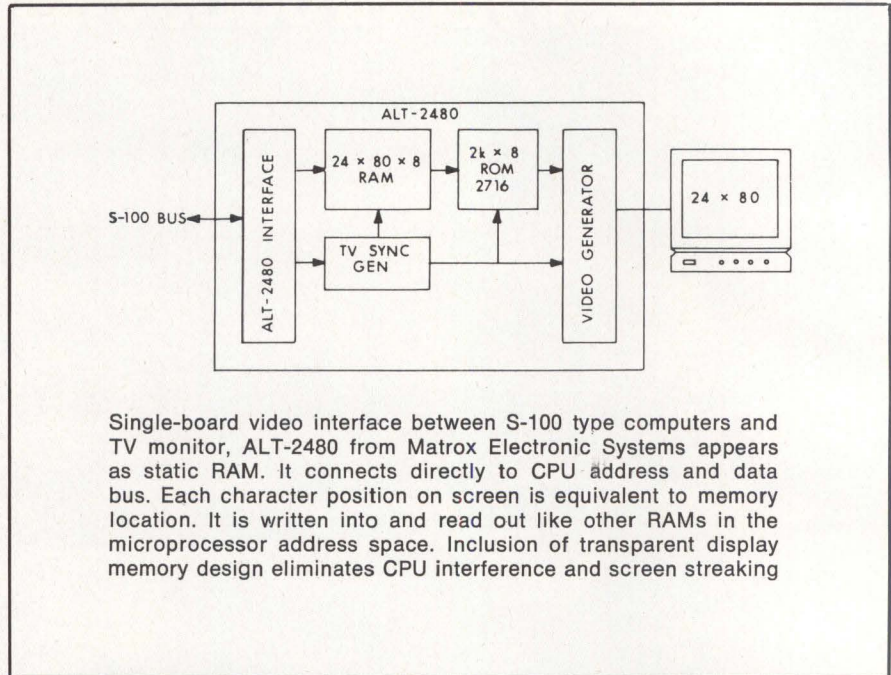
Transparent Memory Eliminates CPU Halting and Display Streaking

Transparent memory, the design concept incorporated into the ALTR-2480 24 x 80 character alphanumeric video interface card for the S-100 bus, solves the memory contention problem common to all CRT displays. This occurs because the display refresh memory must be accessible both by the CRT controller for CRT refresh and by the CPU.

Standard solutions have been to use the video RAM approach or the DMA approach. The former allows the refresh memory to be switched between the CRT controller and CPU using data multiplexers and 3-state buffers. The problems encountered are streaks or glitches on the screen, and restricted speed of CRT screen updates. The DMA solution slows down the CPU and adversely affects system timing since the CRT must be refreshed constantly.

The transparent memory design by Matrox Electronic Systems Ltd, 2795 Bates Rd, Montreal, Quebec H3S 1B5, Canada eradicates these problems. The CPU accesses the refresh memory at any time, the display is glitch free, and the CPU is never interrupted. The general method does not rely on the timing characteristics of a particular CPU, allowing its use with most mini- and microcomputers. A multiplexing technique permits nonconflicting access by both the CRT controller and CPU.

The memory feature has been incorporated as well into three industry standard buses—the Intel/National SBC-80 (MSBC-2480 board), Digital Equipment Corp LSI-11/2 (MLSI-2480), and Motorola EXORCISER (EXO-2480)—at no extra charge. All cards in the series feature memory mapped addressing. This allows full power of the processor's instruc-



Single-board video interface between S-100 type computers and TV monitor, ALT-2480 from Matrox Electronic Systems appears as static RAM. It connects directly to CPU address and data bus. Each character position on screen is equivalent to memory location. It is written into and read out like other RAMs in the microprocessor address space. Inclusion of transparent display memory design eliminates CPU interference and screen streaking

tion set to be used for display data manipulation. The 128-location character generator features the full ASCII set with upper/lower case characters and limited graphics. A 5 x 7 dot matrix in a 6 x 10 dot cell provides noninterlaced flicker free display. Models meet both American and European TV standards and operate with a single 5-V power supply.

Features of the ALTR-2480 include a user programmable character gen-

erator (2716 EPROM), external/internal sync, normal/inverse/blink control, and a 500-ns access time. It combines with the ALT-256 or ALT-512 graphics controller cards, which have variable resolutions ranging from 256 x 256 to 512 x 256 points. Prices of the video interface card are \$295 in single quantities and \$256 in 100 quantities.

Circle 412 on Inquiry Card

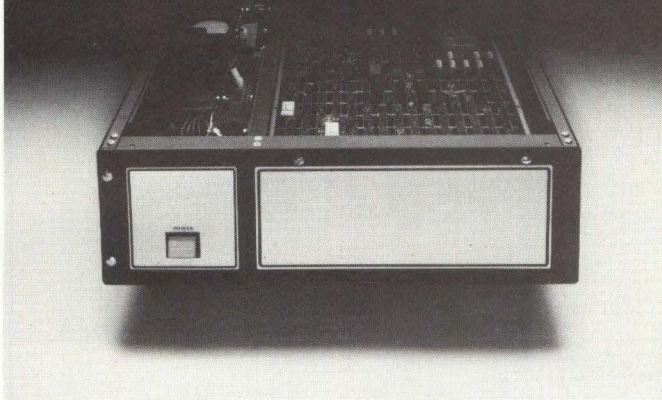
Combined Microprocessor Cards Form S-100 Bus Multiprocessor System

SLAVEMASTER 2650 is an S-100 bus multiprocessor system that uses all available bus time. Multiprocessor control is implemented with two Signetics 2650 microprocessors through one ribbon cable interconnect; one processor is identified as slave and the other as master. However, the only functional difference in the two is that the master can stop, reset, or jump the slave. A synchronizing circuit allows the two microprocessors to operate with fetch/execute cycles interleaved. Precise single processor timing is maintained; once synchronized, the two processors do not interact.

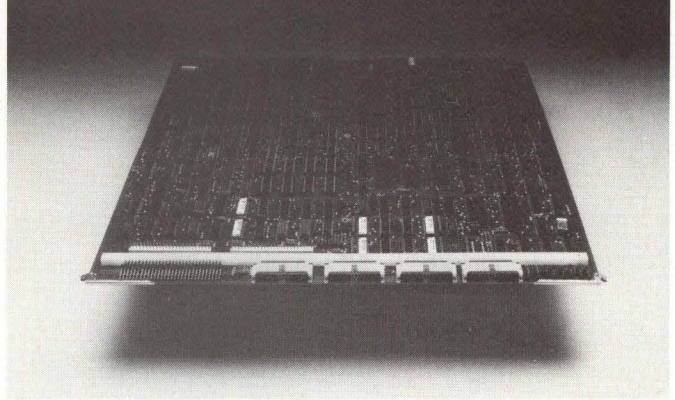
Various configurations in which the cards from Victoria Micro Digital, 401 Dundee St, Victoria, TX 77901 may be used are two for multiprocessing, one as a standalone microcomputer, and they may have an RS-232 or 20-mA current interface. Realtime control, parallel processing, and frontend preprocessing are possible applications; the most practical, however, may be its use as a development system. The master is the dynamic debugging tool; it changes and monitors any of the slave's S-100 resources while remaining fully transparent.

Each card has 4k of 2708 EPROM sockets; one serial I/O port; 20-mA and RS-232 voltage levels; 110, 300, 600, or 1200 baud; one Kansas City cassette interface; eight vectored

**MSC Makes
The Best Controller
You'll Ever See.**



Or Won't.



On the left, the cabinet model of our 1000 Series disk-based controller. On the right, our host resident version of the same series. But left or right, a lot of folks for a lot of reasons think of the 1000 Series as "the consummate controller."

It's simply got so much more going for it.

More Functional. More Versatile. More Reliable. More Maintainable.

In short, the 1000 Series by MSC is a more sensible controller buy. Because that's the way we designed it.

Powerful. So that users can access up to 1200 megabytes of on-line storage at data transfer rates of up to 1.2 megabytes/sec.

Flexible. So that users aren't locked into one manufacturer's drive or one particular drive technology. The MSC 1000 Series accommodates both removable and Winchester fixed media — in Ampex, Memorex, CalComp, CDC, ISS, Microdata, Okidata, Kennedy and Fujitsu drives.

Modular. Simple. Smart. So that users can easily upgrade the 1000 Series in the field. And so that maintenance and downtime will be negligible anyway. Thanks to the single board construction, low parts count, on-board microdiagnostics, all quality components and low stress design that account for a phenomenal MTBF.

More Features Up Front. More Experience Behind It.

The MSC 1000 Series boasts a history of proven performance in a wide range of minicomputer operating systems. As a single, host resident board in the Nova and Eclipse,

as well as with Interdata. And as a separate cabinet in the HP3000 and 21MX. IBM Series/1. PDP-11. Microdata 1600.

In the four years that MSC's 1000 Series has been at work in the field, the installed base has grown to over 2000 units. So that when we talk reliability, maintainability, power and performance, it's more than just talk.

And when we talk operational features like error correction, sophisticated channel techniques, automatic self-test, overlap seek capability and logical to physical drive correlation, we are talking about *a commitment to incorporating innovation in all of its scope and each of its details into every product we design and manufacture.*

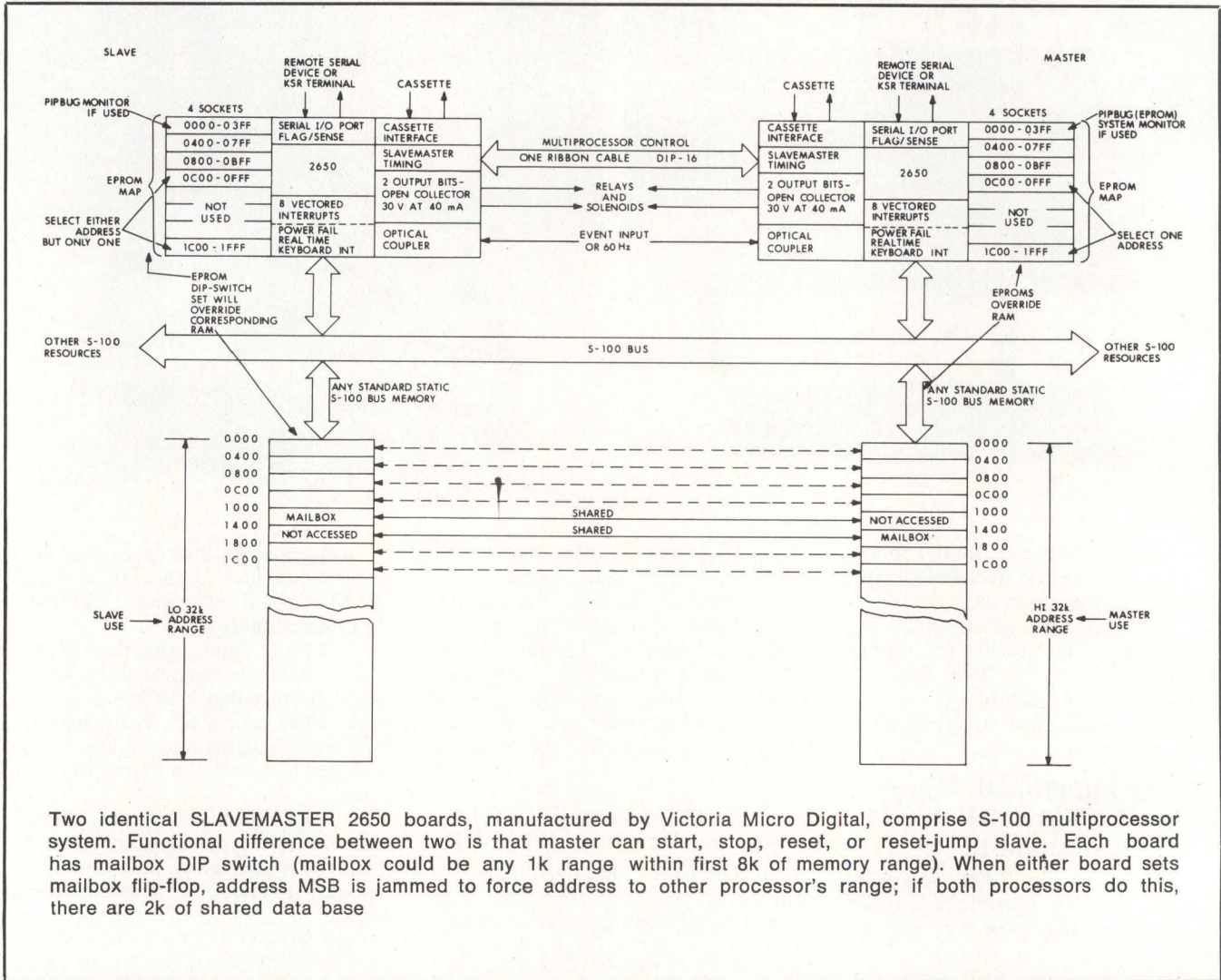
The MSC 1000 Series disk-based controller is a measure of that commitment.

**More Information:
(408) 733-4200.**

MSC. Microcomputer Systems Corp.
432 Lakeside Drive, Sunnyvale,
Ca. 94086. TWX 910-339-9359.

**One
More Miracle
From Microcomputer
Systems Corporation.**

The 
**MSC 1000
Series.**



Two identical SLAVEMASTER 2650 boards, manufactured by Victoria Micro Digital, comprise S-100 multiprocessor system. Functional difference between two is that master can start, stop, reset, or reset-jump slave. Each board has mailbox DIP switch (mailbox could be any 1k range within first 8k of memory range). When either board sets mailbox flip-flop, address MSB is jammed to force address to other processor's range; if both processors do this, there are 2k of shared data base

priority interrupts; and keyboard, realtime clock, and power fail interrupt driven realtime functions. Any S-100 bus mainframe with static type RAM accommodates these cards. Three DIP plug connectors on each card connect a serial terminal, cassette recorder, and slave to master interconnect ribbon cable.

Two methods of sharing data bases are the mailbox with split memory mode and common memory mode. In split mode each processor is restricted in its own 32k S-100 bus memory range. The DIP switch addressed mailbox shares data. In effect, each processor can access a 1k block of the other's memory, giving a possible 2k mailbox. During start up or initialization, the master downloads through the mailbox prior to

reset/jumping the slave. In common mode, both processors may execute anywhere in physical memory and have access to all data in memory.

Software being marketed with the system are Signetics PIPBUG and LITTLE ASSEMBLER, optionally available on 2708 EPROM. PIPBUG is a system monitor program that replaces typical front panel functions. It communicates through the serial I/O port to a serial terminal device; it is self-synchronizing to 110 or 300 baud, and may be changed to 600 or 1200 baud by altering one RAM constant. The LITTLE ASSEMBLER functions as an immediate machine code generator, using all Signetics symbolic op codes. It features error detection as well as pseudo-ops for ASCII string entry and changing

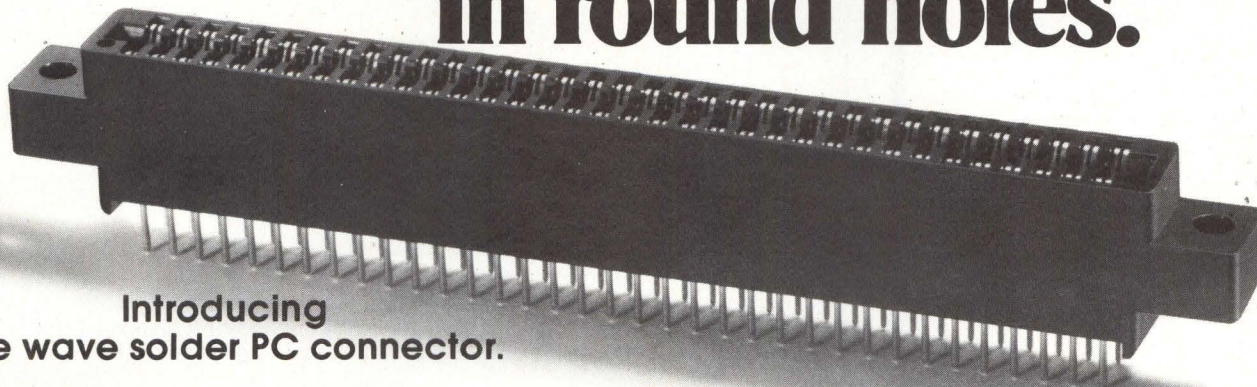
origin address. EDITOR-2650 and RTC-2650 (realtime control) will be available soon on cassette or 2708 EPROM. The boards cost \$269 assembled, \$198 in kit form; software costs \$25 each.

Circle 413 on Inquiry Card

Graphics Generator Creates Moving Displays Needing Realtime Update

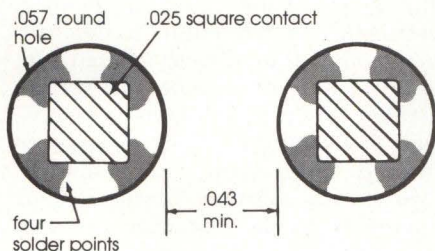
The single-board RG-SBC graphics generator for Intel's SBC Multibus™ produces a composite TV output signal for display on a standard 525-line monitor. The instruction set with seven instructions facilitates program-

No more square tails in round holes.



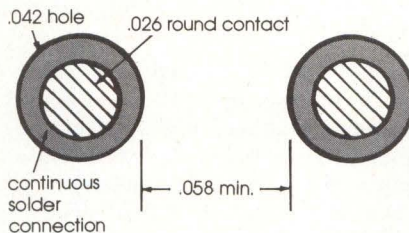
Introducing the wave solder PC connector.

What an electronic design engineer will make-do with in a pinch is astonishing. For example — converting wire wrap* PC connectors to wave solder.



How it's done: you saw off the square .025" tail and push it through a .057" round hole in the PC board. You get only 4 contact points for solder. And there's room for only one tracing between holes. But, so what...it works.

At last — The obvious answer



Our own design engineers, not afraid of doing the obvious and simple thing, have done just that. They've taken a series of our PC wire wrap connectors — and given them .026" round tails. Everything else stays the same: the insulator, semi-bellows contacts, pin and row spacing.

So what?

So — the .026" round pin slips into a .042" round hole in your PC board for an excellent solder connection. So — you can now get multiple tracings between rows.

We have two tail lengths: a .200" short one and a .250" longer one to take the AS400 Solderpak** System. These are available in connectors with contacts on .100", .125" and .156" centers, and in layouts from 6 to 50 positions.

Use our coupon and we'll send you all the details.

There's more. There are some things we haven't told you — including materials and other details you need to know. Ask us for the literature.

NAME _____

TITLE _____ TELEPHONE _____ EXT. _____

COMPANY _____

ADDRESS _____

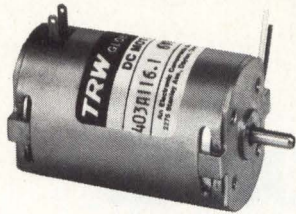
CITY _____ STATE _____ ZIP _____

 **Viking**
CONNECTORS

21001 Nordhoff Street, Chatsworth/CA 91311 U.S.A.

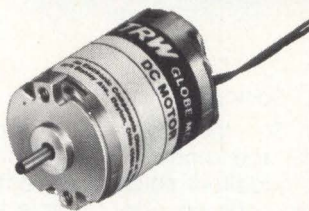
(213) 341-4330/TWX: 910-494-2094

*A registered trademark of the Gardner-Denver Company. **A registered trademark of the Raychem Corporation.



New 1½" DC motor-tach cuts noise in your system

With the new EM-15 motor-tach, you don't have to run AC power lines into noise-sensitive areas of your system. Rated voltage: 6 to 24 v.d.c. Tach frequency: 8 cycles/rev. AC tachometer is brushless. You get accurate speed at low cost.



Low-cost DC PM motor only 1¼" in diameter

Our economy EM-13 motors have many of the features of our quality military motors. Torque constant: 2.6 oz. in./amp for 12 v.d.c. version. Voltage constant: 1.92V/K rpm. Available in 6, 12, or 24 v.d.c. versions. Tooled for high-volume production.



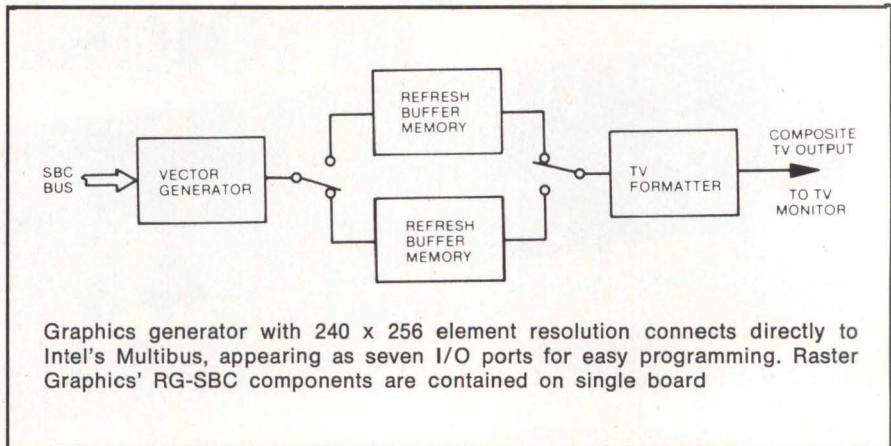
In a hot spot? Cool it with our fans and blowers

Cool your critical components with our miniature DC fans and blowers. Power source 12 to 115 v.d.c. 10 to 315 cfm free air. Propeller, centrifugal, tubeaxial, vaneaxial, and propaxial types. Diameters 1.25" to 5.75".

TRW GLOBE MOTORS

Dayton, Ohio. (513) 228-3171. Distributed by Hall-Mark, Hamilton/Avnet, Jaco, Pioneer.

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS



Graphics generator with 240 x 256 element resolution connects directly to Intel's Multibus, appearing as seven I/O ports for easy programming. Raster Graphics' RG-SBC components are contained on single board

ming in assembly, BASIC, or other high level language. Moving displays requiring realtime update can be created. Two stored and two erase modes of operation are possible.

Features are 240 x 256 element resolution, a vector generator, dual refresh memories, composite tv output, and stored and nonstored modes of operation. Manufactured by Raster Graphics, po Box 23334, Tigard, or 97223, the generator plugs into the

bus and appears as seven I/O ports for programming. Each single-byte instruction is written to a different I/O port within a user selected I/O page. Tasks of creating the vector, writing it into refresh buffer memory, and producing the tv signal are performed transparently in hardware. Application software covers symbol rotation, circle generation, and ASCII character generation.

Circle 414 on Inquiry Card

Communications Option For Analyzer Extends Diagnostic Capability

Capabilities of the MicroSystem Analyzer (μ SA) have been enhanced by a multipurpose communications option that enables downloading of test programs, production testing of microprocessor based products, and infield service testing. Field service personnel can perform onsite diagnostic testing at remote field maintenance and depot/repair facilities over standard telephone lines; this allows a specialist to acquire full diagnostic control for troubleshooting the system under test (SUT). Thus, the test P/ROM inventory required in the field is reduced.

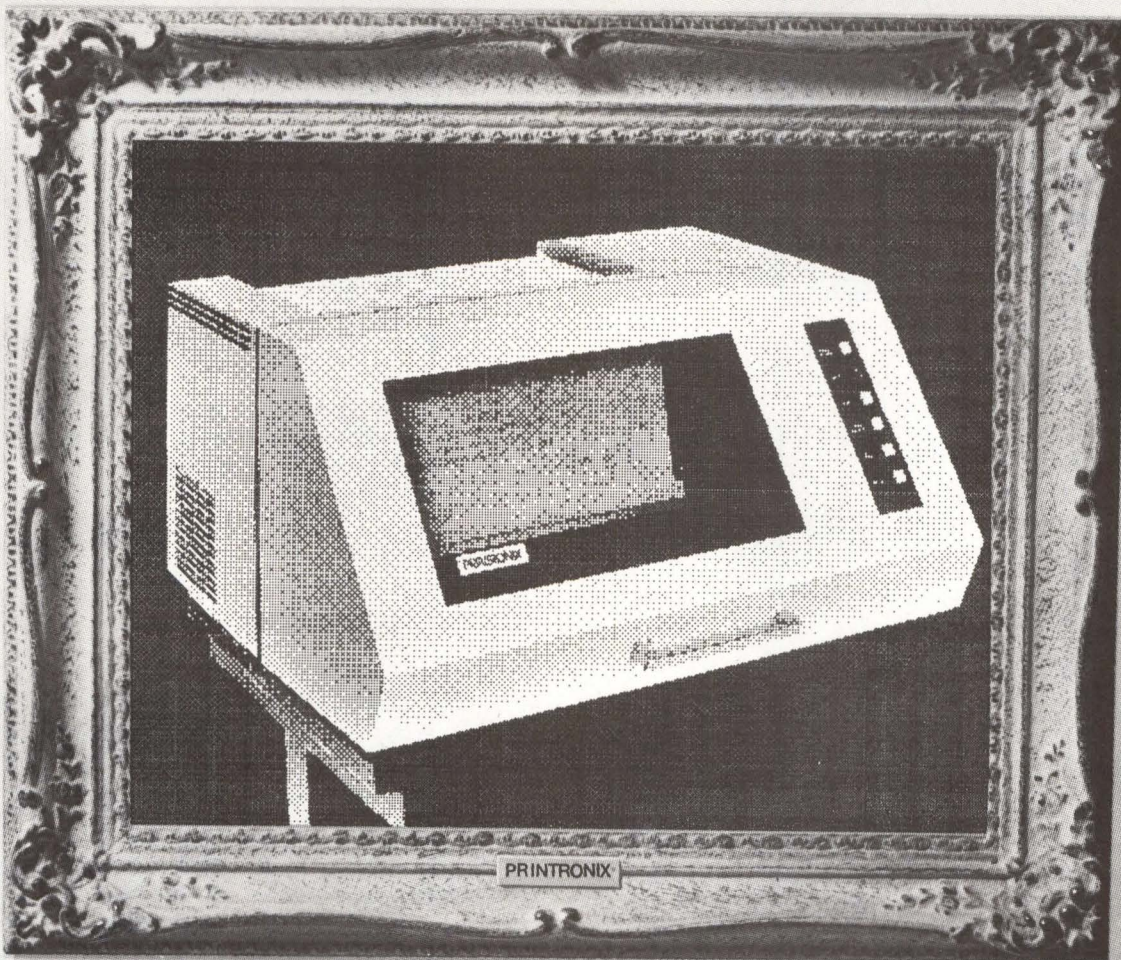
One or more analyzers can be controlled by a central host—mini-computer or development system. This allows all program access from one central data source without plugging test P/ROMS into each analyzer. Updating of a test program in a central data base assures that it is updated everywhere.

The option consists of a single board with 8k bytes of RAM and software that fits into a slot in the top of the analyzer system (see *Computer Design*, Nov 78, p 176). Master and slave μ SAs are coupled via modems and couplers. A cable from the analyzer is connected to the SUT, where the microprocessor has been unplugged. The master unit establishes control over the slave and initiates testing over the telephone link. The slave keyboard is normally locked out; however, diagnostic information is displayed on both the local and remote analyzers.

Serial interface runs at 110, 200, 600, 1200, 2400, 4800, or 9600 baud through either a standard 103 modem or direct link via RS-232-C level signals. Communication is block oriented with ASCII or hexadecimal data strings in block sizes up to 256 characters. Each block has its own checksum and header information.

A related announcement from Millennium Systems, Inc, 19020 Pruneridge Ave, Cupertino, CA 95014 introduces μ SA support for Intel 8085

Self Portrait of a very remarkable impact line printer.



It's a picture worth a thousand words about Printronic impact matrix line printer versatility and cost/performance value.

When the Printronic elegantly simple printing mechanism was conceived, it was determined that its primary role in life would be to produce multi-copy print quality no other impact printer could match, with far greater reliability than other matrix, drum, chain or belt line printers. It has done just that, as proven by more than 5000 units in the field.

But that's only half the picture.

As the "self portrait" shows, Printronic printers can also print drawings, graphs, charts, large characters, bar codes . . . any plotting you may need for a complete distributed data capability.

Other matrix, drum, chain or belt line printers can't do both. Yet a Printronic printer/plotter costs about the same, or less, than an alphanumeric printer alone.

Contact us for complete information on our 150, 300 or 600 lpm printer/plotters. Get a clear picture of the money you can save! Printronic, Inc., 17421 Derian Ave., P.O. Box 19559, Irvine, CA 92713. (714) 549-8272. TWX:(910) 595-2535.

PRINTRONIX

The picture of performance!

CIRCLE 91 ON INQUIRY CARD

and 8085A-2 microprocessors. The tester performs emulation at both 3 and 5 MHz, functioning through an umbilical plug that mates with the microprocessor socket in the SUT. The unit provides hardware breakpoints; single-step program execution; manipulation of CPU register, memory, and I/O values; signature analysis; and time domain capability.

Circle 415 on Inquiry Card

Lightpen Controls μComputer and Peripherals Without Use of Keyboard

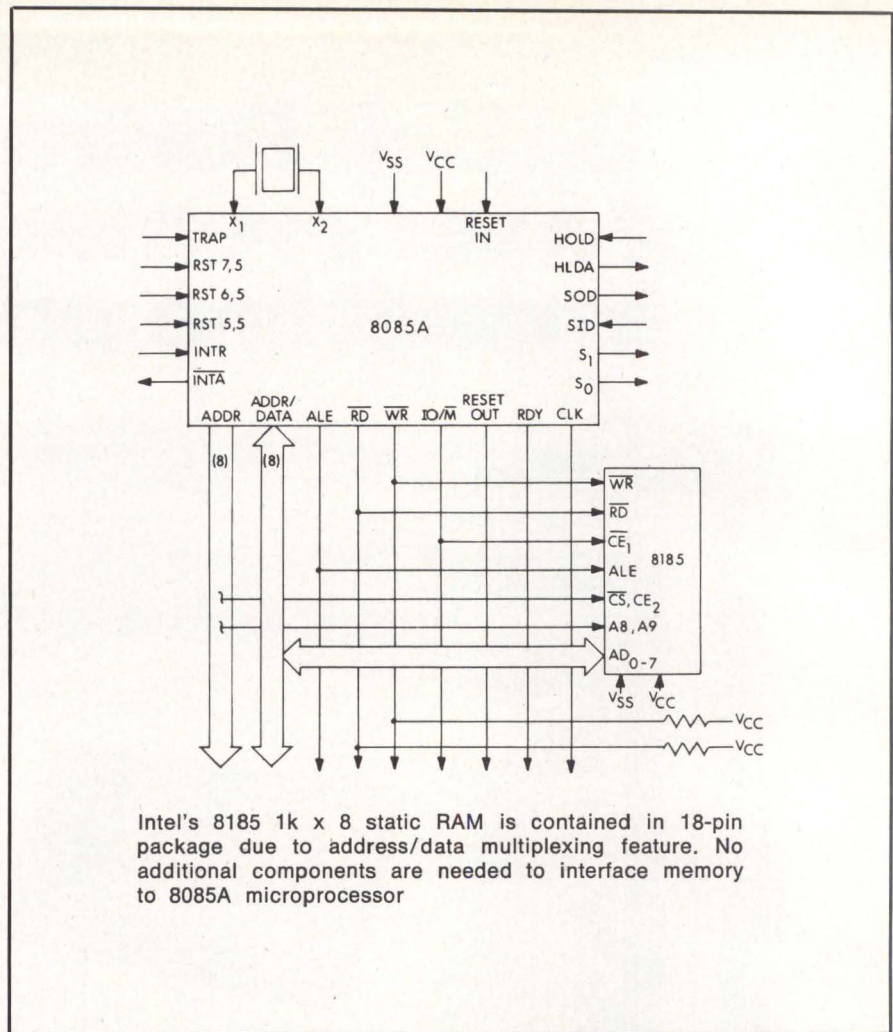
Menu selection, peripheral control, program branching, data input, and graphics aid are among the functions performed by a low cost lightpen for microcomputers. It can be used on any standard TV or display monitor in black and white or color. Complete with interface, the pen provides an x,y coordinate number to the bus when the pen is activated by a touch sensitive switch or from software control. The x,y values of up to 255 in Y and up to 511 in X are software dividable to fit any screen size.

Designed by Symtec, Inc, PO Box 462, Farmington, MI 48024 for the Apple II computer, the pen installs into the Apple I/O plugs. It resolves a single high resolution point, for use with all Apple graphics and text, and performs all of the keyboard's functions. A demonstration cassette is written in integer BASIC for easy modification and to allow use of the pen in the user's own programs. A comparable lightpen for S-100 bus computers will soon be available.

Circle 416 on Inquiry Card

1k x 8 Static Random Access Memory Requires Only 18 Pins

The use of address/data multiplexing permits the 8185 1k x 8 static RAM to fit an 18-pin package. The memory is compatible with the 8085A microprocessor series to build higher performance microprocessor systems while reducing space requirements and the number of components. Because Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 designed the



Intel's 8185 1k x 8 static RAM is contained in 18-pin package due to address/data multiplexing feature. No additional components are needed to interface memory to 8085A microprocessor

8085A to provide address and data multiplexing, each device in the system can save the eight pins that would have been required for independent data lines.

Tradeoffs between the number of functions provided and the number of pins in the memory were allocated to reducing the package size. It is shorter and narrower, featuring 0.3" (0.762-cm) spacing. Several of the saved pins were delegated to increased functions. For example, the device has two latched chip enables, which control power down, and an unlatched chip select, which expands

the decoding options and eases system timing requirements, plus separate read and write controls for system flexibility.

Built from HMOS technology, the memory operates from a single 5-V supply. Operating temperature range is 0 to 70 °C with storage temperatures of -65 to 150 °C. Two versions are the 8185 for use with the 8085, and the 8185-2 for use with the 5.0-MHz 8085-2. The device also expands the memory of single-chip microcomputer systems, the 8048, 8049, 8035, and 8748.

Circle 417 on Inquiry Card

Portable Computer Collects, Stores, and Processes Remote Data

Data are processed and stored on-site, with immediate tabulated printouts, using the portable computer system from Instat Systems, Inc, 1475 S Pierce St, Lakewood, CO 80226. Users can transmit data from the

computer to their company computers by telephone in less than two minutes with a phone modem.

System components are an encoder, Instapak memory cartridge, and main computer terminal. Fitting into the operator's hand, the encoder is the computer's remote data collector. Instead of using an LED display, the unit is manipulated by touch and



TRANSMISSION:
Page; Field; Modified
Field; Prompted
Transmission; Device
Status; Function Keys

INTERFACE:
EIA RS-232; Current
Loop; 17 data rates
(switch selectable)
including 19, 200
chars/sec; Half duplex
support; Line
turnaround characters;
Reverse channel.

**EDITING
FUNCTIONS:**

Insert/Delete line and
character; Columnar
Tabbing; Cursor
Addressability; Cursor
Sense; Numeric Only
fields; Security fields;
Erase Variable/
Protected fields.

OPTIONS:

Buffered Printer
Interface (RS-232
and parallel),
separately
addressable from
the CPU;
Standard Polling;
Paging.



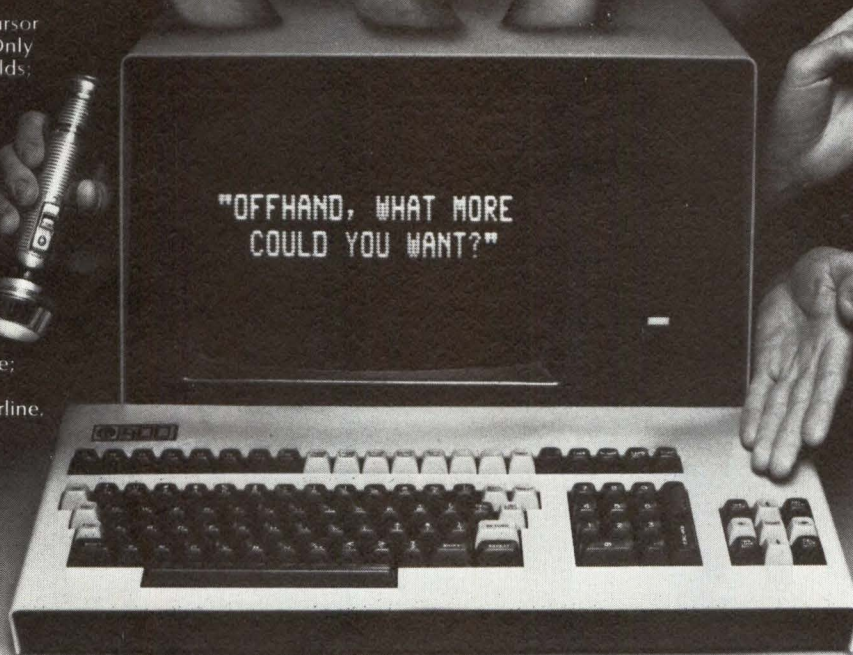
VIDEO:

Normal; Reverse;
Blink; Low/half
intensity; Underline.

"OFFHAND, WHAT MORE
COULD YOU WANT?"

KEYBOARD:

Removable, solid
state with international
character layouts.



When it comes to flexibility, the Infoton 400 Data Display terminal can hand you all you need.

Designed around the Z-80 microprocessor, it offers complete control of all Blocking and Editing functions through software settable modes. One thing that's especially easy to handle about the I-400 is that it's the most versatile terminal you can get your hands on for the price.

More information on the I-400 is quickly within your grasp. Call Infoton toll-free today at (800) 225-3337 or 225-3338. Ask for Barbara Worth. Or write Barbara Worth today at Infoton, Second Avenue, Burlington, MA 01803. We have offices throughout the United States, Canada and Europe. In Canada, contact Lanpar Limited, 85 Torbay Road, Markham, Ontario, L3R 1G7. (416) 495-9123.

Created by Chickering/Howell Advertising, Los Angeles

CIRCLE 92 ON INQUIRY CARD



INFOTON 400

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS



User inputs data into handheld Instat encoder where information is stored on Instapak memory cartridge. Cartridge is removed from encoder when full, and is inserted into portable computer system for further processing

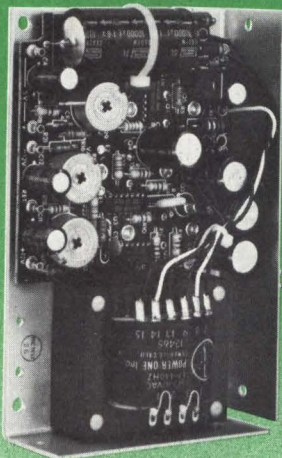
auditory feedback control. This "touch-tone" audio feedback system with operator earphone ensures accurate data compilation. The self-contained encoder works on a standard 10-key operation with visual position control and is powered by four AA batteries.

Information entered into the encoder is stored on a reusable Instapak memory cartridge which records 4k to 16k characters. The unit contains a full capacity indicator and is powered by three AAA batteries with a life of approximately one year. When full, the cartridge is removed from the encoder and inserted into the computer where it is immediately transferred onto computer memory tapes.

The 17 x 21 x 7" (43 x 53 x 18-cm) computer then reads and processes the information for final tabulation and projections. Included are a full alphanumeric keyboard; 10-key pad; 40-character dot matrix display that guides the operator through various program steps; a memory of 16k bytes, expandable to 64k bytes; two minicassette tape storage units; and a 96-character alphanumeric printer that can use 8.5 x 11" (21.6 x 28-cm) sheets or 3.5 to 8.5" (8.9- to 21.6-cm) rolls. It operates from 110 V. Software services are being prepared for the system. Circle 418 on Inquiry Card

FIRST

...in Triples



POWER-ONE offers the largest off-the-shelf line of triple output D.C. power supplies in the industry. 13 Models, from 16W to 150W. Precision regulated D.C. voltages for logic, memory, interface, linear devices, and Floppy-Disk memory systems.

- 115/230 VAC Input
- OVP on +5V Outputs
- ±.05% Regulation
- Two-Year Warranty
- UL and CSA Recognized

Get all the details on our 84 standard open frames. Send for our new Catalog.

Still Only \$49.95
Microcomputer Model HTAA-16W
Output #1 5V @ 2.0A with OVP
Output #2 9-15V @ 0.4A
Output #3 (-)9-15V @ 0.4A or -5V @ 0.4A

IN-STOCK NATIONWIDE... FOR IMMEDIATE DELIVERY

EASTERN REGIONAL SALES OFFICE: Schenectady, N.Y. (518) 399-9200 **ALA.:** Huntsville, Rakes Engr. & Marketing Corp. (205) 883-9260 **ARIZ.:** Phoenix, PLS Assoc. (602) 279-1531 **CAL.:** Pasadena, A-F Sls. Engr. (213) 681-5631; San Diego, A-F Sls. Engr. (714) 226-8424; San Jose, Richards Assoc. (408) 246-5860 **COL.:** Denver, PLS Assoc. (303) 773-1218 **CT.:** Litchfield, Digital Sls. Assoc. (203) 567-9776 **FLA.:** Orlando, OEM Marketing Corp. (305) 299-1000 **GA.:** Duluth, Rakes Engr. & Marketing Corp. (404) 476-1730 **ILL.:** Chicago, Coombs Assoc. (312) 298-4830 **IND.:** Indianapolis, Coombs Assoc. (317) 897-5424 **MD.:** Wheaton, Brimberg Sls. Assoc. (301) 946-2670; Baltimore, Brimberg Sls. Assoc. (301) 792-8661 **MASS.:** Waltham, Digital Sls. Assoc. (617) 899-4300 **MICH.:** Southfield, L.H. Dickelma Co. (313) 353-8210 **MINN.:** Minneapolis, Engr. Prod. Assoc. (612) 925-1883 **N.J.:** Whippany, Livera-Polk Assoc. (201) 377-3220; Marmora, Holdsworth (609) 398-4340 **N.M.:** Albuquerque, PLS Assoc. (505) 255-2330 **N.Y.:** Roslyn Hts., Livera-Polk Assoc. (516) 484-1276; Syracuse, C.W. Beach (315) 446-9587 **N.C.:** Charlotte, Over & Over Inc. (704) 527-3070 **OHIO:** Cleveland, Marlow Assoc. (216) 991-6500; Dayton, Marlow Assoc. (513) 434-5673 **OKLA.:** Tulsa, Advance Technical Sls. (918) 743-8517 **ORE.:** Portland, Jas. J. Backer (503) 297-3776; Salem, Jas. J. Backer (503) 362-0717 **PENN.:** Pittsburgh, Marlow Assoc. (412) 831-6113; Newtown Sq., Holdsworth & Co. (215) 356-8550 **TEX.:** Dallas, Advance Technical Sls. (214) 361-8584; Solid State Electr. (214) 352-2601; Houston, Advance Technical Sls. (713) 469-6668; Solid State Electr. (713) 772-8483 **UTAH:** Salt Lake City, PLS Assoc. (801) 466-8729 **WASH.:** Seattle, Jas. J. Backer (206) 285-1300; Radar Elec. Co. (206) 282-2511 **WIS.:** Milwaukee, Coombs Assoc. (414) 671-1945 **EUROPE:** Hanex, L.A., CA (213) 556-3807 **CANADA:** Duncan Instr., Weston, Ontario (416) 742-4448; Winnipeg, Manitoba, Cam Gard Supply Ltd. (204) 786-8481

"Think about **Power-one** INC.
D.C. POWER SUPPLIES

Power One Drive • Camarillo, CA 93010 • Phone: 805/484-2806 • TWX: 910-336-1297

SEE OUR COMPLETE PRODUCT LISTING IN EEM & GOLDBOOK

Microcomputer Board Supports Oncard Multichannel A-D Module

Designed for data acquisition and direct control applications, MLZ-DAQ carries an ADAC ADAM-12 or ADAM-12 APG A-D module providing 16/32 12-bit channels of analog input. Inputs may be paired for monitoring differential analog signals. Four software selectable gains allow a mixture of both high and low level signals to be monitored. Input voltage ranges are -5 to 5, 0 to 5, -10 to 10, and 0 to 10 V.

Heurikon Corp, 700 W Badger Rd, Madison, WI 53713 offers 2- and 4-MHz configurations for Intel Multi-bus users. Other standard features are a Zilog Z80 CPU, two RS-232-C ports, dual baud rate generator, four 8-bit ports, four counter/timers, 1k static RAM, and sockets for 4k/8k bytes of EPROM. Mounting holes in each corner and auxiliary power input are provided for single-board applications. □

Circle 419 on Inquiry Card

**C-R-T, C-R-T, alpha-numeric,
ASCII-key, multi-key, programmability,
Blinkity, blankety video-bility,
Up-down-left-right cursing, absolute addressing,
Insert string, delete string, erase and back-tabbing,
Editing,
editing,
C-R-T editing . . .**



No bones about it.

**What you need now is some straight talk
about Smart Editing CRT Terminals.**

Selecting the right CRT for your system isn't easy. You're trying to find a fully capable Editing Terminal in a CRT marketplace that's crowded with a dizzying array of contenders at prices ranging all the way from a few hundred dollars to several thousands.

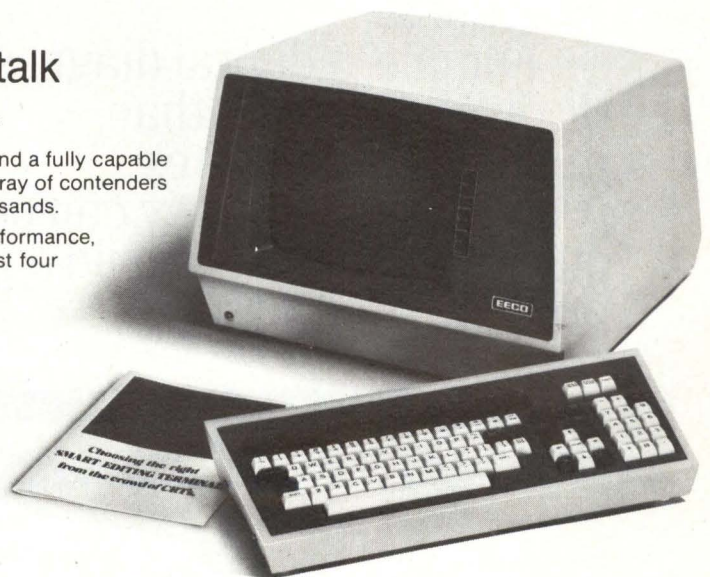
You'll be glad to know that for \$1500 or less, you can buy all the performance, reliability and support you need in a Smart Editing Terminal from at least four manufacturers — ADDS, Beehive, LSI, and EECO, of course. That's the conclusion of a comprehensive, straightforward report that frankly compares your alternatives model by model, spec for spec.

Get it straight — write for your free copy of "Choosing the right Smart Editing Terminal from the crowd of CRT's" today.

EECO editor

EECO, 1441 East Chestnut Avenue, Santa Ana, CA 92701 • (714) 835-6000

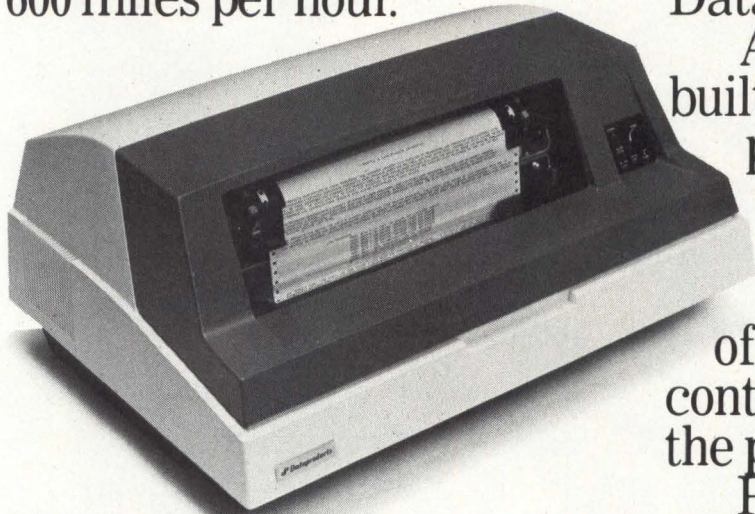
CIRCLE 183 ON INQUIRY CARD



300 LPM. AT 600 MPH.

The Dataproducts B-300 band printer is available for immediate delivery.

So, if you need a shipment PDQ, we can air freight it to you -- 300 lines per minute at 600 miles per hour.



The B-300 comes complete with standard features our competitors don't offer as options.

For one, a digital diagnostic display system that monitors and isolates problems so that they can be quickly resolved -- should a problem ever arise.

For another, the field-proven, friction-free Mark V hammer system. Its legendary reliability is standard.

But the standard that others can never match is Dataproducts' dependability.

And there's even more built into the B-300: lower power consumption, horizontal font print quality, operator changeable band, and the simplicity of design that makes all controls easily accessible and the printer easy to maintain.

Plus 95% spares commonality with the B-600, our 600 LPM band family member.

So, if you're looking for the next 300 LPM standard, and the best price/performance ratio in the industry, we'll ship it at 600 MPH! Call us collect, today.



The Printer Company

The Dataproducts B-300 Band Printer.

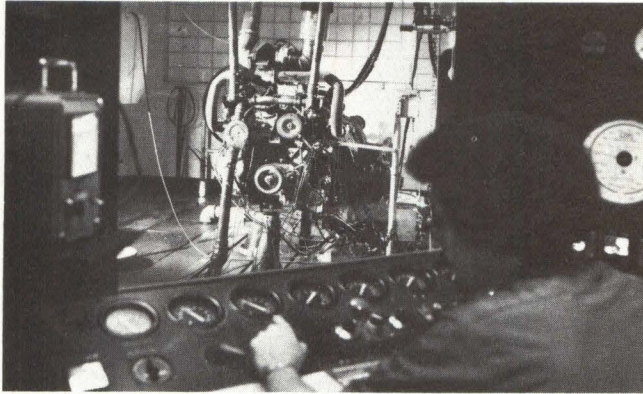
Dataproducts Corporation, 6219 DeSoto Ave., Woodland Hills, Ca. 91365. Telephone: (213) 887-8451 Telex: 67-4734
Darmstaedter Landstrasse 199, Frankfurt, W. Germany. Telephone: 681-034, Telex: 841-416344.



**"BEFORE WE COULD BUILD THE WORLD'S LARGEST INDUSTRIAL DATA ACQUISITION SYSTEM, WE NEEDED NETWORK AND SYSTEMS CAPABILITIES WE COULD DEPEND ON."
"ONLY MODCOMP HAD THEM."**

Jim Springer, Director of Data Systems,
AVCO Electronics, Huntsville, Ala.

Jim Springer is building what will be the largest industrial data acquisition system in the world. This system will be used for development and testing by one of the world's largest producers of diesel engines.



To implement the system, Jim chose MODCOMP's Classic® Computers, the MAX IV operating and communications system, and the MAXNET IV network extension.

"Network software capability is the key."

"The MAXNET IV network extension integrates all 120 computers in the system. This provides us with the performance characteristics of a stand-alone system, and the economic advantages of network resource sharing.

"In a real-time environment, that's essential."

"MODCOMP gives us the high speed and performance we need — at a cost we can afford."

"The MAX IV operating system is ideal for this type of real-time multi-programming. And with the Classic's extremely fast floating-point processor, we have more than enough speed.

"This is essentially the same system we specified for testing NASA's Space Shuttle. Ordinarily, that kind of superior quality and reliability would be out of reach for industry.

But because of their experience with the NASA system, only MODCOMP could meet the assigned high performance levels at a cost industry can afford."

"MODCOMP's tougher on their equipment than we are."

"Our customer was concerned about equipment reliability in their plant. And with good reason. The temperature can get as high as 120 degrees. But we've seen the Classic perform in worse places. MODCOMP's 'hot room' test facility, for instance. That's 132 degrees."

"Obviously we have a lot of faith in MODCOMP."

"We're just in the first phase of this system. But we have to know that, say, 3 years from now, the hardware will be available and that the software can be implemented or interchanged as needed.

"We recommend MODCOMP because we have a lot of faith in them. In their company, their equipment and their service.

"We know they can deliver. It's as simple as that."

At MODCOMP, we specialize in building real time computer systems and the network software capability to make them work.

Easily. Reliably. Affordably. And with the kind of performance you'd expect to find in the world's largest industrial data acquisition system.

If that's what you're looking for from a computer system supplier, do what Jim Springer did. Call MODCOMP.

MODCOMP
Dedicated to your success

Modular Computer Systems, Inc.
1650 McNab Road, Ft. Lauderdale, FL 33309
(305) 974-1380

Sales offices: Atlanta, GA • Boston, MA • Chicago, IL • Cincinnati, OH • Dallas, TX • Denver, CO • Detroit, MI • Hartford, CT • Houston, TX • Los Angeles, CA • Clark, NJ • Orlando, FL • Pittsburgh, PA • San Jose, CA • Washington, DC

RAM RELIABILITY IN LARGE MEMORY SYSTEMS—IMPROVING MTBF WITH ECC

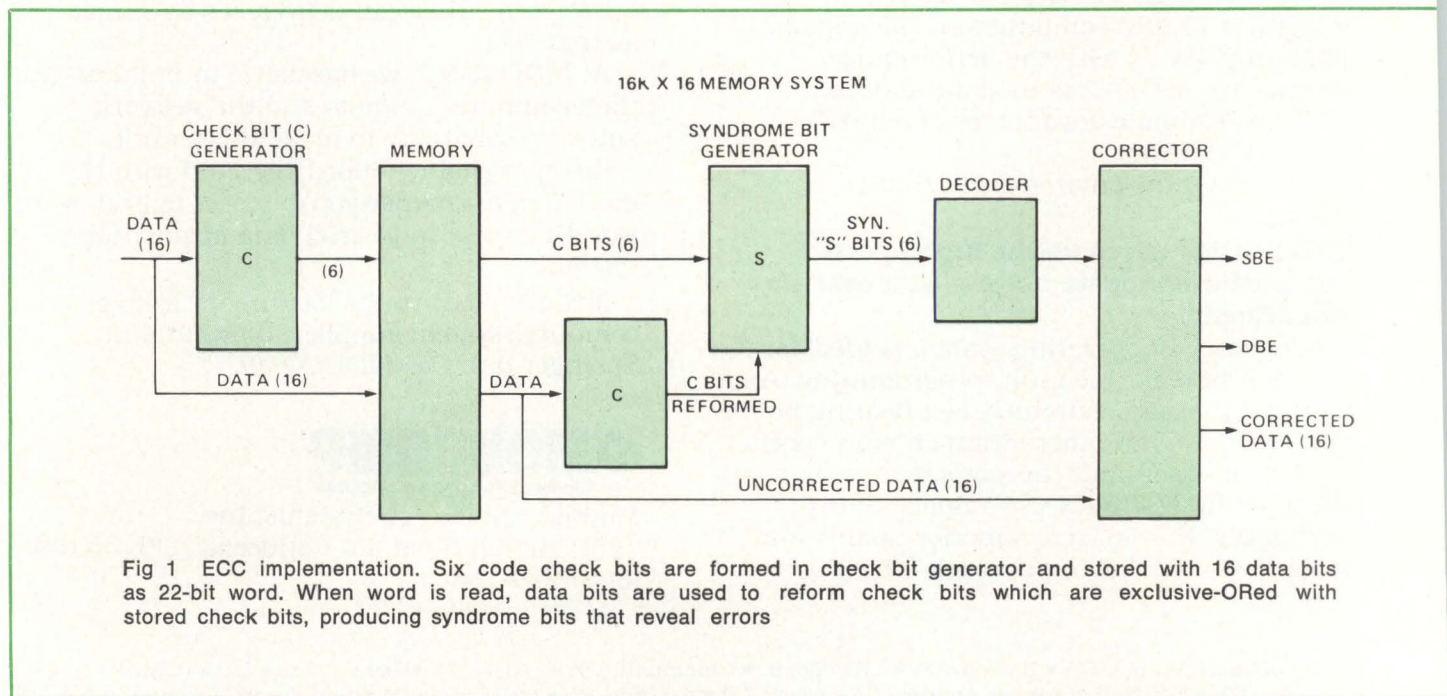
Robert Koppel

Intersil Incorporated,* Memory Systems Division,
Cupertino, California

Reliability of a random-access memory is a function of the number of elements, failure rate of each element, density, and operating parameters. Statistical techniques (see "RAM Reliability in Large Memory Systems—Significance of Predicting MTBF," R. Koppel, *Computer Design*, Feb 1979) enable reliability to be predicted as a function of the relevant variables. These techniques demon-

strate that as a memory system grows the predicted mean time between failures shrinks proportionally, reducing the probability that the system will meet its operating requirements. However, this predicted mean time between

*Mr Koppel is currently employed by Nitron Corp, Cupertino, Calif.



failures can be substantially improved by using error checking and correction techniques.

Error checking and correction (ECC) is a technique for extending parity checking concepts to disclose not only that a data word contains an error, but also to indicate which bit is in error, thus allowing it to be automatically corrected. When applied to memory systems, a typical ECC capability will correct any single-bit error resulting from a faulty RAM or bit-oriented support circuit. Soft errors (not repeatable, due to system noise or pattern) will be corrected as well as hard errors (permanent failures). Furthermore, at slightly increased cost, the occurrence of a double-bit error can be detected.

Use of ECC Codes

A block diagram of the ECC subsystem for a 16-bit word is shown in Fig 1. The code used is a modified Hamming code which, in addition to providing single-bit error correction and double-bit error detection, also detects even-bit multiple errors. Six code check bits (C-bits) are formed in the check bit generator for each 16-bit word of incoming memory data.

The code (shown in Fig 2) demonstrates generation of the C-bits, which are stored with the 16 data bits to form a 22-bit memory. When a memory word is read, bits 0 to 15 are used to reform the six C-bits in the same circuits as used previously.

These reformed C-bits are then exclusive-ORed with the stored C-bits to produce outputs called "syndrome" (S) bits. These S-bits reveal whether: no error occurred, a single-bit error (SBE) occurred (identifying that bit), or a multiple bit error (MBE) occurred. If SBE occurred, a signal is generated that inverts (corrects) the bit in error before it is latched in the output register. In addition to correcting SBEs, the ECC system can output an SBE flag, an MBE flag, and syndrome bits. These signals provide sufficient information to implement an automatic error logging system.

During operation of the error correction circuitry, the data and C-bits stored in memory are not changed by the error correction logic. If a single data bit is in error, the error is corrected in the output data. No attempt is made

to write corrected data back into memory. There are two reasons this is not done.

First, there is no point in writing back the data if a hard failure in the memory circuitry exists at that bit location, since that failure will again cause the bit to be in error. If the error was due to a soft failure or random noise interference, the information is probably stored correctly and, if accessed again, will probably be read correctly.

Secondly, to rewrite the single bit detected to be in error would require additional time and would extend the read cycle into a read-modify-write cycle, thus adding at least 150 ns. Since nothing is gained (and something may be lost) by writing the corrected bit back into memory, the bit is only corrected and then output properly.

For other word lengths, Table 1 gives the relationship between word length and number of ECC bits required. It should be noted that as the word length increases, the percentage requirement of ECC check bits becomes steadily smaller. For example, a 16-bit data word (falling in the 12- to 26-bits/word range in the table) would require six ECC bits, a 37.5% increase in bit count. This also implies an approximately 37.5% increase in board components. However, doubling the data word length to 32 bits requires only 7 check bits, an increase of 22% in bit (and parts) count. It may be possible in some applications to reorganize a 64k x 16 system internally into one of 32k x 32, resulting in a substantial saving in ECC bits.

Improving Reliability With ECC

Error correction's basic effect is to reduce the effect of RAM failures dramatically. In fact, if all RAM failures were single bit failures, RAM failures could effectively be eliminated. With the use of ECC, mean time between failure (MTBF) will depend almost entirely upon the nonstorage circuit components. This conclusion results from an analysis of double-bit failures within a word.

The distribution of failure modes experienced for 16k RAMs at Intersil is indicated in Table 2. While the majority of the failures involved isolated single bits, 9.2% involved failure of entire rows (resulting from a defective

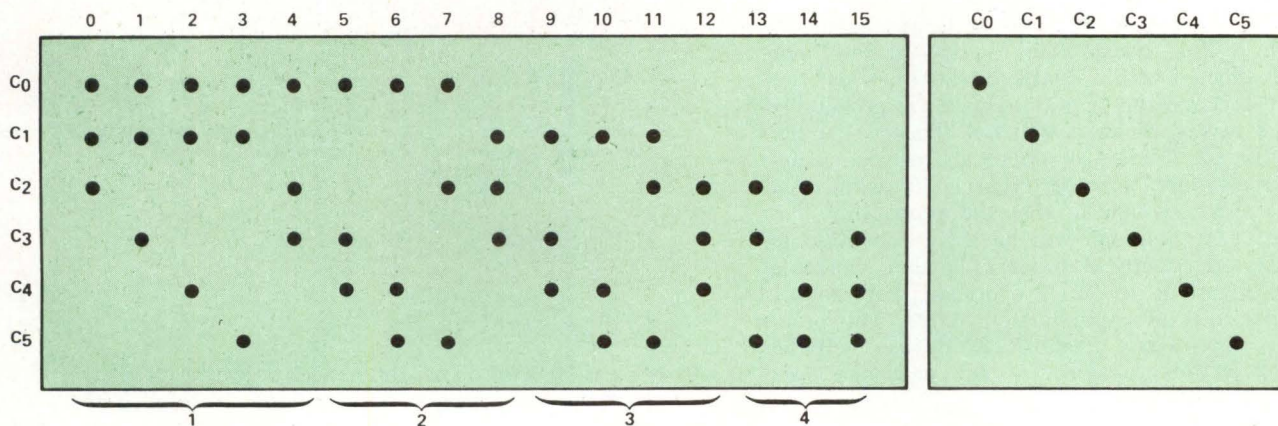


Fig 2 16-bit error correction code. Coding algorithm (1) generates four zones using binary combinations of C₀, C₁; (2) generates diagonal from C₂ to C₅ for each zone; (3) builds up each vertical column to three bits each by adding one bit to each column of zones 2 and 3 and by adding two bits to each column of zone 4

line driver) or entire columns in the 128 x 128-bit memory. Another 1.2% of the failures resulted from failure of the entire RAM. Although least frequent, this type of failure has the greatest impact on system reliability.

Consider a 22-bit/word arrangement made up of a series of 22 RAMs of 16k bits each. Assume that exactly 2 of the 22 RAMs fail during a specified period of operation. What is the likelihood that those two failures will involve 2 bits in the same 22-bit word, in at least one word location?

Table 3 summarizes the various failure modes that could lead to at least one double-bit failure, and assigns probabilities to each. Given a single-bit failure in one RAM, only 1 of 128² failure locations in the other RAM will lead to two single-bit failures in the same word; this produces the probability of (1/128)² at the upper left of the table. The probability that a single-bit failure in either RAM will correspond to a failed row or column in the other RAM is 1 in 128. If a row (or column) fails in one RAM, an orthogonally oriented failure in a column (or row) of the other will lead to a juxtaposition where row and column cross; the probability that this orthogonality results from two such failures is 0.5. There is also a probability of 0.5 that the 128-bit row failures will be parallel, with a 1/128 probability of juxtaposition (combining as shown in the central entry of the table). Finally, a total-RAM failure in either RAM will lead to a juxtaposition with a probability of 1 given a failure of any type in the other RAM.

Next, the conditional probabilities of Table 3 must be weighted by the relative probabilities of occurrence of the various failure types. For example, the upper lefthand entry, representing the juxtaposition of two single-bit errors, must be multiplied by (0.896)², and the lower righthand entry of the table must be multiplied by (0.012)². The resulting values, listed in Table 4, represent the weighted probabilities that the two failing RAMs will provide each of the kinds of juxtaposition. It is interesting to note that the highest probabilities, in descending order, are from juxtapositions of total-RAM and bit modes, row and column modes, and total-RAM and row modes.

The sum of the values in Table 4 is approximately 0.028, which is P_{DB}, the probability that at least one word will be affected with a double-bit failure when two RAMs fail. All that remains is to determine the probability that exactly 2 of the 22 RAMs will fail. This probability depends on the total period of operation between maintenance intervals. One good criterion is to define that period to be short enough so that the probability that ≥ 3 of the 22 RAMs will fail will be small compared to the probability of exactly 2 RAMs failing. A workable level can be found at 10⁴ h of operation, with failure probability per RAM at approximately 0.003. The probability, P(2), that exactly 2 of the 22 devices will fail (given that p is the probability of any particular RAM failing) is

$$P(2) = \frac{22 \cdot 21}{2} p^2 (1 - p)^{20}$$

Furthermore, the probability, P(≥ 2), that 2 or more of the 22 devices will fail is

$$P(\geq 2) = 1 - [(1 - p)^{22} + 22p(1 - p)^{21}]$$

For p = 0.003, these equations yield P(2) = 0.0019 and

TABLE 1

Wordlength Vs ECC Bits

Data Bits/ Word	ECC Bits (SE Correction + DE Detection)
2 to 4	4
5 to 11	5
12 to 26	6
27 to 57	7
58 to 120	8

TABLE 2

16k RAM Failure Distribution

Failure Type	Percent	Resulting Bits Failed/100 RAMs
Single-bit	89.6%	90
128-bit	9.2%	1177
Total RAM	1.2%	19,660

TABLE 3

Failure Combinations Involving Two 16k-Bit RAMs

RAM 1 Failure Types	RAM 2 Failure Types		Total-RAM (0.012)
	Single-Bit (0.896)	128-Bit (0.092)	
Single-bit (0.896)	$\left(\frac{1}{128}\right)^2$	$\frac{1}{128}$	1
128-Bit (0.092)	$\frac{1}{128}$	$\frac{1}{2} + \left(\frac{1}{2} \cdot \frac{1}{128}\right)$	1
Total-RAM (0.012)	1	1	1

Note: Numbers in parentheses represent relative probabilities from Table 2 relating to occurrences within each RAM

P(≥ 2) = 0.0020. The difference between these two values, 0.0001, represents the probability [P(≥ 3)] that ≥ 3 RAMs will fail in the 10⁴-h interval.

Table 5 summarizes these results for two different maintenance periods, 10,000 and 2000 h, using the above equations. Key values are those for P(≥ 3) and P_{DB}·P(2) found in columns IV and V. Values for P(≥ 3) (column IV) represent the cumulative probability of ≥ 3 RAM failures (not weighted to indicate double-bit juxtapositions) and those for P_{DB}·P(2) in column V show 2-RAM

LOOK WHAT WE'VE GOT ON BOARD

Core & Semiconductor Memories

	Capacity	Type	Memory System
DATA GENERAL			
NOVA 2 Series	32KB	Core Add-In	PINCOMM™ N
NOVA 3 Series	32KB	Core Add-In	PINCOMM N
NOVA 1200 Series	32KB	Core Add-In	PINCOMM N
DIGITAL EQUIPMENT			
PDP-11	32KB-128KB	MOS Add-In	PINCOMM PS
PDP-11	32KB-248KB	Core Add-On	BUSCOMM™ 11
PDP-11/70	128KB-1MB	Core Add-On	ECOM™ 70
RF-11/RS-11 Emulator	512KB-2MB	Core Add-On	BUSCOMM DS-11
PDP-11/70	256KB	MOS Add-In	PINCOMM 70S
GENERAL AUTOMATION			
SPC-16 Series	16KB, 32KB	Core Add-In	PINCOMM A
SPC-18/30	16KB, 32KB	Core Add-In	PINCOMM A
16/330, 16/440	32KB	Core Add-In	PINCOMM A
16/110, 16/220	32KB-128KB	MOS Add-In	PINCOMM AS
INTERDATA			
7/16, 7/32, 8/32	32KB	Core Add-In	PINCOMM I
Models 50, 55, 70, 74	32KB	Core Add-In	PINCOMM I
GENERAL PURPOSE	16KB TO 256KB per card		
Core & Semiconductor			

BUSCOMM, ECOM & PINCOMM are registered trade marks of Standard Memories. Interdata, General Automation, Data General, and Digital Equipment Corp. and their various model designations are recognized registered trade marks.

with immediate delivery and 1-year warranty

STANDARD MEMORIES
has grown into a new name

**Applied Magnetics
Trendata**

3400 West Segerstrom Ave.,
Santa Ana, CA 92704. (714) 540-3605



For an instant quotation call The Memory Man toll free: (800) 854-3792, (in California) (800) 432-7271.

TABLE 4

**Double-Bit Error Probabilities
Within Same Word as Function of Failure Types**

RAM 1 Failure Types	RAM 2 Failure Types		
	Single-Bit	128-Bit	Total-RAM
Single-Bit	4.9(10) ⁻⁵	6.4(10) ⁻⁴	0.01
128-Bit	6.4(10) ⁻⁴	4.3(10) ⁻³	(10) ⁻³
Total RAM	0.01	(10) ⁻³	1.4(10) ⁻⁴

Note: Results are based on assumption of exactly two RAM failures and do not depend (at this stage) on probability of individual RAM failure nor number of bits per word

TABLE 5

Double-Bit Error Summary

I	II	III	IV	V
Maintenance Period (h)	p	P(2)	p(≥3)	P _{DB} • P(2)
10,000	0.003	0.0019	(10) ⁻⁴	5.3(10) ⁻⁵
2000	0.0006	8.5(10) ⁻⁵	3(10) ⁻⁶	2.4(10) ⁻⁶

Note: Sum of values in box provides conservative estimate of 5.4(10)⁻⁶ double-bit error probability in 2000-h period

TABLE 6

MTBF of 64k x 16 System With ECC

Component	λp Failures/10 ⁶ h	Quantity	Total Failures/10 ⁶ h
IC	0.05	80	4.00
Ceramic Capacitor	0.01	88	0.88
Tantalum Capacitor	0.02	15	0.30
Resistor	0.001	70	0.07
PC Board	0.50	1	0.50
Delay Line	0.008	1	0.008
16k RAM	0.30	88	λ _{DB} *

Total Nonstorage λ = 5.758 Failures/10⁶ h

*λ_{DB} = 0.011 Failures/10⁶ h

failure probability, which is weighted (using the Table 4 sum of 0.028) to account for double-bit juxtapositions. Making the very conservative assumption that all failures of three or more RAMs will cause a double-bit failure, and using a 2000-h maintenance period, an estimate of double-bit failure probability is obtained by summing values for P(≥3) and P_{DB}•P(2) in the bottom row of Table 5, obtaining a value of 5.4(10)⁻⁶.

Retaining the 2000-h maintenance period, this result can be expressed in failures per million hours by multiplying

by a factor of 500; multiplying by an additional factor of 4 (to represent a 4-card 64k-bit system) produces a failure rate of 0.011 failures/10⁶ h. This value can then be inserted as λ_{DB} in Table 6, but is insignificant relative to nonstorage failure rate. The total for the system can then be computed as λ_S = λ_{DB} + λ (nonstorage) = 5.769/10⁶ h or an MTBF of ≈170,000 h, almost entirely dominated by the nonstorage circuits.

Procedure for Reliability Improvement

For ECC to be effective, it is essential that periodic maintenance be performed on the memory system to insure that hard-failed RAMs are replaced before a second failure occurs in the same data word. The maintenance period may be determined from the definition

$$\text{Reliability} = R(t) = e^{-t/M}$$

To insure a reliability of 99%, t should not exceed M/100. For the system with a MTBF of M = 170,000 h, the maintenance period t ≈ 1700 h (approximately 2.5 mo). This corresponds fairly closely to the 2000-h value that dropped out as a natural choice in the earlier analysis.

To improve memory system reliability, there are other steps to be taken at both the device and system level. At the device level, parameters (V_{BB}, V_{DD}, timing, temperature) should be varied over a wide operating range, exposing the RAM to worst-case read/write test patterns. It is important to design for reasonable voltage and speed margins, burning in RAMs dynamically under voltage stress to weed out infant failures.

At the system level, it is advisable to select the lowest cost RAM that meets system performance requirements. It is better to select high speed support circuits than high speed RAMs to meet high speed requirements. Conservative board layout rules should be used, boards should be submitted to thermal cycling/burn-in, and a parity/reaccess system should be employed. In the final card test, the RAM should be run for 24 h using worst-case test patterns, incorporating error logging.

Summary

The use of error correction coding provides major benefits in the reliabilities of large memory systems. RAM contribution to system failure rate without ECC was estimated (in the February column) to be 19.2 failures/10⁶ h in a 64k x 16 memory system. With ECC and appropriate selection of a maintenance cycle, that contribution is reduced by a factor of approximately 2000. System reliability has been improved from the 23.45 failures/10⁶-h rate obtained without ECC to the 5.769 failures/10⁶-h rate quoted previously.

Penalties for the use of ECC, as illustrated here, include a 35% increase in system cost and a 50 to 75 increase in system access time. For sufficiently large memory systems that are not borderline with respect to speed requirements, the cost is worth it. In general, system size and applications will establish the utility of ECC in each individual situation.

Bibliography

- Intersil, Application Note 37, "Layout Considerations using 4k MOS RAMs," Intersil, Inc, Cupertino, Calif, June 1976
- MIL-HDBK-217B, Reliability Prediction of Electronic Equipment, Sept 1974
- MIL Std-781B, Reliability Testing, July 1969

SYNERTEK PERFORMS

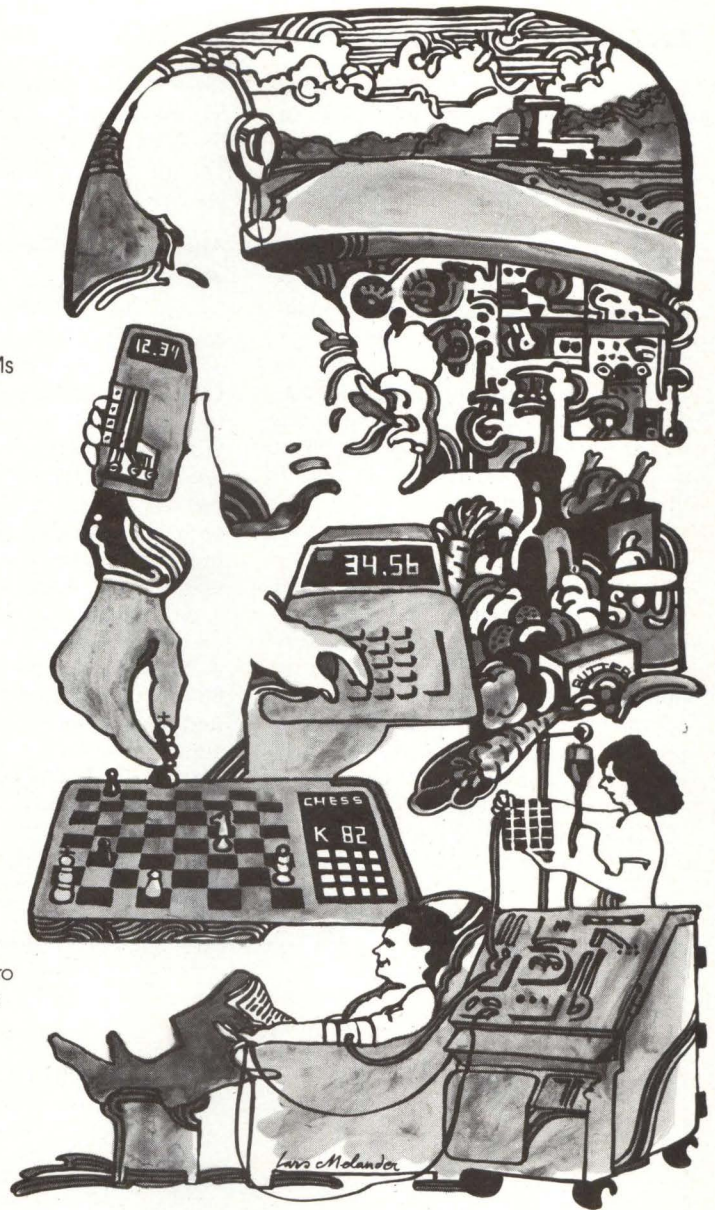
5101 CMOS RAMs. Now. In quantity.

Performance and delivery you can count on. That's what you get with our 5101 static RAM. Because one without the other leaves you out in the cold.

Contact your local distributor, or Synertek direct, and you'll get the 5101 RAMs you need. And you'll get them when you need them. With all the features that make the 5101 the industry standard 256 x 4 CMOS RAM— for any low power or battery back-up application.

50 Microwatts is all you need to cover standby power requirements with the 5101. It's pin for pin compatible with the power hungry 2101. Features include chip-enable standby operation, single +5V power supply, power down memory retention (2 volts), separate data inputs and 3-state outputs that are TTL compatible.

If you're not getting the deliveries you want when you need them, call on the people who perform. Contact your area Synertek distributor or Memory Marketing, Standard Products Division, Synertek, Inc., 3001 Stender Way, Santa Clara, California 95051. (408) 988-5611. TWX: 910-338-0135. Synertek sales offices: **Eastern Region**, 400 Humphrey St., Suite 2, Swampscott, MA 01907 (617) 595-1170; **Central Region**, 4615 W. Streetsboro Rd., Suite 204, Richfield, OH 44286 (216) 659-4195; **Midwest Region**, 2805 Butterfield Rd., Suite 150, Oakbrook, IL 60621 (312) 986-8989; **Western and Northwest Regions**, 20863 Stevens Creek Blvd., Bldg. B3, Suite C, Cupertino, CA 95014 (408) 255-3941; **Southwest Region**, 1000 Quail St., Suite 290, Newport Beach, CA 92660 (714) 752-5535; **Europe**, Honeywell House, Charles Square, Bracknell, Berkshire, England, Rg 12 1Eb. Direct Dial: 011-44-344-24555.



Part Number	Access Time	Standby Current	Guaranteed 2.0 Volt Memory Retention
SY5101L-3	650nsec	200 μ A	Yes
SY5101L	650nsec	10 μ A	Yes
SY5101L-1	450nsec	10 μ A	Yes
SY5101-8	800nsec	500 μ A	No

Off-The-Shelf Delivery From These Synertek Distributors:

Arrow Electronics	General Radio	Advent Electronics
Kierulff Electronics	Alliance Electronics	Quality Components
Sterling Electronics	Parrott Electronics	Taylor Electric
Zeus	Summit Distributors	Western Microtechnology
Century/Bell	Lionex	Future Electronics
Sheridan Sales	Hall-Mark	Emitter Electronics
Technico	Intermark Electronics	R-M Electronics

SYNERTEK, INC.

3001 Stender Way, Santa Clara, California 95051
(408) 988-5600. TWX: 910-338-0135.

Bucket-Brigade Charge-Transfer Devices Operate on Analog Signals

A family of charge-transfer devices of the bucket-brigade type perform sophisticated signal processing upon analog inputs. Two of these devices are signal correlators: the R5403 correlates (or convolutes) a pair of analog signals; the R5401 correlates (or convolutes) an analog input signal with a digital signal. The third member of the family, the R5501, is a parallel in/serial out (PISO) device. Finally, the R5701 is an analog signal averager that, in the averaging process, effectively improves the signal-to-noise ratio of signals buried in incoherent noise.

Functioning as tapped analog delay lines, all of these CCDs are single-chip implementations of n-channel silicon-gate technology, developed by EG&G Reticon, 345 Potrero Ave, Sunnyvale, CA 94086. This manufacturer indicates that the signal processing operations carried out by these CCDs previously required a digital computer. General information concerning CTD technology can be found in "Charge-Transfer Devices—Part 1: The Technologies," and "Part 3: Di-

verse Uses of CTDs for Analog, Digital, and Optical Applications," by E. R. Garen (*Computer Design*, Nov 77, pp 146, 150, 152 and Jan 78, pp 154-157, respectively).

Analog-Analog Correlator

The R5403 consists of two CTDs, each having 32 individual taps with corresponding taps on each line acting as inputs to 4-quadrant multipliers. Outputs from these multipliers are then summed onchip, their sum providing the chip output. Signal progression in one of the delay lines can be selected to be either forward or reverse, so that the signal processing can be either correlation or convolution (see Figure).

Additional characteristics of this correlator include sampling rates to 4 MHz, a dc power dissipation of 330 mW, a 60-dB dynamic range, and 2% linearity. The input analog signal may be sampled by either of the CTD delay lines at rates from a minimum of 1 kHz up to a maximum of 2 MHz at 25 °C. Each of the CTDs require 2-phase complementary

square-wave clocks of 15-V amplitude.

Circle 350 on Inquiry Card

Binary-Analog Correlator

The R5401 also performs a correlation or convolution between two signals, operating, however, on an analog signal and a programmable binary function. It consists of a pair of CTDs, each with 32 taps equally spaced one sample-time apart along the device. The composite of these elements is a 64-stage tapped analog delay line into which samples of an input analog signal are continually shifted.

Each stage of the delay line has a tap with series solid-state switches, which are controlled by the true and complement outputs of a corresponding stage of a static digital shift register. A binary word loaded into the digital shift register selects the pattern in which the taps are to be connected to two output lines: a 0 in the nth shift-register stage will connect the corresponding tap to one output line, and a 1 will connect the tap to the other output line.

An analog signal may be sampled at rates from 1 kHz (at 25 °C) up to a maximum of 10 MHz. After every clock transition, the temporarily stored analog samples are multiplied, point by point, with the binary pattern residing in the static shift register.

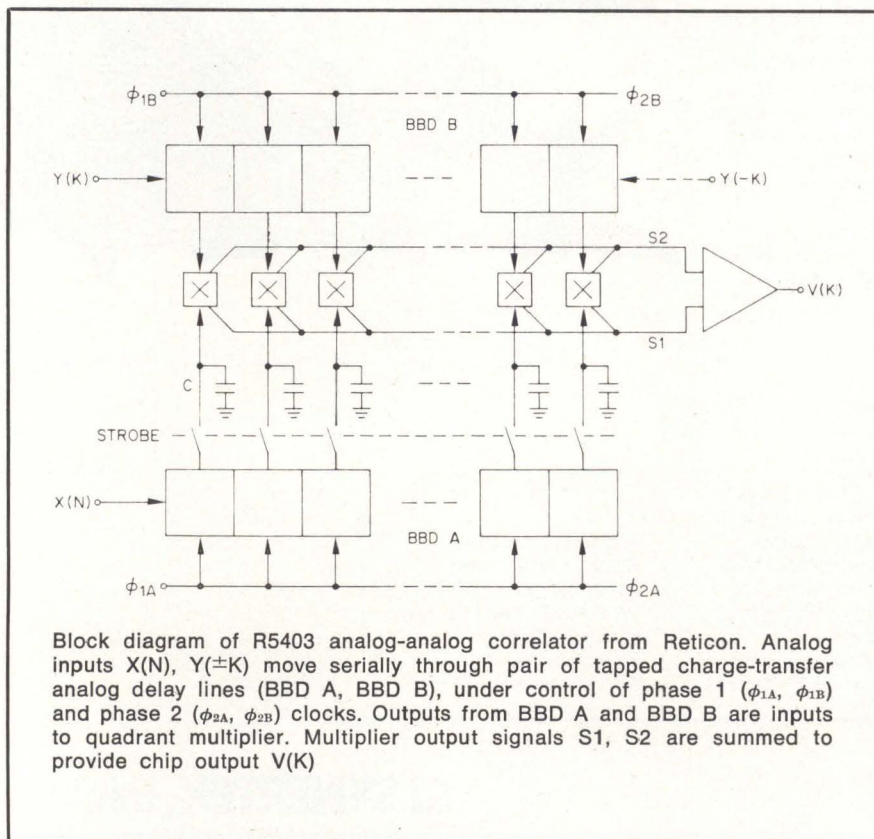
Characteristics include up to 10-MHz analog sampling rate, a 1-MHz register shift speed, and 360-mW power dissipation. Typical applications involve use in image comparison/identification, data communication/error correction coding, bit/word synchronization, and pulse compression.

Circle 351 on Inquiry Card

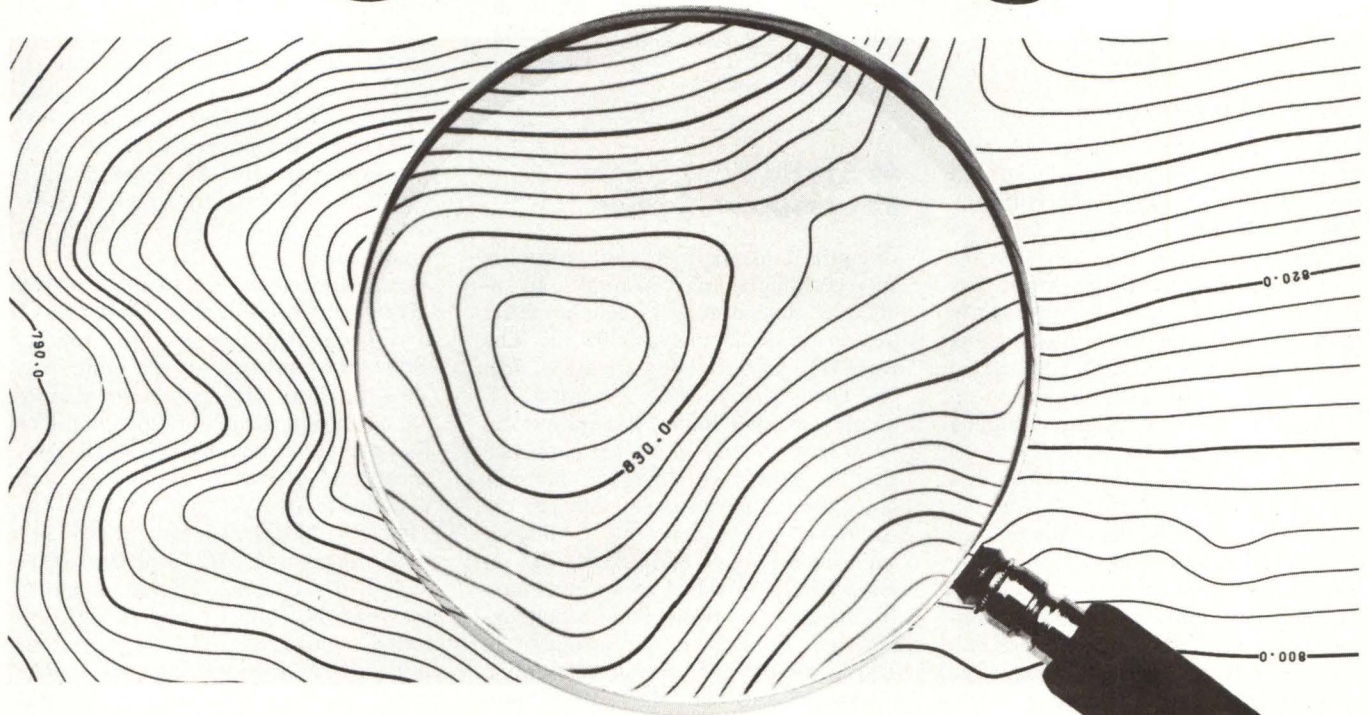
Parallel In/Serial Out CTD

The capabilities of the R5501 include parallel-to-serial conversion and input convolution. It provides for time-domain multiplexing by receiving a 32-sample data block from 32 parallel data channels and then reproducing those data in a serial stream of 32 data points. Input convolution is performed through summing successive weighted parallel input samples.

Analog values are entered in parallel into the serial delay line stages.



No one else looks this good under glass.



If you're shopping for a medium-priced drum plotter, the old eye-ball test is still a good place to begin.

And so's CalComp.

Because no matter how you scrutinize our graphics — or measure our output — one thing comes clearly into focus: CalComp makes the best drum plotters in the world. Period.

Case in point: Our new 1030-Family of medium-priced drum plotters. In terms of accuracy, line quality, speed and good old-fashioned price/performance, they literally outdraw the competition. At every turn.

Better yet, all three new plotters are perfectly suited to a wide range of graphics applications. And that means, with the help of a new 1037, 1038 or 1039 plotter, any data now in your computer can work even harder for you outputted in an easier-to-understand graphic form.

A clear case of superior engineering.

For starters, we made all three new models completely d.c. servo-motor driven. For increased accuracy in every mode. On-line. Remote/time-sharing. And off-line.

Then, we gave them all a newly-designed linear drive pen mechanism. For the kind of pen force control that produces consistently superior line quality. In every application.

Next, we greatly increased overall throughput — especially in on-line environments — by implementing "smarter," microprocessor-based controllers.

Finally, there's even greater built-in versatility. Because both the 1037 and 1038 can be field-upgraded — all the way up to a new 1039 — without ever leaving your office.

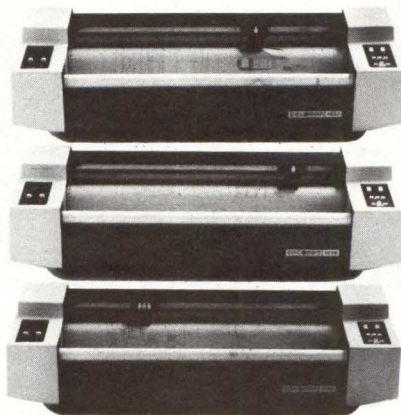
Service and Support that's a sight for sore eyes. The one thing we haven't changed is CalComp service and support. It's still worldwide and second to none. For field service personnel. For in-place field systems analysts. For the kind of help you expect from the world leader in digital graphics.

All of which proves, when it comes to drum plotters, it pays to set your performance sights a little higher.

THE NEW 1030 DRUM PLOTTER FAMILY

plotter model	mm-per-second	pens	step size in mm
1037	50.0 (≈ 2.0 in.)	1	.05 (≈ .002 in.)
1038	112.5 (≈ 4.5 in.)	1	.05 (≈ .002 in.)
1039	112.5 (≈ 4.5 in.)	3	.05 (≈ .002 in.)

Draw your own conclusions. It's easy with a free CalComp sample plot. For your own evaluation copy, call: (714) 821-2011. Or write: CalComp, 2411 La Palma Avenue, Dept. MS-3, Anaheim, California 92801.



CALCOMP
CALIFORNIA COMPUTER PRODUCTS, INC.

WEST: Orange, CA (714) 639-3690 / Santa Clara, CA (408) 249-0936 / Houston, TX (713) 776-3276 / Dallas, TX (214) 663-2326 / Englewood, CO (303) 770-1950 / Beaverton, OR (503) 646-1186 / Bellevue, WA (206) 747-9321 / Tempe, AZ (602) 894-9468 / Tulsa, OK (518) 663-7392 / SOUTH: Norcross, GA (404) 449-4600 / Huntsville, AL (256) 533-6260 / Orlando, FL (305) 857-2920 / MIDWEST: Southfield, MI (313) 569-3223 / St. Louis, MO (314) 968-5537 / Rolling Meadows, IL (312) 392-1320 / Dayton, OH (513) 276-7915 / Cleveland, OH (216) 362-7280 / Shawnee Mission, KS (913) 362-0707 / Bloomington, MN (612) 854-3448 / EAST: Waltham, MA (617) 890-4850 / Union, NJ (201) 686-7000 / Bala Cynwyd, PA (215) 667-1740 / Rockville, MD (301) 770-5274 / Pittsburgh, PA (412) 922-3430

Each piece of information is spaced one clock period from its neighbor so that the entire parallel input packet may be read out sequentially in a serial stream of 32 discrete-time analog samples. A device consists of three functional sections: bucket-brigade transport; 32 input storage capacitors with associated transfer switches; and output stage.
 Circle 352 on Inquiry Card

Analog Signal Averager

The R5701/ASA-32 consists of two CTDS each with 32 taps equally spaced one sample-time apart, but with the taps individually connected to a set of capacitors by means of a transfer gate. Each set of capacitors also has a reset switch to delete the previously stored information before accepting signals from a new signal integration cycle, thus allowing flexibility in selecting any number of input analog word patterns. Averaging is based on a signal-processing algorithm employing a first-order difference equation at each of the individual storage sites or taps. The algorithm is effectively the same as that of a single-pole recursive filter; however, it is not subject to the degradation of the signal-to-noise ratio inherent in recursive integration caused by the process of recycling coherent noise. Therefore, the device has an advantage over the recursive averager in its ability to cycle a greater number of integration periods.

Having a sampling rate up to 2 MHz, a rapid resettable storage memory with storage duration of >10 s, and a low power dissipation, the device has a wide variety of applications. It finds uses in biomedical en-

gineering, speech communication, data communication, nuclear science, seismology, acoustics, and analog processors.

Circle 353 on Inquiry Card

In general, the devices in this family feature simple interface, peripheral, and drive circuitry. Dual in-line packages are 28-pin (R5403), 16-pin (R5401), 40-pin (R5501), and 22-pin (R5701).

4k Static RAM Offers Power-Down Option

Organized as 4k x 1 and operating from a single ± 5 -V supply, an n-channel silicon-gate circuit provides access times as fast as 200 ns. The Am9044, produced by Advanced Micro Devices Inc (901 Thompson Pl, Sunnyvale, CA 94086), is a fully static RAM having TTL interfaces and dissipating 368 mW. Identical features characterize a companion device, the Am9244, which has the additional capability for powering down via an automatic chip select to approximately 50% power consumption when deselected. Both RAMs are available in 18-pin plastic and ceramic dual-inline packages and undergo 100% processing to the requirements of MIL-STD-883.

Circle 354 on Inquiry Card

Compact Hybrid Data Acquisition System Provides 16 Channels

Provided in a 2.2 x 1.7 x 0.22" (5.6 x 4.3 x 0.56-cm) package, a hybrid

data acquisition system offers all functions available with large, modular systems. Including a low drift, internal instrumentation amplifier, the SDM857, priced at \$125 in 100s, performs digital conversion and multiplexing of analog inputs as high as ± 5 V and as low as ± 10 mV, eliminating any requirement for external signal conditioning in applications involving thermocouples, strain gauges, and other low level signal sensors. Gain can be selected from 2 to 500 with one external resistor. Throughput sampling rates are from 29 kHz (12-bit resolution) to 70 kHz (8-bit resolution) in the overlap mode of operation.

Another model, the SDM856, priced at \$99 in 100s, differs from the -7 model only in that it does not include the instrumentation amplifier. This provides the option of adding an external instrumentation amplifier for specific requirements such as high speed and digital programming. Both models are available from Burr-Brown (PO Box 11400, Tucson, AZ 85734) with selectable 16-channel single-ended or 8-channel differential input, and can be fully expanded with external multiplexers. Three-state output buffers are provided for easy interface to microprocessor and other bus oriented systems. Other system components include a multiplexer, sample/hold amplifier, analog-to-digital converter, address latch, and delay timer.

The analog multiplexer consists of two CMOS integrated circuits. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting the amplifier inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation, respectively.

A complete standalone circuit, the sample/hold amplifier features buffered output, 10- μ s acquisition time, and 100-ns aperture time. Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions such as automatic gain ranging, with no loss of aperture time.

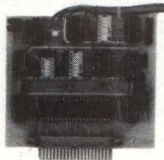
The ADC is a 12-bit, 25- μ s converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight

**Jumpers, etc.,
etc., etc...**

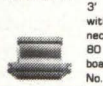
See page 89

TRS-80^{E.S.} SERIAL I/O

- Can input into basic
- Can use LIST and LPRINT to output, or output continuously
- RS-232 compatible
- Can be used with or without the expansion bus
- On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line
- Requires +5, -12 VDC
- Board only \$19.95 Part No. 8010, with parts \$59.95 Part No. 8010A, assembled \$79.95 Part No. 8010 C. No connectors provided, see below.



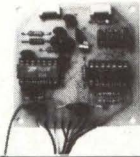
EIA/RS-232 connector Part No. DB25P \$6.00, with 9', 8 conductor cable \$10.95 Part No. DB25P.



3' ribbon cable with attached connectors to fit TRS-80 and our serial board \$19.95 Part No. 3CAB40.

MODEM*

- Type 103
- Full or half duplex
- Works up to 300 baud
- Originate or Answer
- No coils, only low cost components
- TTL input and output-serial
- Connect 8 Ω speaker and crystal mic. directly to board
- Uses XR FSK demodulator
- Requires +5 volts
- Board only \$7.60 Part No. 109, with parts \$27.50 Part No. 109A



VERBATIM MINIDISK



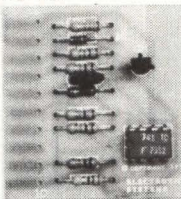
Box of 10

\$29.95

RS-232/ TTL*

INTERFACE

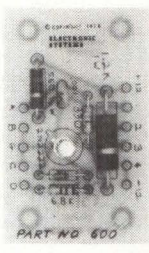
- Converts TTL to RS-232, and converts RS-232 to TTL
- Two separate circuits
- Requires -12 and +12 volts
- All connections go to a 10 pin gold plated edge connector
- Board only \$4.50 Part No. 232, with parts \$7.00 Part No. 232A 10 Pin edge connector \$3.00 Part No. 10P



RS-232/ TTY*

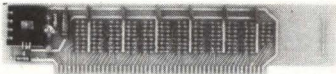
INTERFACE

- Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232
- Two separate circuits
- Requires +12 and -12 volts
- Board only \$4.50 Part No. 600, with parts \$7.00 Part No. 600A



S-100 BUS * ACTIVE TERMINATOR

Board only \$14.95 Part No. 900, with parts \$24.95 Part No. 900A



APPLE II* SERIAL I/O INTERFACE



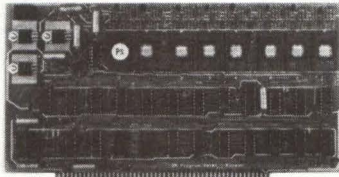
Baud rate is continuously adjustable from 0 to 30,000

- Plugs into any peripheral connector
- Low current drain. RS-232 input and output
- On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even
- Jumper selectable address
- SOFTWARE
- Input and Output routine from monitor or BASIC to teletype or other serial printer
- Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some electrics.
- Also watches DTR
- Board only \$15.00 Part No. 2, with parts \$42.00 Part No. 2A, assembled \$62.00 Part No. 2C

8K EPROM PIGEON

Saves programs on PROM permanently (until erased via UV light) up to 8K bytes. Programs may be directly run from the program saver such as fixed routines or assemblers.

- S-100 bus compatible
- Room for 8K bytes of EPROM non-volatile memory (2708's).
- On-board PROM programming
- Address relocation of each 4K of memory to any 4K boundary within 64K
- Power on jump and reset jump option for "turnkey" systems and computers without a front panel
- Program saver software available
- Solder mask both sides
- Full silkscreen for easy assembly. Program saver software in 1 2708 EPROM \$25. Bare board \$35 including custom coil, board with parts but no EPROMS \$139, with 4 EPROMS \$179, with 8 EPROMS \$219.



WAMECO INC. WMC inc.

FDC-1 FLOPPY CONTROLLER BOARD will drive shugart, pertek, remic 5" & 8" drives up to 8 drives, on board PROM with power boot up, will operate with CPM (not included). PCB \$42.95

FPB-1 Front Panel. (Finally) AMSA1 size hex displays. Byte or instruction single step. PCB \$42.95

MEM-1A 8Kx8 fully buffered, S-100, uses 2102 type RAMS. PCB \$24.95, \$168 Kit

GMB-12 MOTHER BOARD, 13 slot, terminated, S-100 board only \$34.95 \$89.95 Kit

CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCB \$25.95 \$89.95 Kit

RTC-1 Realtime clock board. Two independent interrupts. Software programmable. PCB \$25.95, \$60.95 Kit

EPM-1 1702A 4K EPROM card PCB \$25.95 \$49.95 with parts less EPROMS

EPM-2 2708/2716 16K/32K EPROM card PCB \$24.95 \$49.95 with parts less EPROMS

GMB-9 MOTHER BOARD. Short Version of GMB-12. 9 Slots PCB \$30.95 \$67.95 Kit

MEM-2 16Kx8 Fully Buffered 2114 Board PCB \$25.95, \$269.95 Kit

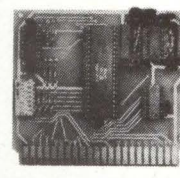
T.V. TYPEWRITER

- Stand alone TVT
- 32 char./line, 16 lines, modifications for 64 char./line included
- Parallel ASCII (TTL) input
- Video output
- 1K on board memory
- Output for computer controlled cursor
- Auto scroll
- Non-destructive cursor
- Cursor inputs: up, down, left, right, home, EOL, EOS
- Scroll up, down
- Requires +5 volts at 1.5 amps, and -12 volts at 30 mA
- All 7400, TTL chips
- Char. gen. 2513
- Upper case only
- Board only \$39.00 Part No. 106, with parts \$145.00 Part No. 106A



UART & BAUD RATE GENERATOR*

- Converts serial to parallel and parallel to serial
- Low cost on board baud rate generator
- Baud rates: 110, 150, 300, 600, 1200, and 2400
- Low power drain +5 volts and -12 volts required
- TTL compatible
- All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity.
- All connections go to a 44 pin gold plated edge connector
- Board only \$12.00 Part No. 101, with parts \$35.00 Part No. 101A, 44 pin edge connector \$4.00 Part No. 44P



TAPE * INTERFACE

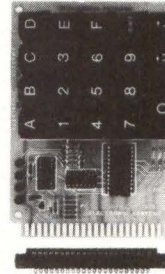
- Play and record Kansas City Standard tapes
- Converts a low cost tape recorder to a digital recorder
- Works up to 1200 baud
- Digital in and out are TTL-serial
- Output of board connects to mic. in of recorder
- Ear-phones of recorder connects to input on board
- No coils
- Requires +5 volts, low power drain
- Board only \$7.60 Part No. 111, with parts \$27.50 Part No. 111A



HEX ENCODED KEYBOARD

E.S.

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only \$15.00 Part No. HEX-3, with parts \$49.95 Part No. HEX-3A. 44 pin edge connector \$4.00 Part No. 44P.



DC POWER SUPPLY*

- Board supplies a regulated +5 volts at 3 amps., +12, -12, and -5 volts at 1 amp.
- Power required is 8 volts AC at 3 amps., and 24 volts AC C.T. at 1.5 amps.
- Board only \$12.50 Part No. 6085, with parts excluding transformers \$42.50 Part No. 6085A

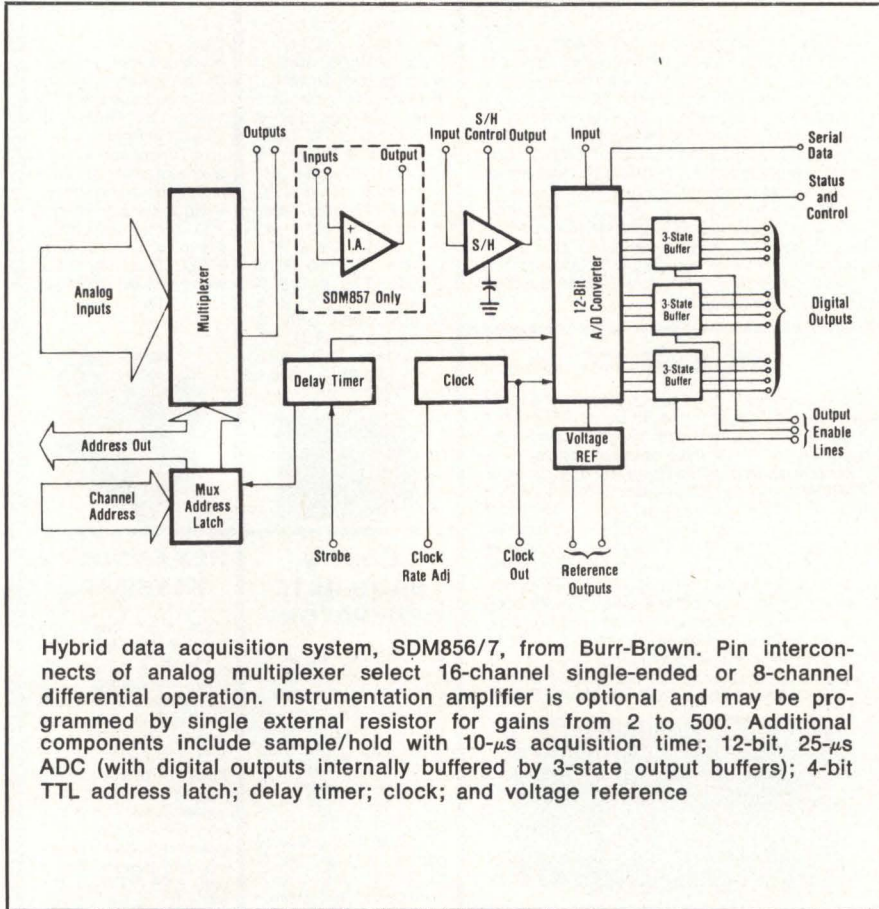


To Order: Mention part number, description, and price. In USA, shipping paid for orders accompanied by check, money order, or Master Charge, BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D. orders. California residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling, no C.O.D.'s. Checks and money orders must be payable in US dollars. Parts kits include sockets for all ICs, components, and circuit board. Documentation is included with all products. Prices are in US dollars. No open accounts. To eliminate tariff in Canada boxes are marked "Computer Parts." Dealer inquiries invited. 24 Hour Order Line: (408) 226-4064



For free catalog including parts lists and schematics, send a self-addressed stamped envelope.

ELECTRONIC SYSTEMS Dept. CD, P. O. Box 21638, San Jose, CA USA 95151



Hybrid data acquisition system, SDM856/7, from Burr-Brown. Pin interconnects of analog multiplexer select 16-channel single-ended or 8-channel differential operation. Instrumentation amplifier is optional and may be programmed by single external resistor for gains from 2 to 500. Additional components include sample/hold with 10- μ s acquisition time; 12-bit, 25- μ s ADC (with digital outputs internally buffered by 3-state output buffers); 4-bit TTL address latch; delay timer; clock; and voltage reference

binary or 2's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

Outputs of the 4-bit TTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input.

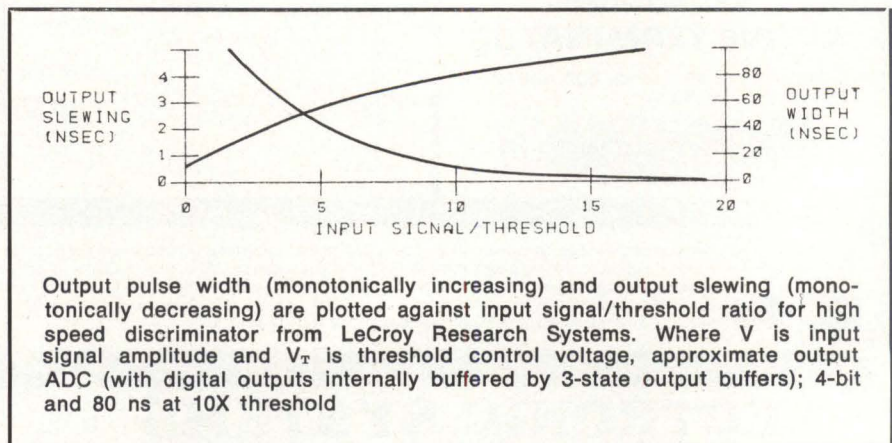
Settling time before conversion begins is provided for the multiplexer, amplifier, and sample/hold circuits by the delay timer. Delay is adjustable over a wide range through use of an external resistor or capacitor. This allows for longer settling time of the instrumentation amplifier when operating at high gains, or shorter settling time for lower resolution operation.

Absolute maximum ratings specify that the analog input voltage stay within ± 20 V without damage, and within ± 6 V for linear operation. Temperature must stay between -25 and 85 $^{\circ}$ C during operation and between -55 and 100 $^{\circ}$ C in storage.

Circle 355 on Inquiry Card

High Speed Discriminator Detects Low Level Pulses

A very fast pulse discriminator for the detection of low level pulses is used for direct connection to signal sources such as fiber optic data receivers, pulsed laser detectors, optical radar systems, and nuclear in-



Output pulse width (monotonically increasing) and output slewing (monotonically decreasing) are plotted against input signal/threshold ratio for high speed discriminator from LeCroy Research Systems. Where V is input signal amplitude and V_T is threshold control voltage, approximate output ADC (with digital outputs internally buffered by 3-state output buffers); 4-bit and 80 ns at 10X threshold

Circle 356 on Inquiry Card

struments. It was specifically designed to optimize the usefulness of multi-wire proportional chambers in high energy physics experiments. In contrast to conventional designs where long amplifier risetimes (30 to 40 ns) and high input thresholds (1 to 5 mV) combine to create excessive time dispersion (discriminator slewing), the LD604 has a low minimum threshold of -200 μ V and an inherent amplifier risetime of 4 ns, which essentially eliminates the electronics as the source of time dispersion in the system. This fact permits narrower coincidence gates (simplifying track recognition by admitting fewer accidentals), reduces chamber dead-time, and lowers chamber high voltage, helping to increase chamber lifetime.

Produced by LeCroy Research Systems Corp, 700 S Main St, Spring Valley, NY 10977, the device consists of a fast preamplifier differentiator-coupled to a biased voltage comparator with complementary ECL outputs, capable of driving twisted-pair or 50- Ω coaxial cable. Outputs are compatible with ECL levels, permitting direct connection to fast logic elements without level shifting or sacrifice of speed and delay.

The high impedance differential input permits flexibility in choice of input terminals and tolerates common mode noise and offset up to ± 0.4 V. Input-to-output delay is less than 15 ns. Response to a step input is a pulse whose duration is a function of input overdrive and the 30-ns time constant of the internal RC coupling network. At 20-V threshold the output pulse width is approximately 100 ns.

OEMS. TAKE A FREE TRIAL SPIN ON US, HARDTOP OR CARTRIDGE.



The Proven MX Winchester Technology Family

From the world's largest alternative manufacturer of Winchester technology disk drives, Fujitsu offers excellent price/performance and reliability. The M2251, M2252, and M2253 provides 12.5, 25, or 50 megabytes of unformatted storage along with flexible program or data loading from a variety of external sources: diskette drives, cartridge drives, storage module drives, tape drives, and communications lines. MTBF is in excess of 10,000 power-on hours. Access times are 10-ms track-to-track, with 40-ms average. And pricing in 100 quantities is very aggressive.

The Unique, Front Loading SMD-Compatible M2201

As the only front loading drive around, the M2201 offers new convenience and flexibility in configuring your small business systems, intelligent terminals and other micro/minicomputer based systems. It offers 50 megabyte capacity. Has a reliability factor that's 50% better than the industry average (6,000 POH MTBF). And stores at an off-line cost that's lower than either top loading cartridge or storage module drives. Access times are

6-ms track-to-track. There are no data staging requirements. Plus, a servo/track record system assures cartridge interchangeability.

Free Offer

For a limited introductory time, Fujitsu is providing no-strings-attached evaluation units, including paid freight, to qualified OEMs. Order yours now by calling Byron Wicks, Marketing Director, collect at 408/985-2300. NOTE: reference your call to the operator as the Fujitsu Evaluation Offer. Or send the coupon to: Fujitsu America Inc., 2945 Oakmead Village Court, Santa Clara, CA 95051 Telex: 357402 TWX: 910-338-0047 Tel: 408/985-2300. Offer subject to change without notice.

- I want an evaluation unit. Now.
- Please send data on your Winchester technology products
- Please send data on the M2201
- Have product representative call on application

Application area _____
 Name/Title _____
 Organization _____
 Street/City _____
 State/Zip/Telephone _____



FUJITSU OEMS. YOU'RE IN THE DRIVER'S SEAT WITH FUJITSU.

Precision Thin-Film Ladder Network Provides Up to 12-Bit Resolution

A family of high precision, thin-film ladder networks provides 8-, 10-, or 12-bit resolution for voltage or current summing in analog-to-digital and digital-to-analog conversion applications. Of the four current ladders, the D-350 is a 12-bit binary weighted device; the D-351 is also a 12-bit design, but BCD weighted; and the F-352 and F-353 are, respectively, 8-bit and 4-bit binary current ladders. The D models are

housed in 24-pin dual-inline hermetic packages, while the F models are 14-lead flat packs. Temperature tracking for all models is better than 1 ppm/°C and accuracy is $\pm\frac{1}{2}$ LSB (or $\pm 0.012\%$ at 12 bits).

Produced by Electro Films Inc, 100 Meadow St, Warwick, RI 02886, the four models are intended for use with such quad switching devices as the Analog Devices AD550 and AD555, and the Intersil 8018. They are completely interchangeable with the AD850 series or the Beckman 816-50 ladder networks.

Circle 357 on Inquiry Card

for common-anode LED displays. The 7-segment decoding is implemented with a ROM providing the user with the option of specifying alternative fonts.

Produced by Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, the NE 586 is pin compatible with standard 7447, 9374, and 8674 drivers. Data (BCD) and LE (latch enable) inputs are low loading so that they are compatible with any data bus system. Due to the constant current outputs of 25 mA, essentially independent of output voltage, power supply voltage, and temperature, the driver is suitable for multiplexed operation of large size LED digits. Applications include use with digital panel meters, measuring instruments, test equipment, digital clocks, and digital bus monitoring.

The circuit has a supply rating of -0.5 to 7 V, with an operating supply voltage between 4.75 and 5.25 V. Input rating is -0.5 to 15 V, while the output rating is -0.5 to 7 V. Ambient temperature is restricted to the range from 0 to 70 °C during operation, while storage temperature must stay between -65 and 150 °C.

Circle 360 on Inquiry Card

Two 8192-Bit Schottky P/ROMs Reduce Package Count in Control Memory

Organized as 1024 words of 8 bits, two Schottky programmable read-only memories utilize titanium-tungsten fuse links, low current pnp inputs, fast programming, and multiple select lines to simplify memory expansion. These P/ROMs feature 45-ns typical access time, 70-ns maximum enable time, and power consumption of 630 mW typical, about half that of two 4k P/ROMs.

Manufactured by Texas Instruments Inc, PO Box 5474, Dallas, TX 75222, the devices are provided in two versions. A 3-state output characterizes the SN74S478, while the SN74S479 has an open collector output. Both models are supplied in the industry standard 24-pin dual-inline package configuration and are plug-compatible with 4k 24-pin P/ROMs, the S474 and S475 by the same manufacturer. The devices are available in plastic (N suffix) and ceramic (J suffix) DIPs.

Circle 358 on Inquiry Card

32k-Bit UV Erasable P/ROM Features 450-ns Maximum Access Time

Organized as 4k x 8, a 32,768-bit ultraviolet erasable and electrically programmable read-only memory is interchangeable with the Intel 2732. Distributed by Fujitsu America Inc, 2945 Kifer Ave, Santa Clara, CA 95051, the MBM2732 operates from a single 5-V power supply, has a 450-ns max access time, and a power consumption of 450 mW typical, 75 mW standby.

Fabricated using the manufacturer's proprietary FAMOS structure (floating avalanche injection MOS), the EPROM uses an output enable function to eliminate bus contention, has a 3-state output for direct bus connection, and provides TTL compatibility on all inputs and outputs. It is provided in a 24-pin dual-inline package with a transparent lid.

Circle 361 on Inquiry Card

IC Operates As dc Motor Speed Control To Provide Stability

Accurate, pin programmable speed ratios for slow, medium, or fast motor velocities are selected by a monolithic integrated circuit, designated as the CS-175. The dc motor speed control is produced by Cherry Electrical Products Corp, 3600 Sunset Ave, Waukegan, IL 60085 and is designed to provide flexibility by reducing requirements for adjustment and external components in multiple speed applications.

While many other applications are possible, the device is intended primarily for use with ac tachometer signals. It is capable of providing a level of stability such that errors are dominated by terms created by the finite loop bandwidth made

necessary to ensure stability with the dynamics of the specific motor and load.

List price is \$1.68 with a net cost in 1000-piece quantities of \$0.79 and in 10,000 quantities of \$0.65. The unit is provided in a 14-lead plastic dual-inline package.

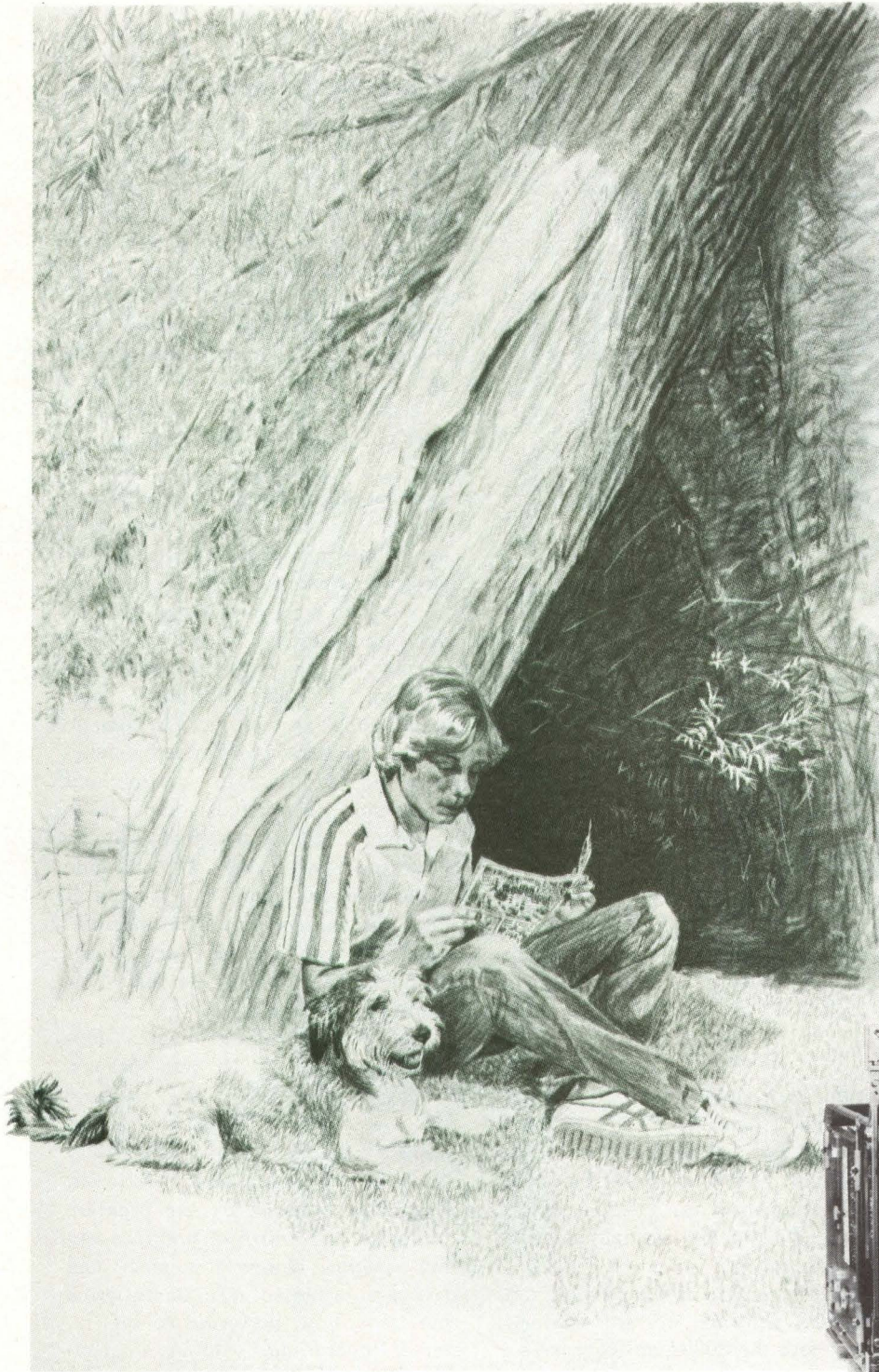
Circle 359 on Inquiry Card

LED Decoder/Driver Has Latched Inputs, Constant 25-mA Outputs

An integrated circuit, featuring latched BCD inputs, constant current outputs of 25 mA, low loading bus compatible inputs, and ripple-blanking on leading and/or trailing edge zeros, functions as a decoder/driver

GROWING UP TOGETHER

... there's no more certain path to understanding



The years we've spent growing up with the alphanumeric terminal industry—years of working closely with the designers and makers of the final product—have given us the insight and understanding of the industry's needs that could have come no other way.

This relationship has helped Motorola grow to be a leading supplier of CRT display modules to the industry. Leading not only in terms of sales, but also in terms of quality, reliability and technology; leading in terms of performance vs. price.

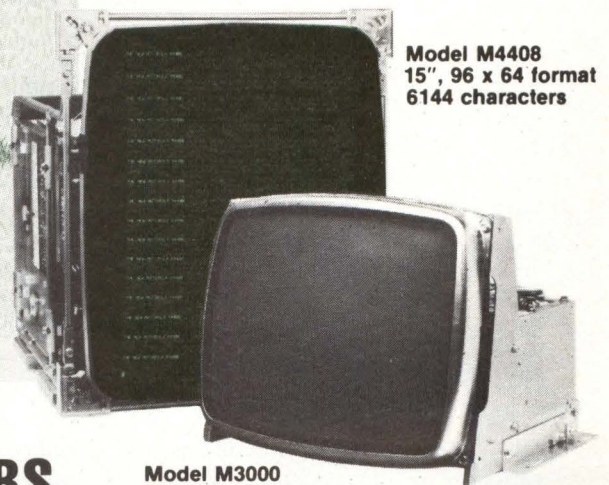
When you're considering the single most important hardware item in your terminal design, you'll want the supplier that can put all those years of experience, understanding and leadership to your best benefit.

Call the sales office in your area:

Sunnyvale, California (408) 744-1277
Tustin, California (714) 838-5621
West Chicago, Illinois (312) 231-4400
Dallas, Texas (214) 233-2006
Salem, New Hampshire (603) 898-5921
Shrewsbury, New Jersey (201) 544-9541
Baltimore, Maryland (301) 821-0062

Overseas, ask for International Sales Manager, West Chicago, Illinois

*(312) 231-4400
TWX: 910-230-3117*



Model M4408
15", 96 x 64 format
6144 characters

Model M3000
12", 80 x 24 format
1920 characters

BENEFIT FROM EXPERIENCE ... OURS

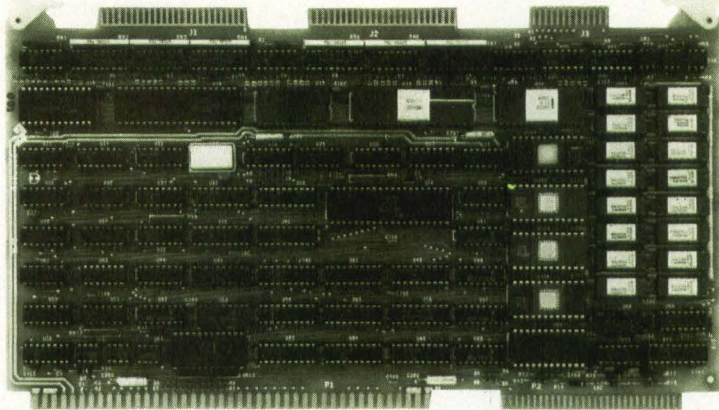


MOTOROLA INC.

Display Systems

1155 Harvester Rd., West Chicago, IL 60185

PRODUCT FEATURE



Multibus/Z80A Based Microcomputer Offers 32-Bit Floating Point Arithmetic

A single-board OEM microcomputer operating from a 4-MHz clock, the Monolithic Systems Corp MSC 8004 is fully compatible with the Intel Corp Multibus™ and is built around a Zilog Z80A™ central processing unit. It includes up to 32k bytes of dynamic RAM and can accommodate up to 32k bytes of ROM/EPROM. An optional Advanced Micro Devices 2- or 4-MHz Am9511 32-bit floating point processor can be used for intensive computational applications.

Operation is in a multimaster system with either parallel or serial priority resolution. Concurrent and asynchronous operations can be

carried out on both internal bus and Multibus when the CPU uses local memory and I/O devices. Bus access is usually required only for communication between tasks, enabling enhanced system throughput with multiple masters.

Incorporation of the Z80A CPU provides software upward compatibility with the 8080A microprocessor and execution of all 8080 instructions without modification. Multibus compatibility enables the microcomputer to be used either to expand existing SBC 80 based systems or as the basis of a new design with the variety of components now on the market.

Characteristics and Capabilities

Basic features of the Z80A CPU—such as a double complement of registers, block transfer I/O instructions, index registers, BCD subtraction, nonmaskable interrupt, and block search and move instructions—reduce system size and increase speed of application programs. Execution of the fastest CPU instructions require 1.25 μ s.

The optional arithmetic logic unit (ALU) is capable of 32-bit operation using floating point as well as fixed point. All transfers, including operand, result, status, and command information, are pushed into an internal stack, and a command is issued to perform an operation on the data contained in the stack. The results are then made available for retrieval, or an additional command may be entered. Arithmetic and transcendental-derived functions in addition to control and conversion commands and basic arithmetic operations that can be performed with the ALU include trigonometric, common and natural logarithmic, and e^x or x^y exponential functions; constant pi; square root; and single, double, or floating stack control and change sign.

Full Multibus control logic permits as many as 16 bus masters, including other MSC 8004s, to share the system bus. Three bus modes allow exchange of bus master every cycle, every instruction, or never. Bus modes are set by the program for optimum control of multiprocessing systems. Onboard memory and I/O are accessed via an internal bus, enabling performance of internal operations without interference with Multibus activities.

Dynamic RAM in a basic system provides up to 32k-byte storage capacity in a 16-chip array partitioned into two 16k- or 4k-byte sections. Arrays are addressed by either the CPU address lines or the Multibus direct memory access. The

OUR COMPETITIVE EDGE

Precision, extra-long life character elements for high-speed printers, point of sale equipment, teleprinters and similar printing and stamping equipment.

By what criteria do you design the character transfer elements of your printing and stamping equipment? Are they engineered to give the performance you require throughout the product life?

Mark Stamp Steel, a division of Mohawk Data Sciences Corp., engineers and manufactures quality print drums, print wheels, type slugs and similar character elements for some of the largest printer and teleprinter manufacturers in the world.

Quality design and engineering insure that your specifications are exactly met. Availability of high-technology processes, including powdered metal, cold rolling, and precision engraving, insure that your character elements are manufactured using the best possible process. The result, optimum uniformity throughout product life.

Choose from a library of over 5000 characters, including OCR, MICR, IBM, CDC, and numerous special and foreign fonts. Or, let us design a font to your specifications.

Mohawk Data Sciences is one of the leading suppliers of distributed data processing, key-to-disk and peripheral systems, with a customer base of over 7000 worldwide. Mark Stamp Steel has played a major role in the success of MDS products and their reputation for exceptional performance and reliability.

To receive additional information, or a price/performance quotation on your application, fill out and return the attached coupon. We'll tell you how our competitive edge can improve the price and performance of your product.

I'd like to learn more about your products and services:

- Please send literature.
- Please send quotation (My specifications and requirements are attached).
- Please have a design specialist call.

Name _____ Title _____

Company _____

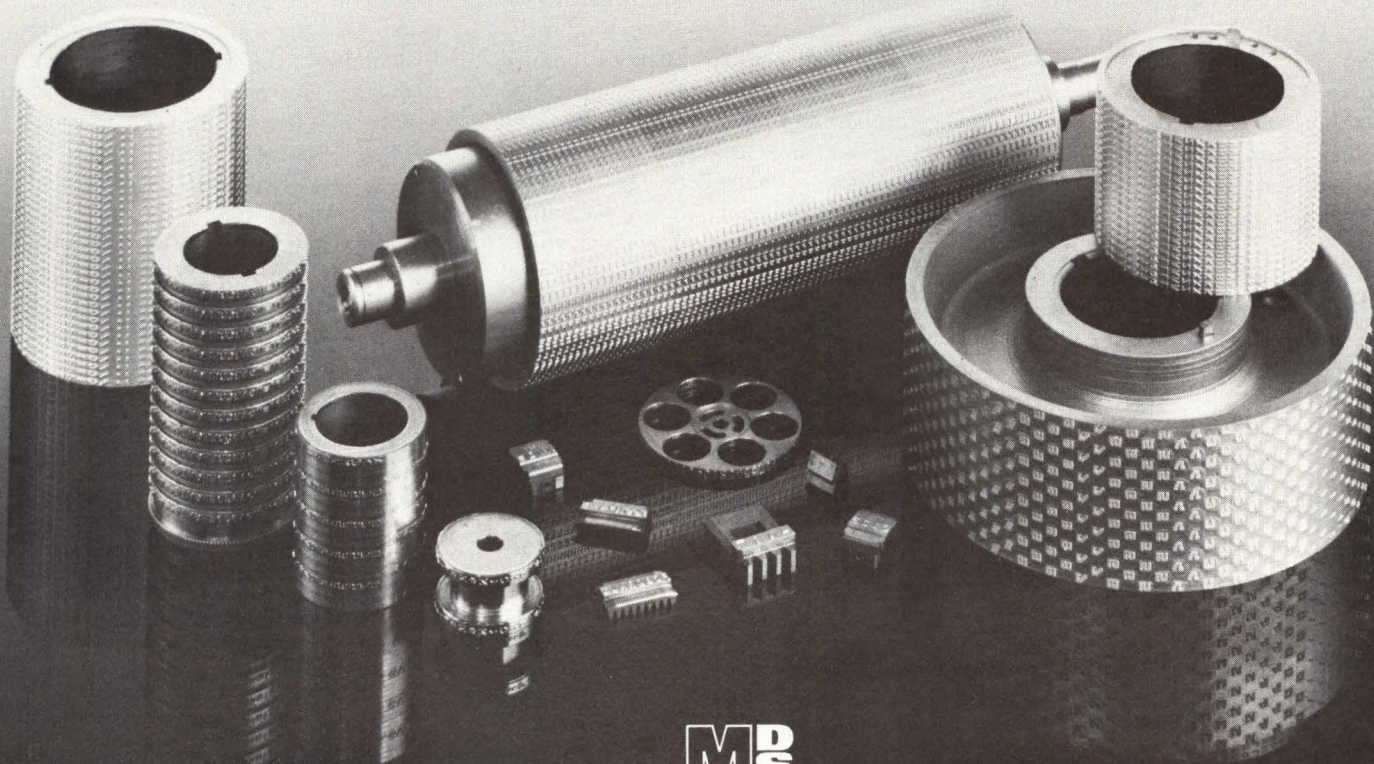
Street _____ City _____

State _____ Zip _____ Phone (____) _____

Mark Stamp Steel, a division of Mohawk Data Sciences Corp.,
Palisade Street, Herkimer, N.Y. 13350
Telephone: (315) 866-5300 (Ext. 5406).

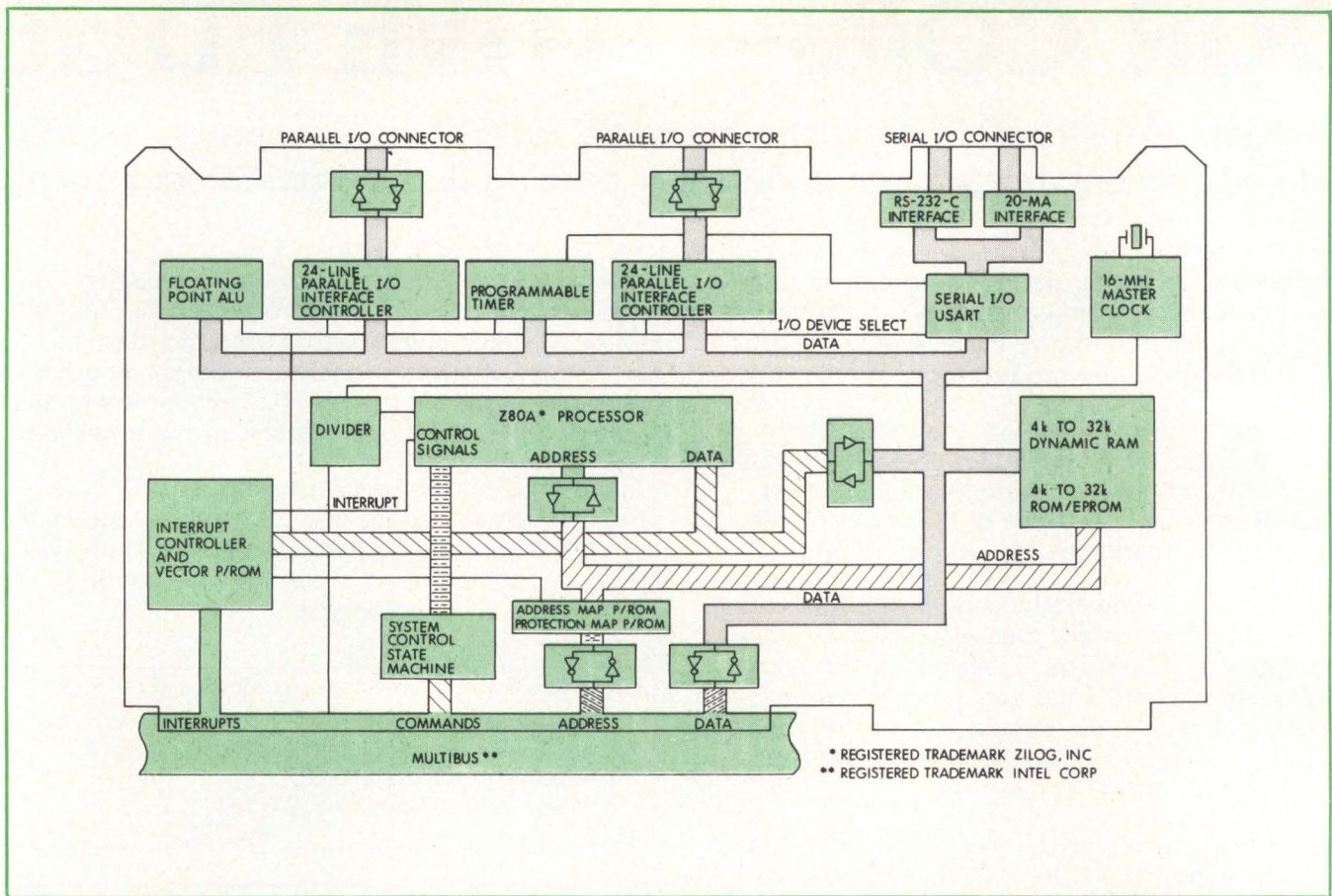
CD 3-79

CIRCLE 102 ON INQUIRY CARD



MDS

Mohawk Data Sciences



refresh cycle is automatic, and hidden so that requested memory operations are performed with minimum time delay. Four ROM/EPROM sockets accommodate most 8-bit wide 1k, 2k, 4k, or 8k memory devices with standard 24-pin callout. A protection P/ROM allows selection of system resources available to other Multibus masters. Any or all of the RAM, ROM, or I/O subsystem may be protected from external access.

RAM and EPROM are addressed under P/ROM control on 256-byte boundaries. An optional feature provides two complete address maps under program control. The system always powers up under the first map. Since the system has to have a ROM at location zero to start properly, a ROM is mapped into low memory. Then the program switches to the map that contains RAM in low memory. This capability permits the use of software written for 8080 and Z80A processors that previously could not be run on a single-board computer.

Data are transmitted and received in either parallel or serial form. A

serial I/O interface designed around a universal synchronous/asynchronous receiver/transmitter (USART) and a programmable timer matches current serial data transmission protocols and permits configuration for either RS-232-C TTL or optoisolated 20-mA current loop operation. Serial baud rates of 75 through 9600 are software selectable. A pair of interface controllers receive and transmit information on 48 parallel lines of two edge connectors on top of the board. Each connector supports three 8-bit ports.

Vectoring is provided for eight levels of priority interrupt plus a nonmaskable interrupt. Because all onboard interrupt sources are open collector, a number of devices can share the same level. Three operating modes and priority assignments may be configured anytime during system operation via software control.

The nonmaskable interrupt provides a method of dealing with system power failure or for diagnosing certain hardware and software problems. Because this interrupt functions independently of existing

interrupt hardware, a power-fail service routine can be added to an existing SBC 80 program without major changes.

Most of the microcomputer's logic is synchronous with the master clock. A standard 16-MHz master clock frequency is used to derive the 8-MHz bus clock. Additional independent system timing functions include power up, initialization, and watchdog timer.

Power requirements are 5, -5, 12, and -12 V to match the Multibus. Physical dimensions are 12 x 6.75 x 0.5" (30.5 x 17 x 1.3 cm).

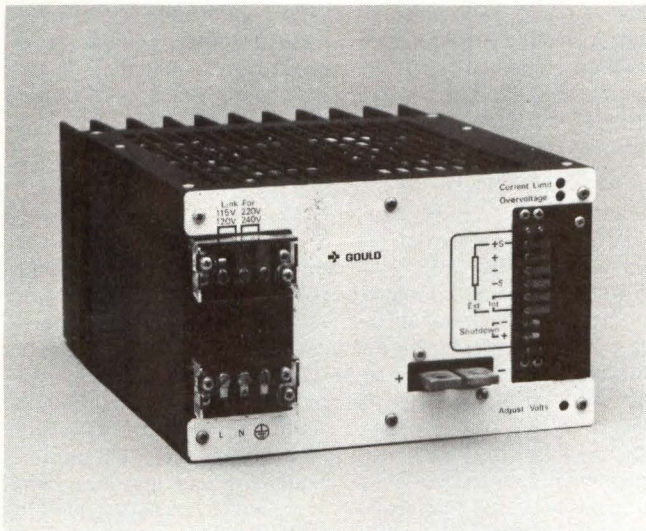
Price and Delivery

Single-quantity price for the MSC 8004 single-board microcomputer with 16k bytes of RAM, all serial and parallel I/O, and the Am9511 floating point processor is \$1440. OEM quantity discounts are available. Typical deliveries are 30 to 45 days ARO. Monolithic Systems Corp, 14 Inverness Dr East, Englewood, CO 80112. Tel: 303/770-7400.

For additional information circle 199 on inquiry card.

The big switch

...is to full cycle holdup.



The 500 watt MG5-100: 28 millisecond holdup.

Switching power supplies offer substantial holdup. Linears don't.

A Gould switcher will give you full regulated output at -20% line. Or during complete loss of power you'll get full output power for more than a missing line cycle.

Switchers offer other benefits too. They're 1/3 the size and 1/4 the weight of linears.

And they save energy with efficiencies of up to 85%.

Gould offers single and multiple output switchers with power levels from 8 to 2,250 watts. Custom designs can be provided to meet your exact specifications. You'll be backed by a high volume production capability and worldwide service network that only a \$1.6 billion company like Gould could offer.

For more information or to arrange for an evaluation unit, contact Gould Inc., Electronic Power Supply Division, P.O. Box 6050, El Monte, CA 91731. Phone (213) 575-4777.

Gould.
The power in switching power supplies.

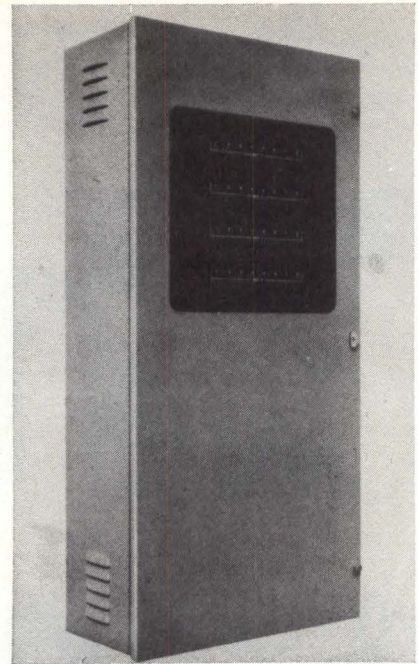


PRODUCTS

Microprocessor Based Remote Control Unit Capable of Controlling Up to 32 Loads

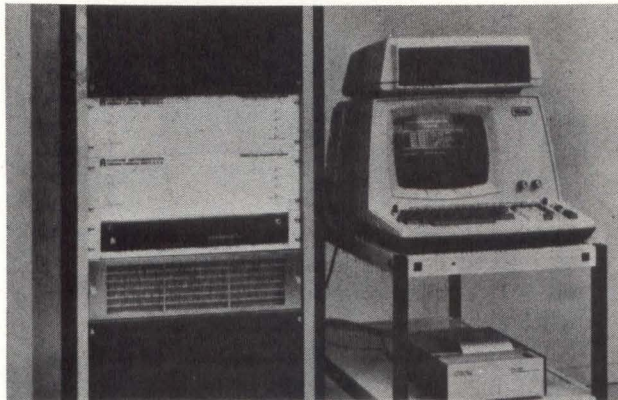
Designed to monitor digital and analog input signals, transmit data over telephone lines to a host computer, receive instructions back, and execute local control in event of a communications failure, the RCU 400 features 8080A microprocessor, capability of controlling up to 32 loads, power distribution assembly with battery backup, and communications with host computer over std telephone lines. The microcomputer chassis incorporates a PC motherboard which interconnects various plug-in modules, eliminating backplane wiring. Since functions are modularized, maintenance can be performed on a module exchange basis. Program storage is provided by EPROM and data storage by RAM. Max system configuration allows up to 32k EPROM and up to 32k RAM. Full duplex serial communications is provided by the communications module. Single- and dual-channel modules include RS-232-C and current loop interface. I/O interface is provided by a 32-channel photoisolated 24-Vdc input module and 16-channel photoisolated 24-Vdc output modules. **Detection Sciences, Inc, Digital Systems Div, 14050 21st Ave N, Minneapolis, MN 55441.**

Circle 200 on Inquiry Card



Data Acquisition System Provides Complete Data Reduction Capability

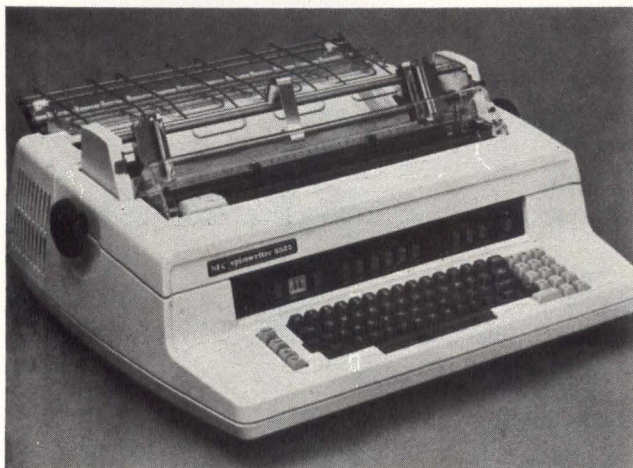
A complete data acquisition, control, and data reduction system, the 7252C includes a computer with built-in math



functions. The system contains 10 low level inputs for thermocouples, RTD, strain gauges, or millivolt signal; 5½-digit full function DMM with reading rate of 12 samples/s; scanner/mainframe with capacity for 13 extra I/O cards; and 80-col, 320-char/s utility printer. The 9" (22.9-cm) CRT can display 16 lines of 64 char, bargraphs, and quasi-graphics. The computer has a std ASCII keyboard plus 43 special function keys. It operates in BASIC and has most BASIC terms as single keystrokes. Included are a 42k BASIC interpreter ROM, 8k RAM (expandable to 32k), and an 89k mini-diskette (expandable to 178k). Std software packages are provided for $Y = MX + b$ linear scaling, linearization for 6 thermocouple types, limit setting with 4 limit points/channel, individual labeling for each channel, exception reporting, output relay, DAC, pulse or digital control, and signal averaging. Math functions include std arithmetic operators as well as mathematical functions; exponential functions in degrees, radians, and gradians; and matrix functions. **FI Electronics, 968 Piner Rd, Santa Rosa, CA 95401.**

Circle 201 on Inquiry Card

RO and KSR Printer Terminals Provide Six Selectable Data Transmission Rates



Spinwriter model 5515 receive-only and 5525 keyboard send-receive terminals are microprocessor controlled serial impact printers that operate on communications lines at data rates to 1200 baud. Using the company's thimble printing element, the units print at speeds to 55 char/s in an online communications environment. Both support RS-232-C communications interface, as well as an optional current loop interface. Compatible with Diablo 1610 and 1620 terminals, the printers duplicate their escape-code sequences and are fully compatible with existing software routines, including plotting software. Additional benefits include expansion of printable character sets from a max of 88 to 128 char, including the full 94 printable ASCII chars; a 16% increase in print speeds, from a max of 45 char/s to up to 55 char/s; and up to 6 std operator-selectable data transmission rates, including 110, 150, 200, 300, 600, and 1200 baud. Noise level output of the terminals is 67 dBA without covers, and as low as 60 dBA with die-cast aluminum cover installed. **NEC Information Systems, Inc, 5 Militia Dr, Lexington, MA 02173.**

Circle 202 on Inquiry Card

Xylogics Technology Delivers an LSI-11[®] Cartridge Disk Controller.

Xylogics advanced state-of-the-art technology has done it again.

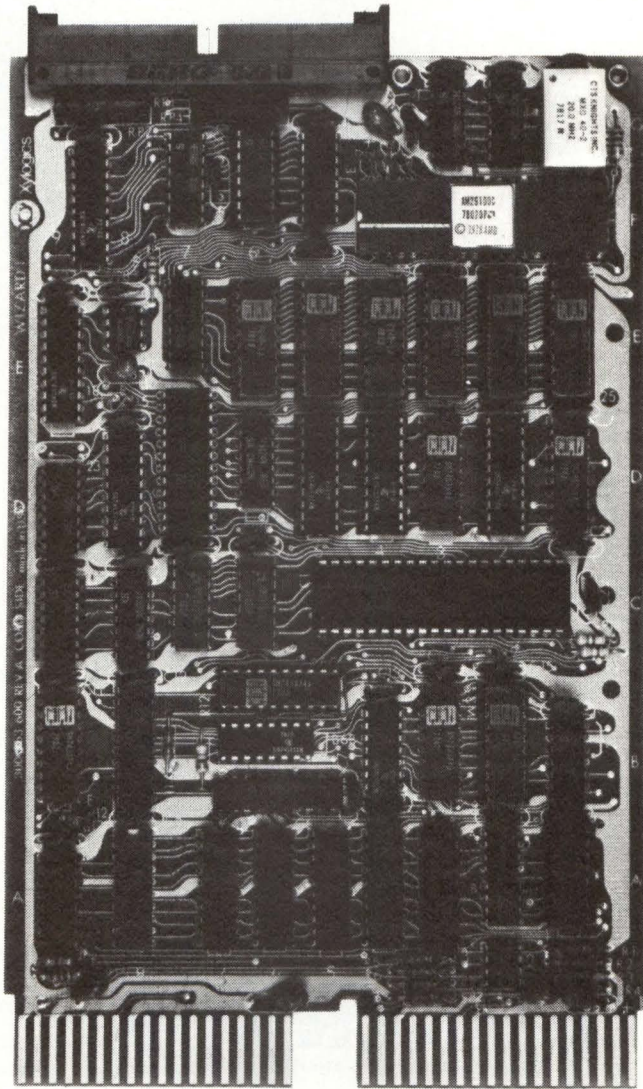
Now you can get the Model 510 Wizard, the only microprocessor based hard disk controller on a dual width board. This means fewer electronic components and best of all, superior controller performance in a cost-effective package.

The Model 510 Wizard provides the LSI-11 user with the on-line storage capacity flexibility of cartridge disk technology. Emulating the RKV11, the self-contained bootstrap permits direct start-up of RT-11 without need for a REV11 card. Subsystems using the Model 510 Wizard are available with 5MB, 10MB and 20MB cartridge disk drives.

Xylogics also offers complete LSI-11 based systems with software to meet most applications.

At single quantity price of only \$1995, including ROM bootstrap loader, the Model 510 Wizard looks good. Add in quantity discounts, performance, and reliability that comes from Xylogics technology and you'll see that Xylogics delivers outstanding results.

Call or write today.



Xylogics

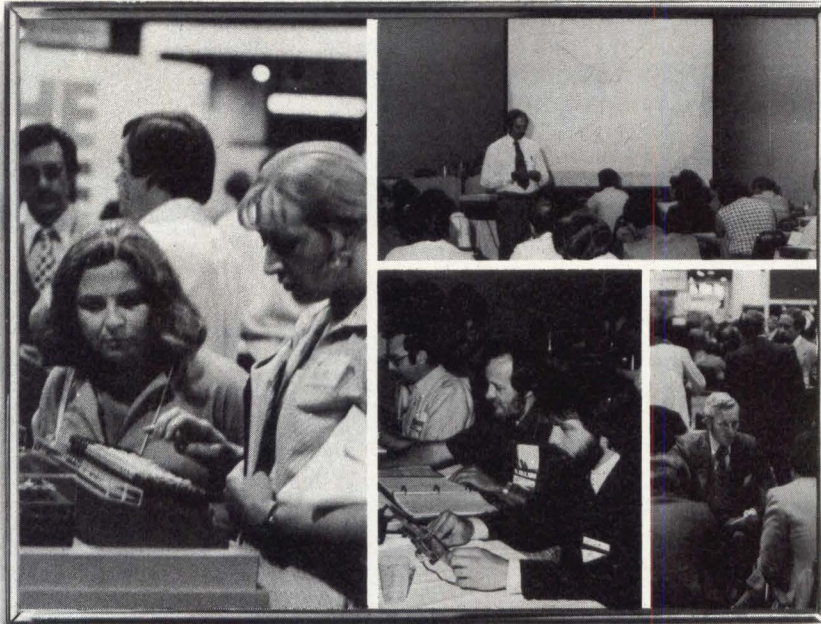
®LSI-11 is a registered trademark of Digital Equipment Corp.

Xylogics, Inc., 42 Third Avenue, Burlington, Massachusetts 01803 (617) 272-8140

We did it with . . . innovation/imagination/integrity

JOIN THE CLASS OF '79

National Computer Conference June 4-7



A unique and extraordinary learning experience will be available to you at the 1979 National Computer Conference, June 4-7 in New York City. The combination of more than 150 technical and professional sessions, a record-breaking exhibit of 1,700 booths, 16 Professional Development Seminars, a comprehensive Personal Computing Festival, plus a wide range of special events will make NCC '79 an exceptional educational offering.

For \$60 you can register in advance for the technical and professional program, conference exhibits, and the Personal Computing Festival — a \$15 savings on full-conference registration on-site. And you can add to this value by taking advantage of the one-day Professional Development Seminars, each available at \$50 including complete course material.

The conference program will meet

the needs of commercial and industrial users through sessions on management, marketing, applications, and the impact of computers on society. Special "mini-conferences" will cover such areas as use of computers for financial transactions, in law and public policy, in health care, as well as privacy and security.

Emphasis at the Professional Development Seminars will be on database/data communications, mini/micro technology, the automated office, and structured methodologies. Specific topics range from database machines, implementing a word processing system, and structured systems design to computer systems performance, human engineering in teleprocessing systems, and an introduction to microprocessors.

And there's more. At the NCC '79 Personal Computing Festival you'll learn about the latest developments in microcomputer systems and services for personal or business use. The Festival will feature more than 25 sessions, noncommercial applications demonstrations, and commercial exhibits by more than 100 participating organizations.

Join the NCC class of '79. To pre-register for the full-conference program and exhibits... or to obtain additional information on NCC '79, including complete details on other registration categories and housing... use the coupon below. Whichever registration category you select, or whether you attend as a guest of a participating exhibitor, your badge will be mailed to you well in advance of the conference. Deadline for advance registration is May 15.

REGISTER NOW:

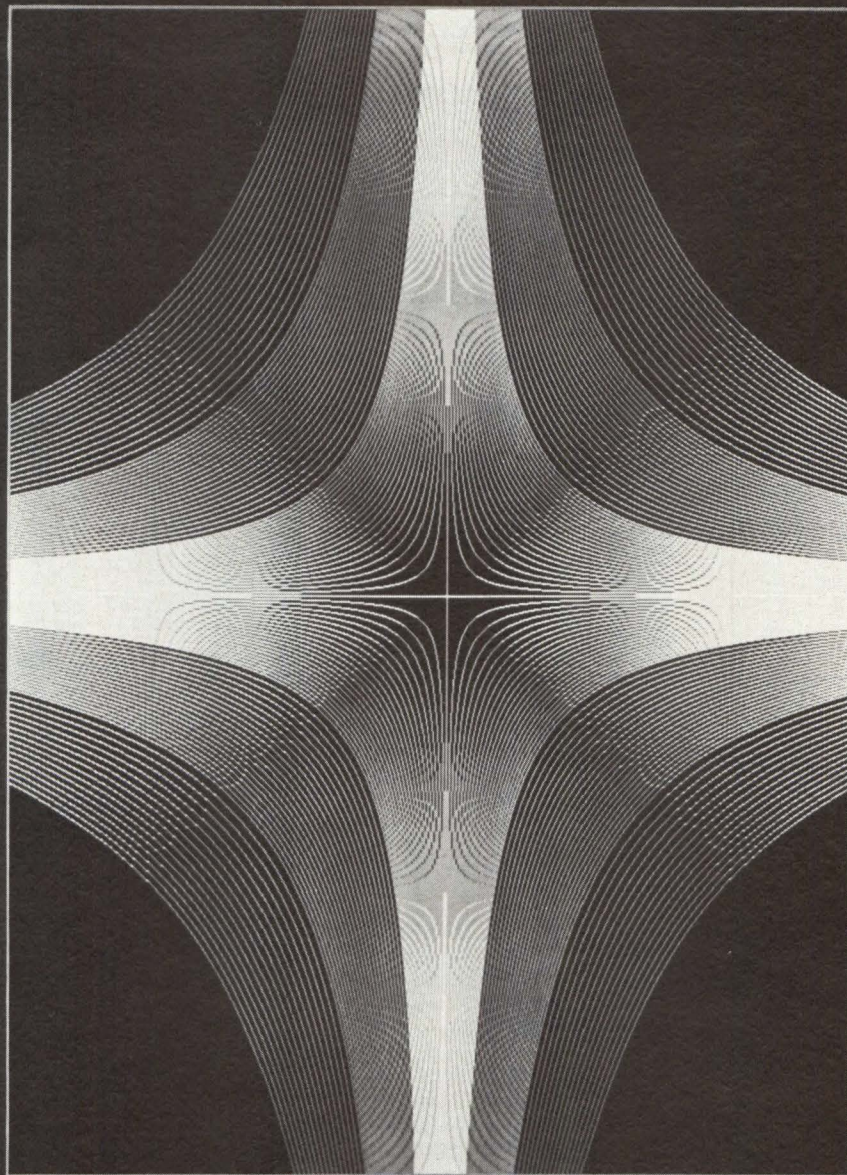
To be part of the picture at NCC '79, return this coupon today.
 Send to: NCC '79, c/o American Federation of Information Processing Societies, Inc., 210 Summit Ave., Montvale, N.J. 07645.
 Or telephone: 201/391-9810.

- I wish to preregister for the full conference and have enclosed \$60.
- Please send me additional information on NCC '79, including housing and registration.
- Please send me information on the Professional Development Seminars.
- Please send me information on the NCC '79 Travel Service.



Name _____
 Title _____
 Company _____
 Street _____
 City _____ State _____ Zip _____

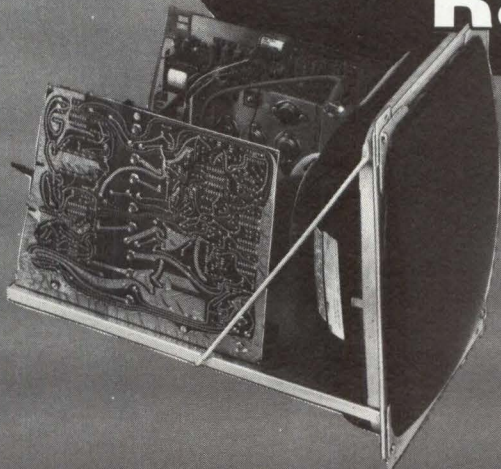
Only from CPT



Raster-scan graphics as pretty as this picture.

But it's not just another pretty OEM data display module. Consider:

- generates 1,024 X 768 pixel raster
- 105 megahertz band-width
- mono-chromatic
- non-interlaced raster scan



FOR MORE INFORMATION
OR A DEMONSTRATION WRITE:

CPT

CORPORATION

OEM SALES MANAGER
1001 SECOND STREET SOUTH
HOPKINS, MINNESOTA 55434
OR PHONE: (612) 935-0381

WORD'S GETTING AROUND...FAST!

CIRCLE 105 ON INQUIRY CARD

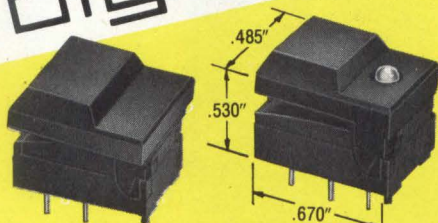
Low profile Schadow Modular Switches

disc



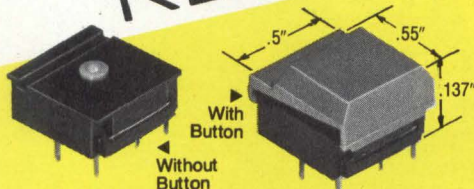
- Low cost
- 3 point sealed contacts
- High reliability
- SPST, momentary, crisp tactile feel
- Cycle life: 5×10^6 @ 50mA
- Broad range of switching power...from a few milliwatts to 30 watts
- Low bounce (less than 100 micro-seconds)
- Variety of actuators with or without L.E.D. illumination

digitast



SPDT momentary switch with crisp, tactile feel. Cycle life: 5×10^6 @ 20mA. Black, white, red, blue, grey, green, orange, yellow buttons. L.E.D. illumination and graphics optional. Variety of cap styles.

REK



Flat compact design. Low cost. SPST or SPDT. Crisp, tactile feel. Cycle life: 1×10^5 @ 10mA. Electrical rating: 20mA. Black, white, red, blue, green, orange, yellow buttons with or without graphics.

Fast service on free samples, specs and price quotations.

Ask for switches by our first name

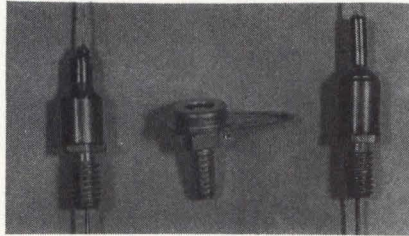
...Schadow

ITT Schadow Inc.
8081 Wallace Road, Eden Prairie, MN 55344
612/944-1820 • TWX 910-576-2469

ITT Schadow

PRODUCTS

EDGE, SURFACE, AND LASER DIODE LIGHT SOURCES



Edge emitting diodes T-820 and T-823 are of stripe geometry GaAlAs double heterojunction design with current confinement action for improved coupling. T-810 and T-813 surface emitting diodes of high radiance GaAlAs double heterostructure design have approx $150\text{-}\mu\text{m}$ dia etched well in substrate for light emission. Emitting region dia is about $50\ \mu\text{m}$. Models T-910 and T-912 double heterojunction AlGaAs injection laser diodes of stripe geometry yield low threshold current values and small source dimensions. All device outputs are compatible with silicon PIN and APD detectors. **ITT, Electro-Optical Products Div**, 7635 Plantation Rd, Roanoke, VA 24019.

Circle 203 on Inquiry Card

RACKMOUNTED POWER SUPPLY DESIGN KIT

Kit allows engineer to select features, lay out power supplies to suit application, and determine cost. Amassed of std components, systems are delivered assembled, with power supplies installed, and wired and tested. Front panel configurations may include push-button selector switches, lighted circuit breaker, front panel voltage adjustment, digital volt/amp meter, LED output indicators, individually fused modules, perforated rack cover, and slides. **ACDC Electronics, Div of Emerson Electronics Co**, 401 Jones Rd, Ocean-side, CA 92054.

Circle 204 on Inquiry Card

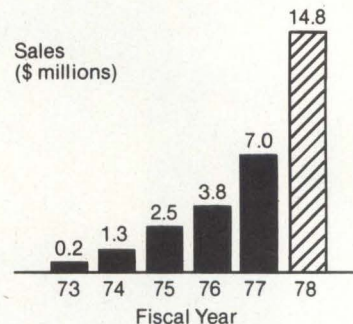
4-CHANNEL SYNCHRONOUS MULTIPLEXER

Data transmission economies are achieved with DDS circuits or regular telephone lines by splitting the available data rate between several terminals. Micro700 is a 4-channel, bit-interleaved time-division multiplexer that permits up to 4 synchronous data terminals to share a single telephone line or DDS link, operating at speeds to 19.2k bits/s. Channels may operate at $\frac{1}{4}$, $\frac{1}{2}$, or $\frac{3}{4}$ the phone line's modem data rate. **Micom Systems, Inc**, 9551 Irondale Ave, Chatsworth, CA 91311.

Circle 205 on Inquiry Card

ENGINEERS AND PROGRAMMERS — GROW NEAR SAN FRANCISCO

Back in 1973, when we started, sales of Triad computer systems were only \$200,000. Last year we sold nearly \$15 million worth of systems, and next year we'll deliver even more. You may find it hard to believe, but we've grown to only 280 employees! Now we need a few more.



As a Triad employee in our new Sunnyvale headquarters on the San Francisco Peninsula, you'll be part of the leading supplier of turnkey, on-line multi-terminal computer systems for a number of distribution industries.

Triad needs engineers and programmers to design computer systems, including CPUs, interfaces, controllers, terminals, and systems and applications programs. Projects involve conception, specification, development, generation of final documentation and training manufacturing, field service and sales personnel. Positions are available for both experienced professionals and recent college graduates.

Consider your growth opportunities. Consider the excitement of being part of an industry-leading computer systems company. Consider living in, and exploring, this beautiful part of America. Send your resume to Don Ruder, Vice President of Engineering, Triad Systems Corporation, 115 Independence Drive, Menlo Park, CA 94025. We are an equal opportunity employer.



TRIAD
Systems Corporation

← CIRCLE 106 ON INQUIRY CARD

CIRCLE 107 ON INQUIRY CARD

INTERACTIVE LABORATORY SYSTEM

ILS

SETTING THE STANDARD IN SOFTWARE SYSTEMS FOR INTERACTIVE SIGNAL PROCESSING

PROGRAMMED IN HIGH LEVEL LANGUAGES

FOR PDP™-11 COMPUTERS

- RSX-11 (in FORTRAN)
- IAS (in FORTRAN)
- RT-11 (in FORTRAN)
- UNIX (in C)

FOR VAX™-11/780 SYSTEMS

- VAX/VMS™ (in FORTRAN)

™ Trade Mark of Digital Equipment Corp.

NOVA™ & ECLIPSE™ SYSTEMS

- RDOS (in FORTRAN)

™ Trade Mark of Data General Corp.

STANDARD FILE STRUCTURES

- SAMPLED DATA FILES
- ANALYSIS FILES
- RECORD FILES
- LABEL FILES

INTERACTIVE OPERATION

- GRAPHICS
- STATISTICS
- PATTERN RECOGNITION
- DATA SCANNING
- DATA MANIPULATION
- SIGNAL PROCESSING
- SPEECH ANALYSIS

At a purchase price of \$4,500 ILS saves time and money in program development, and provides an organized software system with sharable programs and files. With its 85 command programs, and 250 subroutines, ILS contains a wide variety of tools for signal processing, and lets you concentrate on your specialized applications rather than system design and routine program development. The software is distributed in source form, along with the necessary command files to build the system. Documentation includes an installation manual, 400 page users guide, training manual, and programmers guide. Support covers consultation, updates, error corrections, and newsletter.

For Further Details, Contact Dr. Larry Pfeifer



SIGNAL TECHNOLOGY, INC.

15 West De La Guerra □ Santa Barbara, CA 93101 □ (805) 963-1552

PDP-11* interface . . . from MDB

Peripheral Device Controllers ■ Systems Modules
General Purpose Interface Modules
Communications/Terminal Modules
I/O Cables ■ Accessory Hardware

When it comes to PDP-11 interface, MDB has it:

- Peripheral Device Controllers for most major manufacturer's
 - Printers
 - Card equipment
 - Paper tape equipment
 - Plotters
- Systems Modules
 - IEEE instrumentation bus
 - DR11B Direct Memory Access single quad module
 - DR11C General Purpose Interface module, a direct DEC equivalent
 - Digital I/O Module
 - Unibus Terminator
- General Purpose Interfaces
 - 11B Direct Memory Access with 12 IC positions for user logic
 - 11C Module with 16 bit input and 16 bit output registers; 20 user wire wrap positions
 - 1710 Bus Foundation Module with pins for 40 user IC positions
 - Wire Wrappable Module with pins for 70 user IC positions
- Communications/Terminal Modules

MDL-11 Asynchronous

Serial Line Adapter
MDL-11W Asynchronous Serial Line Adapter with line frequency clock

MDU-11 Synchronous Serial Line Adapter

- Cable Subassemblies
 - I/O cable for 20mA current loop
 - I/O cables for EIA Asynchronous and Synchronous
 - Double-ended jumper cable
 - GP I/O 50, 40, 34, 26 and 20 conductor ribbon cables

MDB interface products always equal or exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are completely software transparent to the host computer. MDB products are competitively priced, delivery is 14 days ARO or sooner.

MDB places an unconditional one year warranty on its controllers and tested products. Replacement boards are shipped by air within twenty-four hours of notification. Our service policy is exchange and return.

MDB also supplies interface modules for LSI-11*, IBM Series/1, Data General and Interdata computers. Product literature kits are complete with pricing.

MDB 1995 N. Batavia Street
Orange, California 92665
714-998-6900
SYSTEMS INC. TWX: 910-593-1339

*TM Digital Equipment Corp.

PRODUCTS

0.4" DIP DISPLAYS AVAILABLE IN FOUR COLORS

MAN4000 series 0.4" (1.02-cm) displays feature a choice of orange, green, red, or yellow, and come in std 14-pin DIP with the same package size and lead configuration as the company's 0.3" (0.76-cm) displays. They are available in common cathode right hand decimal point, common anode right hand decimal point, and universal overflow (± 1) models. **Monsanto Commercial Products Co., Electronics Div**, 3400 Hillview Ave, Palo Alto, CA 94304.

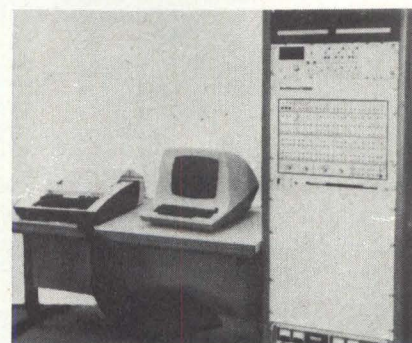
Circle 206 on Inquiry Card

DISC CONTROLLER FOR NOVA/ ECLIPSE TYPE COMPUTERS

All computers of the Nova and Eclipse type can accommodate up to 4 storage module or cartridge module drives with the 850 disc controller, providing storage capacity of 1.2G bytes of unformatted data. Utilizing a microprogrammable processor, the unit emulates the Data General 606X. Media compatibility can be obtained with Memorex 601 or 677, and CalComp T-100 or T-200 drives with storage module type interface. **Xylogics, Inc**, 42 Third Ave, Burlington, MA 01803.

Circle 207 on Inquiry Card

DYNAMIC BURN-IN MEMORY TEST SYSTEMS



Basic characteristics of model 5004 are a 1M-word address field of up to 48 bits, and 100-ns (10-MHz) cycle time. System consists of special purpose microprogrammed ECL computer with general purpose microprocessor for program control and generation. It has 0.5M-bit dual floppy disc data storage and 15k-bit static RAM. Furnished software is SYSGEN, program development, and ERRPAC failure analysis and error logging package. Options include CRT terminal, line printer, automatic power supply margining, and programmable clocks. **TestMaster**, 3191-D Airport Loop Dr, Costa Mesa, CA 92626. Circle 208 on Inquiry Card

The smart, reliable **TELERAY 1061:**



Highest Ever Features/Price* Ratio

*\$1090 list (desk stand optional)

NEW!
32 keyboard-
programmable functions

Call up forms, control sequences, etc... using up to 527 characters in any combination. **PLUS** these standard 1061 features:

- Independent I/O and peripheral speeds—programmable.
- Format and protect modes—dim, blink (or blank), underline and inverse video—programmable in any combination.
- Programmable tabs—up to 16 column positions.
- Monitor mode—32 control codes displayable.
- Peripheral port, RS232C—programmable enable/disable.
- No-tools self-service in seconds, with snap-out, snap-in modules.
- Block mode transmission—page, part of page, line, part of line, and character by character.
- Programmable wide (40/line) or standard (80/line) character format with clear, readable 7x9 characters.
- Insert and delete—character or line at a time.
- Clear—page, to end of page, to end of line.
- SUPER SERVICE—replacement modules in reusable mailers... it works!

And many more feature/benefits... hard to believe at the price.

Call your nearest **TELERAY** Sales Office.

TELERAY Sales Offices:

(201) 652-7055	(301) 589-2802	(412) 243-8421	(613) 225-0411
(201) 944-1600	(303) 279-7796	(416) 622-6752	(617) 459-2578
(203) 623-5352	(305) 421-4989	(503) 292-3505	(713) 780-2511
(205) 881-9298	(305) 645-3444	(512) 451-5174	(714) 273-4771
(206) 641-6444	(312) 655-0040	(512) 828-0937	(714) 552-7850
(212) 947-0379	(313) 354-6421	(513) 223-8421	(716) 381-4120
(213) 328-9770	(404) 955-0293	(518) 587-2313	(801) 969-4034
(214) 661-0300	(405) 528-6071	(602) 968-5962	(808) 523-1326
(216) 585-8421	(408) 744-1930	(612) 535-5330	(919) 883-9125

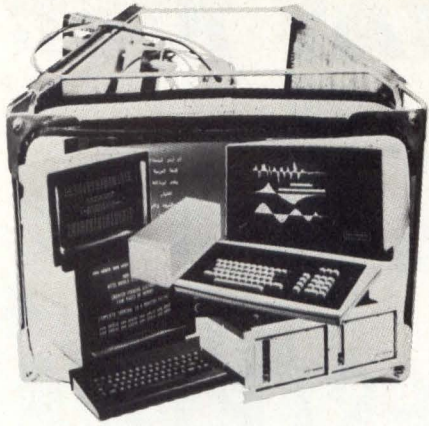
SEE US AT INTERFACE '79

TELERAY



DIVISION OF
RESEARCH INC

BOX 24064 MINNEAPOLIS, MINNESOTA USA 55424
PHONE (612) 941-3300



When An Off-The-Shelf Display Terminal Just Won't Do . . .

...CALL ANN ARBOR!

Lots of manufacturers offer vanilla terminals that meet *their* specifications. And, in lots of applications, that may be all you need. But, if you're a design engineer with a tailored system in mind, why sacrifice it to comply with your CRT's limitations? You do have an alternative. Ann Arbor sells *user-defineable* terminals.

We take a standard CRT design (ours or one of the vanilla manufacturer's), and add the extra function keys you want...delete the features you don't use...vary the display configuration...customize the character set...match the packaging to your user's en-

vironment. In short, we fit our terminal to *your* systems design.

All at a surprisingly low cost to you!

So if you're in the market for CRT displays, and vanilla isn't your favorite flavor, contact us at 6107 Jackson Road, Ann Arbor MI 48103. Tel: 313-769-0926 or TWX: 810-223-6033.

ANN ARBOR
TERMINALS, INC

CIRCLE 181 ON INQUIRY CARD

ROYTRON™ plug-compatible reader/punch

Desktop combination reader/punch with serial asynchronous RS-232C compatible interface. Designed to operate with a terminal device on the same serial data lines or alone on a dedicated serial line. Reader will generate data at all standard baud rates up to 2400 baud.

Punch accepts data at all standard baud rates up to 600 baud continuous or 4800 baud batch, utilizing a 32 character buffer.

Two modes of operation are provided: *Auto Mode* — Simulates Model ASR 33 Teletype using ASCII defined data codes (DC 1, 2, 3 and 4) to activate/deactivate the reader or punch; *Manual Mode* — Code transparent mode. Panel switches control activation/deactivation of reader or punch and associated terminal device.

Tape duplication feature is provided by setting unit to LOCAL mode.



MODEL 1560-AS

High-speed, compact, with self-contained electronics and power supply. Complete in attractive noise dampening housing.



For full details, write or call us.

SWEDA INTERNATIONAL, INC.
Litton O.E.M. Products

34 Maple Avenue, Pine Brook, N.J. 07058/(201) 575-8100

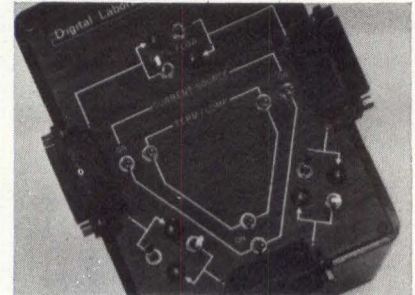
IN U.K. — ADLER BUS. SYSTEMS/OEM PRODS., Airport House, Purley Way, Croyden, Surrey, England

IN FRANCE — SWEDA INTERNATIONAL/OEM, 103-107 Rue de Tocqueville, 75017 Paris, France

CIRCLE 182 ON INQUIRY CARD

PRODUCTS

DIRECT DATA TRANSFER INTERFACE



Direct computer to computer connections and communication between serial devices are handled without software modification by the 3R universal junction unit. Measuring 5.3 x 2.3 x 7" (13.5 x 5.8 x 18 cm), the connection box has 3 ports, each with switches to interchange transmit and receive signals, and establish operation in the RS-232-C or 20-mA mode. Additional switches provide 63 possible connections between I/O devices. **Digital Laboratories Inc.**, 600 Pleasant St., Watertown, MA 02172.

Circle 209 on Inquiry Card

TAPE PUNCH CODE CONVERTER

Model 5071 code converter perforator is an intelligent tape punch using the 75-char/s asynchronous Facit 4070 mechanism. A microprocessor in the interface enables any 5-, 6-, 7-, or 8-level code to be converted to another 5-, 6-, 7-, or 8-level code by change of control memory. Current versions include ASCII to Baudot, Baudot to ASCII, hex to EIA, and EIA to hex. Both RS-232-C and current loop (20 to 60 mA) are provided as input circuits. Power requirements are 110/127/220/240 Vac, 40 to 62 Hz. **Data Science**, 1189 Oddstad Dr, Redwood City, CA 94063.

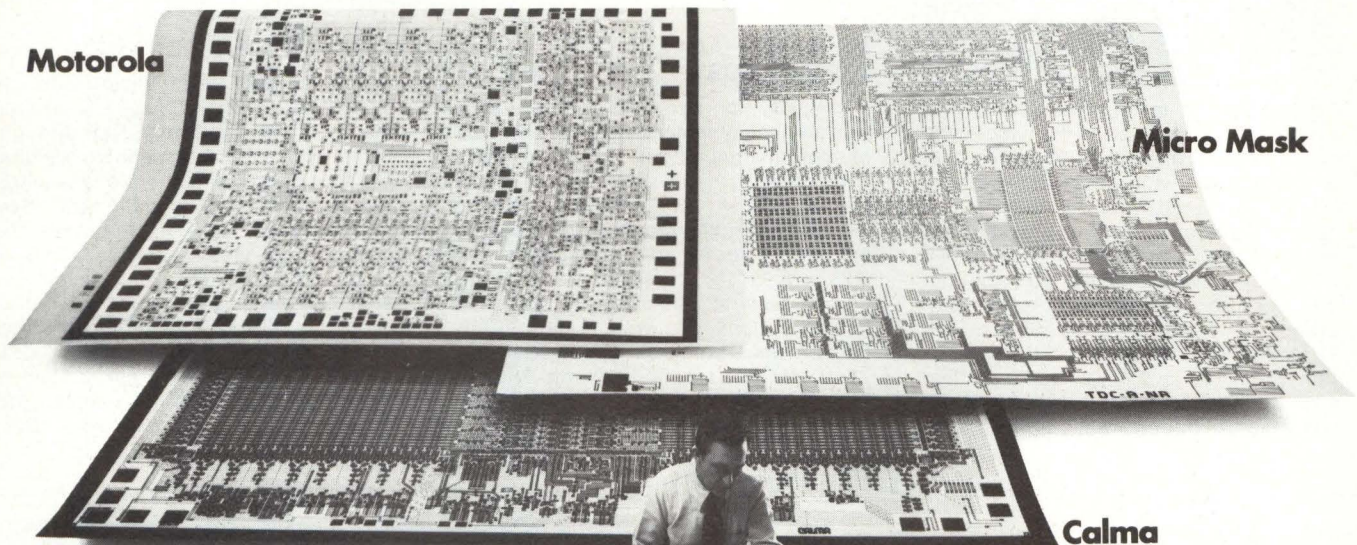
Circle 210 on Inquiry Card

TRANSPARENT POSITION SENSOR FOR CRTs

Formfitting CRTs in displays and computer terminals, E270 allows the operator to interact with the system by touching a point on the sensor to transmit coordinates of that point to the terminal. The sensor consists of a curved glass sheet coated with a transparent resistive substrate. A voltage is alternately impressed along orthogonal axes; at the point of contact, the voltages are digitized by an electronic controller, providing numerical coordinates. **Elo-graphics, Inc.**, 1976 Oak Ridge Tpk, Oak Ridge, TN 37830.

Circle 211 on Inquiry Card

Break the IC plotting bottleneck. With Versatec.

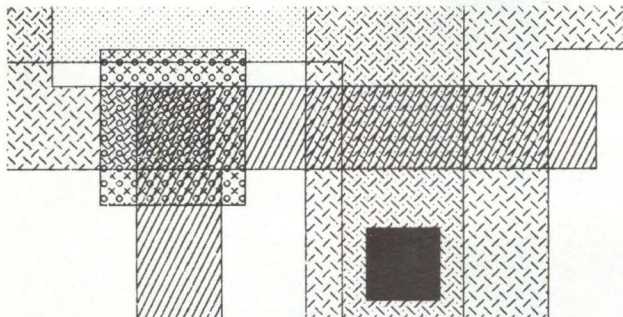


Calma does it. Motorola does it. ETEC helped Micro Mask do it. Leading IC system builders, semi houses and mask makers are breaking the IC plotting bottleneck with Versatec electrostatic plotters.

While your pen plotter is struggling to make one circuit drawing, they get two, three or more.

They produce plots more complex than anything you've ever attempted with a pen plotter. Up to four million vectors, not counting fill-in patterns.

Need clearer discrimination of levels? Their electrostatic plotters label circuit paths on different levels with shading, not color outlines. No more



penciled fill-ins by hand! And see how well shading patterns identify intersections.

They plot in widths up to six feet. On translucent paper for fast, accurate overlays.

Their electrostatic plotters cost less to buy, less to operate than pen plotters. They never lose plots to a skipping pen or a balky solenoid.

They were up and running fast. Versatec

hardware/software interfaces link to their computers and application programs.

They did it. So can you. Circle our number for literature, plot samples and the application report—"Plotting IC and PCB drawings." Versatec can end your CAD plotting bottleneck.

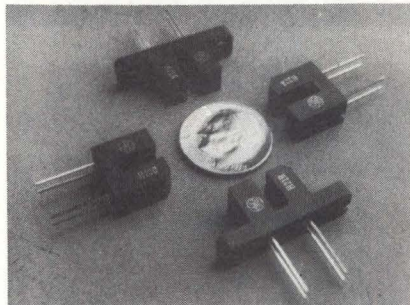
VERSATEC
A XEROX COMPANY

2805 Bowers Avenue, Santa Clara, California 95051 (408) 988-2800

XEROX® is a trademark of XEROX CORPORATION. Versaplot is a Versatec trademark. Sample plots courtesy of Calma, Motorola and Micro Mask. Shading patterns courtesy of Calma.

PRODUCTS

SUPERSENSITIVE INTERRUPTER MODULES



Equipment can take advantage of precision microprocessor performance with the series of interrupter modules that are compatible with most logic systems. H21/H22 provide up to 25-mA min specified output and 55-V blocking capability, and a consistent light beam with max dimensions of 1 x 1.5 mm; 12 transistor detectors feature low saturation voltage (≤ 0.4 V at 1.8 mA) and 12 darlingtonts feature high output current (≥ 50 mA at 1.5 V). **General Electric Co, Semiconductor Products**, W Genesee St, Auburn, NY 13021. Circle 212 on Inquiry Card

SOLID-STATE RELAYS FOR COMPUTER PERIPHERALS

Available in all solid-state (zero voltage switching) and reed-coupled (high input noise immunity) versions, relays are provided with either chassis or PCB mount. Low voltage and low current triggering make the devices compatible with computer technology. 2500-Vac dielectric isolation is typ between I/O and base plate. Output ratings are from 0.5 A at 120 Vac to 40 A at 330 Vac. Built-in snubber network across output minimizes effects of line transients. **Essex Controls Div/Stancor Products**, 3501 W Addison St, Chicago, IL 60618. Circle 213 on Inquiry Card

MILITARIZED CARTRIDGE TAPE MEMORY

A memory for use with ROLM's militarized minicomputers stores 4.3M bytes of unformatted digital data on 3M's high capacity tape cartridge, or alternatively, 2.8M bytes on the std 3M DC300A cartridge. Model 5100-R weighs approx 14 lb (6 kg), measures 11 x 6.25 x 5.75" (28 x 15.88 x 14.61 cm), and is built to MIL-T-21200. Designed for continuous use within the -10 to 55 °C temp range, it can operate at 71 °C for short periods. **North Atlantic Industries, Inc, Qantex Div**, 60 Plant Ave, Hauppauge, NY 11787. Circle 214 on Inquiry Card

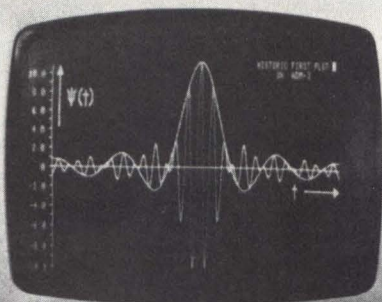
TOUCH INPUT FLAT PANEL DISPLAY

Displaying 12 lines of 40-char each, 2.5" (6.35-cm) thick flat panel also provides touch input capability, permitting rapid and efficient operator interaction using menu driven displays. The Vue-Point™ panel's microprocessor based controller provides all std smart CRT features plus touch response in matrix or screen echo modes, multiple display buffers, and alternate char sets. Communication is by std 300- to 19.2k-baud asynchronous RS-232 protocol. **General Digital Corp**, 700 Burnside Ave, East Hartford, CT 06108. Circle 215 on Inquiry Card

HIGH SPEED REMOTE LINE PRINTER INTERFACE

Sprintprint 300, compatible with all DEC CPUs, helps eliminate cost and delay of mailing and improves throughput of line communications simultaneously. Error correction on synchronous line assures data integrity. System includes two microprocessors, which provide an avg 300-line/min print speed using a 4800-baud synchronous serial communications channel. XON (DC1) and XOFF (DC3) protocol allows host micro to control data from CPU up to 9600-baud serial asynchronous. **Interactive Information Systems, Inc**, PO Box 37403, Cincinnati, OH 45222. Circle 216 on Inquiry Card

Retro-Graphics™



For your Dumb Terminal. The Retro-Graphics PC card mounts easily in the Lear Siegler ADM-3A to provide you with an affordable graphics computer terminal.

Features:

- Z-80 Based
- 512 by 250 Dot Matrix
- Simple Plug-in Interconnect
- Point Plotting
- Automatic Vector Generation
- Optional TEKTRONIX Software Compatibility

You will be impressed with the packaging, performance and price of the Retro-Graphics card. Write or phone today for complete specifications.

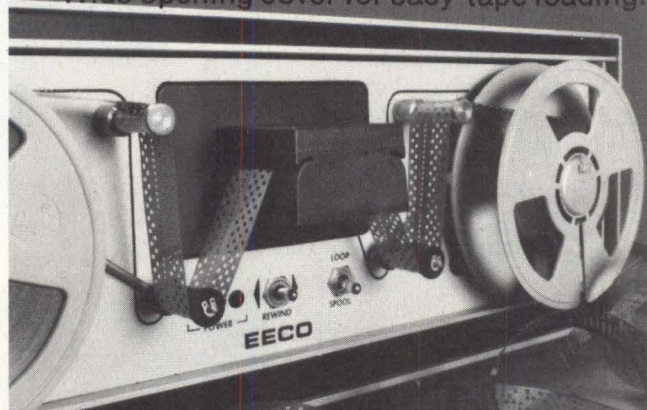
DIGITAL ENGINEERING, INC.

1787 Tribute Road, Suite K
Sacramento, CA 95815
(916) 920-5600

LOW COST TAPE READERS

Reader/Spooler for CNC and automatic Machine Control application.

- Reads tape at 200 cps
- High speed rewind
- Wide opening cover for easy tape loading.



Send for literature on EECO's 2001 Series.

EECO The Future in Tape Readers

1601 East Chestnut Avenue • Santa Ana, California 92701
(714) 835-6000

C-10000



THE FIRST TV CAMERA DESIGNED FOR COMPUTER INTERFACE

SUPERB RESOLUTION—

Observe minute detail with resolution over 1000 TV lines.

VIRTUALLY DISTORTION-FREE—

Image is accurate, linear from center of screen to outer edge with less than 0.2% distortion.

STABLE—

Less than 0.05% drift per 24 hours, less than 0.2% from 10° C to 40° C.

PLUS ALL LINES NEEDED FOR DIGITAL AND ANALOG COMPUTER INTERFACE

**THIS UNIT IS "INSTRUMENT QUALITY"
—NOT A VIDEO SYSTEM FOR
ENTERTAINMENT VIEWING**

APPLICATIONS:

MEDICAL

Tissue analysis
Blood analysis
Neurological—X-Y movement analysis
Optical Instrument data analysis
Other analysis of visual data

INDUSTRIAL

Aerial photography analysis—crop areas,
insect infestation
IR Analysis—detect forest fires, direct robot
fire fighters
Bottle inspection—using polarized light
Dimension analysis and control, area
measurement, displacement measurement
Printed pattern analysis and control
Missile tracking

UNIVERSITY

Analysis of any visual information that can be
measured through variation in light intensity
Medical research
Physics research
Laser technology

HAMAMATSU

HAMAMATSU CORP. • 420 SOUTH AVENUE • MIDDLESEX, NEW JERSEY 08846 • (201) 469-6640

PRODUCTS

IEEE STD 488-1975 BUS EXTENDER



Bus capability for distances up to 300 m is enabled by the GPIB-100 extender system, consisting of 2 GPIB-100 units plus interconnecting cable. 14 GPIB-compatible devices may be attached to std connectors on each unit allowing expansion of a system from 15 to 28 devices, plus the 2 extender units. Data and control signals are transmitted by differential RS-422 line drivers and receivers. Only 2-way cable propagation time reduces data rate. All bus functions transparent to user's software and hardware except parallel poll, whose response lags by 1 poll. **National Instruments**, 9513 Burnet Rd, Austin, TX 78758.

Circle 217 on Inquiry Card

RS-232-C INTERFACE FOR IR COMMUNICATIONS SYSTEM

Using std 25-pin EIA plug, interface permits connection of terminals, data concentrators, computers, and other data sources to the company's model 736 optical communicators for up to 10 mi (1.6-km) line-of-sight data transmission. All handshaking needed for either synchronous or asynchronous transmission is handled, as well as all aspects of RS-232-C protocol including either internal or external clocking in synchronous mode. Std rates to 9600 baud can be programmed into unit. Telephone quality voice channel is optionally available. **American Laser Systems, Inc.**, 106 James Fowler Rd, Goleta, CA 93017.

Circle 218 on Inquiry Card

PANA/BASIC[®] MULTIUSER SOFTWARE

The Most Comprehensive Software System Available for Microcomputers.

Our PANA/BASIC Software is the most comprehensive operating system available for microcomputers. It combines the power of ANSI COBOL file processing with the flexibility of a multiuser interactive operating system enhanced by the programming simplicity of BASIC. The result is a powerful yet simple system, which is ideally suited for handling a variety of functions such as: small business accounting, word processing and text editing, inventory control, media conversion, engineering/scientific analysis and interactive software development.

Our PANA/BASIC System offers you many features not available on other

microprocessor software:

- Multiuser capability
- Powerful string handling
- Time-shared multi-terminal operation
- Interactive data entry and control
- Quick response times
- COBOL style format edit control and string match
- Multiuser file protection
- File capabilities equivalent to ANSI COBOL
- AND MANY MORE

The system is available for a variety of microprocessors including Intel 8080/8085 and Zilog Z80.

For details, write us: Panatec, Inc.,
1527 Orangewood Ave., Orange, CA 92668.
Phone: 714 633-8961

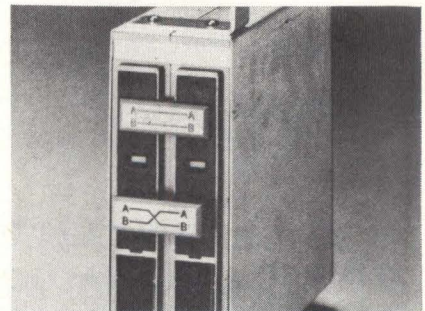
PANATEC

COLOR RASTER DISPLAY SYSTEM

Run length encoding on the CVD/2 compresses adjacent points of the same color to a single datum, achieving compression ratios of 30:1 for typ computer generated pictures, and permitting real-time animation display at 15 frames/s. Display generates 480-line by 640-point TV resolution pictures, with 64 colors selectable. Packaged with a minicomputer or in a std 4-slot system unit mountable in PDP-11 cabinets, system's character generation hardware provides software defined fonts with variable width and drop shadow. **Three Rivers Computer Corp.**, 160 N Craig St, Pittsburgh, PA 15213.

Circle 219 on Inquiry Card

COMMUNICATIONS CROSSOVER SWITCHING MODULE



Normal or cross-switching of the EIA RS-232/CCITT V.24 interface between 2 modems and 2 computer ports or terminals is permitted by this passive 2" (5-cm) wide modular switch with 4 rear connectors—2 for modems and 2 for data termination equipment. Two color-coded pushbuttons implement mechanical switching action; a color-coded indicator shows the status of the switch. All 24 leads of the interface are switched. The switch is freestanding or can be attached by mounting ears. **Dynatech Data Systems**, 7644 Dynatech Ct, Springfield, VA 22153.

Circle 220 on Inquiry Card

BEEHIVE'S MICRO B 1S

designed
for
emulation
plus!



Have you ever wished you could change terminal vendors without losing your investment in software? Well, the new socketed Micro Bee 1S can do exactly what you want. This terminal is perfect for the person who knows his application and needs, and can specify what he wants to do.

The basic terminal configuration comes with: 3K of RAM, plus sockets available for an additional 3K of RAM population for a total of 6K; six sockets for ROM (total 12K), all of which are depopulated; and a socketed/populated auxiliary port, character generator, and line drawing generator. The Micro Bee 1S offers full communications capabilities with a standard RS232C/current loop main port in addition to the bidirectional serial auxiliary port. The empty RAM/ROM sockets allow for the expansion capabilities of the terminal to meet a wide variety of customized product applications.

Beehive offers emulators for the DEC VT52™, Microdata Prism™, Data General Dasher™, ADDS Regent 100™ and Beehive's own Micro Bee 1A™ . . . for starters.

Plus . . . if the emulator you want is not available you can custom generate your own software for your specific applications!

Whether you want to buy a standard package from Beehive or develop your own highly specialized application software, why not give us a call today to learn more about this new and versatile product? *It's just what you've been looking for!*

TOLL
FREE
USA **(800) 453-9454**

or contact our sales office nearest you.

SALES OFFICES

USA: California (714) 540-8404, (408) 738-1560; **Colorado** (303) 343-7093; **Florida** (305) 830-4666; **Illinois** (312) 593-1565; **Massachusetts** (617) 272-7136; **New York** (212) 682-2760; **Ohio** (513) 435-7073; **Pennsylvania** (215) 825-0243; **Utah** (801) 355-6000; **Virginia** (703) 356-5133; **Washington** (206) 838-4881

EUROPE: Amsterdam, The Netherlands Phone 020-451522



**BEEHIVE
INTERNATIONAL**

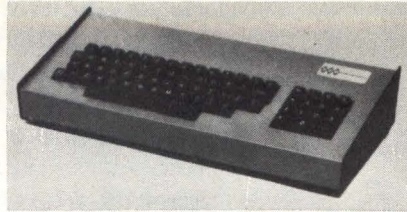
USA: 4910 Amelia Earhart Drive • Box 25668 • Salt Lake City, Utah 84125
Phone (801) 355-6000 • TWX 910-925-5271

EUROPE: Schiphol Airport • Building 70 Schiphol East • Amsterdam, The Netherlands
Phone 020-451522 • Telex 15284

PRODUCTS

KEYBOARD FOR MICROCOMPUTER SYSTEMS

Keyboard subsystem model 771 includes 56 alphanumeric keys providing entire 128-char ASCII u/lc set, and separate 15-key numeric/cursor control keypad. 4 encoding modes include uc only. 4 power supply options handle any supply source. Interface allows user selection of data, strobe, and parity



sense. Optional adapter converts keyboard to self-contained transmitter with 110- to 9600-baud RS-232 or current-loop serial data output. Std features include auto-repeat, 2-key rollover, and fully buffered outputs. **George Risk Industries**, GRI Plaza, Kimball, NE 69145. Circle 221 on Inquiry Card

Our new ChainTrain[®] 1210 zips along at 1000 LPM's ... and has inherited the best features of its 1200 LPM big brother.

We geared down the revs on our new Model 1210 — and we also geared down the price accordingly. Yet, we still gave it all the best features of its 1200 LPM Big Brother. The new Model 1210 has motorized upper and lower tractor positioning, heavy-duty ChainTrain reliability, and it's completely microprocessor controlled.

We geared down the LPM's but didn't take away any of the goodies. Write or call for all the pertinent facts.



DATA PRINTER CORP
99 Middlesex Street, Malden, MA 02148
Tel: (617) 321-2400 TWX: 710-348-0794
Sales Offices: Costa Mesa, CA, Clifton, NJ



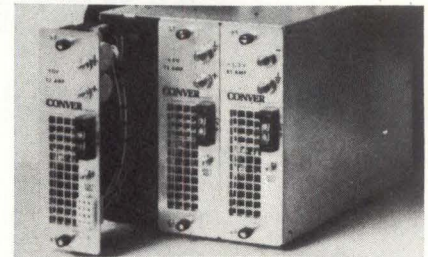
Visit Data Printer Corp. at Booth 1230,
INTERFACE '79, Chicago, April 9-12.
CIRCLE 151 ON INQUIRY CARD

PENCIL SIZED RS-232 LEVEL LOGIC PROBE

Batteryless, 0.5 oz (14 g) in weight, and 5" (12.7 cm) long, PAP can be used to check any lead for high, low, or positive clock indications, as well as ground or broken connections. LEDs are displayed in front, at point of contact. Probe tip fits female RS-232 sockets and ground clip stores in probe's case. Unit may also be used to check TTL levels. Voltage protection to ± 75 Vdc is provided. RS-232 lead identification is printed on unit and operational instructions are included. **Expander Inc**, 400 St Claire Plaza, Upper St Clair, PA 15241.

Circle 222 on Inquiry Card

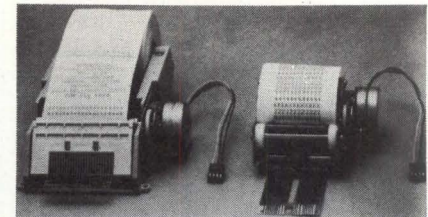
MULTI-OUTPUT SWITCHING POWER SUPPLY



UL-approved 6000 series provides 3 independent outputs of 600, 600, and 350 W, and total output of 1300 W. Construction is of standardized PCB modules. Features include digital remote margin control, remote on/off and sequencing, LED faulty channel indicator, and signals for out of tolerance, input power failure, and current limit. A 6-year guarantee is offered. **Conver Corp**, 10631 Bandley Dr, Cupertino, CA 95014.

Circle 223 on Inquiry Card

ALPHANUMERIC THERMAL LINE PRINTER ASSEMBLIES



EPN9112 and EPN9120 provide 12- and 20-char full alphanumeric capabilities respectively. 5 x 7 dot matrix is achieved by printing lines of 5 dots for each char while a stepping motor advances paper to form 7 dots/col. Thermal mechanism uses beam-lead technology, with connections and blocking diodes built into printhead device. Low peak power requirements suit both units to battery-powered applications. **Texas Instruments, Inc**, PO Box 22 5012, Dallas, TX 75265.

Circle 224 on Inquiry Card

Delta Data Systems

introduces ...

If you think all text processing terminals are the same, you're precisely the person we'd like to talk to. To call the new DELTA 7300 16-bit microcomputer terminal a *different kind of text processing terminal* is an injustice; to call it better than all others is an understatement.

Why don't you be the judge. First compare our features against the competition. Then match them--point by point--to your text processing needs.

With the Delta 7300, text preparation, manipulation and processing has never been easier, more convenient and more cost-effective. And to prove it, we'll let you put us on the spot with a short demonstration--you name the time and the place. Contact us today for full details including technical literature or applications assistance.

These are a few of the outstanding features offered in the new DELTA 7300 text processing terminal:

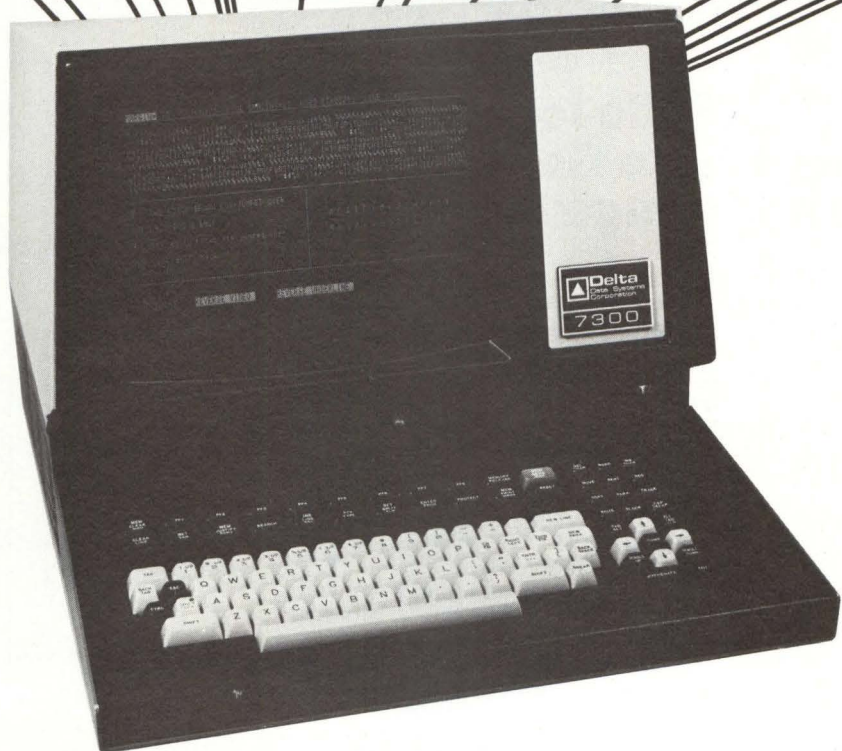
- MULTIPLE SPLIT SCREENS
- UP TO 26,000 CHARACTERS OF DISPLAY MEMORY
- UP TO 892 SPECIAL SYMBOLS AND CHARACTERS
- USER DEFINABLE FUNCTION KEYS
 - POLLED AND NON-POLLED COMMUNICATIONS CAPABILITY
 - AND THESE IMPORTANT TEXT PROCESSING FUNCTIONS:

Automatic Ragged Right Justification, Adjustable Margin, Justify Paragraph, Search (four functions), Define, Move, Copy or Delete.

Word/Sentence/Paragraph, Block, Fractions, Insert/Delete Line, Discretionary Hyphenation

Ideal for distributed processing environments where large amounts of text must be processed.

THE TEXT PROCESSOR



Service in over 150 locations in the U.S., and 14 European countries and Canada



Delta Data Systems Corporation
Woodhaven Industrial Park
Cornwells Heights, PA 19020
(215) 639-9400

U.K. Subsidiary:
DELTA DATA SYSTEMS LTD.
Welwyn Garden (07073) 33833

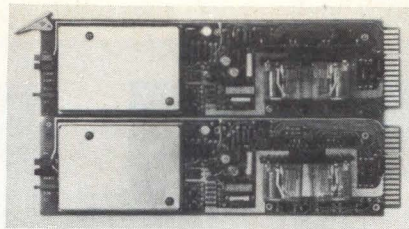
See us at Interface, Booth #207.

CIRCLE 152 ON INQUIRY CARD

PRODUCTS

COMPUTER FRONTEND DUAL CHANNEL MODULE

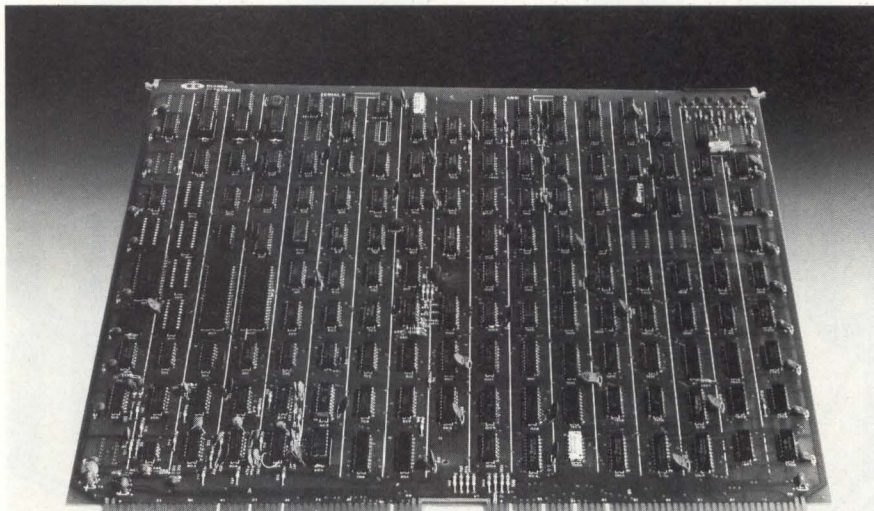
SAM X combines signal conditioning, amplification, and multiplexing in a single module to process digital and analog I/Os. The amplifier/channel computer frontend offers flexibility of selectable filter bandwidth and programmable gain, as well as front edge test points and built-in amplifier and bridge



calibration circuitry. Other features are digitizing, offset correction, averaging, and $\pm 0.1\%$ full-scale accuracy. **AVCO Electronics Div**, 4807 Bradford Dr, Huntsville, AL 35805. Circle 225 on Inquiry Card

PERMANENT MAGNET STEPPING MOTORS

Positional accuracy of $\pm 3\%$ is a key feature of the size 23, 1.8° motor; 11 4-phase models have rated voltages from 1.3 to 28 Vdc, current/phase from 0.30 to 4.70 A, and nom rated torques from 23 to 100 oz-in (0.16 to 0.7 N·m). For 120-Vac operation, 2 60-Hz models provide current ratings of 0.10 and 0.20 A, and torques of 25 and 100 oz-in (0.18 and 0.7 N·m). Max length ranges from 1.5 to 4" (3.8 to 10 cm). Special models can be provided. **Novatronics East, Inc**, PO Box 521, Dover, NH 03820. Circle 226 on Inquiry Card



Made for each other: Your Data General Computer— Our Storage Module Controller.

Our 25XX Controller interfaces Data General computers with Ampex, CalComp, CDC, Hitachi, Okidata, or Microdata storage module disk drives, and you won't find anything like it anywhere else.

For example, it's software transparent—you don't have to change programs to use it. Its format program is built into the firmware. It's microprocessor-controlled. And it automatically selects alternates to bad tracks without operational software intervention.

Optionally, it controls up to four 300-megabyte disk drives.

The Controller consists of a single plug-in circuit board containing four registers:

- Status—16 bits read only
- Memory Address—16 bits read/write
- Command/Cylinder Address—16 bits write only
- Disk Address/Sector Counter—16 bits read/write.

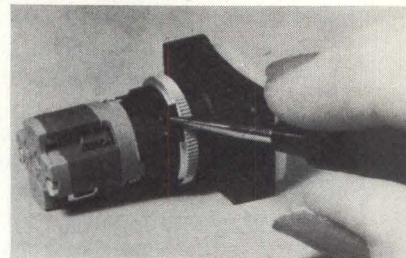
The 25XX Controller, configured to your requirements and complete with necessary cabling and external rack mount level shifter panel (where required) is available for 30-day delivery from:

 **RIANDA**
ELECTRONICS, LTD.

2535 Via Palma Ave. • Anaheim, CA 92801
Telephone: (714) 995-6552

Contact us for all your Data General controller needs.

CONVERTIBLE LIGHTED PUSHBUTTON SWITCHES



Convertible from alternate to momentary mode, lighted pushbutton switches are available as TH01 with tapered bezel, TH31 with straight bezel, and TH42 with covered bezel (extended lens). Round, square, or rectangular translucent or transparent lens models with up to 4-pole switching are T-1 $\frac{3}{4}$ compatible. Wipe-and-roll gold-plated silver self-cleaning contacts handle loads up to 5 A at 250 Vac with min contact bounce. **Unimax Switch Corp**, Ives Rd, Wallingford, CT 06492. Circle 227 on Inquiry Card

OPEN FRAME LINEAR POWER SUPPLIES

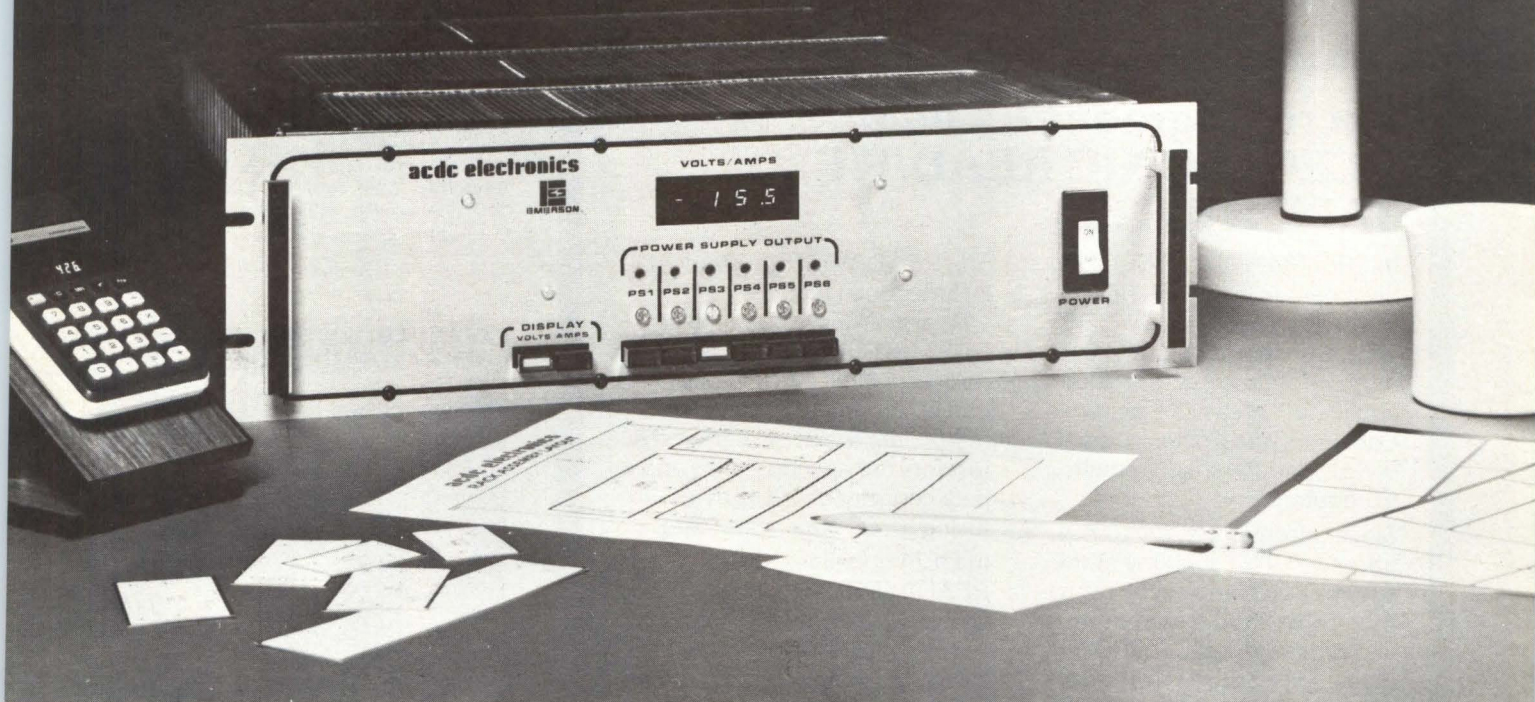
UL 478 recognized Q and QPS single output units are rated for 5 to 28 Vdc, 1.0 to 9.3 A, and max 273 W. QD dual output ratings are ± 12 to ± 15 Vdc at 0.6, 1.7, and 3.0 A. QT and MPS triple output supplies are suitable for most microprocessors and peripherals. Q series units have line regulation of 0.02% and load regulation of 0.05%; others have 0.1% line and load regulation. **Deltron, Inc**, Wissahickon Ave, North Wales, PA 19454.



Circle 228 on Inquiry Card

Power Supply Rack System

Do it Yourself Design Kit



It's simple. At your request, we send you a design kit that allows you to lay out up to six off-the-shelf-power supplies in our new standard 19" rack. The power supplies you select can be linear or switching supplies of various sizes to give you up to six outputs. And, the racks come in three different RETMA sizes, four front panel configurations and a wide range of features and options for maximum flexibility of design. The kit includes stick-on die cut outlines of all our standard power supply case sizes and a simple method for determining the system's cost . . . all in just a few minutes. An easy-to-complete order form is also included for your convenience.

Here's what we do . . . We assemble the power supplies into the rack, completely wired. Using specializ-

ed testing equipment, your entire system is checked for every function. And we provide you with the wiring diagram and an outline drawing for each rack assembly we deliver.

Selectable Rack Features

1. Push-button selector switches
2. Lighted circuit breaker
3. Front panel voltage adjustments
4. Digital volt/amp meter
5. LED output indicator
6. Individually fused modules
7. Perforated rack cover
8. Rugged slides
9. AC input barrier strip or optional line cord.

Send for your free design kit on your company stationery now.

acdc electronics

401 Jones Road, Oceanside, California 92054 Telephone: (714) 757-1880

211 West Clay Avenue, Roselle Park, New Jersey 07204 Telephone: (201) 241-6077

PRODUCTS

PORTABLE ASR OFFLINE EDITING TERMINAL



An automatic send/receive computer terminal reduces connect time with any major timesharing service using a built-in acoustic coupler. Miniterm model 1205 features an expandable 8k RAM for offline editing, and a removable 68k-char mini-cassette memory for unlimited offline storage. Minimizing connect time and related timesharing costs, the terminal also has a microprocessor controlled, 50-char/s printer. The self-contained unit weighs 21 lb (9.5 kg).

Computer Devices, Inc., 25 North Ave., Burlington, MA 01803.

Circle 229 on Inquiry Card

Micro upgrades its *new* ELECTRONIC READ/WRITE TAPE SYSTEM.

MICRO COMMUNICATIONS has been delivering its new ELECTRONIC READ/WRITE Tape Transport System to a number of customers in such application areas as Program Loading, Data Logging, Point of Sale and Personal / Small Computers.

Since introduction, Micro has upgraded the capability of the system to include such features as a 4800 baud transfer rate and *double density* (3200 fci). Mainly based upon the size and weight of the system (less than 6" in length; less than 6 ounces in weight), the system is a natural for microprocessor integration.

The READ/WRITE System includes such features as: TTL and CMOS compatibility, START/STOP TIME of 30/40 milliseconds, a block construction of *die cast aluminum*, a *read/write* speed of 3 ips and a fast forward speed of 6 ips and a data capacity of 120K bytes (using a 50' wafer cartridge).

In OEM quantities, the READ/WRITE System is \$69.00. Delivery is two weeks ARO. Micro supplies mechanical transports at \$25.00 per unit in 1000 unit quantities. Data sheets and system documentation are available upon request.

Call or write today for details.



MICRO

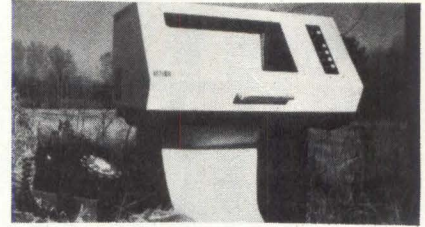
**MICRO
COMMUNICATIONS
CORPORATION**

80 BACON STREET
WALTHAM, MASS. 02154
617/899-8111

A BUCKEYE
INTERNATIONAL
COMPANY



INTELLIGENT REMOTE LINE PRINTER



300-line/min printer achieves full compatibility with XON/XOFF, ACK/NACK, and CTS serial transmission disciplines. COM/300 uses the reliable Printronix printer that supports full 12-channel VFU, 1 to 6 part paper up to 16" (41 cm) wide, and a full 96-char ASCII set. The unit requires only a 4-wire cable and RS-232 connector to hardwire to any computer with asynchronous interface. **Technical Analysis Corp.**, 120 Wieuca Rd, NE, Atlanta, GA 30342. Circle 230 on Inquiry Card

EXPANDABLE WORD LENGTH ROM/RAM SIMULATOR



With the ED-6000, user can develop and test machine code software in microprocessors, bit-slice, and minicomputer systems. Word length is expandable beyond 128 bits. A data monitor displays word lengths of over 40 bits. System permits rapid editing functions, and can interface with a variety of peripherals. Memory address from either multiple or independent addressing sources in 2k x 8-bit increments is std. RS-232 interface for data display and entry, and an internal digital cassette are available. **Electro-Design, Inc.**, 7364 Convoy Ct, San Diego, CA 92111. Circle 231 on Inquiry Card

MILITARIZED DISC DRIVE

Developed as a peripheral for the company's PDP-11/70M, the C3-RM03 is a ruggedized version of DEC's RM03 for field, shelter, and shipboard applications. Containing 67M bytes of usable data, the unit has a 38-ms average access time and 1200k-byte/s data transfer rate. DEC hardware compatible, the drive interfaces with military MASSBUS and contains an adapter for use with commercial MASSBUS. **Norden Systems**, 2 Helen St, Norwalk, CT 06856. Circle 232 on Inquiry Card

When it comes to computers, SAMS PUBLISHES THE BOOKS

Introducing...



THE **BLACKSBURG** CONTINUING EDUCATION SERIES™

It has long been the objective of the "Blacksburg Group" to develop timely and effective educational materials and aids that will permit students, engineers, scientists and others to quickly learn how to apply new technologies to their particular needs. The members of the group have long been involved in digital electronics, minicomputers, and microcomputers.

The Blacksburg Continuing Education Series™ is an easy to read format consisting of 16 titles. Subjects range from basic electronics through microcomputers, operational amplifiers and active filters. Each title in the series includes detailed experiments, "hands-on" learning experiences, and examples to reinforce basic concepts. Book Size 5½" x 8½", softbound.

Howard W. Sams & Co., Inc.
4300 West 62nd Street
P.O. Box 558
Indianapolis, Indiana 46206



Design of Phase-Locked Loop Circuits, with Experiments
by Howard M. Berlin

The first book of its kind to be published, and is an excellent introduction to the theory, design, and implementation of phase-locked loop circuits using TTL and CMOS integrated circuits. Seven chapters cover phase detectors, voltage-controlled oscillators, loop filters, and synthesizers. In addition, useful applications for signal conditioning, instrumentation, and data communication are presented along with device data sheets and over 15 experiments on various aspects of the phase-locked loop. 256 pages.

No. 21545 \$8.95

Design of OP-AMP Circuits with Experiments
by Howard M. Berlin

Covers the selection of op-amps and the fundamentals of operational amplifier circuits useful for solving various instrumentation, signal conditioning problems for analog signals. Topics covered in 10 chapters are linear amplifier circuits, integrators, differentiators, comparators, waveform generators, active filters, single supply circuits, and the instrumentation amplifier. Primarily using the popular 741 op-amp, there are 35 various experiments. 224 pages.

No. 21537 \$7.95

Design of Active Filters, with Experiments
by Howard M. Berlin

This book covers the theory, implementation, and design of filter networks built around operational amplifiers, which are often used in instrumentation and audio applications to remove unwanted signals from the signal of interest. Describes the best design of the various types of low-pass, high-pass, bandpass, and notch filters, with many design graphs and tables as well as worked out illustrative examples. This is the first book of its kind to present the design of active filter networks with a series of 26 experiments to teach you how each filter operates. 240 pages.

No. 21539 \$7.95

PLUS . . . there's 13 more timely computer titles. Order Today! See the complete selection on the order form below.

ORDER FORM

Quantity Ordered

- _____ DBUG: An 8080 Interpretive Debugger No. 21536 \$4.95
- _____ Design of Active Filters, with Experiments No. 21539 \$7.95
- _____ Design of Op-Amp Circuits, with Experiments No. 21537 \$7.95
- _____ Design of Phase-Locked Loop Circuits, with Experiments No. 21545 \$8.95
- _____ Interfacing and Scientific Data Communications Experiments No. 21546 (March 1979 Publication Date) \$5.95 (Tentative)
- _____ Introductory Experiments in Digital Electronics and 8080A Microcomputer Programming and Interfacing
- _____ Book 1 No. 21550 \$12.95
- _____ Book 2 No. 21551 \$10.95
- _____ Two Volumes No. 21552 \$20.95
- _____ Logic and Memory Experiments Using TTL Integrated Circuits
- _____ Book 1 No. 21542 \$9.95
- _____ Book 2 No. 21543 (January 1979 Publication Date) \$9.95
- _____ Two Volumes No. 21544 \$17.95
- _____ Microcomputer—Analog Converter Software and Hardware Interfacing No. 21540 \$9.50
- _____ 8080/8085 Software Design No. 21541 \$9.50
- _____ NCR Basic Electronics Course, with Experiments No. 21549 \$9.50
- _____ NCR Data Communications Concepts No. 21548 \$6.95
- _____ NCR Data Processing Concepts Course No. 21547 \$7.95

Quantity Ordered

- _____ 555 Timer Applications Sourcebook, with Experiments No. 21538 \$5.95
- _____ The 8080A Bugbook® Microcomputer Interfacing and Programming . Bugbook® is a registered trademark of E & L Instruments, Inc., Derby, Connecticut 06418. No. 21447 \$10.50

_____ Sub Total
_____ Add local sales tax where applicable.
_____ Total Amount

Name _____

Address _____

City _____ State _____ Zip _____
(please print)

- Save handling charges by enclosing payment with order.
- Payment Enclosed (No Shipping and Handling Charge)
- Bill Me (Shipping and Handling Charge will be added)
- Send me Free Sams Book Catalog

Prices subject to change without notice. 430

Return To:
Attention: Sales Department
Howard W. Sams & Co., Inc.
4300 West 62nd Street • P.O. Box 558 • Indianapolis, IN 46206

PRODUCTS

HIGHLY STABLE ACOUSTIC COUPLER/MODEM

Operational features of TC3002, a Bell-compatible 103F and 113F unit, include 300-baud asynchronous data rate and switch-selectable originate and answer modes. Acoustic and DAA/private line interfaces, half/full duplex, EIA and 20-mA interfaces, power and carrier interfaces, high accuracy and stability over wide variations in temp, data rate, line



voltage, and received signal amplitudes, and -50 -dBm sensitivity are also offered. **Tek-Com Inc**, 1147 Sonora Ct, Sunnyvale, CA 94086.

Circle 233 on Inquiry Card

ULTRA RELIABLE DYNAMIC RAM BOARDS

Collectively called nKRA, this family of 4 dynamic RAM boards provides 16k, 32k, 48k, and 64k bytes. Memories have synchronous refresh and switch-selectable addressing. Worst case access time is 400 ns, and cycle time, 520 ns. Power required is 8 to 40 Vdc at 1 mA max, 15 to 19 Vdc at 150 mA max, and -15 to -19 Vdc at 50 mA max. Supplies need not be regulated. Provision is made for future addition of bank select option which allows memory expansion beyond 64k bytes with all memory continuously online. **Processor Technology Corp**, 7100 Johnson Dr, Pleasanton, CA 94566.

Circle 234 on Inquiry Card

T-Bar[®]

INTRODUCES

a new 6PDT miniature latching relay with T-Bar[®] reliability

T-BAR's new 205 miniature latching relay for computers, voice/data communications, instrumentation, medical electronics and process control applications . . .

- 6 pole double throw
- printed circuit board mountable*
- unique bistable action
- T-BAR Sit Still[™], Must Operate reliability
- Edge-to-Dome[®] low level dual contacts with orthogonal wiping action
- 2,500,000 operations
- available now
- for further information contact: T-Bar, Incorporated. Switching Components Division. 141 Danbury Road, Wilton, Connecticut 06897. Phone: 203/762-8351. TWX: 710/479-3216.

T-Bar[®]
INCORPORATED

*subject to care in cleaning

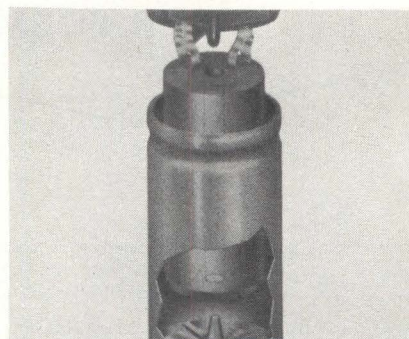
Actual size.

CONTIGUOUS MOUNTING RECTANGULAR LED DISPLAYS

Designed to allow stacking in X or Y direction for contiguous panel displays, CM-64 series discrete LED indicators have typ luminous intensity of 4.0 mcd at 20 mA for red and yellow and 3.0 mcd at 20 mA for green. Forward voltage at 20 mA is 2.0 V typ, 3.0 V max. Storage and op temp ranges from -55 to 100 °C. Forward-facing lighted area measures 0.220 x 0.125" (0.56 x 0.32 cm) and provides 140° field of indication. Rigid rectangular leads allow for wirewrap or solder connection. **Chicago Miniature Lamp Works, General Instrument Corp**, 4433 Ravenswood Ave, Chicago, IL 60640.

Circle 235 on Inquiry Card

LONG LIFE, HIGH TEMPERATURE CAPACITORS



Large computer-grade aluminum electrolytic capacitors, operating over a temp range of -55 to 125 °C, have passed 200-h life tests at 125 °C and max rated voltage, due to Thermal Pack[™] construction. Capacitance ratings of type 125 devices are 1400 to 72,000 μ F, and voltages are from 5 to 40 Vdc. Equivalent series resistance values range from 0.004 to 0.040 Ω at 10 kHz. Ripple current capability is up to 35 A at 85 °C and 10 kHz. **Sangamo Capacitor Div, Sangamo Weston**, Box 128, Pickens, SC 29671.

Circle 236 on Inquiry Card

Your Computer Design Bookstore

(An easy way to order your professional books by mail.)

MICROPROCESSORS AND MICROCOMPUTER SYSTEMS

By G.V. Rao. A completely up-to-date report on the state of the art of microprocessors and microcomputers, written by one of the nation's leading experts. It thoroughly analyzes currently available equipment, including associated Large Scale Integration hardware and firmware. Topics in the book facilitate communication between hardware and software specialists, as well as between marketing and training personnel. An essential reference for engineers, designers and computer specialists. 260 pp., 8½ x 11, \$24.50. **Circle #142 on Reader Inquiry Card.**

A PROGRAMMED REVIEW FOR ELECTRICAL ENGINEERING

By James H. Bentley and Karen M. Hess. For candidates preparing for the Professional Engineering Examination in Electrical Engineering. A step-by-step review of electrical engineering fundamentals that presents the kind of questions you'll be asked. Each problem illustrates a specific concept, and its solution is clearly explained. Included is a wide variety of tables, formulas, charts, graphs, and schematic diagrams. 240 pp., illus., 8½ x 11, \$15.95. **Circle #143 on Reader Inquiry Card.**

SYSTEMS DESIGN AND DOCUMENTATION:

An Introduction to the HIPO Method

By Harry Katzan. Introduces HIPO (Hierarchy, plus Input, Process and Output) as a highly effective method for designing and documenting computers and information systems. HIPO describes systems in terms of their inputs, outputs and constituent processes, and places these functions in a meaningful hierarchy. Emphasizing a system's function rather than its structure, HIPO is one of the most effective aids to planning, analysis and decision making available. 157 pp., illus., 6 x 9, \$13.95. **Circle #144 on the Reader Inquiry Card.**

COMPOSITE/STRUCTURED DESIGN

By Glenford J. Myers. Provides a methodology for producing less expensive programs that are also more reliable, extensive and maintainable. By discussing underlying theory and then using procedural examples, case studies and exercises, the book tells how to design the structure of medium- or large-sized programs. The author covers the relationships of design to programming languages, the "Jackson design method", and other programming methodologies. 174 pp., illus., 6 x 9, \$15.95. **Circle #145 on Reader Inquiry Card.**

Just published!

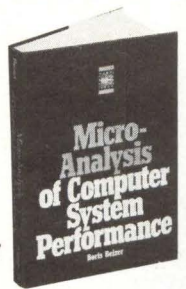
MICRO-ANALYSIS OF COMPUTER SYSTEM PERFORMANCE

By Boris Beizer

Here are proven techniques for analyzing system performance. Analytical methods—as contrasted with simulation—are featured, providing you with an easy-to-follow approach to the construction, validation and use of analytical models. Only expressions that can be programmed with relative ease are included. Mathematical prerequisites are minimal and formal derivations are used only when they serve to explain, illustrate or build intuition. This book will save you countless hours of experimentation and reinvention of analytical methods.

Gives you thoroughly tested procedures.

All the techniques have been proven in practice and can be directly used in the performance analysis of systems based in mini- or microcomputers, analysis of component elements of a large system, and the kinds of analyses done with limited resources such as a calculator or a pocket computer. The assembly language and system programmer will find tools for optimizing the design of individual routines or program modules; the system user and designer will find most of the analytical techniques likely to be required; and the system modeler will find practical methods that quickly get to the heart of a problem. The book includes numerous illustrations and examples that help answer the questions you face daily. 402 pp., illus., 6 x 9, \$22.50. **Circle #141 on Reader Inquiry Card.**



DATA COMMUNICATIONS DICTIONARY

By Charles J. Sippl. An indispensable reference for keeping pace with the rapidly expanding field of data communications. It defines 14,500 terms, concepts, acronyms and abbreviations used in data processing and communications, and is the first dictionary to cover these interrelated areas in one convenient volume. The dictionary clarifies terminology relating to the most important procedures, processes, equipment, capabilities and software. It provides current, concise definitions in new areas such as microcomputers, multi-mini computer systems, and developments in satellite, "packet" and laser communications. 545 pp., 6 x 9, \$19.95. **Circle #147 on Reader Inquiry Card.**

RISS: A Relational Data Base Management System for Minicomputers

By Monte Jay Meldman, Dennis J. McLeod, Robert J. Pellicore, and Morris Squire. Describes a complete minicomputer relational data base management system and its implementation. Reveals how novice users can interact with a computerized data base without needing a programmer—an important cost-saving feature. Also covered are the design approach and structure, user interfaces, and examples of how RISS can be put into practice. 128 pp., illus., 6 x 9, \$14.95. **Circle #148 on Reader Inquiry Card.**

TOP-DOWN STRUCTURED PROGRAMMING TECHNIQUES

By Clement L. McGowan and John R. Kelley. Defines structured programming and sets forth how it is applied. Computer scientists in private industry, the federal government, major universities, and in a growing number of commercial software companies are advocates of the techniques in this handbook. It covers software, the use of the DOWHILE, loop invariants, program correctness and structured programs, structured flow-of-control in FORTRAN, structured flow-of-control in COBOL, and how to structure unstructured codes. 288 pp., illus., 6 x 9, \$16.95. **Circle #149 on Reader Inquiry Card.**

ENCYCLOPEDIA OF COMPUTER SCIENCE

Edited by Anthony Ralston and C.L. Meek. A comprehensive reference containing over 480 articles and 1,000 illustrations, tables and charts. Featuring contributions from over 200 computer science authorities, the volume covers data processing, computer science, information processing, and symbol manipulation. All areas of software, hardware, languages, programs, systems, mathematics, networks, applications, theory, history, and terminology are investigated. 1,523 pp., illus., 7 x 10, \$60.00. **Circle #146 on Reader Inquiry Card.**

15-DAY FREE EXAMINATION

To order free-trial copies of any of these books, simply circle the appropriate number(s) on the Reader Inquiry Card at the back of this magazine. At the end of 15 days if satisfied, send remittance plus postage, handling, and your local sales tax. Otherwise, return the books and owe nothing.

SAVE: If you prefer to enclose payment now, we will pay postage and handling charges. Same return privilege, full money-back guarantee. Your local sales tax must be included with payment.

Offer good in U.S.A. only. Payment must accompany order with P.O. box addresses. Prices subject to change.

C4012

 **VAN NOSTRAND REINHOLD**

We top them all!

Up to 50% Savings on minicomputer mag tape systems? The *guaranteed* total compatibility of Digi-Data systems with most minicomputers means you can bank on it.

Whether you're talking operating software or hardware, our systems and theirs are completely interchangeable. With one major difference: the proven ultra-simple Digi-Data design that saves you money also provides greater reliability and the time/cost economy of simplified maintenance. And, in many cases we offer improved features over the tape drive system supplied by your minicomputer manufacturer.

It's all part of the philosophy of excellence behind our 17-year record of corporate stability. You'll see more proof of it in the fast 30-day ARO delivery and competent service that back up our line of minicomputer mag tape systems.

To free yourself from the big-name, big-price squeeze, call or write for details of our full line of transports, formatters, computer interfaces and buffered tape systems.



**DIGI-DATA
CORPORATION**

8580 Dorsey Run Road, Jessup, MD 20794
(301) 498-0200

® . . . First In Value

CIRCLE 158 ON INQUIRY CARD



PRODUCTS

LSI PRODUCTION TEST SYSTEM



A production oriented system reduces LSI testing costs by offering Sentry™ program and performance board compatibility and general purpose architecture that adapts to changes in device technology. The Sentinel™ mainframe contains an FST-2 24-bit computer with 32k memory, a high speed functional unit, and a precision measurement unit; peripherals include a floppy disc, video keyboard terminal, summary printer, and optional medium speed line printer. Other components are 3 programmable device power supplies, 5 pair of programmable reference voltage supplies, and max of 2 LSI or Sentry-type high speed test heads, available in 30-, 44-, or 60-pin configurations. **Fairchild Camera and Instrument Corp, Test Systems Group, 1725 Technology Dr, San Jose, CA 95110.**

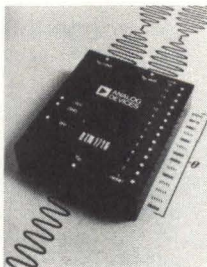
Circle 237 on Inquiry Card

MASS MEMORY VIDEO DIGITIZER

Output of a vidicon or CCD TV camera can be digitized by the model 8258 without in any way compromising the camera's analog recording capabilities. The digitizer is applicable where large amounts of data must be acquired and stored at a high rate. With CCD cameras it can be operated as fast as 20 MHz. It can digitize 512 samples/line of standard video with 256-level resolution. Companion memory modules allow expansion in 128k steps for storing from 1 field or 128k words up to 8 full frames of the digitized standard video signal. Data output is via either a 10-MHz max parallel external port or CAMAC dataway. A synchronization bit is provided for use with analog displays. **LeCroy Research Systems of California, 1806 Embarcadero Rd, Palo Alto, CA 94303.**

Circle 238 on Inquiry Card

DIGITAL TRIGONOMETRIC MULTIPLIERS



Accepting either ac or dc analog reference signals plus a 12- or 14-bit digital representation of an angle (θ), two vector generators provide outputs of both the sine and cosine of θ times the analog input signal. Performing quadrature signal and oscilloscope generation, as well as coordinate rotation, it functions as a trigonometric multiplying DAC. Housed in 3.125 x 2.625 x 0.4" (79 x 67 x 10-mm) packages, DTM1716 has 14-bit digital

input resolution and DTM1717 has 12-bit resolution. Both are available in 0 to 70 °C and -55 to 105 °C operating temp ranges. Specs include full-scale outputs of ± 10 V, accurate to $\pm 0.1\%$ (± 3 arc-min), and full-scale input of ± 10 V. **Analog Devices, Inc, Rte 1 Industrial Pk, Norwood, MA 02062.**

Circle 239 on Inquiry Card

CHASSIS MOUNT REGULATED AC-DC POWER SUPPLIES



CM series is available in 11 models: single output 5 Vdc at 500, 1000, or 2000 mA, and dual output ± 12 or ± 15 Vdc at 60, 100, 200, or 300 mA. They incorporate stable references and high gain, low phase shift broadband regulator circuits. Low thermal masses and gradients permit min delay in reaching equilibrium. Typ specs include line/load regulation, 0.02%; voltage tempco, 0.02%/°C, and no derating from 0 to 70 °C. **Intronics**, 57 Chapel St, Newton, MA 02158.

Circle 240 on Inquiry Card

CHAIN PRINTER CONTROLLER/INTERFACE



S1403/HP 3000 controller contains all interface, control, and power functions necessary to make the HP 3000 plug-compatible with IBM models 1403-2, -3, and -N1 train and chain printers. 1403 printers offer type set and char changeability, plus better printing quality, and 80" (203-cm)/s paper slewing. Controller memory stores the universal char set for each type set to be used, making the controller software-compatible with HP 3000 programs. **Spur Products Corp**, 1904 Centinela Ave, Los Angeles, CA 90025.

Circle 241 on Inquiry Card

HIGH-POWER TRIPLE-OUTPUT POWER SUPPLIES

Line operated series MP provides 6 models with outputs of ± 12 or ± 15 Vdc at 1 or 1.5 A, and 5 Vdc at 3, 6, or 12 A depending on model specified. Input is 115/230 Vac, 50 to 60 Hz, with no derating at 50 Hz. Basic series specs are: output ripple, 1 mV rms max; line/load regulation, 0.05/0.1%; tempco, 0.01%/°C; efficiency, 45%; op temp range, 0 to 71 °C; and transient response, 50 μ s max. **Datel Systems, Inc**, 11 Cabot Blvd, Mansfield, MA 02048.

Circle 242 on Inquiry Card

ULTRA MINIATURE SOLID STATE INDICATOR LIGHTS

High brightness 249 series lights are available from 3.6 to 28 Vdc at a max current of 20 mA, and can be driven directly by TTL levels. An internal fresnel ring pattern used in the lens design assures max distribution of light. Indicators have std black anodized finish which produces high contrast ratio for optimum indication and are available with red, green, or yellow LEDs and red, white, or clear transparent lenses. **Dialight**, a North American Philips Co, 203 Harrison Pl, Brooklyn, NY 11237.

Circle 243 on Inquiry Card

MICROPROCESSOR BASED ASCII INTERFACE

SL111 asynchronously handshakes between computers, microprocessors, teletypewriters, display terminals, and the company's series 100 analog scanners. Data format is serial ASCII; jumper selectable RS-232-C or 20-mA current loop data transmission is provided. Transmission error analysis routine and diagnostic subroutine test write or start command errors, unit's internal circuitry, and external transmission lines. **The San Diego Instrument Laboratory**, 7969 Engineer Rd, San Diego, CA 92111.

Circle 244 on Inquiry Card

ECLIPSE

NOVA

SLOT SAVER II™ Multi-peripheral Controller

Save space, save money with the multi-controller Slot Saver II • Single 15" board replaces 3 or more Data General boards • Console terminal and 2nd serial channel • Real-time clock • 4-channel MUX • Parallel line printer (all brands) • Data General software compatible • One year warranty • 30 day delivery • Service and support

*We've built our reputation on quality and service.
See us for all your Data General controller needs.*

NOVA and ECLIPSE are Registered Trademarks of Data General Corp.

CUSTOM SYSTEMS INC
2415 ANNAPOLIS LANE
MINNEAPOLIS, MINNESOTA 55441
Tel: (612) 553-1112, Telex: 29-0975

Plug into an INSTANT-PERIPHERAL™ for highly reliable cassette program loading and storage.

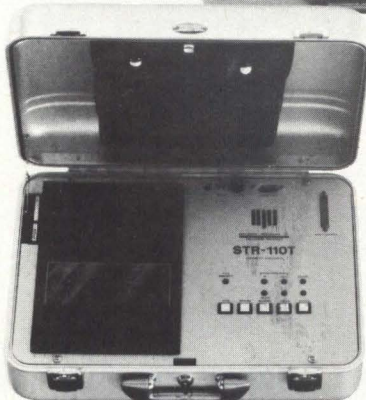
EPI's Speed Tolerant Recording (STR®) technique gives you error rates of less than 1 bit in 100 million. That's reliable! Good enough for recording, storing and loading critical programmable controller instructions or digital system diagnostic routines. Unlike many loaders using low-cost cassettes, these systems offer guaranteed unit-to-unit compatibility. That's backed by experience with more than 4000 units in the field.

Fast, reliable program loading... convenient program and data storage... easy interface to your system. Good reasons to rely on an INSTANT-PERIPHERAL™ for all your low-cost digital recording and programming tasks. Contact Electronic Processors, Inc., 1265 W. Dartmouth Ave., Englewood, Colorado 80110. Phone (303) 761-8540.



8-bit parallel STR-110 allows memory dumps or program loading up to 125 characters per second. \$1328 in single quantity.

Microprocessor controlled STR-LINK II provides manual or remote control of Standard RS-232 functions via handshake lines or with control characters in serial data stream. Buffer option allows 9600 peak BAUD rate. Starts at \$1735 in single quantity.



Custom designs, like this STR-110T for the Texas Instruments 5TI Programmable Control System, can handle special loader needs. We can provide automatic verification in both read and write modes, remote control and more. Just ask us.

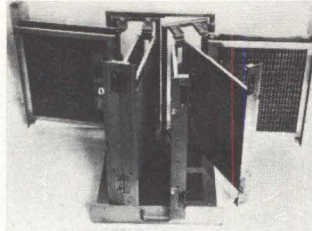
**ELECTRONIC PROCESSORS
INCORPORATED**

The INSTANT-PERIPHERAL™ Company

PRODUCTS

VERTICAL PAGE INTERCONNECTION SYSTEM

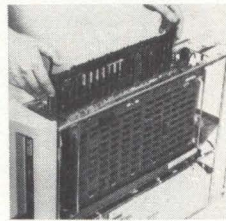
Up to 8 of the company's std IC wirewrap panels accommodating up to 2520 16-pin devices are packaged in the vertical page system that facilitates mounting of the multiple boards in a std 19" (48-cm) cabinet with RETMA spacing.



Boards that form the pages are held together by quick disconnect devices for easy access to the component and wiring sides. Providing for dc power entry of 2 voltages and ground, each pair of pages is held in a slotted frame that facilitates cabling between boards. Overall system measures 26 x 19 x 19.75" (66 x 48 x 50 cm). Assembly's bottom section holds slides, 4 fans, filter, dc power entry, and fuse holder. TTL, ECL, and Schottky boards as well as mirror boards are available for the system. **Augat Inc, Interconnection Products Div**, 33 Perry Ave, Attleboro, MA 02703. Circle 245 on Inquiry Card

Circle 245 on Inquiry Card

MICROPROGRAMMED LARGE DISC SYSTEM CONTROLLERS



Compatible controllers for large disc storage requirements of PDP-11 computers offer identical performance characteristics to DEC controllers. Model SO11/A emulates the DEC RP11/RP02/RP03 subsystems; the /B emulates the RH11/RM02/RP04/RP05/RP06 subsystems; and the /C emulates the RK611/RK06/RK07 sub-

systems. Different operating modules are configured through firmware changes. Compact units have 2 PC boards that can be plugged into any pair of std SPC slots; std Unibus interfacing is via 1 of these boards. Features include automatic self-test, subsystem diagnostics in onboard firmware, std SMD interfacing, fully buffered disc I/O circuitry, and power requirements of 9 A from an internal 5-V source. **Emulex**, 17785 Sky Park Cir, Suite D, Irvine, CA 92714.

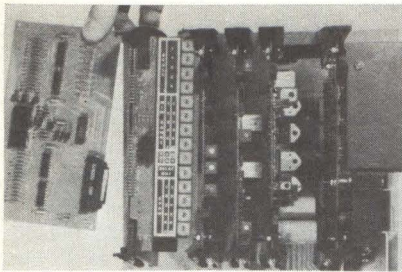
Circle 246 on Inquiry Card

HIGH RESOLUTION COMPUTER GRAPHICS DISPLAY SYSTEM

A gray scale, 1280-pixel/line x 1024-line (1,310,720-point) raster computer graphics display system uses a full CRT screen. Density provides detail clarity, and minimizes distortion and "stair-step" visual effects. System contains programmable graphics processor with 150-ns internal cycle time and set of 55 mnemonic instructions, high resolution CRT including cables, Monitor Control module, 16k MOS/refresh RAM, CPU interfacing, and Graphics Operating System software. Cross assembler software package written in FORTRAN IV is optional. Up to 12 monitors can be operated from 1 system. **Genisco Computers, div of Genisco Technology Corp**, 17805 Park Circle Dr, Irvine, CA 92714.

Circle 247 on Inquiry Card

DIGITAL ULTRASONIC LEVEL MONITOR



Serving operations requiring long range, noncontact level measurement and control, the LM3000 employs ultrasonics. The sensor (monitoring transducer) is mounted above the material to be monitored. Options include a microprocessor meter card for switch selectable calibration; a digital display card with 4 LED readouts; and an averaging card for noise immunity. The monitor operates on 115/220 Vac, 50/60 Hz, $\pm 10\%$. **WESMAR Industrial Systems Div**, 905 Dexter Ave N, Seattle, WA 98109. Circle 248 on Inquiry Card

HIGH RESOLUTION DATA DISPLAY TUBE

370 HCB4, a 15" (38-cm) data display tube, offers 1500-line resolution. Other features include uniform spot size, low cost, electrostatic focusing, 110° deflection angle, electromagnetic deflection, and exclusive direct-etch nonglare face surface. Primarily intended for alphanumeric applications, tube's high resolution makes it suitable for graphic uses. **Panasonic Co, Electronic Components Div**, 1 Panasonic Way, Secaucus, NJ 07094.

Circle 249 on Inquiry Card

TTL OR CMOS DIGITAL COMPARATOR



Low cost ± 1999 digital comparator has built-in thumbwheel switches and relay output. Model 316 compares a $\pm 3\frac{1}{2}$ -, $\pm 4\frac{1}{2}$ -, 5-, or 6-digit parallel bit word with selected settings on thumbwheel switches. Three LEDs on front panel provide visual status indication. Reed relay output is controlled by 3-position switch on the front panel for separate high, equal, or low output signal. **International Microtronics Corp**, 4016 E Tennessee St, Tucson, AZ 85714. Circle 250 on Inquiry Card

LED INDICATORS WITH RED OR GREEN LIGHT OUTPUT

Two LED chips connected in reverse parallel provide either red or green light output depending on polarity of supply voltage in these LED indicator lights. Both outputs have similar brightness by matching chip characteristics. Model 4301 H1/5 is a clear T-1 $\frac{1}{4}$ housing with uninsulated leads. Model 5100 H1/5 is in a black nylon mounting with insulated leads, for snap-fitting into a 0.25" (0.64-cm) dia mounting hole in a 0.031 to 0.062" (0.08 to 0.16-cm) thick panel. **Industrial Devices, Inc**, 7 Hudson Ave, Edgewater, NJ 07020. Circle 251 on Inquiry Card

BISYNC/ASYNC SERIAL CONVERTERS

An EBCDIC binary synchronous host or terminal interfaces to any serial RS-232-C ASCII device or teleprinter with the converter. Two configurations are BAX-1-80, compatible with 2780/3780 devices for batch operation, and BAX-1-75, compatible with IBM 3275. Both employ IBM-type communication terminals and perform all buffering and realtime requirements of protocol. Synchronous speeds are up to 4800 baud, and asynchronous to 9600 baud. **Alpha-matrix, Inc**, 1021 Millcreek Dr, Feasterville, PA 19047. Circle 252 on Inquiry Card

ECLIPSE

NOVA

THE COMMUNICATOR™ 8-Channel Multiplexer

Plug The Communicator into your Data General mini-computer for reliable, versatile communications. • Up to eight channels asynchronous communications on one 15" x 15" board • Jumper-selectable formats and baud rates, 110 to 19,200 • RS-232 or current loop • Modem control with automatic answering • Full Data General software compatibility • One year warranty • 30 day delivery • Service and support.

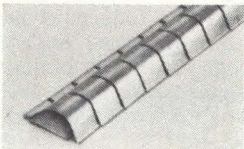
*We've built our reputation on quality and service.
See us for all your Data General controller needs.*

CUSTOM SYSTEMS INC
2415 ANNAPOLIS LANE
MINNEAPOLIS, MINNESOTA 55441
Tel: (612) 553-1112, Telex: 29-0975

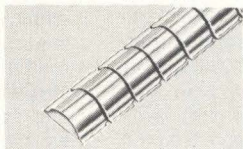
NOVA and ECLIPSE are Registered Trademarks of Data General Corp.

When RFI problems get sticky,
try **stickn fingers**®

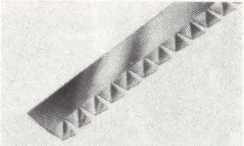
Attaches faster, shields better than anything else!



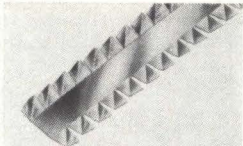
SERIES 97-500 The original Sticky Fingers with superior shielding effectiveness.



SERIES 97-520 A smaller size strip; highly effective in less space.



SERIES 97-555 New Single-Twist Series for use when space is at a premium. Measures a scant 3/8" wide.



SERIES 97-560 New 1/2" wide Double-Twist Series, ideal for panel divider bar cabinets.

Now you can specify the exact type beryllium copper gasket that solves just about every RFI/EMI problem. Perfect for quick, simple installation; ideal for retro-fitting. Self-adhesive eliminates need for special tools or fasteners. Write for free samples and catalog.



INSTRUMENT SPECIALTIES COMPANY, Dept. CD-57
Little Falls, N. J. 07424
Phone — 201-256-3500 • TWX — 710-988-5732

CIRCLE 162 ON INQUIRY CARD



**SINGLE
& DUAL**

McLEAN CENTRIFUGALS

Std. or Mil. Spec. Over 25 models with airflows from 50 to 2000 CFM. Static pressures from 0." to 3.0". Motors and wheels precision balanced — quiet, vibration free. UL approved motors for any AC frequency or power, single or three phase. Custom-built units available.

SEND FOR CATALOG

McLEAN McLEAN

ENGINEERING LABORATORIES

Princeton Junction, NJ 08550

609-799-0100 • TWX 510-685-2543

ENGINEERING MIDWEST

9560 Eighty-Fifth Ave. N.
Maple Grove, MN 55369 • 612-425-4747

CIRCLE 163 ON INQUIRY CARD

PRODUCTS

MILITARIZED COMPUTER

The 1602B computer and its I/O chassis (model 2150) meet the Integrated Logistics Support requirements of the U.S. Army, as well as the environmental requirements of MIL-E-5400 and MIL-E-16400. Conductively cooled 19.56" (49.68-



cm) ATR chassis has single-sided access with captive fasteners and plug-in 47- to 440-Hz ac or optional dc power supply. Features include extensive instruction set, DMA capability, and 16 levels of programmable priority interrupts. Processor

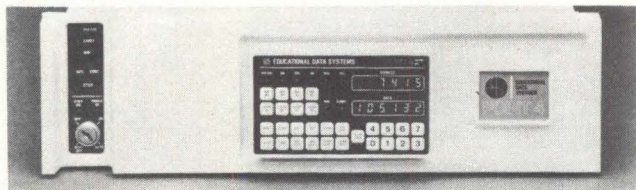
chassis holds up to 64k words of memory, 7 I/O interfaces, and a model 1642 interface to a remote control panel. Std operating temp range is 0 to 65 °C case temp; storage temp range (amb) is -65 to 105 °C. **ROLM Corp**, 4900 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 253 on Inquiry Card

MICROPROGRAMMED DATA TRANSMISSION CONTROLLER MODULES

Controllers for the company's 300 process computer systems improve efficiency and flexibility in distributed automation networks. All transmission procedures are microprogrammed into EPROM, the microprocessors being responsible for executing them in the data transmission controllers. The DUST 3966 for computer to computer communications includes HDLC/SDLC procedures. The 3964 links up the 210 microcomputer system for the lower automation range; synchronous transmission is up to 9600 baud. For basic mode procedures (BSC and MSV), the 3965 also has a connection for automatic dialing in public telephone networks. These controllers are not marketed in the U.S. **Siemens AG**, Postfach 103, D-8000 Munich 1, Federal Republic of Germany. Circle 254 on Inquiry Card

HIGH SPEED, GENERAL PURPOSE MINICOMPUTER



Featuring a 0.4- μ s instruction time, the POINT 4 computer with 16-bit instruction set is compatible with the IRIS operating system and Mighty Mux multiplexer as well as with other software and peripherals designed for Nova-type minicomputers. The CPU and up to 64k, 16-bit words of semiconductor memory are packaged on a single PC board. Also included are a writable control store with 100-ns cycle time and an interprocessor bus capable of speeds up to 2M words/s. A software program loaded from P/ROM allows all normal control panel functions and others to be performed through the master terminal CRT. A handheld control unit is optional. A second program tests all CPU and memory functions as a built-in diagnostic. **Educational Data Systems**, 1682 Langley Ave, Irvine, CA 92714.

Circle 255 on Inquiry Card

MICROPROCESSOR CONTROLLED THERMAL PRINTER



Requiring only power supplies and ASCII input for operation, TP-3150 features patented drive mechanism using single high-torque motor, minimum of moving parts, 18-char buffer, 5 x 5 dot-matrix chars, and solid-state thermal printhead. User may control print direction and char rotation. ASCII data acceptance is in synchronous parallel or asynchronous bit-serial format. Std 64-char ASCII subset is accepted. **Bowmar Instrument Corp**, Commercial Products Div, 8000 Bluffton Rd, Ft Wayne, IN 46809.

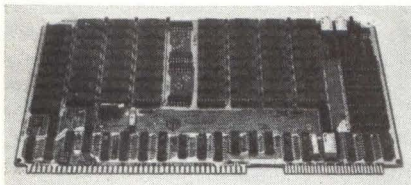
Circle 256 on Inquiry Card

ALPHANUMERIC LED DISPLAY

1.16" (29.46-mm) LED display with 5 x 7 matrix array and X-Y select is side-stackable for "walking" displays. Available in red, yellow, green, and orange, series LRT1057 features single plane, wide angle viewing, with bold 0.083" (2.108 mm) dots, low power, and high brightness. All units have gray face with translucent dot appearance. Series is compatible with ASCII and EBCDIC formats. **Industrial Electronic Engineers, Inc**, 7740 Lemona Ave, Van Nuys, CA 91405.

Circle 257 on Inquiry Card

COMBINATION 32k RAM/8k ROM



An Intel Multibus™ compatible memory provides 32k of static RAM in 2 individually addressable 16k banks, and sockets for 8k of 2716 ROM/EPROM or equivalent memories. As an expansion memory for the company's RM-117 dual-port memory, the CM-118 provides 32k RAM with 200-ns access time. For system memory use, CM-118-SL and CM-118-SL-16K provide 32k and 16k RAM, respectively; each has a 450-ns access time. Access time is programmable from 1 to 16 times the period of the constant clock on the bus. **Datacube SMK, Inc**, 670 Main St, Reading, MA 01867.

Circle 258 on Inquiry Card

USART TEST PACKAGES FOR LSI TEST SYSTEM

Test packages for programmable communications interface devices, including the 8251, 8251A, 9551, 2651, and 8261, consist of device programming unit (DPU), manual device board (MDB) or handler/prober device board (HPDB), and test program and documentation (CADP). Designed to operate on all the company's MX-17 LSI testers, packages can test and verify all operating modes. Features include lot reporting, binning, continuity alarm, dc parametric tests, and dynamic current tests.

Adar Associates, Inc, 154 Middlesex Tpk, Burlington, MA 01803.

Circle 259 on Inquiry Card

SERIAL LINE PRINTER INTERFACE FOR LSI-11

A line printer handler for the RT-11 operating system communicates via any DLV11 interface. All that is necessary are serial data transmit and receive lines. Functions are identical to those of the std RT-11/V3B LP handler. Throughput is limited only by the printer. A personality module plugs into the printer and accepts a 25-pin RS-232 connector from the computer; modules are available for the TI 810 line printer.

Salcris Corp, PO Box 43247, Birmingham, AL 35243.

Circle 260 on Inquiry Card

SCHOTTKY TTL IC PLUGGABLE WIREWRAP PANELS

Series SCH13 panels are of multilayer construction with a center Vcc voltage layer and 2 outside common ground planes, forming a low impedance, high capacity power distribution system. Supplied in groups of 30 16-position patterns/section with pin 16 connected to Vcc center plane and pin 8 connected to the outside ground planes, these devices are available in from 1 to 8 sections with either 26 I/O pins/section or 24 I/O socket-terminals/section. **Garry Manufacturing Co**, 1010 Jersey Ave, New Brunswick, NJ 08902.

Circle 261 on Inquiry Card

HIGH POWER MODULAR D-S CONVERTER

Series H1673 drives 1 size 11 torque receiver and can switch such a receiver through a 180° angle. Damping circuits assure smooth movement of the receiver to avoid jittering and to reduce peak power demands. The converter will operate from ±15- and 5-Vdc regulated power supplies, as well as from 28-Vdc unregulated supplies. It is internally protected to MIL-STD-704C. The units may be built to 883B specs. Frequency is 400 Hz. **Transmagnetics, Inc**, 210 Adams Blvd, Farmingdale, NY 11735.

Circle 262 on Inquiry Card

MFM floppy, 1 head or 2

AED's field-proven 6200 Series floppy disk system has recently been expanded to provide the minicomputer user with a wider choice of disk drive capability. The AED6200 Series now offers double density (MFM) systems in four configurations: 2 drives with single head (5¼" and 7" cabinets), 4 drives with single head (10" cabinet), 2 drives with dual head (7" cabinet) and 4 drives with dual head (two 7" cabinets). All systems come complete with formatter, power supply, drive electronics and CPU interface. Interfaces for LSI-11, PDP-8 and 11; Nova/Eclipse, Varian, Interdata and CAI are all available from AED.

Here is a checklist of the AED6200's outstanding user benefits:

- low cost, fast access storage
- 1.2 megabytes/diskette
- industry standard 8" media
- programmable formatter for ideal record size
- multiple source drives
- 8 computer interfaces available
- expandable to 4 drives
- CRC and IPL for easier loading
- delivery from stock on all popular models

Get all the facts by calling or writing our Marketing Manager today.

Advanced Electronics Design, Inc.

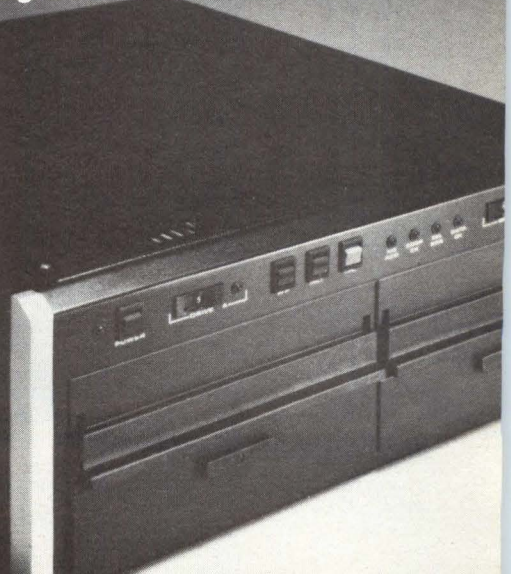
COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400
Fullerton 714-738-6688. Telex 357498.



CIRCLE 164 ON INQUIRY CARD

AED 6200

gives you more for your mini



Mr. Field Service

How do you select a tape to adjust amplitude?



- Use available scratch tape
- Borrow from a customer
- Assign an arbitrary site average
- Some of the above.

Lack of a specified procedure or use of multiple standards invites an ERROR condition.

Our secondary standard amplitude reference tape matches the NBS with a tolerance of 2%.

Select with confidence. Come and see us for your Test Tape needs.

THE ALIGNMENT SPECIALISTS

PERICOMP CORPORATION

14 Huron Drive, Natick, MA 01760 • (617) 237-4052

Manufacturers of SKEW • TRACKING • MASTER OUTPUT TAPES

CIRCLE 165 ON INQUIRY CARD

MINI-STEPS MAXI-STEPPERS

PM and VR steppers—responsive and precise—with slewing rates to 20,000 steps/sec. and higher. We offer an unlimited range of step angles, frame sizes and configurations. And high torque/size ratios. Options include: dampers, heat sinks, encoders, pulse sources, drivers, preset indexers, gearheads, and more. Standards and specials—the best of both.

Send for literature.



Eastern Air Devices Motor Division
Electro Audio Dynamics, Inc.
Dover, N.H. 03820 • (603) 742-3330 • TWX (510) 297-4454

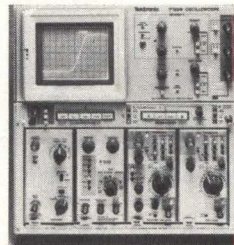
CIRCLE 166 ON INQUIRY CARD

PRODUCTS

REMOTE DATA ACQUISITION AND CONTROL SYSTEM

Ruggedization for severe industrial environments and inclusion of a microprocessor unit with systems oriented architecture suit this high performance sensor based system to realtime process monitoring and computer communications networks. Extended logical/arithmetic and control programming capabilities are expandable to over 256 analog I/O or controller functions. Design includes plug-in cards for the microprocessor unit, memory modules, analog and digital I/O modules, and optional data displays, plus provisions for operator control panel and ac or dc power supplies. Interchangeable RAM and nonvolatile P/ROM can be used during initial data acquisition software development. **Applied Systems Corp.**, 26401 Harper Ave, St Clair Shores, MI 48081. Circle 263 on Inquiry Card

1-GHz BANDWIDTH PLUG-IN OSCILLOSCOPE

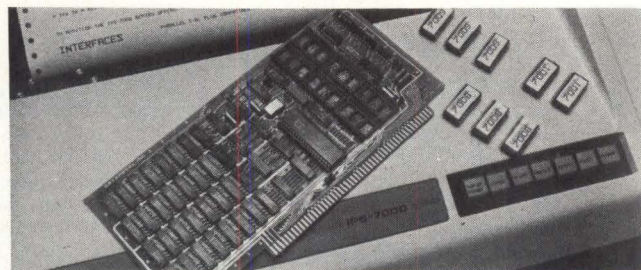


Model 7104 is a general purpose unit with bandwidth of 1 GHz and writing speed of 20 cm/ns. It incorporates a distributed horizontal deflection system, a meshless scan expansion lens, and a microchannel plate electron multiplier. The design uses micro-stripline layout techniques and an interconnect system of metallized elastomer contacts. Horizontal (X-Y) bandwidth is dc to 350 MHz, risetime is ≤ 350 ps, and calibrated sweep speeds are to 200 ps/div. The full size CRT display features a bright, high visibility trace, visible in normal amb lighting. Vertical sensitivity is 10 mV/div to 1 V/div. The model accepts up to 4 of the company's 7000-Series plug-in modules. **Tektronix, Inc.**, PO Box 500, Beaverton, OR 97077.

Circle 264 on Inquiry Card

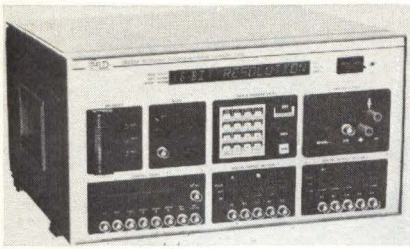
PARALLEL PRINTER FIRMWARE PACKAGES

Firmware packages represent 3 intelligent IPS-7000™ printer configurations, each with parallel interface; they combine a 160-char/s matrix printer and 8-bit microcomputer with RAM and P/ROM. The IPS-7001 prints 64 ASCII char in a 5 x 7 dot matrix; and 7008 and 7009 each print a 96-char set in 9 x 7 matrix. Models 7001 and 7008 each offer a 500-char buffer, while model 7009 features a 3.5k-char circular buffer. Other features of the 7008 and 7009 are programmable vertical format control for 6 or 8 lines/in (2 or 3/cm), audible alarm, and self-test switch. The similar 7001 operates at 6 lines/in (2/cm). **Dataroyal, Inc.**, Main Dunstable Rd, Nashua, NH 03060.



Circle 265 on Inquiry Card

AUTOPROGRAMMABLE 10-CHANNEL TIMER/COUNTER



Z80 controlled timer/counter simultaneously stores 999 program sequences that can be executed from 1 to 9999 times in any sequence. Cycle range is from 2 μ s to 9999 s. Sequences are conditionally alterable during execution. Programming is by response to English-phrased questions. A 16-char, 16-segment alphanumeric display, modified 10-slot S-100 bus, and 0.02% crystal-controlled accuracy are other features of the 8.75 x 17 x 12.75" (22.23 x 43 x 32.39-cm) unit.

Micro Data Collection, PO Box 115, Novato, CA 94947.

Circle 266 on Inquiry Card

HEAVY DUTY EPROM ERASING SYSTEM



C-91 Memorase[®] system erases one batch of up to 96 EPROMs in <7 min. Using more than 7' (2.1 m) of pure quartz tubing light source gives max even output at 254 nm without destructive hot spots. Occupying less than 14 sq in (91 cm²) counter space, unit can be stacked for multiple runs. System features 1-h exposure timer, cumulative 2-h recorder, viewing ports, and interlock device for accident-free operation and ozone-free transmission.

Ultra-Violet Products, Inc., 5100 Walnut Grove Ave, San Gabriel, CA 91778.

Circle 267 on Inquiry Card

DIGITAL PROCESS INDICATORS

Visipak VIP500 series provides direct engineering-unit digital display for process variables such as temperature, pressure, flow, weight, torque, speed, linear position, and frequency. Instruments accept direct transducer inputs from process sensors including thermocouples, resistance-temperature-detectors, strain gauges, potentiometer slide-wires, magnetic pickups and linear variable-differential-transformers.

Action Instruments Co, Inc., 8601 Aero Dr, San Diego, CA 92123.

Circle 268 on Inquiry Card

2-INPUT/MULTIPLE-OUTPUT POWER SUPPLIES

Series NHX miniaturized power supplies provide dual isolated inputs that can be externally switched in event of primary power loss. User selects two input capabilities (115 Vac at 47 to 500 Hz, 12, 28, 48, or 115 Vdc) and eight isolated outputs (3 to 300 Vdc with up to 300-W total output power). Packaged per MIL-STD 810B, supplies are conduction cooled and feature efficiencies to 80% and short circuit protection.

Arnold Magnetics Corp., 11520 W Jefferson Blvd, Culver City, CA 90230.

Circle 269 on Inquiry Card

THIN FILM D-A CONVERTER

The 4000 is a 12-bit, ECL compatible DAC that offers a 40-ns settling time and remains accurate to 1 LSB over a temp range of -55 to 85 °C. Designed with a low glitch of 2.5 mA/ns, it is packaged in a 24-pin, hermetic DIP with 0.1" (0.25-cm) spacing between centers. Incorporating an internal reference supply, the converter uses thin film resistors that are functionally trimmed with lasers. The 1.4 x 0.8" (3.6 x 2.0-cm) unit can be manufactured to MIL-STD-883A.

HyComp, Inc., 146 Main St, Maynard, MA 01754.

Circle 270 on Inquiry Card

MULTIPLE OUTPUT SWITCHING POWER MODULES

Eight models added to the D series line of 100-W modular switchers include four 3-output versions and four 4-output units. In 4-output models, the fourth output is a 3-terminal regulator driven off of an auxiliary output. Total output power is limited to 110 W, distributed as follows: output 1, 75 W or 15 A max; outputs 2 and 3, 36 W or 2 A max; output 4, 15 W or 1 A max. Initial tolerances are \pm 0.2% on primary output, \pm 0.5% on outputs 2 and 3, and \pm 5% on output 4.

Etatech, Inc., 187-M W Orangethorpe, Placentia, CA 92670.

Circle 271 on Inquiry Card

DEC COMPATIBLE FLEXIBLE DISC SYSTEM

Double density 440 system offers software and diagnostic compatibility with DEC RX02. Available with interfaces to LSI-11s, PDP-11s, and PDP-8s, system can record data either in DEC double, or IBM 3740 single density format. 512-word bootstrap program built into LSI-11 and PDP-11 DMA interfaces also performs diagnostics on interface, controller, and CPU memory. Stand-alone diagnostics for controller and drive assembly execute independently of the computer. System is packaged in 5.25" (13.34-cm) chassis.

Data Systems Design, Inc., 3130 Coronado Dr, Santa Clara, CA 95051.

Circle 272 on Inquiry Card

DGC/IBMable floppy disk

AED's low-priced 3100 Series floppy disk drive unit is fully compatible with Nova/Eclipse and μ Nova computers from DGC in addition to IBM3740/3600 diskettes. AED3100 Series drives, which have been field-tested for over four years, use either side of your diskette for double capacity storage providing Read/Write data at less than \$18 per megabyte. Programmable formatter permits ideal record size compatible with OEM's operating system. This economical drive unit can be used as a system device or for auxiliary storage, and will interface with one or two CPU's simultaneously. Available in 4-drive or 2-drive cabinets, the AED3100 is the ideal answer to reliable, low-cost data-storage problems for DGC users who require IBM-compatible diskette media.

Check this list of AED3100 user benefits:

- programmable formatter permits ideal record size compatible with your operating system
- used with RDOS, IRIS, BLIS/COBOL, etc.
- provides random access data at \$18/MB
- DMA interface
- built-in bootstrap loader
- double-sided disk capability
- available completely packaged or in kit form
- includes diagnostics and documentation
- immediate delivery from stock

Advanced Electronics Design, Inc.

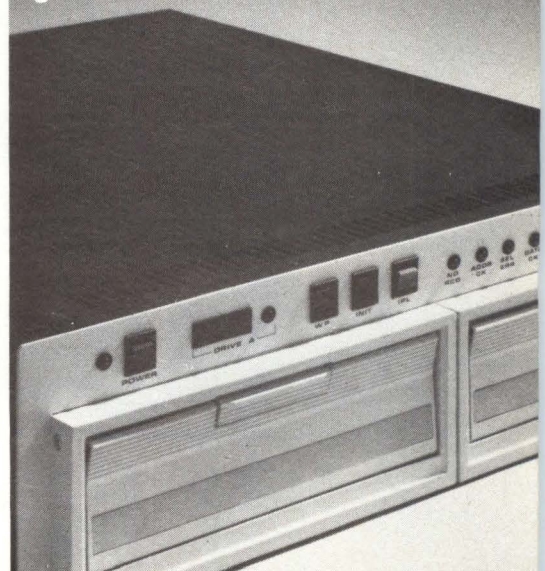
COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400
Fullerton 714-738-6688, Telex 357498.



CIRCLE 167 ON INQUIRY CARD

AED3100

gives you more for your mini



6800 SOFTWARE

FOR: EXORcisor™, SWTP/FLEX™, Smoke Signal, MSI, EPA, Wavemate, Cincinnati Milacron, Conrac 480, Mizar Labs, and more.

BUSINESS BASIC COMPILER (\$210)

- 10 Digits BCD
- Formatted Output
- String Manipulation
- Disk File I/O
- Error Trapping Under Program Control
- Long Variable Names
- If - Then - Else
- Fast Execution
- SDOS Compatible

SDOS - SD'S OPERATING SYSTEM* (\$220)

- Files to 2.15 Billion Bytes
- Dynamic Allocation and Expansion of Files
- Random and Sequential Access
- Supports Floppies and Large Drives Simultaneously
- Long File Names
- Easily Interfaced to New Drives and Peripherals
- Simple Command Interface
- Command Files
- Extensive Error Reporting
- Interrupt-Driven

MAL - 6800 ASSEMBLER (\$140)

- Long Labels
- Conditional Assembly
- Sorted Symbol Table Dump
- Extended Arithmetic Operations
- Motorola Compatible
- Error Cross Reference
- SDOS Compatible

EDIT - CONTEXT EDITOR (\$110)

- Change, Delete, Replace Text with Automatic Display of Change
- Single Keystroke 'Display Next Line'
- Powerful Macro Facilities
- More Useful than Motorola's Editor
- SDOS Compatible

IDB - INTERPRETIVE DEBUGGER (\$ 70)

- Single Step with Register Display
- 4 Realtime Conditional Breakpoints
- Several Display Modes
- MIKBUG Compatible
- Much More Useful than MIKBUG
- Requires 3K ROM, no special hardware

EXORcisor is a trademark of Motorola, Inc. FLEX is a trademark of Technical Systems Consultants.

*Not available for SWTP and Smoke Signal.



SOFTWARE DYNAMICS
2111 W. Crescent, Suite G
Anaheim, CA 92801
(714)635-4760

CIRCLE 168 ON INQUIRY CARD



ROLLS & TAPES
for every
business need

... THE BEST FOR MODERN DATA PROCESSING EQUIPMENT

PAPER TAPE — 7 Colors plus Black Opaque; Printed Top/Arrow; Oiled and Unoiled Rolls: **FOLDED TAPES** — For specialized applications.

THERMAL PAPER — Rolls and Folded. Marginally punched and cross perforated for all types of printers and calculators.

MYLAR TAPE — Paper/Mylar Laminations; Foil/Mylar Laminations; Metalized Mylar.

FOLDED LISTER PAPERS — For Digital Print-out Units.

TELETYPE ROLLS: Single copy; Multi-copy Carbon inter-leaved and Carbonless Friction Feed Sprocket feed.

CONTINUOUS TELETYPE FORMS: 8½" x 11" Carbon inter-leaved 1 through 6 part; Carbonless 1 through 6 part (NCR).

ESCO

EASTERN SPECIALTIES COMPANY, INC.

P. O. Box 350, Holyoke, Ma. 01040, Tel: 413 533-7103

Send for Brochure

Branch Office
Mt. Laurel, N.J. 08054
609 234-1276

Branch Office and Warehouse
Northfield, Ill. 60093
312 446-8780

PRODUCTS

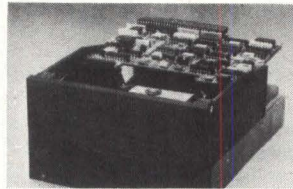
HIGH PRECISION, MICROPROCESSOR CONTROLLED 5½-DIGIT MULTIMETER



Based on a 6802 microprocessor, model 191 is a 200k-count, manual-ranging bench DMM with dc volts and ohms ranges std. It provides readings from 1 to 1200 V on 5 voltage ranges, and 2 and 4 terminal measurements from 1 mΩ to 20 MΩ on 6 resistance ranges. An ac volts option measures 10 μV to 1000 V. The meter is capable of 0.0005% resolution and 1-μV/1-mΩ sensitivity. Error messages show improper range/function combination and overload indication. In the ADC, a microprocessor combines charge balance and single slope conversion techniques. An automatic, nonlinear digital filter, enabled on 200-mV and 200-Ω ranges, suppresses microvolt-level noise. A front panel pushbutton nulls any onscale reading. **Keithley Instruments, Inc.**, 28775 Aurora Rd, Cleveland, OH 44139.
Circle 273 on Inquiry Card

DOUBLE-DENSITY FLOPPY DISC DRIVE

Storage capacities of up to 250k bytes of data on one side and 500k bytes on both sides of a 5.25" (13.34-cm) diskette are obtained from model B51 and B52 drives, respectively. For precise alignment, an automatic diskette positioning and



ejector mechanism pre-positions the diskette over the spindle hub before the clutch centering device is engaged. A band head-positioning device reduces track to track access time to 5 ms. The stepper motor turns a precision pulley, which moves the recording head forward or backward to a track. Double-sided drive head assembly uses a fixed bottom head with a gimbed top head. Drives accommodate FM, MFM, M²FM, or GCR encoding techniques. **Micro Peripherals Inc.**, 21201 Oxnard St, Woodland Hills, CA 91367.

Circle 274 on Inquiry Card

CRT DISPLAY MONITOR ASSEMBLY

NDC-15 CRT monitor provides separate horizontal drive, vertical drive, and video signal inputs, as well as composite video, for simple interface circuitry. Featured are a 35-MHz video bandwidth, uniform focus characteristics across the entire screen, typ horizontal retrace time of <6 μs, vertical retrace time of <300 μs, horizontal frequencies from 15,750 to 20 kHz, and a skip scan with settling time of <20 μs. Electrically and mechanically compatible with Motorola and Ball Brothers monitors, the unit has a min MTBF of 10,000 h. P4 phosphor is std; P31, P39, and P42 phosphors, and a power supply module are optional. Resolution is a min of 1000 TV lines at the center, 750 lines at the corners of the display. **TSD Display Products, Inc.**, 35 Orville Dr, Bohemia, NY 11716.

Circle 275 on Inquiry Card

HIGH RESOLUTION RASTER SCAN GRAPHICS MONITOR

Geared for the OEM market in graphics and image processing applications, high density HRD-15 display module uses 15" (38-cm) CRT to display 1024 x 768 noninterlaced raster. The 105-MHz bandwidth system scans at 64k scan lines/s, with entire image updated at 60 frames/s. Dot resolution is rated at 0.01" (0.25 mm) with clear definition, since rise/fall times are less than 3 ns. Std phosphor is P-104, with others available on request. **CPT Corp**, 1001 Second St S, Hopkins, MN 55343. Circle 276 on Inquiry Card

DIGITAL LED TACHOMETER SYSTEM

A series 727 tachometer which shows monitored r/min in red 17.8-mm LED display digits, 10-ft (3-m) conductor cable, and magnetic pickup and 60-tooth gear for sensor input comprise the series 747 system, which monitors most machine shaft speeds. CMOS/LSI circuitry of the tachometer is immune to electrical noise. Synchronized to maintain power company frequency, the unit features reading updates 60 times/min and measures up to 10k r/min. **Selco Products Co**, 7580 Stage Rd, Buena Park, CA 90621. Circle 277 on Inquiry Card

MULTISPEED SYNCHRONOUS LINE DRIVER

Multispeed, limited distance synchronous line driver transmits data up to 20 mi (32 km). Operation is 4-wire full-duplex, or 2- or 4-wire half-duplex, in point-to-point or multipoint/pollled modes. Modem can transmit at 4800 bits/s for up to 6 mi (9.6 km) and at 9600 bits/s for up to 4 mi (6.4 km) on a 26 AWG nonloaded cable. Available in both fixed and multiple speed versions, with switch selectable data rates from 1200 to 28,800 bits/s, unit meets Bell spec 43401. **Prentice Corp**, 795 San Antonio Rd, Palo Alto, CA 94303. Circle 278 on Inquiry Card

TERMINAL OR CONNECTOR DOUBLE-DUTY WRAP POSTS

Tin-plated T46-5-9 or gold-plated T46-5A-9 posts function as terminals for wrapped-wire interconnections or as pins which mate with ribbon-wire connector. Sharp square-edge 0.025" (0.635-mm) post insures gas-tight wraps. The 0.24" (6.1-mm) top and 0.64" (16.2-mm) bottom lengths allow 2 and 3 wirewraps, respectively. The 0.044" (1.816-mm) diag center section provides solid wedge fit in std 0.042" (1.066-mm) perforated board holes. **Vector Electronic Co, Inc**, 12460 Gladstone Ave, Sylmar, CA 91342. Circle 279 on Inquiry Card

DEC PLUG COMPATIBLE CARD READER

Compatible with DEC PDP-11s, 80-col model CR 300/11 operates at 300 cards/min. Vacuum feed mechanism aids in handling badly worn or damaged cards. Unit is direct replacement for DEC CR 11. Subsystem includes card reader, cable, and interface module that plugs into PDP-11 backplane. **Cardamation Co**, 9A, Frazer Mall, Frazer, PA 19355. Circle 280 on Inquiry Card

BCD TO 7-SEGMENT PANEL DISPLAY



Model 416 readout converts BCD information to a 7-segment LED digital display. Features include display hold and blank, programmable decimal point, and lamp test; choice of 2-, 3-, or 4-digit display; 5-, 15-, or 24-Vdc signals; 1 or 0 true logic input; and power from 5-, 15-, or 24-Vdc or 117-Vac source. The extruded aluminum case fits a 3.625 x 1.75" (9.2 x 4.4-cm) panel cut-out and extends 4.5" (11.4 cm) deep. Black-bordered face with red lens cover measures 4.5 x 2.25" (11.4 x 5.72 cm). **Cincinnati ElectroSystems Inc**, 469 Ward's Corner Rd, Loveland, OH 45140. Circle 281 on Inquiry Card

LOW POWER, FAST START-UP CLOCK OSCILLATORS

Model CM-2000 TTL clock oscillator operates in the 500-kHz to 50-MHz range. The 0.780 x 0.510 x 0.320" (1.981 x 1.295 x 0.813-cm) unit features a true hermetically sealed crystal package with std 4-pin configuration, low power consumption, fast start up, and electronic integrity achieved through multicavity transfer molding. **Crystek Microelectronics**, 2659 Nova Dr, Dallas, TX 75229. Circle 282 on Inquiry Card

MAGNETIC TAPE SUBSYSTEMS

Featuring vacuum column tape drives, the Supermini series operates at 75 or 125 in (191 or 318 cm)/s. Compatible with the DEC PDP-11 and Data General Nova and Eclipse computers, subsystems have operator selectable dual recording densities of 800 or 1600 bits/in (315 or 630/cm). They process data at 200k bytes/s at the higher density and 120k bytes/s at the lower. **California Computer Products, Inc**, 2411 W La Palma Ave, Anaheim, CA 92801. Circle 283 on Inquiry Card

EMULATOR CONTROLLER

The AED8000 emulator/microcontroller provides cost effective data control and intermediate data buffering between your CPUs and Mass Storage disks. A total of 8 disk drives in any combination, including Winchester, can be utilized at one time; and up to 4 CPUs can be interfaced through the AED8000 Microcontroller interface electronics. The AED8000 emulates the OEM disk controller through generational changes, saving you money by not requiring you to write the software driver over and over again. And the controller not only runs the software for the emulated disk, but runs the mainframe manufacturer's disk diagnostics as well!

Here is a checklist of the AED8000's outstanding user benefits:

- RP-03, RP-04 and RP-06*¹ emulation
- microprogrammable 24-bit power
- writeable control store microcode
- controls 8 storage module drives
- handles SMD and Winchester drive mix
- handles any combination of Ampex, Calcomp, CDC, ISS and Memorex drives
- 56-bit Fire Code Error Correction
- 256 x 16-bit data buffer

Get all the facts by calling or writing our Marketing Manager today.

*¹ Registered trademark of Digital Equipment Corp

Advanced Electronics Design, Inc.
COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400
Fullerton 714-738-6688, Telex 357498



CIRCLE 170 ON INQUIRY CARD

AED8000

gives you more for your mini

AED 8000

LITERATURE

Measuring Methods for Telecommunications

Compiling some principles of telecommunication measurement techniques, with sections discussing voltage and level measuring, data transmission, distortion, and PCM measuring technology, 58-p brochure is illustrated with schematics, line drawings, and graphs. Write on company letterhead to **W & G Instruments, Inc.**, 119 Naylor Ave, Livingston, NJ 07039. Circle 300 on Inquiry Card

Array Processors

Three-bus architecture, internal CPU, FORTRAN support, and I/O rates up to 36M bytes/s are features of MAP I/O interfaces discussed in brochure. **CSP Inc.**, Burlington, Mass. Circle 301 on Inquiry Card

Narrow Profile Power Supplies

Bulletin describes 1.68" (4.27-cm) thick single, dual, and adjustable output supplies with photos, dimensional drawings, and specs. **Acopian Corp.**, Easton, Pa. Circle 302 on Inquiry Card

VLSI System Design

Preliminary design manual explains concept of CAD for ECL VLSI, and defines initial library of 85 fully characterized major, interface, and output macrocells. **Motorola Semiconductor Products, Inc.**, Phoenix, Ariz. Circle 303 on Inquiry Card

Dc/dc Power Supplies

Dimensional package drawings, pinouts, and selection spec chart for single, dual, and triple output microprocessor and microcomputer power supplies are featured in 4-p catalog. **Stevens-Arnold, Inc.**, South Boston, Mass. Circle 304 on Inquiry Card

PC Board and Panel Mount I/O Connectors

Catalog lists design features and specs, includes photos of available styles, and supplies full-scale dimensional drawings plus line drawings of available options for seven series of I/O connectors. **Control Products Div., Amerace Corp.**, 2330 Vauxhall Rd, Union, NJ 07083.

Process Control Software

What, why, and how format of brochure emphasizes ease of BASIC language programming and lists process I/O subroutines; both are for use with industrial control and data acquisition microcomputers. **Wyle Laboratories/Computer Products**, Hampton, Va. Circle 305 on Inquiry Card

Solid Tantalum Capacitors

Series of engineering bulletins presents specs, performance and application data, test procedures, optional radiographic inspection, and optional surge current testing for Hyrel[®] ST capacitors. **Sprague Electric Co.**, North Adams, Mass. Circle 306 on Inquiry Card

Computer Directed Measurement and Control

Local parallel, standalone, smart-remote, dumb-remote, and IEEE-488 GPIB operations using RTP standard bus products are described in brochure. **Computer Products, Inc.**, Fort Lauderdale, Fla. Circle 307 on Inquiry Card

Solid-State Disc

Brochure includes paging performance and price/performance graphs comparing CCD storage subsystem to IBM fixed head disc system it emulates. **Storage Technology Corp.**, Louisville, Colo. Circle 308 on Inquiry Card

Programmable Controller System

I/O tracks, portable programmer/monitor, and programmable controller comprise model 2524 automatic industrial unit presented in brochure. **Industrial Timer Corp.**, Parsippany, NJ. Circle 309 on Inquiry Card

Planar Gas Discharge Displays

Photographs augment descriptions of procedures for inspection, handling, and installation of gas discharge displays, in 12-p application note. **Beckman Instruments, Inc.**, Fullerton, Calif. Circle 310 on Inquiry Card

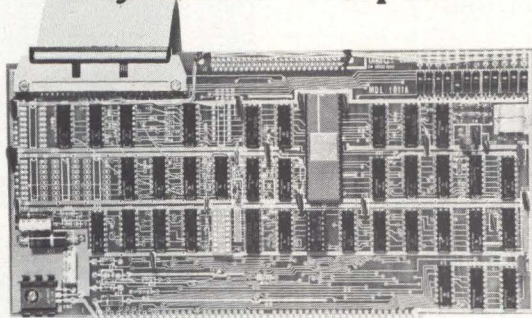
Microprocessor Based Modem

Features, advantages, description, diagnostics, applications, and specs for FCC registered, Bell compatible model 212A are listed in data sheet. **General Data Comm Industries, Inc.**, Danbury, Conn. Circle 311 on Inquiry Card

Power Supplies

Linear feedback, switching, and ferroresonance type voltage and current stabilizers; smart supplies; and switchers are featured in catalog with application hints and design tutorial. **Kepeo Inc.**, Flushing, NY. Circle 312 on Inquiry Card

Tarbell Floppy Disc Interface Designed for Hobbyists and Systems Developers



- Plugs directly into your IMSAI or ALTAIR[®] and handles up to 4 standard single drives in daisy-chain.
 - Operates at standard 250K bits per second on normal disc format capacity of 243K bytes.
 - Works with modified CP/M Operating System and BASIC-E Compiler.
 - Hardware includes 4 extra IC slots, built-in phantom bootstrap and on-board crystal clock. Uses WD 1771 LSI Chip.
 - 6-month warranty and extensive documentation.
 - **PRICE:** Kit \$190 Assembled \$265
- *ALTAIR is a trademark/tradename of Pertec Computer Corp.

Tarbell
Electronics

950 DOVLEN PLACE, SUITE B
CARSON, CA 90746
(213) 538-4251 • (213) 538-2254

Optoisolators

Dimensional outlines; time response; power dissipation; typical application circuits; and input to output, temperature, distortion, and life characteristics are provided in catalog for LED-CdS optoisolators. **Hamamatsu Corp.**, Middlesex, N.J. Circle 313 on Inquiry Card

Military Memory Systems

Designed to meet all military requirements for size, weight, and reliability, computer memory products and systems offering capacities to 32k 18-bit words in a single plug-in package are described in 4-p brochure. **Fabri-Tek**, Minneapolis, Minn. Circle 314 on Inquiry Card

Keyboards and Keyboard Switches

Diagrams, photos, and specs for custom designed, solid-state, gold crosspoint contact, and standard keyboards plus gold crosspoint keyboard switches are featured in 32-p catalog. **Cherry Electrical Products Corp.**, Waukegan, Ill. Circle 315 on Inquiry Card

Data Communications Products

Catalog covers products addressing line costs, transmission errors, and computer port utilization in communication applications. **Micom Systems, Inc.**, Chatsworth, Calif. Circle 316 on Inquiry Card

Planar Cable

Flat cable and connectors, laminated and bonded cables, Twis'N'Flat™ twisted pair cable, and insulation displacement contact connectors are outlined in catalog. **Spectra-Strip**, Garden Grove, Calif. Circle 317 on Inquiry Card

Alphanumeric Printers

Journal, ticket, and sprocket-drive printers that use std 3.875" (9.8-cm) adding machine paper are supplied in brochure along with print samples and ASCII character subset sample. **Syntest**, Marlboro, Mass. Circle 318 on Inquiry Card

Line Printers

Four models with speeds ranging from 600 to 1200 lines/min are covered in brochure containing photos, specs, standard features, and options. **Data Printer Corp.**, Malden, Mass. Circle 319 on Inquiry Card

Data Conversion Design

Data sheets and applications for 8700 series A-D converters and 9400 series V-F and F-V converters are featured in 80-p design manual. **Teledyne Semiconductor**, Mountain View, Calif. Circle 320 on Inquiry Card

Computer Graphics and Imaging

Advantages of various display technologies are presented and compared to those of the System 3400 Video Image Processor in 28-p brochure. **Lexidata Corp.**, Burlington, Mass. Circle 321 on Inquiry Card

Matrix Printers

IPS 7000 family of intelligent printing systems that can change operating characteristics with the replacement of firmware P/ROMs is described in 8-p brochure. **Dataroyal, Inc.**, Nashua, NH. Circle 322 on Inquiry Card

Functional LSI Board Test Systems

L135 systems housed in rigid cabinet kiosks offer building block modularity expanding pin capacity in groups of 6 to a max of 456 static pins. **Teradyne, Inc.**, Boston, Mass. Circle 323 on Inquiry Card

Secure Voice Terminal

Literature describes features of all-digital terminal and lists steps required to prepare the terminal for operation, monitoring, and control. **GTE Sylvania Inc.**, Needham Heights, Mass. Circle 324 on Inquiry Card

NOVA & ROLM users ...here's plug compatible cartridge storage



CARTRIDGE TAPE DRIVE THE MODEL 650 PROVIDES:

- 30 IPS Read/Write, 90 IPS Rewind/Search
- 48,000 Bits/Sec Transfer Rate
- 2.5+ Megabytes per cartridge
- Small Size—Rugged Design

TAPE STORAGE SYSTEMS

- Model 2200—1 or 2 Tape Drives in 5" package
- Model 2400—Up to 8 Tape Drives in 9" package
- Model 2710—Portable Recording System with up to 2 Drives
- Model 86008 Formatter—Used in all Tape Storage Systems. Complete ANSI compatibility with powerful data handling features.

INTERFACES

All tape systems are available with the following controllers: PDP-11/LSI-11/NOVA, ROLM/INTERDATA/ALTAIR/8080/RS232/NTDS.

For more information, call us today.

Qantex

DIVISION
NORTH ATLANTIC INDUSTRIES, INC.

60 PLANT AVE., HAUPPAUGE, NEW YORK 11787 • 516-582-6060 • TWX: 510-227-9660

SEE US AT INTERFACE '79—BOOTH #349.

CIRCLE 58 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the page on which the item appears—not the reader service number. Please do not circle the page number on the reader service card.

	PAGE		PAGE		PAGE
MATERIALS					
SHIELDING					
Shielding Components					
Instrument Specialties	240				
HARDWARE					
CONNECTORS AND INTERCONNECTION SYSTEMS					
PC Connectors					
Viking Industries	187				
Interconnections					
Spectra-Strip	89, 119				
Interconnection Systems					
Augat/Interconnection Products	238				
FANS AND BLOWERS					
Centrifugal Blowers					
McLean Engineering Laboratories	240				
INDICATORS; READOUTS; DIGITAL DISPLAYS; LAMPS					
Displays					
Monsanto Commercial Products/Electronics	220				
Panel Displays					
Cincinnati ElectroSystems	245				
LED Displays					
Chicago Miniature Lamp Works/General Instrument	234				
Industrial Electronic Engineers	241				
LED Indicators					
Industrial Devices	239				
Indicator Lights					
Dialight/North American Philips	237				
Digital Process Indicators					
Action Instruments	243				
PANELS AND BACKPLANES					
Wirewrap Panels					
Garry Manufacturing	241				
PARTS					
Sprockets					
La Vezzi Machine Works	170				
Flat Cable Clamps					
Panduit	253				
WIRE AND CABLE					
Flat Cable					
Spectra-Strip	51				
WIRING PINS AND TERMINALS					
Wrap Posts					
Vector Electronic	245				
COMPONENTS AND ASSEMBLIES					
CAPACITIVE COMPONENTS					
Capacitors					
Sangamo Capacitor/Sangamo Weston	234				
ELECTRON TUBES; CRTs					
Data Display Tubes					
Panasonic/Electronic Components	239				
MOTORS; ROTATIVE COMPONENTS					
Motors					
Howard Industries	116				
TRW/Globe Motors	188				
Stepper Motors					
Eastern Air Devices	242				
Novatronics East	230				
Motor Speed Control ICs					
Cherry Electrical Products	208				
		Tachometer Systems			
		245			
		218			
		224			
		243			
		237			
		230			
		237			
		192			
		231			
		228			
		243			
		213			
		218			
		64			
		234			
		224			
		208			
		218			
		72, 73			
		230			
		226			
		236			
		202			
		40, 41			
		60, 61			
		74, 75			
		50			
		7			
		113			
		28, 29			
		204			
		190			
		208			
		208			
		243			
		208			
		208			
		245			
		206			
		244			
		171			
		90, 91			
		241, 243, 245			
		57			
		11, 243			
		19-21			
		5			
		104			
		199			
		65			
		39			
		207			
		90, 91			
		232			
		16, 17			
		215			
		103			
		19-21			
		238			
		185			
		87			
		230			
		220			
		59			
		1			
		245			
		236			
		232			
		105			
		251			

	PAGE
Cartridge Tape Drives	
Data Electronics	48, 49
3M/Data Products	179
Qamtex/North Atlantic Industries	224, 247
ROM/RAM PROGRAMMERS AND SIMULATORS	
ROM/RAM Simulators	
Electro-Design	232
EPROM Erasing Systems	
Ultra-Violet Products	243
SEMICONDUCTOR MEMORIES	
Semiconductor Memory Systems	
Chrislin Industries	254
Dataram	5
Monolithic Systems	137
Mupro	126
Standard Memories	199
32k RAM/8k ROM Systems	
Datacube SMK	241
Dynamic RAM Boards	
Processor Technology	234
Memory ICs	
Intersil	113
16k RAMs	
NEC Microcomputers	28, 29
Static RAMs	
Advanced Micro Devices	204
Intel	190
P/ROMs	
Fujitsu America	208
Texas Instruments	208

INPUT/OUTPUT AND RELATED EQUIPMENT

COMPUTER PERIPHERALS

Micro Peripherals	
Andromeda Systems	117
Computer Peripherals	
Ball Computer Products	114, 115
Electronic Systems	205

DATA TERMINALS

(See also Graphic Equipment)

Text Processing Display Terminals	
Delta Data Systems	229
CRT Display Terminals	
Beehive International	227
Infoton	191
EECO	193
Perkin-Elmer/Terminals	66, 67
Telera/Research	221
Printer Terminals	
Computer Devices	232
NEC Information Systems	214

DISPLAY EQUIPMENT

(See also Data Terminals and Graphic Equipment)

CRT Display Monitors	
C. Itoh Electronics	250
Motorola Display Products	209
TSD Display Products	244
Single Line Displays	
Digital Electronics	178
Touch-Input Panel Displays	
General Digital	224

GRAPHIC EQUIPMENT

Plasma Display Equipment	
Interstate Electronics	97
Color Graphic Display Systems	
Grinnell Systems	68
Graphic Display Systems	
Genisco Computers/Genisco Technology	238
Graphic Display Subsystems	
Digital Engineering	224
Graphic Display Terminals	
Hewlett-Packard	44, 45
Graphic Display Monitors	
CPT	217, 245
Lexidata	122
Graphics Generators	
Raster Graphics	186
CRT Position Sensors	
Elographics	222
Lightpens	
Symtec	190
Transparent Memory Video Interfaces	
Matrox Electronic Systems	184
INTERFACE EQUIPMENT; CONTROLLERS	
Disc and Tape Controllers	
Dataram	140

	PAGE
Disc Controllers	
Emulex	238
Microcomputer Systems	185
MiniComputer Technology	87
Rianda Electronics	230
Xylogics	220
I/O Subsystems	
Adac Electronics	30
Interface Boards	
Custom Systems	237
MDB Systems	220
Bus Extenders	
National Instruments	226
Line Printer Interfaces	
Interactive Information Systems	224
Salcris	241
Chain Printer Controller/Interfaces	
Spur Products	237
Transparent Memory Video Interfaces	
Matrox Electronic Systems	184

	PAGE
Direct Data Transfer Interfaces	
Digital Laboratories	222
Communications Interfaces	
San Diego Instrument Laboratory	237
IR Communications Interfaces	
American Laser Systems	226
Communications Converters	
Alphamatrix	239
KEYBOARD EQUIPMENT	
Lighted Keyboards	
Stacoswitch	124
Keyboards	
Cortron/Illinois Tool Works	181
Micro Switch/Honeywell	72, 73
George Risk Industries	228
PLOTTING EQUIPMENT	
Digital Plotters	
Hewlett-Packard	123



Give your PDP-11 a Calendar.

When you equip your computer with a TCU-100, you'll automatically have the date and time available when you power up.

It's an easy way to keep track of downtime, too. Furthermore, you can use the unit like an alarm clock. Set it to interrupt at preset times—or at intervals as short as 1/2048 second.

TCUs are shipped preset to your local time, but can be set to any time you want by a simple software routine. The built-in battery back-up is good for months with out computer power.

For the LSI-11 user, we offer the TCU-50 — the same reliable timekeeper without the interrupt capability. With either unit, time is cheap. The TCU-100 is just \$495. And the TCU-50 is only \$325.

Time is only one way we can help you upgrade your PDP-11 or LSI-11 system. We'd also like to tell you about the others.

So contact Digital Pathways if you're into -11's. We are too.



DIGITAL PATHWAYS INC.

4151 Middlefield Road • Palo Alto,
California 94306 • Telephone (415) 493-5544

	PAGE
Houston Instrument/Bausch & Lomb	Cover III
Drum Plotters California Computer Products	203
PRINTER/PLOTTERS	
Electrostatic Printer/Plotters Versatec/Xerox	223
PRINTING EQUIPMENT	
Line Printers	
Okidata	4
Printronix	189
Technical Analysis	232

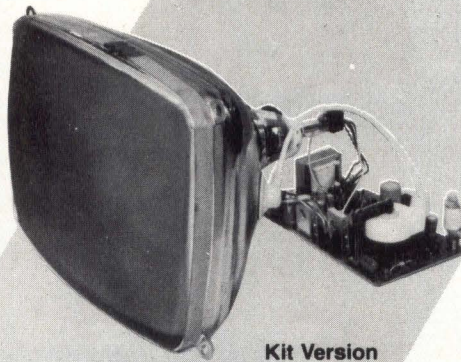
	PAGE
80-Column Printers C. Itoh Electronics	163
Impact Printers Integral Data Systems	47
Band Printers Centronics Data Computer	13
Printers	
Data Printer	228
Dataproducts	194
Dataroyal	242
NEC Information Systems	37
Tally	2
Form Printers Practical Automation	112

Thermal Printers Bowmar Instrument/Commercial Products	241
Texas Instruments	228
Line Printer Interfaces Interactive Information Systems	224
Salcris	241
Chain Printer Controller/Interfaces Spur Products	237
Printer Elements Mohawk Data Sciences/Mark Stamp Steel	211
PUNCH CARD EQUIPMENT	
Card Readers Cardamation	245
PUNCHED TAPE EQUIPMENT	
Punched Tape Readers Decitek/Jamesbury	177
Tape Reader/Punches Sweda International/OEM Products	222
Paper Tape Transmitters Addmaster	252
Tape Punch Code Converters Data Science	222

CIQ Series

9" and 12" CRT DISPLAY MONITORS with a Horizontal Rate of 15.72 KHZ

Compatible with TV120 or TV90
Priced Below the Competition
Built-in Quality, Performance, Dependability



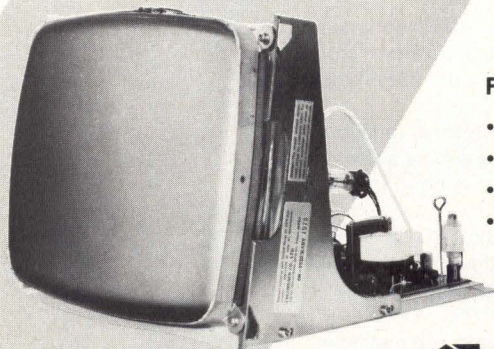
Kit Version

The low-cost CIQ-9 and CIQ-12 CRT Display Monitors with a horizontal rate of 15.72 KHz provide data equipment manufacturers with sharp, highly reliable image presentation.

Separate horizontal drive, vertical drive, and video signal inputs mean elimination of composite sync and video signal processing and simple output circuitry.

The completely new design of the compact integrated PCB utilizes the latest semiconductor and other components, providing a dependable performance level never before possible.

Delivered with P4 phosphor as standard. Available options are P31 and P39 phosphors, sturdy zinc chromate plated chassis and a power supply module which is compatible with practically any power supply standard in the world.



Chassis Version

FEATURES

- Uniform High Resolution
- Integrated PC Board
- Dependable Construction
- Squareness of Picture

C. ITOH ELECTRONICS, INC.
5301 Beethoven Street Los Angeles, Calif. 90066
Telephone: (213) 390-7778 Telex: (WU) 65-2451
280 Park Avenue, New York, NY 10017
Telephone: (212) 682-0420 Telex (WU) 12-5059

COMPUTERS AND COMPUTER SYSTEMS

COMPUTER AUXILIARY UNITS	
Array Processors Floating Point Systems	81
Program Loaders Electronic Processors	238
DESKTOP COMPUTERS	
Portable Computers Instat Systems	190
GRAPHICS PROCESSORS	
Color Graphic Computers Chromatics	24, 25
Color Graphic Processors Three Rivers Computer	226
Graphic Processors Megatek	Cover II
MICROCOMPUTERS AND MICROPROCESSORS	
Color Graphic Computers Chromatics	24, 25
Microcomputers	
Control Systems/Microsystems	182
Intel	76, 77
Intelligent Systems	100
Monolithic Systems	210
North Star Computers	31
Ruggedized Microcomputers Electronic Memories & Magnetics/ Severe Environment Systems	15
Data Acquisition and Control Microcomputers Heurikon	192
Control Microcomputers Detection Sciences/Digital Systems	214
Micro Multiprocessor Systems Victoria Micro Digital	184
Microcomputer Systems TecMar	182
Program Control Unit Chips Advanced Micro Devices	40, 41
Microprocessor Family	
Intel	74, 75
Zilog	60, 61
In-Circuit Emulators Intel	78, 79
Microprocessor Development Systems Tektronix	120, 121
Development Systems Intelligent Systems	100
Microsystem Analyzers Millennium Systems	188
Microcomputer Software Panatec	226
MINICOMPUTER; SMALL- AND MEDIUM-SCALE COMPUTERS	
Computers	
Hewlett-Packard	106, 107
Militarized Computers Roim	125, 240
Minicomputer Systems Perkin-Elmer/Computer Systems	8, 9

	PAGE
Minicomputers	
Educational Data Systems	240
Modular Computer Systems	195
Sperry-Univac	98, 99
Systems Engineering Laboratories	62
MULTIPROCESSORS	
Micro Multiprocessor Systems	
Victoria Micro Digital	184
DATA COMMUNICATIONS EQUIPMENT	
COMMUNICATIONS COUPLERS	
Acoustic Coupler/Modems	
Tek-Com	234
COMMUNICATIONS INTERFACES	
Communications Interfaces	
San Diego Instrument Laboratory	237
IR Communications Interfaces	
American Laser Systems	226
Direct Data Transfer Interfaces	
Digital Laboratories	222
Communications Converters	
Alphamatrix	239
Communication Switches	
Dynatech Data Systems	226
COMMUNICATIONS MULTIPLEXERS	
Multiplexers	
Custom Systems	239
Synchronous Multiplexers	
Micom Systems	218
COMMUNICATIONS SYSTEMS	
Data Concentrators	
Telcon Industries	71
Data Transmission Controllers	
Siemens	240
DATA TRANSMISSION EQUIPMENT	
Fiber Optic Data Link Kits	
AMP	33-36
Synchronous Line Drivers	
Prentice	245
MODEMS; DATA SETS	
Acoustic Coupler/Modems	
Tek-Com	234

DATA ACQUISITION AND CONTROL EQUIPMENT

A-D AND D-A CONVERTERS	
D-A Converter ICs	
HyComp	243
DATA ACQUISITION SYSTEMS	
Data Acquisition Systems	
FI Electronics	214
Remote Data Acquisition and Control Systems	
Applied Systems	242
Hybrid Data Acquisition Modules	
Burr-Brown	204
Data Acquisition and Control Microcomputers	
Heurikon	192
DATA TRANSFER AND INTERFACE EQUIPMENT	
I/O Processors	
AVCO Electronics	230
I/O Subsystems	
Adac Electronics	30
I/O Modules	
Opto 22	54
Bus Extenders	
National Instruments	226
MONITORING AND CONTROL EQUIPMENT	
Control Microcomputers	
Detection Sciences/Digital Systems	214
Digital Ultrasonic Level Monitors	
WESMAR Industrial Systems	239
S-D AND D-S CONVERTERS	
D-S Converter Modules	
Transmagnetics	241

TEST AND MEASUREMENT EQUIPMENT; INSTRUMENTATION

COMPARATORS	
Digital Comparators	
International Microtronics	239

	PAGE
COUNTERS; TIMERS	
Timer/Calendar Boards	
Digital Pathways	249
Timer/Counters	
Micro Data Collection	243
DIGITAL EQUIPMENT TESTERS	
Logic Analyzers	
Gould/Biomation	83
Tektronix	46
Logic Probes	
Expandor	228
LSI Test Systems	
Fairchild Camera and Instrument/ Test Systems	236
LSI/USART Test Packages	
Adar Associates	241
Memory Test Systems	
TestMaster	220
Memory Exercisers	
Wilson Laboratories	111
Microsystem Analyzers	
Millenium Systems	188
METERS	
Digital Multimeters	
Keithley Instruments	244
Tachometer Systems	
Selco Products	245
OSCILLOSCOPES	
Oscilloscopes	
Tektronix	242
VIDEO DIGITIZERS	
Computer Interfaced Cameras	
Hamamatsu	225
Mass Memory Video Digitizers	
LeCroy Research Systems	236
OTHER PRODUCTS; SERVICES	
EDP ACCESSORIES AND SUPPLIES	
Rolls and Tapes	
Eastern Specialties	244

	PAGE
Alignment Tapes	
Pericomp	242
EDUCATION	
Seminars	
Integrated Computer Systems	174, 175
EMPLOYMENT OPPORTUNITIES	
Employment Opportunities	
Northrop/Defense Systems	164
Triad Systems	218
EQUIPMENT BUYING, SELLING, AND LEASING	
Electronic Equipment Rentals	
Rental Electronics	92
Electronics Distributors	
Wyle Distribution	85, 86
Terminals Distributors	
TransNet	253
EXHIBITIONS	
Conference/Exhibitions	
National Computer Conference	216
ELECTRO 79	173
MARKET REPORTS	
Market Reports	
Frost & Sullivan	252
PUBLICATIONS	
Books	
Blacksburg Continuing Education Series	233
Van Nostrand Reinhold	235
SERVICES	
Transportation	
Delta Air Lines	26
SOFTWARE	
Software	
Software Dynamics	244
Microcomputer Software	
Panatec	226
Signal Processing Software	
Signal Technology	219

Micro computer size

Macro data capacity

Raymond's Model 6409 Mini-Raycorder packs 128K bytes of storage and the performance of much larger systems into micro-sized hardware. Yet, it has all the reliability which you have come to expect from Raymond, The Small Tape Drive Experts.

For complete information, contact:

Raycorder Products Division
Raymond Engineering Inc.
 217 Smith Street, Middletown, Connecticut 06457 (203) 632-1000
a subsidiary of Raymond Industries

RS232C



Paper Tape Transmitter

- 50-9600 baud Computer compatible
- RS 232 / Current loop or parallel outputs available
- 5-8 level tape, 7-11 frames per character
- Stops and starts on character at all speeds
- Uses manual control or x-on, x-off
- 90-260 volt, 50-60 Hz power
- Even or odd parity
- Desk top or rack mount

Addmaster Corporation
 416 Junipero Serra Drive San Gabriel, California 91776
 Telephone: (213) 285-1121

CIRCLE 174 ON INQUIRY CARD

STEPPING MOTION CONTROL PRODUCTS MARKET

Frost & Sullivan has completed a 264-page report on the Stepping Motion Control Products Market. Sales forecasts are supplied for 19 products and components in these categories: stepping components, support components, dc hybrid components, incromotion systems; by these major applications: discrete manufacturing (3 types), business machines (3 types), industrial logistics (2 types), energy resources (2 types). A separate forecast is made for the export market, and also for the activation market for incremental motion control products by sectors that are sensitive to OEM demand. Company profiles are provided on major suppliers, evaluating their capabilities and product and marketing strategies. User and supplier responses to F&S surveys provided market intelligence on products being purchased with forecasts into the future. Product comparisons are made and a number of product descriptions and end use applications are provided to emphasize conclusions. The future impact of micro-processors and of intelligent modules that combine micro-computed stepping commands with high volume solid state memories are considered.

Price \$800. Send your check or we will bill you. For free descriptive literature plus a detailed Table of Contents contact:

 **FROST & SULLIVAN, INC.**
 106 Fulton Street
 New York, New York 10038
 (212) 233-1080

ADVERTISERS' INDEX

acdc electronics	231
Adac Electronics Corp.	30
Addmaster Corp.	252
Advanced Electronics Design	241, 243, 245
Advanced Micro Devices	40, 41
American Microsystems, Inc.	94, 95
AMP, Inc.	33-36
Ampex Memory Products Div.	65
Andromeda Systems	117
Ann Arbor Terminals, Inc.	222
Applied Dynamics	254
Ball Computer Products Div.	114, 115
BASF Computer Systems	172
Beehive International	227
Blacksburg Continuing Education Series	233
California Computer Products	203
Centronics Data Computer Corp.	13
Charles River Data Systems	57
Chrislin Industries	254
Chromatics, Inc.	24, 25
Cipher Data Products, Inc.	59
Comark, Inc.	118
Control Data Corp., Peripheral Products Group	39
CPT Corp.	217
Custom Systems	237, 239
Data Electronics	48, 49
Data General Corp.	138, 139
Data Printer Corp.	228
Dataproducts	194
Dataram Corp.	5, 140
Data Systems Design, Inc.	11
Datum, Inc.	23
Decitek, a div. of Jamesbury Corp.	177
Delta Air Lines, Inc.	26
Delta Data Systems Corp.	229
Digi-Data Corp.	236
Digital Electronics Corp.	178
Digital Engineering, Inc.	224
Digital Pathways, Inc.	249
Distributed Logic Corp.	69
Eagle-Picher Industries, Inc.	64
Eastern Air Devices, Inc.	242
Eastern Specialties Co., Inc.	244
EECO	193, 224
Electro '79	173
Electronic Memories & Magnetics Corp., Severe Environment Systems Co.	15
Electronic Processors, Inc.	238
Electronic Systems	205
Ex-Cell-O Corp., Remex Div.	19-21
Floating Point Systems, Inc.	81
Frost & Sullivan	252
Fujitsu America, Inc.	207
Gould, Inc., Biomation Div.	83
Electronic Power Supply Div.	213
Grinnell Systems, Inc.	68
Hamamatsu Corp.	225
Hewlett-Packard Co.	44, 45, 106, 107, 123
Houston Instrument, Div. of Bausch & Lomb	Cover III
Howard Industries	116
Illinois Tool Works, Inc., Cortron Div.	181
Infoton Data Display Terminals	191
Instrument Specialties Co., Inc.	240
Integral Data Systems	47
Integrated Computer Systems, Inc.	174, 175
Intel Corp.	74-79
Intelligent Systems Corp.	100
Intersil, Inc.	113
Interstate Electronics	97
C. Itoh Electronics, Inc.	163, 250
ITT Schadow, Inc.	218
Kennedy Co.	1
La Vezzi Machine Works, Inc.	170
Lexidata Corp.	122
LSI Computer Systems, Inc.	50
3M Co.	179
MDB Systems, Inc.	220

Megatek Corp.	Cover II
Memorex	183
MFE Corp.	105
Micro Communications Corp.	232
Microcomputer Systems Corp.	185
Micro Peripherals, Inc.	150
Micro Switch,	
a div. of Honeywell	72
Minicomputer Technology	87
Modular Computer Systems, Inc.	195
Mohawk Data Sciences Corp.	211
Monolithic Systems Corp.	137
Motorola, Inc.,	
Display Systems Div.	209
Semiconductor Products Div.	169
muPro	126
McLean Engineering Laboratories	240
National Computer Conference	216
NEC Information Systems, Inc.	37
NEC Microcomputers, Inc.	28, 29
Northrop Corp.	164
North Star Computers	31
Okidata Corp.	4
Opto 22	54
Panatec, Inc.	226
Panduit Corp.	253
Pericom Corp.	242
Perkin-Elmer Corp.,	
Computer Systems Div.	8, 9
Terminals Div.	66, 67
PerSci, Inc.	171
Polaroid Corp.	27
Power-One, Inc.	192
Practical Automation, Inc.	112
Printronix, Inc.	189
Pushpa International	104
Qantex,	
Div. of North Atlantic Industries	247
Ramtek Corp.	Cover IV
Raymond Engineering Corp.	251
Rental Electronics, Inc.	92
Research, Inc.,	
Telera Div.	221
Rhinetek	180
Rianda Electronics, Ltd.	230
Rockwell International	159
Rolm Corp.	125
Scientific Micro Systems	52, 53
SD Systems	43
Shugart Assoc.	90, 91
Signal Technology	219
The Singer Co.,	
Librascope Div.	103
Software Dynamics	244
Spectra-Strip, Inc.	6, 32, 51, 89, 119, 204
Sperry-Univac Mini-Computer Operations	98, 99
Stacoswitch	124
Standard Memories	199
Standard Microsystems Corp.	70
Stanford Applied Engineering	165
Storage Technology	16, 17
Sweda International, Inc.,	
Div. of Litton Industries	222
Synertek	201
Systems Engineering Labs	62
Tally Corp.	2
Tarbell Electronics	246
T-Bar, Inc.	234
Tektronix, Inc.	46, 120, 121
Telcon Industries, Inc.	71
Telera Div.,	
Research, Inc.	221
TransNet Corp.	253
Triad Systems Corp.	218
TRW/Globe Motors	188
Van Nostrand Reinhold Co.,	
a div. of Litton Industries, Inc.	235
Versatec,	
a Xerox Co.	223
Viking Connectors	187
Wilson Laboratories, Inc.	111
Wyle Distribution Group	85, 86
Xylogics, Inc.	215
Zilog, Inc.	60, 61

TERMINALS FROM TRANSNET

PURCHASE 12-24 MONTH FULL OWNERSHIP PLAN 36 MONTH LEASE PLAN

DESCRIPTION	PURCHASE PRICE	PER MONTH		
		12 MOS.	24 MOS.	36 MOS.
LA36 DECwriter II	\$1,595	\$ 152	\$ 83	\$ 56
LA34 DECwriter IV	1,295	124	67	45
LA120 DECwriter III, KSR	2,295	219	120	80
LS120 DECwriter III, RO	1,995	190	104	70
LA180 DECprinter I, RO	1,995	190	104	70
VT100 CRT DECscope	1,695	162	88	59
TI745 Portable Terminal	1,875	179	98	66
TI765 Bubble Memory Term.	2,795	267	145	98
TI810 RO Printer	1,895	181	99	66
TI820 KSR Printer	2,395	229	125	84
ADM3A CRT Term.	875	84	46	31
QUME Letter Quality KSR	3,195	306	166	112
QUME Letter Quality RO	2,795	268	145	98
HAZELTINE 1410 CRT	895	86	47	32
HAZELTINE 1500 CRT	1,195	115	62	42
HAZELTINE 1520 CRT	1,595	152	83	56
DataProducts 2230	7,900	755	410	277
DATAMATE Mini Floppy	1,750	167	91	61

FULL OWNERSHIP AFTER 12 OR 24 MONTHS
10% PURCHASE OPTION AFTER 36 MONTHS

ACCESSORIES AND PERIPHERAL EQUIPMENT

ACOUSTIC COUPLERS • MODEMS • THERMAL PAPER RIBBONS • INTERFACE MODULES • FLOPPY DISK UNITS

PROMPT DELIVERY • EFFICIENT SERVICE



TRANSNET CORPORATION
2005 ROUTE 22, UNION, N.J. 07083
201-688-7800

CIRCLE 175 ON INQUIRY CARD

NEW Flat Cable Clamp



Adhesive Backed Releasable • One-piece

- Secures flat cable widths up to 2" and stack heights up to 1 1/64".
- Provides uniform pressure throughout entire stack height range.
- Releasable and reusable for easy revisions.
- One-piece design speeds installation and reduces total installed cost.
- Adhesive backed (with peel-off paper cover) or without adhesive for screw mounting or bundling applications.
- Black, flame retardant polypropylene.

Sold through Panduit Distributors

FREE
SAMPLES



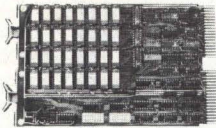
Tinley Park, Ill. 60477 • Phone: (312) 532-1800 • In Canada: Panduit (Canada) Limited

Visit Panduit at Electro '79,
Booth 2718-2720.

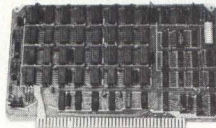
CIRCLE 176 ON INQUIRY CARD

64KB MICROPROCESSOR MEMORIES

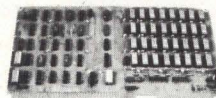
- S-100 - \$695.00
- LSI 11 - \$750.00
- SBC 80/10 - \$750.00
- 6800 - \$750.00



CI-1103 32K x 16



CI-6800 64K x 8



CI-8080 64K x 8

CI-S100 — 64K x 8 on a single board. Plugs directly into the IMSAI, MITS, TDL, SOL and most other S-100 Bus computers. No wait states even with Z80 at 4Mhz. Addressable in 4K increments. Power 6 watts. Price \$695.00

CI-1103 — 8K words to 32K words in a single option slot. Plugs directly into LSI 11, LSI 11/2, H11 & PDP 1103. Addressable in 2K increments up to 128K. 8K x 16 \$390.00. 32K x 16 \$750.00 qty. one.

CI-6800 — 16KB to 64KB on a single board. Plugs directly into Motorola's EXORcisor and compatible with the evaluation modules. Addressable in 4K increments up to 64K. 16KB \$390.00. 64KB \$750.00.

CI-8080 — 16KB to 64KB on single board. Plugs directly into Intel's MDS 800 and SBC 80/10. Addressable in 4K increments up to 64K. 16KB \$390.00. 64KB \$750.00.

Tested and burned-in. Full year warranty.



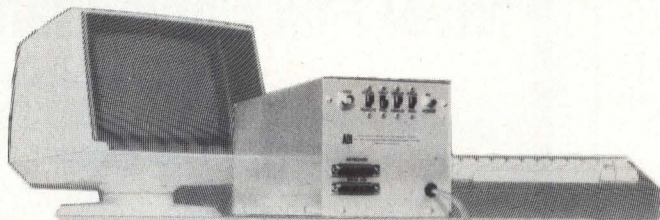
Chrislin Industries, Inc.

Computer Products Division

31352 Via Colinas • Westlake Village, CA 91361 • 213-991-2254

CIRCLE 177 ON INQUIRY CARD

No matter what your needs —



**the Basic Universal Terminal
will solve your problems!**

Whatever your needs — a simple terminal or a unique configuration — ADI's new Series 60 Basic Universal Terminal, the first easily affordable CRT terminal ever to address the total spectrum of user protocol requirements, will solve your problems, with the greatest reliability yet offered in a terminal.

The Series 60 B.U.T. is completely flexible to meet your needs, and there's never any NRE, in any quantity. The Series 60's unique dual microprocessor and modular PROM software will make your "B.U.T." as dumb or as intelligent as you will ever want it to be — in any code you can think of — and as often as you need to change your mind. It's so flexible it just can't become obsolete.

We have the solutions, it's your problems we need. You can't afford not to know more about the Series 60 B.U.T. It's in production now — the price is right — and Fred Hambrecht is waiting to tell you all about it.



APPLIED DYNAMICS INTERNATIONAL

3800 STONE SCHOOL ROAD/ANN ARBOR, MICHIGAN 48104/PHONE 313-971-7840

SALES OFFICES

NEW ENGLAND AND UPSTATE NEW YORK

CALDWELL ENTERPRISES, INC.

Lindsay H. Caldwell
129 Cedar Hill Rd.
East Dennis, MA 02641
(617) 385-2533

LONG ISLAND AND MIDDLE ATLANTIC STATES

CALDWELL ENTERPRISES, INC.

Richard V. Busch
Princeton, N.J. area
(609) 924-6300

SOUTHEASTERN STATES

COLLINSON & CO., INC.
Newton B. Collinson, III
Anthony C. Marmon
4419 Cowan Rd., Suite 302
Tucker, GA 30084
(404) 939-8391

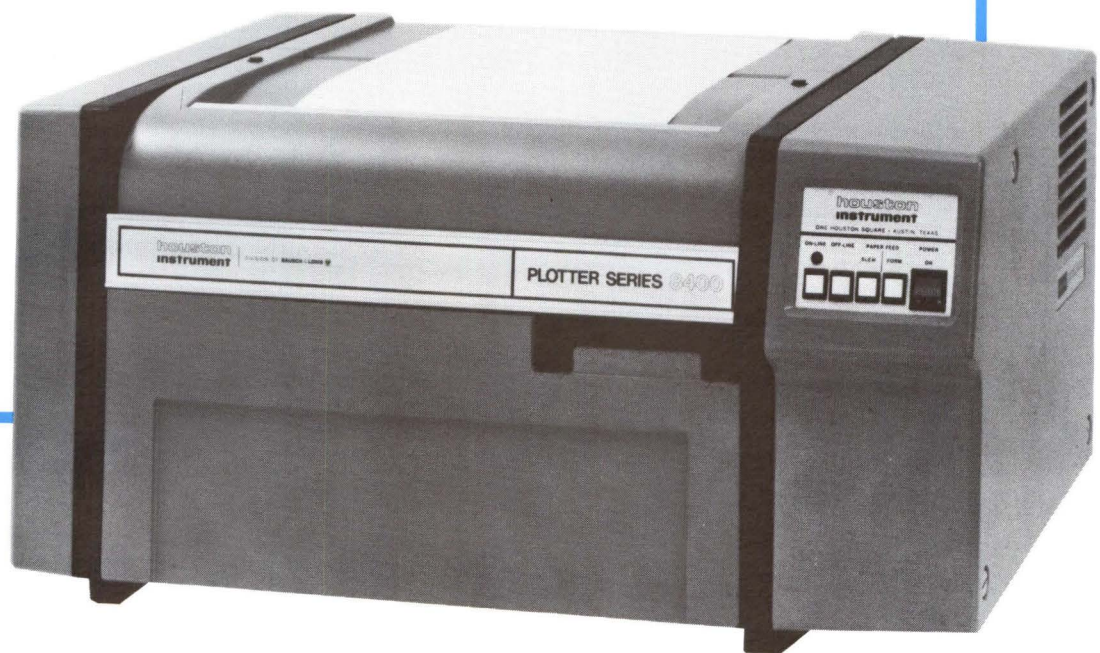
MIDWESTERN STATES

Berry Conner, Jr.
88 West Schiller St.
Suite 2208
Chicago, IL 60610
(312) 266-0008

WESTERN STATES

BUCKLEY/BORIS
ASSOC., INC.
Terry Buckley
Tom Boris
John Sabo
912 South Barrington Ave.
Suite 202
Los Angeles, CA 90049
(213) 826-4621

The sensible alternative to Versatec Series 1100 and Series 800 plotters



The Houston Instrument Series 8400 is a better choice for OEM users of the Versatec Series 1100 and 800 plotters. The 8400 Series gives you unparalleled performance and speed in presenting either free form graphics or alphanumeric data at a price well below that of competitive plotters-plotter/printers.

- Plug compatible with existing 1100 and 800 plotters.
- Software compatible with existing 1100 and 800 plotters.
- Performance compatible with existing 1100 and 800 plotters.
- All of this with quantity one prices starting at \$5150.

*U.S. Domestic Price only
* Registered trademark of Houston Instrument

For rush literature requests or local sales office information only, persons outside Texas call toll free 1-800-531-5205

COMPLØT[®] SERIES 8400 ELECTROSTATIC PLOTTER/PRINTERS — PLOTTERS

Give us a call today for complete information.

**houston
instrument**

ONE HOUSTON SQUARE
(512) 837-2820

DIVISION OF BAUSCH & LÖMB

AUSTIN, TEXAS 78753
TWX 910-874-2022

EUROPEAN HEADQUARTERS: Rochesterlean 6 8240 Gistel Belgium
Phone 069/277445 Telex Bausch 81399

"the graphics - recorder company"

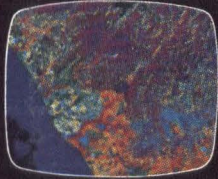
CIRCLE 179 ON INQUIRY CARD

When you need color graphics, Ramtek has it all.

Color. A surprisingly powerful way to add information, manage it, increase the efficiency of its use. However you plan to use it, there is only one company with the breadth of line, the technological mastery, to give you the choices you need without compromise—or needless costs.

It's Ramtek. For color graphics. For imaging. Ramtek has what you need:

The Ramtek 3000. Eight models let you explore the possibilities of color graphics the moment you plug in your application software. Stand alone image processing and graphics. Fully integrated and ready to go. Desk configuration.



The Ramtek 9000 Series Display Controller. Four models. Total modularity. Buy just what you need; add to it at any time. The high-performance family.

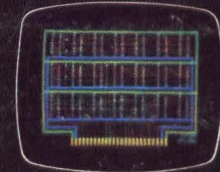
The industry standard in imaging and graphics raster scan color.

The Ramtek 9050 Series Display Controller. Four models. The most popular elements of the 9000 Series are here packaged for economy. All

are software compatible with the 9000, have expandable memory and interactive capabilities.

The Ramtek Colorgraphics Computer Terminals.

Three models let you choose between economy, optimum price-performance, or maximum resolution-performance. Easy



to program. Easy to use. Easy to interface. Interfaces to the Xerox 6500 Color Graphic Printer for color hard copy output. These are the price, industry and performance leaders in raster scan color graphics terminals.

The Ramtek Monitor Family.

Nine models. Up to 1024 line addressability on the screen in color or black and white. CRT sizes 13" or 19" Cabinet or rack mounted versions.

Ramtek Large Screen Projection.

Interface Ramtek's or your own large screen projection unit easily, quickly. And there's more to come. From Ramtek, the world's largest independent manufacturer of raster scan color graphics and imaging equipment. Direct sales in the U.S. and Canada. Distributors worldwide plus a worldwide network of customer service and depot repair stations.

For more information, write:

Ramtek, 585 N. Mary Ave.,
Sunnyvale, CA 94086.



ramtek
Our Experience Shows

REGIONAL OFFICES: Sunnyvale, CA (408) 735-8400 • Newport Beach, CA (714) 979-5351 • Dallas, TX (214) 422-2200 • Huntsville, AL (205) 837-7000
Cleveland, OH (216) 464-4053 • Washington, D.C. (301) 656-0350 • Metropolitan N.Y. (201) 238-2090 • Boston, MA (617) 862-7720 • West Germany (0611) 771070