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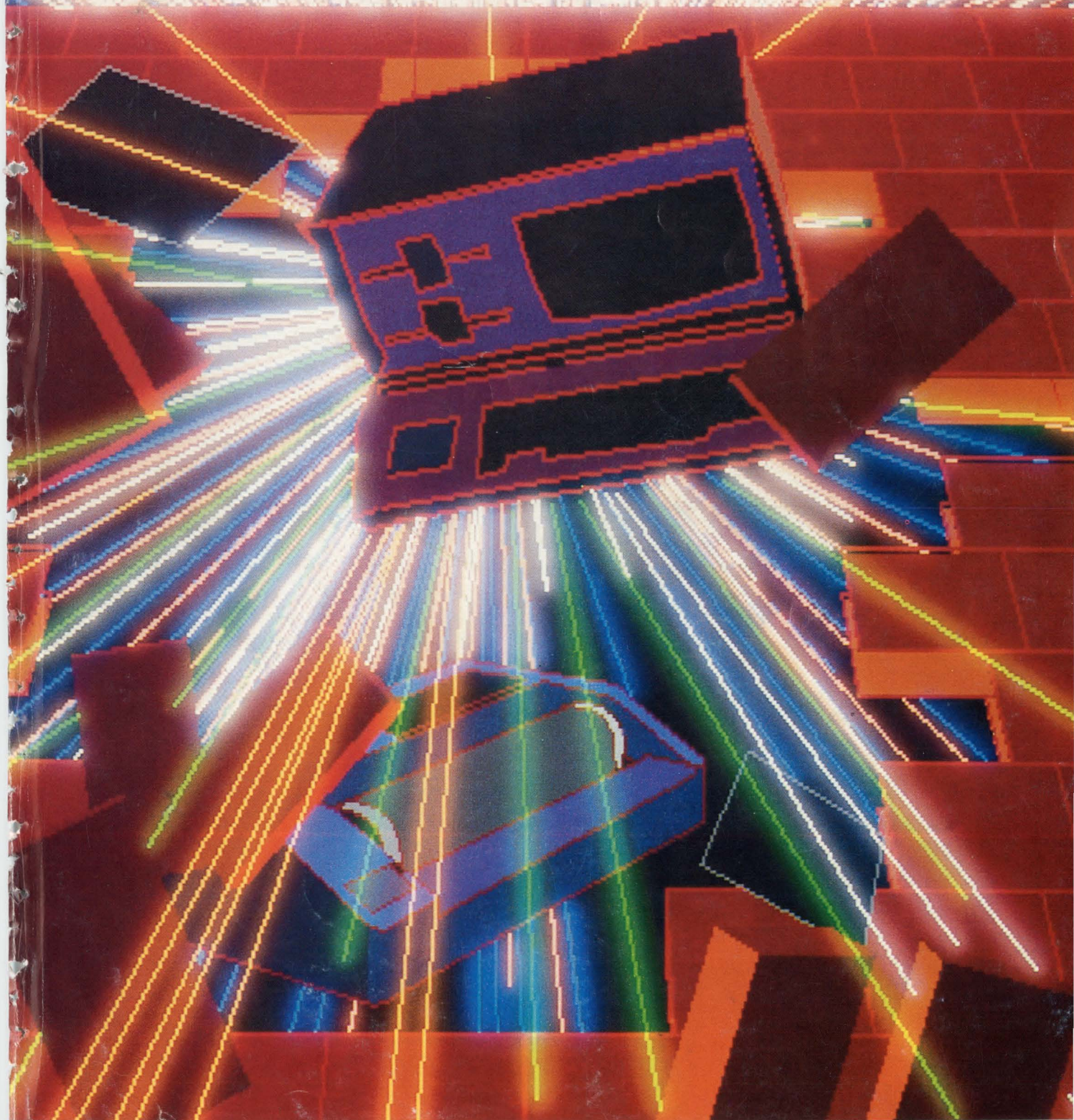
# COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

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## BREAKTHROUGHS IN MINICOMPUTER SYSTEMS



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CIRCLE 1

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CIRCLE 2

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## Realtime system integrates process control and plant information

Parallel processing has brought about complete integration of process and information management in a control system announced at the October Instrument Society of America (ISA) conference in Houston. The TDC 3000, introduced by Honeywell's Process Management Systems Div of Phoenix, Ariz, functions in real time through a local control network (LCN). Data Hiways link microprocessor-based multiloop controllers, application modules, and computing modules to the 5-Mbit/s LCN via gateways that buffer and translate data. Other gateways link the system to plant computers and instrumentation subsystems.

Three levels of control are maintained: the hardware oriented single function process level, the unit control and optimization level, and the plant-wide strategy level. All levels interface through a universal station that provides a single window to all information. Plant data acquisition and control functions for both continuous and batch processes are integrated. Information access is provided at the station via keyboard and CRT or through an optional touch screen. When an alarm light flashes on the display, the operator merely touches that alarm on the screen. Detailed information to assist the operator's next action then appears.

## I/O system converts Rainbow to data recognition systems

Although not yet officially announced by Data Translation (Marlboro, Mass), the Digital Equipment Corp booth at ISA contained a DT311 I/O subsystem attached to a Rainbow 100 personal computer to form a complete data acquisition and control system. A microprocessor interface to the Rainbow controls all analog and digital I/O operations and self-test functions. The subsystem, part of the manufacturer's PC/DAX family, can be programmed under CP/M or MS-DOS.

## The other PCs still in evidence at ISA

Programmable controllers, which were known as PCs long before the now better known personal computers were even available, are still a major part of the plant and factory control picture. Both types of PCs could be seen at various ISA booths but it was apparent that the new PC was not likely to eliminate the longer established PC in the near future.

## True 32-bit micro debuts

Claimed to be the first commercially available 32-bit microprocessor, the NS32032 was introduced last month by National Semiconductor of Santa Clara, Calif. The chip, a member of the company's NS16000 family, features true 32-bit internal and external architecture and supports high level languages. Unlike its competitors, the IC's internal and external buses both for addresses and data as well as the ALU and registers are all 32 bits wide. This configuration effectively speeds up computational operations, in some cases halving the time that data circulates among memory, ALU, and registers. The company anticipates that, because of the chip's features, many current mainframe and minicomputer OEM companies will find it easy to transport their 32-bit high level software onto 32032-based systems. A 6-MHz version of the chip is available immediately for \$220 in high volume quantities. A 12-MHz chip will be available in the first quarter of 1984.

## UP FRONT

### Word processor types as if it writes

A handheld word processor that uses only five keys to type a letter as one would write the letter by hand has been imported from England by Microwriter Ltd of New York. The unit contains an 8-Mbyte nonvolatile memory and can be attached directly to printers. It is programmed, when attached to a video screen via an RS-232 serial interface, to send out ASCII code according to the sequence of the activated five keys. The company claims that a typical user can learn the appropriate sequence of keys for the entire alphabet including punctuation marks and numerals in about an hour. Unit price is \$499.

### English is not English-like

Themis, a friendly query program, uses artificial intelligence concepts to allow users of VAX-11 machines to pose commands in English. This frees the users from learning another set of English-like instructions, which is a common chore for most query programs. The software can understand up to 900 common English words and can be expanded by the user for a specific application. The package runs in 1.5 to 2 Mbytes of main memory and requires either VAX-11 Datatrieve or the Oracle relational database management system. Themis will be available from Frey Associates of Amherst, NH in the first quarter of 1984 at a price of \$24,500. A similar program for running on IBM machines will soon follow.

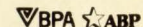
### Netting relational data bases

Ingres owners can now expand their reach by using Ingres/Net, a software package that allows distributed access to remote data bases on any VAX computer that is part of a DECNET network. Thus functions can now be distributed with applications running on the user's local system while the Ingres database management systems can run remotely. According to the company, Relational Technology Inc of Berkeley, Calif, this configuration decreases communication costs and improves response times for interactive applications. With Ingres interfaces such as queries, graphics, reports, and applications-by-form, the user can display, update, or retrieve data stored on any VAX in the network. Network access is transparent to the user. Ingres/Net will also be available on 68000-based systems that support Ingres in the Unix environment.

### Matrix printer prints quality letters

A letter-quality multimode matrix printer will be introduced at the Comdex Fall show later this month in Las Vegas. Designers have incorporated key features in today's office printer in a dot-matrix unit such that the output is distinctly letter quality. Letter mode runs at 45 char/s while "draft" mode prints at 250 char/s; a third mode yields a 16 x 72 matrix at a rate of 100 char/s. Multiple fonts are available. The multi-color graphics resolution is 240 x 720 dots/in. Advanced Matrix Technology, Inc (Newbury Park, Calif) plans to have full production capabilities by the first quarter of 1984. Initial OEM price will be \$2995.

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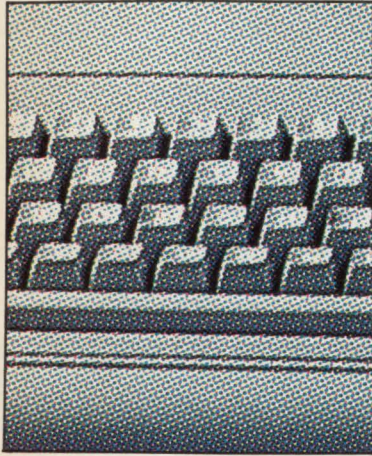
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CIRCLE 4

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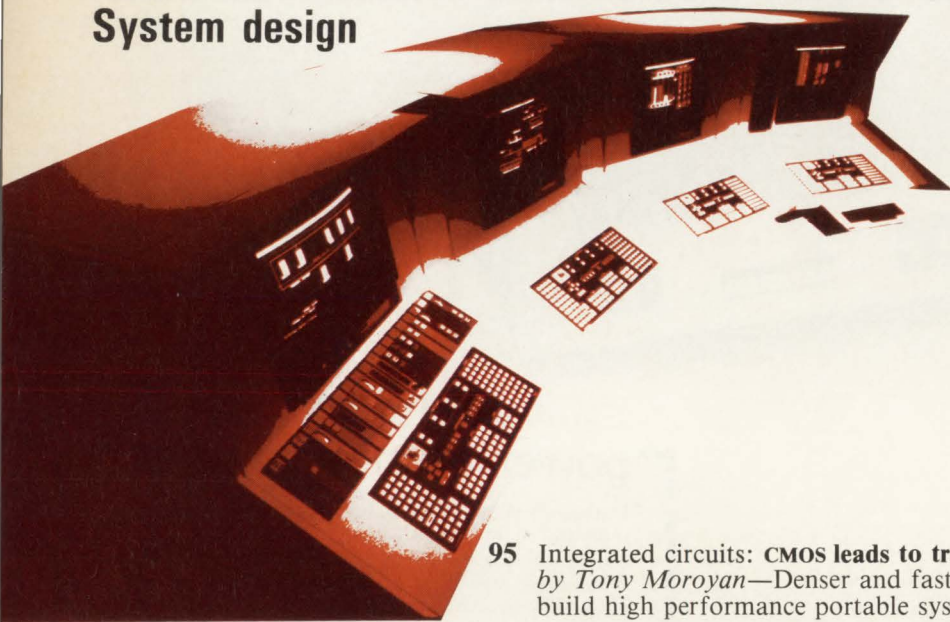
## System technology



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## System design



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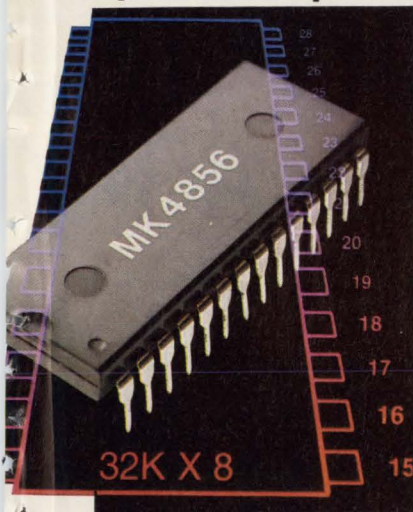
## Special report on minicomputers

- 163 Caught in the throes of change, minicomputers are taking on new technology and adopting new architectures in preparation for the future. These moves, necessary to fend off the sallies being made by both micros and mainframes, are both evolutionary and revolutionary. With performance levels boosted by both technology and innovation, today's systems continue to hold the price line. Newcomers entering the market bring with them nontraditional concepts. This influx of new blood virtually guarantees that minicomputers will fend off threats from 32-bit micros as they arrive on the scene.



This month's cover was created and designed by Mark Lindquist and Alan Green on the Digital Effects Video Palette III and D-48 high resolution camera system.

## System components



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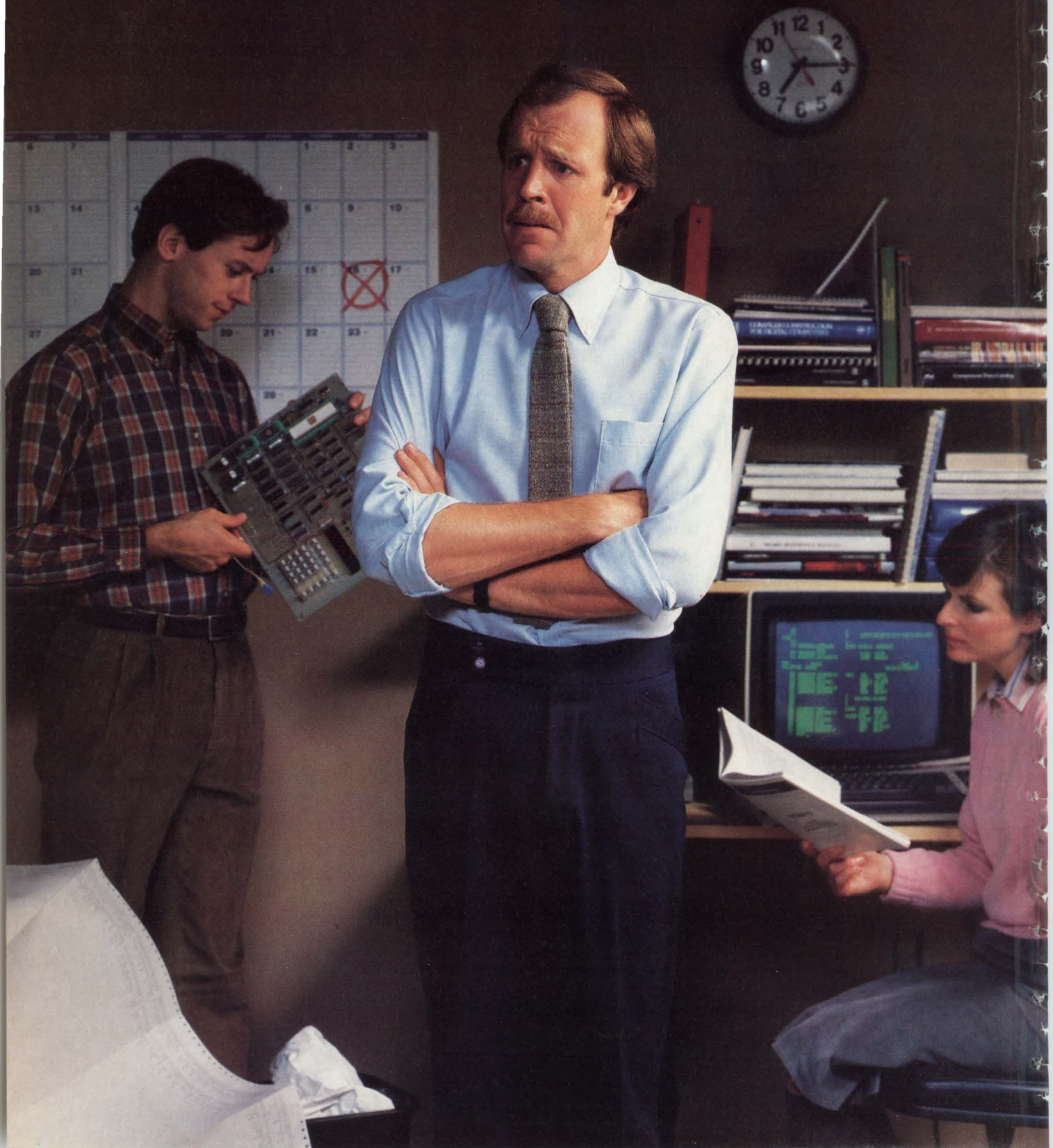
## Designers' preference survey\*

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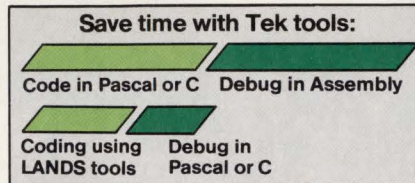
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\*Patent Applied For

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```

end;~
UAR~
  current := state;~
~
PROCEDURE wait(seconds : integer); EXTERN;~
  (* waits for "seconds" seconds and returns *)~
~
FUNCTION pedestrian : boolean; EXTERN;~
  (* returns true if a pedestrian pushed the crosswalk button *)~
~
PROCEDURE maple(newcolor : color); EXTERN;~
  (* changes Maple Street light to "newcolor" *)~
~
PROCEDURE crosswalk(newmessage : message); EXTERN;~
  (* changes crosswalk signal to "newmessage" *)~
~
BEGIN (* trafficlight *)~
  current.light := green;~
  maple(current.light);~
  crosswalk(dontwalk);~
  WHILE true DO ~
    BEGIN~
      WHILE NOT pedestrian DO (* nothing *) ;~
        current.light := yellow;~
        current.time := yellowlength;~
        maple(current.light);~
        wait(current.time);~
        writeln;~
    END;~
  END;~
Parsing complete, no errors detected.

```

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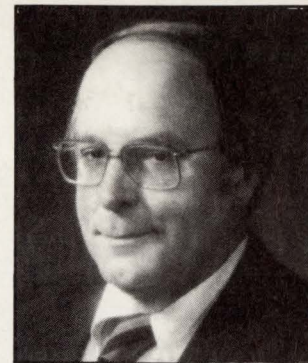
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# DEMOCRATIZING THE IEEE

What I have to say this month is more of a personal statement than an editorial. As a long-standing and long-suffering member of the Institute of Electrical and Electronics Engineers, I believe control of that organization should be returned to its membership. To further the goal of making the IEEE a participatory democracy, I hope to cast a write-in vote for Irwin Feerst, chairperson of the Committee of Concerned EEs, as president-elect.



I say that I "hope" to cast my vote because, unlike most IEEE members, I have not yet received a ballot form. One of the many ways in which the IEEE subverts the democratic process is to mail ballot forms via third-class mail instead of first-class mail. The postal service does not forward third-class mail, therefore, those engineers like me who relocated to pursue new job opportunities are automatically disenfranchised. However, the IEEE is careful to send bills for membership dues via first-class mail. So, the message from the IEEE seems to be "We want your money but don't bother to vote."

Such petty harassment, however, is not a new experience for IEEE members. What does seem new is the organization's recent heavy-handed suppression of possible dissent within its ranks. In moves reminiscent of Richard Nixon's famed "Saturday Night Massacre," the IEEE fired Malcolm Drummond, head of its Pension Task Force, and precipitated the resignation of David Lewis, head of its Manpower Task Force. Both men seemed guilty of nothing more than doing their jobs: Drummond dared to write a letter to the president of RCA asking why retirement benefits of two RCA engineers had apparently been arbitrarily reduced. Lewis had testified at hearings of a Congressional subcommittee on immigration and had dared to recommend a return-home requirement for foreign engineering students after their graduation from U.S. colleges.

Drummond acted at the direct request of two IEEE members. If he had failed to act, he would have neglected an obligation of his position. As it turned out, however, he need not have bothered because his superior within the IEEE—Edward J. Doyle, vice president for Professional Activities—subsequently apologized to RCA and fired Drummond. Lewis also fell victim to the treachery of Doyle. In the July 1983 issue of *The Institute*, an IEEE publication, Doyle coauthored an article with Lewis in which they supported legislation requiring alien engineering students to return home upon graduation. After the article was published, and long after Lewis had gone out on a limb before the House Subcommittee on Immigration, Doyle reversed himself and voted with the rest of the U.S. Activities Board of the IEEE to permit many exceptions to the original policy.

The list of ways in which the IEEE has resisted participatory democracy seems endless. There have been a succession of proposed constitutional amendments to do such things as increase the number of signatures required on a nominating petition, move up the dates by which petitions must be filed, and delay by a year the date on which a new president-elect assumes office. Also, overseas members have long held proportionately greater representation than U.S. members, thus violating the basic principle of "one person, one vote."

All things considered, I have the feeling that the corporate and academic hierarchy controlling the IEEE no longer gives a damn about the individual members or the unpaid volunteers who help run the organization. Though I disagree with Irwin Feerst on some issues, I think he really cares about American working engineers—who constitute the bulk of the membership of the IEEE—and he has steadfastly represented their interests for many years. Finally, I would add that it seems fitting for such an Orwellian organization as the IEEE to be celebrating its centennial in 1984.

Michael Elphick  
Editor in Chief

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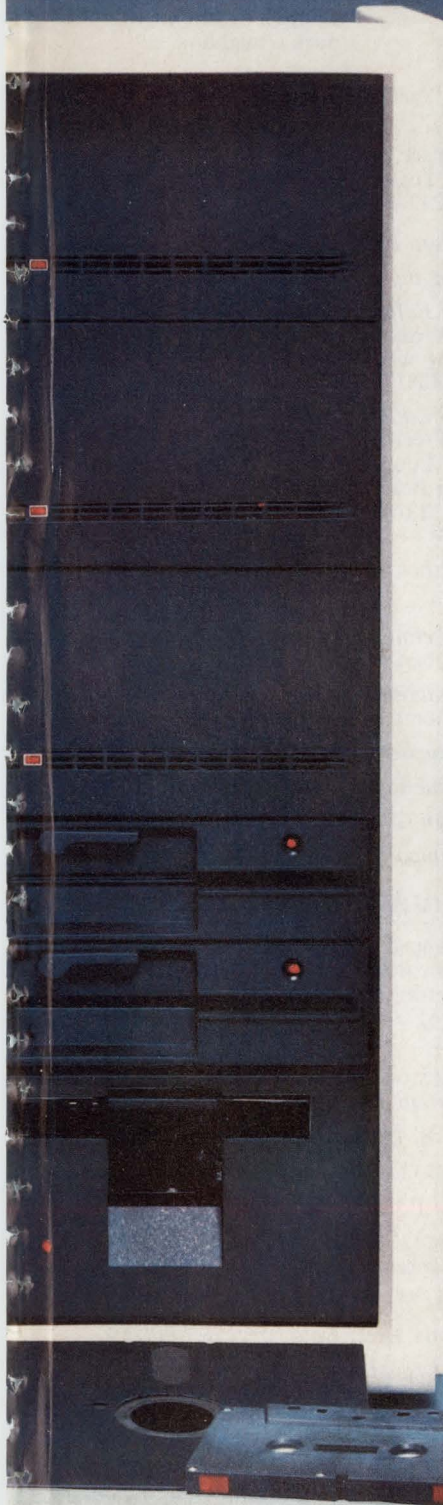
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Best of all, CARTOS runs on a family of low-cost, flexible minicomputer systems called dataCASE/5. dataCASE/5 supports a large variety of CPUs and storage media. Floppies. Winchester. Streaming tape. Use any media you want in any combination you choose up to 1/2 gigabyte of capacity. With a 45 MB tape backup.

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## Major Capabilities

### State analysis

- Symbolic debugging
- Disassembly display
- Multi-tracing
- Multi-triggering

### Timing analysis

- EXT 8 channels
- Sampling clock...max. 100ns
- Glitch detection...min. 15ns

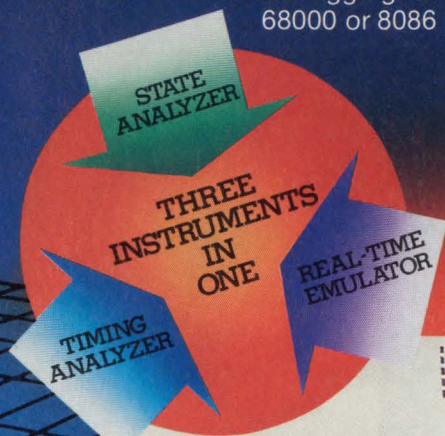
### Real-time emulation

- Internal 28K bytes RAM
- Assembly function of single-line program
- Active tracing

### Standard Accessories

- Minifloppy disk drive
- RS-232C interface
- Video/hard copy ports

Microprocessor Compatibility:  
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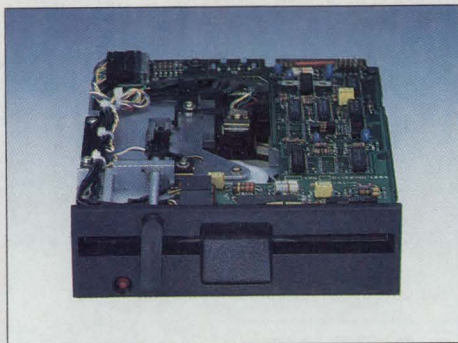
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# ACADEMIA AND THE SHARK—PART II

This magazine, in its Sept 1983 editorial "Academia and the Shark," criticized the universities in general, and me in particular, for exaggerating the threat to the U.S. of the Japanese Fifth-Generation Computer Project. Even though the cart came before the horse, I welcome this opportunity to familiarize the editor and readers of *Computer Design* with my views on this important topic.

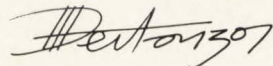
Many of us believe that the information revolution will affect our world more profoundly than the industrial revolution. Looking back, we find at the world's economic and geopolitical helm the countries that led that older revolution. Looking ahead, we can expect the same fate for the nations that will control the information revolution. Japan recognizes this historical inevitability. Drawing on its superior electronic base and its technologically oriented population, and motivated by its lack of natural resources, Japan has declared its intent to achieve world supremacy in information technology within a decade. Its lead vehicle is the Fifth-Generation Computer Project, a \$1 billion government-industry effort to harness 1000-processor machines and artificial intelligence techniques into systems that understand human speech and images, translate spoken languages, and provide expert services.

This effort deserves our most serious attention for the following reasons. First, it deviates from the Japanese tradition of incrementally improving the cost-performance of existing goods, and strives instead to leapfrog the products and strategies of U.S. computer companies. Second, unlike our own corporate orientation, it focuses on potentially the most "cerebral" part of the information revolution. Finally, it will develop, within the leading Japanese companies, numerous experts in artificial intelligence, multiprocessor architectures and their applications. As a result, Japan may produce novel variations in ordinary products, like speech-driven TV sets, even if their loftier project goals are never met. An unprepared U.S., awakening to such surprises 5 or 10 years from now, will not be able to recover gracefully because it will need several years to build comparable knowledge within its own companies.

To compete with Japan in this new arena, we must strengthen our long-term orientation. One proven method is to increase government funding of basic research. The current Department of Defense initiative, which has yet to be approved by Congress, is a good start toward that end. Meanwhile, we can hear the familiar criticism that such programs need more specificity—a carry-over of our short-term bias that kills the flexibility needed for successful long-term research. The Microelectronic and Computer Technology Research Corporation is another good start, but it must prove its resilience against the short-term pressures of its corporate owners. Beyond these steps, more could, and should, be done to link longer-term thinking with the profit motive: For example, substantive tax credits could be given to companies pursuing longer-term research, and long-term financial instruments could be used to spread the associated costs and gains among willing investors. Our companies could also learn from the Japanese to carefully watch rather than ignore academia's long-term dreams and results. There are also things that we must not do. We must not, for example, restrict access to basic research, since the benefits of reduced information leakage would be overshadowed by our inability to share ideas and to utilize the brainpower of foreign scholars.

One reaction to such proposals is that competition between the U.S. and Japan is a provincial and less desirable alternative to international cooperation. Yet, we are starved for examples of technological progress without competition, so that in the long run the global welfare may be better served by competitive national tribalism.

The editorial suggests another reaction: that academics use the Japanese threat in order to increase their research budgets. Motivation notwithstanding, the fact is that industry will be the principal beneficiary of the programs under way by at least a 70 to 30 ratio. Finally, the editorial's principal contention—that the actual damage caused by sharks is considerably smaller than the accompanying Hollywood hoopla—offers little comfort to a swimmer devoured. Complacency is no substitute for vision.

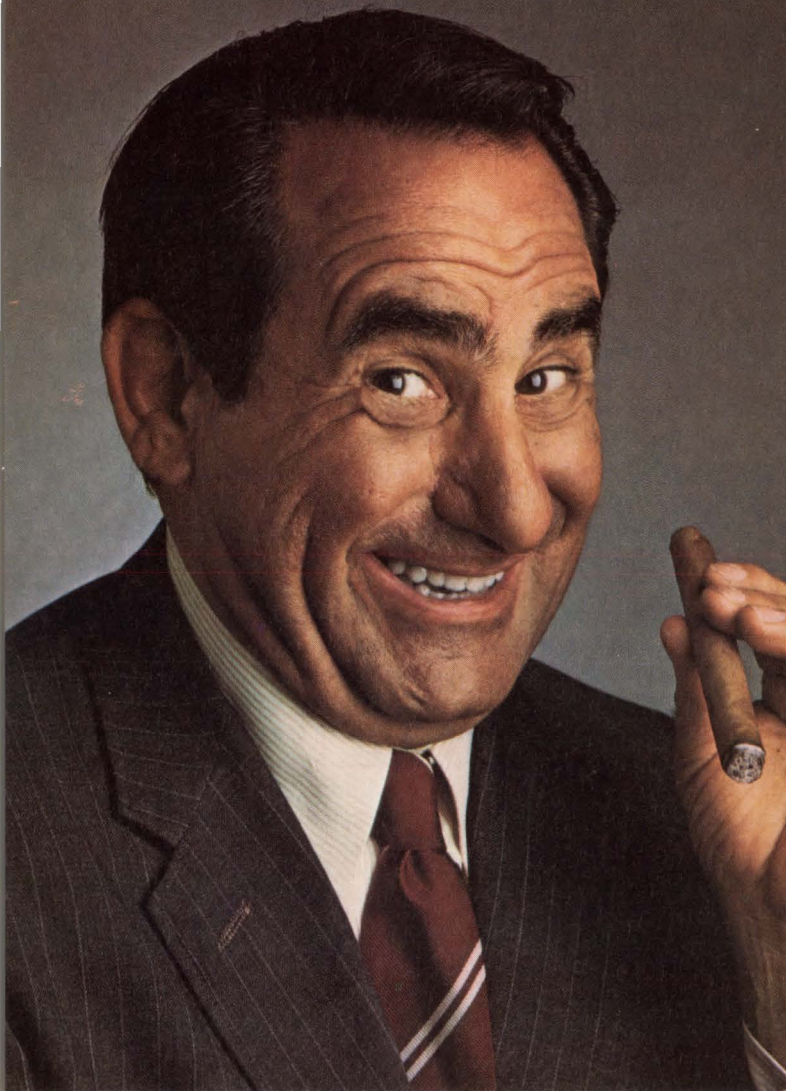


Michael L. Dertouzos  
Professor and Director  
MIT Laboratory for Computer Science



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“If you average all  
our outgoing shipments.”

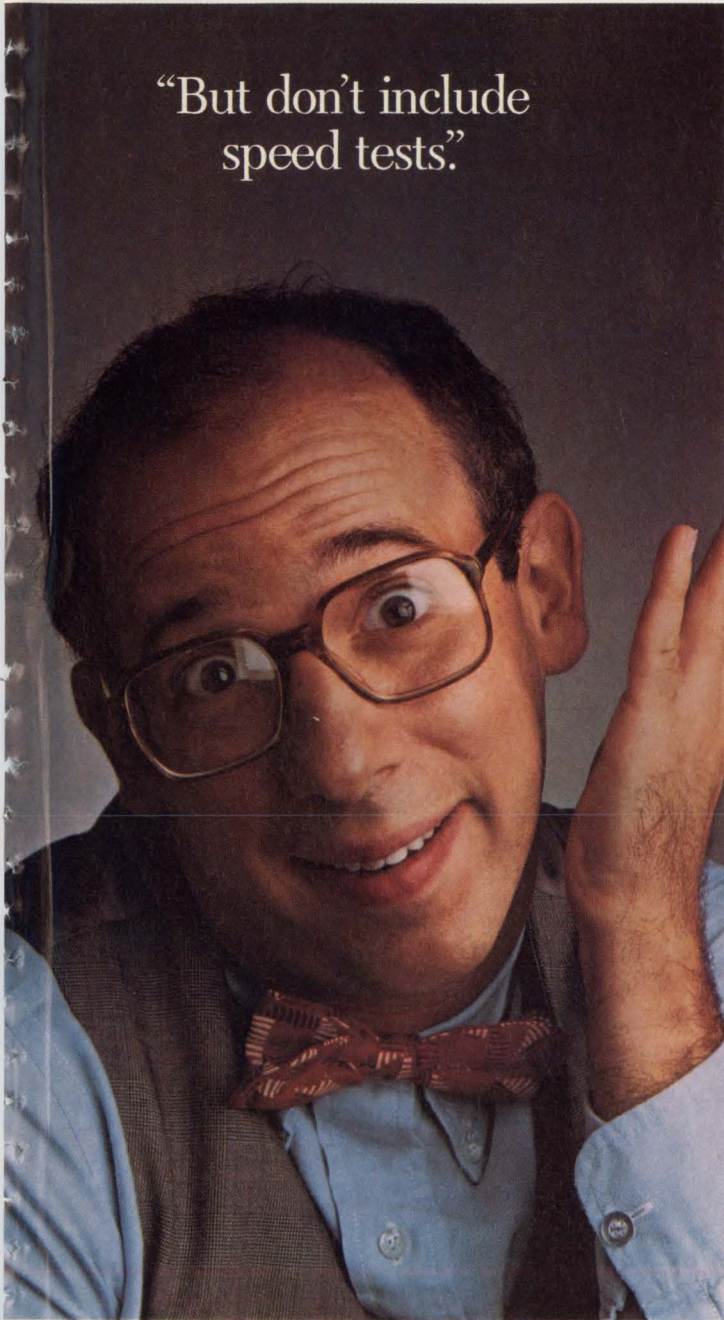


“And test at room  
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# ANDS. NO BUTS.

"But don't include  
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Some chip makers spend more time making exceptions than they do making parts. Their guarantees run on and on and on.

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How much are you willing to bet on the new technologies that promise more and more megabytes in a 5 $\frac{1}{4}$ " drive?

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Your reliability?

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You could end up betting them all, and losing, because many of the new technologies are still unproven and could result in serious damage to your customer's data base.

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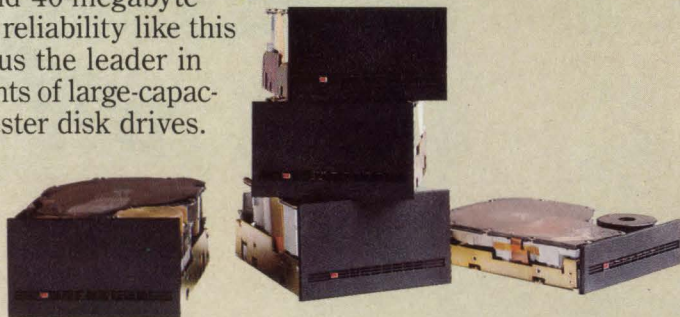
The result of this philosophy is a remarkable plug-and-play reliability record for our complete line of 12, 19, 26 and 40-megabyte drives. And it's reliability like this that has made us the leader in volume shipments of large-capacity 5 $\frac{1}{4}$ " Winchester disk drives.

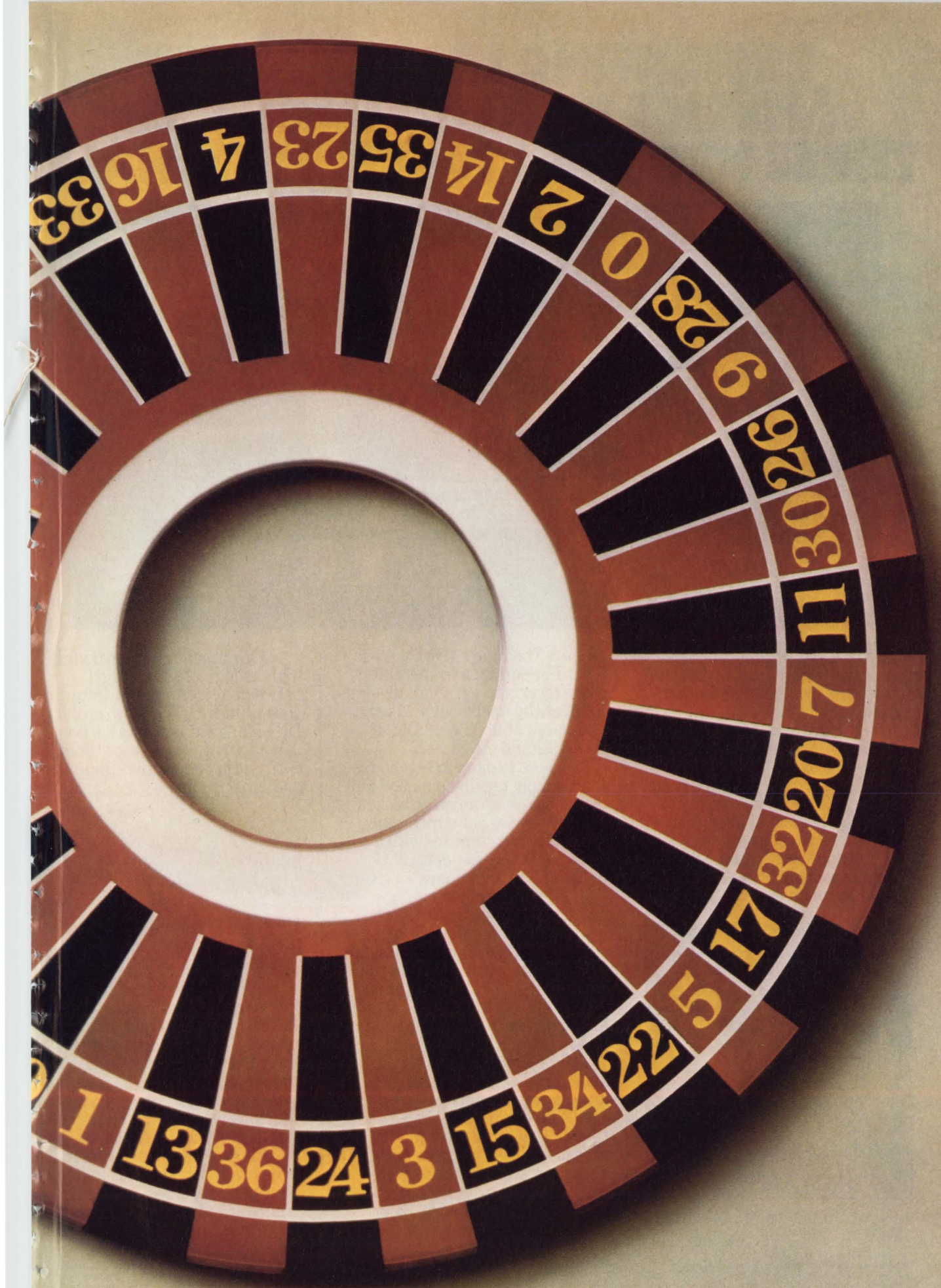
Of course, the time is coming when the industry will demand a 60 or 80 or even a 160-megabyte 5 $\frac{1}{4}$ " disk drive, and you can expect Computer Memories to deliver it. Without delivering a risk.

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Have you noticed that the more high technology we put into the workplace, the more human touches the workers put in? There's a real need to soften the interface between people and high technology.

That's why we designed our new High Touch™ terminals to work together with biology, not just with technology.

Our new generation of High Touch terminals brings an elegant new touch to our American

Dream Machine (ADM™) tradition. The family features three new ergonomic terminals designed to meet the needs of OEMs and end users alike: The ADM 11, ADM 12 and ADM 24E.

There is more to ergonomics than simply tacking on a few fad-dish features as an afterthought. That's why we put our thinking in up front. And came up with a whole new way for terminals to relate to humans.

No aspect of terminal design escaped our deepest consideration. Or reconsideration. Dozens of little touches add up to the convenience and comfort of High Touch. For example, we put the power "on/off" switch and contrast control knob in front where they're easy to reach.

The monitor not only tilts and swivels, it stops positively in almost any position.

The clean, crisp display features a large character matrix on an easy-to-read green or amber non-glare screen—made even easier to read by the hooded bezel. Screens are available in 12" or 14" sizes.

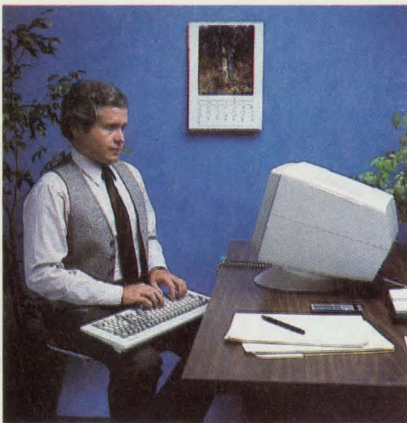
Our uncluttered keyboard, with its logical separations between key groupings, improves your efficiency. The low-profile, DIN-standard keyboard is not only tapered, its angle of tilt is easily adjusted for maximum operator comfort.



*Low profile DIN-standard keyboard with adjustable tilt.*

The Selectric® layout with its sculptured keys makes data entry easy and efficient. And we placed the *control* and *escape* keys close to the alphanumeric keys, where people just naturally expect to find them.

The ADM 11 is a High Touch conversational terminal that accepts data continuously at 19.2 kilobauds. It features separate cursor control keys logically arranged in a cross for ease of use. Four modes are provided for the printer interface: page print,



*6' coiled cable lets you put the keyboard anywhere.*



	<b>ADM 11</b>	<b>ADM 12</b>	<b>ADM 24E</b>
Programmable Function Keys	4 (Shiftable to 8)	16 (Shiftable to 32)	16 (Shiftable to 32)
Non-Volatile Function Keys	Optional	Standard	Standard
Function Key Legends on 25th Line	From Host	From Host	Standard Non-Volatile
No. of Pages of Display Memory	1	2	2 or 4
Display Memory Configurations (Plus 25th message/status line)	24 lines by 80 characters	(2) 24x80 or (1) 48x80 or (1) 24x158	User-Definable up to 96x80
Scrolling	Standard Scrolling	Smooth, Jump or Horizontal Scrolling Split Screen	Smooth or Jump Scroll Split Screen
Transmission Mode	Conversation Mode	Conversation or Block Mode	Conversation or Block Mode
Editing	Limited	Full Editing & Protected Fields	Full Editing & Protected Fields
Visual Attributes: Reduced Intensity, Blink Blank and Reverse Video. Underline also on ADM 12 and ADM 24E	3 Embedded 1 Non-Embedded	5 Embedded or Non-Embedded, plus Full Screen Reverse Video	6 Embedded or Non-Embedded, plus Full Screen Reverse Video and Highlight
OEM Flexibility	Modifiable Set-Up Characteristics	Modifiable Set-Up Characteristics & Personality	Modifiable Set-Up Characteristics. Add to Program in ROM or Down-Line Load in RAM (56K ROM or RAM. Plus up to 22K Display Available) Room for add'l Logic Boards.

line print, transparent print, and display and print. There are four programmable function keys (shiftable to eight). And two levels of setup mode to reduce errors while still giving the operator maximum flexibility.

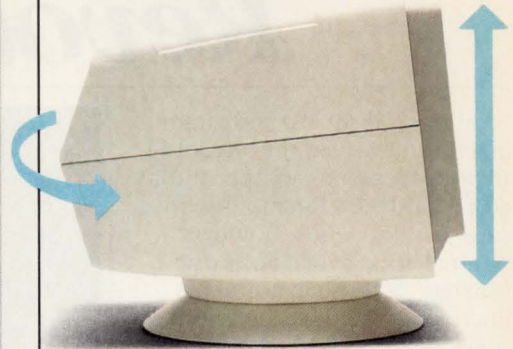
For a High Touch terminal with editing and more, choose the ADM 12. It features five non-embedded attributes. Embedded mode can also be selected for existing applications. And 16 programmable non-volatile function keys (shiftable to 32). The display memory can be configured as two 24 x 80 character pages, or one 48 x 80 page, or one 24 x 158 page. The terminal runs in either conversational or block mode.

Or choose our top-of-the-line ADM 24E which features a moveable 24-line window you can use to look at 48 (or 96) lines of memory. The ADM 24E also offers plenty of additional space for OEMs, with up to 56K ROM or RAM available for add-on programs. Plus up to 22k display RAM.

When it comes to terminal technology, we're the historic leader with the largest installed base. Our terminals are used in

more computer-based systems than any other.

When you buy Lear Siegler, you're buying proven quality and reliability, backed by the broadest network of full service centers anywhere. That means you can get walk-in Express Depot™

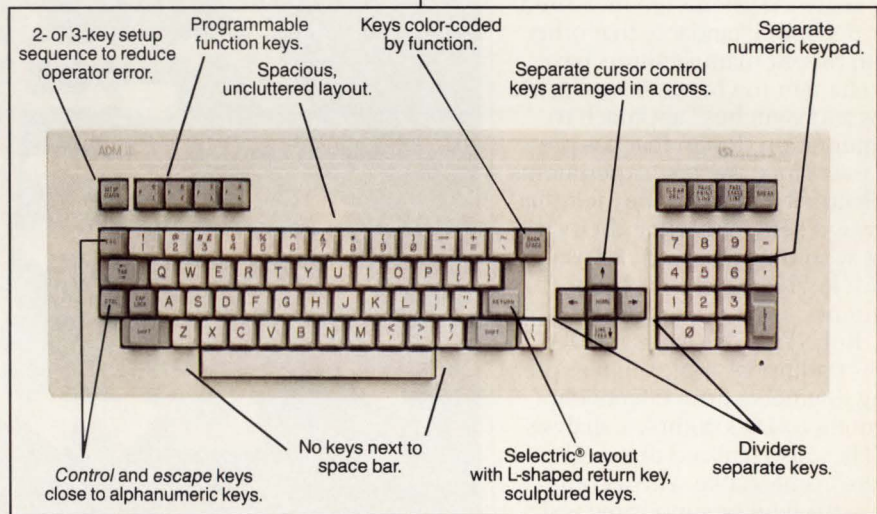


Monitor tilts and swivels to almost any position. Available with 12 or 14 inch screen.

service, on-site service and extended warranty service in 3,000 cities nationwide.

Lear Siegler High Touch terminals are made in America—designed, engineered, manufactured and shipped from Anaheim, California to provide you with the best local support.

And that's just one more reason they're called the American Dream Machines.



ADM 11 keyboard.



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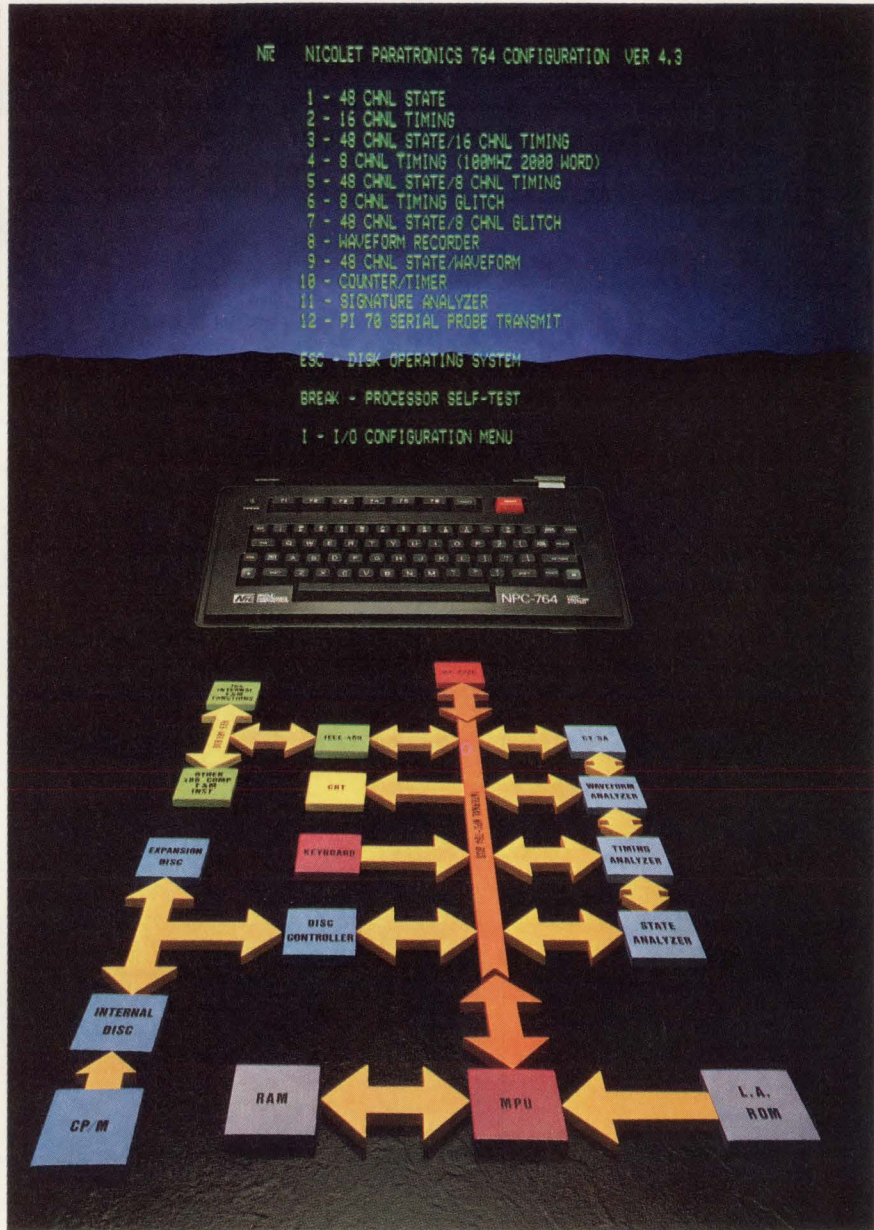
# The NPC-764: More Evolutionary than Revolutionary.

In the mid-1970's, instrument manufacturers viewed the advent of the microprocessor as an opportunity to replace hardware functions with software. Until recently, however, the external appearance and basic functionality of these instruments remained unaffected by the internal microprocessor. As far as the user was concerned, knobs still had to be rotated, switches set, and LED or similar displays interpreted.

The NPC-764 was the first instrument to give the user direct access to its internal microcomputer. This was made possible by replacing all knobs, switches, and readouts with an ASCII keyboard, a CRT, and an integral floppy disk. Since its introduction, the NPC-764's feature set and accessories have been greatly expanded. Today, because it is a proven, highly-reliable instrument, the NPC-764 is the standard by which similar analysis systems are measured.

It's understandable that other test equipment manufacturers have been reluctant to change from the old "knobs and switches" approach to instrumentation design that has prevailed ever since the first experiments with electricity. Perhaps they felt that there was a certain risk that their customers would not be ready to use an ASCII keyboard to control an instrument.

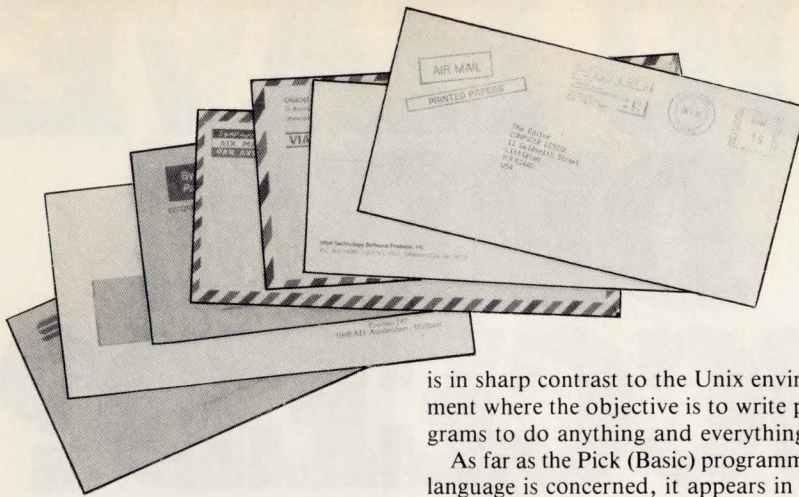
But NPC's designers realized that this traditional approach was preventing engineers from effectively performing today's complex analysis tasks. They also realized that engineers are comfortable with a computer controlling or supporting test functions.



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### Other 16-bit options

In the article "Options Abound in 16-bit Operating Systems," (Aug 1983, p 113), there was no mention of the participation of Zilog Systems, along with the three firms, in a joint development effort with Western Electric, to produce versions of the Unix system V operating system compatible with leading 16-bit microprocessors.

The planned z8000 version of system V demonstrates Zilog Systems' continuing commitment to Unix, which began in 1979 when Zilog became the first microprocessor manufacturer to acquire a source-code license for a Unix system. Furthermore, the new operating system will also run on our system 8000 family of "supermicro" computers, which has used a licensed Unix system since its introduction in 1981, making it the leading commercially installed microcomputer running Unix or its derivatives.

Joan Marzullo  
Zilog  
1315 Dell Ave  
Campbell, CA 95008

### Pick system and its "Basic" language

In regard to the short review of the Pick operating system in Chris Brown's article on 16-bit operating software (Aug 1983), I have found the Pick system to be an excellent application development environment, and feel that there needs to be more media awareness of this system.

Mr Brown accurately pointed out two of the system's biggest problems, lack of visibility, and lack of communication support. I feel, however, that his discussion of the data management capabilities and language support has instilled some misconceptions in readers' minds.

Mr Brown missed the major thrust of what the Pick system is—ie, a system for data management and application development in which writing a program to do a task is viewed as the last resort. This

is in sharp contrast to the Unix environment where the objective is to write programs to do anything and everything.

As far as the Pick (Basic) programming language is concerned, it appears in retrospect that the use of the word "Basic" to describe it was ill conceived. Although it is true that the general syntax is similar to Basic, that is where the similarity ends. The Pick programming language, which I will call "D," is a compiled language that supports the high level programming constructs expected of a language today. These include

```
Multi-line IF-THEN-ELSE
LOOP stmt UNTIL/WHILE exp DO stmt
REPEAT
BEGIN CASE CASE exp [CASE exp] . . .
END CASE
```

The "D" language also provides separate compilation of external subroutines, extensive character string manipulation and formatting facilities, and special constructs to operate on the variable length dynamic string arrays used in the relational file structure of the system.

Toby L. Kraft  
Kraft Enterprises, Inc  
7822 Convoy Ct  
San Diego, CA 92111

### Technological boycott of Soviets

In response to the Soviets' shooting down an unarmed commercial Korean airline (KAL Flight 007) on Sept 1, 1983, the Independent Computer Consultants Association is taking action to restrict future delivery of high technology to the Soviets.

These capabilities have recently been used to stalk and murder 269 innocent citizens of the free world. The Soviets are continuing to insist that they have the right to utilize any power they possess in any manner they see fit, without regard to international law.

In light of this situation, we are asking all high technology professionals in the free world to join with us in a total boycott of the Soviet Union. We plan to halt all shipments of computers, computer parts and components, software, technical support, manuals and publications to the USSR and its satellites.

We request that all high technology professionals in the free world look into their own hearts and, considering their own personal values, decide whether they should be party to the delivery of any more technological capabilities to the Soviets.

This boycott will last two years, or until the Soviets demonstrate a change in policy which indicates a developing sense of responsibility.

Tom Scott  
Independent Computer Consultants  
Association  
909 Mulberry Lane  
Bellaire, TX 77401

### Engineers and exploitation

Finally, some editor has dared to point out that the emperor was indeed wearing no clothes. Whereas almost the entire world applauded the magical "125% solution" and salary freezes instituted by some companies, your perceptive editorial in the Aug 1983 issue correctly pointed out the very short-sighted nature of these quick fixes. There is little question that, if the opportunity presents itself, the exploited engineers will seek employment elsewhere.

Why then, did these companies elect to use these tactics? After all, it is these same employers who are moaning about an "engineering shortage." Surely, if this shortage were real, the employers would understand the great risk they run by reducing salaries while, at the same time, insisting on a longer workweek.

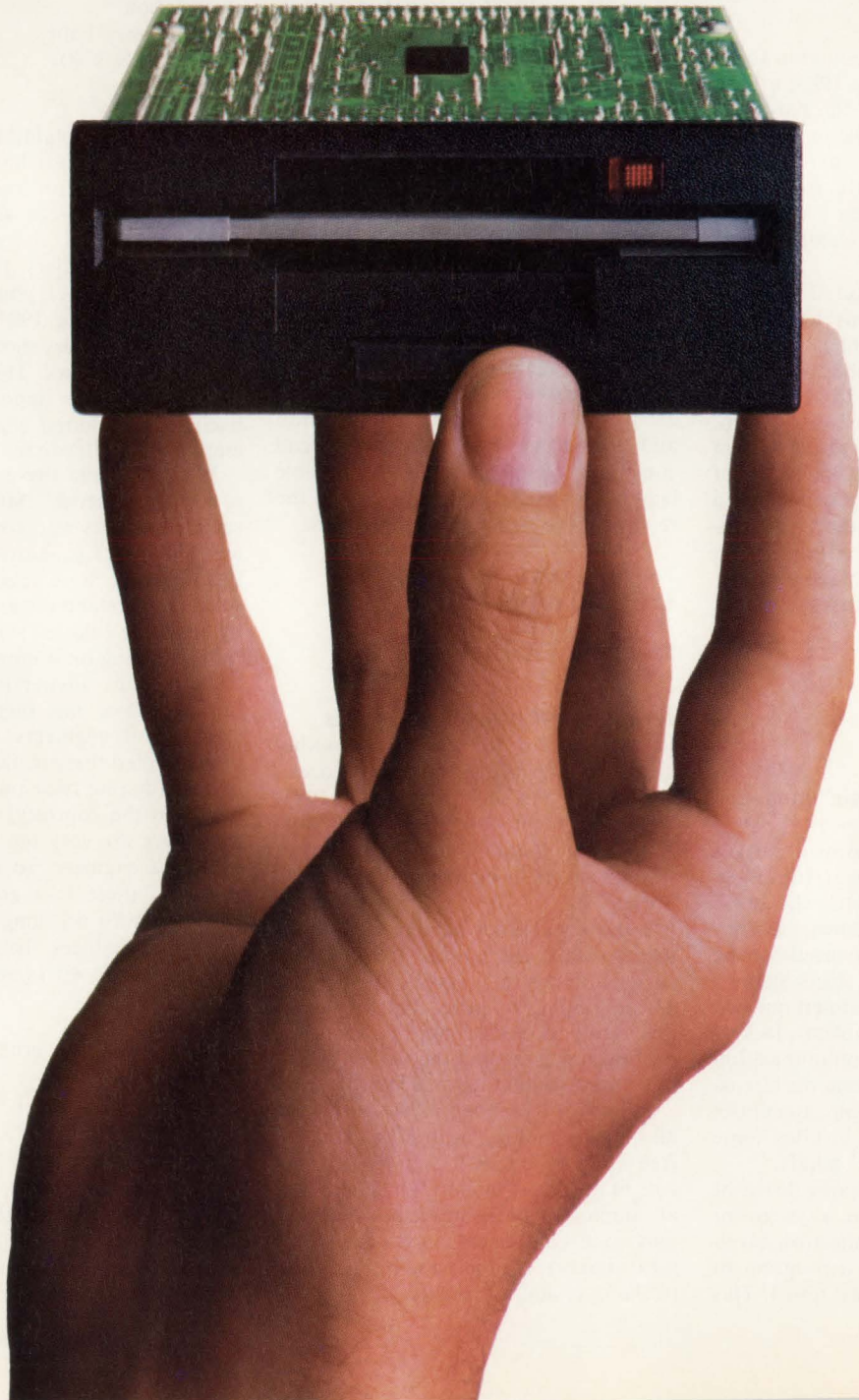
To me, the answer is clear. There is not now, nor has there ever been, a shortage of engineers. The companies who adopted these tactics are well aware of this (despite their public pronouncements to the contrary) and understand that there are very few places for their exploited engineers to go. One hopes, however, there is a great shortage of engineers who will long tolerate a company that reduces their wages and/or lengthens their workweek.

Irwin Feerst  
Committee of Concerned EES  
PO Box 19  
Massapequa Park, NY 11762

### NTIS correction

In the Sept 1983 article, "Ada Compilers—Validated and Available at Last, p 73, the NTIS order number for Ada/Ed was incorrect. The correct order number is AD-A128 707/7.

**DO YOU HAVE  
THE DRIVE  
TO SUCCEED?**



You do?

Good. So do we.

Shugart's 3.5" microfloppy drive. The SA300 by name.

And, considering where the personal/home/portable computer market is headed (betterfastercheapersmallerwithmorestorage), it's not a moment too soon.

It's also quite an achievement. One that allows you to engineer a wealth of advantages into smaller, more competitive systems.

Take the most obvious advantage, for instance.

Size. With the SA300 you can make your personal and home systems less imposing, more, well, personal. Our microfloppy takes up 75% less room than a standard sized Minifloppy.™

And it weighs just a tad over a pound. So your portable system can be more, you guessed it, portable, even with two drives in it.

Yet the SA300 still delivers 500 Kbytes in the single-sided version (1 Mbyte in the double-sided version) and uses less power, worst case, than an 8-watt night-light.

It's also so quiet, you can't hear it running unless you put your ear right down on top of it.

And with an MTBF of over 10,000 power-on hours, it should run for quite some time.

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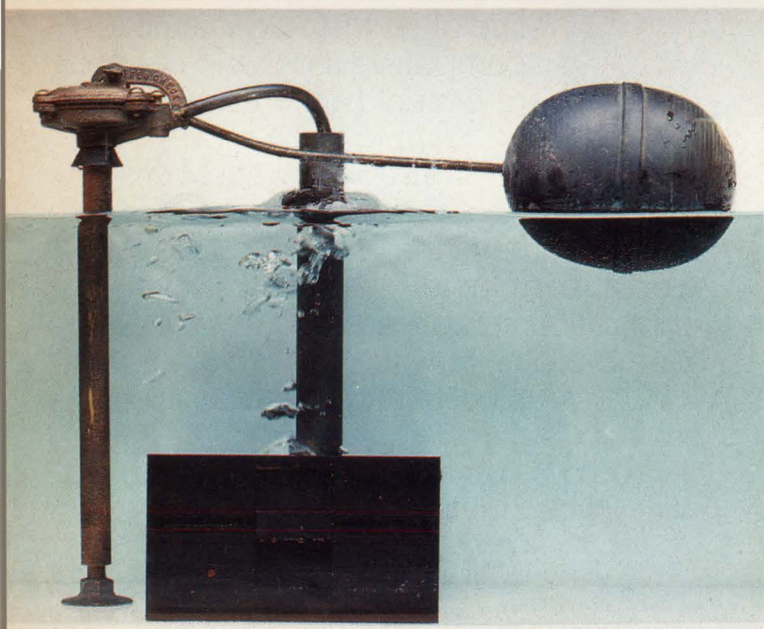
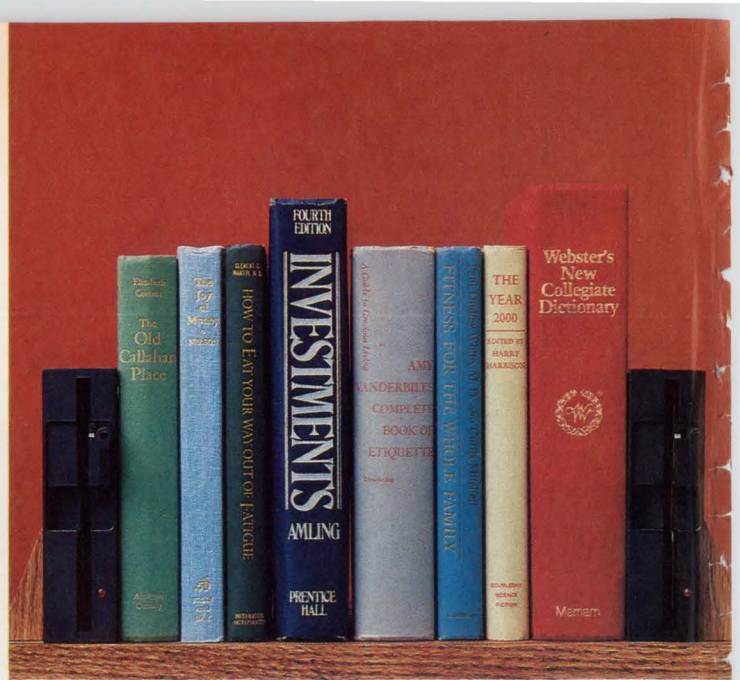
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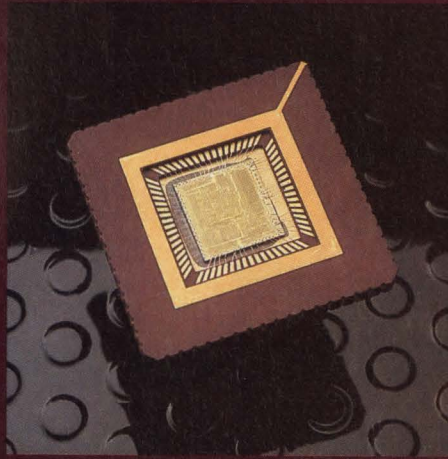
CIRCLE 17

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CIRCLE 18

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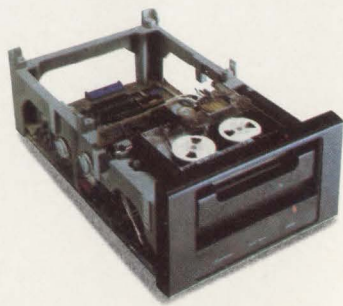
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CIRCLE 19

## Artificial intelligence systems make their mark

Computers of a higher order than the current generation of number manipulators are about to be unleashed on the engineering community. The machines are an outgrowth of the scientific community which has been, for the last 25 years, trying to learn how man thinks and how to duplicate the thinking process in a machine. A special breed of scientists has even proclaimed the term artificial intelligence as the goal of their pursuits. Comprising this group are not only bright computer scientists, but also specialists in such disciplines as linguistics, mathematics, psychology, and philosophy. While scientists in these respective disciplines have separately strived to understand and replicate man's thinking process for the past quarter century, recent maturation of commonly held concepts about human intelligence and the relatively cheap computing power available with today's technology have finally borne fruit to actual artificially intelligent systems.

Typically referred to as "expert" systems, these machines purport to possess knowledge about a subject such as the building blocks for designing VLSI circuits, and to display this knowledge in a symbolic form. The expert system then arrives at a solution by making judgment calls that are based both on an operator's input and on the machine's embedded knowledge base. Unlike today's computers that use long and cumbersome sequential line instructions to manipulate data, expert systems use symbolic procedures to yield a fast and intelligent solution based on IF... THEN rules. In terms of current programming environments, this means that instead of writing lines of code that describe all possible characteristics about an abstract object and subsequently writing more code to describe the various possible results, the programmer can make up lists of the properties associated with the object. The bank of lists is referred to as the knowledge base. Processing the knowledge base is accomplished via a control engine.



**An expert system specific to train locomotive repair is embedded in CATS-1. Users type-in responses to questions concerning the malfunction displayed on the CRT. At any time, users can call up detailed drawings of the locomotive's various components. The system identifies the cause of the malfunction and also demonstrates repair procedures from a videodisk on a separate monitor.**

The knowledge base and the control engine make up the expert system—a close approximation of human intelligence. But a machine's intelligence is derived from inference only; the engine infers certain results based on known assumptions using a tree parsing routine based on the IF... THEN rules to reach conclusions.

The artificial intelligence (AI) language that comes closest to describing the lists and procedures has predominantly been the List Processing Language (Lisp). Developed in the late 1950s, it has only recently borne fruit in practical commercial applications. Modern Lisp is a highly interactive language that incorporates powerful editing and debugging tools. It allows a programmer to address many types of large and complex problems more efficiently, and even some problems that are imprac-

tical to solve using conventional computer languages.

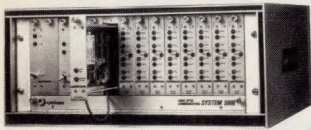
Recently, a number of companies formed by scientists who were originally doing work in theoretical AI have announced products that have Lisp as the core of their knowledge-based systems. Among these are Symbolics, Inc (Cambridge, Mass), LISP Machine Inc (Culver City, Calif), Xerox, Special Information Systems (Pasadena, Calif), General Electric Co (Schenectady, NY), Inference Corp (Culver City, Calif), Teknowledge (Palo Alto, Calif), and Intelligentics (Palo Alto, Calif). In addition to these companies, many large firms have internal programs in AI research that have resulted in expert systems for internal use. Digital Equipment Corp (Maynard, Mass) for example, has developed a

*(continued on page 34)*



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CIRCLE 20

## SYSTEM TECHNOLOGY/SOFTWARE

### Artificial intelligence

(continued from page 33)

number of expert systems that help configure and customize orders for a particular DEC computer system. The company expects to offer some kind of expert system on the market in the future. Schlumberger/Fairchild Mountain View, Calif has also built an expert system for internal use to analyze oil well logs-and mineral exploration. Both the DEC and Schlumberger systems are Lisp based (see special edition on *Office Systems Design*, Fall 1983, p 37).

### Direct programming in Lisp

As might be expected, describing lists and procedures can be a time-consuming chore for the programmer if done in the machine's assembly language. LISP Machine's Lambda computer has made that chore easier by having the programmer utilize the machine's microcompiler and virtual memory to microprogram directly in Lisp. The Lambda is built around a 32-bit Nubus architecture with a 37.5M-byte/s transfer rate that was developed at Massachusetts Institute of Technology's computer science laboratory. This architecture allows use of a variety of processors, memory, I/O devices, and other devices since the system diagnostic unit senses what kind of devices are installed and then conforms system operation accordingly. The machine's 4-board Lisp processor has a 24-bit virtual address space and a 4K cache.

Basic system software includes 10,000 compiled functions and over 30,000 symbols representing an initial core image of about 4 million words. Approximately 200 microcoded functions reside in 10K of user-writable control memory for output to a high resolution display (800 x 1024 pixels) that is refreshed at 60 times/s. A window capability is also built in to maintain an editing and execution environment side by side. The operator can choose from any of the standard features available within the window system or add new ones. The editing function is performed using the Zmacs editor. Zmacs accepts over 400 commands in addition to allowing users to construct their own. As an example of how easy it is to use this editor, if users choose the

APROPOS command, they have at their disposal all commands for those containing relevant key words. Thus, APROPOS FONT will generate all appropriate commands containing the work font for the user.

The Lambda also features a 16 x 16 matrix multiplier, a 256K x 32-bit error-correcting physical memory, a 470M-byte Winchester disk drive with a storage module drive controller capable of handling four drives, display, keyboard, and a 3-button mouse, all for \$72,000.

LISP Machine Inc was founded, among other entrepreneurs, by the principals of Inference Corp to allow Inference to obtain Lisp machines for its AI development projects. One of Inference's products is a symbolic manipulation program (SMP), a productivity enhancing tool used to manipulate algebraic and other symbolic mathematical expressions. SMP can perform mathematics symbolically at different levels, from high school algebra to advanced theoretical physics. The manipulation of mathematical formulations is done automatically and interactively. SMP can differentiate and integrate most mathematical expressions, solve linear and nonlinear equations, and perform matrix and tensor algebra. Mathematical expressions can be evaluated numerically, or they can be expressed graphically in two or three dimensions.

This particular program has not been written in Lisp, but rather in the C programming language. It is thereby ready for sale to the C-based end user and can be used on a variety of different computers. Currently, SMP runs on the VAX computer both under the Unix and VMS operating systems. Inference offers the program at a cost of \$36,000 for permanent license on VAX-11/780 installations.

Inference sells inference engines—not complete expert systems. Its latest product is an inference engine called the advanced reasoning tool (ART). Coupled to any of a number of knowledge bases, ART becomes the engine that infers conclusions in the expert system. The system is basically

(continued on page 36)

# NS16000

## The World's Most Elegant Microprocessor Family will turn "Cartwheels" on your VAX-11.

More and more programmers and systems designers are coming to the conclusion that the NS16000™ microprocessor family will be the foundation for the next generation of high-performance, low-cost computers. Why? Because it features a totally new, totally practical, highly symmetrical architecture; high-level language and modular-software support; a powerful instruction set; and the implementation of Demand Paged Virtual Memory.

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**Once your programs are compiled, you'll want to download them to our DB16000 evaluation board for execution and debugging.**

The DB16000 is a complete microcomputer system comprising the NS16032 CPU, the NS16201 Timing Control Unit, sockets for our Memory Management Unit, Floating Point Unit, and Interrupt Control Unit, 128K bytes of on-board RAM, a wide range of both standard and optional I/O interface devices, and a monitor program in PROM. To facilitate the development of efficient software, either of our cross-software packages communicates with the monitor program (via a serial link), allowing you to down-load, execute, and debug your programs in the DB16000's native environment.

**Finally, for seamless integration of your software and NS16000-based hardware application, you'll want our ISE/16, a powerful in-system emulator.**

Our easy-to-work-with ISE/16™ allows real-time emulation of the NS16000 chips, for testing and debugging hardware and software in your own hardware environment. This ISE—which includes the NS16032 CPU, the NS16082 MMU, and the NS16201 TCU, and 30K bytes of mapping RAM—plugs directly into your target system, requiring no target-system modification. (\$9,450.00)

**Today, the NS16000 family—and it alone—can enable you to put large-computer-like products on the market at microprocessor prices: from elegant personal and business computers to graphic workstations to industrial control systems.**

This elegance, we believe, will breed success—which might make you want to turn one or two cartwheels yourself.

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**Artificial intelligence***(continued from page 34)*

generic and can perform reasoning tasks that are needed for any number of applications. The company is actively pursuing joint venture partners to develop expert systems in software engineering, applied sciences, manufacturing, and the financial industry.

A very specific expert system has been developed by General Electric's Research and Development Labs. CATS-1 is a locomotive troubleshooting system whose knowledge base is embedded with the expertise of the company's top locomotive field service engineer. In operation, the user asks questions concerning the malfunction displayed onscreen (see Figure). The user can also call detailed drawings of various components at any time during the question and answer session. The expert system reaches conclusions about the malfunction by searching deeper into the layers of the locomotive's mechanism. Repair procedures for that malfunction are also displayed onscreen. The CATS-1 program evolved from the more basic GEN-X development efforts at GE. This project is an effort to develop a generic expert system that could streamline the development of specific expert systems such as CATS-1.

A similar course of action is being followed by Teknowledge Inc. The company is pursuing knowledge engineering—the engineering discipline that formalizes knowledge in expert systems. The company designs and supports commercial knowledge-based expert systems for industrial clients. Founded in 1981 by computer scientists from MIT, Stanford University, and the Rand Corp, the company will introduce its first commercial product early in 1984. It will be the first in a series of tools that will enable organizations to implement their own practical, large size, knowledge-based systems. Teknowledge's System 1 will be an integrated package of software and services for the development of such systems. It is intended for developing consultation systems that solve problems requiring complex symbolic inference or judgment. Applications include diagnosis, recommendation, classification, and

global planning. An underlying rule-based structure is integrated with an Algol-like language for controlling the consultation. Using Algol will augment the need for proficiency in a symbolic programming language, says Teknowledge.

**Bell's ACE repairs cables**

A completely different approach to expert systems has been demonstrated by Bell Labs. Its automated cable expertise (ACE) is an expert system for troubleshooting telephone cable faults. ACE uses a conventional data management system for its knowledge base. The primary sources of knowledge are the users' database system and primers on maintenance analysis strategies. Thus, ACE differs from other expert systems in two ways: it manipulates a massive amount of data, in addition to its problem-solving rules. Also, rather than being a computerized consultant that is called upon on an as needed basis, Bell Lab scientists claim that ACE is a self-motivating analysis system with ongoing responsibility. The expert system digests hundreds of telephone cable maintenance reports daily from data provided by a data management and report generation system. ACE uses this knowledge to provide "bottom line" information and recommendations

concerning trouble spots to telephone engineers. Prior to ACE, telephone workers were at a loss to keep up with the online reporting system since interpretation and decisions were still left to them.

Now, ACE provides not only reports, but also suggests the proper procedure to immediately resolve the problem. In determining the proper decision, the system itself poses as the user and queries the data base. The expert system therefore not only answers the questions, but also poses them. ACE is Lisp-based and runs on the VAX-11/780. Support routines for ACE include interfaces written in Unix. The system is initiated nightly to study transactions, and reports them on an interface terminal's electronic message board. A typical production rule by which ACE lives might be translated into English in this way: IF a range of pairs within a cable have generated a large number of customer reports, AND IF a majority of work on those pairs was done in the terminal block, THEN look for a common address for those repairs. A total of 100 production and 50 related condition and action functions are contained in ACE's knowledge base to make up the set of related rules that collectively do the analysis.

—Nic Mokhoff, Senior Editor

**DATA COMMUNICATIONS****Workstation analyzes and simulates LANS**

Controlling and debugging an Ethernet network is a demanding task. With several stations on the net, each passing traffic at 10M bps and fighting for access, identifying problems can be extremely difficult. Testing a network under load requires the ability to generate real messages, not just bit streams.

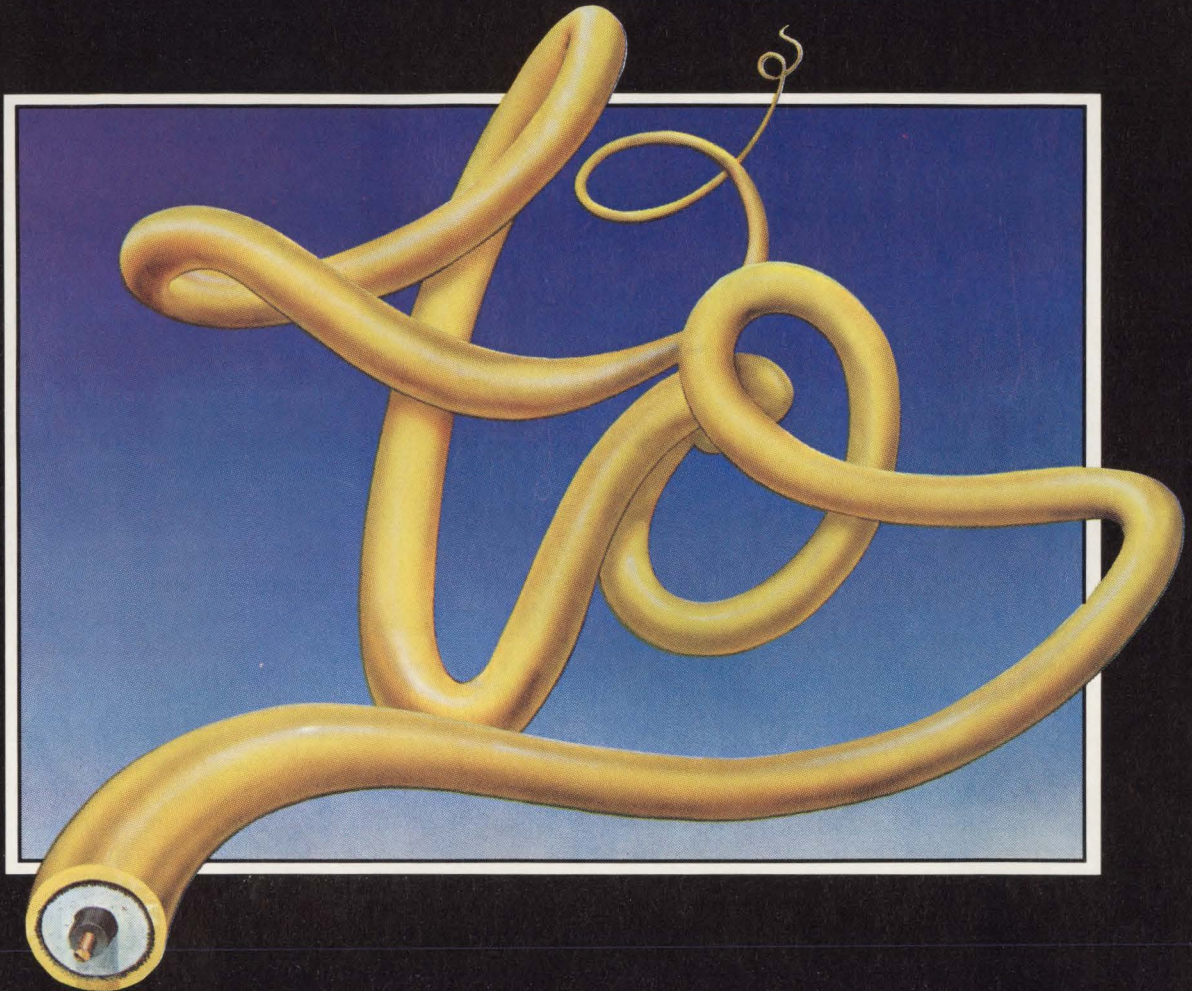
The Nutcracker, a local area network (LAN) analyzer/simulator from Excelan addresses just these problems. The unit is a standalone Multibus-based workstation, whose 8086 CPU controls multiple state machines to monitor every packet

passed on the net. Pattern recognition software allows inspection of both valid and aborted packets, monitoring of individual stations or groups of stations, transmission of any number of data packets at any rate required, and generation of statistics and reports on net activity.

Hardware debugging, from the chip level to complete net stations, is an obvious application. With a known good node, marginal or faulty node identification becomes much easier. Software algorithms that implement the higher levels of the

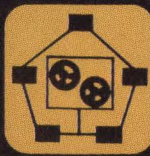
*(continued on page 38)*

# IBM



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and other local area networks



AUSCOM introduces the proven solution for connecting your IBM mainframes to Local Area Networks. Using the 8911 Programmable IBM Channel Interface, AUSCOM can connect your network directly to the channel and, through software, provide the necessary drivers to incorporate the LAN protocol of your choice. You select the LAN; AUSCOM will make the connection to your IBM!

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## Workstation analyzes LANs (continued from page 36)



**Excelan's Nutcracker is a standalone workstation for controlling and monitoring Ethernets. With its combination of high speed TTL hardware and object-oriented software a net manager can monitor and control traffic, as well as identify problems.**

International Standards Organization protocol have not been standardized, and the Nutcracker will allow them to be debugged and optimized in a realistic environment.

Full characterization of a large system before it is installed will make performance guarantees possible, and allow the prospective purchaser to make rational decisions about combinations and types of nodes necessary for a given application. The unit will also help meet government requirements for performance documentation, and speed the acceptance of LAN technology by giving purchasers confidence that a system will perform as advertised.

Nutcracker hardware is contained in a desk-sized unit, with a 12" CRT screen, detachable keyboard, a 20M-byte Winchester disk, and a 600K-byte floppy. Internally, an 8086 CPU card and 896K bytes of parity-checked RAM contain the system software, while several high speed TTL state machines handle the signal processing tasks involved in monitoring traffic in real time.

Object-oriented multiprocessing software provides a menu-driven user interface for controlling the

system, as well as the ability to generate "canned" programs—standard routines for repetitive tests. The system is thus easy to use on two levels: inexperienced users can walk through the menus to exercise the system functions, while experienced users can move quickly to needed functions.

### Software subsystems

The Acceptor uses the hardware state machines to capture both good and bad packets from the bus in real time. This way, even partial packets that have been part of a collision between two stations trying to send traffic at the same time can be examined. The Acceptor contains "filter" routines that examine packet headers (address and routing information), and can select packets to be examined on the basis of any bit pattern, up to 128 bytes long.

The Tracer selects packets captured by the Acceptor, and prepares them for further processing. It acts as a trigger, initiating storage or further processing the selected packets.

The Injector is a traffic generator. It builds packets with any required

header structure, in effect mimicking any possible Ethernet transmitter. Both good and bad packets can be constructed—packets with cyclic redundancy check errors, alignment errors, etc, are useful for testing the response of the net. The packets can then be injected onto the Ethernet cable, either politely—using the CSMA/CD protocol to avoid collisions—or impolitely, deliberately causing collisions to test how stations on the net react. In addition, it can embed time-stamps in the transmitted packets, so that performance measurements of traffic to and from nodes can be made.

The Statistician collects and processes data about the packet traffic observed on the net. It maintains counts of how many packets are transmitted, and their lengths, measures interpacket spacing (which indicates how large message buffers need to be), plots frequency distributions, and prepares graphs, tables and histograms for human analysis. Statistician reports can be used to characterize the entire net, or fine-tune the performance of a particular node or node set.

The Nutcracker is priced at \$49,500. Shipment of evaluation units to selected sites began in September, and delivery of production models is expected this month. **Excelan, Inc.**, 2030 Fortune Dr, San Jose, CA 95131.

—Sam Bassett, Field Editor

Circle 240

**SYSTEM TECHNOLOGY**  
(continued on page 47)

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# THERE ARE AT LEAST EIGHT MORE TERMINALS HIDING IN YOUR VAX.

All you need is one Able VMZ/32 asynchronous terminal controller to find 8 more lines in your DEC VAX-11/730, /750 or /780, for a total of 16. With an additional VMZ/32 you can discover 16 more lines.

The VMZ/32 board plugs into the same space as the standard DEC DMF32 board it replaces, providing 16 lines instead of 8. Without patches to the VMS. And with complete VMS compatibility.

Immediately you'll unleash a minimum 13% increase in processing speed. You'll instantly realize a 50% reduction in costs per line, obtain a 50% space savings in the backplane and see a surprising reduction in power consumption.

The VMZ/32 also reveals hidden performance within your CPU by increasing its availability (idle time) up to 500%.

To handle this newly acquired power, the VMZ/32

gives you modem control on all sixteen lines. This lets you easily manage the terminals, including those remotely located. Plus, you can easily vary the speed on each line from a 50 to a 19.2K baud rate, including split baud capability.

Here's a dependability clue: an MTBF of over 100,000 hours. To back it up, the VMZ/32 comes with a one-year warranty from Able that can be extended if you like. Ask your Able representative for full details.

If you do unearth a problem, Able Support Service is as close as the phone.

You can also uncover extra performance hidden in your printer with Able's VMZ/LP. The VMZ/LP provides a dramatic reduction in CPU overhead and is LPI1 cable compatible.

So, to discover the full potential hiding in your VAX, Able's got a simple solution: just plug in the VMZ/32.

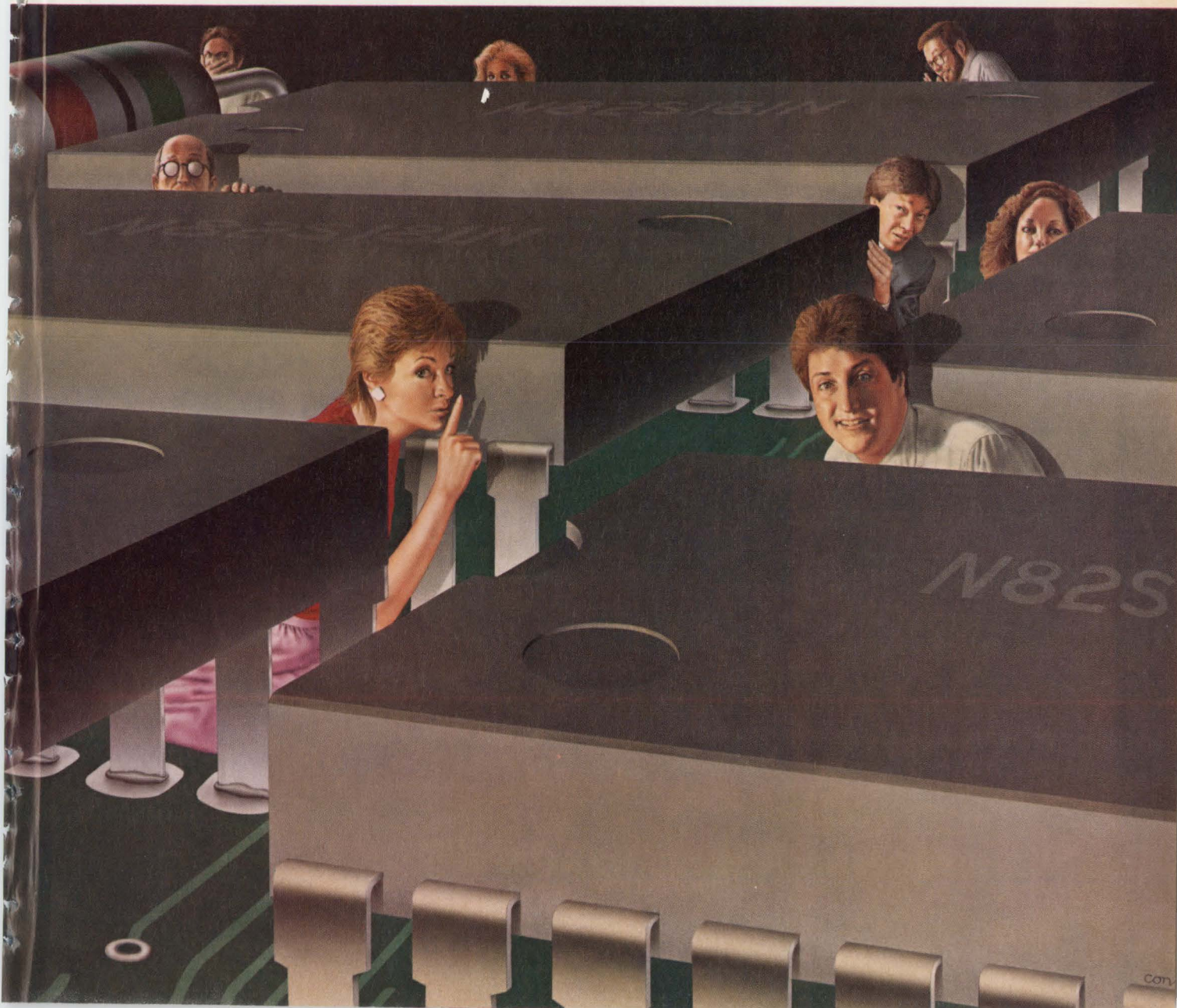


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**CIRCLE 23**

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# Floating Point Systems array processor to break

## The FPS-5000 Series from Floating Point Systems

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words is available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the

Typical performance examples of geophysical, medical imaging and signal/image processing applications.

Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation/Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 msec.

Based upon specifications subject to change.

FPS-5000 Series sets a new standard for cost-effective computing, breaking the \$2,000 per MFLOP\* barrier—the first time this has been achieved in any floating-point computing system.

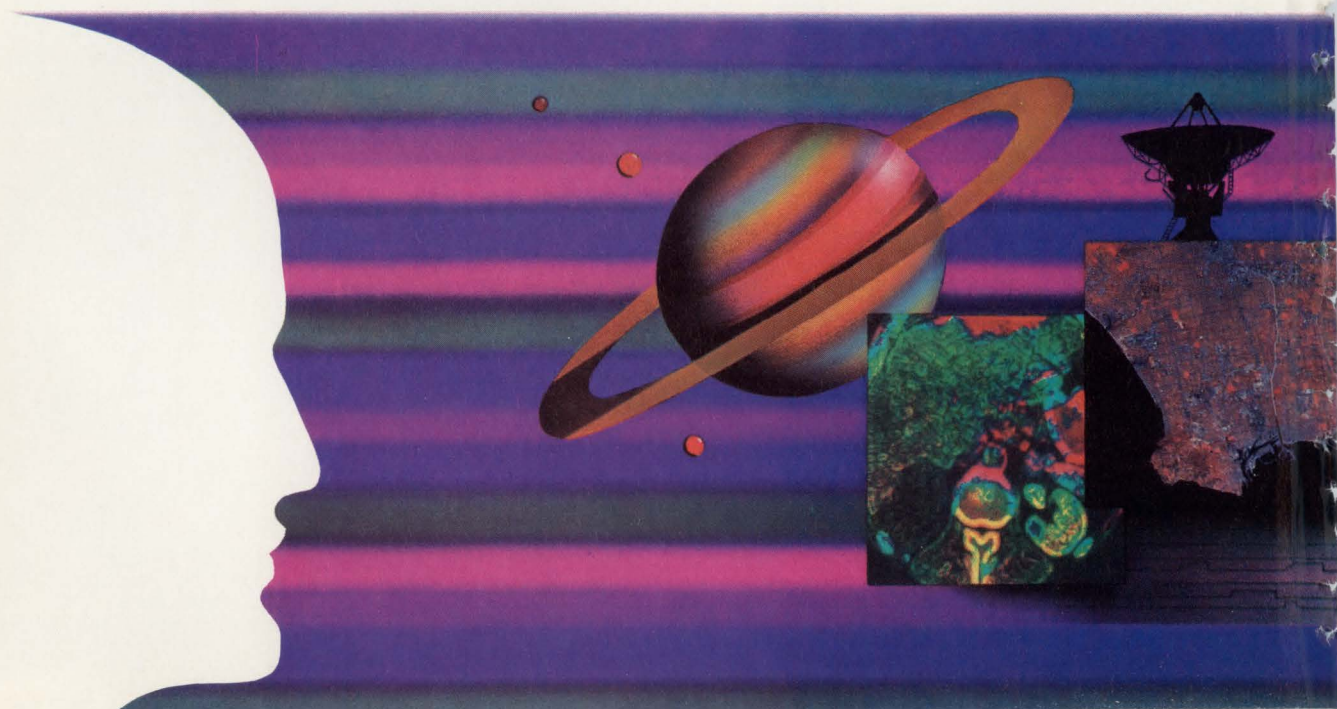
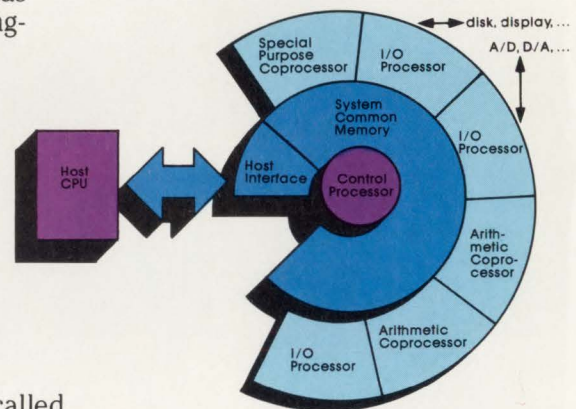
\*Based on U.S. Domestic Prices

## Distributed processing architecture

The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called

Arithmetic Coprocessors. Data flow is simultaneously managed

## FPS-5000 Series Architecture



# introduces the first the \$2,000/MFLOP barrier.

by a combination of independent I/O Processors and the central Control Processor.

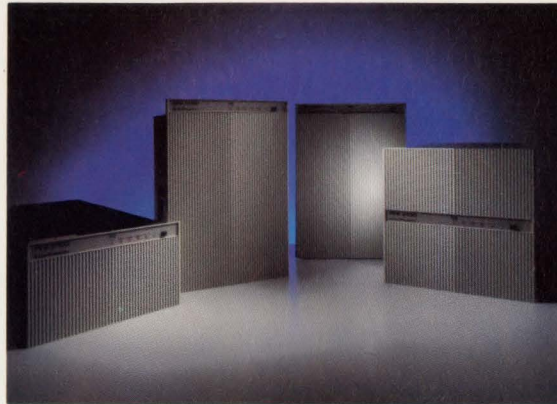
Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

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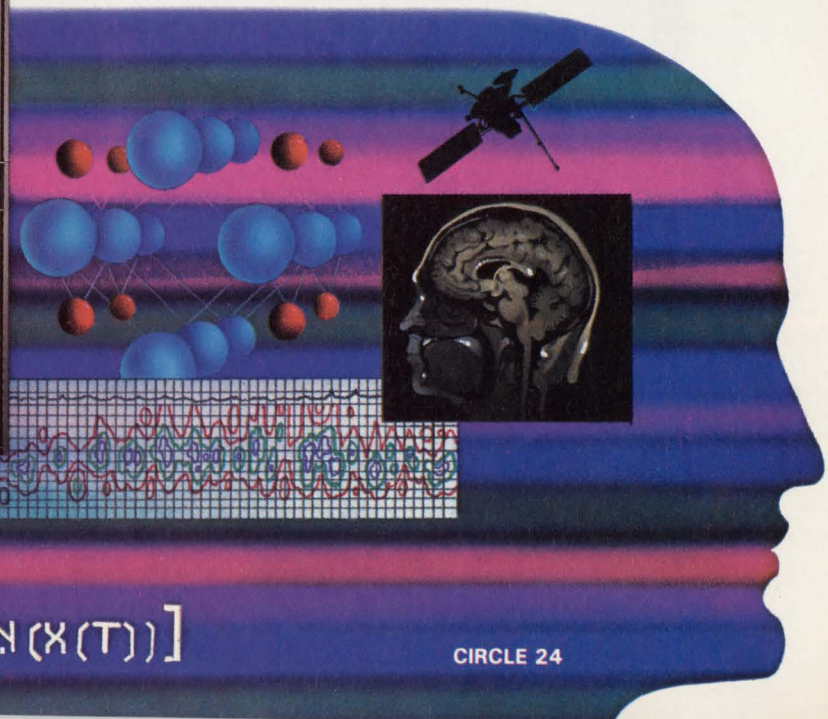
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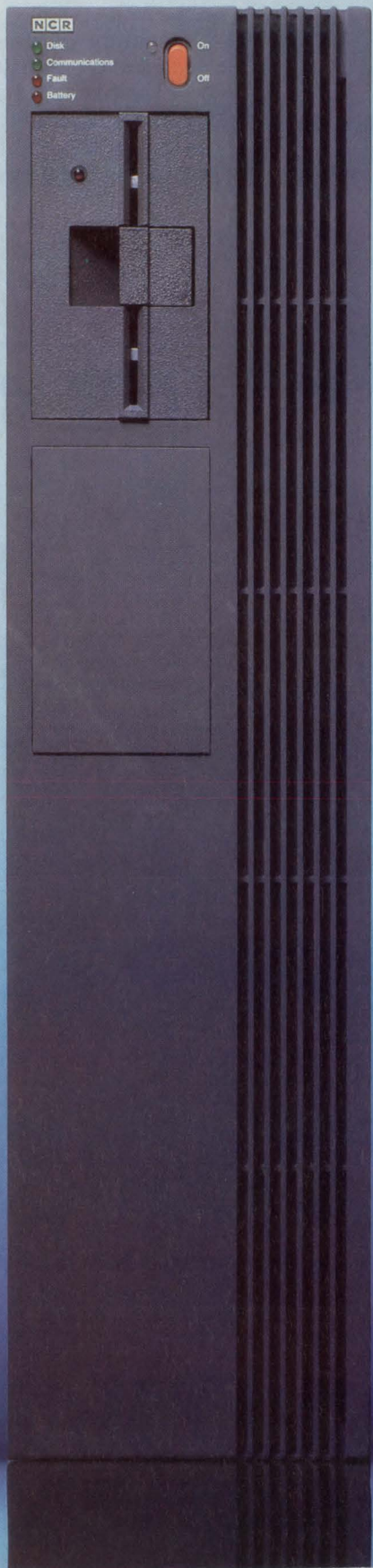
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CIRCLE 24



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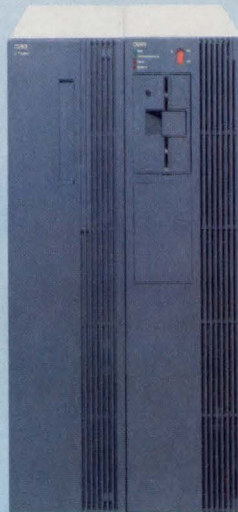
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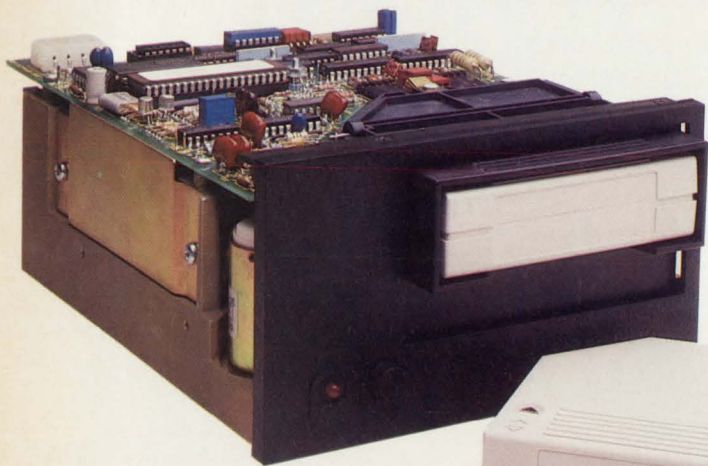
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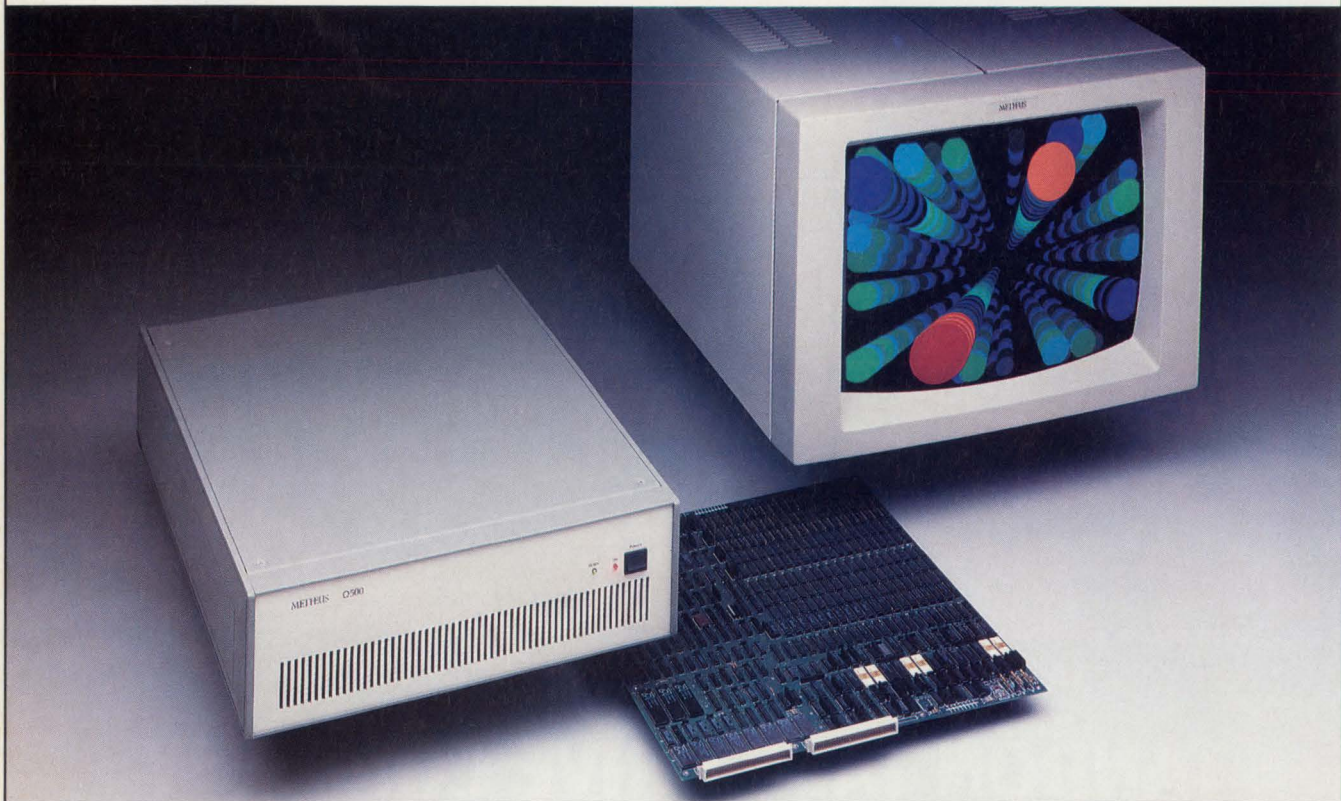
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## Software puts Unix micros on the network

Distributed processing—the ability to access data and programs on non-local machines—has been on wish lists for 25 years or more. Microcomputer systems have grown in power, and experience with distributed processing has accumulated to the point where commercial software for microprocessors has begun to appear.

Two examples have recently been announced, both of which implement a distributed Unix. One of these, Excelan's (San Jose, Calif) Transmission Control Protocol/Internet Protocol (TCP/IP) package, implements the Advanced Research Projects Agency network (ARPANET) protocols. The other, Altos Computer's (San Jose, Calif) Altos-Net II, provides both Ethernet and proprietary interfaces. Users of ARPANET have had this ability for several years, as have researchers in selected academic settings. These implementations have typically involved mainframes and large minicomputers, together with specialized communications hardware.

Both the individual user and the manager who must justify the purchase of computer equipment derive great benefits from distributed processing. Unlike some situations, though, the benefits are complementary, and not antagonistic. The user's machine, in effect, expands and becomes more powerful. Specialized database searches, for example, can be offloaded to a mini or mainframe whose hardware and software are optimized for that work; heavy number crunching can be offloaded to an array processor; printing, plotting, and typesetting can become remote and automatic.

Distributed processing lets the manager buy only as much equipment as is needed for a given application, and still keep users happy. Multi-user microcomputers are cheap when compared to the hardware and software costs of hanging several more terminals on an IBM mainframe or a VAX. The microcomputers provide quick response time, and a reasonable amount of local storage. Offloading the user interface to a micro speeds up the mainframe too, since communication overhead in-

volved in handling terminals disappears. Important corporate files can be kept (and controlled) in one place, and not spread in pieces over a large number of machines.

System integration likewise becomes easier—microcomputer oper-

ating systems are simple compared with IBM's OS 360/370, or VMS for the VAX. Each system piece can handle a few functions well, instead of trying to oversee the entire system performance. Hardware modularity is  
*(continued on page 49)*

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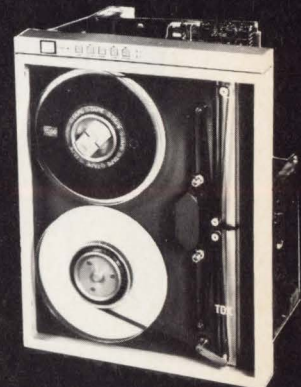
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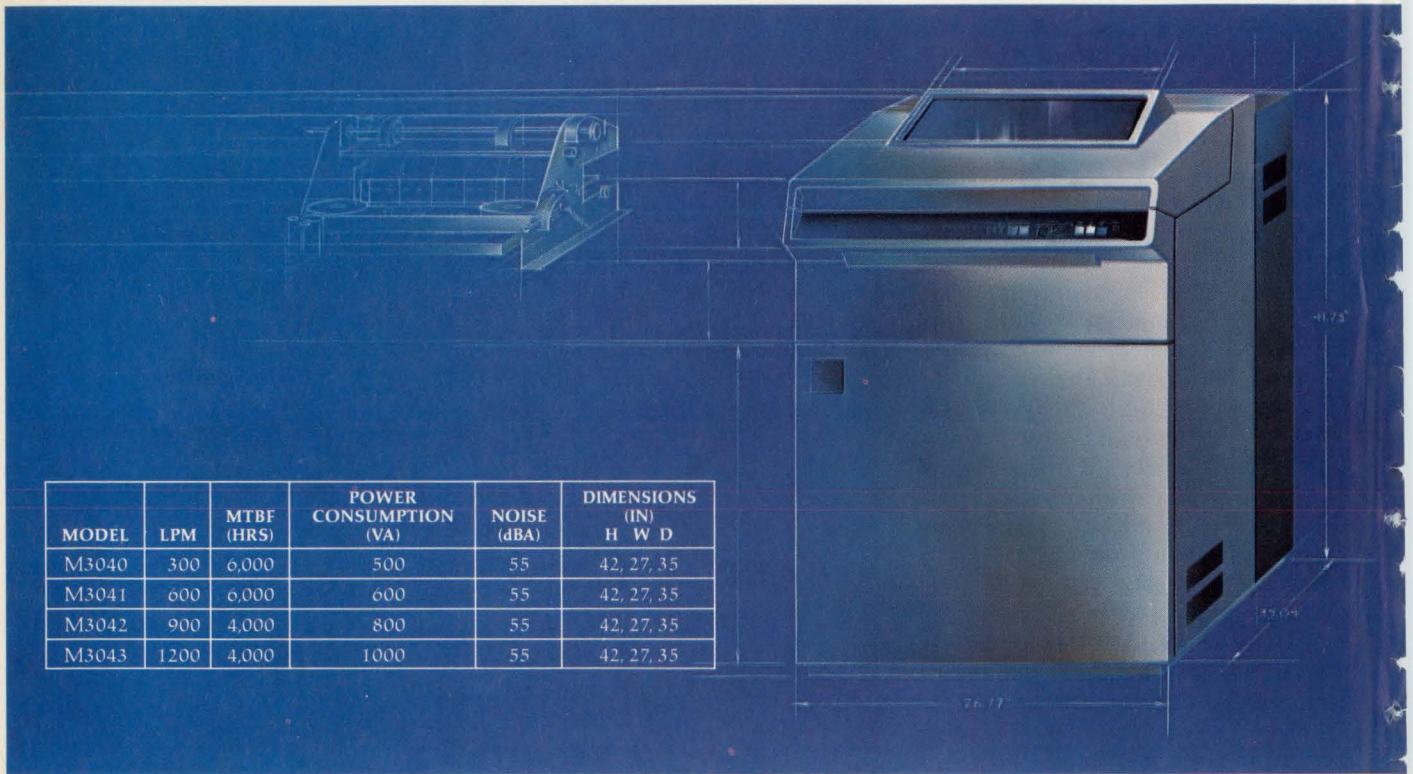
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## Unix micros

(continued from page 47)

an obvious and attractive complement to modular programming. In both cases, the object is to break up large systems into chunks which are small enough for one person to understand, and fix.

## Unix on the Ethernet

Excelan's TCP/IP package for Ethernet systems uses their Exos/101 frontend processor (see *Computer Design*, Apr 5, 1983, p 34), now called the Excelan/101. The 2-part package implements the ARPANET protocols for transferring data and programs between machines.

The first part of the package, written in machine language, resides in the Excelan/101, consists of 40K bytes of code and 20K bytes of buffers, and acts as the software driver for the hardware Ethernet interface on the board. The TCP/IP interface is independent of the host operating system—all that is necessary is to

load a buffer with the data to be transmitted and some statistics, then signal the Excelan/101 to begin transmission. Similarly, on receipt of data, the package interrupts the host and passes a pointer to the buffer where the incoming data reside.

A Unix system networking kit that runs on the host computer is the second part of the package. It is written in C, with system calls for the Berkeley 4.2 version of Unix. It also includes a small software driver to talk to the TCP/IP interface, which must be resident in the host at all times, and five transient network application packages.

The first is an ARPANET protocol formatter, which handles all the details of assembling data packets for transmission and attaching headers and error correcting codes as required by the TCP/IP protocol. Second is a Berkeley remote copy utility, which is a fast routine for copying files be-

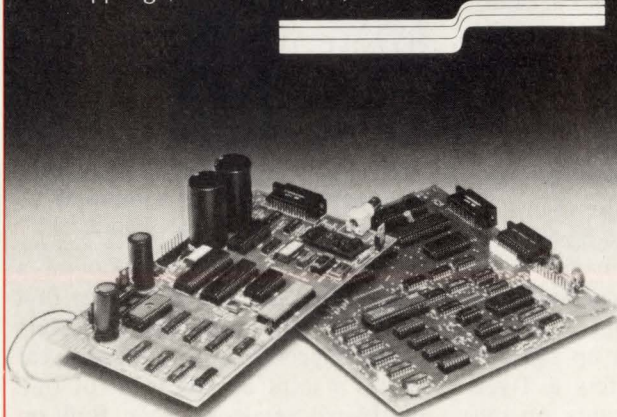
tween systems. The third transient network application package is the Berkeley remote shell utility, which lets a user "see" what files and programs are available on other machines in the net, as well as access or run them. Next is the Berkeley remote login that lets one system operate as a virtual terminal on other systems. Finally, there is the Berkeley Email utility that establishes "mailboxes" and handles electronic mail and conferencing.

The TCP/IP package is compatible with all Berkeley 4.2 Unix, as well as Xenix from Microsoft (Bellevue, Wash), and ports of Unix to the 68000 by Unisoft (Berkeley, Calif). It is supplied on either 9-track, 1600-bpi magnetic tape or 8" single-sided, single-density floppy disks.

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(continued on page 50)

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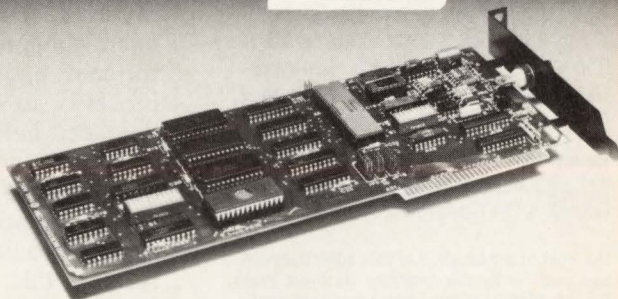


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## Unix micros

(continued from page 49)

for quantities over 1000. Included are the source code for the Unix utilities, as well as reproduction rights for them and the TCP/IP software. Source code for the TCP/IP interface costs an additional \$20,000.

A development license costs \$2000 (applicable towards purchase of the production license), includes source code, and the right to make three copies of the package for testing purposes. Additional copies can be made for \$1000 each, not applicable to the price of the production license.

## Xenix on Altos-Net

Altos-Net II software provides distributed processing, both via an Ethernet interface, and via the Altos proprietary twisted-pair network scheme. The software provides essentially the same capabilities as the Excelan scheme, but structures the interface differently.

A new directory is introduced at the top level of the tree-structured

Xenix file system. Called the "@@" (pronounced "at") directory, it contains the root directories for all machines on the network. The normal way to invoke programs in a single-machine Unix system is to enter a file specification: {Directory Name}/{Subdirectory Name}/.../{Program Name}. To invoke a program under the Altos-Net II system, the user would enter: @/{Machine Name}/{Directory Name}/... etc.

Protocol drivers that invoke hardware drivers within the host operating system handle the transfer of command strings and data files. As such, it is transparent to the user or application programs written for the system.

Altos-Net II software is currently available and costs \$495 per CPU, with multiple-CPU discounts also available. Upgrades for the company's previous networking release, Altos-Net I, are \$100.

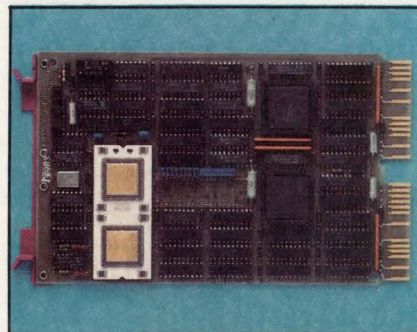
—Sam Bassett, Field Editor

## MICROPROCESSORS/MICROCOMPUTERS

### DEC counterattacks with advanced Q-bus boards

Nontraditional suppliers offering advanced systems based on sophisticated 68000/Multibus/Unix or other combinations, make LSI-11/Q-bus products seem outclassed and outdated. A range of advanced products now on the way from Digital Equipment Corp should change that impression. The first of these, billed as a "new generation of Q-bus products," includes a board-level microcomputer with PDP-11/70 performance and a high speed peripheral processor to offload the Q-bus, an upgraded Falcon single-board computer, and an extension of Micro-power/Pascal that runs under VMS or RSX-11 operating systems in a multi-user environment. To up the ante further, DEC now offers a 1-year return-to-factory warranty on CPU board-level products—an industry first that smaller competitors may have a hard time duplicating.

For computation intensive applications, the most important of these



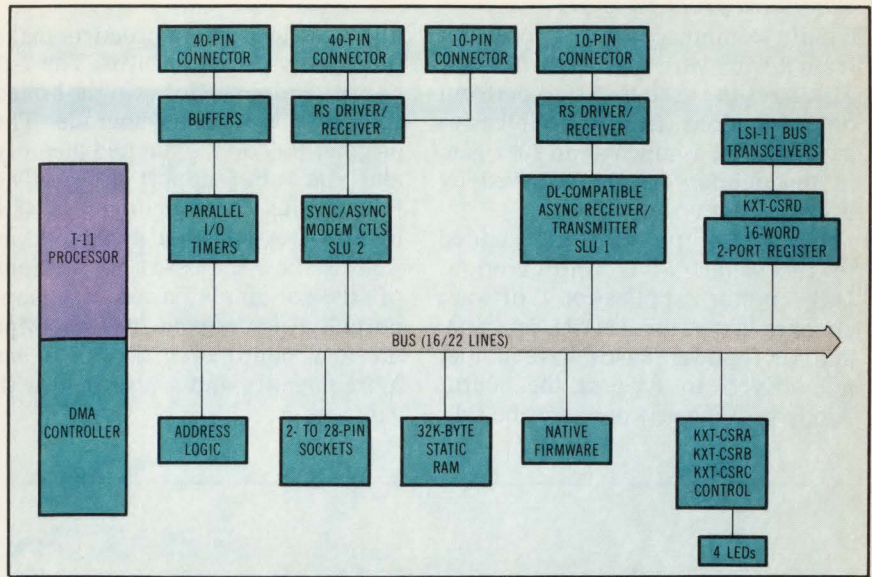
The LSI-11/73, using the J-11 processor chip, puts the power of a PDP-11/70 minicomputer on a single board.

Q-bus products is the 11/70 on a board, the LSI-11/73. This is the first product built around the 20-MHz J-11 microprocessor introduced a year ago as a joint development of DEC and Harris Semiconductor. Built on the same dual-height size module as an -11/23, but with four times the power, it finally gives DEC something to counter the inroads of MC68000-based microcomputers. The J-11

microprocessor engine for the -11/73, like the 68000, uses 32-bit internal and 16-bit external data paths. But it has onboard floating point hardware while users are still waiting for Motorola's floating point coprocessor. The J-11 also has onchip a 4-level pipelined architecture, cache support, and memory management implemented in VLSI CMOS.

The LSI-11/73 is a powerful microcomputer with memory addresses extended to 22 bits (4M bytes), 46 FP-11 single- and double-precision hardware floating point instructions, PDP-11/70 system registers, 8K-byte cache, and Q-bus interface. All PDP-11 operating systems can be run on the LSI-11/73 and, for the first time, Unix is sold and supported by DEC.

Like other microprocessor buses, the Q-bus can get overwhelmed by I/O intensive applications. To increase throughput in such cases, the KXT 11-C peripheral processor was



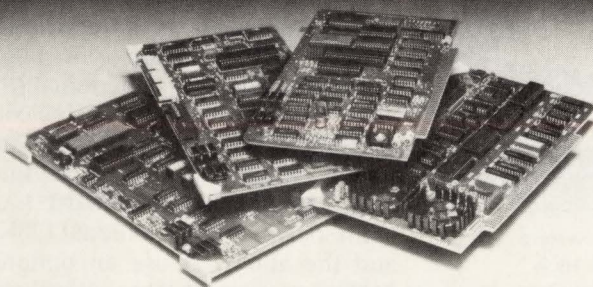
The KXT 11-C peripheral processor is an intelligent communications controller which offloads the Q-bus, freeing the CPU for other functions.

developed. This single-board computer is based on the T-11 microprocessor and functions as an intelligent controller. With synchronous and

asynchronous interfaces, parallel interface and a 2-channel DMA controller, the KXT 11-C is optimized to  
*(continued on page 52)*

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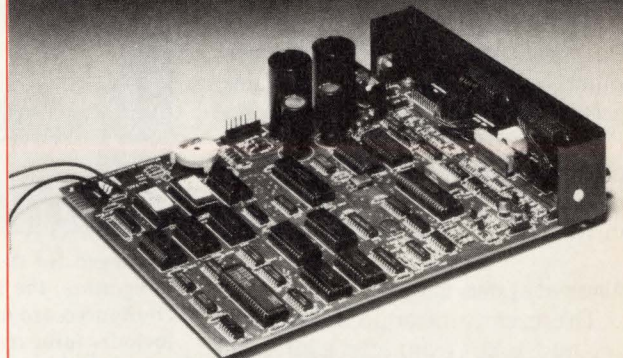


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## Q-bus boards advance

(continued from page 51)

handle communications processing from a wide variety of DMA devices. This frees the arbiter CPU to perform other functions. In very I/O intensive applications, as much as an 80% gain in throughput can be achieved by using the KXT 11-C.

Up to 14 of the units can be added to the same Q-bus configuration. Only minor application software changes are needed. RT-11, RSX-11M, and Micropower/Pascal have utilities and drivers to support the board. Along with the new processor boards,

upgrades to existing products make them more useful to OEMs. The T-11 based Falcon-Plus single-board computer is such an upgrade. The original Falcon had limited memory and did not support RT-11. The Falcon-Plus can support up to 48K bytes of RAM so that RAM-based as well as the ROM-based applications of the original Falcon are supported. Price remains the same for the new board even though it has more memory and is now built with gate arrays.

Micropower/Pascal (*Computer Design*, April 5, 1983, p 119) has also been extended. As a combined operating system and high level language, Micropower/Pascal can develop dedicated applications that are implemented under RSX-11M, RSX-11M Plus, and VMS. This software was previously available only on RT-11 based systems. **Digital Equipment Corp, OEM Group**, 77 Reed Rd, Hudson, MA 01749.

—John Bond, Senior Editor  
Circle 241

## Advanced microprocessors spark next generation PCs

As speed becomes an issue in the microcomputer field, advanced microprocessors are stealing the limelight from their still young competitors. Taking over are Intel's 80186 and 80286. The Intel 8088, while supplying more speed and a larger address space than the 6502 and Z80, is being pushed aside because of its 8-bit data bus, as is the 8086 with its 16-bit data bus. Pipelining and onchip memory management combine with two to five times better throughput and reduced parts count to give the newer parts the edge.

While no major manufacturer has publicly committed to either chip, both Intel's OEM Systems Div and Wyse Technology have introduced systems using them. Manufacturers of add-on boards for the IBM PC, such as AST Research (Irvine, Calif) are hinting that they will soon have products on the market, probably introducing them at the Comdex show in Las Vegas this month. There has been much speculation that the next generation of PC products from IBM (Boca Raton, Fla) will use one or the other chip, but confirmation will have to wait until the units are actually introduced.

### Aimed at system integrators

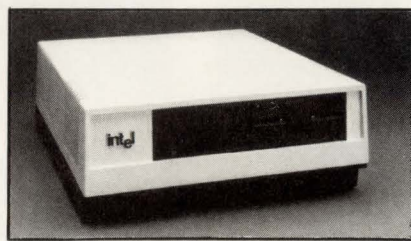
The recently introduced 286/310 and 286/380 systems from Intel address the technical and OEM market. Spokesmen are adamant that they are not in the retail or end-user market, but



**The WY-1000 is a microcomputer module that utilizes an 80186 16-bit microprocessor. The system includes a WY-1000 microcomputer, WY-50 alphanumeric terminal with 14" 132-column display, two 5 1/4" floppies, and three RS-232-C ports.**

rather are aiming their products at system integrators.

Both systems are based on the Multibus, and include the CPU, a Winchester drive, a floppy disk drive, two RS-232 serial ports, and a



**Packaged for OEMs and system integrators, the Intel 286/310 is configured around an 80286 CPU, includes industry standard 5 1/4" Winchester and floppy disks, and provides four free Multibus slots for additional functions.**

Centronics-compatible parallel port. The 286/310 has four free slots, a 10M-byte 5 1/4" Winchester, and a 320K-byte floppy. The 286/380 has eleven free slots, a 35M-byte Winchester, and a 1M-byte floppy.

Two operating systems are offered: Intel's proprietary iRMX 286R realtime operating system with an assembler, Fortran, C, Basic, Cobol, Pascal, and PL/M; and Microsoft's (Bellevue, Wash) Xenix 286 implementation of Unix, with Cobol and C.

The 286/310 will be available in December, and will cost \$9900 with 512K bytes of ECC RAM. Either Xenix 286 or iRMX 286R is an additional \$2000. The 286/380 will be available this month, and is priced at \$29,860. OEM discounts are available for volume purchases.

### Moving up from terminals

Previously known for their line of monochrome and color terminals, Wyse Technology is introducing a desktop computer sized to fit snugly under a low cost smart terminal (the WY-50) that they are introducing concurrently. The WY-1000 is a single-board computer with an 8-MHz Intel 80186 CPU, 128K of onboard RAM (with sockets for an additional 128K), and the ability to use an optional 512K memory card. The unit includes as standard two 5 1/4" IBM PC type floppy disks, with an option to replace one floppy with a 5 1/4"

(continued on page 54)

# Lundy computer graphics maintenance always generates a very reassuring picture for you and your company.

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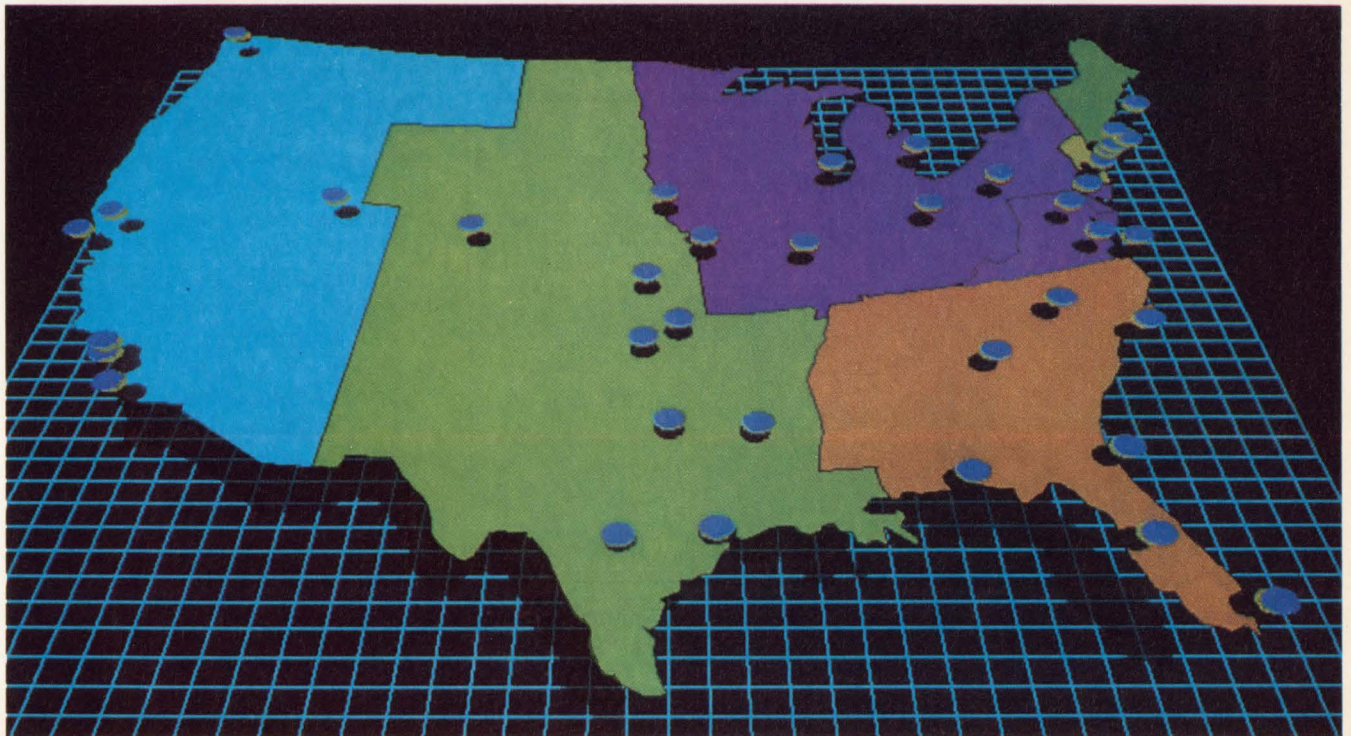
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# LUNDY

*The Lundy service map was generated on a Lundy T5688 raster terminal. Both Lundy products and Lundy service set industry standards.*



## Advanced microprocessor (continued from page 52)

Winchester. Processing speed on the company's demonstration unit is noticeably faster than that of a PC.

An intriguing hardware option is a graphics board which communicates via unused lines in the RS-232 interface with either the WY-50 or the WY-300 graphics terminal to overlay graphics on the alphanumeric display. The horizontal and vertical sync signals, as well as the bit rate clock, are captured from the terminal, and the graphics display (800 x 338 pixels in

monochrome, and 800 x 286 in color) is then transmitted to the terminal for display. Sixteen colors can be displayed simultaneously, and the Digital Research Inc (Pacific Grove, Calif) GSX graphics package provides software support.

The unit is offered with either Digital Research's Concurrent CP/M-86, or Microsoft's MS-DOS. A wide range of languages and programming tools are available for each operating system.

The complete system—terminal, computer module with two floppies, and 128K of RAM—will be available late this month through OEMs and distributors at a list price of \$2495. **Intel Corp, Integrated Systems Operation**, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123. **Wyse Technology**, 3040 N First St, San Jose, CA 95134.

—Sam Bassett, Field Editor

## MEMORY SYSTEMS

### Hardware disk cache boosts online performance

A movement toward disk system cache memory, becoming more apparent in the minicomputer arena, promises to raise performance in I/O-intensive applications. Supermini manufacturer Gould/SEL (Fort Lauderdale, Fla), the first minicomputer manufacturer to endorse the technique, puts a hardware-based disk

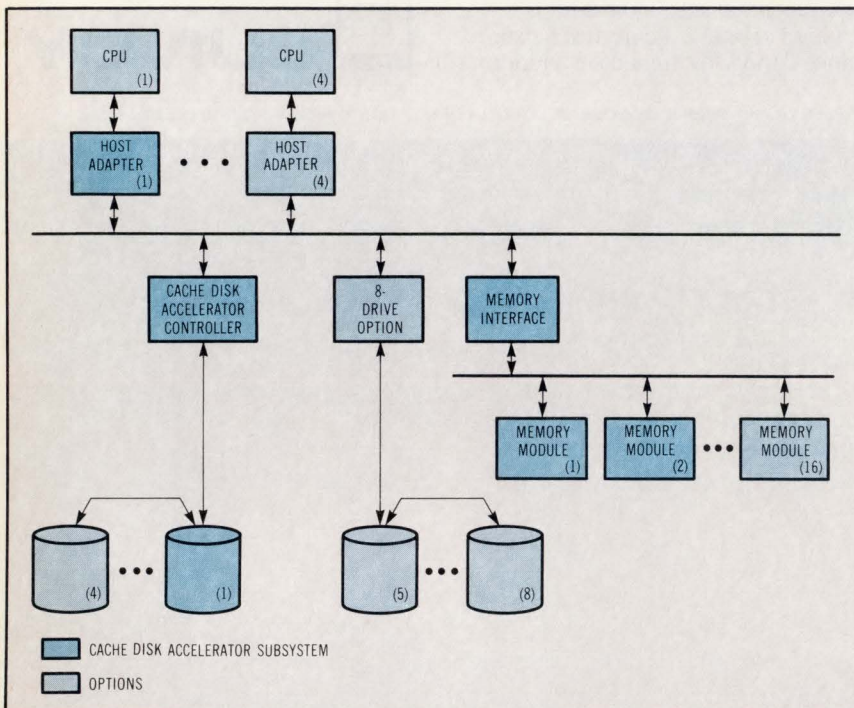
cache system on its Concept/32 series to triple performance.

Disk caching technology was developed first for mainframes. The pioneer was Amperif (Chatsworth, Calif) who developed their first system over two years ago to be plug and program-compatible with Sperry Corp (Blue Bell, Pa) mainframe disk

systems. Using a custom built bit-slice processor (2901) and 2M to 18M bytes of memory, the Amperif system shows as much as a 400% improvement in disk I/O turnaround time. The IBM 3880 Model 11 followed more recently, but that system only takes paged data sets from disk. A full disk cache system, the 3880 model 13 is now available from IBM. Sperry has also introduced such a system and Control Data (Minneapolis, Minn) is reported to have a disk cache under development.

For medium performance minicomputer systems, Qualex Technology Inc (Westlake Village, Calif) will start shipping cache disk drives for HP 3000 systems by the beginning of the year. With a 68000 as a controller and 0.5M to 4M bytes of 64K dynamic RAM cache, the HP system gets two to four times the usual throughput controlling a Fujitsu Eagle 474M-byte disk.

As a contrasting approach to the evolution of a cache disk system, realtime computer systems have used context switching or swapping between disk and main memory for a long time—since 1969 for Gould. This software approach to disk caching is starting to appear on medium performance machines. In May, Hewlett-Packard announced a software-based disk cache for the HP 3000 family of computers. Masscomp (Littleton, Mass), a  
(continued on page 56)

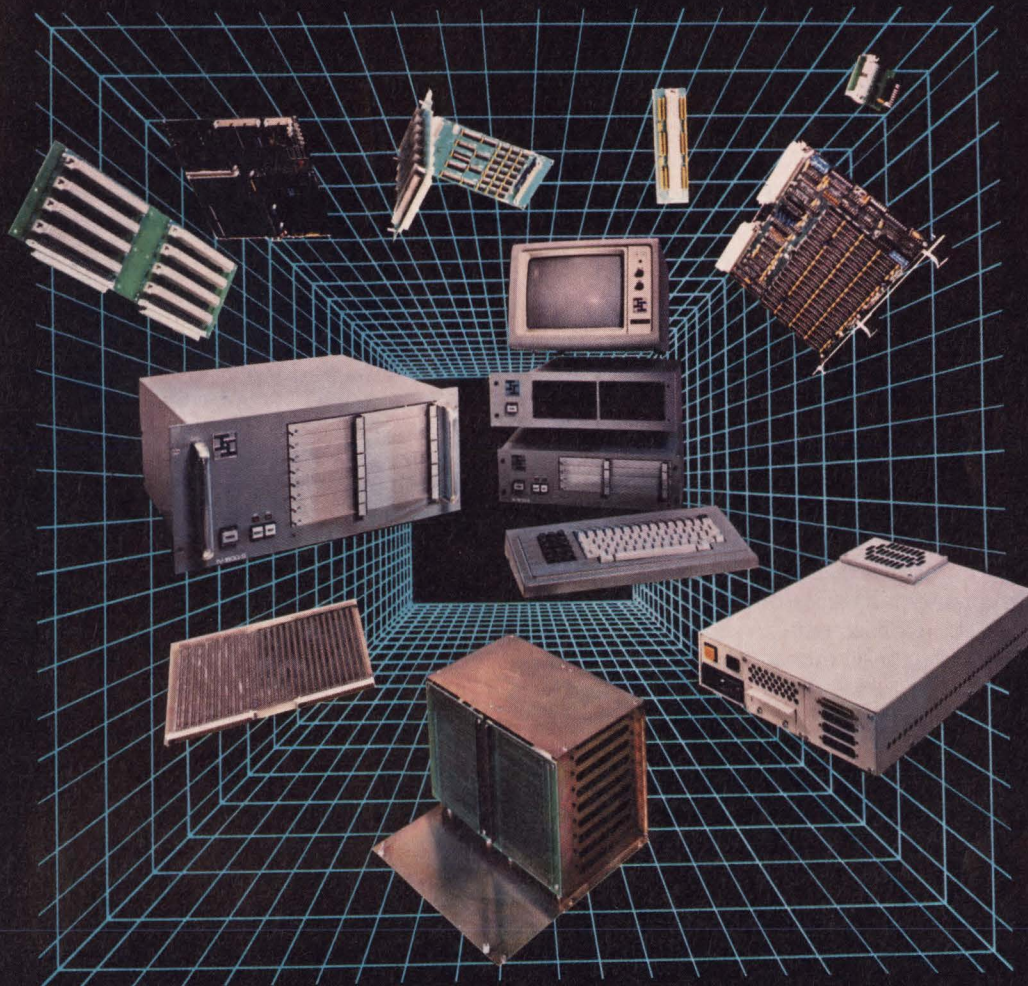


The cache disk accelerator subsystem can boost performance by as much as 300% in disk I/O intensive applications. Built around bit slices, internal cache manager and disk controller manage the control unit, handling transfers to and from the CPU on request.



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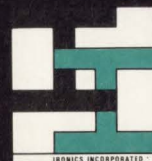
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CIRCLE 34

## Hardware disk cache

(continued from page 54)

manufacturer of high performance 68000/Unix-based microcomputer uses an approach similar to HP, and is eyeing hardware disk cache as a future enhancement.

The trend will accelerate as processors become faster and throughput is increasingly limited by disk access times. Pitted against the mechanical and aerodynamic limits of flying heads and rotating disks, designers are developing schemes to solve the problem. The traditional solution has been to interpose a cache memory between mass storage and main memory. This is typically 4K to 16K bytes of high speed bipolar or, more recently, NMOS static RAM. The "hit rate," or probability of finding the sought after information in the cache, is determined by how iterative the program is and the size of the cache.

Disk caches are much larger and are managed by an internal processor instead of the CPU. Consequently, entire large programs can be moved into the cache and accessed as if

they were on the disk itself. Gould's hardware cache approach used on a 32/8780 computer, already one of the fastest superminis available, can triple its performance in disk I/O intensive applications.

The cache disk accelerator subsystem contains two 16-bit microengines—a cache manager and a disk controller. Each is built around four 2901 4-bit slice processors. The system contains 2M to 16M bytes of high speed static RAM for disk cache memory and one to eight disk drives of up to 675M bytes each.

During read operations on the Gould system, large programs and data files can be kept in the cache for computer access. This can reduce average access time from the 30 ms of a moving head disk to only 1 ms. During write operations, the CPU transfers large blocks of data to the cache and forgets about it. The controller actually writes the data to disk. Along with increased speed, reliability is improved by this process.

Data are less fragmented on the disk because of cache buffering. Thus, there are fewer head movements and a consequently lower MTBF for the mechanism.

To optimize transfer rates between disk and cache, read/write requests are delivered according to the relative position of the heads. The cache has two modes of operation. The first of these, static mode, treats the cache memory as a high speed disk for very fast access. The second dynamic mode uses the cache as a high speed buffer between CPU and disks. This is similar to, but larger than, a conventional cache.

Data reliability can be improved by mirror writing/shadow reading. When this technique is used, the host computer treats two physical disks as a single logical unit and writes data on both. Reading on one or the other is done according to their respective angular positions, to shorten access time.

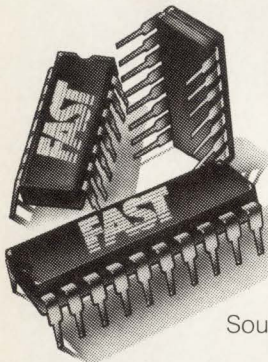
Unlike the Gould brute-force high performance hardware approach to disk caching, the Hewlett-Packard method of software disk caching may be more appropriate for less expensive systems. As implemented in the HP 3000 computers, it allows the use of high density, low cost/M-byte disks without performance penalty. Management of cached disk domains is integrated into the operating system kernel. Disk regions are prefetched and cached in main memory and data are moved between cached disk images and process data areas at memory speeds. The amount of main memory available for cache varies from 0.25M to 2M bytes or more depending on the space available in memory. The memory manager takes precedence over the disk cache. By taking advantage of main memory access speeds, transaction throughput is improved by 30% to 70%.

—John Bond, Senior Editor

SYSTEM TECHNOLOGY  
(continued on page 64)

**December Preview—**  
1983 system components  
roundup.

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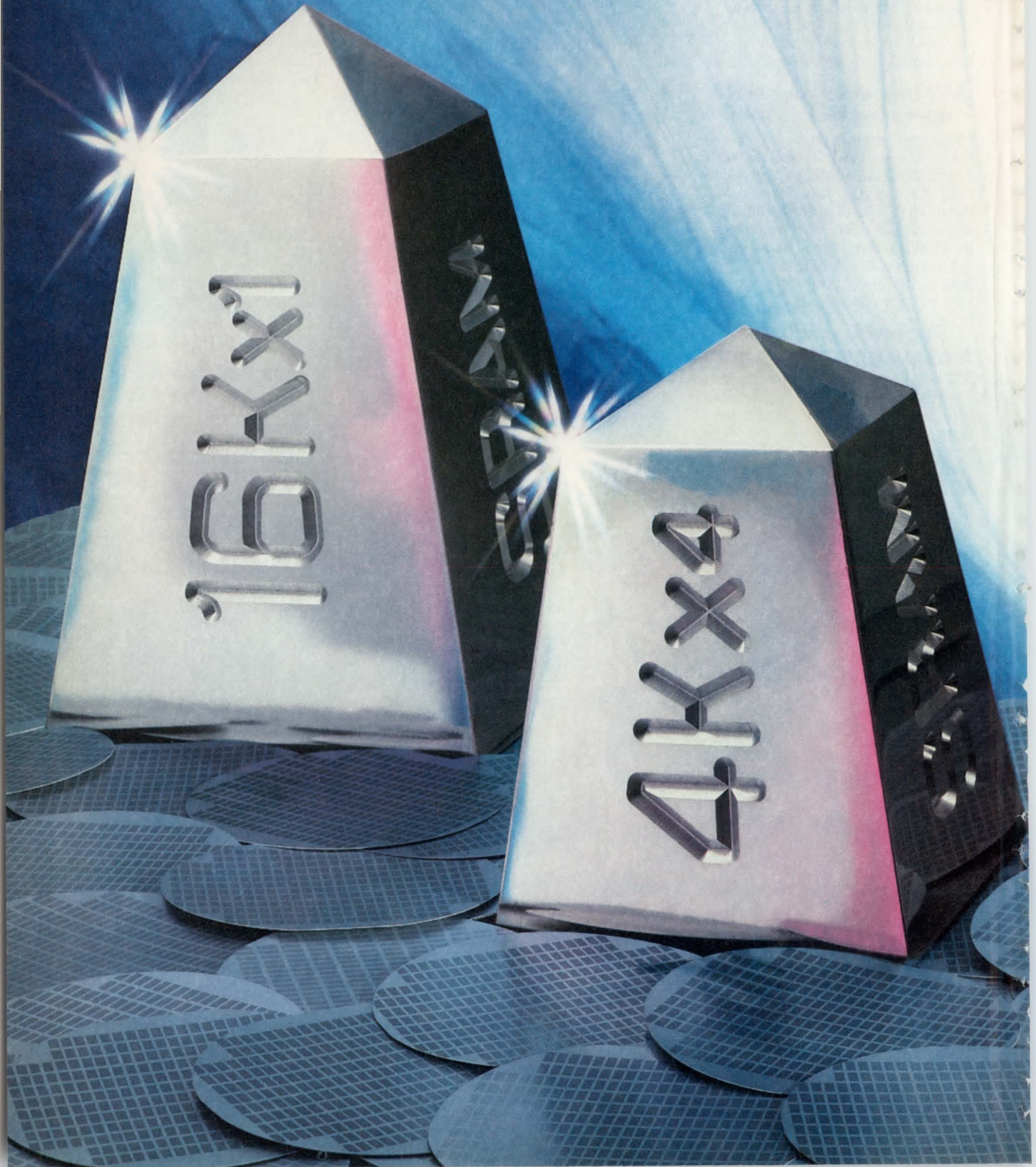
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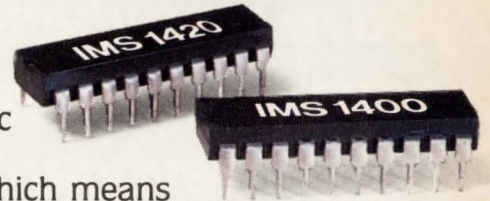


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	45	660	110	IMS1400-45
	55	660	110	IMS1400-55
	70	495	83	IMS1400-70L
	100	495	83	IMS1400-10L
4K x 4	45	605	165	IMS1420-45
	55	605	165	IMS1420-55
	70	495	83	IMS1420-70L
	100	495	83	IMS1420-10L

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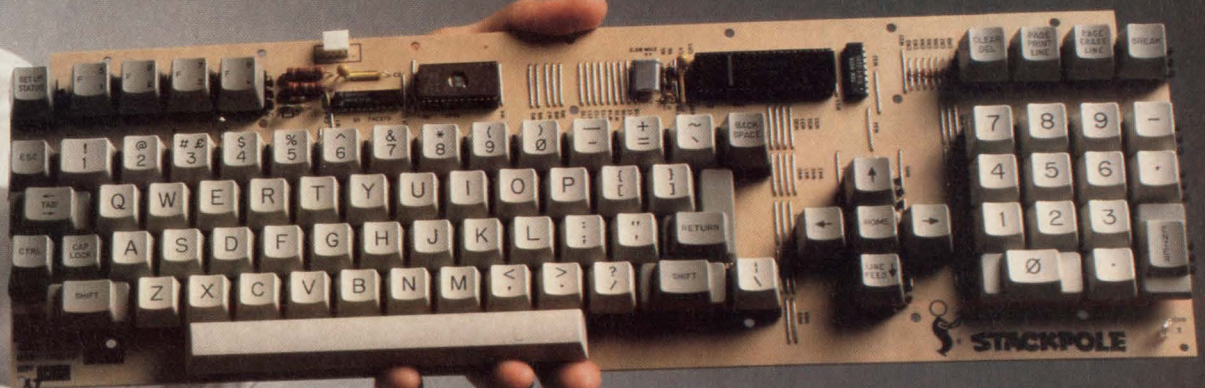
If your design calls for a membrane keyboard—one that works well from the first touch and will continue to work well over its rated life of 20,000,000 cycles—ask about the KS-500E. It's available in a wide selection of two-shot keycaps, a variety of colors and finishes and in either low profile or ultra-low profile.

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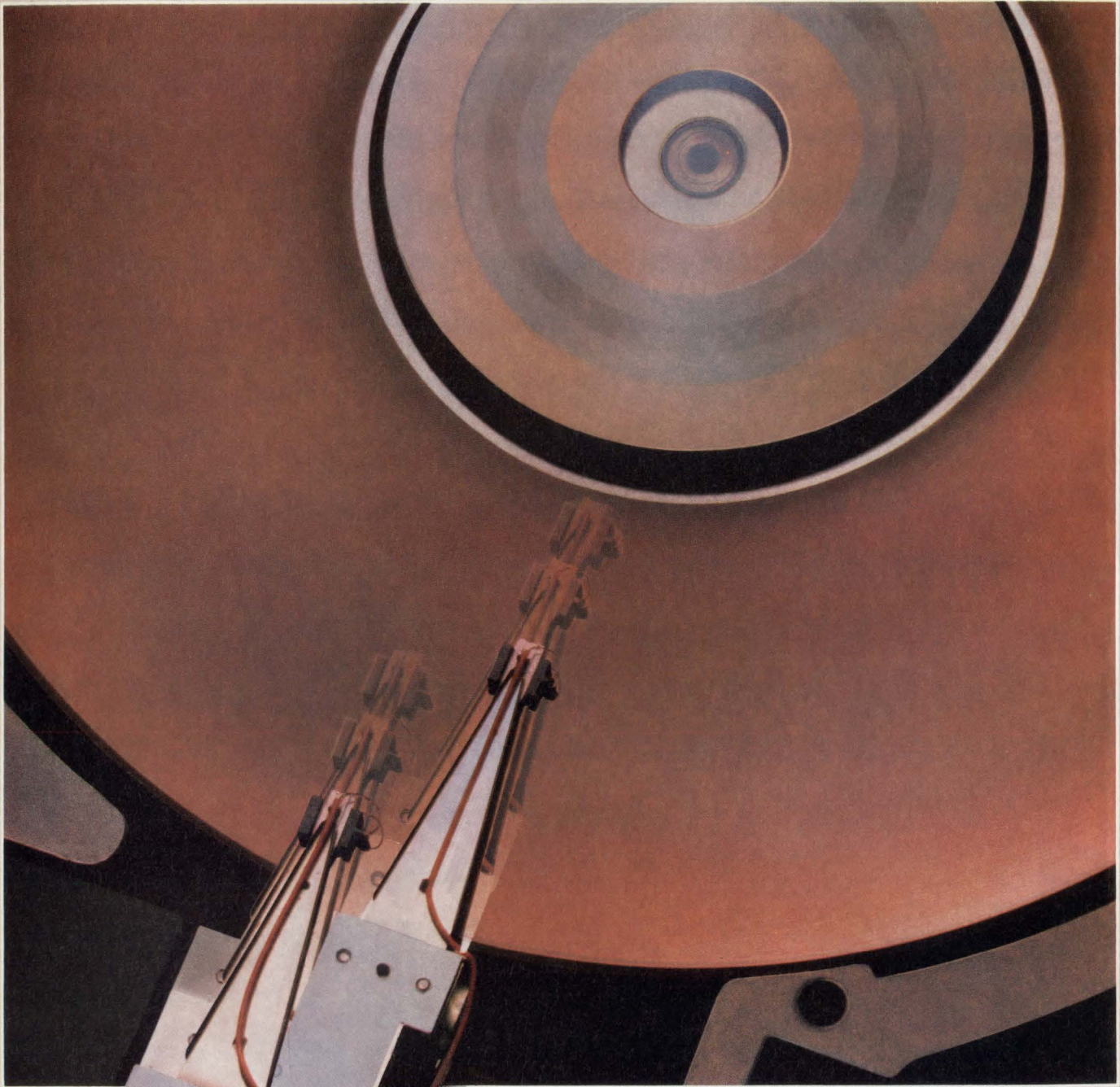
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## Processors divorced from peripherals with separate I/O bus

Device independence dominates the philosophy behind the Small Computer System Interface (SCSI). Moving peripherals from the system backplane to a separate I/O bus isolates host processors and operating systems from changes in disk drives, tape drives, and printers.

The proposed ANSI X3T9.2 standard expands the original emphasis of the Shugart Associates System Interface (SASI) on floppy and rigid disk drives to include other serial I/O devices. Under either scheme, hardware host adapters translate the unique message protocol of a specific system bus (Multibus, Versabus, or S100) to a common protocol understood by all SCSI devices. In addition, software commands are issued for such generic devices as disks, tapes, and printers. Specific device information (eg, sector addresses) is omitted.

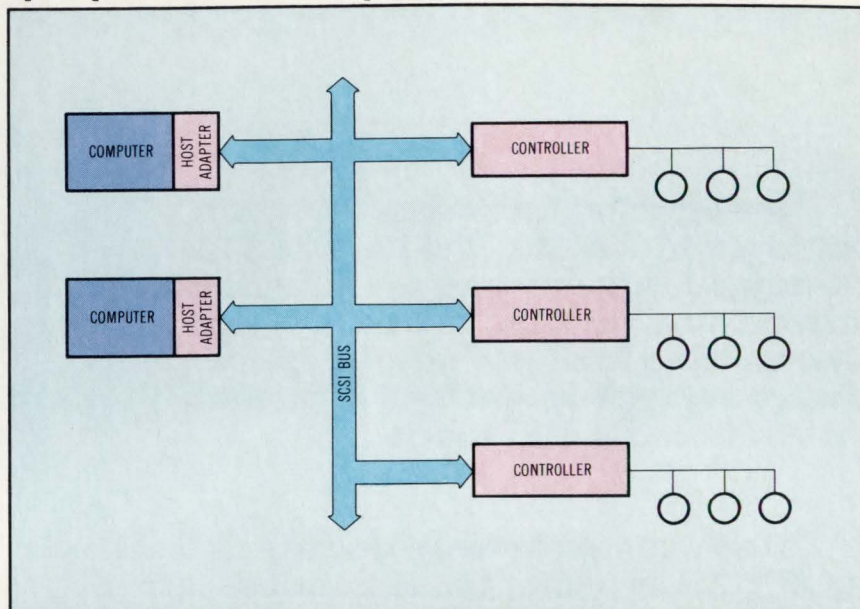
Peripheral controllers assume responsibility for physically addressing devices. Host processors merely specify the first block address and the number of data blocks to be transferred. Up to 64K bytes of data can be transferred with a single host command.

Task execution and I/O processing can occur simultaneously because host adapters can be disconnected from the I/O bus once the host processor issues an I/O command. This frees the host processor to execute other tasks. Controllers also disconnect from the I/O bus after receiving the command from the host adapter. This bus remains free for other I/O operations until data needs to be transferred between the controller and host adapter.

### Design considerations

Flexibility does, nevertheless, come with a price. System designers must choose the level of intelligence needed in host adapters and controllers. Also, existing host peripheral drivers and I/O supervisors must be rewritten to take advantage of the high level command sets available in SCSI.

The intelligence of the host adapter still remains the determining factor for functionality of the SCSI. A simple



The SCSI bus can be described as a peer-to-peer architecture. Host adapters and controllers can assume either the role of request initiators or targets to perform operations. Up to eight host adapters and eight controllers can be attached in this manner.

adapter composed of discrete logic continues to place the brunt of I/O supervision on the host processor. This provides an easy way to add controllers and peripherals into existing systems. System software remains largely unchanged since the I/O bus acts as an extension of the system backplane.

However, system overhead is not reduced with this implementation. About 50% of system bus capacity is usually dedicated to servicing I/O operations, according to the product line manager with Shugart Associates (Sunnyvale, Calif). Minicomputers are notorious for bogging down in multitasking environments because their operating systems cannot speed through data to the processor. Adaptec (Milpitas, Calif) has approached this problem by moving I/O processing from the host operating system to the host adapter. This effectively frees 50% of the system bus for task execution. The host operating system still retains its supervisory functions, such as event scheduling and interrupt handling.

Through the use of intelligent host adapters, peripherals and controllers

can transfer data at 1.5M bytes/s along the I/O bus. Adequate buffering on the host adapter and controller compensates for different transfer rates between the I/O and system buses.

Moving physical sector addressing, formatting, error correction, and other device-specific operations to intelligent controllers further simplifies host operating systems. However, users must rewrite the device drivers that link application programs with necessary I/O services. In the past, they have contained commands geared to a specific controller/peripheral combination.

### Outlooks for SCSI use

As host adapters and controllers become more intelligent, so too will the peripherals. Rigid disk drives from several vendors now include SCSI controllers, with tape and floppy disk drives soon to follow. Intelligent modems and network controllers are likewise under development for use on the I/O bus.

Integrating a SCSI controller on the drive becomes more viable as key functions (eg, data separation,  
*(continued on page 67)*

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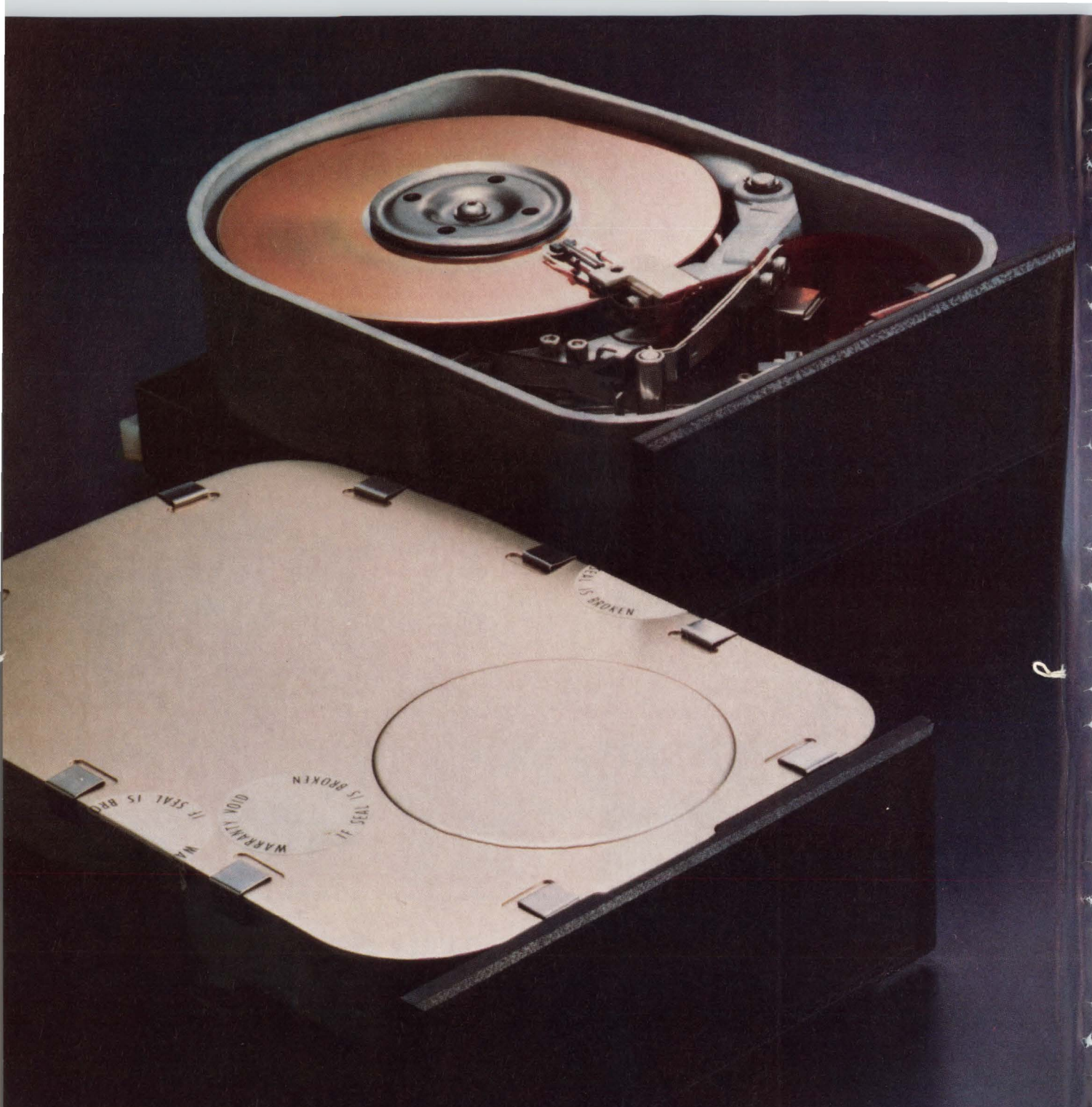
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**OTARI**

# SYSTEM TECHNOLOGY/ INTERFACE

## Independent processors (continued from page 64)

serializing/deserializing, and formatting) are implemented in silicon. Chip sets are already available from Adaptec, Intel Corp (Sunnyvale, Calif), National Semiconductor (Santa Clara, Calif), and Shugart Associates. NCR Corp also shows an interest in marketing chips sets.

Current embedded SCSI controllers require a separate board apart from that used for the drive electronics, despite the high level of integration. A device level interface such as ST506 or a SMD is also needed to translate SCSI system level commands to the control signals that are directly executed by the drive. Disk drive vendors using this scheme include Cynthia Peripheral (Palo Alto, Calif), Fujitsu America Inc (Sunnyvale, Calif), Iomega (Salt Lake City, Utah), and Shugart.

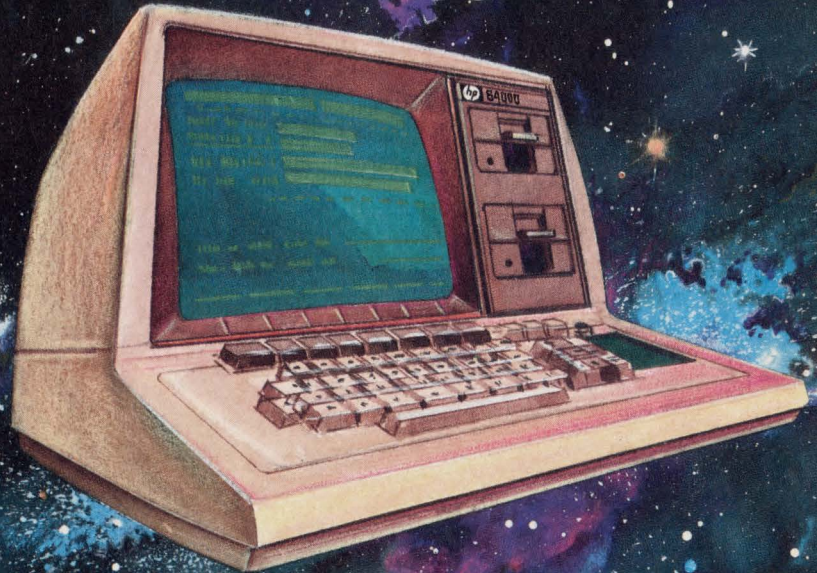
Tape drive manufacturers view embedded SCSI controllers as a ready means to back up rigid disk drives. The interface proposal contains a COPY command that enables streaming operations without host intervention. Also, the interface has gained industry acceptance in its present SASI implementation. Questions still surround the only competitive tape interface, QIC-02, proposed for quarter-inch cartridge drives (see *Computer Design*, July, 1983 p 48). Tape drive vendors publicly supporting SCSI include Archive Corp (Costa Mesa, Calif) and Memtech Corp (Salem, NH).

Serial I/O communications will also play a part in future SCSI implementations. A combination printer controller/modem is under development by Adaptive Energy and Data Systems (Pomona, Calif). The auto-dial/answer modem will spool messages on a disk drive in much the same manner that printer spoolers are currently implemented. Interrupts are used to inform the host or modem that messages are in the queue. Network communications can be handled in a similar manner.

—Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY  
(continued on page 74)

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EMULOGIC VAX 11/780

REGISTERS		HS MAPPING		TRACE		SYSTEM	
NO	ADDRESS	WFC	FROM TO	ASSC TYP	ON OFF	BREAK POINTS	
B0	00000006	A0	00000100	-	0 OFF	B7	> B0 000230 DM
B1	12345678	A1	00080000	-	000000-000000	0 OFF	
B2	00005555	A2	00080003	S	000000-007FFF	1 RAM	B1 UNDEF OFF
B3	00086789	A3	00042354	S	008000-00FFFF	2 RAM	B2 UNDEF OFF
B4	FFFF0000	A4	00FOFF0E				B3 UNDEF OFF
B5	00770077	A5	00000000	SFC	6		B4 UNDEF OFF
B6	00000FFF	A6	00FOFEFE	DFC	6		B5 UNDEF OFF
B7	00888888	US	000014FE	VBR	00000100	T S I X N Z V C EFC	B6 UNDEF OFF
PC	000200	SS	000003F0	SR	2705	0 1 7 0 0 1 0 1 S	B7 LOGICAL DM

LOC ADDRESS	INSTRUCTION	DATA	78643210	C	ACRE	P	MP	F	NO	SI	MI
499	00022C TRAP B0	4E40	00000000	6	1111	7	11	0	00	11	1
500	00022E NOP	4E71	00000000	6	1111	7	11	1	00	11	1
501	0003F4	DATA	022E	00000000	5	1111	7	11	0	00	11
502	0003F0	DATA	2700	00000000	5	1111	7	11	0	00	11
503	0003F2	DATA	0000	00000000	5	1111	7	11	1	00	11
504	0003F6	DATA	0080	00000000	5	1111	7	11	0	00	11
505	000180	DATA	0000	00000000	5	1111	7	11	1	00	11
506	000182	DATA	0230	00000000	5	1111	7	11	0	00	11

EMULOGIC

TYPE: 68010  
 FREQ: 8000 KH  
 SIGHT:  
 MODE: COMMAND

EMULOGIC

SETUP

ESC / 2 # 3 4 5 6 7 8 9 0 - = BACK SPACE BREAK 7 8 9 -

TAB O W E R T Y U I O P { } DELETE 4 5 6 ,

CTRL CAPS LOCK A S D F BELL G H J K L ; : RETURN \ 1 2 3

NO SCREEN SHIFT Z X C V B N M < > ? SHIFT LINE FEED 0 ENTER

# WAKE UP YOUR SLEEPING GIANT.

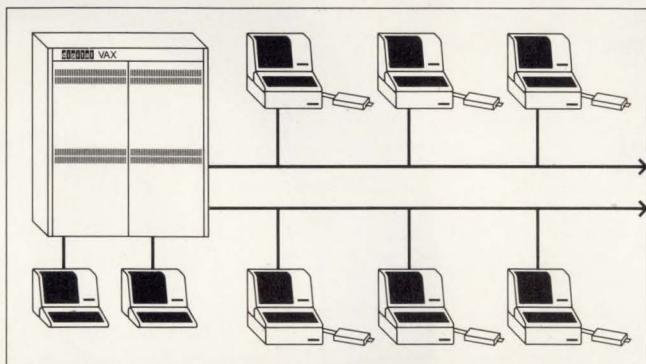
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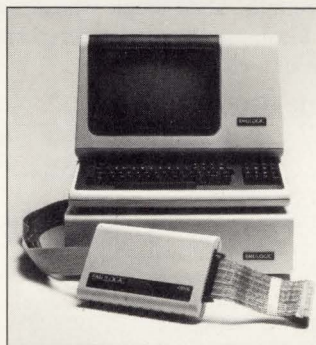
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INTELLEC® DEV. SYSTEM	8" floppy	NOW	NOW	3/84
IBM® PC	5¼" floppy	NOW	NOW	1/84
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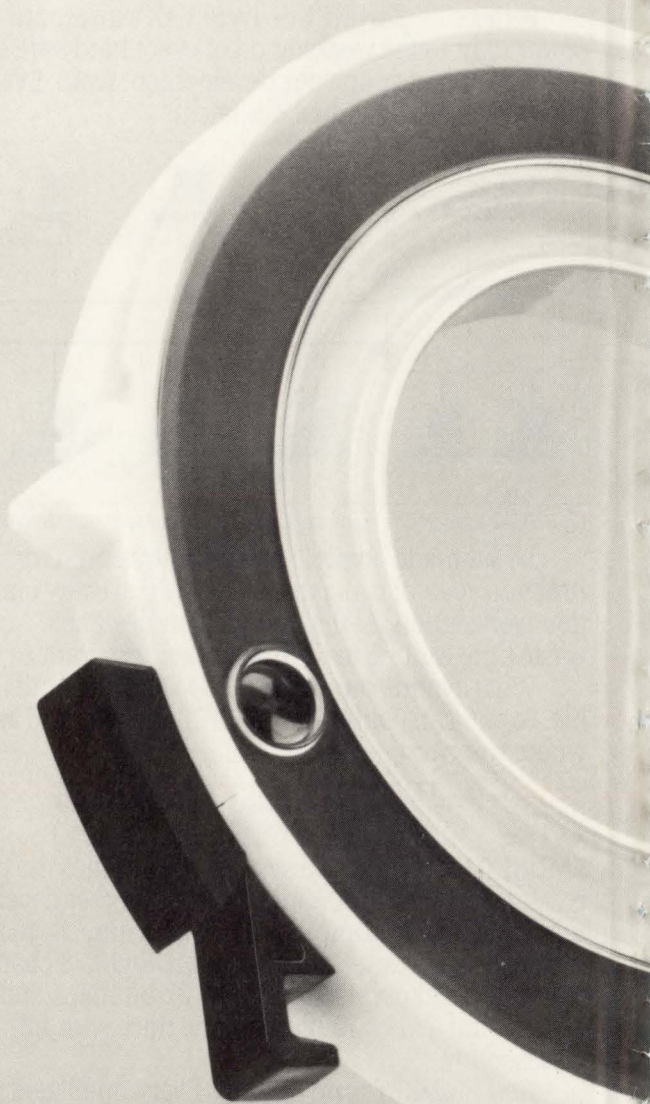
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CD11/83

\*CP/M version operates with other systems, including Altos, Heath, Kaypro, Osborne and more.

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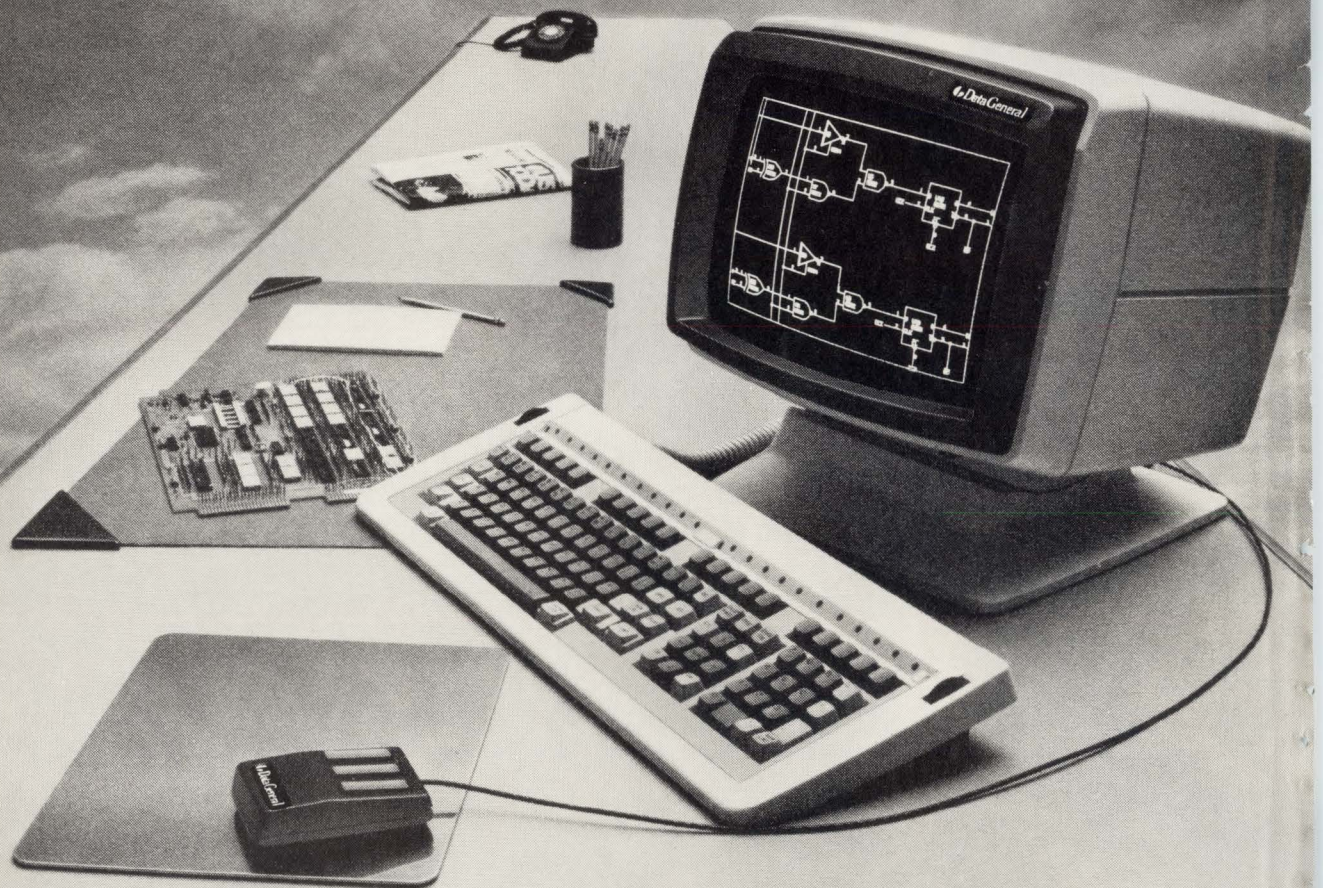


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CIRCLE 44

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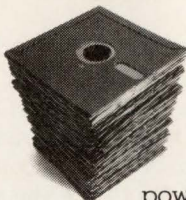
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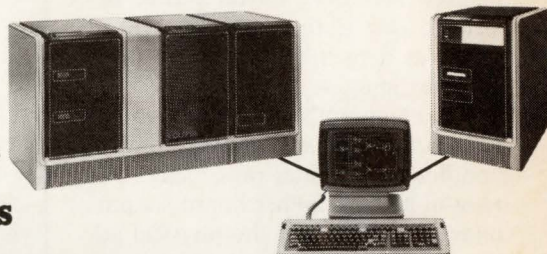


It accepts both popular micro-based operating systems (CP/M-86, MS-DOS) as well as three of Data General's widely-used operating systems (AOS, RDOS, MP/AOS).

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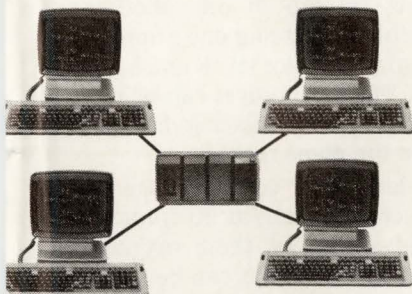
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## Color graphics system accesses images at 20M bytes/s

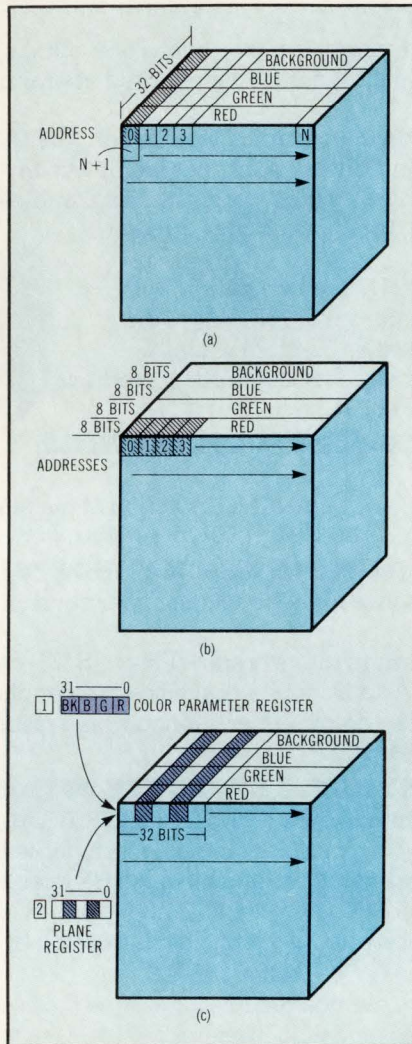
Graphics designers can manipulate individual pixels with the CD1100 color subsystem from Symbolics Inc (Chatsworth, Calif). Multiple addressing modes give direct access to any pixel or blocks of pixels anywhere within the 1280 x 1024 pixel display memory. Furthermore, designers can define any pattern of pixels as a primitive to create more complex images.

The company's 3600 computer (see *Computer Design*, May 1983, p 280) handles all graphics processing. The plug-in color graphics board set puts image memory into the physical address space of the main processor. The board's 2M-pixel memory gives users a choice in the resolution of each pixel (8/16/24/32 bits). A color map that outputs a maximum of 10 bits for each of the primary colors—red, green, and blue—offers potential for 1G colors.

Integrating the display memory with main memory avoids many limitations found in dedicated graphic workstations. Such systems typically are tied to the main processor via a high speed serial link. When main memory is separate from display memory, graphic information must be compressed into display lists for transmission across the link. Once transmitted, the display must be translated into pixel and color information by a separate graphics processor.

Rather than being limited to the transfer rate of the serial link (usually running at 19.2k bps, the Symbolics processor can update the image memory at the 20M-byte/s data rate of the system bus. The image memory bus is dual-ported so that the video controller refreshes the screen on a separate color bus.

Placing image memory on the system bus eases the implementation of the multiple color address modes. Each of the three modes (pixel, plane, and fill) represents a different logical color mapping of the physical image memory. Designers select the desired mode by specifying an address contained in the computer's virtual address space.



Addressing modes for the color memory map are best viewed in terms of a 3D block of cells: (a) pixel mode causes a single 32-bit deep pixel to be changed; (b) packed mode has a single 32-bit word to update four pixels simultaneously; (c) fill mode uses the color parameter register to hold a desired color value, while the plane register designates specific bits to be altered.

Pixel mode is useful for such applications as image processing where the pixel is the important addressable unit. A single 32-bit word can map eight levels of each of the three primary colors with an 8-bit background shade also included (see Figure). Packed mode becomes useful if color memory is only 8 bits deep. A single 32-bit word can then color four adjacent pixels in one

memory operation. Fill mode is applicable when patterns (eg, stipples, half-tones, or characters) must be written quickly. A color parameter register uses a 32-bit word to color 32 adjacent pixels. Another 32-bit word stored in the plane register determines which pixels will contain the pattern. Each 600-ns memory write operation can fill 1024 bits/s.

Software overlays can be created when the fill address mode is used in conjunction with "rasterop." This technique allows a rectangular pixel pattern (raster) to be modified by a preselected command (op). Up to 16 Boolean operations are microcoded to manipulate patterns anywhere within both main and display memories. Graphic primitives such as triangles and circle splines are manipulated with rasterop. Users can also create their own graphic primitives.

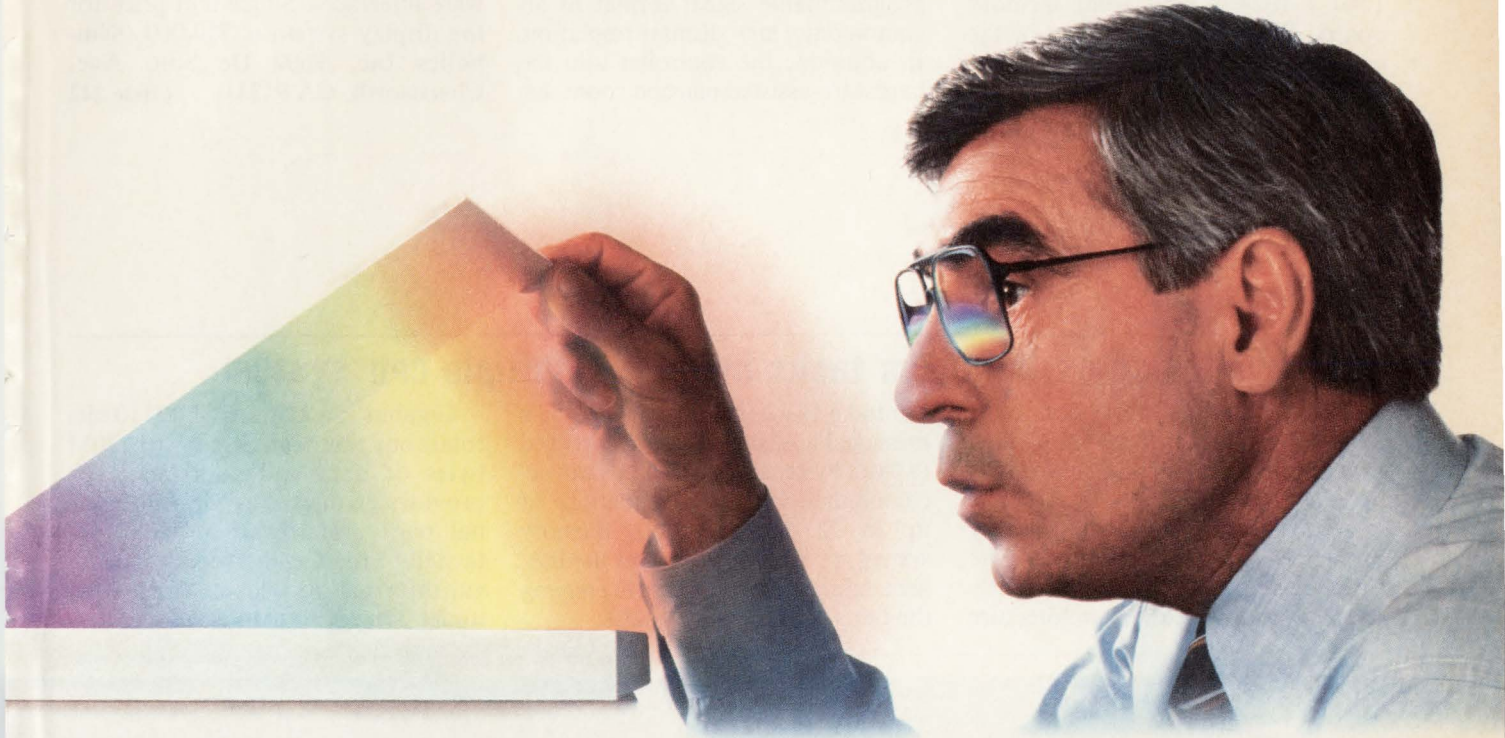
The fill addressing mode provides the means to place four such primitives on top of one another. This is done by placing one primitive at each of three color levels and background. These primitives can be hidden or displayed by placing different values in the plane register.

An elementary computer animation scheme running at 30 frames/s takes advantage of these overlays. The rectangular arrays can be stored and then redisplayed at different display memory locations via the fill addressing mode. More elaborate animation involving complex 3-D images with hidden surfaces takes considerably longer. To complete complex animation schemes, extensive numerical computations are needed to accurately move the object as a whole.

Applications such as computer aided design, image processing, and animation benefit from tools such as the ZMACS display editor and Zetalisp interpreter, which can manipulate both text and graphics. However, separate graphics and programming languages are needed to develop such applications in conventional host/workstation environments.

(continued on page 76)

# The Newest Innovation in Controller Technology From the Oldest Name in Multifunction Controllers.



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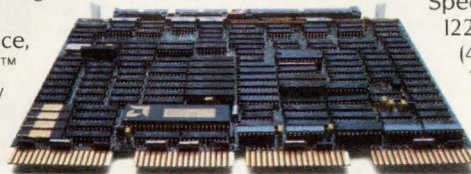
The SPECTRA 25 emulates DEC's RM02/5 and RM80 disk subsystems, and DEC's TSII tape subsystem. It also provides complete emulation for operation with DEC's RT-II, RSX-IIM, RSX-IIM-PLUS and RSTS/E operating systems.

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## SPECTRA LOGIC

## Color graphics system

(continued from page 74)

The CD1100 color display system comes standard with a video controller, video paddle card, and one 1280 x 1024 x 8-bit color memory board. With this configuration, the color map operates in the pseudo-color mode to simultaneously display

256 colors. More memory boards increase pixel depth in 8-bit increments.

The video controller contains a programmable signal format to accommodate any display resolution. In addition, the controller also has hardware-assisted pan and zoom that

can move and zoom to any line or pixel. The video paddle card contains the required connectors and hardware interfaces. Single-unit price for the display system is \$30,000. **Symbolics Inc.**, 9600 De Soto Ave, Chatsworth, CA 91311. **Circle 242**

## COMPUTERS

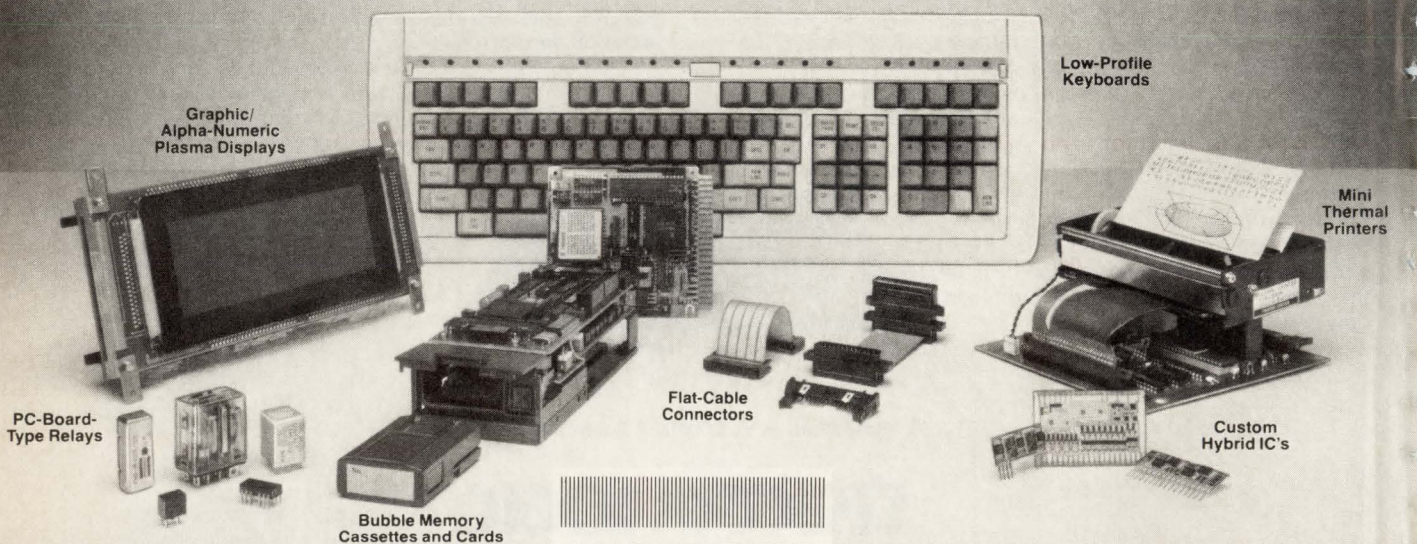
### Message-based OS balances tasks in 64-bit multiple CPU system

A 64-bit multiple processor computer system can execute 4M to 40M Whetstone instructions/s. Configured with up to 10 processors, the system handles physical memory capacities up to 192M bytes. The Elxsi system 6400 bases its tightly coupled multiple CPU architecture

around a 64-bit wide system bus and a message-based operating system called EMBOS. System configurations can accommodate various combinations of up to 32 modules (CPU, memory system, or I/O processor) on the bus. Scheduling and load balancing among the CPUs is handled by EMBOS.

Gigabus is a 25-ns, 64-bit (110 bits total) bus that transfers up to 320M bytes of data and addresses/s. It provides error checks via full internal parity. Hardware modules attached to the Gigabus communicate via information packets (messages) under control of EMBOS.

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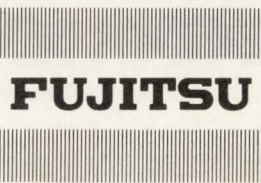
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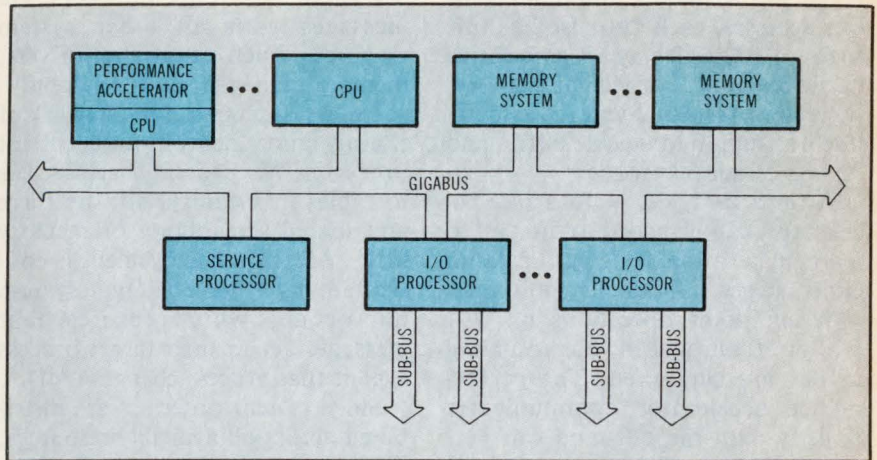
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System modules connect to the bus through controllers which are differentiated for their given function by microcode. Thus, a CPU consisting of three cards need occupy only one slot on the Gigabus; a single memory controller can accommodate from 4M to 32M bytes. Up to 16 controllers can be attached to the bus in one cabinet and two cabinets can be connected together for a total of 32 bus slots.

One bus slot is occupied by the 68000-based service processor. The microprocessor handles system start-up and bootstrap functions. In addition, the service processor performs system diagnostics to locate and aid in the repair of malfunctions, as well as error logging and environmental monitoring. It also provides terminal and communication facilities for local and remote diagnostics.

The CPU consists of an arithmetic logic unit, a cache/translation



A typical system configuration for the Elxsi system 6400. Systems expand from 1 to 10 CPUs and handles from one to eight memory modules. As many as six I/O processors may be configured. All modules connect via microprogrammed controllers to the Gigabus. All communication between hardware modules, as between processes, takes place via messages.

lookaside buffer, and an optional performance accelerator. Making extensive use of ECL gate array logic, a single CPU can execute 4 million in-

structions per second (MIPS). Each CPU has 64-bit wide data paths and 16 sets of 64-bit general purpose  
*(continued on page 78)*

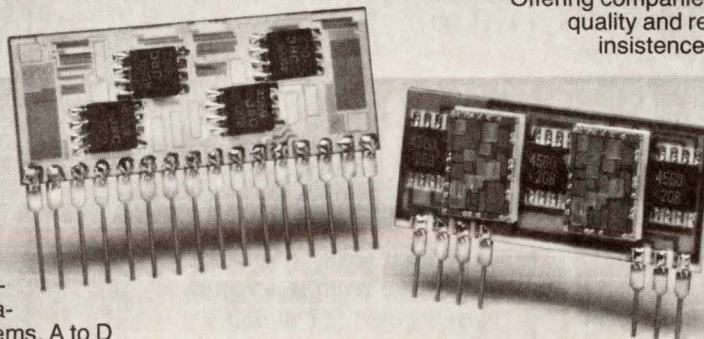
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## Message-based OS

(continued from page 77)

registers. To reduce the number of bus accesses, each CPU also has 16K bytes of 100-ns 2-way set-associative cache memory. For virtual memory, there are 16 sets of 2-way set-associative translation lookaside buffer and 32 bits of address space.

A third card, the performance accelerator, can be added to the CPU to manipulate variable length data in either integer or floating point format. Floating point operations on 32-, 64-, or 80-bit data in four rounding modes are supported. The performance accelerator communicates directly with the CPU and can perform a 64-bit register-to-register add in 200 ns.

From 4M to 192M bytes of main memory attach to the Gigabus via microprogrammed memory controllers. The CPUs' 32-bit address space provides up to 4G bytes of virtual space per user process. ECC supplies single- and double-bit error detection and single-bit error correction with detection of most multiple-bit errors. Cycle time is 400 ns.

Dedicated I/O processors, which likewise connect to the bus via microprogrammed controllers, can provide two 8M-byte/s channels, or sub-buses. Each sub-bus has 16 ports and connects to dual-ported I/O device controllers. These include disk controllers, tape/line printer controllers, and a communication multiplexer.

The disk controller supports one to eight drives in any mix of 300M or 675M bytes per drive. It is powered by a 2900 bit-slice processor which performs physical to logical address translations. The communication multiplexer can supply 32 full-duplex asynchronous lines at 110 to 19.2K baud, or synchronous support for SDLC, HDLC, ADCCP, and bisync protocols.

## System software

Parallelism of the hardware architecture is complemented by the message-based EMBOS operating system. EMBOS distributes processing tasks among all CPUs currently attached to the system, adjusting scheduling to match processing demands. An operating system kernel resides

on each CPU and interacts via messages with all other system resources, such as the I/O drivers, memory manager and file system.

EMBOS is structurally a network of timing and location-independent processes. No process shares access to tables in memory, nor are there any shared semaphores or memory locks. Message management is controlled by the message system microcode, which ensures that messages get to their target process even if that process changes CPUs.

Since system processes are distributed across all available resources, throughput is maximized and can be enhanced incrementally by adding resources. For instance, throughput is doubled from 4 to 8 MIPS simply by adding a second CPU. Up to 10 CPUs can be placed on the system for an aggregate speed of 40 MIPS.

Along with EMBOS, which has a Unix-like user interface, the Elxsi system 6400 provides such high level languages as Pascal, C, Fortran 77, and Cobol-44, as well as the INGRES database management system. Due to the large, 4G bytes of virtual memory which each user process can have on top of the 192M-byte main memory, it is possible to implement a "mapped files" concept. Mapped files automatically map the data base into the user's virtual process space. An extra step of address translation is thus eliminated for data accesses and increased throughput. Elxsi, 2334 Lundy Place, San Jose, CA 95131.

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## SYSTEM TECHNOLOGY

(continued on page 87)

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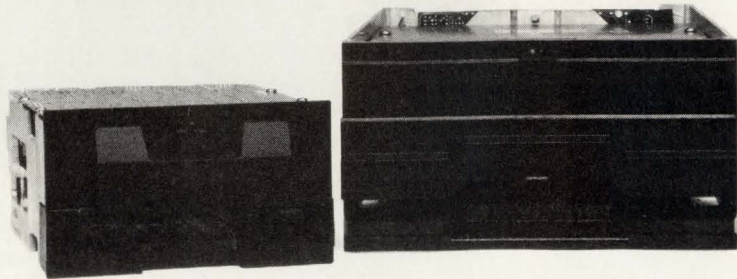
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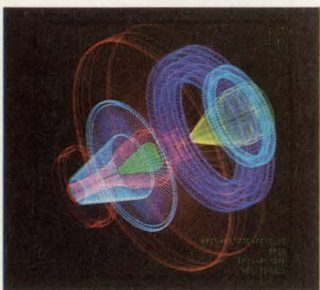
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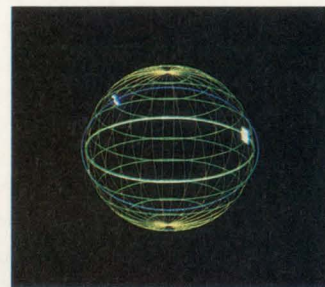


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## Commercial GaAs digital ics run at 2 GHz

Digital integrated circuits using gallium arsenide technology will soon be released as commercial products by Harris Microwave Semiconductor. The first products will be small scale integration (SSI) parts using a 1-micron process on 2" (5-cm) wafers. They will include a 4-bit universal shift register and a divide by 2/4/8 divider. Clock speeds will initially be 1.5 to 2 GHz.

These initial parts are primarily intended for signal processing applications which push the digital front closer to the raw signal, taking over functions that were formerly performed by analog devices. Harris' interest in digital GaAs ICs, however, appears to be long term and is turning toward the computer arena.

A joint contract is currently underway between Harris and Cray Research (Mendota Heights, Minn) for exploration of memory and gate array technology. The goal of this joint venture is to develop a 64- x 1-bit RAM chip. Since memory technology generally drives gate array technology, first developments from this project are expected to be GaAs memory chips. To achieve emitter-coupled logic (ECL) compatibility among the chips, the reference voltage to a given value is set depending on whether the device is operating in a GaAs environment or interfacing to ECL.

The soon to be released 1.5-GHz shift register utilizes a serial or parallel I/O, shift right or left, and has a setup time of less than 350 ps. The chip is approximately 80 mils per side and is housed in a flatpack. Numerous ground pins are interspersed among the signal pins to reduce crosstalk at high clock speeds. Power dissipation for the shift register is currently about 1.5W.

In addition to the divider and shift register, Harris plans to introduce various SSI logic elements, such as flipflops, NAND, NOR, and XOR gates, and buffers, within the next six to nine months. Clock rates for

these parts are anticipated to be in the 3- to 4-GHz range.

Harris is revamping all aspects of the technology—from designing and building its own large capacity crystal grower to creating its own test equipment—and foresees the technology evolving along a learning curve that will significantly reduce power dissipation and increase speed. Current power dissipation is approximately 40 mW per gate, and 0.5mW per gate is considered feasible. Although low power is not a primary objective at this time, it will become a significant concern as circuit complexity increases. Among the current advantages are the wide operating temperature range, -55 to 100 °C and a substantially greater hardness to radiation than silicon.

In addition to the ICs to be released, Harris considers currently feasible a gate count complexity up to 200, and a typical power dissipation of 15- to 25-mW gates. Custom IC engineering and device fabrication is available now, and Harris is presently moving to 3" (8-cm) wafers. Four different devices are already fabricated on a wafer and the larger size will undoubtedly increase yield and reduce costs. **Harris Microwave Semiconductor**, 1530 McCarthy Blvd, Milpitas, CA 95035.

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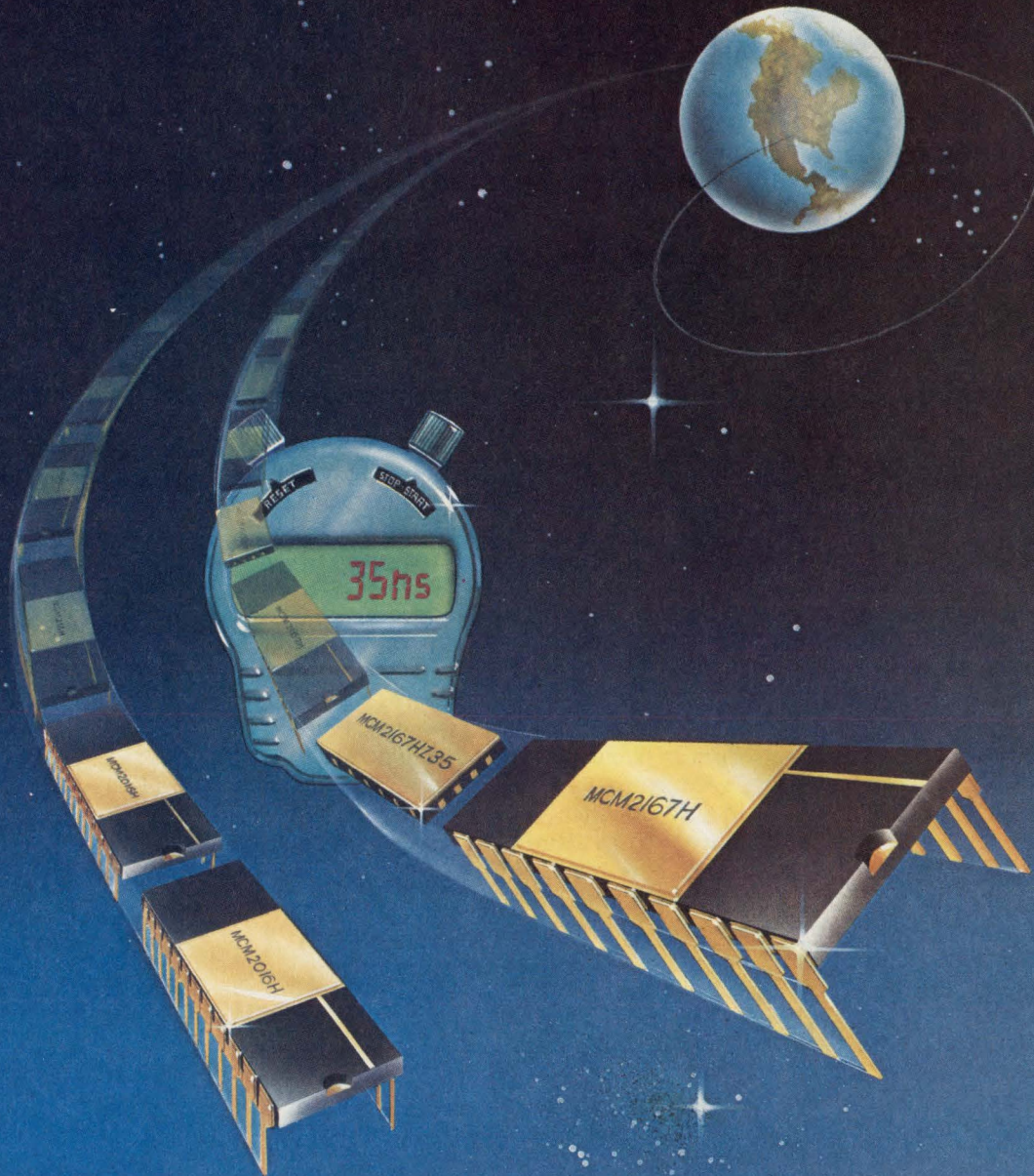
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## Absolutely no clocks or timing strobes.

As stated, these are fully static memories. No clocks or timing strobes are used. Power down is controlled by

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ORGANIZATION	ACCESS TIME (MAX)	PART NO.	PACKAGE TYPE	OPERATING CURRENT (MAX)	STANDBY CURRENT (MAX)	TECHNOLOGY
16K x 1	35,45,55 35,45,55 35,45,55	MCM2167HL MCM2167HZ MCM2167HP	300 Mil Ceramic DIP Leadless Chip Carrier 300 Mil Plastic DIP	120 mA 120 mA 120 mA	20 mA 20 mA 20 mA	HMOS HMOS HMOS
2K x 8	45,55,70 45,55,70 45,55,70	MCM2016HY MCM2016HL MCM2016HP	300 Mil Ceramic DIP 600 Mil Ceramic DIP 600 Mil Plastic DIP	120 mA 120 mA 120 mA	20 mA 20 mA 20 mA	HMOS HMOS HMOS
2K x 8	120,150,200 120,150,200	MCM6116P MCM611L16P	600 Mil Plastic DIP 600 Mil Plastic DIP	55 mA 55 mA	2000 uA 100 uA	CMOS CMOS
4K x 1	55,70 55,70	MCM6147P MCM611L47P	300 Mil Plastic DIP 300 Mil Plastic DIP	35 mA 35 mA	800 uA 100 uA	CMOS CMOS



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A  MCM2167H    B  MCM2016H    C  CMOS

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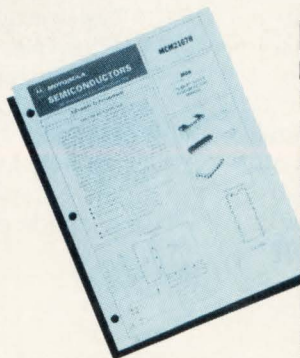
Name \_\_\_\_\_

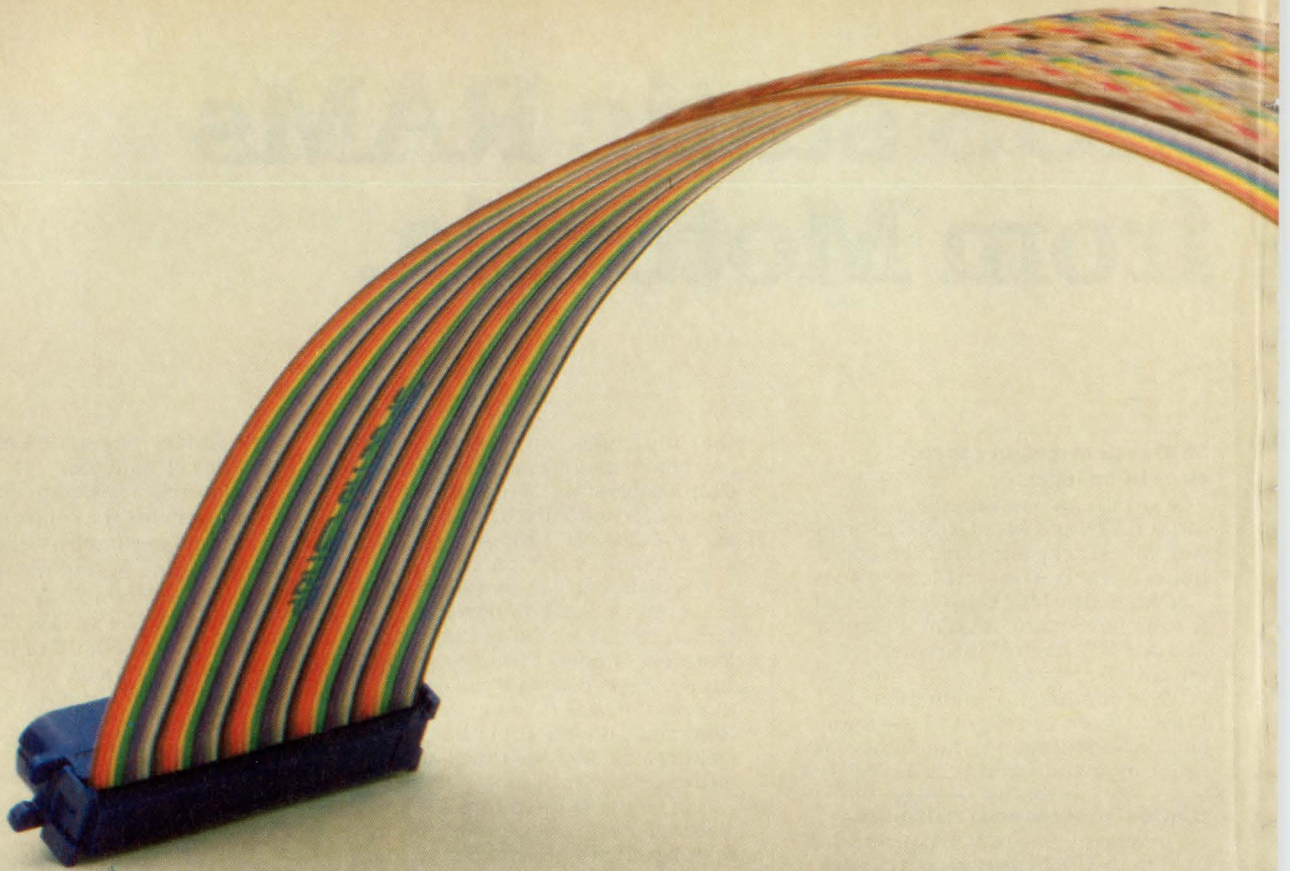
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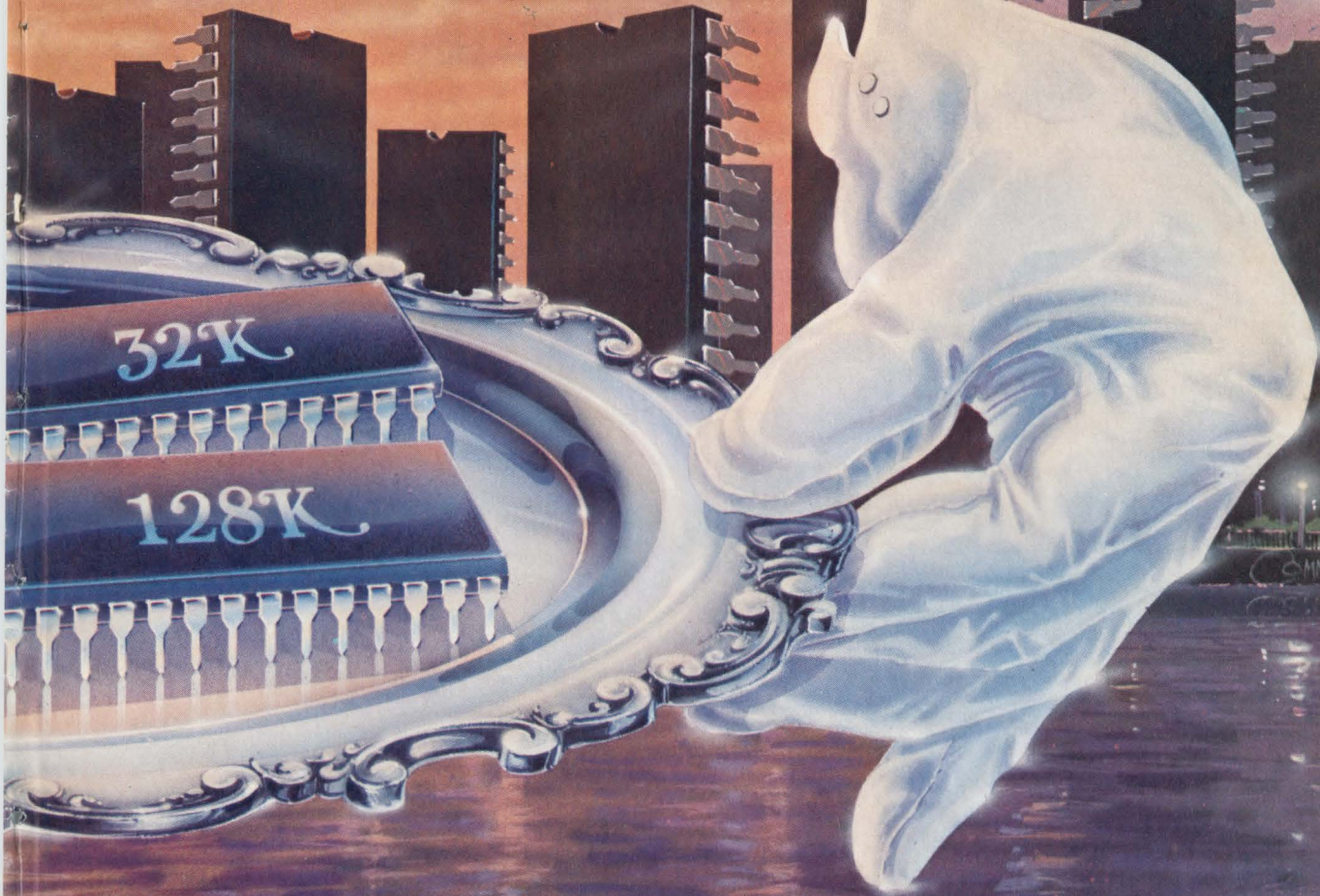
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NMOS MASK PROGRAMMABLE ROM					
Capacity	Part No.	Organization	Access Time Max. (ns)	Power Dissipation Max. (mA)	
				Active	Standby
16K Bit	TMM334P*	2K x 8	450	80	—
32K Bit	TMM333P*	4K x 8	450	100	—
32K Bit	TMM2332P*	4K x 8	350	100	15
40K Bit	T6635**	4K x 10	350	90	—
64K Bit	TMM2364P**	8K x 8	250	40	15
64K Bit	TMM2365P**	8K x 8	200	100	25
64K Bit	TMM2366P*	8K x 8	200	100	25
64K Bit	TMM2368P*	8K x 8	200	100	—
80K Bit	T6436**	8K x 10	350	90	—
128K Bit+	TMM23128P**	16K x 8	200	80	20
128K Bit	TMM23127P**	16K x 8	200	80	—
256K Bit	TMM23256P**	32K x 8	150	40	10
CMOS MASK PROGRAMMABLE ROM					
32K Bit	TC5332P*	4K x 8	450	7	20
32K Bit	TC5333P*	4K x 8	450	7	20
32K Bit	TC5334P*	4K x 8	450	7	20
32K Bit	TC5335P*	4K x 8	450	7	20
64K Bit+	TC5364P**	8K x 8	250	7	20
64K Bit+	TC5365P**	8K x 8	250	7	20
64K Bit+	TC5366P*	8K x 8	250	7	20
256K Bit+	TC53257P**	32K x 8	200	40	20

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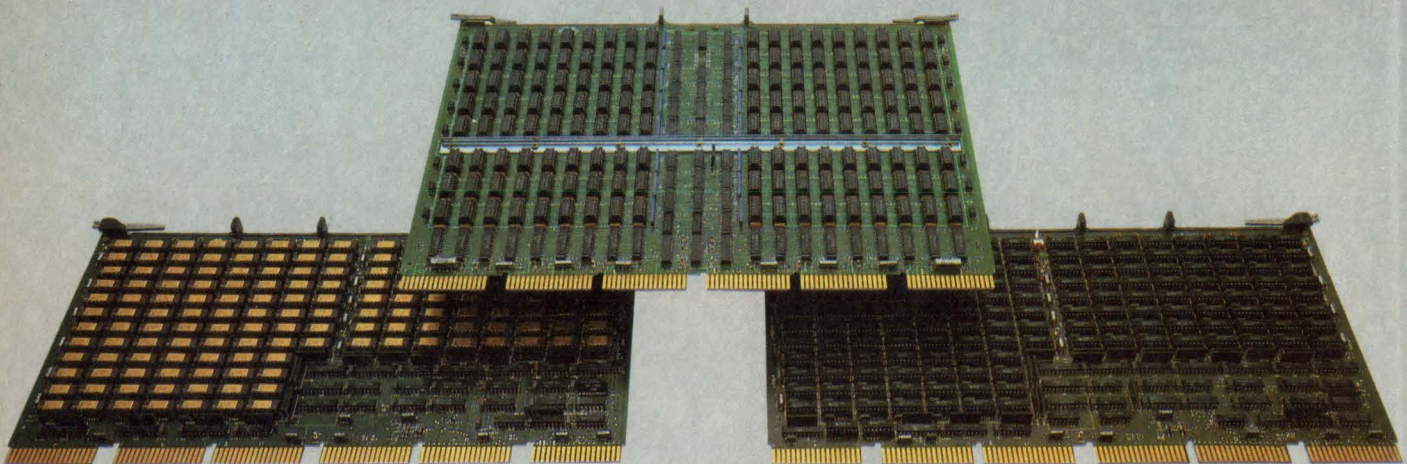
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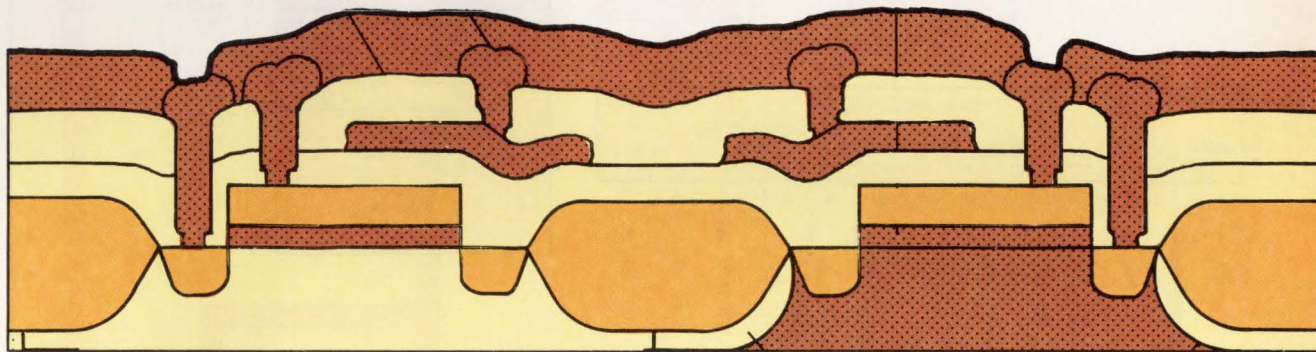
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# CMOS LEADS TO TRUE COMPUTER PORTABILITY

**Denser and faster CMOS VLSI encourages designers to build high performance portable systems.**



by Tony Moroyan

The first generation of "portable" computers can be more properly characterized as transportable. These N-channel metal oxide semiconductor-based systems require hefty power supplies and close proximity to a power outlet. But advances in very large scale integration complementary metal oxide semiconductor technology are paving the way to lightweight battery-operated computers that can be carried and used anywhere.

In fact, due to the greater research and development emphasis the major semiconductor manufacturers are placing on complementary metal oxide semiconductor (CMOS), CMOS could very well become the preeminent very large scale integration (VLSI) technology of the 1980s. CMOS has inherent advantages over the various technologies. These include much greater noise immunity, a wide power supply voltage range, a broad operating temperature range, and the ability to power down in the static state. These CMOS features are critically

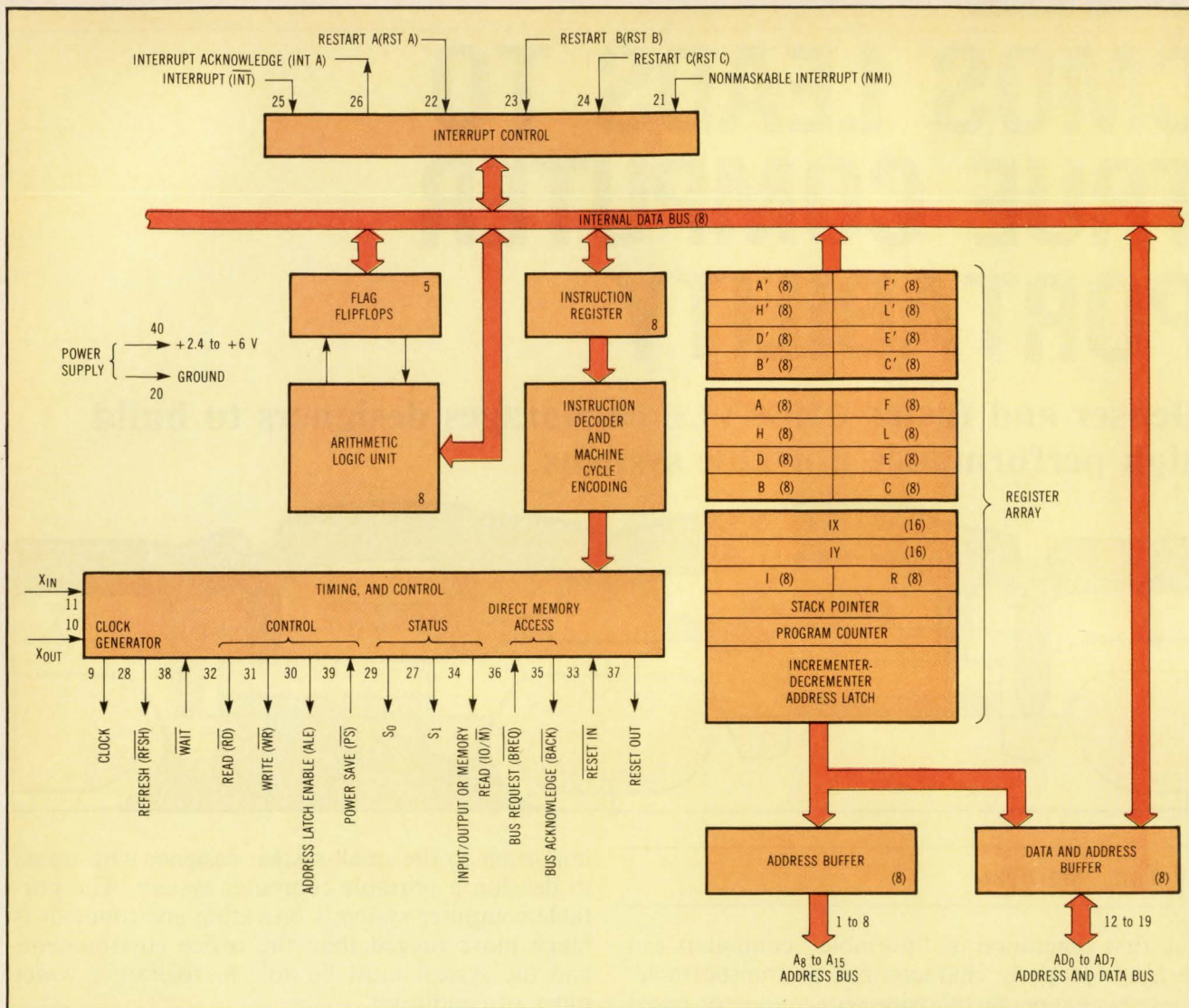
*Tony Moroyan is marketing manager at National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, where he is responsible for CMOS microprocessors. He holds a BA in mathematics and an MS in electrical engineering and computer science from the University of California, Berkeley.*

important to the small-system designer who wants to develop a portable computer system. The portable computer system's operating environment is much more rugged than the office environment, and the system must be able to tolerate a wider range of conditions.

## **A high performance CMOS processor**

For the small-system designer intent on developing a portable computer, the NSC800 CMOS processor incorporates many of the best features of current N-channel MOS (NMOS) devices and provides them in a low powered, easily interfaced package. Internally, it has the identical complement of registers and instruction set as the Z80. Externally, it presents a multiplexed data and address bus like the 8085 processor (Fig 1). It dissipates only 5% of the NMOS device power in its performance class and yet can operate at speeds up to 4 MHz (higher speed and lower power versions of NSC800 are already in design). It is available in a standard 40-pin dual inline package and in special high density surface-mounted packages such as leadless chip carriers for military applications and plastic-leaded chip carriers for commercial ones.

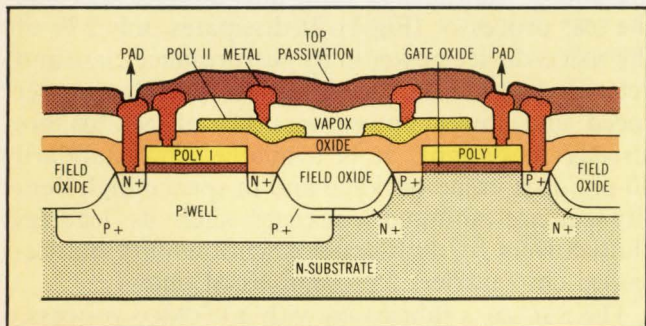
The NSC800 is fabricated with a P<sup>2</sup>CMOS process, one of National's microCMOS processes. This is a silicon gate technology (P<sup>2</sup>CMOS) with two levels of polysilicon and one level of metal for interconnection to provide greater density (Fig 2). Future products



**Fig 1** The NSC800 8-bit microprocessor is fabricated using P<sup>2</sup>CMOS and combines the low power consumption of CMOS with the technology's high performance. It has the Z80 instruction set and register file, but uses an 8085-type multiplexed bus.

will incorporate two levels of metal (M<sup>2</sup>CMOS, another national microCMOS process) for further density improvements. As densities improve, there is a corresponding increase in speed as interconnect resistance is lowered and passive capacitances are reduced. Silicon geometries in CMOS are still larger

than those in NMOS, but are closely tracking their reductions. The NSC800, originally fabricated using 5-micron gate widths, is now designed using a 3-micron width. Devices such as the NS16000 16-bit processor will incorporate less than 2-micron gate widths in their CMOS versions to further improve density and speed.

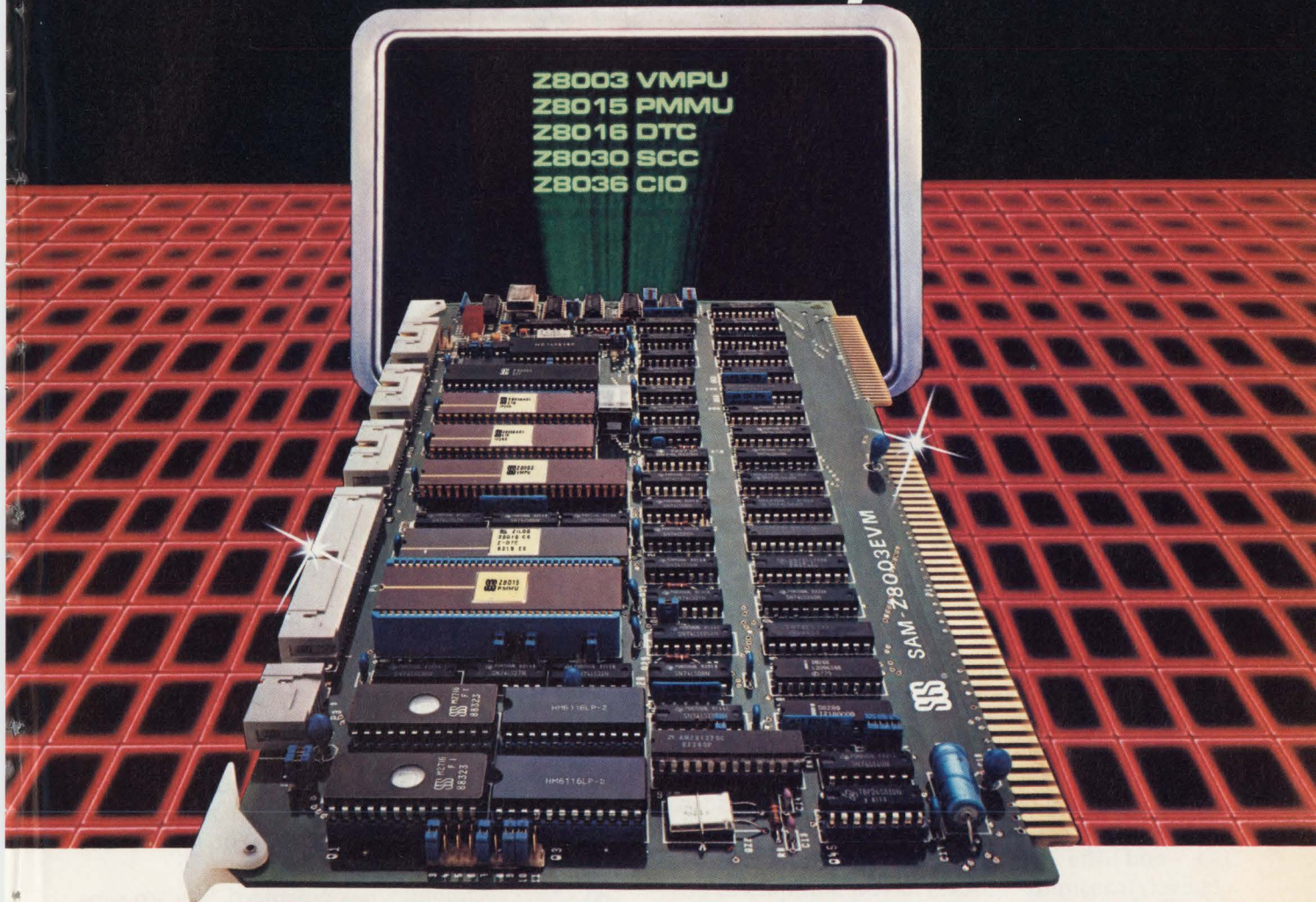


**Fig 2** The P<sup>2</sup>CMOS process uses silicon gates and two polysilicon levels for interconnects. Short channel lengths and thin gate oxide layers provide high transconductance in the transistors.

Z80-based development software, operating system software such as CP/M languages, and application programs will run without modification and speed penalty on a NSC800 system. This is a major advantage for the small-system builder, who can plug into a large existing software base.

With the Z80 architecture, the programmer has 158 instruction types (identical to Z80) with 10 addressing modes, 22 programmable registers, 256 directly addressable input/output (I/O) locations, and a 64K-byte memory address space. In addition, the multiplexed bus frees up pins that permit extra functions not found on the Z80. These include three additional interrupt lines for faster interrupt

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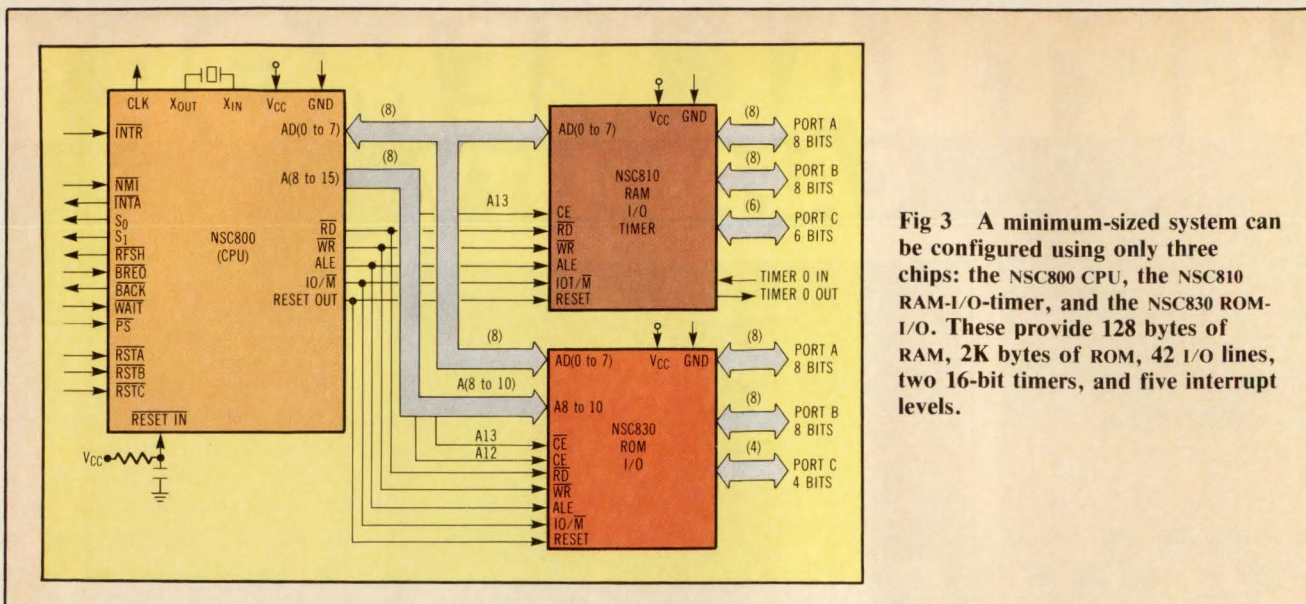


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**Fig 3** A minimum-sized system can be configured using only three chips: the NSC800 CPU, the NSC810 RAM-I/O-timer, and the NSC830 ROM-I/O. These provide 128 bytes of RAM, 2K bytes of ROM, 42 I/O lines, two 16-bit timers, and five interrupt levels.

response times, two special status lines for decoding processor states, an onboard clock generator, and a power-save feature. This last feature further reduces power consumption but can also be used to single-step through a program for debugging.

### Using a multiplexed bus

The multiplexed bus consists of 16 address bits and 8 data bits. The upper 8 bits of the address bus are present on the A8 to A15 lines. The lower 8 address bits are time multiplexed on the 8-bit data bus AD0 to AD7. Systems can be configured that use the multiplexed bus, or the buses can be divided into separate 16-bit address and 8-bit data buses. All NSC800 family components, such as the NSC810 random access memory (RAM)-I/O-timer, the NSC830 read only memory (ROM)-I/O, the NSC831 intelligent I/O, and the NSC858 universal asynchronous receiver/transmitter (UART) have a multiplexed bus structure and thus can interface directly with the NSC800. The address latch enable (ALE) control strobe of the central processing unit (CPU) is used to control bus demultiplex timing.

The advantages of using a multiplexed bus are that it frees up extra pins on the CPU which can be used for other functions and that one third less bus lines are required to interconnect devices. Both of these result in a lower system part count and reduced circuit board complexity. The 8085-type peripherals and many memory devices support this kind of multiplexed bus.

In systems using components that cannot interface directly to a multiplexed bus, the address/data bus must be demultiplexed and divided into separate buses. The 24-pin MM82PC12 is an 8-bit I/O port that can be used to implement latches, gate buffers, or multiplexers. It includes an 8-bit latch with tri-state buffers that have chip selects and control logic. Controlled by the bus acknowledge

(BACK) and ALE pins of the CPU, it provides the low order address bus on separate lines than the low order data bus. A larger system requires bus buffering to drive external components. This can be accomplished with the MM82PC08, an 8-bit bidirectional transceiver.

Using only the NSC800, the NSC810, and the NSC830, a minimum system can be configured (Fig 3). This system would contain 2K bytes of ROM, 128 bytes of RAM, two 16-bit programmable counter/timers, 42 I/O lines, and five interrupt levels. For larger systems, the address lines must be decoded to prevent address overlapping. The MM74HC138 3- to 8-line decoder serves this purpose. As shown in Fig 4, it can be used to decode a 1K x 8 memory array composed of 1K x 4 static RAMs (NMC6514s). These memory components (and the 4K x 1 NMC6504) are designed to be compatible and do not require any demultiplexing logic.

As CMOS technology has advanced, NSC800 support chips, such as the 858 programmable UART with speeds up to 1M bps, the MM74HC942 modem, the MM58167A realtime clock, the ADC0802/44 analog to digital converter, and the DAC0830/32 digital to analog converter have been developed. Furthermore, hundreds of general support chips have been devised (eg, the MM74HCXX series), often pin-for-pin replacements of the common transistor-transistor logic (TTL) "glue" circuits, such as the 74XX family of digital logic.

With their performance characteristics, these devices are replacing bipolar TTL chips in many applications. National Semiconductor, Motorola, Texas Instruments, and most other major semiconductor companies in the mainstream logic business are aggressively second-sourcing these devices. In addition, CMOS gate arrays are reaching densities of 10,000 gates/chip, and many companies are using gate array technology for integrating system support logic. They are also implementing special

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### HM-6616/6616B PRODUCT SUMMARY

Part Number	Size	Organization	Pins	Speed*	Standby Current
HM-6616	16K	2K × 8	24	120 ns	100 μA
HM-6616B	16K	2K × 8	24	90 ns	50 μA

\*Guaranteed over full industrial and military temperature and voltage ranges.

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The multiplexed bus frees up processor signal lines, some of which have been used to provide three more interrupts as compared with the Z80. The standard nonmaskable interrupt (NMI) and the multimode interrupt (INT) are compatible with the Z80, and in mode 0, the 8080. The NMI is used as the highest priority interrupt line and is useful in situations, such as power-fail conditions, where the processor must be alerted for smooth power-down operations. It is also an edge-sensitive input line that causes a direct restart to the memory location 0066 hex.

The INT input has three modes: 0, 1, and 2. Mode 0 corresponds to the 8080 interrupt handling method. An interrupting peripheral places a restart instruction on the data bus. The processor then executes the instruction, usually a call to a subroutine. Mode 1 provides an automatic restart location (0038 hex) so that in small systems, the peripheral does not have to strobe the restart instruction onto the data bus. With mode 2 interrupts, the processor reads a

vector from the interrupting device, which is used with the contents of the I register to create a pointer to the table entry's address containing the interrupt handler routing address. This interrupt is maskable on or off and is controlled by system interrupt enable flipflops internal to the NSC800 CPU. These are software settable as in the Z80.

The remaining three interrupt lines, restart A (RST A), restart B (RST B), and restart C (RST C), provide three different but fixed restart addresses. These are similar to the 8085 interrupts and are also maskable under program control.

Two other extra pins in conjunction with the input/output or memory read (IO/M) line are used for providing the processor's status during each machine cycle—memory read, memory write, I/O read or write, opcode fetch, or bus idle. This information can also be used during hardware development to aid system debugging.

In many applications, power consumption is so critical that it is helpful to put the NSC800 itself into a standby mode where possible. A single power-save input pin suspends CPU operation and reduces power

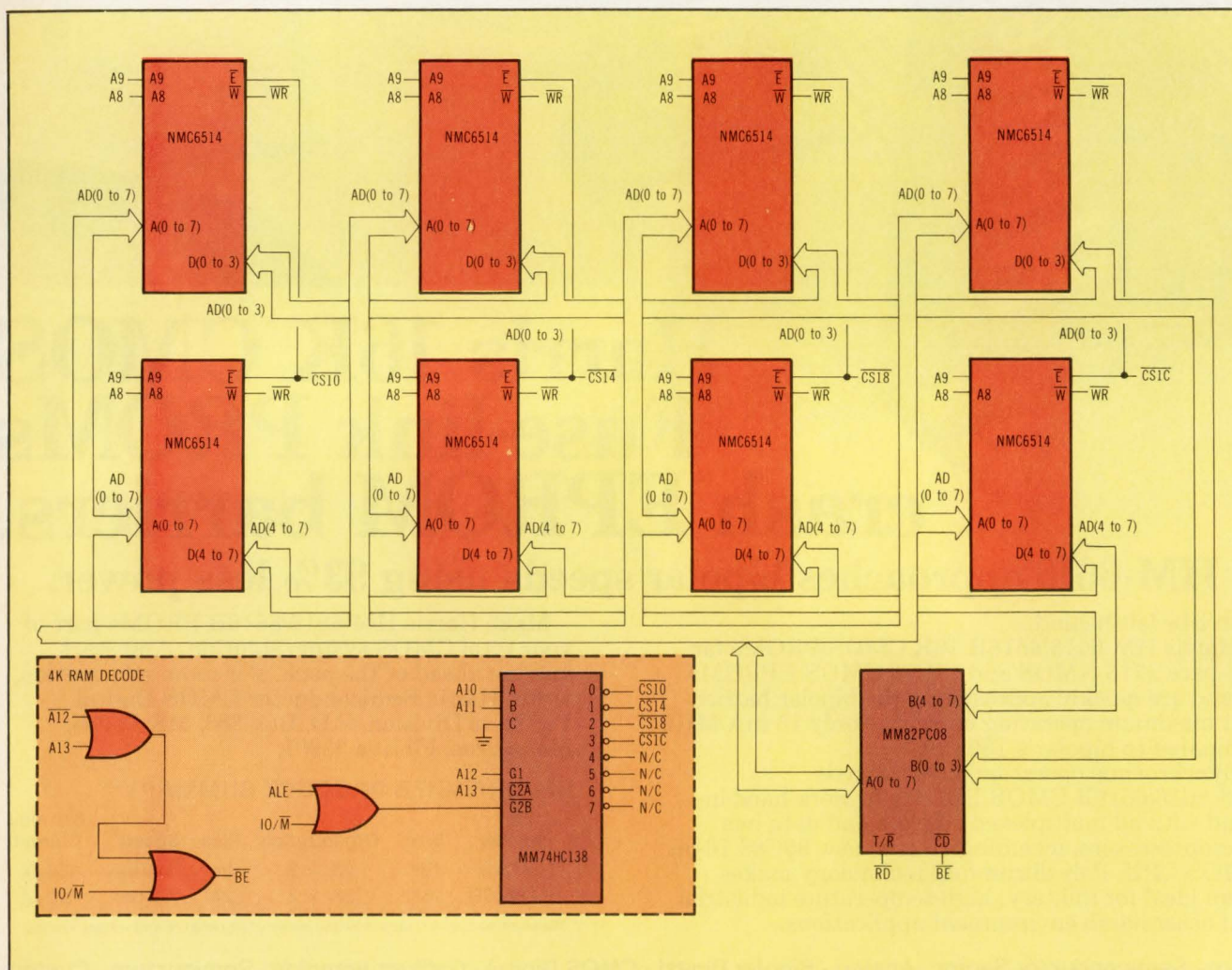
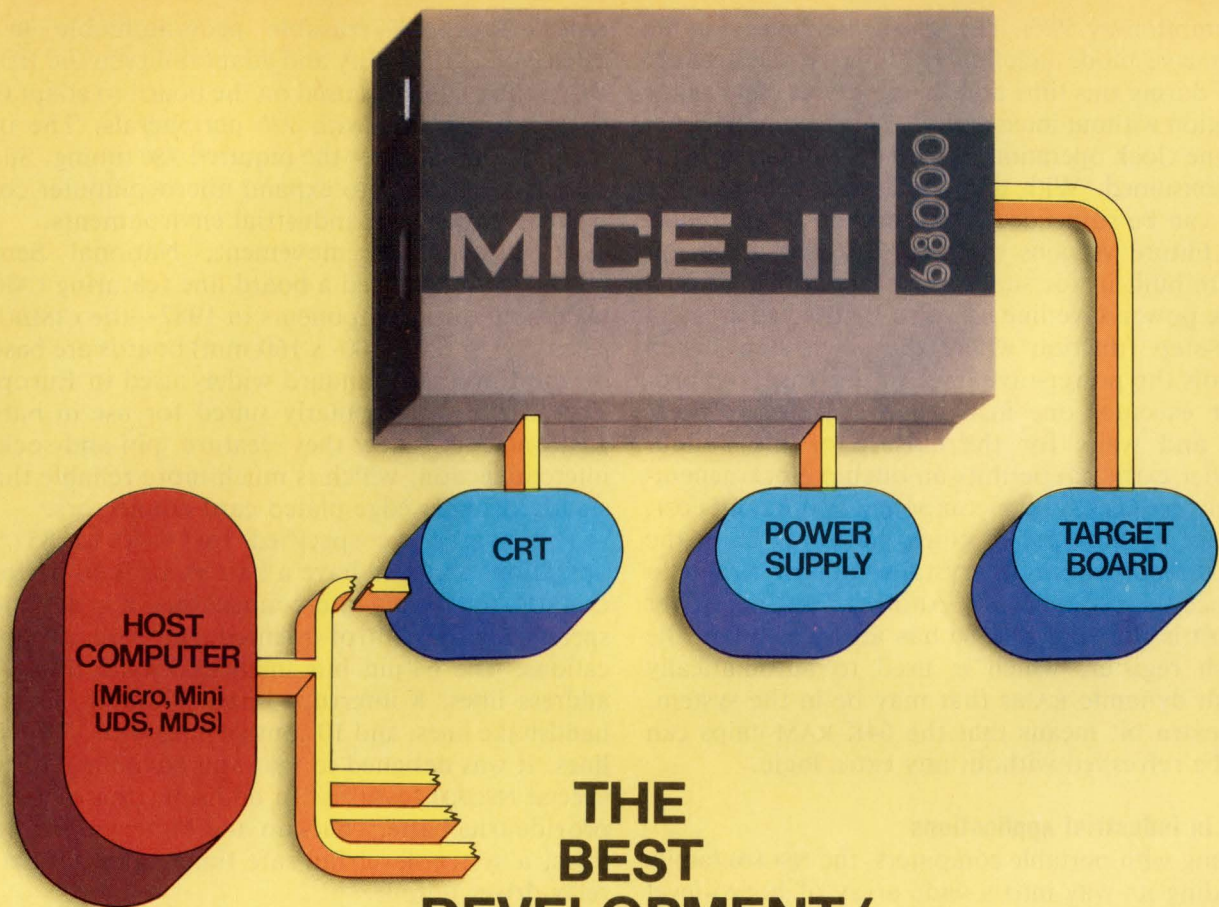


Fig 4 To expand a system beyond the minimal RAM, address decoding logic is required. This is easily accomplished with CMOS parts like the MM74HC138. This 4K-byte memory array shown uses the 138 to generate chip select signals, which in conjunction with the ALE signal, selects the appropriate memory device.



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consumption by 50%. The NSC800 can be held in the power-save mode indefinitely. Internal registers are saved during this time and the processor can resume operation without interruption. This feature does not stop the clock operation, however, so some power is still consumed. With additional circuitry, even the clock can be suspended for maximum power reduction. Future versions of the NSC800 will have this feature built in for super-low power dissipation.

The power-save line can also be used to create a single-step function where the single-step switch controls the power-save line. In this case, the processor executes one instruction, suspends operation, and waits for the closure of the switch. Another extra pin permits an onchip clock generator that reduces system component count and cost. In place of an external clock generator chip, the NSC800 requires only a crystal oscillator circuit to produce the system clock. Another advantage over the Z80 is that the NSC800 has an extra bit in the refresh register, which is used to automatically refresh dynamic RAMs that may be in the system. This extra bit means that the 64K-RAM chips can now be refreshed without any extra logic.

### **CMOS in industrial applications**

Along with portable computers, the NSC800 family is finding its way into a wide array of board-level products. Industrial applications tend to be low power, and require good noise immunity. Thus, it was natural that designers would use the NSC800 in boards designed for rugged environments. Established bus standards like the STD bus are being challenged and complemented by new CMOS specific bus structures like the C-44 and the CMOS industrial microcomputer bus (CIMBUS). Designers have managed to supply NSC800 products that meet a number of applications within these bus conventions.

For example, using CMOS components overcomes the problems inherent in using the STD bus for industrial microprocessor control applications. Although the smaller size of the STD boards (as compared with the Multibus) is important, electrical noise, wide temperature fluctuations, and power outages in industrial sites cause havoc with an NMOS-based system and require a battery backup system.

CMOS-based systems can overcome each of these problems, but they must be compatible with the existing bus signal lines and be entirely of CMOS to obtain the full benefit of the CMOS temperature range, noise immunity, and low power consumption. One company achieving these goals is Baradine Products Ltd of North Vancouver, BC Canada. Its STD-NSC800 board is fully compatible with STD bus timing requirements, uses byte-wide memory components in standard 28-pin configurations suitable for either RAM or ROM, and uses the

NMC27C16 CMOS erasable programmable ROM (EPROM) for flexibility and adaptability in the field. Bus timing logic was used on the board to adapt the NSC800 to operate with Z80 peripherals. The on-board logic simulates the required Z80 timing. Such boards are helping to expand microcomputer control use into rugged industrial environments.

To hasten that movement, National Semiconductor introduced a board line featuring CMOS microcomputer components in 1982—the CIMBUS. These 3.9" x 6.2" (100- x 160-mm) boards are based on the Eurocard standard widely used in Europe. They are also particularly suited for use in harsh environments since they feature pin-and-socket interconnection, which is much more reliable than standard finger edge-plated card connectors.

The boards are specified for -40 to 85 °C operation, and also have a battery backup option. CIMBUS, the system interconnect bus, was designed specifically for control-oriented, run-forever applications. The 64-pin bus includes 8 data lines, 16 address lines, 8 interrupt lines, 5 timing lines, 5 handshake lines, and 10 control lines with 12 power lines. It was designed to take full advantage of the special NSC800 features. In addition, these boards provide true battery backup and battery operation logic, a system-level fail-safe timer, and an alarm relay driver output.

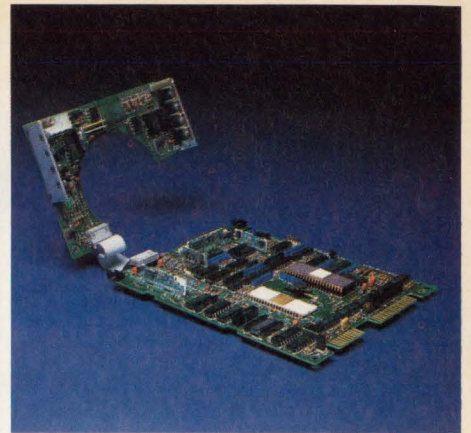
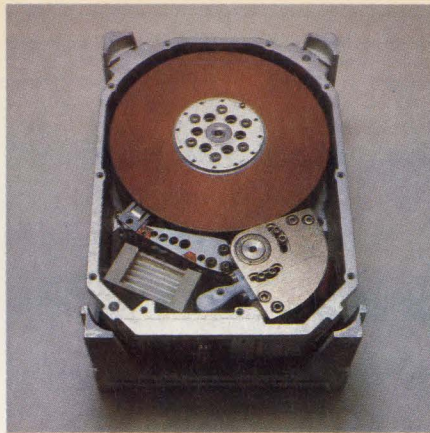
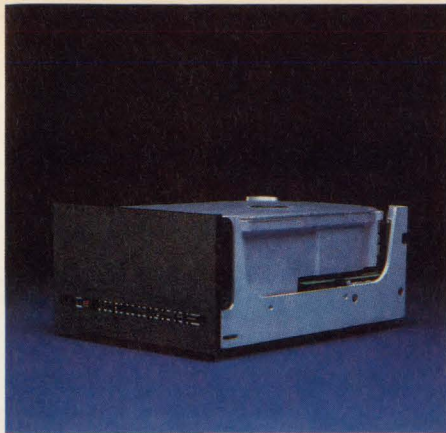
A distributed I/O bus is the isolated interface to discrete I/O devices such as relays, hex keypads, and display/indicators. It simplifies remote I/O handling and eliminates the wiring problems associated with many control applications. The CIM-802 board features a NSC800, 2K or 4K bytes of PROM, 2K bytes of static RAM, two 16-bit counter/timers, 16 I/O lines, support for 8 vectored interrupts, a system level watchdog timer, and 8-ms and 0.5-s timers (Fig 5). The watchdog timer can revive a system that has become inactive due to a CPU failure or program hang-up.

### **Handheld terminals and portable computers**

While portable terminals and computers do not need to withstand the shocks encountered in many industrial applications, CMOS noise immunity and low power offer many benefits. Hundreds of companies are designing CMOS and the NSC800 into portable products of all types. These include handheld terminals, medical instrumentation, videogames, teletext and videotex terminals, telecommunication devices, and military terminals, battlefield computers, and sensing equipment.

One of the more recent introductions was the X-07 handheld computer from Canon (Tokyo, Japan). It boasts a dual-CPU structure with a NSC800 as the main processor, and a custom 8-bit CPU used to control an ASCII keyboard, realtime clock, and the 4-line x 20-character liquid crystal display (LCD). The main unit is merely 8" wide, 6" deep,





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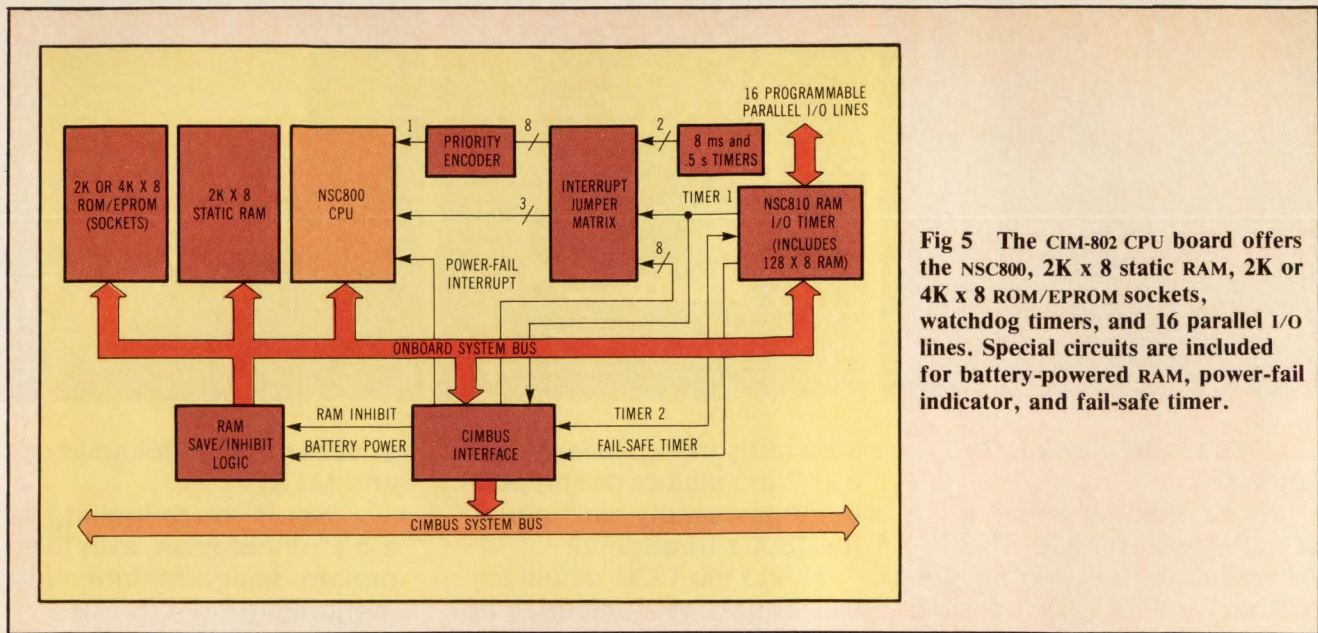
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**Fig 5** The CIM-802 CPU board offers the NSC800, 2K x 8 static RAM, 2K or 4K x 8 ROM/EPROM sockets, watchdog timers, and 16 parallel I/O lines. Special circuits are included for battery-powered RAM, power-fail indicator, and fail-safe timer.

and 1" high (20.3 x 15.2 x 2.5 cm) and weighs 1.06 lb (0.48kg). But in this package it offers the power of the NSC800 CPU, 20K-ROM Basic and monitor, 8K bytes of RAM that is expandable to 24K bytes, a typewriter-style ASCII keyboard, a Centronics-compatible parallel interface, an RS-232-C serial interface, audio-cassette recorder interface, a realtime clock, a miniature speaker, and a system-bus connector for expansion. It is battery operated and has an ac adapter. In addition, it offers a MicroSoft-compatible Basic for high level programming.

The X-07 also features a wide range of accessory computing products such as a miniprinter, a graphics printer, credit card-sized memory expansion modules, an RS-232-C serial communication adapter, a video monitor adapter, and an optocoupler. Through wireless communications, this optocoupler allows the X-07 to transmit or receive programs and messages from other X-07s or peripheral units. Using infrared light beams, it can also be used at distances up to 30' at rates up to 2400 baud.

Another Japanese company, Sanyo Electric (Osaka, Japan), is also marketing a handheld unit small enough to fit in the palm of a hand. The Sanyo HHC includes the NSC800, 16K of ROM, and 4K of RAM. The 64-key keyboard and 27-character display provide basic computer power for in-the-field data collection. An interface unit lets the HHC be connected to four peripherals including a 300-baud modem with acoustic coupler, a small dot-matrix printer, an audio-cassette drive, and an ac power source. In addition to providing substantial computing power in a handheld package, the HHC can be used as an online terminal when connected to timeshare services.

The LEX-31 personal communication computer from Lexicon Corp (Fort Lauderdale, Fla), fea-

tures 16K bytes of RAM and 12K bytes of ROM. A 40-character light emitting diode display and full ASCII keyboard permit portable operation. With its built-in modem, the LEX-31 can be used to dial-up timeshare computers in order to access data bases. The 16K of RAM can be divided into 20 local memory files for holding multiple pages of information. A sophisticated word processing editor allows manipulation of display and internal data. Weighing less than 2 lb (0.9 kg), the LEX-31 operates from rechargeable or replaceable batteries, or 115-Vac power with an adapter. It is a mere 10.5" x 5.25" x 1.75" (26.6 x 13.33 x 4.44 cm) in size.

Of all the portable computers introduced this year, probably the one closest to meeting the needs of the serious computer user is the Athena I from Athena Computer and Electronic Systems (San Juan Capistrano, Calif). The Athena I is a 15-lb (6.8-kg) unit that includes a standard, fully programmable ASCII keyboard and a 4-line x 80-character LCD. More importantly, it offers a substantial amount of main memory organized into a solid state disk and dual-NSC800 processors, one for I/O functions and one central processor.

The system has a 128K- to 1M-byte main memory capacity and supports the CP/M 2.2 operating system, which is installed in system ROM. While the price of a fully loaded Athena I is higher than the first generation of transportable computers (such as the Osborne), it offers a 3 to 10 times performance improvement due to the solid state disk's fast response time. The basic unit has no moving parts and is designed to withstand rugged environments.

Bundled software includes CP/M, JRT Pascal, a spreadsheet program, and a general purpose text editor. The 4-line x 80-character display is handled as a window onto a larger full-sized screen and the user is able to scroll to any desired location. The

combination of Z80 compatibility and the CP/M operating system makes available a wealth of standard business application programs for the system.

In the office, the Athena I can be used as a desktop computer with attached full-screen terminal, modem, plotter, or printer. Accessories include a double-density 5¼" floppy drive, and an ac power adapter/battery charger. A proprietary networking link permits up to 15 Athena I systems to link together in a local area network. A 30M-byte hard disk subsystem is available to allow networked units to share common data files.

Athena I's power becomes apparent when you leave the office, however. The batteries can operate the system for up to three hours and will retain the mass memory for up to six hours in the field. Of course, the ac adapter can be used as well as the 12-V power cable for operation from an automobile cigarette lighter receptacle.

Internally, the system is comprised of three modules. The first is a NSC800 processor board with a 4-MHz NSC800. The second is a communication module with another NSC800 and dedicated communication buffer space, LCD interface, two RS-232 serial ports, a parallel I/O port, and a floppy disk interface. The third module is the expandable dynamic RAM card with a 1M-byte maximum memory size. The computer is designed in a very

modular fashion and even the memory expansion is achieved through easily handled and carried modules. There is also a spare circuit board slot for future expansion.

While only a small percentage of the present Athena design is CMOS, the company expects it to be almost entirely CMOS within a few months. The major circuit exceptions will be the dynamic RAM chips and the mass storage device controllers. What is driving the development of such powerful portable computers is the availability of standard CMOS processors and support circuits, in addition to the industry commitment to produce more powerful CMOS processors in the future. As CMOS technology continues to be refined and scaling approaches the sub-2-micron level, even more powerful processors such as the NS16C032 and NS32132 (full 32-bit CPU) will become available in CMOS, as well as denser memories that will make even more impressive systems possible.

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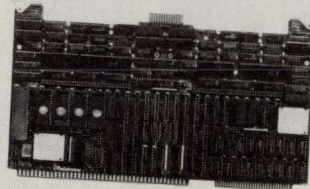
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# OCCAM ARCHITECTURE EASES SYSTEM DESIGN —PART I

**Software development is simplified by constructing a language—Occam—suitable for the description of multiple processor systems.**

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**by Pete Wilson**

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*In the first of a series, this article introduces Occam as a language-based approach to system design and implementation. Occam's suitability for constructing complex systems will be demonstrated by walking through the language's design steps.*

Language-based architectures help simplify complex multiprocessor system software. The Occam language, a recent and well-publicized example, was designed to promote such simplicity. It was named after William of Occam's famous postulate—Occam's Razor. This postulate states that the simplest solution explaining all observable phenomena is the right one. Although it does not claim such universal applicability, Occam does simplify complex system design.

With the proliferation of computer systems in all facets of society, multiprocessor use has also increased. Add-on processors for personal computers, distributed systems connected by networks, and tightly-coupled systems involving tens of pro-

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*Pete Wilson is microcomputer applications manager at Inmos Corp, PO Box 16000, Colorado Springs, CO 80935. He holds a BS in physics and mathematics from Sheffield University, England.*

cessors and array processors are all reasons why the number of systems built with several computers is increasing. In addition, many such systems include intelligent subsystems, where a local processor acts as a dedicated controller for some system resource.

The number of multiprocessor systems is expected to increase even more. New system architectures such as the fifth-generation projects being pursued in Japan, Europe, and America will necessarily rely on highly concurrent hardware. Very large scale integration (VLSI) technology will also make microprocessor-based signal processing, image processing, and true array processors economically attractive.

## **Structuring the language**

There are many possible topologies (network, bused, starred, tree, array, etc) and interconnection technologies (shared store, multiple buses, local area networks, point-to-point connections, and vector arrangements) for multiprocessor systems. Because their experience is limited to the design of the relatively simple sequential system software, the advent of concurrency may seem like a mixed blessing to system designers. With hundreds of millions of instructions per second of computational power available, how should the processors be connected and programmed?

There is hope, however, since characteristics common to all these systems allow a coherent engineering discipline to bear on the problems of design, implementation, and use. Such commonality allows the construction of formal system description tools to define and describe all such systems. Thus, computer aided tools for description, simulation, and construction can be built.

The situation becomes tractable if the search for the design rules is limited to methods for designing connected computer collections. Systems are formed by connecting computers using their input/output (I/O) facilities. This approach is a building block style, with computers as the building blocks. It matches VLSI technology's capabilities since it is now straightforward to put a complete computer on a chip.

Formalizing this model of system design is the next step. Here, choice of primitives is crucial. The wrong choice can lead to a formalism that is not useful because it embodies either too many assumptions, which limits its applicability, or it is too distant from the real world.

Because the primitives must reflect the informal model's components, one should be able to recognize a computer, with memory and I/O, in the structure. In a system, however, different memory, I/O capabilities, and various computer connections must be representable. Consequently, the model has three primitive objects: computers, memory, and I/O.

*Variables* represent the contents of a computer's memory. A number of *channels* represent the I/O. Computers can be connected by running a channel from one to the other, making arbitrarily large systems of any describable topology. The computer itself is represented by a *process*.

To use the resources in the model, variables must be manipulated and values must be communicated through channels. Normal arithmetic and logical operations are appropriate for manipulating variables. Choosing I/O operations, however, is more difficult. Communication primitives should be simple and direct, allowing whatever choice of buffering, high level request/acknowledge, error recovery, routing, or flow control the application calls for.

Choosing a simple, unbuffered synchronized I/O operation fulfills the requirements. In general, two separate computers will be unsynchronized. Some handshake is necessary for them to communicate. The model chosen is a handshaken data transfer of a value down a channel. One process (computer) outputs, the other inputs. The computer that acts first halts operations until the other one acts. The value is then copied from the outputting process to the inputting process, and both continue.

To describe the behavior of computer collections, it is necessary to identify some computers and define how they work together. Limiting these operational modes keeps things simple. Three major modes are sufficient: the computers all act together; they act one after the other; or just one of them is chosen to act. In addition, convenience dictates some method of requiring computers to act repetitively and conditionally. Putting these methods together and choosing a simple syntax establishes the desired formalism.

For example, a fixed-length pipeline of machines could describe a collection of computers working together to do a Newton-Raphson (NR) square root. Each machine will accept input, do a step to provide a better approximation to the root, and then output that value to the next element in the pipeline. The behavior of one computer in the pipeline illustrates this. It has an input channel *in*, an output channel *out*, and some memory containing variables *x* and *estimate*. It must first input values from *in* to *x* and *estimate*, then perform some computation, output the new value of *estimate* to *out*, then be ready to accept the next numbers.

The operation of input, computation, and output can be written as follows:

```

SEQ
  in ? x
  in ? estimate
  estimate := (estimate +(x/estimate))/2
  out ! x
  out ! estimate

```

The key word, SEQ, in the syntax chosen introduces a collection of processes and describes how they are to execute sequentially. Indentation shows the extent of the collection—everything at the same level of indentation belongs to the same collection. The collection ends when the indentation level goes back out again. The text means that this is a collection of processes which will act in the order they are written: input from channel *in* and put the result in *estimate*; compute a new value for *estimate*; output *x* to the channel *out*; and output the new value of *estimate*.

The text can be simplified to:

```

SEQ
  in ? x, estimate           -input x then estimate
  out ! x, (estimate+(x/estimate))/2-output x then new estimate

```

Because the computer is supposed to repeat this, the user can specify the following:

```

WHILE TRUE
  SEQ
    in ? x, estimate           -input x then estimate
    out ! x, (estimate+(x/estimate))/2-output x then new estimate

```

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In describing the complete pipeline behavior, each cell does the same things, but the channels differ. Describing a cell by a shorthand parameterized notation is convenient, because multiple copies of the same cell with appropriate parameters can be called up. The syntax for this is straightforward.

```
PROC nrstep (in, out)=
  WHILE TRUE
  SEQ
    in ? x, estimate           -input x then estimate
    out ! x, (estimate+(x/estimate))/2-output x then new est.
```

Now the complete collection can be described (for a 5-deep pipeline), as shown below.

```
PAR
  nrstep (in, link0)
  nrstep (link0, link1)
  nrstep (link1, link2)
  nrstep (link2, link3)
  nrstep (link3, out)
```

This reads as a collection of processes (computers) acting in parallel. While channels link0, link1, link2 and link3 are specified explicitly, it would be convenient to describe structured collections of channels and processors parameterically. (While explicit specification here is relatively easy, describing a 1024-point fast Fourier transform machine would be tedious.)

The common notion of a variable which is an array can be extended simply to both channels and processes. For simplicity, this article looks at 1-dimensional arrays (vectors). The vector of channels in the preceding example has a name (link) and a size (4). Individual channels can be accessed as link[0], link[1], etc. Before using such a collection, it needs to be introduced with a declaration.

```
CHAN link 4 :
```

(In the earlier examples, we should also have declared the individual channels and variables.)

A collection of processes may act concurrently, in sequence, or selectively. In building vectors of processes, these capabilities must be maintained. To describe a parallel vector of processes, one can write the following:

```
PAR i = 0 FOR size
  nrstep(link [i], link [i+1] )
```

This has exactly the same meaning as writing out:

```
PAR
  nrstep(link [0], link [1] )
  .
  .
  .
  nrstep(link [size-1], link [size] )
```

The complete description of the NR approximator is as follows:

```
PROC nrstep(CHAN in,out)=
  VAR x:
  WHILE TRUE
  SEQ
    in ? x, estimate           -input x then est.
    out ! x, (estimate+(x/estimate))/2-output x then new est.

  CHAN link 5 :

  PAR i= [0 FOR 4]
    nrstep (link [i], link [i+1] )
```

Value pairs, representing numbers and first approximations to their square roots—eg,  $x/2$  as an approximation to  $\text{sqr}(x)$ , are fed into channel link[0] with results coming out of link [5].

Using these elements, any collection of connected computers can be described. Explicit declarations enumerating the connections allow irregular topologies to be defined. Using computer and channel vectors quickly describes structured collections (eg, arrays or trees). The constructors (PAR, SEQ, etc) and their vector variants (the replicators) can be nested to any depth, since a collection of computers (processes) behaves exactly like a computer. A 2-dimensional array of computers is defined:

```
PAR i= [0 FOR xsize]
  PAR j= [0 FOR ysize]
    .
    .
    .
```

These descriptions are not just paper exercises. It is easy to write a translator to convert the descriptions into a form executable on any real computer; then the descriptions can be run providing a simulation of the system. To execute such a description on a computer, a method is needed to multiplex it between the processes in the description, and to implement the communication. This may be achieved using a kernel containing a round-robin scheduler for the multiplexing, and short code sequences to provide message passing. Typically, the complete kernel will need less than 100 instructions. The translator then arranges for the invocation of the kernel facilities when needed.

This formalism is not limited to just describing systems constructed from collections of computers. It is also appropriate for describing generalized hardware subsystems where various components operate together and communicate. For example, a processor design can be constructed with the pipelined activity of instruction prefetch, decode, and execution units clearly laid out. Executing this description yields an efficient design simulation. Large and complex systems with mixed components





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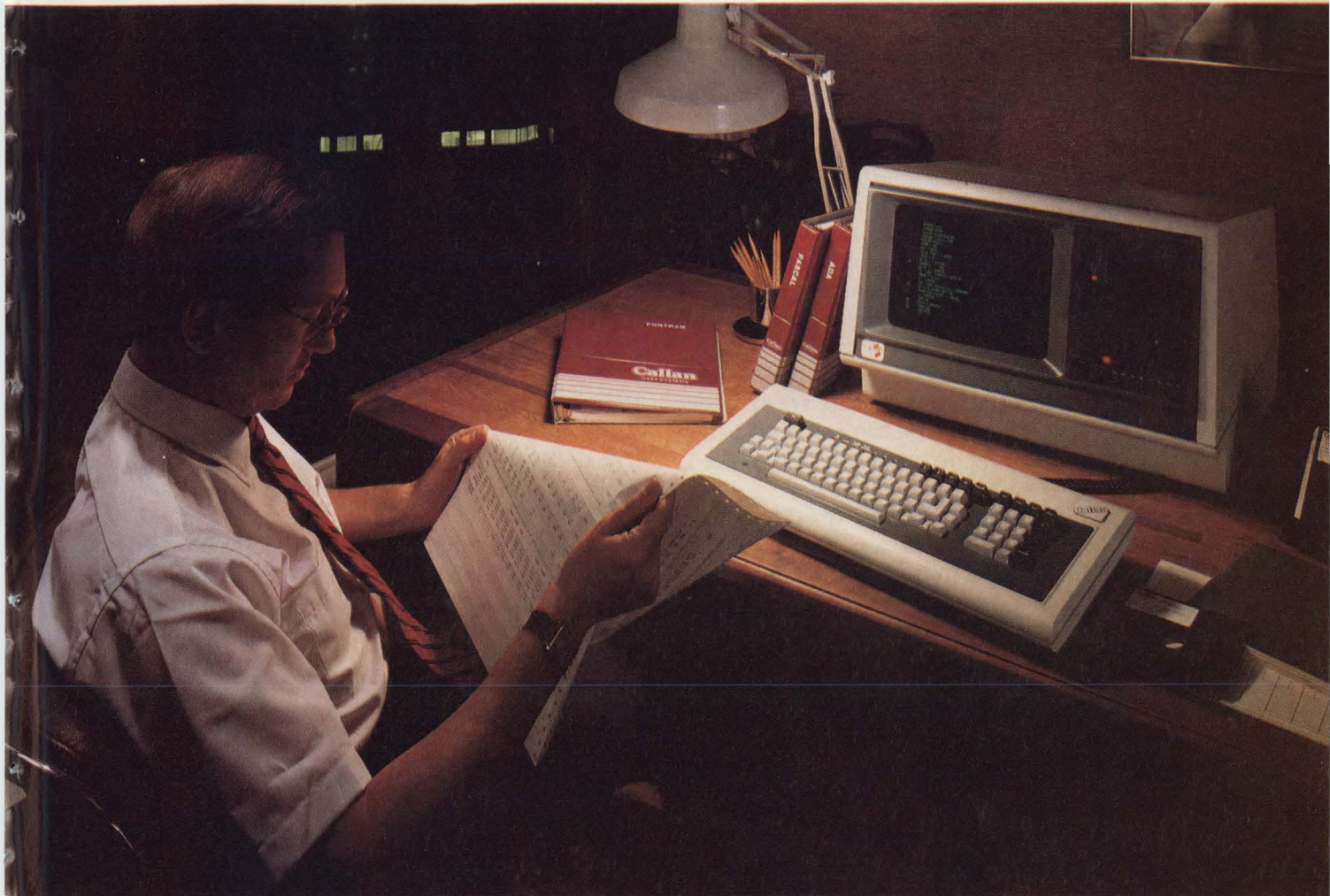
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can also be described, including human beings and sensors.

Using the formalism, it is possible to describe not only the gross behavior of the collection of computers, but also the behavior of the programs they are executing. This opens up the possibility of designing a complete system inside one framework. In addition, the boundaries between operations to be implemented by special hardware (eg, a special purpose processor) or by software can be shifted towards the end of a design. Those parts of the system to be implemented in hardware are given a formal specification by their Occam description. To implement the software part of the system, the appropriate portions of the Occam description merely need compiling into executable code.

When the language was limited to describing a system's behavior, it was possible to ignore mapping details—in particular, which physical intercomputer links were which channels, and which collections of processes were to be multiplexed onto which real computer. When used as an implementation language as well as a definition language, these facets must be addressed. Priority scheduling—for interrupt handling and user set priorities—must be considered. Thus, the constructors are extended to encompass priority and placement, and a new key word is introduced to map physical links to logical channels.

Various compilers currently exist for Occam, targeting simple language evaluation, serious system simulation, and real multiprocessor implementation needs. For evaluation purposes, a simple compiler-editor that runs on the UCSD p-System, generating p-Code, is available for many machines (eg, the IBM PC and the VAX). For design simulation, a VAX-based system generating VAX native code is available. And for multiprocessor implementations, the VAX software with a cross compiler for the 8086 (soon for the 68000 and the Inmos Transputer) family microprocessors is available; or a workstation-based product with the same facilities exists.

### Occam in simulation: a processor description

Occam's use in the design of a new 16-bit microprocessor illustrates its functionality as a design and simulation tool. The microprocessor is not complex, with just an accumulator and a workspace register. The instruction set is simply encoded—all instructions are one word long, with a 1-byte opcode followed by a 1-byte operand. The machine does arithmetic between the accumulator and a value specified by the operand, either a literal or a memory location whose offset from the workspace register is specified. Other instructions provide indirection and relative branches.

To increase performance, the processor is pipelined. An instruction prefetch buffer is followed by

an instruction decoder (which will fetch operands from memory as necessary), an execution unit, and an operand write unit. The prefetch, decoder, and operand write units contend for use of the memory subsystem. When a jump occurs in a real machine, the pipeline must be flushed in a sanitary fashion; when operand reads are done, an interlock with operand writing is required. For simplicity, only parts of the design are shown here. From the top level of the processor as a collection of connected units, the Occam description of the machine can be written as shown below.

```
CHAN mem.fetch,      -path from memory to fetch, for instructions
  fetch.mem,        -fetch to memory, for addresses
  decode.fetch      -path from prefetch buffer to decoder
  mem.decode,       -path from memory to decoder, for data fetch
  decode.mem,       -decoder to memory, for addresses
  execute.decode,   -path from decoder to execution
  write.execute,    -path from execution to write
  write.mem1        -path from write to memory for data write
  write.mem2        -data read address
  mem.write:        -memory to write for data

PAR
  fetch
  decode
  execute
  write
  memory
```

The decoder inputs single instructions and looks at the opcode. If it is an operation giving input to the execution unit (eg, load variable, load literal, add literal) the decoder creates two message words—a modified opcode in one word, followed by the value. For write operations, two values are again sent: the first unmodified opcode; the second unmodified operand.

```
PROC decode=
  VAR instruction
    opcode,
    operand:
  WHILE TRUE
  SEQ
    fetch.decode ? instruction      - get instruction from fetcher
  PAR
    opcode:=instruction>> 8         -this can be done in parallel
    operand:=instruction/\255
  IF
    opcode 127                     -then decode opcode
    opcode 127                     -if not a load instruction
    decode.execute ! opcode, operand
    opcode = add.literal            -typical literal operation
    decode.execute ! add,operand   -send "add" opcode and opnd
    opcode = add.variable          - typical of
    SEQ                             workspace instructions
    PAR
    SEQ
    decode.mem ! W+operand         -get value from workspace
    mem.decode ? operand
    decode.execute ! add           -..send opcode in parallel
    decode.execute ! operand      -then send value
  .
  .
  .
```

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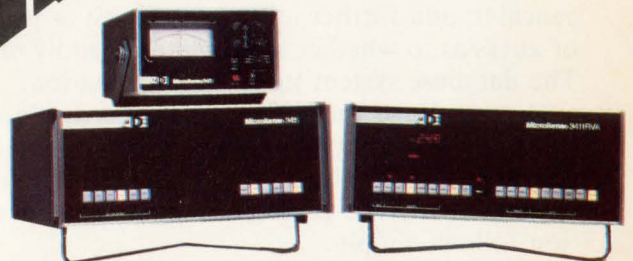
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The execution unit is clear-cut—it always expects two input values from the decoder. The value is ready to use for input operations, but not for write operations (the write unit will use it).

```

PROC execute=
  VAR accumulator,
      opcode,
      operand:
  WHILE TRUE
    SEQ
      decode.execute ? opcode, operand
                          -get opcode and operand from decoder
    IF
      opcode > 127      -pass writes through to write unit
        execute.write ! opcode, operand, accumulator
      opcode = add      -deal with others
        accumulator:=accumulator+operand
      opcode = load
        accumulator:=operand
    .
    .
    .

```

### Occam as a system description language

An example of the type of complex structure, describable by Occam is an action information organization (AIO) system used for naval command, control, and communications. An AIO system captures data from warship sensors, collates and processes the results to form a picture of the situation, and constantly updates this for its users. It consists of a heterogeneous set of components—radar and sonar systems, computers, software, radio links, screens and keyboards, and people. Some elements can migrate from software to hardware as technology changes. As functional requirements increase in flexibility, some may move from dedicated hardware to software. A single description of the whole system can ease this movement.

In a typical AIO system, surveillance radar outputs are digitized and fed through a pattern recognition box that searches the return for target-like patterns. Output is fed to a correlator, which attempts to match any detections with predicted positions of targets already known to the system. When the correlator finds a return it cannot correlate, it will create a new target and inform the operator. The operator can then ignore the action, confident that the system knows what it is doing; cancel it; add further information such as priority; or guess as to whether the target is friendly or not. The database system stores all information.

Occam allows the actions of the hardware, software, and human components of the system to be described. From the top level description of the radar system, the corresponding Occam description follows simply.

```

CHAN
  ...list of all inter unit links

PAR
  radar      -scans
  digitizer  -digitizes radar returns
  detector   -looks for signals in digitized returns
  correlator -compares detections with predictions
  human      -gets told infor to which (s)he may respond
  database   -holds all information

```

As far as the other components of the system are concerned, human behavior is considered part of the ordinary process. Thus, information is output to the user (presumably using a screen or other comprehensible method), where it will be processed using (hidden) algorithms. The system does not care what these algorithms are: the results of the processing, reflected in the messages the user chooses to send to the system are what affect it.

*As functional requirements increase in flexibility, some may move from dedicated hardware to software. A whole system description eases this.*

This is an example of the behavior of a process being specified only in terms of the messages sent or received by it. The internal workings are hidden, and may be changed without altering the specification of the system containing the process. In a real AIO system, there may well be some procedural rules that a user must obey before acting, but these will not be discussed here; if such rules do exist, then the “human” process may be expanded to deal with them.

Human involvement can be shown in the Occam description as shown in the example.

```

PROC human=
  VAR new.target.ident,
      result:
  WHILE TRUE
    SEQ
      dbase.human ? new.target.ident
      think.about (new.target.ident, result)
    IF
      result=cancel
        human.dbase ! cancel, new.target.ident
      result=moreinfo
        human.dbase ! update, new.target.ident, moreinfo:

```

For an accurate picture, the item *moreinfo* needs some expansion. The process *think.about* represents the hidden operations the operator uses to contemplate received information and to conclude what, if anything, to do about it.

*Occam's Razor claims the simplest solution explaining all observable phenomena is the right one.*

The database process is connected to all information generating or needing processes. It receives the message from the correlator instruction to create the new track, and informs the user of the event. Because it wants to maintain database integrity, it will only accept one request at a time from all connected processes.

```

PROC database=
  VAR request:

  SEQ
  initialize
  ALT
  correlator.dbase ? request
  IF
  request = newtrack--message from the correlator
  SEQ
  PAR
  correlator.dbase ? trackinfo [0 FOR record.size]
  dbase.human ! newtrack.number
  write (trackinfo, newtrack.number)
  .
  .
  .
  human.dbase ? request--message from the human
  IF
  request = cancel
  SEQ
  human.dbase ? track.number
  cancel (track.number)
  request = update
  SEQ
  .
  .
  .
  
```

While describing Occam's design and looking at some programming examples is instructive, it leaves many questions unanswered. Part II and Part III will address the problems of designing for concurrency and establishing Occam channels in hardware.

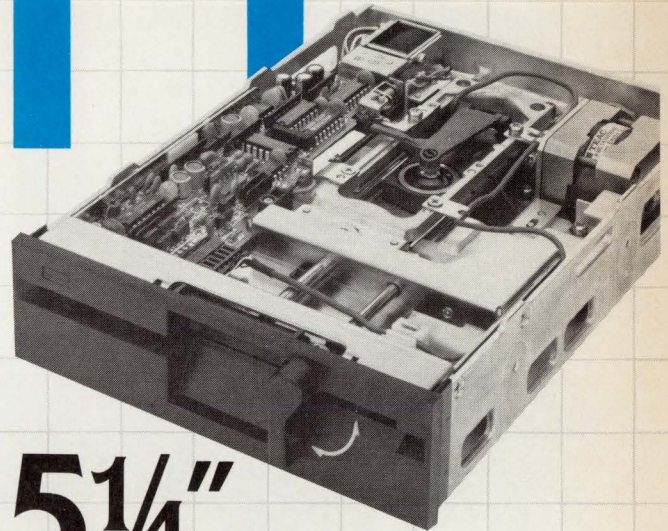
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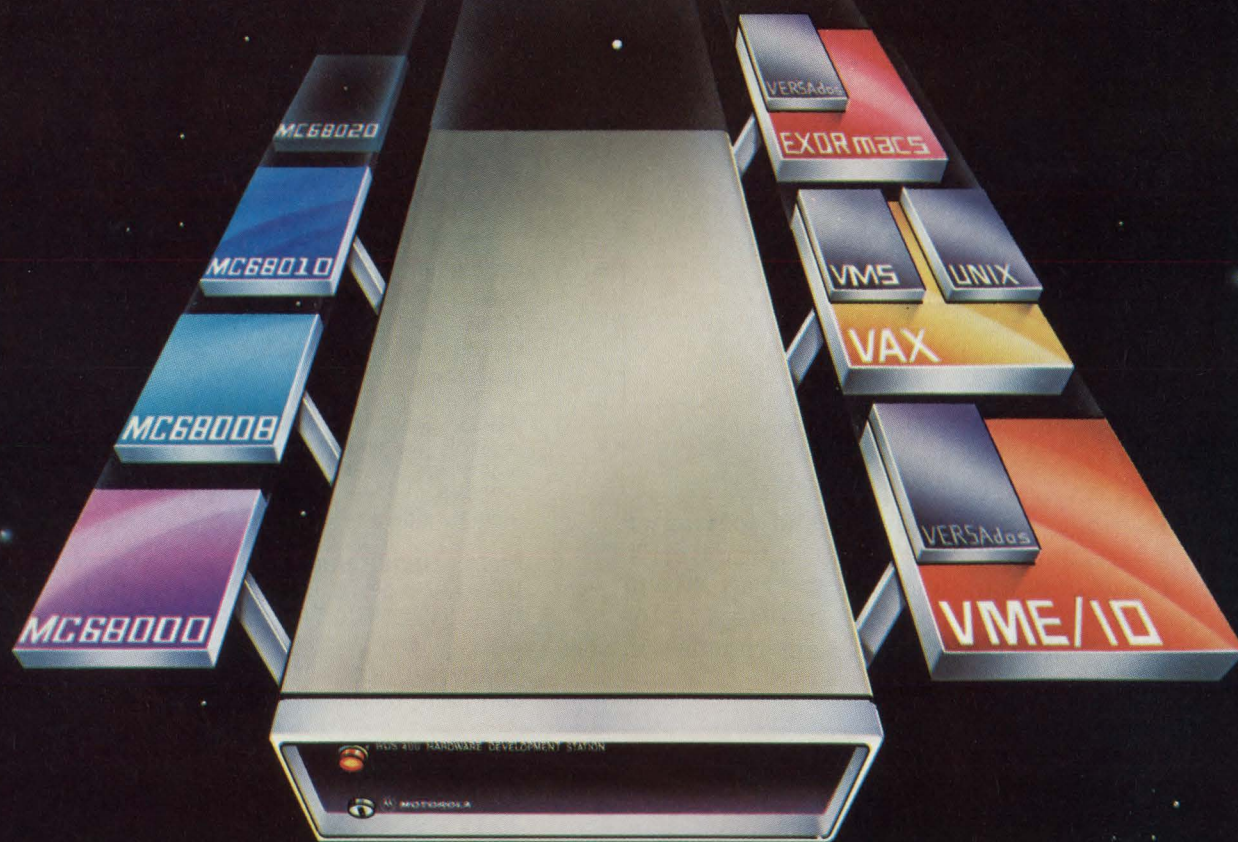


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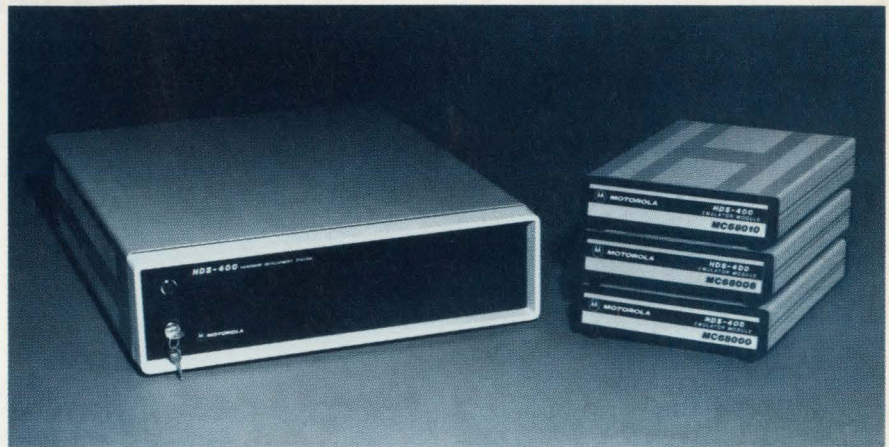
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# DATA HIGHWAY PROVIDES DATABASE MANAGEMENT

With the industrial environment, a high performance network prevents degradation of distributed control processing.

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by Kirk D. Houser

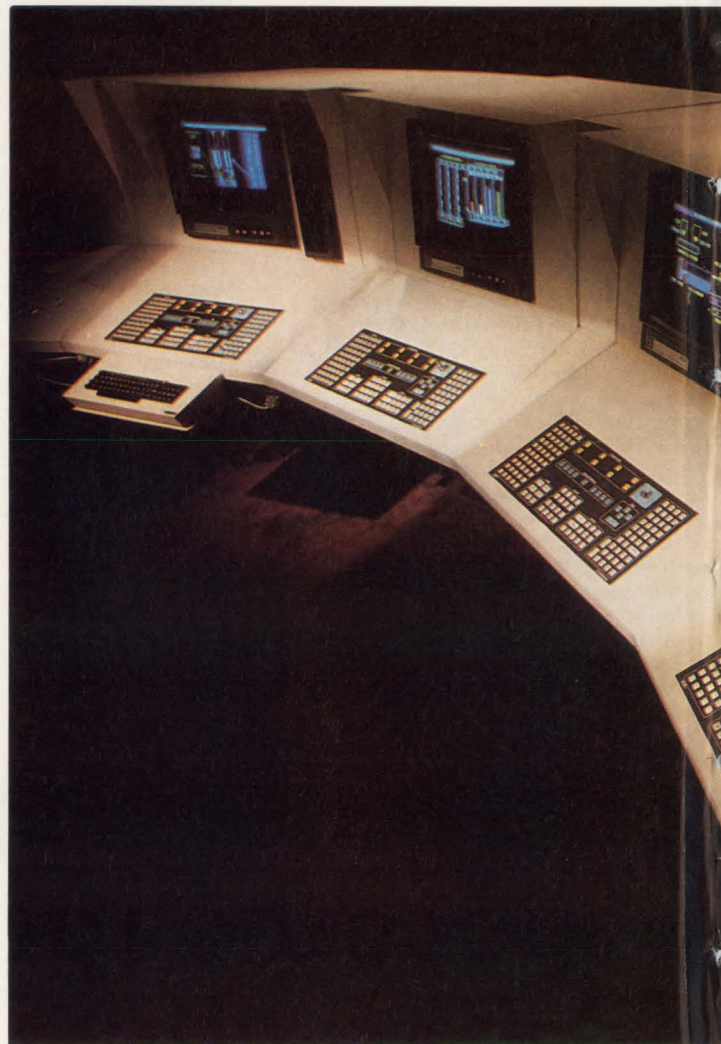
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The communication medium is the heart of a distributed process control system. Not only must it update information every second, but it must be instantly available for use by operators in monitoring plant status, changing tuning parameters, and performing manual control. Previous radial and linear networks did not address these requirements and allowed cathode ray tube display station updates and control loop processing to degrade under worst-case plant conditions. A truly effective data highway must provide these features while also addressing system redundancy and reliability.

The key to providing an effective system is transparency between the distributed microcomputers (drops) and the data highway. Each drop must concentrate on its assigned task and remain independent of other system events. To achieve this level of isolation, the data highway must provide the system's database management. This allows drops to obtain information regardless of origin, thus greatly reducing system software complexity.

One method previously used for moving information from one drop to another was to send multiple-directed messages containing the information to

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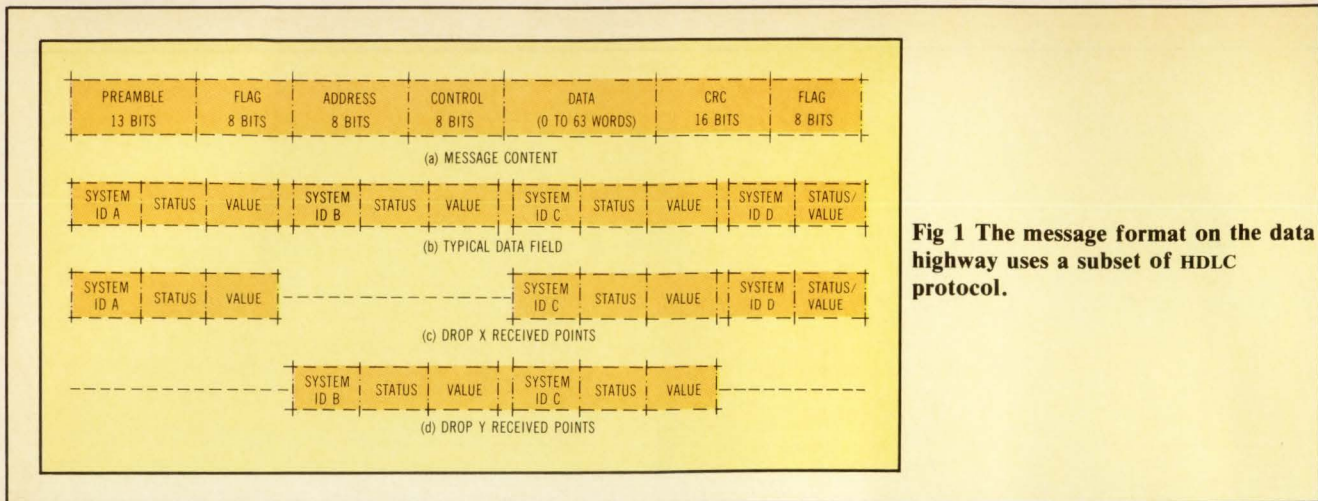
each drop. Because noise or hardware malfunction could cause message loss, each receiving drop had to acknowledge the receipt of a message so that it could be re-sent if necessary.

A better alternative to directed messages is the broadcast technique. In this method, each drop broadcasts all pertinent information over the serial communication link. All other drops listen to all information being sent and retain only the information that they need. Thus, every drop functions either as a broadcaster or a listener at any time. A major added benefit is that a drop does not need to know where its transmitted messages go or where its received messages originate.

#### **Data highway communication**

The data highway uses a subset of the high level data link control (HDLC) protocol. Only the basic format is used, and the definition of the address and control fields and various network arrangements are different. The serial transmission block has seven components: the preamble, the opening flag, the address field, the control field, data (0 to 63 words), the cyclic redundancy check (CRC) word, and the closing flag. Data are transmitted at a 2M-bps serial rate. Biphase Manchester encoding provides a self-clocked waveform free of dc components. Fig 1(a) outlines the standard frame format.

The preamble has a mark of approximately  $2.4 \mu\text{s}$  followed by 8 biphase zeros. This enables the drop's transmitter, and properly synchronizes the phase-lock loop in each receiver. Opening and closing flags use a special synchronizing character, ('7E 'H), to

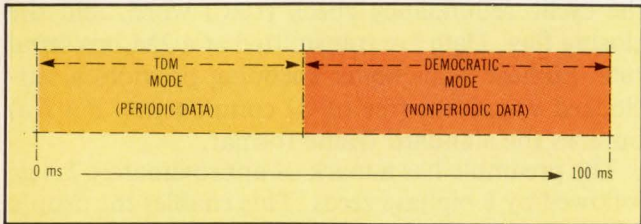


**Fig 1** The message format on the data highway uses a subset of HDLC protocol.

define the beginning and end of the HDLC frame. Zero insertion and deletion prevent this unique pattern from recurring in the remainder of the message. The address field specifies the index into the current bus allocation list of the next drop to transmit. The control field determines the current message mode, the next frame's message mode, whether a recovery is needed because the previous handoff was unanswered, or if an abnormally long inactive period was detected on the data highway.

The data highway uses two different modes of operation: the time division multiplexed (TDM) mode and the democratic mode. These modes are repeated every 100 ms on the highway, and support periodic and nonperiodic data, respectively (Fig 2). During the TDM portion of the 100-ms cycle, each drop transmits its periodic information. The originating drop may designate specific information for transmission at regular intervals of either 100 ms or 1 s. The 1-s period is adequate in data acquisition applications, while the 100-ms period is often required for interlocks between distribution control loops.

For information that a drop does not originate but needs to receive, there are table entries directing the data highway processor to receive the transmitted information and update the local copy of the element's attributes in shared memory. The data highway processor also notifies the drop's microcomputer (the functional processor) if any elements being received fail to be updated during a period approximately equal to three times the expected transmission interval.



**Fig 2** With the data highway, two modes of operation, TDM and democratic, are used. These are repeated every 100 ms.

Value and status readings are transmitted at regular, user-selected intervals in either analog or digital form. Other attributes, such as English description, point name, or limits, are not transmitted on a periodic basis, but only on specific requests from the local functional processor, or any other drop, during the democratic mode.

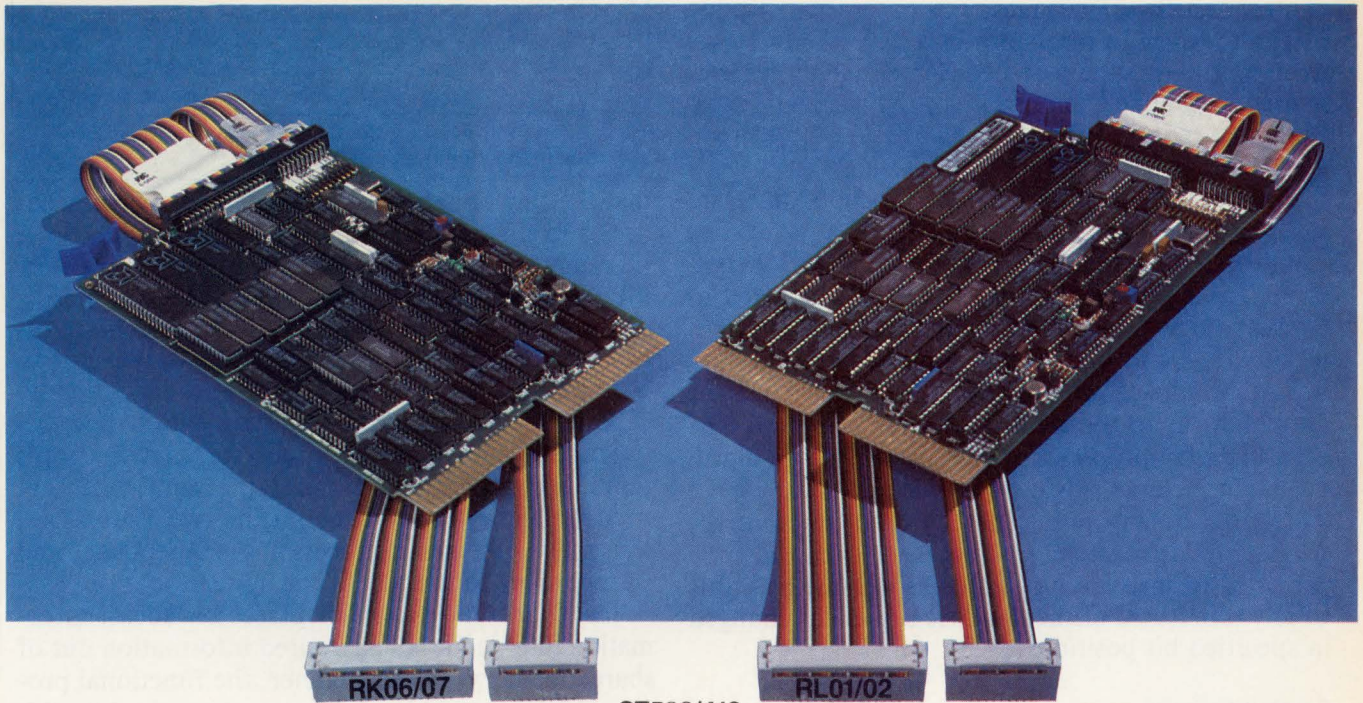
Digital elements include 2 bytes for the system identification number (ID) and 2 bytes for the status and single-bit value. Analog elements are similar except that the value is stored separately in the 4-byte field in floating point format. Fig 1(b) shows a typical arrangement of three analog elements and one digital element in the message data field. Depending on its interest in the system IDs [Fig 1(c) and 1(d)], an individual drop may choose to receive any, or all, or none, of these elements.

A data highway TDM message may contain up to 31 digital or 15 analog elements, or any intermediate combination. The Westinghouse distributed processing family (WDPF) system supports more than 16,000 different system IDs at transmission rates of over 10,000 elements per second. At this level of loading, over 50% spare capacity is reserved for the democratic mode.

Every 100 ms, the data highway enters the TDM mode. In order to synchronize all drops to the identical 100-ms period, three drops are designated as timekeepers. When a drop broadcasts the transfer to the TDM mode, all drops take a "snapshot" of their internal clock timers. The three timekeepers, which are the first three drops in the TDM bus allocation list, transmit the contents of their timer snapshot. Once drops have received the snapshot information, all drops vote and adjust their timers if necessary. This allows the system-wide realtime clock to be maintained in all drops with a resolution of 1 ms and an accuracy of  $\pm 125 \mu\text{s}$ . The timekeepers also restart the data highway if any drop fails to properly pass the token to the next transmitting drop.

During the democratic portion of the 100-ms cycle, many drops can transmit any nonperiodic messages that have been requested. The number of drops that

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may transmit during a given cycle is limited only by the time remaining until the next TDM period.

Messages sent during the democratic mode are either one-shot broadcasts, messages to originator, or general messages. One-shot broadcasts send all element attributes to everyone receiving the element. The local functional processor, or any other drop, can request these messages.

The message to originator is received only by the drop originating the specified element. This message is used to change one or more of the element's attributes, to request a one-shot broadcast, or to send general messages to the originator.

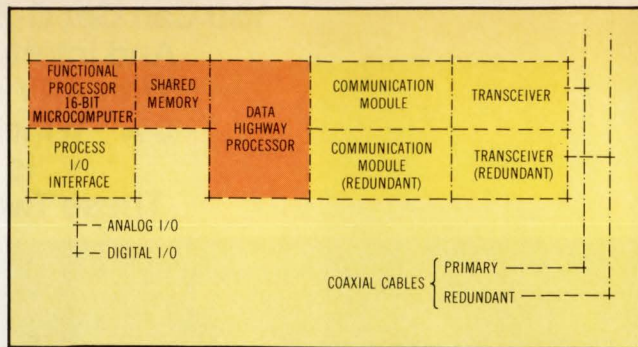
General messages support such functions as downloading of programs, operator messages, or cathode ray tube (CRT) diagrams, and are handled by communication first in, first out (FIFOs) organized as circular buffers in shared memory. There are eight input FIFOs and one output FIFO. Each FIFO supports variable-length entries as received from the data highway or the local functional processor. The data highway processor may also provide an alarm FIFO that includes single-word entries containing the system ID of any point (not currently monitored) found in alarm. A status-change FIFO can also be provided to save the system IDs as well as the status of any monitored element whose status has changed in specified bit positions.

### Fault tolerance

To minimize the possibility of any single failure causing a system-wide problem, fault detection is incorporated in each drop. If a failure is detected, the drop may isolate itself from the data highway and provide fault status to the functional processor. Significant logic is used to detect transmitter failures, since a failed transmitter could cause a system-wide bus failure. The fault detection logic ensures that the transmitter is driving only the coaxial highway when the data highway processor enables the transmission. It also monitors the transmission time to detect and inhibit messages that exceed the maximum length. Other diagnostics check that a drop receives transmissions every 100 ms, that the transceiver does not detect more than three consecutive CRC errors from its own transmissions, and that the functional processor is still active.

The drop microcomputer (functional processor) incorporates a 16-bit 8086 microprocessor and an 8087 numeric processor. Depending on the type and function of a particular data highway drop, these may be used to implement control strategies, perform data acquisition, or display CRT graphic diagrams.

As a high speed bit-slice processor, the data highway processor is responsible for message handling, data highway protocol and arbitration, time synchronization, fault and error detection, and self-test. The data highway processor broadcasts information



**Fig 3 A typical drop on the data highway contains two processors: functional and data highway.**

that the functional processor generates, when it has access to the data highway. This database manager examines all received information and selects only the elements that its functional processor needs. Thus, it extracts the information pertinent to its drop, while adding other information to the system-wide data base.

Shared memory is the communication link between the data highway processor and a drop's functional processor. It stores the data base that becomes the interface between the two processors, thus maintaining each processor's independence and transparency to the rest of the system.

The functional processor places broadcast information into and takes all desired information out of shared memory. In this manner, the functional processor does not need to initiate communication with the rest of the system and treats all information as local to itself.

### *The data highway uses two different modes of operation: the TDM and the democratic.*

Via the data highway, the communication module transmits and receives data messages under the control of the data highway processor. The processor establishes messages in blocks for transmission. Received messages are deserialized and placed in a buffer for the processor to examine. The communication module performs HDLC message generation and reception. It also provides timers to ensure that the data highway token has been properly passed to the next transmitting drop. Fig 3 outlines the hardware structure of a typical drop containing a functional processor, the interface to process input/output (I/O), and the data highway controller.

### Media applications

The WDPF data highway can use either coaxial or fiber optic cable for data transmission and reception. Standard applications use a coaxial cable driven by a transceiver at each drop. This transceiver is passive and does not amplify or repeat signals that originate from other drops. The coaxial



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cable may be up to 6 km in length with Parameter III 412 series cable. Up to 254 separate drops can be configured with bit error rates better than  $10^{-7}$ .

A relay controlled by the data highway processor isolates each transceiver from the coaxial cable. The relay is energized only if the drop successfully passes its startup self-test diagnostics and is capable of receiving its own transmissions. In this way, transceiver electronic failures can be detected, and the drop can be isolated from the coaxial cable without affecting the remainder of the system.

### *Using either coaxial or fiber optic cable, the data highway can easily be configured with redundant highways.*

A fiber optic cable may be provided for systems that require high levels of noise immunity, or electrical isolation, or are situated in locations susceptible to lightning. While the coaxial cable is a linear network, with the cable routed as needed by the particular application, the fiber optic cable is organized in a star configuration [Fig 4(a)]. Each drop is connected to a central transmissive star coupler that allows light originating at any drop to passively propagate to every other drop in the system. Thus, the fiber optic highway is functionally equivalent to the linear coaxial highway, with no detectable difference in performance.

Fiber optic highways operate much the same as coaxial highways. The transceivers and the star are passive, and do not repeat signals that originate at any one drop. Thus, the light originating at the light emitting diode (LED) of the transmitting drop travels passively to every receiving drop. System reliability is high because there are no active components other

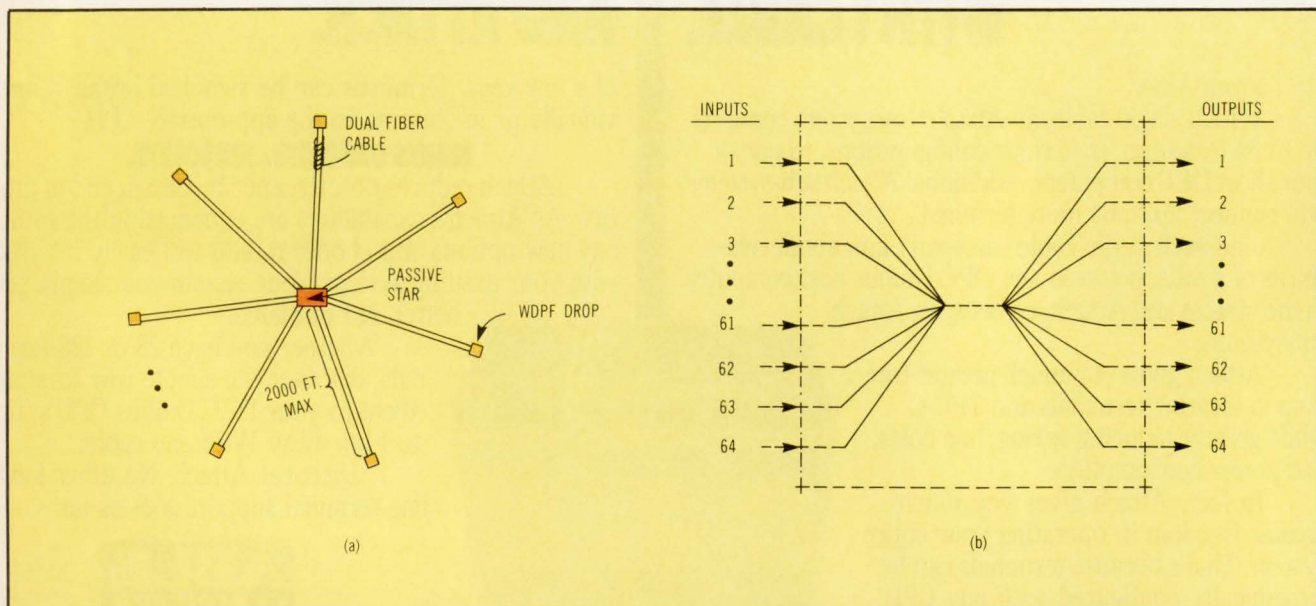
than the drop transceivers. Since each drop monitors its own transmissions, failures in a transmitter can be detected and eliminated without disrupting the data highway. Moreover, should a fiber optic cable be broken, only one drop is affected; the remainder of the network operates without interruption.

The LED in each transmitter launches  $100 \mu\text{W}$  of optical power at 850 nm into a  $100/140 \mu\text{m}$  semi-graded fiber optic cable. This light propagates up to 2000' to a  $64 \times 64$  port transmissive star [Fig 4(b)]. The star coupler divides the light about equally among the 64 output ports and distributes it to every drop in the system via the return path of the duplex fiber optic cables. The P-channel intrinsic N-channel diode and the receiver amplifier in each drop are capable of detecting 30 nW of optical power at a bit error rate better than  $10^{-9}$ .

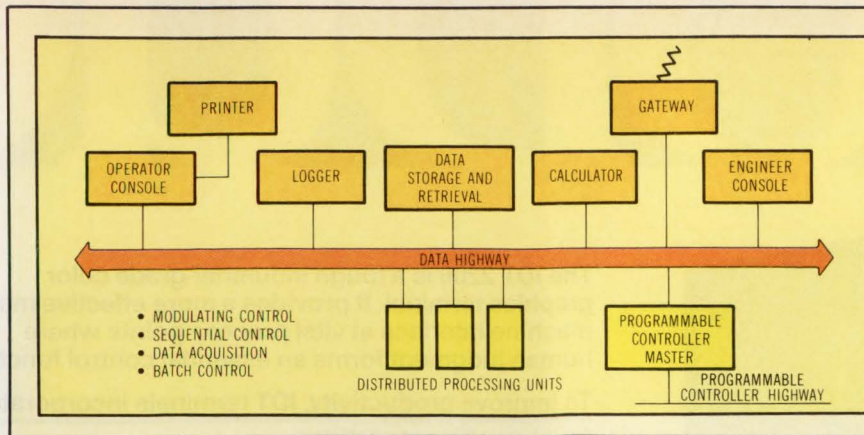
### **Redundant operation**

Using either coaxial or fiber optic cable, the data highway can easily be configured with redundant highways. Redundancy is transparent to the system with no loss of network performance. The redundant coaxial configuration uses a second communication module, a second coaxial transceiver, and a second coaxial cable. In addition, the redundant fiber optic configuration uses a second communication module, a second fiber optic transceiver, a second duplex fiber optic cable, and a second transmissive star.

Redundancy improves data highway reliability as well as the effective bit error rate because both highways operate concurrently. The data highway processor transmits every message on both highways via the dual communication modules. However, it only receives the first "good" message from either communication module and ignores any messages



**Fig 4** Where a fiber optic data highway is used in lieu of coaxial cable, a star configuration is used instead of a linear network.



**Fig 5** The data highway is central to the WDPF system. Transparency between it and the distributed microcomputers (drops) allows each drop to remain independent of external events while the data highway provides system database management.

received with a bad CRC. This method avoids the inherent problem of determining which highway a drop should use and promptly diagnoses failures on either highway should they occur.

The WDPF data highway architecture lets all drops have transparent access to any other drop's process point values without communication overhead. Instant transparent access to the most current global process data base permits control loops in one drop to execute, using process values generated elsewhere in the system. This allows distribution of the functions that would traditionally reside in a central processor. Parallel processing permits each drop to concentrate on its assigned function, regardless of

what else is occurring in the system. Thus, drops performing diverse functions such as CRT graphic updates, control loop processing, data acquisition, alarm reporting, historical data collection, or log printing (Fig 5) all respond as quickly during plant upsets as they do under normal steady-state conditions.

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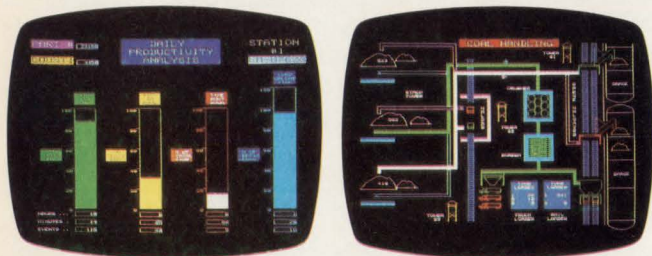
All color graphics shown were photographed directly from the screen and are unretouched.

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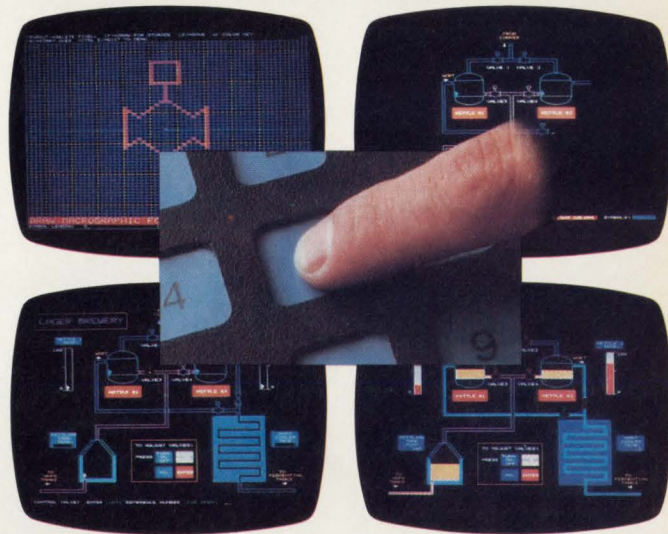
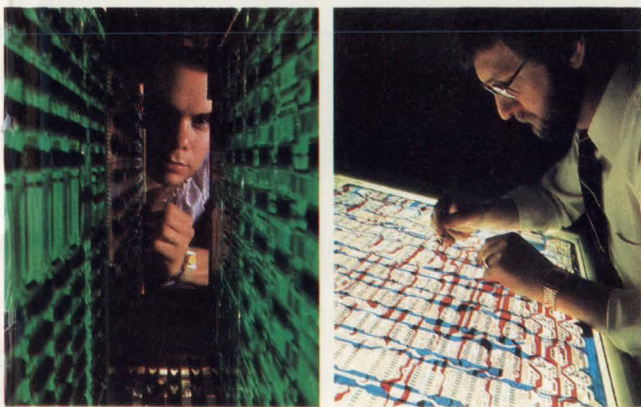




### 3.) *Adaptability to suit your needs.*



Scalable character fonts and numerous application packages are among the features available in the IDT 2200. Application packages include strip chart recording for process monitoring, and dynamic bar graphs for providing real-time production statistics. Other application packages, expansion modules, and options such as touch screen and programmable entry panels are easily retrofitted to any IDT 2200, from the earliest to the latest model.



### 4.) *Simplified programming for rapid graphics development.*

The IDT 2200 terminal utilizes a unique "subpicture" approach for graphics construction, enabling the user to create and store separate graphic images within the terminal itself. Storing these subpictures in the terminal greatly reduces host programming time, host workload, and host-to-terminal communication time.

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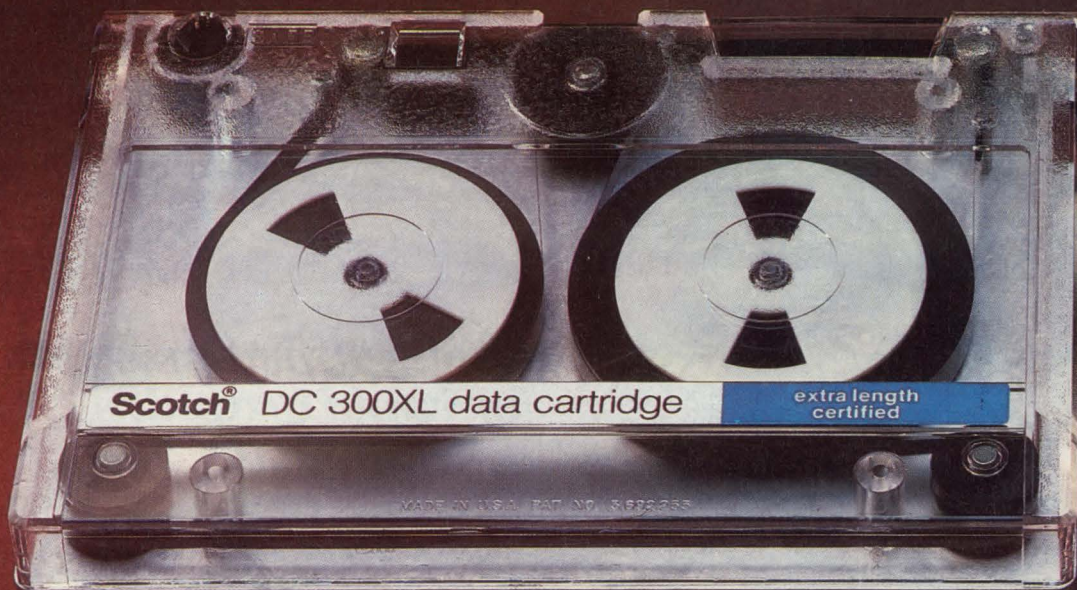
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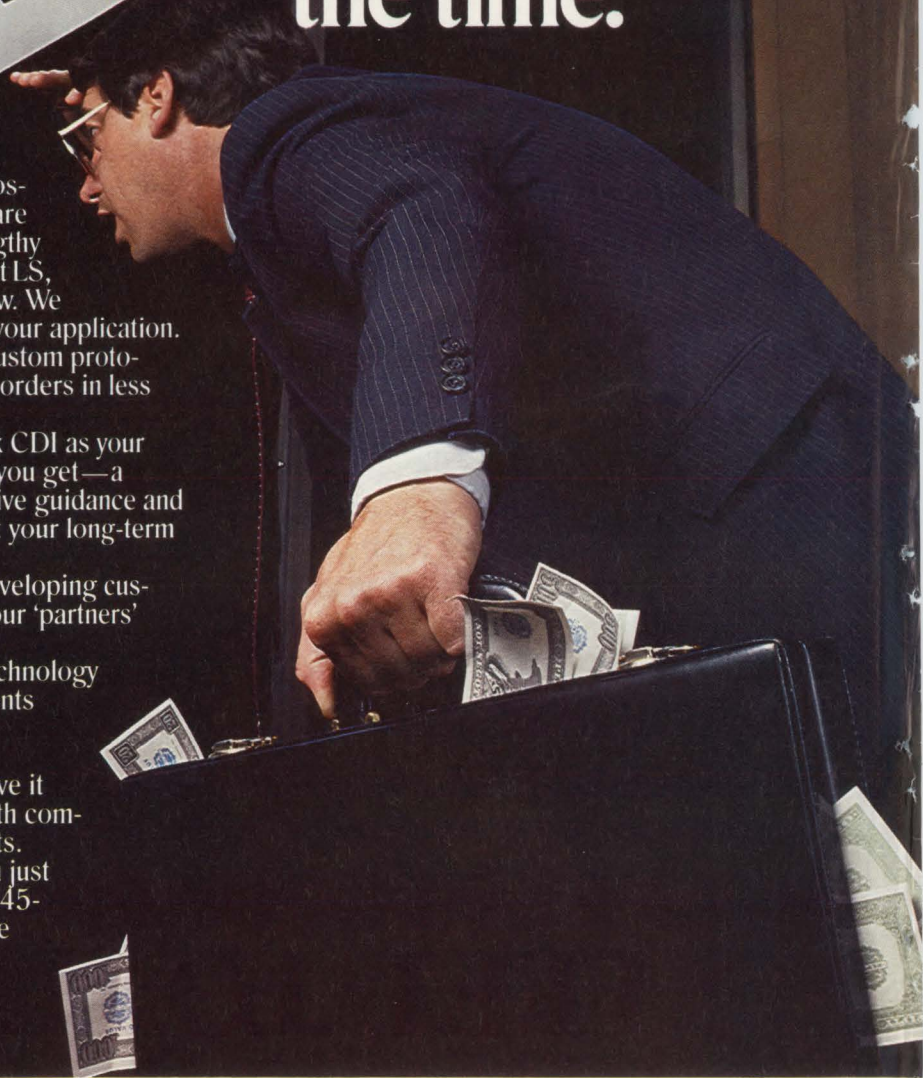
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CIRCLE 73

# DEVELOP VLSI TEST SOFTWARE QUICKLY

**With complete test hardware devoted to each pin of a VLSI device under test, users can write test programs in Pascal for a multi-user environment.**

---

**by Lance Lawson**

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Today's very large scale integration testers use a single-user software development environment in which test engineers must write programs that often exceed 25,000 lines of code. Without adequate software tools, they must do object-level patching and debugging, as well as manually analyzing test results. As a result, programs for very large scale integration devices can take more than a year to develop. Because program development and production tests cannot run concurrently, program development often monopolizes expensive tester hardware. Thus, test program development is included in the critical path for getting a very large scale integration device to market in an industry where a device's expected lifetime is only a few years.

The complexity of testing very large scale integration (VLSI) devices has made test program development the number one testing cost. Traditionally, the automatic test equipment business has taken an "instrumentation" approach to tester design; test systems have been bundles of instruments lashed together for a special purpose. Emphasizing specialized hardware has fostered a belief that specialized software was also necessary. Indeed, it has

---

*Lance Lawson is a software product marketing manager at Megatest Corp, 1090 Ridder Park Dr, San Jose, CA 95131, where he is responsible for MegaOne software. Mr Lawson holds a BS in math and a BA in German from Stanford University, and an MS in computer science from the University of Alabama in Huntsville.*

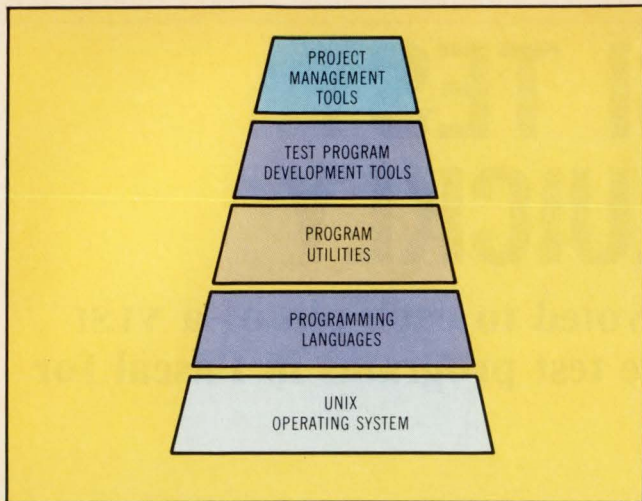
forced the test engineer to write programs in terms of the specific, register-level characteristics of that hardware. Nevertheless, the ideal atmosphere for developing test software should be the same as the ideal software development environment for less specialized systems—that is, it should provide general purpose tools for software development and debugging.

Recognizing these problems, the Megatest MegaOne VLSI tester uses a radically different design approach. It provides independent test hardware for every tester pin, and treats the tester itself as a computer system. Without degrading the system's production test performance, this allows the test system to provide sufficient hardware resources to support the software. This includes a general purpose operating system, high level programming languages, utilities, program development tools, and project management tools.

## **Tester-per-pin versus shared resources**

In the past, hardware design limitations have kept tester software behind the times. For example, testers from prior generations use a shared-resource design scheme. The tester must use a complex switching matrix to connect the limited testing resources (including timing generators, wave formatters, and direct current setups) to a much larger number of pins. Moreover, test engineers must configure the tester for each device test. Then, to test a device properly, they have to manually manage low level tester resources by working with what is nearly assembly language.

In contrast, the tester-per-pin approach puts a full complement of tester hardware resources on



**Fig 1** The MegaOne has five software levels organized as a multi-user computer system. The tester hardware is viewed as yet another system resource.

each pin of a device under test (DUT). This provides the speed and accuracy for testing present and future logic and microprocessor devices. In addition, the complete set of test hardware dedicated to each pin relieves test engineers of the need to manually reallocate test resources. Therefore, almost all test programs can be independent of test hardware. Test engineers can program in terms of the test functions rather than the tester configuration. This leaves test engineers with only two hardware-specific concerns: the tester's basic performance and the physical connection between the DUT and the tester. The system computer takes care of the rest.

The computer approach to test system design looks at tester hardware as just another system

resource. Hardware becomes transparent to users who access hardware resources through tester-independent software. Fig 1 shows the tester's software structure. Its five support levels range from the operating system to the project management tools. Each level reflects the tester-independent approach that the tester's architecture allows.

At the heart of the MegaOne tester software system is Bell Labs' Unix operating system, which runs version 4.2 BSD (Berkeley Software Distribution). Unix was designed primarily as a timesharing system and does not address test engineering's strict realtime requirements. Therefore, Megatest enhanced Unix to meet those needs by adding system calls to the Unix signal handling processor. The way the system handles these signals ensures that each test head gets service from the central processing unit (CPU) in a guaranteed maximum amount of time. Because it has high priority, the test-head interrupt is always serviced before user routines.

### A compiled/interpreted Pascal

To keep hardware user transparent and increase testing productivity, the MegaOne uses American National Standards Institute (ANSI) Pascal with Berkeley extensions as the test programming language. Berkeley extensions are useful for test engineering because they allow separate source files. This leads to structured programming, easier sharing of debugged files and test patterns, and shorter compile times for individual modules (Fig 2). Thus the debugging, finetuning, and maintenance of large test programs become easier and faster to do. For example, once a test program is debugged

```

for actable := BasicFunctionAC to QAACAC do
begin
  ACTableSet( actable );
end;

lotcount := 0;
test := WaferSort;
while RunTest do
begin
  testcount := 0;
  while GetNextDut do
begin
  if test = WaferSort
  then WaferSortTest;
  if test = Production
  then ProductionTest;
  if test = QA
  then QATest;

  end
end;
writeln('@Done@')
end. (* 8243.p *)
Emacs: 8243.p (Normal) --77%-- >
-> Breakpoint at line 31

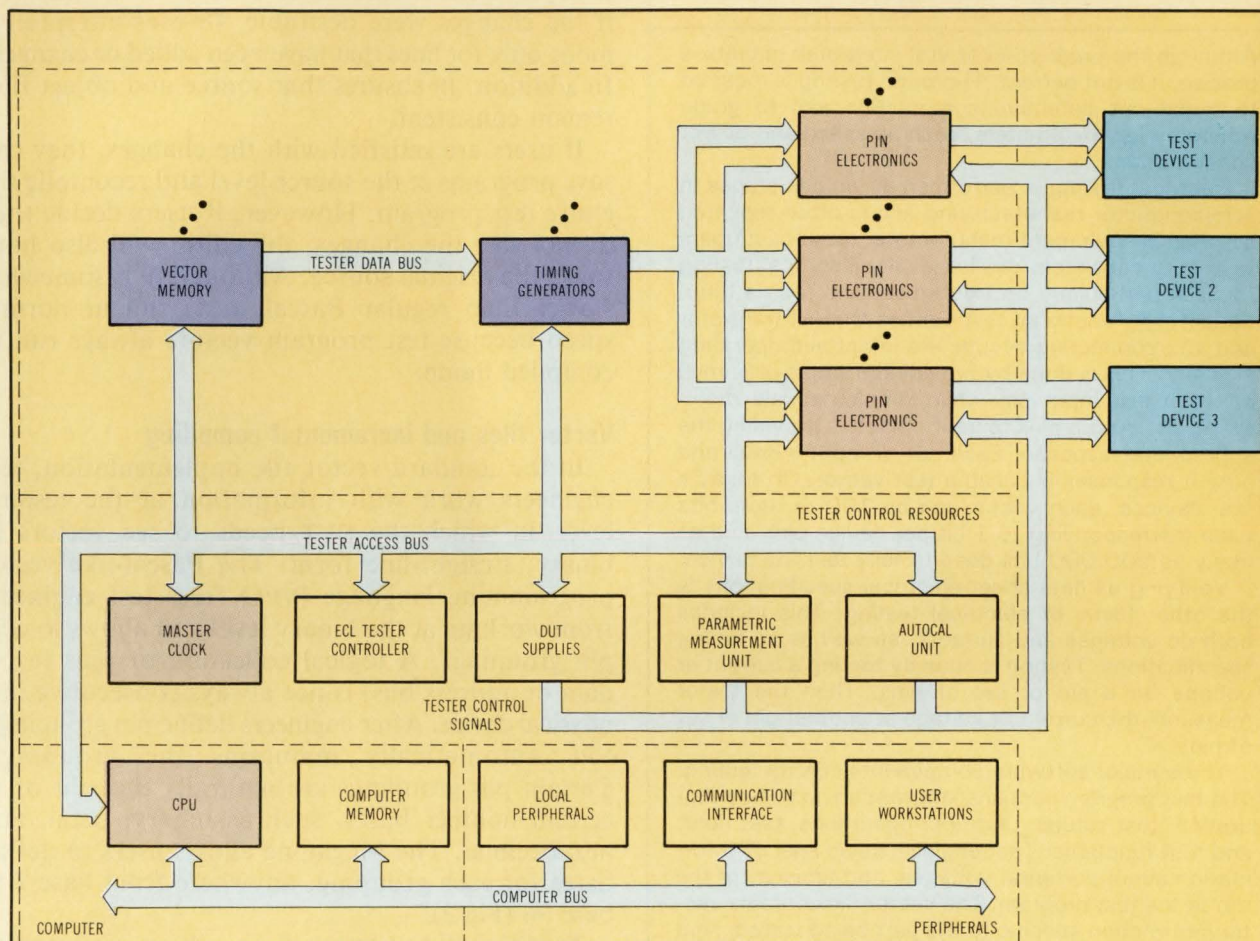
** Emacs: shell (shell) --Bot-- >

```

**Fig 2** In the Pascal test programming language, the programmer puts the cursor at line 31 and enters a breakpoint during a debugging session. At this point, when the program runs, the user can call a file or insert a Pascal line.



## Tester-per-pin hardware



Traditional shared-resource architecture is based on the observation that the same currents, voltages, and timings are present on various pin groupings during testing. To make the shared-resource architecture work, testers bundle a limited number of timing generators together. The pulses are routed to the common pin groupings on the DUT via a complex switching matrix. More and more often, the complexity and size of parts cause test programs to exceed tester resources. To write tests, test engineers have to reallocate resources.

The MegaOne implements tester-per-pin architecture in a VLSI tester (see the Figure). Drivers, comparators, programmable current loads, and parametric test units are resources available on each pin. Parametric measurement units and DUT power supplies are also in the test head. This system's modularity and speed make it feasible to put up to three test heads on the MegaOne, thereby effectively tripling tester productivity.

Timing generators and test vector memory (TVM) are also available on a per-pin basis in the tester mainframe. To ensure enough memory to accommodate the largest test for the next several years, the TVM is 1M vectors deep. All of this is under the command of a high speed controller. The emitter-coupled logic (ECL) controller sequences vectors at 40 MHz, does the current and voltage setups in less than 5 ms, per-

forms parallel parametric tests in 5 ms, and does timing and level searches in 1 ms.

System environmental monitors check all system currents, voltages, air flow, and temperature. They also provide automatic shutdown for each card cage to protect the system from damage if a problem is detected.

MegaOne's 68010-based computer controls tester hardware. The computer has direct memory access to all tester hardware through 48M bytes of address space. It also has up to 16M bytes of error correction code memory, Ethernet connection, disks with capacity up to 1.8G bytes, a high speed tape drive, bit-mapped graphics terminals, and a modem for remote diagnostics. This single processor implementation accommodates up to 16 users. The MegaOne computer can be configured with up to four processors to handle three test heads and 48 users.

Because the test programming language can be high level, the MegaOne can offer a standard programming language: Pascal, Berkeley version 2.0. However, this choice is not hardwired into the tester. MegaOne can accommodate the preferred programming language of engineers.

The operating system is also hardware independent. Moreover, the choice of Unix reflects the concern for putting mainstream, powerful programming tools at the hands of MegaOne users.

## Testing VLSI logic chips

Although the production of VLSI integrated circuits is precise, it is not perfect. Thorough testing is required to weed out defective components and to grade others by key parameters, such as speed and power consumption.

Electrical testing is performed at various stages in semiconductor manufacturing and is often repeated by original equipment manufacturer (OEM) customers to ensure consistent quality levels. Electrical testing focuses particularly on two areas. The first is functionality. A functional test verifies that all transistor and interconnecting circuits are intact and operating properly. This is done by providing a series of stimuli on each DUT input pin while simultaneously monitoring DUT output pins to verify that it is providing the appropriate response. Each set of input stimuli and output responses is called a test vector. On today's VLSI devices, each vector can be 100 or more bits wide (corresponding to 1 bit per device pin), and as many as 500,000 bits deep to fully test the device.

Verifying all data sheet electrical specifications is the other focus of electrical testing. This includes both dc voltages and currents, as well as ac timing specifications. Testing is done by forcing a current or voltage on a pin or set of pins. Then the tester measures the current or voltage at another pin or set of pins.

Three major software components control testing. The test program contains information on DUT configuration, test setups, test floor operations, test flow, and test functions. Test engineers also specify information about currents, voltages, and timings for the DUT in the test program. The vector file contains vector information specific to the part being tested. And finally, the operating system brings the first two components together with the tester hardware. Inevitably, the operating system controls the environment under which the test engineers and tester operate.

and running, test engineers must compare program performance to the DUT. This often requires many small changes throughout the program. Separate source files can make finetuning easier because recompiling is faster.

Reducing debugging time can substantially increase testing productivity. Therefore, Megatest developed an Interactive Pascal (IP) whose syntax is identical to regular Pascal in a single-user environment. While interpreted versions of Pascal and Pascal debuggers are not new, the MegaOne combines compiled and interpreted Pascal in a way that allows test engineers to check changes as they occur. IP promotes source-level interaction and substantially reduces debugging time by eliminating the need to recompile an entire program to test small changes—changes that are required to match the device's real performance.

Users do not have to predict analysis steps and compile them into the test program. Instead, they can interactively insert standard Pascal calls into the compiled program and immediately execute IP, which runs an unchanged part of a test program in

compiled mode. Then users can input program changes and immediately run the new version to see if the changes were desirable. IP uses interpretive mode only for lines that have been added or changed. In addition, IP ensures that source and object files remain consistent.

If users are satisfied with the changes, they can save programs at the source level and recompile the entire test program. However, if users decide they do not like the changes, the editor will also have saved the original source. Although IP is somewhat slower than regular Pascal, tests run at normal speed because test program vectors always run in compiled mode.

### Vector files and incremental compiling

In the standard vector file implementation, test engineers work with information at the tester's level, in which the DUT needs to see vectors in binary, straight-line form. The Pascal-like vector programming language (VPL) frees test engineers from working at the binary level and allows logical pin groupings. A logical collection of pins (eg, a data or address bus) is not always consecutive in a physical device. After engineers define pin groupings, VPL automatically maintains the groupings. Certain pin groupings are naturally thought of in certain number bases, such as binary, octal, and hexadecimal. The MegaOne allows users to define bases for each grouping, anywhere from base 2 to base 36 (Fig 3).

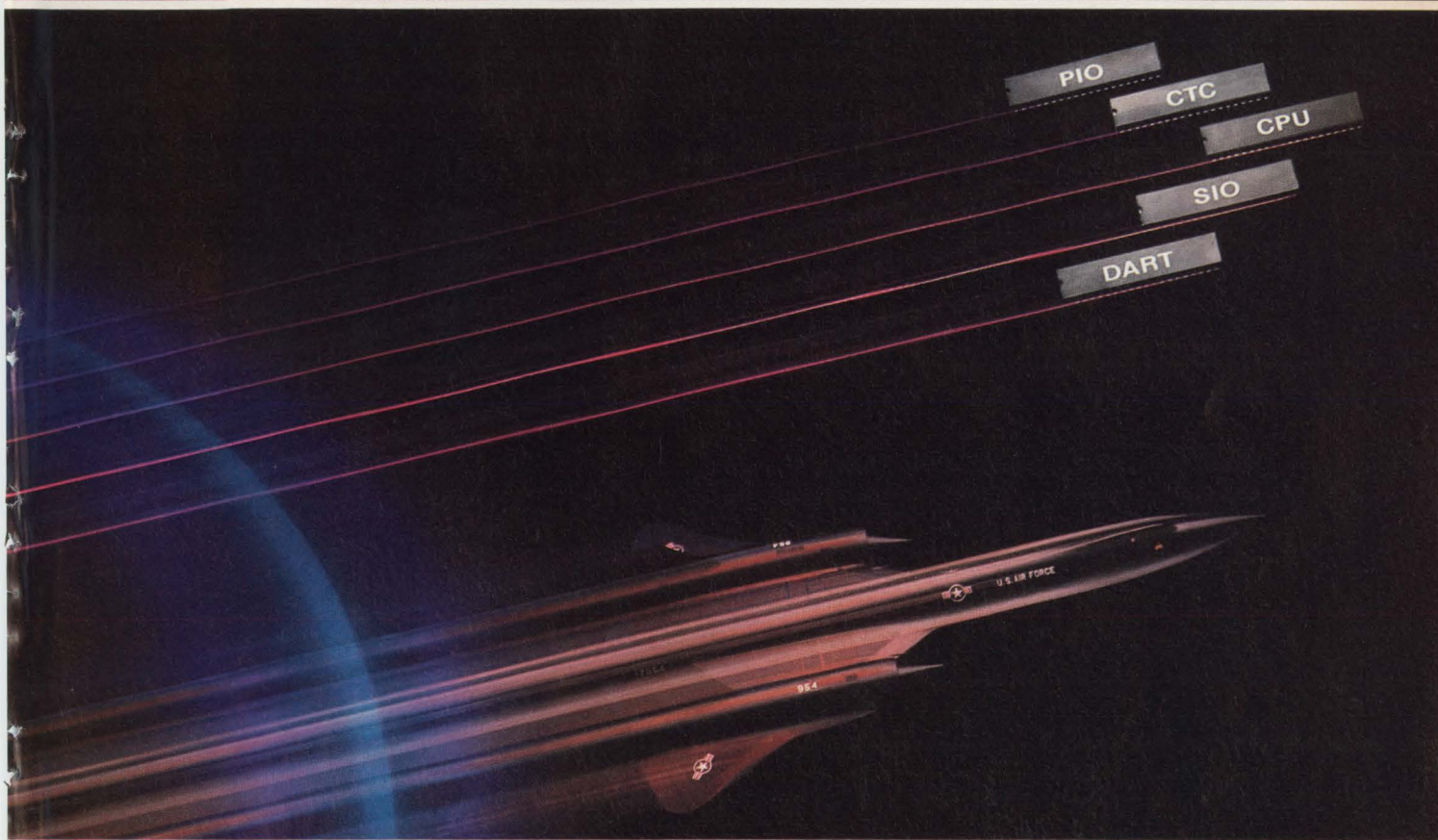
Traditionally, test engineers have maintained vector files by "twiddling bits" at the object level. That is, to avoid tedious recompilation in updating vector files, they change a bit here and there. This approach is undesirable for several reasons: such interaction is time consuming, mistakes are easy to make, and changes usually go unrecorded. A frequent result is that the source and object codes no longer match.

The solution is to make source-level interaction more attractive than object-level interaction by means of an incremental compiler for VPL files. The tester's user interface provides programming tools that decide which lines of a vector file need to be changed. Then, the VPL compiler (VPLC) compiles only changed lines and inserts them into the object file. This automates what test engineers have already been doing by hand. The VPLC saves compiler time, ensures accuracy, and guarantees that object and source files are the same.

### Test program utilities and tools

A large part of test-device characterization tasks are common to many programs that test engineers write. To enhance productivity for repetitive tasks, the MegaOne's utilities library provides a standard Pascal interface. Utilities include schmoos, binary searches, and data logging.

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```

ENABLE DB,MB; REM* EOB8 ;
SET F 0110000010 1110000010 0100000111 1000001011; REM 0007;
LSET MA 0111111111 1111110000 0001100011 1101111110;
ENABLE DB,MA;
SET F 0110000011 1110000010 0100011111 1000001011; REM 0008;
ENABLE DB,MB;
SET F 0110000011 1110000010 0100011111 1100001011; REM 0009;
ENABLE DA,MB; REM FFFF2 (T1);
SET F 0111111111 1100100010 0100000111 1100111111; REM 000A;
ENABLE DB,MB; REM E6FF ;
SET F 0110011011 1111110010 0100100111 1000001011; REM 000B;
** Emacs: 8086 (Normal) --19%-- >
(* EOB8 *)
gct(3,1,0) [5, 3, 4, 2, 1, 0, 0]; (* 0007 *)
gct(4,1,0) [7, 3, 4, 2, 1, 0, 0]; (* 0008 *)
gct(3,1,0) [7, 3, 4, 2, 1, 0, 0]; (* 0009 *)
(* FFFF2 (T1) *)
gct(3,0,0) [F, F, 4, 2, 4, 1, 1]; (* 000A *)
(* E6FF *)
gct(3,1,0) [7, 3, 4, 2, f, 1, 1]; (* 000B *)
gct(4,1,0) [7, 3, 4, 2, f, 1, 1]; (* 000C *)
gct(3,1,0) [7, 3, 4, 2, f, 1, 1]; (* 000D *)
(* FFFF4 (T1) *)
** Emacs: 8086.vpl (Normal) --20%-- >
mktg 5 % factor 8086 8086.vplX

** Emacs: shell (shell) --99%-- >

```

Fig 3 Three blue screens show the binary vector input files, the VPL output vector file, and the command the user typed to do the translation. The first line highlighted in green shows a test vector in its binary form. The second line in green shows the same vector grouped and defined as hexadecimal numbers.

Test engineers use schmooos to characterize devices and determine trouble spots. Basically, a schmoo is an X-Y plot of parameters, such as timing versus voltage. From the hardware standpoint, it involves repetitions of the same test program, continually modifying hardware settings. Clearly, software utilities simplify the test engineer's task. From a software standpoint, the schmoo utility provides unlimited tracking parameters; results that can be sent to a file, as well as to the printer or a video display; and inputs that can be saved and recalled interactively (the interactive syntax is identical to that used in Pascal programs).

With the binary search utility, users can search for any time (including cycle period or any input or output edge), voltage, or current. Similar to the schmoo, users can do binary searches interactively from a Pascal program. They can then store the search parameter and recall it later. The data-logging utility allows test engineers to store test data in a data base. By using online or offline tools to analyze these data, they can then determine information (including a part's pass/fail rates).

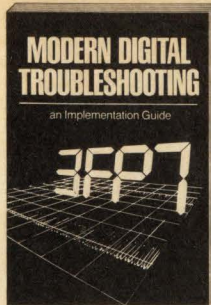
In a good computer system, a tester should also provide users with some programming help and a user interface. To tie the basic language capabilities together, the MegaOne uses an editor called Emacs. This version of Emacs is more than a display editor; it also gives test engineers tools to generate, compile, link, and run programs. Emacs also offers extensive online help and documentation. Although Emacs serves as the primary user interface, the

tester offers a menu-based interface for users who do not need all of Emacs's facilities.

A computer aided test program generation (CATPG) facility helps users develop test programs quickly. Because basic test program structure is similar for all test programs, CATPG can be an invaluable aid for initial program generation. The CATPG menu interface takes the user through a logical description of the DUT. Then, CATPG generates the program's structure and format. This eliminates much of the repetitive work involved with writing a test program. By guaranteeing a syntactically correct Pascal program from the start, it also reduces the possibility of error. When users have answered the CATPG questions, the tester can generate up to 90% of the test program's final code.

To help users track program revisions, the tester uses the Unix revision control system (RCS). RCS allows users to store and retrieve multiple revisions of a program without using extensive disk space. RCS also provides release and configuration control to help users identify a program module's purpose and release state.

Because it acts as a computer system, the tester can also provide project management support for the large amount of data the test process generates. Data are frequently collected on all devices tested—up to 500,000 devices per month on the MegaOne. Tools included on the MegaOne are a spreadsheet calculator, the Unify database management system, the Ethernet network, and electronic mail. The project manager can use these tools to get



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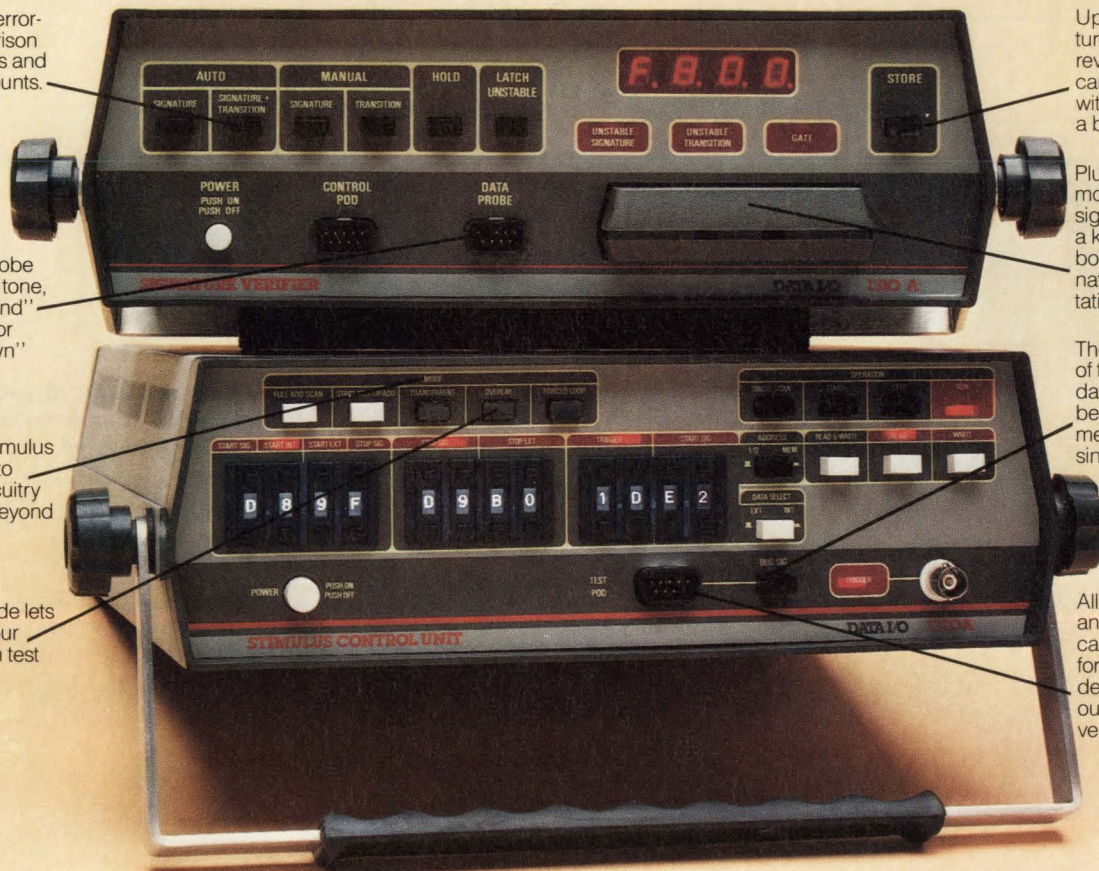
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Circle 74 for literature

Circle 76 for sales contact

# DATA I/O

```

TestSet( ShortsVectors, acvectors);
opensvectors := 'Opens.vpl';
TestSet( OpensVectors, opensvectors);
basicfunctionvectors := 'Basic.vpl';
TestSet( BasicFunctionVectors, basicfunctionvectors);
leakagevectors := 'Leakage.vpl';
X TestSet( LeakageVectors, leakagevectors);
vilvihvectors := 'Basic.vpl';
TestSet( VilVihVectors, vilvihvectors);
volvohvectors := 'Basic.vpl';
TestSet( VolVohVectors, volvohvectors);
iccvectors := 'Basic.vpl';
TestSet( IccVectors, iccvectors);
stressvectors := 'Basic.vpl';
TestSet( StressVectors, stressvectors);
acvectors := 'Basic.vpl';
TestSet( ACVectors, acvectors);
ACTableClose;

end;

** Emacs: assoc.p (Normal) --62%-- >

TEST (M) UNIX Programmer's Manual TEST (M)

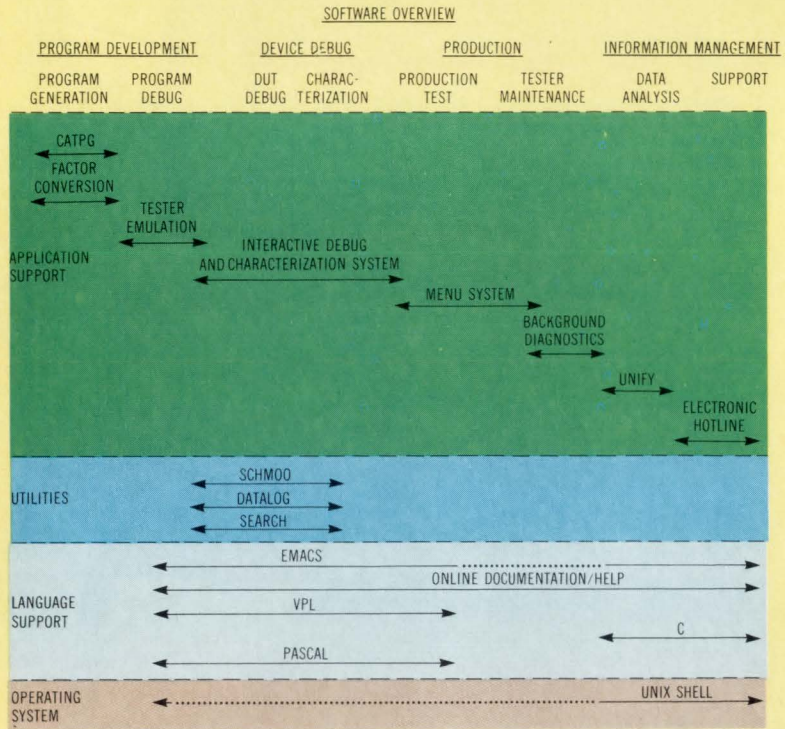
NAME
Test - Functions that perform and control execution of vpl,
input leakage, and user defined tests.

SYNOPSIS
procedure TestSet ( test:TestName ; var vplfile:String );
procedure TestGet ( test:TestName ; var vplfile:String );
function Test ( test:TestName ):Result;

Emacs: Manual entry (Normal) --Top-- >

```

**Fig 4** Users can simultaneously display multiple windows of information. In the upper window, the compiler has flagged an error. In the bottom window, the user is consulting the online manual to identify the syntax problem.



**Fig 5** Pictured is the MegaOne software cycle, from development through debugging and maintenance.

information about yield, worker productivity, and machine uptime—all on line. These additional tools will not degrade actual test productivity.

### A session on the tester

In a typical work session, users work with multiple windows on the screen. In Fig 4, the test engineer is writing a test program for an input/output expander. Here, the windows are the test program source file and a software manual page. During program development, the test engineer can consult the online documentation to answer any questions or use the shell window to issue commands to the Unix operating system.

Next, the test engineer compiles the completed test program, which is an automatic procedure. A combination of Unix and Emacs features allows the test engineer to start the compile with a single keystroke. Because finding compile errors in a program with multiple source files can be difficult, the editor uses a window to display each source file where an error was found. Then, it steps the programmer through the error listing and puts the cursor at the line where the compile error was found. This allows programmers to correct most compile errors on line without consulting a hardcopy version of the test program.

The next steps in program development involve debugging the program for runtime errors and finetuning the program for the DUT. Again, the tester provides software tools, leaving the production tests unaffected by program development. Software tools include IP and tester simulator software.

Finally, the test engineer recompiles the changed and finetuned program. Then, the user stores the source and object files in the archival system to make them available to others. The final step may involve sending mail to announce the program completion. Fig 5 gives an overview of the software development and debug cycle.

The MegaOne tester's design approach provides specialized hardware to meet the needs of VLSI testing and a general purpose software development environment. The result is a test system that doubles tester productivity. Future improvements to this system will provide better source-level interaction with the VPL, terminals with improved hardware support for windowing, and an interface to computer automated engineering chip design systems.

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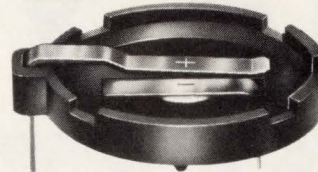
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Average 711

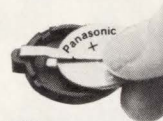
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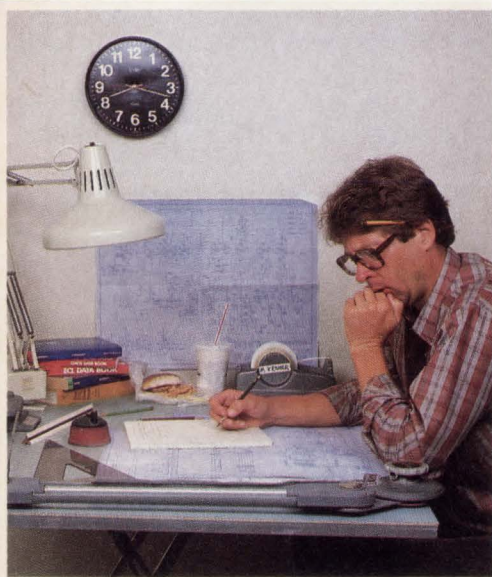
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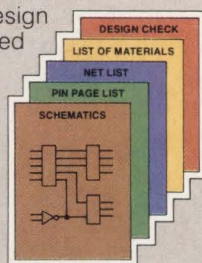
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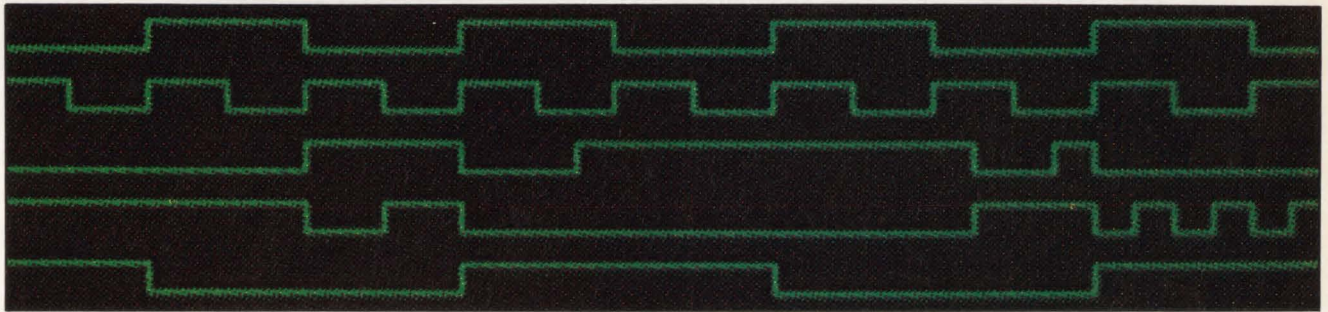
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# CAE UNIFIES LOGIC AND GATE ARRAY DESIGN

Standalone computer aided engineering systems prevent logic errors and force correct layout. Results are lower equipment cost, reduced feedback time, and computing power for designers.



---

by John Wright

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Until recently, system designers seemed to be creating equipment that improved productivity for everyone except themselves. Instead of automating their own work process, they have been stuck with pencil-and-eraser methods in the most crucial step—the frontend design.

To increase designer productivity, a new generation of computer aided design (CAD) equipment was created. While previous equipment was capable only of computer aided artwork, the computer aided engineering (CAE) system tackles the entire task of logical design, engineering, and physical layout.

A CAE system provides a single data base that carries a design from its earliest functional description to a finished and verified product. It gives design teams an electronic mail system, access to the latest revised design, file sharing, and networking to create the best mix of local and remote computation.

---

*John Wright is technical support group manager at Daisy Systems Corp, 139 Kifer Ct, Sunnyvale, CA 94086. Mr Wright holds a BSEE from San Jose State University.*

For example, the Logician, a CAE system from Daisy Systems Corp, was used to design Seeq Technology Corp's Ethernet chip. It is currently being used for complex design tasks, including several 32-bit microcomputer projects.

Built around Intel's 8086 family of processors and coprocessors, and driven by over 1.5 million lines of field-tested code, this CAE system is a standalone portable engineering workstation. It uses a Multibus architecture, a Unix-like file system, Ethernet, and phone line (RS-232-C) serial communications, and up to 1.5M bytes of random access memory (RAM). Mass storage from 10M to 80M bytes is supplied with each workstation, with more storage available through Ethernet. Daisy's next generation of workstations will center around the iAPX 286.

File sharing between workstations is also allowed by the system's database management software. Using Ethernet, the workstations can interface with any equipment that uses the Xerox XNS protocols. The designer interacts with the system through a keyboard, a data tablet, and a 17" or 19" color or monochrome display with 800- x 1024-pixel resolution.

Another CAE system, the Gatemaster, has all of the capabilities of the Logician, as well as additional hardware and software that handle the physical

implementation of the gate array. While presenting new design methodologies, both the Logician and Gatemaster preserve the designer's existing tools. This includes the ability to generate drawings at any point and to interface to any proprietary software that the designer has developed.

### Incremental compilation is key

Probably the most important features of CAE systems are their ability to make incremental compilations of the design file, to automatically generate the input files for utility programs, and to process them locally. Previously, designers had to complete the schematic and net list for their designs, as well as code the designs for a simulation program before seeing any feedback on their logic. Moreover, the design was often taken through the layout and fabrication stages before errors were found.

As a result, days and sometimes weeks went by before the designer could receive feedback. When it came back, there were many errors to be corrected and it was often hard to tell which step had caused an error (see Fig 1). Designers would have to make the corrections they hoped would make the design perfect, then totally recompile the design and wait again for the lengthy feedback process. Typically, designers may have to go through this process five or six times to achieve a verified design.

Incremental compilation makes propagating changes through the design process easier and faster. Only changes need to be recompiled, rather than the entire design. As changes in the higher levels of the hierarchy affect the more detailed lower levels, those portions of the design must also be recompiled.

When incremental compilation is combined with the Logician's ability to link different hierarchical design levels, the designer can save a lot of time. This linkage allows the CAE system design methodology to conform to the human mind's nonlinear flow. The designer can "flesh out" a particular portion of the

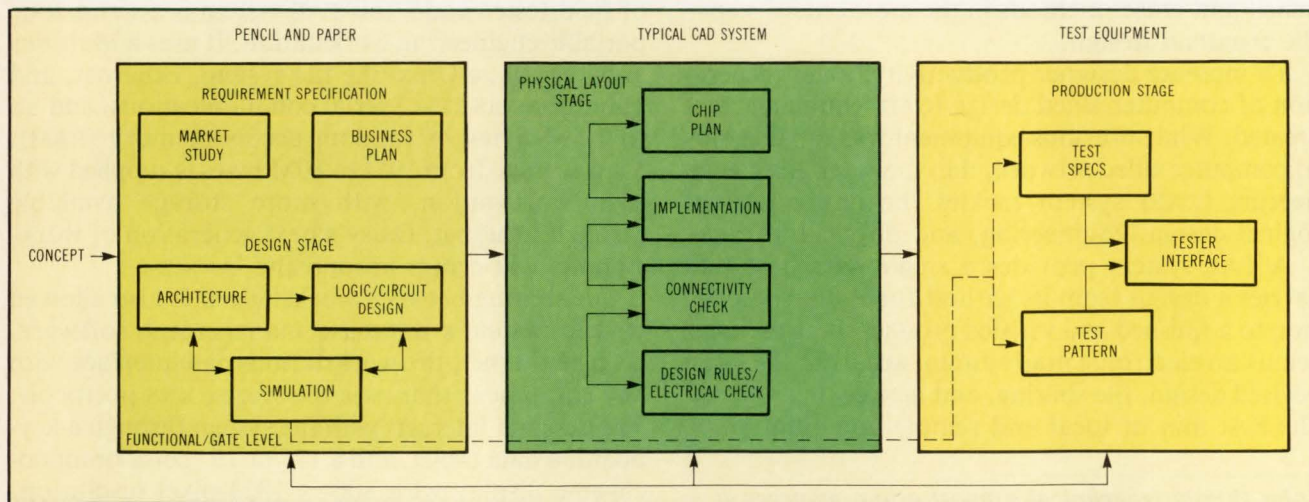
design with detail. Then the Logician links that portion with others that are still in the functional block stage, presenting the design as a single entity to the simulation programs. Later, the designer can "flesh out" another section, have that increment compiled, have the coding for the simulation programs generated automatically, and get quick feedback on that part of the design effort.

These mixed-mode simulations are particularly useful when a designer needs to look ahead to see whether an entire architectural approach is feasible. A typical question to be answered would be, "If this architecture cannot support a 100-ns machine cycle, then we must discard the whole approach. How can we know before we sink all this design time into it?" Instead of detailing the whole design only to find that the approach is wrong, the Logician allows the designer to simulate a few critical portions of the design, both in logic and timing, while the rest of the design is still in the functional block.

### The Logician as personal computer

As Fig 2 shows, this incremental compilation and editing method breaks the logic design process into several steps, each of which can give quick turnaround in pointing out errors. When compared to Fig 1, which shows the pencil-and-eraser method loading into a timeshared mainframe environment, it becomes clear that error feedback time can be reduced from days to minutes.

The CAE system becomes the designer's own professional computer, and makes the design process faster and more interactive. Any designer who has waited for batched output from a timeshared central processing facility knows that it is much better to have one-tenth the computation power readily available at all times than it is to be one of 10 users timesharing a mainframe. With a 10-MHz 8086 processor executing 0.8 million instructions per second, the system's computational power is considerable. On



**Fig 1** Without an integrated design system, circuit and chip design are broken into several sections: hand design, artwork preparation, and testing. Feedback to the designer can be very slow, sometimes coming only after fabrication.

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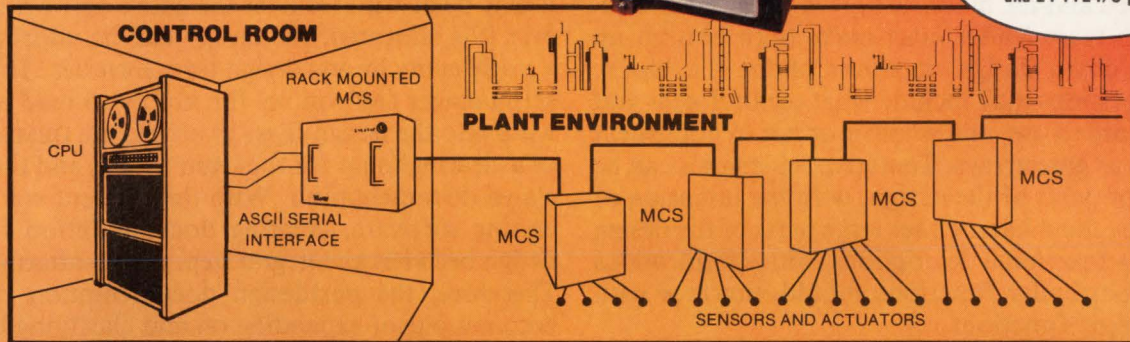
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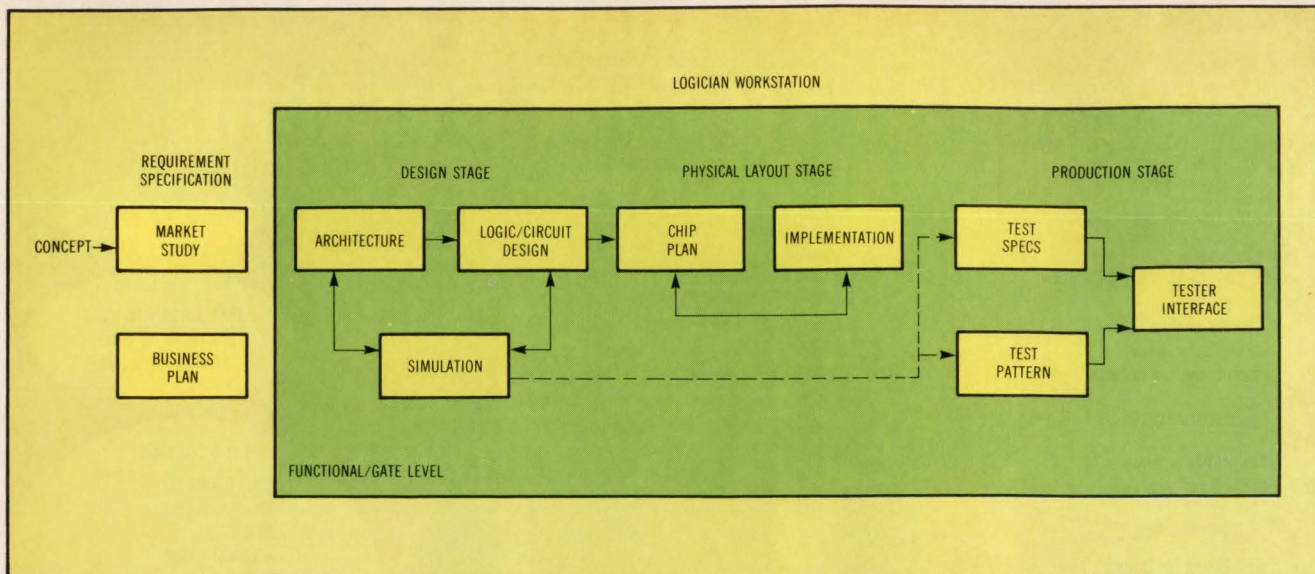
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**Fig 2** By compiling the design as a single entity at an early stage and offering local processing, the CAE workstation can break the error feedback process down into a series of short automated loops, thereby encouraging a fault-free logic design process and a correct by construction layout methodology.

certain specialized functions, such as logic simulation, its power is comparable to a mainframe.

### Past and present design methods

Circuit design begins with the project manager's decision on the initial architecture. The design is then partitioned and the blocks are given to the team leaders. Each team leader must make both bottom-up and top-down design decisions about the block. These decisions may include what technologies and architecture to use, and whether or not to implement portions as gate arrays. Tentative schematics can be drawn for parts of the design, with the intention of discarding them later. Other large parts of the design are left as functional descriptions, with specifications of how particular functions should interface with other major functions.

The difference between the old methodology and the new is immediately clear. With the old way, each designer is still working with paper at this stage. With the CAE system, each designer enters notes and block diagrams directly into the design data base.

Even communicating ideas within the design team does not require a meeting. It can be done using the system's electronic mail system. Information such as a functional block diagram can be entered through the Logician's graphics editor, which has linkage to schematic representations that are the expansion of any functional block. Using the electronic mail system's word processing function, comments and explanations can then be entered.

At this early stage, the CAE system shows definite advantages. With the paper-and-eraser method, notations propagate around the design team, but it is very hard to keep track of the latest version. This is simple with a CAE system, because all of the designers feed into and retrieve information from a common design data base. The database manage-

ment system (DBMS) keeps careful track of which new ideas go with which revision level, and it ensures that the designer is always working with the latest revision.

The actual disk memory that holds the design data base may be physically resident in one system, or it may be distributed over the entire network. However it is allocated, the design can be addressed as a single entity by any design team member. The project manager can control the ability to read and/or write into the design files. In effect, the DBMS works as a clearinghouse for the team's ideas and the associated documentation. With the resident word processing software, creating documentation for the design becomes an integral step, not an afterthought. Therefore, the postdesign documentation process becomes one of expanding on and clarifying the designer's notes.

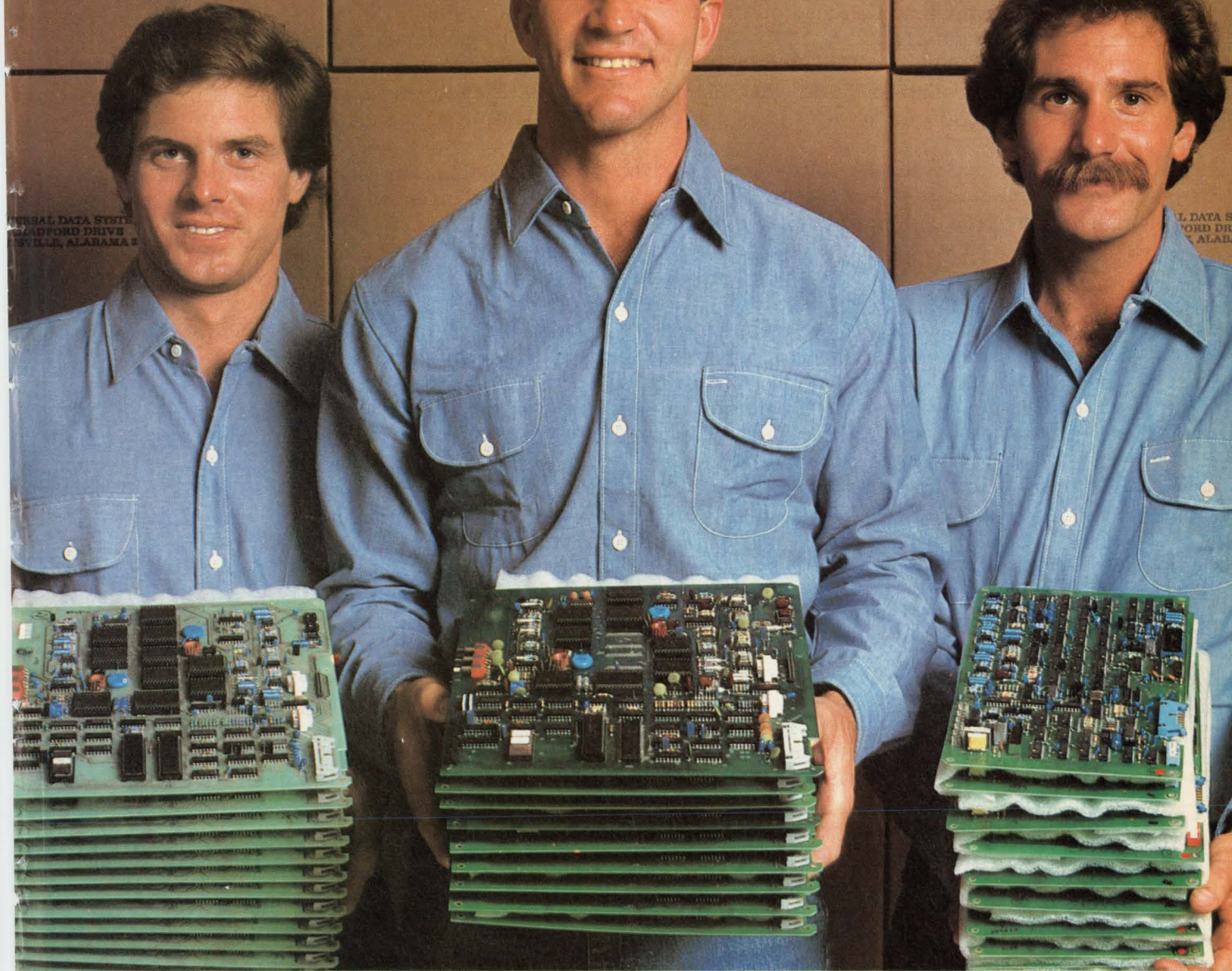
### Schematic entry becomes easy

After giving the functional block some thought, the designer begins to define the logic. In the past, this has meant drawing and erasing the schematics on a number of drafting sheets. It has also involved shuffling drawings and paperwork on the designer's desk. With the CAE system, the shuffling is done electronically. The system only takes a few seconds to redraw each page from memory, as needed.

Entering schematics can be done in three ways: the various components can be entered from a menu on the data tablet, they can be copied from an existing drawing, or they can be entered using the 28 user-programmable soft keys on the Logician keyboard. With some or all of the components in place on the schematic, the designer then graphically enters the connection between components by placing the cursor on the tablet over the point to be connected. Any change in the direction of the wire's path is similarly

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indicated. All components and signals are automatically named by the system.

According to comparisons run by Mitel Corp, the result of this computer aided method of schematic entry is that schematics are created five times faster than they were manually. This alone represents a significant time savings for the designer, along with automatic extraction of net lists from the design data base.

At this point in the process, the designer using the pencil-and-eraser method must manually extract the connectivity of the design. Code that expresses the design in the format required by a logic simulation program must then be written. This process is tedious, repetitive, and extremely exacting—the very thing that should be done by a computer.

In creating a net list, the designer can overlook a connection and ruin the simulation. Syntax errors in coding the input file for the simulation run are also very common, and require further revision cycles. A CAE system creates the net list automatically, along with the simulation input file and a number of other functions.

### **Modeling unlocks engineer's tool box**

Once the schematic is entered into the design data base, a number of utility programs can give the designer quick feedback on some of the more common errors in logic design. At the same time, the design information is automatically prepared as input files to various simulation routines. The designer can invoke these utility programs through 1-button soft-key implementations of the modeling system.

Soft keys can call the Daisy network connectivity extractor, the Daisy resolving linker, or the simulation input generator. These programs operate on the design in a few seconds or a few minutes, and each gives the designer the kind of error feedback needed early in the design process. They act as guides to a fault-free logic design, from schematic entry through completion of the logic design.

The network connectivity extractor acts as a design compiler, as well as a connectivity and syntax checker for each page in the design. The resolving linker links the pages and checks the syntax and connectivity between pages. It also resolves the functionality of larger blocks onto separate pages to allow the mixing of different hierarchical design levels for simulation purposes. This mixed-mode linkage allows the designer to get fast answers from simulation programs, even though the design has not been created in detail.

With the page and interpage errors cleaned up, and with the design pages linked into a single entity, the designer is ready to extract a component and network list and to format the design file for any available simulation program. The simulation input

generator program and its variants can do this automatically. One variant (Sing) prepares the design file information for simulations on external mainframes, a second variant (Sift) prepares inputs for the onboard logic simulator, a third (Som) prepares the design for the onboard timing verification, and a fourth (Update) prepares the logic design for physical layout in a gate array.

In the past, designers have had to learn the intricacies of coding for each different simulation program, including knowledge of the different operating systems and assembly language quirks of individual mainframes. With the simulation input generator, the whole process is reduced to a 1-line direction to perform the Sing function (or its variants) upon the design file, and to target the coding for the chosen simulation program.

### **Local or remote simulation**

When such simulations are run, the system presents the choice of processing them on remote mainframes or using the native computational workstation power. For remote processing, the Logician can act as an intelligent frontend processor. It can emulate an IBM 2780 or 3780 intelligent terminal transmitting IBM remote job entry protocols at 56K baud. A standard serial (RS-232) communication interface is available to any mainframe.

These remote processing capabilities extend to any custom utility program that the designer's company may have developed. Because the majority of design analysis programs are custom programs, it is good to know that such an existing software base need not be abandoned. The Logician already has the models to translate a design file into an input file for popular logic simulation programs such as Tegas and Logcap, and for circuit simulation programs such as Spice and Aspect.

Interfacing the Logician to the user's custom analysis programs is done once for each custom program. With the Daisy modeling language, the interfacing is simple. Once the custom program input requirements are modeled, the Sing function can automatically format subsequent design files to serve that program.

The system also offers local simulation processing, including logic simulation on the interactive logic simulator, timing simulation with the timing verifier, and circuit simulation with Daisy's Spice simulation capability. As with externally processed simulations, the Logician automatically supplies the input formatting and coding necessary to translate the design file into an appropriate input file for the simulation program.

While local simulation saves the cost of time-sharing, its prime benefit is that it dramatically reduces the error feedback turnaround time. The ability to link detailed and block-level portions of



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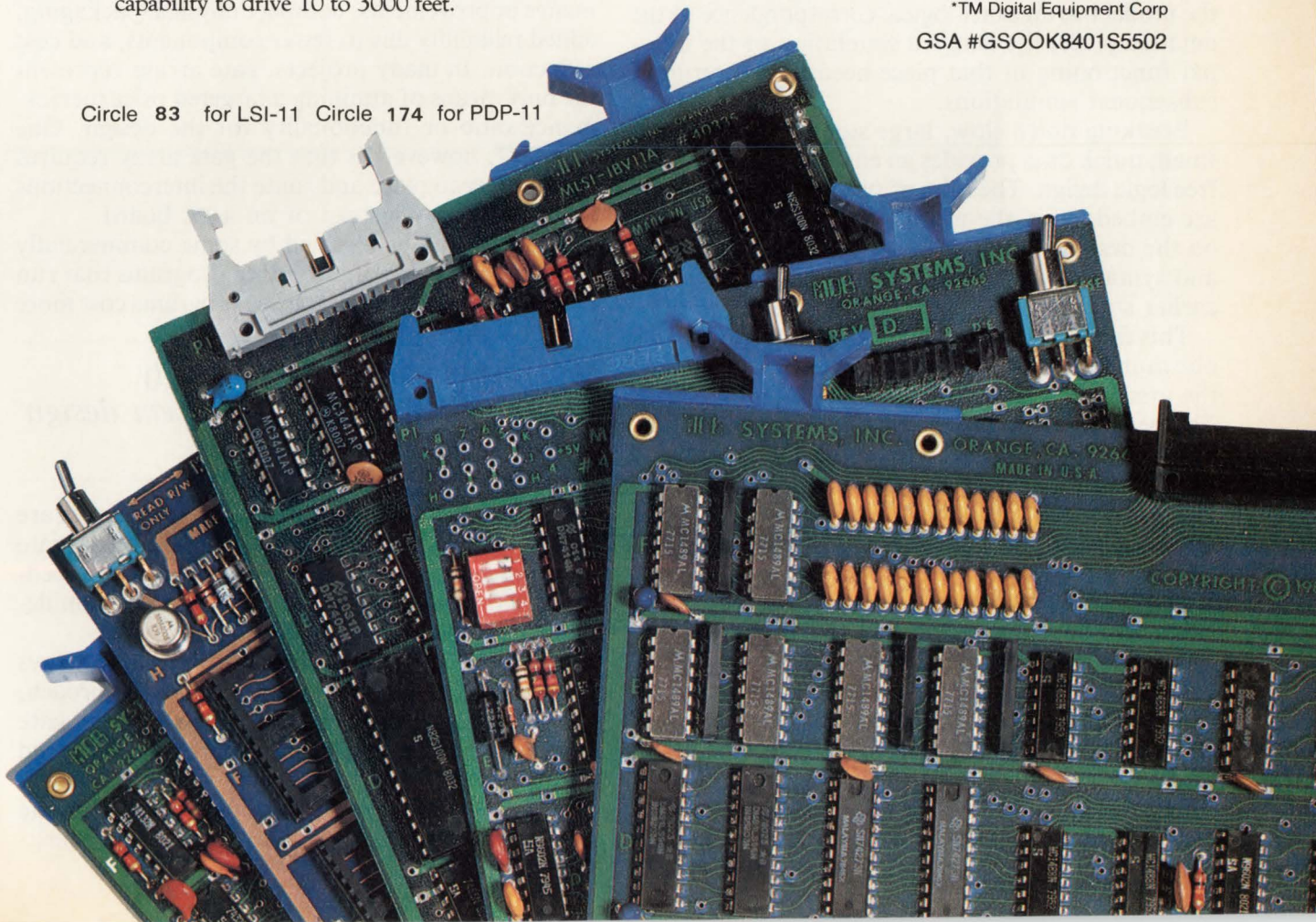
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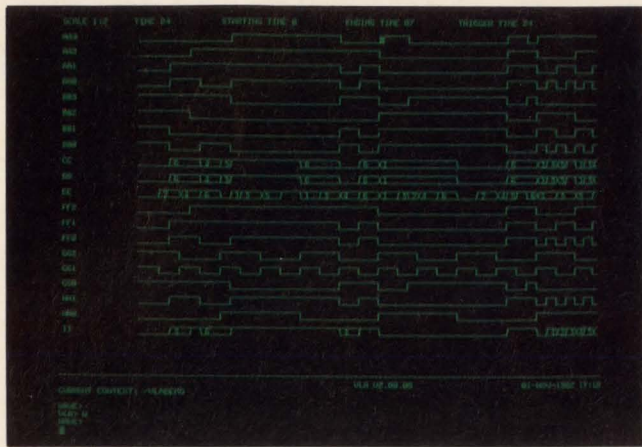
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**Fig 3** Rather than wait for the design to reach the hardware stage, the CAE workstation can perform logic analysis using results from the simulation programs. If an error condition is suspected, a designer can even stop a simulation in mid-run to examine status and register contents. Here, a pseudowaveform representation of the logic state changes at key points is displayed.

the design into a single entity, along with the ability to make incremental compilations, allows the designer to make incremental simulations.

For example, an otherwise large simulation can be broken down into several smaller ones by running simulations on pieces of the design as they are developed. Once a detailed piece has been simulated, it can be represented by its model on subsequent simulations involving larger pieces of circuitry. Since the model has an exact logical correspondence to the detailed piece, the detailed simulation of the internal functioning of that piece need not be rerun in subsequent simulations.

Breaking down slow, large steps into a series of small, quick ones provides an environment for fault-free logic design. The rules of syntax and logic design are embedded in the utility programs that operate on the design. Through a CAE system, logic design and syntax rules can enter the design process at an earlier stage than was previously possible (Fig 3).

This fault-free design methodology quickly points out mundane errors to the designer and pinpoints the more subtle system errors in later simulations. The designer can even instruct the simulation program to stop a simulation upon reaching a possible error condition. If such a condition can be specified, the simulation program can stop at that point and display all system parameters and activity.

### **Making a design change**

Unless the design is perfect the first time, the simulation programs will reveal flaws. The designer must then correct the design, which requires changes in the schematics. With the pencil-and-eraser method, the designer has to have new schematics drawn, determine how the change will affect other parts of the design, recode the input files for each of the simulation programs, recompile the programs,

and wait for the results of the new simulations to come back from the mainframe computer center.

With the CAE system, the designer just has to make the schematic change with the drawing editor (new plots can be generated automatically). Then, pressing the function keys for the network connectivity extractor, resolving linker, and simulation input generator, the designer can recheck the design piece by piece. The connectivity extractor and resolving linker will recheck only those portions of the design that have been affected by the change. Single variants will recompile only portions of the simulation input file that have been affected by the change. As mentioned before, the incremental nature of these changes to the design files saves both computation time and the designer's time.

### **Development ease opens up gate array usage**

Once the designer is satisfied that the design logic and timing are correct, and that a circuit simulation performance proves out, the actual physical implementation of that design can begin. If the system designer is working with standard components, then the placement and routing on a printed circuit (PC) board can be handled by a program such as Sci-cards.

Gate arrays are an increasingly attractive supplement to system design using standard components. Since gate arrays make the extensive use of large scale integration possible, they can offer performance improvements, compact physical packaging, added reliability due to fewer components, and cost reduction. In many projects, gate arrays represent the only means of attaining a targeted price/performance ratio or functionality for the design. One trade-off, however, is that the gate array requires the designer to place and route the interconnections within the array instead of on a PC board.

This task can be handled by some commercially available placement and routing programs that run on mainframes. However, these programs cost more

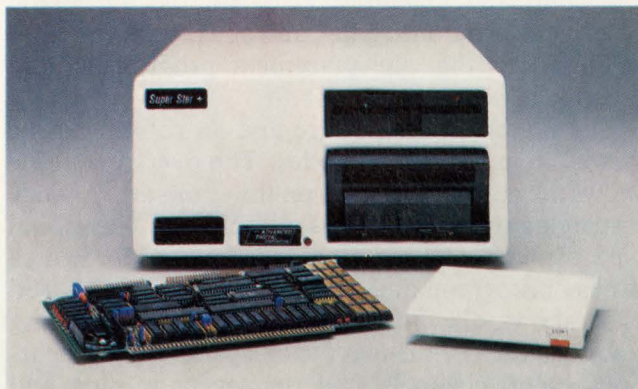
### *Gate arrays are an increasingly attractive supplement to system design using standard components.*

than \$200,000. Moreover, if schematic changes are necessary to make a given design fit onto a gate array, then the designer experiences the same feedback delay as with batch-oriented mainframe simulation programs.

Incorporating a layout capability for gate arrays into a CAE system is a more cost-effective approach. This has the added advantage of making the gate array layout program an integral part of the frontend design process, assuring a cohesive methodology. Thus far, the only CAE system to incorporate gate array layout capability is the Daisy Gatemaster.

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The incorporation of physical layout into the CAE system, like the inclusion of automatic generation of simulation input files, reduces the designer's learning curve. Widespread use of gate arrays had been hampered by the need to stick with a single manufacturer's gate array, because each manufacturer had a different development system. Each development system, in turn, meant learning a new design methodology, and each gate array required a new set of design rules.

Gatemaster simplifies the learning process by presenting one methodology that works for all gate arrays. Moreover, the design rules for each different gate array are downloaded directly into the machine. Thus, the design system keeps track of them rather than the designer.

A description of a given array's design rules is contained on the same Daisy-supplied diskette that contains a description of the bare gate array. When this description is loaded, the Gatemaster uses it to ensure that all stages of layout design are correct by construction. This brings design rule implementation up to the earliest steps in the physical layout design.

### Beginning the layout process

The Gatemaster's capability is a superset of that of the Logician (Fig 4). All the tools and techniques for achieving a fault-free logic design are also available for gate array design. In addition, the Gatemaster will prepare the design file for placement and routing, which allows fully automatic or interactive placement of the design components on the bare array. As a last step, Gatemaster prepares a formatted tape that can then be used directly by the gate array manufacturer to fabricate the array.

Software links between the simulated design file and the physical layout of the gate array in the layout editor provide the ability to merge component and network lists. These lists have been extracted from the design file with a file that describes the bare gate array. If any changes are later made in the sche-

matics, the incremental recompilation will use this function to prepare the altered design for layout.

Then the actual layout process can begin. The designer may rely entirely on the automatic placement program, or may wish to mandate the placement of certain critical components and let the automatic placement program take care of the remaining components. Either way, the entire placement and routing process will be connectivity driven. That is, the Gatemaster only allows the placement of components and networks that are in the design schematic. It also assumes the interconnection of components in accordance with the schematic. This feature is extremely important because it ensures that the layout is always correct by construction with the schematic. The layout editor also performs an extensive set of design rule checks in real time to verify that the placement and routing of all components corresponds to the gate array manufacturer's specifications.

Once the components are placed, the designer can ask the Gatemaster to display the cell placement on the bare array, as well as display histograms around the periphery of the array. This indicates figures of merit on the cell placements. Figures of merit tell the designer how much of the array the design has used so far, and whether that design is routable in its present form. To improve the figures, the designer can command Gatemaster to run the automatic placement program again, and specify the number of iterations that the placement program should attempt in seeking a better fit.

The placement procedure and its results can be viewed in any of three modes. The overview mode shows the cursor's position on the entire array, while displaying only empty cells and blocks. The global view displays component placement and is used to display histograms and figures of merit. The detailed view shows all, including the particular routing tracks on each of the two metal layers, vias, obstructions, empty channels, underpasses, pads, pins, and nets. If the designer has selected a particular net for editing, all pins, traces, and vias on the net will blink or be shown in reverse video (Fig 5).

Each of these views can be accessed instantly by pressing the appropriate view button. The designer can move quickly around the array by jumping into the overview, moving the graphic cursor to the desired chip coordinates, and then switching back to a more detailed view. If, at any time, the designer wants a plot of the current view on the cathode ray tube (CRT), the designer types Plot, selects one of four plot scale factors, and presses the Execute button. Because the panning and zooming instructions are executed in hardware on the Gatemaster, the designer can pan and zoom several times faster than with traditional software panning.

Gatemaster has three different routing programs: an automatic global route program, a channel

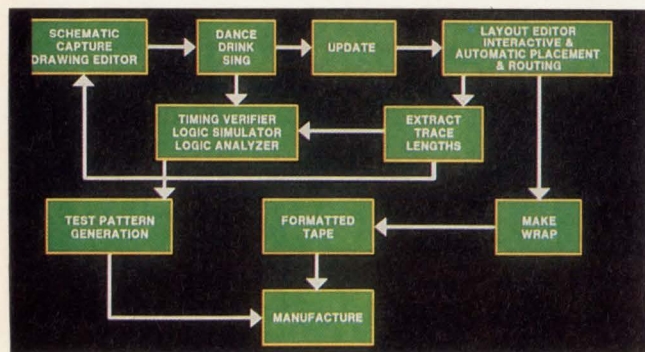
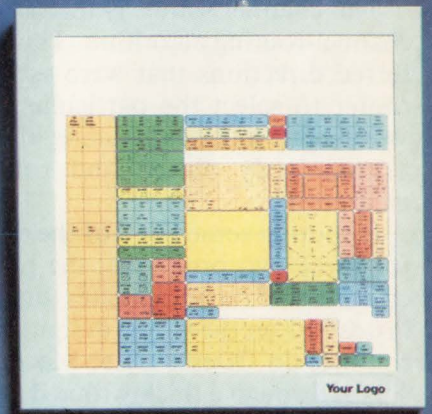
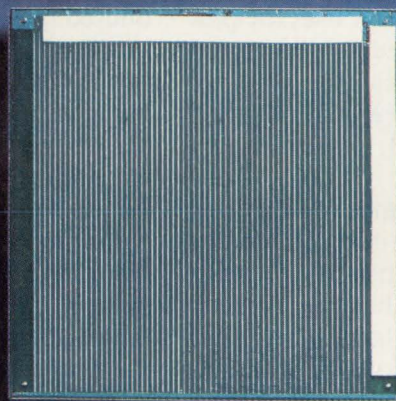
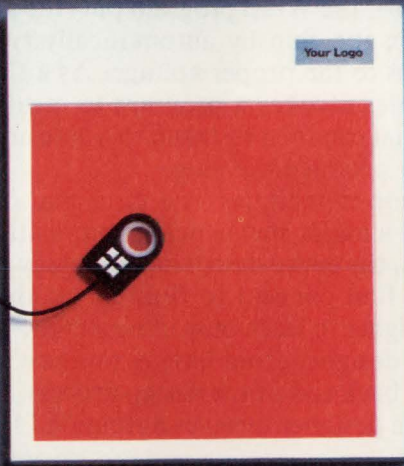
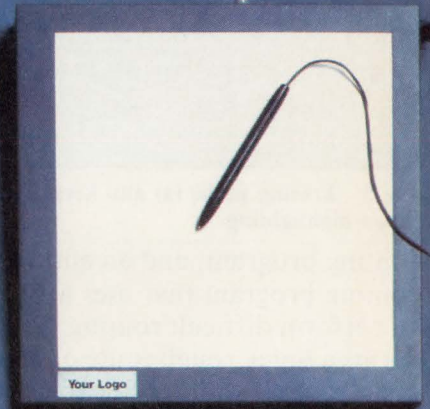
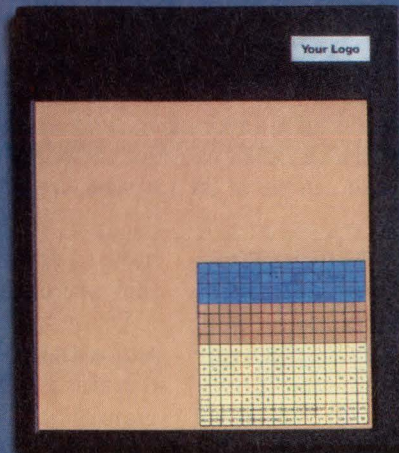
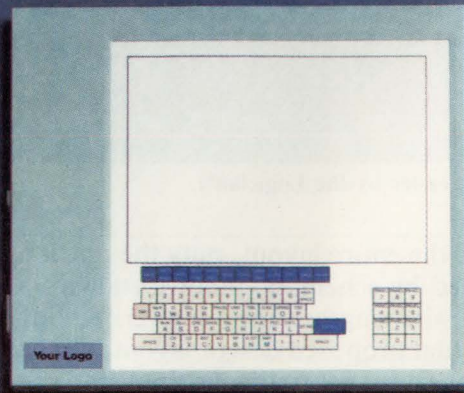


Fig 4 The Gatemaster not only provides network connectivity extraction (Dance), page linking (Drink), and simulation input file preparation (Sing), it also handles the interactive placement and routing of the logic design on the gate array. This provides formatted tape and test patterns for the manufacturer. Gatemaster's layout modules also provide back annotation to the design schematic.

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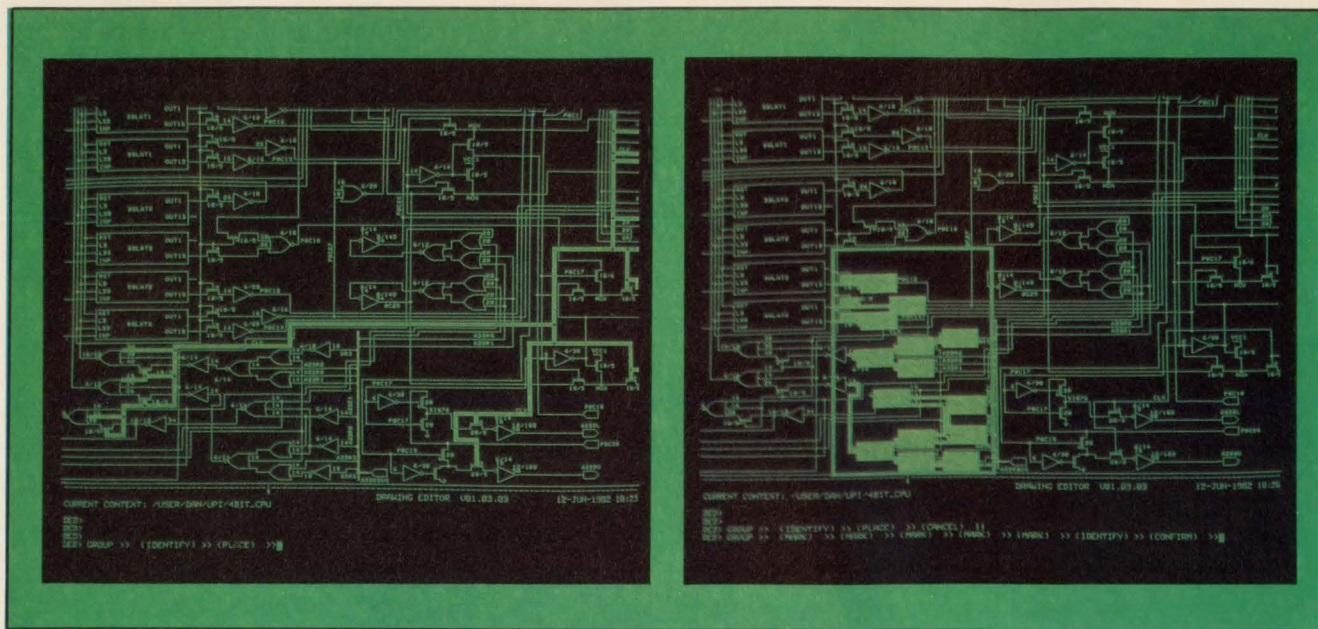


Fig 5 Tracing paths (a) and keeping track of nets (b) in the schematic are made easier by the Logician's video highlighting.

routing program, and an autonet or point-to-point routing program that uses a Lee Moore algorithm to perform difficult routing. The global router performs a quick rough route on the array. It does not concern itself with specific track assignments, it only assigns preferred directions.

The channel router is then invoked to execute a channel-routing algorithm. This router uses the preferred directions that were assigned by the global router to select the particular tracks for routing. When both routings are done, the designer may have a completely placed and routed design implementation.

If routing some parts of the design is too difficult for these two programs, the point-to-point router can handle it. It operates on a net-by-net basis instead of on the whole design, as the other routing routines do. It uses a Lee Moore algorithm to find a path through a thickly routed section of the design. If such a path exists, it will find it. To use the point-to-point routing routine, the designer simply selects the net to be routed and presses the appropriate function key.

### Wrapping it up

After generating an actual layout, the designer will want to rerun the timing verifier program using the actual wire lengths in the proposed layout. Upon rerunning the timing verifier, assumed wire lengths may be found to create race conditions or violate setup and hold time requirements. The actual layout may have made a critical path, (eg, as a clocked input to the flipflop) that is too long, slowing down data so that it is still transition before it is latched. This problem might be corrected in layout, or the designer may decide to change the schematic to take out the race condition. In such a case, the designer does not

have to rework the entire layout, only the portions that are changed by schematic modifications.

Using actual wire lengths for timing verification, and with an actual proposed design layout, all that remains is for the designer to invoke the Wrap program. For example, the Wrap program puts the polishing touches on the chip by automatically tying unused input pins to the proper voltage. As a final touch, the designer invokes a program to create a formatted tape that can then be taken to a gate array manufacturer to produce the chip.

With all of these capabilities, it is clear that CAE systems represent a major step in design automation. For the first time, the entire design methodology can be unified from first concept to finished product, requiring the designer to learn only one method. The system frees the designer from having to know the intricacies of the back end of the design process. For the first time, the designer receives automated help in the front end.

However, this design method is only the beginning. The price of such systems is expected to fall along the same curves as the prices of their component parts, including RAM, Winchester disks, CRT displays, and microprocessors. At the same time, the functionality of such systems will increase in more or less the same fashion as semiconductors.

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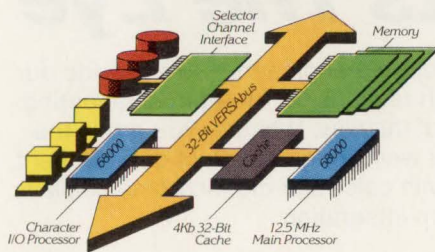
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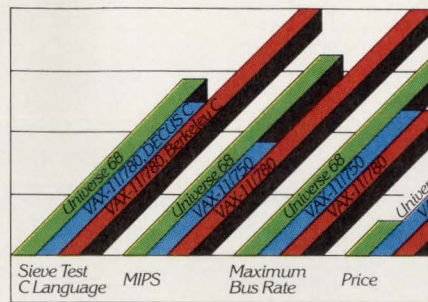
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# SPECIAL REPORT ON MINICOMPUTER SYSTEMS

As 32-bit microprocessors begin their invasion of the marketplace, minicomputer system designers search for alternatives to maintain their share of the pie. Microcomputers have been responsible for upsetting the previously stable position of traditional minicomputers. They must also be credited for the growth evidenced by 32-bit minicomputers. The pressure exerted on low end machines has not only widened the market, but has also forced manufacturers to look at higher performance 32-bit systems. Meanwhile, the power being packed into these machines has brought them into competition in areas traditionally the province of mainframe level machines. It has also given them the power to fit into rapidly growing application areas.

Pressure from above and below has not stunted the market, but has instead fostered its growth. Predictions are that the market will come close to \$3 billion in 1984. Even IBM has, for the first time, used the word "supermini" in a recent product announcement. Others have been just as fast to move in. Traditional vendors have filled out their lines with board-level and high end machines, as well as every performance level in between. Newcomers to the arena have introduced concepts that were heretofore only experimental.

While some traditional vendors take on state-of-the-art technology to expand existing lines, others add hardware to enhance performance levels. Newcomers tailor their architectures to support high level languages and standard operating systems in what may become the way of the future. Reducing the size of the instruction set is yet another ploy used to limit complexity and gain performance. This too shows great potential for future systems.

Looking at the ways and means taken to achieve these aims, this report considers both traditional and new wave system design. Both evolutionary and revolutionary designs bring the industry an aura of excitement. Even old hands may remark that there is indeed "something new under the sun."

*Peg Killmon*

Peg Killmon  
Senior Editor

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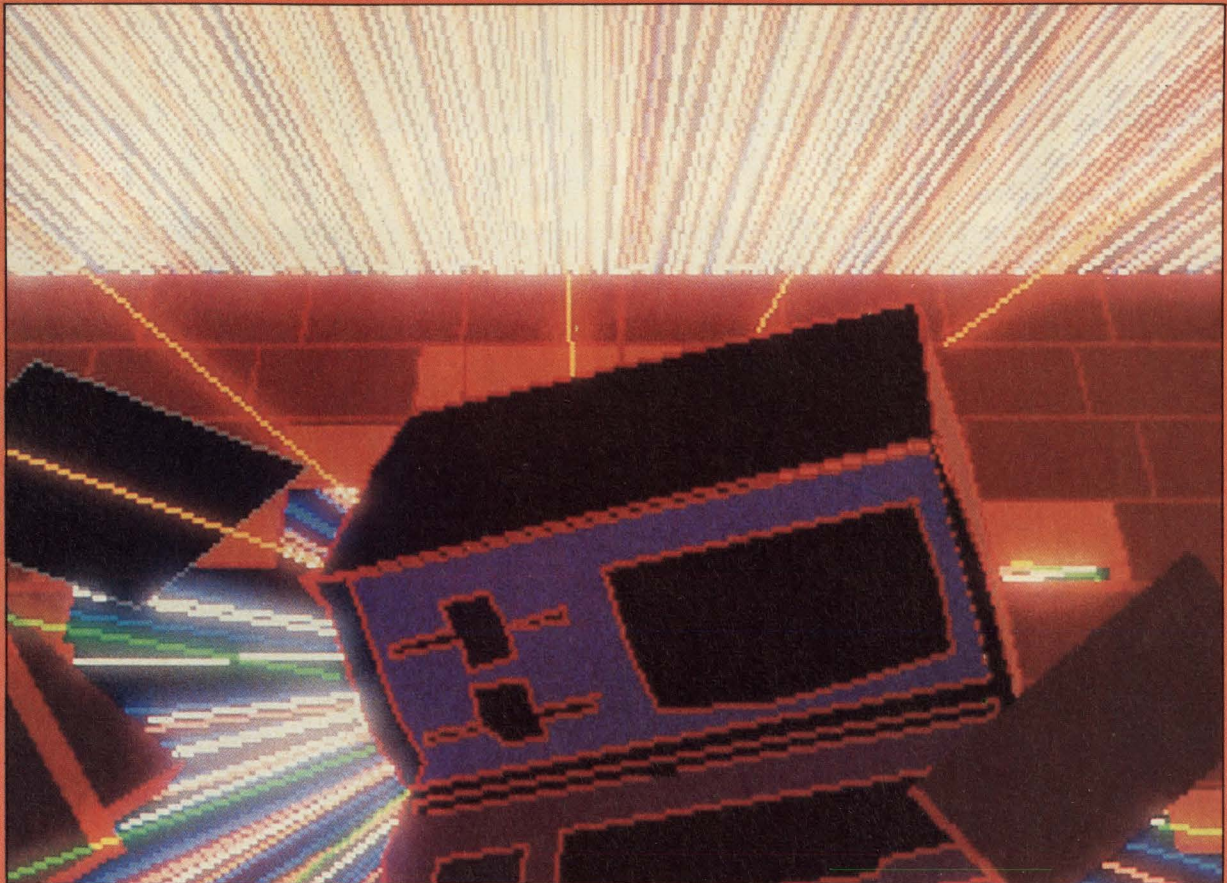
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# SUPERMINIS: CHANGING DIRECTION FOR THE FUTURE

**Breaking the evolutionary trend, newcomers bring innovative architectures to the superminicomputer performance race.**

---

by **Peg Killmon,**  
**Senior Editor**

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Breaking free from constraints that have bound them to a proscribed architecture, new 32-bit minicomputers promise real competition in the price/performance race. Using concepts fresh from research labs, newcomers in the field bear watching as oncoming machines boost performance to competitive levels while keeping costs in line.

Taking aim at a market that has been dominated by Digital Equipment Corporation's (Maynard, Mass) VAX family since its introduction in 1977, the new breed hopes to step into the breach created by DEC's failure to field a high end machine in the VAX line. Propelled by rumors that the new VAX flagship will debut next year, newcomers hurry to market. Recognizing the need for haste, they have sidestepped the software development cycle by adopting Unix or Unix-like operating systems. Using standard off-the-shelf parts has further reduced the length of their design cycle, while guaranteeing a higher performance follow-on product. Crucial to the performance of these machines is a new way of doing things.

A Unix dedicated machine implements the reduced instruction set concept drawn from laboratory research activities. A Lisp language processor furnishes the facilities to handle the stack computations and function calls demanded by that artificial



**A high performance 32-bit minicomputer, Perkin-Elmer's 3250XP permits easy migration from 3 MIPS to 21 MIPS. Reducing the cost of entry, the 3250XP upgrades to a 3200MPS multiprocessor with the addition of a \$37,000 Power Pak.**

intelligence language. Promising to contend with both minis and mainframes, a 64-bit multiple processor system claims data rates to 213M bps over a 64-bit wide system bus.

Meanwhile, more traditional vendors have not been idle. Among their contributions—single-board implementations of high end CPUs and an increasingly large range of compatible systems—a chip level implementation of the famous VAX architecture has finally appeared.

### **What's in a name?**

Tagged superminicomputers to distinguish them from their more stable siblings—the minicomputers—these machines sport internal word lengths greater than 16 bits, but have established 32 bits as their trademark. Other distinguishing characteristics consist of 1M-byte or more main memory with a similar logical address space. Major system elements hang together over a bus structure. Thus, superminis are distinguished from minis by their word length and direct addressing capability, and from mainframes by their use of a bus rather than point to point structure. In other aspects, they resemble mainframes much more closely than they do their ancestor, the 16-bit minicomputer.

Their 32-bit architecture gives these systems certain advantages. The 32-bit bus structure, on which part of this definition is based, not only allows rapid data movement, but also supplies fast access to masses of data. By formulating memory addresses in 32-bit registers, these machines can directly address 4,294,967,296 memory locations. Thus, large programs can be accommodated, vastly increasing their application areas.

Another attribute of the larger address space is the ability to readily implement virtual memory schemes and to provide some measure of memory protection. Add to this the arithmetic precision attained when dealing with 32- or 64-bit numbers and the facility to implement multitasking systems and you have speed, power, and precision all wrapped up in an increasingly neat package.

While mainframes have supplied these attributes for years, minicomputers still hold the edge when it comes to size, interactivity, and price—with systems generally falling in the \$40,000 to \$300,000 range. Said to account for \$1.6 billion in sales last year, superminicomputers will compound that at an annual rate of better than 30% to pull in \$4.8 billion in 1986. These numbers, from Venture Development Corp's "The Superminicomputer Industry 1981-1986: A Strategic Analysis," reflect the growing number of applications into which the systems' increasing power and performance slot them. Among these is the rapidly expanding computer aided design/computer aided manufacturing (CAD/CAM) area, which feeds on the computa-

tional capabilities provided by the current crop of superminis and, self-aggrandizingly, will supply the potential for future mechanisms.

In computational areas such as this, superminis have a sure toehold, because of their large program size, volume of data storage, and timesharing facilities. In the more traditional scientific and engineering applications where they began their illustrious career, they run the high level scientific languages necessary to handle the complex algorithms that manipulate the masses of raw data. Not only that, but rising ratings on Whetstone benchmarks demonstrate their dedication to continuing to provide more scientific processing per second per dollar of cost than either mainframes or minicomputers.

### **How they got that way**

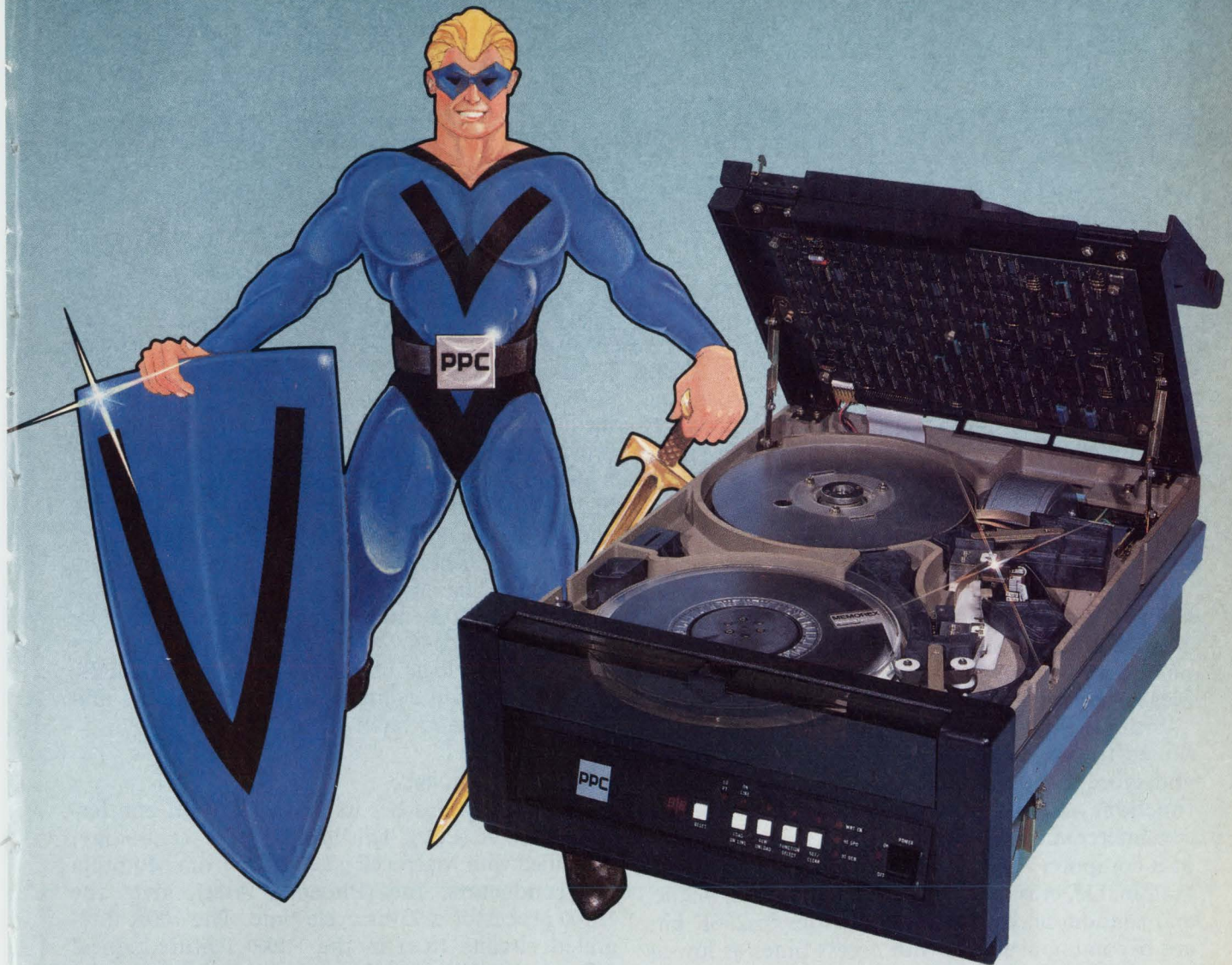
Today's leaders exhibit performance that overlaps that of low end mainframes such as the 43XX family from IBM Corp (Rye Brook, NY). Striking fear in the hearts of established mini vendors, IBM's 43XX series added even more potent competition with the arrival of the "Glendale" series in mid-September. Reflecting the company's drive to reduce prices by 25% per year, the 4361 model 4/5 sells in the \$150,000 to \$200,000 range. The 4381 models fit between 4341 and 3083 processors with 2 and 2.7 million instructions per second (MIPS) ratings. The 4361 models are rated at 1 and 1.4 MIPS in commercial applications; scientific ratings are from 2 to 3 times higher.

Scientific ratings on the 4361 are achieved by adding a high accuracy arithmetic facility and a hardware floating point multiply accelerator. The unit's instruction processor and cache buffer have a 100-ns cycle time, while an input/output (I/O) processor operates concurrently with the instruction processor. Still, performance leaders in the superminicomputer class offer resistance to this infringement on their territory. Some even compete with IBM 308X processors.

What gives them all this power? Well, take a look at what's inside. Just as minicomputer capabilities were extended by drawing upon existing technologies, forays into the mainframe bailiwick have brought them technological advances that further broaden their power base. Used to advance high end performance, pipelining, parallel techniques, and cache memories all derive from mainframe systems.

In the performance race between machines in this class, components and architecture are the major forces. Higher and higher density components now compress 2000 or more gates into a small fraction of the total available circuit board area. In addition to their role in developing the high density memory modules that have lifted superminicomputers into expanded roles, they also play a major

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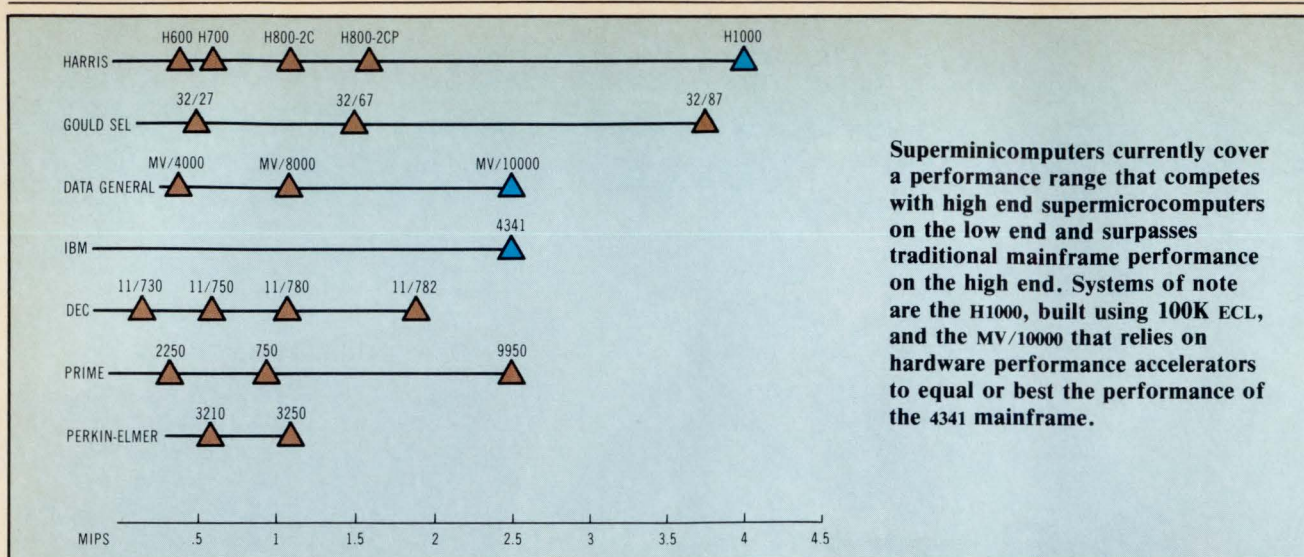
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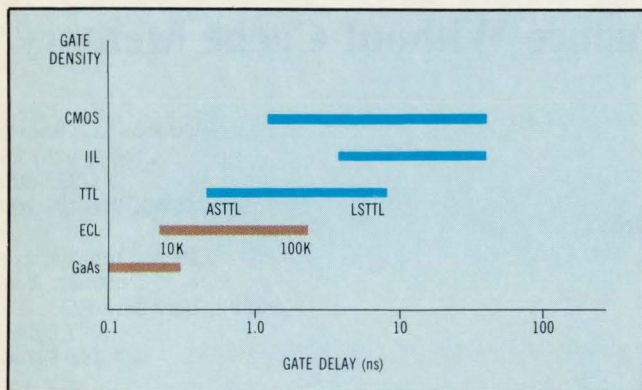


part in putting more function into the processing engine itself. This density not only allows designers to put more function on a board, but provides these functions at lower cost, higher speed, and with lower power requirements.

### Using what you've got

Some machines use advanced components as soon as they emerge from the laboratory in sufficient numbers. Others rely on standard parts, but put them together in novel ways that result in increased performance.

From the days of the transistor, parts have continued to provide more function, more flexibility, and more speed. The choice of prepackaged logic functions now ranges from the simplicity of one or two interconnected logic elements to the complexity of a computer. Memory chips are available in programmable, erasable, reprogrammable, nonvolatile, and random access forms. Capacities to 256K bits are becoming available with access times as low as 100 ns. IBM recently talked about an experimental 512K chip that can be read from in 120 ns.



Complexity of gate arrays ranges from a few hundred to 8000 gates on commercially available CMOS chips. Gate delays, technology dependent, range from 200 to 400 ps on bipolar ECL circuits to 0.8 to 2 ns on Schottky TTL, integrated Schottky logic (ISL), and Schottky transistor logic (STL). CMOS delays are dropping steadily as design rules shrink down toward 3  $\mu$ m.

As alternatives to the small scale integration/medium scale integration (SSI/MSI) devices that provide fixed functions with fast gates, more flexible, high density devices are used to build compact, high performance systems such as DEC's VAX-11/750 and -11/730, Data General's (Westboro, Mass) MV/10,000, and Harris Corp's (Fort Lauderdale, Fla) 1000. Depending on design alternatives, design constraints, and function being implemented, gate arrays, standard SSI/MSI devices, custom arrays, or programmable logic fill the bill. The choice usually is resolved by an examination of constraints and their relative importance.

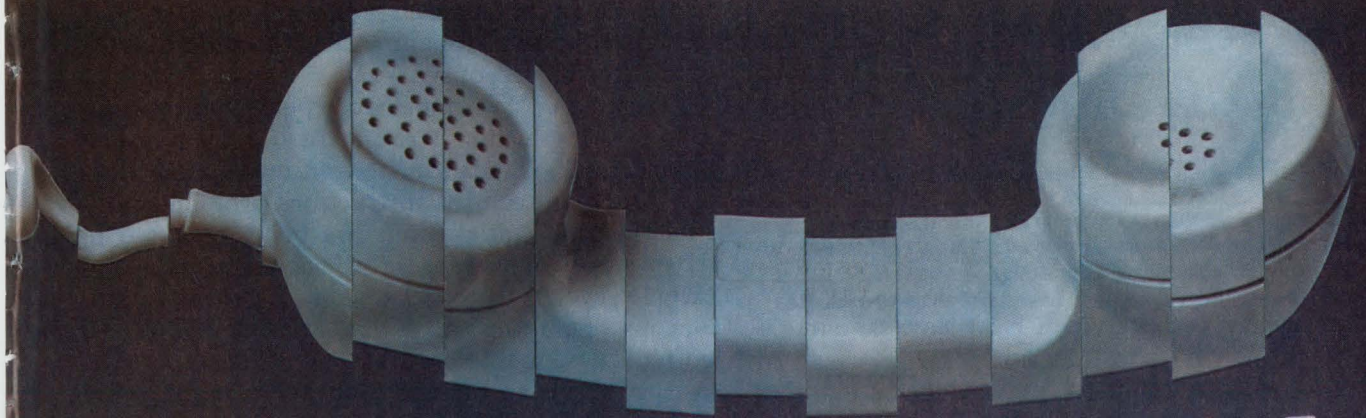
### Here's what you get

Harris Corp has bet its stake on 100K emitter-coupled logic (ECL). This leading edge technology, combined with Macrocell gate arrays from Motorola Semiconductors, Inc (Phoenix, Ariz), gives the H1000 processor a 75-ns cycle time. The 100K integrated circuits (ICs) in the H1000 feature typical 0.75-ns gate delays, with counters, registers, and flipflops operating in the 400- to 500-MHz range. This doubles or triples the performance potential over Schottky transistor-transistor logic (TTL) or other ECL families. Use of ECL also allows high speed large scale integration (LSI) circuits and static random access memories (RAMs) to be used. This is critical to the CPU's high operating speed.

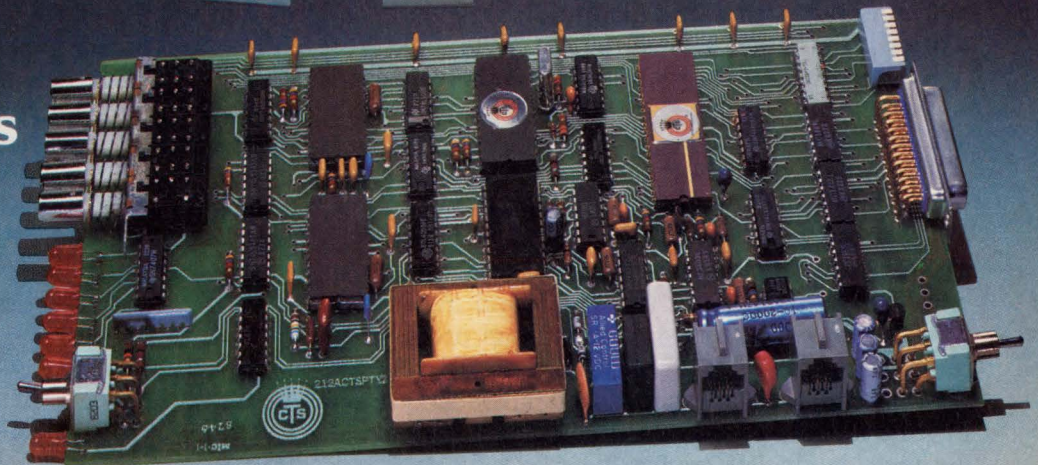
Proprietary circuit integration and packaging technologies enable 60,000 logic gates and 1M static RAM bits to be incorporated on a single CPU card. Thus, the same cabinet and footprint size can be kept while performance, function, and reliability are increased.

Pure semiconductor technology holds this machine out in front. A close rival, the Gould/SEL (Fort Lauderdale, Fla) 32/87, relies on dual processing units to wring performance out of its machine which is based on older, slower 10K ECL technology, while Prime Computer's (Natick, Mass) 10K ECL machine uses speed enhancing techniques

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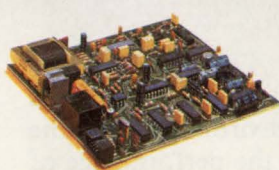


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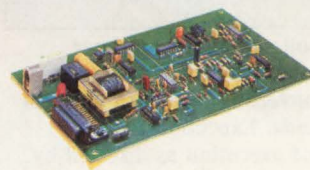
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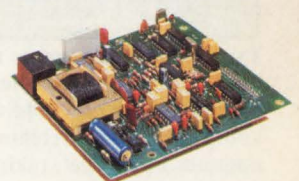
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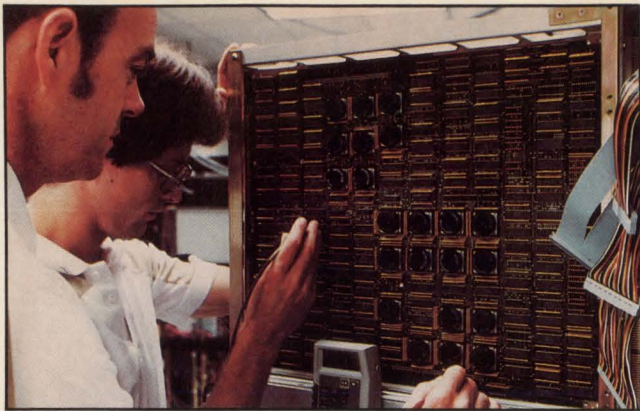
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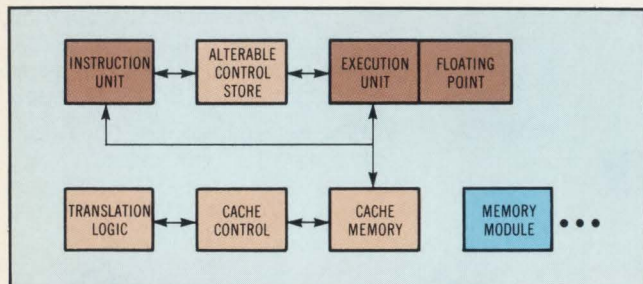
Harris' H1000 uses 100K ECL integrated circuits to earn Whetstone ratings of 4 MIPS. PC boards that accommodate the LSI and MSI circuits and custom designed gate arrays use embedded resistor technology. Lasers are used to etch the boards, and the termination resistors are physically buried in the boards.

within the CPU to boost performance. Another machine that relies heavily on processing techniques rather than semiconductor technology for speed is Data General's latest, the MV/10,000, which is built using advanced Schottky TTL combined with bipolar bit slices.

The second factor in the equation—architecture—determines how these components are used. Among the wrinkles made feasible by the ready availability of high density, high speed parts is the concept of parallelism. Parallelism may be found in instruction stream processing, in data stream processing, or in some cases, in both. There are two major ways in which parallelism can be introduced: a set of functional units may be organized to compute in parallel, or pipeline processing may be used.

### Two ALUs are better than one

Parallelism increases the speed of the CPU by processing several instructions concurrently instead of sequentially. While one instruction is being executed in the arithmetic logic unit (ALU), the next instruction is being read from memory. By introducing another ALU into the processor unit, two or more instructions can be executed at the same time. Although the amount of hardware necessary



Typical functional units with 32-bit superminicomputer CPUs. Instruction unit handles instruction fetch and decode, computing operand addresses, converting logical to physical addresses, and prefetching operands. Execution unit operates in parallel, taking care of execution as directed by microinstructions from control store.

increases with added parallelism, hardware costs have fallen to the point where parallel processing techniques are economically feasible.

Pipeline processing techniques break a sequential process down into subprocesses. The pipeline, a collection of specialized processors, performs part of the process in each processor and passes the result to the next. This allows several computations to occur simultaneously.

A common place to introduce pipelining concepts is in the instruction stream. Also known as an instruction lookahead buffer, an instruction pipeline reads consecutive instructions from memory while previous instructions are being executed in the processor. This causes the instruction fetch and execute cycles to overlap and perform simultaneous operations. If a first in, first out (FIFO) buffer is used to implement the pipeline, a queue of instructions is formed to wait for decoding and execution on a FIFO basis.

In a 4-segment pipeline, such as that used by Ridge Computer (Sunnyvale, Calif), the sequence consists of fetching from memory, calculating the effective address, fetching the operand from memory, and executing the instruction. This sequence, used with a FIFO buffer, will keep the pipeline full until a branch instruction is encountered. There are, however, a couple of kinks that can slow down the process. For example, if the branch takes the next instruction outside the prepared-for sequence, then the information in the first two segments of the pipeline must be discarded and the pipeline refilled with the next instructions.

Since this can degrade performance from the expected maximum, some designs have taken steps to avoid it. In Prime's 9950, for example, in addition to the instruction stream, the machine tracks program branches. On encountering a branch instruction in the prefetched instruction stream, it attempts to predict which direction the branch will take. Based on predictions, instructions from that branch are prefetched and stored in the 256 entries of a branch cache memory. This technique claims an 80% success rate.

The technique used by Ridge Computer puts "compare and branch" logic in the prefetch unit to predict branches. Both conditional and unconditional branches are detected within the prefetch unit. Another means of forestalling degradation is to store instructions from both possible branches, then to discard those pertaining to the branch not taken.

### Using parallel techniques

Gould/SEL builds dual internal ECL processors operating in a multiple stream environment into the 32/8780 multiprocessor to boost the performance of their Concept/32 series machines. Two separate



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# COMTAL



CPU, IPU, and floating point processors in Gould's Concept 32/87 minicomputers are implemented in 10K ECL. The systems attain 4 MIPS performance levels through large cache memory, 4-stage instruction pipeline, and dual instruction/execution unit architecture.

processing units within the processor complex operate on multiple instruction streams. The CPU handles I/O, interrupt and computation, while the internal processing unit (IPU) concentrates on computational tasks. Both processors have access to main memory. Each internal processor is complete with execution/instruction unit, cache, control store, and floating point processor. Internal 75-ns buses connect functional units within both CPU and IPU.

Honeywell's (Waltham, Mass) most recent entry in the 32-bit minicomputer arena is the top of the line DPS 6/95. This unit starts with 2M bytes of memory and adds in increments up to 16M. Its central subsystem includes high speed cache and three separate processors—central processor and parallel commercial instruction and scientific instruction processors—linked through 32-bit data paths. The memory bus supplies 32 data lines and 24 address lines operating in an asynchronous split cycle mode. Data transfers from main memory occur through the extended Megabus to cache in the central system. All three processors access this cache to execute data as appropriate, providing response time and throughput of a 1-MIPS system. Incorporating advanced microprocessor technology, system architecture is based on the 30-slot Megabus chassis.

To meet high performance needs until their high end VAX appears, DEC has constructed a dual-

processor configuration of the VAX-11/780. The VAX-11/782, a tightly coupled asymmetrical multiprocessor system, joins two VAX-11/780s. Both processors share the same operating system, code, and data structures, interacting transparently through shared memory. This coupling of processors achieves a performance improvement of 60% to 80% over that of a single-processor system.

The VAXcluster concept takes this one step further using network technology. Tying as many as 16 VAX-11/780 or -11/750 processors together into a loosely coupled complex, this scheme is based on a 70M-bps interface and a passive star coupler. Each processor runs its own copy of the operating system and can access all files in the cluster, whether local to another processor or shared.

Perkin-Elmer's (Oceanport, NJ) attached processor approach builds on existing 3200 machines. The 3200MPS exemplifies multiprocessing concepts, attaching up to nine associated processors as slaves to a controlling central processor system. This tightly coupled, asymmetric system of processors communicates through a single global memory. The CPU manages all system resources, scheduling auxiliary processing unit (APU) memory management, I/O, and fault handling. APUs execute user program code simultaneously with the CPU and other APUs. Machine performance potential is realized when the application can be segmented into separate tasks to take advantage of parallel processing. A full blown system with CPU and nine APUs has been benchmarked at a 21-MIPS Whetstone rate.

### Changing the way it's done

While developments over the past few years have relied primarily on hardware advances to step up processing performance, new wave machines blend advanced technology with innovative software concepts to achieve even more spectacular results. Representative of this approach is the 1-to-8 processor system built by Elxsi, (Sunnyvale, Calif). Their System 6400 represents the culmination of recent breakthroughs in hardware technology combined with new concepts in operating system design.

Semicustom ECL gate arrays compress the CPU of Elxsi's 64-bit System 6400 onto three multiwire boards. Each CPU in the multiprocessor complex operates on a 50-ns cycle time, completing some 64-bit instructions in 100 ns. Systems expand from one to ten CPUs without modification to software or existing hardware and claim to deliver from 2.5 to 20 MIPS. Central to the machine's bus oriented architecture is the main system bus, the Gigabus. Providing an effective system bandwidth of 320M bytes/s (compare this to Gould's 26M-byte/s or Perkin-Elmer's 64M-byte/s bandwidth) with usable data rates ranging from 160M to 213M bytes/s, the bus serves as a synchronous 64-bit



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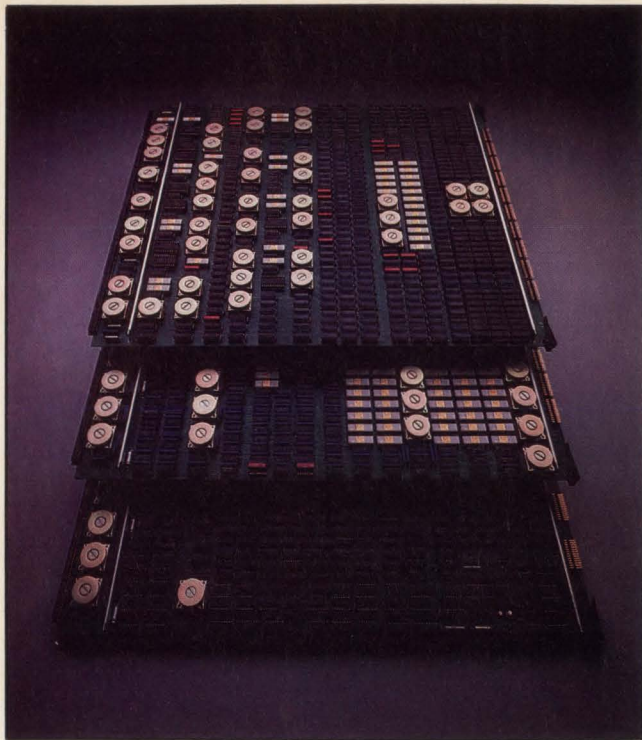


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Display Image  
Unretouched

CIRCLE 95



A 64-bit multiprocessor, Elxsi's System 6400 delivers 2.5 MIPS in a single processor configuration. Key to this power are the ECL and high density LSI components that form the system's modular tightly coupled processing units.

wide channel that connects all major system components. With 192M bytes of main memory, the system accommodates memory intensive applications.

Message-based, Elxsi's EMBOS operating system organizes resources and provides load balancing by distributing processes across multiple CPUs. The message-based concept eliminates the need for privileged instructions or addressing modes. Data movement from one domain to another is handled only through the message system. Each CPU contains messenger and scheduler functions as firmware. This improves performance and reduces operating system complexity.

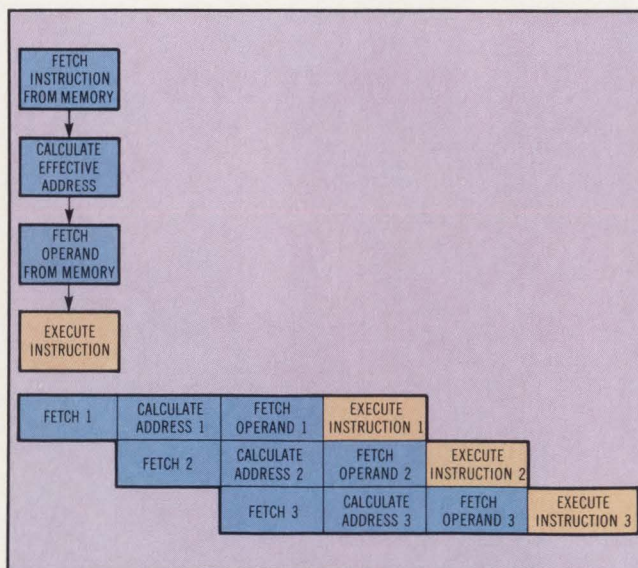
Another candidate for new wave honors, Pyramid Technology's (Mountain View, Calif) 90x leaves the advanced technology to the next generation and draws on a smaller, simpler instruction set for performance, using a reduced instruction set computer (RISC) concept. Hoping to draw supporters from the established Unix base, the machine is totally dedicated to the Unix operating system. Ridding itself of the high overhead usually devoted to developing operating system software, the young company has focused on getting optimum performance from standard hardware.

The 3-board CPU comprises instruction, execution, and microcode sequencer implemented using fast Schottky TTL parts. Operating in a 3-stage pipeline, the processor separates instruction pre-fetch, operand prefetch, and instruction execution steps, performing most instructions within two

125-ns processor cycles. The real key to performance, however, is said to be the processor's register intensive architecture. The 528 32-bit internal registers are divided into 16 global registers, and an additional 16 levels of 32 registers each. This stack arrangement allows transparent allocation of 32 registers to each procedure as called. This not only makes it easier to keep track of subroutines, but enables operations to be performed register to register. As such they occur 2 to 4 times faster than cache operations and 8 to 10 times faster than memory operations. All this makes access faster and hardware simpler and provides faster generation of code from the compiler.

The instruction set consists of about 90 micro-coded instructions compared to a typical set of upwards of 200 for a traditional supermini. For example, in an addition operation, DEC's VAX would use 66 instructions, while the RISC system requires only 9. The set retains, however, those instructions necessary to support floating point, memory management, and operating system functions.

Another example of the power obtained by simplifying the instruction set, Ridge Computer's Ridge Thirty-Two achieves an 8-MIPS rate. The instruction set limits addressing modes and incorporates only basic operations such as the load, store, and arithmetic operations that predominate in high level scientific languages. Whereas the VAX allows any addressing mode on any instruction—an orthogonal instruction type—this machine provides a single register oriented addressing mode for each arithmetic operation. Like the VAX, the Ridge system is a register oriented machine. However, its architecture contains sixteen 32-bit registers. Uniformity allows any arithmetic or address operation to be performed on any register. Built like the Pyramid



Execution of instructions can be staged by providing separate partial processors, each dedicated to one portion of the instruction sequence. Preexecution steps can thus be performed in parallel, resulting in higher total throughput.

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system, from off-the-shelf bipolar MSI and LSI components, the processor uses pipelining techniques in combination with the simplified instruction set to boost processor speed.

### **And more to come**

Rumor has it that a minicomputer based on this concept will make its debut from IBM. This one reportedly takes its lessons from the experimental 801, talked about at scientific meetings in the late 70's. Dubbed the 802, and based on the RISC concept, it is expected to appear in a minicomputer type architecture sometime in 1984.

Under development in Irvine, Calif, for release late this year, is a 32-bit processor that relies on custom chips and high speed TTL circuits to implement two parallel ALUs. Changes in traditional CPU architecture result in a 100-ns processor cycle time. One ALU performs the usual arithmetic tasks and logic comparisons while the second handles only the lookahead carry operation. This eliminates the buffer that normally sits between the ALU and lookahead carry generator along with its delay time. Planned for release in one to four processor configurations, each processor is capable of 2 MIPS, double the rating of a single-processor VAX-11/780.

### **Making machines smarter**

Other machines have taken on the task of bringing artificial intelligence out of the universities and making it more useful. Always limited to mainframe systems because of the enormous quantities of memory required, advances in semiconductors enable these systems to run on more affordable machines—witness Symbolics and Lisp Machines.

Among those machines destined to bring artificial intelligence languages into more common use, LISP Machines' (Culver City, Calif) Lambda supports the Lisp language in such a way as to make it feasible for commercial use. To run Lisp, with its intricate linking mechanisms, a processor must supply large storage capacity. Whereas the architecture of a typical machine is designed for numerical languages such as Fortran, Lisp's nature requires stack computations and function calling.

Drawing on experience with the original Lisp machine, the MIT CONS, Lisp's processor builds on a high performance Nubus. Nubus, a device independent architecture, is based on a 32-bit bus with 37.5M-byte/s transfer rate. The processor itself uses high speed Schottky TTL in a 32-bit microprogrammable design that pipelines execution of complex order codes. The four boards making up the processor divide up functions: ALU, dispatch logic, and scratchpad; control memory; memory interface; and random gates. On the memory interface board along with cache, a specialized high speed cache state machine manages memory access in a

lookahead, lookbehind mode. Memory access occurs through a 2-level virtual paging system that uses three virtual to physical address maps.

Macro instruction addresses are fetched two at a time, and decoding hardware operates in a single operation to save processing time. Both pipelining and operation of the virtual control store are handled by the microprogram.

Scratchpad and dispatch memory hold multiway branch tables. Another scratchpad includes a 2K pointer addressable RAM that stores the top of the system stack in a manner similar to that of a cache. The recursive nature of Lisp causes a large percentage of main memory references to go to the stack, speeding processing.

Based on a 36-bit tagged, stack oriented architecture, Symbolics' (Chatsworth, Calif) System 3600 uses 32-bit data paths and executes 1M instructions/s. It fills Lisp's requirements for large main memory and processing power by supplying 2.3M-byte RAM that expands to 34M bytes and a 20M-byte/s memory bus for data transfers.

### **Making memories faster**

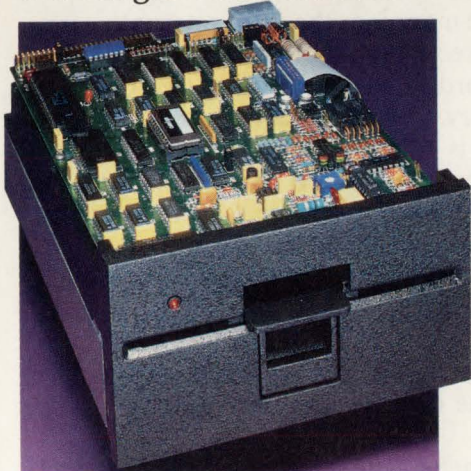
An important attribute of machines of this caliber is ability to directly address quantities of memory. These large memories, however, are slow. Since pipelined processors execute instructions at least twice as fast as they can be fetched from main memory, designers have devised means to more closely match memory and processor speed. Here is where memory interleaving, mapping, and cache memory techniques play their part, and where the decreasing costs of high speed, high density memory come into play.

To fill the demands for large memory spaces 64K RAMs are crammed onto boards to form memory modules storing from 1M to 2M bytes each. When one or more of these heavily loaded boards are put in a system, designers shorten the access cycle through interleaving techniques. This technique arranges memory modules into separate banks, one containing even addresses, and the other odd addresses. Now the processor can access sequential addresses without waiting for one to complete before beginning the other. With 4-way interleaving, four memory accesses can occur concurrently to four separate modules. Self-interleaving memories as in Prime's high end 9950 allow multiple accesses on the same module through a multiple port structure. Gould/SEL's low end 32/27 allows two read cycles to be overlapped on one module; write cycles need two modules for overlapping.

While economics force designers to stick with 64K RAMs in medium speed ranges for main memory, there are higher speed parts available, albeit at a substantial premium. The trick is to use small amounts of the very high speed devices—in the 25- to 45-ns speed range—to store instructions

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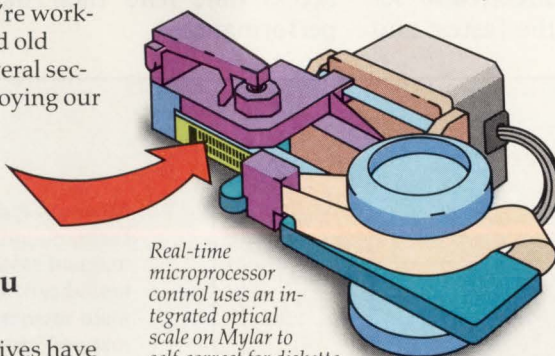
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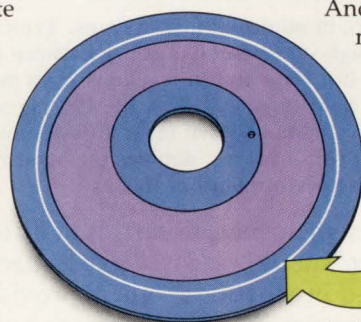
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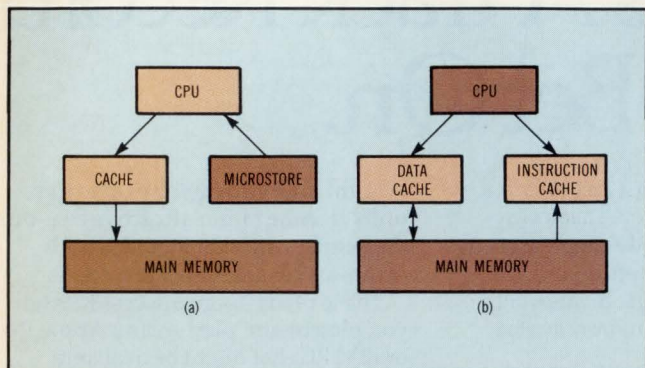
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or data that are most likely to be next in line for execution. Then, most memory accesses can take place from this small fast memory, and access to main memory can occur as a background task, without substantially slowing down the instruction execution process.



**Memory's place in minicomputer systems.** Typical placement puts a single high speed cache memory between the CPU and main memory (a). Data and instructions from main memory reach the processor through the cache. Placing separate data and instruction caches between main memory and the processing unit (b), however, doubles the bandwidth to memory, solving performance problems.

Again, designers have done this in different ways to suit their special needs. Some machines mix operands and instructions, others provide separate stores to allow simultaneous access to both. (This is most useful when the processor uses both instruction and data stream pipelining techniques.) Also differing are the means of correlating main memory addresses with cache memory addresses. The size of cache relative to that of main memory is also a trade-off, with some systems using large single or double cache, some using large instruction and small data cache, and some using just one small cache to do the whole job.

Mapping processes—the means of correlating the main memory address of a piece of information to its location in cache—need to be considered in relation to cache memory. Of the three types of mapping procedures—associative, direct, and set associative—associative mapping is the fastest and

most flexible. It is also the most expensive because of the added logic associated with each cell. However, speed results from its ability to store both the address and content of any memory word in any location.

Direct mapping divides the CPU address into two fields—an index and a tag field. Each word in cache consists of the data word and its associated tag. When the CPU accesses cache, the index field is used for the address in cache. The tag field of the CPU address is compared to the tag on the word read from cache. If they match, the desired data is taken from cache; if they don't match, the word is taken from main memory.

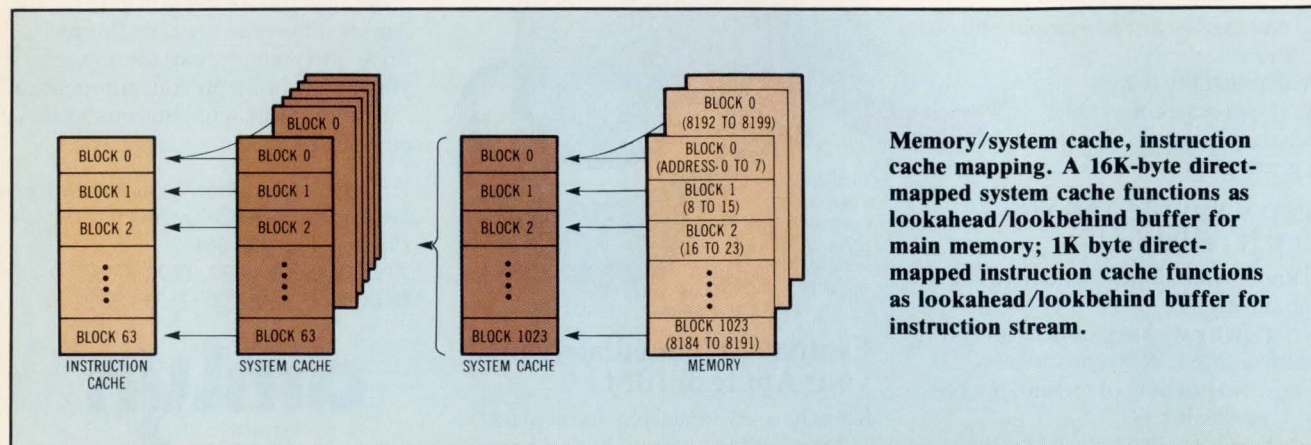
Set associative mapping, the third alternative improves on the direct mapping technique. Using this scheme, each word of cache can store two or more words of memory under the same index address. Each data word is stored with its tag. The number of tag word items in one word of cache is a set. A set associative memory of set size  $K$  accommodates  $K$  words of main memory in each word of cache.

The 8-way set associative cache used in Gould's 32/87 expands to supply from 32K to 64K bytes of fast memory to both IPU and CPU. Separated into instruction and operand stores, cache allows a double word fetch to the CPU/IPU with an effective 75-ns access time.

Harris' ECL cache also segregates operands and instructions, providing 3K bytes for each. This processor sends a request to both direct mapped cache and main memory, eliminating delays if information requested is not in cache.

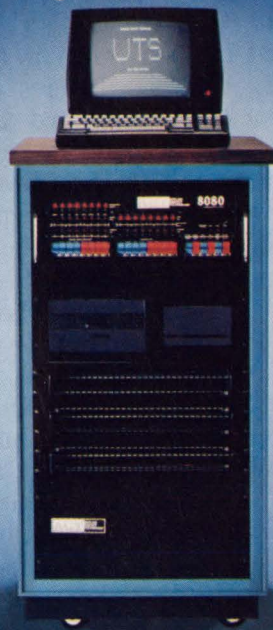
Cache memory within Prime's 9950 CPU provides 16K bytes of storage with a 40-ns access time. Its 95% hit rate results in an effective main memory access time of 84 ns.

Memory in Pyramid's system is arranged as an 8-word block device allowing 8-word blocks to be read one block/cycle after a couple of cycles of set up time. The 4K-byte set associative code cache and 32K bytes of optional data cache with 125-ns access time lend their hand to speed processor performance.



**Memory/system cache, instruction cache mapping.** A 16K-byte direct-mapped system cache functions as lookahead/lookbehind buffer for main memory; 1K byte direct-mapped instruction cache functions as lookahead/lookbehind buffer for instruction stream.

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Ridge's machine avoids problems of self-modifying code machines by separating code space from data space and forbidding store operation access to code space. The 256-byte instruction cache has a 125-ns access time warranted by the speed of its main memory.

### **Making more look like less**

Another trend fostered by the increasing availability of high density components is the computer-on-a-board concept. This time, however, instead of micro-based minis, we're talking about putting the power of a 32-bit CPU on a board.

All major manufacturers of 32-bit systems have managed to field a family of machines that spread across a wide performance/price range. This is easily accomplished by trading one device type off against another. Performance features can be left out to gain lower cost, or cost benefits can be attained by simply using lower cost standard parts. All of this results in a range of possibilities, one of which is the computer on a board.

Bringing the power of the VAX down to the micro level, DEC's microVAX I can sell for under \$10,000. Even at that price, the system packs in the power of the 11/730 (former low end of the VAX line) with full VAX instruction set and virtual memory capability. Termed a "bridge" unit, the system is based on the Q-bus rather than the Unibus of other members of the family. This provides users with the full complement of LSI-II and Micro 11 compatible peripherals, more in line with system costs than Unibus peripherals.

Inside the basic box, quad modules hold a 2-board CPU, 512K to 2M-bytes main memory, and SLU. The box is roomy enough to hold a 5" 10M-byte Winchester disk. The CPU boards use a 32-bit wide single data path chip implemented in very large scale integration (VLSI). This 64-pin N-channel metal oxide semiconductor chip (NMOS chip) provides 48 internal registers. Micro control store uses 40-bit wide microwords resident in five 8K-byte read only memories (ROMs). The second memory management board is based on discrete logic. It provides an 8K-byte cache and a 512-entry translation table to hardware map virtual memory. The Q-bus supports addressing for 4M-bytes of physical memory, as well as block mode data transfers at 2.5M- to 3M-byte/s rates.

To bring their 3200 series processor down from four boards to a single board, Perkin-Elmer applied advanced VLSI technology and component packaging techniques. The result, a fully configured system in a 30" cabinet, runs all high level software, both system and applications, written for the 3200 series.

Packed on the CPU board in the 3205 are 1M bytes of memory, memory addressing to 64M bytes, and integral floating point capability. Cramming the

1M-byte memory onto the board with the CPU required special packaging. Single inline packages (SIPs) mount four 64K x 1 RAMs in leadless chip carriers onto an alumina based substrate to reduce memory array area by 75%. Thus, a 256K-bit array requires just 22 pins and plugs directly into the printed circuit board. A second board brings system capacity to 4M bytes by supplying 3M bytes of memory expansion.

Implementing common I/O functions on another card, the system's multiple peripheral controller uses microprocessors to handle operations. This single board supplies communications, a data handling assist feature, loader storage unit, universal clock, parallel printer port, and self-test features. These functions typically occupy three chassis slots.

Together these three boards carry the power that occupies 13 boards in the low level 3210 configuration. Reductions such as these in board counts as well as in component counts guarantee increased system level reliability.

Gould packaged its single-slot 32-bit CPU with memory modules and I/O processor as the basis of its Concept 32/27 line. The CPU board supplies eight general purpose registers to programmers, and three registers are for use in indexing. Instruction lookahead allows fast execution of instructions. Memory management hardware allows the CPU to address 16M bytes of physical memory.

---

### *While minicomputers remain more versatile, micros in a box cost less than the minis they mean to replace.*

---

Interfacing direct to the SelBUS, integrated memory modules contain 256K bytes of RAM, memory controller, error correction, and refresh circuits. Read cycles can be overlapped on a single module, such that one can begin every 300 ns. When multiple modules are installed, writes can be initiated every 150 ns.

Data General's low end 32-bit ECLIPSE, the MV/4000, follows the same track but relies on a 2-board CPU and optional floating point. The design takes advantage of gate array logic and programmable array logic technology to build in features while holding the price line.

The sequential control unit (SCU) board handles system sequencing and control as well as memory refresh and error correction. Its microsequencer contains the control store and logic to control program flow. On the scratchpad unit (SPU) board are ALU, address translation unit, scratchpad, and I/O controller. These handle basic arithmetic functions, logical to physical address translation, and I/O implementation.

With these low end packages providing 32-bit power at cut rate prices, the plan is to stave off



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The MV/4000, Data General's low end 32-bit ECLIPSE, rated at 500K Whetstones/s, supports 8M bytes of main memory and accommodates 64 terminals. Housed in a 1-m high cabinet, the system's 2-board CPU takes advantage of gate array and programmable array logic technologies.

thrusts by microcomputers into that vulnerable and price sensitive area.

While the microcomputer remains more versatile, micros in a box, priced temptingly low, cost far less than the minis they are meant to replace. The current crop of micro-based minis still seem limited to attacks on low end minicomputers. This, however, promises to change as the first 32-bit microprocessors appear in products. Even the 32-bit minicomputers will feel the pinch.

### Micromainframes

A desktop computer, Hewlett-Packard's (Palo Alto, Calif) HP 9000 uses micro technology to squeeze key functions of a mainframe into a compact package. The 32-bit machine, complete with 1M byte of memory, contains only 98 chips. Compare this to the 5000 chips that make up most of the current crop of superminis.

The CPU uses a 32-bit address/data bus with pipelined data transfers at 36M bytes/s. It has a 55-ns cycle time and performs 1M instructions/s. The unit directly addresses 500M bytes of memory. Internal memory up to 2.5M bytes is formed from 128K-bit RAMs in increments of 256K bytes. Pipelining yields 165-ns access with a 110-ns cycle time. Memory controller chips supply memory mapping, error detection/correction logic, and memory "healing." When a single-bit error is detected, the controller both corrects the bit in error and copies the word to a special healer location. Further accesses go directly to the healer location.

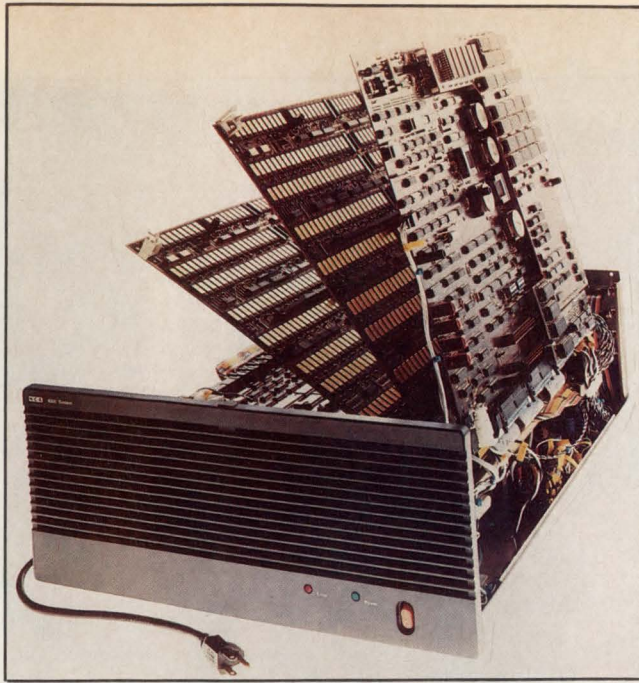
Based on a 4-chip VLSI set, NCR's (Dayton, Ohio) 9300 puts a midrange mainframe in a 2-cu ft, 50-lb box. Measuring 7½" high, 17½" wide, and 25¾" deep, the system uses 10% of the power of an equivalent system. In the box with the 32-bit externally microprogrammable CPU reside up to 4M bytes of memory, and a communication processor multiplexer.

Providing 160 microinstructions, the central processor chip uses six internal data paths and two external paths—processor memory bus and instruction storage unit—for fast memory to memory operations. Its 3-stage pipeline yields a microinstruction execution time of 150 ns. Scratchpad cache has a fetch cycle of 300 ns and real memory uses a 450-ns fetch cycle.

As interface between CPU and main storage, the address translator, with 128M-byte virtual address capability, performs address translation using a 16-entry associative memory. These content addressable address translation registers use a 25-bit page descriptor and result in 600-ns virtual memory fetch cycle time.



Based on a VLSI 5-chip set, the processor in the HP 9000 packs in key functions of a 32-bit mainframe computer. Slightly larger than a personal computer, the desktop workstation uses a multiple processor architecture to offer three levels of performance by plugging in up to three CPU boards.



VLSI technology allows the 32-bit power of NCR's 9300 to be packed in a 2-cu ft, 50-lb cabinet measuring 7½" high, 17½" wide, and 25¾" long. The four circuit boards (extended for the photo) lie flat in the cabinet like pages in a book. The processor board (right) houses the 32-bit VLSI chip set, the second and third boards each hold 2M bytes of memory, and the fourth board (left) takes care of data communications.

Using multiple parallel processors in a shared logic architecture, Convergent Technology's (Santa Clara, Calif) MegaFrame also falls in this category. Consisting of three main processing elements, MegaFrame uses MC68010s for application processing, and Intel 186s for file, terminal, and cluster processors. Each application processor supports 2-level virtual memory paging with memory management and provides 512K to 4M bytes of dual-ported RAM. The 11M-byte/s asynchronous backplane lets all processors operate in parallel. Processors communicate as if accessing memory, rather than by interrupting an external processor.

File processors execute the Unix file system, while the application processor performs applications. Cluster and terminal processors, like the file processor, contain 8-MHz Intel 186 and 256K to 768K RAM. Unix terminal handling tasks are taken on by multiple independent frontend processors instead of the main processor. This offloads the main processor and allows device, character, line, or page to be addressed without interrupting the main processor.

This tack of distributing function between processors also serves in Masscomp's (Littleton, Mass) MC-500. The CPU in this machine encompasses two MC68000s. A 4K-byte instruction and data cache works with these processors. Performance is optimized by using a 1024-entry address translation buffer to store translated virtual to

physical memory addresses. Memory management processing, as well as cache misses, are handled by a second MC68000 processor to ensure efficient operations.

A separate data acquisition processor, formed of bipolar bit slices, handles realtime I/O. Executing an instruction every 125-ns, this processor includes 1024 (40-bit) words of control store, 256 24-bit temporary registers, two 16-element FIFOs, and one 64-element FIFO.

Only time will tell what the next generation of 32-bit processors will bring. The potential for high end machines using the high speed, high density GaAs devices beginning to emerge seems virtually limitless. The future indeed is dazzling.

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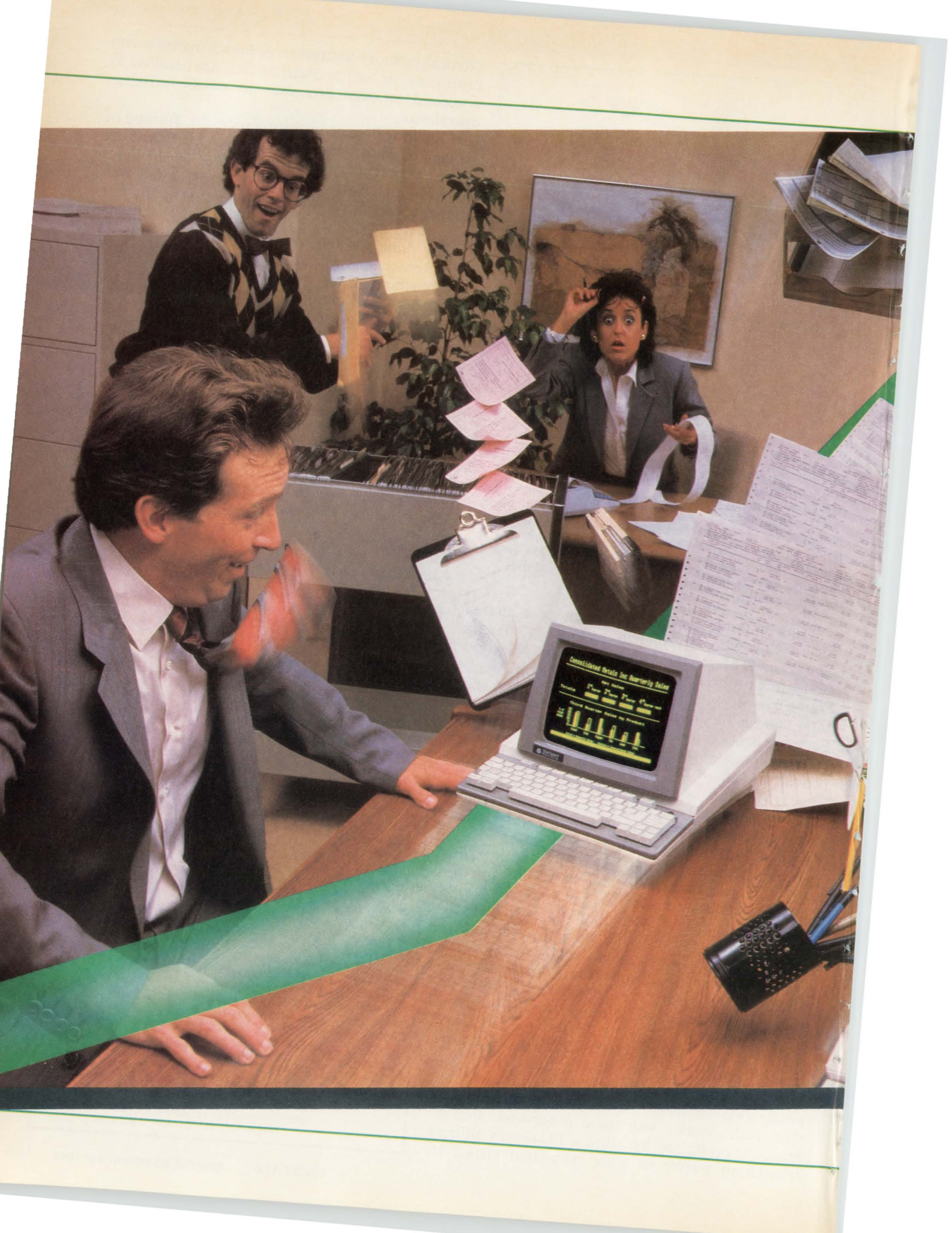
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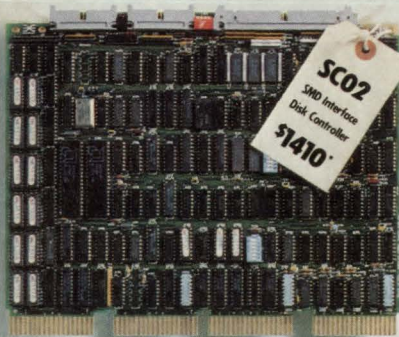
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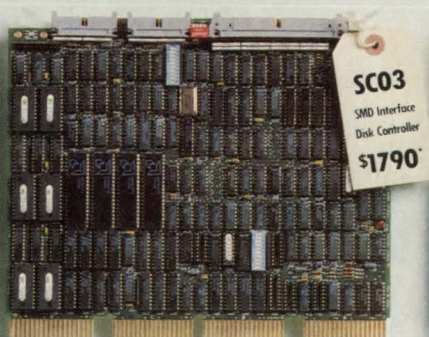
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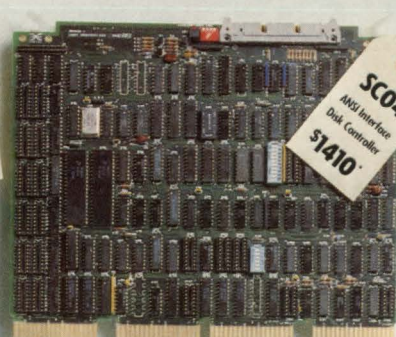
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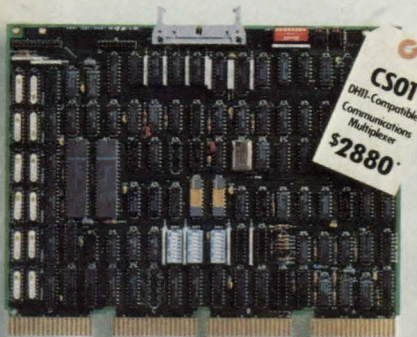
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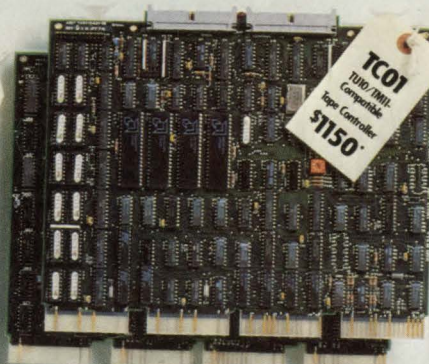
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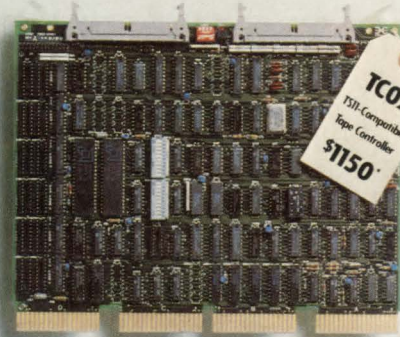


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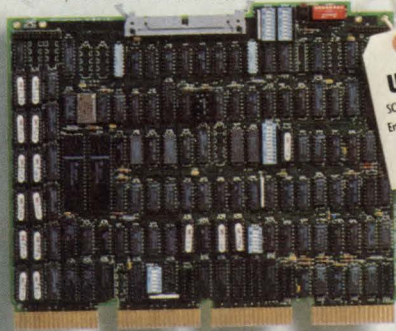
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# APPLYING RISC THEORY TO A LARGE COMPUTER

**Melding theoretical Reduced Instruction Set Computer concepts—large register stack and overlapped register windows—with I/O techniques from traditional systems forms a highly effective minicomputer architecture.**

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**by Robert Ragan-Kelley and  
Roy Clark**

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Recent research into Reduced Instruction Set Computer (RISC) theory, particularly at the University of California at Berkeley, raises some important issues regarding the support of high level languages in computer architecture. Although the name implies emphasis on the instruction set alone, one of the most significant results of this research is the concept of large register stacks organized as overlapping register sets.

The experimental RISC I processor developed at Berkeley showed improved high level language performance and also minimized time-consuming memory accesses by allowing parameter passing through “windows” in the overlapping register sets. Aspects of this important RISC concept form the basis for the proprietary instruction set and register-intensive architecture of the Pyramid 90x.

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*Roy Clark is CPU project manager at Pyramid Technology Corp. He holds a BSEE from Purdue University.*

This machine integrates architectural elements garnered from the Berkeley research that conform with the overall design goal—to supply dedicated support for the Unix operating system and high level languages, such as C and Pascal.

In addition to this overall goal, other, more specific design criteria included an instruction set that would be suitable for a wide range of implementations: uniform code generation from high level language compilers, and transparent execution of high level functions in software, firmware, or hardware within the same system. High level functions would be included without increasing the system's complexity or decreasing its base performance. The particular processor implementation of an installed system would not limit performance level and functionality.

## **Meeting system goals**

To attain these goals, the general purpose architecture provides high performance for programs written in high level languages, a “simple” base processor, and hardware extendability. The 32-bit, virtual memory system supplies up to 16M bytes of main memory, supports up to 128 users, and has 528 registers for high level language optimization. The proprietary central processing unit (CPU) has a 125-ns cycle time and is implemented in fast Schottky TTL. Also provided are a 32M-byte/s XTEND bus; sophisticated virtual, physical, and cache memory management; and intelligent input/output (I/O) processors.

With these criteria in mind, designers studied several contemporary architectures in addition to the Berkeley RISC I processor. These included traditional designs such as Digital Equipment Corp's VAX-11/780, Intel Corp's 432, and Motorola's MC68000. More experimental designs such as IBM's 801 processor were also considered.

### RISC versus CISC

RISC theory is often compared with Complex Instruction Set Computers (CISCs), which have dominated computer design for the past decade. Both types of computer design seek to maximize performance and accommodate programmer needs. However, there are some philosophical differences between the two approaches.

CISC machines typically have a large number of specialized instructions, many addressing modes, and pipelining and cacheing features. Emphasis is on embedding system functionality in hardware and firmware. The instruction set of a CISC machine is raised to the semantic level of the desired programming language. This type of rich, orthogonal instruction set seeks to simplify the compiler writer's tasks by providing statements similar to those found in high level languages. For example, a CISC instruction set would include case and call. A CISC compiler considers the many cases presented by the instruction set and performs a large number of memory transfers in executing an instruction. Thus, several machine cycles are usually required.

RISC theory, as exemplified in the RISC I processor developed at the University of California at Berkeley, is register intensive: all operations except memory loads and stores are register-to-register. Overlapped register sets minimize data movement in procedure calls and allow parameter passing. There are fewer, simpler instructions in a RISC design, instruction format is fixed, and little or no firmware is used. RISC design is intended to make compiler writing easier by simplifying the number of different cases to be considered. A RISC compiler quickly decodes and executes many short, simple instructions instead of searching for a single, matching complex instruction, typically in one machine cycle. RISC instruction sets are designed to include only the most often used functions, such as procedure calls. Overlapping register windows are used to minimize memory loads and stores. The emphasis in RISC machines is on software and overlapping register sets.

In implementing the Pyramid 90x supermini, designers drew on both theories, and added some ideas of their own. CISC attributes were most useful in providing traditional large system features such as floating point and heavy I/O management in the Pyramid 90x. The RISC overlapping register set concept enhanced the Pyramid 90x's performance, and facilitated high level language support.

Traditionally, machines designed with high level language support as an objective have either relied on additional hardware to supply speed, or have attempted to bring the computer's instruction set closer to the semantic level of the particular language. In considering this approach, designers examined the possibilities of a directly executable

language (DEL) architecture. Drawbacks that eventually disqualified DEL type designs included a tendency to be too language specific, and to be optimized for object-code size or source to object-code translation, rather than for actual hardware implementation and execution of "real" programs. A multilingual DEL approach, in which the processor is microprogrammed to execute idealized machines for diverse language environments, came closer to the objectives. However, this architecture requires a large amount of interpretive support in the instruction-unit hardware.

A highly orthogonal instruction set with powerful addressing modes, intended to support a wide intersection of languages such as Pascal, C, Fortran, and Cobol, presented yet another possibility. However, high level language compilers that generate efficient code are difficult to develop for this type of machine, since the large number of cases and combinations prohibits simple translation. In addition, many combinations that are desirable from a code size standpoint are costly to execute. As a result, a huge amount of compiler decision-making is required to handle the subtle performance implications of many instruction and addressing modes.

### RISC fills objectives

Problems inherent to these approaches led the designers to examine the more experimental RISC designs. They attempted to identify RISC machine features that would enhance system objectives while blending with traditional features required of large machines, such as floating point, heavy I/O activity, and computation-intensive processing. Principal RISC performance advantages relate to the use of high level languages. RISC design optimizes computer architecture for high level languages by focusing on extensive register operations that reduce the need for main memory access, and by including simple, carefully chosen instruction sets that facilitate compiler optimization.

Perhaps the purest example of an experimental RISC implementation is the RISC I processor. RISC I research was oriented to the following constraints to maximize performance: to make all the instructions the same size, execute one instruction per cycle, access memory only with load and store instructions, and use register operations for all logical functions. The processor uses no microcode to fulfill these requirements; it relies instead on logic circuitry. The register stack and the overlapping register window organization further reduce the frequency of load and store instructions. Two other contributing features are a fixed instruction format, and an instruction set containing no primitives that require multiple cycles (such as floating point). The principle design advantages of the implementation are speed,



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### Typical C Program Statistics (Traditional Computers)\*

Statements	Usage Frequency	Machine Instruction	Memory References
Call/return, including setup, save, restore	12%	33%	45%
Loops	3%	32%	26%
Assignment	38%	13%	15%
If	43%	21%	13%
Other	4%	1%	1%
	100%	100%	100%

\*Source: "VLSI RISC" D. Patterson and C. Sequin, *IEEE Computer*, Sept 1982.

simplicity, and the flexibility to adapt to emerging technology without extensive hardware redesign.

The most interesting aspect of the Berkeley study was the processor's high level language performance compared with that of VAX-11/780, MC68000, and Z8002 processors. RISC I outperformed these processors in tests that compared program execution speed in high level languages with assembly language speed for the same benchmarks, using the same compiler technology.

Examining these results and the RISC I architecture convinced designers that the large register stack and overlapping register window scheme contributed significantly to the processor's superior high level language support. These concepts are implemented in the Pyramid 90x's design.

#### Reducing loads and stores

The large register stack and overlapping register windows improve high level language support in a large machine in several ways. Tests demonstrate that register-to-register operations are two to four times faster than cache memory operations, and are 8 to 10 times faster than main memory operations. The large number of registers produces efficient high level language compilers by reducing the number of memory references and register allocation decisions that must be made. Optimizing compilers, combined with simpler procedure calls and the reduced execution time for load and store operations, significantly increase the machine's overall performance. Only 15% to 25% of the machine's executed instructions require memory loads and stores. This compares with 50% to 70% for conventional architectures.

In a C language procedure call/return overhead comparison, where two parameters are passed and three registers are saved as necessary, the register window implementation requires one-tenth the execution time of a traditional computer. The number of memory accesses made by the Pyramid implementation are an order of magnitude less than the other implementations.

Consideration of the high level language statement frequencies of Algol-like languages such as C and

Pascal led to an efficient architectural approach. In addition, Fortran, Cobol, Lisp, and APL were examined to determine types and frequency of operations and accesses; of arithmetic operations by classification; and of statement types such as call/return, assignment, if, goto, case, and loop. These and other studies revealed several major trends which point to register-intensive instruction sets. The results show that most operands are local scalar items, and that the most frequent statements are "if" statements and assignments. Procedure calls and returns, however, account for the largest part of the program execution time (see the Table).

To maximize these operations, the Pyramid design provides only one type of call and one type of return statement. This simplifies the integration of code developed in different high level language compilers on the same machine. The design accommodates nested procedure calls with 512 registers, each with 32 bits (4 bytes) of space. These are implemented in stack form with 16 levels of 32 registers each, plus 16 global registers for a total of 528 registers (Fig 1).

From a programmer's point of view, the architecture appears as a 64-register machine, including 16 global registers, 16 parameter registers, 16 local registers, and 16 temporary registers. The global registers include the program counter, a pointer to the top of the data stack, and a pointer to the base of the current stack frame in the data stack. The 16

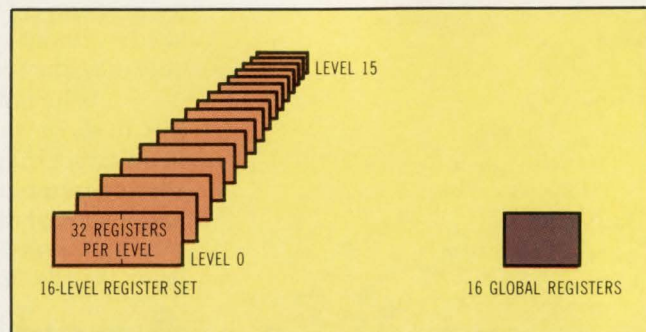
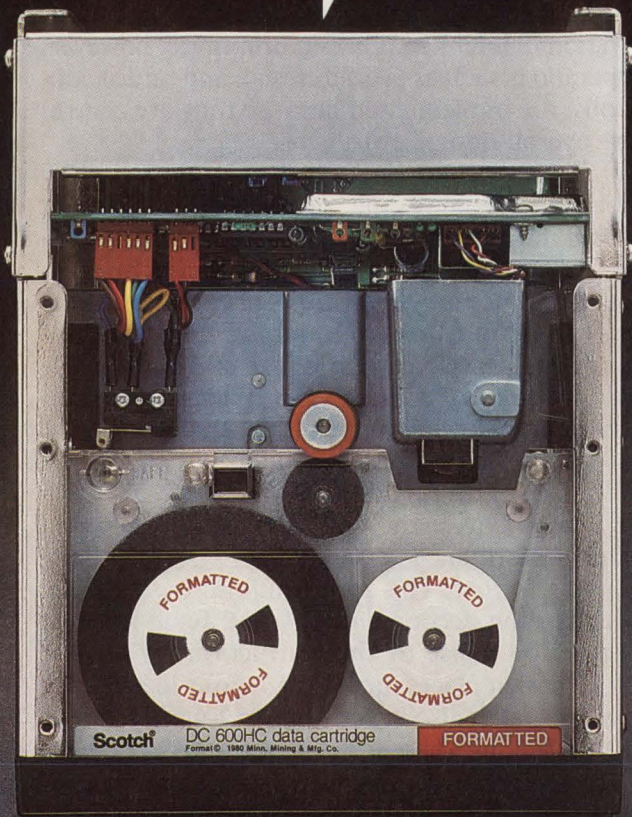
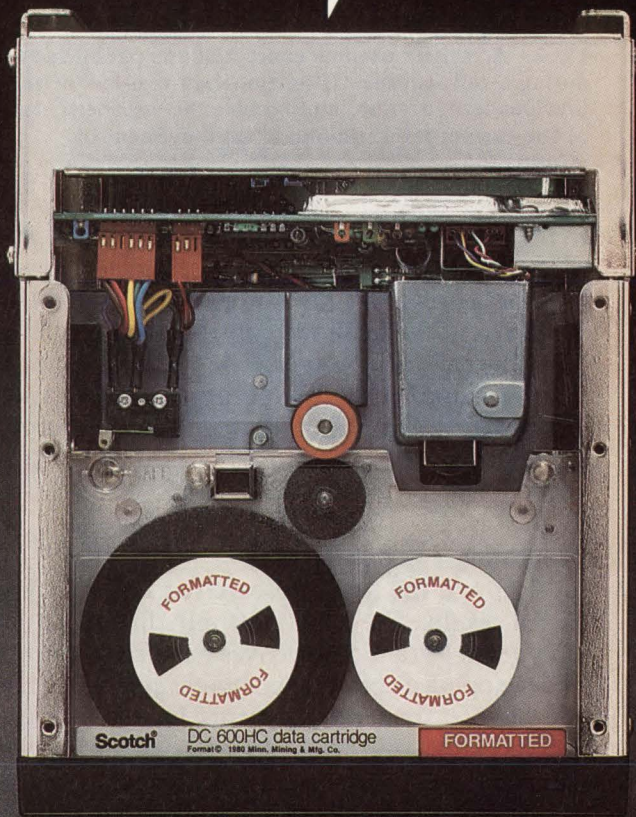


Fig 1 The Pyramid 90x register stack implementation supports nested procedure calls up to 15 levels without having to access memory to store parameters and return values.

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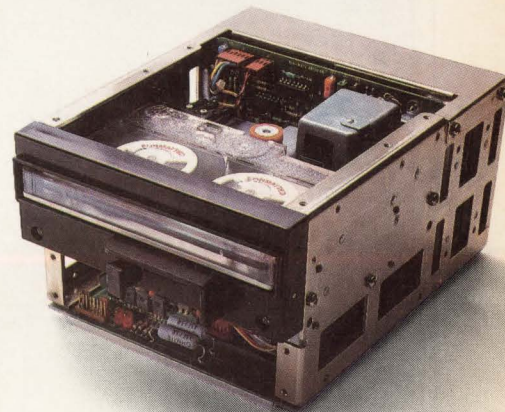
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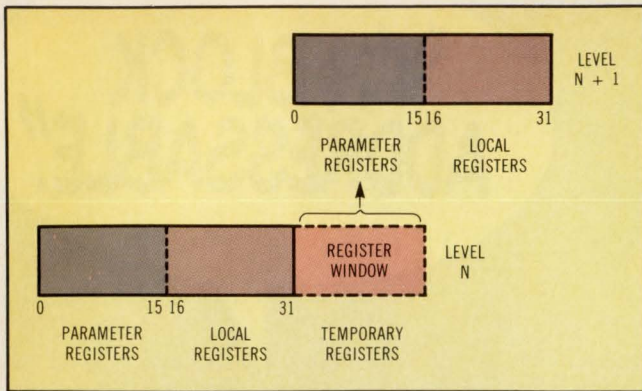
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**Fig 2** A register window concept allows parameter passing during a call sequence. The temporary registers of the previous level overlap, and become the parameter registers of the current level without actual movement of information.

parameter registers are mapped through a window to the previous level where they were temporary registers (Fig 2). Additionally, the parameter, local, and temporary registers are mapped to a control stack. The current frame in the control stack is referenced by a control stack pointer. The current frame of registers (excluding the temporary registers) and previous frames are also addressable as memory. This allows their addresses to be passed to subsequent procedures.

### Integrating extended functions

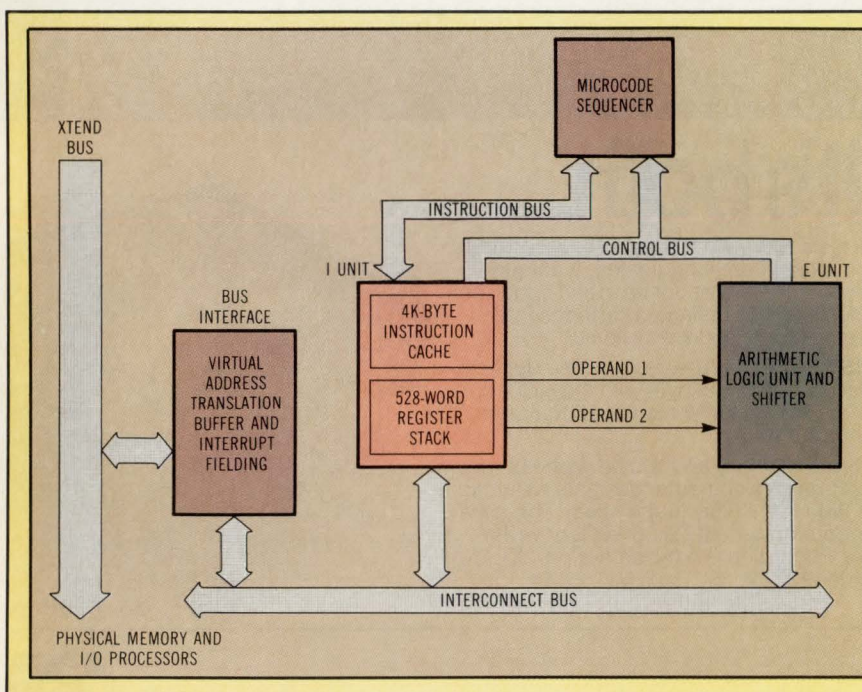
Although the RISC I research at Berkeley yielded useful results, the goals not only differed substantially from Pyramid objectives but also stopped short of developing a complete computer system. Pyramid's complete system requirements included operating system support, I/O support, virtual memory, floating point, and, in general, a more extensive set

of functions. The 90x accomplishes this by integrating RISC aspects, such as the large register stacks and overlapped register window scheme, with more traditional large computer features and some proprietary features.

As a general rule, the design implements a workable class of primitive functions, and provides for future expansion of that class. Specific problems such as stacks, data structure manipulation, operating system functions, and language implementation were avoided. This not only retains the simple instruction set, but leaves performance and later innovation uninhibited. Certain primitives, however, for operations such as procedure call and return conventions, are implemented because they are central to the overall design objectives.

Hardware execution is controlled by firmware, or microcode. Dividing the processor by using a detached instruction fetch and execution approach allows execution capability to be extended through selective addition of hardware. This approach also allows certain functions to be implemented in firmware for entry level versions of the machine. These functions can later be upgraded with hardware accelerators to provide floating point, decimal arithmetic, trigonometric functions, hashing, or any other desired multicycle functions.

To a large extent, the RISC I processor's simplicity and performance result from its simple fixed instruction format. This format allows for a simple, fast instruction decode and operand fetch prior to the execution phase of the instruction. While the Pyramid design places most instructions in a similar 1-word format, it also includes some 2-word formats for 32-bit literals. These serve as operands or address displacements for data moves or control instructions.



**Fig 3** The I- and E-units within the CPU are interconnected through two 32-bit operand buses. A microsequencer uses a control to control bus execution of both I- and E-units.

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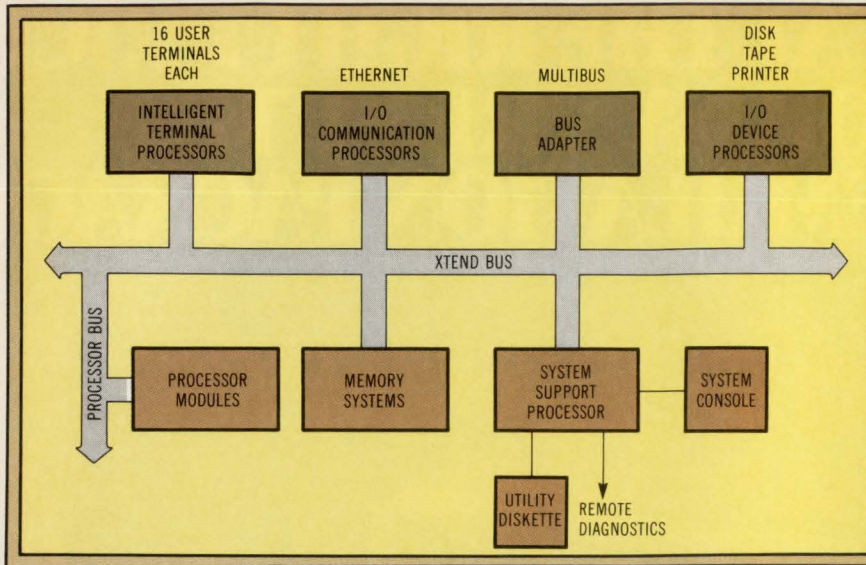
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**Fig 4** In the Pyramid 90x block diagram, the message-based XTEND bus and intelligent I/O processors offload the main CPU and allow for future expansion. The RISC register structure combines with traditional large system features to form a high performance superminicomputer.

The commitment to high level language support and performance is reflected by the fact that most instructions are register-to-register operations. However, certain other classes have been introduced to specify literal operands (6-bit signed or 32-bit immediate), as well as certain address computations (register direct, base index, base displacement, or displacement index). On the other hand, such artifacts as indirect pointers in memory, auto-increment/decrement, and base-displacement-index are not included in the addressing modes.

In a "pure" RISC design, heavy use of a function that does not occur in the instruction set will severely degrade performance. This potential problem is averted by providing for specialized microcoded instructions. Optional hardware logic controlled by microcode can be included to supply high performance in specific applications.

### Melding RISC and CISC

The basic processor contains an instruction fetch unit (I-unit), a firmware sequencer, and an execution unit (E-unit), as shown in Fig 3. These are all interconnected through a series of buses, including two 32-bit operand buses, one 32-bit result bus, and control buses that are used by the sequencer to control execution and allow overlapping of various CPU processes. The I-unit contains a 4k-byte instruction cache, and up to 16 frames of registers for the control stack. It operates with a simple 3-stage pipeline: instruction fetch, operand fetch, and execute.

The basic E-unit contains a simple arithmetic logic unit and barrel shifter. Microcode within the base processor handles floating point and other instructions for which there is currently no special hardware. Hardware accelerators, including floating point, may be incorporated into the system by attaching them to the processor bus, and modifying the firmware to invoke the hardware function where appropriate. The virtual memory translation buffer is implemented at the interface between the

processor and the system bus. This same interface is upgradable with a general data cache control section, for modular inclusion of data cache.

To manage the demands placed on a larger system, several features enhance efficient memory use and act to offload the CPU. In the 3-tiered virtual, physical, and cache memory system, byte-addressable virtual memory allows each Unix process to use up to 4G bytes of address space. Physical memory can be configured with from 1M to 8M bytes using 1M- or 2M-byte memory modules with error correction code.

The message-based XTEND bus and intelligent I/O processors (IOPs) offload the main CPU to increase system efficiency and speed. The XTEND bus also allows for future hardware expansion by giving additional symmetric or asymmetric CPUs the ability to share memory and peripherals in a tightly coupled fashion. The IOPs use bit-slice or microprocessors for terminal handling; disk, tape, and printer controllers; high speed communications; and networking. The IOPs break the I/O bottleneck found in earlier large Unix-based systems, and preserve system response as users are added (Fig 4).

Integrating the execution speed and high level language support provided by a RISC register structure with traditional large system features such as operating system and I/O support, achieves the stated design objectives. Combining the best performance and support features of newer RISC technology with the traditional, large system technology results in a better machine than a narrower design approach would have allowed.

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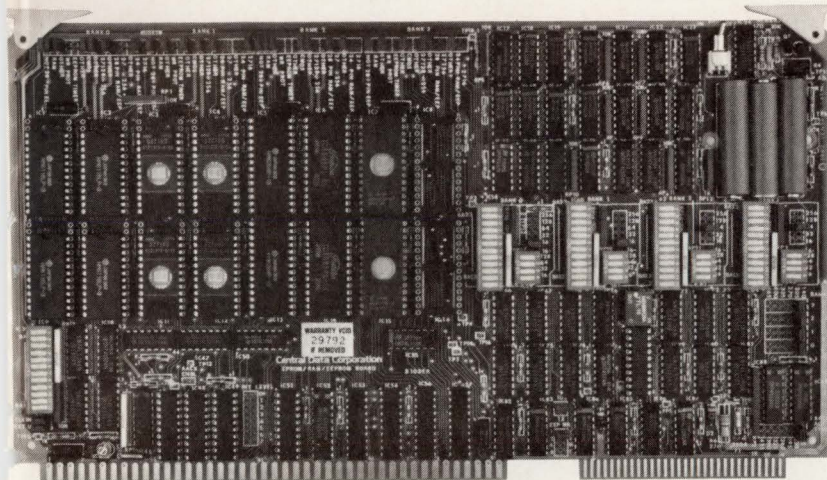
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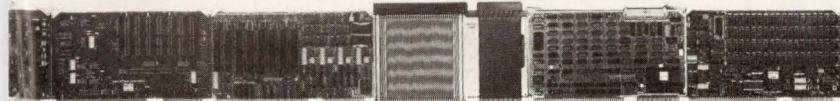
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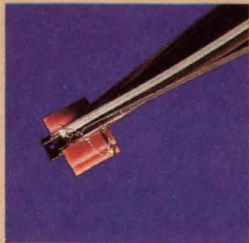


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#### Winchester Cleanliness

The Arapahoe 7110 does not compromise Winchester cleanliness and reliability just because it has a removable disk. When the cartridge is removed, the fixed-disk chamber is sealed by a proprietary active hub seal



around the spindle. With the cartridge installed, only the cartridge interior is part of the clean air system. The HDA chamber is purged to a Class 50 environment within 45 seconds of power-up. Air quality within the positively-pressurized plenum chamber is maintained by a recirculating air filter that provides 20 times the scrubbing capacity of other fixed or removable drives.

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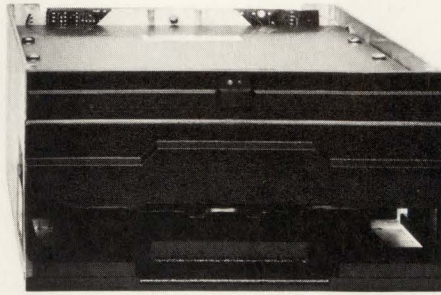


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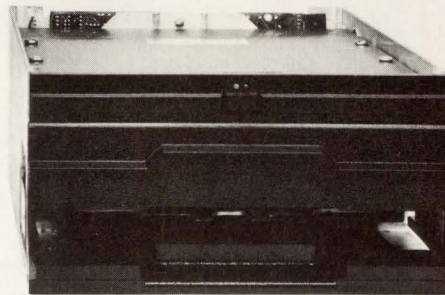
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CIRCLE 109

# FRONT.



# BACK.



## **Any Way You Look At It, Superior Storage Solutions.**

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## **Front View: High Reliability Primary Mass Storage.**

There are several powerful reasons to seriously consider the Alpha 10 as a primary mass storage device. First of all, each cartridge stores 10 Mbytes of data—easily matching capacity with today's Winchester.

But just as important, the Alpha 10 matches the Winchesters in reliability, thanks to several IOMEGA innovations in flexible disk and removable cartridge technology. As for versatility, the unique cartridge format of the Alpha 10 speaks for itself—a straightforward approach to library management and data interchange.

## **Back View: High Versatility Back-Up And Archival Storage.**

The Alpha 10's advantages for back-up and archival storage are just as impressive. For instance, a 10 Mbyte Winchester file can be dumped onto a single Alpha 10 cartridge in literally minutes, not the usual hours. You can look forward to a new standard of reliability that is integral to our design. And, because our cartridges are the most inexpensive on the market today, archival storage doesn't cost you an arm and a leg.

## **Overview: The Careful Evolution, And Immediate Availability, Of A Drive Design Revolution.**

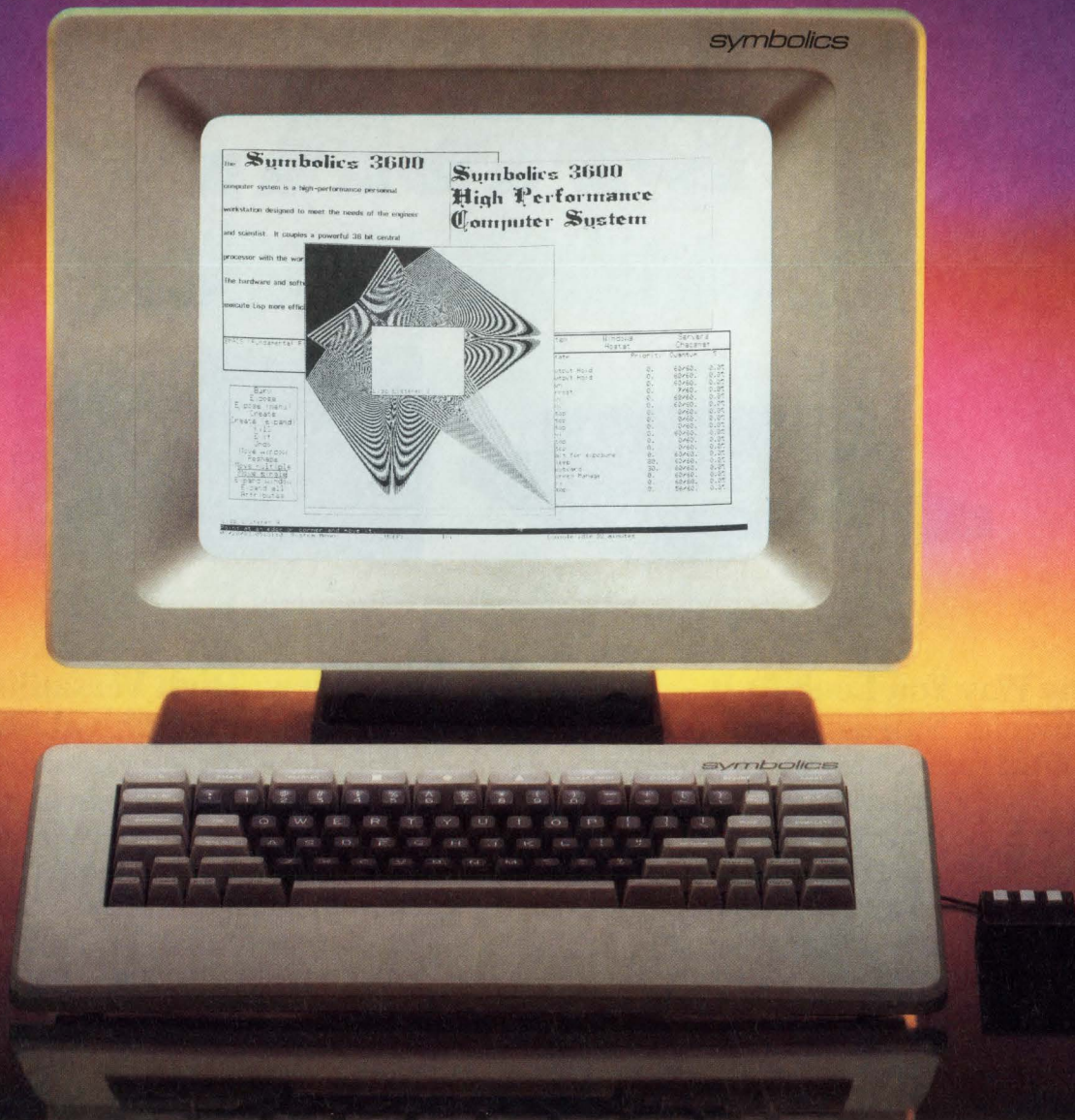
Any way you look at it, the Alpha 10 is a breakthrough in data storage device design. Actually, it's a series of breakthroughs, including non-contact head-to-disk interface, high linear bit densities, a run-length limited code that compresses the data stream from the host, and closed servo control of the head positioning, all to achieve the economy and versatility of flexible disks with the capacity and reliability of hard disks.

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# LISP MACHINES COME OUT OF THE LAB

**No longer restricted to the research lab, artificial intelligence is becoming increasingly attractive to commercial users thanks to computer architectures designed to support the Lisp language.**

---

**by Mache Creeger**

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Artificial intelligence, defined as the science of enabling machines to reason, make judgments, and even learn, is often seen as a field whose practical benefits will be realized only at some future date. This is not entirely true. Artificial intelligence researchers have already contributed to the development of such techniques as timesharing, networking, and window systems—a part of the commercial computing world. However, a powerful software tool developed by the artificial intelligence community, the Lisp language, is just beginning to make an impact outside of the research labs.

The Lisp language deals with the complex and unpredictable data characteristic of the artificial intelligence (AI) field. It permits large, powerful programs that traditional programming techniques cannot handle to be written, tested, and modified. However, traditional computers (such as Digital Equipment Corp's system10 or VAX, and similar machines), cannot support Lisp so that it can become an efficient tool for commercial use. As a result, the power and productivity of the language

---

*Mache Creeger is director of marketing at LISP Machine Inc, 3916 S Sepulveda Blvd, Culver City, CA 90230, where he is responsible for sales and marketing of the company's Lambda machine. Mr Creeger holds a BS and MS from the University of Maryland.*

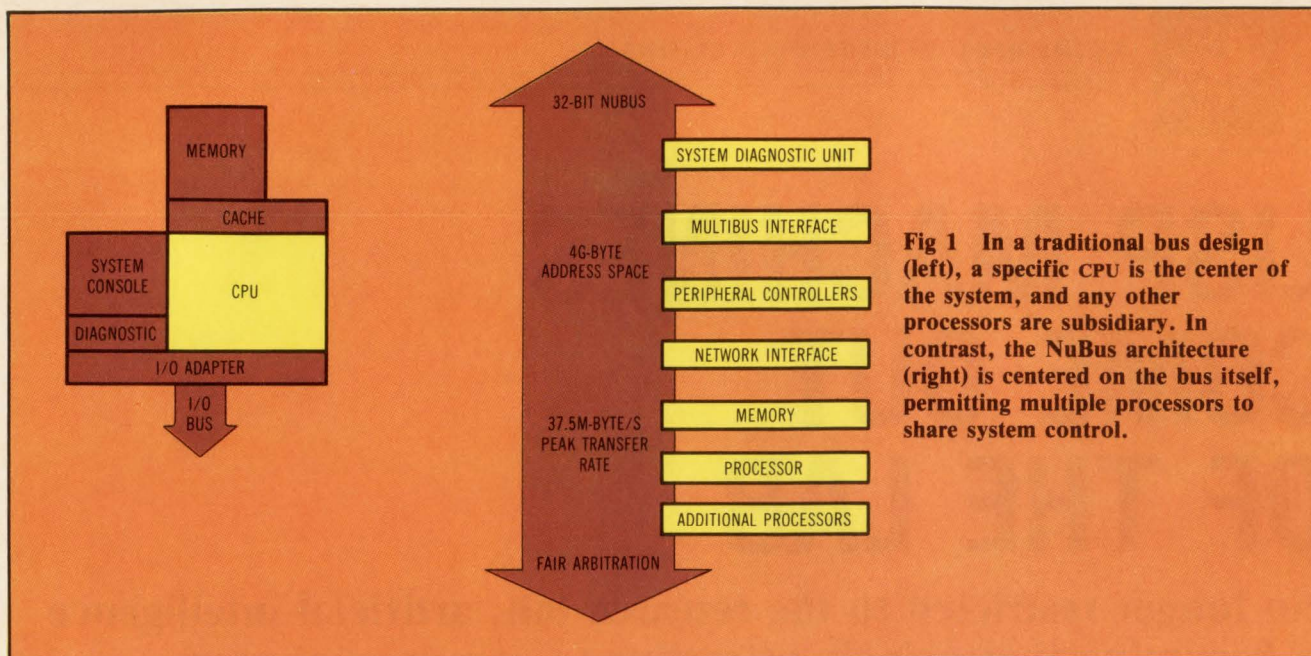
have remained in the research lab, where functionality, rather than speed, is the major consideration.

An efficient Lisp implementation requires an architecture optimized for the structure of the language, as well as very high storage capacity. In addition, Lisp must be integrated with other computing environments to eliminate the need for an all-at-once changeover from present software and/or hardware. Such a machine offers a programming environment that provides substantial productivity increases for the development of a range of software systems, as well as an evolutionary means of bringing "intelligence" to existing computer systems.

## **Lisp and the commercial world**

While this potential should make it attractive to software developers and system integrators in the commercial world, the lack of appropriate hardware for the language has kept it in the research labs. Before the development of the first Lisp machines at the Massachusetts Institute of Technology (MIT) in the 1970s, Lisp implementations ran on mainframes. Since the architecture of these machines was optimized for numeric languages such as Fortran, much of the Lisp environment was in software, thereby imposing substantial overhead on program execution. The applicative and recursive nature of Lisp requires an environment that efficiently supports stack computations and function calling.

In addition, Lisp's memory requirements exceeded even the capacities of these large



**Fig 1** In a traditional bus design (left), a specific CPU is the center of the system, and any other processors are subsidiary. In contrast, the NuBus architecture (right) is centered on the bus itself, permitting multiple processors to share system control.

computers. Frequent stops for garbage collection made execution slow. Methods used to implement data-typing imposed another handicap. Lisp is a weakly typed language, meaning that functions can deal with a number of different data types (eg, fixed and floating point numbers) through a process called coercion, where a function recognizes the kind of data object it is dealing with and reacts accordingly. Traditional memory organizations require this process to be handled in a number of inefficient ways. Devoting fixed areas of memory to specified types causes memory fragmentation; other devices required extensive software overhead. Other problems were the language's poor arithmetic capabilities, since overcome by better compilers and hardware support, and its "stand-alone" nature. Because it was developed for use as a research tool by individuals or small groups, it did not integrate well into more traditional multi-user computing environments.

### Lisp machine design

To illustrate how Lisp machine design overcomes these handicaps, consider the Lambda Machine from LISP Machine Inc. It is a lineal descendant of the original MIT Lisp machine, the CONS, which required mainframe support to operate. This machine was superseded by the CADR, which was later brought to the marketplace by LISP Machine Inc. The CADR was a personal, networked computer for programmers developing large, complex software systems. Drawing heavily on design experience gained from the CADR, the Lambda adds Lisp-oriented enhancements to the advanced high performance NuBus, also developed at MIT. Combining the Lambda processor with the NuBus architecture produces a modular, expandable Lisp machine with multiprocessor

capabilities. The Lambda offers an integral Multibus, Ethernet-II networking, and the Lisp Machine Lisp/Zeta Lisp operating environment.

NuBus's device-independent architecture, originally developed at MIT's Laboratory for Computer Science and now supported by Texas Instruments, centers on a 32-bit bus with a 37.5M-byte/s peak transfer rate. Important aspects are its ability to support multiple processors and the architectural flexibility furnished by the system diagnostic unit (SDU). Both of these distinguish it from traditional architectures (Fig 1).

Traditional bus architectures center on a single processor, with major subsystems arrayed around a specific central processing unit (CPU). In contrast, the NuBus is a communication-centered design that allows rapid interchange of data between a variety of devices within a 4G-byte address space. Input/output (I/O), interrupt, and memory signals are initiated uniformly over the bus, and transactions are based on a "master/slave" concept: any given device may control the bus and address another device as a slave for that transaction. A simple handshake protocol used between master and slave enables modules with different speeds to communicate. This arrangement allows a variety of processor combinations to be used.

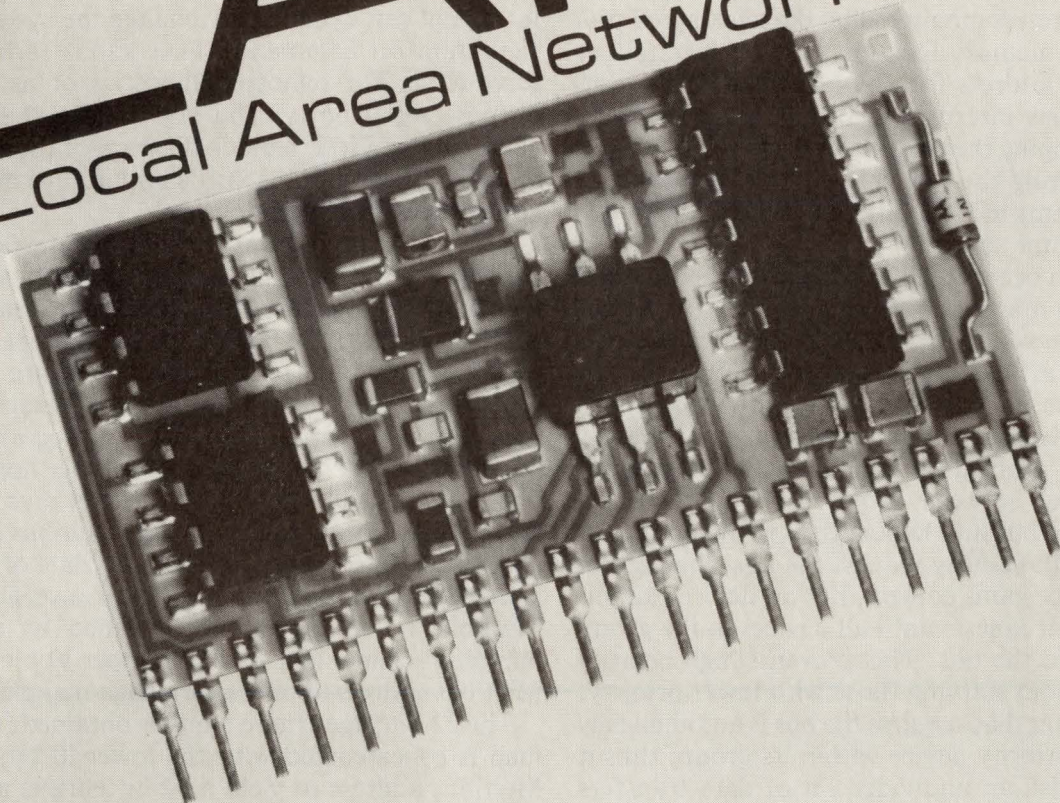
NuBus architecture handles five functional classes of signals. Four card-slot identification signals assign a unique physical location to each of 16 boards, so that any system module can occupy any board location; no dual-inline package switches, jumpers, or special backplane wiring are necessary. Six control signals—CLOCK, RESET, START, and ACKNOWLEDGE for data transfers, and two transfer mode (TM) signals for type of transfer—perform all control functions. Modes include 8-, 16-, and 32-bit (full-word) transfers as well as block transfers of up to

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16 words. Thirty-two signals carry a 32-bit address at the beginning of each clock cycle, and 32 bits of data in the remainder of each cycle. Five signals control bus arbitration, and two indicate system parity and parity validity.

### Multiprocessor operations

Two elements of this high speed bus design are particularly important for supporting multiprocessor operations: the memory mapped interrupt scheme, and the distributed bus arbitration logic that governs the master/slave relationships among devices. There are no interrupt lines on the NuBus. Instead, interrupts are accomplished by write transactions into memory addresses monitored by the interrupted processor. Any memory location may be specified as an interrupt address for any processor. This technique specifies interrupt priorities in software by memory mapping the priority level of each interrupt, thus eliminating the difficulties otherwise encountered in systems using multiple processors with differing interrupt schemes.

Arbitration occurs each time control is transferred between bus masters, and is independent of data transfers. The winner of the arbitration controls the bus until an arbitration is won by another device, but control is not transferred until the losing bus master completes any current data transfer. The distributed bus arbitration logic provides fair bandwidth sharing between processors by organizing devices on the bus into logical groups. When several devices simultaneously request the bus, the highest priority device gains control, but no device can initiate new bus requests until all devices in the group have acquired the bus. This prevents high priority processors from starving those with lower priority.

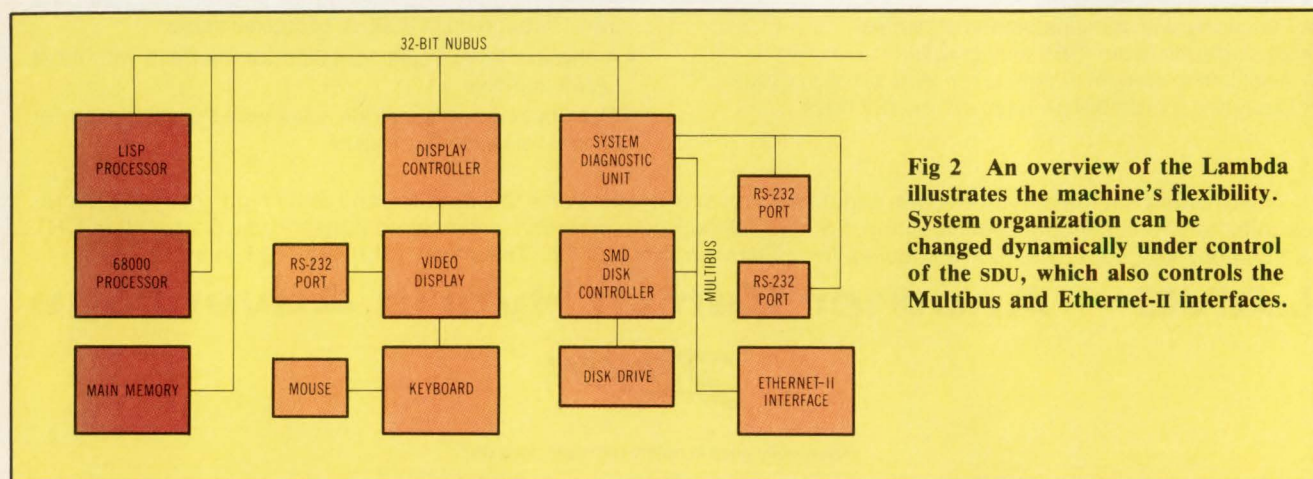
A bus master that acquires the bus is automatically the highest priority device within its group; thus it can accomplish an undivided set of data transfers by continually arbitrating for, and winning, the bus. If no other processor requests the bus, the current bus master may continually initiate data transfers without re-arbitrating for the bus each time. This

scheme speeds up processing by relieving a bus master of unnecessary arbitration overhead.

The NuBus's modularity and device independence comes from the SDU. This 8088-based board serves both as an architectural supervisor and as a smart diagnostic front end. Upon power-up, the SDU verifies bus integrity, identifies boards in the system from the contents of a small read only memory (ROM) on each board, and configures the system accordingly. It tests each board, signals the presence of any defective modules, and then boots the system. The SDU stores system configuration information in a nonvolatile battery-backed complementary metal oxide semiconductor random access memory (CMOS RAM) and can dynamically change the system configuration on command. Two RS-232 serial ports serve either for remote diagnostics or as general purpose serial ports. The SDU is also the system clock source. Fig 2, a block diagram of the Lambda machine, illustrates the SDU's importance in system control and configuration.

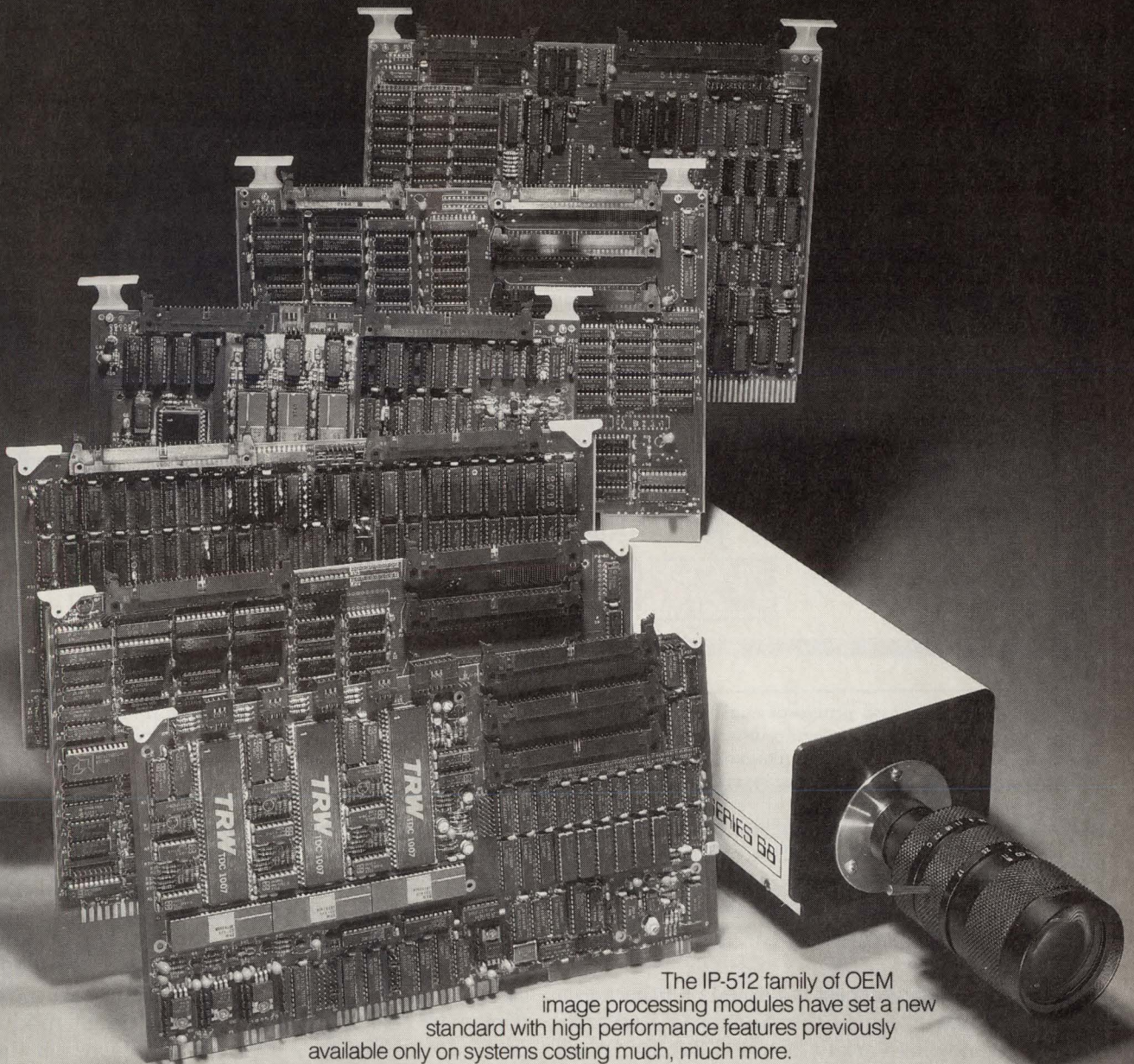
The SDU also serves as the NuBus interface with the Multibus. The Multibus allows the Lambda to interface with numerous peripherals and board-level products. The two buses operate independently except during bus conversions, which are accomplished through a hardware mapping scheme that requires no participation by the 8088 processor. The Multibus's entire 1M-byte address space appears as one continuous block in the 4G-byte NuBus address space. Conversion from NuBus to Multibus is transparent; a NuBus processor can access data or execute a program from Multibus memory. Conversion from Multibus to NuBus is accomplished by a page-mapping scheme that uses the upper 10 bits of the Multibus address to reference a page-mapping table.

The 22-bit page-frame number obtained from the map is concatenated with the lower 10 bits of the Multibus address to yield a 32-bit NuBus address. Interrupts originating in the Multibus are mapped into NuBus interrupt addresses by the 8088 processor; interrupts from NuBus to Multibus are written by the NuBus to an addressable latch on the



**Fig 2** An overview of the Lambda illustrates the machine's flexibility. System organization can be changed dynamically under control of the SDU, which also controls the Multibus and Ethernet-II interfaces.

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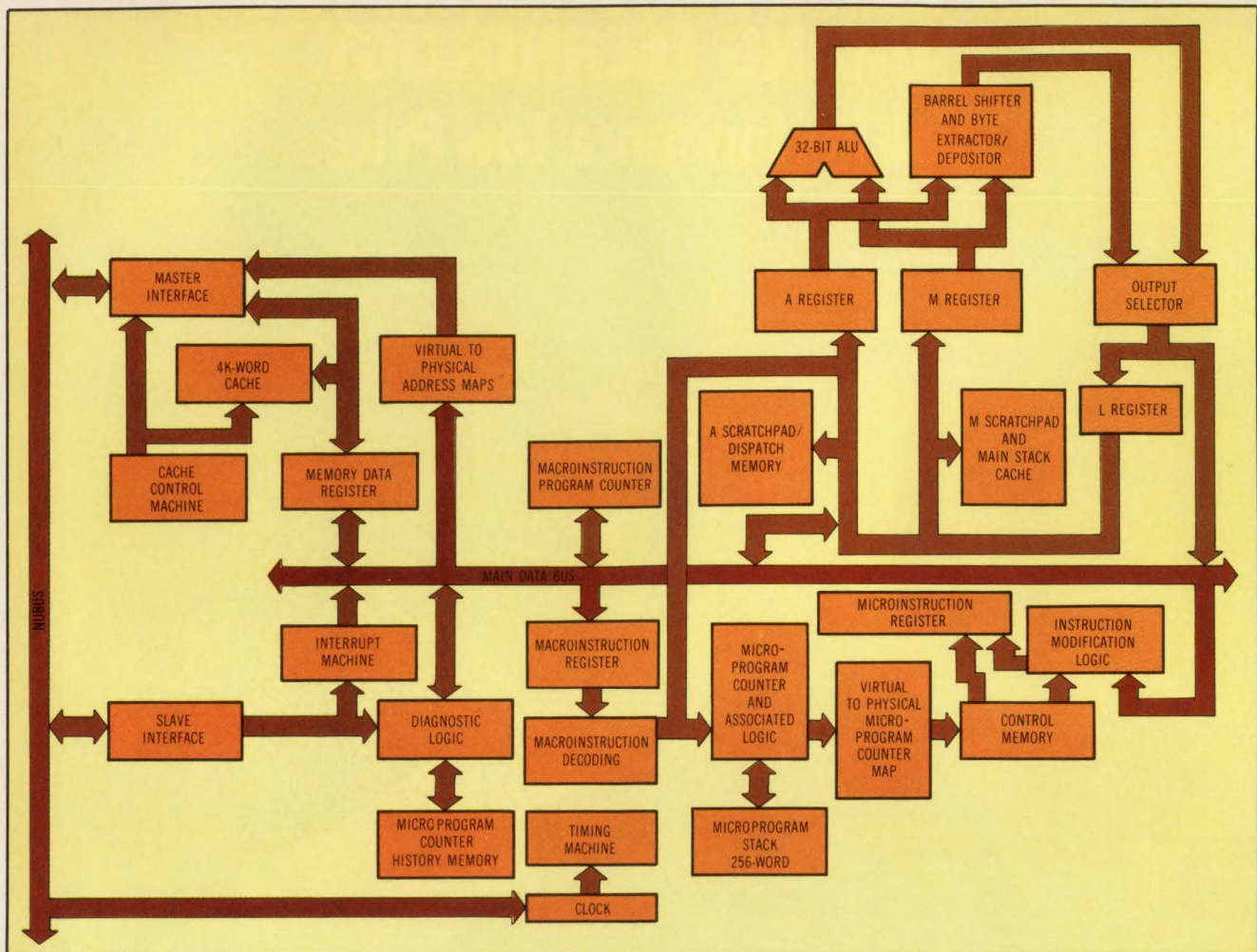


Fig 3 The Lambda's Lisp processor consists of four boards (not outlined in this diagram). Clockwise from the top left are the memory interface board, which interacts with the NuBus; the data paths board, where data manipulation takes place; the control memory board, which contains the microcode functions; and the random gates board, which includes several control and diagnostic functions.

SDU, which creates the appropriate Multibus interrupt. If both buses request each other simultaneously, the SDU prevents deadlock by giving priority to the slower Multibus-to-NuBus transfer, since NuBus-to-Multibus transfers can be rescheduled faster.

Another important aspect is Lambda's Ethernet-II interface, which executes the Advanced Research Projects Agency network (ARPANET) Transmission Control Protocol/Internet Protocol (TCP/IP). This interface facilitates resource sharing and interuser communication, easing the task of integrating a Lisp machine into an existing system. The Ethernet-II interface is controlled by another 8088-based board that provides the hardware interface and handles all network control protocols (NCPs). This frees the processor(s) from the overhead usually associated with NCPs, making protocol updates simpler and less time consuming.

Other hardware elements enhance NuBus operation. Memory boards in the NuBus system are self-contained memory controllers that support block transfers and error correction and logging. The

memory holds 39-bit words: 32 bits of data and 7 bits of error-correction code. The video display system supports a high resolution (800 x 1024) display with two 1M-bit video buffers (useful when screen updates should not be seen), onboard logical functions, and a keyboard-mouse interface. Rounding out the generic aspects of the architecture are a disk controller that can handle four storage module device (SMD) drives, a 470M-byte Winchester disk drive, and a card cage with 21 slots: 13 for NuBus, 5 for Multibus, and 3 for either.

### The Lisp processor

Four boards, utilizing high speed Schottky transistor-transistor logic (TTL) devices and communicating through a private bus on the backplane, constitute the Lisp processor. This general purpose 32-bit microprogrammable processor provides efficient pipelined execution of complex order codes. Although its optimal function is interpreting the Lisp compiler's bit-efficient 16-bit order code, the processor easily adapts to high level language execution as well as to specific

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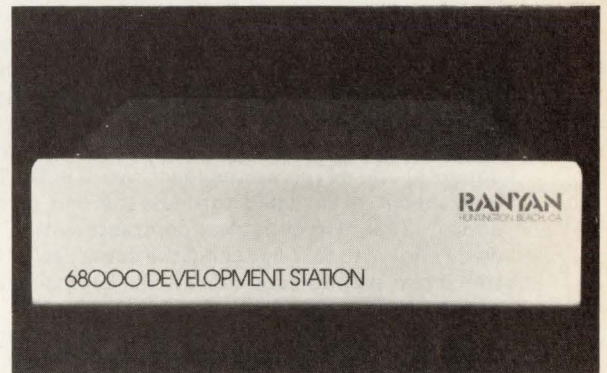
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## The Lisp language

The Lisp (List processing) language deals with arbitrary symbols—that can represent any concept—rather than numbers. The basic Lisp data structures are the atom and the CONS node. An atom, as its name indicates, is a data object that cannot be further broken down. A CONS node is a data structure that consists of two fields, each holding a pointer to another Lisp data object, which in turn may be an atom, another CONS node, or any other Lisp object, such as a string or an array. Any number of CONS nodes may be linked together to form data structures of arbitrary size and complexity; such structures prove ideal for handling unpredictable data such as natural-language representations. The list is one of the most important forms these complex data structures can take—hence Lisp's name.

Each Lisp atom has associated with it a property list, which gives additional information about the atom, including the atom's value (if it is a variable), its print name (a pointer to its character representation in memory), or any other property the programmer assigns. For instance, an atom that is an English word might have as a property its part of speech, its phonetic representation, or even its connotations.

Part (a) of the Figure illustrates Lisp's data structure. It represents a simple list—(THROW (THE BIG RED) BALL)—made up of six linked CONS nodes (the double squares) and seven atoms (each word in the list). NIL is a special atom used to mark the end of a list or sublist. This Lisp construct contrasts with a Fortran array shown in (b) containing the same list. In the Fortran array, parentheses indicate the beginning and end of sublists.

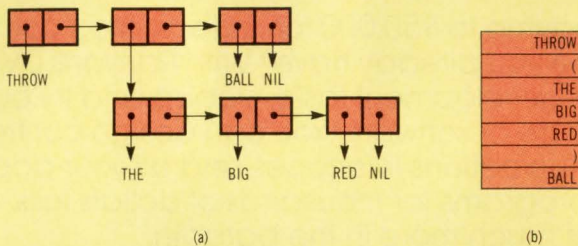
The Lisp list structure offers several advantages. For example, if a single sublist—such as "THE BIG RED"—appears in many lists, it need be represented in memory only once, and pointers in each main list can reference it. Moreover, the elements of a list need not be adjacent to each other within memory, allowing efficient use of storage space. Furthermore, elements can be easily added to or deleted from a list without affecting other data elements—only pointers need be changed. In contrast, many elements in a Fortran array must be moved up or down when one is inserted or deleted. In addition, Lisp allows sublists to be skipped during searches of main lists; as a result, Lisp can process large lists much faster and more efficiently than Fortran.

Productivity advantages stem from Lisp's functionally based programming style, its runtime nature, and its extensive editing and debugging facilities. In contrast to traditional programming, where a great deal of time is spent merely specifying application parameters that may not be fully known until the program is finished, a Lisp programmer can have a program up and running very quickly. It then can be modified to suit the needs of end users based on their actual experience with the software. As an example of Lisp's productivity enhancements, LISP Machine Inc devised a sophisticated Lisp-based CAD system that it in turn used to design its Lambda machine. The CAD system was completed in less than two man-years; if designed with traditional programming methods, completion would have required an estimated 50 to 100 man-years.

Lisp programs consist of a group of functions, in contrast to traditional languages, which consist largely of sequential instructions and attendant subroutines.

Lisp is thus a naturally modular language, and programmers can readily break down a function into many easily handled subtasks, or smaller functions. Lisp is highly recursive, allowing a function to call itself. This is a useful feature when a subtask is identical to the main task.

The language can either run interpretively or be compiled. In the interpretive mode, Lisp functions and data have the same structure; therefore, functions can manipulate or even create other functions. In modern Lisp machines, every bit of software, from the operating system to the editing and debugging utilities, is written in Lisp and can thus be easily customized to suit a programmer's needs. For example, a programmer can design applications software that creates a function in data-structure form, submits that structure to the system Lisp compiler (which is itself a Lisp pro-



gram), and then automatically executes the resulting compiled program as part of the applications software.

Lisp's runtime nature, which stems from its dynamic storage allocation and link-edit features, eases program generation by allowing programmers to defer decisions regarding the form of the final program. In contrast to traditional programming languages, Lisp does not require a declaration of required storage prior to writing the program. New storage is allocated during program execution as the program requires it. When the system senses that an area of memory can no longer be accessed by a program (eg, when a sublist's pointers are deleted from the main list), the inaccessible storage is automatically reclaimed and made available for new allocation through a process called garbage collection.

In addition, Lisp programs do not require a separate link-editing phase during compilation. Instead, functions are linked at run time and therefore can be easily changed even after compilation. Program modifications involve editing only those functions affected by the change and recompiling them—there is no need to recompile and link-edit the entire program.

Since Lisp has been the language of choice in the artificial intelligence field for many years, a powerful set of editing and debugging tools have been developed for it. Using such tools, a programmer can, for example, concurrently observe program source and execution, retrieve and modify any function, and recompile the modified function back into the program with very few keystrokes. Furthermore, because all of the programming utilities are written in Lisp, they can be easily incorporated into an applications program through Lisp's dynamic-linking capability. For example, the Lambda's Lisp Machine Lisp/Zeta Lisp environment includes an extensive window system, implemented by a message-passing feature called Flavors. This window system can be easily modified to serve as a user friendly interface for an applications program.



applications that rely on certain macroinstructions, which can be microcoded for faster execution. Main data paths of the processor are shown in Fig 3.

Four boards centralize related areas of the Lisp environment. Briefly, the data paths (DP) board contains the arithmetic logic unit (ALU), dispatch logic, scratchpad memories, and associated registers. The control memory (CM) board incorporates microcode functions and associated logic, and the microinstruction stack. The memory interface (MI) board, a NuBus master, contains cache, cache state machine, location counter, and diagnostic logic. Responsible for relations between the Lisp processor and the NuBus system, its operation is especially important for multiprocessor applications. Finally, the random gates (RG) board holds the macroinstruction decoder, statistics counter, history RAM, clock, matrix multiplier, and a slave NuBus diagnostic interface.

The Lisp processor's data paths are 32 bits wide: 24 bits for data and 8 bits for data-typing and other operations, giving the Lambda 67M bytes of address space ( $2^{24}$  4-byte words). A 40-bit enhancement (planned for early next year) will expand the address space to 21.5G bytes. Since the number of bits used for data-typing will remain the same, little or no reprogramming will be necessary.

In addition to its large address space, the Lambda uses a technique known as CDR-coding to reduce storage demands of list structures by almost 50%, making the address space seem even larger. CONS (constructor) nodes (see the Panel) cannot be inserted into a list compressed by this technique. However, since the processor automatically reexpands the CDR-coding when the list is accessed for modification, the technique is transparent to the user.

### Processor design aspects

Data are passed to and from the Lisp processor under control of the cache state machine, a specialized high speed processor. Using NuBus block-transfer capability, the cache state machine manages memory accesses in a look-ahead/look-behind mode based on the principle of set-local operations, or locality. Presuming that the next word to be accessed is nearby the last word requested, the machine transfers an entire block (up to 16 words) centered on the requested word into the cache.

To avoid the problem of one processor interfering with another's data and resulting inaccuracy of the data buffered in a processor's cache, the NuBus is monitored continuously. The cache state machine, in combination with the master interface, constantly checks the NuBus to determine whether any other processor is writing into a location represented in the cache. If so, it invalidates that location, thus both assuring reliable data and avoiding the need for cache sweeping—a fragile and unreliable method of cache verification.

Memory access occurs through a 2-level virtual paging system that employs three virtual-to-physical address maps to map 24-bit virtual addresses into addresses within physical memory in the NuBus. This paging implementation also supports an efficient garbage-collection algorithm, which reclaims static-memory areas less often than more volatile areas, thereby consuming less processing time.

The system's vectored interrupt system gives each device an address space in the interrupt slot, and assigns an address in software to each type of interrupt. Each interrupt's status is stored in a RAM, which is scanned to see if any device has requested an interrupt. When an interrupt request is found, scanning stops, thus preventing interrupts from being lost (new interrupts are still stored). No other interrupt is noted until the current one is serviced and cleared. Provision for both fast and slow interrupts provides a flexible interrupt environment.

Associated with the interrupt machine is the slave interface to the NuBus, used largely for diagnostic purposes. It communicates with the diagnostic logic. This logic includes a 4K x 16-bit microprogram-history RAM that holds the control memory addresses of the last 4096 microinstructions executed. For debugging, the system can be manually halted. It can also be programmed to halt in the event of a specified error or other condition, such as the execution of a given instruction a set number of times. At the time of the halt, the system's state is saved with no loss of information: the machine state is exactly as it was during the execution of the instruction that initiated the halt.

Diagnostic logic can then be used for unlocked transactions to trace machine state, or can single-step the system with user-generated clocks to track down possible timing problems. In combination with software debugging facilities, these diagnostic capabilities enable programmers to easily pinpoint and correct problems from the largest programs to the user-written microcode. The RG board also contains a high speed 16 x 16 matrix multiplier. This greatly speeds array referencing as well as simple arithmetic.

A macroinstruction program counter holds the address of the next macroinstruction to be executed. Since two consecutive instructions are usually used, two macroinstructions are fetched concurrently, packed into a single 32-bit word, and placed into the macroinstruction register. Macroinstruction decoding hardware allows a transfer to the appropriate microcode subroutine in a single operation, saving a significant amount of processing time.

Processor pipelining and virtual control store operation are governed by the microprogram counter and its associated logic. The logic tracks the options available when making or returning from a microinstruction subroutine call. This tracking prepares the machine for rapid execution of the next

macroinstruction after it completes a microinstruction subroutine. A microcode subroutine-return stack, the 256-word microprogram stack, in addition to standard microinstruction addresses, contains extra control bits used to speed the execution of macroinstructions.

A virtual microcode paging implementation, the system's 64K x 64-bit virtual control store, is paged into a 16K x 64-bit physical control memory. A Lisp microcompiler allows programmers to write into the control store using Lisp, thus taking advantage of the language's productivity and editing facilities even while microprogramming.

The DP board performs actual data operations. Most significant design aspects for the execution of Lisp programs involve the scratchpad memory organization and some pipelining enhancements. The A scratchpad/dispatch memory holds multiway branch tables that are selected by a field in each dispatch microinstruction. In the M scratchpad memory, a 2K pointer-addressable RAM stores the top of the system stack, with hardware stack pointers. Due to Lisp's applicative, recursive nature, a large percentage of main memory references in the Lambda are to the stack, so this stack cache speeds up processing. Instruction modification logic associated with the control memory and microinstruction register supports relative addressing in the

scratchpad memories. The L register stores information to be written back to the A or M scratchpad. This write is delayed until the beginning of the next microinstruction because of the Lambda's pipelined nature. If data in the L register are to be transferred from the A or M register (for use in the ALU) on that instruction, scratchpad memory is bypassed. Data are sent directly on and the scratchpad is updated from the L register.

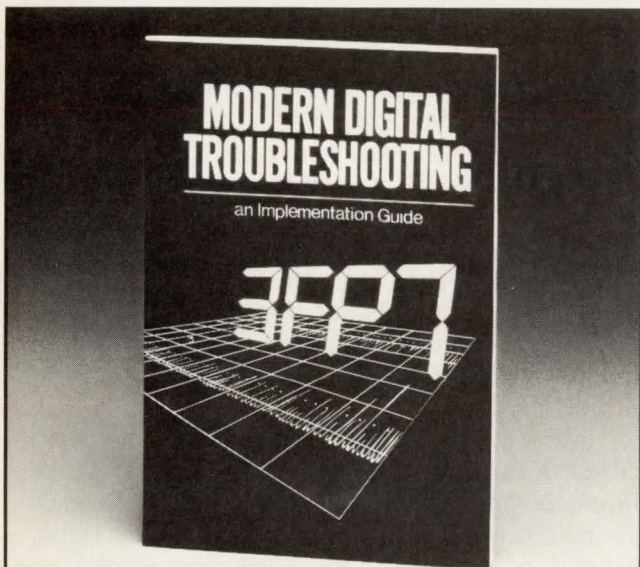
### Lisp as a tool

Multibus compatibility of the NuBus in the Lambda enables system integrators to take advantage of compatible products. Furthermore, the NuBus's multiprocessor capability aids in integrating Lisp into existing computing systems. An optional 68000-based processor, which implements a Berkeley-Unix environment, runs concurrently with the Lisp processor. The two computational environments are linked by a Streams/Pipes interface, based on the communication primitives of Lisp and Unix.

Serving as a backend processor to Lisp, the 68000 can allow current software to continue operating under the supervision of an evolving Lisp applications program. Conversely, the 68000 can act as a multi-user, multitasking front end to package and send requests to the Lisp processor, thus overcoming traditional limitations of the Lisp language.

The large programmable control store and the Lisp microcompiler allow the Lambda to be optimized for a given application by microcoding frequently called functions. This general purpose aspect of the Lambda design is likely to be extremely important to system integrators. For researchers, the microprogramming facilities are useful in emulating higher level language environments to aid in the design of advanced architectures. For example, the Lambda processor can be configured to perform Prolog-specific operations. (The Prolog logic programming language, based on Lisp, was chosen by the Japanese for their much publicized Fifth Generation Computer Project.) In addition, other machines' instruction sets can be emulated in microcode for efficient and flexible simulations.

Finally, the user of a device-independent bus such as the NuBus creates an open ended system. While a rigid computer architecture locks users into obsolescence, the NuBus's device independence concept permits processors, boards, and peripherals to be added as needs demand. Thus, Lisp machines can evolve along with user needs.



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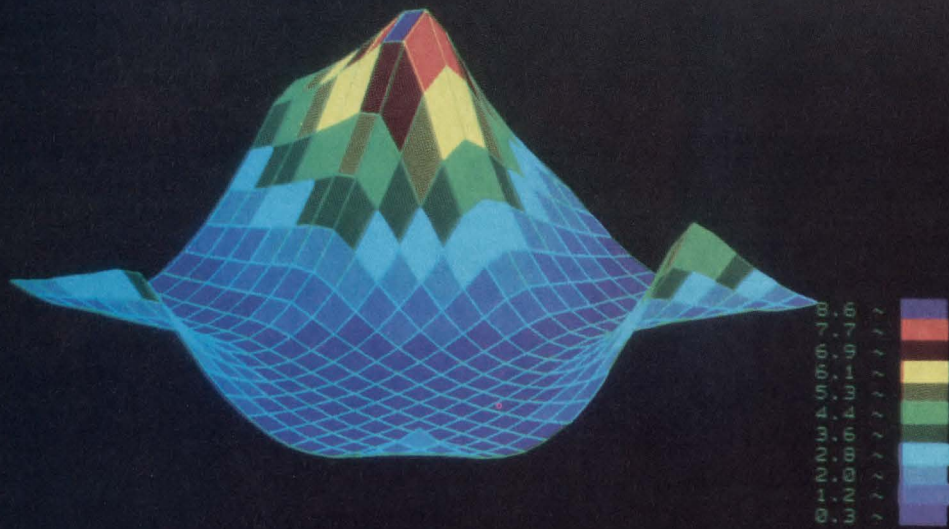
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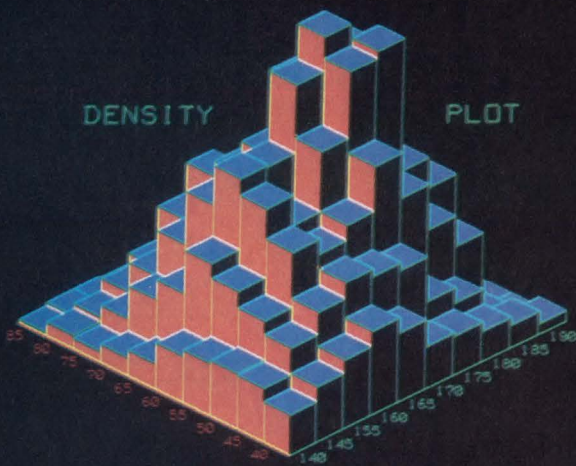
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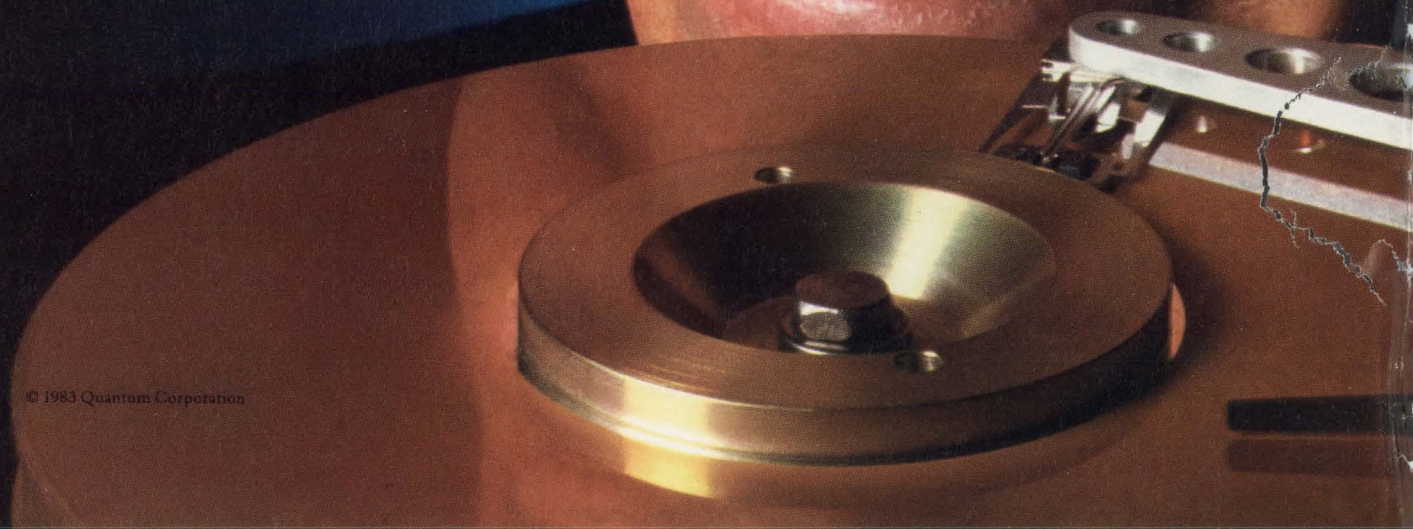
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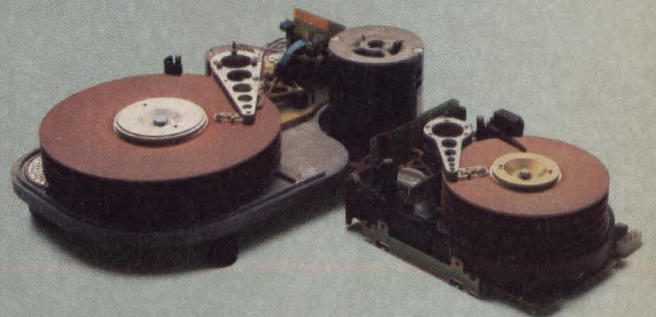
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# PARALLEL ADDRESS GENERATION SPEEDS SUPERMINI

**Architectural enhancements endow TTL superminicomputer with ECL-like performance. Increasing the pipeline staging allows loads and stores to appear as single-cycle events.**

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**by Robert Beauchamp and  
Steve Staudaher**

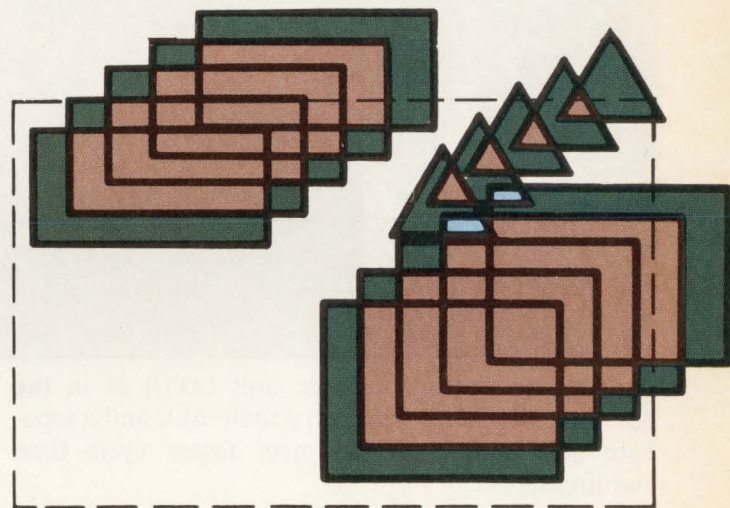
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The stated aim of the minicomputer industry since its inception has been and is to double performance every two years without increasing cost. It goes without saying that there are several routes to this goal. One track relies on the added performance inherent to state of the art semiconductors; another builds on architectural enhancements using off-the-shelf parts. Data General's MV/10000, a 32-bit supermini computer with performance levels equivalent to those obtained using emitter-coupled logic semiconductor technology, follows the second track.

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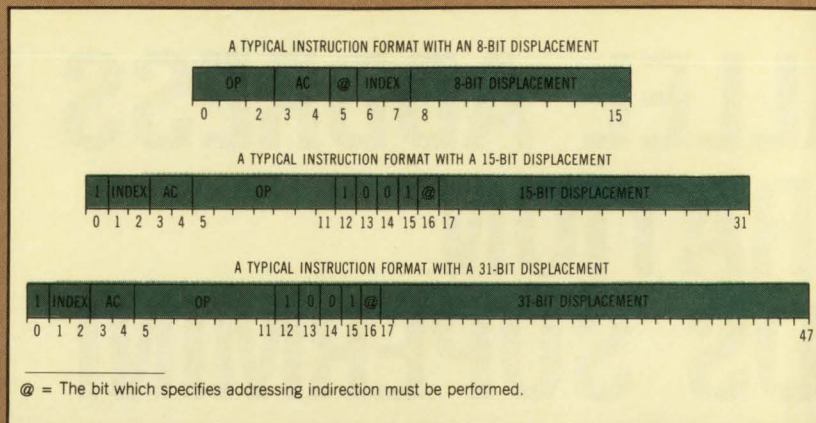
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*Steve Staudaher is project engineer at Data General Corp. He is responsible for hardware development on the MV/10000. Mr Staudaher holds a BSEE and an MSEE from Worcester Polytechnic Institute.*



Building on the foundation laid down by the MV/8000, the Eclipse family's previous top of the line machine, the processor incorporates additional performance accelerators to achieve its goal. While gate arrays and emitter-coupled logic (ECL) would achieve the cycle time reduction necessary to meet performance goals, available parts were either under developed or too expensive to fit the cost half of the equation. Therefore, the design uses standard transistor-transistor logic (TTL) parts. Performance is attained by incorporating dual-ported cache memory, instruction processor (IP), and a pipelined microsequencer—all concepts carried over from the MV/8000. However, instead of double

## Architectural addressing



Four 32-bit accumulators (AC0 to AC3), a CARRY bit, a program counter, four floating point accumulators, four stack management registers, and a pair of status registers make up the machine's programmer-visible state. Each instruction consists of a 16-bit opcode. Opcodes either contain an 8-bit displacement or are followed by a 16- or 32-bit displacement.

The instruction set supports an addressing structure that has four address calculation modes and can reference byte, double byte (word), and quadruple byte (double word) operands. These addresses can also follow indirection chains. The four addressing modes, referred to as index modes, are

- Absolute** Displacement is used as the operand address.
- PC Relative** PC of the displacement is added to the signed displacement and used as the operand address.
- AC2 Relative** Contents of AC2 are added to the signed displacement and used as the operand address.

**AC3 Relative** Contents of AC3 are added to the signed displacement and used as the operand address.

Most addresses form a 31-bit logical address (some generate a 32-bit byte boundary address). The address translation unit (ATU) translates this address into a physical memory address. The ATU speeds the translation and memory protection enforcement process by storing entries of memory resident page translation tables in cache. If indirection is specified, the index mode calculation is performed first. Then data contained at that address are used to continue the indirection resolution or to address the desired data. The decision to terminate the indirection resolution is based upon the most significant bit of the deferred address datum: 1 implies continue, 0 implies stop.

Load effective address (LEF) instructions and instructions that operate on the displacements as data (ie, immediate instructions) are also handled. Formation of an effective address is referred to as an EFA calculation.

cycling the arithmetic logic unit (ALU) as in the MV/8000, the design relies on a main ALU and a separate addressing ALU to meet faster cycle time requirements.

### Cache memory

A time-multiplexed cache that can be accessed independently from either the central processing unit (CPU) or a separate input/output (I/O) processor, the dual-ported cache cycles at twice the CPU rate and dedicates alternate cycles to each port. Multiplexing greatly reduces contention between I/O and CPU memory bandwidth demands. The cache can be referenced by the CPU every microcycle; it is pipelined to accept addresses for the next memory reference while it is processing the current reference. This is especially valuable for multiple reference instruction types such as stack manipulations (push, pop, etc). However, load

accumulator (LDA), and store accumulator (STA), type references still require two microcycles: one for address generation and one for data transfer.

The IP probably contributes most to performance enhancement in that it is capable of performing instruction encachment, prefetching, decoding, and displacement formatting. The instruction cache (1K byte for the MV/8000 and 4K bytes for the MV/10000) reduces memory bandwidth contention with the CPU data stream. Eliminating prefetch and decode time from instruction execution time results in a 200% to 300% speed improvement for simple instructions, such as register-to-register add.

Special operating modes in the MV/8000 ALU allow an address to be calculated during the first half of the CPU clock cycle. The second half of the clock cycle is used to perform another operation, such as transferring data to or from the data cache, or generating an intermediate arithmetic calculation.

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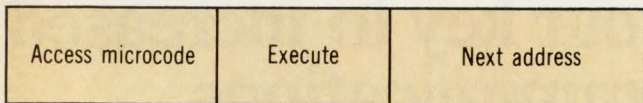


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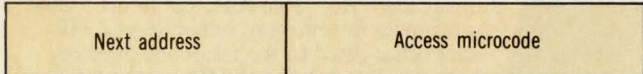
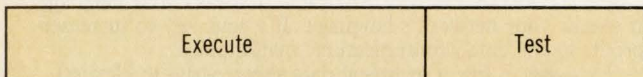
[The second half of the cycle is also used by the address translation unit (ATU) to generate the physical address to the data cache.] This split cycling effectively allows address generation to occur in parallel with other arithmetic operations for most memory reference intensive instructions.

### Pipelined microsequencer

Microcoded architectures typically execute the current microinstruction, generate the next micro-address, and access the microcode all in one clock period. This allows conceptually simple microcode because sequencing is based on tests that reflect the results of the operations being performed in that same cycle.



Better overall performance, however, results when these operations are pipelined in one or two stages. In the MV/8000 and MV/10000, staging parallels the next address selection and microcode access with the execution and test selection.



Notice that the test condition is selected by the microcode which is being accessed; ie, the microinstruction following the one that is generating the operation to be tested. One level staging works better than two, since other operations in the system (notably address generation and translation, and memory access and transfer) require an amount of time that balances this staging extremely well. In addition, staging these other operations would require significant amounts of additional logic to detect and handle serial dependencies, as well as added logic for the staging registers.

Taking these performance accelerators into account and considering even faster cycle time requirements, a separate addressing ALU seemed a natural extension. (Double cycling the main ALU as with the MV/8000 did not appear realistic.)

Since this independent address generation hardware lies idle during the final cycle of all micro-routines, the next macroinstruction is allowed to use it during its otherwise idle period.

### Performance evaluation

The address generator (AG) significantly improves the performance of some instructions. One that benefits is the LDA instruction. How much

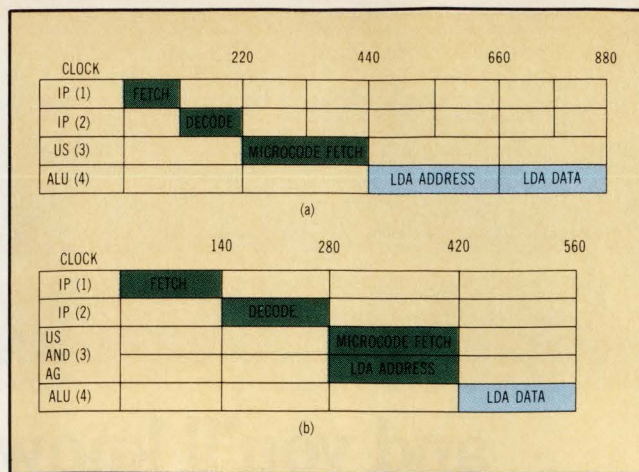


Fig 1 Comparing the operations required to perform an LDA instruction in the MV/8000 (a) and the MV/10000 (b) shows the degree of improvement attained by the addition of an independent address generator. Not only is the /10000 cycle faster, but the ALU is used for one cycle instead of two, reducing the effective execution time.

improvement results can be seen by comparing required operations for the MV/8000 and MV/10000 (Fig 1). Since the MV/8000 cycles at 220 ns and the MV/10000 at 140 ns, the LDA instruction executes better than three times faster.

Although the instruction is in some partial stage of completion for four cycles in both machines, the MV/10000's ALU stage is used half as much. Since the ALU is the slowest stage and limits the overall throughput of a pipeline, halving its use greatly reduces the effective execution time. Effective execution time for an LDA instruction is 140 ns on the MV/10000 versus 440 ns on the MV/8000. In addition, the AG constitutes a broader use of the third stage of the pipeline.

Analyzing the Whetstone program (an accepted benchmark) for dynamic instruction usage revealed typical relative occurrence of instructions that would benefit from the AG. The resulting histogram of instructions, used with estimates of instruction execution times, led to predictions that an additional 5% increase in the logic (half a board out of an 11-board system) would have great performance payoff.

*Since the ALU is the slowest stage, halving its use reduces the effective execution times.*

The accumulator update path from the ALU to the AG was given top priority during the design of the system interconnection (see Fig 2). Since indexing modes require the use of AC2 and AC3, it is necessary to maintain a copy of these and other accumulators (ACs). Much of the microcode never

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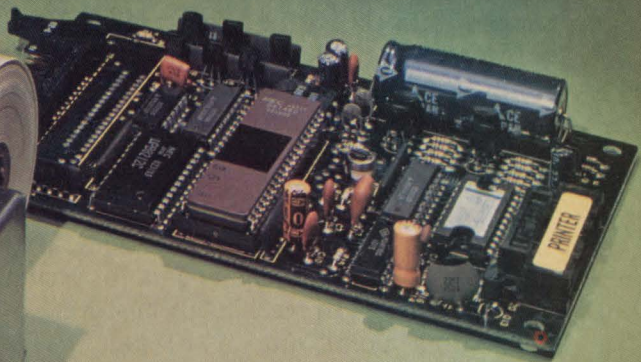
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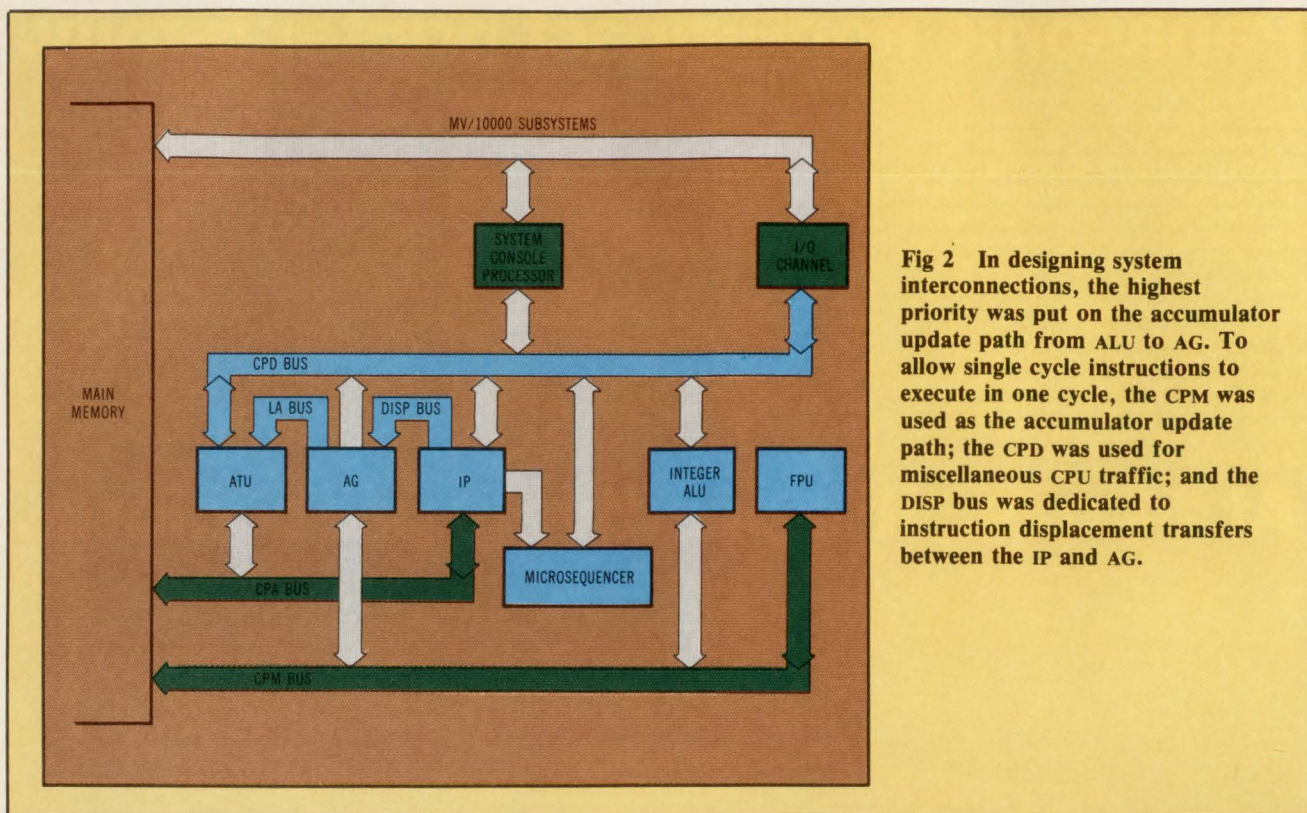
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**Fig 2** In designing system interconnections, the highest priority was put on the accumulator update path from ALU to AG. To allow single cycle instructions to execute in one cycle, the CPM was used as the accumulator update path; the CPD was used for miscellaneous CPU traffic; and the DISP bus was dedicated to instruction displacement transfers between the IP and AG.

explicitly knows which particular AC it is updating, since it defers through the macroinstruction's destination accumulator field.

### Accumulator copies

Single cycle instructions—LDA and register to register operations (add, sub, etc)—must execute in one microcycle to achieve the performance goals. Keeping the LDA instruction fast implies that memory data should be able to load directly into the AG's register file. This makes the central processor memory (CPM) bus the best candidate as the accumulator update path, if the ALU can produce results fast enough to transfer them across this bus to the AG.

The best transfer time results from keeping capacitive loading on the CPM to a minimum. Therefore, only those boards that require data for accumulator loads are allowed to receive this bus: ALU, AG, and the floating point unit (FPU) pair. A second, general purpose central processor data (CPD) bus handles miscellaneous data traffic for the CPU. The CPD bus communicates with the I/O channels for their control, with the IP to read the logical program counter (PC), and with the ATU to service translation cache misses. It is also used for state save and restore during page faults and other exception conditions.

Using the memory bus as the accumulator update bus, however, poses a problem for the IP since it needs a memory data path to fill its instruction cache. Even though the memory bandwidth is not

consumed by the CPU, the bus bandwidth is. Giving the IP a connection behind the cache, common with the memory bank controller, resolves this problem, but raises a question. Should the IP request its data from the bank controller or the data cache?

Simulations with data and instruction streams obtained from the MV/8000 microcode simulator proved that the best memory system performance was obtained by having the data cache service the IP. The larger size of the data cache (4K bytes) enabled it to back up the instruction cache (1K byte) without adversely affecting the data stream's hit ratio. The most pessimistic simulation showed a decrease of 0.2% in the data stream hit ratio while producing a 34% hit ratio on the stream of references which missed the IP's cache. This increased the system's aggregate hit ratio from 96.5% to 97.3%, resulting in a fair savings in memory bandwidth and time, since the cache responds faster than main memory. Measurements on actual hardware running moderate system loads show an average hit ratio of 50% on the IP miss stream and 70% at times. Although data are provided by the cache, the IP can capture desired data from the bank controller when the cache misses.

### Instruction displacements

A dedicated bus between the IP and the AG allows instruction displacements to be transferred. Since the IP functions autonomously within the system, this eliminates the need to arbitrate the CPD bus, which is multiply sourced and controlled

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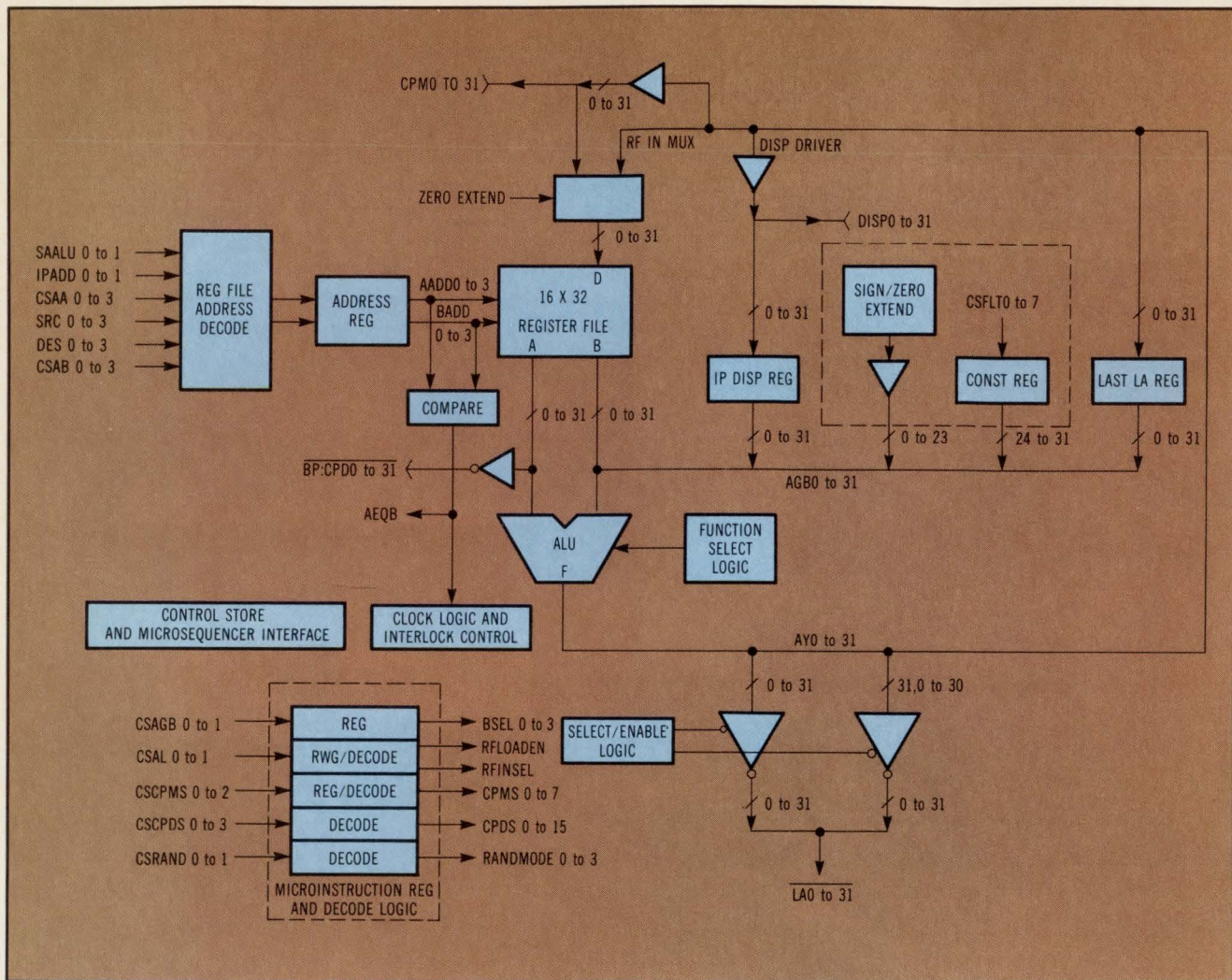
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**Fig 3** Primarily a dual-ported 16 x 32 register file and an ALU, the AG is controlled by both system microcode and instruction decode information enabled through microcode control. IP decode information provides specifics for memory start and index information.

by microcode. The displacement (DISP) bus is also used to transfer the logical PC back to the IP whenever program flow must be changed (ie, jumps). No performance disruption occurs, because current IP operations are already invalidated by the change in program flow. Additional benefits of using the DISP bus for jump addresses, are that the logical address (LA) bus can be shorter and more lightly loaded, and that the pinout requirements for the IP board are reduced.

From a performance standpoint, the AG's most important job is pregenerating operand addresses. The AG is predominantly a dual-ported 16 x 32 register file connected to an ALU. Three additional alternate operand sources are connected into the B leg of the adder: The DISP register holds instruction displacements, the LAST-LA register holds the last started memory address, and the CNST register provides sign-extended 7-bit constants from the microword. The austere ALU can only perform A + B, B - A, and Pass B functions.

Two mechanisms control the AG (Fig 3). One is the system microcode and the other is instruction decode information enabled through microcode control. Microcode control consists of five fields (these are detailed in the Panel, "Address generator microfields"). Microcode fields have the following form:

- AA Designates the A port Reg File Address
- AB Designates the B port Reg File Address
- AGB Designates the source for the B leg of the ALU
- AOP Indicates the operation the ALU will perform
- AL Controls the Write Enable to the Reg File and the source of the data to be written into the Reg File

When the microcode enables address pregeneration to occur, control defers to the IP decode information and the interlock logic on the AG is enabled. This decode information contains specifics for the particular memory start to be performed: Read or Write, the size of the operand access (Byte, Word, Double Word), and the index information for the A port address and interlock hardware.



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## Address generator microfields

### AA/AB: Address Generator Areg/Breg Specifier

#### Mnem Val Description

AGO	0	Macroprogrammer Accumulators
AG1	1	" MUST BE Copies of the ALU's AC0-AC3
AG2	2	" at New Instruction boundaries
AG3	3	"
SP	4	Wide Stack Pointer
ONE	5	Constant = 1
TWO	6	Constant = 2
LAT	7	Reserved Register for Long Address Translations
ARO	8	Microprogrammer General Registers
AR1	9	" No content restriction as with AG0-3 above.
AR2	A	"
AR3	B	"
AR4	C	"
AR5	D	"
SRC	E	Register addressed by ACSR
DES	F	Register addressed by ACDR

Notes: 1) The AA field cannot be used during EFA calculations.

A-2

### AGB: Address Generator AGB Buss Source Specifier

#### Mnem Val Description

D	0	Displacement register
B	1	Register File B port
C	2	Micro Constant register
L	3	Last LA register

Notes: 1) Last LA Reg is loaded only on memory starts, it is not loaded during LATs.  
2) D must be coded in this field during EFA generation.

### AOP: Address Generator ALU Operation Select

#### Mnem Val Description

SUB	0	B - A (Carry in of 1 for 2-comp. subtract)
ADD	1	A + B (No carry in)
PSB	2	Pass AGB bus
EFA	3	Attempt to perform next EFA calculation

### AL: Address Generator Register Load Specifier

#### Mnem Val Description

N	0	No load
M	1	Load from CPM
Y	2	Load from AY bus
C	3	Load from CPM bus only if Test selection coded this cycle is true

Notes: 1) All loads are done to the register addressed by the AB addressing field.

In addition, the IP controls the loading of the DISP register with a Write Enable signal which is activated depending on the state of the instruction pipeline. If the next instruction needs a displacement and the AG has not received it, then a wait state is inserted into the executing microcode stream instead of a real starting microaddress. Other important decode information, such as the signal which determines that a memory start should be performed with the initiation of the new instruction, is also qualified by the existence of valid starting micro and displacement information.

### Pregeneration of addresses

Address pregeneration is accomplished by reading the index operand from the register file onto the A leg of the ALU and the displacement operand onto the B leg. The ALU performs the appropriate operation as shown below:

Index	ALU Operation
0 Abs	Pass B
1 PC	Pass B*
2 AC2	A + B
3 AC3	A + B

\*Note that the IP has already added in the PC for this case.

Hardware must force the correct address to the register file's A port and determine the ALU's operation. Both decisions are enabled by the fourth encoding of the ALU operation microcontrol field. Microcode must select the DISP register onto the B leg of the ALU. Therefore, AG microcode for the last line of any microroutine looks like:

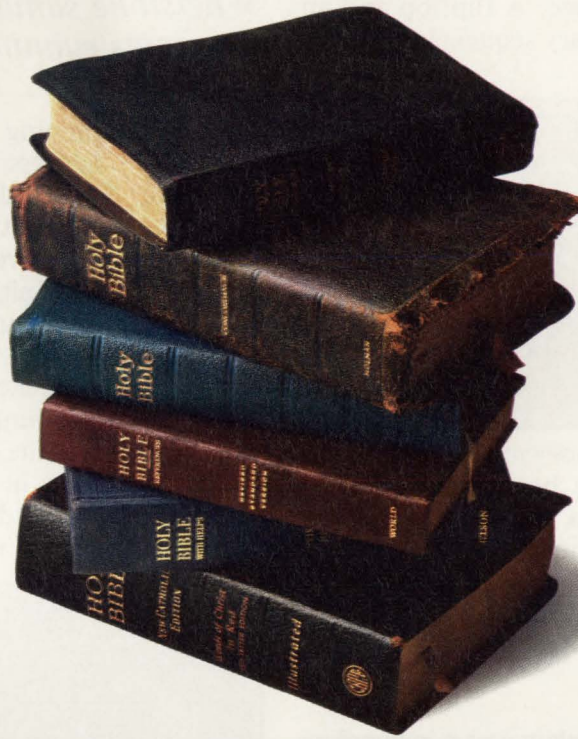
Microfield: AA AB AGB AOP AL  
Value: 0 x D EFA x

Those fields that control register file loading (the AB address and the AL mux select load enable) are not specified. The microprogrammer can use these resources to ensure that the AG's primary assumption is valid: that copies of AC2 and AC3 are available.

This simultaneous updating capability brings up a second problem inherent to the AG—the synchronization of serial dependencies. An example of a serial dependency is the use of an index register that is modified by the previous instruction (Interlock).

Effective addresses (EFAs) can only be performed in the last cycle of a microroutine. At that time, only one accumulator potentially needs updating. Therefore, comparing the addresses of the register file's A and B ports detects the interlock case. Any index register that is in use will be addressed by the A port and any register that is being updated will be addressed by the B port. This comparison is further qualified by index mode 2 or 3 (the only two which

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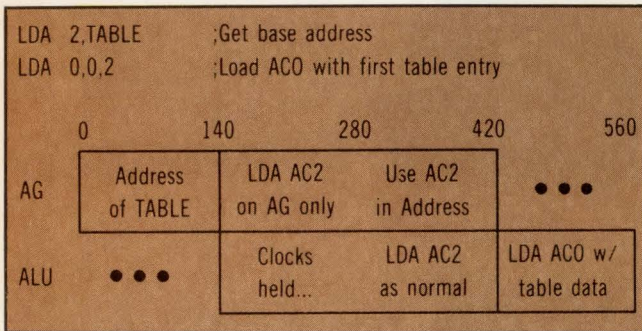
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use ACs) and by decode information that designates if an EFA is required.

When an interlock situation is detected, the operation must still be correctly executed. At this stage, all hardware control is trying to perform the correct operation; only the A port data is incorrect. To correct this problem, clocks to all of the system except the AG's register file are held. This allows new data to be written into the index register. From there it is read out to the A port during the second half of the extended clock period, allowing the addressing operation to complete. A flipflop and an AND gate provide the necessary sequencing for the clock hold control signal.



Synchronization with memory must also be mentioned, since wait states can be generated by the memory system and the data to update the index register may come from memory. Therefore, the clock control signals generated by the memory system must have priority over the clock control signals generated by the interlock detection hardware.

### Immediate instructions

The address generator also plays a part in handling immediate type instructions. Here it simply stages the immediate data from the displacement register into the logical address register (LAR). The initial microinstruction of the immediate instruction's routine then accesses the data from LAR, thus saving the IP additional staging hardware and data paths. The path from LAR into the ALU is carefully timed. This timing allows an arithmetic operation to be performed on the immediate data and the result to be transferred to update an AG accumulator. Thus, instructions such as WADDI (32-bit add immediate to accumulator) can execute in one cycle.

The AG was designed to serve as an independently controlled ALU for address generation within microroutines. In this role, it increases machine performance by freeing the main ALU. Thus, the main ALU can concentrate on operations such as bounds checking and data movement in the stack instructions.

Its potential utility can be shown by an instruction that is not standard, but could be implemented through the machine's Writable Control Store option. To implement this ADD REAL ARRAYS

instruction, requires an inner microcode loop containing only three instructions (assuming that appropriate setup and completion is handled outside the loop). The operation is pipelined three levels deep. This pipelining allows the previous answer to be written while the add is performed on the current operands and the next set of operands are fetched.

### Performance evaluation verified Whetstone simulation, showing some programs running 2.5 times faster.

After determining the need and cost effectiveness of an address generator, the design team embarked on the detailed work. Early worries about the complexity of the system interactions turned out to be relatively simple problems to solve. One of the initial concerns was the ability to keep the two accumulator copies identical. To this end, the microcode simulator was programmed to verify the consistency of these registers at each macroinstruction boundary. Only a few cases were discovered where the microcode was in error due to this requirement; in general, the constraint was easily achievable and required little extra thought or programming effort.

Operation: X + Y → Z			
AG	FPU		ALU
address Y element	Compare.	Read next X	Handle loop count
address Z element	Prescale and add.	Read next Y	
address X element	Normalize and round.	Write last Z	

Needless to say, the preliminary design was not flawless, but laboratory checkout identified the deficiencies and remedied them. Performance evaluation verified the Whetstone simulation to be correct and some programs were found to run better than 2.5 times the performance of the MV/8000.

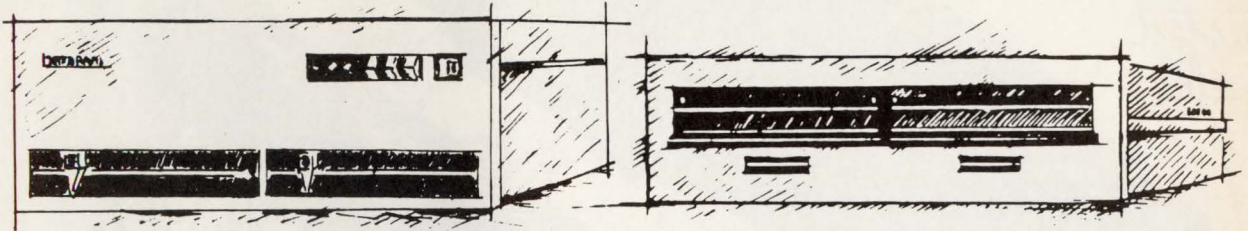
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Q-bus and UNIBUS compatible versions of the FD-311 provide dual RX02-compatible 8" floppy drives for \$2,400. Our new 7" high A21 combines dual RX02-compatible 8" slimline floppies with an 8-quad slot Q-bus card cage for only \$3,500. Both products are supported by the industry's widest range of LSI-11 compatible products. Call or write for details.

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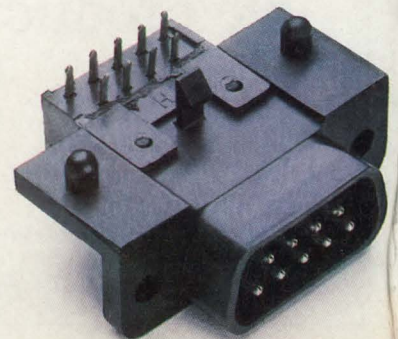
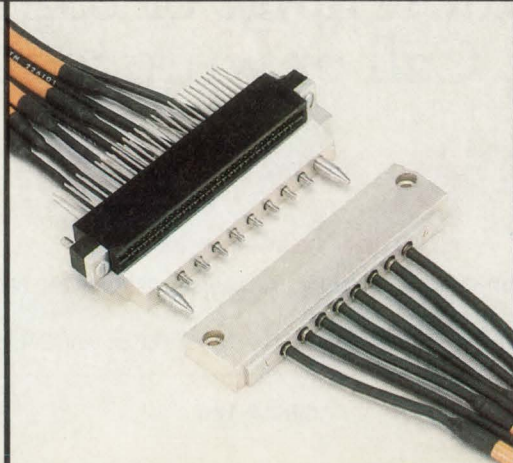
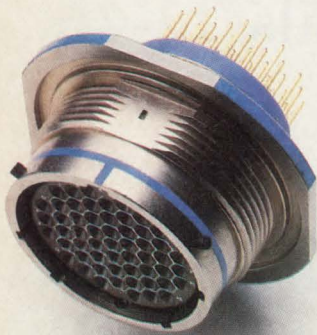
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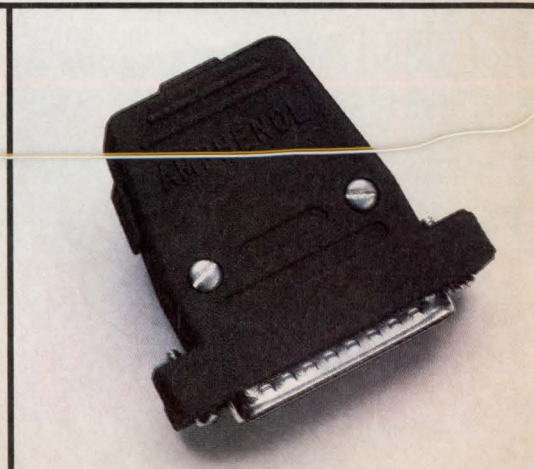
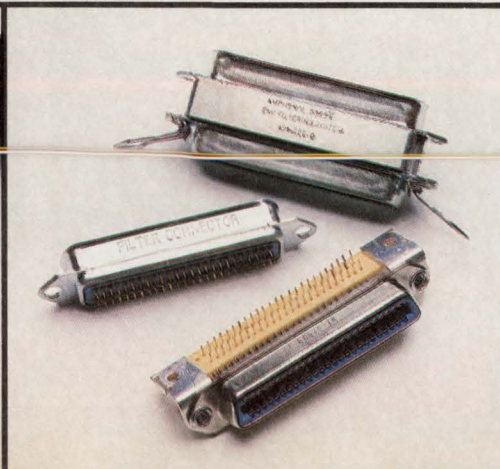
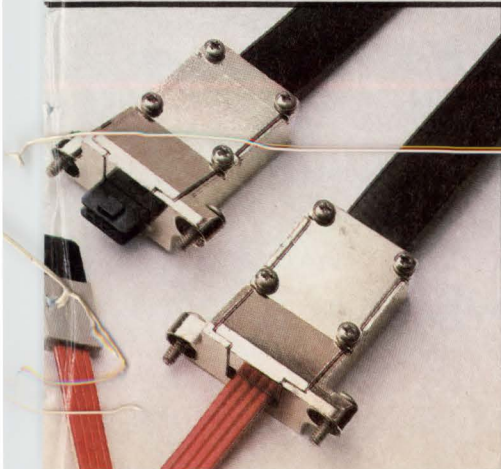
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CIRCLE 181

Planar Coax Interconnect Harness

Filtered Ribbon Connectors

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*They are Momentum 32/4s.<sup>TM</sup>*

*Inside and out, the most versatile high performance professional workstation available to OEMs.*

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*The look of the 32/4 gives you an immediate sense for its capabilities. Its lines wrap smartly around the most compact package in its class. A class by itself. Designed by the Italian styling master, Bertone.*

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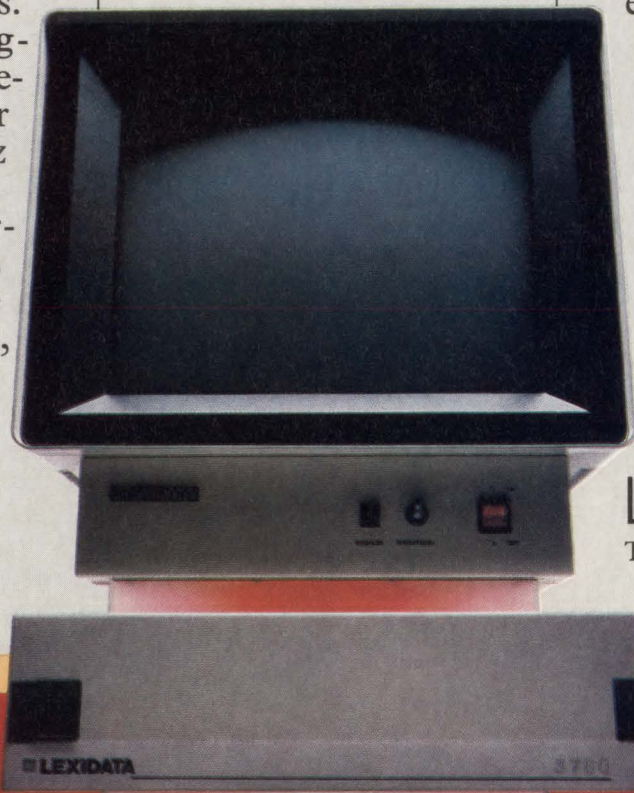
*42 million  
pixels  
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CIRCLE 183



# COMPUTER SYSTEM ISOLATES FAULTS

**Maintaining transaction processing systems in continuous operation, a special computer system detects and isolates faults, then transfers work loads to the appropriate backup resource.**

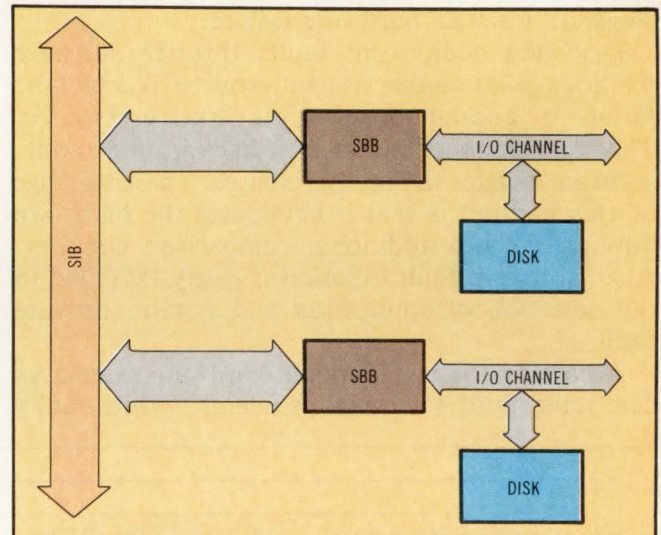
by Donald E. Hall

Online transaction processing is the technique of accessing computer information in real time from one or more local or distributed data bases. In many online transaction processing systems, the computers must be "up" or online continuously since users now expect uninterrupted service. Making a system uninterruptible (fault tolerant) involves the use of redundant hardware, hardware fault detection through software, or a combination of both methods. But whatever the method, fault tolerance is a complex issue encompassing cost, hardware, software, operator intervention, data integrity and recoverability, and system availability.

One company addressing these issues is Tolerant Systems, with its Eternity series computer system. An Eternity system is actually 1 to 15 computer systems, called system building blocks (SBBs), interconnected by a communication network. Fig 1 shows a block diagram of the modular, loosely coupled system.

Modularity is provided by Tolerant's flexible architecture technique. This allows a user to expand

*Donald E. Hall is product manager at Tolerant Systems, 81 E Daggett Dr, San Jose, CA 95134. He is responsible for product marketing for the Eternity series. Mr Hall holds a BS in electrical engineering from the University of Washington and an MS in computer science from the University of Oklahoma.*



**Fig 1 Eternity computer system's flexible architecture is centered around complete processors called system building blocks (SBBs). Multiple SBB systems communicate over a passive coaxial cable called the system interconnect bus (SIB).**

system capacity with nondedicated computers that can be assigned to tasks such as increasing processing power, user accessibility, and database size as dictated by needs.

A loosely coupled system enhances system reliability. Errors that can be propagated in a tightly coupled system are more likely to be detected in the loosely coupled variety. For example, if the two disk drives in Fig 1 are connected to the same controller or input/output (I/O) channel in a tightly coupled system, errors introduced by the controller

or I/O may be copied to both disks. If the drives are connected to separate systems—loosely coupled—this replication of errors does not occur.

### The state of fault tolerance technology

No redundant hardware technique for fault tolerance provides a completely satisfactory solution to all system problems. For example, the most primitive method (“hot standby”) has manual switching. In such a system, an operator must manually switch the backup computer online if a failure occurs in the primary computer. In addition to the obvious problems of human intervention, hot standby is an expensive solution since the backup machine performs no work while in the standby mode.

Another hardware fault tolerant scheme uses multiple processors performing the same operation and comparing outputs. This is often implemented as a majority voting system in which three processors compare outputs. Two of the three must agree for the operation to be carried out. While this scheme was used successfully in the space program, that program considered reliability rather than cost as the highest priority. Moreover, a problem with multiple processors is that the circuitry used in the comparison or voting processes may itself be the cause of a system hardware failure.

Detecting component faults through software methods relies on one system resource to detect the failure of another previously operating resource. Through diagnostics run in a background mode, software isolates the faulty resource. The advantage of this method is that it eliminates the hardware duplication and additional comparison circuitry. Also, software fault isolation is easily extended to the detection of application and system software faults.

According to one viewpoint, hardware techniques can solve fault tolerance problems. While faulty

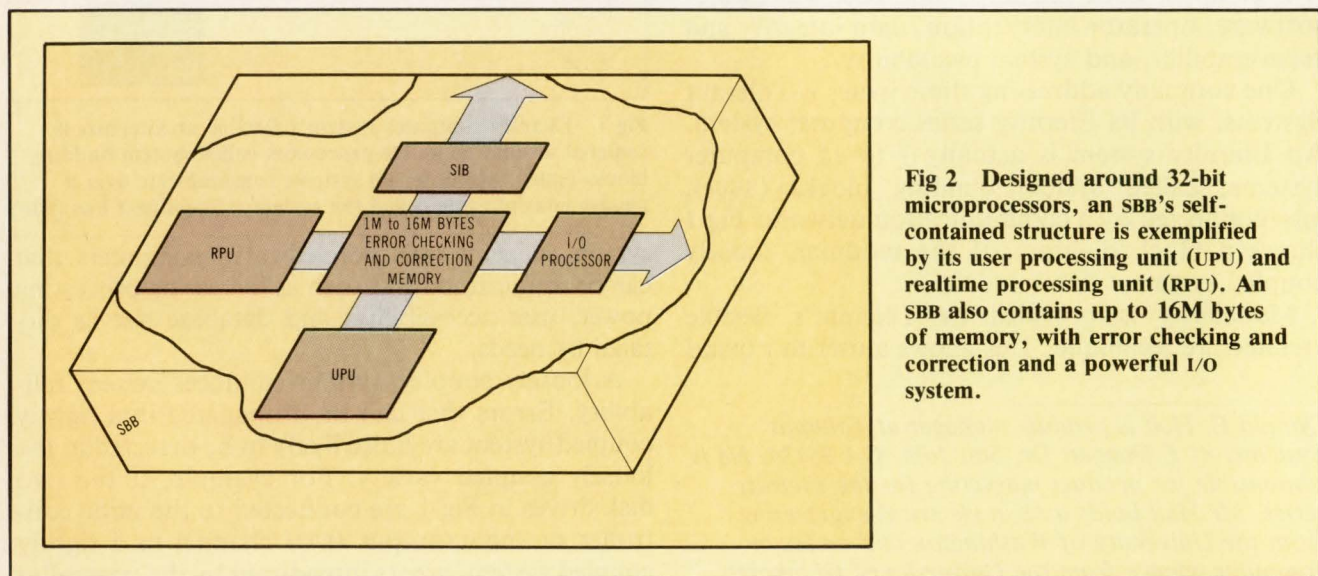
components are identified and isolated from the system through hardware techniques, this is just one facet of the problem. Transactions must still be “backed out” of the system and reconstructed by another system resource. And data bases must be duplicated and kept consistent despite power outages and other system crashes. Operator inputs must be checked to reduce or eliminate erroneous inputs and data accesses must be restricted to authorized data bases or memory space. Hardware fault detection does not address any of these problems, nor guarantee alternate data paths. Thus, it cannot be considered a total solution to fault tolerance.

### *Errors propagated in a tightly coupled system are more likely to be detected in a loosely coupled variety.*

The Eternity system has many fault tolerance problem solving features: fault detection, logical isolation of the fault, and rapid reporting of its occurrence; an architecture that does not propagate system errors; multiple data paths to ensure alternate data flow; and “backing out” of transactions and their restoration on another processor. It also offers distribution of transaction loads from failed processors among the remaining system resources; replication of data files and their distribution to ensure against data loss due to head crashes, vandalism, or environmental disasters; and transparent restoration of repaired system resources (system users are unaware that a problem has occurred).

### An overview of Eternity

Any SBB within the system can both perform and devote its processing power to one or more basic distributed system tasks: application processing, file serving, or communication serving. Moreover,



**Fig 2** Designed around 32-bit microprocessors, an SBB's self-contained structure is exemplified by its user processing unit (UPU) and realtime processing unit (RPU). An SBB also contains up to 16M bytes of memory, with error checking and correction and a powerful I/O system.

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any SBB's functionality can be dynamically redefined for system tuning or expansion. For example, a system with heavy file I/O traffic can be tuned for optimal performance by changing the functional balance of its SBBs from application processing to file serving. If more processing capacity is required, one or more SBBs may be added while the rest of the system remains online and productive.

An SBB contains two 32-bit processors, each dedicated to a separate task. One handles a real-time interrupt-oriented task while the second is devoted to the user's application. Since each task has its own special needs, each is serviced by a different operating system. A realtime executive is used for interrupt service and I/O management. A Bell Labs Unix-compatible operating system manages user process-oriented tasks.

Communication interface processors (CIPs) attached to an SBB's I/O channels meet data communication needs. Transaction throughput is increased by offloading the system's data communication and networking software into the CIP, which performs frontend data communication processing.

The system supports most computer industry protocol standards. This allows the system to coexist with existing host computers and peripherals. Standard high level language compilers allow many currently written, debugged programs to run in a fault tolerant environment with few, if any, changes.

Fig 2 is an SBB block diagram. The unit contains five major modules distributed over four boards: the user processing unit (UPU), internal memory, a realtime processing unit (RPU), I/O channels, and system interconnect buses (SIBs). A 64-bit wide memory bus serves as the highway between all processing elements. This allows all system resources to access memory without waiting for another data transfer to complete. The bus has a 14-MHz sustained bandwidth and is capable of 40M-byte/s direct memory access (DMA) transfers.

### Dedicated internal processors

Both the UPU and RPU are based on National Semiconductor's NS32032 32-bit microprocessor. The first commercially available, true 32-bit processor, the device has both a 32-bit internal architecture and a 32-bit external data bus. The UPU uses National's very large scale integration memory management unit (MMU), the NS16082, to translate logical addresses generated by the NS32032 into physical memory addresses. Read/write memory page protection, provided by the MMU, enhances the system's fault tolerance.

During program execution, the MMU aborts the processor to load a nonmemory resident page and immediately retry the same instruction. In short, the MMU provides complete memory management.

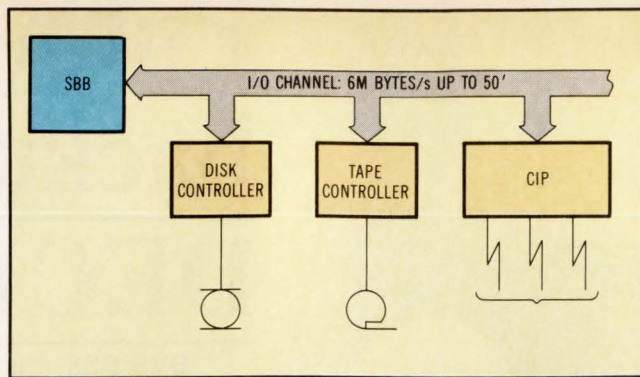


Fig 3 Since online transaction processing depends heavily on I/O communications, the Eternity system provides high speed I/O channels—6M bytes/s—by which disk, tape, and communication controllers are attached to the system.

An 8K-byte cache memory in the UPU makes memory accesses more efficient; that is, it uses block accesses rather than random accesses. To round out the UPU hardware, a National NS16081 floating point unit supports technical environments and Fortran application programs.

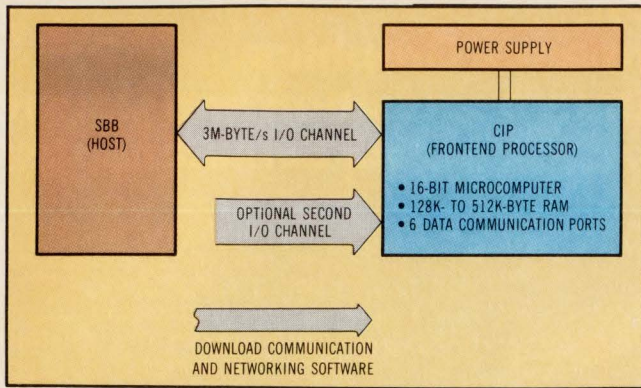
Online transaction processing (OLTP) system response needs often dictate that frequently accessed data remain in memory for rapid access. Thus, OLTPs require a large, physical resident memory. Each SBB contains 1M to 16M bytes of memory, including error checking and correction (ECC) circuitry. The ECC permits single-bit error correction and double-bit error detection.

Operating under its own realtime executive, the RPU serves the system's realtime processing activities. In addition, the RPU coordinates communication between SBBs and performs ongoing system diagnostics. Diagnostics constantly occur in the background of user application programs and are reported via a diagnostic port on the RPU.

To access files, OLTP environments require a powerful I/O system. SBB I/O channels allow attached controllers to communicate with user memory through byte random access, or more efficient block-multiplexed DMA transfers. Both of the SBB's 16-bit wide I/O channels have bandwidths of 3M bytes/s and can operate at distances up to 50'. Up to 15 controllers can be attached to each I/O channel. The I/O architecture (Fig 3) produces a system able to accommodate large file I/O and/or data communication requirements.

SIBs interconnect the system's SBBs. An SIB is a dual-coaxial cable that uses passive ac-isolated connections. This ensures that the addition or removal of an SBB will not break the communication paths to other SBBs. Both SIB channels perform productive work by independently transferring information. In the event of a failure, the remaining SIB picks up the full work load. SIBs can be separated by up to 2.5 km, enhancing the system's immunity to environmental failures and accommodating the distribution of the local user community. Total SIB





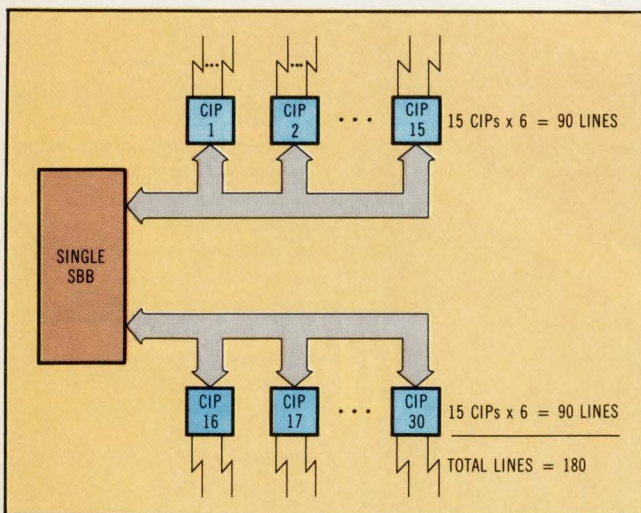
**Fig 4** The communication interface processor (CIP) in Fig 3 handles frontend communications for its SBB, thereby reducing the processor's overhead. CIPs maintain dual communication interfaces—with two SBBs. If one SBB fails, a user's data path switches over to the working SBB.

bandwidth allows a system to be composed of 15 SBBs, with a distributed performance of 22.5 million instructions per second (MIPS).

### Flexibility through communications

The intelligent communication controller (CIP) shown in Fig 4 is attached to Eternity's I/O channels. This frontend communication processor off-loads most SBB data communication tasks and overhead. A CIP contains sufficient memory—up to 512K bytes of random access memory and 32K bytes of read only memory—to operate in a multi-protocol environment. It also has the processing power to handle six I/O lines at a transfer rate up to 56K bytes/s.

Each CIP contains its own power supply and two I/O channel interfaces. If a power supply fails, its impact only extends to the six lines served by that CIP; lines to other CIPs are unaffected. Dual-I/O channel interfaces allow a CIP to communicate with two I/O channels (SBBs) simultaneously. If either an SBB or an I/O channel fails, the user does not lose



**Fig 5** Data communication is handled on a modular basis. An SBB can support 30 CIPs, each of which provides six I/O lines. Thus, a single SBB may control 180 I/O lines.

the physical data path. System software takes over to maintain the integrity of all potentially impacted user sessions and input data. If a user requires continuous availability at the CIP level, two CIPs can be configured as a redundant system to ensure availability all the way to the user's terminals.

The six serial ports served by a CIP can be defined dynamically as asynchronous, bit synchronous, or byte synchronous. This flexibility provides the ideal environment to support the majority of data communication protocols in use. A CIP also supports hardcopy requirements by allowing one port to be configured as a Centronics parallel interface. Another CIP operates in accordance with the IEEE 488 to meet the needs of the industrial and instrumentation markets. All CIP interfaces are supported in a realtime manner.

Adding CIPs modularly expands data communication service to serve many lines and protocols. Each I/O channel can support up to 15 CIPs or 90 lines. An Eternity system with 15 SBBs will support well over 2500 active lines. Fig 5 is a block diagram of the data communication architecture.

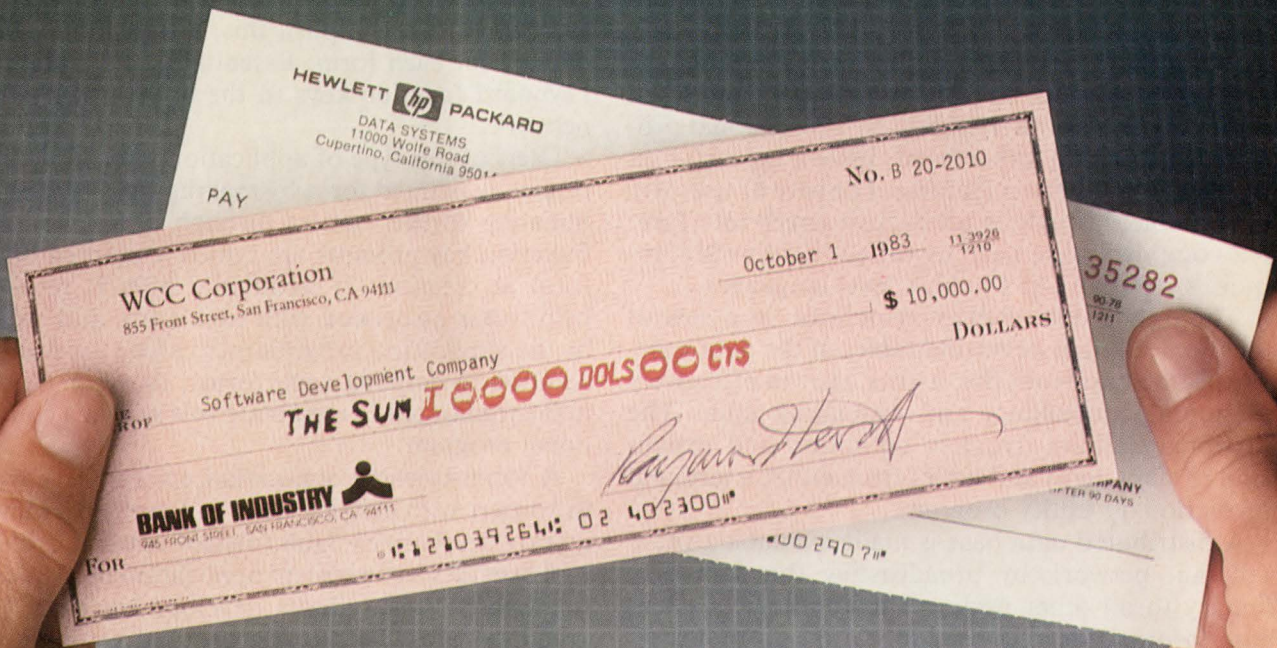
An Eternity system can handle three compatible types of storage module drive (SMD) disk systems, each with different storage capacities: 84M, 165M, and 474M bytes. The drives can operate at 20-ms average access times and at 1.2M to 1.8M-byte/s transfer rates. The system supports one or more 1600 bpi tape units running at 25 ips in start/stop mode, or 100 ips in streaming mode.

### Software tackles hard tasks

To support commercial online applications, Eternity's integrated system software package contains a file system, an integrated operating system with transaction processing, a relational database management system, application development, distributed processing, system utilities, and data communications/networking. The system's Eternal operating system stems from Bell Labs' Unix. Its internal code, however, has been adapted for commercial fault tolerant transaction processing. The external application programming interface remains intact and is compatible with the Berkeley version 4.1 call interface. This is a nonproprietary interface that allows many off-the-shelf applications to immediately run on the system. Unlike conventional transaction processing software, Eternal offers fully integrated transaction management—it does not require an additional transaction management system.

The file system handles logical n-plexing of files. This allows a user to replicate a file or files from one disk onto any number of other disks in the system. The file system also provides protection from media and environmental failures—head crashes, fires, sprinkler system failures, etc—and permits higher system throughput through the





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load balancing of database accesses to the multiple file copies.

Included in the relational database management system are a full set of user interface components: the SQL query language, a data dictionary, a report writer, and an application development facility. SQL is a high level relational database access language developed by IBM to allow queries, data manipulation, and data definition. The language permits nonspecialists to be casual users and learn only the simplest query features. Professional programmers, on the other hand, have a powerful set of data manipulation features. For ease of use, SQL is available through an interactive screen interface. All compilers have been modified to allow SQL inquiries from any of the high level languages.

The online data dictionary defines, in a central location, all data items and tables in the data base. This is the basic tool that assists users in effectively planning, controlling, and evaluating data. The dictionary allows dynamic definition and expansion of data items and tables from either a terminal or dictionary utility program.

A distributed data base is made available over a Tolerant network by broadcasting the data dictionary to all other nodes. This topological database information relieves application programs of that responsibility. Such an operating system service allows applications to be written and distributed throughout the network, with the knowledge that the Eternal operating system can locate all the required data.

In addition to text formatting, the report writer offers SQL query capabilities. Thus, a user can produce reports that combine information from the data base with textual information, such as headings, explanatory text, and other material. The report writer can derive reports from a single table or from any combination of tables through an SQL query.

Since business-oriented application programs have traditionally been developed in Cobol, Fortran, Basic, or PL-1, compilers are provided for each of these high level languages. These compilers enhance their standard instruction sets with the SQL set. Thus, application programs written in these languages can efficiently access files in Eternity's optional relational database management system. Moreover, Eternity can supply Pascal and C compilers with the same capabilities.

To aid development of fault tolerant OLTP applications, the system provides a set of interactive application development facilities. Using the facilities, a programmer can link with other forms or program segments to interact with the relational data base or with conventional files. Application design is a simple task. A programmer first "paints" the form by moving a cursor and entering the text and/or field designators. Then the system

queries the programmer—via split screen—for the attributes of each field (menus simplify the process). A programmer can specify video attributes, data types, validation criteria, default values, and formatting. The system supplies defaults for each.

Once defined, forms can be linked to one another or to programs, as in a tree or network structure. To accomplish this, a transition table is defined for each form. Essentially, the table maps keyboard function keys to the links in the tree or network.

Users of this type of application interact with the originally painted form by making field entries and initiating further action through a function key. Function key prompts are typically painted onto a form at creation. If additional help is required, help forms associated with each form and created by the application programmer can be accessed. In addition to defining such forms, they can be used in the traditional I/O template role within a conventional program.

A forms-oriented application environment works in concert with existing data and user programs to quickly develop new fault tolerant applications. The tool provides a convenient application implementation vehicle that reduces development time, programmer errors, and operator input errors during execution.

---

### *Faults in a computer system are not necessarily hardware malfunctions.*

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A single, heavily accessed data base often creates a bottleneck in a multi-user environment. If an application requires access to an n-plexed file, the Eternal operating system routes the request to the least accessed copy. Such load balancing promotes higher transaction throughput. Tasks are load balanced across the system by dynamically associating a process serving the needs of a terminal with a specific server process. An intermediary (the dispatcher) receives and queues requests from many terminal processes. As a server process becomes available—there may be many identical copies—it queries the dispatcher for work. Terminal and server processes can be distributed over many SBBs on the same system, or over many networked systems. This logical type of association is not bound by physical limitations.

Utilities permit the system to be dynamically reconfigured and the resulting performance to be monitored. System administrators can fine tune their system for maximum performance. Moreover, other utilities exist for managing the file system, spooling subsystem, and users.

The system's data communication environment embraces both the protocol-specific code running in the CIPs and the SBB functioning, in part, as a

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communication server. The CIPs resources can handle requirements of multiple data communication protocols. These are downloaded from an SBB when needed. The standard protocols supported are the Async (point-to-point and multipoint), X.25, SNA 3274/3276, Bisync 3274, and Bisync 2780/3780 protocols. Users who require nonstandard protocols can write their own in C to run under the realtime executive on the CIP.

Terminals with a variety of physical characteristics can be simultaneously connected to the system. Traditionally, the application program handled these characteristics. Eternity solves the problem with a virtual terminal that presents a single type, global view of terminal characteristics to the application program. This substantially aids application development by relieving the application programmer of the burden of compensating for different terminals in the program.

An additional protocol—the tolerant network protocol—allows geographically distributed Eternity systems connected directly, or by a global network, to function logically as one system. Requests for local data are routed to other local file server SBBs via the SIBs. Requests for data on a remote tolerant system are translated into the tolerant network protocol and routed—via a CIP and perhaps an intervening network—to the destination system. Flow control and routing are provided if all network nodes are tolerant systems. A log-in request to an outside global network precedes the initial data request if two or more tolerant systems are connected by a foreign network.

### Handling OLTP system faults

Faults in a computer system are not necessarily hardware malfunctions. Often, incorrect use of application software and systems is a greater contributor to system unreliability. Eternity systems use a number of techniques (hardware, software and architectural) to detect, correct, and recover from such failures.

Each SBB isolates errors through combined hardware and software checks. At the lowest level, all memories and data paths are protected by ECC circuitry. Watchdog timers on the UPU and RPU prevent system software or application programs from going into infinite loops. The MMU provides read/write protection at the page level. Central processing unit (CPU) traps detect errors such as dividing by zero. The Eternal operating system provides so-called sanity checks—the validity of pointers. Also, diagnostic tests run continuously as background tasks. Thus, all hardware elements in the SBBs and attached I/O resources are exercised. Fig 6 shows a hierarchical view of the system's fault detection architecture.

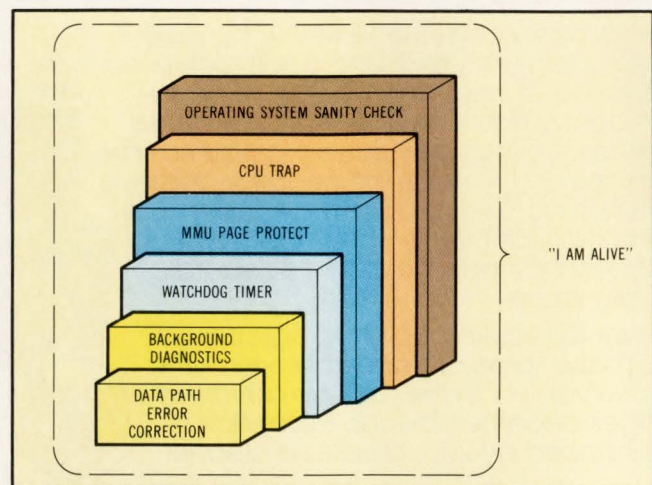
A failure in any of the preceding categories causes the faulty resource to be isolated from the

system. If the fault is within an SBB, communication with other SBBs will be incoherent or cease. Timeouts in other SBBs will initiate action to logically isolate the faulty SBB. Incoherent communication with other SBBs is often detected by the faulty SBB, since each SBB will listen to its own system transmissions.

When a fault is detected and isolated, a call goes out to a repair center to report the fault. Faults are further indicated by onboard fault indicator lights. There can be a case in which a faulty SBB cannot report its condition (eg, its power supply is inoperative). In this case, another SBB in the system must initiate the call.

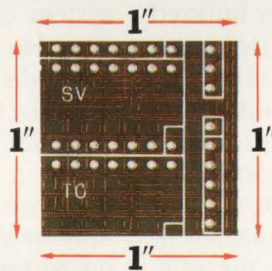
Alternate multiple data paths are guaranteed through a variety of resources: dual-system interconnect buses, replicated distributed system functionality (multiple SBBs across a system acting as application processors, file servers, and communication servers) replicated files, and dual-ported CIPs. Restoring the transaction and ensuring data base consistency then become the operating system's responsibility.

The operating system provides a fault tolerant environment by implementing a number of application-transparent facilities. Such facilities were not provided by earlier systems. Traditionally, the recovery and integrity mechanisms used to protect disk-based data from hardware or software failures were inside the file or database system and/or partially at the application level. These techniques used recovery logs built atop the basic file-access method and/or checkpoint calls in the application. The system provided calls only if proprietary, non-standard application development tools were used. The relatively high level implementation of these mechanisms introduced significant performance overhead and still did not guarantee recovery at all times.



**Fig 6** System faults are detected and isolated through combined hardware and software checks. If faults are detected by this hierarchy of test procedures, the malfunctioning device is quickly isolated from the system.

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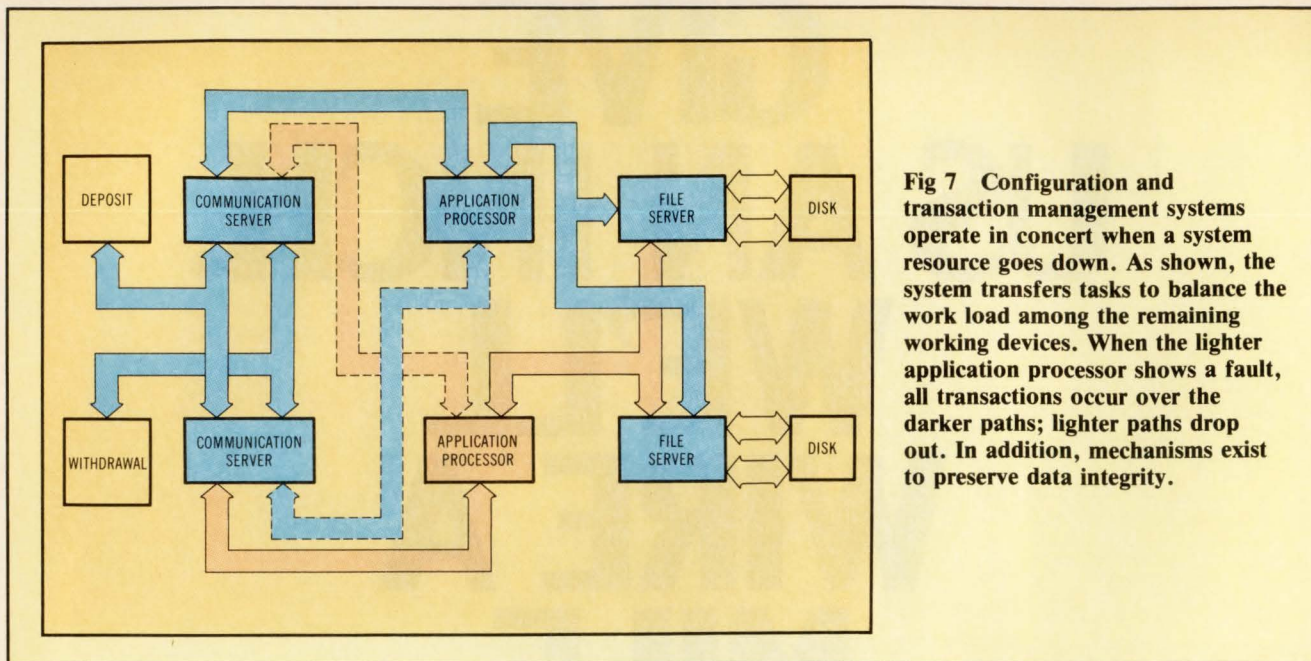
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**Fig 7 Configuration and transaction management systems operate in concert when a system resource goes down. As shown, the system transfers tasks to balance the work load among the remaining working devices. When the lighter application processor shows a fault, all transactions occur over the darker paths; lighter paths drop out. In addition, mechanisms exist to preserve data integrity.**

Eternal provides application-transparent recovery and integrity mechanisms at a low level in the file system. This yields a performance-oriented system in which any disk-based data (sequential or indexed files, relational data bases, or system dictionaries) can be protected from failure by the underlying "before image" and rollback/restart facilities.

To preserve a transaction's process context across a failure, several functional areas in the operating system work together to save the relevant state at the beginning of each transaction. The management I/O function is responsible for recording the existence and state of all I/O links belonging to the process. The memory management and process management functions are responsible for saving the state of the typically few process pages "dirtied" since the last "begin transaction" point. This is fast and occurs at the least critical time: between transactions as perceived by the user.

If a failure occurs, configuration management and transaction management work together to re-establish the process on the system's other SBBs in a load-balanced fashion. Fig 7 shows how the system provides continuous availability and data integrity. The new processes are initialized to the current transaction's "begin" point using the saved-state information. Transaction management then tells low level file recovery which transactions should be "rolled back." With the disk data restored to the "begin transaction" state, the transaction is re-executed using the terminal input log.

Users can configure the fault tolerance level with SBB's ability to provide different types of functionality. This ensures affordable, continuous service availability. A single SBB provides a powerful, standalone, minimum fault tolerant system by providing data integrity through the ECC feature and duplication of files/data bases. These features

permit complete recovery and restoration of the data bases to a consistent state following resolution of a problem. A minimum, continuously available system contains two SBBs, each configured as a complete system. This allows the support of mirrored disks on each SBB so that the loss of one will not take the data offline. Such a configuration also provides twice the power of a single SBB system.

For a system to be online at all times, rapid response to service needs is critical. This process may be expedited by the computer reporting diagnosed faults and the user repairing them.

Using background diagnostics, the RPU constantly monitors all resources. If a fault is detected, the RPU logically isolates its SBB by not informing other SBBs of its availability. It then notifies a service center by auto-dialing through a 2-way diagnostic port. If a technician needs additional help with the problem, the system's remote diagnostics may be run.

Eternity is designed for users to handle most repairs. Each of the four SBB boards has indicator lights and is easily removed. Power supplies are on easily removed slide-mounted, plug-in modules. Repairs can be accomplished while the rest of the system remains online.

After a faulty board is replaced, the system runs a test to verify the newly repaired module's integrity. The module will then reconfigure itself into the system without operator intervention.

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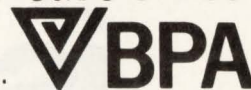
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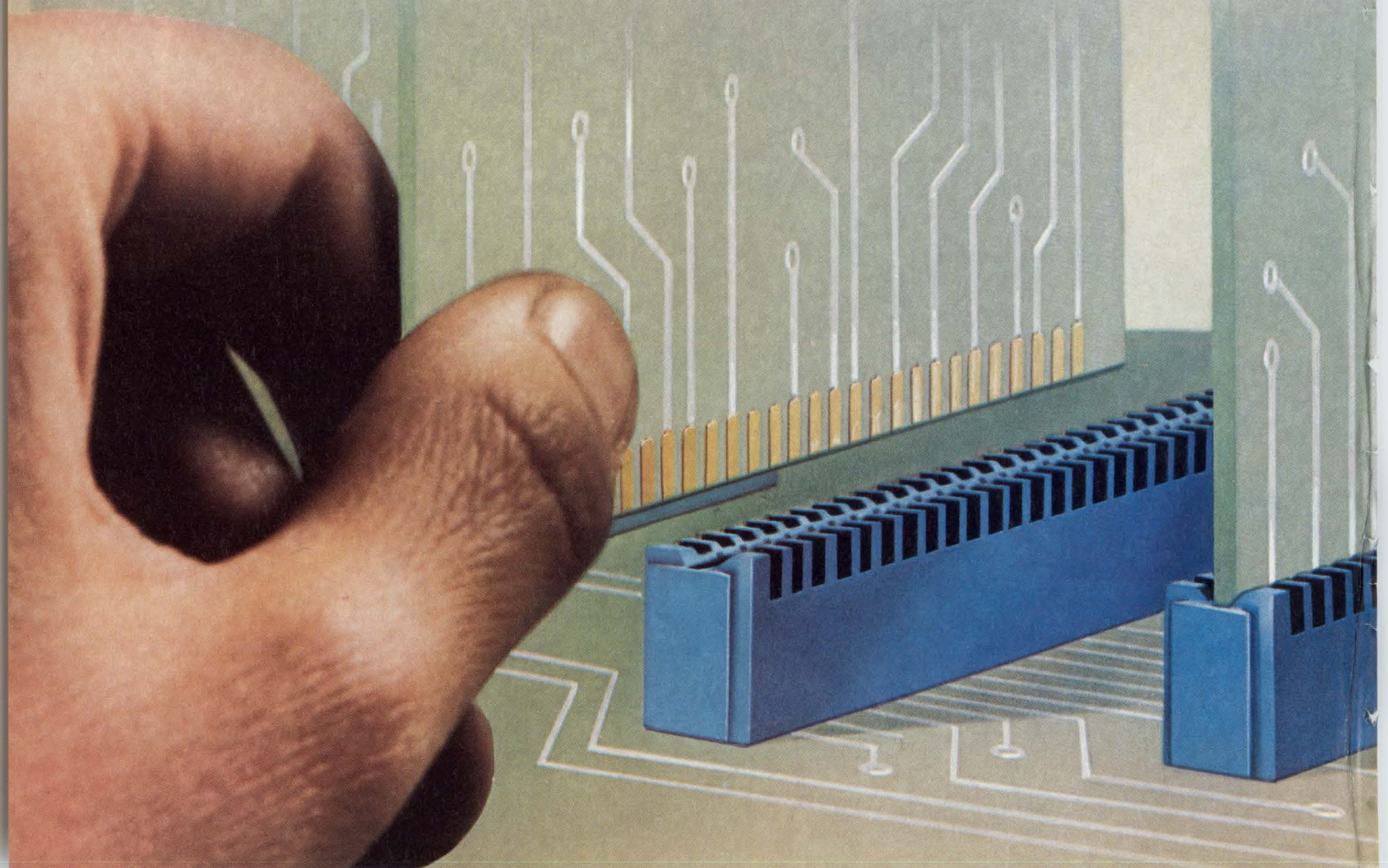
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**Contact Rating:** 3 Amp

**Contact Resistance:** Spring contact to test board—8 milliohms

Total circuit resistance—9 milliohms

**Operating Temperature:** -55°C to +85°C

**Voltage Rating (Sea Level):** .100" centerline spacing—1000 VAC

**Insulation Resistance:** 5,000 Megohms

**Durability:** 100 cycles

**Salt Spray:** MIL-STD-1344, Method 1001

**Thermal Shock:** MIL-STD-1344, Method 1003

**Physical Shock:** MIL-STD-1344, Method 2004

**Humidity:** MIL-STD-1344, Method 1002, Type II

**Vibration:** MIL-STD-1344, Method 2005

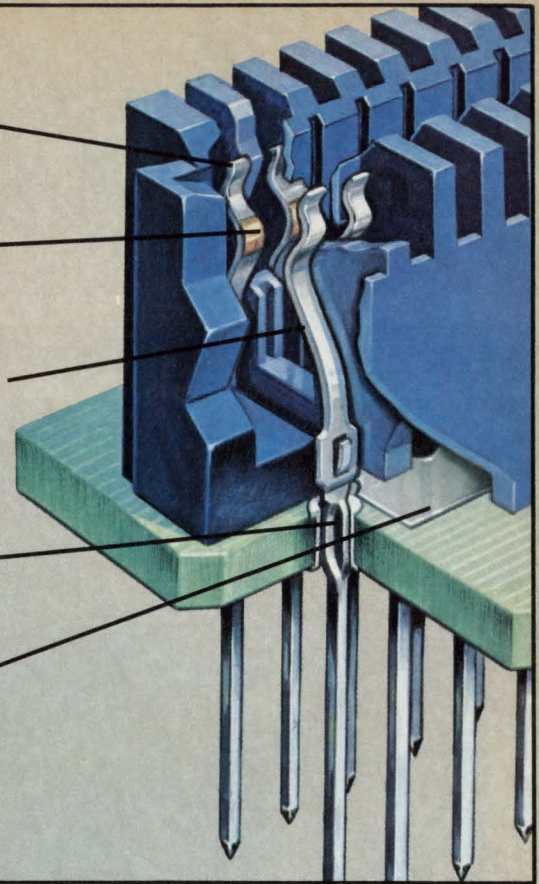
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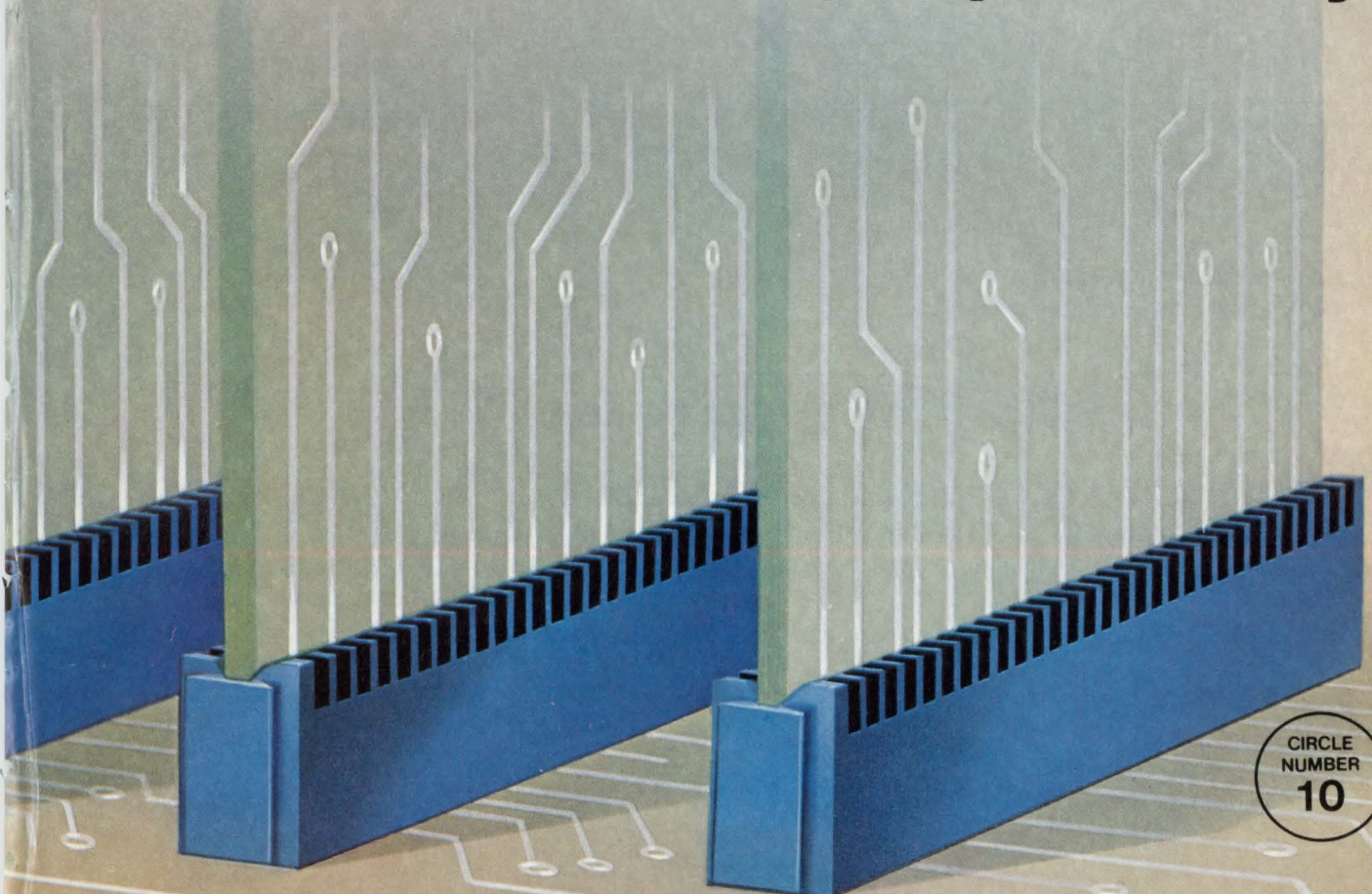


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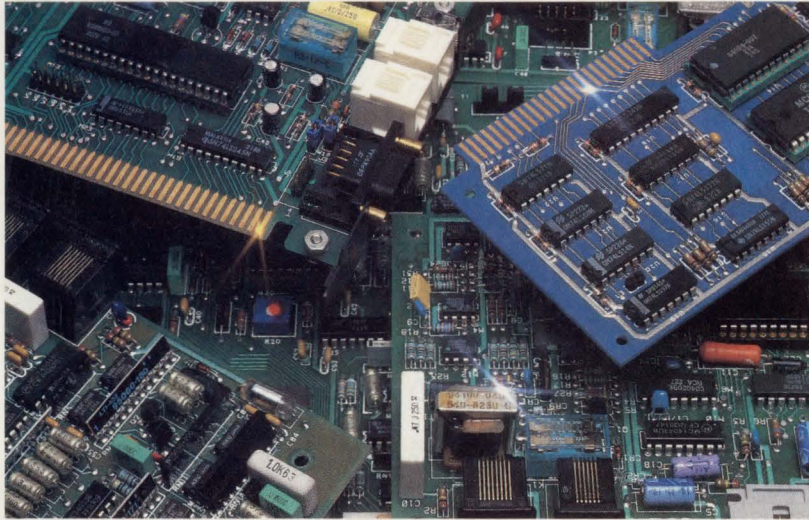
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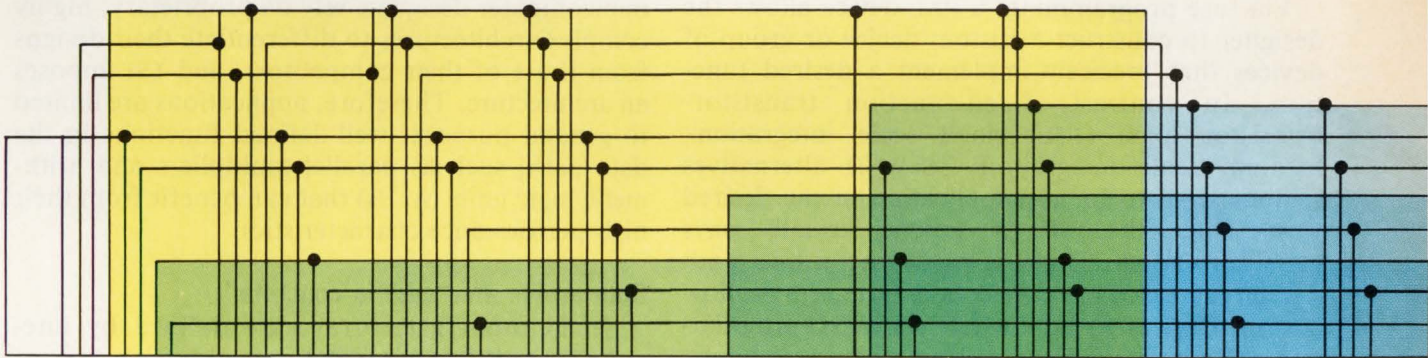
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# LOGICAL ALTERNATIVES IN SUPERMINI DESIGN

**Becoming the technology of choice in superminicomputer design, programmable array logic mixes with alternative devices to meet design constraints.**



by **Bradford S. Kitson and  
B. Joshua Rosen**

Programmable array logic devices have been a driving force behind the latest generation of 32-bit superminicomputer designs. These superminicomputers range from redesigns of existing architectures that reduce cost or overcome packaging limitations, to designs requiring ultrafast turn-around, to high performance architectures specified to take full advantage of such devices.

Superminicomputers designed with programmable array logic (PAL<sup>®</sup>) include the VAX<sup>®</sup>-11/730

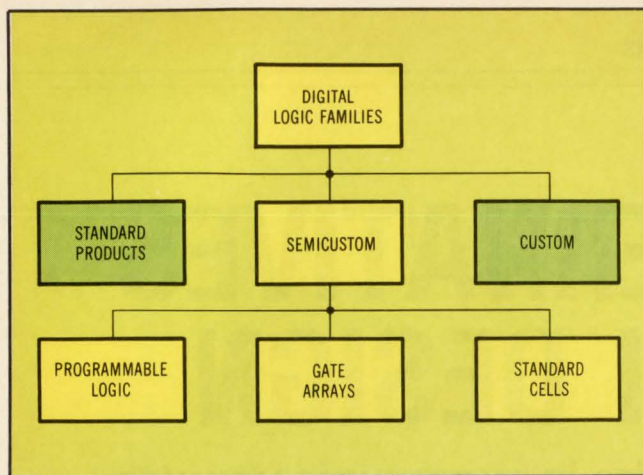
*Bradford S. Kitson is section manager in product planning and applications for programmable logic devices at Advanced Micro Devices, 901 Thompson Pl, Sunnyvale, CA 94088. He holds a BS in electrical engineering and computer science from the University of California at Berkeley.*

*B. Joshua Rosen is manager of processor design at Dataflow Systems Corp, 42 Nagog Park, Acton, MA 01720. He was manager of processor development at Computervision Corp, Bedford, MA, when this article was written. He holds a BA in physics from Lawrence University and an MSEE from Northwestern University.*

from Digital Equipment Corp, the MV/8000 and MV/10000 from Data General, and Computervision's APU<sup>®</sup> (analytic processing unit). A reimplementa-tion of the original VAX-11/780, the VAX-11/730 sup-plies 25% of the performance in 10% of the board space. Programmable array logic was chosen by the MV/8000 designers to allow the shortest possible design cycle and to catch up with their competitors. The MV/10000 upgrades performance of the MV/8000. The Computervision APU was designed for high performance with PAL devices in mind, and provides excellent examples of how to use such devices to their fullest.

## Logic design alternatives

Although by no means the only option, pro-grammable array logic has become the technology of choice in superminicomputer design. Logic design alternatives (Fig 1) include standard prod-ucts (fixed-function devices), semi-custom (programmable logic, gate arrays, and standard cells), and fully-custom logic devices. In supermini-computer design, the primary alternatives are stan-dard products, gate arrays, and PAL devices. The best choice for any given function depends upon the design alternative capabilities, the design con-straints, and the function actually being im-plemented.



**Fig 1 Basic categories of digital logic present designers with trade-off opportunities. Standard products fit where cost is a major concern; custom and semi-custom products can be used where high diversity is desirable.**

Via fuse programming, a PAL device allows the designer to construct a custom device or group of devices that precisely implement a desired function. In contrast, fixed-function transistor-transistor logic (TTL) small scale integration/medium scale integration (SSI/MSI) alternatives seldom seem to fit any application in the desired way. Thus, the SSI/MSI designer usually pays penalties via extra logic levels in the critical path and an increased package count. Gate arrays allow custom devices to be created via mask programming. However, designers using a gate array must finalize architecture early in the design cycle. Any errors will require a mask change, which can take months.

In most cases, the best choice is a combination of the alternatives and probably includes some memory as well. Typically, the six basic design constraints are performance (speed), cost, density (packaging), power dissipation, reliability, and design turnaround. Assigning a priority to these constraints will usually define the logic alternative that a machine is based on. Actual implementation trade-offs are made at the function level. The three basic functional portions of a design are data path, control path, and interface.

### Standard products have their place

Standard products are defined as devices created for a wide market. Examples of standard products are TTL SSI/MSI, fixed instruction set metal oxide semiconductor (MOS) microprocessors, and micro-programmable large scale integration (LSI) building blocks. These devices are usually multiple sourced and produced in high volume, resulting in lower individual device costs. In a design where cost is the main concern, and performance, power dissipation, density, and design turnaround are of little or no importance, standard products are probably the best choice. In a design such as a superminicom-

puter, where these other considerations have a high priority, inherent disadvantages limit standard product use.

While SSI/MSI devices offer fast individual gates, on a system level their density, power dissipation, and reliability characteristics are not as good as those of the alternatives. In addition, design turnaround characteristics are inadequate because changes usually require printed circuit (PC) boards to be laid out again. In most superminicomputers, therefore, SSI/MSI gates are used only in selected critical path functions that require one or two gate levels (at the expense of density and power dissipation), and in interface applications, such as bus buffers, latches, registers, and transceivers.

Standard LSI products (mostly bipolar) offer exceptional performance, power dissipation, density, and reliability characteristics, but their inflexible architectures limit their application range. Superminicomputer designers rely on proprietary, highly complex architectures to differentiate their designs from those of their competitors, and LSI imposes an architecture. Therefore, applications are limited to general purpose, well-defined functions in the data path, such as parallel multipliers and arithmetic logic units (ALUS) that can benefit from their high performance characteristics.

### Gate arrays are "cast in concrete"

Semi-custom gate arrays are defined by integrated circuit (IC) manufacturers as large arrays of unconnected gates. End users specify how gates are interconnected with actual interconnection occurring at the metal-mask layer of the IC process. The main advantages of gate arrays are high density and the ability to customize a design, while primary disadvantages are cost and design turnaround. Each custom device is single sourced and low volume; therefore they are not cost-effective unless the application is density limited or the volume is very high. Gate arrays can adversely affect design turnaround because the system designer must design both the IC and the system in which the IC is used. In addition, any change in the gate array requires new masks and a delay for each mask iteration.

By using gate arrays only where the design can be defined early, designers minimize these turnaround disadvantages. They then hedge their bets by surrounding the gate arrays with logic that can correct any design bug(s) discovered later on. As in LSI, what is "cast in concrete" is usually the data path. However, gate arrays allow more of the data path to be integrated because the device can be optimized for specific design requirements. A proprietary 16-bit ALU slice might be a typical gate array.

Gate arrays are also used to interface multiple onboard buses together as data path "glue." Control-path and interface applications, however, tend to be too likely to change. Therefore, control

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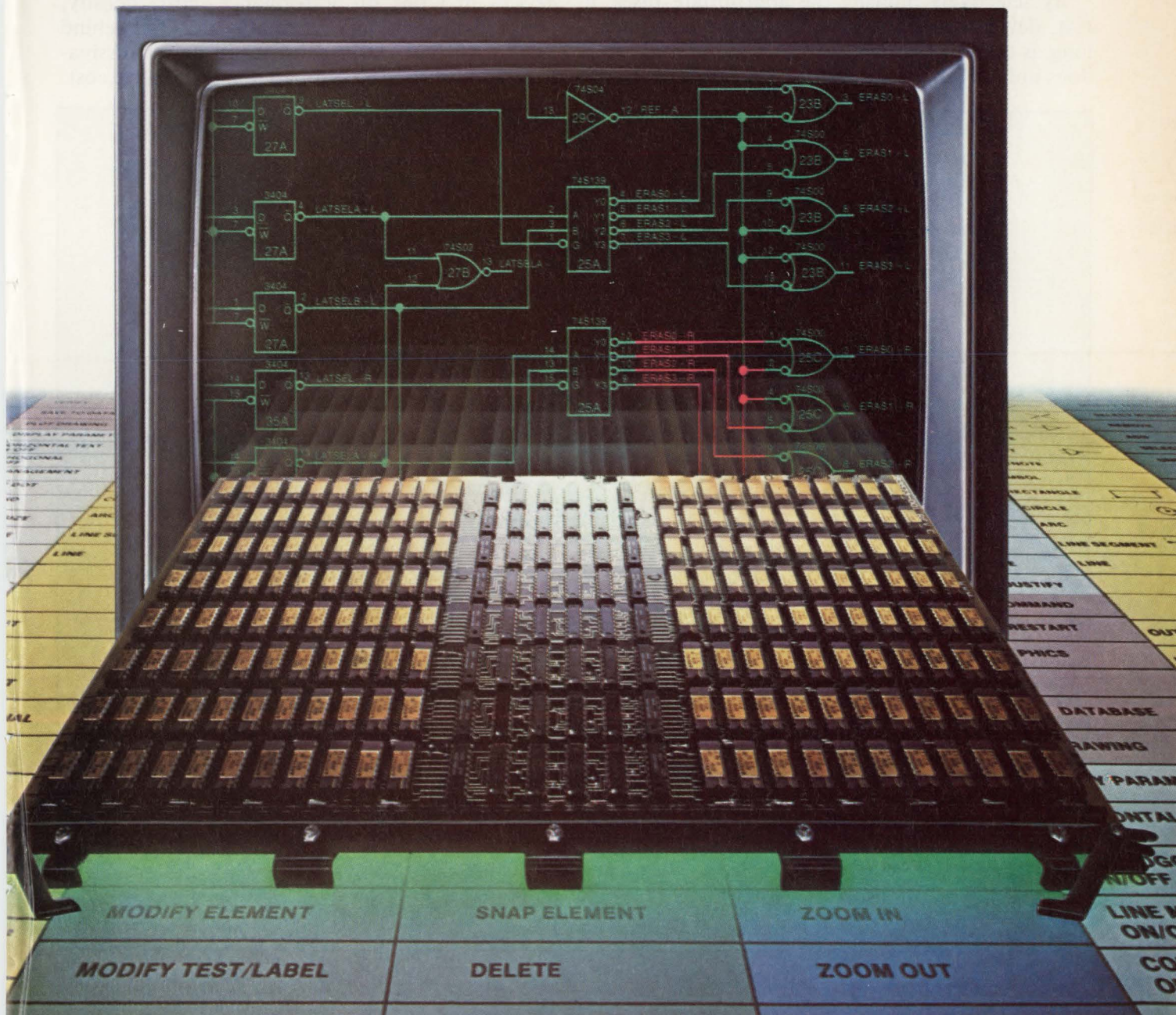
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path functions are based on implementation techniques such as writable-control-store (WCS). Interface applications frequently require changes because of the need to interface one designer's board to another's. Consider the critical timing between a cache, an instruction fetching unit, and multiple register-files. The exception handling capability required for typical operations, such as a cache miss, can be an indeterminant problem affecting all of the above-mentioned functional units in the system. Should a bug occur in the cache unit, the interface section of all other units will have to be changed to accommodate the correction.

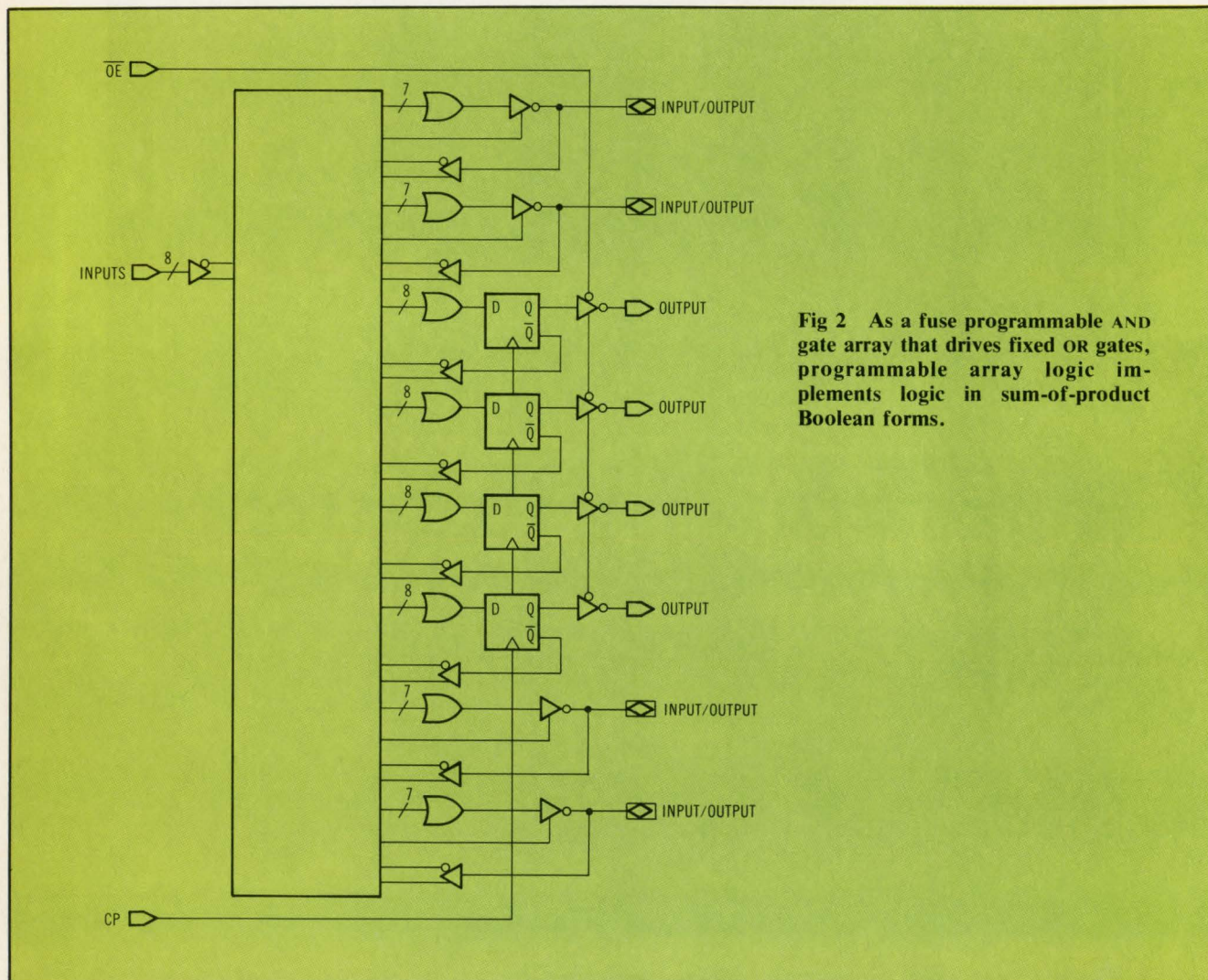
### PAL structure paves the data path

Combining simplicity and flexibility, the basic PAL structure is a fuse-programmable AND gate array that drives fixed connection OR gates, allowing logic to be implemented in sum-of-products (AND-OR) Boolean form.

By selectively blowing the appropriate fuses, a PAL device can implement any logic function as long as the number of inputs or AND gates required does not exceed the number provided in the device

chosen. In the AmpAL16R4, for example, the true and complement version of each of the 16 inputs is connected via fuses to each of the 64 AND gates in the device (Fig 2). PAL devices provide additional features, such as programmable input/output (I/O) pins and registered outputs with internal feedback that further enhance their ability to implement logic functions efficiently. Programmable I/Os are especially useful for trading off the number of device outputs for inputs to fit the exact number required by the logic functions being implemented. Internal registered feedback is desirable when implementing complex state machine designs.

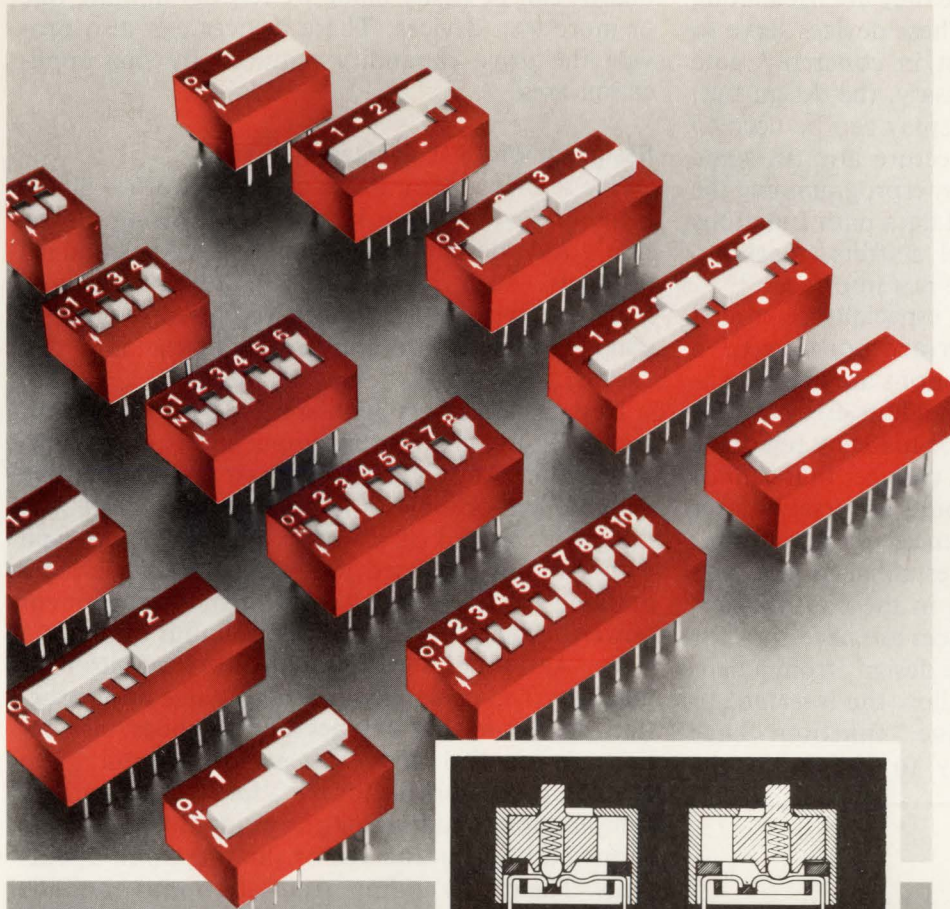
Programmable logic devices, like gate array, are semi-custom devices. Created by the IC manufacturer, they are alterable by fuse programming for a specific application. Designed specifically for logic-oriented applications, PAL devices enable designers to create custom devices with fast turnaround time. PAL devices compare favorably to alternative devices in terms of performance, cost, density, power dissipation, and reliability. They fall behind gate arrays and LSI in density and power dissipation, and behind SSI/MSI in individual device cost.



**Fig 2** As a fuse programmable AND gate array that drives fixed OR gates, programmable array logic implements logic in sum-of-product Boolean forms.



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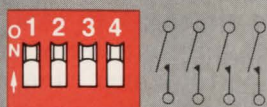
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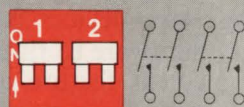
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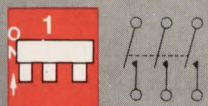


2PST, 1 - 5 stations;

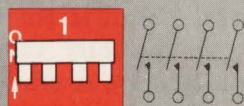
### DOUBLE THROW— Alternating Side "On" Positions



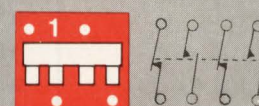
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(Note however, that PAL devices are cheaper on a system basis.)

Performance and density characteristics of PAL devices have led to significant applications in the data paths of superminis where they are used along with LSI and/or gate arrays. These devices serve to "glue" the LSI and the "cast in concrete" gate arrays into the system. If necessary, the design turn around capability that they display can be used to optimize the data path architecture and, in some cases, fix a bug in a gate array by reprogramming the PAL devices around it. Typical data path functions for the devices include barrel shifters, masking, code conversion, and multiple bus interface.

Design turnaround becomes especially beneficial in the control path and interface portions of a design. Most control path functions are highly random and are prone to change and/or error. While WCS allows design changes to be made by rewriting microcode, PAL devices permit changes that cannot be made in microcode, or would adversely affect system performance. For instance, one supermini-computer manufacturer has established the rule that a gate array can be used in the control path only if eight or more PAL devices are necessary for the same function. In interface design, from a density standpoint, PAL devices allow the interface to merge with the data path "glue" function. Since the interface is just as likely to change as the

control path, but without the benefit of WCS, design turnaround becomes a factor. If one board's designer needs to change the interface, the designs of many other boards are impacted. Updates on all boards can be easily made by reprogramming one or more PAL devices. These devices can also provide the drive capability required by this application area.

### Designing with PAL devices in mind

Trade-offs among PAL devices and other digital logic alternatives were key factors in Computervision's APU design. In conjunction with standard products, such as ALUs, LSI multipliers, and memory devices, PAL devices were used to create a patented architecture not feasible in standard TTL SSI/MSI.

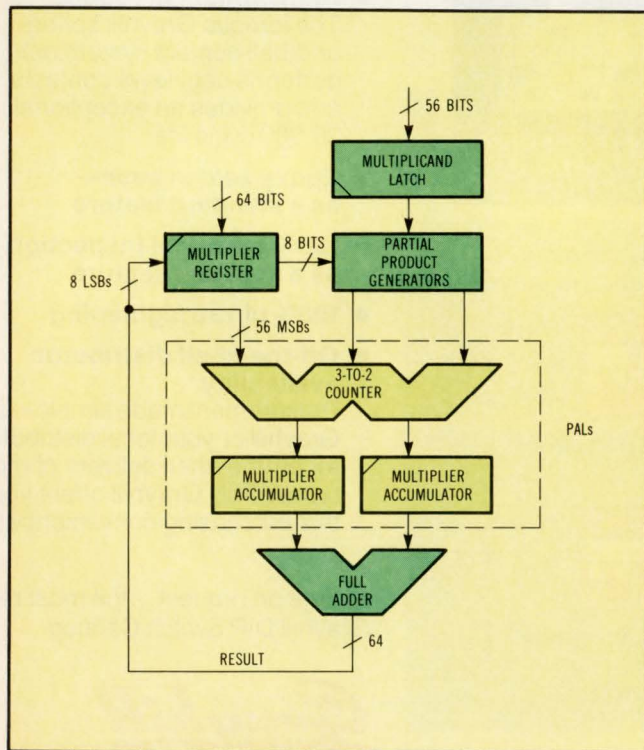
Designed as a very high speed 32-bit supermini-computer for engineering applications, the Computervision APU is twice as fast as competitive designs, yet occupies the same board space. Its designers, instead of merely replacing TTL SSI/MSI with PAL devices, used PAL as customizable logic building blocks. This allowed them to implement powerful logic functions in a minimum of space.

The APU processor board set is divided into four modules. The parser/sequencer contains an instruction processor that fetches and decodes instructions in parallel with the execution unit. The control processor performs address and integer computations and the floating point pipe (FPP) performs both scalar and vector floating point operations. The cache/address translation unit contains a 256-slot area page table entry cache and a 16K-byte memory cache.

Approximately 25% of the chips in the APU board set are in PAL. Since the APU is the first implementation of the new CPU architecture, many design aspects are subject to change as the architecture evolves. PAL devices permit designers to rapidly modify hardware to fit the architecture needs, and to implement feature and performance enhancements with minimal impact on the development schedule.

Ability to generate a very large number of custom ICs (over 200 different PAL codes are used in the APU), significantly reduces the processor's size while increasing overall performance. This means that, although the APU and Digital Equipment Corp's VAX-11/750, a gate array-based machine, consume exactly the same amount of board space, the APU is more than twice as fast. In fact, the APU's Fortran performance is substantially faster than that of the VAX-11/780, a machine that consumes 5.2 times as much board space as the APU.

Designed as a high speed arithmetic extension to the APU execution engine, the APU FPP, unlike comparable machines, is an integral part of the



**Fig 3 Multiplier calculates 56-bit x 56-bit product. Partial product generation logic uses seven 8 x 8 slices to form 8 x 56-bit multiplication array. Carry-save adders implement 3-to-2 counting techniques to form two operands that are summed in a lookahead ALU.**

internal architecture and not an optional add-on. As a result, the FPP not only accelerates scalar and vector floating point arithmetic, but also performs byte, word, double-word, and quad-word string operations. In addition, it serves to enhance the performance of important nonfloating point instructions such as Procedure Call and Return. A total of 79 PAL devices are used for both control- and data-path applications on the FPP board.

### Counter solves multiplication problem

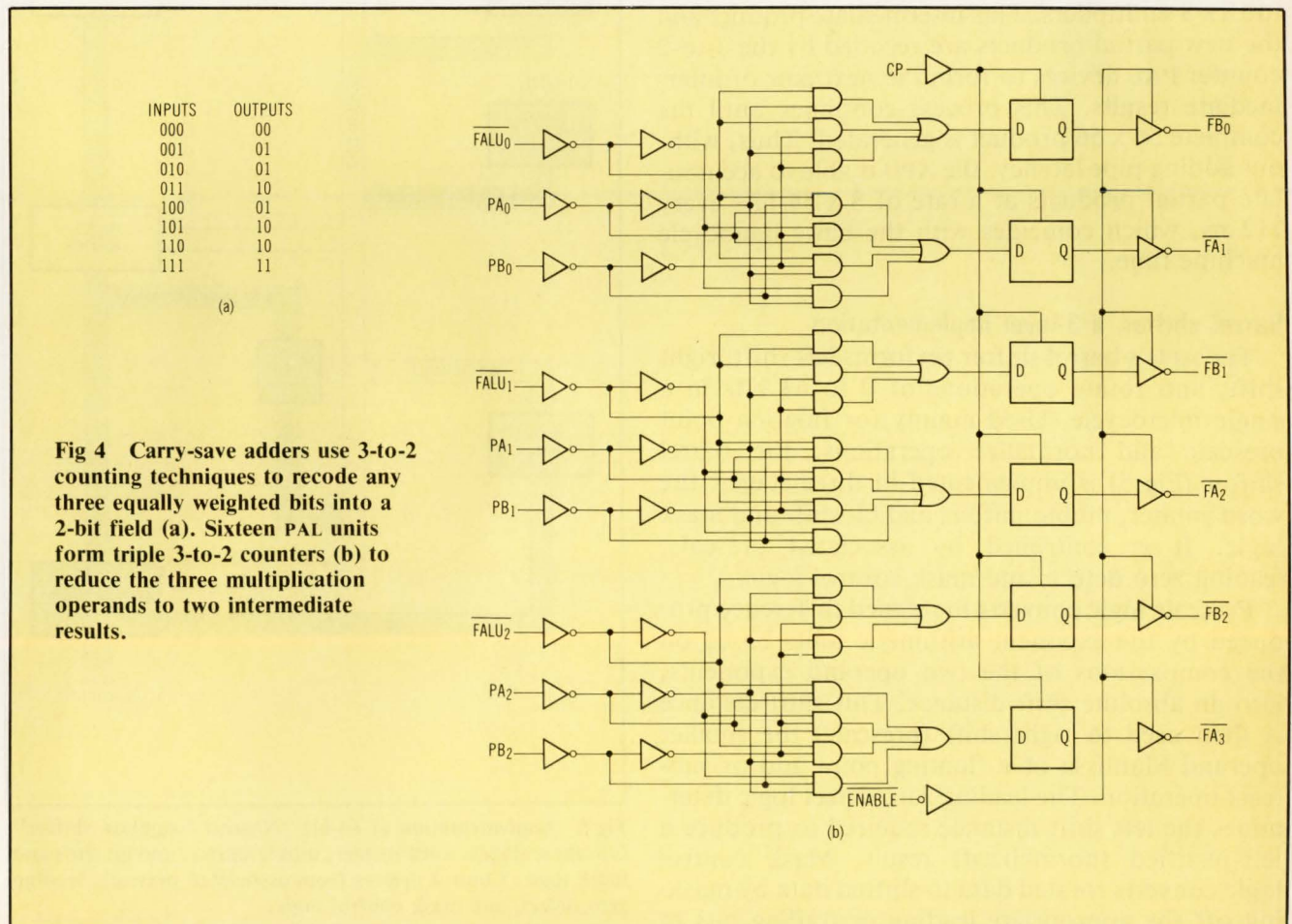
The heart of the FPP is the multiplier section (Fig 3). Double-precision floating point multiplication requires the calculation of a 56-bit x 56-bit product. Unfortunately, 56 x 56 parallel multipliers do not exist on silicon. From a cost/performance standpoint, the best solution is to use a number of small multipliers to build an intermediate sized parallel multiplier and then produce a large product (56 x 56) in multiple cycles.

Partial product generator FPP logic uses seven Am25S558 8 x 8 multiplier slices to implement an 8 x 56-bit multiplication array. Each multiplier chip produces a 16-bit product. In general, the 8 most significant bits (MSBs) of each partial product generator must be added to the 8 least significant bits (LSBs) of the next higher slice to generate the full

64-bit partial product. Exceptions are the 8 MSBs and LSBs.

This technique also requires the ability to accumulate partial products with the partial products from previous cycles. Thus, each cycle must be accompanied by two additions: the partial product summation and the intermediate product accumulation. While this can be done by following the multipliers with two levels of lookahead adders, usually 74S181s, the resulting nanocycle time is approximately three times longer than the partial product generation time of the 8 x 8 multipliers. Modifying this scheme, however, by adding registers between each level of logic, the pipeline multiplier reduces the nanocycle time to near the propagation delay time of the multiplier chips plus the clock to output time of the multiplier register plus the setup time of the intermediate result register. This scheme has two disadvantages: increased pipe latency, caused by the two extra levels of pipelining, and a high parts count.

Still another technique involves replacing one level of the pipe and one level of lookahead adders with carry-save adders between the partial product generators and the pipeline registers. Carry-save adders are used to implement a technique that is called 3-to-2 counting. As seen in Fig 4(a), any



*Without adding pipe latency, the APU is able to accumulate partial products at a rate of 8 x 56 bits every 112 ns.*

combination of 3 equally weighted bits can be recoded into a 2-bit field.

This makes it possible to reduce the three operands generated by the multiplication process (high and low partial products and 64-bit intermediate product) into only two operands which may then be summed together in a single lookahead ALU. The 3-to-2 recoding requires no-carry propagate logic and is therefore very fast. Only one level of pipelining is required because of the 3-to-2 counter's speed, resulting in both a reduced parts count and a reduced pipe latency.

In the APU floating point engine, 16 AmPAL16R6s, programmed as triple 3-to-2 counters, are used to reduce the three multiplication operands to two intermediate results [Fig 4(b)]. The registered PAL outputs are connected to the input buses of the Mantissa ALU that is also used for floating point addition and subtraction. The Mantissa ALU then calculates the next intermediate product in parallel with the partial products calculations occurring in the 8 x 8 multipliers. This intermediate product and the new partial products are recoded by the 3-to-2 counter PAL devices to form the next pair of intermediate results. This process continues until the complete 56 x 56 product is generated. Thus, without adding pipe latency, the APU is able to accumulate partial products at a rate of 8 x 56 bits every 112 ns, which coincides with the basic nanocycle machine time.

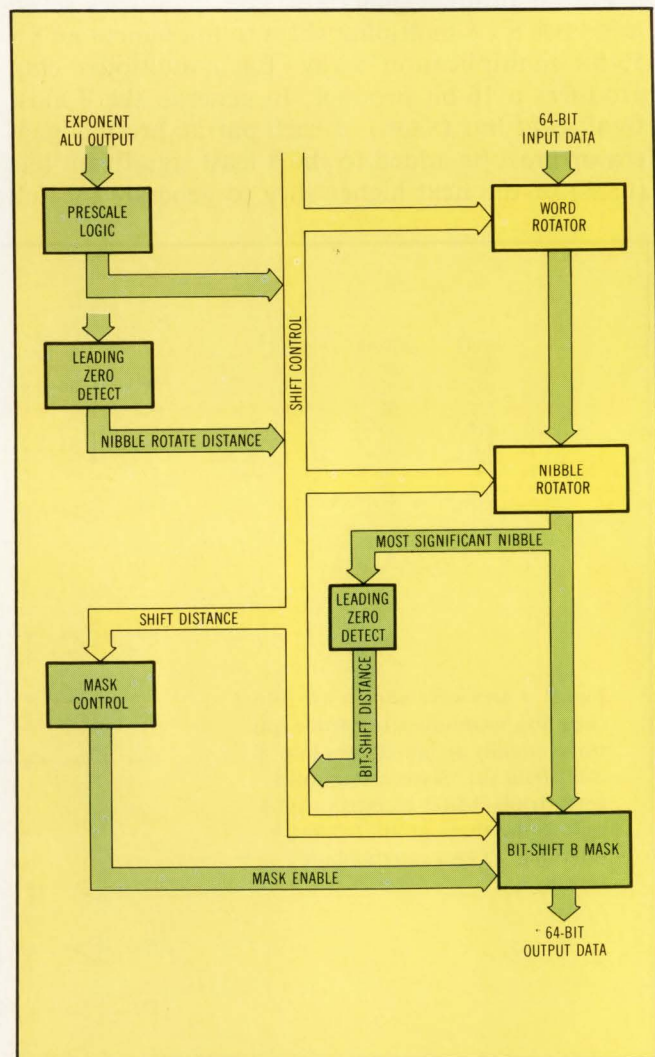
### Barrel shifter, a 3-level implementation

The APU's barrel shifter performs left shift, right shift, and rotate operations of 0 to 63 bits in a single microcycle. Used mainly for floating point prescale and normalize operations, the barrel shifter (Fig 5) is implemented in three stages: the word rotator, nibble shifter, and bit shift and mask logic. It is controlled by associated prescale, leading zero detect, and mask control logic.

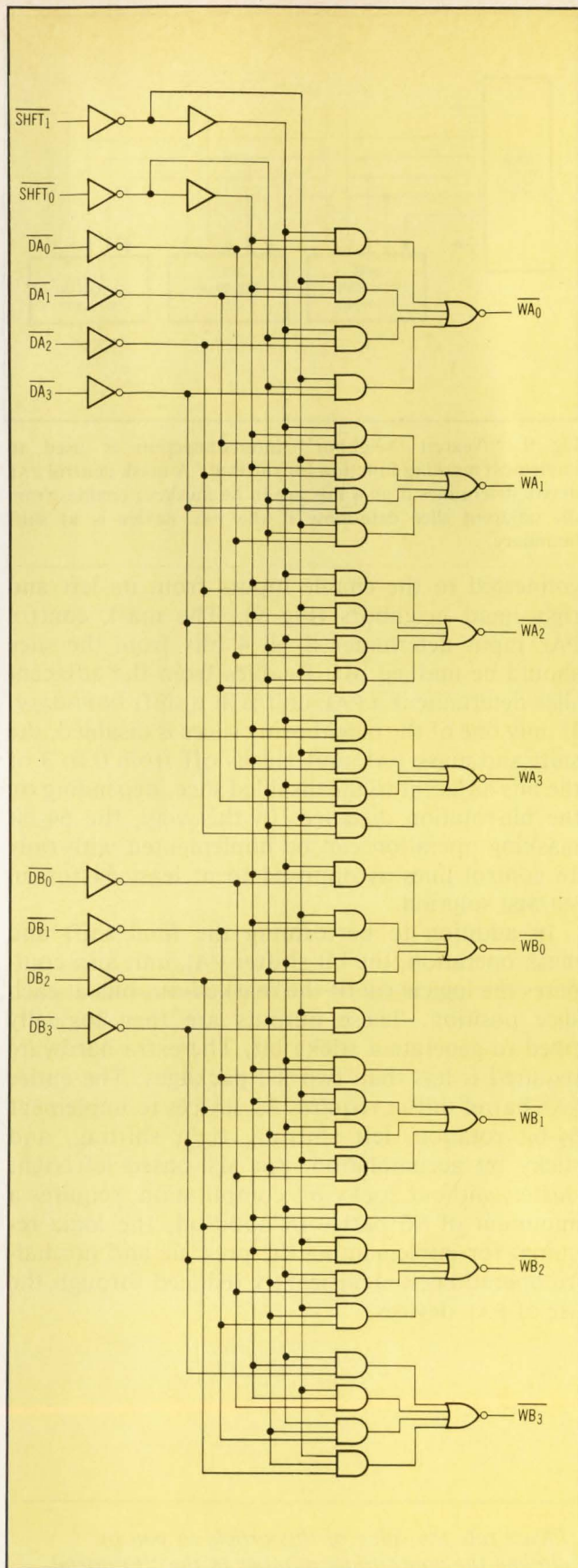
Prescale logic converts the signed difference produced by the exponent arithmetic units based on the comparisons of the two operand exponents, into an absolute shift distance. This shift distance is then used to right shift (prescale) the smaller operand Mantissa of a floating point add or subtract operation. The leading zero detect logic determines the left shift distance required to produce a left-justified (normalized) result. Mask control logic converts rotated data to shifted data by masking off the appropriate leading or trailing bits to

implement right or left shifts. These three sections are implemented in PAL.

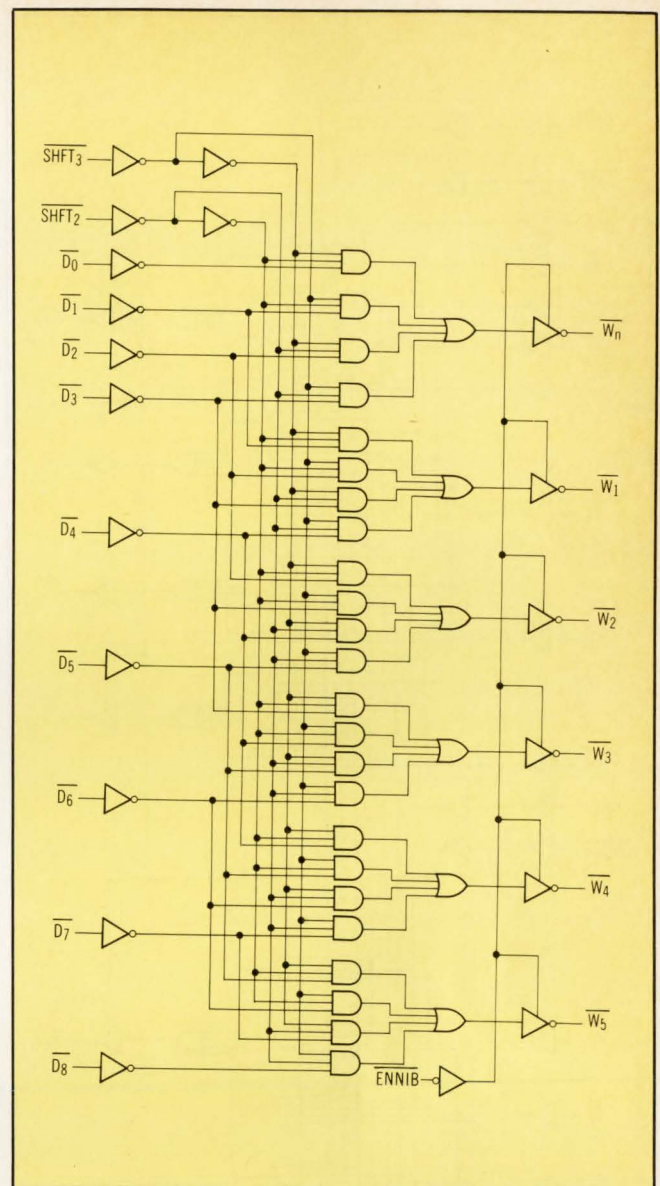
Implementing the 3-level, 64-bit barrel shifter in MSI requires the use of Am25S10 4-bit shifters. The first level is the word rotator which performs a circular rotate of 0, 16, 32 or 48 bits. Although implementation is simple, the MSI solution requires 16 packages. The second level is the nibble shifter, essentially identical to the word rotator but wired to rotate 0, 4, 8, or 12 bits. The final barrel shifter stage requires not only bit rotate but also leading and trailing bit masking and sticky bit computation (ie, the logical OR of the masked-out bits). An MSI solution requires not only the 16 packages of AM25S10s, used in each preceding level, but also 16 AND gate packages for masking, with another 16 AND packages for the sticky bit computation. Control logic for the mask operation requires as much logic as the entire shift path. A more practical solution consists of building separate left and right



**Fig 5 Implementation of 64-bit "Nearest Neighbor Shifter" is in three stages: word rotator, nibble shifter, and mask logic. Control derives from associated prescale, leading zero detect, and mask control logic.**



**Fig 6** Word rotation, first level of 3-level shifter, consists of eight PAL units, each programmed as two 4-bit rotators. It performs a circular rotate of 0, 16, 32, or 48 bits.

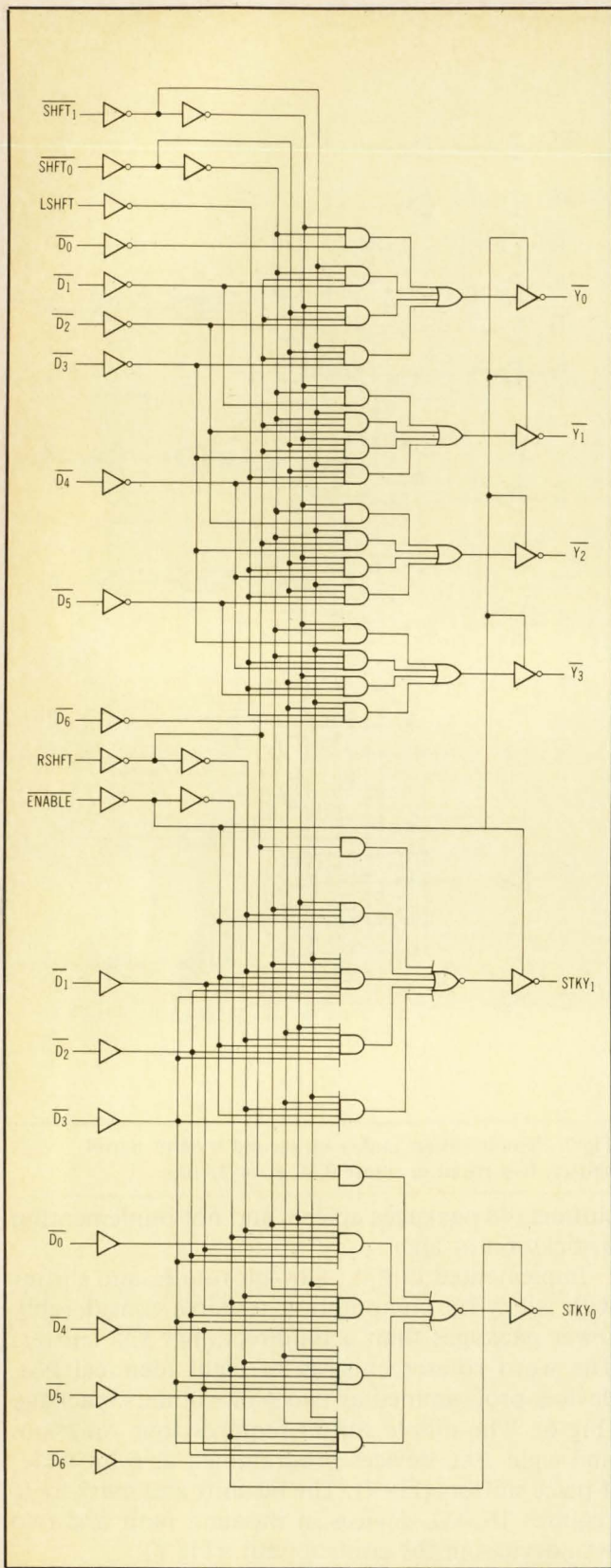


**Fig 7** Nibble shifter makes up second level of barrel shifter. It is wired to rotate 0, 4, 8, or 12 bits.

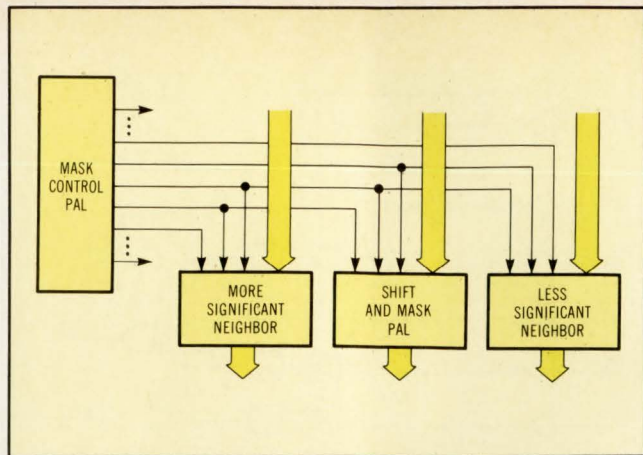
shifters, 48 packages apiece, and not implementing a sticky bit at all.

Implemented in PAL, a 64-bit rotator and shifter with sticky bit computation requires considerably fewer packages than a unidirectional MSI shifter. The word rotator consists of eight identical PAL devices programmed as two 4-bit rotators/package (Fig 6). The nibble shifter requires four Am25S10s and eight PAL devices programmed as 6-bit wide, 4-place shifters (Fig 7). The bit shift and mask logic requires 16 PAL devices in the data path and two PAL devices in the control path. (Fig 8).

To implement the masking function required for shifting, a technique called "Nearest Neighbor Shifting" (U.S. patent pending, Computervision Corp) is used. Each shift and mask PAL device has an enable input from one mask control PAL unit. In addition, each shift and mask PAL device is also



**Fig 8** Bit shift and mask logic for barrel shifter requires 16 PAL devices in the data path and two PAL devices in the control path. Each shift and mask PAL device has an enable input from one mask control PAL device and is connected to enable inputs of its left and right neighbors. The 64-bit masking operation requires only 16 control lines.



**Fig 9** "Nearest Neighbor" interconnection is used to implement masking function for shifting. A mask control PAL device determines if all 4 bits are to be masked; enables from the adjacent slice determine if the PAL device is at shift boundary.

connected to the enable inputs from its left and right-hand neighbors (Fig 9). The mask control PAL input determines if all 4 bits from the slice should be masked off. Enables from the adjacent slice determine if a PAL unit is at a shift boundary. If only one of the neighboring slices is disabled, the shift and mask PAL unit masks off from 0 to 3 of the bits adjacent to the disabled slice, depending on the bit-rotation distance. In this way, the 64-bit masking operation can be implemented with only 16 control lines as opposed to at least 64 for an SSI/MSI solution.

In addition to performing the final shift and mask operation, the bit-shifter PAL unit also computes the logical OR of the masked-out bits at each slice position. These outputs are then logically ORED to generate a sticky bit. The extra hardware required is less than two SSI packages. The entire PAL barrel shifter requires 38 devices to implement 64-bit rotation, left shifting, right shifting, and sticky bit accumulation. An MSI-based left/right shifter, without sticky bit computation, requires a minimum of 96 parts. In addition, the logic required for implementing the prescale and normalize operations is significantly reduced through the use of PAL devices.

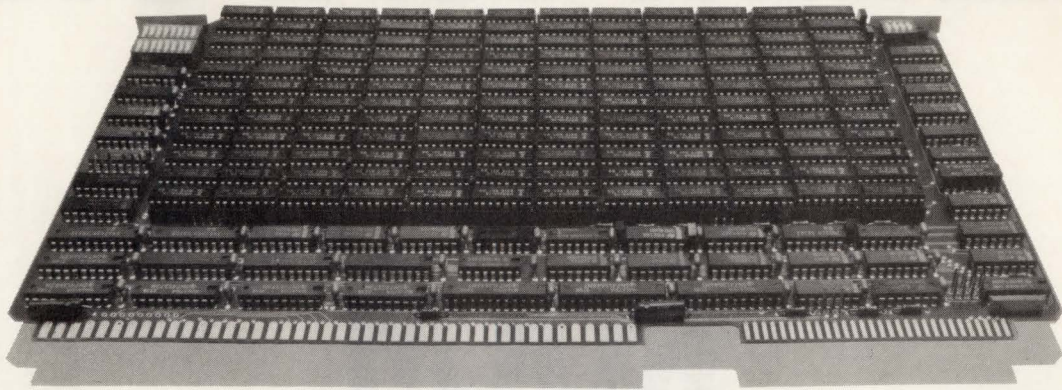
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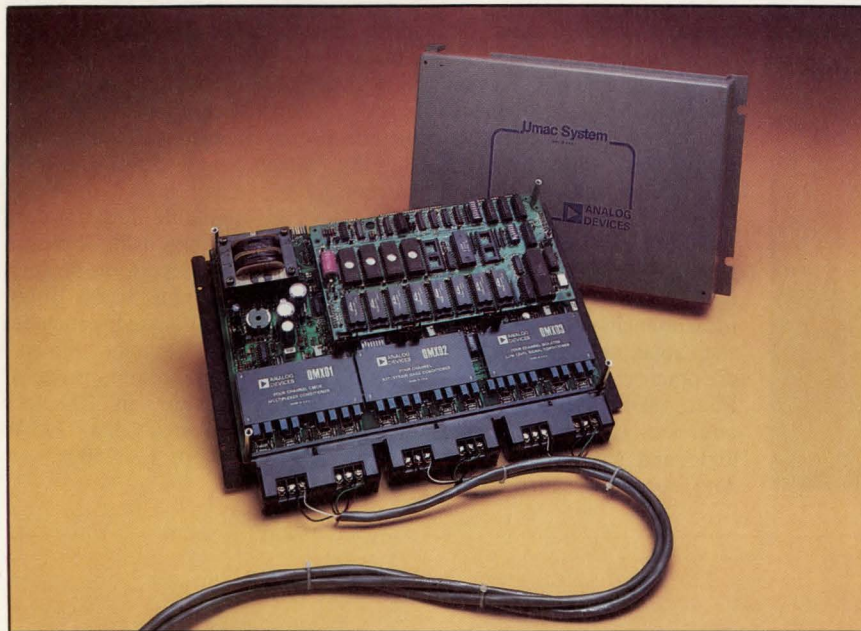
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### Measurement and control system employs powerful Basic



The  $\mu$ MAC-5000 is a single-board, programmable measurement and control system providing an extended Basic for custom applications. In addition, complete signal conditioning, digital I/Os, and serial communications are available.

System hardware includes up to 12 channels of plug-in signal conditioning, a 14-bit ADC, an 8088 microprocessor, 64K bytes of battery-backed RAM (52K bytes user accessible), and 96K bytes of ROM (16K bytes user accessible). There are eight digital input and eight digital output channels, two optional channels for frequency and pulse inputs, and two communication ports supporting RS-232, RS-422, RS-423, and 20-mA current loop interfaces.

Industrial grade signal conditioning permits direct sensor connection with common mode voltages up to  $\pm 1000$  V, input-to-output and channel-to-channel. Also, plug-in modules containing all the elements needed for specific sensor types come in isolated and nonisolated forms for a variety of applications. Four channel modules can be mixed in any combination, at three modules per board. Expansion boards allow connection to hundreds of analog and digital I/O points, in clusters or multidrop configurations.

Enhanced Basic, known as  $\mu$ MACBasic, provides error trapping statements that aid in program development. It goes beyond compiling user instructions and checking for compiler errors by ferreting out runtime errors caused by illegal program operations. The ON ERROR GOTO GOSUB tells the program which line to move to if, and only if, an error occurs. Users can also program their own error conditions.

Software interrupts are another enhancement over standard Basic. This versatile programming tool allows the system to switch over to execute a procedure that is flagged by an interrupt. Clock-based interrupts separate critical events (precise PID loop calculation) from lower priority events (program statements). Event counting interrupts flag  $\mu$ MACBasic on reaching zero from a preprogrammed number of events. Additionally, communication interrupts halt program execution when serviced with a user-defined character.

The language improves software documentation through structured programming and lengthened variable names.  $\mu$ MACBasic allows variable names up to 256 characters, including the underscore, so that variables can appear as more than one word. The only requirement with the

extended variable names is that they begin with a letter.

A modular programming approach offers several advantages. First, modules are less prone to errors and easier to fix; errors can be isolated to a particular module so that only the module and not the entire program has to be debugged. Second, several programmers can work on modules separately for improved productivity. In addition, modular structures allow programmers to add new keywords and call complex operations with one keyword. This is particularly useful for repetitive applications.

Each program module—which contains a main program or procedure/function—uses a particular section of memory called a workspace. The software allocates room for variable and module code in the workspace. A procedure acts much as a subroutine would in standard Basic. Within procedures are series of commands that trigger actions, such as displaying messages. Functions, on the other hand, assume particular calculated values, for instance, the sine of X. Once completed, functions and procedures return to the main program.

Both functions and procedures are written in Basic. Once debugged, they are permanently added to the system using a COMPRESS command. After this command is executed, the module cannot be edited or listed, making it inaccessible to the programmer. To delete functions and procedures the battery backup and ac power are disconnected, thereby deleting everything in RAM. The PROGRAM command will transfer the modules into ROM for permanent storage.

Either dumb terminals or personal computers can be used for program development. Firmware will initialize the system and prepare it for Basic programming. For faster execution, programs can be written in assembly language. The microprocessor directly executes the code and avoids the compiler. The CALL statement is used to access assembly language routines from a program.

The system is priced at under \$3500 with 12-channel isolated inputs. **Analog Devices, Inc.**, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. Circle 260

## New generation, 32K x 8 DRAMS provide wide operating margins

The MK4856 is especially designed for small microprocessor-based systems that require minimal amounts of solid state

memory. Fabricated with double-level polysilicon and double-level metal interconnection, the DRAM uses the LD<sup>3</sup> process. This is a scaled NMOS process technology that minimizes the transistor's short channel effects and produces high density coupled with fast access times. Hidden refresh feature allows the output to be held valid for up to 10  $\mu$ s by holding  $\overline{G}$  active low (where  $\overline{G}$  is the output/refresh control). This allows refresh cycles to be performed while holding data valid from a previous cycle.

Chip applications include terminal, industrial controls, and electronic test and measurement equipment. In such applications, the DRAMs are practical for two reasons. First, their nonmultiplexed addresses eliminate system logic and simplify timing. And, second, an integrated

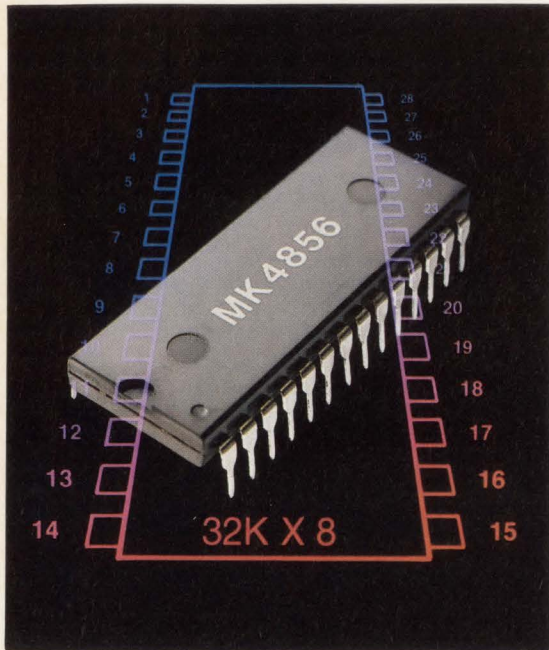
refresh counter reduces the external overhead logic.

The chip's power specs include single 5-V ( $\pm 10\%$ ) supply, 275-mW maximum active power, and 27.5-mW maximum standby power requirement. In addition, all inputs are TTL compatible, low capacitance, and protected against static charge.

Electrical characteristics for ac are an input capacitance of 5 pF (on pins A0 to A14) and 10 pF on  $\overline{E}$ ,  $\overline{G}$ , and  $\overline{W}$ , pins. Input and output capacitance of DQ is 8 pF. Electrical characteristics for dc include 50-mA operating current, 5-mA standby current, and 50-mA refresh current.

The device is available in a standard 600-mil, 28-pin package using a pinout compatible with other Bytewyde devices. There are three available access times: 100, 120, and 150 ns. Packaging includes a plastic DIP, leadless hermetic chip carrier, or cerDIP. The preliminary price for the DIP 150-ns version, in 100-piece quantities, is \$100. **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 261



## Multi-user development system runs Unix version

Using Genix, a derivative of Berkeley Unix 4.1, SYS16 develops applications for the NS16000 16/32-bit microprocessor family. The system features access to assembler, C, and Pascal compilers, as well as realtime in-system emulation tools. Emulation and software development can be performed concurrently.

Two main units make up the system: a processor module and a disk/tape module housing a 20M-byte 8" Winchester disk with 20M-byte 1/4" streaming-tape backup. Optional disk drive modules increase system capacity in 40M-byte increments up to 140M bytes.

Demand-paged virtual memory expedites development of systems that operate in multiprogramming and large database environments. Internal data paths, 32-bit registers, and an ALU provide fast processing. Information is transmitted over a 16-bit data bus that links the CPU to 32-bit floating point, memory management, and custom processor chips.

The system configures with up to eight terminals. Each user can independently address up to 16M bytes of memory, using virtual memory management to



swap 512-byte pages of program or data directly between main and disk memories. Main memory itself consists of 1.25M bytes of RAM, expandable to 3.25M bytes with provision for error checking and correction.

In its standard configuration, the processor module connects CPU, serial I/O, memory, and disk/tape controller boards in four of six available slots. The remaining two slots accommodate optional memory boards.

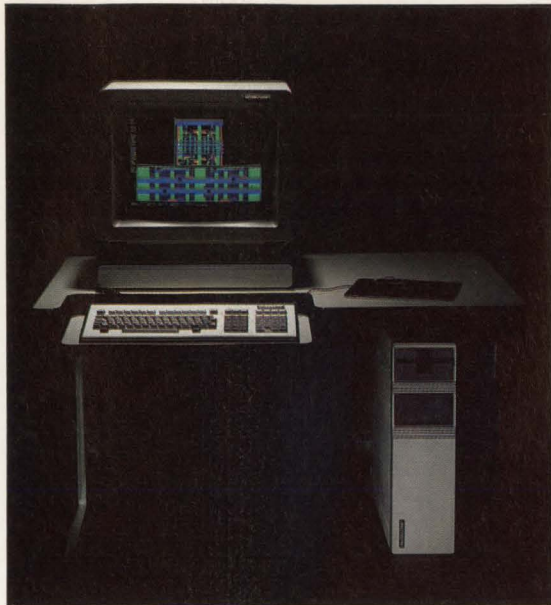
The CPU board contains the NS16032 microprocessor with peripheral support chips. Diagnostic firmware; 256K bytes of RAM; and parallel, GPIB IEEE 488, and RS-232 ports also reside onboard. The

intelligent serial I/O board contains logic to support the eight RS-232 user ports. Each port operates at up to 9.6k baud, with FIFO buffers to increase system throughput. The disk tape controller board manages up to eight disk drives with streaming-tape backup.

Hardware support for the system includes external PROM programming and an optional ISE/16 NS16032 in-system emulator. The SYS16 will cost around \$30,000. The system will be available for customer shipments by the end of this year. **National Semiconductor Corp, Microcomputer Systems Div**, 2900 Semiconductor Dr, MS D3670, Santa Clara, CA 95051.

Circle 262

## High performance workstation offers processor options



Processor-independent WorkStation 500 partitions key applications to dedicated processors and incorporates hardware and software standards. Because of this, the workstation meets many requirements of the OEM marketplace.

System design is based on the company's Performance Architecture for high speed system throughput and realtime performance. It features an 8M-byte/s memory interconnect bus, dual 32-bit

10-MHz VLSI processors with a 4K-byte cache, a 1024-element translation buffer, and a 1024-entry I/O map with 6M bytes of error correcting memory (supporting a 16M-byte virtual address space).

An integral part of the system is the Independent Graphics Processor (IGP). Available with resolutions of either 1024 x 800 or 832 x 600, it contains an 8-MHz 68000 with its own 128K-byte program storage. The IGP independently processes graphic images to free the CPU for application programs. Each processor supports rapid dynamic image transformations and multiplanar displays. To do this,

the processor has up to 1.2M bytes of raster memory in dual frame buffers up to 10 planes deep. The monochrome display requires a single memory plane (to be driven by the IGP), while the color display requires either 6 or 10 memory planes. A 60-Hz noninterlaced refresh rate eliminates screen image flicker. Both displays feature a 117-key low profile keyboard, plus an optional mouse or data tablet and puck.

Within the system CPU, floating point or combined floating point array processors can be added for increased performance. The independent floating point processor performs a single-precision (32-bit) add or multiply in 1.6  $\mu$ s. It also provides double-precision (64-bit) IEEE standard arithmetic. Sixteen sets of 32-bit single-precision registers enhance multiprocessing performance.

The floating point array processor performs a 1024-point add or multiply in 413  $\mu$ s. This combination supports single- or double-precision, floating point, and vector math. It can also store 16k 40-bit elements locally and maintain floating point capabilities.

Also included in the system is the enhanced 6M-byte/s Multibus, which connects the CPU with system peripherals and operates under RTU, a realtime virtual memory Unix operating system. The operating software includes Unix support, text processing, and communication utilities, together with editors and the source code control system. Both the C and Bourne shells are provided. Other RTU features include memory locked processes, guaranteed process priorities, contiguous files, and high speed pipes.

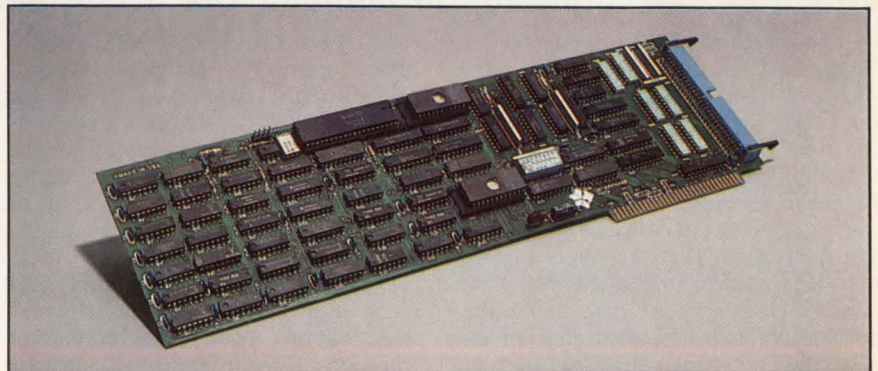
Prices for the system range from \$7095 to \$29,585, depending on configuration. **Masscomp**, 543 Great Rd, Littleton, MA 01460. **Circle 263**

## Rigid disk controller for IBM PC supports SMD interface

The Maverick SMD PC-80 rigid disk controller for the IBM PC and PC look-alikes supports the SMD interface often used in minicomputers. The controller accommodates 8" or larger disks and fixed/removable cartridges without hardware or software modifications.

It supports two SMD disk drives with storage capacities ranging from 16M to 800M bytes each. High performance SMD-compatible drives from Control Data Corp, Fujitsu, and Amcodyne make the Maverick's throughput three to four times faster than an IBM PC-XT equipped with a standard Winchester disk. Also, the reduced parts count improves reliability.

The controller is fully compatible with PC operating systems. Software drivers are available for IBM-DOS 2.0, as well as for UNETix—the Lantech Systems multi-tasking networking operating system that implements Unix. The company will also supply a BIOS for easy interface to other operating systems.



In applications, the device provides capacity for large database management areas at the PC level. It also eases performance bottlenecks at network file servers and can provide economical mass storage for all PCs in a network.

System architecture is fully buffered with a bipolar state machine managing the high speed data stream. External to this data stream is a CMOS processor that regulates onboard activity. Bus transfers

are supported through either high speed DMA or through programmed I/O. In addition, the controller has dual-porting and fully programmable sector sizes up to 960 bytes. Automatic error correction with 32-bit ECC, bad track and sector replacement, and overlapped seeks are all provided. The Maverick is priced at \$1895 in single quantities and \$1200 in 100-piece lots. **Interphase Corp**, 2925 Merrell Rd, Dallas, TX 75229. **Circle 264**

### Superminicomputer uses 100K ECL for high speed

The Harris 1000 computer system, designed with 100K ECL technology, features a 4-MIPS Whetstone performance, while using less power than earlier ECL circuitry. This advanced technology, combined with hardware implementations for virtual memory and transcendental functions, gives the system a high speed appli-

cation base that includes scientific and industrial areas.

The basic system configuration includes a CPU with 6K bytes of cache, 16 external interrupts, a line frequency clock and an interval timer, the VOS operating system, and dual cabinets. In addition, special functions are performed by the maintenance aid processor (MAP), the integrated memory subsystem (IMS), and the communication network processor (CNP).

As a separate microprogrammed processor, the MAP runs power-up diagnostics and checks memory, I/O channels, and CPU data paths before loading microcode. The IMS combines the memory controller with 1.5M bytes of memory on a single board (with capacities to 12M bytes) for both main and shared memory.

Each CNP in the system (up to 14 can be added) simultaneously supports communication via async, sync, isochronous, and X.25 protocols. IEEE 488 and parallel

line printer interfaces are also available. Single-board CNPs support up to 16 communication lines for local or remote device connection. Each line is individually programmable and can concurrently support different protocols at different speeds.

A soft control store implements the CPU microcode for instructions in RAM instead of PROM. Volatile RAMs are automatically loaded each time the machine is powered up. Any time the microcode is enhanced, the control store can be updated by distributing new microcodes.

The system's virtual memory is demand-paged and totals 48M bytes (configured in 3K-byte pages). The CPU includes one virtual address register for each page to track virtual to physical memory relationships.

Additional high speed features include pipeline processing, which allows seven instructions to be processed simultaneously with a CPU cycle time of 75 ns, and precisions ranging from 32-bit single precision to 96-bit quadruple precision.

The basic system 1000 is priced at \$250,000. **Harris Corp, Computer Systems Div**, 2101 W Cypress Creek Rd, Ft Lauderdale, FL 33309. **Circle 265**



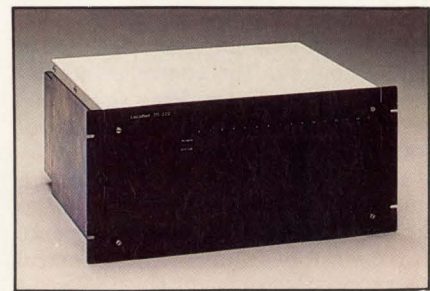
### Modular PCU improves broadband LAN performance

A packet communication unit (PCU), designated the LocalNet 20/220 S-MUX, improves data throughput and functional characteristics of broadband LANs. The modular units allow users to add packet communication processors (PCPs) in 2-port increments. A single chassis offers up to 32 ports (16 cards with two ports on each card). Different types of PCPs can be placed in the same chassis. PCP types include async, bisync, and async-only encrypted. The encryption option uses the U.S. National Bureau of Standards' Data Encryption Standard algorithm for data security and network protection. Also used is the key distribution scheme, available to users on Sytek's Secure LocalNet 20/100 Z01.

Through the same PCU, users can transmit and receive presentation level data using different async data terminating equipment. Bisync support will include 3270-type terminals, Hasp, and 2780 and 3780 RJE devices.

Every PCU dedicates a 6-MHz z80 processor to each PCP and employs a proprietary digital arbitration scheme for modem sharing by PCPs. Each PCP contains all the software necessary for the modem interface, the attached device interface, and implementation through Level 6 of the 7-layer ISO open system interconnection model for data communication. This software arbitration technique enhances the company's carrier sense multiple access with a collision detection (CSMA/CD) contention management mechanism. CSMA/CD offers two distinct advantages: reduced network packet collision rate, and maximum capacity data throughput on the broadband channels.

Network managers can define each 2-port PCP with an independent unit identification address so that a variety of applications and port contention rotaries can be handled by a single S-MUX. PCPs are enabled automatically when power is



turned on, and a multiple reset capability allows users to reset individual PCPs or the entire unit. Each PCPs port can operate at data rates between 75 and 19.2k bps. Aggregate throughput per PCP is greater than 28k bps.

The fully configured device is priced at \$345 per port, with 32 async connections. Initially offered as async PCPs; bisync and encrypted versions are due early in 1984. **Sytek, Inc**, 1225 Charleston Rd, Mountain View, CA 94043.

**Circle 266**

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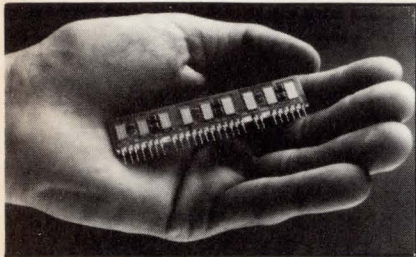
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CIRCLE 132

## Dynamic RAM modules



Memory modules HS2648 and HS2649 are designed for use in high-end computer systems. The modules contain eight or nine 64K-byte RAMs along with decoupling capacitors. Employing chip and wire technology, the modules have access times of 200 ns and cycle times of 335 ns. The RAM devices are bonded directly to thick-film hybrid substrate, then dipped in conformal-coating bath. In addition, the substrate has been laid out so that 256K- or 1M-bit chips can be used on the module. In quantities of 100 the prices range from \$100 to \$114. **National Semiconductor Corp**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle 267

## STDbus memory module

Processor independent memory module 5006A accepts 32K bytes of static memory in the form of type 6116 RAMs, 2716 EPROMs, 5-V pin-compatible EEPROMs, and MOS ROMs. All types can be freely intermixed without module reconfiguration. Unused sockets are disabled automatically, eliminating the potential for wasted memory space. With 6116 series RAMs, access times of 100, 120, or 150 ns can be achieved. The populated version is \$250 and the depopulated version is \$99. **STD Microsystems**, 399 Sherman Ave, Palo Alto, CA 94306. Circle 268

## DRAM board for STDbus processors

Dynamic RAM board SB8130 is compatible with processors using the STD bus system and is available in either a 64K- or 128K-byte version. Basic board has two 64K-byte banks with bank selection provided for 8-bit processors allowing more than 64K bytes to be addressed. Featured is a transparent onboard refresh with optimization circuits that generate wait requests for access time or refresh considerations. Both versions are compatible with CP/M 2, CP/M 3, MP/M-11, and CP/M-86. In quantities of 10 to 24 prices range from \$400 to \$580. **Micro/sys**, 1367 Foothill Blvd, La Canada, CA 91011. Circle 269

## Expandable EEC memory

High-density dual-height ECC memory modules are configured in 256K to 2M bytes. MECCV11-L memory system has 22-bit and 18-bit addressing capability and includes control and status registers compatible with DEC diagnostics. All single bit errors are corrected with no access time penalty. The register logs single and double bit errors and diagnostic modes verify error correction logic integrity. System consists of a controller with four 512K-byte memory boards. Single-unit pricing is \$895 to \$3695. **PEBX**, 501 Vandell Way, Campbell, CA 95008.

Circle 270

## Optical storage device

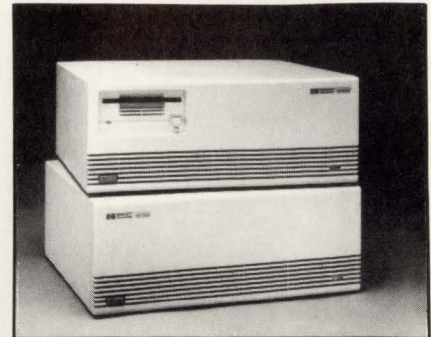
H-6975-1 storage device uses a 12" optical disk with a capacity of 1,310M bytes/side. This capacity allows 20k A4 (215- x 297-mm) size documents to be stored. In addition to storing characters and illustrations, it can also store coded computer data. Average access time is 250 ms. Also available are optical disk library devices. The H-6975-A1 uses 16 optical disks and has an avg access time of 5 s. The H-6975-A2 uses 32 optical disks and has an avg access time of 6 s. **Hitachi America, Ltd**, 1800 Bering Dr, San Jose, CA 95112. Circle 271

## Higher capacity drives at same price

Models 1302 and 1303, members of a 5 1/4" Winchester series, have increased capacity without increasing price. Model 1302 is a 26M-byte drive with access speeds up to four times faster than comparably priced drives. Model 1303 offers 43M bytes and is 50% faster. Both drives feature a positioning system to achieve a 33-ms avg seek time, including settling. Both drives are ready for immediate shipment. The 1302 is priced under \$800 and the 1303 is under \$900. **Micropolis Corp**, 21329 Nordhoff St, Chatsworth, CA 91311. Circle 272

**December Preview—  
1983 system components  
roundup.**

## Small computer Winchesters



HP9133V and 9133XV Winchesters are specifically designed for small computer systems. The hard disks, which have formatted capacities of 4.8M and 14.5M bytes, respectively, team up with a 270K-byte, 3.5" microfloppy. Microfloppy media is packaged in a hard polymer jacket with an auto shutter and hard center. A disk monitor signals when the disk should be replaced. Prices begin at \$3000 for the 5M-byte version and \$3600 for the 15M-byte version. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303. Circle 273

## VMEbus board with up to 2M bytes

MM-6000D memory board provides from 128K to 2M bytes. The single board VMEbus memory uses either 64K- or 256K-byte DRAMs depending on an on-board jumper. Features include a 330-ns cycle time, 210-ns access time, single 5-V supply, odd parity generation and checking, and module selection on 1000 boundaries in the 16M-byte address field. All boards are temperature cycled and burned in for 48 hrs while memory diagnostics are run. Single-quantity price is \$1250 for the 512K-byte version. **Micro Memory, Inc**, 9436 Irondale Ave, Chatsworth, CA 91311. Circle 274

## Increased memory storage for PC

PC-8000 memory subsystem is designed for use with the IBM PC and PC compatible microcomputers. It attaches up to 1G byte of memory storage to a PC or compatible. The subsystem is used for very large database applications, software development, and as a file server for computer networking. The system consists of a controller and one or two disk drives with from 16 to 500M bytes of capacity each. It is hardware and software compatible with fixed/removeable disk media and offers 17-ms access times. **National Memory Systems Corp**, 355 Earhart Way, Livermore, CA 94550. Circle 275

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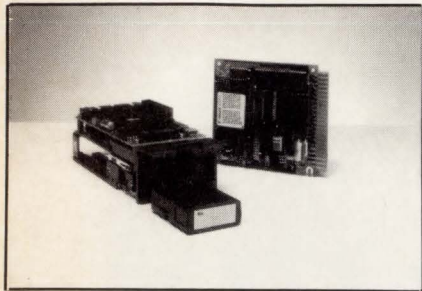
If your skills made you pick up this magazine, you could put them to work in the Peace Corps. From recently graduated nurses to experienced cattle ranchers, math teachers or mechanics, there is no such thing as a "typical" Peace Corps volunteer. They're all ages with one belief in common: Whatever they have to give can be shared to help people help themselves. And it's being proven every day by Peace Corps volunteers in more than 60 different countries around the world.

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## Bubble memory cassette system



The 1M-bit bubble memory system consists of a 1M-bit bubble cassette, an 8-bit parallel interface, and an expansion holder. Operating features include 12.5-ms avg access time (shortened to 2.6 ms in the Seek mode), ECC and bus parity, 24 commands, and three subpages for the 128K-byte data area for storing sub-system control data. Expansion holder units allow memory capacity to increase to 512K bytes. It can be used as a program loader and data file for testing machines and numerical control equipment. **Fujitsu America, Inc, Component Div**, 918 Sherwood Dr, Lake Bluff, IL 60044. **Circle 276**

## Paired interleaving RAM card

NS789 is a 1M-byte RAM memory card that supports VAX hardware, software, system, and std peripheral options. Configured as a 256K x 39-bit hex card, it provides 1024K bytes of memory. Typ read access time is 225 ns, with a read/write/refresh cycle time of 425 ns. An on/offline switch permits the user to isolate the card from the system without actually removing it from the backplane. The price is \$2700; since they are compatible with the paired board interleaving technology of the VAX, they will normally be sold in pairs. **National Semiconductor Corp**, 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 277**

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## DEVELOPMENT SYSTEMS

### Enhanced Multibus display

As a single-board design aid for Multibus environments, the ZX-906B provides nine latching hex displays. They will display 20-bit address and 16-bit data values as they occur on the Multibus and select the bus cycle type (memory-I/O and read/write). In addition, the board provides five rotary hex address/port selector switches and toggle switches for 8/16 bit, first/last, =/≠, read/write, and memory I/O. It also monitors the 5- and 12-V lines, eight interrupt lines, and plugs directly into the Multibus backplane. The board is priced at \$565. **Zendex Corp**, 6644 Sierra Lane, Dublin, CA 94568. **Circle 278**

### Prototyping system

The 8X305KT1SX allows low cost prototyping and evaluation of 8X305-based systems. It develops firmware and application circuitry. Consisting of a single circuit board, it includes a target microcontroller and peripheral devices. The microprogram resides in writeable control storage. A second processor controls system operation by loading the control storage and activating the run/step logic. The byte-oriented microcontroller features a 200-ns cycle time. **Philips Electronic Components and Materials Div**, PO Box 523, 5600 AM Eindhoven, The Netherlands. **Circle 279**

### Interactive circuit analysis

Mspice runs on the Idea 1000 workstation and is an enhanced version of the Spice linear circuit analysis tool. The software provides interactive analog circuit development support available in a standalone or locally networked CAE system. Mspice plots voltages and currents, provides access to currents without dummy voltage sources, and offers most std Spice simulation capabilities. Interactive analysis control includes setting probes, monitoring and interrupting analyses, and looping and conditional operations. Mspice is priced at \$9000. **Mentor Graphics Corp**, 10200 SW Nimbus Ave, Portland, OR 97223. **Circle 280**

### Development for CP/M-80 software

System-HMCS enables any CP/M-80 system to serve as a development station for Hitachi HMCS-40 micros. The software system includes macro assembler, interactive editor/assembler, text editor, cross-reference generator, and offloading

facilities. The macro assembler has full macro and conditional assembly features, as well as the ability to chain source files together during a single assembly. Individual development systems are available for \$150 each on CP/M 8" soft-sector or 5" North Star, Osborne I, Kaypro II, or IBM PC diskettes (among others). **Allen Ashley**, 395 Sierra Madre Villa, Pasadena, CA 91107. **Circle 281**

### Development system emulator

The HP 64292S, as an addition to the 64000 system, is an NSC800 emulator. Features include realtime operating mode, single stepping, display and modify memory, I/O modes, and interactive modes with other 64000 emulators. The emulator allows hardware and software designers to test and debug code and circuits for NSC800-based products. Because emulation executes from specified combinations of emulation and target system memory, hardware and software components can be tested as developed, independent of the amount of completed hardware. The emulator is priced at \$3800. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 282**

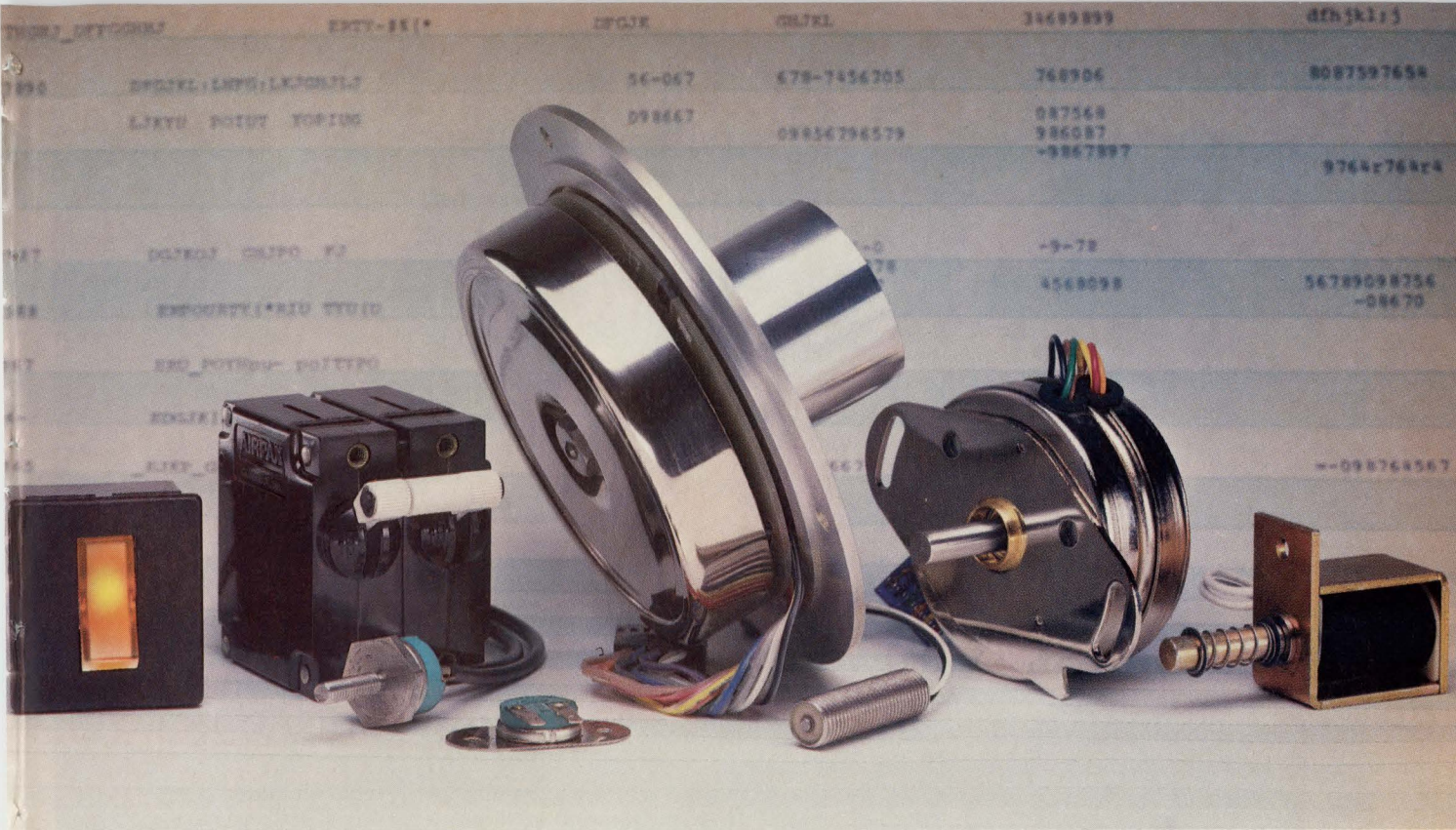
### Software development system

An entry level development system, the KDS-908 supports in-circuit emulation and logic analysis modules while networking with other KDS or 2300 series units. Dual 5¼" slimline floppy disk drives containing 616K bytes of storage integrate into the compact workstation. The terminal contains a Z80 CPU, 256K bytes of RAM, 12" green phosphor screen, two RS-232 ports, and a Centronics-compatible printer port. Price is \$6500. **Kontron Electronics**, 5730 Buckingham Pkwy, Culver City, CA 90230.



**Circle 283**





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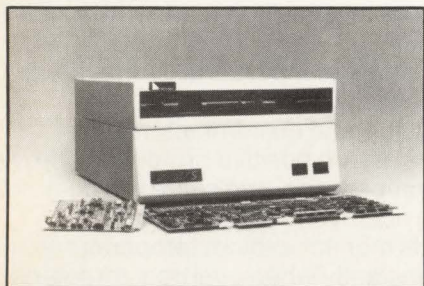
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Keeping computers in touch with people

CIRCLE 135

## SYSTEM COMPONENTS/DEVELOPMENT SYSTEMS

### STD bus system



The DS22/S functions as a STD bus development system. The std unit uses a Z80 or 8085 CPU with 64K bytes of RAM, 20 card slots, two RS-232-C ports, dual 8" double-sided/density floppy disks, and a CP/M operating system. Options include 8088 CPU, CP/M-86, 5M-byte hard disk, PROM programmer, Centronics parallel I/O port, and Fortran, Forth, Basic, C, and Pascal languages. Applications include small production runs such as in special purpose test stations or process control systems. The DS22/S is priced at \$5250. **Micro/sys**, 1367 Foothill Blvd, La Canada, CA 91011. Circle 284

### Microprogramming development

Model DS470 offers development, integration, and test of custom microcode for high performance processor-based designs. The standalone workstation includes the DS270 Emulyzer (PROM emulator and logic state analyzer) plus a micro with Multibus motherboard, VT100-compatible CRT with detached keyboard, memory, and disk storage. Operating systems include Unix (with 68000 CPU) or CP/M (with Z80A CPU). Base price with 68000/Unix is \$19,900, and \$12,950 with Z80A and CP/M. **Hilevel Technology, Inc**, Irvine Technology Ctr, 18902 Bardeen Way, Irvine, CA 92714. Circle 285

### DEC-compatible software development

The 8561 multi-user software development unit supports one or two users, and is upgradable to an 8560 for four to eight users. It features the TNIX operating system that is based on Unix v.7 and provides a team-oriented filing system, auto-build control, text processing tools, and

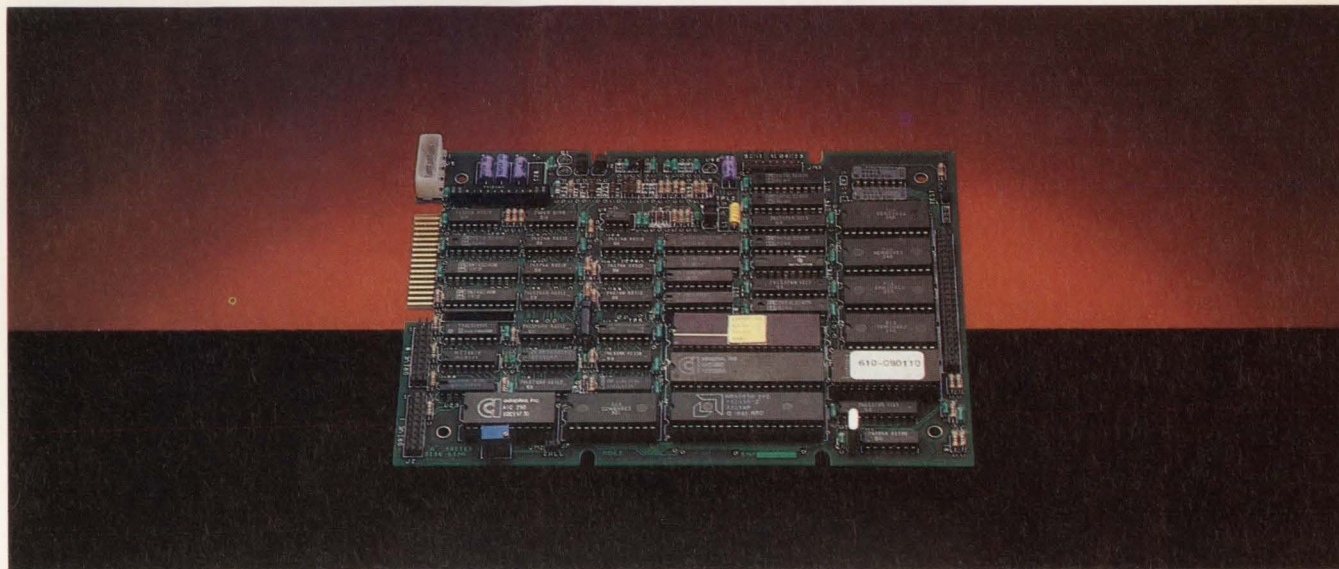
electronic mail. Unit is based on an LSI 11/23 processor and comes std with 256K bytes of RAM, 1M-byte flexible disk, 13.5M-byte hard disk, two user ports, and two line printer ports. RAM is expandable to 512K bytes or 1M byte. The device is priced at \$12,000. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077. Circle 286

### Color development system

CPP18S695 microboard computer provides software development for any CDP1802-based system in assembly or floating point Basic 3. Software features include ROM-based editor, ROM-based assembler, ROM-based monitor including 13 utility commands, and a tape-based PROM programmer. Hardware has 4K bytes of RAM and up to 8K bytes of ROM. The system consists of a video, audio, keyboard interface board with 128 user-programmable characters, and a memory and tape I/O control module. In quantities of one to nine, the system is priced at \$1499. **RCA/Solid State Div**, Rte 202, Somerville, NJ 08876. Circle 287

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The DAVID also supports the new higher performance Winchester disk drives having anywhere from 8 to 16 heads. Each DAVID supports up to 2 ST506 drives. Additional features include 256 and 512 byte block sizes, overlapping seek capa-

bility and standard ST506 mounting holes. The DAVID is also equipped with mounting holes compatible with XEBEC's 1410.

### Host interface

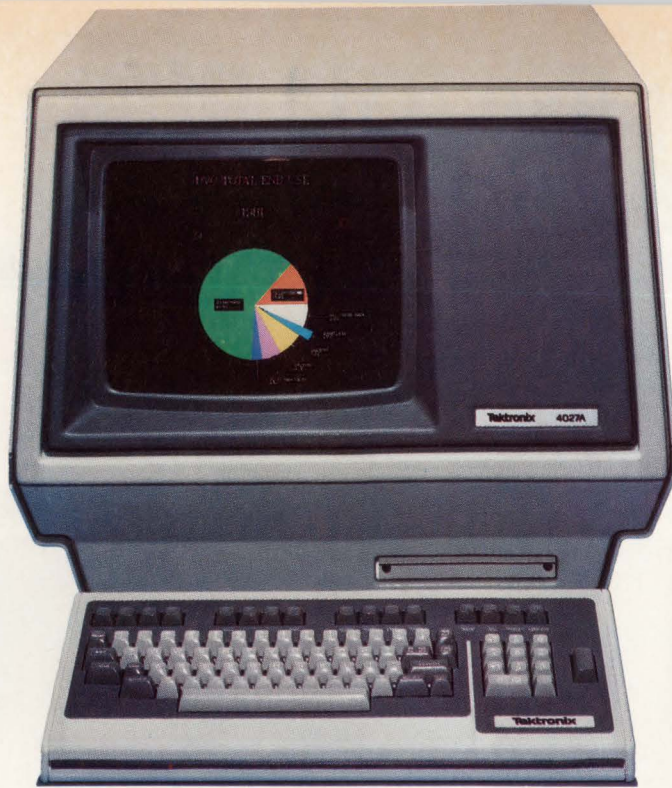
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## Getting Business Computing Together.

## Ultra-linear A-D converter

Model 3514 A-D converter is 1  $\mu$ s, 12-bit (4000 channel) and designed for gamma and X-ray spectroscopy. It offers 250 to 4000 channel conversion gains. Integral and differential non-linearities are better than  $\pm 0.0375\%$  and  $\pm 1\%$ , respectively. The unit operates in a peak detect mode with coincidence or anticoincidence gating or in a strobed sample mode for dc or slowly varying ac signals. Self-strobing permits sampling the input from 100 ns to 35  $\mu$ s after threshold crossing. Price is \$2495. **LeCroy Research Systems Corp**, 700 S Main St, Spring Valley, NY 10977. **Circle 288**

## Monolithic 12-bit DAC

The AD567SD DAC provides an output settling time to  $\pm 0.01\%$  in 500 ns max. The device provides a double-buffered data latch, a versatile micro interface, and a voltage reference. It accepts data in 4-, 8-, or full 12-bit words (for 12- or 16-bit bus compatibility) and is fast enough for any micro with minimum WR pulse width of 100 ns and zero hold time. Data and control inputs are TTL-compatible. Interface logic consists of

four independently addressable registers in two ranks that provide a double-buffered approach. The DAC is housed in a 28-pin cerDIP and costs \$59 to \$68 in 100s. **Analog Devices**, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. **Circle 289**

## Low cost A-D converter

ADC803 is a 12-bit A-D converter with a 1.5  $\mu$ s (guaranteed max) conversion time. Accurate to  $\pm 0.015\%$  of fsr, it operates with no missing codes over a  $-25$  to  $85^\circ\text{C}$  temp range and offers serial and parallel output. Input scaling resistors provide internal selection of analog input ranges of 0 to  $-10$  V,  $\pm 5$  V, and  $\pm 10$  V. The internal D-A converter drives a comparator input separate from the input signal so the driving circuitry does not have to handle large fast transients. In 25s, the price is \$214. **Burr-Brown**, Box 11400, Tucson, AZ 85734. **Circle 290**

## High accuracy converter

Model IDC-35303, a 4000-count inductosyn/resolver to digital converter, has an accuracy of  $\pm 8.5$  min with 1 LSB repeat-

ability. It operates over the reference and signal frequency range of 2 to 22 kHz with a 150-rps tracking rate. A control transformer algorithm provides higher accuracy and jitter-free output. The device measures 3.125" x 2.625" x 0.42" (7.938 x 6.668 x 1.07 cm) and weighs 4 oz (113 g). Depending on the model, the converter operates over 0 to  $70^\circ\text{C}$  or  $-55$  to  $105^\circ\text{C}$ . The price is \$245. **ILC Data Device Corp**, 105 Wilbur Pl, Bohemia, NY 11716. **Circle 291**

## Micro interface ADC

TSC7135 A-D converter outputs data in a multiplexed BCD format. The chip offers auto-zeroing, sign-magnitude coding, noise averaging, and high impedance inputs. Strobe output reduces the number of I/O port pins required to interface a converter to a micro through the use of software register counters. This method results in slightly faster interrupt response, as the micro does not have to loop while identifying each digit. **Teledyne Semiconductor**, 1300 Terra Bella Ave, Mountain View, CA 94043. **Circle 292**



GRAPHICS-PLUS is a field installable enhancement board for the popular Zenith<sup>1</sup> Z19 video terminal adding many powerful features found only on terminals costing much more. GRAPHICS-PLUS provides Tektronix<sup>2</sup> 4010 compatible vector drawing graphics, VT100<sup>3</sup> compatible 80 and 132 column display formats, off-screen scrolling memory, programmable function keys, "Plain English" menu-driven Set-up mode, and a host of other enhancements. Installation can be accomplished within 15 minutes using only a screwdriver.

## GRAPHICS-PLUS an enhancement For Z19 Terminals from Northwest Digital Systems

- Tektronix<sup>2</sup> 4010 Compatible Graphics
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- 80/132 Col and 24/49 Line Text Displays
- Seven Page Off-Screen Text Memory
- Menu-driven "Plain English" Set-up Mode
- 16 Programmable Keys- 128 Chars Each
- Optional Hardcopy Port
- Simple Field Installation

1 TM Zenith  
2 TM Tektronix  
3 TM DEC

GP-19 Upgrade for Z19 Terminal	\$ 849
Z19 Terminal With GP-19 Installed	\$ 1495

Northwest Digital Systems

P.O. Box 15288, Seattle, WA 98115 (206) 362-6937

## Nonimpact page printers

HP 2687A desktop text printer and HP 2688A text and graphics printer are nonimpact models based on laser printing technology. They use std sheets of A4/B paper and each prints at 12 pages/min, 300 dot/in. The printer noise level is less than 55 dBA. The 2687A allows up to four character fonts/printed page and has

word processing features. When used with word processing software, the 2688A generates documents, charts, graphs, and diagrams. A max of 32 character fonts can be combined on one page. The 2687A is priced at \$12,800, while the 2688A is \$29,950. **Hewlett-Packard Co.**, 1820 Embarcadero Rd, Palo Alto, CA 94303. Circle 293

## Cost effective sonic digitizing is here.



### SAC® GP-8.

You asked for it, and here it is: The new technology and packaging of our Graf/Bar\* GP-7 digitizer combined with the proven capability of the L-frame microphone array used with our GP-3 and GP-6 series digitizers. Now we've packaged these components as the new Model GP-8 sonic digitizer with the following new features:

- Five-function menu.
- Two-way communication.
- Computer control.
- RS-232, BCD parallel, or binary parallel interface.
- Remote trigger capability.
- Optional 16-digit display.

The GP-8 with active areas up to 60" x 72" features an eight-bit microprocessor which permits the system to perform five program functions via menu entry, including ORIGIN, LINE, METRIC, STREAM, and CANCEL. Either stylus, cursor with cross-hairs, or both may be used with the GP-8 to take data and to make menu selections.

The L-frame microphone sensor assembly borders the active work area, allowing interaction with a variety of images

such as CRT and plasma displays, projections from x-rays and films, maps or drawings on drafting tables, and graphic systems for CAD/CAE/CAM. The L-frame requires no special digitizing surface, resulting in a transparent, unencumbered work area.

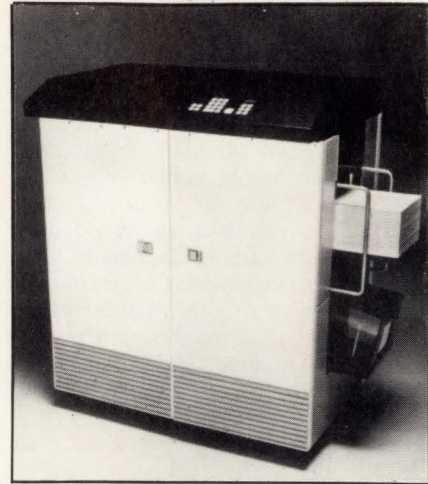
All said, the GP-8 quickly and economically allows the conversion of graphic information into numerical or digital form for convenient input in data processing, recording, or transition equipment. A typical GP-8 system includes a user provided host computer, as shown.

**The new GP-8 has brought the reality of state-of-the-art digitizing closer to you. It's a 36" x 36" active area for under \$2,000.00! And now's the time to let us tell you all about it. We're Science Accessories Corporation, 970 Kings Highway West, Southport, Connecticut 06490, (203) 255-1526, Telex 964-300.**

\*Trademark of Science Accessories Corporation.

**SAC® SCIENCE ACCESSORIES CORPORATION**

## Remote nonimpact page printer



Model 8360 ion-deposition printer outputs at speeds to 60 pages/min without tele-processing software. The Pixnet communication system enables remote users to access the host computer's printer at speeds up to 57.6k bps over satellite or analog/digital lines. Ion-deposition technology uses a noncontact ion projection cartridge which charges an image cylinder; then paper and toner are pressed together to complete printing. The model is priced at \$80,000. **Paradyne Corp.**, PO Box 1347, 8550 Ulmerton Rd, Largo, FL 33540. Circle 294

## Dual-mode printer

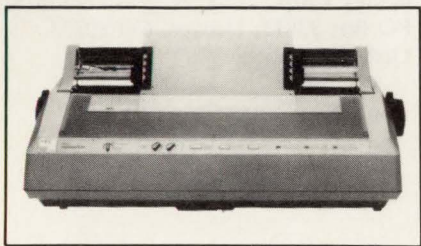
Omni 800 model 855 dot-matrix printer provides both letter and draft quality printing. In the draft mode, the printer offers a 150-cps speed. With a button or software command, an electronic daisy wheel can be selected. Three fonts can be used simultaneously so the user can switch print styles without stopping. It delivers 35-cps printing using a 32 x 18 dot-matrix format in the letter quality mode. The printer is capable of printing an original and two copies and can accommodate paper from 3" to 11" in length. Prices range from \$935 to \$995. **Texas Instruments Inc, Data Systems Group**, PO Box 402430, Dallas, TX 75240.



Circle 295

### Letter quality printer for IBM PC

Compatible with the IBM PC and its application software, the Spinwriter 2050 attaches to the parallel printer port and is functional for both data and word processing applications. It prints normal text at a speed of 20 chars/s. Form handling options accommodate single bin sheet feeder and add-on second bin or envelope feeder, unidirectional forms tractor, and bidirectional forms tractor. The thimbles can hold up to 128 chars and print two different type faces. The Spinwriter is priced at \$1250. **NEC Information Systems, Inc.**, 5 Militia Dr, Lexington, MA 02173.



Circle 296

### Enhanced cursor

Apache electro-optically aided cursor automatically corrects common operator positioning errors, while increasing tracing speeds. Added to the cursor is a 16-button multifunction keypad, display bar for system status and operator prompts, and an optional interface. Operators can auto digitize lines as fine as 0.004" and as wide as 0.09" in the correcting mode. Keypad allows a choice of operations such as point or stream mode, rate or vector (incremental) distance mode, and a digitizing rate of 1 to 100 points/s. The cursor is priced at \$18,000. **Atek Corp.**, 2150 Industrial Pkwy, Silver Spring, MD 20904.

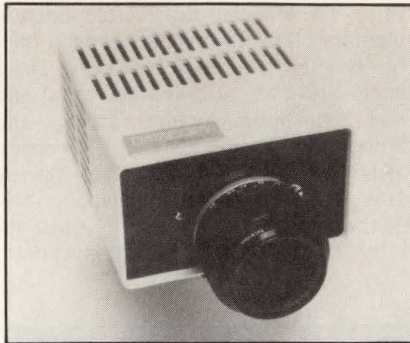
Circle 297

### RS-232-compatible joystick

Model 232 RS-232 joystick is designed for almost any business or graphics application. Joystick offers precision-tracking rates up to 19.2k baud, twice the speed of control alternatives. The smart device is programmable via erasable PROM. Cursor-related functions are assigned to joystick positions, permitting it to perform like a command keyboard. Device communicates in ASCII and plugs into a std 3- or 5-wire RS-232 port. All joystick components are available individually for easy custom operation. Model 232 sells for \$395. **KA Design Group**, 6300 Telegraph Ave, Oakland, CA 94609.

Circle 298

### Image processing camera



Model 610 is an electronic digitizing camera allowing complex images to be entered into a desktop computer without the use of a keyboard. The camera requires little illumination and the desired image is captured through a std 35-mm camera lens. Inside, there is a linear array of 1728 solid state photosensors which are moved across the image. The image is then organized into 4.9M pels and then digitally converted. In addition to the camera, the Model 110 image processing interface is available for the IBM PC with additional interfaces planned. **Datacopy Corp.**, 1070 E Meadow Cir, Palo Alto, CA 94303.

Circle 299

### Remote plotting for PDP-11, VAX

Emulating Hasp or 3780 workstations, Versatec electrostatic remote plotting systems support binary sync communication protocols. Configuration includes remote plotting controller, random element processor, plotting software, and any Versatec printer/plotter. Two software systems, Versaplot and Versaplot Random, enable plotting using commercial graphics packages. The random software package reduces data at a seven-to-one ratio. Plotting systems are priced from \$6500 and printer/plotters are priced from \$8950. **Versatec, a Xerox Co.**, 2710 Walsh Ave, Santa Clara, CA 95051.

Circle 300

### Share your knowledge

*Other system designers face the same problems you've already solved. You could help them by writing a technical article for Computer Design. For a free copy of our Author's Guide, circle 503 on the Reader Inquiry Card.*

### Color terminal/display station

The 215 color text/graphics terminal offers color graphics and alphanumeric capabilities. The 239 color graphics display station with a 19" screen, local graphics processing capability, and high resolution color display, was designed for tabletop or rackmount configurations. The 215 has a 640 x 409 resolution and can display eight colors from a palette of 64. A 16K x 16K-byte address space and graphics primitives and characters are provided. It is priced at \$3450. The 239 offers 640 x 480 resolution, local display list processing, and hardware pan and zoom. It is priced at \$9450. **Envision**, 631 River Oaks Pkwy, San Jose, CA 95134.



Circle 301

### Portable data recorder

A data capture device, called the Portable Data Recorder, simplifies and speeds a broad range of data collections. Information is read from an 80-char full alphanumeric LCD. Data are entered via a fully programmable 70-key keyboard. Other features are 128K bytes of memory (expandable to 256K bytes), and printer and data comm interfaces. The device measures 11" x 7" x 1.5" (28 x 18 x 3.8 cm). **General Instrument Corp.**, 1775 Broadway, New York, NY 10019. Circle 302

### DEC-compatible display

Model 102 display terminal is compatible with DEC VT100 and VT102. It also supports Tektronix 4010/4014 compatible graphics with added graphics card. Std features include a 14" green phosphor screen, tilt/swivel display, DIN std keyboard, eight programmable function keys (shift 16), buffered aux port, and 10- x 12-char matrix. Graphic enhancements include circle and arc draw and fill. Graphics option card provides 768 x 293-pixel resolution on a 50/60-Hz non-interlaced display. The 102 is \$1095; graphics card is \$895. **Visual Technology Inc.**, 540 Main St, Tewksbury, MA 01876. Circle 303

## Dual-mode Hazeltine/DEC terminal

Model 100/1500 emulates both the Hazeltine 1500 series and the DEC VT100 series of units. Terminal can replace Hazeltine terminals in situations where a change to ANSI controls is needed. In ANSI mode, it emulates the VT100 series except for VT52 compatibility. It provides 132-col x 24-line display, block transmission, bidirectional RS-232 port,

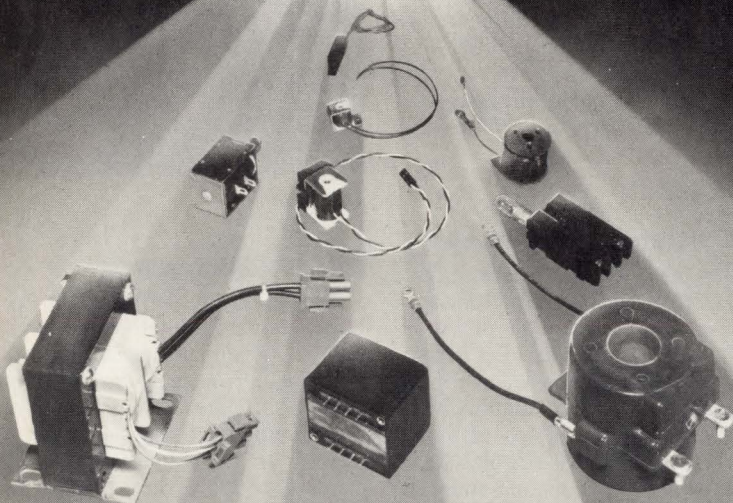
256-char input buffer, and smooth scroll rates. The 880-char nonvolatile function memory offers 20 keyboard programmable functions on dedicated keys. Three enclosures (9", 12", and 15" CRTs) and CRT phosphors (white, green, and amber) are available. The 12" version sells for \$1745. **Research Inc, Teleray Div**, PO Box 24064, Minneapolis, MN 55424. **Circle 304**

## CAD/CAM graphics workstation

The AGW II is a low end desktop version of the advanced graphic workstation. It offers full-function, 32-bit graphics processing and is compatible with the existing advanced graphics workstation family. Included are a standalone 32-bit central processor, virtual memory operating system, and either Auto-trol series 5000 or 7000 graphics software. The workstation contains a 17" black and white raster display monitor with a 1024- x 800-pixel resolution. Two serial RS-232 ports are std, and the unit has a 1.2M-byte floppy disk. The workstation is priced under \$60,000. **Auto-trol Technology Corp**, 12500 N Washington St, PO Box 33815, Denver, CO 80233. **Circle 305**

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CIRCLE 140

## DATA COMMUNICATIONS

### Terminal-accessible catalog

VideoLog is a videotex product catalog for the electronics industry. The system is accessible by dumb ASCII terminals, personal computers, and NAPLPS terminals. The system will be expanded to include an online directory of all manufacturers of electronic components, equipment, and services. The service will be mainly advertiser supported, therefore online charges to users will be less than \$0.17 per minute. Products and specs can be placed on the system in 24 hours. **Videotex Information Corp**, 213 Danbury Rd, Wilton, CT 06897. **Circle 306**

### Single-board LAN protocol software

A high level protocol software package, the TCP/IP is for use with the Excelan 101 Ethernet frontend processor. The package consists of two parts: a TCP/IP protocol module and a Unix system networking kit. The protocol module is an object module that loads into the processor, independent of the host CPU or operating system type. It provides a generalized interface for any host hardware/software architecture and gives the host access to all protocol layers. The Unix kit includes a simple I/O driver for the protocol module and networking application programs. The software license is priced at \$10,000. **Excelan**, 2180 Fortune Dr, San Jose, CA 95131. **Circle 307**



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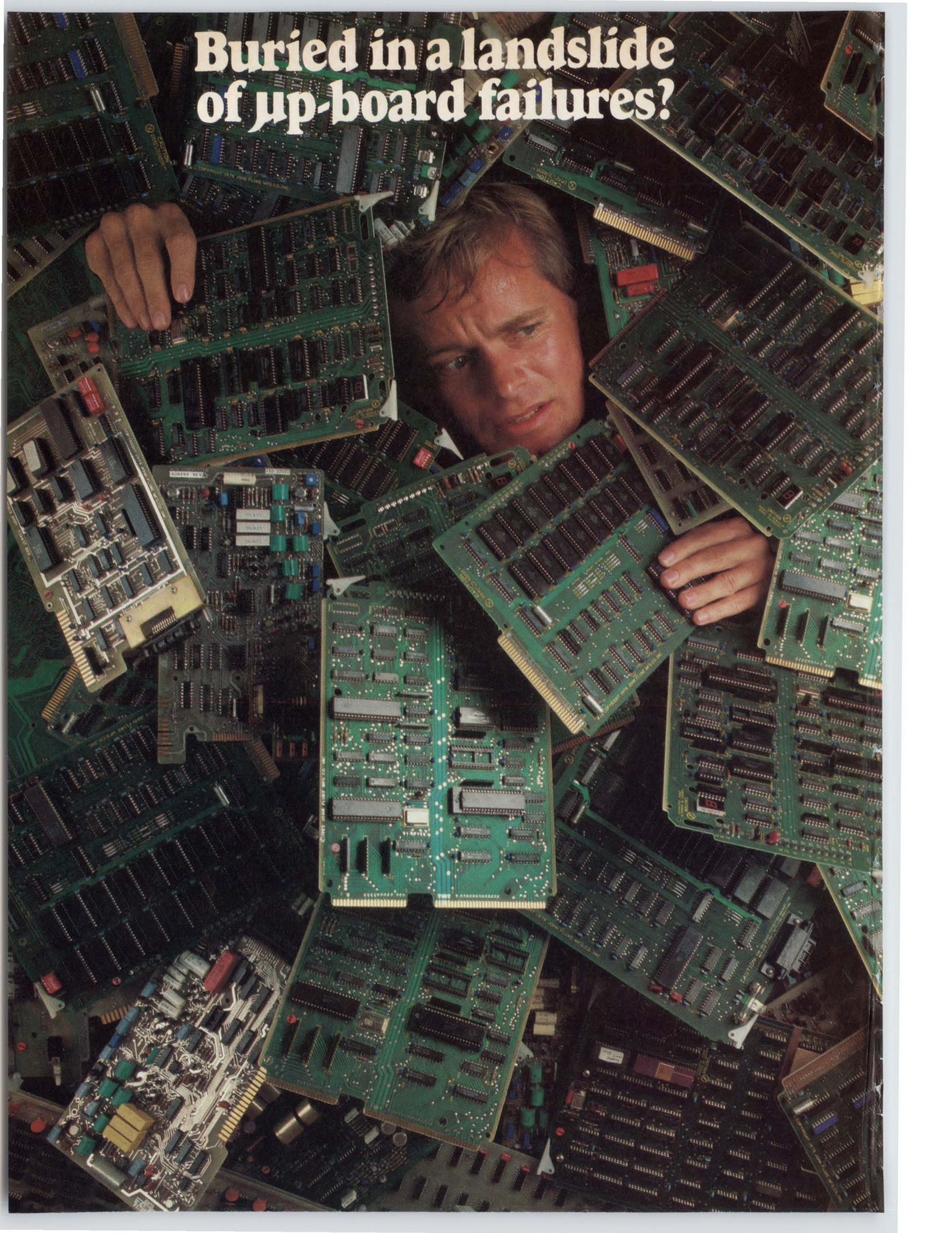
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*Diagnostic messages explain faults in plain English on the alpha-numeric display.*

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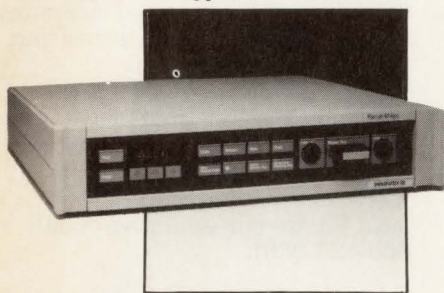
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For technical data circle number **142**

## Link data encryptor



Datacryptor III secures data over point to point wideband circuits at data rates up to 112k bps. Operating synchronously on full-duplex leased line facilities, it is equipped with both V.35 and RS-232 interfaces wired in parallel. Features permit key management and diagnostics to be controlled from the front panel and remote diagnostics to be performed unattended. The device uses the DES algorithm in the single-bit cipher feedback mode, which provides complete protocol transparency. Price is \$4995. **Racal-Milgo**, 8600 NW 41st St, Miami, FL 33166. **Circle 308**

## Micro mainframe link

DecisionLink/34 data gateway system links personal computers to the IBM system 34. The bidirectional interface uses async communication to link up to 16 PCs to the mainframe. Data files can then be selectively transferred from the mainframe to the PC and back again. The system includes an intelligent front-end controller and software modules. Interfacing occurs through a single SDLC comm channel. The controller communicates via async modems or local cable connections. **Laguna Laboratories, Inc**, 1300 Normandy Pl, Santa Ana, CA 92705. **Circle 309**

## Answer-only triple modem

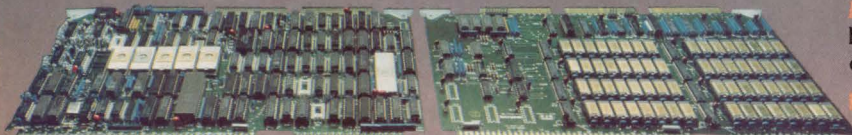
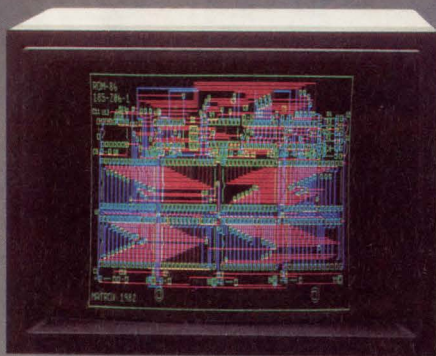
DSM/Triple modem automatically responds to Bell 212A, Bell 103, and Vadic VA3400 originating modems. The rack-mount answer-only unit handles serial binary data at 1.2k bps sync, async at 1.2k bps, and 0 to 300 bps. Character lengths run from 8 to 11 bits. The internal micro implements a modem detect

algorithm that determines the type of unit starting the call, and automatically switches to a compatible mode. Diagnostics include local, end-to-end tests, and analog and digital loopbacks. **Infotron Systems Corp**, Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003. **Circle 310**

## Local data distribution MUX

The CCM cable MUX supports up to 32 Type-A IBM terminals and printers over a single coax cable to an IBM 3274 controller. For terminal relocation the device requires additional cable only between the terminal and the nearest MUX, making installation and expansion quicker and easier. Std channel speed is 2.358M bps. Terminals can be placed up to 2952' (900 m) from the MUX unit and linked to another unit located up to an additional 4920' (1500 m) away. Purchase price for the standalone unit is \$1100 and for the 32-port CCM, \$3350. **Codex Corp, sub of Motorola Inc**, 20 Cabot Blvd, Mansfield, MA 02048. **Circle 311**

## COLOR GRAPHICS BOARDS



### MATROX GXB-1000 - The complete color graphics solution.

The GXB-1000 is a complete color graphics display system implemented on two Multibus boards. The system executes a display file containing high level graphics commands, generated by the user's host CPU. The GXB-1000 includes all the necessary hardware and software to draw lines, polygons, circles, characters, etc.

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Multibus - TM Intel, \*QTY 100

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**SPEED:** Four on-board processors draw graphics primitives at 50 to 800 nsec/pixel

**COLOR:** 16 display colors from a palette of 256

**SOFTWARE:** On-board 16 bit CPU with resident graphics software interprets over 256 commands

**MODULARITY:** GXB-1000 is fully Multibus compatible (IEEE-796), and requires only +5V

**PRICE:** \$3225.00 complete\*



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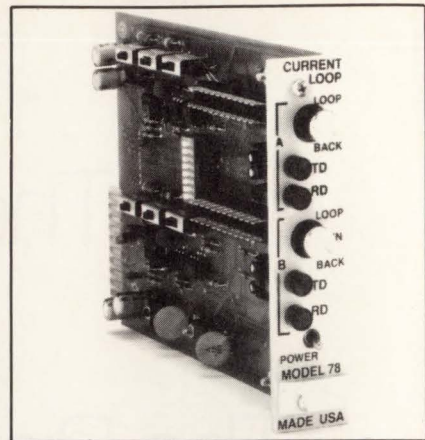
**(503) 226-7760**

**Fiber optic modem**

Biolink 1 is a full-duplex async fiber optic modem that operates bidirectionally over a single fiber. The modem is EIA RS-232-C and CCITT V.24 compatible. A 20-mA current loop and TTL interface are strap selectable. Data rate is 100k bps max up to 4 km. Bit error rate is 10<sup>-9</sup> or

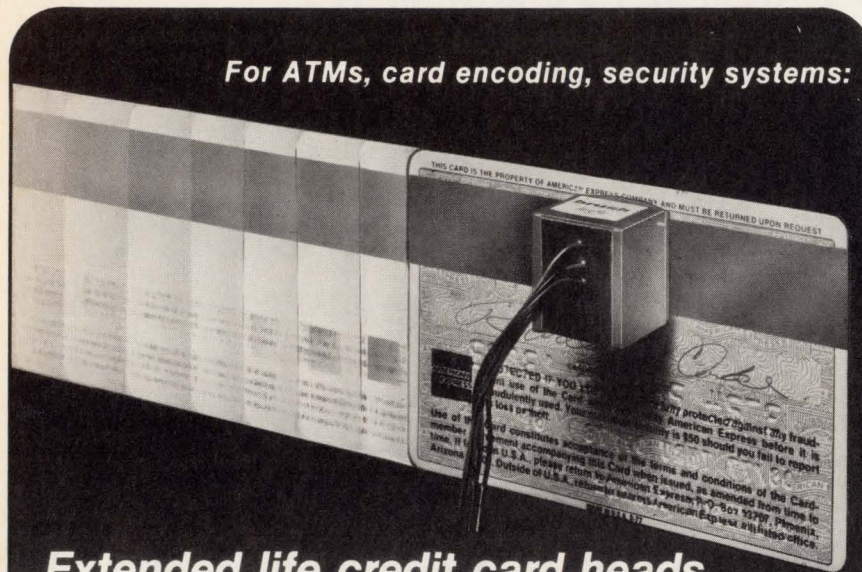
better. Power supply suppresses line transients and emi/rfi. It is intended for use with a 200-micron core plastic clad silica fiber. Unit price is \$600; in quantities of 50 or more, the modem is \$500. **GTE Atea, Optolab Div, Atealaan, B-2410 Herentals, Belgium.**  
Circle 312

**Modular converter with LANs**



Model 78 dual current loop converter supports the need for LANs based on star or ring topology. It features two independent converters on one module. Each converter uses a loopback switch and transmit and receive data indicators. The switch loops the RS-232 back on itself through the current loop circuitry thus testing total operation. Operation is provided for both 20 mA and 60 mA loops up to 9.6k baud. Unit price is \$195 with quantities of 100 selling for \$156. **Telebyte Technology Inc, Remark Datacom Div, 148 New York Ave, Halesite, NY 11743.** Circle 313

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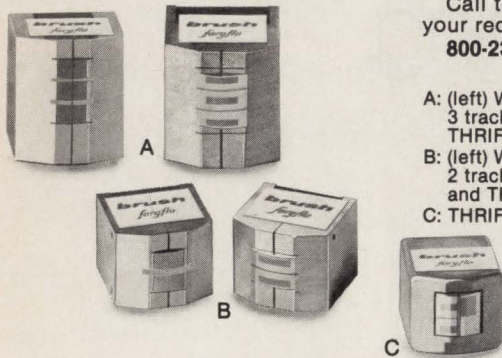
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**LAN to PC interface**

The PN-IBM is an interface card for the IBM PC providing LAN capabilities. It plugs into the host computer, then is linked to the network through the cable interface. Features include token-passing reliability, built-in 64K-byte FIFO buffer, signal regeneration at each node for high signal to noise ratios, and NBS encryption for data security. Operating system compatibility is provided for MS-DOS, CP/M, and Unix. Operation occurs over 10,000' at 1.0M bps. **Percom Data Corp, 11220 Pagemill Rd, Dallas, TX 75243.** Circle 315

## Voice/data modem

Local area Adminet modem transmits both voice and data simultaneously over std unconditioned telephone lines. The modem operates full- or half-duplex at speeds up to 9.6k baud. Auto-baud ability allows the device to adapt to any data rate. Protocol transparency to any character code makes the unit compatible with async terminals. It is implemented on a custom designed LSI circuit integrated with thick film hybrid technology. The devices cost \$449 per pair. **Adminet Inc**, 27 Goulburn Ave, Ottawa, Canada K1N 8C7. Circle 316

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## CONTROL & AUTOMATION

### Heavy-duty encoder

Developed with opto-electronic technology, the series 25 incremental encoder can be used in process control, robotics, machine tools, and automation equipment. The encoder is housed in a cast metal frame and uses environmental seals. Options and features include resolutions to 2540 pulses/revolution plus index; frequency response to 100 kHz; 5-, 12-, or 15-Vdc power input; open collector, TTL, or line driver outputs in single-ended or complementary configurations, and a std flat on the shaft. **Disc Instruments**, a sub of **Honeywell Inc**, 102 E Baker St, Costa Mesa, CA 92626. Circle 317

### Process transmitter

ST 3000 smart transmitter is based on three basic sensors providing the pressure sensor range previously covered by 11 transmitter sensors. The transmitter allows recalibration from the control room or field. Using a handheld touch pad, operators can tap into the system

and alter pressure sensing requirements. Each transmitter consists of a sensor, custom ICs, and a microprocessor. A transmitter contains one of three sensors: 400" of water full scale, 500 psi or for 10,000 psi. **Honeywell Inc**, Honeywell Plaza, Minneapolis, MN 55408. Circle 318

### Visual processing VME subsystem

DSSEIMAG-56 VME-bus image-processing subsystem uses the 68000 micro and can be used in automatic visual applications. These include measuring, counting, routing, and quality inspections. The image display can be used in realtime or in a digitized image from memory. The subsystem contains an acquisition board, an image memory board, a display board, and an image processing software library. The CPU on the memory board allows storage and processing without display interaction. The subsystem is priced at \$7500. **Data-Sud Systems/US, Inc**, 2219 S 48th St, Tempe, AZ 85282. Circle 319

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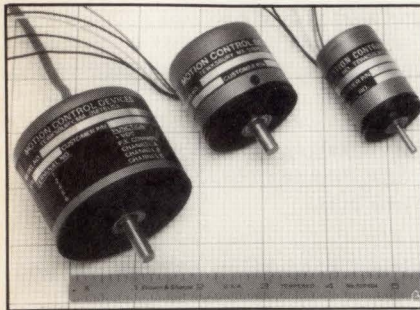
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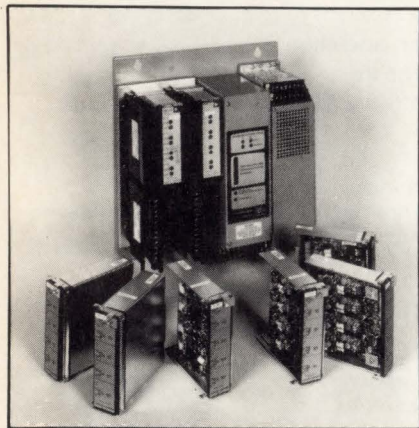
## Miniature encoders



The 80 series of encoders is expanded with a size 11 model (1.1"/2.8 cm) and a size 15 model (1.5"/3.8 cm). The miniature self-contained encoders offer solid state LEDs coupled with signal sensing silicon solar cell arrays, which are the optical system's building blocks. Array minimizes the effect of eccentricity and shaft loading. Square wave TTL or CMOS complementary outputs are offered at 5 to 15 V. Prices start at \$100. **Motion Control Devices, Inc.**, 80 Stedman St, Lowell, MA 01851. **Circle 320**

## Analog MUX modules

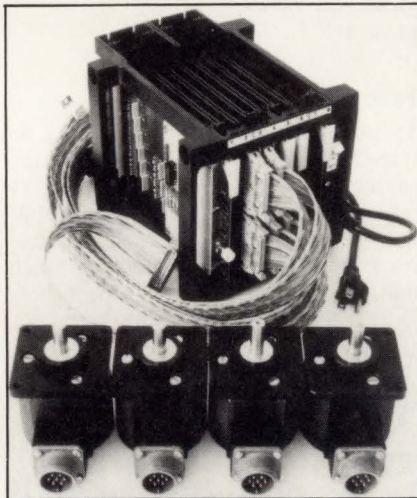
Three input modules electrically compatible with Directrol MUX stations have source signal ratings of 1 to 5 Vdc (4 to 20 mA or 10 to 50 mA with shunt), 0 to 5 Vdc, or 0 to 10 Vdc. Inputs accept common industrial-level analog signals, digitize them, then send them to the communication link. Output modules are available in 4- to 20-mA, 0- to 5-Vdc, and 0- to 10-Vdc output signal configurations. They produce analog outputs proportional to digital data received on the communication link. Both module types feature four signal/module capacities and 12-bit resolution. **Eaton Corp., Cutler-Hammer Products**, 4201 N 27th St, Milwaukee, WI 53216.



Circle 321

## Remote MUX via RS-232-C

C-1020 remote MUX provides accurate position measurement over long distances. It plugs directly into a 120-Vac power main and keeps track of up to four axes. Optical incremental encoders derive position information and 16 TTL-compatible digital inputs can sense states of switches, contacts, and faults. The device offers bidirectional measurement of linear or rotary displacement. Internal buffering enables the computer to read clean position data at any time. Position measurement accuracy can be as high as one part in 4.3 billion. **Buckminster Corp.**, 99 Highland Ave, Somerville, MA 02143.



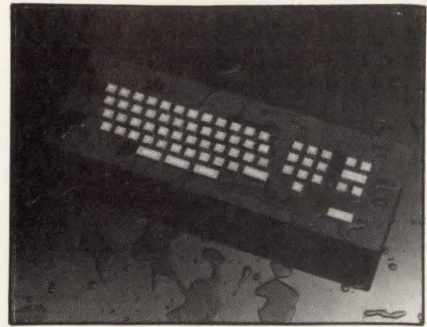
Circle 322

## Automation monitoring language

Display generator language is an English language operator's interface that automatically directs a user through correct programming procedures. It has menus, operator assistance messages, and labeled function keys. The language is similar to Basic and lets the user compose, compile, and run a program from any terminal, or direct it to a printer. It is available with all Logicon factory automation systems that operate under RSX-11M and RSX-11M-PLUS. **Logicon, Process Systems Div**, 10398 Democracy Ln, Fairfax, VA 22030. **Circle 323**

## Micro-based keyboard

MAKB-1 is a 64-function ASCII keyboard for harsh environments. Keyboard is microprocessor-based for interfacing with the host system using serial or parallel ASCII codes. Completely sealed with emi/rfi shielding, the device is tested to MIL-STD-810 for -35 to 55 °C operating temps, humidity 5% to 95% at 65 °C, rain



tested, vibration (operational 0 to 500 Hz), and shock to 40 G. Switch actuation force is 300 G  $\pm$  100; switch travel is 0.045"  $\pm$  0.015" (1.143 mm  $\pm$  0.381 mm) using snap action dome technology and gold contacts. Board is available for \$1160 in quantities of 500. **Industrial Electronic Engineers, Inc.**, 7740 Lemona Ave, Van Nuys, CA 91405. **Circle 324**

## Operator interface

The RacPac terminal's 19" rackmount enclosure houses a 9" monochrome video display, terminal control electronics, and a power supply. An RS-232-C interface and built-in 28-key sealed membrane keypad with audible feedback are std. Optionally, 20-mA, RS-422-A, and RS-423-A interfaces, as well as a detachable full-size keyboard, are available. The terminal can display 16 thin line and 64 block graphics characters, 33 ASCII 2-letter control codes, and 95 alphanumeric characters. **Xycom, Inc.**, 750 N Maple Rd, Saline, MI 48176. **Circle 325**

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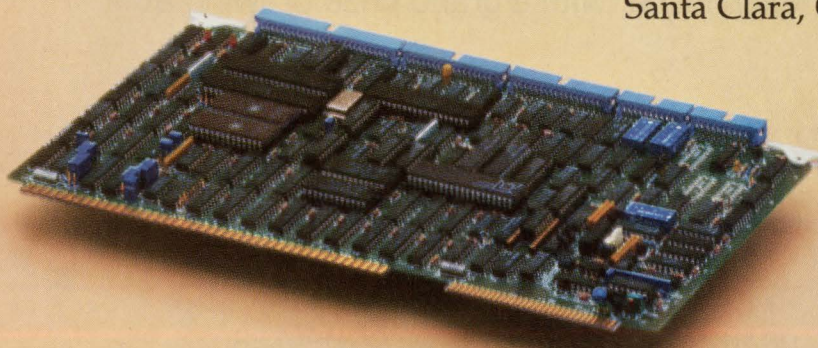
On the other hand, you could use a controller that's especially built to wring every last bit of performance out of supermicros.

DSD's RAMTRAC controller.

It controls Winchesters, floppies and tape. All on a single MULTIBUS board.

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Our line of three RAMTRAC controllers emulate Intel's® iSBC® 215, iSBX™ 217 and iSBX™ 218. And they're compatible with all SA460-, SA850-, SA1000-, and ST506-type drives.

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Winchester	5¼"	5¼"	8"
Floppy	5¼"	8"	8"
Tape	QIC-02	QIC-02	QIC-02

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Eastern Region Sales and Service: Norwood, MA, (617) 769-7620. Central Region Sales and Service: Dallas, TX, (214) 980-4884. Western Region Sales: Santa Clara, CA, (408) 727-3163.

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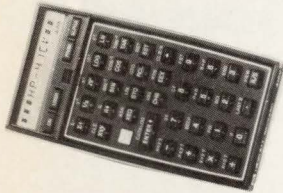
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### **MONTHLY DRAWING — HP 41CV PROGRAMMABLE CALCULATOR**

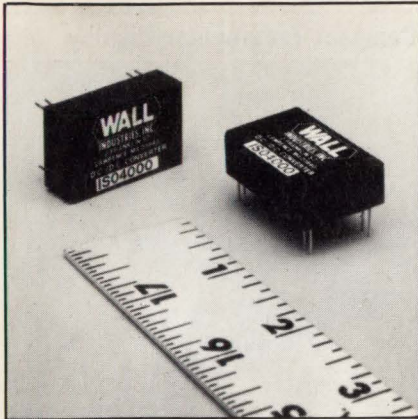
The HP 41CV offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total functions in program library. Memory expandable to almost 6,500 bytes.



### **ANNUAL DRAWING — HP 85 DESK TOP COMPUTER**

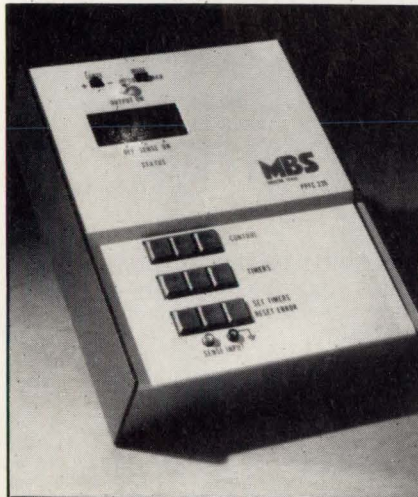
This portable (20 lb.) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56K byte memory, CRT screen, and 150 built-in BASIC language commands. You can add peripheral and software packages to expand system capability. A \$2800 value!

**Mini high isolation converter**



A dc-dc converter, the ISO-4000B features high I/O isolation in a 1.5-W package. An 80% efficiency is the result of circuitry with an oscillator frequency greater than 50 kHz. For short circuit protection, it uses power foldback. Applications include A-D and D-A converters, op amps, micros, memory, and analog to analog with isolation. The converter has a low profile and 24-pin DIP compatibility. Pricing starts at \$29.95. **Wall Industries, Inc.**, 2 Franklin St, Lawrence, MA 01840. Circle 327

**Simulation for power failures**



Model 235 programmable power fail controller provides essential data during development, production testing, service, and trouble shooting online microprocessor controllers. The controller features both auto and manual modes of operation, four-digit monitoring display, and a programmable control panel. It delivers continually changing repetition of timed power fail sequences. In addition, it can be used to identify intermittent power fail problems days or weeks apart. **Mini Base Systems**, 10857 Rockley Rd, Houston, TX 77099. Circle 328

**Rackmounted ac power supply**

The KB series combines a microcomputer control and measurement system with an ac power source. The internal measurements for single or multiphase systems provide verification of programmed output voltages, currents, and phase relationships and reports these via a fluorescent display and/or an IEEE 488 interface. A synthesized, crystal controlled sine wave oscillator combined with a linear power amp (100 VA to 54k VA) achieves output specs of less than 1% thd and 0.5% load regulation over selectable frequency ranges from 45 to 10k Hz. Units are priced from \$4775 to \$16,000. **Behlman Engineering Corp.**, 1142 Mark Ave, Carpinteria, CA 93010.



Circle 329

**Power for industrial environment**

The AN series of switchers provide up to 375 W of regulated dc power. The units are designed for 115 or 230 Vac, single phase, 50/60/400 Hz input, and can accommodate large line variations. One to four outputs are available providing the following voltages:  $\pm 5$  V,  $\pm 12$  V,  $\pm 18$  V,  $\pm 24$  V, and  $\pm 28$  V all dc. Protective features include input spike protection, 15-ms holdup for power fail, reverse polarity protection, emi suppression, soft start, and inrush current limit. **EG&G Almond Instruments**, 1330 E Cypress St, Covina, CA 91724. Circle 330

**High power switchers**

The XL750 family of 750-W power supplies use proprietary proportional drive and current mode design. It features single wire current sharing for parallel or redundant applications. Additional features include over current/voltage protection for each output, proportional drive, current mode, status indicators, overtemperature protection, and built-in cooling. All outputs can be used with either polarity. The switchers range in price from \$656 to \$825 in quantities of 250. **Boschert Inc.**, 384 Santa Trinita Ave, Sunnyvale, CA 94086. Circle 331



**The New Color Standard For VDT's.**

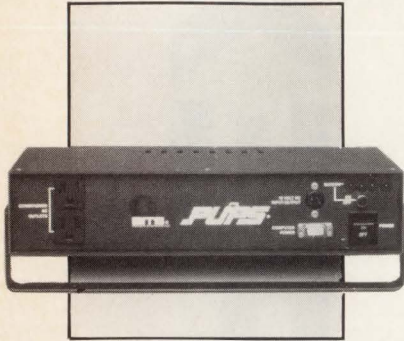
The eyes have it. Now the best-looking terminals are the best terminals to look at because they're in Ampex amber. Why amber? Because recent scientific research proves it to be 25% more relaxing on the eyes than green\*. As a result, West Germany, Norway and Sweden already prefer it in the workplace. And Ampex offers it as standard on our new Emulation Plus terminals. They not only emulate twenty models of other major manufacturers, they also offer you the amber the others don't. Open your eyes to amber. Call 213-640-0150. Ampex Corporation, Memory Products Division, 200 N. Nash St., El Segundo, CA 90245.

\*Data available on request.



CIRCLE 149

**Solid state portable power supply**



An uninterruptible power supply is designed for portable and desktop computers. The 115-V, 60-Hz isolated output ensures computer operations are not affected by utility gaps, spikes, surges, noises, or outages. Backup or portable operating time ranges from 5 hr at 25 W to 1 hr at 100 W. Input power is switch selectable for either 115 or 230 Vac, 50/60 Hz. Internal charging system is auto controlled and regulated. A 12 Vdc power cord is included. The price for the supply is \$495. **Bits Power Systems, Inc.**, 11020 Audelia Rd, Dallas, TX 75243. Circle 332

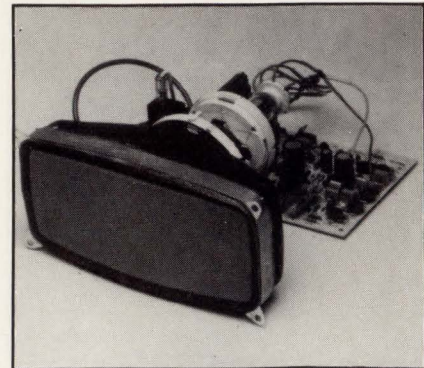
**Cost-effective switcher**

CE-35-102 is a 40-W power supply designed for terminal and PC applications. It features a 90- to 135-Vac, 47- to 440-Hz input. Std features include PC board construction, current inrush limiting, natural convection cooling, short circuit protection, 5-V overvoltage protection, 115-Vac operation, emi filter, and low noise geometry. Regulated dc outputs are 5 V at 3.5A, 12 V at 2.5 A and -12 V at 0.4 A. Base price is \$30 at 1000-piece quantities. **General Instrument Corp, Computer Products Div**, 401 Lomaland Dr, El Paso, TX 79935. Circle 333

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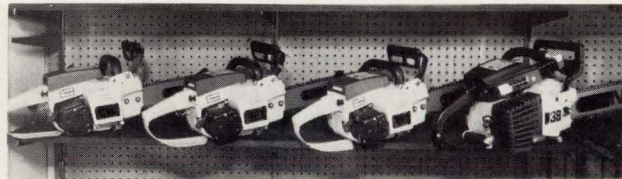
**SYSTEM ELEMENTS**

**Compact rectangular display**



The DTH-5900 CRT features a tube with a 29-mm neck and a 3" x 8" display area. The unit comes with any listed phosphor including European amber, in both frameless and wireframe versions. The UL/CSA approved display offers a bandwidth in excess of 35 MHz. Line rate can be specified in the range of 15.75 to 35 kHz. Power requirement is 24 Vdc at 35 W. **Dotronix, Inc.**, 160 1st St SE, New Brighton, MN 55112. Circle 334

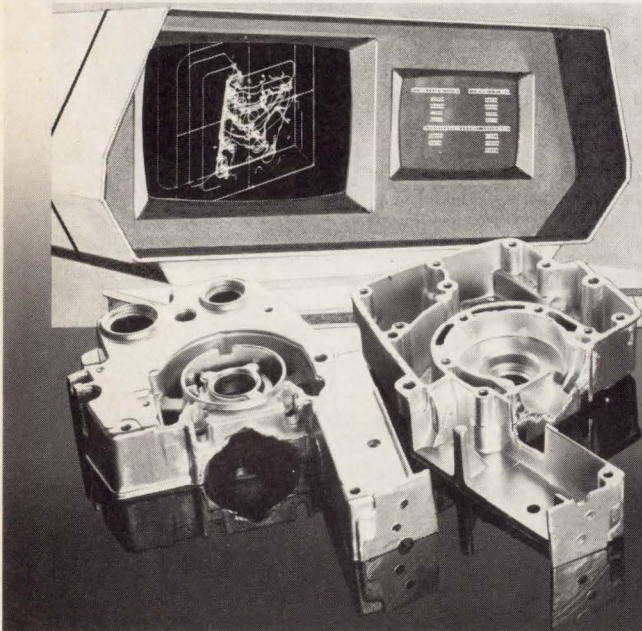
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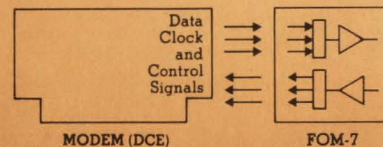
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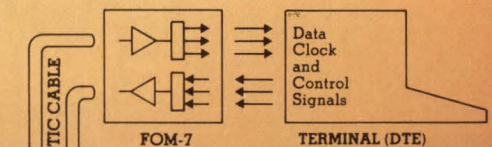
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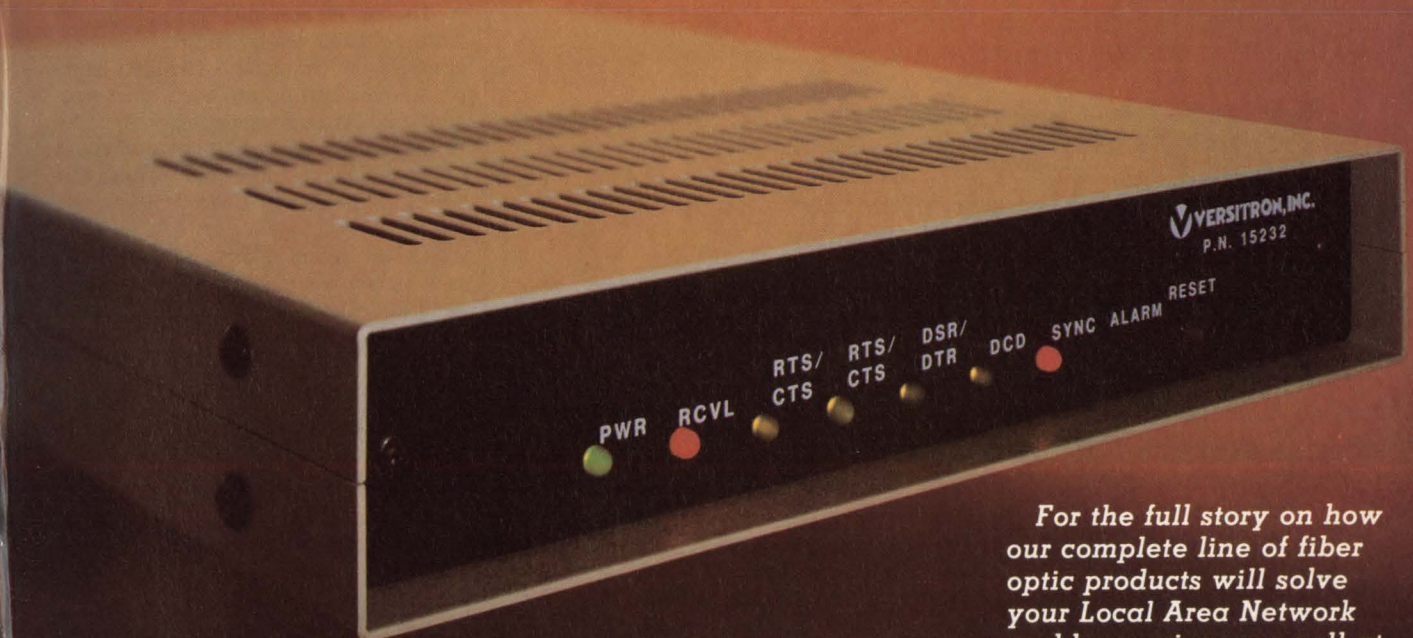
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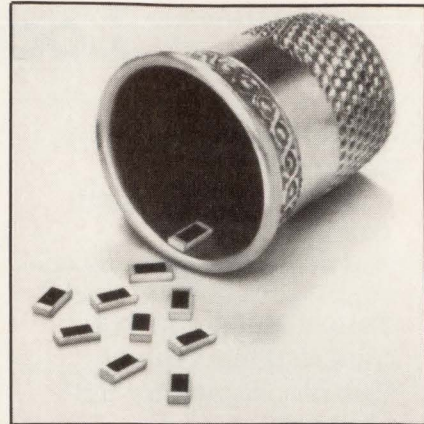
CIRCLE 151

## Low power multiplier/accumulator

Dissipating 150 mW at a 6-MHz clock rate, the ADSP-1012 multiplier and ADSP-1009 multiplier/accumulator specify max cycle times of 110 ns and 130 ns, respectively. The 12 x 12-bit multipliers guarantee operation over the full -55 to 125 °C ambient temperature range. Typical applications are in digital signal processing, including correlation, digital filtering, FFTs and matrix manipulation. All models are available in a 64-pin hermetically sealed cerDIP, a 68-pin pin-grid array, or a 68-terminal LCC. Prices range from \$80 to \$340 in 100s. **Analog Devices, Inc.**, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. Circle 335

processing, including correlation, digital filtering, FFTs and matrix manipulation. All models are available in a 64-pin hermetically sealed cerDIP, a 68-pin pin-grid array, or a 68-terminal LCC. Prices range from \$80 to \$340 in 100s. **Analog Devices, Inc.**, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. Circle 335

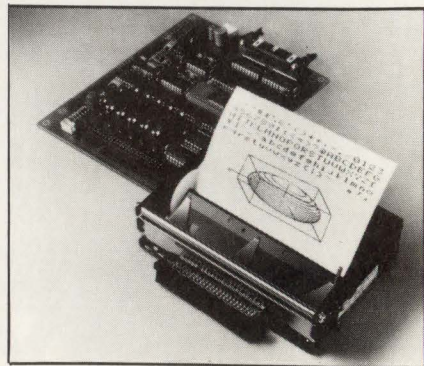
## Chip resistors



Series CRC are thick film chip resistors designed for high density surface mounting. Available in a 3.2 x 1.6-mm size the resistors offer a choice of two terminations: Model CRC (terminations and resistor elements on the same side) and Model CRCW (wraparound terminations). Nominal wattage ratings are 1/8 W at 70 °C; continuous working voltage is 200 V max. Std resistance range is 10 Ω to 2.2M Ω in ±2% and ±5% tolerances. Packaging choices include tape and reel, and bulk with prices in the \$0.05 range (per 5000). **Dale Electronics, Inc.**, PO Box 609, Columbus, NE 68601. Circle 336

## Mini printer

A 20- or 40-column thermal printer features fixed-head printing for clear graphics and characters. The light, compact models conform to Centronics standards and can easily mate to host systems. A fixed printing head allows virtually noise- and maintenance-free operation. In addition, the printers offer last-line visibility. Applications for the printers include measurement and analysis systems and personal computers. **Fujitsu America, Inc., Components Div.**, 918 Sherwood Dr, Lake Bluff, IL 60044.



Circle 337

# EZ-PRO II + IBM PC = WINNER



**EZ-PRO II**  
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**Start with IBM.** EZ-PRO II is a development station which connects to your personal computer via RS232. Use MS-DOS™ 2.0 and the IBM editor to generate source code and EZ-PRO II supplies the rest.

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CIRCLE 154

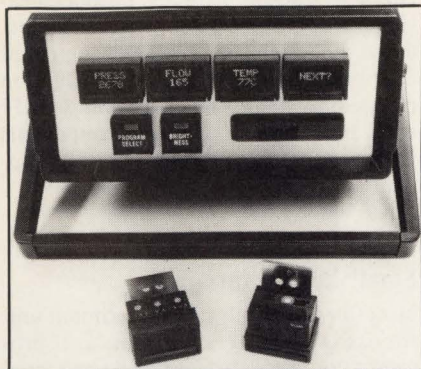


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**Interactive programmable button**



Display pushbutton is microprocessor based and has manual control for communication between operator and computer-based systems. Through interface with a logic and refresh control unit, the device is a combination of a solid state Hall effect pushbutton that sends information to a computer and a dot-matrix display that returns information to the operator. Each unit's display of 560 LEDs uses a 16 x 35-pixel array to display two rows of six chars (5 x 7 font) or one row of three chars (10 x 14 font). Cost of a single unit is \$495. **Micro Switch, div of Honeywell**, 11 W Spring St, Freeport, IL 61032. **Circle 338**

**Hybrid steppers**

PH26X stepping motors provide double the step angle accuracy of conventional 1.8 deg steppers. These motors feature 0.9 deg full steps and 0.45 deg half steps/pulse with  $\pm 3\%$  positioning accuracy. Stepping 400 times/360 deg revolution, the two-phase motors deliver 25 to 52 oz-in holding torque. In either bipolar or unipolar design, the motors come in 4, 6, 12, and 24 Vdc or custom configurations. Price depends on model, configuration, and quantity. **Oriental Motor New England Corp**, 101 Coolidge St, Hudson, MA 01749. **Circle 339**

**Subminiature toggle switches**

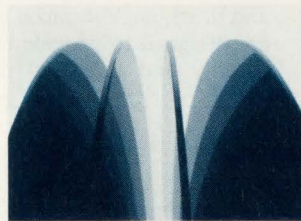
s series 10-A/125-Vac switches come in spdt, dpdt, 3-pdt, and 4-pdt in on-none-on circuitry. Two bushing sizes are offered: 6-mm threaded bushing with two hex nuts, locking ring, internal tooth lockwasher, and a slip-on white toggle cap; and 12-mm with two hex nuts, locking ring, and internal tooth lockwasher. Switches have silver-plated solder lug terminations and are insert molded into a heavy phenolic base. **NKK Switches of America, Inc**, 14415 N Scottsdale Rd, Scottsdale, AZ 85260. **Circle 340**

**Page scanning sensor**

CCD151 line scan sensor features a high resolution 3456 x 1 array, 7-micron pitch, and high sensitivity. Designed for page scanning applications, the sensing elements provide a 400-line /in resolution across an 8.5" page. Each photoelement is 7 x 7 microns on 7-micron centers. A

development board is also available that includes all necessary clocks, logic drivers, and video amps. The board is fully assembled and tested. The sensor is priced at \$1500 and the board is \$500. **Fairchild CCD Imaging**, 3440 Hillview Ave, Palo Alto, CA 94304. **Circle 341**

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**Fast octal drivers**

DP84240 and DP84244 are octal tri-state drivers designed to drive high capacitance dynamic RAM arrays. The 84240 is an inverting driver that is pin compatible with the 74S240, while the 84244 is non-inverting and is pin compatible with the 74S244. Outputs are specified at MOS switching levels (0.8 to 2.7 V). Symmetric rise and fall times specified at 500 pF minimize propagation delays. Other features include PNP inputs, low static and dynamic input capacitance, and glitch free power up/down. Available in both cerDIP and molded 20-pin DIPs, the devices are fabricated on the advanced low power Schottky process. **National Semiconductor Corp**, 2900 Semiconductor Dr, Santa Clara, CA 95051. Circle 392

**Stackable LEDs**

Series LR2057 2" (5-cm) character, 5 x 7 alphanumeric dot-matrix LEDs come in red, green, yellow, and orange. Gray face with translucent dots enhances the dead front appearance when panel is off. Each dot is X-Y selectable in multiplexed drive schemes. They are X-Y stackable, with

interlocking notches for full dot patterns. Features include high brightness, wide angle viewing, and uniform illumination. Price is \$4 in 100-piece quantities for the std red. **Industrial Electronic Engineers, Inc**, 7740 Lemona Ave, Van Nuys, CA 91405. Circle 342

**Toggle switches**

Series 571 (mini toggle switches), series 573 (PC mounted toggle switches), and series 577 (PC mounted with support brackets) are now available with a tapered, flattened toggle arm. Each series offers three lengths, the two longest having a diameter of 0.20" (5.08 mm) and the shortest with a diameter of 0.165" (4.191 mm). All are 0.10" (2.54-mm) thick. **Dialight, a North American Philips Co**, 203 Harrison Pl, Brooklyn, NY 11237. Circle 343

**Plastic replacement LED and sensor**

OP298, a GaAlAs infrared emitting diode and OP598, an NPN silicon phototransistor are designed to provide better lens uniformity and increased reliability over

hermetic units. The lead frame construction allows automation in unit production and improved optical qualities. Improved characterization includes output measured in aperture on axis power. The specified radiant incident power is improved over hermetic units due to the reduction of one optical interface. Pricing is \$0.53 each/1000. **TRW Electronic Components Group, Optoelectronics Div**, 1207 Tappan Cir, Carrollton, TX 75006. Circle 344

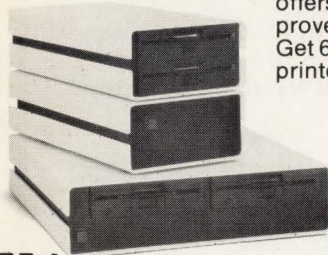
**Small hybrid terminal**

BUS-65101 is a dumb remote terminal unit for use in MIL-STD-1553 terminals. It provides a complete interface between a serial MUX data bus and a subsystem parallel tri-state data highway. The unit includes a transceiver, a Manchester II encoder/decoder, dual rank input and output storage registers, and internal clock oscillator. Output flags are provided when broadcast, mode code, and own address (with parity) are detected. Available in ±12 or ±15 Vdc models, it is priced at \$729 (one-to nine-piece quantity). **ILC Data Device Corp**, 105 Wilbur Pl, Bohemia, NY 11716. Circle 345

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Statement of the Ownership, Management  
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September 29, 1983

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Publisher

## Monitoring tool for AOS/VS

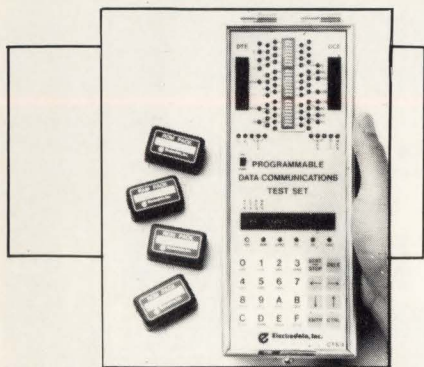
AOS/VS performance monitor software lets users analyze their 32-bit Eclipse® system environment. It provides information about the seven major operating system areas: memory management, demand paging, disk I/O, the scheduler, process management, CPU utilization, and character I/O. The monitor has 15 displays; two display the general operating system state, ten are for AOS/VS major areas, and three others are help oriented screens. The monitor is priced at \$6000. **Data General Corp, Information Systems Div**, 400 Computer Dr, Westboro, MA 01581. **Circle 346**

## More capability in test set

A modular addition to the 411A digital channel access test set adds TIC diagnostic and interface features to resident test functions. The 1411A MUX/deMUX/simulator allows T-carrier transmission and digital switching systems. It also allows monitoring or testing of any channel in TIC bit stream. This occurs without affecting traffic in other channels. It can also be used for in and out of service testing for MIC MUXes. Module can be ordered separately for field retrofit or premounted. **LSI Sierra, div of Lear Siegler, Inc**, 3885 Bohannon Dr, Menlo Park, CA 94025. **Circle 347**

## Programmable test set

CTS 3 is a handheld battery operated data communication test set. It will execute a user generated simulation program, and simultaneously monitor both transmit and receive data. In addition, it will perform bit and clock error rate tests, distortion tests, and pulse transition trapping. All menu selected operating parameters are retained when memory is off. It can be programmed to simulate full duplex, half duplex or multidrop sync, HDLC, or async network protocols. The test set costs \$2495. **Electrodata, Inc**, 23020 Miles Rd, Bedford Heights, OH 44128.



Circle 348

## Set tests digital transmission

S5104 digital transmission test set allows complete characterization of systems operating at the DS1, DS1C, and DS2 transmission rates. Framed and unframed pattern generation and error measurements are provided at all three rates. Using the jitter injection and measurement option, jitter can be injected into all transmitter modes using external frequency or internal oscillator. Either a pseudo-random sequence, all ones, or a programmable short pattern can be generated for error measurement. Price is \$6800. **Tau-tron Inc**, 27 Industrial Ave, Chelmsford, MA 01824. **Circle 349**

## Comm interface test set

Model 1500 Comit is designed for testing modems, MUXes, printers, and terminals. It uses a 28-key keyboard and an 80-char LCD with functions selected through a single-key stroke or menu options. Sync and async modes operate for all std bit rates through 19.2k bps, with sync rates extended to 72k bps. Async data stream format can be evaluated for bit rate, character size, parity, and number of stop bits. It provides a real-time monitor display of either DCE, DTE, receive, transmit, or both. Device is priced at \$2145. **Phoenix Microsystems, Inc**, PO Box 4206, Huntsville, AL 35802. **Circle 350**

## Vertical amp for scopes

The 7A42 logic triggered vertical amp incorporates basic logic trigger functions with wide bandwidth and high performance vertical amps. The 2-compartment amp for the 7000 series scopes provides analog representation of digital signals for analyzing ringing, overshoot, and undershoot. Device provides accuracies to better than 200 ps, offers digital triggering, and has four independent amp channels. Std features include a variable threshold setting and a trigger filter. The 7A42 is priced at approx \$6000. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077. **Circle 351**

## Emulator for NSC-800

EM-800 diagnostic emulator provides support for NSC-800 micros. Emulator replaces the micro in the user's system. The system then runs the same as with the original chip, but the user has control over, and visibility into, the system. It runs the system transparently in real time up to 4 MHz. Emulator includes up



to 64K bytes of RAM overlay, a 254-step by 32-bit trace memory, two hardware breakpoints, preprogrammed and user programmable tests, and upload or download in Intel format to any host computer with no special hardware or software. System base price is \$3750. **Applied Microsystems Corp**, 5020 148th Ave NE, PO Box C-1002, Redmond, WA 98052. **Circle 352**

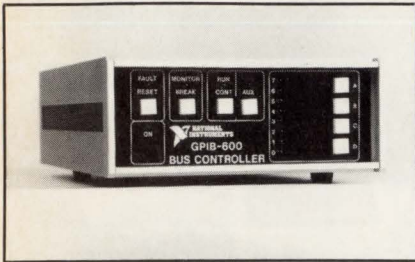
## Micro-controlled function generators

Two 12-MHz function generators, models 273 and 275, feature arbitrary sweep and arbitrary waveform capability, respectively. Model 273 allows a programmable frequency sweep vs time. Memory is 12 bits x 1000 points. Sweep memory, in two sections, can be user defined or preset with 2K bytes of memory. Model 275 features 12 bits of vertical resolution and 2K points of horizontal memory. Waveforms can be sent from 267 ns to 267 s/step. All models have a step by step calibration procedure that speeds up performance verification. The 273 is \$3095 and the 275 is \$3695. **Wavetek**, 9045 Balboa Ave, San Diego, CA 92123. **Circle 353**

## Compact disk certifier/processor

A high speed rigid disk magnetic memory test and verification instrument, PQ5801 can fully test a high density 5 1/4" disk in less than 60 s. Variable spindle speeds from 200 to 6000 rpm can be selected. Functions include complete analytical testing in a single pass in spiral mode or by using a step and repeat test. Both provide complete ANSI test capabilities. Operators can quickly test, analyze, and certify 8" or 5 1/4" disks of various densities. The device is priced from \$79,850 to \$105,000. **ProQuip, Inc**, 1725 De La Cruz Blvd, Santa Clara, CA 95050. **Circle 354**

## Standalone IEEE 488 controller



GPIB-600 is a general purpose IEEE 488 bus controller. The device can function as a standalone controller with complete listener, talker, and controller capabilities. It contains a Z80A, an IEEE 488 bus port, an RS-232-C serial port (full modem support), 16K-byte dynamic RAM, and 8K-byte EPROM. The EPROM contains a monitor program and an operating system with user callable routines for communication with the IEEE 488 bus and the RS-232-C port. Three 8K-byte EPROM sockets are provided for user application programs. Baseline GPIB-600 is priced at \$1800. **National Instruments**, 12109 Technology Blvd, Austin, TX 78759. Circle 355

## Cartridge tape drive coupler

PM-CTCV11A coupler board provides LSI-11 interface to any QIC-02 compatible 1/4" streaming tape drive. The coupler offers an auto boot function which enables read and execute commands to any given block of bootable tape. An off-line utility (cartridge image backup) allows compact backup of DEC's RL01/02, RK05, RK06/07, and RM02/03 disk drives. No special interfaces or commands are required to integrate different tape drives with the LSI-11-based system as the QIC-02 is compatible with the QIC-24 format. Price is \$1320. **Plessey, Peripheral Systems, Computer Products Div**, 1674 McGaw, Irvine, CA 92714. Circle 356

## Binary call board

Communication controller BCB-300 permits interfacing to four modems and four auto-dialers. The board is not limited to ASCII communications—it can handle any character length up to 1.5k bits. Each port provides both an RS-232 modem interface and an RS-366

auto-dialer interface. Two 8253 timers provide four independent receive clocks and two shared transmit clocks. The 8085-based board is Multibus compatible and has DMA via a 16K-byte window in 1M byte of address space. Prices range from \$800 to \$990, depending on quantity. **Micro Digital**, 12791 Western Ave, Unit C, Garden Grove, CA 92641. Circle 357

## Image sensor

RA256X256 area image sensor has a total of 65,536 photodiodes in a 2-dimensional 256 x 256 matrix. It features both single-frame or odd/even interlaced readout at a data rate up to 5 MHz. Partial frames can be scanned at a faster rate. Image acquisition can be started in the middle of a readout sequence through a frame reset feature (for high speed sync or stroboscopic applications). The sensor is capable of a full-silicon spectral response of 200 to 1100 nm. The 100-piece quantity price is \$2125. **EG&G Reticon**, 345 Potrero Ave, Sunnyvale, CA 94086. Circle 358

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### IBM PC combination board

PDI464-SP features expansion memory, two async serial channels, a realtime clock, a disk emulator, and parallel or serial print spoolers—all for the IBM PC. Memory is expandable to 256K bytes in 64K-byte increments and has onboard parity generation/checking. Disk emulator is configurable for single- or double-sided drive emulation and does not require patching of any system files. The spooler allows serial channel print pool while running other applications, is menu oriented, and has a selectable buffer size. Prices range from \$453.52 to \$682.18, depending on the amount of memory. **Pure Data Ltd**, 950 Denison St, Unit 17, Markham, Ontario, Canada L3R 3K5. Circle 359

### Multibus system controller

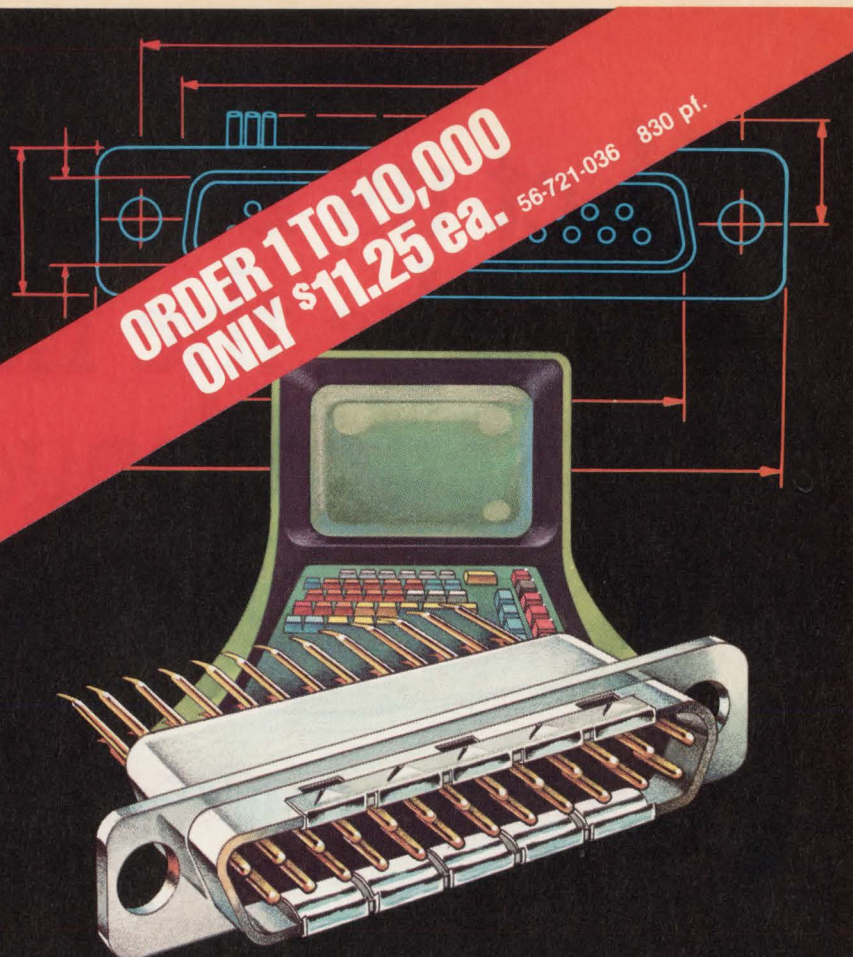
A multiline async controller, UB2012 is designed for use in any Multibus system. As a Multibus component board, it supports eight async terminals or lines. The controller includes a NS16008 micro, 64K-byte buffer, 16K-byte PROM, and eight full-duplex lines with programmable baud rates up to 38.4k bps. Interfacing is available for either RS-232-C or RS-422 connectors. The device controls all character by character processing usually done by the host and guarantees 16 interrupts/s max. Single-board price is \$1995. **Unidot, Inc**, 602 Park Point Dr, Golden, CO 80401. Circle 360

### Winchester disk controller

David is a Xebec 1410-compatible Winchester disk controller. Features include consecutive sector operations with one to one interleaving, onboard data buffers ranging from 1K to 8K bytes, and 256- and 512-byte block sizes. It supports two ST506 type Winchester disk drives. In addition, performance features are multi-sector operations on consecutive sectors without interleaving, high performance defective media relocation, and overlapping seek. The controller's host interface is the SASI bus std. **Adaptive Data & Energy Systems**, 2627 Pomona Blvd, Pomona, CA 91768. Circle 361

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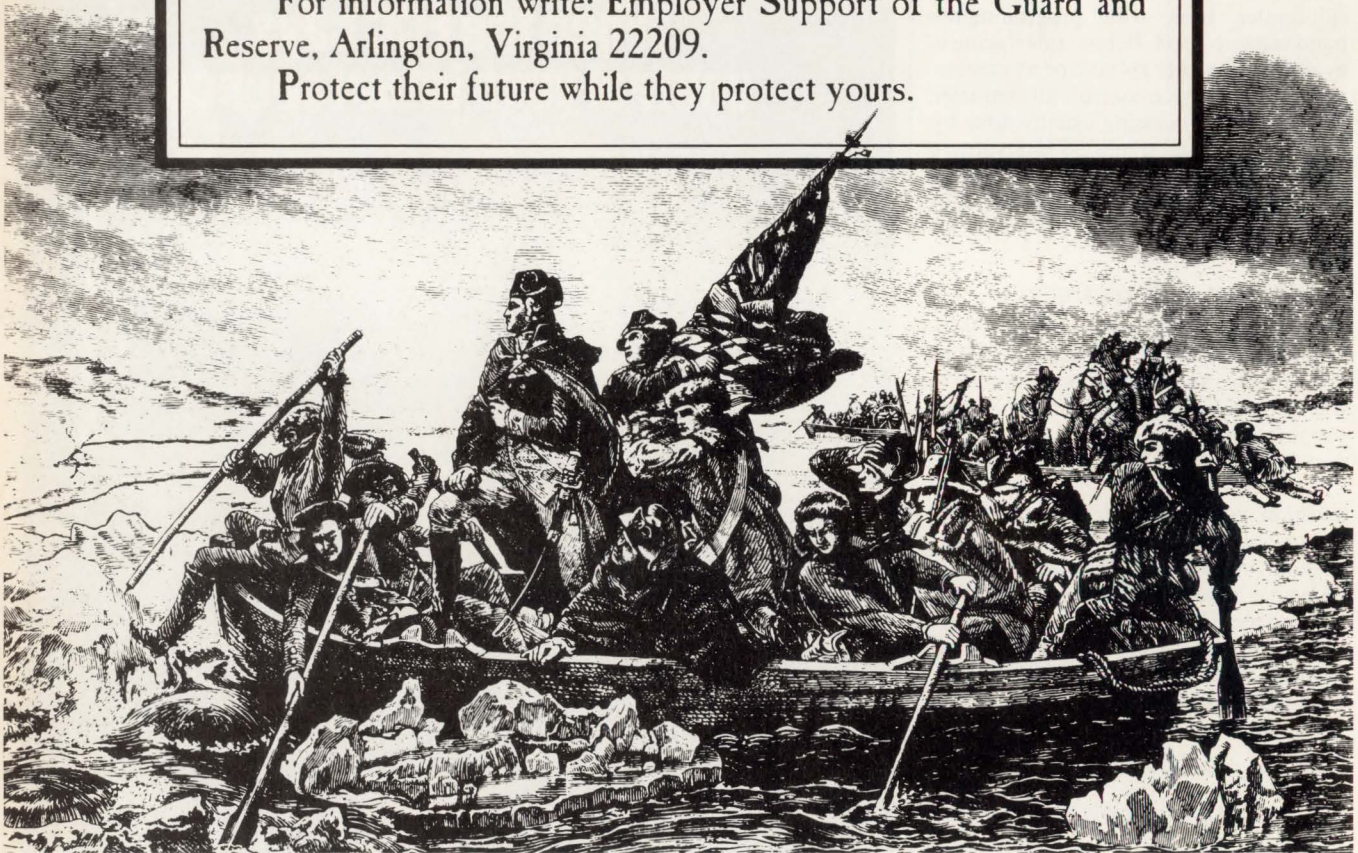
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## Microprocessor display drivers

The TSC7211AM and TSC7212AM are 4-digit bus-compatible display decoder and driver ICs. The CMOS TSC7212AM drives four 7-segment LEDs. The TSC7211AM drives four 7-segment LCDs and contains an onchip backplane oscillator. Devices can be slaved together to drive multidigit displays with a common backplane. Both devices accept BCD input data; a 4-bit input word is latched and decoded into the 7-segment code B output format. A 2-bit input code selects the digits. Operating supply is 4 to 6 V. Available in 40-pin plastic DIPs, the devices range in price from \$3.85 to \$4.85, all in 100-piece quantities. **Teledyne Semiconductor**, 1300 Terra Bella Ave, Mountain View, CA 94043.

Circle 362

## Single-supply quad op amps

MC34074 series op amps operate over a range of 3 to 44 V with a single supply, or from  $\pm 1.5$  to  $\pm 22$  V with dual supplies. With input pole-zero cancellation and Miller loop compensation at the all-npn output, the amps provide a 4.5-MHz gain bandwidth and a 13-V/ $\mu$ s slew rate without p-channel JFET technology. Max input offset voltage is 2 mV for the prime and 4.5 mV for std devices. Typ input bias current is 100 nA. All-npn output stage minimizes total harmonic distortion to 0.02%. Devices are packaged in 14-pin plastic or ceramic DIPs and range in price from \$1.95 to \$9.75 (in quantities of 100 and up). **Motorola Semiconductor Products Inc**, PO Box 20912, Phoenix, AZ 85036.

Circle 363

## Power efficient uVEPROM

R87C32, organized as 4K x 8 is a 32K CMOS uVEPROM supporting 8- and 16-bit bus structures. Max dissipation is 132 mW in the active mode and 0.525 mW in standby. It is pin compatible with its NMOS equivalent and uses the std programming voltages. The EPROM features a 24-pin DIP, a single 5-V supply, completely static operation, TTL-compatible inputs, and three state outputs. Two speeds are available: a 350-ns version and a 450-ns version. Five operating modes are available: read, standby, program, program verify, and program inhibit. Prices are from \$8 to \$11.25 each. **Rockwell International Corp, Semiconductor Products Div**, 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.

Circle 364

## Video DAC

Three VDAC-444TDS are 4-bit video DACs that operate with conversion rates to 40 MHz and 10-ns settling times. They provide a palette of 4096 colors and interface between the computers and CRT in a high resolution color graphics terminal. A full output is developed across a 75- $\Omega$  load

and the output is virtually glitch free. All three outputs have composite blanking to inhibit any display screen illumination during beam retrace periods. The 100-piece cost for the device is \$75. **Intech Inc, Microcircuits Div**, 2270 Martin Ave, Santa Clara, CA 95050.

Circle 365



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## High performance ROM

Am92256 256K-bit ROM features automatic power down, controlled by a separate chip enable pin. A separate output enable pin controls outputs providing system flexibility and eliminating bus contention. Access time is 300 ns. The device uses late-mask programming techniques for guaranteed lead times of six to eight weeks. In addition, it operates from a single 5-V power supply and is pin compatible with Am27256 256K-bit EPROM. The ROM is available in 28-pin plastic packages and is priced at \$11 each in 1000s plus a \$2000 mask charge. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086. Circle 366

## Direct memory access interface

SCB68430 DMAI is a single-channel controller on a chip that transfers data between memory and peripherals in systems designed around the 68000. Designed for I/O intensive applications, the device transfers data at the rate of 5M bytes/s. The DMAI transfers operands in byte, word, and long-word formats. It is readily programmable for operation in single-cycle or burst mode; burst mode handles block sizes up to 64k operands. In addition, the chip provides bus arbitration, logic support for vectored interrupts, and auto rerun on bus error. **Philips, Electronic Components and Materials Div**, PO Box 523, 5600 AM Eindhoven, The Netherlands. Circle 367

CMOS level voltage inputs. Two chip-enable inputs gate the address and output buffers and power the chip down into the standby mode. Output enable terminal controls the output buffers to eliminate bus contention. The ROMs come in either a 28-pin cerDIP or plastic DIP and cost \$8 in 10k-piece quantities. **RCA, Solid State Div**, Box 3200, Somerville, NJ 08876. Circle 368

## Wide range of RAM access times

EDH82H16 static RAM offers 22-pins and a 16,384- x 2-bit organization. Unit is available in address access times of 45, 55, 70, and 100 ns and in NMOS, low power CMOS, or MIL-STD-883B versions. The chip is pin-compatible with industry std 16K x 1 parts and provides  $\overline{CE}$  power down and separate data-in/data-out. Max active power dissipation is 1200 mW (500 mW CMOS), 80 mW standby (500  $\mu$ W CMOS). In 100-piece lots, prices range from \$31.95 to \$59.95, depending on version. **Electronic Designs Inc**, 35 South St, Hopkinton, MA 01748. Circle 369

## Low power/large storage ROM

CDM53128 is a static ROM organized as 16K x 8. The 128K-bit CMOS mask programmable device features a 250-ns max access time from address. At a 250-ns cycle time, the max operating current is 30 mA. In the standby mode the chip draws 2  $\mu$ A (typ) and a 50  $\mu$ A max with

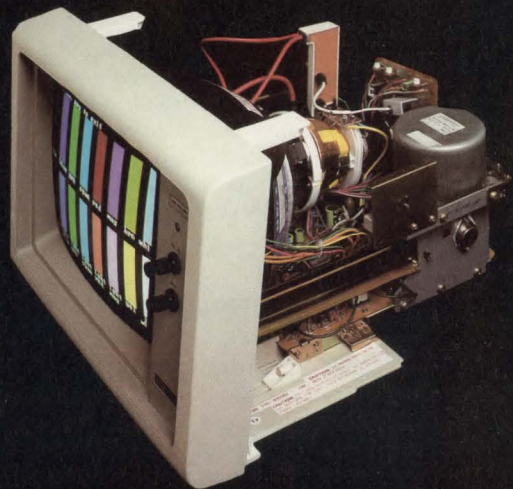
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# High Resolution RGB Color Monitor

<b>CRT</b>	12" Diagonal, 76 Degree, in-Line Gun, .31 mm dot pitch black matrix, non-glare surface (NEC 320CGB22)
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<b>Video Bandwidth</b>	15 MHz
<b>Scan Frequencies</b>	Horizontal — 15.75 KHz Vertical — 60 Hz
<b>Misconvergence</b>	Center: 6 mm max, Corner: 1.1 mm max
<b>Display Size</b>	215 mm X 160 mm
<b>Resolution</b>	Horizontal — 690 dots Vertical — 240 lines (not interlaced) 480 lines (interlaced)

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### User friendly EEPROM

ER5901 is a word-alterable EEPROM. The 1K-byte wide, 5-V only device can store data even with the power off. This ensures data integrity, enhanced security, and operational efficiency. The chip offers in-circuit erasability with auto-erase/write cycle and  $10^4$  erase/write cycles per word. Onchip data and address latches free the processor for other tasks. Access times are less than 300 ns and data retention span is 10 years or more. The device is organized as 128 x 8. **General Instrument Corp, Microelectronics Div, 600 W John St, Hicksville, NY 11802.**  
Circle 370

### High density EPROM and DRAM

Approved as Class B military components (MIL-STD-883B), the M27128 EPROM and M2164A DRAM offer high densities. The EPROM provides 128K bits of non-volatile memory. Organized as 16K- x 8, it has a 250-ns max access time. Active current is 150 mA and standby is 50 mA. Device is programmed using the company's intelligent programming algorithm. The DRAM features a 64K- x 1-bit organization, and has a 150-ns max access time with a 260-ns cycle and 128 refresh cycles every 2 ms. In quantities of 100, the 28-pin DIP EPROM sells for \$412; the 16-pin DIP DRAM sells for \$32. **Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051.**  
Circle 371

### Single-chip controller

The 7250 CRT display controller can be masked programmed and is designed to provide an interface block between std micros and any CRT. Mixed characters and graphics modes, including mosaic and line graphics, are std. Nine internal registers are externally addressed to control all display features like page scrolling, and cursor position control. Screen attributes include blank screen, reverse video, underline, and highlight. An input clock signal and a single RAM are the only requirements for video display output. The 100-quantity price is \$18.80. **NCR Corp, Microelectronics Div, 1635 Aeroplaza Dr, Colorado Springs, CO 80916.**  
Circle 372

### Serial I/O controller

MK68564 interfaces a 68000-based micro to serial communication channels using async, bisync, or SDLC protocols. The dual-channel serial chip features two independent, full-duplex channels in a single 48-pin package. Onboard are two inde-

pendent baud rate generators with an internal crystal oscillator input. The 1M-bit sync data rate allows the controller to be used in LANS. The peripheral chip provides quadruple-buffered receive data registers and double-buffered transmit

registers. In plastic packages of 1000-piece quantities, the chip costs \$34 each. **Mostek Corp, a sub of United Technologies Corp, 1215 W Crosby Rd, Carrollton, TX 75006.**  
Circle 373

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**8086 CPU Set:** 8 MHz 8086 CPU • CPU Support board includes a console serial port, a second serial port, Centronics parallel port, vectored interrupt controller, four 16-bit timers and EPROM monitor for 8086 • MS-DOS 2.0 plus development utilities • 8087 numeric coprocessor is optional  
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**64k Static RAM** Fully static design makes interfacing easy • Compatible with a variety of CPU and DMA devices • High-speed (85 ns) RAMs operate to 10 MHz with no wait states • 16k, 32k, and 48k OEM versions are available  
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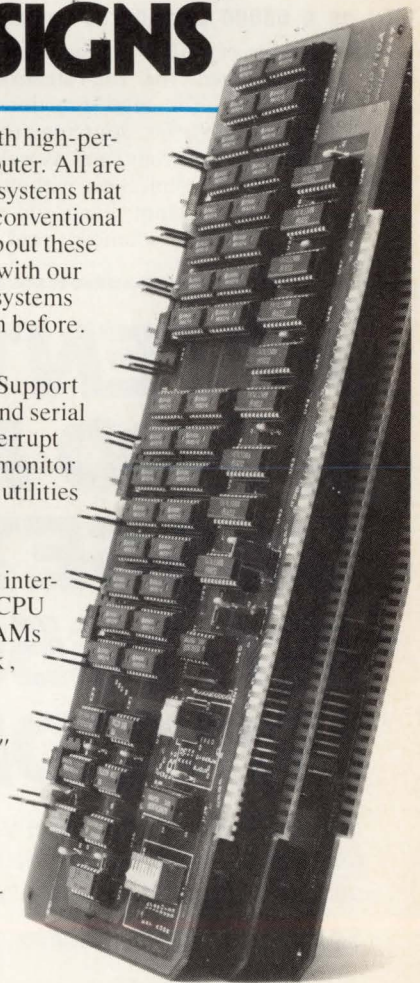
**Disk Master™** Controls as many as four 8" and four 5.25" floppy disk drives simultaneously, in any combination • Uses 1793 disk controller chip • Can be used with 10 MHz CPUs • **Single Qty: \$325.00**

**Multi-Port Serial Card** 2- and 4-port versions are available • These RS-232 ports operate as either "data sets" or "data terminals" • 36" cables included  
• **Single Qty: \$280.00 (4-port)**  
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Dealer and OEM inquires are invited.



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**Quad comparator**

The LP339 chip has four independent voltage comparators designed to draw 60  $\mu$ A of total current. A low power drain allows the chip to be used in battery-driven or voltage-independent applications. Device was specifically designed to interface with the CMOS logic family. Features include sensing at ground potential, a pinout identical to the LM339, and a high output sink current capability (30 mA at  $V_O = 2$  Vdc). Biasing current is 3 nA, input offset current is 0.5 nA, and input offset voltage is 2 mV. Parts are priced at \$0.72 in quantities of 100 or more. **National Semiconductor Corp.**, 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 374**

**FIFO as a 68000 peripheral device**

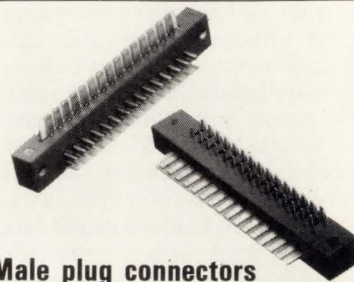
MK68345 high-density 512 x 9-bit dual-port FIFO was designed for the MK68000 16/32-bit micros. The FIFO functions primarily as a rate buffer, sourcing and absorbing data at different rates as well as providing async connection without arbitration. Full and empty flags and a two-port cell permits simultaneous read/

write cycles. The use of flags prevents data underflow and overflow. The peripheral is currently available with access speeds of 120, 150, and 200 ns. Prices range from \$28.50 to \$31.50, depending on access times. **Mostek Corp.**, a sub of **United Technologies Corp.**, 1215 W Crosby Rd, Carrollton, TX 75006. **Circle 375**

**Microprocessor iRAM**

The 2187A 64k-bit iRAM is organized as 8192 x 8. The chip features a refresh row address counter and MUX onchip, power-down, auto refresh mode, and extended cycle operation. The RAM is designed for sync applications where arbitrary wait states or system delays are not allowed. All normal dynamic memory refresh functions are performed internally. It is manufactured using HMOS D III double-poly process. Tech specs include access times of 250, 300, and 350 ns with a power dissipation of 385 mW. In 1000-piece quantities, the chip is priced at \$19.95. **Intel Corp.**, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123. **Circle 376**

**INTERCONNECTION & PACKAGING**



**Male plug connectors**

Series 63 male plug connectors can replace gold-plated edge fingers on PC boards. Benefits include reduced insertion values and higher durability than with PC board fingers. The connectors have copper-alloy contacts on 0.156" (3.962-mm) centers and from 6 to 24 contact positions with both single- and dual-readout. Current rating is 5 A continuous. Insulator housing is diallyl phthalate and mounting holes secure the connector to the PC board. Pricing is \$0.02 to \$0.04 per tab. **Methode Electronics, Inc., Connector Div.**, 7447 W Wilson Ave, Chicago, IL 60656. **Circle 377**

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*Pericom Corporation, 14 Huron Drive, Natick, Massachusetts 01760 USA Tel. (617) 655-7660.*

**Plug-in heat sinks**

A series of heat sinks plugs into TO-220 semiconductor devices and eliminates time-consuming fastening. The plug-in design features spring action clips that eliminate air gaps and ensure a tight fit between semiconductor and heat sink. Vertical and horizontal mountings are accommodated. There is a choice of three heights and the sinks can be furnished with or without tinned tabs for soldering. With fins on both sides, the devices provide air circulation for heat removal. **Aavid Engineering Inc.**, 30 Cook Ct, Laconia, NH 03247. **Circle 378**

**Expandable VERSAbus system**

VERSAbus-compatible interconnect system includes a card file, logic panel (daughterboard), and backplane (motherboard). Four-slot backplane is expandable to 12 slots and has signal traces on the outer layer, which comes with all std connections, resistors, and contacts for grounding. Edgecard connectors consist of pressfit gold-plated contacts with wirewrap tails installed in the plated

through holes. The backplane is configured with 100 I/O signal pins to provide alternating ground/signal pairs that minimize crosstalk. **Stanford Applied Engineering, Inc.**, 340 Martin Ave, Santa Clara, CA 95050. **Circle 379**

**SOFTWARE**

**Software for protocol analyzer**

An applications software package extends the capabilities of the HP 4955A protocol analyzer. It adds specialized protocol decode and display software. Using this software, the analyzer will decode at speed SNA, DDCMP, and HPDLC protocols. The analyzer will also be able to decode BSC-framed X.25 protocol. In addition, the software provides a simultaneous frame and packet display so the user can have level 2 and level 3 information. The protocol analyzer with decode tape is priced at \$18,680. **Hewlett-Packard Co.**, 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 380**

**Emulation of 3270 for micros**

Micro/Remote 3270 software allows any micro to emulate an IBM 3270 mainframe computer terminal. The software lets the user access the mainframe's data bases through virtual screen capabilities. The virtual screen is a buffer containing data translated into ASCII. The attribute characters remain in EDCDIC form. Written in C for portability, it is, in source form, easily integrated into ROM-based products with min memory requirements of 15K bytes of ROM and 6K bytes of RAM. **ATON International, Inc.**, 1765 Scott Blvd, Santa Clara, CA 95050. **Circle 381**

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## C compiler for 8086/8088

Designed for the iAPX 86 and 88 micro family, the C-86 is a C language compiler. C-86 runs under the universal development interface on the Isis-II, INDX, and IRMX-86 operating systems. The compiler supports the object module format allowing C-86 object code to be linked with object code from other Intel compilers. It features a full std I/O library, including functions for file I/O, printing, and reading from a terminal. Also included are 32-bit and emulated floating point routines, conversion and string manipulation routines, as well as special case operating system interface routines. The compiler sells for \$3500. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051. Circle 382

## Processor software for 4300

Modular applications system software is now compatible with the IBM 4361 model groups 4 and 5. The software includes MAS-manufacturing, MAS-payroll, MAS-personnel, MAS-decision support, and MAS-project management. MAS software is available for all IBM 4300 and 30XX processors under SSX, DOS/VSE, VS/1, and MVS operating environments. Pricing of the software depends on the number of modules purchased. The MAS-manufacturing ranges from \$25,000 to \$179,000. Other modules are priced from \$19,000 to \$73,000. **Martin Marietta Data Systems**, 6303 Ivy Ln, Greenbelt, MD 20770. Circle 383

## Cache board spooling software

OR-88CPS is a software package that adds print spooling to the MDS series II, III, and 800 development computers. Together with the OR-88C disk cache board, the software requires no external hardware. Installation consists of defining a macro file that selects either a parallel port or a serial port at any baud rate (up to 9.6k baud). The x-on/x-off protocol is supported. Spool command format and installation macro are in a help file. Up to 196K bytes can be spooled at a time. The price of the board remains at \$2850. **Origin, Inc**, 9136 Gibson St, Los Angeles, CA 90034. Circle 384

## Second generation tester software

Release 2 software package expands the capabilities of 810 and 900 series of in-circuit testers. Running under Unix, it features a signature verifier routine, mixed mode, netcomm, install, bus fault isolater programs, and Unix utilities. Signature verifier calculates digital signatures

of ICS from expected data streams. Mixed mode enables simultaneous analog and digital stimulus and measurement. The bus fault isolater program increases board diagnostic capabilities. Release 2 is provided free of charge to 810 and 900 customers. **Zehntel, Inc**, 2625 Shadelands Dr, Walnut Creek, CA 94598. Circle 385

## COMPUTERS

### PC with built-in LAN

PCTerminal functions as an intelligent terminal in an IBM PC network. It has a monitor, keyboard, 8088 micro, both serial and parallel interfaces, 256K bytes of memory, and built-in network capabilities. A proprietary network protocol allows the unit to initialize its operating system from remote floppy or hard disk. In addition, communications can occur with the PCTerminal without its own floppy drive. Up to 16 terminals can be connected to one IBM PC or XT. Price for the device is \$1295. **Santa Clara Systems**, 1860 Hartog Dr, San Jose, CA 95131. Circle 386

### STD bus package with 8" floppy disk choice

The driveless version of model 702 STD disk package is a user configurable micro-controller system. The front panel is cut for easy installation of one or two std 8" floppy drives. It is designed to serve as a package for STD bus applications requiring mass storage such as data collection, process control, and automated test equipment. The all-metal package contains a 13-slot STD bus card rack, a four voltage switching power supply, and a forced air cooling system. **Pro-Log Corp**, 2411 Garden Rd, Monterey, CA 93940. Circle 387

### Micro with Unix System v

Unistar 300 68010-based micro system features 32-bit architecture that supports virtual memory and the Unix System v operating system. System v benefits include faster C compiler execution and inter-task communications. The system offers 2M bytes of memory with parity checking and no wait states. The 5 1/4" Winchester provide up to 160M bytes of storage. High speed sync I/O bus handles transfer rates to and from memory at 4M to 5M bps. Prices start at \$20,000. **Callan Data Systems**, 2645 Townsgate Rd, Westlake Village, CA 91361. Circle 388

## MICROPROCESSORS/MICROCOMPUTERS

### Processor board with 32-bit system

A 68000-based UniVax processor board for the PDP-11 offers increased speed, Unix power, and continued use of existing peripherals. The combination of processor, operating system, and memory is available at the board level or as part of a fully integrated system. The single quad board provides memory management, 16M bytes of logical address space within the 4M-byte physical address space of the Q-bus, and dual-bus architecture. Throughput approaches 1M bps. Single-quantity list price is under \$8000. **Cambridge Digital Systems, div of Compumart**, PO Box 568, 65 Bent St, Cambridge, MA 02139. Circle 389

### VMEbus interface on 68000 board

Single-board CPU 01 is VMEbus compatible using the 68000. It offers 256K bytes of RAM and 64K bytes of ROM/EPROM. Serial interface includes three RS-232-C ports and a parallel port. There are four timers: one 8-bit timer, two universal 8-bit timer/counters, and one 24-bit timer counter. Other features are sixteen 32-bit data, address, and stack registers, 14 address modes, 16M-byte address range, an 8- to 16-MHz CPU clock, plus a real-time clock with battery backup. It accepts 56 types of command and five data types: bit, byte, word, longword, and BCD. Prices range from \$1250 to \$1950 depending on configuration. **Dec-Tec, Ltd**, 2221 Jackson Cir, Carrollton, TX 75006. Circle 390

### Slave processing micro

Spu-Z combines a Z80-B, 192K bytes of memory, and two full RS-232-C serial I/O ports on a single board. Flexible bank switching allows a 4K, 8K, or 16K global area that can be in low or high memory to accommodate CP/M-Plus or Oasis. Serial port parameters are software selectable. The board can be used as an 8-bit node in a multi-user, multiprocessing environment with up to 16 boards in the same mainframe. It meets all IEEE-696/S-100 specs. **CompuPro, a Godbout Co**, Oakland Airport, CA 94614. Circle 391

**December Preview—  
1983 system components  
roundup.**



Ad  
Council

Photo: Peter B. Kaplan

## If you still believe in me, save me.

For nearly a hundred years, the Statue of Liberty has been America's most powerful symbol of freedom and hope. Today the corrosive action of almost a century of weather and salt air has eaten away at the iron framework; etched holes in the copper exterior.

On Ellis Island, where the ancestors of nearly half of all Americans first stepped onto American soil, the Immigration Center is now a hollow ruin.

Inspiring plans have been developed to restore the Statue and to create on Ellis Island a permanent museum celebrating the ethnic diversity of this country of immigrants. But unless restoration is begun now, these two landmarks in our nation's heritage could be closed at the very time America is celebrating their hundredth anniversaries. The 230 million dollars needed to carry out the work is needed now.

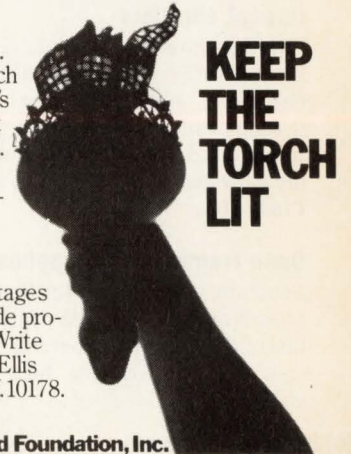
All of the money must come from private donations; the federal government is not raising the funds. This is consistent with the Statue's origins. The French people paid for its creation themselves. And America's businesses spearheaded the public contributions that were needed for its construction and for the pedestal.

The torch of liberty is everyone's to cherish. Could we hold up our heads as Americans if we allowed the time to come when she can no longer hold up hers?

### Opportunities for Your Company.



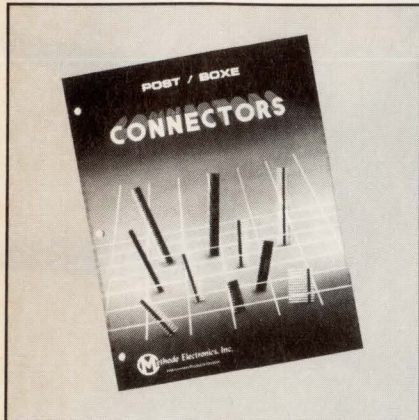
You are invited to learn more about the advantages of corporate sponsorship during the nationwide promotions surrounding the restoration project. Write on your letterhead to: The Statue of Liberty-Ellis Island Foundation, Inc., 101 Park Ave, N.Y., N.Y. 10178.



KEEP  
THE  
TORCH  
LIT

Save these monuments. Send your personal tax deductible donation to: P.O. Box 1986, New York, N.Y. 10018. **The Statue of Liberty-Ellis Island Foundation, Inc.**

## Board to board interconnects



Illustrations and photographs describe Post/Boxe high density connectors and headers; 0.100" grid system consists of 3-A single and dual, straight and right-angle models. **Methode Electronics, Inc.**, Rolling Meadows, Ill.  
**Circle 410**

## Data bus products

Catalog features MIL-STD-1553 line, giving specs and delivery information for each product, and functional block diagrams for bus control units. **SCI Systems, Inc.**, Huntsville, Ala.  
**Circle 411**

## Resistor/capacitor guides

Guides list standard mil-spec approvals for fixed film resistors, networks, and trimmers, and for aluminum electrolytic and tantalum capacitors. **Mepco/Electra, Inc.**, Morristown, NJ.  
**Circle 412**

## Switching regulators

Folder gives characteristics, features, and max ratings on LAS6300 series 3- and 5-A regulators, with diagrams of technical applications. **Lambda Semiconductors, div of Veeco Instruments, Inc.**, Corpus Christi, Tex.  
**Circle 413**

## Optical encoders

Foldout shows RA absolute and RI incremental series rotary optical shaft angle encoders, and lists solid shaft and through-hole configurations with resolutions to 0.31 arc-seconds. **Itek Measurement Systems Div.**, Newton, Mass.  
**Circle 414**

## Open frame power supplies

Brochure covers specs for line of dc supplies from 40 to 250 W, including outlines and mounting diagrams for various case sizes. **Power-One Inc.**, Camarillo, Calif.  
**Circle 415**

## Direct current motors

Folder outlines dimensional data and electrical, mechanical, and performance specs of 2300 series, 0.250" to 0.500" diameter dc motors. **Harowe Servo Controls Inc.**, sub of **Bowmar Instrument Corp.**, West Chester, Pa.  
**Circle 416**

## Power converters

Photos and dimensional drawings complement product descriptions and application information on H-series 1.5-W dc-dc converters. **Stevens-Arnold Inc.**, South Boston, Mass.  
**Circle 417**

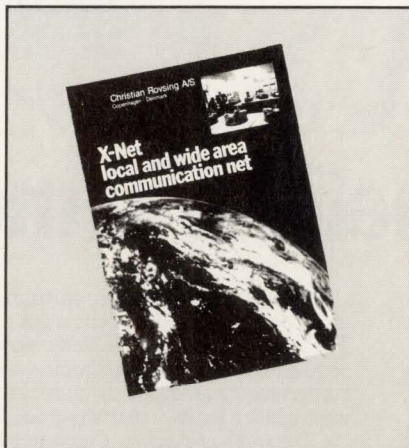
## Industrial computer

Folder outlines capabilities, specs, and features of the IMC-4000 microcomputer, which is designed for localized plant monitoring as well as data collection in large factory integration systems. **Gould Inc.**, Nashua, NH.  
**Circle 418**

## High-resolution DACs

Bulletin for users of CMOS data converters above 12 bits discusses DAC design and trade-offs using R-2R, segmentation, and binary weighting; application problems of temperature stability, output capacitance, settling time, digital feedthrough, grounding, output offset, reference levels, and output amplifier effects are detailed. **Hybrid Systems Corp.**, Billerica, Mass.  
**Circle 419**

## Data communication network



Pamphlet gives full range of applications, functions, and components of the X-net local and wide area network, which links 50 to 50,000 noncompatible mainframes, minicomputers, terminals, and peripherals into a single shared system. **CR Computer Systems, Inc.**, Orange, Calif.  
**Circle 420**

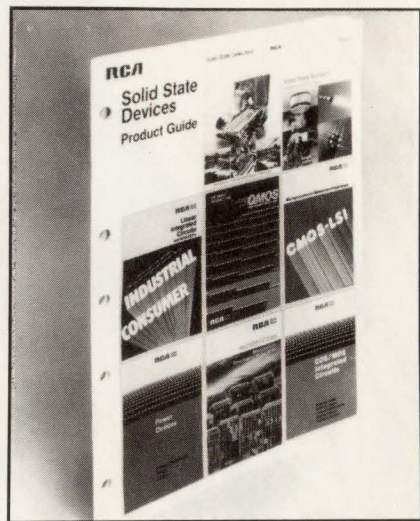
## Rotary switch

Dimensional diagrams of low-profile PC mount model 3.13007 highlight features and technical data. **Ledex Inc.**, Vandalia, Ohio.  
**Circle 421**

## Analog products

Key advantages and applications of op amps, buffers, monolithic dual transistors, and voltage references are accompanied by schematic diagrams and graphs. **Precision Monolithics Inc.**, Santa Clara, Calif.  
**Circle 439**

## Solid-state devices



Product guide summarizes significant features and applications of a broad device range; each section references specific company catalogs that contain more detailed information, as well as data books that provide complete technical specs. **RCA/Solid State Div.**, Somerville, NJ.  
**Circle 422**

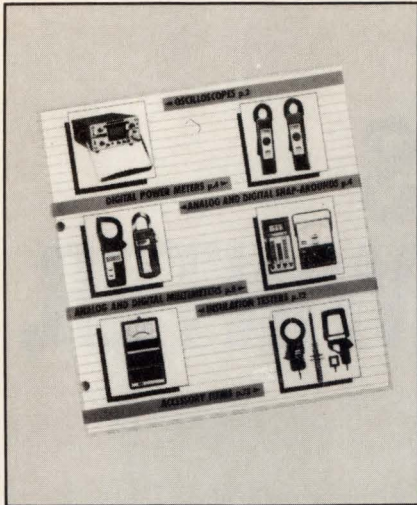
## Programs for PDP-11

Source book covers 33 application and system software categories; each program entry lists operating systems it runs under, support levels, and compatibility with VAX minicomputers. Key words and directory to company sources are also supplied. Request on company letterhead from **Digital Equipment Corp.**, Printing and Circulation Services, 444 Whitney St., Northboro, MA 01532.

## Digital signal processors

Brochure describes components, including multipliers, multiplier-accumulators, A-D and D-A converters, special functions, and storage products. **TRW LSI Products**, La Jolla, Calif.  
**Circle 423**

## Portable test equipment



Electrical equipment catalog covers oscilloscopes, analog/digital snap-arounds and multimeters, insulation testers, indicating devices, and accessories; photos, specs, and packaging information are included. **A.W. Sperry Instruments Inc**, Hauppauge, NY.

Circle 424

## Transient waveform recorders

Brochure describes and specifies SE2550 series multiprocessor controlled recorders, examining various menu pages and simultaneous 4-trace display. **Thorn EMI Technology Inc**, Atlanta, Ga.

Circle 425

## Polycarbonate sheet

Brochure describes properties of Lexan<sup>®</sup> sheet material, highlighting attributes like high impact resistance, ability to withstand temperature extremes, and long-term endurance. **General Electric Co, Plastics Operations**, Pittsfield, Mass.

Circle 426

## Connectors shielding emi/rfi

Catalog geared to help designers meet FCC Docket 20780 requirements provides product descriptions, performance characteristics, electrical data, contact arrangements, mounting/termination and assembly data, and tips on selecting the proper connector. **ITT Cannon Electric Div**, Fountain Valley, Calif.

Circle 427

## Graphics systems

Foldout discusses series 100 system hardware, graphics software, distributed communications, pattern generation, user support, design aids, and system productivity. **VIA Systems, Inc**, North Billerica, Mass.

Circle 428

## Electronic packaging

Indexed catalog describes breadboarding, prototyping, and packaging items, with special sections devoted to circuit boards, racks and cages, connectors, terminals, accessories, and tools. **Vector Electronic Co, Inc**, Sylmar, Calif.

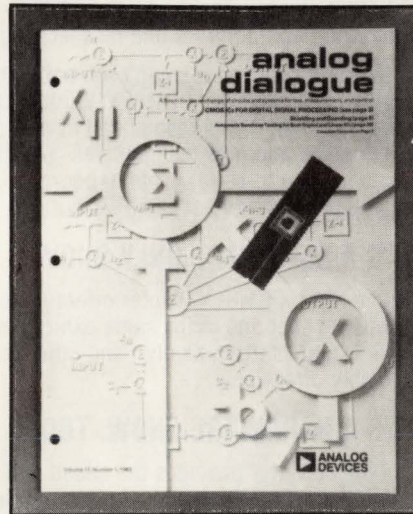
Circle 429

## Environmental simulation

Booklet describes temperature/humidity chambers, dynamic burn-in systems, altitude chambers, electrodynamic vibration equipment, walk-in rooms, thermal shock chambers, and a full range of instruments designed for environmental simulation equipment and systems. **Thermotron Industries, Inc**, Holland, Mich.

Circle 430

## Signal processing applications



Issue of *Analog Dialogue* technical journal (vol 17, no 1) discusses CMOS ICs for digital signal processing; in addition, it features application notes on shielding and guarding analog circuits to reduce interference-type noise and essential components in logarithmic D-A converters used for automatic gain control. **Analog Devices**, Norwood, Mass.

Circle 431

## Power supplies

A pictorial index with functional diagrams comes in this bulletin of 1.5- to 60-V, 60-A rackmount models, redundant output systems, and custom-made units. **Acopian Corp**, Easton, Pa.

Circle 432

## Data service unit

Data sheet describes Bell-compatible TP-500, a direct replacement for DSU-500, covering front panel controls and indicators. **TeleProcessing Products, Inc**, Simi Valley, Calif.

Circle 433

## Port selection switches

Application notes illustrate use of automatic switching and automatic scanning units with desktop microcomputers, giving connection requirements and sample Basic programs. **Giltronix**, Palo Alto, Calif.

Circle 434

## Intelligent displays

Guide outlines basic operation, package dimensions, features, applications, and technical specs of Litronix alphanumeric line display; dimensional drawings are included. **Litronix Div, Siemens Components Inc**, Cupertino, Calif.

Circle 435

## Intelligent data switches

Brochure describes the Develnet modular local data nodes, and outlines technical data; each node supports 248 data lines with 3M-char/s throughput. **Develcon Electronics Inc**, Doylestown, Pa.

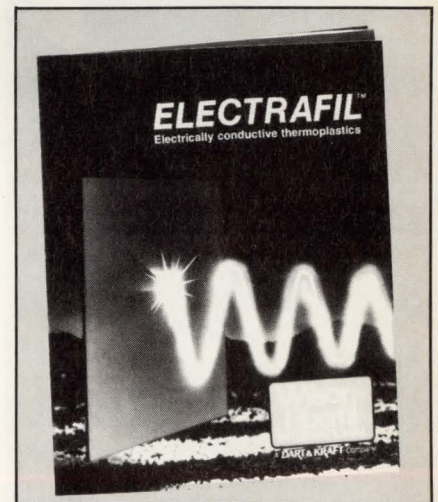
Circle 436

## Documenting VLSI

Programming manual for the J941 VLSI test system demonstrates the relationship of programming syntax to system architecture; a step-by-step explanation of a complete sample test program and separately bound, detachable appendix are included. **Teradyne, Inc**, Woodland Hills, Calif.

Circle 437

## Conductive thermoplastics



Booklet introduces Electrafil line of electrically conductive materials, describing properties of various thermoplastic composites; charts highlight surface resistivity vs shielding effectiveness, and tabulate mechanical, physical, thermal, and electrical characteristics of the various materials. **Wilson-Fiberfil International, a Dart & Kraft Co**, Evansville, Ind.

Circle 438

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## CONFERENCES

**NOV 28-DEC 2—Comdex/Fall**, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600

**DEC 5-7—Future of Optical Storage, Video Disks, and Computers to the Year 2000**, Hotel Inter-Continental Maui, Kihei, Hawaii. INFORMATION: Joanna Spilman, Technology Opportunity Conf, PO Box 14817, San Francisco, CA 94114. Tel: 415/626-1133

**DEC 5-6—Internat'l Electron Devices Meeting**, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Assocs, 1629 K St NW, Washington, DC 20006. Tel: 202/296-8100

**DEC 7-9—Realtime Systems Symposium**, Crystal City Marriott, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**DEC 12-14—Computer Networking Symposium**, Sheraton Hotel, Silver Spring, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**DEC 13-15—Automatic Testing and Test Instrumentation Conf and Exhibition**, Metropole Convention Ctr, Brighton, England. INFORMATION: Network Exhibitions Ltd, Printers Mews, Market Hill, Buckingham, MK18 1JX England. Tel: 028-02/5226-5227

**DEC 15-17—Internat'l Conf on Information Systems**, Houstonian Hotel & Club, Houston, Tex. INFORMATION: Maryam Alavi, Dept of Systems and Strategy, College of Business Administration, Univ of Houston, Houston, TX 77004. Tel: 713/749-3727

**JAN 17-19—Mini/Micro-Southeast**, Orange County Convention and Civic Ctr, Orlando, Fla. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

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**JAN 17-19—Southcon**, Orange County Convention and Civic Ctr, Orlando, Fla. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**JAN 31-FEB 2—Communication Networks Conf & Exposition**, Washington Convention Ctr, Washington, DC. INFORMATION: Judie McDaid, Hajar Assocs, 280 Hillside Ave, Needham Heights, MA 02194. Tel: 617/444-3946

**FEB-MAR—Invitational Computer Confs (European Series)**, Stockholm, Sweden; Paris, France; Munich, West Germany; Frankfurt, West Germany; and London, England; various dates. INFORMATION: Susan Fitzgerald, B. J. Johnson & Assocs, Inc, 3151 Airway Ave, Suite C-2, Costa Mesa, CA 92626. Tel: 714/957-0171

**FEB 20-22—Office Automation Conf**, Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**FEB 21-23—Softcon**, Superdome, New Orleans, La. INFORMATION: Peggy Kilburn, Northeast Expositions, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/343-2222 (outside Mass)

**FEB 22-24—ISSCC (IEEE Internat'l Solid-State Circuits Conf)**, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria, Coral Gables, FL 33134. Tel: 305/446-8193

**FEB 22-28—Imprinta (Internat'l Congress and Exhibition for Communications Techniques)**, Dusseldorf, West Germany. INFORMATION: Borman/Williams Inc, 222 Park Ave S, New York, NY 10003. Tel: 212/254-5400

**FEB 28-MAR 1—Compcon/Spring**, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**MAR 12-15—Interface**, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: Richard Katzeff, The Interface Group, Inc, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

**MAR 12-16—Internat'l Conf on Robotics**, Atlanta Hilton, Atlanta, Ga. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**MAR 19-21—Phoenix Conf on Computers and Communications**, Phoenix Hilton, Phoenix, Ariz. INFORMATION: David Gretton, Digital Equipment Corp, 2500 W Union Hills Dr, Phoenix, AZ 85027. Tel: 602/869-5273

**MAR 26-30—Internat'l Conf on Software Engineering**, Orlando, Fla. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

## WORKSHOPS

**DEC-MAR—Technical courses in Digital Processing, Man/Machine Systems, Micros and Minis, Networks and Systems, and Software**, various dates and cities. INFORMATION: Michael Sanson, Integrated Computer Systems, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: 213/450-2060; 800/421-8166 (outside Calif)

**DEC 6-8—Software Maintenance Workshop**, Naval Postgraduate School, Monterey, Calif. INFORMATION: Janice Thill, Code 54Ss Naval Postgraduate School, Monterey, CA 93940. Tel: 408/646-3212

**DEC 11-13—Computer Aided Graphic Arts and Visual Communications**, Essex House, New York, NY. INFORMATION: Barbara Jeffe, Pratt Ctr, 505 White Plains Rd, Tarrytown, NY 10591. Tel: 914/631-8772

**DEC 12-16—Advances in Digital Signal Processing: Analysis, Synthesis, and Applications; DEC 12-16—Modern Communications and Signal Processing; AND DEC 14-16—Multi-User Communication Systems and Networks**, George Washington Univ, Washington, DC and Seapoint Hotel, San Diego, Calif. INFORMATION: Continuing Engineering Ed, George Washington Univ, Washington, DC 20052. Tel: 202/676-6106; 800/424-9773 (outside DC)

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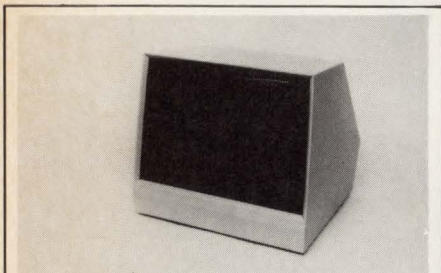
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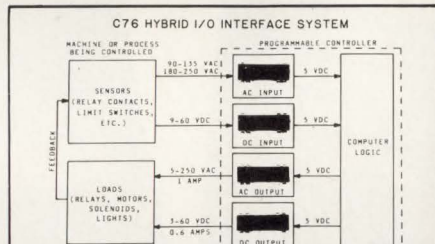
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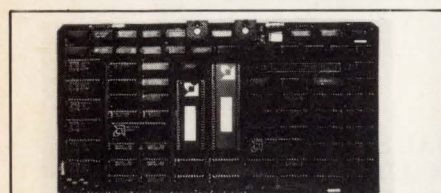
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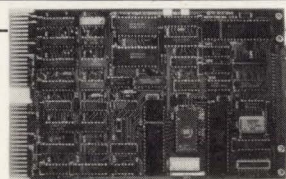


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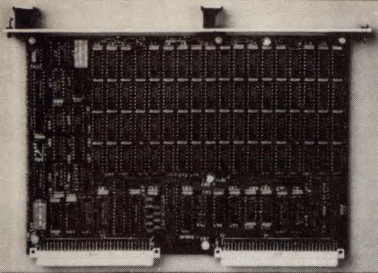
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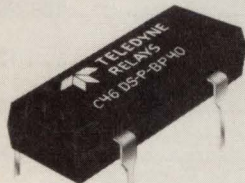


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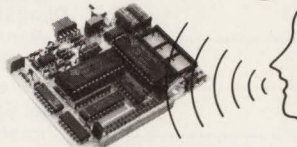
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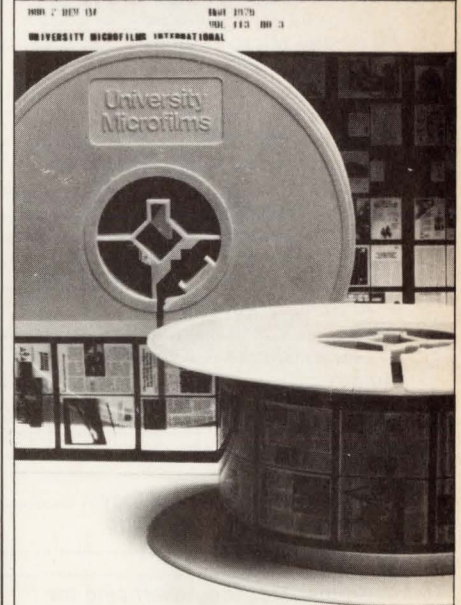
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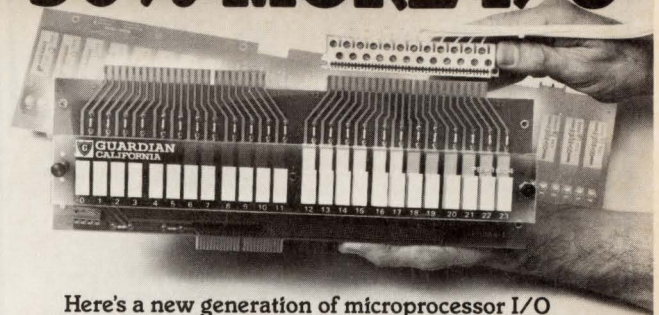
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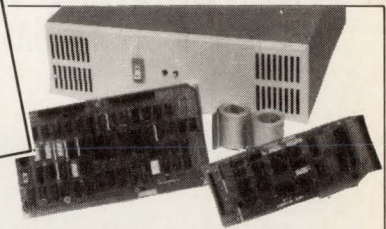


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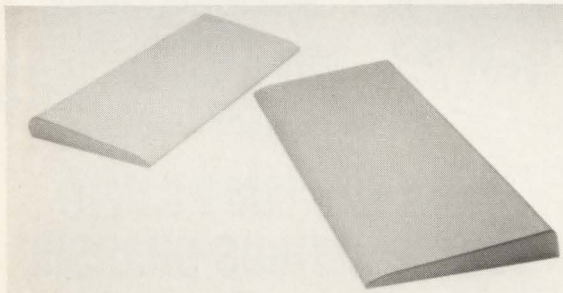
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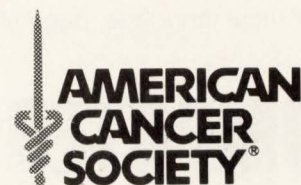
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