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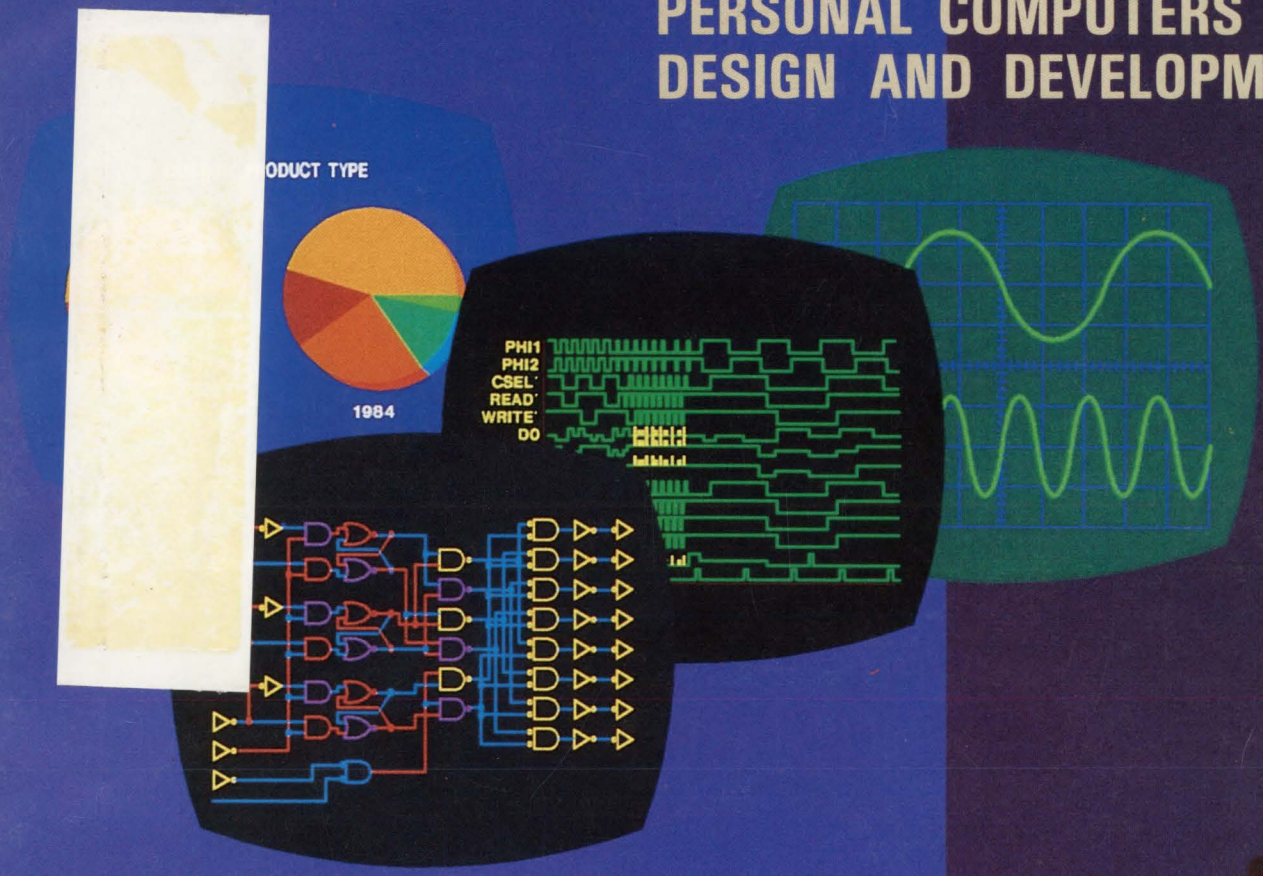
NOVEMBER 1984

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

PERSONAL COMPUTERS FOR DESIGN AND DEVELOPMENT



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PROGRAMMING LANGUAGE COMBINES BEST OF THREE WORLDS

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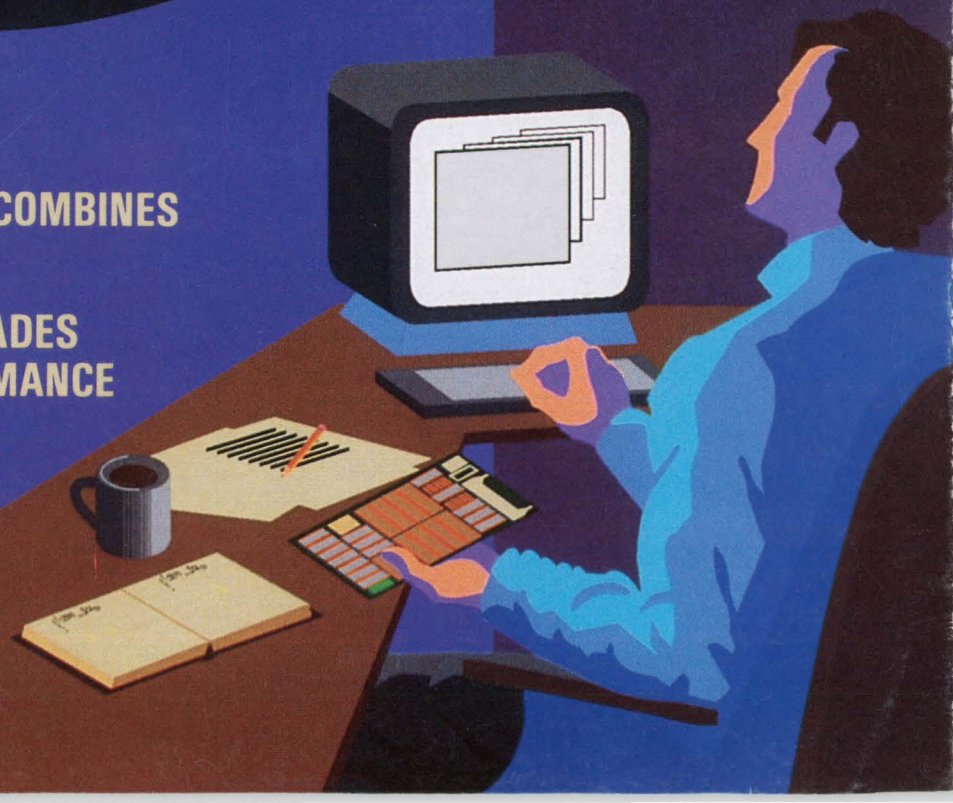

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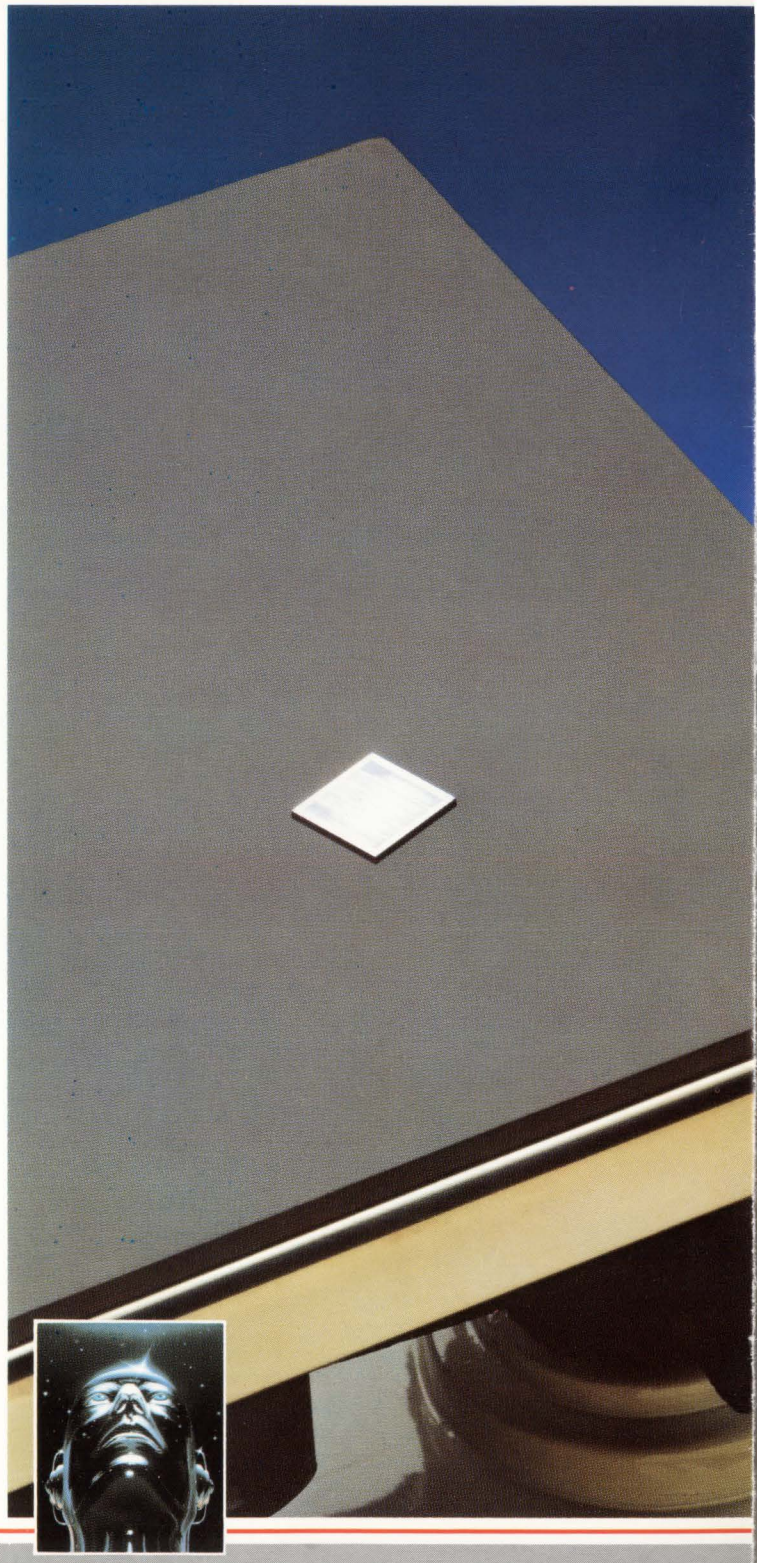

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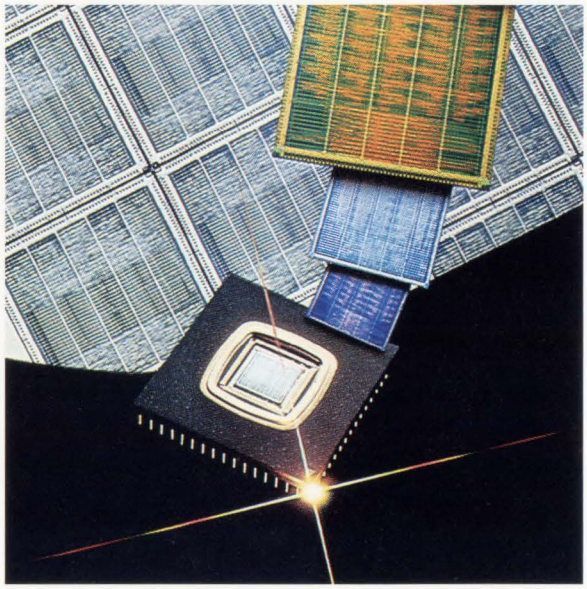

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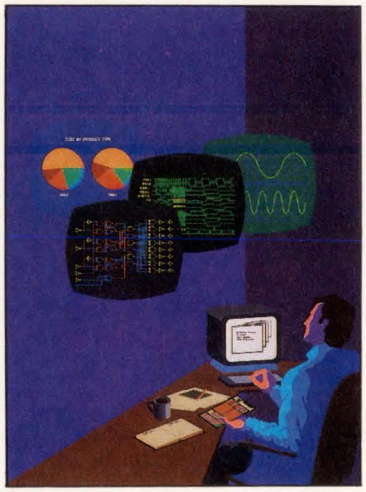


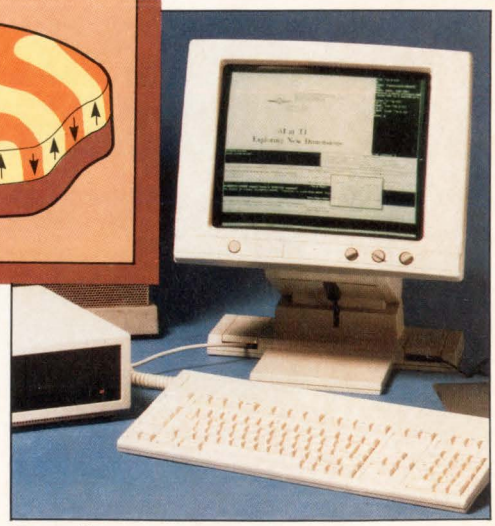
This month's cover was designed and created by Steve Branch at Coddbarrett Associates, Inc. It was executed using a Dicomed D-38 design station and a D-48 high resolution film recorder.

SPECIAL REPORT ON

PERSONAL COMPUTERS FOR DESIGN AND DEVELOPMENT

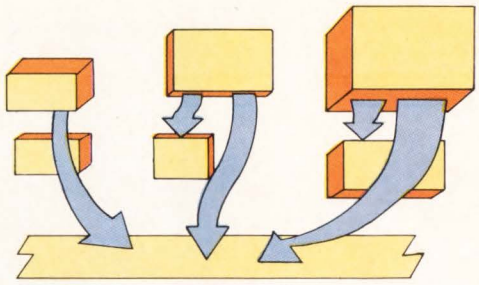
SYSTEM TECHNOLOGY

Page 30



Page 45

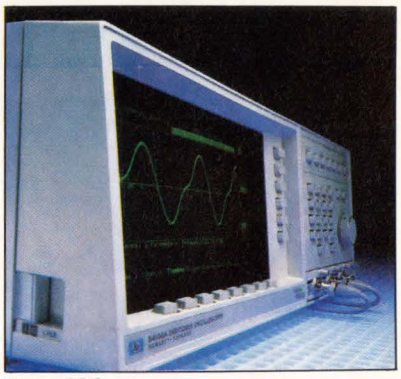
SYSTEM DESIGN



Page 133

DEPARTMENTS

SYSTEM COMPONENTS



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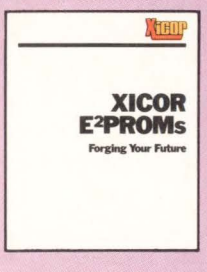

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CIRCLE 3

UP FRONT

Fifth-generation computers and the emperor's new clothes

Not everybody at the recent Association for Computing Machinery's annual conference was enthusiastic about "the challenge of the fifth generation." The opening panel nearly glowed with optimism until an unscheduled speaker, former ACM president Dr Herbert Grosch, took to the podium. "The emperor is naked from the ankles up," Grosch thundered, referring to fifth-generation technologies. "All he's wearing is a heavy pair of wing-tipped shoes. Those are expert systems, and we've had them for 30 years. All the AI boys did is relabel them." Grosch admonished everyone to resist "greedy entrepreneurs" and "journalists with crazy stories," and declared that most of the technologies being discussed won't be available for decades.—*R.G.*

Connection between incompatible systems made easier

Communication software packages from Advanced Computer Communications (Santa Barbara, Calif) and Network Research Corp (Santa Monica, Calif) are bringing users closer to the day when they can access various computers independent of their architecture or operating systems. Advanced Computer Communications' ACCES and Network Research's FUSION packages incorporate levels 3 through 7 of the ISO Open Systems Interconnection model. The latest addition to the ACCES family is a Virtual Terminal Service (VTS), a software package (written in C) that provides transparent communication between terminal and host on a multivendor, multi-operating system network. Meanwhile, Network Research has released its version 3.0 of FUSION for the VMS operating system and systems incorporating the TCP/IP protocols. FUSION is geared toward implementation in local area networks where incompatible processors and operating systems must be made compatible to network hardware from a variety of vendors.—*N.M.*

Laser reveals logic states at chip level

Mechanical probing of VLSI chips to determine logic states may become obsolete. An IC laser logic analyzer developed by the startup Dataprobe, Inc (Santa Clara, Calif) and built off-shore by Mitsui & Co (Franklin Lakes, NJ) represents the first commercial use of a laser to analyze IC logic states. An external pattern generator is used to exercise a delidded IC while a helium-neon laser beam probes a circuit node, causing photocurrents in the illuminated transistor. Depending on the logic state, the coupling of the induced photocurrents to the power bus will differ. This variation in current determines the logic state of that node. More than 3 nodes/s can be automatically accessed to record logic states throughout the chip. Unlike mechanical probing, the system is noninvasive and does not disturb the passivation layer.—*J.B.*

Cost sets pace for computer integrated manufacturing

Computer integrated manufacturing is at least 10 years in the future. Some recognized experts say even 15 may be optimistic. But that may not be the only problem. Speakers at the recent Autofact conference in Anaheim, Calif stressed the cost—crucial for small companies—and the need for technological breakthroughs. They point out that many of the smaller companies will find that less sophisticated automation will suffice. But 21st-century solutions for the major manufacturers will be based on revolutionary approaches, particularly more advanced artificial intelligence.—*S.F.S.*

Custom building with 32-bit bipolar blocks

A family of VLSI bipolar 32-bit parts has been developed by Advanced Micro Devices (Sunnyvale, Calif). Called the Am29300 family, the parts differ from AMD's earlier bipolar bit-slice parts in that they are specifically intended as building blocks for 32-bit processors for which the designer can develop application-specific architectures and instruction sets. The family consists of a 32-bit ALU with an onchip 64-bit funnel shifter, a 64- x 18-bit register file, a floating point processor, and a 32- x 32-bit parallel multiplier. In addition, there is a 16-bit sequencer with realtime interrupt. The family is intended to fill a power/flexibility niche between standard 32-bit microprocessors and full custom CPUs.—*T.W.*

Another Eagle leaves the nest

Putting serious pressure on disk drives in larger form factors, Fujitsu's latest ups the ante to 689 Mbytes. Retaining the actuators, heads, and media of its 10½-in. Eagle drives (considered the epitome of Winchester technology), the new drive also provides an 18-ms average positioning time. Accompanying the 45 percent increase in capacity is an increase in transfer rate—from 1.8 to 2.4 Mbytes/s. Such a rate increase helps solve the throughput problems encountered in multi-user systems.—*P.K.*

Datakits for budget-minded users

One Datakit virtual circuit switch (VCS) for some 100 physical connections and another that can switch up to 2500 virtual circuits are the latest additions by AT&T Network Systems (Morristown, NJ). The VCS product family is basically local area networks that use a star topology with a centralized short bus. This bus allows virtual circuits to be switched at an 8-Mbit/s rate using packet switching technology. Datakits can be connected using twisted-pair copper wire or fiber optic cable. While designed for telephone companies and extensively used within AT&T, the latest Datakit models are geared toward smaller businesses that prefer to maintain the compatibility and reliability provided by AT&T.—*N.M.*

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DATARAM

CIRCLE 4

UP FRONT

Syte fades from view

Syte Information Technology, a startup based in San Diego, Calif, has abruptly closed its doors on the very eve of its first product shipment. Syte had been promised a $4 million dollar second round of financing from its original investors if it could raise another $2 million from outside sources. When it failed to do that, the investors pulled the plug. Still up for grabs, apparently, is the company's main technology, the Global Environment Manager (GEM). This operating system kernel can wed different operating system environments in different hardware systems—all transparent to the user. As of this date, Syte has reported no takers for the sale of GEM.—*T.W.*

A "low cost" 64-bit supercomputer

Brought to you by the star in Tracy Kidder's book, *Soul of a New Machine*, is the Convex (Richardson, Tex) C-1. Steve Wallach's latest project introduces interactivity to supercomputers. The C-1 combines key characteristics of traditional supercomputers with the packaging of minicomputers. It opens up 64-bit scalar and vector processing at rates around 60 MIPS in a broad range of scientific applications. The price is under $500,000.—*P.K.*

T&M giants move slowly with EE software

The computer aided engineering workstation has been ignored by traditional automation and engineering companies for so long that a healthy crop of young companies has grown to near maturity serving that demand. Recently, however, on-the-job automation has grabbed the attention of major suppliers like IBM, Hewlett-Packard, and Tektronix. But, these companies are holding back on the introduction of CAE software for electrical engineers, probably until early 1985. One Hewlett-Packard spokesman says he feels that enough in-house software is ready for introduction on its workstation. He also notes that because the software has been developed for in-house use, the company is probably waiting for adequate documentation to be developed before announcing products. Tektronix may be in the same position. Many engineering companies have developed such software for internal use, but documentation is not up to customer standards. The question is will Tektronix and Hewlett-Packard move into the CAE engineering market quickly enough? Just a month ago, it looked as though the opportunity to serve the technical and scientific communities had been forfeited to IBM, with its announcement of the PC AT and the host of follow-up announcements of GPIB capabilities and graphics enhancements. Maybe it isn't too late for the others.—*B.F.*

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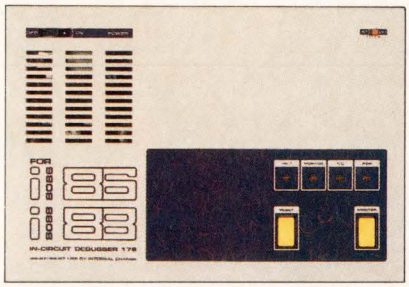

i8086/88

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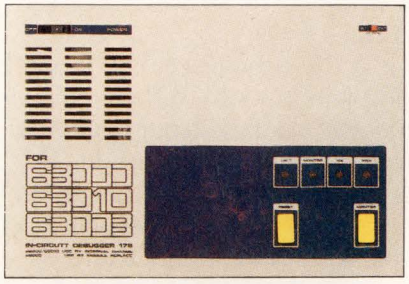

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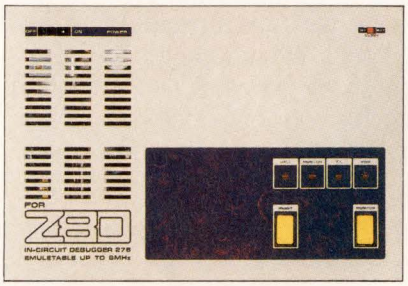

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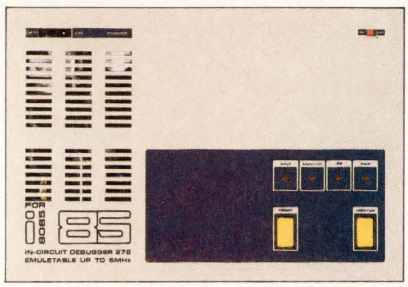

i8085

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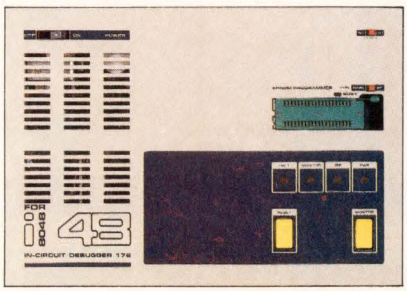
- i8085A-2



i8048

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- i8050
- i8748
- i8749
- i8039
- i8035
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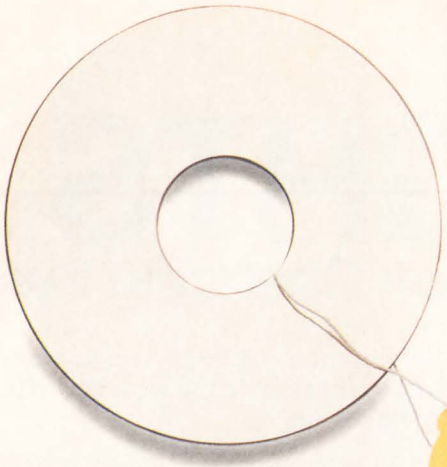
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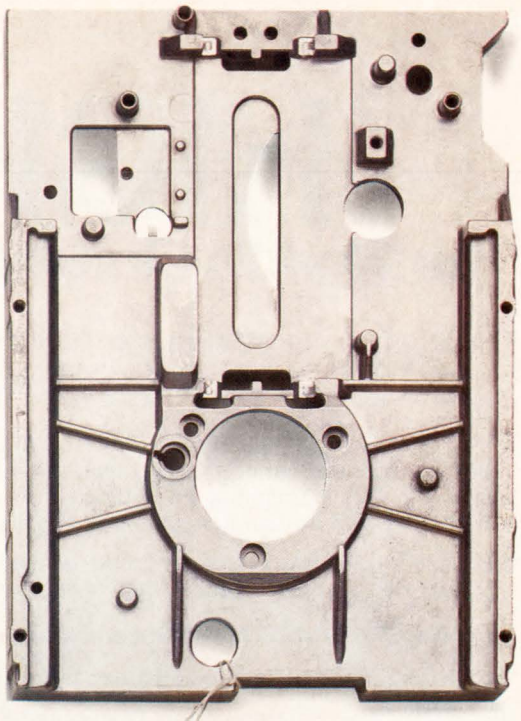
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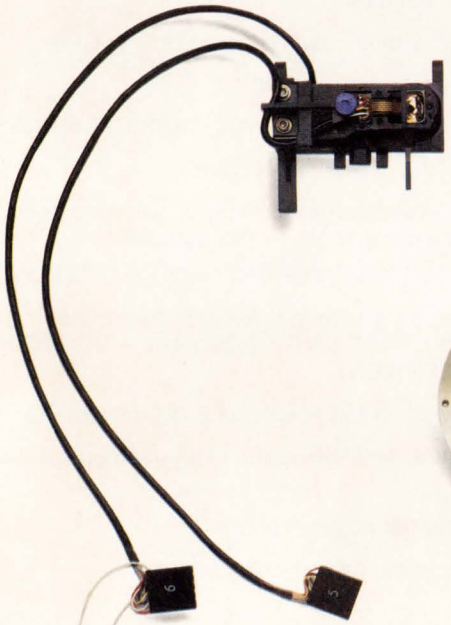
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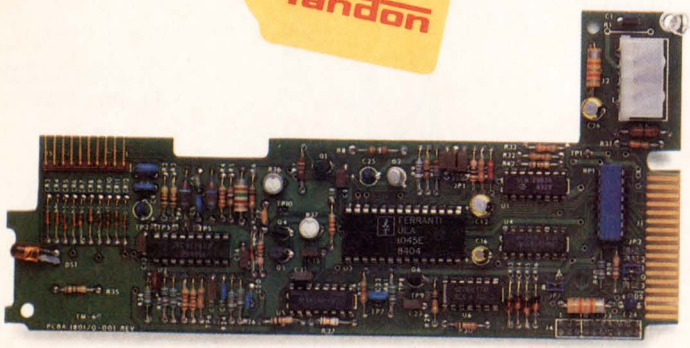
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CIRCLE 7

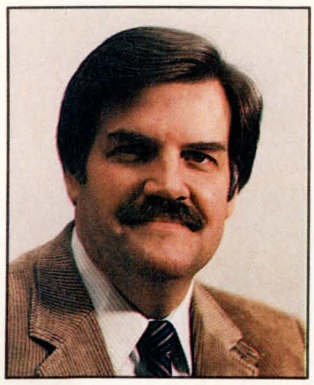
SHARING THE LOAD

Back-to-back editorials on management techniques might seem like overkill, but being the new kid on the block at *Computer Design*, it's natural that management concerns are high on my list of priorities. Faced with new challenges, I did what every good scientist or engineer does—research. I scurried off to a local book store and surveyed the shelves marked "Management." There were titles such as *Managing for Results*, by Peter Drucker (every manager should know Drucker) and *Modern Management Techniques in Engineering R&D*, written by a consultant and three PhDs. Now this last one was heavy stuff, but not exactly what I was looking for. My search ended with a book entitled *Managing for Excellence*, by David L. Bradford and Allan R. Cohen. This book proved to be much more than I expected. It helped clarify and confirm some ideas about the editorial approach *Computer Design* should follow in view of the complexity of the design, test, and manufacturing problems faced by builders of state-of-the-art computer-based products.

In their book, Bradford and Cohen go beyond the much-touted concept of quality circles. At the heart of their management philosophy is the concept of shared responsibility. At first glance, the two appear the same because everyone seems to get involved in the decision-making process. The quality circle, adapted to American industry, however, still casts most participants in the role of "recommenders" with a technical "hero" or an organizational "hero" calling the shots and riding to the rescue when "needed." But, in today's industrial world, engineering problems are often too technically complex for one individual to comprehend fully. What's more, many organizations are often too large and their elements too closely related for any one person to coordinate them effectively.

The concept of shared responsibility, on the other hand, demands that every participant assume a measure of responsibility for the success of the entire organization. For shared responsibility to work, however, everyone must measure up to their role. This requires active development of every participant's technical and/or organizational abilities to the highest levels possible—levels that exceed, at least in specific areas, those of "managers."

There's probably no better example of a complex management environment than the development cycle of a computer-based product. Each development phase—from initial product specification to hardware design, programming, integration, production testing and manufacturing to marketing—requires a high level of expertise. Furthermore, the complex relationship between the different phases of the development cycle make the task of coordinating them overwhelming. Since no individual can be an expert in every area, the manager as heroic technician or heroic organizer has become an anachronism in the business of making computer-based products. More so, perhaps, than in any other segment of industry.

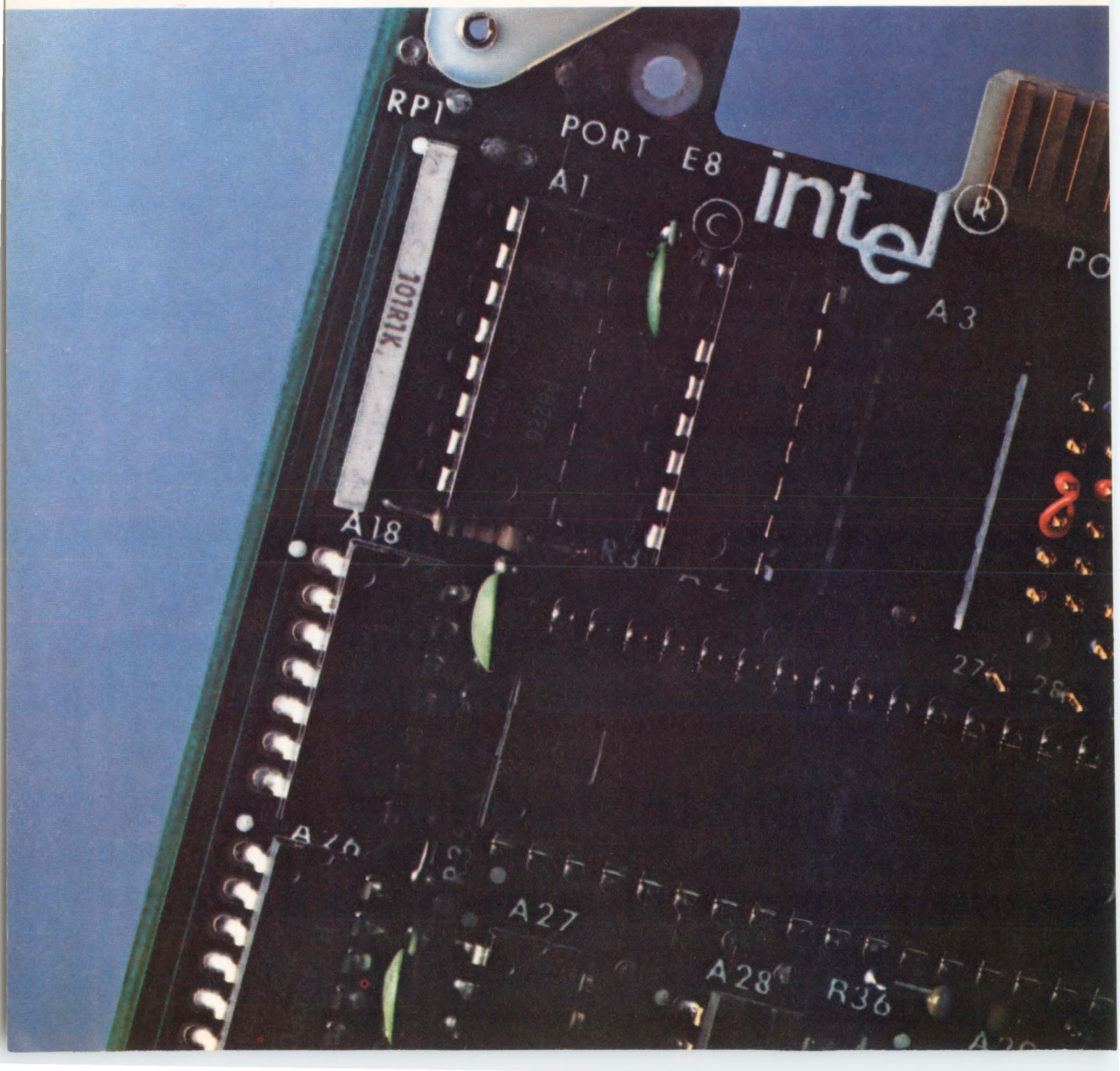


Shared responsibility provides one solution. It requires that all participants have a thorough knowledge of their own areas of responsibility, as well as a knowledge of how their decisions affect others and how the decision of others affect them. Decisions made about product specifications, hardware, software, test capabilities, and manufacturing processes reverberate throughout the entire development organization. And a bad decision can produce "cracks" that are costly to patch.

If publications serving the engineering community aren't to become anachronisms—especially *Computer Design* which serves managers, senior engineers, and others that will have to make critical design decisions—we must always emphasize the relationships that exist within the design process and between the design process and the other phases of product development. The temptation to discuss hardware, software, testing, or whatever, in isolation is great. The editorial life is much simpler that way, but the resulting editorial product isn't all it could be. To make shared responsibility work we have to share in that responsibility by providing the new decision maker with the wide-ranging perspective needed.

John Miklosz
Executive Editor

THE BEST PLACE TO BOARD THE BUS.



Of course, we're talking about the MULTIBUS® architecture. The most widely accepted, best supported bus architecture in the world.

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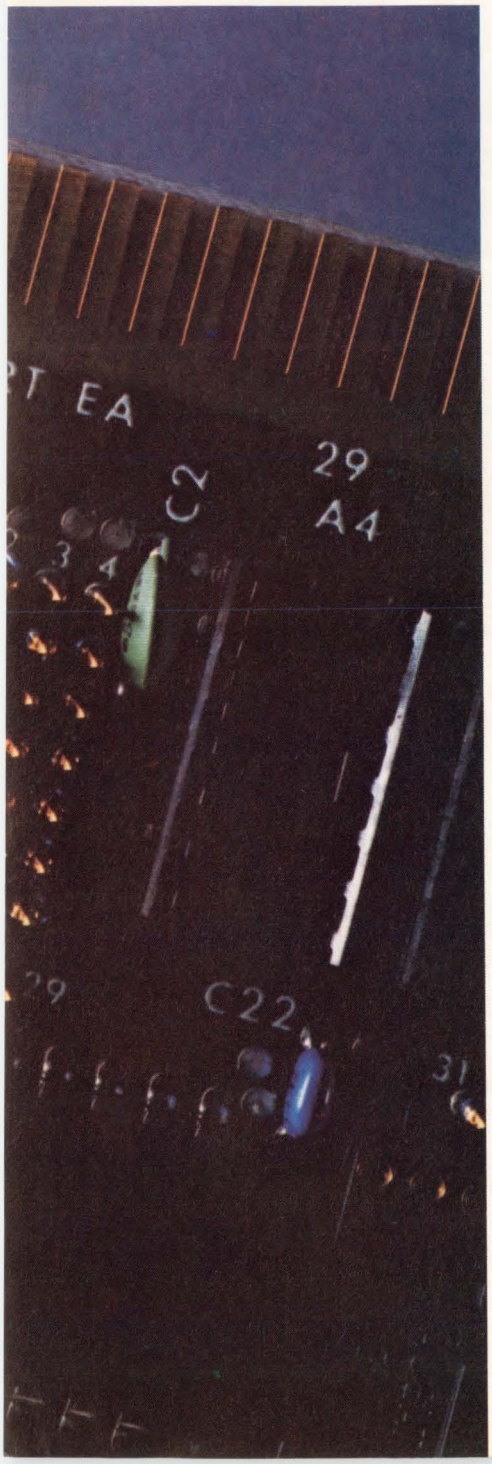

Right here. Because as you might suspect, we know just about all there is to know about MULTIBUS. After all, we invented it. And we have the largest selection of MULTIBUS products to be found. Anywhere.

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Then there's the selection. A big one.

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CIRCLE 8

COMPUTER DESIGN

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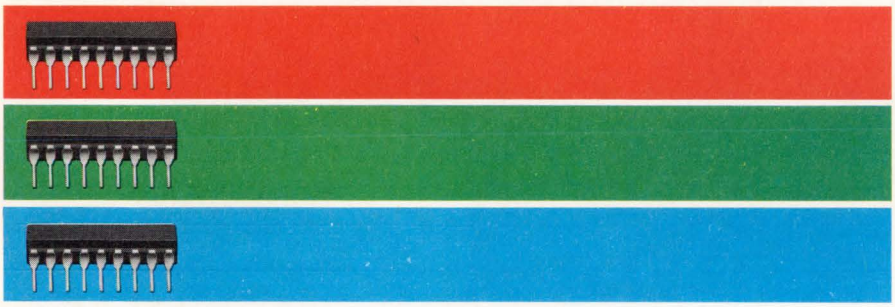

Give yourself a head start with a monolithic DAC designed specifically for raster scan systems—the TRW TDC1034 4-bit, 125 MSPS D/A converter. It directly drives CRTs to video compatible levels. Save on circuitry—no extra registering, buffering or deglitching. Save space—the 4-bit TDC1034 is an ultra-thin 18 lead DIP.

And you get terrific performance. This monolithic 4-bit DAC is ideal for either monochromatic or RGB color raster graphics (4096 colors!). Its high speed scans more pixels per picture to produce razor sharp high resolution displays. And because it's built with TRW's OMICRON-B™ 1-micron bipolar process, you get high reliability and low power consumption (600mW).

The low-cost 4-bit TDC1034 is your one chip solution to high volume production of CAD/CAM work stations, computer graphics, and high resolution video. If your application needs all the options that an 8-bit, 24 lead DIP offers, consider the TDC1018—the first monolithic 8-bit, 125MSPS D/A converter.

Check these key performance features:

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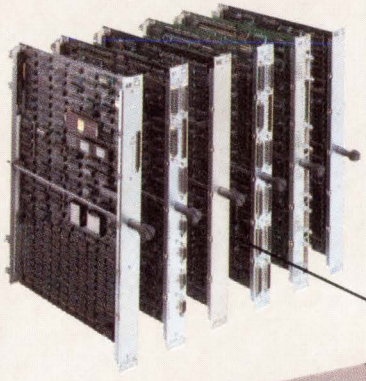
CIRCLE 13

IT WILL GROW ON YOU.



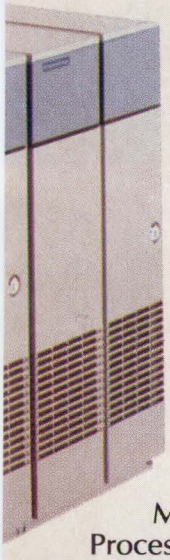
CONFIGURABLE ACCORDING TO USER NEEDS. As many as six processors can be installed in each enclosure. CPU-intensive jobs utilize multiple Applications Processors. Systems with heavy disk usage can distribute this load among several File Processors. The number of user ports can be increased by adding more I/O Processors.

MODULARITY EXTENDS TO DISK STORAGE. Compact 50 or 140 Mbyte Winchester modules simply plug in . . . four per cabinet. Optional external SMD drives are also supported. File backup utilizes Winchester cartridges, ½-inch magnetic tape, or both.

MegaFrame™. Now OEMs can offer a high-performance UNIX™-based system that can't run out of performance.

OEMS can now deal cost-effectively with the problems encountered when user applications produce computing demands that outstrip the capabilities of conventional systems.

Convergent Technologies' MegaFrame is a revolutionary new UNIX-based super-minicomputer—so innovative in its architecture that it represents the ultimate in multiuser systems design. It grows exponentially from a system offering minicomputer-level performance to an enormously powerful engine serving as many as 128 users with 36 parallel processors, 24 megabytes of RAM and gigabytes of disk storage.



No other system can match the MegaFrame's potential for field expansion. It enables manufacturers and systems builders to keep pace with today's requirements for more and more computing services . . . but *not* at the cost of discarding hardware or performing expensive CPU upgrades.

MegaFrame's architectural breakthrough. Dependence on traditional single-CPU shared-logic architecture is the root of systems bottlenecks.

Convergent's response: a novel system utilizing *multiple* specialized processors to distribute workloads for optimum performance—even if user needs are unpredictable or subject to rapid change.

MegaFrame's virtual memory Applications Processors each have a 32-bit CPU, up to 4 Mbytes of RAM and run a demand-paged version of UNIX System V. Up to 16 of them can operate in parallel.

The File Processors effectively function as back-end machines providing DBMS, ISAM and other disk-related services. Up to six File Processors each with four disks can operate in parallel.

Terminal and Cluster Processors can also be added—the latter serving front-end communications needs. They off-load communications from the other processors by running protocols such as SNA and X25 networks.

MegaFrame's daisy-chained cabinets offer total expansion potential of up to 36 slots. OEMs configure the system needed for specific applications simply by adding the correct number/combination of processors.

Flexibility in applications development. Inclusion of one or more Applications Processors allows running UNIX System V. All standard UNIX tools are provided, along with COBOL, FORTRAN-77, BASIC interpreter and compiler, plus Pascal.

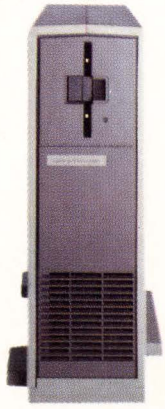
The "least-cost solution" to serving a wide range of UNIX-systems needs, MegaFrame has won acceptance from OEMs in the U.S. and abroad. The uniqueness of its modular design, its versatility in providing upgrade-path options and its price/performance advantages give it market-share potential of outstanding dimensions.

The system that will grow on you starts at a very attractive price: about $20,000 for a system that effectively supports 16 users. Send now for a comprehensive Information Package including reprints of magazine articles. It explains how MegaFrame's growth potential can impact favorably on your plans for growth in the UNIX market.

Convergent Technologies, Data Systems Division, 3055 Patrick Henry Drive, Santa Clara, CA 95050. Phone: 408/980-0850. Telex: 176-825.

MiniFrame™: the entry-level multiuser UNIX system.

Starting at under $5,000 for a single-user system, Convergent's MiniFrame offers outstanding capabilities for small to medium sized organizations running large UNIX-based applications. Utilizing an MC68010 microprocessor operating at 10Mhz, with no wait states, it provides impressive CPU speed—comparable to VAX™-11/750 running the AIM™ Benchmark. MiniFrame features virtual memory management, with demand-paged implementation of UNIX System V. It runs as many as eight terminals, with up to 50 Mbytes of integral mass storage. MiniFrame and MegaFrame are object-code compatible, allowing OEMs to offer a *complete family* of systems unrivaled in price/performance characteristics.



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give you 150 ns speed μA power. Pick a winner.

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The high-density HCMOS MCM65256 low-power leader's maximum power dissipation is only 50 μA in standby with full rail inputs, 5 mA in standby with TTL inputs and just 50 mA, active. However it still offers a fast 350 ns access time, and just 100 ns max. from output enable.

Certainly speed is the biggest attraction of the high-performance N-channel HMOS MCM63256, yet maximum power dissipation is a low 15 mA, standby, and 100 mA active.

There's also a 200 ns version of the MCM63256, and matching high-speed 128Ks are available, too.

All in the industry-standard 28-pin family.

Beyond the ideal differences in their speed and power, these advanced-technology ROMs share many common operating characteristics and benefits, including availability now in the JEDEC-standard 28-pin dual in-line package.

They utilize late-process programming to minimize prototype turnaround, and they require no clocking on the chip enable because they're static. They operate from single +5 volt supplies, shift automatically into the power-down mode, and offer user-selectable address and mask-programmable chip and output enables.

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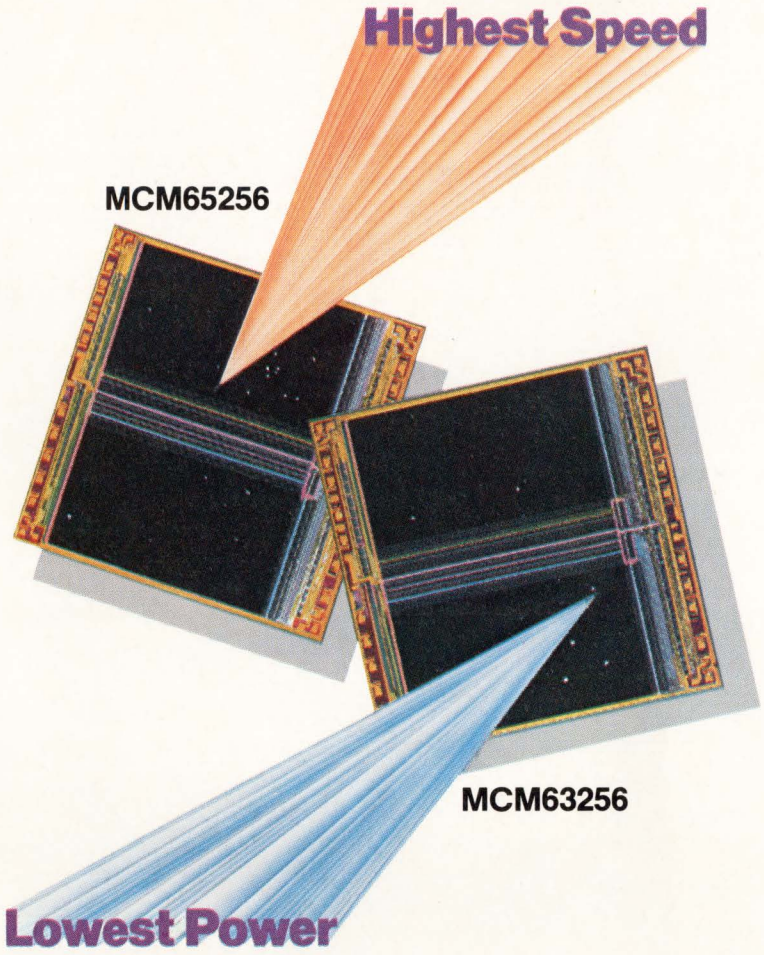

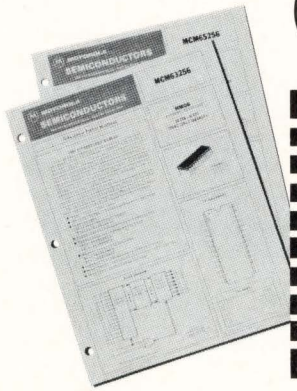

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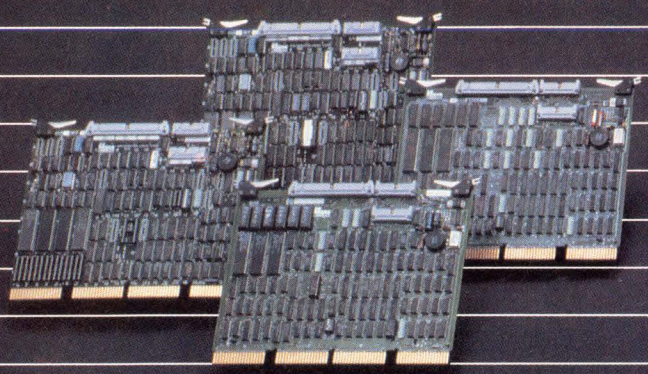

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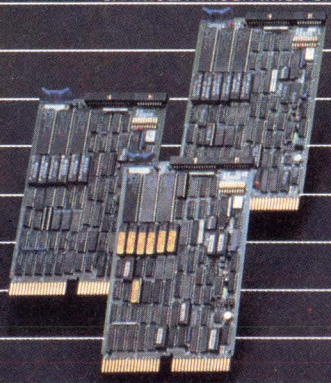

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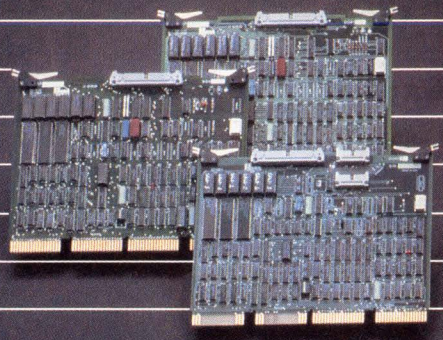

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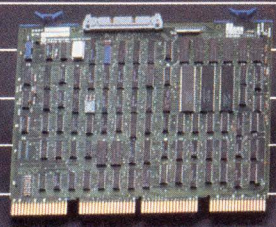

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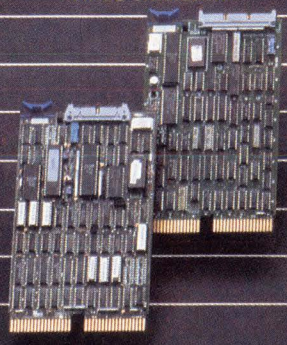

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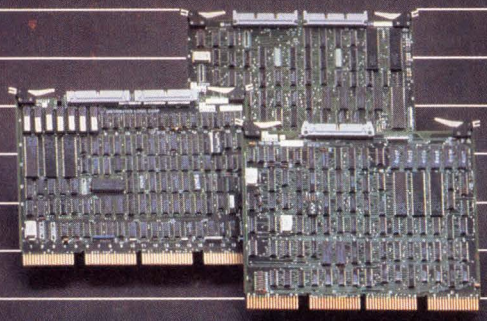

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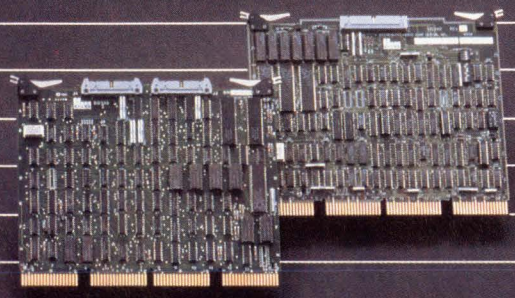

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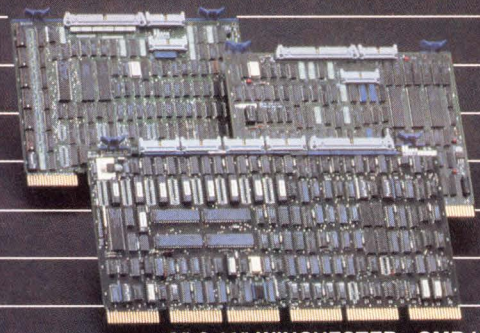

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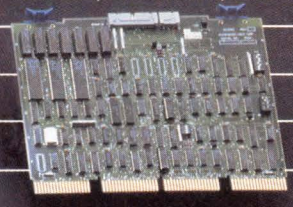

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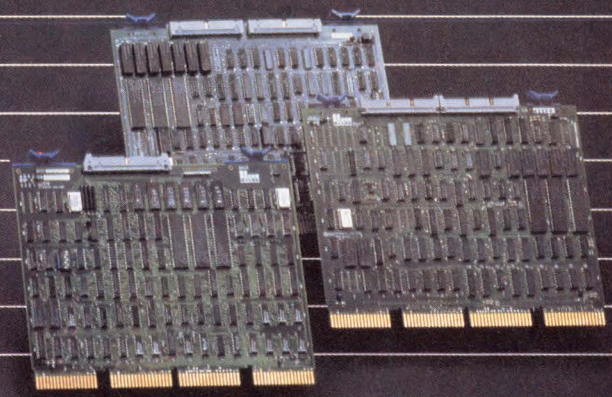

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CIRCLE 15

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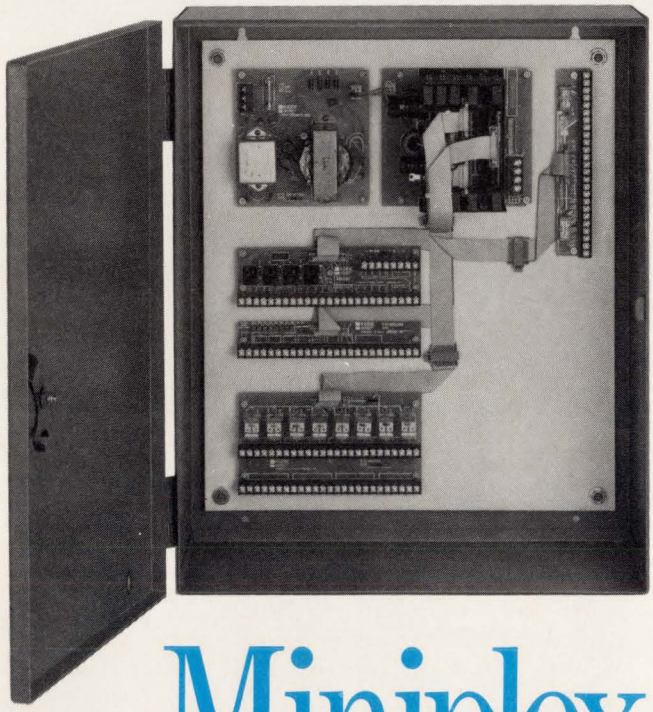

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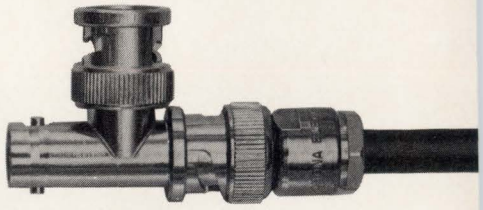

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Network Communications for Industry

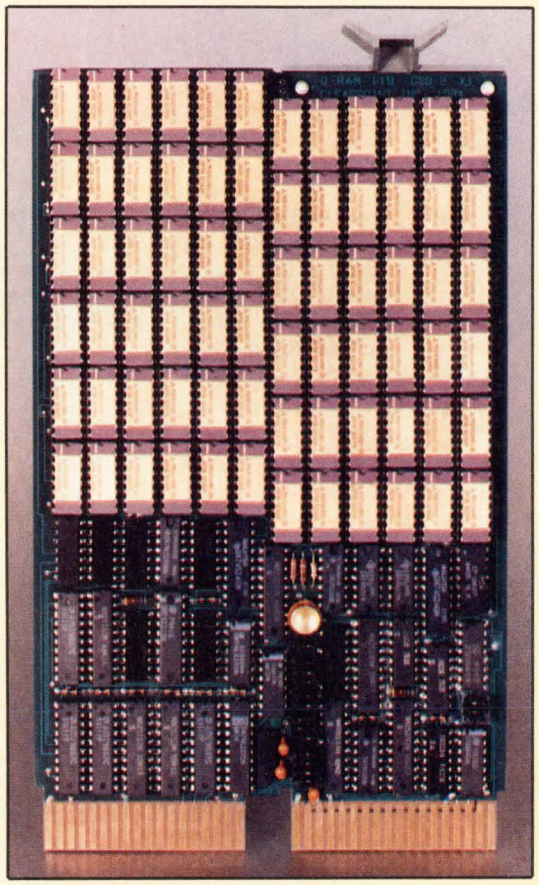
CIRCLE 16

Compatible memories bridge gaps for DEC minicomputers

The rapid expansion of main memory capacity in minicomputers has triggered calls for add-in and add-on memory and new demands for massive secondary storage. Demand for disk drives storing 300 Mbytes and more has soared, followed by a rise in demand for tape subsystems packing over 100 Mbytes on a single reel.

Independent manufacturers of minicomputer peripherals are thriving in this environment because of the rapid growth of the minicomputer industry and the inability of CPU manufacturers to dedicate sufficient resources to build the variety of storage devices that their customers demand. The sheer number of DEC minicomputer installations makes DEC compatibles a particularly busy area.

Along with these demands for larger storage capacities, concerns about how fast the data can be passed to and from the CPU have grown. Brought about by the increasingly multi-user, online nature of the minicomputer's typical application, storage peripheral manufacturers have shown intense awareness of access time and have devoted much attention to its improvement. Minicomputers have benefitted most from the resulting developments because of their relative position on the cost/performance curve. Since half of the total equipment cost in a computer installation is typically devoted to peripherals, a system in the $100,000 range can afford the relatively high price associated with high performance peripherals such as tape and disk drives.



With large, fast memory modules designed to plug into DEC's Q-bus CPUs, Clearpoint's Q-RAM 44B uses 256-Kbit DRAMs to supply 2 Mbytes of capacity on a single card.

Speed-critical applications

Several approaches result in more speed than can be achieved from a disk-based subsystem for realtime applications. U.S. Design Corp's (Lanham, Md) system can access 760 Mbytes of data in less than 10 ms. To achieve this, the VIP/X manages multiple independent disk actuators. Its controller uses several microprocessors in conjunction with 512 Kbytes of onboard multiported cache memory. By operating each actuator independently, contention problems can be virtually eliminated in multi-user environments.

Another high speed approach uses solid state disk emulating systems. In this case, Imperial Technology Inc's (El Segundo, Calif) MegaRAM-11 supplies up to 16 Mbytes of data storage and directly emulates various DEC disk drives such as RK06 and RK07. Use of semiconductor memories eliminates the seek time that limits the access speed of disk drives.

To serve applications in the 10-Mbyte/s range (typically the province of fixed-head disk subsystems), Dataram Corp (Cranbury, NJ) packages up to 40 Mbytes in a box that can supply data at a 200-Mbyte/s rate. Called Wide Word 2000, the memory subsystem uses 8-way interleaving and internal data words up to 160 bits wide to achieve these transfer rates. Typically, systems are dual-ported with one accepting high speed input and the other providing a link to the minicomputer.

To belong to the high performance minicomputer club, memory arrays must be large and provide fast access to data. Buying add-in and add-on

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Compatible memories

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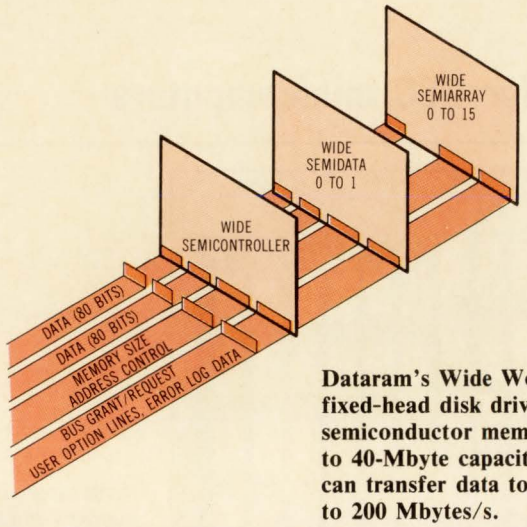


Dataram's Wide Word 2000 replaces fixed-head disk drives with semiconductor memory. Supplying up to 40-Mbyte capacity, the subsystem can transfer data to the CPU at rates to 200 Mbytes/s.

memories from outside vendors can save up to 50 percent, a major factor considering the size of most memories. Not only that, but these outside sources frequently use the latest in semiconductor technology (eg, 256-Kbit RAMs before they become available from the CPU vendor). Thus, memory can be extended without using more slots in the CPU backplane. These come in 64- to 1024-Kbyte versions for Q-bus machines and in 256 to 1024 Kbytes for Unibus and VAX systems.

Faster, larger main memory

Equivalent to DEC's MS780-E, a field replacement memory system for VAX-11/780 uses 2048-Kbyte memory arrays to allow 32 Mbytes/backplane, instead of the original 16 Mbytes. Installed in the CPU cabinet with 4 Mbytes, EMCVT-780-4MB from EMC Corp (Newton, Mass) sells for less than $27,000, 30 percent less than a comparable DEC upgrade. The system is fully compatible with the CPU and requires no modification the to VMS or Unix operating systems.

Raising main memory of the 11/750 to 8 Mbytes from its previous 2-Mbyte limit, a 2-Mbyte minimum upgrade kit from EMC can be field installed. The kit sells for $11,500; additional 1-Mbyte cards are $2450. National Semiconductor Corp, Memory Systems Div (Santa Clara, Calif) provides 256- to 1024-Kbyte memory arrays for both Unibus and VAX systems as well as 64- and 1024-Kbyte versions for Q-bus machines.

Implementing block mode DMA protocols on the Q-bus, ADAC Corp's (Woburn, Mass) 18MP-1024 supplies timing, control logic, refresh, parity control, and status register. Featuring 22-bit addressing, dual-height, half-quad 256- or 512-Kbyte 18 MP boards allow plug-programmable selection of 18-bit addressing. General Robotics' (Hartford, Wis) MSV11-Q replaces two or more DEC MSV11-P modules. The 1-Mbyte single-quad height board has 255-ns read access time, 280-ns write time. A high speed MSV11-QH version performs about 40 percent faster. Capable of read and write access time of 60 ns, the Q-RAM 11B from Clearpoint, Inc, (Hopkinton, Mass) uses 64-Kbit DRAMs to supply 512-Kbyte capacity on a dual-height card. A 2-Mbyte module, the Q-RAM 44B uses 256-Kbit DRAMs and offers 85-ns read and 60-ns write access times.

Supporting mass storage demands

Virtual memory addressing capability of systems like the VAX runs to 2 Gbytes. Supported by the Digital Storage Architecture (DSA), disk drives and tape drives capable of handling masses of data can be mixed and matched to fit system needs. Storage Module Drive (SMD) Winchester disk drives and half-inch tape drives typically take care of online storage tasks. Transfer rates for disks run in the 2-Mbyte/s and up range with tape drives capable of rates to 160 kbytes/s.

Matching the capacity of DEC's top of the line RA81 disk drive, the Aquarius II, a high performance data storage system, meets capacity needs of VAX and PDP-11. Designed for use over VAX CMI, SBI, or Unibus, the unit from First Computer Corp (Westmont, Ill) supplies 474 Mbytes on a Fujitsu Eagle Winchester disk drive and provides magnetic tape backup using a GCR CacheTape drive from Cipher Data. The system accommodates up to three disk drives and sells for from $29,990 to $51,450.

A Winchester/cartridge tape combination, Emulex's Medley supplies 35 or 110 Mbytes of formatted storage as well as 70 Mbytes of streaming tape backup. Using the Small Computer System Interface, the subsystem is operating system- and diagnostics-transparent to Q-bus and Unibus systems. The host adapter uses DEC's mass storage control protocol to adapt to various disk drives without operating system patches.

Cyclone series subsystems from Qualogy Inc (San Jose, Calif) offer storage capacities from 36 to 120 Mbytes formatted for Q-bus computers. Fully compatible with DEC's DSA, the subsystems incorporate Maxtor's 5-¼-in. Winchester disk drives with a quarter-inch cartridge tape drive (Kennedy 6455) capable of storing Mbytes. Average access times of 30 ms on the disk drive are enhanced by a complex data buffering scheme on the controller/interface that facilitates fast transfer of data to and from the Q-bus.

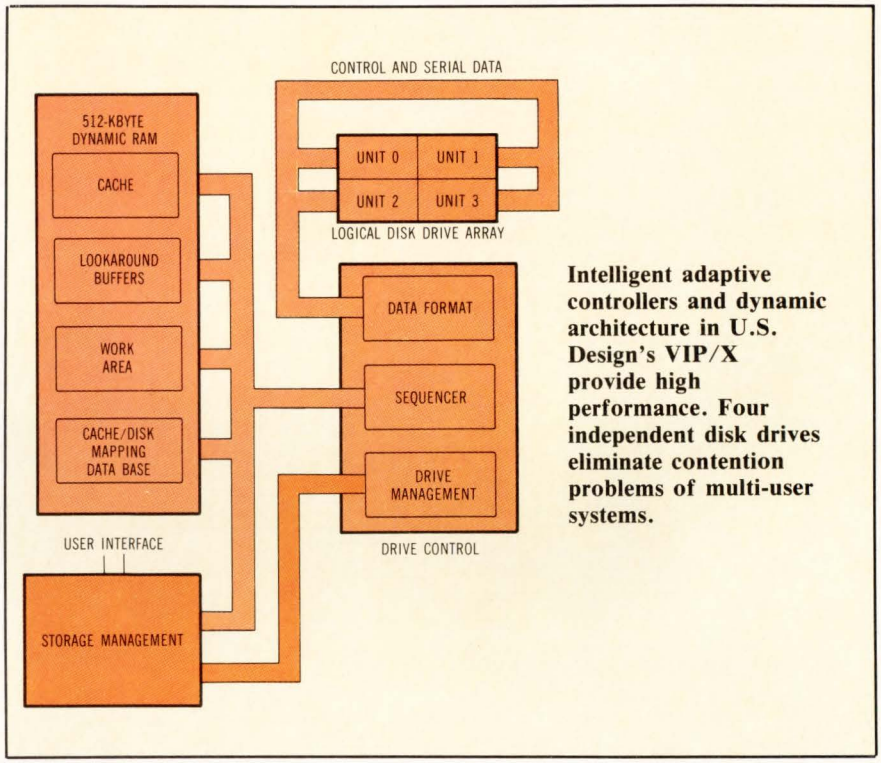
GCR tape drives for DEC machines provide easy backup for large data bases. Aviv's (Woburn, Mass) GCR-125 Tri-Density tape system, for example, can pack 140 Mbytes on a single tape reel. Recording 6250/1600/800 bits/in. at 125

in./s, the drives connect with DEC and support Pertec and Telex interfaces.

Interfacing to VAX, PDP-11/70, and Unibus machines, the System Industries' (Milpitas, Calif) 9621 operates at twice the speed of DEC's TU80. At 50 in./s, the dual-density tape system records at either 1600 or 6250 bits/in. and transfers data at rates up to 312 kbytes/s. Its integrated formatter/controller connects to Unibus, 11/70 Cache, 11/750 CMI, and 11/780 SBI.

Digi-Data Corp's (Jessup, Md) half-inch magnetic tape systems store up to 138 Mbytes on a single reel. Compatible at the system level with VAX, PDP-11, and LSI-11, the start-stop or streaming drives record at speeds from 12.5 to 125 in./s.

Designed for integration into various vendors' CPUs, GCR tape subsystems from California Computer Group (Costa Mesa, Calif) store 180 Mbytes on a single reel. Based on StorageTek's dual-density model 2920 Avalanche or Kennedy Co's tri-density model 9400 drives, the systems record on standard 10.5-in. reels of tape. Controllers from Emulex, Western Peripherals, Rianda, Spectra Logic, Macrolink, or Dylon serve as the drive-computer link.



Intelligent adaptive controllers and dynamic architecture in U.S. Design's VIP/X provide high performance. Four independent disk drives eliminate contention problems of multi-user systems.

Making the connection

Fixed-media Winchester drives from Control Data, Ampex, Century Data, Disk Tech One, Fujitsu, Kennedy, and Tecstor connect to Unibus systems over Distributed Logic Corp's (Garden Grove, Calif) DU218. This SMD interface-compatible RM02/RM05 controller provides software transparency with RSTS and RSX-11 operating systems. In addition, it is interchange compatible when used with removable pack drives such as the 80-Mbyte CDC 9762 and 300-Mbyte CDC 9766.

Emulating RM02, 03, 05, or RK06/07 disk drives, controllers from MDB Systems Inc (Orange, Calif) are software and diagnostic transparent to DEC operating systems as well as Unix and TSX. Interfacing SMD disk drives to Q-bus, Unibus, and VAX systems, firmware in the controller accommodates changes in drives by interrogating a switch as to drive in use and emulation mode. It automatically structures the firmware to identify drives by number of cylinders, sectors, and heads as well as number of blocks in each logical unit.

Transfer rates to 2 Mbytes/s for disk and 800 kbytes/s for tape are supported by Spectra Logic's (Sunnyvale, Calif) Spectra 121 disk/tape controller for Unibus systems. These data rates are achieved by a dual sequencer design based on a 16-bit 29116 microprocessor. Emulating RM02/05, RM80, and RP06 disks and TS11 tape drives, the board is compatible with RT-11, RSX-11M, RSX-11M-Plus and RSTS/E operating systems. Separate buffering for tape and disk allows simultaneous transfers at full speed while eliminating data late errors.

All those attempting to slipstream DEC's systems with storage devices are aided by the relatively open system buses. While hardly in the public domain, information necessary to gain access to these proprietary buses is certainly not guarded with the fortitude that IBM applies. In addition, Digital's DSA readily accepts performance variables, making the job still easier for those who wish to supply mass storage needs.

—Peg Killmon, Senior Editor

SYSTEM TECHNOLOGY

(continued on page 30)

EMULEX IMPROVES AND TAPE BACKUP BY

Emulex sets the pace with three great storage subsystems for the full range of DEC QBus and Unibus systems. Whether you need Winchester disk, cartridge disk, ¼" streaming tape, or a combination unit, you'll be a step ahead with Emulex.

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Emulex rises above the competition with the Vault.™ This 70-MByte tape subsystem is built around the CDC Sentinel ¼" cartridge tape streamer and uses Emulex's own TC05 (QBus) or TC15 (Unibus) tape coupler to interface with your system. The Vault is totally software transparent to standard TS11 software. So this compact tape unit looks just like a big ½" TS11 subsystem to your operating system and diagnostics.

Vault comes complete with power supply in a single compact cabinet. It's the perfect backup unit for smaller QBus systems such as the MICRO/PDP-11 and MICRO/VAX.

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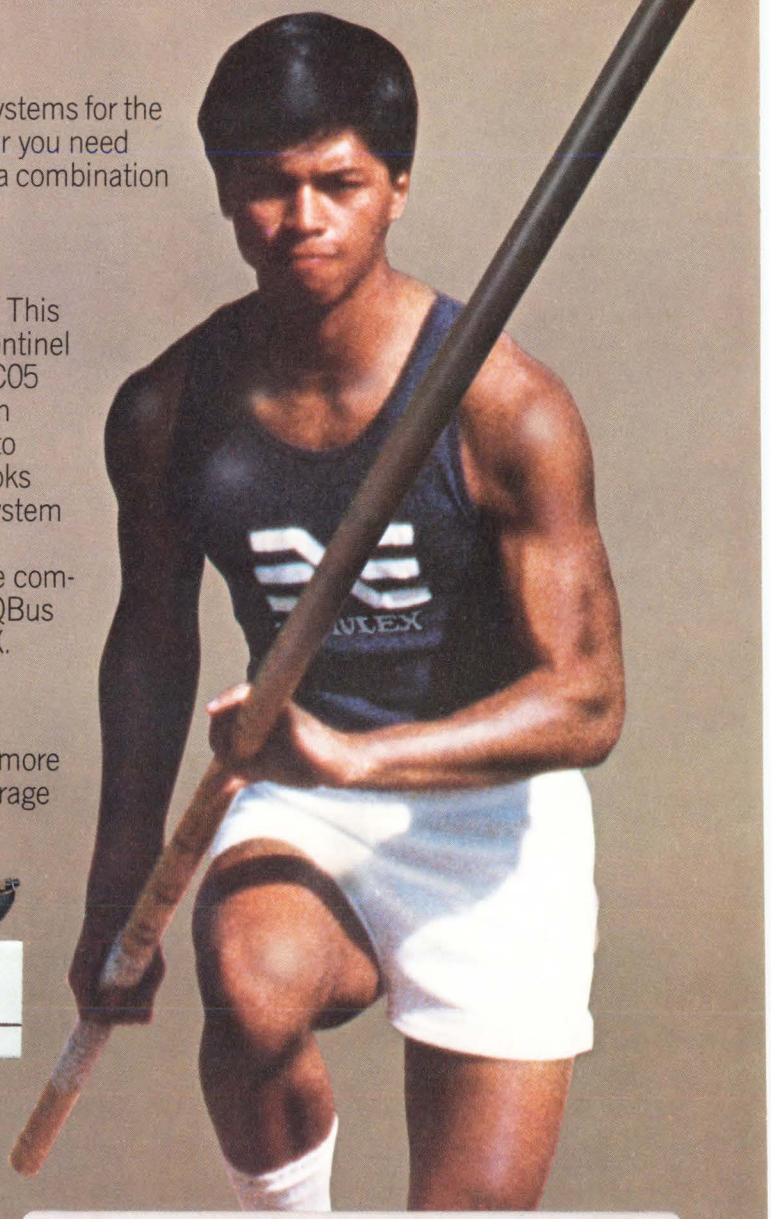
SABRE™ is a sharp solution for LSI users who need more storage and backup. It packs 31.2 MBytes of main storage onto a 5¼" Winchester and 10.4 MBytes of backup onto a removable 8" cartridge disk.

And since SABRE is an exact RL02 emulation, all existing operating and diagnostic software can be used as is.

SABRE is 5¼" high and slips into any 19" RETMA enclosure. A desktop version is also available. Both come complete with power supply, host adapter and connecting cables.

SABRE needs only one-eighth the space and one-quarter the power of four RL02s. And it eliminates the need for a separate system bootstrap, bus terminator and clock control board.



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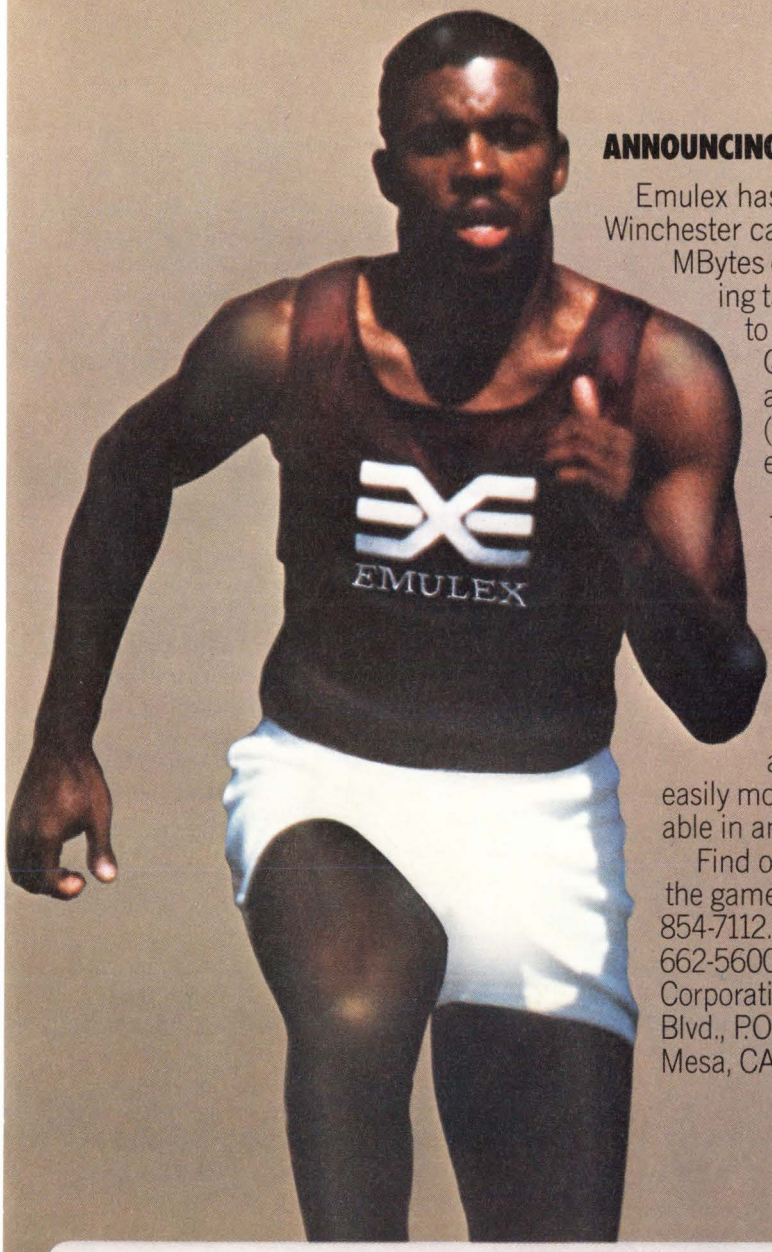
DEC DISK STORAGE LEAPS AND BOUNDS.



ANNOUNCING MEDLEY.™

Emulex has another winning combination with the Medley™ Winchester cartridge tape subsystem. It gives you either 35 or 110 MBytes of formatted storage and up to 70 MBytes of streaming tape backup. The Medley is fully software transparent to the operating system and diagnostic software of QBus and Unibus CPUs. And it uses the powerful and versatile Small Computer System Interface (SCSI) which keeps your options open for peripheral expansion.

Medley is interfaced to the system with a TC05/TC15 tape coupler and a UC02 (QBus) or UC12 (Unibus) host adapter. By using the Mass Storage Control Protocol (MSCP), the UC02 and UC12 allow the operating system to utilize the precise characteristics of the Winchester disk drive without patches or modifications to the operating system.

For convenience, Medley's disk drive, tape drive and power supply all fit into an attractive cabinet that easily mounts in a standard 19" rack. The Medley is also available in an attractive desktop version.

Find out how Emulex subsystems can keep you ahead of the game. Call toll-free (800) 854-7112. In California (714) 662-5600. Or write Emulex Corporation, 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626.

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CIRCLE 17

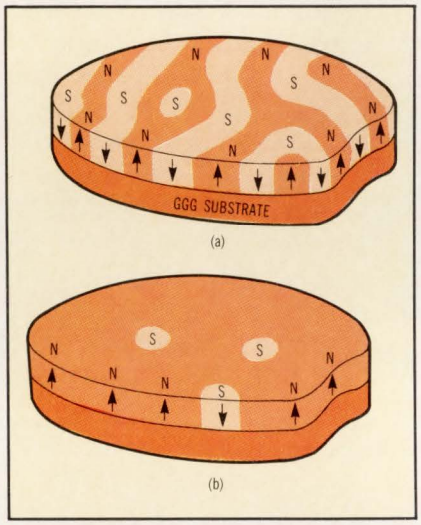
Magnetic bubble memories making a comeback

Bubble memories are demanded in more key computer equipment today than anyone could have predicted 20 years ago. For the most part, the type of equipment housing bubbles is designed for applications in harsh environments. Original predictions in the 1960s expected magnetic bubble memories to replace magnetic disks. Subsequent forecasts in the 1970s told of the bubble's demise as a nonvolatile memory alternative. Both claims have proved inaccurate in the reality of the 1980s.

Inherent advantages of magnetic bubble memory over other nonvolatile memories have held designers' interest. Now, 1-Mbit chips are readily available and 4-Mbit bubbles are slated for production in late 1985. In fact, experts expect bubble memory density to increase to 64 Mbits by 1988. Despite the fact that this potential capacity is provided in a much smaller package than movable disks can hope to occupy, only a handful of companies are active in magnetic bubble memory development. Only two American manufacturers (Motorola and Intel) and three foreign producers (Fujitsu, Hitachi, and Sagem) are offering bubble chips and the heavy support that these chips demand in both control circuitry and interfaces.

To be sure, bubble memories are not the simplest chips to produce. Invented by Andrew Bobeck at Bell Labs in the late 1960s, bubble memories have a history of support by several U.S. semiconductor companies. These have included Texas Instruments, National Semiconductor, Rockwell International, Bell Labs, Motorola, and Intel. Now, only Motorola and Intel remain in the running with the Japanese and the French. Even Bell Labs' Bobeck sadly admits that his research group no longer pursues development of magnetic bubble memories.

In 1966 Bobeck found that a magnetic thin film can store digital information by controlling the presence or absence of tiny magnetic domains in the film. These magnetic domains resemble bubbles, thus their name. They are formed perpendicular to the surface of a gadolinium gallium garnet substrate when a vertical magnetic field of appropriate intensity is applied. By changing the horizontal magnetic field, the bubbles can be moved within the film. The bubbles function as a memory when a one or zero is assigned to the presence or absence of a bubble at a given position in the thin film.



A magnetic garnet crystal grown on a gadolinium gallium garnet (GGG) substrate is used for the ferromagnetic film from which bubbles are formed. In the presence of a weak magnetic field, the magnetic domains form a serpentine pattern (a). When the field strength is increased, the domain becomes circular (b). By changing the horizontal magnetic field, the bubbles can be moved within the film.

Bubble memory technology has made great advances in bubble density and chip size. Plotting the capacity attained by bubble devices as a function of the year in which they were introduced suggests that capacity will quadruple every two or three years. The projection is based on success in developing and manufacturing of bubble memories that use ion- implanted contiguous disk technology.

With this technology, stress created by ion implantation induces an in-plane anisotropy in the surface layer of the garnet chip. Domain walls forming near pattern boundaries when the in-plane magnetic field is applied have poles that attract the bubble domains. When the in-plane field rotates, the charged walls circulate around the nonimplanted area, causing the bubble domains to propagate.

This technology using ions implanted on contiguous disks offers a gain of 4 to 16 times the density of currently manufactured permalloy asymmetric technology. Now under research, this technology will require changes in manufacturing techniques or chip architecture before the bubble memory devices can be produced. According to Mark Kryder of Carnegie-Mellon University (Pittsburgh, Pa), "The contiguous disk technology remains the most promising high density technology and will probably become dominant when the permalloy technology reaches its limits in producing bubble memory cells smaller than 4 to 6 μm."

For bubble memories to see widespread use, their price per bit must become less than that of other magnetic media. In the last four years, bubbles have become the least expensive solid state alterable nonvolatile memory. Today, however, mechanical mass storage devices still cost less per bit than bubbles. Mechanical devices will remain more cost effective, according to Mark Eisele, marketing manager at Intel Corp (Santa Clara, Calif). "Bubble memories will never be lower in cost per bit than floppies or Winchesters; and the garnet used by bubbles as a memory storage substrate will never cost less than the plastic substrates used in diskettes," he says.

Bubbles' access times, however, can compete head-on with those of mechanical disks. Motorola, for instance, has a 1-Mbit chip with an

(continued on page 32)

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CIRCLE 18

Magnetic bubble memories

(continued from page 30)

access time of 11.5 ms, better than many mechanical media having an equal amount of storage capacity. Access time of bubble memory devices depends on chip architecture, chip capacity, and the frequency of the drive or current used to access the data.

All current bubble memories use major-minor loop or block-replicate chip organization. In these organizations, data in parallel "minor loop" shift registers are accessed by another shift register (major loop or output path) that leads to a detector. The access time to the first bit in a block of data is roughly proportional to the number of bits in the minor loop. This, in turn, is proportional to the square root of the chip capacity.

To avoid an increase in access time while increasing chip capacity, manufacturers have put multiple detectors on a chip, and raised drive frequencies. Detectors occupy considerable space and require relatively expensive associated sense electronics. This places a limit on the number of detectors a chip can hold, according to Gus Hermann, marketing manager at Motorola.

As a result, manufacturers are offering full memory boards that contain all the necessary control, drive, and sense electronics, as well as subdividing memory capacities into 128-, 256-, 384-, and 512-Kbyte chunks. Motorola's 1-Mbit board and Fujitsu's Multibus-compatible circuit card are only two such examples. Fujitsu's FBC504M4M board, for instance (*Computer Design*, June 1, 1984, p 202), features a 12.5-ms access time and uses a single 5-V power source.

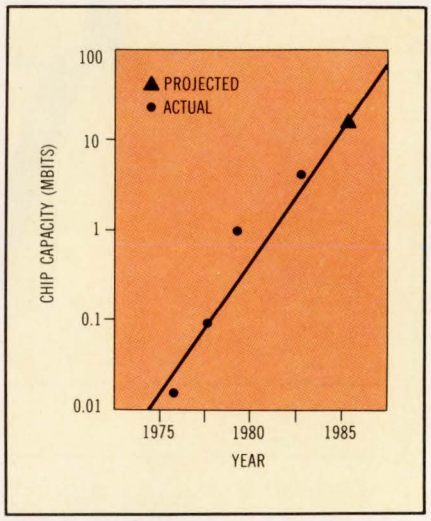
Intel has chosen a page size of 64 bytes, instead of the more commonly used 32 bytes, that uses fewer storage loops but more bits per loop. This ensures a higher reliability at the expense of a slower access time (40 ms). Intel's chip can operate over wider temperatures because its replicated bubble generator is less sensitive to temperature extremes and requires much less current than the nucleating generator used by other manufacturers. In addition, Intel's bubble memory chips become completely interchangeable at the component level with their support ICs.

According to Intel's Eisele, the bubble memory market has segmented into three temperature ranges, each suited to different applications. The most cost-effective bubble devices for commercial applications are rated for temperatures greater than 10 to 55 °C. In the 40 to 50 percent price premium are the industrial applications with bubbles operating at higher than the 0 to 70 °C range and military applications covering the full −20 to 85 °C range.

When introduced in the 1970s, bubbles were limited to switching systems and numerical control applications. Today, costs have gone down somewhat, and reliability has been enhanced. The mean-time between failures of bubble memory systems is now 1000 times better than that of the typical microfloppy disk drive. As a result of these improvements, bubble memories are now used in measuring instruments, medical equipment, building control and hotel systems, point-of-sale and banking terminals, as well as in automation equipment including personal computers, portable word processors, and facsimile machines.

This widespread demand has prompted manufacturers to include large capacity memories in their product lines. All producers are expected to sample 4-Mbit devices within the next year. Fujitsu is also aiming to develop 16-Mbit bubble memories in the future. The company claims these devices will be competitive with magnetic drum and disk units that have a storage capacity of up to 100 Mbytes.

One firm has already introduced a mass storage peripheral that uses a 1-Mbit bubble memory to replace floppy disk drives in computer systems specifically designed for high reliability applications and hostile environments. Hicomp Computer Corp of Redmond, Wash is offering 0.5 or 1 Mbyte of bubble memory in an enclosure the size of an 8-in. floppy disk drive (*Computer Design*, Oct 15, 1984, p 154). The MBM-1A can be interfaced to a computer system as either a floppy disk drive or as a block access peripheral.



The rate of progress of chip capacity for the years when bubble memories have been introduced can be extended to project that by 1988, a 64-Mbit magnetic bubble memory chip will be in production. By that time, the cost per bit for bubbles should settle at 3.5 cents per bit, as compared to 10 cents per bit today.

Using a Shugart-compatible floppy disk controller, the unit can operate as an alternative to either four 5¼- or four 8-in. drives. In the block access mode, individual blocks of memory can be accessed in 512-byte block segments. An internal switching power supply guarantees protection from line surges and data dropouts.

After many years of contradictory predictions, it remains to be seen whether offerings such as these are a prelude to a new breed of magnetic storage devices, on par with rotating disks. One thing, however, is certain—as the appetite for online storage increases, and as equipment becomes smaller in size, magnetic bubble memories can become another viable choice for computer systems.

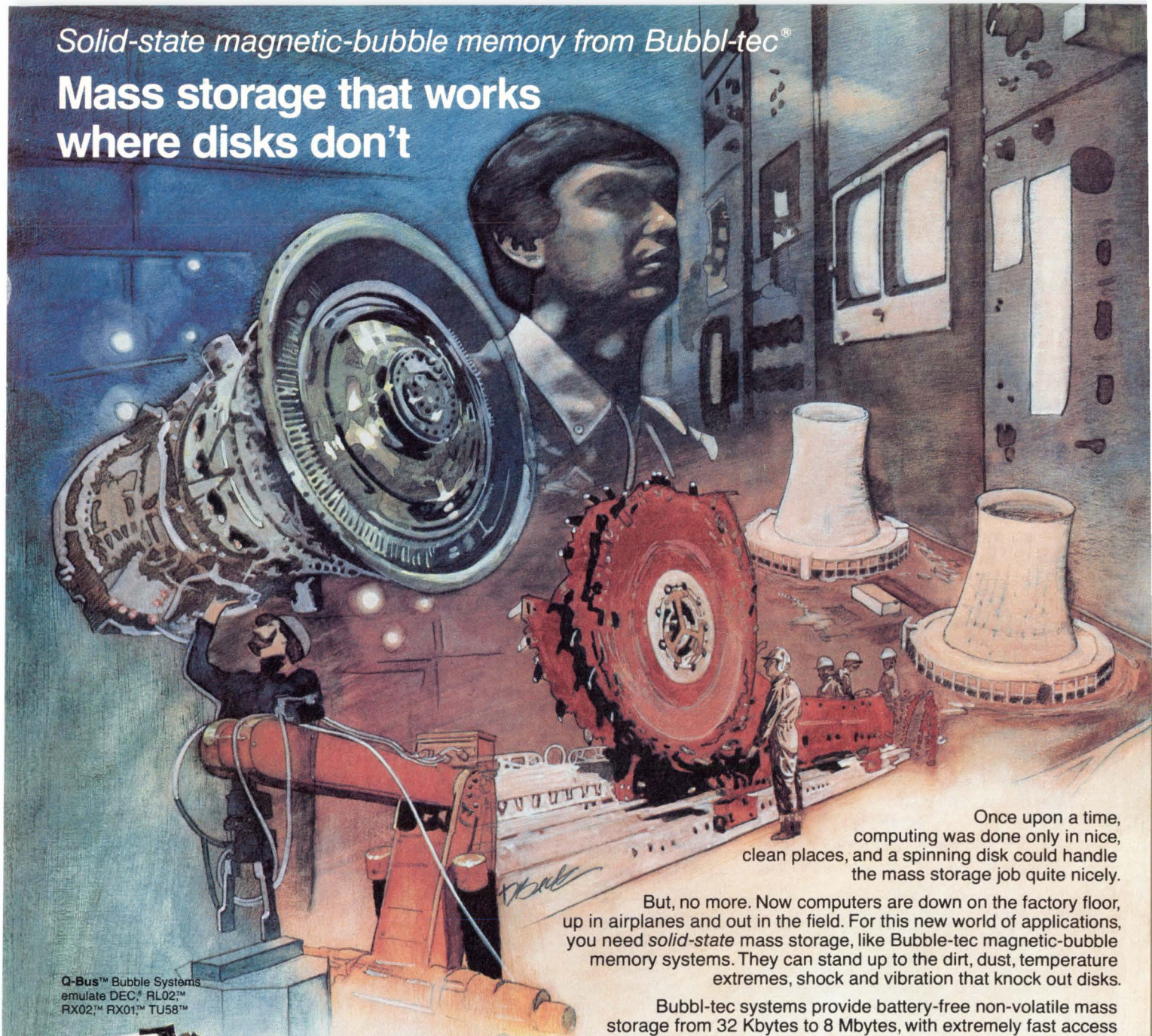
—Nicolas Mokhoff,
Senior Editor

SYSTEM TECHNOLOGY

(continued on page 34)

Solid-state magnetic-bubble memory from Bubbl-tec®

Mass storage that works where disks don't



Once upon a time, computing was done only in nice, clean places, and a spinning disk could handle the mass storage job quite nicely.

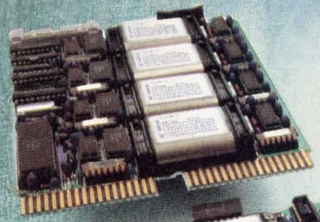
But, no more. Now computers are down on the factory floor, up in airplanes and out in the field. For this new world of applications, you need *solid-state* mass storage, like Bubble-tec magnetic-bubble memory systems. They can stand up to the dirt, dust, temperature extremes, shock and vibration that knock out disks.

Bubbl-tec systems provide battery-free non-volatile mass storage from 32 Kbytes to 8 Mbytes, with extremely fast access to every data block, And our systems plug directly into your microcomputer bus—no need for another chassis or power supply.

Since 1979, we've been shipping solid-state mass storage systems for every popular microcomputer bus, including Q, MULTI, STD, S-100, VERSA and VME. In fact we have more systems in the field than any other bubble-system supplier.

So, if you don't want to contend with disk deterioration, head crashes, and mechanical breakdowns, contact Bubbl-tec. Our mass storage solutions have a solid foundation.

Q-Bus™ Bubble Systems emulate DEC,® RL02,™ RX02,™ RX01,™ TU58™



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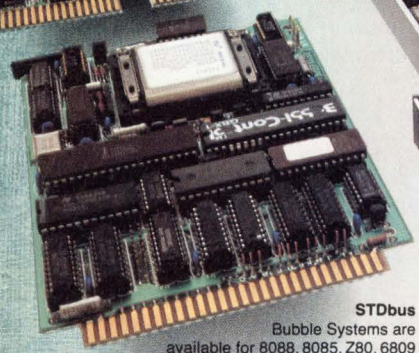

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CIRCLE 19

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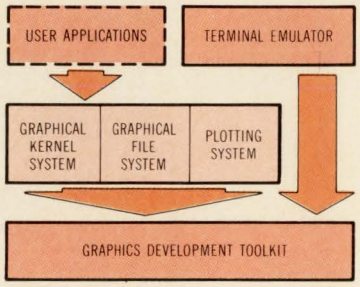
Graphics standards get boost from IBM announcement

After a long wait for the American National Standards Institute and the International Standards Organization to put their stamps of approval on graphics standards, the industry is going ahead with *de facto* standards on its own. The die was cast when IBM announced its PC Professional Graphics Series, thus throwing its weight behind three proposed standards: the Graphical Kernel System, the Virtual Device Interface, and the Virtual Device Metafile. The Professional Graphics Series is a software package from Graphic Software Systems (GSS) in Wilsonville, Ore.

IBM could hardly have picked a supplier with closer ties to the standards-making process. Several GSS executives are members of the ANSI X3H3 committee, which is evaluating the GKS, VDI, and VDM standards. The chairman of the committee, Peter R. Bono, is GSS' director of strategic technology. GSS President Tom Clarkson and Vice President Burt Perry are both voting members of the same committee. In working with GSS, IBM is virtually guaranteed that its products will be compatible with the standards ANSI approves.



IBM's PC Professional Graphics Series implements the proposed Graphical Kernel System standard as part of its own Graphical Kernel System. The Graphical File System implements the Virtual Device Metafile. The Graphics Development Toolkit provides a Virtual Device Interface.

"This is the first time in the graphics standards effort that a major supplier has endorsed the concept of standards," says GSS Marketing Director Mark Rawlins. And, Rawlins notes, the endorsement is a significant turnaround for IBM.

"They are supplying software that is completely nonproprietary. It is almost in the public domain. Anyone can write to ANSI, get a functional specification, and do the job themselves," he says.

Because the VDI standard provides a device-independent interface, the user can mix and match peripherals from different suppliers. Moreover, an application is not restricted to a particular operating system, such as MS-DOS. An application written for the IBM graphics package can run with any environment once the code is recompiled and linked.

Since the GKS and VDI were already well on their way to becoming *de facto* standards, IBM's announcement should not shock the industry. Rather, it will strengthen current trends. A standard competing with GKS—Core—is still being pushed by the Association for Computing Machinery, but ISO and ANSI have chosen GKS. A number of companies are working on implementations of GKS and VDI.

Status of Graphics Standards at ISO and ANSI

Standard	ISO Status	ANSI Status
2-D Graphical Kernel System (GKS)	Adopted June 1984. Final document to be published Nov 1984.	Public review completed. Final approval expected early 1985.
GKS Language Bindings: Fortran	Draft proposal to be circulated Fall 1984.	Part of GKS standard (above).
Pascal	Draft proposal to be circulated Fall 1984.	Public review in Winter 1984-85.
Ada	Draft proposal to be circulated Fall 1984.	Public review in Winter 1984-85.
C	Not an ISO standard language.	Working draft within X3H3. Public review possibly in 1985.
3-D GKS	Draft proposal by late Fall 1984. Circulate for comment within ISO.	Participating in drafting effort within ISO. Will comment on ISO draft when circulated.
Virtual Device Metafile*	Draft proposal circulated Summer 1984.	Public review completed. Second public review on changes only Winter 1984-85.
Virtual Device Interface**	New work item proposal to be voted on early 1985.	Working draft available. Public review in 1985.

*Known as Computer Graphics Metafile (CGM) in ISO.
**Known as Computer Graphics Interface (CGI) in ISO.

Layers of standards

Graphics standards represent a hierarchy, or set of software layers, somewhat analogous to ISO's seven-layer model for data communications (see "Graphics Standards Finally Start to Sort Themselves Out," *Computer Design*, May 1984, p 167). The GKS is a source-code portability standard concerned with programmer interface. The VDI is an object-code portability

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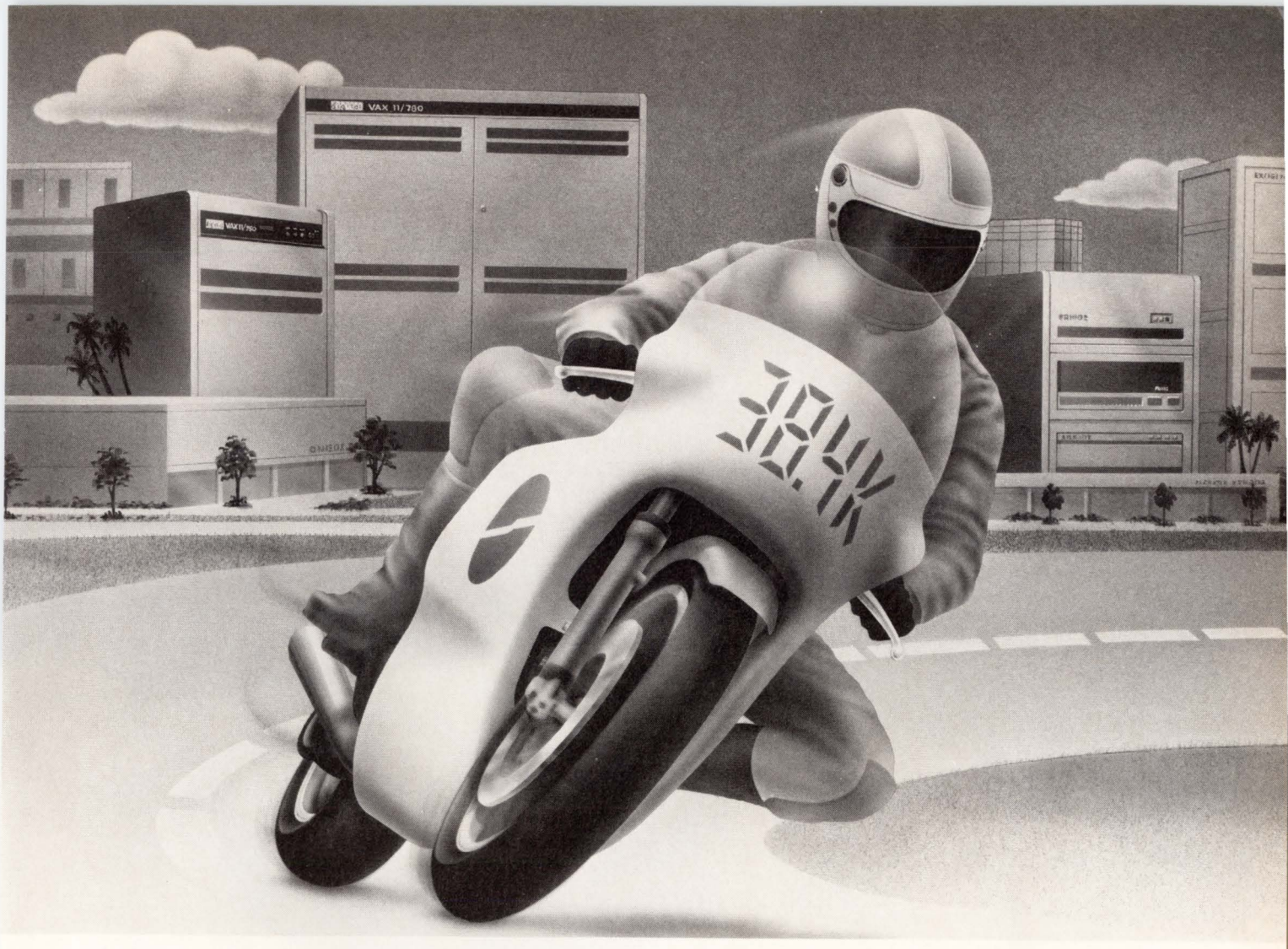

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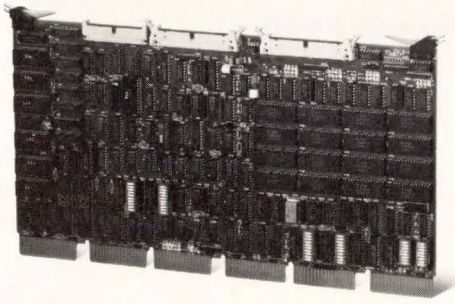

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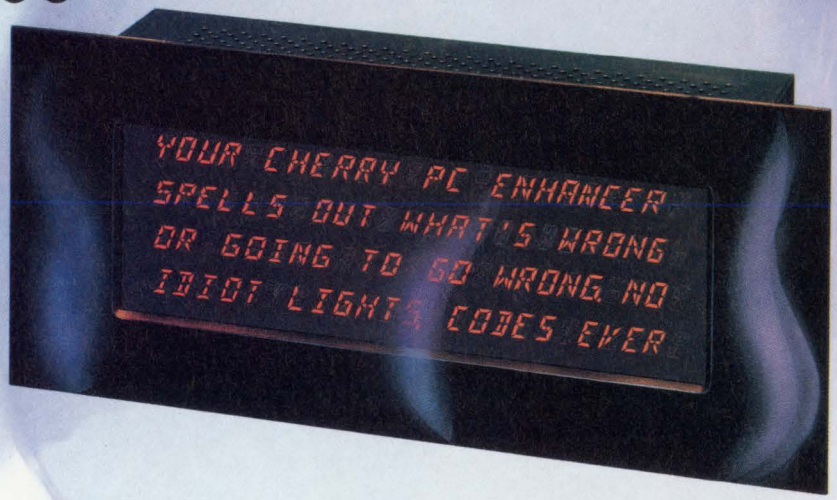

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Graphics standards
(continued from page 34)

standard that provides a device interface, while the VDM is a communications protocol standard being developed in conjunction with VDI.

The GKS (or Core) layer provides a standard interface to a defined set of graphics utilities and tools. In essence, it converts an application program carrying picture descriptions into a viewing package. At present, GKS has one limitation that Core does not—it is a two-dimensional standard. However, work on a three-dimensional standard is underway, and GSS expects to release a three-dimensional GKS when the standards become clearer.

Unlike Core, GKS provides bindings for programming languages such as Fortran, Pascal, Ada, and C. A number of these bindings are being reviewed by ISO and ANSI (see the Table). The IBM GKS package, called the Graphical Kernel System, has bindings to Fortran, Basic, and C.

VDI provides a uniform interface between high level graphics applications and I/O devices. Thus, it allows graphics applications software to be device independent. Application programs can ignore the limitations of physical devices, and graphics data can be displayed to the highest available quality for any device.

IBM implements VDI in a package called the Development Toolkit, which comes with a library of software routines that control IBM I/O devices. Even though the Development Toolkit only provides drivers for IBM peripherals, the user can write or purchase a device driver for some other device, and display graphics data on it. The GSS VDI package, GSS-Drivers, can now support about 40 devices from various manufacturers. GSS also expects to sell "off the shelf" drivers.

IBM's implementation of VDM is called the Graphical File System. Like VDM, it provides a standard for encoding and storing device-independent graphics or text data. It also allows graphics data to be transferred from one computer to another.

In addition to the GKS package, Development Toolkit, and Graphical File System, the PC Professional Graphics Series includes a plotting system and a terminal emulator. The plotting system allows programmers to develop data representation software. The terminal emulator provides emulation of a Tektronix model 40XX/41XX-type graphics terminal or a Lear-Siegler model ADM-3A alphanumeric terminal.

(continued on page 38)

Graphics standards

(continued from page 37)

Of all the graphics standards, the VDI could have the strongest impact on the marketplace. For now, IBM's endorsement of VDI means that third-party programmers will not have to worry about device-dependent code. That means software developers will be able to get their applications running quickly on IBM PC display environments.

Ultimately, VDI could alter the relationship between chip manufacturers, peripheral vendors, software developers, and microcomputer manufacturers. At the moment, these four groups are locked into a relationship that makes innovation difficult. Suppose, for example, that a chip manufacturer developed a fast, new architecture. The software developers would have to rewrite all existing graphics software. The peripheral manufacturers and the microcomputer manufacturers would have to prepare a whole new line of products for which software would probably not exist.

With VDI, however, a new architecture would not be so threatening. The software vendors will write code for the VDI—they will not have to rewrite each application for every device. Peripheral manufacturers will be assured that new devices will work with new and existing software. And, microcomputer manufacturers will have more freedom to innovate, because software and peripherals already in the marketplace should be compatible.

In general, standardization in the graphics industry should produce numerous benefits. Among these are software portability, ease of application program design, and the use of common interfaces that allow users to select products from different vendors. It appears that GKS, VDI, and VDM standards will be published sometime in 1985. Meanwhile, IBM's graphics package says that standardization will be the rule.

—Richard Goering,
Field Editor

Ada kit cuts compiler development time

As the Pentagon's mandate for Ada takes hold, a growing number of manufacturers are clamoring to get Ada on their machines—quickly. While vendors such as Harris Semiconductor, Rolm, Westinghouse, IBM, and Singer have Ada compilers up and running, other manufacturers seeking to join this select club face many man-years of effort if they write their own compilers. In addition, many manufacturers need cross compiler capability for a multitude of embedded systems.

A do-it-yourself adaption kit from Telesoft (San Diego, Calif) shortens development time and lets users port Telesoft's Ada compiler to their own systems. Billed as a new way of marketing compilers, the adaption kit requires the user to write a machine-dependent code generator on a VAX/VMS or Sun/Unix development host. The code generator is used to produce a cross compiler, which is then rehosted to a target system.

Telesoft's compiler is part of a trend toward the increasing use of multistage compilers (see "Multistage Compilers Move from Mainframes to Micros," *Computer Design*, June 1, 1984, p 45). Multistage compilers include a machine-independent front end that generates intermediate code, and a machine-dependent back end. The Telesoft compiler has a front end and middle pass. Its back end is a code generator that produces machine code object modules for each target computer. A small portion of the code generator is machine-independent, but most of it must be rewritten for each computer.

Telesoft's adaption kit consists of documentation support and software modules that are delivered sequentially. It allows the user to develop a fully operational compiler on a step-by-step basis. Users write and test a code generator, produce a cross compiler, and rehost it to a target system.

(continued on page 40)

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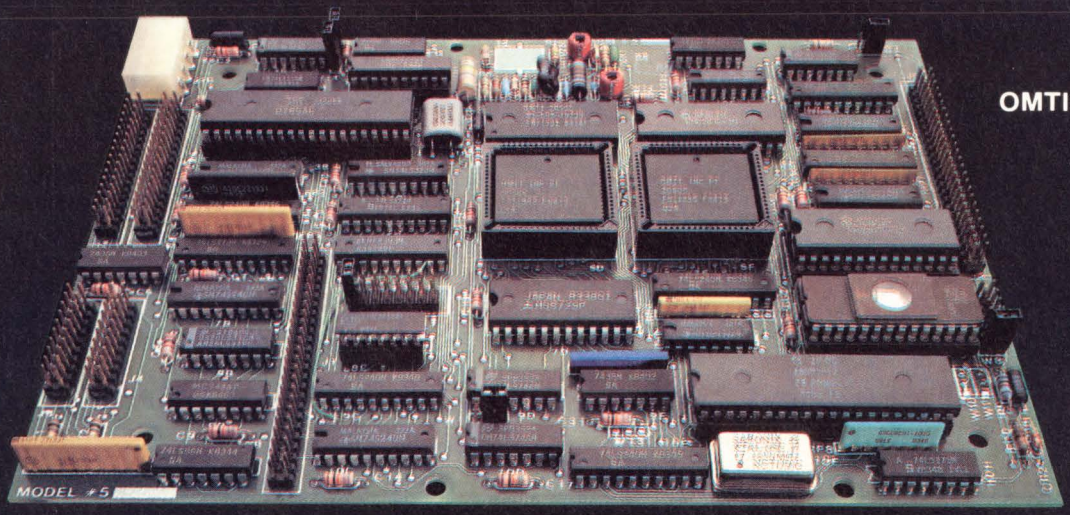

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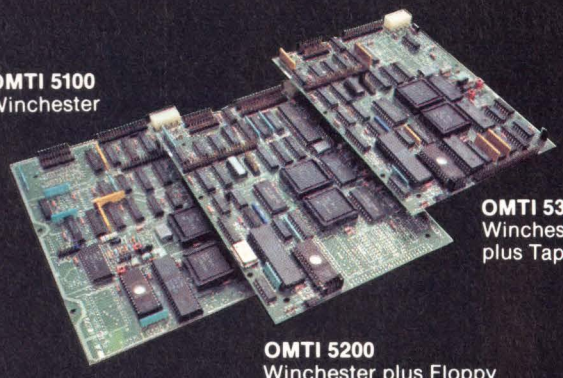

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CIRCLE 24

Ada adaption kit
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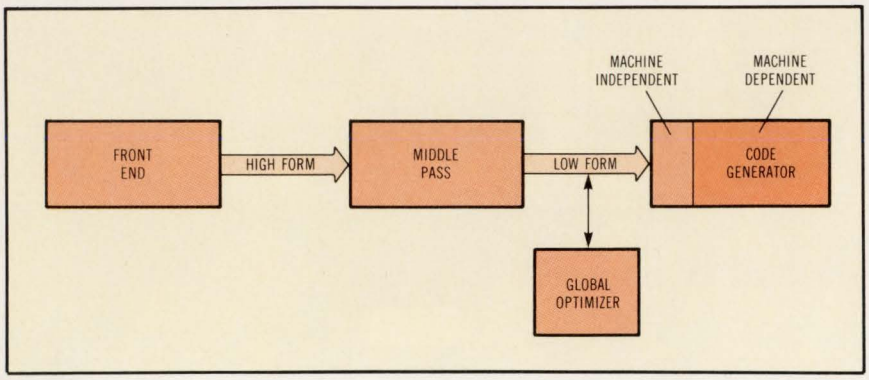

Telesoft's Ada compiler includes a machine-independent front end and middle pass. Most of the code generator is machine dependent. When sold as part of an adaption kit, the user will write the machine-dependent portion of the code generator on a development host. Telesoft estimates this effort can be completed in 6 to 12 man-months.

Telesoft delivers object code for the front end and middle pass. Although the middle pass is machine-independent, Telesoft recompiles it with parameters that describe the target system.

Source code is provided for the interface between the middle pass and the code generator, and for a Kernel Ada Programming Support Environment (KAPSE) interface. A code generator module provides the tools necessary to produce a machine-dependent code generator. When this is completed, the customer uses a retarget module to test the code generator and complete a cross compiler.

A rehost module produces a portable Ada compiler running on the customer's target system. The customer is responsible for validating the completed compiler. However, Telesoft will validate any changes resulting from its own updates to the front end or middle pass.

The adaption kit includes a KAPSE interface that allows Telesoft's compiler to conform to the characteristics of each host environment. Most of the interface is machine independent, but the user will generally have to provide a few hundred lines of code for each environment. This portability, however, requires some sacrifice in access to system services. If users start adding machine-dependent options, they will have to write code to support these options.

Multiple passes

The compiler's front end checks the source code, and builds a graph-like representation called high form. This representation is similar to DIANA, the Department of Defense-supported representation designed in the early Ada days, but is considerably more compact. The middle pass converts high form to another graph-like structure called low form. This representation is said to be more portable than the p-code previously used by Telesoft's Ada compiler.

If the user desires, low form can go through a global optimizer. It then goes through a low form interface to the code generator. The machine-independent portion of the code generator performs some minor optimization, and provides a graph traversal. The machine-dependent portion then generates output code for the target machine, with linking and relocation information.

When users write the machine-dependent portion of the code generator, they must resolve issues such as memory management, register modeling, exception handling, and task switching. For a highly optimized compiler, the user could write up to 40,000 lines of code. However, the company expects most customers to remain within a range of 5000 to 10,000 lines of code, and estimates that 6 to 12 man-months will be required to write a typical code generator.

The KAPSE interface allows the user to port the Ada Programming Support Environment (APSE), the compiler, and applications from one host to another. A portion of this interface is dedicated to system-dependent parts of system procedures, and is usually written in the same language as the host system. In the Unix implementation, for example, this package is about 300 lines of C code, and it makes the interface portable across different versions of Unix.

The adaption kit is currently available to OEMs and distributors. By the second quarter 1985, Telesoft will sell its own "off the shelf" code generators to end users. The company has reportedly signed up several major computer manufacturers for its adaption kit. Due to the growing demand for Ada, and the sheer complexity of the language, this approach may help set a trend in the way Ada compilers are marketed.

—Richard Gcering,
Field Editor

SYSTEM TECHNOLOGY
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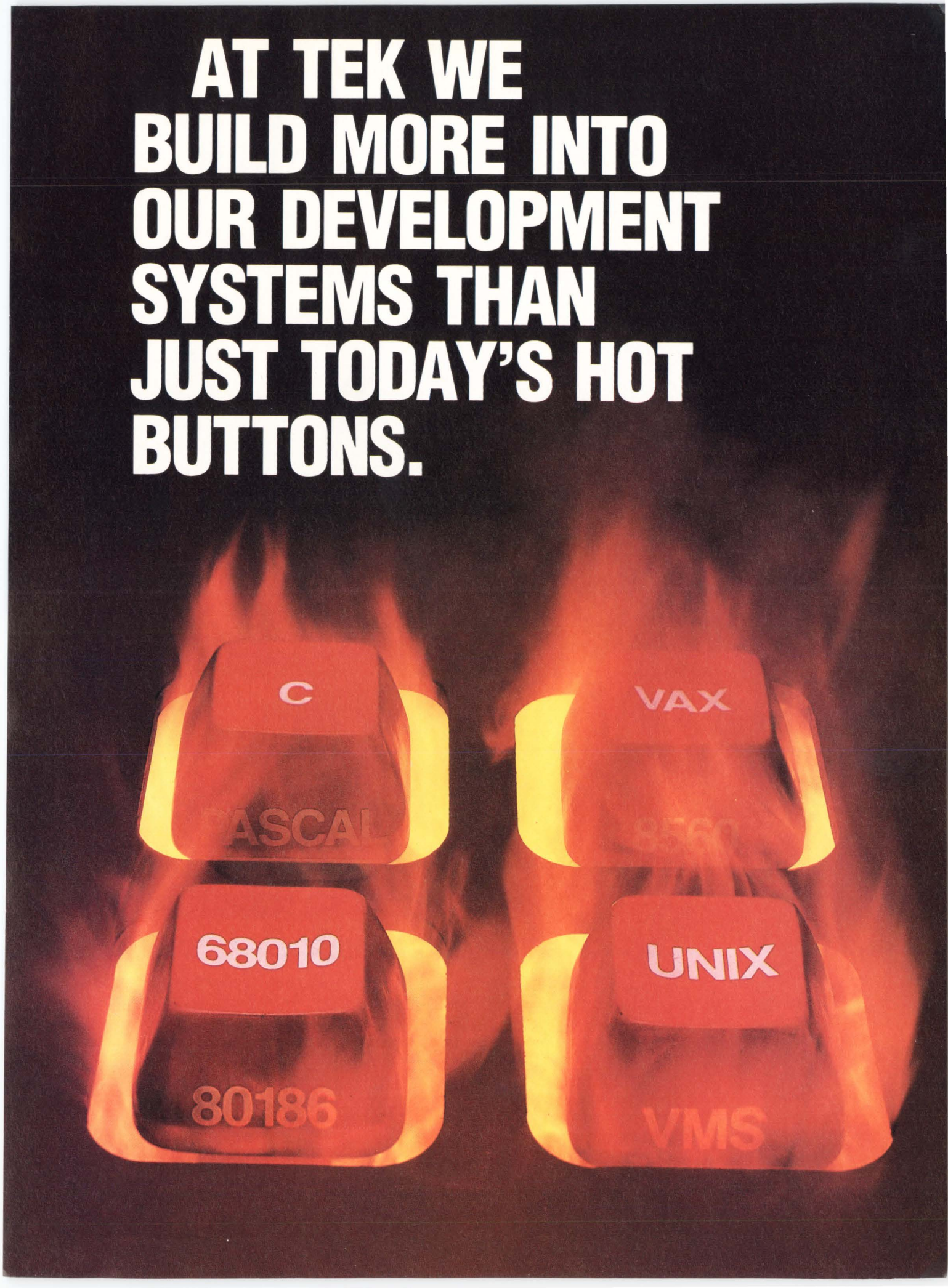

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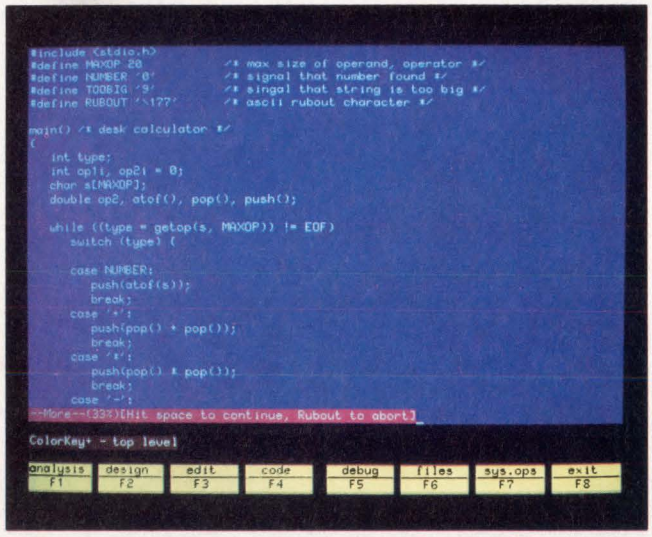

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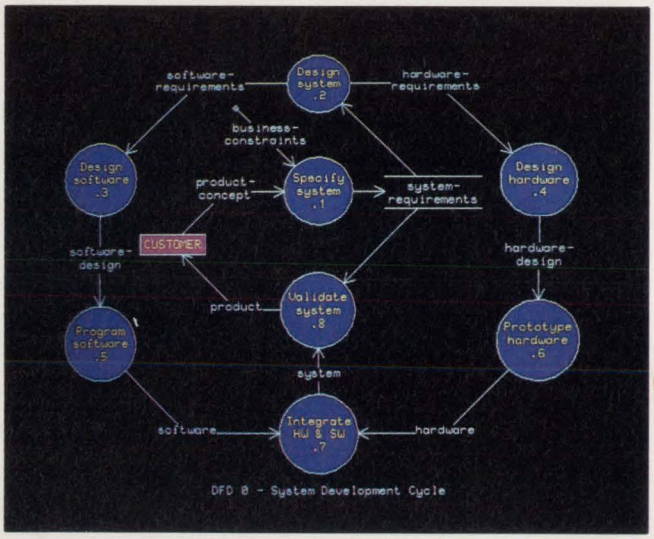

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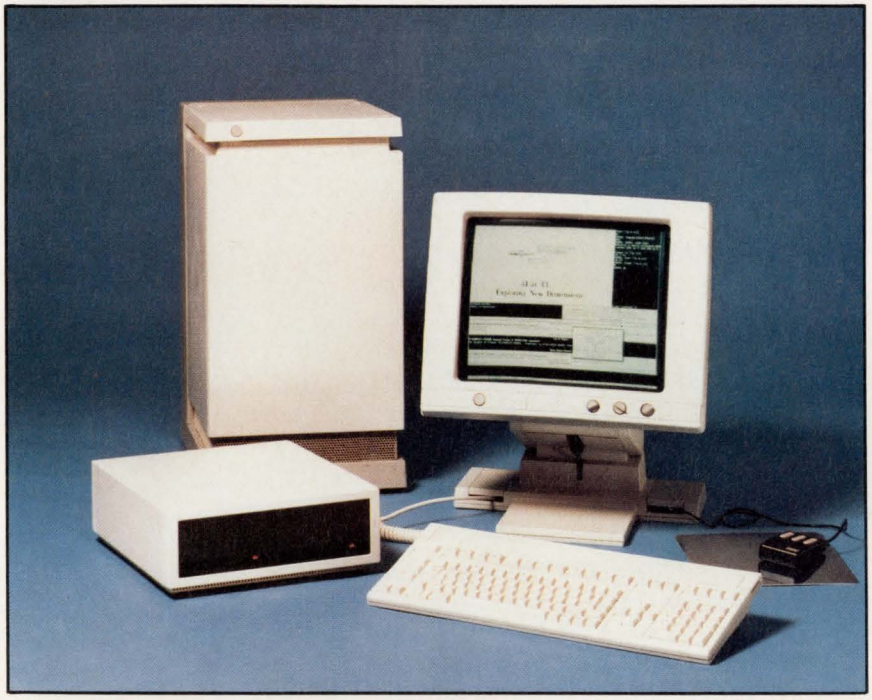

The smallest, dedicated symbolic processor presently available, TI's Explorer includes 5¼-in. Winchester disk drives, a high resolution monitor, and a keyboard that includes Lisp specific keys.

A recent entry among dedicated Lisp processors promises to open new symbolic processing applications. Smaller and less expensive than some of its competitors, Texas Instruments' Explorer is a single-user symbolic processing computer with hardware specifically designed for a Lisp environment. Despite the number of manufacturers offering Lisp on standard machines, the TI Explorer faces only two major competitors in the artificial intelligence market: the Symbolics 3600 family and the LISP Machines, Inc Lambda series.

But that competition is not what it first appears to be because Explorer is the result of a collaboration between LMI (Los Angeles, Calif) and TI (Austin, Tex). (LMI's Lambda series is built from TI's NuMachine with LMI's Lisp processor plugged into the NuBus.) Although it is smaller and less expensive than the Symbolics (Cambridge, Mass) and LMI machines, the Explorer is also less powerful. The machine includes a dedicated microprogrammed 32-bit Lisp processor, large virtual address space, 2 Mbytes of physical memory expandable to 16 Mbytes, high resolution graphics display, and 112 Mbytes of online mass storage. The TI machine also has 128 Mbytes of virtual memory space, a local high bandwidth processor memory bus, and a 32-bit NuBus system bus. The NuBus can support multiple processors, and is processor independent so that additional Lisp or conventional processors can be added. Bus transfer rate on this synchronous bus is 37.5 Mbytes/s.

The dedicated Lisp processor handles Lisp's flexible data structures more efficiently than conventional processors. It has 16-K x 56 bits of writable control store and a tagged architecture for typed data. Certain bits within each data word are used to tag and identify data types at run time. (The dynamic nature of symbolic processing prevents the operating system from identifying data types or the length and order of fields at compile time.)

The Explorer difference

Despite a common Massachusetts Institute of Technology heritage, there are substantial differences between the Lisp machines of LMI/TI and the industry leader, Symbolics. One of the most important differences is the tagged architecture. The Lambda/Explorer processors keep the tag bits within the 32-bit word. The Symbolics 3600 processor extends the word to 36 bits to append tags, allowing a larger address space and full 32-bit data. Thus, IEEE floating point can be used. According to Symbolics engineers, the Lambda design is too dependent on microcode to circumvent the machine's limitations.

The Symbolics approach accomplishes as much as possible in hardware. The 3600 family is stack-oriented with high speed buffering of the stack frames. Hardware assists in runtime checking for data type mismatches, uninitialized variables, and array bound errors.

Along with tagged architecture, Explorer and other dedicated Lisp processors require bit-field hardware (for manipulating complex data structures) and hardware-assisted garbage collection. In the cases of Explorer and Lambda, concurrent garbage collection is provided with four levels of volatility. This is needed because volatility varies according to the type of information. For example, program data is highly volatile; a compiler is not. Thus, time can be saved by performing the most frequent garbage collection on highly volatile data structures.

Given the large memory and disk capacity of systems currently available from Symbolics and LMI, it is questionable whether TI's new machine is destined for the same market niche. TI will sell the machine to LMI on an OEM basis, as well as sell it independently. Explorer will be the

(continued on page 47)

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Yeah, we could shout with the best of 'em.

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VERTEX

QUIETLY BUILDING THE BEST

Single-user symbolic processor
(continued from page 45)

seventh machine in the Lambda series, but will not compete with other Lambda machines.

According to LMI president, Frank Spitznogle, "LMI needed a high volume manufacturer to build low cost Lisp delivery vehicles." Given the cooperative relationship that already existed, he says, "TI was a natural choice." Spitznogle also notes, "TI has an equity position in LMI. Consequently, LMI licensed TI to build the architecture and software-compatible Explorer—with some limitations."

The agreement between the two companies provides LMI with a royalty for every machine that TI sells, and ensures that LMI will be able to purchase machines at the lowest price available to any customer, according to Spitznogle. "Furthermore, the agreement allows only low cost standalone machines with limited disk capacity," he says.

Restrictions apply

The maximum capacity 112-Mbyte disk size places the most severe restriction on Lisp performance. Both LMI and Symbolics use Zetalisp, a particularly rich dialect of Lisp that has absorbed many of the constructs of Xerox's Smalltalk and added numerous other improvements. A full Zetalisp implementation, however, takes approximately 4 million lines of code—considerably more than Explorer can handle. For the Explorer, TI chose Common Lisp, a subset of Zetalisp that is software-compatible with LMI's Lambda. Common Lisp only takes about 200,000 lines of code to implement.

LMI expects that most customers will opt for a full Zetalisp environment for program development. Thus, customers will develop expert systems or other AI-based products on the larger Lambda systems, but will use the Explorer to run such applications in the office or the lab. LMI hopes that this will result in greater sales of larger Lambda systems for development work, as well as high volume Explorer business for both companies.

TI, however, expects that many users will develop applications on the Explorer itself and offers numerous Lisp program development tools to make it easier. A realtime window-oriented display editor, a Lisp listener for user interaction with the Lisp interpreter, a Lisp compiler, an inspector, and a command interface toolkit are a few of the tools available. Along with these, TI has included facilities for debugging, system definition and patch, and performance monitoring. Optional software includes a text formatter and toolkits for graphics, natural language interface, a relational table manager, and Prolog development. The Prolog toolkit includes an interpreter and software to help build expert systems. Another utility helps the user describe knowledge that can be represented as a semantic network.

Symbolics questions the need for a machine like the Explorer since it is the company's experience that users require more—not less—capability in their Lisp processors. Symbolics considers Explorer to be a mid-range machine in price, but a low-end machine in performance, and questions the market niche that TI and LMI are staking out.

This may prove to be a theological argument among Lisp gurus. But even if those who doubt TI prove right, it will only be a few years before higher performance and lower prices are available. TI has announced a $6 million, 27-month, Defense Advanced Research Projects Agency (DARPA) contract to develop a custom Lisp processor chip. Based on 1.25-micron CMOS technology, the Lisp microprocessor will operate at speeds up to 40 MHz and will eliminate several hundred ICs. Although the chip will be designed for military systems, it will open up many new commercial applications for symbolic processing.

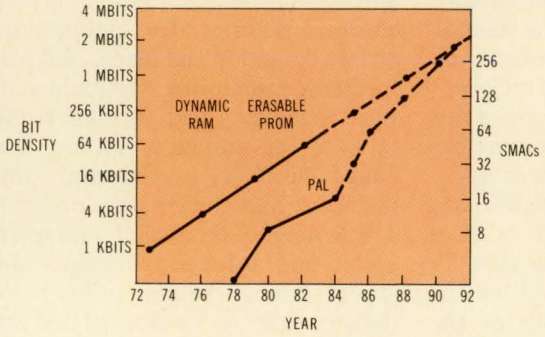
—John Bond,
Senior Editor

SYSTEM TECHNOLOGY
(continued on page 48)

Dense programmable logic takes aim at semicustom devices

Programmable logic devices, long considered compact "glue" for reducing package count in systems, may be gaining the density needed to take over logic functions formerly the domain of gate arrays and semicustom chips. The introduction of a 5000-gate PLD may presage the time when the designer will be able to program logic functions using design software and then produce a prototype part instantly.

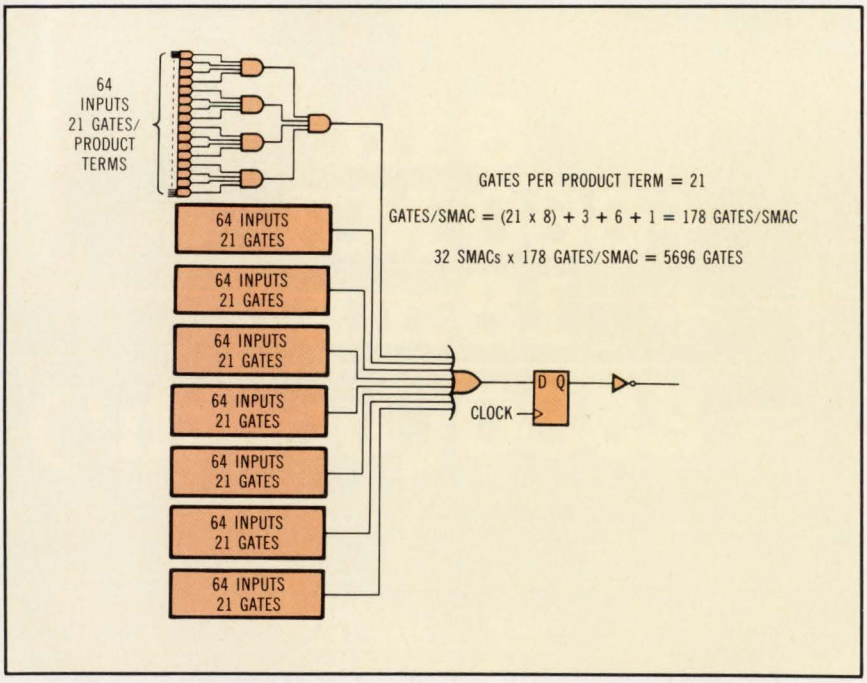
Such a development, being introduced by Monolithic Memories (Santa Clara, Calif) will certainly not replace gate arrays and semicustom ICs. But, it will give the system designer a further choice when considering time-to-market and hardware prototyping. The company's PAL64R32, called the MegaPAL, provides 32 input lines and 32 programmable output lines that can be programmed with 32,000 fusible links. The MegaPAL also incorporates product term sharing. This allows more flexibility in defining output expressions because the designer can vary the number of product terms per expression.



Analysis of programmable logic density versus memory shows that bit densities should converge around 2 Mbits. At that time, a 16-bit multiprocessing unit could be produced on a programmable logic device.

Where a product term is any combination of input variables or their complements ANDed together, product term sharing allows the programmer to modify these terms via OR gate inputs. To give a clearer picture of the logic capacity of a PLD, Monolithic Memories has coined the term state machine atomic cell (SMAC).

The SMAC is a 1-bit state machine using a D-type flipflop to feed back into an array of four-input NAND gates. The MegaPAL uses 64 inputs per product term. Since it uses four-input gates, this requires a total of 21 gates to reduce 64 inputs to a single product term. Since each SMAC has 8 product terms, this number (21 x 8 = 168) plus the OR gates and the gates in the flipflop comes to 178 gates per SMAC. Thus, the 32 SMAC part has the equivalent of 5696 gates, which is a useful figure when comparing programmable logic to gate array logic.



The state machine atomic cell (SMAC) incorporates 21 gates for each of 8 product terms. The flexibility is furthered by the ability to share product terms via the OR function. The PAL64R32, for example, has the equivalent of 5696 gates.

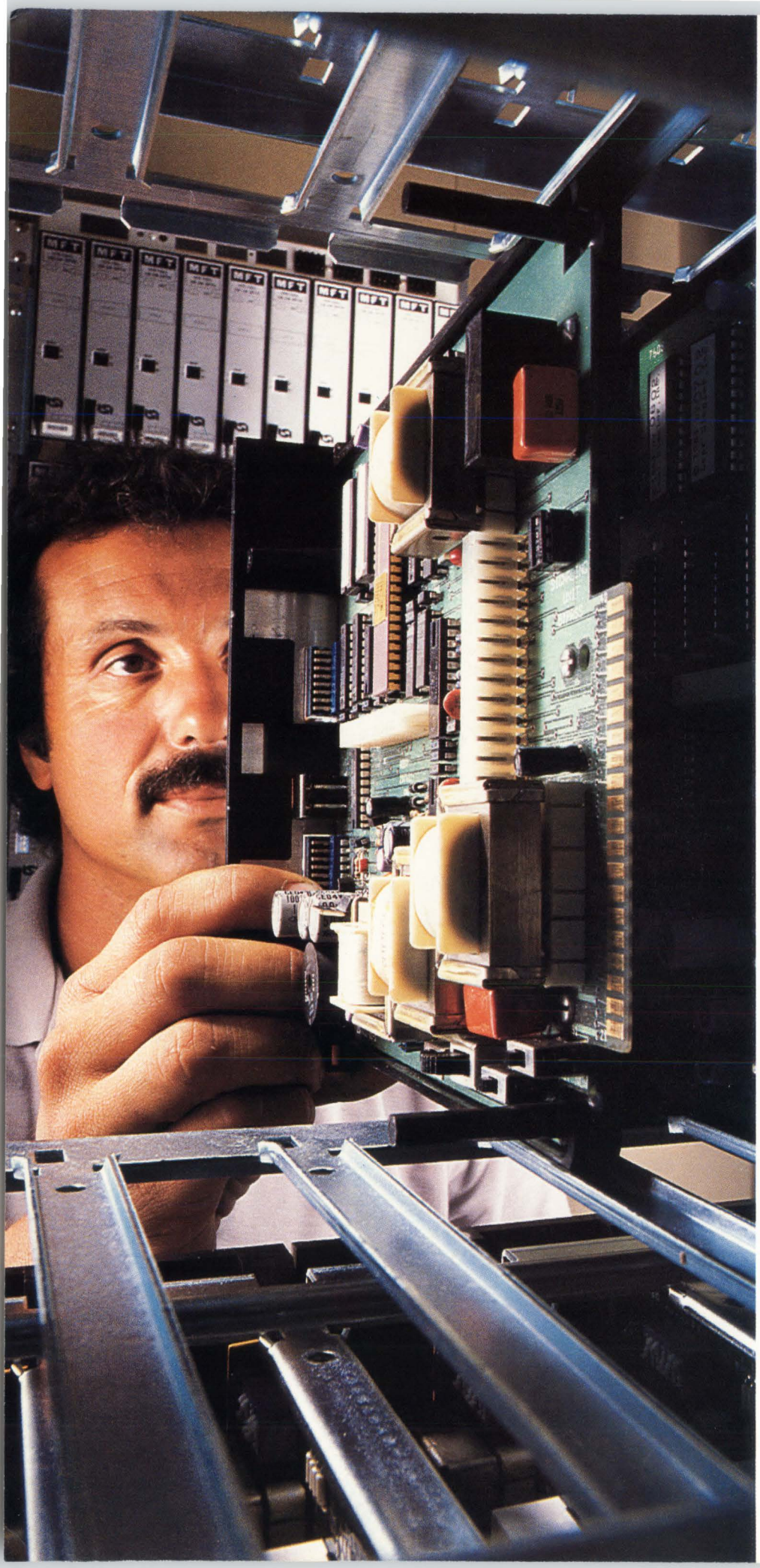
Increased PLD recognition

In comparing raw bit density, the PLD's number of fusible links serve as a yardstick. The company has cited a corollary to the famous Moore's Law, which states that memory density increases by a factor of four every two to three years. It is that logic density that doubles every two to three years. When compared to dynamic RAM and erasable PROM density, it is clear that PLDs are gaining, and that the point has already been passed where they are merely a convenient glue for solving interfacing problems in limited space.

(continued on page 53)

Texas Instruments digital signal processor helps Lear Siegler Inc. make your message loud and clear...from anywhere.

- **TI's single-chip, high-performance TMS32010** digital signal processor (DSP) assures highest quality telephone transmission *(Page 2)*.
- **TMS320 DSPs from TI** support high-speed and numeric-intensive applications from communications to seismic processing *(Page 3)*.
- **Complete development support** for TI digital signal processors includes hardware, software, documentation, and application workshops *(Page 4)*. ▶



TI digital distortion

When you're depending on the telephone to get your message through, you don't need "singing" on the line. A standard two-wire circuit "sings" when signals traveling in opposite directions are insufficiently isolated in a repeater. To eliminate this problem, Lear Siegler, Inc., manufacturer of repeaters used worldwide, relies on the Texas Instruments TMS32010 digital signal processor (DSP). And cuts setup time for each repeater from hours to minutes.

In the unique VFR-7608 repeater, TI's TMS32010 performs all the functions of analog equalizers, filters, and amplifiers (see diagram opposite). It compensates automatically for line impedance 8,000 times per second. Completely isolates the opposing signal streams. Puts an end to "singing."

TMS32010 eliminates reflections "by the numbers"

The standard solution to "singing" is an analog network designed to cancel out reflected signals on the line. But even with expensive "precision" hybrids, the best solution is a compromise that limits usable bandwidth and gain.

Digital signal processing with the TMS32010 balances the circuit across the entire frequency band every 125 μs. Because the repeater adapts continuously, the circuit *cannot* "sing" at any frequency, and its gain can be fully utilized.

DSP cuts setup time to minutes

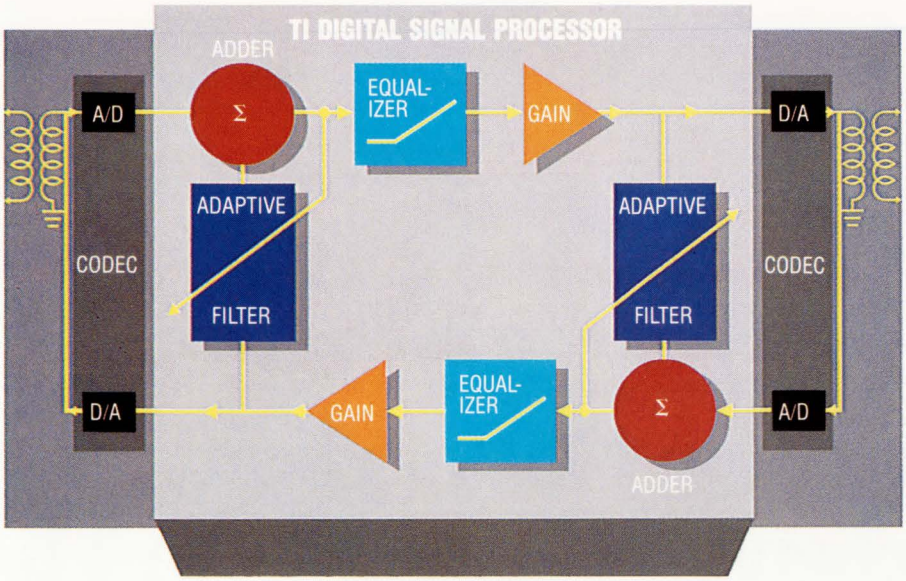
Tuning each analog repeater is an hours-long, trial-and-error procedure for a highly skilled technician. Using a comprehensive history of each circuit, he must set 68 switches in an analog repeater. TI's TMS32010 in Lear Siegler's new digital repeater eliminates 65 of those switches. Ends the need to keep detailed circuit histories. And the small, affordable plug-in unit is interchangeable with older repeaters.

So your message can always come through—loud and clear.

◀ **Setup is as simple as 1-2-3** with Lear Siegler's adaptive telephone repeater using TI's TMS32010 DSP. Whereas manual adjustment of an analog repeater can take many hours, only three simple switch settings are required to assure rock-stable, "sing"-free performance from the digital repeater.

27-4973

signal processor squelches in unique adaptive repeater.



Heart of the adaptive repeater is TI's single-chip, 16/32-bit TMS32010 digital signal processor. All the functions shown are achieved in real time through software operating on signals digitized by conventional single-chip codecs.

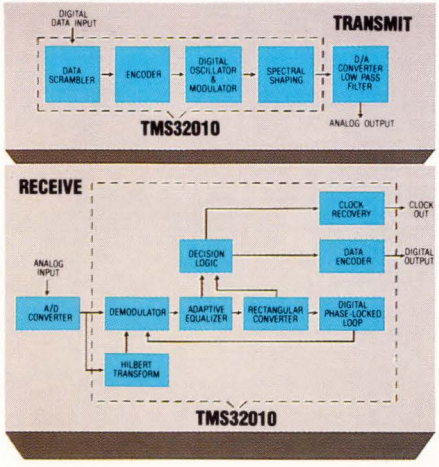
The TMS320 family from Texas Instruments: "Workhorse of digital signal processing."

The TMS32010, first member of the TMS320 DSP family, is TI's trailblazing contribution to an important new technology. A Lear Siegler engineer who has been following the progress of digital signal processing from its inception says, "The TMS32010 is the first device that can reliably do what we need. It's a real workhorse: The '8080' of DSP."

TI's TMS320 DSPs excel at high-speed, numeric-intensive applications

High-performance TMS320-family DSPs from Texas Instruments will find widespread use in many fields where large volumes of high-speed computation are required. In telecommunications, they can also be used to build high-speed modems with data-transmission rates up to 9,600 baud. They can make speech recognition, analysis, and synthesis practical. Speed image processing and pattern recognition. Facilitate high-speed process control and instrumentation. Process radar, sonar, and seismic signals. And furnish the multiple functions often required for a single application.

For example, a TMS320 DSP could enable an industrial robot to synthesize and recognize speech, sense objects and their orientation, and perform mechanical operations through digital servo-loop computations.



High-speed modem functions are effectively performed by TI's TMS32010, as well as such expanded functions as auto-dial/answer, dial-tone verification, busy-signal detection, and self-test routines.

The TMS320 family, with its extensive development support *(see page 4)*, can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, fast Fourier transforms—performing a 64-complex-point FFT in only 550 µs. And for seismic processing involving very low frequencies which only a digital system can implement.

Image enhancement, pattern recognition, and data compression are all possible with TMS320 processors. They can extract features and perform template comparisons for optical character recognition.

A one-chip alternative to bit-slice processing

TI's 16/32-bit TMS320 DSPs offer an inexpensive alternative to multichip bit-slice processors. They combine the flexibility of a high-speed controller with the numerical capability of an array processor—on a single chip, in one 40-pin DIP.

Highly pipelined architecture and a comprehensive instruction set give the TMS320 the speed to execute five million instructions per second with 32-bit precision: More than fast enough, for example, to handle the 40 additions and 40 multiplications necessary for realtime voice-frequency processing within the 125-µs sampling interval. A conventional microprocessor, operating at 8 MHz, would require 900 µs, and quickly become bogged down in the signal stream.

Now in three versions

The TMS32010 microprocessor has 288 bytes of on-chip data RAM, and can address up to 8K bytes of off-chip memory at full speed.

The TMS320M10 microcomputer is identical to the TMS32010, but it also includes 3K bytes of on-chip mask-programmed ROM.

The military version, SMJ32010JDS, is processed to the extended temperature range requirements of MIL-STD-883B.

To learn more about the many applications and available development support for TMS320-family DSPs, return the coupon on the following page.

See back page for more information.

In-depth support for the TMS320 family of TI DSPs includes a host-independent development system, an evaluation module, emulator and analog interface board, as well as assembler/linkers and simulators that can run on a variety of host computers and PCs. Documentation is extensive and thorough.

Develop your own DSP applications with comprehensive support from TI.

Texas Instruments has assembled an extensive group of development-support packages for the TMS320 family of VLSI digital signal processors *(see table)*. Included are all the hardware, software, and documentation you need to utilize the power and speed of TMS320 DSPs in your designs. A rapidly growing volume of third-party support is also available.

Use your own PC as a TMS320 development station

The latest addition to TI's development-support software is the TMS32010 Digital Filter Design Package developed by Atlanta Signal Processors Inc. It makes your Texas Instruments Professional Computer or IBM PC a cost-effective, easy-to-use, digital-filter design station. With it you can produce the TMS32010 source module. Then you can assemble the code and simulate it in software on the PC. Later you can download the code into the hardware-development system for realtime emulation.

Two versions are now available: **DFDP-TI001** for the Texas Instruments Professional Computer, and **DFDP-IBM001** for the IBM PC.

TMS32010 Software and Hardware Support

Host Computer	Operating System	Part Number
Macro Assembler/Linkers		
TI990	DX10	TMDS3240120-08
DEC VAX	VMS	TMDS3240210-08
DEC VAX	Berkeley UNIX 4.1	TMDS3240220-08
DEC VAX	Berkeley UNIX 4.2	TMDS3240230-08
IBM	MVS	TMDS3240310-08
IBM	CMS	TMDS3240320-08
TI/IBM PC	MS-DOS	TMDS3240810-02
Simulators		
DEC VAX	VMS	TMDS3240211-08
TI/IBM PC	MS-DOS	TMDS3240811-02
Hardware		
Evaluation Module (EVM)		RTC/EVM320A-03
Analog Interface Board (AIB)		RTC/EVM320B-06
Emulator		TMDS3262210

Learn in TI workshops

Texas Instruments supplies comprehensive documentation with each device. A growing library of application reports will also assist you in the design of digital signal processing circuits using TI's TMS320 DSPs.

Three-day DSP workshops, including extensive hands-on experience, are conducted periodically at Texas Instruments Regional Technology Centers. For registration information, call the Regional Technology Center nearest you: Atlanta, (404) 452-4686; Boston, (617) 890-4271; Chicago, (312) 228-6008; Dallas, (214) 680-5096; Northern California, (408) 980-0305; Southern California, (714) 660-8164.

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Please send me information about:

PR 22 ☐ TI's TMS320 family of Digital Signal Processors.
PR 24 ☐ Third-party support for the TMS320 family.

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Dense programmable logic

(continued from page 48)

Monolithic Memories claims that the MegaPAL can be used to implement a 4-bit microprocessor and that a PAL that had 256 SMACs could easily accommodate the logic to emulate a 16-bit 68000 microprocessor. Logic density of this magnitude could very well alter some common assumptions about the design process.

The advantages of PLDs lie in the fact that the actual physical device used in the system or prototype can be produced on the spot. The current wisdom of CAE is to produce perfect software models of an IC before fabricating any silicon. While that approach certainly has many advantages, there is a place—especially in specialized parts that are required in relatively small numbers—where the programmable logic approach would make more economic sense. Monolithic Memories is advocating a product life cycle approach that would use the PAL as a prototyping device to be replaced in the production versions of the product by the hard array logic (HAL). HALs are functionally identical but somewhat less expensive than PALs because they can be made somewhat smaller. The company will also support migration to derivative semicustom devices for those cases where production volume makes that economically attractive.

The obvious question raised by this jump in logic density is that of the software needed to conveniently program such devices. Ideally, the same kind of design interface used in CAE for designing gate arrays and semicustom devices could be used to implement logic functions on PLDs.

Of the major CAE vendors, only Daisy Systems (Sunnyvale, Calif) appears to have a state machine definition package for use in programming PLDs. Called the Hardware Compiler, the package allows the user to define a finite state machine in terms of an "algorithmic state machine"—a flowchart. This state machine definition can then be translated into the code needed to blow the proper fuses in various PLDs.

Monolithic Memories has recently introduced a new version of its software package, PALASM, which is an assembler used specifically for defining programmable logic. To answer the demands of the increased logic density, PALASM2 has a syntax that allows indexed equations and string substitutions for defining logic equations. PALASM2 has also been expanded to be able to handle system level descriptions for cases where several devices are needed to implement some overall logic function.

Higher level tools

Some programming tools that use higher level concepts are available from independent sources, notably from Assisted Technology (San Jose, Calif) and Data I/O (Redmond, Wash). Both of these companies have approached PLDs with the view of giving the programmer higher level tools that can be run on personal computers, and both are in the process of adapting their products to serve the MegaPAL and its succeeding generations.

One tool, CUPL, from Assisted Technology allows the designer to define and group pins, and give them names so that equations can be written in terms of pin names. CUPL further allows the naming of internal nodes. The newest release of the ABEL package from Data I/O uses a state machine syntax to generate the actual equations. This allows the user to group pins for a given state machine and define a table of cases and states. As yet, no one has made any announcements, but it is safe to assume that companies with experience in higher level definition software for PLDs are actively pursuing the major CAE companies to achieve a smooth incorporation of these devices in the total logic design process.

Also coming in PAL are CMOS parts. Monolithic Memories has an agreement with Cypress Semiconductor (San Jose, Calif) to develop a PLD using 1.3-micron technology. Also, erasable PLDs can be expected to appear within the next year or so. With the logic densities that are now possible, this would lead to some interesting possibilities.

For one thing, spare parts inventories could be reduced for a variety of logic parts. This would mean keeping a supply of unprogrammed PLDs on hand and the data needed to program for the various functions. Replacing a part would be a matter of blowing the proper fuses. In addition, erasable PLDs open the door to dynamically alterable logic functions. And, CMOS clears the path to an already vast area of portable equipment.

—Tom Williams,
West Coast Managing Editor

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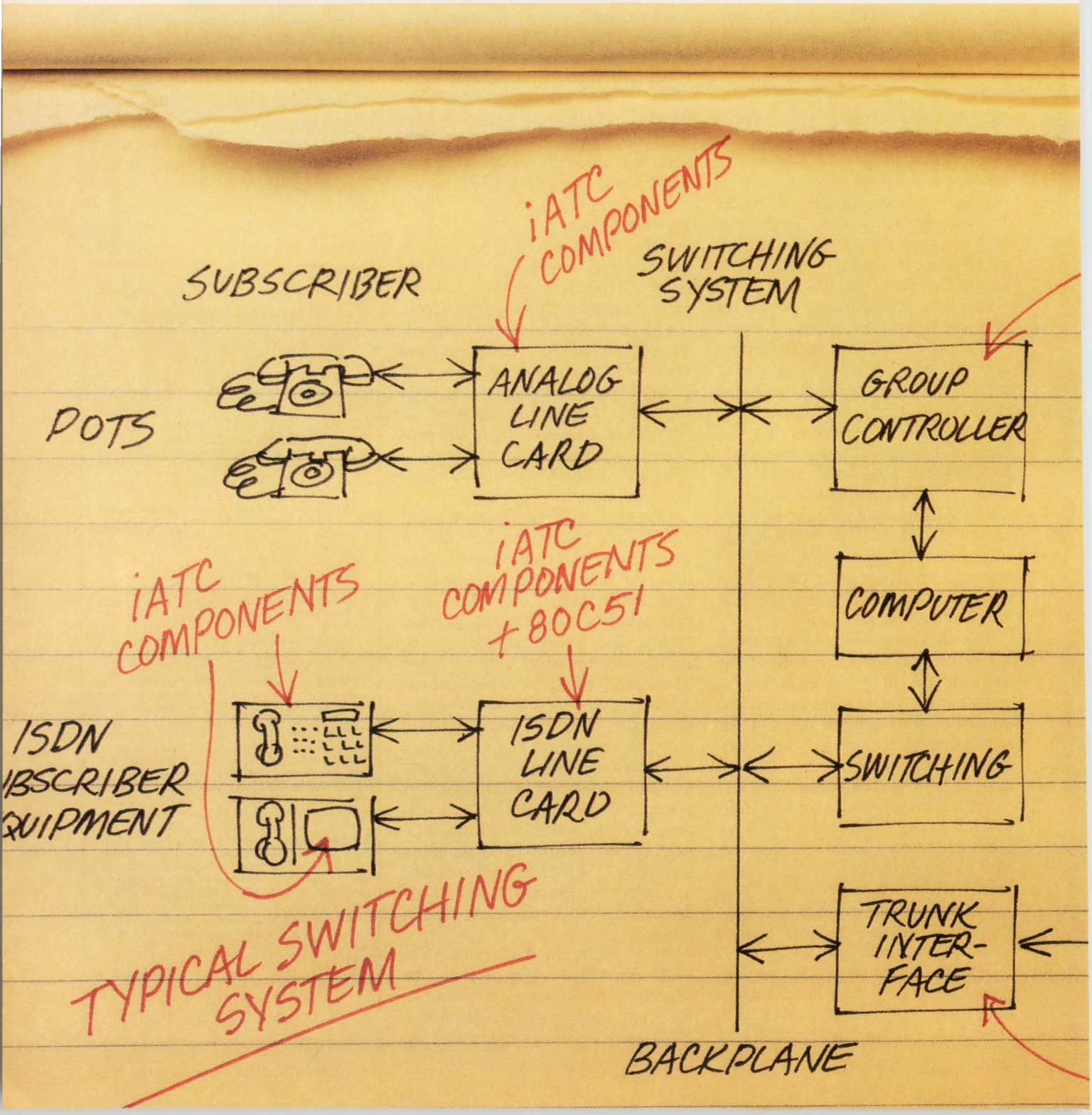

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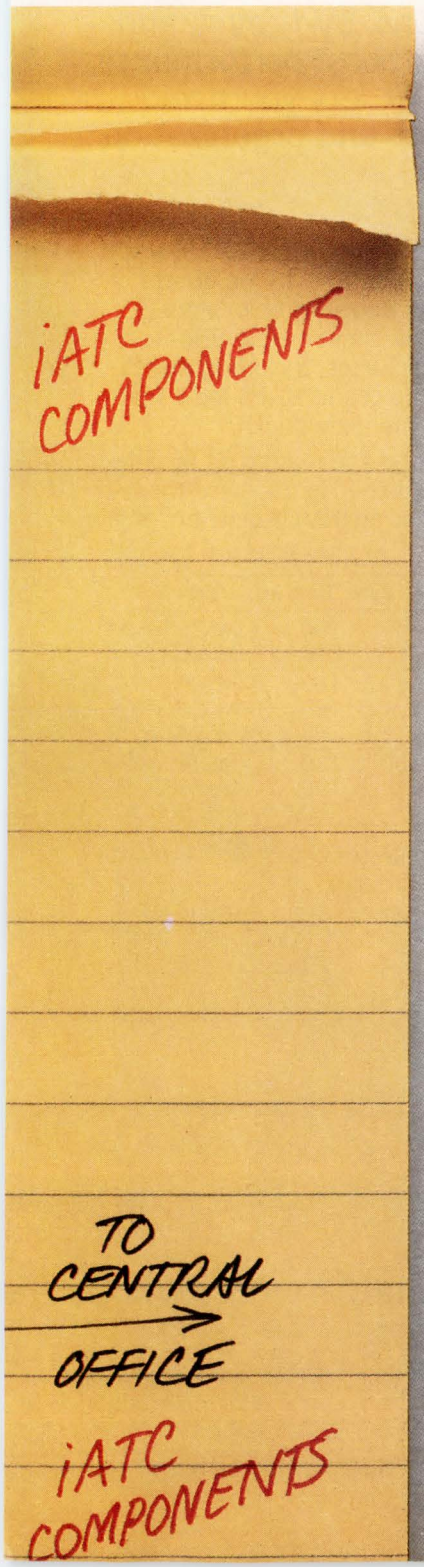

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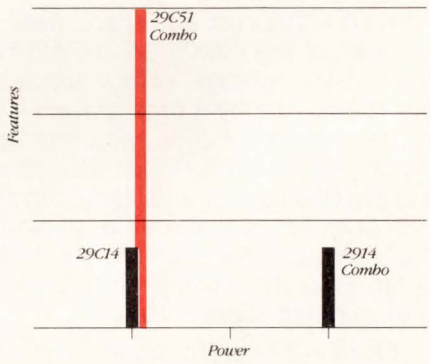

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CIRCLE 30

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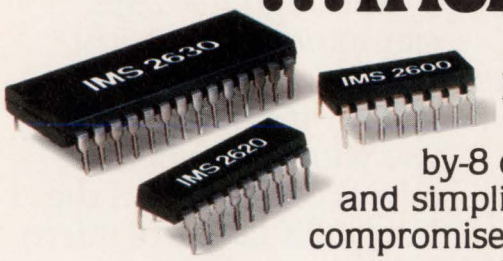

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8K x 8 — The cost and space saver. This newest member of the INMOS 64K DRAM family, available in a plastic package, offers access times of 120 and 150ns. The by-8 organization is a natural for microprocessor designs and other applications that require word width rather than memory depth...in process controllers, intelligent terminals, and buffer memories for example. And its pin 1 refresh makes it a very attractive alternative to 8K x 8 static RAMs. Because it combines low power and low cost with minimal support circuitry.

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64K x 1 — The big-system choice. This DRAM also gives you a choice of 100, 120, and 150ns access times. What's more, it includes "Nibble Mode," which allows effective cycle times below 85ns. Available in a variety of packages, including plastic DIPs, ceramic DIPs, and chip carriers, it's ideal for systems requiring lots of memory depth.

Check the chart. You'll find the industry's broadest family of 64K DRAMs...and the right device for your requirements. Then call an INMOS distributor for all the details.

Organization	Access Time (ns)	Cycle Time (ns)	Part No.
8K x 8	120	190	IMS2630-12
	150	240	IMS2630-15
16K x 4	100	160	IMS2620-10
	120	190	IMS2620-12
	150	240	IMS2620-15
64K x 1	100	160	IMS2600-10
	120	190	IMS2600-12
	150	230	IMS2600-15

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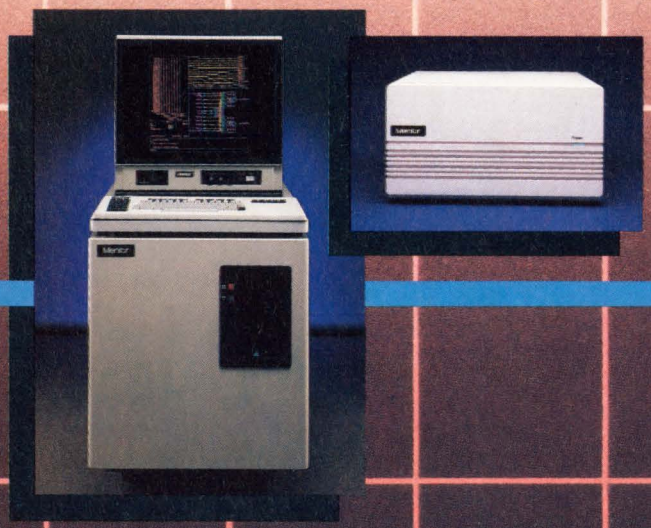

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- **Provides secondary data channel**

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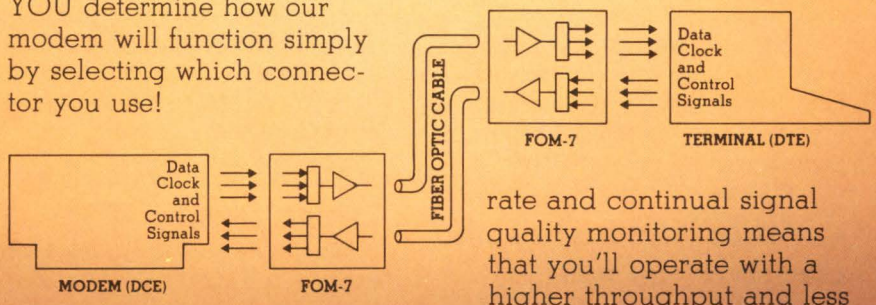

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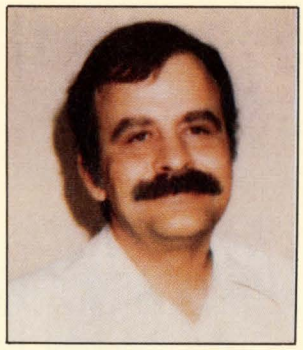
CIRCLE 33

SPECIAL REPORT ON

PERSONAL COMPUTERS FOR DESIGN AND DEVELOPMENT



Personal computers are now bringing design, development, and test capabilities wherever they are needed. These new capabilities apply throughout a product's life cycle with an intensity never seen before. An obvious reason for this increased level of design and test automation is the increased pace of product development. Add to this the demand for enhanced reliability, and it is easy to see why engineers are attracted to the low cost intelligence that can be brought to bear on their problems through personal computers.

With the personal computer, engineers can draw from a common data base and can interact with others in various departments. Communication is especially important at the initial design phases to ensure that subsequent test requirements can be realistically met. Even in a field so accustomed to rapid changes, the transition to personal computers has been explosive. These changes are apparent not only in improved productivity and advanced designs, but in increased product reliability, quality, and desirability.

Before IBM introduced its PC just three years ago, very few microprocessor-based computers had found homes in the engineering environment. The few Apples and other personal computers found in engineers' offices were used to reduce test data and to run test setups, budgets, business programs, and word processing.

Today, IBM PCs are frequently found in engineering offices, and that in a way is due to the ingenuity of our engineers, rather than a tribute to the superiority of the IBM machine. Strangely enough, engineering is considered a splinter-group to personal computer manufacturers, who measure their markets in millions of units per year. It has been estimated by some who are designing products for that group of computer users, that the total possible personal computer market for engineering and scientific use is less than 4 million units. Considering that it would take at least 10 years to saturate that market, this represents a mere trickle as opposed to the flood let loose by office automation.

So, unserved by the larger manufacturers, the engineering community has served itself (and very generously) by creating engineering tools, software, and hardware for the IBM PC. These tools incorporate design, software development, and automated instrumentation. Each has added new testing powers to its engineering discipline.

These PC-based engineering tools have helped PCs become a *de facto* minimum standard for engineering workstations. Most engineers are welcoming the PC as a low end workstation for the same reason that their managers are—they are very cost effective. Compared to the more powerful and glamorous workstations that cost around $80,000 to $120,000, a highly useful PC-based engineering workstation can be acquired for under $20,000. A specialized PC workstation can be assembled for even less. Even if price were the only thing going for it, the trend would continue and even pick up speed.

Bill W. Furlow

Bill Furlow
Senior Editor

Analogic News

BUSINESS NEWSPAPER

ONE DOLLAR

FEBRUARY 1984

ISSUE NO. 1

AP400 ARRAY PROCESSOR INSTALLATIONS PASS 1,500 MARK

INSIDE-

• New Analogic Houston Office to Support Array Processors In Oil Industry

• AP400 Series Now Interface Directly with HP A-Series Computers

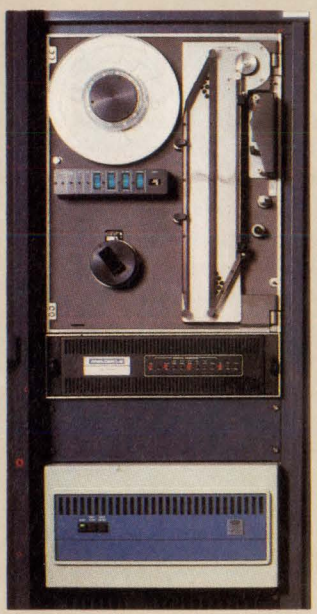
AP500 Array Processor Offers Unique, Stand-Alone Super-Computing Capability

WAKEFIELD, MA...The AP500 line of array processors has now joined the well-established AP400 line from Analogic. However, unlike any other array processor available, the AP500 has an on-board microprocessor that allows it to operate without a host for certain operations. This unique

AP400 Installed Base Now Greater Than Any Comparable Machine

WAKEFIELD, MA...Analogic Corporation has shipped the 1,500th AP400 Array Processor from its Wakefield, Mass. facility. The AP400's high performance and low cost have generated such widespread acceptance that it now has the largest installed base of any array processor in its class. The AP400 has found application in such diverse areas as medical imaging, automatic test equipment, and seismic data analysis.

The availability of the AP400 in card-set form has made it a popular choice for OEM's wishing to upgrade the



A major application of the AP400 is as a subsystem within automatic test systems such as this LTX... The AP400 offers a cost-effective means of adding powerful linear test capability to digital ATE systems.

The AP400 and ATE

The AP400 Array Processor's high-speed number-crunching power can make it a key component within an ATE system. It can serve a number of purposes in such a system, acting as an active signal filter, a high-speed data manipulator, or even as a waveform synthesizer.

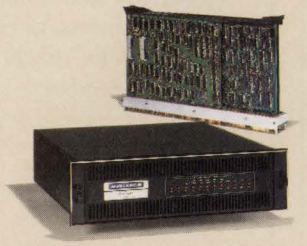
The AP400 brings the performance of computationally-intensive operations into the real-time domain. Transfer function analysis, convolution and correlation, and power spectrum calculation are but a few of the procedures which can be performed in just milliseconds with an AP400 — several hundred times faster than with an unaided minicomputer.

Minimizing host burden was a prime consideration in designing the AP400. Such features as direct memory access to the host, a powerful on-board control processor for internal housekeeping functions, and internal table storage and lookup ability mean that for many applications the host processor need only be involved in telling the AP to start and in picking up the processed data. The auxiliary input and output ports also help minimize host burden. Raw data can enter the AP400 directly, without host involvement, and processed data can be sent directly to peripheral equipment. This feature is particularly useful when the AP400 is used as a waveform generator. The AP400 can send the synthesized signal directly to a test bed without involving the host. The AP400 is currently in use in such diverse applications such as checking codec pairs and airborne radar testing. To find out more about how the AP400 can help you with your ATE problems, contact

Bruce Mackie
Analogic Corporation
Computing Systems Group
Audubon Road
Wakefield, MA 01880
1-800-237-1011
(In Massachusetts call,
617-246-0300, X2176)

AP400 Performance Features

1024 point complex FFT	7.4 ms
Real convolution (1024 data, 512 kernel)	7.3 ms
2048 point power spectrum (with Hamming window)	13.5 ms
1024 point, ensemble-averaged transfer function	1.2 s



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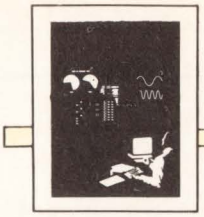
CIRCLE 34



PERSONAL COMPUTERS HAVE A GO AT ENGINEERING TASKS

The lower entry cost of PC-based design, development, and test tools, compared to dedicated workstations, opens the doors to design automation for users with modest budgets.

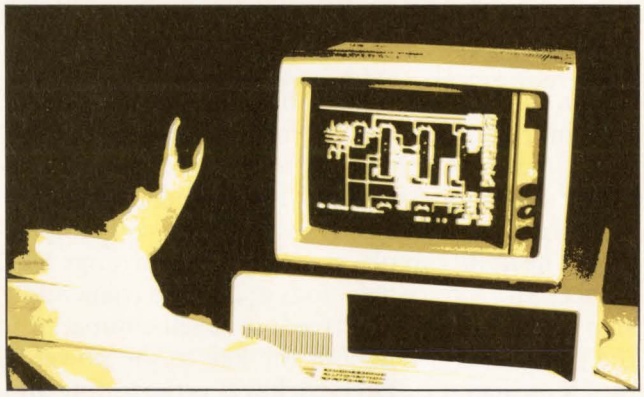
by Bill Furlow,

So many companies are now providing technical, scientific, and engineering add-ons for the personal computer that it is hard for engineers to keep up with what is available. By and large, the engineering uses of personal computers fall into three categories: design tools, software development tools, and automated instrumentation. Because all of these tools run on a common hardware base (the IBM PC) and many of them run under a common software operating system (MS-DOS), personal computers are becoming a *de facto* minimum standard for engineering workstations.

These are the same hardware and software standards that have taken the leading position in office use. Thus, the same management tools available for any manager/personal computer user are available to engineers. It is no small irony that the personal computer—first designed for office work—can save engineers more time than many engineering tools.

A recent Dataquest survey reveals that engineers spend nearly two-thirds of their workweek on nontechnical activities (eg, budgeting, planning, scheduling, report writing, and meetings). Therefore, most engineering offices should have no trouble justifying the purchase of personal computers. Dataquest also estimates that over 3000 personal computers with some form of computer aided design/computer aided engineering (CAD/CAE) capabilities were placed in engineering offices last year. Furthermore, that number is growing by 63 percent each year.

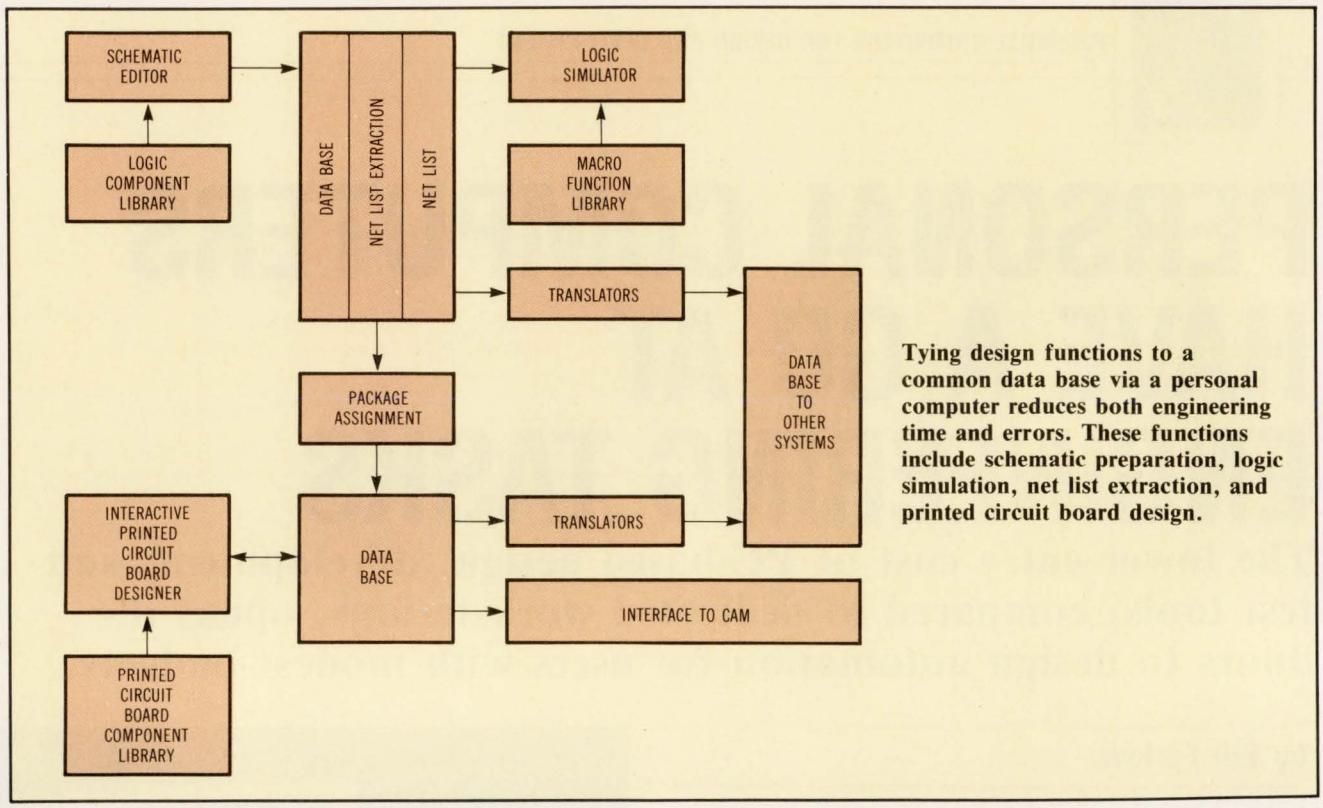
Once in the engineer's office, the personal computer becomes almost all-pervasive, taking over task



after task. The personal computer is most often used as a design tool, along with schematic design and drafting automation. Again citing Dataquest, the productivity gains from personal computer-based CAE systems are cost-effective and reaching deeper into the engineering environment every day.

Besides word processing, spreadsheets, and other reports required for their own internal controls, engineers and managers will find software packages for the personal computer that serve well for project control. Critical Path Management (CPM) and PERT packages are now available for the IBM PC, providing fast updating of project "bubble-charts" and frequent revisions of the required progress reports. Even personnel requirements and especially continuous cost analysis can now be tracked as frequently as needed, and maintained at a local level.

The day is coming when an engineer will be able to control an entire project from a personal computer. There are software packages that offer parts libraries to support schematic design and printed circuit board layout or wirewrap lists needed to automate the



Tying design functions to a common data base via a personal computer reduces both engineering time and errors. These functions include schematic preparation, logic simulation, net list extraction, and printed circuit board design.

design and production of board-level subsystems. Design packages are upgraded constantly. Most likely, major systems level projects will soon be within the capabilities of IBM PC design packages.

The packages currently available are very impressive. The ability to place, move, and rearrange logic devices and interconnections at will is a tremendous step forward in design freedom, even compared to the paper and pencil. But the key to the power of the PC schematic design packages is the testing ability early in the product cycle. Logic simulations can be run frequently, and the results of the design can be verified interactively.

Personal computers are moving testing and intelligence into the engineering cycle so quickly that anyone who has been out of an engineering lab for more than a year will not recognize the changes. There are, though, limitations to this impact. In fact, it is doubtful that personal computers have slowed down the sales volume of minicomputers or mainframes at all. The recognition of limitations at the upper end of computational capability seems to be better understood in the technical fields, and engineers are not apt to try to replace a VAX with a personal computer when the requirements are unrealistic.

The lower end of the computer market is an entirely different story. The computer terminal market, especially, is taking a terrible beating. Les White, a senior engineer at Jet Propulsion Labs, California Institute of Technology (Pasadena, Calif) reports that any engineer who is about to purchase a terminal today should consider purchasing a personal computer instead. He notes that the price difference between a terminal and a personal computer with terminal capability is very slight, and the offline computing power of a personal computer is always available. Therefore, a good use is always found for it. An offline terminal, on the other hand, merely occupies space. White notes that there were over 300 personal computers in his company about six months ago, and more come in every week. The IBM PC is the most popular with the Digital Equipment Corp Rainbow a distant second.

Testing before designing

FutureNet, Inc (Canoga Park, Calif), a newly acquired subsidiary of Data I/O Corp (Bellevue, Wash), has pioneered several design packages for IBM PCs. Introduced just two years ago, FutureNet's DASH-1 system includes a large library of pinout and operating parameters for TTL, CMOS, and ECL logic devices, as well as microprocessors, memory and support chips, and discrete components on disk. FutureNet vice president of marketing, Terry Zimmerman, reports that his company has now delivered more than 1500 of these design packages. According to other industry watchers, this accounts for 8 out of 10 such software packages sold to date. With optional enhancements to the basic software package, designers can go beyond schematic design. They can also verify the design and generate net and materials lists.

The DASH-1 system includes two expansion cards (a RAM card with 256-Kbit memory, a serial port,

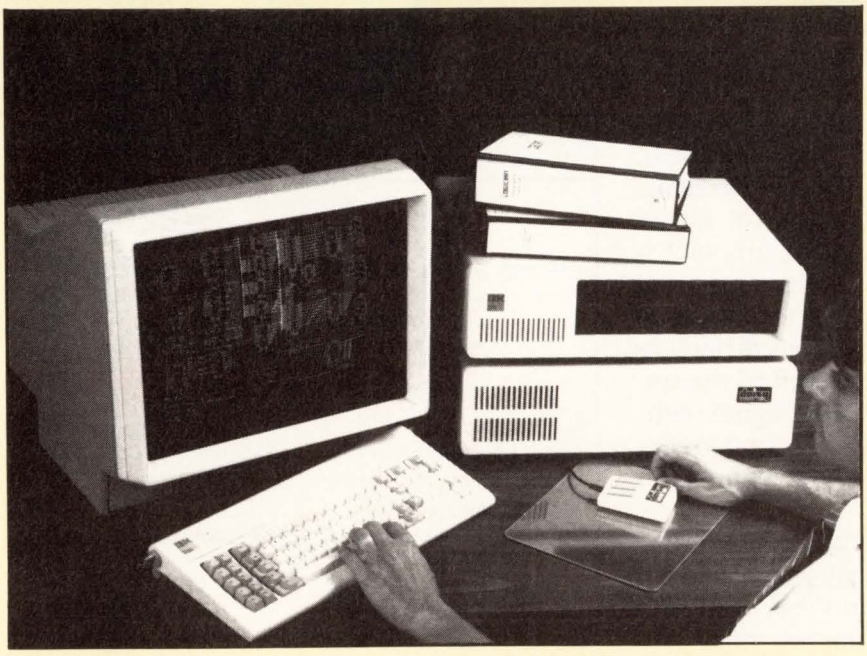
and a graphics controller board that also controls the mouse), a mouse, software library, and a 132-col printer that can generate E-size engineering drawings. The system costs less than $5400 alone or just under $13,000 if you purchase the PC with DASH-1 already installed and tested by FutureNet. The company's XT-based hard disk model is $15,000.

Zimmerman has also revealed that FutureNet will continue to enhance to the DASH systems. Priced $600 above the DASH-1, DASH-2 introduces new features, which many prospective users insisted were required before they would purchase a PC-based design package. They are tag and drag, which allows the user to capture a symbol or area on the screen and move it under mouse control; rubber banding, which allows all connecting lines to follow in real time as a device or area is moved about the screen; snap, which automatically attaches a wire to the pin which is within correct proximity when the attach command is given, even when the mouse controller is slightly off the intended target; and window save, which allows the user to mark up to four windows and recall these displays with a single keystroke. Other features of the DASH-2 system are multilevel zoom, auto-pan, and online help screens.

Design Check, an enhancement package for the DASH-1 system, checks schematic designs for unconnected inputs or outputs, duplicate signal names, missing page-to-page connections, and automatically generates a sorted list of signal names and cross-references of signal locations. Design Check costs $200. Other DASH-1 enhancement packages include software to extract net lists and lists of materials. Most companies offering schematic design packages also offer drafting packages as natural companions.

The future of PC-based CAE looks so bright that many large corporations are now being drawn into the market. McDonnell Douglas Automation Co. (McAuto of St Louis, Mo) has dipped its toe into the market with a relatively inexpensive ($500) software package for systems designers, DFDdraw. DFDdraw contains templates for all of the graphics symbols needed for the interactive production of data-flow diagrams. Scaling and size functions permit enlargement and/or reduction. The pan and zoom features allow examination or editing. Symbols are placed, connected, and annotated with text under direct user control and can be output to Epson FX-80 or FX-100 printers or a Hewlett-Packard plotter While the package is fairly simple, it is useful and inexpensive. McAuto will send a demonstration disk for $15.

Personal CAD Systems, Inc (Los Gatos, Calif) whose founders refer to the company as "P-CAD," is barely over a year old, but has captured a major portion of CAE sales for the IBM PC. Its specialized design and drafting software packages are used by mechanical and electrical engineers and architects. P-CAD is currently supplying about 15 percent of all the CAD/CAE packages being purchased for use with the PC. At that rate, FutureNet and P-CAD represent 95 percent of all such engineering packages. The company's Electronic Design Automation System (EDAS) is a series of software modules which takes the designer from schematic design through logic simulation and verification to complete a printed circuit layout with automatic schematic capture, design database creation, net lists, parts lists, and any desired hardcopy output. The separate software modules are PC-CAPS (design package),



Enhanced graphics, achieved in the Daisy Personal Logician through the use of a graphics processor, a larger monochrome or color monitor, and an Ethernet link to the local area network, turn the IBM PC into a powerful workstation.

Special interest group for engineers

PECUS (Personal Engineering Computers Users Society) is a special interest group formed last year to help engineers keep track of products, problems, and developments in the use of personal computers. The membership fee is $25 per year. For this fee, the member receives a monthly newsletter, the *Personal Instrumentation News*, and discounts on other society publications. The newsletter is scheduled to be 24 pages, minimum, and provides applications information, new product introductions, and extensive user comments.

The society's first publication, *Personal Engineering Manufacturers Directory* is also ready for distribution. The cost is $25 per copy ($10 to PECUS members) for this listing of 300 companies which manufacture engineering enhancements for personal computers. Each entry provides the company name, address, telephone, and a listing of their products. Compatibility information and a list of which computers are supported is also provided. For membership information contact: PECUS, PO Box 983, Boston, MA 02117.

PC-LOGS (logic verification), and PC-CARDS (printed circuit board generation). The entire package is priced at $9000, and modules can be purchased separately.

The schematic capture program from P-CAD supports up to 1000 nets (or symbols), 1000 components or elements, and 10,000 pins in 16 colors and as many as 50 layers. The printed circuit board package can be invoked to operate on the data base supplied by the schematic generation program and provides automatic layout for printed circuit boards of up to 500 components with up to 10,000 pins, also with 16 colors and up to 50 layers.

Using the net list generated by the schematic design package, P-CAD's timing verification module provides a logic analyzer style timing screen that models the timing behavior of up to 10,000 components. Richard Nedbal, the company president, defends the computing ability of the PC with a detailed report covering over a dozen engineering workstations. This series included tests of systems ranging from microcomputers to DEC VAXs. The times required to run the simulation ranged from a high of 45 min to a low of 11 s. Nedbal recognizes that the 11-s time (logged by a Mentor Graphics IDEA 1000) is quite a bit faster than the P-CAD time, but he notes that P-CAD's 30 s beat some minicomputers.

Requirements for P-CAD systems are an IBM PC with two disk drives (PC/XT recommended), 512-Kbit memory, color monitor, IBM color graphics card, RS-232 port, and a cursor control device (mouse or digitizer). The use of color graphics is clearly becoming a trend in the PC design areas, and is not a frill. The addition of color information to the CRT display can make a tremendous difference in the amount of information conveyed to the system user. In schematic design various signal paths can be color coded for differentiation in complex displays, as can the various wiring levels in multilayer printed circuit boards.

Other companies building workstations around the IBM PC include Case Technology and Chancellor Computer Corp, both of Mountain View, Calif. The Case CT-1000 system supports, among other software, the schematic capture and logic design (SCALD) series of timing verifiers, logic simulators, and net list post processors—familiar to users of Valid Logic's larger SCALD system workstations. The Chancellor-enhanced PC's are noteworthy because of their improved graphics. Supporting a large 19-in. full-color monitor, the Chancellor CAD 2000 provides 1024 x 768 pixel resolution, compared to the standard IBM resolution of 320 x 200 pixels.

Still not perfect

Surprisingly few efforts have been made to implement the 8087 math coprocessor with the IBM PC. Since there is a socket on the PC motherboard right next to the 8088 specifically to use the coprocessor, it would seem only natural that entrepreneurial companies would be anxious to support that capability. Despite the complaints voiced about the inadequate computing power of the PC, most companies making add-ons have found the number-crunching ability to be adequate. For those who do run into legitimate speed restrictions, some companies support the 8087. MicroWare of Kingston, Mass has hardware upgrade kits with an 8087 chip and supplies software designed to take advantage of the increased system speed. Besides development software it also offers a wide range of 8087-enhanced high level language packages, including Fortran, Pascal, C, and Basic.

Weighing the Advantages

	Advantages	Disadvantages
IEEE 488	Parallel ports, wide selection of peripherals and test equipment, and one-slot design serves many peripherals	Slower than plug-ins, 8-bit bus, complex protocols, and diverse implementations
Plug-ins	Fastest, internal bus	Limited number of slots, requires opening case to change
RS-232	Inexpensive, large number of peripherals, and one expansion board serves many peripherals	Serial ports, slowest
LANs	Fast (up to 10 MHz)	Very expensive

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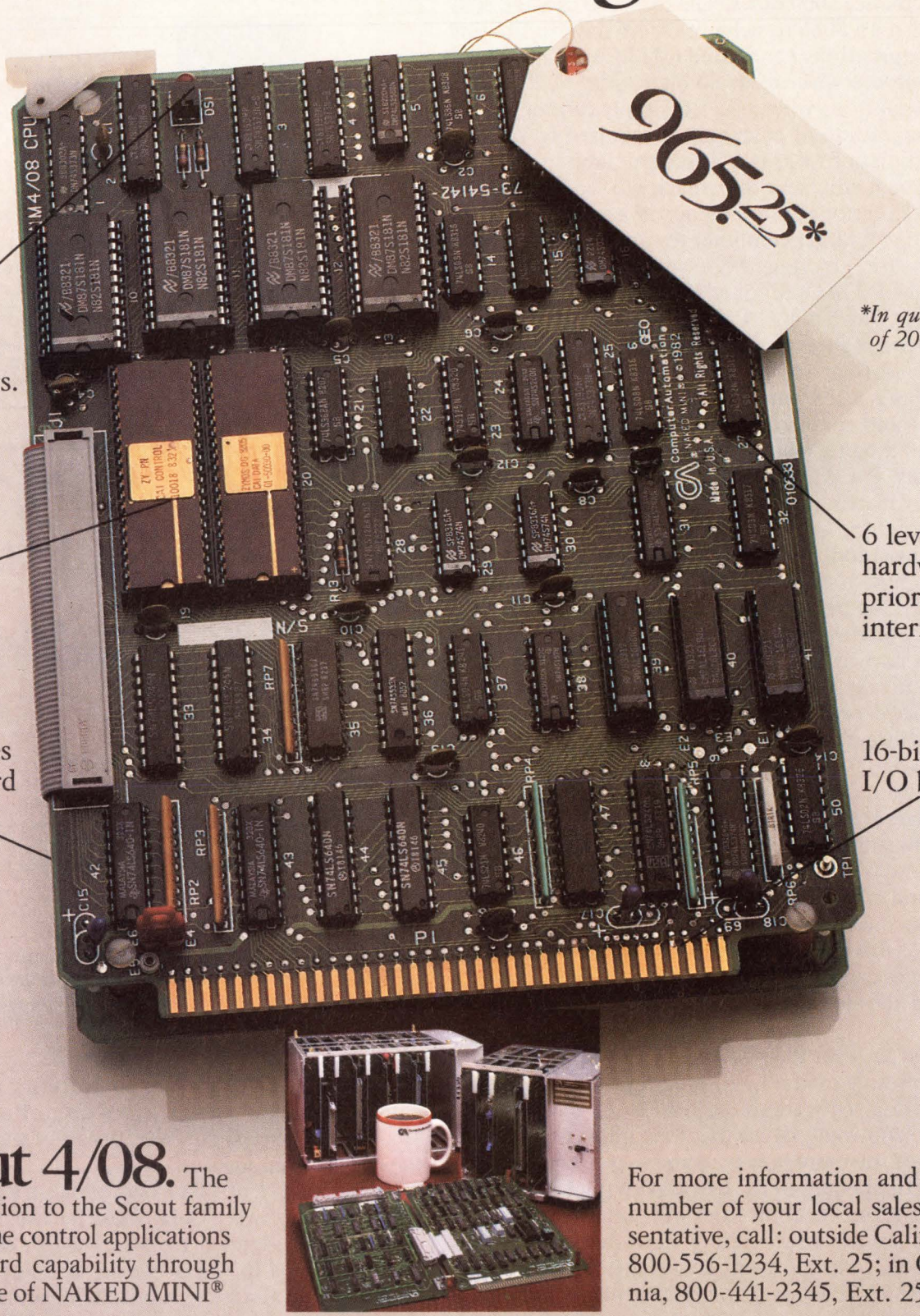

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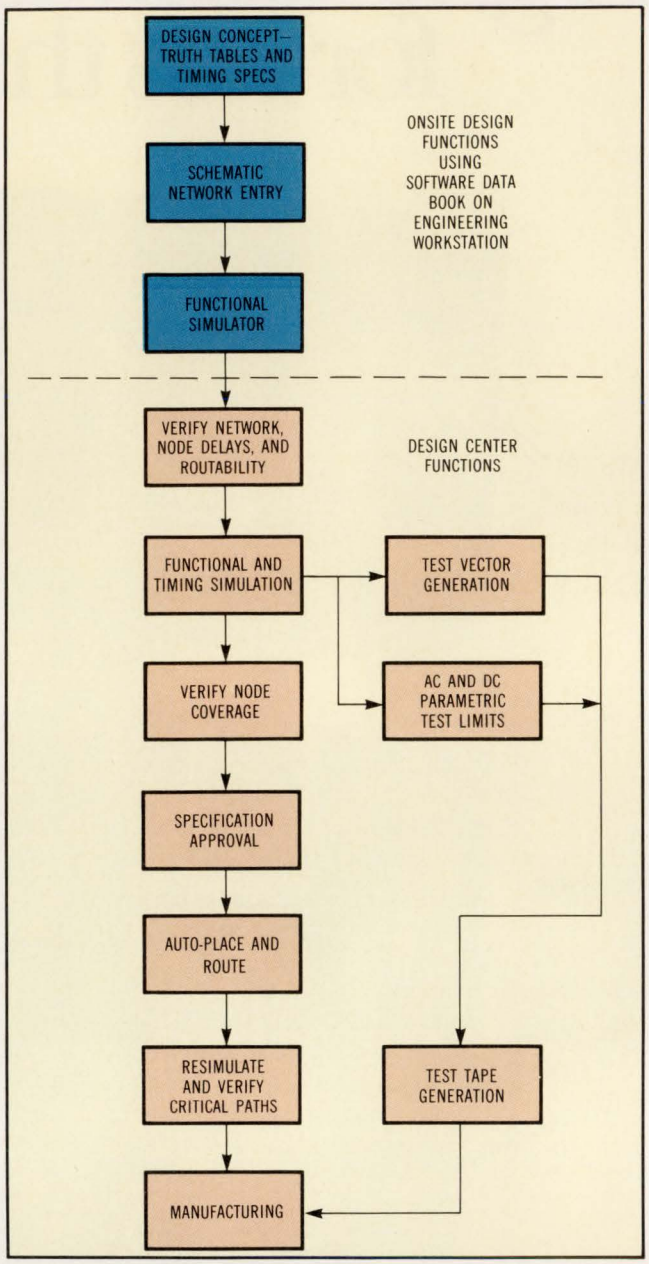
Should some really raw speed be required, Systolic Systems (Campbell, Calif) manufactures an array processor for the IBM PC that claims to increase performance 1000 times. The PC-1000 uses the 8087 and also an 8086 to achieve its 4.6 million floating point operations per second (MFLOPS) speed, and can operate with up to 80-bit words.

In situations where the PC simply cannot handle the magnitude of calculations required to provide test simulations within a reasonable amount of time, or where it still lacks the capacity to crunch through the calculations, the designer is usually forced to upload to a larger computer for analysis. These situations are growing more scarce, however. This summer P-CAD announced its NX-TDL software package which allows P-CAD's CAE software users to upload logic designs to the Tegas simulator in the correct format for analysis.

Tegas is a software package running on minicomputers and mainframes which simulates logic for devices ranging from ICs to VLSI circuits and entire systems. P-CAD has also entered into OEM agreement with Engineering Automation Systems, Inc (Kensington, Conn) which provides PC/XT workstations, modified by P-CAD along with its software, and a 10.5-Mbit/s Ethernet network link between the PC workstation and the larger EAS/770 CAD workstation. This link provides the designer with a start-to-finish design environment for the first time. It takes them from initial design concept to a finished printed circuit board.

The integration of design tasks, as in the printed circuit design packages, will be a major area of concentration as manufacturers refine their engineering packages for the PC. More than that, the integration and sharing of database information between the various design phases is receiving considerable attention and effort as the various makers strive toward their goal of providing a totally integrated workstation. As this cooperation occurs, prices for the design packages can be brought down dramatically, due to shared development costs.



Some VLSI design work is divided between mainframe and personal computers in the cooperative effort between FutureNet and LSI Logic Corp. The resulting system moves as much of the design effort as possible on to the PC. But, it still requires extensive mainframe support.

VLSI on an IBM PC—almost

The result of the intense design efforts focused on porting software to the IBM PC is really beginning to snowball. Areas that were once the exclusive realm of the more powerful and expensive workstations are opening to PC users. Although the limitations of the machine are still apparent, several companies are now offering VLSI design packages for the PC. The hardware is stretched in these applications, however, and no pretense of design testing or timing and logic verification is made.

With these limits acknowledged, what can be done with a PC is impressive. LSI Logic (Milpitas, Calif) and FutureNet have teamed up to provide a PC workstation and the required software for semicustom gate array designs. ICs up to the 6000- to 10,000-gate level of complexity can be designed on the PC. The testing is carefully divided between the customer's PC and LSI Logic's mainframe. Using LSI Logic's Software Data Book, the user can verify some of the design work on the PC (eg, calculation of logic delays in the network, and checking for electrical rule violations), but the heavyweight calculations are left to Tegas and the mainframe at LSI.

Using the PC-based workstation can save mainframe use charges while developing a custom IC. Additional time savings is also possible. Since the

PC will be at the designers workplace, travel time to and from the IC manufacturer, or mailing time required to exchange data on either tapes or disks will be reduced. But the day when an entire LSI design can be done on a PC is still in the future.

At Daisy Systems Corp (Sunnyvale, Calif) somewhat the same division of effort is made with its PC-based Personal Logician, though the hardware approach is considerably different. Daisy's engineers completely bypassed the IBM graphics, opting instead to provide a separate graphics processor and large-screen monitor, either monochrome or color, and to link their Personal Logician to other Daisy computers or the mainframe through Ethernet.

The Personal Logician represents quite a saving over Daisy's Logician Series workstations, being priced at $17,000 for the monochrome version and PC/XT. The high resolution color version is an additional $8000. This puts the Personal Logician directly astride the price barrier of $20,000, which many market research projects have established as the upper price limit for mass purchases of engineering workstations by the average engineering management company. This one is a powerful entry though, and its ability to communicate with the higher capability Daisy systems over Ethernet (a $2500 option) makes it all the more useful.

Software development on the IBM PC

At the stage of the design cycle where the software has been developed, and the hardware is designed, it is time to put the system software into firmware, then integrate and test the system design. No shortage of design effort has been noticed at this point either, and many companies are offering products to assist the designer's efforts to turn a PC into a microprocessor development system, a PROM/programmable logic array blaster, and a test system.

Several systems vie for the opportunity to turn the PC into a device programmer, most notable perhaps are Data I/O with ABEL, a high level language system for mapping and programming PROMs and PLAs, and Valley Data Sciences (Mountain View, Calif) with CUPL-based packages. These systems, priced at $7000 to $8000, run about the same as a standalone programming system. Valley Data marketing manager, Steve Walters, points out that the PC-based units are the Cadillacs of this market, because of the increased advantages of high level language, far easier setup, and the ability to write test programs that will run as soon as the device has been programmmed. All these features would add greatly to the price of a standalone unit.

Software development system prices are being driven down by the PC workstation, too. Microcosm (Portland, Ore) has adapted development system software and manufactures in-circuit emulators for the 16-bit Intel microprocessor families, including the 8088, 8086, and 80186, to run on the PC. Since this eliminates the cost of the manufacturer's development system hardware, users can save a significant amount by pressing their PC into development service. By the time they have reached the software stage, engineers who do not already have the development system required for the latest designs will have to take a hard look at the PC approach. Like others in the field American Automation, Inc (Tustin, Calif) has chosen the RS-232 port to swap

IBM discovers engineering market

A unique opportunity existed for other manufacturers to grab a large piece of the engineering computer market for the first three years after IBM introduced the PC. However, following the introduction of the IBM PC AT (see *Computer Design,* Oct 1, 1984, pp 27 and 225), IBM also announced graphics and engineering enhancements, proving that it is now interested in the engineering computer market. The company has served notice to other manufacturers that the window of opportunity is closing.

While the PC AT silenced many critics who claimed that the PC simply was not powerful or fast enough to be a true engineering computer, several users still voiced reservations over using a business machine in engineering, especially lab instrumentation. IBM has directly addressed these concerns with its engineering design tools.

The PC data acquisition and control adapter provides a PC user with four analog inputs and two analog outputs, 12-bit A-D resolution and 16 channels of digital input and output. At $1275 per board and $160 for the controller software package, a PC is suddenly a very viable industrial or laboratory controller. Since each PC can control up to four of these boards, the limitations of using PCs in this application have been pushed back considerably.

Graphics for the PC are also considerably enhanced with two new color displays and controllers. IBM's Enhanced Color Display and its adapter board provides 640-pixel/line horizontal resolution and 350-line vertical resolution with 16 onscreen colors selectable from a palette of 64 colors. But the big news for CAE users is the new PC Professional Graphics Display. This $1295 monitor and its $2995 controller provide 640 x 480 pixel resolution with 256 colors displayed onscreen from a palette of 4096 colors. Using 60-Hz refresh (versus 30-Hz for most color systems), to provide flicker-free display, the Professional Graphics System signals IBM support of the Virtual Device Interface (VDI) and the graphics software standard from Graphics Software Systems of Wilsonville, Ore (see *Computer Design* Nov, 1984, p 34).

Richard Nedbal, president of Personal CAD Systems, says that the adoption of this standard by IBM bodes well for engineering PC users. P-CAD's software packages have supported the VDI since they were introduced, and Nedbal credits the system for his company's ability to support so many different monitors for CAD/CAE use of the PC. It allows them to write hardware independent display drivers that will handle any monitor, and Nedbal says that VDI is the first usable standard to be introduced.

data between the PC and its emulators which have a great deal of added intelligence. Choosing to communicate through the RS-232 port has made many of the in-circuit emulators rather host independent.

Although Microcosm supports VAX, PC, or Intel development systems, marketing vice president, Rob Haubner notes that 80 percent of the product inquiries he receives concern products for use with the PC. The PC adds lower price and ease of use to the system, according to Haubner. His equipment stores all trigger definitions and setup parameters to disk. Thus, users can pick up exactly where they left off with a single keystroke, instead of checking an array of switches or entering a long setup procedure. Haubner sees no problem in supporting 32-bit micros with the PC, noting that his company will be announcing support for non-Intel, 16- and 32-bit microprocessors. Most engineers designing systems around 8-bit processors already have development systems in-house. Thus, he feels, there is no market for those systems.

Other suppliers of development systems for the PC include Genesis Microsystems (Sunnyvale, Calif), Hilevel Technology, Inc (Irvine, Calif), and Atron Corp (Saratoga, Calif). Atron recently introduced the PC Probe, which provides a logic analyzer, a realtime trace, and high level language compatibility with assemblers and PL/M, Fortran, Pascal, and C compilers. It is intended for software/hardware development and debugging. Total Logic Corp (Fort Collins, Colo), one of the early supporters of Apple-based logic analyzers (along with NorthWest Instrument Systems), offers a 32-bit logic analyzer for the PC which boasts a 1-Kword memory and 15-MHz operating speed.

Altera Corp (Santa Clara, Calif) has just introduced a PC development system to support its EP300 Erasable Programmable Logic Device (EPLD), a CMOS floating gate erasable PROM, bringing a level of prototyping ability to the PC that fits right in with the software development now being done on PCs. Others providing the capability to download to field-programmable devices include Valley Data Sciences, Seattle Computer, Inc (Seattle, Wash), and Apparat, Inc (Denver, Colo).

Untraditional test equipment

The control of test equipment setups with PC engineering tools is not a new idea—IEEE 488 controllers have been doing that for more than a decade. So, it may be merely a logical extension of traditional test equipment, oscilloscopes, logic analyzers, and voltmeters made or adapted to run under PC control. The result is more synergistic, though. The data logging capabilities of PC-based instruments are overwhelming compared to the general-purpose

Automated checking of design rules and verification of system logic are typical of personal computer design systems. This system from EAS and P-CAD provides complete printed circuit board design, from the initial layout to the finished product.

As many as 320 Winchester drives can be tested every eight-hour shift using Wilson's new MDTS-1000 Multiple Drive Test Station.

With a continuous flow of 32 drives attached, the system can automatically certify up to eight drives* every 12 minutes. That's faster throughput than from any other digital test system on the market!

For All Volume Users

Designed for production floor testing, large-scale incoming inspection and burn-in applications, the MDTS-1000 accommodates all 5¼" drives with ST506 interface, up to 16 heads and 2048 cylinders. Future advanced interfaces such as ESDI, ST412HP, etc., can be added easily on site.

Composed of eight standard Wilson DTS-1000 Drive Test Stations linked through an RS-232 MUX to an MS-DOS based microcomputer, the MDTS-1000 uses the computer for centralized logging, test control, CRT display and data printout via a high-speed printer.

The standard Wilson test includes verification of basic drive functions, followed by media verification, read margin and drive voltage margin testing. Modified or custom tests can be added if desired.

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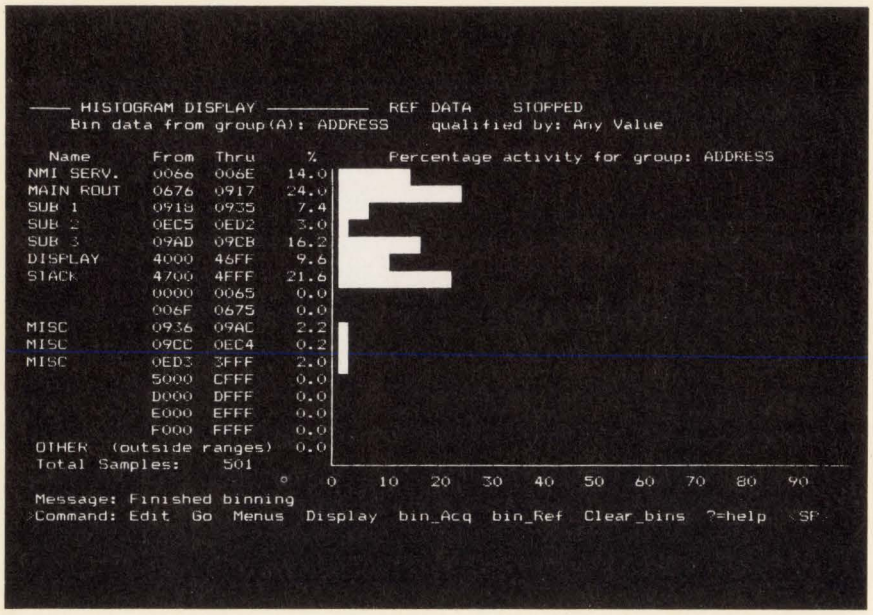


A histogram display on the PC-based logic analyzer by NorthWest Instruments details the percentage of bus activity via memory address blocks. Because of their computational ability, such instruments offer unusual flexibility and data logging capability.

interface bus (GPIB) devices because of greater bus bandwidth and larger memory. This feature is very handy for scopes and analyzers running in unattended automatic test equipment (ATE) configurations, because records can be more complete. Also, waveforms that appear on the PC screen are digitized and ready for further processing. Beyond that the appeal of an integrated design, development, and test workstation is obvious.

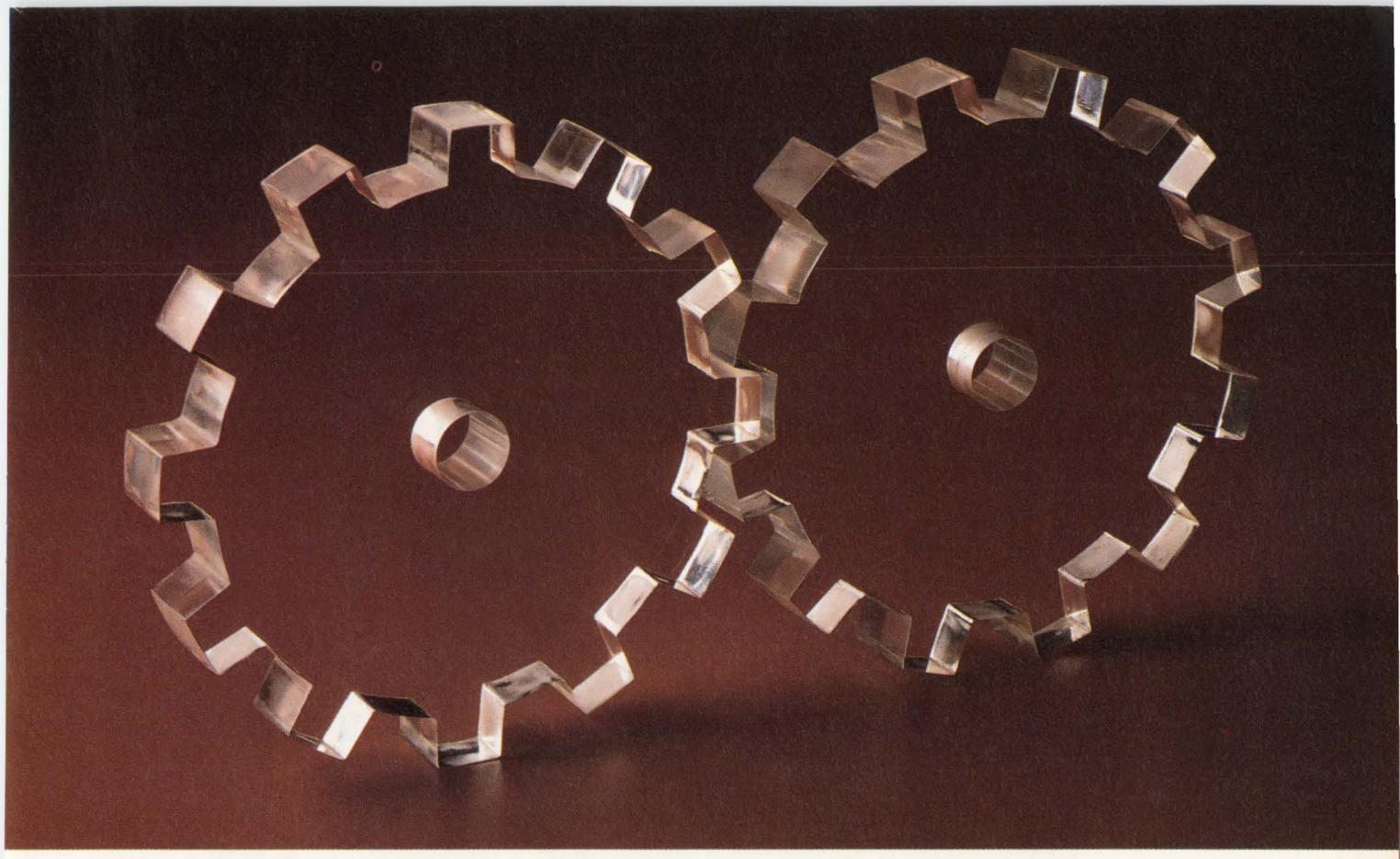
NorthWest Instruments, Inc (Portland, Ore) was probably one of the first companies formed specifically to build instrumentation capabilities into personal computers. Starting with a dual-channel oscilloscope for the Apple II, less than three years ago, its engineers, quick to see the change that was quietly underway, introduced μScope products for the IBM PC. Its newest line of products is the μAnalyst system, a series of interactive state and logic analyzers with up to 80 channels of data acquisition at up to 100 MHz. Besides supporting the Apple II series, IBM, and Compaq personal computers, NorthWest has been very active in verifying its system's compatibility with other personal computers. The company recently announced that its logic analyzers have also been verified to be compatible with the Columbia MPC, Columbia VP, and Eagle PC-Plus.

NorthWest has also recently inked an OEM agreement with Mentor Graphics (Beaverton , Ore) who will market the μAnalyst under the Mentor label as a hardware verification system (HVS). The HVS would be an option for the IDEA-Series workstations. Test and development tools like the μAnalyst are proof that personal computer-based testing is a serious engineering technique. Most likely traditional test and measurement equipment manufacturers will follow this direction in the near future.

Limited expansion slots a problem

Some drawbacks to expanding the IBM PC are the limited number of expansion slots and the hassle of swapping expansion cards in and out of the system. There are three unused slots in the standard PC, five in the XT (although some are not full size) in their usual configuration. Although there are many advantages to plugging directly into the PC bus, the space to do so has definite limits. Keeping the lid off of the PC to make changing boards easier is inconvenient, because the lid is the normal support bench for the monitor. Another drawback is that the original PC is supplied with a 65-W power supply that will not carry much additional load. Although the supply for the XT has double the power of the PC, it is still not endless. The IBM expansion unit offers a ready solution for many of these problems. But, since it is available only with a 10-Mbyte hard disk, it is not an inexpensive solution.

Many manufacturers have opted, therefore, to communicate to the PC through either an IEEE 488 parallel bus adapter or an RS-232 serial port. More companies are now also beginning to support the high speed local area networks, such as Ethernet. Each of these solutions requires only one expansion slot on the PC, and offers almost unlimited access to external test equipment. The IEEE GPIB interface is supported by Hewlett-Packard, Tektronix, and Fluke, as well as others. This solution brings



The Strategic Supplier Knows That Accomplishment Is Best Driven By A Direct Relationship

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CIRCLE 37

most ATE equipment within reach of the engineer using a PC. The high volume production levels reached by the PC bring it to the user at a price below any of the generally used GPIB controllers, and this has prompted many companies to offer GPIB controller boards for the PC.

The data logging capabilities of PC-based instruments are overwhelming compared to those of the GPIB devices.

Joe Looney is president of Tampa, Fla-based Vistar, a supplier of analog instrumentation and IEEE 488 controllers for the IBM PC. He feels that the strength of the PC in instrumentation is its ability to interpret between the GPIB peripherals from different manufacturers. As these instruments become standardized, the slight differences can often be accounted for in the controller program.

One of the original companies to supply PC-based instruments, NorthWest Instruments, is touting its new μAnalyst as second to no other logic analyzer. According to Jim Fischer, vice president of marketing, the μAnalyst stands up to any standalone analyzer on the market. He feels that a spec-by-spec comparison against a machine like the Hewlett-Packard 1630 makes this obvious. For example, NorthWest offers 80 channels versus 65 for the 1630; 15 trigger levels versus 5 for the 1630; 60 word recognizers versus 5 for the 1630; and the list goes on. According to Fischer, the two systems measure up like this because the 1630 is a discrete instrument at the end of its development line, while PC-based instruments are just beginning to mature.

Several control interfaces

In an unusual move to allow the use of its new system digital multimeters, the Metrawatt Div of Brown Boveri Corp (Broomfield, Colo) has announced that the M2110 will be available with the choice of three different control interfaces at $695. It is available with IEEE 488, RS-232-C, or Centronics parallel interface, and boasts 30,000 count resolution as opposed to the usual 20,000 count meter. Citing 1-mV resolution at 24 Vdc or 1 μA when measuring 20-mA current loops, the M2110 can be set and triggered either locally or by remote control over its bus—a handy feature for some test setups. There is one disadvantage, however, that helps explain the lower than normal price—it does not talk back to the bus. Readings must be taken visually by an operator. ATE systems will find little use for such limited capability.

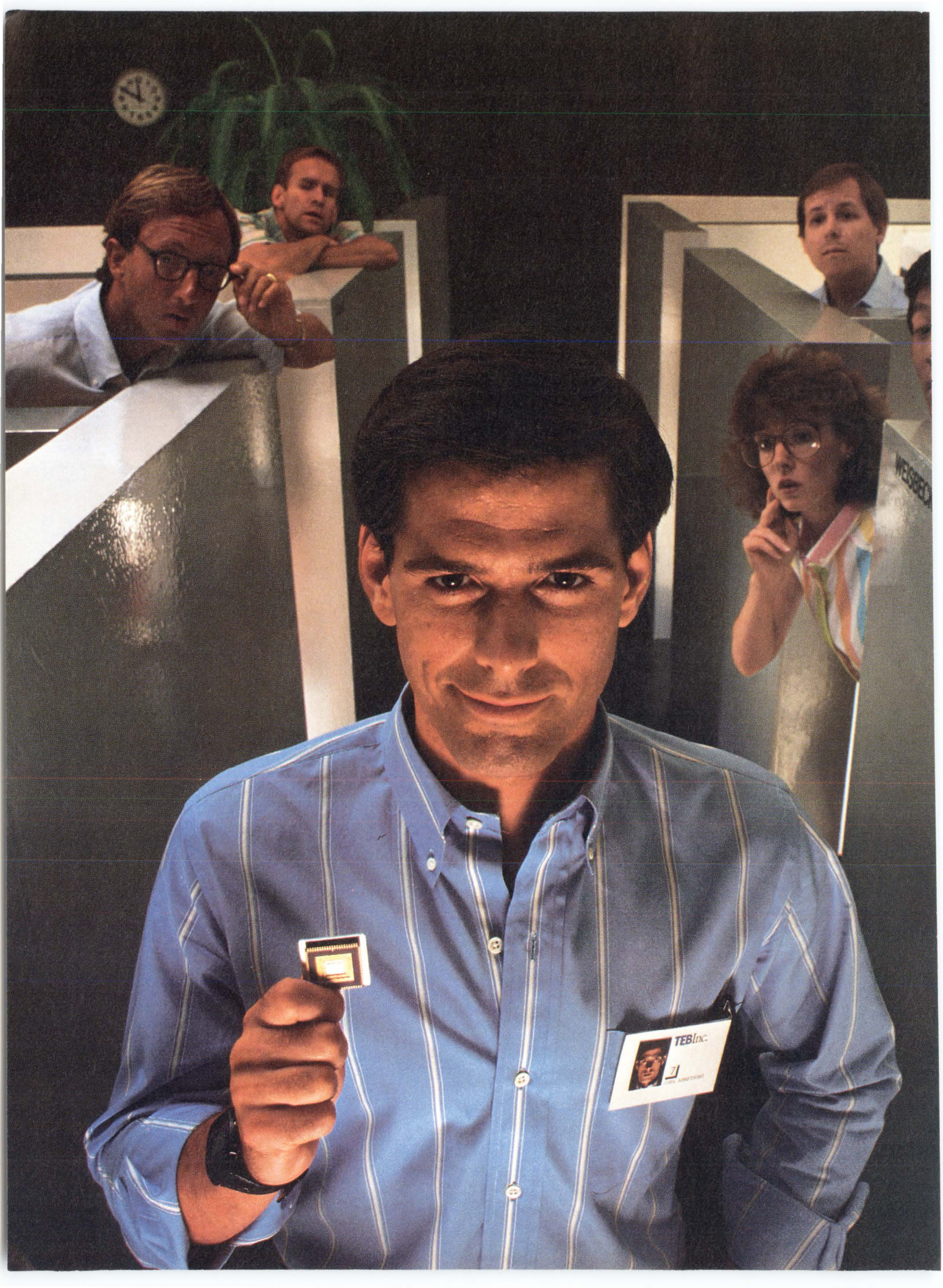
Production test facilities, however, looking for a method of automating their test setups and willing to dedicate a test operator to reading and recording the dial, may find some appeal to this scheme. A great deal of engineering skill has been applied to turning the PC into a piece of ATE. Engineers wishing to put the PC to this application will find many vendors anxious to assist. Just as samples of such, Data Translation, Inc (Marlboro, Mass) provides a variety of data acquisition modules to tie the PC to external sensors. GPIB interfaces are available from a half dozen manufacturers, which will provide access to a wide range of test equipment all controllable from the PC.

Sophisticated test equipment

Finally, as a sort of preview of the truly sophisticated ATE that we could be seeing in the future, there is the Logic Master series of functional testers. Designed by the group of engineers who created the Tektronix DAS, Integrated Measurement Systems' (Beaverton, Ore) Logic Masters are actually host independent, interfacing over RS-232 or IEEE 488 buses. But it has been demonstrated with a PC host, and a lot of early interest has been shown in this configuration. IMS spokesmen claim the machine is the missing link that is needed to tie test and verification into CAE. Its Logic Master aims at automating the test fixture and test pattern generation which consumes so much time during the design of custom ICs. The mainframe contains all the hardware required to stimulate prototype and production ICs, acquire the resulting output, and verify proper functioning. The Logic Master also links with the design console of Daisy, Mentor, Valid, Calma, or Metheus workstations to automate the test development from the design data base.

The IBM PC has started a revolution in engineering design and development. It is bringing testing ability wherever it is needed. As the PC tackles engineering tasks, better products and utilization of work time should result.

Got a second?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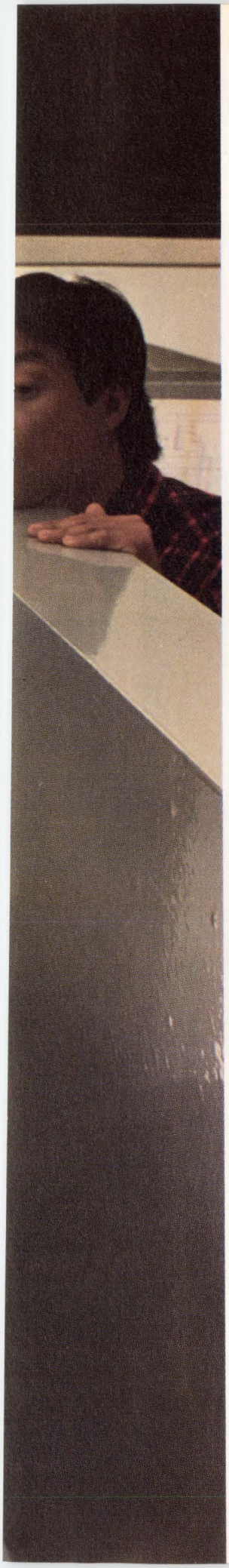

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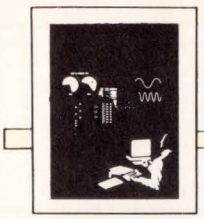


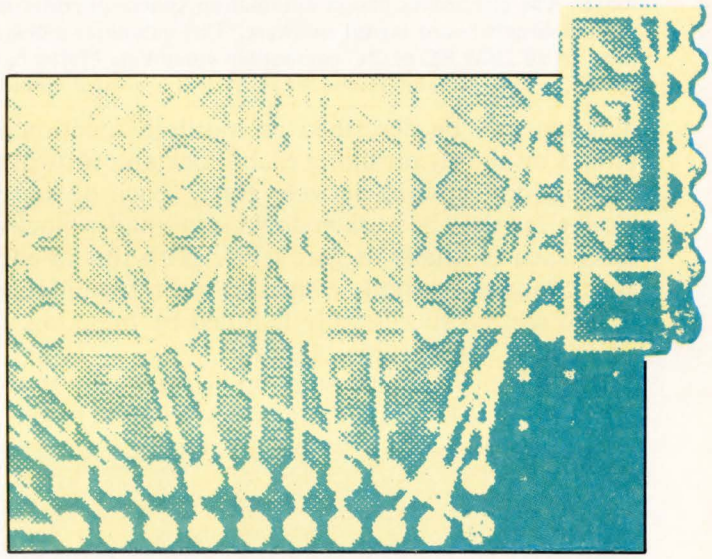
SOFTWARE OFFERS LOW COST DESIGN AND SIMULATION

A set of CAD/CAE tools for IBM PC and PC-compatible computers provides logic design, logic simulation, and interactive printed circuit board design.

by Greg Houston

Workstations have reduced the entry costs of computer aided design/computer aided engineering systems to less than $100,000, but the cost is still too high to provide each engineer with a workstation. A CAD/CAE package running on a personal computer, however, would bring a complete standalone system with local memory, dedicated computing power, and disk storage to the engineer's desk. The engineer would learn one operating system and one keyboard, and have a consistent interface to both local and remote tools at every design step. One computer that can support CAD/ CAE is the IBM PC. Although the PC does not have the power to create a full custom VLSI chip design, or to auto-route a large, dense printed circuit board, tasks such as logic design, simulation, and interactive printed circuit board design are well within its capabilities.

The electronic design automation (EDA) family of CAD/CAE tools from Personal CAD (P-CAD) Systems, Inc combines hierarchical logic design, interactive logic simulation, and printed circuit board layout software in an integrated set of modular packages that run on IBM, or IBM-compatible, personal computers. Schematic capture and logic simulation for integrated circuits are also provided. These packages provide not only a complete front-to-back path, but also allow entry and exit anywhere along the path (Fig 1).



In the conceptual stage of layout and design, the logic design package, PC-CAPS, is used. An engineer can design the logic of a board or integrated circuit with a hierarchical design approach, using a top down and/or bottom up strategy. A complete logic

Greg Houston is director of marketing for electronic design automation at Personal CAD Systems, Inc, Los Gatos, Calif. He is one of the company's founders and has over 10 years' experience in CAD/CAE.

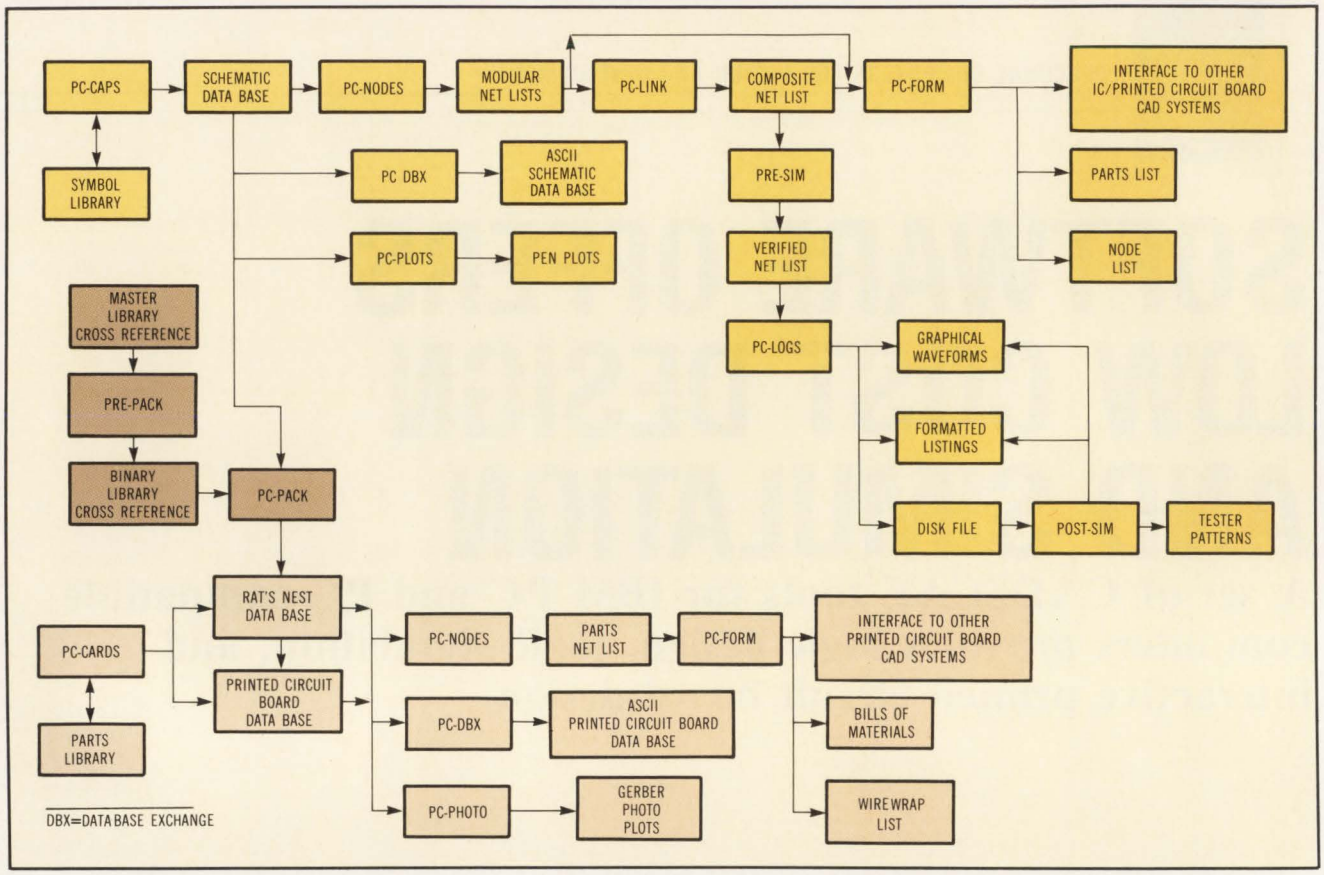


Fig 1 The electronics design automation system provides hierarchical logic design, interactive logic simulation, and printed circuit board layout software. This computer aided design/computer aided engineering (CAD/CAE) system runs on an IBM PC or PC-compatible computer. Major components include PC-CAPS, a logic design package; PC-LOGS, a logic simulator; and PC-CARDS, a printed circuit board design package.

diagram can be described as multiple functional blocks by simply outlining each block and showing the interconnections between them. Each of these blocks can then be broken down into smaller blocks until each is finally at gate level. With this divide and conquer method, even the most formidable design can be successfully handled by breaking it down into manageable blocks.

Conversely, a logic design can be created by starting at the gate level, building up one or more blocks, and then combining the blocks to form higher level blocks. If needed, one portion of the logic can be created from the top down and another from the bottom up. In this way, very large complex designs can be broken into manageable levels. At any time, an engineer can "push" down into a block to examine its component parts or alter its structure, then "pop" back to the parent level (Fig 2).

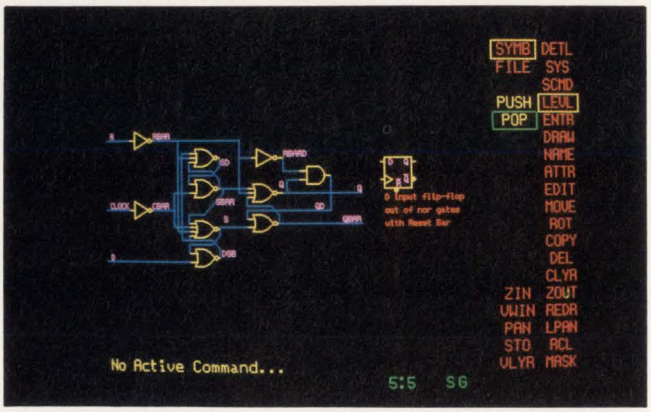


Fig 2 The PC-CAPS logic design package allows logic design to start from the top down or the bottom up. The engineer can "push" down into a block to examine its component level, then "pop" back up to a higher level.

Using a hierarchical approach

The graphics editor of PC-CAPS is also designed with a hierarchical approach. Commands that are not directly involved in creating or editing data are nested below the data entry commands. For instance, while in the middle of creating a net between schematic elements, engineers can perform several different operations. They can pan to different areas of the logic, zoom in or out, view another window of data, change the active layer or grid, and select a different line type or width. As soon as the nested commands are finished, the system pops back the net being created with a rubberbanded line from the last point. This nesting feature allows engineers to manipulate the data base graphically and change parameters without losing track of the work being done.

Net lists and simulations can be done from any level of this hierarchy, even from multiple levels.

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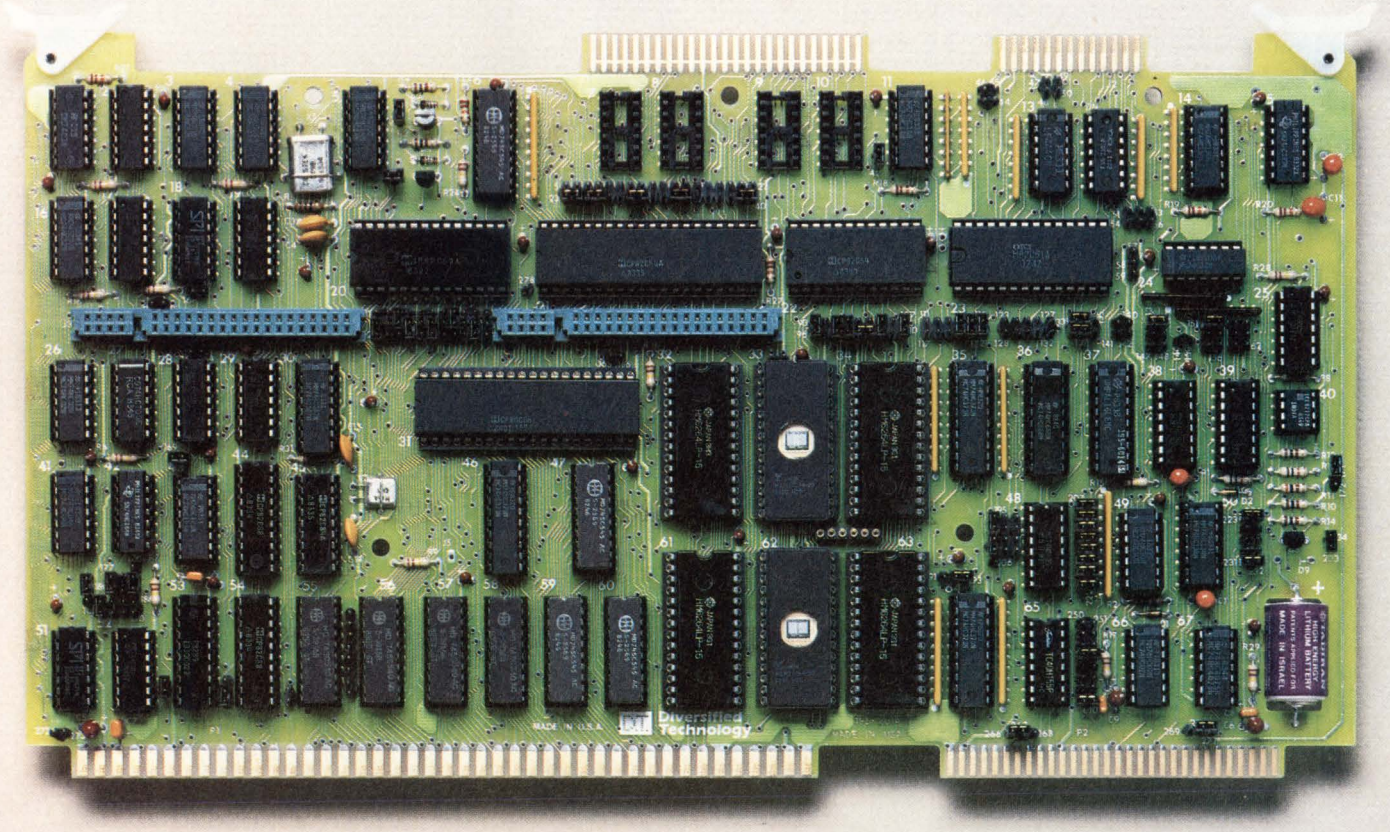

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PC-CAPS is designed to support multiple levels of hierarchy with each level capable of handling 1000 components, 1000 nets, and 10,000 pins. A menu-driven graphics editor allows the engineer to manipulate logic elements on the screen quickly and easily, and interconnect them. Key attributes can be assigned to each element, pin, and signal. Supply and driving strengths, pin names and functions, and other electrical characteristics can be given. Interconnects can be named as they are created. Otherwise, they will be automatically assigned by PC-CAPS.

To help the engineer avoid wiring errors, connectivity is created and checked in real time. Nets can be created by starting at any point, and disjointed nets can be connected by giving each net the same name. To avoid confusion, an entire net can be highlighted instantly by simply touching it. Tasks such as entering net names are simplified by an automatic net naming command. Once a net name has been given, the net can be identified by touching it anywhere. The entire net is highlighted, and the name is automatically shown on the screen. The cursor is then used to position the name wherever it is desired, at any size or rotation.

The integrated data base lets rise and fall delays be separately modeled and specified at the logic creation level.

Edits or changes are facilitated by a complete set of edit functions operating in real time. When symbols are rotated or dragged around the screen, all connections are automatically maintained and rubberbanded with the symbol. Symbols or elements can be altered or created on the fly without having to save the schematic. The user can create a symbol, then call back the schematic to use it. Altering existing nets is accomplished by a set of edit features that can move, add, or remove vertices (corners), and move for delete segments.

Simulation: analysis before building

When a logic diagram, or a section of a logic diagram is completed, the logic simulator (PC-LOGS) can be used to analyze the logic for functionality and performance. PC-LOGS is an interactive 12-state simulator that uses the net list from PC-CAPS as its input. This simulation package will typically simulate from 500 events/s on a normal IBM PC, or IBM-compatible computer, without an 8087 coprocessor. PC-LOGS uses an event-driven algorithm. This means that only the logic elements that have changed states need be evaluated at any given point in time.

Twelve logic states are provided with three logic levels (high, low, and unknown) in four driving

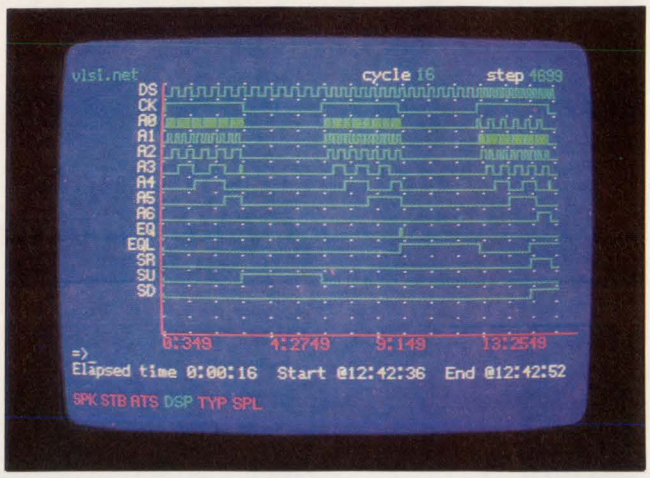

Fig 3 During the logic simulation phase, the engineer can view outputs from PC-LOGS as graphical waveforms. The simulation can be started and stopped at any time, with up to 16 output states probed at once.

strengths (supply, driving, resistive, and High-Z). These 12 states allow accurate modeling of wire-ORs, MOS transistors, and other 3-state devices. Net lists can be extracted from PC-CAPS at any level, or multiple levels, of their hierarchy and simulated. Up to 5000 nodes or approximately 3000 components can be handled. The outputs from PC-LOGS can be viewed on the screen as graphical waveforms (Fig 3), and formatted text listings. They may also be saved on a disk file for later use in generating test patterns, pen plots, or for further post processing.

An engineer using PC-LOGS has, in effect, an oscilloscope probing a board. The simulation can be started and stopped at any time, with up to 16 output states being probed on screen at one time. These probed nodes can be changed at any time, and their values can be forced to a given state to alter the logic interactively. The user can set programmable break points, rubberband the clock times to compress or expand the clock rates, and trap hazardous conditions such as spikes and zero-delay oscillations. And, the user can control the analysis of all these conditions.

Due to the integrated data base, rise and fall delays can be separately modeled and specified at the logic creation level. PC-LOGS can simulate at both the logical gate level and at the transistor or switch level. Higher level blocks such as ROMs and RAMs are modeled as well. P-CAD builds in an extensive set of logic elements for quick, easy modeling. A post simulator program provides a utility to process the simulator output, thereby creating tester programs and formatted listings.

Once a logic diagram has been created and simulated, the physical layout of a printed circuit board can be accomplished with PC-CARDS. The first thing a designer notices with PC-CARDS is that the menu interface is very similar to PC-CAPS. All similar commands are in the same place and work in the

same manner. PC-CARDS allows board designs up to a maximum of 60 x 60 in., with 500 components, 2000 nets, and 10,000 pins on one to 50 layers. Unlike many other systems, PC-CARDS allows layers to be named. These names include, for example, component side, solder side, padmaster, silkscreen, etc. In addition, PC-CARDs allows the designer to select the number of layers desired. If the designer creates 8 layers, only 8 layers are shown. More layers can be added to the design at any time by naming the layer, assigning it a color, and deciding whether or not to view it.

Printed circuit board design

If a schematic is done on PC-CAPS, an autopackager program will compile all logical gates into physical devices and perform a rough placement of all components onto a board. This lets the layout designer begin the design with all components already inserted, and all connections shown as airlines or rat's-nest connections (Fig 4). The designer can then swap and move components while viewing the rat's nest to improve placement. The updated rat's nest shows how the board routing is affected by the swap or move. After all components have been arranged for optimum placement, the designer can enhance the routing further by swapping gates within ICs, and swapping pins among gates.

The next step in the layout process is to interconnect or route the traces. Traces can be wired by starting at any point: at a component pin, an existing wire, or in free space. As with PC-CAPS, PC-CARDS checks online continuity while making the connections. Also as in PC-CAPS, the nested viewing commands allow the user to view the results of component manipulation while creating or editing data.

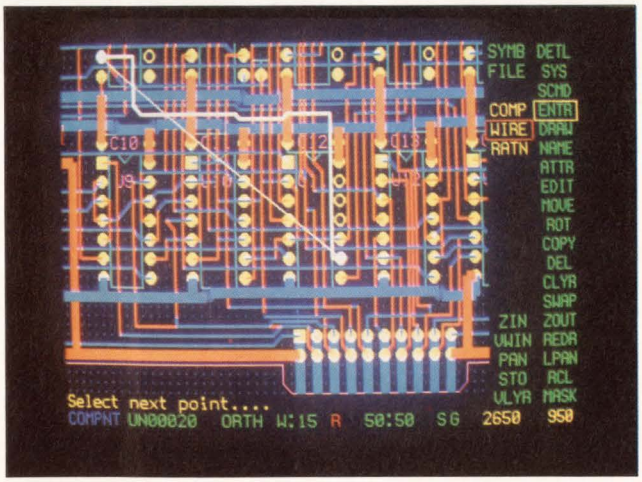

Fig 5 PC-CARDS allows the engineer to automatically "stitch" wires between layers, while routing traces interactively. Choosing the layer select option in the menu ends the line on the current layer, inserts a feedthrough, and starts a line segment on the next layer.

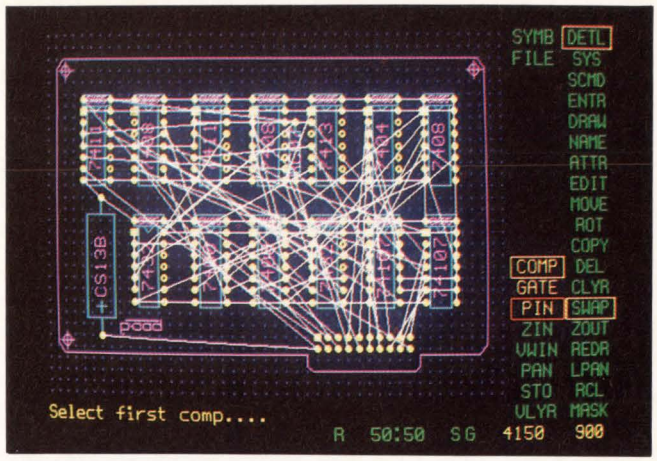

Fig 4 The PC-CARDS design package shows the rough placement of all components on a board, with rat's-nest connections. The engineer can swap and move components while viewing the rat's nest.

During trace routing, designers can automatically "stitch" wires between layers while interactively routing traces (Fig 5). By setting two or more layers enabled for routing, designers can begin a wire on one of the enabled layers, and start routing it to the next point. When forced to drop a feedthrough and move to another layer, designers can choose the layer select option on the menu. This ends the line on the current layer, inserts a feedthrough, and starts a line segment on the next layer. If only two layers are enabled for stitching, the layer toggle will switch back and forth between these two layers. If three or more layers are enabled, each selection of the layer toggle option will go to the next higher layer. Finally, the selection will return to the first layer once the last layer has been toggled. Thus, designers can interactively route as many layers as desired, or stay with the traditional layer-pair method of designing.

Designers also need to change trace widths. The ability to change widths in the middle of a trace makes "necking down" of wire widths between IC pads easier. A layer-viewing command allows designers to change the color of a layer at any time and then turn it off or on, for viewing or plotting. For instance, in routing internal traces, they need to view only the padmaster, the layer showing reference designators, and the trace layers they are working on. The tedious job of editing existing traces is done quickly and easily by using specified commands. These commands allow moving of wire segments among layers (with Automatic via Removal), moving wire corners, and adding and deleting points from an existing wire.

Customized commands: user defined

Some specific board designs require special commands or processes, such as wire pairs and controlled stub lengths for 100-K ECL designs. To address these problems, PC-CARDS and PC-CAPS incorporate

a user defined macro capability. This feature allows the user to create macro level commands from those supplied by the company. To create a macro, the user chooses a name or key by which the macro will be called and begins executing the desired commands. Each command selection, cursor move, and keyboard stroke is recorded for playback. A macro can contain variable length pauses, and wait for user input, or for either defined or user input coordinates. Every feature of PC-CARDS or PC-CAPS is usable by macros, and macros can be "nested" or called from each other.

Error recovery and power failure backup are major concerns with any CAD/CAE system. Since all jobs are held in RAM while being worked on, a power failure could result in the loss of an entire day's work. Massive errors can also be introduced by a user who inadvertently deletes a major section of a job or uses all incorrect trace widths or components on a job. PC-CARDS and PC-CAPS help avoid these problems by automatically creating an operator log with each session. When a session is started, a disk file is opened in which every command, keystroke, and cursor move is logged to disk as the buffer becomes full.

If power is lost, the user merely restarts the program and executes this command file. This command file operates on the same principle as a macro. Everything previously done is replayed at high speed and recreated up to the last point at which the log is filed to disk. If users make an error, they have two options. They can replay the file and stop it before the error was induced—or they can edit the file with a word processor to remove or change the error. Since this feature is automatic if turned on, it ensures that a running backup is constantly maintained. The ability to play back a session also helps in finding where a design error occurred and aids new users.

Postprocessing: the final step

A common source of irritation to CAD/CAE users is the poor support of postprocessing operations. They are either unsupported, or are cumbersome and inefficient to use. The company provides a full set of utilities that functions in the same fashion as its main programs. Some of these utility programs are available now (such as facilities for pen and photo plotting, wirewrap lists, back annotation, and net list extraction). Others will be available in the near future and will include facilities for N/C drill tapes and bills of materials.

As an example, PC-PLOTS supports over 20 different industry standard pen plotters with one program. With this approach, users can add a pen plotter to the system later and not have to return to P-CAD for a specific formatter. Or, if beginning with a low cost plotter and later upgrading to a faster, larger plotter, users already have the software. They do not have to wait or pay for a new program. To create a plot, users define a plot window on the job by any two opposite corners. A file is written to disk containing only the graphic information within the defined window on the layers that were viewed. This disk file is used by PC-PLOTS on the particular system to which the plotter is hooked.

Designers can interactively route as many layers as desired, or stay with the layer-pair method of designing.

Users choose the plotter, sheet size, the area of the sheet to be used for the plot, and the desired scale. The system does not allow a scale that will result in a plot larger than the given area. It will also automatically center the plot on the defined area. Pens are selected by the system, based on the colors used in data creation. If the plotter is a drum plotter, the paper is automatically advanced to a clean area after the plot is finished.

By using a disk file, users can define several plots at one time and continue working without waiting for the first one to be completed. PC-PLOTS also takes advantage of print spoolers to plot in background mode while users work on another design. A future product for N/C tape generation, PC-DRILL, works in the same fashion, supporting the multiple formats of drill machines.

Photo plots can be created by several methods: photo data can be sent over a modem to a remote photoplotter; a magnetic tape can be generated and sent to a service bureau; or a photoplotter can be driven directly by the personal computer with P-CAD software. Other future utilities include PC-BILL for bill of materials generation and wirewrap lists, PC-DRC for design rules checking, PC-NCC for net list consistency checking, and PC-BACK for back annotation of schematics.

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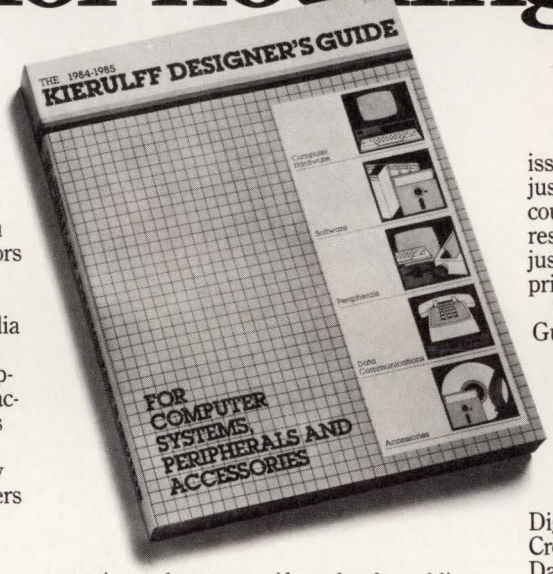

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CIRCLE 42

SOLVING THE MYSTERY OF THE BLUE SKY PHENOMENON.

This is the 2nd in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.

In the microprocessor world, the "Blue Sky Phenomenon" refers to microprocessor development code crashes. The code simply and quite mysteriously disappears. The most common culprits are bugs. And the fact is, simple program bugs will crash most microcomputers.

The hosts for some of these bugs have famous names. What they all have in common is an absence of mechanism to protect against crashes. There is one exception.

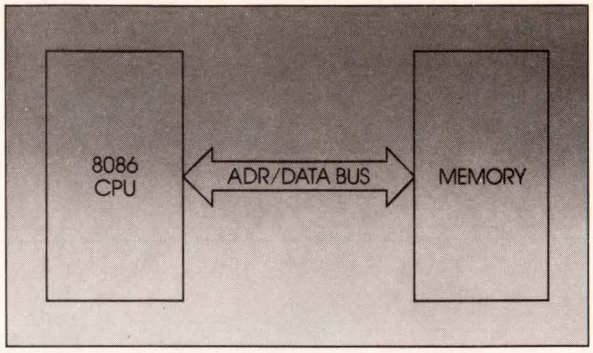
The Zilog Z8000® family provides comprehensive hardware protection to help create systems that are resistant to system crashes so common in primitive architectures. The Z8000 CPU is not only more reliable in this sense, but it's easier to learn how to use. Especially if you already know how to use the ubiquitous Z80® CPU.

LOST IN THE WILD BLUE YONDER.

There is a technological reason why some microprocessors are so prone to corruption. It stems from the direct connection of the memory to the processor. Without any checking hardware between the processor and memory, the processor can change any area in its memory at will—without regard to the consequences. Such a lack of restrictions allows illegal operations such as changing program memory stack underflow (running the stack into the data area), and even modifying the code of the operating system. This lack of appropriate technology has two glaring results:

- Illegal operations cannot be detected before damage has occurred.
- Any damage to the program and data cannot be undone.

There are far-reaching implications for a lack of memory protection. Systems designed without it do not support multiple users, nor even UNIX™ very well. The simplest bug will crash the system. There is no protection and no recovery mechanism against even minor problems of access violations. The ability to handle more than one user is usually not allowed, or is strongly discouraged.

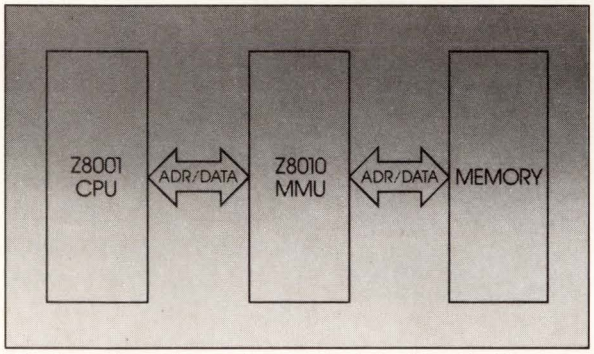


A typical Intel 8086-to-8088 configuration, the lack of memory checking hardware—the memory to the processor. The processor can change any area in its memory at will, without regard to the consequences. The result: illegal operations cannot be detected before damage has occurred; and any damage to the program and data cannot be undone.

THE Z8000 CPU—THE FULL-PROTECTION MICROPROCESSOR.

Zilog's Z8000 CPU solves these problems by inserting a chip called the Z8010 MMU (memory management unit; available in paged or segmented versions) between the processor and memory. This chip normally passes addresses from the processor to the memories—checking each memory access for its address and type of operation as it occurs. If the MMU chip detects an illegal operation, or the use of an unauthorized address, it suppresses the illegal operation and interrupts the program. It passes control to the operating system. Once the program is stopped, the operating system can inspect, correct, or abort the program that caused the error. All with no wait states.

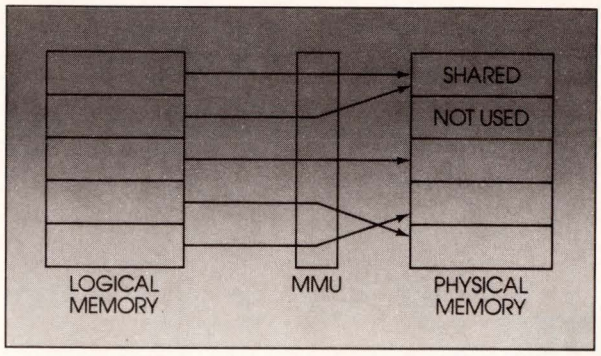
A system constructed with the Zilog MMU can allow many different programs to run without the fear that one program could entirely stop the rest or even corrupt the rest. But, the memory management hardware goes beyond providing protection. It also simplifies system implementation.



Zilog's configuration system prevents the Blue Sky Phenomenon by inserting a chip called the Z8010 Memory Management unit between the processor and memory.

HIGH LEVEL LANGUAGES REQUIRE MEMORY MANAGEMENT.

One of the strengths of 16-bit microprocessors—and the Z8000 CPU in particular—is that they support high level languages such as C, PASCAL and FORTH. A goal of most users is to allow more than one of these high-level language programs to execute in the processor at the same time (multi-user/multi-tasking)—gaining more effective utilization of the computer. The challenge is to provide an architecture that allows a language compiler to produce code targeted to run at one address, but allows the actual placement at a different physical address. This mapping is known as logical to physical translation—a feature of the Z8010 MMU.



Zilog satisfies the common requirement for systems to share information with our MMU. The logical-to-physical translation capability allows more than one logical area to access a common physical area.

SHARED MEMORY IN THE Z8000 CPU.

Another common requirement for systems is the need to share information. With Zilog's Z8010 MMU, the logical-to-physical translation capability allows more than one logical area to access a common physical area. When combined with the protection capabilities of the Zilog MMU, you can set up areas that can be common read-only while the same physical area could be read AND write when accessed under different conditions (operating system access).

For example, you could construct a process control system that posts status information into a common area. The central core of the system is allowed to read and write this common area. Application programs that need access to this information can read it through a totally different segment that is translated into the proper physical address—but with the provision that all access must be reads, not writes. If an application program were to run wild and attempt to corrupt the common area by writing into the read-only space, it would be intercepted before any write could occur.

The key benefit to using Zilog's MMU to implement shared memory is its flexibility to make multiple logical segments access a common physical area with all of the protection—or lack of protection—desired. All with no overhead per access. What's more, Zilog's MMU and other Z8000 devices are available from a host of reliable second sources.

Solving the problem of the "Blue Sky Phenomenon" is only one of the technological hallmarks of the Z8000 CPU. Others will be discussed in this continuing series of technical papers from Zilog, Pioneers of the Microworld. For details on the Z8000 CPU, call our Literature Hot Line at 800-272-6560.* Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.
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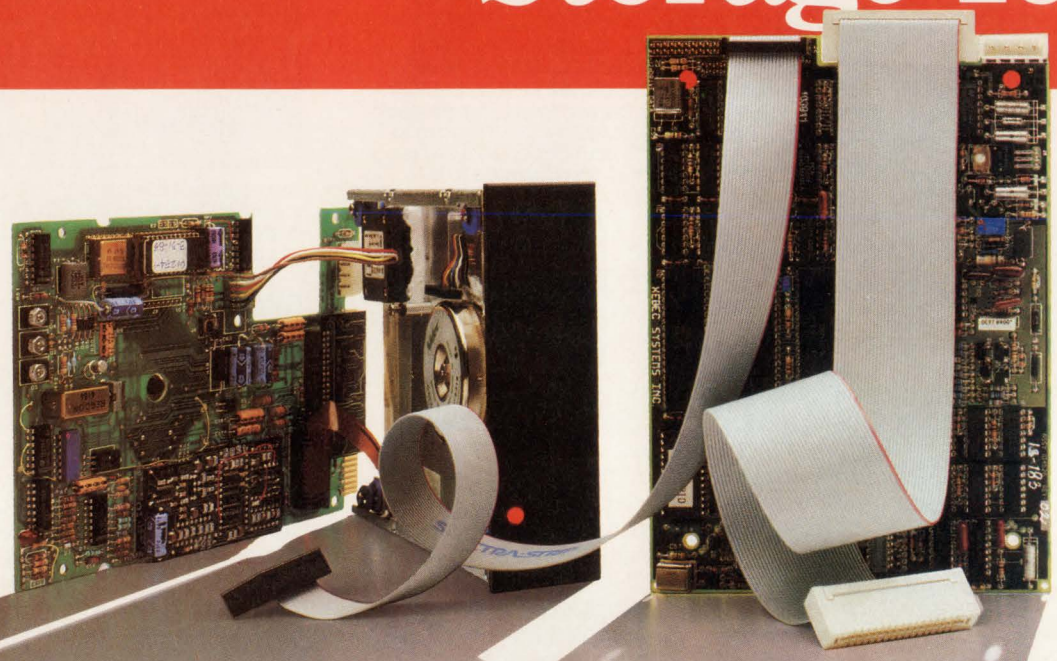

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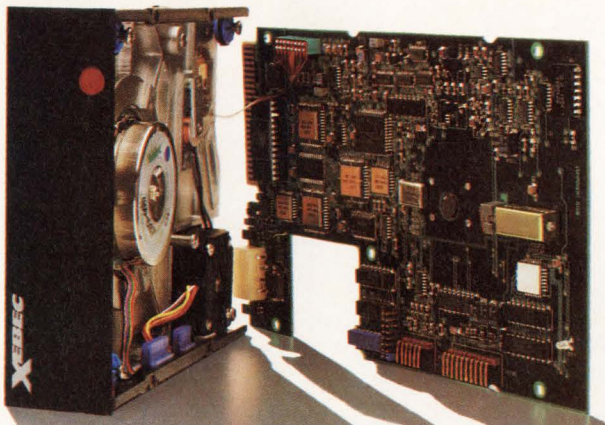

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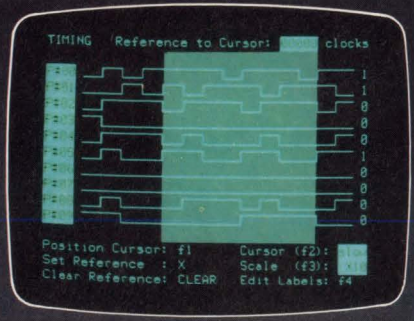

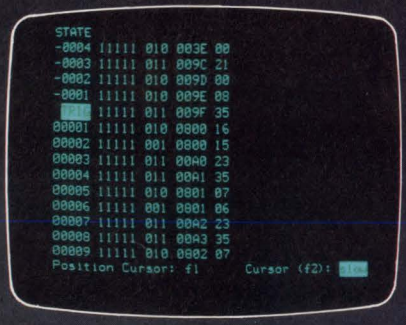

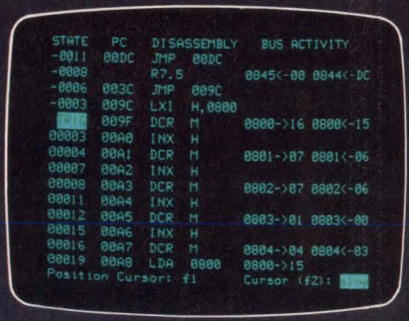

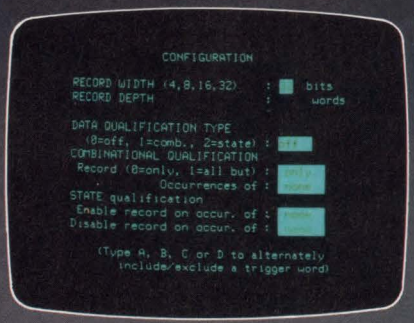

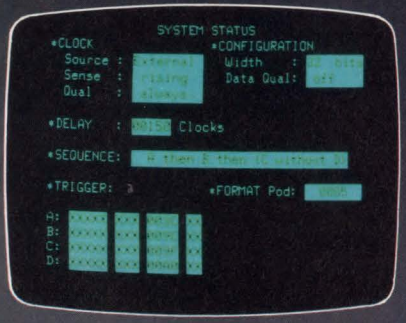

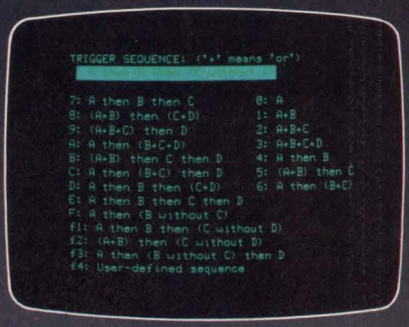

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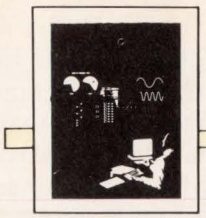

LOGIC ANALYZER CHECKS OUT PLAs

PC-based test equipment can provide dynamic in-circuit testing of in-house programmed logic devices, eliminating reliance on static screening to weed out detective parts.

by Thomas A. Brubaker and Edwin L. Harper

Many companies have introduced new versions of traditional electronic test instruments that are combined with personal computers. These systems offer the engineering community relatively inexpensive, but very capable computer-based instruments that have potential for test and measurement in the design and manufacturing of electronic equipment.

One example is the LA-200, a logic analyzer for use with the IBM PC. The LA-200 transforms the PC into a logic state analyzer with a 32-bit data/trigger bus. The analyzer and the test procedures can be called from software as subroutines. In addition, they can place data onto the PC data bus or into memory to be called by other routines. Thus, data collected can either be logged continuously or stored on magnetic media. Both of these functions lend the LA-200 an advantage as its storage is limited only by the storage limits of the PC.

The analyzer stores 32,768 bits per data set, and can store 17 captured data sets per floppy disk in the IBM format. In addition, each data set stores the parameters which were set for the tests, so that recalling a particular test set for comparison can also set the current test. As a part of a PC-based design and test system, test sequences can be developed at the time of the initial design work or they can be derived from the design data base. This information can be shared among all departments, which will require it for later testing of either the individual components or the systems in which they are installed.

One useful application for such an instrument is the testing of programmable logic arrays (PLAs) and ROMs used to implement combinations of logic, firmware, and logical sums of products (AND/OR logic). Because they offer a significant parts count reduction, these logic elements are used to implement a broad spectrum of combinational and sequential logic ranging from decoders to sophisticated state machines and microprogrammed computer structures (see the Figure).

PLAs and ROMs are tested statically during the programming process. Here the logical expressions are programmed into a system and appropriate

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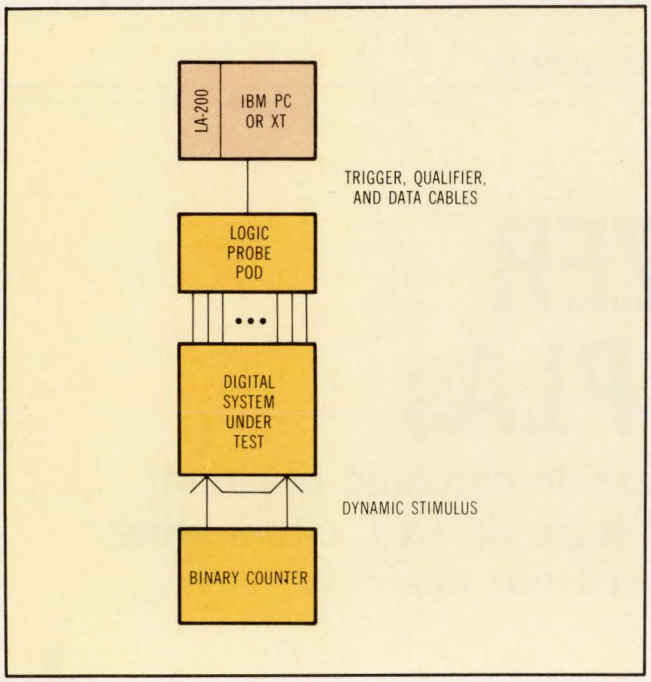


Testing field programmed devices during the programming cycle tests only static characteristics. Using a simple binary counter as a dynamic stimulus and a PC-based logic analyzer as a monitor provides an inexpensive dynamic test set for these devices.

circuit links "burned." High and low voltages are measured and appropriate error messages are generated if the device does not meet specifications. Besides checking the correct voltage levels for each bit, checksums are one evaluation of correct programming and are often provided.

Checking PLAs and ROMs during programming only provides a partial evaluation of the integrity of device operation. The devices are typically not excited dynamically with signal sources during the programming phase. As a result an assessment of the devices' dynamic operation is not available before they are integrated into a digital system. Dynamic testing requires a source to excite the device under test and a logic analyzer to capture the data. The source and the logic analyzer may now be integrated with the IBM PC to form a programmable low cost test system.

Testing PLAs and ROMs with PC-based logic analyzers and sources is a more meaningful test of these devices. As a result, manufacturing and field service costs could be reduced through prescreening the components. The testing of systems that incorporate PLAs and ROMs is also advisable, and can incorporate some of these same techniques along with the overall test of the system.

This test set is more useful than a conventional logic analyzer because it can store a complete and verified test sequence in computer memory and record data only when the input does not result in correct output. A trace of the entire test sequence need not be recorded. Recorded documentation of the test can be as simple or as complex as circumstances dictate. Perhaps more important, a test may be filed away for months and repeated whenever a small batch of new devices is ready for testing since test setups are stored on disk along with results.

Testing programmable logic arrays

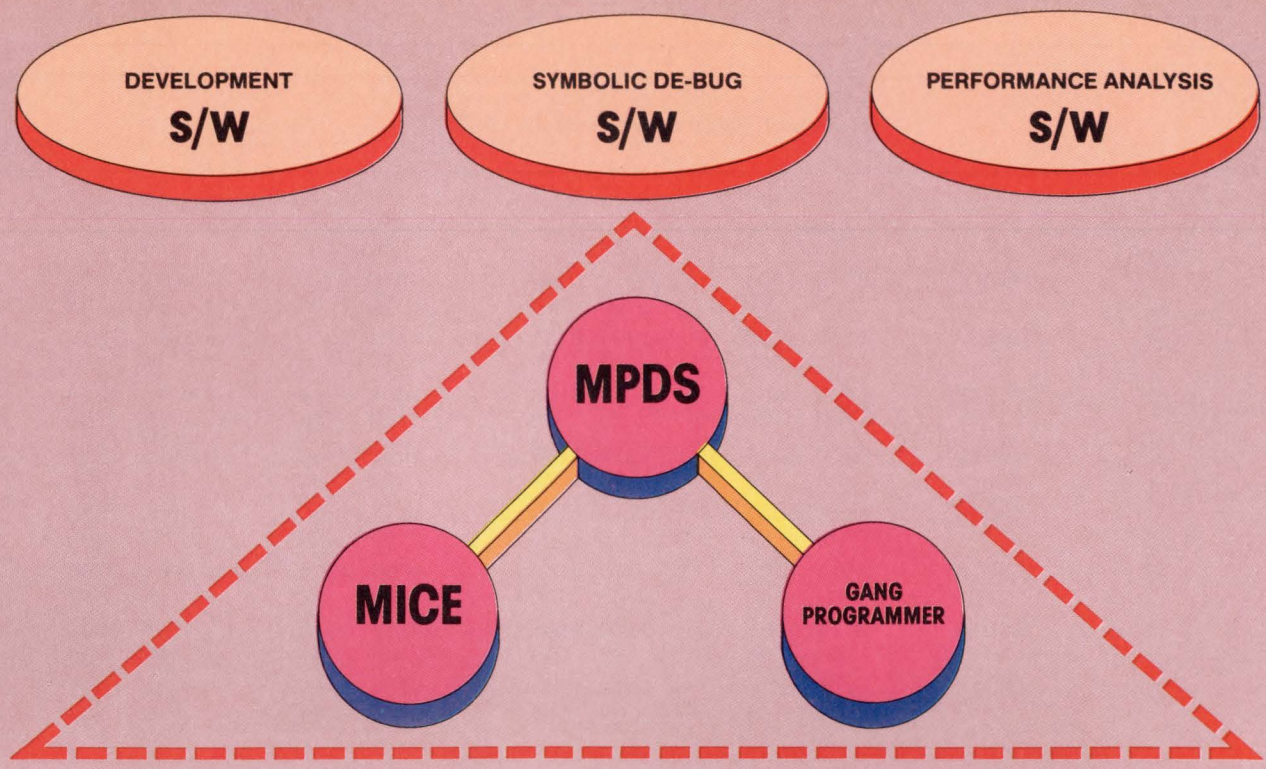
To illustrate the use of the LA-200 in testing PLAs, consider the combinational logic 20-pin AND/OR or AND/NOR devices such as the PAL-20 family manufactured by Monolithic Memories. These devices have 18 input and output pins, ranging from 10 inputs and 8 outputs to 16 inputs and 2 outputs. Each input represents one term in a logical product and each output represents a logical sum of products or the inverted logical sum of products. For the 16-input system with one OR output, a maximum of 16 product terms can be implemented. A 10-input system with 8 outputs allows 8 logical sums of products to be implemented with each sum having 2 products.

One simple method that can be used to excite a PLA is a counter. If all 16 inputs are used, a 16-bit counter is required to generate all possible input sequences given by $2^{16} = 65{,}536$. The time required to generate the input combinations equals 65,536 divided by the clock frequency. Because most logic analyzers store only 1024 to 2048 data points, efficient testing will utilize clock qualifiers. An appropriate clock qualifier is connected to the output and the 16 data lines are connected to the logic analyzer inputs. When an input sequence activates the output data line, the input sequence is stored. Otherwise the input sequence is ignored. (See the Table, "Typical Trigger Schemes for the LA-200.")

The storage limit of the PC is the only restraint on the LA-200's storage capacity.

From a timing point of view, if the counter is driven using 0-1 transitions from a clock, the logic analyzer can be armed to accept data on the 1-0 transitions of the clock. This requires the clock pulse width to be greater than the delay time of the PLA under test. If the zero hold specification of the LA-200 is used, the logic analyzer is armed to take data on the 0-1 clock transitions. Here the 0-1 clock transition at time $t = nT$ results in a PLA output after the delay time D. The PLA output activates a clock qualifier which enables the logic analyzer to store the input sequence on the 0-1 transition of the clock at time $t = (n + 1)T$.

If only sequences that fit the logical design of the PLA can generate an output, the stored data will



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CIRCLE 46

Typical Trigger Schemes for the LA-200

Triggers		Byte 4		Byte 3		Byte 2		Byte 1	
1	START	0100	1001	0010	0100	0010	0010	0010	0000
		(4)	(9)	(2)	(4)	(2)	(2)	(2)	(0)
2	SEQTR	1100	0100	0001	0111	1111	1010	1001	0010
		(C)	(4)	(1)	(7)	(F)	(A)	(9)	(2)
3	SEQTR	0100	1001	0010	0100	1001	0010	0101	0010
		(4)	(9)	(2)	(4)	(9)	(2)	(5)	(2)
4	SEQTR	0000	1001	1111	1100	1000	1100	1001	0011
		(0)	(9)	(F)	(C)	(8)	(C)	(9)	(3)
5	SEQTR	1010	0001	0011	1111	1111	1000	0000	0010
		(A)	(1)	(3)	(F)	(F)	(8)	(0)	(2)
6	SEQTR	0100	1001	0010	0100	1000	0100	0010	0100
		(4)	(9)	(2)	(4)	(8)	(4)	(2)	(4)
7	SEQTR	1110	0101	0010	1101	0101	0010	1010	1001
		(E)	(5)	(2)	D)	(5)	(2)	(A)	(9)
8	SEQTR	1111	1111	1011	1110	1101	1111	1110	1011
		(F)	(F)	(B)	(E)	(D)	(F)	(E)	(B)

Delay 100 clock cycles before trace
Trigger condition begins trace
Analyzer captures data on rising edge of clock

show only the proper input sequences. In this form of testing, the Don't Care terms that are used in the generation of the logical sum of products will also cause PLA outputs. These sequences must be taken into account when evaluating the test. If errors are present in the PLA, the stored sequences will be incorrect. By comparing captured data with stored data, the incorrect sequences in the captured data can easily be highlighted on the PC screen for rapid check by the operator.

Integrating a dynamic test source and a logic analyzer with a PC forms a programmable low cost test system.

At the other end of the spectrum, PLAs with 10 inputs and 8 outputs will be tested using a different strategy. The 10 inputs require a 10-bit counter to generate 1024 input sequences. Most analyzers can store at least 1024 data sequences so connections can be made to the 10 inputs and 8 outputs. The output sequences will be compared to the input sequences to validate the integrity of the logical design. Using the zero hold feature and taking data on the 0-1 clock transitions results in synchronized input and output sequences. Thus, the input and output data will line up on the display. Again, the captured data from a device under test can be compared with stored data. The differences can be highlighted to the operator or stored for subsequent printout.

The PLA that has flipflops as an integral part of the devices must be tested differently because both combinational AND/OR logic and clocked flipflop outputs must be evaluated. In addition, these PLA structures offer Hi-Z output capabilities and this must be taken into account during testing.

Typical 20-pin PLAs such as the PAL-16R6 from Monolithic Memories have a clock input and 8 data inputs. A third input is used to provide a control for the three-state outputs. The Hi-Z control for the combinational outputs is provided by correctly programming the internal PLA. With only 8 inputs, the generation of input sequences can be generated with an 8-bit counter. To test a device, eight of the data lines from the logic analyzer are connected to the input lines and the outputs from the PLA connected to other analyzer data lines.

The 0-1 clock transitions that drive the PLA flipflops are selected to drive the data into the logic analyzer. Because of the delay through the PLA flipflops, the flipflop outputs will be delayed from the input sequences by one clock cycle while the combinational outputs exhibit no delay. The combinational logic and flipflop Hi-Z outputs will be interpreted as logical by the logic analyzer.

In addition to testing the actual devices, digital systems that use PLAs can also be tested. Here, the actual inputs that drive the PLA will be monitored along with the outputs. Any deviations can quickly be identified and the bad PLA replaced. This type of testing is important in manufacturing as the integrated circuit components are assembled into systems.

In maintenance, PLA testing allows the technician to quickly locate and replace defective units.

The difference between ROM and PLA structures is two-fold. First, ROM structures have an input consisting of an address and an output consisting of data. PLA on the other hand has inputs and outputs with little, if any, reference to address and data lines. The density of the PLAs is thus typically less. A similarity exists when ROMs that have AND-TIE/OR-TIE structures are utilized to implement logical sums of products. A second and important difference is speed. PLA now operates with delays down to 25 ns, while ROMs typically have delay times greater than 100 ns.

Testing ROMs

Today only the most high volume designs use mask programmed ROM; most ROM is programmable on in-house programming systems. PROM, ROM, and erasable PROM memories can all be tested as follows. Given the address (input) and data (output) structure of ROMs the testing is carried out somewhat differently than that for PLAs. For the number of address lines equal to or less than 1024, the address sequence fits into the storage range of most personal computer-based logic analyzers. The testing of these devices is then done by connecting the logic analyzer data lines to the ROM address and data lines. The ROM inputs (the address lines) are excited by a 10-bit counter and the ROM function can quickly be tested by comparing the sequences on the address lines and the data lines.

For ROMs with more than 10 address lines, the testing must be sequential in nature. For example, with a 32-K x 8-bit ROM, we have 15 address lines and 8 data lines. This means we have $2^{15} = 32 \times 1024$ sequences. In terms of a logic analyzer with the capability of capturing 1024 data points, we must capture 32 sequences to fully test a ROM. In practice, the transfer of data from the logic analyzer to the personal computer main memory can be done at bus speeds, but the transfer of the data to a floppy disk is time consuming. For total testing, we want to use main memory to store the data. This will optimize testing speed.

For testing, a 15-bit counter can again be used with 1024 sequences being captured at a time. Capturing data from the 15 address lines and the 8 data lines requires connection of 23 data lines into the logic analyzer. Each sequence requires 3 bytes of information in main memory resulting in a requirement of 96 Kbytes of main memory to store the data from one test. The system is sequenced by first activating the address lines. A_0 through A_9 from a high speed counter with lines A_{10} through A_{14} held at a logical zero. The counter is then stopped while the captured data is transferred to the personal computer main memory. Then the counter is activated for another 1024 counts, and this is repeated until all address lines have been dynamically driven. The stored data is then compared to known good data. These comparisons can be carried on in the background while the analyzer is capturing data. When the test is completed, only bad data values will be displayed to minimize the requirement for searching through massive amounts of data by the operator.

In these systems, a known sequence of microprocessor instructions are programmed into the ROM. Testing requires the capture of the sequences as they are generated from the microprocessor program counter. If the ROM sequences are found to be correct, the operation of the microprocessor can be tested by following the execution of the ROM stored instruction. This requires monitoring of the conditions causing branches to occur so that branch conditions can be traced through program execution.

The ROM-driven microprocessor forms the heart of many systems and the testing of the ROM and microprocessor operation is a first step in determining the valid operation of the system. After these components are tested, outboard support integrated circuits will require that a test strategy be designed so that the total system can be tested. This is desirable for self-contained board level products, printed circuit boards, subsystems, and finally, total systems.

PCs offer flexibility

Designing testable digital systems is currently of great concern. No precedent has been set and in many cases testing is not an important part of the design process. In the future more emphasis must be placed on both static and dynamic testing. Static testing will involve testing for shorts and opens, while dynamic testing will focus on testing for valid system operation of actual clock rates.

An important aspect of the design will be consideration of the type of instrumentation that will be used for testing during design, manufacturing, and maintenance. Successful test methods will probably result in similar instrumentation being employed at all three levels and because of their flexibility and ease of use, PC-based instruments have great potential for being integrated into test strategies.

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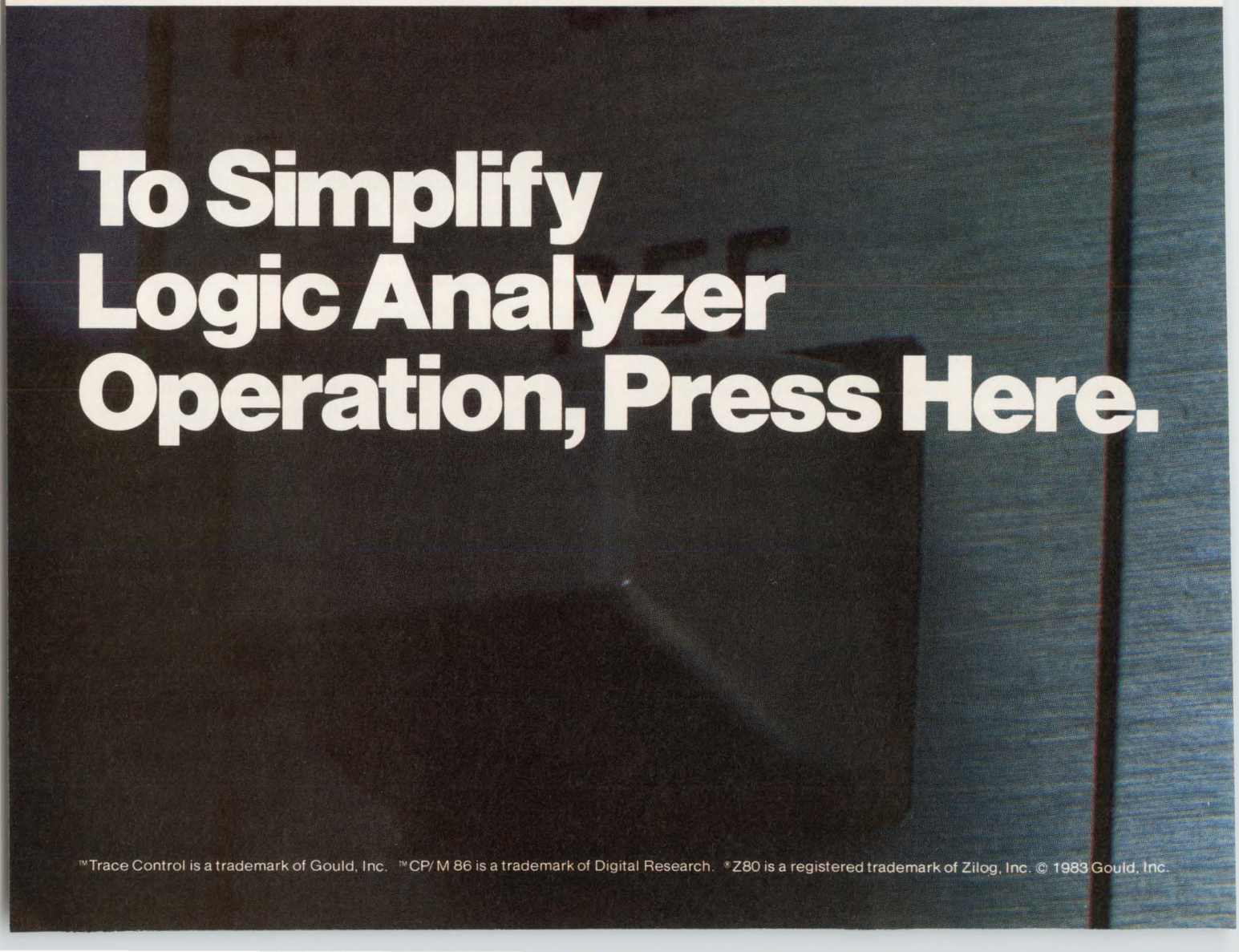

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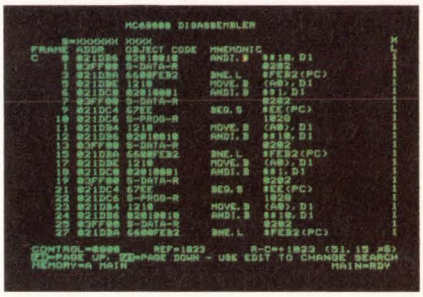

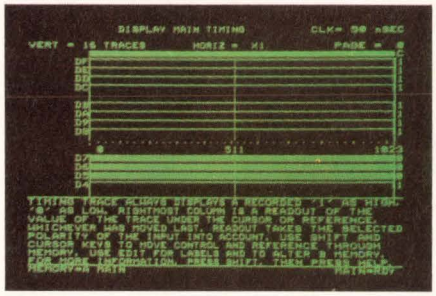

The K105 offers you two levels of HELP at the press of a button. The first displays step-by-step operating instructions across the bottom of the analyzer screen. The second brings a menu to the screen, allowing you to select more detailed help from an integral 28-page manual.

CIRCLE 47

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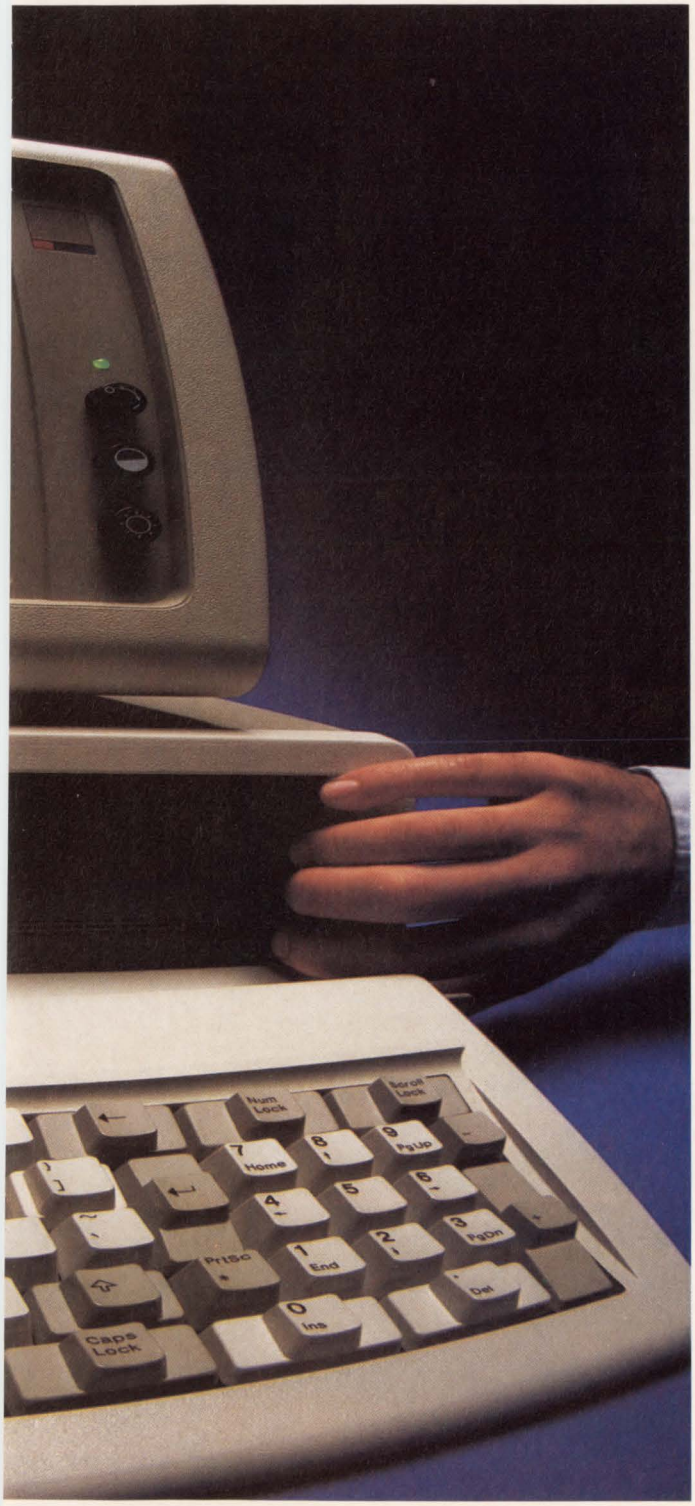

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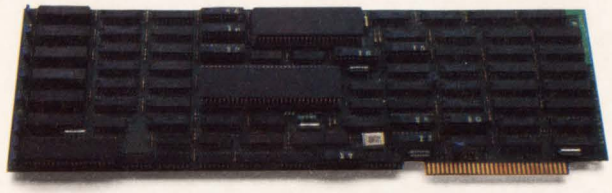

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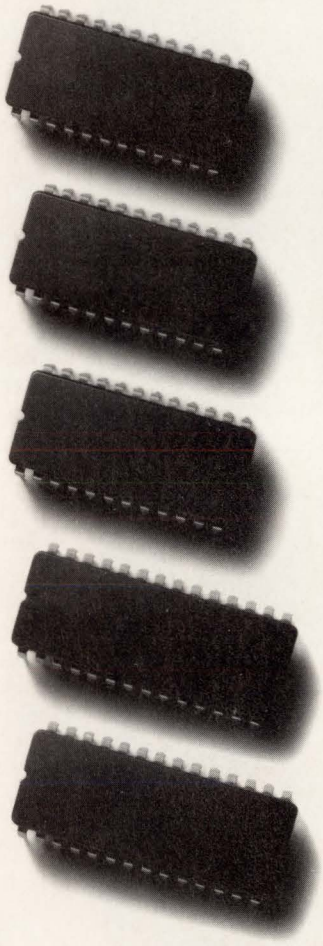
While everyone quit at 5,



2K x 8 latched

2K x 8 latched timer,
2816A compatible

2K x 8 latched,
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8K x 8 latched timer

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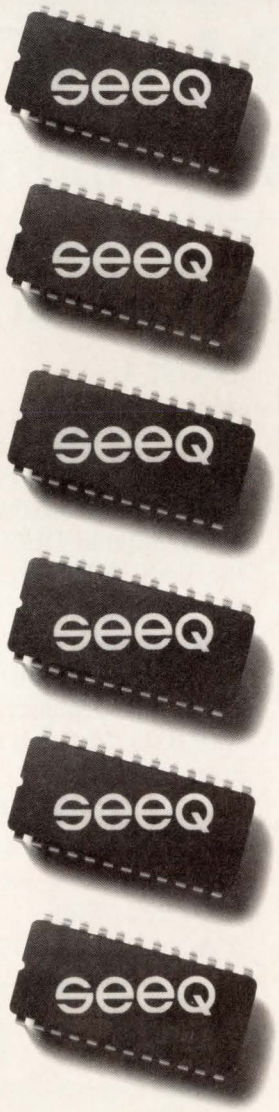


2K x 8 latched

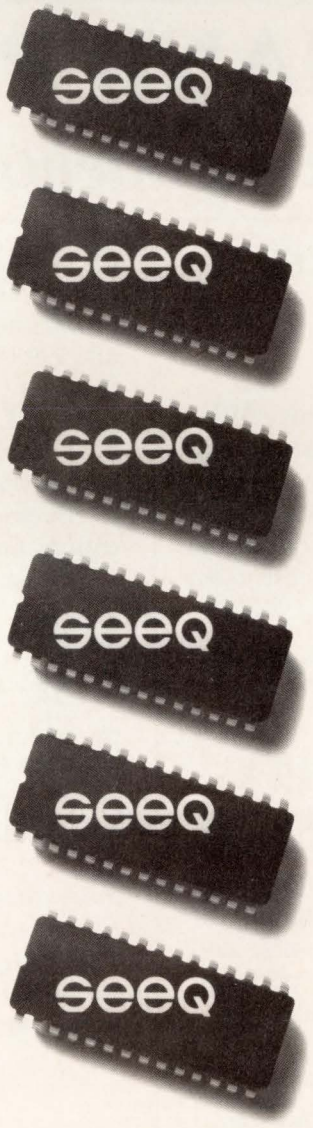
2K x 8 latched, 1ms write

2K x 8 latched timer, 2ms write

2K x 8 latched timer, 1M cycle endurance

2K x 8 latched, full military temp.

2K x 8 latched, 2816A compatible



8K x 8 latched

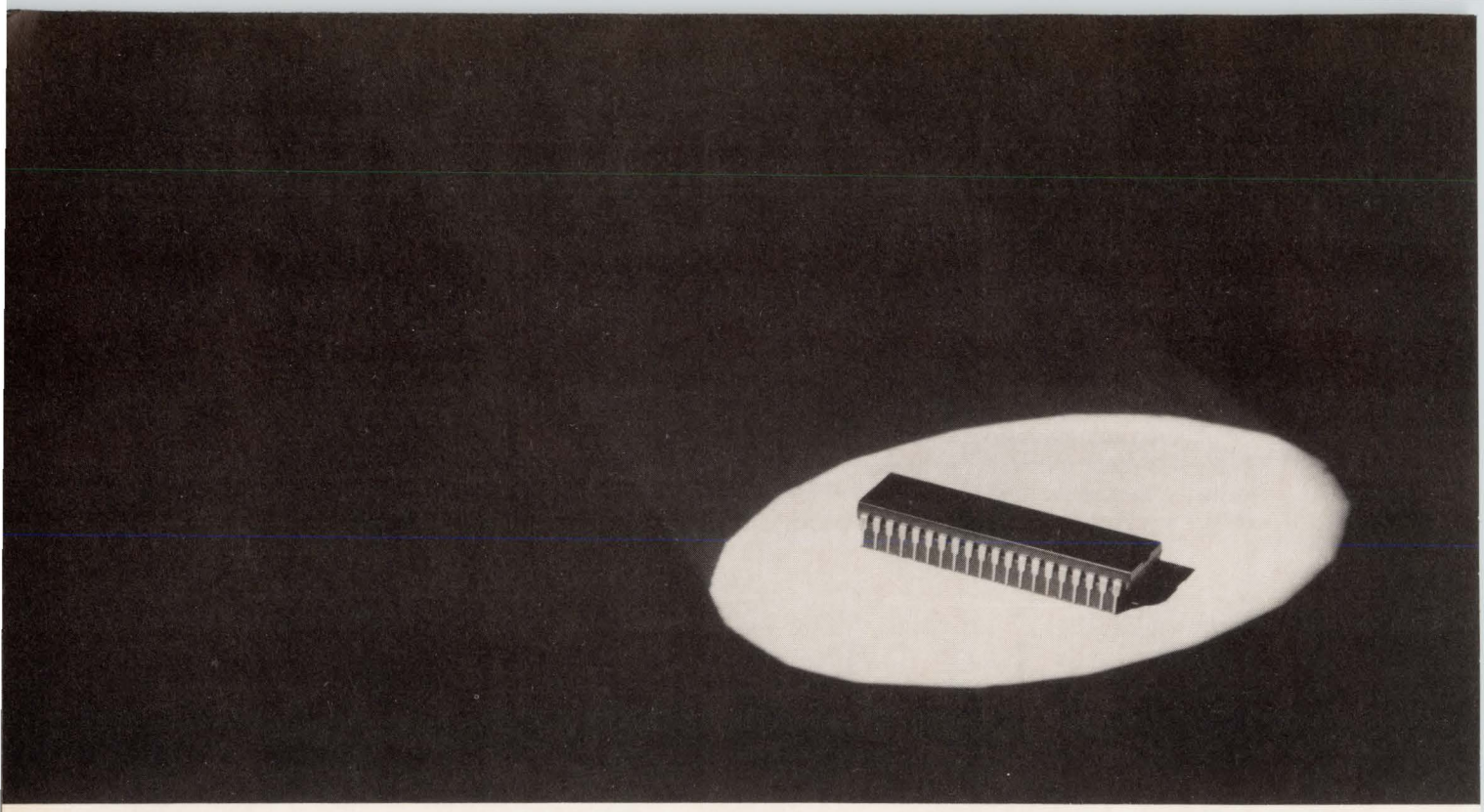
8K x 8 latched, 1ms write

8K x 8 latched, full military temp.

2K x 8 latched timer, 2817A compatible

2K x 8 latched timer, 2817A w/1M cycle endurance

8K x 8 latched, 1ms write, full military temp., 1M cycle endurance



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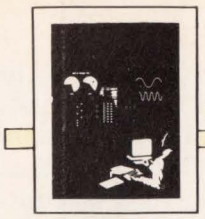

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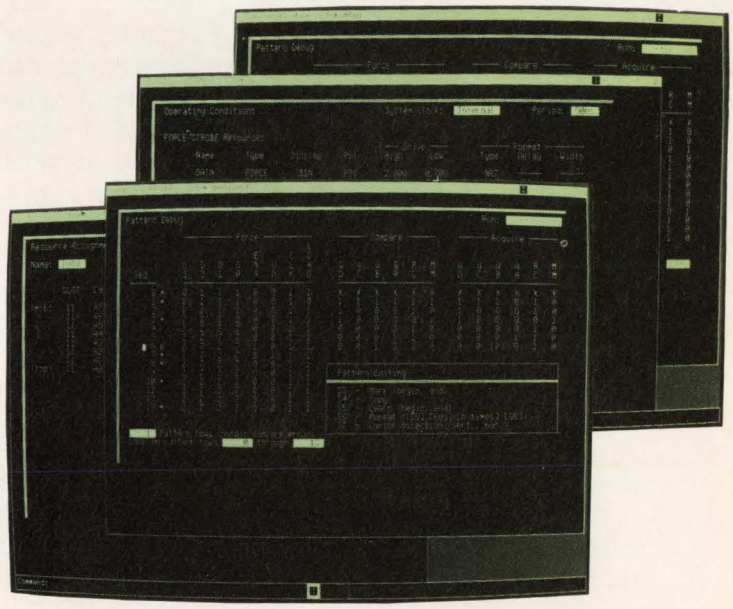

by Gerd Hoeren, Jerry Sewell, and Mike Connell

The rapid proliferation of computer aided circuit engineering tools is having a substantial impact on the way semicustom ICs are designed and tested. As circuitry once destined for board-level implementation descends to the IC level, engineers must use new methods for testing and verification. At the same time, CAE tools such as simulation allow the testing of complex circuitry before the design is realized physically. But, most IC test system interfaces bear little or no relation to the sophisticated interfaces associated with CAE tools.

Traditionally, engineers have had two choices regarding IC testing. One has been to use an automated test equipment (ATE) system such as those used by semiconductor manufacturers. These million-dollar systems use special test system languages that require months of operator training. The other choice has been to create an "instrument cluster" based on the IEEE 488 General Purpose Interface Bus (GPIB) standard. This approach involves relatively extensive system development, performance trade-offs, and complicated human interfaces.

A test system from Integrated Measurement Systems—Logic Master—uses an interactive, full-screen interface, and a simple command language to implement control of the test hardware. The system supports the initial development of test vectors, control over test hardware, debugging of test vectors, and interpretation of test results. A mainframe contains a pattern generator, data acquisition/comparison modules, and a realtime interface between these entities. It also includes a controller unit that governs system operation with an RS-232 or GPIB host computer. This host can be an IBM PC or XT or any other controller (Fig 1). The verification station provides a controlled impedance fixture to the device under test.

In operation, the system accepts a set of test vectors from the host computer. These vectors can come

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Mike Connell is a software designer at IMS. He holds a BS in electrical engineering.

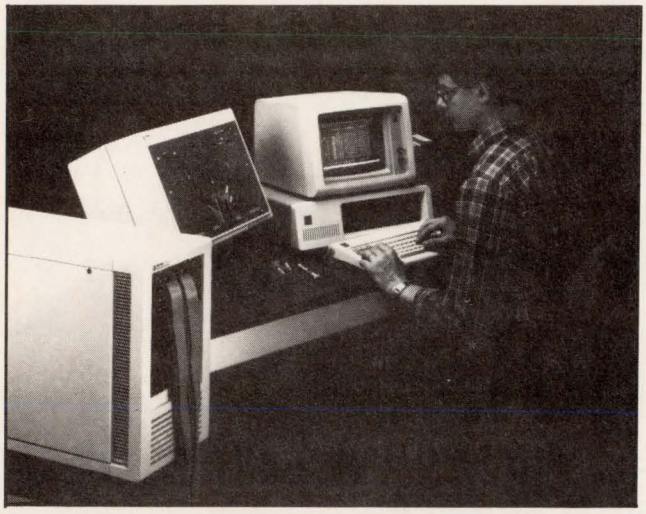

Fig 1 The Logic Master Series of functional testers puts integrated stimulation, acquisition, and realtime comparison into the hands of the IC designer already using the IBM PC.

from a CAE simulator program or any other source. The system also includes a pattern file translator to ease vector transfer from the CAE simulator to the test system hardware. Each vector consists of stimulus bits and comparison bits, and can be downloaded into the unit's pattern generator and realtime comparison memories.

When a test is run, the pattern generator inputs stimulus patterns to the prototype IC being tested. A second realtime comparison module provides the comparison data, which is then compared with the acquired output of the test device. If the comparison is false, the bit is flagged to show a discrepancy and stored. In addition, a special high speed bus connects the pattern generator and acquisition/comparison modules, allowing the pattern generator to jump within the vector space. However, this depends on the outcome of the acquisition/comparison process.

Full-screen interface simplifies operation

A major requirement for a test system operating in a CAE-based design environment is human interface. This interface must be easily understood by engineers who are experts in circuit design, but not in IC test procedures. Most large systems and instrument clusters have interfaces requiring complex command strings. This approach may be best for a production test environment where engineers have constant daily exposure to the interface command set, but it is inefficient in a design situation where the test interface is just one of many engineering tools.

Logic Master simplifies many test operations by giving the designer a full-screen, interactive interface. This allows modification of the test system parameters and test vectors in real time, without intermediate processing by the host computer. During operations such as test pattern debugging, this interactivity can save substantial amounts of time.

The best way to demonstrate this interface is to implement a typical test sequence for an IC. First, a configuration screen shows the state of the system prior to the test. It displays what modules are located in what slots, and if they have passed their diagnostics. A quick summary of the setup appears at the bottom of the screen so the user can tell at a glance what the basic configuration of the system is.

Next, the relationships between the test channels, the probes, and the test device are defined. In most applications, the probe assignments break down into logical groups, such as the DATA group shown in Fig 2. Two separate but corresponding representations are used to easily verify or change the resource channel to device pin assignments. The area on the left uses a table with parallel columns to show how input and output channels relate to device pin names and numbers. The area on the right uses a symbolic representation of the device to display the pin names and numbers in their actual chip locations. This test fixture schematic allows immediate and accurate wiring of the verification station. At the same time, it allows easy identification of input and output channels. Any of the displayed information can be modified through simple cursor-oriented editing.

Fig 3 shows how all the channel resources come together to form the overall test setup. The group DATA, for example, is at the top of the list under the FORCE/STROBE resources. This category

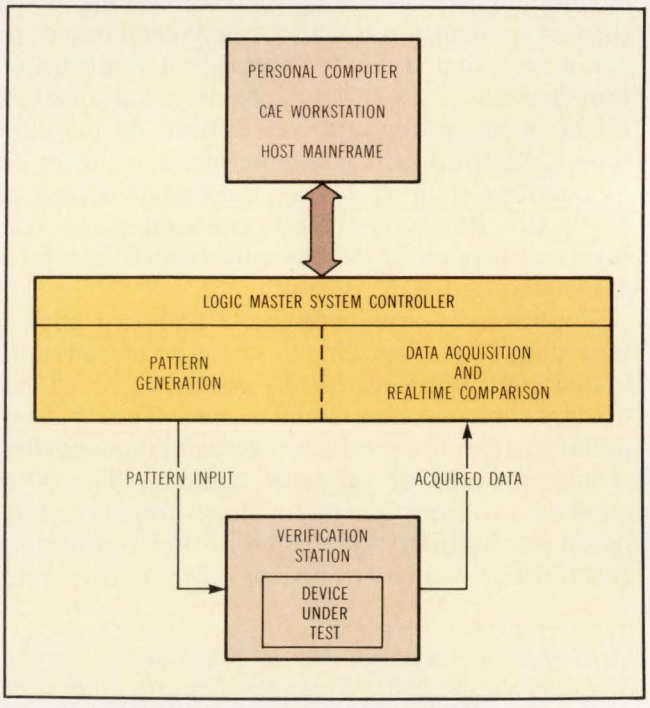

Fig 2 Integrated Measurement System's Logic Master includes a system controller, a pattern generator, and data acquisition/comparison modules. Test vectors are downloaded to the pattern generator and realtime comparison memories. The pattern generator inputs patterns to the test device, and the acquired data is compared by the comparison modules.

comprises the data used by the pattern generator. Notice that the DATA channels have both a delay and pulse width associated with them. These parameters can be controlled in increments down to a 1-ns delay and a 10-ns pulse width. They define the behavior of these channels relative to the test cycle. In this example, the test cycle is set at 50 ns.

At this point, the pattern file produced by the CAE system's logic simulator can be downloaded. Through simple editing, the file has been converted to the intermediate format used by the Pattern File Translator. All that remains to complete the translation and download is the entry of a single function key that downloads the pattern file.

Debugging test patterns in real time

Once the pattern is translated and downloaded, it must be debugged. This is the most demanding phase of the test operation. No matter how well a simulator performs, it is impossible to predict the exact conditions of the actual prototype. For instance, even slight variations in process parameters can result in timing skews that were absent during simulation.

Batch processing, as performed on large test systems, has been the traditional approach to test pattern debugging. Once the test pattern has been developed on the system's host computer, it is compiled into a form usable by the test hardware, downloaded, and executed in its entirety. The resulting data is then uploaded to the host computer and output to a printer. To correct an error, the pattern file must be reaccessed, modified, recompiled, and then downloaded to the test hardware again.

The IMS system shortens this process by allowing realtime interactive pattern debugging. Once the pattern is downloaded into the system's test hardware, all debug operations can occur locally. As indicated at the bottom of this realtime debugging display (Fig 4), the pattern has been set to loop on rows 0 to 13 instead of running through the entire pattern depth. This allows the pattern to be debugged in manageable sections. The other line at the bottom of the display reports the total number of comparison errors encountered; in this case, one. The error's location is identified by an "e" next to the line number (see line 6). The actual error is marked by parentheses in the ACQUIRE column.

The test system interface is designed to make the development of test and verification procedures as simple and straightforward as possible. Realtime, interactive control through a graphics-oriented interface makes the test system as easy to use as any other design automation tool in a CAE environment.

In theory, the test vectors used by CAE simulators should be a valuable resource in generating vectors to be used during IC testing. However, the

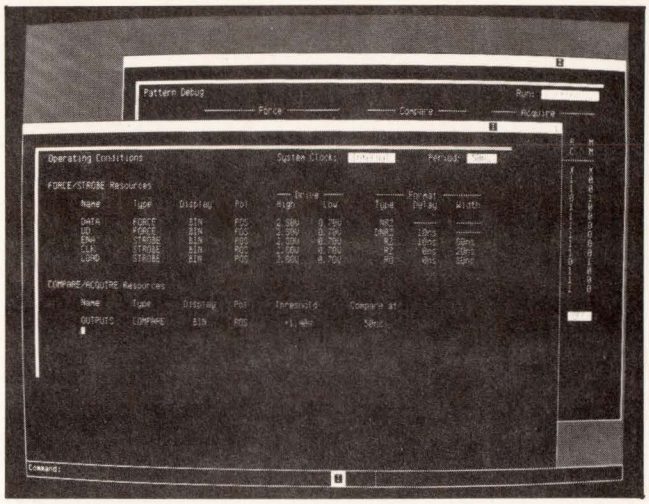

Fig 3 This screen shows how channel resources merge to form the overall test setup. The FORCE/STROBE resources are data used by the pattern generator.

vectors used during simulation are not directly transferable to the test system. This incompatibility is the product of three differences between simulators and test systems: timing, data formatting, and assignment of simulator data to physical pins.

A simulator, working with a software-based model of the actual circuit, samples circuit responses in unit time steps. These "units" are usually interpreted as nanoseconds. This amount of resolution on a continuous basis is not available on any test system. To achieve 1-ns resolution when testing a part, most test systems use programmable strobes and formats that are set to specific delay and width values prior to test execution. Based on these programmed delays, the cycle times of the simulator must be converted to test sequences in the tester memory. However, these sequences are limited to the maximum clock rate of the test system when the pattern is executed. Also, many simulators only display data when a

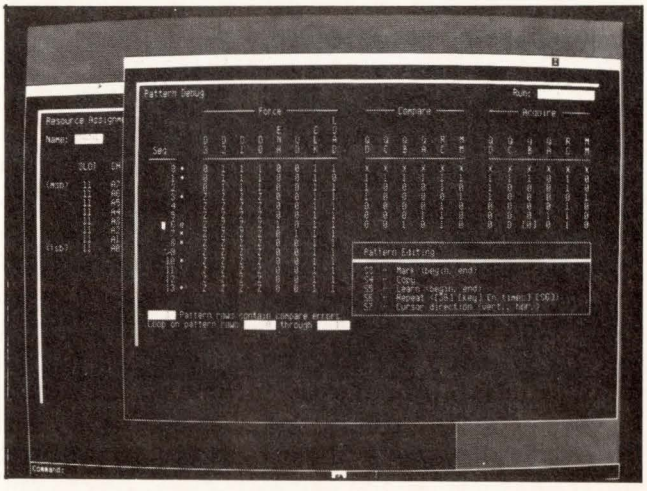

Fig 4 This realtime debugging display shows a portion of the pattern file with acquired data and comparison data. There is one comparison error on line 6.

TABLE 1

Pattern File Conversion

Simulator Data Capture File					Logic Master Pattern Sequences				
Time	Inputs		Outputs		Sequence	Force		Compare	
(ns)	IN 1	IN 2	OUT 1	OUT 2		IN 1	IN 2	OUT 1	OUT 2
0	0	0	0	0	1	0	0	X	X
10	0	0	1	0					
30	0	1	1	0					
50	1	1	1	0	2	1	1	1	0
80	1	0	1	1					
100	1	0	1	1	3	1	0	1	1
200	1	1	0	0	4	1	1	1	1
230	1	1	0	1					
250					5	1	1	0	1
300					6	1	1	0	1
350	1	1	1	0	7	1	1	0	1
400	0	0	0	0	8	0	0	1	0

pattern change occurs, and this change does not occur on a cycle-by-cycle basis. For the test pattern to accurately represent the simulator pattern, all of the above timing factors must be handled during the conversion process.

Table 1 shows a pattern file as it might be output from a simulator, and the resultant test vectors that would be derived from conversion to sequences in the Logic Master pattern memory. In this example, the inputs to the part are programmed to a nonreturn to zero (NRZ) format where the data changes at the start of the cycle and remains at the programmed level throughout the cycle. The part's outputs are to be sampled by the comparison strobes at 40 ns into the cycle. The clock rate of the simulation was 20 MHz, corresponding to a 50-ns cycle time. Each 50-ns period, the conversion program will load a new sequence, based on the NRZ format and the 40-ns comparison strobe, into the test system pattern and comparison memories. Note that between 230 and 300 ns there was no change in the simulator data.

Conversion and compatibility

Logic Master still loads the last vector into sequences that correspond to 250 and 300 ns to preserve the timing integrity of the test. The data loaded into the comparison is the last output value at or before 40 ns into the cycle. The first cycle loads comparison mask values (Xs) into the comparison memory since there is no data for time preceding zero.

The second compatibility difference between simulators and the test system is in file structure. Logic Master's convert file format is similar to the tabular outputs of most simulators, facilitating conversion in the host system editor. Special convert command directives allow the differences in pattern presentation to be handled with minimal typing. An example of this is a directive that tells the Logic Master to translate all U values in the simulator file into Xs to load into memory. Table 2 shows a typical simulator output file and the corresponding convert file format. The similarity of the these files illustrates the ease of format conversion.

The final conversion problem is the ordering of data in the pattern file so that it is loaded into the correct channel in the test system. Logic Master will load its force and compare memory from the conversion file in the order it appears on the pattern debug screen. Users must reorder the display to match the order of the file to be converted, before activating the conversion process. After the file is loaded into

TABLE 2

Simulator Output File Translation

Typical Simulator Output File

	D 3	D 2	D 1	D 0	N A	U D	A D	C L	Q A	Q B	Q C	Q D	R C	M M
0	0	1	1	1	1	1	1	0	U	U	U	U	U	U
10	0	1	1	1	0	0	1	1	U	U	U	U	U	U
20	0	1	1	1	0	0	0	1	0	1	1	1	1	0
30	0	1	1	1	0	0	0	0	0	1	1	1	1	0
40	0	1	1	1	0	0	1	0	0	1	1	1	1	0
50	0	1	1	1	0	0	1	1	1	0	0	0	1	0
70	0	1	1	1	0	0	1	0	1	0	0	0	1	0
80	Z	Z	Z	Z	0	0	1	0	1	0	0	0	1	0
90	Z	Z	Z	Z	0	0	1	1	1	0	0	1	1	1
110	Z	Z	Z	Z	0	0	1	0	1	0	0	1	0	1
130	Z	Z	Z	Z	0	0	1	1	0	0	0	0	1	0
150	Z	Z	Z	Z	0	0	1	0	0	0	0	0	1	0

Reformatted Simulator File in Logic Master

Define U = X
Units = 1 ns

0	0	1	1	1	1	1	1	0	U	U	U	U	U	U
10	0	1	1	1	0	0	1	1	U	U	U	U	U	U
20	0	1	1	1	0	0	0	1	0	1	1	1	1	0
30	0	1	1	1	0	0	0	0	0	1	1	1	1	0
40	0	1	1	1	0	0	1	0	0	1	1	1	1	0
50	0	1	1	1	0	0	1	1	1	0	0	0	1	0
70	0	1	1	1	0	0	1	0	1	0	0	0	1	0
80	Z	Z	Z	Z	0	0	1	0	1	0	0	0	1	0
90	Z	Z	Z	Z	0	0	1	1	1	0	0	1	1	1
110	Z	Z	Z	Z	0	0	1	0	1	0	0	1	0	1
130	Z	Z	Z	Z	0	0	1	1	0	0	0	0	1	0
150	Z	Z	Z	Z	0	0	1	0	0	0	0	0	1	0

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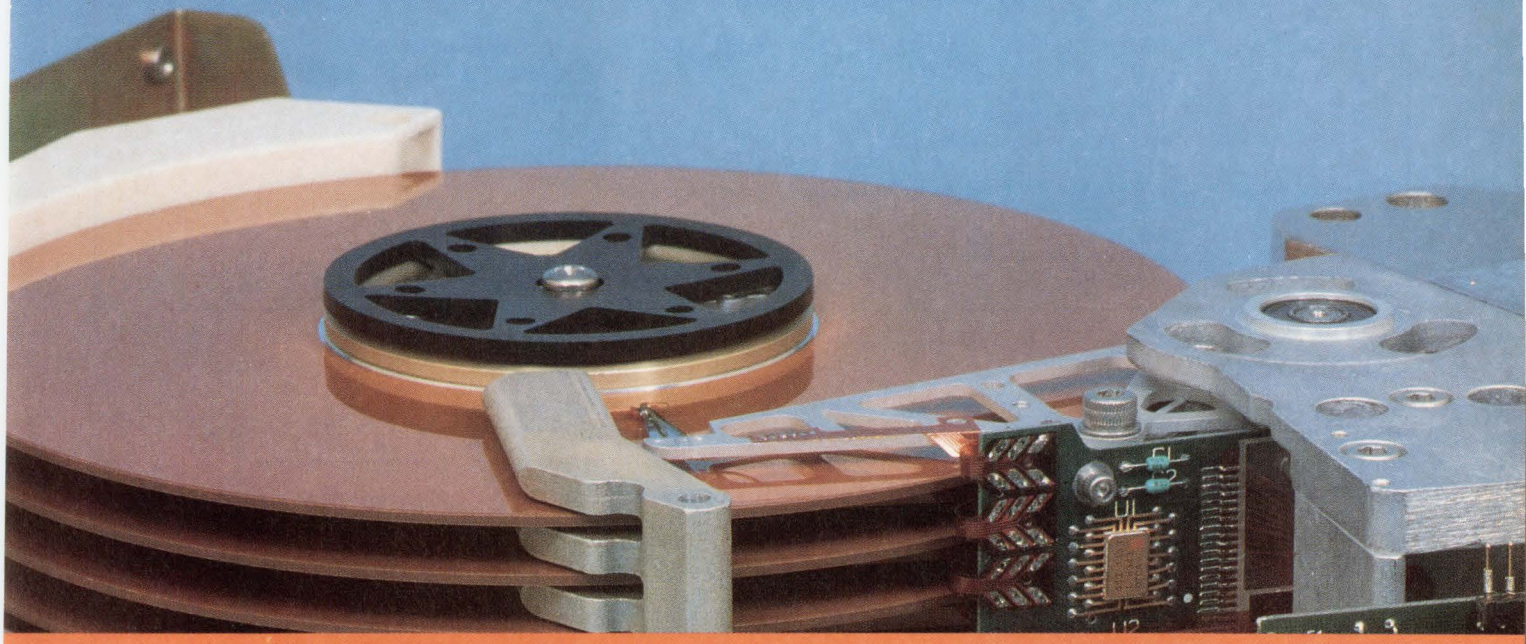

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TABLE 3

Sample Test Program

```
100 REM *** Prepare the Logic Master to receive the setup file
110 REM ***
120 OPEN "COM1:9600" AS #1                          ' Use 9600 baud RS-232
130 OPEN "SETUP.IMS" FOR INPUT AS FILE #2           ' Open setup and pattern file
140 WHILE NOT EOF(2)
150   INPUT #2, L$                                  ' Read one line from setup file
160   PRINT #1, L$                                  ' Send line to Logic Master
170 WEND
180 REM *** Prompt operator to insert device and start the test
190 REM ***
200 INPUT "Insert Part and press RETURN", A$
210 FOR DELAY = 10 TO 40 STEP 1
220   REM *** Vary the Logic Master compare time from 10 ns to 40 ns
230   REM *** from the start of each clock cycle.
240   PRINT #1, "compare data="; DELAY; "ns"
350   PRINT #1, "start all"                         ' Begin the test
360   PRINT #1, "fail?"                             ' Query number of errors
370   INPUT #1, FAIL$                               ' Read response from Logic Master
380   IF FAIL$ <> "FAIL 0" THEN 440                 ' Terminate test if part failed
390 NEXT DELAY
400 PRINT "Device Passed"
410 GOTO 200
420 REM *** Print delay value where the device failed
430 REM ***
440 PRINT "Device failed at "; DELAY; "ns"
450 GOTO 200
460 END
```

Logic Master, ordering may be changed as desired for display during testing.

Thus, Logic Master supports the downloading of files from simulators with minimal user effort. This gives designers an immediately available test program that evaluates the simulated functionality of prototype parts. The conversion process can also be reversed to return the file to the simulators. This allows the simulation to be rerun with the actual vector data presented to the part. It can also serve as an interactive feedback loop to resolve problems with models, or to compare actual behavior to expected behavior in the simulator.

Algorithmic control of system tools

Logic Master provides a command language interface that supports the screen interface's measurement capabilities and allows algorithmic control of system resources. Since Logic Master is host independent, the IMS Command Language consists of directives that describe testing resources and setup parameters in simple English statements. These commands are embedded as input and output parameters or as files in any programming language. This allows designers to use their own tools, such as editors and compilers.

The commands can be used in conjunction with or completely separate from the screen interface. Several test situations are best addressed by the command language interface and may not be possible with screens only. Iterative testing with one or more changing parameters, such as varying threshold or comparison time with successive test pattern executions, is easy to do. Other examples of command language uses are logging test results into a data base or prompting nontechnical operators in a production environment.

Table 3 is an example of a program using the IMS Command Language. Written in IBM PC Basic, the program prompts a nontechnical operator to insert a test device. (Basic statements are shown in upper case to differentiate them from IMS commands.) In this example, the setup and pattern parameters are sorted in the file SETUP.IMS. The program initializes Logic Master, downloads the SETUP.IMS file, then prompts the operator to insert a part and begin the test. The test repeats the pattern over the specified range of delay for the data output, and the number of errors are polled to determine if the device passed or failed the test.

This example illustrates the powerful operating environment created within Logic Master when the screen interface and command language are fully utilized. Testing a device is simplest using the directed procedure provided in the screen interface. Once the system is set up, and the desired test pattern is loaded and debugged, the complete setup and pattern can be saved for later use in the Command Language. The setup and test pattern can also be embedded in a program with other Command Language directives to do sophisticated iterative analysis and data logging.

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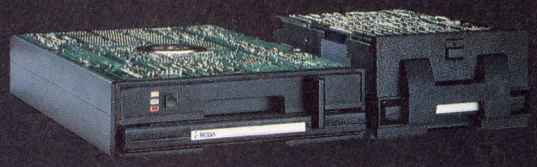

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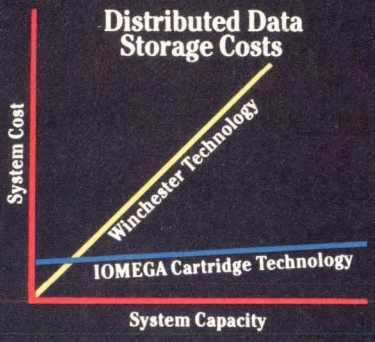
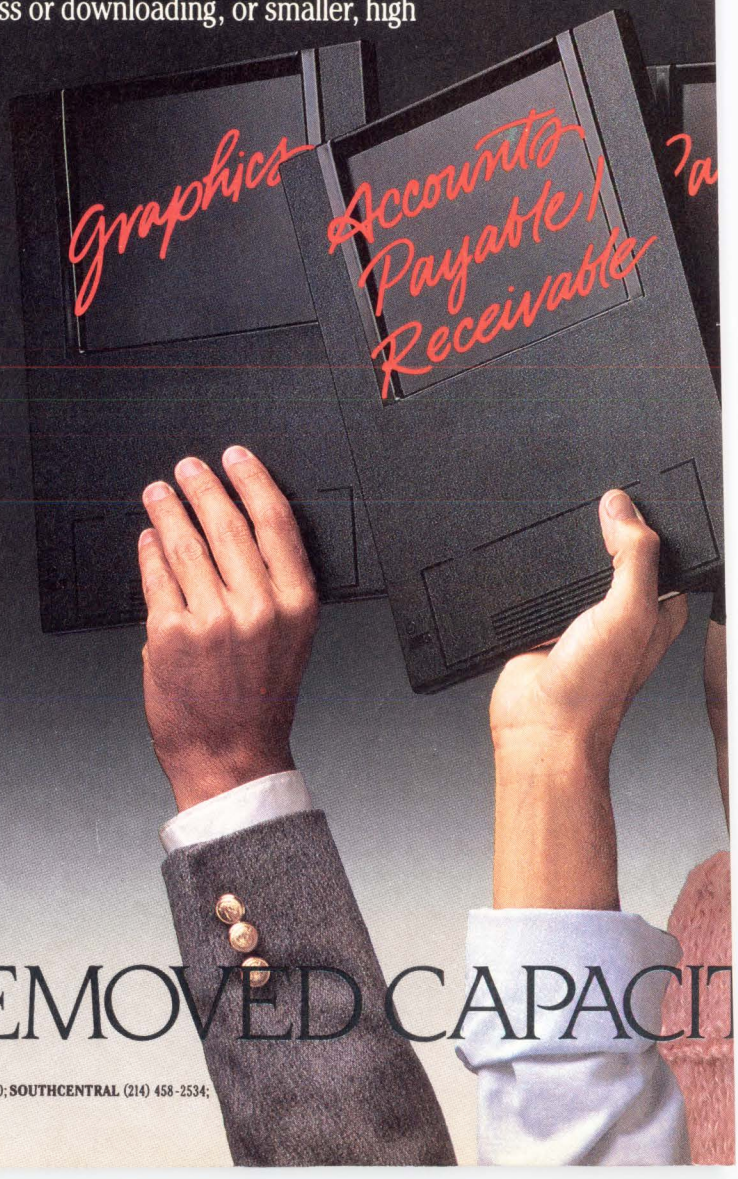


Slavery By Any Name . . .

There are lessons here. That the central issue isn't more data, but more data dynamics. And that Winchesters are hardly data dynamic at all.

Consider the aggravations of "wait your turn" access, or the need for lots of "system savvy" on the user's part. Consider the time consumed in backing up and restoring data. And consider the ever-present risk of a system going down or files lost to expensive head crashes.

Now consider the alternative.



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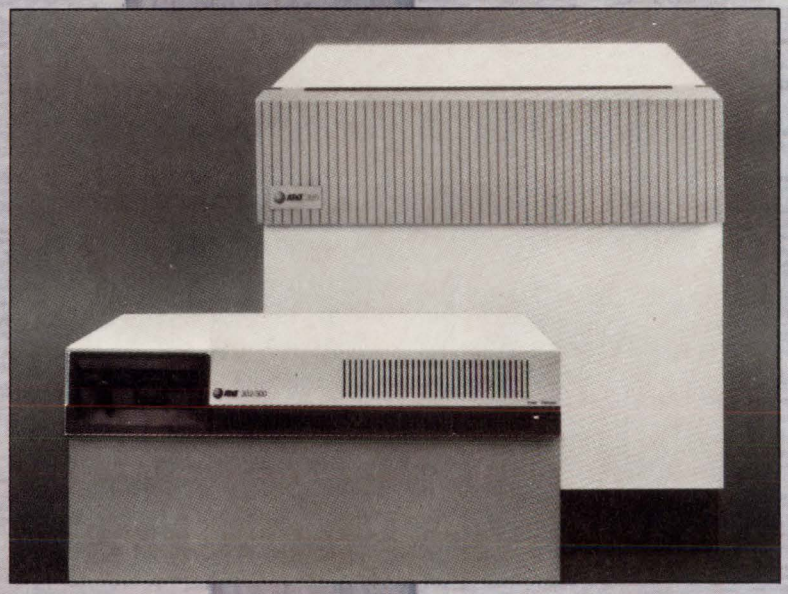

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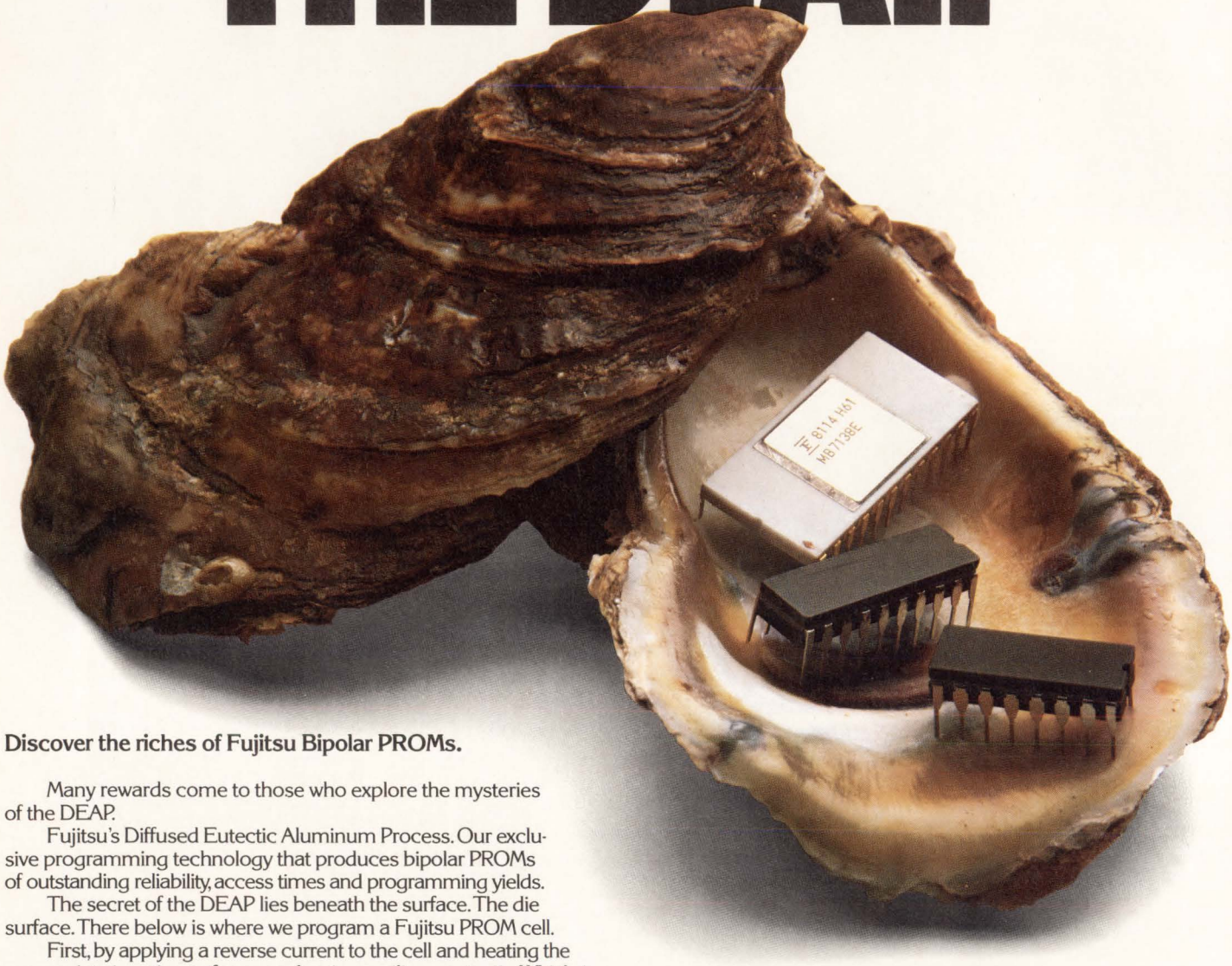

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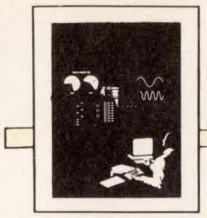
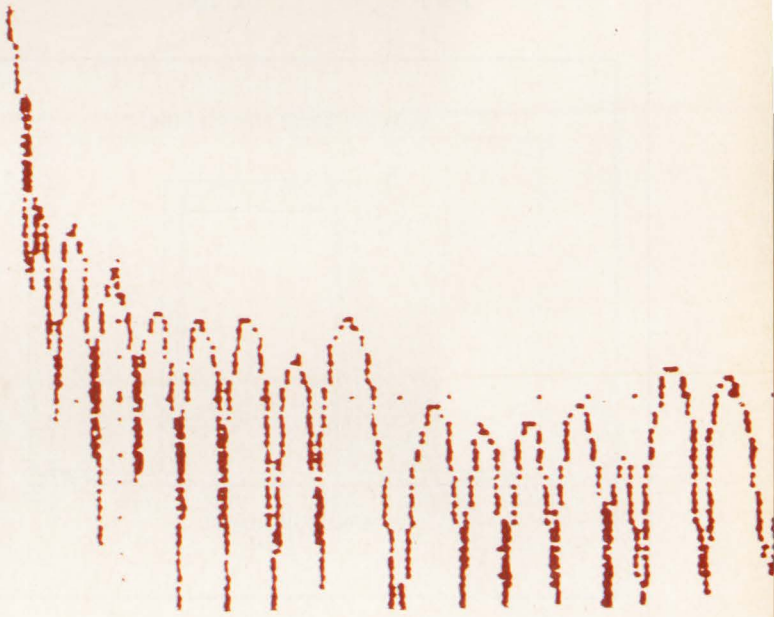


SOFTWARE PACKAGE BRINGS FILTER DESIGN TO PCs

A set of programs running on the PC lets designers implement a variety of filters using the TMS32010 digital signal processing chip.



by Ronald W. Schafer,
Russell M. Mersereau, and
Thomas P. Barnwell III

Several technological advances have come together recently to create a favorable climate for the cost-effective application of digital signal processing techniques using personal computer tools. First, the theory of digital signal processing has advanced to a high level. Second, integrated circuit technology provides an increasingly sophisticated selection of microcomputer chips and A-D/D-A chips for implementing digital signal processing algorithms. Finally, the same integrated circuit technology that has revolutionized digital signal processing applications has also led to an explosive growth in the use of personal computers. Now, inexpensive computer systems can provide the computational resources necessary for the development and testing of digital signal processing algorithms.

These three factors make it a virtual certainty that digital signal processing (DSP) methods will eventually dominate the design of electronic systems in areas such as communication systems (voice, data, and images), consumer electronics, medical electronics, and defense systems. Lack of widely available design tools, however, may be holding DSP back.

The design of DSP systems is fundamentally different from the design of analog systems. At the conceptual or block diagram level the two are much the same, but there are major differences at the circuit level. The analog designer must first decide upon a configuration including resistors, capacitors, op

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Russell M. Mersereau is a vice president of Atlanta Signal Processors, Inc. He holds a PhD in electrical engineering.

Thomas P. Barnwell III is a vice president of Atlanta Signal Processors, Inc. He holds a PhD in electrical engineering.

Digital filtering

One of the most common signal processing operations is linear filtering. The incoming analog waveform, denoted by x(t), is first passed through an analog low pass filter, known as an anti-aliasing filter. This filter removes all of the components in the incoming waveform at frequencies greater than one-half the sampling rate. The filtered waveform is then sampled by an A-D converter to produce a sequence of samples, x(nT), where T is the sampling clock period.

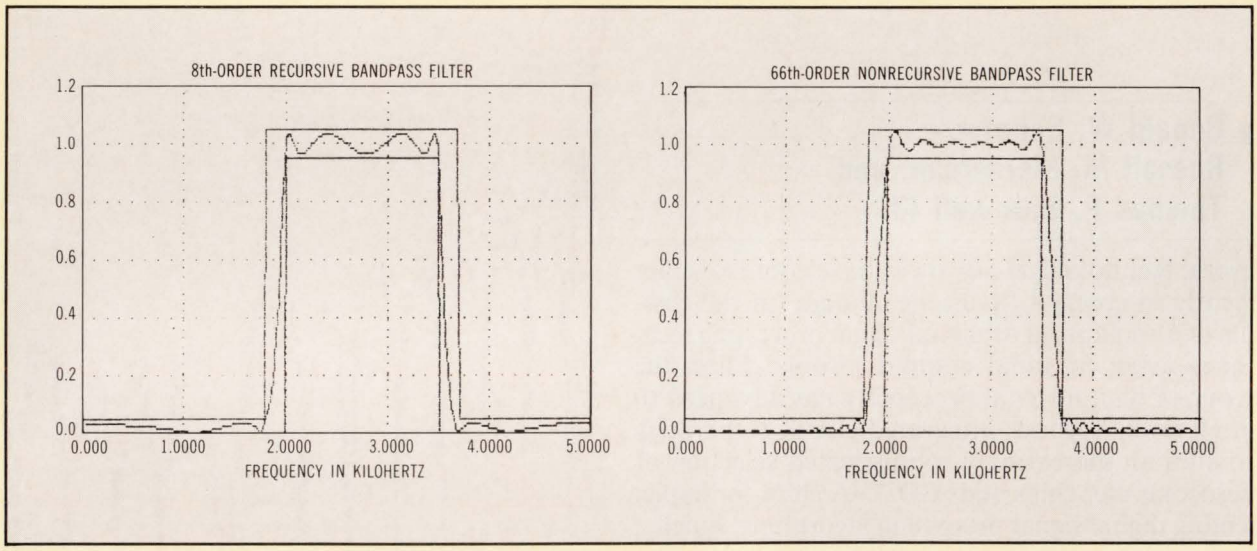
The output of the A-D converter can be operated upon numerically by a digital processor to produce another sequence, y(nT). The altered data from the output of the processor is then converted back into a continuous-time waveform by a D-A converter. The final analog low pass filter is required to compensate for the characteristics of most commercially available D-A converters.

Filtering of the signal can be accomplished by programming the digital processor to implement a difference equation of the form

$$y(nT) = \sum_{k=1}^{N} a_k y(nT - kT) + \sum_{k=0}^{M} b_k x(nT - kT).$$

Such discrete time systems have impulse responses that are theoretically of infinite duration; thus they are called infinite impulse response (IIR) systems. Such systems are also called recursive due to the feedback of output samples. If all of the a_k coefficients are zero, the system has a finite duration impulse response and the system is called a finite impulse response (FIR) system. Since there is no feedback of output samples, such systems are also called nonrecursive.

If a digital processor is used to implement the above difference equation, the frequency response of the overall system, including the analog filters, A-D, and D-A will depend on upon the coeffients of the difference equation. Therefore, the design of a digital filter is reduced to finding the coefficent sets a_k and b_k so a prescribed set of specifications is met. Shown below is the frequency response of an 8th-order recursive digital filter ($M = N = 8$) and a 66th-order nonrecursive filter ($N = 0$, $M = 66$), both of which meet the same set of design specifications (shown by the tolerance band). In general, IIR filters can be implemented with less computation (lower order) than FIR filters, but FIR filters can have linear phase response, which is often worth the extra computation.



amps, and comparators to accomplish a given signal processing function. Generally, such systems are designed hierarchically, wherein many subsystems connect to solve a given problem. The typical design engineer has few tools to help solve the impedance matching, dynamic range, and noise problems of such designs.

Designers of DSP-based systems will have two basic concerns when using current technology. These issues are the timing and noise problems in the design of a more or less standard configuration involving A-D, D-A, and microprocessor chips; and the programming of the microprocessor. Analog designers look at such problems and see only a few tools, such as cross assemblers, to help them write programs. These do not compensate for designers' lack of experience and intuition in designing the algorithms to be programmed, however. Fortunately, the required tools can be provided and the widespread availability of such tools will bring DSP techniques into the mainstream.

No matter how many tools are available, there is no substitute for a basic understanding of the properties of discrete systems. To consider DSP systems to be approximations to analog systems is an often-made mistake. Holding this view can often lead to designs that do not take full advantage of the powerful features of DSP. For example, the Fourier transform is primarily a theoretical analysis tool for analog signals and systems, but Fourier transforms

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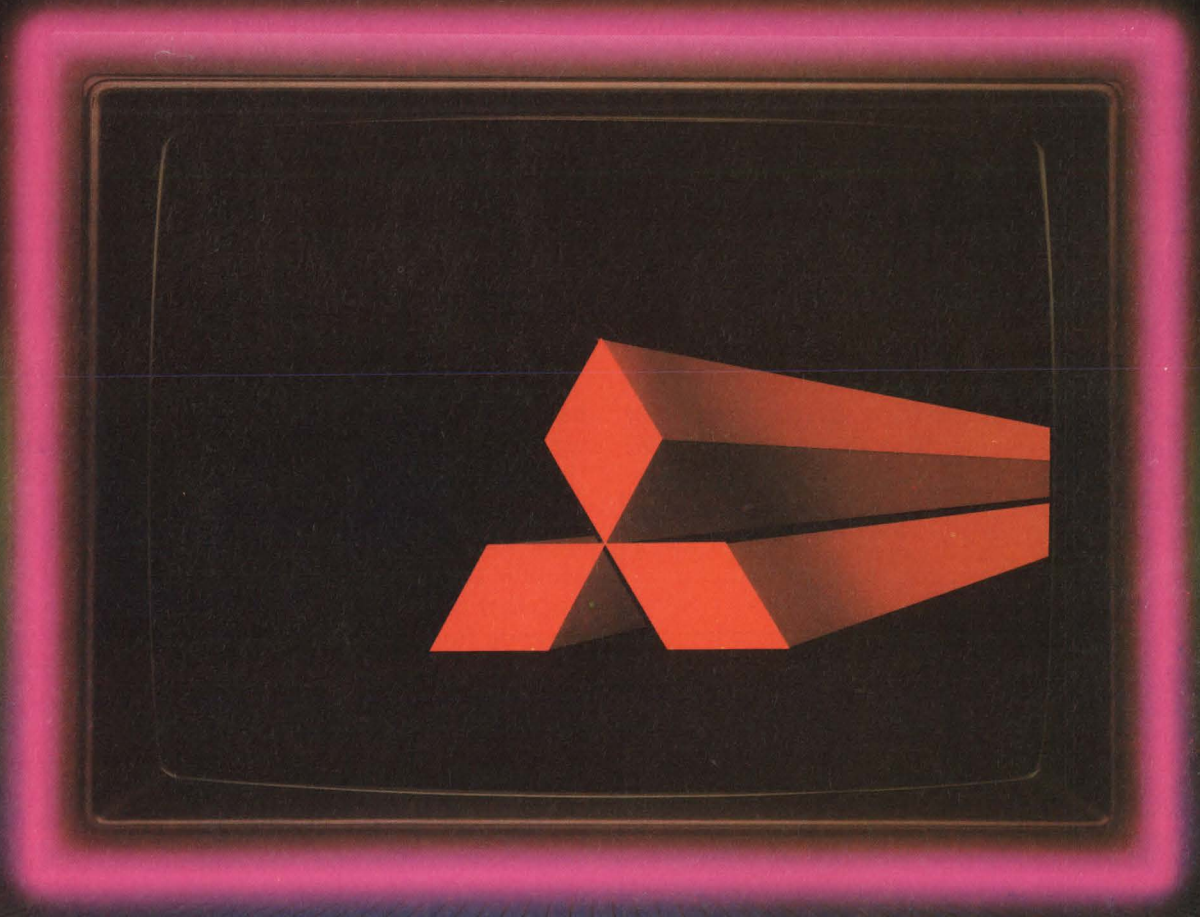

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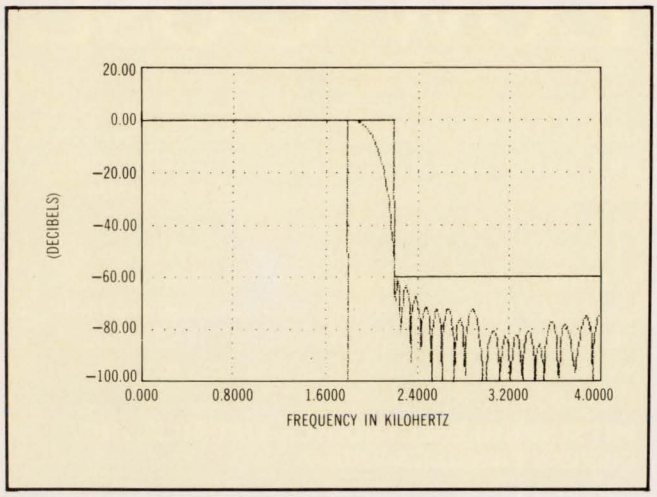


Fig 1 Frequency response of 75th-order linear phase nonrecursive low pass filter shows flat passband and 60 dB stopband attenuation.

of discrete signals actually can be computed. And they can be computed efficiently. The Fourier transform of discrete signals is similar to the continuous time Fourier transform, yet it is significantly different in a number of its important properties. To use discrete Fourier transforms to implement signal processing systems requires a basic understanding of the underlying mathematics of such transformations.

PCs and DSP design tools

Much of the research on DSP has involved the use of interactive hands-on computers with good interactive graphics for displaying signals and system response functions. This is particularly true of the current line of PCs. With appropriate software and A-D/ D-A capability, a PC can become a self-contained DSP laboratory for analyzing signals or simulating DSP systems. The PC can be used to carry out the design of digital filters and other DSP algorithms, and it can run cross assemblers for assembling code for DSP microcomputers.

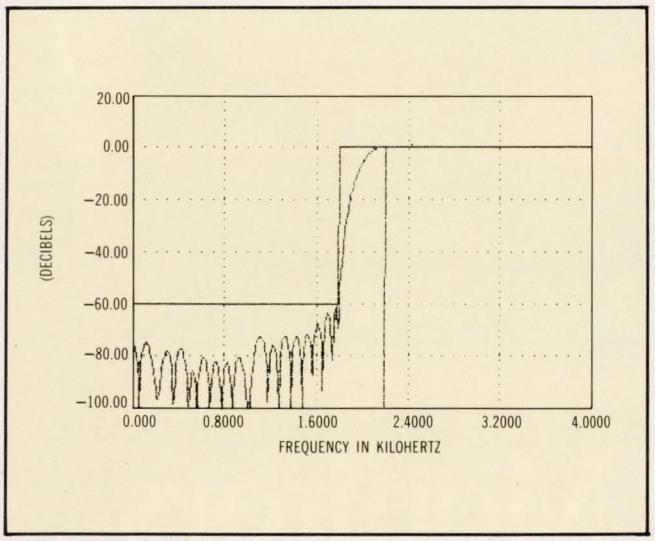


Fig 2 Frequency response 75th-order linear phase nonrecursive high pass filter is complementary to the low pass filter in Fig 1.

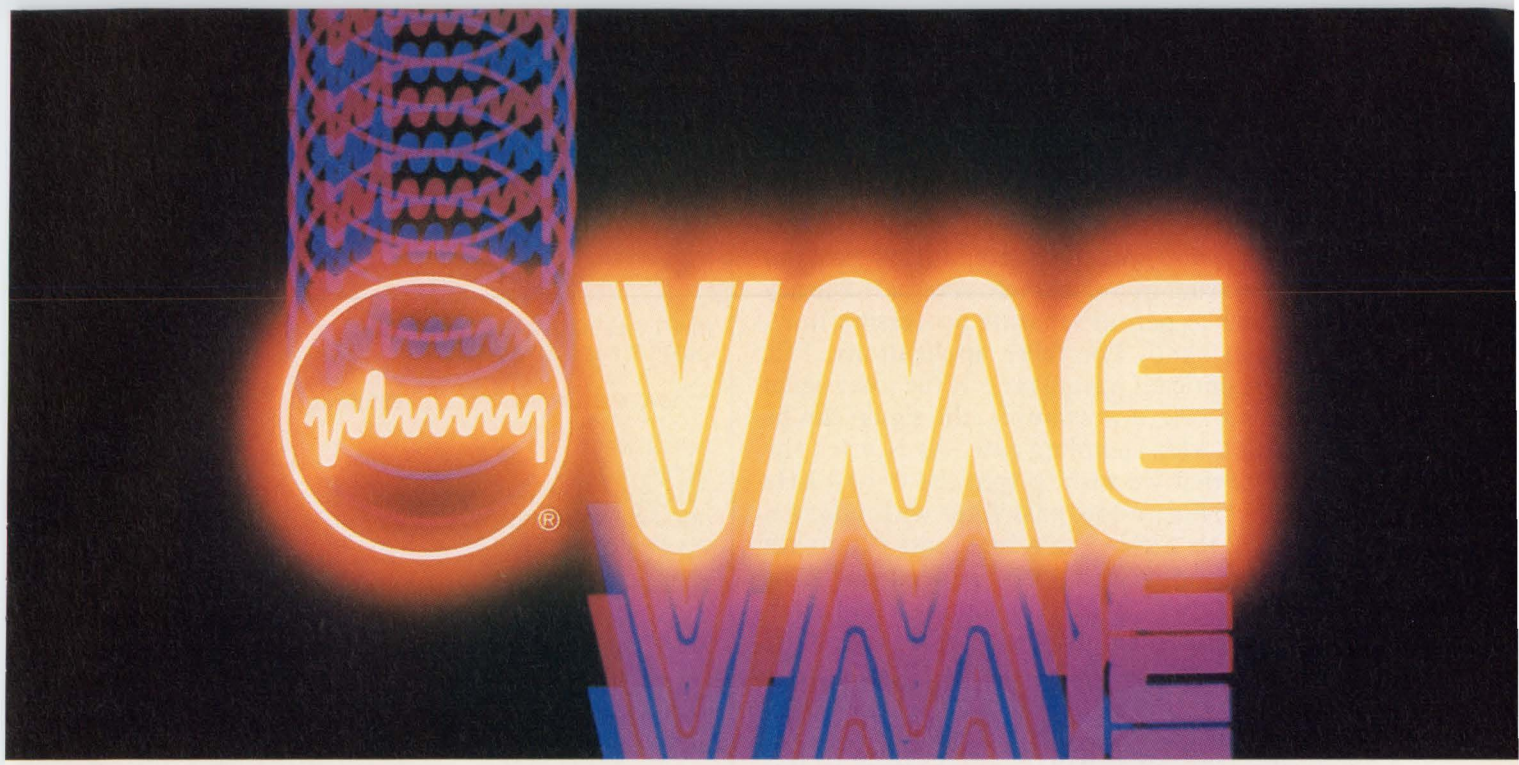
An example of a more sophisticated design tool is a package of programs developed at Atlanta Signal Processors, Inc (ASPI) for filter design and implementation. The package consists of modules for designing Butterworth, Chebyshev, and elliptic infinite impulse response (IIR) filters and linear phase finite impulse response (FIR) filters using the Kaiser window and Parks-McClellan methods (see Panel, "Digital filtering"). These interactive design programs are integrated with a program that produces assembly code implementing the filter on the Texas Instruments' (Dallas, Tex) TMS32010 microcomputer. Using this package of programs on an IBM (Boca Raton, Fla) or TI PC, the designer can go from a set of filter specifications to a TMS32010 implementation simply by responding to menu prompts. With such a program, a designer can easily explore the many trade-offs involved in the practical implementation of a DSP system involving digital filters.

In analog design, a simple system can be built and tested on a breadboard and later committed to a printed circuit board layout. In the case of DSP systems, the breadboard could be a simulation program running in the PC workstation. Such simulators should include software emulation of the DSP microcomputer to be used in a hardware system. In contrast to the analog case, if the simulation accurately takes into account the arithmetic properties of the DSP microcomputer ultimately used to implement the system, the system and the simulation will behave identically.

If the system requires realtime breadboarding, a hardware development system or in-circuit emulator must be used. Moreover, it will probably be "mothered" by a PC. The manufacturers of DSP microcomputer chips can be expected to provide such hardware. An example is TI's Evaluation Module (EVM) and Analog Interface Board (AIB). Together they provide everything needed to assemble code for the TMS32010, insert breakpoints for program testing, and run programs in real time with A-D input and D-A output. These types of hardware development systems represent a first step. More sophisticated hardware/software development systems that can be resident in the PC would offer greater convenience. Such a system will be available soon from ASPI; and, without doubt, other companies will offer similar products.

A design example

The digital filter design package can be used to go from specifications on the response of a filter, all the way to a program for implementing the filter on a TMS32010 microcomputer. The algorithm design software can mate with a vendor-supplied



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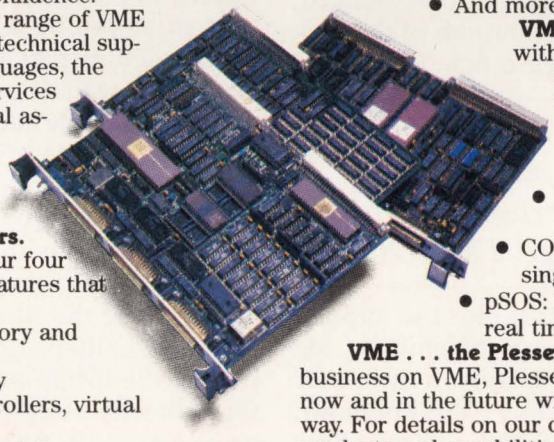

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In such applications as communication modems, tone detectors, and speech coders, a need exists to divide the spectrum of a signal into several frequency bands in order to permit separate processing functions on each band. For these applications, FIR filters have significant advantages. If the total signal bandwidth is 4 kHz, for example, the signal can be sampled at a 8-kHz sampling rate. As is often the case, suppose that we wish to split the 0- to 4-kHz band in half. Thus, a low pass filter with nominal passband of 0 to 2 kHz and a high pass filter with nominal passband of 2 to 4 kHz is needed. Let us further assume that a 60-dB rejection is required in the stopbands of the filters to provide adequate separation.

Quick turnaround

Using the IIR and FIR design programs in this filter design package, it is easily determined that these specifications can be met with a 31st-order Butterworth, a 12th-order Chebyshev, an 8th-order elliptic, or a 75th-order Kaiser window linear phase FIR filter. Any of these designs can be completed in less than half a minute of computing time and a complete summary of response characteristics is generated for evaluation of the design. Initially the filter coefficients are given to the full floating point precision of the PC. However, most DSP microcomputers, including the TMS32010, use fixed point 16-bit arithmetic, making that coefficient quantization necessary. The frequency response of the quantized filter is evaluated and compared to the specifications. If quantization causes the specifications to be violated, the designer can decide on the seriousness of the deviation, and, if necessary, design a new filter.

As part of the interactive design process, the user can specify the locations of both the program and data storage areas in the TMS32010.

At this point, the designer can plot the impulse response and frequency response (magnitude, log magnitude, phase, or group delay) of the filter. Examples of two FIR band-splitting filters are shown in Figs 1 and 2. These are 75th-order linear phase filters designed by the Kaiser window method. A significant advantage of these filters in speech applications is that their outputs add up exactly to the input (ie, the sum of the two frequency responses in Figs 1 and 2 is unity). Also, since the signal bandwidth at the output of both filters is only 2 kHz, the sampling rates of the outputs can be reduced by decimation to 4 kHz, thereby saving time for use in other operations.

```
***PROGRAM MAP***

INPUT FILE :LOWPASS.FLT
OUTPUT FILE :LOWPASS.TMS

***DATA STORAGE***        BEGINNING   END   LENGTH

FILTER INPUT                  0
FILTER OUTPUT                 1
EVM CONSTANT MEMORY           2          4      3
COEFFICIENT MEMORY            5          7      3
DELAY MEMORY                  8         82     75

***PROGRAM STORAGE***

COEFFICENT STORAGE            8         10      3
EVM CONTROL CODE             11         41     31
INT. SUBROUTIN               42         62     21
FILTER SUBROUTINE            63        218    156
```

Fig 3 The memory map shows allocation of data and program memory in the TMS32010 implementation of the low pass filter in Fig 1. With this information, digital signal processing designers can decide if the processor can handle other DSP chores or if it is saturated.

Once the specification and design phase has been completed, the filter coefficients can be saved in a file that can be accessed by the automatic code generation module of the design package. This program can take the output from any of the filter design programs and create an assembly level subroutine which directly implements the filter on a TMS32010. This subroutine can be used in standalone applications or included as part of some more complex signal processing realization.

As a part of the interactive design process, the user can specify the locations of both the program and data storage areas in the TMS32010. Moreover, the filter generation program provides a complete associated storage map that shows the allocation of data and program memory. This makes it relatively simple to merge the filter subroutine into more complex TMS32010 programs. In addition, the user can request the inclusion of code that implements the filter directly using TI's EVM in-circuit emulation board and AIB A-D/D-A board. In this environment, the filter can be thoroughly tested or can be directly used for a filtering application.

As an example of this aspect of the design process, Fig 3 shows a memory map for the filter subroutine and the associated EVM code for the low pass filter having the response shown in Fig 1. In this case, the data storage required is 81 locations (the TMS32010 has 144 RAM locations for data storage) and the program storage required is 221 (the TMS32010 can

address 4096 words of program storage), of which 156 are associated with the filter subroutine itself.

More sophisticated tools

Generally a DSP-based system would involve several filters and perhaps many other operations. Thus, a filter subroutine would be merged with a larger program and the resources of the DSP microcomputer would have to be time-shared among several signal processing functions. The low pass filter uses over half of the RAM of the TMS32010. By counting cycles, however, it is apparent that the 156 instructions of the low pass filter subroutine require only 31.2 ms of the 125 ms between data samples. The amount of computation is identical for the high pass filter. Thus, there is plenty of time left to implement the high pass filter (and more). The data memory in RAM, however, would have to be swapped out and reinitialized before computing the output of the high pass filter.

These considerations raise another issue in the design of DSP-based systems. If the computation required is beyond the capability of a single processor, another processor must be added. This puts us into the realm of multiprocessor computing, however. The need for design tools that aid in the partitioning and programming of multiprocessor DSP systems becomes even greater; without a doubt, no matter how fast the processor chips become, some problems will always require more computing resources than are available with a single processor. Although this is still very much a research topic, there is hope that design aids for multiprocessor DSP systems can be made available soon.

The theory is available, the applications abound, and the DSP chips are starting to appear in large variety. Logically, the next step in the technology of DSP systems is the direct design of VLSI implementations of entire systems. Until designers in both large and small organizations have access to such miraculous technology, there remains much to do in providing the design tools for making use of the current technology. Initial tentative steps have been taken. Much more should happen soon if DSP is to realize its full promise.

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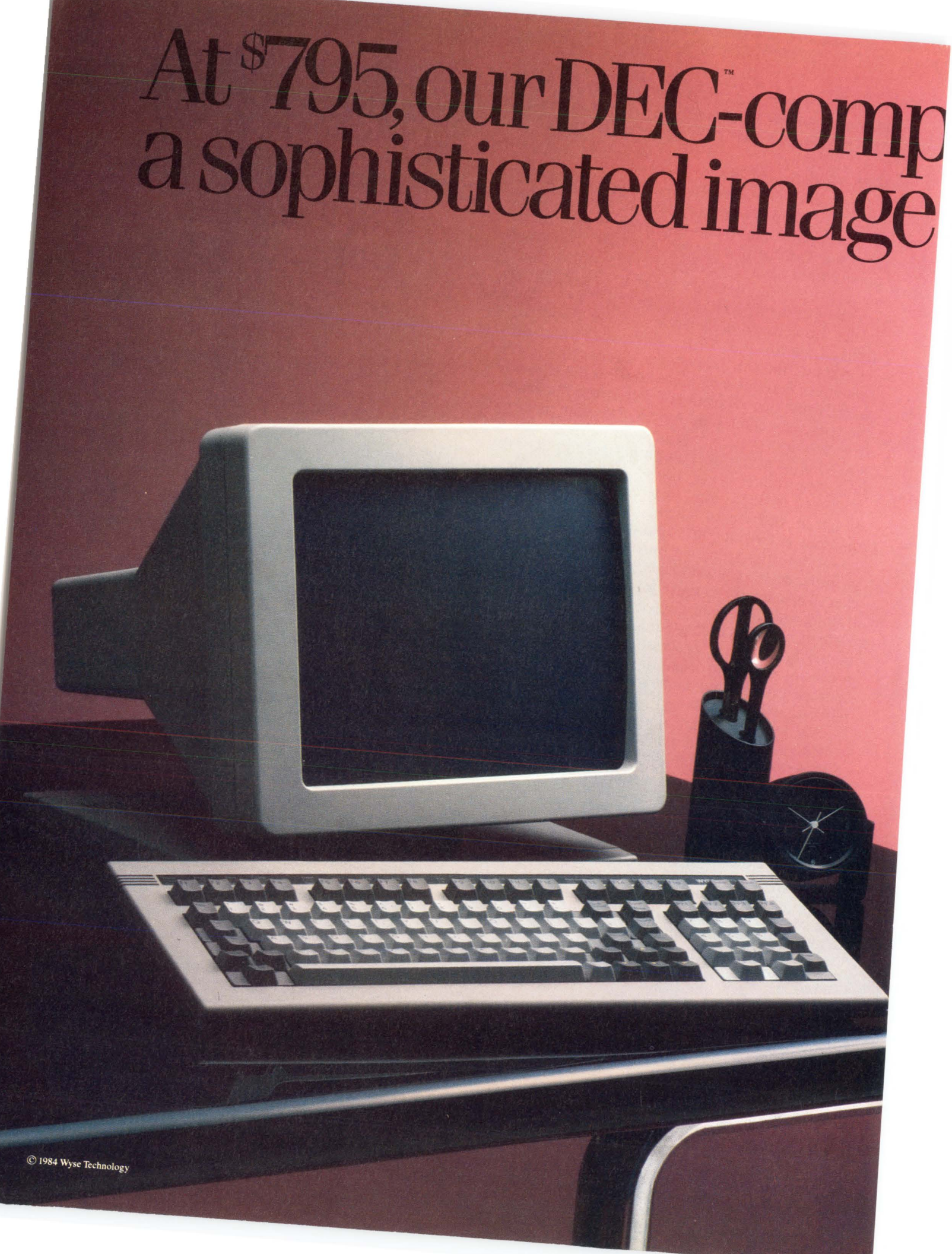

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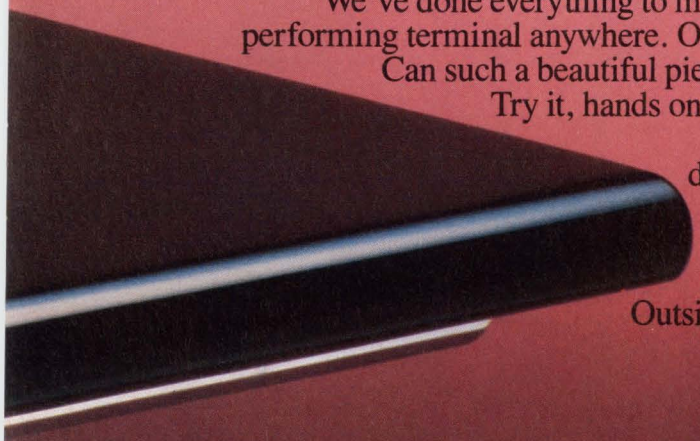

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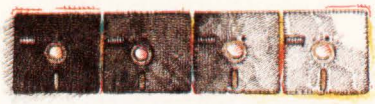

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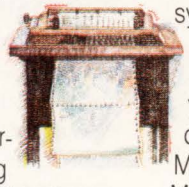

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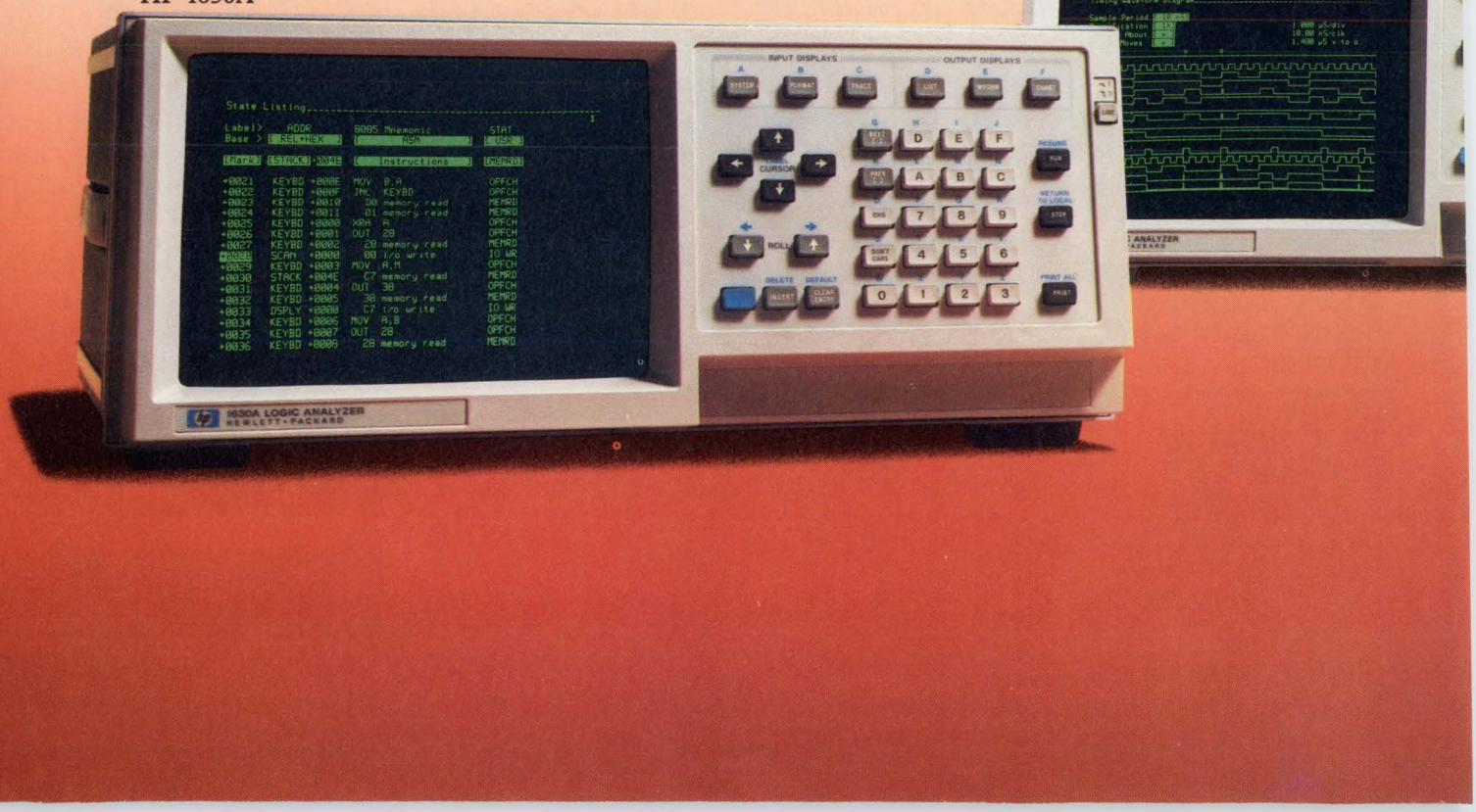

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CIRCLE 60

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CIRCLE 61

CACHE BOOSTS MULTIPROCESSOR PERFORMANCE

A cache for every CPU in a multiprocessor system reduces bus contention and memory latency. But efficient operation requires close attention to cache policy.

by Walter Mayberry and Gregory Efland

Designers use cache memory to boost performance in mainframes and superminis. This local memory between main memory and the CPU helps alleviate bottlenecks in systems with fast CPUs and large memory arrays. Now that the latest generation of microprocessors such as the NS32032, MC68020, and iAPX 286 exhibit supermini performance levels, it makes sense to incorporate caches into microcomputer systems.

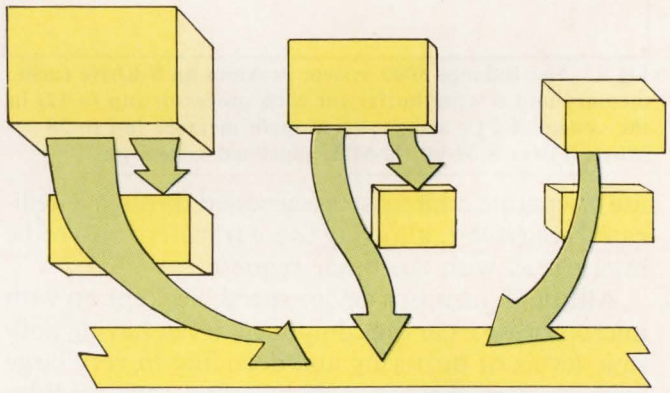
At the same time, designers are seeking multiprocessor aid in improving the performance of microprocessor-based systems. But multiprocessing creates some new difficulties for computer designers who want to use cache memory to maximize performance. Nonetheless, with proper design, cache memory can be used effectively in a tightly coupled, multiprocessor system.

A cache for every processor

Sequent's Balance 8000 system (Fig 1), for example, incorporates up to 12 Series 32000 32-bit microprocessors that operate at 10 MHz and are tightly coupled by a high performance system bus. Each processor has a dedicated 8-Kbyte cache, and shares a 28-Mbyte global RAM. Because the processors are identical and can access the entire global memory, they allow user applications, operating system routines, and I/O requests to be executed on any processor.

Walter Mayberry is director of hardware systems engineering at Sequent Computer Systems (Portland, Ore). He holds an MS in electrical engineering.

Gregory Efland is a systems design engineer at Sequent Computer Systems. He holds an MS in computer science.



The operating system, an enhanced version of Berkeley Unix 4.2, dynamically assigns work loads to CPUs according to process priority. It provides automatic load balancing for maximum throughput. In addition, the system allows access to peripherals and networks with Small Computer System Interface (SCSI), Multibus, and Ethernet I/O channels. Up to four of each can reside in a single system.

Since the 32-bit 10-MHz processors and multiple I/O channels place considerable demands on the system, two potential bottlenecks result from system bus contention and main memory latency. When multiple CPUs and I/O processors share the same path to main memory, the bus bandwidth becomes critical. This is because processors must contend for access, especially if the system is heavily loaded.

To maximize performance under these conditions, the 32-bit bus is pipelined to permit simultaneous read, write, and I/O requests from different processors. Such overlapping improves system performance by using more of the available bus bandwidth. Interleaving bus requests reduces CPU wait states by allowing some processors to initiate requests, while others wait for memory or I/O device responses. Up to three read requests and two write requests from the CPUs, SCSI, and Ethernet channels may be outstanding at one time. I/O requests to the Multibus

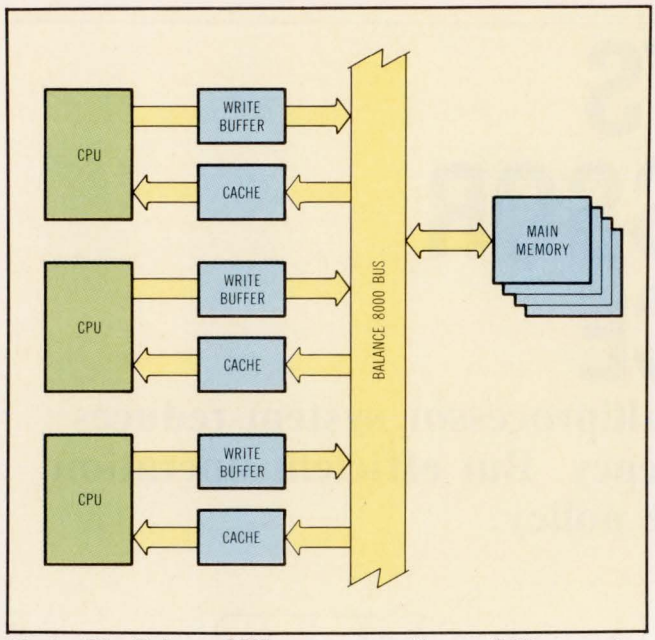


Fig 1 The Balance 8000 system provides an 8-Kbyte cache memory and a write buffer for each processor (up to 12) in the system. CPUs access shared main memory (up to 28 Mbytes) over a 32-bit, 10-MHz pipelined system bus.

use a separate address space accessed through a dedicated controller, allowing these transfers also to be interleaved with the other requests.

Although memory device speed has kept up with microprocessors at the component level, having multiple levels of buffering and decoding in very large memory arrays slows response time considerably. Unless some method is used to speed up memory response, CPUs are forced to insert wait states into their instruction cycles to allow the memory subsystem time to return data.

A cache memory placed between the system bus and each CPU in a multiprocessor system minimizes the effects of bus contention and memory latency. Keeping data and instructions in the fast, dedicated caches eliminates most wait states. Approximately 15 percent of the total CPU requests use the bus. This greatly reduces system bus traffic. When data is fetched from main memory, it can be transferred to the cache in larger blocks (8 bytes for the Balance 8000), using a 32-bit wide data path. This makes bus transactions more efficient.

A cache acts partly as a buffer matching CPU peak requirements to the average data rate of main memory. It fetches a block of data surrounding the immediate requirements of the CPU in anticipation of upcoming requests. Data that is adjacent to the last data accessed is likely to be used as well. Thus, when the CPU requests subsequent bytes, they are already resident in the cache and can be supplied to the CPU with no wait states.

When the CPU finds the required data in the cache, it is called a cache hit. If the CPU does not find the required data in the cache because the previously fetched bytes have been used, this is a cache miss. When this happens, the cache must read another block from memory and the CPU must wait for the first available word. Since cache misses seldom occur, CPU wait states are mostly eliminated.

Measuring cache effectiveness

The cache hit ratio measures cache success. The hit ratio equals the number of cache hits divided by the total number of memory requests and is heavily influenced by the total size of cache memory. Since programs usually have many iterative program structures, the hit ratio is greatly enhanced if the cache is large enough to contain an entire looping structure most of the time. Thus, no misses would occur, except possibly for data requests, until the loop is complete. (Sequent engineers used simulations of typical superminicomputer work loads to determine the optimum cache memory size. Results show that an 8-Kbyte cache provides a hit ratio of about 95 percent in the Balance 8000 system.)

The size of a cache is not the only factor determining its hit ratio. Another critical parameter in cache design is block size, or the number of bytes fetched from main memory after a cache miss. It is the one parameter that shows a negative performance improvement correlation between cache hit ratio and bus traffic levels. Increasing the block size improves the hit ratio because more bytes are prefetched for each miss that occurs. But increasing the block size also has a negative effect on bus traffic because more total bytes are transferred; and contention is more likely to occur with longer transfers. An 8-byte block size results in slightly higher bus traffic than a smaller block, but yields a significantly higher hit ratio, especially during worst-case conditions (context switching). For this reason, it is the best size for the system.

Performance is also sensitive to cache management policies. There must be an efficient mapping of the large main memory physical address space to the relatively small cache space. A subset of the main memory physical address (bits A3 through A11) helps determine where to store a block in the cache. These bits, taken from the middle of the full address word, help ensure that a series of locations in a program sequence, such as a loop structure, do not overwrite each other and drastically reduce the hit ratio.

Cache write policies

When data is written from the CPU to memory, it affects both the cache and main memory. Consequently, there are a variety of write policies with important performance and economic trade-offs (see the Table). A multiprocessing environment places emphasis on system bus operation, as well as memory response. Since cache memory reduces demands on main memory and the bus, bus traffic

Cache Memory Design Trade-offs

Design Factor	Effects on Hit Ratio	Effects on Bus Traffic	Effects on Overall Performance	Effects on Cost
Write Policies				
Write back	No effect on what is kept in the cache, hence no effect on hit rate	Produces minimum bus traffic since no local data is written to main memory until a block is replaced	Best for bus traffic reduction, but incurs software overhead	High development cost—risk of difficult software bugs
Write once	No effect	Less traffic than write through, slightly more than write back	Best performance improvement	High parts cost and complexity
Write through	No effect	Greatest bus traffic	Performance penalty largely overcome by write buffer	Medium hardware cost—increase software reliability
Write allocation	Increases bit rate since new data is available from cache	Slightly increase bus traffic	Slight increase due to higher bit rate	Performance not worth extra cost
Write buffer	No effect	No effect	Improved individual processor latency	One-deep buffer increase parts cost, but large performance gain
Total Cache Size	Larger cache increases hit ratio with diminishing returns	Higher bit ratio reduces bus traffic and wait states	Higher performance due to less wait states	Cost scales with size—best cost benefit at 8 Kbytes for Balance 8000
Block Size	Larger block size increases hit rate	Larger block size increases bus traffic slightly	Optimum performance at 4 to 8 bytes	Smaller block size requires more tag storage
Set Size	Two-way much better than one—not such improvement beyond two-way	Higher hit ratio reduces bus traffic	Significant performance improvement for two-way	Very costly—more than two-way not justified

is an important consideration for multiprocessor cache memories. Both cache size and write policies affect the success of cache memories in reducing bus traffic.

For maximum benefit, and to maintain symmetry, the Balance 8000 dedicates a cache to each processor in the system. However, having multiple caches in a system with shared memory creates a potential data consistency problem that must be solved by the cache controller logic through its write policy. Since there are no system restrictions on the memory areas that can be accessed by a particular processor, multiple copies of data can exist in different caches. This presents no problems on memory reads. But, if one of the CPUs modifies data by writing to main memory, the corresponding blocks in all caches become invalid and will remain so until the data is reread from main memory. To prevent processors from using stale data, each cache controller must recognize when another CPU invalidates any of its cached data blocks. This is necessary to allow the data to be updated.

Several policies have been devised to accomplish this (Fig 2). The "write back" technique relies on software to distinguish global data from local data. Only global data is immediately updated in main memory and made available to other processors. Local writes go to the cache. When a modified cache block is about to be replaced, then the local data is written to main memory for permanent storage. Therefore, it is important for system software to maintain data consistency. However, it is difficult to prove software algorithms for the write back policy correct under all conditions, reducing software reliability.

Another technique, called "write once," is performed completely in hardware. The first time the CPU writes to a particular cache block, the cache controller also writes the block to main memory. This not only updates global memory, but also makes the event visible on the system bus. The first write to main memory acts as a signal to all other cache controllers to make their corresponding blocks invalid and inaccessible. Subsequent writes to that

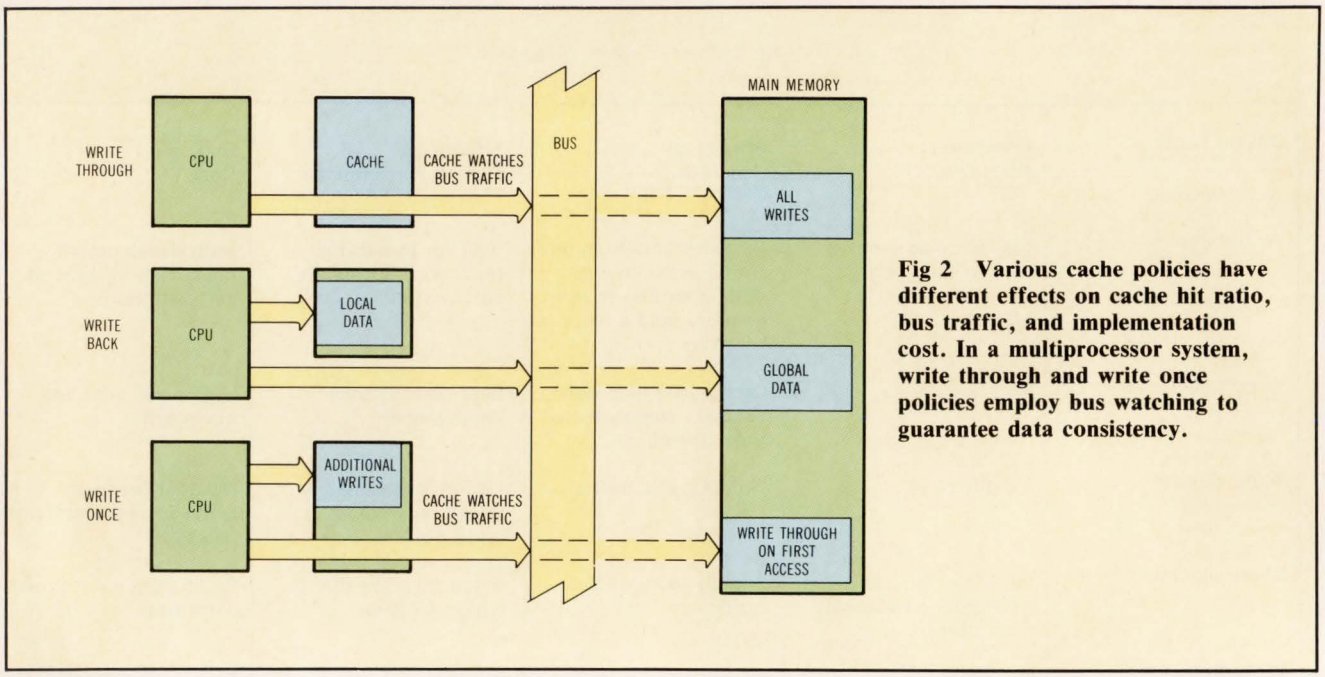


Fig 2 Various cache policies have different effects on cache hit ratio, bus traffic, and implementation cost. In a multiprocessor system, write through and write once policies employ bus watching to guarantee data consistency.

block go only to the local cache. All cache controllers continuously observe the system bus, looking for write operations—a process called bus watching. This scheme's advantages are no software overhead and easy procedure verification in all operating conditions. In addition, write once offers low bus traffic as only the first write to each block requires a bus transfer. However, the logic required to implement the write once policy is complex and expensive.

Another technique, similar to the write once, but simpler and less costly to implement, is called "write through." Using this technique, all write operations are made to main memory, ensuring that valid data is always stored there. Bus watching is still required for data consistency, but the algorithm is considerably less complex. The Sequent design utilizes write through.

With write through, cache memory write allocation, or writing data to the cache when it is written to main memory, may or may not be employed. Cache write allocation increases the chances of a cache hit, if the written data is subsequently read. But it also results in a more complex and costly implementation. Since writes are a relatively small portion of total memory accesses, less than 10 percent, the Balance 8000 performance improvement due to write allocation does not justify its implementation cost.

A write through policy is chosen instead as the best compromise between cache complexity and performance. Each cache controller forces all memory writes to update main memory. Unlike the write back method, this approach uses a hardware mechanism to guarantee data consistency. Unlike software-based mechanisms this makes it easier to demonstrate correctness, which results in improved system reliability. Write through eliminates software overhead and slightly increases bus traffic.

Since most accesses fetch instructions, a typical processing work load performs many more read requests from memory than writes. A small percentage of back-to-back writes, two write operations in succession, occur during procedure calls and context switches. Consequently, adding a small write buffer that allows write requests to be queued, waiting for access to the bus, while the CPU continues on, eliminates most CPU wait states due to memory writes. Balance 8000 has a one-deep write buffer associated with each CPU that allows one write request to be queued without CPU delay (Fig 3).

Until the request in the write buffer has been executed, the local (cached) data is different than the copy in shared memory. System hardware tests for an empty write buffer whenever it is necessary to guarantee that the write has actually completed. Main memory receives a valid copy of all data that

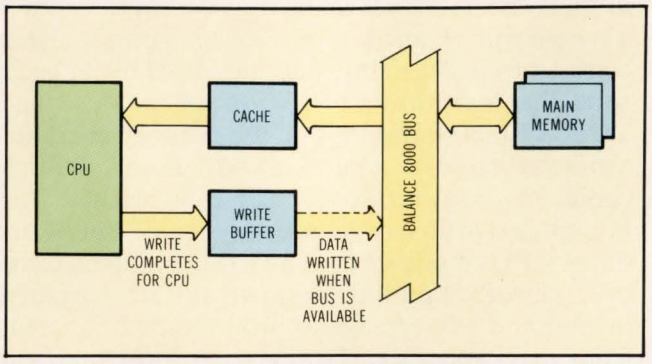


Fig 3 A write buffer enables a CPU to perform a write request and continue processing even if the bus is currently busy. The buffer is effective since back-to-back writes are relatively rare. Thus, most writes are accomplished without wait states.

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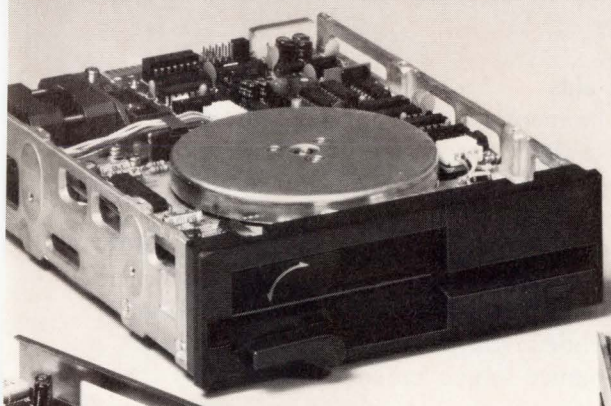

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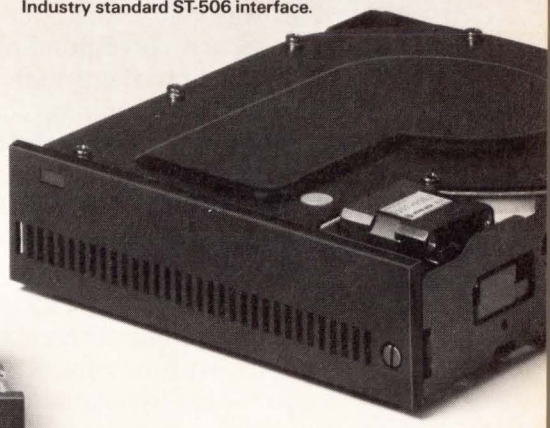

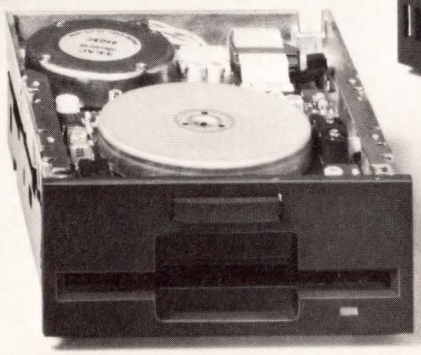

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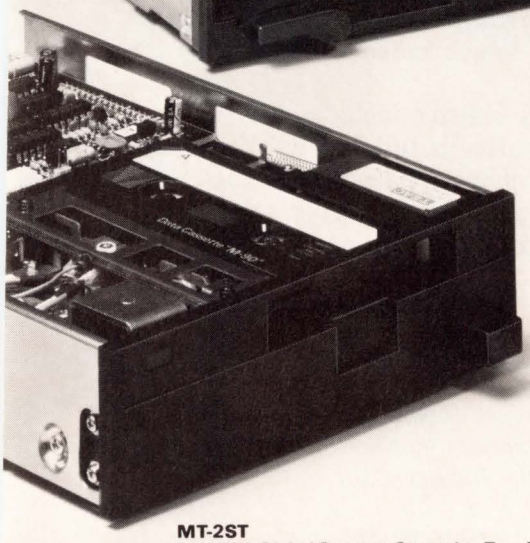

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CIRCLE 62

has been written as the bus becomes available to the write buffer.

When a CPU reads data from main memory, the cache controller uses the main memory physical address to select one of two locations in the cache. Of the two data storage cache locations, the controller displaces the "oldest" one with the new entry, since it is the least likely to be reused.

Bits A3 through A11 select a cache block, and bits A0 through A2 select a byte within the block. Bits A12 through A24 of the physical address are stored along with the actual data and are called the tag field. The tag makes the entry unique even though many physical addresses could potentially map to the same cache location.

Two-way set associative memory

The availability of two locations in the cache for a block of data is called two-way set associative addressing. It greatly reduces the chance that CPU reads to widely separated physical locations will overwrite each other in the cache if bits A3 through A11 were identical. Overwriting would significantly degrade performance by drastically reducing the cache hit ratio.

For example, consider a program that set its stack pointer and program counter to locations with identical address bits A3 through A11. If the program executes a loop to move data on the stack, the CPU alternately fetches instructions and data from areas that map to the same cache locations. Without two-way associative addressing, the data and instructions would consistently overwrite each other in the cache.

With two-way addressing, the cache controller determines the two corresponding cache locations and compares the tag fields with the upper bits of the physical address upon receiving a read request. If a match occurs, data is taken from the cache. In addition to the tag field, each cache location also has a validity bit that indicates whether the data in the cache is identical to the data in main memory, and a "set number" bit that indicates which of the two entries was the least recently used.

Tag checking is done with two address comparators combined with two tag RAMs (Fig 4). Each RAM stores 512 tag bytes and works with the comparator to match addresses. They are used in pairs (per set of associativity) to store the tag field and validity bit. The cache block index (bits A3 through A11 of the physical address) selects one of the 512 entries, and the comparator performs the tag comparison to see if the entry is valid. A single static RAM component is used to record the most recently used set number for each cache block. One bit per block is sufficient to cover the two sets.

Two-way associative addressing is the best choice. It significantly improves the hit ratio over one-way addressing. Four-way addressing makes only a small additional improvement at great cost. Since the cache must simultaneously watch both the onboard processor and system bus accesses, a second set of tag RAMs is used by bus watching to minimize cache contention. This set of tag RAMs is identical to the first set.

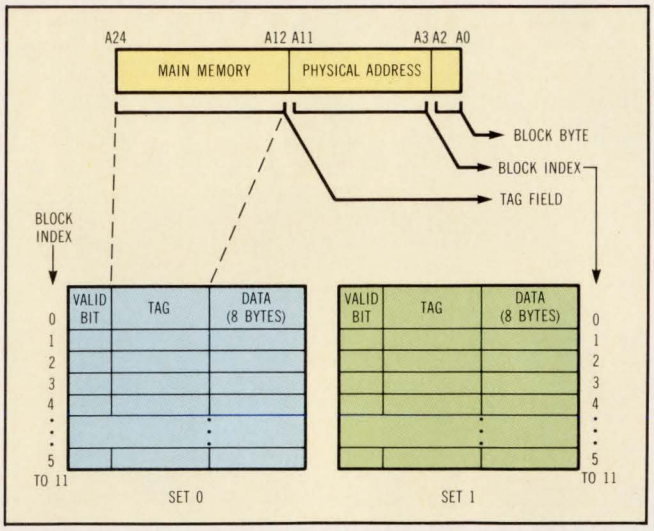
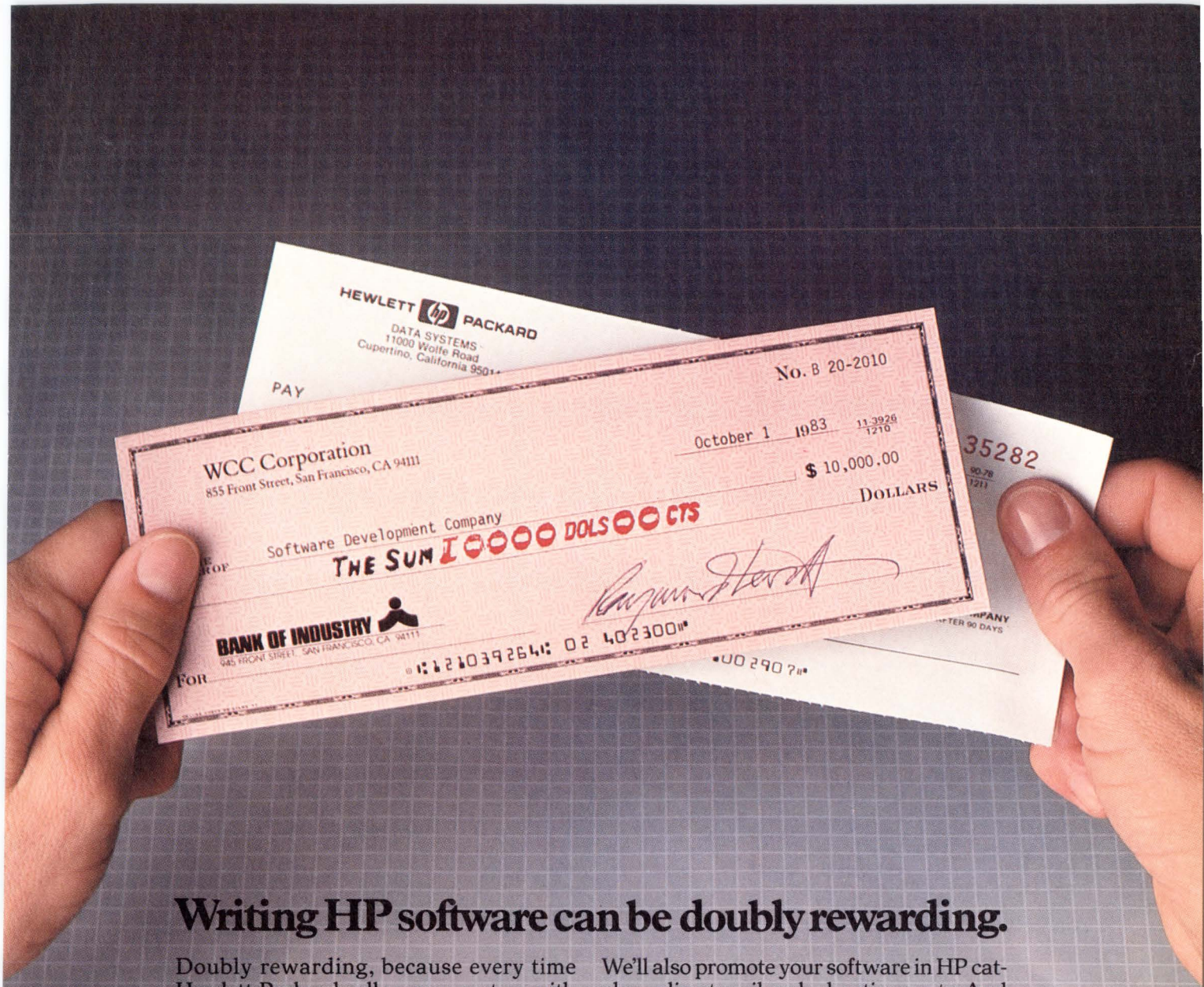


Fig 4 When a block (8 bytes) is stored in the cache, bits A0 through A2 of the main memory physical address identify the byte within a block. Bits A3 through A11 are used to select one of two potential cache locations (set 0 or set 1). The least recently accessed set is used. A tag field (bits A12 through A24) is stored with the data to distinguish between all possible addresses mapping to the cache location. A validity bit indicates if the data in the cache is current.

Diagnostic aids

The cache memory incorporates features to aid normal operations, as well as system diagnostics and monitoring. A cache control register includes a bit that invalidates the entire cache immediately. This feature is used during initialization and in diagnostics that check cache operation. Bits that disable the cache and the write buffer are useful for isolating problems while in diagnostic mode and in assessing the performance improvements provided by these facilities.

A cache status register includes bits indicating when the write buffer is full and whether the last access was a hit or miss. The first of these bits is useful to system software that must guarantee the data is written to main memory. The hit/miss bit aids in diagnostics by indicating whether the data came from cache or main memory.



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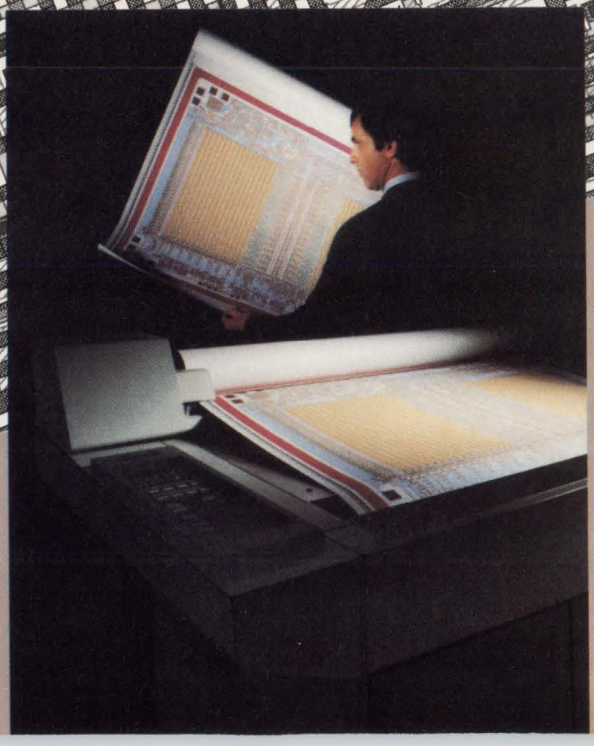

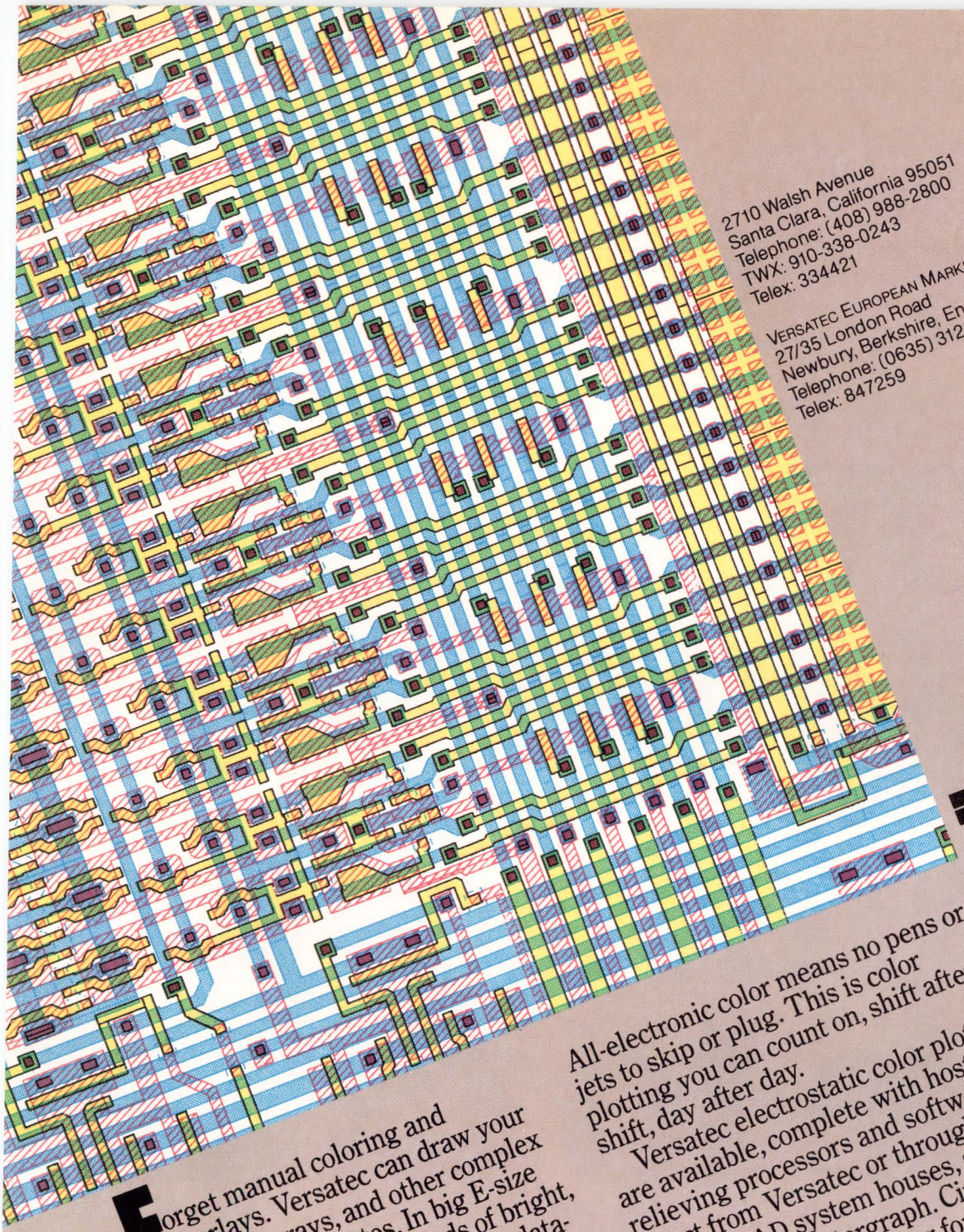

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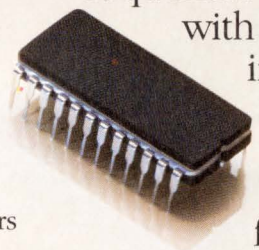

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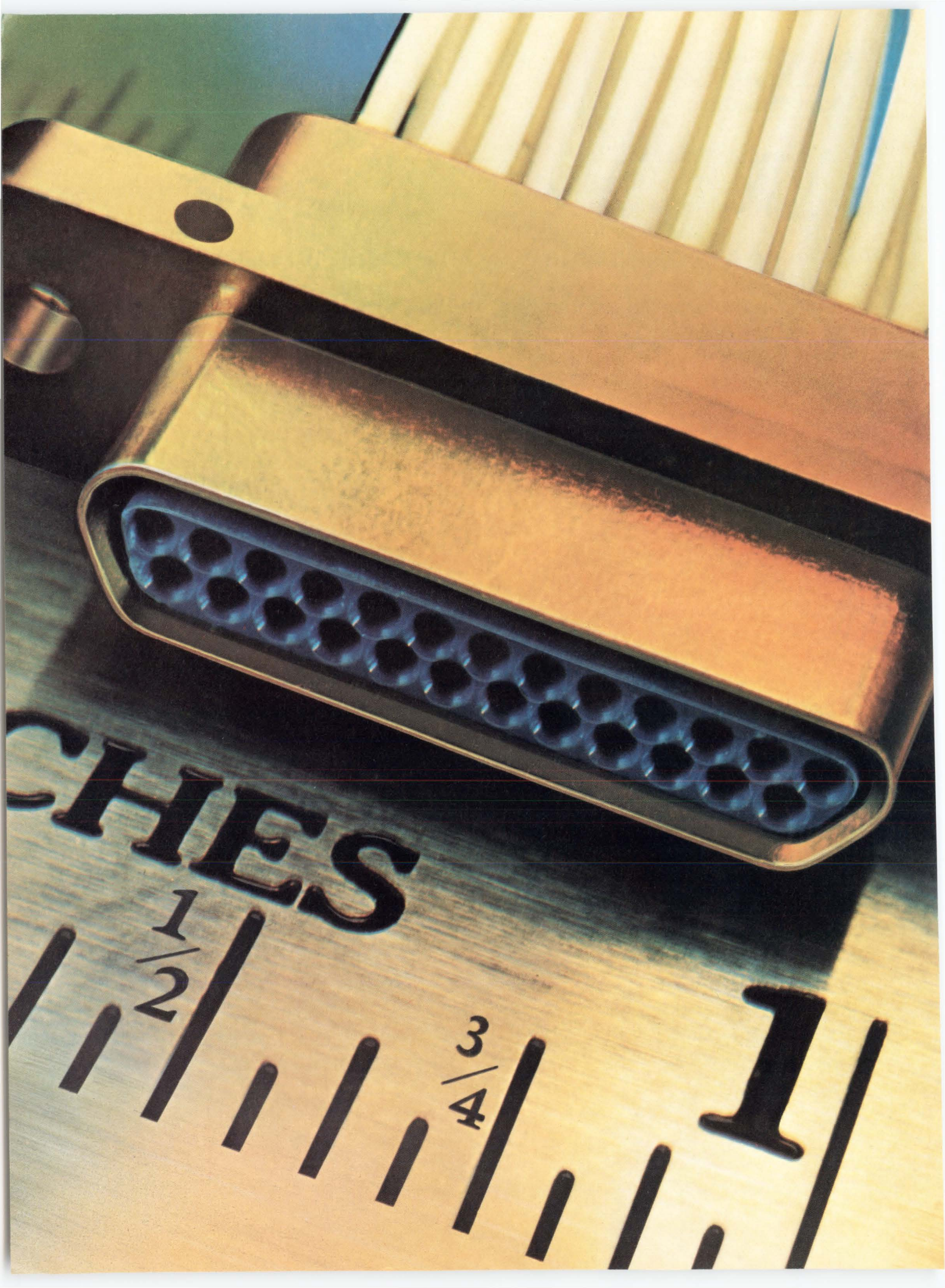
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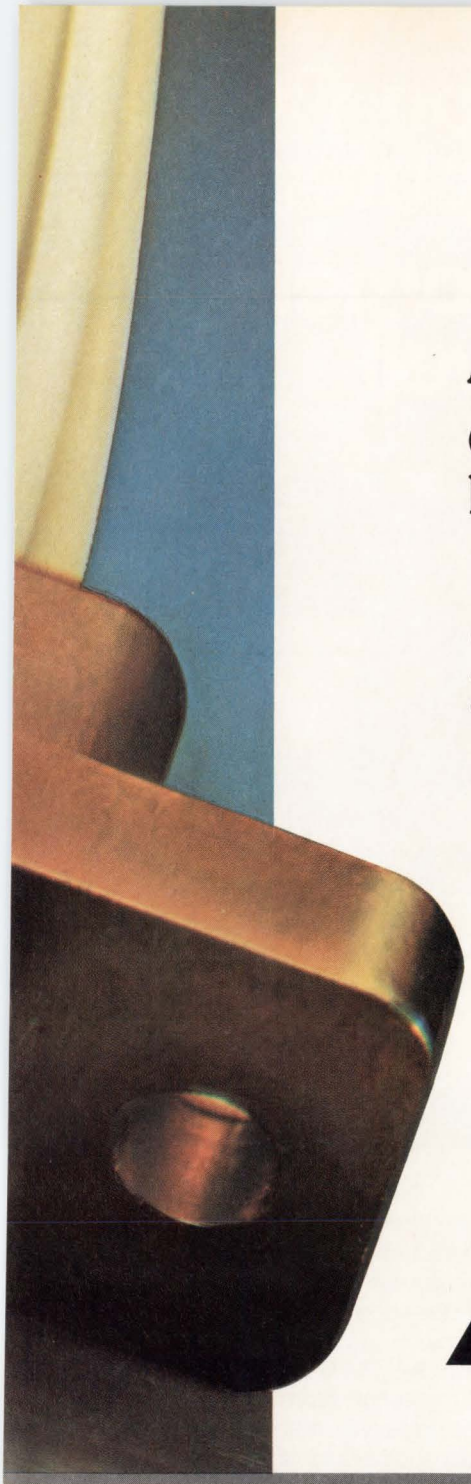

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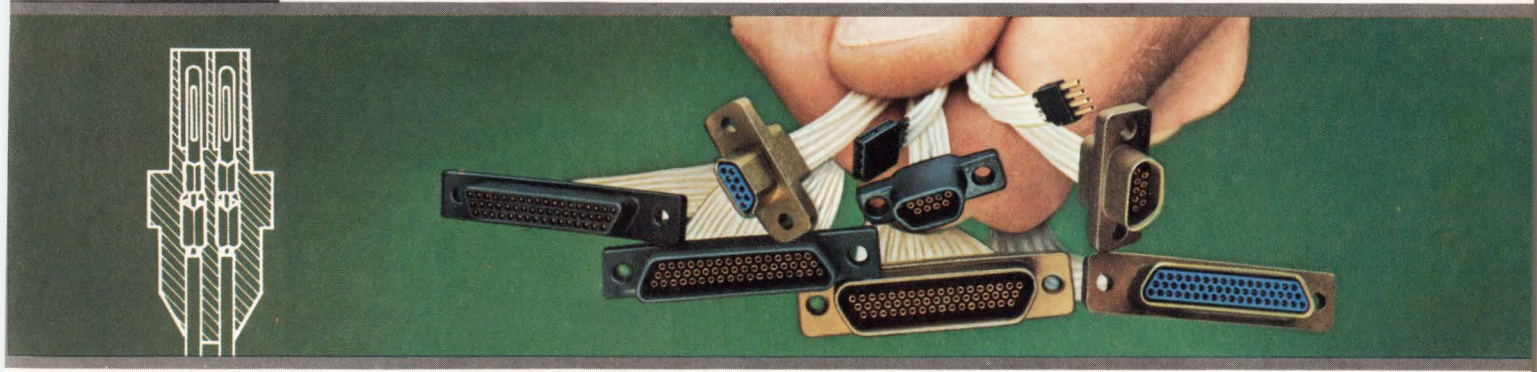

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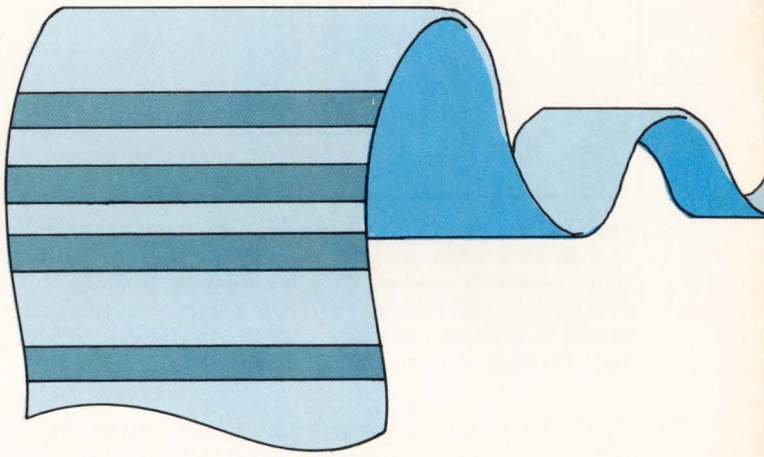
CIRCLE 66

PORTABLE COMPILER EASES PROBLEMS OF SOFTWARE MIGRATION

A layered approach to compiling high level languages separates language specifics from hardware dependencies, providing source code portability across different CPUs and operating systems.

by Lowell Wolf and Kin-Man Chung



Faced with market pressures to provide popular application software packages, most microsystem designers have had to choose between two strategies. They can either limit their microprocessor choices to those with a high level language compiler or accept delays in introducing products built around new microprocessors.

By drawing from off-the-shelf microprocessor chips, computer system designers have been able to respond rapidly to the competitive microsystems market with powerful systems for consumer, business, and engineering environments. But, unlike the traditional mainframe market, the purchaser of these microsystems is often the user. A manufacturer could once satisfy mainframe computer purchasers with powerful hardware and a set of tools for the software development environment. The microsystem manufacturer, however, must satisfy users by giving them powerful hardware and an extensive repertoire of software application packages.

Consequently, the microprocessor chip that has eased hardware design has also toughened the manufacturer's task of ensuring a wide software base for microsystem products. Now, in order to transport a system design to a new microprocessor, the manufacturer must find a quality compiler for porting application software written in various high level programming languages (such as Fortran, C, Pascal, Basic, and PL/1) or implement one independently. Faced with a two- or three-year wait while a production-quality compiler is developed for the new

Lowell Wolf is product marketing manager at Digital Research, Inc, Pacific Grove, Calif. He holds a BS in economics.

Kin-Man Chung is a senior staff engineer at Digital Research, Inc. He holds a PhD in computer science.

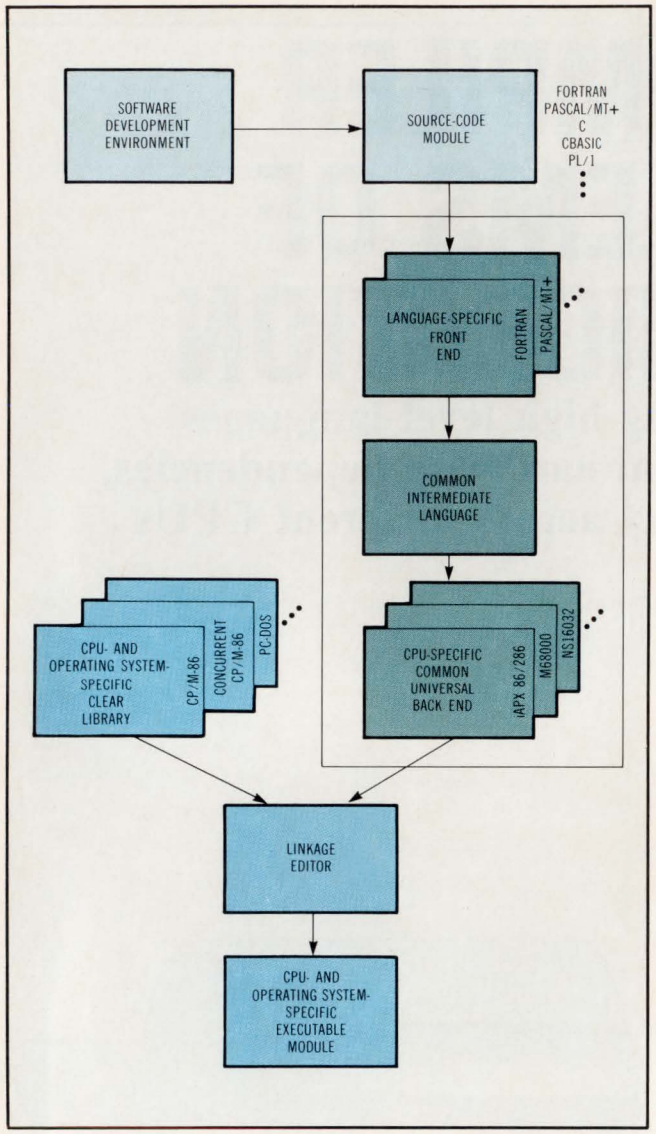


Fig 1 Portable compiler technology separates compilation of high level languages into two separate phases. A linkage editor combines modules from the common language environment and runtime (CLEAR) library with compiler output to produce executable modules for specific CPUs and operating systems.

microprocessor, system designers are often forced to accept a costly, perhaps fatal, delay in product introduction.

Compiler components

A portable compiler technology developed by Digital Research cuts this delay by offering a layered approach that separates a high level language from the vagaries of a particular microprocessor instruction set (Fig 1). Separate frontend packages for each high level language translate source code into a common intermediate language (CIL). Conversely, a special common universal backend package—unique to a given microprocessor—converts this CIL code into the machine instructions for a particular microprocessor.

Because the common intermediate language separates language specifics from hardware dependencies, this approach requires only one frontend package for each high level language and only one backend module for each type of microprocessor. As a result, Digital Research can quickly rehost its entire set of high level language compilers to a new microprocessor simply by creating a new backend module.

Still, because the execution of an application package depends on the availability of various resources during run time, transporting application software requires more than rehosting a quality compiler. It also requires a consistent runtime environment. Thus, part of the portable compiler technology includes a common runtime library that provides language-independent support of various data types, functions, and utilities.

Multiple aspects

A look at the various aspects of programming languages, program implementation, and code execution helps define the role of this new compiler technology. To use a simple assignment statement, such as A = B + C, several aspects of computer science come into play at different stages. These include language design, language implementation, program compile time, program load time, and program run time.

In implementing an accepted language like Fortran or C, software engineers follow standard approaches for the first phase. This is where the attributes of the various elements of a language are determined. For example, Fortran language design dictates that A, B, and C are values like real numbers (by default) or integers (by declaration) rather than, say, strings.

During language implementation, on the other hand, software specialists determine the code that will be used to assign the sum of B and C to A. At compile time, the language compiler determines the specific attributes of the variables. For example, a Fortran program might have declared A, B, and C as integers, resulting in an integer assignment to A, B, and C during compile time. The compilers manage these latter two phases, thereby producing machine-specific code in a format that is called the object-time format.

All external references contained in this object-time code are resolved during load time. For example, a program called a linkage editor resolves references—subroutine calls to library modules—in an application program that uses the common runtime library. The result of this phase, which produces a runtime format, is the specific image of the program as it will exist in system memory when it is loaded for execution. During execution—program run time—the value of A will finally be determined.

Other approaches to porting software to different microprocessors have depended on the concept of

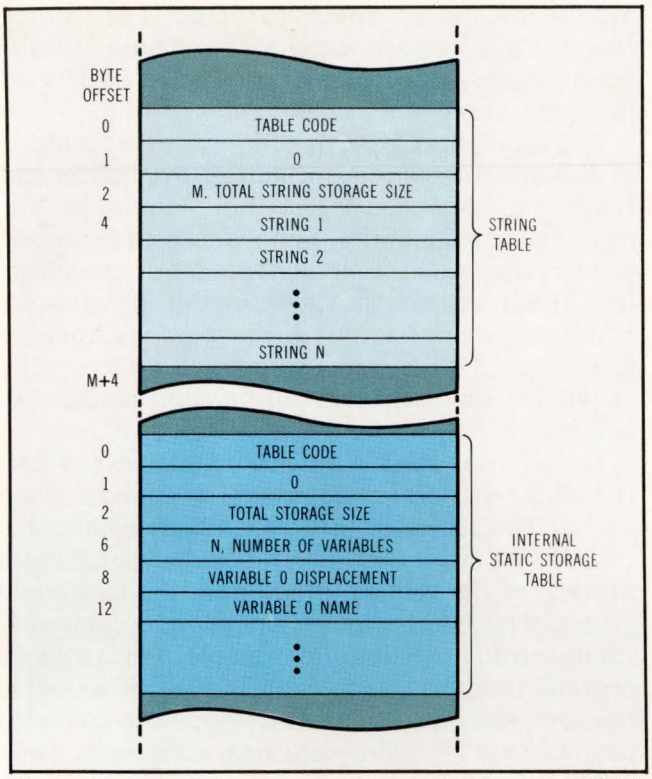


Fig 2 As part of the common intermediate language (CIL) file, the symbol table file contains addressing information for the source code. The string table contains names of all symbols used in a program. Variable names in other tables are actually references to this string table.

a virtual machine. Rather than producing object-time code that is specific to a particular microprocessor, virtual (or pseudo) machine language translators produce an intermediate code targeted for a theoretical virtual machine. For example, in some Pascal systems, a Pascal language translator produces an intermediate code, called p-code, which is executed by a Pascal virtual machine, called a p-machine. A specific microprocessor interprets this intermediate code at run time to execute the source code. Because this interpretation phase cuts into the CPU cycles available for execution of applications, users can never gain full benefit of the power of a microprocessor. The obvious solution is to compile the pseudo code instead of interpreting it.

A compiler technology that produces native code at compile time bypasses any interpretation phase and focuses the maximum power of a microprocessor on program execution. Nevertheless, because this compiler technology relies on compilation of an intermediate code, it shares the software portability benefits of interpretive approaches.

Processor independence

When a compiler parses symbols and analyzes source program statements, it is involved in the key language-dependent phase of compilation. The portable compiler explicitly separates this phase from the hardware by using frontend modules that are constructed specifically for a given language. Besides the existing Fortran module, frontend modules will be available for a number of popular high level languages including C, Basic, and Pascal.

Because these frontend modules all generate CIL format files, any frontend module can be paired with a particular CPU-dependent backend to create a high level language compiler for the target microprocessor. Furthermore, these frontend modules are all written in C. This ensures a rapid migration to different microprocessors and operating systems, while maintaining the compatibility of source code.

A frontend module produces a pair of files that specify a particular program completely. While the symbol table file contains addressing information for all variables, the intermediate code file contains the remaining control information for a program. Backend modules use the information contained in these files to generate native code. For added speed in compiling small programs, these files can reside in system memory, rather than being transferred between memory and disk storage.

This separation of address information in the symbol table file from the intermediate code file simplifies use of the symbol table by a single-pass compiler. Moreover, it makes the table expandable. Derived from the symbol table produced by the frontend module, the symbol table file consists of a number of different tables for the various types of symbols used in a program. The string table is an important piece of information maintained in the symbol table file. It contains the spellings of all names used in a program (Fig 2). Other tables such as the internal static symbol table have address displacement information for variables as well as a reference to the names of symbols contained in the string table.

Operators and references

The intermediate code file contains CIL operators, which encode program flow and execution, and references to symbols in the symbol table file. Although these CIL operators can appear in different formats, the first byte (called the opcode) indicates the action to be performed. Because the action of some operators can also produce a value for other operators' use, alternate formats include specifications for data type and size (Fig 3). CIL accounts for many high level instructions available on some microprocessors. This is achieved by inclusion of operators for such high level instructions as array indexing, case statements, range checking, and block activation and exit.

The CIL arranges expressions and procedure calls in postfix notation (a reverse Polish logic representation). For example, a statement A = B + C becomes ABC+ = in postfix notation. Operators refer to previously specified operands with this notation. Dyadic operators, like add or multiply, refer to the previous two operands. Thus, ABC+ = causes the

addition of B and C in the first operation, leaving A = for the final operation. In fact, the intermediate code generated from this statement closely resembles the postfix notation:

```
REF(A)    /* get the address reference for A */
REF(B)    /* get the address reference for B */
VALUE     /* get the contents of B's address */
REF(C)    /* get the address reference for C */
VALUE     /* get the contents of C's address */
ADD       /* add the previous two operands */
ASSIGN    /* save the result in A's address */.
```

In accessing variables, such address references as REF(A) call up the corresponding entries in the symbol table file. Because this address reference describes an offset within a CIL table rather than a memory location, CIL address references are totally disassociated from a particular processor's memory model. The backend module retains responsibility for constructing the form of address specific to a particular CPU—whether linear or segmented.

Program control and execution

Besides having arithmetic and logic operators to specify operations, the intermediate code file contains special CIL operators for program control and expressions. For example, CIL contains a full repertoire of the kinds of conditional jump instructions that are typically a part of a microprocessor's instruction set.

One CIL operator—Save—retains the results of common subexpressions for use in different parts of a program. For example, if B + C from the previous example is also used in another part of the program, a Save operator stores the result of B + C in a temporary location for later use. (The Save operator is placed after the ADD operator in the example above.) This cuts the amount of redundant code in the compiled output, resulting in a more compact, and often faster, runtime module.

Similarly, a CIL representation of a program can compress multiple references to constants into a single storage location. When a frontend uses the Constant operator, CIL can determine the type and size of scalar constants and handle their allocation.

Another form of CIL operator passes information from the frontend to CIL or to the linker. This type of information can include compiler switches, file names, and listing controls. Linker directives permit declaration of code, static, or common sections with an optional external name or size, and permit initialization of static or common sections with data.

Once the frontend module has created the two intermediate files, a common universal backend (CUBE) module uses these files to complete the compilation process and generate native machine code for the target microprocessor. Production of efficient machine code for a CPU depends on many aspects of the intermediate code. The coding required to implement a piece of code may be different in, say, an accumulator-oriented CPU than in a general register machine.

As a result, the CUBE module draws on a number of different components, including a tree builder and walker, a local code generator, managers for registers and temporaries, a pool of constants, a code emitter, and an object-module formatter. In evaluating CIL expressions, the CUBE module uses the tree builder to generate acyclic directed graphs from the CIL. The CUBE's tree walker then traverses the graphs, carrying such global information as addresses and registers down the tree.

Once the tree walker has converted CIL expressions to values, the local code generator analyzes these values. The generator then emits an assembler-like code for the target CPU that is based on special case analysis of the values. In addition, the local code generator performs a limited amount of optimization for instruction selection; for example, it uses a single operand increment instruction instead of a double operand add instruction. This code generator also handles constant folding and array references, using a CPU's index registers whenever possible.

CUBE's register manager classifies registers into such distinct classes as 8- or 16-bit data registers or address registers. It also mediates references to registers by maintaining information about the status of each register. Because this information reflects the register's runtime status, it is constantly updated during compile time. The register manager also maintains a priority value associated with each register. Whenever the code generation process requests a register, the manager selects the register with the lowest priority. In some cases, this selection process spills the contents of a register into a temporary location for later retrieval.

Another CUBE component, the temporary manager, maintains temporary storage locations on the

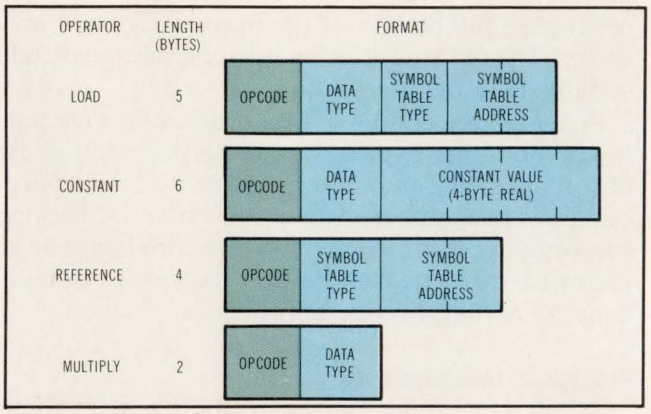


Fig 3 Although CIL operators occur in various formats, the first byte is always the CIL opcode. Because some operators such as Constant are associated with a value, the CIL operator also includes fields that specify data type and even contain values.

Standard Data Types Supported by Compiler Technology

	Basic	C	Fortran	Pascal	PL/1
Aligned bit	—	—	Yes	Yes	Yes
Array	Yes	—	Yes	Yes	Yes
Bit	—	—	—	—	Yes
Bit dynamic	—	—	—	—	Yes*
Bit varying	—	—	—	—	Yes
Character	—	Yes	Yes	Yes	Yes
Character dynamic	Yes	—	Yes*	—	Yes*
Character varying	—	—	Yes*	Yes	Yes
Complex	—	—	Yes	—	Yes
Entry	—	Yes	—	Yes	Yes
Fixed binary	Yes	Yes	Yes	Yes	Yes
Fixed decimal	—	—	—	—	Yes
Float binary	—	Yes	Yes	Yes	Yes
Float decimal	Yes	—	—	Yes	Yes
Label	—	Yes	—	Yes	Yes
Pascal set	—	—	—	Yes	—
Picture	—	—	—	—	Yes
Pointer	—	Yes	—	Yes	Yes
Unsigned	—	Yes	—	Yes	—

*These data types are extensions to the ANSI standard.

processor stack. In order to keep the pool of temporary locations small, the manager releases storage when temporaries are no longer needed and reuses locations for other temporaries. At the termination of a procedure or subroutine, this manager releases the routine's associated temporaries.

On the other hand, such constants as character strings stay in a central pool in a program's static data area. In order to avoid wasting space caused by keeping several copies of the same constant, the constant pool manager searches for an existing copy of a constant before adding a new one.

Finally, the code emitter generates binary machine opcodes from the assembler-like code produced by the local code generator. This component of the CUBE module also selects short- and long-jump instructions as needed and keeps track of all the address relocation information needed by the object-module formatter. This object-module formatter is responsible for producing the final object file.

Operating system independence

In the portable compiler technology, hardware-independent frontend modules team up with language-independent CUBE modules to create efficient compilers for a variety of host microprocessors. Still, these high level language compilers must function within the confines of a particular operating system. Application software developers cannot always be certain of a particular level of capability or set of functions within an operating environment. Consequently, the software migration process must have a consistent base of functions and utilities available across a wide range of operating environments.

The common language environment and runtime (CLEAR) library supports the native code produced by CUBE compilers with an extensive set of data types, functions, and utilities. These are available across all supported languages and operating systems. Furthermore, along with such storage management, conversions between data types, I/O, and overlay management, the CLEAR library establishes calling conventions that go so far as to permit procedure or subroutine calls between different languages.

Just as a frontend and CUBE module are combined into a language- and CPU-specific compiler, a particular CLEAR library is specific to a particular host CPU and operating system. For example, rather than relying on its own implementation of those CLEAR library functions supported directly by a particular CPU and operating system, the library draws on the capabilities of its environment. On the other hand, the CLEAR library provides operations on data types not directly supported by the hardware. Moreover, it handles functions not offered by the operating system—whether for I/O, error handling, or storage and overlay management.

Because a fundamental component of any program is its data types, the CLEAR library provides programmers with an extensive set of data types, each supported in several precisions (see the Table). For example, unsigned integers can be 1, 2, or 4 bytes in length, signed integers can be 1, 2, 4, or 8 bytes, and floating point binary numbers can be 4, 8, or 10 bytes. Each set corresponds to the IEEE specification for short, long, and extended formats.

One of the more common data types within such popular application programs as spreadsheets and word processors is the string (a sequence of bits or characters). In the CLEAR library, bit and character elements occupy 1 and 8 bits, respectively. Thus, a string of 16-bit elements is 2 bytes long, while a string of 16 character elements is 16 bytes long.

A string can appear in three forms in CLEAR—fixed, varying, or dynamic—based on the way its maximum and current length are controlled. A string's maximum length is the maximum number of elements that can be stored in the memory area currently allocated to the string. Its current length is the number of elements in use at a specific time during execution.

In addition to a wide variety of data types, the CLEAR library also supports descriptors for such data objects as strings and arrays. A data descriptor consolidates information about a data object and offers programmers a convenient mechanism for

manipulating large data structures. Descriptors are generally useful for working with an object located in a program's dynamic storage areas or for passing an object as an argument in procedure or subroutine calls.

Programmers sometimes use descriptors to establish a more uniform method of dealing with data. String descriptors, for example, permit a uniform treatment of bit or character strings. Furthermore, programmers can maintain descriptors for arrays so that frequently used information is more accessible. Using the CLEAR library's array descriptor, programmers have ready access to type, size, and subscript range information about an array (Fig 4).

Standard calls

One vital aspect of the standardization effort deals with the details of language syntax and interaction with operating systems less than with the runtime interface between different procedures or subroutines. This is the case whether those procedures are implemented in the same language or not. The CLEAR library defines a particular stack-oriented method for passing arguments between procedures. Because the CLEAR architecture must support such stack-oriented languages as Pascal/MT+, PL/1, and Digital Research C, a stack model was elected for the runtime environment of all supported languages.

In this approach, arguments are put on the stack in reverse order during a subroutine call. Thus, for example, in the call SUBR (ARG1, ARG2, ARG3, . . . , ARGn), ARG1 appears at the top of the stack (Fig 5). A particular argument in a subroutine call can be the argument value itself, a pointer reference to the argument value, or a pointer to an argument descriptor.

Large data structures, such as arrays and data types of variable length, are always passed by reference or descriptor. This encourages a uniform language environment, because most languages cannot pass these data types by value. For languages such as Pascal/MT+ that can pass large data structures by value, the CLEAR approach requires the called procedure to copy the values into temporary storage. For functions—procedures that return a value—CLEAR generally returns the value (or pointer) through a CPU register, rather than through memory.

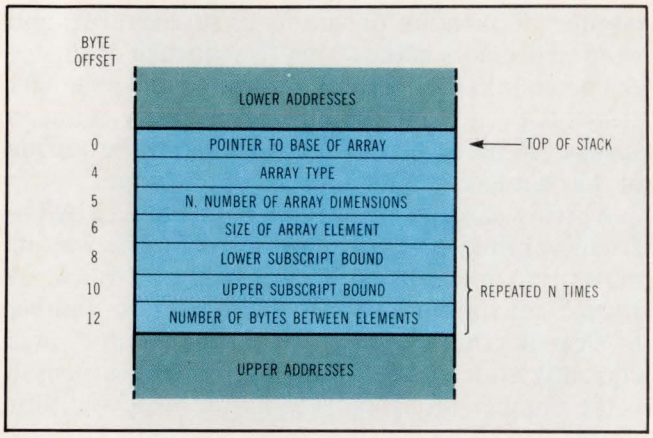


Fig 4 Descriptors provide programmers with a convenient means for dealing with large data structures. For example, an array descriptor contains detailed information about the associated array. Descriptors also offer a uniform approach for routines to manipulate an associated large data structure.

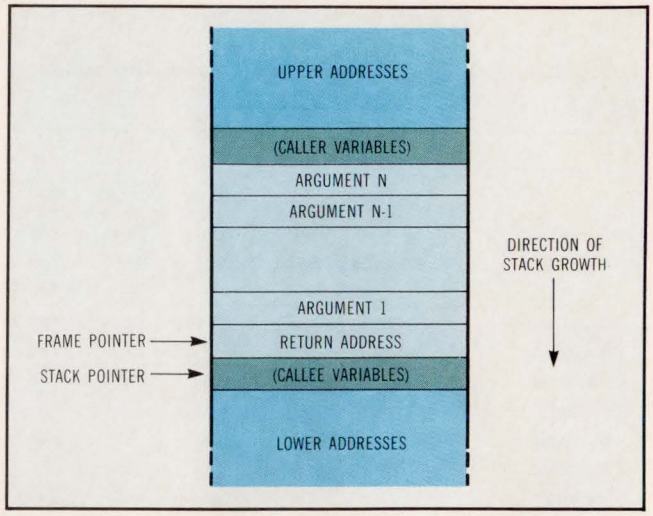


Fig 5 The CLEAR library uses a stack-oriented approach to provide a common convention for subroutine or procedure calls. After a subroutine call with N arguments, the first argument is the closest to the top of the stack—at a lower address in memory. The called subroutine can also use the stack for its temporary variables.

Overlay management

In order to execute programs that are larger than the physical memory of a computer system, programmers must ensure that only a part of the complete code for a program is present in memory at any time. In many environments, operating systems with virtual memory management handle this by shuffling virtual memory pages or segments between disk and physical memory.

Many current microprocessor-based systems, on the other hand, do not provide this complex virtual operating environment. Especially for these systems, the CLEAR library provides a method based on segment overlays. In this approach, programmers separate unrelated code (and data) into different segments. Because the separate segments contain unrelated code and data, a particular segment—a portion of the entire program—can exist in system memory apart from the other segments that contain the rest of the program.

Consequently, unrelated segments can be brought into memory and actually laid over the code for another segment. Because of the destructive nature of the overlay approach, programmers follow definite rules for creating overlayed programs. One rule dictates that the global data be maintained in a

nonoverlayed segment (the root segment) as in a Common block in Fortran, for example.

Although the programmer's responsibilities in using overlays are relatively simple, execution in an overlayed environment requires careful maintenance of subroutine calls and returns. In the CLEAR environment, when a program calls a subroutine or procedure located in another overlay segment, it actually calls the CLEAR overlay manager directly. If the required overlay is not already resident, the overlay manager loads the overlay into memory and permits the original subroutine call to proceed. Conversely, when the subroutine call returns, it does not attempt to return to the (possibly no longer resident) calling segment. It returns to the CLEAR overlay manager instead. As with the original call, the overlay manager ensures that the required segment is resident before permitting the return to proceed.

Tools and standards

The CLEAR library and its conventions for passing arguments provide development tools to serve software design and implementation in several languages. Libraries of subroutines for CRT management already exist, along with modules for various file access techniques. Furthermore, other productivity tools such as those for high level graphics and multitasking management are logical additions.

As in many other arenas, the acceptance of standards has benefitted both manufacturers and consumers. Now with the establishment of standard languages, the expanding market for microsystems will continue to grow by transporting the large application software base rapidly to a variety of CPU architectures.

Similarly, software vendors can cut through the tedium of rehosting software simply by recompiling and linking into the target environment. As a result, software developers can concentrate their skills on creating new software products, rather than just converting old ones. Finally, microsystem users will benefit from standard languages when popular application programs become available on a wide variety of microprocessors.

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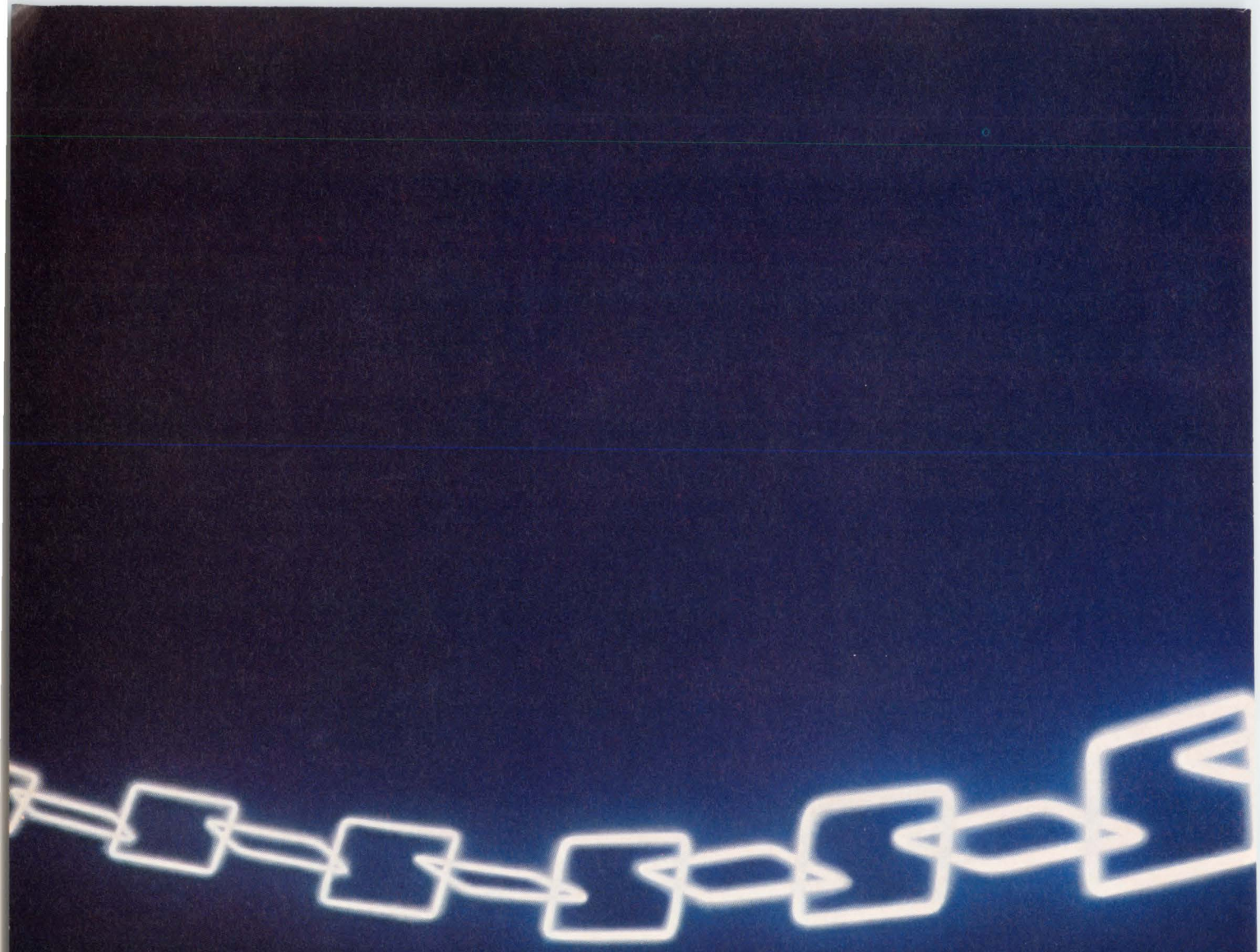

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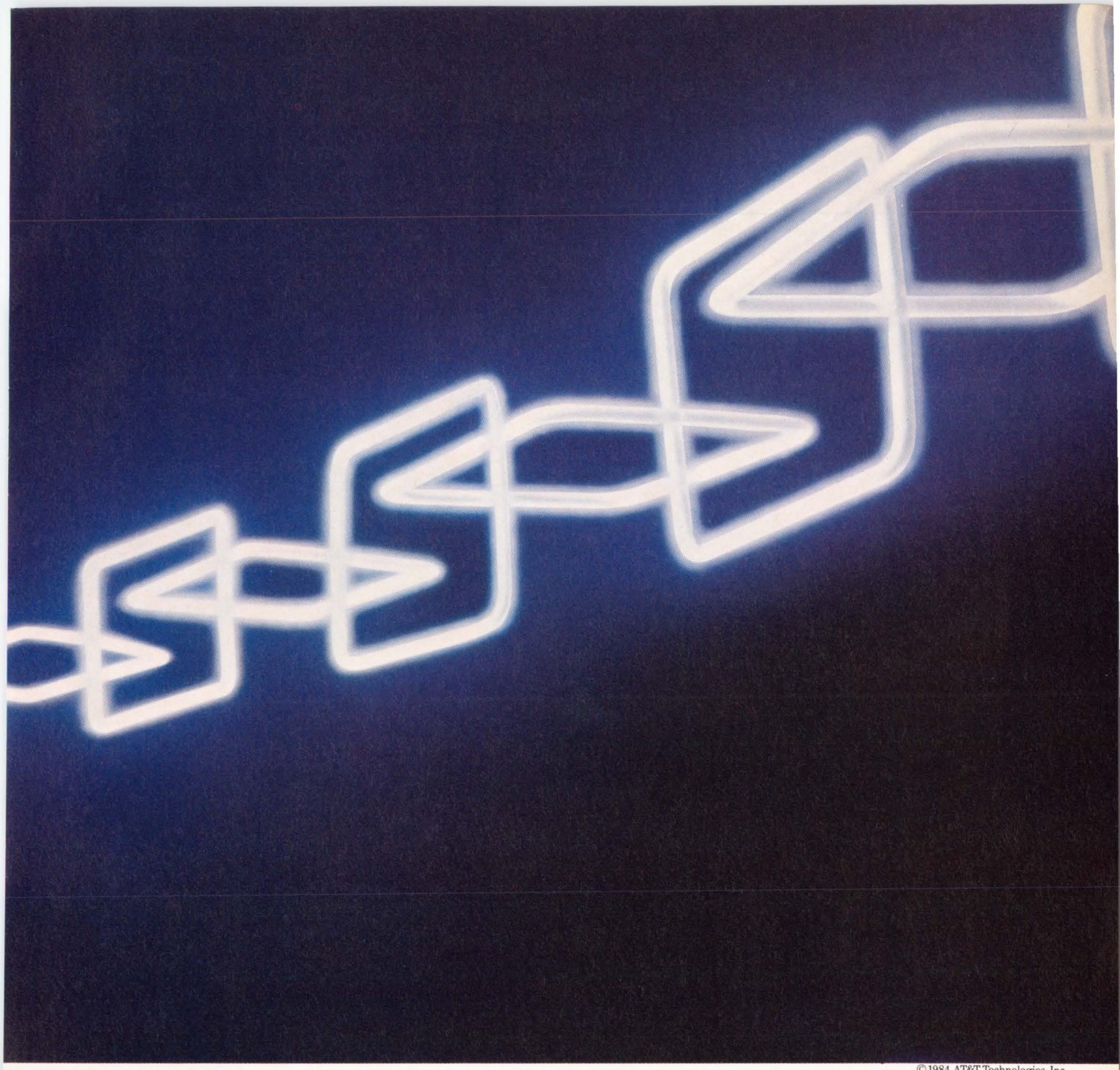

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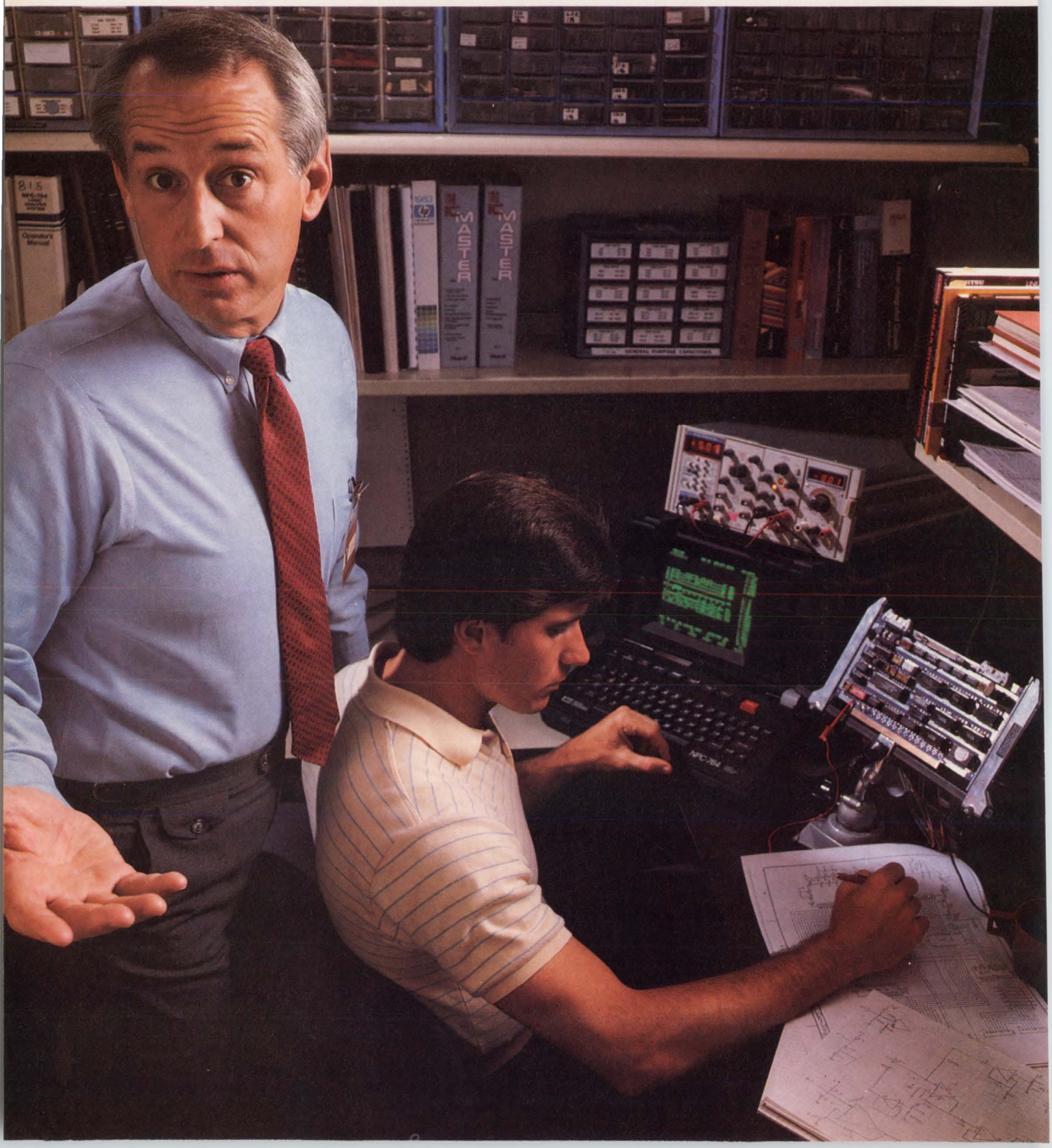

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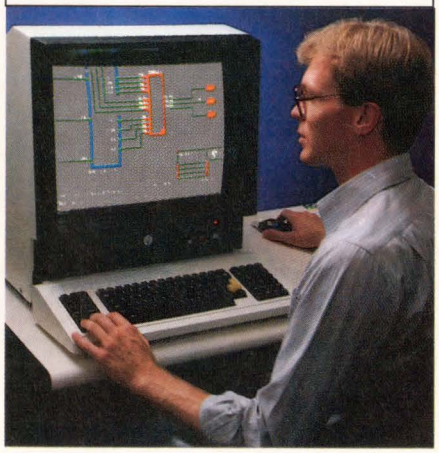

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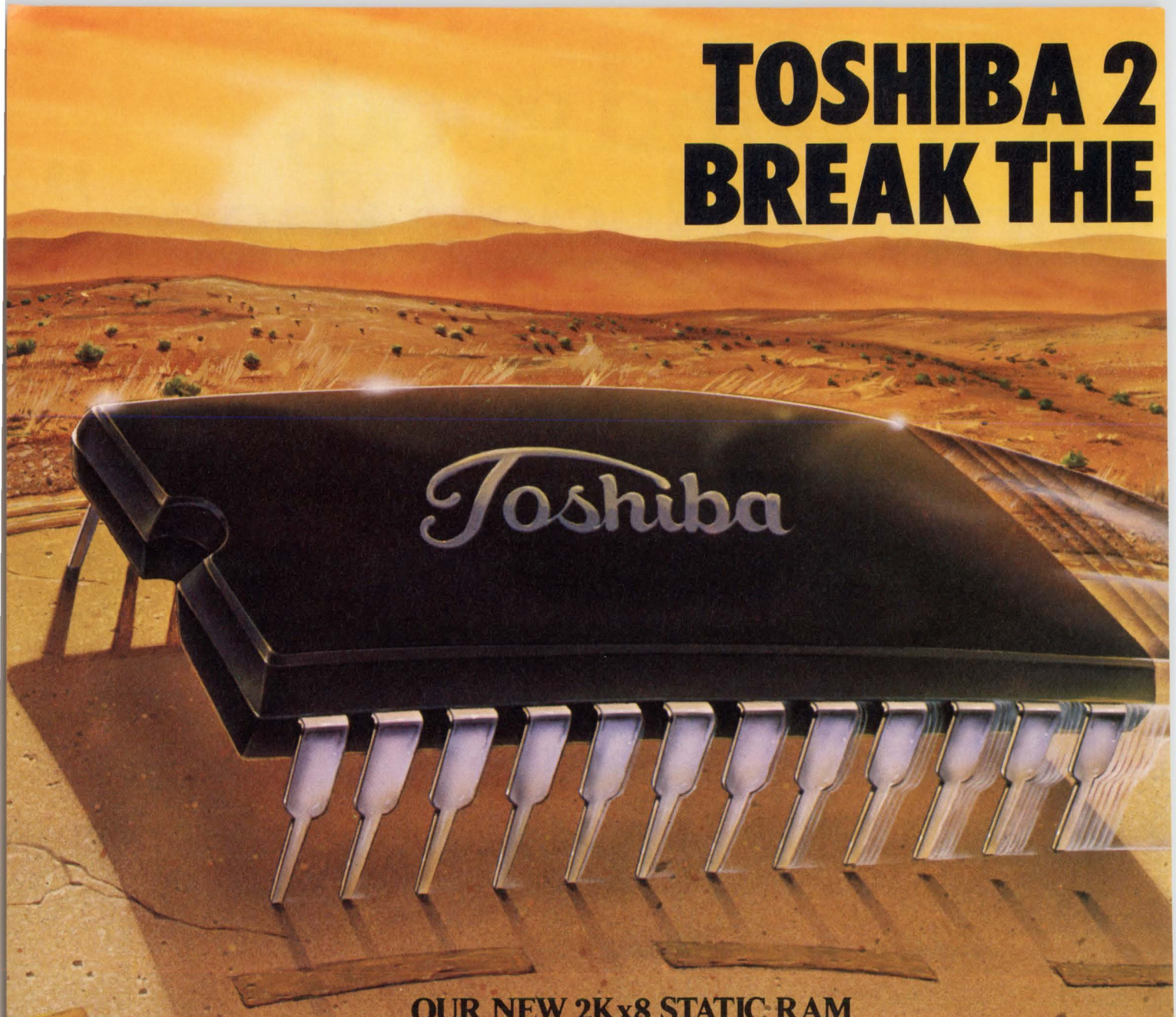

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*2015AP-10	NMOS	100ns	65mA	7mA
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**5517AP	CMOS	250ns	55mA	30 μA
**5517AP-2	CMOS	200ns	55mA	30 μA
**5517APL	CMOS	250ns	55mA	1 μA
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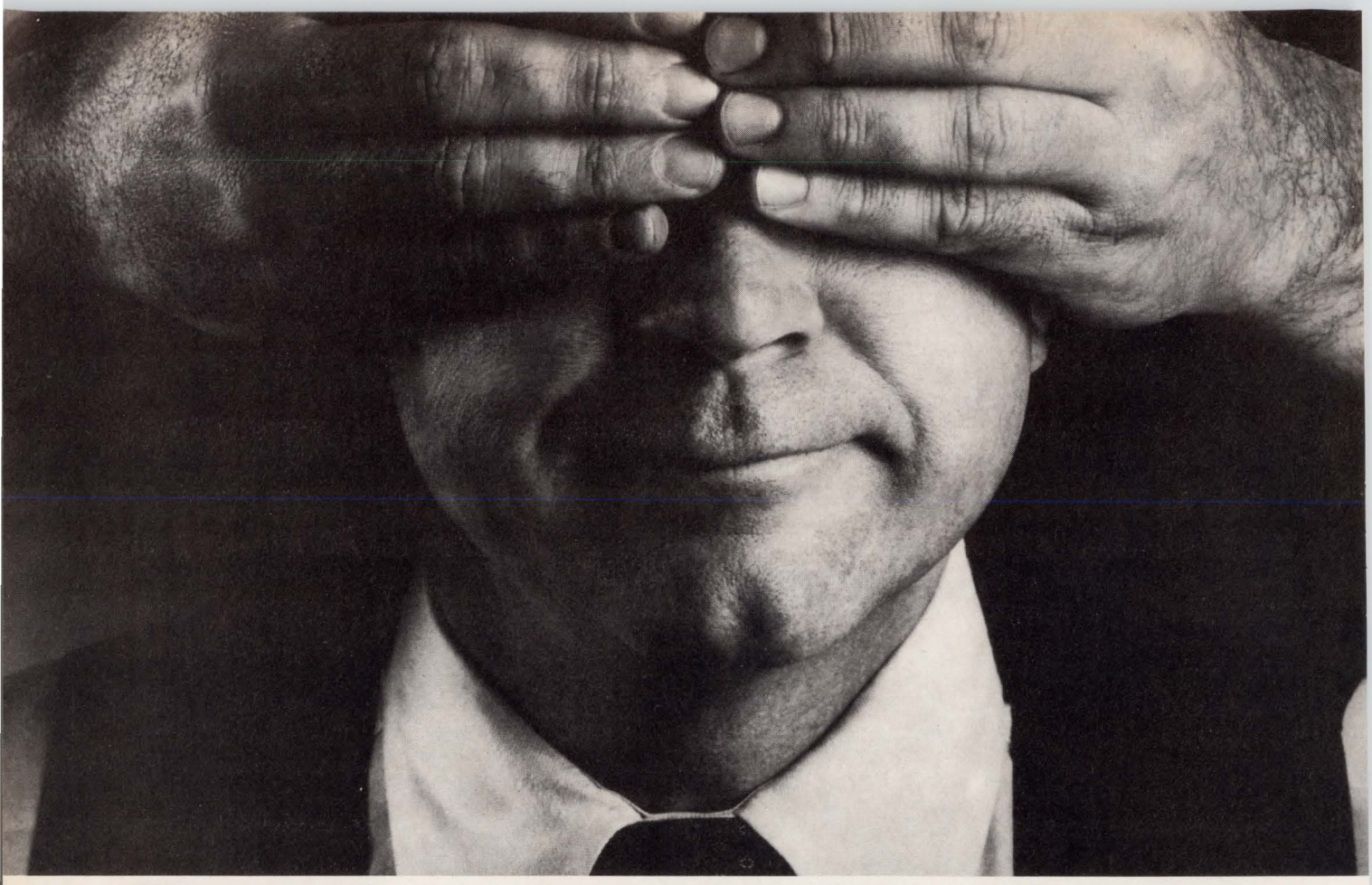

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CIRCLE 70

SPEED UP, POWER DOWN FOR BIPOLAR LOGIC

Bipolar logic—renowned for its high speed performance—uses improved processing techniques to produce chips that are not only fast, but consume little power.

by W. T. Greer, Jr and Bob Bailey

Designers know that fast logic elements—glue chips—exact a price in return for speed. That price is high power dissipation. Until now, there has been no choice but to pay the power penalty for designing with TTL, low power Schottky TTL, Schottky, and other forms of bipolar technology. Through a host of processing innovations, however, new bipolar logic not only runs faster but makes far fewer demands on a system's power budget than its predecessors.

Two families of high speed, power-conserving bipolar logic from Texas Instruments—advanced low power Schottky (ALS) and advanced Schottky (AS)—are not new, but are improved versions of low power Schottky (LS) and Schottky families. By carefully evaluating a system's speed requirements, performance can be significantly enhanced with ALS and AS components.

An application gap exists between low power, relatively slow CMOS logic, and power-hungry, extremely fast bipolar logic such as ECL. Generally, most of the signal paths in high performance systems have intermediate speed requirements. These paths need high performance logic, but not the highest speed available. To fill such "in-between" sockets, a designer's best ally is logic that provides good speed/power trade-offs. ALS and AS technology offer that capability.

In addition to trading power for performance, designers require a compatible range of devices. For example, if a logic family consists merely of SSI and MSI functions, it can be difficult to interface to LSI and VLSI chips, such as microprocessors and memories, if the larger devices come from a different family. The most successful designs will be built around complete families—SSI through VLSI—having the same blood lines. For this reason, the ALS and AS families run the gamut from simple two-input NAND gates to sophisticated chips such as a 32-bit error correction and detection circuit, a 16-bit barrel shifter, and a register file. Under development are an 8-bit slice, a 16 x 16 multiplier, and a 14-bit microsequencer.

The most widely used parameter for evaluating logic IC efficiency is the well-known speed/power product. This is computed by multiplying a logic gate's typical propagation-delay time by its typical power dissipation. This yields an energy value measured in picojoules (pJ). The number of picojoules represents a figure of merit for a logic device or device family. Semiconductor manufacturers seek

W. T. Greer, Jr is department manager for advanced low power Schottky VLSI products at Texas Instruments, Dallas, Tex. He holds an MSEE.

Bob Bailey is the strategic marketing manager for advanced bipolar products at TI. He holds an MBA and a BS in electrical engineering.

TABLE 1

Key Performance Parameters of TTL Logic

Circuit Technology	Series	Gates: Propagation Delay Time	Gates: Power Dissipation	Gates: Speed/Power	Flipflop Frequency Range
Schottky-clamped	SN54S/74S	3 ns	19 mW	57 pJ	dc to 125 MHz
	SN54LS/74LS	9.5 ns	2 mW	19 pJ	dc to 45 MHz
	SN54AS/74AS	1.5 ns	8 mW	12 pJ	dc to 200 MHz
	SN54ALS/74ALS	4 ns	1.2 mW	4.8 pJ	dc to 70 MHz
	54F/74F	3 ns	4 mW	12 pJ	dc to 175 mHZ
Gold-doped	SN54H/74H	6 ns	22 mW	132 pJ	dc to 50 MHz
	SN54/74	10 ns	10 mW	100 pJ	dc to 35 MHz
	SN54L/74L	33 ns	1 mW	33 pJ	dc to 3 MHz

to produce the lowest speed/power product devices for highest efficiency.

How ALS/AS logic shapes up

The original 54/74 family of TTL logic devices provides a convenient speed/power product reference point. A typical TTL gate offers a 10-ns delay time at a power dissipation of 10 mW, giving it a speed/power product of 100 pJ. Another useful parameter is the maximum toggle frequency under which a flip-flop will operate. Prudent designers will never attempt to use this figure for system designs since there are always circumstances under which a device will not operate properly at the maximum frequency. It is, however, a useful guidepost. The reference point again is the TTL, and the maximum frequency is 35 MHz.

Table 1 compares the highest performance bipolar technologies available to designers, including 54/74 TTL for reference. Basically, the two primary technologies in existence are Schottky-clamped and gold-doped. For each logic family within the two technologies, its propagation-delay time, power dissipation, speed/power product, and maximum operating frequency are listed.

Gold doping was an early attempt to pull higher speed out of conventional TTL. As Table 1 shows, 54H/74H logic runs 40 percent faster than TTL, but at the expense of over twice the power dissipation. Hence, its speed/power product—132 pJ—is worse than that of TTL. But, 54H/74H did extend the operating frequency of bipolar logic to 50 MHz.

Following the gold-doping experiment, manufacturers moved into Schottky barrier-diode bipolar technology. The result was two fast and fairly low dissipation families, 54S/74S and 54LS/74LS. For very high speed applications, 54S/74S offers speed twice that of "H" logic, dissipates less power, and provides a vastly superior speed/power product—57 pJ, as compared to 132 pJ. Its stablemate, 54LS/74LS, is intended for the many system sockets that operate at intermediate speeds.

When manufacturers of high speed CMOS logic (HCMOS) make comparisons against bipolar technology, it is the LS family that is almost always the bipolar representative. With a speed/power product of 19 pJ and a frequency range of 45 MHz, LS devices were ideal for the majority of system applications.

The arrival of truly high performance bipolar logic (represented by the ALS and AS families) is marked by significant reductions in device geometry as well as a number of processing innovations. In general, increases in the speed of an integrated circuit result

TABLE 2

Fan-in/out Specifications for ALS/AS Logic

Gates: Family	V_{OL}	I_{OL}	I_{OH}	I_{IL}	I_{IH}	Fan-in	Fan-out
Advanced Low Power Schottky	0.5 V	8 mA	400 μA	100 μA	20 μA	80/240*	20/600*
Advanced Schottky	0.5 V	20 mA	2 mA	500 μA	20 μA	40/128*	100/600*

*Bus Driver Output and Input

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MK77763	MDX-UMC2	Universal memory card	$150	22%
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from reductions in feature sizes. For example, LS is a 5-micron technology, whereas ALS is a 3-micron. As shown in Table 1, ALS runs twice as fast as LS.

Table 1 also shows the significant strides made by ALS/AS devices over their LS/Schottky counterparts. ALS, for example, not only runs at better than twice the speed of LS, it achieves even lower power dissipation (1.2 versus 2 mW) despite the increase in speed. In the past, higher speed accompanied increased dissipation. ALS/AS devices dramatically turn the tables on this now outmoded "rule of thumb."

The new AS family is vastly superior to Schottky logic in the same way that ALS is to LS. Running at a superfast 1.5-ns delay time with just 8 mW of dissipation, AS boasts a speed/power product of 12 pJ, compared to 57 pJ for the Schottky series. Moreover, AS logic is rated for a toggle frequency of 200 MHz, the highest of any TTL technology and a full 75 MHz faster than Schottky devices.

Upgrading I/O specifications

The ALS/AS families deliver the same drive capability as their LS/Schottky counterparts. Table 2 shows that an ALS gate sinks 8 mA and an AS gate, 20 mA. Thus, from a fan-out standpoint, a designer can directly replace an LS device with an ALS (or a Schottky with an AS) without concern for driving considerations, since both pairs are equivalent.

A significant difference exists between the families, however, on the input or fan-in side. Table 2 gives an I_{IL} value of 100 μA for ALS and 500 μA for AS. In both cases, the I_{IL} specifications are one-fourth those of the LS and Schottky families. The same holds true for the high level input current (I_{IH}) values (Fig 1).

In a mixed system—LS and ALS logic—the lower ALS input-drive requirements provide significant design benefits. If an LS gate drives ALS devices, for example, the LS gate's fan-out is increased four times because of lower ALS input specifications. That is, an LS gate can drive 80 ALS inputs as opposed to 20 of its own type. Since an LS low-output is 8 mA and an ALS low-input is 100 μA, 8 mA/100 μA = 80 fan-out. The same argument applies to a mixed Schottky and AS system. Since a Schottky gate normally drives 10 of its own type loads, it can drive four times that number, or 40 AS loads.

In addition to the standard 8-mA I_{OL} drive for ALS devices and 20 mA I_{OL} for AS devices, bus driver chips, having greater sinking and sourcing capability, are also available. An ALS bus-driver IC sinks 24 mA and sources 12 mA. If an ALS bus driver handles standard ALS inputs, it can drive 240 such loads (24 mA/100 μA = 240). With AS drivers, the loads number 128 (64 mA/500 μA = 128).

Fan-in and fan-out are dc loading characteristics and are better in ALS/AS logic than in the LS/Schottky series. With fan-in, ac loading of the input must be considered. Switching at a gate's input requires a certain amount of ac current. The lower the input capacitance, the less ac current needed to effect switching. LS gates have typical C_{in} values between 4 and 5 pF. An ALS gate's C_{in} is only 2.6 pF. Therefore, switching an ALS gate requires considerably less ac current. AS devices provide the same effect.

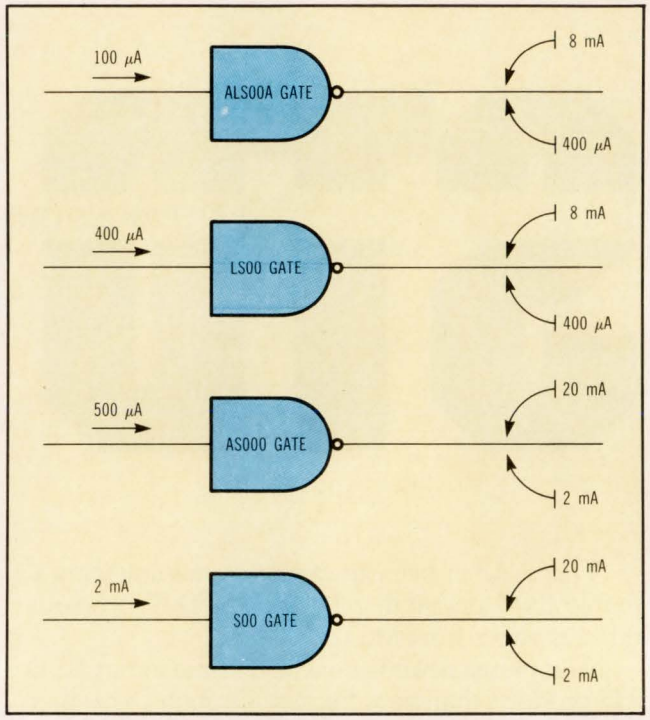

Fig 1 Standard low power Schottky/Schottky (LS/Schottky) logic and the advanced low power Schottky/advanced Schottky (ALS/AS) family provide the same output-drive capability. The difference is at the inputs. Both ALS and AS inputs are one-fourth the input current of LS and Schottky devices. LS/Schottky devices can drive four times as many ALS/AS chips than those of their own type.

Traditionally, TTL technology has been only average in noise immunity characteristics. Now circuitry can substantially improve device noise margins. A

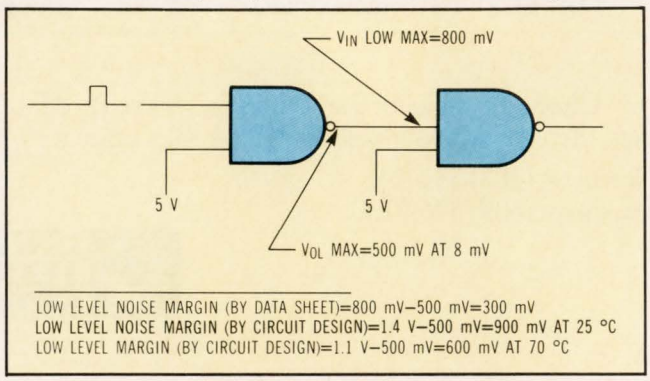

Fig 2 The low level noise margin for TTL devices is defined by voltage levels. Conventional LS/Schottky logic's noise margin is 300 mV over the full 0 to 70 °C temperature range. Redesigned circuitry allows ALS/AS logic to double the margin.

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CIRCLE 72

Bipolar logic performance—processing leads the way

Continual semiconductor processing refinements are the foundation for performance improvements in bipolar logic chips. With ALS and AS logic families, ion-implanted, shallow-junction transistors, and oxide-sidewall isolation provide higher performance. These processing innovations and others result in lower power, higher speed, and denser gate structures.

New processing technologies also permit a 70 percent reduction in device size. The Figure shows the structure of standard LS and Schottky compared to the new ALS structure. Feature sizes in ALS devices have shrunk to 3 microns, against 4 and 5 microns in standard LS chips. Still further geometry reductions are possible—2 microns is the next step—that will lead to further power reduction and speed operation gains.

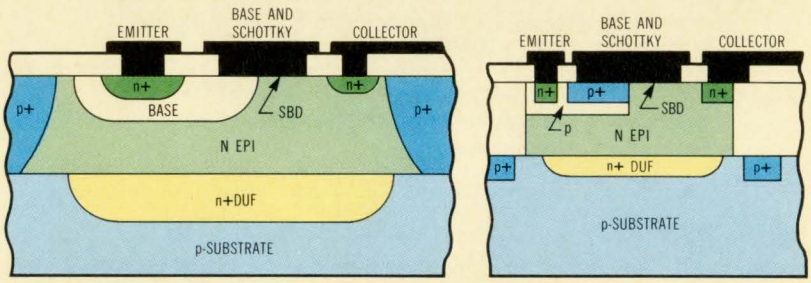
Note that the old junction-isolation technique has been replaced by oxide isolation. The new isolation method eliminates the parasitic capacitance and leakage current effects associated with pn junctions. Parasitic capacitance, in particular, imposes frequency limitations on device operation. Oxide isolation eliminates much of the parasitic effect, and allows circuit nodes to charge faster. This results in higher speed operation.

Ion implantation is a low temperature process for introducing impurities into semiconductors. It provides flexibility and precision not possible with standard diffusion processes. In bipolar transistors, for example, the base can be implanted through the emitter.

As IC speeds climb, transmission line characteristics become a factor in device operation. For example, bipolar logic devices have nonlinear input and output impedances that make them act as unmatched transmission lines. Since a typical gate is not matched to the driving or driven line, voltage over and undershoots occur. Overshoot is not a major problem, but undershoot—voltages below ground—is. In the undershoot condition, a substrate parasitic transistor (npn) can be turned on, and in turn, can pull transistors at logic-high levels to low levels. As a result, false logic states are present in a system. To counter these effects, TI adds selective grounded guard rings around input and output transistors. A guard ring lets an npn substrate transistor draw current from ground after it is turned on. This prevents the errant switching due to negative undershoots.

Other processing advances include circuitry that permits a device to automatically enter the three-state mode as soon as power is removed. Device cross talk is reduced by another circuit that serves as a current generator to recharge substrate capacitances that introduce propagation delays. Finally, bus drivers are constructed with double-level metal to reduce voltage drops and noise caused by excessive lead-inductance.

The ALS/AS logic elements that emerge from advanced processing are not only superior in performance to their predecessors, they offer designers increased system reliability.



simple gate circuit (Fig 2) illustrates how low level noise margins are defined for TTL logic such as ALS/AS devices. From a data sheet, the maximum output low level voltage (V_{OL}) from a gate is specified as 500 mV. The maximum low level input voltage applied (V_{IL}) to a gate is 800 mV. V_{IL} is the highest low level voltage that a gate will recognize as a logic 0. Assume that the driving gate puts out a 500-mV logic 0. This signal can have 300 mV of noise riding on top of it and the driven gate will still recognize the input signal as a logic 0.

Noise margins in TTL circuits are closely related to the dc threshold voltages of individual transistors in a logic state. The typical LS gate (Fig 3) has an input threshold voltage of 1 V at 25 °C. This is derived by adding the base-emitter voltage drops (V_{BE}) of transistors Q1 and Q4 and subtracting the forward voltage drop across diode D1: 0.7 + 0.7 − 0.4 = 1.0 V.

From these circuit parameters, the real maximum value of V_{IL} is 1.0 V. If the maximum V_{OL} is 500 mV, the real logic 0 noise margin is $V_{IL} - V_{OL}$ = 1.0 V − 500 mV = 500 mV. This is 200 mV greater than the datasheet noise margin. However, 500 mV is the noise margin only at 25 °C, and TTL is specified to operate up to 70 °C. Since bipolar

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CIRCLE 73

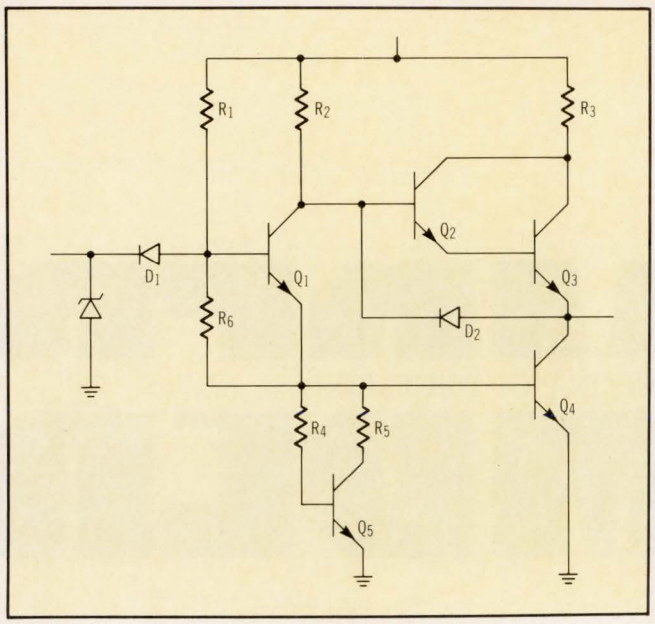

Fig 3 The noise margin depends on the logic gate's input threshold voltage, which is a function of circuit design. This typical LS gate's threshold voltage is determined by the base-emitter voltage drops of transistors Q1 and Q4, and the forward voltage drop of diode D1. Noise margin improves if threshold voltage can be increased.

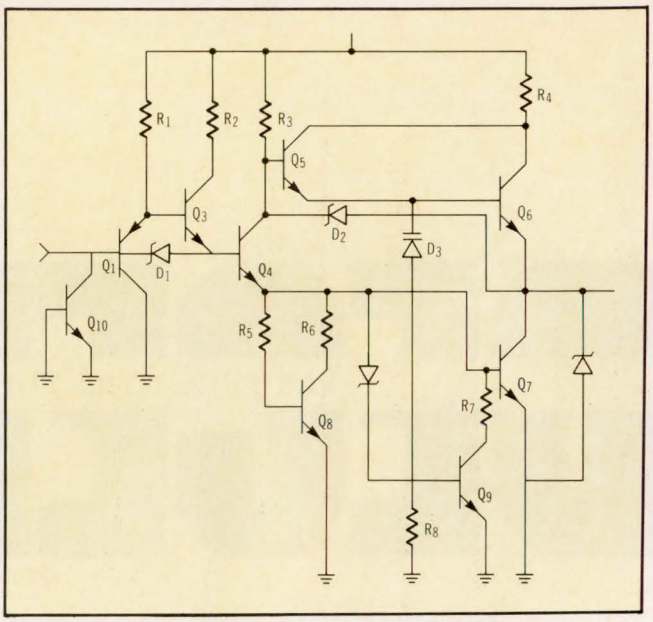

Fig 4 The improved circuit of this typical ALS gate results in a two-fold increase in ALS low level noise margin over conventional LS logic. A higher threshold voltage, determined by transistors Q4, Q3, Q7, and Q1, gives this design much more noise immunity than a typical LS gate. The same circuit improvements have given AS improved performance over Schottky.

transistors have a negative temperature coefficient of base-emitter voltage, the V_{BE} values of Q1 and Q4 will be lower at 70 °C. In fact, the threshold voltage at 70 °C is about 850 mV. Therefore, the noise margin at this temperature is $V_{IL} - V_{OL} = 850\ mV - 500\ mV = 350\ mV$. Thus, the maximum value on the data sheet is specified at 300 mV (50 mV less than the real value to account for processing and other variations).

Fig 4 shows a completely redesigned circuit representing the transistor configuration of ALS/AS devices. For this circuit, the input threshold voltage is:

$$V_{BEQ4} + V_{BEQ3} + V_{BEQ7} - V_{BEQ1} = V_{INThresh}$$
$$0.7 + 0.7 + 0.7 - 0.7 = 1.4\ V$$

Thus, the threshold for ALS/AS logic is 1.4 V at 25 °C, or 0.4 V greater than its LS/Schottky counterpart. At 25 °C, the noise margin is $V_{IL} - V_{OL} = 1.4\ V - 500\ mV = 900\ mV$. Of course, the transistors in the circuit have the same negative temperature coefficient (V_{BE}) as those of the LS/Schottky circuit. At 70 °C, the threshold voltage of the circuit will fall to about 1.1 V, giving a logic 0 noise margin of $V_{IL} - V_{OL} = 1.1\ V - 500\ mV = 600\ mV$.

Because of advances in circuit design and processing, the new ALS/AS logic provides a noise margin improvement of roughly 2:1 over the older families. In fact, the noise margin of ALS/AS logic at 70 °C is better than that of LS/Schottky at 25 °C. The result is more reliable system design and operation.

Speed/power product, drive capability, noise margin improvements, and availability are features that make ALS/AS devices the choice in applications when LS/Schottky chips are used. Two of the latest package styles, pin-grid arrays and surface-mount plastic chip carriers, are set to oust DIPs. Aside from the mechanical difficulties presented by large DIPs, the newer packages allow designers greater printed circuit board density than is possible with DIPs.

The ALS family contains 142 different logic elements with more to be added. AS presently offers 122 elements, with more expected. Approximately half of these logic devices are pin-compatible with LS/Schottky types, so direct replacement is possible.

The most efficient system designs will use ALS/AS devices judiciously. Designers can aim for optimum performance by reducing power requirements while maximizing operating frequency concurrently. Since the truly high speed sockets in systems are limited, it is likely that AS devices will be needed for about 30 percent of the total chip count. The remaining 70 percent can be filled with ALS to maintain high speed while reducing power consumption.

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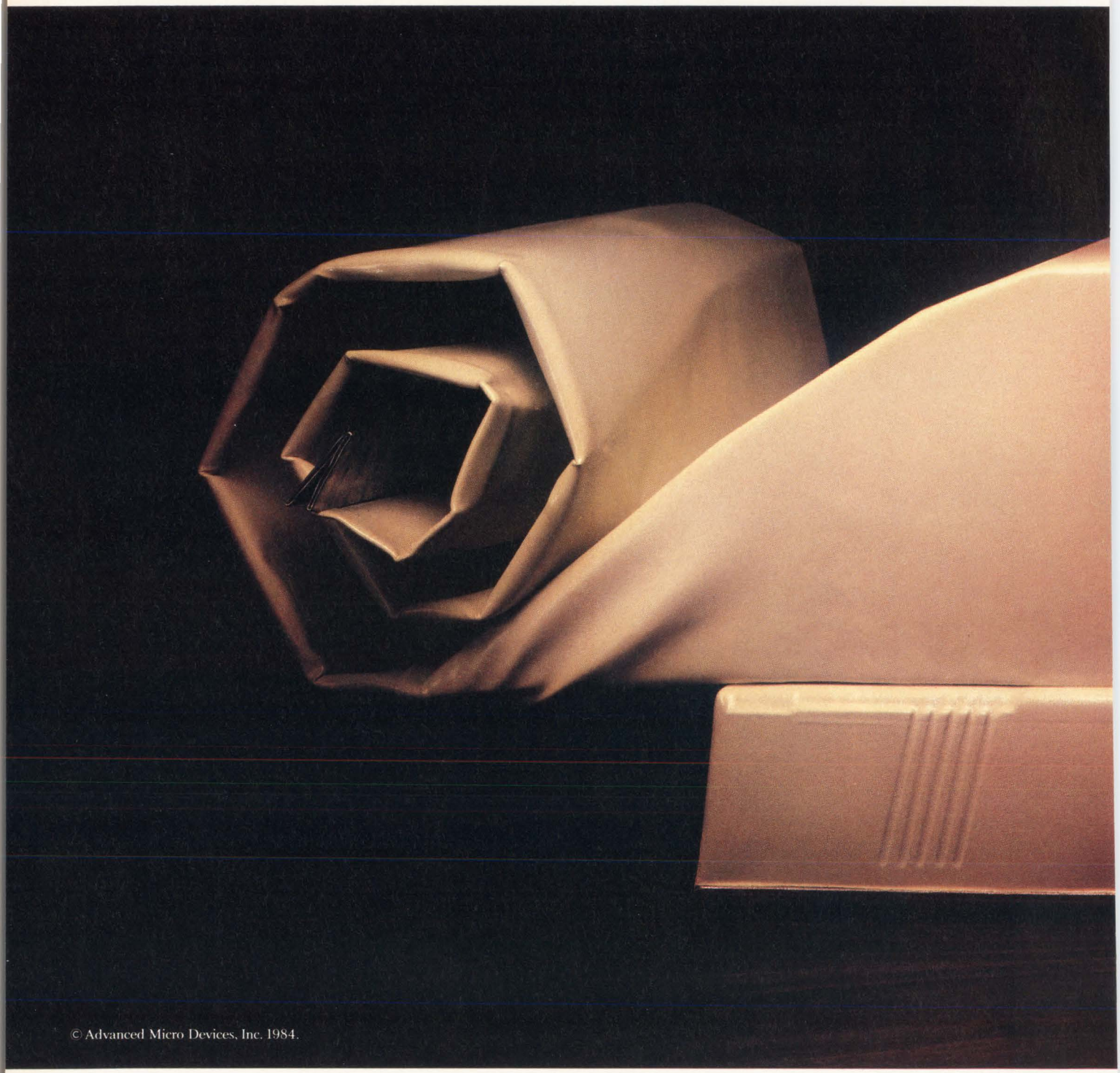

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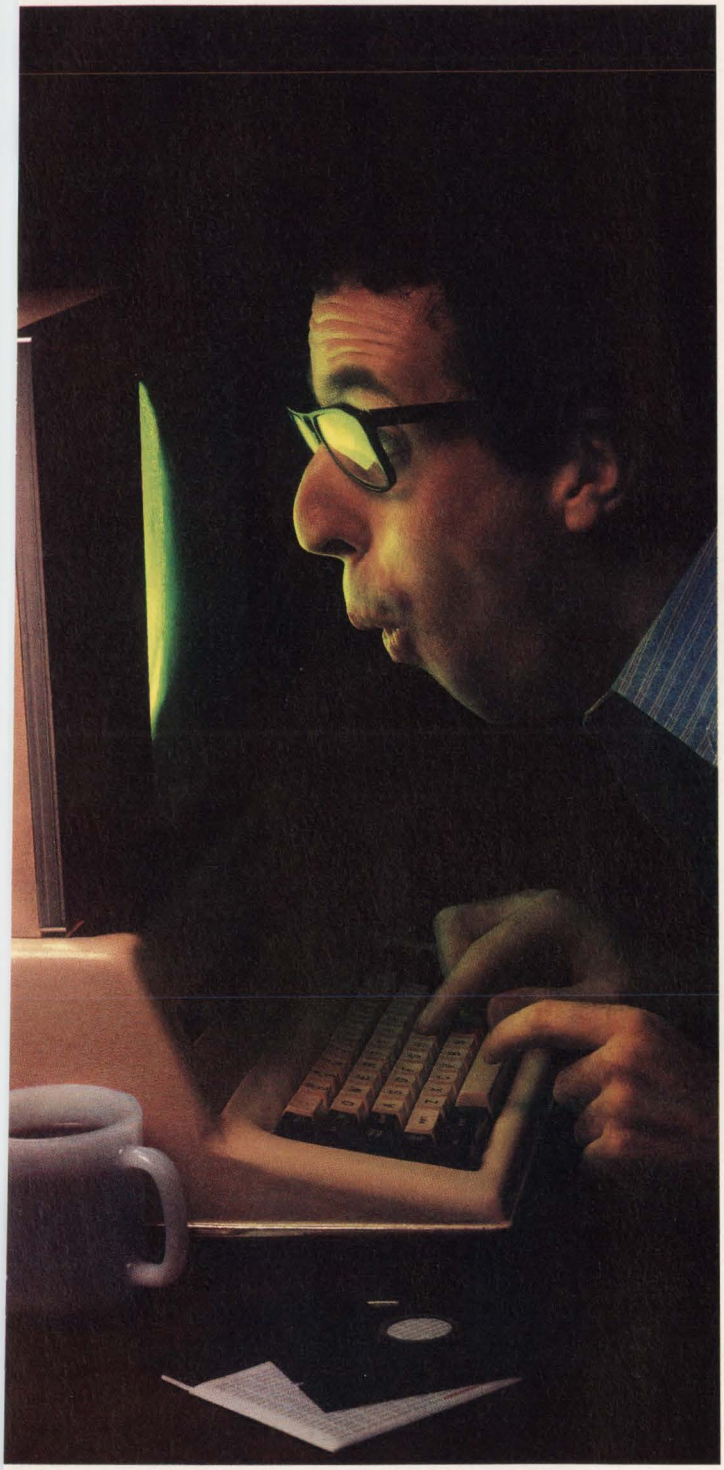

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CIRCLE 75

Hitachi's

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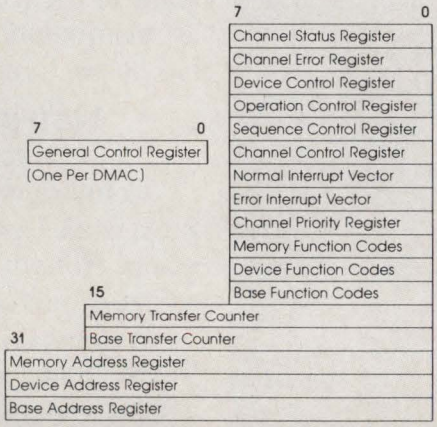

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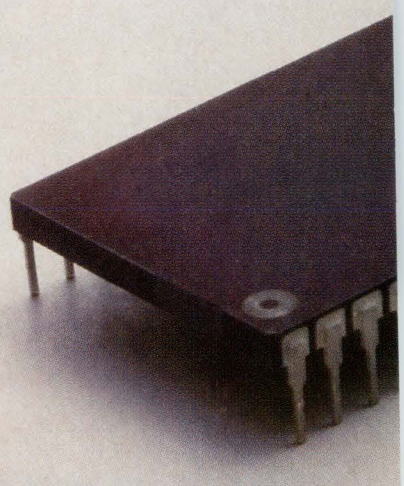

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CIRCLE 76

HIGH SPEED D-A CONVERTERS YIELD PRECISION GRAPHICS

Megasample-per-second chips improve resolution, precision, and flexibility of computer system displays.

by Randel R. Castleberry

Since the CRT is an analog device, digital computers that can display graphics information on a CRT terminal require a D-A converter. The D-A converter decodes the information in the computer's binary data output and translates it to an analog voltage or current. This current determines the display brightness at any point on the screen. For color graphics displays, three separate D-A converters are required—one each for the red, green, and blue portions of the composite video signal.

Until recently, designing a high resolution graphics display system meant using discrete components or complex and costly multichip hybrids to provide the composite video signal. Now, however, there is a high speed D-A converter that has buffer amplifiers, video synchronization, and blank insertion circuitry on a single monolithic chip. All this is in addition to the usual D-A conversion circuits found onchip. For computer system designers, this chip means a simpler, more reliable system design, shorter design time, greater miniaturization, reduced power dissipation, and reduced design and manufacture cost.

Randel R. Castleberry is a senior engineer at TRW Electronic Components Group, La Jolla, Calif. He holds a BA in mathematics and physics and a BS in engineering.

As computers become more sophisticated and handle higher operating speeds (see *Computer Design*, Sept 1984, "Parallelism Makes Strong Bid for Next Generation Computers," p 104), the number of applications for computer-driven graphics displays increases. These applications will require greater flexibility, resolution and precision, and that means the process of converting digital data to analog must be accurate and fast. The performance of D-A converters for these applications is usually measured in megasamples/s. So, with its 8-bit format and conversion rate of 125 megasamples/s, the TDC1018 D-A converter is suited for high precision and high resolution systems (see Panel, "A versatile graphics technique").

Raster scan display

Most computer graphics systems use a raster scan similar to that used for television video screens. In this design, the video signal output from the D-A converter must be combined with synchronization and blanking signals to produce the correct display. Fig 1 shows the basic characteristics of the composite video signal for a display system using the NTSC standards for television broadcast. Most computer-controlled graphics systems are designed around these standards.

For the raster scan, a synchronization pulse is required at the start of each horizontal line. The video signal is blanked at the end of each line during the retrace time. The screen is also blanked at the

A versatile graphics technique

Graphics technology is always moving toward higher resolution, wider dynamic range, and increased versatility in its images—in short, toward more realism. Digital signal processing (DSP) is one method used to achieve this realism. For example, for many years, DSP techniques have been used to enhance images taken of natural phenomenon by space probes or satellites.

In this DSP application, the raw image data is computer processed and displayed on a CRT screen. The image displayed is an abstraction of a real image and usually does not have the best "mix" of information for all applications. DSP allows the user to enhance the image by emphasizing wanted information and deemphasizing that which is unwanted. In some cases, missing information is restored by interpolating or extrapolating from the known data.

There are many other uses for DSP. The intensity of the image of part of an operating IC observed through an electron microscope is dependent on the voltage potential at that part of the circuit. This property might be useful for determining the voltage at any circuit node. The voltage resolution desired may be hard to achieve with a simple "gray scale" of intensities.

To improve this situation, DSP can be used to enhance the image such that a wide variety of colors represent the narrow voltage range of interest. The resultant data is therefore much easier to interpret.

Contrived images, such as a three-dimensional computer aided design display, can also benefit from DSP techniques. One common DSP chore is spatial antialiasing. This procedure removes the jaggies from image boundaries and is the most common DSP use in graphics technology. Other possibilities for DSP in graphics image enhancement include linear and nonlinear filtering, interpolation, shading, texturing, and compression/expansion.

end of the raster scan while the trace is returned to the first line for the start of the next frame. Screen blanking takes slightly longer than signal blanking. In a color system, the "reference white level" shown in the figure represents the maximum intensity of either red, green, or blue.

In the standard RGB color video system, graphics resolution is specified in terms of a matrix of picture elements (pixels). A pixel is the smallest controllable brightness increment. For example, a resolution of 1024 x 2048 means a display of 1024 horizontal lines, where each line contains 2048 light dots. If the screen is updated 60 times/s, about 125 million pixels must be generated per second (about one every 8 ns).

Another important factor in computer color graphics is color resolution. In theory, an infinite number of color tones and shades are possible by combining the three colors in all possible combinations and all intensity levels. However, in practice, there is seldom, if ever, any need to exceed the resolution capabilities of the human eye. For example, in an 8-bit system, it is possible to provide 2^8 or 256 intensity levels for each of the three colors. The total of 2^{24} or nearly 17 million colors and shades far exceeds any conceivable requirement for a practical system. A simpler design, and one that presents high quality displays, provides 16 intensity levels per color for a total of 4096. A display with this color palette and a resolution of 1024 x 1280 pixels provides realistic graphics. Such systems are suitable for applications such as flight simulators and cinematography.

A color graphics raster scan system can operate as an intelligent peripheral to a host CPU (Fig 2). The CPU can download most of the processing required for the graphics display to the programmable microprocessor. The display data is stored in digital form in the RAM and then supplied to the D-A converters, one for each color, through buffers. The D-A converters, in turn, drive the three intensity grids of the color CRT.

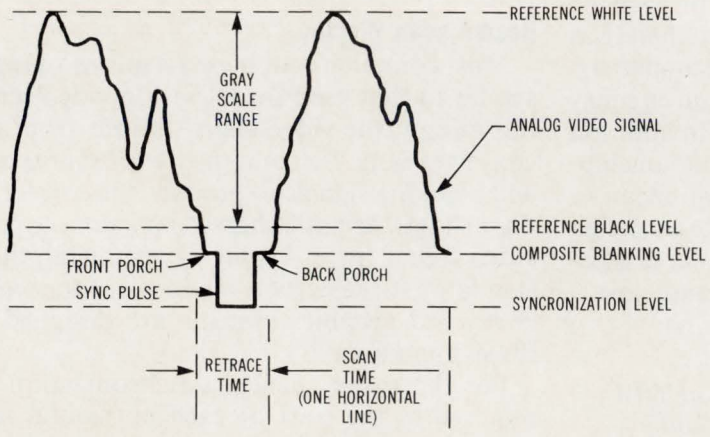
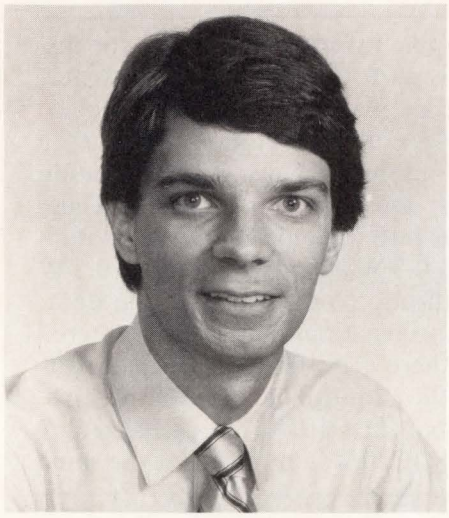


Fig 1 A composite waveform accommodates video, blanking, and synchronization signals for two horizontal lines in a raster scan system. A blanking input drives the video output into the "blacker than black" region so the horizontal retrace is invisible.

Central Data is Multibus* I/O Control



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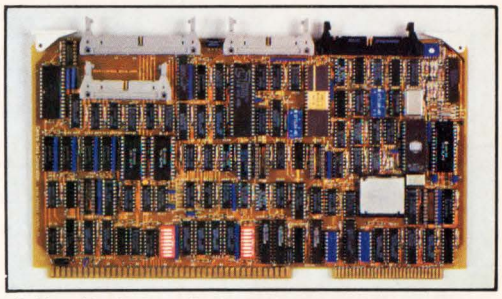
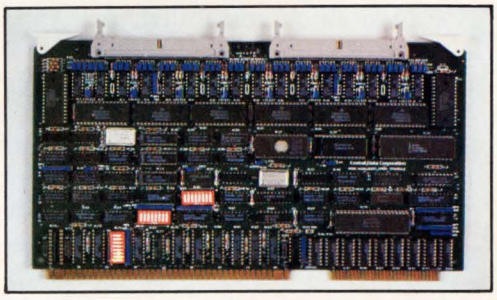


The new **Multibus Multi-Media Controller** is the industry's first to support up to 12 storage media — four each 5¼" Winchester disks, floppies and QIC-02 streaming tape drives, and at an economical price. On-board buffers provide 1:1 interleave transfers and the board supports both bus-vectored and non-bus-vectored interrupts. The board self-tests internally and corrects up to 11-bit burst errors with a 32-bit ECC for Winchester drives. For even greater performance, an optional iLBX* DMA interface is available with the board's (80188) 8/16-bit processor. The **B1030** is available in 100 up pricing at $895.



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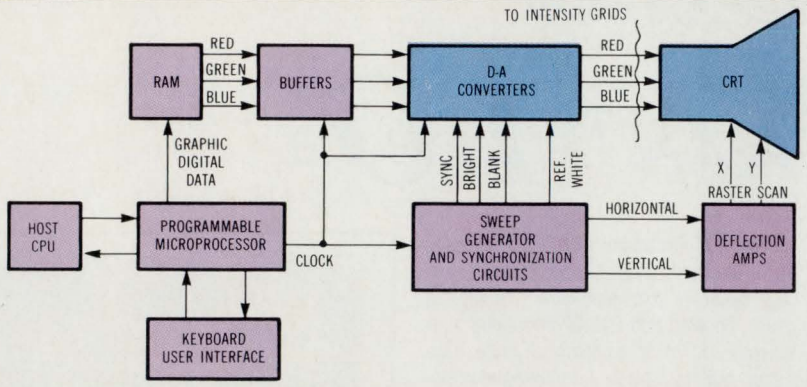

Fig 2 A raster scan color graphics display can operate as a host CPU peripheral with a programmable microprocessor and an interactive keyboard interface. Graphics digital data is ROM-stored until it is clocked through buffers to a D-A converter set where it is decoded.

The X- and Y-axis CRT deflection is controlled by the sweep generator and synchronization circuits. These also provide the synchronization pulse, blanking, and reference white inputs to the D-A converters. Data transfer from the RAM through the buffers to the D-A converters, as well as the timing of the sampling processes in the D-A converters, is system clock controlled.

Monolithics are better

The availability of a graphics ready monolithic D-A converter chip has important implications for the system designer. The term graphics ready means that nearly the entire process of converting digital data to analog graphic information, ready for display on the CRT, is performed onchip. In essence, the chip looks like a "black box" to the designer.

As stated, the D-A converter eliminates the need for separate buffer amplifiers, video synchronization and blank inserters, and deglitching circuits. These circuits are all built into the chip whose maximum power dissipation is 0.8 W and approximately 0.5 W in most configurations. Note also that the data, blanking, and synchronization inputs are all entered synchronously so there is no need for special software to control the timing of these functions. Fig 3 shows the 8-bit, TDC1018 D-A converter. A 4-bit version, the TDC1034, can perform the same

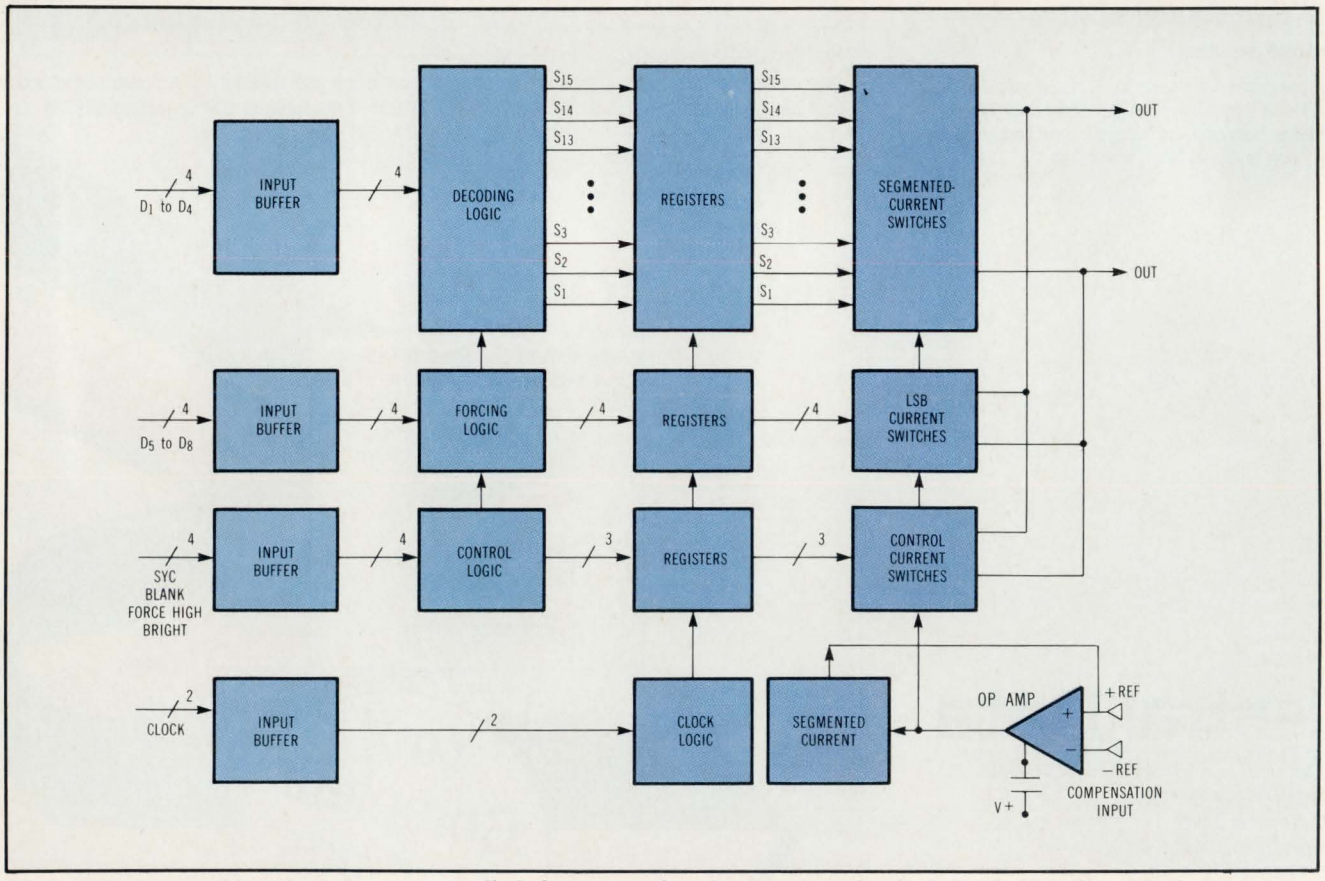

Fig 3 The D-A converter's design ensures glitch-free processing. Its digital section includes buffers for eight input control lines, decoding logic, clock, and register circuitry. The analog portion has linear current switches and op amps for buffering and switch driving.

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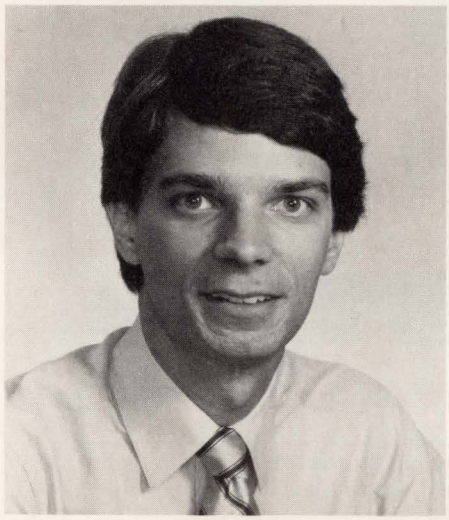

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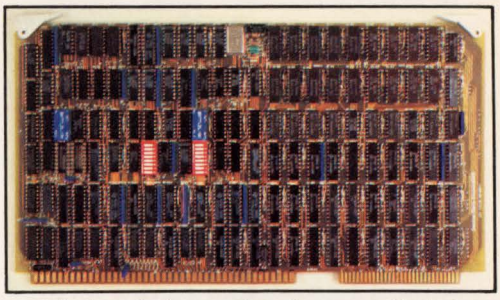
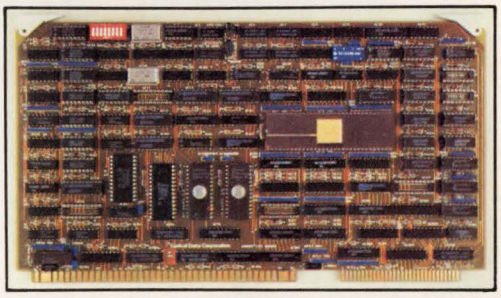


The new **Multibus iLBX* Cache Memory Board** delivers processor independent, high speed memory through the iLBX interface on the Multibus. The board's unique cache memory images the entire Multibus memory using a two-set LRU caching algorithm and stores 4K bytes of the most recently used memory. Access time is under 100ns, much faster than any dynamic RAM board. This new board also features write through operation, extensive error checking, and automatic and invisible deselection on error with interrupt. Its forced miss mapping allows use with dual-port memory on the Multibus. The **B1041** is available in 100 up pricing at $1145.



The new **Multibus 12.5 MHz 68000 CPU** also takes advantage of the iLBX architecture by allowing connection to the Cache Memory Board or to dual port iLBX memory. The board's central processor is the powerful 68000 or optional 68010 and features paged SUN memory management. It supports 8 Multibus interrupt levels in either the bus-vectored or non-bus-vectored mode. The board has three programmable timers and two EPROM sockets for monitor or bootstrap programs. Its full multi-master capabilities allow the use of several processor boards and DMA devices on the bus at one time. The **B1045** is available in 100 up pricing at $975.

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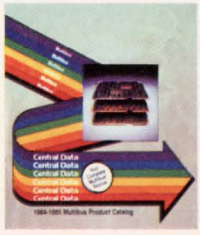

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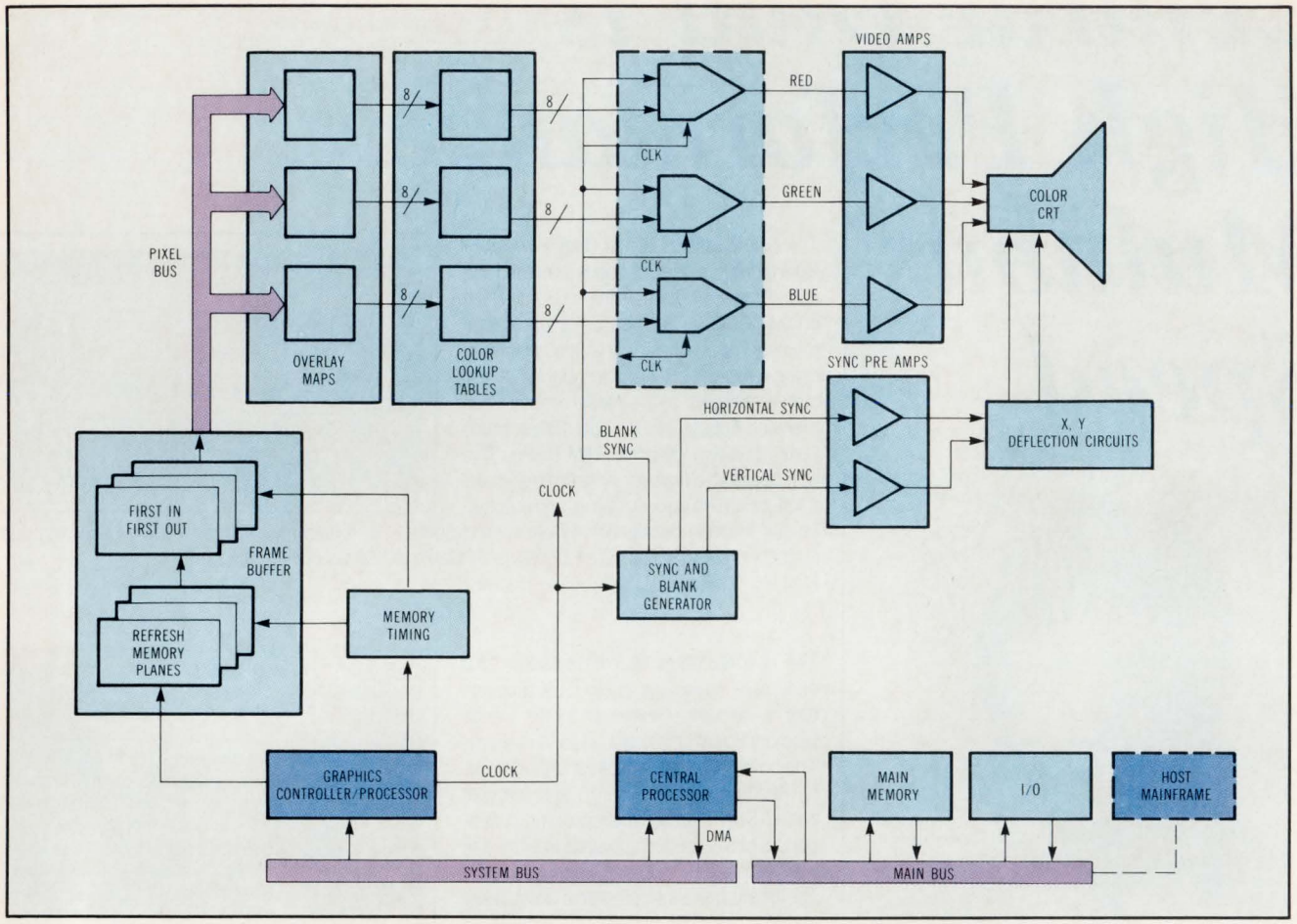

Fig 4 A precision, high resolution graphics system (standalone or with a host mainframe) can use three D-A converters. Overlay maps allow the setting of color precedence in simulated three-dimensional displays. Color lookup tables provide addressable maps of all possible color combinations.

operating speed and resolution. Both the 8- and the 4-bit D-A converters are available in standard DIP and cerDIP packages of 24 and 18 pins, respectively.

The D-A converter's five basic stages include input buffers, decoding and control logic, clocking and register circuits, an op amp, and a bank of current switches. The input buffers are compatible with ECL, and translate the data and control inputs into current-mode logic. The chip uses differential decoding logic for high speed and minimum noise. Control inputs, in addition to the synchronization and blanking signals, include a force high input that can be used to set up a standard white level for test and calibration. There is also a bright input that creates a "whiter than white" output for use in highlighting cursors, messages, or menus.

The D-A converter also uses differential clock circuitry to reduce clock signal feedthrough at higher speeds and to improve the spectral purity of the clock in noisy areas. Other important features include an internal op amp that buffers the reference current and drives the output current switches. These switches are configured to ensure glitch-free signal transfers.

An important contribution to glitch-free operation is the proprietary decoding technique that converts the four MSBs of a data word to a 15-bit word. That word is placed in a register where it is added to the four LSBs of the same word. This design eliminates a common source of glitches at midscale transitions. These occur, for example, when the digital input changes from 10000000 to 01111111. In the 19-bit code used, only 1 bit changes at the midscale transition. Registering the data after decoding achieves further glitch reduction and minimizes data skew.

More designer benefits

Video output levels from the TDC1018 are consistent with 8 bits of accuracy and are well within the ±5 percent tolerance permitted by most video system standards. Both normal and inverted video outputs are provided. As a bonus, the D-A converter provides multiplication capability even though this is not usually a demand in video D-A converters. This capability can be used in designs where gain correction and level scaling are needed. The converter can perform linear multiplication over a range of ±5 percent at speeds up to 1 MHz when the internal amplifier is augmented by an external high speed op amp. An analog output line included in the feedback loop of the op amp helps to achieve

precise amplitude stabilization. This configuration is suited to auto-calibration of system gain and scaling levels.

The number of bits/pixel determines the color resolution of a graphics system. In a typical high resolution graphics system using three TDC1018s (Fig 4), there are 8 bits/pixel. This specification dictates the number of memory planes required in the frame buffer—one per plane/bit. Eight bits/pixel means that any one picture element can consist of any one of 256 different shades and colors. The frame buffer is a high speed multiplexed memory that can store a complete frame or raster of graphic data in digital form. The refresh or update rate is 60 frames/s.

Color graphics

Pixel data from the frame buffer is routed serially to a set of overlay maps and color lookup tables. The overlay maps provide the means for setting color precedence for simulated three-dimensional graphics. For example, if some parts of the red and blue portions of a frame overlap, the overlay map is programmed to mask the blue so that the blue plane appears to be behind the red plane in the presentation.

The color lookup tables provide the means to address some specific portion of the total color range for each of the three basic colors. Because the design is an 8-bit system, red, green, and blue each have 256 different possible addresses. As a result, for any pixel in the raster, there is a choice of 256 colors and shades (selectable from anywhere within the total range of nearly 17 million). The addresses are under control of, and may be changed by, the system software.

The graphic system is under the control of a graphics controller/processor. A central processor handles all the calculations and data processing required to generate the graphics display in digital form. Programs and data files are stored in main memory and can be written to disk or tape through an I/O interface. This interface also provides user interaction through a keyboard and connects the system to offline peripherals such as printers and plotters.

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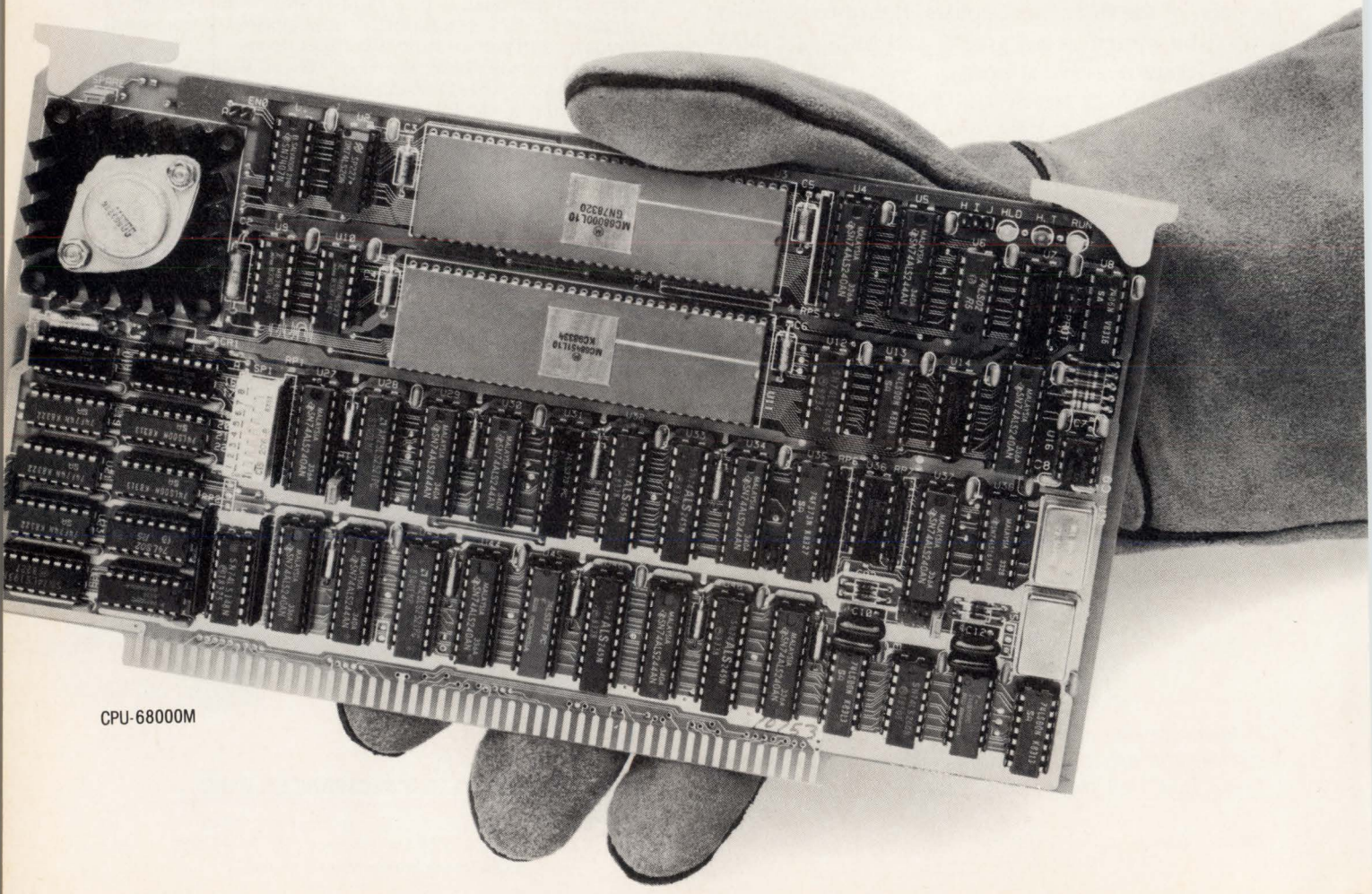


CPU-68000M

CIRCLE 80

FORTH EFFICIENCY BLENDS WITH C AND PASCAL SYNTAX

A programming language developed for hardware designers combines interactivity with a structured, maintainable syntax and brings universal abilities to popular operating systems.

by Arnold Epstein,
Jeffrey D. Morris,
and Barry Unger

Some modern computer languages such as Pascal and C are structured to encourage better programming and documentation. Others such as Basic, are interactive and easy for the beginner to learn. Another popular language, Forth, is both interactive and extensible. The virtues found in each of these languages point out the need for a single language that combines many of their best features.

The computer language Magic/L can provide the right mix of such features since it combines interactivity with a structured, maintainable syntax. Influenced by Forth, it brings a Forth-like efficiency to hardware development but has a syntax similar to the C and Pascal programming languages. It is available for computers using CP/M, MS-DOS, RSX-11, RT-11, and various M68000-based Unix Systems.

Arnold Epstein is president of Loki Engineering, Inc, Cambridge, Mass. He holds a BS, MS, and PhD in physics.

Jeffrey D. Morris is vice president of Loki Engineering, Inc. He holds a BA in physics.

Barry Unger is chairman of Loki Engineering, Inc. He holds a BS in engineering and humanities, a BS in management, and a PhD in administration and planning.

A hardware design environment

Software is often written by hardware designers for the sole purpose of testing and debugging hardware as it is developed. Such software represents overhead in the design process because it is usually created only for one specific hardware configuration. Thus, it is likely to be used only once and then discarded or forgotten. With traditional programming environments such as assembler, Pascal, or C, the creation and use of this code tends to be especially awkward and time-consuming. When the hardware does not work on that first test, as is almost always the case, a cumbersome process of program modification is required to determine whether the problem is in the hardware or in the software that tests it.

The software used for debugging and testing should be easy to write, read, and document. Ideally, it should also be usable for other purposes. The Magic/L language and programming environment supports all these objectives. This interactive software tool was designed to allow programming to be a spontaneous, creative process, freeing the user to concentrate on hardware design. Experience with the language in such areas as image processing and analysis, graphics display, and data acquisition demonstrates that hardware developers become more productive because many of the problems imposed by traditional programming languages are eliminated. In addition, the language can be extended to provide a diagnostic environment, as well as a base

language for the tailoring of end-user oriented command languages.

A natural reaction to the creation of yet another computer language is to question whether it is really necessary. There are enough drawbacks to most languages that a case can be made for something better. While each language has its strengths, each also has deficiencies that diminish effective support for the design process.

Another language

Compiled languages such as Fortran, Pascal, and C are easily readable, and the superstructure (the tying together and sequencing of subprograms) is quickly accomplished. But these languages have two major disadvantages. First, as compilers, they require that when a code is changed (however slightly—eg, changing a variable name), it must be edited, compiled, linked to the necessary system libraries, and then executed—hardly the kind of flexibility and quick response required for creative design. This is especially true for the designer who wants to engage in rapid cycles of "try something...see how it works...now change it...and see how that works." Nor is it useful for debugging hardware configurations in a reasonable amount of time. When hardware that is being tested does not do what it is supposed to do, it is difficult to detect whether the error is in the code or in some device or part of the hardware that did not work correctly. At worst, the error may be found only by systematically altering the software and the hardware little by little and checking the results with, for example, an oscilloscope. Traditional compiled languages require that each step of this trial-and-error process at the keyboard be accompanied by recompilation of the entire code, and this procedure can add hours, even days, to the debugging process.

Second, high level compiled languages generally offer little access to the machine level, which is often required for "tweaking" or examination and modification of specific memory locations corresponding to device inputs or display pixels. Consequently such access, an important part of the hardware debugging process, is achieved only by writing separate subroutines in assembly language. Because the subroutines are not integrated with the main program written in the high level compiler, it is difficult for the subroutine to access or specify the same global variables used in the main program. Program development and debugging is also awkward because each test and change requires frequent repeating of the entire procedure of "edit/compile/link/run," including linking in the assembly language subroutine.

Basic was developed in the late 1950s as a simplified teaching language. Its purpose was to accommodate first-time computer users by requiring them them to grasp only a small vocabulary. It also provided a high degree of feedback to the student at the terminal, thus simplifying the effort required to write code that runs successfully. That is, it was interactive, providing the ability to immediately execute changes as they were made, rather than having to compile and link.

To achieve simplicity, Basic sacrificed the flexibility and efficiency producing features important to the serious language user. Thus, most versions of Basic are nonstructured, lack user-defined record structures, and have significant syntax limitations, such as in the choice of subroutine or variable names. Control is accomplished mainly by user-developed *ad hoc* sequences of GOTOs to various numbered lines dispersed throughout the body of a program, rather than through more modular or stylized structures like the "WHILE REPEAT" forms found in C, Pascal, and other high level compiled languages. Subroutine (eg, GOSUB) and command calls in Basic must usually refer to numbered lines of code rather than to named subroutines and commands. Argument passing must be done explicity (eg, "X = 5" and "Y = 6") using the same variable names as in the subroutine rather than as arguments to the call.

This interactive software tool allows programming to be a spontaneous, creative process, freeing the user to concentrate on hardware design.

The interactivity and user feedback that are such attractive features of Basic are, unfortunately, accomplished through the mechanism of "interpreting" (ie, recognizing and translating each line of code at run time without precompilation) rather than through compiling code. This procedure greatly slows the execution speed. For example, after each increment in an iteration or do loop, the same Basic code must be recognized and translated again. As with many high level compiled languages, Basic is also removed from the machine level. So, to access the hardware at the byte and bit level, as is often required in hardware applications, the user must use separate assembly language subroutines, thus diluting the advantages of interactivity. Finally, in most versions of Basic, external subroutine calls are not allowed, meaning that even the awkward use that high level compiled languages make of separate assembly language subroutines is not feasible.

Because of such difficulties, the hardware developer is frequently forced to program in assembly language. Although this allows access and control of the hardware at the machine level, even simple terminal I/O can be painful to implement this way. It is not easily readable; because it is not interactive, much time is wasted coding the superstructure. Developers often use simple monitors such as ODT

TABLE 1

Comparison of Magic/L to Other High Level Languages

	Magic/L	Basic	Fortran	Pascal	C	Forth
Interactive	Y	Y	–	–	–	Y
Structured	Y	–	–	Y	Y	Y
Forward notation	Y	Y	Y	Y	Y	–
Extensible	Y	–	–	–	–	Y
Complex data structures	Y	–	–	Y	Y	–
Access to system calls	Y	*	*	*	Y	–
Built-in assembler	Y	–	–	–	–	Y

*System dependent

or MACSBUG for direct access, even though this may cost them the ability to easily generate simple looping or conditional constructs. So we come full circle to the need for a high level language that has the interactivity and access to the machine level so important in hardware design.

Examining the incremental compiler

Invented about 15 years ago, forth would seem to answer most of these needs and, indeed, can be very effective in the hands of those willing to live with its shortcomings. Forth allows direct machine access through a built-in assembler, a major advantage to the hardware designer. Most significantly it is an "incremental compiler."

In an incremental compiler, each line is compiled as it is entered at the keyboard or from a file. As soon as the compiler determines that a complete syntactic structure has been entered and compiled, the code is executed and the compiler waits for additional syntactically complete code to execute. This is a major advantage because it makes programming spontaneous: everything that is entered at the keyboard has an immediate effect. This feature can dramatically alter the way programming and debugging are done, in effect following the incremental, interactive flow of human thinking. For example, code can be typed in, put into a do loop, and tried successively with ten different values, all without the tedious process of waiting each time for the whole program to recompile and link.

Forth actually contains a very limited amount of predefined syntax and functions but still provides extensibility. That is, function extension statements are used to define the additional functions necessary for programming in a specific task domain. In the hands of a talented programmer, Forth becomes a powerful mechanism for creating a "language within a language" customized for a particular problem or application area.

Unfortunately, Forth has a number of problems in readability, ease of modification, and maintainability. Some of these are inherent since they are related to the strengths discussed above. Forth requires the use of reverse Polish notation rather than algebraic notation. Also, the programmer must keep track of stacks because, to provide a compact compiler, Forth uses the programmer as the front-end to the compiler. Many programmers have found that these features make it difficult to modify their own code later, and to read and understand Forth code that others have written.

Extensibility is a useful feature for handling an occasional special procedure that must be repeatedly specified. But the Forth strategy of providing only a small set of predefined syntax and functions, then relying on the user to create the appropriate functions for a given task, leads to communication problems. This is especially true where teams of programmers are involved. Each user is in effect forced to write a new "dialect"—define a set of functions and elements of syntax such as appropriate record structures—whenever programming in Forth. This impedes programmers trying to read or modify their own code or that of others. When function extensions must be so heavily used, one programmer's necessary extensions can become another's nightmare. Because this problem can be so severe, some programming managers have dubbed Forth a "write-only language."

An interactive environment

In developing Magic/L, the goal was to create a productive programming environment that combined the best features of each of the major languages used in hardware development while remedying many of the deficiencies. Magic/L provides the interactivity of Basic and Forth. It has the readability, maintainability, and other useful functions, such as user-defined record structures, that are found in such structured high level compiled languages such as Pascal.

Major features include user-defined data types (for record structures), type checking in expressions, forward notation, full interactivity through an efficient incremental compiler, and a variety of interactive

programming aids. Other features include mixed mode checking, control structures, user-defined data structures, a system independent I/O package, formatting output facility, and dynamic allocation of local variables.

A resident interactive assembler that does not require additional linking is integrated into the Magic/L programming environment for whatever host is used. Unlike Forth's built-in assemblers, which use reverse Polish notation, the built-in Magic/L assembler takes the form of the CPU vendor's assembler. Thus, Magic/L provides the extensibility offered by Forth, and readability and other features oriented to the designer, such as user-defined command syntax. Table 1 compares the features of high level languages.

Programming does not have to proceed based on untested assumptions about what the hardware can and cannot do.

From the project manager's viewpoint, an additional advantage of the interactivity and access to the machine level is that it is easier to keep development efforts attuned to hardware realities. Programming does not have to proceed based on untested assumptions about what the hardware can and cannot do. Problems are less likely to develop in such areas as handshaking with I/O ports or separate processors, or low level protocols.

When you must use assembler

The most common reason why programs are written in assembler is that a small percentage of the program requires it for hardware access or efficiency. Consequently, the whole program gets written in Assembler. In contrast, Magic/L with its built-in assembler allows programmers to write the whole program in high level code, identify the bottlenecks, and, if necessary, rewrite just those problems in assembly language (Table 2).

It is easy to quickly identify the slow running parts of a program. For example, one could enter:

```
ITER 10000
[The name of the routine to be benchmarked goes here]
LOOP; ;BEEP
```

Then the speed of the routine can be timed using the second hand of a watch. This kind of testing is not easily done on Pascal or Fortran. However, designers using Magic/L are encouraged to use this capability regularly, benchmarking software as they write it.

For hardware designers who need interactivity, Magic/L is an attractive alternative to Basic. It executes much faster, has better high level constructs, allows access to the machine when needed, and provides access to operating system specific facilities. Magic/L includes commandline recall and edit, text file editing, and command execution facilities. These features, including the interactive language, are available without leaving the Magic/L environment. Some of the language features included are data typing for CHAR, INTEGER, LONG, REAL, and string data. User-defined records allow specification of arbitrarily complex data structures. A complete I/O package provides random access, variable length I/O to any file.

A program example

Traditional compilers and assemblers introduce significant software overhead into the hardware development process. Each time the hardware designer requires a new routine, four steps must occur. These are, in order: enter the source text (1), assemble (2), link (3), and run the program (4). Steps (3) and (4) are overhead. In addition, any functionality in the program beyond the actual test routine (eg, menu

TABLE 2

Interactive Assembler in the Magic/L Environment

Consider the high level code for TRIP, a function that returns three times its input value.

```
DEFINE TRIP INTEGER
        INTEGER IVAL
  TRIP := IVAL * 3
END
```

To achieve greater speed, the above function may be replaced by the equivalent assembly code. Below are the equivalent routines for various Magic/L interactive assemblers.

PDP-11 Assembler

```
entry trip integer
  mov     (r5), r0
  add     r0, r0
  add     r0, (r5)
  next
```

M68000 Assembler

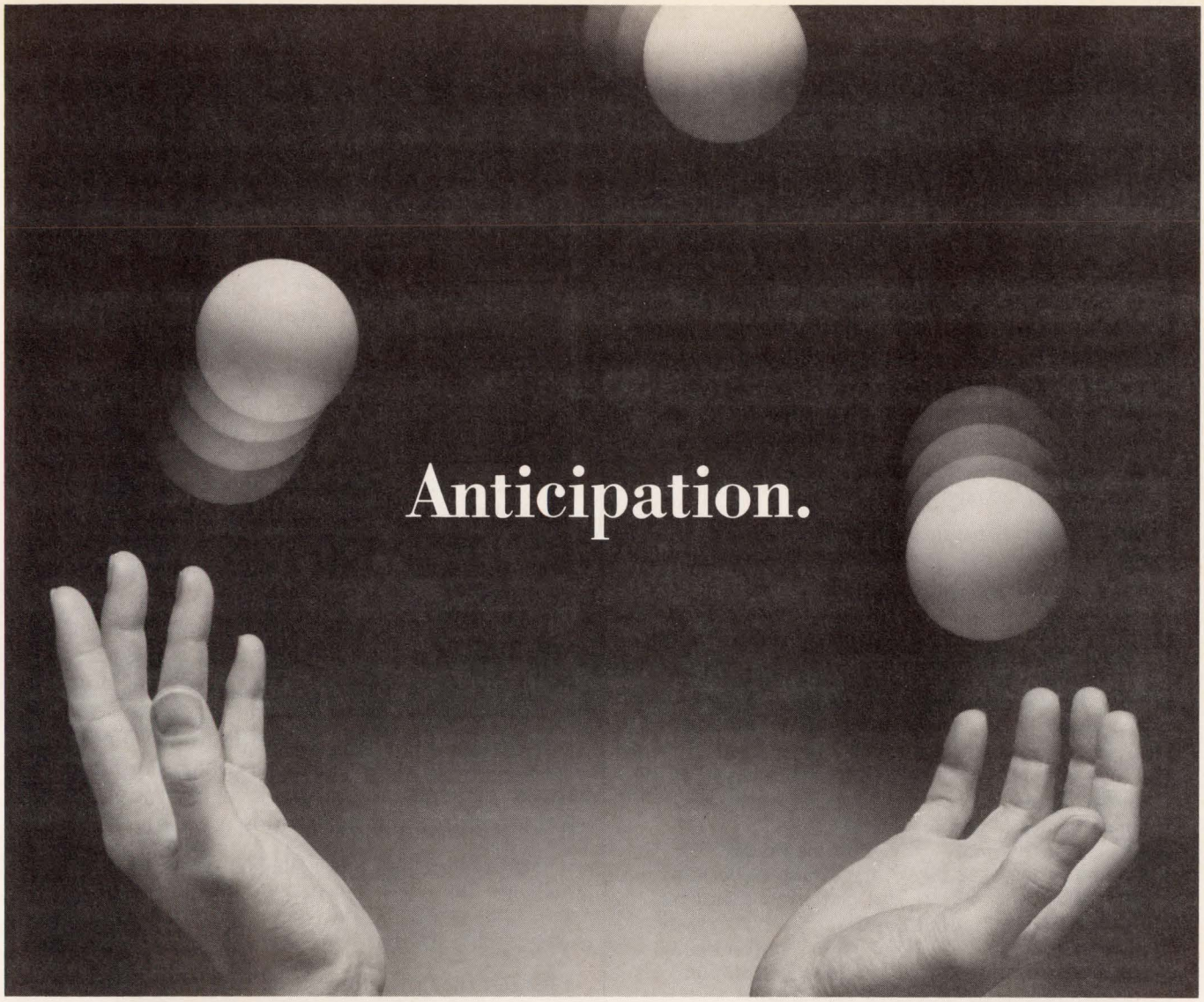
```
entry trip integer
  move.w  (a5), d0
  add.w   d0, d0
  add.w   d0, (a5)
  next
```

8080 Assembler

```
entry trip integer
  pop     d
  lxi     h 0
  dad     d
  dad     d
  dad     d
  push    d
  jmp     next
```

8086 Assembler

```
entry trip integer
  pop     ax
  mov     bx , ax
  add     bx , bx
  add     ax , bx
  push    ax
  jmp     next
```



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CIRCLE 81

or command selection, inspection of data) must be explicitly coded, thus diverting resources from the task at hand. Magic/L eliminates software overhead, allowing the primary focus to be edited off-line or entered directly from the keyboard. Once entered it is ready to run. Any existing routine can be run any time, all values can be displayed, and new routines can be added as the need arises.

Although the language excels at high level constructs, it has the ability to do the kind of register manipulation needed for hardware development. The Panel, "Defining device interface code," shows a section of code that formally defines a device interface and serves as a setup for the programming example. The setup could be entered by keyboard or previously defined in a file.

The interactive programming example chosen to demonstrate Magic/L is the testing of a camera stand interface. The motorized camera stand consists of a moving platform, which can be stepped up or down under computer control. Switches at the top and bottom of the stand indicate to the computer when the moving platform has reached the end of its travel.

In this example, a camera stand interface has just been installed in the computer and the engineer must perform the initial testing of the hardware, normally a frustrating and time-consuming process. Magic/L will provide the direct access and immediate feedback needed to test and debug problems quickly. The special prompts indicate the level of nesting as control structures and definitions are entered.

Before starting, a log file is created so this dialog will not be lost.

```
mgl>logon test.log
```

First test the upper limit switch. If ?top returns zero, the switch is not activated.

```
mgl>print ?top
      0
```

Holding the switch by hand should change the status:

```
mgl>print ?top
     -1
```

Now move the stage up one step:

```
mgl>mvup
```

If that works, try 10 steps:

```
mgl>iter 10
mgl>>mvup
mgl>>loop
```

Now try downward motion:

```
mgl>mvdown
```

If the platform does not move down, put it in an infinite loop to facilitate testing with a ' scope:

```
mgl>begin
mgl>>mvdown
mgl>>forever
```

Defining device interface code

Defining a device interface begins with the interface specifications. For a motorized camera stand, a "read-only" status register provides three bits of status information:

tls	The platform is at the top limit
bls	The platform is at the bottom limit
rdy	The motor is ready to be stepped

A "write-only" control register specifies the direction of the next step.

up	Move the platform up by one step
dn	Move the platform down by one step

The code for that interface follows:

```
; define the record structure of a memory mapped
I/O port record device_rec
    char devstat          ; status register
    char devctrl          ; control register
endrecord

; set the record base to the I/O page address of the
device & device_rec := <I/O page address>
; parameters of status register
parameter rdy := 1        ; device ready
parameter bls := 2        ; platform at bottom limit
parameter tls := 4        ; platform at top limit
; parameters of control register
parameter dn := 1         ; move platform down
parameter up := 2         ; move platform up
; Routines that return status conditions
; return TRUE if the device is ready
define ?ready integer
  ?ready := (devstat AND rdy) <>0
end
; return TRUE if the platform is at the top
define ?top integer
  ?top := (devstat AND tls) <>0
end
; return TRUE if the platform is at the bottom
define ?bottom integer
  ?bottom := (devstat AND bls) <>0
end
; Routines to move platform
; Wait until the device is ready
define wait
  begin until (?ready)
end
; move up one unit
define mvup
  wait
  devctrl := up
end
; move down one unit
define mvdown
  wait
  devctrl := dn
end
; end of required primitive routines
```

Assume the problem has now been corrected and escape from the loop with keyboard interrupt:

```
<control-C>
mg1>
```

Now define a routine to move up until a limit switch is found:

```
mg1>define top
mg1->while (NOT ?top)
mg1->>>mvup
mg1->>>repeat
mg1->>>end
```

Verify by immediately executing the new routine:

```
mg1>top
```

Write a routine to go to the bottom:

```
mg1>define bottom
mg1->while (NOT ?bottom)
mg1->>>mvdown
mg1->>>repeat
mg1->>>end
```

Verify:

```
mg1>bottom
```

By now it is time for the morning coffee break. We leave with the platform cycling up and down:

```
mg1>begin
mg1>>mvup
mg1>>mvdown
mg1>>forever
```

Since Magic/L contains elements from many languages and programming environments, it is not easy to categorize. Because of its built in assembler and its use of high level structures, it can be considered both a high level and low level language—equally adaptable to "top-down" or "bottom-up" programming. It is, strictly speaking, neither a compiler nor an interpreter, but something in-between—an incremental compiler. It is a general purpose interactive language that has been implemented to achieve the readability and ease of programming needed by designers.

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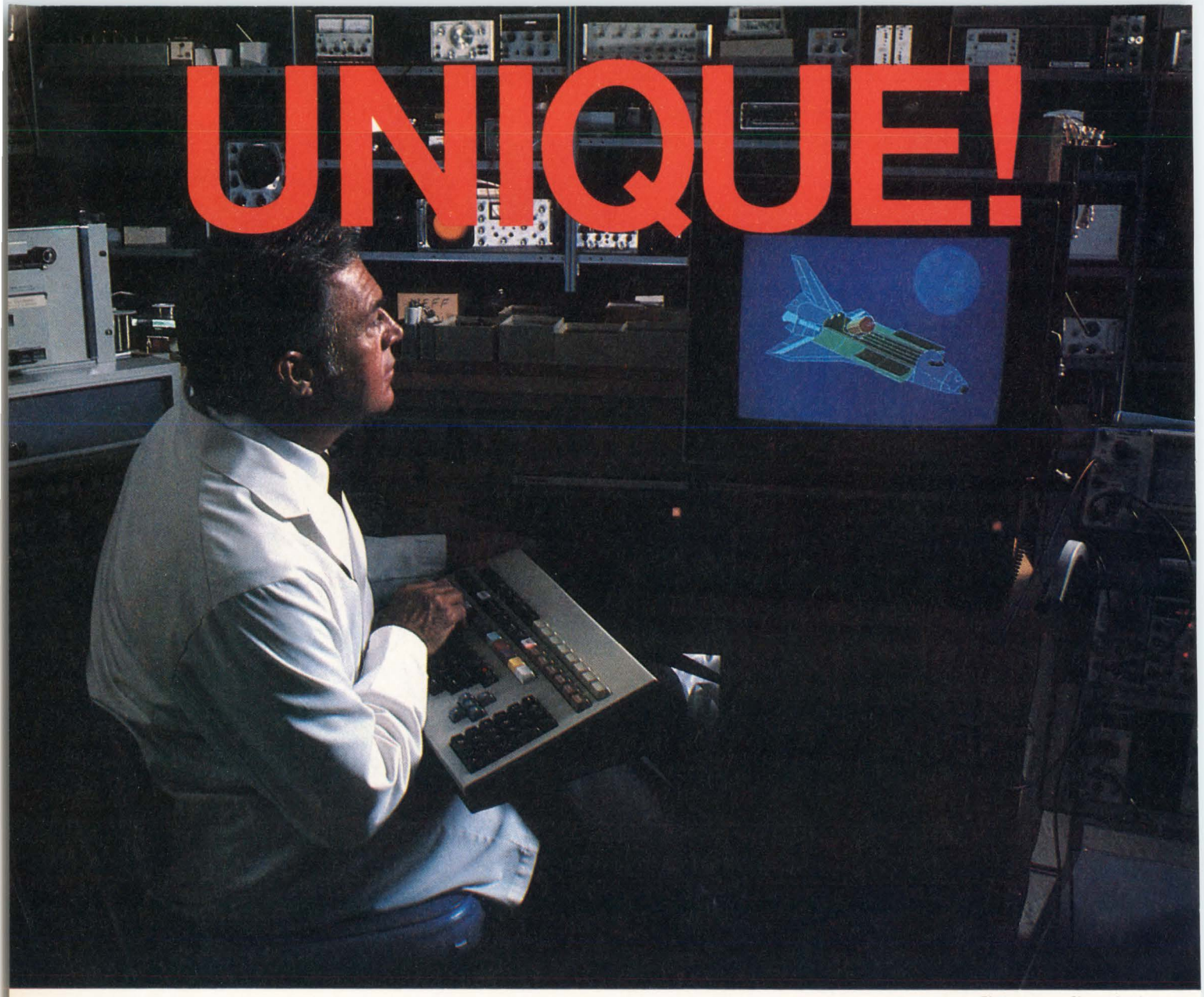

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TRUE FLOATING POINT BETTER AND BECOMING COST COMPETITIVE

VLSI floating point chips have made true floating point representation practical for many applications. Although block floating point is still less expensive, true floating point provides higher accuracy and a better dynamic range.

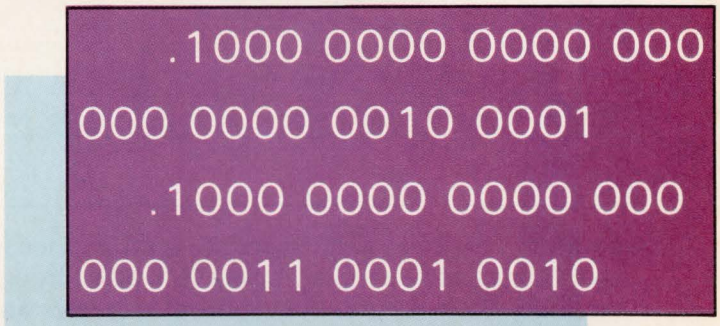
by Eric Hildebrandt and Edmund Y. Sun

Many scientific and technical applications require the accuracy and dynamic range provided by floating point representation. Until recently, however, true floating point systems were expensive, large, complex, and relatively slow. Only block floating point, a technique that provides a single exponent for an array or block of data, was possible for most applications. Realtime processing with true floating point was simply not practical.

Today, floating point multiplier and ALU chips (available from Weitek and other suppliers) make true floating point a practical alternative for many systems. These chips make true floating point faster, more compact, and less expensive than ever before. Block floating point systems are still less expensive because of their smaller memory width requirements. However, increasing memory density and the corresponding cost reductions have reduced the system impact of memory costs.

Eric Hildebrandt is an applications engineer at Weitek Corp (Sunnyvale, Calif). He holds a BS in electrical engineering.

Edmund Y. Sun, a co-founder of Weitek, is product engineering manager. He holds a BS, an MS, and a PhD in electrical engineering.



True floating point systems offer a number of apparent advantages over block floating point systems. True floating point systems are less dependent on system data input, and are more flexible because of greater accuracy and dynamic range. General-purpose computing systems use true floating point, making existing software algorithms available to the user. And, error analysis is data-independent and extensively documented for true floating point systems. All these factors can help the system designer decide whether or not true floating point is worth the extra cost.

The block floating point technique is a modification of fixed point arithmetic where a single exponent is assigned to a data array. After the array is scanned, its largest value determines the exponent and scale factor for the entire array. This ensures that at least one value (the largest) is normalized and has maximum precision. The exponent allows for a greater dynamic range than fixed point systems. However, arithmetic operations are still done in fixed

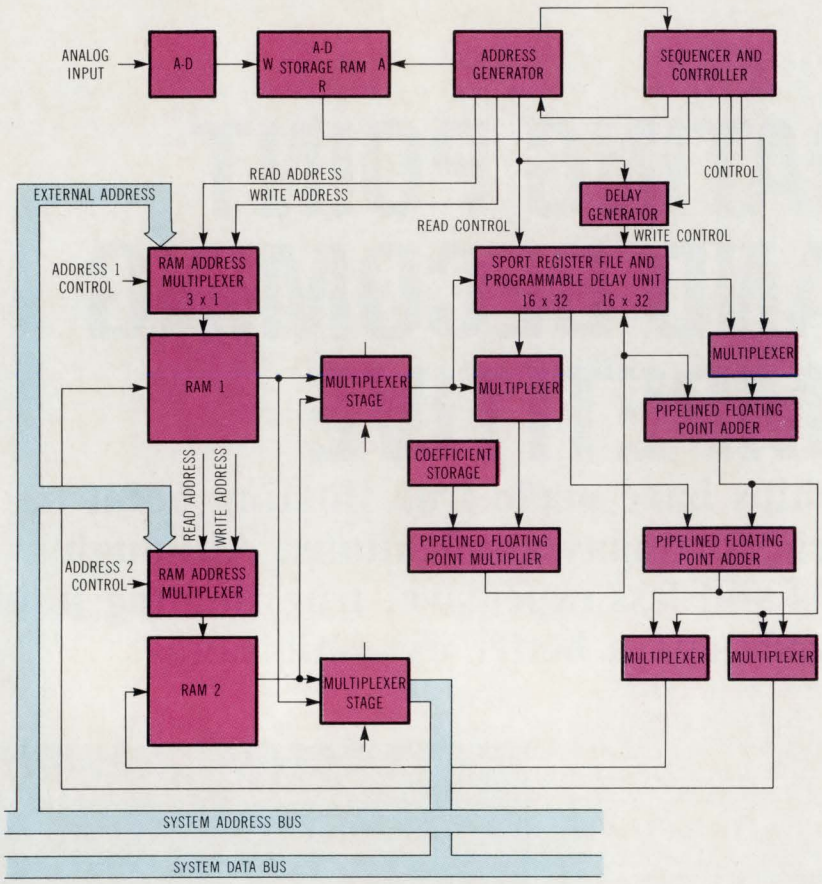


Fig 1 The full floating point design architecture handles a four-cycle butterfly for a fast Fourier transform (FFT) calculation. It can be used with VLSI chips and offers new flexibility to the digital signal processing computer designer.

point, because all values share the same exponent. Overflow must be checked during each pass through the array. If it occurs, the exponent increases and the entire array moves 1 bit to the right.

Note the difference

In a true floating point system, each value in the array has its own exponent. While this approach uses more memory, it ensures maximum precision and dynamic range because all variables are normalized. One example of a true floating point system is shown in Fig 1. In contrast, a block system is illustrated in Fig 2. These systems can handle general-purpose digital signal processing, but are best suited for fast Fourier transform (FFT) calculations. Thus, the main differences between them are data storage, memory width, overflow handling, and rounding logic.

The block system uses a multiplier and an accumulator. While this saves space and increases performance in FFT calculations, it is not readily adaptable to other applications. The true floating point system uses two ALU chips and is somewhat more flexible. The block system must have fixed prescaling in the A-D converter. This is because no shifter exists to prescale the data (although one could be added). While this feature saves hardware and processing time, the expected input data must be well-known to preserve system signal-to-noise ratio.

In the true floating point system, integer data from the A-D storage RAM is fed into the floating point ALU. There conversion to floating point is handled, maximizing input accuracy. Since a complex butterfly involves four multiplies, but only six adds, there are cycles available in the ALU for conversion (without interrupting the FFT calculations).

Both systems offer roughly the same performance in a FFT application, with a complex butterfly calculation done in four cycles. The programmable delay unit is a Weitek-made 32- x 32-bit multiport register file that stores operands for a variable number of cycles. The delay unit adds the desired delay to the write address when data is written into a file. As the read operation is sequential, the amount added to the write address determines how much time passes before the corresponding data is read.

The variable storage in the block system (Fig 2) is 16 bits wide. This reflects the lack of an individual exponent for each data item (and also a smaller mantissa) since 24-bit multiplier parts are not currently available. While it is possible to cascade multipliers to get 24 bits, such a design increases system complexity and cost, and reduces performance.

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CIRCLE 84

Since no individual exponents exist, a block exponent is added. This component is a counter that the microcode initializes and controls. The two-to-one multiplexer, added below the multiplier and accumulator, divides the result by two when overflow is detected. Normally, the multiplexer is set to pass the output.

In order to minimize quantization effects, some form of unbiased rounding must be used with the overflow logic. Quantization is the process of quantizing or rounding a number back to the number of bits which can be stored. This is often accomplished through a programmable logic array. For unbiased rounding, the two possible answers must be studied before the result can be rounded. Because chopping causes the error to be biased in the negative direction (numbers always get smaller), undesirable system effects could occur if unbiased rounding is not used.

In contrast to the block system, the true floating point data storage is wider (8 bits for the individual exponents and 8 bits of extra precision in the mantissa). The extra precision in the mantissa is used for the 32-bit IEEE arithmetic done by Weitek chips (24 bits of mantissa, 8 bits of exponent). Also note that the divide-by-two multiplexer, as well as the rounding and overflow logic, are no longer present: the floating point chips handle all of the floating point complexitiy (including overflow and unbiased rounding).

On accuracy

Since only one exponent is used in a block system, only one normalized value can be guaranteed. Operands that are not normalized may not be accurate. As a result, quantization has a larger effect on the calculations. For example, multiplication produces a result with as many bits of precision as the sum of the two inputs. But, the numbers must be quantized to prevent them from growing indefinitely.

Quantization errors—caused by this process—create more system noise. An unbiased rounding scheme rounds numbers to the nearest value. In cases where the unquantized number is exactly halfway

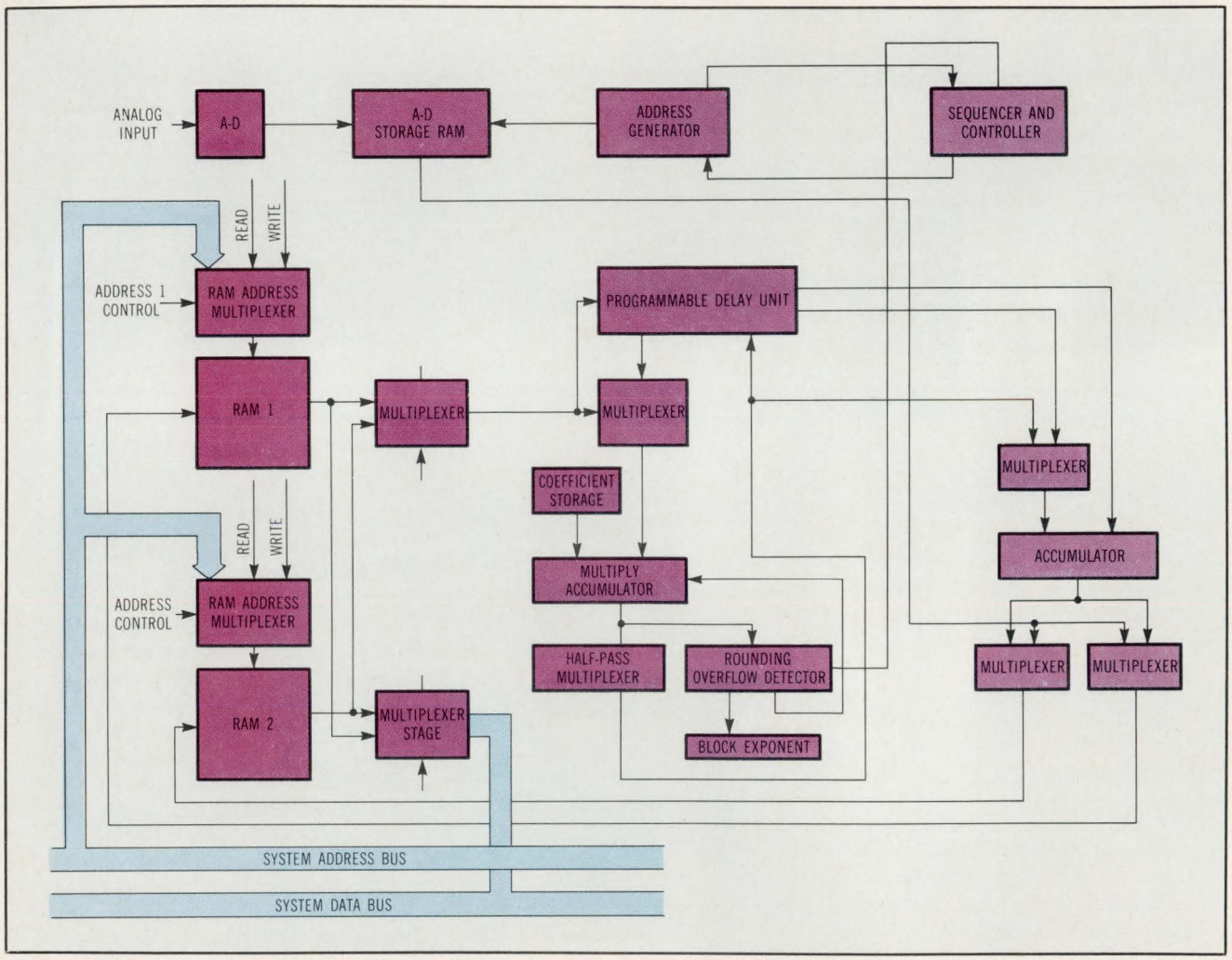

Fig 2 The four-cycle butterfly for a FFT calculation can also be used in a block floating point design. Trade-offs between this design and the equivalent full floating point version need to be understood before designers can pick their architectures.

Quantization effects compared

Suppose the maximum and minimum system data values input into both a block and a true floating point system are 1.0 and 1.0×10^{-3}—a difference of 60 dB. For easy comparison, assume that both systems have a 16-bit mantissa length. As shown in the Table, the larger number has a maximum quantization noise-to-signal level of −96 dB in both cases. The difference between the two systems appears when comparing the smaller numbers. In the block format, the smaller number is reduced to −36 dB. In the true floating format, the smaller number's ratio is maintained at −96 dB.

While equal mantissa length has been assumed, a true floating point system implemented with Weitek IEEE floating point chips would further decrease the quantization noise-to-signal level to −150 dB.

Block versus True Floating Point

Format Value (base 2)	Value (base 10)	Noise-to-signal
Block .1000 0000 0000 0000 $\times 2^1 =$	1.0	−96dB
.0000 0000 0010 0001 $\times 2^1 =$	1.0×10^{-3}	−36dB
True .1000 0000 0000 0000 $\times 2^1 =$	1.0	−96dB
.1000 0011 0001 0010 $\times 2^{-9} =$	1.0×10^{-3}	−96dB

between the two possible quantized numbers, the choice should be random. This design causes the average quantization error to be zero.

The most convenient rounding scheme for fixed or block floating point systems is chopping. The system discards unwanted bits, regardless of their value. Unfortunately, this scheme has an error up to one least significant bit (LSB). If the representation is in 2's complement form, the system rounds down. Chopping tends to increase the quantization noise-to-signal ratio.

Unbiased rounding introduces the least error in either system. A value quantized with an unbiased rounding scheme has a maximum quantization error of 1/2 LSB. For a normalized block number, the quantization error noise-to-signal ratio per operation is $(1/2)/2^{15}$or −96 dB.

Since there is only one exponent for the entire block, differences in magnitude between data values must be absorbed into the mantissa. This results in a loss of precision for smaller values. It is especially detrimental in FFT calculations where word growth can be as high as 10 bits for a 1024-point FFT.

The periodic scaling necessary to prevent overflow for a strong frequency component of an input can cause a severe loss of precision for small frequency components. Quantization error is also magnified in block systems if the input data has a large instantaneous dynamic range. In seismic analysis, for example, the dynamic range between data values can be several hundred decibels.

The single exponent value in a block system limits the dynamic range between data values to the mantissa length. Smaller values can be reduced to a few bits of precision when quantized to block format. Smaller numbers also increase the relative quantization error. A true floating point design keeps the values normalized so the maximum quantization error noise-to-signal ratio is $(1/2)/2^{24}$or −150 dB.

It is helpful to see a real example of the effects of quantization on data values with large differences in magnitude for block and full floating point designs (see Panel, "Quantization effects compared"). Notice the loss of significance in the block format due to the difference in magnitude of the variables. Note also that true floating point can introduce quantization errors on multiplication and addition. The block design introduces error on multiplication, but only introduces error on addition when overflow occurs. This effect is offset by the larger relative errors introduced when block floating values are quantized.

In short, in a block system, the quantization noise-to-signal ratio increases when the signal level decreases, since the exponent is fixed. In a true floating point system, as the signal decreases, the quantization noise also decreases. This is because the full width of the mantissa is always used.

Before the advent of VLSI floating point chips, block floating point was easier to design. Hardware and/or microcode handled the extra complexity of a true floating design. Denormalizing the mantissa before adding (and renormalizing after) added time to the operation cycle. It also required more time to design.

After initial scaling, a block design required less hardware. All operands have equal exponents in this design, so denormalization is not required. The output multiplexer checked overflow, and a counter handled the exponent. Often, however, to maintain maximum signal-to-noise ratio, systems needed to be optimized around the expected data input.

To save processing time, the maximum possible input value determined the block exponent to

What the numbers are

Rounding or quantization is a necessary evil in digital systems. This is because of the limited register length in which to store variables and the performance implications of infinite precision arithmetic. Rounding introduces system nonlinearities that may have adverse effects. So, it is beneficial to select a rounding scheme to minimize these effects. It is also useful to characterize the system's sensitivity or tolerance to rounding effects.

The four rounding modes available with the Weitek floating point chips and examples of what the rounding does (using base 10 for convenience) are listed in the Table. The quantization error is always positive or zero in "round toward plus infinity" mode and always negative or zero in "round toward minus infinity" mode. The maximum quantization error in the "round to nearest" mode is .5. In "round to zero" mode the error is negative or zero for positive numbers and positive or zero for negative numbers. The other three modes allow up to 1.0 (as a fraction of the LSB).

Recall that in the round to nearest (RN) mode, the value chosen is the representable value nearest to the infinitely precise result. If the two nearest representable values are equally near, the one chosen is the one with the LSB equal to zero. In the round toward plus infinity (RP) mode, the value chosen is the representable value nearest, but no less than the infinitely precise result. In the round toward minus infinity (RM) mode, the value chosen is the representable value nearest, but no more than the infinitely precise result. Finally, in the round toward zero mode (RZ), the value chosen is the representable value nearest, but no greater in magnitude than the infinitely precise result.

Rounding Mode Comparisons

Exact Value	Rounded Value (3 digits)				Quantization error (fraction of LSB)			
	RN	RP	RM	RZ	RN	RP	RM	RZ
9.5555	9.56	9.56	9.55	9.55	.45	.45	−.55	−.55
9.8950	9.90	9.90	9.89	9.89	.50	.50	−.50	−.50
9.8850	9.88	9.90	9.88	9.88	−.50	.50	−.50	−.50
−5.4321	−5.43	−5.43	−5.44	−5.43	.21	.21	−.79	.21
−5.4350	−5.44	−5.43	−5.44	−5.43	−.50	.50	−.50	.50

maximize system performance. Today, the design is simpler. Floating point chips can handle the extra complexity of true floating point due to algorithms, VLSI technology, and pipelined design.

True floating designs are less dependent on the system data input and more flexible due to a better dynamic range and increased accuracy. Since general-purpose computers use true floating point systems, several existing software algorithms can be adopted easily. The designer spends less time on the details of implementing floating point and algorithms can be developed and tested in software. This allows the system to work up to capacity in less time.

Unfortunately, errors

Regardless of the system chosen, error analysis is important. When designing a system with unknown or widely varying inputs, extensive error analysis is a necessity. True floating point error analysis is data-independent and extensively documented. Block floating point error analysis is data-dependent, analyzed case-by-case to determine when scaling due to overflow will be required.

Case-by-case analysis can be avoided by making worst-case assumptions (such as an overflow on every add operation). But, this can reduce accuracy to that of a fixed point design. Alternatively, a design using IEEE arithmetic can easily be tested for sensitivity to rounding errors by using the four rounding modes available (see Panel, "What the numbers are"). The value used to initialize the mode register on the floating point chips requires no hardware changes. Thus, the rounding mode can be changed without a problem.

Round to nearest, a form of unbiased rounding, rounds to the quantized value closest to the infinitely precise value. If the infinitely precise result is exactly midway between the two possible values, the one chosen has an even LSB. This form of rounding reduces maximum quantization error to 1/2 LSB, and the quantization error has a zero average value. In most cases, this provides the maximum system performance. The other three modes provide a positive, negative, or toward zero bias. They allow the system to be tested under adverse rounding situations and help uncover system sensitivities to quantization error.

The introduction of fast, compact VLSI floating point chips has given the realtime DSP system designer a choice. No longer are designs limited to fixed or block floating point. Applications not previously possible, as well as those limited to block floating point due to cost, size, or speed constraints, may now take advantage of the superior dynamic range and accuracy of a true floating point system. These systems provide a higher quality product and a shorter design cycle.

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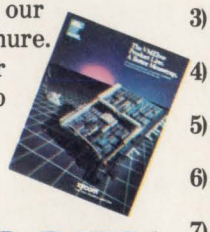

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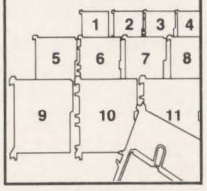

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CIRCLE 87

POPULAR MICRO CONFIGURED FOR DIRECT DRAM SUPPORT

Shrewd use of microcomputer functions permits dynamic RAM support with fewer parts. A nonstandard design approach eliminates most of the glue chips.

by David McCracken

New microcomputers are particularly adaptable and may allow the design of products with a low parts count, resulting in products that are both cost-effective and reliable. Consequently, the most flexible microcomputers have been designed to shrink component count by generating most of the unique control signals needed in a particular application. The Z8 microcomputer, for example, can support an array of 16-pin HM4864P3 dynamic RAMs with no more than three small scale ICs in addition to the DRAMs themselves.

A typical microcomputer application may require linked systems that communicate by using dissimilar protocols or rates. One example of this is a high speed computer that must transmit to a slower printer. Unfortunately, the 125 general-purpose registers in the Z8 microcomputer do not have enough buffer capacity for this situation. But, the CPU can be configured to support 120 (or 124) Kbytes of external program and data memory. In this arrangement, the lower address byte is usually latched from the multiplexed address/data bus. If the external memory is static, then the CPU/memory interface is straightforward. But dynamic memory is preferred for its lower per-bit cost and reduced size.

In the standard approach, the microcomputer's lower and upper address bytes are multiplexed and strobed into the DRAM array. In addition, some mechanism is constantly accessing the memories in order to refresh them. All of this takes many supporting components.

An approach that takes advantage of the microcomputer's hardware flexibility and high speed operation eliminates nearly all supporting ICs. First, the multiplexed address/data bus is manipulated to simulate a multiplexed address bus compatible with the DRAMs. Then, the CPU constantly executes a memory refresh program that consumes one third of its processing bandwidth, and relies on its interrupt capability to handle all other operations. Finally, the microcomputer's I/O ports provide suitable interfacing signals, thus eliminating many support circuits.

The microcomputer's port 1 can function as simple input or output or as a multiplexed bus that first emits A0 to 7. Then, port 1 either inputs or outputs data. To provide the multiplexed address required by external memory, P1 is configured for the A-D bus by loading port 0/1 mode register (RF8h) with 01110101b (75h). This configuration also sets port 0 as input, extends external memory cycles by one clock period, and selects internal stack. As shown in Fig 1, port 1 connects directly to DRAM address A0 to 7. In order to provide 2 address bytes, the microcomputer must "write" to external memory.

Thus, the first byte (which constitutes row address) is emitted as A0 to 7. The second, which is column address, is actually output data. The microcomputer has two alternative instructions for this general function, LDC (load constant) for access to external program memory, and LDE (load external) for access to external data memory. The highly orthogonal CPU makes little software distinction between program and data. However, external hardware is alerted

David McCracken is principal engineer at Synexys Consulting, Aptos, Calif. He is responsible for both hardware and software design of multi-CPU computer systems.

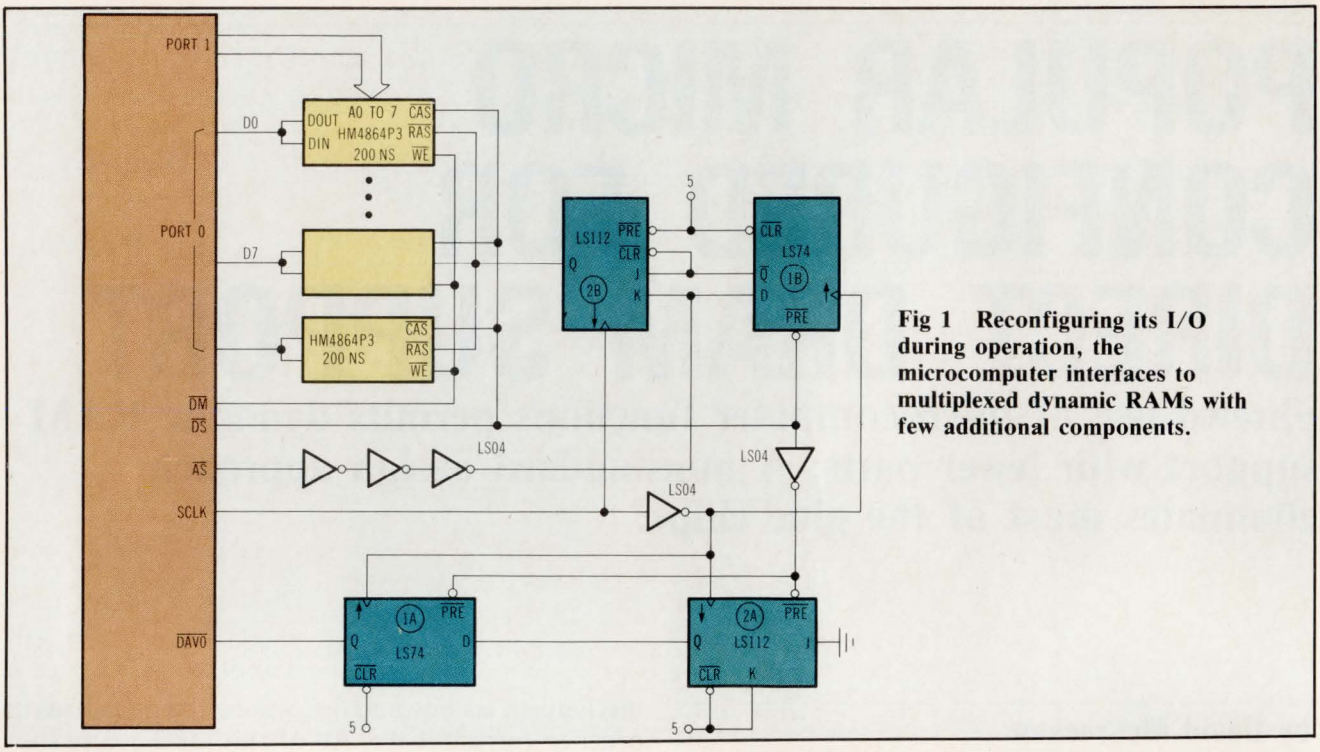

Fig 1 Reconfiguring its I/O during operation, the microcomputer interfaces to multiplexed dynamic RAMs with few additional components.

to the difference by the (negative) assertion of DM (data memory) on LDE instructions. External address pointers are maintained in registers as if normal addressing were in effect. But, the CPU begins external access by outputting the pointer high byte to the address of the pointer itself, eg LDC @RR4, R4 (write to external program). The content of R5 (low address) outputs as A0 to 7, and that of R4 (high address) as data.

A minor but notable advantage of the address method is that it allows access to all addresses as if they were external, including those that overlap internal space and are therefore normally not accessible. This is because the instruction executes simultaneously, both internally and externally. However, the reverse instruction, LDC Rx,@RRy, (read from external program) does not.

Of course, port 1 is unavailable for actual data transfer because it is busy outputting the column address. Instead, data transfers take place via port 0. Writing to the DRAMs is a relatively simple process. The CPU moves data into port 0, configured as output, and then executes the address output. Reading the DRAMs is a complicated process because their outputs are valid only during the relevant bus cycle.

Since the CPU cannot execute the bus cycle and read port 0 simultaneously, this data must be latched. However, a major design goal is to eliminate circuits wherever possible. The microcomputer does this through a handshaking option. When this mode is selected for port 0, by setting b2 of the port 3 mode register (RF7h), input data is latched on the port whenever $\overline{\text{DAVO}}$ (data available or data valid) asserts (negatively). After completing the bus cycle, the CPU reads port 0 data, which remains valid until the next external access.

Dynamic RAMs require a minimum activity in order to maintain data. Memory buffer accessing in response to application demands is unpredictable, and few applications can guarantee that all 256 row addresses will be accessed every 4 ms, as required. Rather than attempt to use application accesses for refreshing, the microcomputer refreshes by accessing sequential row addresses, modulo 256, in an endless loop program.

To provide the fastest execution, rows are not output via LDC or LDE. Instead, simple output is selected for port 1 by clearing both b4 and b3 of port 0 and 1 mode register. A working register, eg R4, provides both the refresh address and loop counter in two instructions, LD 0,4 then DJNZ R4, (previous address). All 256 rows are refreshed in 1.25 ms—31 percent of a 4-ms period—when the CPU is operated at 7.3728 MHz.

External data strobe, ($\overline{\text{DS}}$), functions as column address strobe (CAS) for the DRAMs and asserts only on LDC and LDE instructions. Thus, only a row address strobe ($\overline{\text{RAS}}$) accompanies refreshing, resulting in reduced average power drain. The microcomputer's two 14-bit timer/counters and six priority-set interrupts temporarily suspend refreshing in order to service application tasks. In the remaining 69 percent of its processing bandwidth, the CPU can perform quite sophisticated jobs—eg, controlling a printer mechanism.

In keeping to the objective of low parts count, the microcomputer's flexible inputs and outputs provide

most of the interfacing signals that are required. Four flipflops and five inverters are the only parts other than the microprocessor and DRAMs (Fig 1). Address strobe ($\overline{AS}$) defines the row address window but is not used directly as $\overline{RAS}$ for two reasons. One is that A0 to 7 is specified as valid 50 ns prior to $\overline{AS}$ trailing edge (high going); minimum $\overline{AS}$ low phase is 80 ns, leaving no assurance that the 0-ns row address setup time required by the memory chips can be met.

The second problem is that the 80-ns minimum $\overline{AS}$ does not meet the required 120-ns $\overline{RAS}$ precharge time. Instead, flipflop 2B generates $\overline{RAS}$ based on $\overline{AS}$ and synchronized by the system clock SCLK, that outputs the CPU operating clock when selected by setting b6 and b7 of the timer mode register (RF1h). SCLK also synchronizes $\overline{DAV0}$ output from flipflop 1A to ensure that valid DRAM data is strobed into port 0 on read cycles. Unmodified $\overline{DS}$ provides $\overline{CAS}$ and defines the data window for flipflop 1A. Since the CPU always writes on memory access, the read/write signal is not useful. Instead, $\overline{DM}$ connects to write/enable. Thus, LDC instructions define a read cycle while LDE defines a write cycle.

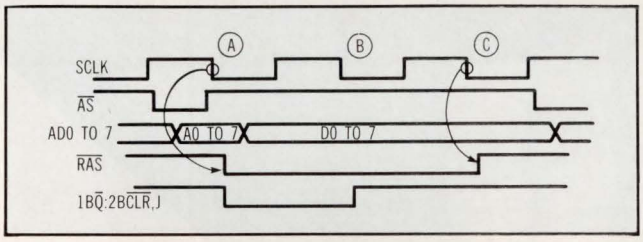

Fig 2 Refreshing occurs when the microcomputer outputs A0 to 7 on port 1, and row address strobe (RAS), synchronized to address strobe (AS) and system clock (SCLK), asserts. Power consumption is reduced because column address strobe (CAS) stays inactive during refresh.

Fig 2 diagrams the timing of a refresh operation. $\overline{AS}$ occurs on every instruction cycle, including those that do not entail external access. Since refresh executes without external access, the cycle lasts for only three SCLK periods. Simultaneously, at point A, SCLK falls and $\overline{AS}$ rises. Three inverters delay $\overline{AS}$ to be sure that it is still high (inverted from low) when SCLK strobes flipflops 2B and 1B. At this time, the Q output of 2B, which acts as $\overline{RAS}$, goes low as does $\overline{Q}$ of 1B.

Port 1 outputs valid A0 to 7 a minimum 50 ns prior to the trailing edge of $\overline{AS}$ as well as 70 ns after it. The DRAMs require that the row address be valid 0 ns before $\overline{RAS}$ asserts (negative), and for 25 ns afterward. $\overline{RAS}$ asserts a maximum 28 ns after $\overline{AS}$ ends, leaving a worst-case address hold time of 42 ns. At the next descending SCLK, point B, $\overline{RAS}$ remains because IC is cleared by $\overline{Q}$ from 1B. However, 1B toggles so that 2B can toggle at point C, thus ending $\overline{RAS}$. $\overline{RAS}$ remains low for 540 ns and high for 270 ns, satisfying memory timing constraints.

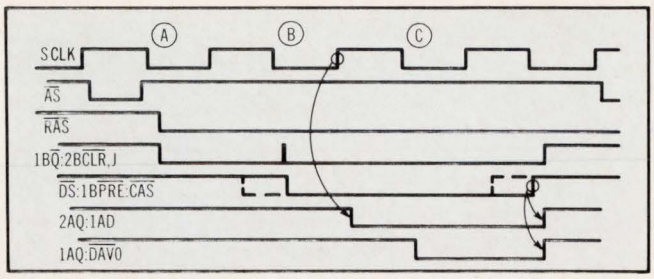

Fig 3 The first half of a memory access cycle is similar to refresh. During the second half, CAS strobes the column address into the DRAMs, and DAV0 strobes DRAM data into port 0 of the microcomputer.

The timing diagram in Fig 3 outlines a memory access cycle. The only timing difference between read and write is the (negative) assertion of $\overline{DM}$ on writes, which occurs long before $\overline{CAS}$ assuring the early write DRAM response necessary to avoid conflicting port 0 and memory outputs. The memory access cycle lasts four SCLK periods because the microcomputer is configured to extend external timing. For the first period, all signals are equivalent to those of a refresh. At the end of the second period, point B, $\overline{DS}$ asserts. Typically, this occurs 25 ns after SCLK falls but may happen even before the clock edge. $\overline{DS}$ provides $\overline{CAS}$ and forces $\overline{RAS}$ to remain low in order to be sure of meeting $\overline{RAS}$ hold time from $\overline{CAS}$. DRAM outputs become valid 135 ns later. Additionally, while $\overline{DS}$ is high, it holds $\overline{DAV0}$ IC 1A's Q output, high. Then, when $\overline{DS}$ is low at point C, SCLK is able to strobe $\overline{DAV0}$ low.

It is important that $\overline{DAV0}$ not assert before this time in order to meet the microcomputer's input data setup time of 0 ns. The uncertainty of $\overline{DS}$ assertion relative to SCLK at time B rules out relying on $\overline{DS}$ alone. If $\overline{DS}$ asserts before SCLK, then DAV0 can assert at point B. The problem is solved by flipflop 2A which, being strobed on the rising SCLK between times B and C, guarantees that 1A will be enabled to toggle only at C. $\overline{DAV0}$ asserts for 270 ns, while the CPU requires 175 ns to latch data on port 0. When outputting data to memory, port 0 is not affected by $\overline{DAV0}$.

By manipulating the functions of the Z8 microcomputer, it can be coupled directly to DRAMs. Thus, a large data buffer can be built with very few supporting components. Besides the obvious utility of this approach to the microcomputer, the more general lesson to be learned is that a thorough understanding of any microcomputer can bring forth unexpected results.

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CIRCLE 88

Dual 68000-based supermicro runs fast with proprietary design

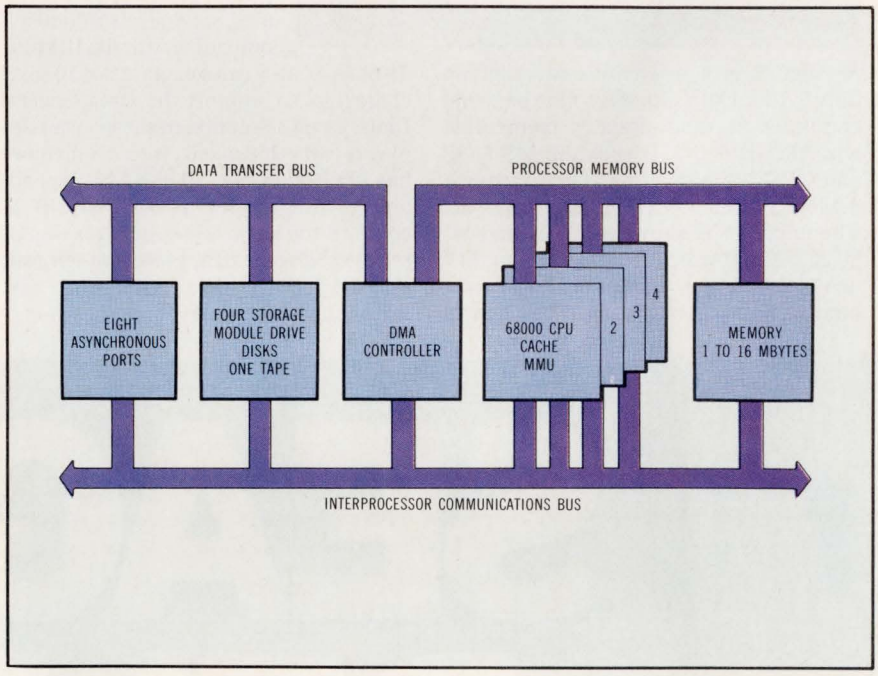
The Model 1124 features a dual-68000 Unix engine. This, along with a multithread architecture, tightly couples the 32-bit processors. Mirrored disk drives, power margining, EDAC memory protection, and redundant cooling are also included in this design.

Designed around a multiple bus structure, the architecture optimizes memory access, interprocessor communications, and data transfer by providing a series of data paths. Supporting the high I/O bandwidth required for online transaction processing, it accommodates 32-bit processors, high density RAMs, and higher performance disk drives (as they become available).

Four separate buses are used. The interprocessor communication bus controls the various processors in the system. This bus also serves as a diagnostic bus, allowing the system to confirm correct memory and I/O subsystem operation. The 32-bit processor memory bus allows the control processor to share its main memory. The unit communicates with mass storage and I/O devices through a 32-bit wide, 33.3-Mbyte/s data transfer bus. General system status signals are transmitted over the utility transfer bus.

The cluster of CPUs is based on up to four 12.5-MHz 68000s, each with a 4-Kbyte cache memory and a proprietary MMU. The cache on each board allows all the processors to share a main memory. The MMU provides two-level mapping, allowing both scatter loading of processes and multiple protection bits per page.

Handling main memory, the DMA/memory controller provides refresh of dynamic RAMs, error detection and correction, and error logging. This controller arbitrates access to the data transfer bus by the I/O processors. It also arbitrates memory requests from the DMA channels and the CPUs sharing the processor memory bus. The memory board holds the main DRAM, and each memory board contains either 2 or 8 Mbytes of RAM. Because online transactions require rapid terminal response time, a set of intelligent I/O controllers processes serial and disk tape I/O. These controllers free the CPUs by providing low level processing. The processors communicate with the CPU through DMA channels or dual-ported memory.



The Model 1124 supports two operating systems—Arix, an enhanced version of Unix System V, and RM/COS, a commercial operating environment that supports high speed file access methods at the operating system level. Unix provides the environment for portable applications software. Identical Cobol compilers exist under both operating sytems, so software developed under Unix can run under RM/COS. Programming support is available in C, RM/Fortran, SVS/Pascal, SVS/Fortran, Ada, APL, and others.

Of the unit's 10 card slots, three handle CPU and memory cards, while six are for I/O expansion. The remaining position is reserved for a memory controller that manages data flow among system cards. Memory is presently available in 2-Mbyte increments, with an 8-Mbyte card planned.

Redundancy in electromechanical subsystems such as disk drives and fans is provided. Components that are less likely to fail, like CPUs, are not always duplicated. Compact, the unit measures 14 x 28 x 54 in. (35.6 x 71.7 x 137.3 cm) and weighs 250 lb (158 kg). Prices range from $60,000 to $75,000 depending on memory configuration. **Areté Systems Corp**, 2040 Hartog Dr, San Jose, CA 95131.

—M.B.

Portable PC-compatible sports full-size LCD

Smaller than a briefcase and weighing only 9.1 lb, Data General's One personal computer is operationally compatible with the IBM PC. It runs the MS-DOS and CP/M-86 operating systems using a 4-MHz 80C88 CMOS microprocessor. The unit's LCD shows a full 25 lines of 80 chars on a screen. Double 3½-in. disk drives located at the side of the keyboard/chassis, provide up to 737 Kbytes of memory. To top it off, a basic package with one disk drive costs only $2895.

Two custom CMOS gate arrays let this portable emulate PC display capabilities. Each array contains up to 4000 gates. The components are surface-mounted on one of three boards comprising all the electronics in the computer. In fact, all components are surface-mounted on the boards, thus eliminating through-holes and saving board space.

In the LCD's dot-matrix format, each character measures 8 x 8 pixels to make it compatible with the IBM PC display. It also can generate 8 x 10 pixel characters to support the Data General fonts. Total resolution of the bit-map display is 640 x 256 pixels. Internal memory has 128 Kbytes of CMOS RAM, expandable to 512 Kbytes. A 32-Kbyte ROM contains the basic I/O system portion of the operating system, power-on self test, diagnostics, terminal emulator, text editor, and communications.

Each One comes with two asynchronous RS-232 ports. One port emulates the Dasher D2 terminal and provides access to Data General's desktop computer products or the Eclipse minicomputer series. In addition, a special software link called the Comprehensive Electronic Office (CEO) Connection allows the user to access documents and files from popular software application programs such as WordStar and Multiplan, then pass those files to larger computers in a CEO automation network.

The One uses either ac power or a battery that lasts for 8 to 10 hours. A battery/pack recharger allows recharging in six hours. The computer consumes an average of 6 W. A portable printer option is available, as well as an IBM PC expansion chassis, allowing access to dozens of third-party IBM PC-compatible plug-in boards. The chassis can also be used to mount additional storage devices. **Data General**, 4400 Computer Dr, Westboro, MA 01580.

—N.M.

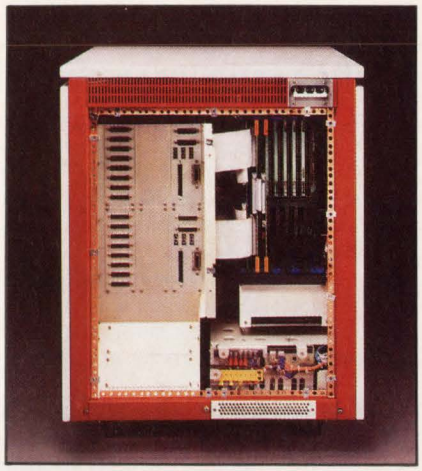
Circle 261

Unix-based 32-bit family tailors computer to application

The Balance 8000 is based on a pool of from 2 to a maximum of 12 NS32000 processors. These processors are allocated dynamically, automatically, and transparently by a single version of Unix 4.2. It integrates the Unix and PC-DOS environments and offers performance levels from a group of micros. These devices range from personal computers to workstations to mainframes.

The processor pool scheme optimizes system throughput by transparently distributing tasks on a priority basis to all available processors. The transparent architecture encompasses both individual computer nodes and distributed networks.

The pool processing technique also allows support for a variety of processors without software changes. All processors in the system share a common memory and a single enhanced copy of Unix. The processors are managed by the operating system—not a master processor—and work as a team under all conditions. Unlike functionally distributed or user-dedicated processing systems, this system architecture allows access to multiple processors during heavy user activity. During times of lighter user activity, the



architecture controls which of the processor's capabilities are used.

Any processor can substitute for any other processor, which makes this system symmetrical. Thus, all processors can execute anything—user processes, the operating system, or I/O routines. And, with the system's dynamic load balancing, whenever any process is ready, it will run on any available CPU. In addition, there is the ability to bump lower priority executing processes in favor of the higher priorities.

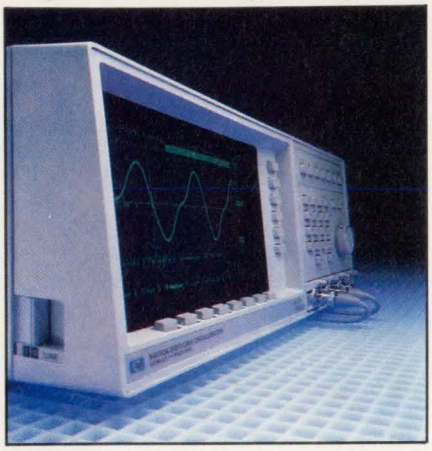
The System Link and Interrupt Controller synchronizes multiple processors by managing interprocessor communication, synchronized access to shared data structures, distribution of processor interrupts, and configuration control. All memory is shared and each CPU has a dedicated 8-Kbyte cache memory that prefetches instructions and stores frequently accessed data, reducing the main memory accesses and traffic on the system bus.

Configurations can range from an embedded engine to a fully-loaded 12 CPU system. The embedded engine includes a 12-slot Balance bus backplane and chassis, 2 CPUs (each with MMU, FPU, and cache memory), 1 Mbyte of RAM, an Ethernet interface, a SCSI bus interface, and Unix, C, and diagnostics for $16,300. A high end network compute node, including 8 CPUs and 8 Mbytes of memory, costs $65,700. **Sequent Computer Systems,** 14360 Science Park Dr, Portland, OR 97229.

—M.B.

Circle 262

Gigahertz-range digital oscilloscope provides clarity and precision



Liberal use of built-in intelligence sets the HP 54100 oscilloscope apart as a thoroughly modern instrument for engineers studying gigahertz-range waveforms. This unit features a 5½- x 7-in. electromagnetic screen (4- x 6-in. user-accessible), 500 x 256 pixel resolution, and screen generated graticules.

The unit's screen provides a continuous menu of available options. Most measurements are performed digitally on the 54100 by simply positioning cursors and requesting the measurement through the keyboard. Cursor positioning can be controlled digitally in some measurements, further increasing precision. For example, the operator can select automatic rise or fall time measurements of 10 to 90 percent or 20 to 80 percent.

The 1-GHz bandwidth of the 54100 permits direct observation of rise times as fast as 350 ps. For measurements involving the rise time of high speed logic families, these automatic measurement capabilities uncover previously undetectable timing problems.

The user can set screen persistence as dictated by the measurements underway. Digital variable persistence mode lets the user set persistence in order to observe only the most recently captured data. Increasing persistence allows successive scans to fill in the screen information for more careful study. Persistence can be infinitely increased, allowing users to retain waveforms onscreen indefinitely. In infinite persistence mode, the screen provides a cumulative display that makes jitter or transient events easier to see.

The 54100 is fully programmable. By combining an HP 9000 series 200 computer with the 54100, users can automatically compare and analyze measurement data. The control language features English-like mnemonics and uncomplicated syntax.

The two-channel scope is available in two configurations. The HP 54100A provides two vertical channels and one trigger input. The HP 54100D provides two vertical channels and two trigger inputs. Price of the 54100A is $17,600. The 54100D costs $19,300. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

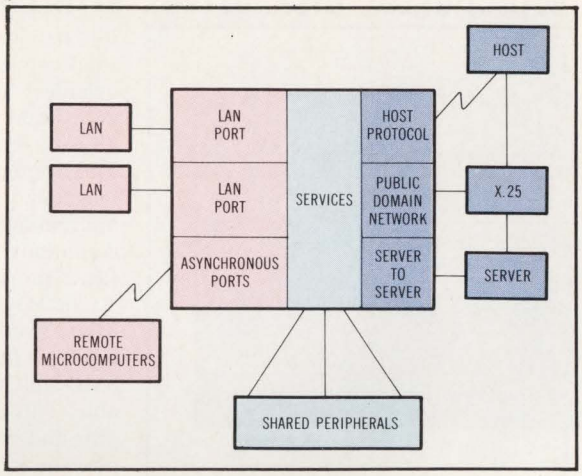
—B.F.

Circle 263

Virtual networking unit builds a bridge to diverse facilities

The Banyon network server overlays virtual networking software on a 68000-based computer. Facilitating location, movement, and use of data and peripherals in microcomputer networks and micro-to-mainframe environments, this network server handles diverse machine communication. A Unix System V operating system creates a virtual network, which addresses this software-intensive problem.

The network server has a proprietary virtual networking system architecture. Consisting of three main parts—front end, services, and back end—this system performs file and peripheral management functions for up to four local area networks (LANs) simultaneously. The front end connects the server to the LANs, while the back end links to various host processors, extended networks, or to other servers. The services are applications that support file and print sharing between heterogeneous systems. They also include StreetTalk, a unique naming and addressing capability. StreetTalk is a global data base for identifying, locating, and controlling access. Because an item's name remains independent of its location, items can be relocated without name changes. It is also a sort of automatic directory assistance.



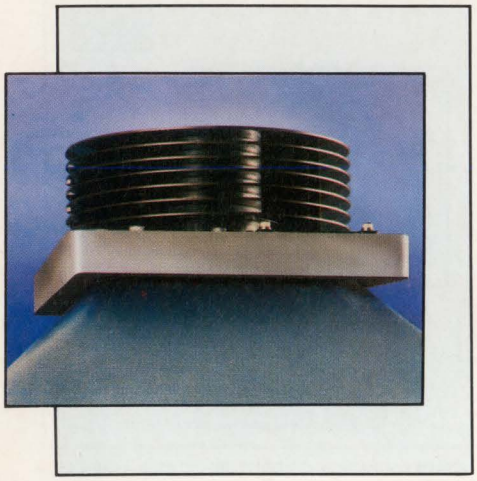
Based on the 32-bit, 68000 processor, this unit contains 512 Kbytes of RAM, expandable to 3 Mbytes. It can be configured with 43 to 160 Mbytes of Winchester disk storage and comes with a 60-Mbyte backup tape drive.

The network server supports communication with LAN controllers in networks that include the Applebus, Ethernet, and Omninet. Remote desktop computers can call into the server, which has asynchronous, auto-answer capabilities. Server prices begin at $16,900 for 512 Kbytes of main memory, 43 Mbytes of disk storage, 60-Mbyte tape backup, and system software. **Banyon Systems Inc,** 135 Flanders Rd, Westboro, MA 01581.

—J. V.

Circle 264

Winchester disk drives stretch 8-in. format



Two 8-in. Winchester disk drives, models MV300 and MV600, provide high capacities. Weighing less than 30 lb and measuring 8.55 x 4.74 x 14.24 in., the MV300 has 331.8 Mbytes of unformatted capacity. It contains seven disks, and has a track capacity of 20,160 bytes, with 1266 cylinders and 13 tracks/cylinder. Seek access time is 3 ms track to track with an 18 ms average and a 40 ms maximum. The average seek time is due in part to magnesium carriage assemblies that weigh approximately 30 percent less than the commonly used aluminum. This allows faster movement.

The MV300's data transfer rate is 9.67 Mbits/s with a recording density of 10,885 bits/in. It has 1000 tracks/in. and standard SMD and SCSI interface options are available. This drive will be ready early next year and will cost about $4200 for 100-piece quantities, depending on the interface options.

The MV600 has 660.4 Mbytes of unformatted capacity and features seven 8-in. oxide media disks. Like the MV300, it has 15 Whitney 3370 ferrite heads, 30,240 bytes of unformatted track capacity, and 13 tracks/cylinder. With 1680 cylinders and two or more fixed sectors, seek access times are 3 ms track to track, with an average of 18 ms, and a maximum of 40 ms. Track density is 1200 tracks/in. and data transfers occur at a rate of 14.5 Mbits/s. Weight and dimensions are identical to that of the MV300.

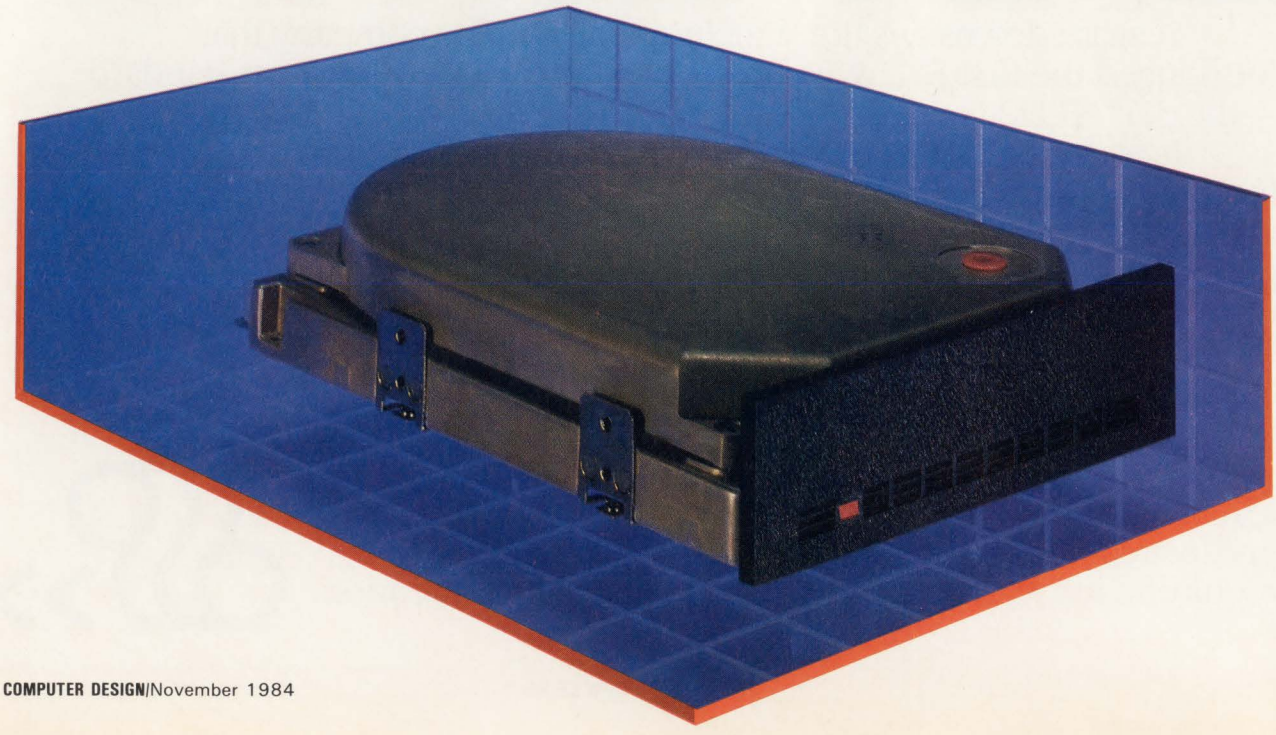
Moving into the territory of the 14-in. drive, these units provide faster access times. These times result from the seven platter approach, as well as linear actuators. Samarium cobolt magnets generate magnetic flux density to further improve access times by exerting more force on less weight.

The MV600 is priced in the $8000 range, depending on the choice of standard SMD or SCSI interface. In addition, IPI-2 will also be available next year. **MegaVault Memories**, 6431 Independence Ave, Woodland Hills, CA 91367.

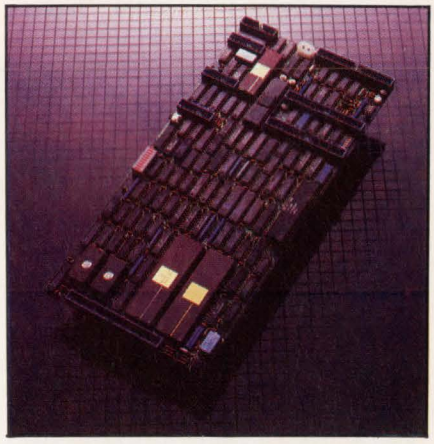
—M.B.

Circle 265

25MB HAL



Controller caches in on sector algorithm



The PM3010 series combines fast access times, high sustained data rates, and an expandable cache on a single board. Using a true sector caching algorithm instead of a track caching scheme, the series provides an integral 128-Kbyte cache RAM that grows to 16 Mbytes via optional memory boards. Because it stores up to 128,000 sectors individually, the cache limits access time to 400 μs. This is approximately 1/200th the time that conventional disk controllers take to do a random disk access.

One 5¼-in. form factor board controls four Winchester drives plus four flexible disk drives. Options include either 8- or 5¼-in. flexible disk support and choice of Winchester control, floppy control, or both. The controller supports any ST506, SA1000, or SMD compatible hard disk drive with up to 16 heads.

A specially defined area on each disk stores optional drive parameters and a media defect map—both automatically loaded by the controller at power up. The media sector defect map is specified during formatting. Additional bad sectors are added—sector by sector—to the map as they are located during normal system operations. The controller automatically detects and reassigns defective sectors without host computer intervention. This reduces system processor work load and simplifies disk interface software.

The sector cache method minimizes data access time. This eases the main performance bottleneck in most small computer systems, particularly those running multi-user operating systems. Each sector is handled individually for more efficient cache use. Only sectors needed by the host are read into the cache. When sequential sectors are addressed, throughput increases due to multiple sector addressing with a single command.

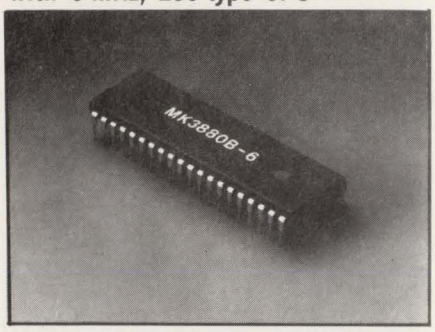
Queues that store internally generated requests for data transfer between disk, cache, and host help achieve the high sustained data rate. Loading missing data into the cache from the disk can be overlapped with the transfer of cache resident data to the host.

All controllers in the series use SCSI with support for the full extended command set. The sustained average data rate over the SCSI bus is 1 Mbyte/s. Price for the controller is $740 in quantity. **Distributed Processing Technology**, 132 Candace Dr, Maitland, FL 32751.

—M.B.

Circle 266

Microcomputer throughput vaults with 6-MHz, Z80-type CPU



A 6-MHz Z80 microcomputer CPU—the MK3880-6—configures with standard memory types to create high performance systems with wide-ranging applications. It allows 50 percent greater throughput than its 4-MHz counterpart. This CPU provides arithmetic and bus control to operate with bused peripheral controllers such as parallel I/O, serial I/O, counter/timer, and DMA circuits. A single-phase system clock, 5-V supply, and onchip dynamic memory refresh counter simplify design. In 1000-piece quantities, these CPUs are $5.50 each. **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 267

Single-board computer uses Forth-based design

The 100 Squared is less than 100 mm long and provides 40 user I/O lines, an RS-232 port, and PROM programming capabilities, Using the R65F12 Forth-based micro, the device can be used as a development system and a dedicated controller. The I/O lines, made up of five 8-bit parts, are TTL/CMOS-compatible. The runtime kernel of Forth supports the operating system functions with 133 runtime routines resident in ROM. The boards are priced between $230 and $290, depending on configuration. **New Micros, Inc** 808 Dalworth, Grand Prairie, TX 75050.
Circle 268

Floating point coprocessor designed for HP 9000 desktops

The FP200 allows a user to run calculation-intensive programs up to five times faster without any modification of existing software. It is transparent to Basic and Pascal and plugs into any available I/O slot. It also easily integrates with assembly language programs. The host computer initiates all floating point operations and is then free to perform other computations. An eight-position switch provides flexible configuration of the address space. **Infotek Systems**, 1400 N Baxter St, Anaheim, CA 92806.
Circle 269

Board running TurboDOS 1.3 handles up to four floppies

A Z80B CPU (or optional Z80H running at 8 MHz) provides the processing speed needed for a Systemaster II single-board computer to serve as master in an 8- or 16-bit system. With 128 Kbytes of parity checked RAM divided into two 64-Kbyte banks, the system allows simultaneous control of up to four 5¼-in. floppy disks. It boots from either floppy or hard disk. Two RS-232 serial ports provide either synchronous or asynchronous communication with software programmable baud rates. **Teletek**, 4600 Pell Dr, Sacramento, CA 95838.
Circle 270

PERFORMANC

Rugged handheld unit withstands tough settings

Husky IS handheld computer survive hazardous environments, and are certified for use in settings where explosive gas/air mixtures are present. Product surfaces are specified, under the BASEEFA "T4" class, not to exceed 135 °C, even under extreme fault conditions. The Husky IS also incorporates a protected socket for a bar-code wand. Applications include direct data capture and safety systems. **Sarasota Automation,** 1500 N Washington Blvd, Sarasota, FL 33577.

Circle 271

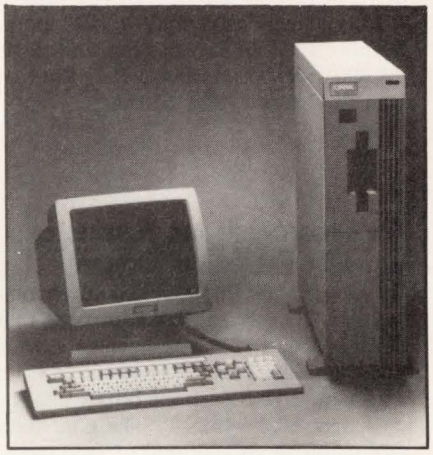
RAM capacity hits 512 Kbytes on single board with video features

The 4500 aims at development tasks in industrial control, robotics, and data acquisition applications. It is available in two basic packages, the low end 65xx and the 6809 Flex-based package. At the heart of the 65xx is a 6502 microprocessor coupled with Microkey's implementation of Forth-79. This board runs the W65SC816—a 16-bit version of the 6502 that can address 512 Kbytes of RAM in two equal-sized banks. The 6809E version uses the Flex operating system, allowing use of Fortran, Basic, and Cobol, among other languages. The board offers two monochrome composite video outputs, each software scrolled, and high resolution graphics to the tune of 640- x 200- or 1280- x 200-pixel resolution, 16 color in analog or 8 color in TTL. The 6809 is available for $425. **Microkey Ltd,** 98a St James's St, Brighton, East Sussex, BN2 1TP, U.K.

Circle 272

High end Oasis operating system adapts to multi-users

The C501OV is a floor-standing system based on the Z80B. In its minimum configuration, the system features five serial ports and one parallel port, a 384-Kbyte RAM, and a choice of 14, 21, 40, or 80 Mbytes of internal Winchester disk storage with tape cartridge backup. Ramdisk and Disk Cache software features are built-in. Ramdisk allows the main memory to be used as a logical disk for frequently accessed data. Disk Cache provides the same service while updating the physical disk. The Oasis operating system, Oasis Basic, and Control/Sort come bundled with the C501V. Product pricing starts at $7990. **Onyx Systems, Inc,** 25 E Trimble Rd, San Jose, CA 95131.



Circle 273

Array processor for microcomputer systems rates at 15 MFLOPS

The Sky Warrior array processor performs over 15 MFLOPS. Packaged on two Eurocard plug-in modules for easy microcomputer system integration, the processor performs arithmetic in full compliance with the IEEE P754 standard for 32-bit and 64-bit data. Together with high speed arithmetic, Sky Warrior offers DMA to system memory of up to 16 Mbytes at a transfer rate of up to 20 Mbytes/s. Performing a 1024 point complex FFT in 3.9 ms, the unit costs $14,900. **Sky Computers**, Inc, Foot of John St, Lowell, MA 01852.
Circle 274

Single-board unit has Winchester controller packed on Eurocard

The Quark/300 single-board microcomputer sports a hard disk controller that incorporates a 12-Kbyte hardware track buffer holding one complete track. Data is transferred between the buffer and the hard disk at 5 Mbits/s. The controller permits buffered and nonbuffered seeks. Multiple drive types can be mixed. The Quark/300 uses a Z80 with individually maskable peripheral interrupts and real-time clock interrupts. The board also features a self-contained video display controller, 512-byte bootstrap loader in PROM, up to 256-Kbyte RAM memory, and 2 Kbytes of character-generator RAM. Prices range from $495 to $895. **Megatel Computer Technologies**, 1051 Clinton St, Buffalo, NY 14206.
Circle 275

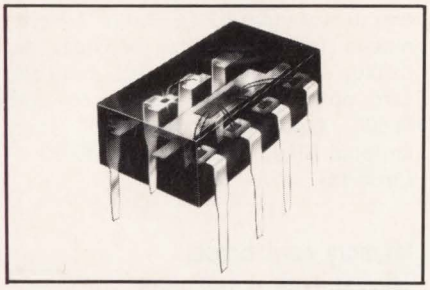
Compact VMEbus module delivers high end processing power

A tightly coupled architecture that combines the 10-MHz 68010, a high speed memory management unit, fast access cache, and a 32-bit VMEbus interface highlights the model PTVME100. Typically, the PTVME100 will execute VMEbus memory resident programs with over a 75 percent zero wait-state hit rate. This processor module measures 9.2 x 6.3 in. (234 x 160 mm). A 4-Kbyte single set, single/double block cache memory reduces bus accesses needed during program execution. Also, the cache can operate with full 32-bit VMEbus read data transfers. **Performance Technologies Inc**, 300 Main St, E Rochester, NY 14445.
Circle 276

Add-on card turns PC or XT into a supermicro

The IBM PC or PC/XT can gain 32-bit power via the Tiger-32. This single-slot, add-on card features the 32032 processor and 32082 demand-paged virtual memory management. The Tiger-32 comes complete with 512 Kbytes of 150-ns RAM as well as the Xenix 3.0 operating system. It is available with optional 10-MHz clock, 32081 floating point, and 1- or 2-Mbyte RAM using 256-Kbit chips. The multitasking, multi-user Xenix system uses the PC as an I/O processor. Tiger-32 interfacing to I/O devices is handled by XIP—a virtual I/O protocol program that runs under PC-DOS 1.1 or later versions. The unit with software costs $2495. **DFE Electronic Data Systems**, Singerstr 3, BRD-7513 Stutensee 1, West Germany.
Circle 277

Solid state relay supplants SPDT mechanical units



A solid state relay, the OMC 110, replaces Form C single-pole double-throw (SPDT) mechanical relays for telecomm and data acquisition switching. This optically isolated SPDT relay requires less than 5 mA. It offers a 10:1 reduction in drive power compared to typically used mechanical relays. The normally open contact of this unit is formed using Optomos technology coupling an infrared LED to a photovoltaic cell to drive a pair of bidirectional power MOSFETs. The normally closed contact is formed by optically coupling into a custom photo darlington IC to drive a second MOSFET pair. The relay handles 300 Vac or Vdc up to 100 mA. Quantity-1000 cost is less than $4 each. **Theta-J Corp**, 8 Corporate Pl, 107 Audubon Rd, Wakefield, MA 01880.
Circle 278

Display sports touch-screen operation, aims at industrial world

The Rack Mount Information Display measures 19 x 12¼ in. (482 x 311 mm) and is primarily designed to bring touch-screen capabilities to industrial settings. The display acts as a standard ASCII terminal, emulates Lear-Siegler ADM-3A cursor addressing, and communicates via an RS-232-C port at rates up to 19.2 kbaud. Screen input is activated by interruption of criss-crossing infrared light beams from LEDs and phototransistor detectors surrounding the display. Up to 648 active touch points can be defined. An 8085 microprocessor combines both touch-active and terminal functions. **Electro Mechanical Systems, Inc**, 801 W Bradley, Champaign, IL 61820.
Circle 279

Active matrix method highlights flat-panel display

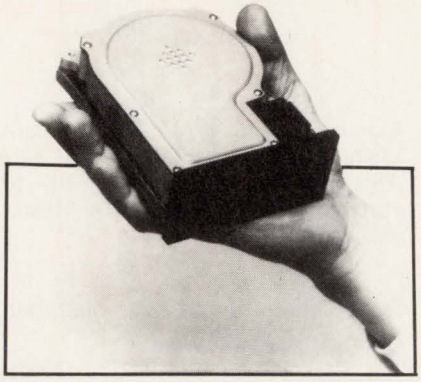
The MiniGraphic flat-panel display presents up to 512 chars (16 rows of 32 chars each) without emitting electromagnetic radiation. With a screen that is 1/2-in. thick, the device is based on an active matrix circuit that turns each pixel into a memory cell. Turning the cells on makes them appear as visible dots from which letters and numbers are created. The Minigraphic offers sharp liquid crystal images and a viewing angle of 45 degrees perpendicular to the viewing face along all axes. The display measures 4 x 5 in. (101 x 127 mm). Frame refresh rate equals 60 Hz while power input voltage is 5 Vdc and dissipation, 3 W. **Panelvision**, 265 Kappa Dr, Pittsburgh, PA 15238.
Circle 280

Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.

Two mass storage subsystems include removable media disk and mag tape

Both system controllers can handle two drives and are field-installable. The disk pack, with MR-608-80 Mbyte 9-in. media, offers high data storage security. It is front-loading and has 67.4 Mbytes of usable data storage. It uses an SMD interface. The mag tape offers a high system data throughput of 400 kbytes/s. Data storage density is 180 Mbytes/reel. The dual-density system can run at 6250 bits/in. for GCR format or 1600 bits/in. for PE formats. The media disk is $21,000, while the mag tape subsystem is $26,000. **Masscomp**, One Technology Park, Westford, MA 01886.

Circle 281



Volume production is expected in the first quarter of next year. Quantity prices are under $650. **Microcomputer Memories, Inc**, 7444 Valjean Ave, Van Nuys, CA 91406.

Circle 282

Drive in 3.5-in. form factor achieves 25-Mbyte storage

Designated the M-125, a 3.5-in. Winchester drive provides 25 Mbytes of unformatted storage (20 Mbytes formatted). It includes an ST412 interface, and sports an 85-ms average access time. It measures 1.625 x 4 x 5.75 in. (41 x 101 146 mm) and weighs 1.7 lb (0.77 kg).

Winchester converts PC compatibles into XT-type machines

With 72 Mbytes, the QuadDisk 5¼-in. Winchester allows a PC or PC compatible to emulate an XT. It requires no external drivers, booting directly from the hard disk. With its 30-ms access time, it is suited for LANs and multi-user systems. Mounted internally in the second floppy disk drive slot, the QuadDisk formats into two logical 31-Mbyte partitions. The system uses standard DOS 2.0 or 2.1 commands for formatting, copying, and backup. The system—with controller card, power supply, and software—costs $6500. **Quadram Corp**, 4355 International Blvd, Norcross, GA 30093.

Circle 283

Memory card boasts 10-year typical retention

A nonvolatile 256-Kbyte RAM module—the 2002—sports STD bus, 8085, 8088, and Z80 compatibility. Data retention is typically 10 years. Four sockets are provided, each accepting a 64-Kbit x 8 nonvolatile RAM. Write protection is switch selectable and access time is 135 ns. Data appears at the block address selected and is immediately available for execution after the block select output is implemented. The 2002 measures 4.5 x 2.7 x 6.5 in. (11.4 x 6.8 x 16.5 cm) and costs $298. **I/O Controls Inc**, 826 Newton-Yardley Rd, Newton, PA 18940.

Circle 284

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CIRCLE 93

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Quarter-inch tape subsystem aims for XT applications

A quarter-inch tape subsystem kit upgrades the IBM XT. The kit represents a complete package that includes file selectable streaming tape drive, controller, cables, software, and data cartridge. End users can use the subsystem in either the file selectable or streaming mode. In the former, the user can address files as with a floppy or hard disk. The latter allows fast backup of a whole disk, but only the actual data—not the unused space—is copied. Unformatted capacity for the drive equals 21 Mbytes. Units are less than $1000. **Data Electronics, Inc,** 10150 Sorrento Valley Rd, San Diego, CA 92121. **Circle 285**

Optical disk system can store 1 billion bytes

An optical disk storage and retrieval (OSAR) library can store 64 optical disk cartridges online. Cartridge access is performed by a robotic mechanism that removes a cartridge from a storage slot and inserts it in one of four optical disk drives. Access time to data stored on a mounted disk is 200 ms. Fine positioning provides 2-ms track-to-track speed. Each optical disk provides 1 Gbyte of nonerasable storage, so a fully configured OSAR library with dual-sided media can total 128 Gbytes. Each OSAR stores the equivalent of 1000 reels of 6250-bit/in. tape. Estimated media cost per megabyte is $.30. Shipments begin in January at quantity prices ranging from $55,000 to $80,000. **FileNet Corp**, 1575 Corporate Dr, Costa Mesa, CA 92626.
Circle 286

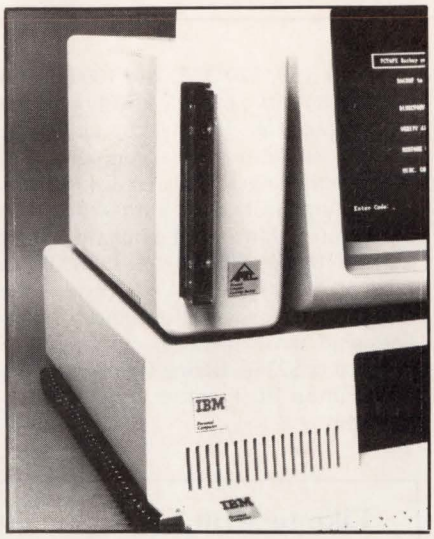
Nine-track tape drive enhances 586 operation

A nine-track tape drive supports Altos 586 computers running the Xenix operating system. The nine-track, half-inch tape drive reads and writes data using a 1.6-Kbit/in. phase-encoded format, making the drive ANSI/IBM-compatible. Software support includes utilities that position the tape and tape drive, identify the format of foreign tapes, and read/write ANSI labeled tapes. The tape drive provides 40-Mbyte capacity with a 2400-ft reel of tape. The tape controller installs in the internal Multibus slot on the 586. A 586 with the nine-track subsystem (tape drive, Multibus controller, cables, and software) costs $6275. **Quest Research,** 214 N River Ridge Cir, Burnsville, MN 55337.
Circle 287

Data storage system aims at VAX and large PDP-11 system needs

Aquarius II is a large capacity storage system for DEC VAX and large PDP-11 computer systems. It is designed for use with Unibus, VAX CMI, VAX SBI, or VAX Unibus structures. In its smallest configuration, the unit has 474 Mbytes of unformatted capacity using a Fujitsu Eagle Winchester drive and 180 Mbytes of unformatted storage provided by a CacheTape GCR drive. The dual-density CacheTape (1600 or 6250 bits/in.) includes a third density option of 3200 bits/in. Price ranges from $29,990 to $51,450 with quantity discounts available. **First Computer Corp**, 645 Blackhawk Dr. Westmont, IL 60559. **Circle 288**

Tape backup employs double buffering software scheme



The PC Tape is a quarter-inch cartridge tape backup system targeted at IBM and other hard-disk based personal computers. A software double buffering scheme coupled with a DMA data channel provides file-oriented streaming backup instead of traditional mirror image backup. PC Tape can append data to a previously written tape and backup only changed files, thus minimizing daily backups. Using ANSI standard cartridges, streaming tape performance reaches up to 1.12 Mbytes/min with 17.7 Mbytes of data stored per cartridge. Software provides DOS 2.0 compatibility, interactive menu or batch mode operation, plus subdirectory backup and restore. PC Tape is priced at $995 in quantities. **Advanced Peripheral Technology, Inc**, 9051-L Red Branch Rd, Columbia, MD 21045.

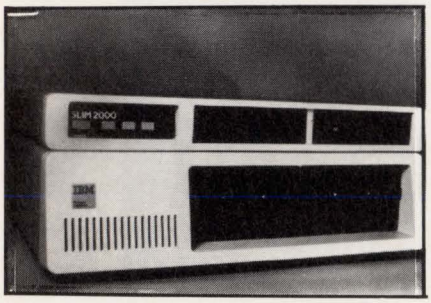
Circle 289

Diskless memory plugs into PC, XT, and PC compatibles

The Omega diskless memory is a multifunction board composed of a main RAM board and optional plug-in boards. Plug-in boards include such features as error checking and correction, serial and parallel I/O, a clock calendar, and coprocessor capability. The product is aimed at the IBM PC market. Key to the unit is its flexible adaptation to 64-Kbit or 256-Kbit RAM use. The optional 80186 coprocessor plug-in greatly increases PC system throughput. Up to 1 Mbyte of memory can be set aside as a print buffer. **Mega-Omega Systems Inc**, 5477 Glen Lakes Dr, Dallas, TX 75231.

Circle 290

Disk and tape subsystem runs on IBM PC



The SLIM 2000 offers 10 Mbytes of formatted hard disk storage and 10 Mbytes of tape backup in the same low profile, integrated system. It features power direction for controlling up to three separate devices and surge suppression. It requires only one PC slot to control both disk and tape. It measures 19.5 x 14 x 2.5 in. (49.5 x 35.5 x 6.4 cm) and weighs 12.5 lbs (31.8 g). It is a match-fit on top of the PC so there is no wasted space. Price is $2995. **Datatron, Inc, Enhancement Products Div,** 2942 Dow Ave, Tustin, CA 92680.
Circle 291

Winchesters offer capacity from 10 to 40 Mbytes

Winchester subsystems aimed at DEC LSI-11 based applications, called CI-820s, come with formatted capacities of 10, 20, or 40 Mbytes. All subsystems contain a 2-Mbyte, dual-floppy or streaming tape backup. Using a 22-bit DMA controller for both floppy and Winchester disks, the drives have an average access time of 40 ms and a transfer rate of 625 kbytes/s. Winchester emulation is RL01/02 compatible and the floppy emulation is RX02/ RX03. The 10-Mbyte model costs $4495, while the 20-Mbyte version costs $4995. The 40-Mbyte subsystem is priced at $5995. **Chrislin Industries, Inc, Computer Products Div,** 31352 Via Colinas, Westlake Village, CA 91362.
Circle 292

Tape drive provides backup without a computer

The Sponge (model T100) is a quarter-inch tape drive subsystem with formatted capacity of 20 Mbytes. Designed to interface with HP machines that include the series 80, 150, 120/125, and 1000, it can back up an entire hard disk without using a host computer. In a backup mode, the Sponge functions like a computer and takes control over the hard disk drive—eliminating the need for a software driver on the host. Maximum emulation burst transfer rate is 300 kbytes/s. MTBF is rated at 20,000 hours. A 64-Kbyte cache memory improves performance of random read/write operations. The Sponge is priced at $2380. **Bering Industries, Inc,** 1400 Fulton Pl, Fremont, CA 94539.
Circle 293

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The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

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The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

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How did we do it? With a preconverged in-line tube/yoke combination unlike any other. Our precision S/ST (saddle/saddle toroidal) deflection yoke is ideally matched to each tube, for near perfect convergence, high repeatability and stability over a wide range of operating conditions.

We combine it with a specially-designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

The result: a triumph over the convergence factor. Find out what it can do for your next color terminal or monitor, and ask about our full line of quality color and monochrome CRTs. Write or call: Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5278.

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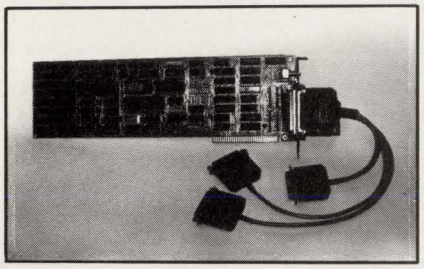
Panasonic
Industrial Company

CIRCLE 99

Personal computers share a plotter via option slot board



Plotter bottlenecks can be reduced with SharePlot, which allows up to three PC users to access a common plotter. Shareplot (ESI-6012 and ESI-6016) occupies one option slot in one PC/XT. Because of buffering, any of three PCs can submit plot commands. The ESI-6012 model lets machines share a serial interface plotter. It accepts input from the host PC/XT, and most compatibles, and from external parallel output ports. ESI-6016 accepts input from the host and from the external serial output ports of up to two PCs. Both data terminal ready (DTR) hardware and X-ON/X-OFF software handshakes are supported at 300, 600, 1200, 2400, 4800, 9600, and 19,200 baud. SharePlots cost $595 each. **Extended Systems**, 6062 Morris Hill Ln, PO Box 4937, Boise, ID 83711. **Circle 294**

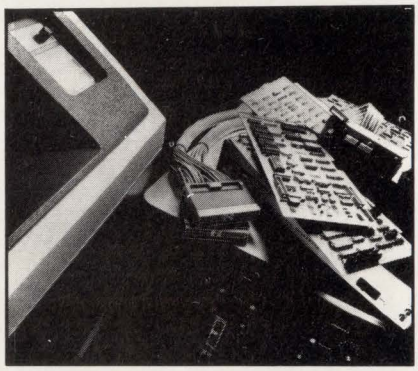
Twelve-bit A-D is marked by comparator and clock

Model 3110 has an internal reference, clock, and comparator. It converts in 500 ns at 8 bits and at 670 ns at 10 bits. Differential nonlinearity is less than ±0.015 percent, and there are no missing codes over the full −25 to 85 °C operating temperature range. Supplied in a 32-pin metal package, cost is $196 each in 100-piece quantities. Delivery is four weeks. **Dynamic Measurements Corp**, 8 Lowell Ave, Winchester, MA 01890.
Circle 295

Disk controller melds ESDI drives to the SCSI bus

Champion disk controllers interface Extended Small Disk Interface 5¼-in. Winchester disk drives to the Small Computer System Interface bus. Champions will integrate up to two ESDI disk drives with any microcomputer or minicomputer, through use of an independent SCSI-based host adapter at the CPU. This PC board measures 5.75 x 8 in. (14.6 x 20.3 cm) and can be mounted on the disk drive or packed within the subsystem chassis. It has a 14-Kbyte data buffer and can connect a range of serial mode ESDI units, including drives with up to 16 read/write heads. The disk controller sells for $395. **Emulex Corp**, 3545 Harbor Blvd, PO Box 6725, Costa Mesa, CA 92626.
Circle 296

Converter works locally without communication software



An enhanced version of the 9135 remote printer converter allows remote printers to function as local output devices without requiring communication software. The product, named RPC/S, includes improved firmware and data compaction. Components include a microprocessor-driven adapter for parallel-to-serial conversion at the host CPU site and a printer-mounted board to convert serial to parallel for hardcopy output at the remote location. Transmission is done using bit-compacted synchronous protocol with speeds to 19.2 kbaud. It will drive line printers at 1200 lines/min and is compatible with industry-standard impact printers. Pricing starts at $4000 with volume discounts available. **Southern Systems Inc**, 2841 Cypress Creek Rd, Ft Lauderdale, FL 33309.
Circle 297

Extended temperature range distinguishes D-A converter

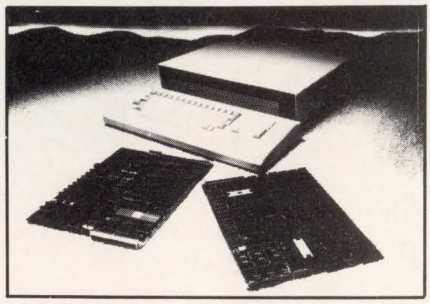
A 16-bit, 15-μs D-A converter provides a 10-V full scale output range and operates over the full military temperature spectrum. The converter is designated the DAC-02900. It contains a 6.4-V precision internal reference and an output op amp. Gain and offset errors for the device can be externally trimmed to zero. The device is a pin-for-pin replacement for DAC-HP16 and DAC-72-type units, but increases their linearity to 15 or 16 bits while operating over extended temperature ranges. **ILC Data Device Corp**, 105 Wilbur Pl, Bohemia, NY 11716.
Circle 298

Micro-to-mainframe link emulates 3270 functions

The 3270 PC Connection combines an add-on interface board with software to deliver micro-to-mainframe communications for IBM PCs and PC-compatibles. This product emulates 3270 functions. Users can alternate between host and PC applications, transfer data to and from the host, and interact with several host applications concurrently using multiple windows. A screen control application program interface allows a DOS application to communicate with up to five emulated 3278/79 host sessions. The board's performance is enhanced by data compression and dual-ported architecture. The board costs $1595. **CXI**, 3606 W Bayshore Rd, Palo Alto, CA 94303.
Circle 299

Controller for wide range of monitors marked by pan and zoom

The CG2100 high resolution color graphics controller consists of a 68000 processor-based graphics display generator with a detachable keyboard. External I/O interfaces easily connect computers to monitors. The CG2100 also provides 1024- x 781-pixel resolution with Tektronix 4100 compatibility. Hardware features include independent pixel pan and zoom over each graphics surface. The product is VMEbus compatible and provides a SCSI/SASI interface. The basic system costs $3995. A two-surface system lists for $5595. **Cybernex**, 1257 Algoma Rd, Ottawa, Ontario.



Circle 300

RELIABILITY RUNS IN OUR FAMILY.

Face it. A computer terminal is like an employee of your company. You have to be able to count on it to do its job. Not just its first day on the job, but every day for years to come. Because reliability translates to productivity, and productivity relates directly to profits. That's why at ADDS we design reliability into all of our products. And our years of engineering and manufacturing experience translates to a quality record that is unsurpassed in the industry.

You can count on ADDS to have a Viewpoint™ for any job that requires a terminal. For example, the ADDS conversational Viewpoint + gives you dynamically allocated function keys, visual highlighting and keyboard adjustable screen contrast — all at an extremely competitive price.

What's more, you can count on the ADDS Viewpoint to get along with everyone in your company. Its plain language menu allows you to select operating characteristics from the keyboard so quickly and easily, time-consuming operator manual references are practically eliminated its first day on the job. And the Viewpoint + is an ergonomic study in how to comfortably match man with machine.

So if you're considering a terminal purchase for your company, consider the ADDS Viewpoint. Give us a call. We'll share even more of our family secrets with you. You'll find how beneficial it can be to have Viewpoint reliability run from our family to yours.

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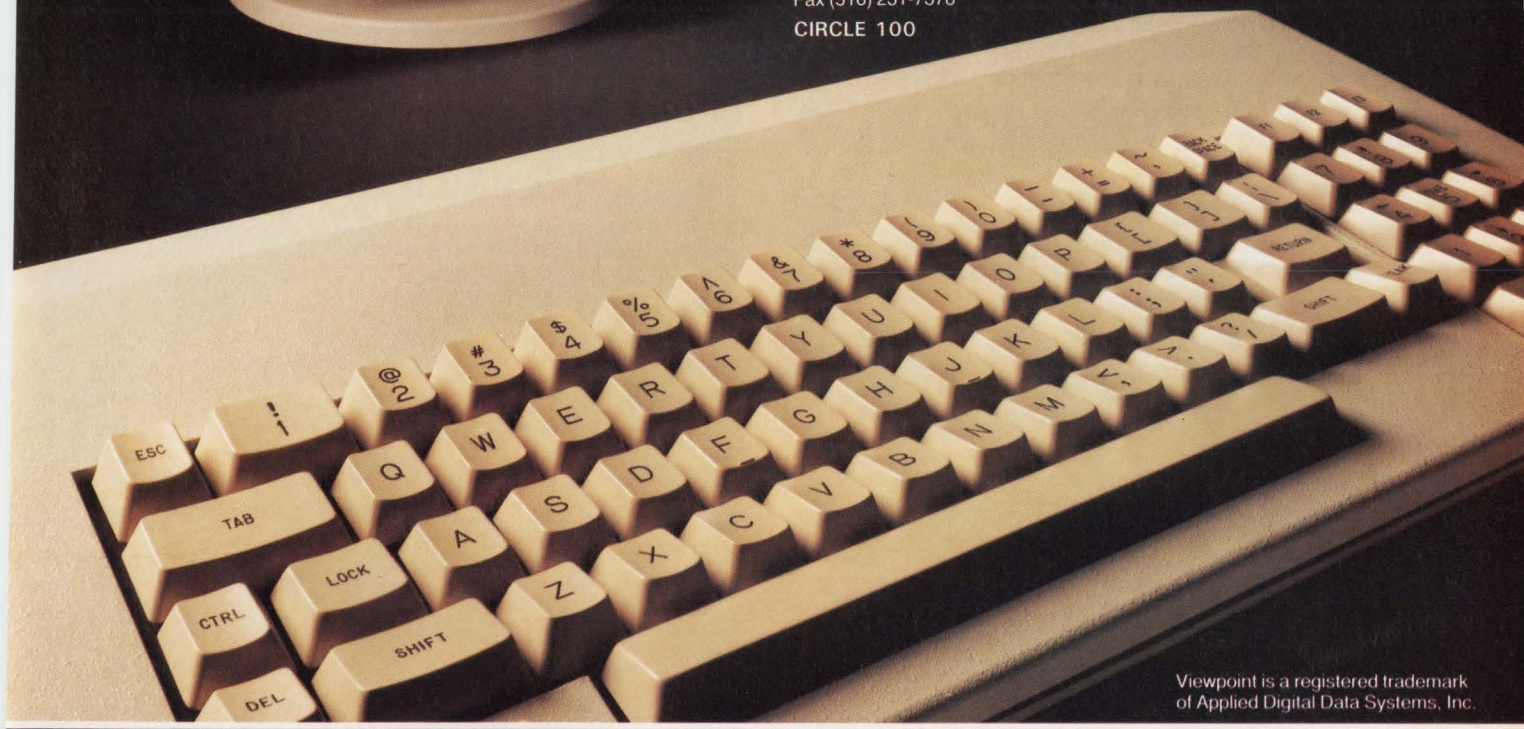
CIRCLE 100



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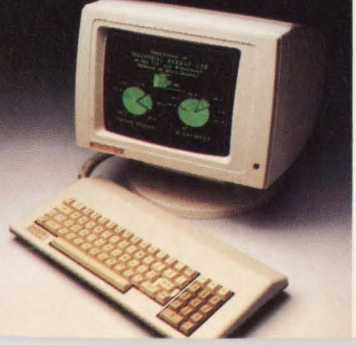
VIEWPOINT + GRAPHICS
Low Cost 4010 Graphics



VIEWPOINT 60 +
Smart Editing Terminal

VIEWPOINT 78
3278-2 Compatible

VIEWPOINT 78 COLOR
3278-2 Compatible and Color

Asynchronous multiplexer handles LSI-11 and MicroVAX computers

The model 2134 DZV MUX is a double-height module that replaces two DEC DZV11 4-line quad-height multiplexers. It is functionally equivalent to the Unibus-type DZ11. It features built-in diagnostics for terminal test and functional verification. Providing up to 38.4 kbaud and split baud rates, the unit strictly controls bus timing for maximum throughput. Address and interrupt are DIP switch selectable throughout the floating ranges. Prices start at $800. **Gen/Comp Inc**, 6 Algonquin Rd, Canton, MA 02021. **Circle 301**

Controller connects PC to local network

The GW 92 is an IBM PC bus-compatible board that converts host messages to and from the CINCHNET network format, while performing error checking, resolving net contention, and queuing messages in both directions. Thus, it connects a PC to the S-485, CINCHNET LAN. It performs the functions for the CINCHNET GW 91 gateway without a separate powered enclosure or an asynchronous communication adapter. The GW 92 queues up to 30 network messages and feeds them to the PC via a 128-byte FIFO buffer. These can be read by the PC singularly or in bursts. The GW 92 is also available in unprogrammed form. **Inconix Corp**, 10 Tech Cir, Natick, MA 01760. **Circle 302**

Front loading 16-bit latches reduce board space

The SM54/74LS646, -47, -48, and -49 are bidirectional devices so data can enter from either side. They have a maximum data to output delay of 25 ns, a maximum clock to output delay of 35 ns, and a clock frequency of 25 MHz. Available configurations include inverted, noninverted, three-state output, and open collector output. Applications include minicomputers, microcomputers, and computer peripherals. Housed in 24-pin skinnydip plastic and ceramic packages, the devices sell for $6.78 and $8.15 each, in 100s. **Monolithic Memories, Inc**, 2175 Mission College Blvd, Santa Clara, CA 95050. **Circle 303**

Laser optical interface expands PC archiving

Optical disks and interfaces in the 007 series offer high capacity storage for microcomputers. They aim specifically at archival TI and IBM PC applications. The 007 is a desktop module providing up to 1000 Mbytes per replacement platter. A single replaceable laser platter can substitute for more than 200 reels of magnetic tape. The device comes complete with host interface, a multifunction controller, and laser optical disk. **National Memory Systems Corp**, 355 Earhart Way, Livermore, CA 94550. **Circle 304**

Data capture module improves programmable controller operation

Model 920 data capture modules enhance the sensitivity of programmable controllers by enabling them to receive signals of 2-μs duration. Optically coupled inputs and outputs provide complete isolation of the unit. LEDs make for easy setup and operation. The 920 comes in 5-, 15-, or 24-Vdc power modules. **Cincinnati Electrosystems, Inc**, 469 Wards Corner Rd, Loveland, OH 45140. **Circle 305**

SOPHIA SYSTEMS STANDS ALONE.

Now you can emulate without a host, target, or other add-on systems. Sophia SA700 personal and portable emulators for Z80™, 8085, 8086, 8087 and 8088 give you powerful, standalone micro development and debugging for less than $10,000. Nothing else compares.

Our disk-based emulators are floppy compatible with Intel Series II/III (ISIS), System 86/330 (iRMX86™), CP/M and CP/M-86™ systems. Plus with our serial link, you can easily connect hosts such as DEC VAX®-11 or IBM® PC, and download to our floppy disk for debug, storage, and program re-entry. Dramatically saving setup time.

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An international market leader of in-circuit emulators, Sophia Systems has delivered more than 3,000 SA700 systems worldwide since 1982. Each system comes with an extensive support program, including a one-year limited warranty, and is backed by our regional service centers.

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STANDARD FEATURES:

- Integrated floppy, CRT, keyboard & ICE™ probe
- Built-in PROM programmer
- Serial, parallel & external ports
- Real-time trace, timing & emulation
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- Multiple hardware breakpoints—CPU, memory, bus, external states
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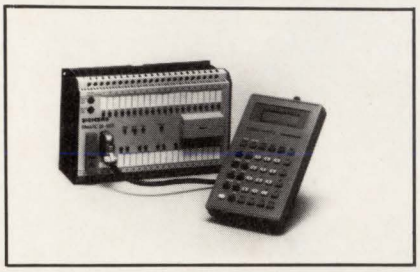
HELPING TO BRING YOUR DESIGNS TO MARKET FASTER.

Low cost programmable controller runs small machine applications



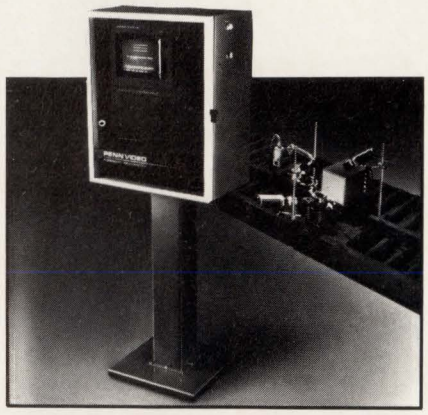
The Simatic S5-101R contains a power supply, processor, programmer interface, and signal I/Os. The handheld PG-605R programmer is used to enter instructions with a ladder diagram language. A CRT programming unit is also available. Contents of the 500-element RAM program memory is retained by an internal backup battery, even with the power off. A plug-in EPROM is also available for nonvolatile program storage without battery backup. **Siemens-Allis Automation, Inc**, PO Box 9128, Waltham, MA 02254.
Circle 306

Industrial miniature D-A converter is microprocessor-compatible

Packaged in a ceramic 28-pin DDIP, the HDSC2306 is a four-quad multiplying sin/cos DAC with 8- and 16-bit micro compatibility. It features up to 1 arc-min accuracy and 16-bit resolution. It requires ±15-V power supplies and offers a radius accuracy of 0.03 percent. Other features include double-buffered inputs, buffered reference input, dc-coupled reference and outputs, TTL/CMOS compatibility, and pin-programmable gain. Prices start at $180. **Natel Engineering Co, Inc**, 4550 Runway St, Simi Valley, CA 93063.
Circle 307

Vision system boasts easy operation in industrial settings

Factory preprogrammed, the Foresight machine vision system can automatically inspect, measure, identify, sort, and orient parts at production line speeds. Binary image processing, gray scale feature analysis, pattern recognition, measurement, and windowing are all available inspection techniques. Setup parameters for each application are user-initiated in response to prompts displayed on the monitor. Foresight links up to four cameras and provides either 320 x 240, or 640 x 485 resolution. Results of the image analysis can be used to automatically reject parts or to control a flexible manufacturing process. **Penn Video Inc**, 929 Sweitzer Ave, Akron, OH 44311.
Circle 308



Gould...Innovation and Quality in UNIX-based systems

Our Firebreathers are scorching old performance standards.

Gould's PowerNode™ 9000 blasts through UNIX* benchmarks at 4.5 times the speed of the VAX™ 11/780. Sound impossible? Give us your real production code or benchmarks and let us prove it.

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Now you can run software development and production at the same time, with highly responsive performance. Tightly coupled dual processors nearly double throughput and virtual memory accommodates large programs. Hardware fixed point and floating point accelerators retain high performance in heavy number-crunching situations. The PN9000 handles mainframe jobs in a multi-user UNIX system or serves as a backend processor in a widely distributed network.

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Gould's own high performance UNIX-based operating system (UTX/32™)—a unique combination of Berkeley 4.2 with special Bell System V features—makes it easy for you to use your VAX-based UNIX software. This allows easy conversion from your system to the increased power of a Firebreather.

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Gould's Compatibility Suite is a collection of application software packages that are compatible across the entire PowerSeries™ product line. Use C, Cobol, BASIC, or Pascal languages intermixed. This close-knit processor family offers all the advantages of a dedicated system plus the lower-cost-per-user option of sharing resources with Gould's standard networking capabilities including Ethernet™. The Firebreathers are the high end of the widest range of UNIX-based systems in the industry.

Gould's Firebreathers are scorching the UNIX market.

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Computer Systems Division
Distributed Systems Operation
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(305) 797-5459

GOULD
Electronics

Software combined with sensors to gather data for the PC

Temperature and pressure data can be measured and controlled via Anasoft, which runs on the IBM PC and PC compatibles. Monitoring, data acquisition, and process control jobs are defined, stored, and run according to information entered on the CRT screen. Anasoft uses Anafaze 8 MCS measurement hardware to gather data. Anasoft costs $295. Complete systems, including the computer and 28 analog inputs with eight control outputs, start at less than $4000. **Anafaze,** 519 La Honda Dr, PO Box 1840, Aptos, CA 95003. **Circle 309**

Industrial computer provides IBM PC/XT compatibility

The ISI 6160 consists of the system baseboard, 5 expansion slots, a 125-W power supply, and a cooling fan. Disk storage is one or two double-sided, double-density 5¼-in. floppy disk drives and optional 10-, 20-, or 30-Mbyte Winchesters. The system supports PC-compatible monochrome and color/graphics monitors and keyboards. Baseboard contains a 4.77-MHz 8088 CPU, space for an 8087, 128- to 256-Kbyte DRAM, a floppy disk controller, a battery-backed calendar/realtime clock, and data ports. **ISI International Corp,** 1275 Hammerwood Ave, Sunnyvale, CA 94089.
Circle 310

System allows realtime data transfer from "PC" to "PC"

Programmable controllers interface with the IBM PC via the FactoryCalc system. This system consists of Information Manager hardware and FactoryCalc software. The hardware consists of a standalone acquisition device that interfaces directly with diverse programmable controllers and has 64 Kbytes of battery-backed RAM. Hardware supports RS-232 and RS-422 communications. Communication rates range from 300 baud to 9.6 kbaud. VisiCalc compatible, FactoryCalc software brings the electronic spreadsheet to the factory. **MISA Corp**, Park 50, 100 Technecenter Dr, Milford, OH 45150.
Circle 311

Portable terminal withstands industrial settings

Aimed at industrial environments, the MAP-501 is a portable workstation terminal that can be linked to any ASCII-compatible control system with either an RS-232 or an RS-422 interface. Contained in a gasketed cast aluminum housing, the unit features a 65-position sealed membrane keyboard and 80-char LCD. Ten control keys and six user-definable function keys are provided. The machine has a 1280-char memory buffer that performs as a 16-line x 80-char terminal. The display is a one-line window into the 16-line buffer. Conversational and line edit modes are offered. MAP-501 costs $825. **Maple Systems, Inc**, 2615 W Casino Rd, Everett, WA 98204.
Circle 312

Industrial control derives from automation package

The Optomux line of I/O equipment links the IBM PC to industrial devices. It includes all the hardware needed to connect the PC serial port with over 4000 points of photo-isolated digital or analog I/O. Communication from host to Optomux is via a four-wire multiplex connection. The Opto 22 system consists of the IBM PC, adapter cards resident in the PC, the Optomux I/O system (including both analog and digital I/O modules), and a complete software driver package. **Opto 22,** 154561 Springdale St, Huntington Beach, CA 92649.
Circle 313

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

SOFTWARE

Implementation of ANSI Fortran 77 available for IBM PC

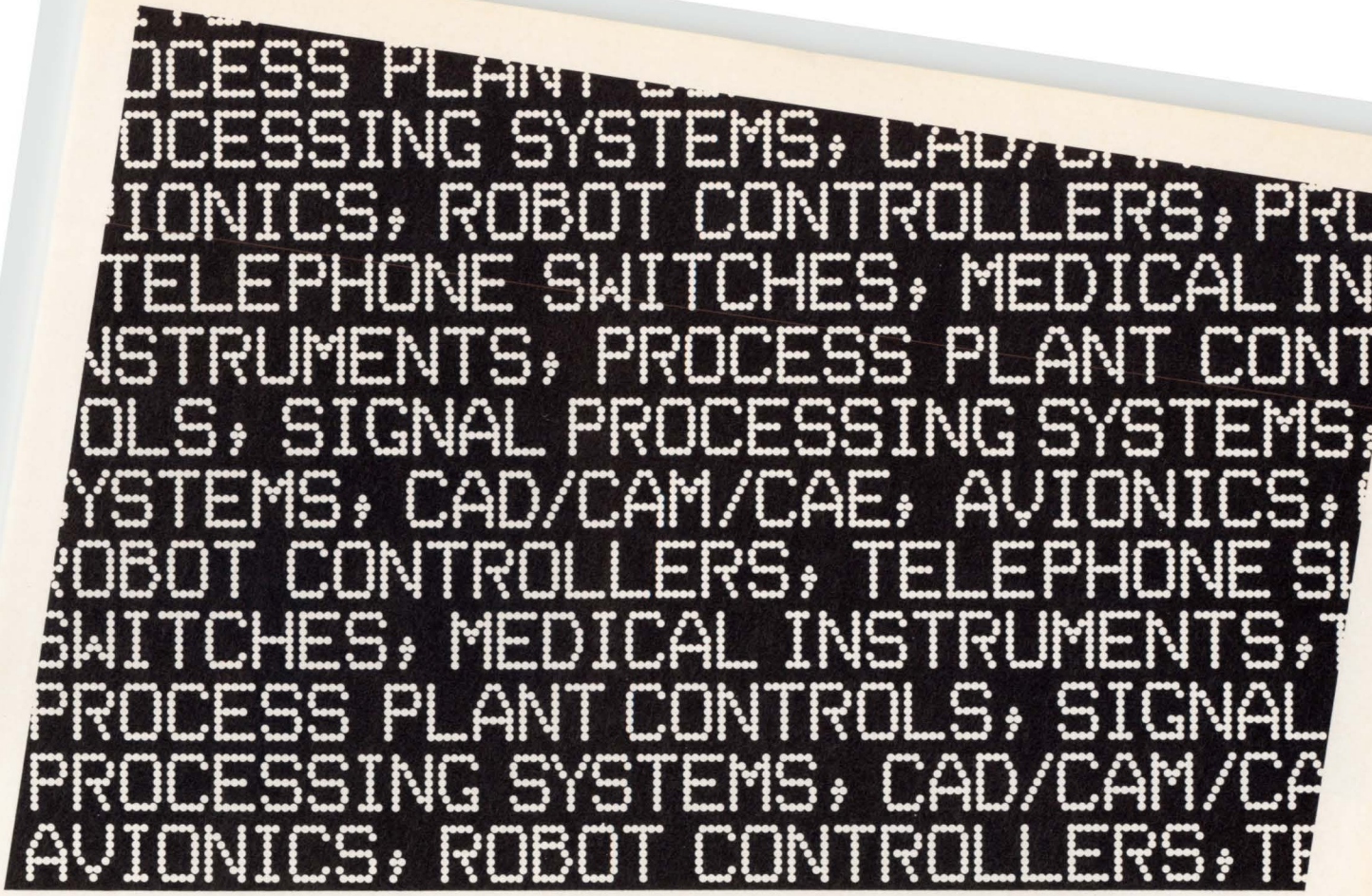
Designed for programmers who want mainframe features on an IBM PC, F77L provides four data types: real, logical, integer, and complex. It includes recursion and break handling, as well as include, option, and chain statements. IBM PC requirements include 256 Kbytes of memory and an 8087 math coprocessor. Source file is free format, comments begin with an asterisk, and continuation lines begin with an ampersand. The software supports the IEEE standard for floating point arithmetic. Cost is $477. **Lahey Computer Systems, Inc**, 904 Silver Spur Rd, Rolling Hills Estates, CA 90274.
Circle 314

AI language builds faster, larger expert systems

OPS83 is a compiler-based programming language designed to serve as a tool in expert system design. It integrates forward-chaining rule-based paradigms with procedural programming paradigms characteristic of Pascal, C, and Ada. The ability to call functions and subroutines from rules permits OPS83 to be more modular and easy to maintain. Tens of thousands of rules may theoretically be incorporated into a single program. Introductory license fees are $10,000 for the first machine and $6500 for each additional machine. **Production System Technologies, Inc**, 642 Gettysburg St, Pittsburgh, PA 15206. **Circle 315**

Kernel makes PC-DOS and MS-DOS multitasking and real time

OS/RT supports all functions needed for process management, dynamic interrupt control, memory allocations, and communications. It requires 10 to 12 Kbytes of memory depending on the features used. The software has resource management capabilities and 256 priority levels. It is written in C and will operate with any 8088 or 8086 CPU with DOS. In addition, it links with programs and run as a single task under DOS. The user has full keyboard, screen, printer, and disk I/O of DOS for DOS resource access. Price is $9600. **The Destek Group**, 830 E Evelyn Ave, Sunnyvale, CA 94086.
Circle 316



OUR MTOS REAL-TIME OPERATING SYSTEMS ARE THE NUMBER ONE CHOICE FOR CONTROL APPLICATIONS WORLDWIDE.

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MTOS is the only system that will control several microprocessors on a common bus. For advanced applications such as vision systems and signal processing, this unique capability is indispensable.

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To learn more about real-time operating systems in general, and MTOS in particular, call or write for our free booklet "On Operating Systems." Industrial Programming, Inc., 100 Jericho Quadrangle, Jericho, NY 11753. Telephone: 800-228-MTOS (in New York State call 516-938-6600). Telex 429808 (ITT).

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The standard-setter in operating system software.

ipi Industrial Programming Inc.

CIRCLE 106

Icon-driven image editor turns real life pictures into computer graphics

An interactive image creator and picture editor with video digitizer support runs on the IBM PC. Known as IMiGIT, the package adds full color graphics editing and composition power to the system. IMiGIT allows multifont annotation, texturing, color-fill, and integration of photos, drawings, logos or scenery. Easily recognizable icons make for quick self-training. The ability to capture and edit high resolution images (up to 640 x 512 pixels) viewed by a standard video camera is a key function. With PC-Eye, a plug-in option board for image capture, the IMiGIT package costs $695. **Chorus Data Systems**, 6 Continental Blvd, PO Box 370, Merrimack, NH. **Circle 317**

Engineering Basic runs on the DEC VAX and IBM PC

A key feature of TBasic is its compatibility with Tektronix 4050 Basic. With TBasic, IEEE 488-compatible instruments can be controlled from a DEC VAX or PC using a Basic that is compatible with the Basic on a dedicated Tektronix GPIB controller. Because it is an incrementally compiled language, syntax checking is done immediately. Features include advanced graphics functions, double precision and integer data types, line labels, and random and sequential data files. The PC version costs $795 and the VAX version is $2000. **National Instruments**, 12109 Technology Blvd, Austin, TX 78727. **Circle 318**

Expert system release enhanced by database query language

An artificial intelligence software product, KEE (for Knowledge Engineering Environment), is updated with a 2.0 release. This system helps users construct knowledge-based (or expert) systems. KEE 2.0 is aimed at providing functional and structural representations of an individual's expertise. The system includes a logic-based language called TellAndTalk. This is a database query language that structures knowledge so that the system can deduce facts that were not explicitly stated. TellAndAsk provides for the use of variables in queries. The 2.0 release also includes the Rule System 2, which makes use of TellAndTalk assertion and retrieval facilities. **IntelliCorp**, 707 Laurel St, Menlo Park, CA 94025. **Circle 319**

Optimized C compiler aims at DOS 2.0 environments

The MWC86, a C programming system for DOS 2.0 environments, allows programmers to debug in C. This optimized C compiler features common code elimination, peephole optimization, and register variables. It supports the full C language, including recent enhancements. MWC86 features large and small models of compilation, the 8087 math coprocessor, and DOS 2.0 path names. The system also includes a program that allows the programmer to set trace points on variables and expressions with full history capability. Programmers can single step through a program, or interactively evaluate expressions to trap bugs. This system is available for $495. **Mark Williams Co**, 1430 W Wrightwood Ave, Chicago, IL 60614.

Circle 320

Enhancements provided by VS Fortran update

Release 4 of VS Fortran implements the Autodble option, compiler-generated reentrant object code, support for VSAM data sets and runtime load capability. On request, the compiler will automatically increase the precision of real data. It allows users to access information directly by keyed data as well as sequentially or by record number. It lets multiple users share a program in memory without loading multiple copies of the same program in each user's virtual storage. Initial license charge is $699. **IBM Corp**, 900 King St, Rye Brook, NY 10573. **Circle 321**

Operating system enhances multi-user communication for PC compatible

An NS-DOS 1.1 package updates the North Star Dimension microcomputer operating system. The multi-user PC-compatible Dimension system, running NS-DOS 1.1, allows data sharing among several users. Software locks at the record level, letting different users simultaneously update information that is stored in different records within the same file. Multi-user applications (eg, dBase II, and Software Connections' Datastore and Datacore) that are written to take advantage of 3Com/Ethernet semaphores now run on the Dimension. **North Star Computer, Inc**, 14440 Catalina St, San Leandro, CA 94577. **Circle 322**

Pascal compiler runs on TRS-Xenix system

A Pascal-2 compiler provides an alternative to C (and RM/Fortran 77, macro-assembler and assembler) for users of the TRS-Xenix operating system. This yields the benefits of Pascal's compile- and run-time error checking as well as readable syntax for debugging and maintenance. The TRS-Xenix software base is accessible because Pascal-2 programs can call subroutines written in C or assembler. Code optimizations include global register allocation, common subexpression elimination, branch-tail merging, constant folding, and dead code elimination. The license fee for the Pascal-2/Xenix system is $699. **Oregon Software, Inc**, 2340 SW Canyon Rd, Portland, OR 97201. **Circle 323**

When you want the ASCII terminal that leads the field in performance, we'll be there.

Now there's an affordable all-purpose editing terminal that's ahead of the pace in quality, performance, and reliability: Qume's new QVT 109™. It comes to you with a full *one-year* warranty. Though that's twice the warranty of most other ASCII terminals, over 98% of our customers never need it. Qume quality control is *that* good.

The QVT 109 also leads the pack in performance, with 19 programmable function keys (38 functions) that can perform a sequence of tasks at a keystroke. There's a capacitive keyboard that combines the responsive touch of a typewriter with ruggedness that stands up to heavy-duty, all-day use. What's more, you're backed by our nationwide service network, as well as our vast resources and solid experience as an ITT company. You can depend on Qume to keep pace with your needs in the years ahead.

For more information about Qume's new QVT 109, our other alphanumeric and graphics terminals, or our full line of daisywheel printers and disk drives, call (800) 223-2479. Or write Qume Corporation, 2350 Qume Drive, San Jose, CA 95131.

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QVT 109™

CIRCLE 107

Port selector ties computer and terminals together

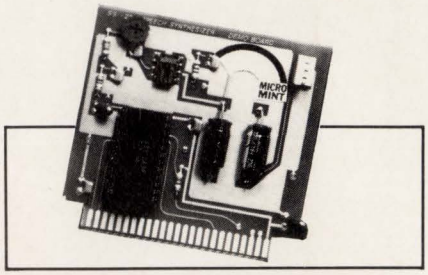
The DSS-1 data PBX uses programmed array logic to reduce dimensions. From 24 to 1320 asynchronous computer ports and terminals can connect simultaneously at 9600 bits/s due to a nonblocking architecture. It forms the hub of a LAN providing user controlled switching, port contention for increased use, and access control with network management. For reliability, standby power supplies, switching logic, and backplane with auto switchover are provided. The basic central unit costs $8800, plus $75 to $100 per line. **Equinox Systems**, 12041 SW 144th St, Miami, FL 33186.
Circle 324

LAN system runs under DOS 3.0 for IBM AT

Operating on PC-DOS, MS-DOS 2.0 and higher, the 10-net release 2.0 can be used on the IBM PC, PC XT, and compatibles. These can all be intermixed with PC ATs in the same LAN. The system includes circuit board, tap box, software, circuit board/interface card that plugs into the bus slot on the PC and attaches through twisted-pair wires to other PCs. Software features include the ability to preserve data when multiple users simultaneously request the same record and provides file access security. **Fox Research, Inc**, 7005 Corporate Way, Dayton, OH 45459.
Circle 325

Speech synthesizer runs with data rates as low as 50 bits/s

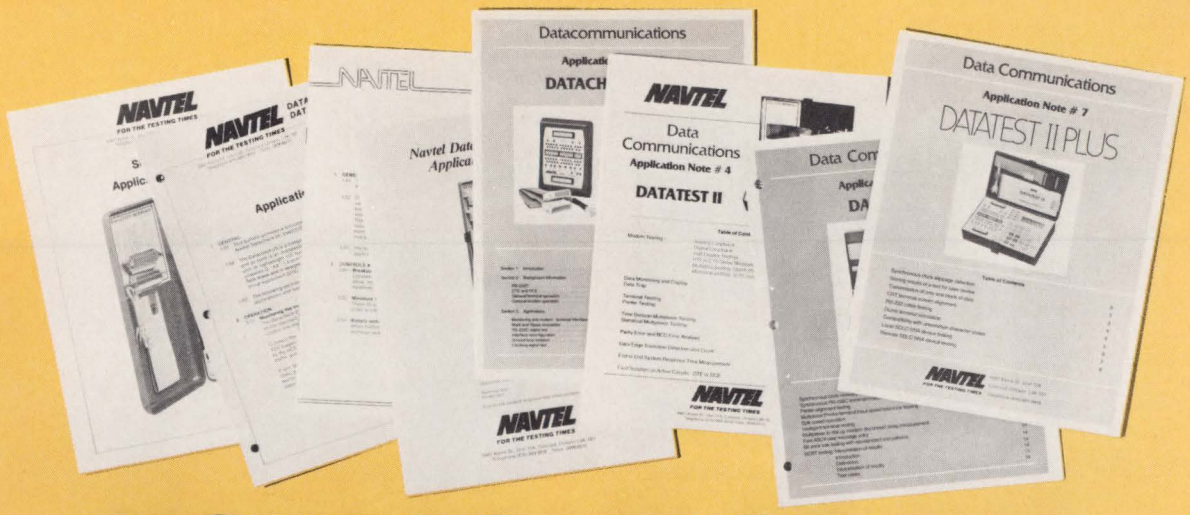
Sweet Talker II is based on the SSI 263 IC. The device can synthesize human singing at rates of no more than 400 bits/s. Phoneme values can be set on the five internal registers. The SSI 263 chip works from a 3.59-MHz color burst crystal divided by a 2- or 4- or a 1- or 2-MHz clock base. It is microprocessor-compatible and operates on a 5-V supply. Control inputs are available for address mapping with several buses. Features include 256 phoneme equivalents, 4096 pitch variations, and an onboard 1-W



amp with volume control. Price is $104. **Micromint, Inc**, 561 Willow Ave, Cedarhurst, NY 11516.
Circle 326

Systems integrate network control and planning functions

The NCS/70 series consists of the 7005 model and the 7020 version. The 7020 features realtime network error and status message displays with intelligent error trapping for rapid diagnosis of error conditions. A standard software package allows use of IBM PCs or compatibles as network control terminals. The unit can generate a detailed message measurement record for each transaction on the network. **Emcom Corp**, 800 E Campbell Rd, PO Box 741715, Dallas, TX 75243.
Circle 327



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Navtel manufactures a complete series of test sets including Datatest I, II, and Datatest II PLUS, with features such as BERT testing, dataline monitoring, flexible format polling, optional X.25 level 2 and 3 testing, Datacheck I, II, III, and IV, the ultimate breakout boxes, plus the Datatest 25 BERT tester and a wide range of interface problem solvers including gender changers, turnover adapters and more.

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INSTRUMENTS

Turn Your IBM PC Into A Development System

Now Kontron offers software development tools, in-circuit emulators, and logic analyzers to make your IBM PC an integral part of a universal development system.

With the Kontron approach, you choose from personality modules for over thirty 8- and 16-bit microprocessors, for the device that's best for your project—*not* the one that happens to work with your machine.

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You get a system that's networkable via Ethernet to other Kontron development systems and to DEC minicomputers.

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With Kontron's help, the PC on your desk can be a lot more powerful than you ever imagined. Kontron software tools include "C" and PASCAL high-level languages, plus assemblers, linkers and high-powered utilities. The in-circuit emulators feature full-speed execution, hardware breakpoints, memory mapping and interrupt control, and the logic analyzers provide 64 channels, with a 100 MHz sample rate and 8K samples.

For more information, contact

Kontron Electronics Inc.,
630 Price Avenue, Redwood City, CA 94063, 800/227-8834 (415/361-1012 in California);

D-8057 Eching/Munich, West Germany, Breslauer Str. 2, 089/3 1901-0.

ADVANCED ELECTRONIC INSTRUMENTATION

KONTRON ELECTRONICS

Circle 110 for Literature

Circle 111 for Demonstration

ARC network opens up to PC system connection

Products including a networking package for the IBM PC herald the opening of Datapoint's ARCnet to heterogeneous system connection. The Intelligent Network Executive-PC (INX-PC), a user-installable interface card, allows alternation between PC-DOS and Datapoint DOS. Further ARCnet enhancements include a Vista-PC connection, direct network interface, and a software package that allows computers attached to an ARC network to execute CP/M application programs. The latter product allows users to switch between PC-DOS and CP/M operating systems. The INX-PC card and software cost $770 per PC. Pricing for the CP/M context switcher (the Intelligent Network Executive for CP/M) is $595 per file processor. **Datapoint Corp**, 9725 Datapoint Dr, San Antonio, TX 78284. **Circle 328**

Ethernet PC interconnect melds with multiple systems

Ethernet Direct Connect (EDC) consists of an Ethernet controller and networking software. It provides complete transport service to higher level applications running on a personal computer. MS-DOS networking software is based on the Xerox ITP. Accessed by a menu-driven utility, a diagnostic application program conducts an internal test of Ethernet controller functions as well as a check of network connections with transceiver loopback and network echo. Price is $775. **Interlan, Inc**, 3 Lyberty Way, Westford, MA 01886.
Circle 329

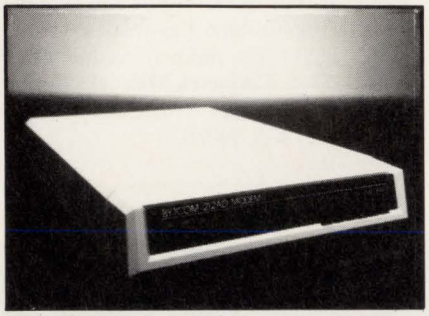
Voice mixes with data in T-1 style multiplexer

Called Omnimux T-1, a time division multiplexer blends voice with asynchronous and synchronous data transmission. It supports voice channels with bandwidth requirements of 16, 32, 48, and 64 Kbits/s, as well as all standard 110-bit/s to 460.8-Kbit/s data channels. It also combines many data and voice channels over wideband circuits. These include special telephone carriers that operate at data rates of 1.544 Mbits/s by North American standards, or 2.048 Mbits/s by European standards. A 44-channel single-chassis Omnimux T-1, supporting RS-232 data, costs about $35,000. **Racal-Milgo**, 8600 NW 41st St, Miami, FL 33166. **Circle 330**

Module touts compatibility with Smartmodem 1200 and Bell 212A

A Hayes-compatible modem, the CH1765, aims at remote data transmission applications. This 16-in.^{2} module is designed to mount on the host's PC board. The CH1765, which also offers Bell 212A compatibility, features electronic call progress tone detection for on-screen display of call status and provides built-in impairment diagnostics. In integrator quantities, modem module prices start at $165. **Cermetek Microelectronics, Inc**, 1308 Borregas Ave, PO Box 3565, Sunnyvale, CA 94088.
Circle 331

Remote boot upgrades intelligent modem



The 212AD intelligent modem gains a "remote boot" feature that allows it to reset a computer from distant locations. A user can wire the reset button, or bootstrap, of the computer to the modem. The modem in turn, upon receipt of a programmable two-character control sequence, toggles an internal switch that resets the computer. The 212AD is a direct connect modem that can store 10 names and numbers of up to 40 chars each. Capabilities include auto-linking, a help menu, and software disconnect. The modem supports synchronous and asynchronous transmission. Price is $495. **Bytcom, Inc,** 2169 Francisco Blvd, San Rafael, CA 94901. **Circle 332**

Three-wire communication interface expands the 8050

Designated the NS 8050U, an enhanced version of the 8050 microcontroller offers expanded communications via a built-in, three-wire serial communication port. The 8050U uses an expanded 8048 instruction set with three I/O pins assigned to the Microwire Plus interface. This enables serial communication between two or more 8050Us or Microwire peripherals. The interface allows serial data exchange with only three wires via a serial I/O port that is essentially an 8-bit clocked shift register. The device is available in both 6- and 11-MHz clock speeds for both commercial and extended temperature ranges. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 333**

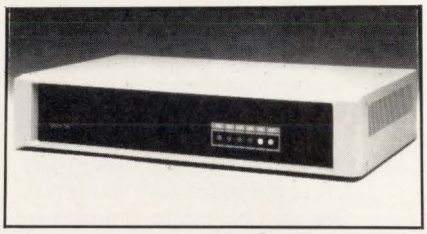
Modems automatically switch voice and data

IPI-1200 fits inside the IBM PC or compatibles while the IPX-1200 is an external standalone version for RS-232 interface machines. The modems feature 300/1200 baud, full duplex, auto dial, auto answer, pulse and touch tone, and full call progress monitoring. They support the Hayes Smartmodem commands and screen responses, but can also be extended to offer more complete on-screen call progress monitoring. Both are fully compatible with Bell 103, 113, and 212A dial up modems. The internal modem is $370, while the external model costs $129.95. **Transend Corp,** 2190 Paragon Dr, San Jose, CA 95131. **Circle 334**

Cable modems transmit up to 3 mi at 9.6 kbaud

Alternatives to RS-232 cabling—virtual cable modems—are available with male connectors (the model 81), female connectors (the model 81F), or phone plugs (the 81P). The model 81 is a full-duplex short haul modem for asynchronous transmission over two twisted-pair wires. Operation is provided up to 1 mi at 19.2 kbaud and 3 mi at 9.6 kbaud. The transmission scheme features a balanced driver similar to RS-422 that complies with Bell System Publication 43401. The model 81 is packaged in a 2.2- x 3.5- x 1-in. (5.5- x 8.9- x 2.5-cm) box. Cost is $58.50 at quantity-250. **Telebyte Technology Inc,** 148 New York Ave, Halesite, NY 11743. **Circle 335**

Modems work at 4.8 and 9.6 Kbits/s and cover CCITT protocols



Mark 48 and Mark 96 modems are online compatible with the Omnimode and MPS modem families. They can also operate as CCITT V.27 bis or V.29 compatible modems for international applications. This line features ease of installation, automatic adaptive equalization, and fast turn-around times of 19-ms RTS/CTS at 4.8 kbits/s and 30-ms RTS/CTS at 9.6 kbits/s for multidrop application. Custom MOS/LSI technology ensures efficient performance over dedicated unconditioned lines in either point-to-point or multidrop configurations. The 48 and 96 are available for $1500 and $2500, respectively. **Racal-Milgo,** 8600 NW 41st St, Miami, FL 33166. **Circle 336**

Package runs phone call history on VAX and PDP-11

Call Tracker provides a telephone history data base and auto-dial features. The Call Tracker keeps track of who to call, when to call, and what was said in past conversations. Written in Dibol, the package runs under DEC RSTS/E or VAX VMS, and can handle as many users as there are terminals. The package allows self-teaching by guiding the user with menus and simple messages. Software and hardware can be purchased separately. The RSTS/E version of Call Tracker sells for $2500 (plus $160 per dialer). The VMS version is $300 plus dialer charge. **Origin, Inc,** 9136 Gibson St, Los Angeles, CA 90034. **Circle 337**

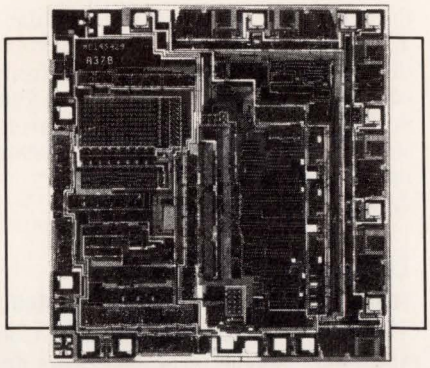
Communication software lets heterogeneous systems converse

An IBM mainframe-based communications software tool—transNET—lets incompatible office systems exchange text, data, and programs. Through SNA, transNET provides communication among systems using IBM's Document Interchange Architecture and Document Content Architecture. The product supports the IBM 5520 system and peripheral devices, IBM Displaywriter, IBM 3270-compatible terminals, WANG OIS and VS systems, as well as IBM PC Display Write II and Multimate word processing software. A modular system allowing features to be added as needed, transNET's base price is $35,000 with added features ranging from $2000 to $35,000 each. **Network Applications, Inc,** 9020 Capital of Texas Highway N, Austin, TX 78759. **Circle 338**

Switching matrix directly connects to 8-bit microprocessor

A switching matrix, dubbed the MO88, handles large scale digital switching functions. The MO88 implements a "not-blocking" time switching matrix of 256 x 256 pulse code modulation channels. The device can connect and disconnect any input channel to any output channel. The MO88 is designed to be connected directly to the bus on an 8-bit microprocessor. This component integrates speech memory, control memory, internal PCM bus, parallel-to-serial conversion for the PCM output links, and control and interface logic to and from the microprocessor. Price is $78 each in quantities of 100 or more. **SGS Semiconductor Corp,** 1000 E Bell Rd, Phoenix, AZ 85022. **Circle 339**

Telecomm interface device converts async to sync

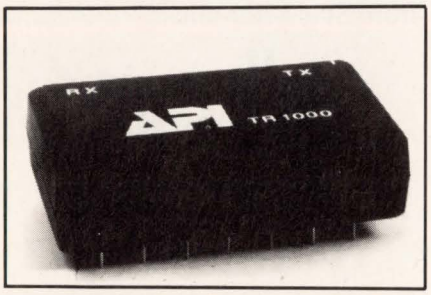


The MC14529 circuit is designed to ease implementation of asynchronous data ports to synchronous channels of universal data link transceiver (UDLT) products. This RS-232-compatible, CMOS device is also known as the telset audio interface circuit. It has a digital subsystem that allows interface to a microcomputer and generates configuration control signals for the chip's analog subsystem. The analog subsystem handles low pass filtering, audio signal routing, gain adjustment, and signal summing required for a digital or analog telset application. Pricing in quantities of 1000 is $4.86. **Motorola Inc, Logic and Special Functions Products Div**, 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 340

Fiber optic transceiver data rates set at 100 Mbits/s

High speed fiber optic transceivers in the TR1001S series can send data at rates of up to 100 Mbits/s. Two versions are available—the TR1001SA with an 8-dB system margin and a surface LED; and the TR100SB, which offers a system margin of 17 dB using a high power edge LED. The TR1001SA and TR101AB sell for $275 and $550, respectively, in quantities of 1 to 24. **American Photonics Inc**, 71 Commerce Dr, PO Box 289, Broolfield Center, CT 06805.



Circle 341

Package interfaces iRMX 86 setups with network development systems

The iRMX-NDS-II Link, a software utility package, connects iRMX 86 systems with the NDS-II net developer. (The NDS-II is a multi-user microprocessor development system that links all 8- and 16-bit Intel development systems in a unified engineering environment.) Using a 10-Mbyte Ethernet to link iRMX systems 86/310, 86/330A, or 86/380 with mass storage and line printer units, the Link environment includes database and resource sharing, hierarchical file structures, and remote job execution. The iRMX-NDS-II Link software license is $2500 for eight copies. The Ethernet controller handset costs $2000. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 342

Multiplexer integrates data, voice, and compressed video

Using bit-interleaved time division multiplexing to combine up to 128 diverse channels into a single data stream, the 430 T-Plexer merges several kinds of high volume transmission. Voice, data, and compressed video travel over T1 (and other) lines. Multiple channel interfaces can be accommodated. These include RS-232-C/CCITT V.24, CCITT V.35, and the 64-Kbit/s Plexerlink. A drop-and-insert feature supports multipoint applications for increased network flexibility and optimized bandwidth use. **Tellabs, Inc**, 4951 Indiana Ave, Lisle, IL 60532.

Circle 343

Network is configured along lines of NBS model

The commercial version of the National Bureau of Standards NBSNET is called TIENET. It allows extended local area networking of diverse computers and peripherals, a 1-Mbit/s aggregate data rate, and cable lengths of up to 5 mi. As many as 1600 users can interconnect via one TIENET cable segment up to 2 mi long. The maximum number of station connections is 24,000. Station data rates can reach 9.6 kbaud for terminals and 19.2 kbaud for computers. The cost of TIENET is from $626 to $910 per connection from 200 down to 12 stations. **Pragmatronics, Inc**, 2015 10th St, Boulder, CO 80302.

Circle 344

Intelligent interface module handles X.25 interfacing

The CC-5656 is an intelligent communication controller designed for a Multibus system. Its single-board design conforms to the IEEE 796 bus standard and supports 12 serial I/O ports plus 16 lines of parallel I/O with handshaking. Hardware includes an MD68B09 processor running at 1.8432 MHz, 64 Kbytes of CMOS static RAM dual ported between the 6809 and the Multibus, and six Z8030s for multiprotocol serial communication. Software uses an executive program to interface between a Multibus system, the hardware I/O support, and various I/O protocol programs running on the board. One of three available protocol programs supports the frame and physical levels of X.25. **Symbicon Assoc, Inc**, 89 Route 101A, Amherst, NH 03031.

Circle 345

Silicon compilation system shrinks design cycles

The Genesil design automation system can describe designs in terms of high level functions and then quickly produce quality VLSI chips. This silicon compiler handles all VLSI development steps following functional description and preceding actual chip manufacture using the methods of expert VLSI designers. It is a turnkey system comprising a DEC VAX-11/750 with 4 Mbytes of main memory, a 450-Mbyte disk storage system, tape storage, and four high resolution color terminals. Software provides IC definition, simulation, timing analysis, and testout. The system sells for $545,000. A CMOS function set will be available early next year. **Silicon Compilers, Inc**, 105 Albright Way, Los Gatos, CA 95030.
Circle 346

Graphics station uses LSI-11/73, paints 256 simultaneous colors

Colorware System 73 graphics workstations use an LSI-11/73 CPU with 16/32-bit architecture. System 73 provides local processing and data storage, and is offered in three models—the 73/10, 73/7, and 73/5. Screen resolutions measure 1024 x 768, 768 x 575, and 512 x 483. Each system has 256 simultaneously displayable colors from a palette of 16.7 million. A 19-in. monitor is used. Additional standard graphics features include firmware anti-aliasing, hardcopy interface, a 90-command protocol, and complex polygon fills. Independent manipulation of eight video memory planes, through use of read/write masking, permits user-developed overlays. **Advanced Electronics Design, Inc**, 440 Potrero Ave, Sunnyvale, CA 94086.
Circle 347

Access time tester measures performance of memories and gates

Featuring 1-ns resolution over the whole 0- to 390-ns measurement range, the AT700 access time tester verifies specs and measures device degradation caused by voltage, current, heat, or other environmental conditions. Gates, ROMs, PROMs, SRAMs, and buffers are among the devices the AT700 can test. Test conditions, which can be stored in nonvolatile memory, are entered from a front panel. An alphanumeric LCD readout presents test results. The AT700 is priced at $2850. **Hilevel Technology, Inc**, 18902 Bardeen Way, Irvine, CA 92715.
Circle 348

Emulators configure for realtime performance in 8-bit systems

The 9610 series plug into both the Colt and Atlas systems. The emulators are available for Z80, 8085, and 6809 micros. Each features a full 64-Kbyte memory, that may be mapped in 256-byte blocks, and unrestricted use of I/O ports and interrupts. Phantom memory blocks allow the user to insert two additional code segments into the program. A view mode displays all register contents, CPU status, and selected I/O port contents. Emulators are priced at $5300, complete with software. **Dolch Logic Instruments, Inc**, 2029 O'Toole Ave, San Jose, CA 95131.
Circle 349

SYNC THE UNSYNCABLE

It's time to get in sync with a revolutionary idea: High-density CMOS static memories that interconnect systems in ways never before possible. We call them BiPORT™ memories. Because unlike any other memory devices, they read and write at the same time.

The first in the series is the MK4501 FIFO, an asynchronous device that's organized 512 x 9 in a 28-pin DIP. It's the fastest, highest-density rate buffer available for interfacing fast processors with slower peripherals.

But that's only a glimmer of application potential. Now consider true parallel computing.

Quite simply, the MK4501 and future BiPORT memories enable you to synchronize processors with different clock rates so that they can communicate with each other. Without complicated arbitration circuitry. What's more, BiPORT memories are fully expandable by word size as well as depth.

All of which means that you can now create the equivalent of a much larger system. For a fraction of the cost.

The possibilities? As far as your imagination can take you. And all you have to do is get in sync. For more information, contact Mostek, 1215 W. Crosby Road, MS2205, Carrollton, Texas 75006 (214) 466-6000. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 296.886.

BiPORT is a trademark of Mostek Corporation.

UNITED TECHNOLOGIES MOSTEK

CIRCLE 115

Programmable system offers subnanosecond rise times

The 2000 series offers programmable subnanosecond rise times and all digital calibration that eliminates the need for manual internal adjustments. It has burst, double pulse, and invert modes with pulse repetition frequency of 1 s to 5 ns internal period the 200-MHz generator's rise and fall times are less than 1 ns for the 5-V ouput model and less than 2 ns for the 10-V version. Programming accuracy results in frequency, delay, and width errors of less than one percent, and rise and fall times within 3 percent. Prices range from $13,500 to $15,500. **E-H Electronics**, 7303 Edgewater Dr, Oakland, CA 94621. **Circle 350**

Bit-slice microprogram development facility runs under Unix

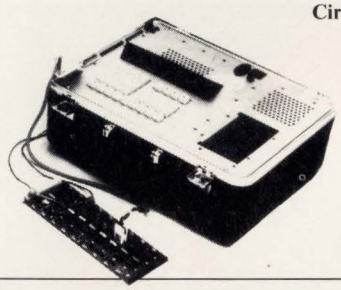
The facility consists of five programs. All are written in C and the source code is provided. Assembler software provides user defined word lengths. Object code files can be sliced into PROM-sized files and transmitted to a PROM programmer. The object file can be downloaded into the Step Engineering PROM emulator. Single CPU source code license is $5000 and additional licenses are $2500 per CPU. The source code is transmitted on 9-track, 800/1600-bit/in. mag tape. **Pacific Computer Sales, Inc**, 100 S Cole Rd, Boise, ID 83709.

Circle 351

Portable in-circuit tester works at component level

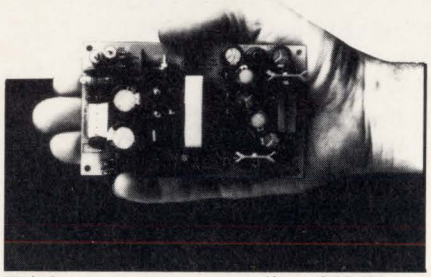
An in-circuit tester, the AFD-48, aims at cutting time in the repair pipeline. A chip-to-chip tutorial guides operators through test procedures. Components that can be tested inlcude opto-isolators, op amps, TTL, DTL, LSI, CMOS, and UARTs. Each testing step takes just 12 ms. The unit is housed in an 18- x 15- x 9-in. case, and weighs 30 lb. The AFD-48 sells for $22,500. **Roan Instruments**, 5655 Lindero Canyon Rd, Westlake Village, CA 91362.

Circle 352



PACKAGING & POWER

Switching power supply redefines the ultraminiature realm



Triple output power supplies of 30 W are key to the 3030 series. For example, the 3030-1 board measures 3- x 5- x 1.8-in. (76.2- x 127- x 45.7-mm), and weighs 0.5 lb. These compact units operate with low output noise and feature 4000 Vac I/O isolation, tight line/load regulation, and user-selectable input voltage ranges of 90 to 130 Vac and 180 to 250 Vac. Cost is $69. **Power General**, 152 Will Dr, PO Box 189, Canton, MA 02021 **Circle 353**

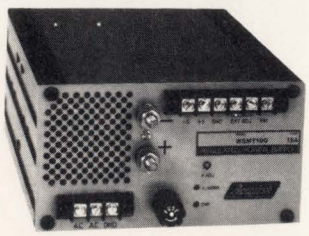
High power switcher incorporates protection features

The 5-output 121 switching power supply is designed to meet VDE 0806 international safety requirements, as well as VDE 0871 radiation specs. It provides line and load regulation of ±1 percent, and low ripple and noise of 1 percent peak to peak. Voltage and overload protection and thermal safeguards are standard features. The device can be used as a single power source for CPU and disk drives. The five outputs include a main 5 V at 60-A output, two 12 V at 10-A outputs, a 12 V at 5-A output, and a 12 V at 5-A output. **National Power Technology**, 2111 Howell Ave, Anaheim, CA 92806.

Circle 354

MOSFET circuitry running at 55 kHz highlights supplies

Series W power supplies provide outputs ranging from 5 Vdc/100 A to 48 Vdc/12 A. MOSFET switching circuitry operating at 55 kHz has reduced component count and increased efficiency compared to comparably rated bipolar designs. Line and load regulation are ± 0.05 percent. The units measure 3.4 x 6.3 x 9.3 in. (8.7 x 16.1 x 23.5 cm). LED indicators signal normal operation and overvoltage protection circuit latchup. Price is $950. **Acopian Corp**, Easton, PA 18042.



Circle 355

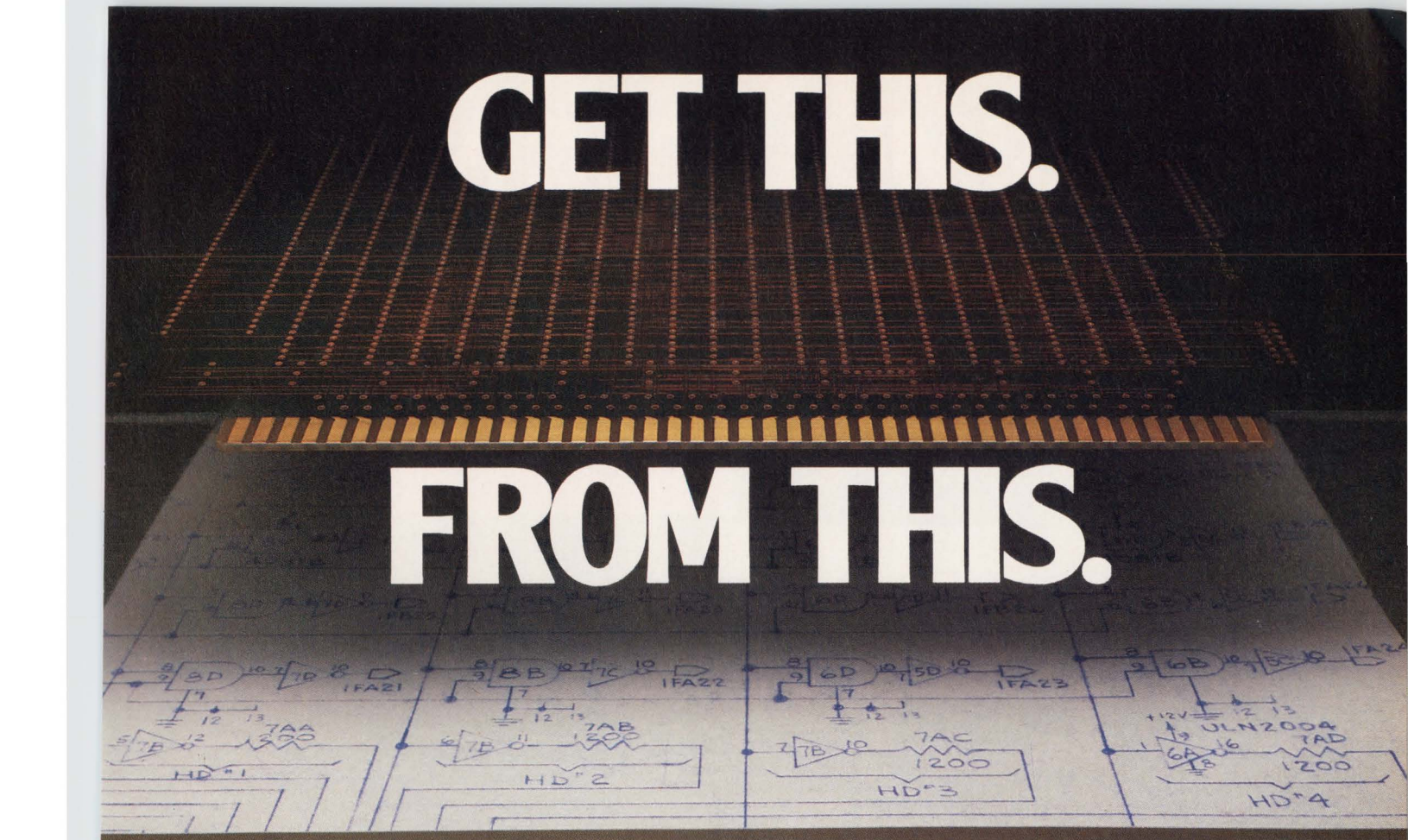
Battery with 100-mA hour capacity apt for microcomputers

Circuit Guard 3.6 is a rechargeable NiCad battery rated at 3.6 Vdc nominal. Designed as a memory backup power supply for microprocessor controls and single-chip microcomputers, this unit comes in two models: a standard temperature cell and a high temperature cell. Featuring 100-mA-hour capacity, the unit is pin-for-pin comparable to GE's Data Sentry and Matsushita's Memory Mount. It is board mountable with DIP-compatible pins and is sealed in a solvent-resistant plastic case. **Telecommunication Devices, Inc**, 2320 Wisconsin Ave, Downers Grove, IL 60615.

Circle 356

Power converter works with portable test equipment

The model 5910 power converter is designed for use with Tau-tron portable test equipment. A compact, self-contained, power conversion system that runs over a −20 to −60 Vdc/Ω range, the unit delivers up to 120 W of continuous output power. The 5910 has a thermostatically controlled output circuit. In the event that the internal heat sink temperature rises above 70 °C, the output power to the load will shut off. When the heat sink temperature drops below 55 °C, power is reapplied to the load. The model 5910 power converter costs $1000. **Tau-tron Inc**, 27 Industrial Ave, Chelmsford MA 01824. **Circle 357**



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CIRCLE 117

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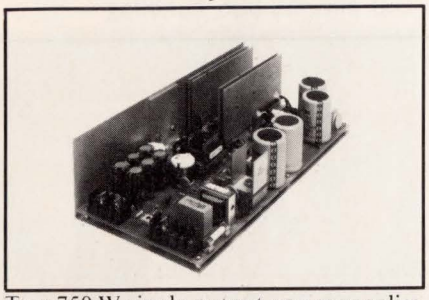

Two 750 W single-output power supplies offer high power density, low noise ouput, and fast dynamic response. The SFG-24-30 provides 24 V at 30 A and the SFG-48-15 provides 48 V at 15 A. MTBF is in excess of 10,000 hours. Outputs are adjustable and line and load regulation is ±0.5 percent. Switching frequency is 50 kHz and remote sensing is standard. Strap selectable ac input may vary from 90 to 132 V or 180 to 240 V, 47 to 63 Hz. Soft start circuitry, containing a distributed rfi filter, limits in-rush current at turn on. Pricing is $419 in 100s. **Todd Products Corp**, 50 Emjay Blvd, Brentwood, NY 11717. **Circle 358**

Load management highlights switching power supply

A 1000-W switching power supply offers three load management techniques for optimizing parallel operation: stress sharing, downslope regulation, and selective overvoltage shutdown. These load management features are packaged internally and require no external balance control circuits, load sharing cables, or master/slave signaling. Thermal stress sharing helps equalize thermal stresses, eliminating premature thermal shutdown. Output is 5 Vdc at 200 A. Designated model FS102B5, the unit is available in sample quantities. **Lorain Products**, 1122 F St, Lorain, OH 44052. **Circle 359**

UPS device aims at microcomputer applications

A UPS for microcomputers and microprocessor-based equipment is called the 300 Micro-UPS. Rated at over 300 VA (240 W), the device can support a typically configured PC/XT for 20 min and it can support a fully loaded PC through a 10-min power outage. The model 300 Micro-UPS sells for $695. **Triad Power Systems**, 10362 Miller Rd, Dallas, TX 75238. **Circle 360**

Transient suppressors have built-in 120-Vac equipment protection

Instead of being plugged into the front-end line cord, the 587B series is intended to be hardwired into equipment between the power switch and supply. It meets and exceeds the IEEE 587 standard and allows lower voltage design components. The device guarantees that line to neutral voltages will not exceed 350 V under worst-case conditions. The series also offers subnanosecond response time, short circuit failure mode, and no voltage overshoot. Models are available with operating currents of 5, 15, and 20 A. **General Semiconductor Industries, Inc**, 2001 W Tenth Pl, Tempe, AZ 85281. **Circle 361**

Industrial computer offers basic multitasking plus enhancements

For industrial applications, the IMC-4400 computer includes command line input filter software for auto-correction of user inputs. Multitasking (with enhancements), industrial I/O packaging, as well as diagnostic and screen-formatting utility packages round out the system. The IMC-4400 can monitor a cluster of programmable controllers or serve as a data gateway for multiple sources. It weighs 17 lb (3.3 kg) and measures 10.78 x 3.75 x 25.06 in. (273.8 x 95.2 x 636.5 mm). **Gould Inc**, 1280 E Big Beaver Rd, Troy, MI 48084. **Circle 362**

Briefcase portable sports 16-line LCD and MS-DOS bundling

The Pivot is a fully portable, PC-compatible, 16-bit computer. The machine has a built-in modem and calculator, plus 128 Kbytes of memory, which is expandable to 512 Kbytes. Choice of one or two 5¼-in. floppies is available. MS-DOS and New Word (a word processing program) are bundled with the machine. Ergonomic design, provided by Studio Red Inc, spotlights this 9-lb machine. The keyboard has 63 full-function, alphanumeric keys with icons on the keyboard to prompt user choices. **Morrow Designs, Inc**, 600 McCormick St, San Leandro, CA 94577. **Circle 363**

System with XT compatibility supports multiple users

Mega PC handles up to eight IBM PC/XT- and PB400-compatible machines. A central unit houses a main file server board, which incorporates an 8088 processor and 256 Kbytes of RAM. This unit does all system housekeeping and overhead. Other server features include hard disk controller, 10-, 20- or 40-Mbyte Winchester disk drive, and 16-Kbyte ROM BIOS. A board containing 11 bus-expansion slots can be used for 8088-2-based application processor cards (APCs) that work while the server manages peripheral I/O. Each APC has a 256-Kbyte RAM (expandable to 512 Kbytes). Standalone and multi-user modes are supported. A two-user Mega PC with a 10-Mbyte hard disk costs $7805. Additional workstations, including the APC, are priced at $1495. **Corona Data Systems, Inc**, 275 E Hillcrest Dr, Thousand Oaks, CA 91360. **Circle 364**

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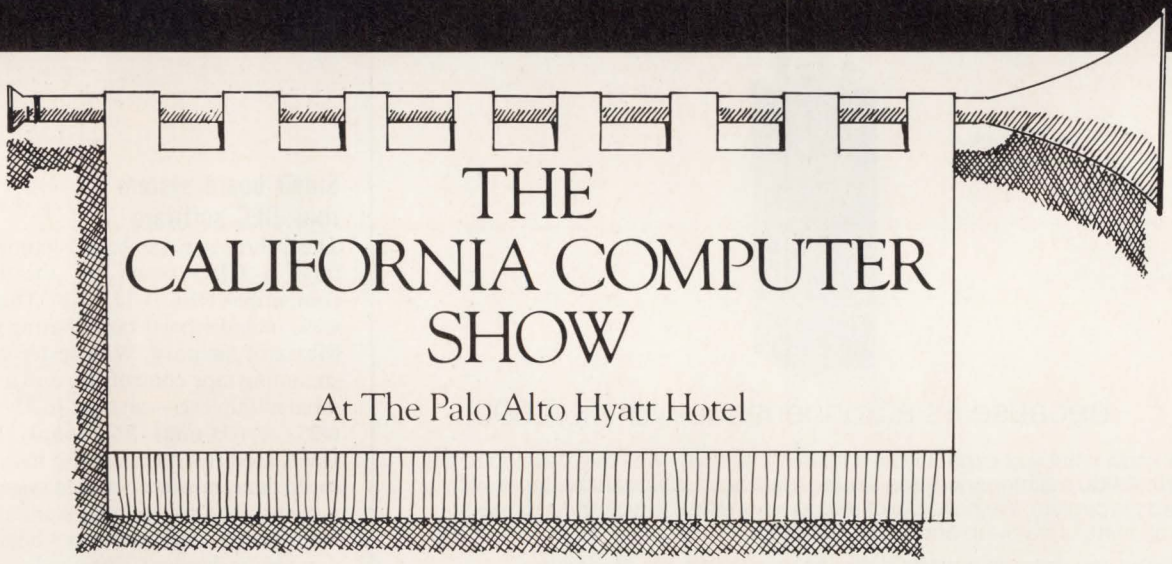

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CIRCLE 120

System supports 24 users and has an iAPX 286 heart

Athena workstations sport a dual-processor architecture combining the iAPX 286 and the Z80B. Also, an iAPX 287 handles math coprocessing. The machine supports MS-DOS, CP/M, and Unix, and can support 24 users simultaneously. Athena's standard configuration includes 256 Mbytes of main memory, 21 Mbytes on Winchester disk, 640 Kbytes on floppy disk, and an intelligent 14-in. CRT editing terminal. Systems are priced at less than $9500. **Spectra Systems, Inc,** 2754 Compass Dr, Grand Junction, CO 81501. **Circle 365**

Performance in the 16-bit range combines with 8-bit bus overhead

Using interchangeable Eurocard boards to accommodate 16 users, the System 96 is based on the 2-MHz 6809 microprocessor. It matches 16-bit performance with low 8-bit bus overhead. The basic system holds 64 Kbytes of memory that expands to 1 Mbyte in 64-Kbyte or 238-Kbyte increments. Dual 5¼-in. flexible drives, along with a dual-serial port, and a Centronics port enhance operation. Languages include Basic 09 (a semicompiled, structured Basic with Pascal features), an ISO 7185.1 standard Pascal, and a C compiler. **Measurement Systems Ltd,** 7B Faraday Rd, Newbury, Berkeshire RG13 2AD England.
Circle 366

Single-board system runs DEC software

The Cobra/16 single-board computer features a CPU based on the PDP-11 compatible DEC J-11 chip. This 16-bit CPU includes hardware floating point, 1 Mbyte of memory, Winchester disk and streaming tape controllers, and a 32-port serial multiplexer—all on a 16.75- x 25-in. (425- x 635-mm) PC board. Integral DMA facilities on the board handle high speed data transfers between system components. The system runs standard DEC software and is available as a board level, desktop, rackmount, freestanding, or custom configured system. The Cobra/16 costs at under $6000 in quantity. **General Robotics Corp,** 57 N Main St, Hartford, WI 53027.
Circle 367

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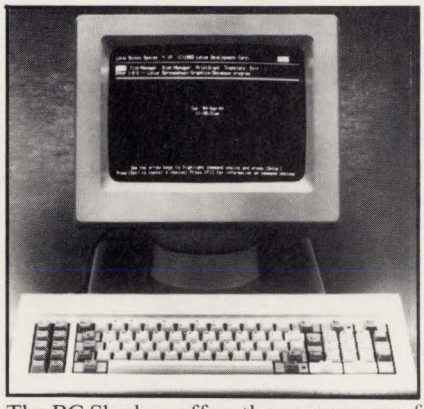
CIRCLE 123

Look-alike terminal shadows the IBM Personal Computer



The PC Shadow offers the appearance of 25-line PC operation and a similar keyboard. It supports IBM graphics characters, and screen attributes such as reverse video, highlighting, blinking, and low intensity. The PC Shadow also supports an auxiliary printer port with a transparent data path that supports X-ON/X-OFF protocols. Users can select the Televideo 925 emulation mode s an option. Price is $895. **Software Link, Inc,** 8601 Dunwoody Pl, Atlanta, GA 30338.
Circle 368

Letter-quality printer sports double-daisy wheel design

Operating at a a 50-dB noise level, the 5055 printer features a double-daisy wheel design. It uses both RS-232-C serial and Centronics parallel interfaces. Thus, the printer can link with diverse personal computers, including those from IBM, Apple, Tandy, and Wang. A 2-Kbyte buffer is available. The unit operates at a 55-char/s rate and prints in both directions with adjustable character spacing of 10, 12, or 15 chars/in., while handling paper sized up to 16-in. wide. External software controls allow the 5055 to print up to 309 international Teletex chars. The unit sells for $1995. **Amdek Corp,** 2201 Lively Blvd, Elk Grove Village, IL 60007.
Circle 369

Miniature thermal printer features 80 columns

The alphanumeric thermal EUY-8T prints on thermally sensitive paper. Characters are formed by a 7 x 5 matrix and are 2.7 mm high. The unit prints at 60 chars/s. Measuring 302.5 x 83.2 x 55.6 mm, the unit prints on 216 mm-wide paper with the expected life of 2 million lines for the printer and 500,000 lines for the head. The printers come without a case so are ready to be mounted into equipment and connect via their ribbon cables and pc connectors. It requires 12- and 5-Vdc power supplies. **Panasonic Industrial Co,** One Panasonic Way, Secaucus, NJ 07094.
Circle 370

Color printer emulates TEK 4695 for single-stroke screen formatting

An emulation package adapts the ACT II ink-jet color printer to Tektronix 4695 applications. Images developed on 4105, 4107, and 4109 display terminals reproduce on this plug-compatible unit. The ACT II can create transparencies. It is a desktop unit offering a palette of 125 colors. Primary applications include CAD and CAE, geophysical mapping, plus scientific and medical imaging. **Advanced Color Technology, Inc,** 21 Alpha Rd, Chelmsford, MA 01824.
Circle 371

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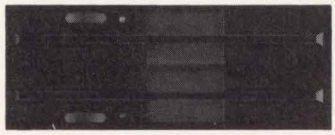
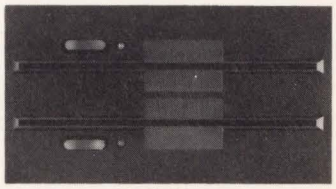


Dual drive:
Standard 2/3 height (57.5 mm) bezel



Dual drive:
Standard full height bezel

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Low cost ergonomic terminal features IBM 3178 keyboard and screen

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Portable printer runs at 60-char/s rate

A fully portable 80-col printer for use with personal computers, the Traveler uses advanced thermal technology to produce 60 chars/s. It will print 100 pages of text and graphics on its batteries, or—using its separate adapter/recharger—it can be plugged into a wall outlet. Built-in NiCad batteries recharge overnight. The Traveler measures 14½ x 7½ x 3¼ in. (368 x 190 x 82 mm). Wraparound facility allows printing text lines longer that 80 chars. The printer is priced at $199.95. **Alphacom Inc**, 2323 S Bascom Ave, Campbell, CA 95008. **Circle 373**

Silent, low cost ink-jet printer designed for character or graphics generation

The model TDP 8800 matrix printer has a bidirectional print speed of 150 chars/s. Print rate is 100 lines/min based on a 60-char line with 10 chars/in. Character fonts are built within a 9 x 9 dot matrix with provisions for descenders and underscoring. Eight-char sets can be generated including international, USASCII, English, and most European languages. A 165-char buffer, expanded print, programmable pitch, proportional spacing, and both horizontal and vertical tabs are standard. Cost is $895. **Tandberg Data, Inc**, PO Box 99, Labriola Ct, Armonk, NY 10504. **Circle 374**

Color display provides choice of switching or linear RGB video amps

Spectrum-14 represents a 14-in., 24-Vdc high resolution color display that offers a choice of switching type or linear RGB video amplifiers. The compact unit comes as a kit or chassis model. It can handle fast scan, high density applications, displaying 720 x 408 pixels. Horizontal frequency rates at 25.7 kHz (with other frequencies available), and horizontal blanking takes less than 8 μs. Vertical frequency is 60 Hz. **Wells-Gardner Electronics Corp**, 2701 N Kildare Ave, Chicago, IL 60639. **Circle 375**

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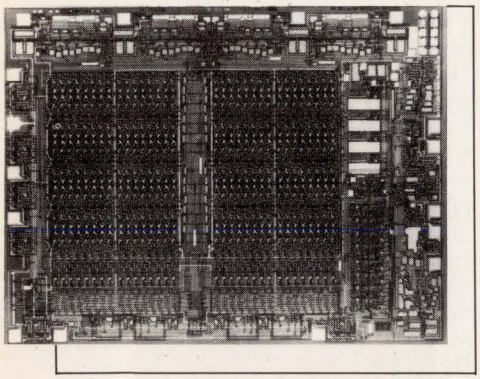
Fast data access highlights low power RAM chip



The H3500, a 256-bit, nonvolatile RAM organized as 64 x 4 bits, has a typical access time of 300 ns. Operating current measures 2 mA and standby current is 100 μA. A store operation requires just 10 ms, while a recall requires 1 μs. This is a 5-V circuit combining the data retention capabilities of an EEPROM with the high speed of a CMOS RAM. Designed for applications that need fast access times, low power, and wide temperature range, the H3500 is configured in an 18-pin DIP or leadless chip carrier. Price is $6.30 in quantities of 1000. **Hughes Solid State Products**, 500 Superior Ave, Newport Beach, CA 92658. **Circle 376**

Four single devices replaced by CMOS quad multiplying D-A converter

MP7628 features separate on chip latches for all DACs for easy micro interface, single 5-V supply voltage, and four quadrant multiplication. The device is bus-compatible with the 6800, 8080, 8085, and Z80. The 100-piece price ranges from $21 to $80.50. **Micro Power Systems, Inc,** 3100 Alred St, Santa Clara, CA 90506.
Circle 377

Mask ROM in CMOS organized as 16 Kbits x 8

A high speed 128-Kbit CMOS mask ROM features organization in the 16-Kbit x 8 realm. The SMM6313 has a worst-case access time of 250 ns. The new ROM uses a proprietary silicon gate CMOS technology to achieve high speed and low power, with typical operating current set at 16 mA (worst case, 30 mA). This device is pin-compatible with 61328 and 23128 types. It is also compatible with the 27128 EPROM, which can be used for breadboarding. The unit joins a CMOS mask ROM line that includes a 250-ns, 256-Kbit device, as well as standard 64-Kbit and 128-Kbit types. Price is $6.22 at the 10,000-piece level. Mask charge is $2800. **S-MOS Systems, Inc**, 50 W Brokaw Rd #7, San Jose, CA 95110.
Circle 378

Chip has 128 Kbits and is mask-programmable

MCM63128 is fabricated in HMOS and organized as 16-K x 8-bit. It remains fully compatible with TTL inputs and outputs while maintaining low power dissipation and wide operating margins. The device contains circuitry for current surge suppression that maintains the chip in an internal deselect mode until VCC approaches 2.5 V, at which time the chip is internall selected. Price, in 2000-piece quantities, is $6.72 with a $3000 mask charge. **Motorola, Inc, Memory Products Div**, 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 379

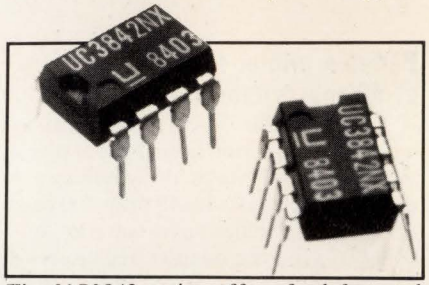
Single-chip display controller boosts video data rates

A high performance graphics display controller, the uPD7220A, can generate video rates up to 128 MHz, while performing read/write/modify (RWM) display memory cycles in 500 ns. An enhancement of the uPD7220, this chip can address up to 4 Mbits of video display memory. It has programmable vertical and horizontal timing and an internal vector generator for drawing arbitrary vectors, arc circles, rectangles, and characters. Other features include zooming, panning, scrolling, and split screen. The chip comes in 6-, 7-, and 8-MHz versions. Price is $130 each in 100s. **NEC Electronics Inc**, 401 Ellis St, PO Box 7241, Mountain View, CA 94039.
Circle 380

Eight-lead, small-outline package saves space on the PC board

The ICL7660, a voltage converter with a small-outline package, saves valuable PC board space. It performs positive-to-negative voltage supply conversion or simple positive voltage supply multiplication. Applications include data acquisition systems where a positive supply is already available for digital functions but an analog voltage supply is required. About one-third the size of a conventional mini-DIP, the device is also aimed at portable system application. Price is $2.36 each in 100-piece quantities. **Intersil Inc, a subsidiary of General Electric**, 10710 N Tantau Ave, Cupertino, CA 95014.
Circle 381

Single-chip uses current mode control for switch-mode power supplies



The UC3842 series offers feed forward line regulation, pulse-by-pulse current control, and enhanced dynamic response. the single-ended input features a totem pole drive designed to source and sink peak currents of up to 1.0 A peak from a capacitive load such as the gate of a power MOSFET. Protection circuitry on the control chip includes built-in under voltage lock out and current limiting. Other features include fully latched operation for double pulse suppression, a trimmed bandgap reference, and a low start-up current of less than 1 mA. Prices are $1.80 in quantities of 100 to 999. **Unitrode Corp**, 7 Continental Blvd, Merrimack, NH 03054. **Circle 382**

High density and low power offered in CMOS EPROM

MBM27C256 is a 256-Kbit part organized as 32 K x 8 bits. This byte-wide architecture is compatible with all micros. The higher addressability reduces chip counts. Available access times include 250 and 300 ns. With a 4-MHz clock, the device dissipates 158 mW—30 mA of active current from a single 5-V power supply. At 1 MHz, active current is 10 mA and standby current is 1 mA. It is offered in either a 28-pin DIP or a 32-pin leadless chip carrier. Each package offers JEDEC standard pinouts. In 100s, prices start at $115 for the 300 ns parts and at $130 for the 250 ns devices. **Fujitsu Microelectronics**, 3320 Scott Blvd, Santa Clara, CA 95051.
Circle 383

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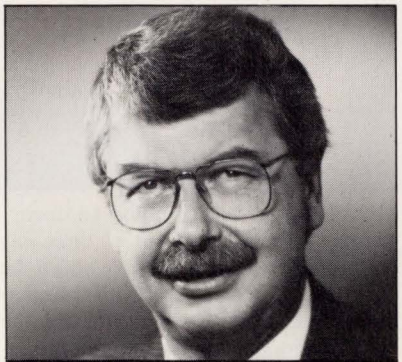

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CIRCLE 129

Power conditioners

Full-line technical catalog describes Line Tamer series power conditioners. Twelve-page item studies Z-Phase, computer, and industrial power conditioners providing power line regulation, isolation, and noise rejection. **Shape Magnetronics, Inc,** Lombard, Ill.
Circle 410

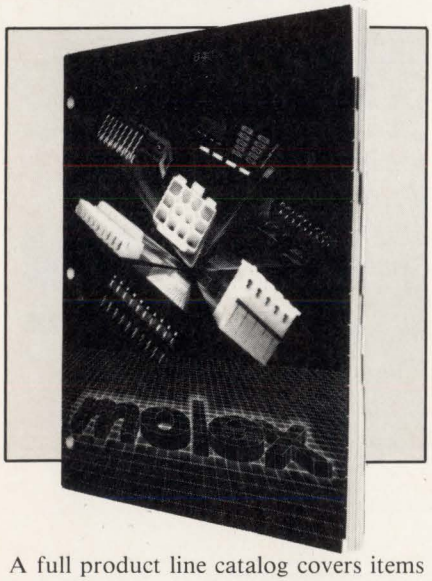
D-subminiature connectors

Catalog details full line of D-miniature rack and panel connectors. Products are shown in photos and dimensional drawings. **Amphenol Products,** Oak Brook, Ill.
Circle 411

Electronic control

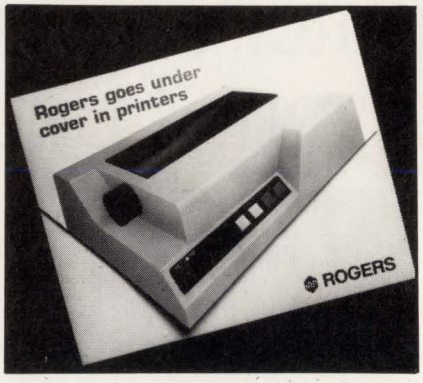
Four-page application note describes multitasking for industrial machine control. This function allows simultaneous execution of several programs on a programmable controller. **Control Technology Corp,** Westboro, Mass.
Circle 412

Full-line interconnection catalog



A full product line catalog covers items including pin and socket connectors, plastic D-subminiature connectors, solderless terminals, PC board interconnection systems, 0.050-in. centerline planar cable connectors, and modular I/O connectors. Photos, 3-D drawings, and technical data cover the spectrum of 25,000 electrical and electronic interconnection components, plus associated application equipment. **Molex Inc,** Lisle, Ill.
Circle 413

Printer parts defined



Components that combine to form a printer are described in a three-page brochure. Included are PC board bus bars, micromotion keyboards, and an interconnection system for flexible circuits. **Rogers Corp,** Rogers, Conn.
Circle 414

Programmable controller

This eight-page brochure details aspects of the Sucos PS-31 programmable controller. Technical data, schematic and block diagrams, examples of applications, and available options highlight this piece. **Klockner-Moeller Corp,** Natick, Mass.
Circle 415

Molded computer cables

Tens of thousands of connector/pinning/cable variables are represented in a molded computer cable product guide. Line includes a large selection of pinnings in standard and custom wiring configurations. **Storm Products Co,** Phoenix, Ariz.
Circle 416

Rotating memory ICs

An eight-page brochure describing rotating memory ICs includes circuits for use with ferrite head and thin-film head disk drives, as well as ICs for use in tape drive and floppy applications. **Silicon Systems Inc,** Tustin, Calif.
Circle 417

Realtime expert system

Process control goes the artificial intelligence route via the Lisp-based, PICON system. This realtime expert system, which runs on the Lambda/Plus Lisp machine, is described in a full-color brochure. **LISP Machine Inc,** Los Angeles, Calif.
Circle 418

Data communications line

This 12-page catalog details a complete line of data communications equipment including concentrators, statistical multiplexers, intelligent switching systems, modems, line drivers, protocol converters, and test equipment. **Infotron Systems Corp,** Cherry Hill, NJ.
Circle 419

Interconnection hardware

Featuring adapters, programming devices, test jacks, transistor sockets, crystal relay sockets, and socket and pin terminals, this catalog describes each by part number listings, photographs, specifications, and engineering drawings. **Augat Inc,** Attleboro, Mass.
Circle 420

Robotic machine

An adaptive assembly robotic machine is considered in a brochure that includes photographs, drawings, and block diagrams detailing system operation. This system can be used with the IBM PC. **Adaptive Intelligence Corp,** Santa Clara, Calif.
Circle 421

Intelligent 8-in. Winchester

This two-page data sheet details the MV212, which features 212-Mbyte capacity and SCSI interface. The closed-loop drive uses eight data surfaces containing 20.1 Kbytes/track and 1316 cylinders with a track density of 960 tracks/in. **MegaVault,** Woodland Hills, Calif.
Circle 422

Software for DEC hardware

Over 100 programs, including recent releases like InfoCen by 3CI and IMON from Bear Computer Systems, are described in a catalog devoted to DEC-compatible software. **Midcom Corp,** Orange, Calif.
Circle 423

Unix-based microprocessor software

Fact sheets covering Unix-based Uniware microprocessor software development tools include a system overview and details on the macro preprocessor, link editor, and cross assemblers that make up this modular tool set. **Uniware, div of Nuvatec/Inc,** Downers Grove, Ill.
Circle 424

Photo: Peter B. Kaplan

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All of the money must come from private donations; the federal government is not raising the funds. This is consistent with the Statue's origins. The French people paid for its creation themselves. And America's businesses spearheaded the public contributions that were needed for its construction and for the pedestal.

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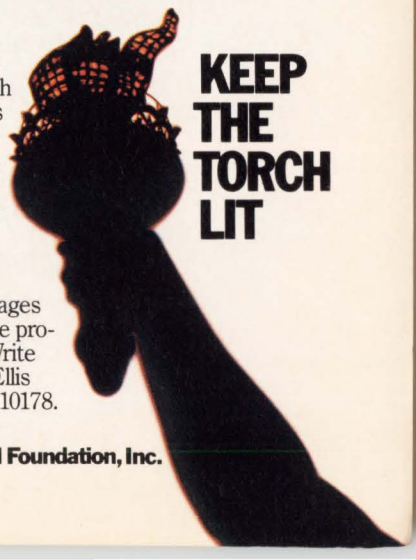

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CONFERENCES

DEC 5-7—Conf on Artificial Intelligence Applications, Sheraton Denver Tech, Denver, Colo. INFORMATION: R. Haralick, Dept of Elec Engin, VPI & SU, Blacksburg, VA 24061. Tel: 703/961-6819

DEC 5-7—Fiber Optics Communications, Washington, DC. INFORMATION: Merril A. Ferber, The George Washington Univ, School of Engin and Applied Science, Washington, DC 20052. Tel: 202/676-6106

DEC 6—California Computer Show, Hyatt Hotel, Palo Alto, Calif. INFORMATION: Norm DeNardi Enterprises, 289 S San Antonio Rd, Suite 204, Los Altos, CA 94022. Tel: 415/941-8440

DEC 6-8—Realtime Systems Symposium, Hyatt Regency Hotel, Austin, Tex. INFORMATION: Miroslaw Malek, Dept of Computer Science, Univ of Texas at Austin, Austin, TX 78712. Tel: 512/471-5704

DEC 9-12—IEEE Int'l Electron Devices Meeting, San Francisco Hilton and Towers, San Francisco, Calif. INFORMATION: Melissa M. Widerker, Courtesy Associates, Inc, 665 15th St, NW, Suite 300, Washington, DC 20005

DEC 10-11—IEEE Computer Society Computer Networking Symposium, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

DEC 10-11—Micro/Personal Computer Operating Systems, Boston, Mass. INFORMATION: Software Institute of America, Inc, 8 Windsor St, Andover, MA 01810. Tel 617/470-3880

DEC 10-14—Hands-On Programming in Ada, Washington, DC. INFORMATION: George Harrison, The George Washington Univ, School of Engin and Applied Science, Washington, DC 20052. Tel: 202/676-6106

DEC 10-14—Modern Digital Signal Processing, Washington, DC. INFORMATION: Shirley Forlenzo, The George Washington Univ, School of Engin and Applied Science, Washington, DC 20052. Tel: 202/676-6106

DEC 11-13—Fifth-Generation and Supercomputer Symposium, Rotterdam, The Netherlands. INFORMATION: Rotterdam Tourist Office, Stadhuisplein 19, 3012 AR Rotterdam. Tel: 010/14 14 00

DEC 11-14—Dexpo West, Disneyland Hotel, Anaheim, Calif. INFORMATION: Natalie Kaye, Expoconsul Int'l, Inc, 55 Princeton-Hightstown Rd, Princeton Junction, NJ 08550. Tel: 609/799-1661.

DEC 29-31—Communications Networks, Conf & Expo, Washington Conv Center, Washington, DC. INFORMATION: Communications Networks, PO Box 880, Framingham, MA 01701. Tel: 617/879-0700.

JAN 24-26—Modeling and Simulation on Microcomputers, Bahia Hotel, San Diego, Calif. INFORMATION: Ray Swartz, Berkeley Decisions/Systems Inc, 730 Park Ct, Santa Clara, CA 95050. Tel: 408/984-6397

FEB 5-7—Mini/Micro West Computer Conf and Exhibit, Anaheim Hilton Hotel, Anaheim Calif. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-1965

FEB 13-15—Int'l Solid State Circuits Conf, New York Hilton, New York, NY. INFORMATION: Lewis Winner, Almeria, Coral Gables, FL 33134. Tel: 305/446-8193/4

FEB 25-28—Compcon Spring, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

FEB 26-28—Automated Design & Engineering for Electronics, Anaheim Hilton & Towers, Anaheim, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311.

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last-minute changes.

MAR 5-7—Southcon & Mini/Micro Southeast, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Dale Litherland, Electronic Conventions, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/7772-2965.

MAR 7-8—Int'l Conf in Industrial Automation, Hong Kong. INFORMATION: Conf Secretary, Autotech Hong Kong, Hong Kong Productivity Centre, 12/F, World Commerce Centre, 11 Canton Rd, Tsimshatsui, Hong Kong. Tel: 3-7235656.

MAR 11-14—National Design Engineering Show, McCormick Place, Chicago, Ill. INFORMATION: Cahners Expo Group, PO Box 3833, Stamford, CT 06905.

MAR 31-APR 3—Softcon, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Northeast Expo, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000.

SHORT COURSES

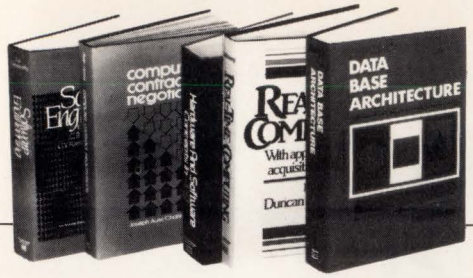
DEC—Programmable Controllers, CAD/CAM, Industrial LANs, various Massachusetts cities. INFORMATION: Kathy Shaw, Office of Continuing Education, Worcester Polytechnic Inst, Worcester, MA 01609. Tel: 617/793-5517.

DEC—Data Communications subjects, various U.S. cities and Puerto Rico. INFORMATION: The Center for Advanced Professional Education, 1820 E Garry St, Suite 110, Santa Ana, CA 92705. Tel: 714/261-0240.

DEC—Data Communications II, New York and San Francisco. INFORMATION: Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075. Tel: 609/764-0100.

DEC—Unix, Chicago, Ill; Somerset NJ; and Tampa, Fla. INFORMATION: The Center for Advanced Professional Education, 1820 E Garry St, Suite 110, Santa Ana, CA 92705. Tel: 714/261-0240.

DEC-MAR—Configuring Distributed Processing Systems, various cities. INFORMATION: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. Tel: 213/417-8888.



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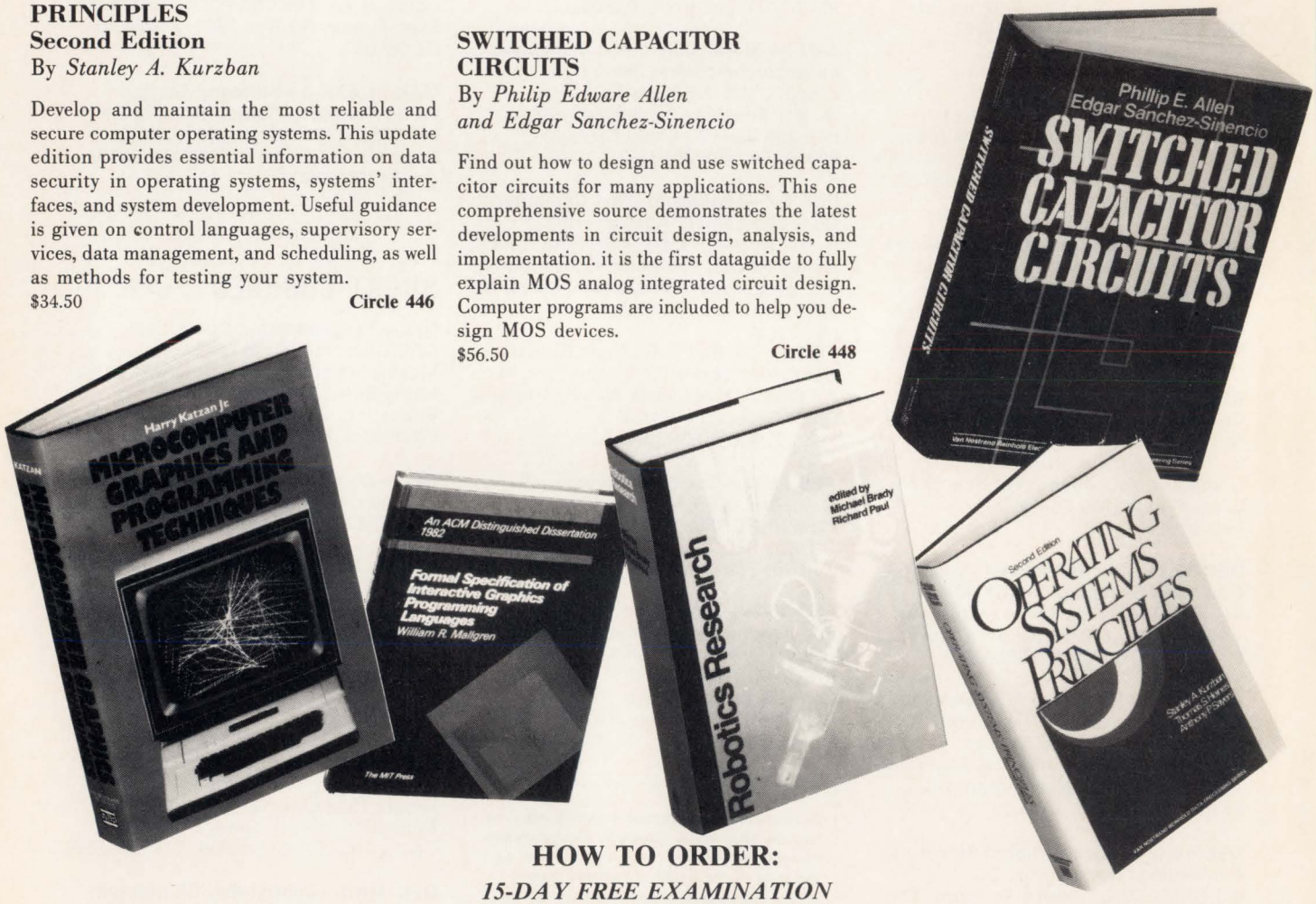

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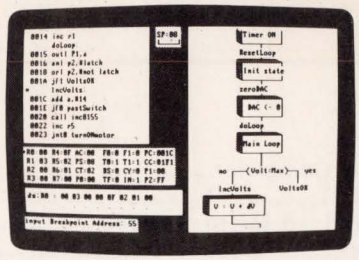

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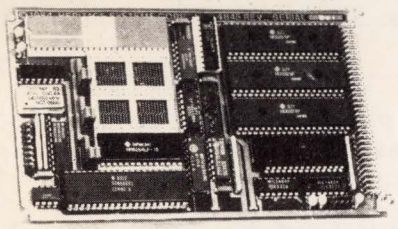

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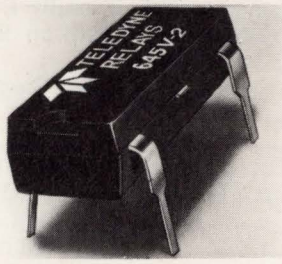

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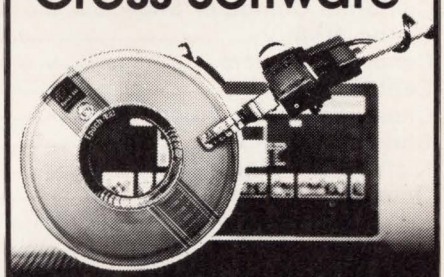

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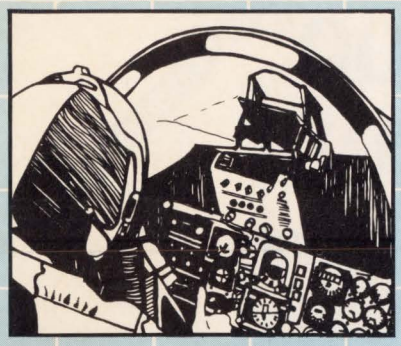

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C-Grid: the Molex .100" x .100" PCB interconnection system.

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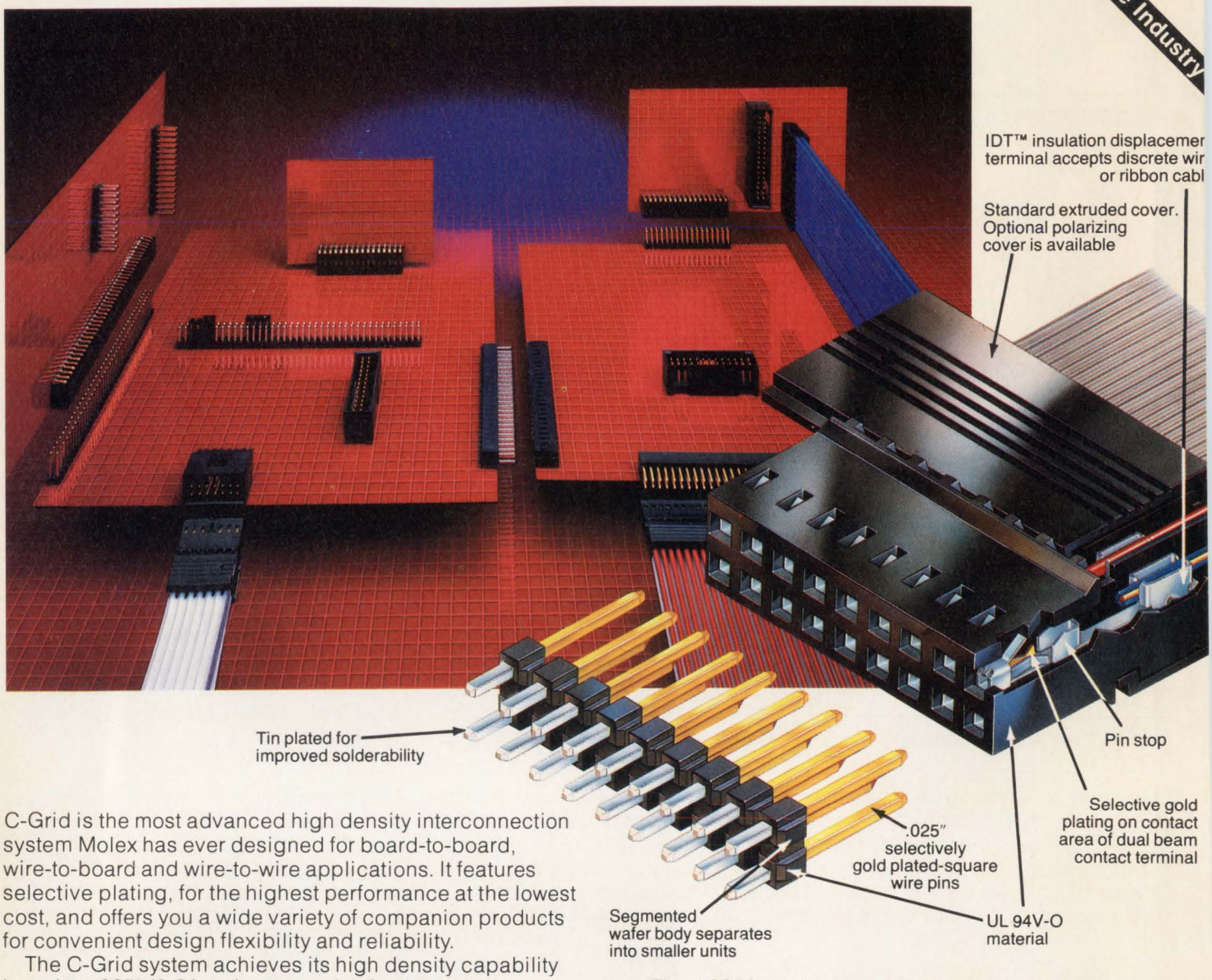

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

The C-Grid system achieves its high density capability by using .025" (0,64mm) square pins for the male connector parts, set in a .100" x .100" (2,54 x 2,54mm) matrix. The pins can either be placed directly in the board or used in volume with wafer bodies.

To load loose pins into the PC board, Molex offers a patented single- or Multi-Pinsetter® capable of up to 156,000 insertions per hour—the fastest on the market.

Shrouded and unshrouded headers are available in straight and right-angle wafer bodies.

The #8676 dual-row, insulation displacement connectors are stackable, end-to-end, and feature IDT™ terminals with mass termination application tooling available to help you achieve greater cost savings in your assembly operations.

Molex closed-or open-end shunts make it easier and less expensive to retrofit board circuitry by avoiding DIP switches.

Molex also offers a female connector (7990-series) to be soldered to one board and mated with the .025" (0,64mm) pins on another. Its features include low mating force, ease of insertion and improved solderability.

For more information on our C-Grid interconnection system, contact the Molex office nearest you.

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Corporate Headquarters: 2222 Wellington Court, Lisle, Illinois 60532 Phone: (312) 969-4550 Telex: 27-0072/25-4069
European Headquarters: Molex House, Church Lane East, Aldershot, Hants, England GU11 3ST Phone: (0252) 318221 Telex: 851858988
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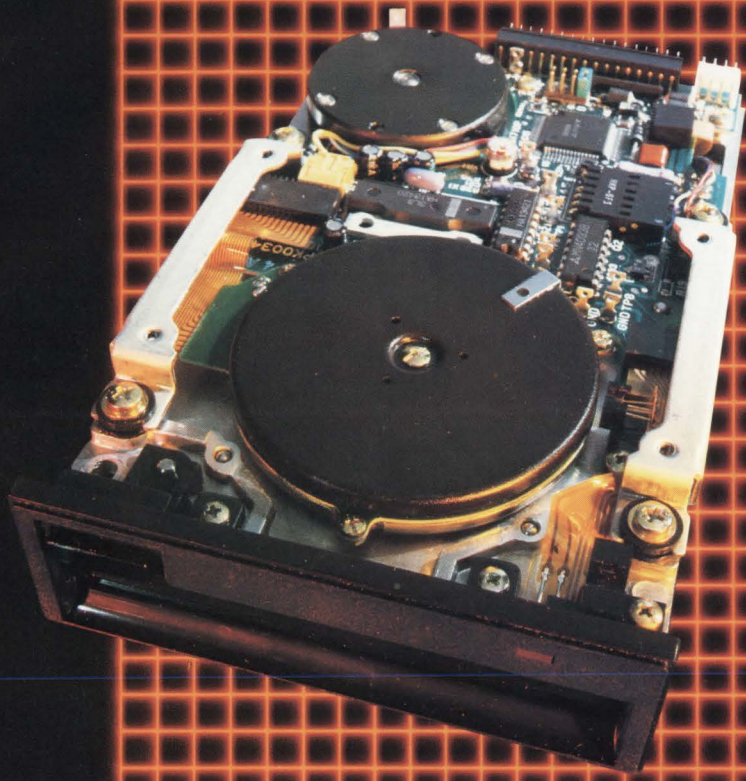
Panasonic 3½" Floppy Disk Drives



3½" disk drives are fast becoming an industry standard. And ours are built for quality performance, with features like:

- Low power, low profile
- Storage capacity up to one megabyte
- 5¼" interface compatability
- Steel band driving mechanism
- Uses standard 3½" hard-jacketed media

Our specifications meet our own high standards as well. For example:

Pwr Cons. (Stdby)	40mW (max.)
Pwr Cons. (Seek)	3.0W (typ)
Capacity	up to 1 MB
Access Time	as low as 3ms
Track Density	up to 135 T.P.I.
Dimensions (HxWxD)	32x101.6x150mm

3½" floppy disk drives. They are becoming an industry standard. But ours meet our standards first.

For more information, call or write: Panasonic Industrial Company, Computer Components Division, P.O. Box 1503, Secaucus, NJ 07094. (201) 348-8044.

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Performance in over-drive

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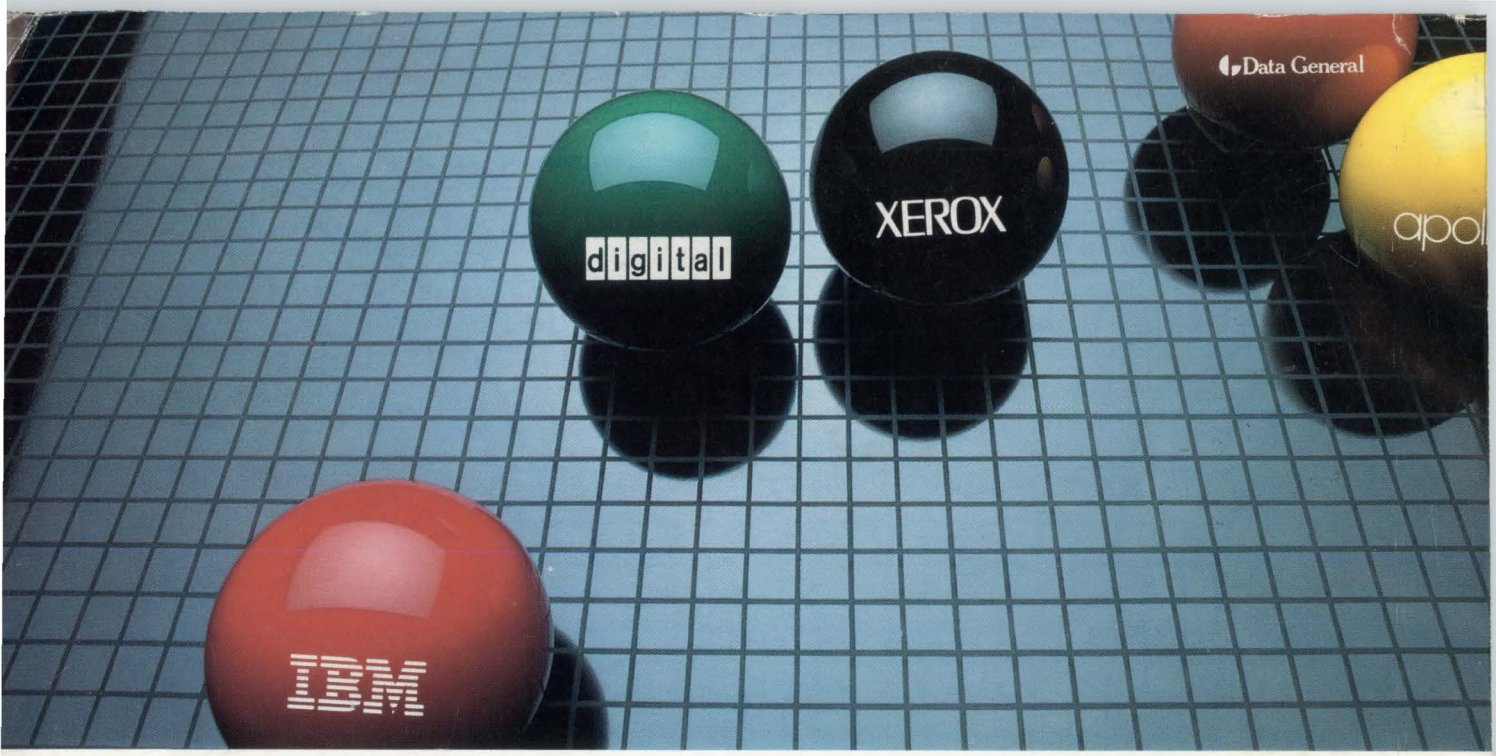

ACCES unifies the Ethernet Game with the most comprehensive network software in the field.

Now you can access information or applications across a network of different computers from different manufacturers. You no longer have to learn commands particular to specific hardware or operating systems. That's the idea behind the ACCES Network Products from ACC.

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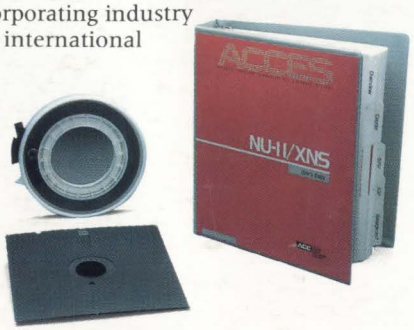
Easily Integrated. OEMs looking for layered protocols and end users incorporating industry and international standards can easily integrate ACCES Network software and supporting hardware in a very straightforward manner — saving development time and operational dollars.



Designed for Multi-Vendor Networks. From inception, the ACCES Network Products were designed for multi-vendor and multi-operating system networks based on industry and international standards. ACCES products don't rely on the operating system to provide protocol services. Protocols and operating systems are separated from each other to increase portability and to anticipate protocol evolution.

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- Proven operation on Digital's VMS, IBM's VM & MVS, Data General's AOS, Charles River's UNOS, Apollo's Domain, and UNIX operating systems.

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