A PENNWELL PUBLICATION NOVEMBER 1992

COMPUTER DESIGN

Technology and Design Directions

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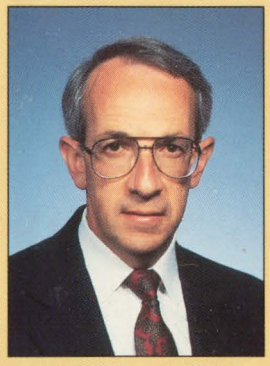
FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



AT&T's Dan DiLeo on:
3-volt mixed-signal ASICs

Design and test engineers alter roles to facilitate test

IC vendors integrate PC telecommunication services

Mezzanine buses gain respect, find new uses

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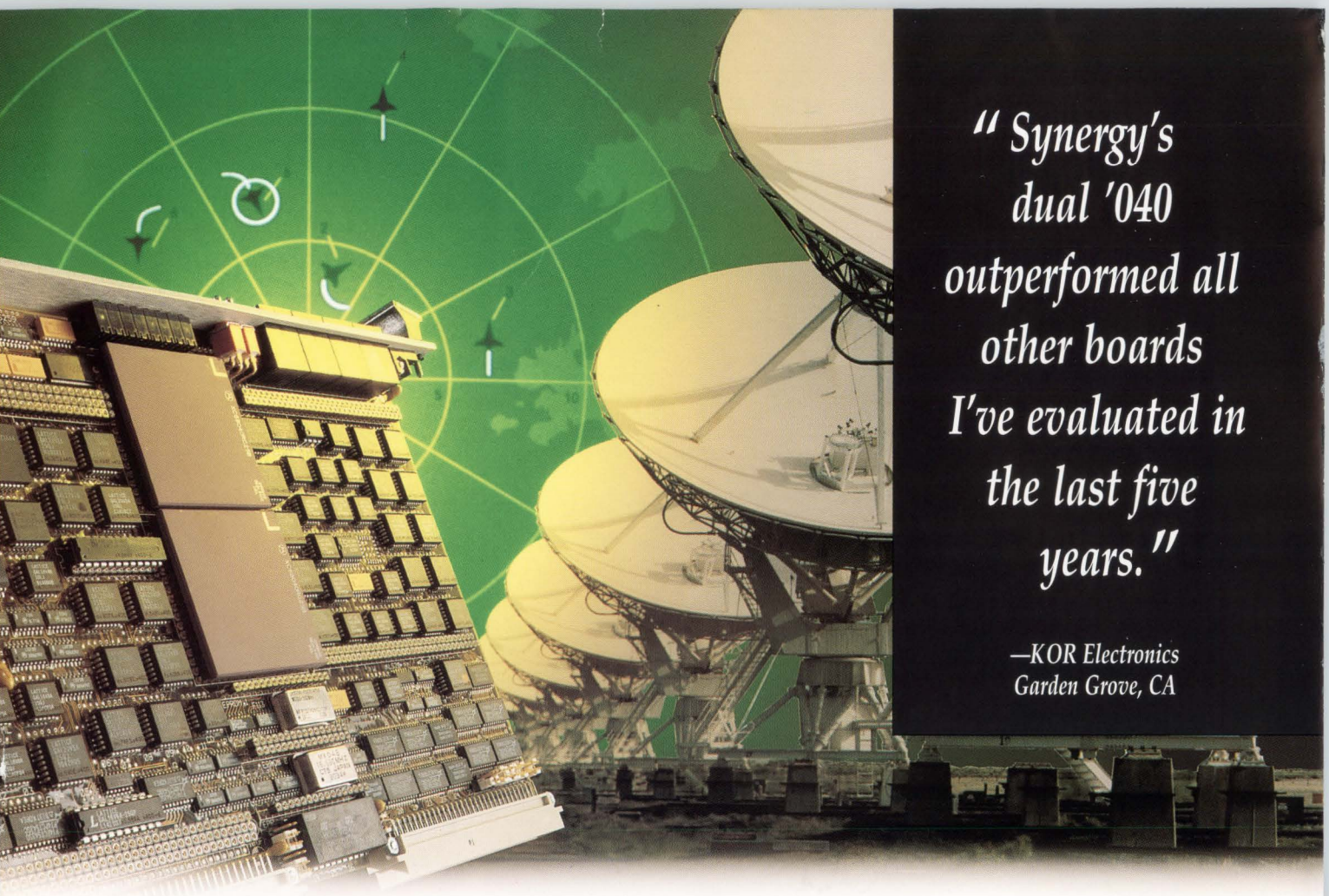
With This Issue:

OEM INTEGRATION Supplement



" Synergy's dual '040 outperformed all other boards I've evaluated in the last five years."

—KOR Electronics Garden Grove, CA

You'll find Synergy products built into the world's most demanding applications.

The Goal:

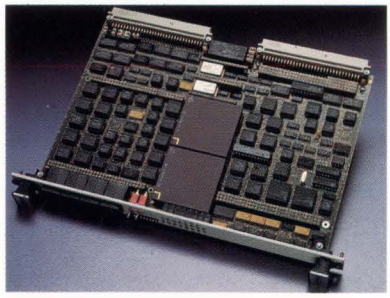
Design the world's only multi-frequency Radar Target Generator System able to simulate hostile threats on the military's diverse radar systems.

The Problem:

To get the needed horsepower, sixteen 68040 CPU boards were required. However, with this many boards, VMEbus bandwidth limits would severely degrade system performance making the project unfeasible.

The Solution:

Synergy's V420 dual 68040 SBC. After evaluating several products, KOR Electronics selected eight V420s which could deliver 320 MIPS without VMEbus bandwidth degradation.



"Not only did we meet our project performance goals, we were able to reduce our costs by 40%."

Unexpected Benefits:

Synergy's dual '040 solution cut KOR's hardware requirements by 50% while vastly increasing system reliability. These unexpected benefits reduced system costs by 40%.

In Synergy, KOR also found a design partner with strong integration expertise and dependable customer support.

"I recommend you call Synergy today."

Next time you need high performance SBCs, do as KOR Electronics did. Call Synergy Microsystems. You'll be as satisfied as they are.

SYNERGY microsystems

High performance SBCs for demanding applications.

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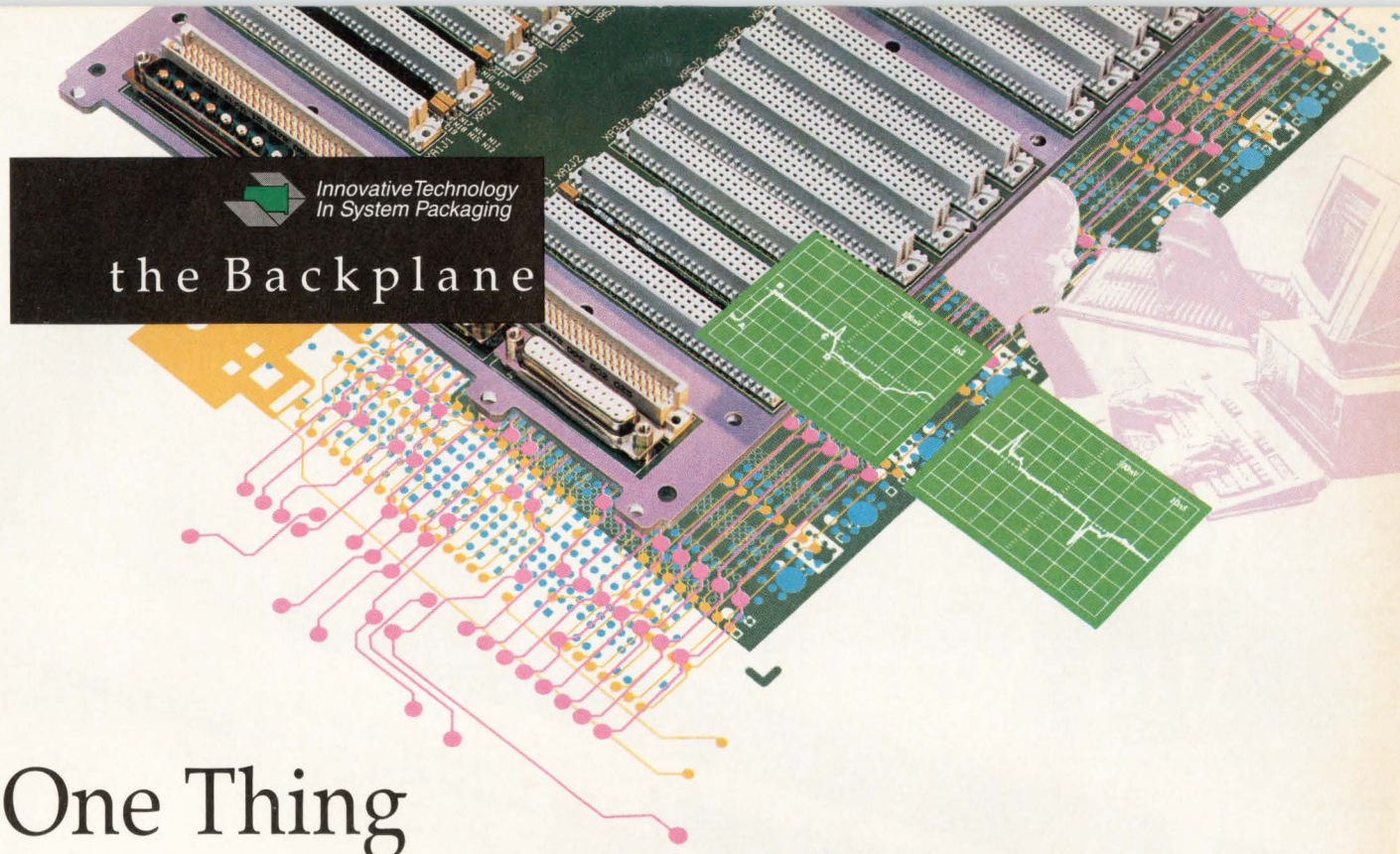

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It's the innovative application of cutting-edge technology to your specific requirements. It's what we do at Electronic Solutions.

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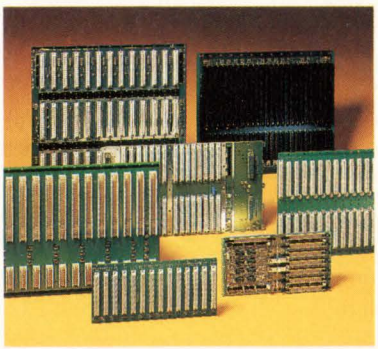
For industry standard backplanes such as VME, Multibus I or II, Sun, VXI, or Futurebus+ we have a line of high performance backplanes available off the shelf. Our backplanes have been independently tested and ranked as the "Best Balanced" backplanes available.



VMEbus
VXI bus
Sun bus
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Futurebus+
Mixed buses
Proprietary buses

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For standard or proprietary applications, there's only one way to get a backplane that's just right for your system. That's to call Electronic Solutions and put our experience to work for you.

One example of our design innovation is our patented **Active Automatic Daisy Chaining** which eliminates the number one field service probem— improperly placed Bus Grant Jumpers. It's superior to the passive auto-daisy chaining touted by other vendors, and it's available *free of charge* on our new VME backplanes.

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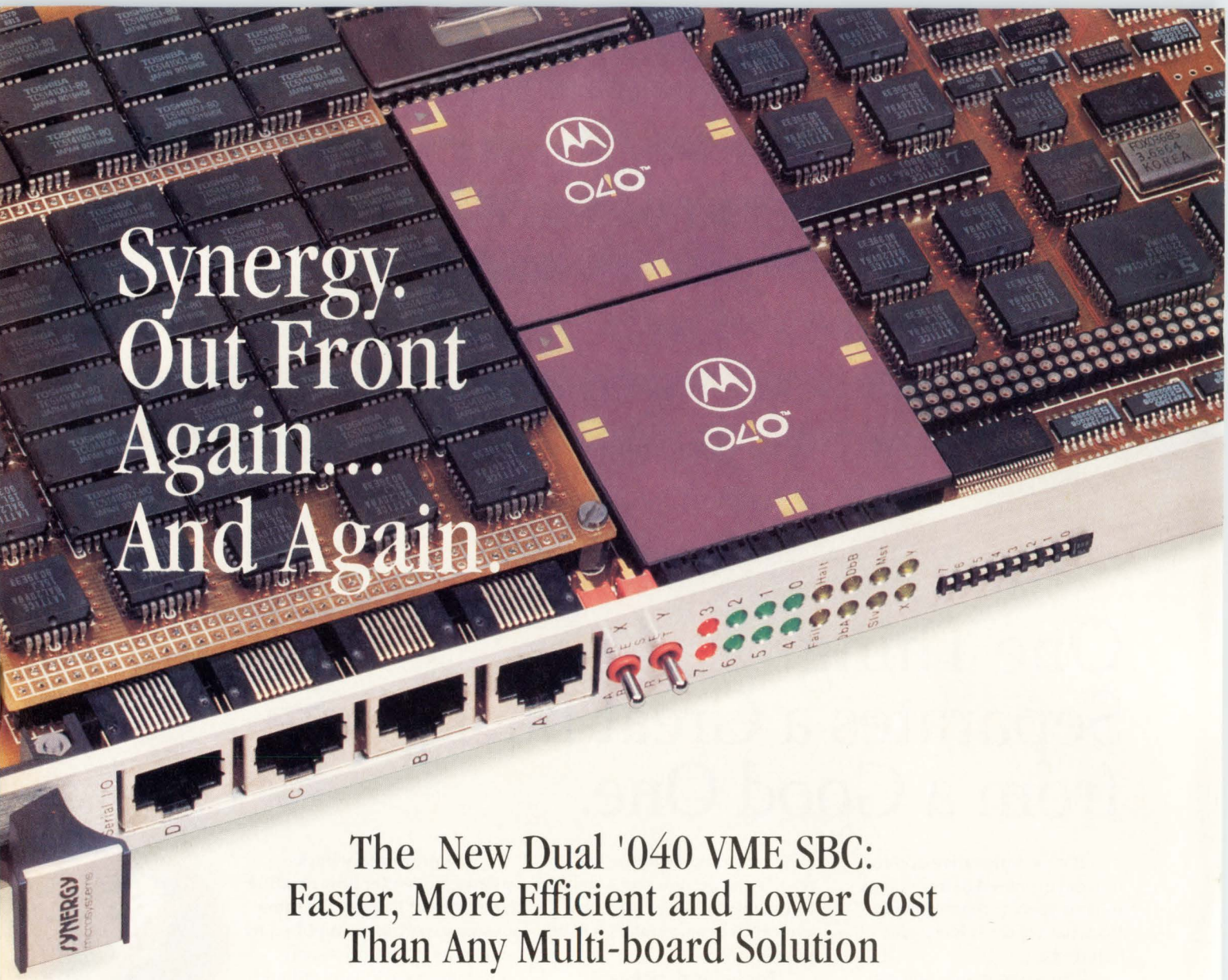


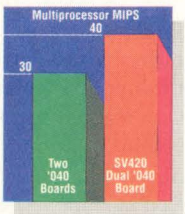
Synergy. Out Front Again... And Again.

The New Dual '040 VME SBC: Faster, More Efficient and Lower Cost Than Any Multi-board Solution

Get on-board multiprocessing and an astounding **40 MIPS** throughput, when you power your system with Synergy's new SV420 single-slot SBC. The SV420's dual-CPU design means you'll need fewer boards in your VME chassis, with no VMEbus bandwidth bottlenecks between the '040s, and system-wide cost saving of more than 40%.

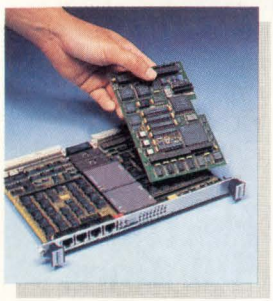
And even if you don't need multiprocessing right now, the SV420 still puts you out front. Use the second '040 as a super-smart DMA controller. When combined with the SV420's **66 MByte/sec** VME64® circuitry, nothing communicates faster over the VMEbus.

Add even more on-board power by selecting from Synergy's big list of high-performance, intelligent plug-on I/O modules – such as our latest Super-VSB module offering 40+ MB/sec over the VSB bus. Or choose another module, from a T1/E1 controller to a super-fast graphics engine, that plugs onto any Synergy SBC.



Better yet, just tell us what you need. We're the company you can talk to about your VME system design problems. You'll find that we listen *and deliver* (every Synergy I/O module on our list started as a customer request). We mean business when we say customer support is our most important mission.

So if you want to be out front in system performance, just be up front with Synergy. Call us today.



Over a dozen smart, powerful I/O modules fit Synergy's '020, '030, '040 and Dual '040 SBC's.

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CIRCLE NO. 3

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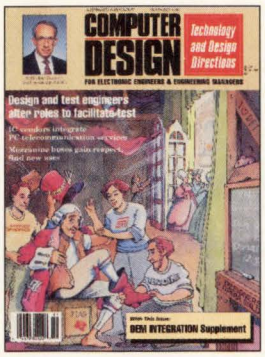
COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



Designers are assuming new roles to facilitate test just as Mozart's young rogues changed roles to test the steadfastness of their "true" loves **85**

Illustration by Bill Morrison

WITH THIS ISSUE

Computer Design's new OEM Integration supplement debuts this month and is being mailed with this issue. If someone has walked off with it, call (508) 392-2124 for another copy.

NEWS BRIEFS

TECHNOLOGY DIRECTIONS

CAE/CAD Tools

Computers & Subsystems

Software & Development Tools

Integrated Circuits

ASICs & ASIC Design Tools

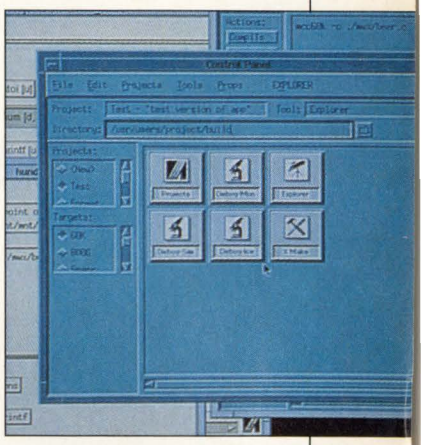
NEW PRODUCT DEVELOPMENTS

Software & Development Tools

CAE/CAD Design Tools

Integrated Circuits

ASICs & ASIC Design Tools



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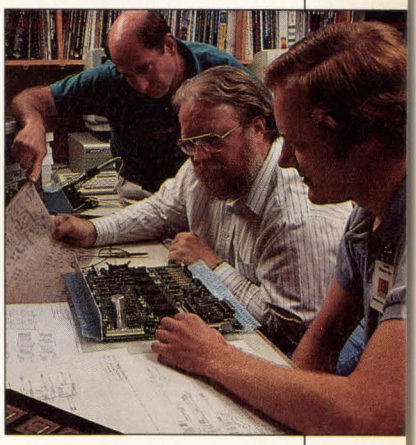

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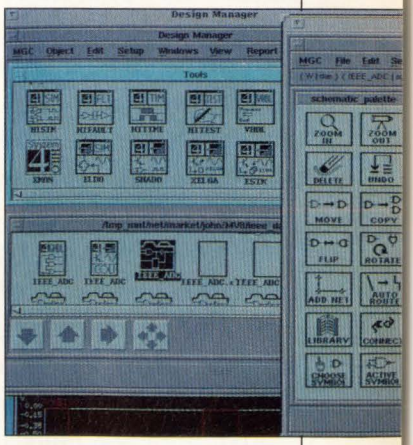

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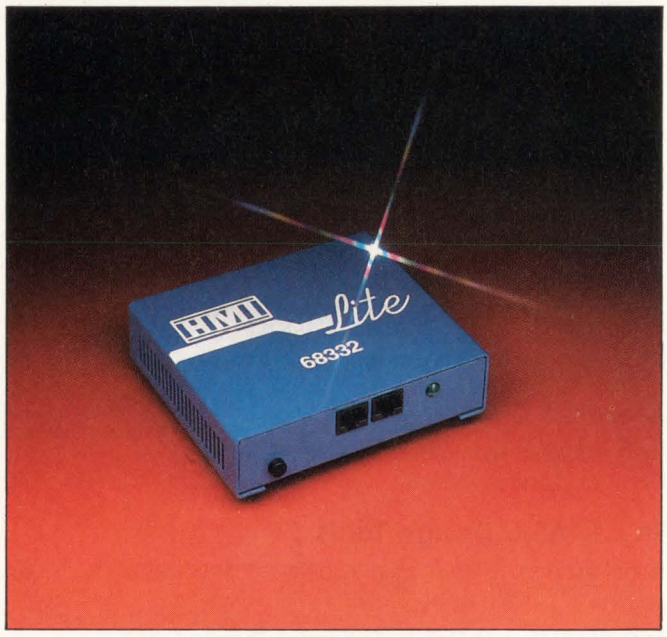
Introducing HMI Lite, the brilliant breakthrough in high-performance, highly affordable development tools.



Our new Lite quietly begins a whole new era in emulation and debugging tools. Because at under $5,000, the Lite delivers more capabilities than you ever imagined possible in its price range.

First, the price includes a complete, full-featured, real-time emulator integrated with HMI's popular SourceGate emulator control and debugging software.

Now, check these features; multiple hardware and software breakpoints, full trace capability including show cycles and dequeuing of prefetched pipelined instructions, and support for all Port-E configurations.

And, the 256K emulator RAM features complete mapping control

including all chip select signals and dynamic bus sizing for 8/16 bit operations. In addition, dual ported RAM is provided for real-time monitoring of critical memory variables.

Oh yes, and this is all packaged in a single 4.5 x 1.5 inch direct-plug pod enclosure.

Write or call for details on the Lite, it supports all industry C, PASCAL and Ada compilers and is ready for use with IBM PC family and UNIX based host computers. The new Lite is the best of our emulation technology—for less. Brilliant!

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COMPUTER DESIGN Technology and Design Directions

CONTINUED FROM PAGE 3

Dan DiLeo on: 3-volt mixed-signal ASICs

As the demand for advanced low-power portable systems—cellular telephone and laptop, palm-size and pen-based computers—increases, the electronics and computer industries are shifting to lower-voltage ICs and ASICs. **17**

COMING NEXT MONTH

32-bit processors in embedded applications

Evaluating PLD design tools

Graphical user interfaces

EISA CPU boards

Automotive systems

TECHNOLOGY & DESIGN REPORTS

IC vendors integrate PC telecommunication services

First came fax-modem combo chips. Now IC manufacturers are attempting to integrate voice messaging and caller ID. They're thinking about color fax and video conferencing. Are there limits beyond which the technology envelope can't be stretched? — *Stephan Ohr* **65**

Mezzanine buses gain respect, find new uses

High-density chips and chip sets are bringing more and more functionality to a single board, often reducing system bus requirements. This opens the way for mezzanine boards, not only to increase available board real estate, but to become an integral part of the system architecture—in some cases to the exclusion of system buses. — *Warren Andrews* **75**

COVER STORY

Design and test engineers alter roles to facilitate test

Time is running out for silicon, circuit board and system houses who haven't taken design-for-test seriously. Old test methods are fast becoming inadequate, while the next generation of systems is waiting in the wings. — *Mike Donlin* . **85**

DESIGN STRATEGIES

Event-driven strategy wins for robot test handler

Engineers at Taltec, working with a customer to develop a robotic pick-and-place machine, saw an opportunity to craft their own system platform, and ended up in the tester/handler business.— *Jeffrey Child* **100**

PRODUCT FOCUS

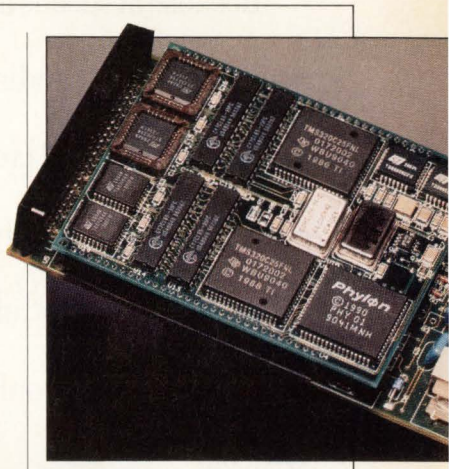
Trace issues drive 32-bit emulator choice

For integrating hardware with software, as well as hunting down the nastiest bugs in your real-time microprocessor-based design, there's no more effective tool than an emulator. — *Jeffrey Child* **107**

COLUMN

MIXED-SIGNAL DESIGN — *Stephan Ohr*

Are automobiles the proving ground for the next generation of electronics? **120**



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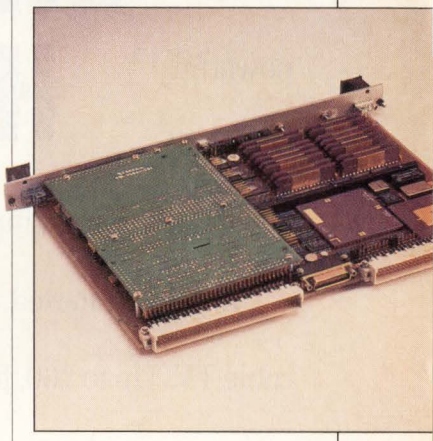

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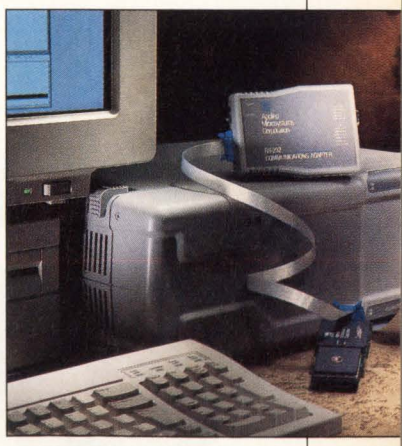

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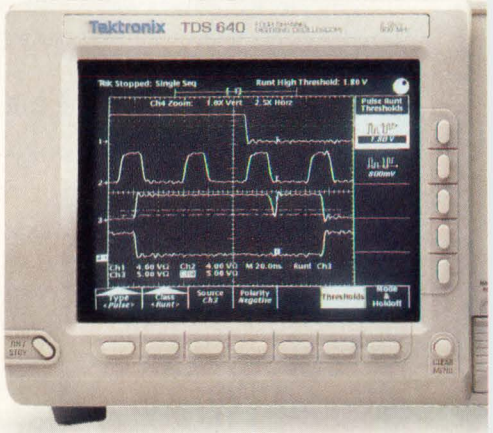
No logic analyzer is, for that matter.

Because at speeds above 25 MHz, even the best designer needs a scope to handle nightmares like race conditions, ground bounce, and crosstalk. And not just any scope, but one tailored specifically for high-speed digital design.

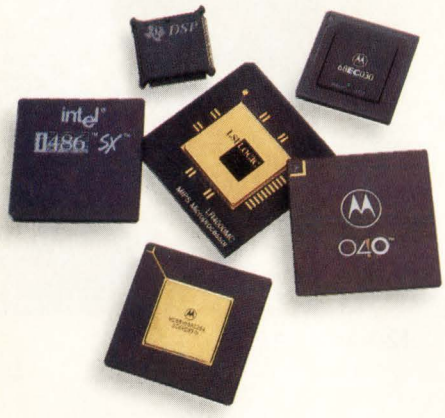
At Tektronix, we understand this need all too well. As proof, we've not only designed and built a great logic analyzer — our powerful new GPX — but also a perfect companion. The TDS 640 digitizing oscilloscope.

EVEN THOUGH OUR NEW LOGIC HIGH SPEED DIGITAL DESIGN,



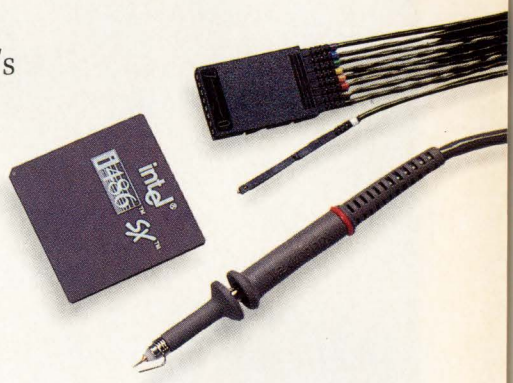
To get you started, the GPX provides more channels than cable TV. Up to 160, for instance, of 80 MHz state analysis, and 32 channels of 1 GHz timing or 160 channels of 200 MHz transitional timing.

In short, enough to handle the world's fastest microprocessors. And with that kind of performance, you can easily track your system at clock rates well beyond 50 MHz, which allows you to locate complex coding errors quickly and accurately.

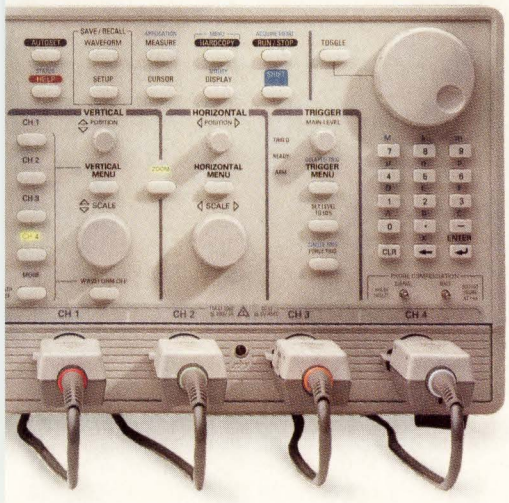


Enter the TDS 640.

With a 500 MHz bandwidth and 2 GS/s real-time sampling on four channels, the TDS displays logic and timing errors with absolute accuracy. And because it was created with the digital designer in mind, the TDS lets you trigger directly on common digital circuit events like glitches, runt pulses, and excessive clock jitter or skew. Put all that together with the power of the GPX and you have a remarkably effective solution.



ANALYZER IS GREAT FOR IT'S NOT NEARLY ENOUGH.



Cost effective, too. In fact, the GPX and TDS together sell for less than competing scope/logic analyzer combinations. And if you buy the pair between now and February 28, 1993, we'll take an additional 10% off the retail price.

Enough, already.

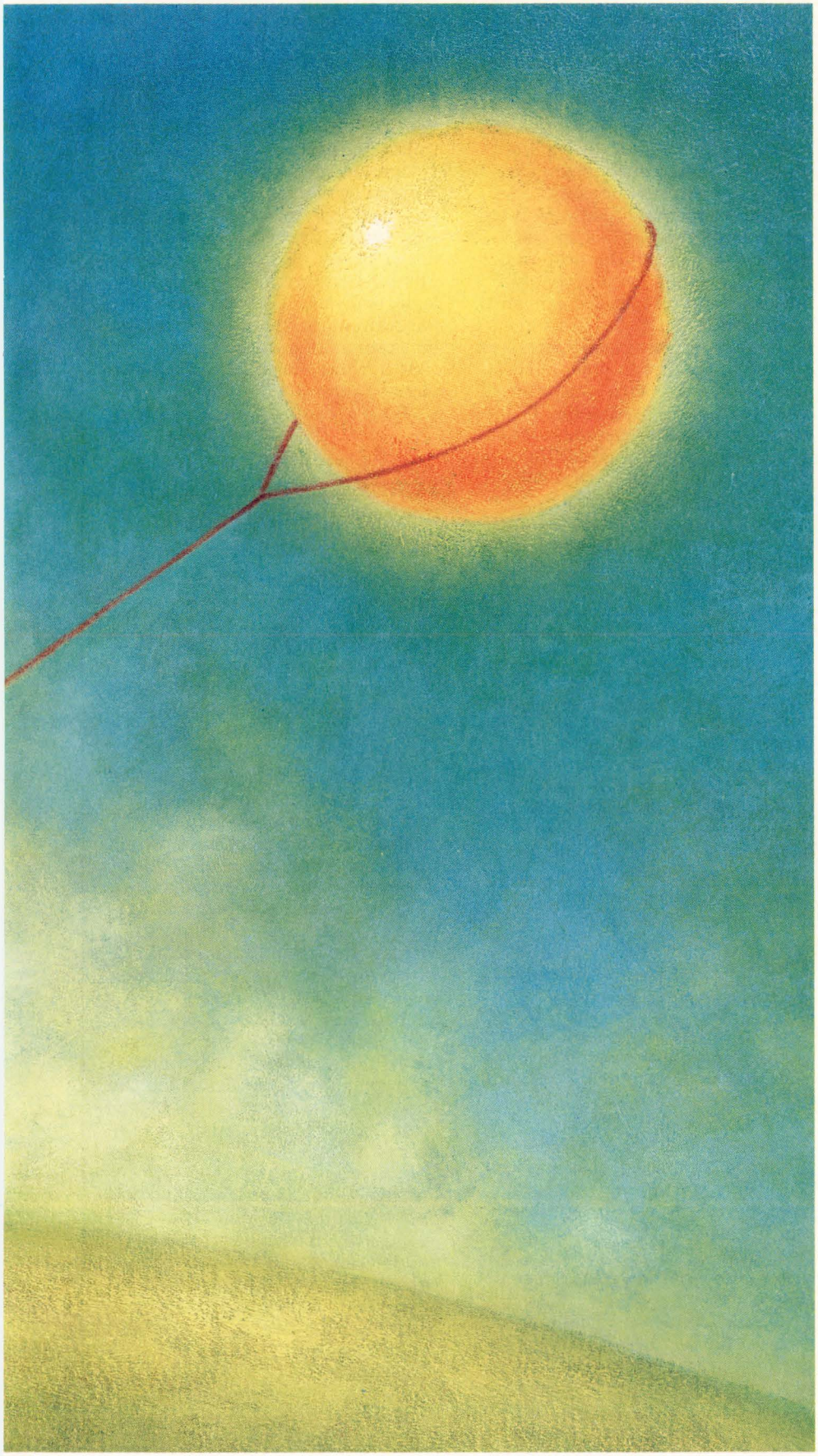
For more information on the very best high-speed digital design tools available, call Tektronix today at 800-426-2200.

Tektronix
Test and Measurement

CIRCLE NO. 5

This is your chance to get the full power of embedded

SPARC. Don't let it slip away.



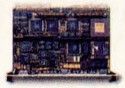
This is one of those times when you just have to seize the day. Because opportunities like this are rare indeed.

Choose from a range of systems, for a highly integrated solution.

You see, FORCE is the only company licensed by Sun to put SPARC™station 2 technology on VME.

So we're the only ones who can give you validated hardware and software compatibility. Allowing you to run SunOS™ with any of your SPARCstation 2 applications and peripherals. Without a hitch.

We also have a whole new family of SPARC 2 products. With everything from our CPU-2CE (6U) board to the *microforce* single-slot system.



Our CPU-2CE features a 40MHz SPARC RISC microprocessor, delivering 28.5 MIPS.

We even have 20-slot systems that allow you to customize I/O. Giving you the perfect combination of real-time and UNIX.

And our SPARC products provide the broadest software offering of any RISC architecture. Including SunOS, real-time operating systems and a host of application software.

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Because there's no reason to let all this power slip through your fingers.

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CIRCLE NO. 6

HP joins open-standards revolution

Last month Hewlett-Packard (Fort Collins, CO) jumped into the real-time, open-bus business with a vengeance when it introduced the 742m. This full-featured CPU carries HP's 50-MHz PA-RISC 7100 processor with floating-point coprocessor. The new board is designed to run the HP-RT 1.0 real-time POSIX-based operating system, and is closing in on 60 SPECmarks.

The board, however, is but one of HP's forays into the open-systems, real-time arena. It's also introducing an entire family of industrial workstations based on VMEbus. The family will be part of the HP Apollo 9000 Series 700 workstations, targeted at the manufacturing, aerospace, telecommunications, and medical and laboratory industries.

The new products are designed to let OEMs, system integrators and users increase performance with HP's PA-RISC architecture and software development tools. Board products are compatible with the company's other workstations.

In making its announcement, HP becomes the second major maker of minicomputers to jump on the VMEbus bandwagon for real-time applications. Last year, Digital Equipment Corporation (Maynard, MA) announced that it would focus on the real-time market, using VMEbus with its Alpha processor architecture. At the time, it announced an agreement with Wind River Systems (Alameda, CA), in which that company would port its VxWorks to Digital's new family of products and integrate Alpha into its existing real-time OS.

Both HP and Digital have traditionally had heavy stakes in the real-time business—HP with its 1000-series minicomputers and Digital with its PDP machines. Both, however, were in jeopardy of losing out to more flexible, standard-bus-based machines. Despite rumors to the contrary, Digital's project leader, Maureen Johnson, reports that the company's VMEbus-based project is on schedule.

—Warren Andrews

Antsy for ANSI

VITA (VME International Trade Association—Scottsdale, AZ) has submitted an application to ANSI to become a standards sponsoring group. The group's objective is to provide a more comprehensive vehicle for the VMEbus specification.

VITA's application is currently going through the approval process at ANSI, a process that's expected to be completed early next year. It's expected that once VITA achieves sponsorship status, it will write a revised VMEbus specification divorced from the present 1014 Revision C, and probably also from the proposed Revision D, which adds VME64 to Revision C.

A new VMEbus specification is expected to emerge in place of these documents, one with SSBLT and all the new timing parameters it mandates. It will also include most of the features discussed for Revision D but not included in that document. In addition, it may include similar features for both 3U and 6U, as well as multiplexed P1 signal lines to give 3U VME 32-bit SSBLT performance.

VITA's ANSI application has a few people in the IEEE upset. "Most of the rock throwing is over now," says Ray Alderman, VITA's technical director. "It's now down to a few substantive issues, which we hope will be resolved soon." But it's an open question as to whether or not VITA's move will result in an exodus of standards from the IEEE. At this time, VITA, which represents both Futurebus+ and VME, isn't planning to move the Futurebus+ specification to ANSI.

—Warren Andrews

Compass selling libraries for foundry, tools

Just weeks ago, Compass Design Automation (San Jose, CA) announced the commercial availability of general-purpose physical layout libraries and compilers for CMOS ASICs and ICs. After Compass library customers choose a silicon foundry, the company will target its Liberty Series of physical layout libraries to the specific process technology, recharacterizing the library elements to get accurate timing models.

"Traditionally, physical layout libraries haven't become available for new process technologies until well after the processes are production-worthy," says Harriet Harvey-Horn, product marketing manager for libraries and process technologies at Compass. "The Liberty Series provides chip manufacturers and designers with a ready-made library solution that can be easily tailored to a particular foundry's design rules in a fraction of the time required by conventional development methods."

Library users can work in Compass' ASIC Navigator top-down design system or with tools from Cadence Design Systems, GenRad, Mentor Graphics, Synopsys, Viewlogic, or Zycad. Dan Skilken, Compass' director of worldwide product marketing, says, "It's the first time a library product includes services to generate simulation models for all leading simulators."

—Barbara Tuck

Mentor Graphics opens six top-down design centers

To reduce the risk to users of transitioning from gate-level to top-down design, Mentor Graphics (Wilsonville, OR) has just opened half a dozen design centers, staffed with its own senior ASIC designers and equipped with Sun SPARC workstations. The centers are located in Boston, Dallas, Denver, Munich, San Jose, and Tokyo. Later this month Mentor will begin a worldwide training program called SmartStart, which covers software, hardware, silicon fabrication, and support services.

To make vendor support available to SmartStart participants, Mentor has initially teamed up with Sun Microsystems and ASIC vendors Fujitsu, LSI Logic, Mitsubishi, and VLSI Technology, as well as FPGA vendor Xilinx. "Mentor Graphics wants to partner with companies that are doing the most difficult, leading-edge ASIC designs," says Dan Ganousis, manager of Mentor's ASIC Design Center program.

Training for SmartStart participants will include seminars, workshops, VHDL language training, and on-site consulting services. During the training, customers will actively participate in taking a design from VHDL to layout through actual hands-on experience.

—Barbara Tuck

Continued on page 12

Twice the Logic in Half the Space

DOUBLE-DENSITY™ FROM IDT

46% BOARD SAVINGS

IDT's new 16-, 18-, and 20-bit Double-Density FCT-T Logic family offers the performance of two octal logic devices in one flow-through 48- or 56-pin high-density, JEDEC-standard, shrink small outline package (SSOP) or Cerpack, for twice the functionality in half the board space.

A WIDEBUS™ UPGRADE

IDT's Double-Density logic family is more than twice as fast as **ACT**, uses 35% less power than **ABT**, and it's form-, fit-, and function-compatible with both of TI's Widebus families. The Double-Density family also offers typical pin-to-pin skew of 250ps and quiescent supply current at 0.05mA (typ.).

3 APPLICATION CHOICES

5V High Output Drive
Ideal for low-impedance bus and backplane applications.

5V Balanced Drive (Low Noise)
Contains on-chip, source-terminating resistors to minimize signal noise. These devices are ideal for driving point-to-point transmission lines and highly capacitive loads, such as a bank of DRAMs or SRAMs.

3.3V Low-Power Logic
Designed for regulated or unregulated 3.3V power supplies, these devices use less power than 5V parts, without sacrificing high speed. 5V-to-3.3V unidirectional and bidirectional translators are also available.

FREE SAMPLES

Call today for free samples and a copy of the **new High-Performance Logic Data Book** and start your Double-Density logic design today!

DOUBLE-DENSITY CONFIGURATION*	I_{OH}	I_{OL}	t_{PD} (Max.)	I_{CCQ} (Typ.)	PIN-TO-PIN SKEW (Typ.)	GND BOUNCE (Typ.)
High Drive	−32 mA	+64 mA	4.1 ns	0.05 mA	250 ps	< 1.0 V
Balanced Drive	−24 mA	+24 mA	4.1 ns	0.05 mA	250 ps	< 0.6 V
3.3V	−8 mA	+24 mA	4.8 ns	0.05 mA	250 ps	< 0.3 V

*Specs are for '244 device

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CIRCLE NO. 7

Continued from page 10

Alpha fab registered for ISO 9000

Digital Equipment Corporation (Hudson, MA) has announced that its semiconductor fab there has been registered to the International Organization for Standardization (ISO) standard 9002. The Hudson site is one of two Digital facilities manufacturing the 200-MHz Alpha AXP family of RISC microprocessors, the world's fastest 64-bit chips.

The ISO-9000 series of quality assurance standards is becoming a prerequisite for conducting business in Europe and other parts of the world. In contrast to the Malcolm Baldrige Award for Quality, ISO 9000 is an ongoing certification rather than a one-time award. ISO-9000 registration requires adherence to strict guidelines and comprehensive auditing by a qualified outside agency. The accredited agency that registered the Digital facility is the Quality Management Institute. With the Hudson registration, all four of Digital's semiconductor fabs are ISO-9002 qualified. The ISO 9002 is the second-highest level of ISO-9000 qualification. Digital is among a small group of IC manufacturers that's registered for ISO 9000.

More manufacturers are expected to follow in Digital's footsteps now that companies such as AT&T, Hewlett-Packard and IBM are requiring their suppliers to move toward ISO-9000 certification.

—Jeffrey Child

Dual use the watchword as defense pares down

With military budgets feeling the pinch due to recession and relaxing world tensions, defense contractors are looking to develop products that can be used in both the military and civilian sectors. They're also more actively marketing products developed for the military into civilian applications. A case in point is Loral Defense Systems (Akron, OH), which is offering a high-speed parallel/associative computer, originally developed for use in airborne warning and control systems (AWACS), for use in VME-based workstations.

The ASPRO-VME is a single-instruction, multiple-data (SIMD) associative computer that finds data by content, not address. It can be built up in modules of 512 processors to a total of 8,192 processors, and can perform between 150 MFlops and 2.4 GFlops. The military uses the ASPRO-VME primarily for target correlation and tracking, image processing and tactical decision support. More general civilian applications include image processing, signal processing, associative database management, artificial intelligence, and neural networks. *—Tom Williams*

Pact to provide real-time UNIX for Intel computers

The Santa Cruz Operation (SCO—Santa Cruz, CA), a leading supplier of UNIX for PCs, has joined forces with Chorus Systems (Paris, France) to produce a real-time version of UNIX for Intel-based computers. The real-time aspects of the system will leverage off Chorus' microkernel technology, which it embodies in its Chorus MiX product. SCO will contribute its 386/486-based SCO UNIX and its SCO Open Desktop X-Window-based GUI.

Initial plans call for the new product to be targeted at replicated-site applications in telecommunications, point-of-sale, and process and manufacturing control, as well as testing and simulation. Given the compact size of the Chorus microkernel, the system should be easily portable to smaller, single-board embedded systems as well. SCO's alliance with Chorus could also be a counter to the threat posed by Sun Microsystems, whose Solaris version of UNIX is poised to invade the Intel-based arena now dominated by SCO. To date, Solaris does not have real-time capabilities.

—Tom Williams

MCMs still waiting in the wings

At the recent International Electronic Packaging Society Conference (Austin, TX), multichip modules (MCMs) attracted the usual group of curiosity seekers, but didn't prove they can garner design wins. Despite predictions that the fledgling technology is poised to become a dominant component of next-generation systems, many designers deem MCMs as either too expensive or too risky to become anything but fodder for technical papers. But AT&T Bell Laboratories (Murray Hill, NJ) hopes to extricate MCMs from this quagmire by incorporating them into its next generation of telephone products.

AT&T is predicting that volume could run up to 500,000 MCMs per year—a figure that may be greater than the sum total of MCMs produced this year. Although AT&T hasn't committed to volume production of MCMs as yet, the company is currently doing feasibility studies of the technology at its manufacturing plants in Kansas City, MO and Shreveport, LA.

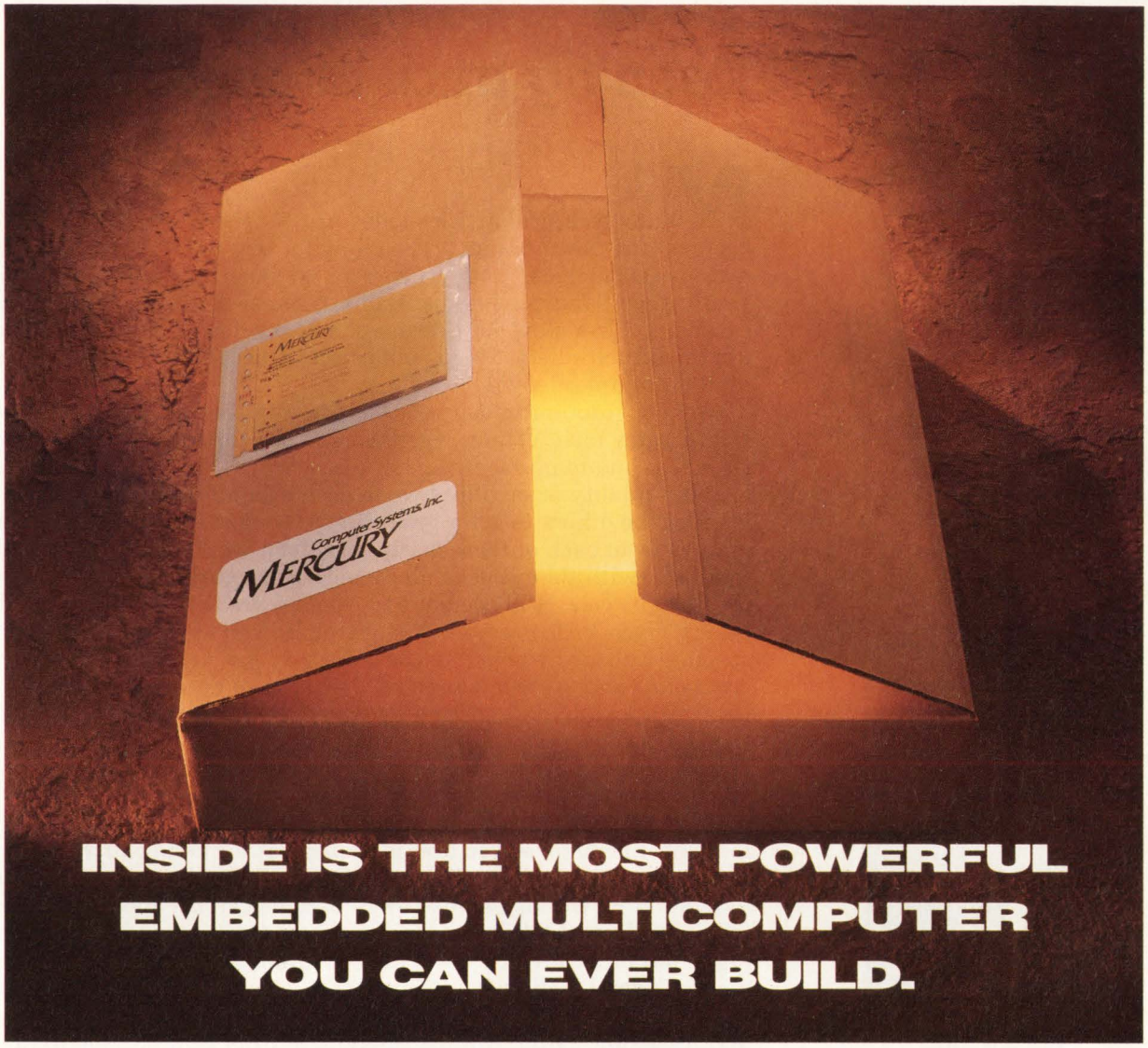
—Mike Donlin

Neural network uses 3-D stacking technology

Irvine Semiconductor (Costa Mesa, CA) is using its 3-D chip-stacking technology and flip-chip bonding methods to develop a multiple-layered neural network device. Dubbed the neural conditioning module (NCM), the device will be able to recognize and abstract features from a focal plane array. According to Irvine, the module's highly parallel architecture and processing power could be combined with next-generation artificial intelligence software to produce a system that could truly emulate the human brain, when prototypes are completed in about two years.

The module hosts a 128×128 detector array that is bump-bonded to a laminated cube using flip-chip technology. Another chip, the lateral resistive layer, is bump-bonded to the NCM, and contains an array of addressable and variable resistances. Signals processed by the device are sent through a crossbar switch that effectively connects the 128 inputs through seven layers of processing nodes to 128 outputs. Irvine spokesmen say the module will result in a new class of smart sensors that can operate on a real-time basis for military and commercial applications.

—Mike Donlin



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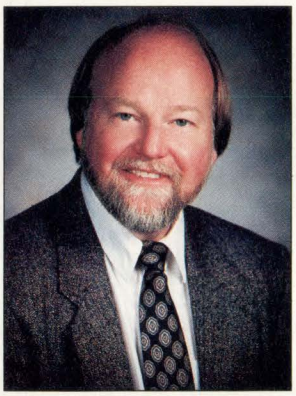
CIRCLE NO. 8

Keeping track of change

"We hear from many sources that the way the electronics industry operates must change."



Mike Donlin
Senior Editor

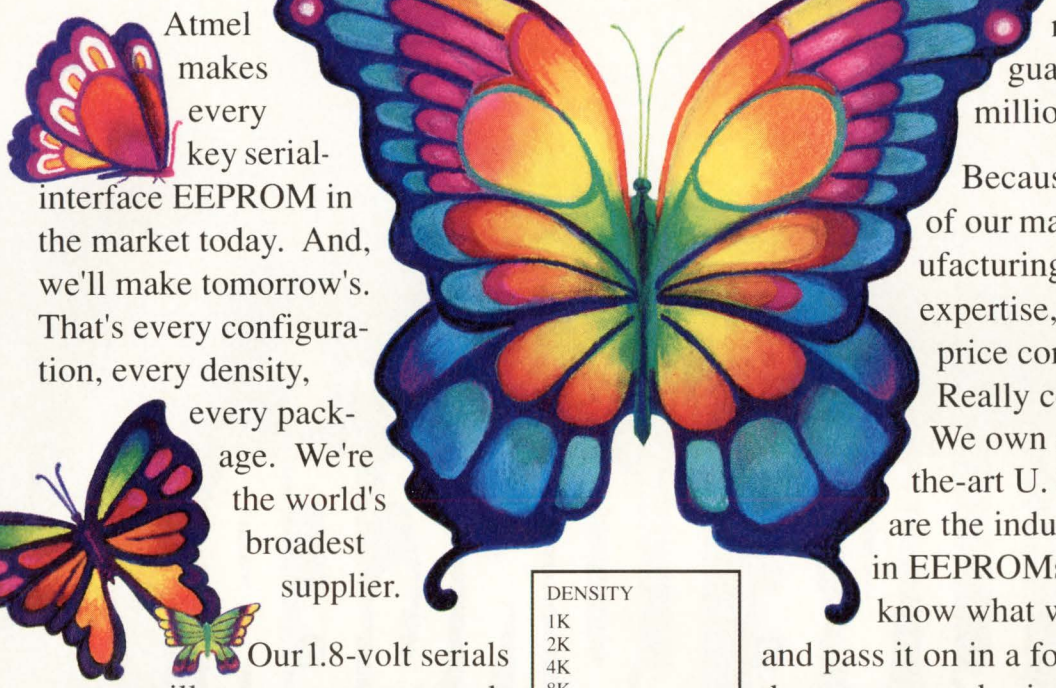
Many technical articles today are peppered with phrases such as "top-down design," "designing for testability," "over-the-wall methodologies," and "concurrent engineering." The use of this verbal shorthand is often justifiable, because the topics under discussion are complex, but overuse can water down these terms and diminish their effect. This is unfortunate, because the concepts behind them are all valid.

We hear from many sources that the way the electronics industry operates must change. Engineers in the insulated worlds of design, test and manufacturing are discovering that precious time is lost and quality is sacrificed when each group must modify the work of the others to get a product out the door. We're told that engineers from each of these disciplines must work concurrently on a project, with the needs of all considered as early as possible in the design cycle. Still, we have to wonder, are these changes really taking place, or is everyone just giving lip service to change while staying stubbornly bound to the old ways? Are semiconductor, circuit board and system houses really trying to design their products with testability and manufacturability in mind? Are the walls that have separated different departments really crumbling? Will engineers and managers accept the ramifications that these changes portend?

Here at *Computer Design,* we're as anxious to know the answers to these questions as you are. It's senseless for us to churn out articles about trends that don't exist, but it's equally senseless for us to ignore real trends because we've become cynical about the electronics industry's ability to embrace teamwork concepts. So, starting in January, we'll be featuring a column called "Tools and Techniques," which will try to answer these and other questions about the changing face of our industry. I'll be spearheading the effort, and my fellow editors will be stepping in from time to time to examine the same trends in their respective beats—buses and boards, integrated circuits, ASICs, and software. But we need your help.

We're looking for input from our readers, vendors and users alike, to help us keep the column in focus. We'd like to hear your opinions about the changes taking place in design, test and manufacturing. We want to track the transition of the designer from rugged individualist to team player. We need to know if those of you in management support these trends, or if you're leery of changes that could poison morale and derail productivity. So give me a call at (508) 392-2123, and let me hear your side of the story. With your help, *Computer Design* can chart what promises to be an interesting journey for us all.

SERIAL EEPROMs: ALL SHAPES, ALL SIZES, ALL 1.8 VOLTS



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CIRCLE NO. 9

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CIRCLE NO. 10

Dan DiLeo on: 3-volt mixed-signal ASICs

As the demand for advanced low-power portable systems—cellular telephones and laptop, palm-size and pen-based computers—increases, the electronics and computer industries are shifting to lower-voltage ICs and ASICs. The relentless shrink in chip geometries is also a driving force, because devices made with 0.5-µm-and-under design rules will require reduced supply voltages.

Some of the larger, next-generation desktop commercial and industrial systems are also moving in this direction, but they will first be based on hybrid 3-V/5-V designs. This is an interim step designed to cope with the higher power dissipation associated with geometries that go below 1 µm—and with tomorrow's 0.5-µm geometries and their higher clock rates.

As this technology unfolds, chip vendors are bringing to market 3-V microprocessors, RAM, discrete logic, and ASIC libraries. Third-party CAE/CAD suppliers are scurrying to develop tools to handle these mixed 3-V/5-V and 3-V designs, coming in both digital and mixed-signal flavors.

Prudent designers must be wary in approaching 3-V technology. To avoid the problems they experienced at 5 V, they must be careful to check out 3-V ASIC libraries, and to look for difficulties with low-voltage ASIC designs. The predictability of low-voltage designs is directly related to ASIC cell characterization and how it's performed. The right way is to fully characterize each and every cell and macro in a library; the wrong way involves the careless application of global derating factors.

The right way vs the wrong way

The proper characterization of cells in a library involves two major steps. First, you select the appropriate power-supply limits so the devices in the library will operate effectively. It's within these voltage limits that the models in a cell library are expected to provide accurate simulation results. Second, each individual cell is completely characterized for delay behavior over a selected range of V_{DD}, input, slew rate, capacitive load, temperature, and wafer-process variations. Engineers designing with a 3-V or 5-V library can then calculate delays using a gate-level simulator and get the delay values they're expecting.

Unfortunately, silicon vendors can publish incorrect methods in order to move product quickly to eager but naive electronic systems manufacturers. One such method involves lowering the power of existing 5-V silicon to 3 V and hoping the ASIC will operate as intended. This is risky because silicon powered down to a lower voltage may exhibit different temperature characteristics or other anomalous behavior due to the change.

With limited characterization data, how can chip-level evaluations be performed accurately? And how can all the circuits in an ASIC and their critical paths be simulated or tested under all worst-case conditions?

A second incorrect approach isn't as risky, but it still doesn't work well in efficient, high-performance 3-V design. This approach uses derating factors, or the estimated average percentage by which device characteristics will change for most, or all, cells in a library. The odds of attaining favorable results aren't good with this method, because each cell derates in a slightly different way, depending on the mix of P- and N-channel devices in it.

Derating is also inaccurate because of increased gate delay, which results from a decrease in transistor gain as the operating voltage is reduced. And differences in how P- and N-channel devices are structured in different gate types cause them to derate differently and to exhibit different gate delay-vs-voltage charac-

Dan DiLeo is director of worldwide ASIC product management, AT&T Microelectronics, Allentown, PA.

teristics. In a NAND gate, for example, P-channel devices are in series and N-channel devices are in parallel. NOR gates, on the other hand, have P-channel transistors in parallel and N-channel devices in series. This variation can result in setup-time errors for different types of flip-flops or in variations in rise and fall times for different gate structures.

Such inaccuracies aren't what systems houses expect as they start to develop new product engineering plans. Aside from wishing to deploy fully characterized libraries, they'll want to keep virtually the same design routines they've used in the past, so the same terms and conditions that exist for 5-V ASIC design must be maintained for 3-V design.

Welcome, analog

The same holds true for analog functions, but with an additional challenge—many digital designers view analog design as an arcane art form characterized by its complexity and unpredictability. It's clear that the challenge is to make analog features and functions as robust and predictable as the digital features and functions with which designers are familiar.

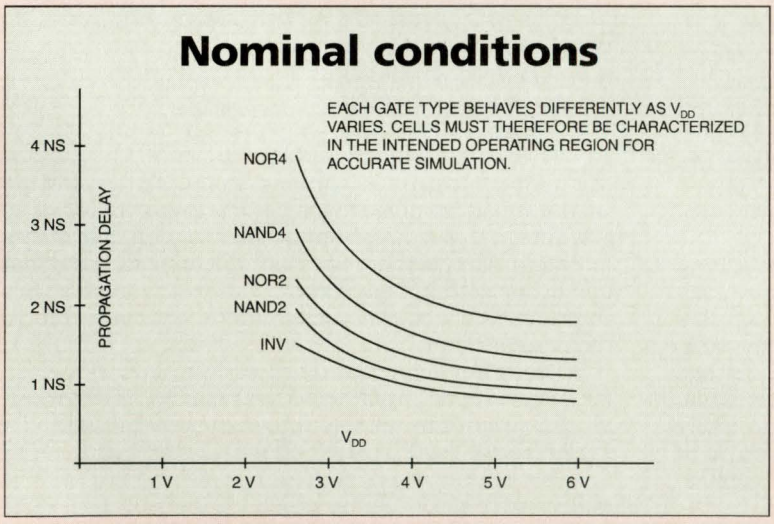
Full characterization of 3-V analog cells must, therefore, be based on procedures similar to those used for 3-V digital cells. But unlike improperly re-characterized or derated digital cells, which can still function, improperly characterized analog cells won't work at all. This is because analog cells require precise accuracy; there's no middle ground, no compromise and certainly no room for estimates.

Analog cell performance springs from three processes: transistor modeling, simulation and post-silicon design tolerance evaluation. First, you need state-of-the-art MOSFET modeling to get the best representation of the performance of an analog circuit via simulation. It's particularly important to base a model on a single equation for the triode, saturation and subthreshold regions of a transistor. Other models use separate equations for each of these regions, but, as a consequence, accuracy of simulation suffers.

There are linear equations for the triode region; other equations cover saturation; and a third group of exponential equations applies to the subthreshold region. As a result, adverse effects known as kinks and glitches occur in the transistor source drain current, transconductance and output conductances at the boundaries between regions. Distortion is created as a consequence. These kinks and glitches also lead to reduced predictability in a model and in the real analog circuitry, so the device might not perform as expected and possibly will fail completely.

An important step in building the accurate models needed for proper analog cell characterization and simulation is extraction of detailed parasitic information from the physical transistor layout and the use of this information in transistor-level analysis to ensure accurate simulation. This information includes transistor sizes, routing capacitances, internode coupling capacitances, and sizes of the parasitic diodes.

The third and final step in producing a high-performance analog cell is taken during the silicon fabrication process. Design tolerance evaluation (DTE) is an integral part of that process; it involves analyzing large groups of finished silicon wafers that represent best-case (fast-device), nominal and worst-case (slow-device) scenarios with various parasitic loadings. DTE is accomplished by controlling the variation of such parameters as channel length, channel width, gate oxide, and dielectric thicknesses. After the devices are fabricated, samples from different process categories are characterized to generate an accurate set of specifications covering extremes of processing, voltage and temperature.

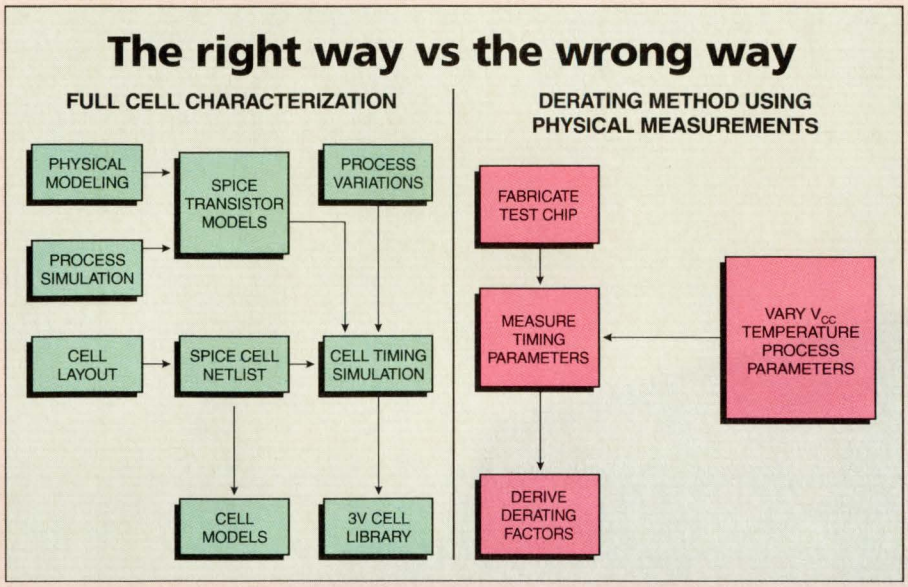


Architecture, signal level, specs

Gaining a good understanding of performance and accuracy criteria for analog circuitry gives designers a basis for dealing with other analog cell issues. Architectures, signal levels and specmanship, for example, have to be confronted in designing low-voltage ASICs. In a world of analog CMOS, the 5-V chip structures and circuitry that vendors have long relied upon won't necessarily work when implemented at 3 V. Designers will also have to be cautious with signal-level specs and input ranges. There's ample headroom on input values at 5 V, but it won't be available at 3 V.

Specifications dealing with such parameters as linearity, resolution, operating voltage range, and temperature, moreover, will be an open question as the industry picks up speed in the 3-V mixed-signal ASIC area. We're only now crossing the low-voltage analog threshold, but within a year specs will be coming from several directions. The questions to be asked are: Is the operating range to be 3.3 V ± 5 percent? Or ± 10 percent? Or will operating ranges be specified even lower than the de facto 3.3-V standard?

It's important that designers understand the ways in which 3-V mixed-signal ASIC vendors specify 3-V analog blocks. They usually establish a tighter operating range for analog than for digital circuitry at the lower voltage. Some analog cells will require off-chip components to achieve higher performance, and these support devices will also need tighter specifications. A more tightly specified, and more expensive crystal, for example, will be necessary to achieve higher fre-



quencies in an oscillator cell.

These fresh technology and design issues add a few wrinkles to the traditional ASIC design flow, the most important of which is mixed 3-V and 5-V operation. System designers pressing ahead in this area must settle at first for hybrid power-supply levels, since not all components today are geared to 3-V operation.

Mixed 3-V/5-V design

One of the big pluses of mixed 3-V and 5-V design is flexibility. Traditionally, designers have had little latitude in changing a design in midstream. Once a design was begun, the best option involved selecting the most appropriate CMOS cell or macro for a specific function. Now designers can tap into both 3-V and 5-V cell libraries and use either CMOS or BiCMOS cells, depending on circuit requirements. Special CMOS cells can be dialed up and mixed and matched, even after the design is well under way. And BiCMOS drivers and buffers are especially valuable for surmounting high capacitance drive barriers.

It's a good idea, then, to abandon earlier engineering thinking and try to understand the nuances of current design practices, particularly in the areas that design managers have long taken for granted, such as layout. Historically, designers have confidently turned over their 5-V designs to silicon vendors for placement-and-routing and the subsequent steps leading to finished silicon. Mixed 3-V and 5-V design, however, introduces fresh concerns at the layout stage, such as getting optimal placement in an ASIC chip of 3-V and 5-V analog and digital cells and macros to attain a targeted performance. Other concerns include verifying on-chip 3-V/5-V interfaces; circuit partitioning to ensure that 3-V/5-V analog and digital chip portions are segmented according to a specific ASIC design and having single-pass timing calculation as part of layout to comply with time-to-market schedules. Systems houses will have to take a greater interest in this part of the cycle, since it can create new problems concerning performance and the design schedule.

To avoid such pitfalls, it's best that floorplanning tools automatically assign separate circuit sections to specific locales within the logic core. Many cell-area possibilities can quickly be checked to reveal the best topology for a given design. Floorplanning tools perform other functions as well, such as clustering similar cells to keep the number of power-supply lines to a minimum. But their most significant capability comes with layout software that can concurrently place all 3-V and 5-V cells for optimized designs. Without these tools, multiple independent placements are necessary.

Silicon vendors can help here by providing expert direction in targeting separate power-supply functions, including specifying the arrangement of power buses to 5-V and 3-V rails. These vendors can also point out design restrictions—whether or not a group of 3-V or 5-V cells is best placed in a certain corner of the chip, for example. Layout accuracy becomes more important here, because masked inefficiencies lead to lower performance.

Inefficient layout also adversely affects the customer's design schedule, because it can create the added burden of troubleshooting. And layout problems in mixed 3-V and 5-V ASIC designs will be more difficult to track and resolve than those at traditional voltage levels, because mixed-power supply/mixed-signal layout entails more tasks and covers diverse areas where more mistakes can occur. That's especially true if silicon vendors use conventional layout tools that require much manual intervention. Unfortunately, when new problems crop up, they translate directly into time-to-market losses and aggravate the risk that latent problems will turn up at the system designer's location.

Outlook for the future

The move to 3 V will yield many system benefits, some of which remain to be discovered. For the present, we can expect extended battery life, increased reliability, reduced electromechanical interference, tighter packing densities, and—one of the biggest advantages—continuing use of low-cost plastic packaging.

The applications most readily moving to low-voltage designs are in the areas of mass storage and mobile computing, with workstations not far behind. In portable PCs, full conversion to 3-V systems will probably be accomplished by the end of next year, with traditional 5-V system implementations phased out of all portables by 1994.

Wireless communications and multimedia represent two emerging applications that will propel 3-V ASIC technology into true systems-level ICs. This will probably involve large-function DSP and communications macros, operating in tandem with other memory and logic structures in the same ASIC chip, all operating at 3 V in both digital and analog circuitry.

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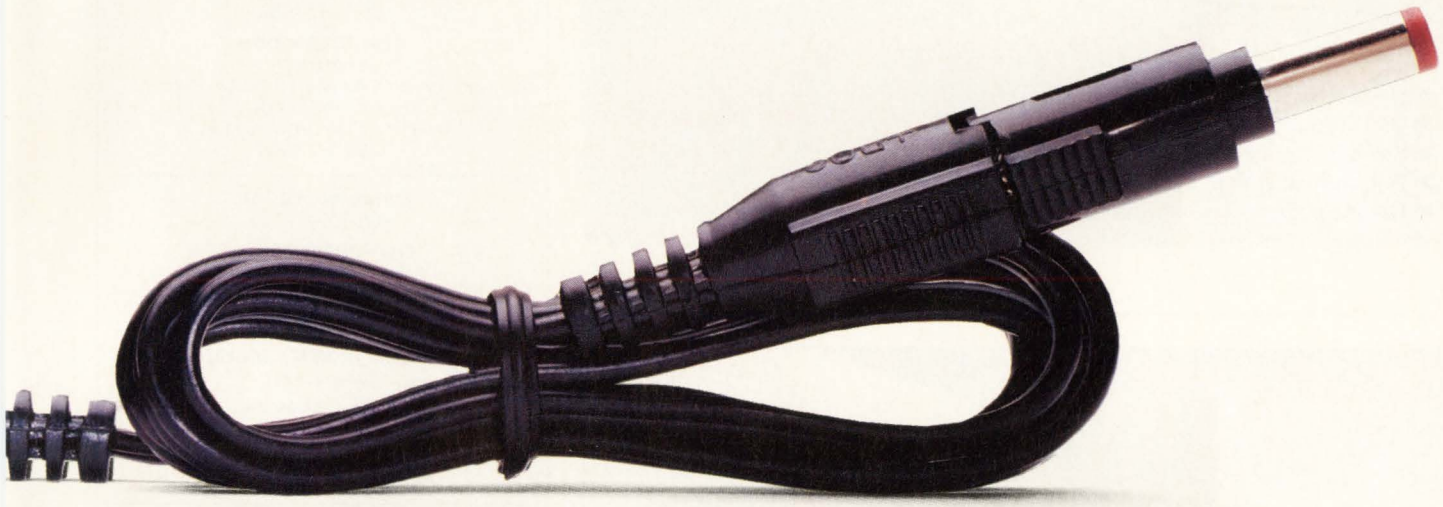

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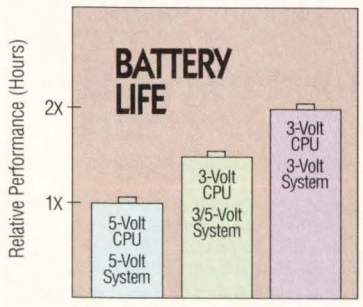

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BPA ABP

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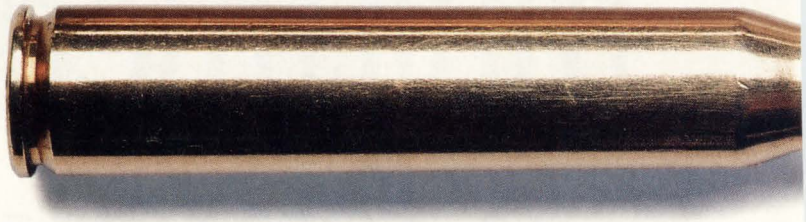

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CONFERENCES

November 16 - 20
Comdex/Fall '92

Las Vegas, NV. Comdex/Fall, one of the largest trade shows in the country for computer and communications products, returns for its 14th year. The show focuses on the strategies and technologies of enterprise computing in the 1990s with five programs: corporate computing, new media, connectivity, the channel network, and international business and marketing. Also featured are four technology showcases, covering network computing, multimedia, imaging, and OEM business. Contact: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, Fax (617) 449-2674. **Circle 267**

November 17 - 19
Wescon '92

Anaheim Convention Center, Anaheim, CA. The Wescon International Electronics Conference and Exhibition expects to draw more than 45,000 professionals to sunny California. Featuring more than 1,400 exhibitors, Wescon '92 presents five separate shows, highlighting such products as semiconductors, ICs, ASICs, EDA tools, and test and measurement equipment. Each show is complemented by dedicated technical sessions, covering topics relating to programmable architectures FPGAs, computer-integrated manufacturing, VXIbus modular instrumentation, and microelectronics packaging. Contact: Patti Masters, Wescon '92, 8110 Airport Blvd, Los Angeles, CA 90045-3194, (310) 215-3976, Fax (310) 641-5117. **Circle 268**

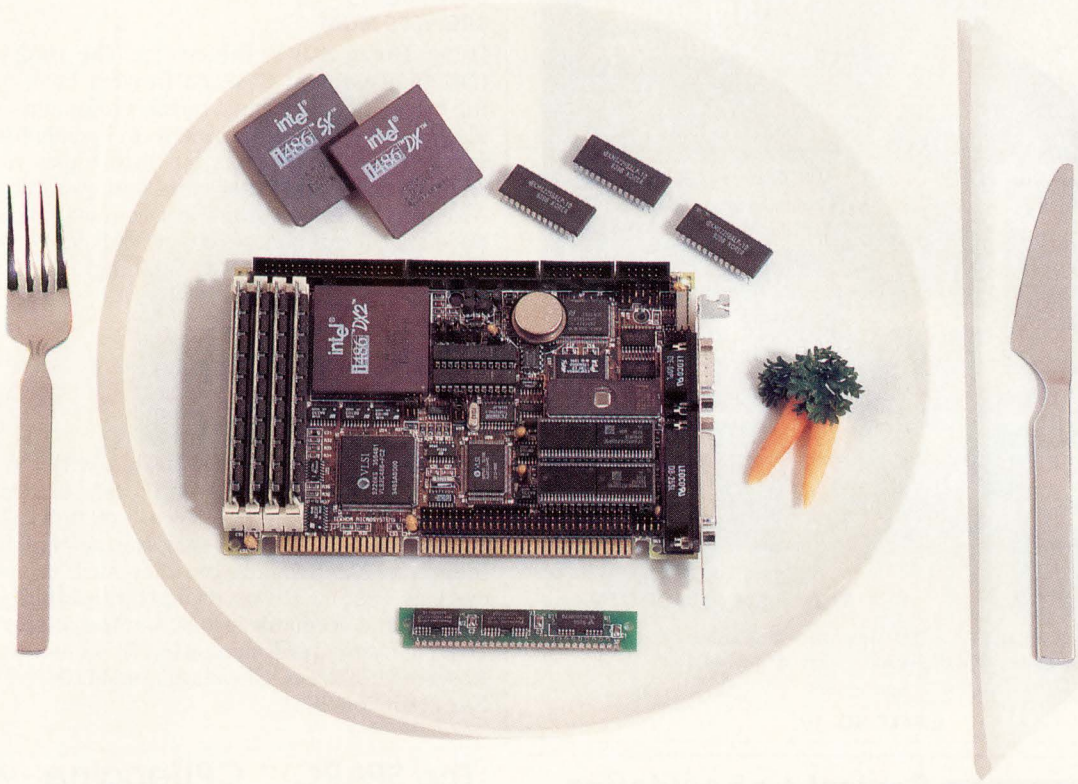
December 1 - 3
AFCEA Hawaii '92

Sheraton Waikiki Hotel, Honolulu, HI. The seventh annual Hawaii Pacific International Electronics Conference & Exposition provides a discussion forum for military, government and industry professionals from the U.S. and the Pacific Rim nations. The technical program will address such topics as electronic security, force downsizing, software reusability, and opportunities for U.S. industry in the Pacific Rim region. Contact: J. Spargo & Associates, 4400 Fair Lakes Ct, Fairfax, VA 22033, (800) 336-4583, ext. 6200, Fax (703) 818-9177. **Circle 269**

December 1 - 3
Technology 2002

Baltimore Convention Center, Baltimore, MD. Technology 2002, the third national technology transfer conference and exposition, features presentations by federal laboratories and contractors on the latest advances in computer, science, electronics, and manufacturing technologies. Sponsored by NASA, NASA Tech Briefs and the Technology Utilization Foundation, the conference offers more than 120 symposia and 60,000 ft^2 of exhibits. Contact: Wendy Janiel, Technology Utilization Foundation, 41 E 42nd St, New York, NY 10017, (800) 944-6272, Fax (212) 986-7864. **Circle 270**

Continued on page 28



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CIRCLE NO. 18

CALENDAR

CONFERENCES

Continued from page 26

December 13 - 16
1992 IEEE IEDM

Hilton Hotel, San Francisco, CA. The 1992 IEEE International Electron Devices Meeting brings together engineering professionals from industry, government and academia. The meeting features 36 sessions on such topics as solid state technology, integrated circuits and quantum electronics. Also offered are several short courses, plenary sessions and panel discussions. Contact: Melissa Widerkehr, IEDM, Ste 610, 1545 18th St NW, Washington, DC 20036, (202) 986-1137, Fax (202) 986-1139. **Circle 271**

January 3 - 6, 1993
VLSI Design '93

Taj Intercontinental Hotel, Bombay, India. The Sixth International Conference on VLSI Design, with the theme *Chip, Board and Systems Design in the 90s*, brings researchers and designers to the west coast of India. The four-day program consists of paper sessions, posters, tutorials, and industrial CAD exhibits, covering such topics as CAE/CAD systems, logic synthesis, design for testability, circuit simulation, and economic issues. Contact: Rochit Rajsuman, Dept. of Computer Engineering & Science, Case Western Reserve University, Cleveland, OH 44106, (216) 368-5510, Fax (216) 368-2801. **Circle 272**

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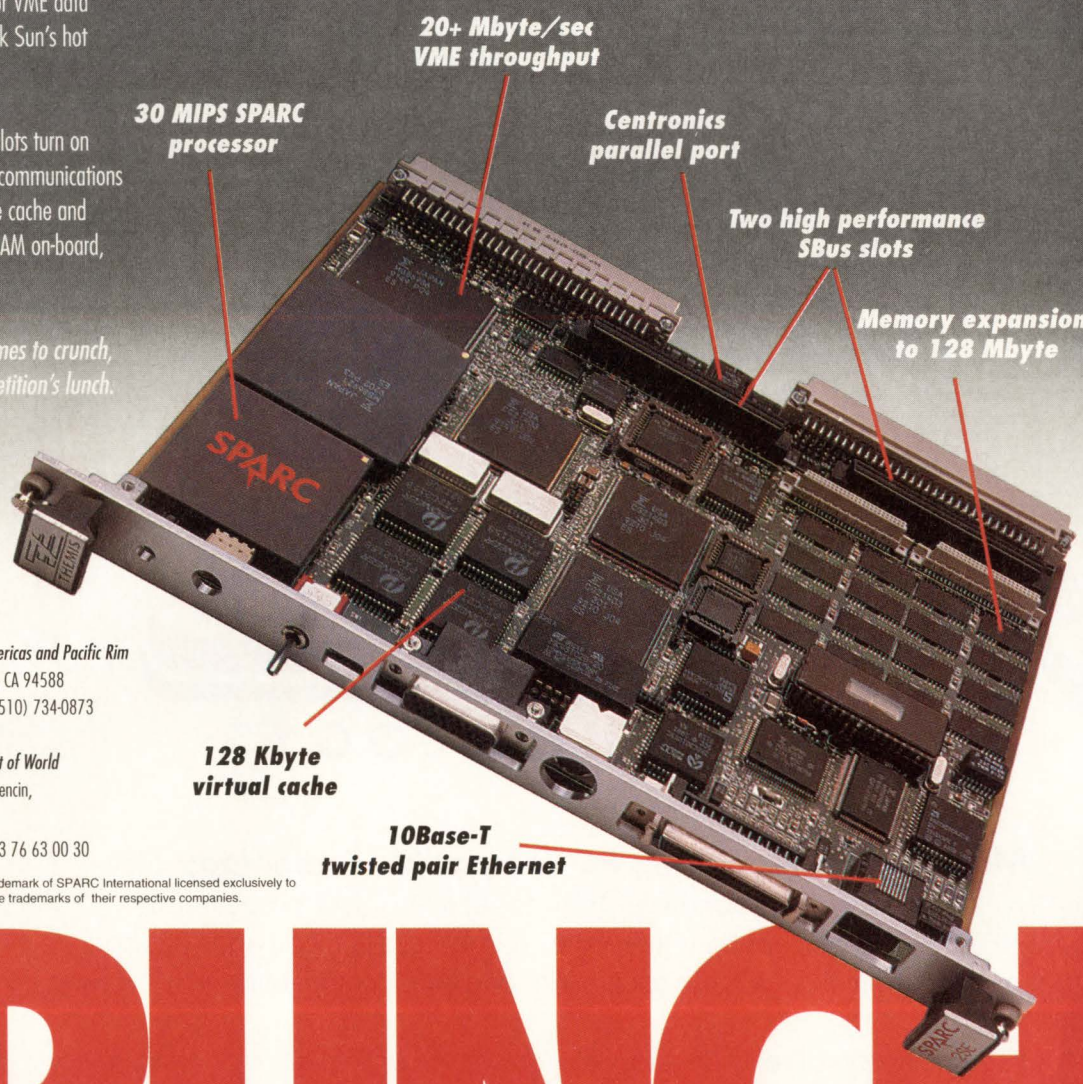

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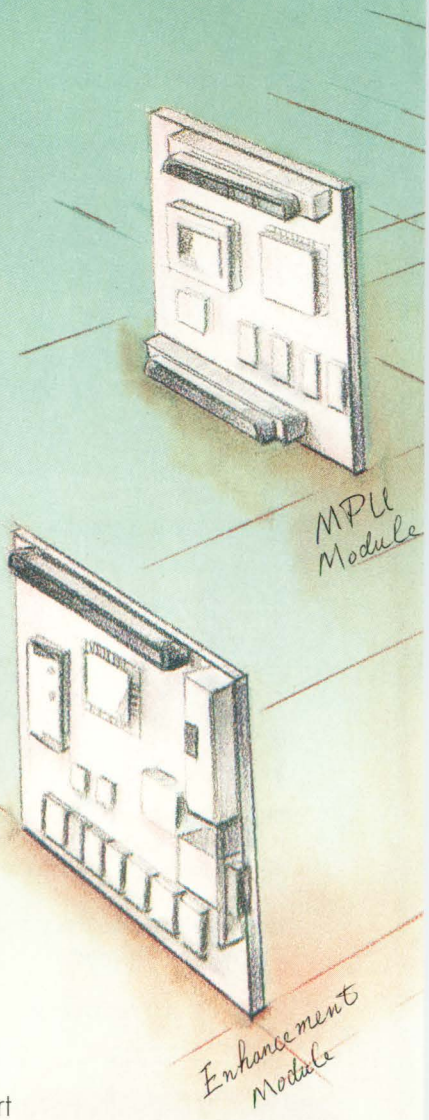

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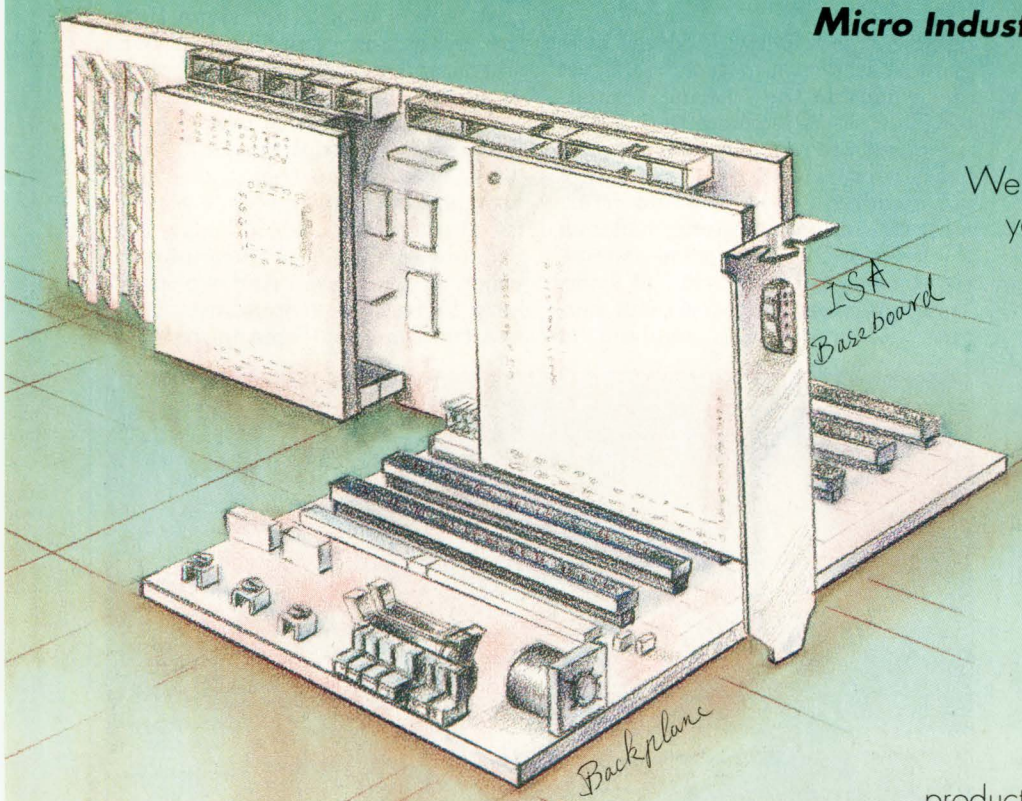

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CIRCLE NO. 22

CAE/CAD TOOLS

EDA and test vendors forge alliances to promote standards

Mike Donlin, Senior Editor

The recent International Test Conference (ITC—Baltimore, MD) marked a shift in testability's role in system design. A spate of alliances and joint technology/marketing agreements heralded what many analysts and engineers alike agree will be a new relationship between design, test and manufacturing departments.

Perhaps the most significant of these announcements was the official launching of the Design & Test Alliance (DTA), a confederation of automatic test equipment (ATE) vendors, electronic design automation (EDA) software suppliers, system houses, and semiconductor companies. Although the Alliance is still in its infancy, initial meetings provided encouraging signs that participating companies would unplug the test bottleneck plaguing the production cycles of today's complex ICs and systems.

The DTA's primary objectives are to spur cooperative efforts between vendors and users of design and test technologies and to raise management's awareness of the importance of integrating these technologies with operations. Through ongoing research programs and projects, the Alliance will try to provide quantitative data and analysis on this integration. Another major goal of the group is to accelerate the integration process by sharing the results of its analysis with the electronics industry.

The Alliance is presently composed of nine companies: Cadence Design Systems (San Jose, CA), GenRad (Concord, MA), Hughes Aircraft (Los Angeles, CA), LTX (Westwood, MA), Mentor Graphics (Wilsonville, OR), Racal-Redac (Mahwah, NJ), Synopsys (Mountain View, CA), Teradyne (Boston, MA), and Texas Instruments (Dallas, TX). These companies will pool resources to create a board of directors, administrative personnel, a steering committee, a research committee, and working groups.

The working groups are currently being formed. They'll address integration issues at a technical level and report to the steering committee. The steering committee will be composed of four categories of members, representing EDA, test, support, and end-product manufacturers, with members from academia involved in the appropriate categories based on their technical focus. These member categories will permit the engineering problems of each group to be represented and addressed adequately at the management level of the alliance.

The DTA is scheduled to present its initial research findings in the first quarter of 1993.

The Alliance hopes that, by bringing a managerial as well as a technical focus to the effort, it will be able to convince the computer industry of the importance of bringing test issues forward in the design cycle. "The way the industry approaches test is fundamentally changing," says Jeff Hotchkiss, vice-president of Teradyne. "Today, there's a broader set of issues that has to do with the integration between silicon vendors, EDA tool suppliers and ATE companies. It affects how designers test their systems."

Although the need for such integration has existed for some time, the increasing complexity of both silicon and systems, and the resulting lack of accessibility for mechanical testing devices, is bringing the design-for-testability issue to a head. "We realize that there have been pockets of design-for-test activity through the years," says Jim Solomon, president of the analog division at Cadence. "And we aren't here to become a standards body. But the time has come to instill in the minds of the design and test communities the need to address product development in conjunction with a synergistic design/test philosophy. DTA aims to educate both camps toward the common goal of productive product development."

Members of the Design & Test Alliance conducted a press conference to kick off the consortium's efforts. Press conference speakers, from left to right, are: Doug Kostlan, TI marketing manager; Vin Ratford, Mentor Graphics marketing manager; Jim Solomon, president of the analog division at Cadence; and Jeff Hotchkiss, vice-president of Teradyne.

Partners for standards

In addition to the announcement of the DTA, the ITC saw the formation of other alliances portending the integration of design and test as well as the acceptance of standards such as IEEE 1149.1 for boundary-scan design methodologies. Tektronix (Beaverton, OR), Teradyne and Tex-

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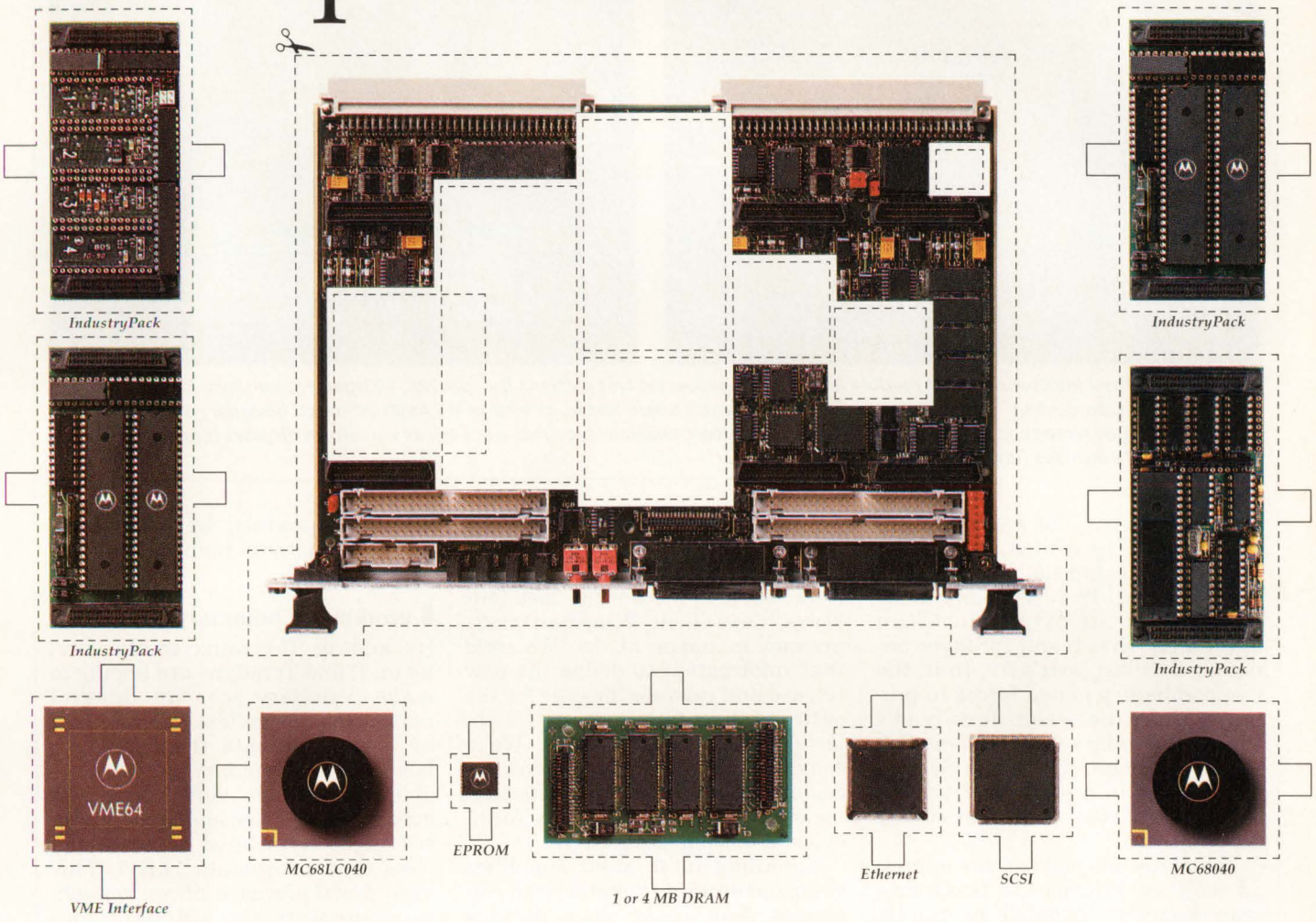

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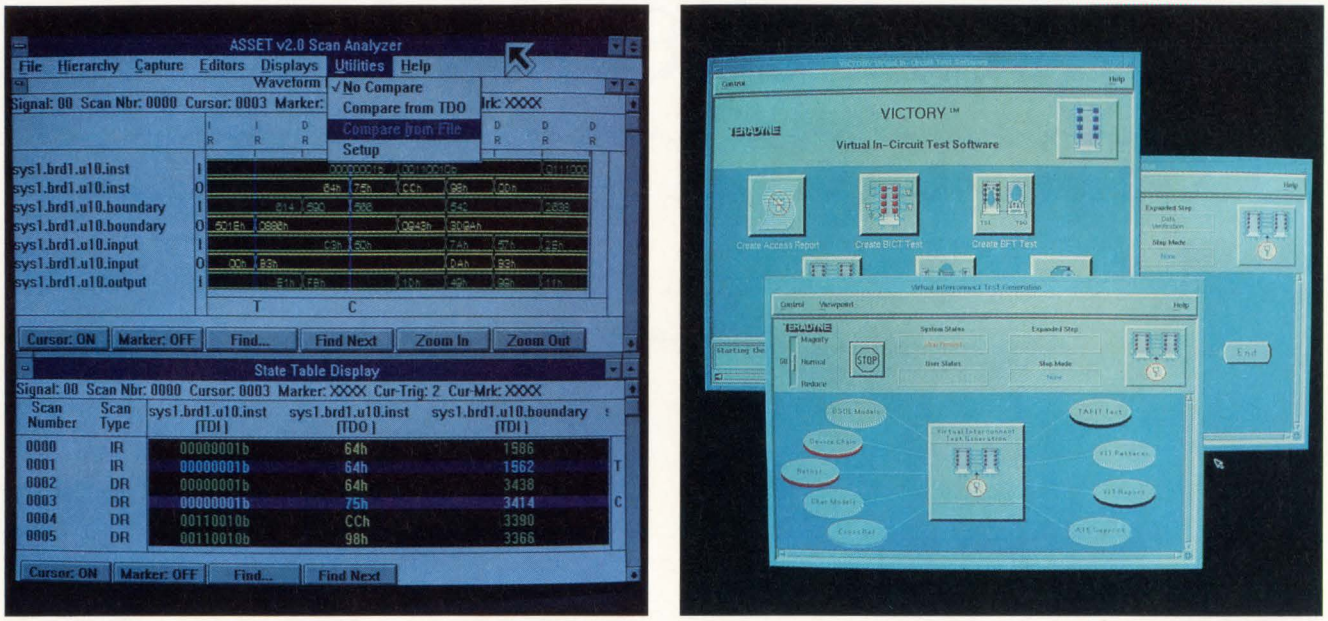

Teradyne's Virtual Interconnect Test module (left screen) generates test patterns that provide 100-percent pin-level fault coverage for boundary-scan devices. The module can link to Teradyne's board testers as well as TI's ASSET PC-based boundary-scan design debug tool (right screen). ASSET's scan analyzer supports logic analyzer-type features such as waveform displays (upper window) and state-table displays (lower window).

as Instruments, for example, announced an agreement on a joint development and marketing effort to support 1149.1. The new relationship is an extension of an agreement that TI and Teradyne announced at last year's ITC. In it, the two companies joined forces to promote links between Teradyne's Victory boundary-scan test module and TI's Advanced Support System for Emulation and Test (ASSET) via Teradyne's Virtual Interconnect Test (VIT) software.

Tektronix will join in these efforts, as well as incorporate boundary-scan diagnostic capabilities into its laboratory rack-and-stack equipment during 1993. "We're pooling our efforts to reach four major goals," says David Fink, market segment manager at Tektronix. "First, we're committed to the development and integration of products supporting the 1149.1 family of buses. Second, we're going to promote industry standards to take full advantage of 1149.1 features. Third, we're going to develop cooperative programs to serve the specific needs of customers through our combined expertise. Finally, we'll be cooperating in joint training, sales and marketing."

Texas Instruments also used the ITC forum to announce a revamped version of its ASSET boundary-scan development suite—Version 2.0. "The new release is based on input from customers over the last four years," says Glenn Woppman, ASSET product manager at TI. "We used that information to define the new release and rewrote the code for the entire product family using C++ object-oriented methodologies. We're convinced that boundary scan's acceptance depends on products that make it easier for designers to include it in their designs."

According to TI, ASSET simplifies scan-path management and increases scan speed via a test-bus controller. Through its object-oriented database and controller-based architecture, the system assumes the burden of counting test clocks and managing test access port state transitions. ASSET also includes an interactive debugger and scan analyzer. By interacting at a functional level, you can scan instructions or data into device test registers and view results.

Another test vector development method that ASSET supports is 100-percent boundary-scan interconnect automatic test pattern generation (ATPG). "Customers told us that ATPG for boundary-scan interconnects is a key concern," says Woppman. "The ASSET VIT product, based on Teradyne's Victory technology, addresses that."

Workbench boundary scan

By adding Tektronix to the JTAG team, TI and Teradyne are hoping to make boundary scan an integral part of the design/test environment by bringing it into the engineer's laboratory. If boundary scan is available as a design verification and debug tool, they reason, then designers might be inclined to choose devices that incorporate 1149.1. This in turn will pressure silicon vendors to incorporate the standard into their off-the-shelf products.

Tektronix hopes that, by offering boundary-scan diagnostic capabilities to its customers, the company may woo them over to buying racks of test equipment from a single source. "People are getting tired of mix-and-match laboratory facilities where they have to try to connect incompatible equipment from different vendors," says Tektronix's Fink. "We're also hoping that the new equipment, which is based on the VXIbus, will let them downsize their equipment racks while increasing the bandwidth of their test systems. The older GPIB standard reaches its limits at around 200 kHz, while VXI

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can accommodate data transfers of up to several MHz."

Looking to the future

With all of this technical clout behind design-for-testability efforts and standards such as 1149.1, members of these alliances are hoping they can overcome the knee-jerk reactions that many designers have to incorporating testability into their silicon and systems. But to do this, all of the players involved must hammer out standards that are useful, flexible and easy to use—no mean feat when so many corporate egos are involved. Still, if the EDA and test industries have learned anything from the trauma of trying to fold test into design, it's that compromise and simplicity are the keys to developing meaningful standards.

"A standard that tries to be all things to all people is bound to fail," says Doug Kostlan, marketing manager for TI's test technology center. "In the latest meeting of the boundary scan description language (BSDL) subcommittee, for example, we decided to leave clocking schemes out of the standard. It's a matter of really evaluating what's necessary to get the job done and get a standard out there so everyone can use it. If you take too long, everyone just goes out and develops their own way of doing things. Rather than just add on features, it's better to simplify and clarify." ■

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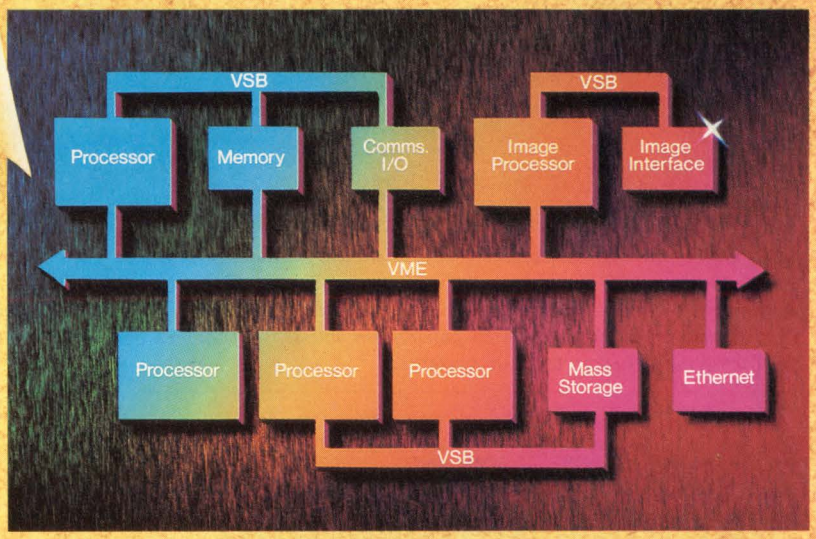

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CIRCLE NO. 25

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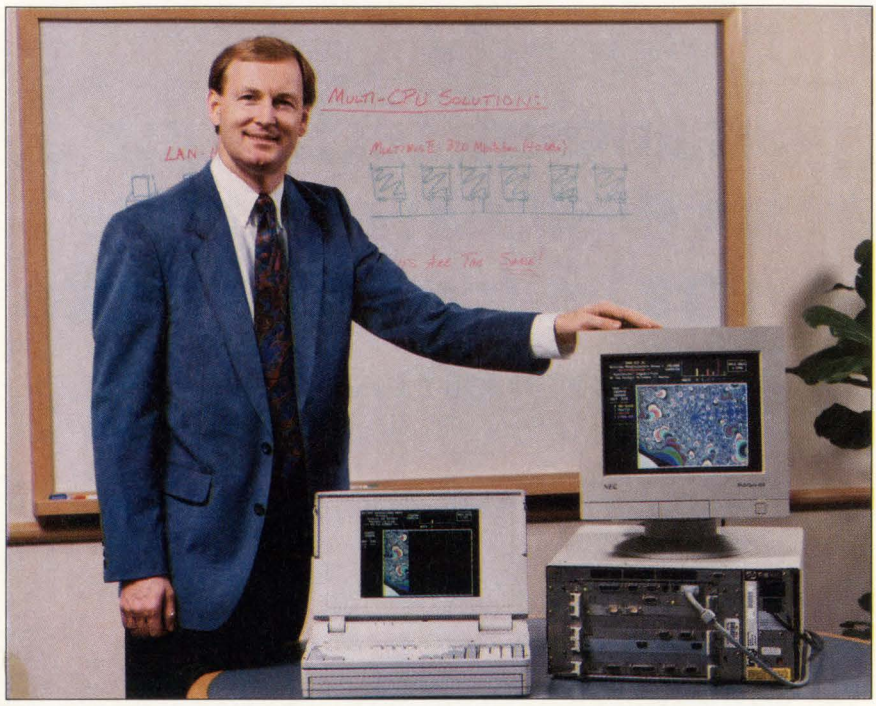

MMG executive director Len Schulwitz is shown at a demonstration comparing a 27-Mips, 33-MHz, 486-based laptop computer with a multivendor Multibus II system capable of churning out more than 300 Mips. The demonstration has the two machines performing a Mandelbrot fractal calculation, illustrating the dramatic difference in performance between the two systems.

2,000-Mips PC rescues high-end applications

Warren Andrews, Senior Editor

The Intel personal computer architecture and PC/MS-DOS operating system are now ubiquitous, and have made steady inroads into many commercial and industrial applications. Once rooted, this technology hasn't always been able to deliver practical solutions, but based on a hardware/software cost ratio of between 1:10 and 1:20, OEMs have been jumping through hoops—and putting their suppliers through ordeals—to make up for any inadequacies while maintaining software compatibility.

PCs have fallen down on the job for a variety of reasons. One is that PCs were intended for a relatively gentle office environment and can't handle harsh physical and electrical conditions. Many PC makers interested in industrial solutions have evolved environmentally hardened, passive-backplane systems, ruggedized motherboards, PCs embedded in other form factors (such as STD, Multibus and VME), and even totally new pin and connector configurations.

These solutions have solved many problems, but new ones have continued to appear—mainly in the areas of form factor, power dissipation and performance.

Form factor, power, performance

Responses to the form-factor problem have come from a variety of manufacturers, from the compact boards of Ampro Computers (Sunnyvale, CA) and the PC/104 consortium, to ESP designs from Dover Electronics (Longmont, CO), to the latest compact industrial PC from RadiSys (Beaverton, OR). Some of these solutions also address the low-power needs of portable and remote instrumentation.

When higher performance was required, OEMs have traditionally had to wait for the next generation of processor to emerge, hoping it will provide the needed performance enhancement.

This need for more and faster processing spawned the RISC revolution, unleashing a new type of processor with less baggage so that new generations can be implemented faster.

And then along comes the need for multiprocessing. Although multiprocessing technology is just starting to reach the marketplace in the form of new workstations, it provides little relief for those committed to the PC/MS-DOS environment. Promised multiprocessing configurations for MS-DOS-based machines haven't yet materialized.

Until now, that is. The Multibus Manufacturers' Group (MMG—Aloha, OR) has just come up with a solution to the problem that theoretically lets PC applications run in Multibus II multiprocessing environments at speeds of 2,000 Mips and beyond. The solution can be implemented today because it uses standard off-the-shelf boards.

The technology, demonstrated at Buscon East (Boston, MA, September 14-18), comes in two systems: a 33-MHz, 486-based laptop PC and a PC-based Multibus II system. In single-CPU configurations, both systems operate at 27 Mips. But the Multibus II system includes six boards operating together that produce more than a tenfold improvement. And, according to MMG executive director Len Schulwitz, the technology is fully scalable to a full 20-slot Multibus system, providing more than 2,300 Mips.

Schulwitz says the Multibus II message-passing capability acts as a fast LAN, which operates at 40 Mbytes/s. "The MMG Technical Committee developed high-speed communications among Multibus II boards and PC-based Multibus II boards which support DOS BIOS," says Schulwitz. "Known as the Multibus II Transport, the most recent release provides backplane communication between MMG boards and any DOS-based PC board on Multibus II."

For the demonstration at Buscon East, the MMG used boards from three vendors: a 120-Mips i860 board from Mentec Computer Sys-

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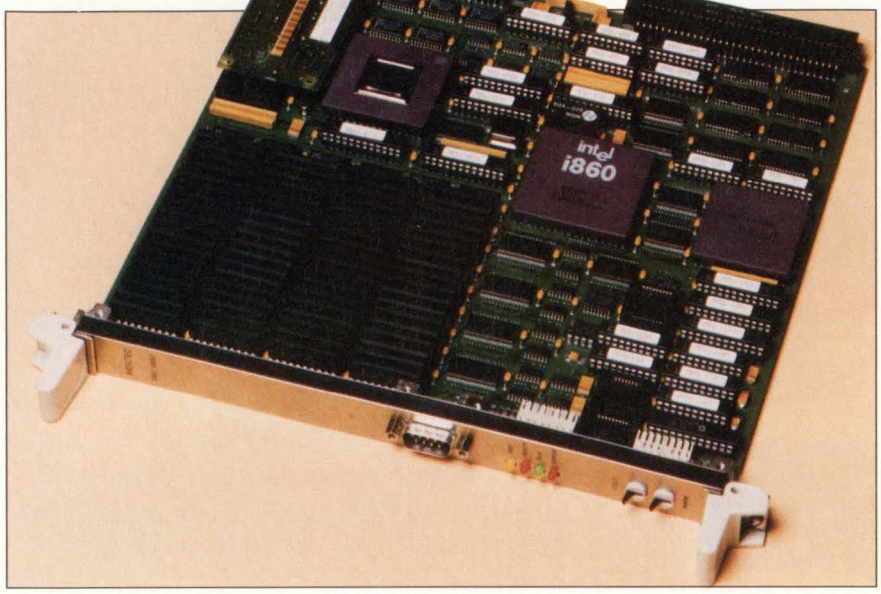
CIRCLE NO. 26

COMPUTERS & SUBSYSTEMS



One of the top performers in the MMG demonstration of high-performance DOS-based machines is Mentec's i860-based accelerator card. The board adds 120 Mips to the processing power of the Multibus II system.

tems (Dublin, Ireland); a 40-Mips i960-based processor board from Micro Industries (Westerville, OH); and three separate 486-based processor boards from Intel.

"To support these dramatically higher levels of PC performance," says Jack Blevins, MMG technical director, "PC systems must be scalable in both hardware and software. Hardware scalability lets you easily add processor boards to support multiprocessing without upsetting the existing system. More important, software which runs on a single-processor system must now be distributed to run on two or more processors."

"To solve the software problems," Blevins continues, "you have to scale PC software over multiple processors. To do this you have to overcome two obstacles. The first is task-to-task communications, which lets two or more CPUs share the load. The

second is sharing system I/O resources. A significant effort is needed to accomplish the seemingly mundane task of sharing disk, terminals and peripherals, and this is true from the exclusive ownership of a single processor, such as in standard PC systems, to coping with multiple processors that must access I/O."

Multiprocessing solution

The idea of using a number of PC-based CPUs in a multiprocessing environment has been tossed around for several years. Former Multibus wizard John Hyde frequently used such a multiprocessing paradigm to describe his view of the future of multiprocessing systems. Hyde left Intel's Multibus group to join the company's advanced processor group, where it's expected he will apply the same model to multiprocessing at the processor-chip level. While we wait for this higher chip-level performance to emerge, perhaps some of Hyde's legacy remains,

"To support dramatically higher levels of PC performance, PC systems must be scalable in both hardware and software."

—Jack Blevins
MMG technical director

since board-level technology that's now available can show significant advances over single-processor approaches in DOS-based systems. It may well even be possible to exceed the current speculations of MMG members.

For example, using the new MMG approach to double the speed of the Multibus II backplane to almost 80 Mbytes/s, intertask communication can take place with even greater ease than is currently the case. Further, Micro Industries recently introduced a DSP board sporting four AT&T DSP32C chips. "Putting 19 such boards to work in a system with an 80486 host could result in dramatically greater performance, solving the right kind of problem," says Micro Industries president Michael Curran. "It's possible to achieve more than 20,000 Mips on a DOS application using such an approach."

The MMG solution might not be for everyone, but it does allow OEMs now married to a PC-based solution to easily jump an order of magnitude in performance without waiting for individual processor chips to reach that level. Costs are high compared

with the PC laptop solution, and it won't fit under your seat in an airplane, but there are many applications where the higher level of performance has to be there and the increased cost is justified.

A pricey approach

The Multibus II approach provides dramatic scalability for those users requiring ultimate performance and willing to accept the increased cost of hardware and software development. Even compared with a pricey 50-MHz 486 (at well under $3,000), the Multibus solution is costly; each of the CPU boards used in the system is priced between $3,000 and $6,000. Then add to this the cost of a backplane, card cage and power supply.

Single-processor solutions aren't likely to reach the 2,000+-Mips performance level in the near future, but the migration from a single-processor PC to a multiprocessor Multibus II system won't be as seamless as going from one generation of CPU to the next. Someone has to tell which task to go where, and the MMG's software doesn't do that yet. ■

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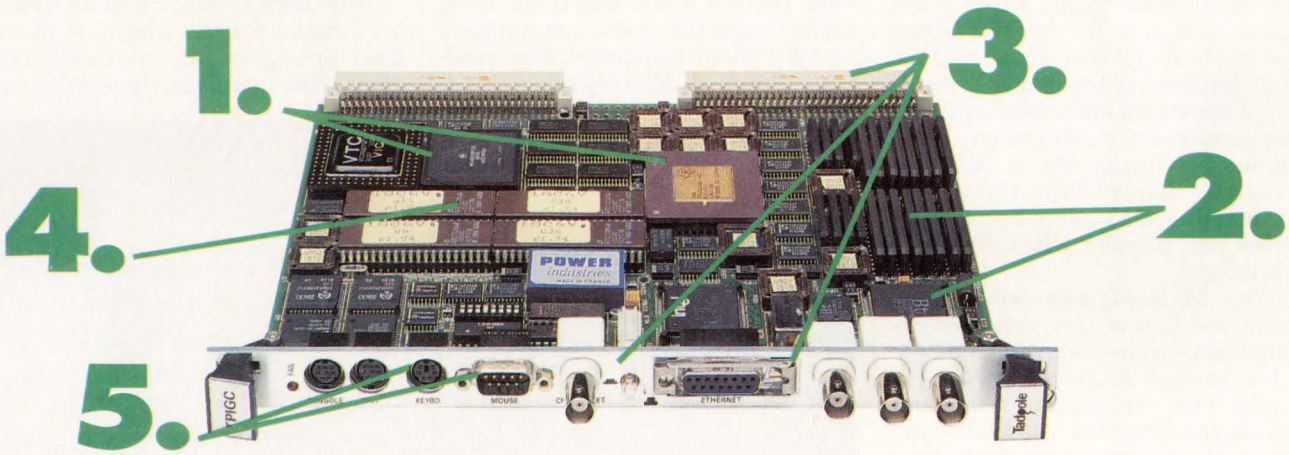

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CIRCLE NO. 29

SOFTWARE & DEVELOPMENT TOOLS

Integrated tool environment targets real-time development

Tom Williams, Senior Editor

Software tool integration isn't waiting for standards. Increasingly, tool vendors are setting up environments that address the way programmers develop code in the real world, which often doesn't conform to theories about how such development should be done. Answering the growing needs of real-time and embedded systems programmers for integrated development environments is Microtec Research (Santa Clara, CA), which has introduced a system based on its proven and popular XRay debugger technology.

XRay MasterWorks provides an integrated C and C++ software development environment for embedded systems engineers. Significantly, the environment doesn't include the front-end structured design and analysis CASE tools that have received so much publicity recently. Rather, XRay MasterWorks concentrates on tools for building programs, generating and debugging code, navigating through source files, and managing projects that are oriented toward enhancing the efficiency of the edit-compile-debug process, which is the way most developers are working today.

Message server at center

The hub of XRay MasterWorks is a message server that ties together the current suite of tools and provides for the integration of future tools. The server provides point-to-point communication between tools rather than broadcasting to all tools on the system. "For example," says product marketing manager Aurobindo Tripathy, "under the file menu, I have a button that says 'remake and reload.' Any time someone clicks that, we have to establish communication between the XRay Make tool and the debugger." The Make tool already knows what needs to be rebuilt, so the message only needs to tell the debugger what particular target is to be rebuilt. The debugger can then instantly be aware of all the files making up the program under development.

In the future, Tripathy says, Microtec is planning to open the messaging scheme so that you can integrate other tools.

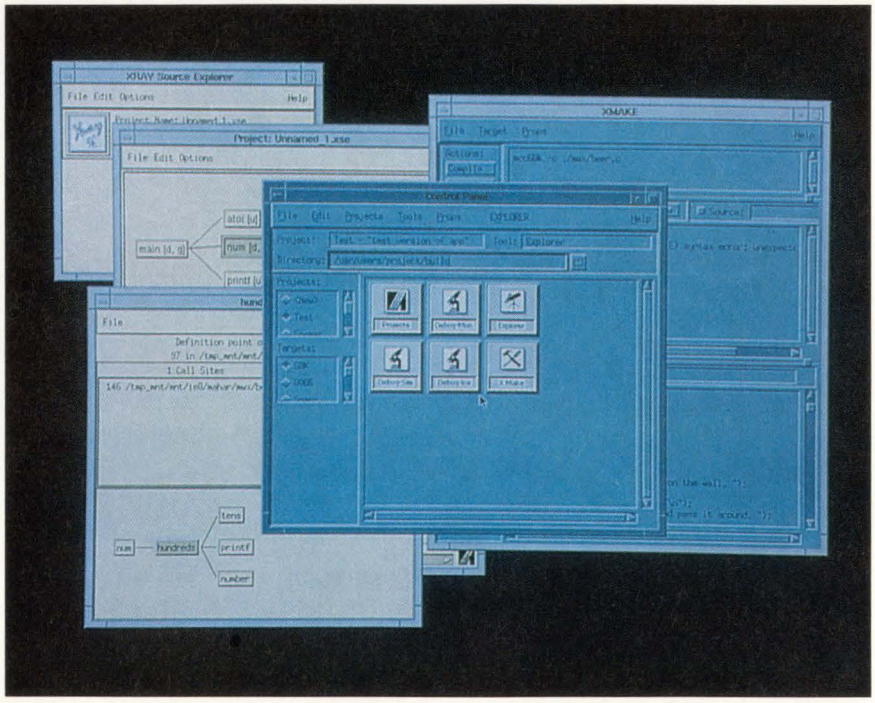
At present, Microtec is working with certain value-added resellers, giving them the messaging protocol to help them integrate their products. Applied Microsystems (Redmond, WA), for example, is working on integrating its in-circuit emulation tools into the MasterWorks environment.

You interact with the system via the XRay control panel, which lets you set up a project and working environment. The control panel is more than a graphical user interface; it lets you select tools, working directories, project-specific source files, and make files to establish the context in which you'll be working. It's possible, for example, to bring frequently used commands that may normally be hidden in a menu onto an on-screen button for easy access. It's also possible to save different contexts for different projects.

The control panel doesn't currently support version control, however. The level of project control provided involves setting up which files are associated with a given project, launching tools and setting up directories, so eliminating many repetitive steps when starting a session.

Microtec has integrated its widely used XRay source- and assembler-level debugger into MasterWorks, along with its relatively new Source Explorer navigation tool. Source Explorer graphically displays a program's calling structure, its function definitions and specific function calls. Integrating Source Explorer with the XRay debugger lets you graphically control program execution at the function level via the graphical program structure display.

Each box in the call tree represents a function and contains information on whether that function is global or local; clicking on a box with the mouse brings up this information. It's possible to display the



The XRay MasterWorks control panel can support different project configurations that can then be launched using buttons in a window. Among the tools supported in the initial release is Source Explorer (lower left), which shows a butterfly graph of a function with its calling functions and the functions called by it.

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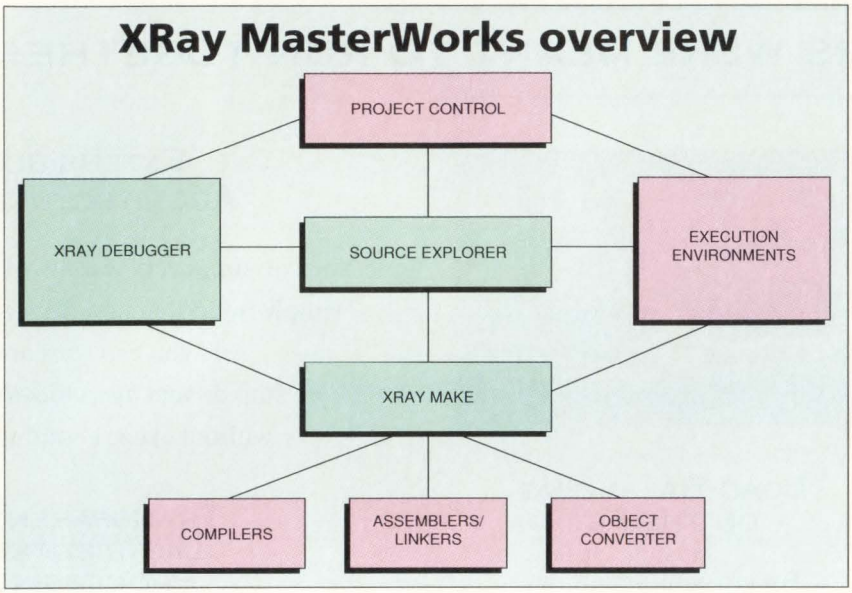
SOFTWARE & DEVELOPMENT TOOLS



XRay MasterWorks integrates functions to aid the edit-compile-debug process and to automate the tedious tasks of program building. Control of a project takes place through a window panel that defines tools to be launched, modules in the project, files, and directories. Tools communicate point-to-point to let you easily find your place in large volumes of code.

whole calling tree of a program, or a limited view in the form of a butterfly graph, showing the callers of the function of interest and the functions it calls. Double-clicking on a function box takes you into the source code.

When the XRay debugger and Source Explorer are running together, program execution can stop at a breakpoint set in the debugger to let you browse through the function definition and control program execution from the function level using debugger commands. This lets you zoom in on problems in one integrated environment, from the structural level down through the source and ultimately to the assembly level.

Automated program building

Program building is automated by the XRay Make tool, which is based on UNIX's make(1). This compatibility lets you use existing make(1) files under MasterWorks without modification. Make also identifies build errors and displays the offending source code lines in a window for quick editing.

XRay MasterWorks gathers a suite of cross-development tools for a range of different CPUs and MPUs. These include ANSI C and C++ cross-compilers, assemblers and linkers. There's also a set of C++ class libraries. In addition, the environment supports instruction-set simulators that can be used with the debugger and Source Explorer before target hardware is ready; they can yield information down to the detail of cycle counts.

Finally, there's an object format converter that can convert the output of the Microtec tools and compilers into forms usable by logic analyzers, emulators and PROM programming devices. These include IEEE-695, common object file format and Intel OMF-86. ■

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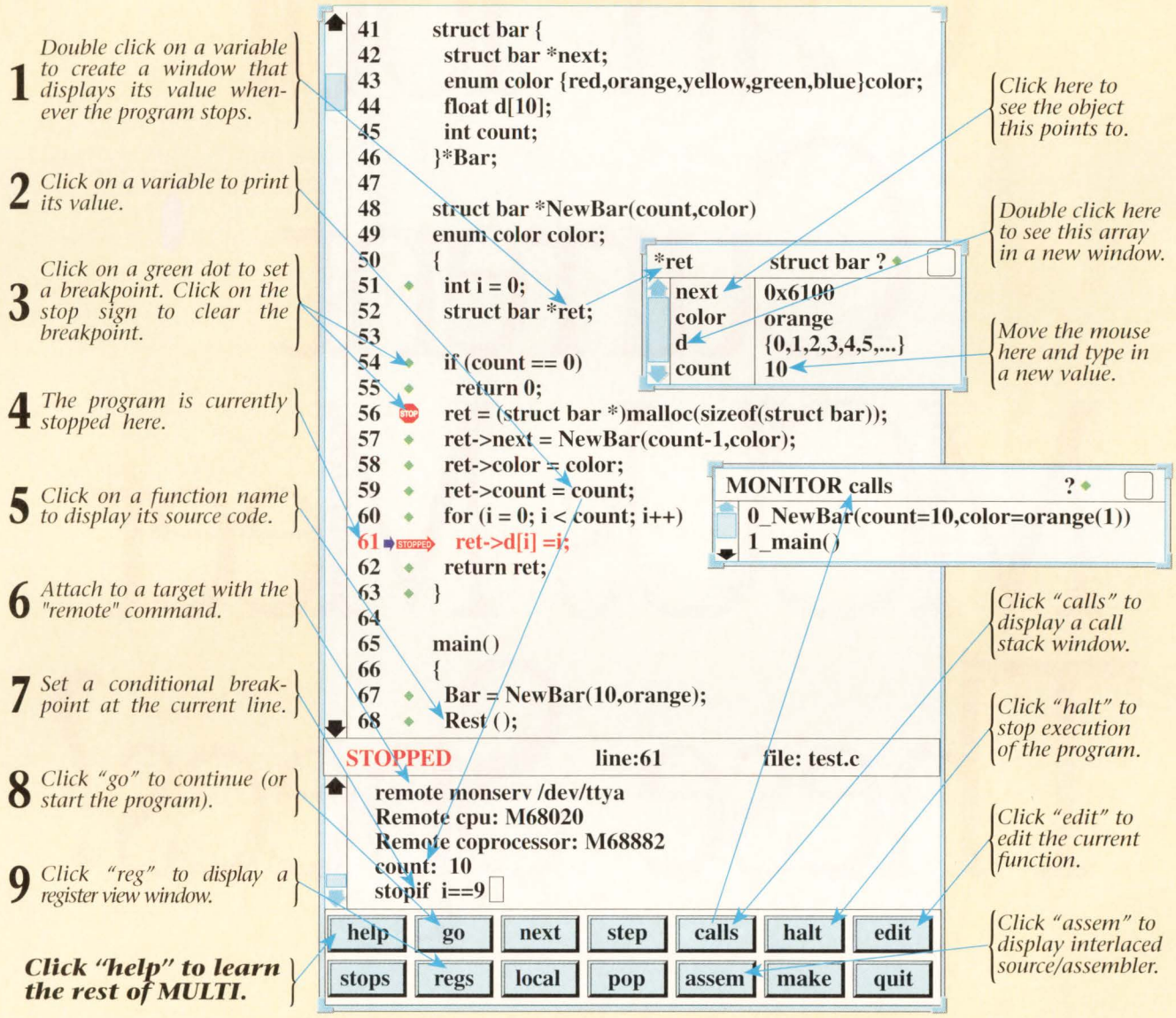

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CIRCLE NO. 32

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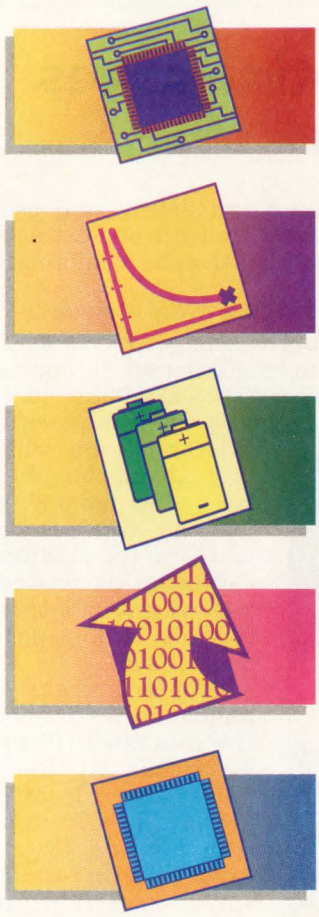

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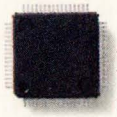

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Powerline spread-spectrum modulation saves copper in LANs and control systems

Don Tuite, Senior Editor

A building's electrical power wiring is an attractive medium for data communication. This is because such wiring, unlike dedicated runs of coaxial or twisted-pair cable, is already in place, so that if the network is ever reconfigured, it won't be necessary to lay more cable. It's even more attractive for industrial control than it is for office LANs, because it connects to most of the devices that have to be controlled, such as lights, chillers and motors.

Unfortunately, those same lights and motors make power wiring a difficult transmission medium for either office or industrial communication. Signals above a few hundred kHz are attenuated by tens of dB, changing loads cause ground bounce in the neutral wire, and fluorescent ballasts and thyristor-based controllers create severe noise.

In the past, attempts have been made to run data at low baud rates over powerlines, with the best-known efforts focusing on remote meter reading. None of these attempts has resulted in widespread commercial success, but a new approach is being pioneered by a pair of companies using spread-spectrum techniques so that narrow-band noise can't interfere with data transmission.

"Facing an assortment of light dimmers, fluorescent ballasts and electric motors, a data packet exists in a hostile environment on the powerlines," reminds Echelon's director of engineering, Tom Tormey (left). Senior engineer Philip Sutterlin and hardware design engineer Amy Hurlbut document the struggle with scope and spectrum analyzer.

Two companies, two approaches

The two companies currently shipping products for spread-spectrum powerline communications are Echelon Corporation (Palo Alto, CA) and Adaptive Networks (Cambridge, MA). Echelon's modules are new elements in its established product line—a complete, distributed-intelligence industrial control system.

Spread-spectrum modulation is usually thought of as an RF data-transmission technique. To date, the most celebrated use of such modulation has been in the U.S. global positioning system (GPS) satellite network. The same techniques, however, that communicate the ephemerides of navigation satellites to a tank commander in Iraq can be used to access a file server on an office LAN.

Spread-spectrum is essentially immune to narrow-band interference, and the effective sensitivity of spread-spectrum detectors is extremely high. To apply spread-spectrum modulation, you use a known pseudo-random bit sequence to frequency- or phase-shift-modulate a carrier. The data is encoded on the pseudo-random sequence by either shifting or not shifting the phase each time the sequence repeats, using an NRZ (non-return-to-zero) format. A correlator at the receiving end detects the pseudo-random sequence and extracts the data from the phase information.

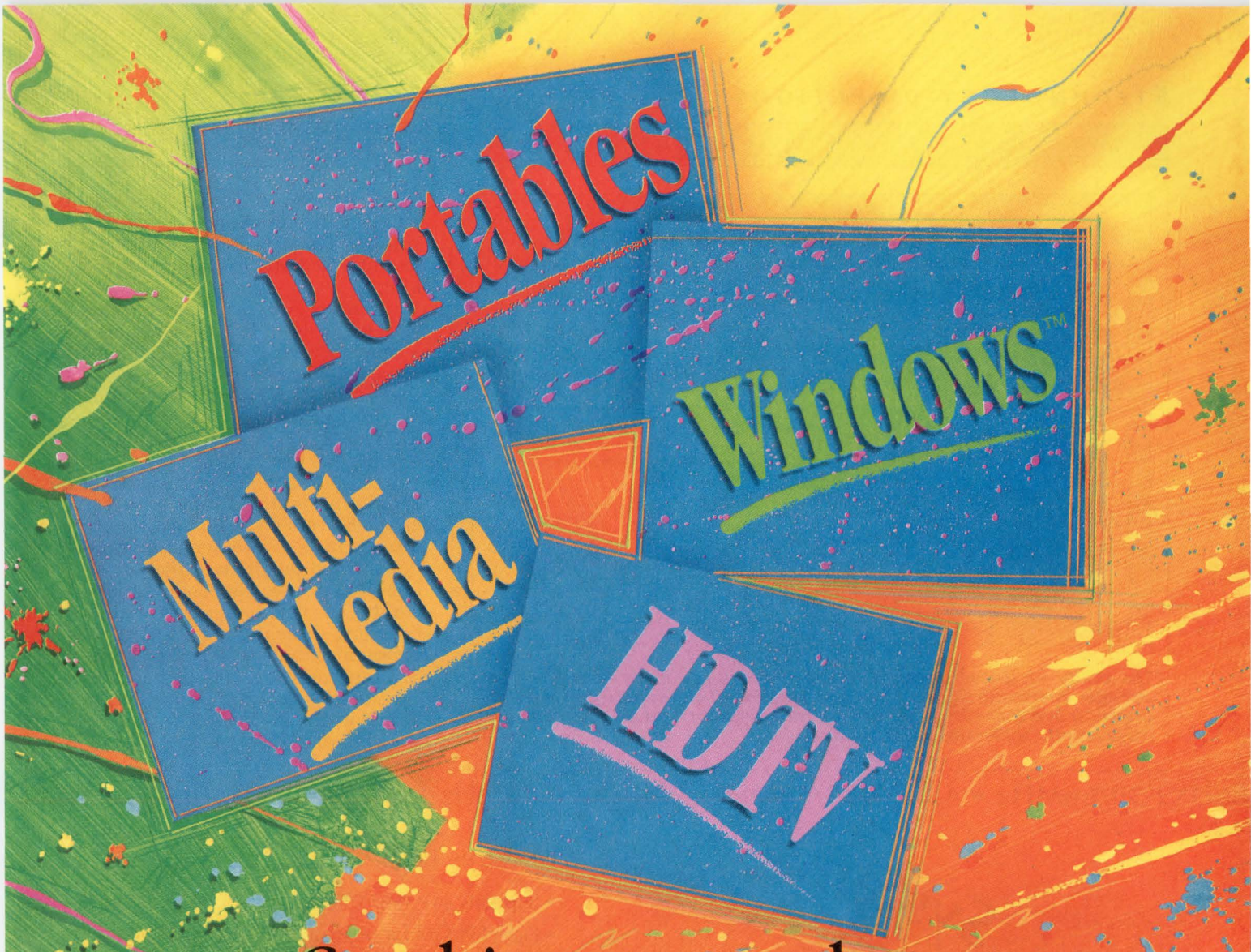
Chipping away at data

Adaptive Networks' strategy is more broadly based, encompassing LANs and WANs in addition to industrial controls. Of the two companies, Echelon is more willing to talk about the physical layer of its protocol, while Adaptive Networks tends to treat its modulation techniques as proprietary, preferring to talk about its flexible token-passing data protocol.

Echelon's transceiver communicates at an effective data rate of 10 kbits/s. According to the company's director of engineering, Tom Tormey, the transmission technique used is direct-sequence spread-spectrum, at 31 chips per bit. (A chip is the narrowest pulse width in the encoding pulse sequence that can be used to represent a bit. The number of chips per bit used in a spread-spectrum encoding scheme represents a trade-off between the degree of spectrum spreading and the bit rate.)

If the modulating pseudo-random sequence consists of a simple series of square pulses, the distribution of harmonics in the frequency domain is a $|\sin x/x|$ pattern. Echelon's engineers have trimmed the modulating signal to provide an essentially flat distribution within the required frequency band, with a rapid rolloff at the upper end.

This was necessary because, in the United States, the spread-spectrum signal must fit between 100 and 450 kHz. The 100-kHz limit is set by practical considerations, because powerline noise increases dramatically below that. The upper limit reflects an FCC require-



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256K x 4	Fast Page Mode/Block Write	MT42C4256*	70,80,100	ZIP, SOJ	Now
128K x 8	Fast Page Mode/Block Write	MT42C8128*	70,80,100	SOJ	Now
256K x 8	Extended Data Out/Block Write/Programmable Split	MT42C8256	70,80	SOJ, TSOP	Now
256K x 8	Fast Page Mode/Block Write	MT42C8255	70,80	SOJ, TSOP	Now
256K x 8	Fast Page Mode/Block Write/ Dual Write Enable	MT42C8254	70,80	SOJ, TSOP	Now
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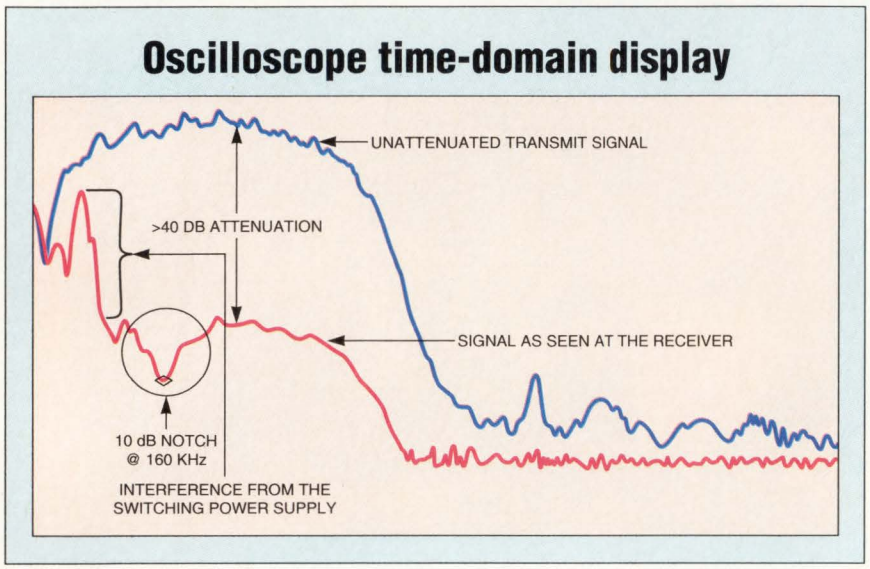

The utility of spread-spectrum communications lies in its immunity to much stronger interfering signals. This representation of an oscilloscope's time-domain display shows the voltage amplitude of a fluorescent light ballast's noise burst as it apparently obliterates a received signal.

ment that powerline signals not interfere with AM broadcasting, which starts at 535 kHz and typically uses an intermediate frequency of 455 kHz.

In Europe, where long-wave radio stations go down to 150 kHz, there's a band between 9 and 95 kHz that's set aside for utility-related applications, such as remote meter reading and load shedding. Using this band, Echelon's 31-chips/bit encoding scheme yields 2 kbits/s.

In a practical system, each of Echelon's Neuron Chips (one per node) delivers 55 to 60 packets per second. To deal with dynamic variations in the condition of the powerline, the transceiver module incorporates an oversampling correlation filter and an adaptive bit timing recovery algorithm to synchronize instantaneously to incoming packets.

If an error occurs, packet reconstruction is faster than packet retransmission. Classical methods for

error correction add more bits than Echelon's proprietary error-correction method, which requires only 6 percent overhead.

Another approach

Adaptive Networks, pursuing its goal of a full data communications network running over powerlines, achieves a 19.2-kbit/s data rate with an error rate of 10^{-9}. The system supports a range of network options and can address over 64,000 nodes. Maximum range is 4 km.

In its data link layer, Adaptive Networks decomposes messages into short frames with error correction. It uses forward error correction, as well as error detection; each frame must be acknowledged before the next is sent.

Where Echelon employs a contention-based protocol, Adaptive Networks uses token passing. Marketing manager Eric Hughes says, "This technique avoids problems that can occur when nodes fail to detect collisions, provides deterministic access to the network under heavy loads, and makes it easier to verify that a destination node is on the network."

Because Adaptive Networks sees a market in industrial control, as well as in workstation-based WANs and LANs, it's interesting to compare its data-layer protocol approach to Echelon's. In contrast to PC-based LANs, industrial control networks can have a large population of nodes with light data loading. In such cases, passing tokens to nodes that have nothing to say wastes time. Adaptive Networks' solution is to switch between static token passing and a dynamic scheme.

The decision to switch between schemes depends on network utilization. In the dynamic phase, which is used when utilization is light, nodes join and leave the logical ring based on whether or not they have anything further to transmit. There's a randomized start-time delay to prevent several new nodes from trying to join the ring at once.

Echelon offers complete control modules, including its distributed-intelligence Neuron Chips, as well as bare transceiver modules. The data interface is optimized for the company's proprietary Lonworks architecture, which includes a control-oriented development environment.

Adaptive Networks' powerline communications module has a more conventional RS-232-style data interface. The two-chip ASIC set is also available by itself. ■

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ASICs & ASIC DESIGN TOOLS

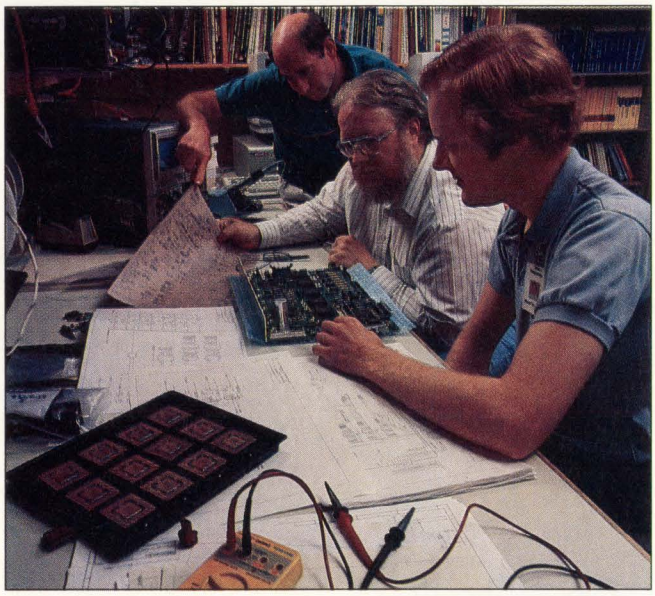
Vendors vying for FPGA market try different strategies

Barbara Tuck, Senior Editor

The use of FPGAs is growing explosively, forcing veteran programmable logic vendors to enhance performance with new-generation products. At the same time, more semiconductor giants are being tempted to enter the field.

Only Xilinx (San Jose, CA), however, is backing its boasts with production silicon. This month the company debuts all five members of its SRAM-based, 0.8-mm CMOS XC3100 FPGA family. The new devices take aim at the current speed leaders, antifuse-based PASICs from QuickLogic (Santa Clara, CA), themselves due to be ported to the Cypress Semiconductor (San Jose, CA) 0.65-µm CMOS process. At the same time, Altera (San Jose, CA) is selectively sampling the first members of its new SRAM-based, 0.8-µm CMOS FLEX 8000 family. And Actel (Sunnyvale, CA) is revealing additional performance numbers as its antifuse-based ACT 3 family goes through process characterization in Hewlett-Packard's 0.8-µm CMOS process.

Intel (Santa Clara, CA), meanwhile, will officially enter the FPGA market next year when it samples its 0.8-µm CMOS EPROM FLEXlogic family with SRAM option, and Motorola (Phoenix, AZ) announced a few days ago that it has concluded a licensing agreement with UK-based Pilkington Microelectronics Ltd. for its fine-grained, dynamically programmable logic device technology. In so doing, Motorola has followed the lead of GEC Plessey Semiconductors and Toshiba.



Examining a prototype of a color printer board are Rod Odenheimer, design engineer; Howard Goetz, hardware design manager; and Dave Knierim, principal engineer, all of Tektronix's Graphics, Printing and Imaging Division. According to Goetz, with the Xilinx 3190, Tektronix "got more than a 2x speed improvement with no resimulation or changing download files."

Faster with plug-in parts

With a process more performance- than density-oriented, Xilinx has doubled the speed of its earlier devices without burdening users with a new architecture or software changes. By making its XC3100 family pin- and software-compatible with 1,300- to 5,000-gate XC3000 devices, the company makes it possible for users such as Howard Goetz to make direct plug-in replacements for higher speed. Goetz, hardware design manager at the Graphics, Printing and Imaging Division of Tektronix (Wilsonville, OR), was using a Xilinx 3090 for memory management in a printer product and running it right at the end of its speed margin when he received a beta sample of the 3190 from Xilinx. "I plugged it right into the system," he says, "and got more than a 2× speed improvement with no resimulation or changing download files."

Goetz says he can't testify firsthand about the validity of the Xilinx claim that its new parts run at 50- to 80-MHz system speeds, because his system processor runs at only 32 MHz, but he adds that he doesn't doubt the 3100 parts can run at speeds greater than 70 MHz. The critical-path challenge Goetz faced was a long accumulator that stretched through seven configurable logic blocks. "I can operate with one wait state now rather than two," he reports.

SRAM switches vs antifuses

With the introduction of its new parts, Xilinx also claims to have unseated QuickLogic as the FPGA speed leader. System speeds of 50 to 80 MHz prove, says Xilinx, that you don't have to go to exotic antifuse-based processes for high performance. FPGA architectures that use antifuse elements as programming switches are much more difficult to scale, according to Xilinx, than SRAM-based FPGAs that use transistors as switches. In going from 1 µm for its 3000 devices to 0.8 µm for its 3100 devices, Xilinx says it's cut interconnect element parasitics in half. And while today's antifuse architectures have limited buffering, resulting in significant variations in delay depending on fanout, Xilinx logic blocks have large output buffers that eliminate most fanout dependency.

To prove its point about variation in delays due to fanout, Xilinx gives path-delay elements from pin to pin for 3100 parts as compared to QuickLogic PASICs. The figures show that the 3100 family can achieve 9- to 11-ns pin-to-pin delays, almost independently of internal fanout, whereas QuickLogic delays increase substantially with high fanout. QuickLogic president and CEO David Laws counters this by noting that with the asymptotic waveform evaluation (AWE) technique, you can use QuickLogic's PASIC toolkit to selectively program heavily loaded paths to be 20 to 25 percent faster than indicated by the high fanout figures given by Xilinx.

Toward better benchmarks

Xilinx also uses JEDEC benchmarks to illustrate a speed advantage over QuickLogic. Pin-to-pin delay for a 9-bit parity circuit implemented in a

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Path delay elements (ns)

Xilinx XC3100		Speed grade	Input delay	Logic block delay	interconnect delay	50-PF output delay	Total Delay
Fanout = 1	Shortest path	-3	2.2	2.7	0.5	3.3	8.7
	Typical path	-3	2.2	2.7	0.5	3.3	11.7
Fanout = 8	Shortest path	-3	3.2	3.7	0.5	3.3	10.7
	Typical path	-3	3.2	3.7	3.5	3.3	13.7
QuickLogic pASIC 1							
Fanout = 1	Shortest path	-2	2.9	4.5	0.0	4.9	12.3
	Typical path	-2	2.9	4.5	3.0	4.9	15.3
Fanout = 8	Shortest path	-2	6.9	10.4	0.0	4.9	22.2
	Typical path	-2	6.9	10.4	3.0	4.9	25.2

With its XC3100 family, Xilinx claims to have unseated QuickLogic pASICs as FPGA speed leader, giving as proof these comparative path-delay figures, which show significant variations in QuickLogic delays depending on fanout. With the application of the asymptotic waveform evaluation technique to selectively program heavily loaded nets, pASICs will run 20 to 25 percent faster than these figures indicate, according to QuickLogic president David Laws. (Interconnect delays for typical paths are estimated at an additional 3 ns for both manufacturers.)

3100, for example, is 12.9 ns, a 39 percent improvement over a pASIC's 21-ns delay. Specific benchmarks can be selected to prove a competitive point, responds Laws. "QuickLogic did the 9-bit parity plus other JEDEC benchmarks to illustrate density, not performance, in response to a specific user's request. For demonstrating performance, the PREP benchmarks, when they're available, will be much better," he adds.

In the meantime, the semiconductor benchmark group called PREP, for Programmable Electronics Performance, is due to have its first ballot on a list of proposed benchmarks that will help you compare various FPGA architectures. After review, the benchmarks will go through a check-and-balance process among FPGA makers before approval and endorsement by the PREP group. A proposed datapath benchmark standard, prepared by QuickLogic and issued by PREP as an example of the

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CIRCLE NO. 37

data reporting format under consideration, shows a QL12X16 PASIC fitting 12 benchmark units and performing the required function at a worst-case speed of 143 MHz. To illustrate the speed of its 3100 devices, Xilinx has published its own preliminary benchmark results, not yet approved or endorsed by PREP. For a 16-bit prescaled counter implemented in an XC3190, for example, results show the Xilinx part fitting 13 benchmark units and performing at 99 MHz.

According to Laws, QuickLogic retains its position of speed leader. "We're still in a 1.2-µm process," he says, adding that he anticipates a speed improvement of 20 to 25 percent for QuickLogic PASICs when ported to Cypress Semiconductor's 0.65-µm process. Under the QuickLogic/Cypress agreement, Cypress will be a source for QuickLogic PASICs, spanning densities from 1,000 to 20,000 usable gates and beyond. The first product available will be a 4,000-gate PASIC in a high-pin-count package. Laws expects die size to decrease dramatically—perhaps by as much as half—to make PASICs cost-competitive. Samples will be available the first half of next year.

Interconnect impedance

What about Xilinx's claim that the RC delay in antifuse-based processes doesn't consistently decrease when a process migrates to finer device geometries—and that the resistance and capacitance in the antifuse-based Actel devices haven't budged since Actel introduced its very first device? QuickLogic's Laws counters that when PASICs are scaled to 0.65 µm, the resistance (determined by the impedance of the antifuse) will be about the same, but capacitance should go down significantly. In addition, with AWE techniques, the resistance of ViaLink interconnects in the most heavily loaded nets can be reduced to less than 50 Ω.

Warren Miller, Actel's product planning and applications manager, says that his company has indeed improved interconnect impedance in each product generation. In fact, for the forthcoming 0.8-µm, 1,000- to 10,000-plus-gate ACT 3 devices, the interconnect impedance is 200 Ω and 6 fF, vs 500 Ω and 16 fF for the 2-µm ACT 1 devices.

Another delay factor is the number of antifuses or switches a signal must travel through to get from source to destination. By making architectural changes, Miller says Actel has reduced clock-to-output time from 30 ns in the ACT 1 family to 10 ns for the ACT 3 family. And still another indication of performance improvement is logic module speed, which Miller claims has been reduced from 5.4 ns in ACT 1 to 3 ns for ACT 3.

Deterministic delays

For the interconnects in its new SRAM-based, register-intensive Flexible Logic Element MatriX, or FLEX,

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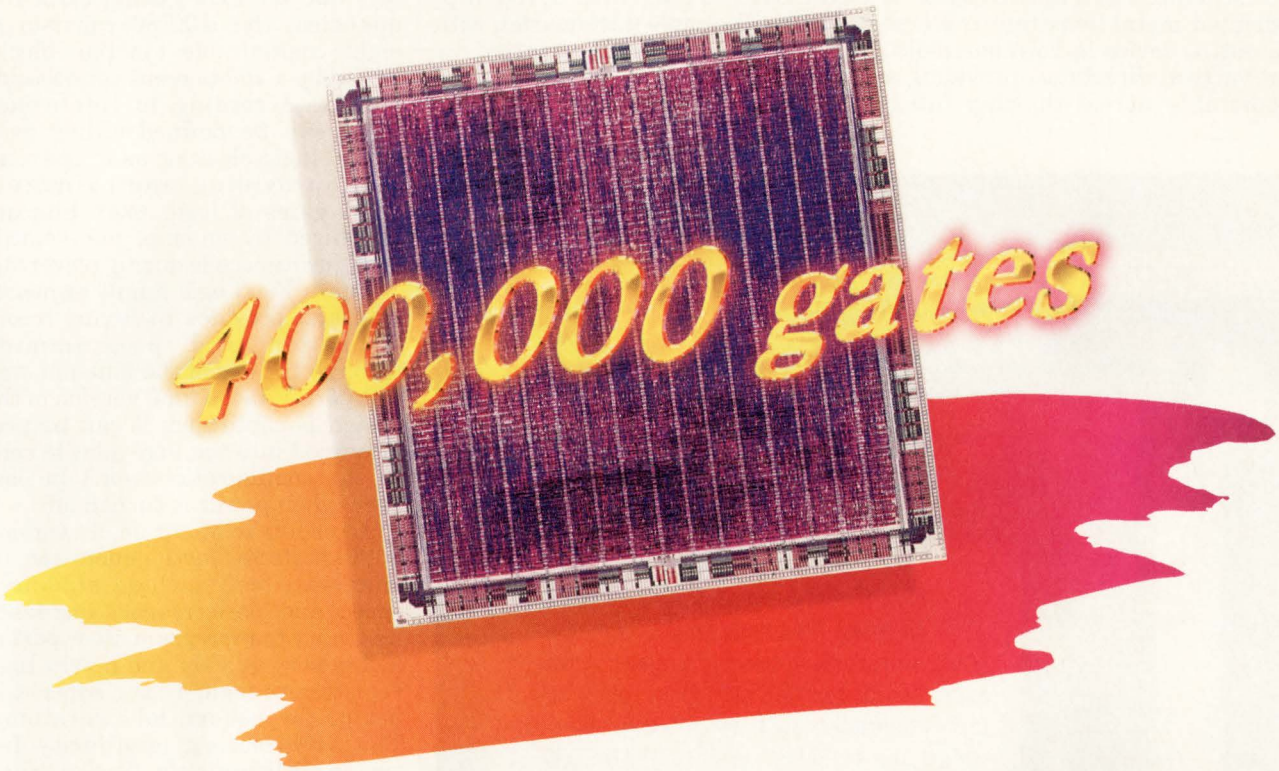

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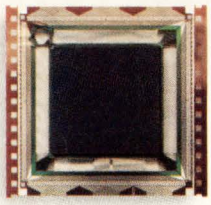

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8000 family of parts with 4,000 to 24,000 usable gates, Altera is using what it calls the FastTrack interconnect scheme. FastTrack consists of dedicated metal lines that traverse the entire device in both horizontal and vertical directions, providing a predictable across-the-chip interconnect delay of 9 ns. With 70-MHz in-system performance, the first of the new devices, the 12,000-usable-gate EPF81188 (with 1,188 flip-flops) will sample next quarter, with production quantities expected by the second quarter of next year.

Intel is readying the first of its EPROM-based family with SRAM option for first-quarter sampling. With deterministic 10-ns pin-to-pin delays and 80-MHz system clock frequencies, the iFX780 consists of eight configurable function blocks linked by a 100-percent-connectable matrix. According to Intel, each block can be defined either as a 24V10 logic block or as a 128 × 10 SRAM, providing approximately 5,000 gates of logic. SRAM bits are initialized by on-chip, non-volatile configuration cells during power-up.

Intel's FlexLogic family supports JTAG and provides in-circuit reconfiguration and programming through the use of the four-pin JTAG test port. When a final version of the design is confirmed, it can be programmed into the non-volatile cells so the configuration won't be lost even when power is turned off.

According to Motorola, its version of Pilkington's fourth-generation architecture will include enhanced speed and performance, increased flexibility to reprogram all or part of a chip very quickly and a very high registers-to-logic ratio, especially useful for sequential operations. The architectural similarity between Pilkington's fine-grained FPGAs and Motorola's metal-programmed gate arrays is expected to facilitate migration from FPGAs to gate arrays. Initial sampling of Motorola's 0.8-µm FPGAs, likely at the 5,000 and 10,000 usable-gate level, is expected in the fall of next year. ■

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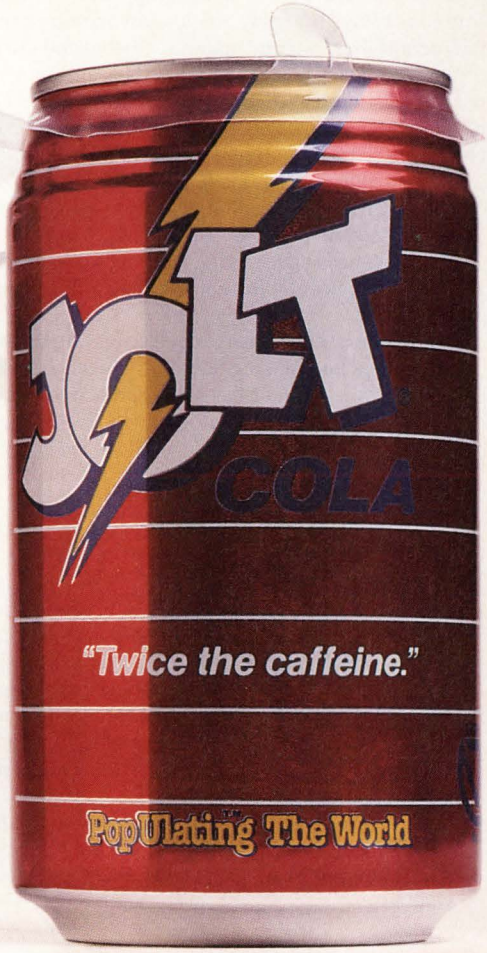

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ECC differs from other industry events because it focuses on providing solutions for a variety of embedded computer applications rather than focusing on technology alone or products alone. Developing these applications and finding the best solutions brings into play single-chip microprocessor and microcontroller implementations; custom and semicustom board designs; standard bus-based single-board computers and peripheral boards; operating systems, real-time kernels and compilers; development systems and debugging tools; embedded PCs, embedded workstations and even embedded microcomputers.

ECC attendees are intimately involved in the design, development and integration of a broad range of products and systems based on embedded computers.

ECC attendees are working in all major industries, where they are designing, developing and building a full spectrum of products and systems.

- In the computer industry, developing workstations and larger computers and making decisions about proprietary buses, open architecture buses or bus-less approaches.
- In process control and automation, developing systems for motor control, process measurement and control, machine vision, robotics and manufacturing automation, traffic control, etc.
- In communications, developing systems for use in cellular communications, PBXs, multiplexers, local area networks and wide area networks, etc.
- In the military/aerospace and avionics industries, building equipment and systems for communications, command and control (C3), weapons guidance and control, simulation, air-borne and ground-based flight-control systems, etc.
- In the test, measurement and instrumentation industry, where equipment and systems are being built for product testing, maintenance and service applications, diagnostics (including medical), resource exploration, etc.
- Research and development, where scientists and engineers are designing equipment and systems for data acquisition, analysis and simulation that range from benchtop systems to space stations.

THE PROGRAM

ECC's technical program has been designed to provide attendees with the practical information they need to incorporate embedded computers in an end product or subsystem. These embedded computers can take the form of dedicated microcontrollers; sophisticated 32-bit CISC or RISC processors; off-the-shelf or customized SBCs; standalone SBCs; standard bus-based subsystems; or OEM workstation, desktop or industrial computer platforms.

While the Technical Program Committee will entertain proposals for presentations covering a broad range of embedded computer approaches, special consideration will be given to proposals dealing with the following major areas of concern:

SYSTEM ARCHITECTURES

Presentations in this category will deal with interprocessor and memory architectures, custom and semicustom system implementations, and loosely and tightly coupled software and hardware models. This section will include a discussion of chip sets for "standard-architecture" machines such as the X86-, SPARC- or MIPs-based workstations and the features that make them suited, or unsuited, to embedded applications. Some other areas of interest are:

- PCs (80X86, P5) in embedded applications
- RISC architectures (Alpha, HP-PA, MIPS, SPARC, 88K) in embedded applications
- Integrating processor, memory and I/O on stand alone SBCs
- Memory architectures with or without cache
- Symmetrical and asymmetrical multiprocessing
- Live-insertion, fault-tolerant, high-availability computing

INTERFACES AND STANDARDS

This track will deal with local on-board interfaces, addressing issues such as architectural considerations, transceiver considerations (cost, power, space, time-to-market) and implementations, current and emerging standards such as PCI and PCMCIA as well as more conventional mezzanine-I/O buses such as IndustryPacks, SBus, MX bus and others. Particular areas of concern include:

- Standard mezzanine/daughter boards
- SBus, TURBOchannel and other workstation I/O buses
- 80X86 (P5) peripheral interfaces
- Networking interfaces such as Ethernet, ATM and SONET
- Peripheral interfaces such as SCSI, HiPPI, and FiberChannel
- MCM standards and interprocessor module buses

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INTERCONNECT ARCHITECTURES

The approaches to interconnecting board-level subsystems are undergoing a revolution, including the development of new standards such as PC/104, SCI (Scalable Computer Interface) and Futurebus+, as well as major changes and enhancements to such well-established standards such as VME and Multibus II.

In addition, there are many other approaches vying for the embedded market such as ESP (Extra Small Package), various STD approaches, G64 and others. Rapidly changing semiconductor technology is forcing changes in bus and interface technology which are reflected in:

- VMEbus, Multibus, Futurebus+, STD/STD32
- Custom and semicustom implementations
- High-performance backplanes
- Bridges and intercrate communications

SOFTWARE AND DEVELOPMENT TOOLS

Because embedded computer applications involve real-time processing, the major software focus of ECC will be real-time issues. Special emphasis will be given to multiprocessing in real-time using both traditional and Windows-based operating systems. Also of interest to attendees are:

- Real-time OS and kernels
- Real-time DOS
- Windows for embedded and real-time applications
- Multiprocessing with DOS and other real-time OSs
- High-performance optimized compilation
- POSIX and POSIX compatibility
- Communications protocols/standards
- Ada in military and nonmilitary applications

Proposals will be considered for presentations on any of the above topics, as well as on any other topics related to the design, programming and application of embedded computer products, subsystems or systems.

THE FORMAT

A combination of one-hour presentations, application-focused multi-paper sessions and tutorials will address a broad range of topics of importance to engineers and engineering managers designing both the hardware and software for embedded computers and subsystems.

- Tutorials are extended presentations intended to provide attendees with an in-depth understanding of core technologies used in embedded computers.
- Individual presentations are focused on various aspects of applying new or emerging technologies and products to solving specific problems in designing products or subsystems using embedded computers. Special consideration will be given to presentations that emphasize make-or-buy trade-offs in specific applications.
- Multipaper sessions consist of several shorter papers that focus on the implementation of embedded computing in specific application areas, including:
  - Medical instrumentation
  - Vehicular traffic control
  - Signal processing/data acquisition/DSP
  - Automated vehicles
  - Machine control
  - Graphics
  - Low-power and portable applications
  - Imaging
  - Visual inspection
  - Virtual reality
  - Military C3I
  - Communications
  - Peripheral interface and control
  - Process control
  - Laboratory automation
  - Multimedia
  - Networking

HOW YOU CAN PARTICIPATE

You may participate in the ECC Technical Program by submitting a proposal for either a one-hour lecture-type presentation, a 20-minute application-focused paper, or a longer tutorial. Please submit your proposal no later than November 20, 1992.

The proposal should be no longer than one page and consist of a short abstract that summarizes the content and goals of the presentation, and a brief outline of the major topics covered by the presentation. Presenters must be technically qualified and able to answer questions from attendees. A short biography of the presenter, detailing his or her technical background and accomplishments must accompany the proposal.

Acceptance of proposed presentations will be made by December 2, 1992. A complete copy of the presentation, including all visuals and graphics, for publication in the Conference Proceedings must be provided by March 1, 1993. Presentations given at ECC will be published in the Proceedings and copyright shall be assigned to Computer Design/PennWell Publishing Company.

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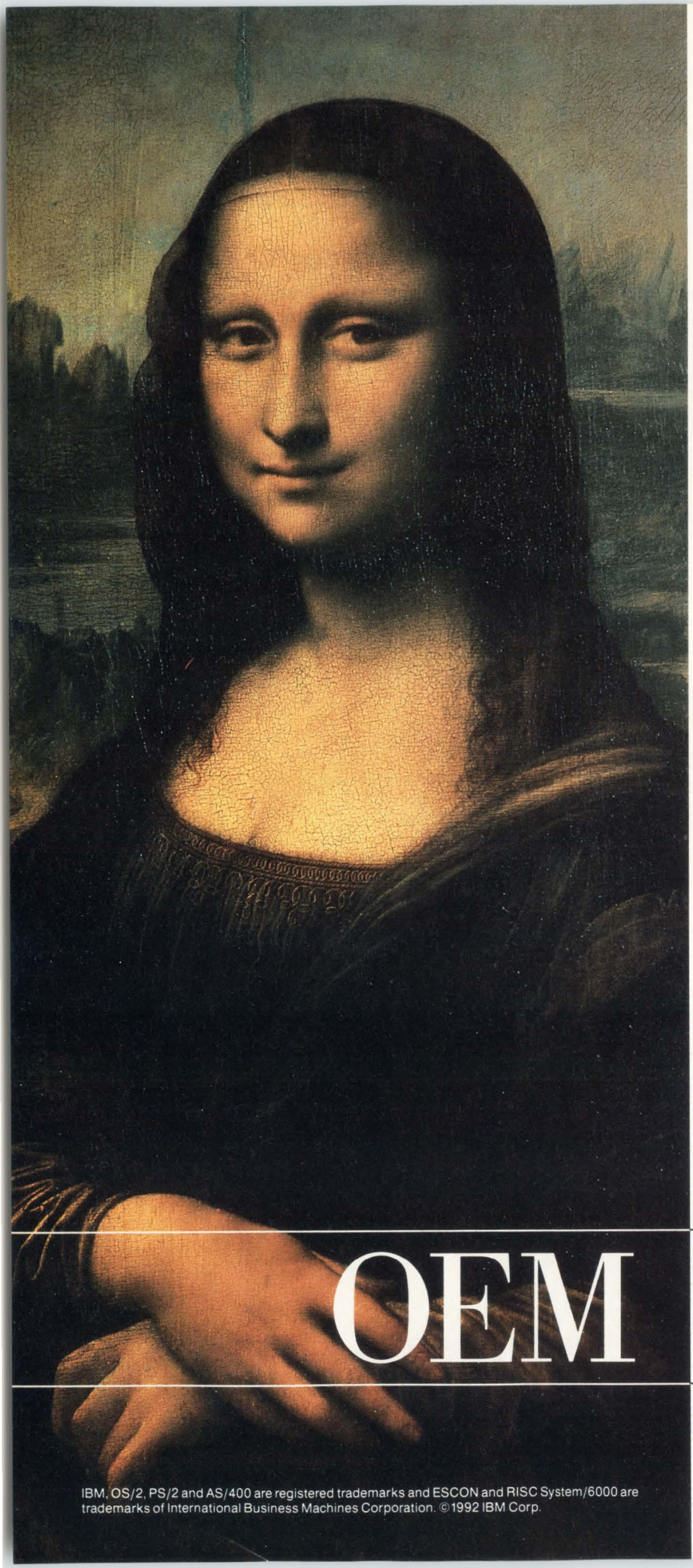

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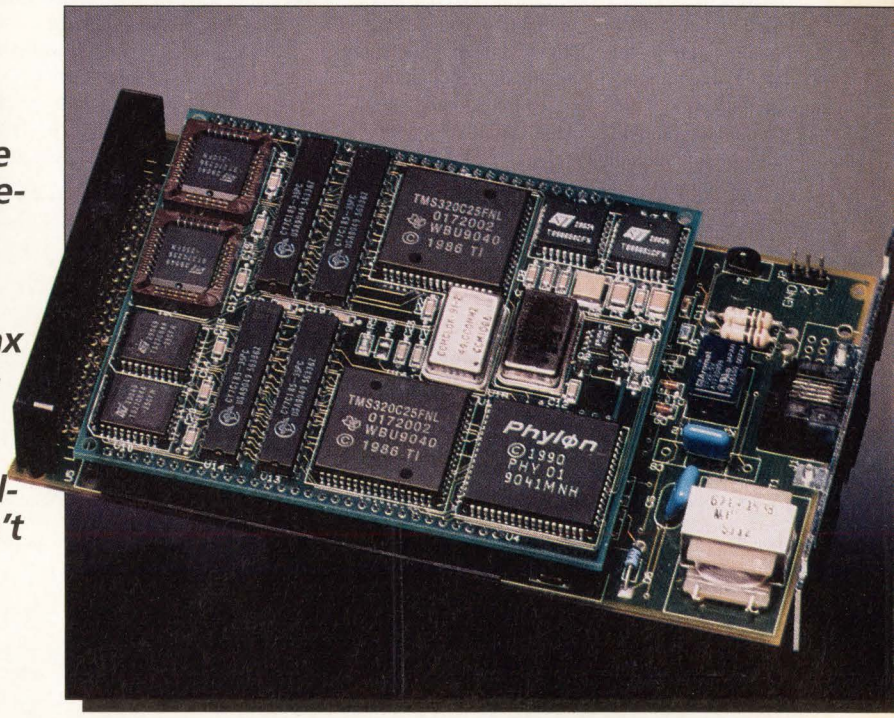
CIRCLE NO. 42

IC vendors integrate PC telecommunication services

First came fax-modem combo chips. Now IC manufacturers are attempting to integrate voice messaging and caller ID. They're thinking about color fax and video conferencing. Are there limits beyond which the technology envelope can't be stretched?

Stephan Ohr,
Contributing Editor



The HeliosCOM+ from Helios Systems is the first fax-modem combo card designed for the Sun SBus. The extra processing power of a Sun workstation speeds the page-formatting process for faxes. The use of Phylon data pumps lets modem data rates go as high as 14,400 bits/s, and supplies Group III fax capability.

There's little doubt that the desktop PC of the very near future will be a communications center as well as a data-gathering and document-publishing center. Business users will set up their PCs to send and receive not just modem data and faxes, but voice messages as well.

In certain parts of the United States, it's now possible to automatically identify the person who calls you. With the aid of Windows-based software, you can pull a file on the caller and put all relevant information (including the caller's picture) on your computer screen—even before you pick up the phone.

Data-compression techniques are on the horizon that will let PCs send and receive color images of photographic quality. In the more distant but still foreseeable future, these same techniques will bring moving video images to the desktop PC for video conferences.

What isn't clear at this point is which telecommunications media will be used to carry multiple communications services. The standard analog telephone line is optimized for a voice-frequency signal with a bandwidth of 3 kHz. With the help of wave shaping, echo cancellation and other digital signal-processing techniques, you can transmit facsimile or modem data at 14,400 bits/s—or almost five times the bandwidth of the phone line. In fact, modem manufacturers are currently developing a standard for 28.8-kbit/s data rates. In addition, it's possible for a receiver to automatically distinguish between voice, modem and facsimile calls. The receiver can also capture a dual-tone multifrequency (DTMF) signal that communicates the phone number of the call originator.

But at this point the PC-as-communications-center idea begins to break down. The call-recognition service known as caller ID is legal in only a few states in this country. Analog phone lines, moreover, don't have the band-

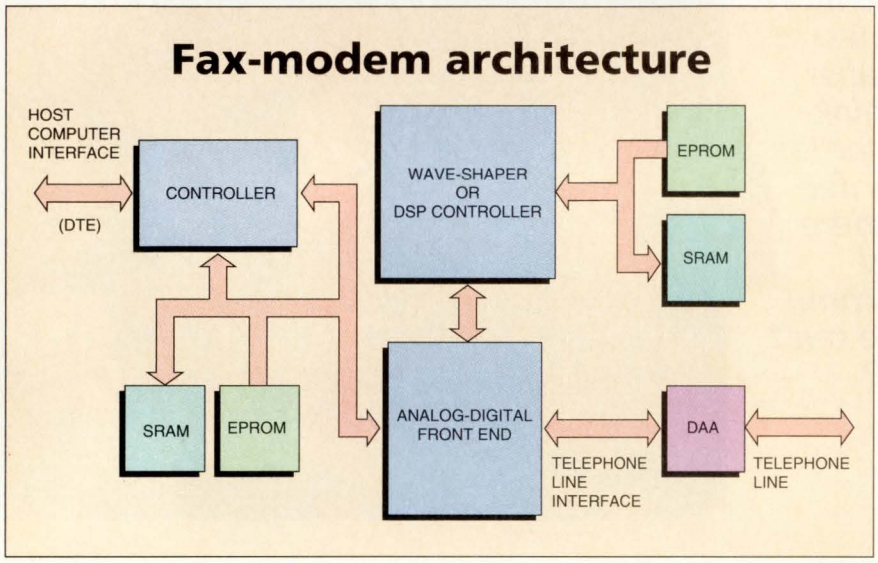
width to transmit moving video images, and compression standards aren't yet set.

Just a stepping stone

Because of these factors, it's not clear whether IC manufacturers developing multiple-service chip sets for standard telephone lines are the wave of the future; they may have taken a fork in the road which ultimately leads to a dead end. To bring in full-video service, it will be necessary to install high-bandwidth capability, which may render current investments in analog technology obsolete. The proliferation of fax-modem combo chips and boards may create, as one PC writer put it, a "Trojan horse." Mike Hogan, writing in a recent issue of *PC World*, insisted that the fax-modem insert card can be thought of as the advance wave which prepares the way for other, more dramatic possibilities. "A cheap fax-modem today is the first step toward much broader communications horizons tomorrow," he says.

The fax-modem may also be an empty promise, an instrument which offers few advantages over less integrated solutions. Early fax-modem combo cards, in fact, created certain difficulties for their users. Unlike ASCII text, which can be sent character by character from computer to computer by modem, facsimile transmission is typically page by page. To send a fax from a computer, an ASCII text file must first be formatted as a bit-mapped page in memory and then transferred, pixel by pixel, onto the phone line. Depending on the page format selected (including such factors as type fonts and graphics enhancement), formatting and sending a page can be extremely time-consuming.

Although the fax-modem board was intended to offer the convenience of one machine performing several communications functions, many early users found it more efficient simply to print out a hard copy of the text and send that piece of paper through a conventional fax machine.



Fax-modems are composed of three major building blocks: an analog-digital front end (transceiver) which interfaces with the telephone line, a waveshaper or DSP controller and a controller that interfaces the modem to the PC or host computer. Voice-compression algorithms and protocols distinguishing fax, modem and voice calls, as well as a number of other functions, are all embedded in the firmware attached to the control processor. An isolation transformer, using a direct access arrangement (DAA), ensures that faulty telephone equipment won't damage the phone line.

Software is the issue

"Much of this is a software issue," insists Greg Lang, product manager for SatisFAXtion fax-modem boards from Intel (Santa Clara, CA). "Two years ago, the software supporting fax-modem boards was just a 'viewer.' Every page you sent or received was big, fat, slow, and required a ton of horsepower to process. Now the software is much more efficient. There's even software with OCR [optical character recognition] which converts a fax image to ASCII text for editing."

According to Lang, as far as the user's concerned, the value of a fax-modem board isn't in the silicon, but in the software. Integrated fax-modem chips have little to do with page formatting and printing, so a higher telecom data rate doesn't result in faster printouts. From the point of view of the board builder, semiconductor manufacturers have made it easier for them to offer competitive products by providing devices with greater integration of functions, higher modem transmission speed and lower cost. "The current generation of fax-modem data pumps," says Lang, "is approximately 30 percent as expensive as a board, down from 60 percent just two years ago."

Integration of voice-messaging functions is something that Lang believes users will demand in years to come. Fred Kamp, director of communication products marketing at Sierra Semiconductor (San Jose, CA), agrees, pointing out that such integration will let small, home-based businesses provide the same kind of voice mail services now used by larger companies. In addition to digital answering machine services, the extra storage space and horsepower of the PC can be used to supply a menu of services to the caller, including a send-fax capability where the caller uses the telephone keypad to identify fax pages to be received.

Chip sets pull it together

Sierra's SQ3214, a four-chip set introduced last month, combines high-speed modem and fax data transceivers and voice messaging with caller ID. The XR-29V00 from Exar (San Jose, CA) is a two-chip set introduced in April that offers a complete data-pump function for Group III fax, 2,400-bit/s data, voice coding with 4:1 compression, and caller ID. During the summer, Phylon (Fremont, CA) introduced two sets of two-chip fax-modem devices, one a low-power chip set optimized for laptop computers and the other equipped for normal desktop operation. Both sets offer V.17 fax and V.32 bis modem capabilities, with data rates up to 14.4 kbits/s, along with adaptive differential pulse code modulation (ADPCM) voice compression and caller ID functions. With a firmware change, says Phylon vice-president of marketing Sid Bagwe, PHY1001/1002 chips can support the new V.Fast standard of 28.8 kbits/s, due for ratification by the Consultative Committee for In-

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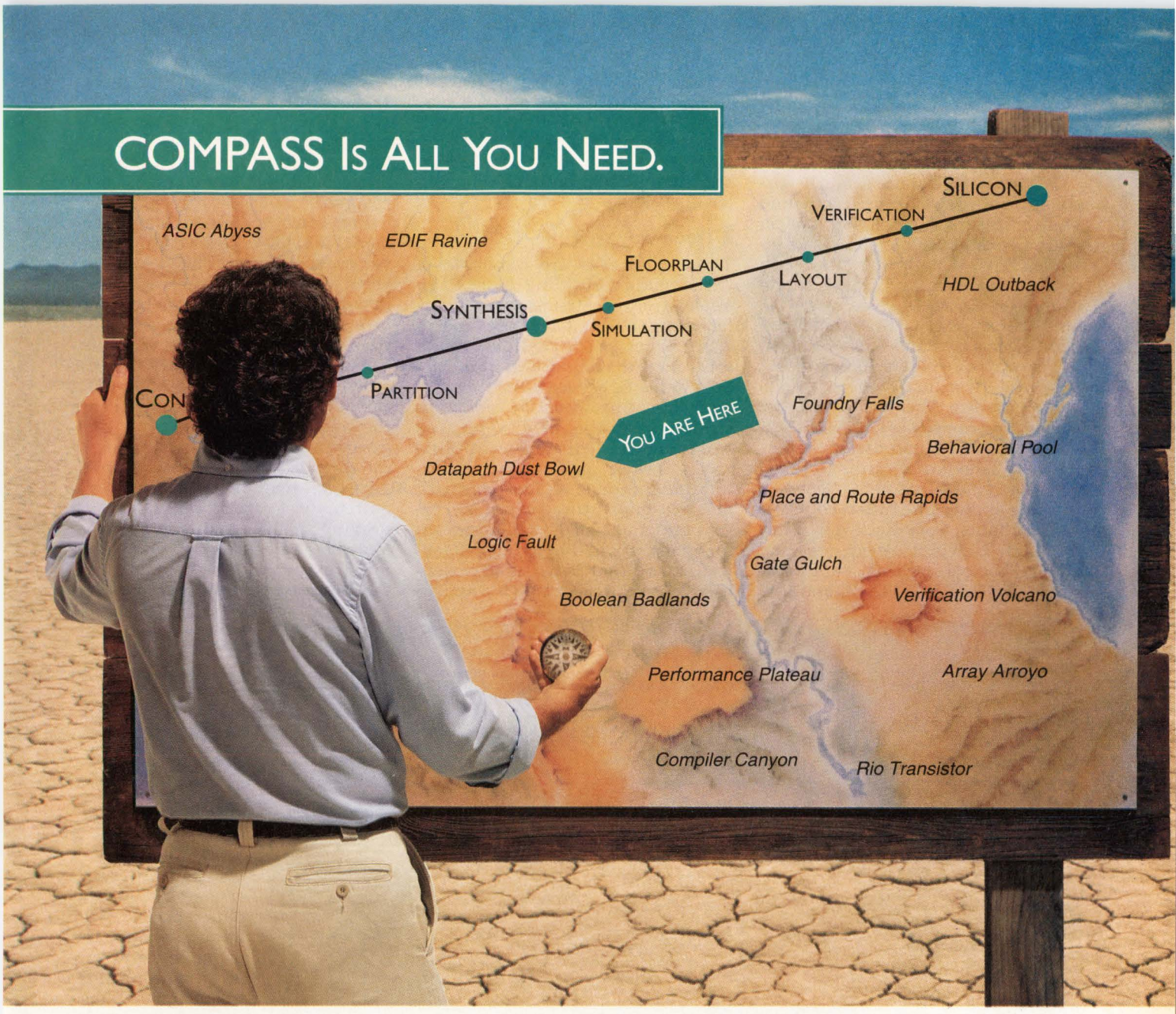

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ternational Telephony and Telegraphy (CCITT) next year.

Phylon has been particularly successful at developing front-end analog interface chips for modem and voice communications. Users include Shiva (Cambridge, MA), with its NetModem/E, and Hayes Microcomputer Products (Norcross, GA), with Ultra 144, a 14.4-kbit/s modem. Helios Systems (San Jose, CA) incorporated the Phylon chip set into the first fax-modem combo board for Sun Microsystems' SBus. The processing power of a Sun workstation all but eliminates page formatting delays that continue to exist in the PC environment.

Other highly integrated chip sets are available from Rockwell International (Newport Beach, CA) and Cirrus Logic (Fremont, CA). Rockwell's two-chip RC144ACL and Cirrus' two-chip CL-MD1424AT provide fax, modem and voice coding and compression, although not caller ID.

Three-way split

These chip sets are composed of three major building blocks: an analog front end (transceiver) interfacing with the telephone line, a waveshaper or DSP controller and a controller that interfaces the modem to the PC or host computer. The four chips introduced by Sierra include an analog front end, DSP waveshaper, dedicated controller, and interface logic. Cirrus claims full integration of all functions with just two chips—three, if you add error-correction and data-compression functions. Exar, Phylon and Rockwell's two-chip sets partition modem functions between a DSP chip and an analog-digital front end. To interface properly to the host, a separate microcontroller may or may not be required.

For voice coding, a fourth element, a voice encoder/decoder converter, is required. This device converts telephone voice frequencies into data patterns that can be stored on a hard disk; it also converts digitized messages back into voice output that can be played back over the telephone line. With most chip sets, this capability is incorporated into the analog front end. ADPCM compression algorithms are applied to the digitized voice patterns to minimize the amount of disk space required; these algorithms, along with protocols to distinguish, fax, modem and voice calls, caller ID, DTMF dialing, Hayes-type AT commands from the host computer, Microcom Networking Protocols (MNPs), and V.42 bis error correction, are all embedded in the firmware attached to the control processor.

Pumping data

A modem's analog-digital front end, typically called a data pump, is a transmitter/receiver combination that puts a basic carrier frequency onto the phone line and varies its amplitude, frequency or phase up or down to signify changes in the serial data pattern. Modems that transmit data at rates below the 3,000-Hz bandwidth of the telephone line (at 2,400 bits/s, for example) use either frequency-shift keying (FSK) or differential phase-shift keying (DPSK) to indicate changes in logic state. Modems that transmit data at rates above the 3-kHz bandwidth use DSP techniques to shape the waveform of an 1,800-Hz carrier frequency. A single

Modem standards

Standard	Fax/Data	Bits/s	Modulation	Baud rate (symbols/s)	Carrier frequency originate-M/S	Carrier frequency answer-M/S	Constellation points
Bell							
103/108/113	D	300	FSK	300	1270/1070	2225/2025	
202	D	1200	FSK	1200	1200/2400		
212A	D	1200	DPSK	600	1200	2400	4
201	D	2400	DPSK	1200	1800		4
208	D	4800	QAM	1600	1600	1800	8
CCITT							
V.17	F	14400	TCM	2400	1800		128
		12000	TCM	2400	1800		64
		9600	TCM	2400	1800		32
		7200	TCM	2400	1800		16
V.21	D	300	FSK	300	980/1180	1650/1850	
V.21 ch2	F	300	FSK	300	1650/1850		
V.22	D	1200	DPSK	600	1200	2400	4
V.22 bis	D	2400	QAM	600	1200	2400	16
V.23	D	1200 fwd 75 rev	FSK FSK	300 75	1300/2100 390/450		
V.26	D	2400	DPSK	1200	1800		4
V.27 ter	F	4800 2400	DPSK DPSK	1600 1200	1800 1800		8
V.29	F	9600 9600 4800	QAM QAM QAM	2400 2400 2400	1800 1800 1800		16 8 4
V.32	D	9600 9600 4800	TCM QAM QAM	2400 2400 2400	1800 1800 1800		32 16 4
V.32 bis	D	14400 12000 9600 7200	TCM TCM TCM TCM	2400 2400 2400 2400	1800 1800 1800 1800		128 64 32 16

Chart courtesy of Cirrus Logic, "Modem/Fax Technology Guide" (November 1991)

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cycle of this carrier wave can carry up to eight bits of data by varying both amplitude and phase, not just by moving up or down several degrees but by modifying the wave at particular angles over a 360° range.

Quadrature amplitude modulation (QAM), the transmission method for V.29 fax modems, transmits data symbols as a recognizable combination of amplitude and phase shifts, as a constellation with targeted points. Trellis-coded modulation (TCM), the transmission method for the V.32 bis 14,400-bit/s data modem, involves QAM with forward error correction—that is, data points are sent twice, and each bit is tested against its predecessor. (A summary of modem standards, their data rates and transmission techniques is shown in the table on p 68.)

There are several modem-resident protocols that, like trellis coding, improve transmission over a noisy signal line but also raise the data-transmission rate. The most commonly used are the MNPs, developed by Microcom (San Jose, CA) for 2,400-bit/s modems. The MNP 3 protocol, for example, is used for synchronous bit-oriented, full-duplex data exchanges. By eliminating the start and stop bits in a block data transmission, the protocol obtains a throughput of approximately 108 percent. MNP 4 is similar to MNP 3, but also has adaptive block sizing and data phase optimization; its throughput efficiency is approximately 120 percent. MNP 5, the most commonly used protocol, adds data-dependent compression to MNP 4. Its throughput is approximately 200 percent—4,800 bits/s—at a 1.6:1 compression ratio.

The V.42 bis is a CCITT error-correction scheme that adds Lempel-Ziv data compression to the link access protocol modem, for a 4:1 data-compression ratio. (The Rockwell RC144ACL, in addition, will support MNP 10, a protocol useful for data transmission over cellular telephone lines or under other adverse conditions.)

The ability to shape the phase of the carrier signal in response to multiple protocols depends on a DSP. This can be an add-on device. Zilog (Campbell, CA), for example, manufacturers a mixed-signal processor with modem, fax and voice firmware. The Z89120 integrates a 16-bit DSP, an 8-bit microcontroller, an A-D converter, and a pulse width modulation D-A converter on a single chip. The firmware permits host interface and control using the AT command set, with voice and fax extensions for the Z8 controller. The modulation and demodulation algorithms performed by the DSP provide firmware support for full-duplex V.22 bis modems with operating speeds of 9,600 bits/s. Voice compression is performed at 7 kbits/s using the DSP and data converters. Motorola (Austin, TX) also offers the 68000-based 68302 as a multiprotocol communications controller.

The caller ID controversy

Caller ID, on the other hand, is a firmware function. "It's relatively simple to implement," says George Urbani, communications business unit manager for Cirrus Logic, which doesn't offer caller ID functions at this time. "You simply capture the V.21 demodulation scheme between the first and second ring." The phone number of the call initiator, in other words, is embedded in a signal from the local telephone company's central switch.

The problem, as Urbani explains it, is that the right to offer caller ID functions—the legality of caller ID, to put it another way—is restricted in many states, including California. There are many professional groups that believe caller ID constitutes a violation of privacy. The argument goes that the identity of obscene callers and unwanted solicitors should be protected. These groups lobby against the proliferation of the service.

This means that if you subscribe to the caller ID service in New Jersey,

ISDN: An uncertain future?

In principle, the service known as ISDN (Integrated Services Digital Network) will provide all the capabilities that fax-modem users want in a business environment. Based on the dedicated lines used to provide multiple telecommunication services between buildings on a campus or various centers of a single company, ISDN offers multiple channels for digitized voice and data at single-channel data rates of 64 kbits/s. Voice is typically digitized at the handset, and multiple channels can be synchronized for higher data rates. The higher bandwidth accommodates all types of image data, including fax, and caller identification is built into the service. So says Jeffrey Fritz, a telecommunications engineer with West Virginia University (Morgantown, WV).

Because several Bell Operating Companies have used West Virginia University as a proving ground for ISDN hardware, Fritz is well versed in its capabilities and current shortcomings. Every caller on ISDN, says Fritz, must have an Internet address. This means the address of the caller, as well as time and duration of the call, are logged automatically on the network, regardless of whether the call communicates voice or data.

Moreover, ISDN will support video conferencing better than analog phone lines can because, at 64 kbits/s for a single channel (or 128 kbits/s for dual channels), image compression is much less than that required for analog lines. In Europe, manufacturers such as Siemens and SGS-Thomson are exploring the uses of a broadband ISDN that will provide data rates of up to 200 Mbits/s. In addition to real-time video conferencing with very little need for image compression, this bandwidth will be so great that high-resolution color images—medical X-rays or CAT scans, for example—can be transferred between hospitals for online consultations. Several video conference systems have been developed in the United States and Japan that use dual-channel ISDN links at 128 kbits/s. West Virginia University, in fact, will soon be trying out such a video conference system from Compression Labs (San Jose, CA).

It's likely that corporate business users will be the first to demand video conference services, and that ISDN rather than analog phone lines will provide the link. But Fritz also foresees ISDN extending to home-office use, just as PC modem and fax links are used in that environment now.

Exar's Richard Reifer agrees that video conferencing is now the primary application for ISDN, and he suggests that it may be its only application for a while. "ISDN is a good conceptual model," he says, "but there are alternatives to it that are less expensive." The high-bandwidth fiber-optic cable needed to bring ISDN to the home won't be available until well into the twenty-first century.

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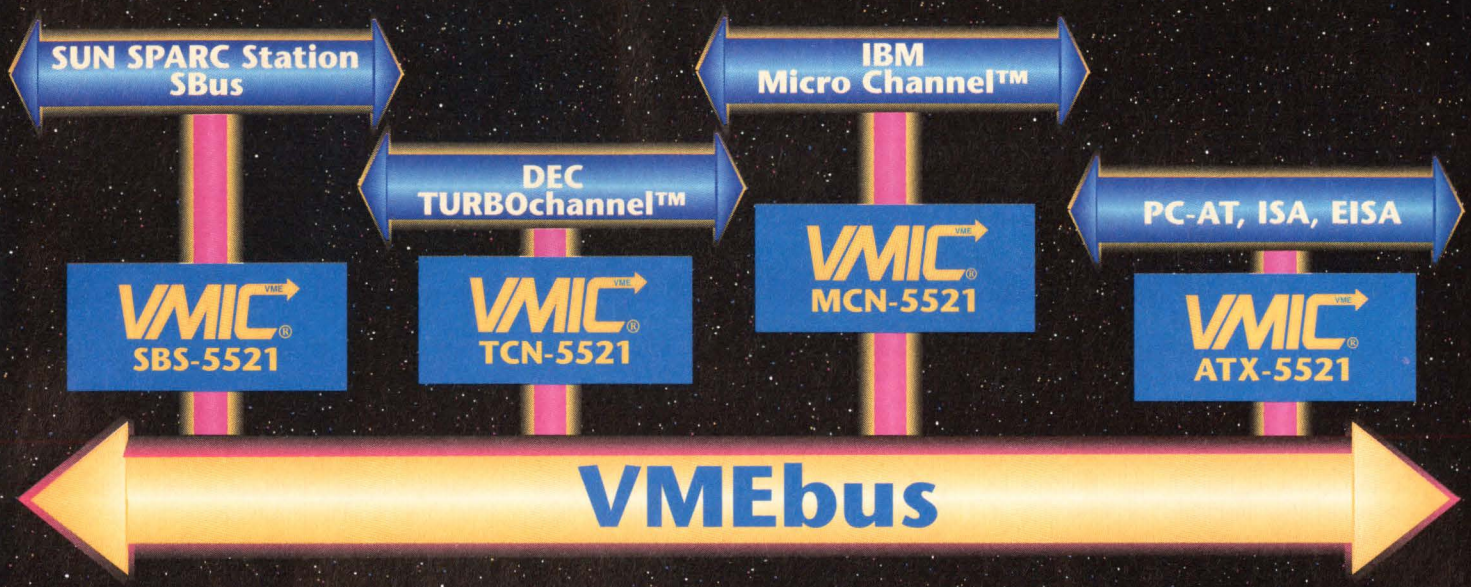

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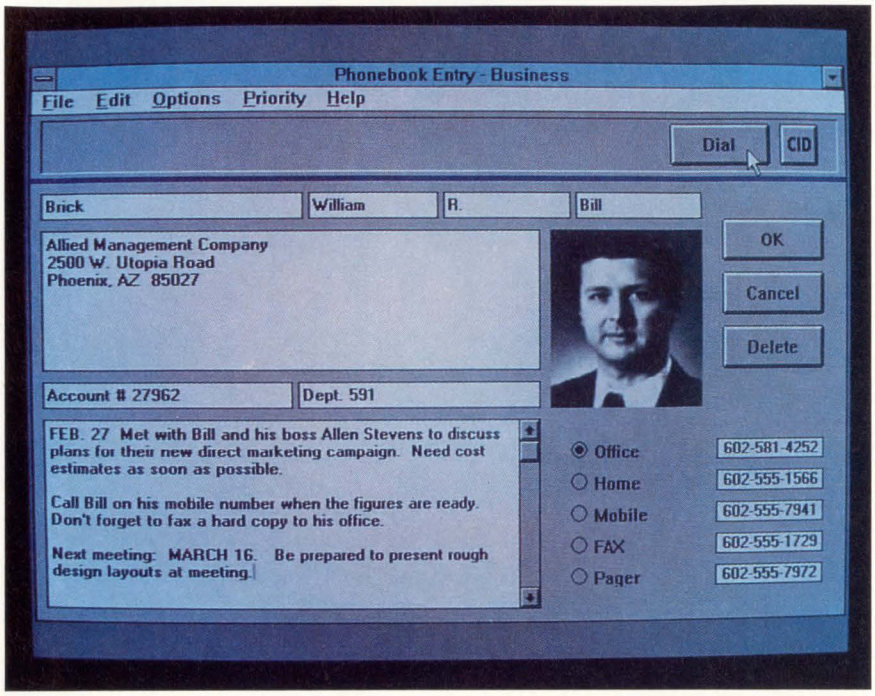

The WindowsPhone hardware/software kit is one of the first to take advantage of caller ID services. The system identifies the caller by telephone number, pulls up relevant information about the caller and displays it on the screen, even before you pick up the phone. But, caller ID services aren't legal in every state.

where it's legal, you won't be able to identify a caller from California, where the service is restricted. "With such restrictions," says Urbani, "caller ID won't live up to its potential."

The IC manufacturers, such as Exar and Sierra, who currently offer call-recognition firmware with their chip sets, are banking that caller ID will be legalized in most business localities and that the regional Bell Operating Companies will provide the necessary identifying tones in the signals that come from their central offices. Exar's marketing manager of communications products, Richard Reifer, for example, believes that caller ID subscriptions will grow at a rate of 12 million per year over the next three years.

Manufacturers of PC insert cards and software are also betting that caller ID will become a vital business service. Data-Cal (Chandler, AZ), for example, has developed a Windows-based hardware/software system which tracks both incoming and outgoing calls to and from a PC host. For outgoing calls, you select a phone number and related files from your database. The computer places the call and automatically records the time spent online. For incoming calls, the WindowsPhone system uses caller ID information to compare the number of the originating caller with numbers in your database. Where there's a match, relevant information on the caller can be brought to the screen, even before you pick up the phone.

Technical restrictions

While caller ID service may be withheld for legal and jurisdictional reasons, there are other telecommunication services that may trip over technical limitations. Armondo Geday, Rockwell's director of worldwide marketing, foresees that a number of communications functions will be impeded by the analog phone line. Color fax, for example, currently isn't possible with telephone communications. Apart from a lack of transmission and reception standards, the major difficulty centers on the inability to print a color hard copy. Color fax won't proliferate until inexpensive color printers become available.

The major problem with analog phone service is its bandwidth; it's too narrow to accommodate moving video images or teleconferencing services. The amount of compression needed to transmit video images over existing phone lines would be far too costly. Even V.Fast, at 28.8 kbits/s, is much too slow. The need for video conference services may even dampen the trend toward putting multiple data communications services on standard phone lines.

Local phone company service, almost everyone agrees, doesn't have the bandwidth for video services such as video conferencing. The ISDN (Integrated Services Digital Network) will provide higher transmission bandwidth, while reducing some of the compression requirements for video transmission. While there's currently a movement afoot to make ISDN national, so as to link services between the regions serviced by local Bell Operating Companies, implementation has been slow. Some semiconductor manufacturers, such as National Semiconductor (Santa Clara, CA) and SGS-Thomson (Phoenix, AZ), have made substantial investments in ISDN; others such as Exar are concentrating on the primary-rate trunk lines. Exar has formed an alliance with AT&T Microelectronics (Berkeley Heights, NJ), in fact, to create T-1 trunk-line products that will operate at 1.544 Mbits/s. But with support so divided, few analysts foresee ISDN reaching large numbers of business PC users anytime soon.

Cirrus Logic's Urbani voices a colorful personal opinion about all this: "The phone company runs its equipment until it dies. They'll use vacuum tubes if you let them," he says. "As a consequence, ISDN was never fully implemented, and much of the technology it was supposed to embody has passed. Perhaps the phone company's new interest in the data and TV businesses will speed up implementation of ISDN." ■

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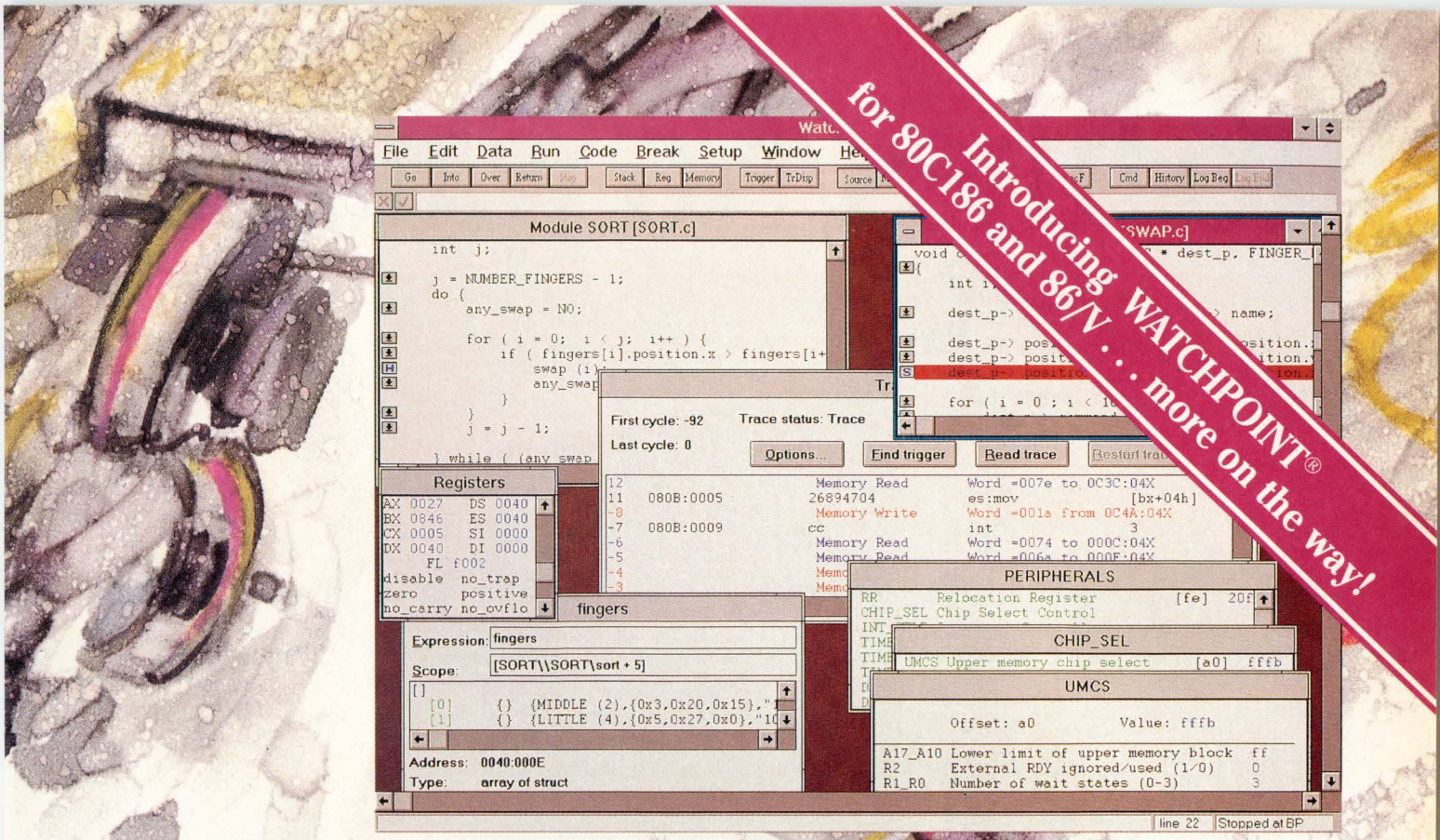

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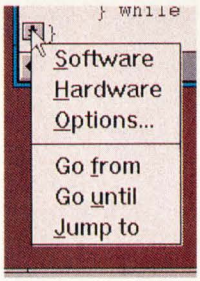

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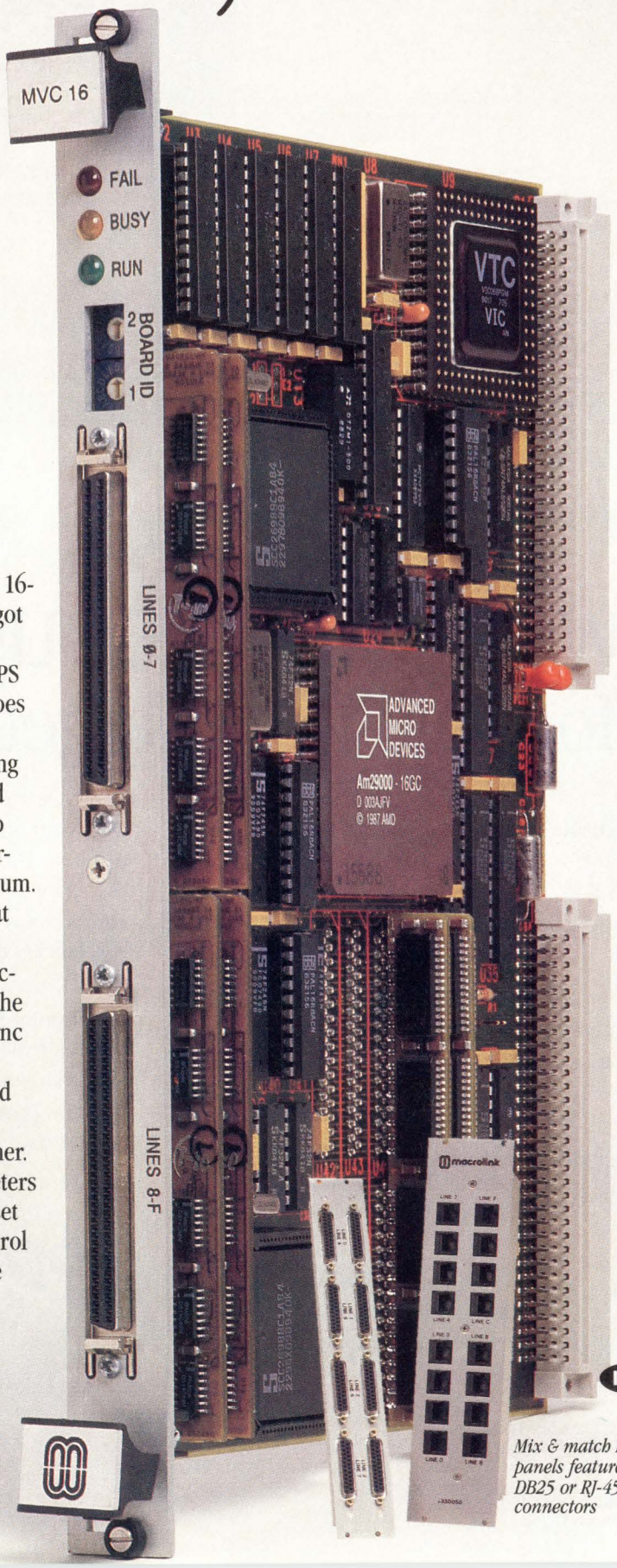

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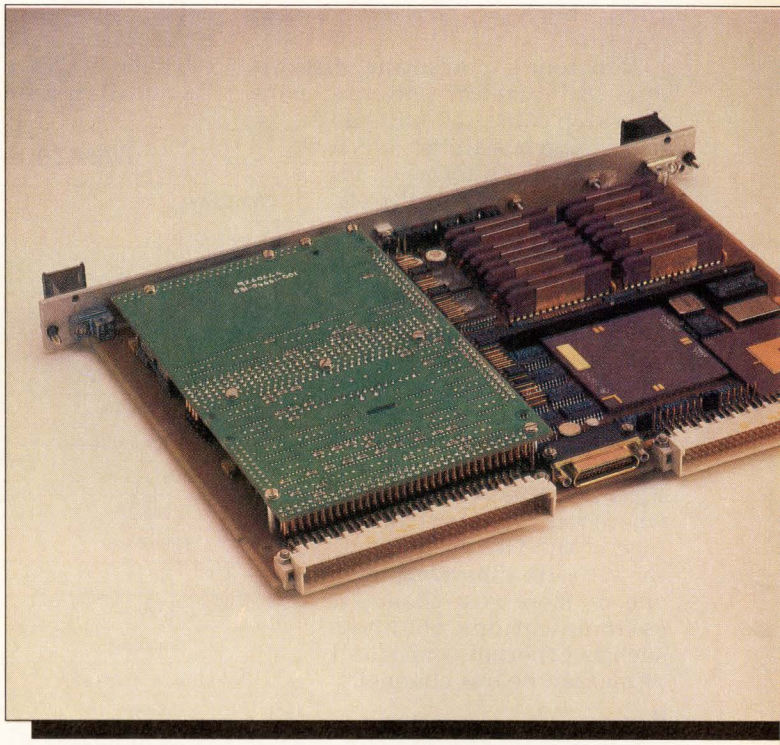
Mezzanine buses gain respect, find new uses

High-density chips and chip sets are bringing more and more functionality to a single board, often reducing system bus requirements. This opens the way for mezzanine boards, not only to increase available board real estate, but to become an integral part of the system architecture—in some cases to the exclusion of system buses.

Warren Andrews, Senior Editor



Mezzanine board technology has made giant strides, including gaining acceptance from one of the world's toughest customers concerning quality and reliability—the U.S. Department of Defense. Radstone Technology's MXbus, which recently passed military muster, is shown here with the company's MIL-STD-48040 processor board.

Once seen as a not-so-reputable fix to system problems, the mezzanine bus is fast becoming a major architectural feature in system design. On one hand, mezzanine buses provide a good way to personalize I/O on standard-bus boards. There's also a growing trend toward a local or mezzanine bus replacing the system bus. This has resulted in a rash of single-board computers (SBCs) with no main system bus, with I/O residing on a number of mezzanine tiles.

Early mezzanine or daughter boards were thought of as kludges, fixes forced by poor initial design. They were necessary but frowned upon—like the soldered-in jumper wires and cut circuit board traces. Such boards were usually ridden with problems related to thermal management and a clean interface to the motherboard.

Mezzanine approaches were also criticized because of questionable reliability. Early connectors and edge-card fingers were suspect and failure-prone. So unreliable were some of these connectors that a critical tool in the serviceperson's kit was a pencil eraser used to burnish plated edge-card contacts.

That period's now behind us, however, because a number of factors have combined to add respectability to daughter board approaches. These include dramatic improvements in connector technology, the availability of modular computers and the growing adherence to hardware and software standards.

Among the factors that have contributed to the growing acceptance and popularity of mezzanine approaches, the most commonly mentioned by users is that mezzanines offer increased circuit density and more efficient use of board real estate. This gives board vendors the ability to customize standard boards for special applications.

Pete Yeatman, president of Radstone Technology (Montvale, NJ), empha-

sizes that his company's aim for mezzanine board technology is to provide enhanced functionality with a device that's an integral part of a system. "Mezzanine boards aren't simply something you add on at some future date to increase basic system function," he says. "Mezzanine board functions are a significant part of the system architecture, both in hardware and software."

Radstone's marketing director, Joel Silverman, concurs, commenting that not only do mezzanine buses offer added functionality in terms of additional I/O, they can also offload the system bus through a separate channel—a local or mezzanine bus. "In many configurations," says Silverman, "a single board's processing power is so great it can call for a number of I/O options beyond the basic system bus. This has resulted in what Radstone calls its FreeFlow system architecture, where VME cards take advantage of the VME system bus, the VSB [VME subsystem bus], one or more SCSI channels, communications channels such as Ethernet, and a local or mezzanine bus channel."

Gaining respectability

While mezzanine boards may have acquired a bad reputation early on, they seem to have come around to respectability—even with one of the industry's toughest customers, the U.S. military. Radstone modified its PEX and APEX buses to meet military muster, resulting in the company's MXbus. "The philosophy behind MXbus is the same as for the PEX and APEX buses," says Silverman, "only the mechanicals had to be changed. These changes include allowing for conduction cooling and permitting connections to the P2 connector rather than to the front of the board." As is the case with other standard boards adapted to military service, the Radstone concept is to provide standard hardware fitting COTS (commercial off-the-shelf) and NDI (nondevelopmental item) military specifications, and so lower-cost.

In addition to being used for basic I/O, specialized mezzanine buses perform other functions, including serving as coprocessor modules. While the most obvious such modules are the SPARC and Motorola 88000 M bus implementations for multiprocessing, others have been used to compress hundreds of MFlops of performance onto a single VME-sized board.

To increase processor density in very-high-performance multiprocessing systems, for example, Cyclone Microsystems (New Haven, CT) puts an i960 processor on one of its Squall mezzanine boards, which in turn plugs into an i960-based VME board. In maximum configurations for applications such as high-speed data-acquisition systems, a single VME rack can include as many as 19 dual-processor boards, delivering the performance of 38 i960 processors. Multiple racks can then be tied together for even greater processing power.

Such approaches have been on the rise for many years, with the VMEbus community alone counting more than 20 different mezzanine-bus approaches released to the public domain. In the Multibus arena, iSBX, one of the first standard mezzanine approaches, has enjoyed a long reign over relatively simple, character-based I/O. It's supported by more than 25 vendors, although its use is starting to tail off as Multibus I gives way to other approaches promising more robust I/O.

Intel's (Hillsboro, OR) iLBX, coming after iSBX, had emerged as the next-generation local bus, aimed at providing high-speed memory to CPU boards without the problems associated with system bus latency. Although widely used, iLBX suffered from being applied to problems that were too highly focused and specialized for Multibus II. Intel also introduced the MIX bus a few years ago. This clever attachment scheme for Multibus II lets mount-on modules essentially share the processor bus of a host CPU board. Intel and others have developed a number of MIX modules, yet the cost per module has tended to keep them out of high-volume I/O applications.

Mezzanine buses

Company	Bus(es)
Compcontrol	Expansion Module
Cyclone	Squall
DataCube	MAXbus
Dynatem	XSCSI, XLAN, XIO
Eltec Electronik	LEB (logical Extension Bus)
Force Computers	Flexi-bus
General Microsystems	SAMbus
GreenSpring Computers	IndustryPack
Heurikon	COREbus
Interphase	IoDB
Ironics	IV3220, IV3272, IV9001
Matrix	Dbus-68
Omnibyte	OMNImodules
Performance Technologies	E PAK, I/O PAK
Radisys	EXMbus
Radstone Technology	PEX, APEX, MXbus
Sun Microsystems	SBus
Mizar	MX-side connector
PEP Modular Computers	CXM, CXC, PiggyBack
Xycom	PC/104

Off the bus

While mezzanine buses have largely been viewed as a board maker's standard bus fix to provide wide-ranging I/O capabilities without changing the basic board, an entirely new architectural approach to embedded computers using them has recently emerged. This approach looks at the system from the viewpoint of the CPU, and uses a local bus rather than a system bus for I/O. This approach differs somewhat from more traditional standard-bus approaches, in that it's more likely to result in general-purpose computer engines steered to particular applications through the I/O.

"More traditional approaches, such as those used by Radstone," says Silverman, "use a board optimized for a specific application, such as high-performance multiprocessing. But while boards may be optimized for an application, it's still only possible to include perhaps 80 percent of what any given customer wants. The remainder can be accommodated with either manufacturer- or customer-built mezzanines."

Over the past several months, several examples of the general-purpose, single-board approach have surfaced. While many system makers have in the past used an SBC with a mezzanine board as I/O or as a personality module, these boards have usually been proprietary, de-

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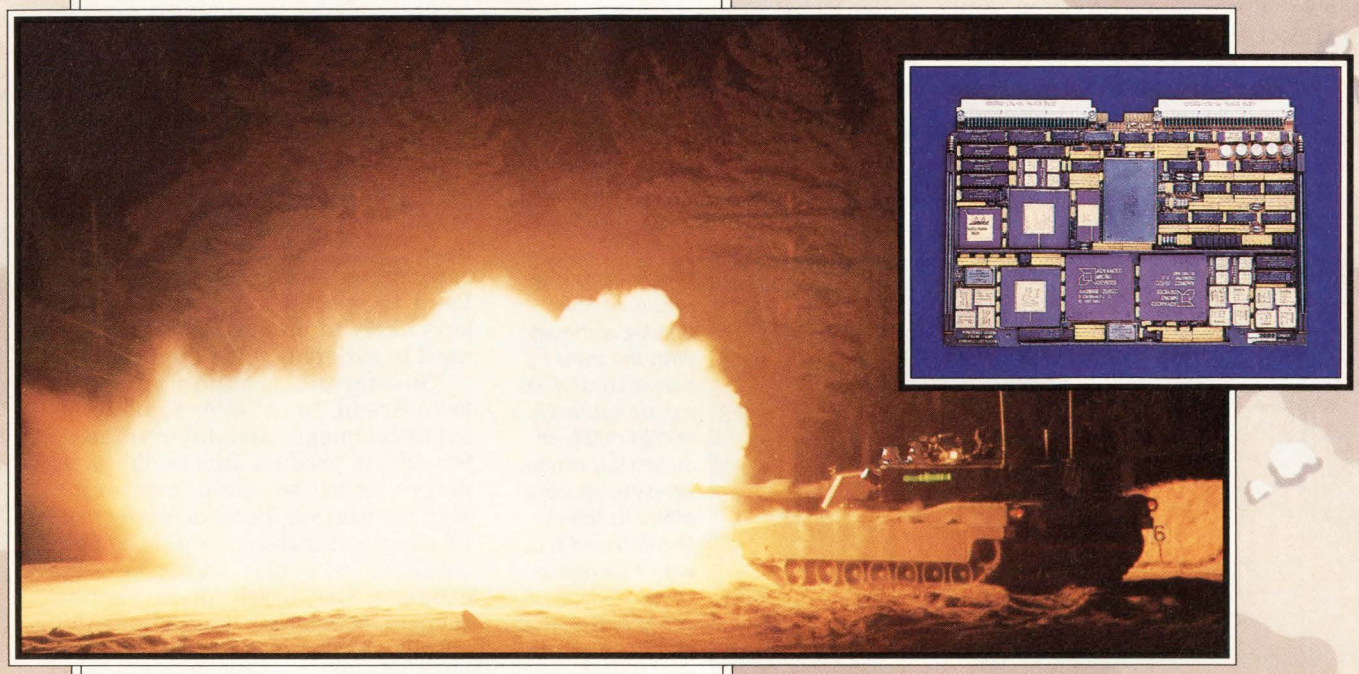

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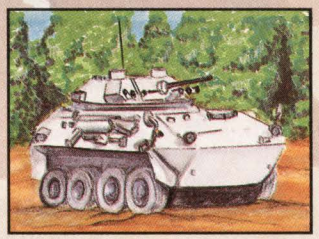
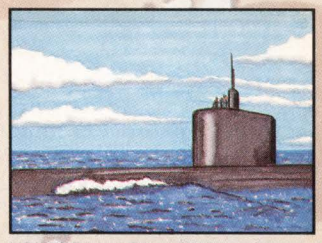
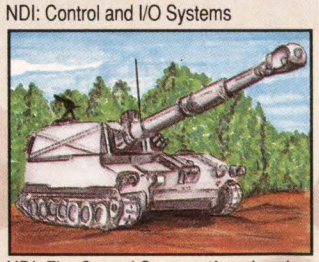


NDI: Control and I/O Systems



NDI: FDDI and Ethernet Networks

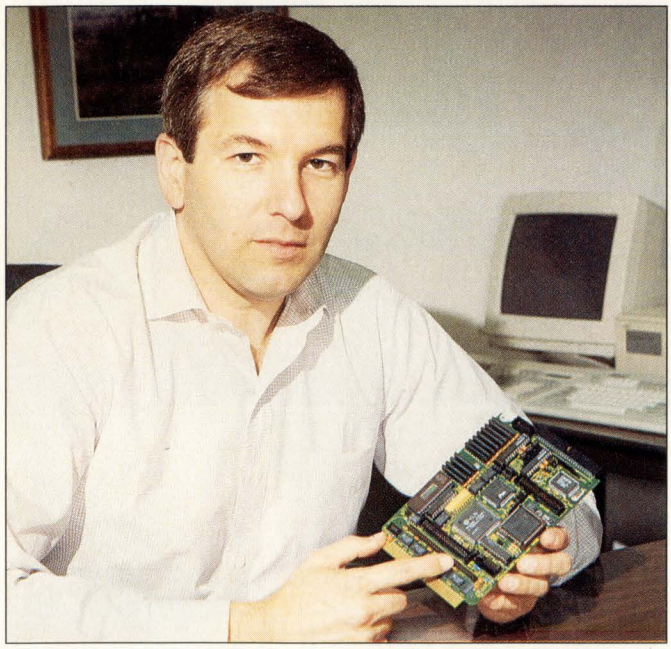


NDI: Fire Control Systems/Auto-Loader

NDI: Gun Control/Auto-Loader

veloped for a single application. One of the first manufacturers to offer such a board as a standard industrial product was Sun Microsystems Computer Corporation (Mountain View, CA), with single-board versions of its SPARCstation 1, 2 and now 10, called SPARCengines. Each of these SBCs includes at least two slots for SBus I/O modules. You can select from among more than 100 Sun and third-party SBus cards.

Others have also jumped on the mezzanine-bus bandwagon. PEP Modular Computers (Pittsburgh, PA), for example, has developed a bus/busless strategy designed for industrial applications. At the heart of PEP's approach is the company's con-



WinSystems vice-president Bob Burckle is shown with the company's latest mezzanine approach, a PC/104 riding on an STD Bus carrier. WinSystems now offers its latest 80486-based CPU with four options: stand-alone, with STD interface, with STD interface and PC/104 mezzanine, and with an umbilical cable to a passive ISA backplane.

troller extension module (CXM). CXM was developed to provide a flexible technology that could carry PEP piggyback boards, as well as provide a relatively large mezzanine platform—about ⅔ the size of 3U VME.

CXMs use a straightforward connection scheme with a 96-pin DIN header connector and a simple addressing scheme that lets you stack up to seven CXM modules on a single base module. In its simplest configuration, a system can be built up without a backplane bus and can interconnect via similar systems using simple field-bus connections. (PEP uses Profibus for this purpose.)

In more complex configurations, however, multiple 3U VME modular and controller boards can be used in a standard 3U VMEbus rack to increase processor power for demanding applications. The approach lets any combination of VME and CXM boards be used.

PEP presently offers a pair of host carrier boards, and already includes about 20 CXM modules covering a wide range of industrial applications. PEP president Josef Kreidl says, moreover, that there are currently at least 20 customer designs either in use or under development. PEP also makes 22 piggyback boards providing digital, analog and miscellaneous functions.

Toward a mezzanine standard

Most recently, Force Computers (Campbell, CA) and Motorola (Tempe, AZ) have joined the flock of mezzanine believers. Force has sided with Sun and provides a VMEbus-based version of Sun's SPARCengines 1 and 2. In addition, the company provides a connectorless 6U-form-factor version of the 2E board without the VMEbus interface. Both boards sport a pair of SBus slots. Force is expected to announce a SPARCengine 10 version shortly.

For its part, Motorola saw a need for broad I/O functionality on a single board and came up with its 162 SBC, which is available with and without a VMEbus interface. For I/O, Motorola has adopted GreenSpring Computers' (Menlo Park, CA) IndustryPack technology. "The IndustryPack," says GreenSpring vice-president X. Kim Rubin, "was designed to be the ideal module for the VME form factor. It's been designed such that two modules fit comfortably on a 3U board, and four on a 6U card. This provides users with a broad variety of options from a single platform." GreenSpring also offers a single-board product with four IndustryPack sites that's based on the Motorola 68332 communications processor.

In the interest of fostering the IndustryPack technology, GreenSpring has submitted it to VITA (VME International Trade Association) for possible adoption as a formal industry standard. But the idea hasn't met with much success. First, because just about every VMEbus manufacturer offers its own mezzanine standard, with many offering two or more; and second, because mezzanine bus technology is often tailored to specific requirements and isn't likely to produce a single standard to satisfy diverse applications.

"Mezzanine technology," says PEP's Kreidl, "must offer rapid product development and differentiation for added product functionality. It makes sense to avoid mezzanine standardization, because many useful existing functions would be made obsolete. PEP's CXM technology, for example, specifically preserves the company's existing bank of smaller I/O piggyback functions while offering a simple, cost-effective bus/busless expansion capability."

Proponents of SBus experienced similar resistance when they tried to introduce that technology as a standard mezzanine for Futurebus+. For the same reason that Kreidl mentioned, companies such as Heurikon (Madison, WI) wanted to leverage their current mezzanine technology for the next-generation standard board. Heurikon's CoreBus approach is designed to provide transfer rates in the 200-Mbyte/s range; the company expects to use its mezzanine on Futurebus+ as well as VMEbus products.

MCMs as mezzanine "boards"

While most mezzanine bus approaches are meant to provide flexible I/O solutions, a family of mezzanine buses is emerging that's aimed at higher performance and higher-density packaging. Although these mezzanine boards are usually referred to as multichip modules (MCMs), the approach and technology are basically the same as those used for conventional I/O modules. While there's discussion of even higher-density approaches, such as silicon-

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on-silicon modules, most of the currently implemented and discussed approaches use standard PC-board or older hybrid circuit technology.

Leading the parade in the commercial implementation of such approaches are the SPARC-based processor modules offered by both Cypress Semiconductor (San Jose, CA) and Texas Instruments (Dallas, TX). These modules include a common cache-coherent interface so that other modules can be added to the system without additional changes.

Both the TI and Cypress modules use the SPARC M bus as a standard interface, with an alternate packet version, XBus, also available. The modules comprise the CPU, cache memory, cache memory controller, and interface circuitry. The first commercial use of the approach was in Sun's SPARCstation 10, which is available with up to four TI SuperSPARC modules.

Similarly, Motorola offers its hypermodule, based on its own 88000 M bus technology. Systems are available that accept up to four such modules. Outside of some server implementations, however, the 88000 approach has met with only limited commercial success.

MCMs are currently in their infancy, though, and a variety of modules will probably emerge in coming months. One initiative, offered by the Modular Open System Architecture Standard (MOSAS) council, comprising some 20 major defense contractors, proposes a standard module and board interface to cut across both military and commercial applications.

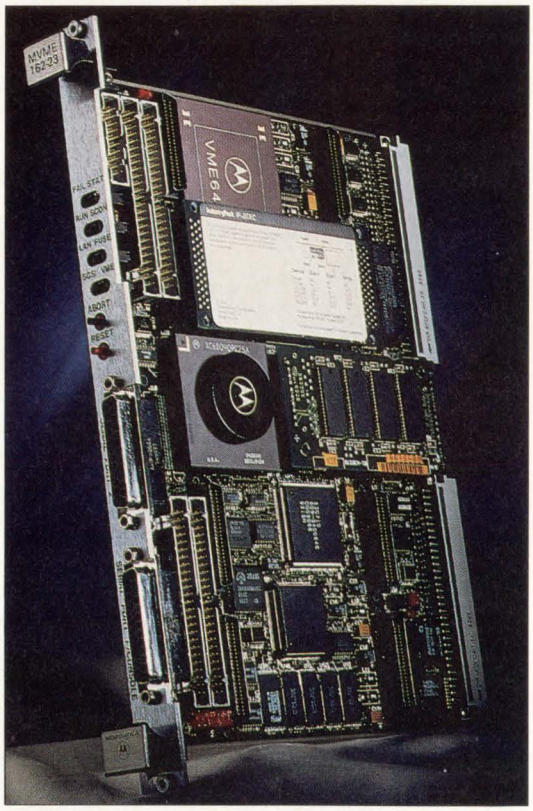
MOSAS is calling for systems based on Futurebus+ protocols, with a standard module form factor, pin-out and module/local interface specification. Initially, four modules are intended to fit on a single SEM-E form-factor board (slightly smaller than 6U in size), with one of them being a Futurebus+ bus-interface module. Others tentatively defined include RISC-based processor, DSP and communications modules.

While the MOSAS concept has merit in attempting to define a universal set of standards, it's come under attack by a number of companies. Some complain that the MOSAS group is exclusionary; others that military applications aren't broad enough to drive the commercial market; and others still that there's no need to introduce yet another format (SEM-E), since there are others already in wide use in the commercial sector; and a single standard such as Futurebus+ on SEM-E with MOSAS modules won't satisfy all applications—not even all land-based, shipboard and avionic military applications, not to mention the myriad commercial and industrial uses.

An option from the PC world

Despite controversy at the high end of the market, the embedded personal computer business is booming. One development that has carried the PC architecture into the industrial marketplace has been PC/104. The small form-factor, stackable PC architecture developed by Ampro Computers (Sunnyvale, CA) and subsequently released to the public domain has skyrocketed in use over the past few months. From a humble beginning only one year ago, the PC/104 consortium, a trade group formed around the emerging standard, has grown to almost 50 members, with more joining almost daily.

PC/104 backers are working to make their specification an IEEE standard—or, more accurately, a subchapter of the IEEE 996 ISA standard. Thus far the consortium has been accepted as a working group and has its own PAR, P996.1. "The project is going ahead with the standard for compact embedded PC modules designation at this time," says Ampro's vice-president of strategic development, Rick Lehrbaum, "just in case there are any changes between the completed IEEE specification and the current PC/104 specification. But I don't anticipate any problems along the way." With or without IEEE approval, PC/104 is well on its way to the critical mass required to become a market standard.



Motorola's board group broke tradition when it offered its first 6U SBC without a VME interface. The board, also offered with a full VME interface, is aimed at cost-sensitive OEM applications. I/O is handled with four sites for GreenSpring IndustryPack mezzanine boards. A marketing agreement between GreenSpring and Motorola lets the latter company resell IndustryPacks.

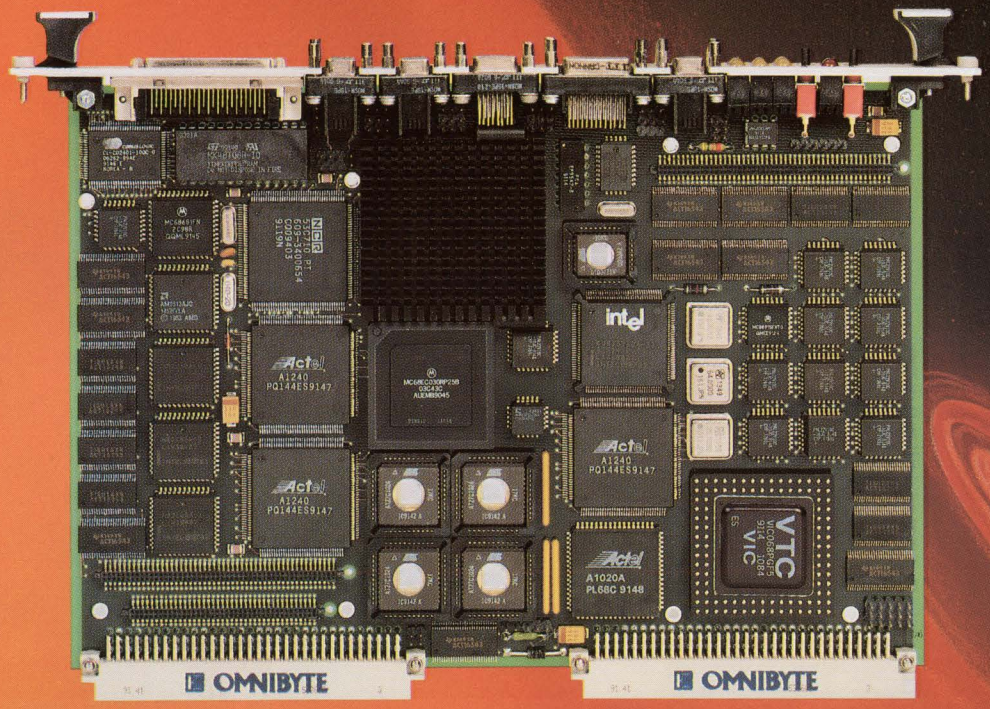
Package, power, price

The small form-factor PC/104 approach has found wide utility: in SBCs using it as a mezzanine bus, in PC/104-form-factor CPUs and in other standard buses such as VME and STD that use PC/104 as a mezzanine. The advantages of PC/104 are that it provides small, inexpensive, reliable, low-power I/O for PC-based designs.

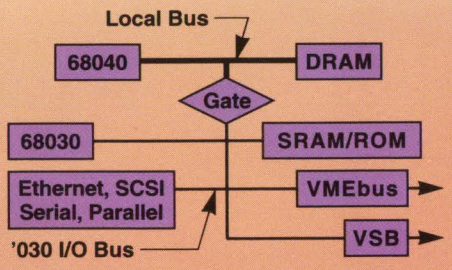
One of the first vendors to see PC/104 as a mezzanine bus for VME was industrial board and system maker Xycom (Saline, MI). The company includes a PC/104 site on its 386-based VME board, permitting fast, easy and low-cost addition of PC-type functions to a VME system. Others in the VMEbus community are reportedly looking at the approach and will probably be making announcements within months.

While VME makers are taking advantage of small, low-cost, low-power PC/104 technology, STD makers are just waking up to the idea. STD Bus has long been regarded as the foremost I/O bus because of the broad range of I/O boards available for it. The idea, then, of using a mezzanine for anything but the simplest function was slow in coming to this community.

68040 + '030 I/O Bus = 39 MIPS



Available: 4-128MB RAM, Ethernet, SCSI, VSB, VME64



Taurus™ Dual Bus Architecture

The Taurus is a dual-processor, dual-bus, single slot VME board. Its dual-bus architecture allows the 68040 to execute code uninterrupted, while the '030 processes on-board I/O. This optimizes the 68040's performance. Using the '030 as an I/O processor simplifies writing your code. You only need to write high level code to the 68040. The '030 handles the device level code. You also can use the '030 as a DMA controller, while the 68040 directly controls all on-board I/O devices. The '030 uses the SRAM with the 128KB of EPROM code provided by Omnibyte.

Performance	68040: 29 MIPS, '030: 10 MIPS, VME: 50MB/sec, VSB†: 50MB/sec
Intelligent I/O	Ethernet: i82596CA†, SCSI: NCR53C710†, 4 RS232D: CD2401
Standard I/O	2 RS232D: 68C681 DUART, 32 Lines Parallel I/O, or 16 w/ Centronics Printer Port
Memory	4MB to 128MB† DRAM, 512KB SRAM†, 8KB NVRAM, 1MB FPROM†, 4MB EPROM
Other	VSB†, VME64†, Watchdog, Calendar Clock, Mailbox, (6) 16-bit Timers, Snooping, Advanced Omnimodule™ Socket
Software	VxWorks[1], OS-9[2], UNIX[3] CrossCodeC, FreeForm[4], OMNIbug

† Denotes optional features.

The Taurus extensively uses intelligent, on-chip DMA devices for Ethernet, SCSI and serial I/O. This helps reduce processor intervention. Up to 2 stackable modules contain the DRAM. This allows upgradable options from 4-128MB.

Advanced Omnimodules provide additional custom I/O. You can stack Advanced Omnimodules up to 3 high. The Taurus can accept 1 memory module and 1 Advanced Omnimodule and still fit into a single slot.

To learn more contact Larry Snow:

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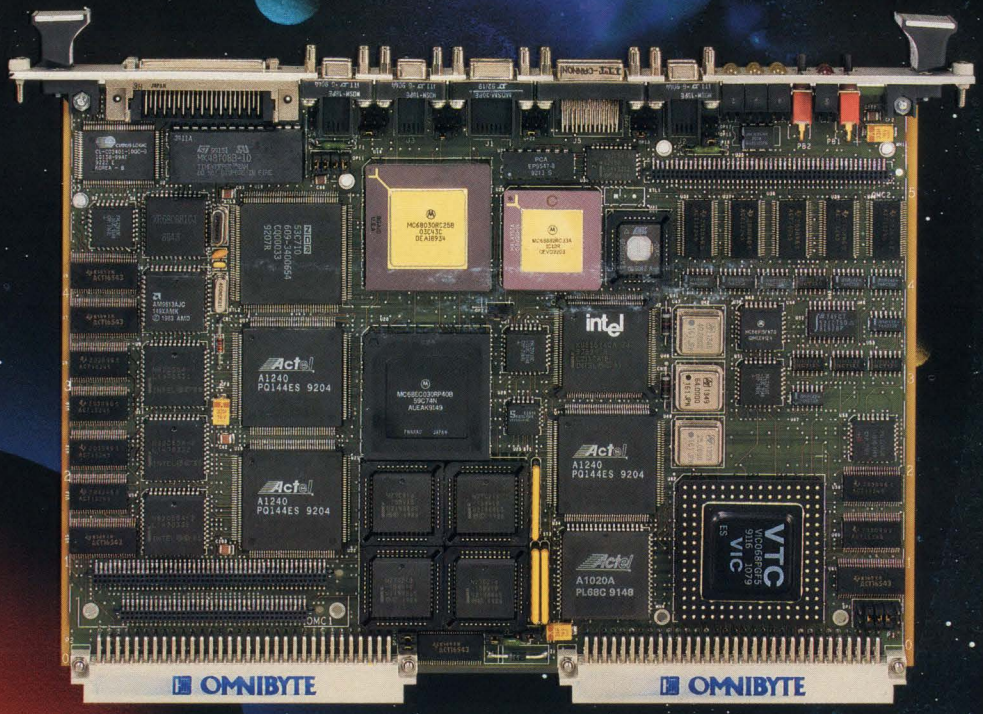
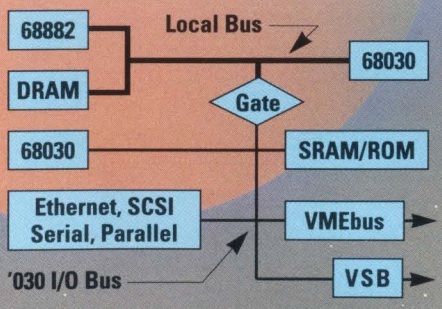


Omnibyte's ARIES™ VME SBC



Aries Architecture

The Aries features 2 68030's. You can use the 2nd '030 as an I/O processor or DMA controller. Using the 2nd '030 as an I/O processor simplifies writing your code. You only need to write high level code to the main '030. The 2nd '030 handles the device level code.

Intelligent I/O	Ethernet: i82596CA†, SCSI: NCR53C710†, 4 RS232D: CD2401
Standard I/O	2 RS232D: 68C681 DUART, 32 Lines Parallel I/O, or 16 w/ Centronics Printer Port
Memory	4MB to 128MB† DRAM, 512KB SRAM†, 8KB NVRAM, 1MB FPROM†, 4MB EPROM
Other	VSB†, VME64†, Watchdog, Calendar Clock, Mailbox, 68882†, (6) 16-bit Timers, Snooping, Advanced Omnimodule Socket
Software	VxWorks[1], UNIX[2], OS-9[3], CrossCodeC, FreeForm[4]

† Denotes optional features.

A gate and I/O bus allow the main '030 to execute code while the 2nd '030 processes its extensive I/O. This optimizes the Aries' overall performance (20 MIPS total).

For less I/O intensive applications, you can get the Aries in a single processor version.

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A Look At Today... A Vision of Tomorrow

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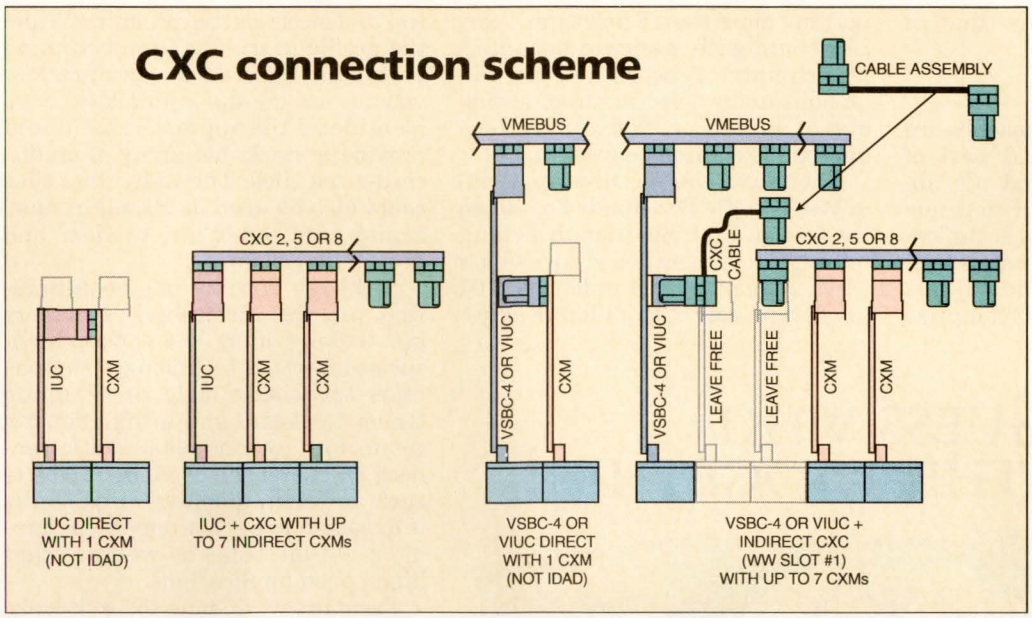

PEP Modular Computers' industrial computer strategy calls for a flexible combination of stand-alone, busless modules; stackable mezzanine boards; piggyback I/O; and standard 3U boards. Using mix-and-match, OEMs can quickly assemble the proper combination of processing power, communications and I/O. Individual modules or combinations of modules can be connected via a field bus.

The first to see the need for something such as PC/104 was STD board maker WinSystems (Arlington, TX). "We've done iSBX modules before, but they were only for simple, character-based I/O," says vice-president Robert Burckle. "What we discovered was that, with the power of PC-based chip sets, it was possible to squeeze all the functions of a powerful PC onto the standard STD form factor. Many of our customers have been using our STD board as a stand-alone SBC with the system bus connectors waving in the wind."

Burckle relates, however, that it became clear that there was almost always some function that a customer wanted that's not included on a card, regardless of how comprehensive it may be. And yet users are increasingly intolerant of the cost of a separate card cage and second STD board—both in terms of dollars and real estate. "PC/104," says Burckle, "because of its widespread following, relatively low cost, straightforward ISA-based interface, and variety of I/O functions available, is the natural choice. There are already 20 or 30 different peripheral functions available and a handful of CPUs. In addition, the form factor makes a nice fit with that of STD."

The latest WinSystems product family has a full-featured 80486 board with four options. The first is a low-cost, stand-alone SBC; the second is the same board with an STD connector and interface; the third option includes a PC/104 interface as well as the STD interface; and the last option has a cable connector for a standard passive ISA backplane. "All options, including the STD-based boards, include mounting holes for stand-alone mounting of the board," says Burckle.

WinSystems apparently isn't the only STD board maker to realize the value of PC/104 technology. Ken Finster, vice-president of MicroSys (Glendale, CA), reports that his company is looking closely at the approach and will probably go in that direction. Like WinSystems, MicroSys provides iSBX connectors and has realized that many users don't want or need the baggage of a full card cage and system bus. But they do need the flexibility to provide different functions without modifying the main SBC.

More alternatives

While PC/104 offers an inexpensive interconnect for a mezzanine, alternatives are fast becoming available, and may supply price advantages, leveraged by the high-volume PC market. One such approach that's largely targeted at memory is PCMCIA. This compact form-factor approach, backed by the leading consumer manufacturers in Japan as well as the U.S., provides high-density flash memory at prices well below those of discrete parts.

Users of IndustryPack and PC/104 technologies can already take advantage of this approach through adapters available from Ampro and GreenSpring. Whether or not PCMCIA can become a major general-purpose I/O technology—as opposed to simply a memory technology—remains to be seen. It isn't likely to become a mainstream I/O technology for industrial applications in the near future, however, because the need for functions such as data acquisition isn't high enough to attract vendors who'll design specialized parts to fit the exacting form factor.

As PCMCIA is making its commercial debut, Intel's latest 80386/486/P5 local bus, PCI (for peripheral component interconnect), is also coming on the scene. Sometimes billed as a local bus, sometimes as a mezzanine bus, PCI has a defined specification and Intel has reportedly developed interface chips. As initially previewed, however, the bus is intended as a solder-in connection for standard peripheral chips handling such functions as graphics, high-speed communications and other peripheral components.

The advantage of PCI—indeed, its reason for being—is that it handles transfer rates far beyond the capacity of conventional ISA and even EISA configurations. Billed as handling rates of up to 160 Mbytes/s, PCI should be well-suited for the more taxing requirements of multimedia applications.

Only a small leap in technology is required to replace the solder-in approach of PCI with a standard signal pin-out and connector, making it a true mezzanine bus. Should this come to pass, PCI will probably displace ISA for most of the common I/O functions. It might not be a shoo-in in the industrial market, however, because once again, relatively low volumes may make implementation

far more costly than, say, that of PC/104.

Trends for the future

Such mezzanine-bus approaches are fast becoming an integral part of system architectures. And it's apparent that the trend will continue well into the future. VITA technical director Ray Alderman predicts that "It's possible that standard-bus products of the future will comprise nothing more than a mezzanine carrier board with standard bus interface circuitry. A board function will be built up by selecting from a variety of processor, communications and I/O mezzanine boards."

The Futurebus+ Desktop Committee (Profile D) already has taken the lead in that direction. It's eliminating the carrier board by using a stack technology, not unlike PC/104 in concept, but with different physical and electrical parameters. While the profile is still far from becoming part of the Futurebus+ specification, visionaries on the committee have identified a tile approach that would provide a stackable array of credit-card-sized tiles. The individual tiles could also be used as standard mezzanine cards on other standard and proprietary boards.

Although nothing has been finalized yet, the Futurebus+ specifiers are looking at a low-power, high-speed interface technology (such as CMOS transistor logic or Gunning transistor logic) and a high-density connector (such as elastomeric connectors currently used in products such as watch displays). Bus traffic is expected to be fast enough to handle real-time video as well as other high-speed applications.

From the work done so far, it looks as if the framers of Profile D are looking to create the ultimate standard mezzanine bus. But as is the case with Futurebus+ itself, it's as yet unclear whether or not one standard bus will be able to solve all problems—that is, to address both low-cost and high-performance requirements in the commercial, industrial and military markets. ■

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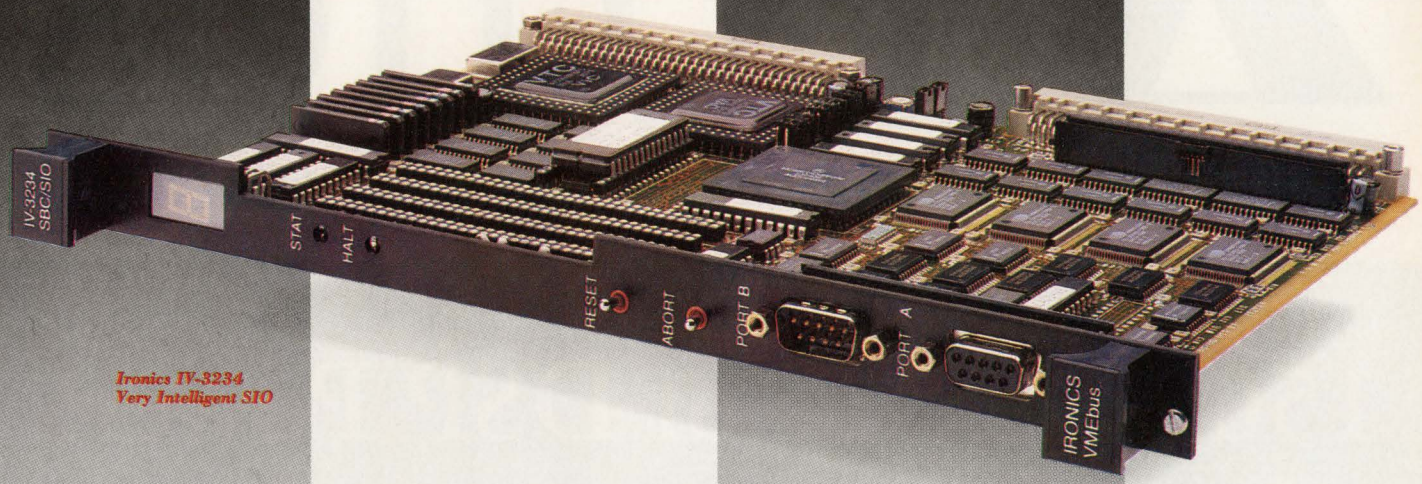

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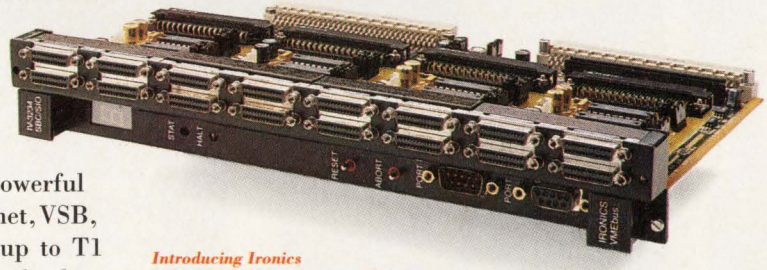

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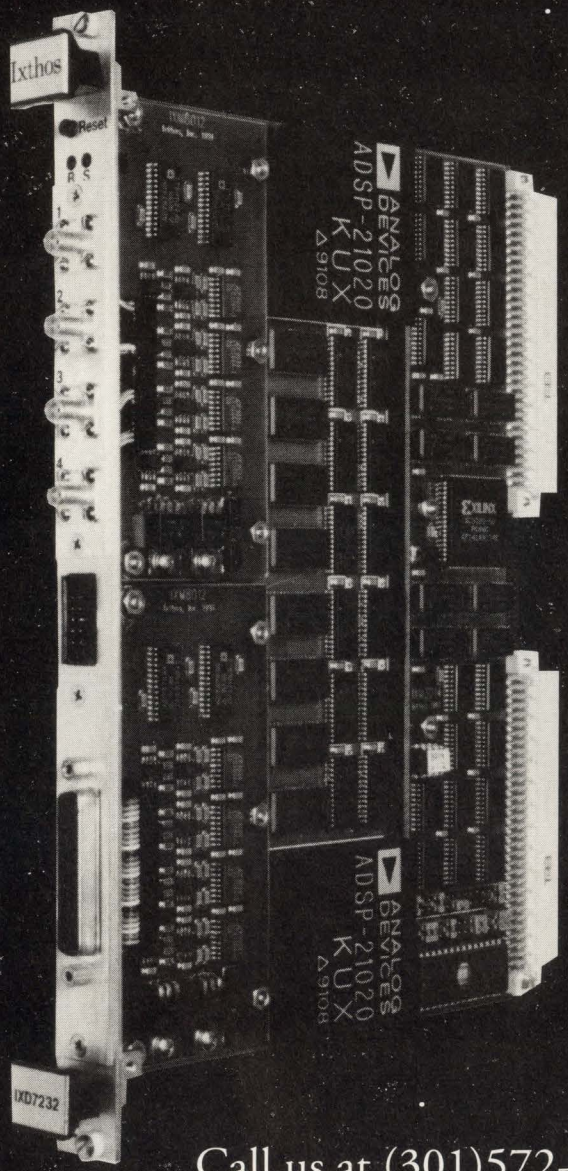

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CIRCLE NO. 51

Design and test engineers alter roles to facilitate test

Time is running out for silicon, circuit board and system houses who haven't taken design-for-test seriously. Old test methods are fast becoming inadequate, while the next generation of systems is waiting in the wings.

Electronics corporations have been singing the praises of designing for testability (DFT) for years. Unfortunately, their arias have been falling on deaf ears and few companies have really embraced true DFT; that is, few are bringing test requirements forward into the design cycle. As components and the systems they drive become more complex and as time-to-market windows close, many companies are, in fact, finding their DFT strategies woefully inadequate. There are myriad reasons for this, but the biggest is simple—unless there is absolutely no way out, people don't like to change the way that they do things.

"Getting design engineers to embrace DFT is a real challenge," says Frank Binnendyk, director of marketing for TSSI (Beaverton, OR). "But right now we have testability problems that are reaching crisis proportions. Packaging and technology trends are producing PCBs and systems that are almost untestable by conventional means, and we can't

Mike Donlin, Senior Editor

simply put a Band-Aid on the problem. But reluctance to change is understandable. Designers still have to worry about everything they always have, and now they're being told that their designs have to be testable as well."

Until recently, design issues were the concern of design engineers, and test issues were the concern of test engineers. Each group was managed differently, and although the gap between the two camps was bridged by the system under development, the two didn't have to deal with each other a lot. If a designer produced a PCB prototype that worked, the board went on to the test engineer, who would more or less start from scratch.

This approach no longer works for many PCB designs, because the smaller traces and surface-mount components of today's PCBs make accessibility by traditional bed-of-nails testers difficult. This means that test points must be placed intelligently on a complex board to make the most of the limited access it provides. Test, then, must be part of the design of a board right from the outset, and there lies the rub.

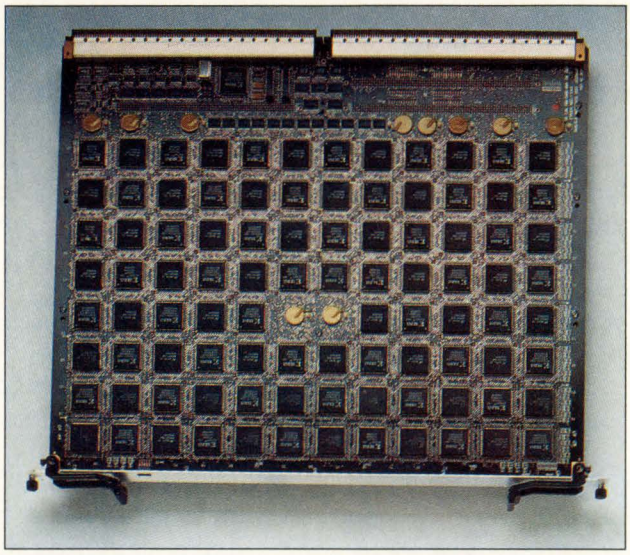
Maturing differently

The EDA and test industries grew up separately, so the concerns of EDA vendors were different from those of automatic test equipment (ATE) vendors. As a result, the tools that each provided to their prospective users weren't able to communicate very well. This was unfortunate because much of the information the designer needed to complete a PCB could be useful to the test department, but the necessary links between the two databases simply weren't there.

To complicate matters, as EDA and test evolved, the technologies that they were helping to create were getting more complex. A prime example is the emergence of multichip modules (MCMs), complex silicon-on-substrate devices that are a test engineer's nightmare. "With traditional PCBs you could take measurements by putting down two probes and analyzing the path between them," says Stephen Taft, CAE product manager at Harris EDA (Fishers, NY). "With MCMs, the traces are much finer, so you really can't inject current or you'll cause problems in the substrate. So people are looking for more passive methods. That means that EDA vendors have to expand their databases to approximate what a capacitance value might be and evaluate problems along a net. The time is ripe for a melding of the two technologies, EDA and test."

As technical advances and market pressures force these two camps to cooperate, both design and test engineers are concerned that they'll have to become experts in the other's discipline. "But it's not really so much becoming an expert in someone else's field as it is getting the appropriate information from one group to the next," says Pete Lwin, marketing manager at Schlumberger (San Jose, CA). "It's really an information management problem. But not many design engineers are willing to implement test strategies simply because another department requests it. So the ATE and EDA vendors have to work to make this transition as painless as possible."

There's tremendous pressure to make these interdepartmental linkages. Corporations embracing DFT strategies have impressive results to crow about, and these results involve the driving forces behind any product's success—cost, quality and time-to-market.



Testability must be implemented from the conceptual phase for complex PCB designs such as this logic emulation board in Quickturn's Enterprise Emulation System. The 24-layer board hosts over 2,400 connector pins and includes 100 quad flat pack ICs. The components are connected by 1.5 miles of wire, and extended over 8,000 nets to 20,000 holes. Use of JTAG made the design testable from prototype to production.

"We're designing 6 × 9-in. VME boards with up to 200 components on them," says Paul Wittenburg, test engineering manager for the Motorola Computer Group (Tempe, AZ). "To make sure that we get the high yield that our six-sigma quality program demands, we use a combination of in-circuit, cluster, functional, and scan testing. We use this test data to weed out manufacturing faults and unreliable component vendors. We are also bridging the gap between EDA and test and are working with companies such as TSSI to make bi-directional links between our testers and simulators. The program is working. Three years ago, it took 12 weeks to develop PCB tests with 65- to 70-percent fault coverage. Today we can develop 95-percent fault coverage in a four-week time frame, and we can envision even better results in the future."

Getting support

Stories such as Motorola's are sure to get the attention of design management and will speed up the development of the necessary links between design and test, but the transition is far from painless. It will undoubtedly take the authority of upper management to drive the effort.

"In many companies, senior management doesn't believe that test, reliability and manufacturability should be the concerns of the design engineer," says Vin Ratford, marketing manager for test products at Mentor Graphics (Wilsonville, OR). "So even if a designer wanted to take the time to incorporate DFT strategies, chances are that he or she would still be evaluated on how fast a prototype was developed. Only when senior management changes the way that it evaluates design engineers' performance—to actually producing a testable, manufacturable product—will DFT take hold."

Undoubtedly, as senior management realizes the benefits of adopting DFT and the consequences of failing to do so, the links between design and test will be mandated. But even when they are, what spe-

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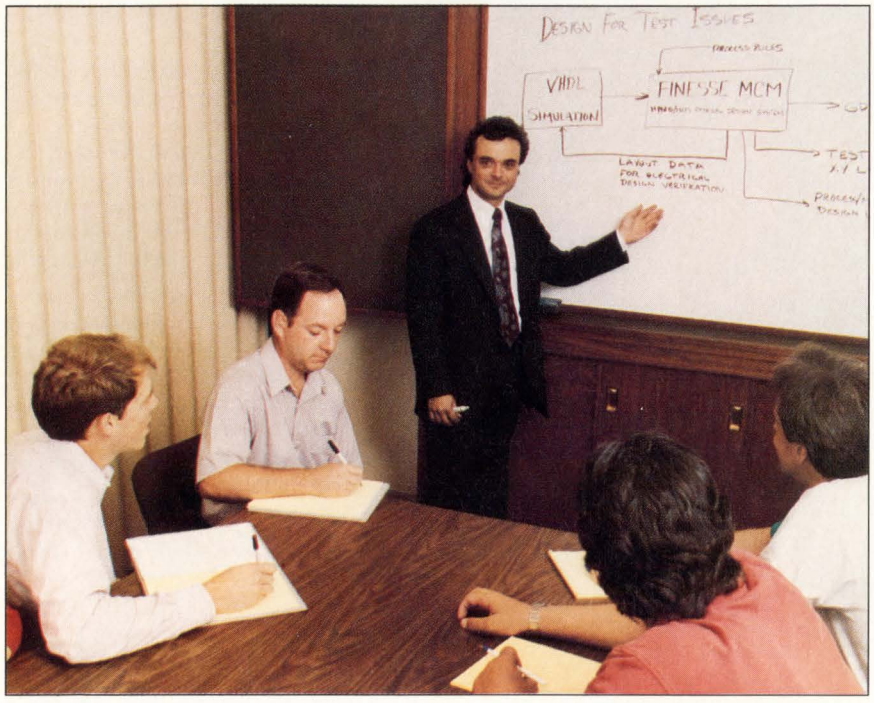
cific products are available to help bridge the gap? One company that's been developing these links is TSSI, whose Wavemaker software accepts data from a variety of EDA sources and generates an intermediate waveform database. The TSSI Waveform Database (WDB) contains behavioral data, independent of simulation and test environments. The database stores unstructured data in a Standard Events Format (SEF) file and structured data in WDB data sets. It permits unrestricted movement throughout the TSSI software system and can be displayed, analyzed, modified, and used in a variety of outputs, including the generation of ATE-specific test programs. The database can also perform both simulation and tester rules checks.



"If you don't incorporate DFT strategies in your MCM design, you'll end up with an untestable product," says Stephen Taft (standing), CAE product manager at Harris EDA (Fishers, NY). "One of the key ways of producing a testable MCM is to take advantage of the information in your design database, so that valuable testability data can be used later on. In our Finesse MCM design tool, for example, we're using an object-oriented database as a decoupling zone to provide a neutral link to test."

Forging a link

Bridging the gap between simulation and test is an important consideration in a successful DFT strategy; otherwise, incorrect and costly assumptions can be made by both the design and test departments. "In a typical test environment, you first run a fault simulation to make sure you have a complete set of test patterns to verify a board's functions," explains TSSI's Binnendyk. "Then, if you're doing functional testing, you create a fault dictionary and set up guided probe diagnostics, which means setting up the right databases to accomplish your testing goals. You take that information and migrate it to the tester and debug the test programs so that they pass a known good board. But when you do this, you change the base level of patterns that were verified by the simulator, so you don't have proof that you have the same coverage. To close the loop, you need to go out of the tester environment and resimulate."

Although products such as TSSI's take advantage of the natural synergy that should exist between design and test data, true DFT needs to migrate up the design cycle, not simply get tacked on at the end. And even though many PCB designs are partially tested through software simulation, the board that comes out of manufacturing can have serious problems if DFT hasn't been implemented. "Not many people are doing full board simulation," says Schlumberger's Lwin. "Even if you simulate functional blocks, it's hard to see how they interact when you get everything put together. There are always a lot of unknowns when you get into asynchronous processes, bus mastering and interrupts. In the past, when you had a lot of test points for observability and many boards were synchronous, testing was easy. But today's asynchronous designs, where you have a microprocessor handling interrupts from peripherals such as keyboards, are much harder to simulate and test. For many companies, it's easier just to make a prototype and debug it."

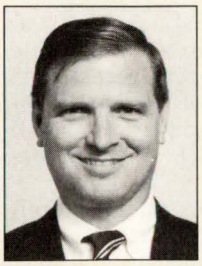
Boundary scan to the rescue?

If designers are going to be persuaded to change their "prototype and debug" habits, an easy-to-use, low-penalty technology must emerge. Fortunately, boundary scan seems poised to assume that role. Also known as the Joint Test Action Group (JTAG) standard, boundary scan was officially adopted as an IEEE standard—1149.1—in 1990. It's a technique that gives you access to the I/O pins of digital circuits on a PCB by means of a test bus consisting of four wires. (A fifth wire is optional.) In a typical boundary-scan IC, a shift register is placed between the core logic and the buffers adjacent to each I/O pin. Each shift register stage lets you control and observe what happens at each I/O pin of the IC.

On a PCB assembled with boundary-scan ICs, the registers for each component can be connected in series to form a path through the design to test each component and diagnose failures. Unfortunately, because few commercially available ICs use boundary scan, it's nearly impossible to populate a board solely with boundary-scan devices. Still, designers see it as one of the few avenues open to them to implement DFT.

"Boundary scan is a powerful remedy for today's test problems, but it's not a panacea," says Chi Yau, supervisor of the boundary-scan technology group at the AT&T Bell Laboratories Engineering Research Center (Princeton, NJ). "PCBs will always have analog parts and jellybean components that don't have boundary scan, but at least boundary scan eases the pinch we're feeling in trying to test PCBs. With boundary scan we can use less test pads and reduce node count. The high node counts in circuit test fixtures are hard to maintain. The small pins are delicate and easily bent, which decreases yield. Bound-

The ultimate design-for-testability technique: 1149.1 boundary scan



Over the years, design-for-testability (DFT) techniques for board test have evolved to respond to changes in device, assembly and test technologies. In the early days of in-circuit test, for example, the basic DFT techniques were published design guidelines specifying the use of test pads on nets without throughhole components, the size and placement of test pads and the like. Later developments include internal scan patterns for the board-test library, tools for in-circuit testability review prior to artwork and simulation of design vectors to be used in test.

Today, however, new technologies are driving electronic manufacturers to embrace the ultimate DFT technique: the IEEE 1149.1 1990 boundary-scan standard. Here the tester hardware is a scan cell designed into the silicon. In the two years since the standard received the IEEE's blessing, dozens of systems houses have started down the boundary-scan path. Teradyne alone has more than 40 customers who are using our software to implement boundary scan.

Three trends

Three major trends are behind the rapid adoption of 1149.1 boundary scan. First, DFT is emerging from the shadows to stand in the spotlight on the concurrent engineering stage. Test and manufacturing engineers have always struggled with testability issues, but other people in the organization, including design engineers, are now thinking about it too.

A second trend is the explosion in device complexity. Typical VLSI device designs today have tens of thousands to hundreds of thousands of gates, resulting in dramatically longer development times for in-circuit test patterns. For a device such as the Intel 80386, for example, it might take seven weeks to develop pin-level fault coverage patterns for in-circuit testing. Custom ASIC devices have similar development times.

The third force behind boundary scan's rise is the lack of physical test access. Nodal access is disappearing because of high-density boards, fine-lead components, surface-mount assembly, TAB, and MCMs. Without physical access, conventional tools simply can't be used. The designer can't access the assembly for prototype debug and verification, nor can manufacturing gain access for bed-of-nails in-circuit testing. These impediments can be so great as to render a product strategically unfit.

Boundary scan solves the problems of pattern generation and test access. Serial test vectors can be generated automatically using ATPG software from ATE vendors, cutting test programming times from months to minutes. And boundary scan provides virtual access through the boundary-scan path, which a board tester or debug accesses from the board's edge-connector.

Despite these advantages for manufacturing and test, device design engineers are quick to point out the drawbacks of boundary scan. Typical objections include the performance decreases from adding the boundary-scan cell's multiplexer in the datapath, the sacrifice of precious silicon to test circuitry and the extra design time that could delay getting the product to market.

These problems are not insurmountable. The typical 1-ns propagation delay can be reduced through intelligent implementation. Designing the boundary-scan cells into the output buffer, for example, can reduce the propagation delay to hundreds of picoseconds or less. The percentage of silicon devoted to the test circuitry declines as device size increases, and large parts are the ones most likely to be designed with boundary scan. On a medium-sized part, for example, 1149.1 circuitry might take up only 2 to 3 percent of the silicon. On a large part such as the 80486, it might be 1 percent. Furthermore, designers can often find ways to employ unused parts of the die, such as the output buffer circuits, as locations for the boundary-scan cells. Finally, to ease the design burden, design tools are becoming available that insert 1149.1 circuitry into ASICs automatically, verify 1149.1 circuitry prior to first silicon and verify BSDL models automatically. Board designers can also benefit from automatic testability analysis software and prototype debug/verification tools already on the market.

Although adoption of the 1149.1 standard may contribute to some increases in design time and costs, the manufacturing group will typically gain far more benefit in terms of reduced time and costs. Compare, for example, the time it takes to develop test programs for Intel's 386 chip without boundary scan to the time it takes for the 486 chip designed with boundary-scan test circuitry. We estimate it takes seven weeks to develop conventional in-circuit test programs for the 386 that deliver 100-percent pin fault coverage. The cost, assuming $50/hour for labor, is $14,000. By comparison, producing boundary-scan test programs with 100-percent fault coverage using ATPG software takes 10 hours and costs $500. If the BSDL is provided by the semiconductor vendor, as is the case with most commercial parts, the time and cost shrink to two hours and $100.

Other benefits

In addition to the savings during manufacturing, 1149.1 offers the potential for faster service response and shorter time-to-market. Strategically, boundary scan opens up an entirely new approach to troubleshooting down systems. Shorter time-to-market comes from time savings in two areas that typically act as gates to new product introduction: prototype debug time and test program development time. Since boundary-scan software and the 1149.1 standard can help shorten both of these activities, they can speed time-to-market. Faster test programming results from the automated programming that can be achieved with boundary-scan designs. Depending on the board design, a lower-cost tester may be able to deliver the same test quality as a much higher-performance, more expensive tester.

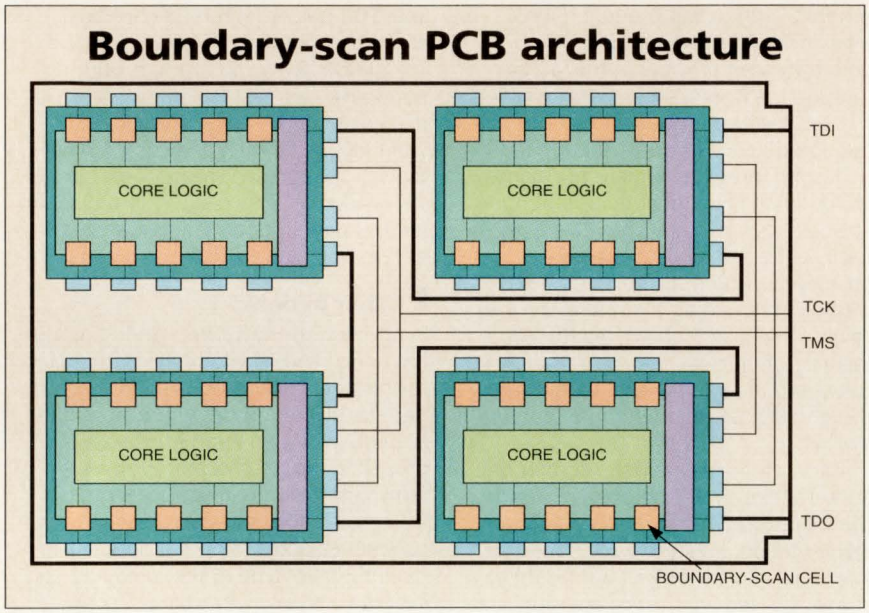
Ultimately, electronics manufacturers will adopt 1149.1 design and test because of the overwhelming economic and competitive benefits. These advantages make boundary scan much more than just a testability technique. It promises to be the most significant factor driving board test economics in the 1990s. And it may well be the third major wave in the history of board test, following functional board testing in the 1970s and the rise of in-circuit testing in the 1980s.

Mark Myers, product manager, Assembly Test Division, Teradyne, Boston, MA

ary scan can alleviate at least part of the problem."

In addition to relieving the design engineer of the burden of cramming test points on an already-crowded PCB, boundary scan can also reduce the time it takes to develop test vectors for complex boards. Assuming that the complex components on a board, such as the microprocessor, have already been functionally tested to make sure they work by themselves, boundary scan can ensure that the part is properly soldered on the board. According to some ATE vendors, these boundary-scan strategies can potentially shave valuable time off design and test cycles, making the technology worth the investment.

"Let's say you want to write test vectors for a 386 to see if you have opens, shorts or stuck-at faults," says Brian Miller, product manager at Teradyne (Boston, MA). "The average time that our test services people would quote to do that is about eight weeks, at a cost of $15,000. But if you took a more complex chip, such as the 486, and it had boundary scan, you could use our test pattern generation software and get the same level of fault coverage in about eight hours. If the silicon vendor gave us the boundary-scan description language (BSDL) files, it would take less than two hours. If someday you could have a board with 100-percent boundary-scan components on it, it's not unreasonable to think about an order of magnitude of difference in the test-development cycle."



Within a PCB assembled from several ICs, the boundary-scan registers for the individual components can be connected in series to form a single path through the complete design. The path, which surrounds the core logic, provides test data input (TDI) and test data output (TDO) connections, and appropriate clock (TCK) and control signals (TMS). In such an arrangement, test data can be shifted through the boundary-scan path from TDI to TDO to achieve node testability. Each boundary-scan cell can capture data on its parallel input, update data onto its parallel output, and serially shift data to its neighbor.

Automated pattern generation

If such time-to-market rewards are to be realized, boundary scan must be embraced by board design and test engineers, who in turn will pressure silicon vendors to implement it. To entice designers to use boundary-scan components, companies such as Teradyne are automating the test pattern generation portion of the design cycle for boundary-scan parts. The company's Victory software, for example, automatically generates in-circuit test patterns for boundary-scan devices. For networks of boundary-scan parts, Victory generates interconnect test patterns that deliver 100-percent pin-level fault coverage. The tool also lets you use the scan path to test the internal logic of boundary-scan devices, and to test non-boundary-scan devices by using the scan cells connected to the boundary-scan inputs and outputs as virtual channels.

Tools such as Victory get their knowledge of a device's boundary-scan circuitry from a model written in BSDL, a subset of VHDL that's tailored to the 1149.1 standard. It offers a standard syntax for defining the topology of the test access port (TAP) and boundary-scan register, including which boundary-scan cell corresponds to which physical device pin.

In a complex device such as a microprocessor, the correlation of the BSDL description to the actual implementation in silicon must be documented correctly, or the resulting BSDL file can do more harm than good. Intel (Santa Clara, CA) recently enlisted support from Hewlett-Packard (Loveland, CO) to help debug BSDL files for the company's 486 microprocessor. Intel plans to publish these files on public bulletin boards such as Compuserve, but first needed assurance that they would be as accurate as possible. HP was chosen for the task because the company was responsible for developing the BSDL standard.

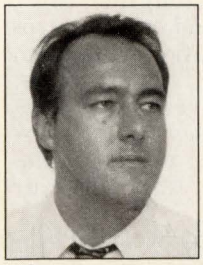
"When you create a boundary-scan test, you create thousands of test vectors," says Stig Oresjo, applications engineer at HP. "It's of prime importance that your BSDL file describes how the boundary-scan chain has been implemented in the component. Because it's a map between the cells and the I/O pins, and there are large vector sets in a complex component, it's important to verify the correct description."

Although the BSDL files for complex devices must be written and debugged with care, one thing is certain. When silicon giants such as Intel start making their BSDL files public and begin implementing boundary scan in their devices, widespread acceptance of the boundary-scan standard is imminent.

Limited use, but useful

For the present, most designers and test engineers are content to use boundary scan to check for open solder connections, shorted solder bridges and devices whose pins are stuck at one or zero due to grounding or shorting to power pins. This rather limited use of the technique might seem like a lot of work for little return, but board manufacturers are convinced that it's worth the effort. "When you're designing boards for military and aerospace applications like we are, fault cover-

DFT is crucial for complex PCB designs



The main strategies for printed circuit board (PCB) test and fault diagnosis are functional test, in-circuit test and boundary scan. Any design-for-test (DFT) considerations must be based on the test strategy that's to be used.

Functional testers make use of the board's edge connectors to drive the circuit's inputs and monitor its outputs. With this method one is obliged to create a unique set of test vectors for each board. Creating these vectors may become excessively expensive as the complexity of the board increases.

In-circuit testers verify the functions of components in situ, on an individual or cluster basis. Creating in-circuit test fixtures for boards with lead-through-hole components mounted on a single side is relatively easy. Circuit boards using surface-mount technology (SMT), however, may create problems for in-circuit test, especially when the components are mounted on both sides of the board. In-circuit DFT considerations include providing sufficient and accessible test points and ensuring that each component can be isolated and tested independently. A component can be isolated by forcing any devices driving it into a tri-state condition.

Boundary scan to the fore

The increasing complexity of components and the introduction of SMT, with its limitations in testability access, have proved to be major driving forces behind the use of boundary scan. All types of scan technology have benefited from being incorporated into logic synthesis, but typically this has only found application in ASICs.

Until recently, the support tools needed to successfully use boundary scan in the PCB realm haven't been available. There's a world of difference between a prepackaged demonstration and the real-world application of a tool.

Although there are some powerful in-house tools, it's only recently that commercial boundary-scan tools have become sufficiently mature for use in the PCB arena. In addition, there's a scarcity of off-the-shelf devices that contain support for boundary scan.

Intergraph, a manufacturer of workstations and associated software, and Intergraph Electronics work together to produce Intergraph systems. These workstations are based on the latest technology, which mandates DFT strategies. As an example of this technology level, consider an 11 × 14 in., multilayer, ultra-high-density, double-sided SMT assembly with over 1,000 devices (102 of which are GaAs), more than 10,000 soldered joints and over 16,000 vias. The via and pad dimensions are 0.016 and 0.030 in., respectively, for through-vias, and 0.010 and 0.020 in., respectively, for blind and buried vias. The board runs at 75 MHz on fiberglass.

Beginning with the concept

At Intergraph, DFT begins at the conceptual stage of the design. The appropriate test strategy is determined by the test engineering team in conjunction with the design team. The test strategy selected then determines the DFT requirements.

Although individual components may be supplied with extensive specifications, there are few published industry specifications that cover the fitness and suitability of materials and components for specific SMT assembly processes. The component engineering team selects component packages for manufacturing process compatibility, including such factors as lead form, package type, lead plating thickness and materials, and operating temperature tolerances. This level of up-front specification provides the receiving department with the data needed to make decisions as to whether or not to accept or reject components and materials.

The component engineering team also specifies the preferred presentation format—that is, the packaging in which the components are to be delivered to the manufacturing group. This ensures that all parts are in a format compatible with the automated manufacturing process, as well as the automated component test process.

It isn't sufficient to develop test procedures that work only with boards that have just been populated. The test procedures must also be appropriate for field returns which have, for example, heat sinks attached to the components.

Multilayer, double-sided, ultra-high-density SMT boards typically have major problems providing access points for in-circuit tester pins. While boundary scan certainly offers some attractions, the scarcity of off-the-shelf boundary-scan devices, and the accompanying overheads of increased gate count and propagation delays, often prove to be deciding factors. Also, in-circuit test is a known and mature technology, and provides the advantages of instant and accurate diagnostics, 100-percent short fault detection and the ability to test analog components.

Since in-circuit is currently Intergraph's test strategy of choice, Intergraph Electronics provides Intergraph with an in-house tool. The PCB-Engineer post-layout database contains all necessary information pertaining to the locations of components on both sides of the board. The database also has information about those components with heat sinks, and about required test-point clearances for components both with and without heat sinks. By examining the PCB-Engineer database, the in-house tool automatically extracts test-point locations for in-circuit test. The tool takes into account component locations, test pads, throughhole vias, and blind vias on both sides of the board. Also, in conjunction with PCB-Engineer, the tool is used to ensure that the positioning of any hand-wires won't affect test-point access.

The test engineering team provides the design team with DFT guidelines; it's also involved in all aspects of the design process to ensure that nothing slips through the net. An example of in-circuit DFT guidelines is the ability to take control of the clock distribution network. With respect to the clock, design guidelines ensure that multiple pipeline stages aren't driven from the same clock branch. ASICs are designed with one pin tied to a soft pull-up. By controlling this single pin, the in-circuit tester can cause all of the ASIC's outputs to go tri-state. Similarly, in the case of PLDs, either an extra pin or an unused state is utilized to cause all the PLD outputs to go tristate.

With the growing use of MCMs, both Intergraph companies are actively pursuing hybrid solutions combining in-circuit test and boundary scan.

Clive Maxfield, a member of the technical staff, Intergraph Electronics, Huntsville, AL

age has to be very high," says Mike Howard, staff engineer at the Hughes Radar Systems Group (El Segundo, CA). "By using boundary scan whenever possible, we can test for manufacturing defects which account for a significant portion of board failures. Boundary scan lets us know whether the problem is in the design or in the manufacturing process of the PCB."

This ability to separate manufacturing defects from design faults is currently boundary scan's chief selling point. Some companies, such as John Fluke Manufacturing (Everett, WA), are banking on boundary scan's acceptance at the bench or field service level. Fluke has been bundling boundary-scan diagnosis capabilities with the PM 3580 logic analyzer from Phillips (Eindhoven, the Netherlands). By connecting the logic analyzer to the boundary-scan ports on a PCB, you can check for shorts, opens or missing components on a prototype. The latest release of boundary-scan software, the PM 3705 BST Explorer, works in conjunction with either a notebook PC or the Phillips logic analyzer to debug boundary-scan boards.

By emphasizing the use of boundary scan to find manufacturing faults, Fluke and Phillips are hoping to convince designers that boundary scan doesn't have to be used only for sophisticated diagnostics. "We envision using boundary-scan analyzers in field repair," says Bob Roth, product marketing manager at Fluke. "This will let field engineers quickly test and swap out defective boards or make simple field repairs. It can also help the people in the repair lab isolate and correct faults on boards returned from the field."

As attractive as boundary scan appears when it's presented in such a flattering light, some engineers are concerned about the trade-offs, either in device and board real estate or in performance. Although boundary scan isn't exactly free, many EDA and silicon vendors are assuring the design community that the penalties are slight when compared to the gains in testability and overall design quality. "On a typical device, you're only talking about a 300- to 500-gate penalty in the logic and about eight to ten gates per I/O pin," says Kelly Gomes, product marketing manager at Synopsys (Mountain View, CA). "Some ASIC vendors have come up with ways to reduce this even further, but in terms of overall percentage of silicon sacrificed, it's not much. By using boundary-scan devices, you can concentrate on debugging the functional side of your design because you've eliminated manufacturing faults as a cause of failure."

"In the past, PCBs were testable because you had access to every node on the board," says Pete Lwin, product line marketing manager at Schlumberger Technologies (San Jose, CA). "But today's complex PCBs make it difficult for even the newest board testers to successfully test every critical path. It's not hard to determine whether a PCB is good or bad, but no one wants to simply discard an expensive board because it didn't pass an in-circuit test. That means extensive diagnosis to determine the cause of a failure, and that means essential links to vital design data."

For its part, Synopsys has released the Test Compiler Plus, which includes boundary-scan synthesis in its automatic test-pattern generation (ATPG) capabilities. Using this feature, you can synthesize the TAP controller, control circuitry and I/O pads, and can automatically connect JTAG to your design.

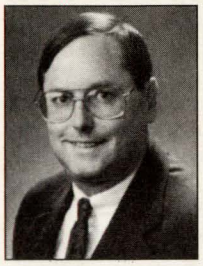
Synopsys has also developed synthesis for partial scan into IC designs. Partial scan is an approach to IC testability that turns some of the sequential elements in an IC design into scan registers or elements that are controllable and observable. This is a variation of full scan, where all of the sequential elements are scannable. According to Gomes, "Partial scan is attractive for design applications that are tightly constrained by performance and area requirements—for example, a CPU that can't afford any performance impact on a critical path."

Stumbling blocks may crumble

Through the efforts of EDA vendors such as Synopsys, the stumbling blocks to DFT may eventually crumble, but not without concerted effort on the part of silicon vendors and ATE manufacturers as well. Cadence Design Systems, for example, has joined the ranks of EDA vendors providing test synthesis tools. At last month's International Test Conference (Baltimore, MD), Cadence unveiled three tools, the Test Synthesizer, Test Simulator and Test Generator. Although these tools target ASIC designs, the increased availability of ATPG software will ultimately make circuit boards more testable, since both custom and off-the-shelf ICs routinely sport scan-chain testability features.

Until the day comes when most components offer boundary-scan capabilities (which is, at best, a way off), designers will have to get creative about using what test access they have. Analog components, for example, aren't generally amenable to boundary-scan techniques, so their networks will require physical access if analog in-circuit testing is necessary. These complications require that designers and test engineers alike communicate their test needs to layout engineers, so that all or most of the PCB can be tested. By designing for access, the needs of test can be met without dramati-

New test strategy needed for complex PCBs



How does an engineering department design a PCB for testability when it contains 24 layers, 100 208-pin quad flat pack ICs, 8,000 nets, 1.5 miles of wire, 20,000 holes, and a 6-mil trace pitch?

That was the challenge facing Quickturn Systems in designing the new Enterprise Emulation System, a very complex hardware emulation system in which testability and reliability are paramount. The Enterprise Emulation System contains up to eleven PCBs (emulation modules), each with more than 100 ICs interconnected through a programmable backplane. A fully populated system contains more than 1,200 complex ICs, which must all be tested and proven to function correctly to provide the reliability demanded by users. One criterion of the board design, then, was to come as close as possible to 100-percent testability.

Team approach

Quickturn determined that the testability problem could only be solved by developing a new set of test strategies. The first thing the company did was form an interdisciplinary team consisting of company engineering and manufacturing groups and key vendors, the latter being: the layout specialist (Shared Resources, San Jose, CA), the board fabricators (Acsist Associates, St. Louis Park, MN; Ambitech, Chatsworth, CA; and Multek, Irvine, CA); and the assembly contractor (Ceridian, formerly part of Control Data, Bloomington, MN). This group was charged with making the emulation modules manufacturable at a very high quality level; it also facilitated a team approach in solving any problems that might crop up.

The team determined very early in the design cycle that testability would be a key success factor. Since faults are more complex and difficult to clear if they're found late in the test sequence, it made sense to concentrate on early error detection. The first goal, then, was to find errors and problems as early in the test process as possible, resulting in easier fixes that would save valuable time and effort.

Since most faults are manufacturing defects—interconnect problems, shorts and opens, and the occasional bad component—the first portion of the test strategy concentrated on developing a strong bare-board test. Testing to the actual netlist instead of using the more common golden board method verified that the design's netlist was correctly implemented and that systematic errors were found. Much care was taken with layout to assure that in-circuit test pins could contact all 8,000 nets on the board. And obviously, it was necessary that large enough commercial test systems were available to handle the design.

Special considerations were also incorporated into the design. For example, except for power and ground, no pins (such as enable pins) are tied directly to the V_{CC} and GND planes in the board. Vias are used on all traces to make sure the tester can reach all signals from the bottom of the board. And surface-mount pads are routed to via holes arranged on a regular 50-mil grid to allow contact with the bed-of-nails tester and provide access to all pins.

System test diagnostics take less time to run, even though the new product is an order of magnitude more complex.

In-circuit test

The next step was to develop an in-circuit test for the assembled board. A major problem was encountered, however. There was no commercial in-circuit test system with enough pins to test the fully wired board using standard techniques. The solution to this problem was in the design of the board itself.

The Enterprise board design consists of large numbers of full-custom ICs designed by Quickturn and of Xilinx FPGAs. The custom chips were designed with a fully functional JTAG implementation, and the FPGAs were also loaded with JTAG circuitry. Special care was taken with the circuitry to allow parallel functional testing of the custom chips and FPGAs. Since a complete system may have thousands of chips, it's impractical to test them all individually. By injecting test vectors to all ICs in parallel and monitoring the T_{DO} pins while running an internal test, the chips could be verified very quickly. The T_{DO} pins should behave in the same way for all chips on a clock-for-clock basis.

If any chip is different, an internal error is indicated. Many of these test vectors are the same as those developed by chip vendors for testing fabricated chips on their IC testers.

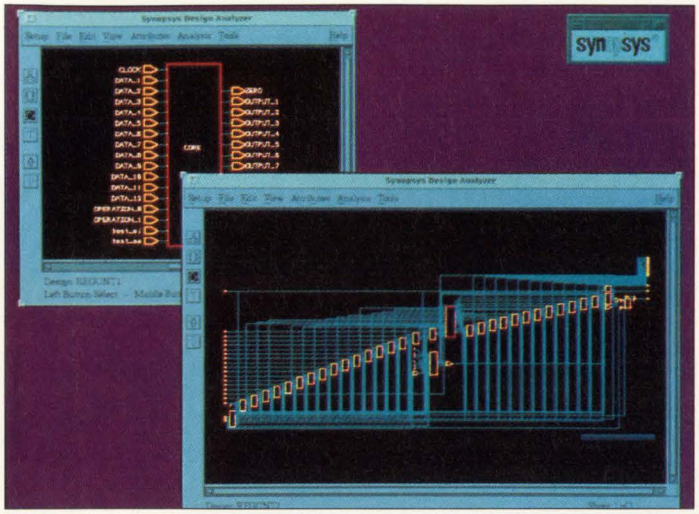
The pin limitation problem was also solved thanks to JTAG. Ceridian test engineers exploited the JTAG boundary scan features of the design and invented a clever signature analysis-based in-circuit test strategy that reduced by two-thirds the number of test pins required to test the board and isolate its faults.

As part of this strategy (and prior to chip availability), Quickturn did a dry run with dummy boards to give all vendors process experience. This let many process problems and mechanical fixturing issues be solved before the prototype boards were even built.

Verification of the emulation modules in the finished system was the next concern. The Enterprise Emulation System is designed to take any circuit netlist and implement it in reprogrammable hardware. The system includes an internal pattern generator and logic analyzer to assist in debugging the user's design. Using these features, the test engineers had the emulator test itself. Test circuits were loaded into the system, exercised with the pattern generator, and, using the logic analyzer, the actual results were compared with the expected results.

Reliability issues were addressed simultaneously with test issues. The exchange of ideas and information between Quickturn and Ceridian test and diagnostic engineers allowed exploitation of a number of strategies, and the team test effort produced excellent results. JTAG simplified the diagnostic routines, and Quickturn added a suite of built-in diagnostic tests that can be run to test the system before starting the emulation process. The system test diagnostics take less time to run than on an earlier version of the product, even though the new product is an order of magnitude more complex.

Dug Stewart, vice-president of manufacturing, Quickturn Systems, Mountain View, CA



Synopsys' JTAG synthesis tool automates 1149.1-compatible synthesis and insertion into ASIC designs (left). It synthesizes the test access port (TAP) controller, control circuitry and boundary-scan register (right) based on parameters defined in a menu-driven user interface.

cally impacting a PCB's design. With clever manipulation of layout and routing, mixed-technology boards can make use of scan chains provided by the I/O pins of a JTAG device, and traditional ATE methods can be incorporated whenever physical access is possible.

Other uses

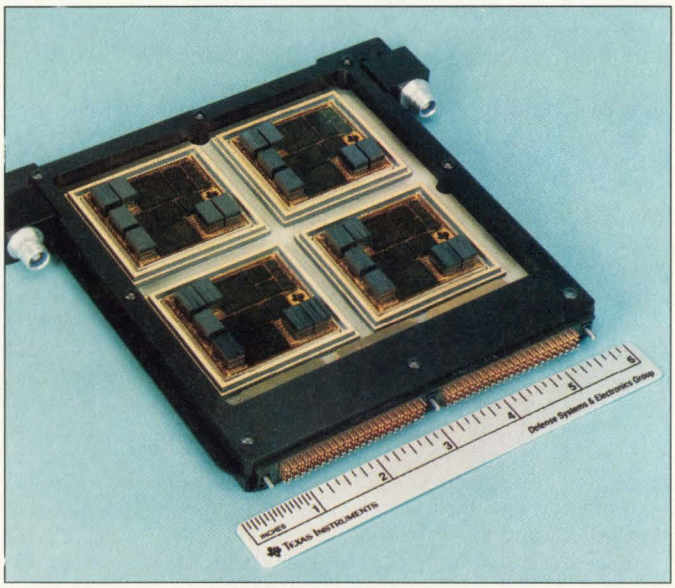
So far, most design and test engineers are using boundary scan to find and correct manufacturing faults, but there are some proponents of the standard who believe it can do far more. The engineers at Texas Instruments (Plano, TX) are using 1149.1 for design verification of complex embedded systems. "TI's position has always been to push JTAG beyond being a low-level exercise for finding interconnect problems," says Pete Fleming, manager of the test technology center at the company. "Our Asset software has always been aimed at providing an interactive debugger where you group bits of your designs into virtual registers, memory buses, address buses, and data buses and manipulate them in a functional manner. This approach lets you manipulate the logic one scan at a time, see what the state is, map it back into the register, and use it for design verification."

The embedded system that TI designed, dubbed Aladdin, is a 100-MHz, high-density parallel processing computer. It employs silicon-on-silicon packaging and three-dimensional memory packaging to achieve 500-Mips of scalar processing performance and two GFlops of floating-point processing performance, all packaged in a 4.5-in. (diameter) cylinder less than 6-in. high. TI used its Asset tool to generate scan tests to verify test bus operation, scan path integrity, internal register access, core logic operation, and IC-to-IC interconnects.

"We were able to find some problems in the design that never showed up during simulation," says Wayne Daniel, an applications engineer at TI. "We also had some catastrophic failures on ASICs that were caused by hardware scan errors. Occasionally, one or more bits caused bad instructions or data to be scanned into the unit under test. A scan error had placed the ASIC in test mode and enabled a boundary-scan I/O direction control cell. This condition caused the device to back-drive a memory port, which quickly led to overheating and caused a power-to-ground short. One painful lesson we learned was about the lack of fault tolerance and fail-safe procedures in 1149.1. While absolute control is required for boundary-scan tests, the standard test bus could be enhanced to reduce the probability of scan errors that could cause physical damage."

While TI's experience certainly shows the limits beyond which the IEEE standard can't be pushed, it will undoubtedly be a while before the average design team uses JTAG so exhaustively. Most designers are taking a wait-and-see approach while innovations such as TI's are published and more devices host JTAG ports. Until boundary scan comes of age, these design and test engineers will rely on standard methods of software simulation for portions of their designs, as well as debugging of the prototype and in-circuit testing.

"Right now there are two camps," says Dan Caldwell, manager of test technology at Plexus (Neenah, WI), a contract electronics manufacturer. "There are people who embrace boundary scan as much as they can, and there are people such as us who feel we can get our product to market faster using other DFT methodologies, along with exhaustive simulation and debug. About 90 percent of the VLSI devices out there don't have boundary scan, and we don't think it makes sense to design ASICs with it if nothing



Engineers at TI (Plano, TX) used boundary scan for design verification as well as in-circuit test on the Aladdin 32-bit parallel processor. Shown here is an Aladdin Basic Processing Module (BPM), which hosts four multichip modules. Each BPM provides a peak throughput of 100 Mips, simultaneously with 400 MFlops of vector processing. The Aladdin system, which includes five BPMs, will fit within a 45-in.^{3} cylinder that's approximately 3-in. high and 4-in. in diameter. It will be used primarily for automatic target recognition systems for intelligent weapons and avionics.

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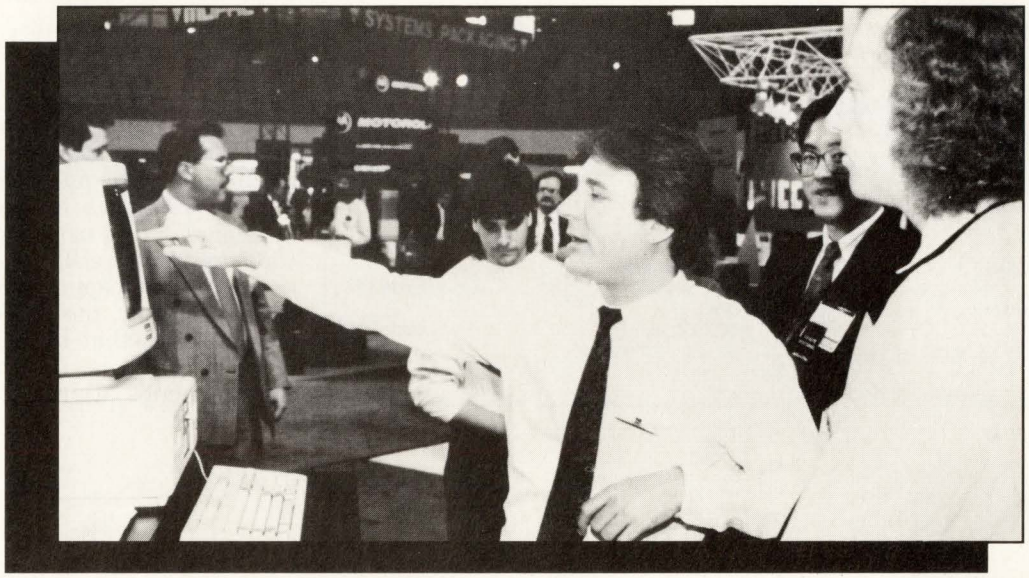

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else on the board has JTAG. We're positioned to use boundary scan when it's more accessible, but right now our methods work fine."

Finding other ways

In addition to traditional design methods of ensuring PCB quality, some design and test engineers are pursuing alternative techniques to test their boards. One such method uses FPGAs to get to inaccessible areas on complex PCBs. Lattice Semiconductor (Hillsboro, OR) has introduced a family of non-volatile, in-system, programmable, LSI (ispLSI) devices that it uses to improve PCB testability. The devices use TTL-level signals for programming, and a simple five-wire interface for programming control. The programming circuitry is embedded in the ispLSI device, which reduces the amount of dedicated circuitry required for testability.

"One of our customers used our devices on a 15-layer, 23 × 28-in. board with surface-mount devices on both sides," says Jock Tomlinson, field applications engineering manager at Lattice. "They used seven of our devices on the board, but instead of programming them for their intended logic functions, they programmed a digital pattern into the FPGA to test sections of the board. One of these is a DRAM controller, which they use to force test vectors into the DRAM bank. They can program it for its normal function after the test."

Tomlinson also says that customers use the parts to isolate devices on the board. By setting the ispLSI enable pin low, all pins on the device are tri-stated, effectively shutting it off for diagnostic purposes.

Even with such innovative ways of implementing DFT strategies, the core problem is still getting design engineers to accept new responsibilities. Certainly, the success stories of companies that have implemented such strategies are bound to get management's attention. But some

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vendors caution against making grandiose claims for DFT methods, or technologies such as boundary scan will end up on the garbage heap of buzzwords and broken promises.

"My big worry is that upper management will invest in boundary-scan parts and methodologies and expect miracles," says Mark Myers, product manager at Teradyne. "They might start looking for test times to immediately be reduced by one-third or one-half. But in mixed technology boards, the testing problems can get difficult in a hurry, particularly if everyone is just learning how to use the new methods. If there's too much pressure on design and test departments to shorten design cycles because someone upstairs thinks boundary scan or some other DFT strategy is a panacea, then there will be a backlash from engineers, who are admittedly reluctant converts to begin with." ■

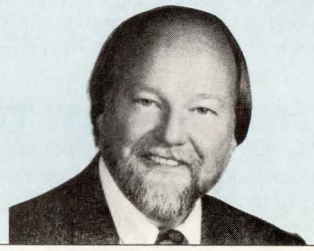
Postscript

Until recently, bringing up the topic of DFT was a sure-fire way to make a design engineer's eyes glaze over. Nowadays, however, the subject often starts intense debates about overworked designers, untestable systems and shifting management roles. The fact is, testability has been playing catch-up with technology innovations for years, but most companies were willing to let the test department scramble for solutions at the back end of the design cycle. But recent developments in IC packaging and MCM technology, as well as increased demands for wringing more performance from smaller systems, are sounding the death knell for the old way of doing things.

At September's International Test Conference in Baltimore, the commitment to DFT was evident. EDA vendors were touting the latest in ATPG software, ATE vendors were displaying links to design tools, and papers were presented that were aimed at the new breed of design engineer who incorporates testability into a design.

These developments are all welcome, but a key ingredient is missing—the commitment of upper management to implementing DFT strategies as part of a corporate philosophy. Until design engineers are convinced that they're part of a team whose goal is to get a reliable, manufacturable product out the door, then the "over the wall" ways of the past will stay with us.

Mike Donlin



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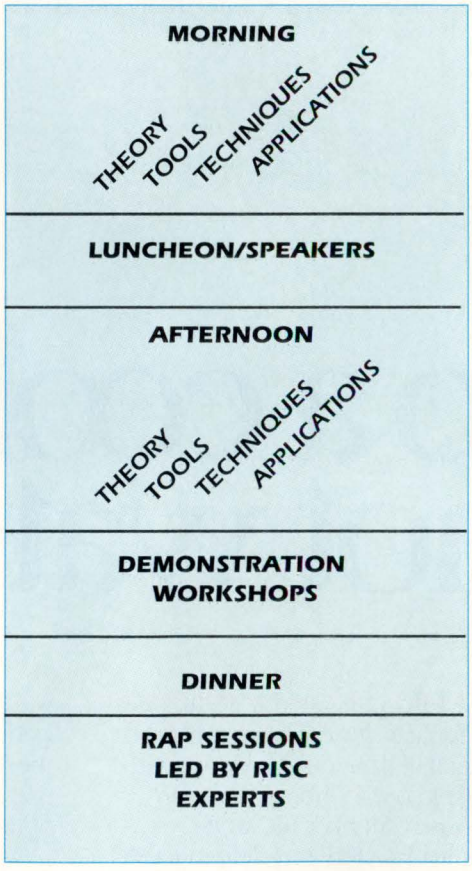

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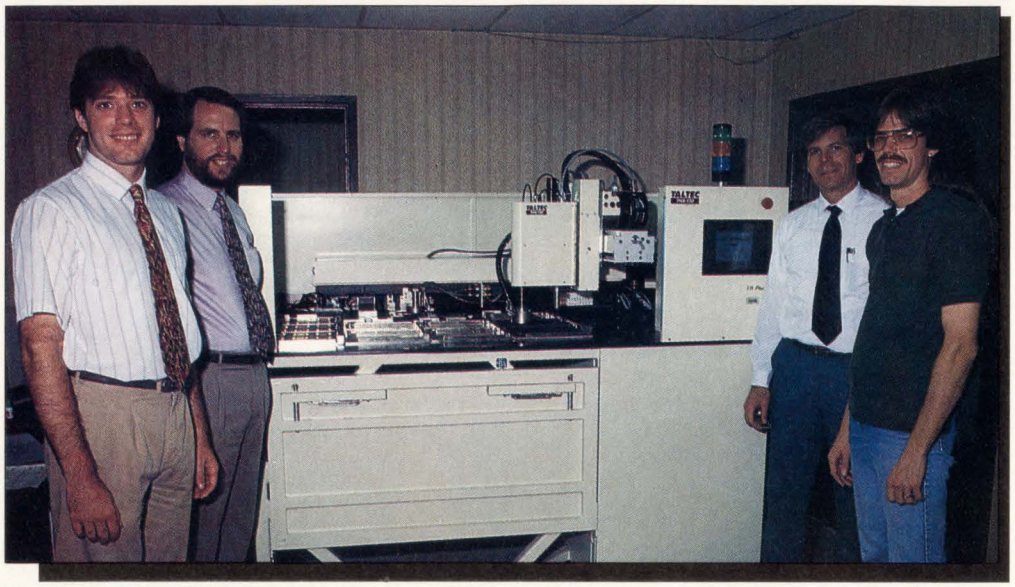
CIRCLE NO. 56

Event-driven strategy wins for robot test handler



The Taltec design team from left to right: Dan Eliason, software engineer; Jeffrey Schaffer, consultant to Taltec; Tom A. La Rovere, president; and Marc Van Dyke, member of the technical staff at Vitesse Semiconductor. In the center is Taltec's THS-120 robotic test handler. The machine was built to support special Vitesse requirements. Because of its flexible software architecture, the THS-120 can handle a wide variety of semiconductor package types without any special mechanical changes.

In 1988, engineers at Taltec (Goleta, CA) worked with a customer to develop a robotic pick-and-place machine, one that could place surface-mount devices—from very small chips to large devices with hundreds of 25-mil pitch leads—on a very large PCB. Originally a consulting firm, Taltec saw this project as an opportunity to craft its own system platform, one it could migrate to other projects in the future. Taltec's designers created a general system architecture for robotics based on a distributed control scheme. To this core technology, custom features could be added as required. After building several machines for different customers, Taltec found an opportunity to use its technology in the tester/handler business.

At the heart of this architecture is what Taltec calls a WorkCell Controller (WCC), a PC/AT-based computer from which Taltec's software controls the various hardware subsystems of the robotic system. These subsystems include a robot controller to control the robot in real time and a vision processor to control the vision functions in real time. Taltec's strategy was to use standard off-the-shelf I/O hardware while investing its development efforts in the software architecture needed to glue it all together.

No simple task

"We enhanced the software to make it more flexible for tester/handler needs," recalls Tom La Rovere, president of Taltec. "The job of the test handler robot is simple: pick up an untested part from the tray, put it into a test socket, communicate with the

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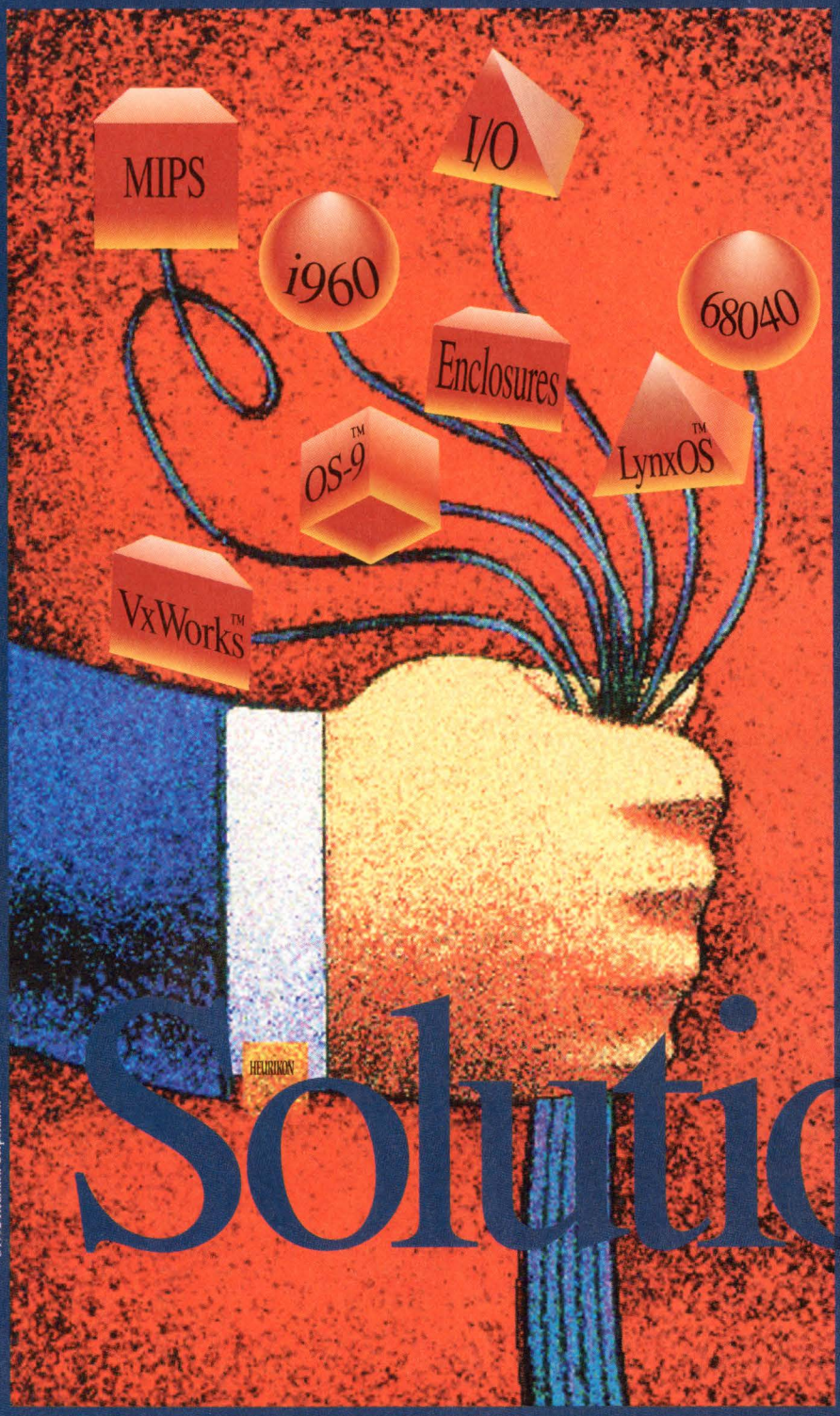
Jeffrey Child, Senior Editor



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Taltec's THS-120 test handler: how it works

The major functional blocks of the THS-120 are a robot controller, the WorkCell Controller (WCC) and various I/O modules. The WCC is a 33-MHz 386 PC/AT that Taltec builds from off-the-shelf parts which fit into a 19-in. rack. A parallel multiplexed interface (PAMUX) connects the WCC to the I/O modules. Those modules provide opto-isolated analog and digital I/O over which the WCC communicates with the robot and the touch screen operator console. Because as many as eight RS-232 lines are connected to the WCC controller in a typical system, an intelligent I/O card resides in the WCC to handle interrupts.

THS-120 in action

A typical sequence begins when the WCC sends a start signal to the customer's test equipment. The test equipment runs its test and returns with a "bin" signal and a test signal. The THS-120 latches up to the signals, making them available to the robot, which determines where it should put the part. As soon as the end-of-test signal returns from the customer's tester, the test press is retraced, permitting the robot to unload the part from the test socket and load the next part.

Once that sequence starts, the robot handles these functions locally, and the WCC, for the most part, sits back as a monitor, waiting for some event such as a bin going empty or an output bin becoming full. When such events occur, the robot informs the workstation controller and the WCC is programed to take effective recourses.

Three-part software

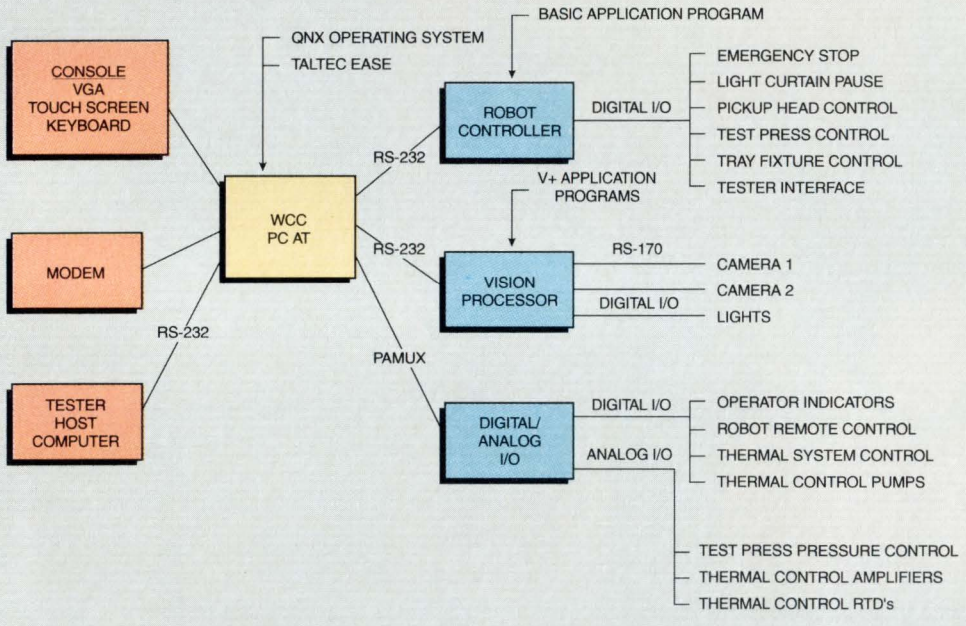
The THS-120's software consists of three major elements: the WCC software, robot control software and vision processor software. On the WCC resides the QNX real-time operating system and Taltec's Event Action Software (EASe).

A table-driven approach is used. When a customer selects a particular test protocol and part to be tested, for example, that data is held on file by the WCC. The robot receives this data and uses it to set up the appropriate conditions for robot control.

While the EASe software is written in C, code for robot control is in a BASIC-like language providing typical robot commands such as "Move to Point." Such commands control the trajectory and type of motions performed by the robot. Logic expressions such as WAIT and IF are also used in this software.

The vision system is programmed in a Pascal-like language. Again, a table-driven approach is used. Tabular data is sent to the WCC, which forwards it on to the vision processor. The vision processor then runs its own program. It sends back predefined messages to the WCC, such as error codes or information about where the center of the part is.

Taltec's THS-120 pick-and-place machine: how it works



customer's test equipment, receive from that equipment a sorting signal, and then place the part into an appropriate sorting tray.

"Very straightforward and simple, or so we thought," La Rovere laughs. "Unfortunately—or, I guess, fortunately for us—it's not that simple. With this type of robotic system, and in this type of application, it's not the task that's difficult. It's the recourses that must be dealt with. By recourses I mean the unexpected events coming from the environment that you have to decide how to respond to. The operator, for example, does something you can't predict. That's where the simple structure decomposes into something much more difficult. That has driven us to orient our software to deal with those kinds of issues and we developed a flexible software architecture."

Customer input crucial

Taltec's most recent version of its test-handler machine was greatly influenced by input from its latest customer, Vitesse Semiconductor (Camarillo, CA). Specializing in

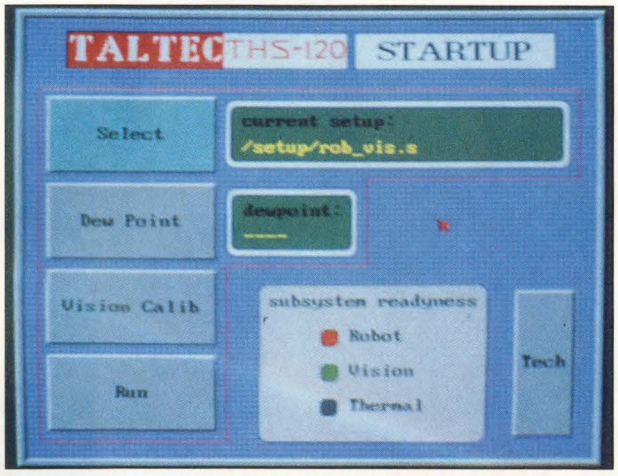
high-performance GaAs ASICs, Vitesse wanted to boost its manufacturing efficiency by automating the process of testing its ICs. The Taltec machine also had to handle Vitesse's wide variety of custom packages, as well as the special power requirements of its GaAs chips.

After rating the available test handlers on the market, Vitesse had difficulty finding a machine that fit all its requirements. "We wanted a machine that could deal with various packages, a lot of which weren't defined at the time," says Marc Van Dyke of the technical staff at Vitesse. "We test very high-speed parts with high pin counts, so the test equipment we buy is some of the most expensive on the market. As a result, our test floor operations are very costly. So we wanted to keep the setup cost and the changeover time between package types as small as possible."

According to La Rovere, "As an ASIC vendor, Vitesse builds a variety of different products. They needed to be able to handle different packages in the system with a lot of different mechanical fixtures. We were also incorporating a vision system programmed to look at the different devices, and place them accurately into the test socket."

One of the initial design decisions Taltec made was in the choice of QNX from Quantum Software Systems (Kanata, Ontario) as its operating system. Jeffrey Schaffer, a consultant to Taltec, played a major role in OS-related software design. He considers QNX to be an excellent choice. "Message passing is the key," he says. "Using a multitasking operating system lets us write individual tasks to model the sections of the machine, so the natural modular structure of the software falls out from designing the machine that way.

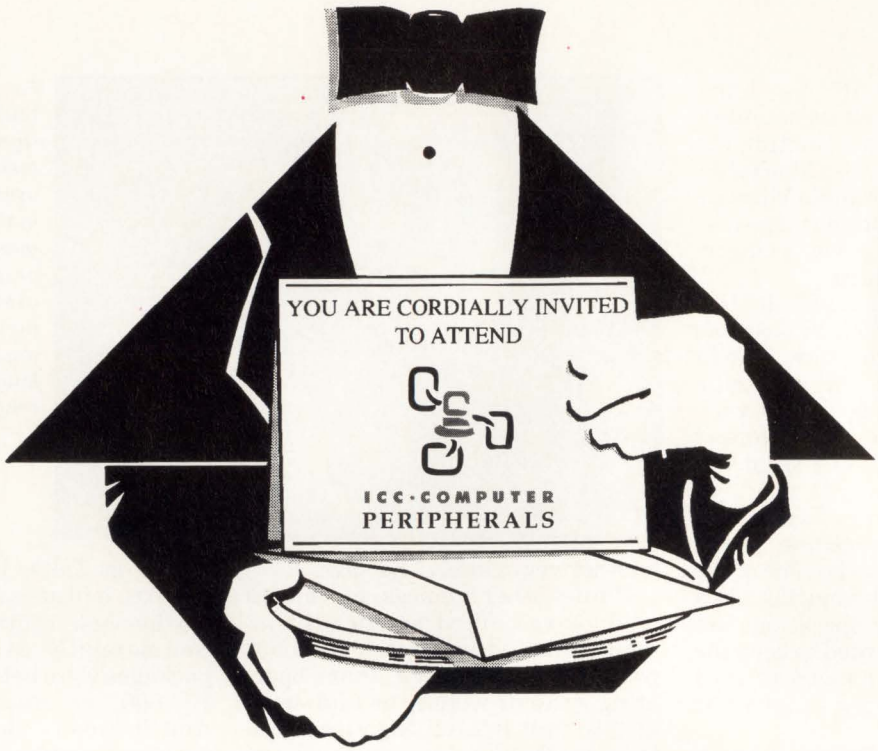
"Earlier, Tom [La Rovere] mentioned error recourse as motivating the event-driven philosophy for design of the system. It turns out that we handled almost every interaction based on this event-driven philosophy. Even in the software we designed ourselves, the Event Action Software (EASe), events that occur are modeled as messages," adds Schaffer. The advantage of this approach was brought home when the team started to draw block diagrams describing hardware and software. "We saw that the hardware and software really mirror one another very closely," he says.



For the THS-120's touch screen, Taltec designers chose to implement the graphical user interface software in their own script language. This makes it easy to adjust to the user interface; it can be done by simply changing a few lines of script language, rather than rewriting C code.

While other choices for an OS might have sufficed, and Ready Systems' VRTX and Integrated Systems' pSOS+ were considered, those operating systems weren't as high-level as QNX. "QNX is a full, high-level system, much like an early UNIX, yet much more refined," says Schaffer. "Our event-driven control scheme fits very well with the message-passing capabilities of QNX."

Just as Taltec bought an off-the-shelf OS, it also could have bought an off-the-shelf control software. But commercially available software packages were between $25,000 and $50,000, too much for this project. And it wasn't clear that a third-party software package would suit the project's needs anyway. That led to the decision by the Taltec team to develop its own director scheme to run the WCC. The result was a soft-



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CIRCLE NO. 59

ware package Taltec calls Event Action Software, or EASe.

The challenge was to create a scheme that was simple for the user, and yet that was still complex enough to let the you work at a high level. For Taltec's earlier pick-and-place machines, that meant finding a way to sequence the OS, and to respond to events and generate recourses.

Director controls system

At the heart of the entire software system—and, therefore, of the entire system—is the Director. The Director controls systemwide behavior. This control is critical in cases where an error occurs that involves more than one subprocess. If the part doesn't get placed right, that error involves the robot, for example, but it also involves the vision system, which has to reinspect the part.

Each hardware subsystem of the machine has its own software program. There's a program that deals with the PAMUX, the digital I/O control points. Similarly, the robot has its own program, which passes event messages over the serial port. "We think of all these messages as events," says Dan Eliason, software engineer at Taltec. "These programs are all capable of generating messages. The PAMUX, for example, watches its input ports; if a certain state change happens, it generates an event."

Besides responding to events from the subprograms, the Director is also responsible for reading a special script language. If you need to make changes in system configuration, you don't have to write any C code. Instead, you rewrite the script. The Director reads the script language, compiles it on the fly, then executes the reaction accordingly. "If a user wanted a light to turn on, for example, when the light curtain was broken, he could just change one line in the script language and it's done," says Eliason. "The customer has the flexibility to make changes, or we can make the change for him."

One change made for the Vitesse product was to replace the ASCII terminal touch screen with a color touch screen. "We had a decision at that point about whether to use the QNX window function calls to do the graphics for the touch screen in a C program," says Eliason. "Instead, we thought we'd try something more flexible, so that if we needed to use a different machine, we could easily do that just by rewriting the actions instead of sections of C code." This led the Taltec team to craft a script language for its user interface as well.

QNX already provides an interface editor that lets you create windows using a mouse, but you still have to write a program to use those windows. "We decided to write a user handler or server that would use a similar script language to the one we use with our Director," says Eliason. "So when the user does something with a window, like pushing a button, that becomes an event just for this user interface. And it has a script language to tie that event to the opening of further windows or generating events from the Director." With this approach, Taltec could keep to its event-driven philosophy.

Lessons learned

As the design progressed, Eliason had some insights about control software structure, and the prospect of using new technologies in future projects. "During this project, we talked a lot about the issue of expert systems," he says. "We surmised that we could use an expert system as a Director. It could determine systemwide things that need to happen based on events that occurred. An expert system operates by scanning lists of conditions; when the conditions are met, it fires the rule or does the list of activities. Our system is structured so that each server is responsible for recognizing things that need systemwide attention.

"One of the things I'd like to explore for the future," contemplates Eliason, "is a sort of event-posting architecture." If an event's important, it gets posted to the Director. But the Director, rather than taking immediate action on the event, can scan its rule list. It could combine the event with other events from other servers to recognize important systemwide conditions.

Would the use of an expert system make any difference in performance? "It's really a philosophical point, because I haven't yet run into an event that we couldn't address with our current architecture," concludes Eliason. ■

COMPUTER DESIGN Technology and Design Directions

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SOFTWARE & DEVELOPMENT TOOLS

Trace issues drive 32-bit emulator choice

Jeffrey Child, Senior Editor

Applied Microsystems has added to its EL 3200 emulator support for Motorola's CPU32 family of microcontrollers. The emulator features a new disassembler technology that correlates instructions with hardware register values and bus cycles. The emulator handles special features of the CPU32 chips, such as dynamic bus sizing and real-time pin reprogramming.

For integrating hardware with software, as well as hunting down the nastiest bugs in your real-time microprocessor-based design, there's no more effective tool than an emulator. But emulators for 32-bit microprocessors aren't cheap. To keep pace with today's fast RISC and complex CISC chips, emulator vendors are forced to outfit their products with advanced and expensive technologies.

Fortunately, designers who can make do without full-fledged emulation can choose from a variety of lower-cost debugging alternatives, such as ROM monitors and instruction-set simulators. But for complex embedded designs, especially those that run in real time, there's no substitute for an emulator.

Trace system most important

Emulators are available for a wide variety of the latest 32-bit CISC and RISC microprocessors. While specifications such as size of overlay memory, breakpoint capability and trace buffer configuration are all significant, you also need to look beyond these numbers to get a true sense of what you're paying for. Perhaps the most important feature to examine is an emulator's trace system. Trace is important for two reasons: first, there are as many different schemes of trace as there are emulator vendors, and trace is one of the key ways emulator vendors differentiate their products. Second, an emulator's trace system and associated triggering usually contributes the most to the total cost of the system.

Richard Jensen, vice-president of new business development at Applied Microsystems (Redmond, WA), agrees that trace is key. "The purpose of trace is to provide visibility into what actually happened in your system against what you planned to have happen," he says. "It's the feature that lets you do deductive reasoning rather than inductive reasoning." Emulator vendors agree on the importance of trace but emphasize different aspects, including the number of trace channels, the intelligence of trace disassembly, trace display, and trace triggering.

One nagging trace issue faced by designers using in-circuit emulators for real-time debugging is that you can't directly examine the contents of a processor's registers. Instead, you have to single-step through the instruction trace, manually calculating the changes in register values.

To address this problem, Applied Microsystems has made some changes to trace disassembly, providing a view of register contents. When the company set out to make disassemblers for Motorola's series of CPU32-based microcontrollers, it wanted to avoid inventing a new disassembler for each member of the family. Drawing on artificial intelligence techniques, Applied incorporated an inference engine in the XICE debugger that controls its emulators. This added intelligence lets the disassembler distinguish among the different chips. As an outgrowth of this new technology, the company has also been able to infer the content of a chip's registers.

The intelligent trace disassembler works by building a model of the processor state, which it modifies as instructions are executed. This provides a history of the hardware register's values and corresponding instructions at any point in the trace. The XICE debugger with intelligent trace disassembly is now offered as part of Applied's development systems for Motorola's 68330, 68340 and 68F333 microcontrollers.

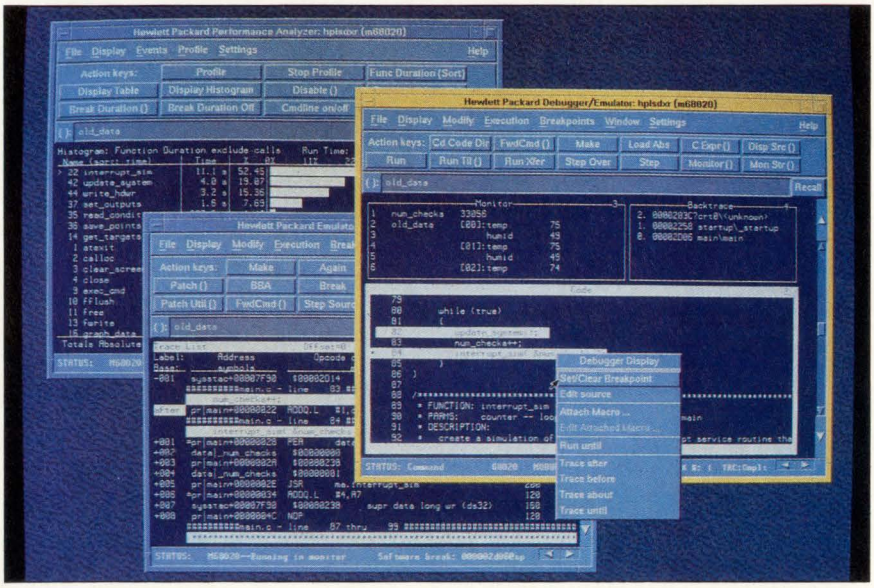
RISC needs more channels

RISC processors, with their pipelined architectures and high pin counts, make life challenging for emulator vendors. The Am29000 RISC processor from Advanced Micro Devices (Austin, TX), for example, has a three-bus architecture that requires from 200 to 250 channels of trace to provide a view of what's happening. More channels are needed than the processor has pins, so an emulator can view not only what's going on inside the chip but everything that's going on around it. "Some emulators force you to switch back and forth between looking at control signals and two buses and looking at three buses and no control signals," remarks Norbert Laengrich, president of Embedded Performance (Santa

Model	Speed (MHz)	Processor(s) supported	Overlay memory (bytes)	No. of hardware breakpoints	No. of break-point levels	Trace buffer depth (bits)	Performance analysis	Price	Comments
Applied Microsystems 5020 148th Ave NE, Redmond, WA 98073-9702 (206) 882-2000									**Circle 301**
CodeTAP CPU32	16, 25	68330, 68340, 68F333	—	4	2	—	no	—	
CodeTAP i960	33	i960CA, CF	—	4	2	8k	no	$7,500	Plugs directly into target device.
CodeTAP 386	33, 44	Am386DX/DXL, i386DX	—	4	2	—	no	$4,995	Plugs directly into target device.
EL3200 CPU32	16, 25	68330, 68340, 68F333	4M	16	4	8/32k × 144	yes	$16,000	Supports dynamic bus sizing, real-time pin reprogramming. Correlates instructions with registers and bus cycles.
EL3200 i960	33	i960CA, CF	4M	16	4	16k × 139	no	$28,575	Supports pipelining, data and instruction cache, burst mode, multiple bus widths.
EL3200 68020/030	33	68020/030	2M	6	4	16k × 144	yes	$24,050	Runs on Sun, PC, VAX; can be accessed via Ethernet.
Embedded Performance 3385 Scott Blvd, Santa Clara, CA 95054 (408) 980-8833									**Circle 302**
SYS29K	25	Am29000, Am29005, Am29050	256k - 2M	50	16	2096	yes	$14,995 - $25,000	Hosted to PC, Sun-3, Sun-4, VAX-VMS, HP9000, Ethernet option.
SYS29K-LYNX	25	Am29000/05, Am 29050, Am29030/35	256k - 4M	50	16	2048	yes	$20,000 - $30,000	Hosted on PC, Sun-3, Sun-4, HP9000, VAX-VMS via Ethernet and high-speed serial interface.
SYS29K-PUMA	25	Am29000, Am29005, Am29050	256k - 4M	50	16	2096	yes	$20,000 - $35,000	Same as above.
SYS29K-TURBO	33, 40	Am29000, Am29005, Am29050	256k - 4M	50	16	8k - 32k	yes	$25,000 - $40,000	Same as above.
SYS33K	25	LR33000, LR33050	256k - 4M	50	16	8k - 32k	optional	$27,000 - $40,000	Same as above.
SYS-R3000	25	R3000, R3000A, R3001	256k - 4M	50	16	8k - 32k	optional	$25,000 - $40,000	Same as above.
SYS-R3051	25	R3051, R3052, R3081	256k - 4M	50	16	8k - 32k	optional	$25,000 - $40,000	Hosted to PC, Sun-4, MIPS via Ethernet or high-speed serial interface.
SYS-SPARC	25	CY7C611	—	50	16	8k - 32k	optional	$25,000 - $45,000	Same as above.
Hewlett-Packard PO Box 2197, Colorado Springs, CO 80901-2197 (719) 590-1900									**Circle 303**
HP64747B	40	68030, 68EC030	0 - 2M	8	8	1k	yes	$9,000 - $24,700	X11/motif-based graphical interface, available high-level debug, real-time software performance analysis.
HP64748A	33	68020, 68EC020	0 - 2M	8	8	1k	yes	$6,000 - $21,700	Same as above.
HP64750A	25	68040, 68EC040	512k	8	8	1k	no	$33,900 - $44,600	
HP64751A	16	68340	0 - 2M	8	8	1k	yes	$6,000 - $21,700	X11/motif-based graphical interface, available high-level debug, real-time software performance analysis.
HP64760A/701	25, 33	i960KA/KB, i960SA/SB	2M - 4M	16	32	1024	yes	$24,000 - $26,000	Available on HP9000s, Sun workstations, PCs.
HP64772A	50	AT&T DSP32C	64k	8	8	1k	no	$42,000	—
HP64774J	25	Am29000/05	0 - 4M	8	8	1k	no	$38,000	—
HP64774K	25	Am29050	0 - 4M	8	8	1k	no	$38,000	—
Huntsville Microsystems 3322 South Memorial Pkwy, Huntsville, AL 35801 (201) 881-6005									**Circle 304**
HMI-200-68020	16 - 33	68020, 68EC020	256k - 2M	4	4	8k × 104	yes	$12,000 - $20,000	Includes SourceGate emulator control and debugger software.
HMI-200-68030	16 - 33	68030, 68EC030	256k - 2M	4	4	8k × 104	yes	$12,000 - $20,000	Same as above.
HMI-200-68040	25	68040, 68EC040, 68LC040	256k - 4M	4	4	8k × 104	yes	$25,000	Same as above.

Model	Speed (MHz)	Processor(s) supported	Overlay memory (bytes)	No. of hardware breakpoints	No. of break-point levels	Trace buffer depth (bits)	Performance analysis	Price	Comments
Microtek International 3300 NW 211th Ter, Hillsboro, OR 97124 (503) 645-7333									**Circle 305**
MICE-III	25	68020/30, 68EC020/30	1M	5	Up to 8	2k × 96 or 32k × 96	optional	$14,000 - $16,000	High-level language debug support optional.
MICE-V	33	256, 386, 386SX, 486, 486SX	128k - 1M	8	4	8k × 141	no	$15,000 - $32,000	Same as above.
PowerPack	40	68330, 68331, 68332, 68333, 68340	256k - 1M	8	4	128k × 96 or 256k × 96	optional	$9,995 - $15,000	Trace collected at MPU clock level.
Nohau Corporation 51 E Campbell Ave, Campbell, CA 95008 (408) 866-1820									**Circle 306**
EMUL16/300-PC	16	68331, 68332, 68340	4M	1	3	512k	yes	$4,000 - $8,000	High-level debugger.
Orion Instruments 180 Independence Dr, Menlo Park, CA 94025 (415) 327-8800									**Circle 307**
8800	40	68330, 68331, 68332, 68340	12k - 2M	65K	4	128k - 512k	—	$8,800	DOS extender on 386 PC host, high-speed parallel interface to host.
Sophia Systems and Technology 777 California Ave, Palo Alto, CA 94304 (415) 493-6700									**Circle 308**
MultiSTAC	25	386/386SX	16M	22	8	8k × 154 or 32k × 154	yes	$15,000 - $17,000	Source-level debugger, fast download.
MultiSTAC	25	487SX/DX	Up to 16M	22	8	154 bits × 8k or 32k bus cycle	yes	$17,000 - $30,000	Microsoft windows-based source level debugger, 9 × 6 × 1-in. module, download speed of 1 Mbyte/s, eight-level trigger.
MultiSTAC	25, 50	68EC020/30, 487SX	16M	22	8	8k × 154 or 32k × 154	yes	$15,000 - $19,000	Same as above.
MultiSTAC	33	486DX/DX2	16M	22	8	8k × 154 or 32k × 154	yes	$19,000	Same as above.
MultiSTAC	33	68020/30	16M	22	8	8k × 154 or 32k × 154	yes	$15,000 - $17,000	Same as above.
MultiSTAC	40	68EC030	16M	22	8	8k × 154 or 32k × 154	yes	$28,000	Same as above.
MultiSTAC	50	68030	16M	22	8	8k × 154 or 32k × 154	yes	$28,000	Same as above.
Step Engineering 661 E Arques Ave, PO Box 3166, Sunnyvale, CA 94088 (800) 538-1750									**Circle 309**
Eclipse JIAG	16	Am29200, Am29205	515k - 6M	—	—	1k × 256	no	$7,995	Integrated SDBUG/XDBUG debugger environment.
Eclipse/LE	up to 25 MHz	Am29000, Am29030, Am29035, Am29050, Am29200, Am29205	512k - 6M	3	16	32k × 256 bits	yes	$14,950	Universal support for all 29K family integrated SDBUG/XDBUG debugger environment.
Eclipse 29K	up to 40 MHz	Am29000, Am29030/35, Am29050, Am29200, Am29205	512k - 6M	63	16	32k × 256 bits	yes	$16,675	Universal support for all 29K family, integrated SDBUG/XDBUG debugger environment.
Excell 930/931/932	up to 50 MHz	MB86730/31/32	512k - 6M	5	1	32k × 256	no	$15,875	Integrated to XDBUG, X-RAY debugger.
Express I	25	i960CA/CF	512k - 6M	9	1	8k × 256	no	$17,950	Integrated SDBUG/XDBUG debugger environment, cache-on support, executes reconstruction breakpoints.
Express II	33	i960CA/CF	512k - 6M	9	1	8k × 256	no	$23,450	Same as above.
Express III	40	i960CA/CF	512k - 6M	68	16	32k × 256	yes	$36,950	Integrated SDBUG/XDBUG debugger environment, range breakpoint (match-words) with qualifiers, cache-on support.

SOFTWARE & DEVELOPMENT TOOLS



Hewlett-Packard has added real-time operating system measurement capability to its 64700 series of emulators. This new tool lets you trace the flow of OS activity through your system. The software displays this trace activity in the actual native service call mnemonics of your OS (middle window). Users can trace all OS service calls, including input parameters and return values.

Clara, CA). "That can be frustrating to designers when they're trying to debug because they really want to look at everything."

In general, RISC chips, especially those based on MIPS, SPARC, 29000, and 88000 architectures, need more channels of trace then there are pins on the chip. "That's something that's often overlooked," says Laengrich. "Each of the RISC microprocessors needs extra channels for its own reasons." SPARC chips, for example, have two buses—a data/instruction bus and an address bus—and these buses are multiplexed. According to Laengrich, "[In the SPARC chip,] on every cycle you get two values on the bus. To really see what's going on in that case, the emulator needs to demultiplex those addresses—or data values as data instructions—and present them in parallel to the trace control." By demultiplexing the buses, you take a 32-bit bus and turn it into two 32-bit buses. Again, that demands more channels of trace.

Embedded Performance supports several families of RISC chips with its Turbo emulator architecture. Each emulator provides from 200 to 256 channels of trace. The Turbo emulator architecture supports 33- and 40-MHz clock rates and offers 8-kbyte trace buffers as standard, with 32 kbytes as an option.

Emulators from Sophia Systems (Palo Alto, CA) offer a feature called fetch triggering that addresses one of the subtleties of trace. Of the emulator's 16 triggers, up to four may be set up as fetch triggers. You may, for example, want to trigger a trace if there's a read from a particular address, but only if you're executing in a certain area of the program. Sophia's emulator lets you specify the address and value of the instruction that was fetched to cause a certain data value. As a result, you can trigger if a particular variable is set by one subroutine but not by others.

"There isn't anybody who's yet figured out how, in real time, to trigger on a variable that's on the subroutine stack," claims Robert E. Hoffman, executive vice-president at Sophia Systems. "If you're willing to stop when you get to the entry point of the function, and quickly record the address of the stack, then you can set up a trigger on the variable at that point. But nobody's do-

ing it in full real time yet. With the fetch trigger you can do that."

Tracing OS activity

The way that trace is displayed by user interface software can also be a critical issue. Designers are accustomed to looking at software at the same level of abstraction at which they're working. People designing in source code, for example, want to see trace information displayed in source-level code.

Hewlett-Packard (Colorado Springs, CO) has taken this concept a step further by outfitting its 64700 series of emulators to perform measurements for embedded designs that use real-time operating systems (RTOSs). Don Logelin, an HP systems design engineer involved in the 64700 project, explains the usefulness of this capability. "When designers have a multitasking operating system," he says, "they want to be able to view that information the same way they are used to dealing with it. Designers using RTOSs are used to dealing with the task names. They know what messages get passed between their tasks, and what semaphores they use. Unless you can display it at that level, they have to go through a very tough translation process."

To perform the required OS measurements, HP uses a sophisticated sequencing and windowing mechanism. "If you have a shared OS task or a shared OS utility that's called by a number of different tasks, for example," says Logelin, "but you're only interested in dealing with it when it gets called by a particular task, you can set up our emulator to trigger and set the storage qualifications to only pick up the data when that particular task is active and when that operating system routine is called. Without that type of sophistication in the emulator, a lot of measurements wouldn't be possible."

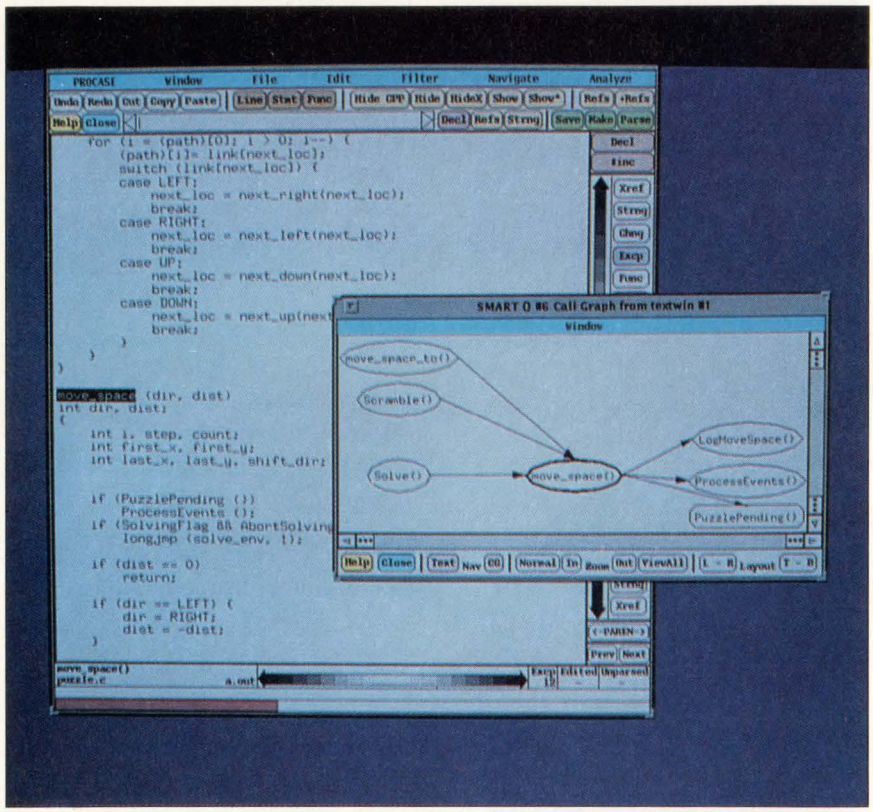
At present, HP provides measurements in the 65700 emulator for RTOSs such as Integrated Systems' pSOS+ and Ready Systems' VRTX32. This measurement capability, coupled with the emulator's graphical user interface, helps you understand the flow of OS activity, track dynamic memory usage, isolate defects based on OS level-task qualifiers, and perform time profiling of task durations.

SOFTWARE & DEVELOPMENT TOOLS

Programming tool integrates functions of UNIX utilities

Recognizing that the majority of C programmers aren't currently using software engineering environments or, for that matter, CASE tools, ProCase has introduced a low-cost tool designed to make life easier for them.

Most programmers still handcraft code in a highly iterative "edit-compile-debug" cycle, and the tools they use are mostly utilities supplied with UNIX.



C/Spot/Run integrates the functionality of some common programming activities in a single window. Here, a graph of part of the calling sequence can easily be related to the underlying code. If a programmer edits a piece of code, it's immediately reanalyzed by the system.

Single-window functionality

C/Spot/Run is a tool that integrates the functionality of such UNIX utilities as Grep, Lint and CScope within a single window so you can interactively select utility functions without shutting one utility down or changing windows. Grep is used to search a file or files for a pattern or string of characters and show file name and line reference for each occurrence. Lint is a C-program verifier that searches files for likely bugs. CScope is a cross-reference tool used to navigate within specified C-source files. C/Spot/Run combines semantic analysis, syntax checking, dependency analysis, and source code filtering, along with the ability to navigate through graphical representations of function calls.

While the UNIX utilities are file-oriented, C/Spot/Run looks at the code from a program/module perspective. Before code is linked and compiled, C/Spot/Run can parse all included code modules and establish a picture of the ones that will make up the compiled program. In parsing, C/Spot/Run also logs all semantic errors, which are listed in an exception report in a separate window. You can click on a listed error and be taken to the line of code in which the error occurs, and then expand your view to see lines of code preceding and following the line of interest.

Maneuvering techniques

To navigate quickly through a calling sequence, you click on a function and see the calling and called functions in a small window. You can then follow that path in a graphical representation and view the code of any function with a mouse click. C/Spot/Run supports dependency analysis so you can specify the language-dependent context in searching for a string. In this way, the system doesn't return every reference to each "i" or "j" in the program.

C/Spot/Run's program-wide cross-referencing lets you follow the impact of changes. The tool filters code to show only the source lines relevant to the task at hand, and can also filter the references to an identifier to give a quick view of dependencies.

The tool runs on SPARCstation workstations under SunOS 4.0 with Open Windows or on Hewlett-Packard 9000/700 systems under HPUX 8.0 with HPVUE. Priced at $995, it will be distributed through UNIX Central. — *Tom Williams*

C/Spot/Run at a glance

- Single tool integrates functions of several UNIX utilities
- Automatically parses code before compilation
- Logs semantic errors and allows instant access to relevant code
- Shows calling sequences in graphical form with mouse-click navigation
- Filters code to show only references relevant to user's task
- Supports commonly used "edit-compile-debug" programming cycle

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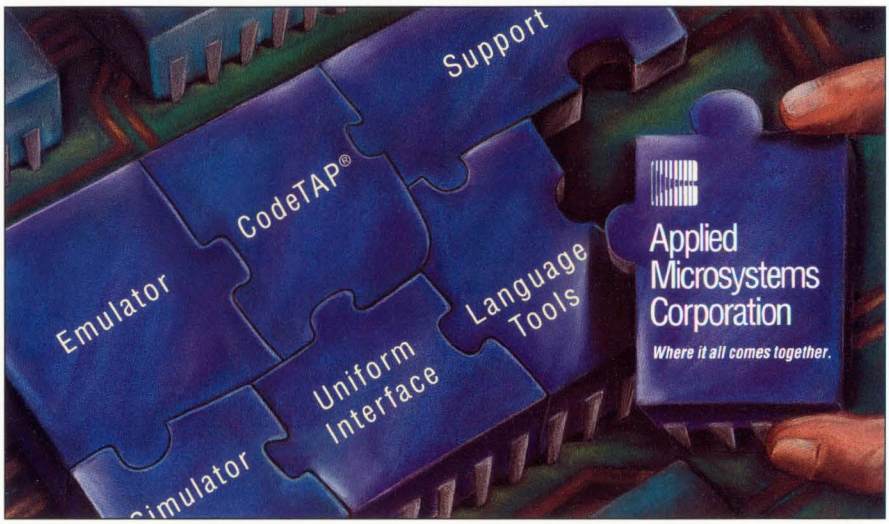

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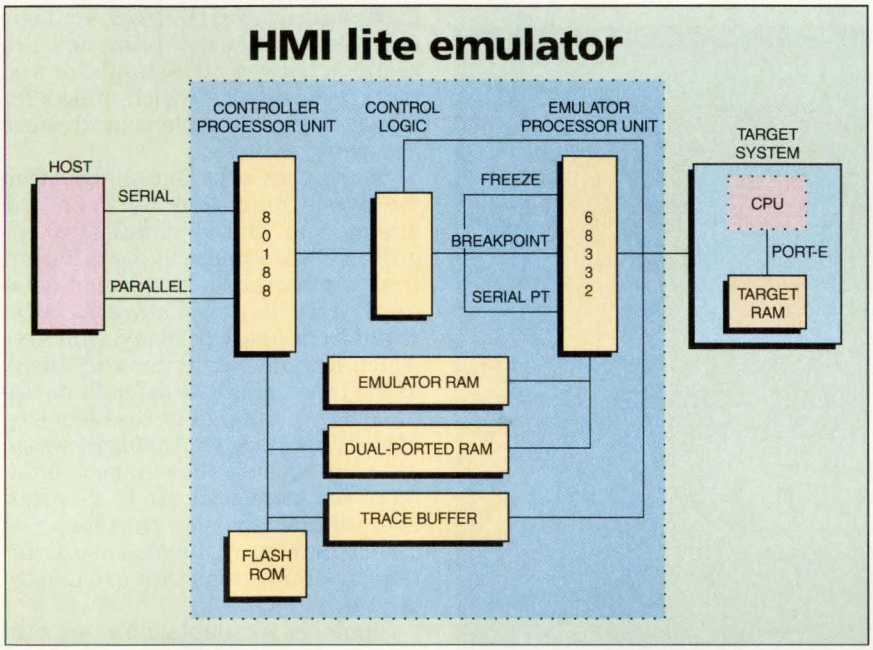
SOFTWARE & DEVELOPMENT TOOLS

Lite emulator does heavy duty

Huntsville Microsystems (HMI) has released its Lite series of emulators for the Motorola 68300 series of microcontrollers. The unit is the company's answer to the problem of emulation cost. While other emulator vendors have addressed the cost issue by offering emulation substitutes that lack trace capability, the Lite can do everything that makes an emulator an emulator. This includes 4k cycle trace, hardware breakpoints and complete emulation of the 68300-series chips. HMI's goal with the Lite is to make emulation technology available to users with limited funds.



Huntsville Microsystem's Lite emulator has a two-processor design. The 80188 (left) talks to the host and controls the emulator. On the right is the chip under emulation (the 68332, in this case). The emulator uses the background mode available on the 68300 processor. The control logic monitors the state of the bus. If it sees something it needs to break on, it sets a breakpoint there. This triggers an acknowledge signal which is sent back to the 68332. From that point, the chip is in background mode, which lets you exchange data via the serial port and read the 68332's registers.

Looking inside

The Lite offers thorough emulation of 68300 chips, including the proper tracing of show cycles—internal transfers which occur inside rather than outside the chip. To trace these cycles, the Lite takes advantage of special features on the chip that put the show cycles onto the bus where they can be accessed.

The problem of pipeline queues provides another example of the Lite's sophisticated tracing. On 68300 chips, instructions are prefetched and queued in a pipeline. The problem is that look-ahead logic on the chip may bypass instructions when a JUMP is encountered. So that these instructions aren't lost to the trace, the Lite emulator uses the same look-ahead logic. It dequeues the trace so that what actually gets executed is what's seen in the trace buffer.

Pesky Port E

A key issue in emulation is the ability to emulate a processor exactly without limiting its use. The 68300 chips have a port called Port E which is frequently used by emulator makers for this purpose. Port E has data-strobe and address-strobe acknowledge signals that normally can be used for emulation, but the port is also reconfigurable by the user for something else, such as I/O. If that's done, the data strobes and other signals are tied up and can't be used for emulation. The Lite emulator gets around the problem by using the chip select signals to access memory and exercise control, while bypassing Port E.

Integrated on the Lite is HMI's SourceGate debugger. It provides full emulator control integrated with source-level debugging and support for all major C and Ada compilers. You can host SourceGate on IBM PC-compatible or UNIX-based platforms. Communications are supported through a high-speed serial port (115.2-kbaud) and a parallel port for downloading code.

The emulator is configured with 256 kbytes of overlay RAM. It supports mapping of all chip select signals with dynamic bus sizing for 8- and 16-bit operations. In addition, two kbytes of dual-port RAM are provided to monitor critical variables in real time.

The unit supports up to four hardware events for triggering breakpoints or traces. There are, in addition, multiple software breakpoints. A 4k × 63-bit trace buffer permits direct viewing of source code. This trace buffer can also record full address, data bus, chip select, and control signal information.

The initial release of the Lite emulator supports Motorola's 68330/1/2/3 microcontrollers. Support for the 68040 and the HC16 family are planned. Offered with HMI's SourceGate debugger, the unit is priced at $4,995. —*Jeff Child*

Lite emulator at a glance

- Supports 68330/1/2/3; support for 68040, HC16 planned
- Full tracing of show cycles, pipeline dequeuing, Port E support
- 256-kbyte overlay RAM
- Two kbytes of dual-port RAM
- 115.2-kbaud serial interface to host

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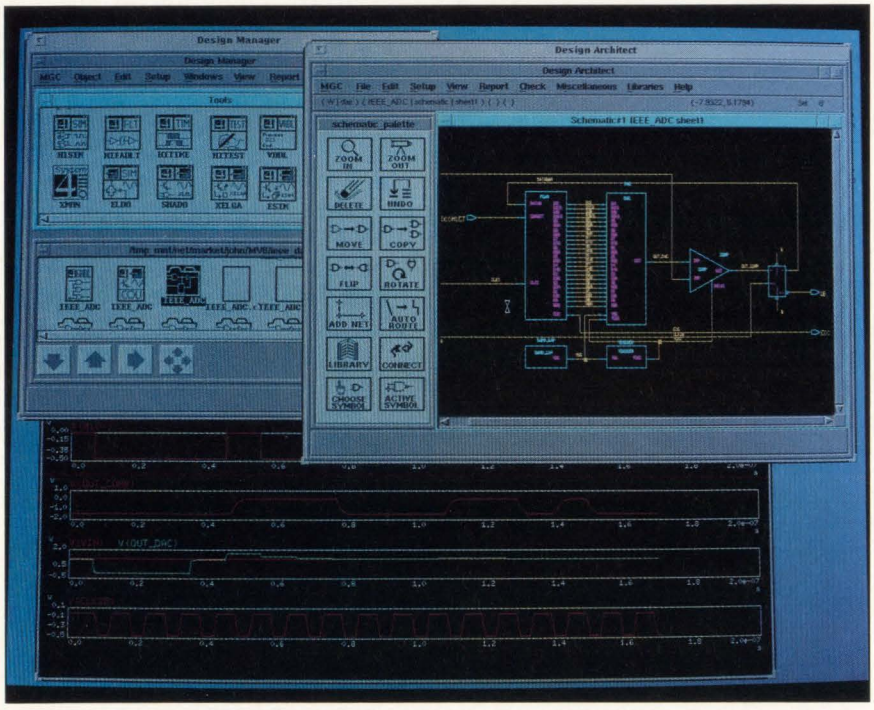
CAE/CAD DESIGN TOOLS

Mixed-signal simulator features high speed, capacity and convergence

GenRad's Design Automation Group has just introduced Shado, a mixed-signal simulator that combines the digital capabilities of HSIM, from the company's System HILO 4 suite, with Eldo, an analog simulator from AnaCAD, a German company that recently opened an office in Fremont, CA. According to GenRad, the Eldo simulator provides an order of magnitude improvement in capacity, up to two orders of magnitude improvement in speed, and better convergence than other simulators.

The Eldo analog engine uses both second- and third-generation equation-solving methods. The second-generation algorithms are Spice-like, and use matrix manipulation and Newton-Raphson (NR) iteration techniques to solve the circuit's differential equations. Although these techniques provide solutions for all types of technology, they sometimes sacrifice performance. For circuit sections with loose couplings (such as MOS transistors), faster third-generation algorithms, such as one-step relaxation (OSR) methods, are used.



Shown here is the Shado mixed-signal simulation of the IEEE 12-bit successive approximation register analog-to-digital converter (upper right). Digital and analog results are shown on a unified display (bottom window).

Balancing algorithms

A key feature of Eldo is that it can apply both NR and OSR techniques to a solution. The simulator uses a patented balancing technique to select the best equation-solving algorithm for a particular section of the analog circuit. Moreover, the NR and OSR algorithms are applied simultaneously to the whole circuit. This can be automatic, with no user intervention.

The aim of the balancing algorithm is to partition the circuit into blocks, each identified as appropriate to NR or OSR. This technique assigns the appropriate algorithms to targeted blocks. In the case of the NR algorithm, the technique manipulates several smaller matrices instead of one large matrix (as is the case with Spice algorithms).

For circuits with severe convergence problems, techniques such as simulated annealing are used. The circuit can also be repartitioned when non-convergence is detected until successful DC convergence is achieved. NR and OSR algorithms are then used for transient analysis, block by block.

The digital side of the simulator, HSIM, supports VHDL 1076, RTL logic and test synthesis. Libraries are common between the simulator and the synthesis tool, which makes for faster design iterations and more accurate synthesis.

Shado uses a lock-step algorithm for synchronization between the analog and digital simulation engines. This approach is different from some other mixed-signal solutions, such as the Calaveras algorithm from Analogy (Beaverton, OR), which lets one simulator run ahead of the other. GenRad defends its approach by pointing out that leapfrog algorithms such as Analogy's waste CPU time because they make a simulator backtrack in time. GenRad does admit, however, that leapfrog algorithms may have an advantage in simulations that are mostly digital.

Shado is available now on Sun SPARCstations and Hewlett-Packard 700 systems. Prices start at $30,000.

— Mike Donlin

Shado at a glance

- Mixed-signal simulator combines HSIM digital with Eldo analog simulation
- Uses second-generation Newton-Raphson algorithms and third-generation one-step relaxation techniques
- Has lock-step algorithm for efficient use of CPU time

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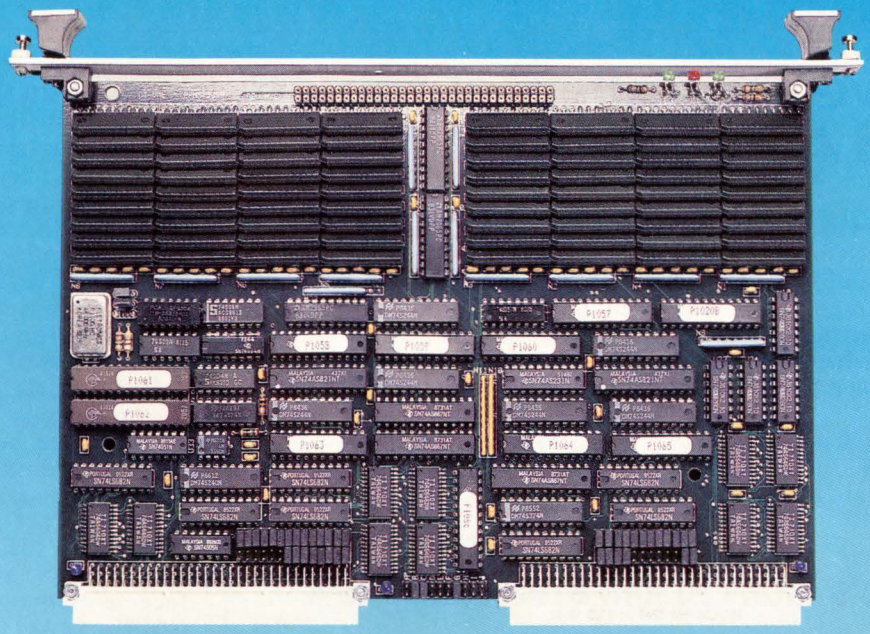

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INTEGRATED CIRCUITS

Disk drive controllers automate SCSI and AT interfaces

Computer users want their disk drives big, fast and inexpensive. They usually get two out of those three characteristics. Two new controllers in Adaptec's AIC8000 family, however, help drive manufacturers come closer to delivering all three.

Adaptec's approach is to integrate data-flow automation into the disk controller, increasing I/O performance and freeing the microcontroller for servo and mechanical operations.

Even with these two new microcontrollers, disk manufacturers have run into limits of capacity and performance. Adaptec's new chips, however, support disk NRZ (non-return-to-zero) rates of 40 Mbits/s for the AT bus and 40 to 48 Mbits/s for SCSI, plus host data transfers to 10 Mbytes/s, with bandwidth for error correction.

Adaptec calls its approach Automatic Data Flow Management (ADFM). In the SCSI interface, ADFM permits automatic management of single or multiple SCSI phases and automated handling of the SCSI control and data signals. In the AT interface, ADFM supports full AT autocommand execution and automatic update of the AT Task File. ADFM provides for automated data flow between host and disk and automated full-track data access from disk for either read or write functions.

The data flow manager is composed of the disk controller, error detection and correction, microprocessor interface, buffer controller, and I/O bus controller, as well as a power manager.

The two controller chips are distinguished by their host interface blocks. In the AT chip, the AIC8160, the host interface block automates the data transfer protocol, so that a 17-sector track can be transferred in 2.6 ms, rather than a conventional controller's estimated 6.0 ms.

Adaptec's SCSI chip, the AIC8110, can handle 10-Mbyte/s synchronous SCSI-2 Fast transfers, or 5-Mbyte/s synchronous or asynchronous SCSI-1 transfers, in either single-ended or differential modes.

On the other side of the drive, the disk controller essentially takes over from the microcontroller after power-up initialization. It contains a 48-word disk format/read/write sequencer RAM.

Between the host and the disk, the buffer controller is the final element in the automated datapath, controlling data flow into and out of the buffer RAM while the host and disk ports are operating. It interfaces to the disk controller through a 16-byte FIFO and to the host interface manager through a 16-byte (SCSI) or 24-byte (AT) FIFO.

Error detection and correction (EDC) can use standard 32- and 56-bit computer-generated codes or an 88-bit non-interleaved Reed-Solomon code. The latter can correct a single-burst error of up to 14 bits.

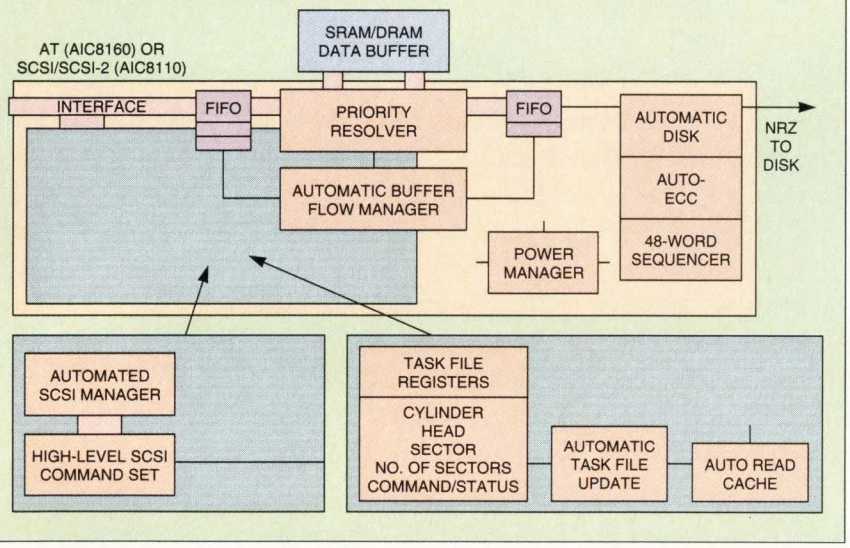
The local microcontroller interface handles most 8-bit microcontrollers with either multiplexed or non-multiplexed address/data buses.

For portable applications, a power manager provides for idle, standby and sleep modes. Adaptec estimates a 30-percent power savings over a controller with no power management.

Both controllers are available in 100-pin thin and standard quad flat packs. In quantities of 10,000, the unit price of the AIC8110 is $18.95, and the AIC8160 is $15.95.

— *Don Tuite*

Adaptec's AIC8110 and 8160 controllers



Adaptec's AIC8110 and 8160 disk drive controllers are similar chips with different host interfaces for AT and SCSI-2 buses. By automating the control functions for the host, drive and buffer interfaces, they unload the disk drive microcontroller and speed the flow of data. Their high degree of integration also lowers the cost of drive systems and speeds time-to-market.

AIC8110/8160 at a glance

- Host interface: 10 Mbits/s, automated command support
- SCSI: AIC8110 reads/writes 40-48 Mbits/s (NRZ)
- AT: AIC8160 reads/writes 36-40 Mbits/s (NRZ)
- Supports most 8-bit microcontrollers

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INTEGRATED CIRCUITS

12-bit A-D converter outputs RS-232

A single A-D converter chip with two-wire, unbalanced RS-232 serial output can replace the customary chain of five or more chips used for remote data gathering in monitoring and control systems. Micro Linear's ML2223 contains a 13-bit (12-bit plus sign) analog-to-digital converter, sample-and-hold, voltage reference, UART, and baud rate generator. You can place the 16-pin DIP right at your sensor and eliminate analog noise problems.

The range of the differential input is –5 to +5 V, and the chip is self-calibrating. Maximum non-linearity over temperature is 0.018 percent. Conversion time, including sample-and-hold, is 45.6 µs maximum.

Although the RS-232C specification calls for shorter cable lengths, Micro Linear claims that it's practical to run signals as far as 200 ft from its chip. Long-range remote sensing can be accomplished using modems or LANs. The data rate isn't limited to the RS-232's 19.2-kbits/s maximum, but may go as high as 200 kbits/s.

Data is output in two 9-bit bytes (including parity). Each byte is framed by one start bit and two stop bits, so a burst of output data is 24 bits long. To help the system controller identify bytes, the least significant is sent with even parity, while the most significant is sent with odd parity.

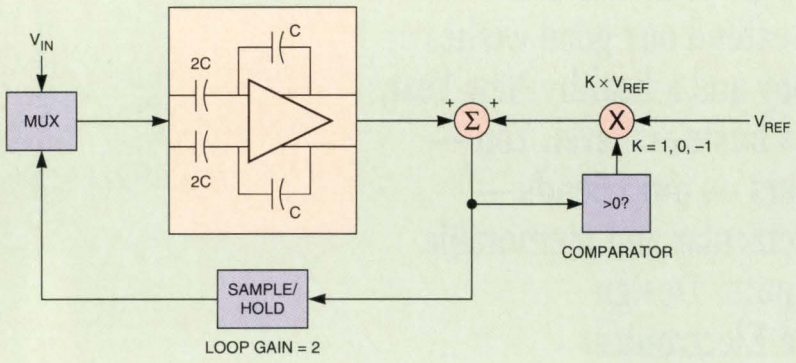
Of the two data output modes, the current mode outputs data immediately after the analog-to-digital conversion is complete, but at the price of longer intervals between conversions. The previous data mode overlaps conversion and data output for a higher conversion rate, but introduces a longer delay between conversion and output.

To achieve 12-bit resolution on a small die, the chip's A-D circuits use an algorithmic approach to successive approximation conversion, rather than the more common technique that involves feedback from a DAC. For positive inputs, the input sample, multiplied by two, is compared to the voltage reference. If it's greater than the reference, the MSB is set to one, and the reference is subtracted from the 2× input voltage, with the remainder stored in the sample-and-hold. If it's less, the MSB is set to zero and the 2× input voltage itself is stored in the sample-and-hold. The process is repeated for successive bits, except that twice the value currently in the sample-and-hold is compared to the voltage reference each time. Negative inputs are handled similarly.

In quantities of 1,000, the unit price of the ML2223 is $14.50.

—Don Tuite

ML2223 conversion scheme



The ML2223 uses an uncommon scheme in which, bit by bit, it converts an input signal to a 12-bit digital representation by comparing the output of a 2× amplifier to a voltage reference, setting the bit, and storing the difference between the signal and the reference in a sample-and-hold. For the most significant bit, the input to the amplifier is the sampled voltage; for subsequent bits, the input is the value stored in the sample-and-hold in 24-bit frames. An 8-bit idle is needed before the next A-D conversion begins. You can choose between seeing data immediately after it's been converted, or waiting one conversion cycle. The first (or current) data mode has the disadvantage of fewer conversions per second, but is preferred in systems in which the absolute value of the measured quantity is of paramount importance. The second (or previous data) mode is preferred in systems in which rate of change is being used to regulate a process.

ML2223 at a glance

- Differential ±5-V input
- 12-bit (plus sign bit) resolution
- Serial RS-232 output, at up to 200 kbits/s
- 16-pin 300-mil DIP
- ±5-V supplies

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San Jose, CA 95131
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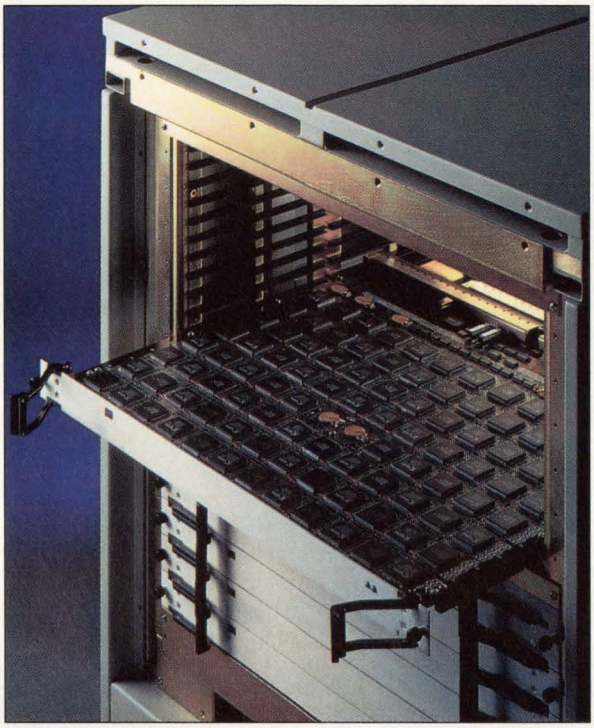
ASICs & ASIC DESIGN TOOLS

Prototyping system emulates up to six million gates

For pre-silicon prototyping, the Enterprise Emulation System from Quickturn Systems (Mountain View, CA) is based on a multiplexed architecture that's separated into logic emulation modules and a reprogrammable backplane. You can plug up to eleven modules, each with the capacity to emulate 30,000 gates, into the Enterprise backplane. By using an Interconnect Module, moreover, you can cluster as many as 22 systems, for a total emulation capacity of six million gates.

The key to the Enterprise architecture is a full-custom, 168 × 168 crossbar switch, dubbed the Multiplexed Interconnect Chip (MIC), that Quickturn developed for both the Enterprise logic emulation modules and its reprogrammable backplane. Each module has 42 Xilinx 3090 FPGAs to accommodate logic and 42 MICs to implement interconnects. By alleviating the need to use FPGAs for interconnect purposes, Quickturn has made it possible to pack the FPGAs much more densely with logic. Each of the Enterprise's 3090s can accommodate up to three times as many gates as identical parts in earlier Quickturn hardware emulators.

Separating logic from interconnect also shortens routing delays, resulting in typical emulation speeds of from 4 to 8 MHz, and simplifies the process of mapping your design into the emulation system. In addition, putting interconnects into MICs rather than into more costly FPGAs lowers overall system cost. On a per-gate basis for a fully configured system, Enterprise costs 25 percent less than Quickturn's previous hardware emulator.



Each Enterprise Emulation System chassis holds up to eleven logic emulation modules, with a capacity of 30,000 emulation gates each. Up to 330,000 gates, then, can be emulated on a single system without interconnect cables. Multiple Enterprise systems can be clustered to emulate designs of up to six million gates.

Automatic partitioning

In the past, Quickturn users have had to manually partition very large designs into manageable logic blocks, but Enterprise users can now assign that difficult task to the Automatic Design Partitioner. This software partitions logic into netlists fitting within a single emulation system and also automates the clustering of multiple Enterprise systems.

Also new with Enterprise are Memory Emulation Modules that automatically map memory elements from a netlist to the emulation system. These programmable plug-in boards eliminate the need to rely on emulation board resources. You can model multiport RAMs with up to 32 ports and single-port RAMs of up to 2 Mbytes on a single board.

Precision Emulation Software, embedded in Enterprise, automatically maps synchronous and asynchronous designs into the emulation system. For debug, the software has a timing analysis tool that supports asynchronous designs. Quickturn claims that its Timing Sensitive Partitioning and Precision Prototype Synthesis algorithms guarantee a violation-free configuration.

For future expansion, Quickturn has reserved interconnect capacity on the Enterprise's backplane to ensure the opportunity to introduce increased-gate-count logic emulation modules when higher-capacity FPGAs replace the 3090s.

The Enterprise Emulation System, available now, is priced at $388,000 for a 120,000-gate system and $798,000 for a 330,000-gate system. — *Barbara Tuck*

Enterprise at a glance

- Logic separated from interconnects
- Shorter delays, simplified mapping
- Emulation speeds from 4 to 8 MHz
- Automated design partitioning
- Plug-in boards for emulating memories

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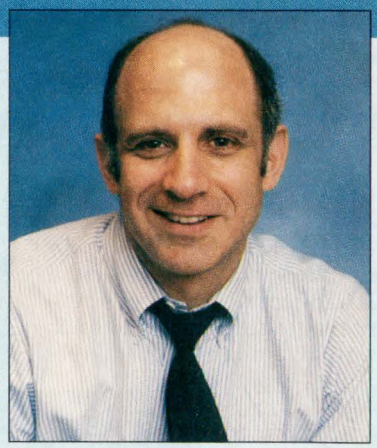
MIXED-SIGNAL DESIGN Stephan Ohr



Are automobiles the proving ground for the next generation of electronics?

Art Fury, the charismatic vice-president of Semitech (Newbury Park, CA), tells a story about convincing automakers to make better use of semiconductors. As an applications engineer for General Electric in the 1960s, he got a design win for power switches by equipping an old car with three-step sequential directionals and driving it to Detroit. His ideas were incorporated into the early versions of the Mercury Cougar, but he reports that until Ford engineers could see the technology in action, they were extremely reluctant to incorporate the electronics into their cars.

Changing situation

Although it tends to shy away from publicity, the automotive industry has become one of the most powerful drivers of mixed-signal technology—for CAE tools as well as smart-power devices. Jean-Philippe Dauvin, the keynote speaker at last month's *Computer Design*/Miller Freeman Analog and Mixed-Signal Design Conference, highlighted the importance of the automotive sector. Dauvin, the market research manager for SGS-Thomson Microelectronics (Paris) and president of WSTS Europe (the independent reporting agency for semiconductor industry statistics), said that over the next five years, automotive electronics will grow faster than any industry segment, including computers, consumer electronics and telecommunications. Auto industry electronic devices account for the smallest percentage of the $710 billion in electronic systems manufactured in 1991—4.3 percent compared to 14.2 percent each for military and consumer electronics and 37.5 percent for computer systems. By 1997, automotive electronics will be 6.1 percent of a $1.065 trillion market, while the proportions of consumer and military electronic systems will decrease. Automotive electronics, said Dauvin, will grow at an 11-percent compound annual growth rate (CAGR) between 1991 and 1997, while computers, with the next largest growth rate, will only grow at an 8-percent CAGR.

Automotive customers now consume only 6 percent of the $54.6 billion in semiconductors sold worldwide, but, once again, this area will give the industry its highest growth rate (14 percent) between 1992 and 1997. By then, automotive semiconductors will be 7 percent of a $92.7 billion market. Of particular IC types, semicustom devices will show the highest CAGR (15 percent) during that period.

Use of electronics expanding

Part of the reason for this growth is that the auto industry is beginning to see the potential of electronics. Whereas the industry once considered electronic controls suitable only for passenger compartment climate control or audio consoles, it now sees semiconductors as vital for automobile braking systems, air bag deployment and engine controls. Some of this has been in response to regulatory pressures. Delco Electronics (Kokomo, IN), the automotive systems arm of General Motors, freely admits that it adopted the Motorola 68332 for engine controls in response to the severe emission standards set by the California Air Resources Board (CARB). But if one looks closely, it's clear that the responses of Delco and General Motors have been significantly above and beyond the need established by CARB. Automotive engineers, for instance, are among the best consumers and enhancers of mixed-signal modeling tools.

There's also a vision of the future driving automakers such as Germany's Daimler-Benz A.G., manufacturer of the Mercedes Benz. In the future, for example, satellite warning and navigation systems will guide drivers and regulate traffic patterns, according to Daimler's chairman, Edzard Reuter, in comments he made about his company's acquisition of AEG Electronics (Frankfurt, Germany) in 1989. Electronic components, currently representing about 5 percent of the value of a Mercedes-Benz, will rise to 25 percent by the year 2000. (The electronics content of automobiles will be much higher, in fact, if automakers are successful in perfecting a low-cost quick-

10 FUNCTION µP SUPERVISOR HAS 6ns CHIP ENABLE

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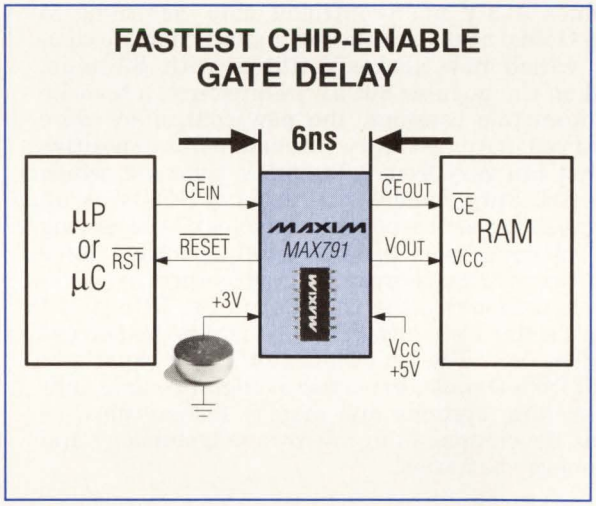

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CIRCLE NO. 70

charge system for battery-powered cars.)

While driven by automotive concerns, Daimler's push into electronics has repercussions for other consumers of mixed-signal technology. Under the Daimler umbrella, AEG and Deutsche Aerospace (Munich, Germany) have formed four microelectronics groups—semiconductors, microsystems, automotive systems, and special technologies. Companies in the semiconductor group include not only Telefunken (Heilbronn, Germany) and Eurosil (Munich, Germany), but also Britain's Dialog Semiconductor (Swindon, England), Matra MHS (Nantes, France), and American-based Siliconix (Santa Clara, CA). Mixed-signal products of the group include smart-power ICs, power transistors and discretes, ASICs and application-specific standard products, as well as microprocessors and microcontrollers.

Matra, in fact, was one of the first companies to introduce a 3-V microcontroller chip, according to Irving Gold, the U.S. marketing manager for the company, which now shares facilities with Siliconix. Based on the popular 80C51 architecture, a favorite for automobile consoles, the new controllers were announced in August and will function from a positive rail that can vary from 2.7 to 5.5 V. Siliconix, which made Art Fury famous in the early 1980s as an evangelist for smart-power technology, was among the first companies to successfully package DMOS power-driver transistors in reduced footprint SO packages—a technology the company calls "little foot." Matra's sister company, Siliconix, is now 80-percent owned by AEG. The semiconductor group expects to benefit from Daimler expertise in engine control antiskid braking systems and display technologies, as well as developments in microwave technology and high-energy batteries.

Sensors and actuators

Current-generation auto system controllers rely on two mixed-signal systems—front-end signal conditioners and back-end amplifiers—which correspond roughly to sensors and actuators. On the front end, a sensor converts engine temperature or brake pressure into a voltage, amplifies it and converts it into a digital number. A microprocessor typically compares this measurement with a reference voltage in ROM-based look-up and issues a corrective response. In some cases, a D-A converter transforms the digital number into a voltage; in others, the digital output of the microcontroller can be used directly to open or close a big mechanical switch—power door locks, for example. In either case, a power transistor must be harnessed to raise the current level high enough to magnetize the coil that turns the motor, activates the relay or squeezes the brake pads. While sensor signal conditioning, with typically low-frequency requirements, is relatively mature, much development work needs to be done in reducing the size and packaging weight of power transistors, and in obtaining tighter integration with control logic, the essence of smart-power technology.

One example of smart-power technology developed for automotive electronics users is Prism, recently introduced by Texas Instruments (Dallas, TX). The Prism technology is composed of a standard-cell ASIC that permits the integration of VLSI logic elements such as microprocessors and memories with linear and power devices. The two keys to Prism are reusable engineering—based on a multipurpose standard-cell library—and a process technology that combines 1-μm CMOS, analog and high-voltage CMOS, and bipolar and power DMOS transistors all on one chip. The technology is said to produce smart-power chips smaller than those coming from the updrain DMOS process of Motorola Semiconductor (Phoenix, AZ) or the BCD-2 process of SGS-Thomson Microelectronics (Phoenix, AZ and Agrate Brianza, Italy). It was developed to impress the automotive system designers at Delco.

More than 100 engineers were involved in the Prism project, according to Delbert Whitaker, TI's vice-president in charge of product development. Prism includes six or more mixed-signal and linear cell libraries. The key to its success, however, is a lateral DMOS transistor structure that drastically reduces the real estate required by DMOS power transistors. One advantage of smaller chip real estate is the ability to replace cumbersome SIP and TO-220 power packages with smaller, less expensive and more manufacturable DIP and SO packaging. Apart from actuators developed for Delco, the first standard TI products to use the technology will be power transistor arrays, data bus latches and transceivers.

Driving CAE tool development

In addition to device technology, automotive equipment makers will be instrumental in the development of analog and mixed-signal CAE tools. They are already among the best customers for Analogy's behavioral modeling tools. A consortium of European auto equipment manufacturers, in fact, is attempting to develop a framework for hardware development and simulation tools. Fueled by engineers at Daimler-Benz and the Bavarian Motor Works (BMW), the consortium's focus is simulating the operation of new systems, even while they're in the conceptual phase. The goal is to test out control system concepts and compare alternatives before the detailed design work is begun.

Key to the success of this initiative is the availability of abstract system-level models, especially those that depict mechanical and electromechanical devices, such as relays, motors, actuators, and switches. These are also among the key concerns of the groups actively tracking the development of an analog hardware description language (AHDL). Gauging by attendance at the Analog and Mixed-Signal Design Conference last month, automotive system builders will be among the first users of an AHDL.

Stephan Ohr is president of Indian Forest Research and editor of the monthly newsletter, Mixed Signals.

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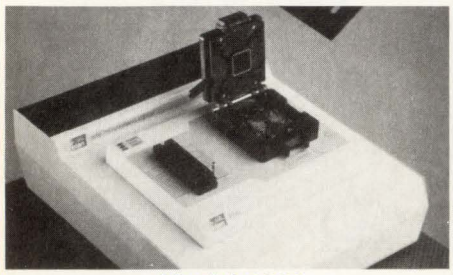

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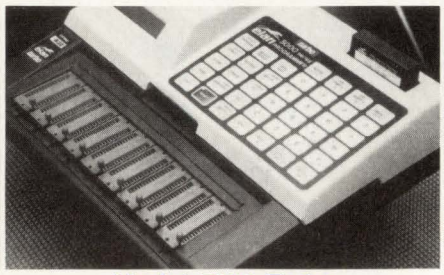

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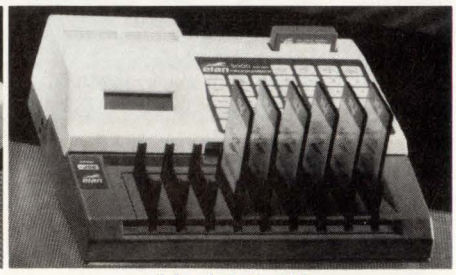

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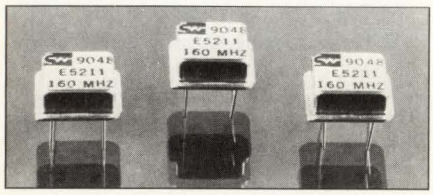

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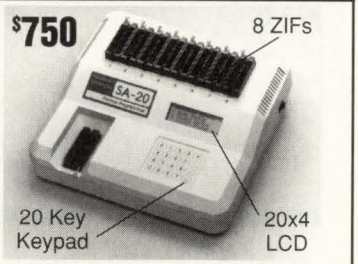

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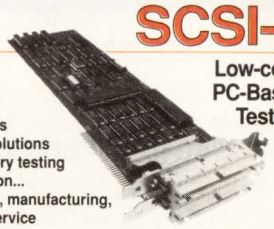

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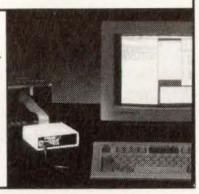

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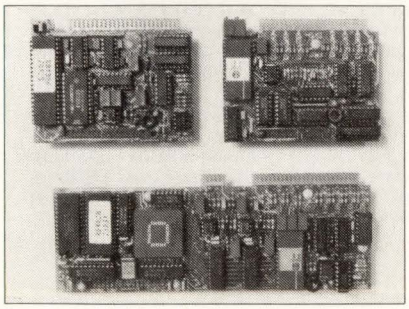

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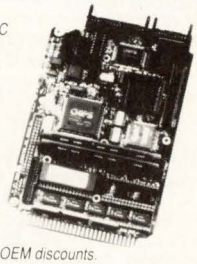

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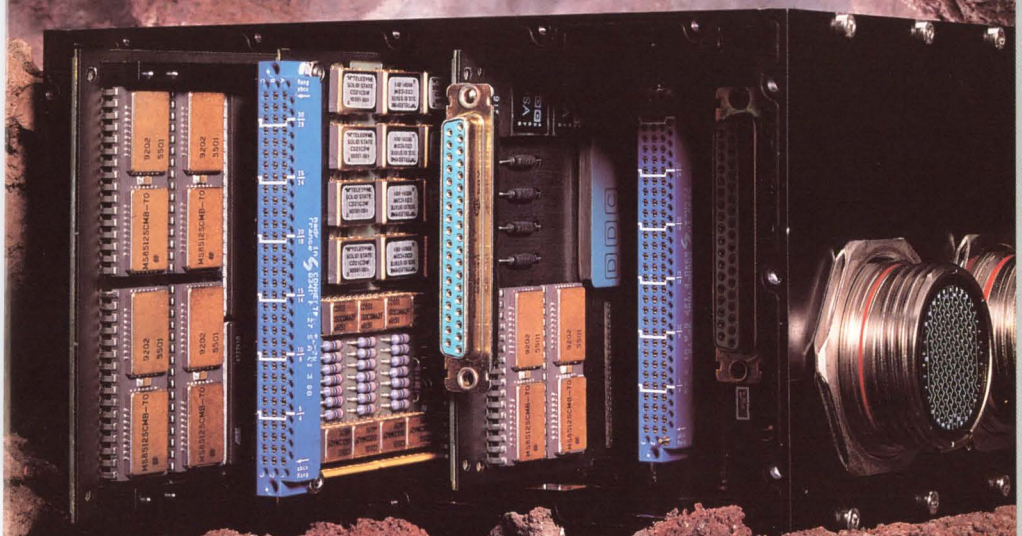

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