JANUARY 1977

# digital design

the magazine of digital systems

MINICOMPUTERS

Their inconclusive battle with microcomputers

How user microprogrammability ups their capabilities

What's happening to peripheral-interface costs?

Optimizing software for Fairchild's F8

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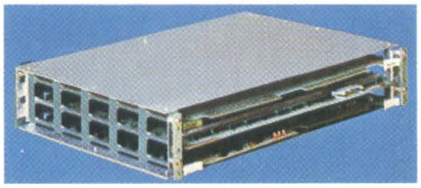

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CIRCLE 1

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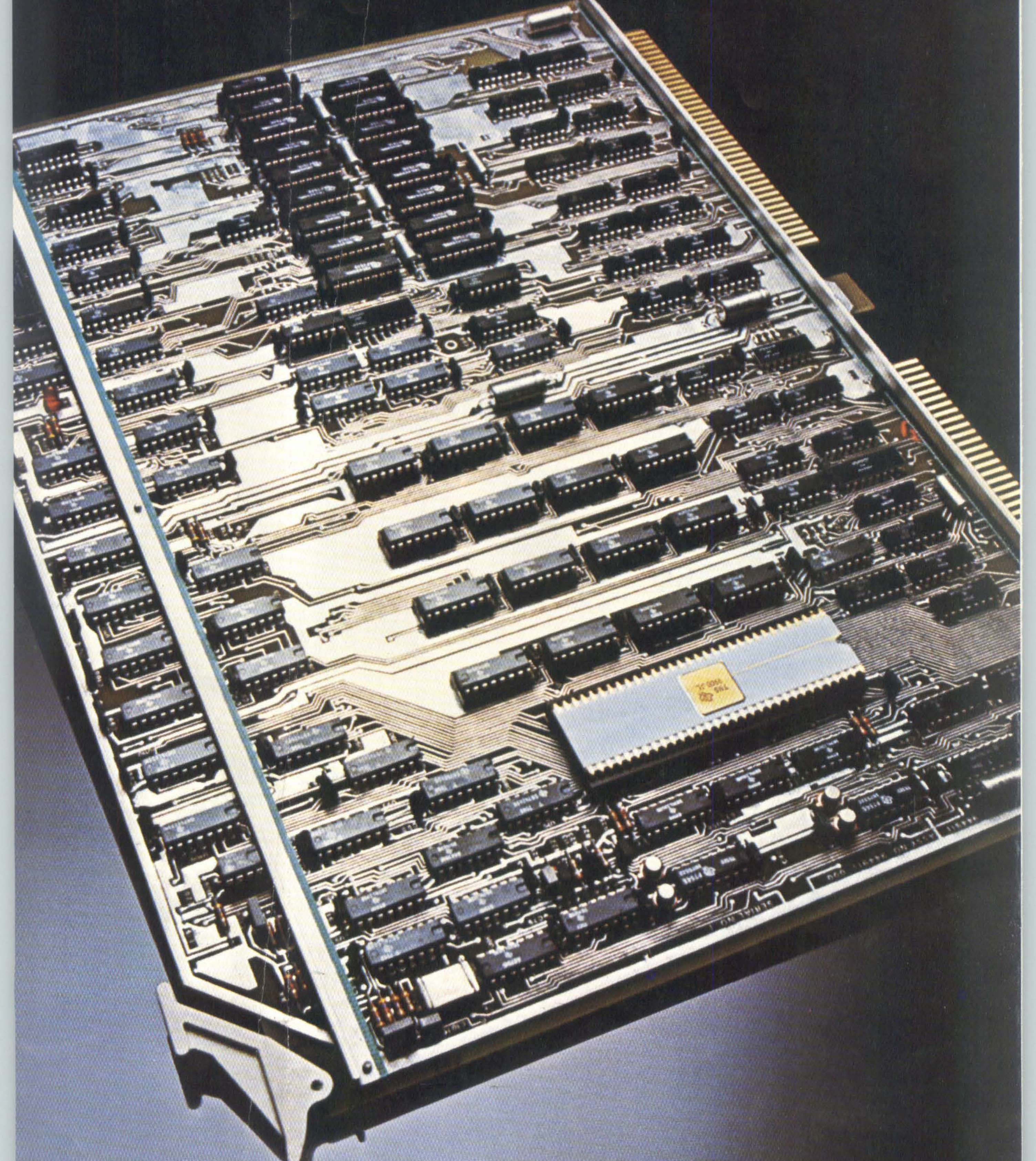

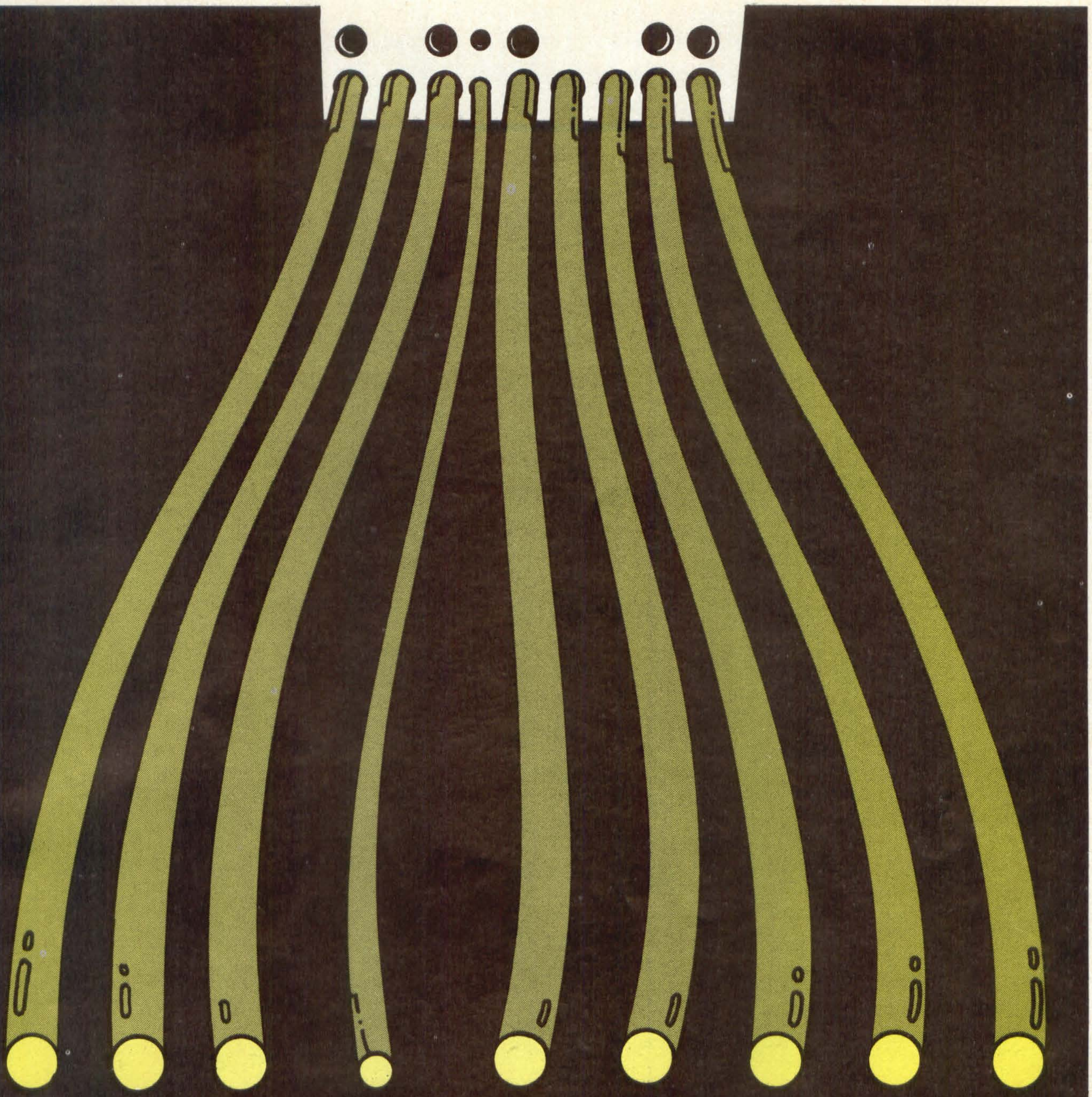

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CIRCLE 4

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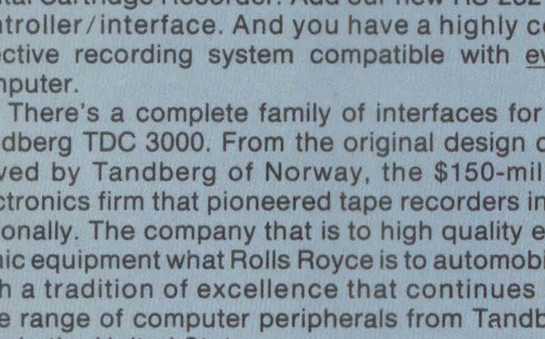
Begin with the industry-proven Tandberg TDC 3000 Digital Cartridge Recorder. Add our new RS-232 I/O controller/interface. And you have a highly cost-effective recording system compatible with every computer.

There's a complete family of interfaces for the Tandberg TDC 3000. From the original design conceived by Tandberg of Norway, the $150-million electronics firm that pioneered tape recorders internationally. The company that is to high quality electronic equipment what Rolls Royce is to automobiles. With a tradition of excellence that continues in a wide range of computer peripherals from Tandberg Data in the United States.

With total communications compatibility, the microprocessor-based RS-232 controller/interface from Tandberg Data is engineered according to EIA Standard RS-232-C, type D and E, and a "teletype-compatible current loop," recording in ANSI/ECMA/ISO-compatible format.

And from the substantial savings in line charges alone, the TDC 3000 with the RS-232 controller/interface will recoup its modest cost in a matter of months. It's hard to beat that kind of cost-effectiveness.



The Tandberg controller/interface is contained on one p.c. board which mounts inside the Recorder. Power is internal from the TDC 3000 built-in power supply. Two interface connectors are provided so that the Recorder can be connected both to a local I/O terminal (such as the Tandberg TDV 2100 Series CRT terminals) and a modem for remote operation.

Thirteen standard baud rates, 75-9600, are user selectable. Data buffers range from a minimum of 256 bytes up to 1024 bytes. The controller/interface responds to all ASCII command codes. Read and write speed is 30 ips and search speed 90 ips.

And for special communications requirements, the 6800 microprocessor allows the Tandberg controller/interface to be OEM-customer programmed.

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Besides RS-232, Tandberg Data provides TDC 3000 interfaces for HP 21MX, PDP 11, Alpha LSI 2, and 8-bit parallel general purpose. All give up to 48K bits transfer rate.

Tandberg Data Inc.
4901 Morena Blvd., Suite 407
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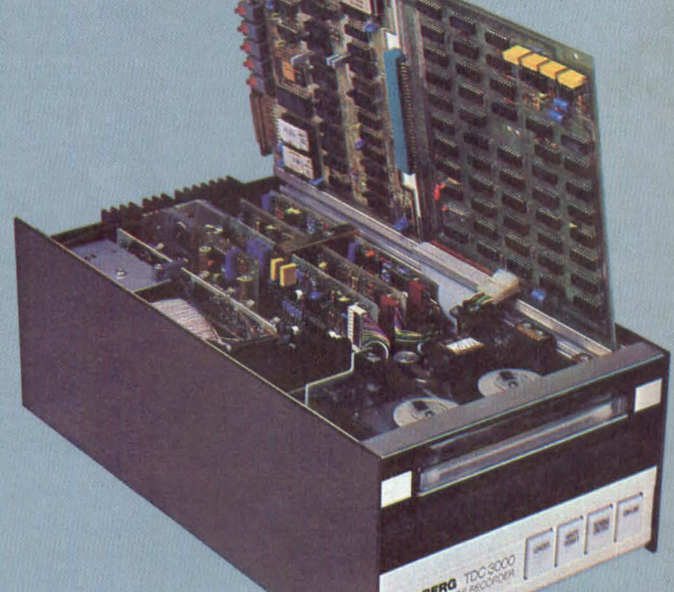
(714) 270-3990



Shown in test position.

Mr. Bruce B. Greenfield, Vice President, Tandberg Data Inc.
4901 Morena Blvd., Suite 407, San Diego, California 92117

I'd like to know more about the RS-232 controller/interface for your TDC 3000. Please send me the RS-232 data sheet and have a Tandberg engineer give me a call to discuss my needs.

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CIRCLE 5

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digital design

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## STAFF

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**CIRCLE 9**

# letters

## punched-tape comments

• Regarding Robert Martell's article, "Punched Tape: Defying Doom & Gloom" (August, page 62), I have a few comments:

★ The article states that the total U.S. market for punched tape systems will rise from $28 million in 1975 to $38 million in 1979. This is not a 75% rise, as the article also states.

★ I am quite positive that the estimate of a 75% increase in market allows for the reduction in price of the hardware. What is the source of these statistics?

★ Paper tapes do require testing to ensure uniform thickness as well as size and alignment of sprocket holes. I encountered such problems in four years at Digital Equipment Corp. – they cause read and parity errors.

★ Ordinary paper tapes cannot indefinitely tolerate hostile environments because they are affected by moisture, corrosive elements and high temperatures.

★ Although paper tapes do not require any special storage facilities, sufficient care should be taken to ensure that they are not mutilated or twisted into knots.

K. SRIRAM
Div. Manager, Computer Div.
Management & Industrial Consultants, Ltd.
Malleswaram, Bangalore, India

• *The author replies: I concede one point. I was in error in my calculation of the percentage increase from $28 million to $38 million. The rise should be 35.7%.*

*Other comments:*

★ *Contemporary manufacturers of paper tape control the thickness of punched tape to an acceptable level, and today's punched-tape reader can read tapes with poor registration and reasonable variation in thickness.*

★ *Nowhere did I say that paper tapes can indefinitely tolerate hostile environments.*

★ *Regarding Mr. Sriram's suggestion about not storing mutilated tapes or tapes twisted into knots, I can only comment that I agree.*

*I should point out that the problems Mr. Sriram ran into at Digital Equipment Corp. do not necessarily occur with every reader. I thank him for his comments but still refute "gloom" reports.*

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That's where you come in. The ASDC will pay substantial royalties to the originators of all software accepted into the ASDC library. If you have written business, industrial or commercial use software for the Altair 8800, ASDC wants to hear from you. It is the aim of the ASDC to stimulate and reward creativity in producing useful software that makes those dreams of "computers for everyone" come true. The ASDC will select only software that measures up to its high standards for system design, coding and documentation. The software will then be further documented and distributed through Altair Computer Centers around the country.

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see next page for a listing of Altair Computer Centers

CIRCLE 10

# technology trends

## Peripheral-interface costs continue to soar, but μPs and LSI chips could reverse trend

Inflated by high costs in engineering and in analog technology, and by computer manufacturers' price markup policies, the cost of a peripheral interface is often higher than the cost of the peripheral it serves. But the increasing use of microprocessors and special-purpose LSI chips could lower interface costs – especially for cheaper peripherals and in minicomputer systems – within the next few years.

So says J. Egil Juliussen, member of the technical staff of Texas Instruments, Dallas. Noting that peripherals accounted for 25% of the cost of a typical minicomputer system in 1970 but could represent 80% of that cost by 1980, he points out that a similar trend affects peripheral-interface costs.

> **"Low-prestige" interface design requires both electromechanical and digital expertise.**

Concurrent I/O processing mandates removing some peripheral control functions from a CPU and placing those functions in its peripherals; controllers for those peripherals have thus themselves become special-purpose computers. The result? Peripheral interfaces have grown more expensive; the cost of those interfaces now accounts for a growing percentage of peripheral-system cost and consequently for a larger part of computer-system cost.

**Mainframe interfaces most expensive.** High-performance peripherals require the most expensive controllers, points out Juliussen, who reported his findings in September at Compcon 76 in Washington, DC. For example, an IBM 3330-2 moving-head disk drive costs $32,000, while its interface costs $74,000.

And mainframes require higher-priced peripheral controllers than minis, primarily because their I/O channels are more complex than minis' unified bus architectures. Mainframe-peripheral controllers also incorporate optional features that minicomputer systems don't require, and the competitive minicomputer marketplace helps keep mini-peripheral interface prices lower than the prices for comparable mainframe-peripheral interfaces.

But while the cost of mainframe-peripheral interfaces remains high, the relative cost of controllers for such low-cost peripherals as floppy-disk drives and cassette drives is also steep. For example, a $750 Shugart floppy-disk drive requires a $1600 interface, claims Juliussen. And an RS 232 interface for a $600 Sykes cassette drive costs $1300.

**Why so high?** These high costs result from engineering, technology and pricing-strategy factors. Many interfaces require specialized designs, must meet few design standards, are designed *ad hoc* and are often produced in low volumes. Furthermore, interface design specialists are hard to find; their relatively low-prestige jobs require both electromechanical and digital expertise, much of which is rarely taught in colleges and rarely found in texts, claims Juliussen.

Among the technology factors that influence interfaces' high cost are the current high price of A/D and D/A circuitry and a lack of specialized linear ICs. And computer manufacturers have traditionally marked up controller prices by greater amounts than they mark up computer prices.

**Help on the way.** Several developments could reverse some of these trends, claims Juliussen. Interface designers can now obtain such components as phase-locked loops and variable-frequency oscillators in linear ICs. And microprocessors make possible interfaces that are "customized" general-purpose computers rather than more expensive special-purpose units.

For high-volume systems, special-purpose LSI chips like Motorola's Peripheral Interface Adapter (designed for use with the M6800 microprocessor) and Texas Instruments' programmable interrupt and I/O chip (for the TMS 9900 micro) are now available. Additional special-purpose I/O chips will no doubt appear in the future.

The use of such chips could provide "*de facto* standardization" and produce the interface standards that mini makers, mainframe manufacturers and peripheral vendors are unlikely to agree upon separately, concludes Juliussen.

## Graphic LED module, 0.25" thick, suits portable, low-voltage display uses

Though its basic display unit currently costs about twice as much as a comparably sized CRT, a 2" x 4" graphic LED display module could eventually replace CRTs in all types of display applications, according to its manufacturer. Measuring 0.25" thick and weighing 0.5 oz/in$^2$, the device currently suits portable terminals, avionic displays, medical monitors and other devices requiring minimum weight and volume and low-voltage operation.

The Model uIS 800 LEDscreen constitutes a basic module from which designers can construct larger displays, explains Joe Aichroth, director of engineering at Integrated Microsystems, Mountain View, CA. Current configurations, of which the firm has shipped less than 100 units so far, contain red LEDs mounted on 1/32" centers.

The firm plans soon to also produce

CIRCLE 11▶

# Who's number one in PDP-11 subsystems?

# Guess again.

Wangco manufactures *more than twice as many subsystem configurations* for PDP-11 systems as you can get from DEC. Or from most system houses. And we're the only major manufacturer of disc and tape peripherals that also specializes in controllers, formatters, and software. What does this mean to you? Single source systems. Systems components designed together to work together. On-time delivery and substantial cost savings.

Wangco disc systems, incorporating Wangco's front or top loading cartridge drives or the moving head fixed disc, offer storage capacity from 2½ to 10 Mbytes per drive; up to 40 Mbytes in a four drive system. The controller, compatible with all PDP-11 software, is contained on four printed circuit boards. Full diagnostics are supplied with each system.

Wangco tape systems are composed of from one to eight of Wangco's highly reliable tape drives with formatters and a two card computer adapter interface. Formatters will handle 7 and/or 9 track drives with any two speeds from 12.5 to 75 ips formatted in NRZI, PE or Dual Density. Diagnostics and drivers are supplied with each system.

Wangco – the peripherals manufacturer that's No. 1 in PDP-11 peripheral subsystems. Call or write for full information to 5404 Jandy Place, Los Angeles, CA 90066, (213) 390-8081. In Europe contact Wangco, Inc., Postbox 7754, Building 70, 1st Floor, Schiphol-Oost, Netherlands. (020) 458269.

**WANGCO**

A UNIT OF
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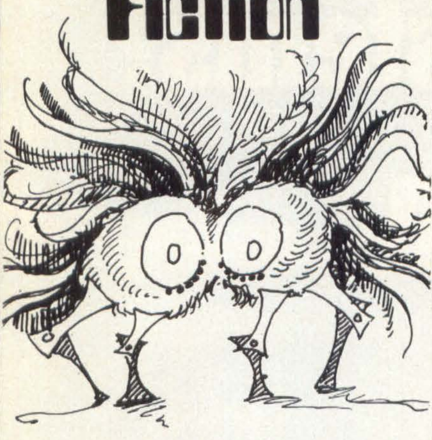

units with one green and one red LED at each addressed point in the display module; the LEDs could light separately, or simultaneously to produce yellow points in an image. Aichroth says that the current scarcity of green LEDs has so far prevented this alternative.

**$\$100$ per square inch.** Direct cost comparisons between the LEDscreen and CRT-based displays remain difficult. Aichroth quotes $\$100/\text{in}^2$ for the LED array and notes that this price represents about twice the outlay required for a 5"-diagonal CRT. But the driving circuitry for the units shipped so far has been custom designed, so no direct comparisons between its cost and that of CRT drivers exists.

The LEDscreen's drivers are more complicated than a CRT's, however. In the modules equipped with only red LEDs, a +5 V signal must go through row and column inputs to each addressed LED.

**Mass production in six months.** Based on a Litton product developed for military applications, the LED display modules should enter mass production for commercial applications in four to six months, according to Aichroth. Their resolution measures 50 lpi (max.), and each LED consumes 2 mA peak at 3 Vdc.

For applications in which a fraction of the LEDs are illuminated at any time, total power consumption remains low, according to the firm. And designers using the device can further reduce this power consumption by utilizing multiplex circuitry with a 1% to 4% duty cycle. But Aichroth concedes that the heat generated by the screen remains the manufacturer's biggest design problem and notes that because of this problem the firm has not yet constructed larger screens.

## Buffer ups throughput in satellite links

"Hurry up and wait" – the old Army maxim that refers to the interminable delays found in many bureaucratic systems can just as accurately describe the unavoidable propagation delays exhibited by all electronic systems. To compensate for the effects of such delays in satellite based data transmissions, designers at one communications firm have configured a device that allows data transmissions over a satellite link at a throughput rate limited only by the link's basic transmission rate and its data terminals' capabilities.

Basically a solid state buffer, the Satellite Delay Compensation Unit (SDCU) allows continuous data transmissions in systems with line protocols that normally use stop-and-wait transmission techniques, explains Dr. Gene Cacciamani, VP for engineering at American Satellite Corp., Germantown, MD. Such protocols, which include IBM's Bisync and Hasp Multi-Leaving, typically transmit a data block and then wait for an acknowledgement or error message before either sending a subsequent block or retransmitting.

**Half-second wait.** Because of its long transmission path, a satellite link between New York and Los Angeles introduces a 270-ms delay between data transmission and reception and an equal delay for the receipt of an acknowledgement or error message at the sender. At data rates above 2400 bps, the resulting throughput-efficiency loss grows intolerable.

## 13-mil ferrite cores bode denser memories

Envisioned for use in submicrosecond (900-ns cycle) military memory systems, a recently introduced 13-mil ferrite core will allow a doubling of current systems' memory density without any change in package size, according to the core's developers. Eventually, non-military systems incorporating similar 13-mil cores could also appear.

The core is the smallest-diameter unit currently available, says Gerald Larson, VP for marketing at Fabri-Tek, Minneapolis, MN. Most core systems now incorporate 18-mil devices. Designated Model 266, the low-drive 13-mil core switches in 270 ns, peaks in 140 ns, requires a 400 mA drive current and operates over the -55 to 100°C range. The firm has also recently unveiled a 32K x 18 military memory system, designated MMS/32, that incorporates the 13-mil unit.

**The time has come.** In 1972, the company introduced a high-drive 14-mil core, but that device was "ahead of its time," according to engineering manager Al Shimp. Although the 14-mil device has found uses in some custom applications, where it competes with semiconductor memory, users have generally not been willing to pay for the increased performance it offers.

# faster, low-cost mass storage

Here is some very persuasive copy about the
new AED 8000 mass storage $\mu$controller for PDP-11 and NOVA/ECLIPSE large disk systems:

| Characteristic | AED 8000 | RP11-C/RPO3 | 4231/4331A |
|---|---|---|---|
| Quantity 1 price | **$17,500** | $33,000 | $30,000 |
| Megabytes per drive | **67.4 → 250** | 40 | 92 |
| No. of drives per controller | **1 → 15** | 8 | 4 |
| Megabytes per controller | **540 → 3,800** | 320 | 368 |
| No. of CPUs per controller | **4** | 1 | 2 |
| 16 bit transfer rate | **1.6 $\mu$s.** | 6.4 $\mu$s. | 2.5 $\mu$s. |
| 16 bit buffer | **256** | 6 | 8 |
| Error Correction Code | **by controller** | none | none |
| Bootstrap | **IPL in controller** | CPU ROM | CPU ROM |
| Micro-processor | **40 ns. 24 bits** | none | none |
| · Emulates DEC/DGC controllers | **yes** | – | – |
| · Macro Instruction Code | **yes** | none | none |
| · Data Scanning & Management | **in controller*** | in CPU | in CPU |
| · Variable Sector Length | **yes** | none | none |
| · CPU to CPU transfers | **bypass the disk** | none | via disk |
| Delivery | **60 days** | ask them | ask them |

*With extra microcode.

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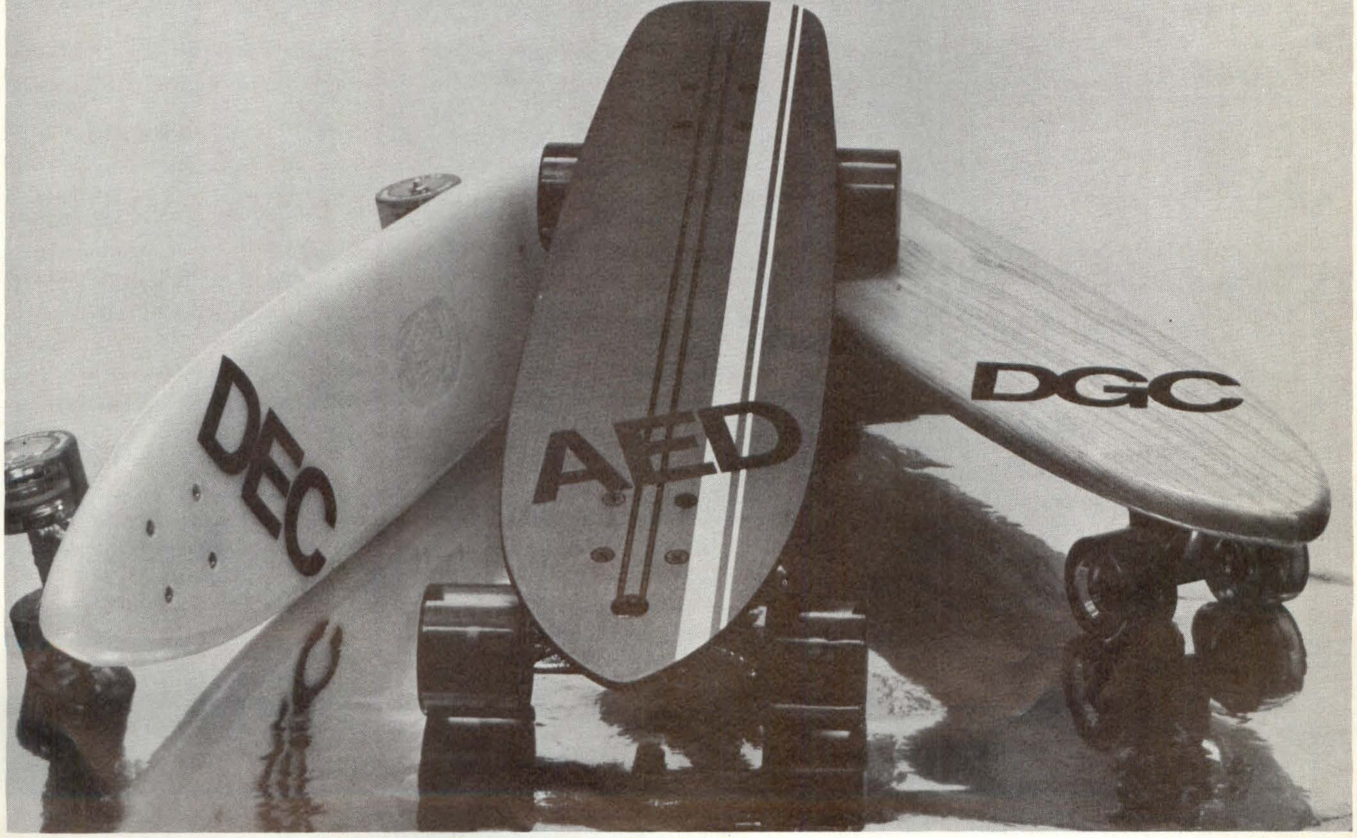
Telephone: 408-733-3555 Telex: 357489



CIRCLE 13

# microprocessor very much.

All it does is process numbers.

Other microprocessors do almost anything you tell them to. And that's proven to be an industry-shaking advantage. But in certain cases there's a hitch. Programming can be kind of hairy, and in many applications general-purpose microprocessors can be cost ineffective.

Our new MM 57109 dedicated microprocessor (the Number Cruncher) is our answer.

It's pre-programmed to do a wide variety of math functions (including log, trig and functions of x), and do it more efficiently, reliably and cheaply.

Use it as a stand-alone or as a satellite to your general purpose microprocessor.

And the price tag?

In quantities of a hundred, a mere $12.

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Gentlemen:
I don't have very much for a microprocessor to do, so send me details on your microprocessor that doesn't do very much.

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# High software costs prod tester designers to swap in-house μC for mini maker's unit

Having chosen to develop their own microcomputer for use in an automatic circuit testing system, engineers at GenRad's Test Systems Div., Concord, MA, remained undaunted by the potential problems in software development they faced. Although the design was the firm's first using microprocessors, says product engineering manager Thomas Coughlin, an existing software development facility should have eased the task of providing support software for the venture.

But Coughlin and his colleagues soon discovered that "as today's advertisements state, microcomputer design is a snap. From a hardware viewpoint, that is." And rather than continue spending large sums on software development aids for the in-house microcomputer, they re-evaluated their design philosophy and chose instead to configure the testing system around a fully designed and documented microcomputer offered by a minicomputer maker.

**Duplicating existing efforts.** In a report to Wescon, Coughlin explains that when the firm first began developing the Model 2230 module test system about three years ago, only one commercially available chip set – National Semiconductor's IMP-16 – offered the speed and instruction set the designers required at the price they were willing to pay. The team's original goal was to use the CPU and control ROMs from this chip set as the heart of the module tester's microcomputer, whose software – 16K bytes of code committed to masked ROM – would be developed on GenRad's existing net.

That net, a multi-user, multi-computer system, incorporates a central station with printers and multi-disk storage units (backed up by magnetic tape) as well as five local user stations, each equipped with a DEC PDP-8 minicomputer, a disk storage system and a video terminal. It also connects to several PDP-8 or PDP-11 based prototype development and product integration systems. Engineers develop programs on the net using a custom designed high-level language.

As software development for the project proceeded, the designers realized that the circuit testing system's 16K byte program length was ill-suited to the then-available microprocessor prototyping kits and large-business-machine oriented assemblers. They developed their own cross-assembler and simulator to run on a minicomputer system, but soon realized that

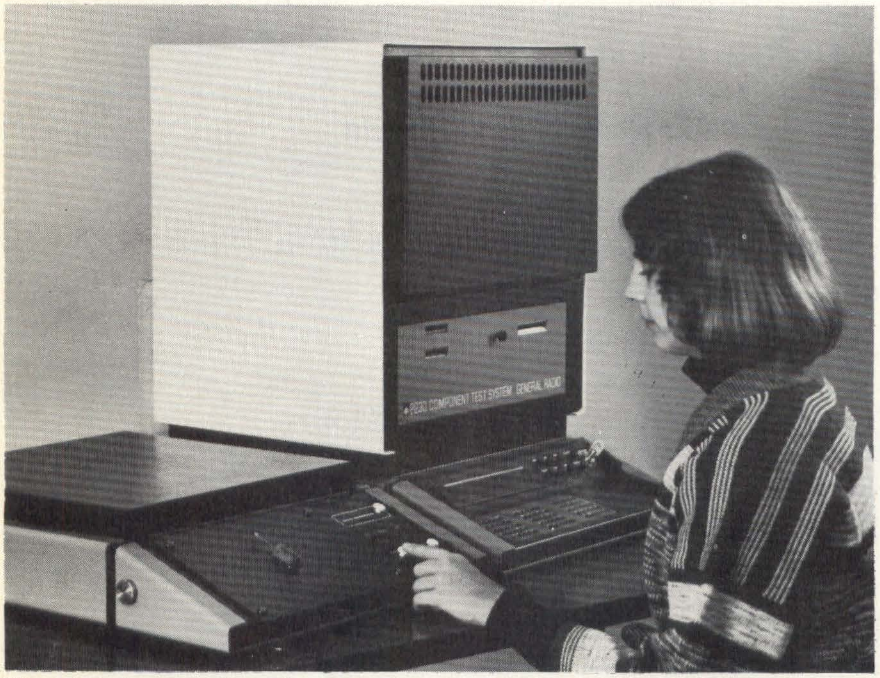
★ They were duplicating their existing software development center

★ They had spent large sums and hadn't even begun to develop the code for the tester systems or the diagnostic and testing routines for that code

★ They were losing product ties to other product lines.

**The big switch.** At this time, minicomputer houses began offering microcomputers, and the team changed its goals and replaced the in-house microcomputer with a DEC LSI-11. Coughlin reports that the switch upped recurring costs but lowered total cost – including software development time, documentation, testing and service setup – by about one-third.

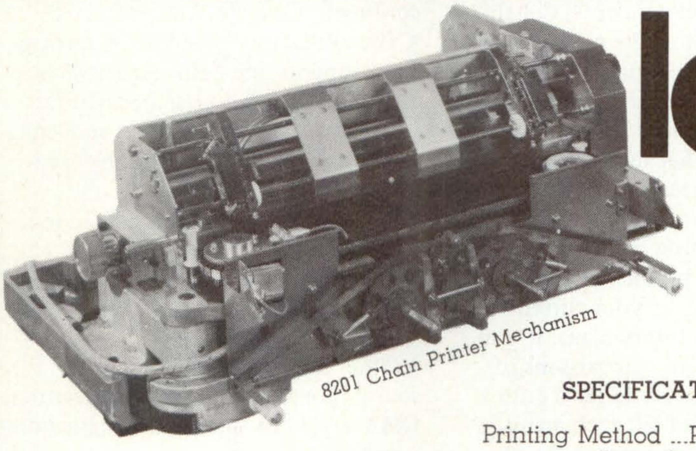
The designers reconfigured the tester's software development system around a PDP-11/35, 72K of core, four disks and several I/0 peripherals, all linked to the central development net. A prototype hardware development station, consisting of another PDP-11/35, 28K of core, a teletypewriter and



**When they discovered that software development costs for their Model 2230 circuit testing system were soaring and that development efforts were duplicating a current development system, engineers at GenRad's Test Systems Div. replaced the unit's in-house designed microcomputer (built around a National Semiconductor IMP-16 CPU) with a fully documented Digital Equipment Corp. LSI-11.**

## Heavy-duty
## 300 LPM-132 COL.

# Chain Printer Mechanism at low cost.


8201 Chain Printer Mechanism

**DOT MATRIX IS NOT** the only technology that can reduce your printer cost.

**MECHANISM-ONLY IS SUFFICIENT** for those who have the capability to produce interface, power supply and cabinet. We can also help you in your design needs.

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Reliability, print quality, high maintainability and low cost are outstanding features of the 8201 Chain Printer Mechanism. Designed and produced by one of Japan's leading watch manufacturers—Citizen Watch Co., Ltd.—it has been incorporated into final products by 20 computer system manufacturers and suppliers in the past 2 years. And price-wise it competes aggressively with today's 165-200 cps dot matrix printers.

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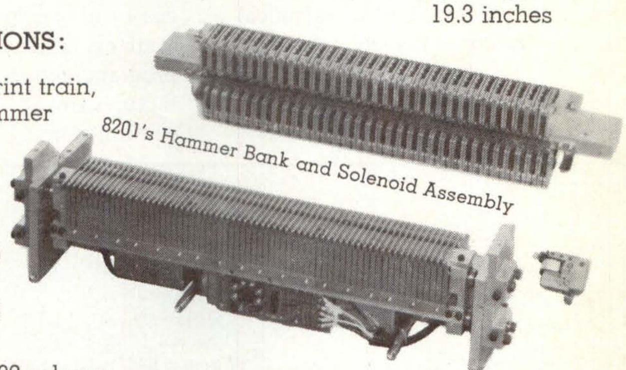
SPECIFICATIONS:

| | |
|---|---|
| Printing Method | Print train, flying hammer |
| Printing speed* | 298-529LPM (48 Characters)<br>250-397LPM (64 Characters)<br>188-265LPM (96 Characters) |
| Number of columns | 132 columns |
| Number of characters | 48, 64 or 96 |
| Character spacing | 10 characters/inch |
| Line spacing | 6 lines/inch |
| Width of print paper | Max. 16 inch |
| Number of copies | 6 (including original) |
| Paper loading | Swing gate |
| Paper feed* | One pair of pin feed tractors, 14 in./sec. (clutchless drive system) |
| Inked ribbon | 1.18 inch W x 132 feet L |
| Inked ribbon feed | Special gear train |
| Frequency | 50/60Hz ± 1Hz |
| Size (HxWxD) | 11.3 x 24.8 x 19.3 inches |
| Weight | Approx. 80 lbs. |
| Noise level* | 68 dB full line printing |
| Operating condition* | Temperature: 40-105°F (5-40°C)<br>Humidity: 30-85% |


8201's Hammer Bank and Solenoid Assembly

*Varies according to customer's design.

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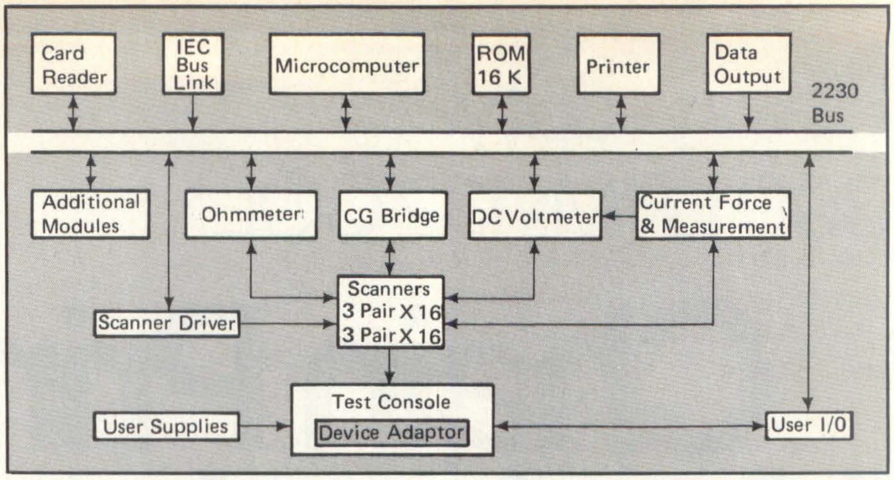
CIRCLE 14

the hardware under development, connects to the tester's software development system. Additional prototyping systems, each designed around an LSI-11, run under the control of EPROM or of RAM loaded from the main system; all program development occurs in assembly language.

"The commitment to such an elaborate software development center was instrumental in accelerating the (testing) system's introduction to the market," claims Coughlin. But the costs weren't minimal; he estimates that software development costs equaled those for the tester's hardware – one finished, documented word cost $7 and required one-half to two-thirds of an hour of development time.

**Meeting design goals.** The testing system's final configuration includes an LSI-11, 16K of ROM, a card reader/writer, a printer, an alphanumeric display, a keyboard for macro-instructions and various measurement modules. Its software consists of a parser that translates keystroke phrases into reduction numbers, which go to a "tree builder and optimizer" that functions like a compiler. This routine calls on action routines that help it create an optimized stored program.

According to Coughlin, the completed tester meets all of its technical and cost objectives, which include a selling price under $20,000, benchtop packaging and the ability to test all 15 resistors in a pull-up network to their limits in less than 250 ms.



**The microcomputer based circuit test system can test all 15 resistors in a pull-up network to their limits in less than 250 ms.**

**Lessons learned.** Looking back over the design team's experiences, Coughlin notes that most of the philosophies governing the application of a microprocessor to a new product either scare potential users or make the application appear so simple that the users rush headlong into increasingly expensive developments.

Treat the selection of a microprocessor as a systems problem, he urges; consider its impact on your current facilities and your future plans. If you can't run benchmark comparisons of available units, at least define a critical program section and ask each manufacturer to code it and report the execution time.

Additional important factors that govern microprocessor selection, according to Coughlin, include:

★ The availability of software development support, including an assembler, a text editor, a linker, a loader, a fast hardcopy capability, a command language and an on-line debugging capability

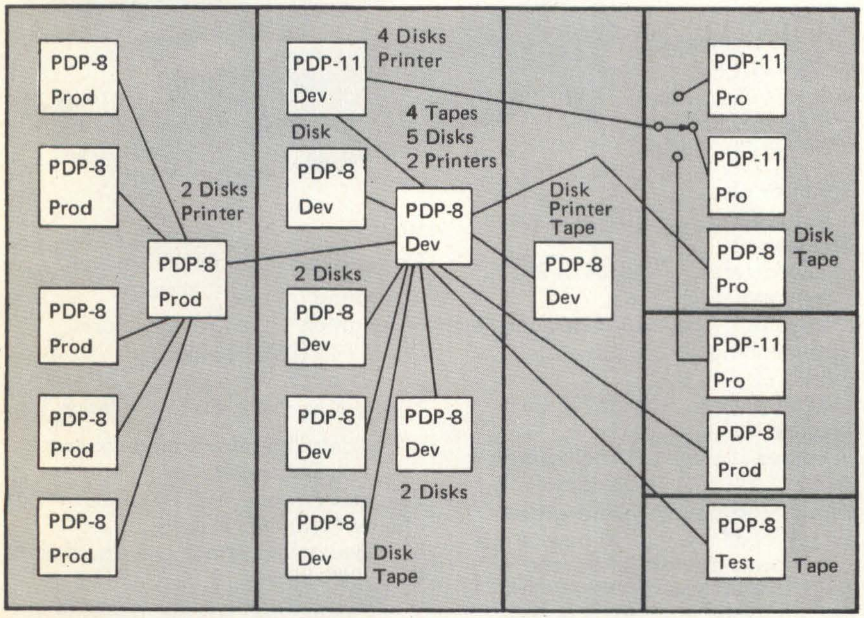
★ A well-developed and accepted instruction set

★ Reliability, user acceptance and cost

★ Testing capability

★ Supplier support

★ Other factors, including second sourcing, execution speed, I/0 features, DMA capability and microprogramming capability.



**Computer network at the GenRad Concord, MA, facility incorporates software development systems (Dev), prototype hardware systems undergoing development (Pro) and product systems undergoing integration. The main software development station uses a DEC PDP-8 equipped with four tape drives, five disk units and two printers; it connects to five other PDP-8 based development stations and to prototyping and production systems. After choosing an LSI-11 as the circuit tester's microcomputer, the tester's design team was able to integrate the tester's PDP-11 based software development system into the net.**

# Workshop to stress down-to-earth design

Aimed at designers who require practical experience in microprocessor based circuit design, a 3-day workshop scheduled for June 10-12 in Philadelphia will provide information on $\mu$P-system software, hardware and debugging techniques. The workshop's organizer claims its attendees will learn how to incorporate microprocessors into designs without the use of expensive program-development equipment.

K. V. Amatneek, consultant at Hahnemann Medical College, Philadelphia, and chairman of the Philadelphia IEEE section's Committee on Professional Update, expects that $\mu$PIEEE-77 will provide a forum for the exchange of microprocessor-system designers' experiences and a source of expertise for first-time microprocessor users. Participants will learn about the pitfalls and shortcuts of firmware writing – and about the design-bench tradeoffs between firmware, software and hard-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ware – from fellow designers who have dealt with such problems.

The workshop will stress a practical engineering approach to microprocessor-system design, says Amatneek. Proceedings will be published beforehand and mailed to participants; workshop sessions will focus on discussions, questions and answers, and demonstrations of participants' designs rather than on paper readings.

**Workshop information.** Amatneek seeks papers on μP-system software, hardware and debugging from circuit designers with a practical engineering approach to μP-system design; all hardware papers accompanied by working boards will be published in the workshop's proceedings. The deadline for paper submissions is Feb 1, although he anticipates that papers arriving after that date will still be considered.

For more information on the workshop, contact Helen Yonan, Philadelphia IEEE, Moore School, University of Pennsylvania, Philadelphia 19174.

## Multi-CPU arrays optimize μP systems, but software scarcity now bars their use

A system that uses 90% of its microprocessor's throughput capacity requires programming three times costlier than a 50%-utilized system's. So keep your system's operational throughput requirements at or near the 50% level, even if that goal requires using more than one processor.

So concludes John Clark, manager of computer systems at Magnavox's Torrance, CA, facility, and he points out that two basic techniques can keep throughput utilization near this desired 50% level. First, filters or other bandwidth compression techniques can operate on your system's microprocessor inputs; such techniques have seen successful use in minicomputer based projects, where CPU cost constitutes "a substantial fraction" of total system cost and using multiple CPUs proves uneconomical.

Second, because microprocessors cost far less than minis, several of them can serve one system whose operation is segmented into a series of less demanding tasks. For example, in a high-resolution radar target tracking system, a microprocessor could handle data for each 1° azimuth slice; the resulting 360 data streams could then go to a common processor for further analysis.

**Wanted: software.** One stumbling block remains before designers can configure such systems of sequential microprocessing elements, says Clark. Microprocessor manufacturers will not only have to develop their products for use in multiprocessing configurations; they will also have to develop software to serve such applications.

Microprocessor makers are generally not in the systems business, and – at least initially – have served applications that don't require sophisticated software tools. And unlike minis and mainframes, most microprocessors replace discrete logic in existing designs; typically they don't function as general-purpose, user programmed devices.

**Compilers wanted.** The need for software has increased, however, and as more designers unskilled in assembly language programming attempt to utilize microprocessors, the need for higher-order language compilers has also grown, claims Clark, who reported to Compcon 76 on the user's view of microprocessor software.

He favors using a Fortran compiler that produces as its intermediate output assembly language programs in source code, and he urges microprocessor makers to provide such compilers as standard software packages. A system designer could use such a compiler to develop a program, then check the program on a host computer, then optimize the assembly language intermediate output, one segment at a time.

**Language tradeoffs.** But what of the argument that assembly language programming produces more efficient code than a higher-level language? True, for high-volume applications with small memory requirements, assembly language programming is most efficient, says Clark. But smaller-volume applications might economically utilize programming written in higher-level languages. His analysis produces a general formula for finding the tradeoff point; an actual estimate (*Digital Design*, August, page 25) shows that production volumes less than about 10 or 20 units mandate using higher-level programming.

Even though compilers for higher-level languages make relatively inefficient use of microprocessors' instruction sets, so do most assembly language programmers; even experienced programmers seldom utilize more than half of a microprocessor's available instructions, according to Clark.

## Hardware/services

**$995 computer.** Incorporating I/0 devices and interfaces, memory, software and keyboard, this 8080-based small computer – designated Sol-20 – comes assembled or in kit form. Components include a 1024-character video display circuit, 1024 words of static low-power RAM, 1024 words of preprogrammed PROM and a custom 85-key solid-state keyboard. Other features include an audio cassette interface that can control two recorders at 1200 baud, parallel and serial standardized interface connectors, a complete power supply including fan and a cabinet with solid walnut sides. Software includes a PROM personality module and a cassette with Basic-5 language plus two computer video games. Processor Technology, 6200 Hollis St., Emeryville, CA 94608. (415) 652-8080 **Circle 140**

**PROM programmer.** For use with the manufacturer's Altair 8800 computer systems, the 88-PPC programs standard 1702A(256-byte) erasable PROMs in less than three minutes. It consists of a separate chassis (10.6" x 4.2" x 11") equipped with a 24-pin zero insertion force socket and connected to the 8800 through an interface card that plugs into the Altair bus. The programmer has a self-contained power supply, and the interface card requires less than 500 mA from the +8 V bus in the 8800. The programmer functions like an addressable 2-channel output port; the even address channel outputs to a "control latch" in the programmer while the odd address channel outputs to either an "address latch" or a "data latch," depending on the state of the fourth bit in the "control latch." The 8800 controls all programmer timing through its software driver. Price (assembled unit only): $456. Mits, 2450 Alamo S.E., Albuquerque, NM 87106. **Circle 138**

*Cont'd p. 25*

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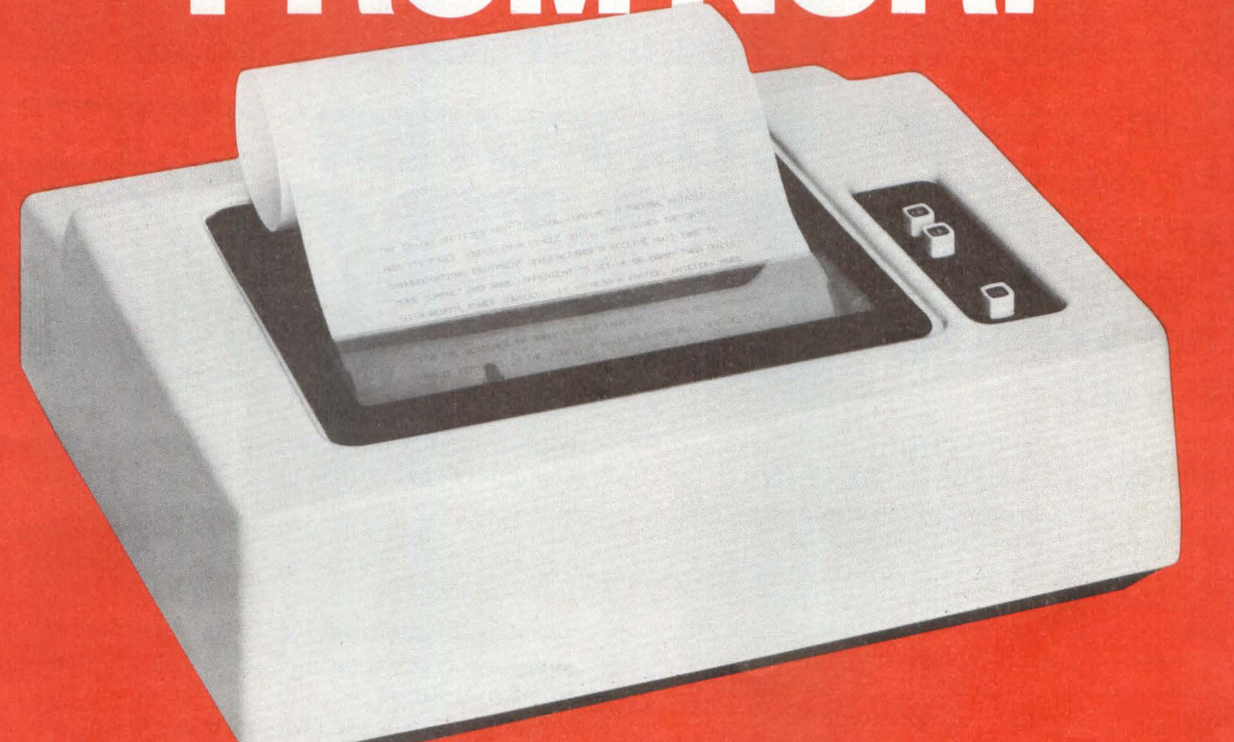

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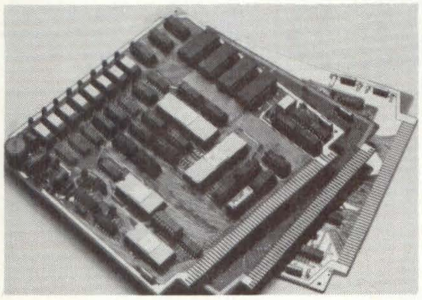

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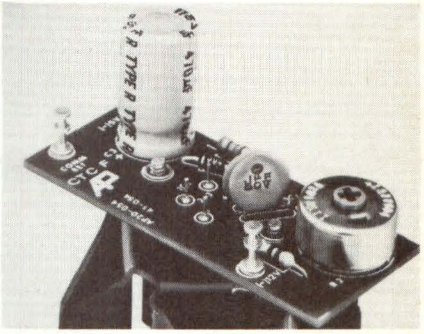


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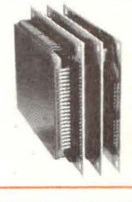
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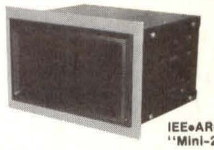
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# Programming novices use µP-based tester to study effects of alchohol and drugs

Experimental subject attempts to match movement of two light spots on a 5" CRT (arrow) while also responding to secondary stimuli from lamps and LEDs ringing the CRT. Sensor in ring tracks eye movement.

Designed for use by psychologists untutored in computer programming, a microprocessor based reaction tester provides those investigators with potentially valuable information on how individuals respond to alchohol and other drugs. By choosing sequences of 2-character mnemonics from a "catalog" of possible operations, the psychologists program the Stimulus Programming System (SPS) to compare a subject's normal performance with his performance "under the influence."

Such comparisons are important, explains system developer Dr. Gershon Weltman, because psychologists have discovered that for a given amount of alcohol intake, a driver's ability to handle a car's wheel, brakes and accelerator (the driver's primary task) is less impaired than the ability to handle such secondary tasks as observing other cars, pedestrians and traffic signals. The SPS helps researchers quantify these differences in ability.

President of Perceptronics, Woodland Hills, CA, Weltman notes that the SPS' National Semiconductor IMP-16 microprocessor, equipped with a 4K RAM, assembles the strings of 2-character mnemonics loaded into it on paper tape by an experimenter. It then generates the stimuli for a test run, records the subject's magnitude of error and elapsed reaction time to the stimuli, and outputs this data to a printer.

**Reprogramming required after shutdown.** The SPS incorporates no ROM; thus, its programming vanishes with system shutdown and must be reloaded from paper tape each time the system is powered up.

Weltman explains that the stimulus programs vary with researcher and subject and that paper tape is less expensive than PROMs for such a programming application. He also notes that researchers at the Southern California Research Institute (SCRI), Los Angeles, favored this approach because they anticipated using the system like a general-purpose computer by modifying its operating program themselves.

**Subjects track light spots.** In a typical test, a subject sits in a chair about 4 ft from a 5" CRT, on which appear two light spots. A pseudo-random function generator controls the movement of one spot and also supplies position signals to the microprocessor.

### Programming The Reaction Tester

A key feature of the microprocessor based tester, according to developer Gershon Weltman, is its programmability by personnel unfamiliar with programming techniques. A catalog supplied by the system's developers provides a 2-character mnemonic for every possible system function an experimenter can specify; the experimenter need not worry about memory locations or computer-program format.

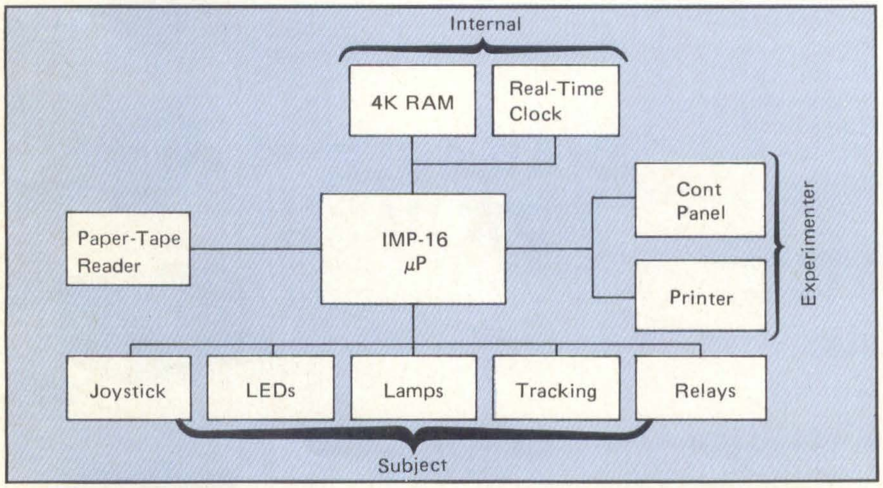
To prepare an instruction tape, an experimenter first divides the desired system operation into sequential blocks. One parameter-sequence block, written in conversational format, might read:

> I want the maximum allowable response time for each peripheral lamp to be 100 sec from the time the lamp first turns on. Next, I want the maximum response time for each target LED associated with a lamp to be 8 sec, measured from the time the target turns off. Each lamp must be on for 4 sec, each target LED for six sec, all other LEDs for 100 sec. All non-target LEDs must remain on when target feedback is satisfied, and a target LED should change to '0' when that condition occurs.

The code string corresponding to this statement is

SB1 PM100 0 TM8 1 PD4 TD6
ND100 PF2 TF2 NFO FVO

After generating it, the experimenter uses a similar procedure to generate a string of code corresponding to the desired instruction sequence. Other sequence blocks specify such test requirements as the color of the ink in the system's printout.



Coding for a typical experimental run in the reaction tester occupies about 2K of RAM. Because the coding varies considerably for different experimenters and subjects, the tester's designers opted for program storage on cheap paper tape rather than PROM; the provision means that experimenters must reload the system's programming after each power shutdown.

The subject's primary task is to track this spot of light by duplicating its motion with the second spot of light, which moves in response to a joystick under the subject's control.

**Adding secondary stimuli.** But the subject must also perform a secondary task. The panel that houses the CRT also houses 40 incandescent lamps on its centerline, 20 on each side of the CRT. Two rows of alphanumeric LED characters appear above these lamps, and two more rows appear below them.

Programmed by the experimenter (*see box*), the microprocessor lights these lamps and alphanumeric characters in various sequences, and the subject must respond to these secondary stimuli by either pushing a button when a specified letter or number appears or moving the joystick to the quadrant in which he thinks that letter or number appears.

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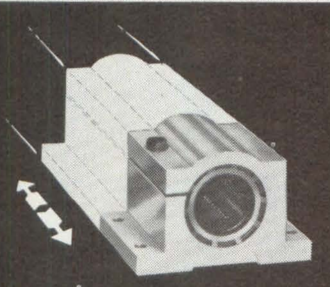

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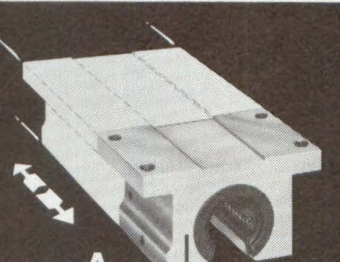

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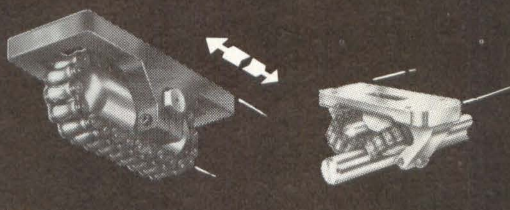

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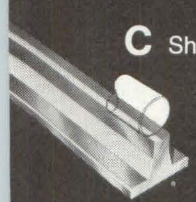

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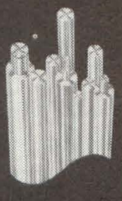

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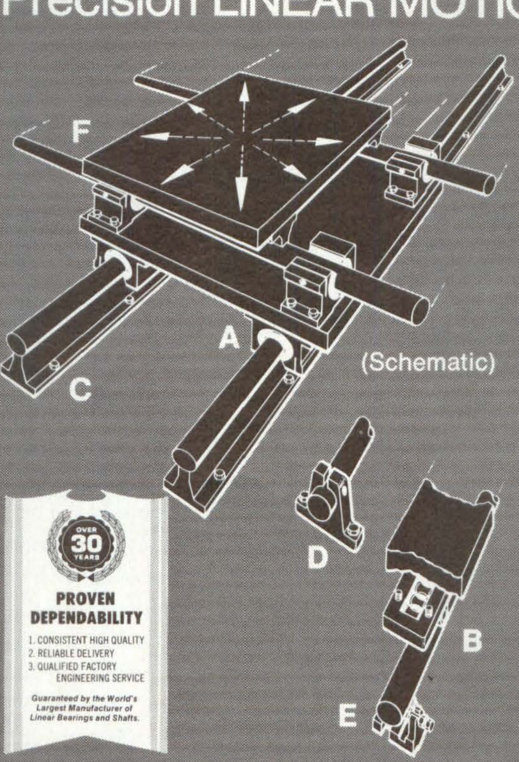

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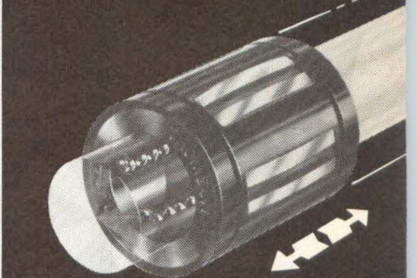

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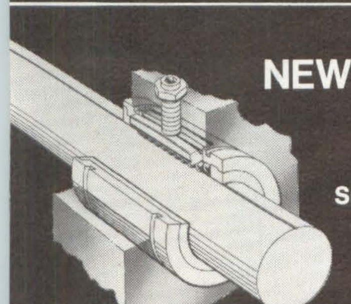

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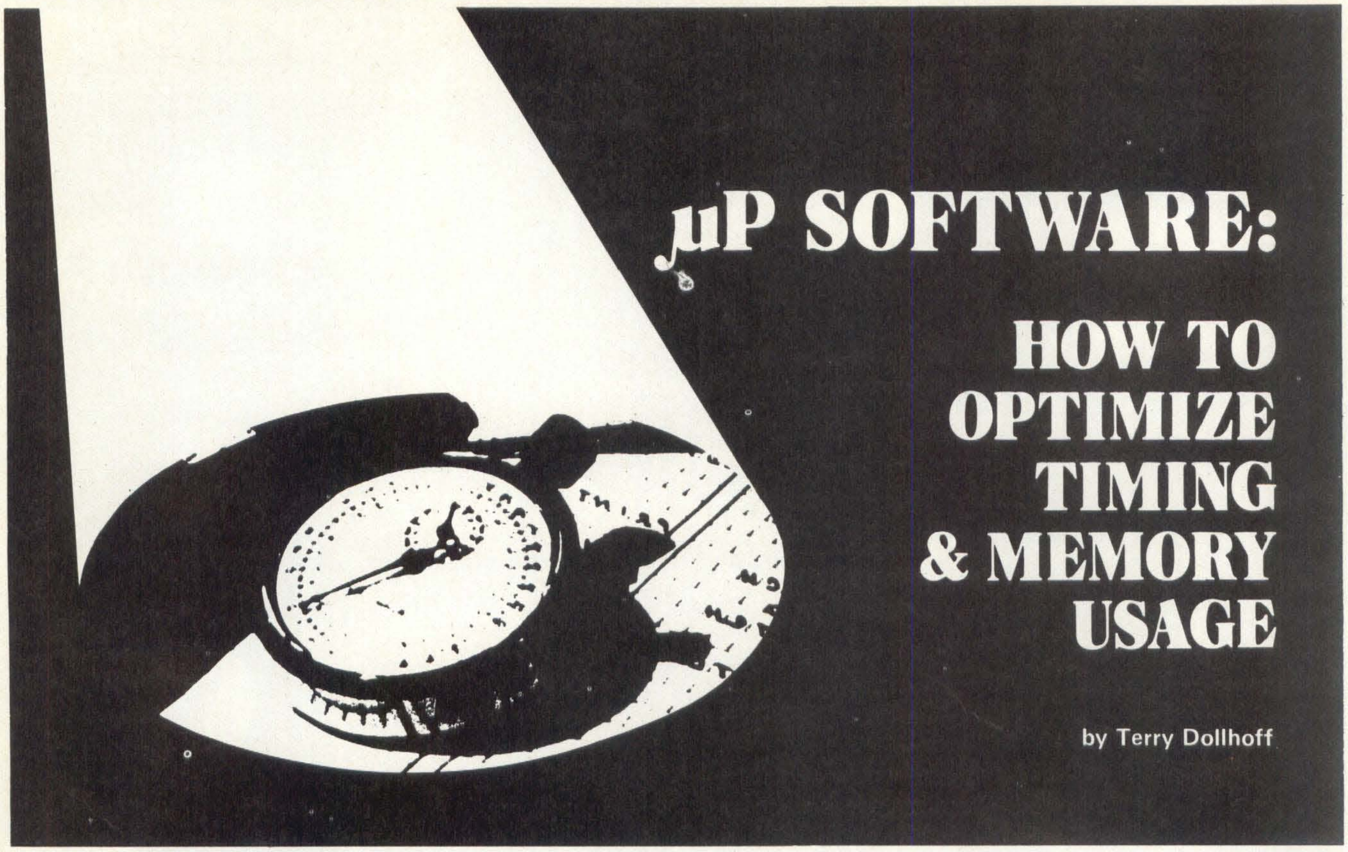
### PART THREE: TECHNIQUES FOR THE FAIRCHILD F8



# µP SOFTWARE: HOW TO OPTIMIZE TIMING & MEMORY USAGE

by Terry Dollhoff

This month's subject for programming tips is the Fairchild F8, an 8-bit microprocessor. Second sourced by Mostek, the F8 is used in several large-volume controller applications; for example, two major gas pump manufacturers have opted for F8-based designs. The F8 has such popularity as a microcontroller because it requires a minimal amount of external hardware – you can build a 2-chip system with this device. Indeed, Mostek will soon provide a single-chip F8, an offering certain to increase the F8's use as a controller.

Because the F8 isn't a single-chip processor, you can build several hardware systems from the basic chip set. Any individual hardware configuration will impact the software in one way or another, so I'll explore the F8's hardware characteristics in a fair amount of detail.

## system architecture

The basis of any F8 system is the CPU chip. Designated the 3850, this chip provides basic processing capability and working registers (Fig 1). But it doesn't include program counter or memory address registers, which are located in one of the companion chips. Removing the addressing registers eliminates the need for an address bus, which in turn reduces the system's pin count (The CPU and support chips are all 40-pin devices). The 3850 also incorporates two I/0 ports, system clock generation and power-on reset.

In addition to the CPU chip, an F8 system includes one or more support chips:

★ Program Storage Unit (3851). This device incorporates a masked ROM, two 8-bit I/0 ports, a programmable timer and external interrupt control. If you combine the PSU with the 3850 chip, you obtain the minimal F8 system (Fig 2), which provides 1K bytes of ROM, four 8-bit I/0 ports, 64 bytes of RAM (the CPU has 64 registers) and a programmable timer. The cost of such a 2-chip system is well under $20, even in modest quantities, so you can see why the F8 is a popular controller choice.

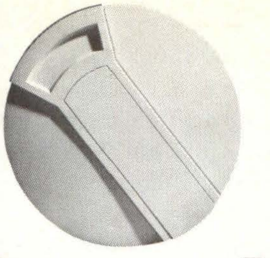
★ Memory Interface Units (3853 and 3852). Because the CPU doesn't contain a program counter or other memory addressing registers, you must add another chip if you wish to interface the CPU with ROM, PROM or RAM. The Static Memory Interface (3853) and Dynamic Memory Interface (3852) perform this task by providing the required address and refresh circuits. The memory interface chips also provide the address bus not found on the basic CPU.

★ Programmable Input/Output (3861). This chip is a subset of the PSU and includes all of the PSU features except masked ROM. It provides added I/0 capability or another programmable timer.

★ Direct Memory Access (3854). Most microprocessor systems achieve DMA by forcing the processor to wait or hold. But because the F8 does not provide a hold or wait input, you must add the DMA chip to the system if you desire this function. The addition doesn't represent a major increase in system components, because you'll always require external logic to control the hold input anyway. One possible version of a full-up F8 system appears in Fig 3.

Cont'd p. 30

**Terry Dollhoff** *is director of computer science at Acuity Systems, Inc., Reston, VA.*



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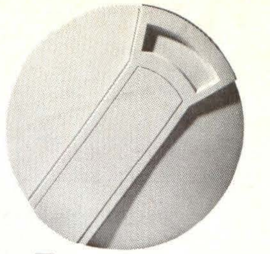

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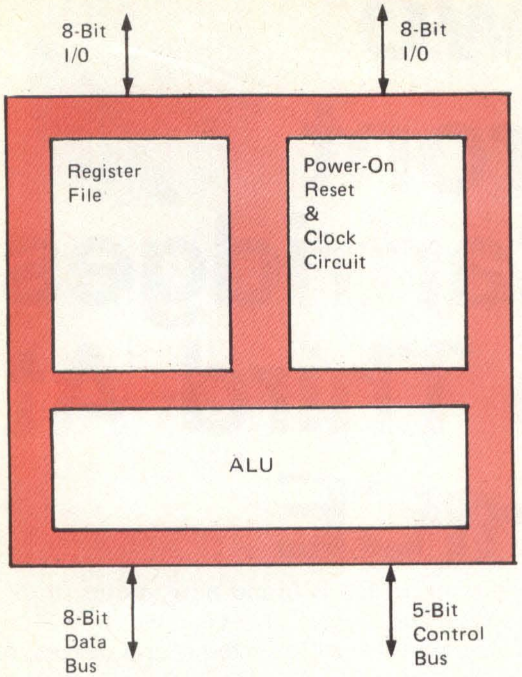

**Fig 1 Designated the 3850, the Fairchild F8 CPU chip provides processing capability and working registers but lacks program counter or memory address registers. The lack of address registers eliminates the need for an address bus, which in turn cuts systems pin counts.**

## internal architecture and addressing

The F8 CPU incorporates an 8-bit accumulator and 64 scratchpad registers. You can only address the first 16 of those scratchpad registers directly; you must access the rest through an additional register – ISAR.

In addition to the CPU's registers, an F8 system incorporates three others – program counter, data counter and program counter stack register (Fig 4). The first is a 16-bit register used to select the next instruction from memory; the second resembles the (H,L) register pair of the Intel 8080 and addresses memory. (Unlike the 8080, however, the F8 can only address memory via this register.) The program counter stack implements subroutine and interrupt linkage; each time your program makes a subroutine call or reaches an interrupt, the return address goes to this register. You must save this register's contents if you plan to make additional subroutine calls.

The F8 offers several addressing modes, many of which are unlike those I've discussed in previous articles:

★ Register addressing. The operand lies in one of the general registers. For arithmetic or logical operations, the first 12 general registers (R0-R11) can be directly addressed. For example,

```
        AS      R10             ;A=A+R10
```

adds the contents of register R10 to the accumulator and places the result in the accumulator.

★ Scratchpad addressing. The operand lies in the scratchpad register whose register number lies in ISAR. For example, if ISAR = 35, scratchpad addressing selects scratchpad register 35. This addressing mode is the only way you can access registers 16-63. Three variations exist: (1) S – The operand is selected by ISAR; (2) I – Same as S, but the lower-order three bits of ISAR are incremented after the scratchpad register is accessed; (3) D – Same as S, but the lower-order three bits of ISAR are decremented after the scratchpad register is accessed.

Notice that only the lower three bits of ISAR change during a scratchpad reference, so you'll find it convenient to access scratchpad registers in groups of eight. Indeed, whenever the lower-order three bits of ISAR are set, a condition code is also set. A branch operation on ISAR lower not equal to 7 is provided as part of the branch repertoire and is useful for loop control.

★ Immediate addressing. The operand lies in the byte following the instruction. For example,

```
        AI      H'12'           ;A=A+12 (hexadecimal)
```

adds the hexadecimal value 12 to the accumulator and places the result in the accumulator. (As with the microprocessors I've discussed previously, the F8 uses a special designation to represent hexadecimal constants (H'12' above). This method is in my opinion the most awkward and is definitely the most error-prone of the several possible representations.)

★ Immediate addressing (short form). You can use this unusual mode of addressing to greatly decrease program size. The operand lies in the lower four bits of the instruction. Thus, this one-byte instruction

```
        LIS     3               ;A = 3
```

loads the accumulator with the constant 3.

★ Relative addressing. This addressing mode determines the destination address for all but one of the F8's jumps. The operand address is formed by adding the second byte of

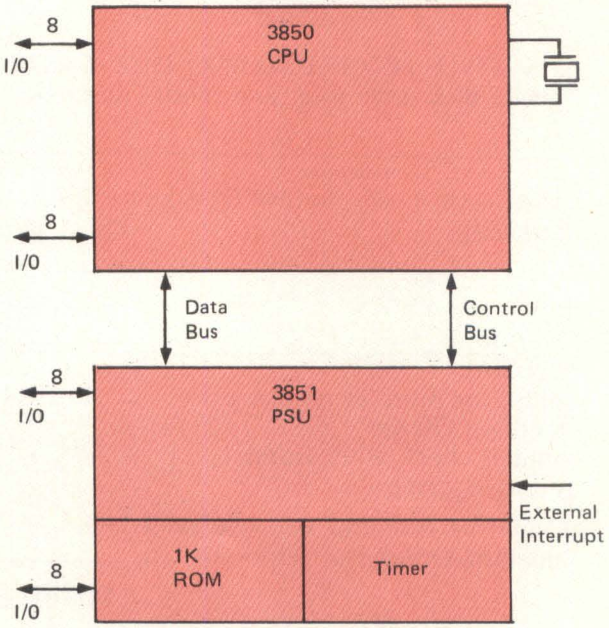

**Fig 2 Costing less than $20 even in small quantities, the minimal F8 system incorporates a 3850 CPU and a 3851 program storage unit, which provides masked ROM, two 8-bit I/O ports, a programmable timer and external interrupt control.**

the instruction to the address of the opcode plus one, a calculation slightly different from the relative address calculations I've discussed before. One method is as good as another, but you must be careful to compute the address carefully if you try to patch a program – a procedure you should try to avoid. This relative addressed instruction transfers control to the current location plus 11:

```
        BR        10                  ;jump relative (PC+1) + 10
```

★ Direct addressing. The operand lies in the memory location whose address lies in the second and third bytes of the instruction. Direct addressing provides access to any of the 65,536 locations in the memory addressing space. Only three instructions use this form of addressing – jump, call to subroutine(PI) and load data counter (DCI). For example, this instruction loads the data counter with 1234(hex):

```
        DCI       H'1234'     ; load data counter with 1234
```

★ Memory addressing. The operand lies in the memory location whose address lies in the data counter (DC0). After referencing the operand, the system advances the data counter by one, a process that can be very useful for manipulating data in memory.

Fig 5 summarizes the entire F8 instruction set and shows the mode of addressing for each instruction. Wherever the symbol r appears (for example Cr for add), r can be a scratchpad register (0-11) or scratchpad indirect (I, S or D).

## instruction oddities

The F8 instruction set exhibits a few characteristics that are atypical and therefore worthy of special attention. If you aren't aware of some of these oddities, you might incorporate hard-to-locate bugs in your programs.

The F8's condition codes differ from those of most other microprocessors; the carry and zero are the same, but the sign flag is different. In particular, S=1 implies a positive result. If you use only the basic branches (for example, BP or BM), this limitation shouldn't present a problem, but if you prefer to "roll your own" (using the branch on condition true or branch on condition false operations), be careful not to reverse your intended test.

Whenever the system executes an extended jump or subroutine call, it modifies the accumulator. This operation is clearly described in the F8's manual but is very easy to forget. It also eliminates one method of passing parameters to subroutines – via the accumulator.

The F8 has one design error you should be aware of. Most F8 systems provide two data counters (DC0 and DC1), but some chips in the system only provide one (DC0). Whenever you load the data counter, all DC0 registers are loaded accordingly. But when you exchange the data counters (using XDC), the chips that have only one data counter simply ignore the operation. If your system contains one chip with two data counters and one with only one (for example, CPU, PSU and SMI) this sequence will produce improper memory addressing:

```
LOOP    LM                            ; load (DC0)
        XDC                           ; exchange DC0 and DC1
        ST                            ; store (DC1)
        XDC                           ; exchange DC0 and DC1
        BR        LOOP                ; continue
```

The sequence isn't unusual, because it is a good way to copy one area of memory to another. The manufacturer's literature doesn't describe this problem, but you should be aware of it if your system has a mixture of the two types of chips.

The F8 performs compare operations unlike other microprocessors. In particular, it subtracts the contents of the accumulator from the compare value; most microprocessors do the reverse. This isn't a major problem, but you should be aware of it. And you might also note that there's no compare with the scratchpad – only with a constant or with memory. To compare the accumulator with the scratchpad, you can place the value in RAM and then use a compare with memory – an impractical operation because of the F8's RAM addressing scheme. Or, you can use the logical or arithmetic instructions. If you must merely compare for equality, you can use

```
        XS        R2                  ; A = A xor R2
```

The exclusive OR produces zero only if the register's contents equal the accumulator's. If you must check relative magnitudes, you can use these three instructions:

```
        COM                           ; A = one's complement of A
        INC                           ; A = two's complement of A
        AS        2                   ; A = R2–A
```

This sequence also illustrates two other important features of the F8 – it doesn't provide a two's complement instruction, and it doesn't provide a subtract.

All memory references in the F8 occur via data counter DC0. After a memory reference the data counter is incremented to accommodate the next data transfer; a process that can be helpful in reducing program size. But don't forget about this automatic increment or you may create some difficult debugging for yourself.

*Cont'd p. 32*

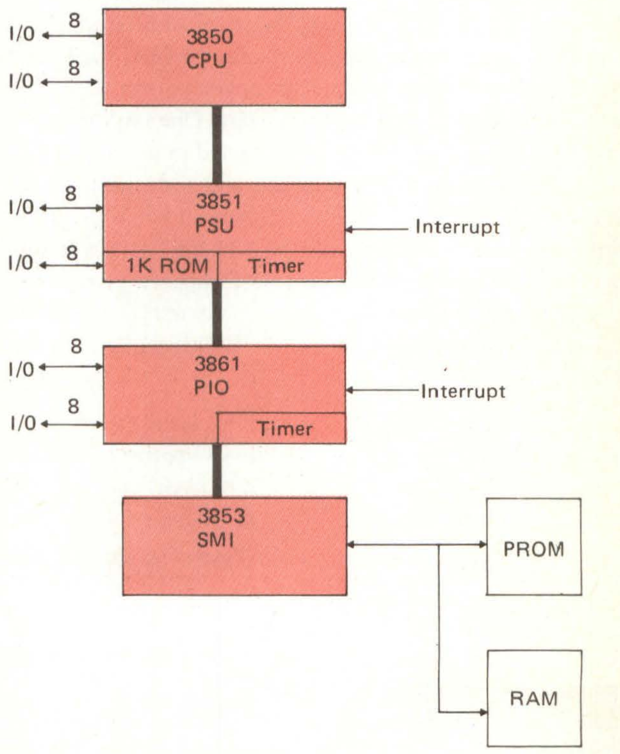

**Fig 3 Possible expanded F8 system incorporates the 3850 and 3851, plus a programmable I/O chip (3861) and a static memory interface (3853).**

One last oddity– the F8 doesn't provide an inclusive OR for scratchpad. But you can fabricate an inclusive OR using the exclusive OR and a temporary scratchpad, RO for example. The required sequence is

```
        LR      R0,A        ;R0 = A
        NS      R3          ;A = A and R3
        XS      R3          ;A = A xor R3
        XS      R0          ;A = A or R3
```

Note at this point that the F8 is a low-end microprocessor, used in simple controller designs rather than minicomputer-like systems. Therefore, you must expect it to have certain limitations. I have pointed out some of these limitations, not to highlight the weaknesses of the F8, but to simplify your programming efforts. Unfortunately, the microprocessor revolution hasn't yet produced what we programmers really want – a single-chip IBM 360.

## program organization

Program organization is vitally important in F8 systems. For example, when you must transfer control outside the range of normal branches, you arrive at a sequence like

```
        BC      GO          ; avoid jump if carry is set
        JMP     AWAY        ;jump if carry is clear
GO      .
        .
        .
```

As I've mentioned before, this sequence isn't efficient because it wastes memory. But the F8 provides an additional penalty in such cases because the JMP alters the accumulator. Subroutine organization thus becomes even more important than before.

Organizing the scratchpad is also important. Many F8 applications – gas pump controllers, for example – don't provide RAM, so all temporary values must be stored in the scratchpad. I can't state any hard-and-fast rules for scratchpad organization, but you may discover an organization that will minimize your program's size. One important factor is that the ISAR register is loaded in parts; one instruction loads the upper three bits and a second loads the lower three bits. Furthermore, a flag is set when the lower three bits are set. You can use these characteristics to implement an efficient sequence for transfering one group of eight scratchpad registers to another. Assume you want to transfer 20-28(octal) to 40-48(octal). This sequence does the job:

```
        LISL    7           ; ISAR lower = 7
LOOP    LISU    2           ; ISAR upper = 2
        LR      A,S         ; A = (ISAR)
        LISU    4           ; ISAR upper = 4
        LR      I,A         ; (ISAR) = A, and
                             increment ISAR
        BR7     LOOP        ;jump if ISAR lower not seven
```

Don't be misled by the length of this or any of my other examples; before you judge efficiency, count up the object code. This sequence requires six instructions, but it uses only seven memory bytes.

## subroutine interface

Whenever the F8 executes a subroutine call, it places the return address in resister P, the program stack. If you intend to make any additional calls, you must store this information. Even if your application requires only one subroutine level, you might have to save this register because an interrupt sequence is the same as a subroutine call; if you enable an interrupt before saving P, you could lose the return address.

One way to save a return address uses the scratchpad. If you set aside one group of eight scratchpad registers to hold return addresses, you can provide four levels of subroutine call, which should prove adequate in most cases. For cases where this procedure proves inadequate, you can save the returns in RAM or in additional scratchpad registers. The first step is to create a pair of routines, CALL and RETN; CALL stacks the return addresses in the scratchpad and RETN restores the last return (Listing 1). The stack is circular, so you can forget about overflow (although this property may form a source of program error). You must also set aside one of the lower scratchpad registers, say R1, as a stack pointer. The stack area is 70-77(octal), and during initial start, you must preset R1 by executing

```
        LI      0'70'       ;A = 70(octal)
        LR      R1,A        ; preset R1
```

After initializing R1, you can use the CALL and RETN routines. At the beginning of each subroutine, transfer the return address to K and then call CALL, which stacks the return. The required sequence is

```
        LR      K,P         ; save P (temporarily)
        ~~PI~~      CALL        ; stack return
```

To exit the subroutine, jump to RETN using a branch or jump operation.

### Listing 1. Routines For Saving Return Addresses

```
CALL    DI                  ; disable interrupts
        LR      A,R1        ;A = R1
        LR      IS,A        ; ISAR = stack pointer
        LR      A,KU        ;A = K upper
        LR      I,A         ; stack A
        LR      A,KL        ; aa = K lower
        LR      I,A         ; stack A
        LR      A,IS        ; restore R1
        LR      R1,A
        EI                  ; enable interrupts
        POP                 ; return to caller
RETN    LR      A,R1        ;A = R1
        LR      IS,A        ; ISAR = stack pointer
        LR      A,D         ; decrement ISAR
        LR      A,D         ; set K lower
        LR      KL,A
        LR      A,S         ; set K upper
        LR      KU,A
        LR      A,IS        ; A = stack pointer
        LR      R1,A
        PK                  ; exit
```

Note that the routines in Listing 1 use PK to transfer control to the original calling routine. The F8 manual describes PK as a subroutine call; I have found it most useful as a return, but it is useful as a call if you must make several sequential calls to the same routine.

## interrupts

The F8 treats interrupts just like calls to subroutines – the return address is stacked and control is transferred to the interrupt address. One characteristic of interrupts, carefully hidden in the F8 documentation, could drastically impact your software design. In particular, external interrupts and timer interrupts from the same chip cannot both be enabled at one time. I feel that this property makes it difficult – if not impossible – to use both external interrupts and timer interrupts from the same chip. But this limitation doesn't mean that you can't use both types of interrupts; it only means that one type of interrupt should be handled by one support chip and the other by a second chip.

Another important characteristic of interrupts in the F8 is their multilevel nature – one interrupt can interrupt another. The F8's documentation is replete with programming examples and is one of the more comprehensive documents produced by the microprocessor manufacturers. One thing the documentors seem to forget, however, is that an interrupt doesn't preclude a second interrupt. So at the beginning of each of your interrupt control routines, be sure to disable all other interrupts.

## passing parameters

To pass parameters in the F8, you can use the unit's first 11 registers. You can't pass parameters in the accumulator, however, because the call alters its contents. Passing parameters after a call is more difficult than in the microprocessors I've discussed so far, but it's not impossible.

The best place to perform such a post-call parameter fetch is in CALL; you can modify that routine to place the fetched parameters in the general registers (R2, R3, etc.). You must indicate how many parameters to transfer; one way is to load a register, say R0, before calling CALL. The general strategy involves transfering the return address to DC and then fetching the parameters. After saving the parameters, you save the return address. The new routine CALL appears in Listing 2.

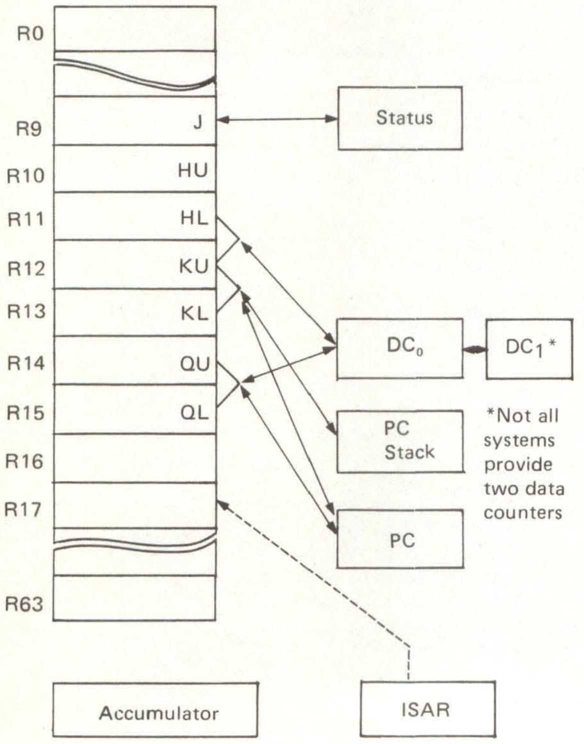

**Fig 4 In addition to its 8-bit accumulator, the F8 incorporates 64 scratchpad registers in its CPU; direct addressing accesses only the first 16 of these registers, and the rest must be accessed through an ISAR register. The system's register complement is completed by a 16-bit program counter (PC), a program counter stack register and one or two data counters.**

**Listing 2. Routine That Performs Post-Call Parameter Fetches**

```
CALL    DI                  ; disable interrupts
        LISU    0           ; set ISAR = 2
        LISL    2
        LR      A,KU        ; transfer K to H
        LR      HU,A
        LR      A,KL
        LR      HL,A
        LR      DC,H        ; DC = return
LOOP    LM                  ; A = parameter
        LR      I,A         ; stack parameter
        DS      0           ; continue to all transfered
        BNZ     LOOP
        LR      H,DC        ; set return
        LR      A,R1        ; set return stack
        LR      IS,A
        LR      A, HU       ; stack return
        LR      I,A
        LR      A,HL
        LR      I,A
        LR      A,IS
        LR      R1,A        ; save stack pointer
        EI                  ; back to caller
        POP
```

Listing 2 looks long but the routine requires only 24 bytes. One improvement in it is possible and might prove useful. Because the F8 provides only one way to load from memory, it requires several instructions to access a random memory location. If the parameters are random values in memory, it may be more convenient to transfer the address of the variable rather than its contents. Change LOOP this way (I use two data counters, but I could have saved DC in Q or K):

```
LOOP    LM                  ; set upper byte of address
        LR      HU,A
        LM                  ; set lower byte of address
        LR      HL,A
        XDC                 ; save DC
        LR      DC,H        ; set the parameter
        LM
        LR      I,A         ; stack it
        XDC                 ; restore the data counter
        DS      0           ; continue till all transferred
        BNZ     LOOP
```

You'd then code a call to a subroutine that expects the parameter addresses following the subroutine call this way:

```
PI      ROUT      : perform the call
DC      PARAM1
DC      PARAM2
 .
 .
 .
DC      PARAMn
```

## improving arithmetic computations

My first arithmetic topic this month is actually a logical manipulation. One frequent task most microprocessors must perform requires converting ASCII input characters into some other form. One common conversion changes a hexadecimal digit into its equivalent binary representation. This task is slightly complicated by the ASCII coding for the hexadecimal characters – a few unused characters exist in the middle of the set. The ASCII coding for the hex digits is

0 - 30
1 - 31
⋮
9 - 39
⋮
A - 41
⋮
F - 46

Assume that the character you must convert lies in the accumulator. The most common algorithm for converting that character to its binary equivalent (and also detecting nonhexadecimal characters) is

# Fairchild F8 Instruction Set

| **Immediate** | | **Memory** | | **Scratchpad** | | |
|---|---|---|---|---|---|---|
| AI | 24 | AM | 88 | AS | Cr | add to acc |
| – | | AMD | 89 | ASD | Dr | add to acc (decimal) |
| NI | 21 | NM | 8A | NS | Fr | and with acc |
| CI | 25 | CM | 8D | – | | compare with acc |
| XI | 23 | XM | 8C | XS | Er | exclusive OR with acc |
| LI | 20 | LM | 16 | LR | 4r | load acc |
| OI | 22 | OM | 8B | – | | OR with acc |
| – | | ST | 17 | LR | 5r | store acc |

**16-bit transfers**

| Rd \ Rs | Immediate | DC | Q | H | K | P |
|---|---|---|---|---|---|---|
| DC | 2A | – | 0F | 10 | – | – |
| Q | – | 0E | – | – | – | – |
| H | – | 11 | – | – | – | – |
| K | – | – | – | – | – | 08 |
| P | – | – | – | – | 09 | – |
| P0 | – | – | 0D | – | – | – |

**8-bit transfers**

| Rd \ Rs | A | IS | QU | Q1 | KU | K1 |
|---|---|---|---|---|---|---|
| A | – | 0A | 02 | 03 | 00 | 01 |
| IS | 0B | – | – | – | – | – |
| Qu | 06 | – | – | – | – | – |
| Q1 | 07 | – | – | – | – | – |
| Ku | 04 | – | – | – | – | – |
| K1 | 05 | – | – | – | – | – |

| | | |
|---|---|---|
| ADC | 8E | add to DC |
| BC | 82 | branch on carry |
| BF | 9t | branch if condition false |
| BM | 91 | branch if minus |
| BNC | 92 | branch if no carry |
| BNO | 98 | branch if no overflow |
| BNZ | 94 | branch if not zero |
| BP | 81 | branch if plus |
| BR | 90 | branch |
| BR7 | 8F | branch if IS ≠ 7 |
| BT | 8t | branch if condition true |
| BZ | 84 | branch if zero |
| CLR | 70 | clear acc |
| COM | 18 | complement acc (1's) |
| DS | 3r | decrement scratch |
| DI | 1A | disable interrupts |
| EI | 1B | enable interrupts |
| IN | 26 | input to acc |
| INC | 1F | increment acc |
| INS | Ai | input to acc – short |
| JMP | 29 | jump extended |
| LIS | 7i | load acc with i |
| LISL | Di | load IS lower |
| LISU | 6i | load IS upper |
| LNK | 19 | add carry to accumulator |
| LR J, W | 1E | transfer W to J |
| LR W, J | 1D | transfer J to W |
| NOP | 2B | no operation |
| OUT | 27 | output acc |
| OUTS | Bi | output acc – short |
| PI | 28 | call subroutine – immed |
| PK | 0C | call subroutine K |
| POP | 1C | subroutine return |
| SL | 13/15 | shift left acc 1 or 4 bits |
| SR | 12/14 | shift right acc 1 or 4 bits |
| XDC | 2C | exchange DC |

**Fig 5 Clip and save this summary of the F8's instruction set; similar summaries for the Intel 8080, Motorola 6800 and Texas Instruments 9900 appeared in previous articles. The symbol "r" denotes a scratchpad register or one of three possible scratchpad indirect addressing modes.**

```
         AI     -H'30'    ; subtract 30 hex
         BM     NOHEX     ;jump if not a hex digit
         CI     9         ; check for 0-9
         BP     HEX       ;jump if 0-9
         AI     -7        ; adjust for A-F
         CI     9         ; reject if <10
         BP     NOHEX
         CI     16        ; reject if >16
         BM     NOHEX
HEX      .
         .
         .
```

This sequence transfers control to HEX if its input is hexadecimal (the converted value lies in the accumulator) and to NOHEX if the input isn't hexadecimal. It's similar to the one I used as an example in my discussion of the Intel 8080. But there's a more efficient way of performing this same function. Instead of approaching the problem as an arithmetic one, try re-examining it as a simple bit manipulation. Check for a number in the range 30-39 (and convert it) with one exclusive OR (exclusive OR the input with 30). That takes care of the 0 to 9 cases. Now what about A-F? The exclusive OR with 30 changes the coding sequence for the other characters so that A-F become 71-76. Check for this result by using an exclusive OR with 70 and a compare. Then rewrite the conversion routine this way:

```
         XI     30H       ; check for 0-9
         CI     9
         BP     HEX
         XI     H'70'     ; check for A-F
         BZ     NOHEX
         CI     6
         BM     NOHEX
         AI     9         ; adjust for A-F
HEX      .
         .
         .
```

This little exercise shows that the simple and obvious solution to a problem isn't always the best one.

Another mathematical problem you'll often encounter focuses on random number generation. Many computer applications, including those for microprocessors, require generation of random number sequences (or as the mathematically pure are quick to point out, pseudo-random number sequences). At first this problem appears simple. How many times have you inadvertantly created a random number generator? Mine was originally intended to multiply two numbers. When you set out to program a random number generator, understanding the mathematical properties of that generator is an important requirement. What is its period? (That is, when will it begin to repeat or generate numbers already generated?) One of the most common generators is described by this formula:

C(i+1) = C(i)*X + B [mod P]

A given random number results from multiplying the previous number by a constant and adding an offset. The product is then truncated via the mod operation; fixed-word-length computers make that operation easy to implement. If X and B are chosen according to the following rules, you'll obtain a random number generator with a period of 2**Q, where Q is the word length of the computer:

X = 2**S + 1
B = odd number

One choice for X is 2**4+1 = 17; the obvious choice for B is 1. To implement the random number generator, first create a multiply routine so you can multiply by 17. I discussed the creation of multiply operations from simple shift operations in a previous article, but the F8 is ill suited to those algorithms because of its very limited shift repertoire. But the choice of 17 wasn't accidental; that number is 16+1, so you need only create a multiply-by-16 to perform the required operation. The shift-by-four operation suits this task; the following sequence multiplies the H resister by 16 and places the result in (R2,R3):

```
         LR     A,HU      ; isolate upper four bits of product
         SL4
         LR     R2,A
         LR     A,HL      ; set lower 4 of upper 8
         SR4
         XS     R2        ; combine with upper 4
         LR     R2,A
         LR     A,HL      ; set lower 8 bits
         SL4
         LR     R3,A
```

Because you really want to calculate H*17+1, you can change the last instruction of this sequence to

```
         INC              ; add in one
         AS     HL        ; add old H
         LR     HL,A      ; save lower 8
         LR     A,HU      ; set old H (upper)
         LNK              ; add in carry from lower 8
         AS     R2        ; add from old product
         LR     HU,A
```

The result remains in H; the sequence ignores any carry from the multiply or add and thereby incorporates the necessary mod operation.

These two routines form the required 16-bit random number generator. Note that the F8 doesn't provide an add with carry operation, so the carry must be added to the accumulator using the LNK instruction. These routines certainly aren't the ultimate in random number creation; many technical articles that describe algorithms for generating numbers have appeared. Why so many? Because the generators are pseudo-random, they all exhibit certain statistical properties, some of which may not be desirable in an application program. Work continues on defining generators that meet certain requirements; one other generator I have used is

C(i+1) = C(i)*X [mod P]
where X = R*2**S±1 and S>2, R odd

*Next month, Dollhoff will continue his exploration of microprocessor software optimization and will focus on the Zilog Z-80.*

◆

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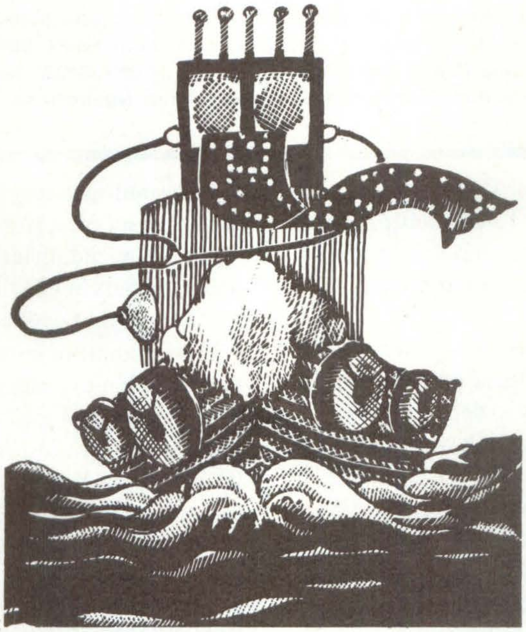
# MICRO-BRAIN ON THE BOUNDING MAIN

**How designers configured a microprocessor based data-acquisition and diagnostic system that detects engine malfunctions and oversees preventive maintenance aboard seagoing tugboats**

by **Steve Tsolis** and **Tony Mathews**



Until recently, the marine industry had no analytical method of monitoring the performance of the eight-to-twenty-cylinder diesel engines that power modern vessels, and ship operators couldn't detect many minor malfunctions in those power plants until the malfunctions caused major breakdowns. And because the plants develop up to 4000 hp, those breakdowns often caused near-catastrophic failures.

We grew aware of these problems when a tugboat operator asked us to determine the cause of several massive crankshaft failures. As part of our investigation, we developed the Seaborne Integrated Diagnostic System (SIDS), a microprocessor controlled data-acquisition and diagnostic system that is now installed on several ocean- and river-going craft.

Using SIDS, a tugboat's crew knows that a failure is approaching in time to do something about it before much damage occurs. The system prints out regular engineering reports and also generates preventive-maintenance alerts 100 hrs or so before work is required. These alerts allow the crew to perform minor repairs during layovers and permit more efficient scheduling of major overhauls.

### designing for computer novices

SIDS' major design constraints included size limitations, a hostile environment and operating personnel totally unversed in either electronics or computer operation. Primarily engines and fuel tanks surrounded by small hulls, tugboats are cramped. With this space premium in mind, we designed SIDS to fit in a 17"W x 10"H x 23"D cabinet. On one ship, we had to install the unit in the most readily available space – the ship's head.

In the monitor's severe operating environment, sensors fixed to the engines experience high temperatures as well as large-amplitude, low-frequency vibration. In addition, crews wash down the engines frequently with a caustic solution. Because some craft are under way for long periods of time, performing service en route is a difficult if not impossible task. Because ships' personnel aren't qualified to adjust or maintain $\mu$P-based equipment, we made SIDS completely automatic. If it fails, it fails gracefully and generates no false warnings. Achieving this capability would normally dictate using an expensive minicomputer system, but cost and size factors precluded this option.

Instead, we chose to use the National Semiconductor 16-bit IMP-16 microprocessor (Fig 1), which in our design accepts a 128-input section of 16 8-channel-type multiplexers that input a 12-bit integrating A/D converter. The microprocessor accesses 8K 16-bit words of PROM and 512 16-bit words of RAM. Because workboat power almost always fluctuates from the levels a computer requires to maintain volatile memory, we configured the system's RAM-stored operating programs and its real-time clock to utilize battery power. That way, the system can save time-related events like preventive maintenance schedules while the ship's engines are shut down. The microprocessor's output section consists of a parallel-to-serial converter and a printer driver; two of the IMP-16's user flags provide aural warning and enable the printer.

SIDS requires a 12-bit data precision to achieve 4-decimal-digit accuracy. We also require the monitor to scan, correct

**Steve Tsolis** *and* **Tony Mathews** *are president and vice president, respectively, of Advanced Electronic Devices, an Old Saybrook, CT, firm that specializes in microprocessor-system consulting and design.*

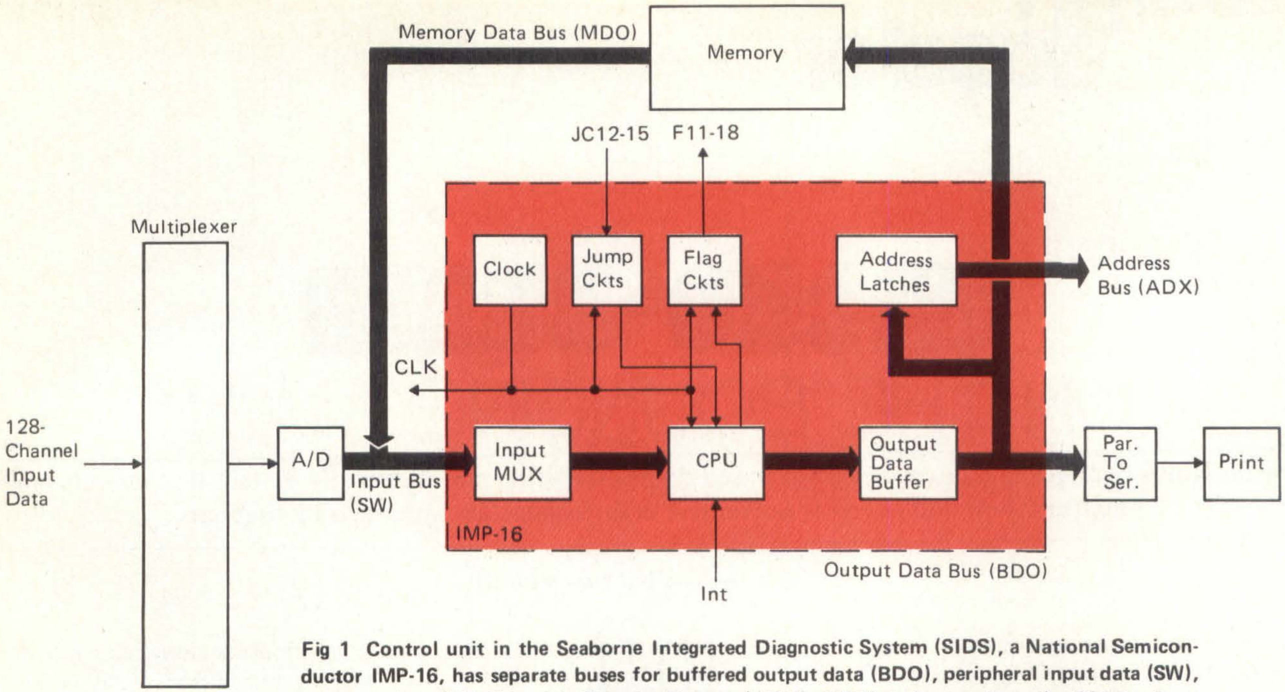


**Fig 1 Control unit in the Seaborne Integrated Diagnostic System (SIDS), a National Semiconductor IMP-16, has separate buses for buffered output data (BDO), peripheral input data (SW), memory data (MDO) and buffered addresses (ADX). SIDS' designers chose the 16-bit microprocessor to meet arithmetic and bit-manipulation requirements.**

and process one data point every 10 ms. The processing operation involves performing two or three 12-bit multiplications (or divisions) while sifting through a multi-level fault tree, so execution time formed the key factor in our selection of a 16-bit microprocessor.

But additional factors also influenced our choice. Sixteen-bit machines require fewer total bits of memory than 8-bit machines, and programs are easier to debug in 16-bit machines. We also liked the convenience of having a little more than sufficient arithmetic accuracy in one computer word; 8-bit processors require double-precision arithmetic to handle data from a 12-bit A/D converter.

After considering all these factors, we determined that while the IMP-16 could sift through the fault tree in less than 5 ms and 8-bit devices required about 8 ms, the combination of arithmetic functions and tree sifting placed 8-bit processors beyond our 10-ms target. Thus, we had to choose a 16-bit device.

Our choice narrowed to a decision between the five-chip IMP-16 and the single-chip Pace – also from National Semiconductor – the only 16-bit devices available in production quantities at the time of our design. The IMP-16 has separate 16-bit buses for buffered output data (BDO), peripheral input data (SW), memory data (MDO) and buffered addresses (ADX). Pace uses a single I/O bus architecture. In the IMP-16, memory locations and peripheral devices can have the same addresses.

The IMP-16 also has 16 user-available flags, one general interrupt condition, one vector interrupt, and four user jump conditions – features important in reducing component count in an interrupt-driven system. Both IMP-16 and Pace use the same basic set of instructions, but the IMP-16 has additional CROM (control read-only memory) that provides 17 instructions, including single-word arithmetic commands (multiply, divide, double precision add and subtract) as well as set bit, clear bit and test bit instructions. The IMP-16 multiply and divide commands produce 32-bit products and dividends in less than 200 $\mu$s – a factor that simplifies software in that device.

The amount of data that SIDS must process makes bit manipulation expedient; the monitor generates many status tables in which it must modify single bits to indicate status changes. Single-word IMP-16 commands set and clear any bit in an accumulator, while the SKBIT instruction increments the microprocessor's program counter if the specified bit is a logical "one". These bit-manipulation capabilities also led us to choose the IMP-16.

### maximizing software use

A typical seagoing tugboat has a 4-engine plant consisting of two turbocharged diesel main engines and two diesel-driven alternators. In a SIDS-equipped ship, sensors measure the temperature of the induction air, the engine coolant and the lubrication system for each engine, as well as exhaust gas temperatures at each cylinder. Other sensors measure pressures in intake manifolds, lubrication systems and fuel lines. RPM tach generators and voltage sensors monitor engine speed and alternator output; cables from all sensors to the controller are generally long because of confined engine-room space.

The 100 mV signals from the sensors go to 8-input multiplexers, each equipped with a single amplifier on its output for isolation (Fig 2). Each channel is clocked at a 10-ms rate, and multiplexer output, through switches, feeds the single 12-bit A/D converter. Twelve-bit parallel data from the converter goes to the IMP-16 SW data bus. One of the IMP-16's user flags (F-12) controls start of conversion; end of conversion is signalled by an extra data bit inserted on the SW bus.

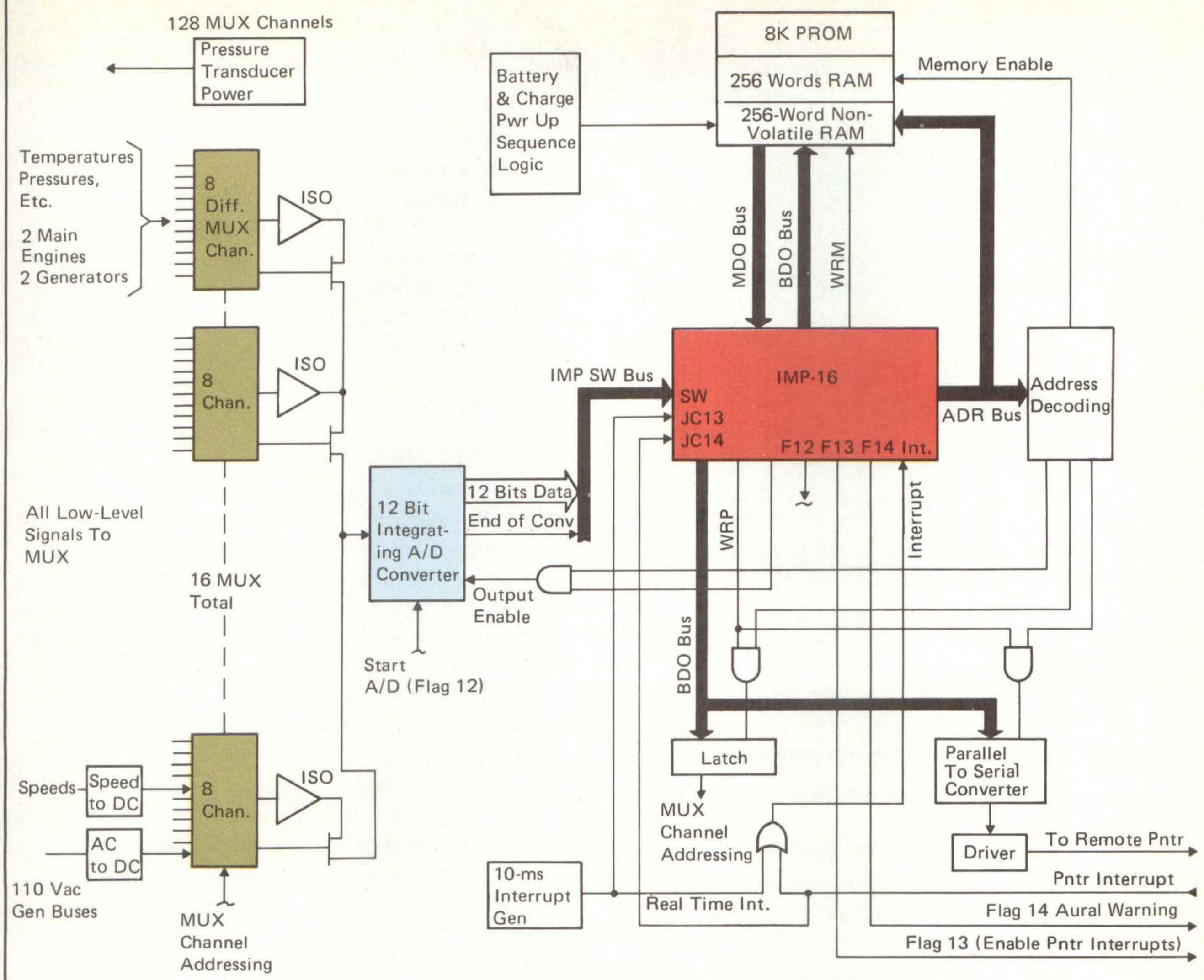


**Fig 2 Temperature, pressure, engine-rotation and alternator-output data input SIDS through 16 8-input multiplexers, whose isolated outputs go to a 12-bit A/D converter and from there to the IMP-16's SW data bus. The microprocessor selects an input channel with a 16-bit word, decoded by latch circuits; it signals start of conversion with Flag 12 and end of conversion through Bit 13 on the SW data bus. Each conversion requires about 8 ms; a 10-ms real-time interrupt forces the system through Jump 13 and the interrupt pin.**

Decoded address lines select the proper channel addresses.

We feel that system software should handle most tasks normally assigned to hardware. This arrangement reduces system complexity, lowers hardware cost and channels a large part of design cost into a one-time, non-recurring software-development effort. It also leads to some interesting instrumentation concepts. For example, the monitor accepts thermocouple signals directly; no secondary-reference junction exists, because reference signals come from PROM-resident tables keyed to nominal thermocouple output. Similarly, signal conditioning or gain setting schemes don't serve individual pressure sensors; signals are standardized through software. The IMP-16 provides all signal conditioning; it inserts scaling, gain and offsets prior to converting data to engineering units for calculation.

The software's processing of data input from the sensors involves multiplying by a conversion factor and adding a constant. Data stays temporarily in RAM for later required references.

## diagnosing the diagnostics

During the monitor's software design phase, we realized that we needed more than seven bits to control the processing of input data, even though the system achieves multiplexer addressing with only seven bits. We gained this added capability without relying on look-up tables, which require large amounts of memory.

The monitor must establish whether incoming data should be tested for high limits, low limits or both; whether the data measures temperature, pressure, rotation or voltage; and whether a given failure requires crew warning. We achieved the required parameter selection for this process by using the nine additional available bits in each IMP-16 word (Fig 3).

The monitor can use sensor data in several ways to deduce a malfunction. But complex diagnostics are difficult to achieve without extensive fine tuning of the software for each engine – a process that produces long routines. Suppose, for example, that the exhaust gas temperature of one cylinder is constantly 20° lower than the temperature of all other cyl-

| IMP-16 Bit | MUX Address | Bit Assignment |
|---|---|---|
| 15 | Bit 6 (Most Sig.) | 0 = port, 1 = starboard |
| 14 | | 0 = data from engine, 1 = data from generator |
| 13 | | 1 = "left bank" required in error message |
| 12 | | 1 = "right bank" required in error message |
| 11 | | 1 = "stop engine" required |
| 10 | | 1 = failed upper limit<br>0 = failed lower limit |
| 9 | | 1 = "stop generator" required |
| 8 | Bit 5 | 0 = temperature, 1 = pressure |
| 7 | Bit 4 | part of address |
| 6 | Bit 3 | part of address |
| 5 | Bit 2 | part of address |
| 4 | Bit 1 | part of address |
| 3 | Bit 0 | part of address |
| 2 | | 1 = don't output this MUX address |
| 1 | | 1 = perform upper limit test |
| 0 | | 1 = perform lower limit test |

**Fig 3 SIDS achieves multiplexer addressing with seven bits; it uses the remaining nine bits of a multiplexer address word to control the processing of input data. The monitor's software outputs each 16-bit MUX address from a table of addresses through which it cycles.**

inders, and that no crankcase-pressure pulsations exist at a frequency equal to the number of rpm. Suppose too that the pressure in the intake manifold opposite the low exhaust gas temperature is constantly lower than the pressure in the other intake manifold. Most probably the clearance of one of the valves for the cylinder with low exhaust gas temperature is wrong. But for another engine of the same type, 10° or 30° could indicate the same condition.

To minimize the size of the diagnostic routines that allow for such variations, we configured SIDS' software so that input data is converted to proper units and then tested sequentially with other data (Fig 4). Such diagnostics give SIDS great power but don't occupy much memory; we had to write only 1000 lines of code for the executive program, the diagnostic routines and the tables.

To accommodate different customer requirements, we partitioned memory and wrote the program with a separate executive that we could commit to ROM after our final design review. We assigned constants subject to change, tables, data unique to specific engines, and tables and subroutines for optional equipment to other specific memory areas. Following checkout, we implemented these parameters in separate PROMs for production.

## prototype development

We developed software and prototype hardware on National's IMP-16P prototyping system, equipped with the IMP-16 CPU card, 8K x 16 words of memory, and interfaces for a Teletype, a high-speed tape drive, a card reader, a high-speed printer and a PROM programming card. The system's memory size allows about 800 labels in the development program.

During prototype development, we used a Documation card reader for source program input; a Texas Instruments Silent 700 for keyboard access, cassette read and write and hardcopy output; and a Centronics printer for assemblies. We modified the firmware in National's Teletype interface card to increase the Silent 700's speed from 10 cps to 30 cps. And we wrote a program that allowed the Silent 700 to store and access support programs on magnetic tape cassettes at 1200 baud.

To speed software development, we used the IMP-16 resident assembler, editor, compiler and Debug programs. Because we owned a card reader, source editing did not pose

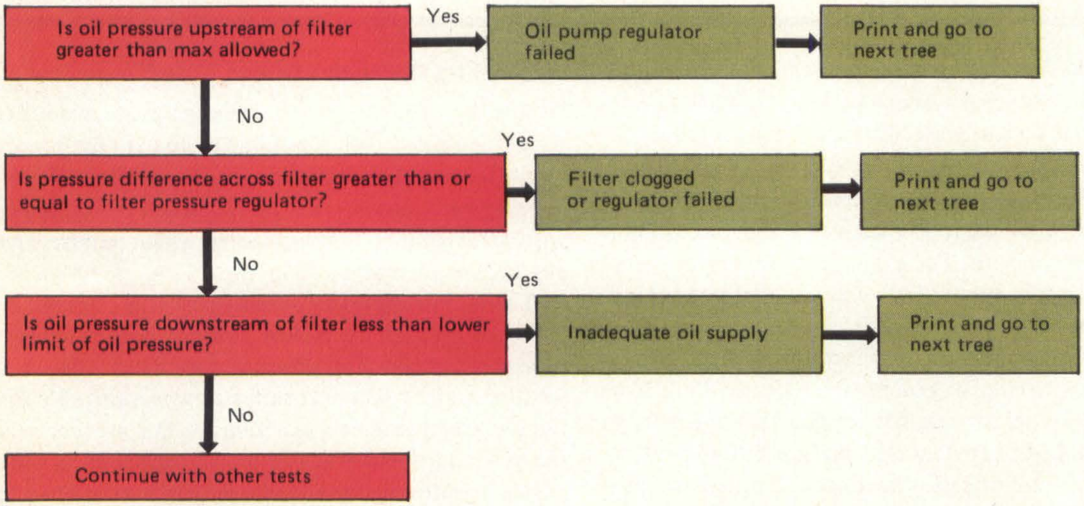


**Fig 4 Sample fault tree illustrates how SIDS sequentially compares input data with PROM-resident limits. The monitor's executive program, diagnostic routines and tables are implemented in about 1000 lines of code.**

the edit/loading problem it could have if we had used paper tape. We "terminal-built" many of the short programs – especially subroutines – on the Silent 700 using a "conversational assembler," to further reduce coding time. And we established systematic breakpoints to allow TTY printout of selected CPU and memory contents during debugging. A limited version of the Debug program served shipboard SIDS verification and checkout.

In its initial version – designed to determine the cause of crankshaft failure in one class of tugboats – SIDS was housed in the IMP-16 prototyper chassis. The assembly included the analog input section, sensor power supply, A/D converter, microprocessor CPU, memory, output interface and operator control panel. (The control panel in the prototyper is a completely independent peripheral; when installed, it allows complete access to CPU and memory, but when removed it does not affect system operation.)

Using this prototype SIDS, we ascertained that the shaft failure resulted from low (20 psi) oil pressure caused when the engine speed dropped significantly below idle as the propeller shaft was shifted into reverse. Since then, we have expanded SIDS to provide unattended shipboard diagnostics. To properly respond to these diagnostics, an engine must turn at constant speed for more than 15 min; otherwise, analysis is restricted to simple limit testing. Generators too must operate for at least 15 min before a detailed analysis.

When SIDS finds a failure, it prints a message in clear language to alert the crew to both the problem and to the required corrective action. It also prints advisory messages. For example, a worn injector produces a rich fuel/air mixture and generates lower-than-ordinary cylinder-head temperatures. While the condition doesn't cause damage immediately, the crew can replace the injector while under way to improve fuel consumption. The advisory message would read

```
PORT GENERATOR
EGT CYLINDER 16
LOW TEMPERATURE
960°F
```

SIDS also tracks PROM-resident preventive maintenance schedules with its real-time clock and prints those schedules to alert the skipper of impending yard time.

While the shipboard printer advises a crew of power-plant performance malfunctions and preventive-maintenance requirements, another function – trending – helps the ship's owners further increase the vessel's efficiency. Weekly, the crew tabulates readings from the printer and from fixed power-plant instruments and mails those tabulations to our headquarters, where they are coded and input to a computer program. The program compares the readings with historical data on the ship's equipment and analyzes trends that could lead to reduced engine performance, potential malfunctions not covered by the on-board system and conditions requiring correction during the ship's next overhaul period. ◆

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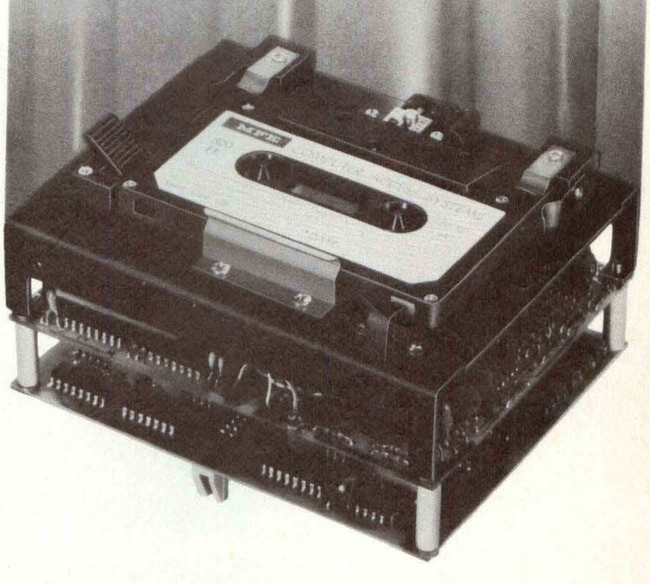

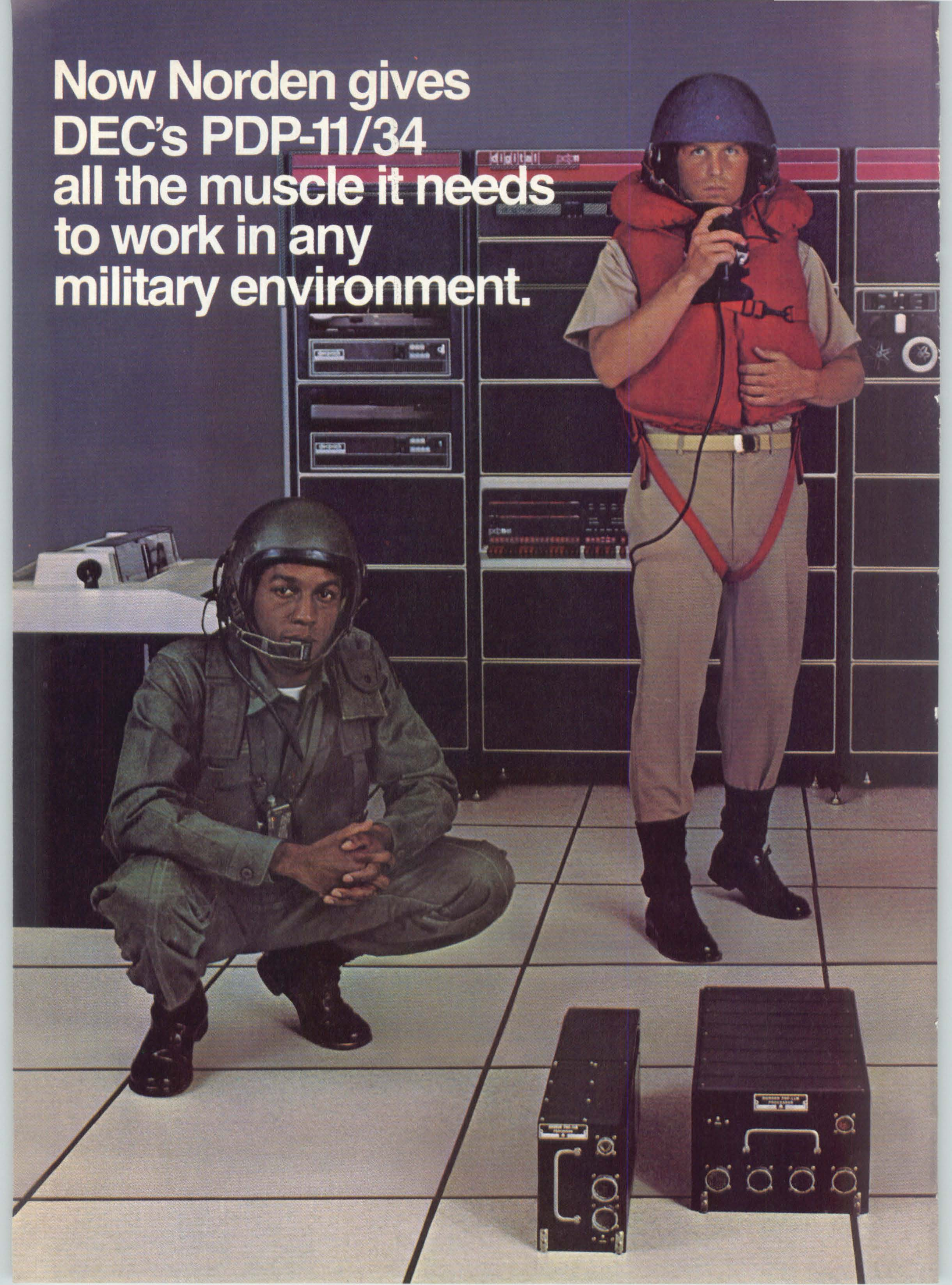

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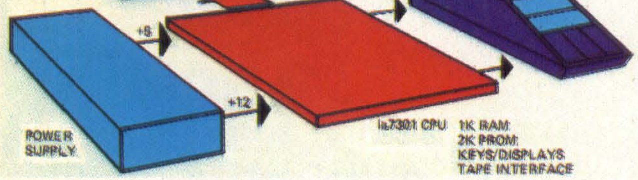

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The microcomputer system features a 24 pad keyboard, 8 seven segment LED readouts that display information in hexadecimal code which is far more versatile and advanced than binary or octal coded systems, and an onboard cassette tape interface for saving programs. The hexadecimal keyboard also contains 6 special mode keys which allow you to call up and change any data or instructions in the CPU registers or in the system's RAM memory. Likewise programs can be executed instantly or they can be stepped through one instruction at a time using the appropriate mode key, so that you learn your way around the inner working of an entire microcomputer system.

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Thus what served as an educational system can now be upgraded for many new applications. We've included a machine language coding pad for writing and documenting programs, working out subroutines and pro-

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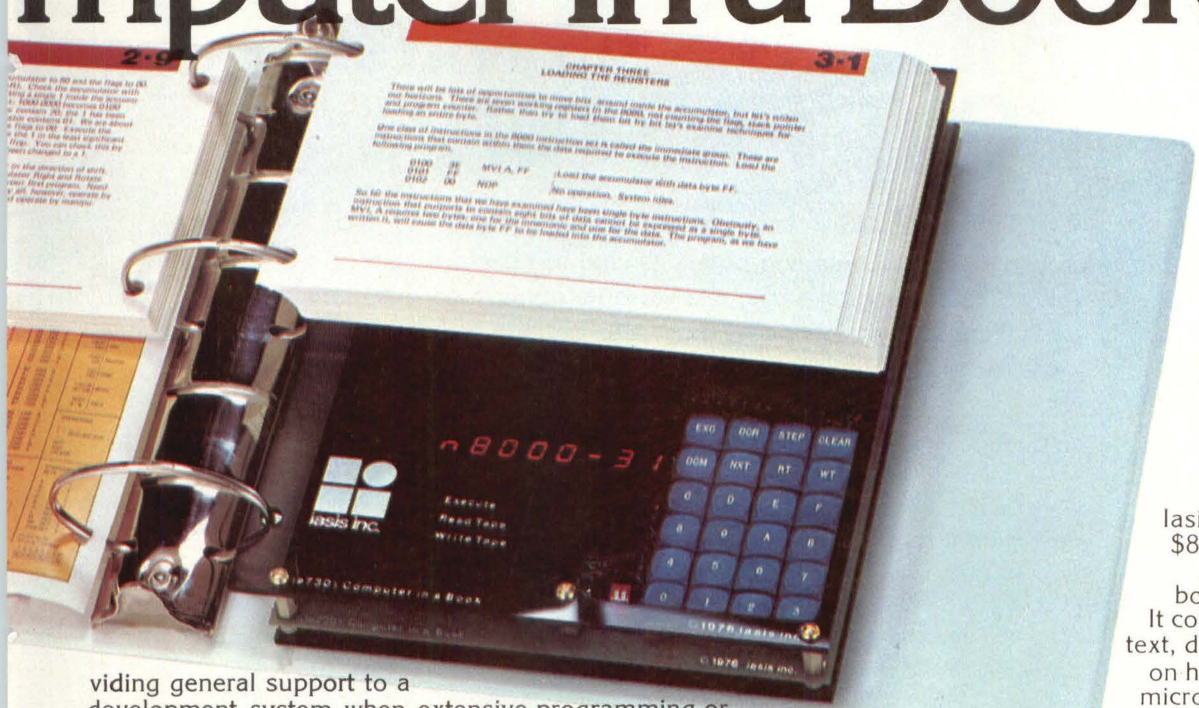

viding general support to a development system when extensive programming or debugging is necessary. The Computer in a Book may also be used to train field service technicians by putting verbal information and programs on cassette tapes. We are coming out with preprogrammed PROMs and extension tapes containing new application packages such as floating point arithmetic and micro-assembler programs. Our goal is simple. We want to provide microcomputers that are useful and practical.

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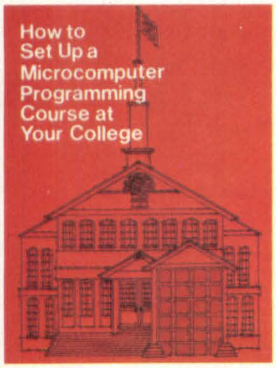
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# MICROPRO

# MAKING YOUR MINI MOVE FASTER

by **John Trudeau**

**User-microprogrammable minicomputers can exhibit performance, structural and cost advantages over less versatile minis in certain applications. How can you pinpoint those applications, and how difficult is their implementation in microcode?**

Microprogramming's "mystique" enhances its image of being very difficult to understand, and as a result many potential users unnecessarily shy away from it. But a microprogramming language, when properly implemented, is no more difficult to use than an assembly language, and in some respects it's even easier to use. The key to its successful use lies in your accurate evaluation of a minicomputer's microprogrammability and in your efficient use of that important capability.

Most users first consider microprogramming when they need greater performance from a mini already in use. Microprogramming a "bottleneck" in an existing application can produce as much as an order of magnitude performance boost without a change in processors. A user who *plans* microprogramming into a new application can expect the same performance increase and even better economic benefits, especially if he identifies the performance-limiting aspects of the application early. Whether used in upgrading an older application or planning a new one, microprogramming offers a good alternative to the purchase of a more expensive processor.

Microprogramming can serve such aspects of minicomputer operation as processing and calculation, I/0 and processor control. In addition, microprogramming lets you "customize" your mini by adding special instructions to its instruction-set repertoire. Typical microprogrammed processing/calculation applications include transcendental and trigonometric functions, floating-point arithmetic and fast Fourier transforms. Ten-to-one speed improvements of microcode over machine language are not unusual in such applications. Microcode can also improve I/0 processing; an I/0 device's interrupt processor requires much less of its mini's processing time when implemented in firmware than in software. And as I/0 processing time decreases, the time available for applications processing increases. You can also often control many CPU functions from microcode, including special bootup initialization and operation-panel control functions, some of which might be impossible to implement in software. Typical "customization" applications include adding an additional stack, adding byte- or bit-oriented instructions, and adding special indexing schemes or matrix operations. User-customized instructions simplify higher-level software and allow the minicomputer to execute that software faster.

**John Trudeau** *is a sales development engineer at Hewlett-Packard's Data Systems Div., Cupertino, CA.*

## what microprogramming does

To properly evaluate a specific minicomputer's "microprogrammability" and ease of use, you must first understand the mini's CPU structure.

The "control system" of a minicomputer (Fig 1) is what implements the basic machine-language instructions that constitute the minicomputer's instruction set. This control system is the hardwired logic designed into the machine – a combination of random logic, complicated clocking and specialized data paths. The activity of the machine is determined by (among other things) the impact of an instruction's bit pattern on the gates, latches, gizmos and gadgets built into this control system.

In a microprogrammed minicomputer (Fig 2) the control system is replaced by a primitive machine (in the true technical sense), programmed to emulate the desired machine. Built into this control processor is an instruction set that executes only primitive operations – gate register R2 to bus, gate bus to register R1, and add, for example. The minicomputer's activity now depends on the execution of "microprograms" by the control processor; a "traditional" machine instruction in main memory merely specifies which microprogram is executed and perhaps defines some parameters like operand address for the microprogram. In this scheme, machine instructions are not executed by a control system but rather are *emulated* by the control processor under microprogram control. The processing of one machine instruction results from the execution of several microinstructions – a microprogram (Fig 3).

# GRAMMING

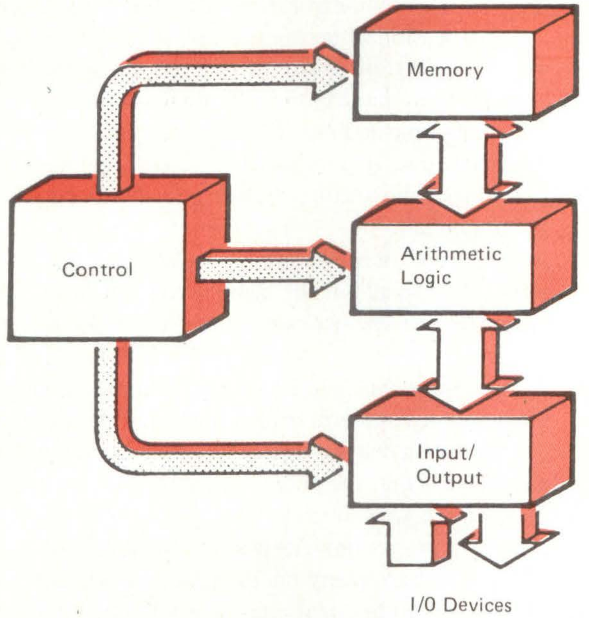


**Fig 1 Conventional minicomputer control system consists of hardwired logic. Each instruction's bit pattern affects the operation of this logic, which in turn governs the minicomputer's operation.**

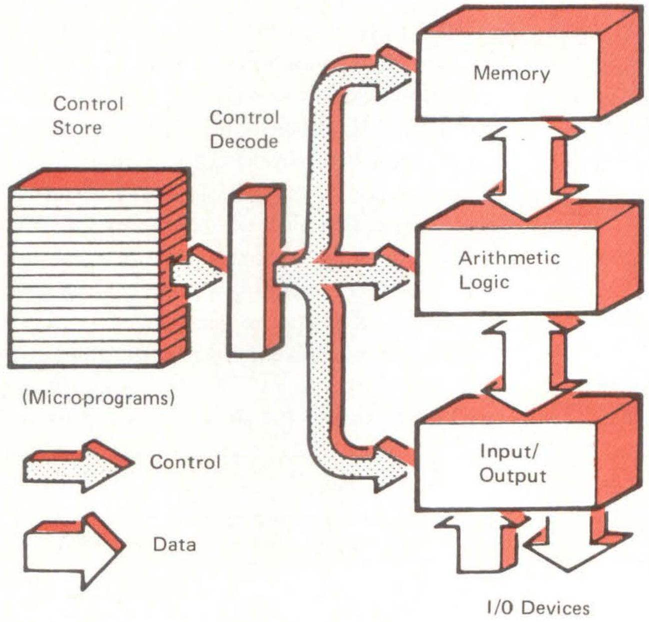


**Fig 2 Microprogrammed minicomputer control system substitutes a primitive machine (control processor) for the conventional mini's hardwired control system. The control processor executes primitive operations (microinstructions) represented by a microprogram and thereby emulates one of the minicomputer's machine instructions; a machine instruction in main memory only specifies which microprogram is executed and may also define parameters.**

Computer designers can see the advantages of this approach: Design a primitive processor, program it, and lo, you have a computer with a very flexible instruction set and enormous "growth power." Too bad it's never really that easy . . .

Computer users couldn't care less *how* instructions are executed as long as the computer does what it's supposed to do, in a timely fashion (that means *fast*). But you may have realized an important point by now – if the computer must execute instructions at a reasonable speed, the primitive control processor must operate at a significantly higher speed. A *user*-microprogrammable mini lets you focus that control-processor power directly on critical parts of your application. There it can alleviate process or I/O bottlenecks or can implement "customized" instructions in your mini's instruction set.

The word size of the control processor may be quite different from that of the emulated machine. Some microprogrammed 16-bit minis have 18-bit, 24-bit, and even 56-bit control processors. Each microinstruction for such machines usually consists of a number of "fields." A microinstruction word organized into groups of small numbers of bits, each of these fields corresponds to a particular control-processor function, and the microinstruction bit pattern in the field describes a particular operation (Fig 4).

The operation described in each field is a "micro-order;" one microinstruction consists of a number of micro-orders that are processed during one "microcycle" of the control processor. Some control processors are "horizontally" programmed – the instructions contain 30 or more fields, each specifying some register, ALU or bus operation that must occur during the instruction's microcycle. Other control processors are "vertically" programmed – microinstructions have few fields, and several instructions may be required to perform a given operation.

The control processor gets its instructions and data from "control store," a special memory often but

*Cont'd p. 48*

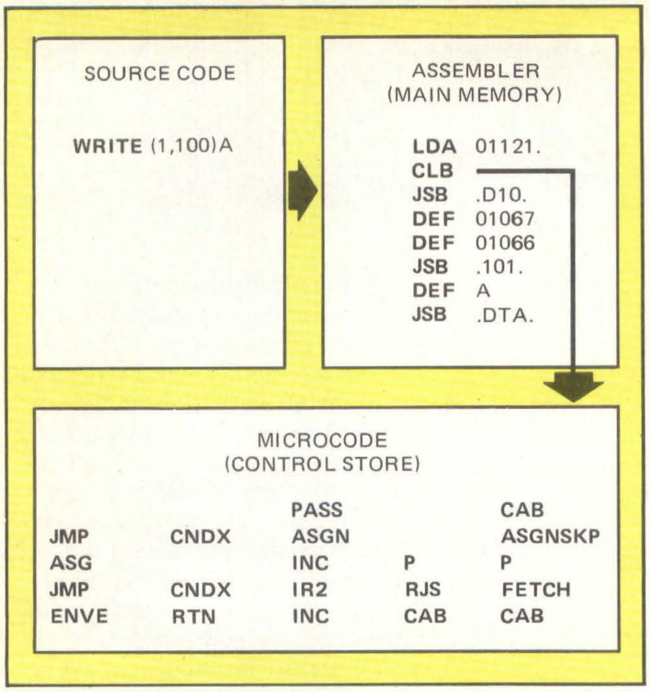


**Fig 3 Heirarchy of instructions in a microprogrammed minicomputer illustrates how one line of source code assembles into eight machine instructions stored in the mini's main memory. One of those machine instructions —CLB— is emulated by a series of microinstructions stored in the mini's control processor.**

not always implemented in ROM. This association with permanent memory gives microprograms their characteristic association with "hardware." A program by any other name, however, is still "software," so we compromise by terming microprograms "firmware." In some instances, control store may be dynamically loaded from software, in which case it's termed "writeable control store" (WCS) or "programmable" or "dynamic" control store.

Writing efficient microcode requires that a programmer be familiar to some extent with the bus structure and logic of the machine. What is not commonly known, however, is that this required extent depends greatly on the architecture and approach taken by the mini's designer and on the level of support offered by the mini's vendor. How can you evaluate the advantages of a mini's microprogramming in a particular application?

## how to evaluate microprogrammability

If a minicomputer is microprogrammed, it is by definition microprogrammable. You may have to be the designer's brother- or sister-in-law, however, to get the information, parts and tools to microprogram it. So a key evaluation parameter for a microprogrammable mini is "*user* microprogrammability." Can you easily obtain the necessary tools, parts and information? Such aids include

★ A properly documented "microassembler" that runs on the target machine and converts micro-order mnemonics and instructions into control processor instructions.

★ Software and hardware that can transfer the microassembler output into control store, including support for WCS and for creation of tapes for ROM and PROM programming.

★ A microprogram source editing and debug facility. A software package that can simulate the control processor can cut debug time and save ROM programming effort.

★ Detailed documentation of the control processor and computer logic, and adequate training in all aspects of microprogramming.

Such tools, however, serve no purpose if they are incomprehensible to all but the highly experienced engineer, are expensive or have inconsistencies ("gotchas," in colloquial terms).

A predominantly horizontally microprogrammed machine can generally offer high speed and flexibility by accommodating many micro-orders per instruction. Its disadvantage is that the micro-orders may be too limited and may require a thorough knowledge of the computer circuitry for proper implementation. In addition, the user must often learn many micro-orders and adroitly juggle them to get all the right ones into a desired instruction.

A vertically microprogrammed machine can offer an easy-to-use and easy-to-learn programming scheme; its disadvantage is slower processing as more microcycles (microinstructions) are required to perform a given task. Both approaches offer about the same efficiency in the use of control store; that is, the microprograms for a given task occupy about the same number of control-store bits in both cases. A slightly more sophisticated control processor, in combination with powerful micro-orders and vertical programming, gives you the best of both worlds – easy-to-comprehend, flexible microinstructions with enough power so that most operations require only a few instructions.

So a second evaluation parameter for a microprogrammable mini relates to the microcode structure – Is that structure simple and easy to use, yet powerful enough to do what you want it to do? You can apply this same criterion to all the hardware and software tools provided by the

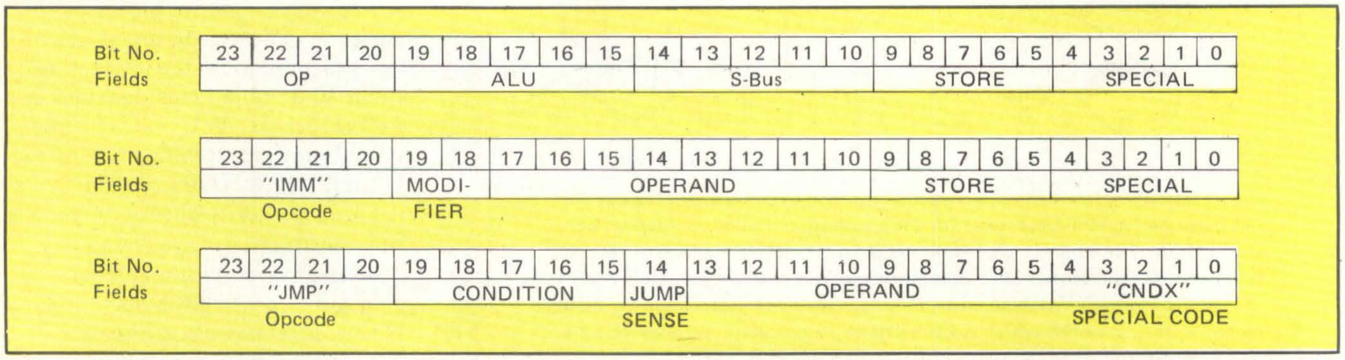


**Fig 4 Sample microinstructions for a microprogrammed minicomputer contain bit-groupings, or fields, that correspond to particular control-processor functions. Microinstructions for horizontally programmed machines can consist of 30 or more fields; vertically programmed machines use microinstructions with fewer fields, and several of these less complex instructions may execute a given operation.**

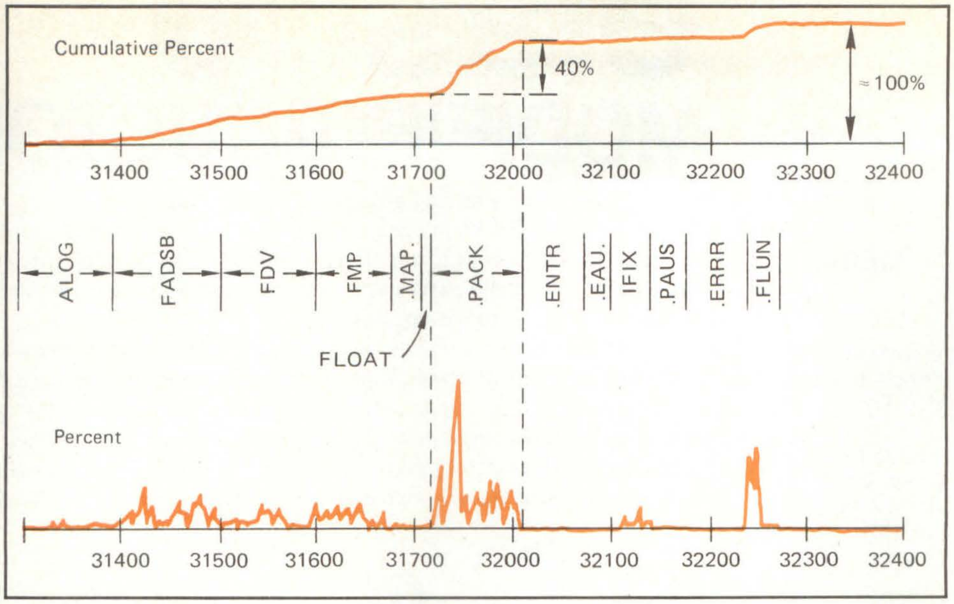


**Fig 5 Activity profile shows how much processor time is required by each of a minicomputer's programs and subroutines and allows a programmer to identify the part of code that would benefit most by conversion to firmware. In this example, subroutine .PACK, stored near memory address 31740 (octal), experiences about 40% processor utilization; implementing it in microcode could improve the mini's performance.**

mini's manufacturer.

More difficult to evaluate, as always, are the "gotchas" in the microcode scheme. Typical of these inconsistencies are:

★ Your use of some part of control store precludes your using some of the manufacturer's firmware; thus you lose some advertised capability of the machine.

★ Some important CPU functions are not microprogrammed or else are not accessible to firmware.

★ Timing or execution speed can depend on the implementation (ROM, PROM, RAM) of your firmware.

All microprogrammable minicomputers have an upper limit on the amount of available control store – it ranges from about 256 words to as many as 16K words, depending on the manufacturer. A manufacturer's implementation of a machine's base instruction set and other options requires some control-store area, so evaluate any possible conflict this usage has with your intended use of control store.

Finally, your microprograms that are speed-dependent (timing loops, or external synchronizations) may not be "transportable" from ROM to RAM (WCS) or PROM if these forms of control store do not operate at the same speed, a factor that may be very important to you during debugging and/or program updating.

## how to microprogram

So you can see how easy it is to write and use microcode, and how to determine when it's appropriate, I'll introduce the concept of an activity profile, a description of the amount of processor time used by different programs and subroutines running in a minicomputer. Fig 5 shows a portion of the activity profile of a Fortran program in terms of processor utilization vs. memory address. Memory addresses in turn correlate with some of the subroutines used by the program. This activity profile shows high processor utilization (nearly 40%) in the routine .PACK, stored near memory address 31740 (octal) for this particular application. By showing the relative processor load of various parts of application code, an activity profile details those portions of code which, when converted to firmware, can produce an improvement in performance. But even if an activity profile is flat, microcode can provide a significant and predictable performance increase.

You can measure the activity profile of an existing application in several ways, most of which depend upon an external sampling mechanism running asynchronous to the application. In a multiprogramming environment, for example, you could run a sampling program at specified internals to analyze your mini's processing. Alternatively, you could use another mini to periodically interrupt and sample your computer's processing. In any event, consider the assistance or support for activity profile generation offered by the mini's manufacturer as an important part of a microprogramming package.

Once you've decided what to put into microcode, writing, compiling, loading and executing the microcode need be no more difficult than using any other language.

Here's a brief outline of how to take a microprogram from concept to execution. Using an activity profile generator, determine the most appropriate part of the application to program in microcode. Then, selecting an available area of control store, write the required code and perhaps even modify the algorithm to use special features available in firmware. A microassembler then converts your mnemonics to binary code for the control processor. Next, using a microdebug/editor facility, load dynamic control store with your microprogram and debug the program, using the code modification and breakpoint features available in a good debug/edit package. When satisfied with your program's accuracy, create mask tapes for permanently burning your program into ROM or else store the object microprogram on a disk file and continue to execute it only in dynamic control store.

Implicit in this description is the use of much hardware and software support provided by the manufacturer. Microcode is of necessity machine-dependent, and its ease of use is determined in large part by the minicomputer manufacturer's implementation of the microcode structure and its offerings of supportive software and hardware.

Microprogramming can be easy and useful, but as with every other aspect of minicomputers, it must be carefully evaluated from many standpoints. This introduction should help you understand the technique so you can evaluate its place in your minicomputer applications. ◆

**COMING NEXT MONTH**
Optimizing Software For Zilog's Z-80

# elasco
# MODIFIED/CUSTOM

The problem of selecting a standard versus a special power supply is a classic one. The basic considerations apply as much to the power supply manufacturer as to the user: the economies of standardization and volume versus the extra costs of customizing design parameters for a "tailor-made" fit to the application.

In over 20 years Elasco has designed and built many different types and configurations of power supplies. Each product has been assigned a design number, catalogued and fully documented. This very large library of designs covering the four major types of power supplies — series regulated, switching, ferroresonant, and DC to DC — combined with our in-house transformer winding facilities allows us to respond

## 1 POWER SUPPLY FOR AN ALPHANUMERIC TERMINAL

**MODEL:** PC4084

**FEATURES:** ■ UL Listing ■ Overload, Overvoltage, and Over-Temperature Protection ■ Excellent Shock and Vibration Construction ■ Electromagnetic Shielded Transformer ■ Self-Contained Forced Air Cooling

**PERFORMANCE CHARACTERISTICS:** ■ Wide Input Ranges of 95 to 130 Vac and 190 to 260 Vac @ 47-63 Hz ■ Four Outputs: +5 Vdc @ 4A, -5Vdc @ 1A, +12 Vdc @ 0.5A, -12 Vdc @ 1A ■ Outputs Adjustable to ±5%

**SIZE:** 11" x 6 3/8" x 7½"

## 2 POWER SUPPLY FOR I/O PROCESSING

**FEATURES:** ■ Ferroresonant Transformer with Series Pass Regulation ■ Overload, Overvoltage and Overtemperature Protection ■ Remote Programming for Margin Checking on the System ■ Built to Meet UL 478

**PERFORMANCE CHARACTERISTICS:** ■ Wide Input Range of 90 to 136 Vac @ 60 Hz ■ Four Outputs: +5Vdc @ 36A, -5Vdc @ 2.5A, +12 Vdc @ 2.5A, -12 Vdc @ 1A

**SIZE:** 13 1/8" x 7 5/8" x 8"

## 3 POWER SUPPLY FOR A DATA ENTRY TERMINAL

**MODEL:** PC4090

**FEATURES:** ■ UL Listing ■ Overload and Overvoltage Protection ■ Outstanding Shock and Vibration Construction ■ External Forced Air Cooling

**PERFORMANCE CHARACTERISTICS:** ■ Wide Input Ranges of 90 to 135 Vac and 190 to 270 Vac @ 47-63 Hz ■ Four Outputs: +250 Vdc @ 0.03A, +5Vdc @ 3A, +12Vdc @ 0.3A, -12Vdc @ 0.3A

**SIZE:** 9" x 5" x 2.75"

## 4 POWER SUPPLY FOR AN AUTOMATIC PAPER SPLICER

**MODEL:** PC2243

**FEATURES:** ■ UL Listing ■ 53,000 Hour MTBF Rating ■ Convection Cooled

**PERFORMANCE CHARACTERISTICS:** ■ Wide Input Range of 95 to 130 Vac @ 50-400 Hz ■ Dual Outputs: +12 Vdc @ 0.3A, -12 Vdc @ 0.3A ■ Outputs Adjustable from 11-13 Vdc

**SIZE:** 5" x 3.3" x 1.75"

## 5 POWER SUPPLY FOR A PUNCH TAPE RECORDER

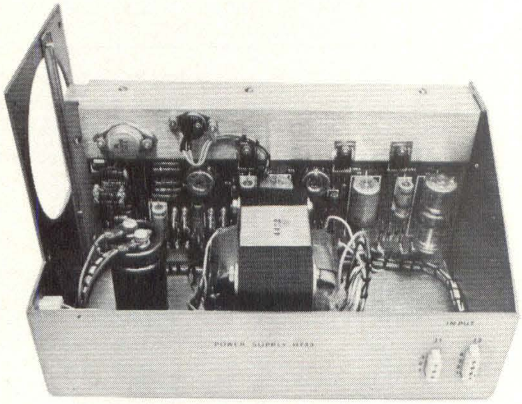
**MODEL:** PC2259

**FEATURES:** ■ Overload and Overvoltage Protection

**PERFORMANCE CHARACTERISTICS:** ■ Input: 115/230 Vac @ 50/60 Hz ■ 70°C Operating Temperature ■ 1000 Vdc Hi-Pot Output to Chassis ■ Dual Outputs: +5Vdc @ 1.2A, +17 Vdc @ 2A

**SIZE:** 6.8" x 4.7" x 3.5"

1



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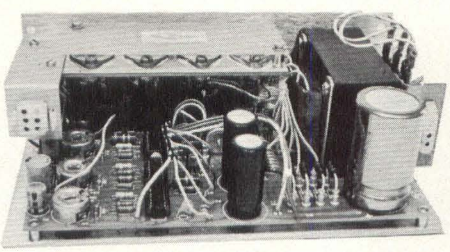

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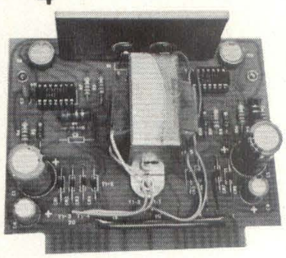

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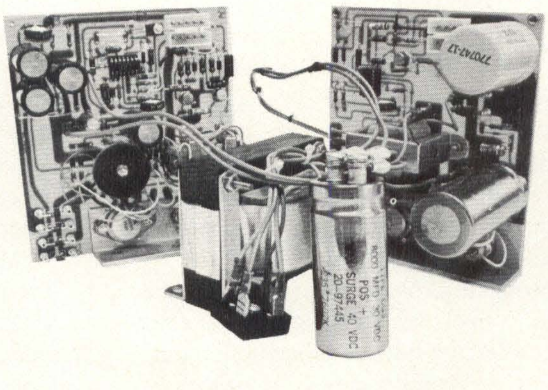

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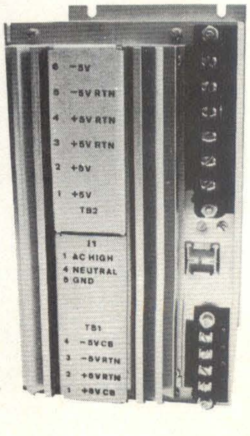


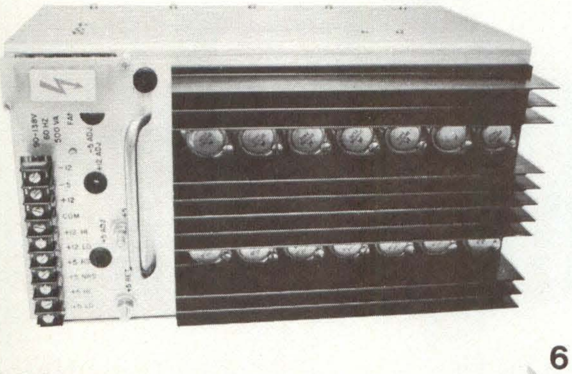
# POWER SUPPLIES

to customers needs for custom-tailored, or "special," requirements with fast turnaround and outstanding cost-effectiveness due to savings in engineering, production, purchasing and set-up time.

In addition, Elasco is accustomed to modifying its standard power supplies, as the clothier would alter a garment, to pass on the savings and proven performance of the standard-off-the-shelf product at the minimal cost additions of a tuck here and a let-out seam there.

The following power supplies represent a small sample, but may help to indicate special features and packaging configurations of interest to you.

2



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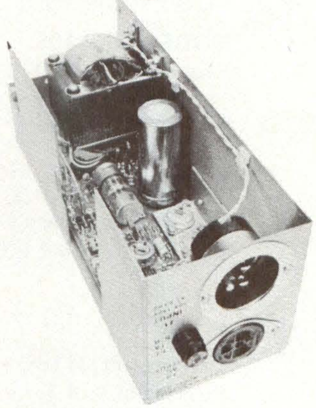

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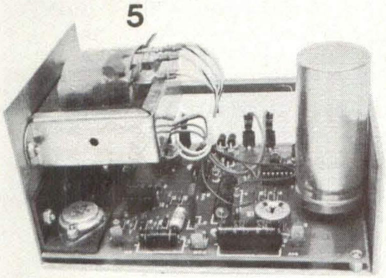

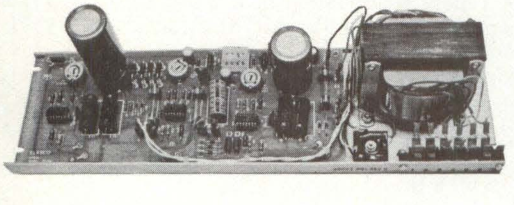

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## 6 POWER SUPPLY FOR COMPUTER PERIPHERAL APPLICATIONS

**MODEL:** PC2241

**FEATURES:** ■ Built to Meet UL 478 ■ Overload and Overvoltage Protection ■ Split Input Primary; 105 to 130 Vac and 210 to 260 Vac @ 47-63 Hz ■ Primary Fuse Protection

**PERFORMANCE CHARACTERISTICS:** ■ Dual Outputs: +5Vdc @ 4A, -15 Vdc @ 1.5A ■ Outputs Adjustable to ±5%

**SIZE:** 12" x 4 1/8" x 5¼"

## 7 POWER SUPPLY FOR A PORTABLE ALPHANUMERIC TERMINAL

**MODEL:** PC4095

**FEATURES:** ■ High Efficiency Switching Regulator Design ■ Modular Sectional Construction to Drop into Customer's Unit ■ Electromagnetically Shielded Transformer ■ Light Weight

**PERFORMANCE CHARACTERISTICS:** ■ Two Input Options of 105 to 125 Vac @ 50-400 Hz or Battery, 11 to 13 Vdc ■ Four Outputs: +5 Vdc @ 7A, -5 Vdc @ 0.5A, +12 Vdc @ 1.5A, -12 Vdc @ 0.3A.

**SIZE:** 6" x 5½" x 1¾"

## 8 POWER SUPPLY FOR A COMPUTER APPLICATION

**MODEL:** PC2246

**FEATURES:** ■ Ferroresonant Transformer with Series Pass Regulator Design. Transformer Construction Permits Frequency Change Via Taps for 50/60 Hz Operation ■ Convection Cooled Package ■ Overload and Overvoltage Protection ■ Plug-In Regulator Card

**PERFORMANCE CHARACTERISTICS:** ■ Wide Input Range of 90 to 132 Vac ■ Dual Outputs: +10 Vdc @ 10A, -5Vdc @ 1.5A

**SIZE:** 10½" x 5½" x 8"

## 9 POWER SUPPLY FOR A KEY STATION TERMINAL

**MODEL:** PC3161

**FEATURES:** ■ Split Primary 117.5/235 Vac @ 47-63 Hz with the Primary Winding Tapped at 100 Vac to Permit Connections to 100/117.5/200/217.5/255 Vac Mains ■ Overload and Overvoltage Protection ■ UL and CSA Listing ■ Electromagnetically Shielded Transformer ■ Convection Cooled

**PERFORMANCE CHARACTERISTICS:** ■ Triple Outputs: +5Vdc @ 3.0A, +12 Vdc @ 2.0A, -12 Vdc @ 0.3A

**SIZE:** 15.75" x 4.7" x 5.87"

## 10 POWER SUPPLY FOR BLOOD ANALYZER

**MODEL:** PC5042

**FEATURES:** ■ Autotransformer with Inputs from 100 to 240 Vac @ 50/60 Hz via Single Tap Change ■ High Reliability

**PERFORMANCE CHARACTERISTICS:** ■ Outputs: 5 Vdc @ 6A, 20 Vdc @ 250 mA, 200 Vdc @ 25 mA, 115 Vac @ 500 mA Isolated from Primary, 30 Vac @ 1A, 5-8 Vac @ 100 mA.

**SIZE:** 5" x 6" x 10"

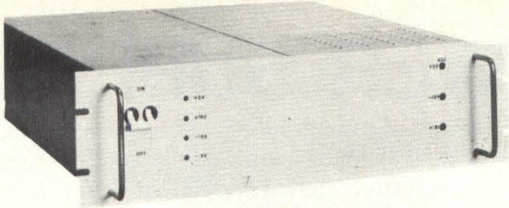
## 11 POWER SUPPLY FOR MAINFRAME COMPUTER

**MODEL:** PC4103

**FEATURES:** ■ 60°C Operating Temperature ■ 45% Efficiency ■ Internal Cooling ■ 5¼" Panel Height ■ Pilot Light Indicators for Each Output ■ Front Panel Voltage Adjusting Pots ■ Front Panel Circuit Breaker ■ Internal Modularized Construction

**PERFORMANCE CHARACTERISTICS:** ■ Inputs: 100 to 130 and 200 to 260 Vac @ 47 to 63 Hz ■ Outputs: +5.25 Vdc @ 81A, -5 Vdc @ 0.9A, +15 Vdc @ 2.3A, -15 Vdc @ 2.3A, -55 Vrms @ 50/60 Hz

**SIZE:** 5¼" x 19" x 19"



## 12 MILITARIZED DC TO DC CONVERTER FOR HELICOPTER GUN CONTROL

**MODEL:** PC216 VI

**FEATURES:** ■ Rugged Construction to Withstand High Shock and Vibration ■ MTBF: 50,000 Hours

**PERFORMANCE CHARACTERISTICS:** ■ Input: 24 to 30 Vdc ■ 26.1 to 29.2 Vdc @ 0.36A

**SIZE:** 2.18" x 1.53" x 3"

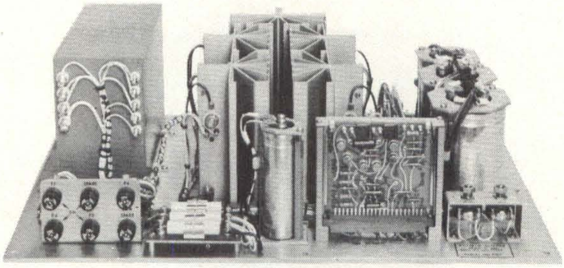
## 13 POWER SUPPLY FOR SONAR APPLICATION

**MODEL:** PCE1259

**FEATURES:** ■ Fully Militarized for MIL 16400 E with No Exception Taken ■ 60G Shock ■ 95% Humidity ■ 60°C Operating Temperature ■ No Moving Air

**PERFORMANCE CHARACTERISTICS:** ■ Input: 230 Vac @ 50-60 Hz ■ Output: 28 Vdc @ 12A

**SIZE:** 17" x 8" x 17"



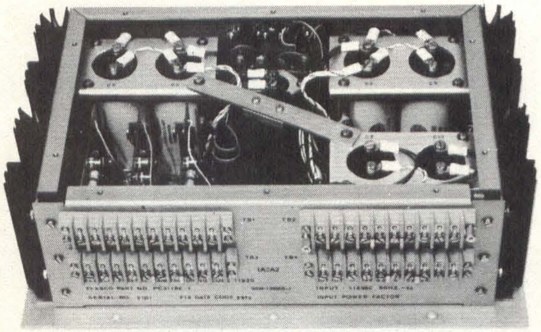
## 14 POWER SUPPLY FOR SHIPBOARD TERMINAL

**MODEL:** PC4105

**FEATURES:** ■ 70°C Operating Temperature ■ -62°C Storage Temperature ■ Overvoltage Protection on All Outputs ■ MTBF of 15,000 Hours ■ Meets MIL-STD 461A/462, MIL-S-901C Grade A, MIL-STD 1678B Type 1

**PERFORMANCE CHARACTERISTICS:** ■ Input: 105 to 125 Vac @ 50 to 400 Hz ■ Outputs: +5 Vdc @ 12A, +12 Vdc @ 4A, -12 Vdc @ 2A, -5 Vdc @ 1.2A

**SIZE:** 6" x 6" x 14.3"



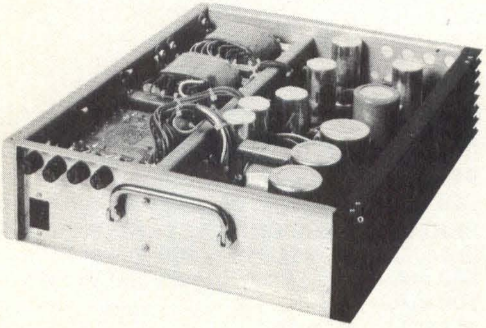
## 15 POWER SUPPLY FOR SHIPBOARD PRINTER

**MODEL:** PC3118E-1

**FEATURES:** ■ Temperature to MIL E 16400 E Class 4 ■ Humidity MIL E 16400 E ■ Vibration MIL-STD 167 Type 1 Equipment ■ Shock Per MIL-S-901 for Class 1 Type A Equipment ■ Salt Spray Per ASTM Publication B 117-67 for a Period of 48 Hrs.

**PERFORMANCE CHARACTERISTICS:** ■ Input: 115 Vac @ 57/63 Hz ■ Outputs: +5 Vdc @ 2A, +14 Vdc @ 4A Av., +14 Vdc @ 16A Peaks, -14 Vdc @ 4A Av., -14 Vdc @ 16A Peaks

**SIZE:** 16" x 5" x 9"



## 16 POWER SUPPLY FOR HIGH SPEED PRINTER

**MODEL:** PC6018

**FEATURES:** ■ Switching Regulator ■ All Six Outputs Synchronized to a Single Clock @ 20K Hz ■ Voltages Have Current Fold Back and Over Voltage Protection ■ Outputs Remote Sensed ■ Overall Efficiency 75% ■ Meets UL, CSA and VDE ■ Convection Cooled

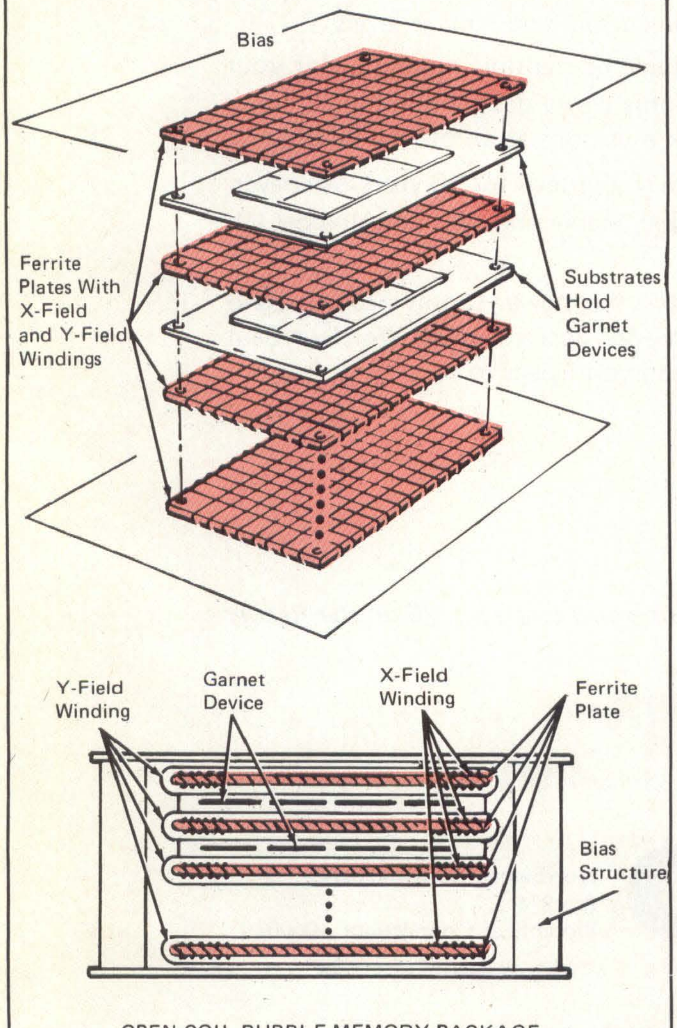
**PERFORMANCE CHARACTERISTICS:** ■ Input: 110/220 Vac ±15% @ 47-63 Hz ■ Outputs: 5 Vdc @ 32A, 7 Vdc @ 3A, 9 Vdc @ 2.5A, 14 Vdc @ 11A, 12 Vdc @ 6.5A, 24 Vdc @ 6.5A

**SIZE:** 17.75" x 14.2" x 4"

# Bubble-memory packaging alternatives: producibility vs. interchangeability

In their efforts to devise efficient packaging structures for bubble memories, engineers at Rockwell International, Anaheim, CA, have developed two alternative methods of coping with the windings required to provide magnetic biasing and to read, write and shift data. Though neither method appears optimum, each provides its own set of advantages, according to Thomas Chen and John Ypma, designers of both the open-coil and stripe-line packages.

In the open-coil version, all memory and coil chips remain separate and interchangeable. Yet this version does not require individual small packages for each coil, because the entire package fits together in sandwich fashion. The open-coil structure eliminates most of the interconnections in the coil levels by packing the memory chip and associated electronics in a single structure, say Chen and Ypma. And because coil windings are separated from the memory chip, the designers can independently adjust the coil sizes for optimum power dissipation and field uniformity. The separate coils also leave spaces for forced-air-cooling flow.



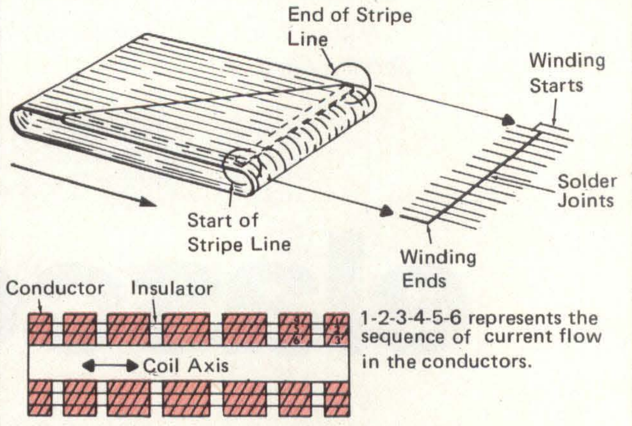
OPEN-COIL BUBBLE MEMORY PACKAGE

To achieve these advantages, the NASA-sponsored team designed a structure in which the coil windings wrap around ferrite plates.

Because of the magnetic shielding effect of the plate, the magnetic field in the space above or below the coil winding equals the field generated by a single layer of conductors. When two identical magnetic plate coils are placed in parallel, the magnetic field between the plates is identical to that generated inside a close-wound coil.

The designers created a rotating field network by orthogonally winding two coils around the magnetic chips, and then stacking a number of these chip coils in a bias structure. The bubble devices fit between the coils.

This approach extends to bubble-memory-module packaging where a large number of chips must be driven in several independent rotating fields, say the designers. All memory devices and their associated electronics can be mounted in planes, and all magnetic chip coils and their driver electronics can be mounted in separate field planes. The device planes are then inserted between the coil planes and within the bias



STRIPE-LINE BUBBLE MEMORY PACKAGE

structure. All memory chips under the same coil windings can be operated as independent units.

Less versatile, but more uniform and easy to produce, the stripe-line coil structure consists of varying widths of conductor etched from a film supported on a polyamide substrate. The multiple-layer stripe-line coil has conductors in series along the layer direction, rather than in the axial direction, which minimizes potential differences, explain the designers, who wrapped the stripe-line layer around a fixed coil form, and electrically connected the outer ends of the conductors as a single loop to form a field coil. Because the etched pattern controls conductor length, width and spacing, coil parameters like size and shape show less variation from run to run than do wire-wound coils. "The stripe-line coil arrangement is also simpler, easier to wind, and has better field uniformity inside the coil and less coil loss at high-frequency operation," they add.

The multiple-layer stripe-line coil structure reduces the high-frequency loss in two ways: Allowing sufficient spacing between the layers or columns of conductors reduces the interwire coupling, and with the winding in the coil connected in series, the current flows through adjacent vertical arrays or columns of conductors. This winding arrangement minimizes the potential differences between neighboring turns, thereby minimizing high-frequency loss due to interwire coupling.

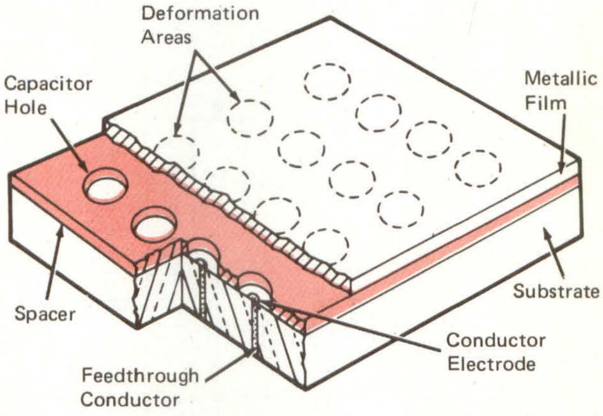
## MOSFET-controlled array readies data for optical storage

Storing data in a laser hologram, an optical memory incorporates a device – termed a page composer – that modulates a laser beam and thereby converts binary electrical inputs into their optical equivalents. Liquid crystals, electro-optic crystals and ferro-electric ceramics can all perform this conversion, but these devices lack sufficient speed or contrast ratio, degrade with extended use, or cannot be addressed from diverse angles, according to G. A. Bailey of NASA's Marshall Space Flight Center and L. S. Cosentino of the RCA Corp.

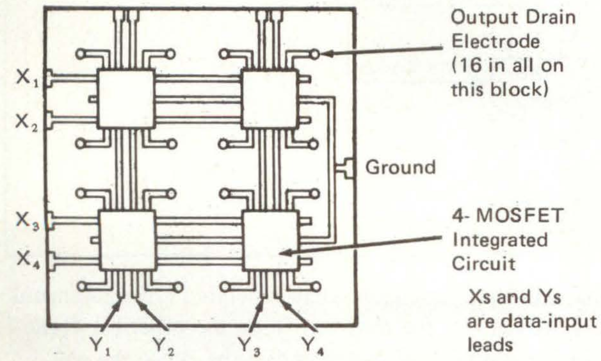
To remedy these shortcomings in conventional page composers, Bailey and Cosentino devised a unit that consists of an array of deformable metal membranes controlled by MOSFETs. A typical 4 x 4 array consists of a 1.25-$\mu$m-thick spacer sandwiched between a glass or ceramic substrate and a thin metallic film. Each 2.5-mm-dia hole in the spacer contains an electrode and thus acts as a capacitor.

Storing a charge in a hole deforms the metal over that hole, and when light from a laser beam scans the array, it scatters from deformed parts of the membrane but is reflected to the holographic storage system from undeformed parts. Scattered light from a specific position produces a zero in the optical memory location for that position.

Selectively energizing MOSFETs on the substrate's backside activates individual capacitors by conducting charge from each energized MOSFET's output drain electrode to a feedthrough conductor that ends at the electrode in the corresponding hole. Each of the four ICs on the backside contains four MOSFETs, and for a MOSFET to be energized, it must lie at the intersection of an energized X lead and an energized Y lead to the array.



4 x 4 PAGE COMPOSER ARRAY



Xs and Ys are data-input leads

UNDERSIDE OF PAGE COMPOSER

Bailey and Cosentino report that 30 V will deform the patented device's membrane. Fabricating the page composer, they first coat the substrate with a photoresist, expose the photoresist and etch holes through it, and fill those holes with conductive material. They then deposit electrodes by a chrome flash followed by about 7 $\mu$m of aluminum, and etch away unwanted material.

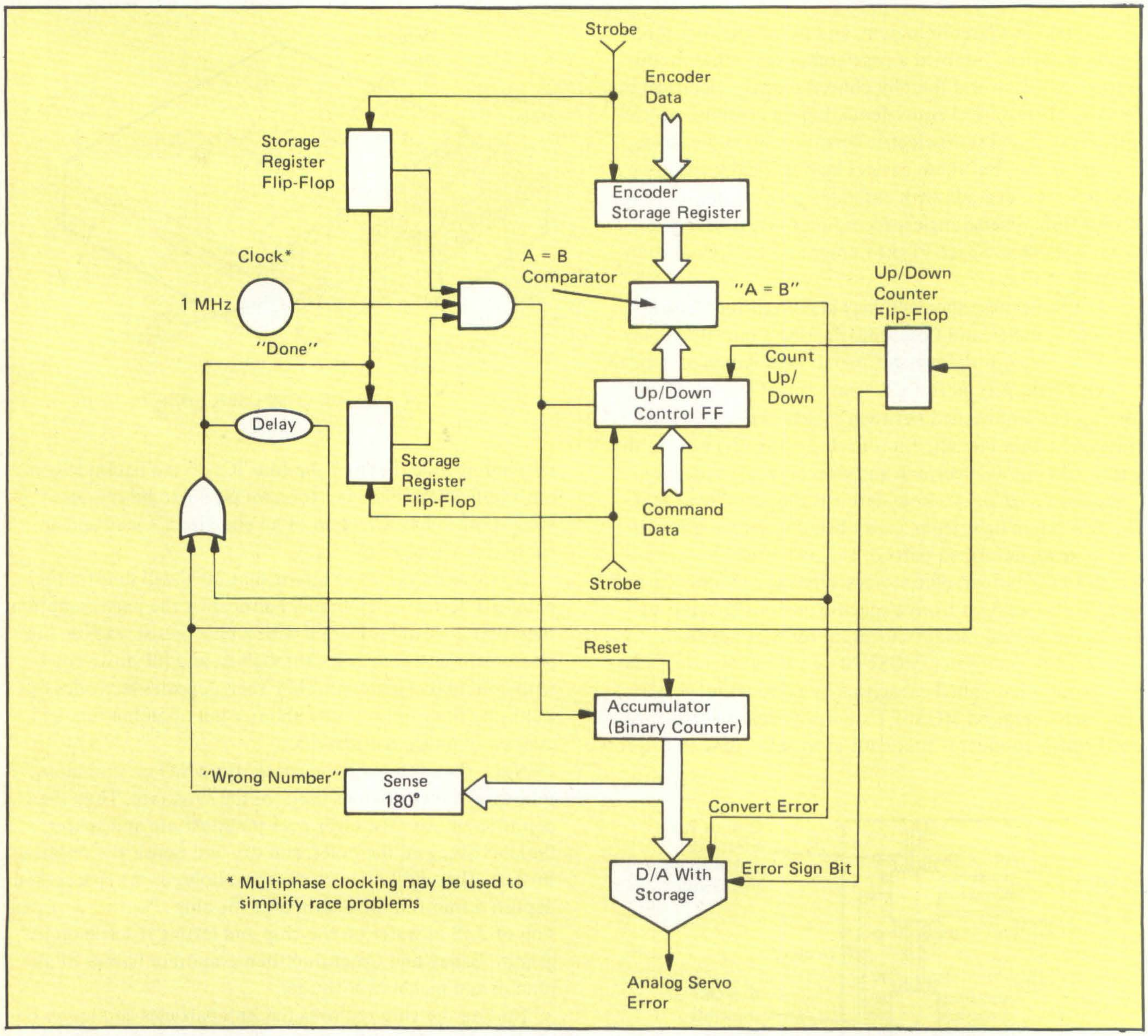
Next, they fabricate the spacer from SiO or aluminum, following the same steps used for the substrate. They then deposit a photoresist layer over the substrate and spacer, thereby filling all the holes, and dry and polish the resulting surface. They drill micrometer-sized holes in the spacer, and deposit a thin film of gelatin over the chip. Pouring a suspension of ZnS in water on the chip and letting it settle on the gelatin, Bailey and Cosentino then evaporate flashes of aluminum and nickel over the gel.

Rinsing the chip removes the ZnS particles and leaves behind a metal film with micrometer-sized holes; this film serves as a seeding layer on which the two designers deposit the full thickness of a nickel membrane. As a final step, they remove the photoresist beneath the membrane by bathing the array in solvent, which drains away through the micrometer-sized holes.

# Digital servo substitutes for synchro system

For angular positioning, a synchro-demodulator servo system can compute the shortest distance between desired and actual position and can resolve all portions of the 360° travel unambiguously. However the rugged synchro is unwieldy, expensive to interface with computers and suffers from a limited accuracy (±0.1°), according to Frank Byrne of the Kennedy Space Center.

Seeking a more accurate, simpler method, Byrne designed a digital control system using digital shaft angle encoders. With error responses similar to those of a synchro, his system computes the correct error magnitude and direction using a "cut and try" routine. Correct error signals can never exceed 180° and incorrect signals always exceed 180°, Byrne notes.



* Multiphase clocking may be used to simplify race problems

While a shaft encoder signals the current position of the controlled device, a parallel BCD signal commands the desired position. With suitable clocks, both encoder word and desired word strobe into two registers, generating a "loaded" signal. The "loaded" command initiates control action, letting the clock increment or decrement the up/down counter – depending on the mode of the direction flip-flop, FF. Simultaneously, the previously cleared accumulator increments – count for count – with the up/down counter.

When the digital value of the up/down counter matches the previously stored encoder value, or when the accumulator count exceeds a value of 180°, the incrementing process terminates and one of two following operations occurs: If the accumulator exceeds 180°, all counters reset, the cycle terminates and no new error data transfers from the error digital to analog (D/A) converter. Additionally, the direction flip-flop for the up/down counter toggles – the controller "wrongly" assumes the error magnitude and direction, and therefore ignores the generated error command, correcting itself for the next try. If, on the other hand, the register comparator signals the end of the cycle, the controller recognizes a correct solution and transfers the resulting accumulator count to the error D/A converter.

# Cooling-fin nomogram helps lower packaging costs

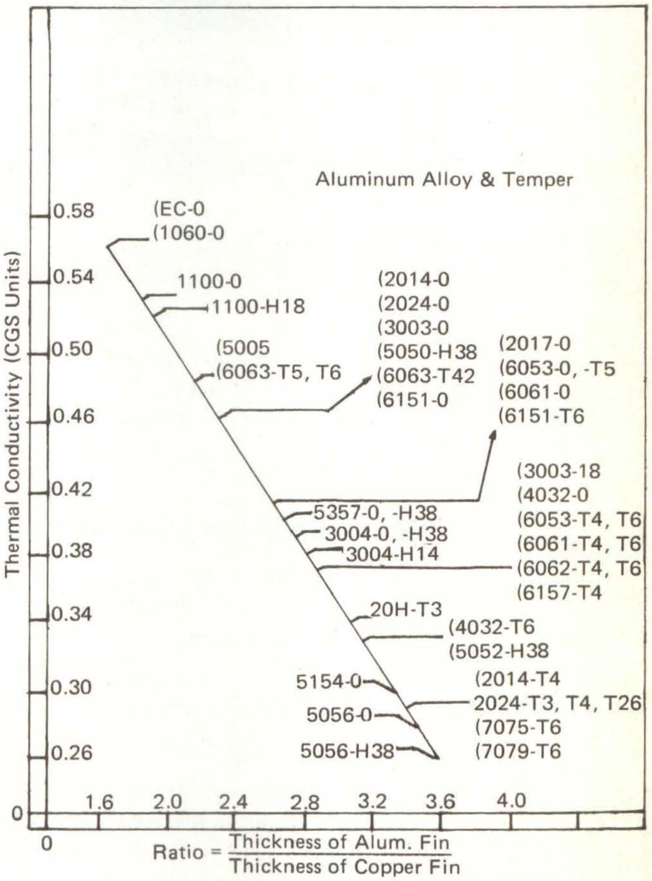
Long used for cooling components within digital systems, aluminum heat sinks may pose more problems than they solve. For example, similarly shaped and sized aluminum heat sinks, used as replacements for expensive copper, can vary in their cooling abilities by as much as a factor of two to one. According to Will Parrish, an engineering manager at International Rectifier Corp.'s Semiconductor Div., El Segundo, CA, "among the alloys of aluminum, each has different properties, which may make it more or less adaptable as cooling fin material in a given application."

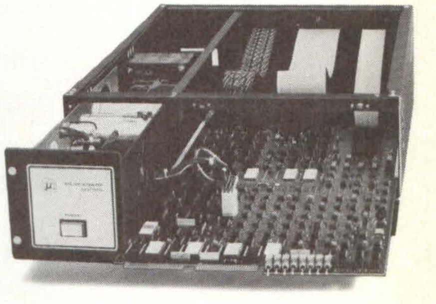
To facilitate your choice of an aluminum alloy to replace copper, Parrish has prepared a nomogram showing a curve of the thermal conductivity of aluminum plotted as a ratio of the thickness of the fin divided by the thickness of a copper fin it replaces. For the various alloys he has included, the thermal conductivity – and thus the thickness ratio – varies over a range of 2.15:1. But beyond thermal conductivity, other selection factors, like weight and machinability, come into play.

As an example, notes Parrish, suppose you select one of the electrical grade alloys of aluminum such as the 1100-H18 with a thermal conductivity of 0.52 in CGS units. Further, assuming that you wish to replace an electrical grade copper with 0.93 thermal conductivity, you can see from the nomogram that the aluminum fin needs to be 1.9 times the thickness of the copper fin to have equal internal thermal resistance. Therefore, with a heat generating device mounted at the center of the fin, the average fin temperature of the newly selected aluminum fin would be the same as the previous copper fin. Thus, assuming that they have equal radiating and conducting surface conditions, the cooling should be identical.

Note that if you used the 5056-H38 alloy of aluminum, the fin would have to be almost 3.6 times the thickness of the copper fin to achieve equal cooling efficiency.

Coupling into the economics of the selection, notice that at today's market conditions, aluminum probably costs no more than 50% of copper per pound, and that aluminum weighs approximately 29% of copper per unit volume. Thus if the aluminum fin is to be 1.9 times the thickness of a copper fin, the relative cost equals the product of the thickness, cost and density ratios. The 1100-H18 alloy costs about 27% of an equally effective copper cooling fin.





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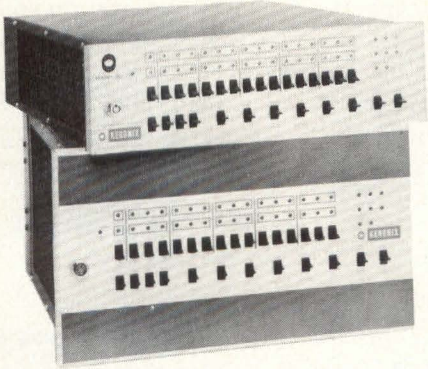

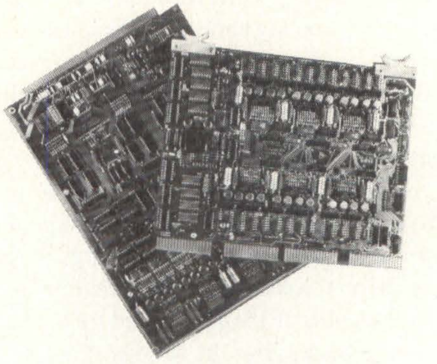

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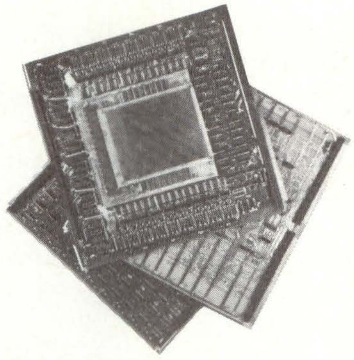

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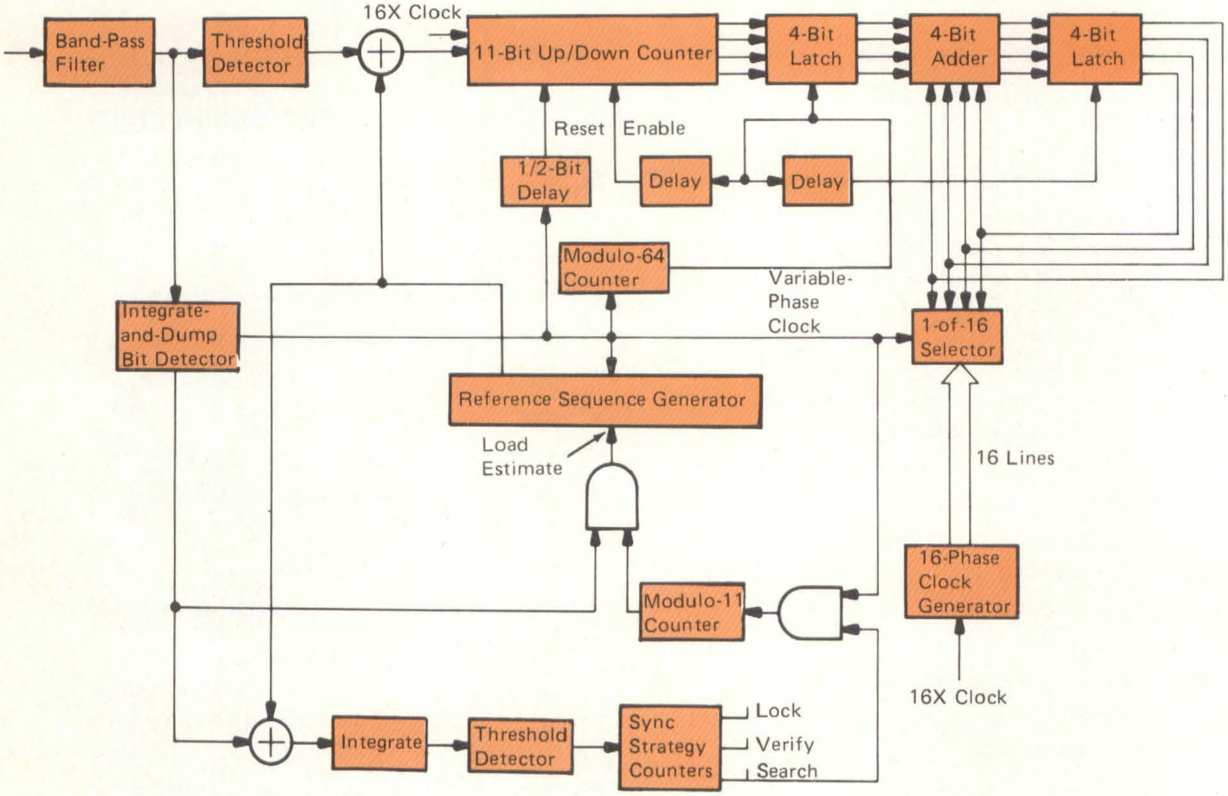
CIRCLE 30

# Digital code correlator increases telemetry's noise immunity

To reduce the temperature dependence and noise sensitivity normally associated with telemetry receivers, a designer at Johns Hopkins Univ., Baltimore, replaced a voltage controlled oscillator and analog filter with a digital circuit. Designed to process biphase-level pulse-code-modulated signals, the code-correlation synchronizer uses "sequential estimation" to reduce the time required to achieve a "lock condition" at small signal-to-noise ratios.

According to Carroll Pardoe, working under contract to NASA's Goddard Space Flight Center, the filtered input signal is applied to a threshold detector for subsequent clock synchronization and to an integrate-and-dump (I-and-D) bit detector for sequence synchronization.



The output of the I-and-D bit detector forms the nonreturn-to-zero equivalent of the input signal. This equivalent signal is compared with an internal reference signal in a modulo-2 adder, whose integrated output forms the required correlation-function estimate. If the threshold detector shows that the correlation is less than the preset requirement, the sync logic activates a search mode.

In this search mode, the output of the reference sequence generator is interrupted for 11 clock cycles, and the I-and-D bit detector output is entered as an initial condition in the sequence generator. After the 11 bits are entered, the reference generator again functions as a normal pseudorandom sequence generator. If the correlation value is then better than the preset value, the sync logic enters the verify mode. The system remains in the verify mode for a preset period (1 to 15 code sequences); if the correlation level is maintained, the system subsequently enters the lock mode. If the correlation drops below the threshold level, the system reverts to the verify mode; if the noncorrelation persists, the system enters the search mode again.

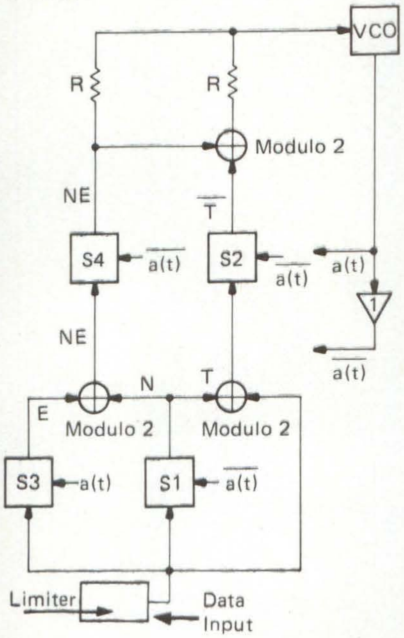
Clock synchronization comes from a threshold detector that converts the filtered system input to a binary signal, and by comparing this signal to the internal reference signal. The result is a square wave that occurs at exactly the clock frequency if the two signals are in phase.

# Random-data detector self-synchronizes signals

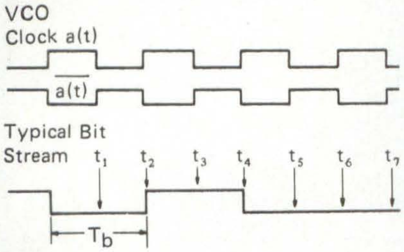
For use with radio or cable data-control links, this synchronizer permits the reception of data without requiring a clock signal or self-clocking coder. According to its designers, Tage Anderson, Jack Holmes and William Hurd, all of Caltech's Jet Propulsion Lab, Pasadena, CA, the detector includes a phase locked loop (PLL) and a voltage controlled oscillator (VCO) to reconstruct the data clock rate at the receiver.

The detector loop incorporates a VCO that generates a square-wave output at twice the frequency of the incoming bit rate. The true and complement outputs at a(t) and a($\bar{t}$) are the data transition sample pulse and the mid-bit sample pulse, respectively. When the PLL is locked, the leading edge of timing signal a(t) occurs at the bit transition, and the leading edge of timing signal a(t) occurs at mid-bit.

The leading edge of timing signal a(t) samples the input data to determine the sign of the phase error and to derive the error signal. The leading edge of timing signal a(t) samples the input data to determine whether a transition has occurred. If a transition has occurred, a binary-valued error voltage is applied to the VCO. If a transition has not occurred, a voltage midway between the two binary values is applied to the VCO. This voltage provides an output frequency from the VCO when no transition has occurred, that is approximately equal to the received data rate.

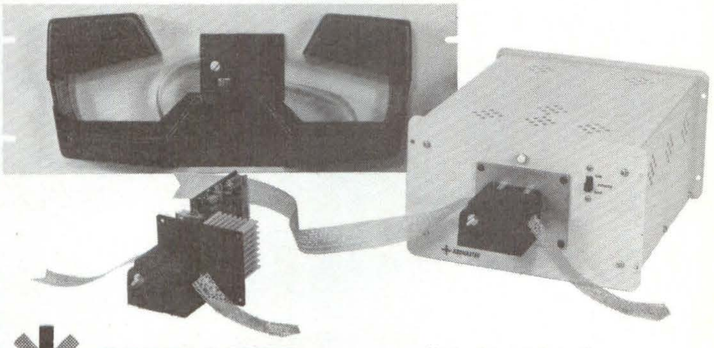


S = Storage Element
T = Transition Signal
E = Error Signal
NE = Normalized Error Signal
VCO = Voltage Controlled Oscillator
I = Inverter
$T_b$ = Bit Time



At $t_1$ the data is first sampled and then stored in storage element S1. At $t_3$ the stored data is added modulo 2 to the present data and is stored in S2. The output from S2 then indicates whether a data transition occurred at $t_2$. At $t_2$ the data is sampled and stored in S3. The output from S3 is added modulo 2 to the output from S1, which serves as a normalizing term N.

This addition assures the independence of the error signal's sign from the transition's direction. At $t_3$ the normalized sign of the error signal NE is stored in S4. The output from S2, the transition detector, remains for one full bit time between $t_3$ and $t_5$. The output from S4, the sign of the error signal, remains for the same length of time. The data is eventually clocked into a serial-input shift register.



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Addmaster's famous Model 601 Paper Tape Reader reads any standard tape at 150 characters per second asynchronously. It has a solid state light source, bi-directional stepper motor drive and the lid lifts for easy loading. It is available with or without TTL-interface including end-of-tape-sensing. Can be purchased in a stand-alone model with parallel or serial output . . . or with a fanfold box holding 150' of paper tape.

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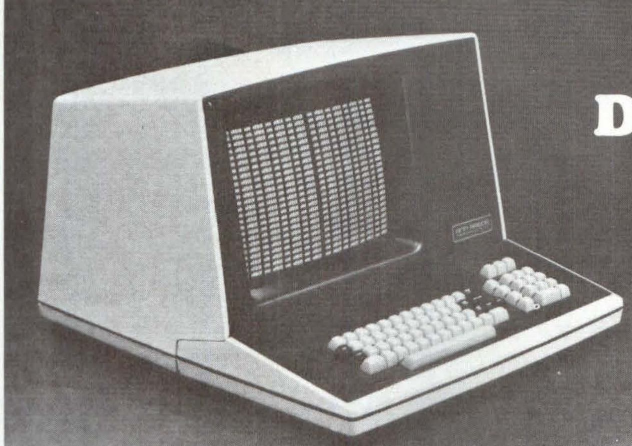
CIRCLE 31



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CIRCLE 32

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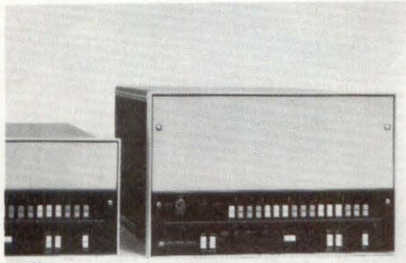
# product news

*Editor's note: Three firms have recently introduced newly designed minicomputer CPUs; we lead off Product News this month with reviews of those machines.*

## MICROPROGRAMMABLE MINIS VARY CYCLE TIME

For use in multi-terminal networks and advanced data analysis, high-speed graphics and computer aided design, the two CPUs in the 21MX E-Series have a 560-ns memory cycle time and a variable microcycle time that ranges as low as 175 ns. The CPUs transfer data at burst rates up to 5.7 million words/sec through a microprogrammable processor port, which directly accesses a CPU's main data bus. A microprogrammable block I/O transfer, which uses the mini's standard I/O structure, allows data-block movement at up to 1.5 million words/sec. The 8¾"-high 2109A accommodates nine powered I/O cards and up to five memory cards (80K words), while the 12"-high 2113A supports 14 I/O cards and 10 memory cards (160K words). Standard features include parity checking, extended arithmetic unit, floating point capability, data communication instructions and power supply. Price: $13,900 for a 2109A with 32K words of main memory, Fast Fortran processor and 1K writeable control store. OEM quantity discounts available. Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501 **Circle 228**



## RACK-MOUNT MINIS SERVE COMM & SENSORS

These two processors, designated Series/1 Model 3 and Model 5, are general-purpose units with both communications and sensor based capabilities. The 19" rack-mountable units accommodate 16K-64K bytes (Model 3) or 16K-128K bytes (Model 5) of memory in 16K byte increments and cycle in 800 ns (Model 3) or 660 ns (Model 5). Available options include a 9.3-Mbyte fixed-disk storage unit, a diskette unit with 1- or 2-sided recording capability, a 120-cps bidirectional matrix printer, a 1920-character display with alphanumeric keyboard and a sensor I/O unit that can accommodate up to eight digital or analog I/O cards. Average weighted instruction time for the Model 3 equals 11.8 μs; for the Model 5, 3.9 μs. Price: $10,000 to $100,000 per system, depending on options. IBM Corp., General Systems Div., P.O. Box C-1645, Atlanta, GA 30301. (404) 256-6797 **Circle 227**

## HIGH-END MINI FAMILY ALLOWS NETWORK CONFIGURATIONS

The three minis that constitute the V77 family can operate independently or – without special conversion interfaces – can form elements in communications and data networks, shared memory systems or distributed networks. All of the units share a dual-bus, microprogrammed architecture and provide 32-bit arithmetic capability and a 187-instruction set with byte, word and double-word addressing. Other standard features include hardware multiply-divide, capability for 64 vectored interrupts, DMA, real-time clock, teletypewriter/CRT controllers and multi-device automatic program loaders. At the low end of the family, the V77-200 comes on one 10.8" x 17" board, has an 8-register CPU and handles 8-, 16- or 32-bit data. It accommodates up to 32K 16-bit words of 660-ns MOS memory, provided in 8K-, 16K- or 32K-word modules in a chassis that includes power supply and I/O controllers. The mid-range V77-400 can function as an upgrade from the V77-200 or as the middle unit in a heirarchical network. It has power fail/restart, memory protect and dual-port memory capabilities and can serve up to one million words if equipped with an optional memory manager; standard main memory support equals 256K words. The unit allows user microprogramming, as does the top-end V77-600, which incorporates a 370-ns cache memory and also accommodates up to one million words of main memory. A Megamap option divides this memory into 512-word pages and assigns these pages to individual application programs. Prices: $1200 for the V77-200 (without memory), $10,100 for the V77-400 (with 32K words of memory) and $22,450 for the V77-600 (with 64K words of memory). Varian Data Machines, 2722 Michelson Dr., Irvine, CA 92713. (714) 833-2400 **Circle 226**

## FIXED-HEAD DISK WITHSTANDS 10G

Compatible with the manufacturer's other disk products and available with controllers for many CPUs, this fixed-head disk memory stores 9.6-76.8 Mbits and withstands 10G, 11ms shock. Model 7510 costs 50% less a bit than the manufacturer's 7300 and 7310 disk memories. Prices range from $8500 to $29,500. Digital Development Corp., 8615 Balboa Ave., San Diego, CA 92123. (714) 278-9920 **Circle 244**

## KEYBOARD DISPLAY SUBS FOR TTYS

For single-machine dial-up applications or multiple-station hardwired systems, this teletypewriter replacement displays 1920 characters in a 960-character format. Besides top-line entry and automatic roll-up, Model 1445 provides a 12" screen with a detachable keyboard that controls 64 displayable characters. Other standard features include switch-selectable automatic line feed and carriage return, blinking underline cursor and a choice of interfaces (including RS232C, TTL or 20/60 mA current loop with switch-selectable 75-9600 baud rates. The 38-lb., portable unit operates in half- or full-duplex conversational mode, serial asynchronous, and utilizes ASCII with odd, even or no parity. You can switch select 10- or 11-bit characters. Price in singles: $1465. TEC, Inc., 2727 North Fairview, Tucson, AZ 85705. (602) 624-2525 **Circle 242**

## 5" FIBER OPTIC CRT FOR LENSLESS PHOTORECORDING

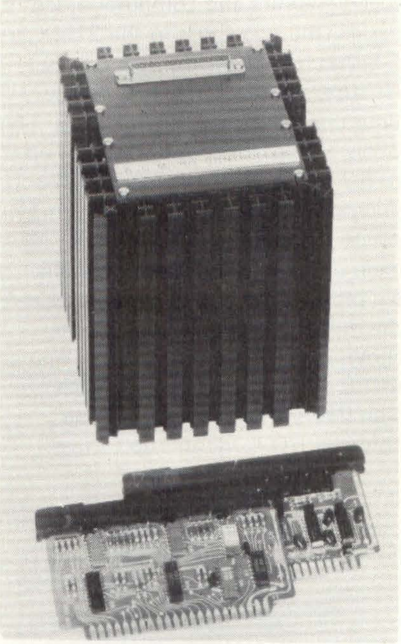
This 5" line-scan fiber optic CRT suits high-speed computer output on microfilm and microfiche, computer aided phototypesetting, high-resolution oscillography and other lensless photorecording applications in which recording film or paper touches the tube face. With a 0.001" line width, Model DC3170 provides a fiber optic faceplate that measures 3.94" x 0.39" with a 2.95" front-surface radius. To ensure sharp character-edge definition, the diameter of the extramural-absorptive cladded fibers measures 6 μm. Measuring 17.32" long, the CRT comes with standard P11 phosphor (options available on request) and requires 12 kVdc accelerator voltage, 5 μA accelerator current and 300 mA heater current. Price: $1500. DuMont Electronics Corp., 750 Bloomfield Ave., Clifton, NJ 07015. (201) 773-2000 **Circle 245**

## STEPPER CONTROLLER OUTPUTS 10,000 STEPS/SEC

Designed to interface with 8- or 16-bit microprocessors, this open-loop stepping motor controller triggers up to one million steps in one-step increments, operates at up to 10,000 steps/sec in one-step/sec increments or 100,000 steps/sec in 10-step/sec increments and offers 100 acceleration and deceleration ramps, programmable remotely or by front panel controls. Model MCU-652 provides three operating modes — manual, semi-automatic and automatic — and three command inputs — start forward, start reverse and stop. An override stop control accommodates single-step, index and slew functions. Price: $800. Advanced Control Systems Corp., 28C Vernon St., Wakefield, MA 01880. (617) 245-8070 **Circle 243**

## COMM CONTROLLER ACCEPTS EIGHT TERMINALS

For formatted data entry, message verification, code conversion, error controls, diagnostic checking, data retransmission, special communications protocols and remote program loading, this communications controller accommodates one to eight teletypewriter-compatible terminals including keyboards, printers, CRT displays, tape cassettes, card readers and floppy disks. Utilizing an RS 232C or current-loop interface, the 8080 microprocessor based controller accepts 110-, 300-, 1200-, 2400- and 4800- baud data and provides a 2-μs instruction cycle. Options include selective calling, automatic answering, data translation, error checking, peripheral clustering and line multiplexing functions. Price: $1000. Applied Systems Corp., 26401 Harper Ave., St. Clair Shores, MI 48081. (313) 779-8700 **Circle 235**



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# product news

## ERASABLE PROM DISSIPATES 450 mW

For high-density, fixed-memory applications requiring rapid turnarounds and program changes, this erasable programmable read-only memory accesses in 450 ns (maximum) and has a 450-ns minimum cycle time. Pin-compatible with the Intel device bearing the same part number, Model TMS 2708JL dissipates less than 450 mW. The 1K x 8 EPROM uses n-channel silicon-gate technology and sets up addresses or data in 10 μs. You can erase data by exposing the chip to ultraviolet light at 10 W-sec/cm$^2$. Price: $64 in 100s. Texas Instruments, Inc., P.O. Box 5012, MS 308 (Att: TMS 2708), Dallas, TX 75222. (713) 494-5115 x3281 **Circle 231**

## INCREMENTAL RECORDER RUNS ON +12 V @ 1 W

Requiring +12 V @ 1 W during operation and 6 mW during standby, this bit-by-bit incremental recorder suits portable seismic and geophysical measurement systems, oceanographic buoys and associated underwater probes, air and water pollution monitors, unmanned weather stations and natural resource exploration. Utilizing an NRZ dual-track complementary recording method, Model ICT-WZ stores up to 2.2 M-bits at 615 bpi on one 300 ft cassette. Transferring data at 100 bps, the unit comes as a stand-alone transport or as a complete system with write-clock stepper and head drivers, parallel-to-serial formatters, A/D converter, sample and hold, and multiplexer for analog inputs. Price for the transport alone: $325 in 1-9 quantities. Datel Systems, Inc., 1020 Turnpike St., Canton, MA 02021. (617) 828-8000 x159 **Circle 232**

## GRAPHICS TERMINAL OFFERS FULL REFRESH

Intended as a Tektronix 4014 terminal replacement, this full-refreshed intelligent terminal interprets commands from the company's TCS Plot 10. Megraphic 6014's basic configuration includes an 8K Data General Nova 3 processor, 17" monitor, graphics processor, ASCII keyboard, RS 232 interface and table with equipment rack. Accompanying software implements dynamic motion without flicker, selective erase, zoom, scale, clip, rotate, translate, rubber-band, blink, window and update. Options include 21" monitor, 128K memory and peripherals including floppy- and hard-disk and magnetic tape. Price: $16,000. Megatek Corp., 1055 Shafter St., San Diego, CA 92106. (714) 224-2721 **Circle 230**

## MOVING-HEAD DISK STORES 0.5M - 2M BYTES

For machine-tool control, moving platforms, chemical plants, oil exploration, food processing and other hostile environments, this moving-head disk drive withstands up to 131°C and as much as 10G. It also operates tilted at up to 45°. Model D-100 stores 0.5-2.0 Mbytes and has 1.1- or 2.2-MHz bit transfer rate. Measuring 7" x 15" x 15" and weighing 20 lbs., the drive has no head-retracting mechanisms and incorporates a spindle mounting that uses preloaded, sealed Class 5 bearings. Price: from $995 in 100s. Digimetrix, Inc., 20954 Corsair Blvd., Hayward, CA 94545. (415) 783-5614 **Circle 234**

## DATA COMM MONITOR DISPLAYS 1024 CHAR.

To help you isolate hardware and software errors in data communications systems, this CRT monitor can present 1024 hex or octal characters as a composite display or as two 512-character data blocks. For displaying data communications transmissions, Interview operates in full- or half-duplex modes at 56 kbps and accepts any protocol, including Bisync and SDLC. Available in rack-mountable or portable versions, the monitor operates on 115V/60Hz or 230V/50Hz and provides a video output port. Clear text appears on the unit's screen as ASCII and EBCDIC, and – with shift characters – as EBCD and Selectric. You can select up to two additional codes. A self-test fills the screen with a 128-character ASCII set without disturbing an active test. Atlantic Research Corp., 5390 Cherokee Ave., Alexandria, VA 22314. (703) 354-3400 **Circle 233**

# Personal Computing

**Personal Computing** is a new magazine about people and computers. In the past year alone, over 10,000 computers were sold to individuals. By the early 1980's, many experts project that over 1,000,000 personal computers will be up and running.

**Personal Computing** recognizes the people's right to know all about computers. After all, the man in the street will make the ultimate decision about the ways in which computers will affect his life. Informed people will make judgements largely favorable to the continuing, rapid growth of the computer market.

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Published bi-monthly, **Personal Computing** will provide educational articles on basic computer jargon, computer architecture, and computer programming. These articles will be written in easy to understand language for the beginner and they will serve as a reference for people already knowledgeable in the field.

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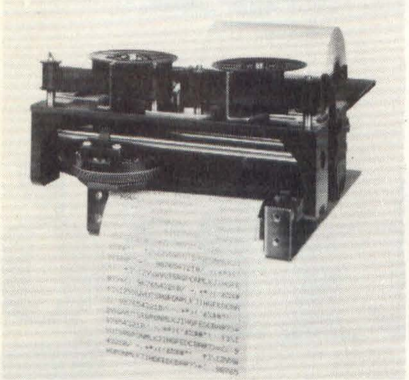
# product news

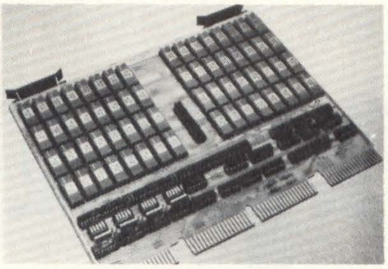
## 7 x 5 MATRIX PRINTER OUTPUTS 120 CHAR./SEC

Using a 7 x 5 miniature needle matrix, this printer outputs 8, 10 or twelve 0.110" H x 0.08" W char./in at 120 char./sec. DMTP-6 series generates a 64 ASCII character set in 36,- 66- or 96-column widths on 3 7/16", 6" or 8 1/2" W roll or fanfold paper. Mounting on a 5¼" rack, the printer suits the bit-parallel, character-serial RS 232C or 20 mA current-loop input transmissions typical of telephone, data and microprocessor coupling. Price: $200. Practical Automation, Inc., Trap Falls Rd., Shelton, CT 06484. (203) 929-5381 **Circle 208**



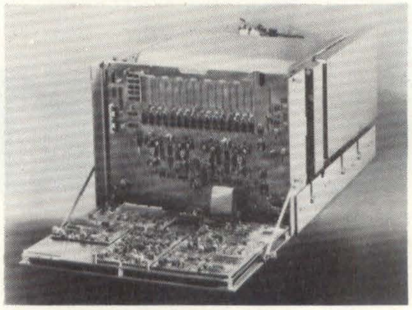
## 16K SEMI MEMORY SERVES ALL PDP-11s

Hardware- and software-compatible with all DEC PDP-11s, this add-in memory stores 16K sixteen-bit words on a 10.44" x 8.44" board that plugs into the mini's DD-11 controller slot. Model WE-VM11-16's 4K x 1 NMOS static RAMs consume 3.6A @ +5 Vdc, derived from the computer power supply through the controller slot. The semiconductor memory accesses in 500 ns and cycles in 850 ns. You can set each of the board's independent 4K memory's starting address location anywhere in the 0-124K range on the mini's bus. Price: $1650. WE Computer Extension Systems, 17311 El Camino Real, Houston, TX 77058. (713) 488-8830 **Circle 229**



## 4.2 MBYTE DRUM MEMORY STANDS 12¼" HIGH

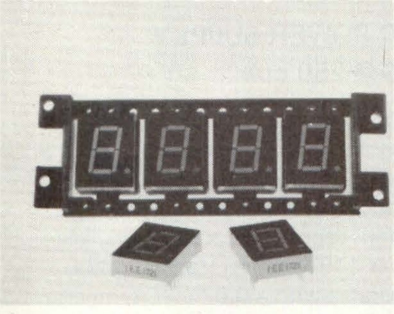
This 4.2-Mbyte, fixed-head drum memory accesses in 8.5 ms and occupies 12¼" of vertical space in a 19" rack. Model 4016 comes with controllers for most 12- and 16-bit



minicomputers and interfaces for DDC, GI and Amcomp head-per-track memories. All the memory's circuit elements lie outside the head and media enclosure, and you can access all interface electronics at the unit's front. Standard features include speed detection and non-contact start/stop heads. Price: $6070 for 1 Mbyte. Vermont Research Corp., Precision Park, N. Springfield, VT 05150. (802) 886-2256
**Circle 239**

## 0.6"-HIGH LEDS OUTPUT 250 $\mu$CD/SEGMENT

These 0.6" H red-character LEDs output 250 $\mu$cd/segment @ 20mA/ 1.6$V_f$. Spaced 0.6" apart on 14-pin DIPs, Series 1721 permits 25-30 ft viewing at up to 160° and displays



the numerals 0 through 9 plus ±1 with right-hand decimal point. With their common anode design, the GaAsP-emitting displays provide dual dies for each segment. Price: $1.15 each in 10,000s. Industrial Electronic Engineers, Inc., 7740 Lemona Ave., Van Nuys, CA 91405. (213) 787-0311 **Circle 240**

## SWITCHING POWER SUPPLY OUTPUTS 750 W

This two-output switching power supply produces up to 750 W and operates with up to 80% efficiency. Model MMX-420 outputs 5 V @ 150 A, and either 2 V @ 24 A, 5 V @ 24 A, 12 V @ 20A, 15 V @ 20 A, 18 V @ 16 A or 24 V @ 10 A. Measuring 5.1" H x 7" W x 12.75" D, the power supply provides 1% peak-to-peak or 50-mV peak-to-peak ripple and noise, 0.4% line regulation and 0.4% load regulation @ 100% change. With 0°C-70°C operating range, the unit responds in 200 $\mu$s to 1% after 25% load change. Price: $685 each for 10-24. LH Research, Inc., 1821 Langley Ave., Irvine, CA 92714. (714) 546-5279 **Circle 237**

## CRT/KEYBOARD DISPLAY FOR INDUSTRIAL JOBS

For machine control, data collection/transmission and other factory-floor applications, this CRT terminal operates with a minicomputer or plugs into telephone lines for remote entry or dial-up applications. Model R-301 fits in a standard 19" computer rack or other machine cabinetry, can withstand dirty industrial environments and requires no cooling fans at ambient temperatures up to 50°C. To facilitate "hunt-and-peck" data entry, the display provides a standard keyboard configuration with slightly closer-than-normal spacing. Displaying up to sixteen 32-character lines, the CRT terminal incorporates a standard RS 232 interface and operates at EIA rates ranging from 110 to 9600 baud. Price: $1890. Informer, Inc., 8332 Osage Ave., Los Angeles, CA 90045. (213) 649-2030 **Circle 238**

# product news

## $4 PLUG-IN TRANSFORMER POWERS MODEMS AND MICROS

For modems, data communications equipment, microprocessors and other LSI circuitry, this plug-in transformer provides four output terminals. Three of the terminals provide a center-tapped 24-V output for deriving positive and negative dc voltages while the fourth terminal serves as a power ground. Other features include an interwinding capacitance of under 30 pF, non-concentric primary and secondary windings and grounded core. An integral thermal circuit breaker with automatic reset protects against short-circuits. Price: $4 in OEM quantities. Ault Inc., 1600 H Freeway Blvd., Minneapolis, MN 55430. (612) 560-9300

**Circle 253**

## ENCAPSULATED POWER SUPPLY OUTPUTS 5 VDC @ 250 mA

This encapsulated power supply outputs 5 Vdc @ 250 mA with a 0.05% line and 0.1% load regulation. Model S-5-250 operates over the -25 to 71°C range with ±1% output-voltage accuracy, 1-mV noise and ripple, and 50-mΩ output impedance at 20 kHz. The single-output supply requires 115 Vac ±10 Vac, 50-440 Hz input voltage and operates with a 0.02%/°C temperature coefficient and 15-μs transient response. It also provides 6.5-Vdc overvoltage protection and short-circuit protection. Price: $32 for 1-9. Cardon Corp., 80 Broad St., Boston, MA 02110. (617) 357-5898

**Circle 254**

## BUSINESS PLOTTER OUTPUTS 667 STEPS/SEC

Plotting 667 steps/sec in 0.004" steps, Model 600-500 converts printouts and statistics into page-sized bar charts, trend graphs, pie charts, demand calendars or other graphic forms. Measuring 19" x 15" x 7½", the 30-lb. business plotter accepts 9"W sprocketed, fan-fold or roll paper and generates less than 65 dB noise. Broomall Industries, Inc., 700 Abbott Dr., Broomall, PA 19008. (215) 328-1040

**Circle 259**

## 8K 22-PIN RAM ACCESSES IN 150 NS

Model 7008's 150-ns access time suits it to high-speed, high-density applications. An 8K x 1 RAM in a 22-pin, dual in-line package, the unit uses a 22-pin 4K RAM's unused 16th pin as an extra address. The memory dissipates the same amount of power as a 22-pin 4K RAM. Prices in 100s: $21 for the 150-ns version, $18 for the 200-ns version. Advanced Memory Systems, Inc., 1275 Hammerwood Ave., Sunnyvale, CA 94086. (408) 734-4330 **Circle 257**

### INTERACTIVE IMAGE PROCESSOR DISPLAYS 19" COLOR PICTURES

This interactive image processing system combines an LSI-11 microcomputer, an image processor, a refresh memory with optional CCD or 16K RAM and the manufacturer's applications software, and either hooks up to a mainframe or operates in a stand-alone mode. Vision One displays image data on a 19" color CRT. For random access applications, the refresh memory holds 512 kbits to 12 Mbits, access time equals 1.5 $\mu$s/byte, and access modes include horizontal by rows, vertical by columns, single pixel (8 bits) and any rectangular shape (x by y). Minimum transfer time for a complete image (512 x 512 x 8) measures 100 ms. Specifications for line sequential access applications include a 1024-kbit to 24-Mbit capacity, standard access time of 8.3 ms (average)/line and optional fast access of 500 $\mu$s (average)/line. Standard access mode is horizontal by rows, and vertical by column is optional. Minimum transfer time for a complete image equals 150 ms. The unit's arithmetic and logical processor uses the PDP-11/35, 40 instruction set and directly addresses 32K 16-bit words. Software provides more than 20 major functions including the ability to read selected images from source data and display it; to select display options; and to search mag tape for the selected image. Price: $25,000 to $80,000. Comtal Corp., 169 North Halstead St., Pasadena, CA 91107 (213) 793-2134 **Circle 258**

### DUAL INTERFACE ADAPTOR GIVES STORAGE UNITS 2 PORTS

Designed to operate with the manufacturer's cartridge storage systems, this interface adaptor converts storage systems into two-port devices. DIA-100 consists of one PC card that plugs directly into storage systems and requires no power supplies. The adaptor interface also permits two or more redundant processor systems to share a common data base (even though the CPUs represent different designs) and communicate with each other in a non-forcing mode. CPUs accommodated by the system include the PDP-11, LSI-11, Nova series, Intel 8080 and Rolm computers. Price: $695. North Atlantic Industries, Inc., Qantex Div., 200 Terminal Dr., Plainview, NY 11803. (516) 681-8600 **Circle 255**

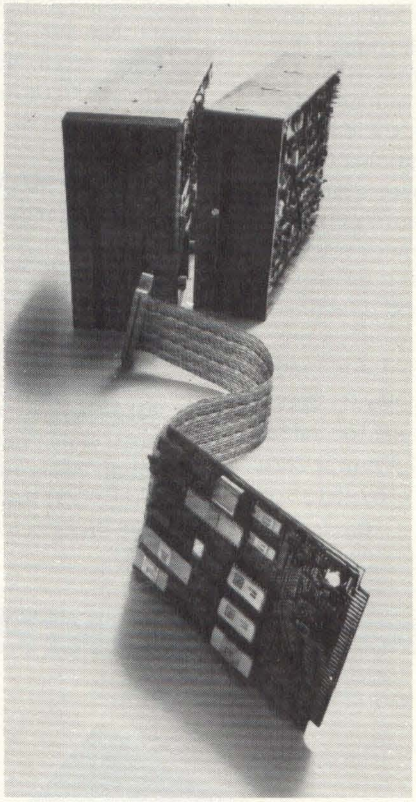
### OPEN-FRAME POWER SUPPLY PROVIDES OVERVOLTAGE PROTECTION

With built-in overvoltage protection, this open-frame power supply accepts 105-125 Vac and 210-250 Vac inputs over the 47-63 Hz operating range. The OEM III series also offers 10% derating output for 50 Hz operation, ±0.15% maximum load regulation for 100% load changes. You can adjust the supply's output voltages, which range from 5 to 24 Vdc, by the ±5% minimum. Prices range from $24.95 to $82. Alpha Power, Inc., 9020 Eton Ave., Canoga Park, CA 91304. (213) 998-9873 **Circle 256**

# product news

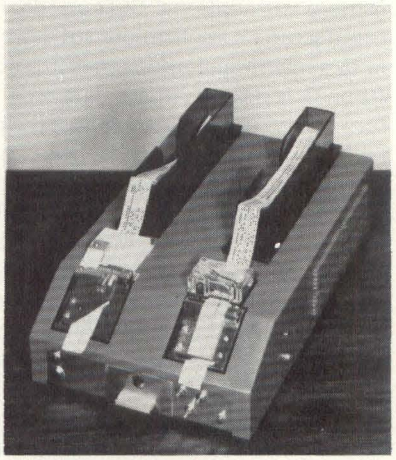
## FLOPPY CONTROLLER SUBS FOR CPU

Serving most major microcomputers, this intelligent diskette drive controller communicates by file name and assumes the housekeeping duties usually performed by a CPU. Built around an Intel 8080 microprocessor, Model 1070 transfers data from a CPU or an RS 232 interface and incorporates internal operating software that controls all file management functions, including IBM 3740 formatting and initializing. Controller commands include seek, write, read, delete and initialize. Price: $1195 in singles. PerSci, Inc., 4087 Glencoe Ave., Marina Del Rey, CA 90291. (213) 821-5545 **Circle 205**



## PAPER-TAPE READER/PUNCH DUPLICATES 50 CHAR./SEC

For code duplication or conversion, this paper tape reader/punch interfaces with communications equipment like IBM Selectric systems, terminals, mini- and microcomputer systems, programmable calculators, CRT displays, optical-character scanners and floppy-disk units. Though basically an ASCII system, the unit can convert incoming data to Baudot, BCD, EBCDIC, TTS or other codes at 50 char./sec. An optional editing capability lets the unit read or skip tape by character, word, line or paragraph. Price: $4250. Tycom Systems Corp., 26 Just Rd., Fairfield, NJ 07006. (201) 227-4141 **Circle 207**



## 9600-BPS MODEM MEETS CCITT V.29

This 9600-bps modem meets the requirements for CCITT Recommendation V. 29 and incorporates an eye-pattern generator, a four-channel multiplexer, a four-channel buffered multiplexer, remote loopback, 75-bps secondary channel, elastic store buffer and built-in modem-sharing unit. Additional features include circuit-quality monitoring capability, which displays line-disturbing phenomena and qualitatively indicates line amplitude and delay distortion. LSI 96/V.29 operates over M58 or M102 lines, offers four operating modes and incorporates a front-panel, 5-digit display. Price: $9350 in singles. Codex Corp., 15 Riverdale Ave., Newton, MA 02195. (617) 969-0600 **Circle 204**

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# product news

## CODE CONVERTER BUFFERS 500 WORDS

Model 975 converts ASCII to Baudot or Baudot to ASCII at 110, 300, 1200 or 2400 baud. For 10-cps ASCII or 100-word/min Baudot terminals, the code converter and data formatter buffers up to 500 words in each direction during speed changes. An alarm indicates a full buffer. The microprocessor controlled unit stores communications-line data until it receives a carriage return or until 20 sec elapse between characters; it then converts the data to the required code and transmits it to the terminal at the switch-selected speed. Price: $1795. Data Terminal Corp. of Maryland, 11878 Coakley Circle, Rockville, MD 20852. (301) 881-7655

**Circle 263**

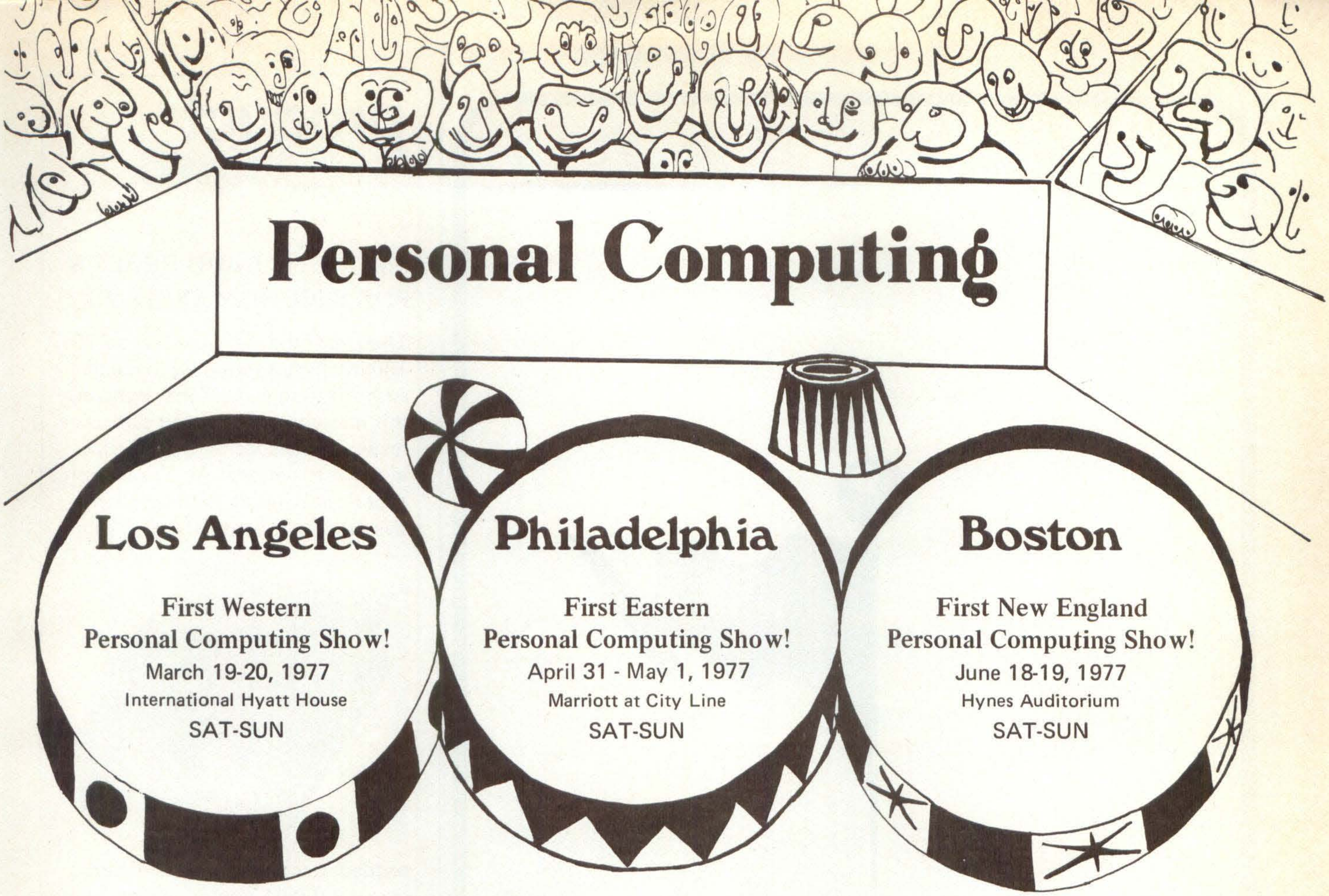
## BAR CODE PRINTER SUITS INVENTORY CONTROL

For industrial inventory control, libraries, hospitals and similar applications, this two-hammer printer generates an alphanumeric bar code plus an independent line of descriptive text. Suitable for random, batch, or sequential label runs, the serial impact printer uses ASCII I/0 and provides a typewriter-like keyboard. An optional RS 232 interface lets you control the printer by computer, intelligent terminal or peripheral input device. An integral PROM-based microprocessor accommodates options or custom items. Model 8130 prints on continuous roll self-adhesive paper labels or perforated tags and uses a dry carbon ribbon. Price: $7487. Interface Mechanisms, 5503 - 232nd St. SW, Mountlake Terrace, WA 98043. (206) 774-3511

**Circle 264**

## FLOPPY DISK SYSTEM INCORPORATES 6-LINE DISPLAY

A single data entry station, this floppy disk system suits decentralized applications in individual departments and permits operation by nontechnical personnel. Storing 500K bytes, Transdata 9210 incorporates a six-line display with program controlled operator guidance, two floppy disk drives, microprocessor, data converter and local peripheral floppy disk I/0. You can also connect a matrix printer, if necessary. Each floppy disk accepts 1898 data records of up to 128 characters each. Siemens AG, Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany. (09131) 7-3394



# Personal Computing

## Los Angeles

First Western
Personal Computing Show!
March 19-20, 1977
International Hyatt House
SAT-SUN

## Philadelphia

First Eastern
Personal Computing Show!
April 31 - May 1, 1977
Marriott at City Line
SAT-SUN

## Boston

First New England
Personal Computing Show!
June 18-19, 1977
Hynes Auditorium
SAT-SUN

# Greatest Computer Shows Ever!

**Personal Computing** magazine is proud to announce that it is sponsoring the first series of regional Personal Computing Shows.

Beginning with the *Western Personal Computing Show* in Los Angeles, and followed by the *Eastern Personal Computing Show* in Philadelphia and the *New England Personal Computing Show* in Boston, **Personal Computing** magazine intends to make everyone aware of low-cost computing.

Other shows are now being planned for the South, Southwest, Canada, and Europe!

Already, invitations have been sent to all the manufacturers in the personal computing field, computer stores, computer clubs and well-known computer experts.

Special areas of the exhibition halls will be set aside for Personal Computing in Education, in the Home, in HAM Radio, and in Small Businesses. These are all first for a computer show.

Seminars and special presentations include: Computer Synthesized Music, HAM Applications, Trends in Microcomputers, Mass Storage Systems, Lemonade Computer Service Companies, The Kitchen Computer, Computers on the Farm, The Small Business System, Software for Fun and Practical Applications, Computer Club Organization, Standards for the Hobbyists, Computer Art, The House Robot, Computer Crime, Software Protection and Future Computing.

In addition, *special tutorial workshops* will cover all aspects of computer hardware, programming in both machine language and higher-level language and applications. Workshops are designed for both beginners and advanced students in the art of personal computing.

We anticipate 150 different exhibits and crowds of up to 10,000 people at each of these shows. Arrangements for the shows are being handled by a professional management company to ensure that everything runs smoothly.

**Cost of Registration:**
At the door:
$10 per show (two days)
$ 6 per One Day Pass
Special Pre-Registration Rates:
$ 7.50 per show (two days)
$ 4.00 per One Day Pass

Note: Show tickets and one day passes entitle you to attend all seminars, workshops, exhibits and other events.

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Yes, I would like to take advantage of your special, pre-registration rates. I plan to attend the following regional Personal Computing Show(s):

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|---|---|---|
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| ☐ Show (two days) | ☐ Show (two days) | ☐ Show (two days) |
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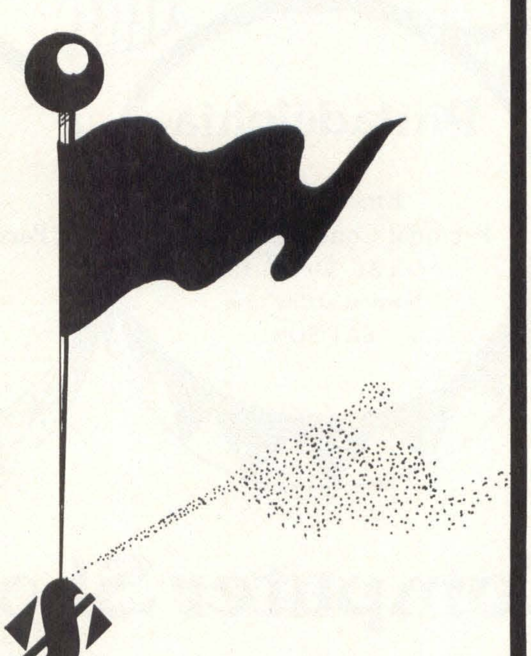
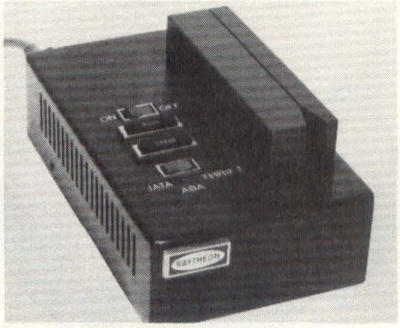


# product news

## MAGNETIC CARD READER FOR SECURITY SYSTEMS

Used with the manufacturer's PTS-100 intelligent terminals in credit authorization and security-control, this microprocessor based card reader can decode magnetic stripes in the International Air Travel Assn., American Banking Assn. and tentative ANSI standard data tracks embedded in most major credit cards. Model 6150-01 displays a customer's credit card number, card-expiration date and name on the PTS-100 screen with authorization and billing data. You can also enter coded security data in a non-display mode. Measuring 5" x 8½" x 4" and weighing 5 lbs., the reader operates on 115 Vac and provides a 20 W output. Price: $750. Raytheon Data Systems, 1415 Boston-Providence Turnpike, Norwood, MA 02062. (617) 862-6600 **Circle 252**



## CASSETTE RECORDER FOR TERMINALS, MINIS

For program loading, data collection, automatic send/receive and paper-tape replacement, this cassette recorder suits terminals, modems, couplers, minicomputers and data acquisition systems. Model 815 operates at 110 and 300 baud, transmits in half- and full-duplex and stores up to 145,000 ASCII, 8-level characters on a Philips-type cassette. Weighing 6 lbs., the recorder provides two RS 232C interfaces and a 20 mA terminal interface. Price: $950, with OEM discounts available. Techtran Industries, Inc., 580 Jefferson Rd., Rochester, NY 14623. (716) 271-7953

**Circle 247**

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## Electro77

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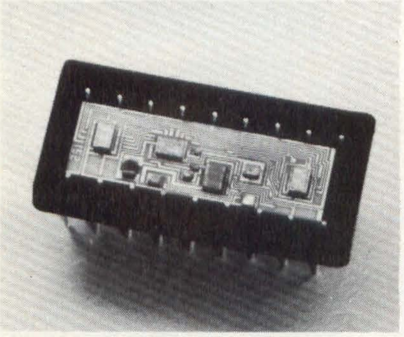
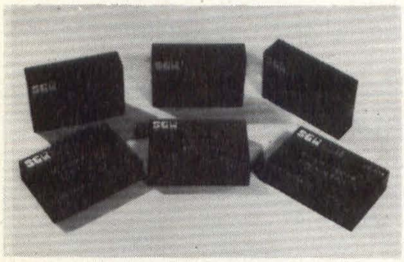
# product news

## 8-BIT D/A CONVERTER WITH BUILT-IN REGISTER



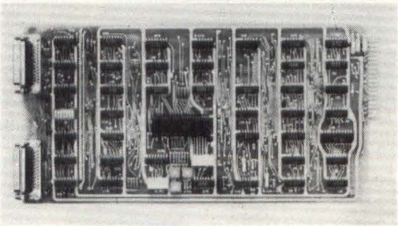
With a storage register built into its dual in-line package, this 8-bit D/A converter interfaces to micro- or minicomputer data buses. Model MN3020, which also incorporates an internal reference and output amplifier, provides laser-trimmed, thin-film resistors that eliminate external components or adjustments and ensure linearity within ± ½ LSB. User-selectable outputs range from 0 to -10V, -5 to +5V and -10 to +10V. With its TTL-compatible input circuitry, the converter offers accuracy to within 1 LSB and a 3-$\mu$s worst-case settling time. Price: $39 each for 1-24. Micro Networks Corp., 324 Clark St., Worcester, MA. (617) 852-5400 **Circle 248**

## POWER SUPPLIES SERVE I/O BOARDS



Providing single, dual and triple outputs in combinations to power analog I/O boards, microcomputers and microhybrid systems, Series 1000 provides dual-tracking output voltages, output-current limiting, over-voltage protection and +½% output voltage adjustments. The microhybrid power supply delivers full-rated 5V output over the 0-71°C ambient range and operates from 115V, 50-400 Hz with no derating. Other specifications include 1mV p-p output ripple, 0.1% maximum line and load regulation, 0.01%/°C temperature coefficient and 50% efficiency. Price: $149-$250 for 1-9. SGR Corp., Neponset Valley Industrial Park, P.O. Box 391, Canton, MA 02021. (617) 828-7773 **Circle 250**

## $500 ADAPTOR CARD SUBS FOR RS 366 INTERFACE



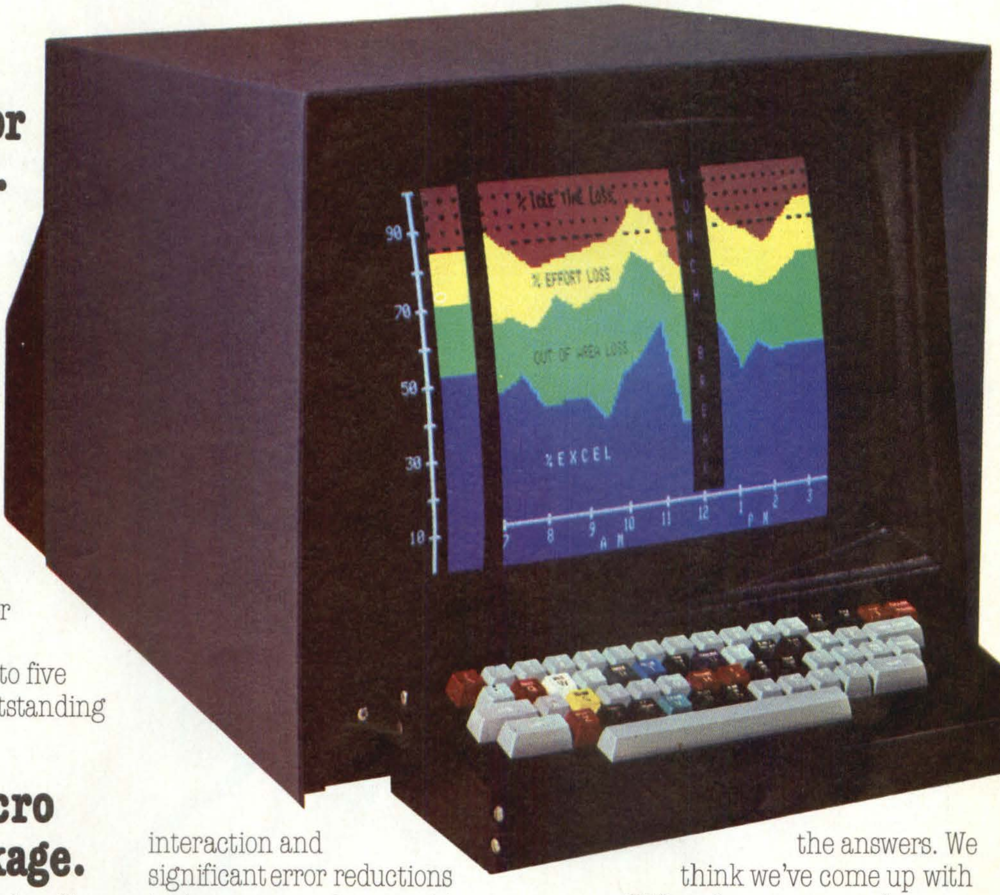
By allowing a computer to initiate and transmit dialing information through an RS 232 modem interface to a Bell or the manufacturer's 801-type automatic dialer, this adaptor card eliminates the sometimes unavailable and often expensive RS 366 dialer interface. Model VA831 incorporates a multiplexer that permits automatic calling control by not passing 801 interface signals — a capability that means you can place an automatic dialer at the distant end of a multiplexer link and access it through an RS 232 interface without hardware modifications. The adaptor card occupies one slot in the manufacturer's VA1616 sixteen-channel, multiple-data-set chassis. Price: $500. Vadic Corp., 505 E. Middlefield Rd., Mountain View, CA 94043. (415) 965-1620 **Circle 249**

## READ-AFTER-WRITE HEAD FOR 3M DRIVES

For 3M-type data cartridges in acquisition systems, telephone PBX controllers, point-of-sale equipment, communication systems, shipboard computers and other small central processors, this read-after-write cartridge tape head accepts NRZI or phase encoded data at 5 to 90 ips. Model 24C-02P outputs 10 mV @ 3200 fci and 30 ips with at least 55% resolution for 3200/1600 fci. Information Magnetics Corp., 5743 Thornwood Dr., Goleta, CA 93017. (805) 964-6828 **Circle 251**

# The Intecolor® 8001

## It's an 8-Color Intelligent CRT for $1995.* Or a Micro Computer for an additional $1495. The choice is yours.



### A $1995 8-Color CRT. Complete.

When we say complete, we mean complete. The **Intecolor** 8001 has 8080 CPU, 4K RAM Refresh, Selectable Baud Rate to 9600, Keyboard, RS232 I/O, and ASCII Character Set. All in one package. It's a complete stand-alone system which features our unique **Intecolor** 8001 NINE SECTOR CONVERGENCE SYSTEM for minimum set-up time and exceptional stability. Three to five minutes is all it takes for outstanding color registration.

### The $1495 Micro Computer Package.

You just give us the word and we'll convert the **Intecolor** 8001 into a stand-alone micro computer with BASIC, Roll, Insert/Delete, Additional 8K RAM Work Space, Graphics Mode with 160X192 Elements, Background Color, Lower Case ASCII, 48 Line X 80 Characters/Line, and 2X Character Height. Plus additional features which make your **Intecolor** personal computer the best buy in the industry.

### Which System Is Right For You?

The **Intecolor** 8001 CRT is a smart, inexpensive way to upgrade the CRT's in your present system from black and white to color. And color has definite sales advantages. Like more efficient man-machine interaction and significant error reductions in data entry and recognition. The **Intecolor** 8001 CRT can also be used or marketed as a complete stand-alone micro computer system with computation or control capabilities. It might even replace your whole system!

Whatever your needs, market or application — Process Control, Medical, Credit Checking, Order Entry, Financial Analysis, Research and Development, or for your own personal computer — you won't find a more usable terminal, color or black and white.

### Write Or Call For More Information

We know you're going to have some more questions, and we've got the answers. We think we've come up with a CRT and computer package that's hard to beat. And one thing for sure. The **Intecolor** 8001 is by far your best buy today in a color CRT micro computer or intelligent terminal. Make us prove it to you with a demonstration by one of our authorized representatives. Or call us direct and talk to an applications engineer.

ISC

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CIRCLE 50

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# bystanders win

# THE MINI-MICRO SHOOTOUT

Pity the poor minicomputer. Just as it caught the fancy of design engineers as an efficient, effective way to apply real-time computer power to a new range of processing and control applications, a new gun came cruising into town.

Some observers say a shootout is inevitable, because the new gun – the microcomputer – grows more competent and competitive with each design generation. The micro is smaller, younger and lighter on its pins than the veteran mini, and it exhibits the mystique of semiconductor development – Who knows how much logic will someday fit on a tiny piece of silicon?

If a showdown occurs, the event will have more than a little irony. The minicomputer originally rose to power because it could perform dedicated computer functions at a lower cost than its larger parents – the same is true of today's micro. Later, mini vendors developed increasingly sophisticated software to take advantage of the mini's increasingly sophisticated hardware – again, the same is true of today's microcomputer. And all during the minicomputer's childhood, pundits theorized about the inevitable shootout between mini and parent computer, just as they do about today's micro and mini. But minis and mainframes can't replace each other, and although skirmishes occur between them every now and then, they have managed to coexist by staking out distinct territories – large computers do their best work in batch environments, while minis lead in distributed processing.

There's a direct analogy, then, between the mini/mainframe wars of yesterday and the micro/mini confrontation of today. The modern micro can flex its silicon and boast of infinite design potential, and it may suit some minicomputer-like tasks perfectly, but it can't match the minicomputer's processing power, memory capacity, and peripheral and software variety. And in case micro watchers haven't noticed, the mini keeps getting stronger, faster and more cost-effective.

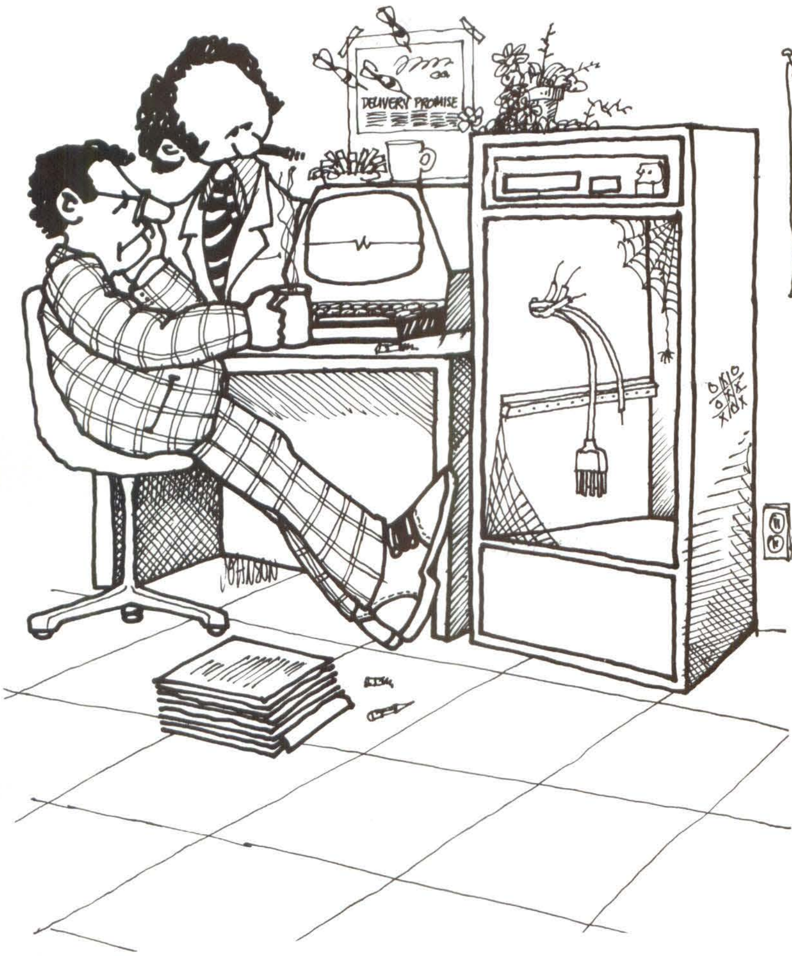
So although some experts look for huge memories, multiple disks and numerous high-level languages on future microcomputer systems, micros just don't suit applications that require these features – but minis do. Minis excel in applications that require large amounts of main memory to handle large programs or complex operating systems. They can capture high-speed data and perform sophisticated analysis in microseconds, and they can supervise and maintain hierarchical networks of dedicated microcomputers. Meanwhile, micros excel at tasks that require lower computing power, small programs and limited I/O – dedicated operations.

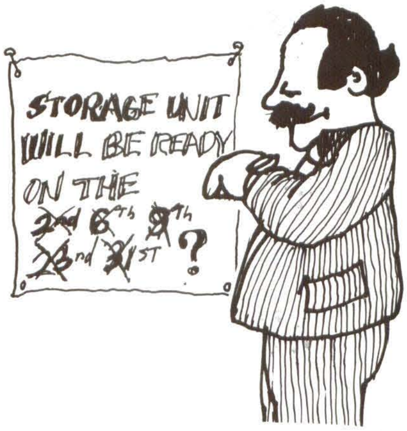
So who wins the shootout? That's easy – you do. For you can now span two technologies to find the optimum price and performance specs for your application. And if you need both technologies to serve a sophisticated application, all the better.

Edward J. Zander

**Ed Zander** *is MicroNova marketing product manager at Data General Corp., Southboro, MA. We will be pleased to provide space for opposing views.*

# Still Waiting For DEC?





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**30 days ARO**

CIRCLE 2

# WE'D LIKE YOU TO MEET MARY

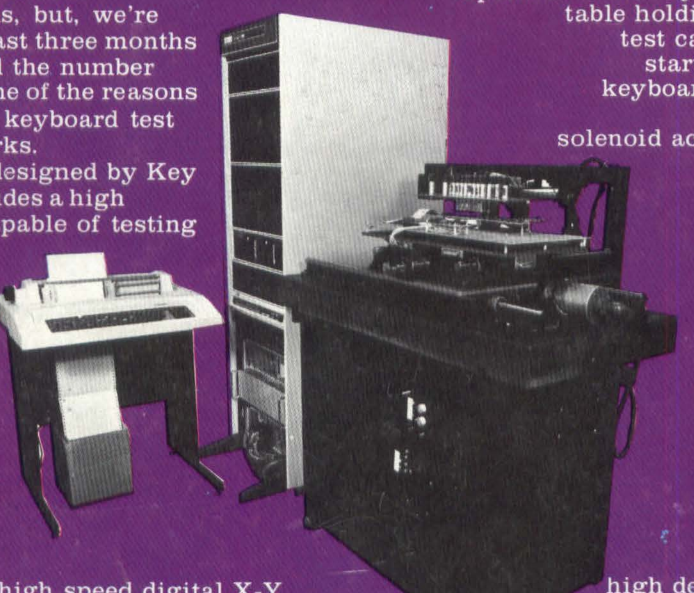
## she works in customer returns.

Of course we're exaggerating a trifle, our plant isn't completely void of customer returned boards, but, we're working on it! Over the past three months we've drastically reduced the number of returned boards, and one of the reasons for this is our automatic keyboard test system. This is how it works.

The Keyboard Tester, designed by Key Tronic Corporation, provides a high speed, flexible system capable of testing many different types of board configuations at rates up to 120 keyboards per hour.

The system also has the versatility of testing both reed and capacitance keyboards and is used for both initial and final test operations.

The test system is comprised of a DEC PDP-11 minicomputer, a high speed digital X-Y table, and a DECWRITER printer.



Test programs are entered into the minicomputer via a tape cassette. The minicomputer designates the X-Y table co-ordinates for positioning of the solenoid actuators over the appropriate key switches and test sequencing.

The following types of keyboard outputs are also verified by the minicomputer, which uses a precision 10mHz clock as a reference.

a. Output codes
b. Voltage levels
c. Contact bounce duration
d. Strobe pulse width
e. Strobe pulse trains
f. Repeat rate
g. Repeat delay

The basic keyboard test sequence is comprised of the operator manually loading each keyboard onto the X-Y table holding fixture, plugging in the keyboard test cable, and actuating the minicomputer start command. The X-Y table moves the keyboard in the appropriate positions under the "mechanical fingers" (battery of solenoid actuators) which are also programmed by the minicomputer for the correct sequencing.

All key switches are tested in both primary and shift/function modes.

Upon completion of the test a printout by the DECWRITER indicates keyboard type and serial number and test status. Keyboards passing the test are so noted by a "No Failure" printout, while the individual failure modes (up to maximum of 10) are listed if the keyboard has failed the acceptance test.

The repeatability and accuracy of the automatic test system brings a high degree of confidence to the Key Tronic test program and additional such systems are scheduled on-line in the near future.

This is just one of the programs we're implementing to put our Quality Assurance department out of business. If you would like further information on our keyboard products, write us.

*High speed film captures a "mechanical finger" as it makes contact with board.*

**key tronic**

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CIRCLE 3