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DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS SEPTEMBER 1985

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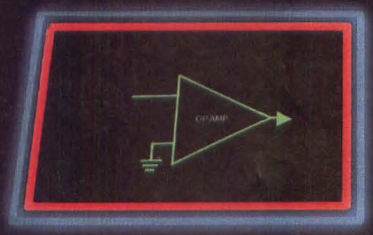
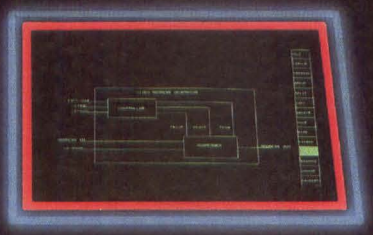
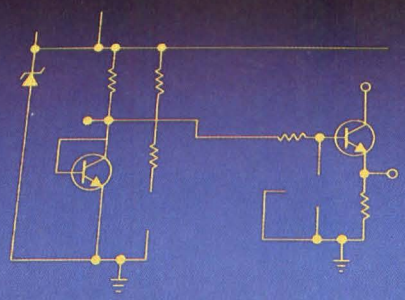
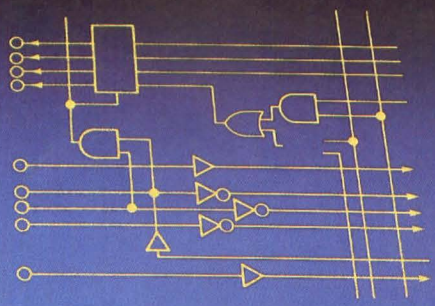
PARALLEL INTERFACES BOOST WINCHESTER ACCESS TIME

ELECTRONIC IMAGING '85 SHOW PREVIEW









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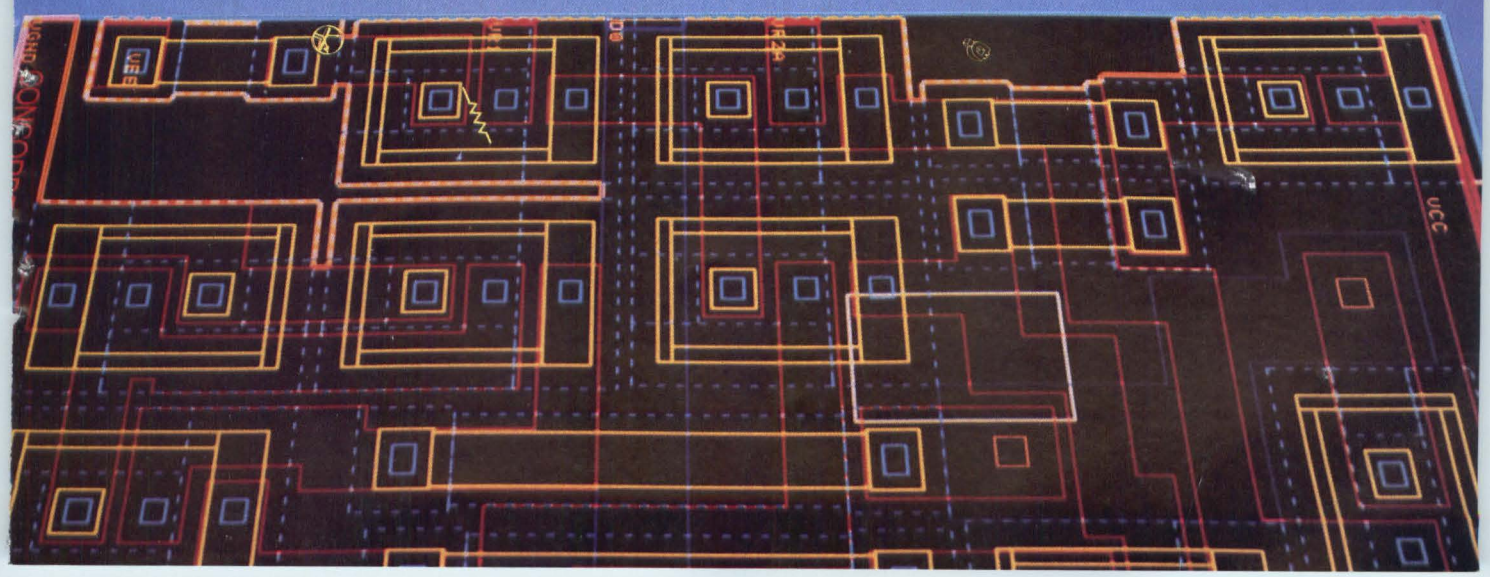

Gould. . . Innovation and Quality in Image Processing

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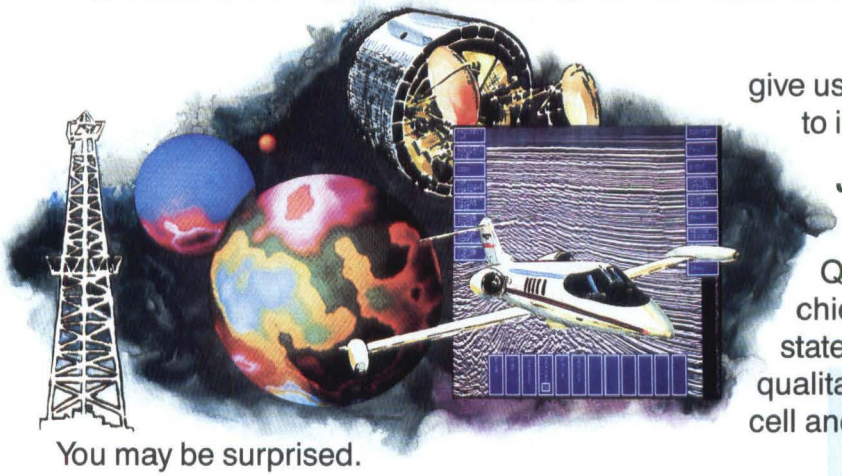

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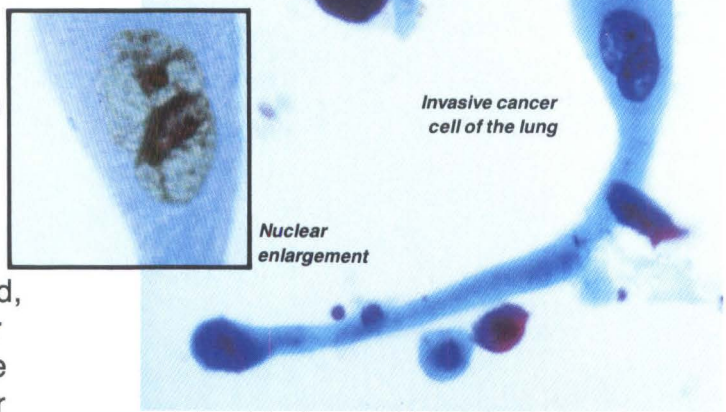

Invasive cancer cell of the lung

Nuclear enlargement

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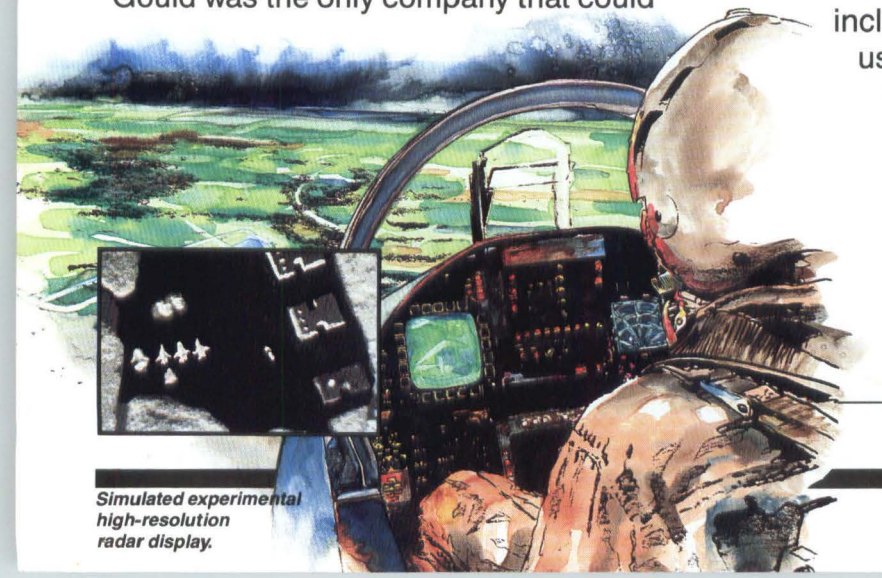

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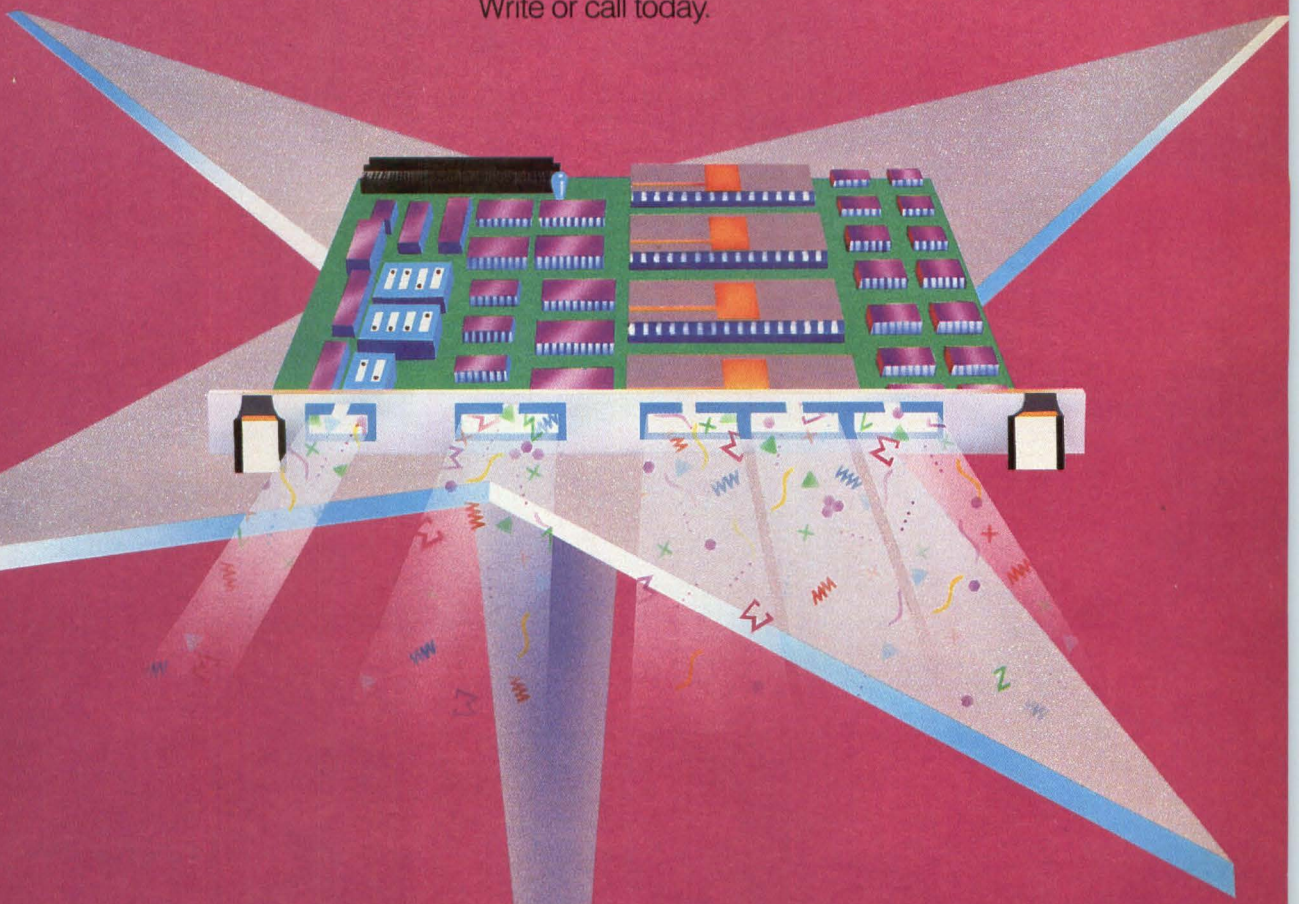

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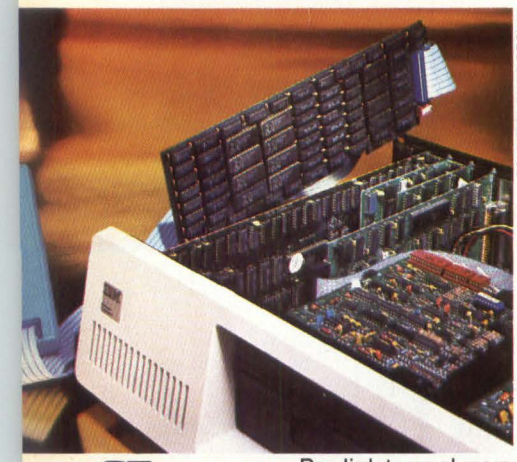

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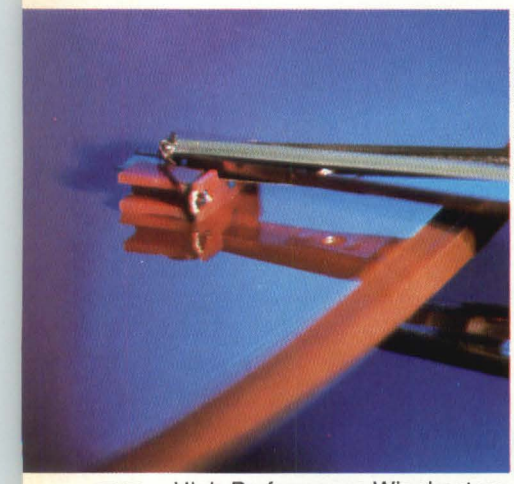

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ON THE COVER

Silicon compilers dramatically reduce the time and training necessary to design complex, application-specific integrated circuits. The Concorde VLSI Compiler from Seattle Silicon offers a broad choice of digital and analog compilers to automate the design of CMOS chips. The compiler is currently integrated into CAE software on workstations from Valid Logic Systems, Tektronix CAE Systems and Mentor Graphics.

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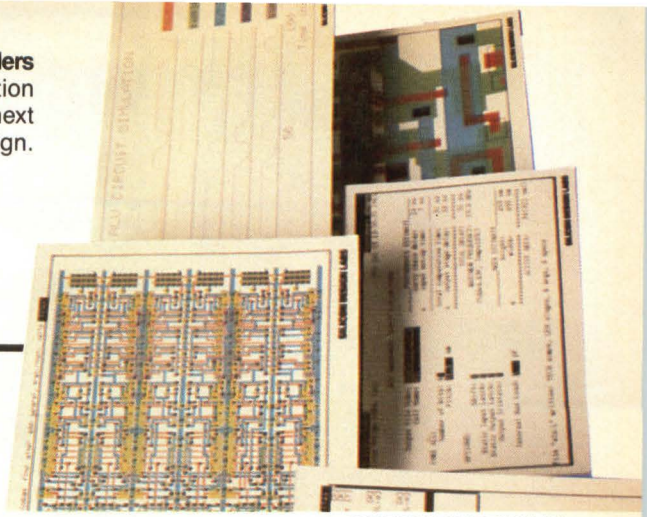
Silicon compilation ushers in the next era in system design.



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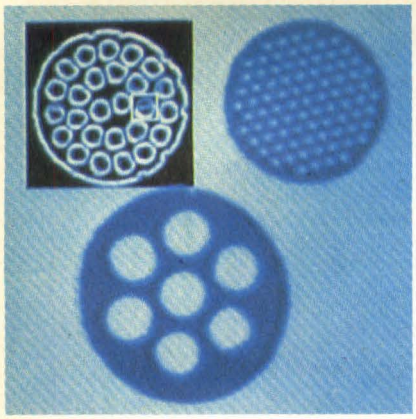

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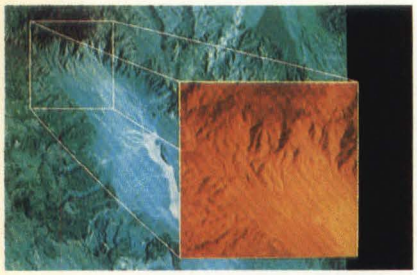

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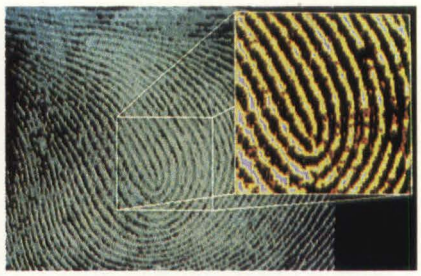

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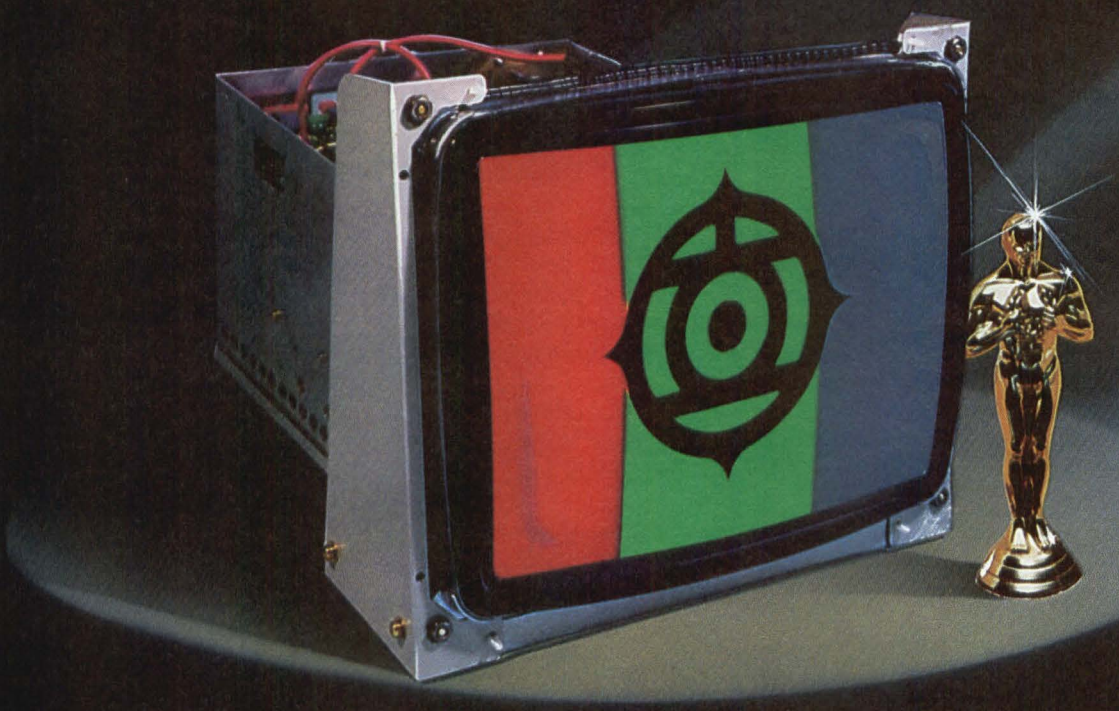

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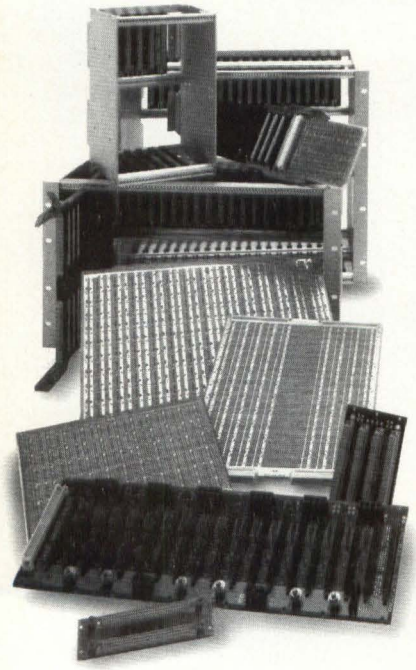

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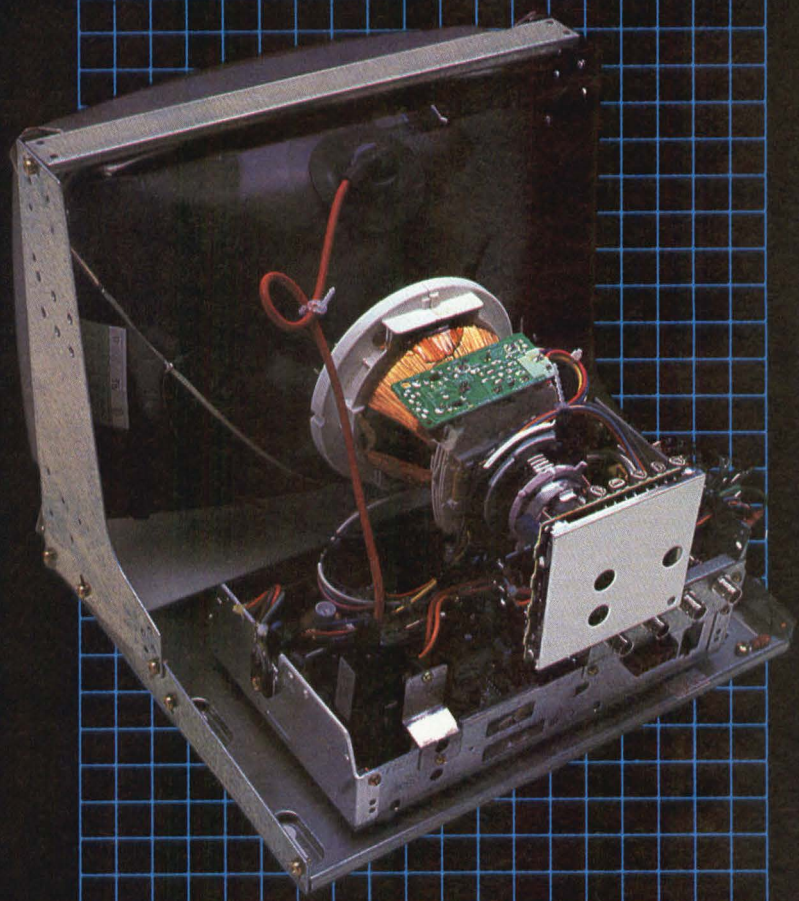

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Circle 18 on Reader Inquiry Card

EDITOR'S COMMENT

Open Systems Close Up

On the surface, the concept of an open systems architecture would appear to be the panacea that all board level manufacturers and systems integrators are looking for. But what exactly is an open systems architecture? My definition includes the following two points. First, the specifications for building to a particular system should be publically available. Second, no license fee or royalties should be imposed on either manufacturers or end users to build a product to meet that specification.

Those companies that do not support these two points are committing marketing suicide by alienating both third party vendors who may actually widen a customer base anyway and, worse still, the OEM who may perceive that legal wrangling and letters from faceless lawyers are something that they would rather not deal with – opting for alternative solutions instead.

Open systems architectures are a good idea. They should, theoretically, allow a vendor to mix and match a variety of products to configure a system. Unfortunately, some open systems architectures may be only partially open. Or, they may start out open, then close. For example, take Pro-Log's new multimaster scheme for the STD bus. A good idea, no doubt, but the scheme is patented and, at the time of writing, no other vendor can build product to the scheme. Good for Pro-Log. Bad for the systems integrator.

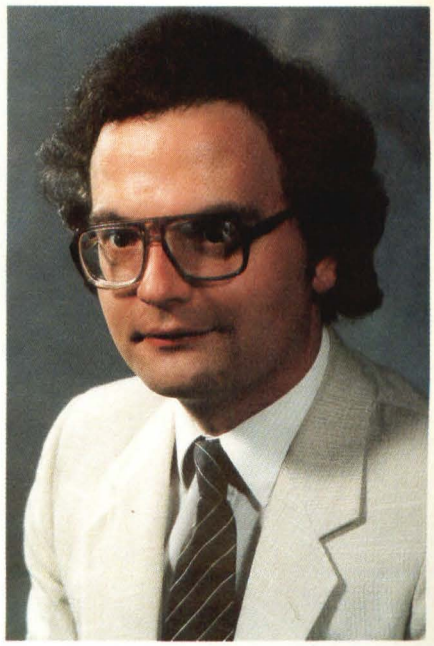
Intel also has created unnecessary paperwork by charging a one time fee for builders of Multibus I and II boards in order to protect their patent rights. It might be a good mechanism to find out where their competition is, but what other good does it do?

Digital Equipment Corp. recently entered the fray with a law suit against Emulex of Costa Mesa, CA. DEC seeks an injunction against further marketing, manufacturing, selling and distribution of Emulex's disk controllers that use DEC's MSCP (mass storage control protocol) or that plug into DEC's SBI, CMI, Unibus and Q-Bus for its VAX, MicroVAX and PDP-11 computer systems. DEC claims that Emulex has infringed its patents and seeks treble damages.

In an open reply, Emulex chairman Fred Cox said that he believes that the industry will be chagrined by DEC's intent to limit its competition in the add-on market by obtaining patents apparently intended for this specific purpose. I agree with Mr. Cox. Depriving OEMs of the opportunity to enhance their DEC systems with more cost-effective peripherals offered by other vendors is not in the best interests of anyone in the industry – even DEC.

Meanwhile, over in the VME camp, vendors and customers are having no such problems with license fees, letters from corporate lawyers or lawsuits. As a result, the VME vendors may be integrating all the way to the bank with a lot of their competitor's business. One can only wish them the best of luck.

– Dave Wilson, Executive Editor



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Circle 9

HOTLINE

GaAs DEVICES MOVE TO LSI-LEVELS OF INTEGRATION The last quarter of this year will find Gigabit Logic (Newbury Park, CA) introducing a 1 Kbit GaAs SRAM, and Vitesse Electronics (Camarillo, CA) announcing GaAs multipliers and A/D flash converters; Triquint Semiconductor (Beaverton, OR) plans to introduce a 500-2000 gate array family.

APOLLO OFFERS OPEN-ARCHITECTURE COMMUNICATIONS PROGRAM Apollo Computer (Chelmsford, MA) has announced a set of communications links to extend the DOMAIN system's resource sharing architecture. The links, available for IBM's SNA computers, IBM's personal computers (and hardware compatibles) and DEC's VAX computers, allow transparent access to data and resources from a DOMAIN system.

LARGE AREA, FLEXIBLE, 0.015" THICK LCD A flexible plastic LCD material has been introduced by Polaroid (Cambridge, MA). The lightweight, 0.015" thick material can be custom produced up to 16" wide and in virtually unlimited length for computer displays.

20,000-GATE GATE ARRAY IN 1.25-MICRON GEOMETRY Honeywell's Digital Product Center (Colorado Springs, CO) will market a 20,000-gate CMOS gate array. The part was developed by ETA Systems for the ETA-10 supercomputer, which is planned for delivery in 1986.

ALTERNATE SOURCE AGREEMENTS FOR ASICS Motorola (Phoenix, AZ) and NCR (Dayton, OH) have signed a co-development and alternate source agreement that includes both CMOS gate arrays and standard cells.

SIX-CHIP IMAGING SYSTEM Sharp Corp. (Paramus, NJ) has announced a complete color imaging system based on five ICs. Based on a 386 × 488 CCD, the four support chips include a color signal separator, clock generators and clock drivers which provide direct RGB output. Sony (Paramus, NJ) will also debut a single-chip color CCD sensor soon.

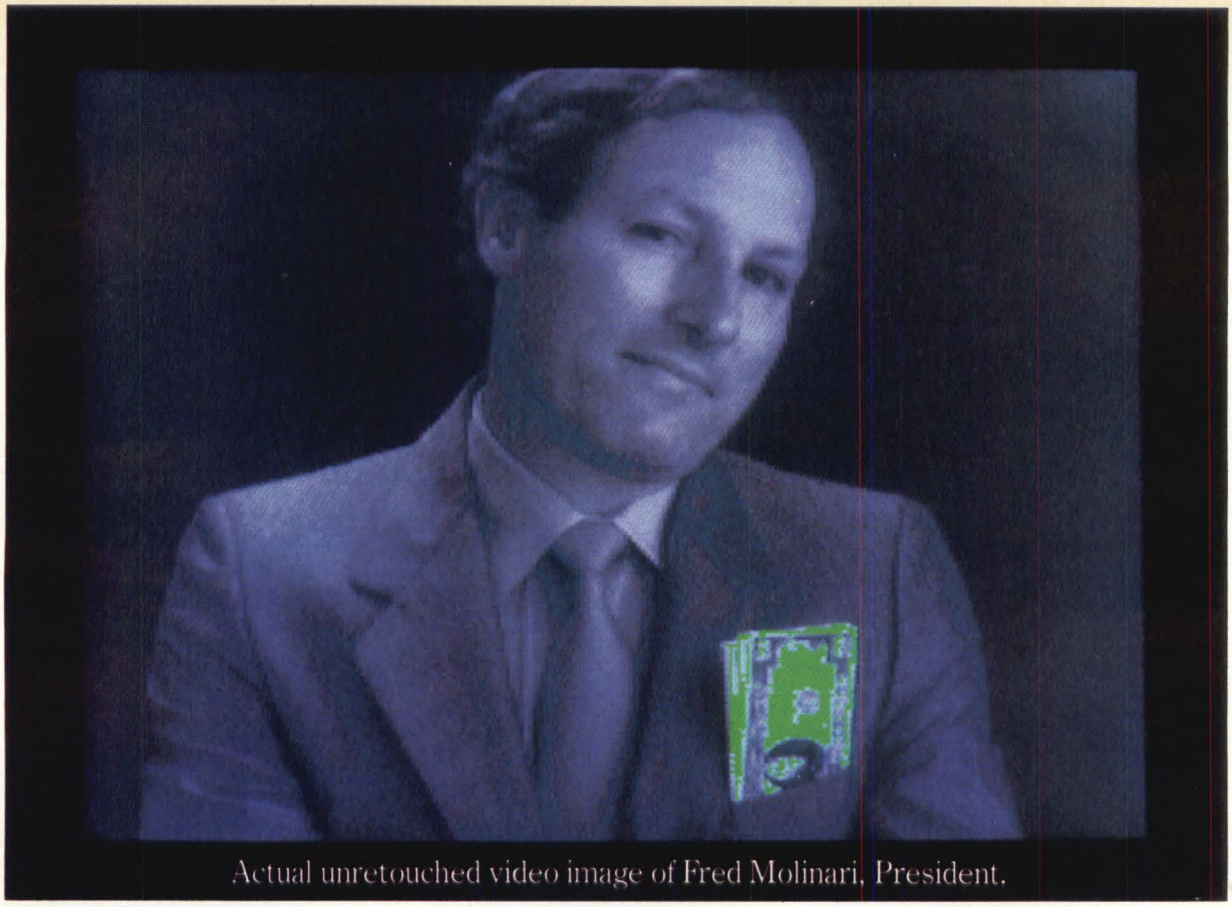
HIGH FIDELITY FRAME GRABBER Shintron (Cambridge, MA) has introduced a color 768 × 505 × 8-bit frame grabber for image processing. Features include a high 13.5 MHz sampling rate, in-built timebase correction and, later this year, a MicroVAX II interface.

DEVELOPMENT TOOLS FOR THE 80C51 Oki Semiconductor (Sunnyvale, CA) has introduced a set of development tools for the 80C51 intended for use on personal computers. A VAX version of the set will be available soon.

COLOR PALETTE AND CONVERTERS COMBINE ON VIDEO DAC Brooktree (San Diego, CA) has announced a triple 4-bit D/A converter with on-board RAM that operates at a conversion speed of 125 MHz. The BT451 features an on-board multiplexer.

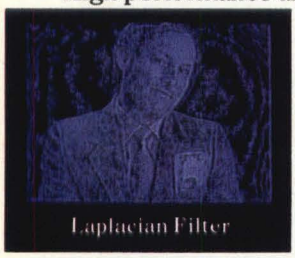
WORLD'S LARGEST CCD AREA ARRAY IMAGER Tektronix (Beaverton, OR) has announced a 2048 × 2048 CCD area array designated the TK2048M with a dark current of 10 nA/cm^2 and a charge transfer efficiency of greater than 0.99999.

HARDWARE FOR INTERACTIVE WARPING Megavision (Santa Barbara, CA) has demonstrated the PDF processor for interactive warping on the 1024XM. The processor is an optional feature to the 1024 image processor which allows global and recursive computations to be offloaded from the 1024.



Actual unretouched video image of Fred Molinari, President.

"It's easy to spot the difference between our IBM PC™-based frame grabber and the others."



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Frame Grab	1/30 (1/25) second per field
LUT's	8, 64 × 8 input; 4, 256 × 12 output
D/A Output	64 colors × 64 intensities, R-G-B; 64 grey levels, monochrome
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TECHNOLOGY TRENDS

SOFTWARE

CAE Techniques Migrate To Software Engineering

The Rational R1000 software development system, in addition to a specialized processor, has a full-screen, multiple window terminal.

Computer-aided engineering has become standard for hardware designers. But software engineers, for the most part, have not been able to take advantage of CAE. Conventional tools no longer provide effective support for developing complex systems, and the conventional process has become inefficient due to time-to-market concerns.

Several companies have manufactured software development systems, combining editors, compilers and debuggers into one package. For example, Promod's (Laguna Hills, CA) ProMod engineering environment operates independently of the target system and language. The environment aids structural analysis, system and program design by automatically creating program modules and checking high-level interface descriptions. It prepares documentation and cross-referenced lists for data, data types and functions.

The Language Development System (LANDS) from Tektronix (Beaverton, OR), part of the company's CAE 2000 workstation product family, is a development toolkit for Pascal and C and popular target processors. A Language Directed Editor intercepts syntax errors in the source file during the editing session. Software configuration and interfaces for prototype hardware, such as low-level code generation and hardware initialization reset, are handled by a tool called the Integration Control System. The LANDS debugger allows debug operations to be performed at the compiler source level during real-time program execution.

Both of these software development systems are available for the VAX; ProMod runs on the IBM PC/XT/AT as well. According to Dave Sharon, marketing manager for software design tools at Tektronix, maintaining a consistent approach, as well as consistent components for such tools, is important. Supporting multiple languages on systems such as LANDS will result not only in higher productivity and reliability, but also in a faster language learning curve for programmers.

On the other hand, Rational (Mountain View, CA) has introduced the Rational R1000 Development System, a special-purpose hardware and software system designed to develop and to maintain large, complex software written in Ada. The R1000 is a universal host with a validated DOD compiler. Like the interactive support provided by CAD/CAM systems for circuit design, the R1000 offers incremental checking of software code for error detection and correction.

A core editor, through an Ada-like command language, invokes compilers, debuggers and object editors similar to an operating system. The difference is that the core editor can automatically sense and switch modes within the next layer of tools. The object editors provide semantic and syntactic checking, correction and completion.

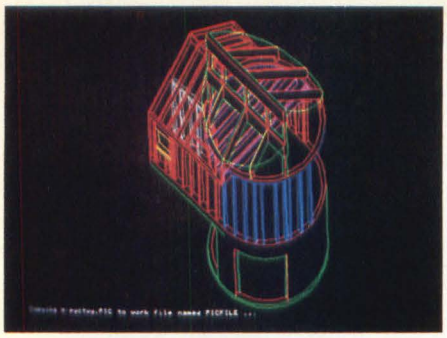
A database directory containing information such as variables and data types of previously compiled programs enables incremental compilation on the R1000. This facility makes recompilation of entire programs after new edits unnecessary; only new additions to the program must be compiled during debugging. Changing pointers in the directory allows new program patches to be spliced into the old program. A software management tool tracks subsystem interfaces for later linkage.

Rational's design of the R1000 processor is a departure from other software development tools. The processor's architecture is optimized for traversing large data structures, making the machine essentially a specialized Ada engine. A 128-bit CPU splits control words so that type checking and addition are performed simultaneously instead of serially. Virtual memory is handled at the microcode and hardware level, rather than by the operating system. In addition, data packing and unpacking also occurs at the hardware level.

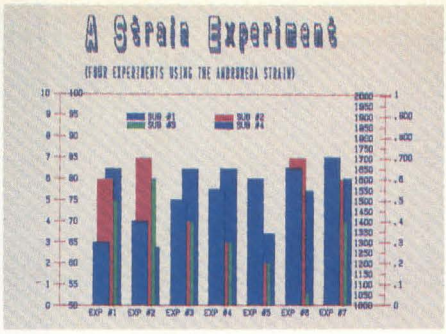
The success of the Rational system may depend more on whether companies using Ada believe that the $595,000 list price is worth the added hardware and software features. With the refinement of Ada compilers for computers such as the VAX, companies may decide to forego the expense of the R1000 in favor of previously invested work, time and money on those computers. In addition, back-end compilers to tailor code to different microprocessors do not yet exist for the system.

The availability of the R1000 and software development tools such as ProMod and LANDS indicates that software engineers are finally able to take advantage of CAE to ease software development during complicated programming efforts. The built-in intelligence of these tools allows software developers to concentrate more on programming and less on paperwork.

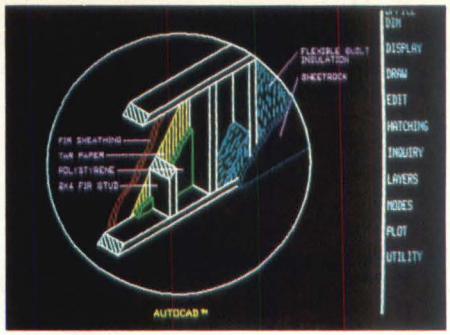
—Meng



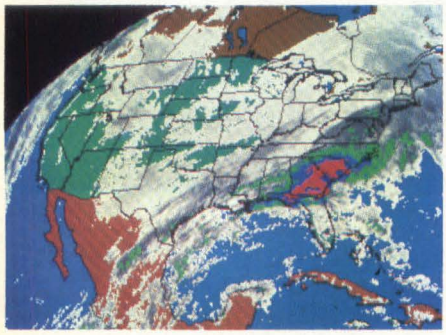
1. High Speed (MicroCAD Software)



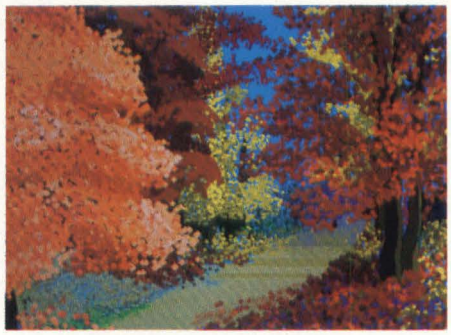
2. Dual Display Modes (Energraphics Software)



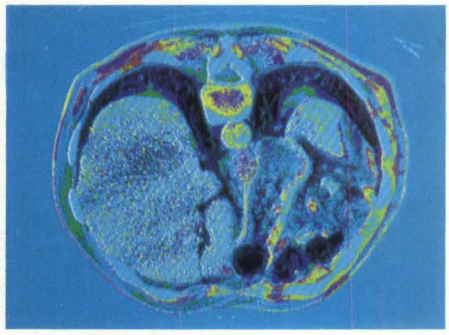
3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

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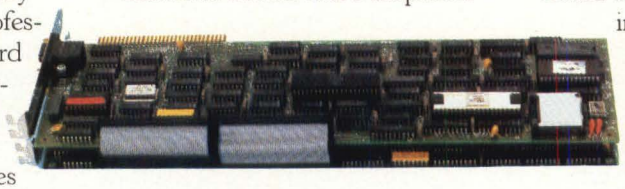

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Circle 7

SYSTEMS

UNIX And 68020 Team Up On CPU Designs

A number of vendors now offer 68020-based CPU boards. In many designs, manufacturers have used Motorola's MMB for page memory management until the 68851 single-chip MMU becomes available (Photo courtesy Dual Systems).

Since its introduction, the Motorola 68020 has been one of the more widely accepted 32-bit microprocessors. Recently, a range of boards and systems have been introduced. Motorola was the first, announcing its VME131 board. Since then, it has been joined by Charles River Data Systems (Framingham, MA) with its Universe 32 system and associated 68020 Versabus board, Dual Systems (Berkeley, CA) with its VMPU-32 module, Ironics (Ithaca, NY) with the IV-3201 VME CPU board and the Multibus-based MAP-2000 from Matrox (Quebec, Canada). Force Computer (Los Gatos, CA), has a 68020 board that will be announced next month.

Most companies have taken full advantage of the VLSI devices offered by Motorola. In addition to the 68020, many manufacturers have elected to use the MMB memory management unit (until the 68851 is in full production) and the 68881 floating point unit. In most cases, vendors offer 12 MHz versions of the 68020. Although some claim to offer 16 MHz devices, the faster part is not yet widely available and supplies of products based on it are limited.

Even though some vendors are distinguishing their product by the processor's raw clock speed (16 MHz vs. 12 MHz), system software, operating systems and compilers actually dictate system performance. UNIX, for example, is already offered by many vendors who support or plan to support it in the near future. Which version they choose and how their hardware supports the operating system is open to a number of different interpretations. AT&T's System V 2.2 enjoys a number of advantages over the earlier System V 2.0. The swapping-based memory manager has been replaced by a demand-paged memory manager. Paging allows fuller use of existing hardware by allowing execution of programs much larger than the main memory and gives a higher degree of multiprogramming.

Bucking the popular trend to use Motorola's MMB, Charles River Data Systems has elected to design its own segmented memory management unit rather than a demand-paged memory management unit. Its Universe 32 is currently supported by the company's own version of AT&T's System V, called UN/System V or UNOS, a UNIX-compatible real-time operating system kernel. In 1986 the company plans to offer an operating system to support demand-paged virtual memory management.

Similarly, Motorola (Tempe, AZ) whose VME CPU board includes the MMB will not have UNIX V 2.2 on a system product until the end of March 1986. However, its first UNIX port (a swapping port) will be released in two months.

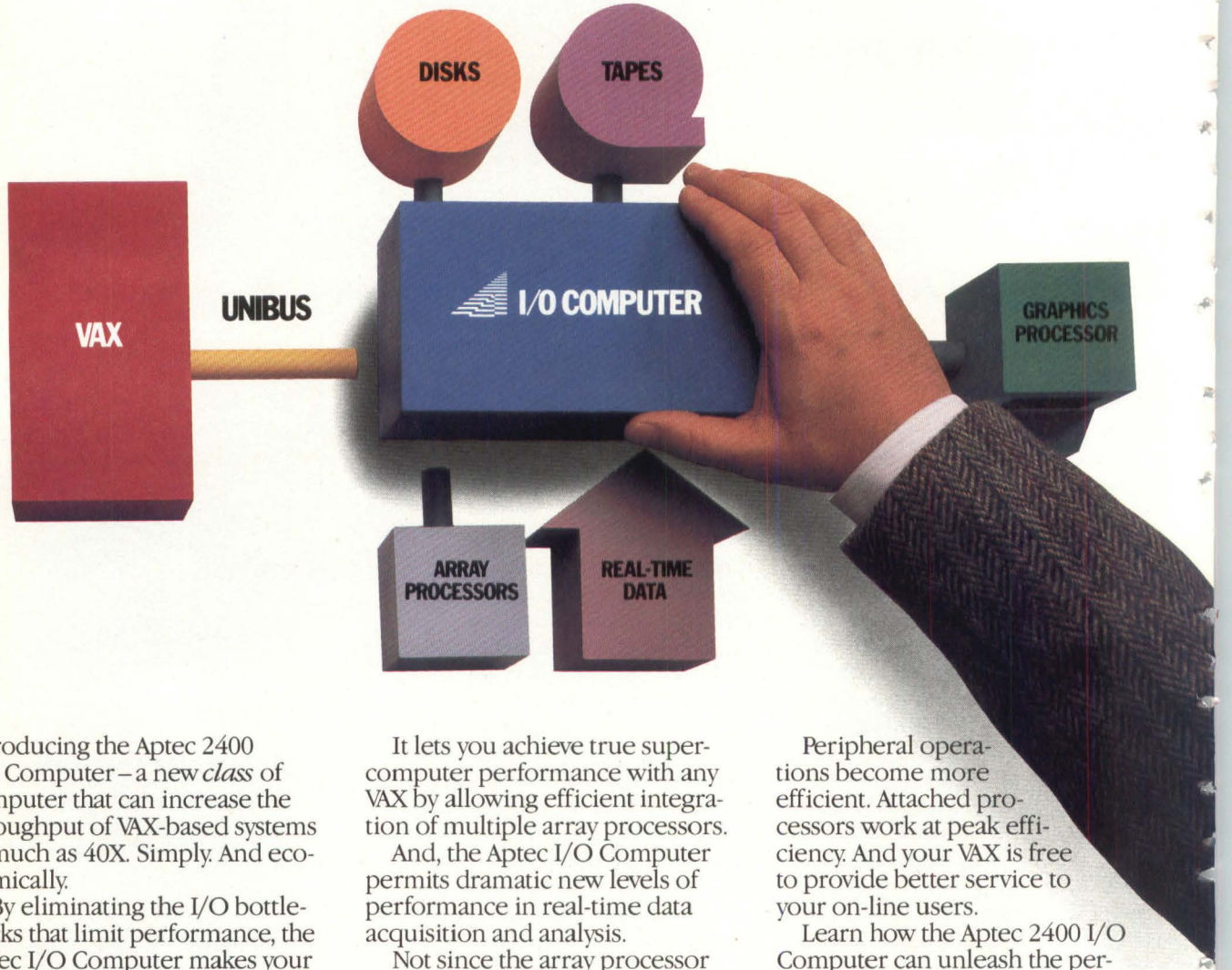
Dual Systems, whose plans also include UNIX V Version 2.2, is planning to commence full production of its VME line later this year. The new modules include a 68020 CPU board, a system controller/arbiter, a 2 Mbyte memory board, an I/O processor, a tape controller and an SMD disk controller.

Although the UNIX operating system is being ported to many of the newer 68020 designs, many applications have more typically demanded a real-time operating system like PDOS or OS/9 that does not have UNIX's overhead.

Clearly, those systems that do support UNIX (Version 2.2 or Berkeley 4.2) are targeted towards the development environment in which tools such as compilers demand larger memory sizes. Of the other 68020 systems that have been announced, Altos Computer Systems (San Jose, CA) claims its 3086 machine will support System V 2.2 starting this month. NCR (Dayton, OH) will also begin shipping its Tower 3232, which supports System V 2, in October. With all of this design activity surrounding the 68020, plenty of hardware is at last available. Software support; however, still appears to be somewhat lacking.

—D. Wilson

THE MOST SIGNIFICANT BREAKTHROUGH IN VAX SYSTEM PERFORMANCE SINCE THE ARRAY PROCESSOR.



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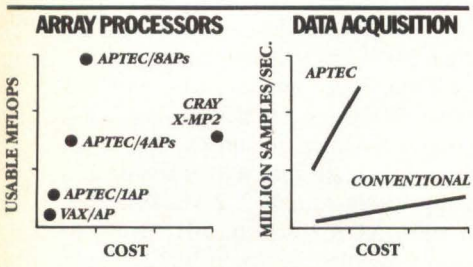

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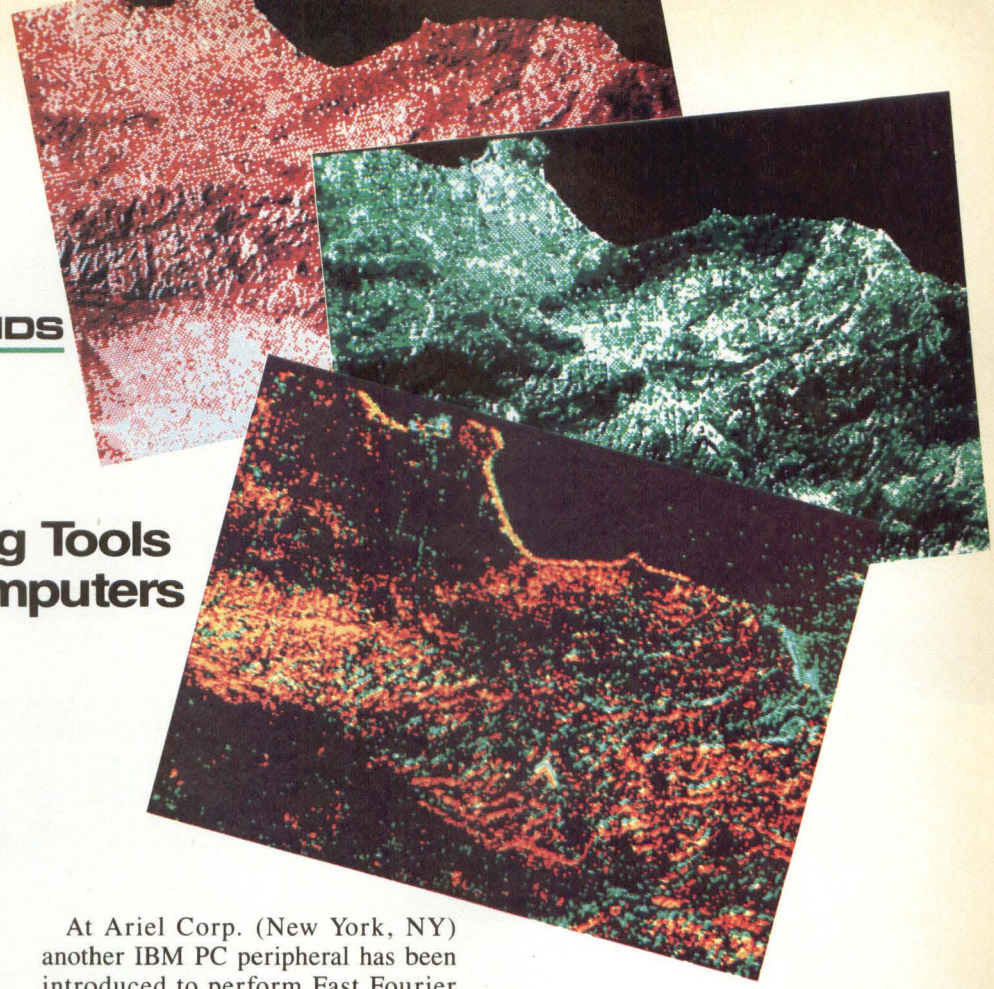
Circle 69 on Reader Inquiry Card

IMAGING

Image Processing Tools For Personal Computers



Infrared LANDSAT images of Los Angeles, illustrating a multiple thresholding operation assigning four colors to represent the 40 grey levels of data. The second image assigns green to the same data while the last image is a modified subtraction of the first two images to detail mountains, freeways and shallow water areas.

Decreasing costs of semiconductor memory coupled with advances in VLSI processors has led to a proliferation of imaging products. Many of these, based on the IBM and other personal computers, will be on display next month at the 1985 Electronic Imaging Conference and Exhibition (p. 50). Indeed, the market potential of such systems is leading both start-up and established imaging companies to introduce a greater variety of products in the area of image processing.

NCR Corp. (Fort Collins, CO) will introduce a development system for the company's Geometric Arithmetic Parallel Processor (GAPP) chip (*Electronic Imaging*, January 1985, p. 66). The GAPP PC development system is composed of two parts. The first is a hardware board compatible with the IBM PC I/O bus. It contains a 12×12 array of processor elements implemented with two GAPP devices. The second part is a software package which allows the user to program the GAPP array in a high-level language and to debug a program interactively.

The GAPP Simulator/Assembler package is composed of two utilities which operate under the UNIX or VAX/VMS operating systems. The first utility is the assembler, GAPASM, which translates GAPP instruction mnemonics and address specifications into binary object code suitable for downloading into a control state. The simulator, GAPSIM, is an interactive package that enables the user to execute GAPP programs and to view the contents of GAPP RAM and the state of the processor element registers in order to verify or debug the program.

At Ariel Corp. (New York, NY) another IBM PC peripheral has been introduced to perform Fast Fourier Transforms (FFTs). Plugging into expansion slots of the IBM PC/XT/AT, the PCFFT board performs FFTs using routines callable in either interpreted or compiled Basic, IBM Pascal or Fortran, Lattice C or Turbo Pascal. Operating on 16-bit integer data, the PCFFT transforms arrays of up to 2048 complex points in less than 20 msec. Other standard algorithms include forward and inverse FFTs, Hamming Windows and Power Spectral Density functions.

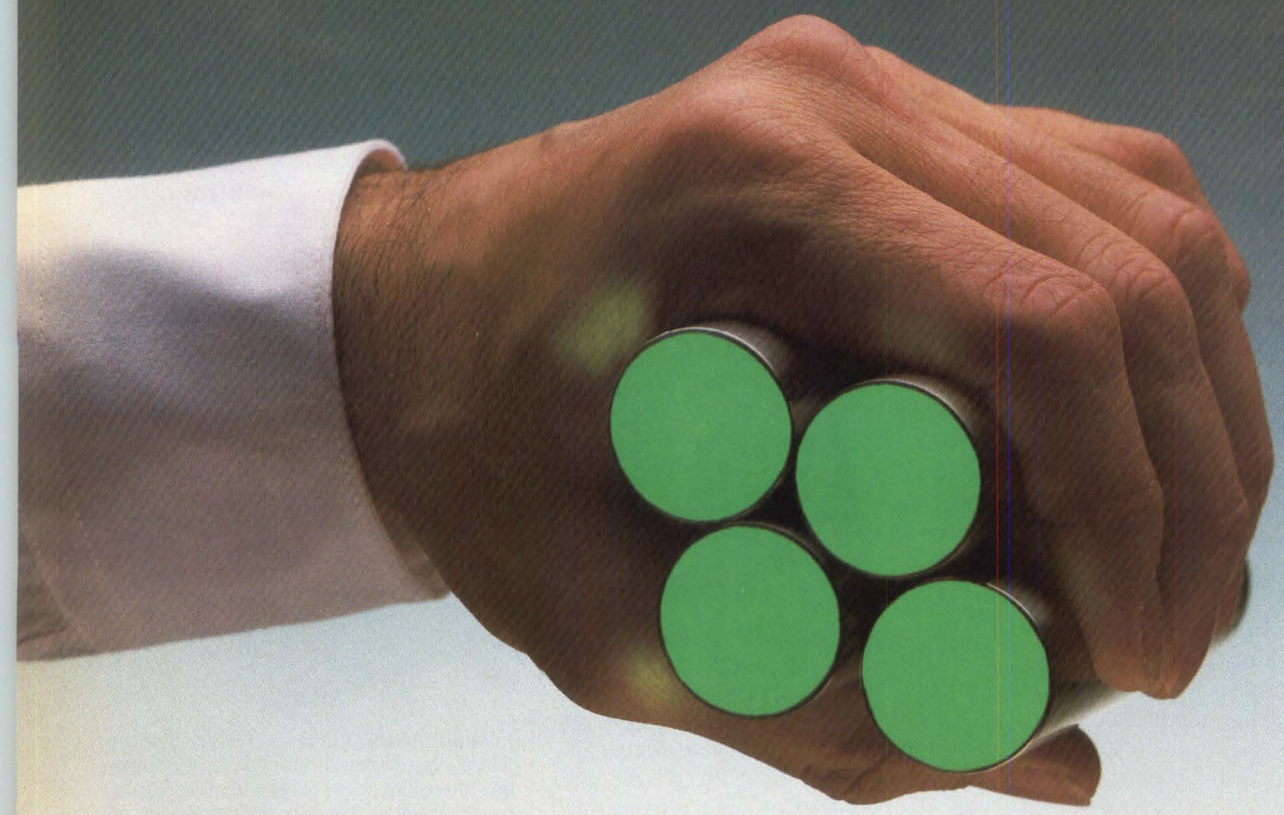
In the past, one of the limiting factors of such hardware has been the lack of software that can easily be used to generate image processing routines. Now, two companies have introduced packages which allow image processing functions to be generated rapidly.

The first, from Quantitative Technology Corp. (Beaverton, OR) is called the Math Advantage (p. 57) and consists of a set of computationally intensive routines which can be linked together to perform many scientific functions. Running on over 20 types of computers, the 180 routines can be called from the user's program in either C or Fortran. In a typical image processing environment, an edge enhancement program can be realized in approximately 20 lines of code as opposed to the 150-200 lines of Fortran that would normally be needed.

The Picture Database Management System, PICDMS III, from MIB Chock (Santa Monica, CA) can be used with PC-DOS systems for image processing and model building in either two or three dimensions. In a similar manner to the QTC system, the PICDMS gives the systems integrator a simplified way of defining a variety of operations on a picture database. Examples of possible operations include the detection of objects or edges of objects, contrast sharpening, pattern recognition and classification, histograms and statistical analysis. First shown at the 1985 SIGGRAPH show, the PICDMS II currently runs under CP/M on the Apple II+ as well as MS-DOS. The MS-DOS version can be supplied with either color or character graphics. PICDMS III requires an additional PL/1 compiler to implement the programs that it generates.

—A. Wilson

Our new CRTs are quite a handful.



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Circle 48

ISDN Promise Emerges With Silicon, Standards

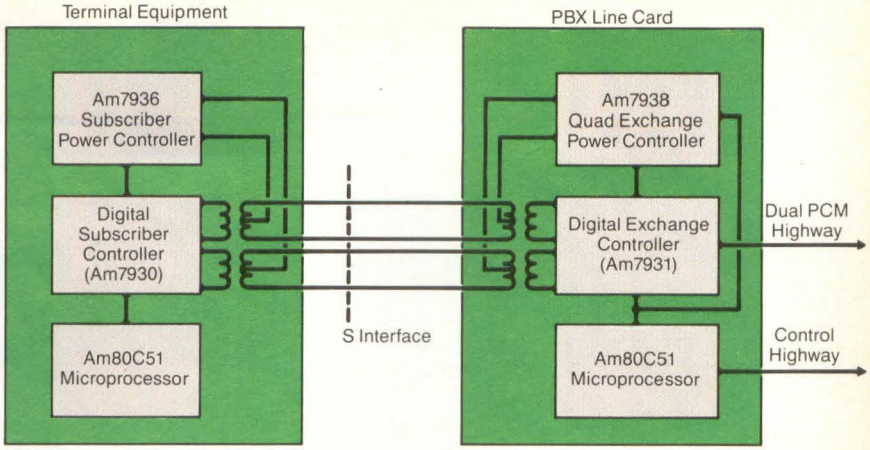

Figure 2: AMD's ISDN products are highly integrated, to allow easy implementation of both the terminal and the PBX equipment needed for ISDN compatibility. Power controllers are bipolar and subscriber and exchange controllers are CMOS.

An all-digital communication network may be some time off, but as international standards are set, some IC manufacturers are ready to produce products. Specifications for parts of the Integrated Services Digital Network (ISDN) are already firm, and others are well underway in the CCITT. The ISDN reference model encompasses three main interfaces defined in the reference model: S, T and U and secondary R and N interfaces, as shown in **Figure 1**.

At present, most of the silicon development is for the S interface to the terminal equipment and for the U interface to the network. Specifications for the U interface are not complete, but Mitel (Kanata, Ontario, Canada), Harris Semiconductor (Ft. Lauderdale, FL) and Intel (Santa Clara, CA) have U interface ICs in development. AMD (Sunnyvale, CA) and Intel are developing chips for the S interface.

The U interface description has been widely debated; whether to use a two-wire or a four-wire scheme is the main question. Four-wire cabling is used for the S interface, so having both S and U be four-wire would improve portability. And although most current telephone connections use 2-wire lines, cross talk is a problem. To solve that problem, an echo-cancellation technique will become standard. Intel, Harris and Mitel digital line interface transceiver ICs all employ echo-cancelling.

Data rates of up to 160 Kbits/sec can be achieved with the transceiver ICs; this is the Basic Rate for ISDN service. Channels within this bandwidth are two 64 Kbit/sec B channels for transmission and a D channel for control (commonly called 2B + D). A broadband Primary Service is also proposed in current ISDN documents for a T1 equivalent at 1.544 Mbits/sec. This would provide users 23 B channels and a 64 Kbit/sec D channel.

ICs for the S interface from both AMD and Intel are scheduled for introduction this year. Others like Motorola (Phoenix, AZ) will produce S chips in the future. S interfaces between the user equipment and the customer-premises switch, so these ICs will be used in PBX, terminal and digital telephone systems implementing ISDN. Up to eight terminal devices can be connected to one S interface; one which is used as master.

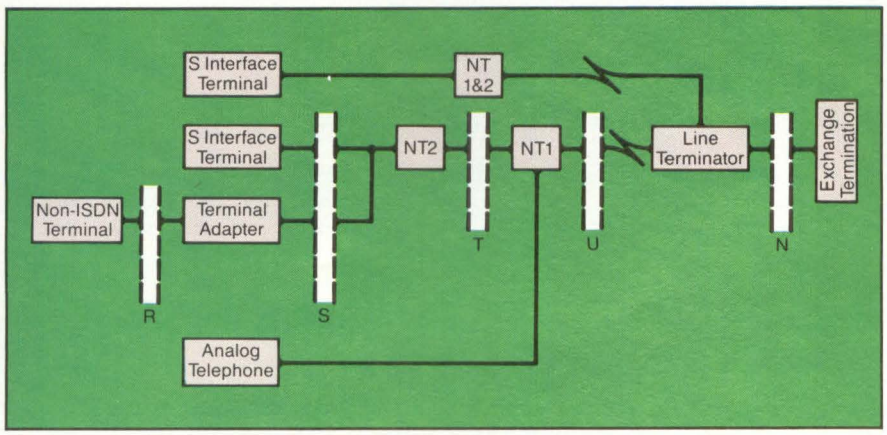

Figure 1: The ISDN scheme for transmitting a variety of video, data and voice services includes three major points of interface where silicon will aid development: S, T and U. The R is used only to interface non-ISDN terminals to a terminal adapter at the S interface and N is part of the network rather than the subscriber equipment.

The most highly integrated S interface proposed, AMD's Am79C30 digital subscriber controller includes codec, transceiver, tone generator and formatter functions. In most other ISDN implementations, three or four ICs will be used for these functions. A companion IC for the PBX line card, the Am79C31 digital exchange controller terminates the four-wire line from each 73C30. In addition to these CMOS parts, AMD is introducing bipolar power controllers for ISDN telephones (Am7936) and exchanges (Am7938). These four ICs, the 79C30 and 7936 on the terminal or phone side, the 79C31 and 7938 on the PBX side and a microprocessor (Intel 80C51 is suggested) on each side (**Figure 2**) can implement a basic S interface.

Intel ISDN ICs will be designated the 29C53 for the four-wire S interface and the 29C55 for two-wire ISDN U circuits. High-voltage power circuits are not available with Intel's technology, however. Two Intel products already in production, the 29C51 programmable feature-control combo and the 2952 line card controller are designed to operate on a PBX line card and will accommodate ISDN. Called a subscriber line data link (SLD) architecture, this scheme requires three wires.

—Pingry

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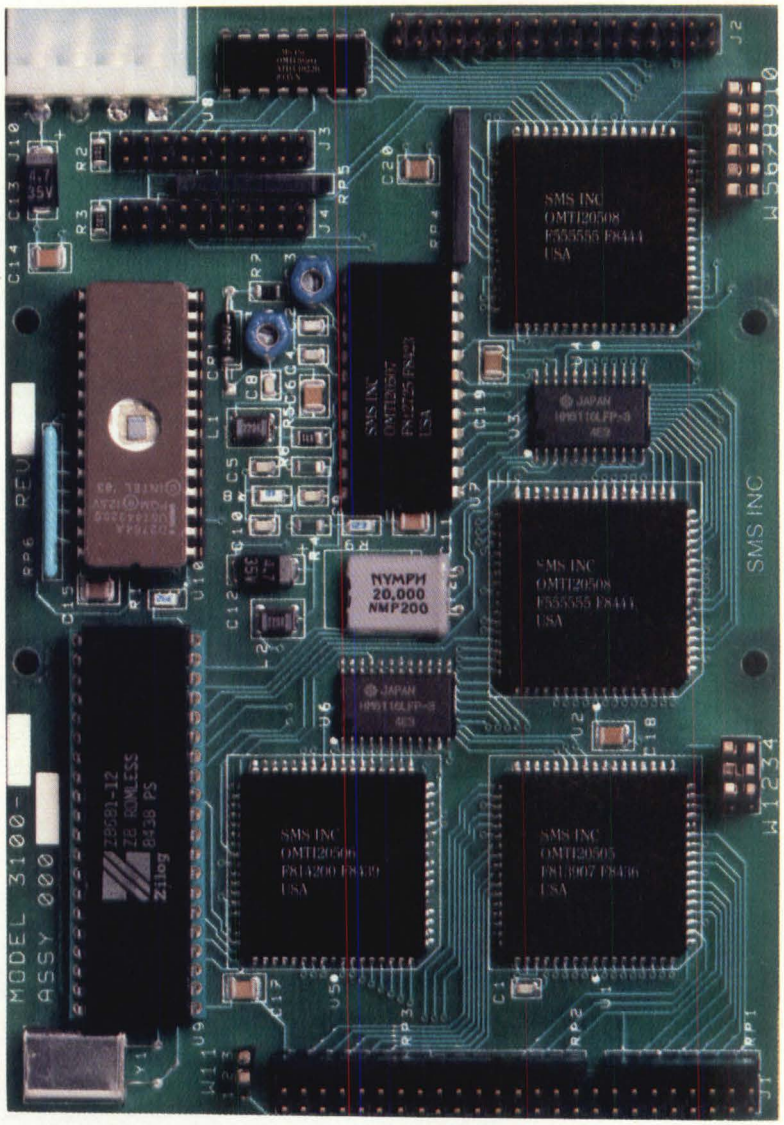

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Analog And Digital Accelerators Speed Simulation

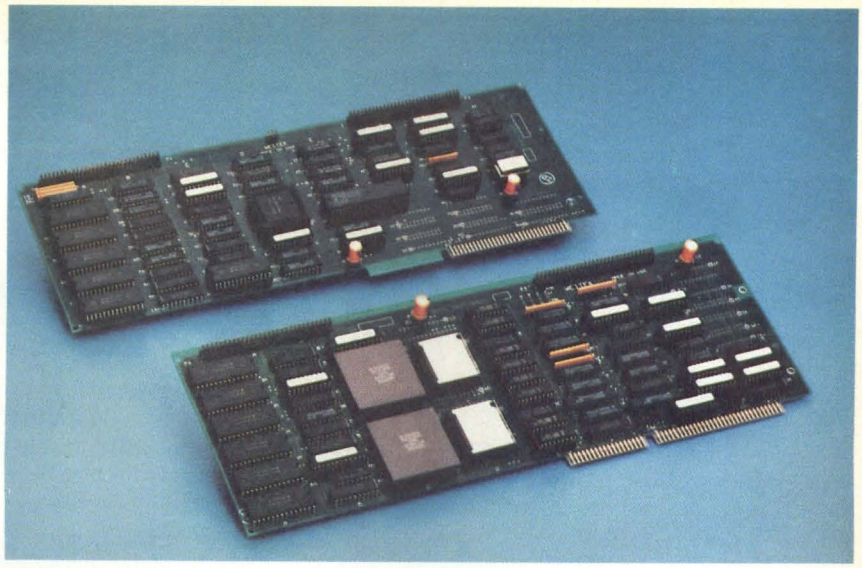

Figure 2: Weitek's WTE 6400 SPICE accelerator is a floating point array processor that uses a set of three Multibus boards and the CSPICE software from Circuit Tools Inc. The system's ALU consists of four WTL 1064 floating point multipliers, four WTL 1066 six-port register files and a WTL 1065 adder.

Verifying whether a design functions properly is among the most costly and time-consuming stages of the design cycle. This is especially apparent with analog circuits and large digital systems. Logic simulators and analog simulators, such as SPICE, running on mainframes provide an alternative to breadboarding, but even mainframes get bogged down with large designs. This has prompted the development of hardware accelerators for both analog simulation and digital simulation.

Figure 1: Shiva Multisystems' SX Series SPICE accelerators execute simulations at speeds ranging from 20 to 100 times faster than a VAX 11/780. The machines' performance is a result of PowerSPICE, a relaxation-based SPICE algorithm, and SPICEngine, a parallel processing number crunching computer. To the circuit designer, the PowerSPICE interface appears identical to traditional SPICE programs.

Until now, accelerators were available for only digital simulation and came from Zycad (St. Paul, MN), Daisy Systems (Mountain View, CA) and Valid Logic (San Jose, CA). Newcomers to the expanding logic simulation arena include Silicon Solutions (Menlo Park, CA) and Cadnetix (Boulder, CO).

For analog simulation, however, the first accelerators were recently introduced by Shiva Multisystems (Menlo Park, CA) and Weitek (Sunnyvale, CA). Prior to these introductions, increasing analog simulation execution rates was done with a combination of mainframes and array processors.

Shiva's accelerators, designated the SX Series (**Figure 1**), reportedly deliver 100 times the performance of a VAX 11/780-based SPICE2 simulator. The speed results from a combination of advanced hardware and software technologies. Shiva's SPICEngine is based on a parallel architecture of two to twelve NS32016 (or NS32032) processors running at 10 MHz. Also included are UNIX 4.2 (enhanced), a floating point coprocessor, 8 Kbytes of local cache memory, up to 28 Mbytes of main memory and a 30 Mbyte/sec packet switched bus. The other half of the system is PowerSPICE, the firm's circuit simulation software package that uses multilevel relaxation algorithms. And unlike traditional SPICE, PowerSPICE determines charge levels, a critical parameter in MOS design. Prices for the SX Series range from $100,000 to $350,000.

Relaxation techniques allow each circuit equation to be solved at its respective rate of change. This takes into account the fact that voltage and current levels of the circuit's devices change at different speeds. Multilevel relaxation is a hierarchical application of standard relaxation that runs at higher speeds. When simulating any circuit, more CPU power is needed to solve equations that change rapidly than those that change slowly. If a particular node is changing quickly, the system takes a very small timestep without penalizing the rest of the circuit; for slow changing nodes, a larger timestep is taken. Traditional SPICE, in contrast, takes the same size timestep for each node in the circuit, determined by the fastest changing node. Prior to relaxation methods, circuit simulators solved all equations at the speed of the most rapidly changing node.

To determine the various timestep sizes, PowerSPICE looks at the local truncation error of each node. Truncation error is the difference between the actual waveform and the one used to approximate the function. Once the truncation error of each node is calculated, the slow nodes and fast nodes are categorized and partitioned into subcircuits. At this stage, the circuit equations are solved using the same timestep for all the nodes within a subcircuit. Since nodes are partitioned by speed, the right amount of CPU power is delegated to each subcircuit, resulting in

higher performance.

Weitek has taken a more traditional approach to the analog simulation bottleneck by using CSPICE (a nonrelaxation algorithm) and array processor technology. Weitek's product, the WTE 6400 SPICE Accelerator (**Figure 2**), consists of three Multibus boards: a two-board floating point array processor and a 4-Mbyte memory board. Peak system throughput is 16 MFLOPS in IEEE double precision mode. The floating point ALU is comprised of four WTL 1064 multipliers, four WTL 1066 six-port register files and a WTL 1065 adder. The WTE 6400 sells for $30,000.

CSPICE, the heart of the WTE 6400, is an optimized version of Berkeley SPICE that was originally developed for Cray Computers by Circuit Tools Inc. (San Ramon, CA), a spin-off of Cray Research. Nonlinear direct analysis, nonlinear transient analysis and linear alternating current analysis are all supported by CSPICE.

When developing the WTE 6400, Weitek concentrated on the two areas that consume the most CPU time in a SPICE run: device evaluation and sparse matrix solving. According to Weitek, when simulating circuits in the 50 device range, 90% of the time is spent in the device evaluation phase; with 600 components, the split is 50-50 between device evaluation and sparse matrix solving. When solving a 3000-device problem (which takes over three days of CPU time on a VAX 11/780), 90% of the time is spent on sparse matrix equations. Solving these equations is a computationally intensive task that the WTE 6400 attacks via a floating point accelerator. However, a portion of its 16 MFLOP performance is lost because vector machines such as the WTE 6400 are inefficient in solving sparse matrices. Nonetheless, Weitek claims that the machine executes simulations 10-50 times faster than the same problem running on a VAX 11/780 with a floating point accelerator.

CSPICE has been tailored to take advantage of the WTE 6400's pipelined architecture for device evaluation. CSPICE works in conjunction with five microcoded subroutines that enable the complete simulation to run on the Weitek board set. The five routines address the primary functions of the SPICE algorithm: sparse matrix solving, device evaluation, truncation error calculation and matrix composition.

For digital simulation, Zycad, Cadnetix and Silicon Solutions have recently introduced digital accelerators. Zycad complemented its existing line of machines with two more: Sprintor and Expeditor. Sprintor is a logic and fault simulation engine that integrates into any IBM PC or Multibus-based engineering workstation. Sprintor handles designs containing up to 25,000 gates at speeds of 200,000 events/sec. Expeditor is a free-standing accelerator that handles designs of up to 50,000 gates and runs at 1,000,000 events/sec. The system interfaces to several host computers, including Apollo workstations, IBM PC/AT and DEC's VAX and MicroVAX. Sprintor is priced at $20,000 and will be offered only on an OEM basis; Expeditor is $125,000.

Silicon Solutions' teamed with HHB Softron (Mahwah, NJ) to develop the Mach 1000 simulation engine (**Figure 3**) which accelerates HHB Softron's CADAT simulator. CADAT is offered by several companies, including Mentor Graphics (Beaverton, OR), FutureNet (Chatsworth, CA) and Cadnetix. The system supports both logic and fault simulation. Moreover, it is a multilevel simulator that simultaneously models devices at the behavioral level, gate level and switch level.

Using a set of 10 full custom ICs, the basic engine handles up to 65,000 gates per accelerator board, with system capacity reaching 500,000; four Mach 1000's can be linked together to accommodate designs of up to two million gates. Execution speed of the Mach 1000 extends from a minimum of 500,000 events/sec to a maximum of 16 million events/sec. One extra board is needed for fault simulation. The Mach 1000 will be sold through HHB Softron and OEM CADAT suppliers; a logic simulation engine with a 65,000-gate capacity costs $85,000, and a logic and fault simulator with the same capacity is priced at $150,000. Both products will be available in the first quarter of 1986.

Figure 3: The Mach 1000, a logic simulation accelerator from Silicon Solutions, is built around the CADAT simulation algorithm and includes 10 full custom ICs, a 68010 front-end processor and up to 8 Mbytes of main memory. Special emphasis has been put on developing a compiler that speeds both design flattening and interconnection, and provides incremental compilation.

Another newcomer to hardware acceleration, Cadnetix's CDX 77000 Simulation Engine performs 200,000 evaluations/sec (about 65,000 events/sec) and handles up to one million gates. The system is configured around an 88-bit-wide bit-slice processor that supports up to 3 Mbytes of main memory. Network control and additional processing tasks are handled by a 68010-based subsystem. The Simulation Engine can be accessed by any CDX-9000 Series workstation in a network environment. Product shipments begin this quarter and the price is $60,000.

—Collett

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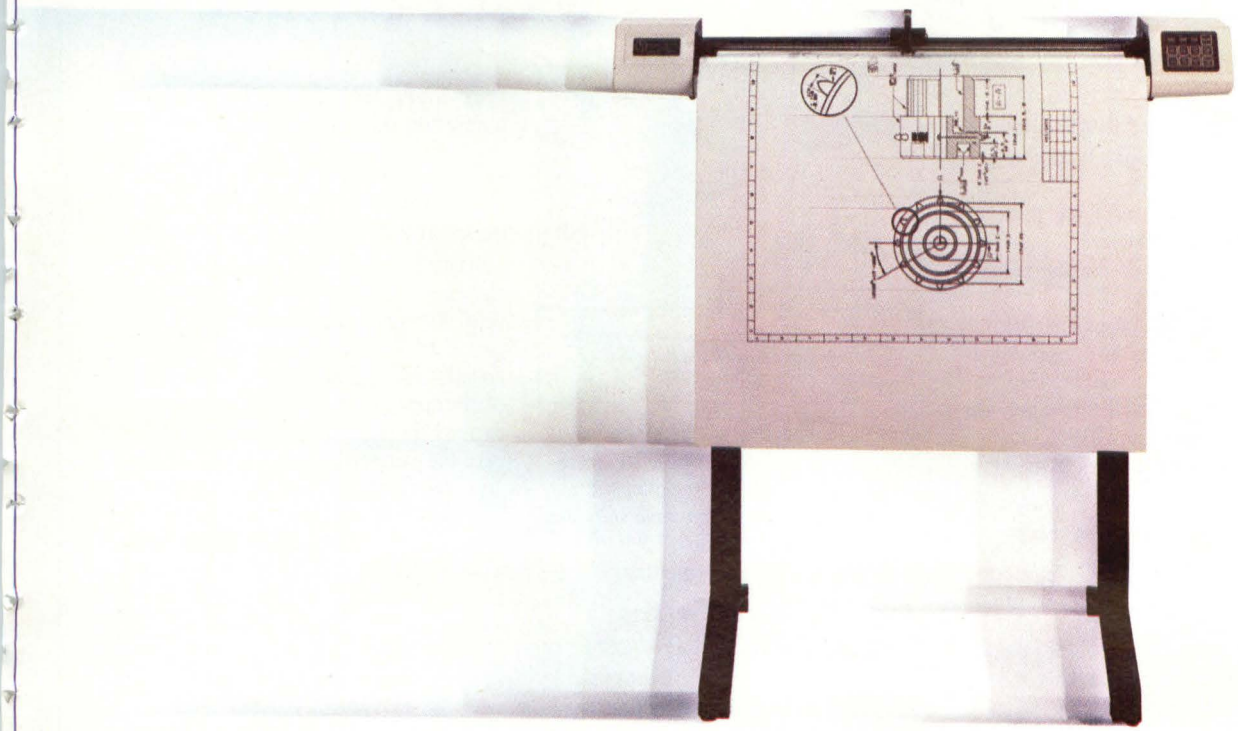

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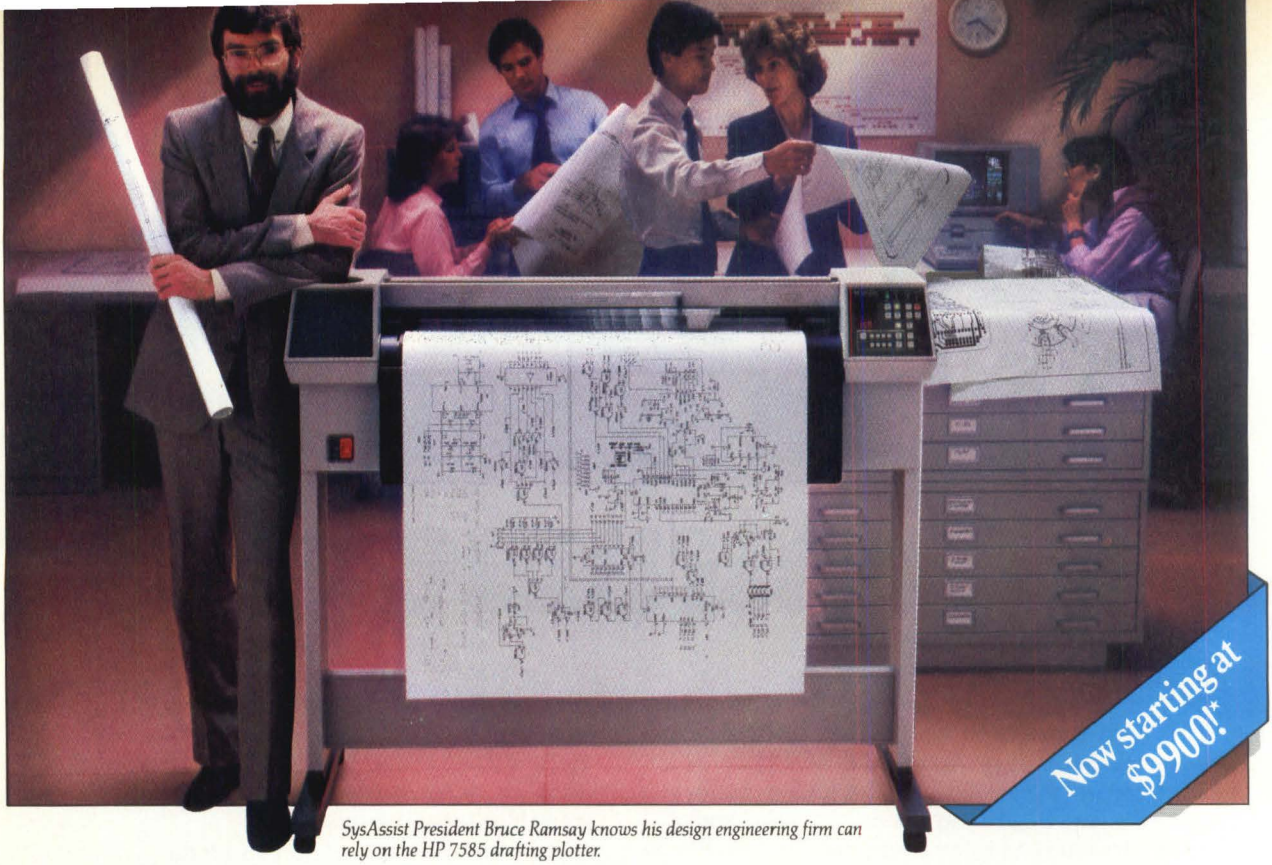

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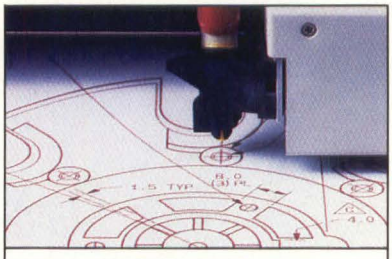

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Personal Computers Mate With Analyzers For Increased Flexibility

Figure 1: The PCI-4304 logic analyzer from Burr-Brown provides 32 input channels via a plug-in board, 3-foot ribbon cable and instrument pod that extends from the computer to the digital system under test.

Nearly 500,000 personal computers are used for scientific calculations, data acquisition and production testing. Such vendors as Burr-Brown (Tempe, AZ) and Northwest Instrument Systems (Beaverton, OR) allow state and timing analysis to be added to these capabilities through tight coupling between test and measurement hardware and the processor and display resources of personal computers via parallel links. This approach is in contrast to the industry practice of using either dedicated microprocessors or linking instruments and controllers via an IEEE 488 general-purpose interface bus (GPIB).

A tightly coupled approach allows users to work with familiar keyboards, displays and disk drives as well as access standard operating systems and languages to take advantage of application programs. The analyzer function needs only test and measurement hardware and related software. Dedicated analyzers need a central processor, keyboard and display in addition to facilities for data acquisition and storage.

Another approach loosely couples standalone instruments to personal computers via a GPIB parallel link. In this configuration, logic analyzers from vendors like Dolch Logic Instruments (Santa Clara, CA), Hewlett-Packard (Palo Alto, CA) and Tektronix (Beaverton, OR) depend on personal computers such as the IBM PC for instrument setup, post-acquisition analysis and data formatting to user specifications. The IBM PC acts as a GPIB controller through interface cards available from manufacturers such as National Instruments (Austin, TX) and Tecmar (Cleveland, OH). Kontron Electronics (Redwood City, CA) takes a similar approach with a proprietary parallel interface.

The loosely coupled approach allows other instruments from several vendors to be added. One drawback of the GPIB approach is that sets of processor, memory and display resources are duplicated in the instrument and the computer. Furthermore, instrument functions must be programmed in the formats specified by each vendor.

Examples of the tightly coupled approach include the microAnalyst 2000 logic analyzer from Northwest Instrument Systems and the PCI-4304 from Burr-Brown. The microAnalyst is a card set that resides in a separate chassis linked via a high-speed parallel link to the backplane of the IBM PC. This configuration accommodates a controller card and up to five data acquisition/memory cards for 16 to 80 input channels for state analysis. The PCI-4304 logic analyzer from Burr-Brown (**Figure 1**) takes up one card slot in the IBM PC to provide 32 input channels.

The high-speed parallel link coupled with fast data acquisition memory mapped directly into the host processor's address permits the microAnalyst 2000 the same operating speed as if physically located on the backplane. The user establishes a memory window by placing the beginning location into the segment register of the 8088 CPU. Through this 4 Kbyte window, the user directly manipulates each analyzer module to acquire data, set event conditions or monitor system clocks. The Burr-Brown system uses a similar scheme.

As many as 15 trigger/store states on the microAnalyst 2000 simplify tracking high-level language execution. Users can define IF-THEN-ELSE condition sequences, as well as count iterations of events and specify logical relationships between conditions. Both trigger events and acquired data can be stored on disk for future use. The user will find similar capabilities in the PCI-4304, but with trigger words limited to eight. The microAnalyst 2000 acquires data at bus cycle rates approaching 10 MHz. Furthermore, users can synthesize their own sample clock from as many as five clock/control signals to track software in systems with complex bus cycles.

Still, closely coupled instruments are hard pressed to offer the full performance of standalone instruments. For example, the Kontron Electronics Series III analyzer provides acquisition memory of 16K words at a 100 MHz sample rate, while the microAnalyst 2000 provides only 2K words of acquisition memory for a 10 MHz sample rate.

For higher performance needs, Dolch and Kontron provide software packages so their standalone analyzers can use the IBM PC for storage of setup menus and reference. Dolch ties its 40C50 logic analyzer to the IBM PC via a GPIB parallel link, whereas Kontron uses its own parallel interface to link its Series III analyzers to the same host.

—Aseo

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ICs

Reducing The IBM PC/AT To A Chip Set

Although the complexity of VLSI design has resulted in a longer time-to-market of custom VLSI designs, the introduction time of application-specific boards has decreased. Because of this, designers of board-level products are constantly seeking ways to improve price/performance without incurring the costs of either custom or semicustom designs. For manufacturers such as Compaq, Texas Instruments and Hewlett-Packard who must compete directly with IBM, this presents a major problem. Realizing this, three companies have introduced ways of reducing the AT to less than 20 components.

Chips and Technologies (Milpitas, CA), will offer a series of chip sets to implement the AT, which will greatly reduce the complexity of microcomputer design. Headed by the ex-president of Seeq, Gordon Campbell, Chips and Technologies will target the areas of microcomputers, graphics and communications. The first product, a set of six ICs, will reduce the AT design from a set of 91 ICs to 20 components. Sampling this month, the chip set will allow designers to use four-layer boards in their products while reducing power supply requirements. Initially, the chip set will be manufactured using both gate array and standard cell technology. By next year the company expects to be offering the parts in a full custom configuration.

At the end of the month, Chips and Technologies will introduce its second product, a set of five graphics chips to create the IBM enhanced graphics adapter. The IBM adapter uses approximately 51 ICs; the chip set will reduce this to a 20 IC design. "With this kind of integration," says Campbell, "manufacturers will be able to offer the same kind of functionality as IBM on a single half-height card." Chips and Technologies' third product offering will be in the area of data communications. Late this year, the company will offer a single-chip Starlan Encoder/Decoder for operation with Intel's 82586. The chip is designed for transmission at 1-2 Mbits/sec over twisted-pair wire; Starlan's developer, AT&T, is a target customer.

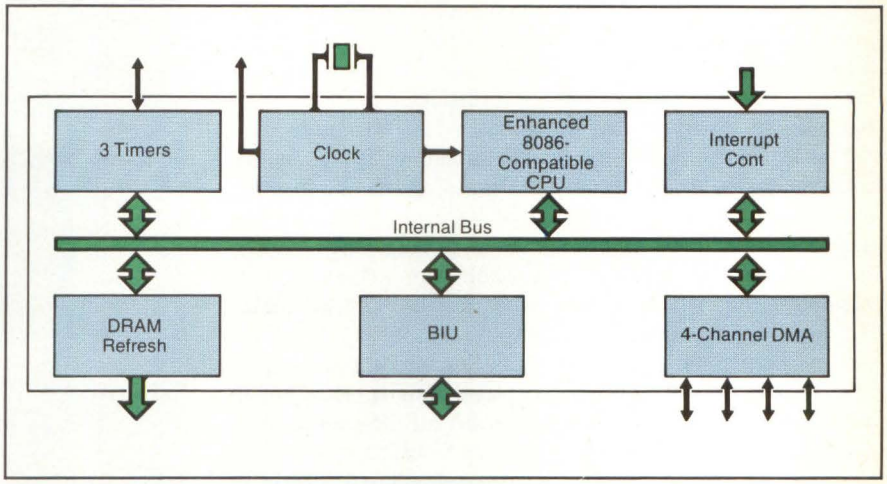


Figure 1: Block diagram of Intel's proposed 80886 PC-on-a-chip IC which will be officially announced in mid-1986.

Seeing the market opportunity in consolidating the AT, Zymos (Sunnyvale, CA) recently demonstrated a method of reducing the AT to a total of four ICs. Using the company's own ZY-DP3 cell library and the ZyP design automation system, the entire AT board, except for the 80286, 80287 and 8042 keyboard controller, was implemented on a single chip. This IC contains 11,642 cells, 512 bits of compiled RAM, 4 Kbits of compiled ROM and 84 compiled PLA terms.

Using this standard cell approach, the designer can work within the framework of the AT design and gain improvements in cost, performance and functionality. For example, at the board level, the 80286 operates with nonmultiplexed and separate data and address buses. However, many peripherals were designed for operation in a multiplexed bus environment typical of earlier CPU designs, requiring the use of external TTL MSI devices to translate signals from the multiplexed to the nonmultiplexed mode. In the Zymos approach the board design is implemented directly without any modification. Thus, a system designer could reconfigure the various peripherals to operate in a nonmultiplexed environment using cell and supercell elements from the Zymos library, eliminating the need for the additional TTL circuitry. This would further reduce the chip size as well as improve throughput.

Intel (Santa Clara, CA), partially owned by IBM and supplier of the processors for the IBM PC families, will not be left out of the race for higher levels of integration. The company has already briefly disclosed information on its 80886 PC on-a-chip that will be announced mid-1986 (**Figure 1**).

As the cost of the AT drops, systems integrators will be able to provide low-cost multiuser, multitasking systems. Designers will also couple these systems with other high-performance processors for coprocessing functions such as image processing and graphics.

—A. Wilson

Managing The VLSI Explosion With Silicon Compilation

by Ronald Collett, Sr. Technical Editor

IC fabrication technologies will continue to outpace all but one avenue of CAE/CAD-based design: silicon compilation. With traditional CAE/CAD systems, engineers will be unable to manage the complexities of tomorrow's designs. Silicon compilation will be the only feasible technology to handle one-million device chips. Nevertheless, there are several reasons why it will not find immediate widespread use.

First, current electronic design automation (EDA) systems adequately handle up to about 12,000 gates, and most gate array and standard cell projects fall below 7,000 gates. Second, the majority of designers have yet to make, or have only recently made, the transition from off-the-shelf parts to semicustom technology (i.e., gate arrays and standard cells). This will make the move to a more advanced design methodology, such as silicon compilation, a gradual process. Silicon compilation also requires greater awareness of system level design practices than semicustom methods or designing with off-the-shelf chips. Engineers work with LSI/VLSI building blocks, as opposed to SSI/MSI devices. So instead of implementing just a portion of a system, designers build a complete system on a board, to be integrated with other engineers' board-based systems.

Third, although many semiconductor firms have the fabrication capabilities to put 100,000 to 500,000 transistors on a chip, the first 50,000-transistor gate arrays have just been introduced. Why? One reason is that present CAE/CAD tools cannot support the design of such dense chips, except at the handcrafted full-custom level. Consequently, logic designers have not been exposed to the difficulties of applying today's tools and design methods to a 100,000-transistor device.

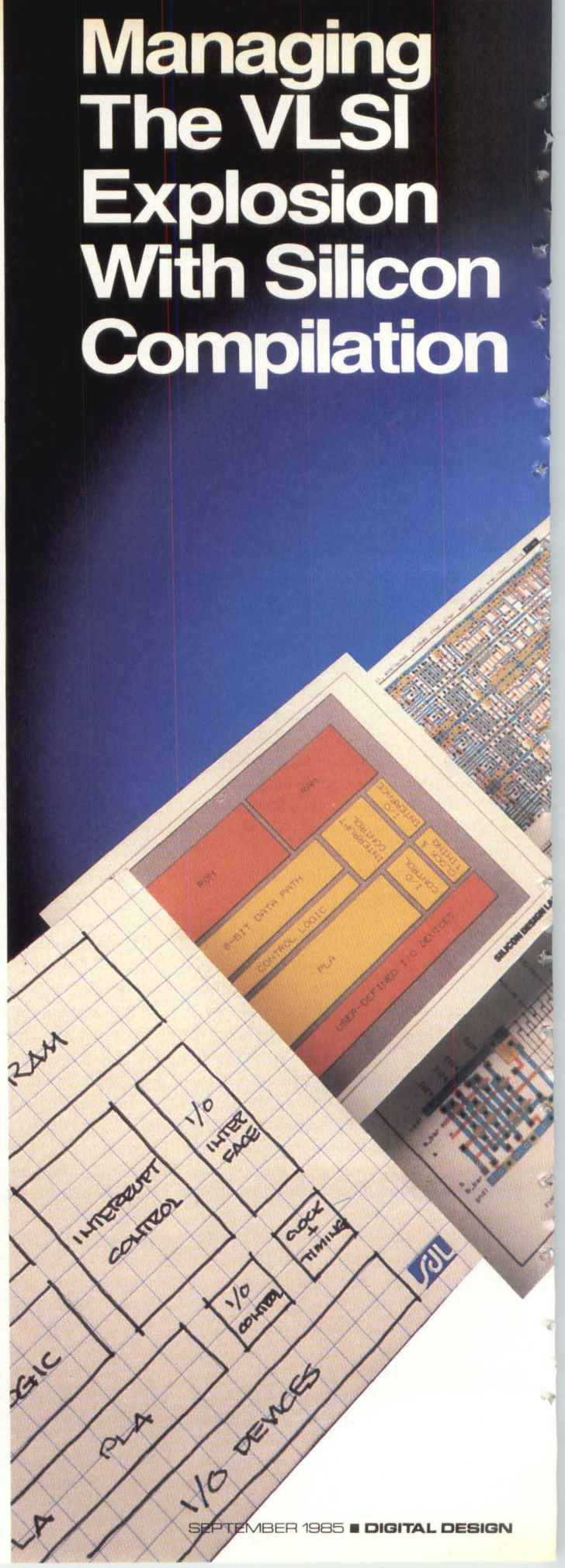
As systems get more complex, larger functional blocks must be used, causing changes in design methodologies. Constructing functions from random logic is an example of a soon to be outdated design practice. Wherever random logic appears to be necessary, engineers will partition it into organized blocks to be implemented by a random logic compiler or PLA compiler.

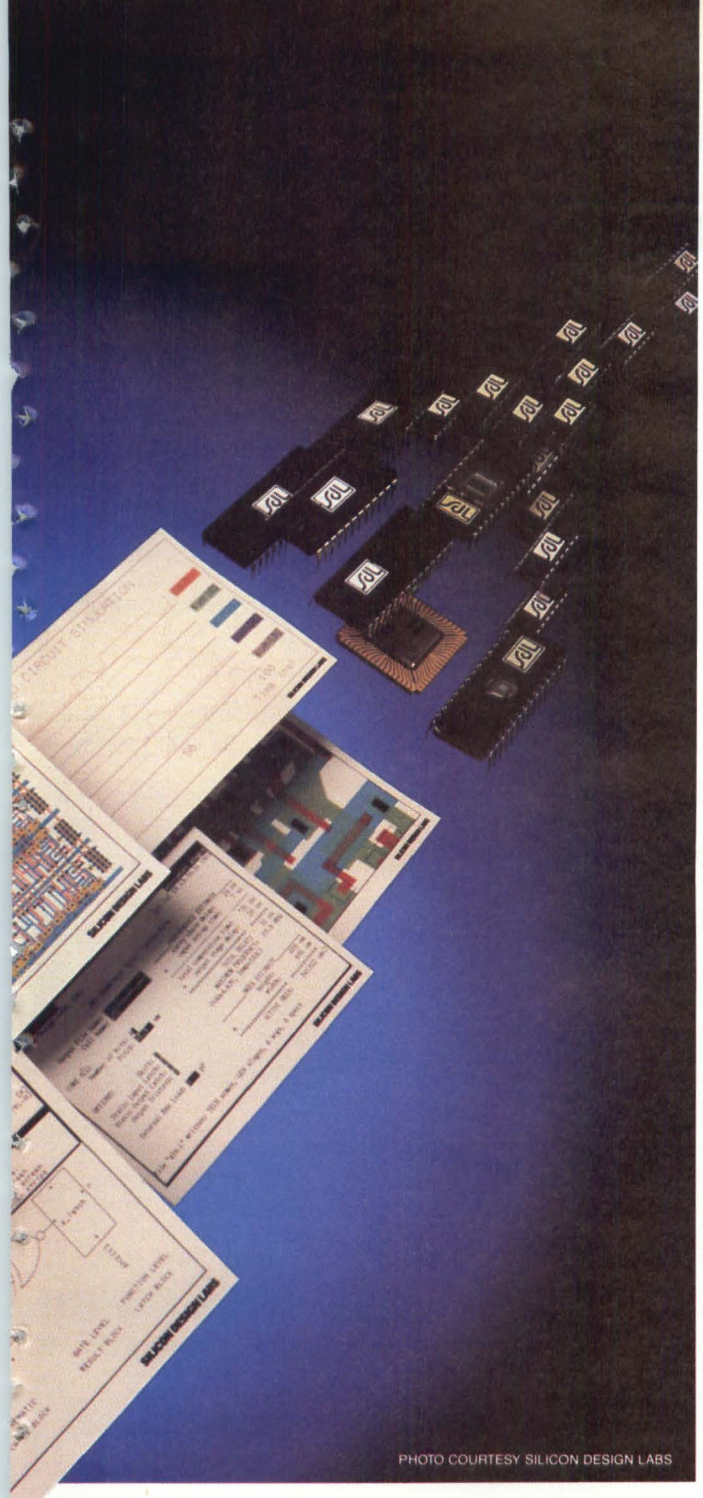
Over the next three years, as higher integration levels form the foundation of system design, the magnitude of the VLSI problem will become apparent. This in turn will necessitate the use of silicon compilers.

Examining The Technology

Most currently available turnkey silicon compiler systems are structural, as opposed to behavioral (**Figures 1** and **2**). Those companies offering turnkey structural silicon compiler systems include Silicon Compilers Inc. (SCI) (Los Gatos, CA), VLSI Technology Inc. (VTI) (San Jose, CA), Seattle Silicon Technology (SST) (Bellevue, WA) and Lattice Logic (Edinburgh, Scotland). Silicon Design Labs (SDL) (Liberty Corner, NJ), SDA Systems (Santa Clara, CA) and VTI provide tools for users to write their own compilers, and Metalogic (Cambridge, MA) offers a behavioral silicon compiler.

Fabrication technology independence (i.e., CMOS, NMOS, bipolar, GaAs) and design rule independence are often viewed as critical aspects of a silicon compiler system. Each semi-





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conductor manufacturer, or foundry, has its own set of design rules that dictate the minimum widths among circuit elements throughout the chip. And the artwork, or masks, describing an IC must obey the particular foundry's design rules. Allowing designers the option of multiple sourcing requires that a design be portable over all fabrication processes and, similarly, that only a minimal effort be necessary to re-implement the design when the rules of the target process are altered.

Turnkey silicon compiler systems from SCI, SST and VTI are comprised of a wide variety of module generators, or cell compilers. Examples of common modules include ALUs, PLAs, RAM and ROM. Designers call particular modules from the module library, fill out a form that lists the module's functional parameters and then push the compile command. This module is then connected to other modules and blocks.

In its present form, SCI's Genesil does not allow users to develop their own modules. Rather, SCI continuously builds new modules and integrates them into the system. SCI puts a high priority on offering new modules, but generating all of the modules that users desire is a difficult task. Determining whether this is a significant drawback is difficult since silicon compilation technology is still in its infancy.

A parallel situation exists with both gate array and standard cell libraries. However, with these semicustom design methodologies, engineers can create functions from primitives. Genesil also permits users to create high-level functions from primitives, but this defeats the purpose behind silicon compilation, which is to distance the designer from working at the primitive level.

Allowing engineers to build their own module generators is one possible solution to the problem. This is the strategy of Silicon Design Labs, Seattle Silicon Technology, SDA Systems and VLSI Technology. Presently, SST and VTI are the only silicon compiler companies offering both a compiler library and the capability to create new generators. Since this provides designers with the best of both worlds, it will likely be adopted by other vendors as well.

In comparing turnkey systems from SCI, VTI and SST, SCI's Genesil is the most sophisticated. Using **Figure 2** as a reference, Genesil is in the structural domain and consists of architectural, algorithmic and functional block level elements. With the Genesil system, users first define a particular function by filling out a specification form and then assigning names to signal buses. Some examples of the available functions are ALU, PLA, Dual-Port RAM, Interface, Random Logic, FIFO and ROM. After the form entry stage is completed, Genesil compiles a custom circuit layout of the function and displays a graphical representation on the screen.

Designs done with Genesil proceed hierarchically through the use of blocks, modules, chips and chip-sets. Blocks are joined together to form a module; modules can be combined to produce a "chip"; and "chips" can be linked to form a chip-set. Chips are modules that have bonding pads, and chip-sets are collections of chips. When laying out the IC, the user interactively places blocks, modules, chips and chip-sets. (See box entitled "A Silicon Compilation Design Example.") In a typical design, the number of blocks, modules, chips and chip-sets ranges from 10 to 50. To interconnect these elements, the automatic router is invoked. The router's features include clock and power bus sizing, low resistivity crossunders for supercritical signals and group treatment of buses, rather than as individual signals.

When specifying a block, the system notifies the user of any syntax errors. In addition, blocks violating layout rules or electrical rules will not compile. Blocks can be interconnected before or after compiling other surrounding blocks. Genesil supports dual-layer metal CMOS or single-layer metal NMOS, with feature sizes of 2 or 3 microns. The user also selects a particular semiconductor foundry to fabricate the chip. SCI currently has agreements with NCR (Fort Collins, CO), AMI

(Santa Clara, CA), IMP (San Jose, CA) and VLSI Technology.

Along with the circuit layout, Genesil generates a simulation model, a timing model and a timing datasheet. Unlike most conventional verification tools, timing analysis is separated from simulation. An independent timing model, comprised of transistor representations and timing delays allows designers to focus solely on the circuit's timing relationships. Moreover, timing analysis does not require test vector generation. To provide users with maximum simulation execution speed, the circuit is modeled at the functional level instead of the gate or switch level. The simulator's capabilities and user interface are similiar to a logic analyzer.

Genesil runs on several hardware platforms: the DEC MicroVAX II, VAX 11/750, VAX 11/785 and the Daisy Systems (Mountain View, CA) Siliconmaster. Prices for the various configurations range from $165,000 for a single-user system to $640,000 for a 10-user system.

Seattle Silicon Technology is a strong supporter of the workstation environment and developed its Concorde-I silicon compiler (**Figure 3**) to run on hardware platforms from Mentor Graphics (Beaverton, OR), Valid Logic (San Jose, CA) and CAE Systems/Tektronix (Sunnyvale, CA). As with Genesil,

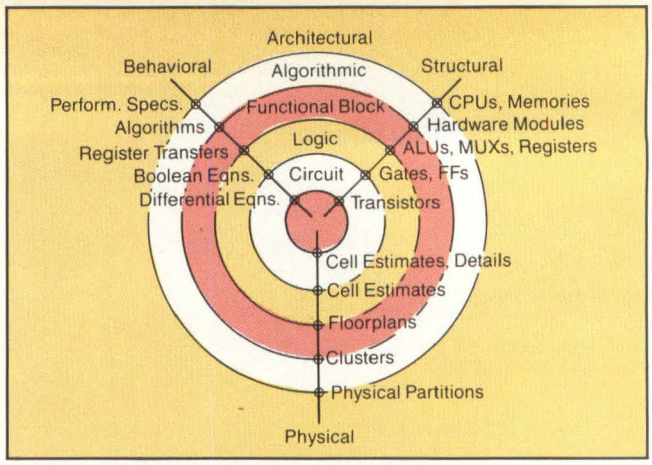

Figure 1: Silicon compilers fall within two domains: Behavioral or Structural, or sometimes a combination of both. The compiler's task is to transform the structural or behavioral description into the Physical domain. This model, suggested by Thomas and Watson at the 1985 Design Automation Conference, is similar to the Gajski/Kuhn model (*Digital Design*, August 1984).

A Silicon Compilation Design Example

During the design process, experimenting with different architectures of the same design gives designers tremendous leverage over its implementation. Since IC designs can be generated rapidly with a silicon compiler, architectural exploration is one of its major strongpoints.

Recently, *Digital Design* used SCI's Genesil Silicon Compiler to design a digital crosspoint switch (**Figure 1**, also see *Digital Design*, May 1985). The specification called for eight 4-bit wide input channels, eight 4-bit wide output channels and a clock. In addition, several control lines were needed to select which input and output channels were active. During one clock cycle, a 4-bit wide path is opened between the selected input and the selected output; on the next clock cycle, a different path can be selected. One application of the crosspoint switch is pipelining, where 4 bits of data are presented at the input and then channeled to a particular output to be used in a computation. The data would then be fed back to the switch's input and passed to the next stage of the pipeline.

During the design cycle, three different architectures were generated that would implement the switching function. The first uses eight 4-bit latches on the input, with the outputs bused together in a wire-OR configuration feeding eight 4-bit output latches (**Figure 2**). A 6:16 programmable logic array (PLA) decodes the six input- and output-select lines that enable the appropriate latches. Each block of circuitry is generated by entering its functional requirements on a form.

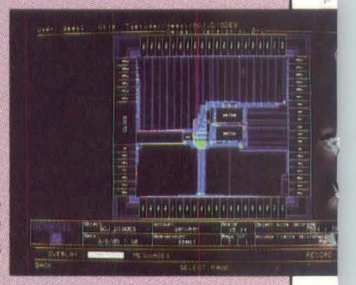

Figure 5: A view of the layout shows that the high number of I/O pins dictates the chip's size.

Once a block is completed, basic electrical rule violations are flagged by Genesil. The user then interactively places the blocks and calls the automatic router. In solution #1, the estimated core area is 122 mils × 65 mils, which includes an approximation of the routing channel area. After running the timing analyzer on the switch, the results show that the device operates at a maximum of 9.1 MHz and dis-

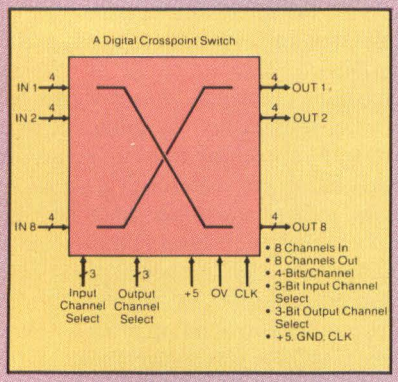

Figure 1: Shown is a block diagram of the crosspoint switch.

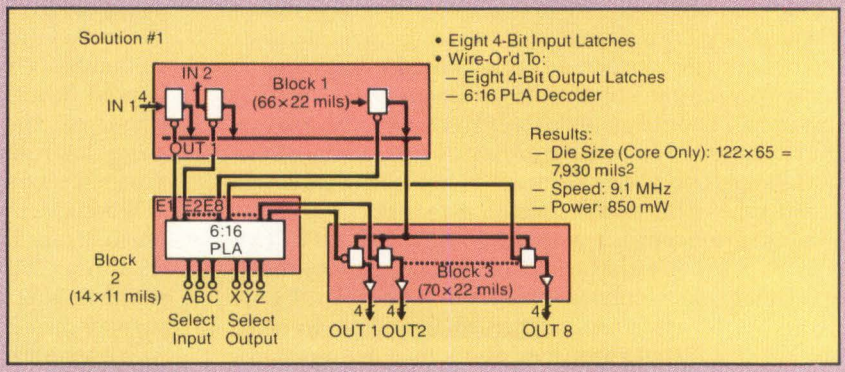

Figure 2: This wire-OR'd configuration runs at 9.1 MHz while dissipating 850 mW.

DEFLECTION

AMPLIFIERS

FEATURES	SPECIFICATIONS
Powerful:	To 20 amps, 60 volts
Fast!	To 6μs scan & retrace
Wide Bandwidth:	dc coupled up to 4MHz
Stable:	To 10μA/°C drift
Accurate:	To 0.001% linearity

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- CRT Test & Measurement
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- E-Beam Welding
- E-Beam Lithography
- Electronic Photo-Typesetting

MODEL NO.	OUTPUT RANGE
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DA-PP2N-7	4 amps, 20 volts
DA-PP4N-7	8 amps, 20 volts
DA-0420	4 amps, 20 volts
RDA-1220-S86 (Lab Standard)	12 amps, 20 volts
RDA-1220-S86C (Water Cooled)	12 amps, 20 volts
■DA-PP2N-5	4 amps, 35 volts
DA-PP4N-5	8 amps, 35 volts
DA-PP8N-5	16 amps, 35 volts
RDA-1635	16 amps, 35 volts
■RDA-1255	12 amps, 55 volts
■RDA-0660	6 amps, 60 volts
RDA-0960	9 amps, 60 volts
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Concorde-I users fill out forms to characterize a particular function. However, Concorde-I is a lower-level structural silicon compiler since most of its cell compilers fall within the functional block level and logic level (**Figure 2**).

Although Concorde-I is not as sophisticated as Genesil, it offers several features that Genesil does not. First, Concorde-I is the only silicon compilation system that has analog compilers. Second, it offers both design rule independence and fabrication process technology independence within the CMOS family. As a result, ICs designed with Concorde-I can be fabricated by most foundries in any CMOS process. SST currently has agreements with several semiconductor makers including VLSI Technology, NCR (Fort Collins, CO), AMI (Santa Clara, CA) and IMP (San Jose, CA). Third, users have access to the firm's SLIC compiler language and can either develop customized compilers or tailor existing ones. Compilers written by the IC designer can be fabricated in any technology, including MOS, bipolar or GaAs.

Concorde-I offers compilers that generate a wide range of functions; datapaths (up to 32 bits wide), PLAs, storage logic

	Behavioral Domain	Structural Domain	Physical Domain
Architectural Level	performance specs	CPUs memories switches controllers buses	physical partitions
Algorithmic Level	algorithms (manipulation of data structures)	hardware modules data structures	clusters
Functional Block Level	operations register transfers state sequencing	ALUs MUXs registers microsequencer microstore	floorplans
Logic Level	boolean equations	gates flip-flops latches	cell estimates
Circuit Level	differential equations	transistors capacitors resistors	cell estimates cell details

Figure 2: Another way of describing the model in **Figure 1** is with a table. The Behavioral domain describes a system's operations, sequencing and timing. The Structural domain describes the functions needed to implement the behavioral specification. And the Physical domain describes the physical implementation of the design.

sipates 850 mW of power.

A second type of architecture takes advantage of the fact that the input is just a large multiplexer. When filling out the entry form, an 8-to-1 4-bit wide multiplexer is requested. Since three control lines are already included in the MUX, the PLA entry form is filled out to generate a 3:8 decoder. Also, block number 3 from the first solution (eight 4-bit output latches) can be used in this design (**Figure 3**). The estimated core size of this architecture is 94 mils × 51 mils. Once again the timing analyzer is run, but this time the device is benchmarked at 12.6 MHz, with power dissipation at 775 mW. Despite the increased performance and decreased die area, block number 3 dominates the floorplan and produces a highly asymmetrical layout, which wastes silicon area.

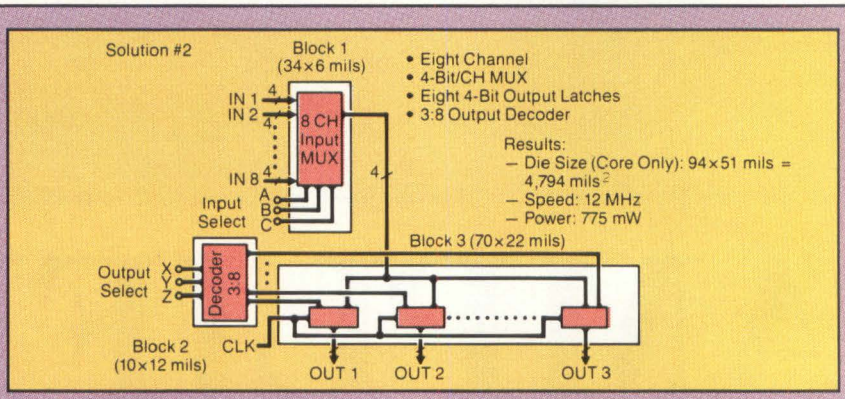

Figure 3: This architecture is based on an 8-channel MUX; each channel is 4 bits wide.

The third design alternative is similar to solution #2, with the exception that block number three is divided in half. Instead of eight 4-bit output latches in a single block, two blocks of four 4-bit latches comprise the output section (**Figure 4**). By dividing the output, the designer can place the output blocks independently and thus produce a more symmetrical layout. This solution yields a device that runs at 13.1 MHz, dissipates 775 mW and has a core size of 68 mils × 61 mils.

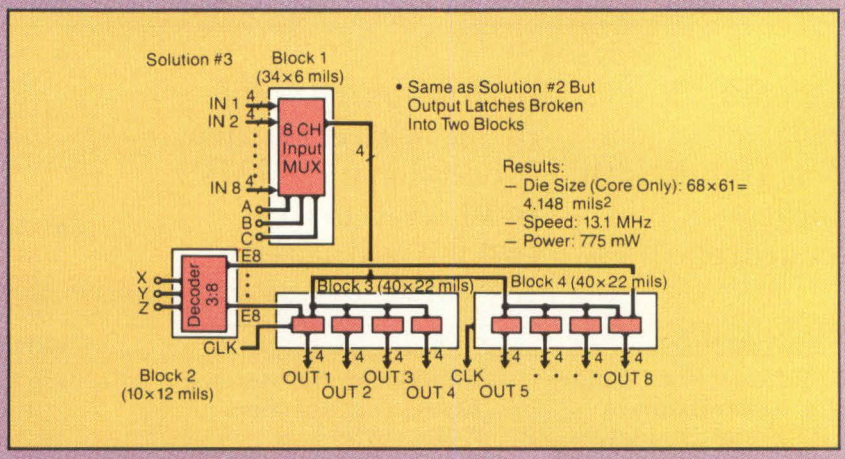

Figure 4: The only difference between this architecture and solution #2 is that the output latches are divided into two blocks.

One problem with implementing this function on a single chip is that the active die area is only 5% of the entire chip (**Figure 5**). This is because the specification calls for over 75 I/O pins. In this instance, die size is determined by both the number and size of the chip's bonding pads. To make better use of the silicon, one solution is to implement the device on two chips, which reduces the number of I/O pins per chip. The resulting ICs would be approximately one-fourth of the present implementation's size. Two smaller chips would also be less costly than the present chip.

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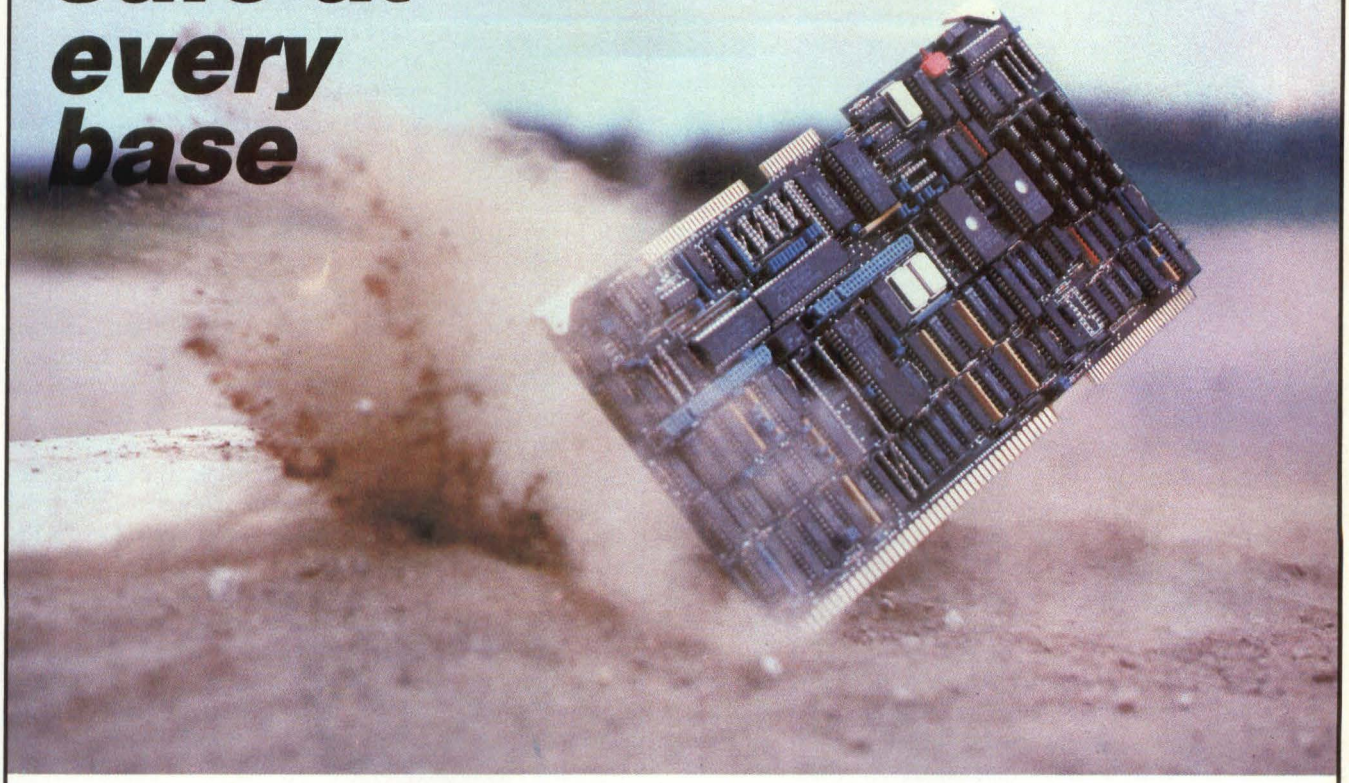

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Figure 3: Seattle Silicon Technology's Concorde-I silicon compiler runs on workstations from Mentor Graphics, CAE Systems/Tektronix and Valid Logic. Shown is the compiler running on the Mentor workstation (left) and the CAE Systems/Tektronix workstation (right). A unique feature of Concorde-I is its analog compilers.

arrays (SLA), RAM, ROM, MSI and SSI functions. Analog functions include op-amps, comparators, filters, analog switches, oscillators, FETs, diodes, resistors, A/D and D/A converters and capacitors. After compiling an analog module, the system immediately displays that modules's power consumption as well as other performance specifications. A SPICE file is also generated for analog simulation.

Another attribute of Concorde-I is the SSTAR (Seattle Silicon Technology Array) module compiler. SSTAR translates block diagrams, Boolean equations, circuit diagrams or truth tables to a folded logic array with internal registers. SST is currently developing performance estimation tools for SSTAR.

Unlike Genesil and VTI's system, Concorde-I relies on the host workstation's simulation and timing verification tools. However, for connecting compiled blocks, Concorde-I includes a set of automatic routing tools called PRIDE. And similiar to Genesil and VTI's system, users manually lay out the chip before routing. Concorde-I's price tag, not including the workstation or analog compilers, ranges from $35,000 to $55,000; a set of analog compilers costs around $25,000; and a typical high-end workstation is $100,000.

Another firm advocating workstation-based compilers is VTI. VTI's software runs on Apollo's (Chelmsford, MA) DN660, and Daisy's Siliconmaster. VTI has been offering compiler technology for several years but recently repositioned its cell compilers by renaming them silicon compilers. Aside from the marketing advantage of the new name, the repositioning coincides with the firm's introduction of Megacells—a technology that facilitates system design. The Megacell concept offers a higher level of sophistication than cell compilers alone. It combines cell compilers with a sophisticated library of handpacked LSI/VLSI functions linked via a bus architecture (**Figure 4**). All Megacells are 110 mils high which allows them to be placed on the chip with minimal wasted silicon. The Megacell library includes a 65C02 microprocessor, bus and DMA controllers, a 128K RAM and UARTs.

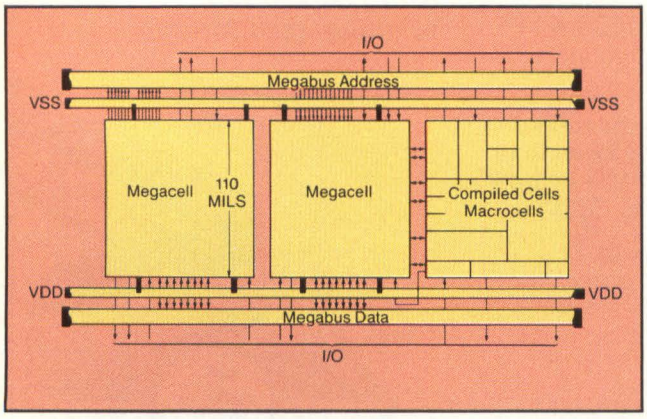

Figure 4: VTI's Megacell concept combines handpacked LSI/VLSI functions with cell compiled functions, all linked together with a data bus and address bus. This approach to silicon compilation provides designers a means to build efficiently laid out single-chip systems. The Megacell library includes a 65C02 microprocessor, ROM (16K, 32K, 64K, 128K), an 82C37A DMA controller and two UARTs.

VTI's compilers are generated by first filling out a form to characterize the function. The user interactively places blocks that are then automatically connected by the router (**Figure 5**). The one exception to this procedure is the logic compiler, which automatically places and routes random logic cells. An extensive line of CAE software including a behavioral simulator and test development tools is also available.

For users who wish to construct customized compilers, VTI provides a compiler language called VIP (VLSI Implementation Program). VIP was the first commercially available compiler language, but it now shares the stage with the L-Language, a compiler language from Silicon Design Labs. VIP is a procedural language that uses text statements to describe IC layouts and is an extension of Mainsail. VIP IC layout descriptions are based on design rules that are described relative to each other in terms of a variable scaling factor called lambda. An advantage of a lambda-based system is that the rules are easily changed when the fabrication process is modified. (When a process is altered, all of the IC's geometries must be sized accordingly.) However, a disadvantage of a lambda-based system is that design rules do not scale linearly as feature sizes approach the 1-micron range. And since many fabrication processes will shortly be making chips with 1.25-micron geometries, modifying a lambda-based rule set could be difficult.

An alternative to lambda rules is a process technology file, a course taken by Silicon Design Labs and Lattice Logic. A process technology file contains electrical information necessary for the generation of artwork. Transistor types, contact types, design rules and definitions of physical layers are among the data found in a technology file. Unlike SDL's current offering which is primarily aimed at IC designers, Lattice Logic's Chipsmith is a turnkey system targeted at systems engineers.

Chipsmith is an automated standard cell and gate array compilation system positioned as a silicon compiler. Designs are input via either the hardware description language Model or schematic capture. As with SST's Concorde-I, designs created with Chipsmith are portable over a wide range of CMOS processes. The compiler software is supported by a switch-level simulator as well as tools for both automatic and interactive placement and routing. The family of CAE/CAD tools as well as the compiler run on DEC's VAX, Perkin-Elmer's 3200, the IBM PC/AT, Whitechapel, and workstations from Apollo Computer and Sun Microsystems (Mountain View, CA). Not including the hardware platform, Chipsmith prices range from $12,000 to $125,000.

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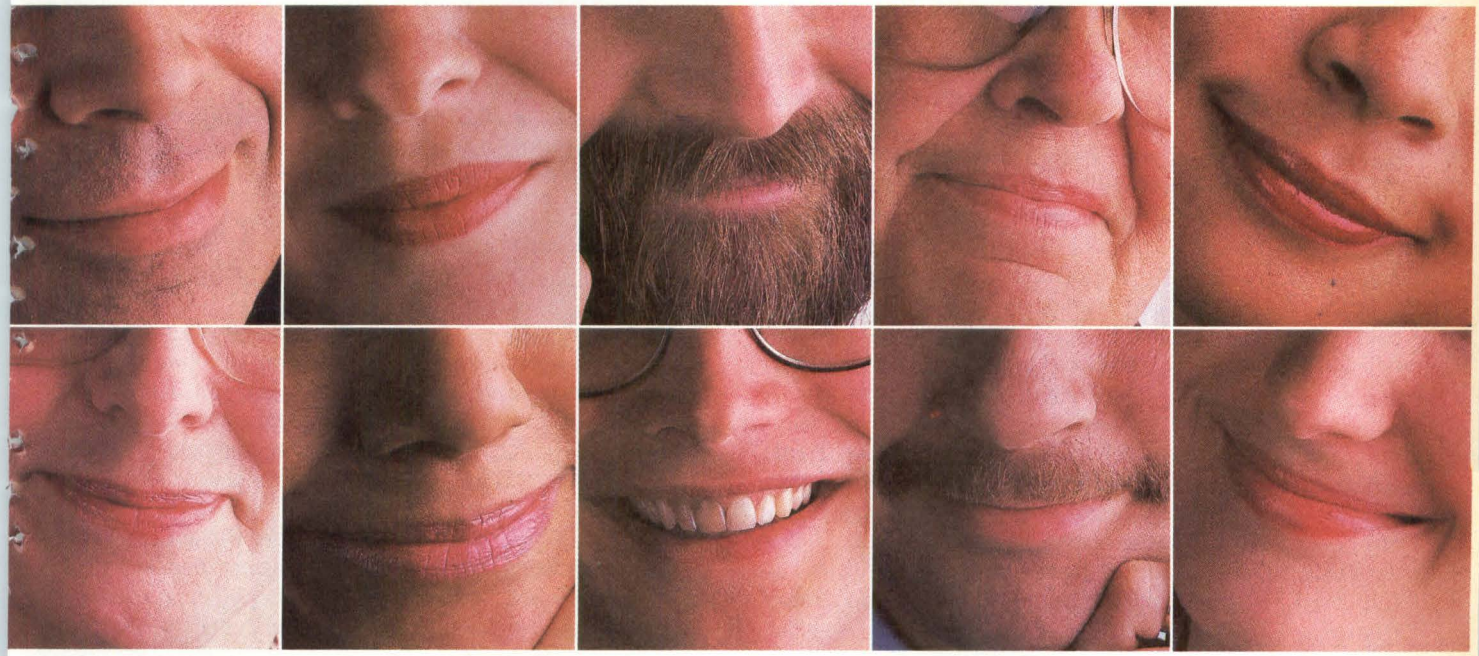

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introduced its Generator Development Tools (GDT), which runs on computers from Apollo and Sun Microsystems. The L-Language (**Figure 6**), like VTI's VIP, allows IC designers to write customized module generators. However, unlike VIP, L is an object-based language that describes ICs in terms of either circuit components, such as transistors, wires and terminals, or geometric elements, such as polygons, rectangles and lines. VIP users, in contrast, must work at the abstract geometric level because the language describes only geometric elements.

GDT includes a technology file, so compilers can be written for any fabrication process and any set of design rules. Technology-independent generators can also be written if fixed dimensions are replaced with variables and symbolic names.

In addition to the L-Language, designers can describe compilers graphically via the L-Editor. L-Editor permits the manipulation of all geometric and electrical objects. It is also the primary means of viewing the output of generators written in L. Modules entered graphically with the L-Editor are automatically converted to the L-Language. An interactive rule checker (design and electrical) is also included in the L-Editor. The rule checker graphically marks the location of a design rule error and provides an accompanying textual description. Block diagrams, schematics and layouts can be drawn, simulated and rule-checked together in the L-Editor. And similar to systems from SCI, VTI and SST, once a module generator is complete, the end-user accessing that module fills out a form to parameterize the function (**Figure 7**).

A set of routers and the L-Simulator, an event driven logical simulator, are also part of the GDT environment. L-Simulator can mix switch-level simulation with functional simulation of large blocks. For timing analysis, GDT translates netlists to SPICE format. When building module compilers, IC designers simply specify the netlist and GDT automatically determines which router to use. GDT has four routers: channel, river, bus and switchbox; placement can be either interactive or automatic. The GDT software is priced at $75,000.

Another firm offering a product to create module generators is SDA Systems. With SDA's Array Compiler, designers can develop generators to synthesize structures including RAM, ROM, PLAs, ALUs, shifters and multipliers. Generators are

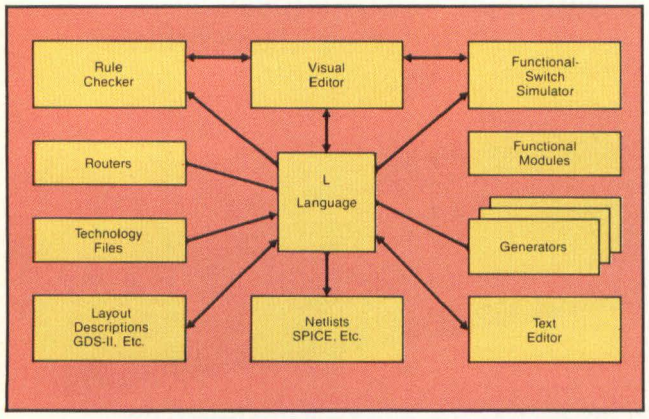

Figure 6: SDL's Generator Development Tools (GDT) environment enables IC designers to develop customized module generators (i.e., cell compilers) for systems applications. Module generators are programs that produce mask geometries and circuit netlists from input specifications. The L-Language supports both geometric objects and electrical objects.

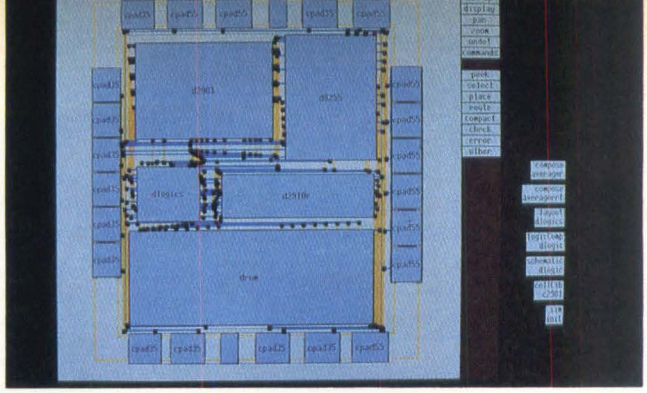

Figure 5: A system designed using VTI's silicon compiler consists of a 2901 bit-slice processor, a 2910 sequencer, a programmable I/O device, ROM and random logic. The 2901 datapath compiler and the logic compiler are two recent additions to VTI's cell compiler library. The 2901 compiler offers expandable bit-slice widths from 1 to 16 bits.

created through the use of array-structure templates, master cell libraries and a personality matrix. An array-structure template is a parameterized block diagram of the module under construction. All generic structural information that is not technology dependent is stored in the array-structure template. The personality matrix defines which cell is to be placed at each location in the template.

When using the array compiler, users fill out the parameterized template and the personality matrix. Then, to further optimize the module generator, the array compiler accepts procedural statements that conditionally manipulate the elements within the array. In effect, the procedural statements are used to generate a new personality matrix. SDA's Array Compiler, which is only available as part of the firm's full custom IC design system (ChipEdge), sells for $120,000.

Metalogic takes a completely different approach to silicon compilation. Metasyn, the firm's turnkey silicon compiler, accepts a behavioral input rather than a structural input. This input description is in the form of an algorithm. Designers using behavioral silicon compilers require no hardware design experience. And Metalogic claims that only moderate programming ability is needed to use Metasyn.

Metasyn is based on MacPitts, a silicon compiler developed at MIT's Lincoln Laboratory (Lincoln, MA). The behavioral description is similiar to a bit-slice microcode program. However, unlike a microcoded bit-slice machine, a Metasyn algorithm is not confined to a fixed target architecture. Instead, the compiler generates the particular hardware defined by the behavioral description. Metasyn can generate architectures with an unlimited number of buses, but only a single datapath. Although CMOS capability is planned for the future, Metasyn generates only NMOS circuits and is design-rule dependent.

Also included with the compiler is a set of performance analysis tools that provide simulation and predict the chip's maximum clocking speed. Presently, Metasyn and the accompanying support tools are available under a 6-month beta-site agreement for $5,000/month. When the system is ready for production, it will synthesize CMOS layouts and be priced at $185,000.

Silicon Compilation: A Technology Based On Marketing

Silicon compilcation technology comes in various shapes, sizes and forms. There are structural silicon compilers, behavioral silicon compilers, systems that have some structural compiler characteristics, systems that have certain behavioral compiler characteristics and systems that have a little of both. There are

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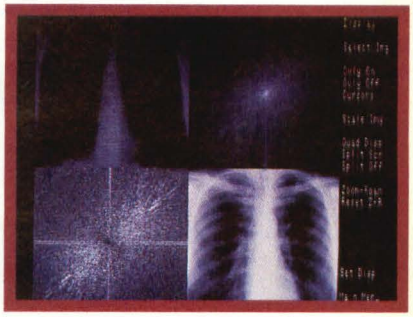

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Circle 40

also languages to build silicon compilers, cell compilers and module generators. The technology, or rather the names given to it, can be confusing. Consequently, the term silicon compiler has been criticized because manufacturers offering very different products position their systems as silicon compilers. To combat the confusion, at least one company, Metalogic, is planning on repositioning its product, Metasyn, as something other than a silicon compiler.

On another front, vendors such as Silicon Compilers Inc. and Seattle Silicon contend that hardware designers do not want to use behavioral compilers like Metasyn. According to those companies, a behavioral compiler does not satisfy designers' need because it does not permit them to manipulate familiar hardware structures. Metalogic, however, maintains that its product is exactly what true system designers want: a tool that allows them to concentrate on the system's function rather than the hardware implementation. Moreover, the company contends that engineers who have written microcode would feel just as comfortable working in the Metasyn environment.

Aside from the duel between behavioral and structural vendors, turnkey silicon compiler companies such as SCI may soon be competing not only with other turnkey vendors, but also with semiconductor foundries. Until now, silicon compiler technology was only available from a few companies. However, tools from vendors like Silicon Design Labs permit IC designers

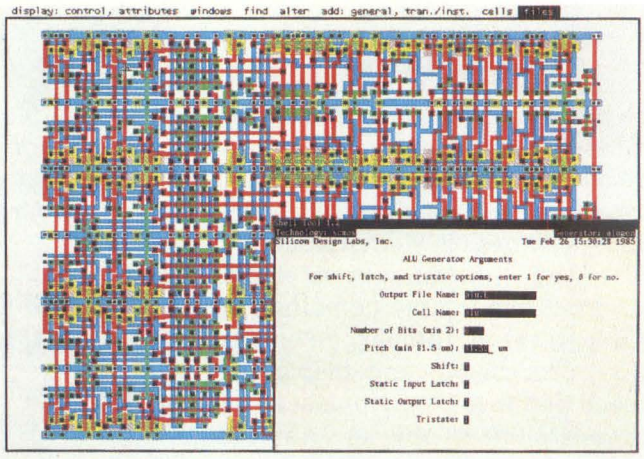

Figure 7: Shown is an ALU generator developed with SDL's Generator Development Tools. To synthesize a module, system designers fill out a form that parameterizes the function. GDT is primarily for IC designers, but SDL plans to introduce tools for system designers as well.

to develop their own compilers. And since the concentration of IC designers is in the foundries, it is natural to conclude that many semicustom IC vendors will soon offer compiler technology. Moreover, semiconductor vendors will have further incentive to adopt compiler technology because it will round out their semicustom product lines. DD

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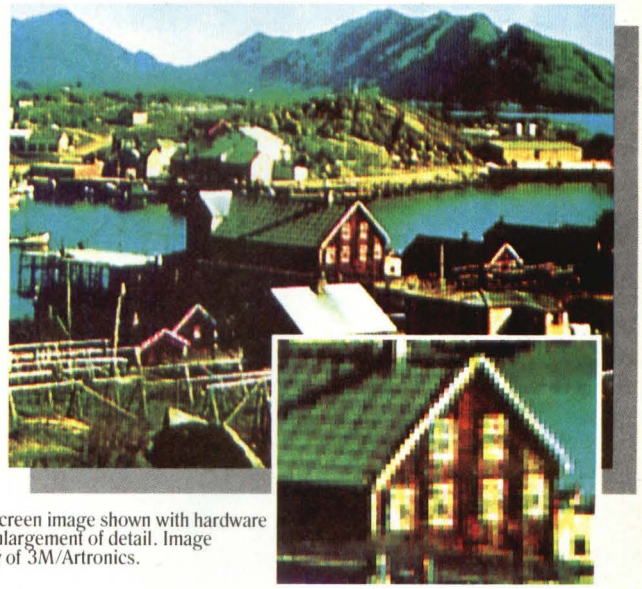

Actual screen image shown with hardware zoom enlargement of detail. Image courtesy of 3M/Artronics.

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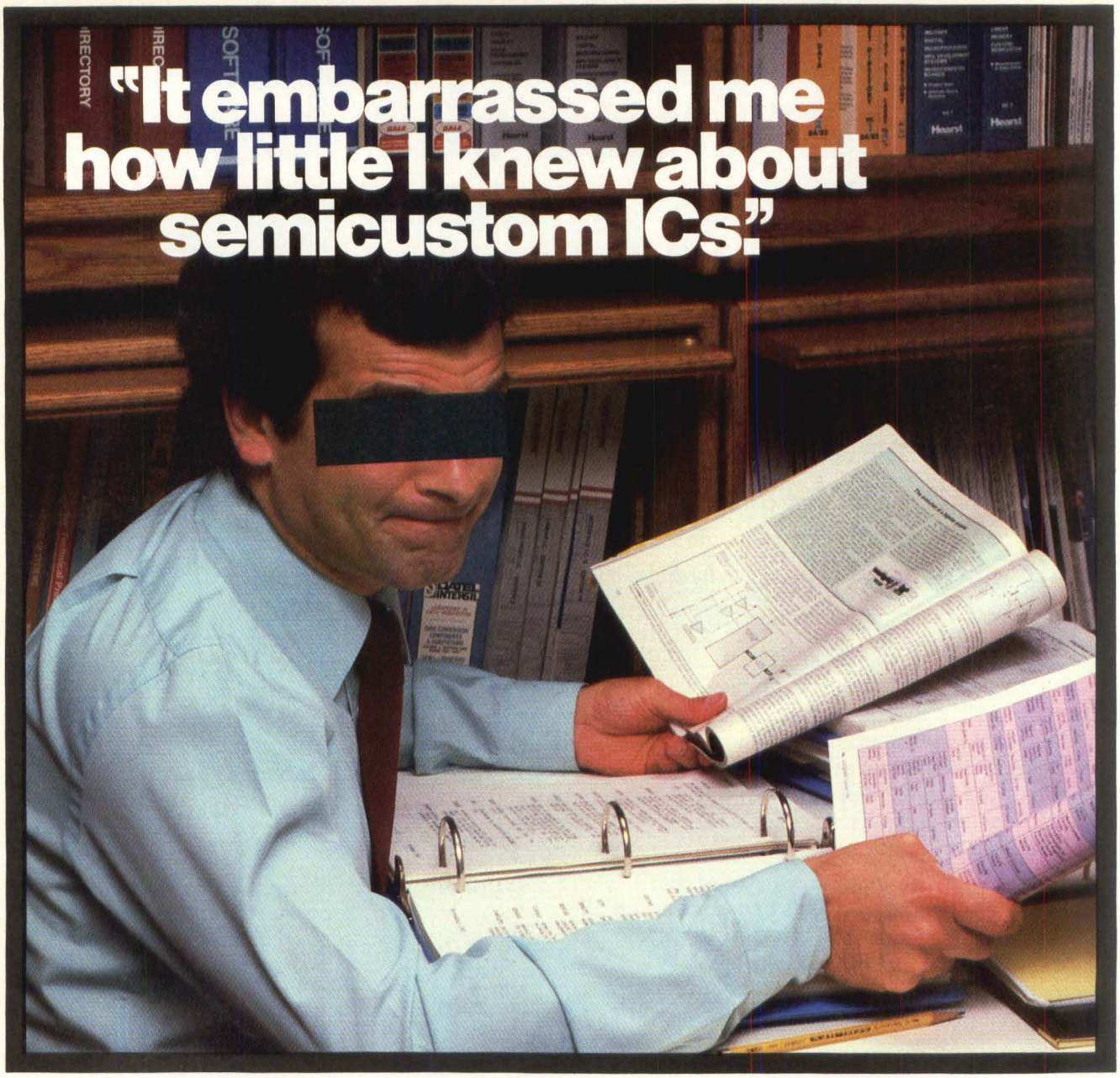

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PART 2

Erasable Programmable Logic Devices Implement A Variety Of Functions

by Clive McCarthy, Altera Corp.

Engineers can quickly design digital circuits with erasable programmable logic devices (EPLDs). This second installment in a two-part series describes the design process; part 1, which appeared in *Digital Design*, August 1985, focused on the technology and internal structure. Using today's development tools, designers can enter a schematic or netlist description of the circuit, and the software will automatically convert it into a form suitable for an EPLD. With Altera's solution, a programming unit attached to the IBM PC or compatible lets users program the EPLD immediately. The whole design process is streamlined—from creating a circuit to making any needed changes in the device program.

As described in part 1, an EPLD is an AND-OR array composed of EPROM transistors. Designers program this array to create the desired digital logic function. Although most of the EPROM array's programming bits implement combinatorial logic functions such as AND, NAND, XOR and NOR, a few bits are used to configure the architecture of the chip. For instance, several bits might control feedback paths and flip-flop connections.

Altera's EPLDs are divided into sections called macrocells. **Figure 2**, a macrocell from the EP1210, shows how the EPROM array feeds a sum-of-products signal to the flip-flop. However, the signal does not have to go to the flip-flop. By programming an appropriate bit, designers can route the sum-of-products through a multiplexer and to an I/O pin or through a latch and to another multiplexer that can then feed the signal back into the EPROM array. With this feedback flexibility, designers can connect the signal to the input of another macrocell. Different programming choices configure the EPLD to perform various functions.

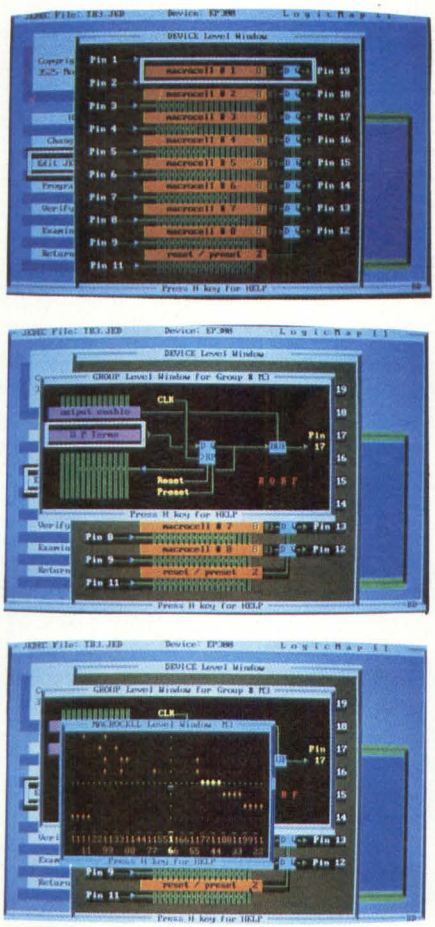

Figure 1: Altera's LogicMap software allows users to examine and change an EPLD's program in three levels of detail: (a) the structure of the EPLD's overall blocks, (b) its macrocells in block form and (c) its macrocells in matrix form.

The elements shown in **Figure 2** comprise only a small section of the EP1210. It has 28 macrocells, including four buried state registers, for an equivalent gate count of more than 1200 gates. To increase design versatility, EPLDs such as the EP1210 incorporate buried registers and a programmable clock option. The buried registers do not connect to I/O pins; instead, they serve as internal feedback elements and thus conserve the flip-flops in I/O cells for functions that must connect to I/O pins. The programmable clock permits the designer to select the clocking signals that enable the EPLD's input latches and flip-flops.

Automated Design Support

Despite the myriad configuration options offered by EPLDs, it is not necessary for the designer to manually choose how each bit will be programmed. Altera's A+PLUS development software automatically fits a design into a given EPLD. The only element of the EPLD development process (**Figure 3**) that demands a great deal of attention from the designer is entering the design.

To accommodate a wide range of design needs, A+PLUS provides three ways to enter a design: schematic capture, Boolean equation entry and netlist entry. The first two methods are accomplished through a CAE program that does not require the user to learn special EPLD methods; a graphics-oriented program allows netlist entry. The user can choose either Personal CAD Systems' (San Jose, CA) PC-CAPS or FutureNet's (Chatsworth, CA) DASH-2 for design entry, and both programs work as they would for any type of circuit design.

Unlike a conventional TTL circuit design, an EPLD design using A+PLUS involves special output configurations. For

schematic capture, these appear in the A+PLUS device library as preconfigured elements whose parts consist of common logic symbols such as NAND, NOR, AND, XOR and flip-flop. A mouse can be used to select these elements from an on-screen menu and place them anywhere in the circuit. The designer is not burdened with how the EPLD will be programmed to make the design possible.

In some cases it is easier to specify a logic function with Boolean equations than to create the actual circuit. In these instances, logic equation macros are combined with other schematic elements in the same diagram or block. The designer specifies only the number of inputs and outputs the blocks should have. The appropriate Boolean equations are then entered to define the functional relationships among the block's I/O lines. A+PLUS then treats this block as it would any other logic function.

The third alternative for entering a design is to specify a netlist. This is especially useful when a hand-drawn schematic has already been created on paper. An A+PLUS program, NetMap, simplifies this entry job by using graphic logic symbols and prompting the user for each input in a circuit. For example, if a 4-input NOR gate is specified, NetMap displays the symbol and prompts the user for input and output connections.

Automatic Functions Assume The Implementation Burden

Once the circuit is entered into the development system, the designer's task is virtually complete. A+PLUS automatically optimizes the design via logic minimization techniques and matches the design's requirements with the EPLD's architecture. Software then converts the design to a JEDEC file that drives an EPLD programming unit. The designer can opt to control the minimization step if special circumstances make this necessary, but otherwise the software handles the entire process.

The minimization procedure converts combinatorial logic to sum-of-products form, then reduces that form to its simplest logical equivalent. Any combinatorial logic can be reduced to a two-level equivalent if the available gates have enough inputs. The effective AND gates configured by an EPLD's EPROM array have an enormous number of inputs, 64 in the case of the EP1210.

Logically inverting functions through the automatic application of de Morgan's theorems also aids the minimization process. For example, a 12-input OR is logically equivalent to a 12-input AND whose output is inverted. Because an EPLD permits the output polarity to be selected, the OR function is defined by merely inverting the AND. The benefit in considering the inverse function is that a 12-input OR might not be available in a target EPLD, whereas 12-input AND gates would be abundant.

The obvious advantage of minimizing logic to a two-level sum-of-products form is that the functions can match an EPLD's structure. Moreover, the procedure reduces the number of gate delays a signal encounters. For example, if a designer creates a circuit using four levels of gates and minimization reduces the circuit to two levels, the total propagation delay has been cut in half.

Although the form of the design after minimization matches an EPLD's structure, fitting the design into the EPLD is not necessarily a trivial undertaking. To use the EPLD's resources efficiently, the software must try a variety of layouts. Because some macrocells have more product terms than others, A+PLUS attempts to fit small functions into macrocells with fewer product terms. I/O pin requests made by the designer may limit the program's layout choices.

When the fitting is complete, the software translates the results into a standard JEDEC programming file. A+PLUS

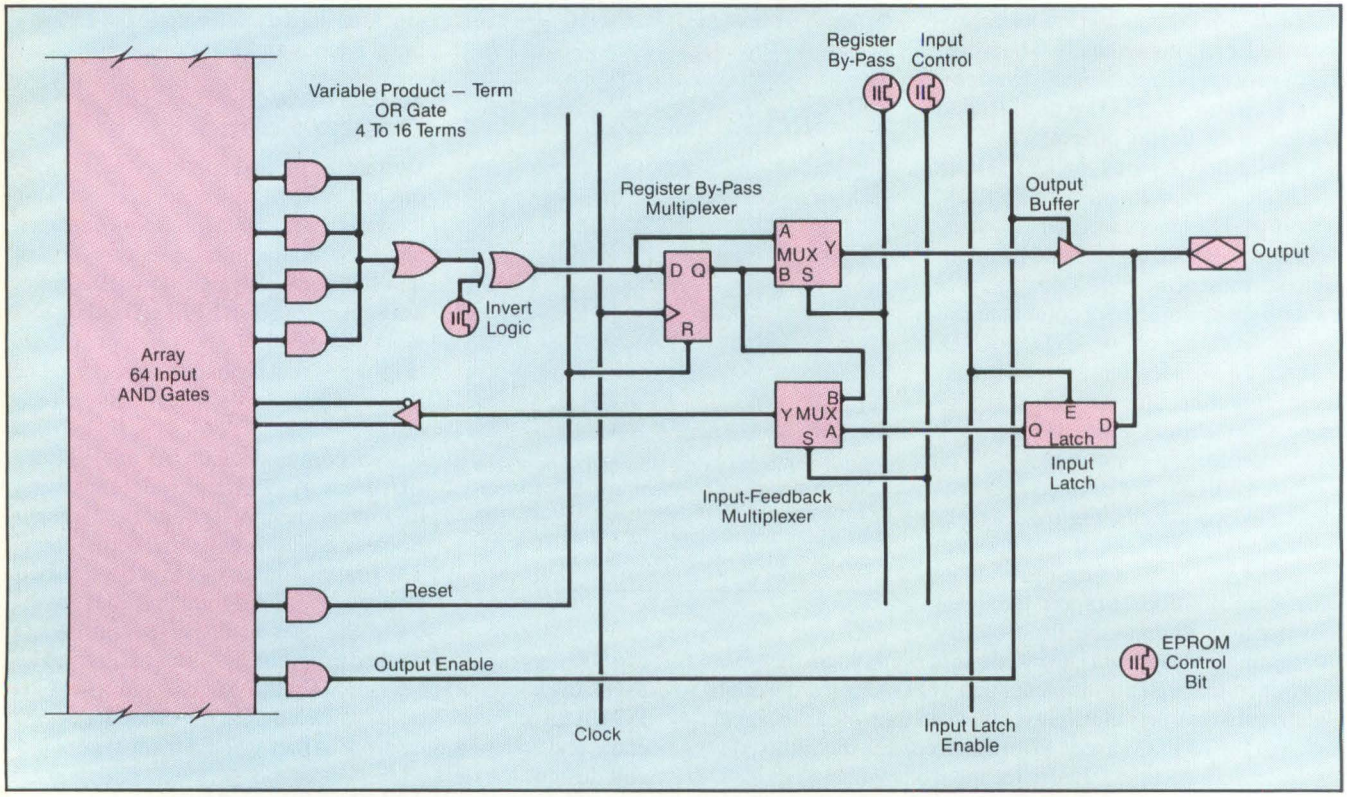

Figure 2: One macrocell from Altera's EP1210 erasable programmable logic device (EPLD) shows the versatility provided by such devices. The programmable features shown here include the polarity of the signal from the AND-gate array, the use of the flip-flop and the feedback path.

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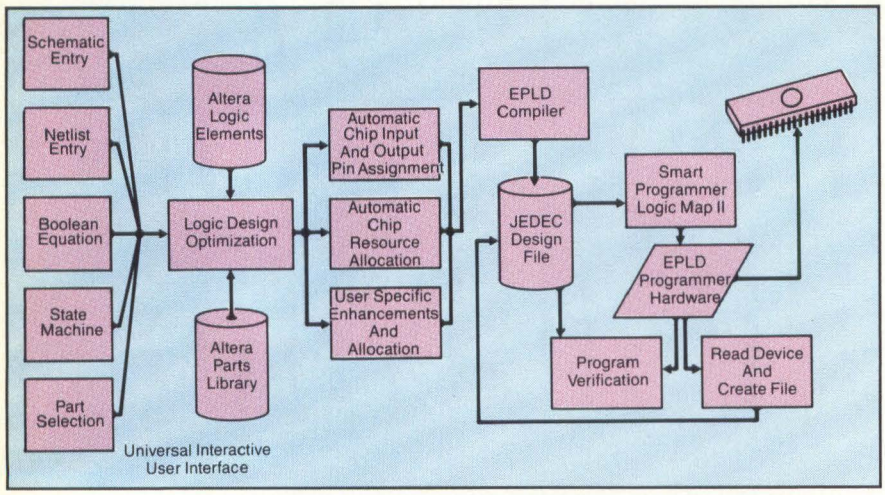

Figure 3: The development process for an EPLD encompasses the steps shown here. Altera's A+PLUS software package automatically handles all the steps after design entry. After the design is entered, the entire sequence usually takes only a few minutes.

simultaneously generates a utilization report that describes how the EPLD's resources have been used. The report includes a pin layout for the device and a list of used and unused resources—information that can be used by the engineer to determine whether it is practical or possible to add more functions to the design. Run on a partially completed schematic, A+PLUS will also determine whether the design fits in a specific EPLD.

Users who want a more interactive way to view the EPLD implementation can employ a program called LogicMap II. Its primary purpose is to program the parts, but it also reads a JEDEC file and graphically displays the configurations of the EPLD's macrocells. Working at three levels of detail, designers can see the structure of the EPLD's overall blocks, its macrocells in block form and its macrocells in matrix form (**Figure 1**). LogicMap also permits changing of the design at this bit level, a capability that is especially useful for reading and revising the contents of a programmed EPLD.

The hardware needed to perform all development steps is an IBM PC or compatible computer; with a programmer, the system can implement the EPLD immediately. A+PLUS simply downloads the JEDEC file to the programmer. Although the entire A+PLUS implementation process encompasses many tasks, it usually requires only a few minutes from start to finish. Minimization and design fitting can take longer in some cases.

Testing Considerations

A primary benefit of erasable technology is that it permits complete testing of all devices by the manufacturer. This is a sharp contrast to fuse-programmable PLDs, which cannot be fully tested because of the destructive nature of programming. Since fuse PLDs cannot be erased and reprogrammed, it is impossible to know ahead of time whether any specific bit will program correctly. One consequence is that the testing burden falls primarily on the shoulders of the device programmers. Each time engineers create new designs using these parts, they must also generate test vectors. On the other hand, after an EPLD has been tested by programming, the device can be erased and thus made ready for normal use.

Because EPLDs have been thoroughly tested by their manufacturer before shipment, it is not necessary to perform extensive testing after programming. At the factory, the devices were programmed with a generic test pattern that allows all possible data paths and circuit blocks to be checked, and functional AC and DC parameters have all been verified. The only EPLD tests left to the user are functional testing and verification of circuit pattern programming. Some functional testing can be done before the device has been programmed by using Altera's optional simulation program. And pattern verification is done automatically by the programming unit.

Circuit Design Examples

To see how EPLDs can be used in a variety of applications, consider two examples: replacing general-purpose TTL parts and replacing bipolar PALs*. The ability to implement the same functions as discrete TTL devices underlies EPLDs' usefulness in all applications. An EPLD not only implements TTL-equivalent gates; it does so with equivalent performance. The CMOS EPLDs achieve TTL propagation speeds. Keeping signals internal to an EPLD instead of routing them between

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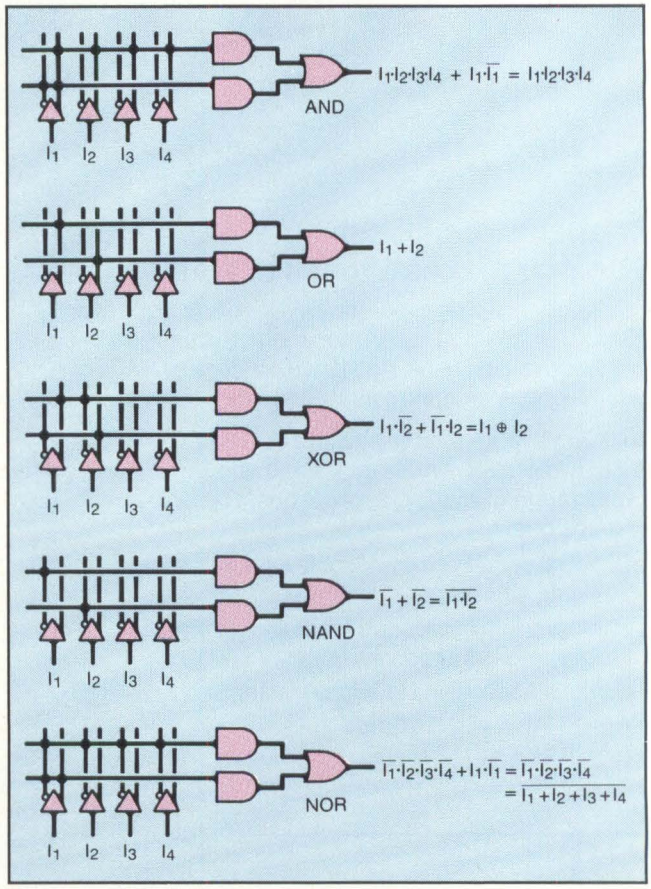

Figure 4: An EPLD's AND array can implement all five basic logic functions. A dot in these matrix diagrams indicates an EPROM cell that completes a circuit between the crossed lines.

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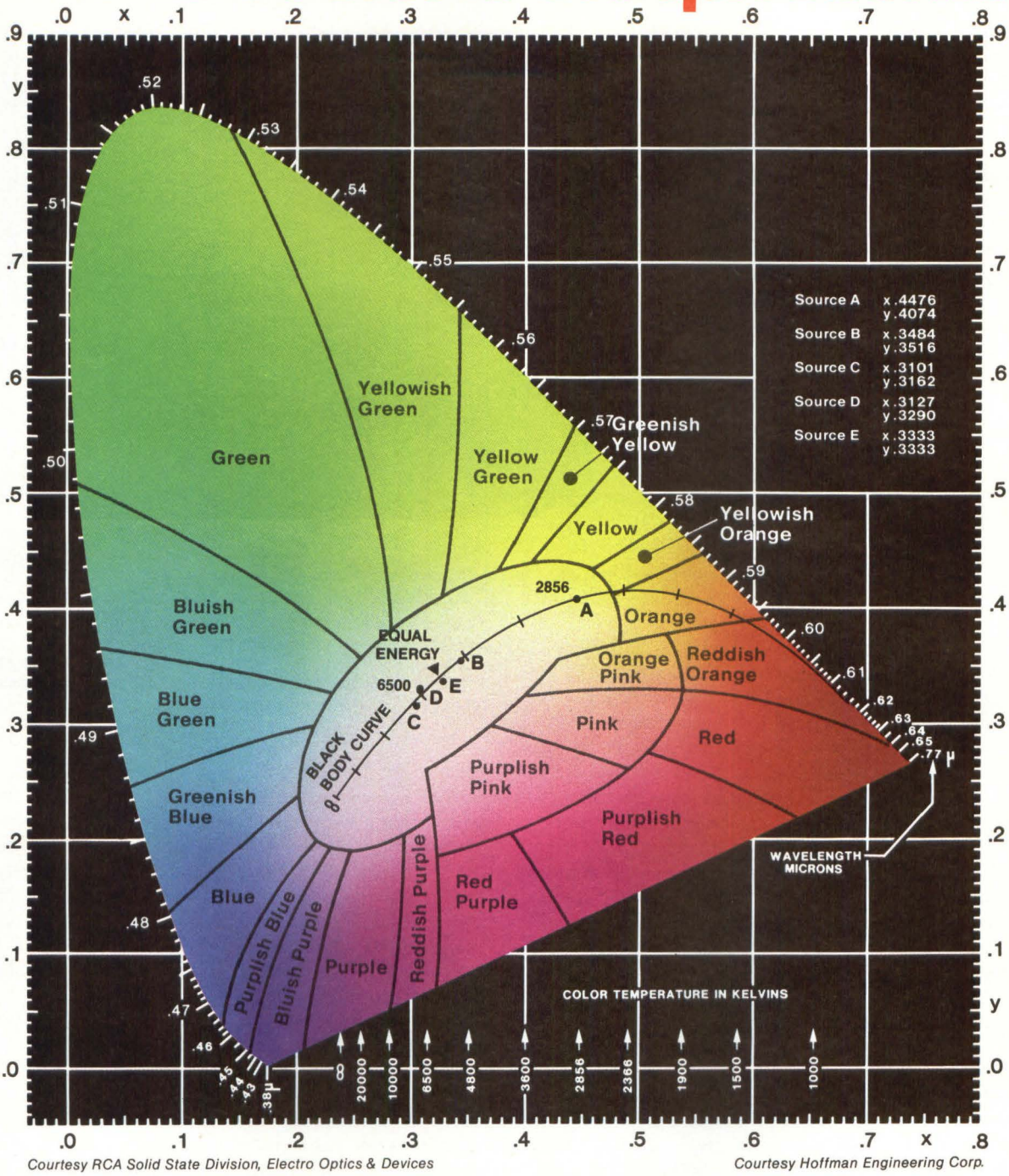

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discrete TTL devices also reduces propagation delays.

A major EPLD advantage over TTL is that only a few EPLDs need to be inventoried to implement a large number of logic functions. When an application demands a specific function, an off-the-shelf EPLD can be programmed in minutes. In contrast, keeping a comprehensive inventory of TTL-based logic functions demands that users stock dozens of different device types.

EPLDs implement a variety of logic functions using their sum of products matrix and selectable inversions. **Figure 4** illustrates the formation of the five basic logic functions. The unused product terms in the AND and NOR are programmed to always equal ZERO, and the NAND and NOR use logical inversion to create functions whose final outputs are inverted. In EPLDs such as the EP310 and EP1210, which permit output inversion, it is not always necessary to use logical inversion to implement NANDs and NORs; **Figure 5** shows another possible approach.

More complex logic functions are implemented by using feedback within the EPLD. For example, an EP310's D-type flip-flop can emulate any other type of flip-flop by using feedback to an appropriate combinatorial logic function (**Figure 5**). Each of the four types has a different feedback configuration in the device's I/O cell.

The same versatility that allows an EP310 to implement a wide variety of logic functions gives the device the ability to replace all commonly used 20-pin PALs. As with TTL replacement, EPLDs offer the advantage of stocking one generic device to perform the same function as 18 different PALs. There are also functional benefits to using the EPLD such as synchronous set and preset and performance advantages such as lower power consumption. Finally, unlike the fuse-programmable parts, EPLDs can be erased and reprogrammed.

Implementing most of the 20-pin PALs is a simple matter of programming the EP310's I/O cell to provide a nonregistered connection from the memory array to the output pins. Selectable output inversion gives the EPLD a great deal of flexibility in these functions. The ability to program the EP310 to provide registered functions allows this device to implement all the remaining output configurations offered by 20-pin PALs.

Future Developments

Where do EPLDs go from here? An obvious answer is that they will incorporate increasing numbers of gates. Currently available devices already provide more than 1200 equivalent gates, and that number will probably increase to 3000 gates over the next few years.

Probably more exciting than the sheer numbers of equivalent gates is the increasing versatility of EPLDs. Future architectures will make the gates in the devices more useful. For example, instead of using feedback to the EPLD's memory array to configure flip-flops, EPLDs will provide flip-flops that can be programmed to directly act as D, J-K, T or S-R types.

In performance areas, future EPLDs will improve in both speed and power consumption. Using proven CMOS technologies, shorter propagation delays will result, and ongoing refinements in feature geometries promise continued speed improvements. As for power consumption, expect EPLDs to reach the "zero-power" standby level offered by some EPROMs. Attaining this in EPLDs is more difficult than in EPROMs because the EPLDs' programmable architecture must stay "awake" and ready for an input even in standby. This barrier can be overcome with the result that zero-power EPLDs will be able to operate at TTL speeds with miniscule amounts of current.

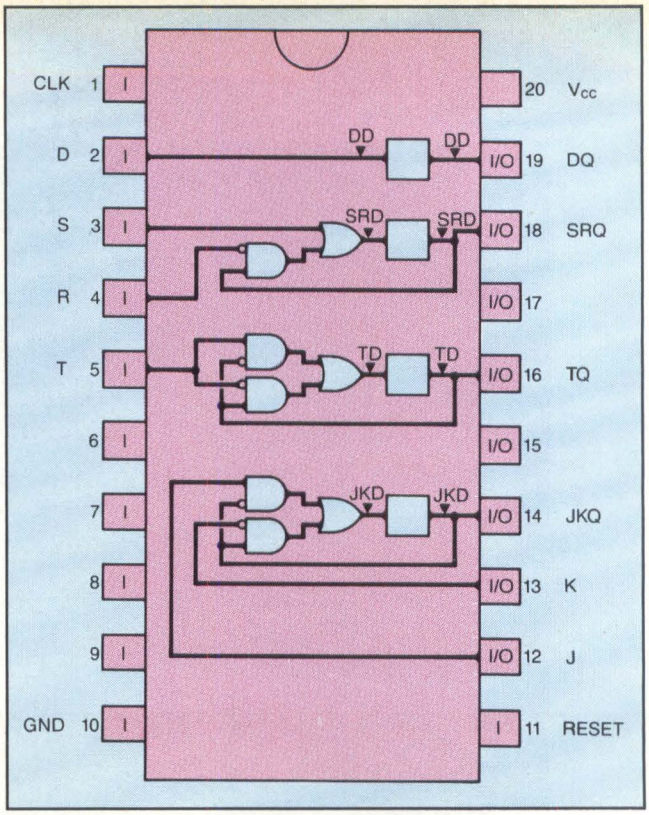

Figure 5: In addition to versatility in implementing combinatorial logic, EPLDs can configure their D flip-flops as any other type by using appropriate feedback functions. The type of feedback required for each flip-flop type is indicated here by the DD, SRD, TD and JKD notations. TD, for example, denotes registered feedback.

The benefits offered by erasable CMOS technology have become obvious even to bipolar PLD manufacturers; some are expected to introduce CMOS devices of their own. In coming years, EPLDs will take over bipolar PLD applications as EPLD benefits such as lower cost, lower power consumption and greater versatility become more widely known.

The impact of EPLDs on logic design cannot be overestimated. The heretofore unheard of ability to program a circuit design into a single device in a few minutes has changed the way designers must think about logic functions. These functions are no longer represented by discrete devices that are taken off the shelf and wired into a circuit board; they are symbols that can be manipulated at will and made physical only when required.

Alternatives such as gate arrays promise the same capability, but the up-front expense and long development time associated with semicustom and full custom devices limits them from some applications. In today's fast-changing market, logic devices must meet designers' requirements for fast turnaround and the ability to modify designs easily in the face of evolving needs. EPLDs offer an elegant way to meet those requirements. DD

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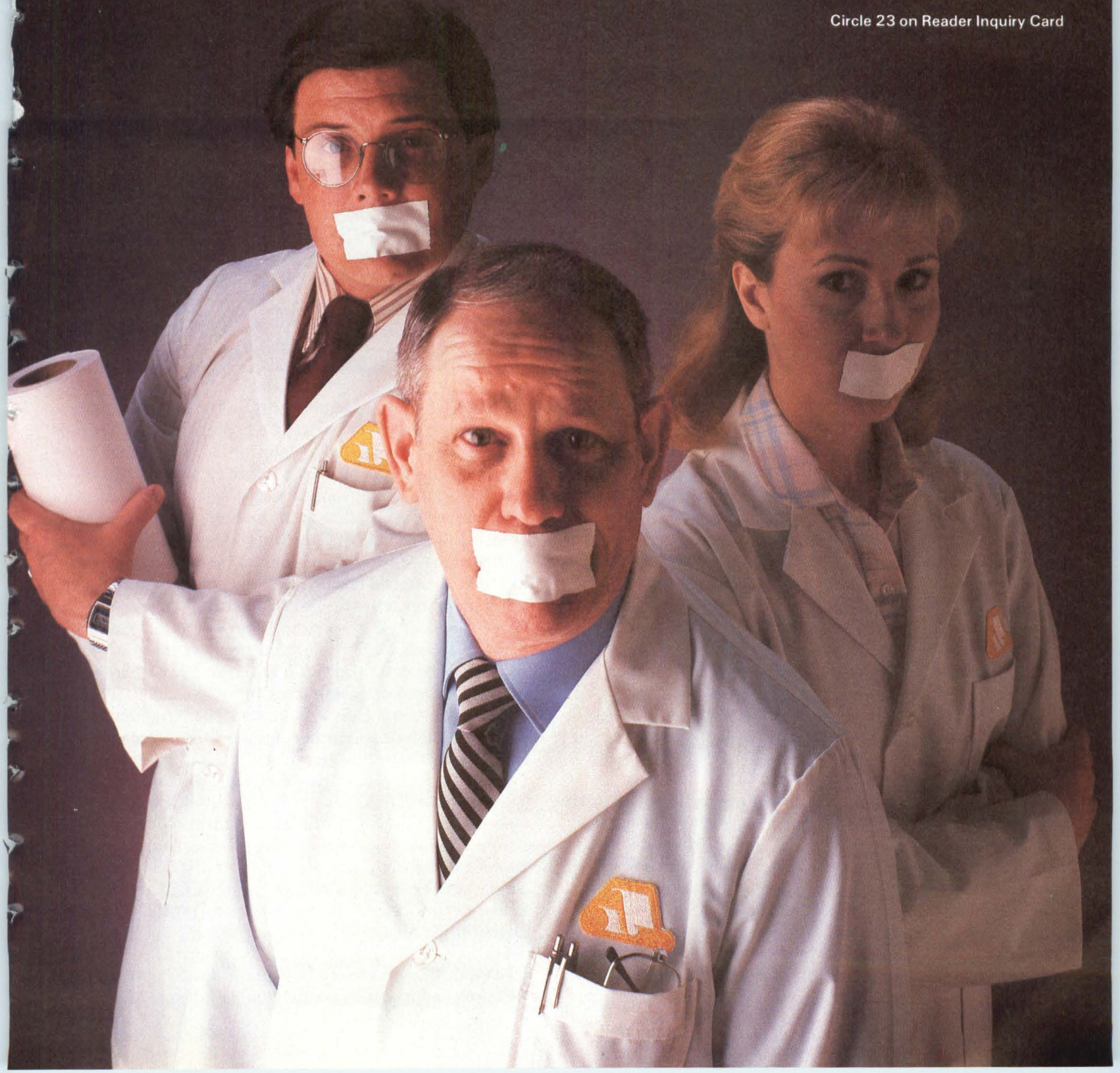

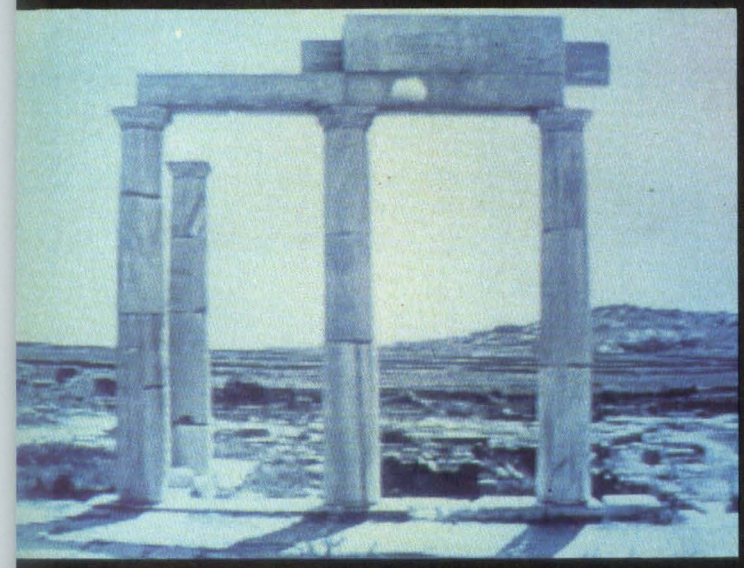

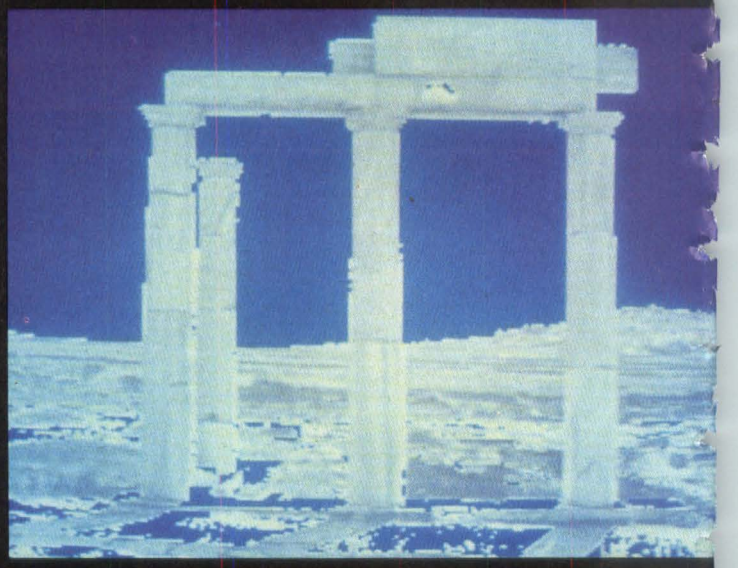

Electronic Imaging '85:

by Andrew Wilson, Sr. Technical Editor

When the second International Electronic Imaging show opens its doors next month, over 2500 attendees will view over 400 products packed into 150 booths. The show, to be held October 8-10 at the Boston Sheraton, will feature products ranging from image capture devices, image processors and image displays. At the same time, the Electronic Imaging conference will discuss the latest developments in imaging technology. Cosponsored by the IGC, SPSE and *Digital Design*, the conference will be divided into technical and application sessions. The technical papers will cover design philosophies and the application sessions will range from intelligent vision systems to medical imaging systems. Coupled with the conference, 12 three-hour minicourses will include solid-state image sensors, flat-panel displays, optical disks and image processing.

Image Capture

Probably the most important element in any imaging system is the component used for detecting an image. Over the last few years, detector technology has been moving from tube-based to solid-state designs. The reasons for this change have been the poor spatial fidelity, grey scale quality and low-resolution of tube devices.

For applications in remote sensing instruments, RCA Advanced Technology Labs (Moorestown, NJ) will discuss a buttable four spectral-band (4 × 5120) linear format CCD and a buttable, two spectral band (2 × 2560) linear format short-wave IR CCD, developed under NASA funding. According to the author, J. Tower, the visible CCD provides high S/N ratio and a high MTF in the red region. And the SWIR device provides high uniformity and excellent MTF in the SWIR band.

A 64 × 64 frame transfer image sensor, developed for machine vision applications, will be described by George Brody of RCA (Lancaster, PA). The pixel size is 20 × 20 microns in both imaging and storage regions, allowing imaging on both registers for strobed imaging or for integration times that are very long compared to the field readout time. A second frame transfer device will be presented by Toshihiro Furasawa of Sanyo Electric's VLSI Manufacturing Division. The device which will be described is a 600 (H) × 502 (V) area array capable of television-quality resolution.

Philips Research Labs (Eindhoven, The Netherlands) will describe a high-density frame transfer CCD, which was first announced at the International Electron Devices Meeting in San Francisco last year (*Electronic Imaging*, February 1985, p. 12). The "Accordion" CCD has a 588 × 604 resolution and is available in color (NXA1020) or monochrome (NXA1010). The design allows the number of vertical direction pixels to be doubled without any increase in chip size. This is achieved by a transport mechanism which enlarges the CCD cells from two to four electrodes (analogous to the stretching of an accordion). Digital shift registers drive this mechanism.

For applications in X-ray and UV imaging, a 32 × 32 element CCD with 28 μm pitch sensors has been developed at the Naval Research Laboratory in Washington, DC. In operation, back-

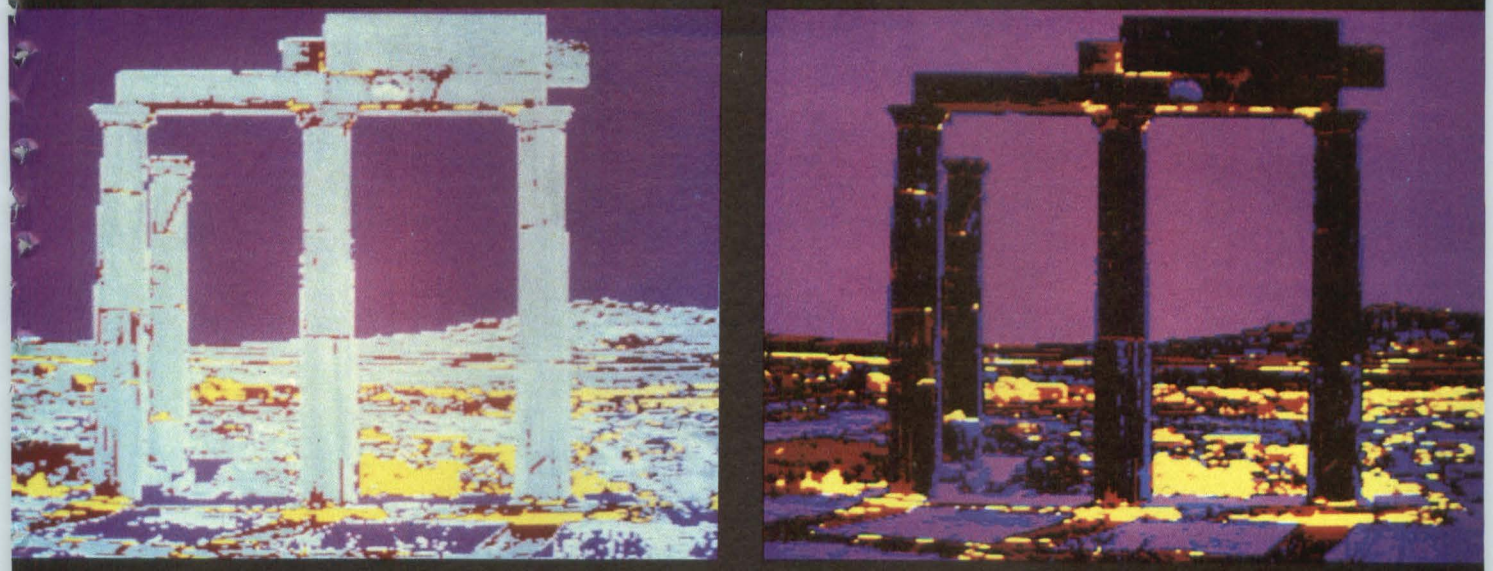

Figure 1: Image processing with personal computers. The photographs show a series of images generated by the DT2803 frame grabber from Data Translation.

Digitizing The World

side illumination is necessary because the UV photons have a small absorption length in silicon of about 100A. In frontside illuminated CCDs, these photons are absorbed in the polysilicon and oxide layers covering the substrate. As this does not occur with backside illuminated CCDs, good quantum efficiency is obtained in both the UV and the soft x-ray region.

Very large format multimode imagers will be the subject of a paper from Texas Instruments (Dallas, TX), which were originally announced at last year's IEDM. Representatives from TI will describe the development of a prototype CCD imager which features a format of 800 × 800 pixels. The device, which can be read through single or dual output, can be read as a single full-frame 800 × 800 image, as two full-frame 400 × 800 images, as a frame transfer 800 × 400 image or as two full-frame transfer 400 × 400 images. TI claims it has demonstrated a fast parallel transfer rate for frame store operation of 3 MHz with the device. In addition to the devices described, researchers from Oki (Tokyo, Japan), General Electric (Schenectady, NY), Mitsubishi (Itami, Japan) and RCA (Princeton, NJ) will describe advancements in other areas of solid-state sensor technology. On the floor of the exhibit hall, many manufacturers will demonstrate cameras, systems and image capture detectors for a number of applications.

At the Pulnix America (Sunnyvale, CA) booth, a range of cameras will be demonstrated, including the TM-34K and 36K series of interline CCD-based products. Specifications for the cameras include 384 × 491 detectors, RS-170 output, 280 × 350 (V) resolution and a minimum illumination of 3 lux. The company will also show a light-intensified camera, the DN-5034, which can be used in applications requiring either daylight or starlight illumination. A microchannel plate image intensifier is used in the camera which is lens coupled to the CCD camera. Two versions of the camera are currently offered by the company; the DN-5000 series, which includes a control circuit to allow operation from 105 lux to 10-31 lux and the NV-3000, which features a manual gain control and is designed for low-light use only.

A solid-state shuttered camera will be the highlight of the booth at Xybion Electronic Systems Corp (San Diego, CA); the SVC-09 will be shown capturing images as fast as every 1/10,000 of a second. The MOS-based camera features adjustable exposure rates from 1/500 to 1/10,000 of a second and produces standard IV pk-pk, 75 Ohm video output. The company will also show a high-speed, black-and-white camera, an intensified solid-state video camera and a multispectral solid-state video camera.

VSP Labs (Ann Arbor, MI) will show a solid-state based camera using a CCD of 604 × 576 detectors. Because of the high pixel density of this array, a proprietary video circuit was developed by the company to format it into a 1:1 aspect ratio, allowing a true 512 × 512 image to be captured. In addition, the SC500 camera uses a pixel oscillator with synchronization correction circuitry to ensure horizontal pixel positioning accuracy.

Expanding the resolution even higher (albeit by tube-based methods) will be the theme of the product demonstration at the MTI (Michigan City, IN) booth. The company's 65 series of

television cameras, which feature an up-to-1100 line resolution, will be on show along with a range of low-light level television cameras and severe environment television cameras. Whatever the EM region to be scanned, the EI show will provide a forum for both manufacturers and buyers to air their opinions on the state of detector technology.

Once images have been detected, the problem of processing them to extract useful information remains. Therefore, a major part of both the Electronic Imaging show and technical discussions will center on the problem of image processing and pattern recognition as it applies in applications ranging from medical diagnostic imaging to machine vision.

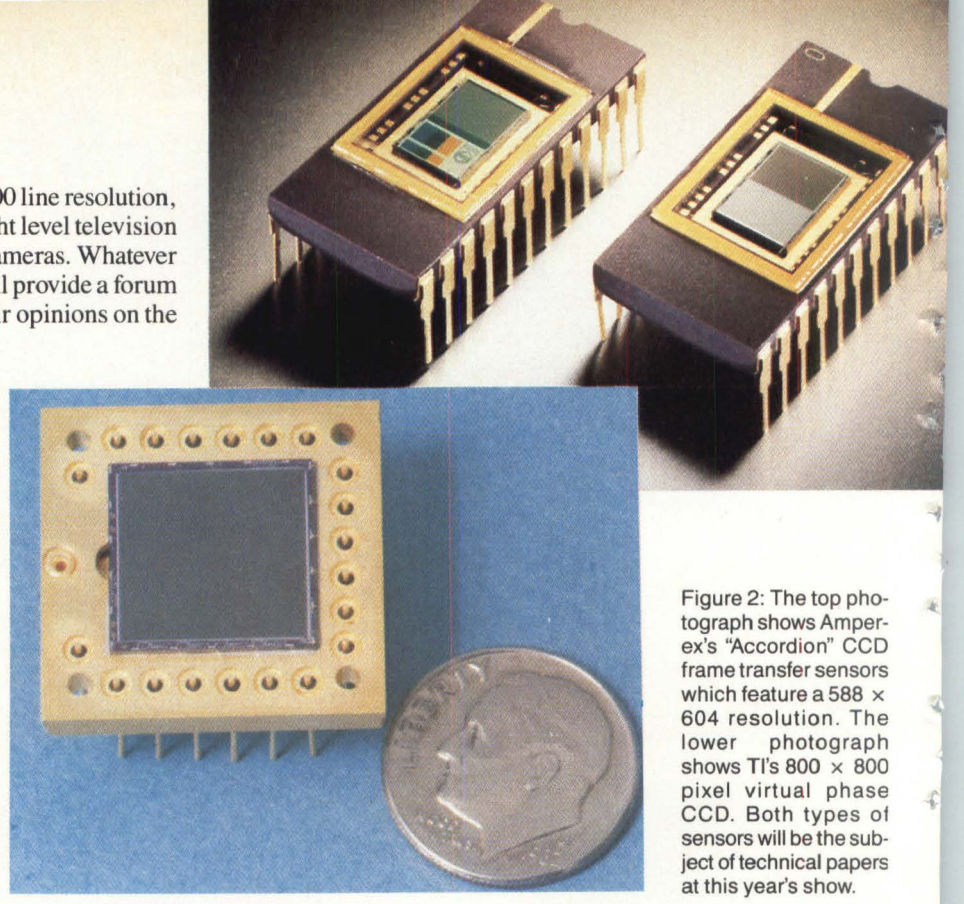

Figure 2: The top photograph shows Amperex's "Accordion" CCD frame transfer sensors which feature a 588 × 604 resolution. The lower photograph shows TI's 800 × 800 pixel virtual phase CCD. Both types of sensors will be the subject of technical papers at this year's show.

Image Processing

Of the 13 technical sessions to be held at this year's show, four will be dedicated to image processing and image processing systems. Application sessions will address the problems of intelligent vision systems, array processors for the VAX and MicroVAX, medical imaging and applications of image processing systems. Subjects covered will range from image processing software to ICs designed primarily for image processing.

Parallel-type computer architectures will be the thrust of many of the papers on image processing as these systems can be used to implement many image processing functions very rapidly. One example of an algorithm inherently suited for multiprocessing is the Burt pyramid which will be described by Roger Bessler of RCA David Sarnoff Research Center (Princeton, NJ). The algorithm provides a band-pass image structured representation similar to that in the human visual system and can be used for television image processing, enhancement and coding and restoration.

Parallel processing will be the theme of a paper from Datacube (Peabody, MA). Dave Erickson and Shep Siegel will explain the benefits of the company's Maxvideo boards (*Digital Design*, June 1985, p. 42). The VME-based boards are composed of Digimax, an analog to digital converter; Framestore, a storage module with three 384 × 512 × 8-bit frame stores on a single VME card; VFIR, a linear pixel processor; SNAP, a systolic neighborhood array processor operating on a 3 × 3 kernal; Featuremax, a real time histogram and feature list extractor and Max-SP, a general-purpose signal processor module.

Implementing an image processor on a chip will be discussed by Mitchell Chase of NEC. Describing the 7281 from NEC (Natick, MA), Chase will discuss how the architecture of the chip differs from traditional von Neumann designs (*Electronic Imaging*, December 1984, p. 42). The chip, the Image Pipelined Processor, employs dataflow techniques on a circular pipeline to avoid the shortcomings of von Neumann machines. Chase will describe image processing systems based on multiple 7281s and provide processing examples.

At Logica (Los Angeles, CA) a high-speed development system for image processing has been developed. Michael Kayat will present details of the company's Vista-IPS image processing software and how specific systems have been implemented using an array processor from Floating Point Systems (Portland, OR) coupled with Logica's frame store.

In another paper, Kayat will discuss an image processing research system designed to help users carry out a multistage development cycle consisting of experimentation, design, assessment and implementation of an image processing algorithm. An example of such a development will be given for an infrared application. Aside for being exhibited on the floor, PC-based image processing systems will be discussed in a paper from Media Cybernetics (Takoma Park, MD). The paper will cover device-independent imaging tools and transportable image formats as well as highlighting the company's own imaging software, Dr. Eye. At the exhibition, many manufacturers will present displays of imaging functions being carried out at high speed. Being one of the target markets for the array processor, no less than seven array processor manufacturers will take to the floor.

Many board-level manufacturers will show imaging boards compatible with Multibus, VMEbus, PC and other formats. Start up Recognition Technology (Holliston, MA) will choose the show to exhibit its range of analog subsystems, digital storage units and pipelined pixel processors for both the VMEbus and Multibus (*Electronic Imaging*, March 1985, p. 14).

Data Translation (Marlboro, MA) will also use the show to introduce a range of VME and Q-bus products, following the success of the company's initial imaging board, the DT2803, an IBM PC-compatible frame grabber which can be used in conjunction with the SKY320PC coprocessor from Sky Computer (Lowell, MA). The new boards consist of a frame grabber for the Q-Bus (the DT2651), an arithmetic coprocessor for the Q-Bus (the DT2658), a frame grabber for the VMEbus (the DT1451), an arithmetic coprocessor for the VMEbus (the DT1458) and two boards for the IBM AT consisting of a frame

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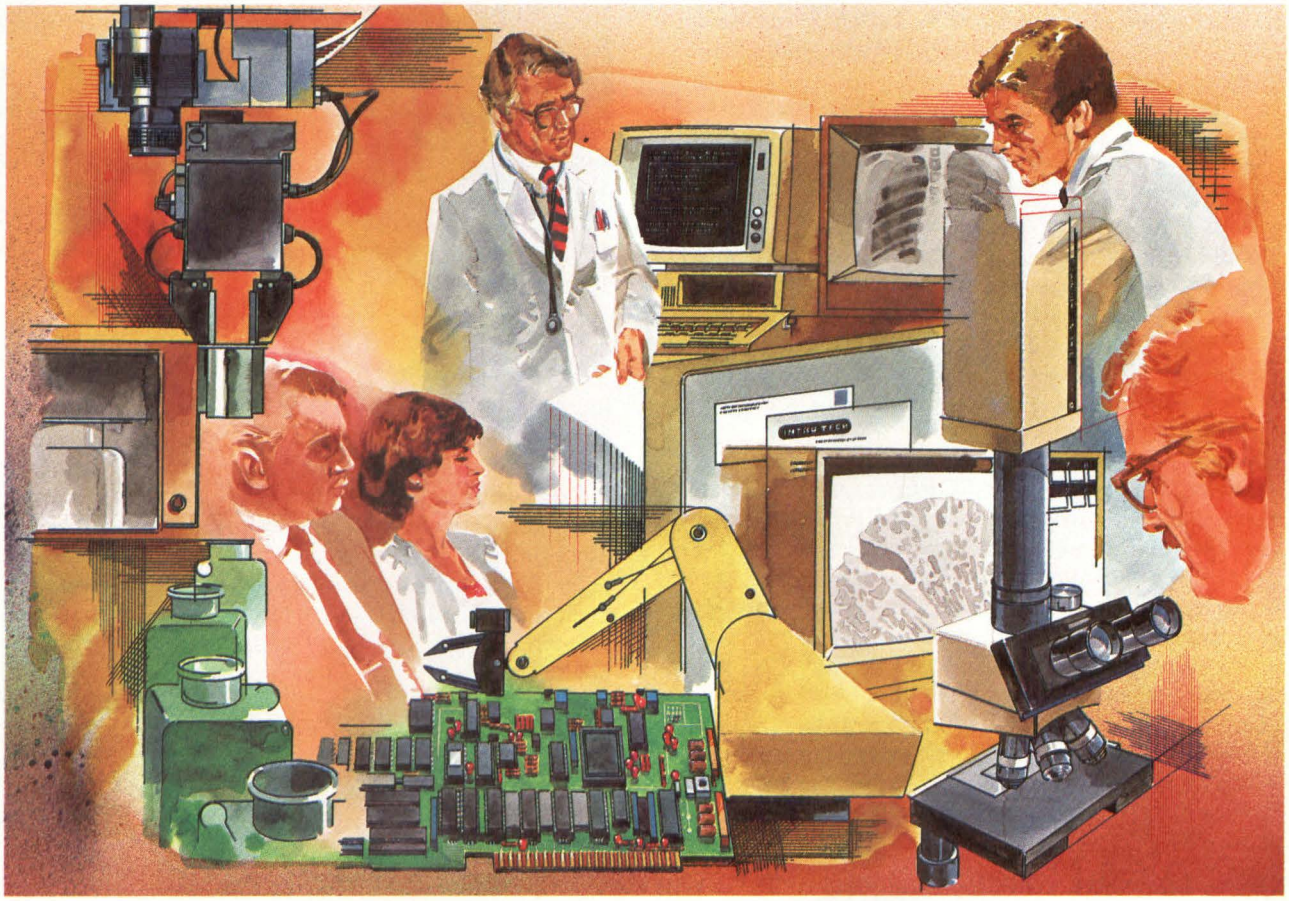

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grabber (the DT2851) and an arithmetic coprocessor (the DT2858). Designed by John Fierke of Data Translation, the frame grabbers feature 512 × 512 frame buffers, except for the DT2603, a lower cost version for the Q-bus which has a 256 × 256 buffer.

Frame stores will also be a feature at the Toko America (Mt. Prospect, IL) booth where the company will show the DR72 Microfreezer, a video memory system for recording and playing back monochrome video images. Two versions of the unit are currently available: the DR72-1, a single frame store, and the DR72-2, a dual frame store with dual video outputs. Specifications of the Microfreezer include 512 pixel/line resolution, 7-bits per pixel and a 10 MHz sampling rate. The company will also show a high-speed stroboscopic video inspection system called the SK1600X Flascope. Using a 2 μsec stroboscopic flash, images are captured by a monochrome CCD camera and sent to a video frame store.

PC-image processing will be the highlight of many of the booths at the show, with over half a dozen exhibitors of frame grabbers, frame stores and coprocessing products. Among these will be New Media Graphics (Burlington, MA) with the GraphOver, a two board set for the PC, XT and AT. The systems allow users to produce an interactive video system controlling video disk playback and superimposing 640 × 400 graphics on video backgrounds. Chorus Data Systems (Hollis, NH) will demonstrate a frame grabber, the PC-Eye, working in conjunction with the Revolution graphics boards from Number Nine Computer (Cambridge, MA). Other personal computer-based vision boards will be the IVG128 frame grabber from Datacube and the PCVision System from Imaging Technology (Woburn, MA).

Figure 3: The GraphOver two-board set for the IBM PC from New Media Graphics allows 640 × 400 graphics to be combined on a video background.

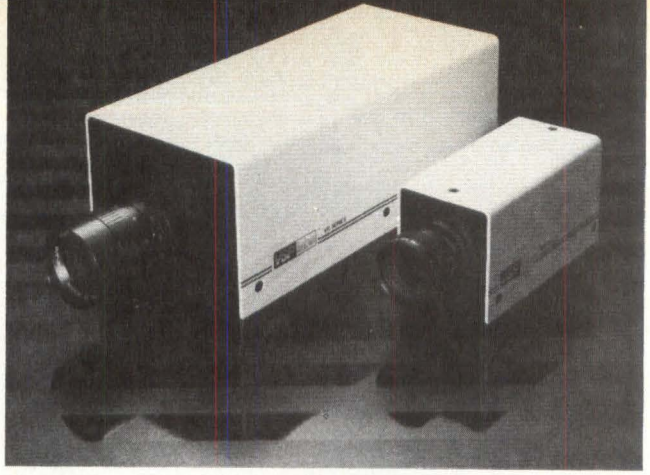

Figure 4: The SC500 CCD-based camera from VSP Labs is capable of digitizing images up to 512 × 512.

Image Display

Image display is, perhaps, the most overlooked group of technologies in the electronic imaging process. Covering both hardcopy and non-hardcopy devices, many different technologies exist to produce images for display. Of these, the most popular are monitors capable of producing high-resolution images. In hardcopy systems, processes range from plotter systems, laser-based printers, thermal transfer devices to electrostatic printers. Each technology has found a specific market depending on the application to which the output device is put. At the Electronic Imaging show, two technical sessions will be devoted to hardcopy technologies, with a third examining the latest developments in display technology.

In the first of these sessions, Shinichi Itoh of Oki Electric will describe a color image printer designed to reproduce TV pictures in under one minute. The printer uses a thermal melting transfer technology which uses a thermal line head of 1024 dots/line with a 400 line/in resolution. Itoh will also discuss several techniques to obtain high-quality images for television-type images. In the same session, Peter Crean of Xerox (Webster, NY) will describe a color page printer using ink-jet technology. Using Rayleigh-stimulated deflected ink-jets, the system uses four jets combined into a monolithic printhead. Crean will examine print quality, color gamut, resolution and printing rate using this technology.

Koichi Takiguchi of Fuji Xerox (Kanagawa, Japan) will present a third variation of hardcopy technology—the laser printer. In his paper, Takiguchi will discuss the optimization procedure of beam diameter and laser power for high-resolution laser printing using the conventional Xerox process.

Wrapping up the first hardcopy session will be a new development from the Tappan Printing Company in Tokyo, Japan. Niro Watanabe of Tappan will discuss the development of a new recording medium that forms a permanent image by means of thermal development and fixing in UV light.

Further details on this year's Electronic Imaging show and convention can be obtained from Ed Martin at (800) 223-7126.

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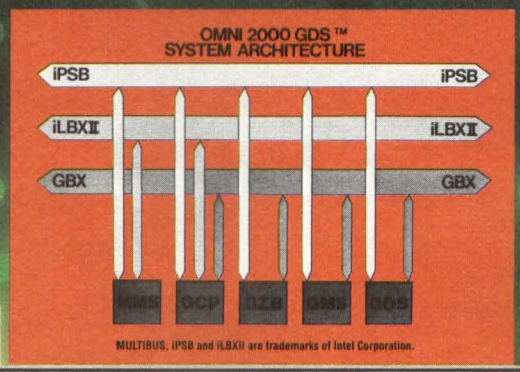

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Preprogrammed Algorithms Ease Development Of Imaging Software

by William Smith, Quantitative Technology Corp., Beaverton, OR

Image processing applications development typically requires a series of numerically intensive vector operations. These operations include vector ratio, vector addition and subtraction and more complex two-dimensional operations such as convolutions, Fourier transforms, and gradient filtering. For most applications programmers, writing code for these algorithms is time-consuming as well as difficult. The routines are also hard to test and debug.

To reduce this coding requirement, Quantitative Technology Corp. (QTC) (Beaverton, OR) has introduced the Math Advantage, a library of preprogrammed core algorithms in both Fortran and C. These routines are specifically designed to assist software engineers developing image processing systems and other numerically intensive applications. By using preprogrammed algorithms instead of writing original code for these complex mathematical functions, engineers working in an applications development environment can concentrate on problem solving and be more productive.

IMPROG, a Fortran program, is a very simple example of how Math Advantage routines can be incorporated to perform image enhancement. The purpose of the program is to enhance the edges of objects within a two-dimensional image, as might be obtained from a satellite imaging system. Edge enhancement is required to make objects within the images appear sharper for easier identification. IMPROG separates the image data into high-frequency and low-frequency components so that the high-frequency data can be filtered to improve the signal-to-noise ratio. The edge-enhanced high-frequency data is then recombined with the low-frequency data to provide a complete image with good resolution. **Figure 1** is a simplified flow diagram of the process, and **Figure 2** is a condensed version of the FORTRAN program.

Initially, the program defines space for the image arrays and the convolution operator. In this example, the arrays are square, but the Math Advantage handles rectangular arrays as well. The typical array size for image processing applications is 512 × 512 pixels; the convolution operator is typically 5 × 5 or 7 × 7. With the Math Advantage, both parameters are variable under user control; however, the better filtering capability of a larger operator must be balanced against the processing speed requirements for the specific application.

CALL VFLOAT (INSIG, 1, SIGNAL, 1, NSIG*NSIG)

Once the inputs are defined, the VFLOAT, a Math Advantage routine, is called to float the integers from the input matrix. This step is required because Math Advantage routines are designed to operate on real (floating point) numbers. INSIG represents the integer input array, while SIGNAL is the floating point output array. The term NSIG*NSIG defines the number of pixels in those arrays.

CALL VCLR (LOFREQ, 1, NSIG*NSIG)

After floating the input matrix, the program calls another library routine, VCLR, a vector clear algorithm to clear the low-frequency array (LOFREQ) since the outermost rows and columns of the input matrix will be left unchanged during the subsequent 2D convolution.

CALL CONV2D (SIGNAL, NSIG, IRB, IRB, NCONV,
NCONV, CONVOP, OPSIZ, *OPSIZ, IIB,
LOFREQ, NSIG, IRB, IRB, O)

The next operation is a 2D convolution to separate the high- and

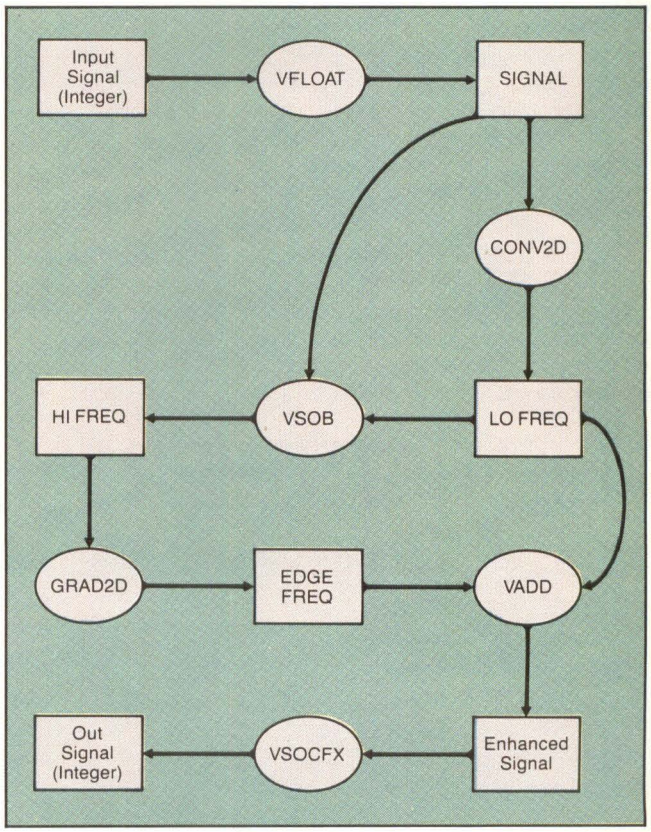

Figure 1: This is a flowchart of IMPROG, a program designed for image enhancement. The squares represent arrays of data. The circles represent operations performed on the image data.

```
      PROGRAM IMPROG
      INTEGER NSIG, OPSIZ
      PARAMETER (NSIG=512, OPSIZ=7)
      REAL SIGNAL (NSIG, NSIG), LOFREQ (NSIG, NSIG), HIFREQ (NSIG, NSIG),
     &             EDGFRQ (NSIG, NSIG),CONVOP (OPSIZ, OPSIZ)
      INTEGER INSIG (NSIG, NSIG), OUTSIG (NSIG, NSIG)
      CALL VFLOAT (INSIG, 1, SIGNAL, 1, NSIG*NSIG)
      CALL VCLR (LOFREQ, 1, NSIG*NSIG)
      CALL CONV2D (SIGNAL, NSIG, IRB, IRB, NCONV, NCONV,
     &             CONVOP, OPSIZ, OPSIZ, IIB, LOFREQ, NSIG,
     &             IRB, IRB, 0)
      CALL VSUB (SIGNAL, 1, LOFREQ, 1, HIFREQ, 1, NSIG*NSIG)
      CALL VCLR (EDGFRQ, 1, NSIG*NSIG)
      CALL GRAD2D (HIFREQ, NSIG, 2, 2, EDGFRQ, NSIG, 2, 2,
     &             NSIG-2, NSIG-2)
      CALL VADD (EDGFRQ, 1, LOFREQ, 1, SIGNAL, 1, NSIG*NSIG)
      CALL VSOCFX (SIGNAL, 1, SCALE, OFFSET, LOLIM, UPLIM,
     &             OUTSIG, 1, OUTSIG, 1 ,NSIG*NSIG, 0)

      END
```

Figure 2: In this simplified Fortran program of IMPROG, arrays and dimensions have been given arbitrary names to reflect their purpose in the program.

low-frequency data. The 2D convolution is typically used to attenuate unwanted signals; in this instance, it is used to improve the signal-to-noise ratio. The input data is convolved with the convolution operator, which acts as a filter, leaving only the low frequencies (LOFREQ) in. The 2D convolution is a multiply and sum operation where one output value is produced for each position of the operator. All the elements in the operator matrix CONVOP are multiplied by the corresponding values of the signal matrix. The products are summed and the result stored in the result matrix, LOFREQ. **Figure 3** shows a comparison between one-dimension and two-dimension convolutions. The large number of arguments in the CONV2D call allows flexibility to handle positioning within the matrices and nonsquare matrices. The argument SIGNAL refers to the input array of floating point data. CONVOP is the convolution filter array; LOFREQ is the output of the low-frequency array. The other arguments represent array dimensions and positions.

CALL VSUB (SIGNAL, 1, LOFREQ, 1, HIFREQ, 1, NSIG*NSIG)

After convolving, the VSUB (vector subtract) routine is called to subtract the low frequencies from the input signal to get the high-frequency data (HIFREQ).

CALL VCLR (EDFRQ, 1, NSIG*NSIG)
CALL GRAD2D (HIFREQ, NSIG, 2, 2, EDGFRQ, NSIG, 2, 2, NSIG-2 NSIG-2)

To enhance the edges, a gradient operation is then performed on the high-frequency data. First, the edge-enhanced array (EDFRQ) must be cleared since the outermost rows and columns will be left unchanged by the gradient operation. VCLR is again called, followed by GRAD2D, which applies the maximum gradient filter to the high-frequency data.

The trouble with most image processing systems is the time it takes to get them up and running.

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CALL VADD (EDFRQ, 1, LOFREQ, 1, SIGNAL, 1, NSIG*NSIG)

After the gradient filtering, the edge-enhanced high frequency (EDGFRQ) is recombined with the low-frequency (LOFREQ) data using the vector add (VADD) routine from the library.

CALL VSOCFX (SIGNAL, 1, SCALE, OFFSET, LOLIM, UPLIM, OUTSIG, 1, OUTSIG, 1, NSIG*NSIG, 0)

To display the image, the data is scaled, an offset is added and the data is matched to a legal range. The output is also converted to integer form. To accomplish these operations, the vector offset, clip and fix (VSOCFX) routine is called from the library.

Using the Math Advantage library routines, instead of writing code for the algorithms in this example, saves the user time and effort. To duplicate the code presented by the algorithms called, the average software engineer or programmer would have to write 150-200 lines of FORTRAN. In addition to the large amount of time required to reproduce the code, the user would have to perform extensive testing on the original code to ensure correct results. The complexity of these particular algorithms makes such testing and debugging difficult. In contrast, the Math Advantage routines have been tested for accuracy and were designed to optimize the performance of most high-speed architectures. The subroutines can also be hardware optimized by QTC to accelerate run time. DD

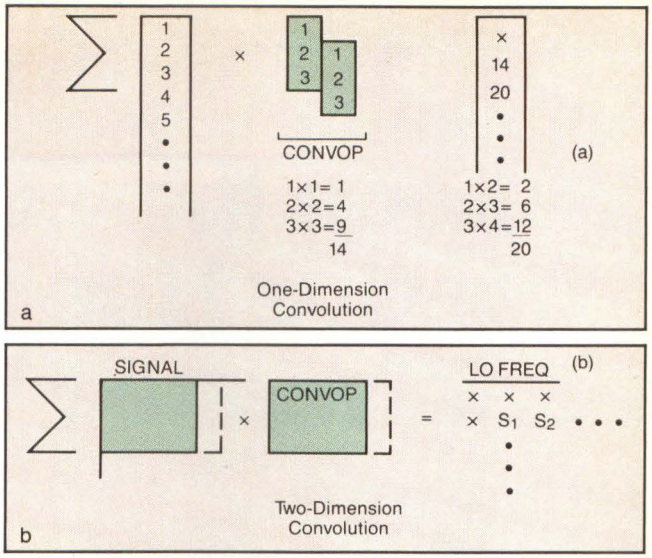

Figure 3: This diagram shows the movement of the filter kernel (CONVOP) across the data in (a) one-dimensional convolution and (b) two-dimensional convolution.

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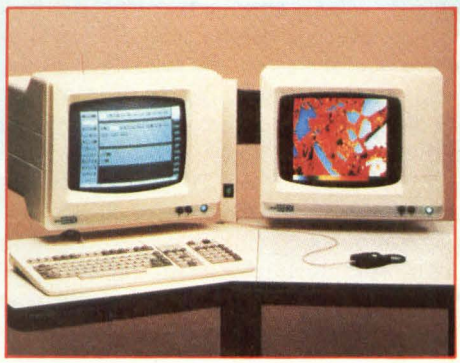
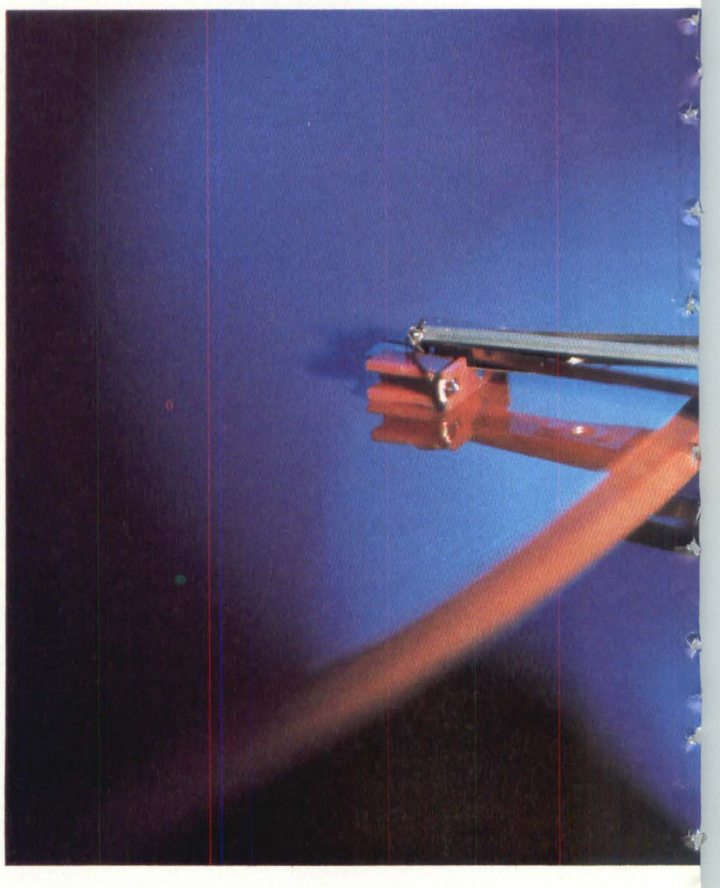


THE SHORTER YOU HAVE TO GO.

Circle 20

Options Increase For Effective Use Of High-Performance Winchesters

by Julie Pingry, Senior Editor



Despite advances in small format Winchesters, high-performance computers continue to use 8″ and larger disk drives with very high capacities and fast access times. But the specifications of these large format disk drives alone do not assure optimal performance for system disk operations. The choice of interface and controller as well as the development of file and driver software can make the performance of the same drive very different in various systems.

Traditionally bound to the SMD interface, 8″, 10½″ and 14″ Winchesters' performance have challenged standard 10 MHz SMD controllers. To keep disk rotation speed constant with increased bit densities, the data transfer rate to and from the disk must increase. Faster versions of SMD, called HSMD, ESMD or SMD-E, have sped up the same basic interface to 15-24 MHz, or up to 3 Mbit/sec transfer off the disk. Although these rates are adequate for most current drives, two new parallel Intelligent Peripheral Interfaces, IPI-2 and IPI-3, are well on the way to standardization and acceptance by the industry. With a parallel interface, more speed will be possible without stretching the specification or using expensive components.

Even with a well thought-out drive interface and a fast-access disk, systems can find disk I/O a major bottleneck. The proper controller for the system must be chosen; one with fewer frills may require more effort in system software development, but can provide greater raw speed and less bus overhead. Various system applications require different schemes for seeking, caching and disk utilization. A primary requirement is a good operating system interface to the disk. Writing drivers for a particular combination of controller and disks may not be an easy task, but it can make the difference between medium- and high-performance from an otherwise well-designed system.

System Integration Keys

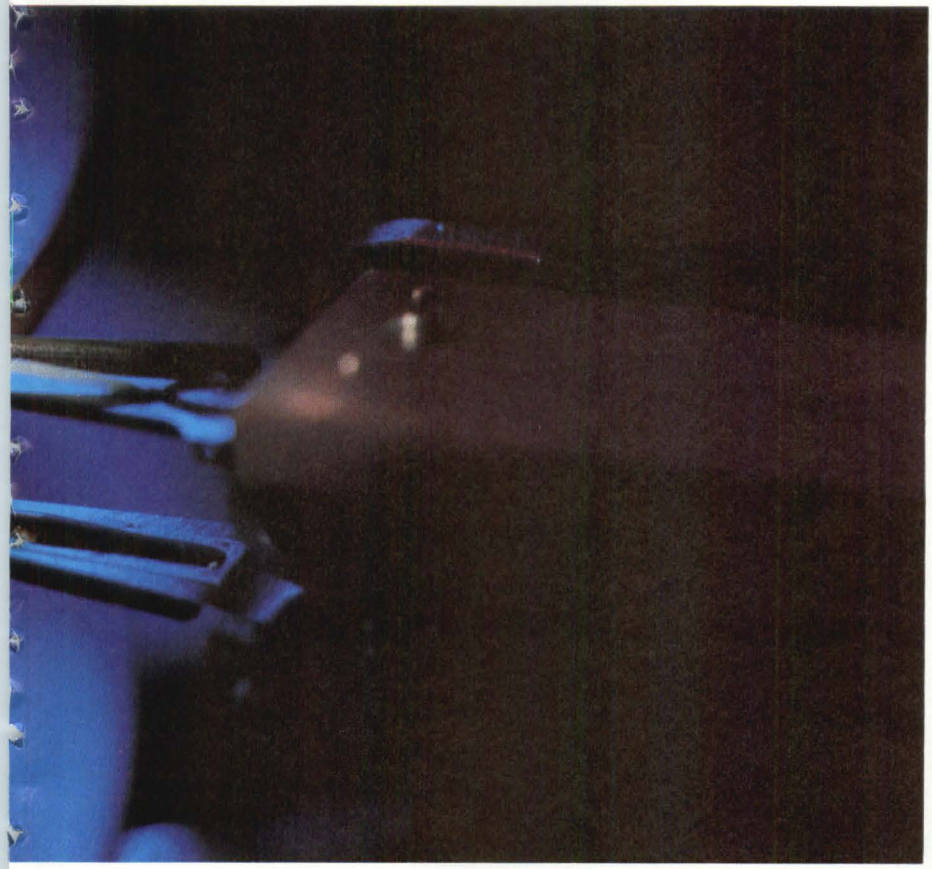
For disk operations to match demands from high-end systems with internal buses and open system buses dedicated to I/O, data must be efficiently transferred from disk to I/O bus. Multitasking operating systems, multiuser and multiprocessor systems change the type of disk access that is most efficient.

Simple look-ahead caches are useful for single task, single user systems; but the disk segmentation under UNIX, for example, dramatically reduces the cache hit rate. Likewise, interleaving of data on the disk is useful for many systems, but in high performance multitasking configurations, disk access speed may be slowed considerably if the disk and controller cannot perform noninterleaved seeks.

When testing controller/disk combinations, consider the application to which the system will be put. Although this seems obvious, it may not be standard practice. Generic testers, like data sheet specifications, focus only on raw speed. In systems with extensive disk interaction, buffering, caching and seek optimization have a large impact on performance. These features are not nearly as important as pure data transfer speed for systems making less frequent large block requests, single application processors or accelerators.

Another area to consider is whether there may be more than one disk drive attached to the system and controller. If so, overlapped seeks can enhance speed. Command chaining and ordering of seeks further aid multiple drive systems. With current drives at several hundred Mbytes to one Gbyte, multiple data channels could aid access to that quantity of information as well. Both SMD and IPI have dual-port capability built into the specification; although primarily used for fault tolerance, with the appropriate software and architecture, this can also be used for dynamic pathing in very high performance systems.

Writing software drivers is also critical. Controller houses should provide some driver support; customers should devote time and resources to developing appropriate I/O drivers. Despite the time needed to write a good driver, better I/O could affect a system's competitive position once on the market. Testing, controller choice and appropriate software drivers are critical. No matter how good the system's architecture is, slow access to disk data can hide or destroy performance. One choice that must be made early is that of drive and host interface.



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Combined with IPI-2, IPI-3 or enhanced SMD interfaces, sophisticated disk technology may now be put to full use; but testing, design for the application, controller choices and software drivers are still key.

Stretching SMD

Storage Module Drive (SMD) is the traditional device interface choice for high-performance systems. Since its introduction as an interface for Control Data Corp. (Minneapolis, MN) removable disk drives, the specification has been improved to keep pace with available disk drives. In addition to the original 1.2 Mbyte/sec data rate off the disk, a 1.8 Mbyte/sec or 15 MHz version has been available for several years. This change required no modifications in controllers or the specification. Fujitsu (San Jose, CA) has increased speed to 20 MHz or 2.4 Mbytes/sec in its HSMD drive interface. Even at that speed, compatibility was ensured by working with controller houses.

Drives using IBM 3380 technology record 12 million bits/sq. in., so data comes off the disk extremely fast. Control Data has increased the speed for its SMD-E (extended) interface to as much as 3 Mbytes/sec or 24 MHz to accommodate these drives. ECL drivers and receivers are needed for the servo, read and write clock and read and write data signals to operate at this speed. **Figure 1** shows the minimum (passive) TTL to ECL translation circuitry required for existing SMD products to be used at 24 MHz speeds.

SMD was the first standard adopted by the ANSI X3T9.3 group. The interface is so established that the federal government has adopted it as a FIPS standard. ANSI revisions (included in the government standard) covering ESMD, HSMD and SMD-E improve not only speed but also error handling and diagnostic features. Despite the complexity of SMD, the established manufacturing history for drives and controllers may give it a long life.

Most drives and systems will not need more speed than the 20 or 24 MHz of the extended SMD specifications in the next few years. Furthermore, as Dal Allen of ENDL (Saratoga, CA) points out, few controllers or drivers have been developed from scratch recently, since established standard interfaces have served most of the market. This may make ramp-up lengthy on controllers and silicon for implementing interfaces that have not evolved from an older standard, further prolonging the life of SMD implementations.

Parallel Development

The IPI interface, designed specifically for high-performance systems with fast disk access, is the natural next-generation interface for systems that have used SMD. In a twist indicative of today's market emphasis on standards, IPI is being defined by an ANSI committee. Many major disk drive, controller, IC and systems manufacturers have had a hand in developing the

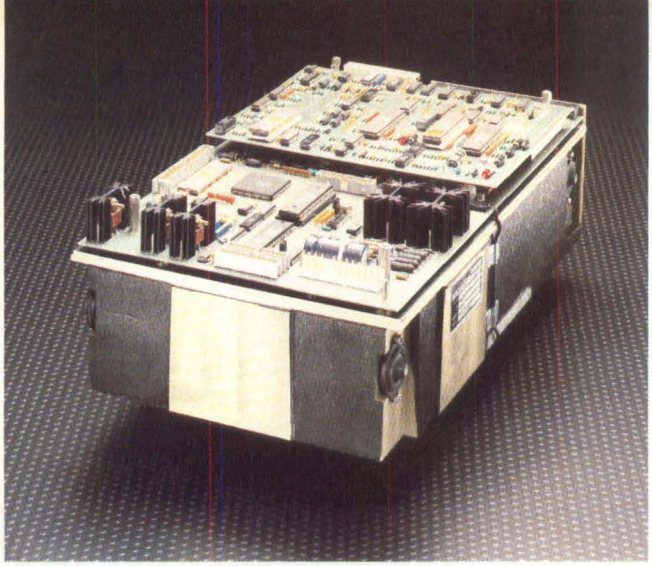
specifications before any implementations have appeared.

IPI's main advantages are that it is not only a standardized interface, but also a parallel interface, and thus more expandable to future system disk access speed requirements. With 16 parallel lines, speeds as high as 80 MHz or 10 Mbytes/sec are currently defined. In contrast, SMD may have reached its practical limits at 24 MHz. High-performance system houses that do not wish to redesign their controller and interface in the next five years should consider the relative lifespans of SMD and IPI-2 when deciding which to use.

Two IPI interfaces are being specified: IPI-2, a drive-level interface, and IPI-3, an intelligent system interface. The two do not depend on each other; the device-level IPI-2 can function with many host interfaces, and IPI-3 can operate with other device interfaces as well.

IPI-2 compares directly to SMD, as a device-specific command set for disk drives. (One for tape drives is also in development.) As shown in **Table 1**, the higher-speed IPI also allows longer, less expensive cabling. The added drive functions are a fallout of the parallel interface, and still require interpretation by the controller. As with SMD, the drive and controller must be tightly coupled.

IPI-2 uses two 8-bit data buses with parity and six interface control signals. Device control is through bus control octets on the data buses, with the A bus serving master (controller) to slave (drive) communication and the B bus for slave to master.



Control Data offers SMD-E at 14.5 MHz or SMD on several new models. The 8" EMD shown has 18 msec seek time to 368 Mbytes of data.

These bus control octets are the first eight bits put out on bus A, not electrical signals as used in SMD for device control. Four types of bus control octets are used: read, write, command (like the Tag Code on SMD) and response (for disk status reports to the controller). Once these are passed, both A and B buses are used in the same direction to transfer information. Disk data is not buffered off the drive, but sent directly to the controller at disk speed.

To enforce true compatibility between disk drives meeting the

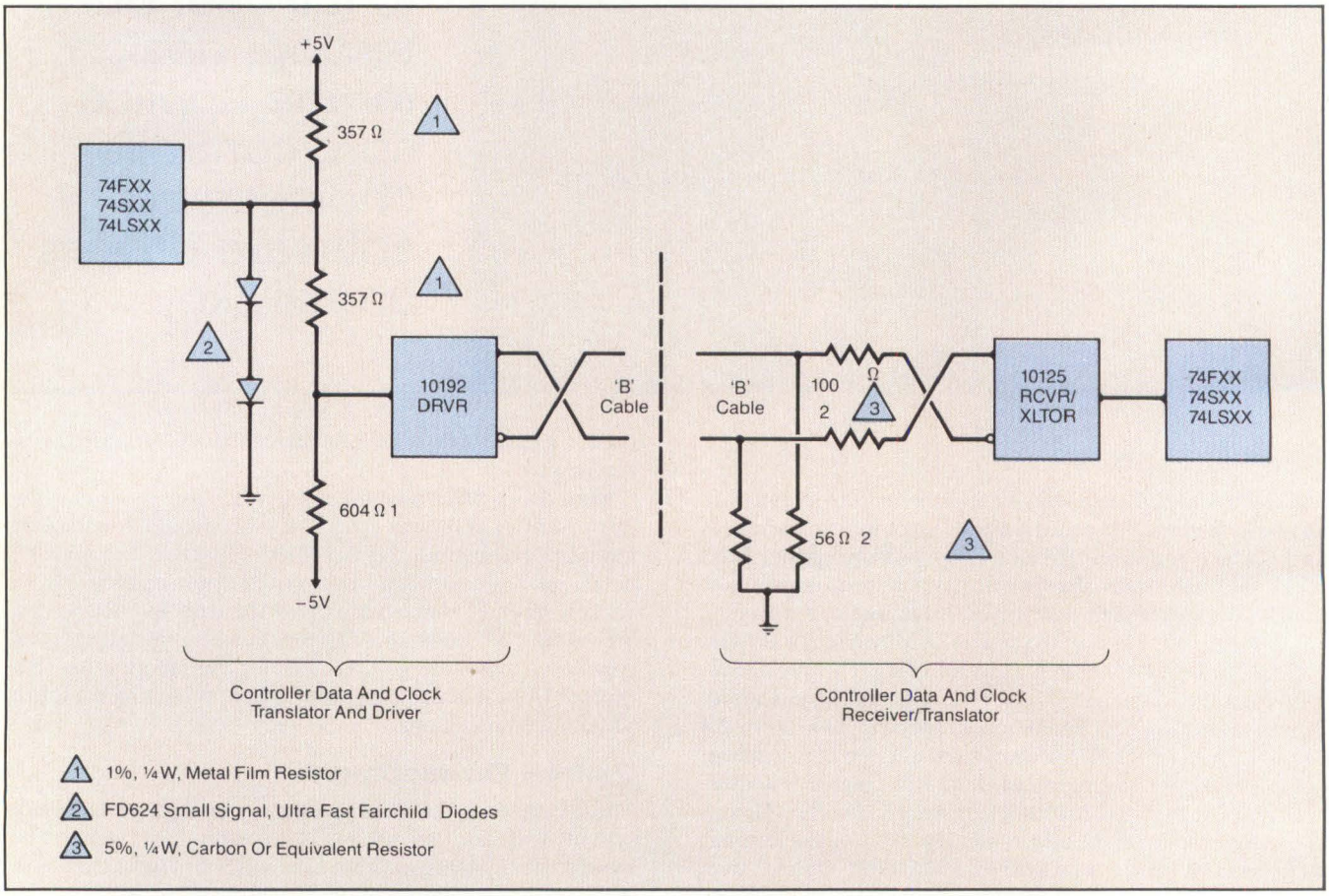


Figure 1: To achieve 24 MHz data transfer rates, SMD disk drives need to use ECL drivers and receivers. As published in the CDC SMD-E specification, this is the minimum (preferred passive) translator circuitry needed for all signals on current TTL SMD systems to reach that speed.

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Circle 51

IPI-2 standard, a two-chip set is being developed by Simulex (Tustin, CA). Eight drive manufacturers have submitted purchase orders for Simulex's chip designs: Control Data/MPI, Fujitsu, Priam (San Jose, CA), Century Data Systems (Anaheim, CA), Ampex (Cupertino, CA), NEC (Boxborough, MA), Pertec (Chatsworth, CA) and STC (Louisville, CO). Others can place orders, with the understanding that their shipments may be later. The purchase includes chip emulator boards and an SMD adapter board as well as prototypes, software for use with the 8051 microcontroller and rights to the design and database. The emulator boards for each chip and the SMD adapter are to be delivered to the original eight buyers in October; the rest are scheduled for shipment in 1986.

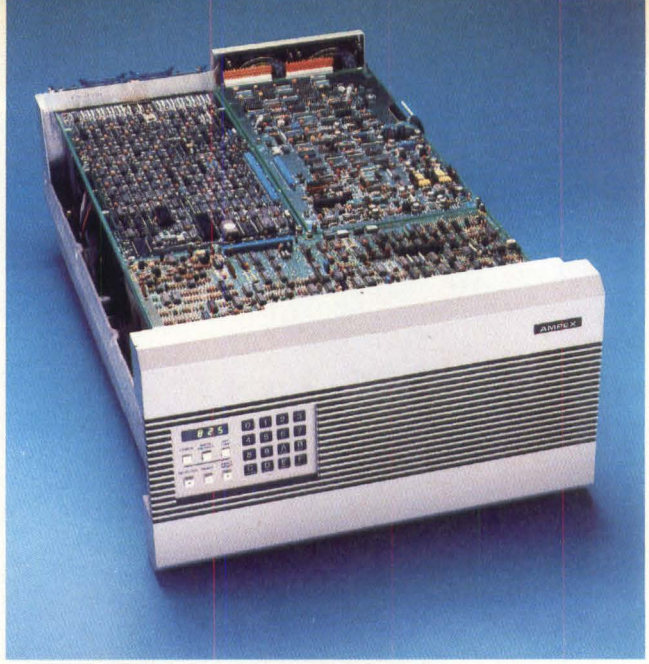
The two chips are the SX1601 Interface Protocol Circuit (IPC) and the SX1602 Serdes (serializer-deserializer) Formatter Circuit (SFC) (**Figure 2**); both are CMOS gate arrays. The IPC interprets bus states, sending Command or Response bus controls to the drive microcontroller and Read or Write controls to the SFC for execution. The interface to the microcontroller on either IC is directly timing compatible with the 8051, MC6801 or Z8 and adaptable for other 8-bit processors. **Figure 2** shows a switched dual-port IPI-2 drive configuration; systems with the speed and performance that have driven development of IPI-2 often demand the reliability of two ports. Only one IPC is needed for single-port drives.

Functions to record, recover and format data on a disk, as well as serializing and deserializing off the interface, are provided by the SFC. It acts as a slave to the microcontroller. Having the Serdes and microcontroller on the disk drive opens up new possibilities for the partitioning of functions. In **Table 1**, functions such as locating the beginning of field and stripping off sync bytes are performed by the drive, easing demands on the controller and on the timing coordination between drive and controller. The significant task of recording and reading out the drive defect map can also be eased with IPI-2. The drive's native chip set and microprocessor can be used for media verification at manufacture, and once in the system, the controller can command the drive to read out its defect map.

Comparison Between IPI-2 And SMD

	IPI-2	SMD
Maximum Data Transfer Rate	80 MHz 10 Mbytes/sec	24 MHz 3 Mbytes/sec
Line Signal Toggle Rate	5 MHz	24 MHz
Maximum Cable Length	50 meters typ. 125 meters max.	15 meters B cable 30 meters A cable
Cable Scheme	1 ea. 50 conductor round shielded daisy chained cable	1 ea. 60 conductor round shielded daisy chained cable 1 ea. 26 conductor round shielded star connected cable per drive
Data Transfer Method	16-bit word serial	bit serial
Features	drive performs PLO synchronization, bit sync, byte sync, strips sync fields and gaps, defines a standard defect map, provides for drive managed ECC, allows for drive defect management (skip or swallow)	drive performs PLO synchronization, bit sync

Table 1: This is how Simulex compares IPI-2 with SMD. IPI-2 is faster and permits less expensive, longer cabling to be used. Both are device-level interfaces, but because IPI-2 is parallel and the drive requires a serializer/deserializer (Serdes), more functions can be performed by the drive.

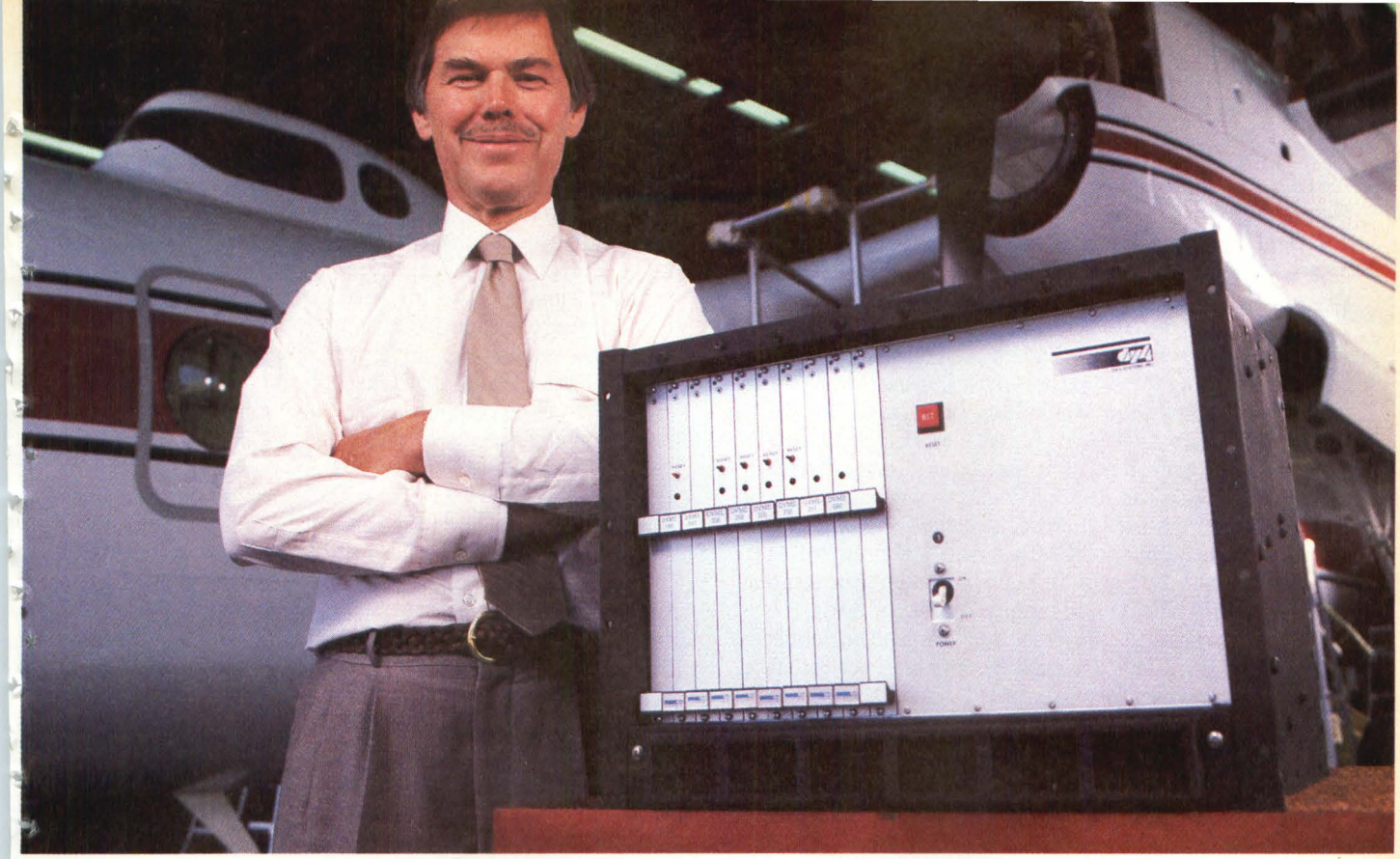


Ampex's 825 14" disk drive uses SMD at 1.859 Mbytes/sec. Models with 330 or 660 Mbytes capacity can be upgraded to 825 Mbytes.

The two-chip IPI-2 interface assures standardization of a subset of IPI-2 functions in eight major manufacturers' drives. Once these drives are out, controllers will likely follow. Bob Morris, manager of development engineering at Simulex, predicts that even though no similar chip set is under development for the controller side, mainframe system houses that want to accommodate 24 MHz drives may produce controllers next year. Control Data has used gate arrays to implement an IPI-2 controller and indicated a willingness to license those. Siemens (Munich, West Germany) is also working on an IPI-2 controller that it may make available on an OEM basis. IPI-2 may be implemented sooner than other new interfaces because it is a drive level interface, not an intelligent interface; this should make writing software drivers easier than for intelligent interfaces like SCSI and IPI-3.

Using Interface Intelligence

Although they are more difficult to design, debug and write software for, intelligent disk drive interfaces are becoming popular. Since the system only addresses the device logically, with no need to know the mechanics of the device being used, intelligent interfaces provide device-independence. This translates into a single system interface for many peripherals, as well as easy integration and upgrade. They also offer low cost for single-drive systems by incorporating many functions into the drive and good performance for multiple drive systems by a large repertoire of functions. Like IPI-3, SCSI is an intelligent interface; it is now offered on some high-performance drives.



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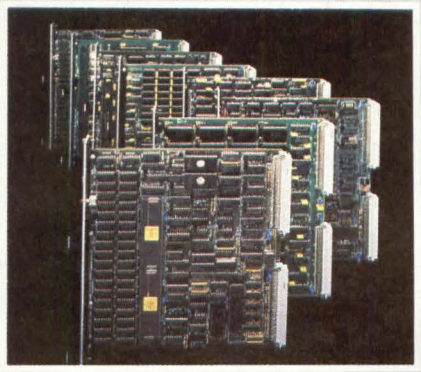

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Circle 27

SCSI is an 8-bit parallel bus that can interface between as many as eight host or slave devices. Several 8" Winchesters are now available with an embedded SCSI interface. Priam's 227 Mbyte 806 and 344 Mbyte 807 models with SCSI are being shipped mainly to CAD, graphics and European system manufacturers. Another example is Amcodyne's (Longmont, CO) fixed/removable Winchesters with SCSI. Fujitsu has developed an SCSI controller for its line of 8" drives; using the 337 Mbyte model, 1.38 Gbytes are available to one controller. NCR's (Colorado Springs, CO) SCSI chip (*Digital Design*, December 1984, p.80) has made it possible for a large number of firms to offer SCSI products early. Still, SCSI is primarily aimed at cost-conscious, not high-performance, applications. The SCSI bus operates at a maximum of 4 Mbytes/sec, and with SMD at 3 Mbytes/sec, the advantages for high-end systems are less than for applications where SCSI replaces ST506 or SASI.

IPI-3 is a similarly intelligent, device-independent peripheral bus. But like IPI-2, it is designed for very high performance. Underlying layers are identical for IPI-2 and IPI-3: electrical and mechanical specifications are called IPI-0; IPI-1 is the bus protocol and state machine. With a maximum speed of over 10 Mbytes/sec, IPI-3 can provide the same isolation from changes in specific peripherals as SCSI for much higher performance systems. IPI-3 also has a richer command set than SCSI. Minicomputer or mainframe manufacturers can design an IPI-3 system interface and plug various peripherals into the subsystem as needed without affecting the system software.

At the IPI Forum, conceived by Dal Allen, industry support for IPI was apparent, and product plans were also unveiled. A range of products from controllers to connectors and chips for both IPI-2 and IPI-3 were discussed. Interphase (Dallas, TX) is developing two controllers for IPI-3. Siemens is designing an IPI-3 host bus adapter for its 7.500 computer. Gould AMI (Santa Clara, CA) has developed a chip for IPI-3 controllers, but there was no commitment to outside availability. A connector for IPI systems from AMP (Harrisburg, PA) was revealed. Perkin-Elmer (Tinton Falls, NJ) expressed its desire for IPI-3 to remove device I/O from the operating system and put it into controllers. Even IBM announced that its future OEM storage products would use an IPI interface.

One of the most important announcements was Control Data/Magnetic Peripherals Inc.'s controller for IPI-3 to IPI-2 interfacing called CM3 (**Figure 3**). Planned for release in mid-1986, the CDC/MPI board will create a working subset of IPI-3. Initial users may include Honeywell, Sperry and Control Data. With such a controller, only a host adapter for the specific host system needs to be designed. And even though IPI-2 and IPI-3 do not depend on each other, having the same

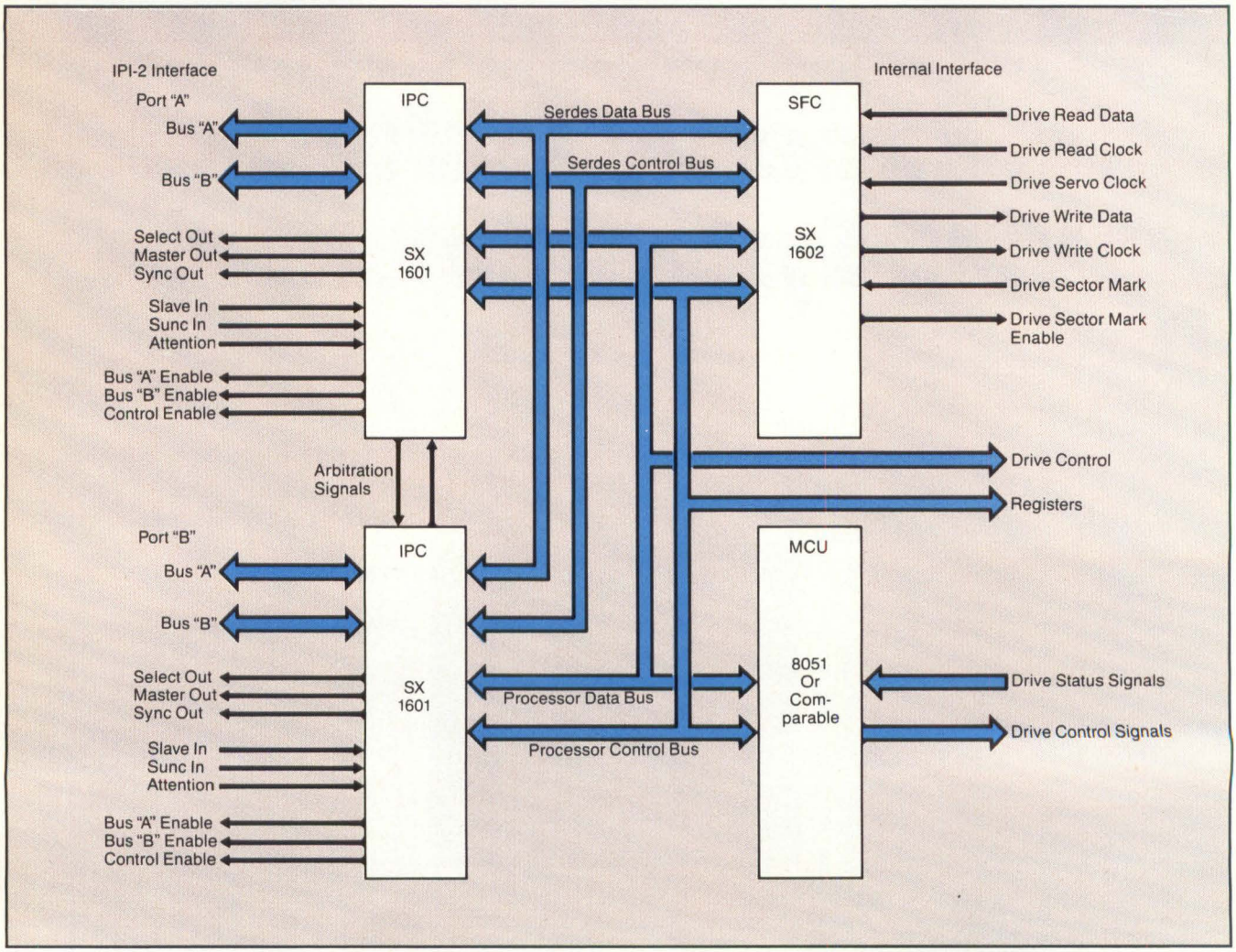

Figure 2: With two Interface Protocol Circuits, a Serdes Formatter Circuit and an 8-bit microcontroller, dual-port IPI-2 can be implemented in disk drives with minimal trouble. The Simulex chip set also ensures a subset of compatibility for all IPI-2 drives that use them.

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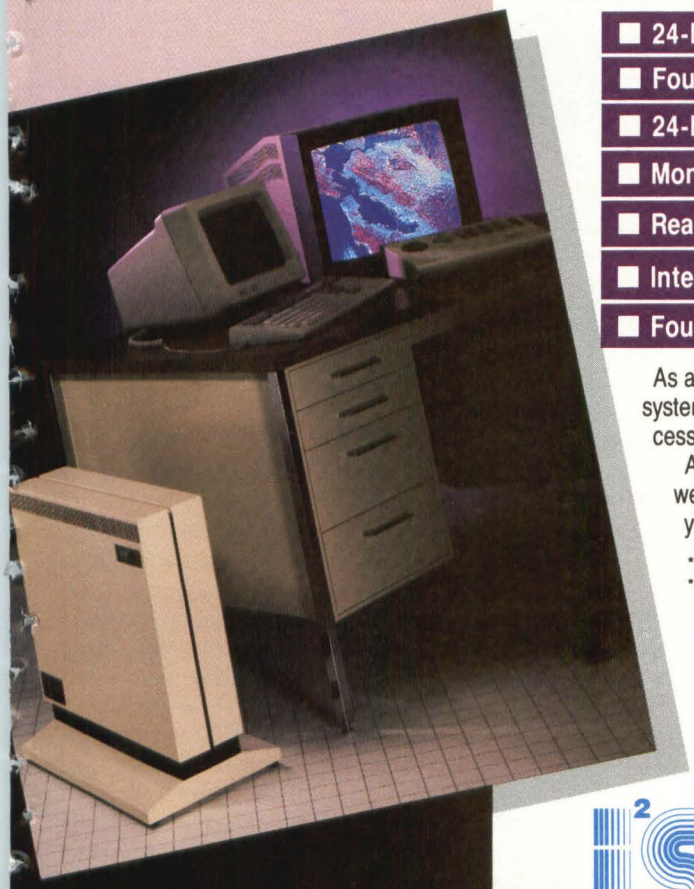

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Circle 52

cabling and bus protocol may streamline I/O subsystems.

At NCC, Hitachi America (San Bruno, CA) demonstrated the SC801 IPI-3 controller. Available in the first half of 1986, the SC801 can handle up to eight Hitachi DK815 8.8" drives. The controller will include multiport capability and may be offered as an OEM product.

The many options available with intelligent interfaces make compatibility across manufacturers virtually unavailable. This is a major drawback for intelligent interfaces. Users of SCSI can attest to the lack of interchangeability. IPI-3 proponents claim that since the interface has not evolved, but has been started from scratch, those problems will not surface. The CDC/MPI Control Module provides the basis for a compatible IPI-3 subset. Dal Allen has also published a document called ENDL-Facto that defines a usable working subset; the document is available for $75 by writing to ENDL, 14426 Black Walnut Court, Saratoga, CA 95070.

New intelligent disk drive interfaces will dictate a different partitioning of functions between the disk drive and the controller. Some flexibility may be taken away from the operating system, with so many of the error management, buffering and seek ordering functions removed to the I/O subsystem. Depending on the system objectives, this removal of functions from the OS may be positive or negative.

Drive Implications

Emerging high-performance interfaces designed for maximum usage of current disk drives will also allow more advanced disk drives and different disk subsystem configurations to penetrate the market. IPI, with the capability to transfer data off disks at up to 80 MHz, can be used with vertically recorded disks. Multiple head disk drives, though a niche market, will also be easier to employ at higher data transfer rates to the system. And with intelligent interfaces, strings of drives can be closely controlled.

Fujitsu's M2350A Parallel Transfer Disk (PTD) is one product that will demand higher data transfer rates. A current subsystem from Storage Concepts (Westminster, CA) uses a proprietary interface to transfer up to 1.86 Mbytes/sec on five channels per M2350A drive, for 9.3 Mbytes/sec total. This speed will be available via IPI as well. The standard allows others to use these PTD drives without designing a proprietary controller and I/O scheme.

Although the technology is not new, vertical recording has not taken hold because controllers and interfaces could not handle data at the speeds they come off these surfaces. Lanx (San Jose, CA) is one of the few companies working with vertical recording that has been able to weather the slim business. Until now, its sales have primarily been standard media, but by next year, IPI drives and controllers that can handle faster data transfer may make vertically recorded media marketable.

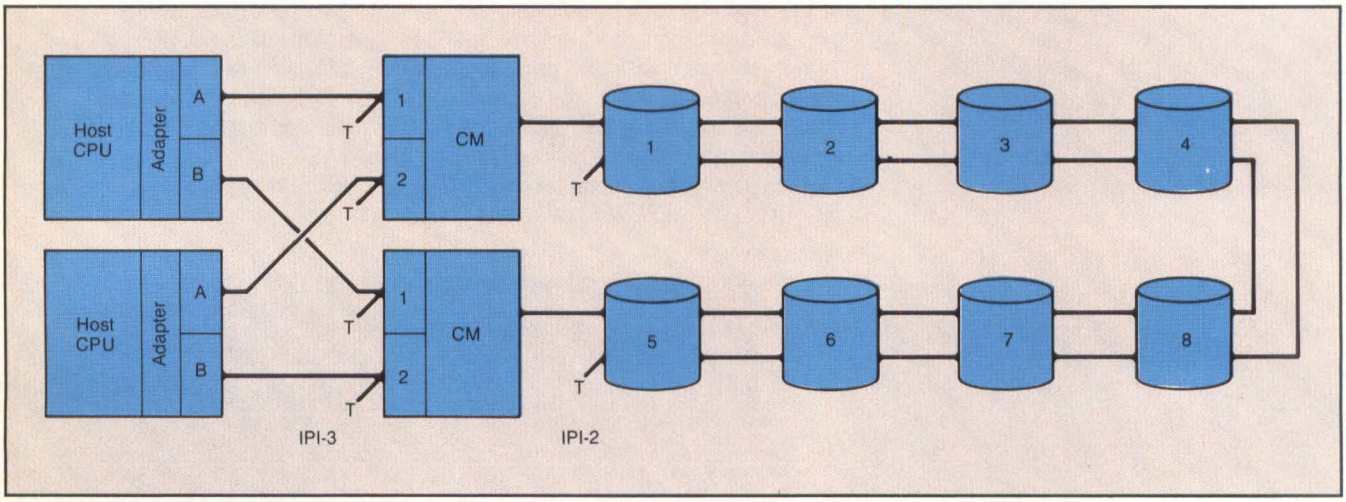

Figure 3: Control Data's CM3 Control Module is an IPI-2 to IPI-3 controller to be available mid-1986. This is a typical system configuration with dual-port drives; 50m cables can be used on the host side and 15m cables on the drive side.

Another type of disk drive that has had a limited market is multiple-head drives. Companies like Alpha Data (Chatsworth, CA) are content with a niche market. But large firms including Fujitsu and CDC also make multiple-head drives. To make use of drives such as Alpha Data's Atlas with 54 moving heads, a faster disk transfer is desirable. For applications that require extensive disk use, more heads assures faster access to data. But only if the interface and controller are properly designed to accept data from heads in rapid succession will the extra performance of this type of disk be seen in system applications.

Multiple heads can also be provided to a controller by using more drives in a string. Again, the speed of an IPI interface may be the factor that allows this configuration to be effective in a system. Systems not designed to accept data from more than one head cannot necessarily optimize the capabilities of multiple head configurations, whether on one disk or many.

For the first time in the past few years, choices are opening up for high-end disk I/O systems. The risk of using a new interface may extend the life of current designs by several years. But extended SMD and IPI interfaces are well documented and will accommodate the disk technology already developed. So interface changes are not an isolated issue in system configuration, but also affect the range of drives that can be used to their maximum. DD

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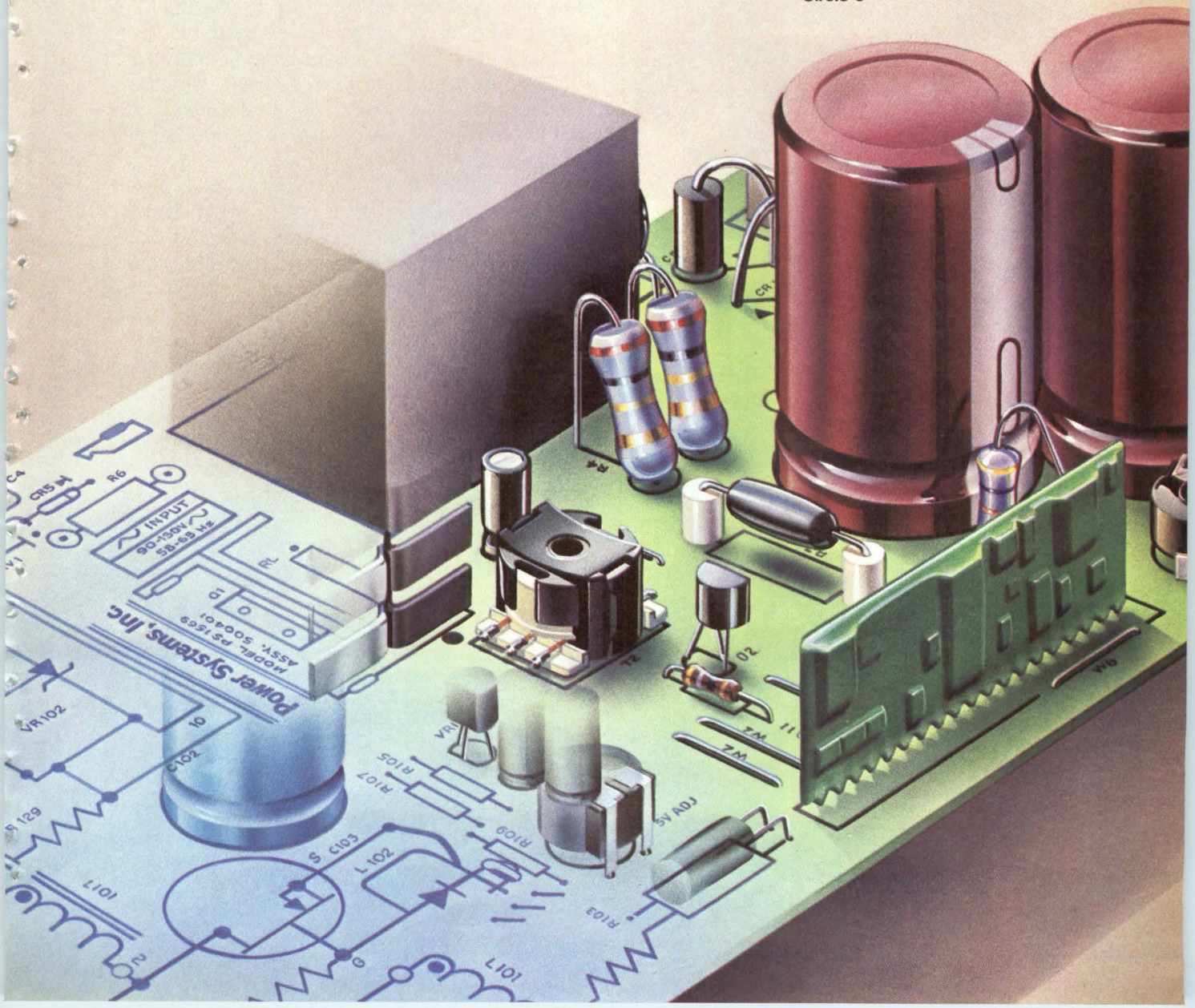

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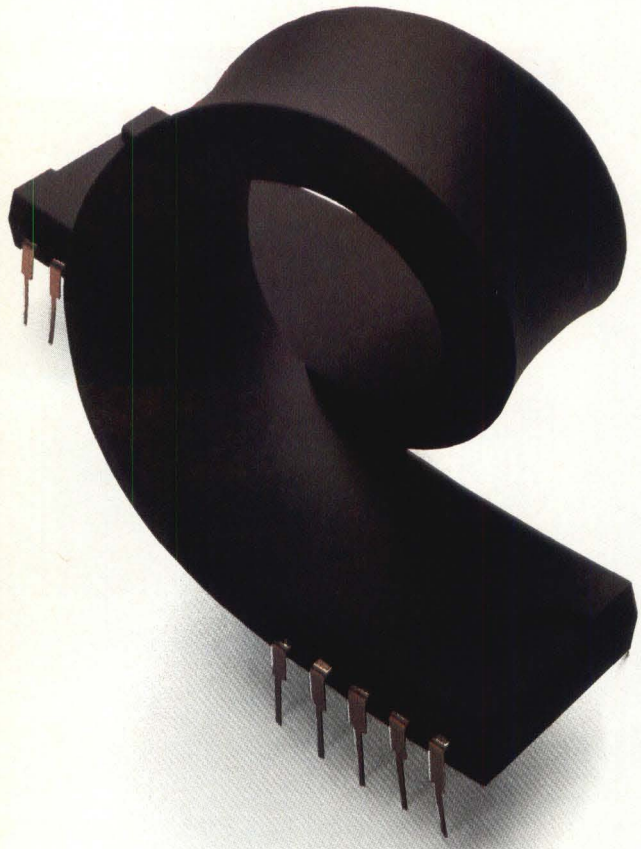

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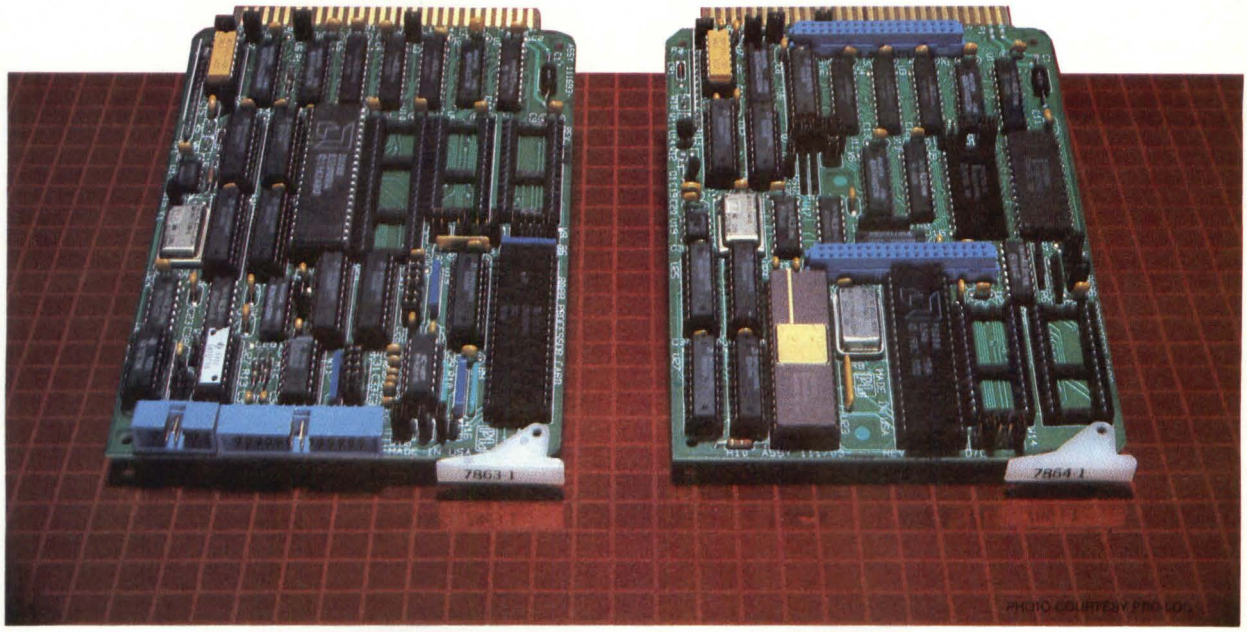
16-Bit Multiprocessing STD Bus Challenges High-End Solutions



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by Dave Wilson, Executive Editor

Developed by Pro-Log (Monterey, CA), and introduced jointly to the marketplace by Pro-Log and Mostek (Carrollton, TX) in 1978, the STD originally was an 8-bit industrial microcomputer bus. Today, a great number of 8-bit processors are available on the STD, including the Z80, the 8085 and the 6800. STD cards that use peripheral chips usually depend on specific timing signals from the processor, and this dependency prevents peripheral cards from being used interchangeably with cards from other families. Therefore, the STD manufacturers designated compatibility by labeling the cards that are processor-timing dependent, with reference to the CPU device, for example, STD-Z80, CMOS Z80 and STD-6800.

According to Philip Hayes, president of Alpha Omega Computer Systems (Corvallis, OR), the Z80 version of the bus represents at least 75% of the market, and although other versions have proliferated, the Z80 has become the de facto standard because of its large market. This has not prevented other manufacturers from putting higher performance processors onto the bus. According to Ziatech (San Luis Opisbo, CA), there are many control applications whose requirements exceed 8-bit processor's memory and execution speed limits. Ziatech and the STD Bus Manufacturers Group introduced an implementation specification for Intel's 8088 and 80188 processors on the STD bus which was adopted in 1983. The reasons given by Ziatech include the fact that the 8088 and 80188 were chosen because of their suitability for control applications and the overwhelming success of the 8088 in the IBM PC and compatible computers.

Although the IBM PC is a well-defined environment, with 8088, RAM, disks and DOS, a dedicated STD system is totally different. It may have an 8088 but is not likely to have large RAM, disks or DOS. According to Ken Finster, president of Micro/Sys (Glendale, CA), these differences are why problems arise when the PC is used as a development station for STD bus systems. A key problem is that the assemblers and compilers for the IBM PC assume the code generated will be running on the PC. Therefore, the structure of the code makes it difficult to get into EPROM. For example, it is assumed that an assembled or compiled program will be loaded from disk at run-time, relocated to available, dynamically allocated RAM, run out of RAM and make DOS calls as required.

Another issue is the linkers on the IBM PC. They gather both

data and code segments into a single contiguous module for loading into RAM. The fact that both data and code are loaded as one module makes it difficult to PROM the code. In addition to the linker problem, high-level languages run-time modules also rely on DOS calls. These problems can be solved, however. By observing a set of rules during software development, it is possible that code modules can be manipulated into the desired ROM/RAM memory map of the STD bus hardware. Relocation utilities must be used that actually take the place of the DOS loader. The designer must have control over the destination load address during their relocation, so that the system can be told where the program will reside for test in the STD environment. A download utility, STD bus resident monitor and PC terminal emulation are needed to debug the software through the PC in an STD bus environment.

A less obvious but equally powerful concept is the development of STD-Z80 systems on the PC. With cross assemblers and cross compilers, even this can be accomplished. Micro/Sys is currently delivering this hardware/software package in addition to the 8088 package.

During 1983, the number of STD bus boards produced and sold approached that of Multibus, even though the actual amount spent was 20% of that spent on Multibus. This is to be expected considering that the relative cost of an STD board is 20% of a typical Multibus board. Designers began looking for boards with more flexibility and multiple functions to reduce the card count and system cost. Also, an increasing number of companies, wanting to computerize their industrial control and processing, began adapting low-cost, prepackaged nonindustrial computers for the task, such as the IBM PC. Hence, the PC became an adversary rather than a complement to the STD.

According to Jim Gesner, applications manager at ISI International (Sunnyvale, CA), the readily available and growing market of IBM PC-compatible software and low-cost systems is effectively attracting system integrators who might otherwise have opted to use the STD bus. This is undoubtedly being encouraged by the rapid growth in available industrial and communication interface adapter boards.

Gesner noted that throughout 1984 there was a flattening of growth in STD products. Even the growth of systems that use

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	Vcc	In	Logic Power (+5 VDC)	2	Vcc	In	Logic Power (+5 VDC)
	3	GND	In	Logic Ground	4	GND	In	Logic Ground
	5	VBB #1/VBAT	In	Logic Bias #1/Bat Pwr	6	VBB #2/DCPD*	In	Logic Bias #2/Pwr Dwn
DATA BUS	7	D3/A19	In/Out	Data Bus/Address Ext	8	D7/A23	In/Out	Data Bus/Address Ext
	9	D2/A18	In/Out		10	D6/A22	In/Out	
	11	D1/A17	In/Out		12	D5/A21	In/Out	
	13	D0/A16	In/Out		14	D4/A20	In/Out	
ADDRESS BUS	15	A7	Out	Address Bus	16	A15/D15	Out	Address Bus/ Data Bus Ext.
	17	A6	Out		18	A14/D14	Out	
	19	A5	Out		20	A13/D13	Out	
	21	A4	Out		22	A12/D12	Out	
	23	A3	Out		24	A11/D11	Out	
	25	A2	Out		26	A10/D10	Out	
	27	A1	Out		28	A9/D9	Out	
	29	A0	Out		30	A8/D8	Out	
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Pushbutton Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground	54	AUX GND	In	AUX Ground
	55	AUX +V	In	AUX Positive (+12 VDC)	56	AUX −V	In	AUX Negative (−12 VDC)

*Low-level active indicator

Figure 1: STD bus connector pin assignment: note the proposed multiplexing of the upper eight address lines (A8-A15) to incorporate 16-bit processors.

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VERSAbus†	4 Mbyte DRAM	•	•	8/16/32	300nS	300nS	•	
iLBX	2 Mbyte DRAM		•	8/16	200nS	200nS	•	
Bubble	2 Mbyte		•	—	36mS	36mS		•

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Circle 70

the PC for development or control but interface to STD bus expansion chassis for the industrial connection appear to have very limited market share. Nevertheless, the STD bus is still a low-cost viable alternative to systems integration that is currently supported by a variety of vendors.

The push towards supporting processors with higher performance continues. Over the past seven years, the STD bus has adapted and evolved, incorporating the latest technology to avoid obsolescence. The latest effort is for manufacturers to incorporate 16-bit processors with full 16-bit-wide data transfers (**Figure 1**). Presently, 20-bit memory addressing is supported by the STD bus using a multiplexed address scheme allowing 1 Mbyte of direct addressing. This same multiplexing concept has been proposed to provide full 16-bit-wide data transfers on the bus while offering compatibility with existing I/O cards.

The only limitation to the new scheme is that old 8-bit memory cards cannot be used with the 16-bit specification, because it is possible for data to be transferred as a low byte, high byte or full word. Currently designed 8-bit memory boards cannot be forced to differentiate between the three states, since they always assume a low-byte transfer.

Requiring a new memory card is, however, not new to the STD. A new card was also needed when 20-bit memory addressing was introduced to support the extended addressing capability of the 8088 and the 68008 processors. According to Jerry Winfield, president of Winsystems (Arlington, TX), data transfer speed can be increased with the addition of a new memory card. Memory cards of 8 MHz can be supported, permitting both the 8086 and the 68000 to run at full speed without wait-state generation. Although memory-mapped I/O cards cannot be supported by this particular 16-bit processor systems architecture, this should not be a problem since nearly all cards are I/O mapped. Most manufacturers having memory-mapped cards also have an I/O map option on board. Even 6809 and 6800 processor cards generate an I/O cycle rather than a memory cycle for their cards.

The development of the STD bus may put pressure on VME board manufacturers to lower the cost of their cards. The 16-bit STD bus has gained performance and cost advantages over the single-card, and some double-card, VMEbus systems. Furthermore, the STD bus is inherently less expensive than the VME; it has 56 bused lines, the VME card has 96. This means fewer bus drivers are needed; therefore the STD bus has a lower associated cost. The STD bus drivers are controlled by simple gating, which many manufacturers have put into inexpensive

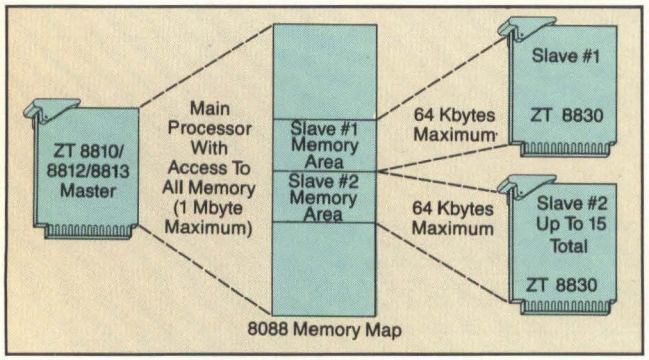

Figure 2: In Ziatech's multimaster scheme, a dual-port RAM is used on slave CPUs.

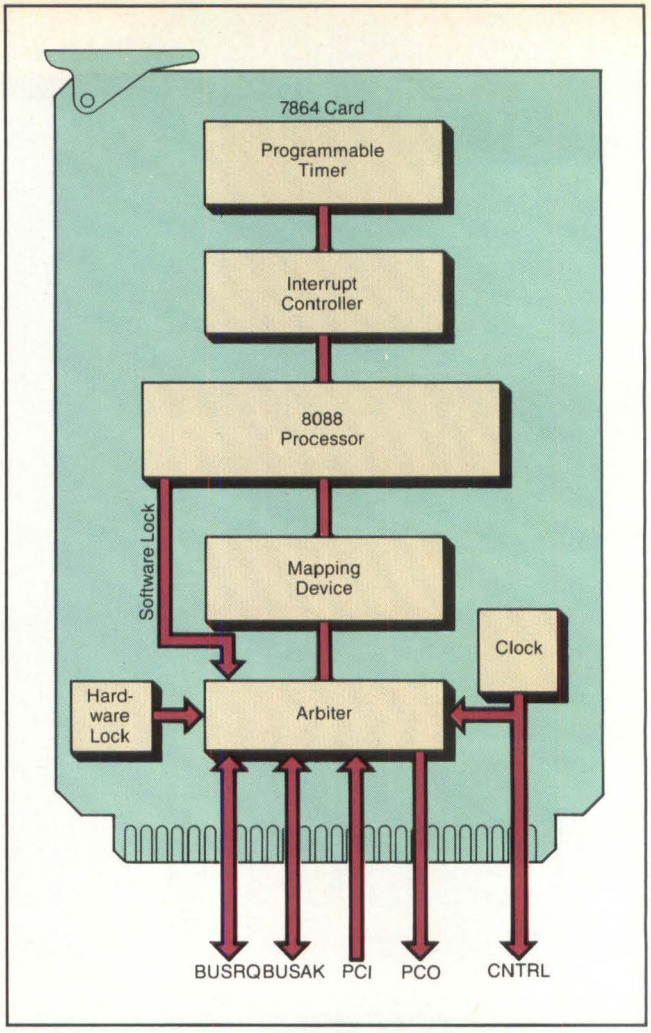

Figure 3: Pro-Log's true multimaster approach is implemented using five of the STD bus control lines.

fuse programmable logic arrays. The VMEbus logic requires complex LSI devices which are only now becoming available.

The STD bus system brings power and ground to the card through dual-power buses located at opposite edges of the card, whereas the VME brings power and ground over widely scattered pins on the A, B and C rows of the DIN connector. According to Fred Beckhusen, vice president of engineering at Micronyx (Richardson, TX), using a standard 50-mil-wide power etch, it is impossible to get power to a two-layer VME card. The only solution is to use a multilayer (four or more) construction. For example, Mostek's double-height VME-DRAM 256 uses eight-layer construction to put 36 RAM ICs on a card nearly three times the size of the STD bus. On the other hand, the STD bus has four-layer cards with the same density of memory devices in a much smaller size. The reliability of the DIN connector on the VMEbus is often promoted as a distinct advantage. But there are some who feel that this is mostly hype. "I have seen reports that the connector is no more reliable than any other," says Philip Hayes, "though it is very expensive." He also criticized the 16-bit enhancements to the STD bus. "The European Gespac (Mesa, AZ) G64/96 offers a better approach; however, no new bus format will offer the two main attractions of the STD—low cost and a large existing installed base."

Although the VME is a high-power bipolar bus, the STD has a wide range of all-CMOS cards available to the system's integrator, which may be used where noise, temperature or power

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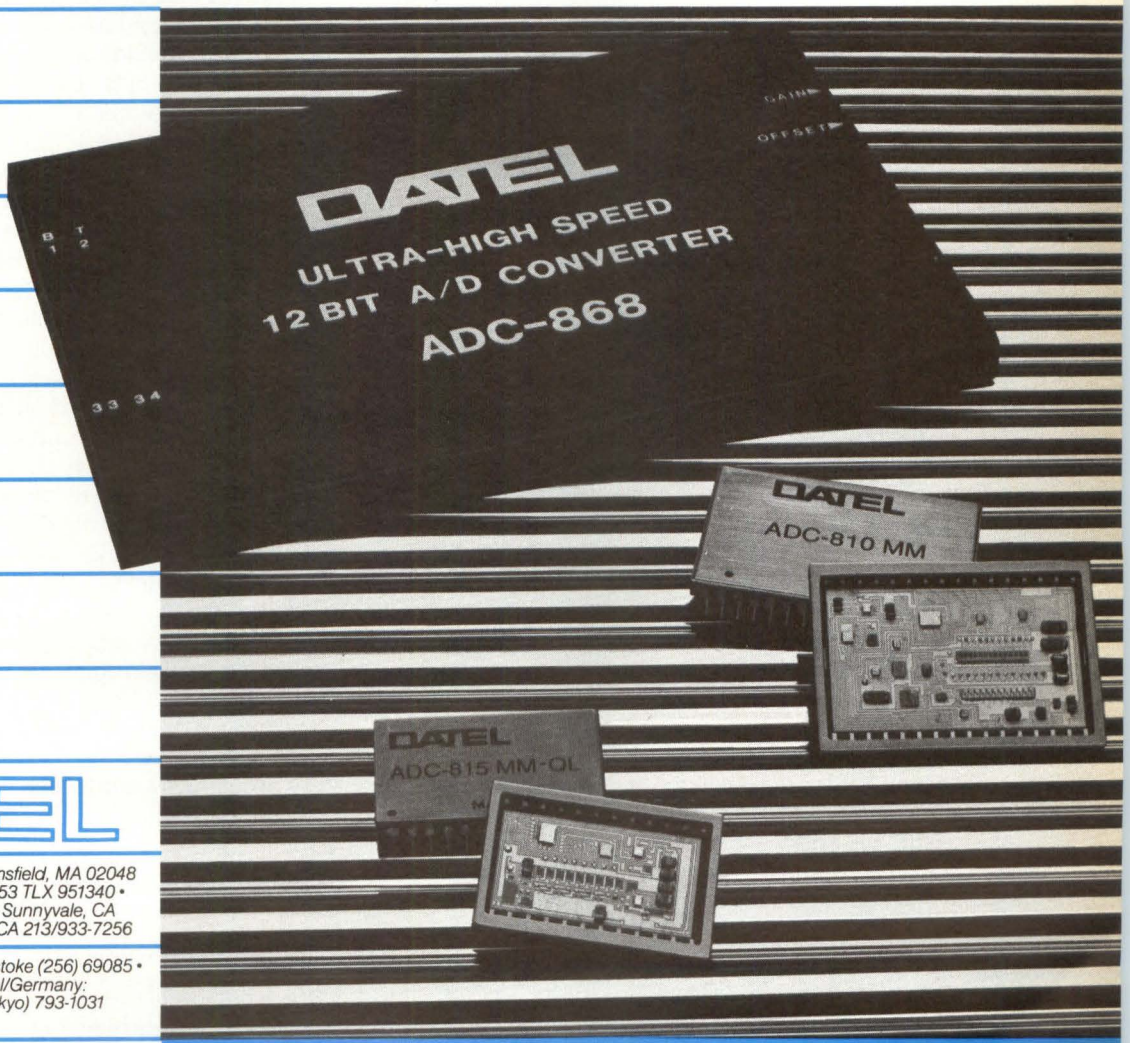

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Circle 22

requirements are extreme. Because of CMOS and 16-bit STD specifications, the Harris (Melbourne, FL) 80C86 processor may be one of the first all CMOS microprocessors ported to the new STD bus. Improving the performance of the STD by placing higher performance processors on the bus is not the only way to enhance systems throughput. In many cases, much of the processing overhead can be moved to intelligent I/O cards, like Mostek's serial and GPIB interface cards.

The STD bus has been limited in allowing multiple masters to obtain control of the bus. The Multibus and Q-Bus, on the other hand, have always had extensive support for multiple masters, with the expense of more bus interfacing and real estate. With just two backplane lines, bus acknowledge (BUSAK) and bus request (BUSRQ), the STD could only support a CPU card and one other bus requesting card. The early solution to the problem was to take the single BUSAK line and radially distribute it to four bus-requesting DMA channels, each prioritized and arbitrated. This allowed up to four DMA-based devices to access a global memory resource on a backplane cycle-steal basis. According to Finster, a second CPU in the same STD bus card rack poses similar problems. In order for both CPUs to be able to access the same memory or I/O resource through the backplace, some form of arbitration must be used to manage the resource. Ziatech proposed a method which uses a dual-port RAM on the slave CPU (**Figure 2**). The RAM is the only resource available to both CPUs. It requires the "locking out" of one CPU while the other uses the memory. Its advantage is throughput; a significant block of data in memory can be available to a CPU very quickly. The disadvantage is the need to select an addressing scheme for the dual-port memory. A slave is limited to either Z80 or 8088 systems. The scheme is achieved via a 3-bit cascade address, multiplexed on the STD bus bits A8-A10.

Another approach to the problem, proposed by Pro-Log, is to use a full multimaster CPU arbitration through the backplane. Unlike the Ziatech scheme which is open to other manufacturers, the Pro-Log scheme is proprietary. However, Paul Virgo, marketing manager at Ziatech, stated that the scheme may be available to other manufacturers in the future.

Pro-Log has implemented its multimaster arbitration interface on its new 7863 and 7864 8088 CPU cards. This has been achieved by a PAL implemented arbiter interface to the STD bus that allows up to 16 CPUs to exist on the bus simultaneously. The arbiter uses five of the STD bus control lines on its implementation (**Figure 3**).

Bus Request and Bus Acknowledge are the two control signals used by the arbiter to indicate when a processor is requesting the bus and when the bus is in use. The priority chain lines are used to prevent multiple processors from requesting the bus simultaneously. Normally, each processor has equal access to the bus. The control line (CONTRLO) is used to synchronize all of the arbiters on the bus. The arbiter can be software configured to operate in one of four fundamental modes; Hardware Lock, Software Lock, Equal Access and DMA Lock. In the Hardware Lock configuration, the CPU sets an output port lock signal. Sensing this, the arbiter keeps the Bus Acknowledge asserted, preventing any other processor from accessing the bus until the lock signal is reset.

The Software Lock is initiated by insertion of a lock prefix to an 8088 instruction. The prefix locks the Bus Acknowledge line

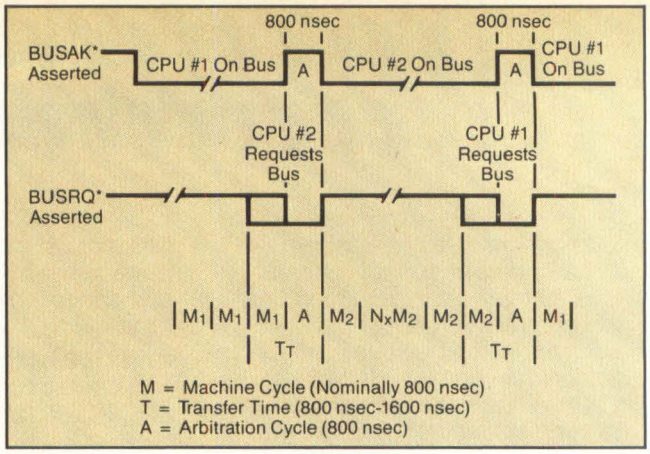

Figure 4: Multimaster bus exchange timing for Pro-Log's implementation.

and prevents any other processor from accessing the bus until the instruction is completed. The equal access mode allows all processors to have equal access to the bus, and any arbiter can initiate a Bus Request when the bus request line is not asserted. At the time of a request, a processor on the bus must release the bus at the end of its current machine cycle. The requesting processor's arbiter then acquires the bus. If there is no pending bus request, arbitration does not take place and the bus remains a continual resource to the present processor (**Figure 4**).

The DMA lock mode is jumper configured. The processor card highest on the priority chain must be selected. This jumper reconfigures the Hardware Lock signal and allows the priority chain line (PCO) to be disabled under program control. All lower priority multimasters are prevented from accessing the bus under these conditions. The Bus Request and Bus Acknowledge lines accommodate DMA operation. The advantage of this approach is that true multiprocessing can be implemented. The disadvantage is that multimaster CPU's cannot access each other's memory and some STD bus signal lines are used in ways other than those in common use over the past seven years.

Finster stated that while the approach is sensible for the Multibus, VMEbus or Q-Bus it may be overkill for STD systems. The Micro/Sys approach is an I/O-mapped slave with its own CPU attached. Two (or more) CPUs cannot access each other's I/O or memory, but must communicate through I/O-mapped mailbox registers. However, each has the ability to interrupt the other CPU to get its attention. The advantages include operation with virtually any host CPU and lack of arbitration hardware. The disadvantage is throughput, as all data goes through a byte-wide channel.

Through the support of 16-bit processors, the STD will continue to hold the low-end process control market and will grow into the low-end minicomputer market. The CMOS bus standard will provide a new market for the STD that is not likely to be challenged by higher performance buses such as VMEbus and Multibus. Low-cost development tools based on the IBM PC will continue to aid system integrators by supplying them with more versatile and easier to use tools. **DD**

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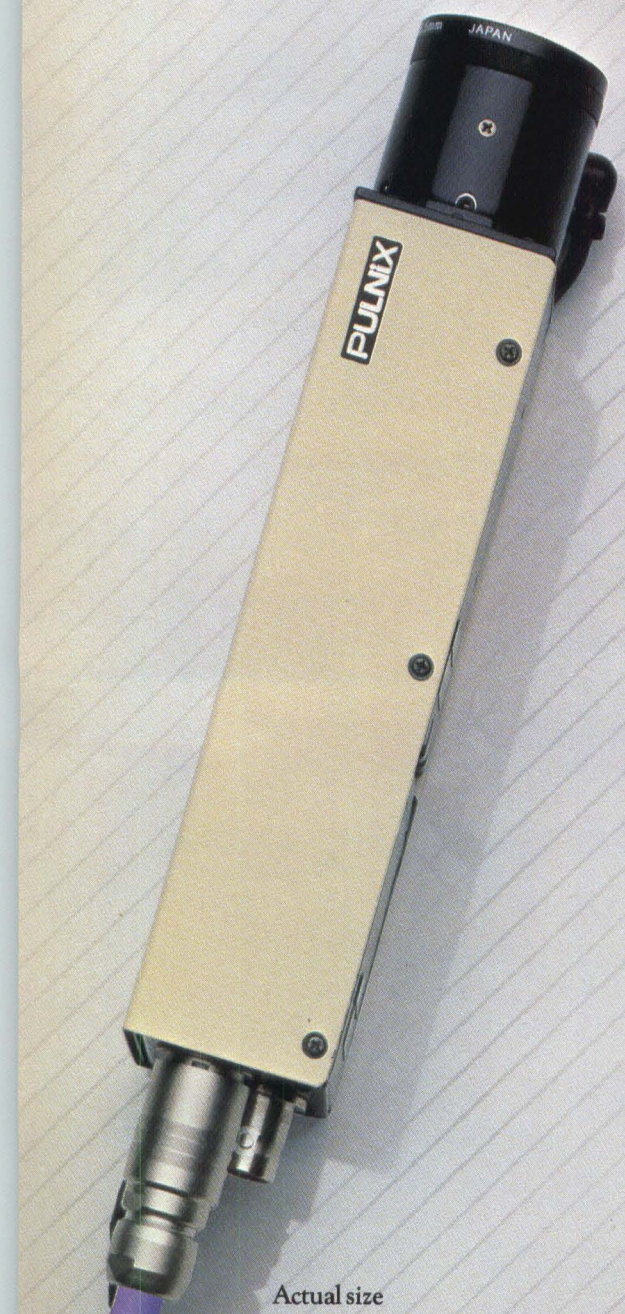

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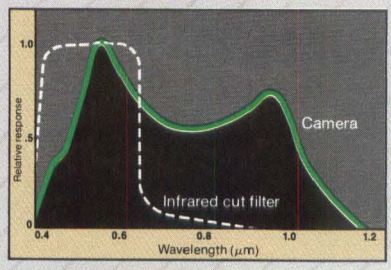

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Microcontroller Eases I/O Processing Burden

by Sunil Baliga, Gregory Goodhue and Jesse Jenkins, Signetics, Santa Clara, CA

High-speed control applications are characterized by the need to test and perform operations on system inputs which are not necessarily in a fixed format or a given length. Typical system requirements are testing one or more flags on a polled or interrupt-driven basis, setting or clearing of subfields within a byte boundary, transferring large amounts of data in a short time and controlling peripheral devices. Concurrent with these operations is the need for predictable real-time response, accurate and tight timing loops, fast conditional branching and basic computational ability. These attributes must be performed at speeds which may be beyond the operating ranges of conventional microcontrollers.

The Signetics 8X401 microcontroller (**Figure 1**), which uses the Harvard architecture, allows pipelining address generation and instruction fetching with parallel instruction decoding and execution. This concurrency results in consecutive read-modify-write cycles, using either external or on-chip memory as either source or destination. The result is executed in a minimum of 150 nsec. The 8X401 represents a functional and performance enhancement over the Harvard architecture found in Signetics 8X300 and 8X305 microcontrollers.

The 8X401 microcontroller is a monolithic CPU implemented in Emitter-Coupled and Emitter-Follower Logic (ECL and EFL). It controls a series of peripheral devices which are attached to it by means of a standard 8-bit I/O bus. The 8X401 can be integrated into most support systems using the 8X300 and 8X400 family support devices.

The 8X401 microcontroller has a fixed instruction set with full on-chip decoding. The user is then spared from the details of writing or understanding microcode, as in bit-slice microcontrollers. The 8X401 has 32 instructions (**Table 1**), which

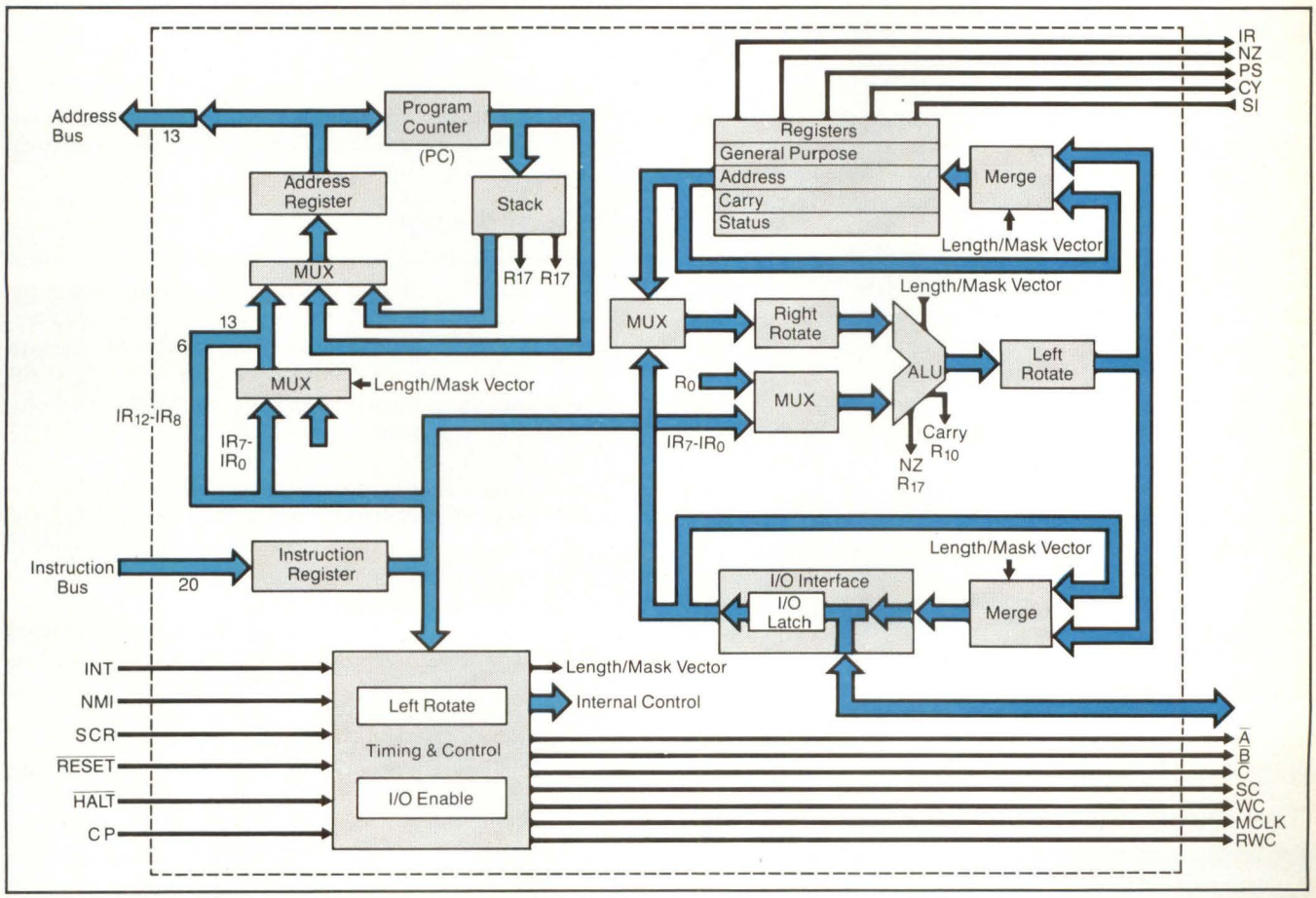

Figure 1: The Signetics 8X401 microcontroller uses the Harvard architecture and allows pipelining address generation and instruction fetching with parallel instruction decoding and execution.

besides such general arithmetic/logic operations as ADD and XOR, includes a variety of conditional jumps and returns.

All instructions are 20 bits long, and instruction memory is 8K words deep. Arithmetic/logic operations may be performed on 1 bit to 8 bits of the operand data subfield. Thus, a subfield (from a data byte) can be selected, an operation performed on it and the result written back to the source byte without disturbing the other bits. To expedite such operations, the 8X401 has an 8-bit ALU with full rotate/merge capabilities. A selectable wrap-around carry is present, allowing multiple byte additions. When a data byte represents the control signals to a peripheral, the 8X401's subfield manipulation ability obviates the need to read the entire byte back to the destination field.

The 8X401 has an independent address section with an independent 13-bit address arithmetic unit and a four-level push-down stack. The chip has status flags (Carry, ALU Not Zero, User Programmable Status Bit and Interrupt Receivable) pinned out as well as register addressable. A Status Input pin is provided which is sampled every cycle and can be used as a serial input, simplifying interprocessor communications.

To implement parallel transacting, three bank-select signals are provided, acting as ninth address bits when accessing data memory. These can switch between the input and the output phases of the same instruction to avoid addressing data memory when executing read-modify-write cycles on external memory. Only one of these signals is active during a peripheral read cycle, but one or two may be active during a write cycle, allowing data to be simultaneously written to two different addresses in external memory, which is particularly useful during initialization. The information conveyed by the 8X401 I/O interface is sufficient to allow 8X400 and 8X300 family peripherals to be attached directly to the 8X401 with no decoding or multiplexing/buffering glue. High-speed, high-throughput systems with minimal chip counts can then be configured with the 8X401 microcontroller.

To complement the 8X401 and to provide compatible interface functions, both the 8X470 I/O port and the 8X450 256-byte RAM fit directly on the 8X401 DA bus. The 8X470 I/O port may have each bit independently fuse programmed as a driver, receiver or latch (from either side) and may supply a status bit to the 8X401 on any specifically programmed bit. This feature, called multiport polling, allows clusters of 8X470s to comprise a composite virtual status register.

The 8X450 is a high-speed static RAM which may be viewed as a register array extension, data buffer or general scratch pad. Two addressing modes allow direct 8X401 interfacing whereas another mode allows the part to be used easily with other standard microcontrollers and microprocessors.

When not using 8X401 family peripherals, the 8X401 microcontroller has an input signal termed Slow Clock Request (SCR) which doubles the executing time of one instruction to transact with slower peripherals. Thus, the entire I/O family of 8X305 and 8X300 microcontrollers may directly interface with the 8X401.

The 8X401 As An I/O Processor

Personal computers are growing increasingly more powerful. Computers which support a variety of peripherals and provide color graphics and network capability are not uncommon. In many of these systems the main processor is called upon to perform routine I/O control operations, in addition to running the user's application program. System performance would be improved if any of the tedious I/O control tasks could be offloaded from the main processor.

Instruction Type	Variation	Description
ADD	ADD	ADD
	ADC	ADD with Carry
	AD8	ADD Immediate 8
	AD5	ADD Immediate 5
AND	AND	AND
	AN8	AND Immediate 8
	AN5	AND Immediate 5
JUMP	JIF NS	JUMP IF SI = 0
	JIF S	JUMP IF SI = 1
	JIF NC	JUMP IF Carry = 0
	JIF C	JUMP IF Carry = 1
	JIF Z	JUMP IF ALU = 0
	JIF NZ	JUMP IF ALU < > 0
	JSR	JUMP to Subroutine
	JMP	JUMP
	PSJ	POP STACK AND JUMP
MOV	MOV	MOVE
RETURN	RIF NS	RETURN IF SI = 0
	RIF S	RETURN IF SI = 1
	RIF NC	RETURN IF Carry = 0
	RIF C	RETURN IF Carry = 0
	RIF Z	RETURN IF ALU = 0
	RIF NZ	RETURN IF ALU < > 0
	RTN	RETURN
	RCC	RETURN and Clear Carry
	RSC	RETURN and Set Carry
XEC	XEC	Execute
XMIT	XT8	Transmit Immediate 8
	XT5	Transmit Immediate 5
XOR	XOR	Exclusive OR
	XR8	Exclusive OR Immediate 8
	XR5	Exclusive OR Immediate 5

Table 1: The 8X401 has a variety of instructions that includes conditional jumps and returns.

With its bit-manipulation orientated instruction set, and its 150-nsec instruction cycle time, the 8X401 is suited for I/O control applications. It can be used as an I/O processor in personal computer applications (**Figure 2**).

System Design

The 8X401 offloads various I/O control tasks from the host processor (**Figure 2**). These I/O tasks, which are controlled by the 8X401, include a 640 × 320 color display, a high-speed network, a parallel printer, a serial port and a keyboard. The host processor in this system is a 68000 microprocessor. The 8X401 presents a high-level software interface to the 68000. Host commands on I/O devices, such as DRAW LINE and TRANSMIT TO NETWORK, are implemented by the 8X401.

The hardware interface between the 8X401 and the 68000 is an 8X320 Bus Interface Register Array chip. The 8X320 can be thought of as a mailbox; it interfaces two independent ports, a primary and a secondary port, using either 14-byte or seven-word addressable data registers. Also within the 8X320 is a 16-bit flag register, which also can be either byte or word accessed. The 8X320 maps one status flag for each of its 14-byte data registers. When either the 68000 or the 8X401 writes to a data register, the appropriate flag is set. The status flags can then be polled to facilitate interprocessor communications.

The secondary port of the 8X320 is tied directly to the 8X401 I/O bus and is mapped onto its A bank. No external "glue" gates are needed. The primary port of the 8X320 is tied to the 68000's local bus. This interface requires the addition of only three glue gates, one OR gate, one NAND gate and one open collector buffer. The 68000 can then access the 8X320 either in byte or word mode. With byte-mode addressing, odd-address bytes are

(continued on p. 85)

(continued from p. 80)

transferred over the 68000's lower data lines, D0-D7. Even-addresses are transferred over the 68000's upper data lines, D8-D15. With word-mode addressing, data is transferred over the entire 16-bit data bus of the 68000. Both read-modify-write and test-and-set classes of instructions are supported at the 68000/8X320 interface.

The various I/O devices of **Figure 2** interface to the 8X401 through eight 8X470 programmable I/O ports and one 8X360 Memory Address Director (MAD). The 8X360 and two of the 8X470s are used to interface to the bit-mapped graphics memory. These peripheral devices are all mapped onto the 8X401's A bank. The 8X360 and the two 8X470s tie directly to the 8X401's I/O bus; no external glue or buffering is needed. The 8X360 generates the address needed to access pixel information contained in the bit-mapped memory. Data that can be either written to or read from the graphics memory is held in two 8X470s.

Two 8X470 I/O ports are needed to interface the 8X401 to the high-speed network. One 8X470 contains data to either be sent to or received from a serializer/deserializer. The other 8X470 is used to monitor and control various other signals needed to implement the network interface.

Because the printer used in **Figure 2** is a parallel printer, the 8X401 requires one 8X470 port to send 8-bit ASCII data to the printer. Printer control and status lines are integrated into the system through a second 8X470. This second control and status 8X470 has additional capability above and beyond the printer interface. This excess is consumed by the serial port and keyboard interfaces.

The two remaining 8X470s are used to complete the UART and keyboard interface. One 8X470 is used to send or receive data from the UART. The second 8X470 is used to receive parallel data from the keyboard. In addition to the eight I/O 8X470s, the system contains one timer/counter 8X470. This port is used to interface the 8X401 to the timer/counter, which is used in system operation.

To improve system performance, it is desirable to provide first-in, first-out (FIFO) buffering for the network, the printer, the UART and the keyboard. The 8X401 implements FIFO buffers for these devices using an 8X450 256-byte RAM and software. This 8X450 is allotted all 256 locations on the B bank.

The 8X401 has 13 general-purpose registers on-board. In order to allow additional temporary storage capability, an 8X450 RAM has been added to the system (**Figure 2**). With devices already residing on the 8X401's A and B banks, the 8X450 is mapped onto the C bank. If desired, portions of this program storage 8X450 can be reassigned for additional FIFO storage.

The software configuration of the system is resident in the 8X401 program PROMs. The software consists of a basic real-time operating system and five applications modules (device drivers), one for each I/O device. The device drivers contained

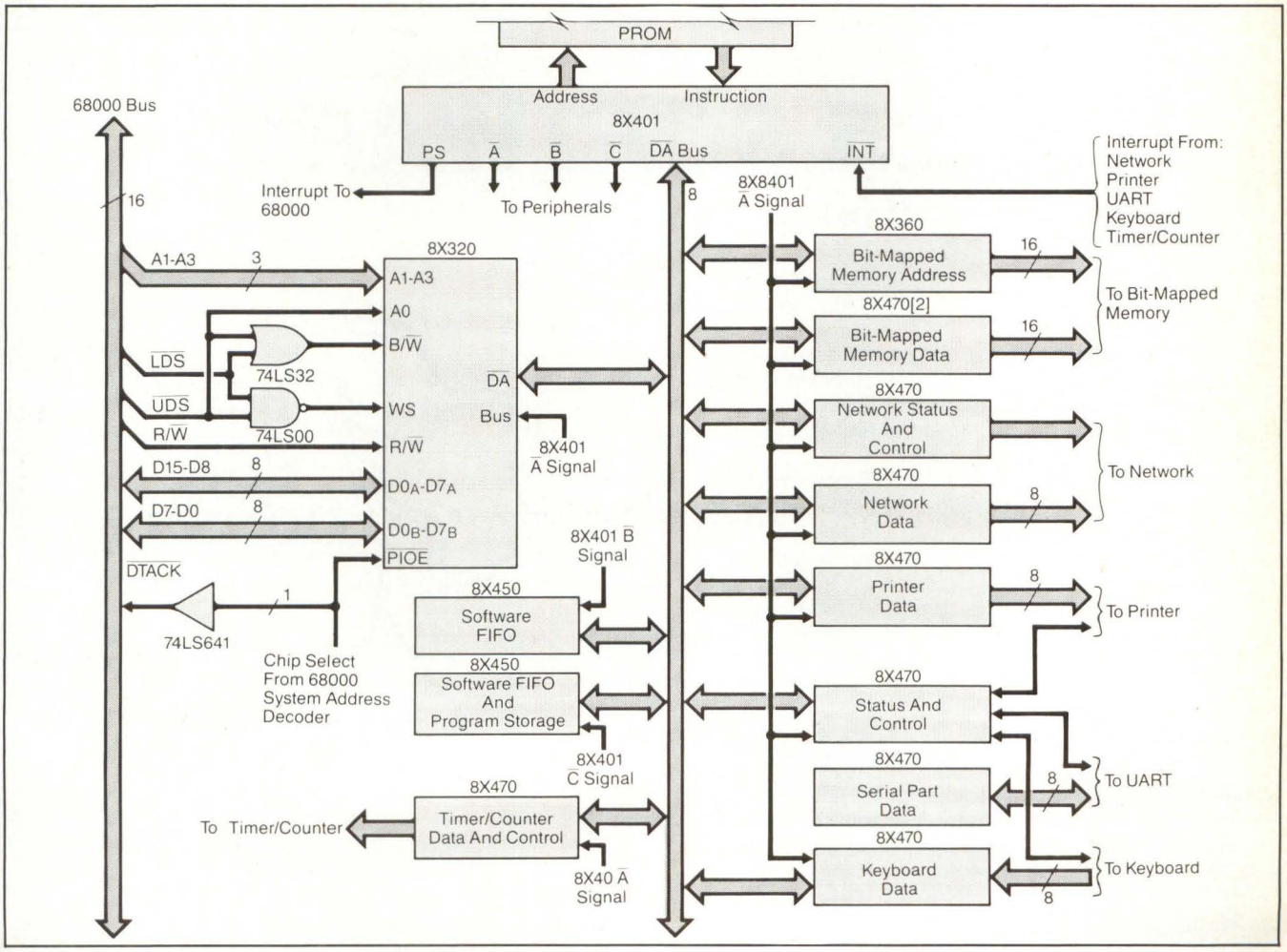

Figure 2: The 8X401 may be used as an I/O processor in personal computer applications.

in PROM perform the actual control of each of five I/O devices.

The operating system has three major parts, a process scheduler, an interrupt handler and a 68000 communications package. The I/O system may have multiple I/O devices active simultaneously. For example, the 68000 may have instructed the 8X401 to send data to both the printer and the serial port. The system may then have multiple device drivers simultaneously active.

To provide each I/O applications module some processing time, process scheduling with a time-slice algorithm is used. The process scheduler selects which active process is allowed to run next. Depending upon its priority, this selected process is allocated a specific amount of microcontroller time. The allocated time is loaded into the timer/counter 8X470 on the A bank, and the process is allowed to run. When the allocated time expires, an interrupt is generated by the timer/counter. The applications program is then interrupted and control is returned to the operating system.

In addition to handling interrupts from the timer/counter, the 8X401 must handle interrupts from the network, the UART and the printer. The interrupt handler determines the highest priority interrupt pending and takes the necessary action.

The last major part of the operating system is the 68000 communications package. Communication between the two processors is bilateral, with both the 68000 and the 8X401 communicating with each other through the 8X320. This communications package can be divided into two portions – a 68000 command module and an 8X401 request module. The 68000 command module, at every time-slice interrupt, polls the 8X320 to determine if any 68000 I/O commands have been given. If a command has been input to the 8X320, the 8X401 takes the appropriate action.

Only the 8X401 request module is allowed to communicate with the 68000. Any device driver which needs to communicate with the 68000 will make a system call. These system calls are responded to at time-slice boundaries, with the 8X401 request module activated. This module polls the 8X320 to determine if space for the device driver's message is available. If space is available, the message is stored in the 8X320 and a 68000 interrupt is generated. This interrupt is asserted using the 8X401's Programmable Status (PS) output pin. When the 68000 acknowledges this interrupt, through the 8X320, the 8X401 releases PS, removing the interrupt. If there is no space available in the 8X320, all messages from device drivers are stored in the 8X450 mapped on bank C.

As power increases in personal computers, greater burden is put on the main system microprocessor. The 8X401, implemented as an I/O processor, can help relieve some of this increased burden on host processors, improving overall system performance as well as price/performance ratio. DD

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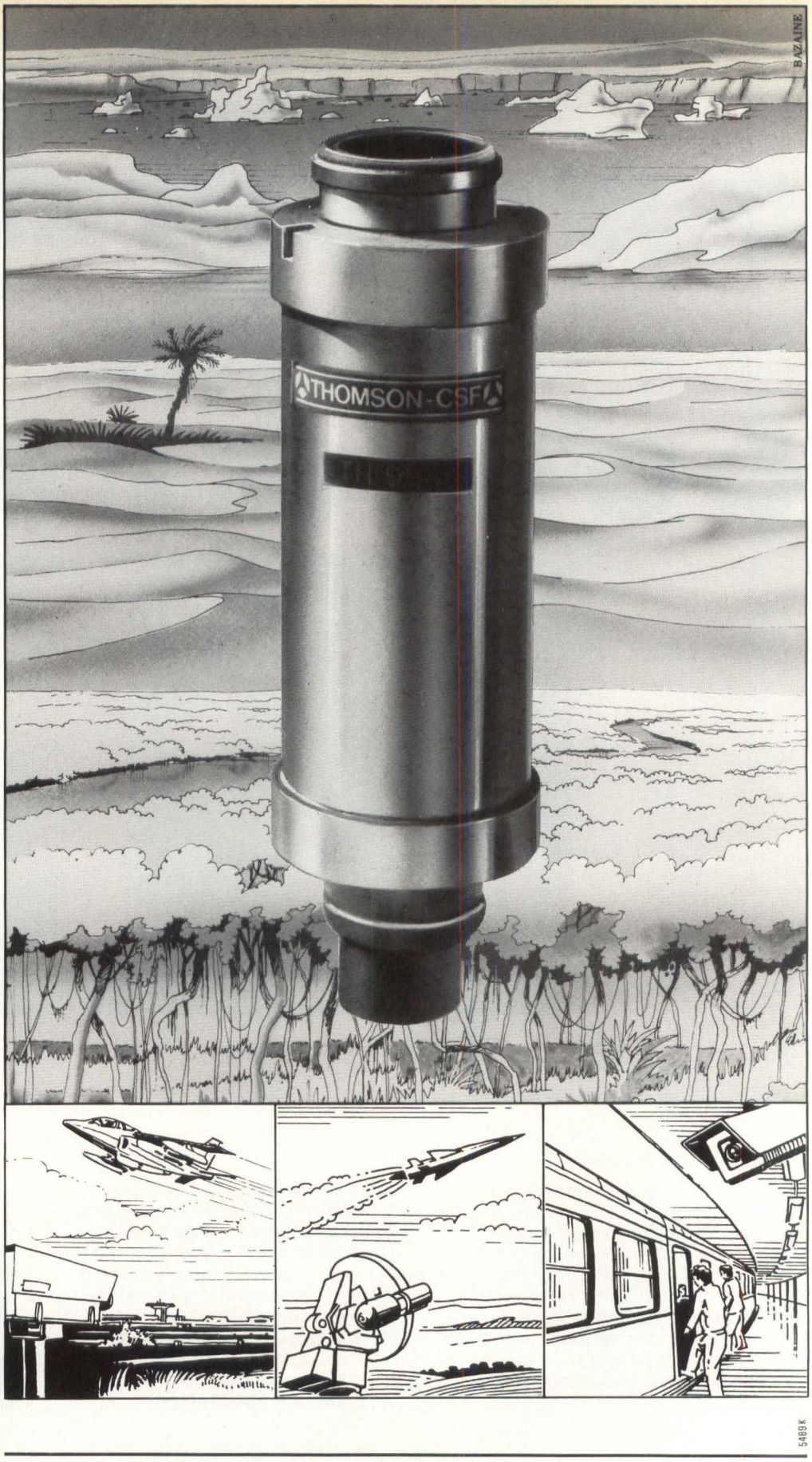

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NEW PRODUCT FOCUS

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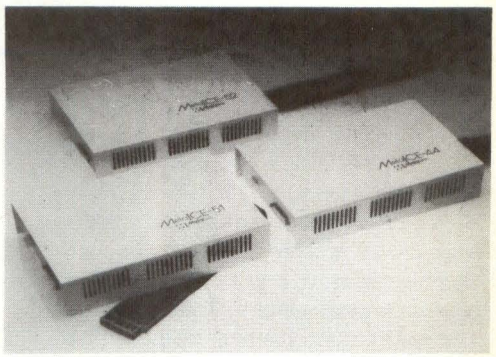
In-Circuit Emulators Use Equivalent Of 8051 Bond-Out Chip



A family of in-circuit emulators for the 8051, 8052 and 8044 single-chip microcomputers is now available from MetaLink Corp. (Chandler, AZ). Running on IBM PC or compatibles with an RS-232-C interface, each provides real-time, transparent emulation up to the maximum 12 MHz operating frequency of the microcomputers. The MetaICE-51 emulates the 8051 chip; MetaICE-52 emulates the 8052, and MetaICE-44 supports the 8044.

Since an 8051 bond-out chip is not marketed by Intel, MetaLink had to develop its own, and the company's functional equivalent of such a chip is resident in the MetaICE series. The 8051 MetaICE series has a menu-driven interface with on-line help facility rather than a command-driven interface. Up to 16,000 hardware breakpoints can be provided by the series' breakpoint mechanism. Other features of the MetaICE products include a disassembler, single-line assembler, save/restore system state, examiner/modify capability of all chip memories, dump/enter/fill/move/search/compare memory commands, experiment editor/compiler, opcode class editor, software simulator mode and optional symbolic debug capability.

In addition to an IBM PC or compatible, the system requires PC-DOS Version 2.0 or later version, 256 Kbytes memory, one floppy disk drive (MetaLink recommends two) and RS-232-C interface and cable. Operating requirements are +5 VDC at 2.0A, +9 VDC to +15 VDC at 150 mA, -9 VDC to -15 VDC at 150 mA. MetaICE-51 is priced at $2,895, MetaICE-52 is $3,195 and MetaICE-44 is $3,295.

—Lamneck
Circle 230

S O F T W A R E

Toolkit Integrates VLSI Design And Test

Intended to ease the design and generation of test patterns for VLSI designs, TesTools from Test Systems Strategies (Beaverton, OR) extracts necessary information from CAD/CAE databases and generates programs for multiple test vendors. The first tool in the package, Pattern Bridge, provides the critical link between the circuit designer's simulation results and the test patterns created by the test engineer. Pattern Bridge converts simulation files directly into test pattern files compatible with the target test system. Information that is extracted and reformatted includes test vectors, format/timing, input/output control and pin definitions. This enables the test engineer to use the circuit designer's simulation results as actual test patterns on the target tester. Test engineers can then determine the optimum conversion format for the desired tester configuration. This format automatically converts patterns from one tester to the other.

In addition, designers can use the test patterns created by test engineers to exercise their design in the simulator, an interaction previously not possible. This provides designers with a record of actual device behavior to compare with their simulations, thus improving prototype evaluation. Test patterns developed by test engineers can also be run on a fault simulator after conversion by the tool so test engineers can assist designers in evaluating the prototype.

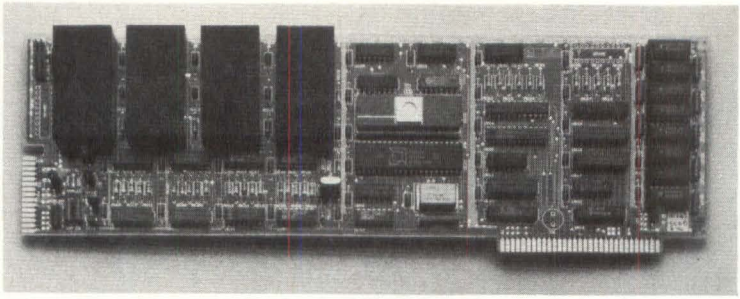
The second tool, a pattern editor, enables test engineers to build a pattern to test a simulated design. Previously, design or test engineers needed to perform a large number of data entries to create or modify a test pattern. The Advanced Pattern Tool accelerates this process with multiple-format pattern generation, the ability to use Boolean operators and equations to compute pattern data from old data, as well as text editing for comments and pin definitions.

Test Systems Strategies also provides the Emulator Modeling Utility for any test engineer who does not have access to a design simulator. It combines an intelligent pattern editor, logic emulator and symbolic assembler to simulate VLSI devices.

The TesTools family is available for use on UNIX, VMS, Aegis and RSX-11 operating systems with configurations for popular design systems, simulators and VLSI testers. The Pattern Bridge ranges from $6,000 for workstations to $12,000 for VAX-11 configurations. The Advanced Pattern Tool ranges from $5,000 for workstation use and $10,000 for use on the VAX-11. The Emulation Modeling Utility is $12,000.

—Aseo
Circle 232

Digitized Audioboard Provides Phone Line Information



A circuit board for the IBM PC/XT, PC/AT or compatible and a software driver provide interfaces for four telephone lines, which can be used to dispense information with toll-quality audio. The four audio channels of the NITA product, using prerecorded rather than digitized voice, can operate simultaneously with other applications on the PC. This is the initial product from Innovative Technology Inc. (ITI) (Roswell, GA).

The line interfaces are 64 Kbit/sec codecs as used for digitized telephone lines. Either 64 Kbytes or 256 Kbytes of dual-ported memory on-board stores the digitized speech as it is spooled off the PC's Winchester disk via DMA. By using the DMA channel, the PC can operate other applications and run NITA in the background. Combined with prerecorded speech, the voice quality is excellent.

A permanently installed re-entrant software driver controls the audioboard's operation and applications. Designed for OEMs and VARs, the NITA driver is written in C for portability. Other aids to software development include two demo application programs and their source code, an interface to the device driver and a simulator for both the PC board and the driver software.

This is one of the first telephone automation products designed for OEM use; ITI provides tools for writing applications rather than tailoring the product for one specific application. In addition, the dual-port memory allows the PC, which controls the system, to run other applications concurrently. NITA requires only about 25% of the PC's ability, mostly in disk access rather than processing power.

Use of all off-the-shelf parts including large RAM chips and single-chip implementations of codecs, DTMF receiver and microcontroller functions, makes the board simple. Price for the board plus driver and sample applications is $1,995 quantity 1-4, with discounts up to 40% for 40 pieces or more.

—Pingry

Circle 231

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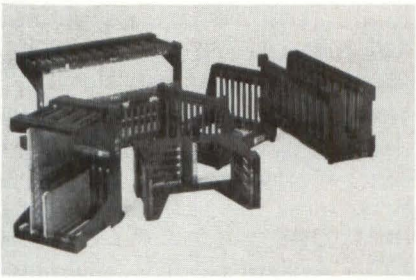
Circle 43

COMPUTERS/SYSTEMS

Open-Frame VME Card Cages



A series of open-frame double-height VMEbus card cages with integral backplanes have been designed to allow mounting in any attitude on any of four surfaces. They are constructed of anodized aluminum with a single motherboard backplane for the VMEbus and separate connectors from the I/O channel, with provisions for a P2 bus. Cages are available with 3, 5, 7, 9, 12, 16 or 20 slot capacity. Unit prices start at $295.00. **Electronic Solutions**, San Diego, CA
Circle 128

Multiple-Node Processor System

Introducing a modular expansion approach to real-time computing applications, the SCI-Clone/32 uses Gould CONCEPT/32R minicomputers connected by a Reflective Memory System (RMS) to provide a real-time distributed database. The RMS distributes computer intelligence among several nodes simultaneously, providing automatic replication in real-time. Modularity allows the SCI-Clone/32 system to assign individual tasks to independent but closely interacting parallel processing nodes (CONCEPT/32 computers). Priced from $277,200 to $1,377,000. **Gould**, Ft. Lauderdale, FL **Circle 132**

Color Workstation With MicroVAX II

The VAXstation 520, based on the high-speed floating point processor introduced with Digital's MicroVAX II, includes 2 Mbytes of main memory, DEQNA Ethernet interface, MicroVMS operating system, 32-Mbyte Winchester disk and dual 400-Kbyte floppy disks. The VAXstation 520 features the 32-bit MicroVAX II processor and a Tektronix 4125 graphics subsystem. Price is $40,790. **Digital Equipment Corp.**, Maynard, MA **Circle 131**

VMEbus Development System

Combined with a terminal, the Plessey PME DS/68-1 VMEbus development system includes a CPU, memory board, intelligent interface, two backplanes and hard and floppy drives in a self-contained internally powered and cooled chassis. The CPU board includes an 8 MHz 68000 microprocessor, 128-Kbyte DRAM, 16-Kbyte EPROM with monitor, 16-Kbyte user EPROM space, 3 RS-232-C SIO channels, a PIO channel, a programmable timer and a real-time clock with battery back-up. **Plessey Microsystems**, Pearl River, NY
Circle 126

Computer-Video Editing System

The Image Master is a computer-video editing system which allows tape shuttling and automatic assembly, multiple-image recording, overlays, complete list management and storage and security. The Image Master includes an audio-follow-video switcher and character generator. The system also includes a SMPTE time code generator and reader for both vertical interval and longitudinal time code. **Comvid**, Anaheim, CA
Circle 134

Family Of Minicomputers With 5-Year Warranty

Parallel Computers' 300 XR family, which replaces the company's previous 300 system family, comprises the Model 30 and the Model 40. Each system is based on redundant, self-checking architecture. All key components, including CPU, memory, disk subsystems and power supplies are duplicated. If a component fails, its twin maintains operation to ensure continuous application integrity. The Parallel 300 XR family provides complete data protection through duplication on separate disk subsystems, automatic recovery from media failure and end-to-end verification. The computer is

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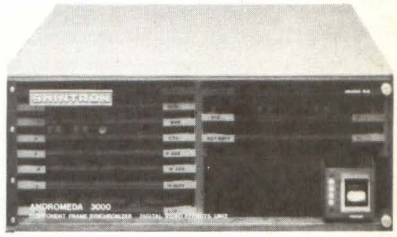

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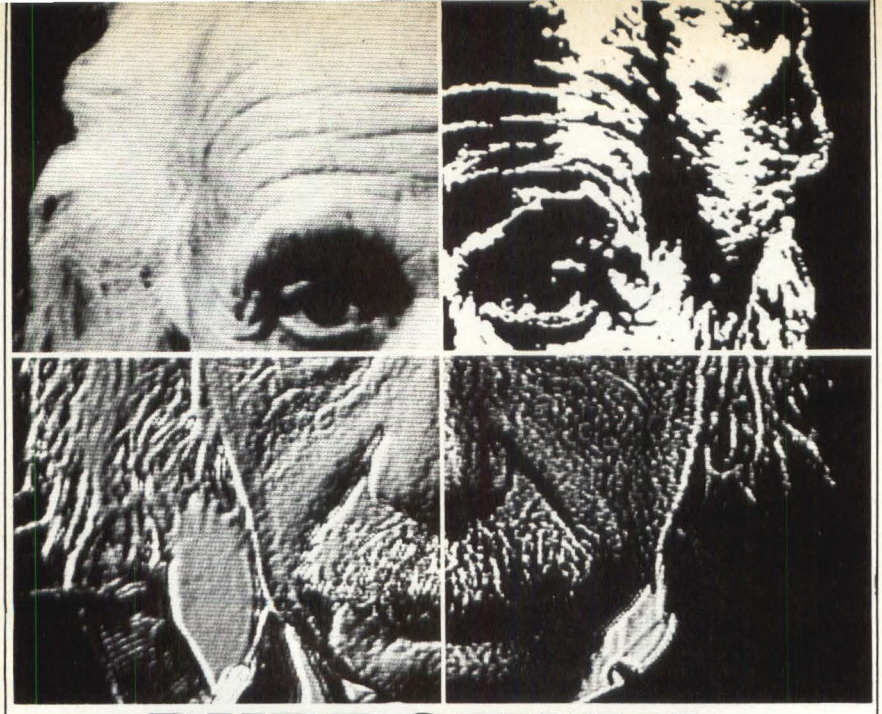

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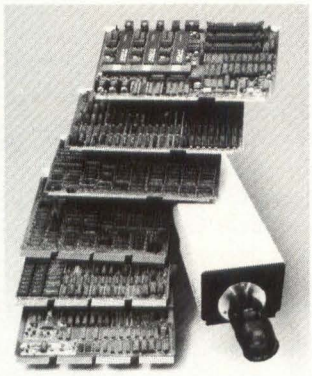

The modules also contain programmable Transformation Tables and provide for B&W and RGB output. Full-color processing is also supported.

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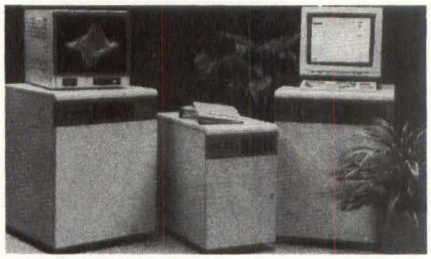
Circle 35

isolated from external power problems by integrated uninterruptible power systems. Model 30 is priced at $59,900, Model 40 at $74,900. **Parallel Computers**, Santa Cruz, CA **Circle 129**

High-Performance Technical Workstations

HP has expanded its HP 9000 technical computer family with the addition of a series of medium to high-performance workstations. Designated the Series 300, the workstations' feature a choice of CPUs, displays, systems software, programming languages and peripherals. Two different CPUs are offered with the Series 300. For use in an entry-level to mid-range system configuration, a 10 MHz Motorola 68010 is available, while a 32-bit, 16.6 MHz 68020 is available for performing high-speed processing. With both CPU configurations, 1 Mbyte of RAM is standard, but expandable to up to 7.5 Mbytes. Integrated programming languages/operating systems available with the Series 300 include Basic 4.0, Pascal 3.1 and HP-UX. Prices for the Series 300 range from $3,500 to $55,000. **Hewlett-Packard**, Palo Alto, CA **Circle 127**

RISC-Based Computer Systems



Four computers designed for computationally intensive tasks, the 32/110, 32/130, 32/310 and 32/330, differ from each other in size, number of users and peripherals supported and amount of real memory. The 32/130 and 32/330 each delivers greater computing power than its series counterpart. Both the 100 and 300 series support the UNIX operating system and SPICE, NASTRAN and ANSYS. Each Ridge compute station supports color or monochromatic displays and standard Ethernet protocols. The 100 series stations are more compact than Ridge's 300 series and are less expandable. Each product can be networked via Ethernet technology to personal computers, superminicomputers and mainframes. Prices range from $39,000 to $69,000. **Ridge Computers**, Santa Clara, CA **Circle 133**

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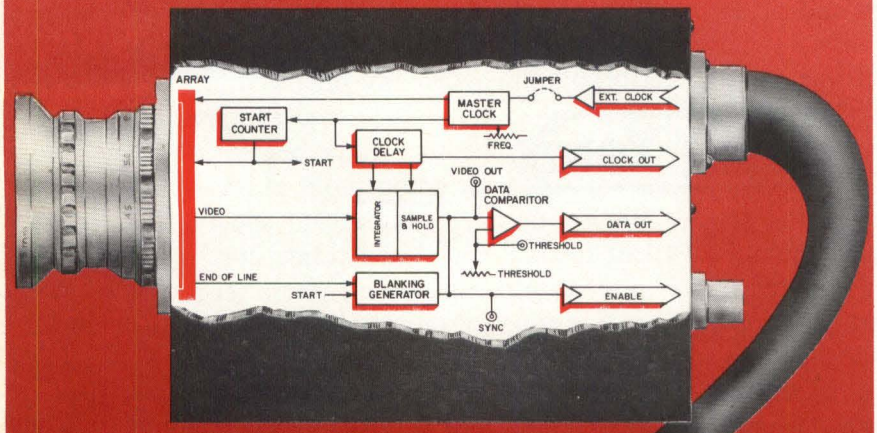

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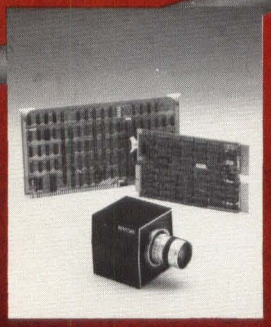

Using a Reticon interface board, the LC310 camera can plug into a Multibus™ or Q-Bus™.

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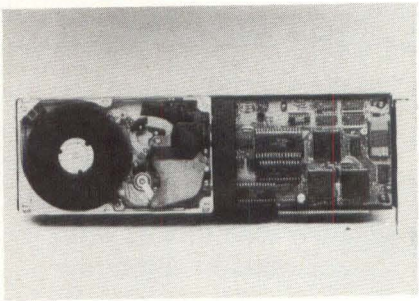
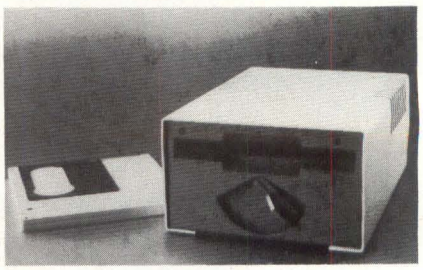
Hard Disk On An Add-In Card



Hardcard, a hard disk on an IBM PC plug-in board, comprises a 10-Mbyte disk drive with electronics, controller and file management and installation software on a plug-in card with dimensions of only 4″ × 13″ × 1″. It can be installed directly into an IBM PC expansion slot. Price is $1,095. **Plus Development Corp.**, Milpitas, CA **Circle 135**

Optical Disk Drive



The optical disk drive 5984 is a 5¼″, WORM (write-once-read-mostly) storage system. Its double-sided 400-Mbyte removable cartridge offers a capacity of over 200 Mbytes of user space per disk side. It features pregrooved media for faster access. With the 5984, optical ROM disks can be read by it. **Optotech**, Colorado Springs, CO **Circle 138**

160-Mbyte Disk Drive

With an average on-line access time of 18 msec under normal demand conditions, the atlas 160-Mbyte disk drive incorporates 50 read/write heads on 3 platters which can be stepped to a total of 160 cylinders or 8000 individual tracks. Each cylinder provides the computer with msec access to a full Mbyte of data. A head lifter mechanism eliminates contact start/stop of the 50 heads. The head configuration reduces the amount of arm movement and maintains acceptable response times under high demand. **Alpha Data Inc.**, Chatsworth, CA **Circle 139**

24″-Wide Electrostatic Color Plotter

Versatec's second-generation color plotter plots at up to 1″/sec with a resolution of 200 points/in on paper or film. It can plot a D-size drawing in full color in 5.5 minutes, a monochrome plot in less than 1 minute. The Versatec plotter can produce a D-size drawing on paper for a total cost of about $0.90, on film for $4.00. **Versatec**, Santa Clara, CA **Circle 137**

Vector CRT Film Recorder

This vector film recorder provides 16,000 points per frame and infinite resolution between points. The recorder needs no vector-to-raster converter to accept the vector data. Two built-in standard interfaces, RS-232-C and HP-IB, are used in the unit. Camera operation, including film advance, is completely automatic. The unit can be networked to allow remote shared operation to greatly reduce the cost of operation to individual users. Price is $13,900. **Hewlett-Packard**, Palo Alto, CA **Circle 136**

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systems at full speed. In addition to the 4-Kbyte EPROM 8751H, a proprietary 12 MHz 8-Kbyte EPROM version, the Am9761AH is also available. The Am9761AH is a production and prototyping device for those applications requiring more than 4 Kbytes of on-chip memory. Priced from $63.00 to $73.70. **Advanced Micro Devices**, Sunnyvale, CA **Circle 144**

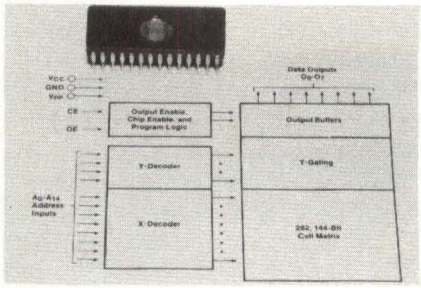
Signal Conditioning Modules

Three signal conditioning modules for 3B Series Signal Conditioning Subsystem are available. The 3B45 and 3B46 are isolated frequency input modules; the 3B47 is a linearized thermocouple input module. The frequency input modules provide signal conditioning for tachometers, flow meters or any other transducer with a frequency-based output signal. The linearized thermocouple module isolates, amplifies and linearizes low-level thermocouple signals for computer-based temperature measurement. 3B45/45 and 3B47 priced at $225 and $250 respectively. **Analog Devices**, Norwood, MA **Circle 147**

Dual-Port Video RAM

The MB81461 video RAM from Fujitsu is a 64K × 4 device which features random access and serial access ports to simplify frame buffer designs. Organized as a 64K × 4 RAM and a 256 × 4 serial port, the RAM provides internal bidirectional data transfer between the two ports as well as I/O via the serial access memory port. Priced from $25.00 to $28.00. **Fujitsu**, Santa Clara, CA **Circle 152**

Fast 256K CMOS EPROM



Implemented in CMOS, the μPD27C256 is an EPROM offering 150 nsec access times and a 32K × 8 implementation. NEC is also offering an NMOS version of the part with a 32 K × 8 implementation. Production quantities of both devices are available in 28-pin cerDIPS. Extended temperature versions and a surface mount package (32-pin leadless chip carrier) will be offered late this year. Priced from $15.15 to $20.65. **NEC Electronics**, Mountain View, CA **Circle 151**

Two 300-Baud Modem ICs

Called the SCI1002 and SCI1003, two standard modem ICs feature full-duplex answer and originate operation. Each device contains all the circuitry needed to handle the signal processing tasks of a Bell 103-compatible modem. A transmitter squelch function simplifies handshaking and switching between voice and data modes. Analog loopback capability is also included for full testing the signal path. Priced from $25.50 to $28.00. **Sierra Scientific**, Sunnyvale, CA **Circle 145**

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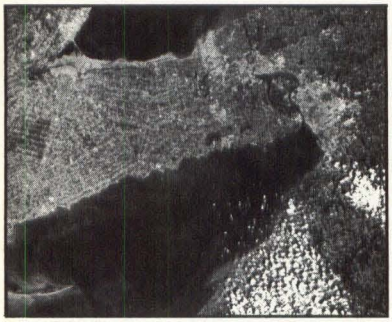
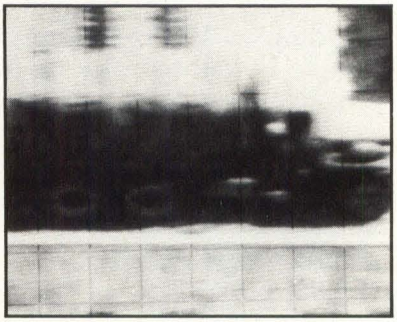
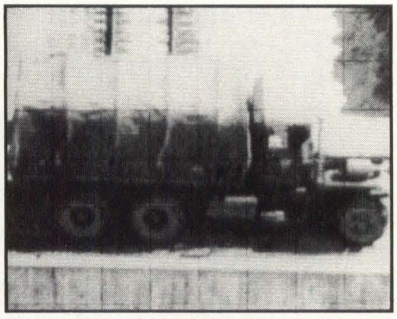


LANDSAT image of Niagara Peninsula



X-Ray security screening



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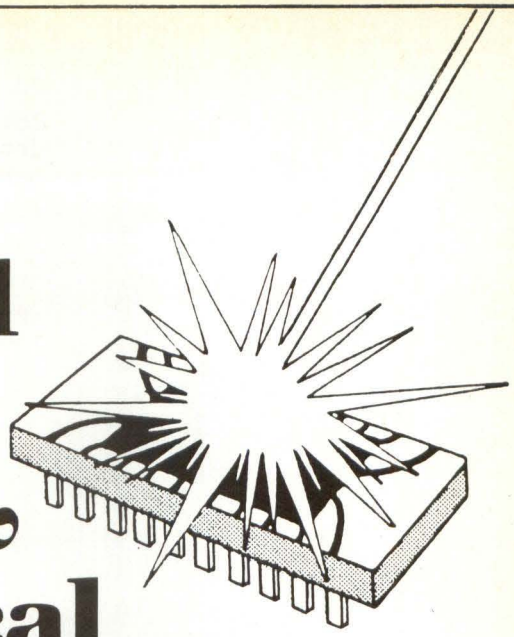
Experimental Physicists Electronics & Electro-Optical Engineers



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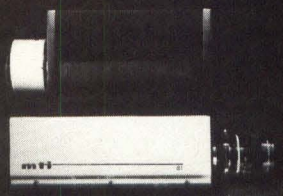

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NEW PRODUCTS

256K DRAMs With Error Correction Coding

Two 256K dynamic RAMs – the 256K × 1 DRAM, MT1256, and the 64K × 4 DRAM, MT4064 – feature on-chip error correction coding (ECC). Both products feature real-time on-chip ECC that results in reduced soft and hard error FIT rates. In addition to the usual 256K (262,144) bits available to the user, these 256K memories contain 128K (131,072) additional bits used for real-time on-chip ECC. ECC utilizes a technique based on the (12,8) Hamming Code that detects and corrects all single-bit errors. Priced from $6.50 to $12.25. **Micron Technology**, Boise, ID **Circle 146**

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- on-board disk storage
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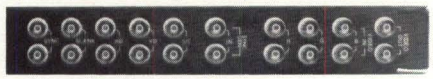

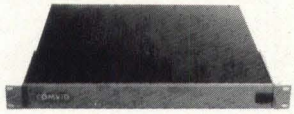

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Circle 49

BOARDS

Caching Disk Controller

Multibus-compatible, with a 2.5 Mbyte/sec transfer rate, this caching disk controller, the Rimfire 1200, supports SMD drives. Its caching architecture is suited to UNIX-based systems. It is possible to segment the cache (up to 32 Kbytes) into 52 byte minimum segments. The Rimfire 1200 can also perform disk handling, overlapped seeks, zero latency track read, sector skewing and sector slipping. Price is $2,195. **Ciprico**, Plymouth, MN

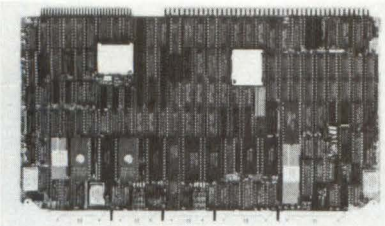
Circle 163

2-Mbyte Multibus RAM Board

Operating all iLBx high-speed memory specifications, the DSB-020EL Multibus RAM board features on-board error correction. Designed to operate with all iLBx-compatible Multibus CPU boards, the RAM board offers integrators of iLBx-compatible CPU boards 1 Mbyte or 2 Mbytes of DRAM on a single card. The board consists of either 44 or 88 150 nsec DRAMs, an LSI RAM controller, an LSI EDC unit and the dual Multibus and iLBx interface. Priced from $1,084 to $1,796. **Pascot Inc.**, Irvine, CA

Circle 149

80186-Based SBCs For Multibus



With Ethernet, hard disk, floppy disk and RS-232 capabilities, these two 80186-based SBCs for Multibus feature 512-Kbyte RAM with parity. The CP-2000 communications processor combines the functionality of a 186 CPU card, a 512-Kbyte memory card, an Ethernet controller card and an Octal RS-232/423 card. The FP-2000 file processor is functionally equivalent to a 186 CPU card, 512-Kbyte memory card, a disk controller card and a quad serial RS-232/423 card. The CP-2000 follows the IEEE 802.3 specification at a data rate of 10 Mbits/sec. The FP-2000 disk interface provides for dual 5¼" Winchesters. Both are priced at $2,995. **Matrox**, Dorval, Quebec

Circle 157

VMEbus Disk/Tape Controllers

The 751 VMEbus SMD disk controller and the 772 VMEbus ½" tape controller are designed on single standard VME size boards. Both support VME 32-bit address and data support. The 751 supports SMD interface disk drive up to 2.4 Mbytes/sec HSMD devices. The 772 will handle formatted ½" tape interfaces and support tape ranging start/stop models at 12.5 ips to GCR streaming models up to 200 ips. In addition, the 751 features a programmable throttle that controls the length of time the 751 remains on the VMEbus. Price for the 751 starts at $2,700. The 772 is priced from $1,300 to $2,000. **Xylogics**, Portsmouth, NH

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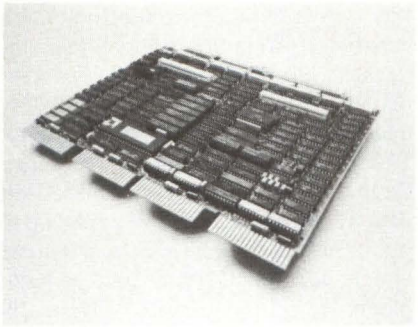
DEC Controllers With 2.5 Mbyte Disk Transfer Rates



Enhanced to handle 2.5 Mbyte/sec disk transfer rates, these two multifunction controllers are designed for Q-Bus and Unibus-based minicomputers. The Spectra-25-Plus and Spectra-121-Plus controllers each support SMD interface disks and ½" tape (1 Mbyte/sec) drives simultaneously. They emulate DEC's RM02/5, RM80 disk and TS11 tape drives. The Spectra-121-Plus also emulates DEC's RP04, RP05, RP06, RP07 disk drives. The quad-wide 25-Plus enables DEC's Q-Bus-based systems to support two physical and eight logical disk drives and four tape drives. Prices are $3,200 (Spectra-25-Plus) and $5,000 (Spectra-121-Plus). **Spectra Logic,** Mountain View, CA

Circle 160

15 MHz Unibus SMD Controllers

With data transfer rates up to 1.8 Mbytes/sec, these two enhanced SMD disk controllers are designed for PDP-11 Unibus and VAX systems. The MDB-DK11-RM/-RP controllers will operate disk drives with an SMD interface that can operate at the standard rate of 1.2 Mbytes/sec as well as the 1.8 Mbyte rate of the Fujitsu Eagle. On a two-drive system, two logical units per drive can be supported for a maximum of four logical units. An onboard disk address translator (DAT) provides attachment of different configuration SMD disk drives to the controller, without requiring modification of system software drivers or the main controller firmware. Price for each is $3,900. **MDB Systems,** Orange, CA **Circle 156**

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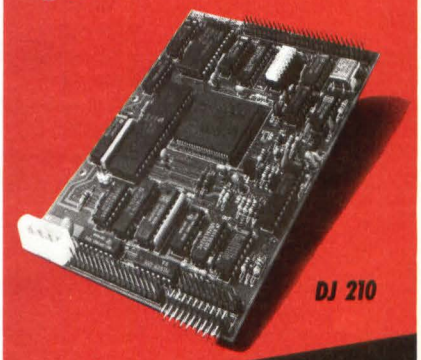

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VME PROM Board

Featuring multilayer construction, this VME EPROM/RAM/EEPROM board has two independent sections each capable of accepting up to 8 memory devices. It can be configured to address between 16K and 1M of EPROM, 16K and 12K of RAM or 16K and 128K of EEPROM, or a combination of the three. Supporting 32-bit addressing and 32-bit data transfers, the board can respond to one or several different address modifiers simultaneously. **Central Data**, Champaign, IL **Circle 159**

Video Disk Graphics/Text Overlay Board

Designed to overlay color graphics images and alphanumeric text onto a NTSC color video signal, this color graphics controller, the OVR-640, contains a separate graphics memory of 640 × 400 × 2 pixels for high resolution with 4 simultaneous colors and text memory for a single page of 25 × 80 characters. The graphics memory can also be configured as 320 × 400 × 4 pixels for mod-

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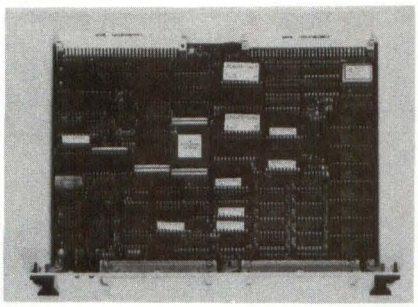
erate resolution with up to 16 simultaneous colors. An on-board ROM-based look-up table selects these 16 colors from a palette of 128 shades. The text memory can also be configured for two pages of 25 × 40 characters. Price is $1,495. **Matrox**, Dorval, Quebec **Circle 158**

Serial Communications For VMEbus



An asynchronous serial communication board, the XVME-428 features eight independently software configurable serial ports that are compatible with RS-232-C, RS-422-A or TTL lines. The board also features on-board intelligence provided by 10 MHz 68000 CPU and firmware, programmable baud rates ranging from 50 to 19.2K baud and the ability to automatically execute XON/XOFF and modem control handshaking tasks. Price is $2,200.00. **Xycom**, Saline, MI **Circle 150**

Controller For 8 To 20 ppm Nonimpact Printers

Designed for 8 to 20 ppm nonimpact printers, this raster image processor is a member of the firm's Pixxon 300 Controller Family. The Pixxon 300/SBC provides text, business graphics and text/graphics merge capabilities. Full vectored graphics via a 1 Mbyte bit map are available as an option. The controller can be interfaced with the Xerox 2700, Canon CX, Ricoh 4080/4121 and General Optronics Holoscan 28, as well as nonimpact printers. Other features include 384 Kbytes of RAM and Centronics-like parallel port. Price is $500. **Electronic Machine**, Los Angeles, CA **Circle 161**

Magnetic Bubble Memory Board For VMEbus

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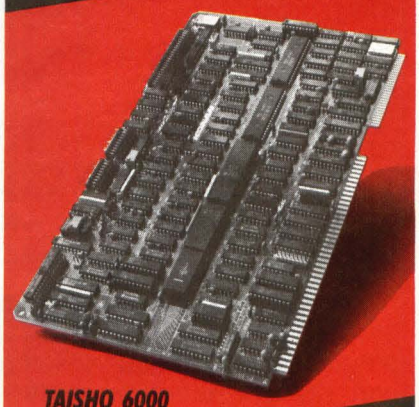

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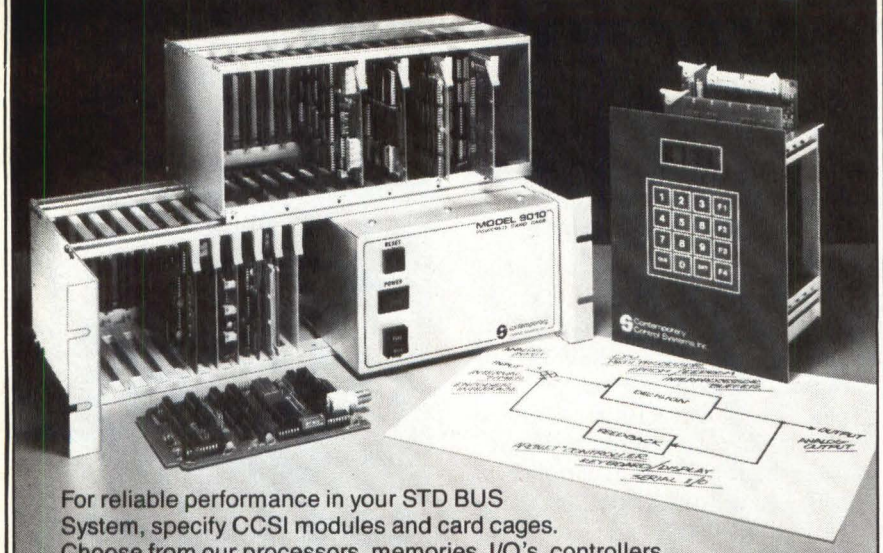

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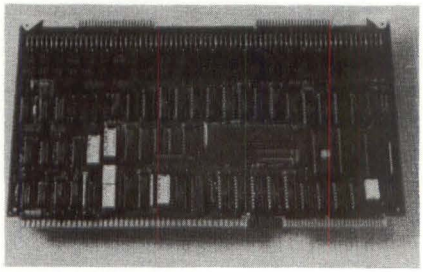
NEW PRODUCTS

ola, this bubble memory board was accomplished using Motorola's MBM-2011 bubble memory chips and an on-board 68B09 CPU for the intelligent interface. The Xycom board is designated the XVME-160: the Motorola is the MVME-250. The module can provide up to ½ Mbyte of nonvolatile storage and is designed to operate in the 0°C to +65°C operating range, and the -40°C to +80°C storage range. A P2 connector provides future expansion capabilities. **Xycom**, Saline, MI **Circle 154**
Motorola, Tempe, AZ **Circle 155**

Compatible Sequence-Of-Events Boards



The MP840 is a 24-channel, Multibus-compatible, sequence-of-events board. It

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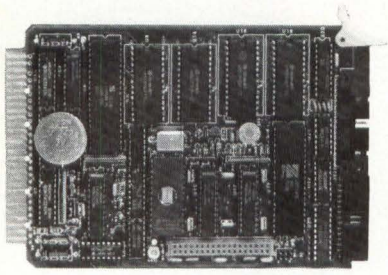

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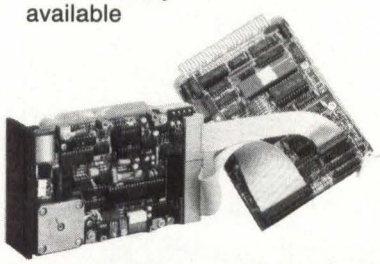

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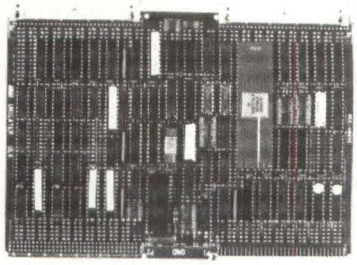
Circle 59

VMEbus 7/9 TRACK TAPE INTERFACE



- Drives 2 mag tape formatters.
- Formatters can control 8 drives.
- Tape drives may be 7 or 9 track.
- Operates as VMEbus slave or master.
- 4K FIFO buffer and DMA controller.
- Vectored interrupt capability.
- Programmable jumper selection.
- On-the-fly or step mode operation.

Integrated Scientific Systems, Ltd.
P.O. Box 3, Portsmouth, RI 02871
401/847-4388

$1695

Circle 63

reads the static state of an input, or monitors the state of a descrete input, and records any change in the state of that input. Data is time-stamped with 1 msec resolution and stored, along with the polarity of the input, for later access by the system's CPU. Data can represent the change of any 1 input or the simultaneous change of all 24 inputs. **Burr-Brown**, Tucson, AZ **Circle 148**

SOFTWARE

PCB Layout System

Recal-Redac has introduced Visula, a fourth-generation printed circuit board design system for high-density boards using CMOS, TTL and discrete components. The software runs on Apollo's (Chelmsford, MA) 32-bit computers and includes Logic Capture for schematic entry, a Memory Router for routing PC board memory areas and an Advanced Router which is a re-entrant, orthogonal fine-line router capable of routing boards up to 50 layers thick. The PCB Design Software handles the latest technologies, including surface-mounted devices, pin grid arrays, buried vias and fine-line routing. Other features of Visula include a relational database and on-line electrical rule checking. Currently available, Visula sells for $120,000. **Recal-Redac,** Westford, MA **Circle 167**

Physical Modeling System For Simulator

HICHIP adds physical modeling capabilities to the funtional model language provided with the HILO logic simulation software package. With HICHIP, inclusion of a VLSI component into a model library requires physically connecting the device to a personality board and describing the external pin connections and their associated delay parameters. Using HICHIP also eliminates the chance for introducing software modeling errors into the design verification process by using the functionality of the actual part during simulation. This guarantees accuracy of simulation results much earlier in the design cycle. Price is $36,000. **GenRad**, Santa Clara, CA **Circle 142**

CAE Design Simulation

The QUICKSIM family is a software application package for logic and fault simulation, as well as worst-case timing analysis. It consists of QuickSim logic simulation, QuickFault interactive fault simulation and QuickTime timing analysis. QuickSim provides true interactivity of stimulus and probes, and 12-state simulation for MOS verification. Simulation support includes 95 classes of primitives models, QuickParts, the Mentor Graphics Hardware Modeling Library and Behavioral Language Models. QuickFault's concurrent algorithm provides fault analysis and a graphical display of cumulative fault detection, undetected faults and fault blockages. QuickTime provides worst-case timing, minimum and maximum timing, and timing using the same stimulus and display format as all QUICKSIM family functions. Priced from $14,500 to $16,500. **Mentor Graphics**, Beaverton, OR **Circle 143**

Expert System Software

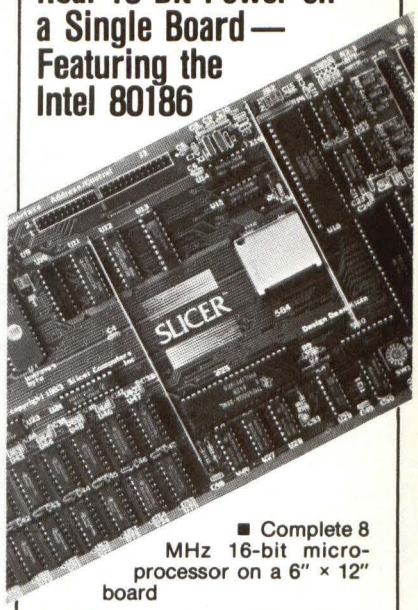
Written in assembly language, the Knowledge Delivery System (KDS) automatically produces up to 16,000 rules per knowledge module, up to 4096 cases and conclusions per knowledge module and up to 12 conditions per case. A developer can make a complete expert system using English in fully interactive process; no symbolic programming or batch preparation is required. The user can select either forward or reverse-chaining, and 128,000 characters are available for optional help screens which can be prepared with a built-in word processor. Price for the development system only is $795. **KDS,** Wilmette, IL **Circle 166**

Comten X.25 Interface With NPSI Capabilities

A network connectivity software product, the Comten X.2 Interface to Packet-Switched Data Networks has features equivalent to IBM's NCP Packet Switching Interface (NPSI) Releases 3.1 and 4.0. It resides in an NCR Comten communications processor and includes an optional module that gives SNA network planners an IBM-type host-dependent implementation of X.25 access. Comten X.25 still offers the packet adapters or packet assemblers/dissamblers (PADs), which control host and terminal connections and link users' SNA and pre-SNA terminals to SNA or emulation hosts via X.25 networks. License fee for Comten X.25 depends on modules selected. **NCR,** St. Paul, MN **Circle 165**

THE SLICER

Real 16 Bit Power on a Single Board— Featuring the Intel 80186



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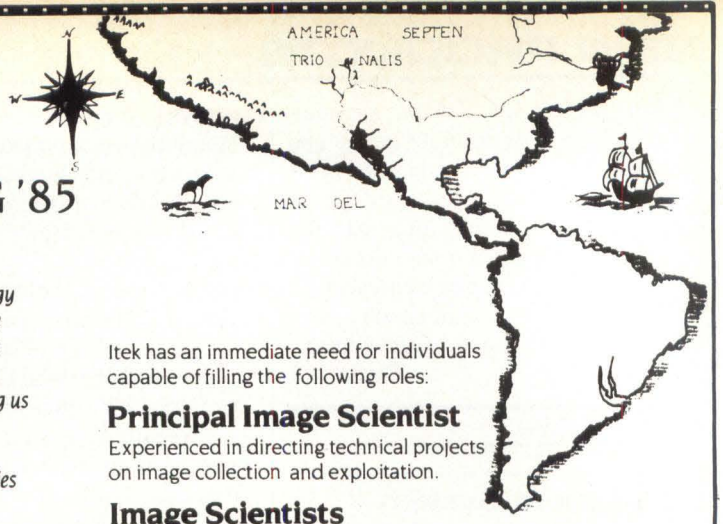

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