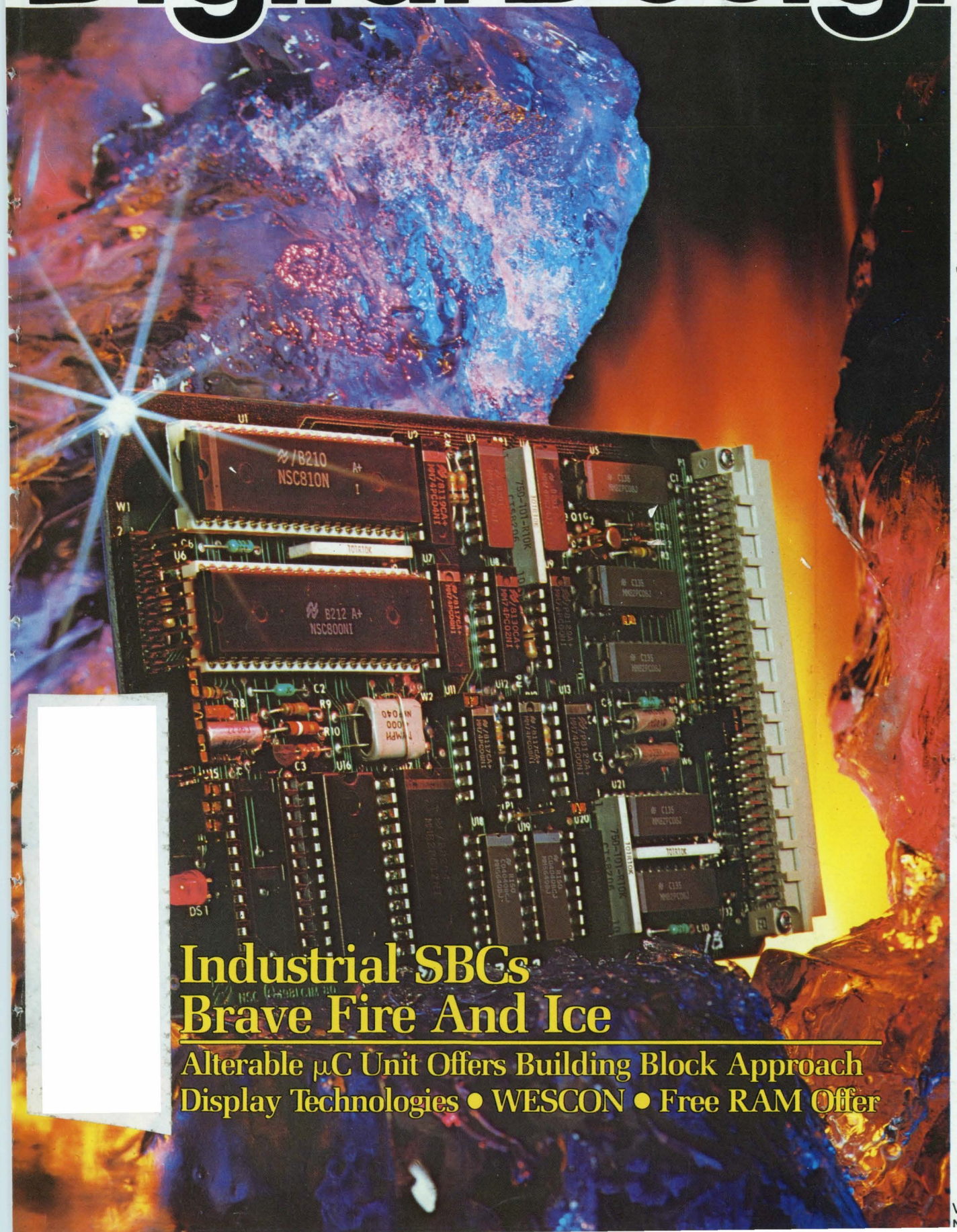
A MORGAN-GRAMPIAN PUBLICATION

Digital Design



Industrial SBCs Brave Fire And Ice

Alterable μC Unit Offers Building Block Approach

Display Technologies • WESCON • Free RAM Offer

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 8/82

VOL. 12
NO. 8

TS-1™ The Most Advanced Business Terminal And Designed To Stay That Way...

The TS-1™ is truly designed with the future in mind, taking full advantage of the microprocessor technology. The TS-1 terminal emphasizes software driven features which provide a wide and unique range of user flexibility, as well as significantly reducing the possibility of obsolescence. All new emulations as offered by *Falco Data Products* as well as options, such as auto-dial 212 plus™ modem 300/1200 bps...full Plot 10 graphics...and the new and powerful *SMART PAGING*,™ can easily be incorporated into the standard TS-1; thereby configuring the TS-1 to exactly what you need when you need it. Never has one terminal had so much to offer to a wide variety of users. But see for yourself just how much more advanced the TS-1 really is.

Some standard TS-1 features are:

• Software-driven emulations • 28 non-volatile user-programmable functions • User selectable personality features • User definable split screen scrolling • User selectable status line • Lightweight w/small footprint • 8 attributes not stored on screen

*Optional

Falco
DATA PRODUCTS

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Sunnyvale, CA 94086
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(408) 745-7123

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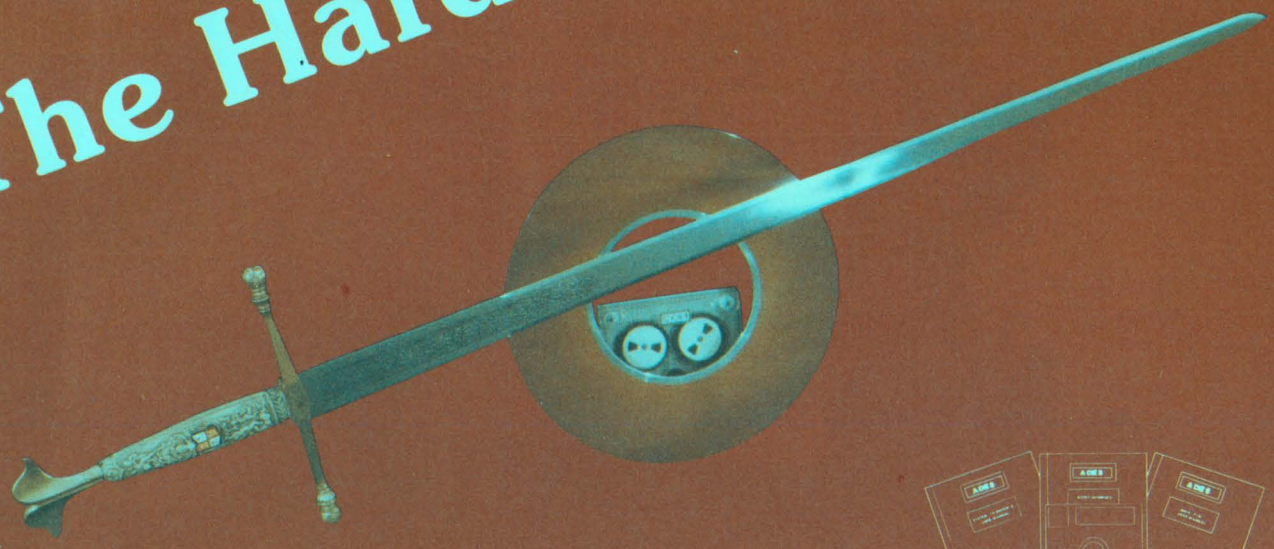
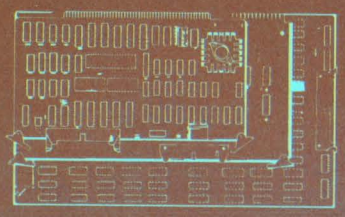
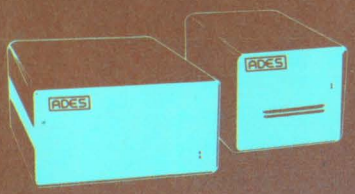
The Hard Edge in performance







SYSTEMS
Whether you are a systems integrator or computer OEM, *ADES* subsystems provide the ultimate solution to your needs. As a fully supported product, *ADES* subsystems provide a revolutionary product capable of displacing cartridge disk drives and floppies.

SYSTEM 8
As a standalone table top or rackmount package, the *GYPSY* based SYSTEM 8 provides the user a disk of 10 MB, 34 MB, or 70 MB of disk capacity with 10 MB or 20 MB removability via the streaming tape.

SYSTEM 14
The *SYSTEM 14* provides 33 MB or 66 MB of disk storage with 20 MB removability via the streaming tape, disk tape packaging.

THE ULTIMATE SOLUTION
With all the performance of the *ADES GYPSY* controller, the *SYSTEM 8* or *SYSTEM 14* can meet your total memory subsystem requirements.

GYPSY
At the heart of the *ADES* product line is the *GYPSY* Winchester/Streaming Tape formatter. By combining the disk and tape functions into a single card, the *GYPSY* provides unprecedented system capabilities.

With a 5 Mbyte/minute offline disk to tape transfer rate, a user can backup or restore a 20 Mbyte logical drive in less than four minutes. When operating in the "Transparent Mode," the host can still access the disk while the *GYPSY* moves data between the disk and streaming tape. In multiuser systems, individual users can backup or restore logical elements without affecting other users on the system.

MORE THAN JUST BACKUP
Compiling the *GYPSY* disk/tape commands with the direct tape access commands provides a system capable of Operating System load, Program Exchange and Selective File storage and retrieval. The streaming tape thus provides more than just backup.

EASY INTEGRATION
The power and flexibility of the *GYPSY* is only surpassed by the ease of host integration. With as few as five 7400-type components, the *GYPSY* can be interfaced to most mini or microcomputers.

EXPANDING HARDWARE SUPPORT
ADES currently supports Priam and Century Data Disks in conjunction with DEI, Archive and Cipher ¼" cartridge streaming tapes.

SUPPORT
ADES supports the most widely used micro-computers, and their operating systems.

GYPSY HOST INTERFACE ADAPTERS (GHIAs)
For the user who desires to bring up his system quickly, *ADES* offers S100 and Multibus host adapters in both Programmed 1/0 and DMA configurations. In conjunction with *ADES* software, the *GHIAs* provide a rapid means of integration, with minimal effort.

THE Z80 CONNECTION
For the Z80-based systems, *ADES* provides the GHIA-Z80 which allows connection of *GYPSY, SYSTEM 8* or *SYSTEM 14* directly to the CPU, thus eliminating the problems of specialized base configurations.

SOFTWARE
ADES support of CP/M™ and MP/M™ makes the *GYPSY* and SYSTEMS 8 and 14 easy to integrate and use. Support levels range from the "non-programmer" and user to the systems integrator configuring high performance MP/M™ systems.

CP/M
The *ADES "BIOS ATTACH"* program allows a user to configure the program to his system configuration, and begin using the disk/tape subsystem as an integral system resource under CP/M 2.2.

MP/M
For the system integrator who must design a complete BIOS or XIOS, *ADES* supplies a series of detailed application notes. These publications allow quick and complete integration of *ADES* subsystems into all system applications.

UTILITIES
All disk/tape subsystems running with CP/M are also supported with an array of utility programs. Format and Verify, Defect Compensation and Backup and Restore are only a few examples.

ADES

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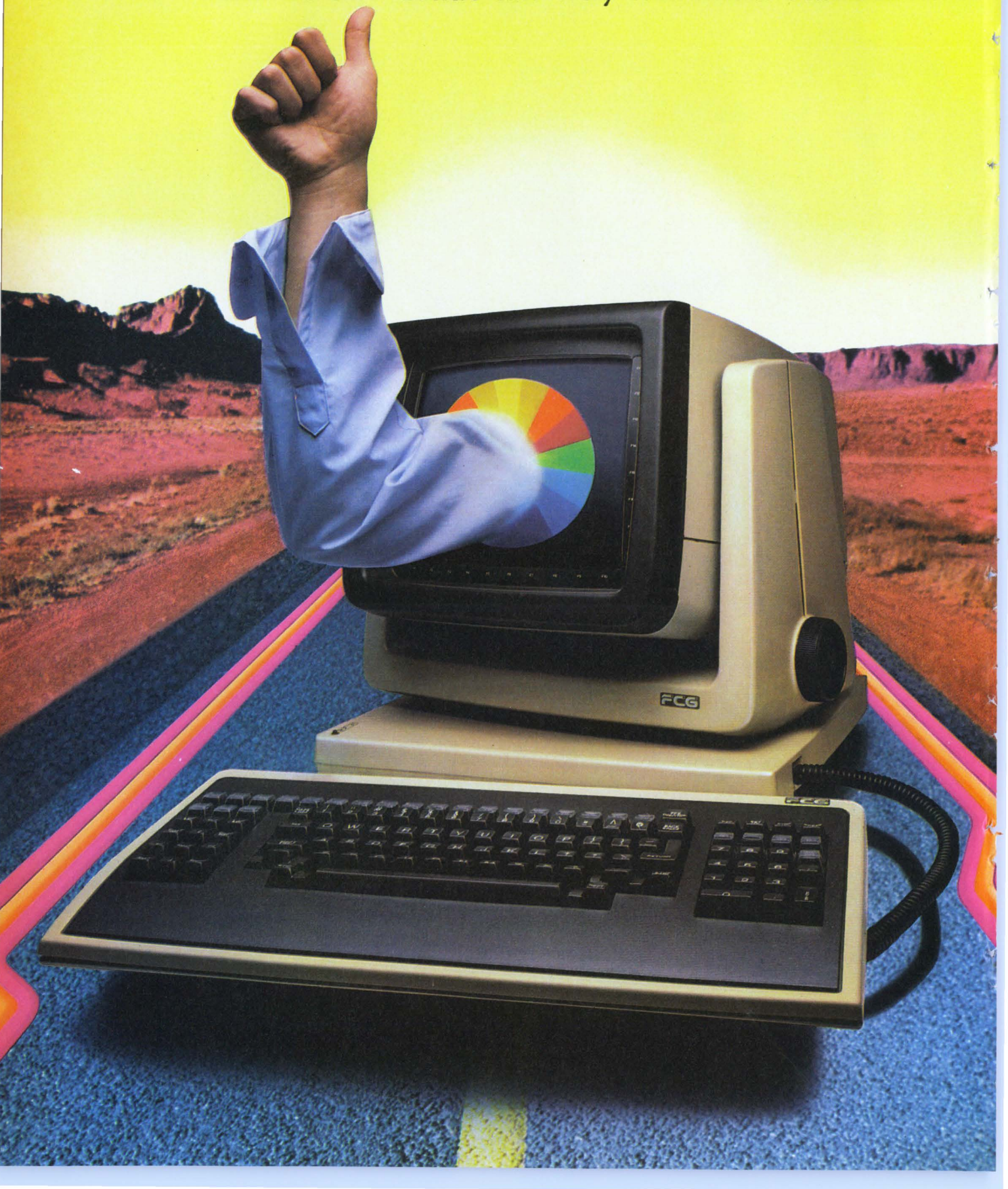
BREAKTHROUGH IN

BEACON™ leads the way with new standards in



COLOR GRAPHICS.

price-performance and human-factors engineering.

Finally, a medium-priced color graphics system with the performance of much more expensive systems.

Introducing Beacon™ from Florida Computer Graphics.

Enhanced productivity for business and engineering.

The Beacon™ System displays a full spectrum of graphics capabilities. Not only multi-color graphs and charts, but engineering diagrams, as well.

As a stand-alone or host-dependent system, Beacon does it all. For enhanced productivity in engineering, marketing, manufacturing, and financial control.

More power where it's needed.

The Beacon System can accommodate up to almost 1 MByte of main processing memory. With the addition of 640 KB of graphics memory, Beacon can create a 1280 x 960 image resolution used in many CAD/CAM applications. This high resolution, combined with standard zoom and roam features on a 13″ or 19″ display, make Beacon ideal for engineering applications. Beacon's own menu driven software and CP/M compatible operating system provide access to a comprehensive library of programs that cover virtually every aspect of business.

Superior graphics features.

The extent and caliber of Beacon's graphics features is unmatched in its price range.

The System's brighter, more vivid colors stem from a unique electronic design and a superior raster scan display. The BeaconBRIGHT™ image, combined with an anti-glare filter eliminates the need for hooding the display—even in brightly lit areas.

Circles, vectors, arcs, rectangles and polygon fills are generated with hardware rather than software. As a result, image response is almost instantaneous.

Beacon's 16x zoom feature can be controlled from the keyboard in 1x increments. Both horizontal and vertical scrolling is variable in speed and exceptionally smooth. Beacon also provides reverse video and underline, as well as blinking and variable height characters.

Other graphics features include: 640 x 480 resolution (standard); 6 memory planes with 256 colors—up to 32 usable at a time (16 in the graphics plane and 16 in the alpha numeric plane)—and 18 programmable function keys on the keyboard and another 18 on the display bezel.

Human-factors engineering.

The human factors, or ergonomics, that make a computer personally comfortable played an integral part in the Beacon System's design.

The critical area of reducing eye strain and fatigue has been accommodated through the development of a screen image *twice as steady* as the image in other computer systems, including those that are advertised as "flicker free." For extra visual comfort, the brightness of the Beacon image is controllable at the keyboard, and an anti-glare filter reduces distracting reflections.

And Beacon's commitment to superior ergonomic design doesn't stop there. To avoid back strain, the monitor tilts, swivels, and uniquely adjusts 5.5″ in height. In addition, the keyboard is separate from the display and can, therefore, eliminate the sense of being tied down to the monitor.

Other hands-on features that make for greater comfort and productivity are: a three-degree adjustable tilt in the keyboard, a palm rest, tactile feedback, sculptured keys, and a dimpled home key in the function and numerical key clusters.

The importance of MPA.

Our MPA, or Multiple Processor Architecture, is unique to the Beacon System. It incorporates six individual microprocessors, each chosen for its efficiency in the performance of specific tasks.

System throughput is optimized with the use of an administrative processor which distributes Beacon's internal workload. A 16-bit bit-slice processor is dedicated solely to graphics tasks and mathematical functions.

MPA is at the heart of Beacon's extraordinary performance.

Quality and service assured.

All equipment is constantly monitored and evaluated from our corporate production facility, utilizing the most sophisticated automated test equipment available today. And our systems are supported by three levels of service, assuring you of minimal downtime.

BEACON™—the beginning.

Beacon is available. NOW. And it's just the beginning of a comprehensive family of systems that will enhance your productivity. Contact us for more information on how the Beacon System can work for you. We'll send you our full color literature. Just write: Marketing Communications Manager, Florida Computer Graphics, 1000 Sand Pond Road, Lake Mary, Florida 32746. Or call (305) 321-3000. In the Continental U.S. outside Florida, dial 1-800-327-3170.

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The most complete line of Interface Products for PDP*-11, LSI-11 and VAX* Computers with features you can't get anywhere else

For DEC users... MDB makes the difference!

You *can* have it all! Along with the benefits of your DEC computer, you can get interface products that significantly extend the capability, flexibility and economy of DEC systems. MDB makes more DEC system boards than any independent manufacturer—some with plain vanilla compatibility; others with plain incredible performance boosting features. For example—

- Line printer controllers for every major line printer, with complete self-testing capability and optional RS-422 "long lines."
- Peripheral device controllers for card readers, X-Y plotters, electrostatic printer/plotters and paper tape readers/punches.
- DZ11 compatible multiplexors for LSI-11 and PDP-11 users; some combine RS-232 and current loop or RS-422 with a single board.
- High speed synchronous serial interfaces; one DUP-11 compatible model has all bit and byte protocols even for LSI plus X.25 capability.
- Inter processor links between Unibus computers or between Unibus and Q-bus.
- System modules including DMA modules with RS-422, general purpose parallel and digital I/O interfaces, an IEEE 488 bus controller and a programmable real time clock.
- PROM memory modules, some with an on-board PROM programmer.
- General purpose interface and bus foundation modules.
- LSI-11 based subsystems and systems with capabilities like TU-58 cartridge storage and memory management.
- LSI-11 system boxes with 22-bit addressing and switching power supplies.
- LSI-11 bus repeater and bus switches to allow sharing of memories and peripherals between processors.

All MDB products are available under GSA contract #GS-00C-02851.

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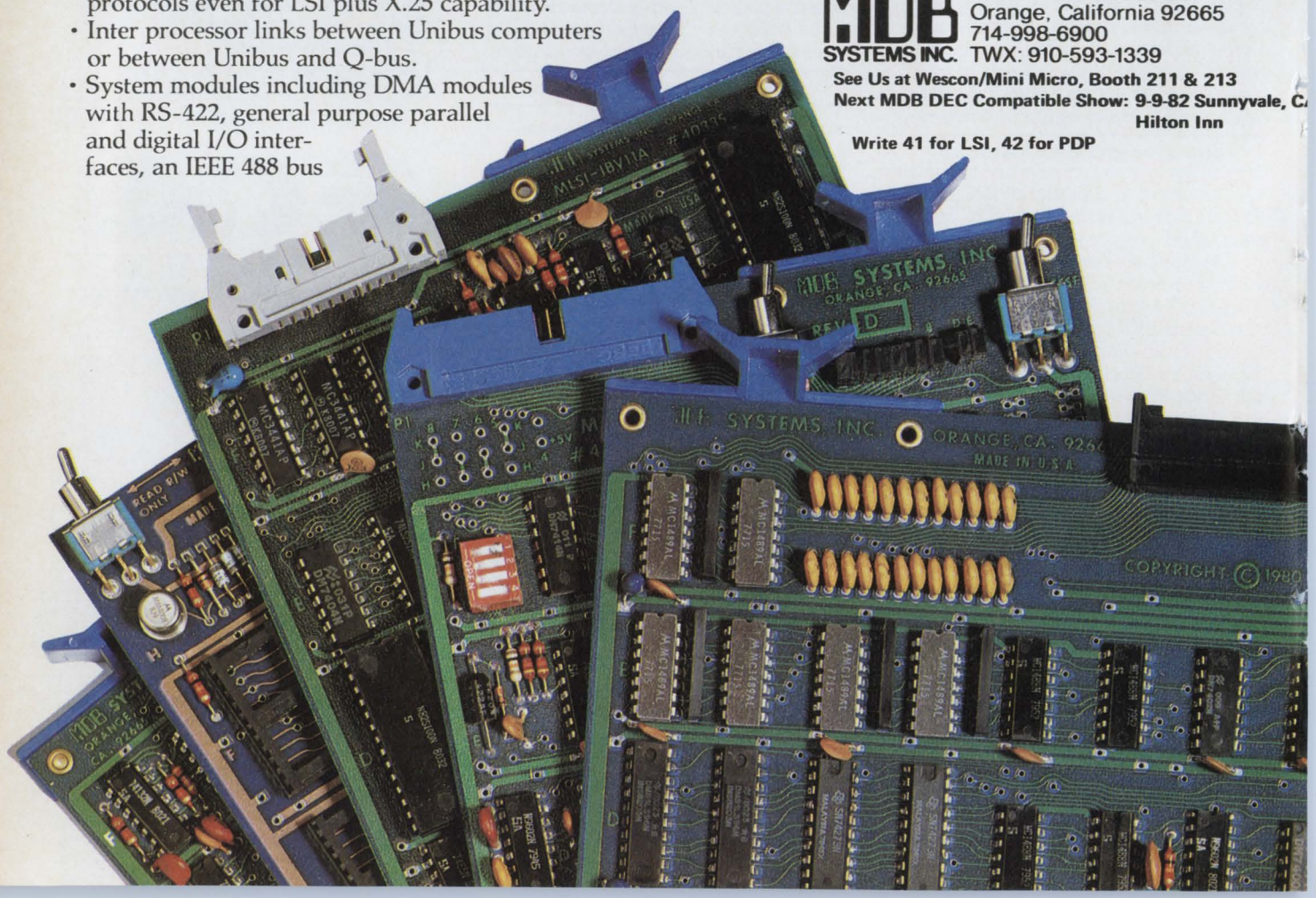

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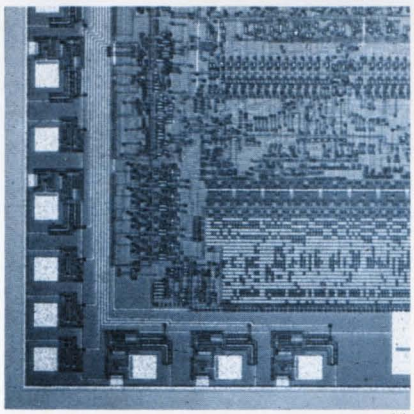

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Cover

Our cover photo illustrates the latest series of industrial μP boards from National Semiconductor. The boards are targeted for harsh environment applications, tolerating a temperature range of −40 to +85 C (see p. 77).

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Buy a Lexidata 8000 and get half a VAX™ free.

Or half a DG MV/6000. Or half a Perkin-Elmer 3230.

Only one graphics processor is designed to free your host of a substantial portion of the processing load imposed by CAD/CAM applications. The System 8000 features dual processor architecture, combining the 16/32 bit Motorola MC68000, the industry's leading microprocessor, with a Lexidata-designed ultra high-speed display processor. The System 8000's unique architecture, graphics software (modeled after the ACM SIGGRAPH CORE), and database structure allow you to distribute the computer's workload to the most appropriate processor: the display controller, the graphics system controller, or the host CPU.

Our software package, LX/GP1, supports a 31-bit precision Object Data Structure™ (ODS) consisting of graphics primitives and functions for defining and changing the bit-map memory. The ODS is a high-level mathematical description of the graphics database maintained in a World Coordinate space. Like a display list, the ODS is kept in vector format; however, the local World Coordinate description allows multiple viewing operations of the database or sections of the database without requiring the host to redefine the objects. In addition, all graphics transformations are performed locally. Therefore, you can redraw the display quickly, without host processing or data retransmission. Unlike conventional display lists, ODS processing is proportional to the number of vectors being viewed, not the length of the display list.

Incorporating System 8000 hardware into your graphics environment ensures a strong processor balance, where no one element is consistently the bottleneck. System 8000 software assures that all elements are equally efficient, leading to high performance and cost effective use of all the hardware in the interactive computer graphics system.

For more details, call (617) 663-8550 or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.

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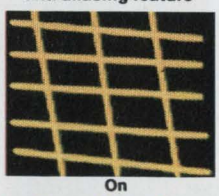
Da Vinci would have traded all his notebooks for this new AED767 graphics terminal.

Today, Leonardo da Vinci's notebooks are priceless objets d'art. They also contain many unique engineering concepts, like the one shown above of the iron framework he designed to reinforce the head and neck moulds for 'Il Cavallo', the horse. Although da Vinci worked periodically on 'Il Cavallo' for 16 years, the gigantic bronze statue, which was to stand some 26 feet tall, never materialized.

AED 767's unique anti-aliasing feature



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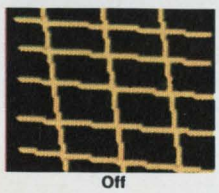

Off

Instead, his patron, the Duke of Milan, used the casting bronze for canons in a war against France.

But what took Leonardo many years to devise could have been achieved in mere hours with the help of AED's new 767 color graphics and imaging terminal. Available in desktop or 3½" high rackmount configuration, this new CAD machine has the kind of innovative features you'd expect only from AED. Features like built-in anti-aliasing (which virtually eliminates jagged lines common to raster-generated vectors). 1K x1K x 8 virtual address space. 768 x 575 pixel viewing window. Up-to-256 simultaneous colors from a palette of 16.8 million. A blue line reference grid that doesn't utilize video memory. Plus a refresh rate, adjustable from tv standard to flicker-free 45 Hz.

The AED767 gives you smoother drawings than any CAD station on the market—and at lower cost. So be a latter-day 'da Vinci' and use the best computer-aided design tool at your disposal. The AED767.

Advanced Electronics Design, Inc., 440 Potrero Avenue, Sunnyvale, CA 94086. Phone 408-733-3555 Telex 357-498. Outside California, Hawaii and Alaska call 800-538-1730.

All images shown taken from screen of AED767.

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Calendar

September 7–10

ICCC '82. Sixth International Conference on Computer Communication. Barbican Center, London, England. Contact: ICCC '82, Box #23, Northwood Hills, HA6 1TT, Middlesex, UK. International Phone: 44 9274 27511.

September 8

Invitational Computer Conference. Boston Mariott Hotel, Boston, MA. Exhibits 2PM–7PM; Technical Seminars start at 9AM. Directed to OEM decision makers, systems houses, and quantity buyers. Contact: Susan Fitzgerald, Conference Mgr., B.J. Johnson & Associates, 3151 Airway Ave., #C2, Costa Mesa, CA 92626.

September 13–15

Autofact-Europe. Exhibition and Conference Center (Palexpo), Geneva, Switzerland. Combined conference and exhibition focusing on the technologies of automated and computer integrated manufacturing. Contact: Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48128. (313) 271-1500.

September 13–16

Sixth International Conference on Software Engineering. Tokyo, Japan. Contact: Sixth Intl. Conference on Software Engineering, PO Box 639, Silver Spring, MD 20901. (301) 589-3386.

September 14–16

Wescon '82. Anaheim Convention Center, Anaheim Marriott Hotel, and the Inn at the Park, Anaheim, CA. Covers: active and passive electromechanical components; computers and peripherals; instrumentation and test equipment; tools and production equipment; control systems; and, power supplies Contact: Eileen Algaze, Communications Coordinator, 999 N. Sepulveda Blvd., El Segundo, CA 90245. (213) 772-2965.

September 14–16

Mini/Micro Computer Conference and Exhibition. Disneyland Hotel, Anaheim, CA. Contact: Eileen Algaze, Electronic Conventions, Inc., 999 N. Sepulveda Blvd., El Segundo, CA 90245. (213) 772-2965 or outside CA, (800) 421-6816.

September 15–17

LAN '82. The Marriott, Los Angeles, CA. Local Area Networks in an exhibition, applications program, and short courses. Covers: distributed data base services, print and file services, work stations, network monitoring and control. Contact: Information Gatekeepers, Inc., 167 Corey Rd., Brookline, MA 02146. (617) 730-2022.

September 20–24

Compcon Fall '82. Capital Hilton Hotel, Washington, DC. Conference on Computer Networking. Contact: Compcon Fall '82, PO Box 639, Silver Spring, MD 20901. (301) 589-3386.

September 21–23

Semicon East '82. Hynes Auditorium, Boston, MA. Contact: SEMI, 625 Ellis St., Suite #212, Mt. View, CA 94043. (415) 974-5111.

September 21–23

SOFTWARE/expo-National. Expocenter, Chicago, IL. Sponsored by Infosystems Magazine. Contact: SOFTWARE/expo, Suite 400, 222 W. Adams St., Chicago, IL 60606. (312) 263-3131.

September 21–23

Voice Data Entry Systems Applications '82. Villa Hotel, San Mateo, CA. Contact: Robert Burgess, Public Information Office, Lockheed Missiles & Space Company, Inc., Sunnyvale, CA 94086. (408) 742-6688.

September 23–25

Computer Showcase Expo. New York Coliseum, New York. Contact: The Interface Group, Box 927, 160 Speen St., Framingham, MA 01701. (617) 879-4502; outside MA (800) 225-4620.

September 28–30

Federal Computer Conference. Sheraton Washington Hotel, Washington, D.C. Intensive 3-day program of sessions and workshops includes special all-day "backgrounder" seminar on first day. Major ADP equipment/systems Exposition on second and third days. Contact: Federal Education Programs, P.O. Box 368, Wayland, MA 01778. (617) 358-5181.

September 28–October 1

Computer Graphics. San Diego, CA. 4-day course covers: technology fundamentals; raster scan, vector and color techniques; software and hardware availability and selection criteria; and equipment selection and implementation of graphics applications. Contact: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd., PO Box 5339, Santa Monica, CA 90405.

September 29–October 1

1982 International Conference on Circuits and Computers. New York Hilton, N.Y., NY. Focus is on VLSI and large-scale systems. Contact: Circuits and Computers, PO Box 639, Silver Spring, MD 20901. (301) 589-3386.

Smart Graphics™ G-100
We Have Only Just Begun.

The **G-100** Graphics Terminal is only the beginning of a family of Computer/Graphics products from Modgraph. The Modgraph **G-100** is a dual purpose expandable computer terminal. High resolution graphics, 8085 processor, 144K RAM, independent high speed alphanumeric overlay, and a wide range of performance characteristics unmatched in the graphics industry.

We call it **Smart Graphics™.** And with good reason. It gives you powerful graphics, multi-page alphanumerics, and more for under $3,000.

GRAPHICS

As a graphics tool the **G-100** is a smart choice; two full pages of 768 x 585 viewable resolution, circle, rectangle, vectors, pattern draw, and of course Plot-10® compatibility.

ALPHANUMERICS

The independent alphanumeric plane allows alphanumeric overlay without overwriting graphics. Length and number of lines are programmable from 41 to 96 characters per line and from 1 to 46 lines per page. Scrollable page memory, split screen, ANSI X3.64 and VT-100® compatibility. All designed to help you work smarter, not harder.

OTHER FEATURES

- CP/M Capability
- 15" P-39 Green Phosphor Screen
- Optional Disk Drive
- Special Function Keys

To fully appreciate the Modgraph **G-100** you have to see it in action. Drop us a line, or give us a call. We'll arrange for a demonstration and show you how powerful graphics can be yours. With **Smart Graphics™.**

® Plot-10 Trademark Tektronix
® VT-100 Trademark Digital Equip. Corp.

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News Update

NEC 16-bit Personal Computer

NEC Information Systems, Lexington, MA, has developed the Advanced Personal Computer (APC) which utilizes the CP/M-86 operating system and is based on a NEC-manufactured 16-bit 8086-compatible μP.

First Commercial Ada Product

The new Ada Syntax Checker, AdaSynCh, from Intermetrics, Cambridge, MA, is a Pascal program which checks the grammatical form of an Ada source program. AdaSynCh determines whether a program is written with proper Ada grammar and format, but also indicates where errors exist.

NS16000 Cross Software Development

The first version of the NS16000 cross software development package, NS-ASM-16, is now available from National Semiconductor Corp. Intended as a support package to facilitate the development of software for NS16032-based systems, NS-ASM-16 will initially be available on the DEC VAX 11 series. NS-ASM-16 cross software development package consists of an assembler, linker, librarian and symbolic debugger.

SPI Offers CMOS Logic ICs

Semi Processes, Santa Clara, has introduced a new family of 33 high-speed CMOS logic circuits available in sample quantities over the next three months. SPI plans to expand to more than 100 devices by early 1983.

Kennedy Acquires BASF Winchesters

Kennedy, Monrovia, CA, has purchased the 8″ Winchester disk product line and manufacturing operations of BASF Systems, Los Gatos, CA, location. The transaction includes the assets, work in progress, spares, inventory and designs, as well as the rights to manufacture and market the BASF 5¼″ disk drive in the US.

NEC Enters Gate Array Market

The Electron Division of NEC Electronics has entered a new market area with the introduction of six high-performance gate arrays. Three TTL arrays range in complexity from 256 to 1,000 gates and have I/O levels that are compatible with 74 ALS series advanced low-power Schottky devices. The three CMOS arrays range from 858 to 2,112 gates and are compatible with standard TTL and CMOS devices.

Seiko Enters Computer Graphics

With the introduction of advanced color and monochrome graphics display terminals, a CRT hard copier, and a pair of digitizing tablets, Seiko Instruments has expanded into the US computer graphics market. The first raster scan graphics display with hardware anti-aliasing is the latest in the series of graphics terminals.

DEC And FPS Announce Agreement

Digital Equipment Corp and Floating Point Systems have announced a cooperative marketing agreement to market a FPS Array Processor and VAX computer combination for use in computation-intensive applications. Floating Point System's FPS-164 Attached Array Processor interfaces with Digital's VAX-11/780 and VAX-11/750 32-bit computers.

Pyramid To Market Supermini

Pyramid Technology will market a general purpose supermini computer later this year, backed by $3 million in venture capital. The 32-bit supermini includes a new proprietary design concept that will permit users to expand processing power and functionality in incremental stages.

Biomation And Millenium Merge

Gould has established a new unit targeted toward the high end of the test and measurement market by combining Millenium Systems, Cupertino, CA, and Gould Biomation, Santa Clara, CA. The new operation, with joint manufacturing, marketing and product development capabilities, is part of Gould's Instruments Division.

Lifeboat Offers EM80/86 Emulator

Lifeboat Associates has announced the publication of the new EM80 emulator which permits SB-80 and other CP/M-80 compatible software to run on the IBM Personal Computer under DOS with no hardware addition or change.

DRAFTING SYSTEM 1

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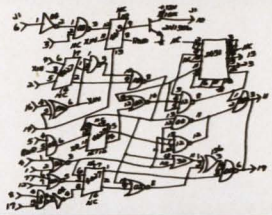
FREE-HAND SKETCH



"DS1" allows operator to digitize directly from a free-hand sketch. Vocal Output prompts operator as IBM Microcomputer collects data. Enter a "D" size in 1 hour. NO GRIDS. EDITS are performed in minutes.

COMPUTER PROCESSING

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Computer straightens slanted lines, uses correct size symbols and enters alignments among symbols entered by user during input. Drum plotter or Electrostatic plotter output.

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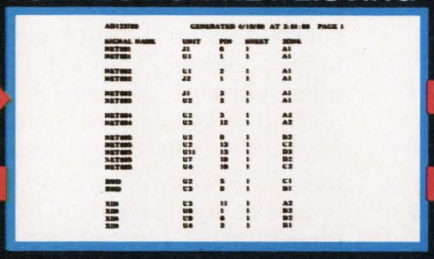
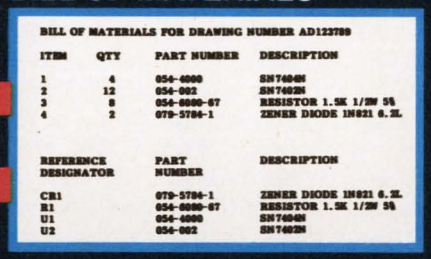


BILL OF MATERIALS



BILL OF MATERIALS FOR DRAWING NUMBER AD123789

ITEM	QTY	PART NUMBER	DESCRIPTION
1	4	054-4080	SN74040N
2	12	054-002	SN74002N
3	8	054-6080-67	RESISTOR 1.5K 1/2W 5%
4	2	079-5784-1	ZENER DIODE 1N821 6.2L

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
CR1	079-5784-1	ZENER DIODE 1N821 6.2L
R1	054-6080-67	RESISTOR 1.5K 1/2W 5%
U1	054-4080	SN74040N
U2	054-002	SN74002N

"DS1" automatically provides Net and Bill Lists directly from data base of digitized schematic.

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COMPUTERVISION
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"DS1" interfaces to P.C.B. Routers, Wire Wrap, Simulation and Test Programs.

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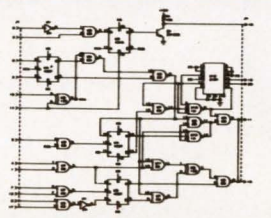

"DS1" performs Back-Annotation from a "Was-To" list derived from the P.C. Router. "Back-Annotation" automatically updates the schematic to agree with the circuit board component placement.

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When Are 4 Crays Not Enough?

Truly a national computer resource, the Los Alamos facility, operated by the University of California for the US Department of Energy, is one of the most extensive computer complexes in the world. Early in May, the press was permitted to peek at the vast range of capabilities hidden in the Northern New Mexico mountains. A day packed with information stimulated discussion about the future super computers.

The extremely sophisticated staff at Los Alamos feel that the present facility is probably two super computer generations away from today's needs. Current needs are barely being met by the Cray 1 machines and by 1990, a machine 100 times more powerful than a Cray 1 or Cyber 205 will be needed for weapons design. They expressed concern that the next generation of super computer may not come soon enough or be good enough. They are also deeply concerned about the nationality of the next super computer generation.

Strong signals coming from Japan indicate that the next super computers may be Japanese. Los Alamos has already started looking at the proposed supers now being developed in Japan. On this side of the Pacific, little seems to be happening in the development of a new super; at least, not with the same level of R & D funding and government investment.

Certainly if the next generation of super computers does originate in Japan, there will be a few more American companies in trouble—to say nothing about our technolgical leadership. It is a dilemma for an organization like the Los Alamos National Laboratory and for the US super computer producers, too. Can a government organization buy imported computers? Yes, under our present laws a US subsidiary of a foreign company can sell to the US government as though it were a domestic supplier, if it follows the existing rules.

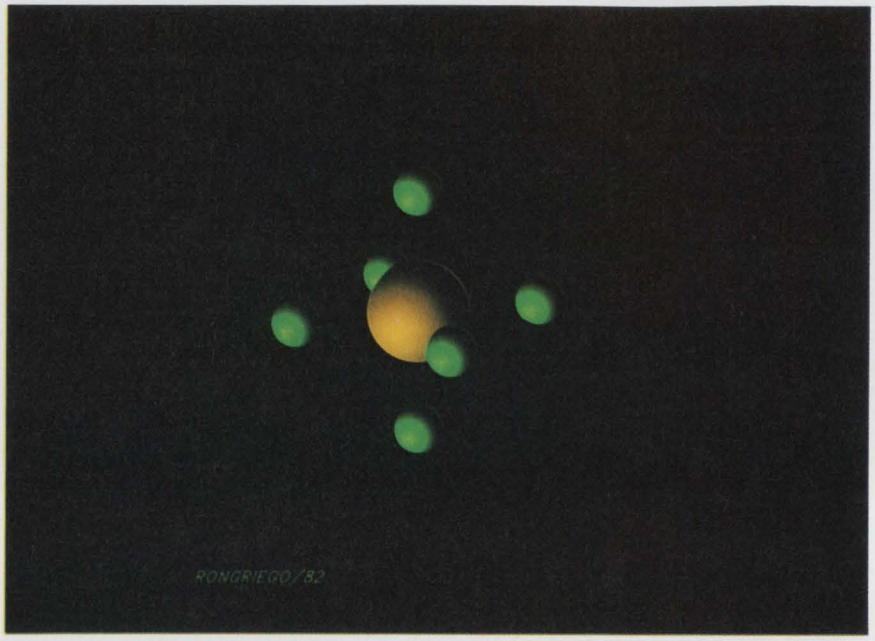


Figure 1: The above representation of an SF_6 molecule was created at Los Alamos National Laboratories by Ronald Griego.

Of course, the other consideration in procuring foreign computers for a strategic resource like Los Alamos would be national security. Media day organizers at Los Alamos did not make this their main issue; however, it is one that the US government and the US computer industry must face in a very short time. Will the US computer manufacturers be able to leap ahead to meet the needs of Los Alamos and other government facilities, or will they concentrate their efforts on short-term markets? The non-government users of the current Crays and other supers now include oil companies and other businesses that do not need to move ahead as fast as Los Alamos. This commercial market is also larger than the government market, so it will get the most attention.

Super Computers

From a few mechanical desk cal-

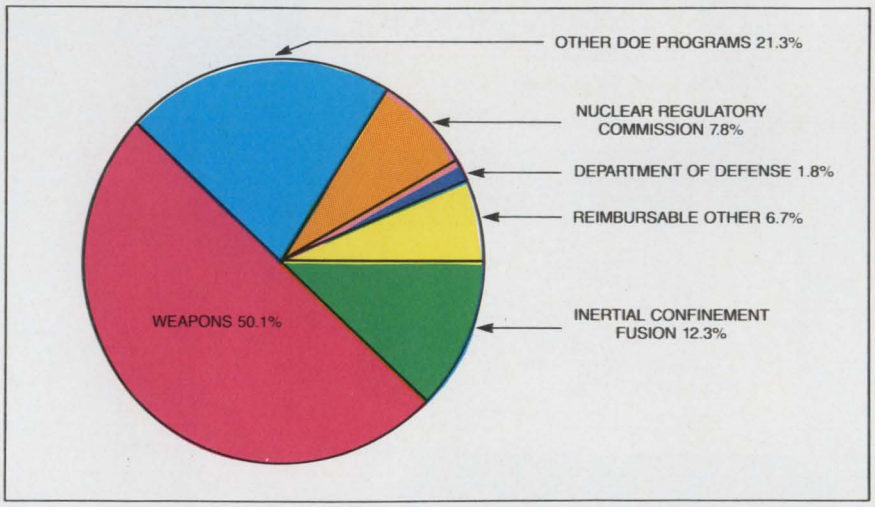
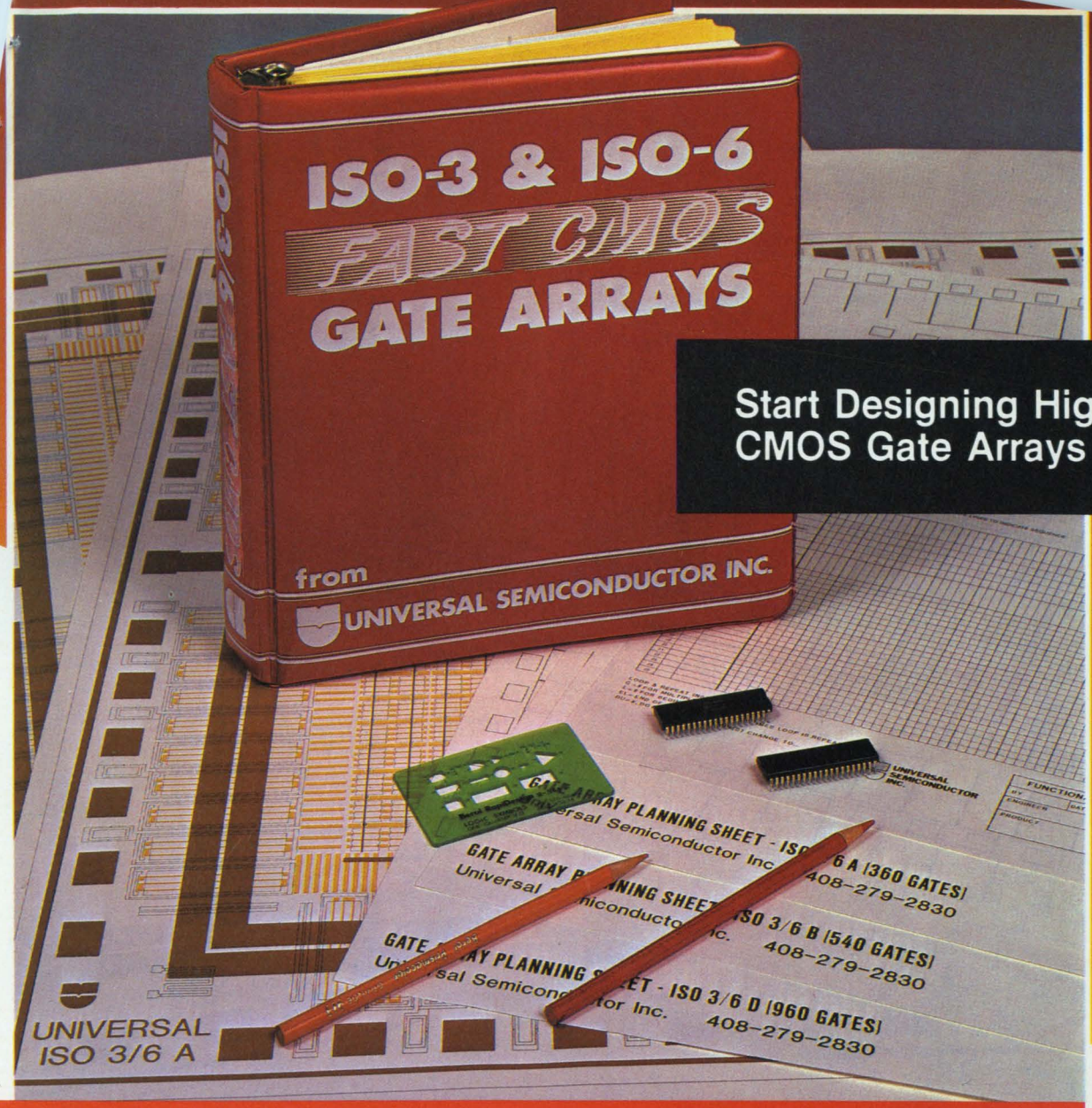


Figure 2: Distribution of computing services, fiscal year 1981.



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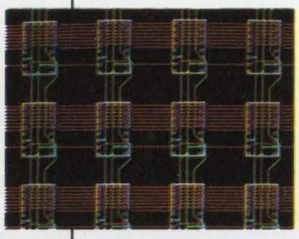

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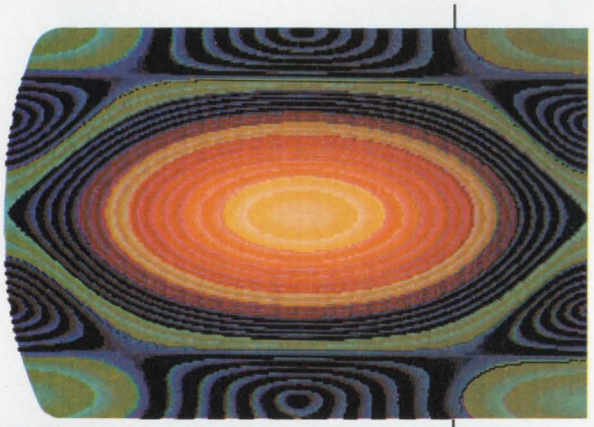

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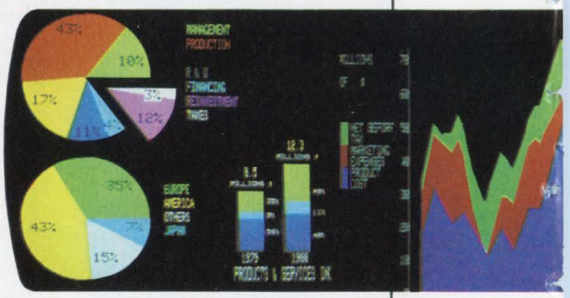

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culators used in 1943 to design the first atomic bombs, the Los Alamos National Laboratory has become a world leader in using computers. Today, four Cray 1 machines with 6 trillion words of permanent memory form the nucleus of the Los Alamos computer operation. Over 3500 users are connected to one of the most complex computer networks ever assembled for interactive time sharing.

Crays are only the tip of the Los Alamos computer pyramid. In fact, a pair of DEC VAX 11/780 are used to operate the Crays. More than 50 other VAX machines are used along with four CDC 7600's, a CDC 6600, and a pair of CDC Cyber 73's to round out the main computing facility. At any given time, the 3500 users have access to about 2.7 trillion words of on-line storage in vast disk forms. Another 4 trillion are stored in IBM 3850 Mass Storage Systems, and these tapes perform like linear disks, with average access time running 10 seconds for any data. The 3850 storage system is managed by an IBM 370/148 and 4341 control processors. Two of the latest model Crays have internal memory capacities of 4 million, 64-bit words.

What can you do with all of this computing power and memory? Things most scientists would like to be able to try. Just think of the results that can be obtained running a program on a Cray for 10–20 or even 100 hours. Problems in hydrodynamics, Monte Carlo techniques, creating a data base for DNA studies, designing nuclear, laser, and particle beam weapons, or searching for safer, more efficient methods of disposing of nuclear wastes are only a few of the daily problems tackled at Los Alamos. By 1990, Los Alamos expects to have 5000 to 6000 users operating on an even bigger network.

Three separate types of computing services are carried out at Los Alamos. First, is open scientific calculation used for a wide range of energy, defense, earth and space sciences, life sciences, chemistry, physics and mathematics. Second, is the administrative operations of the laboratory and its staff of near 7000 people (2700 are technical staff, and half of the staff holds a Ph.D). Third, is the classified computing involved in designing, developing, and testing nuclear and beam weapons for the national defense. This type of computing may account for more than half of the computer usage. It also presents very special problems of security with 3500 users on line.

QUANTITY	DESCRIPTION	SYSTEM	TOTAL POWER (CDC 6600-1)
3500	USERS		
4	CRAY-1	CTSS	64
4	CDC 7600	LTSS	16
1	CDC 6600	NOS	1
2	CDC CYBER 73	NOS	1
50	DEC VAX 11/780 (DP/s)	VMS	10
1	COMMON FILE SYSTEM (CFS)	VS1	
1	OUTPUT STATION (PAGES) (TWO VAX 11/780)	VMS	
1	PRODUCTION CONTROLLER (FOCUS) (TWO VAX 11/780)	VMS	

Figure 3: Los Alamos National Laboratory's major computing resources.

A Real Computer Network

Keeping 3500 users happy is a challenge few computer installations have been forced to meet at the level of scientific computing performed at Los Alamos. Not only must the network manage the communications and time sharing on the vast array of computers, but the hardware must remain transparent to the users. This permits users to work on a variety of computers, depending on availability and the scope of the problem.

Network switching is performed by three VAX 11/780 machines with PDP-11's serving as concentrators and switches. The entire network is interconnected with miles of coax, and fiber optic links are being installed for new equipment.

User terminals have been standardized throughout the facility to TI Silent 700 series, DEC VT100, Tektronix 401X series, and Advanced Electronic Devices' 512's for color graphics. RS232 standards are used; however, by standardizing the network and all of the equipment uses, it becomes much easier to keep the network running without problems. Standard user equipment also helps make the entire system transparent. User codes, for example, are preserved even if the hardware is changed or modified. Users really don't care what equipment is operating.

Classified user access is very tightly controlled with special access codes and verification procedures. Few details were available on the exact system and procedures used, but considering the level of security involved in nuclear weapons design, it has not been incorrectly accessed even by accident since its inception.

Modeling

While most computer models are 2-dimensional, Los Alamos is producing some 3-dimensional models. The concept of modeling is straight forward for most applications. In dealing with explosives, modeling in 3 dimensions is almost a must if the results of an explosive reaction are to be predicted. This is a very new area at Los Alamos; however, they appear to to be making rapid progress. In nuclear engineering, the 3 dimensions added to modeling, for example, are of extreme value in predicting failure modes in a reactor core or determining the smoke plume of a coal-fired pow-

er plant.

Modeling problems, even 2-dimensional, are not easy or fast. On a Cray 1, the designer and the computer can work together very efficiently. A demonstration program run during media day showed how fast the problem of deforming a solid cylindrical object could be solved. While only a demonstration, the process took about 15 minutes on the Cray. The same problem run on the CDC 7600 would have required more than two hours.

Graphics

Color graphics at Los Alamos are enough to make anyone envious. In addition to the CRT displays, hard copy capability is up to 80,000 printed pages per day. In addition, the graphics system can record 150,000 Microfiche images per day along with 6000 frames of 16 mm film and 3000 frames of 35 mm film. About 400 plots, 11 inches wide, and 75 plots, 36 inches wide, can also be turned out in a day. Turnaround time is one hour for paper copy, four hours for Microfiche, and overnight for color film.

The Future

It is hard to imagine that with all the computing power available, the Los Alamos National Laboratory has a problem getting the job done; but they do. Some of the problems they attempt to solve are so complex that they tax the power of the Crays to the limits.

The next step is bigger and faster parallel processors—100 times more powerful than the Crays. Better algorithms may have to do for now, but to support the modeling needs of Los Alamos alone, the only practical solution appears to come from higher speed, parallel processing. Josephenson Junction machines may be part of the solution, but for the short term, the problems with JJ machines may keep them from practical applications for some time. The US main frame manufacturers have a problem meeting the needs of Los Alamos and other government computer centers.

The number of super computers needed for this government segment of the market is too small to justify the large amounts of R & D necessary to solve the problems. Like the semiconductor industry, the computer business is driven by market share, and it can be very costly to serve such a small market with the highest technology. Japan, a country that has government support for its electronics industry, may be willing to risk the R & D investment to gain control of the high end of our computer business—then the middle and the low ends may follow.

—Groves

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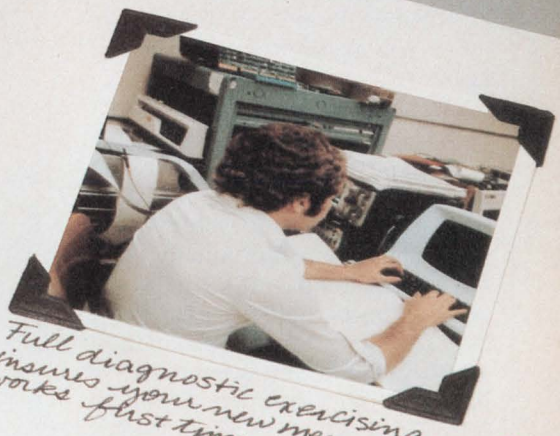

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Japan Leads Robot Boom

In the exploding robot market, Japan is clearly the leader. There are more than 70 Japanese robot manufacturers—more than twice the number of second-ranked West Germany, and nearly three times as many as the United States. Japan also leads in number of installations, with 14 times more robots in use than in the US.

Despite Japan's high production levels, very few robots have been exported, primarily because demand in Japan has exceeded production. Another factor is that robots have not traditionally been mass-produced, making large-scale exports unlikely. In 1974, only 2.9% of Japan's production was exported. This rose to 4.5% in 1977, but dropped again to 2.6% in 1980. According to this report, however, this trend is likely to reverse. Several Japanese manufacturers are looking toward increasing their exports; Dainichi Kiko Co, is exporting about 60% of its production, and Mitsubishi plans to export 30% of its production by next year. Another significant trend is the growing number of joint ventures between Japanese, European, and US companies (e.g., Hitachi and General Electric; Fujitsu Fanuc and Siemens; and Kawasaki, Unimation, and ASEA).

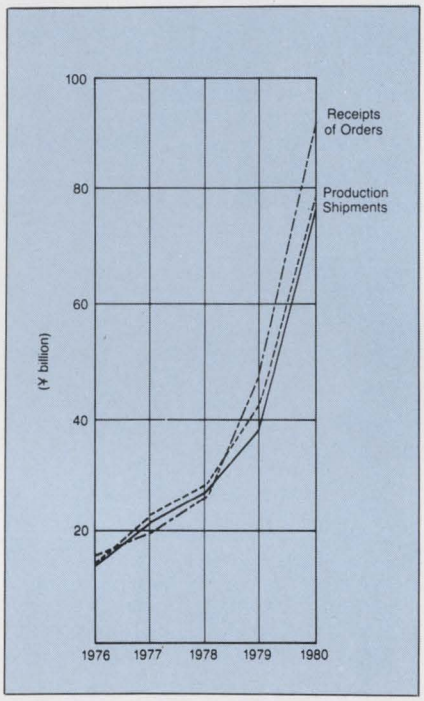


Figure 1: Japanese robot industry growth

Unimation has recently announced the receipt of over $12 million in robot orders from major foreign and domestic automobile manufacturers. The Unimate robots are destined to go to Chrysler, Ford, British Leyland and Daimler-Benz. Unimation will soon supervise the installation of sixty-nine Kawasaki Unimate robots in the Nissan Motor manufacturing truck body assembly plant in Tennessee.

A 228-page report is available from Venture Development Corporation of Wellesley, MA. Industrial Robots Industry in Japan, published by Yano Economic Research Institute Co., Ltd. of Tokyo, presents a comprehensive analysis of the Japanese robotics industry. According to the report, nearly 20,000 robots were produced in Japan in 1980, and estimates for 1981 indicate a five-fold increase in unit production. Since 1976, annual growth in production has ranged from 26% to more than 100% leading to a cumulative total of 76,700 units produced in Japan since 1968. For more information, write: Venture Development Corp., One Washington St., Wellesley, MA 02181.

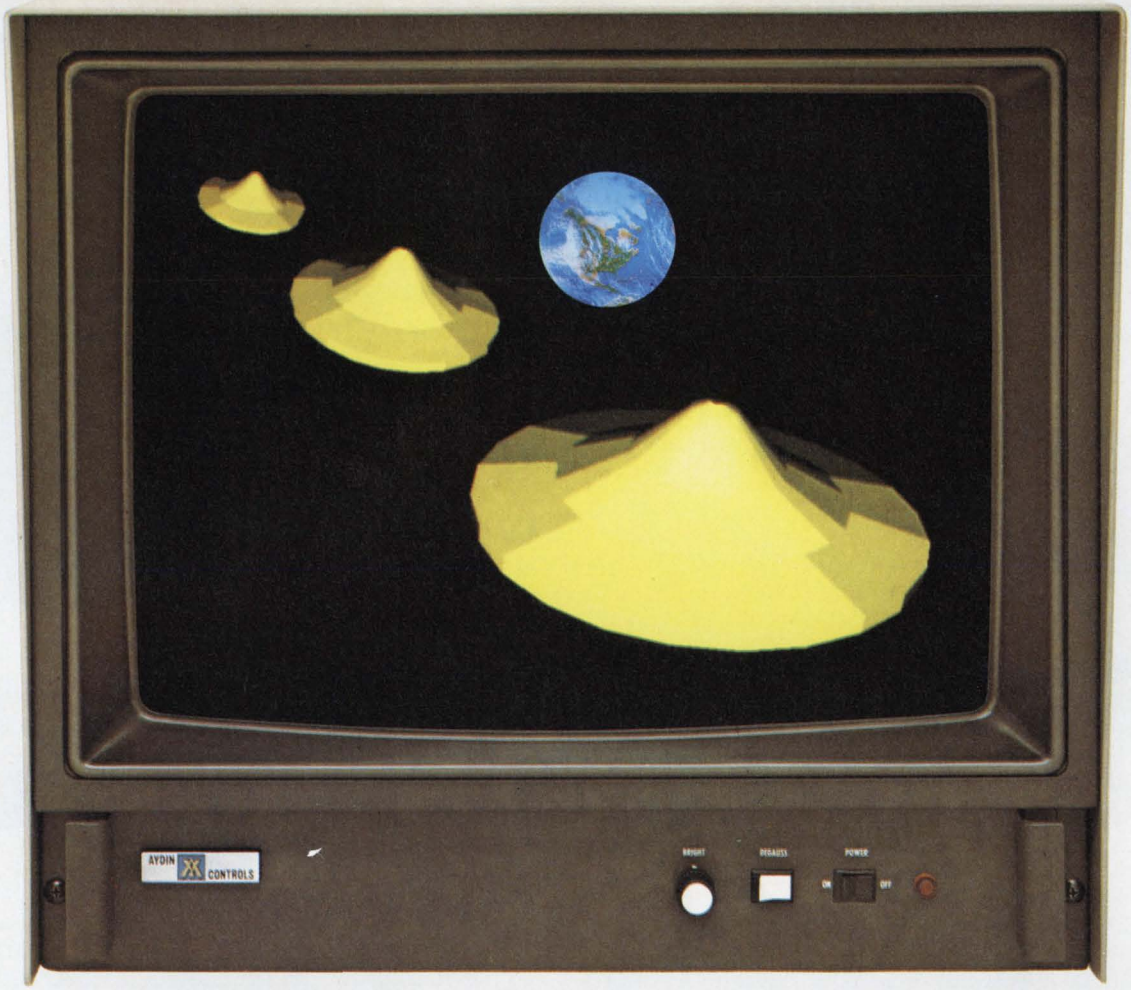
CMOS Markets Top $26.8B In 1990

By 1985, CMOS will displace NMOS in one of the greatest evolutionary transitions in this decade. Although IC makers, board makers, and OEMs recognize that CMOS is improving in speed, many fail to comprehend the magnitude of this transition.

Once used only in watches and calculators due to its slow speed, low power consumption, and its noise immunity, newer CMOS parts offer 2ns switching speeds, lower power consumption, greater alpha particle immunity, and ultimately lower per-cost functions than bipolar or NMOS.

Both US and Japanese companies are developing high-performance CMOS chips. National Semiconductor is aggressive and is developing CMOS versions of its NS16000 16- and 32-bit μCs; Intel is backing into CMOS and has developed 1K, 4K, and 16K static RAMs; and Motorola has developed an 8-bit μP chip set compatible with its 6800 family. They and others are also developing CMOS gate array families.

AYCON 16/SERIES



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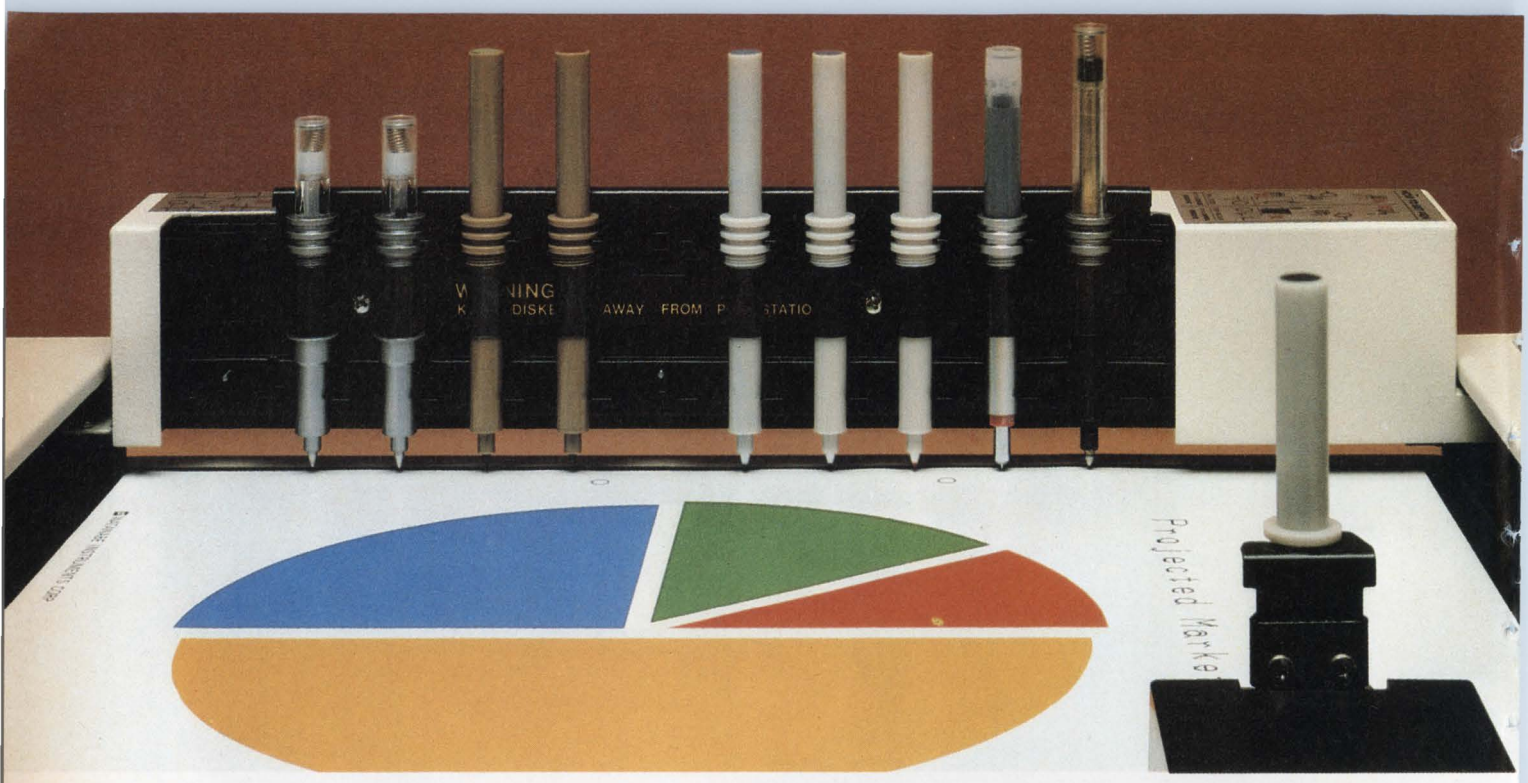

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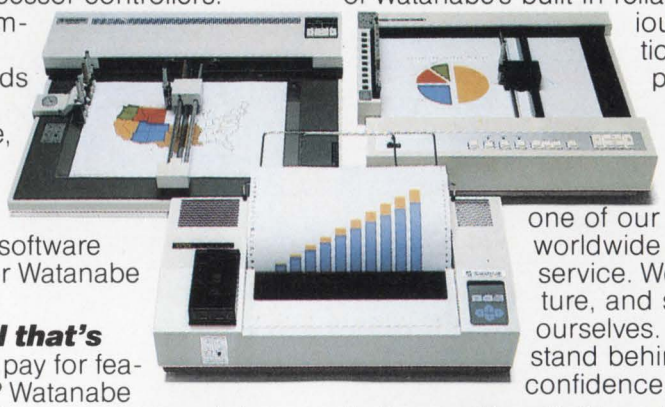

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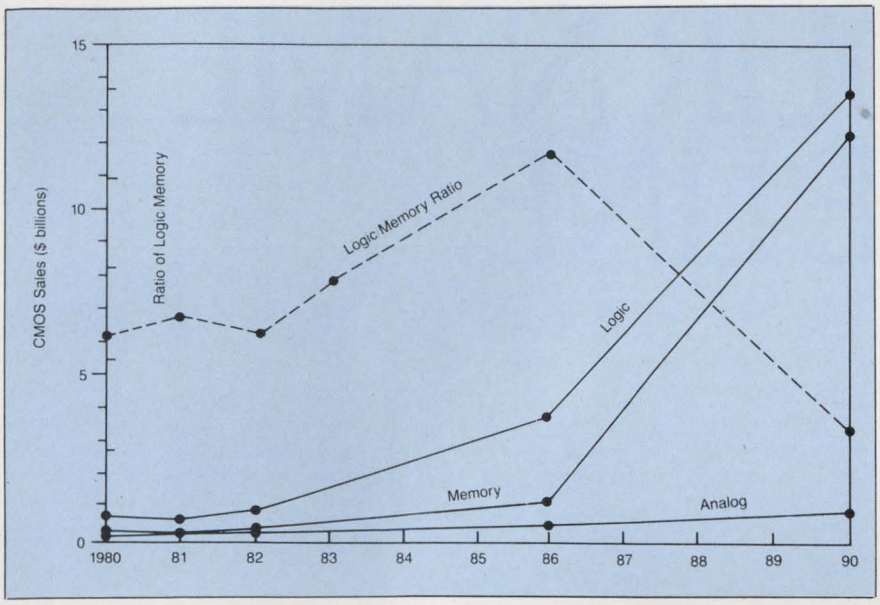

By 1990, the worldwide CMOS market will grow to 26.8 billion. The market for CMOS, in billions of dollars, remained essentially flat up to this year, but will begin a moderate rise in logic, but little in memory, partly because of vendor commitments. In 1986, both logic and memory will assume spectacular growth. The logic/memory ratio (dotted line) will be greatest (about 4.4) in 1986, and rapidly plunge thereafter.

CMOS will not only impact bipolar manufacturers such as Precision Monolithics and Monolithic Memories, but even giants like IBM, DEC, Hewlett-Packard, and Western Electric that have large existing commitments in NMOS and bipolar, and little apparent interest in CMOS at this time. These captive suppliers and others with similar IC technology commitments may see their competitors gain market share in the future as a result of producing CMOS-based equipment with superior performance and lower cost.

These projections were excerpted from a comprehensive CMOS study, report no. 1004, "The Impact of CMOS On Competing IC Technologies" ($1500). For more information, contact: *Mrs. Alenne Glock, Customer Support, Strategic Inc., 4320 Stevens Creek Blvd., Suite 215, San Jose, CA 95129. Tel: (408) 243-8121.*

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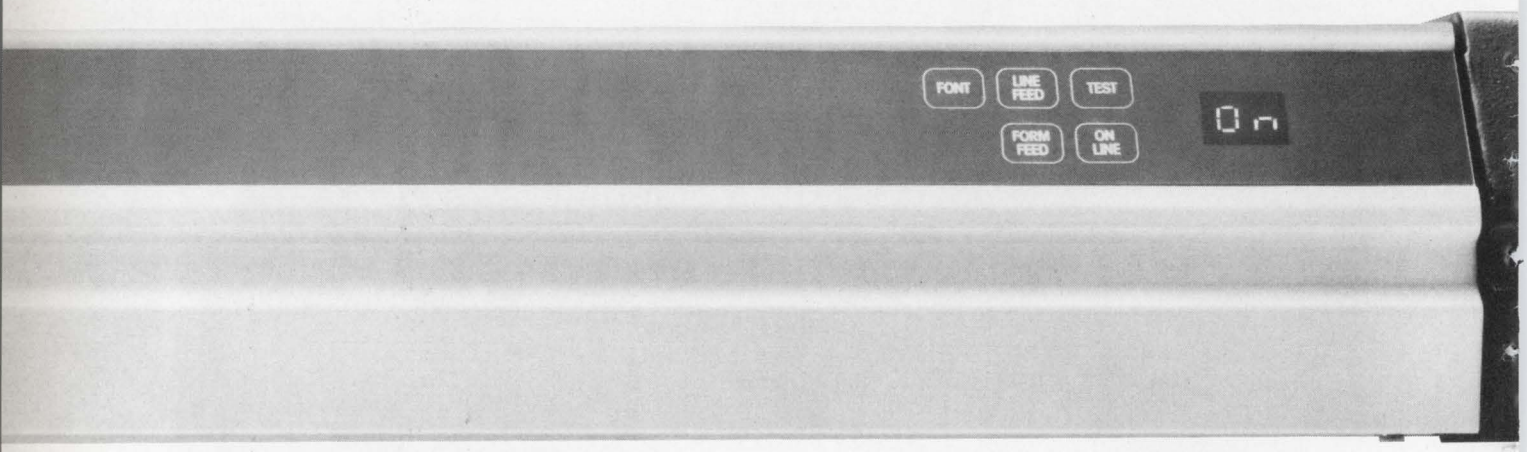

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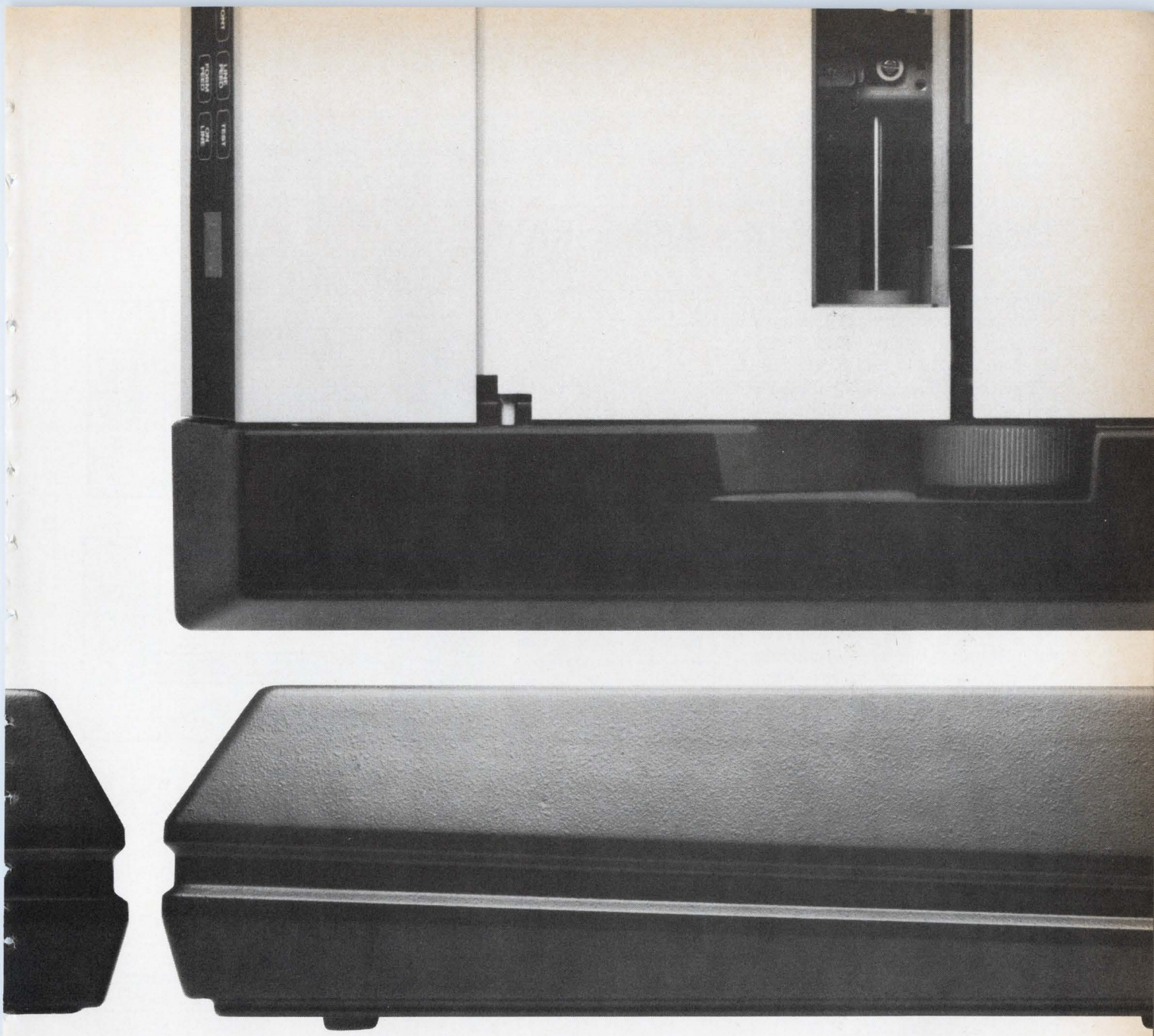

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GENERAL ELECTRIC

Free Samples Of 4K x 4 Static RAMs

The Inmos IMS1420 is a high performance 4K x 4 static RAM having maximum Chip Enable ($\overline{E}$) access times of 45 and 55ns, with a maximum power dissipation of only 600mW. The use of innovative design techniques as well as the latest VLSI technology have combined to produce these characteristics. The IMS1420 features fully static operation requiring no external clocks or timing strobes, equal Address access and cycle times, full TTL compatibility and operation from a single +5V supply. A Chip Enable function provides standby operation reducing power consumption to less than 165mW maximum. The device is housed in a 20-pin, 300-mil DIP.

The Intel 2147H is a 4K x 1 static RAM, having maximum Address and Chip Select ($\overline{CS}$) access times of 45 and 55ns. The maximum power dissipation is 990mW with a standby power dissipation of 165mW. As with the IMS1420, the device is fully TTL compatible and operates from a +5V power supply. The 2147H is packaged in an 18-pin, 300-mil DIP.

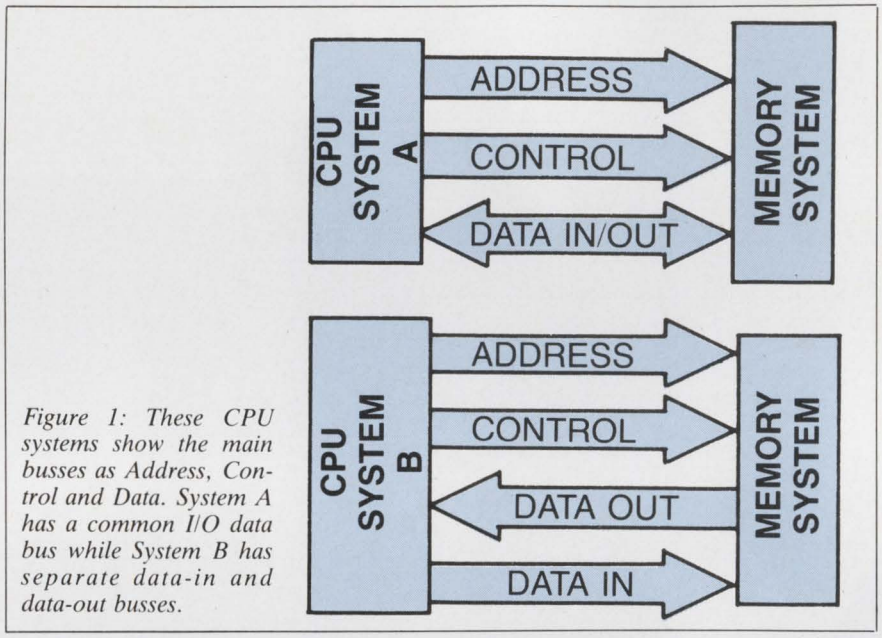


Figure 1: These CPU systems show the main busses as Address, Control and Data. System A has a common I/O data bus while System B has separate data-in and data-out busses.

When comparing the memory devices, the similarities in the pinouts show that both devices are identical in the number of address pins, and both have WRITE ($\overline{W}$, $\overline{WE}$) and SELECT ($\overline{E}$, $\overline{CS}$) control input functions. The differences in the pinouts show that the IMS1420 has 4 common I/O data pins while the 2147H has separate data-in and data-out pins. Com-

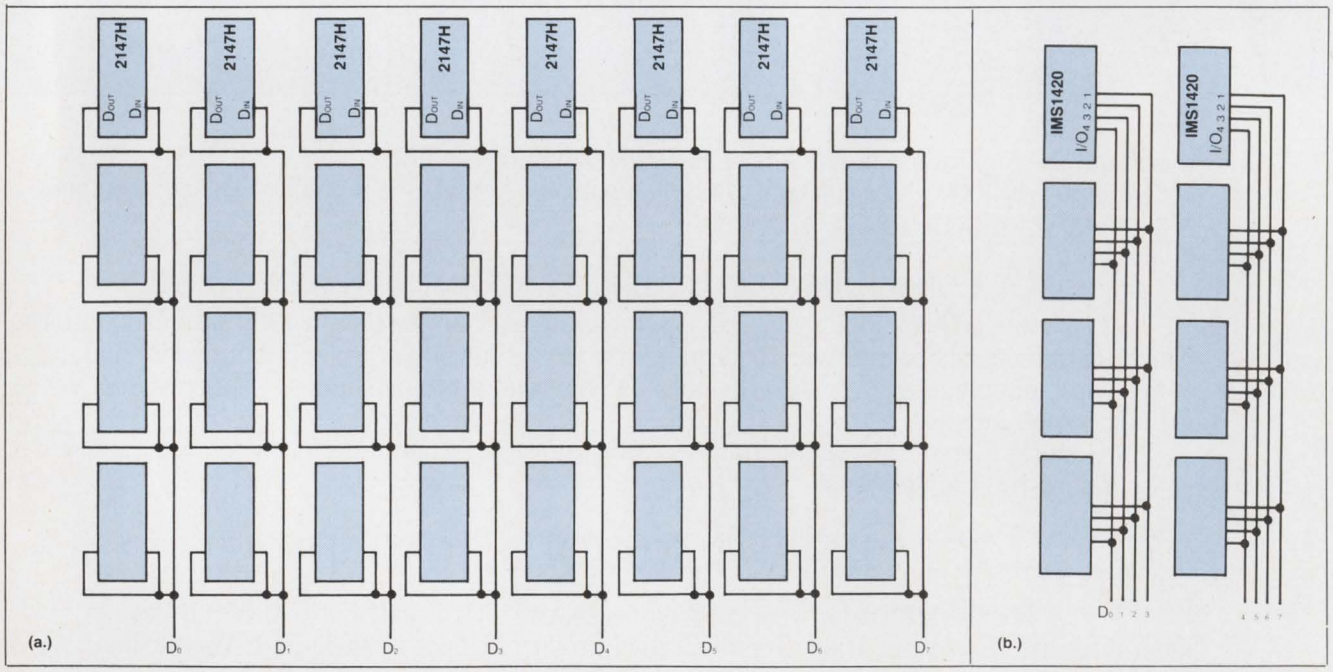
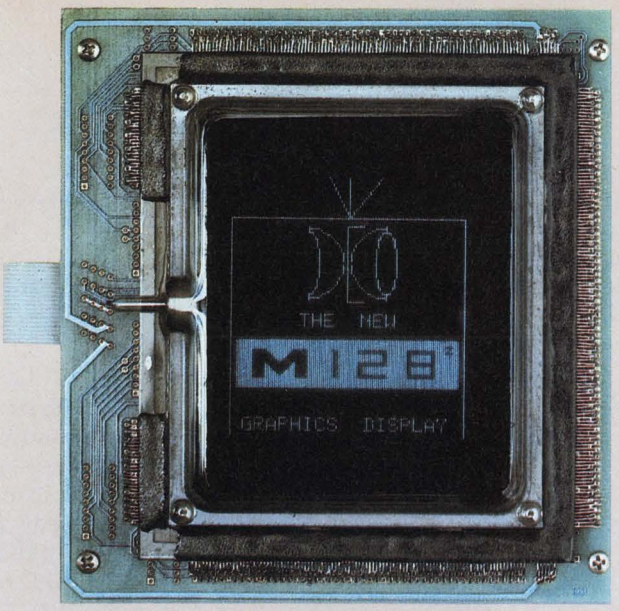


Figure 2: The data I/O pins of the IMS1420 are each tied directly to a bidirectional data line of the data bus.



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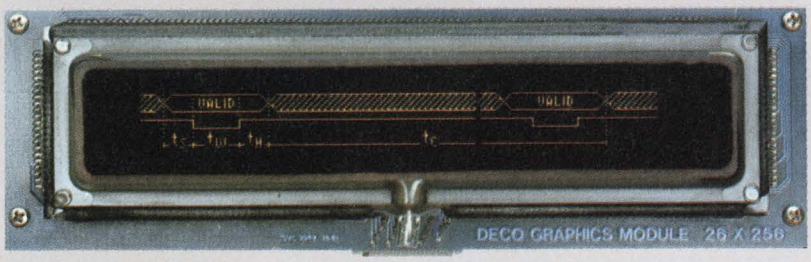
DECO offers the latest in display technology. Close dot spacing and Vacuum Fluorescent technology make the display bright, sharp and highly readable even in daylight with proper filtering. Each dot is independently addressable allowing formation of almost any character or shape the mind can imagine! Graphs, charts, ideograms, waveforms and more can all be displayed. Even reverse video is possible. Complete drive, interface, control logic, refresh and buffer electronics are on board. Only +5 VDC is required to power the unit.

BUT, IF WORDS ARE WHAT YOU WANT, DECO'S SUPER SMART

M128² Thin profile and low voltage made the M128² an ideal alternative to CRT in many applications.

Alphanumeric Displays are specified by engineers all over the world. The bright vacuum fluorescent characters are **highly readable** and filter from natural blue-green to blue, green, aqua, amber and red. VF tube technology offers **high reliability** and tube MTTF up to 100,000 hours. **Low Power** requirements (as low as 65 milliwatts/character) are well below the dissipation of LED or gas discharge displays. DECO's displays are **self-contained ready to use** subsystems. They are microprocessor controlled with all drive, refresh, interface, control logic and buffer circuitry on board. Some units have user programmable character generators. All models have on board power conversion circuitry. Just input +5 VDC and a 7-bit ASCII signal and you're in business!



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DECO'S SINGLE LINERS come in a wide range of sizes from 10 to 40 character positions and 5mm to 9mm character height. 14 segment, 5x7 and even 5x12 matrices available.

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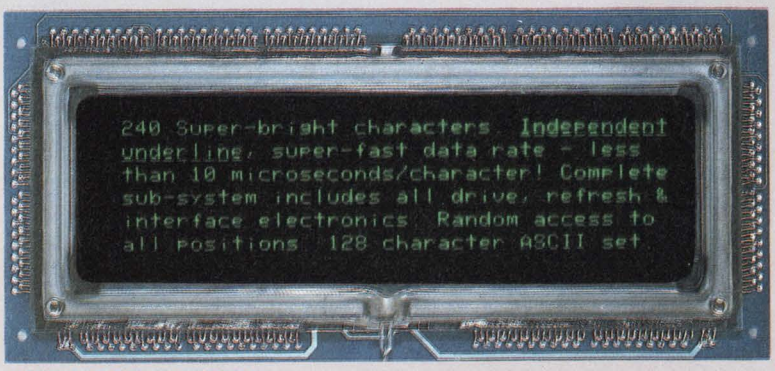

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parison of the READ and WRITE cycles of the devices shows equivalent Chip Enable access times, but shorter Address access and cycle times for the IMS1420.

Interfacing

The CPU systems shown in **Figure 1** show the main busses as Address, Control and Data. System A has a common I/O data bus, while System B has separate data-in and data-out busses.

Interfacing to the address and control bus connections for both systems is straightforward and identical for the 2147H and the IMS1420, with one exception. The 2147H requires the use of a pullup resistor to V_{cc} on the chip select pin, to prevent the device from powering up in the select mode when V_{cc} is first applied. With the IMS1420, when V_{cc} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. Therefore, a pullup resistor from $\overline{E}$ to V_{cc} is unnecessary. After V_{cc} is applied for 2ms, the $\overline{E}$ input controls device selections as well as standby and active modes.

Interfacing to CPU System A is almost the same for the IMS1420 and the 2147H. The data-in and data-out pins of the 2147H are tied together, and then tied to a bidirectional data line of the data bus. The data I/O pins of the IMS1420 are each tied directly to a bidirectional data line of the data bus. (**Figure 2a and 2b**).

Bus contention between data coming into a memory device and data going out of a memory device is only a problem during the WRITE cycle. If $\overline{CS}$ goes low a period of time before $\overline{WE}$ goes low, the device output driver could become active during the time that the input data is placed on the bus. Since both the CPU system and the memory device would try to drive the same data bus line, large current transients can occur. To prevent bus contention, the $\overline{CS}$ must go low after $\overline{WE}$ goes low, keeping the memory output driver in high impedance. Thus, when the input data is placed on the bus, no contention occurs between the output driver of the device and the output driver of the CPU system. This is called a Chip Enable controlled WRITE cycle (**Figure 4**).

The most direct approach to interface 2147H memory devices to CPU System B is shown in **Figure 3a.** Four rows of eight 2147H memory devices are each connected directly to separate data-in and data-out lines. Because the data input and output lines are separate, no special timing during the WRITE cycle is necessary to prevent bus contention.

Four rows of two IMS1420's each can interface to CPU System B, using two 74S240's (or similar bus driver) to interface to the separate data-in and data-out busses. This can be accomplished as shown in **Figure 3b**. The timing for the READ cycle would remain the same, but in the WRITE cycle (**Figure 4**), only a Chip Enable controlled WRITE cycle

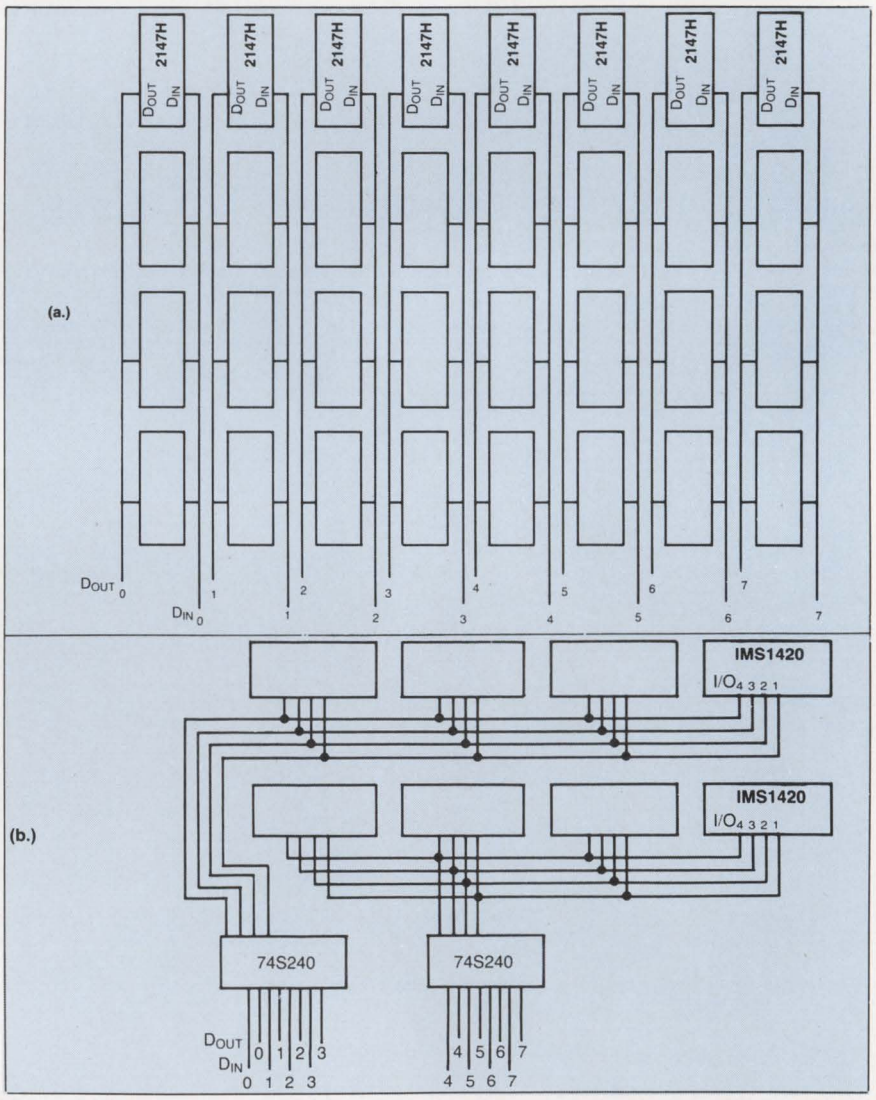

Figure 3: (a) Four rows of eight 2147H memory devices (b) Four rows of two IMS1420s.

could be used. This would keep the data-out drivers of the IMS1420's in the high impedance state during the WRITE cycle, preventing any data bus contention with input data.

Savings

With CPU System A, each IMS1420 could replace four 2147H memory devices.

	2147H	IMS1420	NET SAVINGS
No. of Packages	32	8	24
Area	17.6in²	4.8in²	12.8in²
Power	11.88W	2.2W	9.68W

With CPU System B, each IMS1420 could replace four 2147H memory devices, but two data bus drivers must be added. Still, a net savings can be seen.

	2147H	IMS1420	74S240	NET SAVINGS
No. of Packages	32	8	2	22
Area	17.6in²	4.8in²	1.2in²	11.6in²
Power	11.88W	2.2W	1.6W	8.6W

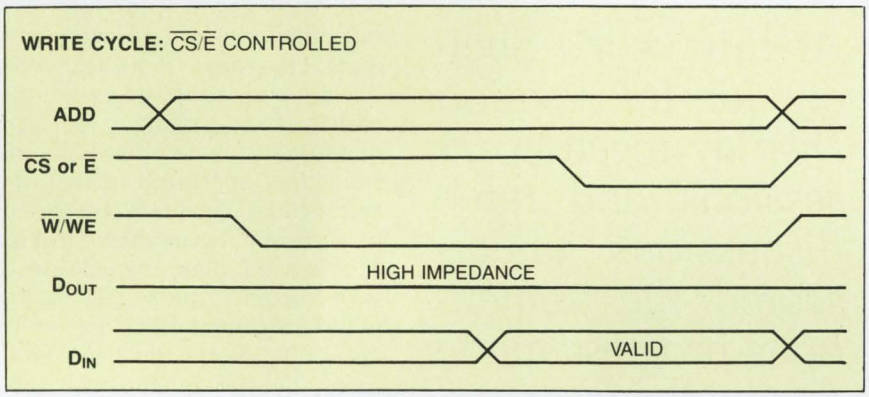

Figure 4: When the input data is placed on the bus, no contention occurs between the output driver of the device and the output driver of the CPU system; this is called a Chip Enable controlled WRITE cycle.

Attention 2K x 8 Static RAM Users:

Inmos is offering a free byte of static memory to 2K x 8 static RAM users who write in on their company letterhead. You must include a description of your 2K x 8 application, including total memory size, access time and power requirements. Two IMS1420 4K x 4 static RAMs will be delivered to the first 100 qualified inquiries. Send your requests to:
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New Technologies Increase Display Alternatives

by Nicolas Mokhoff

Display technologies are reaching new stages of development that promise to razzle and dazzle the user of computer terminals. Such technologies as color CRT, plasma display, electroluminescent display, liquid-crystal display and projection television display are all providing brighter and sharper images while being packaged in ever tighter enclosures that use less power.

Progress in these technologies was reported at this year's Society for Information Display conference held in San Diego, CA, May 12-13. The following achievements stand out:

- Color CRTs will soon display a brighter, sharper picture due to a couple of developments that make use of a focus mask instead of the traditional shadow mask. This increases the screen area that the electron beam excites from the usual 18% to more than 50%.
- A non-multiplexed LCD that uses static addressing techniques allows for both graphic and alphanumeric display by combining the static addressing technique with an interlaced column electrode structure. This LCD matrix yields better electro-optical characteristics than existing multiplexed matrix LCDs.
- Two distinct classes of a relatively new flat display technology called cathodoluminescence are competing for commercialization and both types made significant advances in the past year.
- High-resolution CRTs on the order of 4096 × 4096 pixels are being developed.

CRT Advancements

Engineers at RCA Laboratories in Princeton, NJ developed a focus-mask tube using both dipolar deflection and quadrupolar focusing to triple the beam transmission from 18% of the screen size (which is characteristic of the conventional shadow mask) to over 50%. At the same time the engineers were able to keep the mask operating voltage down to only 2.5% of the screen voltage. This low value relieves the difficulties associated with secondary electrons, dielectric breakdown, and spot degradation in earlier focus masks. A dipole-quadrupole focus mask is made from the apertured plate whose rectangular apertures are bisected by vertical wires as shown in **Figure 1.** When the plate is made positive with respect to the wires, electrons in the horizontal plane are both deflected by the bipolar fields and focused by the quadrupolar fields. Thus the electrons traveling through adjacent windows overlap in the phosphor screen behind the vertical webs of the plate. RCA engineers designed a prototype focus-mask 10″ diagonal color tube with a flat mask and a screen, with the beam hitting the flat mask screen at a maximum angle of incidence of 37.5°. The resultant display has good color purity over the entire screen.

At this year's Society for Information Display meeting, 23 sessions and three discussions underscored the tremendous progress made during the last year.

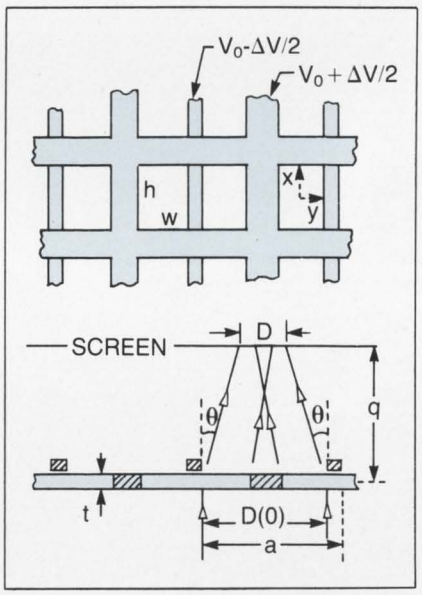


Figure 1: A dipole-quadrupole focus mask is made from an apertured plate, with rectangular apertures bisected by vertical wires.

Engineers at Philips Research Laboratories in Eindhoven, the Netherlands, are using a magnetic focus mask principle for use in color CRTs which can also increase the mask transmission to at least 50%. The method does not require a separate high-voltage connection; the magnetization is straightforward, with a main field configuration being quadrupolar with the north poles on one side and the south poles on the other side of the iron mask (**Figure 2**). The electron beam is deflected between the sandwiched portions of the parallel strips by the magnetic field of the two materials. Because of the enhanced mask transmission figure of 50%, the brightness can be increased or the beam current decreased. In the latter case, apart from the decrease in power consumption, the resolution can be higher due to a smaller spot size.

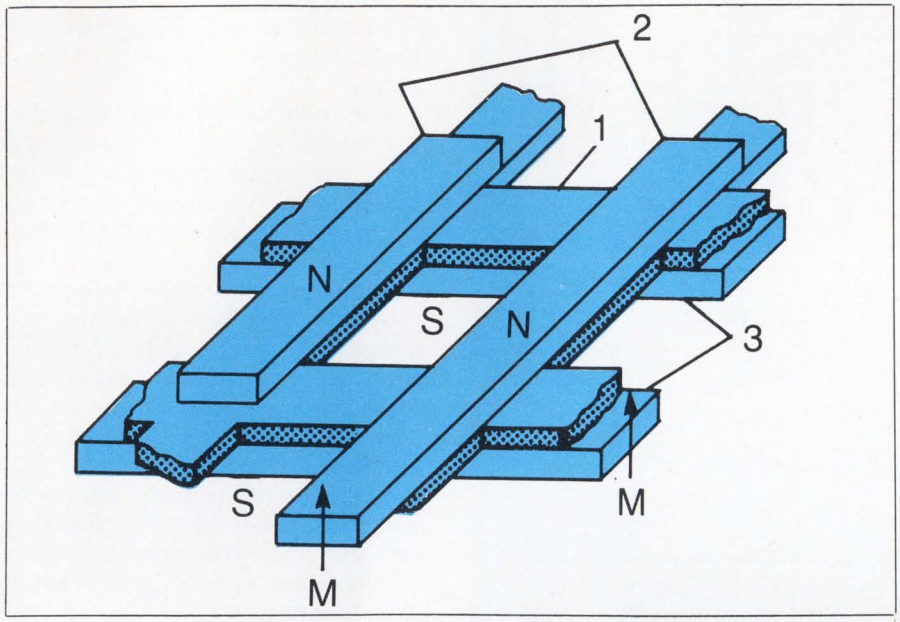


Figure 2: Mask structure with soft iron mask (1), hard-magnetic bars (2 and 3). The arrows M indicate the direction of the magnetization, leading to north poles and south poles.

LCD Developments

In the realm of LCD matrix displays, a number of developments are noteworthy. Engineers at Asubal SA, of Neuchatel, Switzerland, have developed a non-multiplexed matrix LCD whose electro-optical characteristics are distinctly superior to those of existing multiplexed matrix LCDs.

Static addressing with a dot matrix display is made possible by using an interlaced column electrode structure and a special character format. Drive signals are applied selectively to the rows and columns under μP control. The text to be displayed is entered via a keyboard and stored in RAM. The ROM contains the μP program, the quasi-random sequences and the alphanumeric character codes. Each character code is defined by a unique set of column signals. The μP organizes the signals corresponding to each character of the text and stores them temporarily in the RAM. Then the processor reorganizes the contents of the RAM to generate the correct addressing of the signals towards the matrix. Eight consecutive bits are transmitted sequentially via the data bus to the matrix display interface (**Figure 3**). Each data byte is oriented to the appropriate interface register by means of a μP generated address. After the last data byte is transmitted, the RAM reading is re-initialized to force the signals that are applied to the rows and columns to become periodic.

Vacuum Fluorescent Displays

Every year new developments are reported in various flat panel technologies such as plasma and electroluminescence. A relative newcomer is the flat cathodoluminescent display which is defined as a light-emitting display in which electrons in a vacuum strike phosphors to create an image, and in which the tube depth is significantly less than the diagonal.

There are two distinct types of cathodoluminescent displays. The first uses a single modulated electron source which is scanned point-by-point over the display area. The second type uses an area source of electrons, an XY matrix of electrodes to select an element, and a low-voltage phosphor screen. Better known as vacuum fluorescent displays (VFDs), these displays are commercially available and provide bright, low-cost alphanumeric and graphic displays.

One of the limitations of this technology has been the resolution, which has been limited to about a 0.6-mm dot spacing. At Ise Electronics Corp (Ise, Japan), a high-resolution 256×256 dot matrix VFD has been constructed with a dot pitch of 0.4 mm in the X and Y directions and a dot size of 0.2 mm^2. The high-resolution display was fabricated from a unique anode and electrode configuration. The grid configuration has a part of the anode intercepted by the grid when viewed from the front of the panel. The effective visible dot area is approximately uniform regardless of the viewing angle. Compared to the standard grid configuration (**Figure 4(a)**) this version (**Figure 4(b)**) has an improved cut-off property due to the

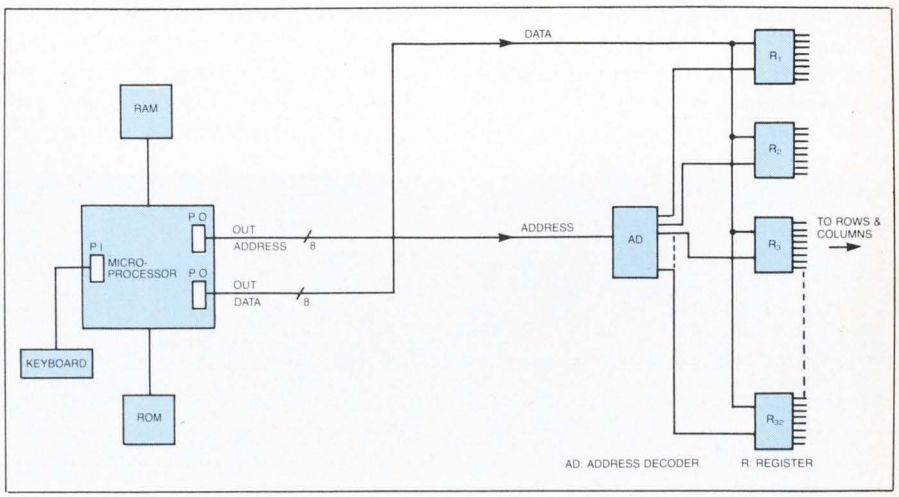


Figure 3: Eight consecutive bits are transmitted sequentially to the matrix display interface via the data bus.

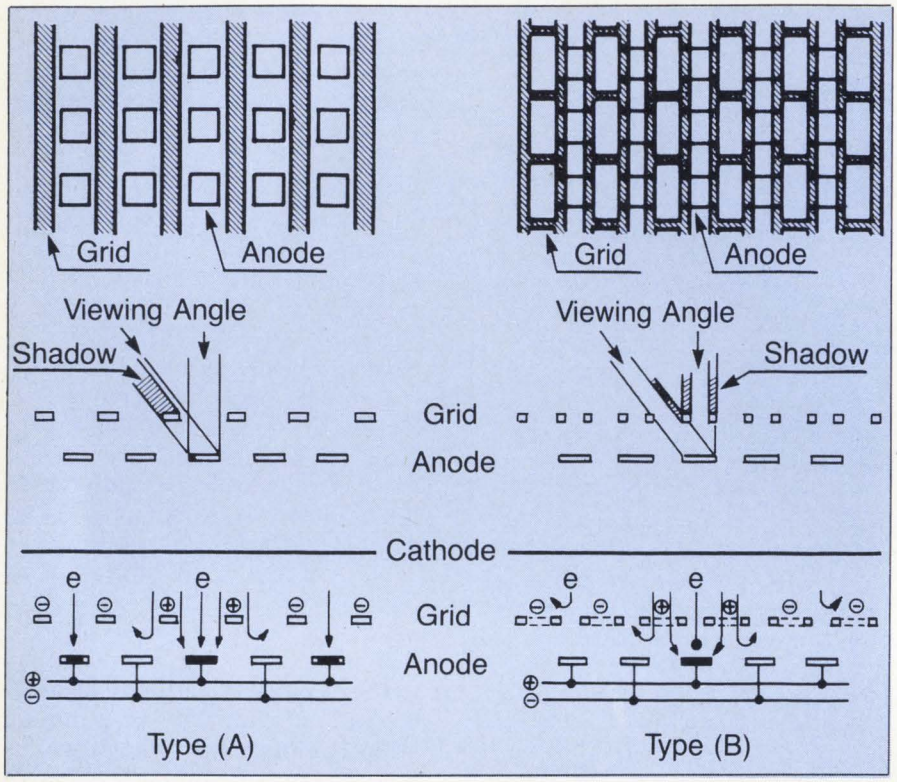


Figure 4: Luminescence versus viewing angle according to grid configurations.

doubling in the number of grid wires which reduces the wire gap. The 256×256 dot matrix VFD exhibits a luminance of about 80 fL under the 120V peak-to-peak voltage condition.

Grid wires also played a crucial role for engineers at the Choa Display Corp (Matsusaka, Japan). They designed an X-Y dot matrix VFD with a dot pitch of 0.3mm. Choa Displays' VFDs are sequentially scanned one grid at a time. The typical rise and fall time is approximately 5μs/dot. A 256×256 dot matrix can be scanned in a relatively short 8 to 10 ms.

A high resolution graphic VFD has also been developed by Futaba Corp (Chiba Perfecture, Japan). Three to four lines/mm were achieved by applying electrodes on the anode substrate while the phosphor is applied on the electrode surface in the form of a stripe. The column electrodes are arranged to cross over the phosphor coating and the specified number of cathode filaments are aligned a specified distance apart from the column electrodes, covering the whole display area. Voltage can be scanned on two grids at a time, shifting sequentially to drive the system. The display signals, synchronized with the scanning, are applied to the anode electrodes according to the pattern to be displayed.

	1980*	1981*	1982*
CRTs (all types)	4,268	4,370	4,650
LED	450	500	550
LCD	440	438	486
Gas Discharge (all)	87	97	110
VFDs	52	60	71
Incandescent	14	15	17
Other	4	4	5
TOTAL	5,315	5,484	5,889

**Millions of Dollars*

Table 1: Estimated worldwide market for electronic displays, in millions of dollars (source: Stanford Resources, San Jose, CA).

The tradeoffs for integrating displays into systems are among the more challenging problems for system engineers. This challenge is being met by researchers at the Naval Ocean Systems Center (San Diego, CA) who have developed a computer graphics technique for interactive design. The MOVIE BYU Graphics Package allows the workstation designer to convert design concepts into graphic images, to generate and refine them and then communicate these images to the user. Thereby, the designer and user can work out the major workstation issues and resolve them jointly.

Using hardware component data sets that are stored in the computers program, the workstation designer combines, replicates or otherwise tailors the component data sets to produce graphics images of entire workstation configurations. Two computer systems are used to generate the component and workstation graphics images. A Univac 1100/82 computer uses the 32-bit word length version of MOVIE BYU, which is principally used for line drawing graphics images. The images are previewed on a Tektronix 4000 series terminal and plotted off-line on a pen plotter.

The second system is a DEC 11/70 that runs on a Unix operating system and supports a Ramtek 9400 color raster scan display system with 1024×1024 resolution and 16-bit planes. The DEC uses the smaller 16-bit version of the graphics software package.

Using these systems, complex workstations can be designed and configured for various applications via remote terminals without the need for designers to be at the site of the central computer.

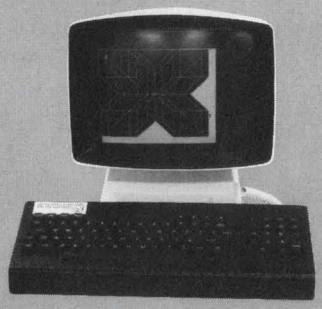
Visual Ergonomics

Emphasis has shifted recently from the display electronics to the interaction between the viewer and the display. This has, in some cases, resulted in some form of regulation for designing, manufacturing and applying these display systems.

Q-BUS

GRAPHICS

From Andromeda



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James C. Greeson, of the IBM Corp (Armonk, NY), highlighted some aspects of the guidelines and regulations that address the reported stress problems in the workplace.

It is generally recognized that four factors contribute to stress from constantly viewing a visual display unit (VDU): the workplace, the equipment, the task and the user. Mr. Greeson is disturbed with the current checklists and regulations which focus exclusively on the hardware subset of the problem. This, he feels, excludes new technologies and new applications of existing technologies which may offer a chance to restructure the actual task involved, directly attacking the stress problem.

Parameters discussed in ergonomic studies usually include character size, luminance and the amount of jitter from a VDU, according to Greeson. One regulation for character size stipulates that characters should not be used if the height of the capital letters without diacritics is less than 2.6 mm for the display. This is done without regard to resolution. Mr. Greeson points out that no similar regulation exists for the print media.

In a study by members of the Ergonomics Technology Foundation of the EE Dept of the Twente University of Technology (Enschede, Netherlands), a device that studies visual sensitivity of workers in their work environment was developed. The principle of the video display eye tests is that the subject has to recognize randomly chosen characters on a variety of backgrounds. The intensity of the characters is increased step by step. The level of intensity at which the character is recognized is then measured. Three vision qualities are tested: contrast resolution, spatial resolution and temporal resolution. Measurements were made before and after demanding visual tasks which had to be performed for three consecutive hours. Information was changed on the screen every 15s and the same information was also presented on a hard-copy output. The result suggested that no specific fatigue symptoms could be attributed to viewing the VDU as opposed to seeing the same material on printed copy for the same amount and frequency of time.

While the ergonomic effects of visual displays must be resolved, it remains an unequivocal fact that the market for all kinds of visual displays is very healthy. Stanford Resources (San Jose, CA), estimates that the total worldwide market for all electronic displays in 1981 was $5.484 billion, up 3% from 1980. The market is expected to grow to $5.889 billion in 1982, an increase of 6.8% (**Table 1**). □

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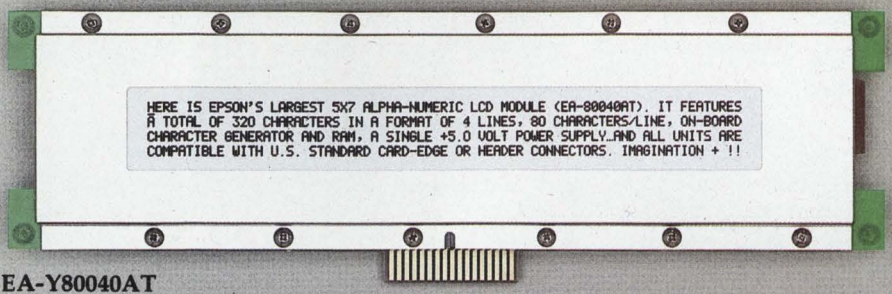
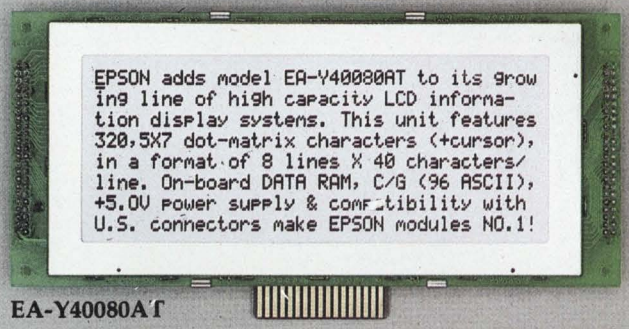
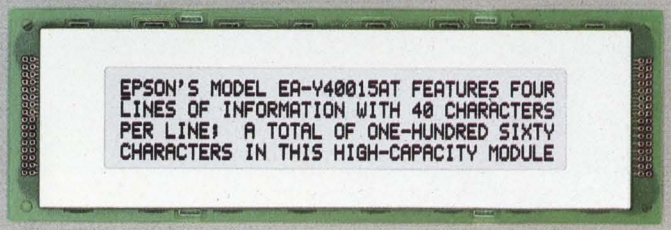


EA-Y80040AT



EA-Y40080AT



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Applications

- Hand-held Terminals (portable)
- Computer Terminals
- Word Processors/Typewriters
- POS Terminals
- Instrumentation
- Telecommunications
- Games/Toys

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EG-Y84320AT

EA-Y20080AT

EA SERIES

Model Number	*Character Format (characters × lines)*	*Character Size (with cursor)*	*Effective Viewing Area*	*Module Size (W × H × D)*
EA-Y16015AZ	16 × 1	2.9 × 4.8 (6.2)	62 × 20	84 × 44 × 14.2
EA-Y16025AZ	16 × 2	2.9 × 4.1 (5.3)	62 × 20	84 × 44 × 14.2
EA-Y20015AZ	20 × 1	3.4 × 5.15 (6.65)	88.2 × 20	125 × 44 × 14.2
EA-Y20025AZ	20 × 2	3.4 × 5.15 (6.65)	88.2 × 20	125 × 44 × 14.2
EA-Y20080AT	20 × 8	3.0 × 4.8 (6.2)	84 × 64	140 × 95 × 19.2
EA-Y24015AZ	24 × 1	2.9 × 4.45 (5.75)	93 × 20	125 × 44 × 14.2
EA-Y40015AT	40 × 1	3.0 × 4.8 (6.2)	156 × 20	192 × 45 × 14.2
EA-Y40025AT	40 × 2	3.0 × 4.8 (6.2)	156 × 20	192 × 45 × 14.2
EA-Y40040AT	40 × 4	3.0 × 4.8 (6.2)	156 × 34	200 × 71 × 25.4
EA-Y40080AT	40 × 8	3.0 × 4.8 (6.2)	157 × 63	205 × 93 × 19.2
EA-Y80015AT	80 × 1	2.1 × 3.38 (4.32)	212 × 18	264 × 53 × 20.7
EA-Y80025AT	80 × 2	2.1 × 3.38 (4.32)	212 × 18	264 × 53 × 20.7
EA-Y80040AT	80 × 4	2.1 × 3.38 (4.32)	212 × 28	293 × 80 × 31.0

EG SERIES

Model Number	*Dot Format (column × row)*	*Dot Size*	*Effective Viewing Area*	*Module Size (W × H × D)*
EG-Y84320AT	84 × 32	0.75 × 0.75	76.3 × 33	132 × 60 × 15.7

Unit: mm

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Wescon '82: The Word Is 16-Bits

This year's Wescon will introduce a wide range of peripheral chips and software for several new families of μPs.

by David Wilson

Expecting to draw more than 70,000 attendees, setting an all time record for the three-day event, the Wescon show still remains one of the highlights on the engineering calendar.

Reacting to the increasing market penetration of computers into more conventional industry, Wescon '82 will have special exhibits on robotics technology. Some of the exhibitors include IBM, Microbot, Quad Systems, LTI Robotic Systems and United States Robotics.

Relevant to this issue, on September 15, a workshop on marketing electronics to the "non electronic" customer base will be given to help manufacturers recognize and prepare for the emerging growth in this market.

This year, a companion event to Wescon will be introduced in Anaheim. Mini-Micro-82 Computer Conference and Exhibition will run concurrently with Wescon, Tuesday through Thursday at the Disneyland Hotel, a few blocks from the Anaheim Convention Center. Mini-Micro is expected to draw an audience of 25,000 who buy or specify products or services.

Microprocessors

The agreement made earlier this year between Motorola, Signetics and Mostek to support the 68000 family will be discussed in terms of the new products each company has developed. For Motorola, John Stockton will outline how the company aims to address two new markets by introducing low and high end processors.

The 68008 will be architecturally

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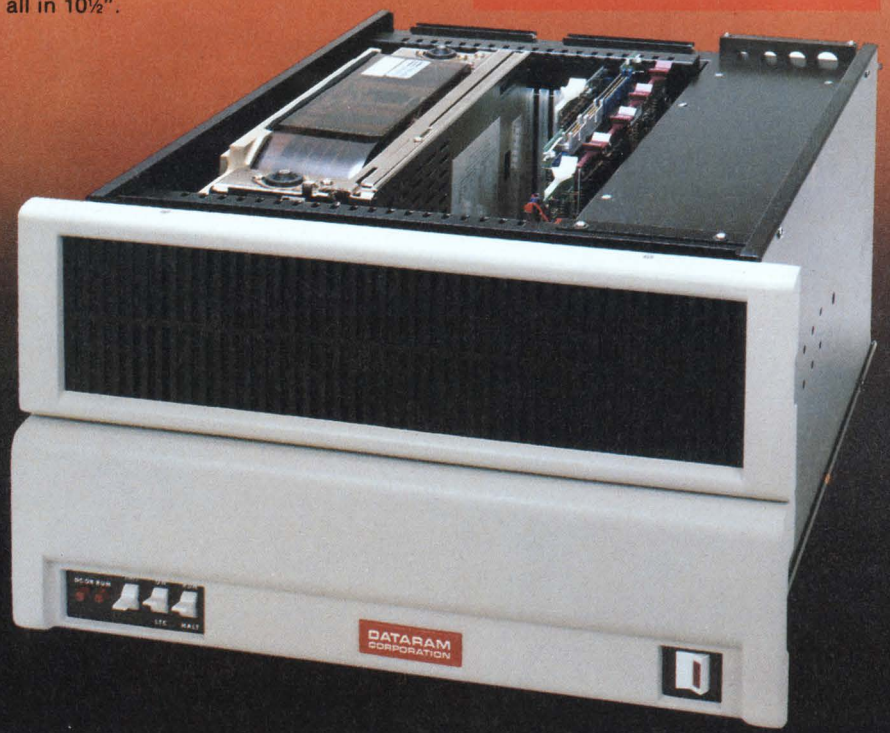

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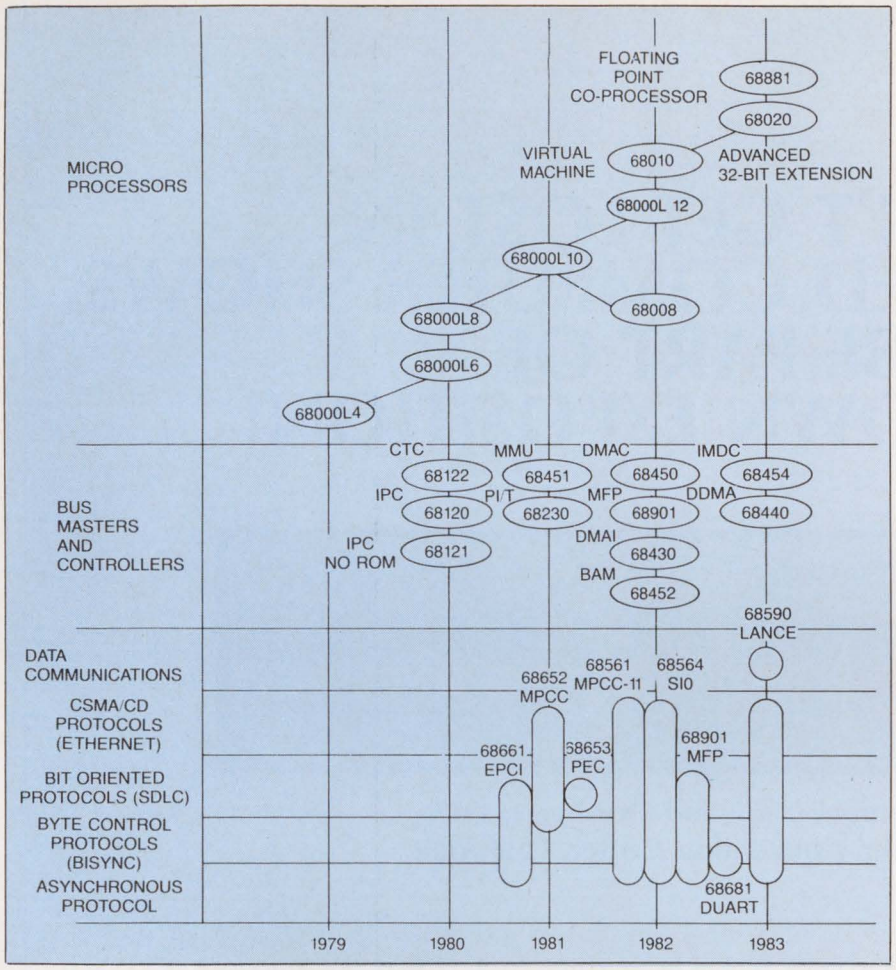

Figure 1: µPs, Bus Masters and data communications devices for the 68000.

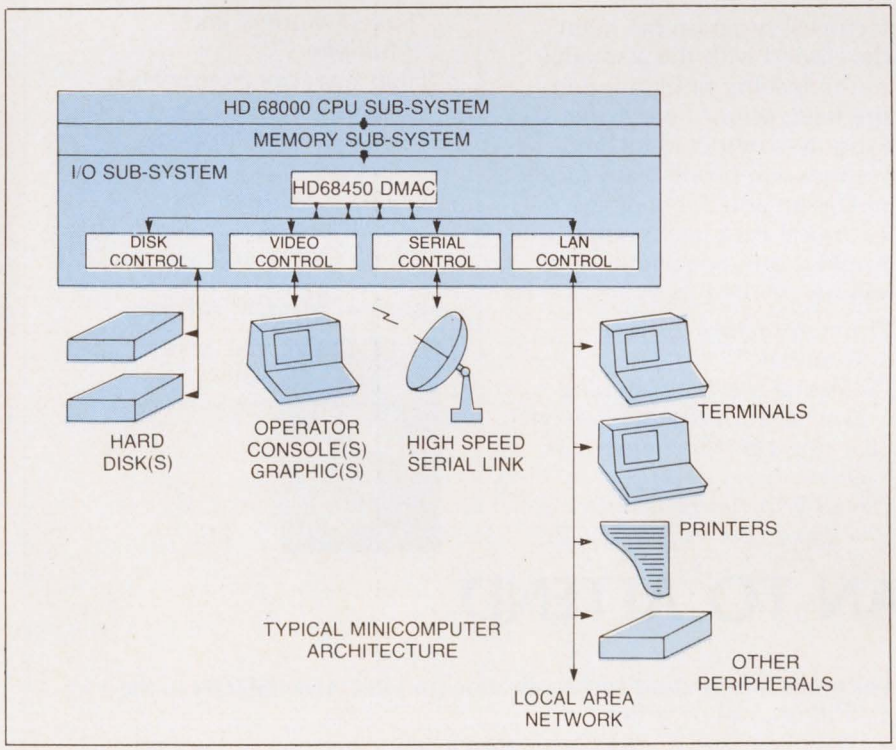

Figure 2: Functional block diagram illustrating the use of the HD68450 DMAC.

compatible with the 68000, as well as offering object code compatibility, so programs that were written to run on an entry level system will be able to be ported over to the MC68008 without any change. This establishes the bottom end of the processor family.

The next step in the evolution of the family will be the introduction of the MC68010 virtual machine. This version, similiar to the others, is also object code compatible and architecturally compatible with the MC68000 machine.

One advantage of the virtual machine is that it can be used in demand paged environments. Additionally, multiple operating systems can run concurrently on the same host processor.

Until recently, it has not been possible for a µP-based system to take advantage of demand paging schemes, so that if a large program were to be run that potentially exceeded the address space of the machine, the programmer had to plan for this and arrange the program as a series of overlays, each being resident only as a portion of the total time. This placed a large burden on the programmer.

The 68010 virtual memory machine will allow programs that exceed the address space of the basic machine to run without the conscious intervention of the applications programmer. This feature will allow systems based on the 68010 to offer features of mainframes at a lower cost, according to Stockton.

The next step upward beyond the virtual machine is the 68020, a 32-bit data bus version of the 68000, that allows programs written for the 68000 to run between 2 and 4 times faster.

Figure 1 shows the family tree of the 68000 family with respect to performance and introduction date.

The Motorola marketing manager may be interested to note a comment overheard at the recent NCC from a graphics terminal designer. He remarked that irrespective of whether his next-generation product could utilize all the capabilities of a 16-bit machine, if it did not have one it would be a lot more difficult to sell.

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Peripherals Too

Already, many of the peripheral circuits for the 68000 are now in high volume production including parallel I/O and timers (68230 PI/T), intelligent controllers (68120 IPC and 68122 cluster terminal controller), memory management (68451 MMU), communications controllers (68652 and 68661) and a bus arbiter (68452). **(Figure 1)**

Additional members of the family have already been defined by the major suppliers. Four of these new devices, to be formally introduced between late 1982 to late 1983 will include the 68200 intelligent control processor, 68450 DMA controller, the 68561 Multi Protocol Communications controller and the 68562 dual universal serial communications controller.

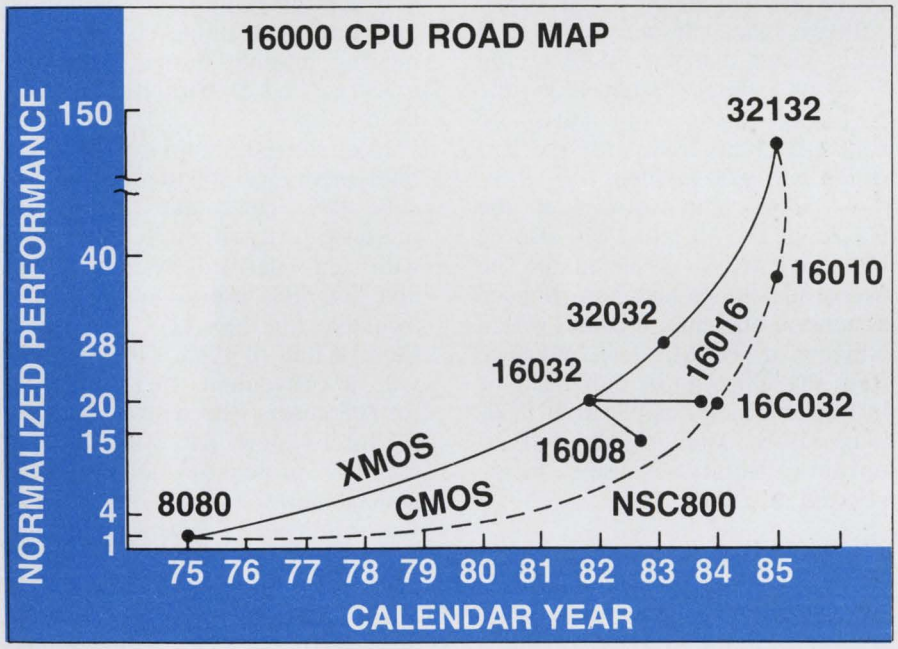

Figure 3: NSC16000 CPU Road Map.

DMA Controller

For Hitachi America, Thomas Cantrell will describe one of the new peripherals for the family - the HD68450/direct memory access controller.

Essentially, a Direct Memory Access Controller is a processing unit for a special class of applications, namely that of moving data within and between system memory and peripheral devices. Peripheral devices which are often interfaced **(Figure 2)** using DMA include disk storage (flexible and rigid), tape storage, video interfaces, CRTs, printers and other data comm devices (i.e. local area networks, IEEE-488, UARTs, etc.).

Like a general purpose CPU (i.e. HD68000), a DMAC acquires use of the system bus, exerting control over the existing data, address and status/control lines.

Once in control, the DMAC in effect executes a short program which accomplishes the high speed data transfer. In this regard, there are two extremes to be considered.

In older DMAC designs, the data transfer 'program' is implemented in hardware. In this case, the main CPU is burdened with the task of initializing the DMAC with every parameter for each transfer.

At the other extreme, the DMAC is no different than a general purpose CPU. The DMAC is responsible for accessing and executing an external data transfer program as well as fetching and storing the data to be transferred. The problems with this approach include making the programmer responsible for all low level control of the data transfer, and significantly reduced performance due to the replacement of dedicated hardware with software.

The HD68450 lies between these extremes, incorporating a fairly high level of intelligence to reduce main CPU overhead, while retaining dedicated hardware to accomplish the data transfer at the highest possible speed.

Road Map

The National Semiconductor 16-bit family approach appears similar to that of Motorola, with an initial offering of 3 products (the 16032, 16008, and the 16016).

At Wescon, Geoffrey Kates from National will point out the directions the company is taking using the 16000 CPU Road Map **(Figure 3)**.

With a full 32-bit architecture, 32-bit registers, data paths and ALU, the 16032 has the ability to support the aborting of any instruction and then retrying it—an essential feature in any virtual memory scheme.

The NS16008, an 8-bit data bus version of the NS16032, is being introduced for users who wish to build low cost 8-bit systems. It is totally software compatible with the NS16032, still retaining the 16 Mbyte addressing range. The only difference between the NS16008 and NS16032, besides the 8-bit data bus, is that the NS16008 does not support virtual memory. The performance of this device is typically 75% of the throughput of the NS16032. The only difference in pinout is that only the bottom 8 lines are now multiplexed, and the NBE signal is not present anymore. Like the NS16032, it comes in a 48 pin package.

For users with a large investment in 8080 software, the NS16016 provides an easy upgrade path. This part is software compatible with the rest of the NS16000 family. The only difference between the NS16016 and the NS16032 is a software switch (consisting of two simple one byte instructions) that allows the user to switch between his original 8080 code and his newly written NS16000 based code; and vice versa. A user can move his

Part Number	Function	Availability
Z8010	Memory Management Unit (MMU)	NOW
Z8015	Paged Memory Management Unit (PMMU)	3Q82
Z8016	DMA Transfer Controller (DTC)	NOW
Z8030	Serial Communications Controller (SCC)	NOW
Z8031	Asynchronous Serial Communications Controller (ASCC)	NOW
Z8036	Counter/Timer and Parallel I/O (CIO)	NOW
Z8038	FIFO Input/Output Interface (FIO)	NOW
Z8060	FIFO Buffer and FIO Expander (FIFO)	NOW
Z8065	Burst Error Processor (BEP)	NOW
Z8068	Data Ciphering Processor (DCP)	NOW
Z8090	Universal Peripheral Controller (UPC)	NOW
Z8070	Arithmetic Processing Unit (APU)	1Q83
Z8052	CRT Controller (CRTC)	1Q83
Z8581	Clock Generator and Controller (CGC)	1Q83

Figure 4: Z8000 Peripheral Components.

8080 over to the NS16016, expand his program and/or optimize the speed critical path in native (NS16000) code.

The approach of moving the original 8080 code over and then adding extra features in NS16000 based code is the approach used by Digital Research in their implementation of concurrent CP/M on the NS16016. They have taken their original version of CP/M, written to run on the 8080, moved it over to the NS16016, and are writing the concurrent features in NS16000 based code. The 8080 portions of the program will run 4 times faster on the NS16016 while the concurrent features will run 20 times faster than if they had been run on an 8080. This 8080 compatibility will enable numerous application packages (all written in 8080 code) to run on NS16016 based systems.

National's first 32-bit part will be the NS32032. This features a 40% improvement in performance over the NS16032 primarily because of its 32-bit bus and the speeding up of certain key instructions. Multiprocessing features have been added. Because of the advanced 32-bit architecture, software compatibility has been maintained with the rest of the NS16000 family. It will come in a 68 pin chip carrier.

The first member of the NS16000 family to be built in CMOS will be the NS16C032, as will the generation of 32-bit CPU's after the NS32032, the NS32132. This CPU will have the Memory Management and Interrupt functions brought on board and will have a 32 bit virtual address space. It will be 3 to 4 times faster than the NS32032 and 5 to 10 times faster than the NS16032. Again both parts are software compatible with the rest of the NS16000 family.

A single chip version of the NS16032, the NS16010 will also be built in CMOS. Designed for the user who wants a high performance system on one chip, it comes with 8 Kbytes of RAM. The interface from this chip can be either I/O or bus oriented, for application flexibility. Both counter/timer and interrupt capability will also be incorporated on-chip.

Z8000 Extras

As of April 1982, Zilog announced an additional second source in Japan: Toshiba will second source the Z8000 in exchange for bringing CMOS technology to Zilog. Plans have been announced for a CMOS part, according to Tom Cramer, Z8000 support manager.

A comprehensive set of peripheral support components were developed specifically for use with the Z8000 CPUs. **Figure 4** gives a list of these products together with the availability dates.

Software

From the Intel camp, there will, no doubt, be a discussion of the recent tie up with Microsoft of Bellevue, Washington to make the Xenix operating system available for Intel's entire range of iAPX86 family of processors.

Intel is supplying prototype hardware and engineering support to assist Microsoft in configuring the iAPX 286 implementation of the operating system and validating its performance.

Xenix operating system implementations for iAPX 86 family members will be marketed by Intel under an agreement with Microsoft. In addition, Intel introduced a Xenix version of the System 86/330 at the NCC in Houston.

The Xenix operating system is Microsoft's 16-bit μP adaption of Bell Lab's Version 7 UNIX system. It is best suited for programs that require terminal-based interaction between the system and the human operators performing tasks in engineering, graphics design, word processing and business data processing.

Intel started shipping the Xenix implementation for the iAPX 86 in July 1982. This makes the wealth of software traditionally associated with Unix-derived systems available for 8086 users. Xenix will be available for the iAPX 286 during the first half of 1983. This will provide a convenient migration path for 8086 users who wish to upgrade to Intel's new μP with on-chip memory protection and memory management.

In addition to performance advantages, the iAPX 286's hardware memory protection isolates each user's memory area from being overwritten by other tasks. It has four levels of privilege for tasks needing different levels of systems access (i.e. operating system kernal, systems, services, application services and applications).

The iAPX 286 also offers the Xenix operating system the advantage of hardware-supported virtual memory management. Since Xenix may have a large number of users running a large number of tasks at any given time, steps need to be taken to assure the efficient and timely allocation of memory resources to each task. □

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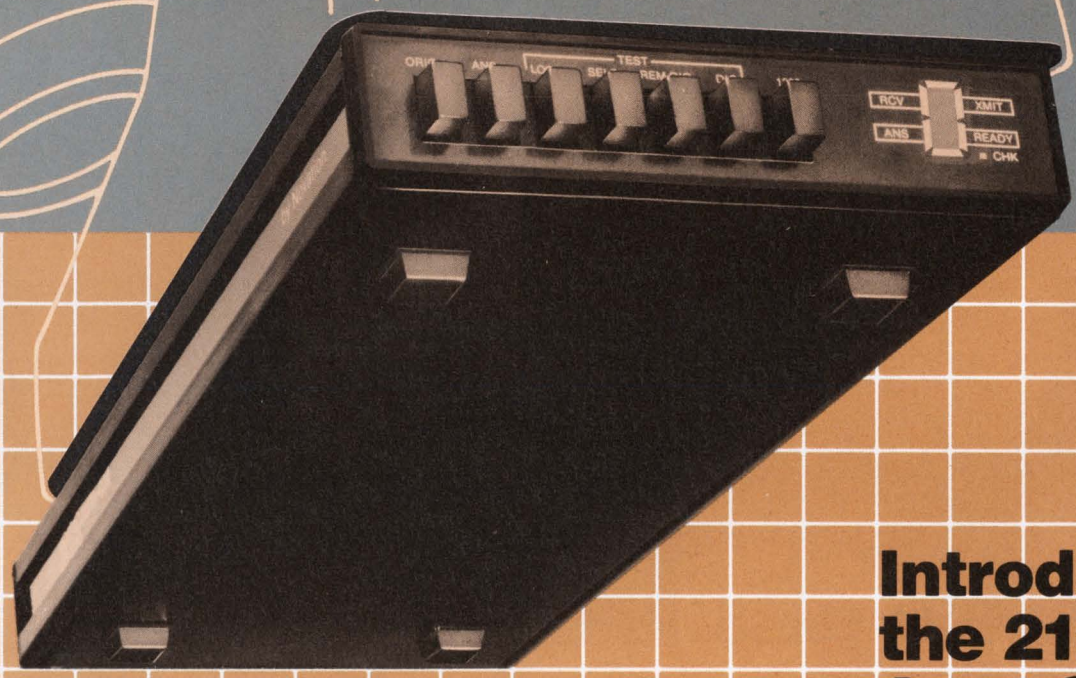

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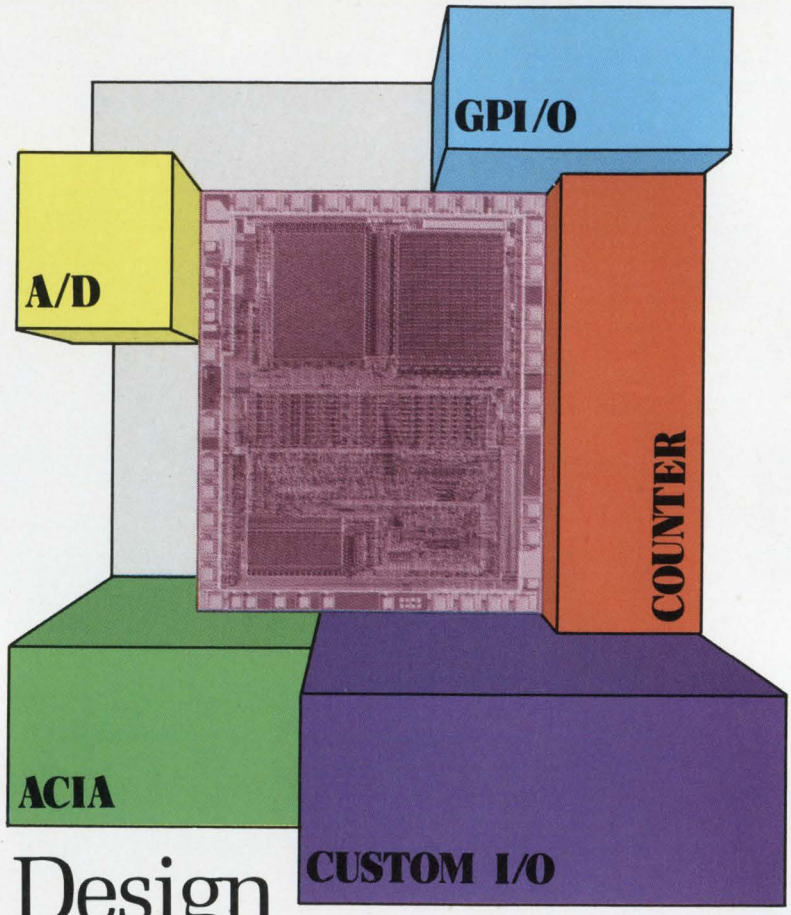
The alterable μC is a new concept in device design. The basic structure of the chip is altered to meet a specific application.



Alterable μCs: Tailoring Chip Design To Meet Applications

by Jerry Randal Bauer

Alterability, as applied to an alterable μC, means that the device is designed to tolerate modifications to its basic elements. These modifications are specified for a given finished device, and the device is constructed. An alterable μC is alterable only while it is being designed, not after manufacture, except as the design may allow programmable configuration. The following sections explore alterations to each of the subunits, the I/O, the memory, and the CPU.

I/O Modifications

The Input/Output, because it is the interface between the processing power of the CPU and the application, is the part of a monolithic μC most subject to alteration. Standard monolithic μCs provide general purpose I/O capabilities in order to be competitive in a wide market. An alterable μC is expected to be customized to the requirements of the application, so there is no reason for I/O to be general; rather, it is advantageous for the I/O to specifically suit its function. To this end, adaptations of the I/O are conceptually unlimited although there are practical limitations. Methods of handling this freedom are incorporated into the design of an alterable μC.

Implications of I/O Modifications

Some of the considerations of modifications to the I/O are silicon area (cost), I/O information transfer bandwidth, and system throughput. Usually, a function implemented in hardware is faster and larger than the same function done in software. If system (or subsystem) speed is the more important factor, hardware is the indicated solution, otherwise software is. If a software driven I/O function is a system throughput bottleneck, then an alteration of that I/O function which makes it more independent (stand-alone) can improve system performance. An important point is that software occupies area (in ROM), so the compromise between an independent I/O subsystem and a software-driven I/O function is based on relative speed versus the difference in area.

There are functions which can not be implemented well, or with any significant savings, in software. Examples are: Digital-to-Analog

Jerry Randal Bauer is with American Microsystems, Inc., 3800 Homestead Road, Santa Clara, CA 95051.

converters, real-time analog processing, and audio filters. These, if needed, are best implemented as stand-alone I/O subsystems.

Memory Modifications

Within the addressing limitations of the CPU, modifications to the memory are quite reasonable. There is no compelling reason why a monolithic μC in a given application should bear more RAM or ROM than the application demands. Unused memory is wasted area (money). Also, it may be advantageous to remove all or part of the memory from the μC. Many monolithic μCs are so heavily I/O oriented that it is not possible to access the address or data buses for memory expansion. Those μCs that are capable of expansion demultiplex the address and data buses from the I/O signals with external components, increasing system complexity and cost. One possible memory modification is to include, as part of an alterable μC, external memory interface circuitry.

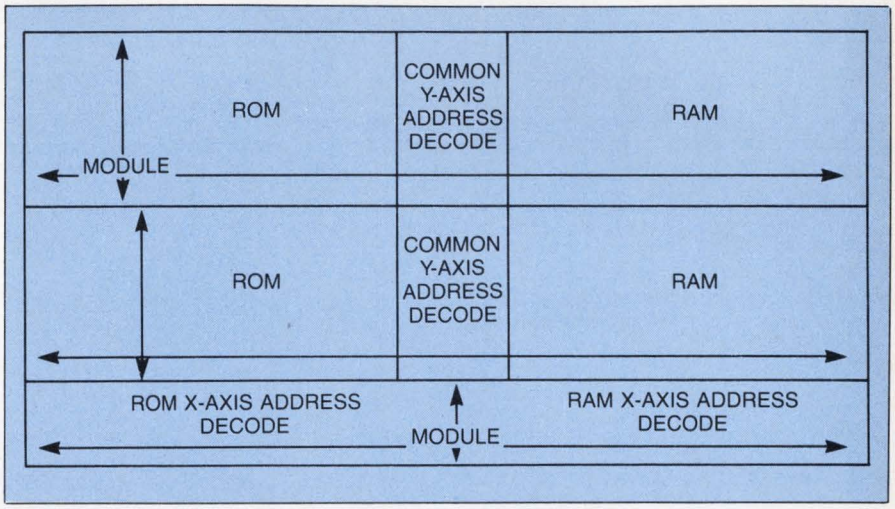


Figure 1: When ROM and RAM share a common address decode, the ratio of ROM to RAM is fixed by the topography. This ratio is maintained in the available memory modules (two are shown here). The x-axis DECODES are also a module.

The physical layout of the memory structure may make it inconvenient to add or delete memory to reach the desired amount. Memory may be more efficiently handled in groups of powers of two, such as 512 bits, bytes, or words. A static RAM element is about sixteen

Microprocessors: The Core Approach

Despite the proliferation of standard μPs, many application requirements fall into capability gaps that exist between off-the-shelf devices. In these cases, systems designers must either use additional chips to boost the performance of a weak processor or pay for the unused performance of a more powerful device.

However, an advanced design concept recently introduced by ZyMOS Corporation (Sunnyvale, CA) extends the range of semicustom design to μC levels of system integration. The new concept centers around the addition of a CPU as an element in a standard cell library. Called a "core μP," the new cell is a general-purpose 4-bit module without memory or I/O ports. The only remaining design task is to add appropriate RAM, ROM, timers, counters and I/O modules to complete user-defined architecture of a customized μC chip.

Until now, the level of complexity in standard cell libraries was limited to small-scale and medium-scale IC modules of gates and flip-flops. Consequently, development costs increased significantly as chip complexity grew. However, a CPU module comprises a total of about 5000 transistors. Providing this level of integration in a single library cell gives designers a head start in solving complex systems problems with simple semicustom chip design.

CPU Architecture

The ZyMOS CMOS core μP is architecturally similar to the 8-bit MCS6502, and includes a 4-bit arithmetic logic unit (ALU), two 4-bit index registers, a 12-bit program counter and address circuits, an 8-bit stack pointer register and an

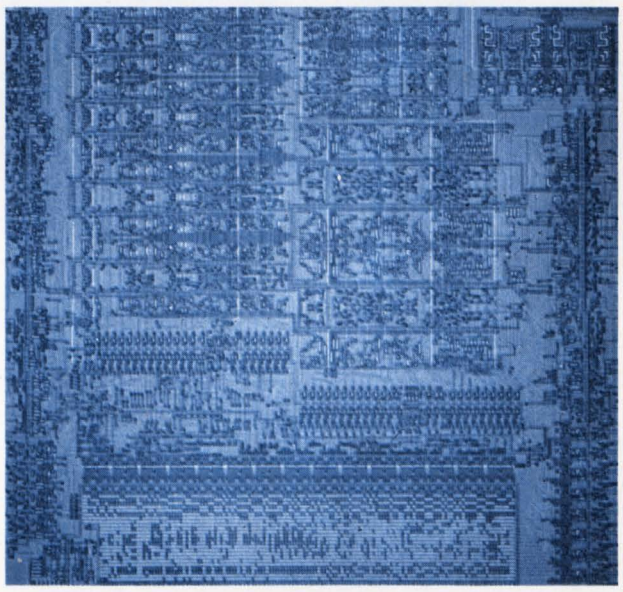


Figure 1: ZyMOS Corp's new "core μP" cell allows users to customize their own single-chip microcomputer. The new cell, designated ZyCOMP-4, is a general-purpose 4-bit μP without memory or I/O ports. By adding to the core processor appropriate memory cells, counters, timers and I/O ports from ZyMOS' ZyP design automation system library, users can quickly tailor the microcomputer chip to meet specific applications.

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8-bit instruction register with instruction decode circuits.

The CPU consists of 3 parts: the ALU, a control section and an address-generation section.

The ALU contains the arithmetic logic unit, four ALU registers and a flag (status) register. The ALU is basically a 4-bit adder-shifter. The X and Y registers are 4-bit index. Register A is a 4-bit accumulator, and register T is used for temporary storage. The 4-bit flag (status) register holds the carry, zero, negative and overflow flags.

The control section includes a micro-state counter, an instruction register and an instruction-state decode programmed logic array (PLA). The instruction register is made up of two 4-bit sections. These are loaded one at a time during the first two clock cycles of each instruction. After loading, the instruction determines the counter states and register control-line activation.

The address-generation section assembles and outputs the addresses required for instruction fetch (program pointer), for data fetch and store (data pointer), for stack push and pull (stack pointer) and for indirect address-register block selection (block pointer).

The CPU clock can be stopped by user-defined circuits sensing a predetermined signal or combination of signals. During this "sleep state," timers continue running and inputs continue to be sensed. However, the processor conserves power by not executing program instructions until a switch actuation or other event signal causes the clock to resume operation. This feature is useful in energy-sensitive applications requiring intensive but infrequent μC usage, such as in pacemakers or aerospace equipment.

Adding Memory

Memory module cells available for user-defined μC designs are all 4-bits wide. RAM cell options are 64, 128 and 256 x 4 bits. ROM cells can be 512, 1024 or 2048 x 4 bits.

The maximum amount of data or instruction memory that can be added to the core processor is 4 Kbytes, making a combined total of 8000 memory addresses—half for instructions and half for data. Each memory address selects a 4-bit nibble of data or instruction. Three mutually exclusive memory control lines (instruction read, data read and data write) determine which memory type is connected to the data bus during each machine cycle.

I/O and Linear Functions

Using latches and pad drivers in the cell library, the designer can customize a variety of I/O ports, such as serial, unidirectional, bidirectional, edge-detecting, and parallel-load serial shift. Similarly, the variety of timer designs possible include adjustable prescale divider (for clocking other items), count-up, count-down, load-only and read/write timers.

Instruction Set

Many benefits of the core-processor reside in the instruction set, which is similar to that of the 6502 8-bit μP. Although there are 256 instruction codes, most are addressing mode variations of a few basic operations.

There are three basic types of addressing modes: implied, memory reference and program control. The first three cycles of all modes are identical. The first two cycles of each instruction fetch the instruction opcode. The third cycle is used for opcode decoding and for fetching a third instruction nibble which may or may not be used. The core processor architecture and its instruction set combine to provide several features usually found only in 8-bit machines.

Designing The μC

Full-service custom houses contribute to all phases of chip design from system concept through prototype delivery. However, those such as ZyMOS with fabrication facilities are interested primarily in processing silicon with minimum design involvement.

The absolute minimum customer input is a word description of system operation, including inputs, outputs and timing relationships. This lower entry level, however, increases engineering costs significantly.

The highest entry level is a chip network listing, which is a list of standard cells (including the core processor) and their interconnections. There are also many other possible entry levels between those described above which depend on the customer's design ability and desires. In any case the result of this design input to a computer is a network listing for automatic cell placement and interconnection. ZyMOS' design automation system, called ZyP, then converts this data to a chip layout drawing showing cell placement and routing patterns for mask tooling and prototype fabrication. The computer uses the same network to provide a logic simulation of the system. Design verification (and test) input patterns must then be created.

Finally, the computer generates the logic simulator output patterns and converts them into functional test parameters for an automatic tester. Thus the ZyP system executes all phases of the design cycle: circuit design simulation, logic design verification, tooling generation and test-program conversion. The customer needs no knowledge of device physics or topological design experience.

With the addition of an entire μP to a cell library, the usual tradeoffs between standard and full-custom designs no longer apply. Now one can have a minimal chip system solution without the cost and time of a full custom single chip μP.

Applications

The core processor is expected to find application in a variety of intelligent appliances, industrial and household controllers. One of the initial applications is in a smart home thermostat. This device has a keypad for inputting temperature setpoints for various times of the day. Temperature and time are displayed on an LCD indicator. In addition to using less power than existing devices, the core processor is expected to make the product easier to use.

Similar application potentials are not difficult to envision. Several controllers could be used in a distributed-thermostat, climatic control system that maintains different temperatures in several areas. Such multiple processor configurations might be fitted with a battery of sensors to control outside and inside lighting. Similarly, distributed process controllers could predict and avoid temperature overshoots and undershoots. Home control systems might also benefit from the use of a μC. For example, whistle (or clap) actuated equipment could be designed to recognize many different commands.

The core μP concept enriches the application potential of sequential logic machines by filling the performance gaps between standard single-chip μCs. And by eliminating a significant part of the development effort, this new approach invites more imaginative solutions to system design problems.

times the size (area) of a ROM element; if RAM and ROM share common addressing hardware then memory should be added or deleted in a ratio of 16 ROM elements to one RAM element. If memory is to reside off-chip then the characteristics of the proposed external memory must be considered in the design of the memory interface. In either case, the design of an alterable μC makes these modifications possible.

Other types of memory, like EPROM or EEPROM, require different considerations. To include EPROM or EEPROM, the manufacturing process must be able to support those types. This is not always (or usually) the case.

Modifications to a CPU that is not designed to be alterable are to be done only if the benefits greatly outweigh the risks.

If the memory is modified to include dynamic RAM (DRAM), refresh circuitry must be incorporated. Such circuitry is associated with the address decodes and memory timing. The refresh timing must be dovetailed with the internal timing of the CPU to achieve transparent refresh. Alternatively, minimal refresh hardware (the sense/refresh amplifiers) could be included and the actual refreshing done in software.

CPU Modifications

Although in the first generation alterable μC the central processing unit (CPU) is not modifiable, in the future this will not be the case. The CPU is potentially modifiable in several ways. Here, three ways are considered. First, it may be desirable to add instructions that implement often-used routines more efficiently, and/or to delete rarely used or inefficient instructions. The ability to alter the instruction set of the CPU can yield savings of silicon area (and expense) by reducing the amount of ROM needed to contain a given function. An altered instruction set might also improve system effectiveness; by allowing faster execution, dedicated speed-enhancing hardware may be eliminated. Instruction set changes are essentially modifications to the system control mechanism.

Secondly, the bit-width of the CPU might be altered. Silicon area can be reduced when data path widths are smaller, and system throughout can be increased when they are wider. Changes to the bit-width can be accommodated without altering the instruction set if they are implemented by multiplexing (or de-multiplexing) the data paths. These changes would require modifications to the system control mechanism.

The third possible change to the CPU is to alter the number of working registers. This would be done to include only those registers needed to perform the desired functions. A decrease in the number of working registers may not entail any change to the system control mechanism, but merely the excluding of unnecessary registers and associated support circuitry. Addition of new registers would require changes to that mechanism. An alterable μC that would tolerate modifications to the CPU is certainly possible, and likely to appear in the future.

Implications Of CPU Modifications

The standard CPU is a well tested, proven component. The complexity of such a device raises it well above the trivial, and any changes to it have the potential of upsetting a delicate structure. In this respect, modifications to a CPU that is not designed to be alterable are to be done only if the benefits greatly outweigh the risks.

Generic Alterable μC

A generic alterable μC is a basic structure that can be altered to customer specifications. As such, it must be a blend of rigid (not easily changed) support circuitry and

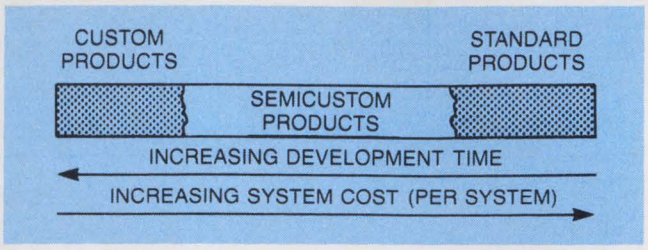

Figure 2: Semicustom products include alterable μCs, gate arrays, programmable logic arrays (PLAs), and even ROMs. They allow flexibility in the customer/vendor relationship by allowing the vendor to offer a wide range of options between general-use standard products immediately available and dedicated, highly specific custom products requiring a long design time. The customer can optimize his investment by choosing the appropriate solution.

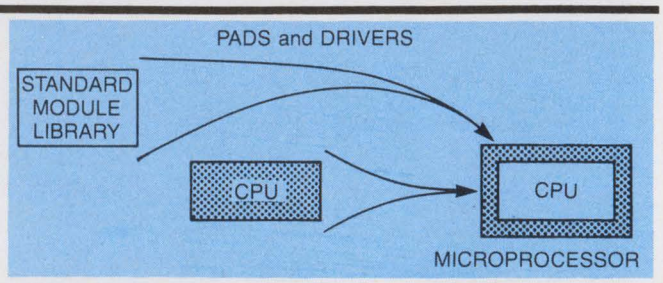

Figure 3: An alterable μC with pads and drivers from the standard module library, is a μP. In the case of the first-generation alterable μC, the corresponding is a 16 bit (9900 type) CMOS device. Because it was designed for silicon efficiency and processing power, it is competitive in the market in its own right.

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AMU Design Sequence

Two intital options are availble to the AMU user. First, AMI can be assigned the full design task. Second the user may design and control his own chip design.

Either approach requires the user to write his own AMU software. To prepare the software, the user needs these items:

(1) — Access to an editor and S9900 assembler, i.e. time share, a personal computer plus a S9900 assembler or a Millennium 9250 plus S9900 assembler. (The Millennium 9250 system costs about $8.5K, $1.5K for the terminal and $1.5K for a PROM burner.)
(2) — Millenium 9508 Emulator (approx. $5K)
(3) — 9508 AMU personality card and pod (approx. $1.5K)
(4) — Amulator(s) at $300 each

If the user provides his own hardware for AMU software, and his hardware has an RS-232 port, he needs only purchase the Emulator and the Amulator. Also, the user needs to have the capability to burn EPROMS in order to perform stand-alone emulation using only the Amulator.

flexible (readily adaptable) customer definable interface. This blend, once defined, must serve a wide variety of unforeseen future alterations.

An alterable μC might be used in three kinds of application:
(1) to replace an existing monolithic μC to enhance the end product
(2) to replace a multilithic μC or system, reducing costs or increasing reliability
(3) to make possible the design of a product which could not be realized with any other technique.

The following performance objectives emerged from analysis of the potential applications:
(1) low supply current, for battery-powered applications
(2) a powerful instruction set with an architecture of at least 8 bits
(3) a flexible I/O handling mechanism for easy alterability
(4) conservative design and process, to function well in harsh environments

Design Considerations

As is often the case, many of the technical decisions that had to be made were closely interwoven with each other. For clarity here, they are separated into: (1) the choice of CPU, (2) the choice of process technology, and (3) implementation of alterability.

Choice Of CPU

What is the best CPU for an alterable μC? The designers of AMI's alterable μC (AMU) investigated the applicability of existing CPUs of many types before choosing the 9900 type of CPU as the best suited.

The characteristics of this CPU include:
(1) The working registers reside in memory so adding or deleting working registers is the same as adding or deleting RAM.
(2) It has a very efficient I/O manipulation mechanism, the Communications Register Unit (CRU). I/O may also be memory mapped.
(3) It has a powerful minicomputer-like instruction set, including multiply and divide.
(4) It has a 16-bit architecture.

Process Technology

A dual-polysilicon CMOS process was chosen for the AMU because:
(1) CMOS provides the desired (low) power consumption and environmental tolerance.
(2) A dual-polysilicon process gives high density and reduced silicon area.
(3) CMOS is a proven high-performance technology.

Implementation Of Alterability

The essential task in the design of an alterable μC is how to make it alterable. Members of the design team had "customized" standard μCs and knew the problems of the "ECO" (Engineering Change Order) approach. These problems include nonstandard documentation and design techniques that may expedite production of the initial runs of the modified part, but complicate production, product improvement efforts, and subsequent "customization" efforts. The AMU team opted for a more structured approach which shares the philosophy of "standard cell" design.

In conventional "standard cell" design, the designer chooses from a library of existing functions and integrates them into a monolithic circuit. This method has the advantages of reduced design time and increased design reliability. The

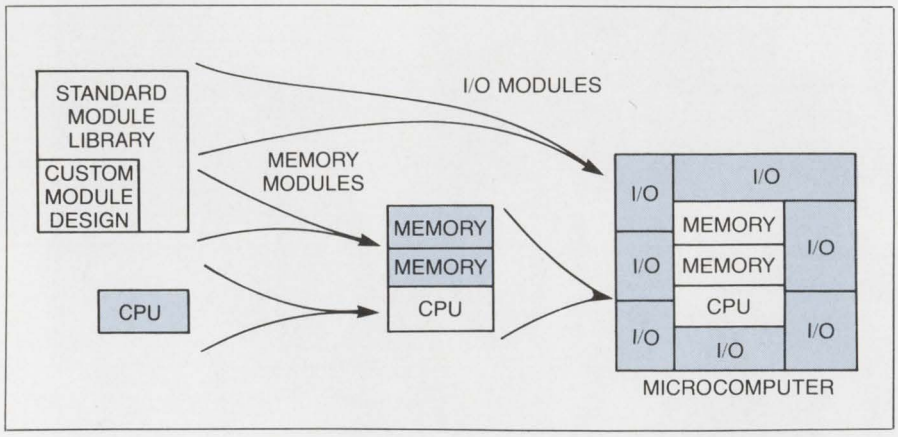
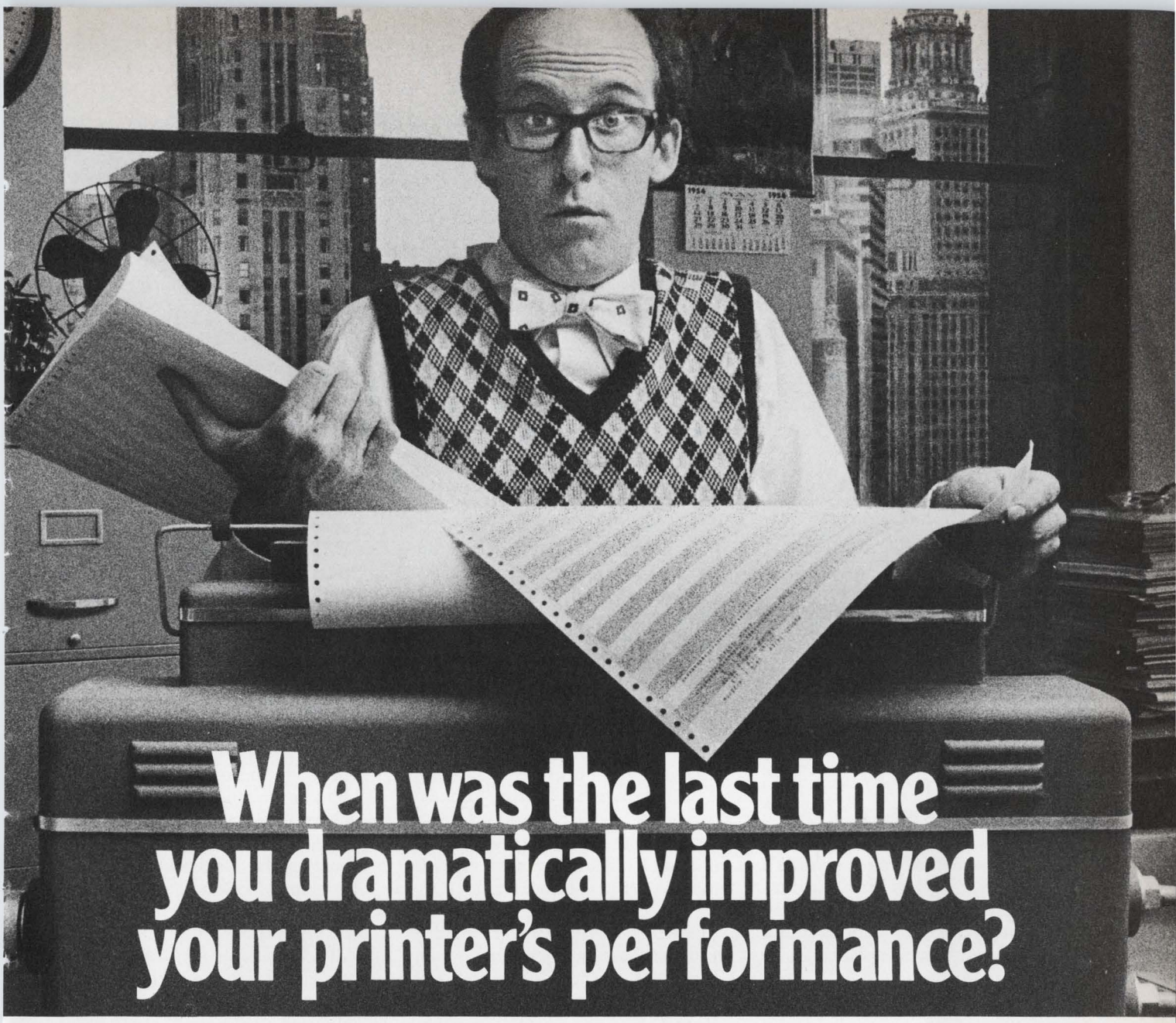


Figure 4: A custom alterable μC is made of modules. Modules may be used intact from the library, may be modified from standard library modules, or may be custom designed and placed in the library. In this illustration, memory and I/O modules are attached to the CPU to make a custom μC.



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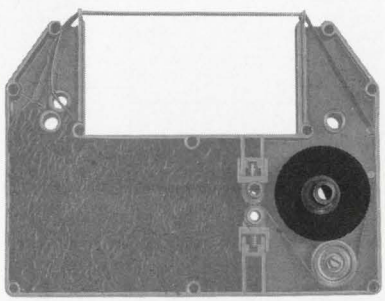

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Typical AMU Design Cost

AMI prepared this example of the design costs for an alterable μC chip. The device selected is designated the S99C50, and it will become a standard monolithic μC. The cost shown and the time are for ballpark estimates only. Every design will have a different price based on complexity and many other factors—but this is to show what it might cost. AMI should be contacted for specific pricing information.

AMU Design—Type S99C50
- 2K ROM
- 128 Bytes RAM
- Dual Modulus 16-Bit Computer
- 32 General Purpose I/O pins

- Design Cost—$35,000
- Turnaround—24 weeks

Volume Pricing for this Device (estimated)
- $45 ea. for 1000 devices
- $15 ea. in high volume

disadvantages of conventional "standard cell" design are that circuits designed with "standard cells" consume more silicon area than entirely custom designed circuits, and the designer is limited to functions available in the library.

The designers sought to eliminate the disadvantages of the conventional "standard cell" approach while retaining its virtues. Certain compromises had to be made. This is the result:

(1) There exists a library of system components, called modules. A module is one or more "cells" grouped together as a functional unit. Modules may be separately packaged for system evaluations before committing to the design of a custom alterable μC.

(2) Each custom AMU is composed of modules.

(3) The CPU is a standard (not alterable) "cell" (module), used as the "core" of the alterable μC. Modules are attached around this core much the same way that standard cells are interconnected.

(4) Modules may be used intact from a library, may be modified from library modules, or may be custom designed.

(5) Memory is available as library modules, or may be custom configured.

(6) Newly designed modules are added to the library.

This "modular" approach preserves the virtues of rapid, accurate design from the conventional "standard cell" discipline and adds the flexibility of custom design.

Technological Considerations

For the first-time designer of a custom AMU, the effort may seem very simple or very complicated. Both views are correct, for while the concept is simple, there are pitfalls in the execution which can be avoided with appropriate assistance. Assistance is available from AMI in several forms, including training seminars, full documentation, extensive development systems, and one-on-one applications support.

A custom AMU design can be viewed as the conversion of a set of related library functions to a single structure. This simplicity is the result of a conscientious design effort, yet there are three areas of concern to the AMU system designer. AMI offers assistance to the AMU system designer in each of these areas; electrical, logical, and topological system considerations.

Electrical Considerations

All components of the system must be electrically compatible, i.e. outputs of one subsystem must be capable of driving inputs of another subsystem, with appropriate margins. In the standard library modules, this requirement was met by the original design specification. If the module is being used in a nonstandard way, has been modified, or is placed in a different system environment, the electrical interface should be scrutinized for compatibility and altered where necessary.

The CMOS process used for the AMU is capable of implementation of sophisticated analog subsystems, such as switched capacitor filters and Analog-to-Digital converters. A system designer using these capabilities should consider system noise effects on the performance of the system. These effects can be reduced if they are recognized and considered.

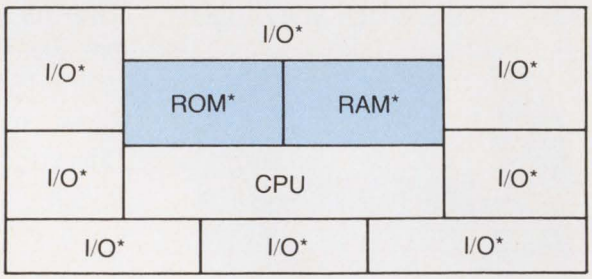

Figure 5: A modified "standard cell" design approach allows the system designer to configure an alterable μC to the application. In this drawing, all portions of the system marked with an asterisk (*) are drawn from the standard module library or are custom configured. Only the CPU selection is fixed, and this restriction will undoubtedly disappear in the future.

Designers Guide To The IEEE-488 Bus – Part 2

If instruments can handle their own processing, this may raise system speed.

In Part 2 of our series related to the subject of busses, Contributing Editor Paul Snigier continues his discussion of the IEEE-488 bus.

by Paul Snigier

In the June issue of **Digital Design**, the basics of the GPIB or IEEE-488 and the HPIL were covered. This month—in the second half of the GPIB series—we will examine problems and implementation guidelines.

IEEE-488, operating in one of its three modes—as listener, talker or controller—permits only one bus controller or talker to be active at a given instant. Up to 14 devices are interconnected on one 24-wire bus, and each is assigned a unique address, so that the controller can address as many listeners as needed.

Devices terminate lines with 3KΩ pull-up and 6.2KΩ pull-down resistors, thus providing uniform line impedance and improving noise immunity. Total cable length must be under 2m times the number of devices, up to a maximum of 20m. Exceeding this can produce timing variations and unreliable operation—unless a fiber optic link is used.

Distance Is No Problem

If a high-speed fiber optic link (FOL) is used, locating 488-compatible devices over 100m away is possible. Due to its noise immunity and isolation, a dual-channel FOL can transfer data bidirectionally between distant sites. Although data rates can exceed 20 Kbytes/s, fiber optic cable (FOC) does attenuate higher frequencies differently.

Since users may want to locate computers in one area and instruments in another, with the distance often exceeding 20m, the FOL is the solution, especially where the environments are often electromagnetically noisy.

However, FOL dual-channel systems are expensive. Units are needed to accept byte-parallel signals and convert them to bit-serial light pulses, and to also reconvert them back into bit-parallel form.

Signal Lines

Negative-logic, TTL-level signals are placed into three groups. The eight bidirectional data lines carry addresses, data or commands. The interface management lines include ATN (attention); if the controller pulls it LOW, it indicates all data line information is an interface address or command. IFC (interface clear) resets all interfaces to a known quiescent state and is initiated by the system controller; SRQ (service request), an interrupt line, is activated LOW by any bus device requesting service. REN (remote enable) is activated HIGH by the controller, allowing remote control. In an instrument device, this allows front panel control. EOI (end or identify) indicates the end of a multiple-byte message-transfer sequence and is asserted by the talker. Or, a controller can use it as a command to tell a device to identify itself after it sent a SRQ. At this, the SRQ-generating device places its own unique address on the bus during the polling sequence.

The third group, the byte-transfer-control lines, make up the three-wire handshake process, utilizing interlocking command sequences to transfer each data byte across the interface. These three sequences proceed at the rate set by the slowest bus device to ensure that all assimilate the data. When the talker forces DAV (data valid) LOW, this indicates the DIO signal lines are valid and safe to read. A listener ready to receive data releases the wire-ORed NRFD (not ready for data) line, letting it float HIGH. After reading the data bus, listeners release the wire-ORed NDAC (not data accept) line, so that it goes HIGH, after which the talker removes its message.

To guarantee valid transfer, an asynchronous three-wire handshake on the byte-transfer lines accompanies each byte transfer. The talker pulls DAV LOW, once all listeners are listening. The listeners pull NRFD LOW to indicate they're now busy reading this data. When the last listener releases NDAC, the talker knows every listener has read the data. The talker then removes its message and pulls DAV HIGH, and the listeners pull

NDAC LOW to show they're all set to read the next byte to come. The cycle repeats. Basically, in a nutshell, this is the IEEE-488 bus.

Problems Exist

The unformatted 8-bit bus data is a weakness. Although there is great freedom for devices or instruments to interpret the unformatted data, an instrument must be intelligent enough to extract the correct information. A good deal of processing is needed to both interpret and implement this data.

ATE-GPIB OEM designers are often hardware types that take a linear philosophy to software development. Structured programming—with preprogrammed modules that were defined, coded, assembled, debugged and adequately documented (rare)—is not the way it's often done. Instead, many firms (particularly small ones) only begin development after they wait for all devices to arrive. They then take a non-structured linear approach that produces code which executes rapidly; but is tougher to write and debug, and lacks structure, control and flexibility. Typically, debugging costs three-fold more than writing ATE-GPIB software.

It is far easier to determine early the needed preprogrammed modules, and then code, assemble, debug and properly document them. Driver modules developed for each device will be called as subroutines; and, after the instrument driver modules are completed, the control modules are developed.

The 488 is not a magical standard. Merely by connecting 488-compatible instruments and devices does not insure they will work instantly in perfect harmony. If they do work, it may be in a degraded mode. The 488 standard does not define the code and format for data nor the bus' operational aspects. Devices must speak the same code and format, but how the data is sent and formatted is up to the user.

In the rush to produce low-cost instruments, some instrument makers cut corners (functions). A programmable switcher with no SRQ can only receive commands to change its level. In a system where the power supply is about to fail, the controller has no warning of impending disaster; the results could be loss of data, or even injury.

Despite changes in the standard, understandability is still lacking. Charges were leveled at it for using non-English commands and unusual things happened when instruments received incorrect commands. The instrument systems using the 488 are generally not closed systems, and instead rely upon people as part of the system. Instrument intelligence, however, is not always enough to send and receive data in a form sufficiently meaningful that a semi-skilled human being can always understand.

Implementation

Should the OEM decide to specify all his 488-compatible equipment from one vendor, he faces the problem of limited selection in terms of available equipment and the functions of the instruments that this selected supplier provides. It is the easiest way, however, and is quick.

More often, it is wiser to shop around and pick and choose the GPIB equipment to get the best buys and functions needed. But, it cannot be expected that each device will support all GPIB functions, or that they all meet the 488 standard in the same way. And, one instrument maker cannot be relied on to help interface another maker's device. He has no vested interest in helping his competitor help you. So, GPIB functions should be checked carefully. Because a device is addressable and meets GPIB talk/listen handshaking protocols is not enough, even if that is all that's necessary to call it GPIB-compatible. Even after the care taken in specifying, time may still be spent to get all devices properly communicating. Software development will also be more difficult.

Beyond Instrumentation

GPIB is being used for more than inter-instrument data transfer. For example, PDP-11 high-speed DMA Unibus interface (to 488) has been offered for several years to implement PDP-11 measurement systems by providing 488 commands in single- or multi-controller envi-

Some IEEE-488 System Disadvantages

- Tedious to program
- Too-high software development costs
- Promotes linear, unstructured programming
- Confuses unwary test engineers
- Instruments truly compatible
- Lower-function instruments lack critical commands
- Unformatted data requires more processing power
- Tediously-written IEEE standards manual
- Confusing spec sheets and acronymated subset implementations
- Slower devices slow faster ones
- Constant referral to tedious instrument manuals causes confusion, wastes time

ronments. A driver program includes interrupt service routines assembled as a callable subroutine package for standalone use, or as a device handler. Such GPIB 11-2 boards were introduced three years ago or so by National Instruments.

More recently, NI introduced a LAN to interface DEC computers. The NI software package links multiple Unibus or Q-bus computers and can support RSX, RSTS/E, Unix, VAX/VMS and RT OS. Speed is its forte, and 500 Kbytes/s file transfers (for PDP-11 and VAX) are possible (with half that for the LSI family).

With the NI NET 488-1 and -2, one of the DEC computers is the system controller or host, while the slaves initiate file transfers. A R/W request from the slave initiates file transfer in one transfer to/from the host. The software handles interface protocols. In this LAN, the host could be a VAX-11/780 with PDP-11/34/23 slaves. This software package linking DEC minicomputers over the GPIB and supporting 0.5-Mbytes/s file transfers, points the direction for future products.

Triggering Modes

The unit with more triggering modes is usually more flexible in the system; and, if unexpected changes must be made later, it is more adaptable. We briefly mentioned triggering earlier and gave four categories, such as manual control, internal triggering (on an instrument clock or internal timer), external hardware with automatic timeout (which also lets the instrument insert a delay, before triggering for settling) and software triggering (by code over the bus). There are two other types to look for: software triggering with an instrument-inserted delay (prior to acting on the trigger code) and the universal GET (Group Execute) statement, which triggers it. With the INPUT statement, data transfer begins with the MSB and continues until it receives a delimiter code. By way of contrast, GET reads only one character at a time, and need not wait for a delimiter (termination character).

This isn't to infer that the instruments specified must have all these triggering modes. It will make such multimode instruments more flexible and adaptable, of course, but it isn't necessary nor does it make sense cost-wise to overspecify.

Flexibility, though it may create potential mis-specification troubles, does permit implementing as many 488 subsets as needed. For a printer, limited programmability works; no more is needed. But for a DMM, full programmability helps. This is reasonably clear cut. But what about two instruments of the same category — say, two DMMs? Then it's a different story, and differences do count a lot. As a rule of thumb, select the instrument with a higher level of subset implementation. Subset implementations are listed as two- or three-character alphanumeric acronyms, such as L4, E1, DT1 and so forth. Too many instrument makers' spec sheets only list one-line of subsets in acronymated form. In these cases, be assertive: call the makers for a list of subset implementations. From this, be careful to select the correct subset levels to match those needed requirements. For example, selecting a T6 subset DMM for use with a printer lacking a systems controller spells trouble. This DMM, if you specified it, implements T6 but lacks a talk-only mode. It has all the other three modes, but that won't help.

The subset acronyms, their descriptions and capabilities, may not be easy to remember. This and other complaints mentioned earlier (plus unfair criticisms of the document's state diagrams) pale compared to software criticisms. Test engineers constantly voice desires for easy-to-program (high level) instruments. Instrument makers cannot do this, for good reason, since this would more than quadruple programming time. These easier-to-program instruments would add more device-dependent characters and inefficiency, so that added-up, these would take unrealistic amounts of time.

Although able to theoretically reach 1 MHz, the 488 operates much slower. Part of the slowness falls upon multi-programming changes. Newer instruments hold enough memory to store program data for quick recall. Upon power-up, these instruments can be immediately loaded; when testing begins, the system will operate faster. Multiple programs are read from memory by use of simple instructions. In essence, distributing intelligence and data, as well as easily-callable local multiple programs, all make for higher system speeds. In more complex systems, buffer memory is becoming more sophisticated. These trends to distributed programs, more memory, more buffering and intelligent instruments will alter 488 test engineering philosophy. Greater capabilities and system throughput won't come without a price: greater complexity.

Next, look at handshaking. As we said earlier, a system is slowed by its slowest instrument. If one instrument has a 3.5 ms handshake and the others are in the 100 μs to 350 μs range, this means system instruments will suffer and automated test times will put your system at a competitive disadvantage. When comparing specs, use the units' response to universal commands and addresses and not handling device-dependent data, as the former more accurately typifies system speed. In most ATE and 488 systems, transmissions consist largely of universal commands or address data.

If individual instruments can handle their own processing, then this will raise overall system speed. Why should an instrument be made to transmit many readings? This also ties up the controller with interfacing with the instrument during its testing. If the instrument is intelligent enough, it can do this alone. Pre-process the data and then transmit the results to the controller.

Documentation

Too much time was (and still is) spent referring to instrument manuals to decipher codes and formats. This will continue to change as the instruments become more intelligent. □

Product Index

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Design Of Raster Scan Graphics Systems

by W. A. Kester

By 1983, raster scan display systems are projected to account for about 74% of all purchased graphic displays.

A typical raster scan display system is shown in **Figure 1.** This system consists of a MOS RAM memory buffer for storing display data in digital form; one or more memory controllers for managing display updating and controlling CRT refreshing; and a programmable μP for display graphics generation and image manipulation. The entire system would operate as an intelligent peripheral device to a host CPU fully capable of downloading most of the processing associated with image and graphics display. It would drive standard television monitors through built-in D/A circuitry.

A pixel is the smallest controllable picture element which is assigned discrete RGB (red, green, blue) values. The picture on the CRT is divided into a number of these pixels. For example, when a picture resolution is specified as

If the user can stand the reduced horizontal and vertical resolution of raster scan, it offers the lowest cost solution in a system application.

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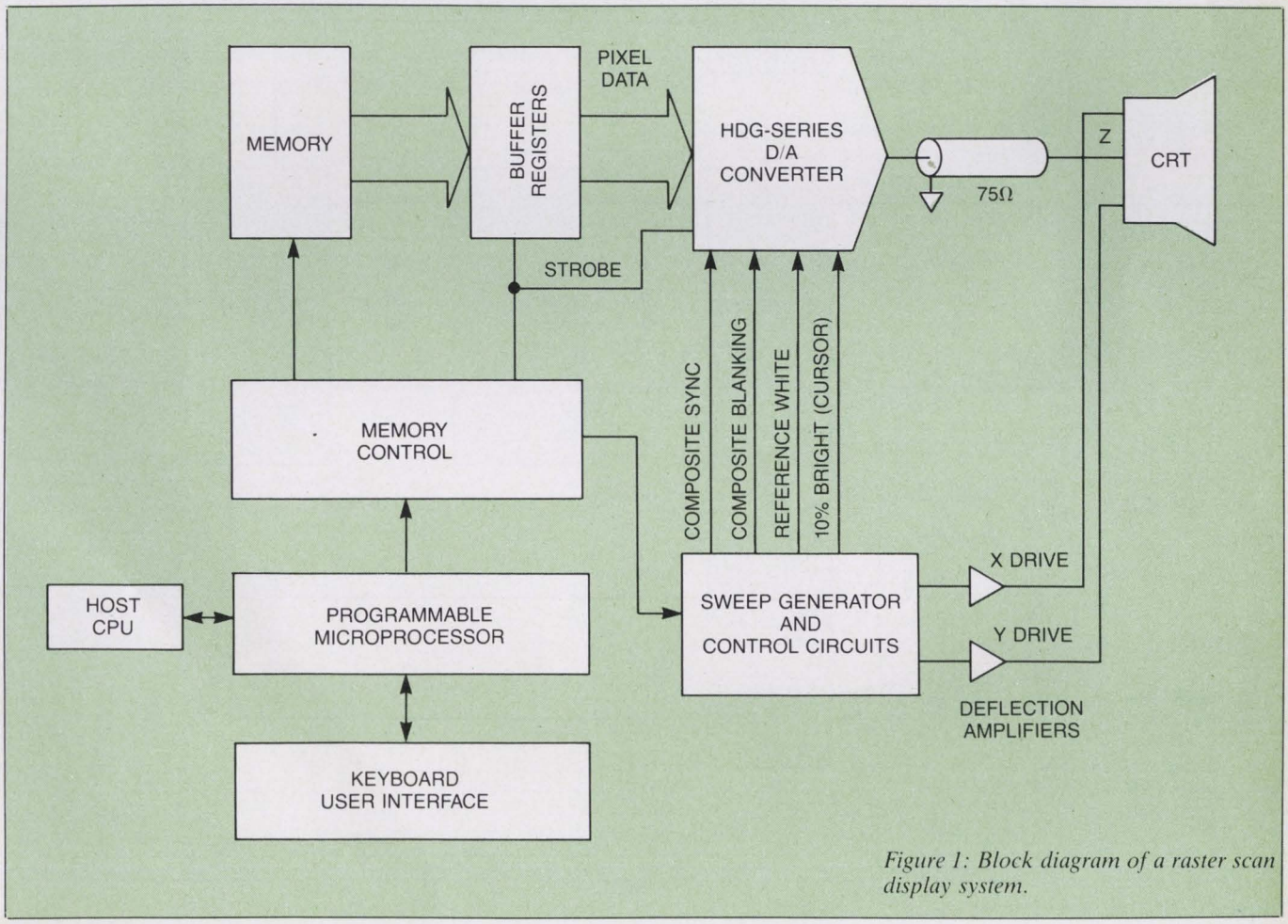

Figure 1: Block diagram of a raster scan display system.

1024 by 1024, it means there are 1024 horizontal lines of 1024 dots each; i.e., there are 1,048,576 total pixels. If the picture of the CRT is to be refreshed 60 times a second, a new pixel must be illuminated on the screen at least every 15.8 ns. This example neglects "overhead time" associated with vertical and horizontal blanking, but serves to illustrate the stringent settling time requirement placed on the D/A converter.

The D/A converter controls the z-axis of the CRT which modulates the brightness of the raster scan beam. For the above example, the D/A must be capable of being updated at the pixel rate of 15.8 ns (63.6 MHz). Obviously, the D/A must be capable of settling to a new value in less than 10 ns. If a white vertical line is being drawn on a black background, the D/A would be required to make a full-scale transition between adjacent pixel elements. **Figure 2** shows the effects of poor D/A settling time on the voltage waveform which is driving the z-axis of the CRT. Note that for the slow D/A, the voltage is not at the "white" level long enough to excite the phosphor of the CRT properly.

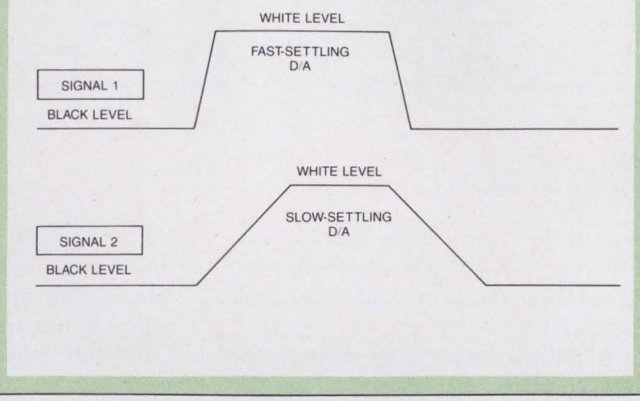

Figure 2: Pixel waveforms for fast and slow D/A converters.

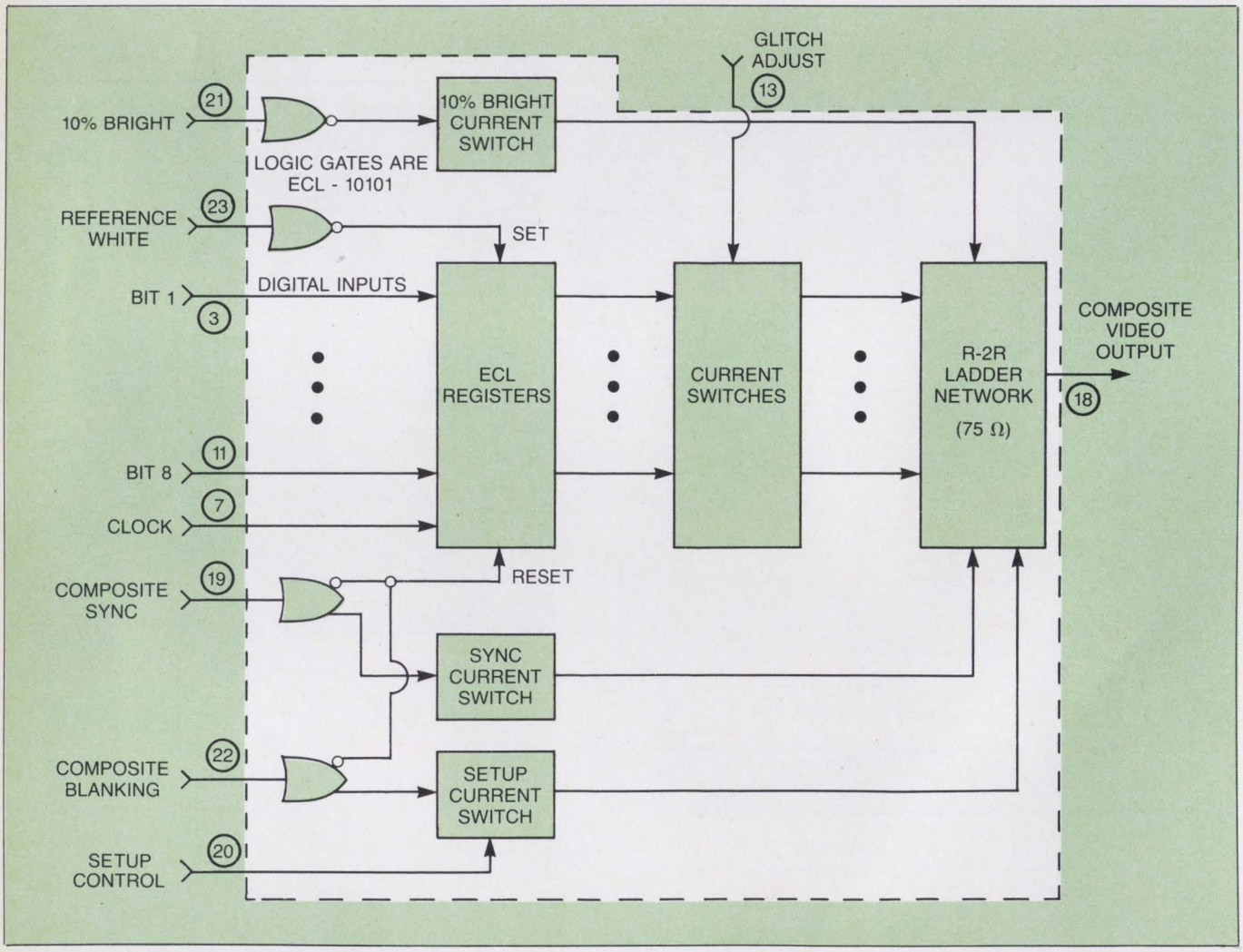

Figure 3: Block diagram of HDG-0805.

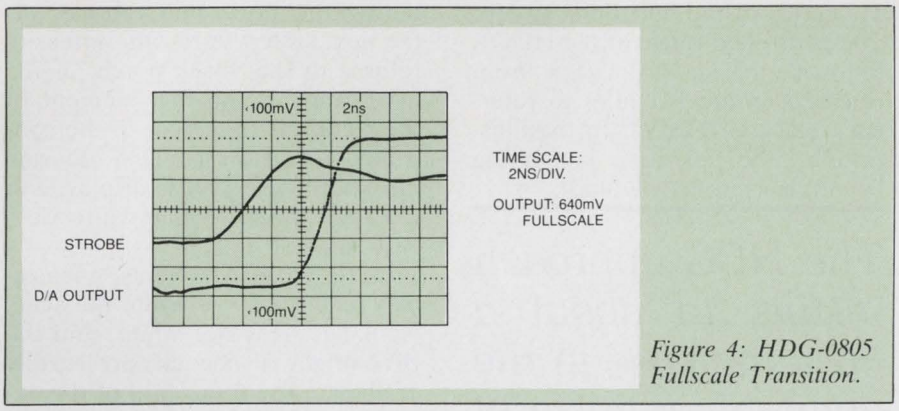

Figure 4: HDG-0805 Fullscale Transition.

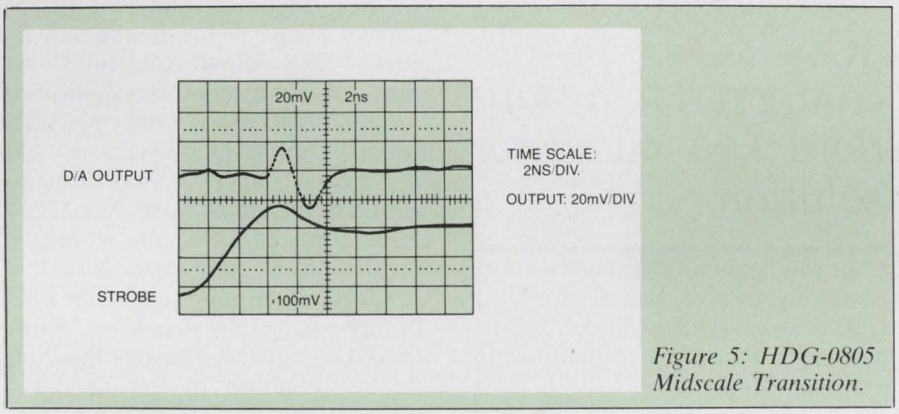

Figure 5: HDG-0805 Midscale Transition.

The quality of a picture on a CRT is directly affected by the speed with which the beam can be turned on and off. The failure to gain and maintain the white level will cause a variation in the relative brightness of the vertical lines in comparison to the horizontal lines. Today's top of the line monitors have z-axis input bandwidths in excess of 100 MHz and are, therefore, capable of handling pixel input signal risetimes of approximately 3.5 ns.

For a monochrome system, each pixel is divided into a number of finite levels determined by the resolution of the D/A. Typical raster scan systems have resolution requirements ranging from 4 bits to 8 bits, representing 16 to 256 levels of gray scale. For color processing, three memories and three D/A converters per terminal are required. Each D/A controls one of the three color guns (red, green, blue) of the CRT.

The capability of pixel-by-pixel addressing at the full refresh rate is probably the single most important factor contributing to the versatility of raster scan display systems. Static or dynamic alphagraphic, vectorgraphic, or photographic images can be combined on a single display surface with full color capability.

To most display users, the tradeoff between vector and raster scan displays means that, if the user can stand the reduced horizontal and vertical resolution of raster scan, it offers the lowest cost solution in a system application. The user may not have the expertise to design a vector display, but many have the capability of designing a successful raster scan display, especially since there are now building blocks within his grasp—such as those D/A's described herein, coupled with low-cost multiplexed CMOS memory devices. This allows the designer to maximize the versatility of his system design in the digital area, without worrying about spending thousands of man-hours in the design cycle for the display. The "value-added" aspect of such an approach is obvious.

On the other hand, if the system designer requires higher and higher resolution at higher and higher speeds, he can look forward to more cost effective products from his CRT system supplier with the newer technology D/A's described here, since the use of these D/A's and the design-timesaving features they employ should reduce the designer's effort and, ultimately, the cost.

Solutions To Raster Scan D/A Requirements

The HDG-Series of D/A converters have been specifically designed to solve the needs of raster scan systems requiring 8, 6, and 4 bits of gray scale resolution. These D/A's will yield 256, 64, and 16 gray scale output levels, respectively, for black and white or color displays. A block diagram of the HDG-Series is shown in **Figure 3**. The following discussion will be centered on the HDG-0805, since it would be used in the most demanding applications.

Resolution for the unit is 8 bits, and fullscale settling to within 1 LSB is 7 ns typical and 8 ns maximum (**Figure 4**). Fullscale settling time to within 1 LSB for the HDG-0605 (6 bits of resolution) and the HDG-0405 (4 bits of resolution) are 6 ns, and 4 ns maximum, respectively.

The output impedance of the HDG-Series is 75Ω (standard for video systems), and the fullscale output current is sufficient to develop the standard 1V p-p video level across an external 75Ω load.

An important feature of the unit is the inclusion of a set of ECL input registers to minimize time skew among bits and minimize glitch energy (typically less than 50 pV-s). To insure that each specific application of the HDG-Series D/A converter has minimum glitch energy, a "Glitch Adjust" input is provided. This adjustment allows the switching transistor's base bias voltage to be optimized for best performance in the customer's system. **Figure 5** shows a typical midscale glitch for the HDG-0805.

The HDG-Series D/A converters are packaged in 24-pin metal hybrid packages, and require only a single –5.2V power supply. Since the D/A is housed in a metal package, the effects of the high noise

environment usually associated with the CRT driving circuitry are effectively eliminated. The small package size allows for better performance and more efficient use of PC board real estate.

One feature of the HDG-Series is the self-contained digitally-controlled sync and blanking capability which is compatible with EIA standards RS-170, RS-330, and RS-343A. This feature is illustrated in **Figure 6**, which shows a typical composite video output waveform. Note that the gray scale (the discrete levels of the video signal between reference white and reference black) is divided into 256 levels by the 8 bits of the HDG D/A converter. Blanking, sync, and 10% bright levels are derived by three additional current switches within the D/A. The 10% bright input feature of the HDG-Series allows the placement of white figures or cursors on a white background.

Figure 6 shows the standard composite intensity waveform over 1½ cycles of the horizontal sweep. The controlled range of the HDG's full scale (0 to –643mV) is from reference white (–71mV) to reference black (–714mV). In the illustration, the intensity is varying from full white to full black.

The HDG approach results in about a 66% increase in the available number of gray scale levels compared to a standard D/A converter solution.

At the beginning of the sync portion, the intensity signal drops to the blacker-than-black "front porch" (–785 mV), and then to the extreme black level (–1071 mV) during the horizontal retrace. As the next sweep starts, the intensity returns to the "back porch" (–785 mV), and, as the first element of the picture is triggered, to the controlled range of the D/A. During this scan, the cursor is displayed at the 10% "brighter than white" level (0 mV).

In raster scan systems, the signals required to generate the sync, blanking, reference white, and the 10% bright (if needed) are readily available. The utilization of the extra sync, blanking, and 10% bright current switches inside the HDG-Series D/A allows the full 8-bit range of 256 levels to be dedicated to the gray scale, with one LSB equal to approximately 2.5 mV. If a standard 8-bit D/A were used to generate the *entire* composite video waveform, the gray scale would be divided into only approximately 154 levels corresponding to an LSB of approximately 4.2 mV. Thus, the HDG approach results in about a 66% increase in the available

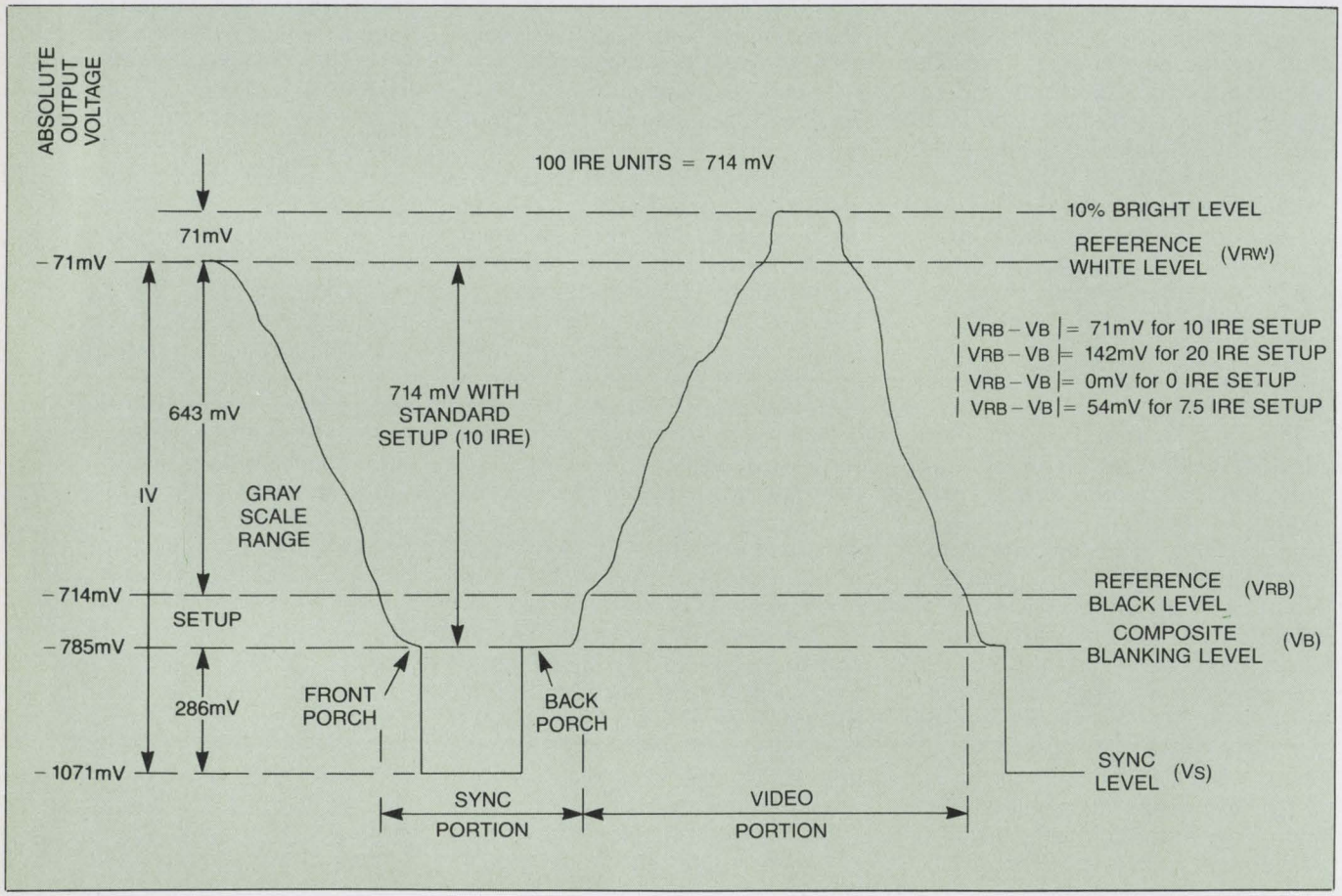

Figure 6: HDG-0805 Composite Output Waveform.

number of gray scale levels compared to a standard D/A converter solution.

Figure 7 shows a system application of the HDG-Series in a typical raster scan system where the sync, blanking, reference white, and 10% bright/control signals are generated within the control circuits of the display.

System Considerations

First and foremost, the converter should be mounted on a double sided printed wiring board with ground on one side and the conductors on the other. The use of a massive ground plane is required to prevent interaction of analog and digital ground currents. The low-impedance ground plane offers a

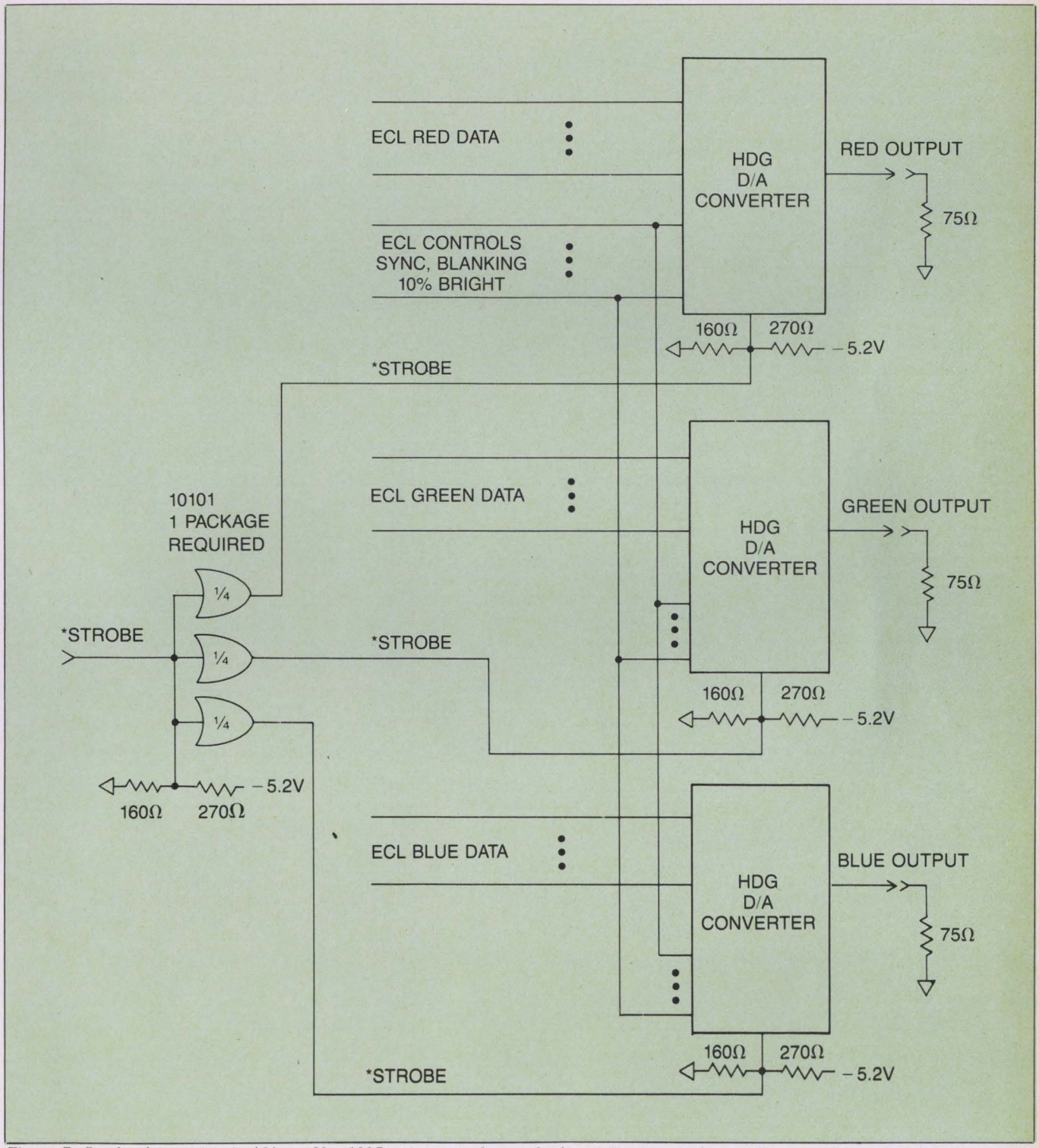

*Figure 7: Strobe driver circuit. *Note: Use 100Ω microstrip for strobe lines. Terminate data and control lines in 1000Ω to −5.2V for runs less than 1 inch. For longer runs use microstrip techniques as shown for strobe lines.*

good "sink" to the fairly high currents that are usually associated with the digital lines into a fast-settling D/A converter.

Electrical isolation of digital and analog grounds is more appropriate to high-resolution converters (14-bit or greater) where small differential changes in ground currents might affect the differential linearity of the converter. For fast settling converters with 12 bits of resolution or less, the massive ground plane technique is more effective.

All D/A converter ground pins should be soldered to the ground plane directly upon leaving the package. The use of plastic or ceramic IC sockets for the D/A is undesirable. If sockets must be used, spring-loaded "pin sockets" for

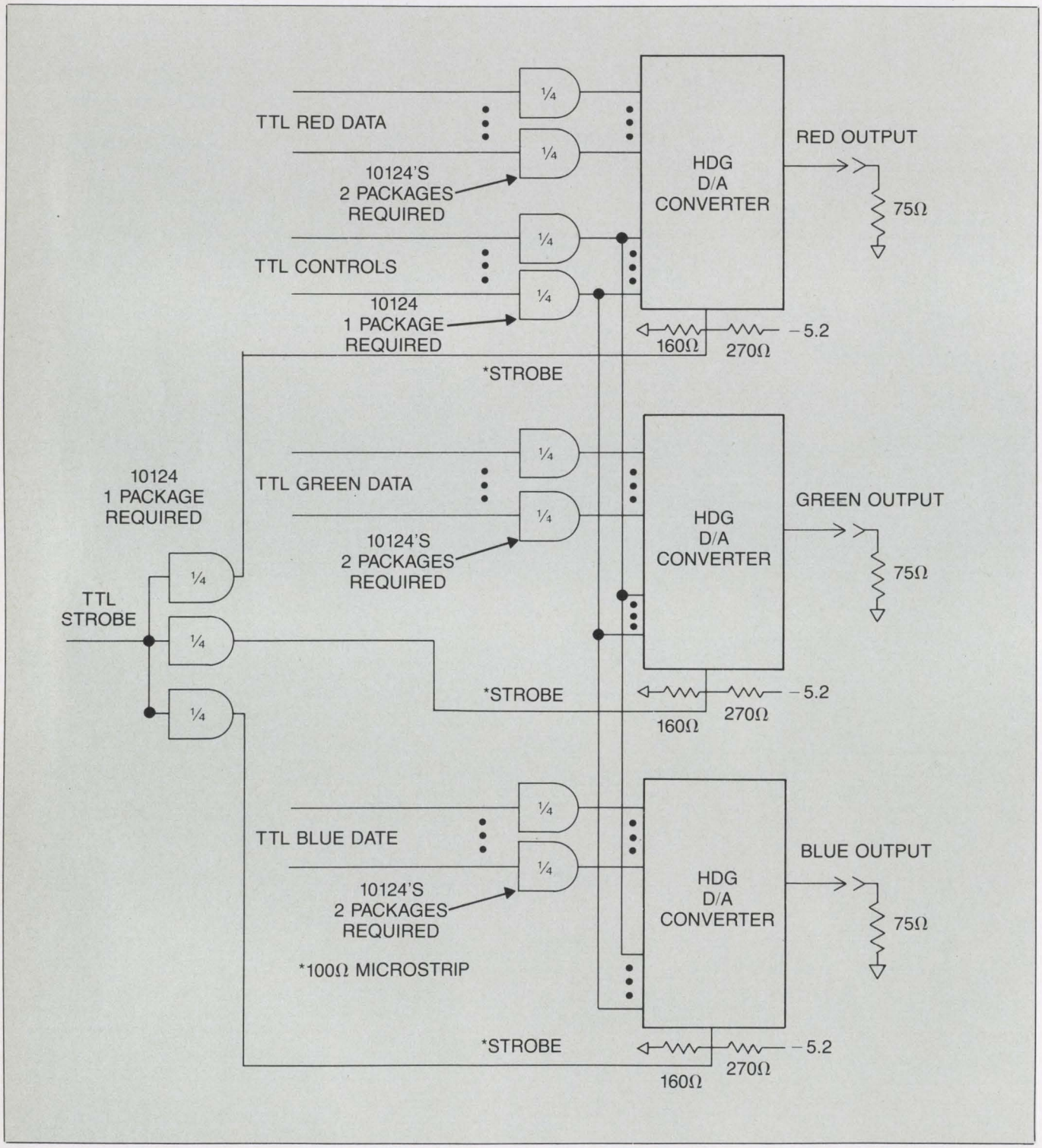

Figure 8: Use of HDG series with TTL inputs. TTL to ECL translators are 1024. Terminate all ECL data and control line inputs 100Ω to −5.2V.

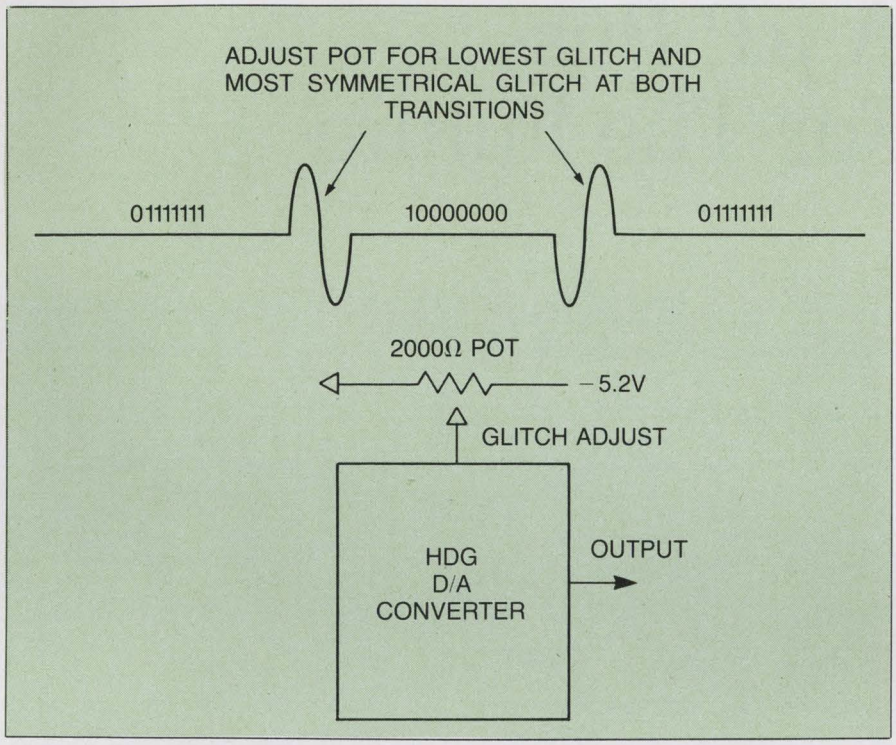

Figure 9: Glitch Adjust Circuit.

each lead are acceptable. These spring loaded "pin sockets" are inserted through plated holes on the printed wiring board and are then soldered to pads on the conductor side of the board.

Microstrip techniques should be used for digital, strobe, or analog runs greater than one inch.[1] It is desirable to bring the analog output from the HDG D/A to the CRT z-axis input through a properly terminated 75Ω coaxial cable of no more than three feet in length. Longer runs may degrade settling time due to the coaxial cable "skin effect."[2]

All power supply inputs to the HDG D/A converter must be decoupled with good quality 0.1 μF ceramic capacitors located as close as possible to the power supply input pin of the hybrid package. It is also good practice to bypass all power supply lines with an electrolytic capacitor (1μF or greater) at a convenient place on the printed wiring board.

Although the use of switching regulated power supplies is in vogue, the spikes put out by these types of power supplies can be several hundred millivolts in amplitude, and contain very high frequency components which are almost impossible to filter. These spikes also tend to get into the grounding system, and can cause noise in the system which is often attributed to the D/A or other analog circuitry. The use of a high-accuracy, linear-regulated power supply for the –5.2V supply to the HDG D/A is recommended for best results. As an alternative, the –5.2V can be derived from any negative rail by using a 7905.2 three terminal regulator.

If a minimum glitch is required, an external potentiometer may be connected to the "glitch adjust" input of the HDG D/A converter.

Special consideration should be given to the "strobe" input of the HDG D/A, especially if three D/A's are to be clocked simultaneously in a color system. The strobe input of a single HDG D/A is equivalent to 8 ECL loads (50 pF and 5000 Ω to –5.2V). The clock driver circuit of **Figure 7** can be used to provide the appropriate drive capability in a color system operating at high pixel update rates.

Although the use of ECL logic on the D/A converter board is highly recommended, TTL to ECL translators (such as the 10124) can be utilized at lower update rates. **Figure 8** shows the translation circuitry required to clock three HDG D/A's simultaneously. The TTL to ECL translators should be located as close as possible to the HDG D/A's for optimum performance.

Finally, if a minimum glitch is required, an external potentiometer may be connected to the "glitch adjust" input of the HDG D/A converter as shown in **Figure 9**. The potentiometer is adjusted to equalize the positive and negative glitches for the best compromise between the up-transition (01111111 to 10000000) and the down-transition (10000000 to 01111111). This adjustment should be performed in the system for optimum results.

Summary

Modern raster scan graphics display systems combine a multitude of analog and digital technologies. The HDG-Series D/A converters have been designed to simplify a portion of the analog circuitry in such systems. In addition to meeting the settling time and glitch energy requirements of modern raster scan systems, the HDG-Series includes a number of control inputs (sync, blanking, etc.).

References

(1)MECL System Design Handbook, Third Edition, Motorola Semiconductor Products, Inc., 1980.

(2)*Handbook of Wiring, Cabling, and Interconnecting for Electronics*, Charles A. Harper, Editor, McGraw-Hill Book Company, 1972, Section 4. □

VMEbus—A μP Bus For The Future

In response to a common set of user and market needs, a new μP system bus has been born.

by Tom Balph

As any observer to the semiconductor industry knows, the flood of 16-bit μP systems is upon us. With the flood have come many varying requirements for system buses that are used to implement the 16-bit computing hardware. The needs include retrofit to older equipment, higher performance, expandability, diagnostic capabilities, new architectural features, or any combination of these and other requirements.

VMEbus is an adaptation of VERSAbus, a μP bus also created by Motorola, and a symbiotic relationship exists between the two. Both share common design objectives: provide a cost effective system bus; support complex systems through fault tolerance and diagnostic capability; support multiple processors and controllers; high performance data rates and throughput; and, allow for future growth.

Origin of the VMEbus

VERSAbus was originally defined because existing industry pseudo-standard buses were found to be deficient. Most common buses started as part of a particular system design and grew in usage as popularity of that system or computer increased. As a result, bus specifications tended to be lacking or non-existent, variations of bus usage were inconsistent or unstandardized, and perhaps most important, these buses did not have the capabilities to support the next generation microcomputer products. VERSAbus was thus created to meet the needs of advanced 16-bit μPs, particularly the MC68000.

Introduced approximately two years after VERSAbus, VMEbus was defined in response to user inputs and market requirements (especially the European needs). Although close in functionality, the two buses have different form factors (card size, connectors, etc.) and different bus timing. The VMEbus is functionally a subset of most VERSAbus features with some modifications. Its card format (commonly called Eurocard format) is smaller than VERSAbus and uses DIN pin-in-socket connectors. This mechanical configuration is used to gain acceptance in European markets and for applications where resistance to mechanical vibration is paramount (such as industrial control).

VMEbus is also unique in that three semiconductor suppliers—Motorola, Signetics/Philips, and Mostek—are supporting its use in system products. With the introduction of VMEbus, the modern systems designer is offered a popularly supported bus with some unique capabilities that compliment its forebearer VERSAbus and shares its power.

Structure and Function

The VMEbus structure is based upon a 16-bit data bus and a 24-bit

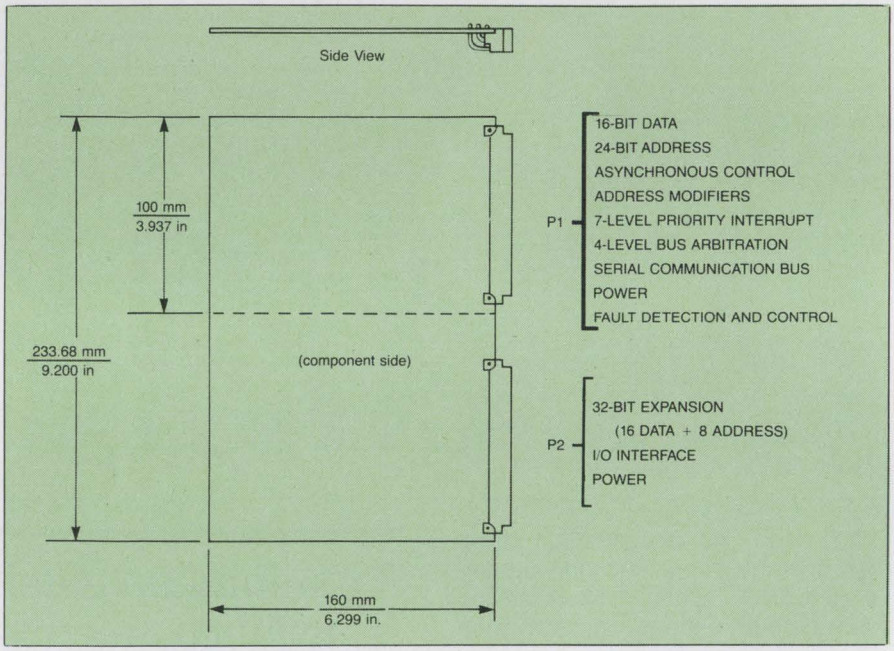

Figure 1: The VMEbus printed-circuit card format uses the DIN Eurocard standard, and allows both single- and double-size cards.

Tom Balph is Manager of Systems Engineering for Industrial Segment Marketing at Motorola Inc., Semiconductor Group, Phoenix, AZ.

address space with both expandable to 32-bits. The DIN Eurocard standard is used for the printed-circuit card format, and both single size and double size cards are allowable **(Figure 1).** The primary 96-pin connector contains 16 data lines, 23 address lines plus 2 data strobes to generate a 24-bit address width, bus arbitration control, priority interrupt control, diagnostic lines, and all additional signals necessary to control data transfer and other bus functions. The secondary 96-pin connector (when used) provides expansion lines to extend both address and data to 32-bits, and provide user I/O lines.

The bus form factor meets DIN 41612 and 41494 mechanical standards which are commonly accepted in Europe. A major advantage is the pin and plug-style connectors that prevent long term contact problems and are also more resistant to vibration.

VMEbus is configured such that only the primary connector J1/P1 is required to support a full 16-bit μP system interface. In this way, both single size and double size cards can be used; and with proper mechanical support, both can be used in the same backplane. The smaller card size is 160 × 100 mm and the larger is 160 × 233.68 mm. The second connector J2/P2 is used for user I/O or for expansion into 32-bit systems. The J1/P1 and J2/P2 connector pin assignments are shown in **Figure 2.**

Functionally, VMEbus can be summarized as having a master/slave asynchronous, nonmultiplexed data transfer structure, seven levels of priority interrupt, four levels of data bus arbitration (supports multiple masters), fault detection and control, and special transfer cycles. **Table 1** gives a summary of its characteristics and compares them to other common buses. Power supply voltages include +5V, ±12V, and +5V standby. Data transfer rates as high as 20 Mbytes/s in the expanded 32-bit configuration are supported. All signal lines are TTL compatible and parallel termination networks are used to reduce signal reflections and ringing, as well as provide a high state pullup for open collector and three-state lines.

Data Transfer Mechanism

Similar to VERSAbus and other common buses, VMEbus has a master/slave asynchronous data transfer format. This allows for multiple bus masters (processors and controllers); and memories and peripherals of varying speeds can be used without slowing the bus to the slowest system device.

VMEbus uses three basic cycle types in its data exchange protocol, these are read, write, and read-modify-write cycles. Common read

J1/P1 Pin Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5*
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK (1)	A17
22	IACKOUT*	SERDAT (1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

J2/P2 Pin Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	User I/O	+5 Volts	User I/O
2	User I/O	GND	User I/O
3	User I/O	RESERVED	User I/O
4	User I/O	A24	User I/O
5	User I/O	A25	User I/O
6	User I/O	A26	User I/O
7	User I/O	A27	User I/O
8	User I/O	A28	User I/O
9	User I/O	A29	User I/O
10	User I/O	A30	User I/O
11	User I/O	A31	User I/O
12	User I/O	GND	User I/O
13	User I/O	+5 Volts	User I/O
14	User I/O	D16	User I/O
15	User I/O	D17	User I/O
16	User I/O	D18	User I/O
17	User I/O	D19	User I/O
18	User I/O	D20	User I/O
19	User I/O	D21	User I/O
20	User I/O	D22	User I/O
21	User I/O	D23	User I/O
22	User I/O	GND	User I/O
23	User I/O	D24	User I/O
24	User I/O	D25	User I/O
25	User I/O	D26	User I/O
26	User I/O	D27	User I/O
27	User I/O	D28	User I/O
28	User I/O	D29	User I/O
29	User I/O	D30	User I/O
30	User I/O	D31	User I/O
31	User I/O	GND	User I/O
32	User I/O	+5 Volts	User I/O

Figure 2: Pin assignments for the J1/P1 primary connector, and the J2/P2, used for user I/O or for expansion into 32-bit systems, are shown above. (NOTE: (1) SERCLK and SERDAT represent provision for a special serial communication bus protocol still being finalized.)

COMPARISON OF THE VME BUS TO OTHER 16 and 32-BIT BUSSES

	VMEbus	VERSAbus	Multibus[1]	Q-Bus[2]	S-100 Bus
Bus Type	Asynchronous Non Multiplexed	Asynchronous Non Multiplexed	Asynchronous Non Multiplexed	Asynchronous Multiplexed	Synchronous Non Multiplexed
Address Width	24 Standard 32 Expanded	24 Standard 32 Expanded	20 Standard 24 Expanded	16 Standard 18 Expanded	16 Standard 24 Expanded
Data Width	8, 16, 32	8, 16, 32	8, 16	8, 16	8, 16
Board Size	Double Width 160 × 233.4 mm = 37344 mm^2 Single Width 160 × 100 mm = 16000mm^2 (Standard Eurocard)	Double Width 235 × 368.3 mm = 86,532 mm^2 Single Width 235 × 203.2 = 47,742 mm^2	171.5 × 304.8 mm = 52273 mm^2	214 × 263.4 mm = 56368 mm^2 214 × 147.3 mm = 31522 mm^2	137.8 × 254 mm = 35,001 mm^2
Connector Type	Pin & Socket	Edge	Edge	Edge	Edge
No. of Pins on Primary/Secondary Connector	96/96	140/120	86/60	36	100
Voltage (V)	+5, ±12, +5 Standby	+5, ±12, ±15 +5 Standby	+5, ±12	+5, ±12, +5, +12 Backup	+8, ±16
Interrupt Levels	7	7	8	4	8
Arbitration Levels	4	5	1	1	16
Multiprocessor?	Yes	Yes	Yes	DMA only	Yes
Error Signals	AC Fall, System Fail, Bus Error	AC Fail, System Fail, Bus Error, Add./Data Parity	None	DC Power OK Power OK	Power Fail, Bus Error
Special Cycles	Read/Modify/Write Block Transfer Access Privilege Levels	Read/Modify/Write Block Transfer Access Privilege Levels	Lock	Refresh Read/Modify/Write Event Interrupt	None
Extendable Modes For Future	Yes (Address Modifiers)	Yes (Address Modifiers)	No	No	No
Separate Serial Bus	Yes	Planned For Reserved Pins	No	No	No
[1]Multibus is a trademark of Intel Corporation [2]Q-bus is a trademark of Digital Equipment Corporation					

Table 1: Summary of VMEbus characteristics and comparison with other common busses.

and write timing flows are illustrated in **Figure 3.** The data transfer protocol is controlled by five signals:
AS*—Address Strobe
DSO*—Data Strobes
DS1*
DTACK—Data Transfer Acknowledge
BERR*—Bus Error

As shown in **Figure 3,** the AS* shows that a valid address is on the bus, and the data strobes DSO* and DS1* signal that data transfer will occur on either the upper byte (DS1* = lines DO8–D15) or the lower byte (DSO* = lines D00–D07) or both. This concept of two types of strobes is required for the read-modify-write cycle. This nondivisable cycle is used to read and update a given system location, and the address strobe is activated for the entire cycle while the data strobes do the handshake required for the read and again for the write. The read-modify-write cycle allows the processor to change or update the contents of memory without intervention of an interrupt or bus arbitration. This is extremely useful in multiple processor systems, or systems with DMA for manipulating semaphor registers.

The slave (peripheral or memory) response to a master is a data transfer acknowledge signifying that the slave has either read data from the bus or has put data on the bus, and the master responds by completing the cycle. A second signal—bus error, BERR*—also causes the master to terminate the cycle. The error signal is normally activated by the slave in response to an on-board error such as a memory parity error.

Another powerful feature of the VMEbus data transfer structure is a field called Address Modifiers. This 6-bit field **(Table 2)** informs any device monitoring bus activity what class of transaction is occurring. The address modifier field devides data transfers into supervisory and user categories and in turn, allows several forms of access within each category. These forms include: standard (24-bit address) program, data, and ascending access (a form of block transfer); I/O access (short 16-bit address); and extended (32-bit address) data, program, and ascending access. Memory and I/O devices responding to a bus cycle use the address modifiers to determine whether they should decode a 16-bit, 24-bit,

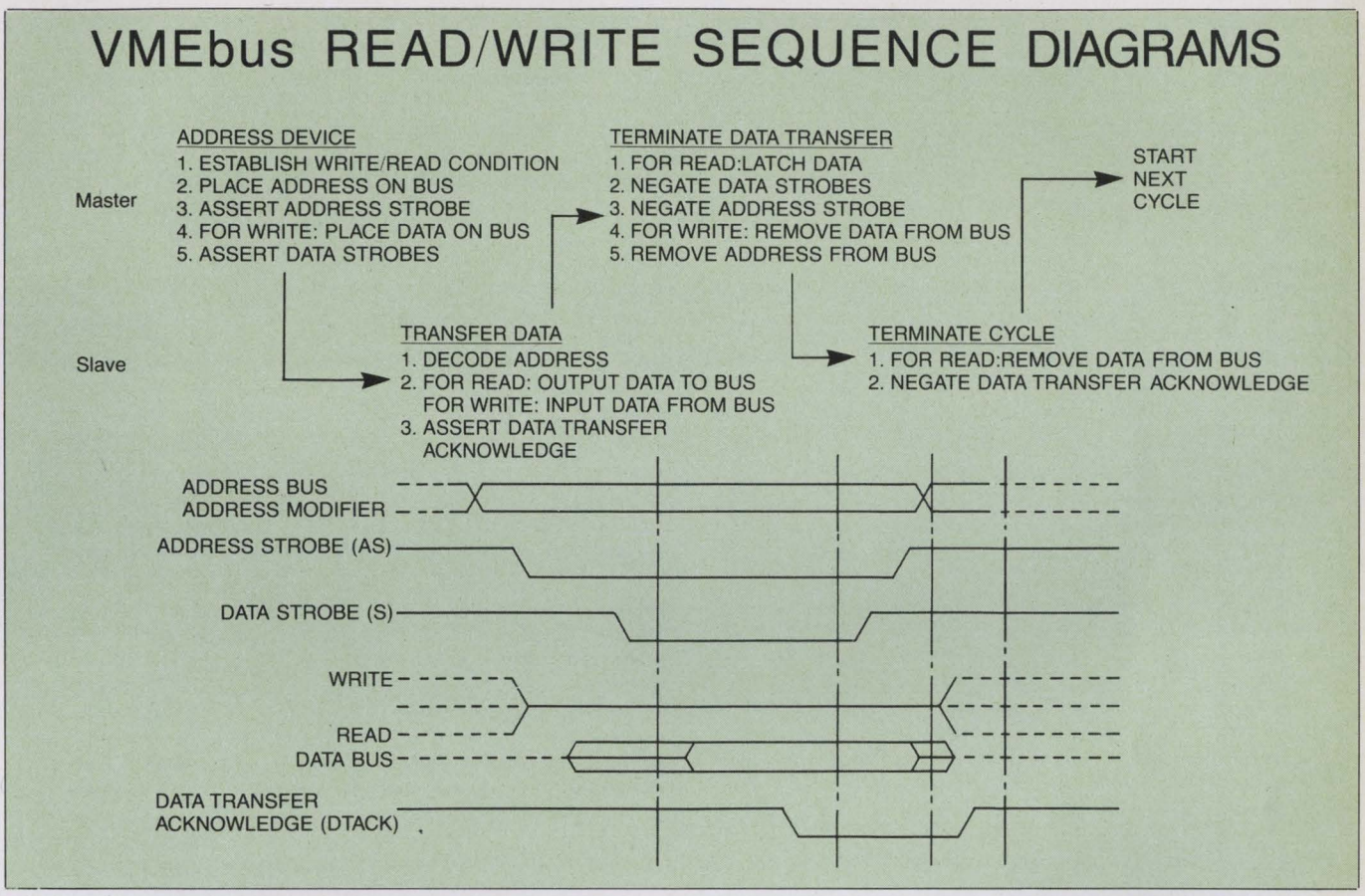

Figure 3: The three basic cycle types used by the VMEbus are read, write, and read-modify-write cycles. Common read and write timing flows are illustrated above.

or 32-bit address accordingly.

The ascending access or block move deserves special mention. This access is similar to the read-modify-write in that AS* is asserted for the entire string of read's or write's. The slave device is reponsible for storing the initial address and increments the address after each cycle. In this way a sequential block of memory can be accessed in a high speed manner. This is very useful for DMA transfers or data transfers between processors.

Also important to the user are the undefined areas of the address modifier codes. Some codes are reserved for user definition and several additional codes are reserved for future definition. As new concepts such as resource management, multiple processors, and distributed memory management mature, the address modifier codes can be changed to support these applications. There is ample room for growth.

Multiple Processor Support

Being an asynchronous interface, the data transfer structure simplifies using multiple processors and controllers on VMEbus. The bus arbitration and interrupt configurations additionally support multiple masters through a flexible structure and definition.

Any bus allowing multiple masters must have a means of allocating (arbitrating) which master has use of the data transfer at a given time. The VMEbus arbitration consists of four prioritized request levels and four prioritized grant levels. A system module called an "Arbiter" receives requests for the bus from modules called "Requesters." Each bus master must have a requester to gain control of the data bus. The Arbiter than gives control of the bus via one of the four levels of bus grant. Masters are priortized both by the level of priority to which they are assigned and by their position within the level.

The VMEbus specifies three options that can be used by the Arbiter: *Priority option* always assigns the bus on a fixed priority basis from highest to lowest; *Round robin option* assigns the bus on a rotating sequential basis going through all levels; and *Single level option* honors only one level of request/grant with multiple masters daisy-chained in priority on that single level.

The first two options are most useful for more complex systems and can be used to optimize bus usage and response time to bus requests. The final option is the simplest and most efficient method suited to a single CPU-based system with a few DMA devices and I/O controllers.

The bus interrupt structure also has options which are useful to multiple master systems. There are seven request lines by which mod-

Address Modifier Codes

HEXADECIMAL CODE	ADDRESS MODIFIER 5	4	3	2	1	0	FUNCTION	DEFINED BY
3F	H	H	H	H	H	H	Standard Supervisory Ascending Access	VME Bus Spec.
3E	H	H	H	H	H	L	Standard Supervisory Program Access	VME Bus Spec.
3D	H	H	H	H	L	H	Standard Supervisory Data Access	VME Bus Spec.
3C	H	H	H	H	L	L	Undefined	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Ascending Access	VME Bus Spec.
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access	VME Bus Spec.
39	H	H	H	L	L	H	Standard Non-Privileged Data Access	VME Bus Spec.
38	H	H	H	L	L	L	Undefined	Reserved
30–37	H	H	L	X	X	X	Undefined	Reserved
2F	H	L	H	H	H	H	Undefined	Reserved
2E	H	L	H	H	H	L	Undefined	Reserved
2D	H	L	H	H	L	H	Short Supervisory I/O Access	VME Bus Spec.
2C	H	L	H	H	L	L	Undefined	Reserved
2B	H	L	H	L	H	H	Undefined	Reserved
2A	H	L	H	L	H	L	Undefined	Reserved
29	H	L	H	L	L	H	Short Non-Privileged I/O Access	VME Bus Spec.
28	H	L	H	L	L	L	Undefined	Reserved
20–27	H	L	L	X	X	X	Undefined	Reserved
10–1F	L	H	X	X	X	X	Undefined	User
0F	L	L	H	H	H	H	Extended Supervisory Ascending Access	VME Bus Spec.
0E	L	L	H	H	H	L	Extended Supervisory Program Access	VME Bus Spec.
0D	L	L	H	H	L	H	Extended Supervisory Data Access	VME Bus Spec.
0C	L	L	H	H	L	L	Undefined	Reserved
0B	L	L	H	L	H	H	Extended Non-Privileged Ascending Access	VME Bus Spec.
0A	L	L	H	L	H	L	Extended Non-Privileged Program Access	VME Bus Spec.
09	L	L	H	L	L	H	Extended Non-Privileged Data Access	VME Bus Spec.
08	L	L	H	L	L	L	Undefined	Reserved
00–07	L	L	L	X	X	X	Undefined	Reserved

Table 2: The Address Modifier field informs any device monitoring bus activity what class of transaction is occurring.

ules called "Requesters" may ask for servicing by an Interrupt Handler (a processor capable of servicing system interrupts). VMEbus allows for two groups of interrupt subsystems: *Single handler systems* which have a supervisory processor which receives and services all bus interrupts; and *Distributed systems* which have two or more processors which receive and service bus interrupts.

The single handler option is most common because single processor systems can use this technique as well as multiple processor systems which assign all interrupt servicing to a system controller or CPU. In this case, the seven request lines are prioritized and interrupts will be serviced on a highest priority basis. In systems with a single processor or main CPU, this device will utilize the system bus a high percentage of the time and will service interrupts as part of its normal activity. If processing is distributed among several processors, the interrupt handler may not have the bus a large part of the time. In this case, the interrupt handler will have to request the bus through arbitration, and response time to interrupts may be slower.

Both interrupt options allow multiple devices to request servicing on each level or request line. The requesting devices on each level are daisy-chained such that the first device on the daisy chain of that level will get serviced.

Error Reporting Aids Diagnostics

VMEbus has three means of signifying bus or systems failure. As previously described, signal Bus Error (BERR*) allows the slave or another device (such as a watch dog timer) to end the present bus cycle. The present bus master can either retry the cycle or enter some kind of exception processing sequence. The other two means of signaling system problems are ACFAIL* and SYSFAIL*.

ACFAIL* signal is asserted whenever the input power source (normally the AC line voltage) has failed. The DC power to the system must remain in specification for a minimum of 4 ms after ACFAIL* is asserted. This allows for an orderly power down sequence of the system. VMEbus is unique (with the exception of VERSAbus) in that the bus arbitration defines as emergency sequence to control mastership of the bus and allow a system controller to gain bus mastership and provide a shutdown sequence.

The SYSFAIL* (system fail) line signals failure of any part of the system. This line can be asserted at system startup and released after a self-test sequence, or any device can assert the line during normal operation if a failure has been detected. Response to the line is dependent on the user system, that is,

it could be initiation of a diagnostic sequence, a halt condition, or an orderly shutdown.

Multiprocessor Communication

To enhance its use as closely coupled multiple processor system bus, VMEbus features: asynchronous data transfer structure, read-modify-cycle for updating semaphores in global memory, address modifiers for resource allocation and future functional expansion, powerful, flexible bus arbitration and priority interrupt structures, and system diagnostic capabilities including defined multiple processor power down sequence.

To top things off, provision has been made for a serial bus for interprocessor communication. Two lines called SERCLK (serial clock) and SERDAT (serial data) are set aside for this purpose. Interprocessor communication, external to normal VMEbus activity, is the key to implementation of high performance multiple processor systems. Each controller or processor has its own operating kernel and has need of coordinating tasks and data exchange with other I/O devices and processors. The serial communication bus or "interintelligence bus" (I^2B), can be used to issue commands and receive acknowledge, provide diagnostic control, pass semaphores, etc.

The serial clock is supplied by a single continuous source and is used by all devices. Serial data is transmitted on the data line by the present serial bus master. Arbitration is done on the serial bus by all those processors wanting to transmit at a single time. Once arbitration has occurred, the highest priority device is allowed to broadcast its message.

The message is a short packet of information. The data can carry priority, source address, destination address(es), message type, functional parameters, and acknowledgements. These information packets do not contain large data blocks; that is, movement of blocks of data would be done via the system data bus. As an example, the serial message can tell a second processor that the first processor (the transmitter) data is available.

A definition for the serial bus format has been proposed by Signetics/Philips (C. Kaplinsky, "Decentralizing Microprocessor Bus Grows Easily From 16 to 32-Bits," *Electronic Design,* pp. 173–179, Nov. 12, 1981.) This definition is now under consideration. Although not presently fully defined, the serial bus will be a major boon to multiple processor systems.

Hindsight And Future

VMEbus was designed using a certain amount of hindsight, that is, learning from the experiences gained from VERSAbus. As stated previously, the basic functionality and architecture of VMEbus were taken from its predecessor. **Figure 4** shows a comparison of features and one can see the differences between the two buses.

The best choice for a system design is in large part determined by the targeted application. VERSAbus is better suited to higher performance, more complex systems by its larger card size and greater sophistication (parity, extended address modifiers, and test control). More processing functions can be put on a single card allowing more sophisticated subsystems. Applications suited for VERSAbus include data processing, robotics, color graphics, CAD, supervisory control, process control, and communications.

VME Modularity

In comparison, VMEbus is more modular with a smaller card size, has pin and plug style connectors, and still retains outstanding functionality. Targeted applications include factory automation, low end process control, and intelligent terminals. The smaller card size of VMEbus will be better suited to more complex systems as more computing power is integrated onto LSI and VLSI devices.

Both buses feature room for future expansion and growth. Both data and address can expand to 32-bits. The Address Modifier codes can be functionally extended as other useful applications are identified. The VMEbus serial communications bus will be defined for multiple processor systems. Although separate entities, VMEbus and VERSAbus will continue to mature and compliment each other. □

FEATURE	VERSAbus	VMEbus
Address	24/32	24/32
Data	8/16/32	8/16/32
System Reset	√	√
System Fail Detect	√	√
Bad Xfer Indic.	√	√
16 MHz Clock	√	√
Power Fail Seq	√	√
Standby +5 V Dist.	√	√
Power Dist.	+5, +12, −12	+5, +12, −12
Interrupt Lines	7	7
Arbitration Levels	5	4
Privilege Maps	256	64
Address Parity	√	—
Data Parity	√	—
PWR-On Test Control	√	—
AC Clock	√	—
± 15 V Dist.	√	—

Figure 4: The above table compares VMEbus with its predecessor, VERSAbus.

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All CMOS Industrial μC Boards

The first 19 members of the new Series/800 line of CMOS Industrial μP (CIM) boards are now available from National Semiconductor. They use the single-wide Eurocard format, and are based on the company's NSC800 CMOS μP. Targeted for applications in harsh environments, the new board line functions over an operating range of −40° to +85°C (−40°F to +185°F).

The single-wide Eurocard format was chosen because its form factor allows the electronics enclosure to be relatively small; the user also only needs to purchase the functionality he requires for his application.

Because the products use CMOS technology, the line may be housed in sealed enclosures for placement in locations requiring intrinsically safe electronics, where wash downs are compulsory, or in corrosive environments. The elimination of cooling fans and vent-filter assemblies results in cost savings to the user.

Uninterruptable power capability may be added to the Series/800 board line by adding an external battery.

The line is based on the Cimbus; this synchronous bus incorporates the unique features of the NSC800, as well as many end system requirements (such as real battery backup/operation, system-level fail-safe timer, and an alarm relay output.)

The Series/800 board line also makes available the Distributed Input/Output Bus (DIB), used for discrete I/O interfaces such as a typical interface to an operator's panel. The DIB replicates many of the Cimbus signals, but also contains control and timing interfaces. The DIB allows all discrete I/O to be handled by the host CPU in the same way. The form factor for user-designed discrete I/O boards is not dictated, and any number of boards can be multi-dropped on the DIB for any count/configuration of I/O devices the user may require.

The BLMX-80C real-time, multitasking operating system, and the Starplex Development System, with the full NSC800 emulation, round out the support.

Board pricing for the Series/800 family ranges from $128 for the CIM-611, to $546 for the CIM-802, to $952 for the CIM-610 (unit quantity suggested resale.)

Write 198

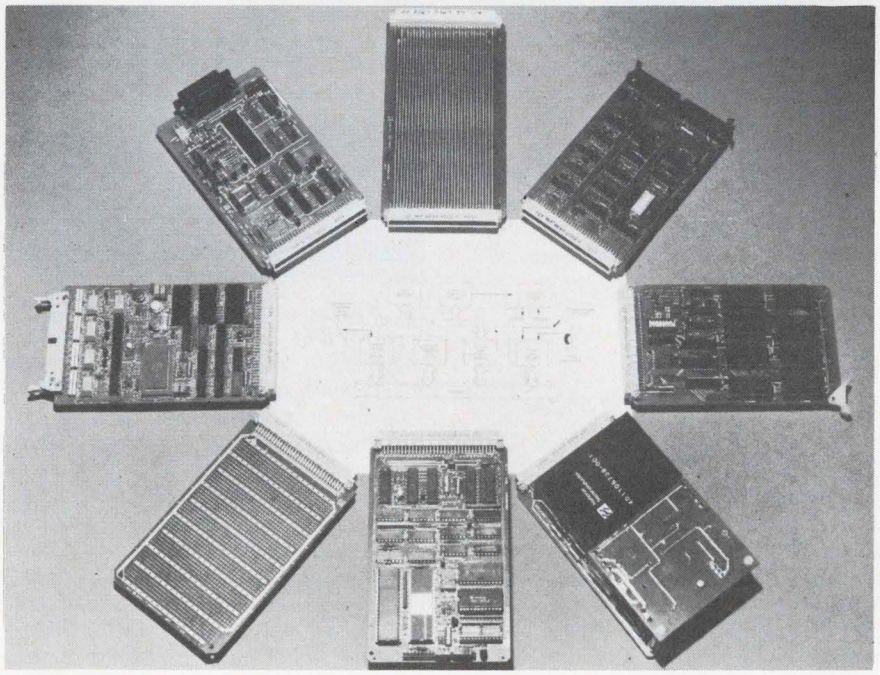


Fig 1: These new CMOS industrial μC boards are ideally suited for applications in harsh environments.

CP/M COMPATIBLE μC

Plug-Compatible With DEC VT-100

The system permits upgrading VT-100 or compatible terminals to run the vast library of available CP/M software. It features a 6 MHz Z80-B μP, 64K of dynamic RAM, a Centronics compatible parallel printer interface, two serial interfaces pin compatible with VT-100 terminals and existing host cable, and an integral

single/dual density floppy disk controller. Available in a variety of configurations including single or dual 8″ slim-line floppy disks, or with a 5 Mbyte Winchester disk and optional 8″ diskette. From $1995 to $4795. **D.A.T.A. Corp,** 396 W. Ironwood Dr, Salt Lake City, UT 84115. **Write 128**

MP/M II VERSION 2.1

Allows CP/M Application Programs To Run In Multi-User Environments

MP/M II version 2.1, for use with the Altos 8-bit microcomputers, has been modified by adding a compatibility attribute that enables the user to run application programs that are useable under CP/M and MP/M 1.13. Extended file locking is also a new facility that enables a user to maintain a lock on a file after the file is closed. **Altos Computer Systems,** 2360 Bering Dr, San Jose, CA 95131. **Write 126**

DEVICE DRIVER SOFTWARE

For Tektronix 4114 Terminals

This device driver software package allows users of PVI's DI-3000 Core-based graphics software tools to take full advantage of the many features of the Tektronix 4114 graphics terminal. It supports such 4114 capabilities as a segment data structure, picking, real-time segment dragging, and highlighting. Users can download fonts into the device, cutting down on I/O, and can create characters with exact hardware sizing. Written in 1966 ANSI Fortran IV, DI-3000 is an integrated system of 160 user-callable graphics subroutines. The system offers a full range of interactive graphics capabilities, including color, 3D, and a graphics data structure. License for the Tektronix 4114 device driver is $1000. **Precision Visuals,** 250 Arapahoe, Boulder, CO 80302. **Write 134**

TABLETOP COMPUTER

DEC Compatible System With Color Display

The COMPAT/23 consists of a DEC LSI-11/23 processor, 256 Kbytes of memory, 10 or 20 Mbyte 5¼″ Winchester disk, one or two 8″ double-sided double-density floppy drives, 14″ 7-color CRT display, VT-100 compatible keyboard and 3 async ports for printer, modem or additional displays. It supports limited color graphics for process diagrams, bar and pie charts. A wide variety of software products include RT-11, RSX-

11 and XENIX operating systems, a CORE graphics package and a relational data base manager. $14,900, qty discounts avail. **General Digital Industries,** 500 Wynn Dr, Huntsville, AL 35805. **Write 130**

16-BIT μC SYSTEMS

Based On The Z8001 And 68000 CPUs

Both units feature 256K of RAM, 15-slot backplanes, 40A power supply, dual 8″ floppy disk drives, and meet IEEE Multibus standards. Options for both systems include up to 16 Mbytes of RAM, Winchester hard disk drives, cartridge disk drives, and complete selection of terminals and printers. The X-8000 system, based on the Z8001 chip, offers 8 serial I/O ports, an operating system that supports from 1 to 32 users simultaneously (each running a different program), and as much as 250 Mbytes of on-line media storage. The X-6000 system, based on Motorola's 8 MHz 68000 CPU chip, is fully compatible with Intel's Multibus, handles up to 64K of onboard EPROM and 128K of onboard RAM, has 7 prioritized vectored interrupts and one non-maskable interrupt, two RS-232 serial I/O ports with 40 bits of parallel I/O and has a triple 16-bit timer/counter for generating interrupts or monitoring external events. From $7053. **Computex Microcomputer Systems Inc,** 5710 Drexel Blvd, Chicago, IL 60637. **Write 142**

COMPUTER SYSTEMS

Memory Capacity From 262K To 2097K 60-Bit Words

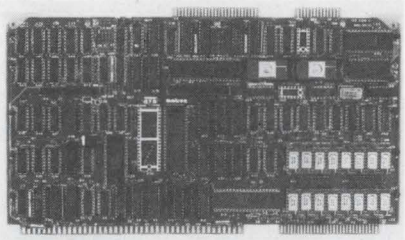
All five Cyber 170 Series 800 models have a cycle time from 400ns to 75ns and operate under the new NOS Version 2 Network Operating System. They run application software operating on the earlier Cyber 170 Series 700. Upper end Models 865 and 875 offer an optional second central processor and a new high-speed disk subsystem, the CDC 885-42, for very high performance levels. They oper-

ate with the broad range of existing Control Data peripherals that can be matched to individual system performance and application. Each system provides state-of-the-art capabilities for interactive, remote batch and transaction processing, as well as data base management in both commercial and scientific application environments. Purchase prices quoted are for minimum configuration of 10 peripheral processors, 12 channels and an operator console. From under $400,000 to $3 million. **Control Data Corp,** Box O, Minneapolis, MN 55440. **Write 127**

16-BIT MULTIBUS SBC

8086-Based Multibus CPU Card

The MBC-86/12 has been designed as an enhanced equivalent to Intel's ISBC-86/12. The two cards are fully software compatible. It includes a 5 or 8 MHz 8086 processor plus a sock-



et for an on-board 8087 coprocessor, 32 Kbytes or 128 Kbytes of on-board dual ported RAM, space for up to 32 Kbytes on-board ROM, 24 lines of parallel I/O, one RS-232C serial I/O port, and 2 programmable interrupt timers. Two expansion memory modules are planned for the 3rd quarter of this year. $1680, OEM discounts avail. **Matrox Electronic Systems Ltd,** 5800 Andover Ave, Montreal, Quebec H4T 1H4. **Write 132**

UNIX SYSTEM

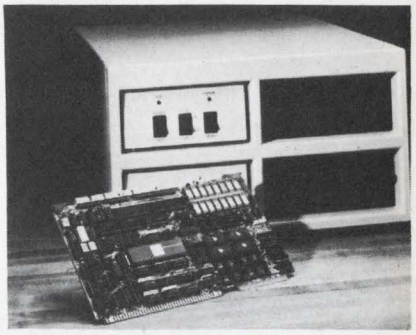
Virtual Memory Implementation For 68000-Based System

The Bell System OS will be offered with the Pixel 100/AP supermicro. UNIX System III offers software developers a strong base on which to build and deliver sophisticated turnkey supermicro systems. A typical 100/AP configuration incorporating UNIX System III, the C compiler, Programmer's Workbench (PWB), 40 Mbyte Winchester disk, and 4 Pixel terminals will be priced at under $15,000 in OEM qty. A packaged UNIX System III implementation with the PWB development utilities is $930 in single qty. **Instrumentation Laboratory Inc,** Pixel Div, One Burtt Rd, Andover, MA 01810. **Write 131**

DEVELOPMENT SYSTEM

For The MC68000 CPU

The OB68K/SYS is an IEEE 796 Bus (Multibus) based system designed to facilitate development of applications software for the MC68000, but is

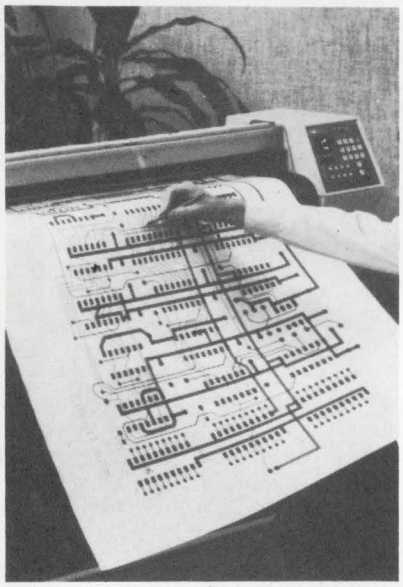


flexible enough to be used as a target system itself. The heart of the system is the OB68K1-128K SBC. It is equipped with 128 Kbytes of dynamic RAM (with hardware refresh controller), 8 sockets that can be user configured for up to 64 Kbytes of EPROM, 2 RS-232C serial ports, crystal controlled baud rate generator (50–19.2K baud), 2 software definable 16-bit parallel ports, and 3 16-bit timer/counters. Typical system pricing (with a 1 Mbyte floppy disk, 20 Mbyte hard disk, and development software) is under $12,000. **Omnibyte Corp,** 245 W. Roosevelt Rd, W. Chicago, IL 60185. **Write 133**

DRAFTING PLOTTER

Targets IC/PC Design Systems

Designed around the micro-grip drive technology on HP's D/Al-size drafting plotter, this E/AO-size HP 7585A features μP control, high resolution, excellent repeatability, 4g acceleration and speeds up to 24 in/sec (60

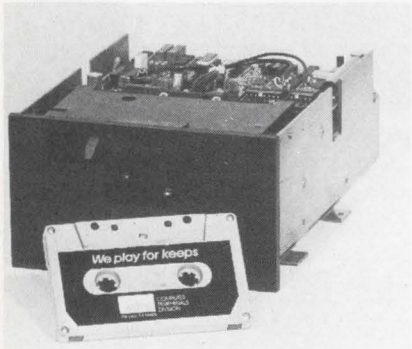


cm/sec). Applications include IC/PC design, electrical schematics, mechanical-parts design and facilities layout. The large-format plotter's built-in intelligence features enhance both programmer and operator productivity, reduce support costs and eliminate many host-CPU tasks. $22,750. **Hewlett Packard,** 1820 Embarcadero Rd., Palo Alto, CA 94303. **Write 188**

10 MBYTE TAPE CASSETTE

Backup System For 5-¼" Winchesters

The Companion series tape cassette system can store up to 10 Mbytes in just 4 minutes on a single tape cassette with a reliability factor of BER

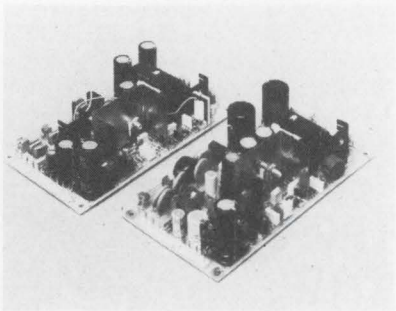


-10^{10}. Available in a 5 Mbyte model (505) and a 10 Mbyte model (510). MFE's backup features reel-to-reel drive for uniform tape tensioning, maximum operational reliability and data accuracy. The improved design eliminates the need for pretensioning or tape conditioning, and read-after-write capability allows for data comparison and improved data recovery. **MFE Corp.,** Keewaydin Dr., Salem, NH 03079. **Write 186**

POWER SUPPLIES

Solves CRT Interference Problems

The XL51 and XL53 switching power supplies eliminate the noise and interference problems commonly encountered in systems using CRT displays. The XL51 delivers the 45W of power normally required by "dumb" terminals, and the XL53 delivers the 65W required by "smart" terminals. These



4 output, open frame units incorporate a new proprietary current controlled feedback network to achieve tight regulation and low ripple and noise which guarantee a flicker-free CRT screen. Both have short circuit protection and input surge current protection (soft start). The XL51 is $98 and the XL53 is $120 in 500 qty. **Boschert Inc.,** 384 Santa Trinita Ave., Sunnyvale, CA 94086. **Write 189**

TAPE BUFFERING/SWITCHING

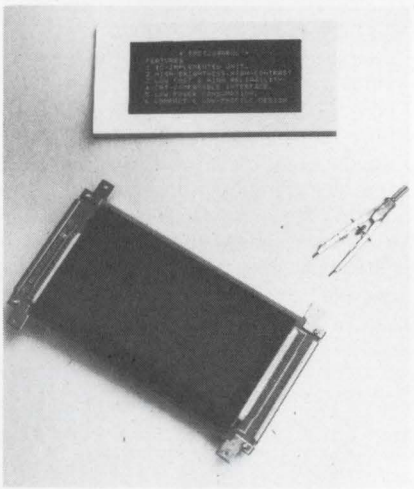
For IBM-Compatible Processors

The 32 Kbyte buffering feature, STC 4500, increases the throughput capability of tape subsystems, especially when attached to data-streaming channels. For example, when using 125 ips drives, the throughput capability of each tape channel increases from 780 Kbytes/sec to over 1,560 Kbytes/sec. Buffered tape control units also achieve higher effective data rates while using fewer dedicated channels. Other types of peripherals can coexist on the same channels as the STC 4500 control unit without the serious degredation associated with non-buffered controllers. $12,000. **Storage Technology Corp.,** 2270 S. 88th St., Louisville, CO 80027. **Write 190**

PLASMA DISPLAY

High Contrast Panel

The FPC 4012 NRUL is an easy-to-view, high brightness, 480 character AC memory type display panel. It uses dielectric strength monolithic ICs for the drive circuits and CMOS LSIs for control logic. The panel has



orange characters on a black face, providing high contrast characters that can be easily read in brightly lighted areas. A CRT-compatible interface permits the display unit to be easily connected to various system buses through a CRT controller. **Fujitsu America, Inc.,** Component Div., 918 Sherwood Dr., Lake Bluff, IL 60044. **Write 193**

LOGIC SYSTEM

Combines Data Development, Device Programming And Functional Testing

A modular system for simplifying the programming and functional testing of programmable logic devices. The Programmable Logic Development System (PLDS), supports over 60 programmable logic devices such as PALs, FPLSs, FPLAs and FPGAs from manufacturers including AMD, Harris, MMI, National, Signetics and Texas Instruments. The PLDS's high-level data development software allows the user to specify logic designs

in truth tables or Boolean equations and key them into the system from a terminal. Then the PLDS translates the user's design into the fuse table needed to program the device. **Data I/O,** Box 308, Issaquah, WA 98027.

Write 192

INTELLIGENT TERMINAL

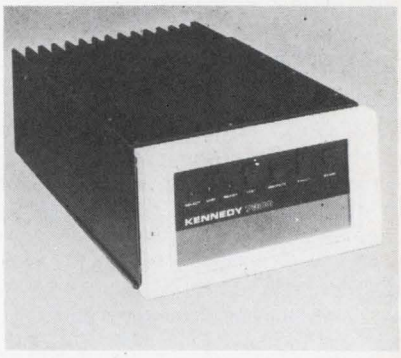
Features Local Processing, Communications

Users can customize the Intelligent I to serve as a computer station for local processing, an intelligent front-end for transaction processing applications, and as a node in communications networks. It has 64 Kbytes of RAM for program storage or local processing; a Z80A μP compatible with the extensive library of CP/M-based applications programs; and local and long-distance communications capabilities. Depending on a user's requirements, the terminal can economically perform the functions of a small computer, a communications device or a high-performance display terminal. $1795; qty discounts avail. **TeleVideo Systems Inc,** 1170 Morse Ave, Sunnyvale, CA 94086. **Write 214**

80 MBYTE WINCHESTER

Occupies Only 0.32 Cu.Ft.

Model 7380 is just 4.62″ high to further conserve front panel space. Two disks may be placed side by side in a standard 19″ Retma Rack, giving 165.8 Mbyte unformatted storage for small systems. Employing composite-material R/W heads, Model 7380 has



a track density of 960 tpi with 823 cylinders-per-surface and a recording density of 9420 bpi. Data transfer rate is 1.209 Mbytes/sec, making the drive compatible with industry standard storage-module device controllers. It employs Kennedy's PosiTrack rotary actuator for fast head positioning and precise track following. Minimum seek time is 6 ms with average and maximum seek times of 30 ms and 55 ms, respectively. A 3600 rpm spindle speed gives an average 8.33 ms rotational delay. $2795 ea. in 500 qty. **Kennedy Co,** 1600 Shamrock Ave, Monrovia, CA 91016. **Write 211**

Write 26 on Reader Inquiry Card

PERIPHERAL INTERFACE

Can Be User-Customized; Doubles On-Chip ROM, RAM

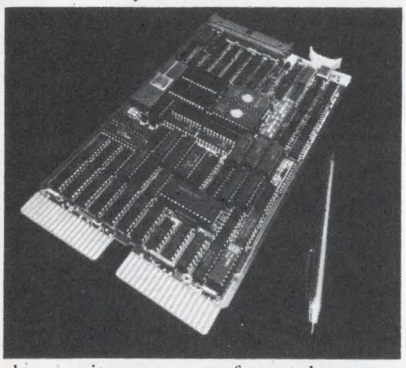
The UPI-42 (8042) is a general-purpose universal peripheral interface (UPI), an intelligent peripheral controller that can be easily customized by the user. The single-chip microcomputer contains 2 Kbytes of ROM program memory, 128 bytes of RAM, 18 I/O lines and a 12 MHz clock. It is available in an ultraviolet EPROM version: the 8742. The 8042/8742 can be designed into systems based on Intel's 8- and 16-bit μPs to control a variety of peripheral devices such as matrix printers, keyboards, and motors. The 8042 UPI is $11.95 in plastic (500 qty). A one-time mask charge is $3000. The EPROM version 8742 is $56.75 (100 qty). **Intel Corp,** 2625 Walsh Ave, Santa Clara, CA 95051.

Write 165

DUAL-WIDE CARD

Controls Both Winchester And Floppy Disk Files

As an alternative to DEC controllers RL01, RL02, and RX02, WINC-05 emulates the functions of all three DEC controllers for rigid and floppy disks. It may be ordered as a stand-

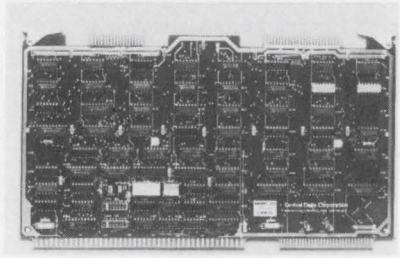


alone unit or as part of a total system, including disk drives. Available as a dual-wide for Q-bus interfacing (LSI-11 minis), and a quad-wide version for Unibus interfacing (PDP-11 minis). Support is provided for either 5MB or 10MB 5¼" Winchester drives, and 5¼" double-density floppy disk drives. The system performs burst data transfer at 625 Kbytes/sec. Data transfer over the entire disk is 259 Kbytes/sec. Up to 4 drives, in a variety of Winchester and floppy disk combinations, may be controlled by a single WINC-05. Under $2000; a typical system with 10MB Winchester and one 5¼" floppy is $6800. OEM qty discounts avail. **Advanced Electronics Design,** 440 Potrero Ave, Sunnyvale, CA 94086. **Write 159**

CARTRIDGE/TAPE CONTROLLER

For Multibus Systems

This board allows the user to add extensive file handling capabilities to any Multibus system. It works with an IMI Intelligent disk and a DEI streaming tape unit, both controlled

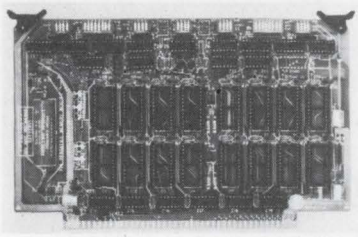


by the same board. The IMI drive is available in 10, 20 or 40 Mbytes and the tape drive, which serves as a backup for the Winchester disk, has 20 Mbytes of on-line disk storage. **Central Data Corp,** 1602 Newton Dr, Champaign, IL 61820. **Write 162**

32K MEMORY MODULE

Accepts CMOS, NMOS And EPROM

Replacing up to 3 different memory modules in a system card cage, this high-density module accepts up to 32K x 8 of CMOS or NMOS RAM or EPROM/ROM devices, configured in 4 independent 8K banks. Each of the board's 16 2K x 8 sockets may accommodate any of the 3 types of devices, interchangeably. On-board power-fail circuitry, write-protect circuitry and a lithium battery allow the module to retain non-volatile memory up to 10 years (at 23° C). Double write protect circuitry guarantees against accidental writes caused by power cycling or transients. Each independent 8K bank, or block, contains base address, enable/disable and write pro-

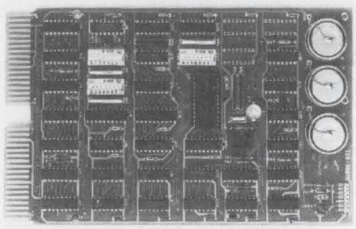


tect switches. Sixteen additional switches allow each device to be enabled or disabled. The GMS6524 is $285 (10-24 qty); $223 (100 qty); fully populated with CMOS devices it is $477 (10-24 qty). **General Micro Systems Inc,** 1320 Chaffey Ct, Ontario, CA 91762. **Write 164**

TIMING CONTROL UNIT

For LSI-11 Minicomputers

The TCU-50DYR option is a combination real time, crystal-controlled calendar clock and 1k CMOS memory on a single plug-in board. Its self recharging batteries maintain clock operation and memory storage for up to three months without an external power source. It has extensive interrupt capabilities. Interrupts can be generated for a wide range of time intervals from 1/10 second to a second, minute, hour, day, week or month, and they can be set at any time of



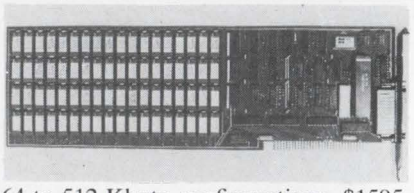
day. The 1 Kbyte of non-volatile CMOS memory can be used to store data registers during power down sequences. In the power down mode, the clock can be set to generate a signal at a particular time. Alarm functions can also be latched to the unit. $325. **Digital Pathways,** 1060 E. Meadow Circle, Palo Alto, CA 94303.

Write 163

512 KBYTE MEMORY

With RS-232C Port

The CI-PCM+ memory/serial I/O module is designed using state-of-the-art 64K bit NMOS dynamic RAM technology. It requires only one I/O expansion slot for 512 Kbytes of memory with parity. The RS232-C port frees one I/O expansion slot allowing the user to add 512 Kbytes of memory to the personal computer requiring no extra I/O expansion slot. It is addressable in 64 Kbyte increments throughout the 1 Mbyte address field of the IBM Personal Computer. The memory has an access time of 225 ns and cycle time of 400 ns. Available in



64 to 512 Kbyte configurations. $1595 (512 Kbyte). **Chrislin Industries Inc,** 31352 Via Colinas #101, Westlake Village, CA 91362. **Write 161**

5¼" WINCHESTERS

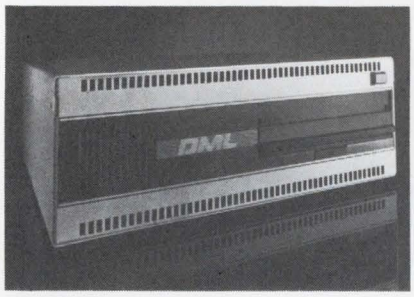
Fast Access Time

The 516 drive offers 16 Mbyte capacity unformatted (13.2 Mbyte formatted) and comes complete with an integral cartridge tape backup system. Average access time is 30 ms including move and settling time. $1794 (500 qty). The 416 drive is a disk-only version of the 516—also offering 16 Mbyte unformatted, but without the tape drive. $1140 (500 qty). Two new controllers are also offered. The 1511 provides all necessary functions to integrate up to two of either the 516 drive or the 510 drive. $585 (500 qty). The 1411 controller is a single board for the 416 drive. $417 (500 qty). **Irwin International Inc,** 2000 Green Rd, Ann Arbor, MI 48105. **Write 210**

8" WINCHESTER

For Intel μP Development Systems

This 8" Winchester provides 26.2 Mbytes when formatted, to be compatible with Intel's operating system. Model 1040 provides up to a 3× improvement in performance compared to double density floppies. It emulates standard Intel devices to main-



tain total software transparency. A single card Multibus interface saves card slots. A powerful backup/restore utility allows for quick and convenient backup of whole data bases or selected projects. $8200; an optional 8" floppy drive is $1000. **Data Management Labs,** 2148 Bering Dr., San Jose CA 95131. **Write 187**

STORAGE CELLS

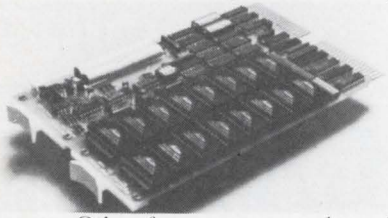
Provide Integrated Mass Memory Backup

The XSC family of Storage Cells allows combining primary and secondary mass storage peripherals into a single physical unit. The XSC100 Series provides a combination of one or two Winchester disk drives with a ½" streaming tape which can be used as backup or media-compatible data transfer, giving users up to 320 Mbytes of on-line storage capacity. The XSC200 Series combines two 8" Winchester disk drives—one a 10 Mbyte removable disk and the other a 40 Mbyte fixed disk. The XSC220 Series uses two fixed 70 Mbyte Winchester disk drives. The XSC240 Series combines up to 70 Mbytes of Winchester disk storage capacity with 17 Mbytes of on-line cartridge tape storage. They are configured with all necessary controllers and power supplies within the standalone cabinets. **Xylogics Inc,** 144 Middlesex Tpke, Burlington, MA 01803. **Write 215**

LSI-11 ADD-IN MEMORY

Provides Either 16 or 32 Kbytes

Employing CMOS RAM and on-board batteries, the MM-1103C is a non-volatile add-in memory for LSI-11/2-11/23 μCs. To ensure non-volatile capability it monitors the +5V power line and issues a BHALT/ upon power failure or shutdown, which causes the CPU to go into a Halt mode. On-board batteries are then switched on to provide backup

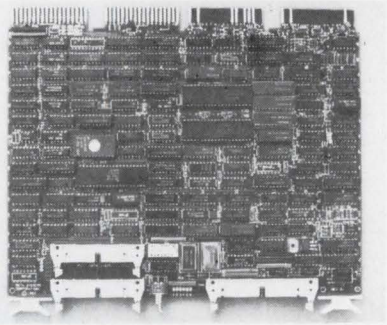


power. Other features are: cycle and access time of 220 ns, 22-bit addressing, Q-bus compatible data inputs and outputs, and module selection on 1Kbyte boundaries in the 4 Mbyte address field (switch-selectable). $875 (32 Kbytes). **Micro Memory Inc,** 9436 Irondale Ave, Chatsworth, CA 91311. **Write 167**

WINCHESTER CONTROLLERS

Seagate And SA1000 Controllers For LSI-11 Series

Model 5121 interfaces 5-¼" disks with the Seagate standard, Model 5122 interfaces 8" disks with the Shugart



SA1000 standard. Each supports up to 4 drives and provides from 5 to 40 Mbytes of formatted disk storage without any software development or changes to the DEC operating system. They emulate a DEC RLV-11 attached to RL01/02 disk drives and use standard DEC supplied RLV-11 diagnostics. Features include an on-board formatter, bootstrap loader, and elaborate self-test features. $1995 plus cabling. **Datasystems Corp,** a Wespercorp subsidiary, 10072 Willow Creek Rd, San Diego, CA 92131. **Write 185**

EVALUATION CHIP

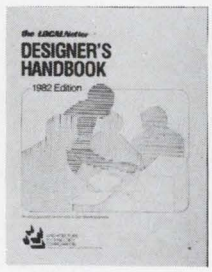
To Test Performance of Q-700 Bipolar Gate Arrays

The Q-700 bipolar gate arrays are high speed, full military temperature range TTL products. The Q-700 Array Evaluation Chip (AEC) is designed using the standard Q-700 1000-gate ECL/TTL array. It helps systems designers determine the performance of Q-700 macros and various I/O configurations by demonstrating the characteristics of Q-700 array systems under actual application conditions. Prospective users can evaluate Q-700 products before committing themselves to a design. Sets of two identical chips, sockets, and support literature is $300; additional chips are $75 each. **Applied Micro Circuits Corp,** 8808 Balboa Ave, San Diego, CA 92123. **Write 157**

Prosys I Control System Variations. Features that permit almost 1,000 system configurations of ADAC's Prosys I multitasking data acquisition and control system are highlighted in this 4 pp. full color brochure. Described are RAM memory options from 64K to 256 Kbytes plus battery back up CMOS RAM. Thirty features of LSI-11/2 and LSI-11/23 based systems for laboratory, process, rest, measurement and other applications are also listed.
ADAC Corp **Write 250**

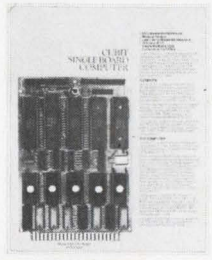
APPS/2 Brochure. APPS/2, a second generation computer system which automatically produces NC part programs is described and illustrated in a new 4 pp. brochure. Complex, two dimensional forms are defined simply by tracing the form. APPS/2 is applicable to X, Y single pass operations, such as milling, laser and flame cutting, routing or welding.
Alden Computer Systems **Write 251**

Series 4000 Literature. This data sheet summarizes the different types of graphics processing facilities, workstations, plotters, and peripherals included in the Series 4000 family of CAD/CAM systems. Applicon's Distributed Graphics Network (DGN) capability; operating system software; graphics applications software; and industry-specific application software are also described.
Applicon **Write 252**



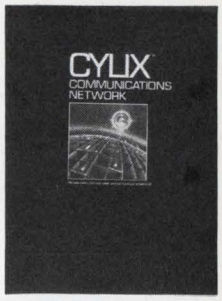
LOCALNetter. The 1982 LOCALNetter Designer's Handbook is a 224 pp. guide to local network specification and design. The Handbook includes: product descriptions, articles on local network standards, discussions of major design issues, sample specifications, equipment features comparision charts, manufacturers listings, and an extensive bibliography.
Architecture Technology **Write 253**

"OmniSystem". An "overview" brochure describes a broad new concept in data acquisition and control called "OmniSystem." Designed to fulfill virtually all process interface needs, "OmniSystem" is used in such fields as chemicals/petrochemicals, simulation, and power generation (including Class 1E and seismic qualification).
Computer Products **Write 254**

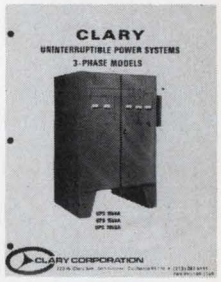


Expanded Microcomputer Line. This brochure describes Cubit's expanded microcomputer line, designed for industrial control applications, and featuring software compatibility with Rockwell's AIM-65. New boards announced in this brochure include: a memory board, a universal I/O expander, parallel I/O expander, and a 5-slot motherboard.
Cubit Inc. **Write 258**

Private Network Cost Analysis. A brochure analyzing the cost of implementing and maintaining a private data communications network. Entitled "Network Cost Analysis," pinpoints six key cost areas—staffing, corporate allocations, nodes, leased lines, modems, and equipment. It provides users with a formula for figuring their own per-drop and overall network costs.
Cylix Communications Network **Write 259**

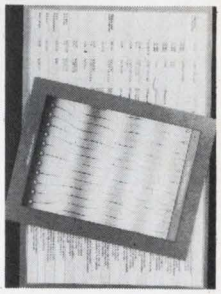


UPS 3-Phase Brochure. This new 3-phase model brochure provides a detailed description of the 10, 15 and 30kVA UPS. In addition to a general overview of power problems and how a UPS operates, this brochure offers a complete specification chart for those seeking technical information. Also contained in the 4 pp., color brochure is a listing of the model's advanced design features and their benefits.
Clary Corp. **Write 260**



D/S Converter. The first low-profile (0.42-inch), 16-bit, microprocessor-compatible digital-to-synchro (resolver) converter is described in this 4 pp., 2-color data sheet. In addition to its compact package, this 16-bit converter offers both 8 and 16-bit microprocessor compatibility. Both input and output are transformer isolated. The data sheet includes features, description, specifications and ordering information.
Natel Engineering Co. **Write 267**

Modem Brochure. This 12 pp., full-color brochure describes Codex's full range of modem products. Included are local distribution modems, new CS Series network control modems, low-speed Bell-compatible modems, medium and high speed modems, and the greater than 9600 bps modems. There is also a special section on modem-related peripheral devices, and a fold-out reference chart.
Codex Corporation **Write 255**

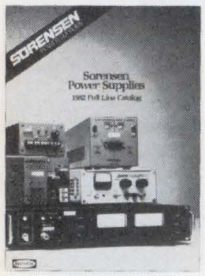


Gate Array Manual. This 227 pp. design manual covers oxide isolated Si-Gate CMOS (ISOCMOS) technology. A number of design aids such as planning sheets, 200X layout sheets, test development formats, special interconnect pencils, a logic symbol template, and evaluations specifications are provided. $69.00.
Universal Semiconductor **Write 276**

CDS 212 Modem. A new 4 pp. technical data sheet describes the features of the 1200 bps full duplex dial modem.
The CDS 212 utilizes high speed, low power μPs to perform signal processing and control. Advanced signal processing techniques, implemented via software, significantly reduces component count and power consumption.
Concord Data Systems **Write 256**

New Literature

Power Supply Catalog. This 8 pp. catalog provides electrical/mechanical specifications, features, photos, and ordering information for the division's line of 162 AC/DC linear and switching power supplies, and DC/DC converters. The catalog also includes details on the newest additions to Power Products' power supply line—a series of low-cost, semi-regulated DC/DC converters.
Power Products **Write 268**



Sorensen Power Supplies. The 1982 product-line catalog contains diagrams, dimensional drawings, and specifications for power supplies in four categories: modular power supplies, power assemblies, power instrumentation, and digital-to-analog programming. In addition to product descriptions, the catalog contains an engineering introduction with information on principles of operation, operating features, and verifying specifications. 128 pp.
Sorensen Co. **Write 275**

Case Study Brochure. The first digital computer-based system to acquire and analyze aerodynamic pressure data is the subject of this four-color brochure. Described is an application case study where Science Applications, Inc., is using a HARRIS 800 super-minicomputer to digitally analyze distortion patterns on jet engine inlet ducts.
Harris Corporation **Write 263**

Multidropping. An 8 pp. color brochure describes the Micro900 Multidrop Concentrator, designed to let minicomputer users garner the economies of polled multipoint communications and statistical multiplexing. Presented are such topics as transparent polling in a minicomputer environment, statistical multiplexing, expansion and reconfiguration.
Micom **Write 266**

Synchro Converter Guide. A new 4 pp. short form guide covers over twenty series of synchro, resolver and inductosyn (TM-Farrand Controls) converters. The guide contains summary performance data on each product series, organized to assist engineers in matching device types to specific applications.
Control Sciences **Write 257**

Capabilities Brochure. An 8 pp. brochure describes the development and manufacture of high-density EPROMS, microcomputers, microprocessors incorporating nonvolatile memory circuits, and advanced nonvolatile electrically erasable devices (E^2ROM) The literature includes discussions of Seeq's 16K E^2ROM, 64K UV EPROM and the Silicon Signature, which encodes programming algorithms, fabrications facility and mask set numbers on the nonvolatile memory for access by programmers.
Seeq Technology **Write 271**

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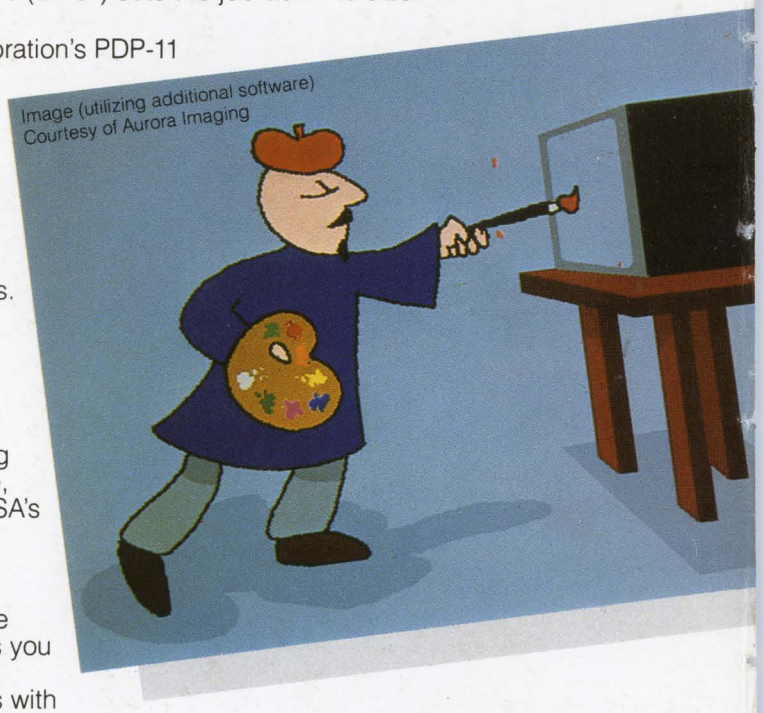

Image (utilizing additional software) Courtesy of Aurora Imaging

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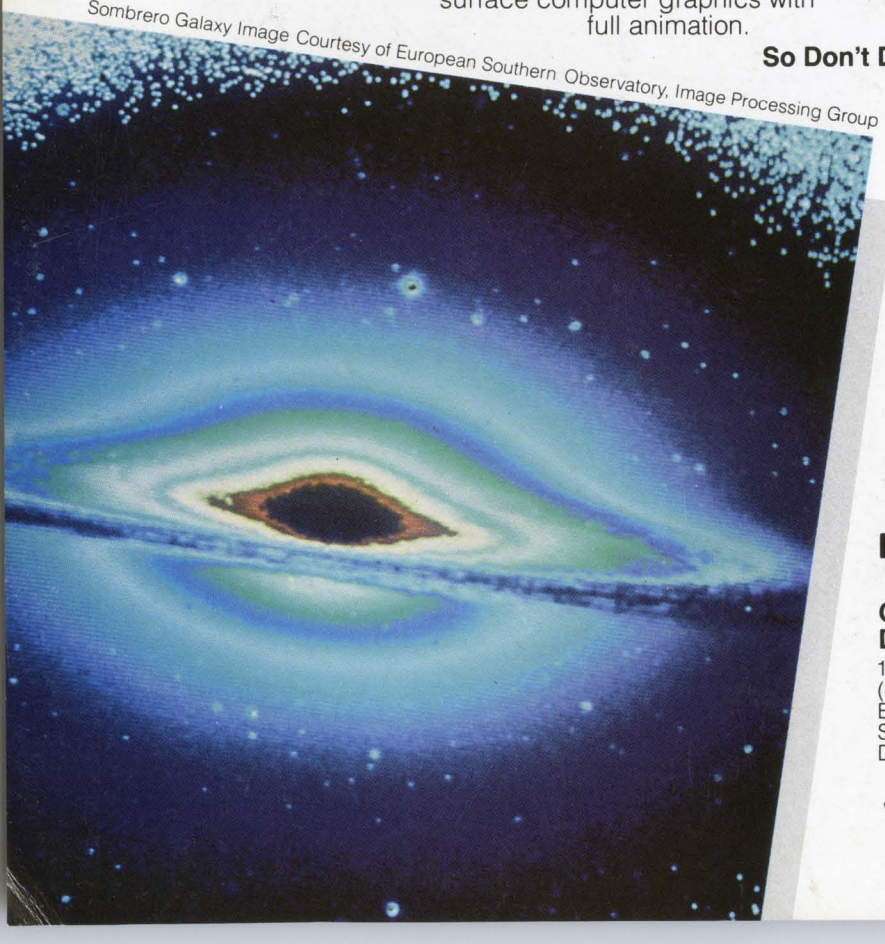

Sombrero Galaxy Image Courtesy of European Southern Observatory, Image Processing Group

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