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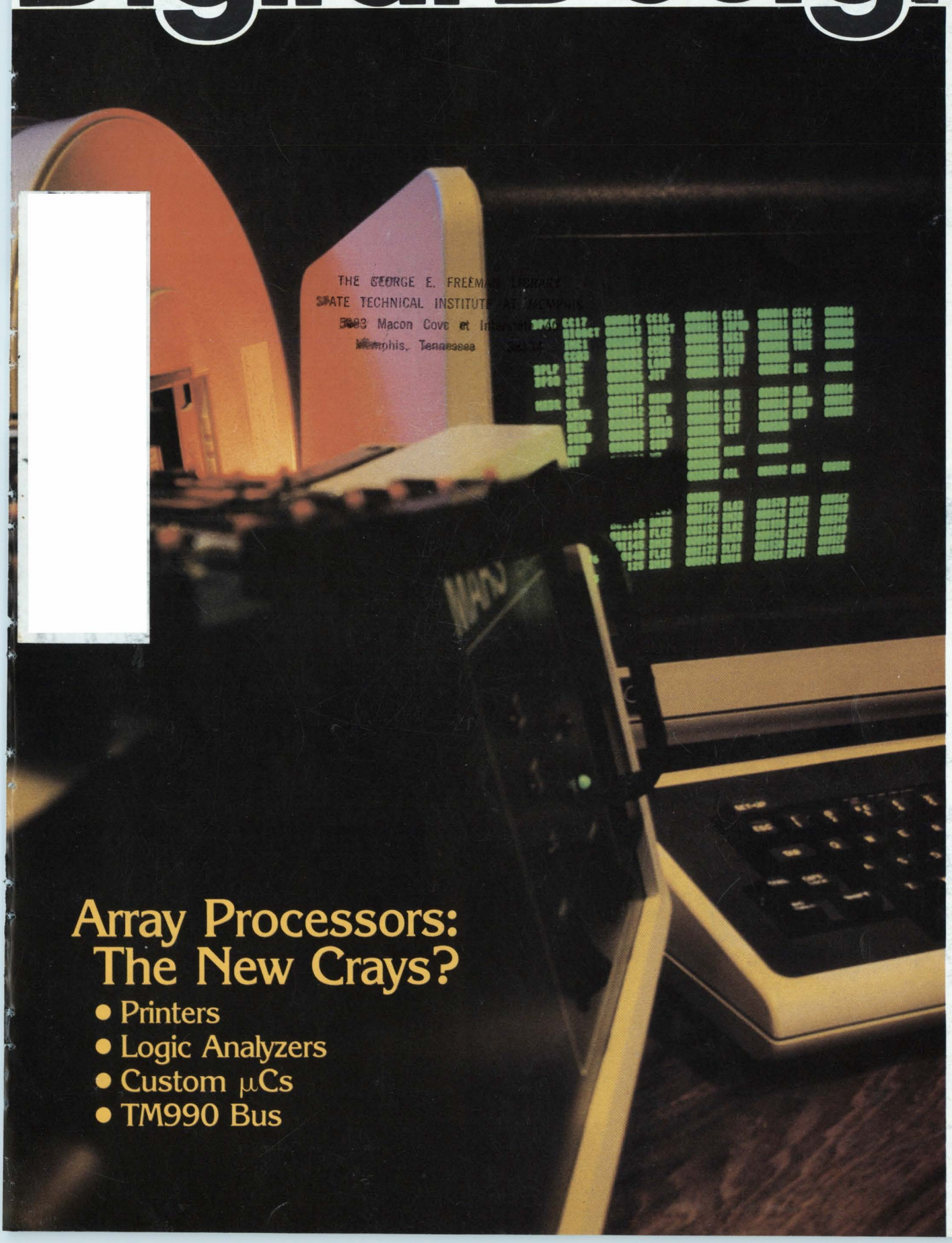
Digital Design



Array Processors: The New Crays?

- Printers
- Logic Analyzers
- Custom μCs
- TM990 Bus

COMPUTERS/SYSTEMS · PERIPHERALS · COMPONENTS · 12/82

VOL. 12
NO. 13

HOLD MEMORY COSTS IN CHECK.

Ever feel rooked by memory prices? Well, you can play the game for less if you make the move to Plessey.

We've just converted our entire memory production to CAD/CAM. That means greater capability, even more consistent quality, and something else—low price.

In fact, when you buy Plessey memories, you get the first one at the 100-unit price. Like a PDP-11/44 1 Mbyte ECC for $2580. Or an LSI-11 SV128 256 Kbyte for $630. Or even a VAX S730 1 Mbyte only $2665.

The savings are the same on all our boards. Core and MOS. 16 Kbytes to 1.0 Mbytes. With Omnibus, Unibus, Q-bus, MJ11, SJ-780, or NOVA bus chassis compatibility.

In fully populated and depopulated versions. Plus, every Plessey memory comes with a free 1-year warranty. And if we install your memory for you, you also get free on-site repair for 30 days.

But chances are you'll never have any problems. Because we inspect and test every memory we make.

So if you want to hold your memory costs in check, mate your system with Plessey. It's the only move you need to remember.

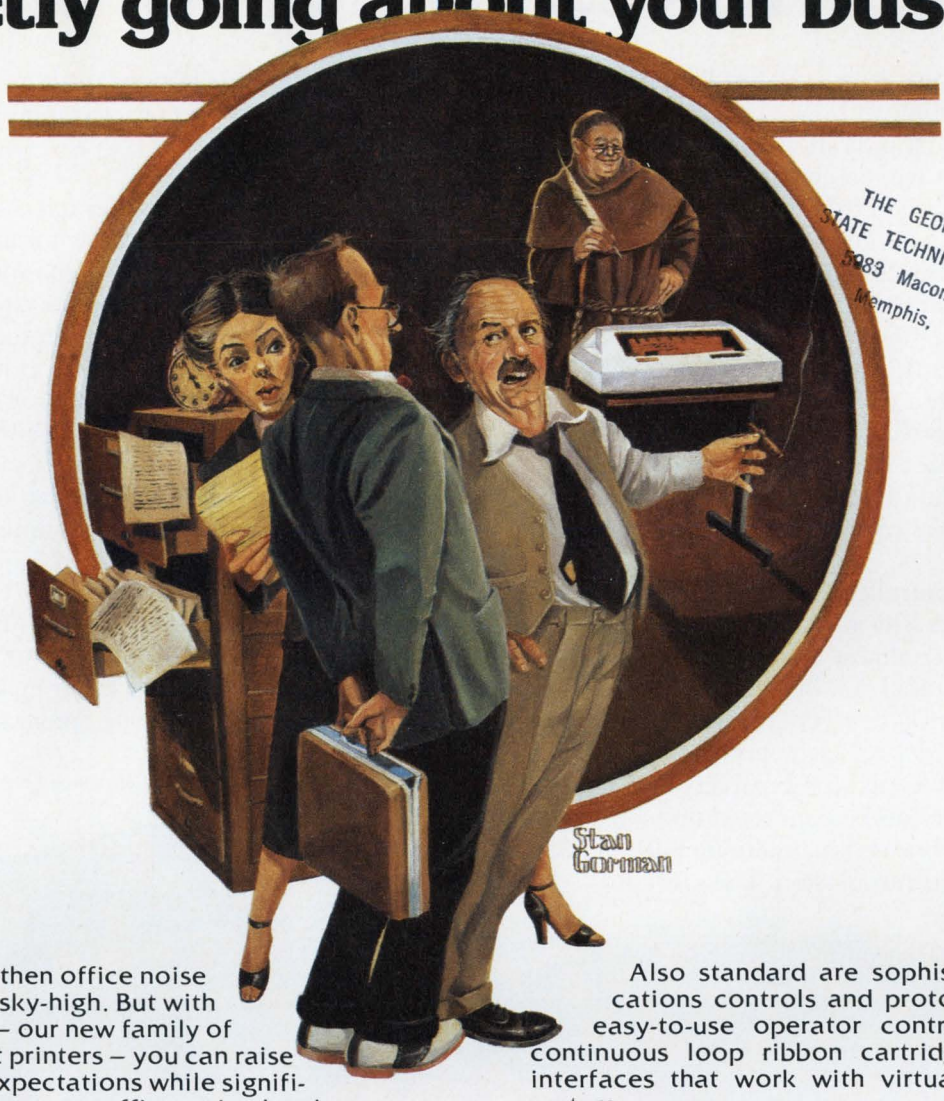
Plessey Peripheral Systems
1674 McGaw Avenue, Irvine, CA 92714
(714) 540-9945

Prices are applicable in U.S. only.

PDP-11, LSI-11, VAX, Omnibus, Unibus and Q-bus are registered trademarks of Digital Equipment Corporation. NOVA is a registered trademark of Data General Corporation.

Write 9 on Reader Inquiry Card

Anadex SILENT/SCRIBE™ printers. Quietly going about your business.



Now and then office noise levels can go sky-high. But with Silent/Scribe – our new family of matrix impact printers – you can raise your printer expectations while significantly lowering your office noise level.

How quiet is "silent"? Silent/Scribe operates at less than 55 dBA, which means that in the average office you may have to look at it to determine whether it's printing.

SILENT/SCRIBE MODELS

Standard Features	Char. per Inch	DP-9000A	DP-9500A	DP-9001A	DP-9501A	DP-9620A
Printing Speed (Char. per Sec.)	10	150	150	120	120	200
	12	180	180	—	—	120
	12.5	—	—	150	150	—
	13.3	200	200	—	—	—
	15	—	—	180	180	150
	16.4	—	—	200	200	164
Enhanced	10	—	—	—	—	100
Expanded Print (Double Width)		Yes	Yes	Yes	Yes	Yes
Dot Addressable Graphics (Dot/In., H/V)		60/72	60/72	75/72	75/72	72/72
Max. Line Width (In.)		8.0	13.2	8.0	13.2	13.2
Audible Alarm		Opt.	Opt.	Opt.	Opt.	Yes
Out-of-Paper Sense		Yes	Yes	Yes	Yes	Yes
Ribbon, Continuous Loop Cartridge (Yds)		30	30	30	30	30
Interfacing:						
Parallel Cent. Comp.		Yes	Yes	Yes	Yes	Yes
RS-232-C Serial		Yes	Yes	Yes	Yes	Yes

And Silent/Scribe is as easy to buy as it is to live with. You can select a variety of printing speeds, fonts and line widths. Some models provide both draft and enhanced quality copy. All models have superb dot-addressable graphics at no extra cost.

Also standard are sophisticated communications controls and protocols, flexible and easy-to-use operator controls, quick-change continuous loop ribbon cartridge, and universal interfaces that work with virtually any computer system.

For full details on how Silent/Scribe can fit your application – quietly – contact Anadex today. You'll find the units attractively packaged, quality engineered, modestly priced, and available now.

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MADE IN USA FOR THE WORLD

DP-9000A

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Line Printer Controllers that test themselves-

MDB makes the difference!

Only MDB has Line Printer Controllers that are completely self testing with PrinTest,™ Loop Back and LED's for visual indication of the data being transmitted. You save maintenance costs and down time. MDB's exclusive PrinTest feature, when activated by an edge mounted toggle switch allows you to exercise the controller's printer interface, interconnection cable and all parameters of the printer (except VFU). Then flip a second switch for Loop Back which causes the controller to function as if in full operation with a printer, while, in fact, the printer is disconnected. You verify controller operation or trouble shoot the module without noise, paper waste or confusion. And the PrinTest feature on MDB controllers can be remotely activated from the printer.

MDB printer controllers can be supplied with a Centronics, Dataproducts, or Data Printer interface, so you can connect almost any printer to a PDP*-11, VAX*, LSI-11/2 or 11/23, PDP-8, NOVA, Eclipse, HP-1000, IBM Series/1 or Perkin Elmer computer. A 15' cable is supplied with each controller.

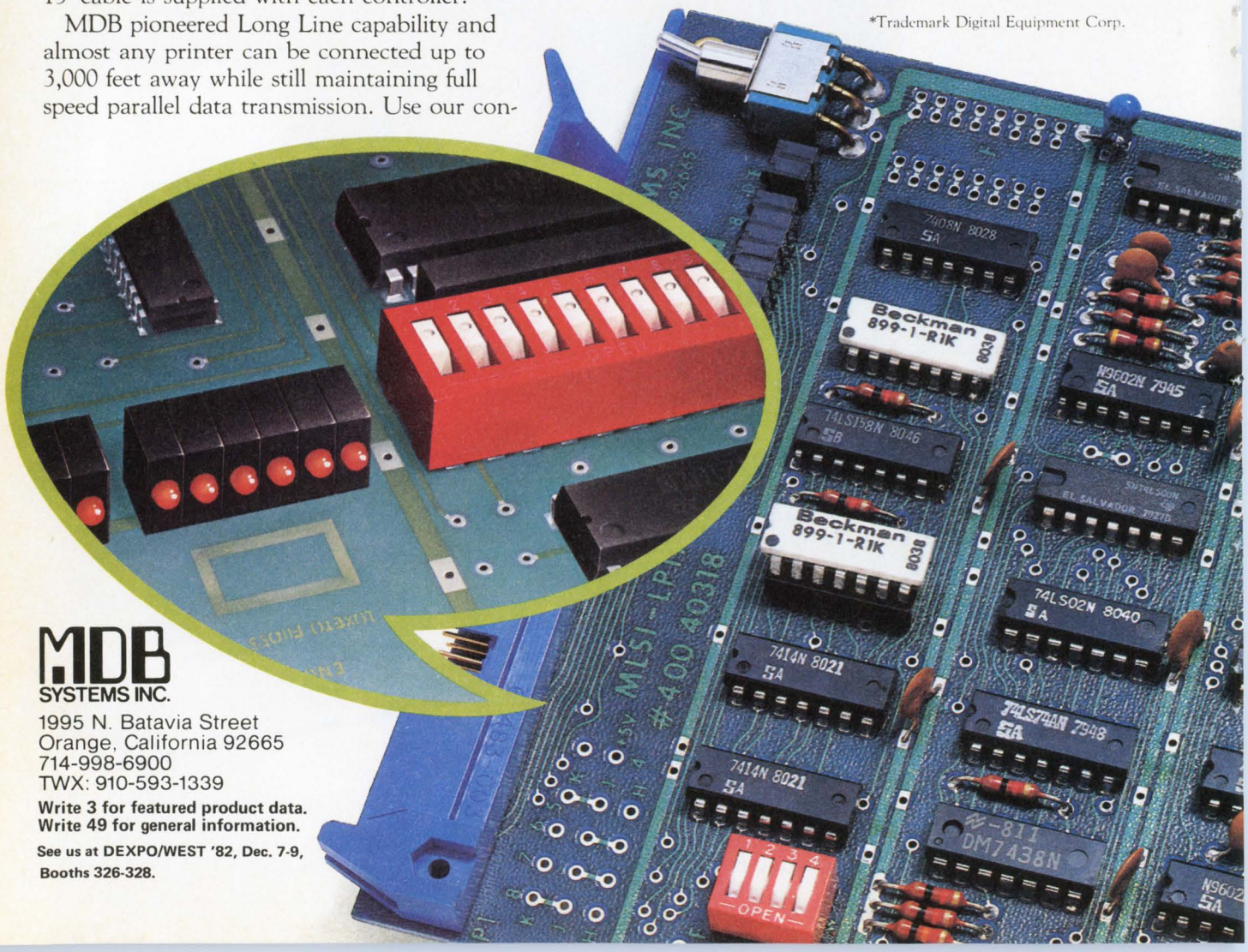
MDB pioneered Long Line capability and almost any printer can be connected up to 3,000 feet away while still maintaining full speed parallel data transmission. Use our controllers with Long Line options, or use our various long line interface products to accomplish remoting of your printer.

If your printer has a serial RS-232 or 20 MA current loop interface, then consider our Asynchronous serial interfaces. They are available for all of the major mini-computers. Most MDB serial interfaces have a Printer Busy/Buffer Ready monitor circuit. So if your printer sends out X-on/X-off protocols and the software doesn't use them, or if the printer doesn't send them, but the software looks for them, we won't let you down. As long as your printer toggles a buffer full status line, we will stop sending data when the printer can't take it. Most MDB serial interfaces also have RS-422 circuitry for remote terminal applications.

Our boards are warranteed for a full year, many are available off the shelf and they can be purchased under GSA contract #GS-OOC-03330.

Want to see the difference we can make in your system? Call or write for all our Specifications.

*Trademark Digital Equipment Corp.



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SYSTEMS INC.
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Orange, California 92665
714-998-6900
TWX: 910-593-1339

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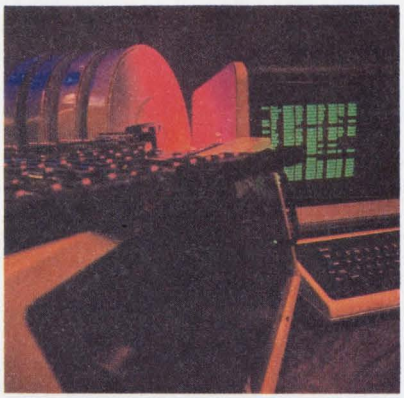
Write 49 for general information.

See us at DEXPO/WEST '82, Dec. 7-9, Booths 326-328.

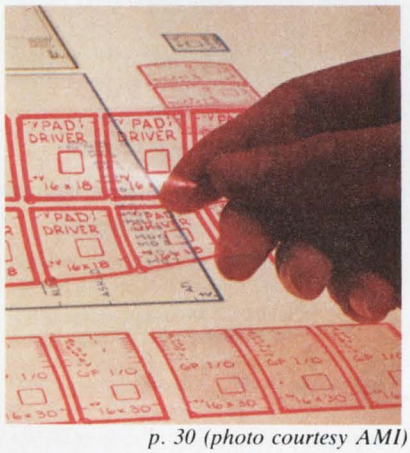
DECEMBER 1982/VOL. 12, NO. 13

Digital Design



p. 22 (photo courtesy Numerix)

p. 53 (photo courtesy Gould)



p. 30 (photo courtesy AMI)

Cover

The fixed-point array processor pictured on this month's front cover is just one of the many types discussed in our array processor feature, beginning on page 22 (photo courtesy Numerix)

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COMPUTERS/SYSTEMS

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WHAT'S BETTER THAN SPEED READING?

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Speed Learning is replacing speed reading. It's easy to learn...lasts a lifetime...applies to everything you read...and is the only accredited course with the option of college or continuing education credits.

Do you have too much to read and too little time to read it? Do you mentally pronounce each word as you read? Do you frequently have to go back and re-read words or whole paragraphs you just finished reading? Do you have trouble concentrating? Do you quickly forget most of what you read?

If you answer "yes" to any of these questions — then here at last is the practical help you've been waiting for. Whether you read for business or pleasure, school or college, you will build exceptional skills from this major breakthrough in effective reading, created by Dr. Russell Stauffer at the University of Delaware.

Not just "speed reading" — but speed reading-thinking-understanding-remembering-and-learning

The new *Speed Learning Program* shows you step-by-proven-step how to increase your reading skill and speed, so you understand more, remember more and use more of everything you read. The typical remark made by the 75,000 slow readers who completed the *Speed Learning Program* was: "Why didn't someone teach me this a long time ago?" They were no longer held back by the lack of skills and poor reading habits. They could read almost as fast as they could think.

What makes Speed Learning so successful?

The new *Speed Learning Program* does not offer you a rehash of the usual eye-exercises, timing devices, costly gadgets you've probably heard about in connection with speed reading courses or even tried and found ineffective.

In just a few spare minutes a day of easy reading and exciting listening, you discover an entirely new way to read and think — a radical departure from anything you have ever seen or heard about. Research shows that reading is 95% *thinking* and only 5% eye movement. Yet most of today's speed reading programs spend their time teaching you rapid eye movement (5% of the problem) and ignore the most important part (95%) *thinking*. In brief, *Speed Learning* gives you what speed reading *can't*.

Imagine the new freedom you'll have when you learn how to dash through all types of reading material *at least* twice as fast as you do now, and with greater comprehension. Think of being able to get on top of the avalanche of newspapers, magazines and correspondence you have to read . . . finishing a stimulating book and retaining facts and details more clearly and with greater accuracy than ever before.

Listen-and-learn at your own pace

This is a practical, easy-to-learn program that will work for you — no matter how slow a reader you think you are now. The *Speed Learning Program* is scientifically planned to get you started quickly . . . to help you in spare minutes a day. It brings you a "teacher-on-cassettes" who guides you, instructs, encourages you, explaining material as you read. Interesting items taken from *Time* Magazine, *Business Week*, *Wall Street Journal*, *Family Circle*, *N.Y. Times* and many others, make the program stimulating, easy and fun . . . and so much more effective.

Executives, students, professional people, men and women in all walks of life from 15 to 70 have benefited from this program. Speed Learning is a fully accredited course . . . costing only 1/5 the price of less effective speed reading classroom courses. Now you can examine the same, easy, practical and proven methods at home . . . in spare time . . . without risking a penny.

Examine Speed Learning FREE for 15 days

You will be thrilled at how quickly this program will begin to develop new thinking and reading skills. After listening to just one cassette and reading the preface you will quickly see how you can achieve increases in both the speed at which you read and in the amount you understand and remember.

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★ ★ ★ EXTRA ★ ★ ★

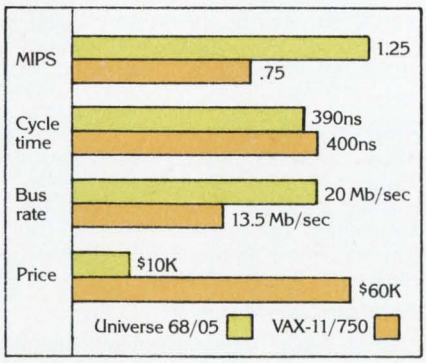
32-Bit Computer Breaks $10K!

Universe 68/05 First to Smash Price Barrier

The new Universe 68/05 is the first true 32-bit computer priced under $10,000 (OEM quantity one). "True" because, unlike other 68000-based systems, the Universe 68/05 handles 32 bits in parallel on its VERSAbus.

Outperforms VAX*

Its *price* is even more impressive when you look at Universe 68/05 *performance* versus that of 32-bit "superminis" several times more expensive, like the VAX-11/750.



High-Speed 68000, 4Kb Cache, 32-Bit Bus

The key to that performance is a 4Kb cache that eliminates processor wait-states and takes full advantage of a 12.5MHz 68000 processor. Also included are a separate 68000 I/O processor, four serial I/O ports (expandable to 64), 256Kb RAM (expandable to 3Mb), 20Mb/sec, 32-bit VERSAbus, 10Mb Winchester, 1.25Mb floppy disk, and 5-slot card cage. All in a 7-inch enclosure.

UNIX-Compatible Real-Time OS, Too

UNOS*, our UNIX* Rev7-compatible operating system with real-time features, runs Pascal, Fortran, C, BASIC, DBMS, and third party application programs.

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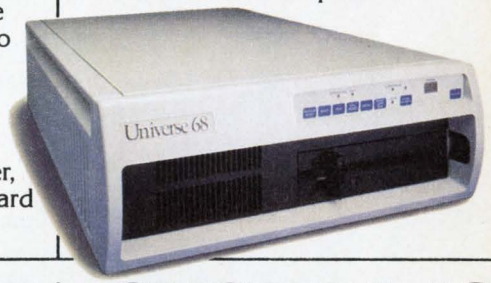

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*VAX is a trademark of Digital Equipment Corporation. UNIX is a trademark of Bell Laboratories. UNOS is a trademark of Charles River Data Systems.

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Calendar

January 4–6

AFCEA 4th Western Conference and Exposition. San Francisco Hilton Tower, San Francisco, CA. Contact: Programs Office, AFCEA Nat'l Headquarters, One Skyline Place, Suite 300, 5205 Leesburg Pike, Falls Church, VA 22041. (703) 578-1037.

January 10–13

ATE West. Automated Testing for Electronics Manufacturing Conference. Anaheim Convention Center, Anaheim, CA. Contact: Kathy Bochonko, Marketing Services Manager, Morgan-Grampian Expositions Group, 2 Park Ave., New York, NY 10016. (212) 340-9700.

January 12–14

1983 Federal Software Conference. Shoreham Hotel, Washington, DC. Contact: US Professional Development Institute, 12611 Davan Dr., Silver Spring, MD 20904. (301) 622-5696.

January 16–19

CADCON '83. Disneyland Convention Center, Anaheim, CA. Covers CAD/CAM design systems; electronic, architectural, and structural hardware and software; system integration; modeling; simulation; and robotics. Contact: Robert A. Poggi, CADCON Conference, Morgan-Grampian Exposition Group, 2 Park Ave., New York, NY 10016. (212) 340-9700.

January 18–20

Southcon/83. High-Technology Electronics Exhibition and Convention. Georgia World Congress Center, Atlanta, GA. Contact: Electronic Conventions, Inc., 999 N. Sepulveda Blvd., El Segundo, CA 90245. (213) 772-2965.

January 20

Invitational Computer Conference. Orange County, CA. Contact: B.J. Johnson & Associates, 3151 Airway Ave., #C-2, Costa Mesa, CA 92626. (714) 957-0171.

January 20–21

1983 Measurement Science Conference. Hyatt Rickeys Hotel, Palo Alto, CA. Contact: Bob Weber, Lockheed Missile & Space Corp., Sunnyvale, CA 98046. (408) 742-2957.

January 21–23

CP/M '83. Int'l Conference On Microcomputer Software. Moscone Center, San Francisco, CA. Contact: Northeast Expositions Inc., 824 Boylston St., Chestnut Hill, MA 02167. (617) 739-2000 or (800) 343-2222.

January 24–26

VLSI Design Tutorial Seminar. Palo Alto, CA. Contact: Hellman Associates, Dept. R, 299 California Ave., Palo Alto, CA 94306. (415) 328-4091.

January 25–27

Advanced Semiconductor Equipment Exposition. San Jose Convention Center, San Jose, CA. Contact: Cartlidge & Associates, Inc., 4030 Moorpark Ave., Suite 205, San Jose, CA 95117. (408) 544-6644.

January 25–27

Automated Office Expo. Moscone Center, San Francisco, CA. Contact: Automated Office Expo, Suite 400, 222 West Adams St., Chicago, IL 60606. (312) 263-3131.

January 31–February 2

Communication Networks. Conference & Exposition. The Rivergate, New Orleans, LA. Contact: CN '83, Box 880, Framingham, MA 01701. (617) 879-0700.

February 1–3

EMTAS '83. Electronics Manufacturing Technologies and Systems '83 Conference. Phoenix Hilton Hotel, Phoenix, AZ. Contact: SME, One SME Dr., PO Box 930, Dearborn, MI 48128. (313) 271-1500.

February 1–5

Kuwait Info '83. 2nd Int'l Information Management Exposition and Conference. Kuwait Int'l Exhibition Center, Safat, Kuwait. Contact: Clapp & Poliak Int'l, 7315 Wisconsin Ave., PO Box 70007, Washington, DC 20088. (301) 657-3090.

February 2–4

Peripherals '83. Peripherals Suppliers Exhibition. Contact: IPC Exhibitions Ltd., Surrey House, One Throwley Way, Sutton, Surrey SM1 4QQ, England. Tel. 01-643-8040.

February 7–9

Electronic Display Technology Course. Contact: The Center for Professional Advancement, Dept. NR, PO Box H, East Brunswick, NJ 08816. (201) 249-1400.

February 22–24

Industrial Productivity Conference and Exposition. The San Jose Convention and Cultural Center, San Jose, CA. Contact: SME, One SME Dr., PO Box 930, Dearborn, MI 48128. (313) 271-1500.

February 23–25

Int'l Microelectronics and Teleinformatics Conference. Milan, Italy. Covers VLSI as a tool and application in teleinformatics. Contact: Bias-Microelectronics Conference, Fast, Pile R. Morandiz, 20121, Milano, Italy. Tel. (02) 78-3051.

February 23–25

ISSCC '83. 30th Int'l Solid-State Circuits Conference. New York, NY. Contact: IEEE, 345 East 47th St., New York, NY 10017.

February 23-25

Microsystems '83. Buyers and specifiers of all types of microcomputers, microprocessors and associated services. Contact: IPC Exhibitions Ltd., Surrey House, One Throwley Way, Sutton, Surrey, England, SM1 4QQ. Tel. 01-643 8040.

February 28–March 2

Optical Fiber Communication. Topical Meeting and Exhibit. Hyatt Regency, New Orleans, LA. Contact: Meetings Dept., Optical Society of America, 1816 Jefferson Place, NW, Washington, DC 20036. (202) 223-8130.

Analogic's AP500, the Emancipated Array Processor

Frees You and Your Host for Greater Productivity

The Emancipation

Analogic's AP500 32-bit Floating Point Array Processor is the first truly independent array processor. It offers the performance and throughput capabilities needed to meet most time-critical, complex, and I/O-bound applications.

With little or no Host involvement, the state-of-the-art Control Processor based on the 32/16-bit MC68000 supermicro and ultra-fast 40-bit Arithmetic Pipeline deliver the power and flexibility to solve most applications in real-time.

The AP500 has unprecedented I/O capabilities for COMPLETE system expansion. Now free the Host from burdensome I/O with the IEEE-796 standard Multibus, the RS-232 Serial Line Interface, and the two 6.25MHz Auxiliary I/O Ports. Only Analogic provides the necessary paths for array processor system growth.

OEM and End-User Benefits

Packaged to Fit—Contained in a 5.25" rack-mountable chassis or available as a card set with backplane, this AP500 is compact/rugged power for the systems integrator.

Easy-to-Use—Programmable in high-level or assembly language, AP500 Software is modularly designed to get most applications off the ground quickly and painlessly.

Tools to Optimize—AP500 Software provides many simple programming techniques for execution-time optimization . . . customized to meet your application demands.

Priced to Please—For comparable performance, you will have to pay from two to ten times as much for other array processors or minicomputers.

Complete System Flexibility

The AP500 supports virtually ANY system configuration. You can build your system from a wide range of Multibus-compatible peripherals including disks, tapes, A/Ds, D/As, display monitors, CPUs and LAN controllers; or configure data acquisition and data display devices to the high-speed Auxiliary I/O Ports.

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COMPUTER SYSTEMS DIVISION

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News Update

$5.5 Million For Parsec Development

Parsec Systems Corp., Richardson, TX, announced completion of its initial funding, $5.5 million in venture capital, for the development of an ultrahigh-performance computer. Parsec's leading investor is the venture capital firm, Sevin Rosen.

Altos And Shasta Sign Contract

Altos Computer Systems, San Jose, CA, and Shasta General Systems, Sunnyvale, CA, announced an agreement on a multi-year contract valued in excess of $20 million. Altos will supply Shasta with the Altos ACS6800 computer system which has been designated the Shasta 3216.

Second-Source Custom Circuits

ZyMOS Corp., Sunnyvale, CA, and Standard Microsystems Corp., Hauppauge, NY, have reached an agreement-in-principle to act as second-source suppliers for each other's custom integrated circuit devices. The agreement covers silicon-gate NMOS and CMOS custom devices and is based on completion of qualification testing at each company's facilities.

ACC Supplies Emulator To AMD

Associated Computer Consultants, Santa Barbara, CA, has entered into an agreement with Advanced Micro Devices, Sunnyvale, CA, for the development of a hardware emulator for the AMD AM7900 Family of Ethernet integrated circuits.

IMI Signs OEM Agreement

International Memories Inc., Cupertino, CA, has signed an OEM agreement with Hewlett-Packard worth in excess of $3 million. IMI will supply H-P's Disk Memory Div., Boise, ID, with its Model 7720 8″ disk drives. H-P is integrating the IMI drives in its 7908 disk subsystem for use with a number of systems.

Codex Contracts 6000 Series

Codex Corp., Mansfield, MA, announced the signing of a $1.8 million contract with American President Lines, Oakland, CA, for 6000 Series Intelligent Network Processors, a DNCS 400 central site network control and management system, the new CS Series network control modems and MX 2400 modems.

VOTAN Expands And Relocates

Larger corporate headquarters and production facilities are being occupied by VOTAN, Inc., a supplier of computer speech technology products in Fremont, CA. Relocation was due to substantial growth expected by the company after receiving the first major installment of a $3.5 million funding from Honeywell.

Perkin-Elmer To Open Facility In Ireland

Perin-Elmer Corp., Oceanport, NJ, announced ground breaking for a new manufacturing facility at Bishopstown, Cork City, Ireland. The firm's high-performance 32-bit superminicomputers will be built at the new site.

Harris, CGIS Sign Marketing Agreement

The Computer Systems Div. of Harris Corp. has signed an unusual joint marketing agreement with Comsat General Integrated Systems (CGIS), in which customers will be offered the high performance of Harris superminicomputers, integrated with CGIS software; including microwave CAE, high frequency circuit design, interactive logic creation/capture, simulation and test.

SofTech Targets MC68000

SofTech, Waltham, MA, has received an Army contract to adapt its Ada Language System to Motorola's MC68000 chip. The MC68000 will be used by the Army in its Communication Control System (CCS) which is part of its Advanced Field Artillery Tactical Data System (AFATDS).

National Speaks Japanese

National Semiconductor and OKI Electric Industry Co., in conjunction with OKI Semiconductor, are having discussions with a goal of establishing a long-term relationship in the field of advanced MOS memory products. The talks have focused on the broad principles of joint development and second sourcing.

News Update

VERSAdos Price Reduction

Motorola has announced a significantly lower licensing fee for use of standard VERSAdos Real-Time Multitasking Operating System software for the MC68000 MPU. The quantity-one internal-use licensing fee has been reduced from $7000 to $2000 for the VERSAdos object code supplied on 8" diskette.

Atari Forms Semiconductor Group

All semiconductor design, development and test operations at Atari have been centralized in the new Atari Semiconductor Group, headed by Gary J. Summers, formerly Sr. VP of Commodore International's Semiconductor Div. ASG will assist Atari's product divisions in testing incoming chips from outside vendors.

Kontron Integrates FutureData

Kontron Electronics, Culver City, CA, announced a new US operation, tightly linking FutureData (acquired from GenRad, 1982) to the worldwide Kontron structure. FutureData has become a division of Kontron, a designer and manufacturer of sophisticated tools used to design microprocessor-based products.

CompuScan And Dictaphone Reach Agreement

CompuScan, a manufacturer of image processing products and systems, has signed a marketing agreement with Dictaphone Corp., a manufacturer of office automation systems. Customers purchasing or leasing CompuScan AlphaWord III PageReaders will be assured of their compatibility with Dictaphone Artec workstations.

Fiber Optic Ethernet-Compatible LAN Demonstrated

Claimed to be the first fiber optic, Ethernet-Compatible Local Area Network Communications System, Fiber Optic Net/One, was demonstrated at FOC '82. The network is the result of a joint technology development effort between Codenoll Technology Corp. (Yonkers, NY), Ungermann-Bass (Santa Clara, CA) and Siecor/FiberLAN, (Research Triangle Park, NC).

For the demonstration, Codenoll Technology developed the Codenet–2020 Fiber Optic Ethernet Transceivers, Ungerman-Bass developed the Ethernet Compatible Network Interface Units and the Communications Software, while Siecor/FiberLAN supplied the Fiber Optic transmission Subsystem including a Transmissive Star Coupler.

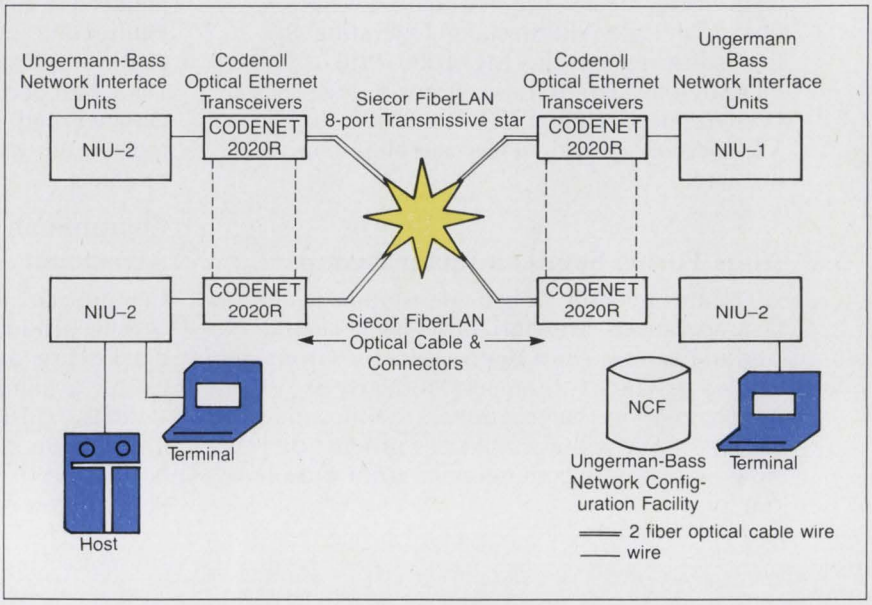

Figure 1: Fiber Optic Net/One, demonstrated at FOC '82, is a fiber optic, Ethernet-compatible LAN system.

Net/One is a general purpose Local Area Network Communications System marketed by Ungermann-Bass. Net/One is available in two baseband versions, including one that is fully Ethernet-Compatible and a broadband CATV compatible version.

Fiber Optic Net/One combines Ethernet and Fiber Optic Technology through Codenoll Technology's Codenet-2020. Michael H. Coden, President of Codenoll Technology Corp., stated, "Since the Codenet-2020 Fiber Optic Transceiver is plug compatible with Ethernet equipment, Ethernet users can preserve their hardware and software investments as well as gain the benefits of fiber optics."

According to Joe Kennedy, Ungermann-Bass' Director of Joint Corporate Development Programs, "The principal advantage of using optical fiber in Local Area Networks is that it is not susceptible to electromagnetic radiation interference, making it a good choice for environments such as factories with heavy machinery, or in close proximity to radar sources.

"Also, optical fibers do not radiate energy and are much more difficult to tap surreptitiously, suggesting applications in security-conscious locations."

Dr. Richard Jones, Director for Engineering for Siecor/FiberLAN, said that Fiber Optic Net/One demonstrates the practicality of using fiber optics in Local Area Networks. "Fiber Optic Net/One has proven to us that fiber optics can work with existing CSMA/CD Local Area Networks, including Ethernet. This demonstration is an important first step that will lead to widespread use of fiber optics in LANS," he said.

MIT Professors Urge Establishment of EE Education Plan

Four Massachusetts Institute of Technology professors say a revolution must occur in electrical engineering education if the United States is to maintain its technological health and its ability to compete in the world marketplace.

In the report, "Lifelong Cooperative Education," MIT professors call for the establishment of a new at-the-workplace education program that is national in scope, closely linked to industry, and based on the view that formal education must be a never-ending pursuit for electrical engineers and computer scientists.

In the knowledge-intensive industries, new theoretical and practical results are being generated faster than they are being effectively transmitted to the engineering community. Nothing less than the proposed restructuring of engineering education, extending the learning environment to include the workplace, can solve the problem, the MIT professors said.

Many continuing education programs for engineers already exist, the MIT professors said, but "the depth and projected course of the engineering manpower crisis demand substantially greater investments of human and material resources than at present, as well as the establishment of new cooperative institutions for development and management of these re-

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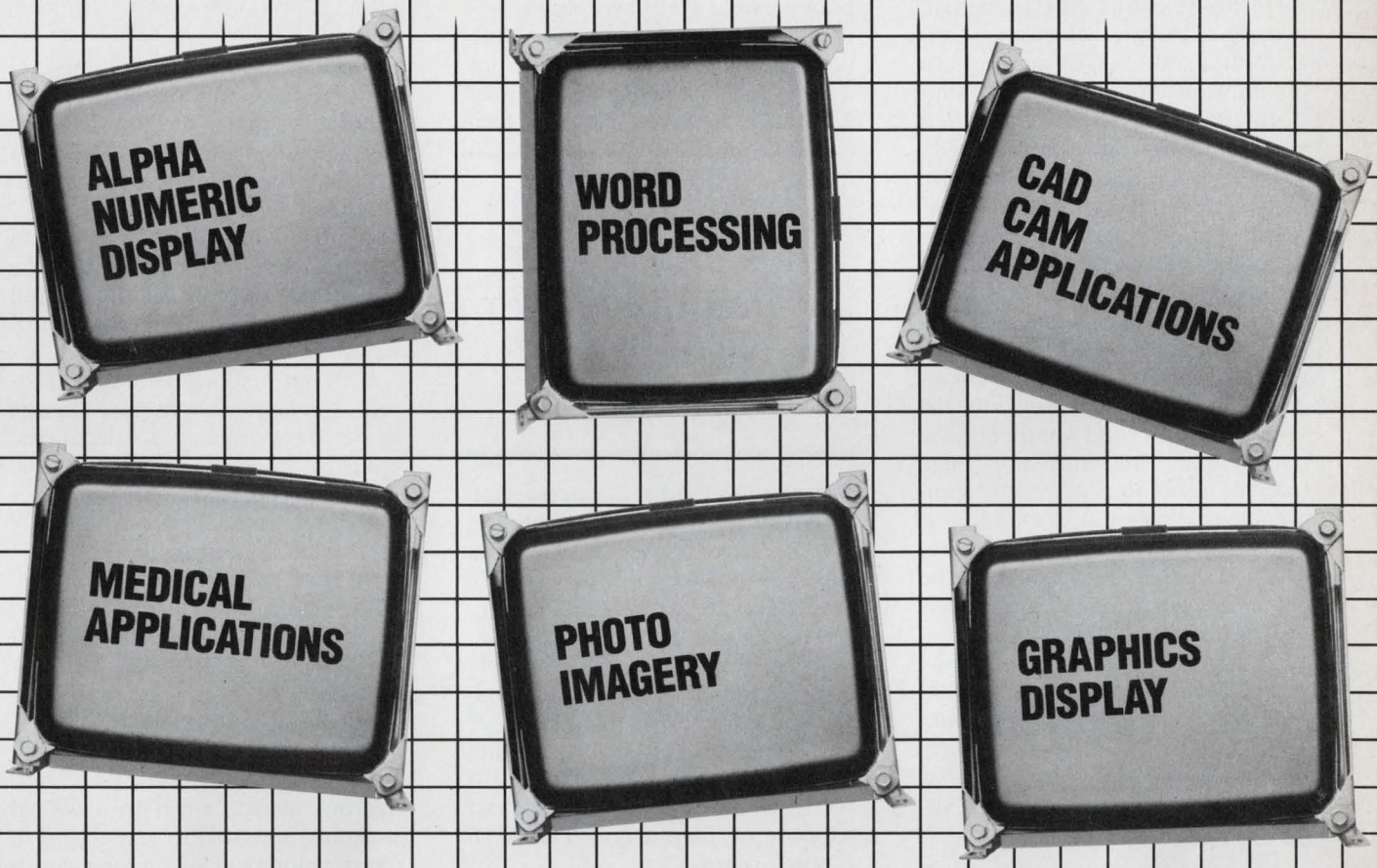

Yesterday's ideas might not be good enough for today or tomorrow, and selecting the proper data display has never been more significant. Recent studies in the computer marketplace indicate the CRT display has become the single-most important element in today's computer systems. An easy-to-read, jitter-free display is of course a dynamic part of this critical man/machine interface.

If you want to look at things with a fresh point of view, an eye-pleasing Audiotronics data display can help insure maximum productivity for the end user.

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sources." The leadership and personal attention of top executives in industry and academia are required, they said.

The report, culminating a yearlong study, stated that the rapid rate of scientific and technical progress in the electronic and computer field "challenges a basic assumption on which traditional engineering is based: that a few years of formal education can provide an adequate foundation for half a century of professional work."

"It has been assumed that new technological developments with which an engineer would have to become familiar after graduation would be extensions of previous ones, or at least based on the same scientific and mathematical knowledge. This has not been true for a number of recent technological developments and it is not likely to be true in the future. Thus, engineers are faced with the problem of learning, during their professional lives, what new generations of engineering students are currently learning in school. Otherwise they risk becoming professionally obsolete at an early age or prisoners of specialties that no longer provide rewarding career opportunities."

The report's authors — Professors Robert M. Fano, Louis D. Smullin, William M. Siebert and James D. Bruce — said the increasing demand for up-to-date engineers can't be met by replacing obsolescent engineers with new graduates, and even if it could the human costs of such a policy would be unacceptable.

For example, staying up to date is difficult for men engineers, but it is especially taxing for women who want to have children. "In a fast-moving field . . . interruption of technical work to raise children can be permanent unless special educational opportunities are available," the report said.

Formal education must be a never-ending pursuit for electrical engineers.

The only apparent alternative: make better use of the available engineering work force through the "preventive maintenance" of human resources by continuing education at the workplace with the active encouragement and support of employers. The MIT report proposes:

- That engineering schools and neighboring industries collaborate toward the development of lifelong cooperative education.
- That engineering schools offer a master's degree program for working engineers using the TVI (tutored video instruction) methodology pioneered by Stanford University.
- That engineering schools encourage participation in their off-campus graduate programs on the part of all engineers, whether or not they intend to become degree candidates.
- That appropriate versions of recently developed undergraduate courses be offered for the benefit of engineers who have been out of school for several years.
- That engineering faculties seek the help of industrial experts in the development of specialized courses, thereby extending the scope of their graduate offerings and of the engineering community that could benefit from them.
- That managements of industrial organizations encourage and support formal study on the part of engineers of all ages, " whether working at the bench or managing large projects."
- That a Council be established, involving industry, engineering schools and professional societies, to provide leadership in the development of lifelong cooperative education.

Interchange Identification Capability Proposed For Tape Cartridges

An Interchange Identification Capability (I^2C) which will identify the format, including track layout, of data recorded on quarter-inch tape cartridges by streaming drives, was defined by The Working Group for Quarter-Inch Cartridge Drive Compatibility (QIC).

The I^2C feature will enable a drive to determine what recording format was used to generate a cartridge and will then enable the drive to read and write data in the same format, if within the capability of the drive. Data exchange would not be attempted with a cartridge whose format is not resident in the drive. The I^2C will prepare the industry for future advances by enabling compatibility with earlier recording formats when implementing new higher-density formats.

QIC has been established to spur widespread use of quarter-inch cartidge tape drives through the development of proposed standards that will encourage industry wide compatibility. Representatives from the following fifteen companies defined I^2C: Archive Corporation, BNR, Inc., Cipher Data Products, Inc., Computer Storage Technology, Data Electronics, Inc., Data Packaging Corporation, Kennedy, Nippon Electric Corporation, Qantex Division of North Atlantic Industries, Rosscomp, Sankyo Seiki Mfg. Co, Ltd., Tandberg Data A/S, TEAC, 3M and Western Digital Corporation. Eight companies have so far established full voting membership (Archive, Cipher, DEI, Irwin Olivetti, Inc., Qantex, Sanyo Seiki, Tandberg and Wilson Laboratories, Inc.). Freeman Associates (Santa Barbara, CA) is organizer of the group.

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Do you have your own wafer fab? "YES SIR! All of our wafers are processed in our modern 4" fab. When you deal with Universal you know who's in command of the technology. Not true with many gate array suppliers who purchase wafers from outside sources and have no control of the production of the processes they are offering."

Do you have a broad selection of gate arrays? "YES SIR! Chances are we have an array sized for your requirement. Our family of seven ISO-3 or ISO-5 arrays ranges in complexity from 360 to 1800 gates. Choose our 5 micron arrays for toggle rates up to 25MHz and our 3 micron arrays for toggle rates beyond. Now you can replace your power hungry TTL or LSTTL circuits with low power, high speed CMOS arrays."

Do you have a design manual? "YES SIR! Our engineers have developed a 220-page engineering manual which contains everything they need to know to design high performance CMOS IC's. Now, you can purchase the same engineering manual professional IC designers use for $69. Delivery is from stock."

Do you have fast turnaround? "YES SIR! For arrays of 720 gates or less, we guarantee an eight week turnaround to tested prototypes starting with your reconfigured logic diagram. For larger arrays, add one week per 150 gates. That means we'll turn a 1000 gate array in 10 weeks and a 1500 gate array in 13 weeks."

Do you have complete CAD capability? "YES SIR! We have the Applicon 4575 System complete with a VAX 750 computer, design peripherals and versatile software programs for interactive routing, automatic checking, logic and circuit simulation, and test program generation. Also, we can supply our data base in Applicon, GDS-I, or GDS-II format if you want to design on our arrays with your CAD equipment."

Do you offer full production testing? "YES SIR! The work horse of our test area is the Fairchild Series 10 high speed production tester. This system has test capability up to 60 pins and is program compatible with the Sentry 7 and 20 Systems. For slower speed testing we use the Pragmatic TM-4 and for high speed analysis we have the Tektronix DAS 9100 50MHz Logic Analyzer."

Do you have second sources? "YES SIR! We have not one but two qualified second sources. Both Siliconix and Nitron have entered into licensing agreements with Universal to design and manufacture the ISO 3/5 CMOS arrays. Both companies are full service semiconductor companies with their own wafer fab facilities."

Can you convert gate arrays to full custom IC's? YES SIR! All of our gate array engineers have full custom IC design backgrounds. If you have a high volume requirement, we can get your product on the market quickly with a gate array. As your production builds, we'll convert the array to a full custom IC. You'll have the lowest cost IC possible when your production reaches full potential."

Do you have competitive prices? "YES SIR! We've saved the best for last. Our ISO-3 and ISO-5 arrays are the densest in the Industry. High density means smaller chips and smaller chips mean lower prices. In reasonable production quantities, we can produce a high performance CMOS array for you for 1.2¢ per gate or less. Call (408) 279-2830 for a production price estimate."

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Record Software Revenues in '81

US computer software revenue grew 45% in 1981, leading the computer services industry to a record $22 billion in revenue. The industry as a whole grew 24% in 1981.

The 16th Annual Survey of the Computer Services Industry, sponsored by the Association of Data Processing Services Organizations (ADAPSO), revealed nearly all sectors experienced positive growth in revenue, profits, and productivity in 1981, despite recession. Revenue from software products resulted in a total increase of 45% in 1981, as shown in **Figure 1.** Integrated systems revenue, included in the study for the first time, followed with a 34% increase. Processing services continued to generate almost half of total industry revenue, though their market share has declined from 49% in 1980 to 45% in 1981. Professional services were second in terms of total size, earning 23% of the markets' revenue.

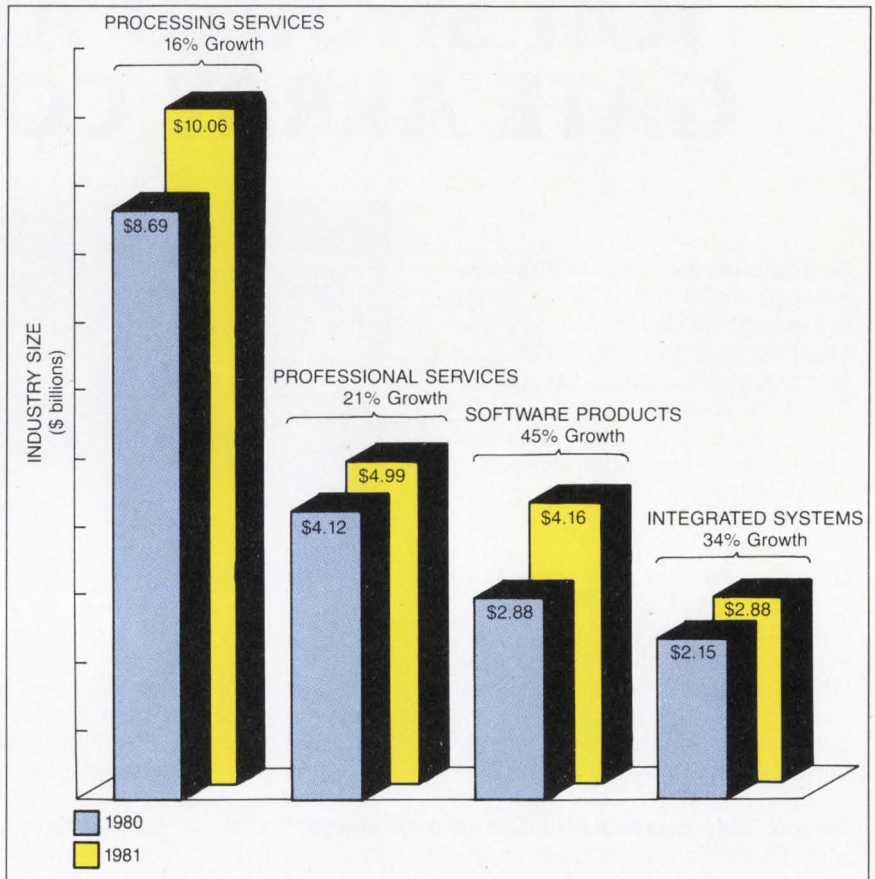

Figure 1: US Computer Services Industry Growth, 1980-1981.

"Computer services is one of the few industries in the US economy currently generating positive net additions to its capital stock," stated Peter A. Cunningham, President of INPUT, an organization providing planning services to the information industry. "In the current economic climate, companies need to streamline operations. Computer services provide a cost effective means for doing so and will likely continue its growth even without a dramatic turnaround in the economy."

The INPUT study is based on interviews with over 600 firms in all sectors of the industry and includes a census of the 250 computer services firms with annual revenues of over $10 million. Financial ratios are presented for 74 public computer services companies.

For additional information, contact INPUT, 1943 Landings Drive, Mountain View, CA 94043, (415) 960-3990.

INFO '82 Predicts The Portable Office

"Wall Street will be anywhere!" said Jon M. Conahan, a partner in the firm of Arthur Andersen and Co. (New York, NY) at the INFO '82 conference held recently in New York. "Finding your broker down on Wall Street to check figures on gold trading in Zurich and Singapore, or the latest prices on T-Bill options soon will be unnecessary. Telecommunications technology will make geography irrelevant."

Conahan spoke of his company's position and philosophy in the information systems/processing marketplace. "On the morning train, you might check current gold trading. As the latest trade from London crosses your pocket screen, you might check it against last night's Singapore closing price, the N.Y. close Fed. Funds Rate, and the current price of an option on T-Bill Futures in Zurich. After a quick calculation you send a 'trade' to your broker's terminal. By the time you get to your office you will have a message waiting on your desktop computer; the price, quantity, foreign exchange impacts, tax consequences and so on. Push a button to file it, and you can get on with your day's business."

Exciting hypothetical scenarios such as this were the rule at the 9th (annual) International Information Management Exposi-

tion and Conference (INFO '82). INFO was geared toward the business and managerial aspect of communications and information interchange equipment, and the selection of such equipment. There were more than 330 companies occupying all four floors of the New York Coliseum. There were also demonstrations of Applications/Problem solutions and methods, Services and Products and many other topics. The exposition and conference, produced by Clapp and Poliak (New York, NY), included 184 speakers, panelists and moderators.

Three keynote sessions were slated which set the tone for the conference. Archie J. McGill, Vice-President of business marketing for AT&T, spoke about "Information Management and Business Decision Making"; William R. Synnot, Sr., Vice-President of the 1st National Bank of Boston, discussed "Satisfying the Information Needs of Corporate Executives"; and, Rod F. Dammeyer, Executive Vice-President of Finance, Northwest Industries, talked about "Getting Quality from the Information Explosion: A Prerequisite for Successful Decision Making." According to some of the speakers we'll see more and more business activity in the home in the very near future, and out of the physical office. In fact, the modern concept of "Office Automation" may already be out-moded because the "office" itself may be a dinosaur in the Information Age, according to Info '82 producer Richard Wolcott. We may see a substantial elimination of the "physical office" due to modern technological trends. "A typist, at home, can now receive the day's dictation, transcribe it via word processor and transmit it by computer to a central point where the letters will spew forth from a high-speed printer," says Wolcott.

Keynote speaker Rod Dammeyer discussed the effects of integrating the management information systems into the routine functions of senior mangement executives. Dammeyer believes that these changes may seriously affect these executives. Junior level executives have learned modern office techniques and "are avidly engaged in pursuing their skills." This may, he believes, "aggravate the pressure on senior executives to catch-up with modern times and methods." Dammeyer further stated, "Even their children may be playing with home computers at Summer Camp," and he concludes "undoubtedly, some managers would feel intimidated by all this. . ." Dammeyer also noted that an excess of information in the office can be counter-productive: "An overload of information can be more harmful than helping . . . up to a certain point, more information leads to better decisions. But after that, the law of diminishing returns sets in, and eventually more becomes less."

"A typist, at home, can now receive the day's dictation, transcribe it via word processor and transmit it by computer to a central point."

Somewhere in the realm of Information Systems and Management, falls, Decision-Support Speaker Daniel Stanford explained, "Decision-support systems change the way people approach a problem and make a decision. People won't change unless top management is firmly committed to the concept and implementation of Decision-support systems." Mr. Stanford is the manager for Decision-support services of Management Decision Systems (Waltham, MA).

The people and the diversity of their backgrounds made Info '82 an interesting and informative conference, in both a theoretical and practical manner. The conference laid the groundwork for business leaders to explain which way they want technology to aim: to progress for the benefit of our nation's economic recovery and to support American business so that productivity as a positive action yields an equal and positive reaction.

—Pevovar

Spectacular Growth In Telecommunications Industry

The telecommunications industry is on the move, as the demand for expanded, more effective communications spurs tremendous growth in the myriad of communications-related industries.

By 1990, annual US shipment levels of telecommunications equipment related to office automation alone will approach $40 billion, roughly 300% of 1982 shipment levels, according to the initial release of a new market analysis from Creative Strategies International (CSI), a California-based market research and consulting firm.

Satellite technology, one of nearly three dozen market/industries examined in the report, will have major impact on telecommunications throughout the 1980s and beyond. There is a tendency to regard satellite communications as a panacea for solving price/performance problems, however this general euphoria may be overstated.

The unique problems associated with both voice and data satellite transmission suggest that the best approach will be to blend satellite with other transmission

technologies, such as conventional channels, fiber optics, microwave, and so forth. As in the past, the decision as to the type of transmission technology will continue to be a matter of cost/performance trade-offs.

Availability Of Common Carriers

The broadening availability of specialized common carriers and value-added networks (VANs) in the 1980s will create a dynamic environment for new and expanded uses of communications, and networks will assume increasingly worldwide characteristics over the next several years. Recently, US voice and data common carriers, specialized common carriers, and VANs have been striving to extend their networks to capture international business. Due to the multitude of telephone administrations that must approve new international services, the actual implementation of fully integrated international networks will be slow.

As more computer products are linked via telecommunications, much industry growth has become closely tied to developments in office automation. The recurring theme of telecommunications in any environment, however, is that virtually every corporate requirement is unique and not amenable to a standardized turnkey solution. Systems will comprise a wide variety of transmission media and network technologies, as well as a diverse mix of terminals and other communications equipment. New business potential is found in the development telecommunications/office systems integration and development.

Future Growth

In the 1980s, telecommunications management will be much more sophisticated and broadly knowledgeable across the board. The impact of increasing user sophistication will have an exponential effect upon the growth of telecommunications products/services in the business community. However, users are also more demanding of total telecommunications solutions, rather than the single-product approach of the past. In addition, non-communications savings or productivity gains, as opposed to direct communications cost savings, will be the basis for justifying communications expenditures.

Industry growth has become closely tied to developments in office automation.

Competition will further intensify as new companies are drawn by the enormous telecommunications market potential, while other companies increase their current participation in the market. Virtually no market segment will be free from possible attack from a new competitor. In particular, smaller companies offering communications products/services should be aware of the "lurking giants" poised to snap up substantial market shares in any attractive market segment. A notable example in this respect will be IBM's long-awaited entry into the U.S. PABX marketplace.

CSI's service, *Telecommunications Strategies For The 1980s*, examines aspects of the telecommunications industry; emphasizing market data, user preferences, applications, and cost impacts. The initial analysis provides market forecasts for 35 product segments, a spotlight on technology trends, and a focus on key industry and competitive issues. A one-year subscription is $15,000. The initial release is available for $12,000. For further information, contact Creative Strategies International, 4340 Stevens Creek Blvd., Suite 278, San Jose, California 95129, (408) 249-7550.

Diminished Role Of Xerox Ethernet Predicted

AMDAX Corporation, a supplier of Local Area Communications Network (LACN) products, is predicting the diminished role of Xerox's Ethernet at the hands of IBM.

"IBM's announcement that Texas Instruments will produce the chip-set for its LACN interface indicates that IBM is very close to a full announcement," said Ivan D. Socher, president of AMDAX. "We have been working with IBM at the IEEE 802 committee meetings on LACNs. The papers presented there by IBM clearly indicate that their LACN will use a token access scheme. This positions IBM squarely against Xerox," he said. "And it seems self-evident that IBM has both the marketing clout and the installed base to come out on top. That's why we are throwing our full support behind IBM."

The company indicated that it plans to announce an IBM-compatible token access LACN product in the very near future. "We are very excited about IBM's move," said Socher. "The marketplace has literally been sitting on its hands waiting for IBM to make a move. Now that IBM has tipped its hand, we want to be the first to jump on the bandwagon."

"Ethernet fell short of the successes predicted it by Xerox," he continued. "IBM's lead will, no doubt, clear up some of the confusion this caused in the market." AMDAX Corporation designs and manufactures a variety of LACN products for business and industry.

For further information, contact Pat Ullrich, AMDAX Corp., 160 Wilbur Place, Bohemia, NY 11716.

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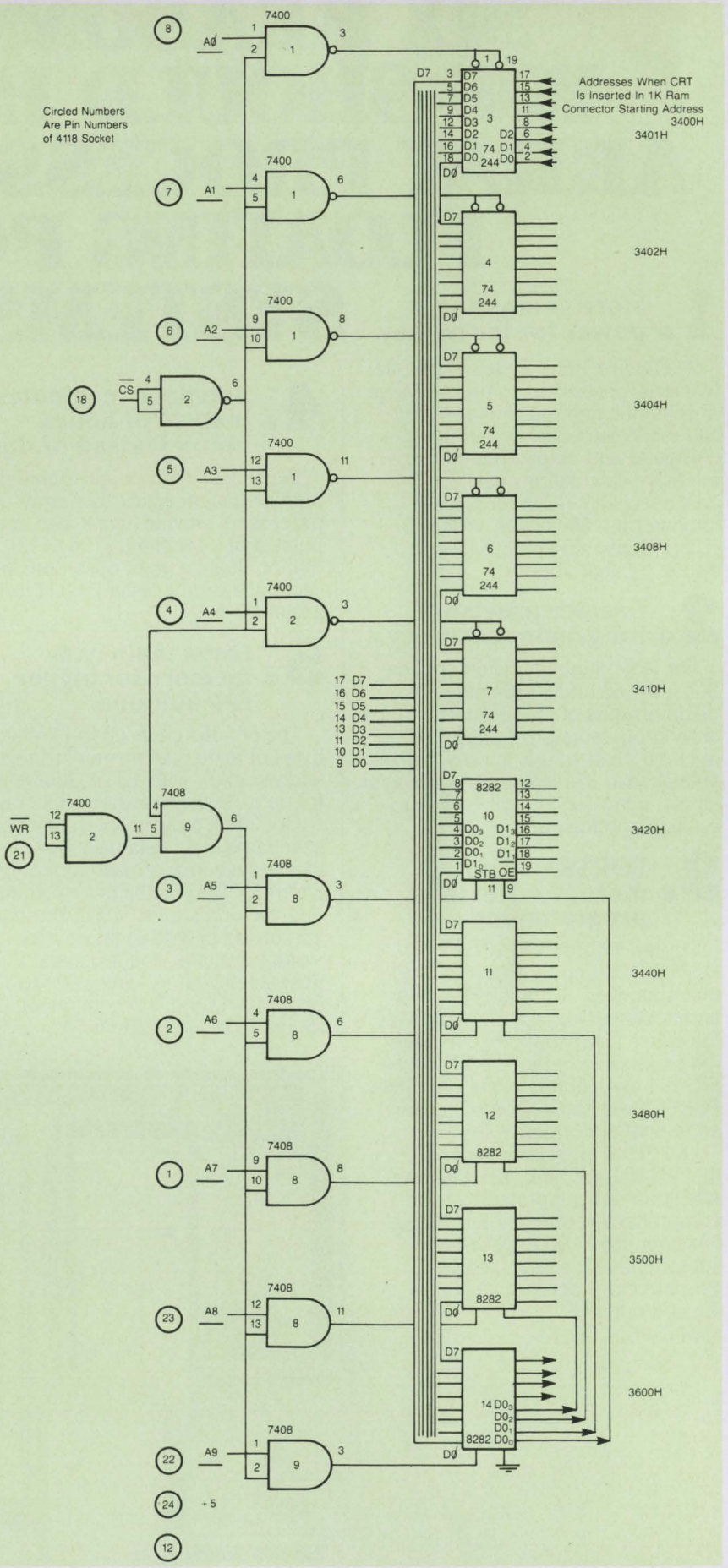
A Portable μP Analyzer

The hand-held analyzer described is a small portable device which aids immensely in trouble-shooting boards using the 8085 CPU chip. Requirements for using the circuit shown are that the CPU board under test should have a passive pull-up on the "ready" and "reset" pins of the 8085 and the RAM memory be static.

With the analyzer attached to the 8085 CPU chip and the "RUN-STEP" switch in "RUN" the CPU runs normally. Set the analyzer to "STOP ON EVERY ADDRESS" and "STEP," hit the "RESET" and the address LEDs on the analyzer will show address 0000H and the LEDs will show the data on the bus for that address. The condition LEDs will show the status of the CPU. The board under test can now be examined because the CPU is in a known state and all its lines are active. The program can be stepped through one instruction at a time to observe its operation.

With the program listing and using the "STOP ON SELECTED ADDRESS" mode it is possible to trace a program to the point it loses control. An address may be selected deep into the program. When the CPU reaches that address and stops, the analyzer may be switched to "STOP ON EVERY ADDRESS" and then single stepped from that point. Using a known loop in the control program, or a loop written for testing, and leaving the analyzer in "RUN" mode, a scope may be triggered on any selected address in that loop so that the busses may examine dynamically. Timing may also be measured in a loop by noting when an action takes place in relation to a selected address.

This analyzer can be extremely useful if the board under test does not operate on first power-up; and as a teaching aid in the operation of the 8085 CPU chip and its peripheral devices. George J. Andrukevich, Pitney Bowes, 380 Main Ave., Norwalk, CT 06852.



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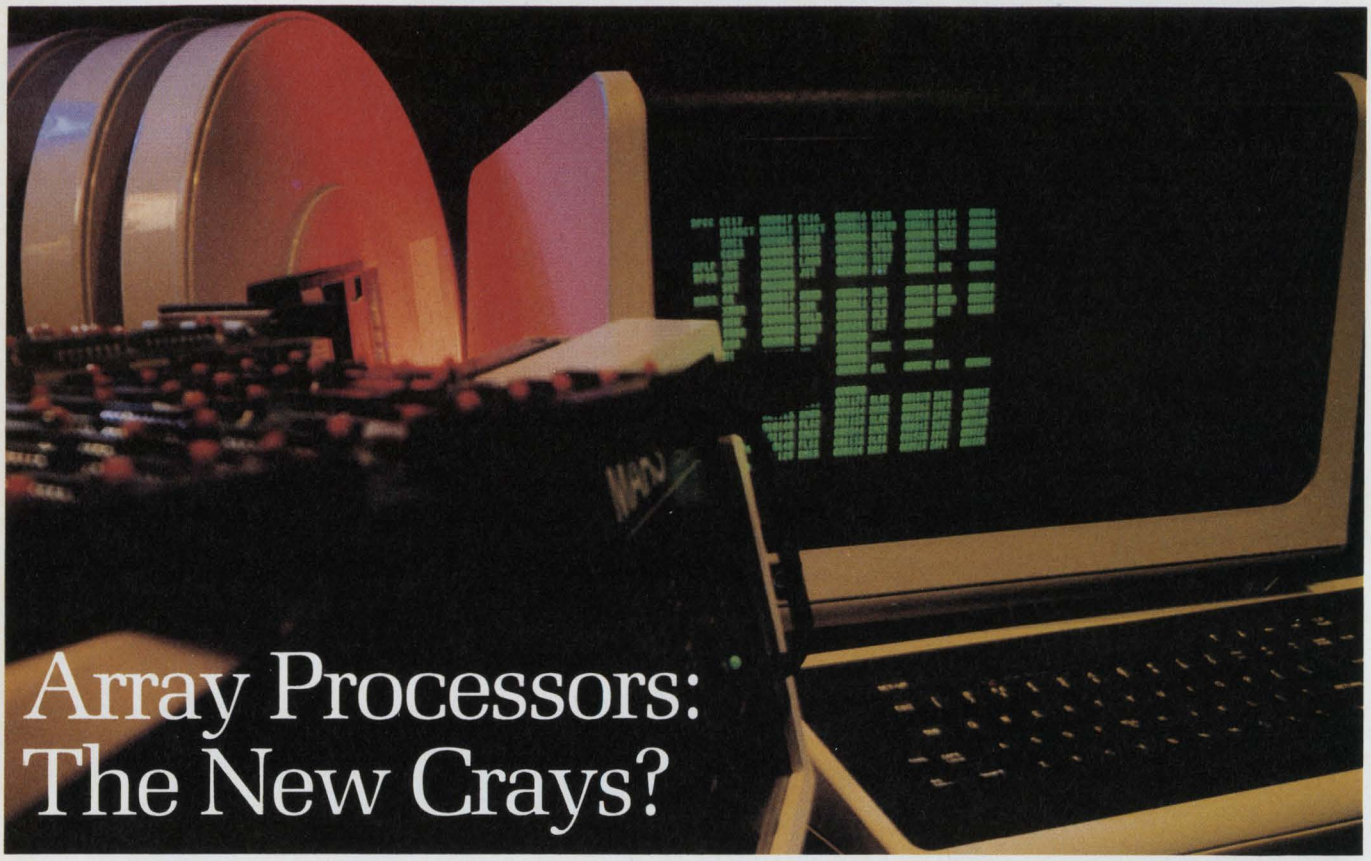

Array Processors: The New Crays?

by Dave Wilson

What is an AP?

Usually working in conjunction with a host such as a mini or mainframe, an array processor (AP) is a specialized computer that can execute complex or repetitive functions that are off-loaded from the host. The AP has been used in a number of scientific applications that include seismic data processing, image and signal processing and scientific research. Typical functions performed by APs include Fast Fourier Transforms (FFTs), vector multiplications, matrix arithmetic, convolutions and correlations.

The array processor market consists of both fixed and floating point manufacturers; Numerix, for example are at present still exclusively in the fixed-point business, while Sky and Analogic offer floating point machines. Although a wider dynamic range and greater precision is available from floating-point systems, many applications in the signal-processing environment dictate the need for fixed-point APs that offer faster speeds.

Inexpensive Solutions

Working in conjunction with μP-based systems has not typically been the role played by APs, but one company that looks set to change that conception is Sky Computer (Lowell, MA). The firm's current offerings (dubbed the Skymnks) consist of three APs: a two-board Q-bus set, a two-board Multibus set, and a one-board Versabus card.

The symbiosis of the mini and mainframe, and now the μC, with the array processor is expanding application environments.

The offices in the old mill in Lowell out of which Sky operates at present are sprinkled with Skymnk compatible computers that the company are presently enhancing with their AP product. The most recent is the Ikier Eagle-1 workstation *(Digital Design,* February, pg. 18). In response to customer demand for high performance arithmetic capability in graphics workstations used for CAD/CAM and image processing, the Ikier workstations can be powerful combined graphics and arithmetic processing capability.

Also underway at Sky is a versabus-compatible AP to work with Charles River Data Systems' latest innovation, the 68/05, a $10,000 32-bit OEM computer that incorporates a fast 4k cache memory, eliminating wait states and allowing the user to drive the computer's CPU at full capacity.

Don DeLea, VP Marketing at Charles River Data, extravagently predicts that "the new machine will sound the death knell for 16-bit

minis." It will be interesting to see what noises will be heard in the industry when the 68/05 joins up with the Skymnk–V. John Carbone at Sky Computer stated that in pointing his guns towards the μC industry, it was necessary to keep the cost of the AP low. This led to the evolution of Sky's architecture (**Figure 1**).

One fundamental design decision was to eliminate large memory overhead costs by keeping only a small amount of data memory aboard the AP, and to use the system memory to hold the user's problem. "Some APs have (large) internal data memory that requires that the user's problem is brought over from the central processor in to the internal data memory before the problem/solution can start," says Carbone.

"The Sky machine only has to bring in the first piece of the problem, then start processing it. At the same time processing occurs, the second piece of the problem can be brought into it. Arithmetics and I/O overlap each other, which saves on time."

From out of his drawers, Carbone pulled a recent timing comparison with the Floating Point Systems AP–120B to hammer home his point. The dot product timing comparison (**Table 1**) shows that for various sizes of dot products representing matrices from 128 × 128 up to 4096 × 4096, the performance of the Skymnk–Q is actually competitive with that of the Floating Point Systems AP–120B array processor. Not only, in fact, competitive but for vector (row or column) sizes up to 512 elements, actually faster!

The reason is that the AP–120B must explicitly move data into the AP before beginning computations, and out of the AP after computations have been finished. This requires seven calls to the AP library and driver. These calls each involve a context switch and operating system I/O interaction. The Skymnk–Q, on the other hand, does not require explicit input or output of data at all. Moreover, only 2 calls are necessary to perform the identical function that the AP–120B requires 7 calls to perform. Further, each Skymnk–Q call does not involve the operating system, but rather communciates with the device directly through the system's I/O memory page. This reduces the overhead to a small fraction of what the AP–120B must endure.

Up to a certain number of elements, of course. After 4096 × 4096, the Sky computer starts to lose out. What the comparison also indicates is the farcical, misrepresentative term "MFLOP" in the industry. MFLOP (million floating point operations per second) is a peak rating that is a sum of the arithmetic and addition speeds within the multipliers and adders internal to the AP. "It's misleading because it focuses attention on only one element of a system that can't be run anywhere near that speed in the real world," says Carbone.

Jonathan Cohler of CSPI takes up the story: "MFLOPS are not a good measure of a machine's power, especially with pipelined architectures—you'll find they're inefficient and never achieve that maximum."

"What it comes down to is the efficiency of the data movement within the pipeline itself," adds Bruce Monk at Analogic, ". . . and internal data movement usually compromises peak performance." Looking back to **Table 1,** it is interesting that the AP–120B is advertised as a 12MFLOP machine, whereas the Skymnk–Q is rated at 1 MFLOP.

"I think we're lazy people basically and we like something that's easy to measure rather than something that's representative of the system," concludes Carbone.

As Sky Computers continue to create a new window at the low cost end of the AP market, it looks as if the new Analogic machine (the AP500) might do the same in the $25,000 price range. Looking at **Figure 2,** the most obvious innovations are the use of the MC68000 as a central processor, Multibus adapter, and an RS–232 link. "When you run diagnostics, you're host dependent in a classical array processor," says Bruce Monk at Analogic. "Everything has to happen over the I/O, so isolating

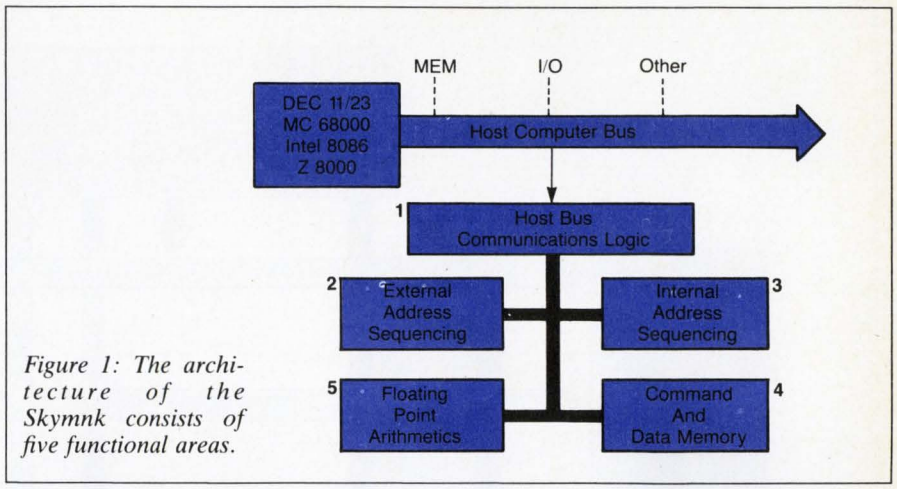

Figure 1: The architecture of the Skymnk consists of five functional areas.

DOT PRODUCT EXECUTION TIME COMPARISON

Matrix Dimension (Row or Column)	PDP–11/34 Time (ms.)	AP–120B Time (ms.)	SKYMNK–Q Time (ms.)
128	78.7	3.88	1.83
256	158.0	4.58	3.17
512	316.0	6.12	5.00
1024	632.0	9.37	11.70
4096	2530.0	29.60	43.30
∞	linear	DMA Rate of PDP–11	DMA Rate of PDP–11

Table 1: Dot-product execution time (courtesy Sky).

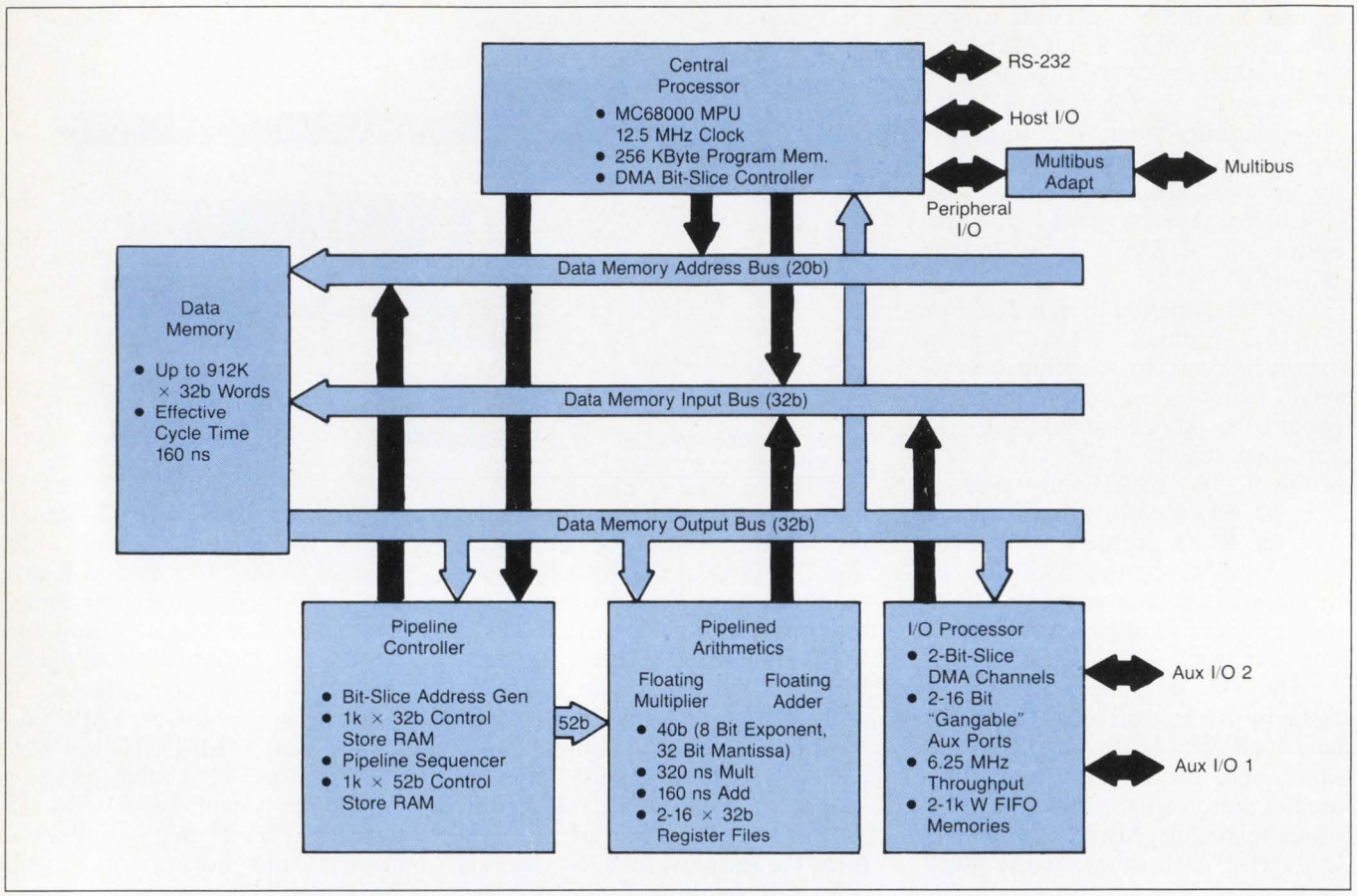

Figure 2: The AP500 from Analogic uses a Motorola 68000 as a central processor.

the problem between host and array becomes a problem. We wanted an RS232 port so the user could plug a terminal in directly, and run diagnostics on the AP."

"A lot of people also want to add peripherals: a Winchester drive, an LAN controller, etc., etc. . . . This led to our selection of the Multibus adapter as a way to do that." The Multibus card fits into the conventional backplane of the user's own system.

Initially, the use of a 68000 in a machine that operates as fast as an AP may seem to be a peculiar design decision, when other controllers tend to be based on fast bit-sliced machines. "A bit-sliced machine's claim to fame and main purpose in life is speed—that's what makes it so good," says Monk. "But to then spend a lot of effort in development of general purpose software to run operating systems and I/O kinds of things is a misapplication of the device," he adds. The Analogic AP500 control processor's tasks include running the AP executive to control the host communications and setting up the DMA controllers; duties that normally fall under control of the control processor are handled by other hardware components such as the 2901 bit-sliced address generator.

The AP500 may be used in a stand-alone configuration. "Supose you want to build a vibration monitoring system," states Monk, ". . . you can connect up a terminal, do A/D through the AUX ports or Multibus, run FFTs, and get the 68000 to do limit comparisons. Then you have a general purpose computer and an array processor in one package." With the introduction of the AP500, Analogic appears to be changing another misconception of the array processor as a machine that is not capable of any general purpose computation.

When making a limit decision on data that has been processed by the AP, the data must typically be transferred back to the host. "With the 500, a decision can be made by the 68000, and the host can be told if a limit exceedence occurs. The 68000 looks straight into data memory, looks at the words, makes a decision, and only if some action is required by the host does it do anything. The whole task can run in the AP," concludes Monk.

Programming the AP

Many array processor manufacturers supply a Fortran compiler with extensive application libraries so that the user can stay in the Fortran language and the operation of the AP is transparent. Characteristic of the end-user environment, according to Bruce Monk, the user may pay a tremendous penalty in performance due to host overhead.

The OEM user may want to optimize his problem, but not use functions classically in the Fortran

library. Supporting multi-level programming in Fortran, assembly language, and microcode, is a concept that both Analogic, CDA and others support for exactly that purpose.

Analogic's AP500 application programs can be written in host high-level language, host assembly language and AP500 assembly language that is an extension of the MC68000 assembly language.

The MSP–3000 from CDA (**Figure 3**) also provides for the development of software at levels below Fortran. At the highest level, a Fortran program operating on the LSI–11, PDP–11 or VAX can call an array library to operate on arrays in the host or in the data memory of the MSP–3000. Array functions can also be directly called from the host computer assembly language.

CDA's "Mini-Language" is similar in form to programming a mini in assembly language and allows the user an intermediate step in programming level.

According to CDA, most APs are programmed at the microcode level when maximum speed and efficiency are required. Apparently, in AP code, 90% of execution time is spent on 10% of the code and it is desirable to microcode the 10% for faster operation. A complete microcode development package is available for the MSP–3000.

Looking back at **Figure 3,** it is interesting to note that CDA is not only in the AP business but also supply a complete image processing system (the Delta–100) based on the MSP–3000 and the DPD–3000 display generator.

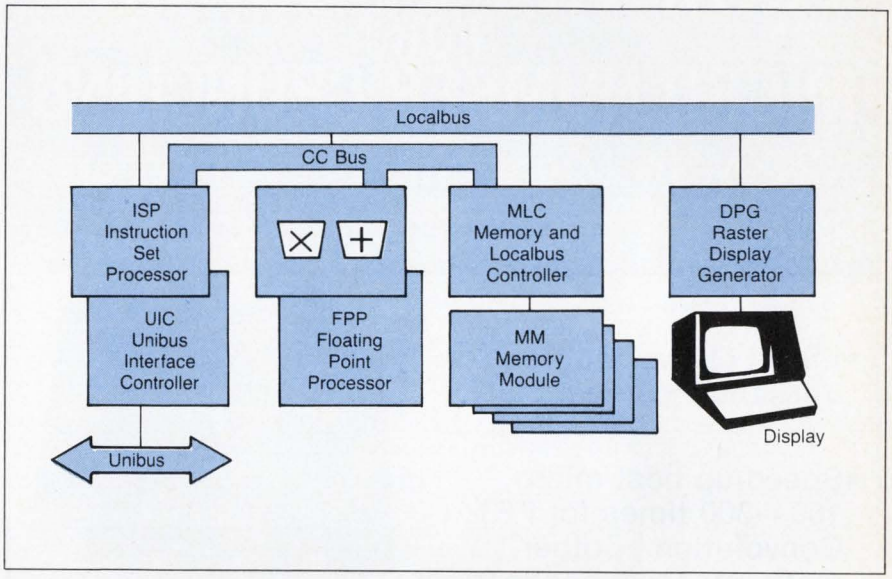

Figure 3: The MSP–3000 from CDA is used in the company's own image processing system.

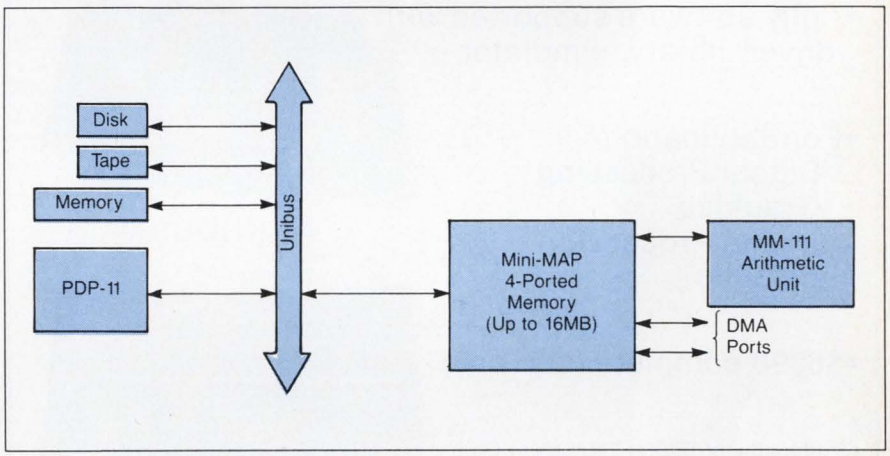

Figure 4: The shared memory of the MiniMap from CSPI.

Shared-memory

The concept of shared memory in an array processor is one that has stirred many a controversial argument during the preparation of this article. Supported by CSPI (for example, in their latest product, the MiniMAP, **Figure 4**), the idea behind the concept is to provide a mechanism for the host and AP to access the same memory without having to transfer date to and from the host and the array processor.

AP manufacturers who do not support the concept of shared memory disagree with the approach. "The price of the memory so far exceeds the price of the AP that the viability of anyone plugging in large amounts of memory is negligible," one marketing manager stated.

Another allegation was that the shared memory concept locks you into an approach of using special high-priced memory that only the manufacturer can supply. "Shared memory is *not* more expensive to buy from the array processor company," retorts Jonathan Cohler at CSPI.

"What our competition neglect to say," says Phil Blake, Marketing Manager at CSPI" . . . is that for particular problems the user may have, shared memory is the only viable solution since it eliminates the time in data transfers between host and AP, which may be critical in I/O intensive work."

Add it on

In the fixed point world, Numerix are taking an approach that allows the user to add on extra processing power in functional modules without the need for buying two APs to do the job (**Figure 5**). Each of Numerix's arithmetic processors contains its own data memory and program memory. A modular interrupt-driven programmable bus controller provides arbitration of data transfer conflicts.

Component processors include data procesors (DP) and interface

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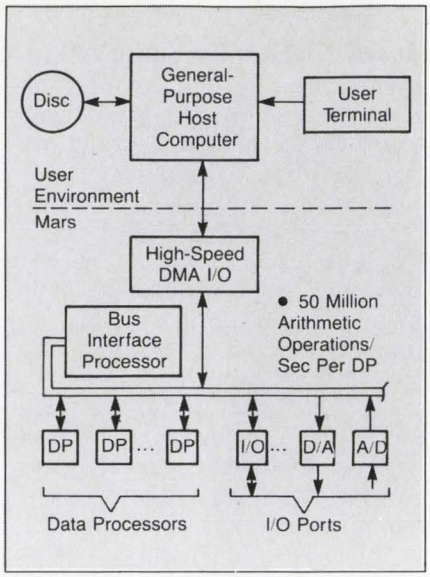

Figure 5: The Mars-232 from Numerix allows the user to add on modules.

processors (IP) along with various interfaces to the outside world for interaction with the host mini or additional digital and analog devices.

Although multiple data processors augment the arithmetic power of the system, if the problem is very I/O intensive then tying up the high-speed bus may not gain the user any significant advantages.

As well as the Mars 232, Numerix can also supply a one board AP (the 132) to the OEM that can be modified to the user's particular application.

According to Ken Wilmer, Director of Software at Numerix, "the architecture of the 132 is the same as that of the 232 with the exception that the 132 has only one Data Processor as opposed to multiples on the 232."

Harold Messias, Vice President of Marketing at Numerix was keeping tight-lipped about next year's product plans. It looks as if a Mars 432, a floating point machine, may by announced around February '83, breaking the company's exclusively fixed-point image.

Look for further exclusive details in *Digital Design*'s AP issue in April, '83.

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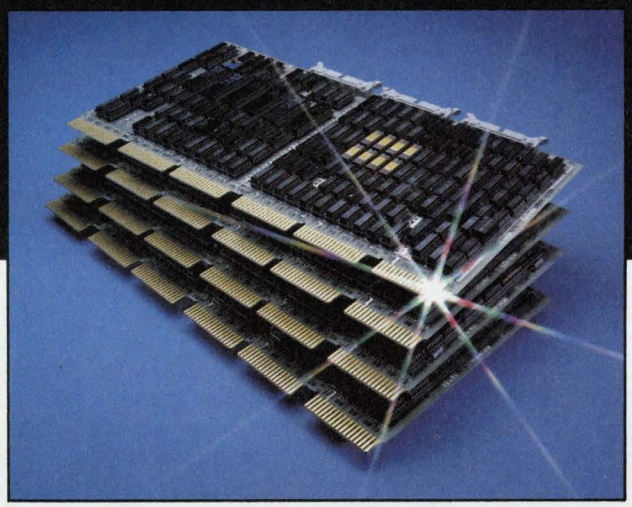

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the Aptec Computer Company Portland, OR, introduced its first product this year in the form of the DPS–2400 (**Figure 6**). The idea of the DPS is to provide multiple attached APs with control and transfer resources allowing them to operate at full capacity.

Elements of the DPS architecture are the peripheral device adapters, the internal bus structure and the mass memory. The data interchange adapters provide an interface for peripheral devices that may include the Unibus compatible APs, disk drives, tape drives and special purpose subsystems such as graphics or image processors.

The backbone of the DPS–2400 is the data interchange bus, or DIP. The DIP's demonstrated bandwidth of 24 MBytes/sec will support the simultaneous I/O requirements of up to 8 APs, according to Aptec. As one AP serves to offload computational tasks from the host, the DPS–2400 will off-load support tasks, according to the company, allowing the user to integrate multiple AP systems.

In announcing the product line, Aptec discussed applications in the reservoir modeling of oil fields. Recent purchases by Exxon and Mobil of Cray–1s indicate the kind of processing power needed in these applications. Aptec's aim is to provide a cost-effective alternative by allowing the user to hook together several FPS–164s.

Summary

Next year should prove to be an interesting one for both the AP designer and user.

For the designer, it looks as if new CMOS multipliers are about to spring forth from the semihouses (Analog Devices have already announced their 8 × 8 APSP–1080 and the 16 × 16 DSP–1016), and it will be interesting to see what advantages Analogic takes of new additions to the MC68000 family in their controller.

For the user, new introductions at the beginning of the year will provide an even greater choice. The industry presently waits eagerly to see what twists the giant Floating Point Systems will take to improve on its low-end FPS–120B—and Numerix's 432 may hold a few surprises.

One word of warning. Most comparative cost/performance data published by manufacturers may be based on one particular narrow problem/solution that promote the advantages of his product. The reader should be aware of the complete scope of his problem before approaching the AP manufacturers, where he may be blinded by carefully constructed comparative data. □

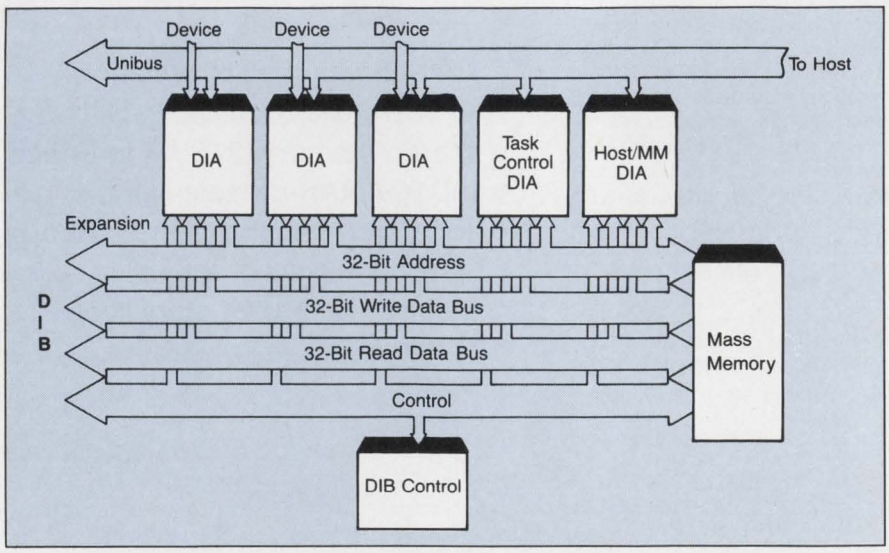
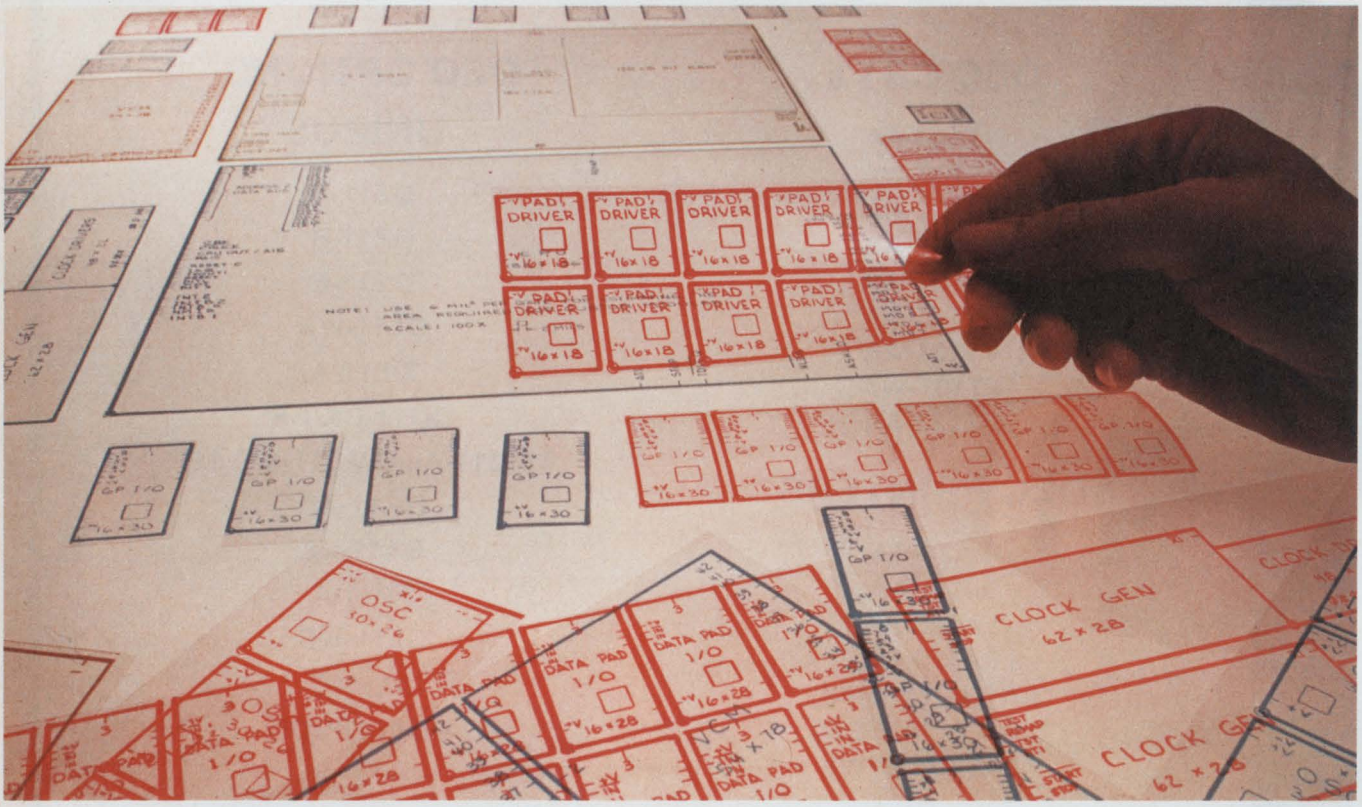


Figure 6: A building block approach from Aptec.



CAD Tools Speed Development Of Custom μCs

by Jerry R. Bauer and H. Lyle Supp

The optimal logic solution for a systems designer is to incorporate a custom μC into his design. This has the advantage of reducing both the size and the cost of the overall system. However, the cost and necessary development time of a custom μC is often prohibitive. Standard, off-the-shelf μCs, on the other hand, result in significant compromises in system capabilities.

The alternative to these options is the Alterable μC from American Microsystems (*Digital Design*, August, 1982). This approach reduces both design cost and development time. The entire process of the creation of a custom μC, from initial design to final production, relies heavily on CAD techniques that eliminate the possibility of design errors, and keep design time spans and costs from increasing rapidly with design complexity.

Consider the design of a computer-controlled fuel injection and ignition control system. First, a system specification is defined. The system is intended for the automatic control of six individual fuel injectors, with simultaneous control of the ignition. The inputs to the system are:

1. Engine rotation pulses generated by a sensor mounted on the engine damper. The pulses are low level and occur at the rate of 1 pulse every 90° of crankshaft rotation.
2. Throttle position voltage from a throttle transducer.
3. Engine synchronization signal which signals the beginning of the combustion sequence and comes from the distributor.
4. Engine temperature and mass air flow inputs from their respective transducers.

Outputs from the system are:

1. Six individual injector drive signals.
2. Ignition timing pulse.
3. Alphanumeric display.

Figure 1 shows the system block diagram.

The system as designed on paper has certain unique problems. First,

Extensive CAD techniques help keep design errors and time and cost over-runs in check.

Jerry R. Bauer and H. Lyle Supp are with American Microsystems, Inc. (a subsidiary of Gould, Inc.), 3800 Homestead Rd., Santa Clara, CA 95051

the signal from the engine damper does not resolve the engine rotation to the degree needed. A circuit must be designed to insert the needed pulses; one per degree of crankshaft rotation is sufficient. Second, the input signals are analog or at least low-level digital signals, and must be amplified and conditioned. Third, it is apparent that the CPU cannot control the injectors in real time; software loops cannot be used to give the precise timings needed: they must be independent of CPU processing. Fourth, the system will be subjected to elevated temperatures and high levels of electrical noise.

After the block diagram of the system is defined, the customer meets with the AMU engineering staff, and together they partition the system into the needed functional cells. **Figure 2** shows a typical partitioning of this system. Five cells are required: the digital input amplifier, the pulse inserter, the 9-bit throttle A/D converter, an injection counter, and an ignition converter. The last two cells are minor alterations of existing family cells. Other cells which are required are: RAM/ROM (3K bytes of ROM on-chip and 1K off chip, and 256 bytes of RAM), some general purpose I/O cells, a serial communications cell, and finally the CPU cell.

Next, the system is breadboarded using the prepackaged equivalents of the existing cells and the custom cells developed for this application, and is assembled on the AMU Emulator board. This board has the CPU, space for memory (RAM and ROM) and space for the functional cells (standard and custom). The emulator system (Gould-Millennium 9508S with the AMU/PR emulator option and POD) communicates with the Millenium 9520 Software Development System or any of many other host systems. The software is developed and tested by actual engine tests running in real time. Finally, road testing must be performed. The program is placed in the ROM of the AMU custom chip, and the chip is fabricated and used in the car under normal operating conditions. **Figure 3** shows this simplified flow in the typical custom AMU design.

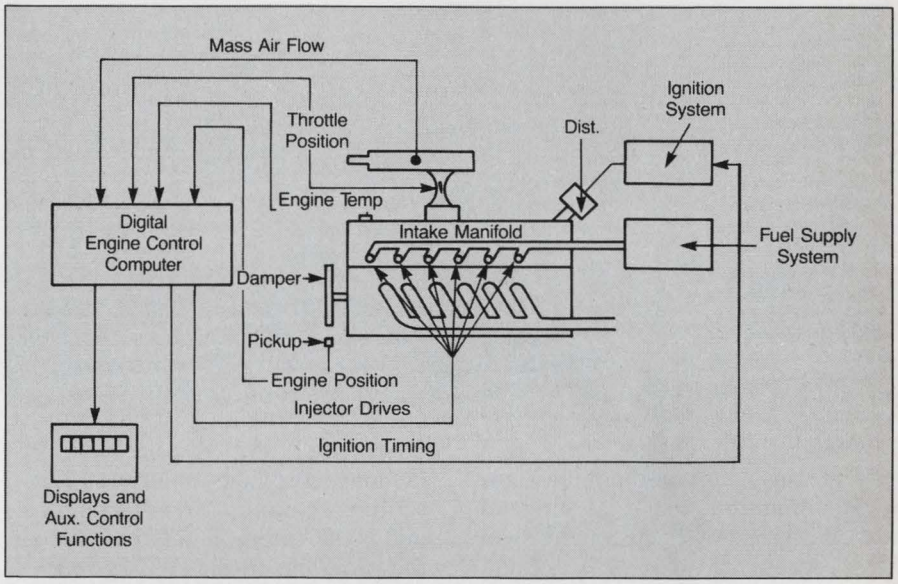


Figure 1: Engine control system block diagram.

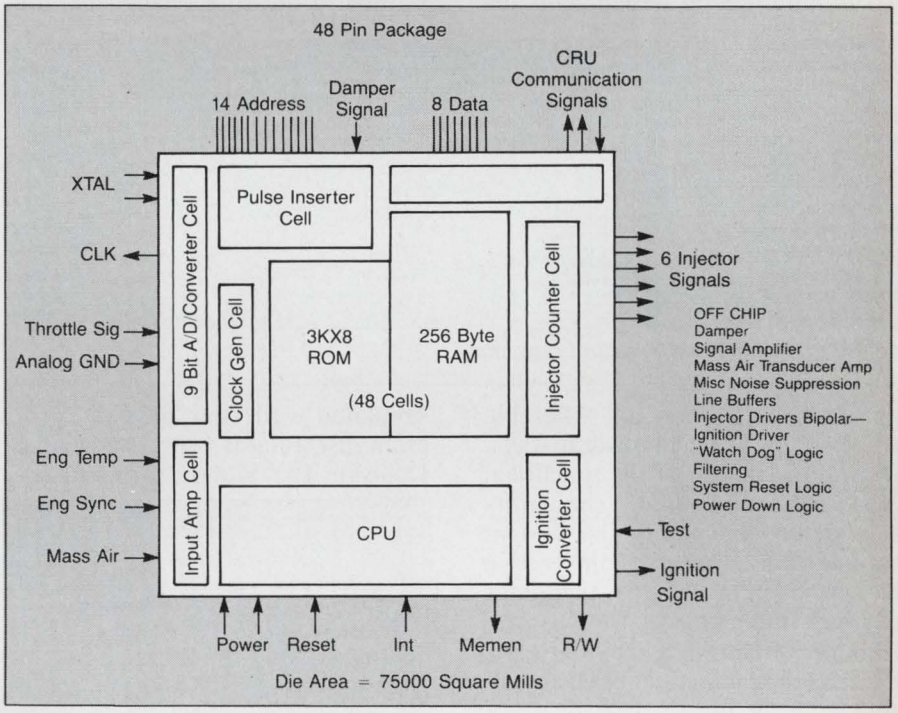


Figure 2: AMU silicon partitioning for engine control application.

The development cycle of a typical functional cell can range from 8 weeks for a simple function to 20 weeks for a complex function. This same sequence of steps may be followed for the development of relatively simple integrated circuits, as well as functional cells. More complex integrated circuits can be dissected into functional subsystems that can then be developed in parallel, for later integration after they have been individually designed.

The physical constraints of silicon manufacture require that the final shape of the microcomputer be rectangular. The placement of the functional cells to give a rectangular chip can be done by a systems designer with the aid of small-scale mylar decals or interactively with AMI's CAD tools. The ACT design system is an integrated computer-aided design system available

SIDS—The Interactive Mask Design Tool

The SIDS system (Symbolic Interactive Design System) is instrumental in the design of an Alterable μC. The mask layout is accomplished by incorporating the functional cells and the necessary interconnections on an alphanumeric color CRT. Symbols of various colors indicate elemental mask configurations, such as those for transistors and inter-level connections. These are combined as necessary by the layout designer into the required topological configurations. All mask levels are designed concurrently, and the software checks and identifies design rule violations in real time, for immediate correction. The SIDS system supports the Alterable μC's library of functional cells. A functional cell may be called from the library and incorporated directly into the system being designed, or it can be modified as needed and reinserted into the library, for later incorporation. The SIDS system layout can be compared with the circuit description (in the BOLT language) and connectivity variances can be flagged, corrected, or justified. When the masks for the Alterable μC are completely designed, the symbols are converted directly into the format required by the numerically controlled mask generation equipment, bypassing the conventional data-capture stage and its associated tendency to introduce errors.

for MOS/VLSI design. The ACT system uses a common database for logic simulation, mask layout, and test design. AMI customers will have access to the ACT system through timeshare, or joint designs.

Computer-aided design tools enter into the process of Alterable μC customization in several ways. During the design of the functional cells, logic and circuit simulators help debug and verify the design, and AMI's Symbolic Interactive Design System (SIDS) facilitates physical implementation. This system has already been used to design standard functional cells available from the library. In the case of custom functional cells, these tools are again used, both in the design of the new cell and in testing its performance in concert with the other system elements.

The implementation of functional cells follows this sequence; First, the requirements of the block are specified. This activity is a part of the larger specification of the entire system, which may entail the design of several functional cells. Second, the design is planned and written in a hardware description language called the BOLT language (Block Oriented Logic Translator). This language provides a means of describing complex logic functions, and is the common data base for all the programs in the ACT system.

Third, the functional cells, as described in the BOLT language, are simulated with the SIMAD program (SIMulator with Assignable Delays). The SIMAD program allows verification of the characteristics of the logic, as well as that of some of the parameters of the physical implementation. This procedure is iterative, so the designer can modify the design and resimulate it until it functions correctly. When the designer is satisfied, he verifies any special circuitry and analyzes critical paths with a similar technique using the AMI–SPICE circuit simulation program, and PATH analysis program. There are other specialized tools available to the designer, especially for the development of active or passive linear circuitry.

Fourth, the mask layout is designed. The SIDS system provides the layout designer with an efficient method of converting the logic description to physical structures. This helps eliminate errors in the

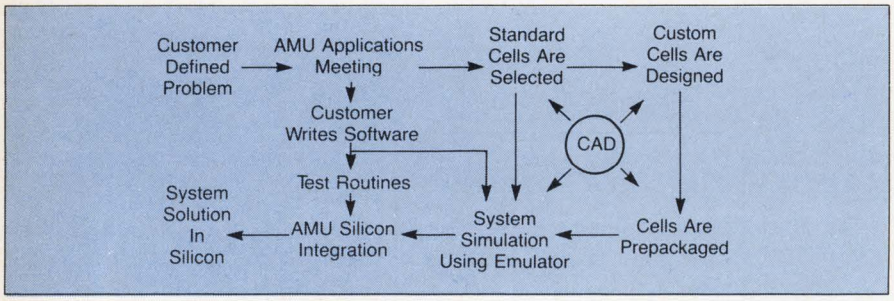
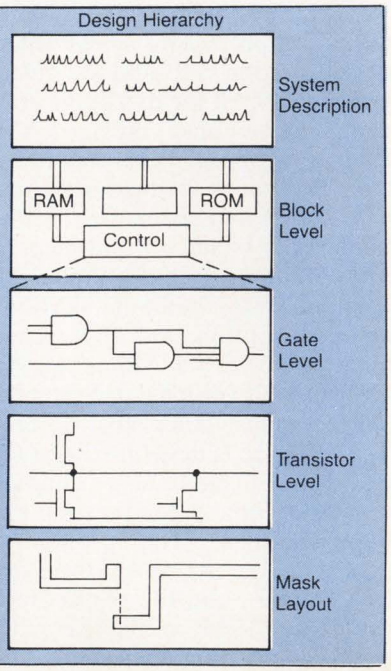
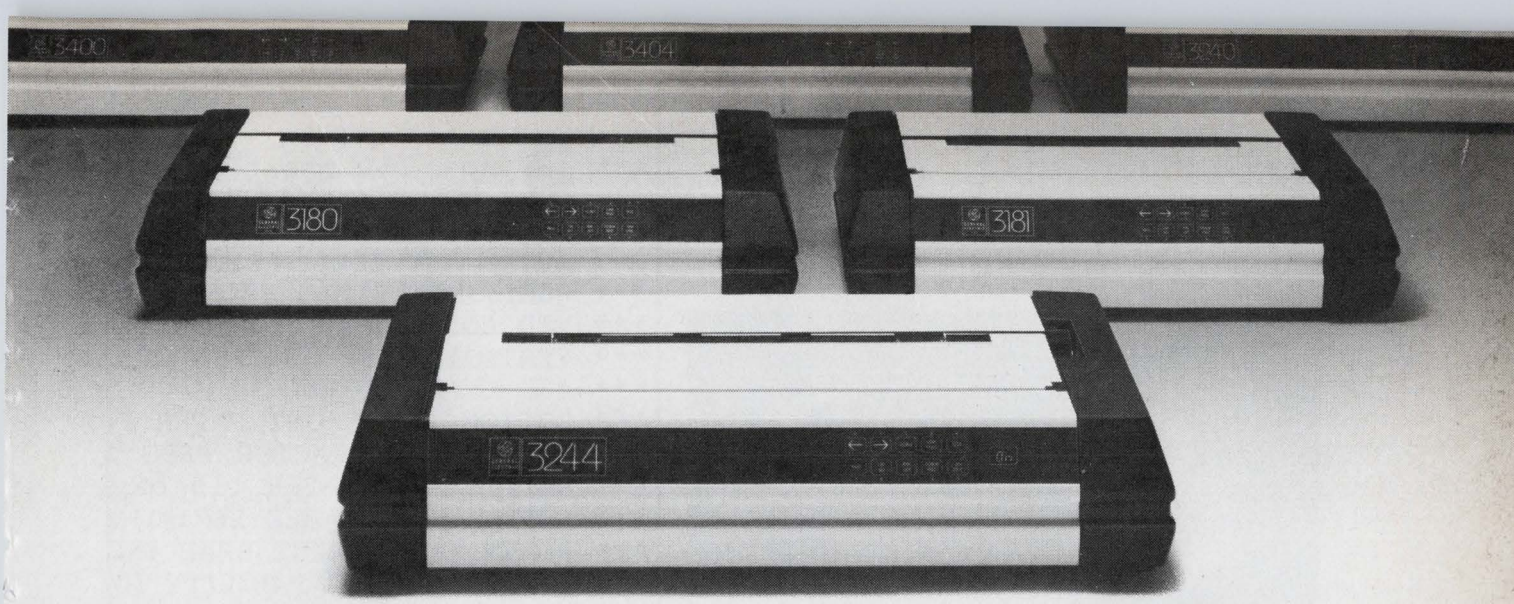


Figure 3: Typical AMU custom flowchart.

BOLT—The Common Database

For many of the CAD tools in AMI's repertoire the BOLT language provides a common input format. This is a hierarchical language, allowing the designer to refine the circuit description successively from the system level down to the discrete transistor level. The BOLT language also contains a flexible macro capability with unlimited nesting and parameter passing mechanisms. Paramaters and circuit elements can be assigned mnemonic names, providing more readable listings and output. The definitions of the basic types of logic and circuit elements are supplied to the BOLT compiler externally. This means that a change to a basic element can be accomplished without changes to the language itself.





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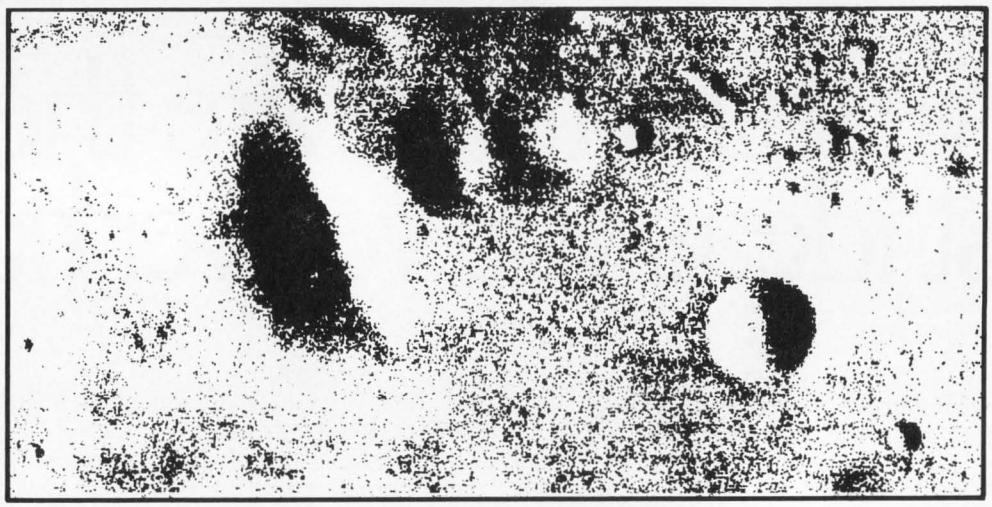

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Design Area	Element	Acronym
Common Database	Block Oriented Logic Translator (Compiler)	BOLT
Logic Design	SIMulator with Assignable Propagation Delays	SIMAD
	PATH Analysis Timing Verification Program	PATH
	Register Transfer Language Simulation	RTL
	Propagation DELAY Calculation from Mask Layout Capacitance	DELAY
Circuit Design	Circuit Simulator	AMI SPICE AMI ASPEC
	Switched Capacitor Analysis Routine	SCAR
	Pole-Zero Location Analysis	PZSLIC
Mask Design	Topological Layout Planning Aid for Full Custom	LPA
	Symbolic Interactive Design System for Full Custom Mask Design Including Design Rule and Continuity Checking	SIDS
	Automatic/Interactive Placement and Routing for Standard Cells	CIPAR
	Automatic/Interactive Placement and Routing for Gate Arrays	GAPAR
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	Capacitance Calculation from Mask Layout	CAPACITANCE
Test Design	TEST Pattern GENerator to Format Compressed Test Patterns	TESTGEN
	TEST PROgram Generation	TESTPRO
	FAULT SIMulator	FAULTSIM

conversion process, and yields a mask layout in a format that can be automatically verified against the circuit description in the BOLT language. There are also other tools available to the mask designer to aid in planning and implementation of the layout. At the same time, the system designer can use the SIMAD, TESTPRO, and TESTGEN programs to exercise the logic and generate test vectors to validate the functional cells after manufacture.

Fifth, the functional cells are manufactured and validated, and the chip's design and mask data are placed in the library for use in the customization of an Alterable μC. □

Figure 4: Each element of AMI's CAD technology is a stand-alone computer program, written in FORTRAN or Pascal. As a result of this, the entire package, or smaller portions of it, can be easily transported to other design centers. The common database, the BOLT language, forms the input format for many of these programs.

Printers: The Industry, Technology, and Markets

by Jerry Borrell

This article is the first in a series that will be appearing throughout the 1983 calendar year. Beginning in January *Digital Design* will present "Industry Spotlights" that will provide our readers with insight into the technology, trends, markets, and manufacturers of key areas of industry. January, for example will focus on the data communications industry. Dr. Walter Bolter, formerly of the U.S. House of Representatives Subcommittee on Telecommunications, will analyze the four aspects of the communications industry mentioned above.

This month we initiate the in-depth analysis of our spotlights in the area of printers and printing technology. Our intent is to provide an overview of their respective fields of interest, and thus assist in the day-to-day *design process.* Perhaps more important is the emphasis these articles will place on trends and issues that will occur over the next five years. We believe that as digital design leads to the convergence of engineering disciplines within computing, we must examine the ways in which these changes are taking place.

One of the difficulties in writing an article such as this for the area of printing technology is that the current enthusiasm for new technologies may overwhelm perceptions of the marketplace as a whole. Color, graphics, and print quality are intensely competitive offerings, which lead to marketplace promises that cannot always be fulfilled. In distinguishing between the real and new—the installed base of devices and market shipment trends—one needs in-depth market research. The information of the International Data Corporation (IDC) and Frost & Sullivan were found especially useful in making this evaluation of the printing industry. Based on these sources we have noted (**Figure 1**) three basic classifications within the printing area: products classified by speed of printing, by method of printing, and by their technique of creating characters. We examine each of these three classifications in terms of their market, their technology, and the trends in their development.

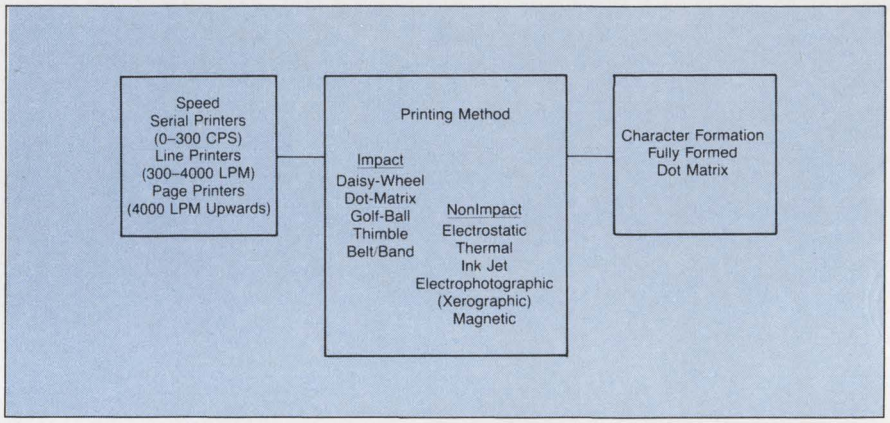

Figure 1: Printers may be broken down into the above printing technology classifications (based on data from International Data Corp.)

Market Growth

The growth of the market for printers roughly parallels that of computer technology. As areas related to computing such as word processing, communications, reprography (xerography), and desktop computing have grown, so has the demand for printers. There were an estimated three million printers installed at the end of 1980, but in 1981 alone approximately 1,300,000 units were shipped. This translates into annual rates of growth of 31% since 1978.

Frost and Sullivan predict an average rate of growth of 20% through 1987, with a peak in 1984 of 40% declining to 9% in 1987. However, determining where the growth will occur for any specific classification is difficult. The ability of any of the methods of printing to

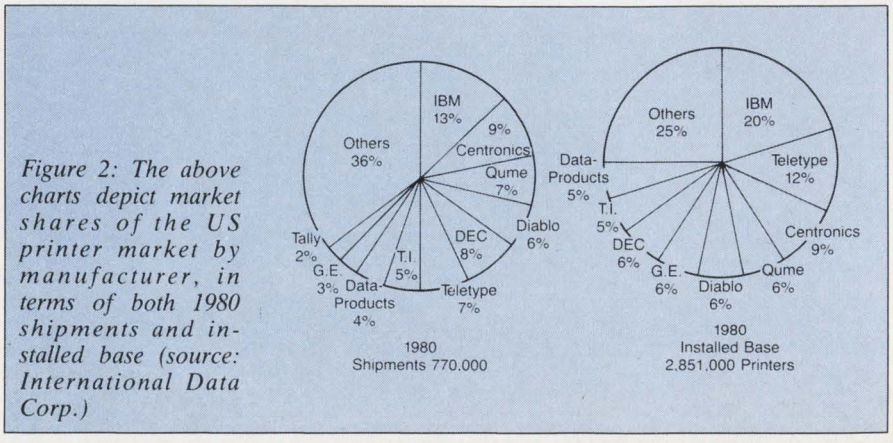

Figure 2: The above charts depict market shares of the US printer market by manufacturer, in terms of both 1980 shipments and installed base (source: International Data Corp.)

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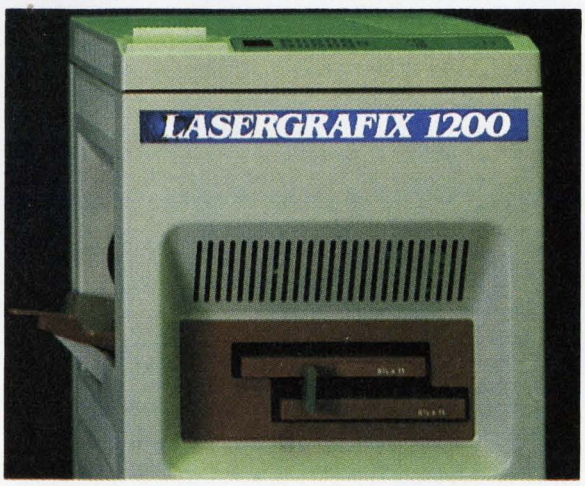

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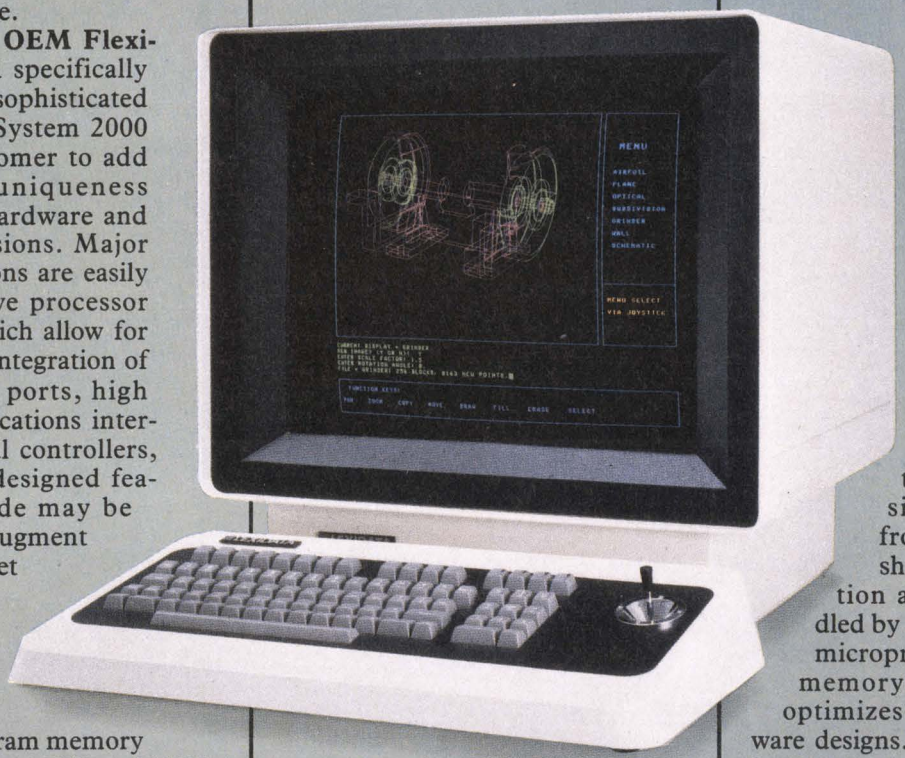

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use plain paper is a key factor because plain paper equates with low cost. The cost of the devices, and of the necessary supplies (paper, toner, etc.) is a primary factor in the market, as it influences purchases and creates new areas of competition. The Japanese manufacturers, for example, make a practice of entering at the low end in order to establish themselves. The current high prices of many areas of printing devices thus provides a market for their products.

Finally the influence of IBM should be noted, and IDC indicates that it has a great deal of power in printing technology because it has been one of the developers of key areas such as high speed belt and ink jet devices, and because of the economic value of the plug compatible market. The newly announced IBM 5225 which allows graphics, bar codes, programmable fonts, and non-Roman characters is typical of their products. Not only is its output flexible, but its technique—dot matrix—gives the technology an IBM imprimature of reliability. The secondary effect is to give an economic boost to the long term well-being of manufacturers such as Printronix and Mannesmann-Tally, who are major producers of dot matrix devices.

Printer Classifications

Speed. The categories of systems according to speed are most often defined as serial, line, and page printing devices. Serial printers make up over 80% of all printers shipped, line printers 14%, while page printers make up only 1% of the market. However, in terms of dollar values, serial printers make up only 57%, line printers 8%, and page printers almost 35%. The latter are so high because their cost per system may be 150 times that of a serial printer.

Technological advances are increasing the application areas of many printer categories, providing more alternatives for system designers.

Serial printers print one character at a time. In this sense, serial refers to the method of laying down type and not to the interface (which may be either serial or parallel). Until recently the upper performance range for serial printers was around 300 characters per second (CPS). Dot matrix technology has matured to the point where serial printing speeds are so high that they actually compete with low end line printers. Florida Data Systems, for example, manufactures a matrix printer with 600 to 800 CPS.

Despite the merging areas of speed for serial and line printers, they are still widely separated in price. Because the majority of the markets are found in the lower speed area, serial printing appears at times to hold a greater market share than is in fact the case.

Speed for line printers ranges from around 1000 to 4000 lines per minute, whereas page printers are defined as printing over 4000 lines per minute. At such high speeds it is clear why impact printing, with all of its mechanical frailities, is limited. Page printers from IBM, Xerox, Honeywell, and Siemens all offer speeds from 8000 to 20,000 lines per minute. The high cost of these page printers, eventual market saturation, and competition from slower page systems is affecting the long term prospects for this market segment. The market for the fastest systems is expected to grow until the mid '80s and then decline markedly as lower volume page printing systems (up to 30 pages per minute) become available.

Printing method. The basic categories of printing are impact and non-impact techniques. Impact devices create an image through the mechanical process of imprinting ink on paper. Some mechanisms strike from the front: daisy wheels, golf-balls, and dot matrix; while others strike from the rear: drum, chain, and belt/band systems.

Non-impact printers have neither ribbon nor striking mechanism. The impact printers are overwhelmingly more important, making up over 92% of total printer shipments in 1980. The installed base of non-impact printers, however, is somewhat lower at 85% because of the high number of thermal pointers shipped. The advantages of impact printers include the use of plain paper, the ability to produce multiple copies, and lower cost. On the other hand, they are slower and more noisy than non-impact printers. Non-impact printers are generally faster, offer more quality in areas such as graphics, and color, but often require special paper and higher initial investments. In terms of market share, 9% of serial printers, 3% of line printers, and 100% of page printers are non-impact.

Non-impact printers include ink jet, magnetic, electrophotographic,

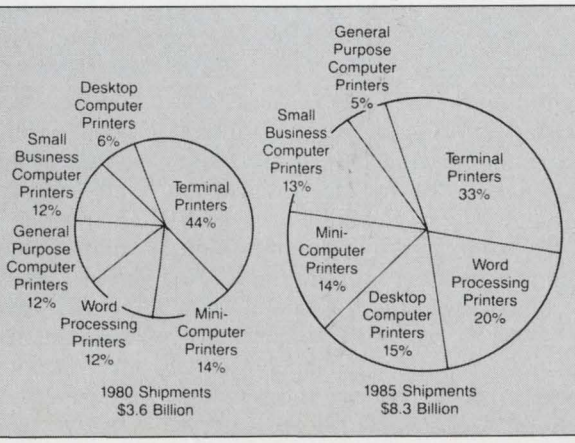

Figure 3: Dollar value break-downs of US printer shipments for 1980 and 1985 show market share increases for word processing printers and a decline for terminal printers (source: International Data Corp.)

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Hi-G Co.		Skokie, IL	Write 190
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Honeywell Information Systems		Dallas, TX	Write 191
Minneapolis, MN	Write 232	Trilog	
IBM		Irvine, CA	Write 192
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Integral Data Systems		Hauppauge, NY	Write 193
Milford, NH	Write 234	Wang Labs.	
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Kent, WA	Write 236	Xerox	
Memodyne		Stanford, CT	Write 196

thermal, electrostatic, and electrosensitive techniques. Of these, the latter three require special paper. While non-impact printers are in the minority, there is an increasing amount of research and development in this type of printing, due to the demand for graphics, speed, and increasing convergence of functions such as office systems, facsimile, and copying.

Among the existing non-impact technologies, the market shares are divided as 71% for thermal printers (the bulk of which are in portable terminals), 20% for electrosensitive printers (silver paper devices such as Tektronix used in scientific and technical graphic applications), 4% for electrostatics (with the majority in CAD & graphics), and 3% for ink jet. At the high speed end, page printers comprise the remainder, for systems which are fastest and most expensive. Other factors which will increase the use of non-impacts are the development of multiple copy capability, color, and increasing quality despite the dot matrix character formation.

Dot matrix and fully formed. Dot matrix printers create characters through the use of a variable matrix of contacts, while fully formed characters are those imprinted directly from a mechanical print

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source. Recent growth of dot matrix devices has given them a 68% share of the market, and their recent use by IBM, Teletype, and General Electric will enhance this market share.

Fully formed characters offer the advantages of the lower price devices and higher quality within certain applications, but dot matrix quality is increasing to diminish this advantage. Dot matrix printers already provide advantages over mechanical fonts such as faster speed, lighter weight of the print head, lower price, and variable output. The latter is one of the most powerful uses, allowing bar codes, graphics, different type fonts, and non-Roman characters to be produced on the system. The disadvantage in dot matrix quality is found in the lower price range, where the character matrix is made up of 5 × 7 points. At a higher price, however, are systems such as the Xerox 9700 with 90,000 dots per square inch, affording much higher quality images.

Market Share

There are several categories of markets for printers: printers used in computer systems, printers associated with applications, and the OEM vs. end-user markets.

Computer systems use of printers. The markets in this category include general purpose computers, small business computers, minicomputers, desktop computers, and terminal printers. The majority of printers used on general purpose computers are line printers, and this category of system is predicted to decrease after 1982 because of a general shift in the computer industry. This decrease is due to small computer growth and the high reliability of printers already installed. Large computers, on the other hand, require an average of 2 printers per device, so their effect on the market is disproportionate to what one might expect.

Small business computers are given a more prosperous growth outlook. About 44,000 were shipped in 1980 and this figure is predicted to double by 1985. The minicomputer market is very deceptive, with only .65 printers installed per system. This is because of their application in diverse areas such as process control and industrial applications. The remainder of the markets—desktops and word processing systems—are experiencing the most dramatic growth. While 243,000 printers were shipped during 1980 for desktop computers, IDC very conservatively estimates the figure to grow to 1.5 million by 1985. While low cost dot matrix printers benefit most from desktop sales, letter quality printer manufacturers such as Qume, Diablo, and NEC also benefit because of the application of desktop computers to text editing. The major manufacturers in the dot matrix market for this area are Centronics, Integral Data Systems, Anadex, Axiom, Okidata, C. Itoh, and Epson.

Figure 4: This demo of the Qantex 7030 dot matrix impact printer shows the character and high density graphics capabilities of the printer. The image is a bit image display created from gray-scale values and interpolated into a black/white dot image.

The word processing market is less straight forward. IBM still holds the lion's share of this market because of its installed base of 200,000 Mag Card Selectrics, which are no longer being sold. Daisy wheel printers have become the new growth area here, with Qume (ITT) and Diablo (Xerox) being dominant. Secondary suppliers include: C. Itoh, Pertec, Ricoh, Wang, Vydec, and IBM. Olivetti has recently established a growth area in very low cost daisy wheel systems with its $500 entry. Firms such as General Electric, Centronics, IDC, and Epson are claiming a larger share of this market with

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MEDIUM SPEED IMPACT DOT MATRIX 132 COLUMN R.O. PRINTERS

Manufacturers Model No.	List Price	Print Speed CPS	Matrix Character	Size of Buffer	Noise	Dot Graphic D.P.I.
Hi-G 9/132PS Durawriter	$1395.00	165 75	9 x 9 18 x 9	3,422	58dbA	72 x 72
Texas Instruments 810	$1895.00	150	9 x 7	256 to 2,048*	72dbA	72 x 60 Optional $600.00
DataSouth DS-180	$1595.00	180	9 x 7	2,000	68dbA	75 x 72
DataRoyal 5000C	$1695.00	165	9 x 9	512 to 2,048*	68dbA	72 x 72 Optional $100.00
Okidata ML-84	$1495.00	200 50	9 x 9 13 x 17	2,048	72dbA	72 x 72 144 x 144

NOTE: Chart based on manufacturer's information available as of October 1, 1982
*Optional @ extra cost

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their "correspondence quality" dot matrix printers, but the daisy-wheel is dominant for professional applications and business.

The phenomenal rates of growth are among the desktop systems, with more than 45% increases, followed by the word processing market with growth rates at approximately 20%. It is the growth of the latter which is causing some of the decline in the minicomputer and small business computer printer sales.

Applications areas for printer. Historically, there have been four primary markets for printers: communications, data processing, document creation, and xerography or reprographics. Today, however, secondary market segments of great importance are developing, including: facsimile, time sharing, office automation, printing, and intelligent copiers. The data processing applications are defined above. Data communications, a second important area, remains important in terms of growth but is undergoing change. Terminal printers have been mainly the "receive and send," and "receive only" type printers in installed markets. Today these systems are giving up market share to portable computers, and CRT/printer markets. The current majority of send and receive is in portable terminals equipped with acoustic couplers used for data base access, with Computer Devices and Texas Instruments being the major producers. Receive only terminals have been dominated by Teletype, General Electric, and Data Products. Unlike the send and receive, however, the receive only terminals are predicted to continue to undergo growth because they can be used as slave printers for CRTs. Other keyboard linked devices include airline ticket printers and mainframe I/O devices which play an important role in specialized markets.

OEM vs. end user market. OEMs control the largest market share in terms of units shipped, but have a smaller share in terms of dollars, because the majority of systems shipped are lower cost serial printers. 90% of OEM shipments are serial printers, and 75% of end user shipments. The end user share of the marketplace is almost entirely captive to mainframe sales of computers. IBM holds almost 70% of this end user market for printers, related to its sales of computers. However, Honeywell, Burroughs, Sperry, DEC, Data General, Hewlett-Packard, and Wang also benefit from this market. DEC and Diablo are primary OEM printer sellers in terms of markets and their printers appear under many other manufacturers' imprints.

OEMs control the largest market share in terms of units shipped, but have a smaller share in terms of dollars.

Manufacturers

The top printer manufacturers in terms of both systems shipped in 1980 and in terms of installed base include in approximated order: IBM, Teletype, Centronics, General Electric, Qume, DEC, Diablo, Texas Instruments, Wang, Computer Peripherals, NCR, Data General, NEC and Integral Data Systems. The majority of these producers manufacture for the OEM market. Recently, Japanese manufacturers have made significant inroads into printer markets. The most important area in Japanese competition has been among the serial printers with NEC, Epson, Okidata, and C. Itoh providing the bulk of imported units sold.

IBM remains the largest producer of serial printers, but evaluations of this may change with the vast number of Epson printers sold to accompany the 1.5 million personal computers sold in 1982. The next largest are Teletype, and Centronics (which sells printers to Tandy for the Radio Shack computers). Third and fourth place in the serial market goes to Qume and Diablo, who have mainly sold into word processing and related markets. General Electric is also an important serial printer producer and has recently shifted to dot matrix with a new line of printers. GE also has one of the largest installed bases among the terminal printer users. Wang, which sells its daisy wheel with its own computer systems and other markets, is next among the serial printer manufacturers.

IBM and DataProducts lead in the line printer market with 50% of market share, spread unequally to IBM. The remainder of this market is held by Printronix, Teletype, Mannesmann-Tally, GE, CPI, Data Peripherals, and Okidata.

The page printer market, which is undergoing dramatic technical development and change, is dominated by IBM and Xerox. The two hold 83% of the market for installed systems. Honeywell has a majority share of the remainder, but is experiencing competition from several companies, notably Siemens. The entire market for high speed page printers is held by a similar group of IBM, Honeywell, Siemens, Xerox, Uppster, and General Electric.

Printer Trends

Frost and Sullivan predict that there will be no new technologies that will change the marketplace dramatically. They also predict that the existing market share will roughly be approximated in the near future, with non-impact printing techniques to remain in the minority of shipments and applications until 1987. IDC points out that an important trend for the manufacturers will be an increasing demand for printers from OEMs, particularly among the mainframe sellers. The IBM example of selecting the Epson printer for use with its personal computer is probably the best indicator of this shift.

IDC also notes important areas of change in the application share. The terminal printer market is a prominent loser, dropping from a 41% growth rate in 1980 to 21% or less by 1985 due to the increase in desktop computer sales. Desktops

and word processing, as pointed out earlier, are going to continue to make large increases yearly and this will be one of the growing arenas of competition from the producers of serial, dot matrix printers.

Despite the loss of market share from terminal printers to desktop printers, the dollar value of the latter will still be 33% of the total market, with general purpose computer printers maintaining 12%. Desktops, which will dominate in unit sales, will have only a 6% dollar share of the market.

Alternatives to printer output will begin to affect the printer market after 1985.

There appear to be some alternatives to printer output that will begin to affect the printer market after 1985. These include CRT based information retrieval systems (such as videotex), facsimile, and the growing group of intelligent copiers which will offer functions such as data communications, text storage, graphics, forms generation, font generation, typesetting, and optical character recognition. Copiers will increasingly offer functions such as those above, but questions remain as to which of the functions are the best solution in the diverse environments that are growing for their use.

Continuing demands for high reliability, speed, price/performance, and graphics will shape the use of new technologies such as laser printers, ink jets, and color thermal printers. Newer developments such as ion deposition and optical printing techniques remain highly speculative. Dot matrix systems, on the other hand, continue to improve in speed, quality, resolution, multiple copy capability, portability, and color. □

Ink Jet Modules Meet OEM Demands

by Stuart Cox and Maurice Wheatley

Designing an ink jet printing module specifically for system designers meant meeting resolution, speed, and flexibility demands of OEMs desiring a color hard copy device while maintaining a price competitive with other printer technologies. PrintaColor's Spectrum 2000 prints images composed of up to 1800 dots across a page at densities up to 150 dots per inch, by any number of dots down the page at 85 dots per inch. The color of each one of these printed dots is selected by the host system with a seven bit pixel color code for each dot.

Use of a state machine memory controller enables these printers to increase data throughput.

These color codes, specifying one of 125 possible colors for the corresponding dot, are transmitted to Spectrum one at a time over an eight bit parallel port. To maintain maximum print speed under worst case condition, Spectrum must be able to accept, buffer, and process this data at a maximum rate of 80 μsecs per pixel color code. In addition to handling the pixel data, the Spectrum processor must control the printer carriage motion and ink jet operation in an optimized fashion. Since all of this is too great a burden for standard 8-bit μPs, the Spectrum processor was designed as two modules: a customized memory controller which receives, buffers and pre-processes the pixel color codes, and a μP-based printer controller which controls remaining printer functions (**Figure 1**).

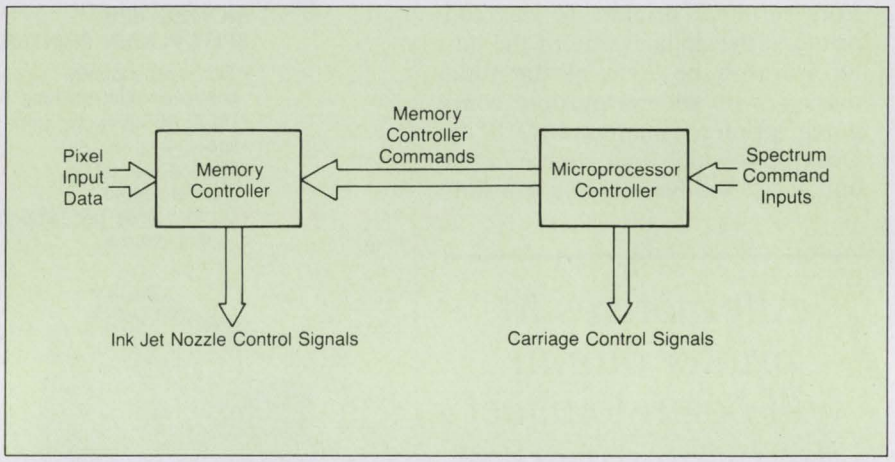

Figure 1: Designed as two modules, the Spectrum processor consists of a memory controller, which receives, buffers and pre-processes pixel color codes, and a printer controller, which controls the remaining printer functions.

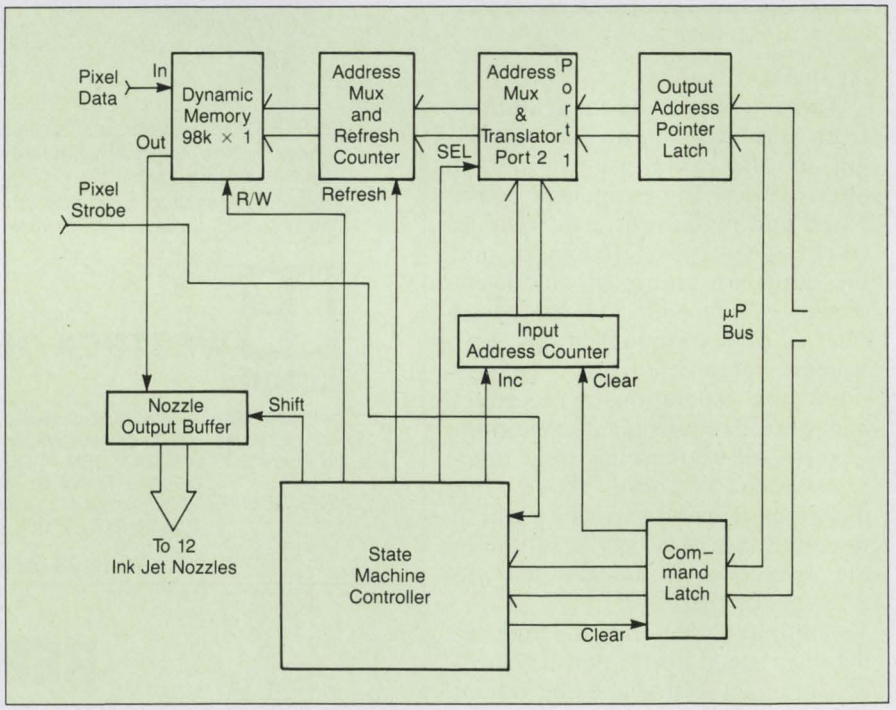

Figure 2: The memory controller consists of two 64K dynamic RAMs, an address multiplexer, an address translator, and the state machine controller.

The memory controller (**Figure 2**) consists of the following sections. Two 64K dynamic RAMs are used for buffering up to eight pixel

Stuart Cox is Software Engineer and Maurice Wheatley is hardware engineer for the Spectrum 2000 ink jet printer at PrintaColor Corp, PO Box 52, Norcross, GA 30071.

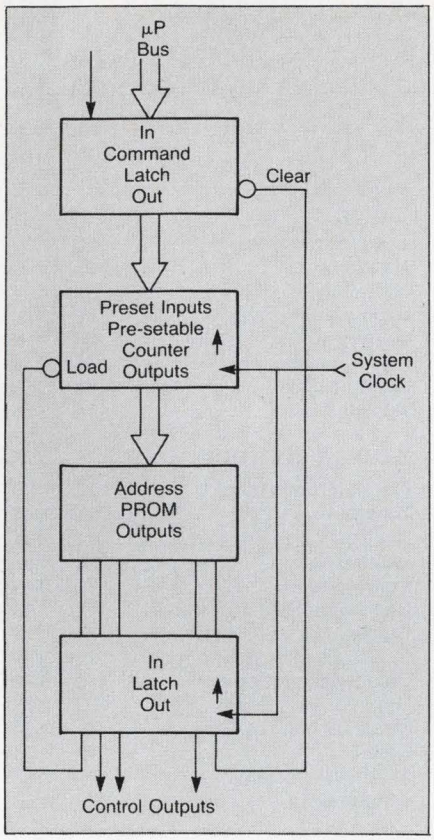

Figure 3: The state machine controlling buffer operation consists of a pre-setable binary counter, PROM, latches for de-glitching the PROM outputs, and a command latch tied to the μP bus.

lines of data. An address multiplexer and refresh chip along with a second multiplexer and address translator provide two address ports for the RAM chips. One of the address ports is connected to the printer controller μP bus through a latch. This is used for specifying which lines of data are to be sent to the ink jet output nozzles of the print head. The second address port is tied to the counter which is used to increment the input addresses as data is being input to the buffer. Data can be strobed into the buffer independent of μP control thus removing this time intensive task from the main system.

The state machine that controls the buffer operation consists of a pre-setable binary counter, PROM, latches for de-glitching the PROM outputs, and a command latch that is tied to the μP bus (**Figure 3**).

In operation, a command is latched from the μP bus and the counter begins counting starting at the location specified by the command code that gets loaded into the counter. As the counter increments, the PROM outputs sequence through whatever states are needed to perform that particular command. Upon completing a command sequence, the command latch is cleared and the counter is loaded with the new contents of the command latch (now zero). The zero location is the start of a no-op sequence which performs a refresh cycle on the dynamic RAMs. At the end of a refresh cycle, the counter is again loaded with the contents of the command latch. If it is still zero another refresh is performed. If another command has been written into the latch then the new command is executed. Thus the state machine is continually sequencing through a specified area in the PROM's address space and then loading in either a new command or a refresh cycle.

Some of the commands used by the Spectrum printer are: Input Pixel, Update Nozzle Buffer, Clear Buffer Line, and Find First & Last Dot. This last command searches through a line of data and finds where the first and last pixel is located so that full logic seeking functions can be performed.

While the pixel data is being manipulated by the memory controller, the μP is free to control movement of the ink carriage, movement of the paper, and firing of the ink jets. The μP therefore has time to perform such functions as full carriage logic seek, printer error state analysis, and implementation of parameter setting commands sent to Spectrum from the host system. Thus the modular architecture of the Spectrum 2000 processor allows full speed pixel data transfer without sacrificing print speed optimization, pixel resolution, or flexibility, and without the use of an expensive high performance μP system. □

Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

Assessing The Latest In Logic Analyzers

by Ed Pevovar

Logic analyzers may be used to debug μP programs and collect valuable data relating to a μP's operational parameters. Various considerations, such as the number of channels, triggering, data display, and data manipulation are important when considering which analyzer to purchase.

Logic analyzers are digital instruments, specifically developed for μP applications that are capable of representing digital signals in two domains: timing and data. Timing analysis requires asynchronous sampling of the circuits signals, usually faster than the clock signal within the circuit. Data acquisition is done in synchronism with a digital circuits clock signal.

As the complexity of logic analyzers has increased, so too has the difficulty in logically selecting a particular model.

Most logic analyzers currently available can perform both types of measurement.

There should be sufficient input capability to acquire data from all address, data, and control channels, simultaneously. 8-bit processors need 32 inputs; 16 for address, 8 for data, and 8 for control; 16-bit processors need at least 44 channels; 20 for address, 16 for data, and 8 for control.

Many manufacturers supply specific probes for each different pro-

Figure 1: Dolch has placed a huge demand on their logic analyzer's operational parameters. They have recognized ICE (In-Circuit-Emulation) as an extremely powerful analytical methodology to follow in software testing. By creating an interaction in ICE, they have gained control of program execution, thus allowing the read-out of initial CPU register values, which cannot be seen directly through the monitoring bus. Equally as important, word-generation is possible.

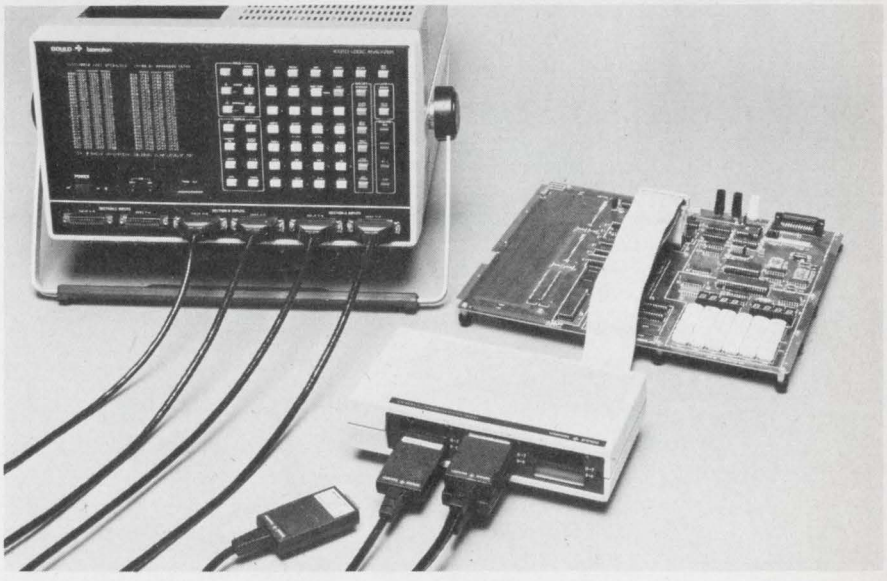

Figure 2: The Gould Biomation K101–D is fairly simple to set-up and use. It has such features such as 12 external clocks, as an aid in performing complex timing and data capture, and a wide variety of data display formats; self-diagnostics which are keyboard controlled can even test the instrument's own calibration.

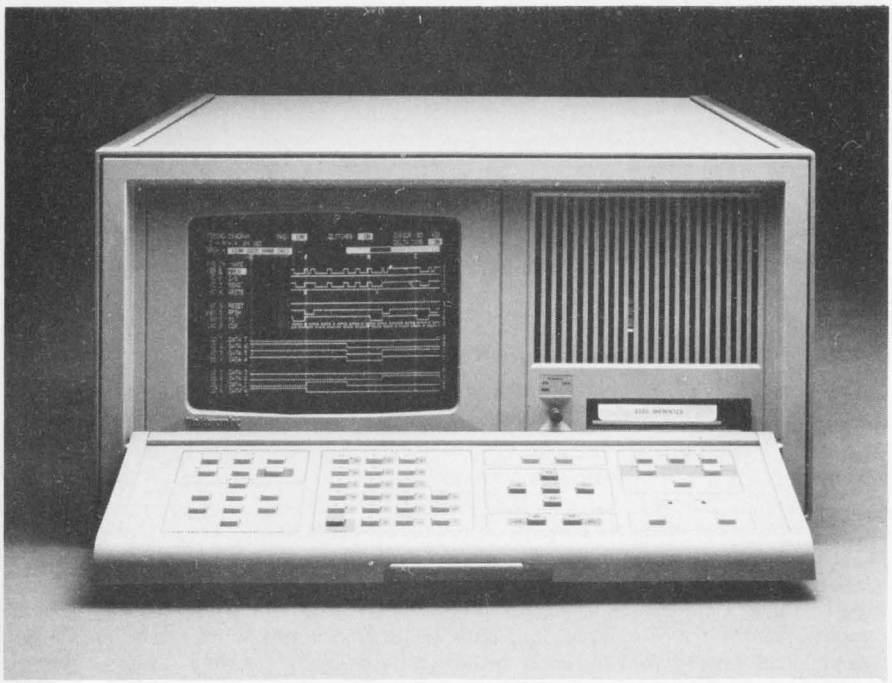

Figure 3: The user may configure various combinations of data acquisition modules with the monochrome 9100 and 9120 logic analyzers/pattern generators from Tektronix. Four modules cover a wide range of data widths and sampling speeds in both synchronous and asynchronous modes. Each module can be installed in one of the vacant cards slots in the machine.

Figure 4: The LA–1020/1025 logic analyzers from B & K Precision are not self contained units, in that an oscilloscope must be connected to gain a CRT display of the analyzed data.

cessor, so that a user may quickly connect to the machine, and disassemble acquired data into the processor's mnemonics.

One of the software dependent design criteria not yet supported by any logic analyzer is the tracing of multiple processor executions having independent clocks, and the time-correlation of their execution.

Logic analyzers have 1 pair of digital memories, called Registers, for each vertical input channel; on a 48-channel logic analyzer, for example, there are 48-Register pairs that serve as memory. When the analyzer receives a *Trigger* command, the contents of one memory of the pair becomes "Set," or reserved for display. The logic analyzer may be set to display its data *prior-to* or *after* the trigger.

Digital Word Recognition

A word or length of parallel bits can be recognized by the input channel present combinations of "L," "H," or "DON'T CARE," usually designated as "X." When these conditions are satisfied at the inputs the trigger pulse is then generated and a display can be obtained.

If the analyzer can view the latest bits at one channel and makes a comparison of this pattern with a preset word at another channel, this operation is called serial word recognition. Only when an equality exists, is there a trigger pulse generated, and the serial word you've preset can be measured and stored, prior to the recognition search.

Terminology

Active Clock Edge — The transition during which all receivers interpret data on the bus; the analyzer uses this clock.

Aliasing — Sampled waveform is displayed in this manner, when the sample rate‹data rate. (‹refers to t..).

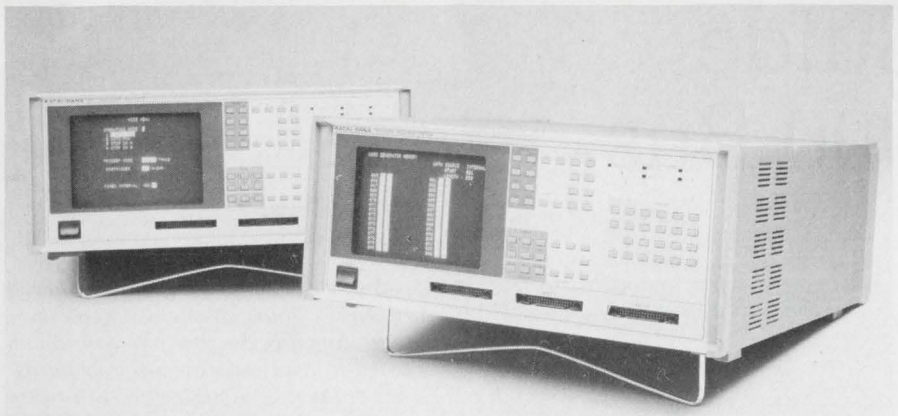

Figure 5: Racal Dana offers three models in its 200 series; the 201, 202, and 205. Many features are offered such as nonvolatile memory (up to 12K bytes on the 205), GPIB interface, and up to 48 channels for acquisition.

Arm — This is an input condition that must be met before the analyzer trigger condition is recognized. (Trigger Enable.)

Asynchronous Analyzer — Asynchronous data tracing — Timing analysis.

Bus System — A network of paths facilitating data flow in digital systems, i.e., the address, data, and control busses.

Clock — A pulse generator administering timing parameters to control the operation of a digital system (There may be more than one in a system.).

External Trigger — Any active signal used to "start" the analyzer.

Full-Duplex — This is a serial system in which there are separate transmit and receive channels, as opposed to having only one channel for both, as does a **Half-Duplex** operation.

Glitch Memory — An auxiliary memory, in which the presence of any extraneous signal between sample-periods, is stored.

Handshake — A system of events which occur to signal "Data Available," "Data Being Read," or "Data Has Been Read."

Hold Time — This is when the analyzer is capable of sampling data after the active clock edge. The logic analyzer should have a Zero hold-time.

Indexing — Setting the number of samples/clock pulses to be "skipped" after the trigger word, prior to obtaining a trace.

Nyquist theorem — 2 samples/cycle min. are needed to characterize a band-limited signal. (You'll find, in practice, that 5-10 are actually required.)

Parity — An extra bit in a data word which makes the entire word contain an even/odd number of bits of one polarity.

Pre-trigger — The number of words to be displayed prior to the trigger word.

Probe — A Pod on an analyzer, (the loading/speed of the probe is a major consideration), which connects the circuit under test to the instrument.

Protocol — The format of events/signals which must occur to properly operate the system.

Skew — The difference in the delays across channels between the probe tip and the point when the data is interpreted by the analyzer.

Threshold — A signal level that divides one state from another.

Trace Triggers — Only trigger words are traced.

Trigger — Defines that point where a logic analyzer references its trace to system activity. □

Designers' Guide To The TM990 Bus

by Paul Snigier, Contributing Technical Editor

The TM990 bus from Texas Instruments has the entire TM990 microcomputer system organized around it, and as such is one of the major buses. In addition, with TI preparing to put a renewed effort behind its micro lines, this bus promises to become even more significant for OEM system designers. Unlike most buses, TM990 is closely tied to its creator's other products. It is possible to discuss the Multibus without really delving into the Intel micros, and it is possible to discuss the S–100 without discussing the defunct MITS Altair. But any discussion of the TM990 bus that ignores the TMS9900 is incomplete.

TM990 Bus

The TMS9900 μC and its family use the TM990 bus, which handles multiprocessing, high-speed DMA, and prioritized asynchronous interrupt structure that permits various-speed peripheral devices to be on the same bus. Also, CRU I/O, the communications register unit, is used by the 16-bit TMS 9900.

The TM990 bus has 16 bidirectional data lines, two CRU data lines, 16 address lines that are expandable to 20, 15 prioritized asynchronous interrupt request lines, power supply lines, five bus control arbitration lines, and several other control lines. The TTL-level bus supports Multibus master devices, and provides signal lines that arbitrate bus control by the master devices. Like certain other buses described earlier in this series, card position determines module priority. Instead of being bused on the motherboard, some bus arbitration control lines are daisychained.

TM990 signal levels are TTL, with certain signal lines driven by tristate devices. Other signal lines

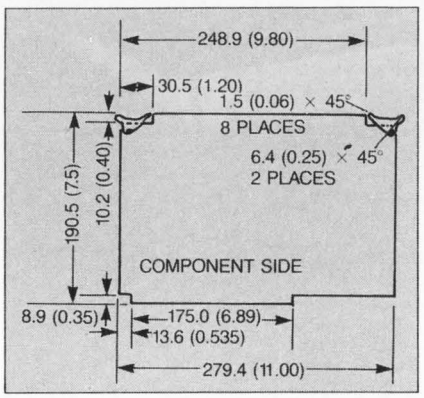

Figure 1: The TM990 bus cards are well defined. A four- or eight-slot motherboard contains the 100-pin connectors needed to mate with the separate cards. The card is rugged and suited to control environments. The board is 0.062" (1.6mm) thick, with a 0.125" (3.175mm) spacing for the 100-pin motherboard connector. Board spacing is 0.75" (19.1mm) and component height is 0.55" (14.0mm). For obvious reasons, locate drivers and receivers close to their interface connections, if you are doing the design.

are open-collector-driven, so wire-ORing of signals is needed. Open-collector gates must be used with external output pull-up (collector) resistors. This allows connecting several open-collector outputs together in combination with a single pull-up resistor, thus performing a logic operation of wire-ORing

TI's TM990 bus, particularly well-suited to industrial and process control, will expand considerably between now and 1985.

(This is the widely-used nomenclature of the dot-OR schematic.) Thus, the collector-dotted array output becomes a logical ONE if and only if the outputs of all collector-dotted gates are logic ONEs; and, conversely, the output becomes a logical ZERO when one or more outputs become a logical ZERO. Some TM990 signals require termination and others do not. The bus uses both positive and negative logic, but the negative logic use is kept to a minimum, as with wire-ORing signals. There are three categories of bus operations, all of which (with the obvious exception of interrupts) are synchronous with respect to clock bus signals on the bus. These three categories are memory and memory-mapped I/O, communications register unit and direct memory access.

Interfacing to the TM990 is by memory-mapped I/O interfacing (a parallel method) and control register unit I/O interfacing (a high-speed serial technique). Of the two, memory-mapped I/O interfacing is the easier, as it is more direct. With this technique, external peripherals and devices interface through logic circuits and appear to the TM990 as R/W memory locations. Memory addressing methods identify each memory-mapped I/O port so that the complete memory bus address bus must be decoded to identify a single port. The address lines AO–A14 are decoded variously by means of gates, decoders and digital comparators. This generates a memory address. This is gated with the TM990 control signals, write enable or $\overline{WE}$ and the

data bus input (DBIN) to generate the appropriate device select signals. As may be expected, the I/O ports are accessed by memory R/W instructions. The memory mapped I/O interfacing technique, though it is very straightforward and easy to use, does suffer from a disadvantage: the 16-bit data bus must be connected to each I/O port. If RAM memory is not adequate, the memory-mapped I/O devices occupy too much address space. With the higher capacity chips coming into common usage, this has become less of a problem.

In respect to memory cycle timing, and with the exception of write enable (pin 78), all memory control signals are synchronized to the trailing edge of the bus clock (pin 22, Φ1). Memory enable (pin 80), memory cycle (pin 84) and ready (pin 90) define memory cycle states. As for handling slow memory, there exist no incompatibility problems. The addressed device supplies the ready signal; and by not implementing Ready True, this stretches memory cycles by the addressed device or slave. But, if a slow processor is integrated into the system implementation, Memory cycle stretches memory cycles, thus permitting a slow processor to handle fast memory.

The communications register unit (CRU) is unusual for a μP and, in fact, does not exist for most others (The microNova is an exception). Not only can the micro address I/O devices as memory locations, but it also addresses a separate I/O field, up to 4K bits and transfers information to and from the TM990 in serial, bit-by-bit format. The CRU I/O technique addresses individual bits—not bytes or words.

You can specify any base address desired and even transfer the middle eight bits from an input port by simply setting the address higher than the base address. Since CRU instructions begin loading and storing in the LSB, the middle eight are transferred eight LSBs in the destination location or register. That you have altered CRU base address to initiate transfer in the middle of an I/O port is immaterial to the CPU; and, in fact, it has no way of distinguishing this.

Let us look at the other CRU control instructions. When the individual bits must control and sense different conditions, these instructions can handle setting, clearing and testing individual bits. The three instructions—SBO, SBZ and TB—all use the register 12 base address to locate individual bits. In order that individual bits can be easily located, and avoiding the necessity of modifying the address stored in register 12, each operation instruction contains an offset. This offset ranges inclusively between −128 and +127. Thus a large range of bit locations can be addressed in all CRU ports. Finally, the instructions just mentioned are defined as: SBO is a set bit to logic ONE, SBZ is a set bit to logic ZERO, and TB is a test bit control instruction.

Bit testing operates with a displacement much like the SBO instruction: it transfers its state into the status register bit 2, EQ or Equal (set when the two bytes compared are equal) on the flag register. Thus, conditional jump instructions can test it. Bit testing does not alter an adressed bit. Nor does it test the bit—it only inputs the bit's state and it is tested later.

At this point if you are familiar with the 8086 and other micros, the CRU I/O interfacing might seem odd. But, it is both a powerful and flexible concept. It is only one of the many techniques that make the 9900 and its bus so powerful—so much so that it survived quite well, despite its being the first real 16-bit micro (other than the PACE) on the scene.

The instruction set, though not as extensive as some, has the advantage of fewer complex instructions to befuddle designers. If you are considering the TM9900 and its TM990 bus, you will find that you can write programs to do just about anything every other 16-bit micro can do—and some a lot better. Unfortunately, the big obstacle has been supporting hardware and alternate sourcing.

Let us now look at some CRU specifics. The memory enable or MEMEN (pin 8) permits CRU operations only when the signal is inactive, at which I/O operations simultaneously occur after an address is put on the A3–A14 lines.

The operation DMA is well known. In the TMS9900, it provides even higher data throughput when data blocks are being transferred. This operation involves memory and bus control exchange operations, all under DMA control. In direct memory access the DMA device acquires bus control, conducts memory operations under its control and then releases bus control. If multiple, sequential DMA acquisition cycles occur, the acquisition and release modes are kept separate from one another. To gain bus control, the DMA device uses six signals. The hold (pin 92) and hold acknowledge or HOLDA (pin 86) signals take control from the processor, while the other four signals establish multiple DMA device arbitration. As for those remaining, they provide the device select signal to the I/O port.

Register 12 stores a CRU base address. With a group of 16 I/O bit addresses, this base address is the lowest bit address. A3–A14, the only address lines employed in the CRU I/Oing, permits addressing up to 2^{12} or 4K bits, thus permitting up to 256 16-bit I/O ports. The register 12 base address is so placed that the address bits correspond to D3–D14, with the other bits being 0.

As a rule, bits are addressed in groups or blocks of 16 bits, thus keeping things easy to track. CRU control instructions permit selecting groups of or individual bits in each 16-bit block of data.

Multiplexers and addressable latches serve as parallel-to-serial and serial-to-parallel converters, respectively, permitting the fairly simple serial transfer of data. Since no memory addresses are needed in I/O device addressing, and relatively few signal connections are needed, this is an advantage of this technique. Addresses do control CRU I/O devices, but they do not use memory control signals, nor are they active simultaneously with the memory.

The CRU control instructions

are important to an understanding of the TM990 bus. Probably the most direct instructions, and definitely the easiest to understand, are the load CRU (LDCR) and store CRU (STCR). LDCR specifies the information source and uses any addressing mode. It specifies, starting with the LSB, how many bits will be loaded. Stored in a general-purpose register, the address can be altered as needed (This could be for various reasons, including the need to suit changing I/O base addresses). This gives you some flexibility for portions to be I/O'd. This is a more flexible interfacing method, but a bit more complex. To control information flow to/from the CRU-controlled I/O devices, there exist special CRU instructions, unlike other micros and buses. In addition, a number of special-purpose interface chips to aid in CRU interfacing are available from TI or second sources.

If you are working with a TI configured TMS9900 system, the CRU functions similar to an I/O port. Conversely, if you are an OEM designing a TMS9900 interface, the instruction accessing the CRU then makes alternative use of a part of the address bus, in addition to the CRU data output (pin 30), CRU data input (pin 29) and CRU clock (pin 87).

Rather than addressing bytes or words for I/O transfers, as we mentioned, it is necessary to address individual bits: the CRU I/O ports must be set up so individual I/O bits can be accessed. This is not difficult, since such bit-addressable input ports are designed from 8-line-to-1-line and 16-line-to-1-line multiplexers. Output port functions are provided by addressable latches. Devices such as the 74150/74151 and 74LS251 are input-port multiplexers, while a typical addressable latch is the 74LS259. High-current sinking/sourcing addressable latches are the NE590/NE591. There are others, some more complex, but these are just some of the examples. Thus, in a typical I/O port configuration, input data is fed to pin 29 (CRUIN), with CRUOUT outputting data, and the CRU clock output CRUCLK, controlling the CRUOUT line signal synchronization. As for the CRUIN synchronization, it is not needed. The address bus, as usual, addresses the individual bits, with A11-A14 being the four LSBs directly addressing the bits.

TMS9900 Basics In A Nutshell

The TSM9900, a minicomputer-derivative, is a powerful 64-pin package processor that communicates with the outside world through a 16-pin address bus and 16-pin data bus. This powerful one-chip minicomputer CPU-equivalent is well-supported and used internally for the 990 minicomputer/microcomputer, so that any 990 OEM designer is actually integrating a minicomputer-type processor having the 990's instruction set.

Unlike the earlier 40-pin or 42-pin package limitations, the TMS9900 used more pins (64), which somewhat hindered its initial acceptance. However, this avoided problems inherent in multiplexing on the bus, since a 40-pin, 16-bit micro cannot I/O with the outside world by two 16-bit buses. Those 16-bit micros that use bus multiplexing will not have much of a speed advantage over a competing 8-bit micro. The 8088 (with its 16-bit internal architecture) and 8086 were introduced in standard 40-pin packages. By contrast, the MC68000 uses 64 pins for separate address and data buses, and internally resembles a 32-bit processor, but provides higher speed than the older 8086 and Z8000 partly due to its separate address and data buses.

To understand the TM990 bus, you must first understand the 16-bit TMS 9900 μC family.

TMS9900 Pros and Cons

The TMS9900 employs memory-to-memory architecture in which the focal point for the instructions is the memory instead of a set of on-chip registers. One instruction can fetch two operands from memory and perform an arithmetic or logic operation and then store the result in memory. All this is possible because instruction execution steps (clock cycles) vary with each instruction under on-chip microinstruction ROM control. This was a radical departure from other conventional accumulator-based architectures. In addition to this bold architectural change, the micro used eight addressing modes, five of which refer to a set of 16 memory words defined as "registers" in a workspace. Multiple workspaces may be defined or located to enhance program flexibility by altering the contents of a single on-chip register (the workspace pointer).

Other TMS9900 characteristics that made it powerful were hardware multiply and divide instructions and the bit-addressable I/O. As for I/O, the micro employs three different types: *memory-mapped I/O* with memory addresses serving as I/O locations for I/O information to be sent over the data bus; *direct memory access* (DMA) so an external controller suspends processing when data is transferred between memory and peripheral (thus speeding up overall system throughput); and *bit-addressable I/O* over a two-wire interface which works with the address bus. It addresses up to 4096 single-bit devices for inputs, with another equal number for outputs when data is to be transferred one bit at a time in or out.

Multiple bit transfers can be made also over the same interface since instructions are available for transferring any number of bits, from one to 16, to or from a peripheral device. It is this I/O characteristic that makes this micro rather useful in process control, particularly when you consider that in such applications many single-bit and multi-bit devices are commonly used.

This choice was not surprising, considering that industrial and process control was then and is now

one of TI's big markets and that this particular bus and microcomputer family fit into TI's overall product line, which ranges form 5AG-type motor controllers, temperature controllers and OCI interface subsystems all the way up to large systems for use by both the OEM integrating them into specific systems, and TI themselves in existing or upcoming systems.

That TI failed to properly market the bus and micro accounted for its slow ramp-up. This is changing. With the shutdown of its discrete devices operations, TI cut profitable lines (which caused it to momentarily fall behind Motorola, which took the world lead) at the wrong time. TI should bounce back from this self-imposed slide shortly. What this means for the TM990 bus and its associated TI family is a greater-than-ever push for larger market share. The resources freed up from the shutdown of the other operations, combined with TI's marketing department seemingly developing a new awareness, guarantees that you will be seeing more of the TM990 bus and its related product families.

Aside from the lack of original marketing push by its creator, why didn't the TM990 bus and TMS9900 become as popular as some of the others? Upon its introduction, many hailed the device as one of great promise. On its better side, the 9900 transfers from one to 16 bits at a time, while those like the 8080A and later upgrades only did so in 8-bit increments. The 9900 required less instructions to transfer data into memory than those using their accumulator I/O method.

Certainly, there was truth to the pundits' claims that the initial superiority that gave it such promise was at the same time its greatest nemesis, since other micros were easier to comprehend, and therefore easier to design with. The cost of graining and retraining hardware and software designers was costly and time-consuming, to say the least, which worked against the TMS9900 and TM990—especially considering the lack of resources originally targeted for training and educating designers, relative to Intel and Motorola. Thus, designers familiar with other popular micros, given a choice, also trended to specifying or recommending micros which they already knew well. Since programming had assumed a greater ratio of overall design project time and budgeting, what resulted was a tendency for software to dictate hardware choices. This made for a growing number of questionable engineering decisions by OEMs, who failed to base their decisions upon sound selections of component availability, functional suitability, true costs and the like. The TI bus and associated micros and related device families—though better-suited for many OEM applications (particularly in industrial and process control)—were too frequently ignored for this reason. The lack of kits and boards available four years ago from TI

Signal Category	(Circuit Side)			(Component Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
Power	1	GND	Signal Ground	2	GND	Signal Ground
	3	+5 V	+5 VDC	4	+5 V	+5 VDC
Interrupts	5	INT8/	Interrupt Request 8	6	INT 7/	Interrupt Request 7
	7	INT 10/	Interrupt Request 10	8	INT 9/	Interrupt Request 9
	9	INT 12/	Interrupt Request 12	10	INT 11/	Interrupt Request 11
	11	INT 14/	Interrupt Request 14	12	INT 13/	Interrupt Request 13
	13	INT 2/	Interrupt Request 2	14	INT 15/	Interrupt Request 15
	15	INT 3/	Interrupt Request 3	16	INT 1/	Interrupt Request 1
	17	INT 5/	Interrupt Request 5	18	INT 4/	Interrupt Request 4
	19	IAQ*/	Instruction Acquisition	20	INT 6/	Interrupt Request 6
Clocks	21	GND	Signal Ground	22	BUSCLK/	Bus Clock (Φ1)
	23	GND		24	REFCLK/	Reference Clock (Φ3)
	25	GND		26	CLK/	Internal Clock
	27	GND		28	EXTCLK/	External Clock
Data	29	CRUIN	CRU Data Input	30	CRUOUT	CRU Data Output
	31	GND	Signal Ground	32	BUSY/*	Bus Busy
	33	D0	Parallel Data Bus	34	D1	Parallel Data Bus
	35	D2		36	D3	
	37	D4		38	D5	
	39	D6		40	D7	
	41	D8		42	D9	
	43	D10		44	D11	
	45	D12		46	D13	
	47	D14		48	D15	
Optional Power	49	−15 V	−15 VDC	50	−15 V	−15 VDC
	51	+15 V	+15 VDC	52	+15 V	+15 VDC
Address	53	XA0	Extended Address Bus	54	XA1	Extended Address Bus
	55	XA2		56	XA3	
	57	A0	Address Bus	58	A1	Address Bus
	59	A2		60	A3	
	61	A4		62	A5	
	63	A6		64	A7	
	65	A8		66	A9	
	67	A10		68	A11	
	69	A12		70	A13	
	71	A14		72	A15	
Power	73	−12 V	−12 VDC	74	−12 V	−12 VDC
	75	+12 V	+12 VDC	76	+12 V	+12 VDC
Control	77	GND	Signal Ground	78	WE	Write Enable
	79	GND		80	MEMEN/	Memory Enable
	81	GND		82	DBIN	Data Bus In
	83	GND		84	MEMCYC/	Memory Cycle
	85	GND		86	HOLDA	Hold Acknowledge
	87	CRUCLK/	CRU Clock	88	IORST/	I/O Reset
	89	GND	Signal Ground	90	READY	Ready
	91	GND		92	HOLD/	Hold
	93	RESTART/	Restart	94	PRES/	Power-On Reset
	95	GRANTOUT/	Grant Output	96	GRANTIN	Grant Input
Power	97	+5 V	+5 VDC	98	+5 V	+5 VDC
	99	GND	Signal Ground	100	GND	Signal Ground

Figure 2: The 100-pin TM990 bus connector pin assignments are as shown. Note the functional grouping, as well as how individual signal pins are arranged to minimize crosstalk (as much as is feasible) and noise problems.

didn't make the OEM's job any easier.

Problems have been reported with the TMS9900–based SBCs, among them *ground lifting,* which can occur with wider buses such as the TMS9900. While working well alone, when interfaced with peripheral and memory cards, bus interactions kept crashing the SBC. At first glance, it would seem that bus timing errors would be the likely culprit, but such was not the case in many of these OEM cases. When the SBC card was interfaced to several peripheral and memory cards down the backplane of a shelf assembly in certain arrangements and proximities, it was discovered that the switching bus lines raised the backplane ground when the READY signal should be stable. Hence, the term "ground lifting," which caused the CPU in each instance to interpret this as a change in state. The solution, as you can guess, was to space signal lines more, use multilayer PC boards (often too costly and non-correctable) and more attention paid to the ground plane layout. Proper termination of the line (which can be the topic for a four-part series in itself!) is also sometimes helpful in these cases.

The lack of initial support—a legacy that is still hard to overcome—is not the only negative factor. There are others, such as its great flexibility being offset by the necessity for add-on devices that increase components count and layout complexity, and ensuing lowered reliability from this resultant greater interconnnection complexity. This also led to higher assembly and testing costs. This drove many OEMs to selecting less-optimized but expandable single-chip micros. Of course, on the other hand, by properly-selecting auxiliary devices, the 9900 can be configured to many applications. It is interfaceable to customized TTL devices and subsystems and provides true software compatibility—a feature that TI has pursued zealously. It has all-external memory, which provides a flexible memory size. These and many other advantages make the TI bus and micro approach quite flexible and suited to fitting a broad spectrum of systems-building possibilities.

As we mentioned earlier, multi-bit transfers over the same interface are possible, making this micro suited to process and industrial control. In addition, various units or devices can be handled even though they require various bit groups (2, 4, 6, 8 or 10 bits), since the CPU is well-suited to handling this type of data transfer. Unlike the 8-bit micros that the 9900 was competing with in the industrial control field, and which it still does, the large data throughput and increased DP power suit it more to these applications than do others. As for architectural similarities with other lesser micros, such as the 6800 types, it also employs memory-to-memory configuration to achieve multiple register files. However, the 9900 designates the first 32 bytes of memory as workspace registers to replace what typically would have been hardware registers.

The hardware 16-bit multiply and divide and direct, command-driven I/O stood out over the crowd a couple of years ago. In terms of its I/O operational characteristics, the 9900 resembles the Intel micros more than Motorola's. For I/Oing, the 9900 possesses 12 address lines and directly addresses a maximum of 4K different peripherals. I/O bits can be addressed separately or in fields of one to 16 bits. This is convenient when it's necessary to sample the state of an indicator (a switch, for instance) that is represented as one bit in an I/O word.

Now that the second-generation 16-bit micros are becoming available, the early designs like the 9900—though they do have improved performance over the 8-bit micros—cannot emulate mini performance in multiprocessing. However, this bus and its allied product family already has a strong market share, particularly in industrial and process control areas, and this influence is predicted by industry observers to indicate that "the sleeping giant" of TI has finally awakened. Expect this bus and allied product lines to establish greater dominance between now and 1985. □

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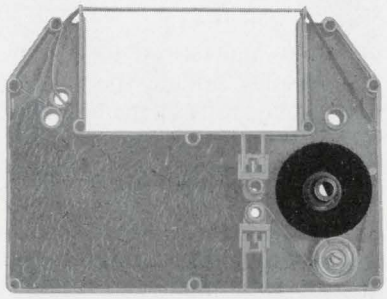

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Custom Processor Eases Display Design

Designing high resolution in color displays, while still maintaining high display update speed and low cost, is a difficult problem for system designers. The reasons are the memory numbers associated with the display. How do those numbers affect the limits to display controller performance?

Figure 1 shows the architecture for a high-performance raster grahics display controller. The heart of this controller is the display refresh memory; this memory must be continually accessed at high speed to provide the data necessary to refresh the CRT fast enough to prevent flicker. The display refresh controller performs the memory addressing operations necessary to refresh the display, and controls such display-related functions as Pan and Zoom.

The high data rates required to achieve this display refresh operation are typically obtained by reading a number of display refresh memory chips in parallel into a video shift register. The data in the shift register can then be shifted at the video rate to provide data at a much higher speed than could be obtained if individual RAM chips were accessed.

The other major function required of the raster graphics display controller is to write new data into the display refresh memory. This data is typically organized into graphic entities such as vectors, arcs, characters, and polygons. Because of the large number of pixels to be written and the rather specialized nature of the computations involved, a dedicated graphics processor is usually provided in the display controller. As we shall see, the display refresh function and the writing of new data into the display refresh memory compete for available memory cycles. This competition can seriously impede overall performance.

The graphics processor must perform its calculations and write pixels at high speed to obtain a high display update speed. Also, the display refresh memory must be continually accessed by the display refresh controller to provide the steady stream of data required to generate video to drive the raster display. The display refresh memory has a finite access and cycle time, limiting its availability to the graphics processor and the display refresh controller. Thus, available memory cycles must be carefully shared between the display refresh and memory update functions.

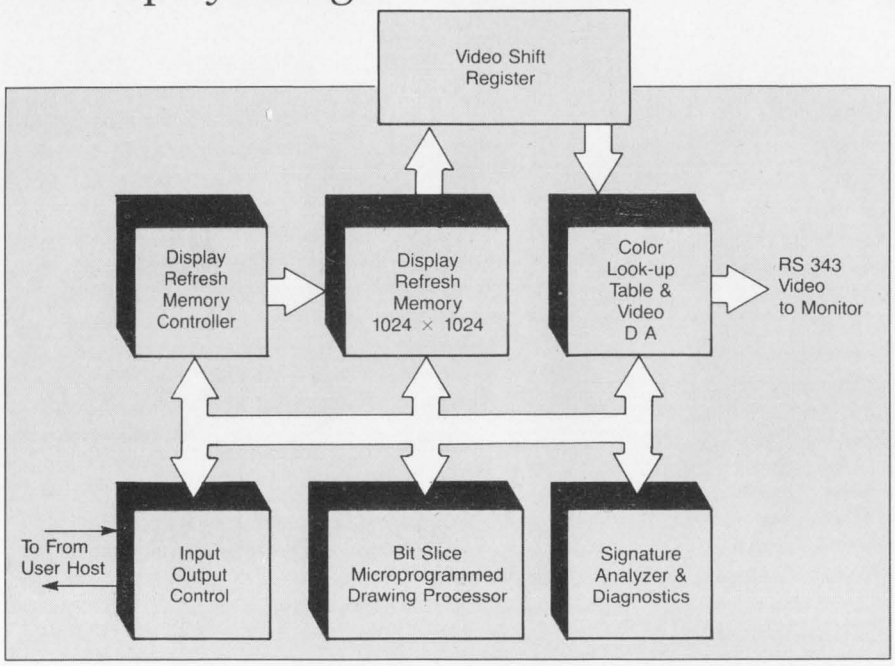

Figure 1: Architecture for a typical high-performance raster graphics display controller.

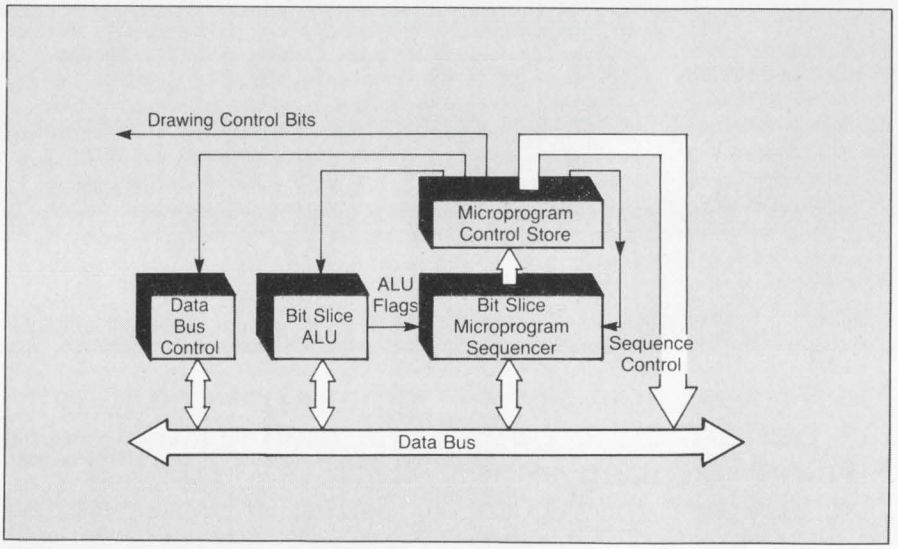

Figure 2: This high speed custom bipolar bit-slice processor uses a 64 bit wide microcode word.

Refresh Requirements

Let's look at these requirements in more detail. For a 1024 × 768 pixel display, refreshed at 33 Hz, pixels must be read from the dis-

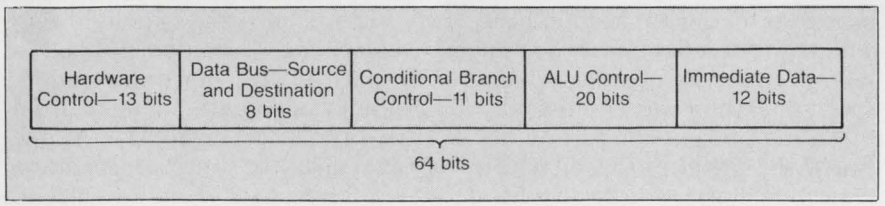

Figure 3: This microinstruction format allows hardware control lines to be manipulated as a part of the microinstruction, without additional attention from the processor.

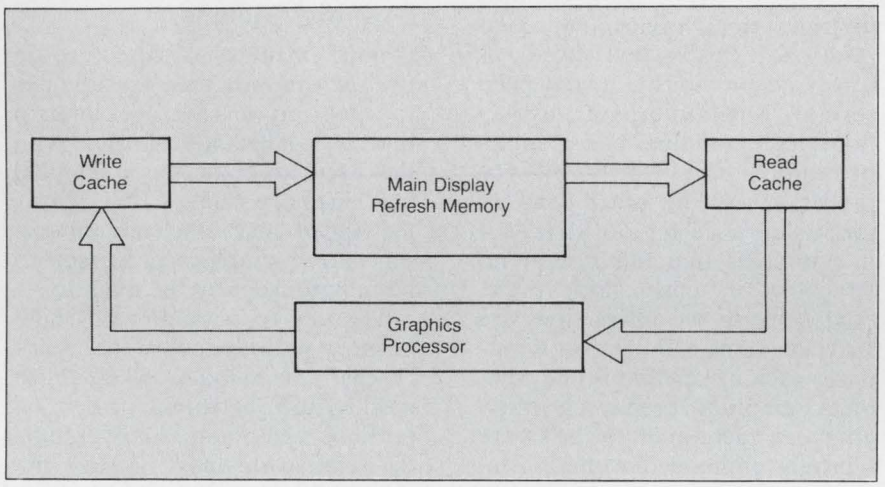

Figure 4: This memory architecture employs two caches, one for read and one for write.

play refresh memory at a rate of 36 MHz, or once every 27 ns. If we choose the display refresh memory size to be 1024 × 1024 pixels, we will need 16 64K memory chips per memory plane, or 64 16K RAM chips. In the interest of low cost, minimizing circuit board area, and increasing reliability, it would be desirable to use the 64K chips. If we read out the 16 chips in parallel into a high-speed video shift register, we can satisfy the 27 ns per pixel requirement by cycling the RAMs every 440 ns. This is comfortably within the capabilities of available 64K RAMs.

But what about the graphics processor, which needs to access memory to redraw the display or add interactive updates? Since display refresh keeps the memory fully occupied during active display intervals, the graphics processor must wait for the display's retrace blanking intervals in order to gain access to the memory. Since retrace blanking typically represents less than 25% of the total display time, the display update rate by the graphics processor can be significantly limited by this restricted memory access.

To allow the graphics processor greater access to the display refresh memory, one could construct the memory from 16K RAMs in place of the 64K parts. In this case, the 64 RAMs required to form one plane of memory could all be read out in parallel for each display refresh cycle. At 27 ns per pixel figure, a memory cycle every 1760 ns would provide the necessary refresh data. This would allow several graphics processor accesses to be interleaved with the display refresh memory accesses. This approach, however, increases system cost and complexity, while reducing reliability.

Double buffering is another approach that increases graphics processor access to the display memory. It requires two complete memory systems, one assigned to display refresh functions while the graphics processor has exclusive access to the other for generating an updated display. The two memories are periodically interchanged, allowing newly created graphics to be displayed, and making the previously-displayed memory available to the graphics processor for creating the next update. This approach allows the graphics processor full memory access for high update speeds, but is costly in that two complete memories are required. The double buffer approach also presents problems in some interactive applications, since the graphics processor must regenerate the entire display image even when only minor changes or additions are required.

In designing our display controller (the Metheus Ω400), we chose a memory design incorporating 64K RAMs without double buffering to minimize both cost and complexity. To achieve fast display updates in spite of memory access limitations, we relied on two techniques. First we designed an optimized graphics processor to fully utilize the available memory cycles. Second, we developed a memory architecture that effectively doubles the speed at which our memory can be accessed for display updates.

Specialized Processor

To keep the processor from becoming a limitation on memory access speed, there are two possible processor choices. One solution uses a fast single-chip μP as the internal processor; the other requires a specialized bit-slice processor.

The advantages of the μP include design simplicity and a predefined instruction set which, once learned, can provide a quick design solution. There is also a savings in circuit board space requirements.

Within those same features, however, there are inherent drawbacks. Even the fastest of processors have speed limitations in their cycle time alone. The design may be completed more quickly,

but the end product will not run as fast as desired. Even those processors that can be clocked at high rates have a slower total running speed, since as many as four clock cycles may be required to complete a single instruction.

Within those instructions there is another brake applied to operating speed. μPs, by their nature, have a general-purpose instruction set. When applying these instructions to real-world design, the result is often three or more instructions to accomplish one system operation. Thus, even a design based on the fastest MOS μPs would run slower than desired due to multiple clock cycles per instruction, and less-efficient code.

For our design, we wanted to run at least twice as fast as available μPs would allow. So, a custom bipolar bit-slice processor was developed, one using a 64 bit wide microcode word (**Figure 2**). Because of the specialized processor design, a specialized instruction set was inherent. With the processor designed hand-in-hand with the instruction microcode for fast graphics processing, high-speed operation was ensured.

We can make a comparison between the Ω400 processor and a typical high-speed μP—the Motorola MC68000. The MC68000 is one of the faster μPs available. Although it can be clocked at rates up to 12 MHz, it requires multiple clock cycles to accomplish each instruction. And, as discussed previously, it may take several general-purpose instructions to accomplish one graphics operation. The Ω400's bit-slice processor, on the other hand, is clocked at a slower 4.5 MHz, but it completes one full system instruction on each clock cycle. And because the instructions are specialized instead of general purpose, each instruction is one complete graphics processing operation. In fact, multiple tasks are typically embedded within a single instruction.

For instance, specially-designated control bits within each instruction allow certain hardware control lines to be manipulated as a part of the microinstruction, without additional attention from the processor (**Figure 3**). At the same time, the processor might be performing one or more calculations on system variables, storing the results of both calculations for future use.

Graphics Memory

Unique memory architecture in the Ω400 allows memory updates to occur in an average interval that is significantly shorter than the cycle time of the individual 64K memory chips. This allows the speed and efficiency of the specialized graphics processor to be fully utilized by the memory.

The key to obtaining this high memory performance is the use of "cache" techniques like those used by high performance general purpose computers to overcome the relative slowness of large dynamic RAMs. The cache is a block of special high-speed memory that forms a "window" into the large main memory. The processor is usually able to read or write the data it needs into the cache, at high speeds, only occasionally requiring access to the slower main memory. Thus, the average memory access time is essentially that of the cache, rather than the main memory.

In the Ω400, two distinct caches (**Figure 4**), one for read and one for write, allow memory to be copied from one portion of the display memory to another. Thus it is not necessary to continually fill and empty the cache to represent the totally different segments of display refresh memory being accessed as the source and destination for the block transfer. As a result of this cache architecture, the Ω400 writes an updated pixel into memory at the full speed of the graphics processor, one pixel every 220 ns—nearly twice as fast as the normal memory cycle time for the 64K RAMs.

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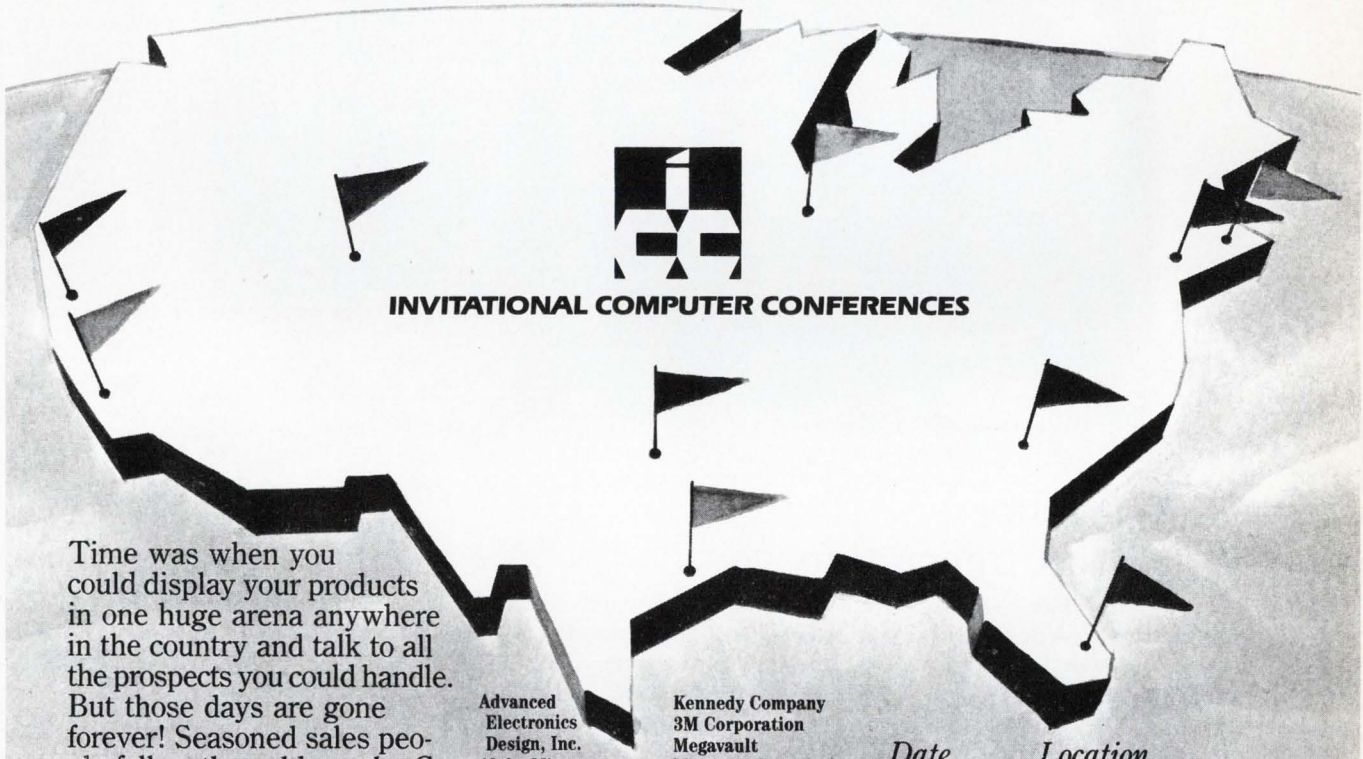

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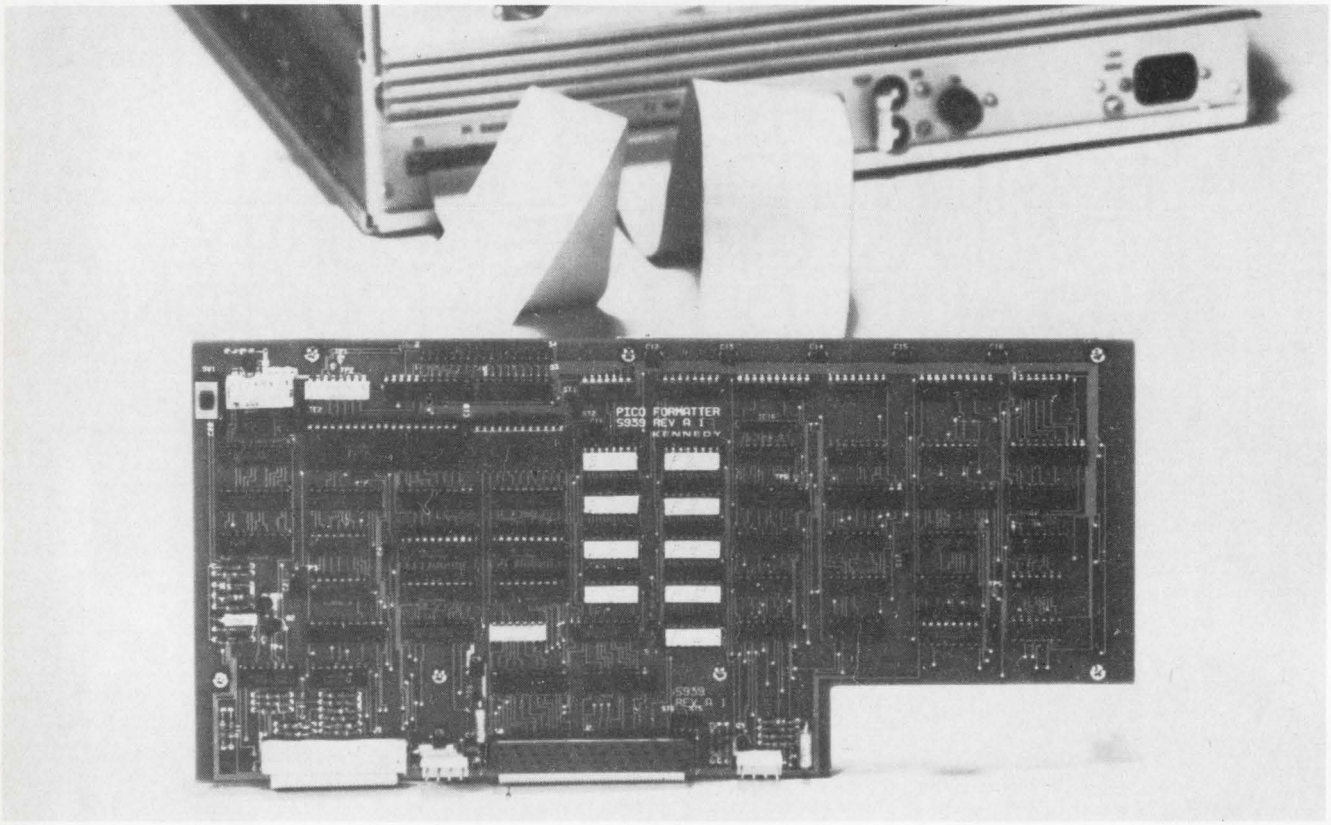

Figure 1: Providing error correction, control of seek and head selection, mapping of defective tracks, establishment of track and sector configurations, and formatting of data for R/W operations, this formatter provides control functions normally found in more expensive controller boards.

Built-In Formatter Simplifies Disk Integration

With increasing interface standardization, and with controller functions being crowded onto a few custom chips and firmware, it seems likely that before long peripheral manufacturers will move the entire controller onto the peripheral itself.

A new intelligent formatter, embedded in Kennedy Co. 82 Mbyte and 165 Mbyte 14″ Winchester disk drives heralds this trend, incorporating many control functions normally associated with the much more expensive disk controllers. Dubbed the PicoFormatter, the board provides error correction, controls seeks and head selection, maps defective tracks, establishes track and sector configurations, as well as formatting data for read/write operations.

Systems integrators may install high-capacity Kennedy disk drives with the PicoFormatter on any minicomputer or microcomputer system. The system requires only a simple interface coupler that translates host commands, data and status to PicoFormatter requirements. The same coupler may be used for tape and cartridge transports provided by Kennedy Co.

The PicoFormatter transfers data either through direct memory access or under programmed I/O. It is capable of sustaining devices with data rates of up to 2.5 Mbytes/sec.

Employing an 8039 μP, the board uses two PROMs to define the logical configuration of the disk drive. The system designer may select any combination of cylinder numbers, sectors per track, bytes per sector and sector-interleave factor.

For error detection and correction, the formatter uses a firecode polynomial which corrects single burst errors up to eleven bits long and detects a single burst of up to 22 bits in length.

Internal firmware provides a means for user-transparent defective track allocation. During disk initialization, up to 30 tracks may be flagged as defective and the formatter will automatically reassign alternate tracks.

The 6″ × 11″ (15.24cm × 27.94cm) card is mounted in the rear of Kennedy Series 5300 Winchester disk drives having unformatted capacities of up to 165 Mbytes. The units have a data rate of 1 Mbyte/sec and an average head positioning time of 30 msec.

Single quantity price of the 5380 with PicoFormatter is $4,995. The 53160 with PicoFormatter is priced at $6,150. (OEM discounts available).

Kennedy Co., 1600 Shamrock Ave, Monrovia, CA 91016.

Write 197

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I	Management
J	Student/Educator
K	Other

AREAS OF MAIN PRODUCT INTEREST

L	Active Components
M	Passive Components
N	Electro-Mechanical Components
O	Tools and Production Equipment
P	Computers and Peripherals
Q	Instrumentation/Test Equipment
R	Control Systems
S	Mechanical/Electronic Packaging
T	Data Communications
U	Power Sources
V	Other

8-BIT CROSS ASSEMBLER

Runs On Prime

A cross assembler which produces object code for many eight-bit CPUs is the CROSS80. CROSS80 has a macro facility that allows the user to modify the assemblers default Z80 instruction set or to define the instruction set of a totally different eight-bit processor. Macro libraries are provided with CROSS80 to accommodate the Intel 8080, 8085, 8048, 8051, etc. The output from the assembler consists of an object file in Intel hex format as well as listing and error reports. A tool to downline load the hex output to a prom programming system through an asynchronous line is also provided. CROSS80 runs on all Prime computer 50 series systems as well as the Prime 400 and 500. The package, including documentation, macro libraries, PROM programming system, and 60 day warranty costs $2,500. **Primarily Software,** 1227 Pearl Street, La Jolla, CA 92037. **Write 154**

FORTRAN86 μC

Based On 8087

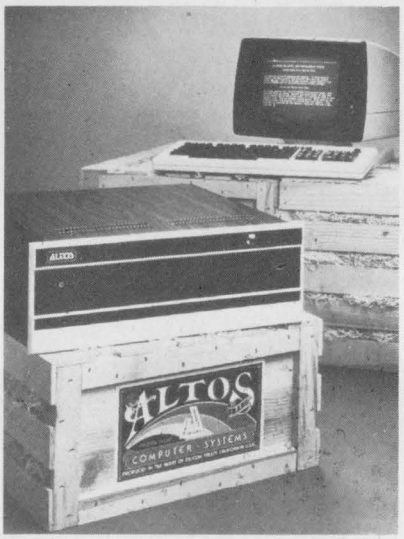
The LABTECH 70 is claimed to be the first commercially available μC to implement FORTRAN86, allowing the user to harness the power of the 8087 floating-point processor directly from FORTRAN. The heart of the system, the Intel 8087 floating-point processor, performs scientific calculations at speeds that equal or surpass the capacity of minicomputer floating-

point processors. The 8087 works as a co-processor with the 8088 on the STD bus. The LABTECH 70 comes with 0.4 Mbytes of memory (which can be expanded to one Mbyte). The system's memory is implemented with the latest generation of 64K RAM chips. Mass storage capacity available as standard with the system is a 5¼", 10 Mbyte Winchester disk drive. Also standard is a 5¼", 620-Kbyte floppy disk drive. Price is $13,800. **Laboratory Technologies Corp.,** 382 Broadway, Cambridge, MA 02139. **Write 148**

16-BIT MICROCOMPUTERS

Three Configurations

The ACS8600 series is offered in three configurations having 20, 40 and 80 Mbyte hard disk drives (each can expand to double capacity.) The units are multi-user, multi-tasking microcomputers serving up to 8 users at once. They have 512 KB RAM, 5 MHz speed, single 8" floppy and expandability from 8 to 16 serial ports with an additional RS-422 port for



800 Kb communications. In addition, the microcomputer features a one port configuration for synchronous communications, and an intelligent disk controller. Proprietary memory management design is optimized for XENIX/UNIX. A parallel interface supports high-speed line printers. **Altos Computer Systems,** 2360 Bering Dr., San Jose, CA 95131. **Write 142**

MULTI-SYSTEM EXECUTIVE

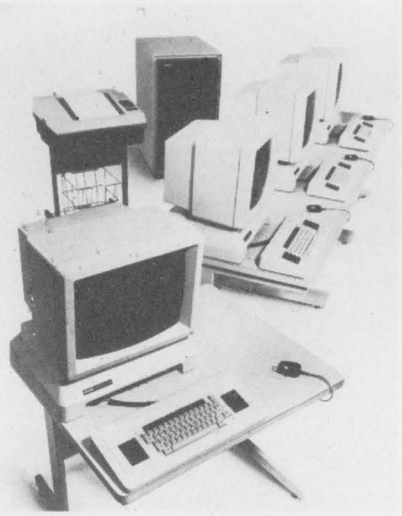
Support Environment For The TeleSoft-Ada Compiler

Intellimac, has announced a commercial release of multi-user Ada. Made possible by Intellimac's Multi-System Executive (IN/MSX), this implementation allows up to 8 users to run TeleSoft-Ada on Intellimac's Multibus, 68000-based IN/7000 Series multiprocessor computer family. Version I of IN/MSX supports up to 1.25 Mbytes of main memory in the single CPU configuration. Version II, can support up to 8 Mbytes of memory and multiple processors. Upon system start-up, IN/MSX asks the operator to enter the maximum number of operators the system is to support. The executive automatically allocates an equal amount of available memory to each user. Each user then starts out his session in the virtual monitor, VMON. From VMON, each user can selectively choose to enter the TeleSoft-Ada Programming Support Environment. Lockouts may be invoked at the device, volume, file, and record levels. **Intellimac,** 6001 Montrose Road, Rockville, MD, 20852. **Write 150**

COMPUTER-AIDED ENGINEERING SYSTEM

Ten Times Faster Design

Scaldsystem, a computer-aided engineering system, consists of a complete set of hardware, procedures, and computer programs that can reduce design time for any digital electronic system by more than ten times, according to the manufacturer. Configured around graphic design stations,



the system offers: A Unix operating system, providing access to a substantial library of software programs; interactive, real-time graphic design stations for schematic editing which can share application programs with a mainframe computer, exchanging large data files at high speed; a cluster system architecture sharing a common data base capable of being accessed simultaneously for a variety of different projects; a new concept of design validation, known as timing verification; a high-speed logic simulator for fast feedback to the design engineer; and a low-cost per terminal system allowing each design engineer the advantages of "personal" computer-aided engineering. **Valid Logic Systems,** 650 N. Mary Ave., Sunnyvale, CA 94086. **Write 143**

ENTRY-LEVEL MAINFRAME

IBM Plug-Compatible

The M80/20 is an entry-level system designed to provide as much as 10% greater performance at a cost 30% lower than IBM's comparable entry level systems, the 4321 and 4331-1. The system is fully compatible with IBM Systems 360, 370 and series 433X software and hardware, including Virtual Storage Extended (VSE) capability and one-level addressing. It is capable of running most operating systems, including VM, VS1, DOS, DOS/VS and DOS/VSE from IBM. It also supports DOS/MVT and MVT/VSE from Software Pursuits. The standard configuration of the M80/20 includes 512 Kbytes of processor storage and two channels along with a system console display and keyboard with audible alarm. A compact version of the M80/20 which occupies 50% less space than comparably configured IBM systems is also available. Features include ECPS:VS1, a hardware assist that reduces CPU time with certain functions in OS/VS1 Release 7 and above; and ECPS:VM/370 extensions, hardware assists that reduce CPU time with certain functions in VM/370 Release 6 and above with associated program products. **Magnuson Computer Systems,** 2902 Orchard Park Way, San Jose, CA 95134.

Write 149

68000-BASED μC

Designed For OEMs

HAWK-32 is a multi-user (up to 16), multi-tasking system that is easily configurable for OEM applications. Its operating system options were selected specifically for OEMs and systems designers, producing a hardware/software combination with a complete set of tools to carry out efficient application development.

HAWK-32 options include two Winchester disk drives with a floppy disk or an Archive streaming tape. The HAWK-32 is available with a choice of either UNIX™ Version 7, with the Berkeley enhancements, or UNOS, the UNIX look-alike from Charles River Data Systems. **Computhink,** 965 W. Maude Ave., Sunnyvale, CA 94086. **Write 146**

AS/9000 SERIES EXPANSION

Three New Models

With the new models, the AS/9040, the AS/9050, and the AS/9070 NAS's AS/9000 series now spans a wide performance range of IBM compatible systems, from the entry-level AS/9040 to the AS/9080. NAS also intends to provide an extended architecture feature as an option for the new AS/9000 models. This feature (previously announced for the AS/9060 and AS/9080) makes the new models of the AS/9000 series functionally compatible with IBM's 308X processor series in both S/370 mode and in S/370 XA (extended architecture) mode. **National Advanced Systems,** 800 E. Middlefield Road, Mountain View, CA 94043 **Write 156**

DESKTOP ENGINEERING TERMINALS

Multi-function Desktops

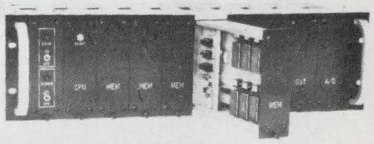
Whizzard 1650 is a new series of raster terminals providing high resolution interactive graphics as well as alphanumeric capability. Digital VT-100/52 compatibility allows users to perform a complete range of functions such as software development and debugging, report and documentation generation, or any other tasks nor-

mally associated with this class of terminals, in addition to graphics operations. Software-compatible with Megatek's top-of-the-line Whizzard 7600, 7200, and mid-range 6200 series of graphics systems, the desk-top Whizzard 1650 features a 19″ display, compact electronics base, and ergonomic keyboard. The single-board electronics package utilizes an Intel 8086 μP for interface and display list management. Other features include: 16 simultaneously displayable colors out of 4096; 640 by 480 full screen pixel resolution; 4096 × 4096 virtual display space; 128 Kbytes standard or 256 Kbytes optional local display list memory. Price is less than $16K in single quantity. **Megatek Corp,** 3985 Sorrento Valley Blvd, San Diego, CA 92121. **Write 155**

INTELLIGENT HIGH LEVEL LANGUAGE CONTROLLER

Features Solid State Disk

The CS105 is an intelligent, high level language controller designed for industrial and process control applications. Operating in ROM resident FORTH, it provides control system designers with the ability to perform program development directly on the machine. The CS105 services a variety of I/O devices and industry stan-



dard busses including STD, IEEE 488 and CAMAC. It can act as a master to existing systems utilizing these busses. The CS105 is supplied with 8085 fig-FORTH. Several other tools include a FORTH de-compiler, an 8085 assembler and a screen-oriented editor. **Controlex Corp.,** 16005 Sherman Way, Van Nuys, CA 91406. **Write 153**

HEMENWAY/FORTH

Takes Advantage of 68000 μP

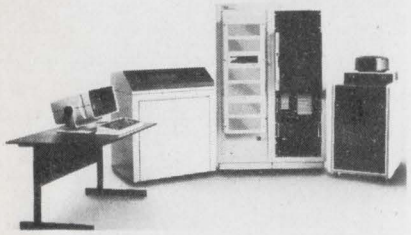
Hemenway/FORTH, a superset of the FORTH-79 standard (of the Forth Interest Group), runs under the MSP/68000 operating system. It is specifically designed to take advantage of the instruction set and 16.7 Mbyte address space of the 68000 16-bit μP. Features of the language system include fast address interpreter routines that increase application system performance; a virtual memory with four 1024-byte block buffers that reduces the number of disk I/O operations needed to perform mass-storage operations; and a 128-character maximum size for variable-length word names, which allows naming flexibility without sacrificing speed within the text interpreter. The language system requires only 8 Kbytes of execution memory and runs most FORTH-79 programs unchanged. Hemenway/FORTH can be incorporated into OEM hardware that runs the MSP/68000 operating system. OEM royalty prices begin at $115 (1–49 units), with quantity discounts and alternate licensing arrangements available. **Hemenway Corp,** 101 Tremont Street, Boston, MA 02108. **Write 147**

New Products • COMPUTERS/SYSTEMS

ADA COMPILER

For Military Computers

A fully implemented DoD-Spec, ANSI 1982 Standard Ada Compiler and Ada Development Environment (ADE) coupled with a powerful multi-terminal, 32-bit computer system, has been announced. Named the ROLM Ada Work Center, the system

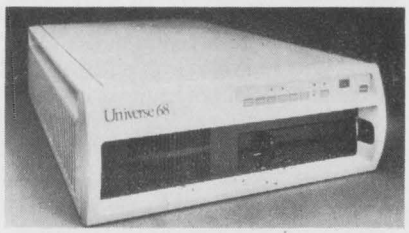


allows from eight to 128 simultaneous users to become immediately productive in the development of Ada language applications. The ROLM Ada Work Center is the first completely integrated package of hardware, software, and technical support available to users who want to get started with Ada now for program design, application development, or Ada training. Complete facilities to develop Ada applications for a full range of ROLM 16 and 32-bit target computers are available. Pricing for the basic ROLM Ada Work Center including the full hardware configuration, license for the Ada software, one full year of comprehensive software maintenance, and one full year of hardware maintenance is $462,000. The target development tools for the 1666/B and MSE/14 are available for an initial software license fee of $25,000 each. **ROLM Corp,** 4900 Old Ironsides Dr., Santa Clara, CA 95050. **Write 145**

32-BIT COMPUTER

Under $10K

The Universe 68/05 is a 32-bit OEM computer priced below $10,000, including disk. The computer has a bus rate of 20 Mbytes/sec (versus 13.5 Mbytes/sec for a VAX-11/750). Its cycle time is 390 nsecs and it has a MIPS (millions of instructions per second) rating of 1.25. The Universe 68/05 incorporates a 165-nsec 4-Kbyte cache memory and is designed around the 12.5 MHz Motorola 68000. The bus structure incorporated is the Motorola VERSAbus, a standard, nonproprietary, 32-bit bus designed for high-performance computers. The single-unit OEM starter-system price for the Universe 68/05 is $9,996, including 256 Kbytes of main memory,



10-Mbyte Winchester disk, floppy disk backup, real-time clock, and four serial ports. At the quantity-ten discount level, the price drops to $9,400, and to $8,330 at the quantity-25 level. End user prices start at $11,900. Systems are available for delivery in 60 days ARO. **Charles River Data Systems, Inc.,** 4 Tech Circle, Natick, MA 01760 **Write 144**

New Products • PERIPHERALS

31.2 MBYTE WINCHESTER SYSTEM

Tape Backup For DEC Q-Bus Minicomputers

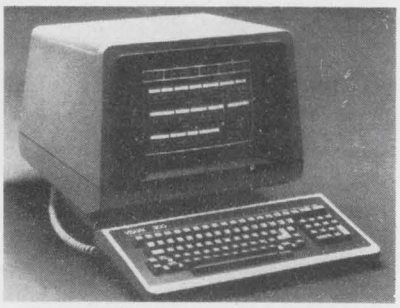
The DSD 890 is a 31.2-Mbyte Winchester system with tape backup. The DSD 890's Winchester emulates three DEC RL02s, while the 890's ¼" tape emulates the ½" TSV05 tape subsys-

tem. This emulation, achieved through the 890's intelligent controller, allows the DEC operating software to communicate to the DSD Winchester and ¼" tape as if they were DEC devices. The 890's ¼" standard cartridge tape drive has start/stop capability to provide transparent DEC software compatibility for tape backup and restore functions. **Data Systems Design**, 2241 Lundy Ave, San Jose, CA 95131 **Write 172**

VISUAL 330

μP-Based Display Terminal

The VISUAL 330 emulates both DEC's VT52 and DG's D200 terminals. Menu-selectable emulation of Lear Siegler's ADM-3A and Hazeltine's 1500 terminals is also included. The terminal features tilt-and-swivel capabilities, 12" or 14" non-glare



screen, high density 7X9 dot matrix characters, detached low-profile keyboard and matte finish keycaps. A menu-style set-up mode eliminates the need for cumbersome switches. Price is $1,150. **Visual Technology**, 540 Main St, Tewksbury, MA 01876. **Write 176**

LOGIC-GATE OPTOCOUPLER

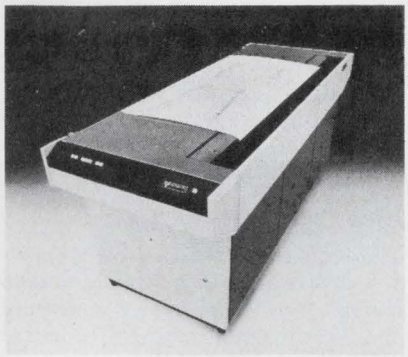
High-Speed,CMOS-Compatible

A new logic-gate optocoupler provides high speed and a wide Vcc capability and is sensitive enough to be driven by most CMOS circuitry. Operating at a typical speed of 5 MBaud, the HCPL-2200 optocoupler accepts a forward current as low as 1.6 mA. The HCPL-2200 optocoupler has a typical supply current of 4.5 mA in logic low and 2.7 mA in logic high when Vcc is 5.5V. Due to its wide, 4.5-volt-to-20-volt Vcc range, the HCPL-2200 can be designed into circuits using 12- or 15-volt supplies. Directly compatible with data busses, the HCPL-2200 offers a three-state output. Thus, in TTL applications, a pull-up resistor is not required. The HCPL-2200 is compatible with LSTTL logic, which makes the new optocoupler suitable for providing isolation of high-speed logic systems and interfacing computer to peripheral or μP to μP. $4.50 each (1000 qty.). **Hewlett Packard**, 3000 Hanover St., Palo Alto, CA 94304. **Write 131**

PLOTTER

Uses 52.5" Width Paper

The 8252-A electrostatic plotter offers the extra plotting width specifically requested by automotive designers, that enables plotting of compact automobile side views without stripping of multiple plots. Plotting resolution is 200 points per inch (40,000 points per square inch). Rated speed of 0.25



inches per second delivers 5.4 square feet of plotted area per minute. The 8252-A prints 652 columns of standard ASCII characters in a high resolution 16 by 20 matrix at 120 lines per minute. **Versatec**, 2805 Bowers Avenue, Santa Clara, CA **Write 175**

STREAMING TAPE CONTROLLER FOR LSI-11

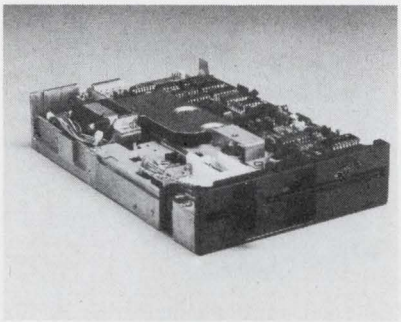
Interfaces Archive And Cipher ¼" Drives To DEC LSI-11 QBUS

The STV11 is packaged as a dual height LSI-11 QBUS module and emulates the DEC TM11 for software compatibility with all DEC operating systems. A single 50 conductor ribbon cable connects the controller to up to two Archive or Cipher streaming tape drives with 2 or 4 recording tracks. The device address and interrupt vector are switch selectable and for selecting a non-standard address and vector. From 10 to 45 Mbytes of data can be stored on a single 450 ft. tape cartridge depending on the tape drive model used. Data may be recorded at rates up to 87,200 bytes/s on 90 IPS drives. These rates allow 1 Mbyte to be recorded in less than 12s. The controller incorporates CRC error checking and results in less than 1 non-recoverable error in every 10 billion bits. Recording methods allow a maximum tape usage efficiency of over 97%. Pricing begins at $1,500 with quantity pricing as low as $945. **General Robotics Corp**, 57 North Main Street, Hartford, WI 53027. **Write 181**

HALF-HEIGHT MINIFLOPPY DISK DRIVES

Feature Fast Track-To-Track Access Times

The Shugart SA455 (48 tracks-per-inch) and SA465 (96 TPI) are exactly half the height of standard minifloppies, allowing users to double existing system capacity by replacing one full-sized drive with two half-heights. 1 Mbyte of capacity is available on the SA465 and 500 Kbytes on the SA455.

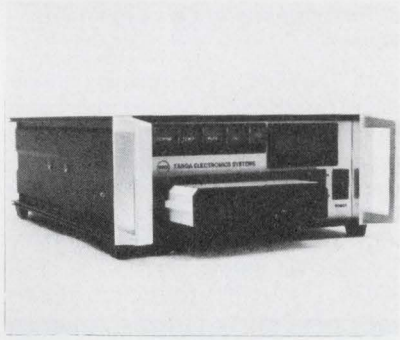


Track-to-track access time is 3ms for the SA465 and 6ms for the SA455. In addition, these drives are media and interface compatible with the industry standard SA400/450 and SA410/460 series. **Shugart Associates**, 475 Oakmead Parkway, Sunnyvale, CA 94086. **Write 182**

BUBBLE MEMORY DATA STORAGE SYSTEM

Includes Four Versions Of Cartridge

The DR3101 recorder connects to any computer or peripheral using an RS232C interface or IEEE 488 bus. The unit includes tape recorder emu-

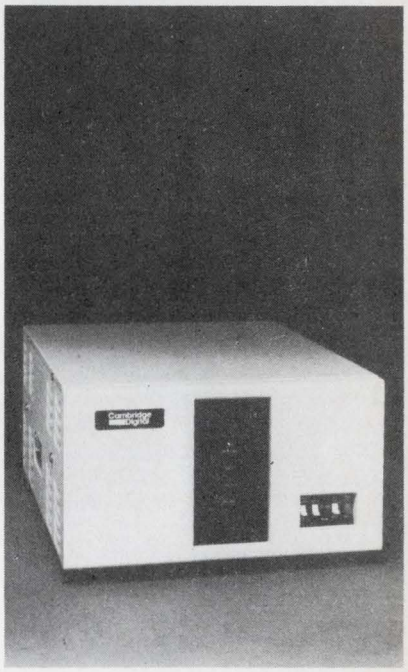


lator software for RS232C interfaces and both tape recorder and floppy disc emulator software for IEEE 488. Custom software is also available as a factory option. Four cartridges are available with data capacities of 128 or 256 Kbytes with operating temperatures of either 10 to 40°C or 0 to 55°C. Each has been designed for repeated insertion and removal a minimum of 20,000 cycles. Data transfer rates are up to 200,000 bps. Data access times average 48 ms, to a maximum of 96 ms. Bit Error rates are on the order of 1×10^{-14}. **Targa Electronic Systems**, PO Box 8485, 3101B Hawthorne Road, Ottawa, Canada K1G 3H9. **Write 174**

LSI 11/23-BASED SYSTEM

Features A 70 Mbyte Winchester Disk And 20 Mbyte Streaming Tape

The system 94 is housed in a compact standalone or rackmounted enclosure. It offers 256 Kbytes of high-speed MOS RAM, expandable to 4 Mbytes; four serial I/O ports; and a

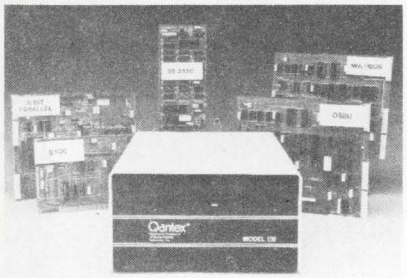


large, extended LSI backplane. An integral memory management scheme allows users to directly access up to 22 bits of address space or 4 Mbytes of RAM. Floating point processors and an array processor are available to enhance the system's computational performance. The high-speed Winchester drive is formatted as two RK07 and one RK06 drives on a single controller. The streaming tape controller emulates DEC's TU10/TM11 tape subsystem, permitting easy file backup and recovery with most available utilities. **Cambridge Digital Systems**, 65 Bent Street, Cambridge, MA 02139. **Write 184**

TAPE BACKUP EXPANDED INTO FAMILY

Now Offers Five Interfaces

The Qantex Model 150 Cartridge Tape Backup System has been expanded, with interfaces for RS-232C, MultiBus, 8-Bit Parallel, Ohio Scientific and S100 Bus. The desk top unit, measuring only 10″W × 5″H × 15″D, requires no additional hardware or software to operate with computer systems using any of the above inter-



faces. The Model 150 in a desk top cabinet consists of the Qantex 451C Tape Drive, controller, cable, and power supply. The 150, designed as a cartridge tape backup system for Winchester hard disks, stores data from the disk on a ¼″ DC 300 tape cartridge with a formatted capacity of 13.4 Mbytes. Featuring a 2 minute-per-Mbyte backup rate, the Model 150 provides file-oriented backup and is menu driven. The new 150 system is suited for data logging and archival storage applications. Single quantity price is $2995 to $3125, depending on interface. **Qantex,** Div. of North Atlantic Industries, 60 Plant Avenue, Hauppauge, NY 11788.

Write 178

4D DIGITIZER

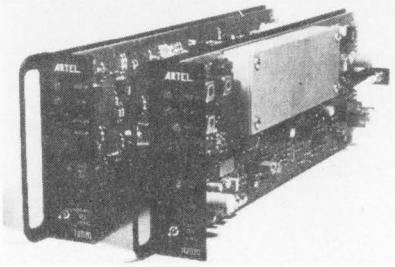
X, Y, Z And Tilt

It is now possible to include a 4th dimension stylus tilt to graphic digitizer tablets. Previously, those who used a stylus and digitizer for interacting with a graphic CRT were limited to 3 dimensional direct manipulation of images. Now it is possible to directly control rotation of 2D or 3D images, or pan while zoomed, by using stylus tilt information transmitted concurrently with the X, Y and Z information. The new technology permits electronic sensing of the magnitude and direction of stylus tilt with respect to the tablet's surface, and transforms the stylus into an unrestrained joystick/digitizer. **GTCO Corp.,** 1055 First Street, Rockville, Maryland 20850. **Write 210**

FIBER OPTIC MODULES

Video And Audio On A Single Card Module Set

With applications in television ENG and distribution, local area networks and closed circuit TV/audio, the T/R-2020 trnasmitter/receiver module allows a maximum transmission distance of 1 km as compared to the 6.4 km (4 mile) range of other SL-2000 module systems. The T/R-2020 card modules plug directly into a S-2000

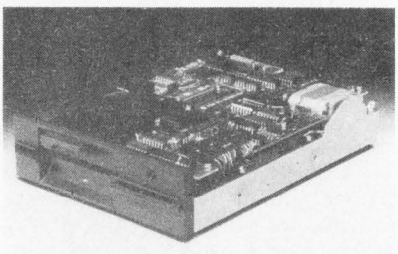


Universal Card Frame, with up to nine modules per frame. The T-2020 Transmitter accepts 75Ω, 1Vp-p video and 600Ω balanced audio, and converts these signals to a composite optical signal which is transmitted through the fiber optic cable. The R-2020 Receiver reconverts the optical signal to full level video and audio. BNC connectors are used for the loop through video inputs and dual video outputs. Three-pin XLR connectors are used for the audio input/output. Price for the T/R-2020 video/audio transmitter/receiver module set is $2250. **Artel,** PO Box 100, West Side Station, Worcester, MA 01602. **Write 180**

5¼″ HALF-HEIGHT DRIVE

8″ Performance In One-Eighth The Volume

With 1.6 Mbytes unformatted storage capacity, the 5¼″ YD-380T drive uses an 8″ drive controller, and is fully compatible with 8″ double sided formats. The YD-380T has a 500 Kbits/s transfer rate, and a 3 ms track-to-track transfer rate. Using removable 5¼″ flexible storage media, the YD-380T's 154 usable tracks provide 96



TPI track density and up to 9646 BPI recording density. The 1.62″ high × 5.75″ wide × 8″ deep size of the YD-380T was accomplished by its smaller motor and a unique head design. To eliminate cross talk between high density packed tracks, a tunnel erase head is used to trim the tracks. Read/write and erase gaps are set by azumith to precisely trace the tracks' curvature, and to accurately define the border between recording and non-recording areas on each track. The head has been shielded against EMI. OEM quanity price is $350 per unit. **C. Itoh Electronics**, 5301 Beethoven St., Los Angeles, CA 90066. **Write 177**

REMOVABLE DISK DRIVE

Uses "Whitney" Technology

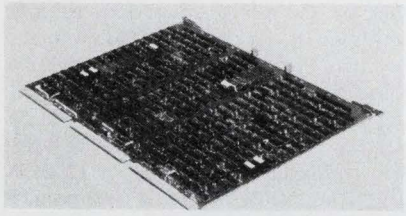
The Arapahoe 7110 is a fixed/removable disk drive with 25 Mbytes of data storage fixed in a sealed enclosure and 25 Mbytes in an ANSI-standard removable cartridge. The 7110 is interface and performance compatible with Control Data Corporation's Lark

II fixed/removable drive. A high-performance servo system incorporates an on-board μP to read servo blocks embedded in each data track. Absolute tracking accuracy, with an average access time of 35 ms is provided. Local or remote testing has been simplified by a front panel interface port that enables diagnostics to be run without the need to power down or remove the drive from its cabinet. With the 8″ floppy drive profile, two Arapahoe drives will fit into a RETMA-standard 19″ rack in a horizontal configuration, or three drives will fit the same rack in a vertical arrangement. The 7110 drive carries a unit price of $3,215 in quantities of 100. Quantity shipments are scheduled for the first quarter of 1983. **Amcodyne**, 805 South Lincoln St., Longmont, CO 80501. **Write 179**

HIGH—SPEED CMI INTERFACE

For Connecting Disk Storage To VAX-11/750

This new interface, which enables existing field-proven 9400 and 9800 disk storage systems to connect directly—via a single board—to the VAX-11/750's CMI bus, can be installed in any one of the three high-speed Massbus adaptor slots. It interfaces up to four host CPUs to the 9400 or 9800 storage systems, enabling users to configure

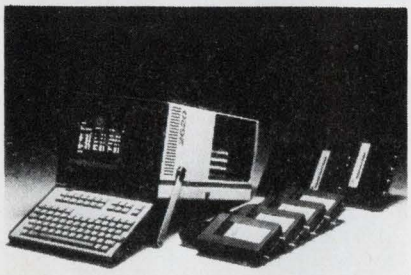


their systems with multiple CPUs and multiple controllers to share a common database. A variety of Winchester- and SMD-type drives with unformatted capacities ranging from 80-Mbytes to 675-Mbytes are available from the company. Drives of different type and capacity can be mixed on the same system offering maximum user-flexibility for expansion. Price for the CMI interface starts at $15,200 for a 160-Mbyte Winchester system including controller; delivery is 30 days ARO. **System Industries,** P.O Box 789, 1855 Barber Ln, Milpitas, CA 95035. **Write 211**

FIELD MAINTENANCE PROCESSOR

First in a Family of Systems Test Products

The 2620 Field Maintenance Processor (FMP) is the first in a series of fully compatible testers designed to provide an integrated systems test approach to the servicing of complex, μP-based products. By combining in-circuit emulation, logic

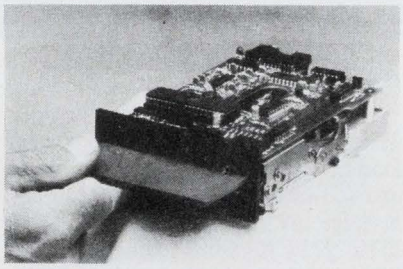


analysis, communication testing and program preparation capabilities with interactive software, the 2600 series enables users to select the most appropriate and cost-effective level of testing—be it on-site, depot or factory, system, board or component—to suit the particular needs of both their field service organizations and their product types. Compact and lightweight (34 lbs.), the FMP is ideal for the testing and repair of large computer mainframes, communications equipment, office equipment, point-of-sale terminals and electronic consumer products. Based on a powerful Z80A μC, the 2620 hardware consists of a software-controlled 7″ CRT display; 265 Kbytes of memory; an 85-key tactile keyboard; a 5¼″ disk drive; a 20-column thermal printer; and a built-in acoustic coupler with modem. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742 **Write 167**

3½″ MICROFLOPPY DISK DRIVE

One-Fourth The Volume of 5¼″ Drive

The TM35 Microline disk drive provides 875 Kbytes on two sides of a 3½″ diameter diskette, accesses this data in an average time of 85 ms, and moves from track-to-track in 3 ms. The TM35's physical package is 1⅝″ high, 4″ wide and 6⅛″ deep. Two models of the TM35 are being intro-



duced to achieve compatibility with two classes of disk drives. The TM35-2 is compatible with the 5¼″ industry standard interface. It will produce a 5¼″ look-alike diskette, with 40 tracks per side, double-sided recording, 250 kbits/s transfer rate and 500 Kbytes capacity. It can fit into a 5¼″ half-height envelope. The second model, TM35-4, is compatible with the Sony OA-D30V microfloppy disk drive's interface, software, and diskette, but has data recorded on both sides of its disk. Price of the full-performance TM35 is in the $200 to $225 range in large OEM quantities. Delivery of evaluation units is scheduled for the first quarter of 1983. High volume manufacturing will commence in 1983. The TM35 features a recording density of 7610 bits per inch, 135 tracks per inch, and 70 tracks per side in the Sony-compatible TM35-4 model. The 5¼″ compatible TM35-2 model features 6255 bpi, 135 TPI, and 40 TPS. Both models use FM/MFM recording. **Tandon Corp,** 20320 Prairie St, Chatsworth, CA 91311 **Write 173**

DEC-COMPATIBLE MASS STORAGE

Features Winchester Disks And Tape

This series of complete, DEC-compatible mass storage systems features advanced Winchester disk technology and high-speed streaming tape backup. Each system can be equipped with up to four Fujitsu Winchester disk drives, and ad advanced streaming tape drive for backup from Cipher Data Products. The Guardian 100, with an unformatted, per drive storage capacity of 84.4 Mbytes, is configured around a Fujitsu 8″ Winchester drive; the 200, with 168.5 Mbytes unformatted storage capacity per drive, uses a Fujitsu 14″ Winchester drive; and the 500 model has 474.2 Mbytes of unformatted storage capacity per drive, and employs Fujitsu's sophisticated 10½″ "Eagle" Winchester package. Single quantity list prices based on one disk drive, tape backup, and controller, are $12,500 for the model 100; $15,500 for the 200; and $20,500 for the 500; quantity discounts are available. **Group III Electronics,** 2615 Manhattan Beach Blvd, Redondo Beach, CA 90278. **Write 168**

CDC 9766 REPLACEMENT

For CDC Line

The AMS 315 is a 300 Mbyte, SMD compatible Winchester emulation for Control Data Corporation's 9766 removable pack drive. It is one-third the size of comparable 3330 technology pack drives with the same capacity, and is plug compatible with CDC's 9766 removable pack drive, Ampex's 9300A, and Century Data's Trident T306. The AMS 315 has an MTBF in excess of 10,000 hours. Features include the Winchester sealed, contamination controlled disk compartment, a ventilated spindle to provide temperature balancing of the disks for reduced off-track errors, a spin motor brake to reduce unstable flight time of heads and minimize data loss, and a carriage lock to prevent movement of heads during shipment. The drives will be priced under $7000 for OEM 100 quantities, with significant discounts for larger orders. **Century Data Systems**, 1270 N. Kraemer Blvd., Anaheim, CA 92806. **Write 171**

New Products • PERIPHERALS

TRI-DENSITY MAGNETIC TAPE SYSTEM

For Intel Multibus Computers

The MTC Model 4000 is a fully self-contained data storage system and is provided complete with all required cabling and documentation. The basic tape system contains a Multibus compatible single board controller, software driver, TELEX tri-density Model 6250 formatted tape transport, equipment rack, manuals and all required cabling. A complete system can be provided within 60 days ARO for under $34,000. Quantity discounts and OEM arrangements are available. **Mesa Technology Corp**, 16021 Industrial Drive, Gaithersburg, MD 20877. **Write 183**

16-BIT MICROCONTROLLER

Offers Fastest Operations, Most Extensive I/O Features

This 16-bit microcontroller, designed for high-speed math and control operations, offers the highest level of integration ever achieved in a single-chip controller. With over 120,000 transistors, the 8096 microcontroller is designed with CPU and I/O handling on the same chip, and both CPU and I/O are tightly integrated in terms of functionality. The 8086's I/O is designed to interface with a wide range of transducers and sensors and to offload real-time I/O operations from the CPU. The new microcontroller's I/O includes an eight-level priority interrupt structure, analog input, PWM output, high-resolution pulse measurement and pulse output, full duplex serial I/O, 40 parallel I/O ports and a watchdog timer. The basic 8096 microcontroller will be available in the first quarter of 1983 in 10,000-unit quantities at a U.S. price of $15 each. **Intel Corp,** 5000 W. Williams Field Rd, Chandler, AZ 85224. **Write 169**

GANG PROGRAMMER

EEPROMS And EPROMS

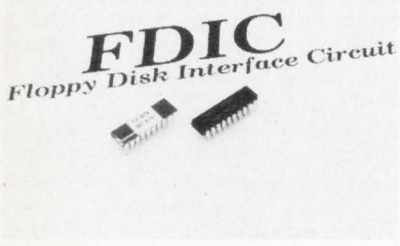
The Z-1200 gang programmer is designed to program, test and verify EPROM and EEPROM devices from 2K × 8 to 16K × 8 (128K bits). The unit has twelve 28-pin programming sockets, 16K × 8 Data Ram expandable to 64K × 8, full editor, dual independent RS-232C Serial I/O ports with all popular communications formats, is self diagnostic and self recalibrating and uses English word prompting for ease of operation. Device types, serial formats, baud rates and functions can be selected either by the unit's keypad, a remote terminal or a computer. By connecting two Model Z-120 gang programming slaves to the Z-1200, each having 12 programming sockets, up to 36 devices can be programmed or verified simultaneously. The Z-1200 is also compatible with the companion Model Z-100 universal slave that, with selected plug-in programming cards, programs devices such as FPLA, PAL, and non-standard bipolar PROMs. **Sunrise Electronics**, 524 South Vermont Ave., Glendora, CA 91740 **Write 170**

New Products • COMPONENTS

INTERFACE CIRCUIT

Floppy Disk Drive Control And Support

The FDC 9229 is designed to complement all popular floppy disk controller/formatter LSI circuits, including the broad FDC 179X and FDC 176X families of controllers offered by Standard Microsystems. Using a number of proprietary, patented techniques, the FDC 9229 incorporates a revolutionary digital data separator, write precompensation logic, head-load timer, and crystal oscillator, all in one 0.3-inch wide 20-pin dual-in-line package. A single pin configures the FDC 9229 to work with either the FDC 179X or μPD765 type of floppy disk controller. The FDC 9229 is available in two versions: the 8 MHz FDC 9229 which is intended for 5¼" disks and the 16MHz FDC 9229B for 5¼" and 8" disks. The FDC 9229 is available from stock in both plastic and ceramic dual-in-line packages. The price in plastic at 100 pieces is $11.30 each for the FDC 9229, and $12.50 each for the FDC 9229B. **Standard Microsystems**, 35 Marcus Blvd., Hauppauge, NY 11788.

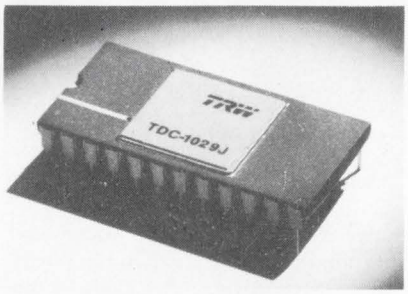


Write 136

A/D CONVERTER IC CHIP

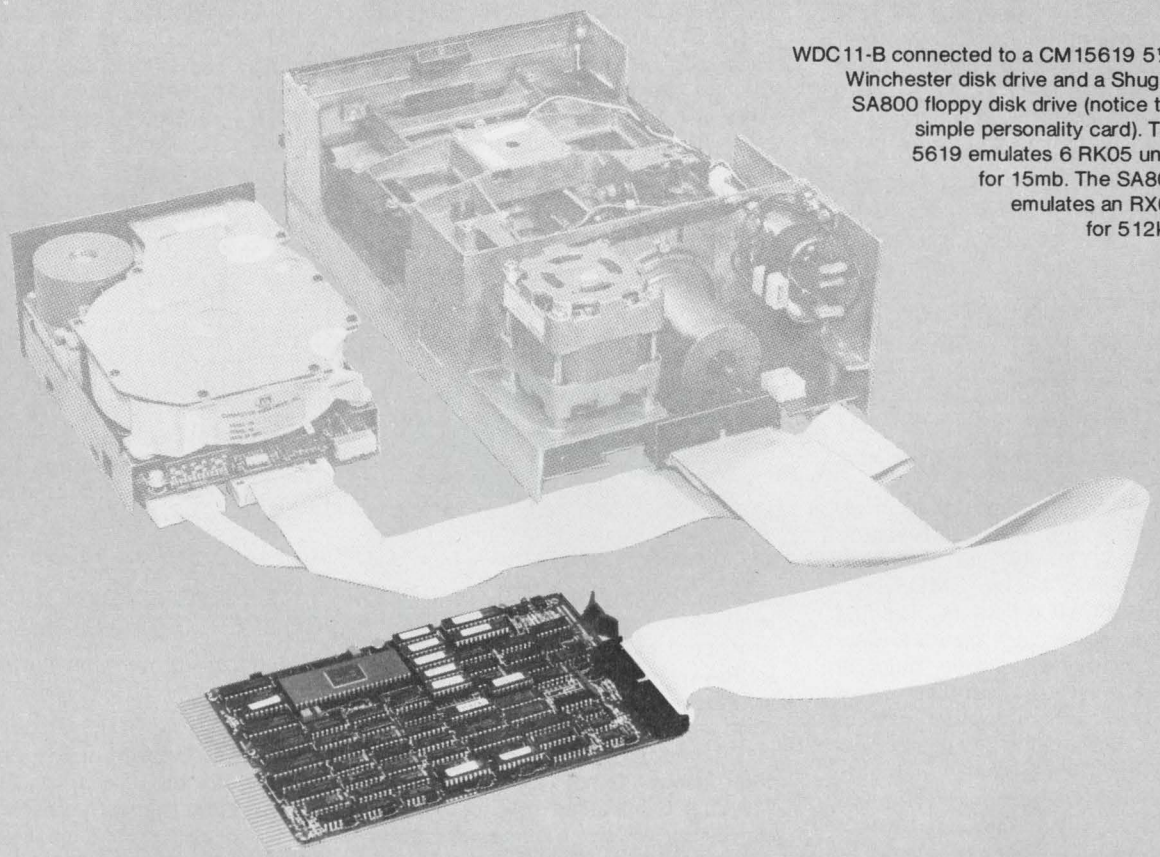
6-Bit Performance At 100 MSPS

This A/D converter IC chip guarantees 6-bit performance at 100 megasamples per second (MSPS) and provides a full-scale analog input bandwidth of 50 MHz while residing in a 24-pin DIP dissipating a maximum 1.8 watts. Utilizing TRW's Omicron-B process as well as two layer metalization, speed and circuit complexity are enhanced to form the world's first commercial one-micron, dual-layer metal VLSI circuit. The TDC1029J operates from a single -5.2 VDC power supply. The full scale analog input dynamic range is 1 volt peak-peak. Digital interface is single-ended ECL compatible. The MSB output is differential, allowing the user select either binary or two's-complement output coding. 100 MSPS operating speed is guaranteed over the full 0-70°C ambient temperature range. **TRW LSI Products**, P. O. Box 2472, La Jolla, CA 92038. **Write 137**



The WDC11 series...

The FIRST family of Winchester/Floppy controllers for the LSI-11/Q-Bus



WDC11-B connected to a CM15619 5¼" Winchester disk drive and a Shugart SA800 floppy disk drive (notice the simple personality card). The 5619 emulates 6 RK05 units for 15mb. The SA800 emulates an RX02 for 512kb.

Unsurpassed Freedom Of Choice

Choose the **disk drive sizes** that are right for YOUR application: The WDC11 controls 8" and 5.25" drives, Winchester and floppy.

The **DEC emulations** that YOU need: RK05, RL01/02, RP02 for the Winchester and RX02/03 for the floppy. All Winchester emulations provide 22-but addressing; RLV21-compatible.

The **disk drive vendors** that YOU want to use: The Following manufacturers build drives that are currently supported: Shugart, Quantum, Tandon, Qume, Computer Memories, Disctron (RMS), Rodime, Ampex, Micro Peripherals, Seagate. Any drive with a standard interface (SA1000, SA800/850, ST506, or TM100-4) can be controlled by the WDC11. A single PROM chip adapts the WDC11 to a specific drive configuration.

The **controller form-factor** YOU want: A single, dual-width card includes the Winchester controller, the floppy controller and an intelligent bootstrap. There is no external formatter board that you need to mount and supply power to. The WDC11 requires only 2.7A of +5V. Simple personality cards adapt the WDC11 to multiple drives, various pinouts and signal levels.

The **experience** YOU are looking for: Andromeda has been shipping WDC11's since the Summer of 1981.

The **growth potential** that YOU require: As new, higher capacity, higher performance disk drives become available, the WDC11 can be adapted to them by simply changing the configuration PROM. New emulations and data formats can be handled in a similar fashion.

DEC, LSI-11, RK05, RL01/02, RX02, and RP02 are trademarks of the Digital Equipment Corp.

ANDROMEDA® SYSTEMS INC.

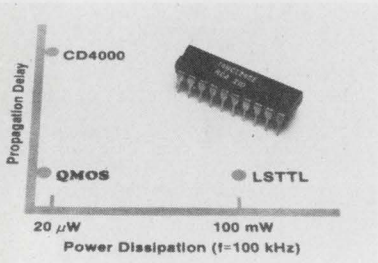
9000 ETON AVENUE
CANOGA PARK, CA 91304
Ph: [213] 709-7600
TWX: [910] 494-1248

Write 19 on Reader Inquiry Card

QMOS LOGIC FAMILY

50 Different Circuit Functions

The advanced family of QMOS high-speed CMOS logic combines the low-power consumption of CMOS technology with the high speed of low-power Schottky TTL (LSTTL). Two series of devices will be available: 74/54*HCT*XXX, having TTL logic levels



QMOS — High-Speed CMOS Logic from RCA

which will be drop-in replacements for corresponding LSTTL functions of the 74/54 family and the 74/54 *HC*XXX family, having CMOS logic levels for all CMOS systems. The first 50 device types include eight varieties of bus transceivers, three different arithmetic circuits, four counter types, four encoder/decoder devices and five multiplexers. The QMOS line features high-noise immunity typical of CMOS technology for HC product and will be fabricated with a 3-micron isolated silicon gate process. **RCA/Solid State Division**, Route 202, Somerville, NJ 08876. **Write 140**

SEMICUSTOM μC

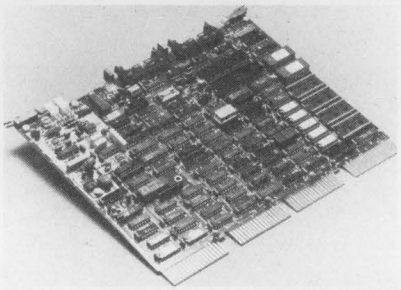
Mask-programmable, Read-only Memory

The 2921, with a mask-programmable ROM, is geared to high-volume applications. Its analog signal processing is a digital μC that has been optimized to handle analog input and output in real time. The 2921 provides four analog inputs and eight analog outputs. It can perform several simultaneous processing fuctions. The single chip handles tasks that in the past have been assigned to a number of separate analog circuits using components such as op amps, resistors and capacitors. All other signal processors on the market are designed with digital I/O and require other components for A/D and D/A conversion. An EPROM version of the 2921, Intel's 2920, is available for low-volume applications. The price per chip (in quantities of 1,000 or more) is $22.90. **Intel Corp.**, 5000 W. Williams Field Rd., Chandler, AZ 85224. **Write 134**

SPEECH SYNTHESIZER

DEC-Compatible Version of LISA

LISA, the high quality, low-bit rate speech synthesizer, is now available in a DEC-compatible version. The LISA/DEC is in a Q-BUS form factor, but can be adapted to either Q-BUS or UNIBUS to make it compatible with the full range of systems from Digital Equipment Corp. LISA/DEC synthesizes speech at 4800 bits per second, and has 64K of dynamic RAM on-board with 53K available to the user, providing 90 seconds of

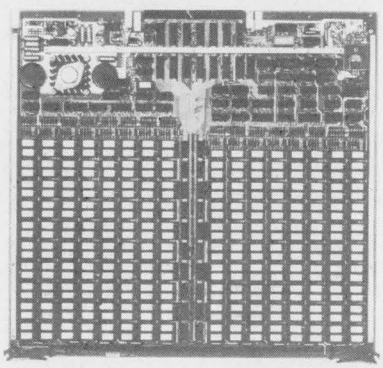


speech. There is also 32K of ROM available for speech data. LISA/DEC consists of a Z80 μP with 64K dynamic RAM, a 16-lattice filter (16-bit arithmetic, 12-bit output DAC), a 4-watt amplifier, and two serial ports (DTE and DCE), and has a quad-wide board. Other applications for LISA/DEC include: computer-aided instruction, audio training, operator prompting, and industrial alert/alarm. The digital speech is generated by Centigram's VoiceWare Development System and stored on disk or burned into PROMs. LISA/DEC is priced at $2,450 (single unit price). OEM prices are available. The device is immediately available, 60-90 days ARO. **Centigram Corp.**, 155A Moffett Park Dr., Sunnyvale, CA 94086. **Write 130**

2.0MB ADD-IN

Perkin-Elmer 3200 Series

This single board 2.0MB DR-330 semiconductor add-in can be used with

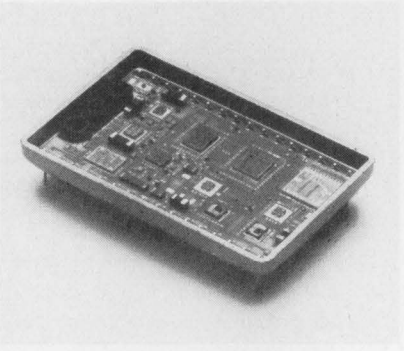


Perkin-Elmer's 3210, 3230 and 3250 minicomputers, while still being compatible with the older 3220 and 3240 members of Perkin-Elmer's 3200 series. The DR-330 is also available in 1.0MB, 512KB, and 256KB configurations. The 2.0MB and 1.0MB DR-330 employ 64K dynamic RAMs; the 512KB and 256KB versions use 16K RAMs. The 2.0MB and 1.0MB DR-330 may be used in place of Perkin-Elmer's 35-694 and 35-764 Storage Modules, respectively. The 512KB and 256KB DR-330 can also be used in place of Perkin-Elmer's 35-694 Storage Module. The DR-330 interfaces to Perkin-Elmer's Memory Interface Board or Local Bank Controller Board. The 2.0MB, 1.0MB, 512KB, and 256KB DR-330 are $10,600, $6,400, $3,900 and $2,640, respectively. **Dataram Corp.**, Princeton Rd., Cranbury, NJ 08512. **Write 127**

16-BIT HYBRID SYNCHRO CONVERTER-TO-DIGITAL

Offers Transformer Isolation and μP Compatibility

The HSD1106 (HRD1106) hybrid synchro(resolver)-to-digital converter offers both high accuracy (1.3 arc-minutes) and transformer isolation for reference and input signal voltages. These converters are both 8 and 16-bit μP compatible. Typical applications for the 1106 include robotics, machine tool control systems, solar panel control systems, avionics systems, antenna monitoring, servo systems, coordinate conversion, axis rotation, fire control systems, engine

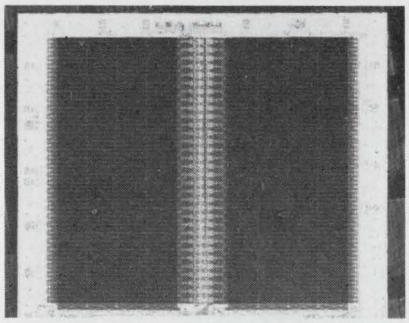


controllers, industrial control systems and simulation. Pricing in 1–9 quantities, is $495, with 6 week availability. **Natel Engineering Co.**, Inc., 8954 Mason Ave., Chatsworth, CA 91311-6162. **Write 166**

256K CMOS MASK ROM

Jedec Approved Pinout

The MP2326 has JEDEC approved pinouts for bytewide memories and is pin compatible with the Intel EPROM 2764. The device features low power dissipation and a fast access time. The true standby supply current value is only 0.1μA (typical, at room temperature) and while in the idle or non-switching state the value is only 40μA (maximum). The device is available in 450 and 850 ns versions. The Model MP2326 has a 32,768 words by 8-bit memory configuration, and interfaces with a number of μPs. Packaging includes a 28-pin plastic and a 44-pin flat pack. The device is available in die form, and a special 28-pin CERDIP can be ordered. Nominal programming charge

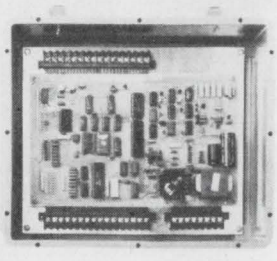


of $2,400; 1,000 piece price for the 28-pin plastic, 450 ns device is $30 each, and the 850 ns device is $27 each. Minimum order of 1000 pieces. **Micro Power Systems**, 3100 Alfred St., Santa Clara, CA 95050. **Write 132**

TRANSCEIVER CONTROLLER

Single Board, Industrial Grade

The SBR-700 "Mini Remote", is a single board, industrial grade transceiver controller for use in supervisory control and data acquisition sys-

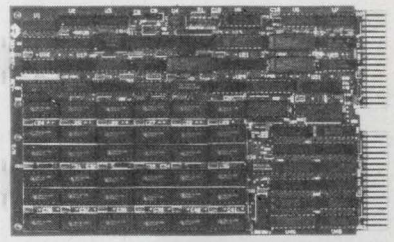


tems. It is designed to provide analog, digital, pulse, I/O control and monitoring, as well as data communications for mini computer systems. The SBR-700 delivers complete with real world connections for both analog and digital signals, as well as a variety of communications interfaces for radio, telephone line and cable. The single board, Intel 8085-based system is furnished with MultiTronics' Compac CN software and is completely debugged and fully documented. Communications drivers are available for a variety of minicomputers and microcomputers. $1,200 in single quantity. **MultiTronics**, PO Box 2295, Dublin, CA 94566. **Write 135**

MSC 4806 MEMORY BOARD

256Kb Full Parity Memory For LSI-11/23

A new dual-high, 256Kb, parity memory board for the LSI-11/23 CPU is now available. The new MSC 4806, which includes a CSR, is a full equivalent of DEC's MSV11-L. Totally supported by DEC diagnostics, the MSC 4806 allows the user to select starting addresses in 4Kb increments throughout the full four Mbyte address range. Single voltage 64K RAMs require only a 5VDC source, and a battery back-up version is also available. High reliability, adherence to DEC specifications, and socketed elements provide the OEM with an excellent alternative which is easily field maintainable. Addressing and capacity are set on-board via jumper blocks (rath-

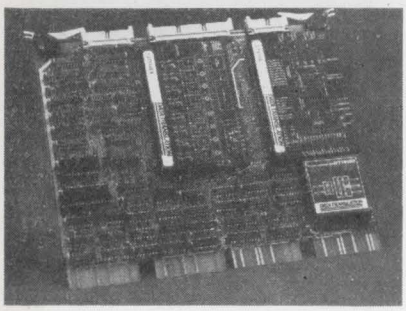


er than switches) for increased reliability. A one-year parts and labor warranty is standard. Delivery is two weeks ARO for small quantity orders. Single unit pricing for the MSC 4806 is $979 for the 256Kb version and $761 for 128Kb. **Monolithic Systems Corp.**, 84 Inverness Circle East, Englewood, CO 80112. **Write 126**

DATA ACQUISITION BOARD

Features Simultaneous Sample And Hold

A new LSI-11 compatible data acquisition board features simultaneous sample and hold (SS&H) capabilities and Continuous Performance data transfers to disk. The DT3388 analog input board allows the user to take a snapshot of up to 12 high level analog

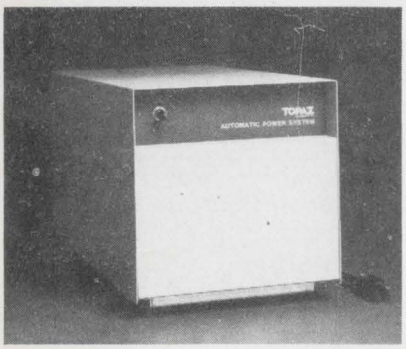


input channels, freezing their values within a +/−5ns aperture uncertainty period, and to transfer the analog data to continuous disk files at rates of up to 90,000 samples per second. Available in 4 and 12 channel versions, the DT3388 is a complete LSI-11 Bus compatible system with analog input functions, simultaneous sample and hold circuitry, a high speed 12-bit 100kHz analog to digital (A/D) converter, and control and bus interface logic all contained on a single quad height board. Prices for the DT3388 in 1-9 quantities are $2795 for the 4 channel version and $3295 for the 12 channel version. CPLIB is priced separately at $1495. Delivery for both is 5 days ARO. **Data Translation**, 100 Locke Dr., Marlboro, MA 01752. **Write 129**

AUTOMATIC POWER SYSTEM

Offers Small Computers Blackout Protection

This 300 VA square-wave Automatic Power System (APS) is specifically designed to protect small computer-based equipment against losses of primary AC power. The APS provides highly reliable brownout and blackout protection and features dual output receptacles for ensuring plug compatibility with virtually any type of equipment, from point-of-sale terminals to security systems. The system consists of an internal 20-ampere-hour battery, a battery charger, a static inverter and a power transfer switch. When line voltage falls below a predetermined level, the transfer switch immediately transfers the load from the AC line to the APS inverter; typical transfer time is four ms. The inverter converts the battery power from DC to AC for powering the critical load. Backup times range from 12 minutes to 180 minutes depending on the APS model and load rating. When adequate line voltage is restored, the load is automatically transferred back to the AC line, and the battery charger recharges the battery for protection against subsequent line failures. Prices start at $690. **Topaz Inc.**, Powermark Div., 3855 Ruffin Road, San Diego, CA 92123. **Write 185**



VACUUM FLOURESCENT DISPLAY

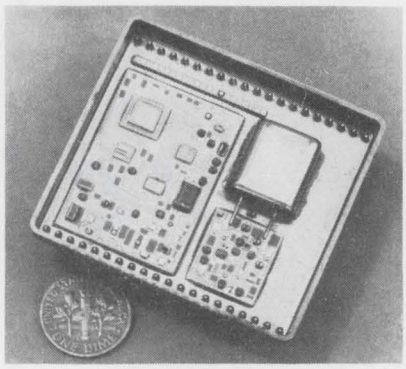
Revised Module Mounts Components On-Board

Model DE/420A features a multilayered single PC board on which all display components, including the +5vdc power conversion, are mounted. All standard features, such as an on-board μP for display buffer, character generation of the full 96 character ASCII set, refresh, cursor control and self-test are retained in the new design. The DE/420A displays 20 uniquely addressable positions of 5 × 7 dot matrix characters, measuring .35″ (9mm) high by .25″ (6.3mm) wide for easy viewing at distances up to 20 feet. The highly visible blue-green upper and lower case characters can be filtered to blue, green, yellow and aqua. Special cross-hatched filters allow the display to be read in many direct daylight applications. Low power consumption (2.5W typical) permits the display to be used for portable applications also. Price of the DE/420A is $250 (qty. 100); delivery is two weeks ARO. **Digital Electronics Corp.**, 197 Airport Blvd., Burlingame, CA 94010. **Write 186**

DIGITALLY COMPENSATED CRYSTAL OSCILLATORS

Compensates For Frequency Drift

A new digitally compensated quartz crystal oscillator, designed for portable or remotely located equipment requiring low power and high stability,

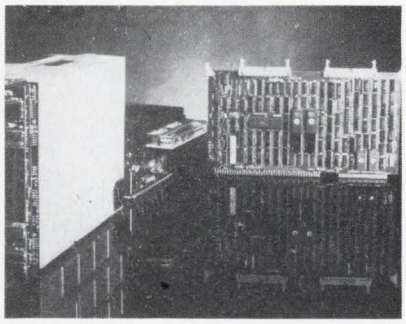


represents the first use of digital techniques to compensate for frequency drift with temperature in hybrid oscillators. They utilize CMOS technology to provide minimal power dissipation and may be customized to meet specific requirements. Available design options include choice of output logic, TTL, CMOS, ECL; choice of supply voltage; package options; stability optimized for specified temperature range; and digital frequency adjustment for aging correction or for system synchronizations. Use of the EEPROM to store the compensation data allows the DCXO to be recompensated or programmed a number of times. The frequency response as a function of temperature can also be tailored to match system requirements. Single unit price of the new DCXO is $900, and delivery is 8 weeks ARO. **Hughes Solid State Products**, Frequency Control Devices, 500 Superior Avenue, Newport Beach, CA 92663. **Write 187**

MULTIBUS-COMPATIBLE CONTROLLER

Handles 8 Disks, 4 Tape Drives

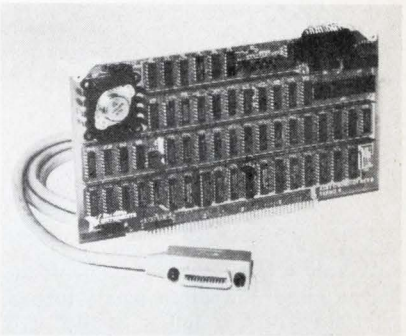
An intelligent, Multibus-compatible controller is capable of handling up to 8 ANSI winchester disk drives and up to 4 3M HCD 75¼" cartridge tape drives. The Rimfire 75 Controller features DMA operation with 24-bit addressing and separate 32-bit ECC word on each sector I.D. and Data Block. It is programmable for 8- or 16-bit systems. The controller's simple Parameter Block Interface provides many programmable options, including Bus Lock, Linked Commands, Interrupts and ECC/Retry Disable Flexible format capability is achieved with an Auto-interleave option. The Rimfire 75 executes commands in six categories: Disk and Tape Drive Control, Disk and Tape Drive Transfer, Dump/Restore and Specials. With Disk Data Transfer, a simple command may transfer up to 65K sectors of data between the system memory and disk. Each sector is buffered on board. Rimfire 75: $1450 (qty 25). **Computer Products Corp.,** 2405 Annapolis Ln, Plymouth, MN 55441. **Write 207**



S-100 TO IEEE-488 LINK

Provides High-Speed DMA Performance

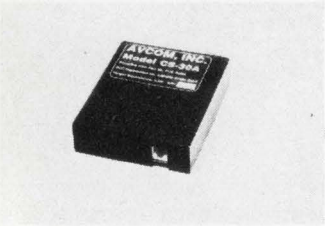
The GPIB-696 is a high-speed interface between the IEEE-488 bus and S-100 computer systems. The DMA capability of the GPIB-696 provides data transfer speeds of 333 Kbytes/sec between the IEEE-488 and the S-100 buses. This speed capability is five to ten times faster than transfer speeds possible on previously available interfaces. The GPIB-696 will also support S-100 systems with 24 bit addressing. All GPIB functions are provided including (Extended) Talker, (Extended) Listener, and Controller. The interface is designed to work in either a single or multiple controller environment with a programmable System Controller feature making it ideal for redundant systems. In single unit quantities the package sells for $995, with 30 day delivery. **National Instruments,** 12109 Technology Blvd, Austin, TX 78759 **Write 208**



MODEM MODULE

Single Component μP Control

Model CS-30A, a state-of-the-art modem module, provides a direct access to phone lines through a single component for microprocessor control. The module has a 300 baud rate capability with logic-selectable answer or

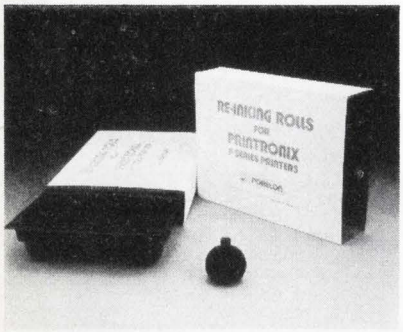


originate modes and is capable of dial out in either DTMF or rotary format. Model CS-30A is only 4″ × 3¼″ × 1″ in size; has a ring detector for auto-answer, plus auxiliary audio-input/received-line audio output functions. It is ideal as a direct-connect data link for data systems or industrial process control monitoring. 1-9 unit price of $149.95 or at $109.00 in 100 qty. **Avcom, Inc**, P. O. Box 29153, Columbus, OH 43229. **Write 133**

INKING SYSTEM

Reduces Ribbon Costs On Printronix Printers

An inking system to increase ribbon life on the Printronix P-series printers has been introduced by Porelon, Inc.



The retrofit system features a barrel-shaped ink roll which provides a constant supply of fresh ink, keeping the ribbon moist and strong. The barrel shape of the roller improves the migration of ink from the top and bottom of the ribbon, as well as assuring proper contact with the printer's ribbon at all times. P-series printers operating at top line speed modified with the system, have experienced 100% to 300% increases in ribbon life. The ink rolls retail for approximately $60 per dozen and the mounting brackets for $23 per set of two. The modification can be made in minutes by installing the brackets with two existing screws located on the ribbon deck assembly of the printer. **Porelon, Inc.,** 1480 Gould Dr., Cookeville, TN 38501. **Write 157**

DEC CONTROLLER MODELS

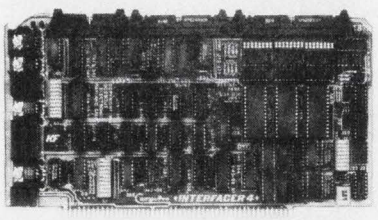
Emulates DEC RK06/07 Subsystems

The new "C" models of the DEC compatible SPECTRA 12 disk controller and SPECTRA 21 multifunction disk/tape controller emulate the DEC RK06/07 subsystems, and enable Spectra Logic to interface with the DEC VAX Unibus. Through this firmware set, these models can now support various mappings and attach a large variety of disk types including the Century Data Marksman, Priam Diskos, Ampex Capricorn and Fujitsu Eagle drives. The enhanced models of the existing SPECTRA 12/A and 21/A controllers emulate the DEC RM02/05 subsystems, and now can attach the same large variety of drive types as the SPECTRA 12/C and 21/C models. Both the A and C models of the SPECTRA 12 and 21 also support various mapping schemes on CDC and CMD compatible drives. The SPECTRA 12/A and 12/C models are priced at $2900 and the SPECTRA 21/A and 21/C models are priced at $3600 in OEM qty. of 50. Larger volume discounts are available. **Spectra Logic Corp.**, 1227 Innsbruck Dr., Sunnyvale, CA 94086. **Write 139**

S-100 BUS I/O BOARD

Accommodates As Many As 32 Users

An advanced serial/parallel interface board which allows as many as 32 contiguous users at the same eight

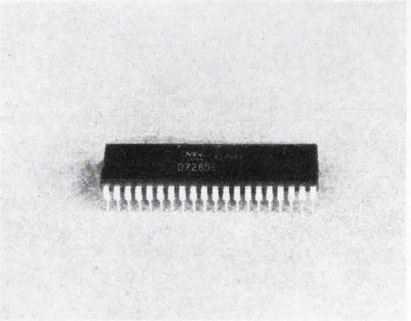


port locations is now available. Conforming to all S-100/IEEE 969 timing specs, the Interfacer 4 incorporates an asynchronous serial interface and two synchronous/asynchronous high-speed channels. It also includes a Centronics-style parallel interface and a universal parallel port for custom interfacing. A proprietary user selection port permits the cascading of up to eight Interfacer 4 boards at the same port address, thereby increasing the efficiency of the software, especially in multi-user environments. Interfacer 4 also features selectable 0, 1, 2 or 3 wait states for system operation at more than 10MHz, and switch selectable port addressing to any 8-port block. In addition, the board's interrupt structure offers a full masking and a flexible strapping capability to facilitate multiuser operation. Interfacer 4 board: (OEM discounts). **CompuPro,** Oakland Airport, CA 94614. **Write 209**

MICRO FLOPPY CONTROLLER

For Sony Microfloppy Disk Drive

The μPD7265 μFDC allows the user to realize the full microfloppy storage capacity of 437.5 Kbytes by conforming to the data format recommended by Sony Corporation. Key features of the μPD7265 controller include: programmable data record lengths,

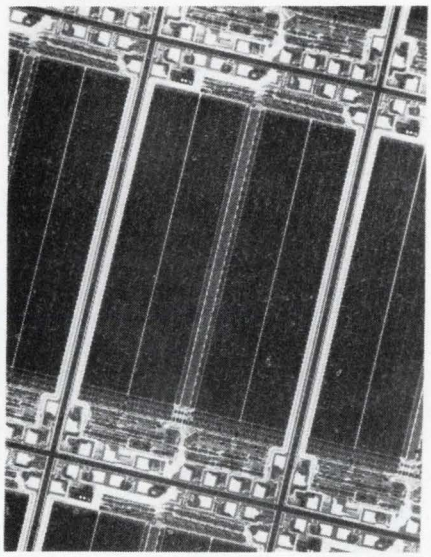


multi-sector and multi-track transfer capability, controls up to 4 drives, DMA or non-DMA mode, parallel seek capability on up to 4 drives, and 5 volt only supply. The μPD7265 utilizes a disk format that differs slightly from the IBM 20 standard. While conforming to the Sony recommended format, the μPD7265 is still able to read standard IBM formats. In addition, it is possible to utilize a combination of Sony drives and standard 5¼″ or 8″ drives. $24, 100 qty. 12 week lead time. **NEC Electronics**, Microcomputer Division, One Natick Executive Park, Natick, MA 01760. **Write 138**

16K CMOS STATIC RAM

Fastest Memory Device In Its Class

A new low-power 16k × 1-bit CMOS static RAM, the IDT6167, is believed to be the fastest memory device in its class for both commercial and military markets. The commercial part specifies equal address access, chip-select

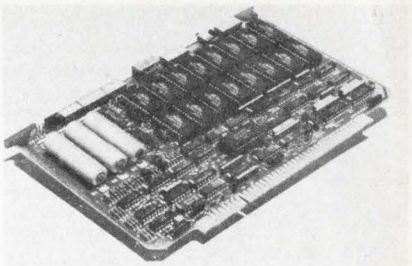


access and read-cycle time options of 45, 55, 70 and 85ns. The military version also offers four speed options, 55, 70, 85 and 100ns. This is more than 20% faster than access times available with NMOS devices. The IDT6167 is aimed at memory applications requiring high speed, high density and very low power consumption. The device is ideally suited for use in telecommunications and industrial systems, and a broad range of military applications. 100-piece prices range from $21 to $42; production quantities will be available in the fourth quarter of this year. **Integrated Device Technology, Inc.**, 3236 Scott Blvd., Santa Clara, CA 95051. **Write 128**

NON-VOLATILE EXORCISER MEMORY

Real Time Calendar, 32K

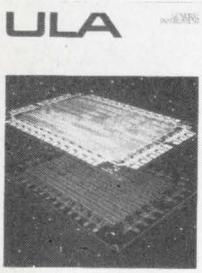
Static, CMOS RAM and on-board batteries provide non-volatile storage for the MM-6800CT memory board that is compatible with EXORciser™ I and II microcomputers. Included in the new board's performance features are: cycle and access times of 250



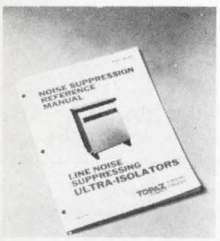
nsec, switch-selectable module selection on 1000 (hex) boundaries, no refresh delays, and bank select that extends the memory map to 1 Mbyte. On-board batteries allow both non-volatile capability and real time calendar functions that operate even if the +5 V supply is removed. The calendar counts seconds, minutes, hours-of-the-day, days-of-the-week, date, month and year. Typical applications for this feature are data logging and instrumentation systems. In unit quantities, price of the 32 Kbyte version of the MM-6800CT is $750; a 16 Kbyte version is $695. Delivery is off-the-shelf. **Micro Memory, Inc.**, 9436 Irondale Ave., Chatsworth, CA 91311. **Write 163**

New Literature

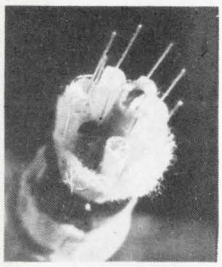
Signal Converter Brochure. A new 4-pp. brochure, complete with transmit line and receive specifications, covers the STU-5M signal converter and terminating unit. In addition to a listing of key product features and detailed applications information, the brochure provides extensive performance characteristics including transmit line and receive specifications, ordering data, and applicable logistic support information.
Dataproducts **Write 264**



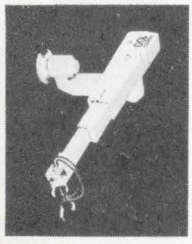
ULA Brochure. This detailed brochure presents a portfolio of CMOS Uncommitted Logic Arrays. Designed as a presentation tool, the brochure explains the logical rationale behind using General Instrument ULAs as replacements for standard MSI and SSI devices for cost and application efficiency. The brochure offers further detailed insight into the philosophy behind ULA design, and approach to ULA development and application.
General Instrument **Write 265**



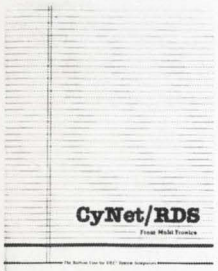
Noise Suppression Manual. A new AC Line Noise Suppression Reference Manual is a basic text on the protection of sensitive electronic equipment from the problems created by AC line noise, transients and spikes. This manual covers the basics of AC line noise suppression, provides valuable technical data and includes many typical applications.
Topaz Inc. **Write 259**



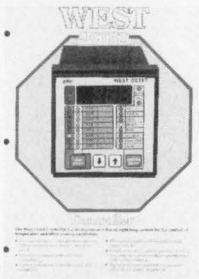
FiberLAN Brochure. A new 8-pp. brochure explains how Siecor FiberLAN functions as "architect and general contractor" in the design, integration, and implementation of fiber optic load area networks. Also described in the brochure is how FiberLAN collaborates with local area network (LAN) system suppliers, manufacturers of terminal equipment, and software companies.
Siecor **Write 275**



Robot Brochure. A new brochure describes the MAKER 100 Robot System. MAKER 100 is a five-axis, electric servo-driven robot capable of handling a 5 lb. payload. The many applications of this flexible, high precision robot include: assembly, material handling, machine tool and injection molding, machine loading and unloading, inspection, and adhesive application.
United States Robots **Write 272**



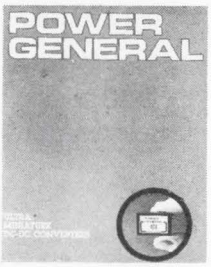
Cynet/RDS Brochure. A 4-pp., 3-color brochure describes Multi Tronic's CyNet/RDS and RDS-1600 combination hardware/software package. The cost savings benefits of buying a pre-packaged software tool (CyNet) for integration into industrial process control systems is outlined. The brochure also describes a modular hardware package (RDS-1600) for use in monitoring and control of industrial signals and control elements.
Multi Tronics **Write 253**



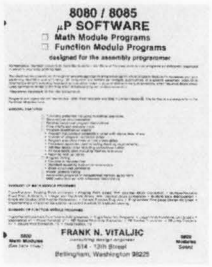
Octet Controller Brochure. The Octet Controller, a microprocessor-based eight loop system for controlling temperature and other process parameter, is fully-described in a new four-color brochure. The brochure lists the Octet Controller's features, applications and specifications. The complete system includes a panel-mounted operator station measuring 96mm × 96mm and a 19″ rack containing the plug-in processing and input/output circuits.
West Instrument **Write 269**

Power Conditioning Equipment. The 24-pp. technical bulletin describes how to protect electronic equipment from voltage dips, surges and electromagnetic noise. Solutions offered to clean up "dirty" power problems include voltage stabilizers, line conditioners and Type ES noise isolation transformers.
General Electric **Write 251**

CAD System 60/10 Brochure. Detailed is a complete CAD work-station for printed circuit design, based on a PDPII–03 central processor, coupled with a high-speed, interactive color graphics interface. Comprehensive programs are included for clearance control, automatic comparison with the original data base, power supply checks, etc.
EIE **Write 252**



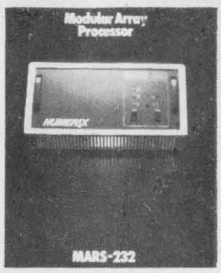
DC-DC Converters. A 2-pp. data sheet describes a new line of 15 to 50 watt regulated DC-DC converters. There are 9 models to choose from and all electrical and mechanical specifications are outlined in detail. Individual model characteristics are presented in tabular form and include complete prices.
Power General **Write 274**



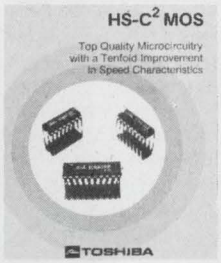
μP Software. A 4-pp. brochure of program specifications for the 8080/8085/6800/6809 microprocessors features programs including: fixed/floating point arithmetic; FP binary/decimal conversion; bit/byte manipulation; number compare; general purpose; trignometric/hyperbolic and their inverses; exponential and power functions; logarithms; square root extraction; polynomial evaluation and more.
Frank N. Vitaljic Co. **Write 257**

Simulation Computer Applications. A new, colorfully illustrated brochure describes dozens of successful applications for simulation computers. Many disciplines are covered, including aerospace, road and off-road vehicles, reciprocating and turbine engines, maritime, missiles, and much more. 24-pp.
Electronic Associates Inc. **Write 263**

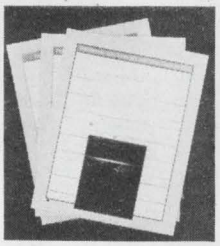
New Literature



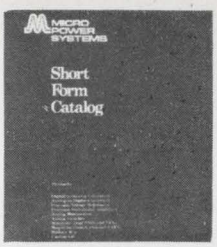
Array Processor Brochure. Brochure describes the MARS-232 Modular Array Processor and includes detailed specifications, features, and applications. Descriptions of both off-line program development software and run-time software are presented. Typical application functions for the MARS-232 Signal Processing Library are included.
Numerix Corp. **Write 273**



Toshiba Fact Sheet. Toshiba America is the U.S. subsidiary of one of the world's largest suppliers of semiconductor and integrated circuits. Current principal products include: 8K × 8 CMOS Static RAM; 64K Dynamic RAM; 2K × 8 Static RAM; 2K × 8 NMOS RAM; 8K × 8 NMOS EPROM; and 32K × 8 NMOS ROM.
Toshiba Semiconductor **Write 278**

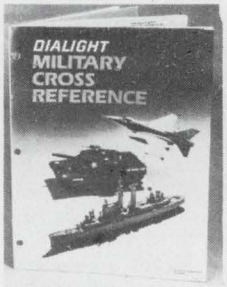


Modems Brochure. This full-color, fold-out brochure provides product specifications, applications diagrams, functional charts, and panel call-outs for the MX Series 2400 bps modems. This special brochure is one of a series from Codex that currently includes the MX Series, CS Series Network Control Modems, and IMS 7000 Series Electronic Data Switches.
Codex **Write 276**



Micro Power Catalog. The b/w, 12-pp. catalog lists all of the current and new products for 1982. Four product areas have been expanded: military ICs, dual transistors, op amps and DACs. MPS now provides a complete line of DACs ranging from a 6-bit DAC up to an 18-bit DAC, and op amps from OP-01 to OP-37.
Micro Power Systems **Write 250**

Laser Capability Brochure. This new brochure lists the many and varied Laser applications capacities of Applied Laser Systems. Applied Laser Systems is a complete Laser machining and processing facility specializing in prototype and production applications of Laser technology.
Applied Laser Systems **Write 254**



Military Cross-Reference Catalog. A new military cross-reference catalog covers indicator lights, indicator-light housing, lampholders and indicator-light lenses. This 20-pp. guide, illustrated with photos and dimensional drawings showing recommended mounting holes, lists military designations side-by-side with current Dialight part numbers for easy reference. All products included in the catalog have received Department of Defense certification.
Dialight **Write 261**

Digital Design pays $70 for suitable Application Notebook articles. These short descriptions of design problems and solutions, circuits or brief programs/subroutines are clipped by EEs and used in their designs. Have you designed and breadboarded a novel useful circuit that would interest other engineers? Or have you written a unique microcomputer (or even programmable calculator) subroutine program? If so, then we invite you to share your ideas with our readers. Circuits and software must not be previously published, and we ask that you include all relevant schematics and block diagrams. Finally, please insure that your program is debugged and your circuit bench-tested. All submissions should be addressed to:

Circuits Editor
Digital Design
1050 Commonwealth Ave.
Boston, MA 02215

New Literature

Product Summary Catalog. A 52-pp. shortform catalog provides descriptions of the integrated product lines available from all five LeCroy Divisions: High Energy Physics (HEP), Acquisition and Control Systems Division (ACS), Fiberoptic (FSD), California (CA), and European Products (EPD). The catalog contains product photos, short descriptive specifications, and comparison and capability charts.
LeCroy Research **Write 255**

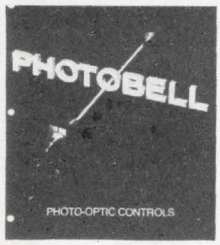
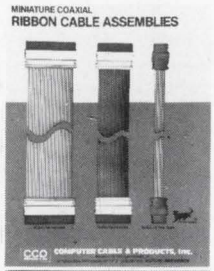


Photo-Optic Controls. A 12-pp. catalog contains guidelines for making selection of photo-optic controls and describes comprehensive product line. Terminology and applications for single unit types and 2-unit projector/receiver types are described. Special application systems, integral controllers, external controllers and housing dimensions are also covered.
Photobell Co. **Write 267**

Multimeter Brochure. A new, 6-pp., four-color brochure features three 4½-digit low-cost multimeters—two handhelds and a benchtop unit. The brochure contains product descriptions, full specifications, pricing and ordering information for all three instruments. Included are the two newest members of the 4½-digit family, the popular 8060A and 8062A handheld DMM's. A complete list of accessories available for the instruments is included.
John Fluke Mfg. **Write 262**

Tape Drive Data Sheet. A data sheet describes the new Series 2000 ½" streaming tape drive. Models in the series record at 1600 bpi (optionally 3200 bpi), with PE encoding. Various models stream with velocities of 50, 62.5, 100 and 125 ips and operate in start-stop mode at speeds of 12.5, 25 or 31.25 ips. Series 2000 features a short tape path and only five moving parts for high data and mechanical reliability.
Digi-Data Corp. **Write 277**

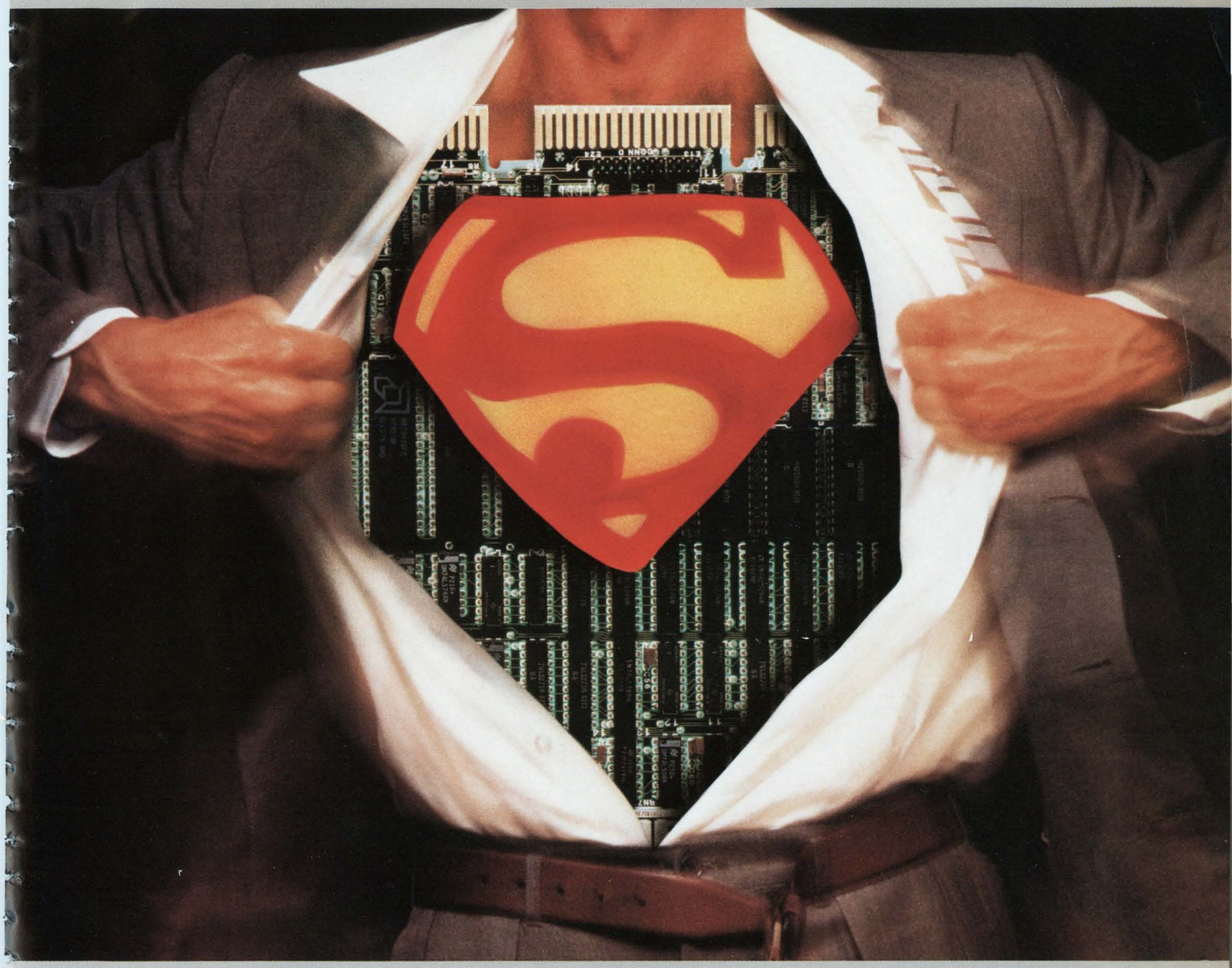


Ribbon Cable Brochure. A new brochure features the complete line of miniature coaxial ribbon cable assemblies. The brochure gives complete specifications and provides ordering information. CCP's line of standard dual latch housing coax cable assemblies are fully described and indicate the advantages of the product. Also shown are Custom Assemblies that provide cost saving with the use of mass terminations.
Computer Cable & Products **Write 256**

1982 General Catalog. The original catalog of computer supplies and accessories features over 3500 products for word processing and computer operations. Included are print-wheels, printer ribbons, word processing and computer forms, binders and binder storage, media storage, microfiche systems, and a complete line of ergonomic CRT furniture and accessories.
Visible Computer Supply Corp.
Write 270

Advertiser Index

IT'S SUPERCONTROLLER!



It's a 6250 BPI (GCR) controller that can handle dual and tri-density drives from STC and Telex.

It's a software compatible streamer controller for today's streaming 1/2″ drives.

It's a TS11* emulator.

It's a 6250 BPI streamer controller for tomorrow's new technology GCR streaming drives.

It's a single board imbedded controller with a 64K byte onboard memory that acts like a large buffer in start-stop mode and as a multiblock staging buffer while streaming.

It's the TS-6251 Supercontroller from Western Peripherals, the company that has put more magnetic tape on DEC Unibus computers than any other independent supplier. Call or write us for technical details.

western peripherals

Division of WESPERCORP

14321 Myford Road, Tustin, CA 92680
(714) 730-6250 TWX: 910 595-1775 CABLE: WESPER

*Trademark Digital Equipment Corporation

Write 2 on Reader Inquiry Card

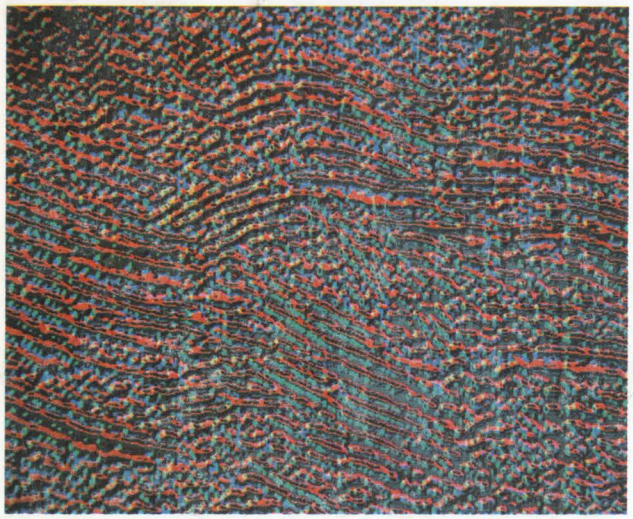
IMAGE PROCESSING: THE FASTEST, LEAST EXPENSIVE WAY TO FIND OIL.

Where to drill? Traditionally, exploring a 25,000 square mile frontier for an answer to that question could take months. And cost over a million dollars for consultant fees and aerial photography.

Today, a DeAnza Image Processing System can narrow the same frontier to a few miles using roughly $100.00 worth of satellite data. *And* help project the final drill site in less than thirty days. Remarkably, the system itself is paid for several times over, exploring just a single frontier.

Get The Complete Picture

Image processing is the *only* way all geological data can be considered *simultaneously:* LANDSAT, SEASAT, radar, magnetic, gravity, topographical, etc. Step-by-step, a DeAnza Image Processing System graphically displays faults, folds and stratigraphic units to pinpoint areas small enough for seismic exploration. Finally, the system enhances seismic data gathered in the field to project final drill sites. And these projections stay completely confidential, because they're done in-house.



Enhanced seismic data of an oil find.

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Gould/DeAnza is one of the world's leading suppliers of image processing systems. For one very good reason. No other supplier offers systems with power, flexibility, and range of operations equal to ours. Nobody. Call or write us today. Let us help you explore the possibilities of image processing. It may be the richest find you make this year.

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