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DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS MAY 1984

DISPLAY FUNCTIONS MIGRATE TO GRAPHICS DEVICES

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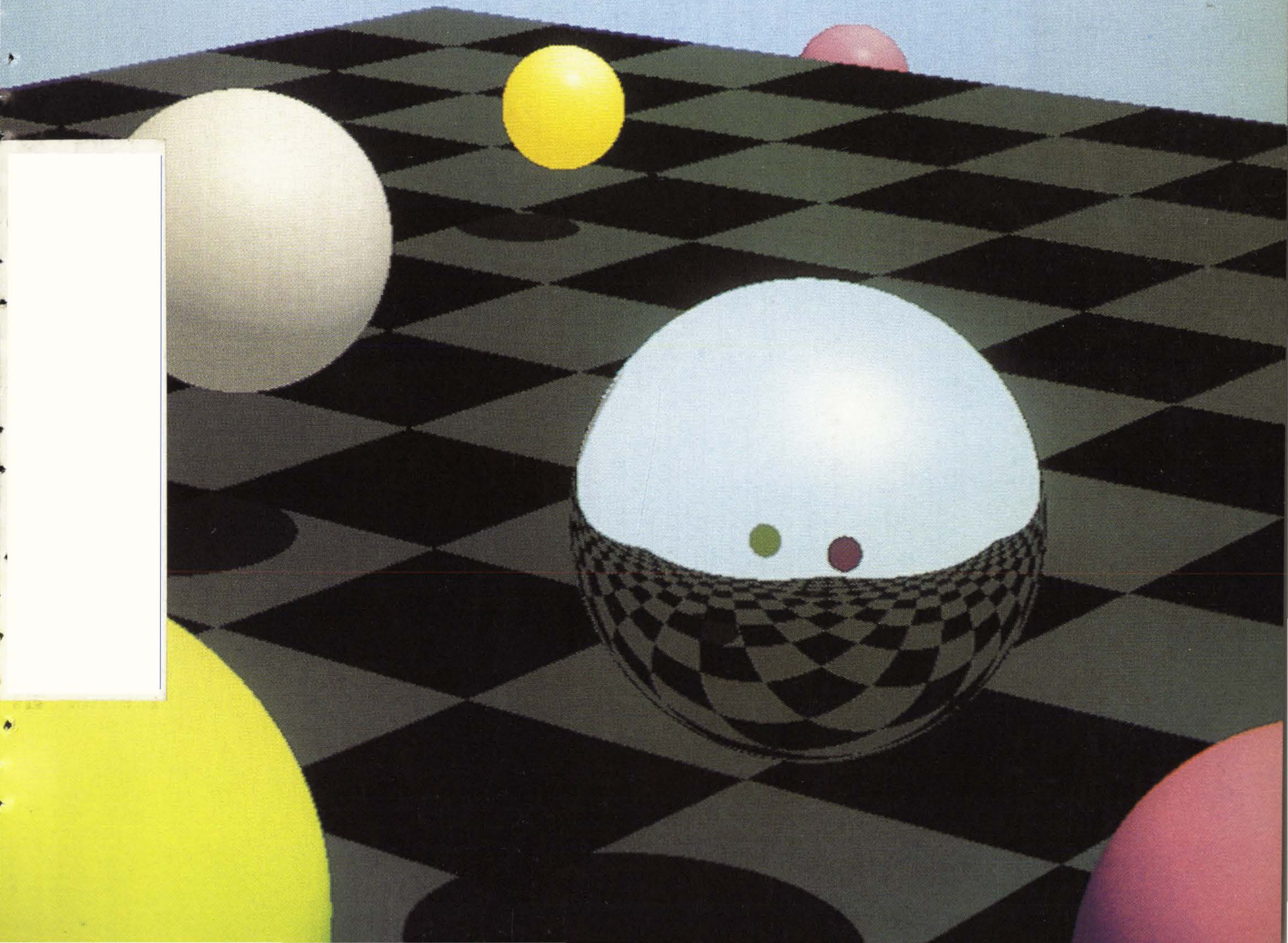


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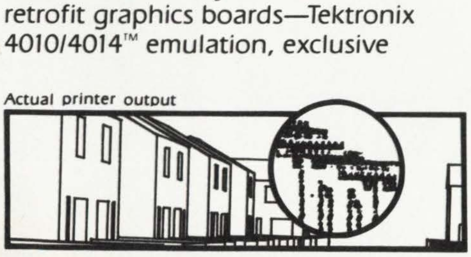
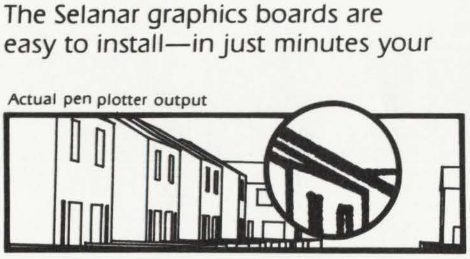


Actual pen plotter output



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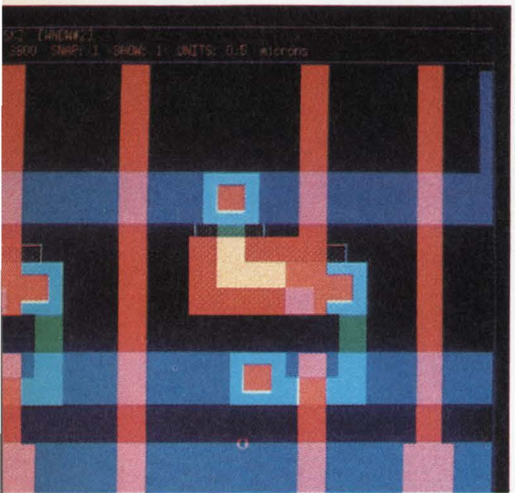

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DEPARTMENTS

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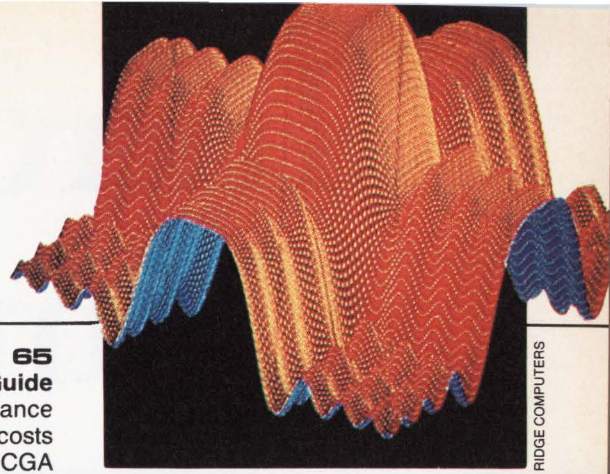
RIDGE COMPUTERS

FEATURES

ON THE COVER

This static synthetic image highlights several features of the Tektronix 4115B display terminal. The 1280 × 1024 resolution allows complex static images to be rendered without anti-aliasing techniques. The terminal's color pallette of 16 million colors permits subtle gradations of color shading. This image was created in a pixel viewport measuring 800 by 1024 pixels. Thirty nine colors were used in the sky, its reflection, and the light source; 8 colors were used in the floor shadows and reflections; 50 colors were used for each different colored sphere. Tektronix, Wilsonville, OR

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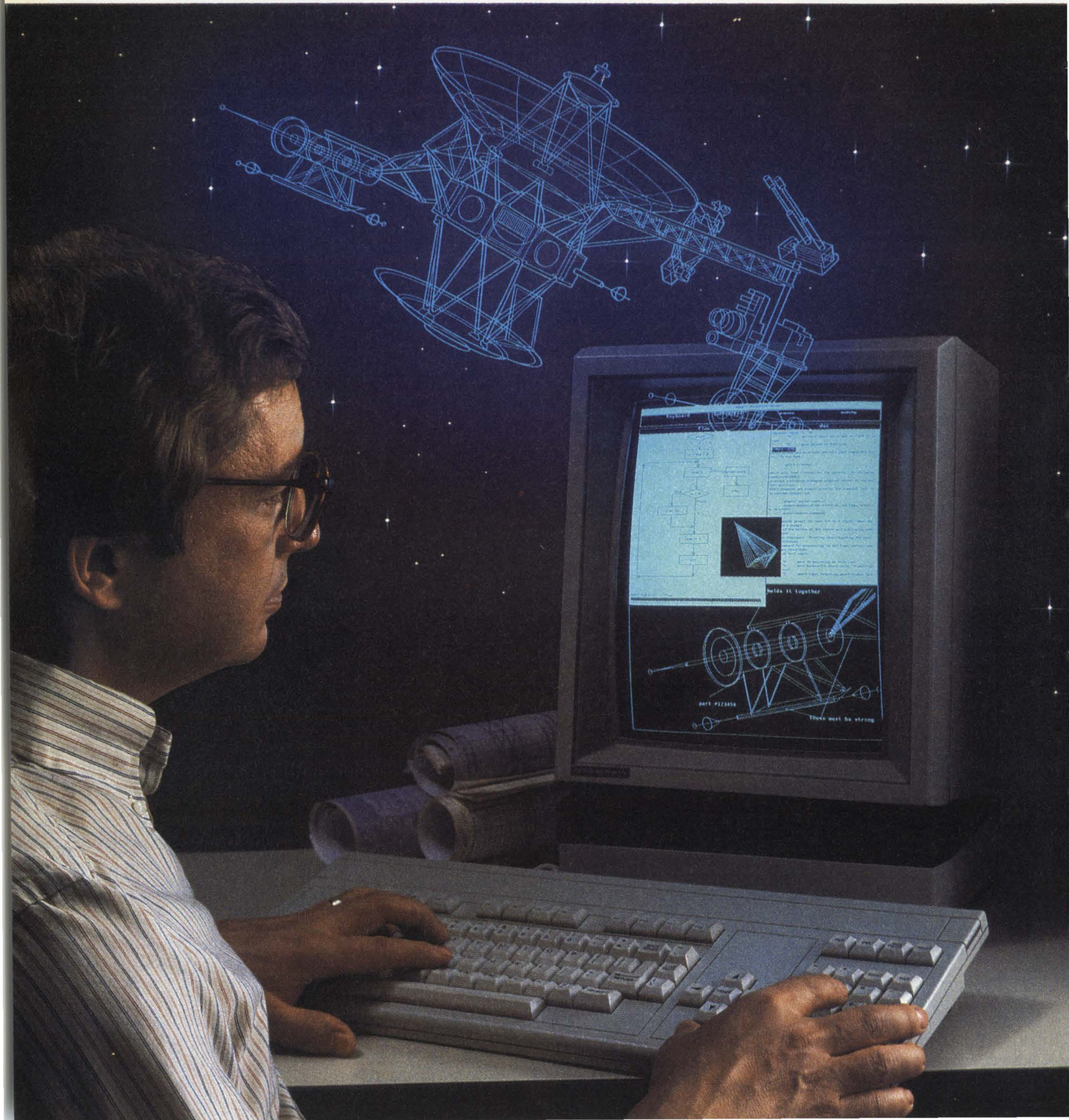

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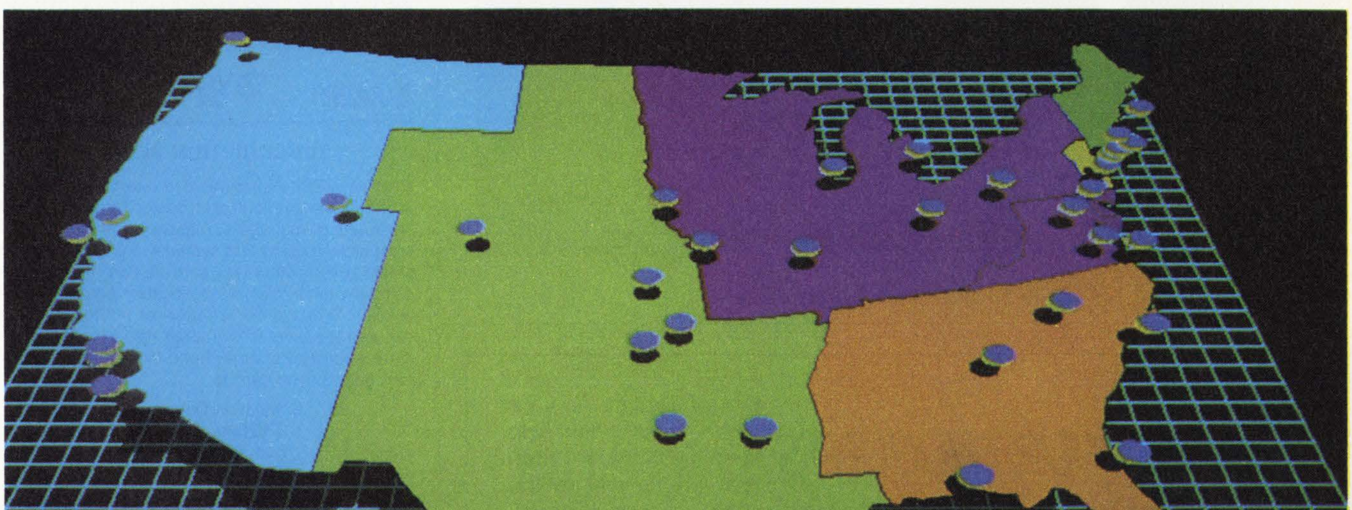

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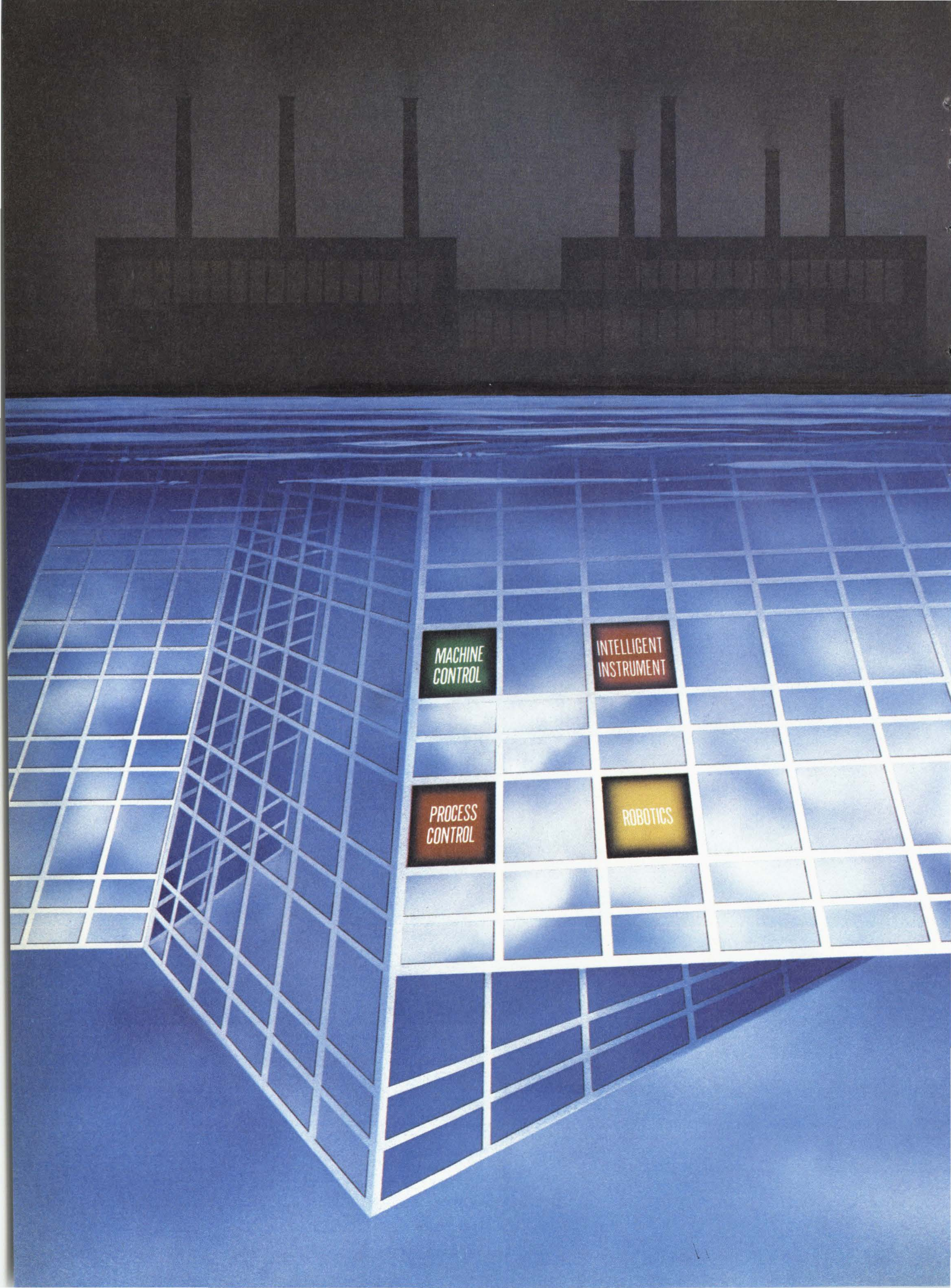
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'Vendors of general-purpose workstations are poised to not only absorb the growth of new marketplaces — such as VLSI design — but to acquire graphics capabilities as well.'

EDITOR'S COMMENT

The summer of 1984 will demonstrate a maturing unrivaled in recent history for a set of technologies – the areas that make up graphics. The annual conferences and conventions of the National Computer Graphics Association, the IEEE's Design Automation show and the ACM's SIGGRAPH will each show a lessening number of manufacturers in competition, but an increased sophistication of design and integration applied in the products.

Two perceptions of computer graphics technology prevail. From the point of view of many users and integrators, graphics technology is today more accessible. From the perspective of graphic systems designers, the architecture of display generation systems continues to face all of the problems of a general computer system while pushing the state of the art in subsystem areas.

Only 15 years ago, the basic algorithms for graphic interaction, picture generation and rendering were just being developed. Today's systems are implementing much of this work as user selectable functions, provided in firmware. This enhanced functionality is further improved by semiconductor advances in CMOS, RAM, semi-custom and processors.

As the secondary level users and manufacturers, represented at the Design Automation show, obtain these silicon and software tools, they contribute to systems that reduce the time to develop a new generation of technology. These more powerful devices in turn offer the programmers and researchers represented at SIGGRAPH a means of developing even more sophisticated tools and algorithms. The overall effect is cyclical, creating an environment of constantly changing and improving technology.

The pace of this change has dictated that graphic system manufacturers dedicate a greater portion of their resources to the study of design and developments in technology than in attempts to develop application-related systems. This focus may be witnessed in all levels of systems: terminals, hard copy peripherals, graphic display systems and turnkey workstations.

Terminals being demonstrated now often have computational capabilities that rival minicomputers. Despite such improvement, prices for terminals have become surprisingly low – often under $5000. To provide users with materials commensurate with the quality of the displays they create, hard copy devices must keep pace. Graphics manufacturers are at the forefront of developments in plotters, as well as ink jet, electrostatic and thermal printers. Today, the output of devices costing under $5000 rivals the quality of printed materials. At the highest levels of performance, graphic display systems are still costly, but functionality constantly improves.

Competition from systems based on open architectures forces graphic system manufacturers to be in constant product development. Display system manufacturers retain a competitive edge in many areas, but vendors of general-purpose workstations are poised not only to absorb the growth of new marketplaces – such as VLSI design – but to acquire graphics capabilities as well.

Perhaps the most encouraging events evident for the systems integrator at the graphics shows has been the progress towards software and device standards that promote device independence. Standards also allow the user to take advantage of greater system functionality without costly graphics subroutines or device drivers. Such changes allow designers to look on graphic capabilities not only as tools for specific applications, but as options available for other system functions, as are peripherals and software. Moreover, systems developers are able to concentrate on their own areas of technical expertise by purchasing graphics capabilities as subsystems. All of this indicates that graphics are being put to meaningful use rather than as experimental performance features.

The most important product of this summer's events, however, are more subtle and relate to future developments for next generation architectures and applications. Sprinkled throughout the papers and exhibits of these shows are systems, software and individuals who already espouse the basic technologies of knowledge data bases, natural language access, machine vision and artificial intelligence. Graphics advances and improvements in VLSI design exhibited here are indicators of the slow but very real progress towards the next generation.

Jerry Borrell, Editor-in-Chief

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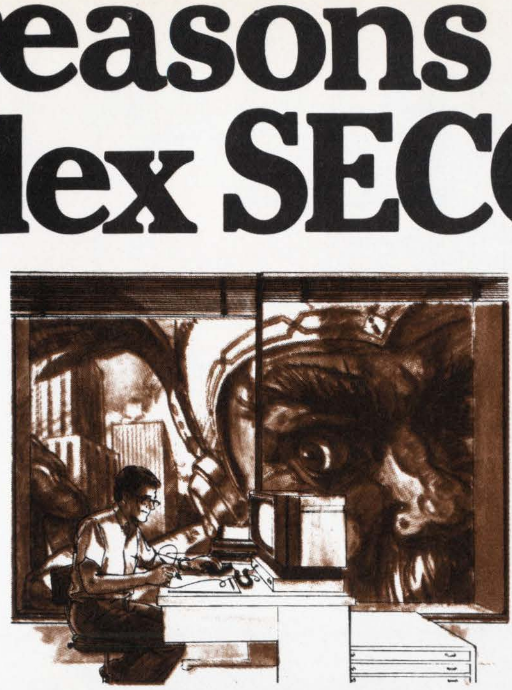

(No wonder "Big Brother" is watching us!)

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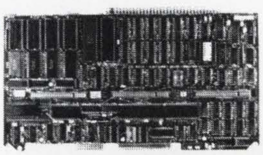

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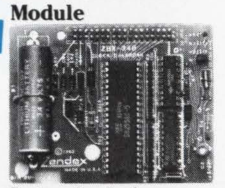

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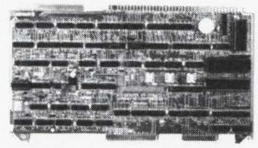

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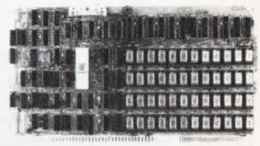

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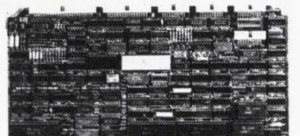

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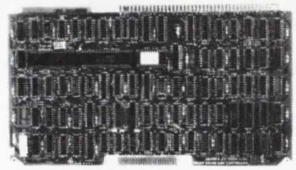

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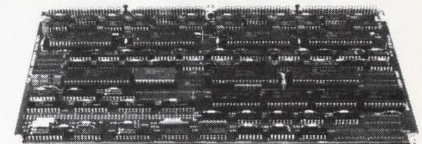

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*From now until May 31, 1984 our $42,000 CX 1500-01 Colorgraphic Engine™ is being offered for $19,995 complete. Includes engine, monitor, keyboard, graphics executive software. Act Fast . . . Limited Offer . . . One Per Customer.

Child's Play.

Complex pictures. Beautifully produced on screen. Easily controlled and manipulated.

For the D-SCAN GR-1104, it's child's play. Because this is the compact desktop terminal that thinks it costs twice what it does. And acts that way.

Picture this. A 60Hz non-interlaced 14" display. Bright. Stable. And flicker-free. With 1024 x 780 resolution!

But that's just the beginning. The 1104 lets you display 8 colors from a palette of 512 (not the usual 64). And lets you expand display list memory to a full 512K!

All of which means someone is going to be very happy. Visual cueing is better. And picture manipulation is localized. Which, of course, makes operators faster and more productive. And mainframes less burdened. Two cost-efficiencies every company can live with.

The 1104 will even support ANSI 3.64. And give you a VT100 keyboard (with 16 function keys). So there are no re-learning curves to finance.

What's more, the 1104 is Plot 10 compatible. Which means it can emulate the TEK 401X instruction set. And you can save a lot of time and money on software development.

Now for some impressive technology.

The 1104 uses four (not the usual one) graphic display controllers. So figures are drawn, filled and manipulated faster. There's no drag on the system caused by processor or memory overload.

Next, the video formatter is our own custom-LSI design. A gate array (2000 gates) that reduces power consumption and board space. And provides the video speed necessary for output to our high resolution display.

Which, we hasten to add, is beautiful. Especially with its .31mm pitch shadow mask. And contrast enhancement filter that eliminates screen glare and improves visual acuity.

You'll also be happy to note that the 1104 supports our Graphics Tablets (there are two) and Color Hard Copier (the one that's already taking the industry by storm).

One last item. Because we design, build, sell and service all of our products, you can count on getting the back-up you need. Direct service from 13 offices across the U.S.

So make life easy on yourself. Call today to get the full GR-1104 picture. It's easy. Just call your local Seiko Instruments sales person, or us at (408) 943-9100, or write 1623 Buckeye Drive, Milpitas, CA 95035.

You'll see that getting better resolution from a more user-friendly terminal, for a lot less money, really is child's play.

SEIKO
INSTRUMENTS

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Computers can not only add and subtract. They can divide.

RACAL

To shorten your electronic design times, you can provide your project teams with Computer-aided Engineering, Design and Manufacturing systems. And those systems will do their individual jobs very well.

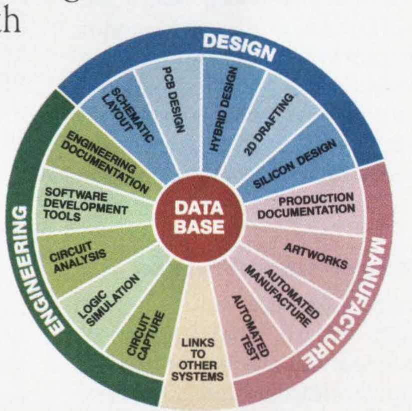
However.

As soon as you try to transfer the data generated by your engineers to the design stage (not to mention manufacturing) you'll find you have a problem. Because none of the systems are fully compatible with each other. Engineering can't get along with Design. Design can't get along with Manufacturing. And vice versa. Worse still, when the systems can't get along, neither can the people using them. So instead of state-of-the-art, you end up with something akin to a state of war.

The solution, of course, is to work with one company that can handle the entire project from beginning to end. A company with a full range of modular systems for every stage of every electronic design project. All fully integrated around a common data base.

That company is Racal-Redac.

With Racal-Redac, you can solve today's problems without creating new problems for yourself tomorrow. Because all the system modules were designed to work together, and grow with you as your needs grow.



Finally, a totally integrated capability for electronics.

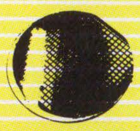
Read that last paragraph again. We at Racal-Redac are talking about a range of complete, totally integrated systems which work for you through every stage of the design cycle.

Only unlike other companies, what we're talking about isn't a vague promise for the future. Racal-Redac systems are already hard at work right now in over 1,000 electronics companies around the world. Any one of which we will be happy to discuss in considerable detail.

Just clip your business card to this ad. Or write. Or call. But don't wait for someone else to work it out. Because the alternative to integration is disintegration.

RACAL-REDAC
Linking Concept to Product
Lyberty Way, Westford, MA 01886 (617) 692-4900

Wafer Technology Expands



National Semiconductor Corp. will begin producing four-, five- and six-inch semiconductor wafers at what the company believes will be the world's first large-scale production facility of its kind. The $150 million plant expansion at Greenock, Scotland, will make National Semiconductor the only manufacturer of six-inch wafers in Europe.

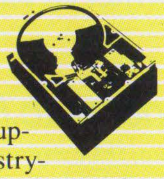
Second-Sourcing the 80186

Intel is completing the transfer of the manufacturing tooling for its 80186 microprocessor to Advanced Micro Devices (AMD). AMD plans to have samples of the part available in the third quarter of 1984, and be in volume production in the fourth quarter. Intel is increasing 186 production 10 times faster than for any previous Intel microprocessor.

$1 Million From Amtrak

CalComp recently received a $1 million order from Amtrak, America's nationwide passenger rail service, for two IGS 500 computer-aided design (CAD) systems to perform a variety of engineering and corporate applications. The CAD systems will be used in various electrical, mechanical, structural and civil engineering projects as well as in architectural applications and facilities planning and management. The systems will also be used to design railroad tracks and equipment.

ESDI Interface Support

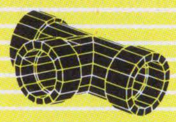


Control Data Corporation and Xebec (San Jose, CA) will increase their support of the disk industry-defined Enhanced Small Device Interface (ESDI) for 5.25- inch Winchester disk drives through a cooperative agreement in design verification, product qualification, and parallel development and production scheduling. Xebec will supply disk controllers with SCSI/ESDI interfaces and compatible ESDI drives from Control Data.

RAM Venture

VLSI Technology, Inc., (VTI), in a joint development venture with VISIC, Inc., (a San Jose startup), will work jointly to enhance VTI's design software for new memory product design and to develop process technologies using VTI's wafer fabrication facility. VISIC will concentrate primarily on the product design and market development of new high density, high performance sub-two-micron RAM circuits.

Prime Buys Medusa



In an agreement with Computervision, Inc., Prime Computer will purchase from Computervision joint ownership of Revision Four of the Medusa® mechanical drafting, design and three-dimensional solids modeling software package. As of June 1, 1984, both companies will be able to market Medusa software worldwide. The Medusa software was developed by Cambridge Interactive Systems Limited (CIS) of Cambridge, England, which was acquired by Computervision in 1983. Currently, and until June 1, 1984, the Medusa software is being marketed in Europe on an exclusive basis by Computervision/CIS and in the United States and outside of Europe on an exclusive basis by Prime.

TI Licenses NUBUS

Under an agreement with Massachusetts Institute of Technology (MIT), the Data Systems Group of Texas Instruments is now licensing its 32-bit NuBus™ technology to commercial and non-commercial users. Designed at MIT, NuBus is a 10MHz synchronous 32-bit bus.

Quality Micro Systems And Xerox Sign

Quality Micro Systems, Inc. and the Printing Systems Division of Xerox signed a $1.2 million contract for the purchase of QMS Wedgebox interface units. The WedgeBox is a stand-alone printer interface/controller capable of connecting printers to many host computers. Xerox will use the WedgeBox units to interface the Xerox 2700 printers to mainframes.

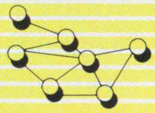
VLSI For AT&T

Rockwell International announced an agreement with AT&T Information Systems to develop and manufacture VLSI devices for AT&T Information Systems' Digital Multiplexed Interface. The Digital Multiplexed Interface (DMI) provides a high-speed, multi-channel digital data link between AT&T Information Systems' DIMENSION® System 85 and the computer and communications systems of other vendors.

Restrictions On DEC

In the wake of several highly publicized seizures of computer equipment on its way to Eastern bloc nations, the Commerce Dept. is now requiring Digital Equipment Corp. to get individual export licenses from the department before it can ship any of its computers to West Germany, Norway or Austria—three countries considered prime diversion points for smuggling computers to the communist bloc. DEC is the only company currently operating under such tight restrictions, but several others have their general export licenses up for renewal in the near future.

Motorola UNIX Approved



AT&T, originator of the UNIX Operating System, has validated Motorola's SYSTEM V/68 Operating System, which is the first UNIX port developed jointly with an outside source. Validation of the SYSTEM V/68 Operating System, developed in agreement with AT&T by Motorola for the MC68000 family of microprocessors, signifies the operating system is a faithful, functional equivalent to the UNIX System V product developed for minicomputer environments.

Fault-Tolerant Contract

Stratus Computer (Natick, MA) has received a contract from Lockheed Electronics Company for a network of fault-tolerant computers which will have a total value of $2.5 million when fully exercised over the next two years. Lockheed was recently selected to modernize and automate the Republic of China's air traffic control system and will incorporate a distributed network of a dozen Stratus/32 Continuous Processing Systems.

OUR MICRO/11 STANDS ALONE FOR ITS AVAILABILITY AND CAPABILITY

You know about the advantages of a Micro/11 computer system. What you may not know is that it's available now. Our MDB Micro/11 is functionally equivalent to the DEC Micro/PDP-11* providing an 11/23 Plus, 256KB RAM, 10.4 MB Winchester and 1 MB Dual Floppy sub-system. But there's more.

This low-cost, compact and highly flexible work station provides the exclusive feature of being software driver and media compatible to the RX02. This unique capability allows diskette transfer to and from other DEC systems. Also, unlike the DEC unit, our Winchester is RL02 software compatible. Even optional 20 MB RL02 or RP02 emulating Winchesters are available to enhance your system.

When it comes to interface modules, however, the MDB Micro/11 has lots of company. The system, with its 8 quad slot (16 dual slot), Q-22 backplane and its rear distribution panel, accommodates all of MDB's unequalled repertoire of FCC compliant Q-bus controllers and interfaces. They include multiplexors, line printer controllers, disk and tape controllers, high speed DMA modules and interprocessor-links.

As for price, we won't hold you up there either. Single units cost only $7,800 and substantial discounts are available for quantity purchases.

So why wait? It's all available now. Start by contacting us today. You won't be alone.

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Write 5 for Q-Bus   Write 6 for Micro/11

WASHINGTON REPORT

by Anne Armstrong

Standards Policy For Tactical Computers

In the face of the continued objections from both Congress and industry, the Department of Defense is reworking its plan to standardize the tactical computers used in weapons systems. Last year DOD drafted its controversial Directive 5000.5X, which was designed to stop proliferation of many new hardware and software systems by narrowing the list of acceptable tactical computer architectures. Opponents of the directive argued that such a policy would lock out new manufacturers and stifle competition.

In a conciliatory mood, DOD has prepared a new alternative for Congressional consideration – the creation of a task force to work with industry to draft interface standards for the next generation of tactical computers. To be called the Computer Systems Interface Working Group, the task force will work with a comparable industry committee. Observers expect the project will take at least one year.

The idea behind the new defense policy is to use commercial standards as much as possible – and DOD wants to be able to obtain tactical computers from several manufacturers and not be locked in to one vendor.

Until the new interface standards are written, the department plans to combine standards temporarily and use the Air Force Mil Std 1750A for 16-bit computers used in avionics and the Army Mil-Std 1862 for 32-bit computers used in weapons systems.

As an added incentive to both the services and to industry to get new standards in place, DOD set termination dates for existing tactical processors. After 1990, for example, Sperry Corp.'s new Navy AN/UYK-43 and AN/UYK-44 computers won't be accepted in any new weapons systems. And the new airborne computer, which both Sperry and Control Data are competing for won't be included in any program starts after 1989.

The new policy to limit the different computer designs which DOD must deal with also applies to the microcomputers. Micros must have competitive sources of supply for their basic processors and memory devices. And DOD wants to establish standard communications interfaces allowing micros from different manufacturers to talk with each other.

The new DOD policy also touches on the need for standardized software. ADA, Defense's high-level language, was specifically designed to solve the Tower of Babel problem in Defense computers but its implementation has not been as rapid as expected. DOD is reaffirming its commitment to ADA as a standard by identifying some of the weapons systems that will use the language.

Among the systems that use ADA are the Air Force's World Wide Military Command and Control System, the Navy's Submarine Command System, its Ocean Surveillance System and its multiple Launch Rocket System.

Export Control Battle

One of the current battles being fought in Washington is the Export Administration Act. Major players in the administration have taken opposite points of view on big issues, and amendments have been tacked on that cover everything from bank loans for South Africa to nuclear equipment in India. The legislation is important to the computer industry because it establishes the rules for the whole export licensing system and designates which government agency will review requests to export computer and other high technology equipment.

In the past, the Export Administration Act has been used for such wide ranging applications as cutting off sales of wheat to Russia and for stopping computer shipments to the Eastern Bloc. Many segments of industry have a vested interest in various bills that are designed to replace the old Export law that expired last fall. When Congress realized that it could not agree on legislation, it extended the old legislation until May 31. And it may have to do the same thing again because although both the House and Senate have passed versions of a new export bill, they show no signs of agreement on key issues.

The Senate version of the export bill gives the Department of Defense greater review authority over export license approval and the power to reject any export license request that could, in the opinion of the Secretary of Defense, involve a threat to U.S. security. The Senate bill also transfers enforcement of export violations from the Commerce Department's Office of Export Administration to the U.S. Customs Service. It retains, however, the General Distribution License which is widely used in industry to ship controlled products to free world countries.

The House version is significantly less stringent and is generally viewed as more favorable to the entire export industry. The Computer and Business Equipment Manufacturers Association (CBEMA) strongly prefers the "normal license procedure" outlined in the House bill. The Commerce Department is also backing the House bill – no doubt because it would retain its enforcement unit.

Computer firms and trade associations have spent enormous time and energy trying to change the restrictive export regulations procedure, but a long battle seems to be in store over the export bill. Unless one house has a change of heart about compromising, extensions of the old law may be all that is possible before the fall elections.

Electronic Data Systems Wins Navy Deal

After two and a half years of bidding, an Electronic Data Systems (Dallas, TX) team beat out Honeywell Information Systems in benchmark tests and won a contract to supply the Navy with computers and software for its $350 million Inventory Control Points project. As part of the contract award, IBM will supply as many as 15 3081 mainframes and up to 54 small computers as part of the eight-year project.

Reduced Tariffs On Semiconductors Exported To Japan

A bill authorizing the Reagan Administration to negotiate the reduction of tariffs on semiconductors exported to Japan is expected to pass both houses of Congress without difficulty. The recommendation to reduce tariffs was made last year and has been agreed to by both the Japanese and U.S. authorities and is supported by industry trade associations.

The fastest...the largest memories... the easiest to program...

MARS-432 Array Processor Speed
A high-speed programmable arithmetic processor used as a peripheral to a general purpose computer.

MARS-432 Array Processor Memories
Program and data memories compatible with programs written for today's array processor applications.

MARS-432 Array Processor Software
An architecture specifically designed to support a FORTRAN compiler and other software development tools.

The state of the art in 32-bit floating point array processors. Direct addressability of up to 16 million words (64 megabytes) of data memory and direct access to the high-speed internal data bus assure the user of highest throughput rates.

MARS-432 Array Processor Features Include:

- Add and multiply times of 100ns
- Computational power of 30 megaflops
- Computes a 1024-point complex FFT in 1.7ms
- DMA transfers at I/O bus rates of 20 megabytes/sec
- Data memory read or write in 100 ns
- Memory paging for uninterrupted processing during I/O transactions.

Program Memory
Virtual and physical address space of 4K words – standard. Expanded configuration uses a 4K cache memory to extend total memory to 64K words.

Data Memory
Data I/O is supported by DMA transfers into data memory with a physical address space of 16 million words. A data memory page-loading feature provides the option of zero overhead background loading of data during time critical program execution. No DMA cycle stealing overhead is incurred. Uninterrupted processing can occur simultaneously with high-speed I/O transfers.

FORTRAN Development System (FDS)
FORTRAN compiler, linker, and trace/monitor provide high-level language access to the MARS-432.

Microcode Development System
Off-line development package includes macro-assembler, microcode diagnostics, and a unique utility for automatic microcode optimization.

AP Run Time Executive Support Package (AREX)
As the interface to the MARS-432 at run time, AREX provides processor initialization, I/O operations, and array function execution.

Applications Libraries
Extensive applications libraries include math, signal processing, and image processing.

NUMERIX

For additional information on the MARS family of high-speed Array Processors, write or call:
Numerix Corp., 320 Needham Street, Newton, MA 02161 Tel. 617-964-2500 TELEX 948032

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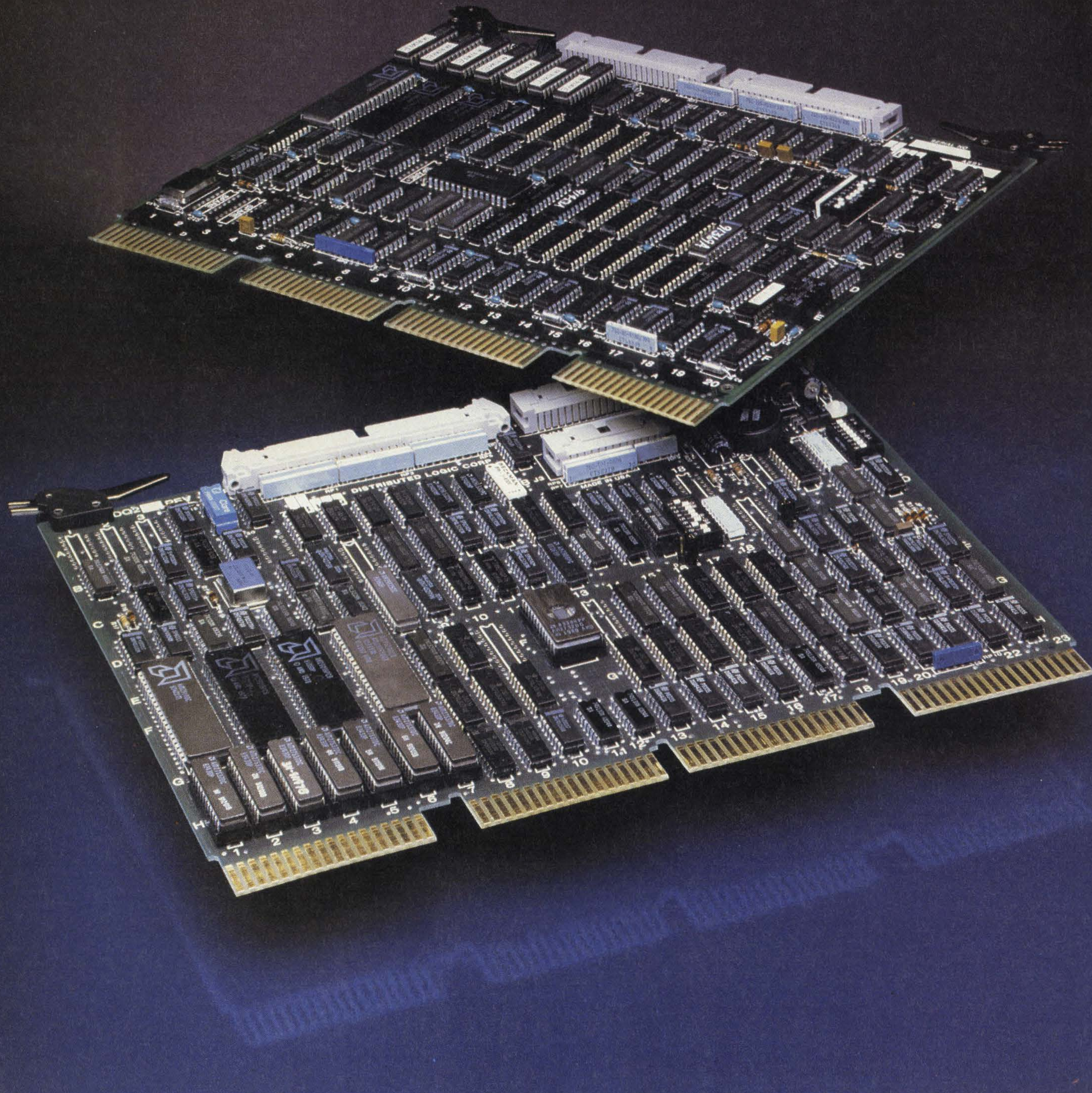
THE BETTER CONTROLLERS



AND FOR GOOD REASONS.

NO OTHER SMD OR ½″ TAPE CONTROLLERS MATCH THEM.

First, they're an economical, high performance pair you can "rack and stack yourself." Or you can get them from your nearby DILOG distributor in a completely supported subsystem package. In either case, they let you interface the RM02/RM05/RM80 emulating 8″ and 14″ Winchester drive(s) and back up with the TS-11/TSV05/TU-80 emulating ½″ tape drive(s) of your choice.

The hard disk controller, Model DQ228, handles one or two 8″ or 14″ SMD I/O drives. And because it has DILOG's exclusive Universal Formatting,™ you can mix or match drives, so long as they have the same I/O. Simply unplug one and plug in another. You get a choice of RSX-11 or RSTS operating systems. The controller also includes 56-bit ECC for accurate error detection, 22-bit addressing for speedy 4-MB access of memory and time saving 2-MB transfer rate.

The Model DQ132, is a ½″ Magnetic Tape Coupler offering you interface of up to four formatted industry standard I/O (Pertec formatted) or streamer/"CacheTape" transports. You get a choice of RT-11, RSX-11 and RSTS. It likewise offers 22-bit addressing for 4-megabyte access of memory and is GCR compatible supporting 600 KB transfer rate.

For complete data on these better controllers, contact the factory or the distributors listed below.

DILOG

DISTRIBUTED LOGIC CORPORATION

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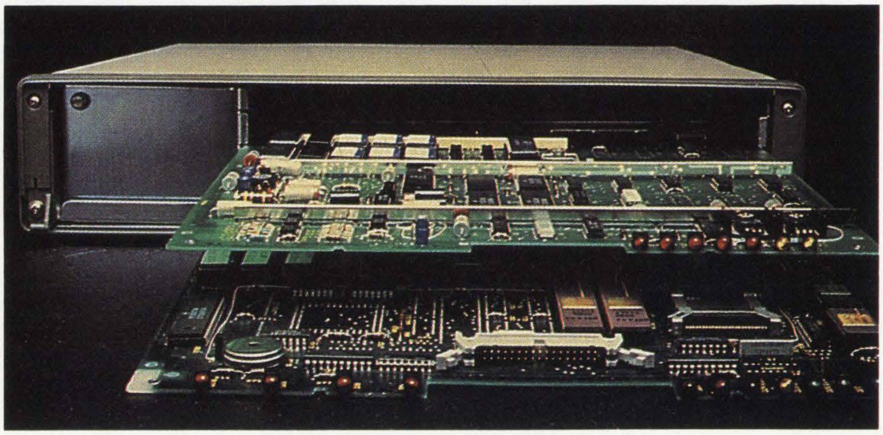
Modems Aid Network Management



Codex 2600 modems are built around the MC68000.

More equipment is being networked in both the LAN and wider areas, making for good intercommunications, but also a monumental task in network management and control. Traditionally a large manufacturer of modems and multiplexers, Codex (Mansfield, MA) has not only added three modems under MC68000 control and two new statistical multiplexers to its line but also a local area network (LAN).

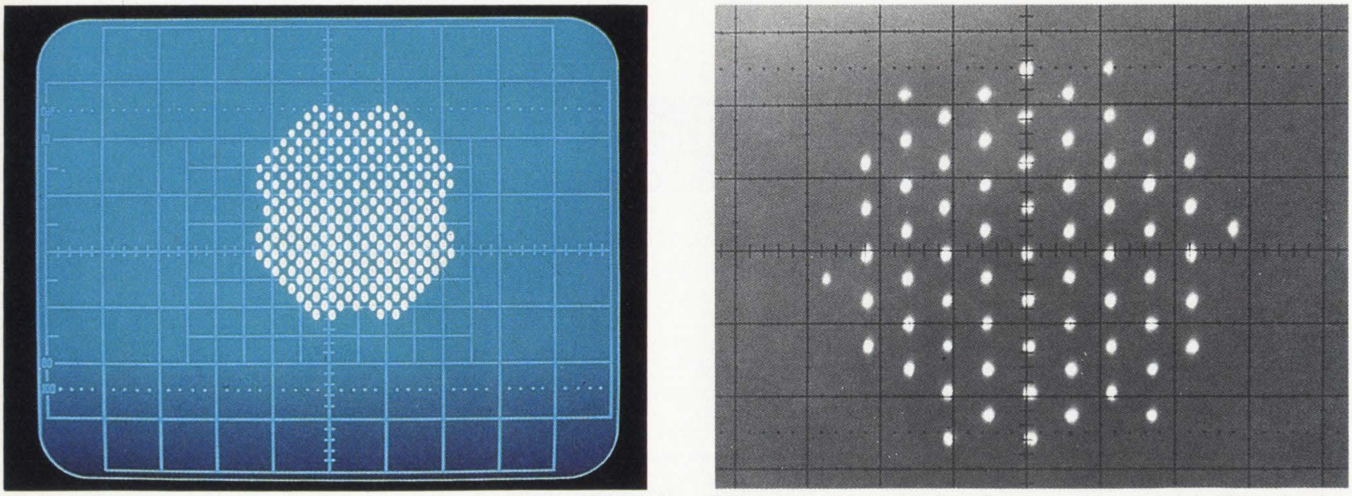
Of all of these introductions, the new modems are perhaps the most innovative, though the product type is oldest. The 2600 Series "network system resource" modems used a proprietary backplane bus under the control of an MC68000. Three new chips, also manufactured by Motorola, Codex's parent, are on the VLSI Signal Processor board, including a 100-pin HMOS signal processor.

Other slots in the four-space backplane can hold a four or six channel buffered multiplexer, dual dial restoral for dial operation in the event of leased line failure. An extender module that allows program downloading to add functionality from a remote network controller is included.

The top-of-the-line 2660 is the first commercial modem to use Trellis Coded Modulation (TCM), for speeds up to 16,800 bits per second. Current QAM (Quadrature Amplitude Modulation) produces high error rates at these speeds, and uses forward error correction coding to improve error rates over channels with a limited signal-to-noise ratio (SNR). But TCM provides the improved error rates without a penalty in increased bandwidth for checking overhead. Codex says that TCM's eight-state redundant transmission scheme gives it a 3 dB advantage against noise as compared to QAM, for performance two orders of magnitude better than other modems at 14,400 bps.

Operation at 16,800 bits/sec will stretch all but the best quality lines. So to keep error rates low at maximum data rates, the 2660 uses an adaptive rate system (ARS) that automatically switches from 16,800 to 14,400 or 9600 bits/sec when line conditions degrade. As conditions improve again, speed is automatically stepped back up, for maximum speed at all times without increasing error rates. The other 2600 series products are also under MC68000 control and operate at 9600 and 4800 bps, with the same VLSI architecture but conventional modulation. These two support multipoint as well as point-to-point transmission in several modes, including CS 48FP and CCITT standards V/29 and V.27 *bis*.

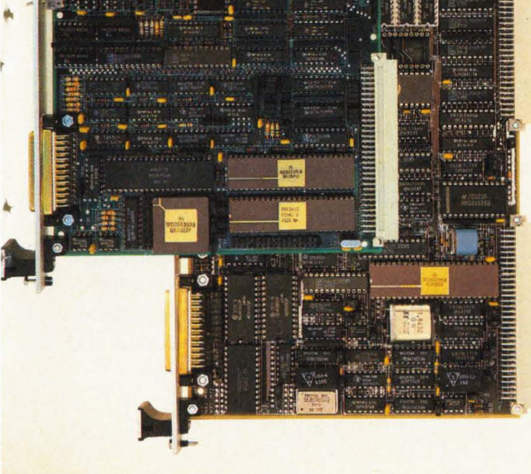
Two statistical multiplexers were added to the Intelligent Network Processor line at Interface, as well. One, the 6002 can handle up to 16 asynchronous devices. Its software strapping permits a mix of manufacturers' equipment and transmission speeds of up to 19.2 Kbps to be multiplexed, as well as changes for future needs or special flow control schemes. For large networks, a 124-channel mux, the 6035, can be used in ring, star or other network topologies for both synchronous and asynchronous transmission. The network monitoring, local and remote diagnostics and network config-



A 14.4 Kbit/sec signal creates a 128-point eye pattern using TCM (left) and 68 points under a QAM modulation scheme (right). The redundant signal points of TCM allow dependency between successive signals, and error checking is against valid signal patterns.

VME ARENA CHAMPIONSHIP

IN THE VME ARENA FORCE PUTS MORE POINTS ON THE BOARD



OUR OFFENSIVE LINE: CPU-1, CPU-2, CPU-3* ALL VMEbus COMPATIBLE

128KB/512KB 68000 CPU-1 VMEbus Board
SYS68K/CPU-1
- On-board storage 128K/512K byte DRAM
- 128K bytes of EPROM
- 3 serial I/O ports plus 1 parallel I/O port
- Real time clock with battery back-up

256KB/1MB 68000 CPU-2 VMEbus Board
SYS68K/CPU-2
- Dual ported RAM 256K/1M byte
- 16K bytes of SRAM, 64K bytes of EPROM
- Floppy Disk Controller (5 1/4 ", SA 460)
- Multiprocessing, multimaster capability
- 1 serial multiprotocol plus 1 parallel port
- Real time clock and battery back-up capability

MMU-DMA 68000 CPU-3 VMEbus Board
SYS68K/CPU-3* (Preliminary Spec.)
- Memory Management Unit
- Direct Memory Access Controller
- 16K bytes of SRAM, 64K bytes of EPROM
- 4 level on-board bus arbiter
- Multiprotocol controller
- Real-time clock with battery back-up

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Other FORCE products of the SYS68K VMEbus family:
- Analog I/O boards
- Dynamic RAM boards
- Static RAM boards
- Floppy/Winchester controller
- SASI Interface with DMA capability
- Multiprotocol serial I/O board
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For further information please contact one of our distributors or representatives or FORCE Computers direct, the VMEbus specialist.

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uration capabilities necessary for such large networks can be distributed or centralized with this device.

As they round out their traditional lines, Codex is entering the local area network (LAN) market, as well. Their "general purpose LAN" is compatible with the Ungermann-Bass (Santa Clara, CA) Net/One version of Ethernet, using baseband, broadband or a hybrid of media with broadband trunks and baseband feeders. A network operating system (NOSS) provides virtual circuit, file transfer, datagram and other network services. In an unusual approach, this network will be available for lease, in addition to typical maintenance and installation services.

The LAN is first in the "4000 Series of internetworking and network management products," a hint that the LAN and phone line networks will soon be tied into a complete communications line by linking products. And such a complete datacomm line from a known firm, backed by Motorola, should be able to offer not just breadth, but further enhancements along the lines of 68000-based modem control.

— *Pingry*
Write 236

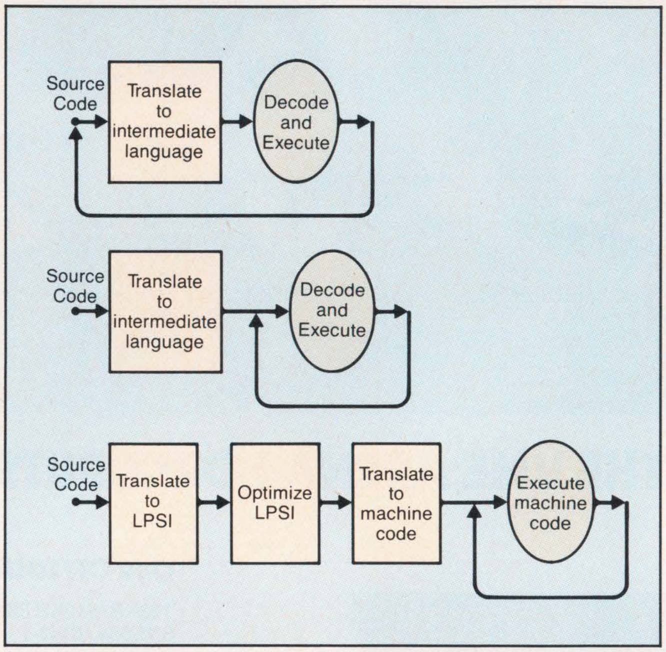
DEPARTMENTS/Software

New Compilers Based On Component Architecture

Aimed at computer manufacturers whose systems use the Motorola 68000 and the Unix operating system, Language Processors, Inc. (Waltham, MA) have introduced four compilers for COBOL, RPG-II, Pascal and C. The family uses LPIs Component Architecture that combines five standard subsystems — a front end, optimizer, code generator, run-time library, and high level debugger into a compiler.

One of the benefits of the Component Architecture is that portions of programs written in different languages may be mixed into a single program. The capability, that LPI has dubbed "Polyglot" also allows programmers to integrate portions of existing programs written in any LPI language into new programs, so they do not have to create and debug new code.

The front end of the compiler is language specific and a separate front-end exists for each language. It is, however, machine independent allowing it to be used with any microprocessor. The global optimizer analyzes each program statement, not only individually, but also in the context of the whole program. It optimizes the program by eliminating redundancies and other program inefficiencies, then generates code. The code generator is the element that tailors the LPI compilers to each type of microprocessor; because a new one must be created for each type of microprocessor, LPI developed a programming tool, called the code generator (CGG) which allows the company to generate the bulk of a code generator by describing the characteristics of the microprocessor for which it is being created.



Many language systems that actually are interpreters are mistakenly called compilers. A traditional interpreter, top, translates source code into an intermediate language, which is then decoded and executed. If that line is to be used again, the entire sequence is repeated, which adds considerable overhead and slows execution substantially. Some compilers translate source code into an intermediate language and store it. Subsequent executions do not have to be translated from source code to an intermediate language, saving a step and increasing performance somewhat. LPIs compilers translate source code into an intermediate language called LPSI. The LPSI code, which retains many of the characteristics of the source code, is optimized to eliminate inefficient statements or redundancies and compiled, during which it is translated into machine code and stored. Subsequent executions are in machine code, which can be executed at the speed of the machine's hardware.

Although more work must be done after the main body of the code generator has been created, the CGG has the effect of reducing the amount of work and shortening the design time usually involved with the software development.

The run time library creates the environment in which the program executes. It is common to all LPI languages, so its functions are identical throughout the compiler family. Largely machine independent, only about 25% needs to be rewritten when it is being adapted to a new microprocessor. To support LPIs Polyglot capability, a high level debugger interacts with the programmer in whatever language he is working, and eliminates the need to switch from one debugger to another when moving to different languages. To complement the range of compilers already available, LPI intends to announce LPI-PL/I this summer, and LPI-Basic by the end of the year.

— *Wilson*
Write 237

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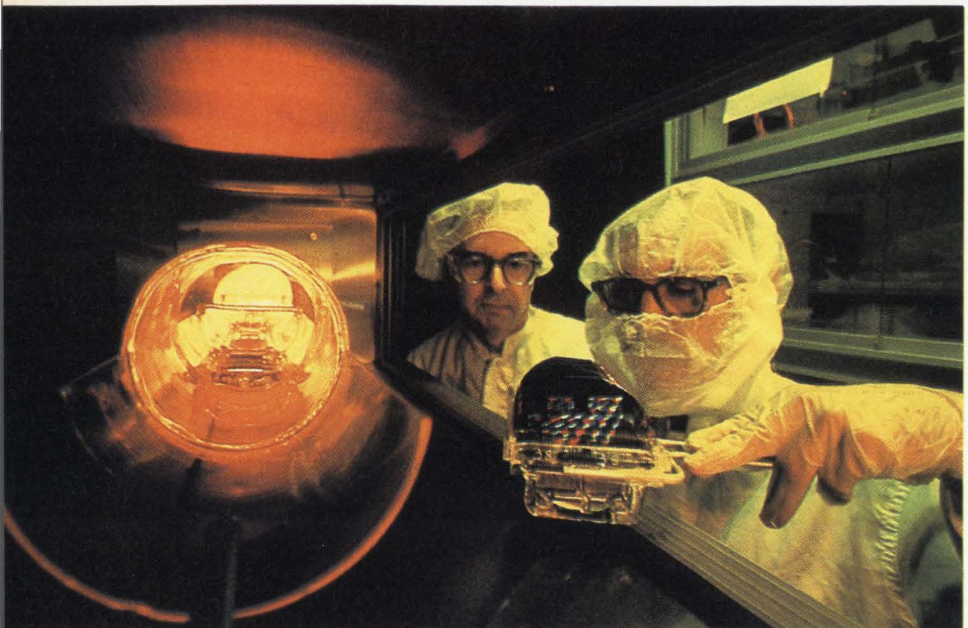
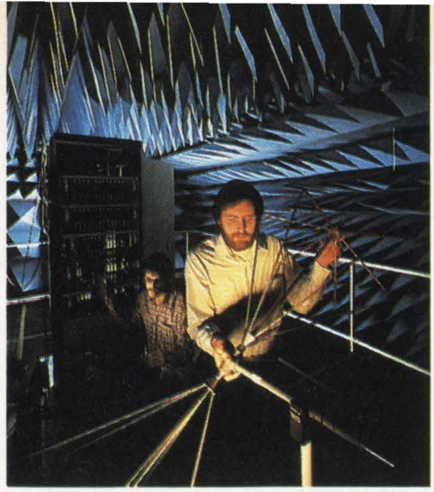
Restructuring At Bell Labs



A wafer of 85 265K RAM chips is inspected.



#5 ESS switches are tested in an anechoic chamber, or quiet room.

Since its founding in 1925, Bell Laboratories has developed some of the most important technologies and devices in electronics, including the transistor. Recently, there has been some discussion as to whether the Labs will still carry out enough pure research to produce new devices and technologies on the magnitude of the transistor. With the restructuring of AT&T, some 7000 people left the Labs; most were farmed out to the research divisions of now-separate companies, AT&T Communications and AT&T Information Systems (See chart). The 19,000 employees left make up the R&D team for the four other sectors of AT&T Technologies, a company that now describes itself as "extremely competitive and . . . basically unregulated."

The word from AT&T and the Labs is that basic research will continue to be extremely important and well-funded—but that research can no longer be open-ended. Indeed, the basic research budget will be roughly the same this year as last; the question is whether the new emphasis on competition in the market and producing products will change the researchers' ability to delve into untapped, unproven areas.

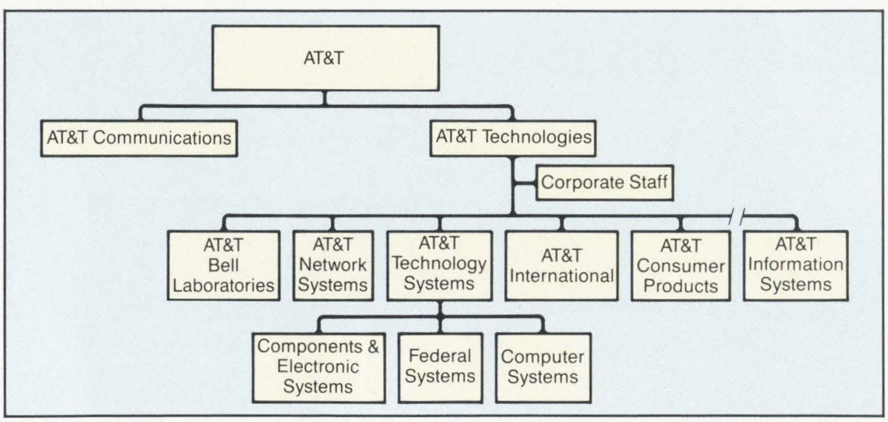
Now that AT&T Technologies is free to enter a variety of markets, developments from the Labs in areas not directly connected to telecommunications can finally be used commercially by the giant. Contrast this to the regulated entity it was, in a monolithic market, where Bell Labs technology was licensed to anyone. And for developments not in telecommunications, the license fees were the only money AT&T could make on the Labs' work. So it is possible that more areas of research will be encouraged by the parent, if they have promise for profit in any of the new "lines of business."

Bell Labs-developed technologies and hardware (as well as UNIX software) has recently hit the market in a new field, with AT&T's 3B computers. The breadth of this initial entry into the market shows an intention to compete in a big way in the new fields open to them, and it could be a bonus to the Labs' research that the parent needs new and better processes and devices to compete successfully. In addition to computers, new AT&T business areas, as shown by the company organization, include consumer products and components and electronic systems.

On an organizational level, the Labs will be affected by these business thrusts, and made more conscious of the competitive environment. One spokesman admits the Labs will be tighter, leaner and more end-product oriented. And that is only to be expected, since the parent is competing openly in many markets now.

AT&T has traditionally recognized the value of good basic research. Many of the projects from the Labs have been pure research originally and turned into highly successful products, both in the phone system and for licensees. AT&T now has the chance to capitalize on the work of one of the largest research organizations in the world. —*Pingry*

Write 232



Organizational chart of the new AT&T.

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Honeywell Links Process Control To Mainframes

Honeywell TDC 3000 process management system fully integrates process control and plant information.

The integration of process control data and plant management information ties the independent systems typically dedicated to areas such as process control, production, planning and data processing. Honeywell, Inc. has extended the technology of their TDC 2000 which, when introduced in 1975, was the first microprocessor-based, digital system for industrial process control, with the TDC 3000 linking process management systems to IBM 4300s.

The TDC 3000 includes integration elements such as distributed computing architectures, sophisticated communication capabilities and information-access concepts. Real-time process information acquired by TDC 3000 from sensors in the process units can be transmitted directly to an IBM 4300 for further manipulation and reporting.

A binary synchronous communications capability is implemented in the TDC 3000 computing module (CM60), a Honeywell DPS 6 computer. Through the bi-synchronous link, the CM60 appears to the 4300 as an IBM 2780/3780 workstation, a HASP multi-leaving workstation or a 3270 series Control Unit with display stations. With this capability, the CM60 could then be used to perform the averaging and formatting of process data for management review.

The SNA file transmission facility, also implemented in the CM60, will provide for the high-speed exchange of large volumes of data associated with process control. Typically, it would enable the user to quickly add process data to the management information data base. Both facilities can coexist in the CM60, making it easy for users of the binary synchronous link to migrate to SNA.

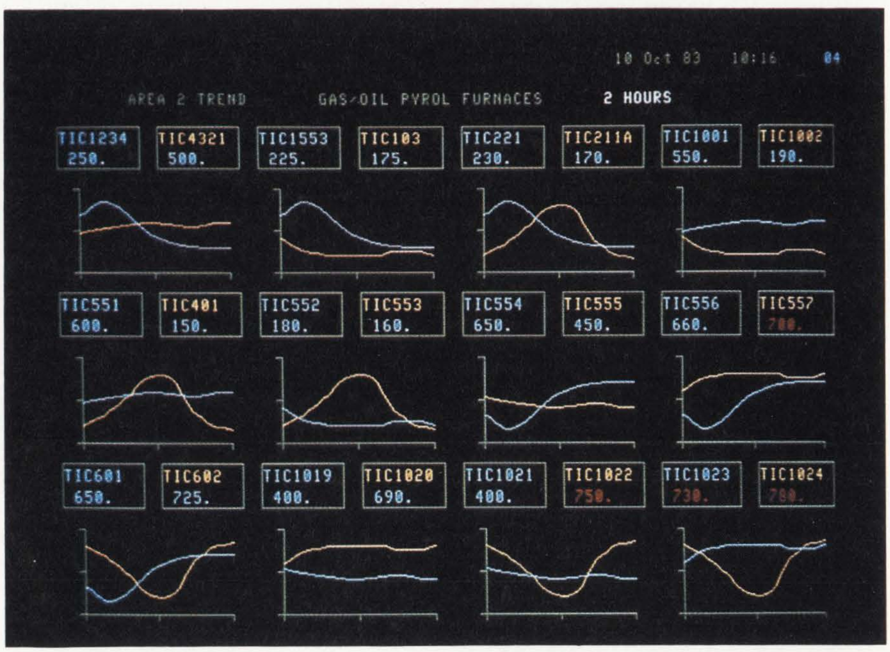
Distributed Computing Modules

In addition to the universal station, TDC 3000 includes modules that execute functions which, until now, had to be performed in a large, central computer. These modules can be expanded incrementally to meet the user's need for increased capacity. Redundancy improves their fault tolerance and, as a result, their reliability.

The history module provides process and event history, storage for additional schematic displays and general file storage. The module's flexibility permits historical data to be collected in different formats to meet user needs throughout the plant.

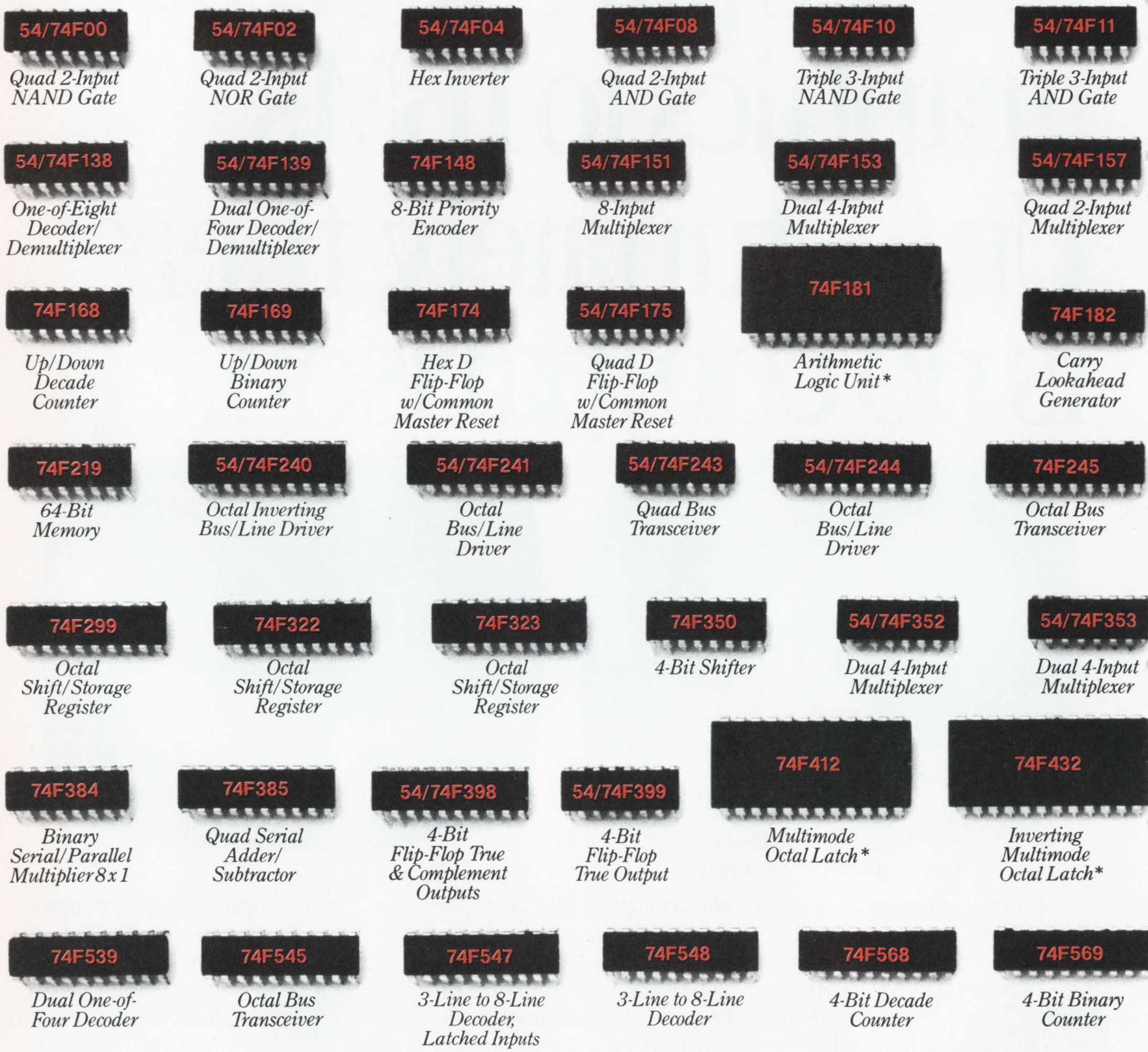
The application module stores and executes advanced control strategies. It also features a powerful control language for the programming of user-defined processing routines to replace or augment the pre-configured routines.

The computing module, which includes microprocessor-based devices as well as models of the Honeywell DPS 6 family, permits users to implement application pro-



Trend overview display of Honeywell TDC 3000 tracking 12 process groups of two variables.

84 FAST



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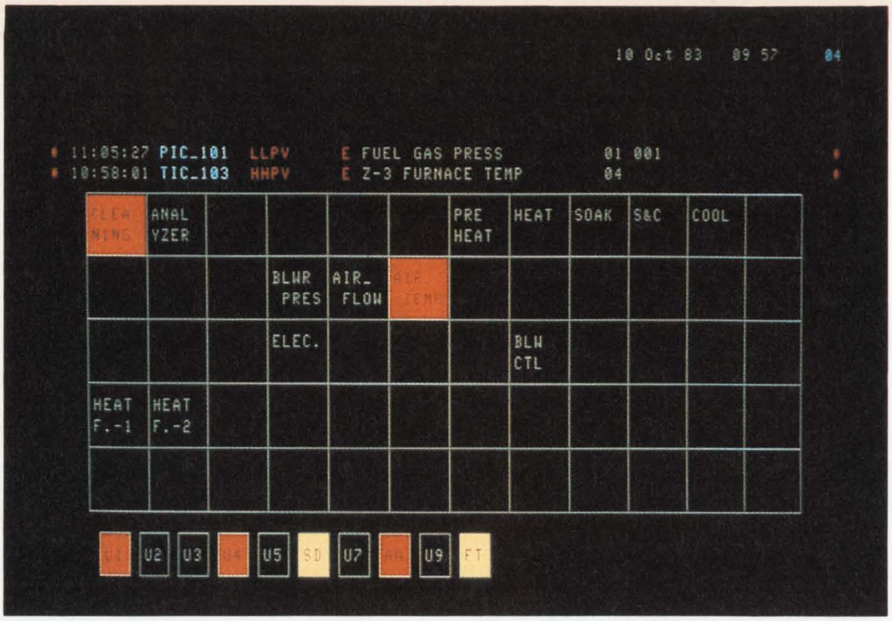
grams which exceed the scope of those available in the TDC 3000 application module. When a Honeywell DPS 6 is used, FORTRAN and Pascal user programming languages are available as well as facilities for advanced control and optimization. The DPS 6 also links TDC 3000 to global networks such as Honeywell's Distributed Systems Architecture (DSA) and other standard industry networks.

Gateways

TDC 3000 gateways serve as the link between the LCN and the Data Hiways and between the instrumentation subsystems and plant computers. Generally, they collect and convert process data into a common format, detect and report events and sequence data transmission to the LCN. The LCN in turn distributes data from each gateway to other modules and/or gateways.

System-Wide Advances

TDC 3000 features include a modular single software structure written in a high level language, industry-oriented application packages and unified control of continuous and discontinuous processes.



TDC 3000 system users can build their own schematic displays in multiple colors, multi-dimensions, and even in different languages.

System availability is achieved through features for fault prediction and error detection and correction. And multiple levels of user-defined redundancy provide back-up for all TDC 3000 devices. Parameter validation and keylocks ensure against unauthorized system access or misuse of information.

Maintenance of TDC 3000 includes automatic testing and built-in self-diagnostics. Malfunctioning devices or modules can be removed from service without disturbing the rest of the system.
–Hanrahan **Write 242**

DEC Compatible Micro For Real-Time And Time Sharing Applications

Announced at DEXPO '84 in Boston, Scientific Micro Systems SMS 1000 Model 40 is a new Q-bus compatible Winchester-based microcomputer system. At the heart of the system is what SMS have dubbed a foundation module. Located under the disk drives it does not occupy any of the Q-bus backplane slots. Functionally, it integrates a mass storage device controller, two serial RS-232 communications ports, backplane circuitry and a support monitor subsystem on a single board (**Figure 1**). The support monitor subsystem itself allows users to perform diagnostics, isolate component failures, examine system status, change system parameters and perform backup and load operations. It is accessible from the front panel or from a menu driven console terminal.

The disk controller architecture is

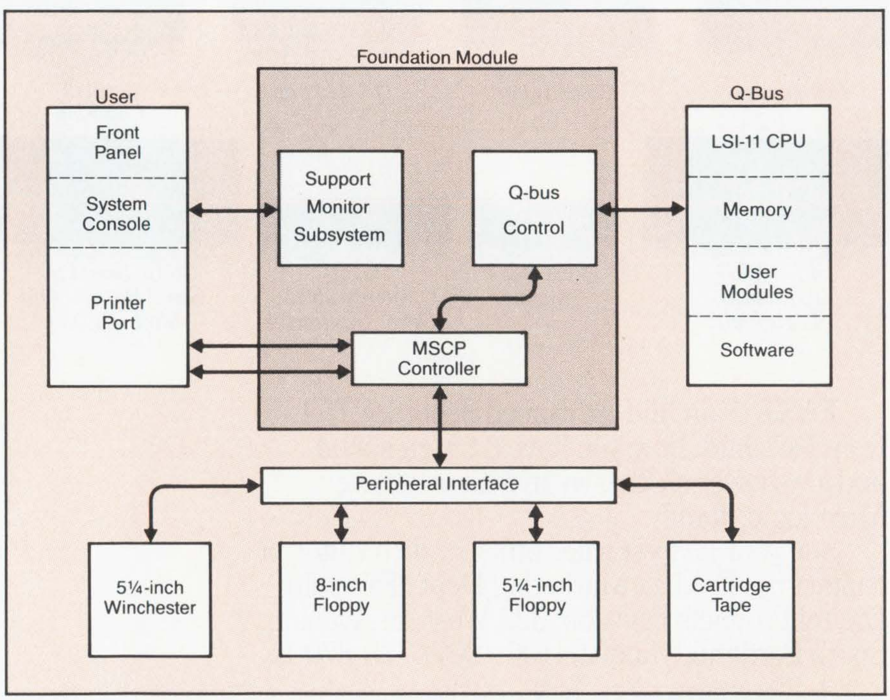


Figure 1: SMS 1000 Model 40 Block Diagram.

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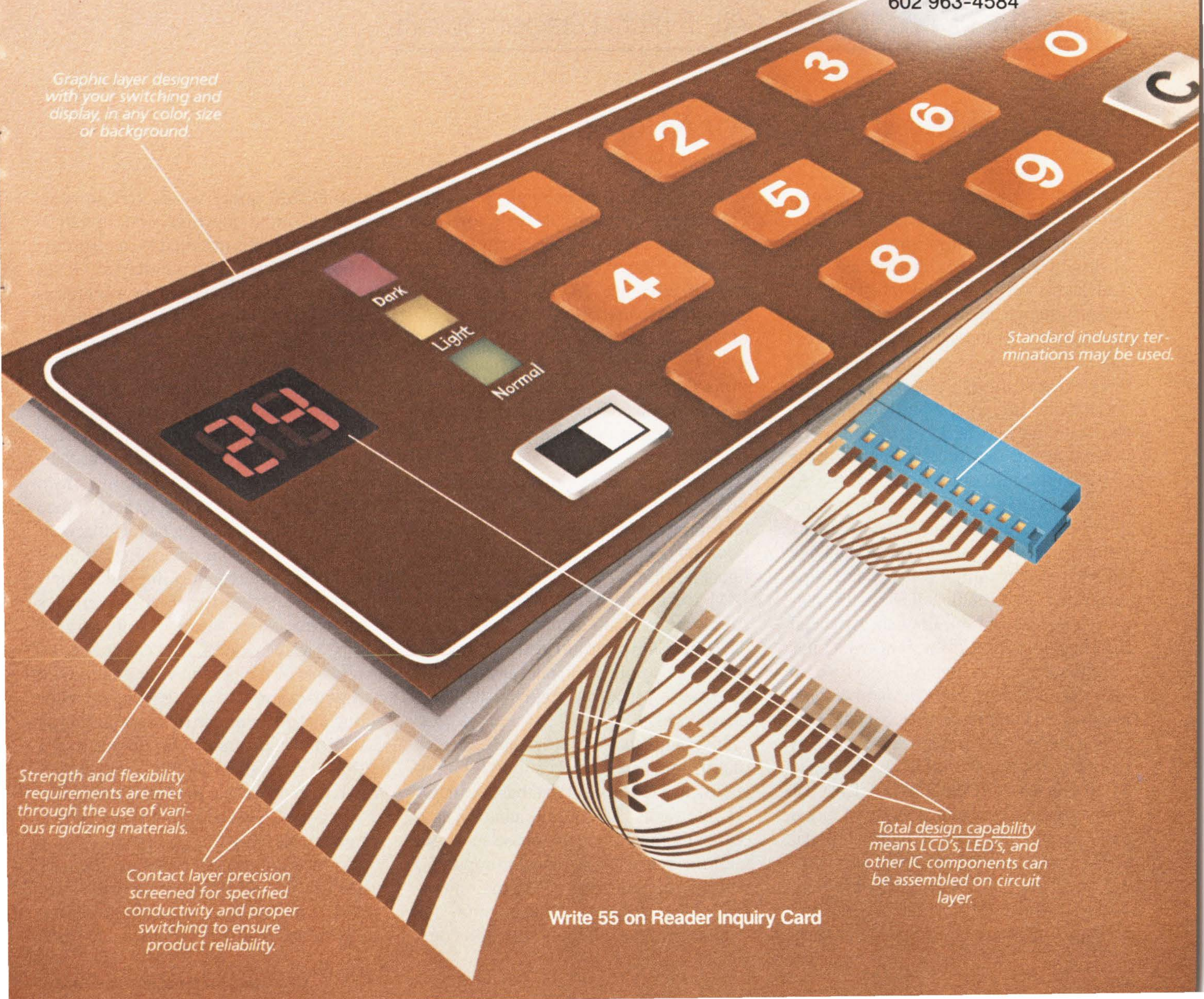

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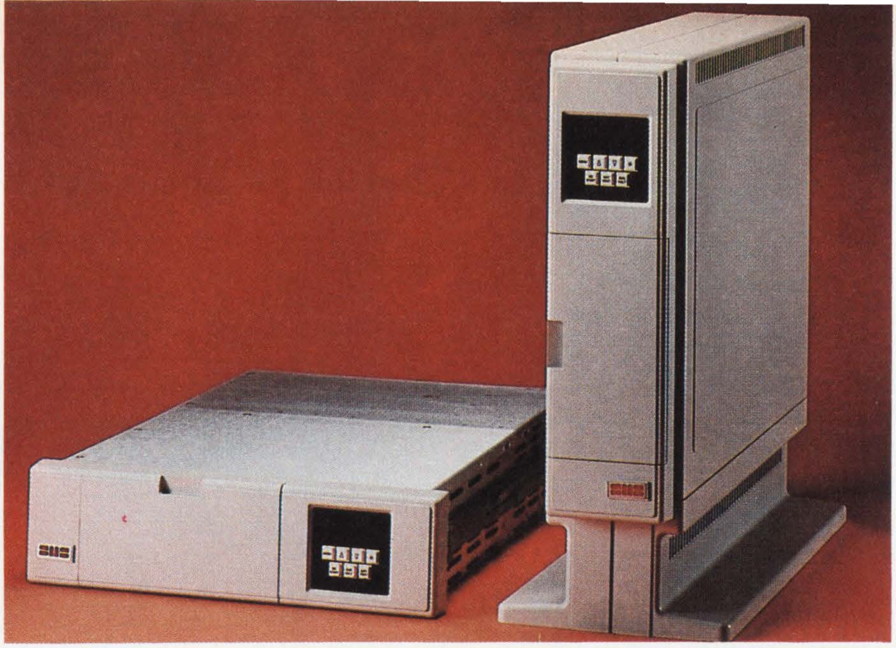
Figure 2: LSI-II Q-bus compatible microcomputer from SMS.



compatible with the DEC Mass Storage Control Protocol (MSCP). SMS' implementation provides features like noninterleaved format for disk, overlapped seek ordering, flaw mapping and error correction. The controller also supports block mode transfers between the disk and main memory.

The system can be configured with a range of 5¼" Winchesters, an 8" floppy and 5¼" floppy disks. An add-on start-stop cartridge tape subsystem is available for high-speed high capacity backup. The Model 40 will also support an integrated streaming tape in the near future.

—Wilson **Write 243**

DEPARTMENTS/AI–Fifth Generation

Artificial Intelligence For Micros

One of the goals of fifth generation computer work is to attain artificial intelligence, which will allow interaction with a computer much as with a human. Several facets of the human interface will have to change, and the technologies are developing now to make this change possible. Expert or knowledge-based decision capabilities, natural language, speech and image recognition and synthesis are all part of AI.

Several software programs now on the market address some portion of the AI puzzle, and though these capabilities are generally demanding of the computer's power, they are now being made available for microcomputers. From a mainframe program called Intellect designed to recognize and use natural English, Artificial Intelligence Corp. (Waltham, MA) has developed a micro-to-mainframe link, so users of IBM PCs and compatibles can use everyday language to access data residing in the mainframe. Another IBM PC program for natural language use is Microrim's (Bellevue, WA) CLIO, or Conversational Language Inquiry Option that operates with their R:base relational DBMS programs. Expert decision making on an IBM PC is also possible with Expert-Ease, an expert system generator program published by Export Software International Ltd. (Edinburgh, Scotland).

Intellect has been available for IBM mainframe systems since late in 1980. In a move telling of the importance of artificial intelligence, IBM entered a formal agreement to market the package in June of last year. The program creates an "English Environment" to understand questions worded not only naturally, but in a variety of ways. The system even looks for ambiguities and multiple meanings to clarify them.

The user needs no knowledge of where the data requested is on the system; Intellect can transparently perform many actions per user interaction, in a truly intelligent fashion. With the link to micros, an IBM or compatible PC with 256K RAM running CP/M-86 can access all of the data under the program in the IBM mainframe. PC application packages run unmodified, yet allow English language interaction.

Just as this natural language access to mainframe databases is important, easy access to PC-resident databases can use AI interfaces. Microrim's charter as a company is to create database management systems for personal computers, and ease of query has gotten their attention. The resulting CLIO option for R:base programs begins with 300 common DBMS query words and phrases. When an input question is not in that library, a dialog is initiated to incorporate it for the future. The number of recognized queries can increase by as much as 500 words or phrases. One particularly useful type of query to define for the system is the result of some calculation or computation, like percent or profit.

Another aspect of AI is an extension of expert systems for problem solving. Expert-Ease is a program that generates decision rules by generalizing from examples entered by an expert. Once several problems and the factors that contribute to a particular decision or solution have been entered into the microcomputer, the software uses these as examples and extrapolates future results on that basis. This way, an PC user can access the expertise of the person who entered the original examples with relevant contributing factors, with the machine acting as a decision consultant. This program, developed in Scotland, is handled in the US by Jeffrey Perrone & Associates (San Francisco, CA) and Expert Systems, Inc. (New York, NY).

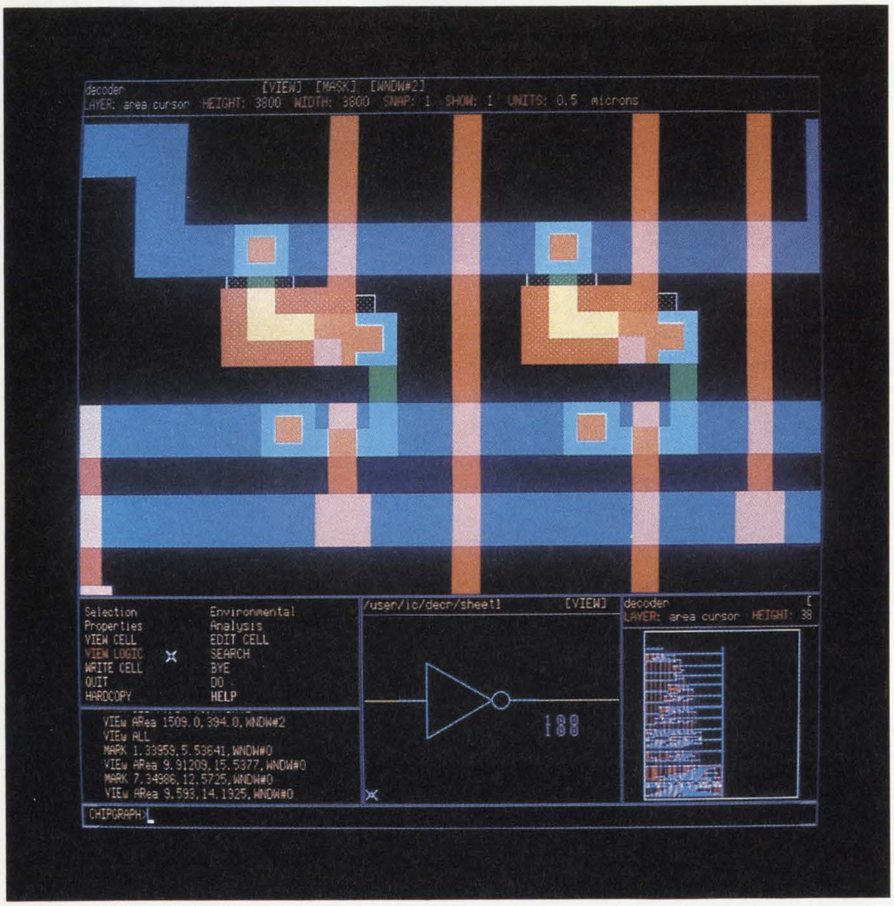
With the appropriate software, then, an IBM PC can understand plain English requests to access data from a mainframe or its own database. An unsophisticated user

no longer need fear his ignorance of where data is within a system, or even how to talk to the computer to get it to find out. And the decision-making prowess that makes only a few people experts in any given field is accessible through a PC. Artificial intelligence is no longer just a dream for huge sophisticated computing centers; the beginnings of an intelligent computer have become available on desktops that house IBM PCs and compatible micros. — *Pingry*

Artificial Intelligence Corp. **Write 234**
Microrim **Write 244**
Expert Systems **Write 245**

DEPARTMENTS/CAD

Logic And Layout Merge



Chipgraph combines logic and layout in a single software system.

In the design of complex VLSI circuits, a flexible approach to design may be reached through supporting user-defined links between logic and layout. Mentor Graphics' (Beaverton, OR) first entry into the fully custom IC design market combines system-logic design and the final layout on silicon.

Full Integration

Designers typically work in a top-down hierarchical fashion. Symbolic logic design deals with graphics symbols that represent the building blocks of an integrated circuit, such as NAND gates, NOR gates and inverters. Designing VLSI chips involves the on-screen capture and interconnection of these various logic building blocks.

From this logic design, Mentor Graphics' Chipgraph editor supports both symbolic and composite (mask-level) capture of the layout information, and automatically converts symbolic designs to mask-level layouts that adhere to all geometric design rules. Symbolic and mask-level layout can be mixed on a cell-by-cell basis – allowing the designer to achieve the optimal speed of design within chip size requirements. Interactive analysis can be performed at any stage, letting the engineer refine the design in progress.

In the Chipgraph editor, each cell stored in the data base contains an indication of the logic component it represents, technology rules, status of checks on the cell, a reference to the cell's possible predecessor and other "header" information, most of which is non-graphic and does not appear on the screen. Each cell also contains information on internal structure and external interfaces to other cells.

The system includes a standard set of symbolic layout tools, such as cells and interconnections. Chipgraph's interactive editing capability lets designers intervene at any stage of the design process, select cells then cut and paste the cells – or portion of cells – among windows. Each window offers a user-defined view, such as a close-up of transistors within a device or an overall view of blocks within the design.

The Chipgraph editor offers interactive analysis of design and electrical rules, enabling engineers to check selected areas of work in progress. Sophisticated path-analysis tools provide fast, thorough final evaluation.

Integrating Chipgraph with the Mentor Graphics' IDEA system of logic and circuit design tools provides a single-system approach to logic and physical design. Mentor Graphics expects the system to be used by electronic and integrated-circuit design engineers, by merchant semiconductor vendors to shorten the preparation time needed to make commercial circuits, and by system houses to create proprietary ICs for specialized applications. – *Hanrahan* **Write 241**

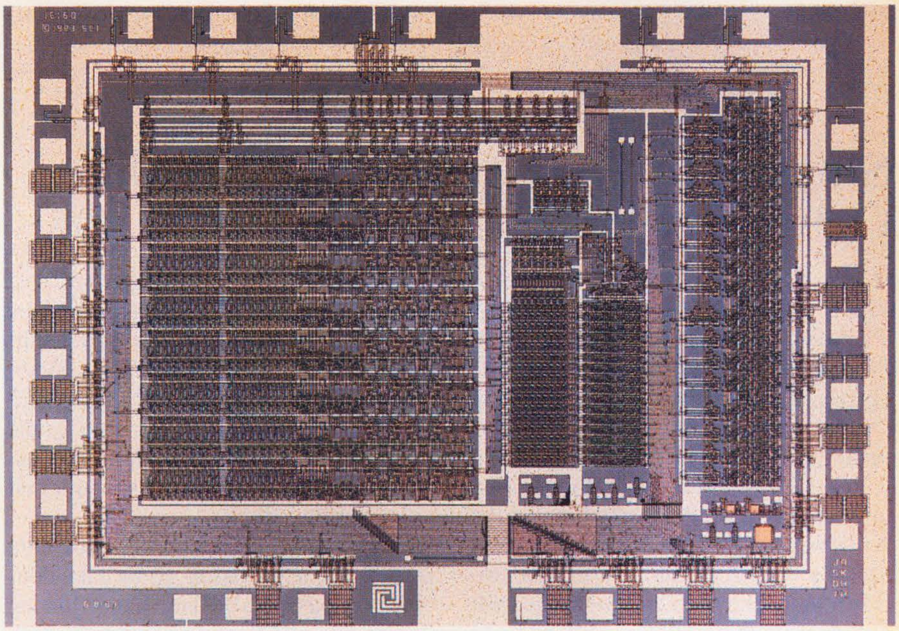
IC Design With Silicon Compilers

An alternative exists for designers restricting themselves to using gate arrays or standard cells in system-level design of custom ICs. Based on concepts that allow a chip to be "compiled" of configurable silicon building blocks, silicon compilers let system designers concentrate on architectural issues and avoid constraints of geometric design rules and other physical IC-design issues. With a compiler, systems designers describe their concepts in an architectural lexicon with which they are familiar. Ultimately that description is translated into the appropriate geometric structures that constitute the equivalent chip layout.

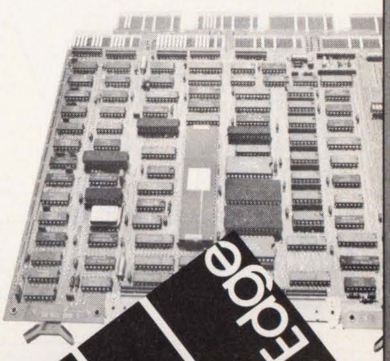
The silicon compiler differs markedly from a standard-cell methodology. In the latter, frequently used subcircuit functions are identified as building blocks and designed geometrically in advance by the provider of the cell library. Because such building blocks lose universality of applications as they increase in function and size, cell libraries typically consist of scores to several hundred low-level functions such as gates or flip flops.

In contrast, a silicon compiler operates from stored sets of rules from which it can synthesize, on demand, extremely complex building blocks – such as arithmetic logic units or even complete data paths – with hundreds of variations possible for the dozen or so generic blocks actually required for modern system architecture.

For example, a complex very-large-scale integrated circuit that supports 16-bit raster or bit-mapped graphics for such applications as personal computers, engineering workstations, graphics terminals and computer-aided design and manufacturing (CAD/CAM) systems has been designed by Silicon Compilers Inc. using advanced silicon compilation design techniques. Called the RasterOp chip, the device provides complete capabilities to scroll screens, manipulate windows, draw vectors or paint characters. Presently it is used in engineering workstations designed and built by Sun Microsystems Inc. Like their DEC MicroVAX I and SEEQ Ethernet chips, Silicon Compiler's RasterOp chip was designed while Sun Microsystems designed the system. The first prototypes were out of wafer fabrication and into working systems



Silicon Compilers' RasterOp controller chip, being used in Sun Microsystems' engineering workstations, was designed for bit-mapped graphics system applications.



within a week. Had Sun not used silicon compilation, the company would have had to design the RasterOp using conventional custom-IC design methods, meaning large investments of time and money. The RasterOp chip was developed in five months.

Chief among the benefits of the RasterOp chip are that it handles all bit shifts and bit masks, replaces about 80 TTL components and provides 50 percent better performance than software implementations of these functions. Additionally, the RasterOp chip supports both black and white and color displays, has 16-bit data paths and implements 256 functions to map destination. The RasterOp chip is available to other companies through a license from Silicon Compilers. *–Hanrahan*

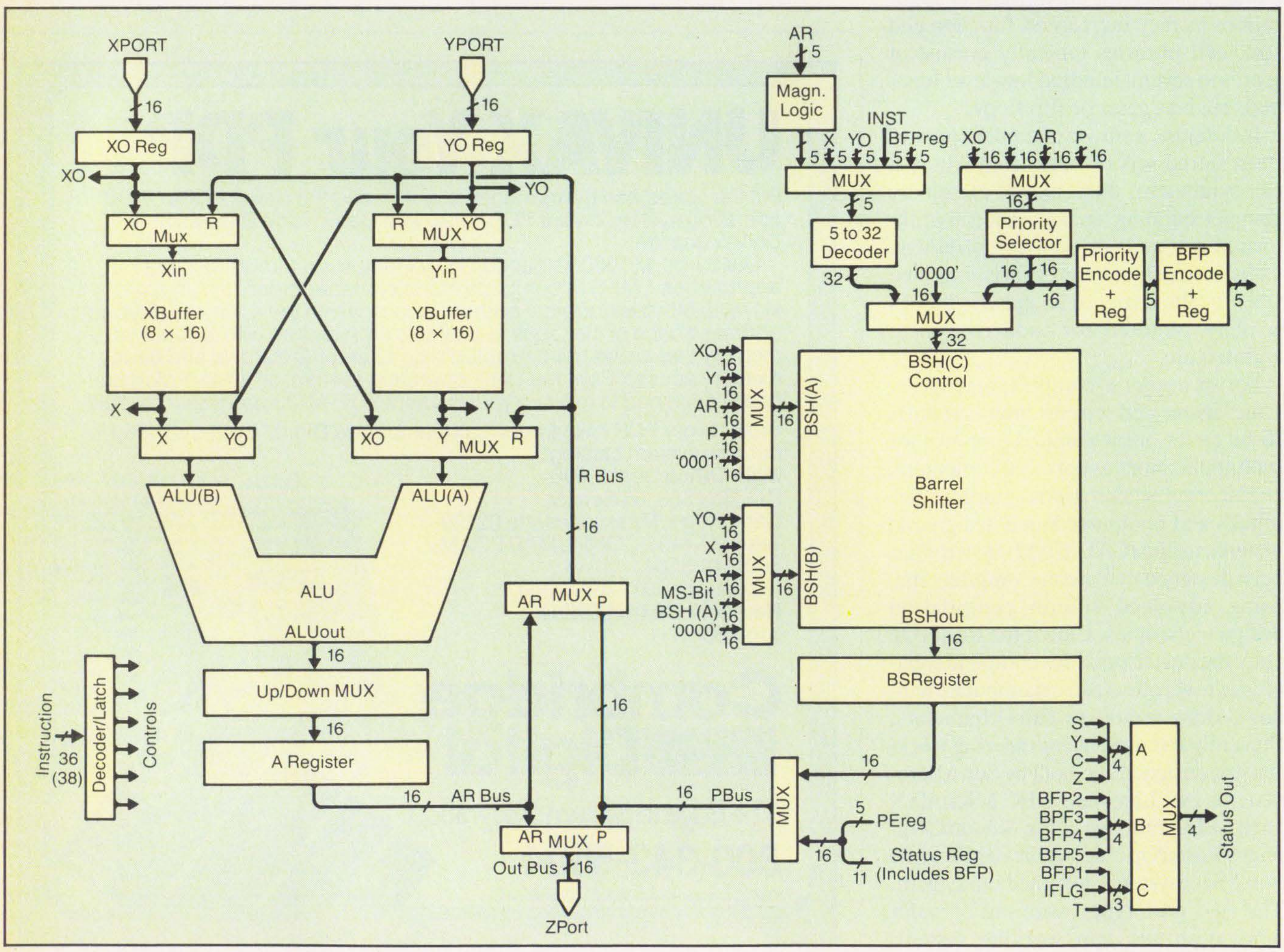
Write 239

Single Chip ALU And Barrel Shift Unit Optimized For DSP Applications

At this year's IEEE International Conference on Acoustics, Speech and Signal Processing, Dr. Jerry Nuttall and John Oxall of Analog Devices DSP Division (Norwood, MA) described in detail their new ADSP-1200. The 1200C CMOS chip features a 16-bit wide ALU, three ports, on board barrel shifter in parallel with the ALU, register files, priority encoder and a highly fielded instruction set. The two major units, the ALU and the barrel shift unit operate in parallel, simultaneously and independently. Data inputs may be operated on directly by the barrel shift unit, the ALU or both. Similarly, either the accumulate register, or the barrel shift register may be used as a source for the output. The ALU output may also be used as a source for the barrel shift unit and vice versa.

The ADSP-1200 handles four data types: single precision, 16-bit data; double precision, 32-bit data; block floating point data and floating point data. With few exceptions, all operations can be done with double precision by using two parts in tandem at only a 10% loss in throughput. All double precision operations except multiplications and divisions can be performed on the single chip but require multiple cycles to perform. A separate mode allows block floating point additions with automatic exponent control.
– Wilson **Write 233**

Arithmetic Logic and Shift Unit.



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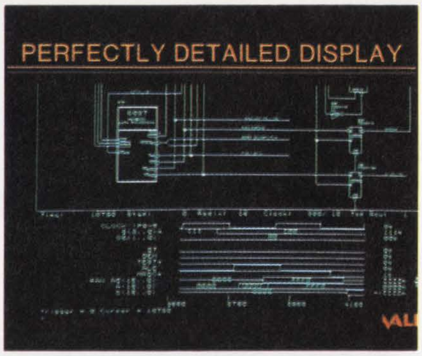
Total System Simulation Uses Actual Copies of Chips

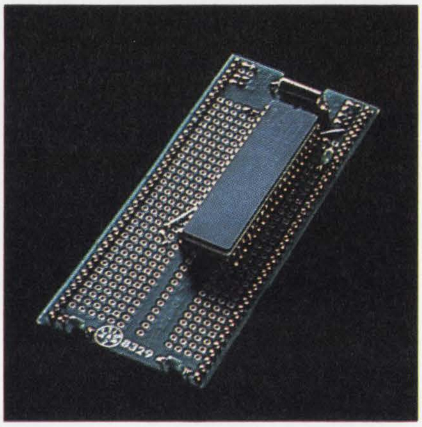
One of the most difficult problems facing designers today is validating designs containing complex VLSI devices such as microprocessors, peripheral chips, and floppy disk controllers. Realchip, a new simulation technology designed by Dr. L. Curtis Widdoes, V.P. and Chief Scientist at Valid Logic Systems, uses an actual copy of a chip as a hardware reference element for simulation purposes.

Advantages over other simulation methods are found in the simulation speed which is increased by one or two orders of magnitude since simulation is performed at hardware rather than software speeds. The model then, is known to be perfect because the device models itself.

Realchip may be added to any of Valid's SCALDsystem I or SCALDstar workstations. SCALDstar offers a single-package coverage of the steps from logic design through geometric layout. The schematic entry, logic simulation, and timing verification hardware and software belong to Valid's SCALDsystem I for logic design. SCALDstar adds software and a color graphics display for IC layout.

Realchip's basic configuration supports up to four reference elements and is housed in either a desktop or mounted on adapter modules that plug into cabinets. Additional Realchip boards may be added to support up to 32 reference elements.





Valid Logic's "RealChip" uses an actual copy of a chip as a hardware reference.

Designers can create their own models of custom or sample devices. Valid will supply models for popular device families such as the 8086, 68000 and 2900 microprocessors. Yet, the technology is not restricted to microprocessors; many models of peripheral chips will also be supplied.

Designers may create models of their own proprietary custom chips or model new devices for which only early sample chips are available. If using the SCALDsystem software device libraries, designers may freely mix software models with Realchip models in designs. When simulating complex designs, the SCALDsystem with Realchip, for example, becomes a virtual logic analyzer exercising a virtual breadboard. Each simulation generates a perfectly detailed, nanosecond-by-nanosecond display of signal activity such as that in an actual logic analyzer display. *—Hanrahan*

Write 246

SBC Includes On Board Operating System

Specifically designed to meet the needs of a broad range of applications that include multiprocessing, front end processing and stand alone use, Intel's new 186/03 single board computer combines a CPU, memory, SCSI interface, serial I/O and interrupt control all onto a single Multibus card. The CPU, an 80186, works in conjunction with the Intel 80130 Operating System Firmware Component (*Digital Design*, January, 1983, p. 52) that provides the nucleus primitives for those applications that require a real-time executive, as well as providing timers and programmable interrupt control. The 80130 component may be replaced by the 80150 CP/M Operating System or the 87100 user programmable firmware component. There are eight JEDEC 28-pin memory sites on the board. Four of these may be used for EPROM or EEPROM program store while the other four RAM sites may be used for static RAM or iRAM data storage or used for additional program storage. The parallel peripheral interface consists of three 8-bit parallel ports. As shipped these are configured for general purpose I/O, but may be reconfigured by the user to be compatible with the SCSI interface by adding two user supplied PALs, moving jumpers and installing a user supplied 74LS640-1 device. Alternatively, the parallel interface may be configured as a DMA controlled Centronics compatible line printer interface.

The board also contains two programmable communications interfaces that use the Intel 8274 Multi-Protocol Serial Controller (MPSC). Two 80186 timer outputs are used as software selectable baud rate generators capable of supplying the serial channels with common communications frequencies. Twenty-seven on board interrupt levels are also provided to service interrupts generated from 33 possible sources. These vectored interrupts are serviced by four interrupt controllers – one in the 80186, one in the 80130, one in the 8259A and one in the 8274. The 80186, 8259A, and 8274 act as slaves to the 80130 master. The highest priority interrupt is the non-maskable interrupt line that is tied directly to the 80186 CPU, and is typically used to signal catastrophic events, such as power failure.

– Wilson **Write 235**

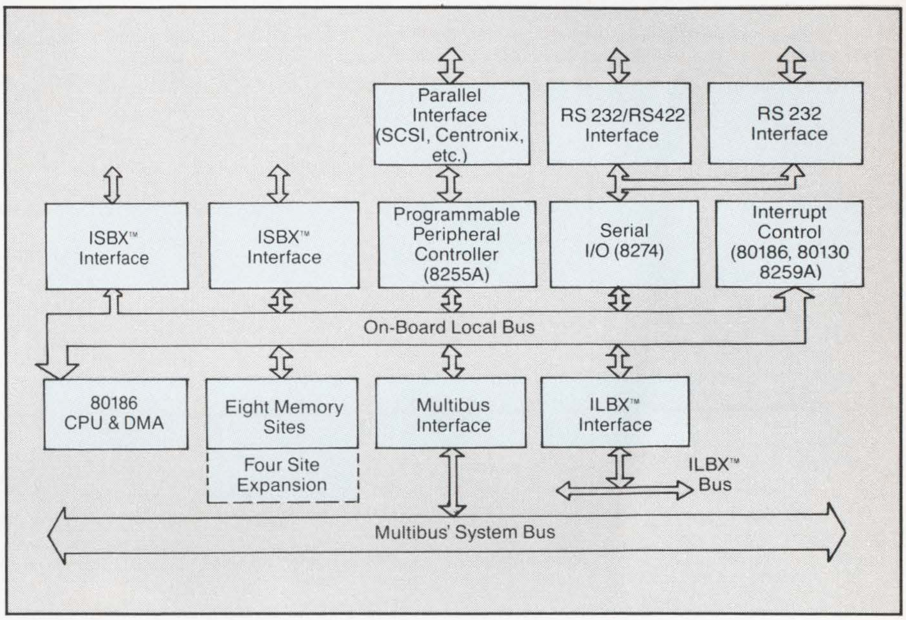
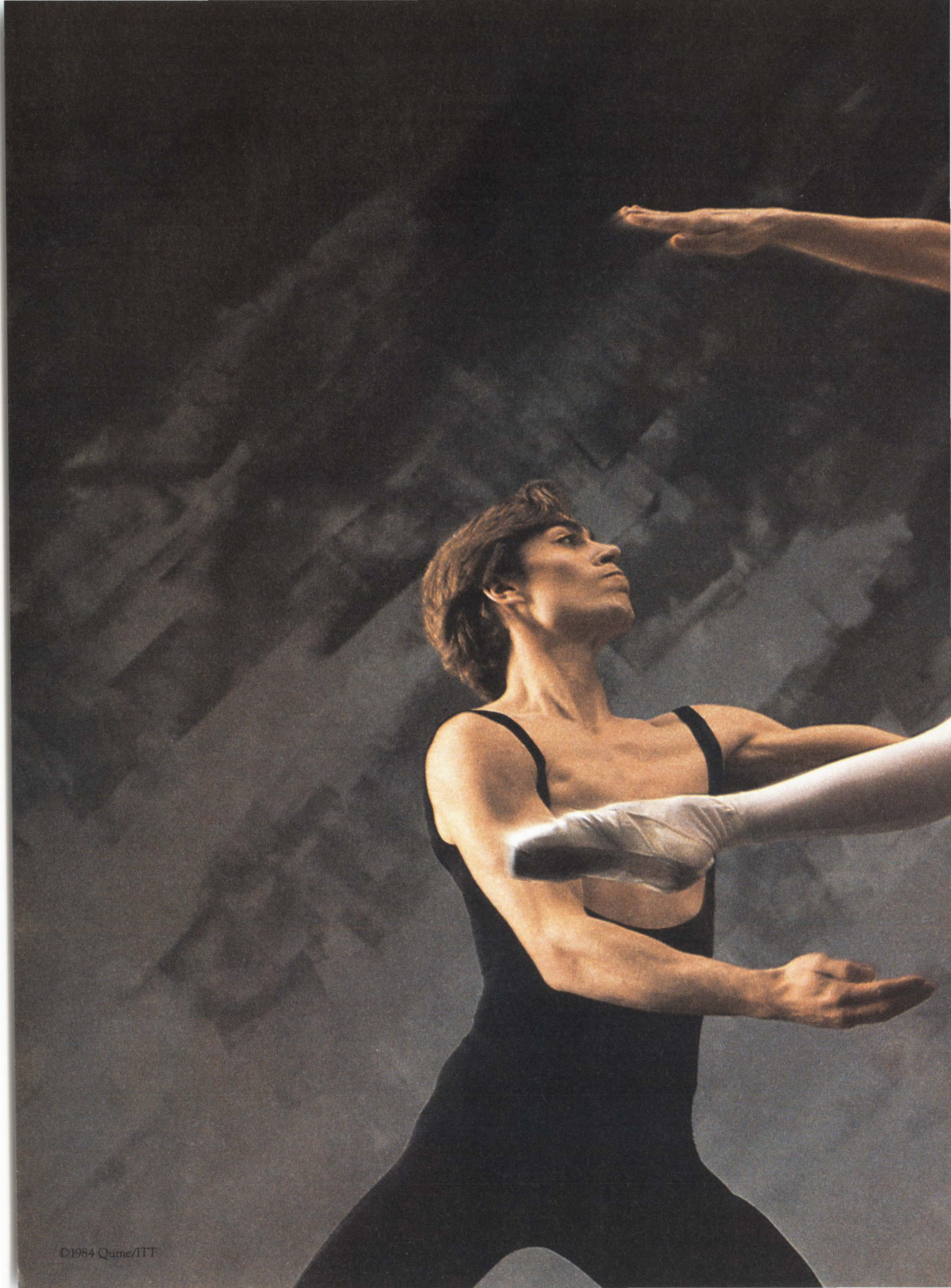


Figure 1: The iSBC 186/03 Board Block Diagram.

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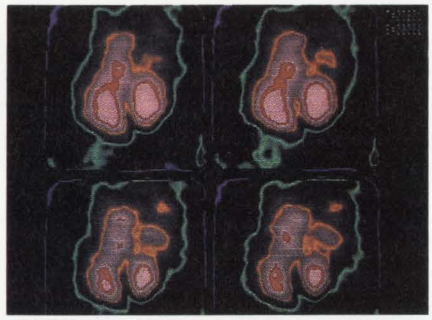
Modular Architectures May Be The Next Array Processor Design



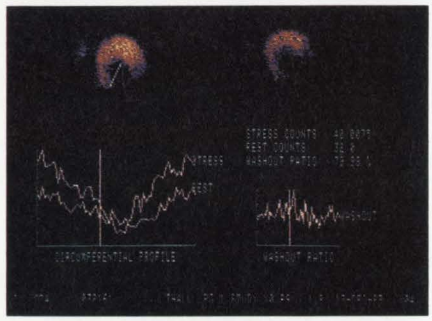


Figure 1 (above left): Photo shows two satellites used for radar signal processing, an application for array processors. (Photo courtesy Floating Point Systems)

Figure 2 (above top): The photograph shows a comparison study of cardiac images using an isocontour color table. (Photo courtesy Computer Design & Application)

Figure 3 (above middle): Images of a heart in stress and rest phases, with supporting curve graphs. (Photo courtesy Computer Design & Application)

Figure 4 (above bottom): An example of a Computer Tomography Scanners image of the brain. (Photo courtesy Floating Point Systems)

by Andrea M. Coville,
New Products Editor

Array processors became affordable and accessible for system designers at approximately the same time that the development and application of microprocessors caught public attention in the 1970s. At that time, array processor manufacturers such as Floating Point Systems and CSPI developed systems to support high speed computation for equipment like Computer Axial Tomography Scanners.

These early machines were programmable number crunchers with prices in the tens of thousands of dollars. Designers were unable to use them as a general tool because prices were exorbitant, algorithms were not suited to the specialized structure of arithmetic pipelines and programming was complex.

In addition, the need for Fortran compilers and a scarcity of programmers with the necessary hardware and software talents were factors.

In its simplest definition an array processor is a specialized computational device which performs iterative vector and matrix calculations. Used as a peripheral to a host, array processors are commonly used in digital filtering and signal processing applications where the host is freed from computationally intensive filters.

Array processors can be categorized as those that perform floating point opera-

Early machines were programmable number crunchers with prices in the tens of thousands of dollars.

tions and those that carry out block floating point and fixed point calculations. The difference between the two is analagous to calculators which give eight places of accuracy and scientific calculators which have eight or ten digits plus an exponent. Floating point numbers provide greater precision if a larger word size is used. Fixed point array processors are faster and their hardware less complex. For certain applications the dynamic range of floating point processors is a necessity while in other situations fixed point machines with the same binary word size are faster and most cost-effective. Previously it was only cost effective for OEMs to integrate the high cost array processors in larger systems. Present prices range from six thousand to one million dollars.

The companies in this survey have addressed problems of overhead, programming and price restriction through architectures with different bus structures, memory architectures, number of processors and methods of I/O.

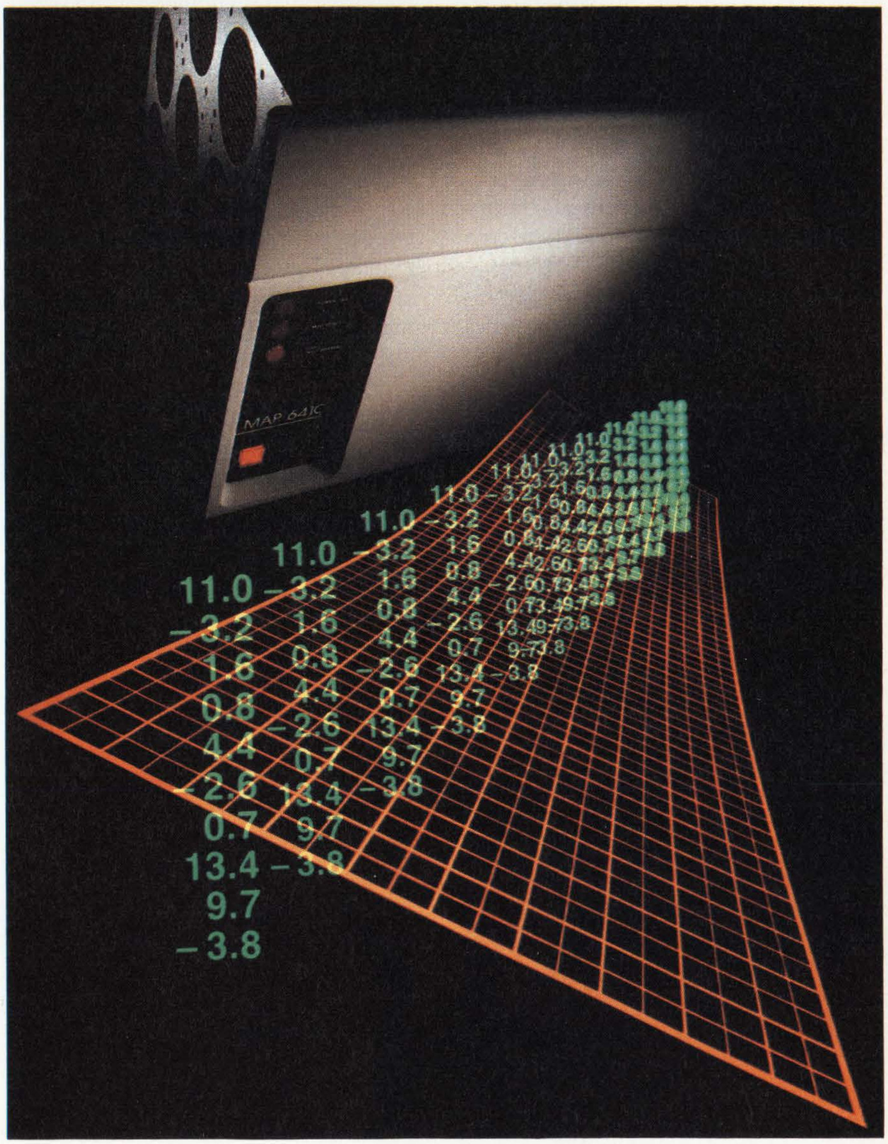
Standalone Array Processors

Manufacturers such as CSPI, Computer Design and Automation, Floating Point Systems and Numerix supply standalone machines for scientific and signal processing environments, a market that is comprised of both fixed and floating point systems. These machines are configured with a power supply, cooling system, and internal bus backplane, which allows the addition of memory options and provides local expandability. Because standalone systems have a variety of memory options, users configure systems for individual applications. This limits the overhead between the host and array processor by controlling program execution and I/O activity.

Among the fundamental design issues are large memory requirements and parallel, pipelined and systolic architectures. Parallel architecture performs serial operations simultaneously, while pipelining is constituted by repetitive rather than disparate operations. Systolic architecture comprises an array of identical computation cells with common interconnects, timing and data flow. Throughput is directly proportional to the number of computation cells.

Numerix, for example, makes the MARS 232, a programmable block floating point machine for signal processing applications and the MARS 432 Programmable Array Processor which performs floating point calculations. Both models have similar architectures with an interface processor (IP) and data processor (DP). The 232 IP, of which two versions are offered, arbitrates the high speed data I/O bus which controls a 32-bit transfer occurring every 200 ns from one of eight asynchronous devices. In the MARS 432, the principle arithmetic element is the DP which is structured to have an explicit separation between data memory (512K) and program memory (64K). For most high performance array processors this is a necessary feature because it allows additional speed to be obtained in the arithmetic processing. There are data paths between the two memories and the data memory may be used as a bulk storage area for large program memory segments. This storage design is a faster alternative to storing programs in the host computer because the transfer rates through the host data interface are relatively slow. The primary arithmetic elements in the data processor are a multiplier and two adders which execute in parallel.

Figure 5: The MPA 6410 64-bit array processor from CSPI.



The MARS 232 data processor is available in two versions; the DP-C which is capable of four multiplies and six adds in 200 ns, and the DPR which does one 32-bit multiply and two 32-bit adds in the same amount of time. Most of the instruction set for these processors is data dependent, a feature that simplifies programming by eliminating branching.

Shared Memory

Founded in 1968, CSPI first produced the MAP 200/300 32-bit floating point array processor. The MAP 6400 followed, which CSPI claims was the first 64-bit floating point machine. Two subsequent models, the MAP 400 and the MiniMAP, were designed for system integrators. Completing the product line are the MAP 6410 and 6420, both 64-bit array processors.

Two problems addressed by CSPI are the saturation of the host CPU and an inadequate turnaround of information. By offloading number crunching tasks to the array processor, the CPU is relieved of the burden of processing large amounts of data, allowing the host computer to quickly perform its regular functions. CSPI's concept of shared memory provides a mechanism for the host and array processor to access the same memory without having to transfer data to and from the host.

In this configuration, the AP instructions are an extension of the host instruction set, which is useful for spreading the handling of moderate size arrays. Illustrating this approach is the MiniMAP Series whose basic configuration consists of four hex boards with 64K of memory. In this system the host Unibus is directly ported into the MiniMAP's memory.

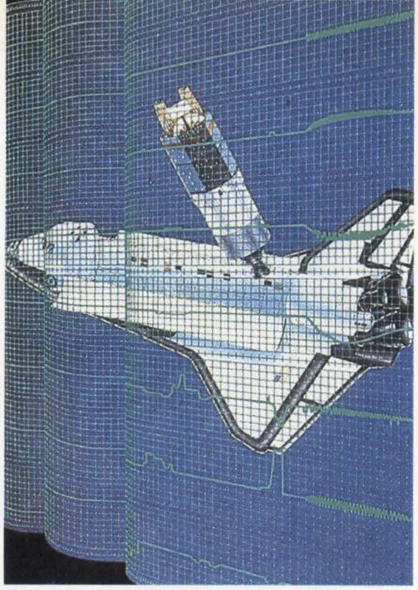


Figure 6: An example of real-time simulation. (Photo courtesy Floating Point Systems)

The memory structure of the MAP 6410 differs from the MiniMAP Series because it has independent program (128 Kb) and data (512 Kb) memories. These memories are linked to a host interface module. The system incorporates a 64-bit arithmetic processor with a non-pipelined architecture, containing 14 multipliers and 14 adders. The MAP 6420 is similar to the 6410, being a 64-bit processor but differs in that it incorporates a Fortran compiler, the central component of the system's development software.

Peripheral Array Processors

Analogic's systems address the market for Peripheral Array Processors (PAPs) characterized as high-speed pipeline processors which are capable of repeatedly performing specific operations on data sets. These processors are treated as I/O devices by the host computer. The PAP is attached to the host bus, and relies on host resident software for operational control. Data is transferred through DMA. Peripheral array processors necessitate large blocks of memory dedicated to the AP which are accessed over the external bus structure.

Analogic's AP400 addresses these limitations with a major change in PAP architecture. Unlike previous PAPs the AP400 control processor is not directly responsible for controlling each cycle of the arithmetic pipeline. Instead, commands are queued allowing it the flexibility to service interrupts, communicate with the host and service auxiliary I/O ports.

To accommodate a variety of hosts, Analogic designed a Programmable Input Output (PIO)/DMA interface.

The AP500 is an enhancement to the AP400. The MC68000 controller, the Pipelined Arithmetic and Logic Unit, and the I/O interfaces operate in parallel to maximize processing throughput. Computations are performed by the AM2901 and AM2910 bit slice processors. DMA access is controlled by the AP500 eliminating host DMA support.

A Fluctuating Market

Star Technologies views the market as rapidly changing with competition in all price ranges. In some instances, such as board level processors, prices are dropping. However for higher performance, prices have remained consistent. Star's approach has been to enhance existing processors to serve new markets.

The ST-100 is a $25,000.00 multiprocessor system that attaches to one or more general purpose computers. The master control processor employs two MC68000 s and 256K of memory. This processor controls three subordinate

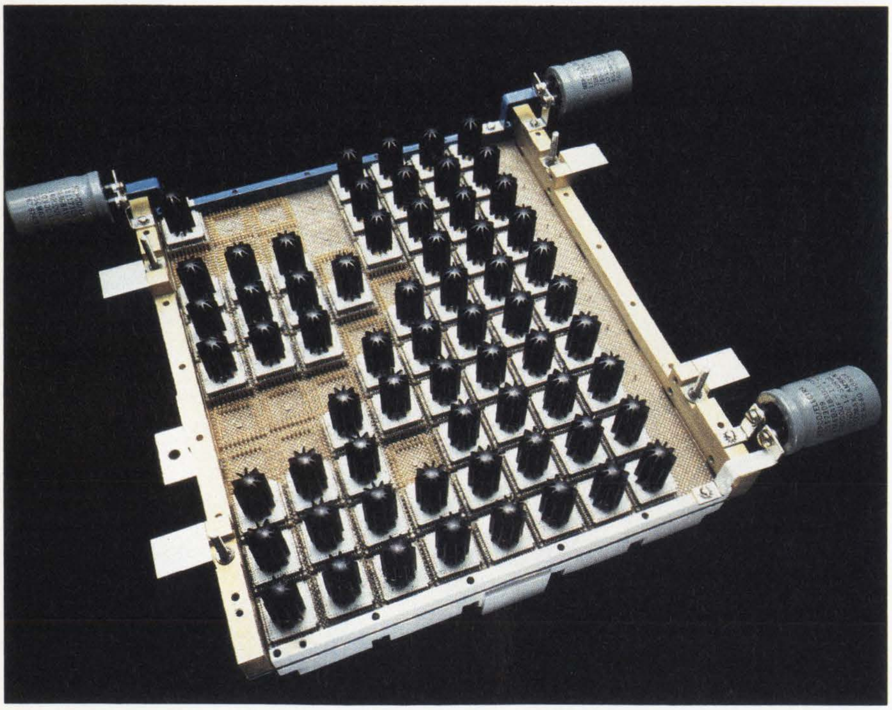


Figure 7: Star Technologies arithmetic unit circuit board. This 13-layer board is populated with Motorola 10K MECL gate array chips.

arithmetic computational units.

The arithmetic section consists of a computation subsection coupled with an arithmetic control processor. It contains two adders, two multipliers which are three step pipelines, and a divide/square root section that is non-pipelined. The control processor consists of four ALU's specified for address generation and loop control. Main memory has three ports which are assigned to the I/O subsystem, the data cache and the DMA.

Software

The MSP-3000 from CDA provides "Mini-Language" a software development tool. An improvement on most array processors which are programmed in microcode, Mini-Language supports programming at the mini instruction level. In array processor code, 90% of execution time is spent on 10% of the code. It is desirable to microcode that 10% for faster execution.

The architecture of the MSP-3000 in a minimum configuration consists of one quad-sized circuit board and five hex-sized boards. The controller board communicates across a Unibus to an ISP instruction set processor, local bus controller, and up to four memory modules. Arithmetics are performed by a floating point processor card.

Applications

Applications for scientific computing when laid out on paper, begin to take on the appearance of a spider's web. Market segments such as structural analysis, computational physics, computational chemistry, electronic circuit design and oil reservoir simulation can be broken down into further application segments such as finite element analysis and quantum field theory.

One company preeminent in the sense of its longevity and influence is Floating Point Systems. The line of array processors manufactured by this company illustrates the breadth of applications to which the machines are applied. FPS array processors are used in medical imaging (CAT,NMR), remote sensing, simulation, fluid mechanics, signal channel simulation and real time acoustical signal processing. A unique application was its integration with the Aptec Dimensional Processing System to perform Landsat analysis. The system interpreted underlying geologic structures masked by sand dune formations.

The FPS-5000 software library contains 200 programs. The FPS-164 contains the Boeing Computer Services library. Both product lines interface to several front-end computers including DEC, Gould and Data General. In the case of the FPS-164, the ability to produce high levels of throughput in a computer facility has led to its use in manufacturing, university and small business environments.

The FPS-164/MAX is the most recent introduction from FPS and is a parallel pipelined machine. Classified as a special purpose computer for matrix operations, its design incorporates a parallel processor architecture which can compute 124 vector operations at a time. The FPS-164/MAX has the scalar capability of the original FPS-164 and the MAX hardware adds the capability to perform key matrix operations such as dot products, matrix-matrix multiplication and matrix factoring.

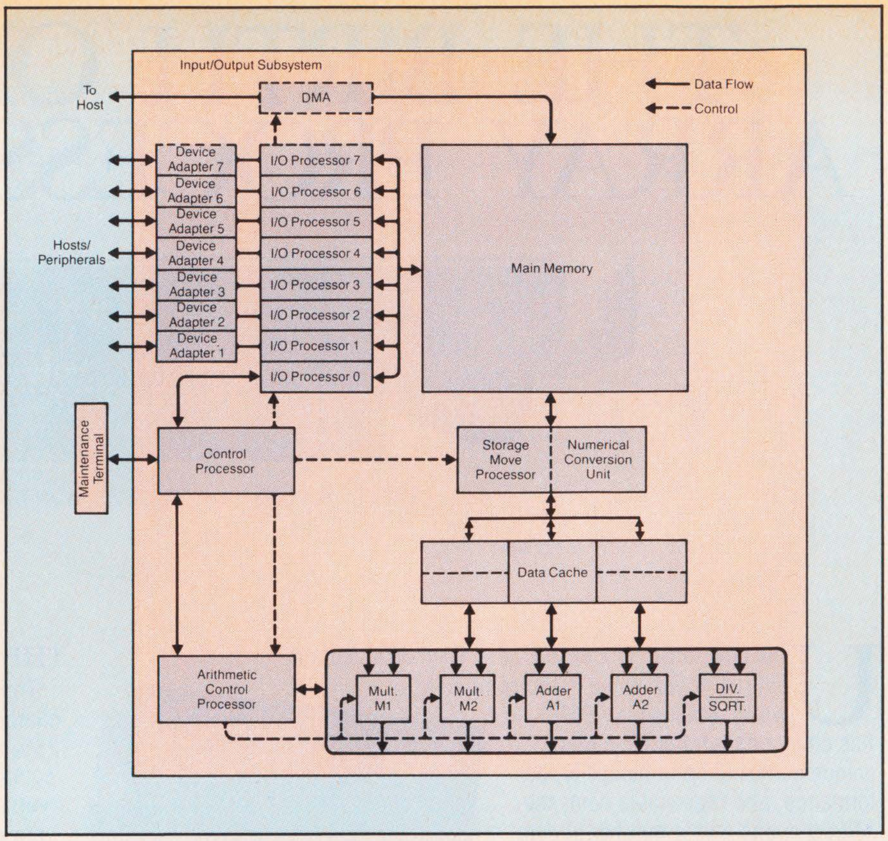


Figure 8: The diagram shows the hardware components of the ST-100 array processor from Star Technologies.

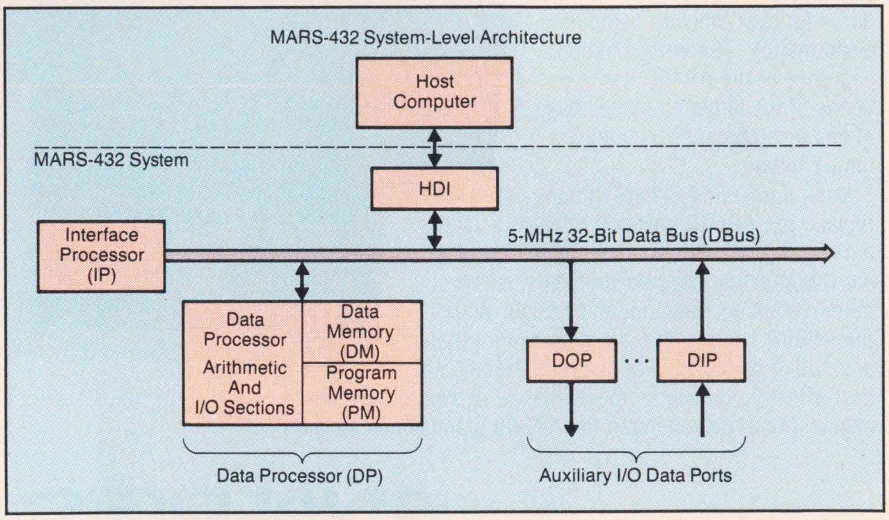


Figure 9: Diagram illustrates the key elements of the MARS 432 array processor from Numerix: the data processor, interface processor and 32-bit wide DBus.

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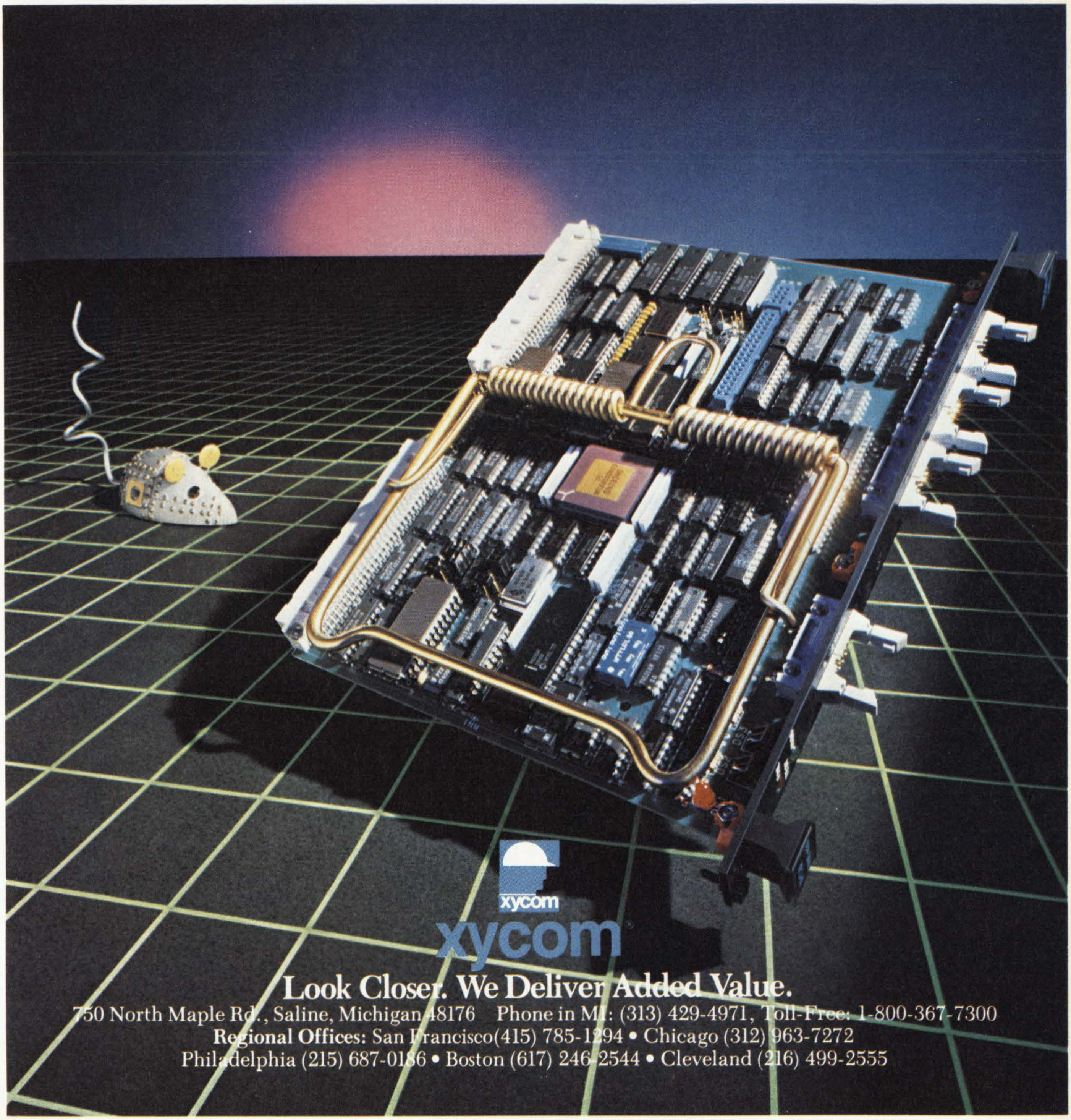

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The Boards

A number of manufacturers address a second arena of array processing equipment, i.e. boards specifically designed for array processing which can be added and interfaced into a host.

The Marinco 3000 line of array processors has two models, the APB-3024PC and the APB-3024M, an IBM PC and Multibus board, respectively.

The APB-3024 appears to the host as two blocks of contiguous data, although its architecture consists of five parts; data memory, program memory, microprogram controller, ALU and parallel multiplier. The data memory (4 to 64K) is dual ported and needs two instructions. Program memory is available as 2K of RAM or 4K of PROM.

The board has triple-ported memory accessible from the backplane, an auxiliary port, and the arithmetic sector card. Internally the data is organized as 24-bit words, but appears to the host as 32-bits. When floating point data is moved from the host's memory to the array processor the higher order 24 bits are stored in the array processor memory and the low order 8 bits are dropped. In the reverse direction, 8 bits are appended to the 24 bits to provide 32-bit value to the host. Integer data (16 bits) is stored in the fraction portion of the array processor's 24-bit memory.

The Marinco boards use Advanced Micro Devices' 29116 16-bit multiplier and 29116 16-bit ALU for the machine's one million 24-bit floating point operations a second. The APB-3024PC is an IBM PC board processor with dual ported memory accessing the PC bus and arithmetic section.

DSP Systems Corp. manufactures three array processor boards, the DSP-FFT-B, the AP-4 and the VAP-64 all for the Multibus. All three use TRW's TMC 1010 multiplier accumulator set designed for signal processing applications. The board is comprised of two double Eurocards. One contains the array processor and the other houses 32K dual port RAM for the main data memory.

DSP's solution to simplifying system software has been in implementing dual-ported RAMs which can be used independently of one another. To eliminate DMA, the AP-4 has a 64K cache memory. Included in the board's firmware are demodulation, peak pick instruction, FFT/IFFT, magnitude detection, block move and block add. It uses a total of 14 single word instructions, all resident in on-board PROMs. Completing the product line is the DSP-FFT-1B with ten macroinstructions to perform FFT.

Mercury Computer Systems ZIP 3200 Series of array processing boards, the 3216, 3232 and 3264 are board sets with a common software language. They are identical with the exception of the arithmetic pipeline. The 3216 has a pipeline designed for image/graphic and signal processing while the 3232 is designed for scientific and graphic applications. The 3264 was created for those areas involving simulation.

All three boards contain a software programmable control processor based on the AMD29116. Mercury optimizes

An Array Processor this fast and flexible can't sell for only $4250.

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The imaging requirements of a geophysical research project at sea demanded intense mathematical calculations.

An array processor was the answer.

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Marinco engineers, driven by necessity, pushed beyond the horizons of conventional array processor design.

A Single Board

They discovered how to shrink circuits to a single board — and to do so without sacrificing performance.

In fact, they enhanced it. Keeping signals within a single board actually made significant speed gains. Then they added other performance enrichments such as memory mapping and an auxiliary port for direct high speed I/O.

Easy to Program

Perhaps as important, the board is easy to program, even for someone with only high-level language experience. Standard routines may be adapted. Or new ones created. Marinco's assembler automatically generates the microcode and tracks the 48-bit control word.

Imaging Productivity

The speed and flexibility of the APB-3000 series can dramatically increase your imaging productivity. Use it for coordinate transformation, hidden line removal, vector-to-raster conversion, interpolation, image enhancement and many other operations.

Very Low Price

Even with all these advantages, Marinco innovations make it possible to offer the Multibus version for only $4250, quantity one, U.S. price. IBM PC versions are also available.

Can an array processor this fast and flexible really sell for such a low price?

Thanks to practical demands and Marinco innovations, it can.

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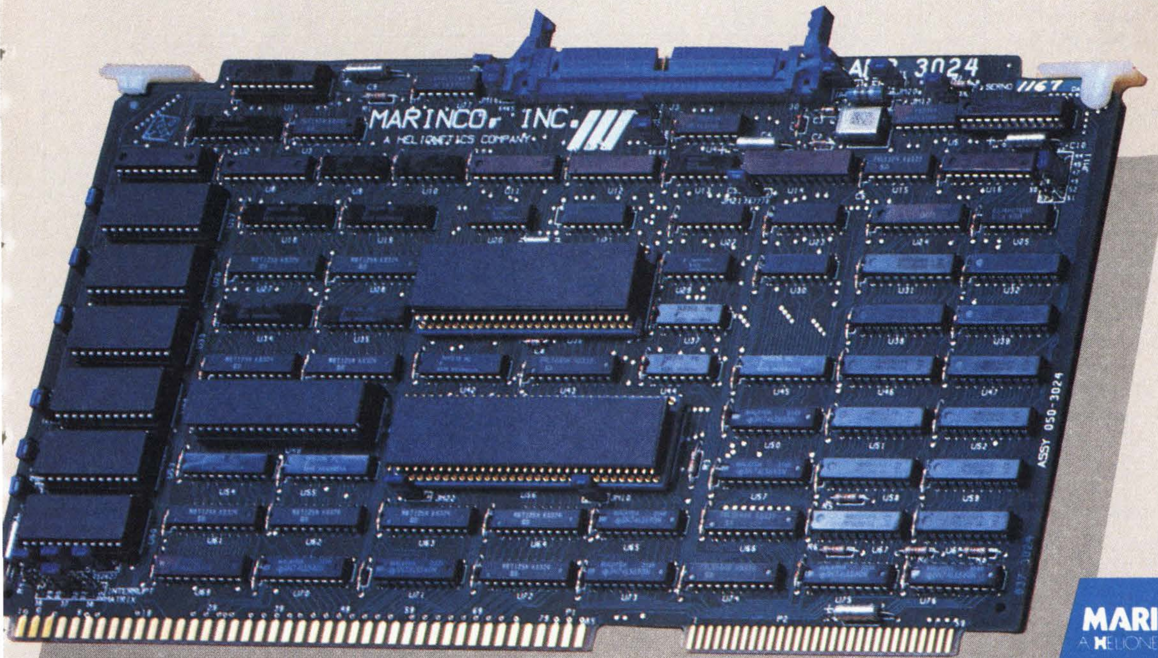
Specifications

Program Memory 2K X 48-bits **Data Memory** 8K words **Data Word** 24 bits long, 8-bit exponent, 16-bit mantissa (floating pt.) or 16 bits (integer).



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its control processor to support external and internal data transfers (16-, 32- or 64-bit), processing sequencing and external real-time events. The control processor can perform autonomous overlap of its program memory and that of the arithmetic processor, with programs stored in the array processor's main memory.

A unique feature of their arithmetic pipeline allows its use as an independent programmable unit. The pipeline has three computational formats, both on block and floating point. Its architecture includes an input buffer, a multiplier, ALU, four accumulators and an output buffer. Mercury also implements dual direct access I/O channels and a dual function host computer interface.

Sky Computers manufactures the Skymnks, a line consisting of four array processors; a two-board Q-bus set, a two-board Multibus set, a one-board Versabus card and a floating point processor designed for use on the Multibus, Versabus, VME, and S-100.

The Skymnks are pipelined, parallel co-processors which operate directly on data in-host memory. This design eliminates the need for separate Fortran calls to transfer data between the array processor and host. The Skymnks can address between 4 and 16 Mbytes of host memory and are compatible to 32-bit floating point operation.

All Skymnk processors have essentially the same architecture. The communications and interface logic performs programmed I/O and DMA transfers. Upon command, the external address sequencer moves data from internal memory to the floating point arithmetic unit as scalar operands. This happens while the host concurrently processes data.

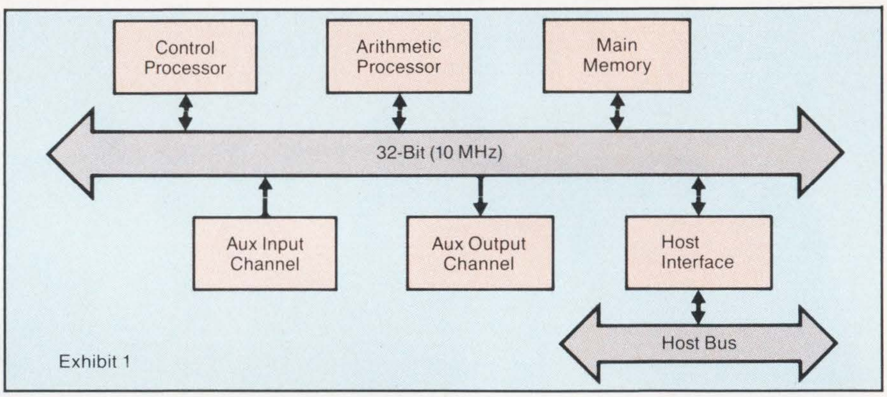

Figure 10: Hardware diagram of the ZIP 3200 series from Mercury Computer.

The advantages of using array processors is so great that sub-industries develop constantly.

Other Industries

The advantages of using array processing systems is so great that subindustries develop constantly. Two examples of these are the Shared Attached Memory System (SAM) from Texas Memory Systems and Aptec Computer's Dimensional Processing System.

Texas Memory Systems developed their product for integration as an auxiliary memory device. The unit has a three stage memory hierarchy allowing a large data array to be buffered by the CPU instead of on the disk.

The SAM Systems is a 128 Mbyte eight port memory system. When attached to an array processor, the SAM 400 chassis may be specified to allow a maximum of 32 Mbytes of memory. Essentially the CPU will use the SAM system as a buffer for large data arrays. Each array processor has access to SAM memory independent of the host bus. The SAM System is accessed by the array processor through I/O drivers which can be linked into the SEL, Floating Point, Perkin-Elmer and Digital Equipment Software libraries.

The DPS (Dimensional Processing System) – 2400 from Aptec mentioned earlier also interfaces to a PDP-11 or

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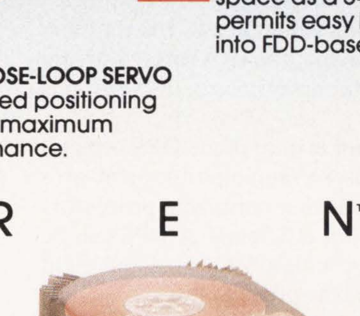

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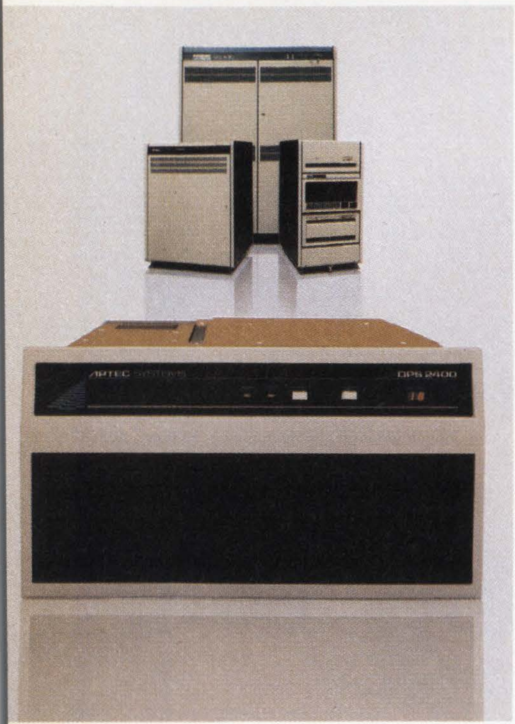

Figure 11: The DPS-2400/VAX Dimensional Processing System manufactured by Aptec Computer Systems.

VAX-11 host via Unibus. It functions as a central node of a subsystem that may include any combination of Unibus compatible peripheral devices, array processors, or other special purpose attached processors. The intent is to offload host control of array processors while providing a mass memory space which will not interfere with their processing capabilities. To do this the host computer is relieved of control overhead and issues firmware calls to the data exchange adapters (DIAs). While a typical array processor supports simultaneous I/O transfers by interleaving, the DIA sends a stream of data to the array processor even if it is busy.

The main feature of the DPS is that it allows a user to run multiple array processors and other peripheral processors at maximum efficiency. A DPS can be configured with a VAX host and eight AP-120B array processors.

Chips

Central to any array processor are the devices which perform high speed arithmetic calculations. TRW, Advanced Micro Devices, and Weitek Corp. produce commonly used chips.

TRW offers three CMOS VLSI multiplier-accumulators, the TMC2010, TMS2009, and the TMC2008. The chips are high speed 8×8, 12×12, and 16×16-bit multiplier-accumulators which operate at cycle times of 100-160 ns; the multiplier and multiplicand may be specified together yielding a 16/32-bit product. Products may be accumulated to a 19/35-bit result. The chips are built with a two micron CMOS process and are pin and function compatible with the TDC1008. TRW also has a line of 16×16 bit multipliers which operate in a 50-145 ns cycle time and are TTL compatible.

The Weitek line of multipliers have, until recently, met the 16×16 standard multiplication rates. Designed in NMOS technology and TTL compatible, the chips are used in array processing applications such as signal and FFT processing. Recent introductions are the WTL floating point multiplier and WTL 1033 floating point ALU. The chip set has add, subtract, multiply, and absolute value capabilities and handles conversion to and from 24-bit fixed point arithmetic. The chips operate in pipeline or flow-through modes and offer software portability to other floating point systems.

Advanced Micro Devices 16-bit bi-polar microprocessors are widely used. Their model AM29116 is the largest and most complex bi-polar device ever produced, with an architecture and instruction set specifically designed for intelligent peripheral controllers. The high speed was achieved by designing the part in ECL with TTL-compatible levels at the pins. All instructions are executed in 100 ns microcycle and because the chip is microprogrammable, it can emulate any instruction set.

Summary

The evolution of the commercial array processor has, in many ways, paralleled the development of floating point hardware. In the 1970s computer manufacturers developed fixed and floating point hardware for minicomputer products. These special purpose processors were associated with their operating systems and compilers. At present, one of the trends in the industry are the instances where array processors are assuming peripheral control, like displays, freeing the host computer for other tasks which increases overall system speed.

Due to the high cost and complex hardware and software architectures of array processors, system designers have not used them extensively when designing microcomputer based systems. However in some instances, chip technology such as gate array, VLSI and semicustom design have reduced the cost of array processors, especially at the board level.

Another evolution may take place in the 1980s where manufacturers will build into their products vector or array processor elements. Data General and Masscomp have already done this. Through modification to the present operating systems and compilers, these elements will become integral to computers. Currently, array processor manufacturers are incorporating enhancements and new design concepts that are moving the array processor nearer to a standalone computer. Future systems will also bring a range of operating systems and software languages. C, for instance, is already being used.

Manufacturers of conventional computers are now implementing architectures that are modular in nature, creating the potential of incorporating array processor modules directly into their systems. As these modular architectures prove effective for cost effective computing, they will gain increasing momentum as the architecture of choice. □

Array Processor Manufacturers

For more information on the following array processor manufacturers write in the appropriate number on the *Digital Design* Reader Inquiry Card.

Advanced Micro Devices	Write 300
Analogic	Write 301
Aptec Computer Systems	Write 302
Computer Design & Applications	Write 303
CSPI	Write 304
DSP Systems	Write 305
Floating Point Systems	Write 306
Marinco	Write 307
Mercury Computer Systems	Write 308
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IMAGE CAPTIONS

Top:

- *Left back corner: 2-D FFT processed in 2 minutes with LIPS Plus.*
- *Four 1024^2 medical images: multimodality, split screen display.*
- *Face: CT scans in 3-D modeling, plastic surgery at Mallinckrodt.*
- *Mountains: LIPS assists fast graphics hardware and large memory matrices with GKS-based Auxiliary Graphics Processor. Courtesy S.A.I.*
- *Pseudo-colored flowers: shows LUT manipulations. Note graphic load display plus intensity reference scale.*
- *Same 1024^2 flowers: shows color cut and paste in 1 frame time.*
- *Jars and pens: Synthetic image like #4, courtesy Pacific Data Images. Photo by Jim Weil.*

Bottom:

- *Two corners: LIPS driver supports 1024^2 LANDSAT imagery, courtesy NASA-Ames Research.*
- *Top bas relief: Matrix filter, the basis of classification and recognition. LIPS allows kernels of any shape and size and executes at video rates.*
- *Histogram: line or pixel analysis under LIPS.*
- *Spheres: fast Z-buffer merge, courtesy Rensselear.*
- *Cake and strawberries: 1024^2 looks good enough to eat.*
- *Bottom: mesh algorithm, courtesy Lunar & Planetary.*
- *Weather satellite: shows graphics overlay, courtesy MacDonald Dettwiler.*

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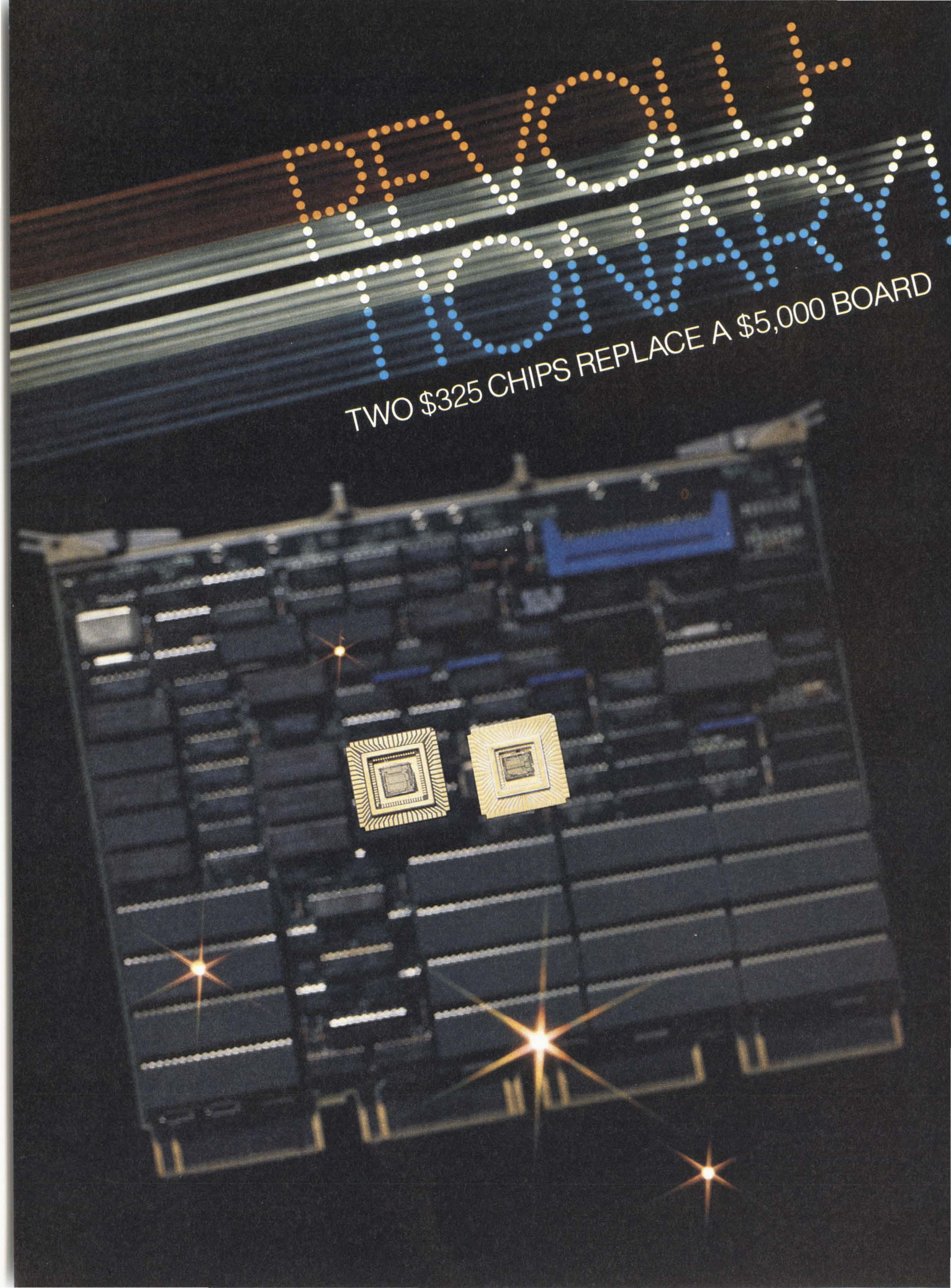
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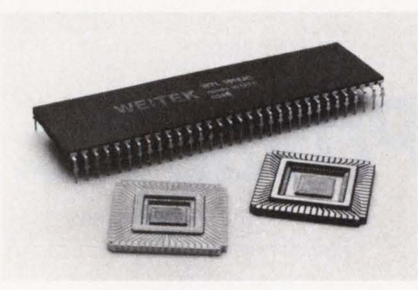

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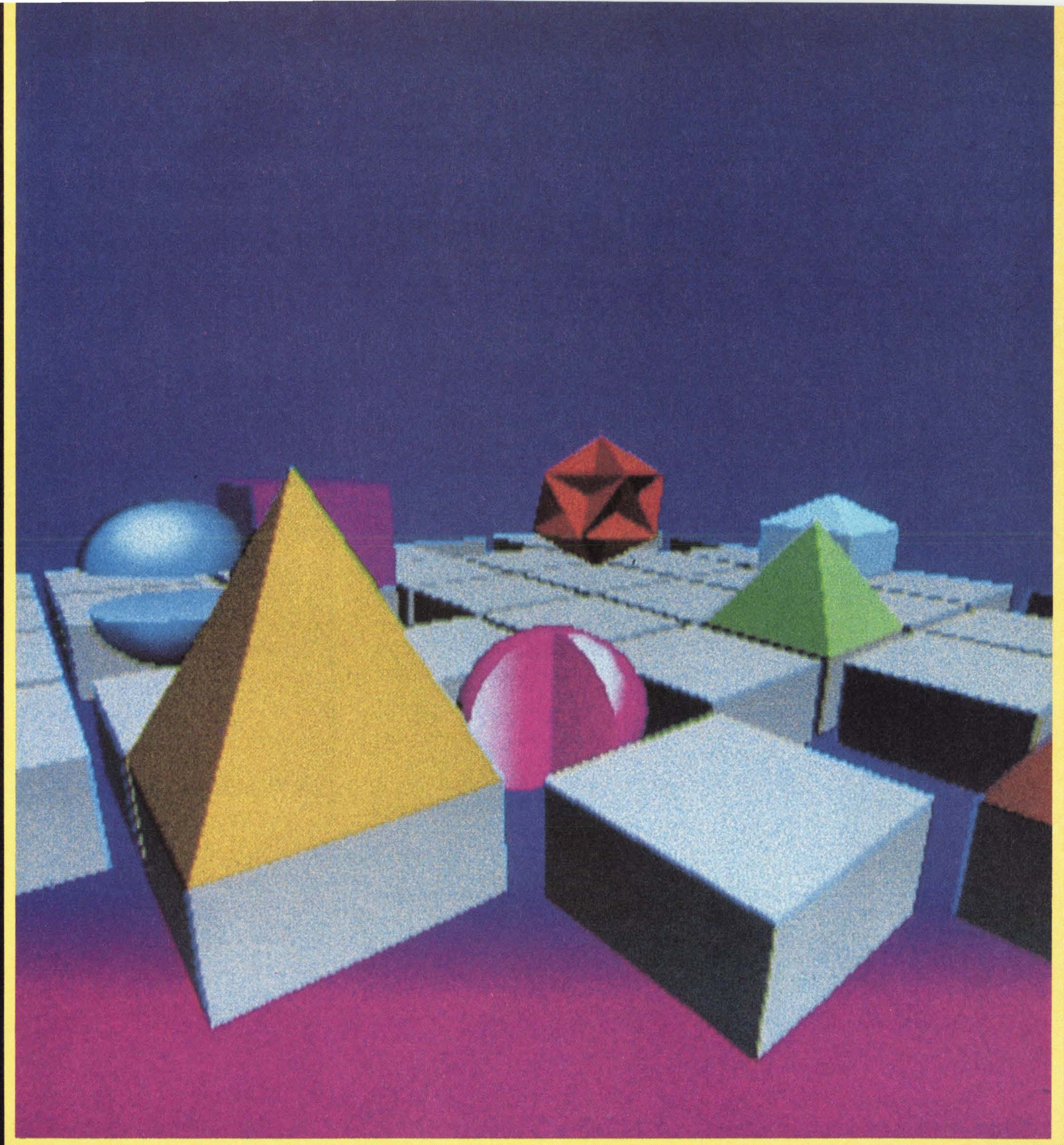

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Designer's Guide Series **GRAPHIC SYSTEMS**

Display Functions Migrate To Graphics Devices

by Jerry Borrell, Editor-In-Chief

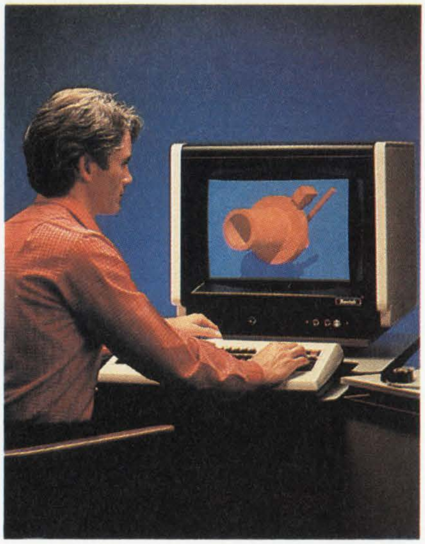
The design and integration of computer graphic systems continues to be one of the most hotly contested areas of computers and electronics. Computer graphics have two distinctions that make the area particularly fecund. First, graphics systems incorporate all of the design complexity of computer systems, but add the troublesome area of high performance analog video. Secondly, computer graphics systems are the primary area where ergonomic design – operator interface – considerations arise and are addressed.

During the 1977 to 1980 period many new manufacturers entered the marketplace. In the last two years the influx has slowed. This is due in part to the near saturation of several market niches, but also due to the high level of engineering expertise and capital needed to successfully compete. Problem areas for the designer/architect of graphic systems include: system architecture, displays, semiconductor/IC, display processor (a.k.a. picture processor or graphics processor) frame buffer and other considerations.

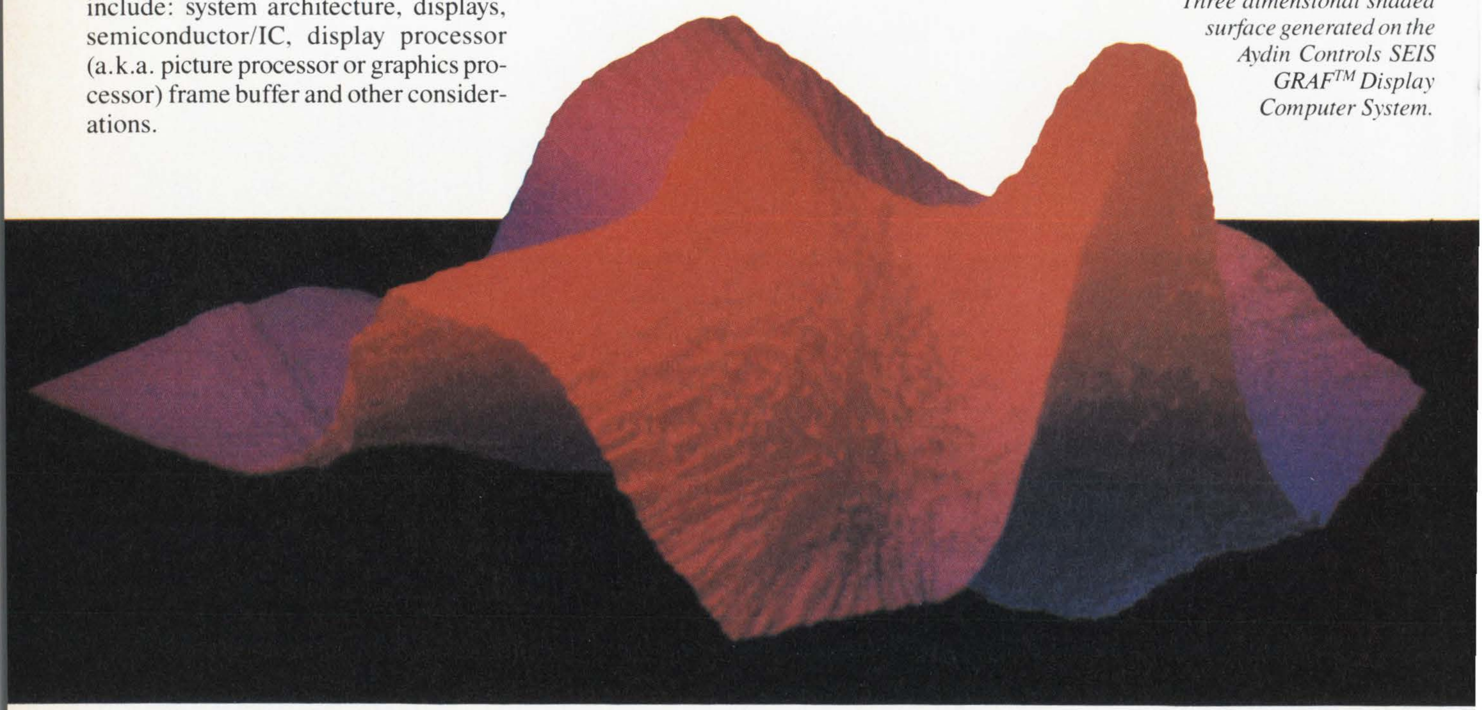
Systems Architecture

The architecture of any proposed system, from chip set to standalone system, is the first consideration from a management point of view. Issues in planning the architecture of a system include: what market the system is intended for, what performance and price the system will offer to a market, what impact the new product will have on current product lines, the hardware and software required to produce the system, whether or not the system can be manufactured reliably, and projected personnel and time requirements to bring the system into production. All of these considerations are complex in the graphics field because of requirements for peripherals such as terminals and their associated software. Further problems accrue because of the lack of quantifiable information about developing markets.

Other than the common considerations



Ramtek's Marquis display system addresses high performance graphics applications, and is based on the 9460 architecture.



Three dimensional shaded surface generated on the Aydin Controls SEIS GRAF™ Display Computer System.

> *As the demand for and the capacity to generate more sophisticated images has grown, intelligence has been added in many areas.*

such as time required to bring a product to market, its manufacturability, how it addresses a given performance range, or what flexibility to build into the system, the most common consideration in planning the graphics system has been in the choice of a host processor. The attempt to offload work from a remote CPU and provide the graphic system with greater functionality is longstanding. In 1967 T.H. Myer and Ivan Sutherland described their work in an article entitled "On the Design of Display Processors" for the Communications of the ACM. They listed four reasons for giving the graphics device more capability in this seminal work: to speed generation of pictures, to generate pictures by computation on host stored data, to provide the user with feedback and to perform dynamic related calculations.

In the course of their design work "the display processor began to resemble a full fledged computer with special graphics features," and a "strange thing happened. We felt compelled to add a second, subsidiary processor which itself grew in complexity. It was then that we discovered a disturbing truth. Designing a display processor can become a never ending cyclical process." This remains the case for high performance system manufacturers today. We see logical units in the architecture of a graphics system consisting of a host, graphics processor, frame buffer, and subsystems for memory, display, and interaction. As the demand for and the capacity to generate more sophisticated images has grown, intelligence has been added in many areas much as was the case with the display processor.

Today the traditional display processor's tasks are divided into raster processing, vector generation, software or firmware processing, and in some cases data base processing and interaction. The breadth of the architectural issues faced in designing a graphics system becomes more clear when functional units of the system are considered separately.

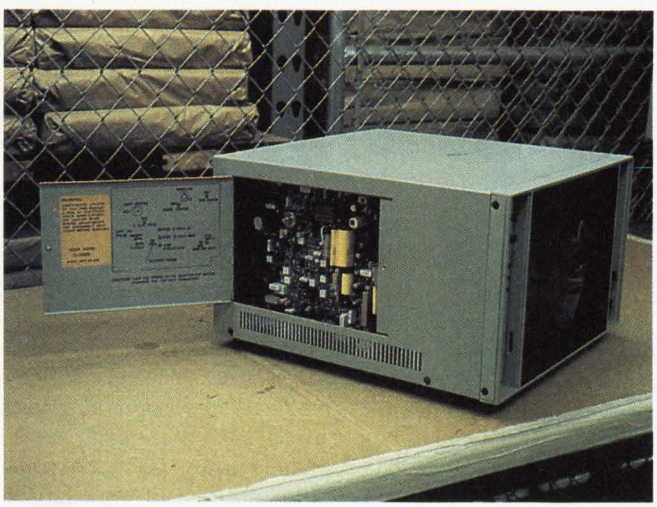
Displays

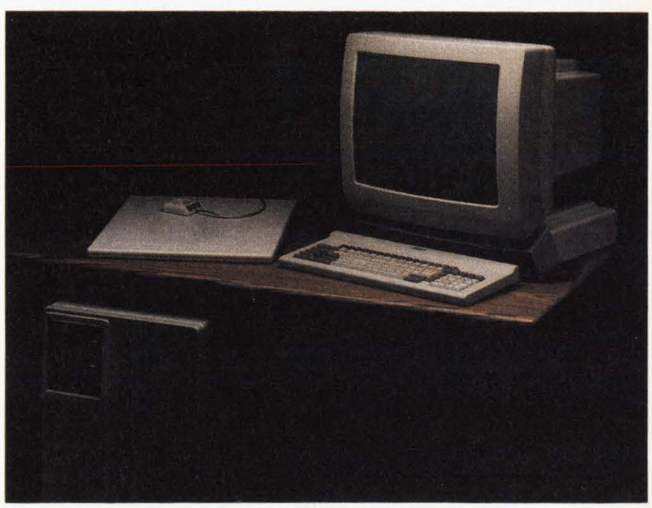
The design and integration of a display may be viewed from two perspectives: that of the CRT manufacturer and that of the integrator. In the case of Intergraph (Huntsville, AL) and Aydin (Fort Washington, PA) these coincide, as the manufacturer does both. Other graphics manufacturers have attempted to do both but since decided to abandon the effort.

The perspective of the display manufacturer is that graphics systems designers often develop the architecture for a system and shop for displays after the fact. In their eyes, when digital engineers who lack analog experience make decisions about video, problems are compounded. They point out two results. First they must perform a great deal of custom work. Fully 50% of Conrac's (Covina, CA) production is done to specification for the OEM. A second result is what they see as the inability of "the systems manufacturer to support graphics processing at promised" performance. The latter is often the origin of very difficult display modifications. The display producer is often pressured to increase performance. The request for 60 Hz vertical refresh rates and 1280 × 1024 resolution are examples which they say are unjustified by the system's capability or operator requirements. They express frustration at being pressed to advance analog technology at a rate similar to that of digital systems, when they feel there is no quantifiable reason to do so.

Graphics system designers' perspective is that one of the worst design constraints for advanced systems is the display. They feel able to produce and offer 1280 × 1024, 60 Hz refresh systems despite a shortage of similarly powerful displays. Furthermore, they note that semiconductor advances will allow them to push performance rates upwards to 2000 × 2000 at 60 Hz, but that there is little likelihood of having displays with such capacity. Reliability is beginning to have an impact on systems; at least one of the five

FCC requirements for shielding may require changes in overall system design due to heat related problems. Conrac's EMI-free packaging is shown. Saber Technology Corp. has recently entered the workstation market with its "Saber Station." The company's 1664 × 1248 monochrome displays will be one of the highest resolution available.



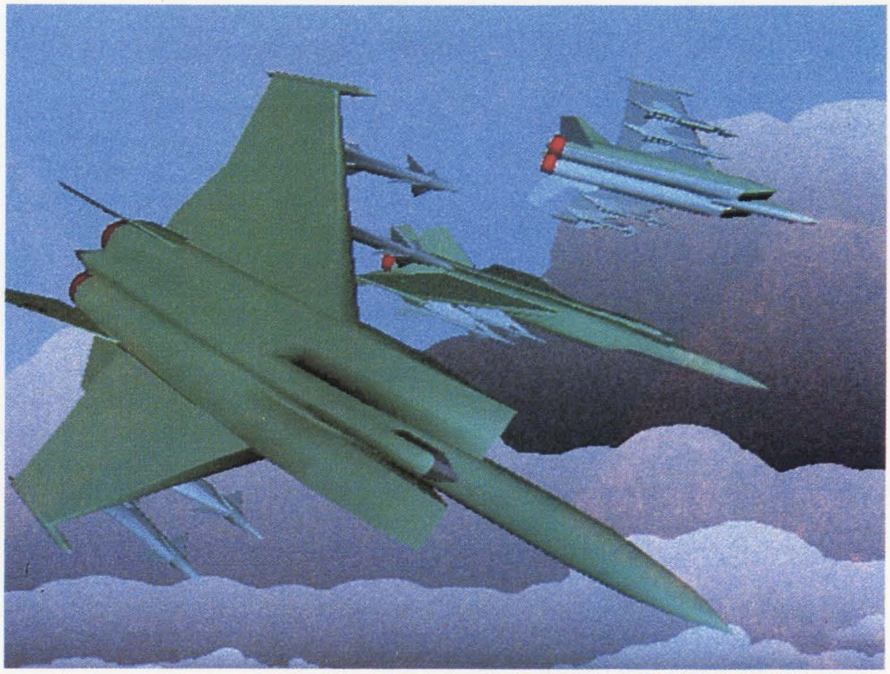


largest producers of CAD systems is said to be having field failures of high performance displays.

Both parties agree that there are questions at present about the ability of current high performance CRTs to withstand long term use, primarily due to heat caused in horizontal beam deflection. There is disagreement on a solution to the problem, and the shielding requirements of the FCC may cause further heat related problems.

Semiconductors

Several basic design issues involving semiconductors must be addressed, beginning with the cost/performance trade-off. In the past these decisions were more straightforward because of the limited number of semiconductor devices supporting graphics and because systems were less complex, e.g. terminals, graphics cards, and display processors. As more functionality has migrated to the graphics system from software supported on a mainframe or minicomputer, the number of design decisions to be made has increased. Today some systems that may be called terminals in that they are host supported, are more properly called display systems because of their capabilities. Similar changes at both the device and board level make architectural considerations problematic, even at these levels.



Cubicomp's CS-5 graphic system, one of the lowest price display systems available is based on the IBM PC. Picture by Peter de Vroede.

Given these changes, even low cost terminal designs incorporate the latest 16 and 32-bit processors and thus require the architect to plan for device availability, associated products such as floating point or coprocessors, future processors, and the availability of software development tools. As systems become more complex, a majority of graphics manufacturers have broken their designs into functional subunits, the CPU becoming only one of the considerations.

As off the shelf processors have become more powerful, most manufacturers have chosen standard products because of second source availability, well documented support tools, and name recognition. At both extremes of performance, high and low, the selection of the CPU has begun to reflect a broadening of options. At the low end, for example, value is added at low cost by combining TTL logic parts to create a custom processor. At the high end, bipolar processors, full-custom devices, PAL/PLA, and increasingly, semi-custom devices are implemented.

In many cases the Motorola 68000 and Intel 8086 family have been chosen because of the reasons described above. They sacrifice in performance of graphics functions, but provide flexibility to the user by having a greater range of applications. In light of these trade-offs, the designer must have a firm grasp of the final use envisioned for the system: as a terminal or as a standalone workstation. The design factors change as either graphics displays or more general computational tasks are sought.

The general purpose CPU, most often the 68000/68010 used in workstations,

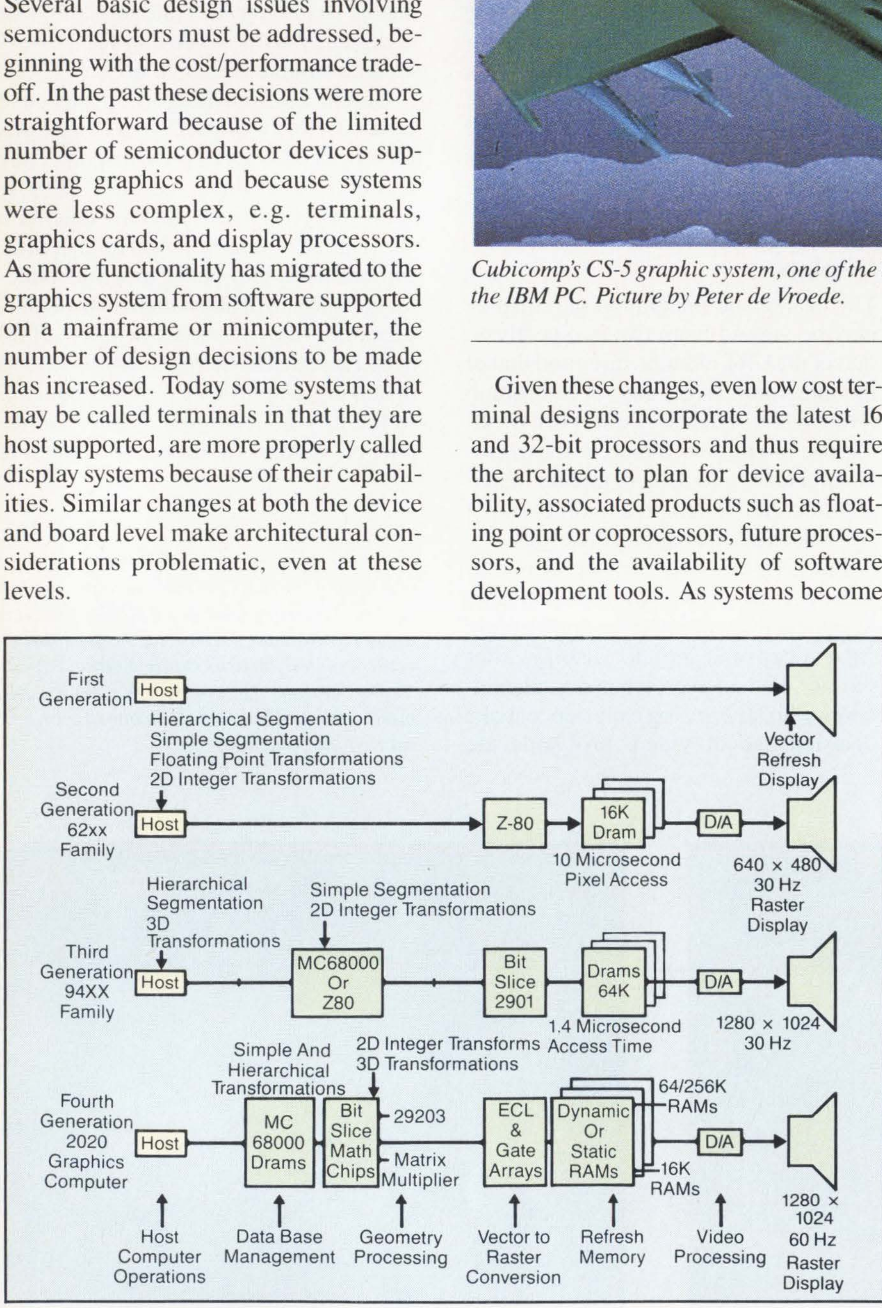
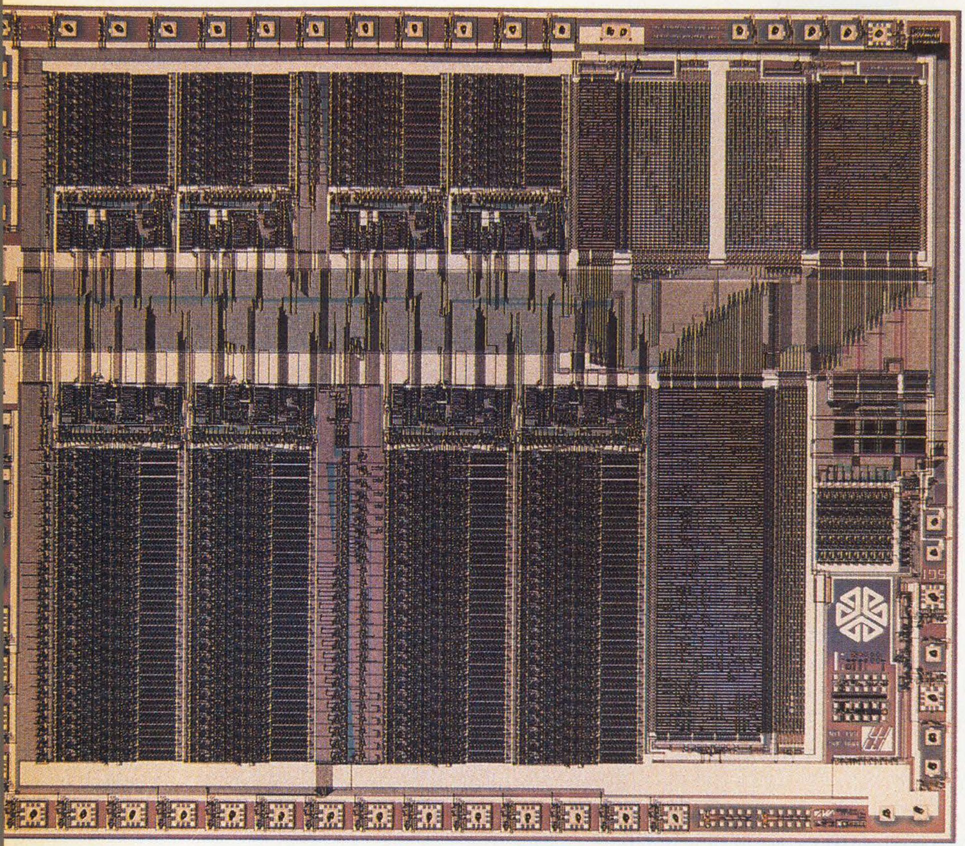
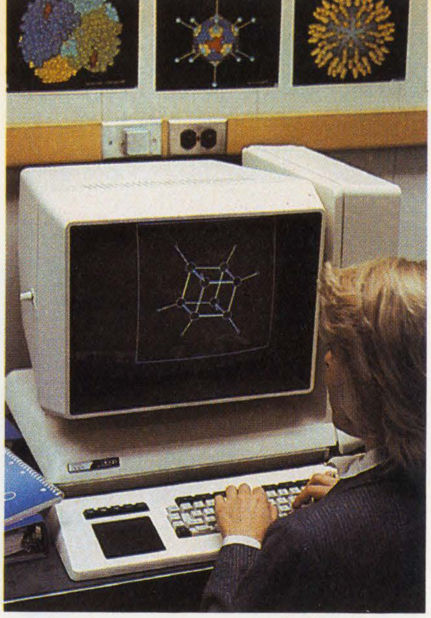


Figure 1: A depiction of the evolution of display processors — courtesy Ramtek.



Custom graphics processor – "The Geometry Engine" developed by James Clark at Stanford University: 10 to 12 of the chips are used in the IRIS System.



Apollo's workstations have found use in direct applications such as molecular modeling and integration into turnkey systems.

has suffered due to a lack of an equally powerful coprocessor, a situation that Motorola is said to be addressing in the near future. The 8086 family has been more successful in this light because of the 8087 co-processor which offers the advantage of easily implemented floating point functions. National's 16032 family, just beginning to appear in systems such as the Syte 3000 line, offers supporting floating point and memory management units.

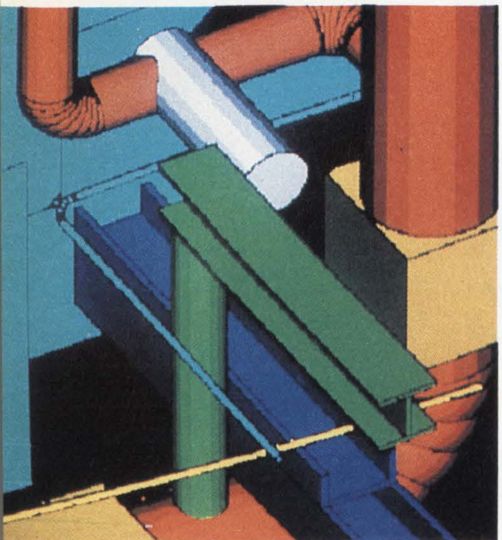
Floating point and memory management become important in graphics functions because of the former's importance in matrix multiplications and the latter's ability to deal with large memory spaces. Memory management, however, has typically been dealt with by the assignment of memory controller support chips. 16- and 32-bit processors address large amounts of direct memory, as well as external program/instruction stores. As this need for external program and data memory increases with the functionality of the system, so has the need to provide memory management.

At these highest levels of performance, systems functions have gradually begun to migrate into supporting units. The accompanying diagram from Ramtek, **Figure 1**, shows that this has occurred not only in the separation of terminals from the host, but of functions away from the graphics system CPU. Some high performance systems announced at the NCGA and SIGGRAPH trade shows this year demonstrate this migration of functionality into the areas below: vector and primitive generation, frame buffer, and display processor. Factors supporting this transition include the availability of development and programming tools that allow an easier transition to instructions in firmware.

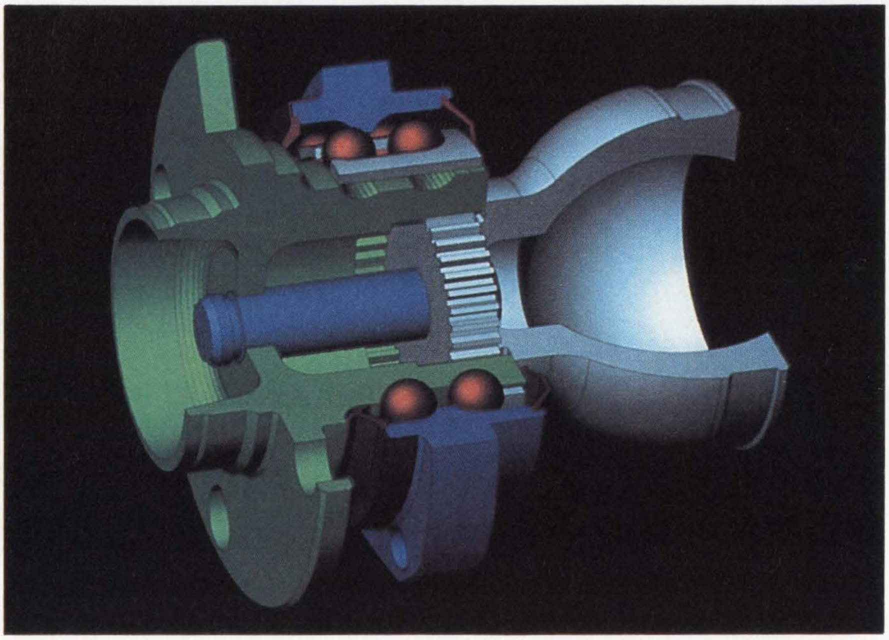
Some manufacturers, however, have selected off-the-shelf graphic processors as the most cost-effective solution. Chips such as the NEC 7220, Intel's 82720 and the Motorola 6845, are found in many manufacturers' products. These devices have allowed the designer to bring a graphics product to the marketplace more quickly, but may place limits on its range of functionality. The NEC/Intel device, for example, provides for geometric primitive drawing functions, certain grey scale and color manipulations, and basic manipulations of the screen such as pan and zoom. While this chip requires support from CRT controllers, it simplifies the task of providing basic graphics functions. In low performance ranges such as terminals, the designer is freed from microcoding or downloading those basic capabilities.

During the next year other graphics processors will likely be available, including devices from Texas Instruments (Austin, TX) and Thomson CSF (Canoga Park, CA). The most promising products are those from Silicon Graphics and Weitek (Santa Clara, CA). Silicon Graphics' IRIS system is based upon Jim Clark's design for a geometry engine but will not be sold to manufacturers except as incorporated into the system. The Weitek graphics engine based on the tiling engine and floating point board sets offers advantages to the system level integrator in the near term on a board level, and is currently being reduced to a chip set for even greater efficiency in the long term. Manufacturers who have chosen to remain with general purpose processors point out the limitations inherent in silicon architectures. If, for example, one wanted to make use of a new approach or algorithm for rendering surfaces such as bi-cubic patches, use of a graphics chip would probably require the user to offload the task onto the host.

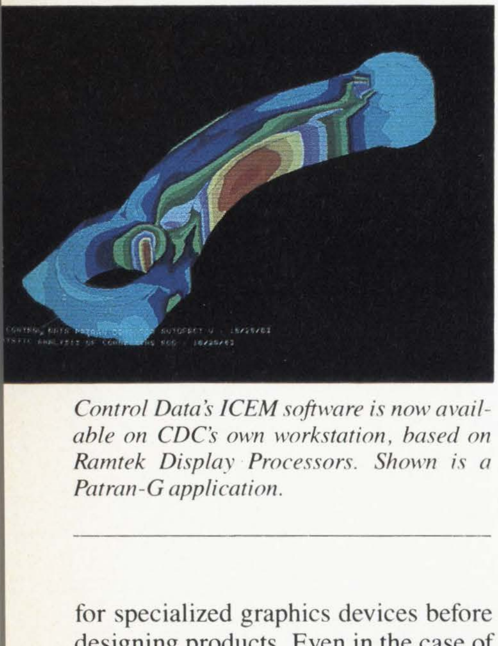
Few manufacturers have elected to wait



Solid modeling generated on a 68000 based IBM desktop, with Cat Solid software. Courtesy of T.R. Binion, Catronix Corp.



Magi's Synthavision demonstrates performance features which shape display system design: lighting, texture, shading.



Control Data's ICEM software is now available on CDC's own workstation, based on Ramtek Display Processors. Shown is a Patran-G application.

for specialized graphics devices before designing products. Even in the case of high performance systems, the need to establish a market presence has led designers to use off-the-shelf parts in the architecture of a processor. The most frequently chosen solution has been to develop a device based upon AMD's bipolar bit slice family. The AMD2901 ALU has been a favorite because it was designed to allow flexible integration for different word lengths. Some processors use only two of the family, for an 8-bit device; others, notably Superset, uses 12 for a 48-bit word length processor.

There are alternate approaches to improving processing of both graphic data and graphic interaction, including the use of semicustom technology (gate arrays and standard cells), as well as work being done by Henry Fuchs that would disperse system intelligence. To date, however, few gate arrays have been designed for graphics functions specifically; rather they are applied to general computing functions.

Display Processors

As was pointed out earlier the definition of the display or picture processor has changed a great deal in the past decade. The demand for greater graphics functionality, and the availability of powerful semiconductor processors has given architects the ability to address higher performance in terms of color, dynamics, generation of primitives, and other functions with dedicated hardware. One problem in this becomes immediately evident – to retain competitive system capability, the graphics system manufacturer will have to focus on hardware applications for graphics.

This has left a gap in the market successfully addressed by more generalized workstation manufacturers such as Apollo, Sun, Perq, Symbolics, Cadmus, Masscomp, and others. One way in which these manufacturers have sought rapid entry into the highest levels of performance has been to add display processors from Lexidata, Raster Technologies, and Metheus. The pressure from these collaborations in turn causes manufacturers such as Megatek, Ramtek, Adage (Ikonas), Genisco, and Evans and Sutherland to increase the performance of their dedicated graphics systems.

Among the demands shaping display processor design are those for speed of drawing, dynamics, color, rendering (lighting, shading, and texture), and windowing. As is shown in the diagram from Ramtek, all of these functions have migrated from the host processor by the fourth generation. As they began to be performed within the graphics device, it became ineffective to use the core memory of a mainframe for both program and display bit map memory. This gave impetus to the design of a separate, display related memory which we most often call the refresh memory.

As display technology made a transition from vector refresh or stroke displays to its current domination by raster devices, one function of the display processor became paramount: converting point and line segment information into a bit map format. As secondary processing tasks accumulate, as is the case in providing graphics displays that have three dimensions, the use of a single processor to perform all calculations becomes im-

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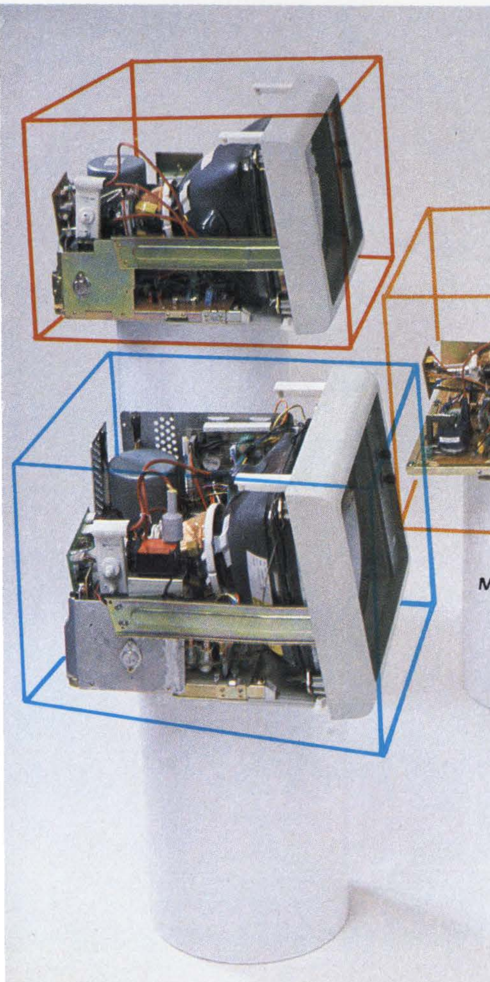

HX-12 SPECIFICATIONS

CRT	12" Diagonal, 76 degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface (NEC 320CGB22)
Input Signals	R, G, B, channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video Bandwidth	15 MHz
Scan Frequencies	Horizontal: 15.75 KHz Vertical: 60 Hz
Display Size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 240 lines (non-interlaced) 480 lines (interlaced)
Misconvergence	Center: .6mm max Corner: 1.1mm max
Display Colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows—8x8 dots)
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

MAX-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor)
Input Signals	Video signal, Horz Sync, Intensity—positive TTL levels, Vertical Sync—negative TTL levels
Video bandwidth	18 MHz
Scan frequencies	Horizontal: 18.432 KHz Vertical: 50 Hz
Display size	204mm x 135mm
Resolution	Horizontal: 900 dots Vertical: 350 lines
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

SR-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface
Input Signals	R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video bandwidth	25 MHz
Scan frequencies	Horizontal: 31.5 KHz Vertical: 60 Hz
Display size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 480 lines (non-interlaced)
Misconvergence	Center: .5mm max Corner: 1.0mm max
Display colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows)
Input Connector	9 Pin (DB9)—cable supplied

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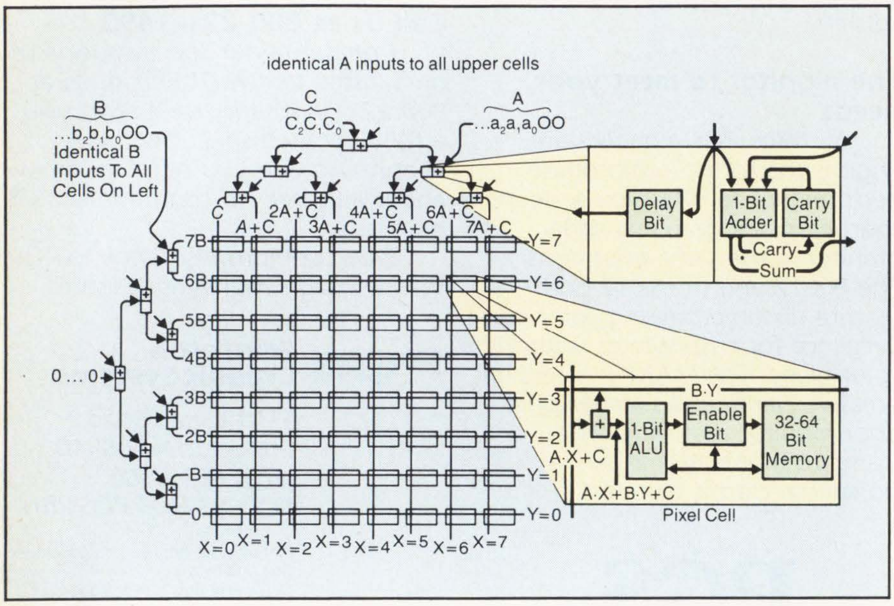


Proposed design for a future frame buffer by Henry Fuchs, Ph.D., Professor of Computer Science at the University of North Carolina. An 8 × 8 pixel-plane image buffer memory chip; Scan conversion, hidden-surface elimination, and color rendering commands are translated outside the memory system into A, B, C coefficients and assorted pixel-planes commands.

practical. This explains why Myers and Sutherland wanted to add a second processor over 15 years ago. By the second generation of the accompanying diagram we see a separate vector to raster conversion processor. By the third generation, bit slice processors were used to perform the conversion tasks. The bit slice devices became important in such tasks because of their ability to be micro-programmed for specific functions or combined for different word lengths.

However, by the third generation, tasks relating to dynamics and two dimensional display processing (matrix mathematics) also moved into the local graphics devices, absorbing much of the functionality of the device display processor. Graphics manufacturers reached this stage several years ago, and it was then that demands for rendering of displays in color, provision of three dimensional operations such as perspective operations, hidden line removal, shading and texture began to move into the graphics system from the mainframe.

Bringing these functions into a graphics display system has been the hall-

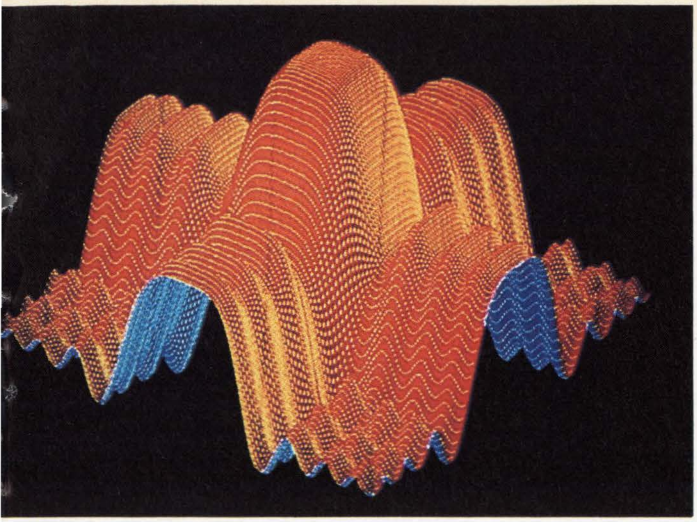


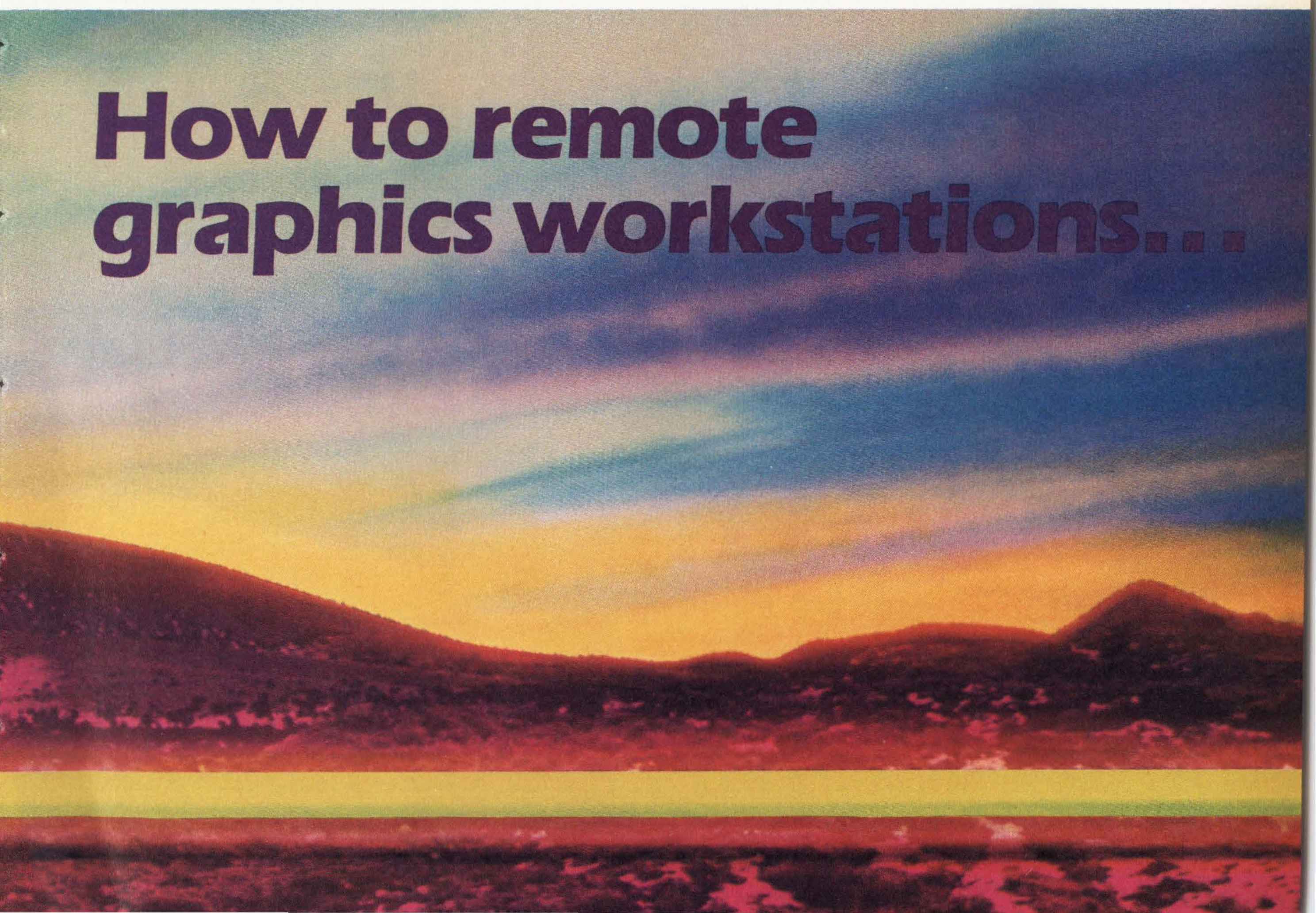
Photo Courtesy of Ridge Computer – supported by Metheus Corp. 400 graphics processor.

mark of fourth generation display systems. It requires the addition of yet another logical unit in the system which would perform three dimensional calculation. This portion of the system is most often referred to as the geometry processor. While manufacturers such as Ramtek and Megatek have designed and built their own geometry processors, others such as AED or Lexidata who are competing at the highest levels of performance must add devices such as array processors from CSPI or Sky Computers.

The computational tasks are so complex today that the original "display processor" has become a 16/32 or 32-bit processor which performs data base management functions. The geometry processor may be built up from bit slice and other devices such as multiplier chips, or purchased as mentioned for integration onto a system bus. To add even more software functionality at the local level, the former vector generator now takes on functions such as control of the frame buffer memory and performing final rendering upon data before sending it to the monitor via video processing.

Two years ago, Lexidata began a race for display algorithm functionality at this level with the Solidview processor; its alternate pixel illumination technique provided hardware-based transparency. Ramtek fired the second salvo in this performance war last year with its 2020, and lowered drawing times for the average pixel to below a microsecond. This year Phong and Gouraud shading as user selectable functions for the vector generator are being shown.

The competition for performance at these levels includes parameters that are not open to ready comparisons. At the base of these systems are computers that rival those made available for general purpose computing. Added to these are several other computers which perform specialized computational tasks, and an increasing body of firmware that relieves



How to remote graphics workstations...

a mini or mainframe computer of all tasks but managing larger data bases than are useful to maintain for a single workstation. Each manufacturer, integrator and applications engineer has to weigh the architectural considerations outlined earlier for a whole series of complex subsystems to make a final evaluation for the overall system.

It is in this area that semi-custom devices are being applied to board level integration. The obvious advantages of less board space, lower power, and greater speed counter the high cost of the limited numbers of these devices that will be produced. For the highest performance, gate arrays may provide operations that were not previously practical at a local system level. It almost goes without saying that ECL logic is used where the demand for performance is paramount.

While some manufacturers claim that raster drawing speeds are still not equivalent to those of vector drawing systems, the demands of users for shaded images may make such comparisons less pertinent.

Frame Buffers

As the display processor moved closer to the display, memory was needed to support the higher performance. The memory for raster display systems provides a variable number of bits for each pixel to be displayed. The distinction between the display size addressable and that which is viewable is, at times, quite confusing. Given that monitors available in production quantities are limited to 1280 × 1024 viewable pixels, a system such as Genisco's or one from Tektronix with 2048 squared pixels available still only has a certain number viewable at any one time.

Even during the second generation of display devices, with bit map arrays of memory as low as 512 squared or 680 × 480, the cost of memory becomes significant. Many techniques have been implemented such as run length encoding, and cell encoding to decrease the amount of memory required for the bit map, but rendering displays with color, shading, and now with Z-buffer functions demands enormous amounts of memory. In a 512 squared plane of bit map, for example, 262,144 bits of memory are required. The increase to 1024 squared requires one million bits of memory per plane. A three plane system, which would support only eight colors, then, would require three-quarters of a Mbit of memory for 512 squared display. Most graphic displays require eight to 16 planes of memory, some use 22 to 24 (Raster Technologies). Imaging systems typically have 32 bit planes, and those custom systems used in commercial animation may have up to 64 bit planes.

Not only does the physical cost per bit become a prohibitive factor in designing a graphics display system, but the time required to access all values for each pixel presents a more confining bottleneck. The successful implementation of 64K dynamic RAMs by Raster Technologies was one important reason why that company was able to reduce costs for their systems. However the 64K RAM chips have only a one bit data path, making access time a bottleneck. Designers then are faced with three crucial considerations in display memories – how to increase speed, manage bandwidth, and keep costs competitive.

Several techniques have been used to lower memory costs for the frame buffer. Color look-up tables are the most widely used. These tables are intermediate memory locations that allow color assignments to be made for combinations of locations. Thus a wider color gamut is provided with less physical address space. The trade-off is made in the additional time required for intermediate processing. It may, however, be least costly to provide additional intelligence in the frame buffer to speed processing via the look-up table.

Another approach is to have wider bit paths available on RAMs. At present, 16K by four bit RAMs are available, and 64K by four bit RAMs are to be available during 1984. However, most designers want an 8-bit channel that would allow a more direct path for color systems based on 8 bits of value (256 colors). 256K RAMs will primarily serve CPU functions, but graphics applications less sensitive to fast refresh will implement the devices, as well.

A third, most intriguing approach is that of architects and designers working on future frame buffer designs. Several sources are pondering a "pixel per processor" approach. One such design is that of Henry Fuchs, Professor of Computer Science at the University of North Carolina.

Summary

The pixel per processor approach brings the designer back to what Myer and Sutherland called the "Wheel of Reincarnation" in their 1967 article, "On The Design of Display Processors." Their point was that, having made a successive round of enhancements in the design of what they then called a display processor, the system had achieved a greater performance level. To initiate performance increases in some portion of today's complex systems, this cycle of enhancements at several levels will need to begin again.

Displays, display processors and frame buffers appear to be the graphic specific issues that architects are dealing with. Other issues such as open systems architectures (VME, Multibus, etc.), interface to peripherals or subsystems, and improvements in semiconductor devices are also critical to graphics system design. Each of these promises to become more active before next season's conferences, as processors, memories, software developments, and architectural developments progress. □

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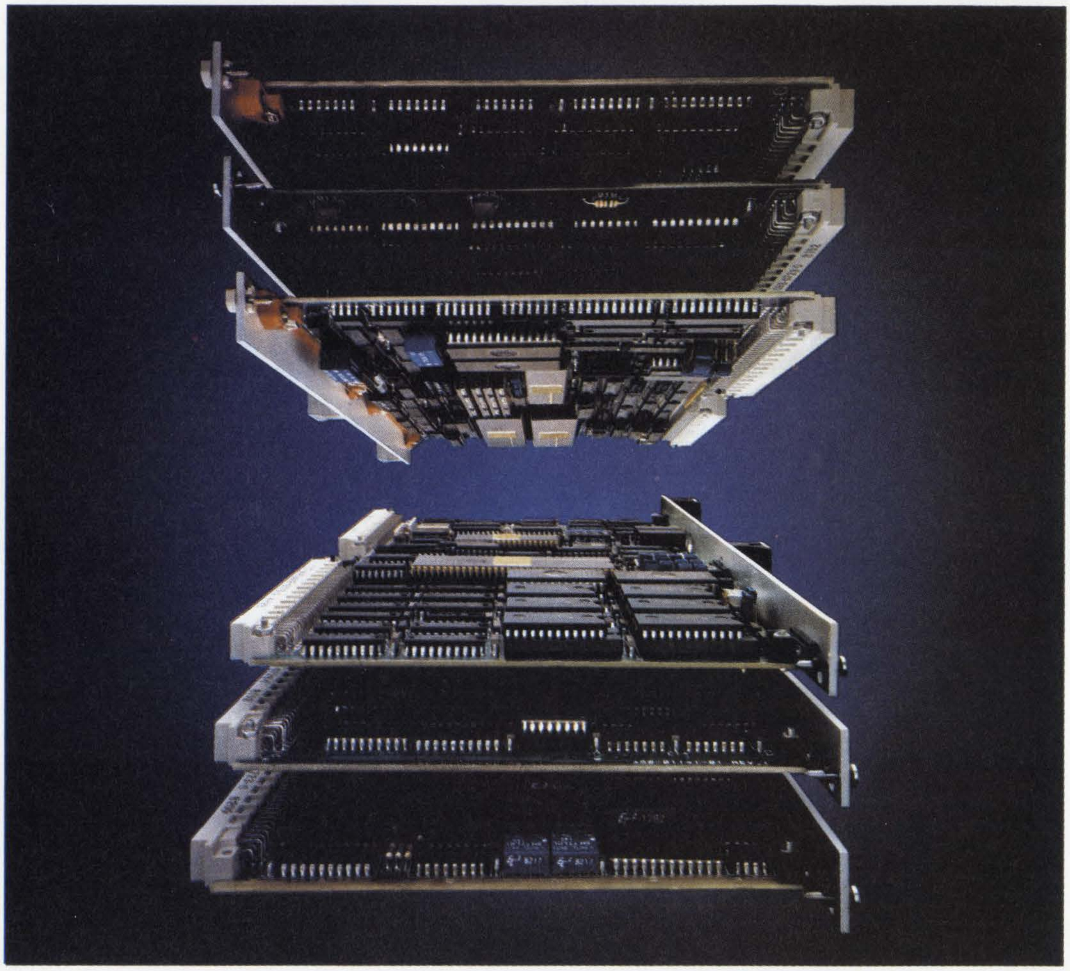
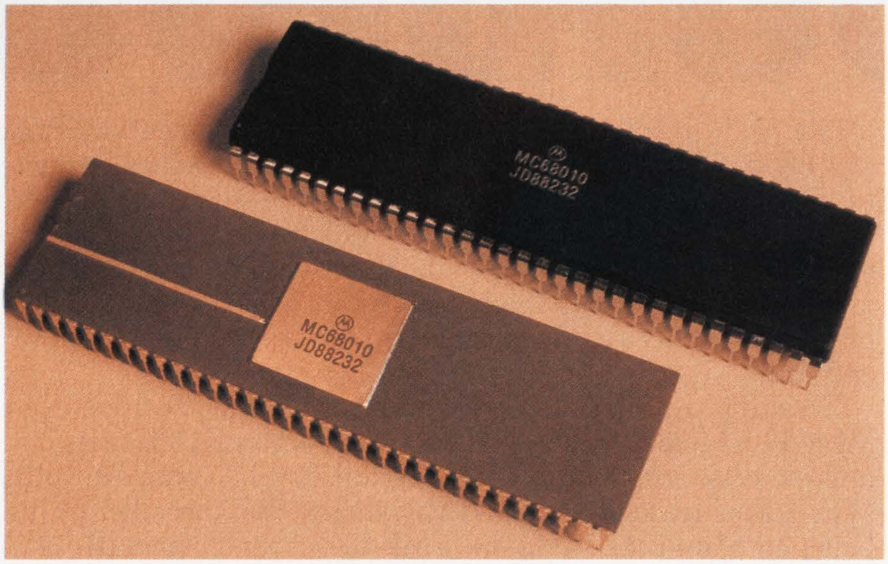


A Family Of 68000s Handles The High-End

An instruction continuation method of virtual memory coupled with processor isolation from fault detection devices makes the programmer see only actual errors.



Motorola's 68000 and 68010 microprocessors.

by Dave Wilson,
Senior Technical Editor

When the MC68000 microprocessor was first introduced, it was only embraced by the high-end marketplace due to its performance characteristics and relatively high cost. Today, that market picture has changed dramatically. As the 68000 itself continues to drop in price, it has won a place in more business/personal computer designs, the most obvious one in recent months being the Apple Macintosh. This illustrates that criteria that once defined the high-end marketplace are now being implemented by lower cost machines.

Soon after the 68000 entered the market, a version of the processor that ran on an 8-bit bus came out. The 68008 is internally identical to the 68000, except for additional circuitry that folds the data bus in two. This means that most instructions run in half the time they would on the 68000, and some run even faster than that. At present, the 68008 is suited to run in home computers or as a communications or I/O controller in a distributed processing environment. In the latter application, the simple fact that all code written for the 68000 will run on the 68008 should cut design time dramatically for those considering such a controller for a 68000-based host.

Next out was the MC68010 microprocessor, which was an upgrade to the MC68000. In general, this product adds complete virtual memory capability to the MC68000, but also has some new instructions and other features.

This year, Motorola will announce its next generation 68000 machine, the 32-bit 68020. The treatment of virtual memory and a virtual machine introduced in the 68010 is extended for the 68020. No new or different methods are employed in the new part, the same techniques are simply expanded to cover new instructions and capabilities that it has over the 68000 or 68010.

The performance of a CPU, however, is only one of many considerations that need to be addressed when choosing a processor for system design. Another is the availability of support devices, such as memory management units, floating point units and DMA controllers. Recognizing this, Motorola has signed several agreements with Signetics, Mostek, Rockwell and Hitachi that have, and will result in a broad range of support devices for the MC68000 (**Table 1**).

Memory Management

Processors and peripherals in the MC-68000 family pass information over an asynchronous bus (**Figure 1**). The asynchronous nature of the data bus breaks the memory system's tie to the system clock, eliminating timing concerns due to signal skewing and unevenly balanced or long PC board traces, and simplifying memory access circuitry. Another advantage is the ease with which a virtual memory system may be designed.

In a virtual memory system, a user program can be written as though it had a large amount of memory available to it when only a small amount of memory is physically present in the system. A memory manager under the control of the operating system allocates and protects the different portions of memory

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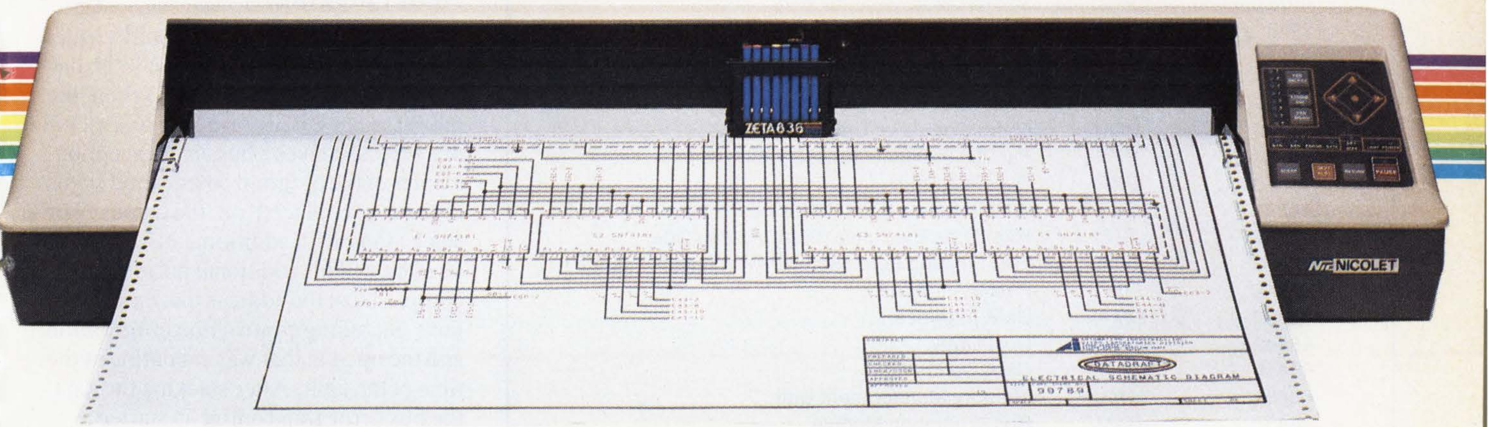

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MC68000 FAMILY DEVICES

PART NUMBER	MNEMONIC	DESCRIPTION
68000	CPU	16-bit Microprocessor
68008	CPU	Reduced bus (8-bit) Microprocessor
68010	CPU	16-bit Virtual Memory Microprocessor
68012	CPU	16-bit Virtual Memory + Microprocessor
68020	CPU	32-bit Microprocessor VM with Cache
68120	IPC	Intelligent Peripheral Controller
68121	IPC-NR	IPC with no ROM
68122	CTC	Cluster Terminal Controller
68153	BIM	Bus Interrupt Module
68172	E-BUSCON	VME Bus Controller
68173	S-BUSCON	VMS Bus Controller
68174	E-BAM	VME Bus Arbitration Module
68200	MCU	Micro-Computer Unit
68230	PI/T	Parallel Interface/Timer
68340	DPR	Dual Port Ram
68341	IEEE FP	IEEE Floating Point (Software Package—M68KFPS)
68342	RTE	Real Time Executive (Software Package)
68343	FFP	Fast Floating Point (Software Package M68KFFP)
68345	FIFO	First In/First Out
68430	DMAI	DMA Interface
68440	DDMA	Dual DMA
68450	DMAC	DMA Controller
68451	MMU	Memory Management Unit
68452	BAM	Bus Arbitration Module
68454	IMDC	Intelligent Multiple Disk Controller
68459	DPLL	Disk Phase Locked Loop
68465	FDC	Floppy Disk Controller
68485	RMC	Raster Memory Controller
68486	RMI	Raster Memory Interface
68561	MPCC-II	MultiProtocol Communication Controller II
68562	DUSCC	Dual Universal Serial Comm. Controller
68564	SIO	Serial Input Output
68590	LANCE	Local Area Network Controller
68605	SDMA	Serial DMA
68652	MPCC	MultiProtocol Comm. Controller
68653	PGC	Polynomial Generator Checker
68661	EPCI	Enhanced Programmable Comm. Interface
68681	DUART	Dual Universal Async. Receiver/Xmitter
68802	LAN-802.3	Local Area Network (IEEE 802.3 Std.)
68851	PMMU	Paged Memory Management Unit
68881	FPCP	Floating Point Co-Processor
68901	MFP	Multifunction Peripheral
68920	MAC	Memory Access Controller

Table 1: The 68000 family of processors and peripheral devices.

and I/O, flagging the processor when improper accesses are attempted. The MC68451 memory management unit (MMU) is the basic element of a memory management mechanism (MMM) in a 68000-based system.

The mechanism partitions the logical address space into continuous pieces called segments. Each segment is a section of the logical address space of a task, mapped via the MMM into the physical address space. Tasks may have any number of segments and segments may be defined as user or supervisor, data only or program only or program and data. They may be accessed by only one task or shared between two or more tasks. In addition, any segment can be write protected to ensure system integrity.

During normal translation, the MMU translates the logical address provided by the 68000 to produce a physical address that is then presented to the memory array. This is accomplished by matching the logical address with information stored in a descriptor and then mapping it into the physical address space. A descriptor is a set of six registers which describe a memory segment and how that memory segment is to be mapped to the physical addresses.

If more than 32 descriptors are needed for performance enhancement reasons, multiple MMUs may be configured in a system. The number of 68451 MMUs used is not logically constrained, but in practice, only six can be used without external buffering, due to buffer drive limitations. A circuit design showing two MC68451s in a system with the 68000 is shown in **Figure 2**.

Fault Flagging

Systems with data integrity and virtual memory are possible with the 68000, due to the bus error indicator. When the 68000 sees a BERR response to a memory access, it takes a bus error exception. Copies of the program counter and status register are placed on the supervisor stack along with additional bus error information. This additional information is comprised of the address that caused the fault, including control line information and the opcode that was executing at the time of the fault. After stacking the data, the bus error trap routine is started.

The information placed on the stack by the 68000 is not sufficient for the same processor to recover from bus faults, though a second processor can do so. The processor can, however, analyse the cause of the fault, log it and cancel the routine that faulted without destroying any data that has already been processed.

In the 68010 Virtual Memory Microprocessor, the function of the bus error has been expanded to permit complete single processor virtual memory systems. In the 68010, not only can bus faults be flagged, but they can be straightened out by the operating system. The mechanism in the 68010 allows not only memory management faults to be handled but also data errors and memory chip faults.

In the MC68010, when a BERR handshake is returned, not only the bus error information is stacked, but also the entire internal state of the processor. This internal state information contains bits and bytes of temporary registers, status codes, pointers and previously fetched instructions and data used by the microcode, bus control and execution units of the processor.

Once all the BERR information and the internal state information is stacked, the processor again begins the bus error trap routine. In this routine, a virtual memory system would determine the nature of the fault. If it was a virtual fault, the processor would determine which blocks of data can be put back on the disk, put them there, determine which blocks of memory need to be put into primary RAM and bring those in off the disk.

Once the memory manager is updated

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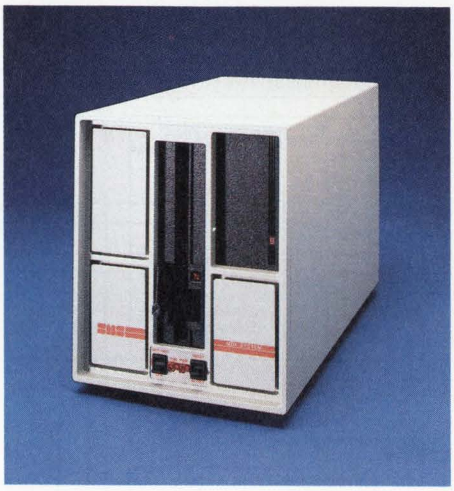

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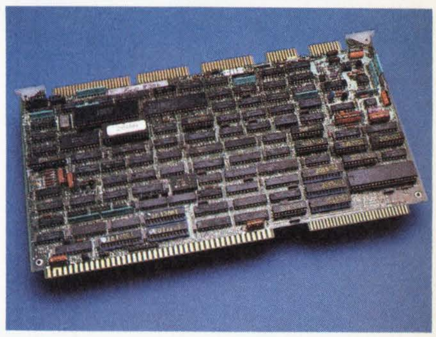

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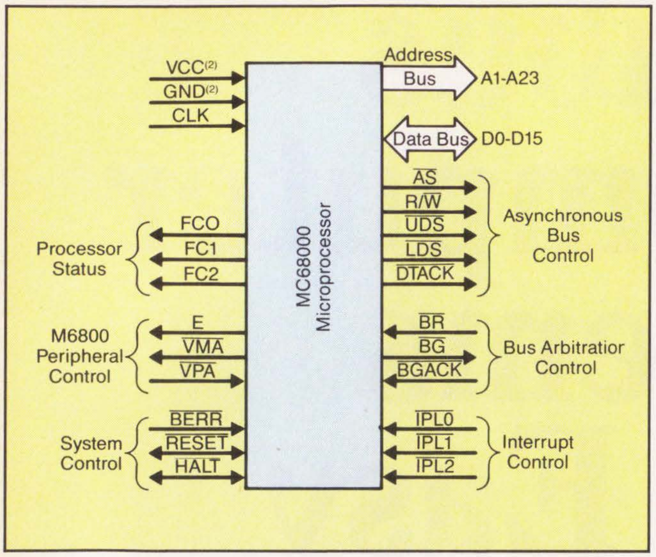

Figure 1: Input and output signals of the 68000.

to include the changed blocks of memory, the processor prepares to return to the faulted routine. Simply by executing the RTE (return from exeption) instruction, the 68010 will automatically recover all of the saved internal state information from the stack. This is placed back in its original locations within the processor, returning the processor to the same state it was in when the fault first came in. The processor then again attempts the bus access that caused the fault originally. It should now complete without incident, so the 68010 can continue executing the faulted instruction without any data errors.

The beauty of this instruction continuation method of virtual memory coupled with the isolation of the processor from the fault detection devices (memory manager, EDAC, etc.) is that the programmer only sees actual errors and only the operating system programmer need know that virtual memory is in the system.

Cache, Co-Processor Speed

There are many techniques for increasing both processor and system throughput. Increased processor performance may be a simple matter of using a processor with a higher clock frequency. Better system performance not only encompasses processor improvements, but also includes means of getting more intelligent units operating concurrently on the same or different tasks.

Concurrent co-processors are one means of achieving increased system throughput. Another technique is to provide very fast local memory from which data or instructions can be fetched. This

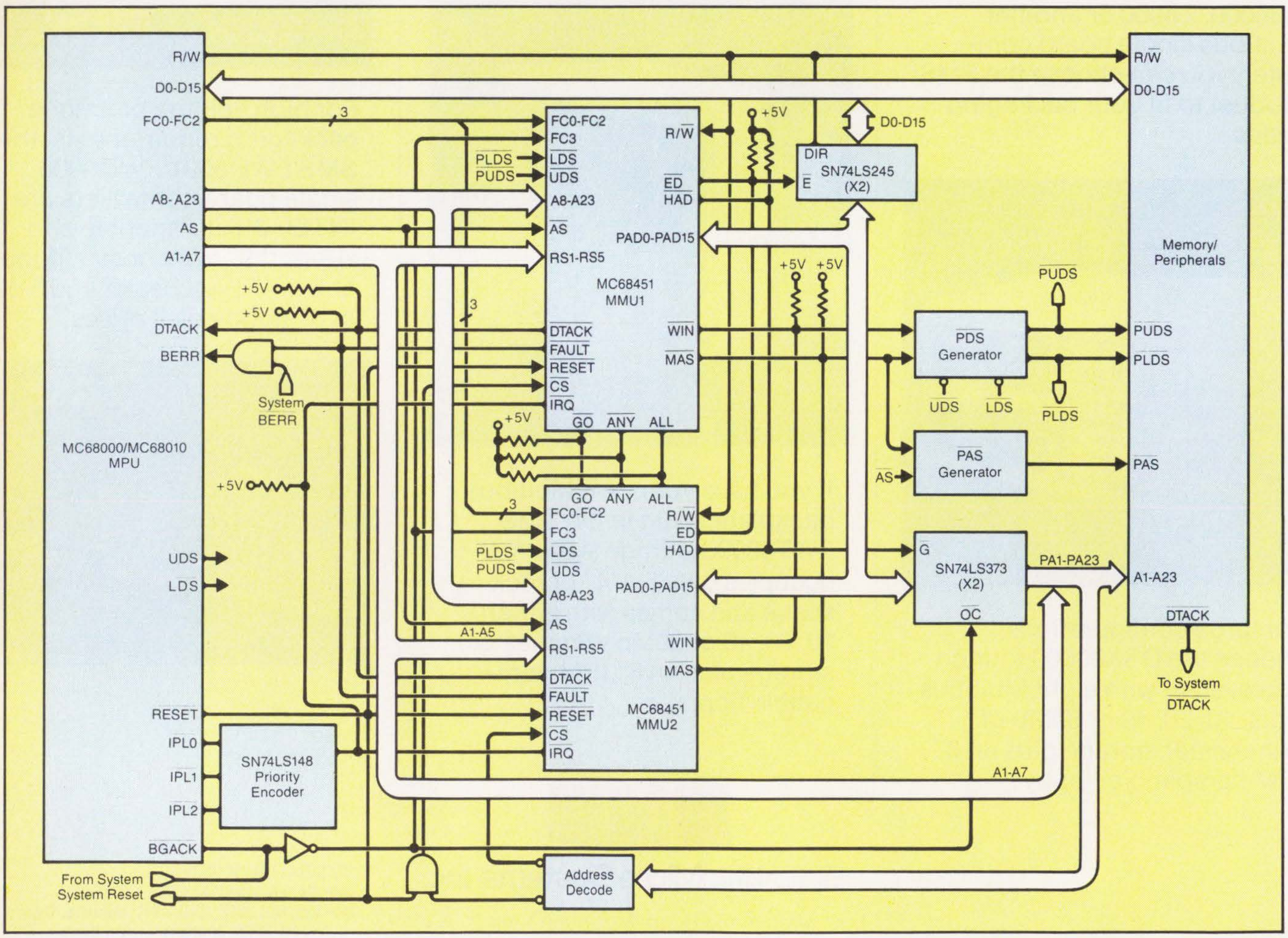

Figure 2: Sample circuit diagram of a two MMU system with the 68000 or 68010.

cache allows the processor to operate without external resources, avoiding delay induced buffering, address translations, excessive signal skewing and the need to address secondary resources that other processors may be sharing. Consequently, the processor can execute faster and the secondary resources are available more to the other processors, allowing faster total throughput.

The MC68020 (**Figure 3**) provides an instruction cache. Each time the microprocessor goes off chip to fetch from the instruction stream, the cache retains the data. Should the need arise to re-execute a recent instruction sequence, it may be that the instruction sequence is valid within the cache. In this case, the processor reads the instruction information out of the cache without accessing off-chip resources.

The instruction cache only holds instruction stream data. Therefore, any time data memory is required by an instruction, external resources will have to be accessed. A co-processor interface is an integral part of both the MC68020 and the floating-point co-processor itself, the MC68881.

The MC68881 utilizes the 68000 family co-processor interface to provide a logical extension of the CPU's instruction set and register set in a manner that is transparent to the processor. It can execute concurrently with the MC68020 and usually overlaps its processing with the MC68020's processing to achieve higher performance. For even greater throughput, up to eight co-processors can be used in a system.

The MC68881 is internally divided into two processing elements, the Bus Interface Unit (BIU) and Execution Unit (EU). The EU executes all 68881 instructions while the BIU communicates with the main processor.

When the MC68020 detects an MC-68881 instruction, it writes the instruction to the memory mapped co-processor interface command register and reads the co-processor interface response register. In this response, the BIU encodes any additional action required by the main processor on behalf of the MC68881.

The virtual machine architecture of the MC68020 is supported by the MC68881. If the MC68020 detects a page fault and/or a task time out, the main processor can force the MC68881 to stop at any time (even in the middle of instruction execution) and save its complete internal state in memory. The MC68020 can also force the co-processor to reload a previously saved state from memory.

Obviously aimed to attack the high-end marketplace, the MC68020 and its companion floating point device, the MC-68881, retain the software compatibility with the earlier parts in the series. Some of the original instructions have additional flexibility, but all of the original capabilities have been retained. New addressing modes, for instance, fit some of the unused bit patterns of the original instructions.

Some of the previously reserved op-code patterns are used in the MC68020 to accommodate new instructions, but regardless, all of the previously used op-code patterns perform the same operations as before.

With market movement demanding more power, the 68000 is now used in personal and business computers.

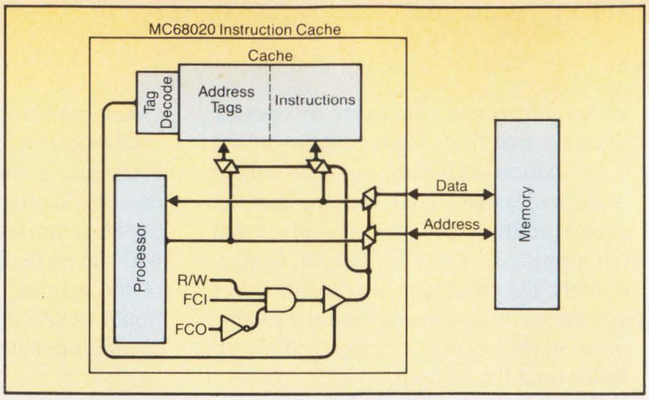

Figure 3: The 68020 incorporates an instruction cache.

Strength in Numbers

With market movement demanding more power at every level of computing, the 68000, introduced as a high-end microprocessor, is now used in personal and business computers. But Motorola has assured that the 68000 will, in some form, continue to serve the high-end of the market, as well. Newer versions, the 68008, 68010 and 68020, have enhanced performance to meet the intensifying demands on processors, while retaining compatibility to the original 68000.

Virtual memory, initially allowed by the asynchronous data bus, has been refined in each version of the processor. The 68020 includes an instruction cache and the 68881 is a floating-point co-processor that speeds throughput further.

This co-processor is just one support device that expands efficiency and assures a broad, high-end range of operation for the family. Memory management units like the 68451 and a variety of controller and I/O chips designed for the processors make the 68000 a complete family. □

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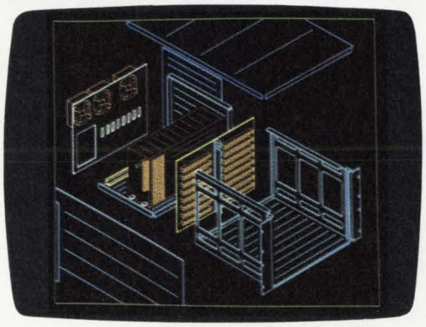

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Local Intelligence	IBM 5080	Spectragraphics System 1500
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2D and 3D Transformation	Yes	Yes
Perspective Transformations, Polygon Fill	Yes	Yes
"Z" Axis Clipping	No	Yes
Backface Testing, Decluttering	No	Yes
Structured Graphics Database	No	Yes
Maximum Number of Simultaneous Colors	256	4096
Maximum Color Lookup Table	4096	16 million
Performance		
Total System throughput computed as the number of 3D vectors processed per second.	25,000*	330,000
Host Support Software		
Available host support software for user applications development.	Device Driver Only	PRISM (Device Driver, plus GKS and extensions)
Configurations		
Communications Processors per Channel Controller maximum	2	8
Workstations per Display Controller Options	1/1	1/1, 2/1, 3/1, 4/1
Communications		
Supported Media	Coax — — —	Coax Microwave Fiber Optic Telephone (T1, V.35)
Price		
Average per Color Workstation	$26.7K	$22.1K
Average per Monochrome Workstation	24.2K	18.3K

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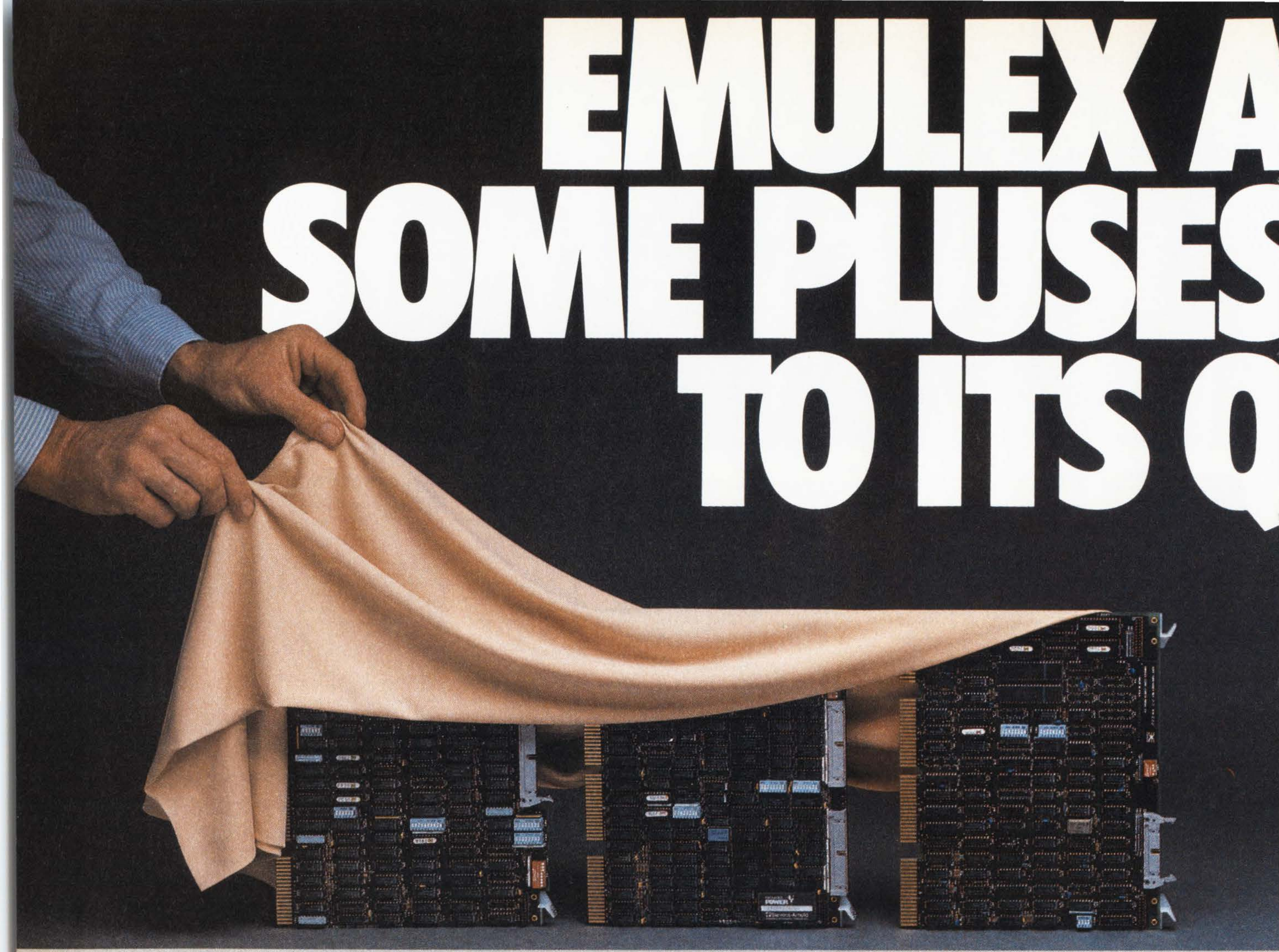

New UC02 emulating host adapter using Mass Storage Control Protocol (MSCP).

New CS02 multiplexer for LSI-11 through 11/23 PLUS and MICRO/PDP-11 computers.

New TC05 tape coupler for CDC Sentinel ¼" streaming tape drives emulates DEC TS11.

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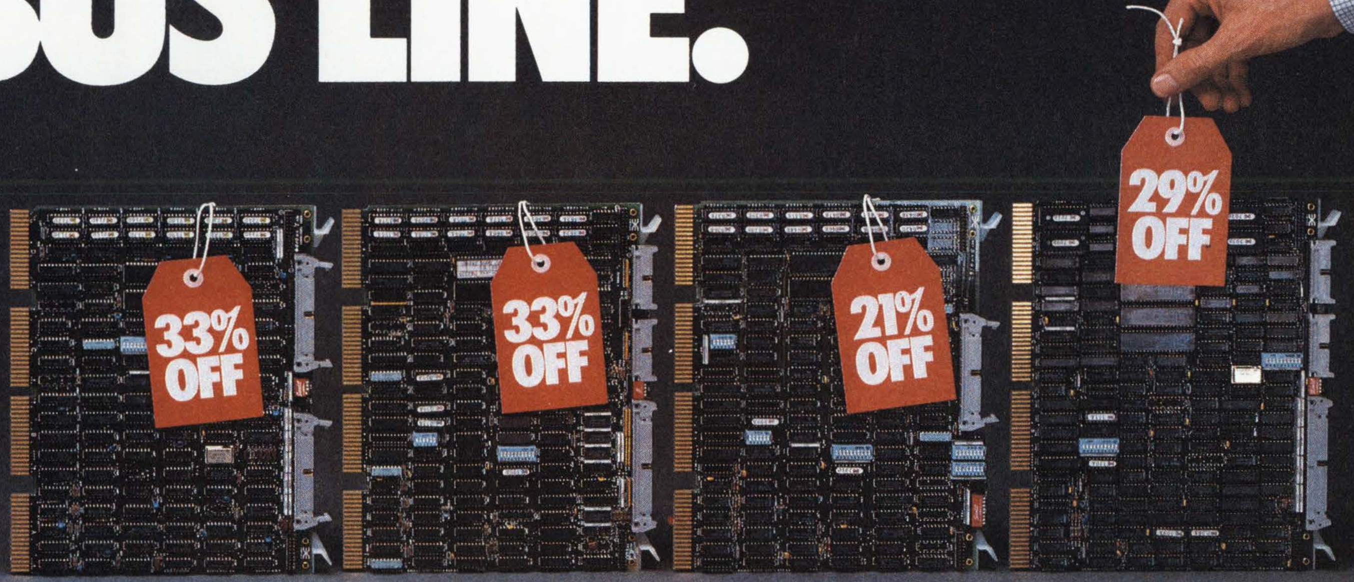

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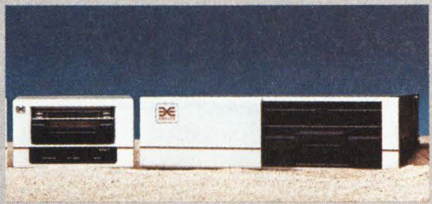

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Photo courtesy Cherry Electrical Products

A Good Year For Keyboards

by Mike Cashman, West Coast Technical Editor and Julie Pingry, Editor

While the keyboard manufacturing industry cannot be called one of the sexier sectors of the computer industry, it is enjoying a vintage time this spring of 1984. The industry is, in general, healthy again and fully recovered from recession.

There is an element of wonder now. Manufacturers are wondering why users are so enamored with the infrared (cordless) keyboards, introduced by the IBM PC jr. While it seemed gimmicky at the time, remote keyboarding is being considered more seriously now.

Membrane keyboard technology is gaining popularity, too. Keyboards using this technology can be made attractive, and printing on the bezel or keycaps allows systems with a high graphics content to communicate their needs more effectively to the user. Flat membrane keypanels have proven the high reliability and low cost of the switch technology. This has encouraged the development of full travel membrane keyboards in which keys move similarly to a typewriter's for data entry.

Ergonomics extend past the full travel keyboard, however. Especially since the 1980 setting of DIN standards for computer configurations, lower profile keyboards and tactile feel keyboards are in demand.

Making keyboards to standard specifications is increasingly important, even in this strongly custom field. The phenomenon that virtually every manufacturer is getting excited about is a quasi-standard keyboard, brought about by the popularity of the IBM PC.

PC Clones

The keyboard industry has always been a custom business, with no two customers ever wanting exactly the same thing. The number of large manufacturers of custom keyboards attests to that volume, and companies such as Micro Switch (Freeport, IL) and Cherry Electrical Products (Waukegan, IL) intend to remain in the custom arena. Still, this custom-only business is changing in the wake of the IBM PC announcement.

"From everything we can tell, there must be upwards of 200 manufacturers thinking of cloning the IBM PC, and they want the same keyboard. In the past, products have more or less been copied, but those vendors couldn't resist changing some design attributes, and that certainly included the keyboard. This time it's different," according to Jim Wieser, an engineer now working as a marketing support specialist for ITW Cortron (Elmhurst, IL).

Membranes boast high growth rates, but the frenzy is over the IBM PC keyboard becoming a standard.

Last fall saw the introduction of a line of IBM PC plug-compatible and look-alike keyboards from Hi-Tek (Garden Grove, CA). Various versions are either


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Figure 1: As an alternative to the IBM PC jr. keyboard, Key Tronic offers a compatible plug-in keyboard with a layout more like a typewriter and a cord connection.

identical in layout to the IBM keyboard or have return and shift keys in typewriter positions. Though the latter "user friendly" option indicates some desire for other models of keyboard, the IBM replica is available not only with IBM-format output, but also with 300 baud TTL ASCII output. This anticipates some demand for the "standard" IBM PC keyboard even for machines that do not emulate all other aspects of the PC.

Cortron's Wieser also sees movement among companies that are out to clone the more elaborate models of the original IBM PC, the /XT and the PC/3270 versions which are based on 122-key keyboards. One could add the DEC Rainbow, the Wangwriter, and products in Texas Instruments' office product line to this list, according to Bob Terwall, director of marketing and sales at Cherry.

"What this seems to be saying is that users want clones to be clones, and that means, at least for the keyboard, not a single key can be out of place. IBM appears to have done everyone a huge favor by shipping a product [the PC] in such numbers that the keyboard became a de facto standard. It holds out the promise that our industry may yet settle on a standard keyboard, at least for data/office processing."

If this trend continues, there are important and mostly favorable advantages that will accrue to virtually every company that assembles systems.

First, keyboard costs can come down, reducing overall system costs. Second, a standard keyboard would accelerate the pace of manufacturing automation. Several manufacturers stated they expect measurable qualitative product improvements from robotic assembly. Third, the manner in which keyboards are sold may change, at least in the business processing sector of the entire industry.

To capture end user business, Key Tronic (Spokane, WA) has taken a tack that its competitors are watching closely by appealing directly to the end users of IBM and Apple PCs. The message is that users may want to consider enhancing their personal computer by equipping it with a keyboard that features LEDs to indicate locked down keys, keys with printed labels instead of symbols, etc. According to Joseph M. Dooley, Key Tronic keyboard marketing manager, the major issue with this approach currently is one of selecting the appropriate keyboard distribution channel for the end user marketplace.

One PC manufacturer is offering the keyboard to their own series of micros as IBM and IBM-compatible replacement keyboards through retail computer stores or directly from the company. Colby (Mountain View, CA) announced volume availability of a small, lightweight keyboard compatible with their own and IBM personal computers at the beginning of the year. With their own PC-1, -2 or -3 models, Colby's keyboard snaps onto the front of the computer to create a portable; at 4″ narrower than the PC keyboard, it can be used in the lap as well.

Interestingly, IBM may be considering an alternative keyboard for the PC jr. It is not clear whether this interest is due to customer reaction to the current rectangular-keyed box manufactured by Advanced Input Devices (Coeur D'Ilene, ID) or for a more business-oriented version of the PC jr.

Key Tronic offers a replacement for the jr. that not only uses a cord, but has a typewriter-like key layout (**Figure 1**) and legends on keys that have only symbols on the IBM version. LEDs on keys that can lock down are another popular way to enhance input ease. The keyboard is promoted as providing professional performance from the PC jr.

Infrared Vision

One feature of the IBM PC jr. keyboard may have a future in other products, according to Cherry's Terwall. It is the cordless feature of the unit that enables it to operate the computer remotely.

"I arrived at last Fall's Comdex in Las Vegas with an attitude that the cordless capability was a minor feature, but after talking to OEMs about end user requirements, I changed my mind."

An infrared connection option, as well as two standard keyboards using wireless connect are available from Cherry now. Both standard models operate with either the IBM PC jr. or the PC. For use with the standard PC, a receiver module must be used (**Figure 2**) at the computer; the peripheral plugs into the keyboard connector and provides parity checking and 16 keystroke buffering.

Terwall says there appear to be more applications for remote keyboards than industry market intelligence has indicated. In the construction industry, for example, blueprints are layed side-to-side over large areas and PC jr. users can move around these layouts with the infrared communicating keyboard. In large manufacturing facilities, users can communicate with systems from balconies or other locations where it would be impractical to move even a relatively lightweight, portable computer. Together with the number of users who apparently enjoy the ability to put the PC jr. keyboard in their lap and do computing from the comfort of a chair on the other side of the room, this may help explain the user popularity of cordless computing.

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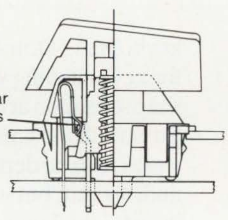

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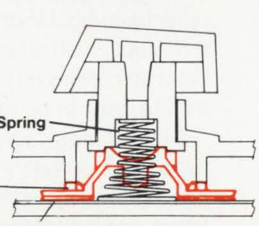

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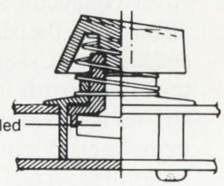

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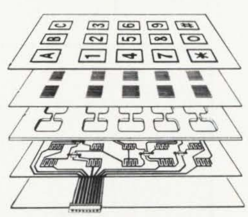

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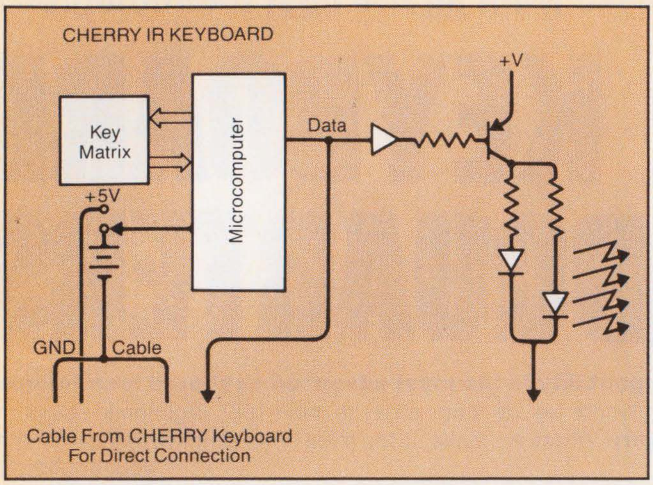

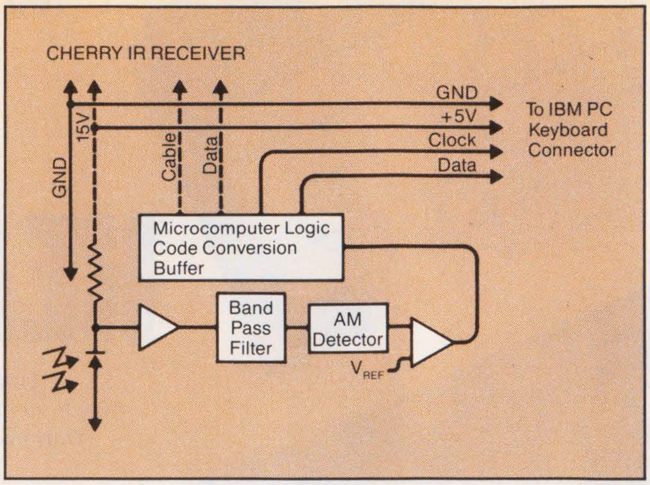

Figure 2: Circuit diagrams of Cherry's IR keyboard and the receiver for use with an IBM PC.

Keyswitch Technologies

Several main switch technologies now produce high quality keyboards. For very high reliability, but high cost, Hall-effect and reed switches have been preferred. These technologies have been in use for many years, but as size shrinks, these have lost some ground, as they are relatively large.

Capacitive switching is the dominant technology for full travel keyboards now, because of its low cost and reliability. Ferrite cores have also been widely used over the past decade and are nearly immune to their environment. Both technologies use sensing electronics, so encoding for byte-wide rather than matrix interface signals can be implemented at little premium in cost.

Several types of mechanical switches are also used to produce keyboards, from metallic hard contact to domeswitch and membrane. Hard mechanical contact switching is the oldest keyboard technology, and generally uses gold or silver contacts. Sensitivity to dust and foreign objects between the contact points has led to bifurcated and even trifurcated contact points, to assure contact closure. Coupled with microprocessors, and sealed enclosures, this technology continues to provide high performance switching.

Two other mechanical switches are widely used in both flat keypanels and keyboards. Domeswitches can be used for keyswitching with a natural tactile, or snap sensation at contact, feel. These use a dome shaped piece of metal that, by its shape, can be depressed to make contact underneath, but will always snap back to its original dome shape. Calculators and other hand-held instruments often use this technique, with relatively little key travel, but with buttons on top of the dome, more movement can be introduced.

Membrane switching has traditionally been used for flat virtually no-travel keypanels. The keypad switch is simply three layers, two polyester layers screened with silver conductor and a spacer between them. These flat panels are simple to make and low cost. Using this technology in full-travel keyboards for data entry, key caps and mechanics are used on top of the membrane layers (**Figures 3 and 4**), which still perform the actual switching. The growth rate of membrane technology figures to exceed capacitance technology keyboards, but will probably not replace it.

The conductive rubber technology used in the IBM PC jr. keyboard is another of its features that is picking up steam. Silicone rubber is the elastomer of choice for keyboards, as it is relatively long lived; domes of rubber impregnated with carbon are used as contact points with the circuit board. These keyboards can be made quite inexpensively, as an entire sheet of rubber can be used instead of single switches.

None of the manufacturers interviewed foresees a fundamentally new technological development threatening the dominance of the familiar capacitance keyboard, at least in business/scientific systems. But most interviewed agreed that the industry seems to be moving toward the goal of combining many of the

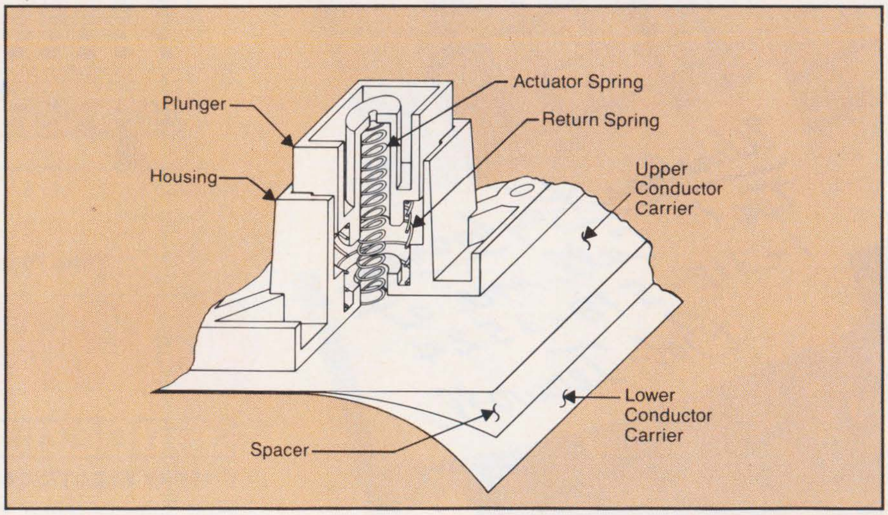

Figure 3: Cutaway of a key in Stackpole's full travel membrane keyboards; the switching is done by the three membrane layers (upper and lower conductor and spacer), by actuator contact.

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desirable features of capacitance and membrane technologies.

"We feel that the technology of the future will be a hybrid that combines membrane, conductive rubber, and capacitance technologies. The keyswitches, if not the boards, will be hermetically sealed, enabling them to work in relatively contaminated environments. And they will be reliable, because noncontacting equates to no wear, and that means reliability," states ITW Cortron's Wieser.

Low Profile DIN

A very pressing issue now is complying with the German DIN standard for low-profile keyboards – and not necessarily as a prelude to entering the European marketplace, according to two sources. "One thing about these new low-profile keyboards: They really make a system look modern and not like something out of 1979," said one.

Set in 1980, the DIN standards for keyboards are aimed at ergonomic data entry. The resulting configurations are lower profile, with slightly less key travel than older generally accepted keyboards, and sculptured keycaps with tactile feel are specified. A maximum height of 30 mm from the top of the desk to "home row," the third row, in conventional keyboard configurations required. For boards slanted from 0°-10° this means that the mechanics must be compact to the base. Older low profile keyboards, developed in 1975, were about twice that height.

Key travel set by DIN is also less: 0.120" to 0.150" as compared to 0.150" to 0.190" typically for low profile keys. The specification of tactile instead of linear feel full travel keys is leading to the research and development staffs at many of the major keyboard manufacturers charged with improving the tactile feel of existing technologies.

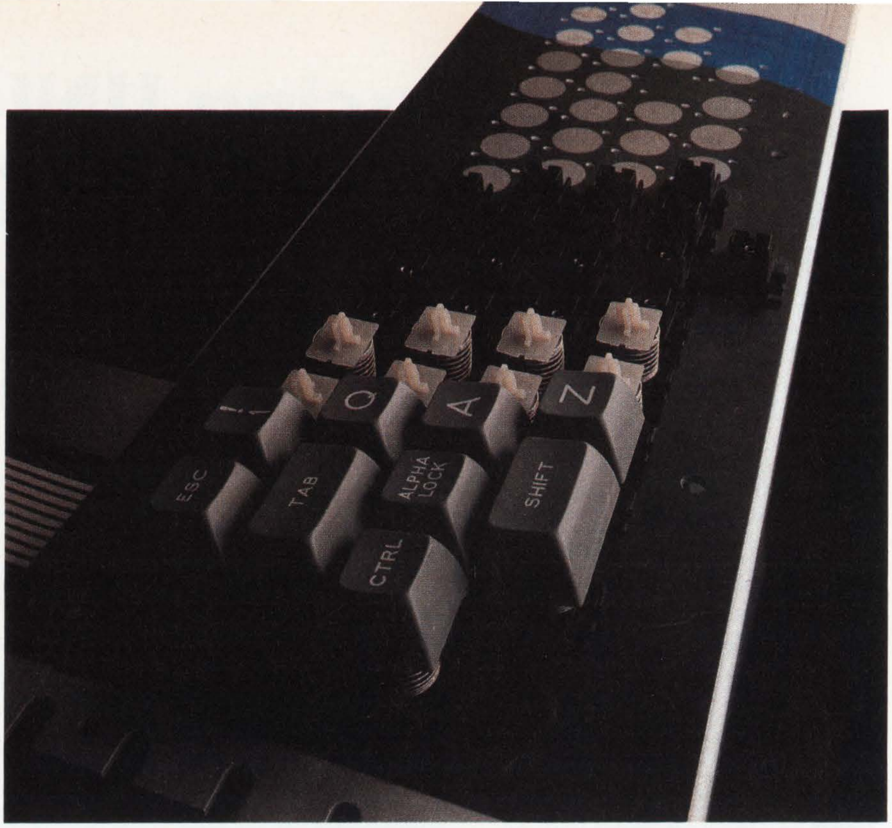

Figure 4: A cut-away of an Oak Switch membrane keyboard shows the build-up of layers from right to capped keys at left.


Figure 5: Keys of Micro Switch's low profile keyboard show reduced height.

Change, Growth

Many technologies and configurations for keyboards will continue to co-exist, not only for the huge variety of applications in microprocessor-based machines from appliances to copiers and bank tellers, but also for data entry. The convergence of several switching techniques is making keyboards optimized for computers and data entry more reliable and less costly.

And though customizing for every application will, no doubt, continue to take place on a huge scale, some standards are taking hold. Sheer force of market share for the IBM PC is making a demand for clones, as well as for other configurations that operate with the IBM PC. The DIN standards to improve usability of keyboards are prevading nearly every product line with lower profile keys and tactile feel.

Innovations for portability and remoting a keyboard with infrared links will have an effect for some segments of the market. Advances in lifetime and environmental immunity are also taking place, in part due to portable computing.

The ongoing pursuit of shrinking virtually everything associated with the computer industry doesn't affect the keyboard industry to nearly the same degree. With chips, memory, and displays continually getting smaller and lighter, keyboards may be the largest physical system component one day soon. So why not put the entire computer in the keyboard?

"We're thinking of taking that approach to come up with a value-added product," according to Key Tronic's Dooley.

Several other manufacturers stated that it was decided that this approach would place them in competition with their customers. These manufacturers are concentrating on the traditional aspects of keyboard design and manufacture: upping quality and reliability, and decreasing costs, prices, and delivery times. □

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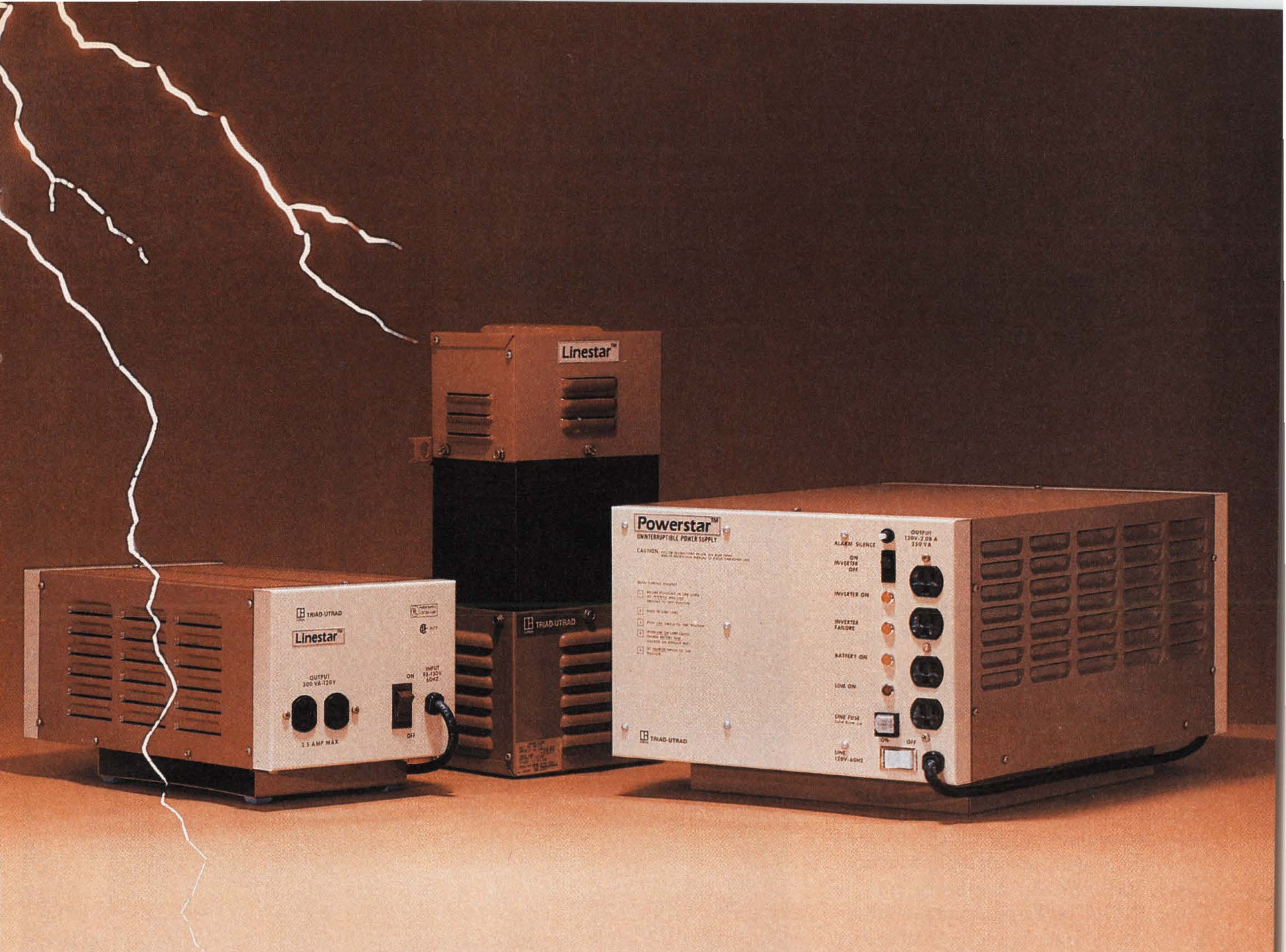

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Device Level Intelligence For Graphic Systems

by Gregg Stempson

The escalating demands of today's graphic systems are placing the system integrator in a classic double bind. On one hand, there is a pressing need to off-load graphics functions from the over-burdened host to the graphics device. On the other, the designer is limited by the often staggering cost of intelligent graphics terminals.

Solutions to this problem may be addressed by a graphics operating system. Genisco Computers Corporation has developed "GENCOR" to facilitate high level functions including 2D and 3D transformations. GENCOR based systems are available at half the cost (or less) of systems with comparable functionality. GENCOR, available on the Genisco G-6200 Terminal, demonstrates a migration to device-level intelligence from the host-level intelligent of systems such as Template and DI-3000.

Three characteristics of GENCOR are:

1) the amount of intelligence provided at the device level in a low cost software/firmware solution. The trade-off for software-based functionality is a sacrifice in hardware operating speed. Very high speed, however, is not required by many applications. The approach allows CAD, stress analysis, and command/control applications access to 2D and 3D functionality at low budget.

2) GENCOR incorporates the best features of the major graphics standards GKS and CORE, and is perhaps the most exact PHIGS implementation available. In addition, GENCOR offers basic imaging operations.

3) GENCOR is portable to future Genisco systems.

The GENCOR operating system is written primarily in the high-level language "C" and 10% in assembly. C was selected becasue of wide acceptance and usefulness in a graphics environment. In addition, the operating system can be ported to new hardware with only a rewrite of the kernel.

GENCOR provides for independent windowing of text, 3D graphics and images.

Multi-Level Display List

The functionality of GENCOR is based on a multi-level display list, unique at the device level. It allows the user to define multiple views of, or to "instance," a single object without replicating it in a local list. In single level lists, the data composing each view or "instance" must be stored within the list, a memory intensive and perhaps prohibitive operation. The GENCOR display list is modeled after a hierarchical structure, composed of view surfaces, view trees, segments and primitives.

View Surfaces define the hardware components to be used for picture construction and display. These components include a graphics output channel; a memory select mask for image construction; a memory gating mask for image display; a window in the addressable refresh memory which defines a Normalized Device Coordinate (NDC) Space; flags signaling "initialized" and "selected"

Gregg Stempson is Director of Software Development at Genisco Computers, where he has been for four years. He holds a B.S. in Computer Science from the University of California at Irvine.

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Today, there is a pressing need to off-load graphics functions from the over-burdened host to the graphics device.

status; and a list of view trees. Several View Surfaces can be mapped into the display area simultaneously. View Surfaces are the only level where the user is responsible for the hardware characteristics of the display; as GENCOR's hardware base evolves, the user can simply modify the View Surface definitions to correspond to increased colors or resolution.

View Trees, so named because their segment structure can resemble that of a binary tree, define which graphical objects are displayed on a view surface, and how those objects are transformed. Trees consist of a 16-bit Identifier for individual reference and manipulation; a display tree of segments defined by a "Root Segment," a current viewing transformation matrix; the parameters that make up that matrix such as "up" and "normal" vectors; a viewport defined in NDC Space onto which the view is mapped; clipping control flags; and a right/left coordinate system flag.

View Trees are made up of a series of "nested" or "instanced" segments, the smallest randomly accessible data construct with GENCOR. Segments are collections of graphic primitives such as move, draw, marker polygon, curve, polylines and polymarkers. In addition to the primitives themselves, Segments also contain attributes such as color, linestyle and linewidth.

Primitives, Graphics and Imaging

GENCOR primitive commands define objects in 2D or 3D world coordinates. Objects are generated through the manipulation of lines, curves, markers and text. Primitive attributes assign color, linestyle and linewidth to the objects created by the primitive commands.

Move primitives position the graphical operating point of a line, text, curve, etc. without any visible change to the display. Move can be absolute, moving directly to the specified world coordinate, or an offset from the current operating point in a relative operation. Line draws construct a vector from the current operating point to the specified position, while polylines construct a series of vectors from multiple points (eliminating constant move-draws). Markers and polymarkers allow a general form of plotting by the placement of arbitrary celled characters.

A primitive unique to GENCOR is the Rational Cubic Curve, that specifies virtually any type of curve, hyperbola or conic section which can be defined using a 4×4 matrix specifying four Third Order Polynomials. The evaluation of the polynomials gives interpolated values to x, y, z and w, with the user specifying the number of vectors to be computed in constructing the curve. This gives a very general arc format and allows arbitrary 3D transformations on the curve. The Rational Cubic Curve primitive gives GENCOR extra appeal for solid modeling and finite element analysis.

Unlike other systems in which polygons are made up of a series of vertices which may limit flexibility, GENCOR uses only two matched primitives to start and end a polygon. Any other primitive, excluding text and marker, may appear within those bounds. The resultant polygon may be either filled or hollow.

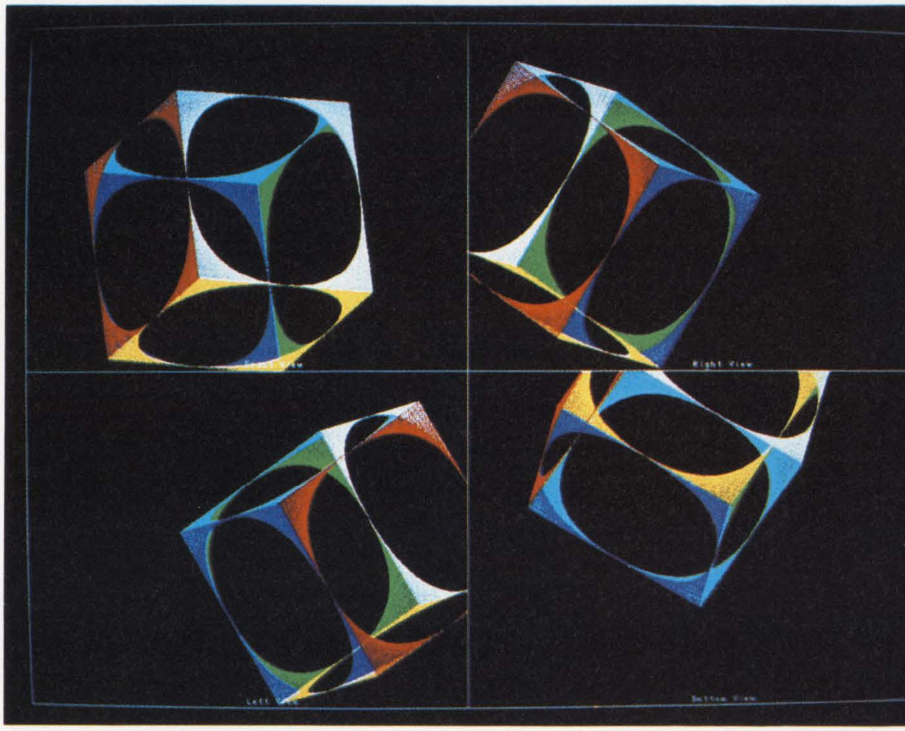
GENCOR also provides the user with considerable flexibility in the choice of character fonts. Two standard types are supported – a raster cell type and a high precision "stroked" type. Fourteen more user-defined fonts are possible.

Primitive attributes, such as color and linestyle, occur at the same level in the "Tree" as the primitives. The attributes exist within the Segments and affect all subsequent primitives until another attribute is set. GENCOR also allows the user to specify eleven linestyles.

Powerful Segments

While primitives in GENCOR define parts of an object, segments define the object as a unit. When created by the user, a segment is given a unique 24-bit name, which allows it, as with View Surfaces and Trees, to be individually accessed.

GENCOR supports a number of segment commands which include open to create a new Segment; delete to remove a Segment from the display list; clear to remove all primitives within a Segment but to retain its structure within the display list; and reopen to open an existing Segment and allow the insertion of new primitives.



This 1200 vector shape was constructed with a single 50 vector segment, which was then transformed into four windows.

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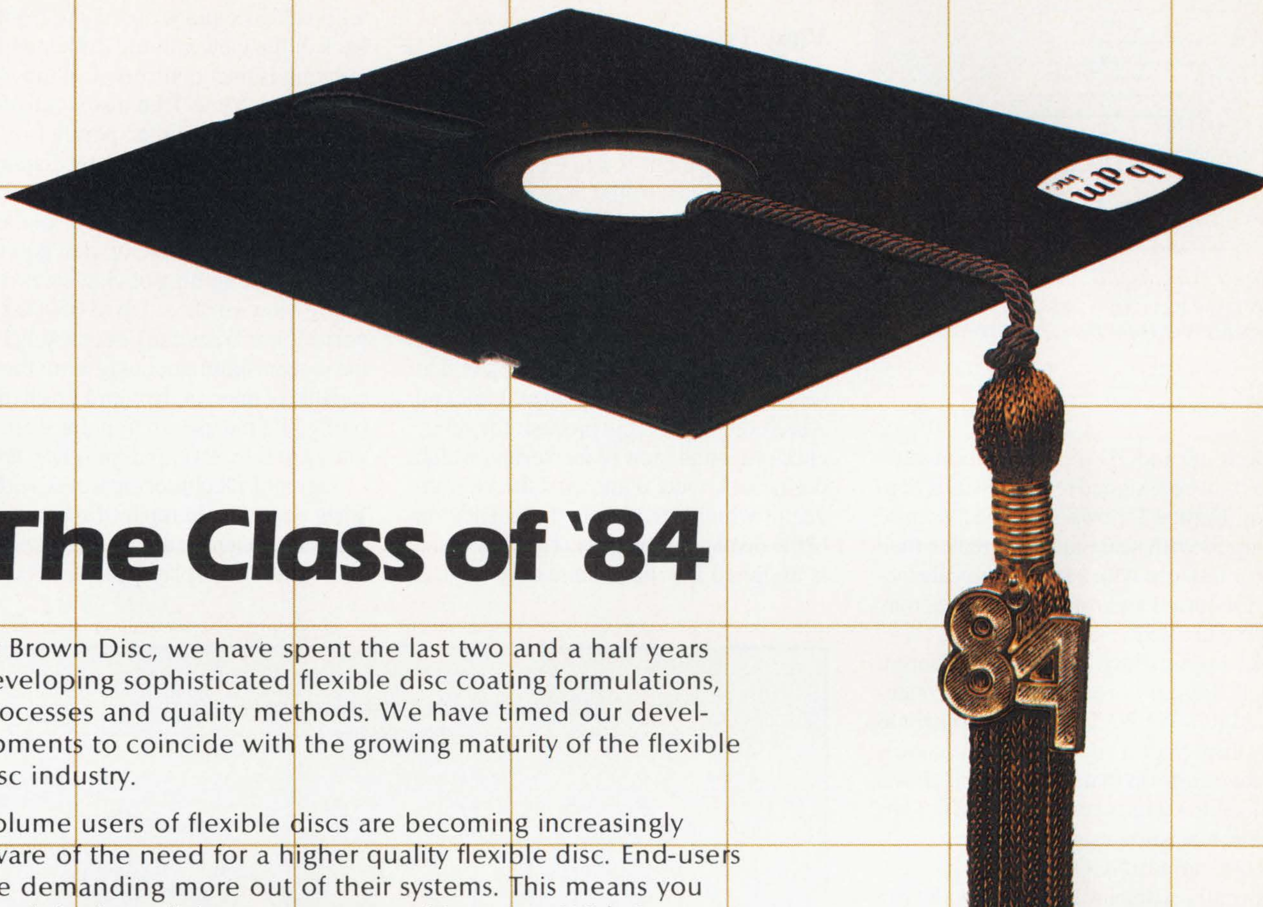

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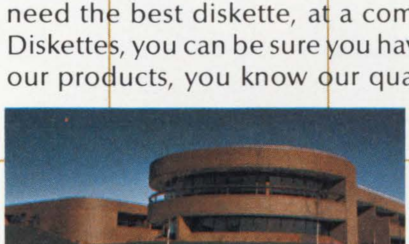

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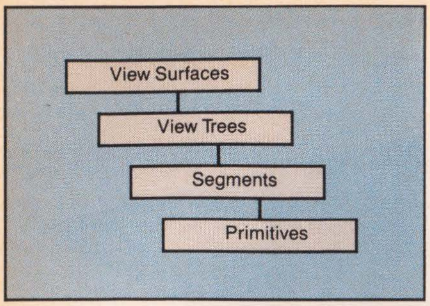


Figure 1: The display list structure of GENCOR consists of View Surfaces, View Trees, Segments and Primitives, hierarchically.

Both 2D and 3D transformation attributes can be assigned to a GENCOR Segment. **Figure 2** shows how objects can be enlarged with scale factors greater than one or reduced with a fractional scale factor. Distorted and mirrored images may also be created.

For applications requiring a different transformation order than scale-rotate-translate, GENCOR offers optional transform matrix commands. The concatenate transform matrix command allows the user to merge new matrix coefficients with the existing matrix.

With the GENCOR display list segment calls, a display list can be built with minimum Segments. Segments are "nested" so that an existing Segment may be used many times by other "segment calls" to define multiple copies of objects. Nesting down to 100 levels gives significant savings in both storage and transmission overhead.

When a segment call is executed, the current transformation is compared with the transformation, if any, of the target Segment. This process is repeated as deeply as the calls are nested. All primitive attributes are saved so the target Segment does not affect those above it.

GENCOR also offers dynamic Segment attributes. These can be changed after a Segment has been defined, unlike primitive attributes which occur only within the segment structure (color, linestyle, etc.). Dynamic attributes, generally manipulated interactively include highlighting (blink) which distinguishes a Segment or groups of Segments from others, visibility or whether a Segment is displayed or not and detectability, or whether a segment may be detected during "Pick" operation.

Lastly, GENCOR supports "Declutter," to define "Visibility Level" for Segments and View Trees. The level is user-definable as a 16-bit value, and allows for conditional visibility.

View Trees

The hierarchical display list created by segment calls is known as View Trees. In **Figure 3**, a View Tree with Root Segment 6 (a root segment is made up of calls to other Segments) would display Segments 4 and 5 which, in turn, would display Segments 1, 2 and 3. Segment 1 is referenced by both Segments 4 and 5, saving storage and transmission time.

View Trees are defined by a viewing volume which limits the 3D object that will be displayed; a 2D view plane on which the object is projected; the reference point and view plane normal which defines the view plane; and the view up vector which determines the orientation of the displayed object(s). The view plane is assigned a window, and only objects falling within that area will be displayed. The objects outside the window will be "clipped" in x and y, and in the front and back of the view volume (hither and yon clipping is user controlled) if the object is 3D. The View Tree also controls the projection type, either parallel or perspective, of the objects to be displayed.

Aspect ratios of an object mapped as a square window in the view plane are maintained by the use of viewports that contain the mapping of view trees onto a single view surface. Up to 65000 viewports/View Trees can conceivably be on the screen simultaneously, with the host capable of interacting with a given tree or port while the user manipulates another via a joystick, trackball or other device.

Segment Declutter operates with the View Tree Declutter in three ways: no declutter in which all segments within a View Tree are displayed; arithmetic com-

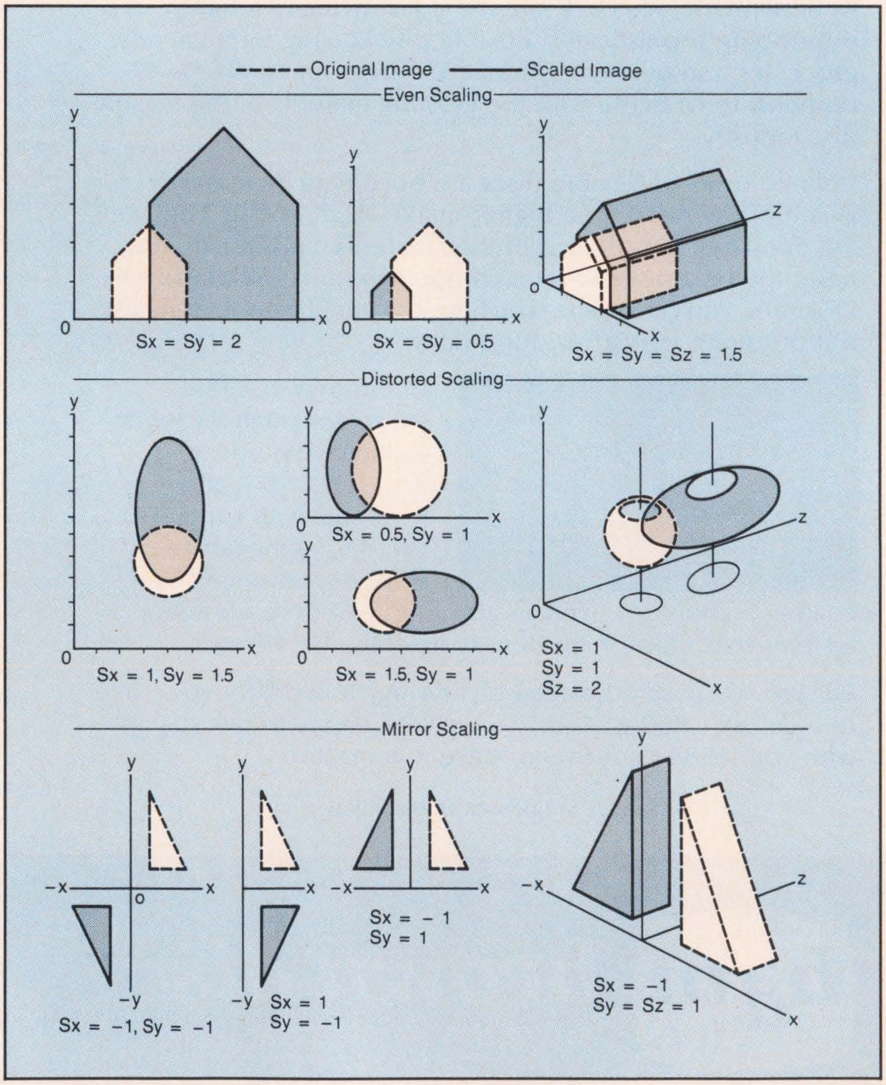
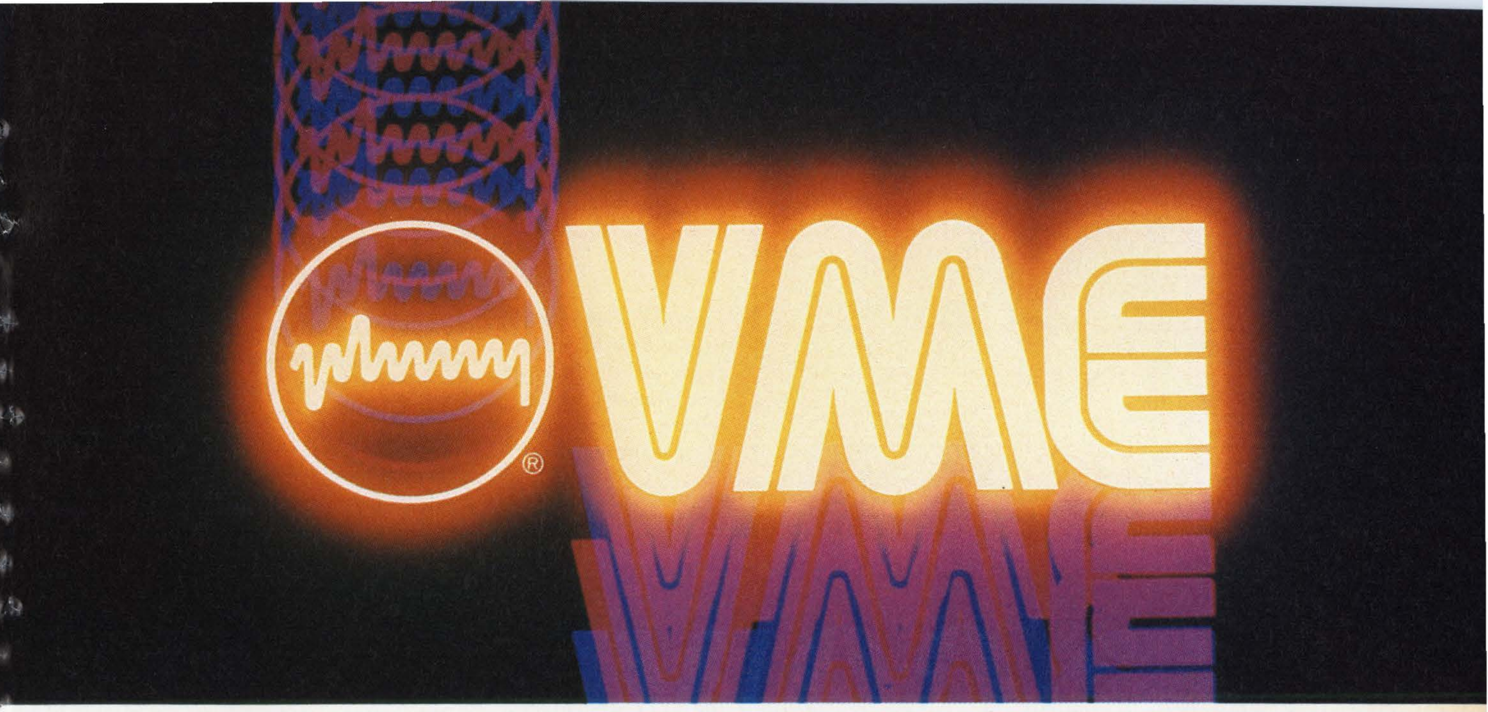


Figure 2: For scaling, the scale factors Sx, Sy, Sz are multiplied by the existing primitive values to enlarge, reduce, distort or, with a negative scale factor, mirror.



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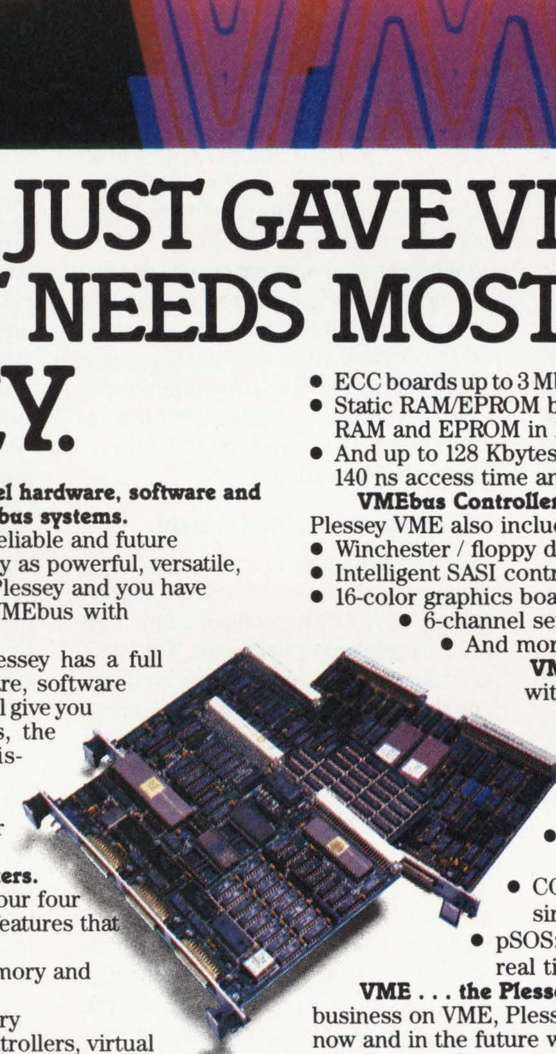

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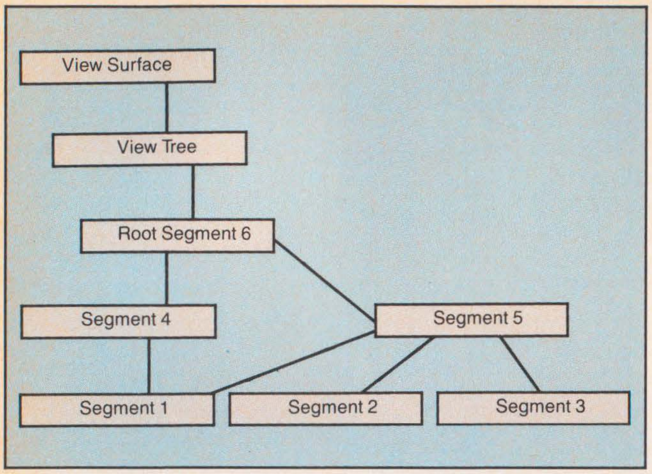

Figure 3: View Trees uses a Root Segment made up of calls to other segments, which, in turn, display more basic segments.

pare which displays only segments with declutter values less than or equal to the View Tree; and, logical compare in which segment declutter values are anded with those of the View Tree, and if the result is non-zero, the segment is displayed.

When the user "zooms in," via a scaling operation, more detailed information may be displayed by increasing the View Tree declutter value. Decluttered data remains in the display list even though not visible. A change in its declutter level requires a single simple command at the View Tree level.

The GENCOR View Tree structure also allows the user to manipulate selected areas of the display without disturbing others. Selected surfaces are erased but other surfaces are unaltered.

All Segment attributes are propagated down the View Tree during a redraw operation. The user simply activates the attribute (highlight, visibility, etc.) at the highest level on the list in which he wants the attribute to exist. All succeeding Segments will then take on the attribute without further commands.

Imaging: Expanding Applications

The ability to do imaging as well as graphics gives GENCOR flexibility not generally found in device level graphics. Image commands are applied directly to refresh memory planes. Since the commands are not part of the display list, they are not affected by any device-independent functions such as transformations, pick, visibility, etc. The image can, however, be zoomed and scrolled if supported by the hardware (pixel replication and scroll).

Images are generated by defining color values for contiguous pixel locations in a left-to-right, right-to-left, top-to-bottom or bottom-to-top direction. Pixel values may be specified individually (pixel write) or by specifying how many contiguous pixels are to be written in a single color (run length encoding).

While most images are created by erasing the view surface and replacing it with new data, GENCOR also provides three additional logical writing modes. These modes perform logical operations using the existing displayed data and the new incoming image via and, or and xor (exclusive or) operations.

Interactive Device Control

While the user may select keyboards, joysticks, trackballs or bitpads to interact with, GENCOR input device functions are independent of hardware. The functions are applied, to four logical classes and their corresponding logical devices. Logical classes define virtual input devices which can be simulated by hardware or software input and include: 1-Locator, 2-Valuator, 3-Keyboard and 4-Choice.

Locator logical classes provide coordinates for moving objects or redefining windows. Local "Rubberbanding" can be achieved by using the cursor to dynamically reposition one endpoint while the origin remains fixed. The locator echo can be set so that all lines are vertical, horizontal or construct a rectangle, or it may be restricted to a specific area of a given view surface, protecting other areas/surfaces from being written into.

A logical locator is used to "Pick" an object on a given View Surface. When an object is picked, GENCOR returns the View Tree and all Segments in the path to the object picked. The Segment picked may then be highlighted, reopened or deleted.

Logical valuator classes provide fixed point real values from a device to be used during an interactive process. These values may be locally linked to part of a Segment transformation (i.e. rotation) to facilitate local interaction. Keyboard operations read character strings from a logical keyboard class and return ASCII values to the host system. Logical choice allows the user to choose among alternatives, usually with a function keypad.

Data received from input devices are returning in one of three modes. Request mode forces GENCOR to wait for a trigger (key or stylus strike) before reading and returning data; Sample mode returns the current value of the device without waiting for operator action (a trigger); and event mode stores request data in an event queue that may be read from the host.

Pieces of Proposed Standards

GENCOR's independent input device handling has been modeled directly after GKS while the viewing transformations are generally patterned after CORE, GENCOR, however, is extended to allow multiple viewing transformations simultaneously. CORE provides only one 2D or 3D viewing transformation, which is applied to all visible segments. GKS is equipped for multiple 2D transformations but only one is active at any given time.

At the segment level, CORE offers 2D or 3D image transformations while GKS has only 2D image transformations. GENCOR allows nested 2D or 3D modeling transformations at the segment level.

Although GENCOR was developed independently of PHIGS (Programmers Hierarchical Interactive Graphics Standard), both provide a multi-level display list structure. The significance of this is that both represent current developments in sophisticated graphics design. GENCOR provides a glimpse of tomorrow's graphics systems – advanced device level intelligence in low cost terminals and workstations – a way out of the graphics designer's double bind. □

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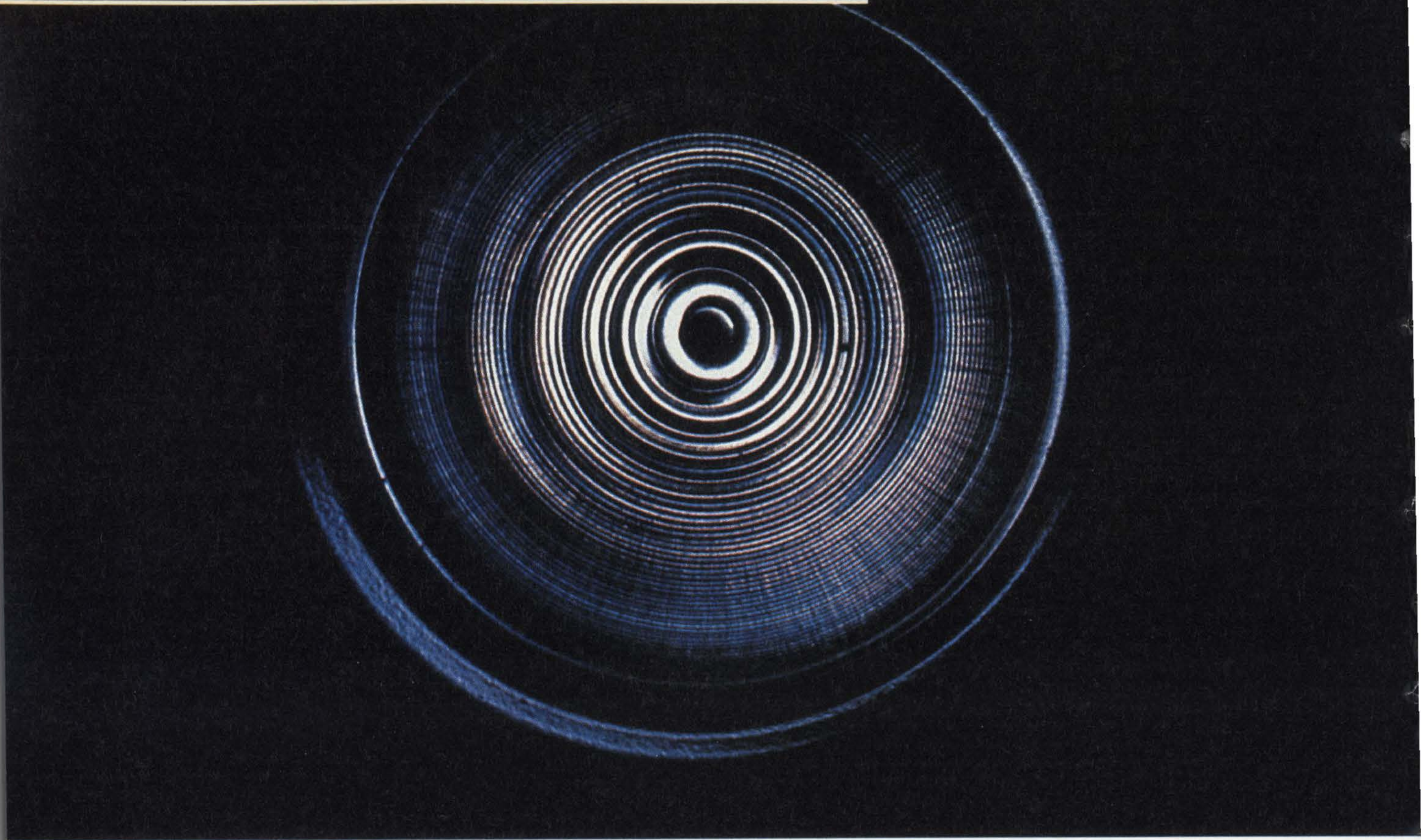
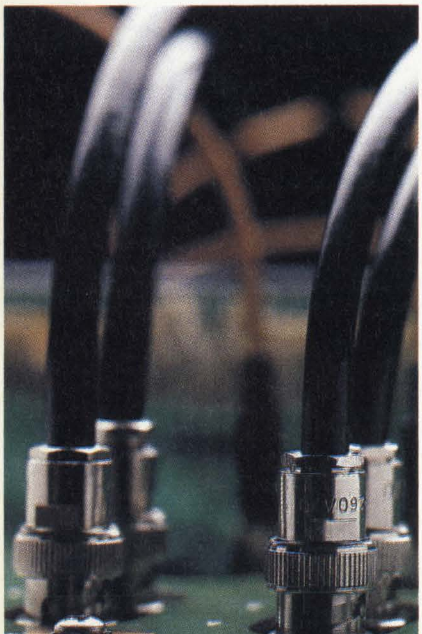


Lasers And Fiber Optics: Data At The Speed Of Light



by Julie Pingry, Editor

Laser light signals through optical fiber media are now commonly used for telecommunications transmission. The advantages are such that in some circumstances, phone companies will not consider wire or coaxial cables for new installations. Technological advances in materials for fibers and active devices as well as manufacturing improvements have made possible extremely fast signal transfer at high bandwidths. AT&T Bell Laboratories (Holmdel, NJ) has sent a 1 Gbit signal down a single 75-mile long fiber with no repeatering or boosting of the signal. Single mode transmission techniques (using long wavelength optical signals at a single frequency or longitudinal mode) allow signals to be transmitted with low enough attenuation to be detected accurately over that distance.

Above: Magnified photo of an AT&T optical fiber cross-section shows layers of a graded index fiber. Left: Slender orange fiber cables and black coax connect into an Artel board.

The bulk of computer communications, however, spans distances under a mile; typical data channels are only in the Kbit or (for very high speed devices) several hundred Mbit per second range. So as the title of the keynote paper for this year's Conference on Optical Fiber Communication (OFC) asks, "Who needs the bandwidth?"

High speed host-to-host and multiplexed device-to-host links do not strain the capabilities of a standard single fiber system. The sheer number of devices operating now, coupled with an increasing awareness of the value of access to data residing on other machines, are driving for faster, more powerful data communi-

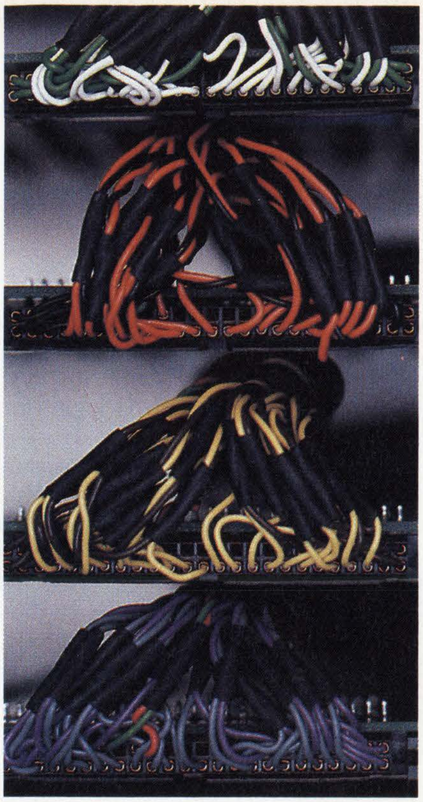


Photo courtesy Artel

cations networks. Another push for high bandwidth transmission comes from increasing use of mainframe-generated graphics and the demand for near real-time screen redraws.

Other characteristics of optical transmission, such as its immunity to and noncreation of electrical interference and its resistance to being tapped without detection, open applications in specific computer environments. Medical and industrial systems are used in areas where other machines create noise that can interfere with the integrity of critical data. For the military, optical free space and fiber systems are used to ensure no signals are emitted that could be detected, intercepted like microwave or tapped as copper cable.

As these specific current application areas suggest, the technology is used only where it fits and its advantages are crucial. For computer communication, optical links will become more popular as components drop in price and are optimized for the application. Further increases in processing and I/O speed and device sophistication, as well as distribution of computers and terminals, will make optical transmission increasingly worth designers' consideration.

For transmitting mixed data, video and voice, optical fiber is ideal. Unlike wire or coax cable, the same fiber cable can transmit any type or mix of signal types. Its inherent bandwidth can also accommodate upgrades in the speed of any of the signals, or add channels for future needs and services.

A Valtec engineer records results of a single mode fiber test.

The single mode optical fiber could become the data communication media of choice if the optical IC can be perfected. For the advantages and speed of integrated optics to be most useful, the single mode signal an optical IC creates would be transmitted in that form, without conversion, throughout a computer. But even if the all-optical computer never becomes a reality, advances in optical components and increasing computer power will provide applications for lightwave data transmission.

Refined Optical Sources

Both lasers and LEDs have been used extensively for sources in fiber optic systems, and considerable development effort is resulting in the optimization of emitter performance. Traditionally, LEDs have been used for data communication systems, since the shorter link lengths have not required great power, and LEDs are simpler, more reliable and less expensive than lasers. However, as devices and data requirements change, a range of emitters will meet various transmission needs.

One major area of improvements for LEDs is output power coupled into a fiber. Unlike a laser, in which photons at the active junction are emitted normal to the surface, the photons in an LED travel in many directions. The high index of refraction of the III-V semiconductor materials allow a small critical angle into which photons can pass and escape. The majority of optical energy is reabsorbed by the material. Of the photons that are emitted by the LED, many are not driven down the fiber, which has its own angle of acceptance (**Figure 1**). By using lenses and coupling media to match the output numerical aperture (NA) or acceptance angle and the source size (the light spot generated) to the fiber's NA and core size, coupling efficiency and power into the fiber is increased with LED sources. Emitters range up to the tens or low hundreds of microwatts power out; work on an LED that couples 1 mW into a fiber is underway at M/A-COM Laser Diode (New Brunswick, NJ) under a contract to the Navy. Similar increases in LED power output will allow longer.

Advances in optical components and increasing computing power will provide applications for lightwave data transmission.

Photo courtesy Siecor

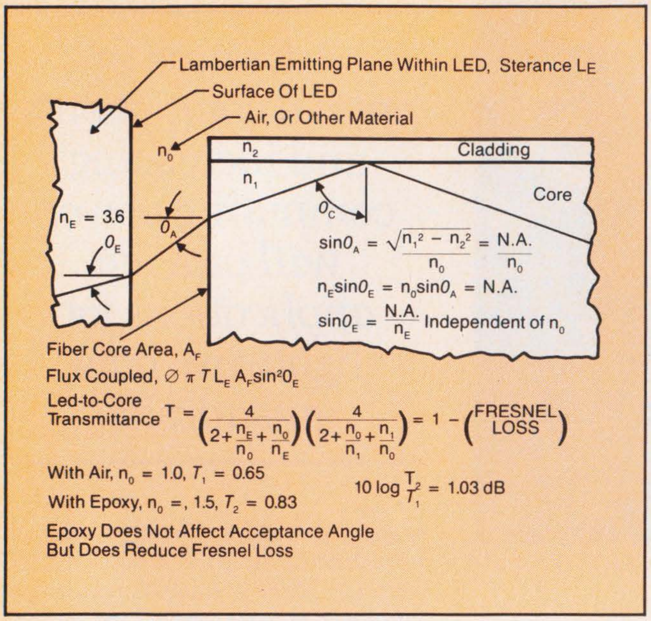


Figure 1: Cross section diagram illustrating fiber acceptance angle (NA) and fresnel loss for LED to fiber power coupling.

distance links, less sensitive detectors, and tapped data bus applications that have formerly been possible only with the use of lasers.

Another way to keep an optical signal strong enough for detection is to produce it at a wavelength that is not attenuated by the media. The optical fibers now available degrade signals at 1300 and 1550 nm very little. So although characteristics are good at the 800-900 nm range, current research is in sources at longer wavelengths. Until recently, only lasers could efficiently operate at 1300 or 1550 nm, but lasers are less reliable and more expensive than LEDs. LEDs with an emission wavelength of 1.3 and 1.55 microns are available from Lasertron (Burlington, MA). RCA (Lancaster, PA), ITT (Roanoke, VA), Plessey (Irvine, CA), NEC (Japan) and Laser Diode offer 1.3 micron LEDs. The lower prices and reliability of LEDs could help system costs and maintenance stay low in long-wavelength systems.

Lasers have an advantage in modulation speed (generally referred to as rise time and fall time) over LED sources. However, experimental heavy zinc doping of InGaAsP active layers, decreasing active layer volume and other fundamental LED structural changes have improved speed to allow several hundred Mbit/sec transmission. Lab tests have even demonstrated speeds over 1 Gbit/sec, but the cost in output power prohibits their use in many designs.

For extremely high speed, long distance wide bandwidth applications, lasers will dominate. Much work is on single mode laser diodes for communication, with a focus on buried heterostructures (BH) and double heterostructures (**Figure 2**) due to their efficiency and relative stability. There are many laser structures being researched that provide various desirable characteristics. This new class of single longitudinal mode lasers could be critical to the success of wideband optical local area networking; their advantages include good power out (10-20 mW typical) as well as good response times. With multidrop data buses, power is crucial because some power is lost at each tap coupling a node onto the line. The number of nodes also puts demands on response time, since the goal of a network is to provide access to remote data as rapidly as to local data.

Two methods for producing AlGaAs lasers with high power single mode output signals have been developed. One, shown by RCA's CDH-LOC (constricted double heterostructure large optical cavity) laser in **Figure 2**, is to produce a large lasing spot size either by thinning the active layer or by increasing the size of the optical cavity combined with some method of guiding away undesired modes. Another way to achieve high power of a single mode is the use of nonabsorbing mirrors at the facets by burying the facets in high bandgap material, growing thin active layers near the facets or Zn diffusion.

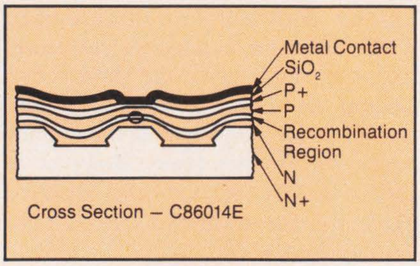


Figure 2: One way to achieve single longitudinal mode light out of a laser is by enlarging the lasing spot and making antiguide layers, as in this C86014E CDH-LOC laser structure from RCA.

Such GaAlAs lasers operate in the 800-900 nm wavelength range (simple GaAs emits at about 900 nm; the Al allows shortening the wavelength), and though fiber loss is somewhat higher for those signals than longer ones, less expensive silicon detectors can be used in these systems. The alternative, with Indium introduced, is long-wavelength lasing. The move towards 1300 and 1550 nm systems is strong for long-distance telecommunications. This has been a dramatic surge, as only two years ago, most of the work in this area was still experimental.

As the telecommunications market for lasers and LEDs increases, advantages pass along to all optical systems. Not only are economies of scale possible (though right now, the demand for sophisticated emitters is keeping some prices high), but manufacturing advances improve the consistency and reliability of devices. Laser lifetimes, especially with any temperature changes, have been a drawback, but the advances are impressive.

Further increases in predictability of laser performance come with new packaging techniques. Temperature sensing and control in the transmitter module reduce thermal effects on the lasing threshold. Refresh circuitry for a laser allows periodic checks to set electronics for stable emission characteristics throughout the lifetime of a device.

Lasers can also be used for transmission without a fiber; free-space communication systems benefit by the work in optical fiber systems, but are not constrained by the attenuation and dispersion characteristics of a fiber. Applications such as linking buildings across a street or within factories have used lasers effectively through space; companies like Codenoll Technologies (Yonkers, NY) offer commercial free-space laser systems.

Though lasers were developed 25 years ago, they have never been produced in sufficient volume to enjoy cost reductions or manufactured consistency. Quantity production of lasers for optical memory recording may have positive carry-over advances for communication lasers, even

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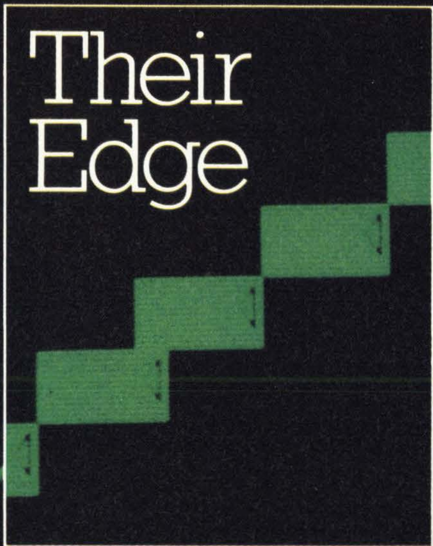

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though optical recording uses short wavelengths and small spots, relative to the output of emitters for fiber optics.

A Thin Line

Advances in materials for and the manufacture of the fiber itself could also improve optical system performance. There is much disagreement as to what size and type of fiber will be most useful for data communications. Parameters and tradeoffs are shown in **Figure 3** for graded and partially graded index silica, plastic and plastic clad silica as well as silica single mode step index fibers. As suggested by the advantages to each of the four possible directions on the axes, priorities of an application could dictate any of the available fibers. The choices of sources, detectors and connectors that rest on fiber type can be more critical to system cost than the fibers themselves, especially in relatively short haul data systems.

The 50 micron core/125 micron cladding graded index fiber (often called 50/125 fiber) has been manufactured in greater volume and for longer than other fiber types. As a result, consistent core alignment and NA is achieved, for fiber near its theoretical transmission limits of dispersion and attenuation. Single mode fiber is now being used in quantity for telecommunications, too, so manufacturing stability is coming about for this very fine core—5-10 micron—fiber. Consistency improvements, particularly in core diameter and alignment, will prove critical to the spread of single mode technology, as alignment for splicing and connectoring has been the biggest drawback to its use.

Research and development are improving the loss characteristics of all types of optical fiber. With the increasing interest in single mode transmission, the depressed index cladding single mode waveguide is worthy of attention. By lowering the refractive index of the material used in the cladding portion of a fiber with phosphorus-fluorine doping, as little as 0.3 dB per Km loss at 1.3 micron wavelength and 0.16 dB per km at 1.5 microns have been reported by AT&T Bell Labs.

There is debate as to whether single mode transmission is ideal for data communications. Traditionally very high loss plastic fibers were considered optimum for computer applications. For short links, products like Hewlett-Packard's Snap-In Link line use plastic fiber with losses of 500-1000 dB per km. The 20-30 meter limit this attenuation dictates still allows communications within equipment and across backplanes. Manufacturers of plastic fiber, notably DuPont (Wilmington, DE) and Mitsubishi (Sunnyvale, CA), are making strides in material purity and manufacturing that could double those lengths and allow 50-100 meter point-to-point links between computers and I/O devices in an office.

Larger core silica fibers have been popular, as well. They combine better loss characteristics than plastic media with a larger core and higher numerical aperture than graded index silica fibers (**Figure 3**). The NA and core size improve power coupling, especially from an LED, as suggested by **Figure 1**, and 100/140 silica fibers are considered a standard for data communication. Still, more material is required to make a length of large core fiber, which could keep costs higher, even if the quantity manufactured matches 50/125.

Material and manufacturing improvements for fibers are ongoing, with lower attenuation and higher bandwidth fiber produced in each class. Plastic fiber and the active devices to make very short connections are extremely inexpensive solutions to noise problems. Relatively low speed data links such as RS-232 generally use 100 or 200 micron core fiber with several dB per km loss. The telephone industry is driving high quality, wide bandwidth fiber to strict specifications, with minimal impurities or inconsistencies.

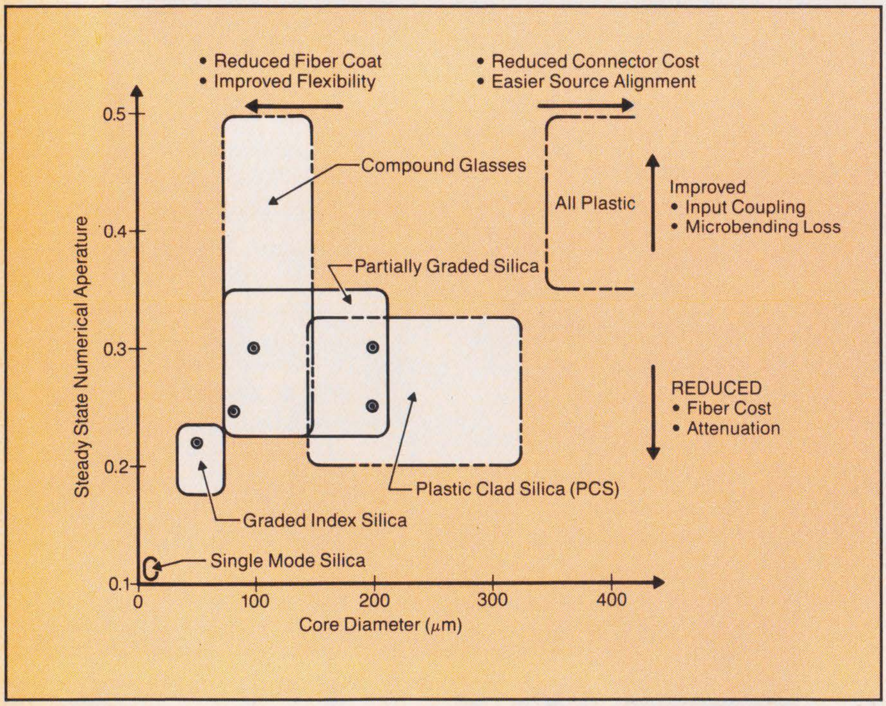

Figure 3: Numerical aperture and core diameter are fiber parameters that vary by type, as shown. Advantages of going either direction on either axis make fiber type choices variable with application.

Optimal Coupling

Connections have long been seen as a problem for optical data communications. Unlike telecommunications lines that can be permanently spliced together, computer links, and especially networks, need the flexibility of unhooking and reconnecting. Methods for automatic mechanical alignment such as grooved or biconical guide pieces are commonly built in to connectors. Since placement is mechanical, fiber tolerances determine power coupling at the connector (**Figure 4**). As core concentricity, numerical aperture and core and cladding diameter are more consistent throughout manufactured fiber, this mechanical alignment of the outside of any two sections of fiber has a better chance of producing cores aligned for maximum power transfer. Alternatives to large air gaps between the fiber ends have also been proven, in fluids that match the refractive index of the fiber cores.

Though no simple plug-in connection (except for packaged data links, for which the supplier must connector the fiber) is yet possible, connections of very high quality can now be made in under five minutes with certain connector types. Until recently, a method using epoxy and sev-

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eral fiber end polishing steps, as well as care in alignment, made each connection up to a half hour job.

Connections between active devices at both transmitting and receiving ends of a link and the fiber between are critical to system performance, too. Methods from building a short piece of fiber into the package, called pigtailing, to having a collimating lens and fiber alignment apparatus at the source output or detector input are in common use. Better designs are taking the guesswork and sensitive testing for alignment out of active device-to-fiber coupling, so packages perform more predictably to data sheet specs for power out of a pigtail or power coupled into a fiber.

In some cases, simple links are not enough. Extensive development has brought about a variety of passive directional and star couplers that provide a reliable method of producing networks and multidrop links. Fused couplers, in which fibers are fused together into a junction where their cores partially transmit through each other, are available to split signals evenly or tap off only a small percentage. Recently, such devices have been demonstrated for single mode 1300 nm transmission by ITT (Roanoke, VA) and others. Passive couplers of several fibers joined at one point have been the basis of optical local area network (LAN) designs, but the power out is typically low.

A star coupler with 19 ports in, 19 out and monitoring capability is under joint development by Siecor FiberLAN (Research Triangle Park, NC) and Kaptron (Palo Alto, CA). Since the power out of such a large number of ports of a passive star can vary as much as 10 dB depending on the distance of the node from the coupler, monitoring on every line is critical. By pulling off 5% of the signal for monitoring, all 19 ports can operate, and if one fails, only the collision detection is lost, not, as with an active star, the entire system.

Active couplers and stars have been developed by companies like Aetna Telecommunications (Westboro, MA) specifically to address the range between telecommunications, where expensive wavelength division multiplexing devices are cost-effective to save multiple fibers over very long lengths and very short haul links that can use multiple fibers and relatively imprecise and inexpensive connectors. The Aetna design has shown just over 1 dB excess losses.

As suggested by the extremely wide bandwidth of optical fiber, many low level signals may be multiplexed over a fiber. Wavelength division multiplexing (WDM), first suggested in 1977, is still a fairly expensive process, but many approaches are being taken and devices are in field test now. Filters, lenses and gratings that separate optical signal wavelengths can be used to separate signals by 30-50 nm, ensuring that only one of the detectors will pick up a particular wavelength signal. The current work in stable single mode lasers should help keep signals separate in WDM devices; if mode stability is improved, each receiver is more likely to pick up signals intended for it and not another channel.

Though expensive now, WDM holds great promise for future upgrades of optical systems. A fiber cable already installed can carry as many signals as a multiplexer combines. Adding multiplexers and demultiplexers to systems will increase the cost-effectiveness of a single fiber, and allow mixing of different types of signals, such as video, data and voice on one line. Dual wavelength multiplexers have been developed by Kaptron, ITT, AT&T Bell Labs, Burr-Brown (Tucson, AZ) and others, and are available to expand a fiber's channel capacity in one direction or make bidirectional links.

Needs Now

Most fiber optic data links are now being sold for military, industrial and other special systems. Since most data is at speeds and bandwidths that coax and wire cable can handle, current driving forces for using optical communication are special environmental demands.

The #5 ESS switch developed by Bell Labs uses internal optical data links to improve circuit isolation and reduce crosstalk and the effects of EMC. The result is a very low bit error rate; after 6 million hours, the 960 links had caused no known errors. In addition, the fiber cable is light weight, small to keep cable congestion down, and allows the flexibility of remoting interface modules. For this densely packed area of links (**Figure 5**), the problems avoided with optical links is worth the small extra premium of a link using LED sources and simple PIN detectors over 50 micron core fiber.

The military has been a mainstay for optical equipment manufacturers, with their need for security, reliability and, in many cases, portability. The Navy's SubACS (Submarine Advanced Combat System), for which IBM (Manassas, VA) is prime contractor, uses optical data bus links. The MIL-STD-1773 bus is a new standard, with fiber media in place of the copper cable used for the 1553 that is a required military bus interface.

There are also current installations that make use of the long distance that a high bandwidth signal can travel down fiber. Phenomenal increases in the capabilities and speed of machines inexpensive enough to be distributed through a facility make for a jumble of cable with distance limitations. A desire for local area networking is strong, and though current configurations allow most links over coax or wire, companies like Proteon (Waltham, MA) frequently install at least one

(continued on p. 119)

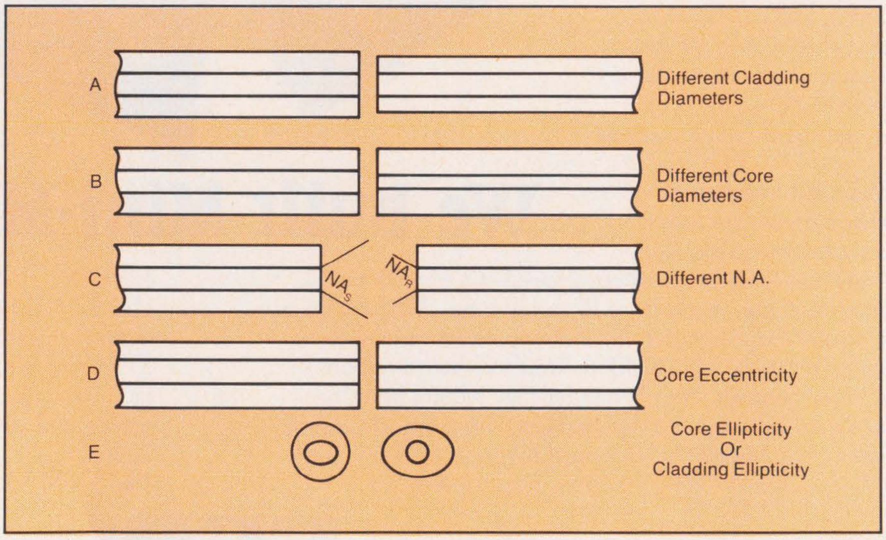

Figure 4: Mechanical alignment in connectors makes fiber tolerances important for matching cores and thus coupling power through.

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Remoting RGB Color Workstations Optically

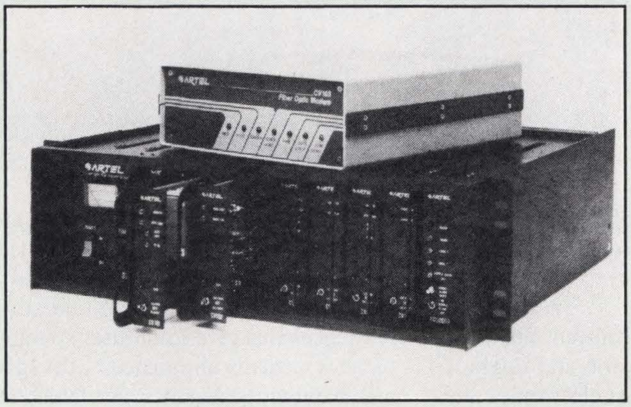

Figure 1: Transmission of RGB signals for 1280 × 1024 raster displays can be transmitted over more than a mile of optical fiber with the Artel CV-103 modem and CV-101 and -102 modules in the rack configuration shown; the right-hand module is an alarm unit.

Figure 2: Indicator lights on a module card provide monitoring of transmission from the front panel.

Color computer graphics are especially useful for CAD/CAM, and mainframe-based graphics systems provide fast, sophisticated manipulation capabilities in real time. There is, thus, a drive to place interactive color workstations in designers' offices, remotely connected to a host display generator. But the ability of coaxial cables to transmit wide bandwidth signals like those for color graphics displays decreases over distance. Even RG-11 video coax cables roll off after 250 feet. The bandwidth/ distance characteristics of optical fiber make it a sensible transmission alternative.

High resolution monochrome computer graphics signal transmission over fiber optics for Computervision and IBM mainframe CAD/CAM systems is possible with interface modules from Artel Communications Corp. (Worcester, MA). The newest addition to the product line is a modem for RGB color signal transmission on Computervision (Bedford, MA) Designer systems.

The CV-103 modem is placed at each Computervision Instaview C color workstation to be remoted. At the Video Display Generator (VDG), an optical transceiver module card (CV-101) and dual channel video transmitter card (CV-102) are used in the S2000 nine-slot rack (**Figure 1**) for each remote workstation. Both modem and rack are designed for plug-compatibility with Computervision equipment.

To transmit the three color signals (red, green and blue) to a workstation and data in both directions, the optical cable must contain four fibers. This single slender cord replaces three coaxial cables and a ribbon cable. Even with 1280 × 1024 displays, optical cable allows transmission over a mile. If several workstations are located near each other but remote from the VDG, a 16-fiber cable that is 0.5″ diameter can be used for four workstations, connecting in to multiple cards in the rack at the VDG.

One feature of the system is the built-in SL2000 test unit and additional monitoring can be added by the ACU2000 alarm control unit (**Figure 1**). These provide alarm, self-test and on-line monitoring of transmission. Indicators on each module show the status of video and data signals, as well as optical levels and module operation.

With high bandwidth graphics signals more in demand, and as color aids the designer, coax can be a limit on workspace allocation. Using lightwave transmission from a host to workstations allows CAD/CAM power to come to the designer's desk, wherever in a facility that may be. **Write 316**

(continued from p. 112)

link of a network in fiber.

Long distance links, high speed mainframe links and multiplexed backbone optical links allow greater flexibility and connectivity for networks. Sometimes, laying a cable between buildings is not possible because of right-of-way restrictions, and a free-space laser link is more suitable. Again, these are special sections of a network. Though entire networks can be made optically, current protocols and network use do not exercise fiber's advantages well enough to make the venture economic.

Multiplexing standard data channels brings economy, and fiber allows longer links than standard cable. For example, RS-232 multiplexers for fiber transmission available from Optelecom (Gaithersburg, MD), Hewlett-Packard and Fibronics (Hyannis, MA) extend the range without a change in cable. Transmission over a single, small optical cable of several channels can be not only a distance advantage for remoting, but much easier to install and less bulky in congested areas.

High resolution graphics generated on a host and downloaded to workstations are prevalent for computer systems, and demand good bandwidth for a single channel. A 1024 × 1024 screen requires over four times the bandwidth for a single screen draw of a 512 × 512. The simultaneous trend toward faster refresh rates pushes bandwidth even more, making coax work to its limits.

Systems like those from Artel (Worcester, MA) and Fibronics are designed for color graphics links. These products allow terminals and workstations dependent on a mainframe to operate in the designer's office, even if it is several floors away. A slender cable with only a few fibers provides better performance over distance than a special graphics cable so large as to be inflexible. Image processing, industrial monitoring and other video systems are even more demanding of bandwidth. The limits on camera to processor distance, as well as the prevalence of electrical noise from other equipment, make copper links cumbersome.

Fibered Future

Designers of systems for special applications are looking at optical transmission now. Just as the move from 8- to 16-bit processors was initially only for sophisticated machines and gradually spread to the desktop, the market will expand as people learn to use available power. Higher speed computing and distribution of access to data are trends that are changing how people work. Once transparent communication is accepted as the norm, demand will skyrocket.

LAN activity is proof that access to data is valued greatly. Current Ethernet and similar bus networks are not ideal for optical media, but point-to-point physical configurations will allow efficient use when needed. Ungermann-Bass (Santa Clara, CA) and Codenoll offer Ethernet optical equipment. But the bus protocol and interface standards are a bottleneck to system performance. Networks between mainframes, and between foreseeable workstations that operate at high speeds will demand the bandwidth/distance performance of optics and totally new networking schemes. Multigigabit transmission by very high speed active devices, preferably in arrays for parallel transfer, could meet the needs of even sizeable networks of faster machines.

All-optical networks could include voice and video services along with data. Not only office, but also industrial, military and design installations could be greatly simplified by a single very high bandwidth optical network to carry all signals. Even now, for new installations, the cost of leased telephone lines is prohibitive and installation of facilities for all of the services needed requires a different cable for each type of signal. A fiber system would allow all current channels, plus room for expansion and upgrade with no new cable, just electronics and perhaps multiplexers at the ends.

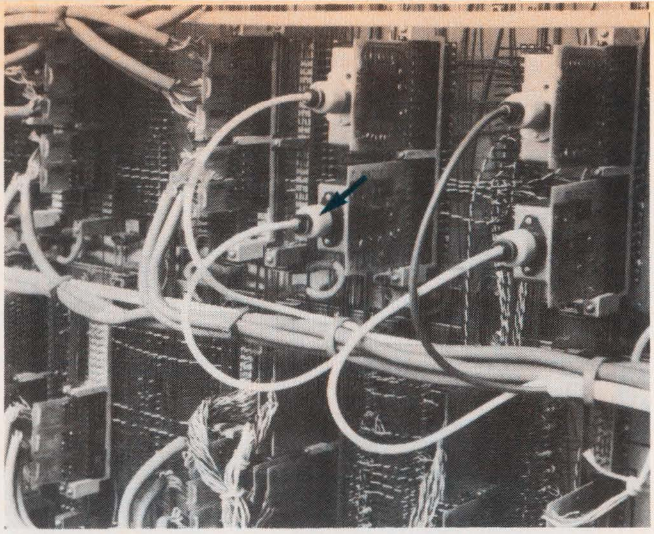

Figure 5: The wiring of a #5 ESS switch is extremely dense; the fiber optic cable, indicated by the arrow, relieves noise and congestion problems in AT&T (Western Electric) equipment.

Mainframe speed is also pushing limits of I/O channels, especially to memory. More devices are being hooked into main CPUs, and the ability of several mainframes to access each others' peripheral devices and files could be advantageous. With the number of devices in mainframe computer centers now, mutual immunity to interference can be crucial. The ability to upgrade speed as faster peripheral devices are available is also a bonus to optical cable.

Multiprocessor computing centers can benefit from sharing memory, but again, with copper and coax, speed and distance are limited. A shared memory network such as that envisioned by IBM between mainframes would require fairly short bus links carrying Gigabytes of information. These mainframe I/O and memory channels may become a reality, though IBM, according to their paper at the OFC conference, expects BERs will need to improve from 10^{-10} to 10^{-12}, with low failure requirements that have been met only by some lower performance components.

Of course, an all-optical computer, which has great potential if an optical IC is successful, would lead to greater extremes of speed and efficiency. Optical to optical coupling and driving, eliminating electrical signals would be a revolution. Though optical computing is not directly at hand, integrated optical components are beginning to bring optical transmission into the computer. Someday, connections between ICs, boards and out to peripherals and networks could be achieved optically. These prospects would change the design of digital equipment.

However, even current optical links change designs. The communications bottleneck that gives multiuser systems a niche is virtually eliminated by the speed and bandwidth/distance available over optical connections.

The main changes resulting from the bandwidth are for the future. If equipment speed or protocols change, or if several machines need access to the same port that served only one before, the cable can handle that with little signal degradation. The trend for increasing speed, graphics capabilities and multiprocessors suggests that building wide bandwidth links may be necessary soon.

Digital to analog buffering circuitry, repeatering and EMI/RFI protection are redundant with optical links. The security, small size and light weight that are driving current uses will be bonus features as optical systems are designed in to meet bandwidth and distance needs.

Optical components are already being better designed to meet data communication needs. Standard DIP packages and connectored devices take the mystery out of devices. As demanding computer applications develop, the manufacturers of optical equipment will optimize and modify basic designs. The combination of high quality, reproducible optical devices and huge increases in the amount and speed of computer operations are compatible trends, opening special corners of transmission as well as unheard-of intercomputing horizons. □

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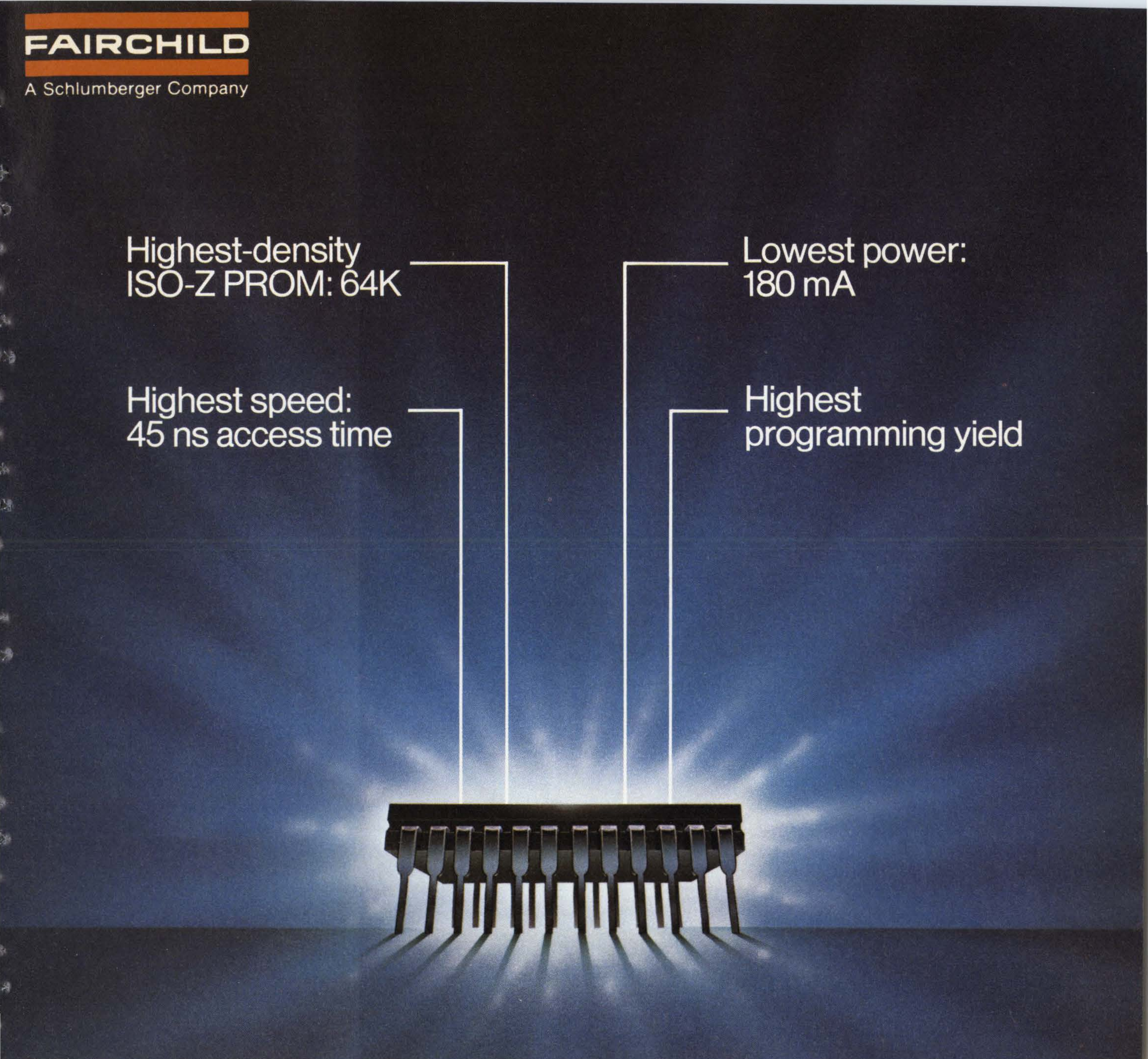

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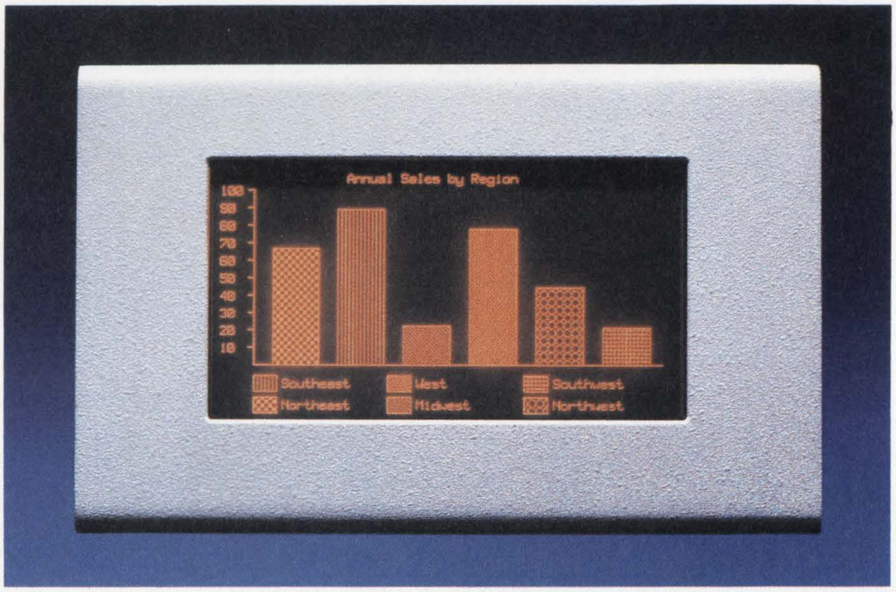
Trends In Flat Information Display Technology

by Joseph A. Castellano

To serve a broader base of operators, and computers, word processors and terminals are being made less intimidating. One aid to "friendliness" is a personal, dynamic visual display. As computing functions become easier to use and more powerful, they become inseparable tools, so it will be important to package all hardware into a compact and transportable unit.

Traditional CRTs require a minimum depth of six to 12 inches (depending upon diagonal measurement) to maintain clarity at the periphery as the beam scans the face. Larger, high resolution tubes require even more depth. In contrast, flat panel display depth is essentially independent of viewing area. This means that eventually a computer or terminal could truly be configured as a "dynamic notebook" using a high information content flat display.

The main reason so few products use flat panel displays is cost. None of the numerous techniques for producing these flat displays is manufacturable for less than about five times the cost of a CRT. The cost of flat panel displays is largely due to the cost of the drive and peripheral electronics; the "glass" portion typically represents less than 35% of the display "module" cost. In addition, most are not yet capable of CRT performance as they lack speed, color, viewing area, resolution or high contrast.



The PlasmaGraphics™ 120 flat panel gas plasma display offers graphics capability as shown here. The image is composed of 120,000 addressable pixels arranged in a 25-line by 80-character format and is housed in a compact 7″ × 10″ × 1½″ case.

Flat Cathode Ray Tubes

The CRT will continue in the near term, to be the dominant display device. In the past few years there has been considerable research devoted to developing truly flat CRTs; two types of small flat CRTs have resulted, from Sinclair Research (England) and Sony.

In the Sinclair device, the electron beam is initially projected parallel to the screen. As a result, it has a 0.175 screen area of 4″ × 2″ and a thickness of only 0.175″. Sinclair has begun manufacturing the device for use in a miniature black and white TV sets having dimensions of 6″ × 4″ × 1″.

The Sony "flat" CRT with a 2″ diagonal screen was incorporated into its first "Watchman TV" product, the model FD-20. The structure consists of two parallel pieces of glass, but the back plate, which is coated with a phosphor, is actually slightly curved. In the FD-20, the tube is viewed through a front piece that uses a transparent electrode for focusing. The electron gun and horizontal and vertical electrostatic deflection plates mounted between the two glass plates, bend the electron beam through 90° so it strikes the phosphor screen. Sony recently reversed the position of the plates with respect to the viewer, eliminating the curved screen.

Philips Research Laboratories (Surrey, England) have also reported on a flat CRT, but for computer terminal applications. Tested in a demountable arrangement in a vacuum system, it produced a 14cm × 18cm TV picture with reasonably good resolution. But Philips isn't saying when the company will begin to manufacture these devices.

For several years, RCA has been developing a large screen, flat panel color TV receiver with a display area of 75cm × 100cm and a thickness of only 10cm. The scheme is based on multiple guns and structural guiding of the multiple electron beams. Three beams in each module scan across the mask to create the picture; off-the-air video in full color has already been demonstrated. Conceptually, this display could be used for computer terminals as well as for TV. However, the cost

Joseph A. Castellano is President of Stanford Resources, Inc., San Jose, CA. He is involved in the study and marketing of the electronic display industry. He has been a part of the display industry for almost 20 years.

The result of flat display development work could be a computer or terminal configured as a "dynamic notebook."

to manufacture this type of panel will be high because of its complex structure.

For computer applications the flat CRT will likely enter the market later in this decade, mainly for desk-top and/or transportable computers; computer-telephones are another potential application. Certainly Sony, with its technological lead in small flat CRTs, will be a leading supplier initially. Other CRT makers such as Toshiba, Hitachi, Matsushita and Mitsubishi are sure to enter the market later, and such companies as Philips, RCA, ITT, and AT&T are likely to join in. Thus, the worldwide market for flat CRTs used in computer applications is projected to reach $18 million by the end of the decade (**Table 2**).

Light Emitting Diodes

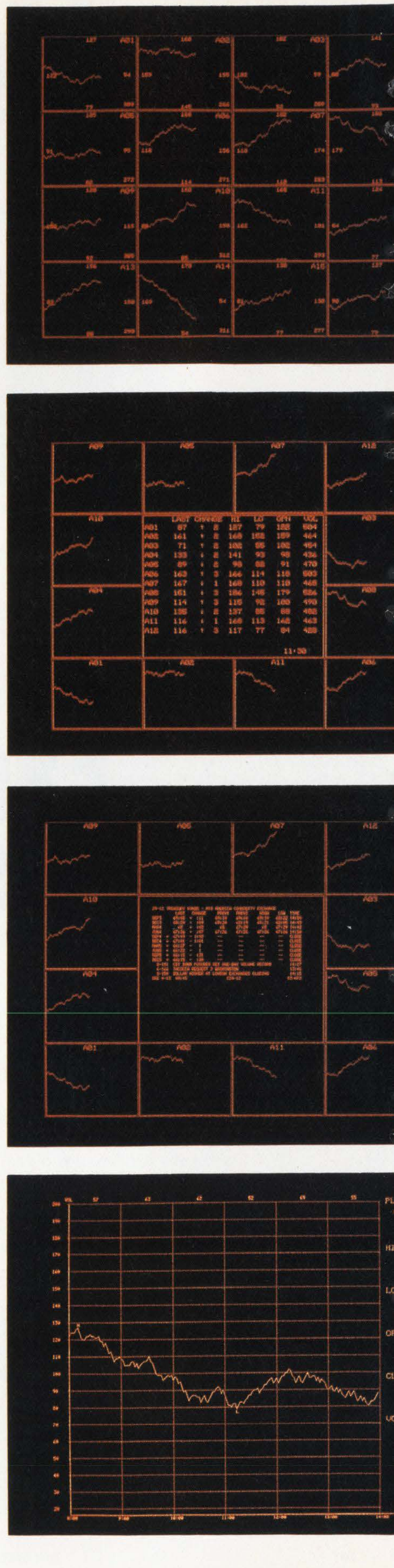
The emergence of highly effective LED light sources is another achievement of solid-state theory and technology. An LED typically consists of a wafer substrate of either single crystal Gallium Arsenide (GaAs) or Gallium Phosphide (GaP) on which a layer of GaAs 1-xPx is formed by vapor phase or liquid phase epitaxial growth. By appropriate doping with Zinc, Oxygen or Nitrogen, a P/N junction can be formed in the epitaxy layer. Thin films of Silicon Dioxide and Silicon Nitride are then deposited over the wafer as a protective layer. An important characteristic of the LED is that it is a diode, with the usual current-voltage relationship found in diodes.

The voltage drop across an LED is 1.5 to 2 volts and the current required is a function of the desired light output and the luminous efficiency. Typically, the power dissipated ranges from 0.1 to 10 watts/square centimeter of the display area. Because the LED mechanism is electronic, the rise and decay times are very fast, typically in the range 1 millionth to 100 millionths of a second. LEDs will operate from −100° to +100°C and typically have 100,000 hours or more of operational life.

The major manufacturers of LEDs are: General Instrument, Siemens, AEG Telefunken, Texas Instruments, AT&T, Matsushita, Sharp, Hewlett-Packard, Stanley Electric, Toshiba, and Sanyo Electric. Toshiba Corporation (Kawasaki, Japan) has developed a multi-color LED flat panel display. The 20″ diagonal panel is composed of 240 × 320 pixels; it uses 300 LED modules, each 20mm × 20mm and containing 16 × 16 red and green LEDs. Red and green Gallium Phosphide (GaP) LEDs are attached to cathode electrode rows on a ceramic substrate. On the back of the ceramic substrate, nine I/O terminals, nine current drive circuits, four current control circuits and two LSI logic circuits are attached using hybrid integration techniques. The display produces red, green and yellow and has a brightness of 150 ft-Lamberts. Power consumption, however, is 120 watts for the LED modules and 220 watts for the interface circuits. Toshiba claims that the display can be manufactured cost-effectively and sees its use in computer terminals for industrial control systems.

Sanyo Electric Co. (Osaka, Japan) has developed and demonstrated a TV display using a high brightness Gallium Phosphide green monolithic dot matrix LED structure. Using conventional IC technology, the monolithic display may be more cost effective than those with an array of individual LED elements on a board. Using a similar fabrication technique but with GaP LEDs that emit different colors depending on the voltage applied, Sanyo has also developed and demonstrated a multi-color graphic display. The prototype with 96 × 64 elements, produced a brightness of 50 ft-Lamberts and four colors: red, green, yellow and orange.

The rapidly growing personal computer market has become a large market area for LED lamps. Every disk drive uses one and many printers use not only LED indicator lamps, but digital displays



Four examples of the Plasma 16 Advanced Information Retrieval System. This flat-screen, high resolution display panel is driven by Eurodex's computer system and represents an innovative application of the IBM 581 Plasma Display Panel. The four screens are from the Reuters news agency showing up-to-the-minute market information.

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Modgraph

(Millions of Dollars)								
TECHNOLOGY TIME	**1983**	**1984**	**1985**	**1986**	**1987**	**1988**	**1989**	**1990**
Flat CRT	0	0	0	1	1	3	6	11
LCD	44	55	72	87	103	109	126	143
LED	107	115	122	128	137	138	146	156
Vacuum Fluorescent	24	27	29	32	35	39	43	48
Plasma Displays	46	38	42	44	44	45	46	48
Other Light Emit.	8	9	13	17	19	20	21	21
Non-LCD Passive	0	1	2	3	4	6	7	9
TOTALS	**229**	**245**	**280**	**312**	**343**	**360**	**395**	**436**

Table 1: The U.S. Flat Electronic Display Market Forecast.

as well. Multiple character LEDs are used in word processing systems, bank terminals, point-of-sale terminals and industrial data collection systems. The worldwide market for LED visible products for all applications showed a 10% growth in 1983 due to the economic recovery. The total worldwide market is projected to grow to $487 million by 1985 and $623 million by 1990 (**Table 2**).

Plasma Display Panels

Plasma display panels (PDPs) are based on the Neon glow discharge principle. A sealed glass envelope containing neon, or a similar noble gas is ionized when a sufficient voltage, defined as the threshold voltage, is applied across the electrodes located in the gas. The ionization of the gas results in a visible, typically orange/red glow. The glow continues even when the voltage is decreased below the threshold voltage. This is known as the holding or sustaining voltage. If the voltage is decreased further, the glow will extinguish. Once ionization occurs, the brightness of the display is directly proportional to the current passing through the gas. Also, the device has bistable memory and a switching threshold, essential factors for matrix addressing a large number of display elements.

In the late 1960s, Beckman (Fullerton, CA) and Sperry introduced seven segment PDPs. Later versions of this type of PDP were extended to include multiple-digits and alphanumerics. Because the segmented planar PDP requires expensive high voltage drive electronics, it has had increasing difficulty competing with displays based on LED, LCD, and vacuum fluorescent technologies. Today, there are only two US manufacturers of segmented PDPs: Cherry Electrical (Waukegan, IL) and Beckman Instruments.

Matrix addressing has been used to reduce the number of high voltage drive circuits. For example, if there are 10,000 display elements arranged in the format of 100 rows and 100 columns, then only 200 electronic driving circuits are required, as compared to 10,000 if individual switching is done.

Several types of PDPs are now being developed: DC matrix addressed, AC matrix addressed and hybrid. The AC types have become dominant for large numbers of characters. Companies currently developing and manufacturing PDPs include IBM, NEC, Fujitsu, Oki, Okaya, Plasma Graphics, Matsushita and ElectroPlasma. A typical display might contain up to 250,000 pixels with a brightness of 50 ft-Lamberts and a lifetime of 10,000 hours or more. The cost with the high voltage driver electronics is in the range of $800 to $5,000. Texas Instruments is the major supplier of high voltage IC driver chips.

Excluding sales related to government contracts for large-scale systems, the US Plasma Display Panel market in 1983 was estimated to be $46 million (**Table 1**). The US is and will continue to be the largest market region for these displays.

Vacuum Fluorescent Displays

Developments in vacuum fluorescent display (VFD) technology have also allowed the display of many characters as opposed to single digits. VFDs are constructed of three basic electrodes (cathode, grid and anode) enclosed in an evacuated glass chamber or envelope. The cathode is a directly heated, small diameter, oxide coated tungsten filament. The grid is a thin metal screen mesh. The anode, which is formed on an insulating anode base, is arranged in seven or more electrically independent segments for displaying alphanumeric characters. Alternatively, the anode may be segmented into a dot matrix array. In either case, each anode segment is coated with a zinc oxide phosphor material. The electrodes are insulated from each other and the chamber is evacuated to remove air molecules.

Most VFDs form multiple digits or characters by internally connecting all common segments of each digit and using control grids of each digit, independently. The multi-character display is used under pulse (multiplexing) conditions by activating each of the characters sequentially and activating the desired segments in phase with the character enabling pulse. The pulse rate is kept high enough so that to the human eye, the light output from each character appears to be constant and continuous. Colors other than blue-green are obtained by using different phosphor materials or colored filters. Driver ICs are available from Texas Instruments, National Semiconductor and Sprague Electric.

There are only four major manufacturers of VFDs in the world: Futaba Corpo-

(Millions of Dollars)								
	1983	**1984**	**1985**	**1986**	**1987**	**1988**	**1989**	**1990**
Flat CRT	1	3	5	9	15	23	37	60
LCD	390	455	534	617	705	745	844	935
LED	414	454	487	516	548	554	587	622
Vacuum Fluorescent	120	133	147	160	172	189	205	224
Plasma Displays	84	79	89	96	100	107	116	125
Other Light Emit.	16	19	22	26	28	30	30	30
Non-LCD Passive	0	3	7	11	15	20	24	30
TOTALS	**1,025**	**1,146**	**1,291**	**1,435**	**1,583**	**1,668**	**1,843**	**2,026**

Table 2: Projected Worldwide Flat Electronic Display Market.

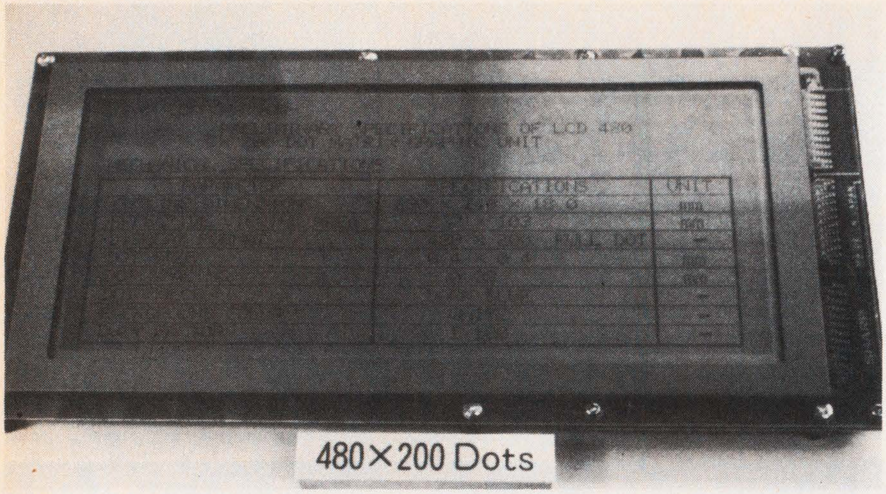

Figure 1: Sharp's high information content LCD.

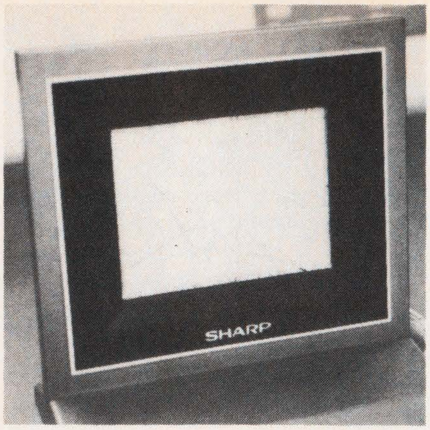

Figure 2: Sharp's electroluminiscent display.

ration, ISE Electronics (a subsidiary of Noritake Electronics), NEC Corporation, and Choa/Techna Display Corporation, a member of the Techna Electronics Industrial Group (represented in the US by MH&W International, Mahwah, NJ); all are located in Japan. In the US, two companies produce modules using VFD display glass: Industrial Electronic Engineers (IEE) (Van Nuys, CA) and Digital Electronics Corporation (DECO) (Hayward, CA).

ISE Electronics (Ise, Japan) has developed a 320 × 240 dot matrix VFD which emits two colors, green and orange-red. The device was constructed by using photolithography to deposit a pattern of blue-green and red phosphor dots. ISE plans to use the new concept in its future products for various applications including computers.

In a front luminous VFD (FLVFD) graphic display with 320 × 240 dots, developed by Futaba Corporation's R&D Division (Chiba, Japan), electrons excite the phosphor, which is coated on the transmissive anode to produce light emission. The panel has been used to display graphics, alphanumerics and TV pictures. Single matrix addressing coupled with a wire grid construction are said to offer lower cost manufacturing than previously high information content VFDs. Futaba hopes to use the technique to develop a full color display by placing striped color filters between the anode wiring and the faceplate or through the use of colored phosphors. A display with 640 × 400 dots at a pitch of 0.28mm is under development.

The current worldwide market for VFDs is $133 million and will show modest gains over the next few years. On a worldwide basis, the size of the market for dot matrix models is predicted to increase by a factor of five by 1990, to $53 million. The total worldwide VFD market for all applications will grow to $147 million by 1985 and to $226 million by 1990 (**Table 2**).

Liquid Crystal Displays

Liquid crystal displays differ from active light emitting types in that they modify (i.e. through scattering or absorption) or control light rather than generate it. This results in a device with very low power consumption.

LCDs may exist in a number of forms. Reflective displays use a reflective material behind the display and require front illumination. Transmissive LCDs, at some small loss in performance, operate by reflection of front surface light or by illumination from the rear. All types use a liquid crystal material sandwiched and sealed between glass plates which have pre-patterned conductive electrodes in contact with the liquid.

Liquid crystal materials are organic compounds which have the optical properties of solids but the fluidity of liquids over a specific temperature range. Operation of displays from −20°C to +70°C is now possible.

Today there are many modes of operation of liquid crystal displays. The Twisted-Nematic Field-Effect (TN-FE) is most commonly used in commercial products. It consists of a polarizer, the liquid crystal field-effect cell with thin electrode patterns on the inner surfaces, a second polarizer at right angles to the first, and a reflector for operation in the reflective mode. The inner walls of the liquid crystal cell are chemically treated to produce a uniform alignment of the liquid crystal molecules.

When voltage (above a specified threshold) is applied across the cell via the electrodes, the "twist" provided by the liquid crystal is temporarily destroyed. The polarized light conforming to the image of the energized electrodes can no longer pass through the second polarizer. The result is that in the "on" or energized state, the field-effect display appears as a dark image, due to the light absorption of the second polarizer, against a light background. Upon removal of the electric field, the liquid crystal molecules rearrange themselves and the twist is completely restored. The displays typically operate from 1.5 to 20 volts; power consumption is measured in microamps.

These TN-FE displays' contrast ratios change as the angle of view with respect to the display face changes. A "viewing angle" at which the display is clearly visible is the angle between a point normal to the display face and a point at which the contrast ratio falls below some figure (say 1.5:1).

Digital TN-FE displays a segmented electrode pattern on one of the plates and a common electrode pattern on the opposite plate. More complex schemes are used for multi-line, multi-character or TV displays. Integrated circuit driving and timekeeping chips for direct drive and multiplex operations are now being made by many companies, including Oki, Hughes, Commodore, Texas Instruments, RCA, National Semiconductor, Seiko, Sharp and Hitachi.

Within the past four years, a number of manufacturers have introduced various types of dot matrix LCD modules. Drive


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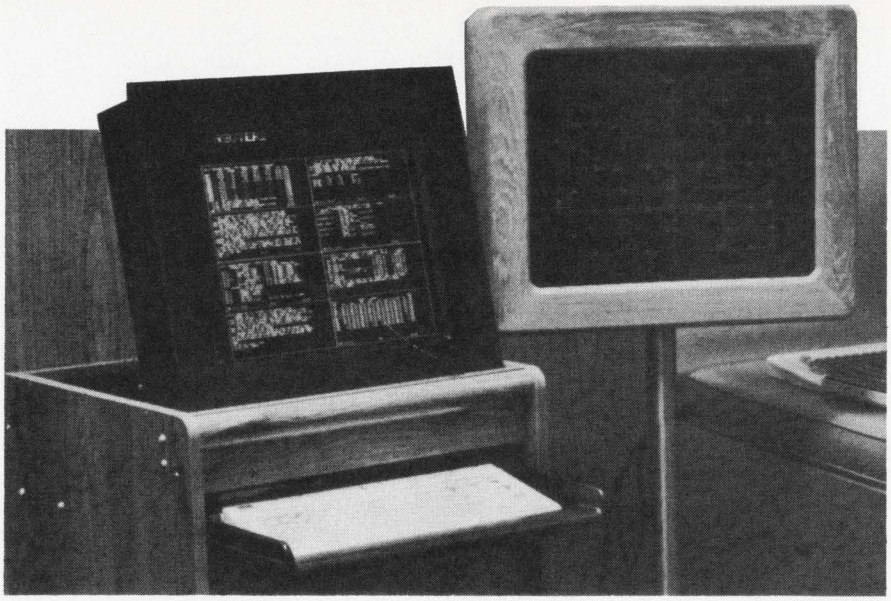
and peripheral electronics are mounted on boards that contain the display glass so that the display "module" is fully integrated. The addressing schemes are fairly sophisticated and often include temperature compensating circuits to eliminate "cross-talk" of unselected segments. Hitachi, Sharp, Seiko Instruments, Epson America, and Toshiba (AND) have taken the lead in offering these products to OEM companies in the USA. Sanyo, Matsushita and PCI (Printed Circuits International) also manufacture these products. Industrial Electronic Engineers and Densitron Corporation sell fully integrated modules using this LCD display glass.

One of the most successful products with a multi-line dot matrix LCD is the portable Model 100 computer marketed by Tandy's Radio Shack. This computer uses an eight line × 40 character/line multiplexed TN LCD and is made by Kyocera of Japan. The multiplexed display has fair contrast and adjustable voltage to change the viewing angle.

This development has led to a flurry of activity to develop LCDs with more lines and an 80 column format. LCDs with up to 16 lines and 80 columns are now available to the US market. Companies such as Gavilan Computer and Convergent Technologies have since introduced microcomputer products using these displays and more such introductions will be coming soon. A goal for these "lap computers" is a 25 line × 80 character display.

Most displays which offer more than 8 lines of characters, such as Sharp's 640 × 200 pixel display, have a relatively poor picture/image quality (**Figure 1**). They are used because no other display technology presently offers the low power consumption required for a portable computer application. When "active matrix" displays, which provide high contrast (> 10:1) over a wide viewing angle, become available later in this decade, these multiplexed units will be replaced.

The switching characteristics of LCDs limit the amount of direct matrix addressing; as the number of rows of characters increases, the contrast decreases. An active matrix or thin-film transistor (TFT) approach permits each display element to have its own individual electronic driving circuit. In addition, this approach has the potential of providing a means to integrate the row and column driver circuits, associated registers and buffer memories on the active matrix substrate.



The Plasma 16 System with Eurodex computer and IBM 581 Plasma Display Panel.

Seiko, Sanyo and Canon have been active in this area. Sanyo has developed a full color, portable LCD-TV using an amorphous silicon TFT approach and color filters. Seiko used color filters and polysilicon TFTs on quartz for its portable color LCD TV. In the US, PanelVision (Pittsburgh, PA) and Alphasil (Sunnyvale, CA), and CNET's Laboratory and Thomson CSF in France are also working on active matrix approaches.

A simpler way to produce highly multiplexed LCDs with good contrast over a broad viewing angle is to incorporate a two-pole, non-linear device inside the display structure. Researchers at Bell-Northern (Ottawa, Canada) used a metal-insulator-metal (MIM) approach to produce highly multiplexable LCDs. Recently, a team of researchers at Suwa Seikosha and Epson demonstrated a high contrast display that used a "lateral MIM" approach. It would not be surprising to see Epson make portable computers with these LCDs in two years.

The value of shipments of LCDs into computers/EDP applications on the US market will grow to $12 million in 1985 and $33 million in 1990. Other large market segments will be automotive dashboard displays. The worldwide market for LCDs used in all applications will grow from $455 million in 1984 to $935 million by 1990 (**Table 2**).

Electroluminescent and Other Emitting Displays

One of the oldest flat light-emitting display technologies is based on electroluminescence, which occurs when an electric field is applied to a thick or thin film of phosphor material such as Zinc Sulphide sandwiched between two electrodes. The color of the light emitted during this field application depends on the nature of the phosphor material. AC Thin Film Electroluminescent devices (TFEL) require high voltages (70+ volts) and thus, expensive IC drivers, to produce good light output.

In the mid-1970s, some significant advances in lifetime and performance of TFEL devices were reported by researchers at Sharp Corporation (Nara, Japan). Since then, a resurgence of activity in this field has occurred. In addition to work being done by Sharp, research is also being conducted by Aerojet Electro-Systems (CA); Lohja Corporation (Finland); Nippon Seiki (Japan); Rockwell (CA); GTE (MA); Planar Systems (OR); Fujitsu (Japan);, and various universities in the United States, Europe and Japan.

In 1981, Sharp began marketing EL displays for computer terminal application (**Figure 2**); mass production is to begin in 1984. Matsushita (Osaka, Japan) will market a similar product in late 1984.

The entrance of these major companies into the commercial TFEL field will no doubt increase the penetration of this technology into the ever-expanding microcomputer market. Up to now, the developers of TFEL displays other than Sharp have aimed their products at military markets. Most of the units sold in

Gas-electron-phosphor displays will not make an impact on the market until late in this decade.

1982 and 1983 were consumed by Grid Systems and several other microcomputer manufacturers for evaluation. Evaluation units were also sold to various companies engaged in developing military display systems.

Hewlett-Packard is believed to be seriously considering the introduction of a transportable computer using the EL display within the next two years. If this happens, other microcomputer makers are likely to get on the bandwagon and cause healthy increases in the market for these displays between 1985 and 1987. Sales of EL panels in 1983 were 3.5 times greater than they were in 1981.

The newest flat emitting technology is the GEP, or Gas-Electron-Phosphor display, developed about five years ago at Zenith Radio Corporation, and being further developed by Lucitron (Northbrook, IL). Siemens (Munich, West Germany) has joined with a venture partner to further develop its data terminal display using the concept.

The technology uses a cold-cathode glow discharge from which electrons are extracted at selected locations; the glow discharge is localized and scanned across the display. The electrons are then modulated and accelerated to impinge upon a phosphor coated screen which then emits light. Lucitron developed the technology for large screen flat TV displays. Siemens has demonstrated smaller panels for computer terminals. Gas-electron-phosphor displays will not make an impact on the market until later in this decade.

Non-LCD Passive Displays

With the development of the LCD, now the most widely used flat passive display, other passive technologies began to receive serious attention in the early 1970s. The impetus for this work was the belief that a high contrast, bright background passive display with low power consumption could replace or compete effectively with the LCD.

For several reasons, after nearly ten years, this has not happened. First, these other passive devices, for the most part, had serious long term reliability problems. Secondly, many required higher voltages and consumed more power than LCDs. The voltages required were generally unavailable with CMOS integrated circuits. Finally, some of the approaches required complex electrical driving schemes.

In spite of these problems, work on the technologies continues. In the case of electrochromics, watch displays using this technology were introduced recently by Seiko and it is expected that clock size displays for various consumer and industrial applications may be forthcoming soon from Seiko. Concerted efforts to develop 2,000 character alphanumeric displays for computer terminal applications using an electrophoretic display technology are underway at both Exxon and Philips. Litton Data Systems continues to develop its magneto-optic display concept.

Forecasts of the US and worldwide markets for non-LCD passive displays are presented in **Tables 1** and **2** respectively. The market becomes significant after 1985 when electrophoretic displays reach the marketplace; the major application will be portable personal computers. The worldwide non-LCD passive display market is expected to grow to $7 million by 1985 and to exceed $30 million by 1990.

Summary

As is presented in **Table 2**, the market for flat CRTs will grow from $5 million to $60 million between 1985 and 1990. Although the market for LCDs and LEDs will be about the same size in 1984, the LCD market will grow faster and reach $935 million by 1990. By 1990, the market for LEDs is expected to reach $622 million and the VFD market will be $224 million. Thus, the total worldwide market for all flat electronic displays is expected to exceed $2 billion in 1990. □

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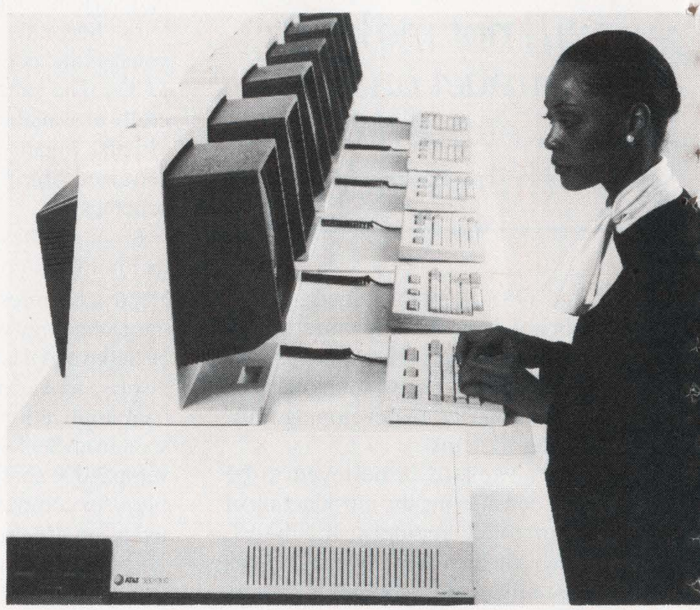
AT&T Enters The Field With A Full Line

The long-awaited announcement of products from AT&T's Computer Products Group (New York, NY) was no let-down. Six 32-bit models, from a desktop supermicro to a fault tolerant "duplex" supermini, are the initial members of the 3B computer family. All operate under UNIX and boast of high reliability; and, except the micro, all have proven themselves in the phone system. Communications were not ignored; an Ethernet-compatible local area network and an interface to the IBM PC were also announced. Except for the PC interface, the 3B products are already available to OEMs, VARs (Value Added Resellers) and selected large end-users.



AT&T's 3B2/300 32-bit microcomputer can support up to 18 users; it is shown here with the 5620 display.

Finally free to use technologies developed by Bell Laboratories in commercial computing products, the family uses Western Electric (now AT&T Technologies) WE 32000 processors and their 256K DRAMs. To address what they see as a whole new market developed around UNIX, the 3B line ranges from the 3B2 supermicro to the 3B5 mid-range minis (comparable to DEC VAX 11/750) to high-end micros in the 3B20 line, including a fault-tolerant model.

UNIX, developed by Bell Labs, has become popular enough to start new trade conferences. The extensive industry work in that system will encourage third-party software and portability. System V is even ported to the desktop 3B, and all of the line is optimized for multi-user UNIX. Third Party hardware is also encouraged, with the "open architecture" bus specifications to be published soon.

Though AT&T has decided not to enter the personal computer fracas, the supermicro 3B2/300 could give the IBM PC/XT a run for its money. The 300 can be accessed by as many as 18 users, or provide great power to a single user. The basic floppy and hard disk memory configurations use none of the four expansion slots, leaving up to 18 ports on a special I/O bus. Since the 32-bit processor and 256K DRAM are their own, AT&T can offer this high-end desktop from under $10,000.

Minicomputers in the 3B line do not require installation on a raised floor, special ventilation or air conditioning. Extensive diagnostics are also standard; on the 3B5 models, diagnostics execute automatically on power-up.

The basic AT&T mini, the 3B5/100, supports up to 40 users with specs at 0.63 MIPS. With the addition of a growth module, it becomes the /200, for 60 users and at speeds of 0.8 MIPS. The single Local Bus is kept moving by I/O Accelerators (IOAs) that offload interrupt processing from the CPU (or, as AT&T says, Central Control). An 8 Kbyte cache helps the speed of the WE 32000 CPU. Basic prices are $57,000 and $73,000 for the two models.

Also introduced were the high-end 3B20s, roughly competitive with DEC's VAX 780s. Like the 3B5s, the basic model, 3B20S, can be upgraded by adding a module, to become the 3B20A. Another similarity is the 8K cache; with the 12 Mbytes of main memory, the effective access time is 400 nsec. The 20s use two dual-channel DMA controllers, dual ported CDC disk drives with 300 Mbytes removable and 675 Mbytes fixed. The upgrade 3B20A adds a second CPU with the same main memory and memory update circuitry as the 20S. Microprocessor-based input/output processors and disk file controllers can act as FEPs, transferring blocks of data through DMA to main storage without CPU handling. These typically list for $230,000 and $330,000 for the S and A models, respectively.

The "Full Time" 3B20D achieves fault-tolerance through duplicate CPUs, 16 Mbyte main memories, cache, DMA disk controllers and I/O processors, the second of which takes over automatically when one is generating errors. Further error-resistance comes from parity checking, error correcting codes and operating system checks on hardware. A special version of UNIX, RTR, supports real-time, as well as UNIX's usual time-shared operation. RTR has a layered architecture matched by 16 hardware execution levels. The 3B20D lists at $340,000.

For communications, the 3BNET LAN provides 10 Mbit/sec Ethernet version 1.0 compatibility. Again using the WE 32000, intelligence is built into the interface unit, for lower network overhead on attached CPUs. According to Jack Scanlon, head of the Computer Systems Group, applications can run at 350-500 Kbits/sec over the coaxial network, including all protocols, contention and programs, for about $3,000 per node.

The only announced product not yet available would allow IBM PC users to access UNIX V through a 3B/300 desktop. In a PC network configuration, the 32-bit micro could take the place of a PC/XT for control and provide resource sharing.

To encourage third party support—and to get a sales team up and running—these initial products are only available to OEMs, VARs and big AT&T end-user customers. As Jim Olson, Vice-Chairman of AT&T said at the announcement, they

Rx FOR HEALTH

INSTALLMENT FOUR

By Lawrence Lee, MD

Dr. Lee is a leading Southern California Internist, specializing in cardiology. He is a co-founder and board chairman of LH Research, Inc. This column is presented as a public service for better understanding of topical medical problems and possible solutions.

HERPES!

SIMPLEX TYPE 2 VIRUS

Diagnosis and Treatment

DIAGNOSIS

(1) Clinical observation is made of the typical small clusters of vesicles (blisters) — most common form of recognition. (2) Isolation of the virus in a cell culture usually takes 1-3 days before the typical cell changes become visible. (3) Scrapings taken from base of vesicles are then stained to see if there are typical cell changes. (4) Blood specimens during and after lesions are then analyzed. If *primary herpes* is suspected, Herpes Simplex (HSV) antibodies can be seen in the blood *after* the initial lesions but *not* during the lesions.

TREATMENT

Primary infection — If the patient can be treated *before* or *during* the typical vesicle development, it is possible to cure HSV by preventing it from entering the nerves. The patient usually waits too long to prevent infection into the nerves. Early treatment with anti-viral drugs is still recommended because it decreases the number of nerves invaded.

Latent infections are not affected by anti-viral drugs, since they act only during the duplication cycle and do not penetrate the nerve cells. There presently is no known treatment for this stage of infection.

Recurrent mucous or skin lesions before vesicle formation — Anti-viral drugs initiated before the vesicles develop may prevent the typical vesicular lesions. A person can be alerted by the classic signals of itching, tingling or pain, which usually precede the actual vesicle clusters (ref. Instal. 3).

Recurrent skin or mucous lesions after vesicle formation — Treatment during this stage with anti-viral drugs has little effect on the lesions, except to reduce the duration of the healing process and its associated symptoms, and possibly, decrease the number of *new* sets of nerves that may be affected. Using drying agents such as zinc sulfate solution, antibiotic ointments to prevent secondary bacterial infection and topical anesthetics for pain will help. Currently, there is no FDA approved drug for recurrent episodes.

The only licensed drug for Herpes Simplex Virus 1 or 2 in the United States is ACYCLOVIR, an anti-viral drug which comes either in an ointment form or by intravenous administration (all recent studies indicate IV is the much more effective treatment). However, this does not prevent transmission to another person or eliminate latent infections.

IS THERE HOPE?? There has been much work done for specific vaccination of Herpes Virus. There is none available at this time. It is possible that a vaccine may help, or possibly some type of deactivated live Herpes Virus which may theoretically invade the nerve and thus prevent infection by the real HSV virus. But, in no way will this cure people who already have the herpes virus.

This is the fourth in a series of columns by Dr. Lee on medical subjects of current interest, although perhaps not fully understood, by the public. If you have a question, please write Dr. Lee at LH Research, Tustin, CA 92680.

Write 72 for Immediate Application. Write 29 for Literature Only.

bring technology, reliability, communications, price/performance and, most significantly for a newcomer in the computer market, staying power.

With a whole range of 32-bit architectures to build around and machines optimized around UNIX, compatible products could proliferate. —*Pingry*

Write 247

Changes In Telecommunications Industry Forecast

The number of private or bypass telephone networks in the U.S. will increase more than five times by the end of the decade, which could result in revenue losses of $9 billion annually among U.S. telephone service providers according to a just-released study, *New Directions in Telecommunications*, conducted by Arthur Andersen & Co.

These networks, which commanded just 2% of the companies in 1980, will be used by 11% of organizations in the U.S. by 1990 as they find it more cost-effective to develop their own systems rather than continuing to use the public network.

The study projects that the U.S. will become a net importer of telecommunications equipment. Imports will more than triple by the end of the decade, increasing from 5% of U.S. production in 1980 to 18% in 1990, with Japan capturing 42% of the U.S. import market followed by Canada with 23%.

Study projections indicate that, in 1990, over two-thirds of residential and business customers will own their equipment, while telephone features and functions will be the most important factors in the decision to purchase business instruments.

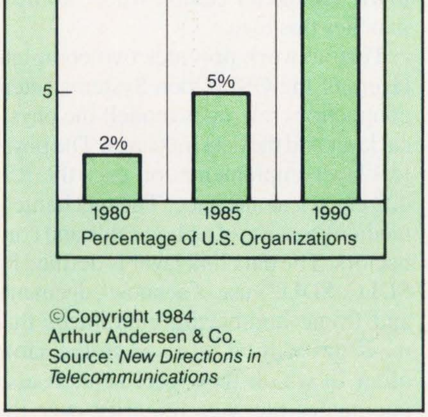


Figure 1: Private Network Growth.

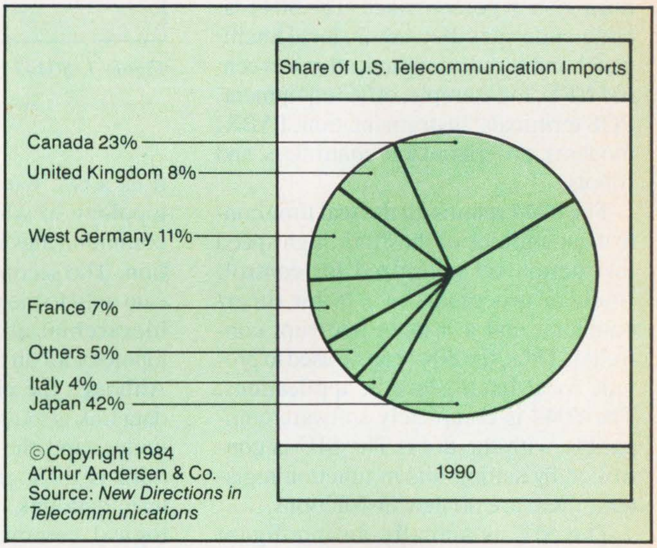


Figure 2: Share of U.S. Telecommunications Imports.

It is predicted that foreign producers will control a significant share of the U.S. office communications market due to advantages in price, installation costs, features and functions. However, it is expected that Western Electric (AT&T) will continue to have the largest segment of the PBX market with a 37% share in 1990.

Capital expenditures in the telecommunications industry are expected to rise dramatically, to $36 billion in 1990 from $22 billion in 1980. The most significant areas of growth will center on development and expansion of plant facilities for service providers and on research and development for manufacturers. In addition, companies in the telecommunications industry will devote 25% more resources to the marketing function in 1990 than in 1980.

In other findings, the respondents conclude that AT&T will continue to lead in long-distance transmission revenues; however, its share will be reduced from over 80% in 1980 to 64% in 1990. Other intercity common carriers, telephone companies and affiliates, as well as bypass networks, will share the remainder of the $65 billion in revenues.

In the areas of mobile communications, cellular radio telephones, virtually nonexistent in 1982, will be purchased at a rate of 550,000 per year by 1990. Sales combined with leasing contracts will put the cellular-installed base at 7 million units in the top 90 U.S. markets in 1990. More customers can be served by cellular than noncellular mobile telephones because cellular offers more channels and those channels can be reused several times in each city. Noncellular mobile phones use each channel citywide, restricting use to one call at a time.

By 1990, fiber optics will be the preferred means of transmission over microwave, copper cable, coaxial cable and satellites, according to the panelists. The major advantages of fiber optics will be: low maintenance cost; ability to handle voice, video and data; high-quality transmission; reliability; capability; expandability to meet demand; and the potential to handle technological advances.

Write 240

Networking With The 8044

The 8044 is a follow-up to Intel's highest performing 8-bit microcontroller, the 8051. With the 8044, Intel replaced the 8051's on-chip UART with a serial communication processor called the Serial Interface Unit, or SIU. The 8051-CPU and SIU operate concurrently to maximize system performance. The 8044 facilitates designs that require local intelligence and serial communication to a central CPU, for example, office equipment, POS terminals, instrumentation, PABX, modems, programmable controllers, and robots.

The 8044 retains all the real time control capabilities of the 8051: high speed instruction set optimized for control, Boolean processor, two 16-bit timer/counters, and a 5 input interrupt controller. Thus, the 8044 can be used to provide local intelligence in applications. The 8044 is completely software compatible with the 8051. The SIU is controlled by setting bits in function registers; there are no new instructions.

The SIU is actually an intelligent SDLC controller. Featuring an on-chip digital phase-locked-loop for data clock recovery for NRZI data, zero bit insertion/deletion and address recognition, the SIU supports data rates up to 2.4 Mbps. The SIU communicates to the 8051 CPU via an on-chip 192 bytes 2-port RAM, and interrupts the CPU only when a valid message has been received.

An important 8044 feature is the Automode. In the Automode, the 8044's SIU automatically recognizes and responds to primary station commands, thereby performing the communication function in hardware. In multiple chip designs, this command recognition function can take over 1000 bytes of code, which also ties up the CPU when a message is received. The 8044 features a flexible mode, in which the on-chip CPU manages communication activities for non SDLC networks, such as HDLC (e.g. addressing an unlimited number of stations), token passing, and CSMA.

The following application describes the design of an SDLC data link using the 8044 (RUPI)™ to implement a primary station and a secondary station.

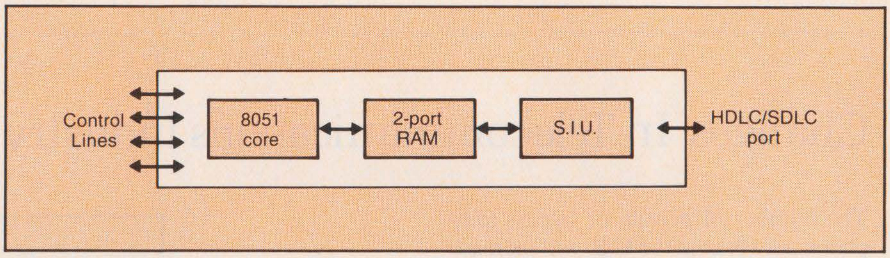


Figure 1: 8044's Dual Controller Architecture.

Application Description

This particular data link design example uses a two wire half-duplex multidrop topology in which the primary station communicates with each secondary station. The secondary stations communicate only to the primary. Because of this hierarchial architecture, the logical topology for an SDLC multidrop is a star. Although the physical topology of this data link is multidrop, the easiest way to understand the information flow is to think of the logical (star) topology. The term data link in this case refers to the logical communication pathways between the primary station and the secondary station.

The application example uses dumb Async terminals to interface to the SDLC network. Each secondary station has an Async terminal connected to it. The secondary stations are in effect protocol converters which allow any Async terminal to communicate with any other Async terminal on the network. The secondary stations use an 8044 with a UART to convert SDLC to Async. **Figure 1** displays a block diagram of the data link. The primary station controls the data link. In addition to data link control, the primary provides a higher level layer which is a path control function or networking layer. The primary serves as a message exchange or switch. It receives information from one secondary station and retransmits it to another secondary station. Thus, a virtual end to end connection is made between any two secondary stations on the network.

Three separate software modules were required for this network. The first module is a Secondary Station Driver (SSD) which provides an SDLC data link interface and a user interface. This module is a general purpose driver which requires application software to run it. The user interface to the driver provides four functions: OPEN, CLOSE, TRANSMIT, and RECEIVE. Using these four functions properly will allow any application software to communicate over this SDLC data link without knowing the details of SDLC. The secondary station driver uses the 8044's AUTO mode.

The second module is an example of application software which is linked to the secondary station driver. This module drives the 8251A, buffers data, and interfaces with the secondary station driver's user interface.

The third module is a primary station, which is a standalone program (i.e. it is not linked to any other module). The primary station uses the 8044's Non-auto or Flexible mode. In addition to controlling the data link, it acts as a message switch. Each time a secondary station transmits a frame, it places the Destination Address of the frame in the first byte of the information or I field. When the primary station receives a frame, it removes the first byte in the I field and retransmits the frame to the secondary station whose address matches this byte.

This network provides two complete layers of the OSI (Open Systems Interconnection) reference model: the physical layer and the data link layer. The physical layer implementation uses the RS-422 electrical interface. The mechanical medium consists of ribbon cable and connectors. The data link layer is defined by SDLC. SDLC's use of acknowledgements and frame numbering guarantees that messages will be received in the same order in which they were sent. It also guarantees message integrity over the data link. However, this network will not

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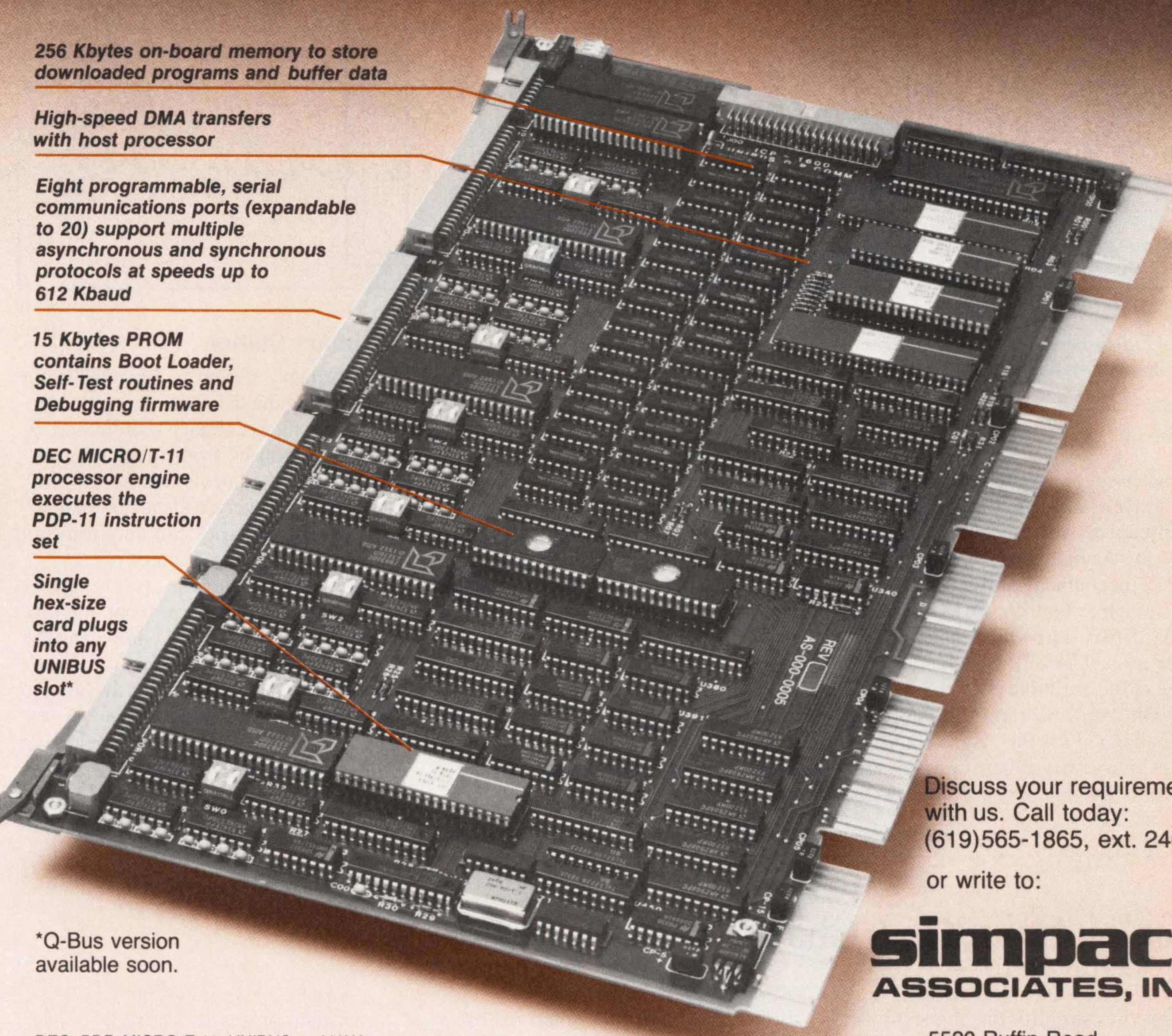

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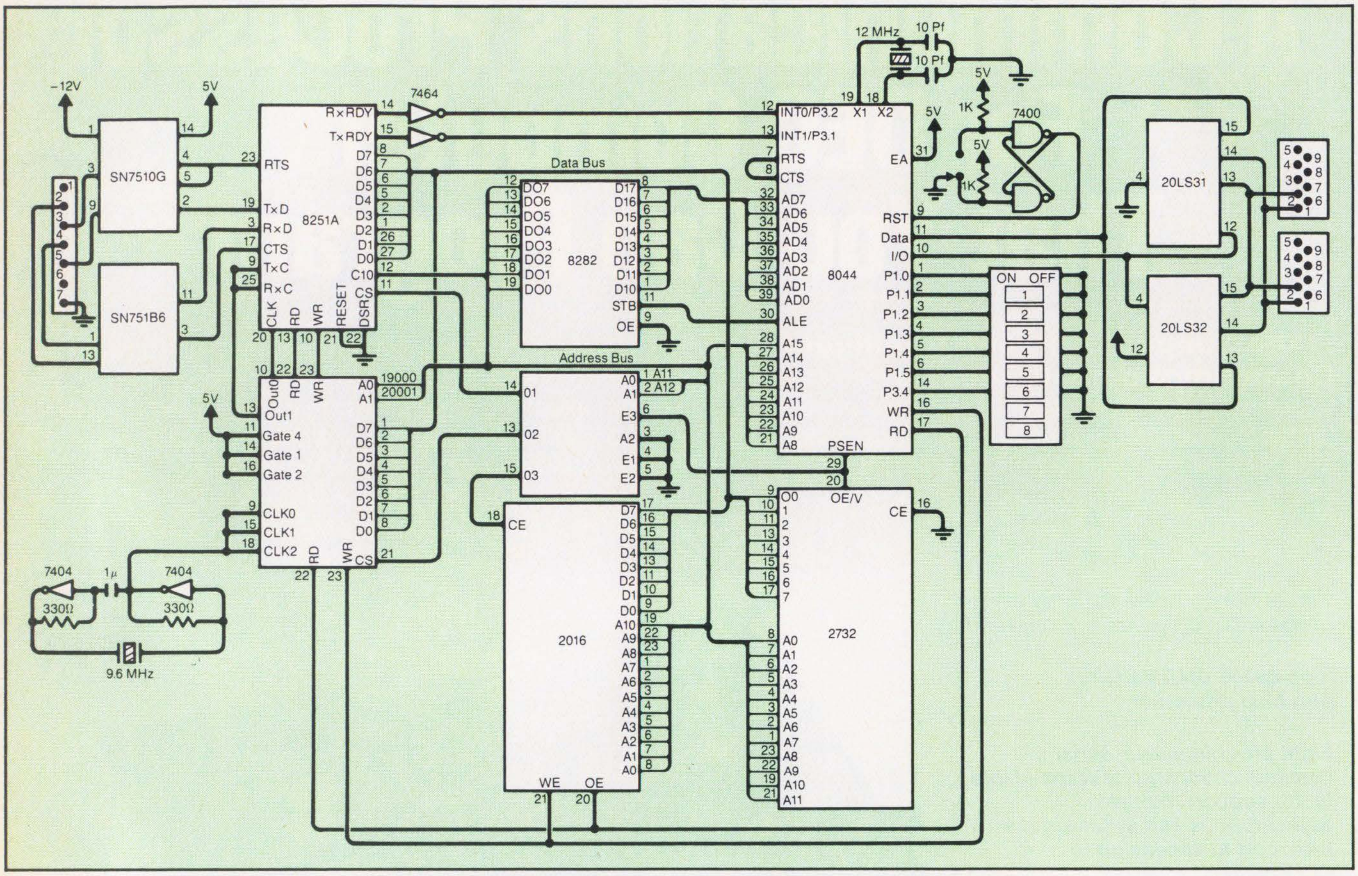

Figure 2: Schematic of ASYNC/SDLC Secondary Station Protocol Converter.

guarantee secondary to secondary message delivery since there are no acknowledgements between secondary stations.

For the Async interface, the standard RS-232 mechanical and electrical interface was used. For the SDLC channel, a standard two wire three state RS-422 driver is used. A DIP switch connected to one of the available ports on the 8044 allows the baud rate parity and stops bits to be changed on the Async interface. The primary station hardware does not use the USART, 8254, nor the RS-232 drivers.

Hardware

The 8251A is used as an Async communications controller in support of the 8044 (**Figure 2**). TxRDY and RxRDY on the 8251A are both tied to the two available external interrupts of the 8044 since the secondary station driver is totally interrupt driven. The 8044 buffers the data and some variables in a 2016 (2K × 8 static RAM). The 8254 programmable interval timer is employed as a programmable baud rate generator and system clock driver for the 8251A. The third output from the 8254 could be used as an external baud rate generator for the 8044. The 2732A shown in the diagram was not used since the software for both the primary and secondary stations used far less than the 4 Kbytes provided on the 8744.

Primary Station

The primary station is responsible for controlling the data link. It issues commands to the secondary stations and receives responses from them. The primary station controls link access, link level error recovery, and the flow of information. Secondaries can only transmit when polled by the primary.

Most primary stations are either micro/minicomputers or front-end processors to a mainframe computer. The example primary station in this design is standalone. It is possible for the 8044 to be used as an intelligent front end processor for a microprocessor, implementing the primary station functions.

– *Young Sohn, Charles Yager, Intel Corporation* **Write 230**

Analog Input·On 8 Channels

Designed to simplify the connection of analog input signals to digital computers, Datel Intersil's SDAS-8 is an 8-channel differential input A/D smart microsystem combined with a full-serial, full duplex terminal I/O port operated by an internal microprocessor. The serial port accepts input commands from the user's host computer or terminal and transmits

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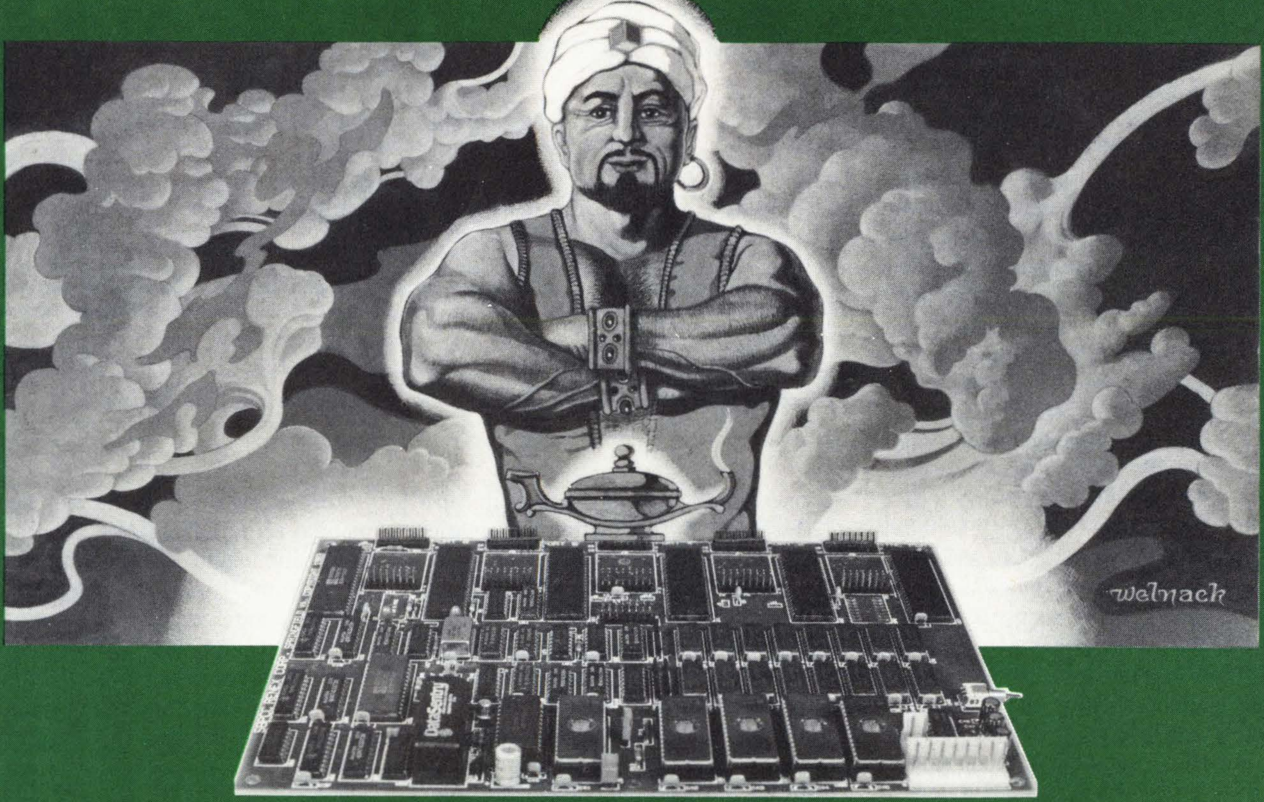

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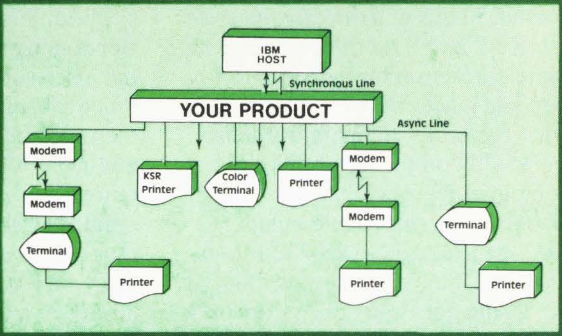

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ASCII analog data and status from DC or slowly varying transducer signals. The SDAS-8 is housed in a steel-cased modular package measuring only 4" × 6" × 0.4" for printed circuit board or standoff mounting. Using standard RS-232-C serial interfacing levels and simple ASCII commands, the SDAS-8 connects to all popular computers including personal computers with a programmable serial port.

The normal application for SDAS-8 is as a remote analog data input to a computer. The user's host computer would take the SDAS-8 data strings under program control and would process this data for arithmetic manipulation (peak detection, averaging, scaling and offset), display formatting (columnizing data with engineering unit labels), and data storage to disk, tape or data retransmission.

SDAS-8 includes two onboard crystal-stabilized clocks, both of which are controlled and displayed with simple user commands. A settable 24-hour (23:59:59) time of day clock may be optionally tagged with each returned data scan transmission. A selectable independent interval timer causes automatic scan transmissions from 1 second to 17:59:59 hours intervals. Direct thermocouple inputs are available using the gain-selected, resistor programmed instrumentation amplifier and a separate cold-junction compensation input channel. Under serial ASCII command, SDAS will directly linearize type J, K, T and S thermocouples with software correction for the local TC-to-copper cold junction EMF error using an external connector temperature sensor. Other ASCII commands produce direct data output in degrees Celsius or Fahrenheit from the thermocouple inputs.

SDAS-8 includes both RS-232-C (non-isolated) and 20mA loop (isolated) serial ports. Using the loop ports, up to 4 SDAS-8 stations (32 Differential channels) may be multi-dropped in series on input and output loops (4 wires).

Individual channels may then be polled under host computer command many hundred of feet away.

Requiring regulated + and ±15V DC power, SDAS-8 readily adapts to existing computers. Remote 2-wire data acquisition to any distance requires the addition of standard RS-232-C auto-dial, auto-answer telephone modems at both ends.

The standard SDAS-8 analog input range is ±4.095VDC full scale at a gain

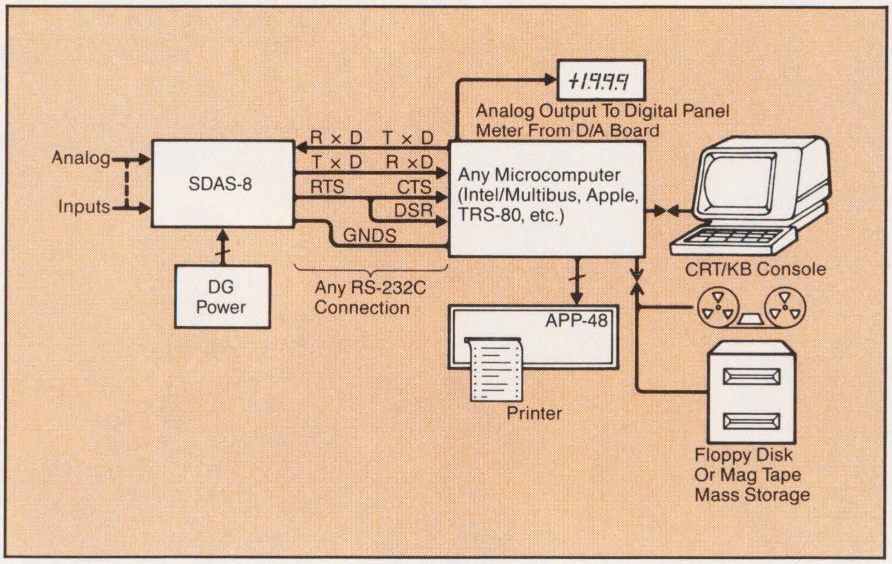


Figure 1: Data Acquisition Computer with Polled Scan Starts or Timer Auto-Scan.

of one. Analog signals are converted to a 12-bit binary representation plus polarity for bipolar signals, yielding a resolution of one part in 8192. For programming convenience, channel data is transmitted either as ASCII decimal or as ASCII hexadecimal under serial command. To simplify program number conversion, bit weighting in hex is 1 millivolt per count at gain = 1. All data is tagged with a hexadecimal checksum which may be compared for data link integrity.

The differential instrumentation amplifier is gain programmable with an external, user-supplied precision resistor for practical gains up to X200. For J and K thermocouples, SDAS-8 is calibrated for a gain of X80. S and T thermocouples require a gain of X160. The gain resistor is omitted for the gain-of-one ±4.095VDC range. The dual-slope, sign/magnitude A/D converter used in SDAS-8 continually overwrites a local random access semiconductor memory (RAM) buffer at 15 samples per second (12.5Hz for 50Hz NMR). Depending on baud rate, protocol overhead and formatting, per channel bandwidth is typically 1Hz.

A/D scan transmissions may be started by the remote host computer in polled mode or after host initialization of the SDAS-8 autostart timer. Scan starts may also occur using a local TTL start trigger input. In this mode, no host computer is needed. SDAS-8 will directly transmit to a serial input printer such as Datel's APP-20 or APP-48 series.

Formatting controls are included for manual set-up, evaluation and calibration. Line length may be command-selected from 20 to 132 characters per line. Editing features include two types of rubout format, similar to micro-computer monitor programs. Line feed characters may be suppressed and filler NUL's may be command-selected for slow printers. Syntax errors which won't execute are echoed with "#".

A status message indicates system state at any time. Half duplex operation may be invoked by supressing the character echo and the string transmission can be throttled for host input buffer management using the XON/XOFF commands. A selectable (20 character) identification message may precede all data to tag the location, date, scale factors, etc. Line formatting prevents skewing or slicing of data for any one channel over two lines.

Careful selection of A/D integration periods offers rejection of 50 or 60Hz input noise.

SDAS-8 input output connections are made through a dual-row right-angle connector whose mating pins may be a PC board or adapted to a flat cable header.

SDAS-8 is also available on the Model ST-705 single-board system which includes an AC power supply, screw-terminal analog input connections and a standard 25-pin RS-232-CDB-25P connector for direct plug-in to the user's terminal or computer.

The ST-705 also includes the local ther-

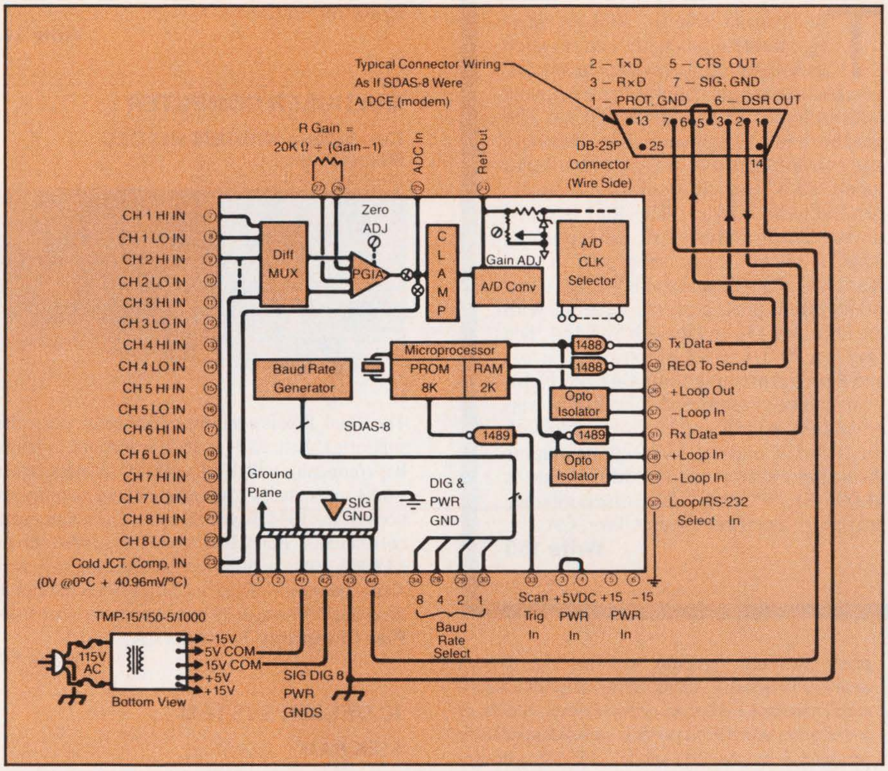


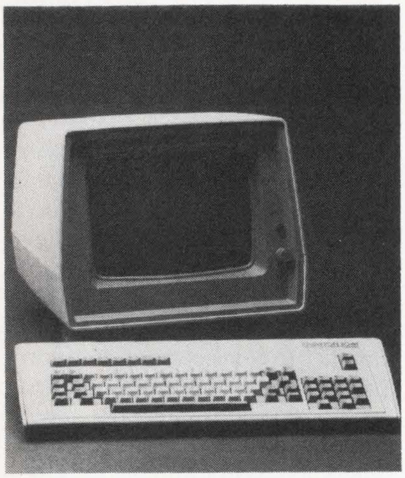
Figure 2: SDAS-8 block diagram.

mocouple cold-junction compensation amplifier and connector temperature sensor. For local triggered scan starts, a TTL one-shot circuit accepts a switch input. Extra PC board pads are included for user-installed input voltage dividers (higher voltage ranges), current shunts (direct 4-20mA measurement, etc.) overvoltage protection clamp zeners or RC hash filters. Barrier screw terminals are installed to connect an AC line cord and pads are included for user-installed gain resistors. The ST-705 is configured on a Multibus format PC board for mounting convenience in Multibus stand-alone card cages or in the user's host Multibus computer. Using a combination of the transformer-isolated AC supply and the opto-isolated 20mA loop serial port, full isolation of the analog inputs is achieved on the ST-705.

Write 231

INTELLIGENT TERMINALS

With Firmware Customization

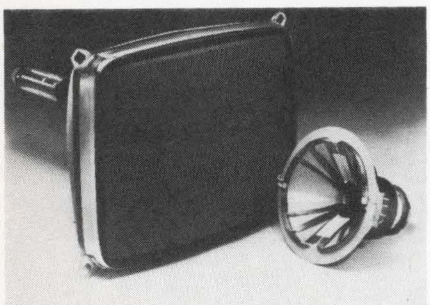


The Ovation 1041 and 1051 are intelligent terminals with features such as soft set-up, firmware customization and expansion capabilities to support custom logic. The Ovation 1051 has 256 graphic and 128 alphanumeric characters and is available in an 80- or 132-column mode. 16 Kbytes of memory can be expanded to 64 Kbytes. The 1051 is based on the Zilog Z80A and incorporates SMC's video logic ship set. It has RS-232C/RS-422 and the RS-232C communications ports and is compatible with the DEC VT-132 and the ANSI X3.64. The Ovation 1041 has 84 graphic characters and 8 programmable function keys. Firmware can be customized. The 1041 is based on Intel 8085A and is compatible with the ADM 31 and the TVI 925. It contains the same memory as the 1051. Price is $1,095-$1,295 and OEM discounts are available. **Zentec**, Santa Clara, CA

Write 150

CRT

Displays 8000 Characters

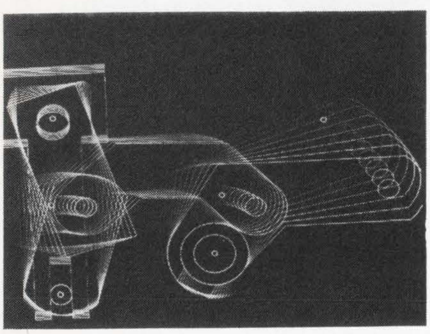


The M38-200 CRT displays 8000 characters and resolves 3.9 million pixels in a scanning area of 7⅞" × 10⅝". The 15" M38-200 has applications in phototypesetting, CAD/CAM graphics, facsimile systems, diagnostic imaging, and word processing. It is available in white and green phosphors. Price is $575. **Amperex**, Slatersville, RI

Write 144

MODELING SYSTEM

For Third Party Analysis Systems

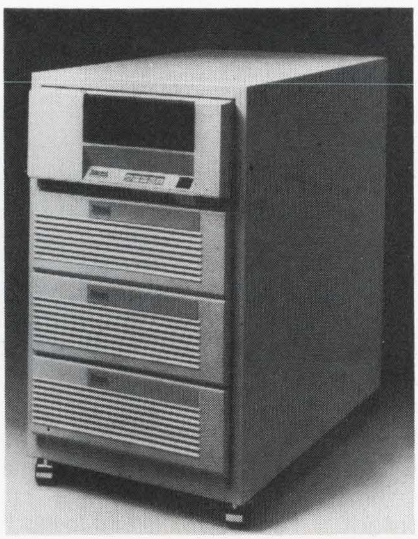


The Mechanism Modeling System is a software package which prepares models for input to third-party kinematic, dynamic, and static equilibrium analysis programs. Using standard graphics software, mechanisms are described as stick models, or wireframe, sculptured surface, or solid models. To produce a mechanism model, MEMS software identifies relationships between parts, types of forces and torques acting on the mechanism. The software will generate graphs, plotting the relationships between displacement, velocity, acceleration, force, and time. **Integraph**, Huntsville, AL

Write 129

SUPERMINICOMPUTER

Unix-Based

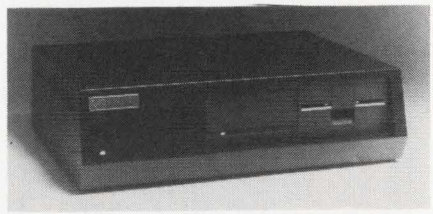


The Eternity Series is a 32-bit super-minicomputer compatible with Western Electric System V and Berkeley 4.1 and 4.2 versions of Unix. The Eternity Series is designed for OLTP and can be programmed in C, COBOL 74 ANSI level II, FORTRAN 77, PL/1, Pascal (ISO), and BASIC languages. The system has fault tolerance and data integrity features, and price is $75,000. **Tolerant Systems**, San Jose, CA

Write 143

MULTIUSER COMPUTER

Compatible With IBM and DEC Mainframes



The Black Box is a multiuser microcomputer that supports enhanced 8- or 16-bit operating systems. It is compatible with IBM and DEC mainframe networks and includes 256K single-board memory options and an IBM Bisync-80 communications protocol emulator. Black Box models use either the Intel 8085, 8086, or 8088 and include floppy or hard disks. Internal storage is 1 Mbyte with the floppy disks and 6 Mbyte or 19 Mbyte with the hard disks. **Rair Computer**, Palo Alto, CA

Write 147

IC DESIGN SYSTEM

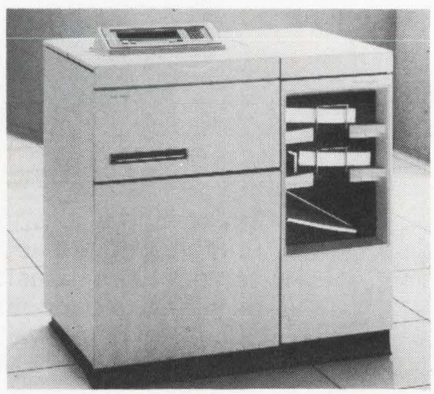
512K RAM

The Clyde is a Motorola 68000-based system for integrated circuit design. Clyde has 512K of RAM and two 5¼" DS/DD floppy drives. It uses a CP/M operating system and has application software for logic design, logic simulation and timing simulation. Macrocell library files and supporting data are included. Price is $10,000. **Cademic**, Scottsdale, AZ

Write 135

LASER PRINTING SYSTEM

57,600 DPI Resolution

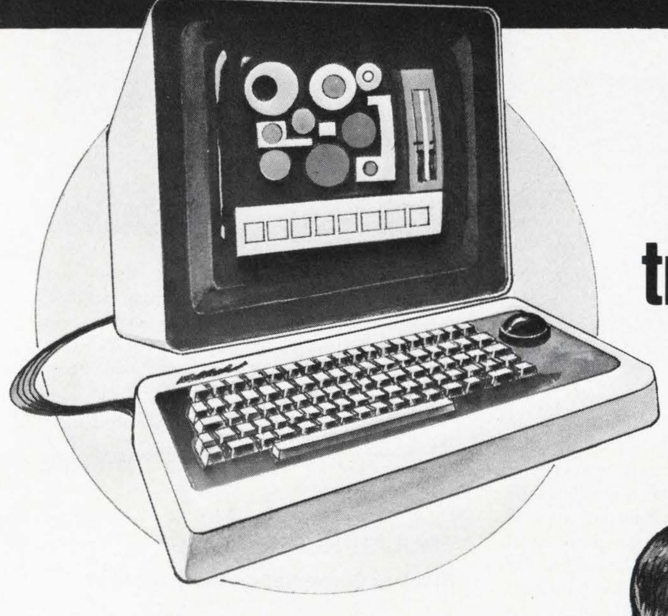


The B9290-30 Intelligent Laser Printing System is compatible with Burroughs mainframe systems. The printer operates in a continuous mode under printer and host system software control and can print on two sides of 8½" by 11" paper in either portrait or landscape, as well as collate and stack completed reports in distribution order. Images are created by a laser diode with a resolution of 57,600 dpi. Price is $65,000. **Burroughs Corp.** Detroit, MI

Write 149

TRACKBALLS

BY Disc



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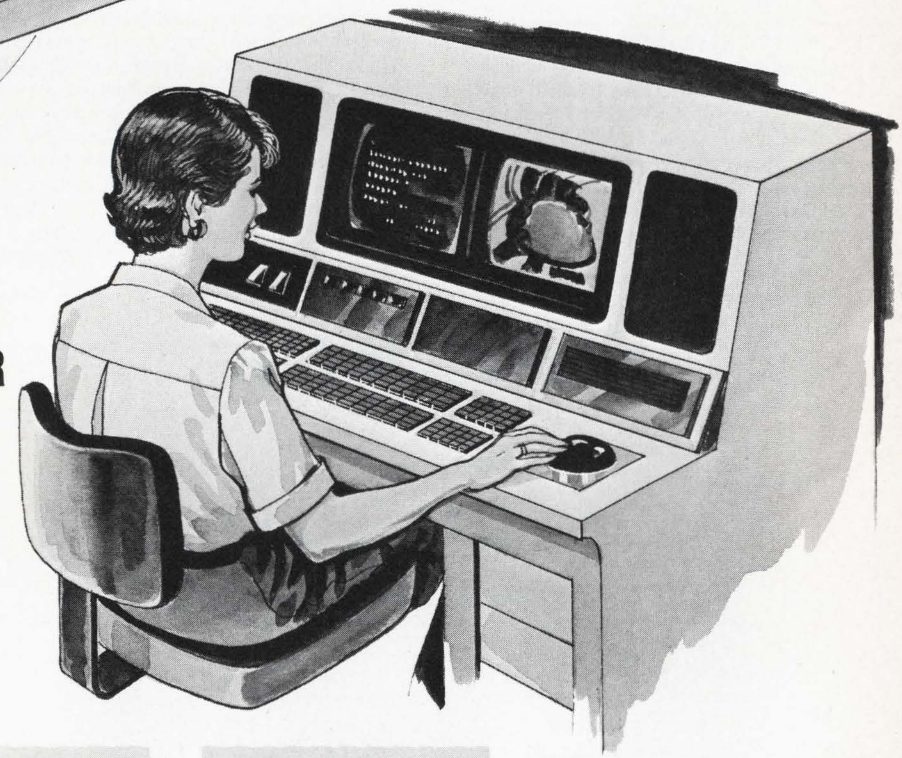

GRAPHIC TERMINALS
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TRAFFIC CONTROL RADAR
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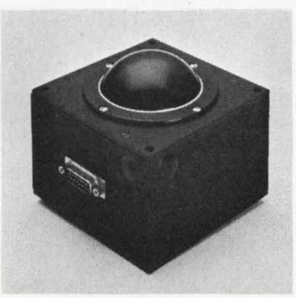

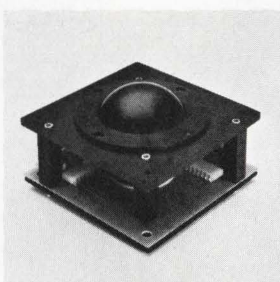

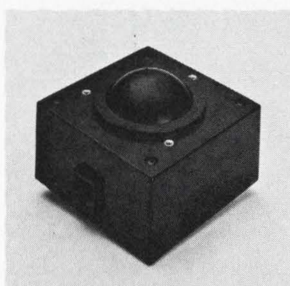

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STANDALONE COMPUTER

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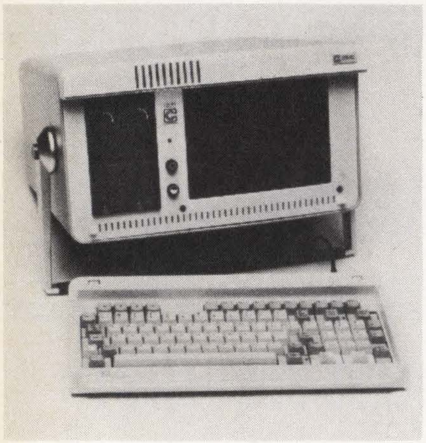


The Colby PC-3 is a standalone IBM-PC compatible transportable computer. The computer has a 9" amber screen, dual 360K double-sided, double-density floppy drives and 3½ IBM-PC expansion slots. The Colby PC-3 has 128K or RAM, a real-time clock, serial port, parallel port, SASI hard disk interface and 80 column × 25 line display with IBM-PC compatible graphics capability. Price is $2,795. **Colby Computer**, Mountain View, CA

Write 139

TOUCH SCREEN MONITOR

For DEC 350 Workstations

The VRTS1 DECtouch monitor is designed for use in a Professional 350 workstation. It responds to input devices such as a joystick, mouse or keyboard. The DECtouch membrane panel is mounted over the CRT display and can sense input position with a resolution of one millimeter. A connector panel contains two serial and parallel connectors for simultaneous attachment of alternate positional input devices. The controller module interfaces the screen to the 350 workstation. Price is $3,295. **Digital Equipment Corp.**, Maynard, MA

Write 141

STAND-ALONE WORKSTATION

768 × 585 Resolution

The GX-100 F5 is a graphics workstation with local processing features. The workstation has dual 5¼" floppy disks and a CP/M operating system and can be run on-line with a mini or mainframe CPU or locally with many graphics packages. The disk controller reads and writes 15 formats. The terminal has 768 × 585 resolution on a 15" screen. **Modgraph**, Waltham, MA

Write 133

EMULATING TERMINALS

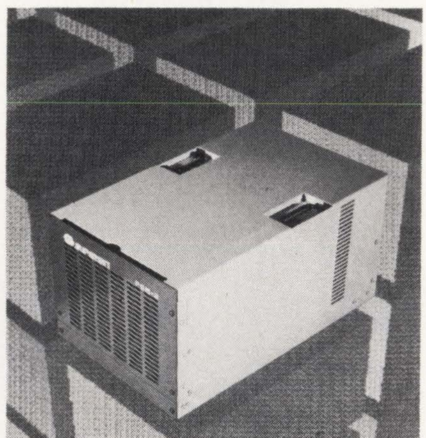
Block or Conversation Mode Storage

The 6531 and 6532 terminals feature detachable keyboards and 8 pages of memory which can be stored in block or conversational mode. All models have a 25 line by 80 column screen format and support eleven languages. The terminals have detachable CRT monitors and are available with tilt/swivel option. Price is $1,950-$2,100. **Tandem**, Cupertino, CA

Write 142

STANDALONE SYSTEM

With 169 Mbyte Disk Drive



The Superset PGM-2 System was designed to execute large scale FORTRAN software packages. The architecture is optimized for multiple I/O operations and has applications as a CAD/CAM processor or finite element analyzer. The basic system includes a 48-bit main processor, 8-bit front-end processor, 400K RAM, 9-track formatter interface and eight RS-232 ports. Up to four disk drives can be attached. **Superset**, San Diego, CA

Write 127

SUPPORT SOFTWARE

For Lasergrafix 1200

This software support package is designed for the Lasergrafix 1200, a laser printer with a programmed graphics laser, letter quality output and a resolution of 90,000 dpi. The non-impact printer can bit-map an 8½" × 14" page and is used for industrial and scientific graphics applications. The support package is named Qtroff and includes utilities for preparing fonts, handling print spooling and for converting CAT typesetter output of troff to appropriate formats for the Lasergrafix 1200. Fonts are loaded to the printer and managed by the software. Qtroff is distributed in C language source form and is configured to be self-installing by using the UNIX make facility. Fonts are available, include Times Roman, Helvetica and Computer Modern look-alikes. The Lasergrafix 1200/Qtroff system has run in UNIX System 3, System 5 and Berkeley Standard Distribution 4.1 implementations. Price is $1,500. **Quality Micro Systems,** Mobile, AL

Write 166

DECnet INTERFACE SOFTWARE

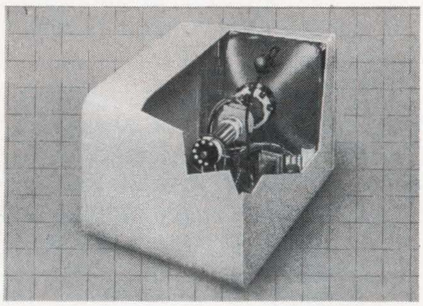
For Unibus Network Controller

EASYWAY/E DECnet Interface is a software package for the easyway/E Unibus network controller. The package consists of an operating system device driver and an application program which is used to configure and initialize the device driver. The controller connects a DEC VAX or PDP computer system to an Ethernet/IEEE 802.3 LAN supporting layers 1 through 4 of the ISO/OSI network architecture. It combines two modules in a hex width board; the host protocol processor contains the UNIBUS interface, data link layer interface and the transport protocol, and the Communications Adapter Board provides the data link and physical layer protocols. Price is $500 for the first VAX, $250 for second and subsequent VAX's. **Able Computer,** Irvine, CA

Write 152

CRT Shielding

Protects Against EMI/RFI Emission



This line of conductively coated cathode ray tubes provide 20 db of shielding against EMI/RFI emission. The conductive coating is sprayed on the back of the tube up to the tension band, but openings are left near the yoke flare and anode button. The proprietary coating is electrically connected to the tension band through a metal foil tape. The cathode tube is available in standard sizes with any Clinton phosphor or anti-glare system. **Clinton**, Rockford, IL

Write 159

COLOR GRAPHICS SYSTEM

1280 × 1024 Resolution

The 9770 Color Graphics Node is suited for three-dimensional applications such as shading and hidden-surface removal. The 9770 is compatible with the CADMUS series of mainframe systems and has 1280 × 1024 pixel resolution on a 60 Hz non-interlaced 19" color monitor. Image memory is expandable from 8 to 24 planes and the system has vector writing speeds of 100 million pixels per second. Price is $37,700. **Cadmus**, Lowell, MA

Write 151

COLOR GRAPHICS TERMINAL

Tektronix Emulation

The GTC314 is a color graphics terminal with bit-mapped display, 4K color palette, polygon fill in color and programmable character sets. Graphic features include a 512 × 480 display and a Tektronix 4010 emulation mode. Three character sets are available, one fixed and two programmable which allow the user to define font and cell size of 256 by 128 pixels. All keys are programmable. **PsiTech**, Irvine, CA

Write 130

COLOR GRAPHICS DISPLAY CONTROLLER

Display 64 Color Combination

The model 4000 color graphics display controller is a plug compatible replacement for the MRD 450 used in Foxboro Fox 3 and Fox 300 Systems. The unit can display 256 simultaneous characters/symbols in 64 color combinations. Price is $2800. **Terminal Display Systems**, Dallas TX

Write 132

2400 BPS MODEMS

Auto-Dial Feature

The Model 2232 is an integral auto-call unit with internal memory storage of phone numbers and alternate number dialing. The dial-up connection can be initiated by the user from a terminal, computer, or telephone keypad. The user can store nine, 40-digit phone numbers in non-volatile memory. Displayed progress messages provide a status of the calling sequence. The Codex 2232 complies with CCITT V.22 bis standard. **Codex**, Mansfield, MA

Write 156

MEASUREMENT AND CONTROL SYSTEM

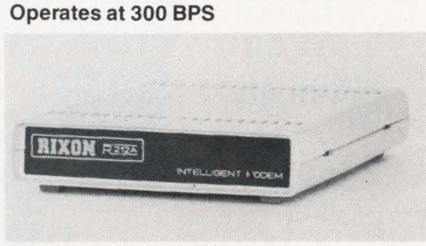
With Touch Screen CRT

The 2452 Measurement and Control System is designed for industrial process control and on-line product testing applications. The 16-bit microprocessor-based instrument has a touch-sensitive CRT display and dot-addressable graphics. The 2452MCS is expandable to sixty channels in the 2400B mainframe and to 1000 channels with extender chassis and I/O options. A distributed data acquisition network can be constructed using a 1722A and up to nine 2400B's in either star or daisy-chain configuration. Price is $15,000. **Fluke**, Everett, WA

Write 140

INTELLIGENT MODEM

Operates at 300 BPS

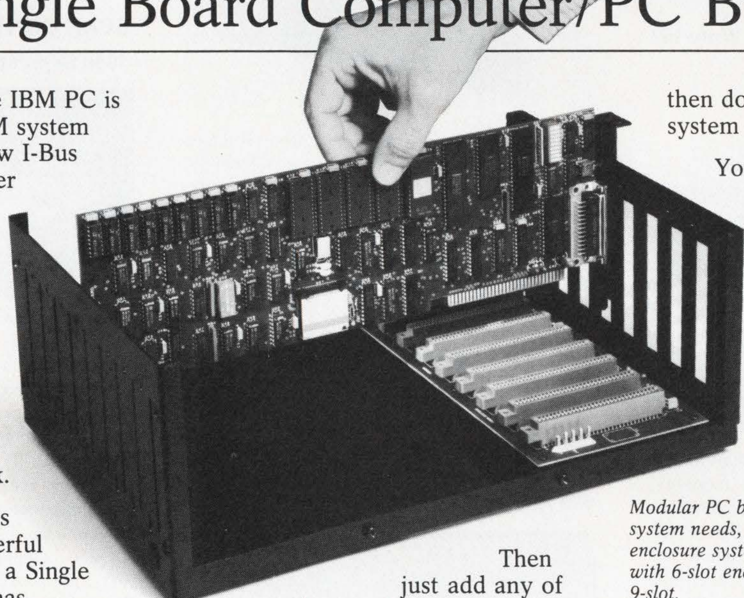


The R212A Intgelligent Modem is an LSI modem that features an integral automatic dialer. It operates full duplex asynchronously at speeds of 300 bps or character asynchronously at 1200 bps over telephone lines. The modem can automatically answer and a standard 500 pulse or tone dial telephone can be used if manual call origination or answering is desired. A six-pin modular cable is furnished with the modem which is compatible with Rixon and Bell 212A, 103, and 113 Series. **Rixon**, Silver Spring, MD

Write 161

Put the Power of the IBM PC Bus into Your OEM System

NEW Single Board Computer/PC Bus System



The power of the IBM PC is now available to OEM system designers with the new I-Bus Single Board Computer and Enclosure systems. Now you can make use of that vast array of PC-compatible expansion cards—for communications, graphics, data acqui sition, peripheral control, and every other imaginable task.

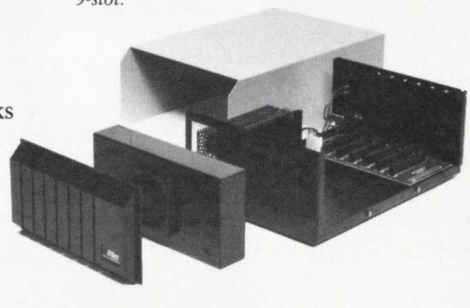
I-Bus Systems has packaged Intel's powerful new 80188 CPU into a Single Board Computer. It has 64K of RAM and up to 160K of ROM on board, plus a serial console port to talk to a terminal or a PC. Just plug the SBC into an I-Bus 6-slot chassis or 9-slot card cage and you have the heart of a computer system, ready to run.

Then just add any of the hundreds of PC bus cards already on the market, to customize your system.

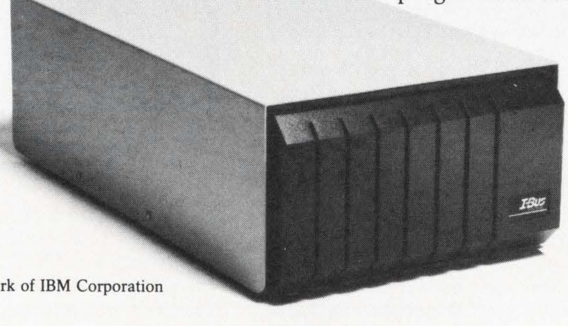
Best of all, the IBM PC works perfectly as a software develop-ment system. You can assemble and test applications programs on the PC, then download them to the I-Bus system for dedicated execution.

You'll have the best of both the PC world and the OEM bus-structured world with this new single board computer from I-Bus.

For all the details, give us a call today at (800) 382-4229. In California, call (619) 569-0646.



Modular PC bus packaging matches your system needs, from basic cage to complete enclosure system. Internal 40W power supply with 6-slot enclosure, external supply for the 9-slot.



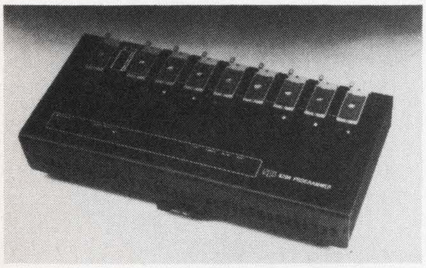
I-BUS SYSTEMS
9235 Chesapeake Drive
San Diego, CA 92123

IBM PC is a trademark of IBM Corporation

Write 79 on Reader Inquiry Card

8-GANG PROGRAMMER

32K Buffer Memory

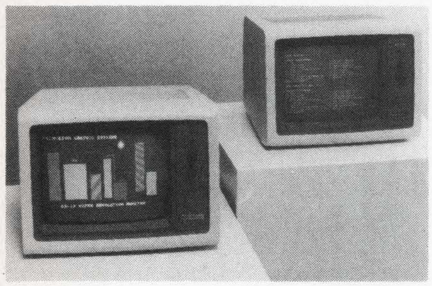


The Model 8204 Programmer is equipped with 32 Kbytes of buffer memory. Features include selectable protocols, block mode data transfer, selectable baud rates, editing and checksum computation. Operating in conjunction with a computer or free standing, Model 8204 programs all EPROMs. These include Intel 2758, 2716, 2732, 2732A, 2764, 27128, Texas Instruments TMS2508, TMS2558, TMS2564, TMS2528, National NMC2724, Motorola MCM 2816, MCM68764, and Hitachi HN48016P. Price is $1,395. **Martel-Spi**, Windham, NH

Write 157

MONITORS

Color and Monochrome



The MAX-12 and the SR-12 from Princeton Graphic Systems are monochrome and color monitors, respectively. The MAX-12 uses an amber phosphor which has the advantage to being shorter in persistence than the standard P39 green phosphor. The SR-12 color monitor features a .31mm dot pitch tube supporting 690 horizontal resolution and 480 vertical resolution. Both monitors are designed for the IBM PC, IBM XT, and the IBM-compatible personal computers. Prices are $249 (Model Max-12) and $799. (Model SR-12). **Princeton Graphic Systems**, Princeton, NJ

Write 158

PRINTER EMULATOR

IBM PC-Compatible

The Passport Printer Emulator is designed to assist the personal computer user by preventing potential time and data loss. It operates in print pass-through and print bypass modes. When selected for print bypass operation, the Passport appears as a standard printer device. During print pass-through operation the Passport will permit print operations. The user can stop an ongoing print operation by reselecting to the bypass mode. The device functions with all IBM PC-compatible personal computers. **Micro Computer Components**, San Diego, CA

Write 185

MICROFLOPPY SOFTWARE

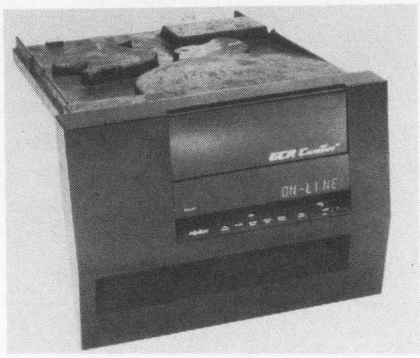
For 3¼" Media

The Dysan Series Software is a package for 3¼" microfloppy computing. The package consists of the software 3¼" Concorde disk drive add-on subsystems, and a dealer support program. The software is Apple and IBM compatible. **Dysan**, Santa Clara, CA

Write 162

TAPE DRIVES

Operates At 6250 BPI

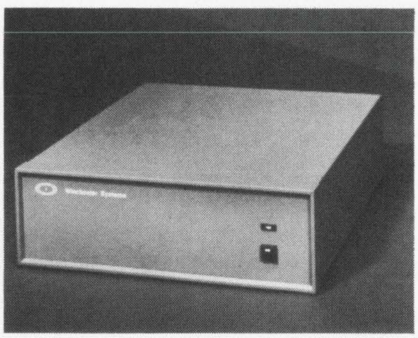


The CacheTape line is a family of 6250 bpi GCR tape drives. Models M990 and M991 use the Cipher ½" tape interface for hardware integration. The M990 has a cache size of 128 Kbytes and a transfer rate of 450 Kbs. The M991 has a 256 Kbyte and a 790-bks maximum transfer rate. Maximum block size is 32 Kbytes for the M990 and 64 Kbytes for the M991. The M990 is priced between $6,000 and $7,000 and the M991 is priced between $7,000 and $8,000, in OEM quantities. **Cipher Data Products**, San Diego, CA

Write 163

WINCHESTER DISK SYSTEM

625 Kbytes/Sec Transfer Rate

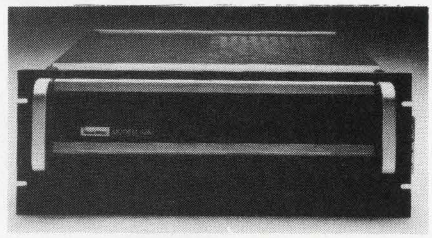


The DataSafe 24 is a 15 Mbyte 5¼" fixed Winchester disk system for Intel Intellec Series II, III and MDS-800 microprocessor development systems. The DataSafe-24 has 24 Mbytes unformatted (15 Mbytes, formatted) storage totaling 115,200 available blocks allocated in four directories: F0, F1, F2 and F3. The four directories, each with 28,800 blocks, permit four engineers to share the storage and keep separate files. The system has a data transfer rate of 625 Kbytes/sec and an average access time of 85 msec. Price is $7995. **Winchester Systems**, Winchester, MA

Write 164

112 KILOBIT MODEM

For Wide Band Carrier Systems

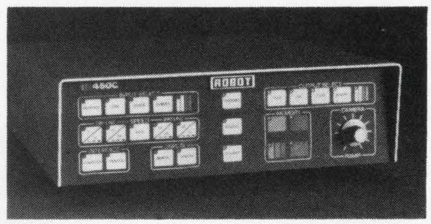


The Modem 112K is a 112,000 bit per second modem designed for wide band carrier systems such as microwave and/or satellite networks. The modem operates full-duplex and features manual down speed switching for compatibility with the Racal-Milgo Modem 56K, and for transmission over degraded communication lines. The modem incorporates Analog Loopback, DTE Loopback, and Data Test diagnostics. The 112K has a CCITT V.35 compatible interface. Price is $16,500. **Racal-Milgo**, Miami, FL

Write 167

SCAN CONVERTER

4096 Separate Color Hues

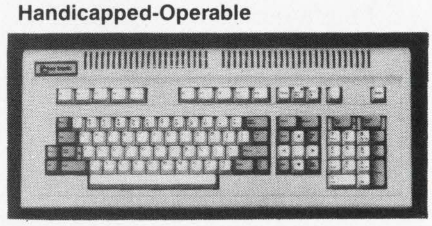


The Model 450C color image processing scan converter provides the interface between a video camera, monitor and computer. Video can be grabbed into one of three memories for black and white images or into all three simultaneously for a single color image. 4096 separate color hues can be displayed in the color mode. Each pixel can be randomly accessed for image enhancement, graphics generation, storage and recall. An internal slow scan video modem allows the transmission of video images over voice grade communications links in 8 seconds. Price is $895. **Robot Research**, San Diego, CA

Write 168

KEYBOARD

Handicapped-Operable



Handicapped-operable replacement keyboards are available for the IBM PC and Apple II personal computers. Individuals without the use of two hands can operate the IBM PC or Apple II with the corresponding Key Tronic keyboard, because of alternate action switches on "shift", "control", and "Alt" keys. The key switch design eliminates the obstacle of having to depress both one of these keys and another key simultaneously. **Keytronic**, Spokane, WA

Write 177

IMPACT PRINTER

Operates At Three Speeds

The IBM 4248 is an impact line printer which operates at 3,600, 3,000 and 2,200 lines per minute. At its lowest speed, it can print optical recognition characters. Through program control, an operator can change speeds, select 6 or 8 vertical line spaces per inch or adjust hammer flight timing. It has self diagnostic functions and can be programmed to show operational, diagnostic and test messages, such as print band identification, in any of eight languages on a 12-character alphanumeric display. The BM 4248 attaches via a byte multiplexer, selector, or block multiplexer channel to system 370, 43XX, 303X, and 308X processors. Price is $99,000 and volume discounts are available. **IBM**, Rye Brook, NY

Write 183

EPROM STATIC RAM TESTER

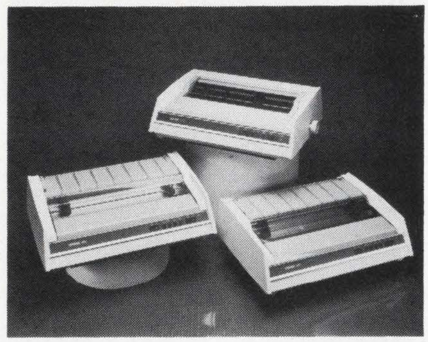
For JEDEC and Static RAM Devices

The Mate M256 memory tester evaluates, tests and measures the access time of EPROM, E^2PROM, and static RAM integrated circuits. The MATE M256 can be used to test bit performance of JEDEC-compatible EPROM and E^2PROM devices of 16, 32, 64, 128, and 256 Kbits of memory, and static RAM devices of 16, 32, and 64 Kbits of memory. Four LEDs indicate pass, fail, device type error, and power on and an RS-232C port is included on the unit to allow memory uploading and downloading from the host CPU. Price is $2,995. **MicroTek Lab**, Gardena, CA

Write 171

DOT MATRIX SERIAL PRINTER

Prints at 200 DPS

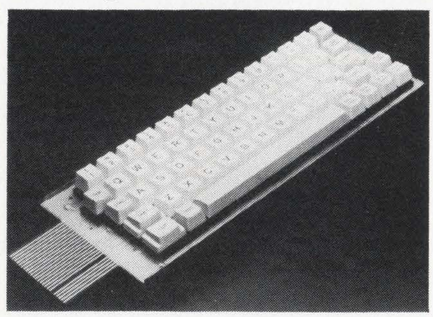


The Printek 930 is a multimode dot matrix serial printer which also serves as a workstation. For word processing applications, the 930 operates in two speeds; 200 cps and 80 cps. For data processing applications, the 930 operates at 200 cps. For graphics, the 930 produces dot addressable charts and graphs in two modes at 4,608 dps. Features include logic-seeking, bi-directional printing, and seven foreign language character sets. Price is $1,995. **Printek**, Benton Harbor, MI

Write 175

MEMBRANE KEYBOARD

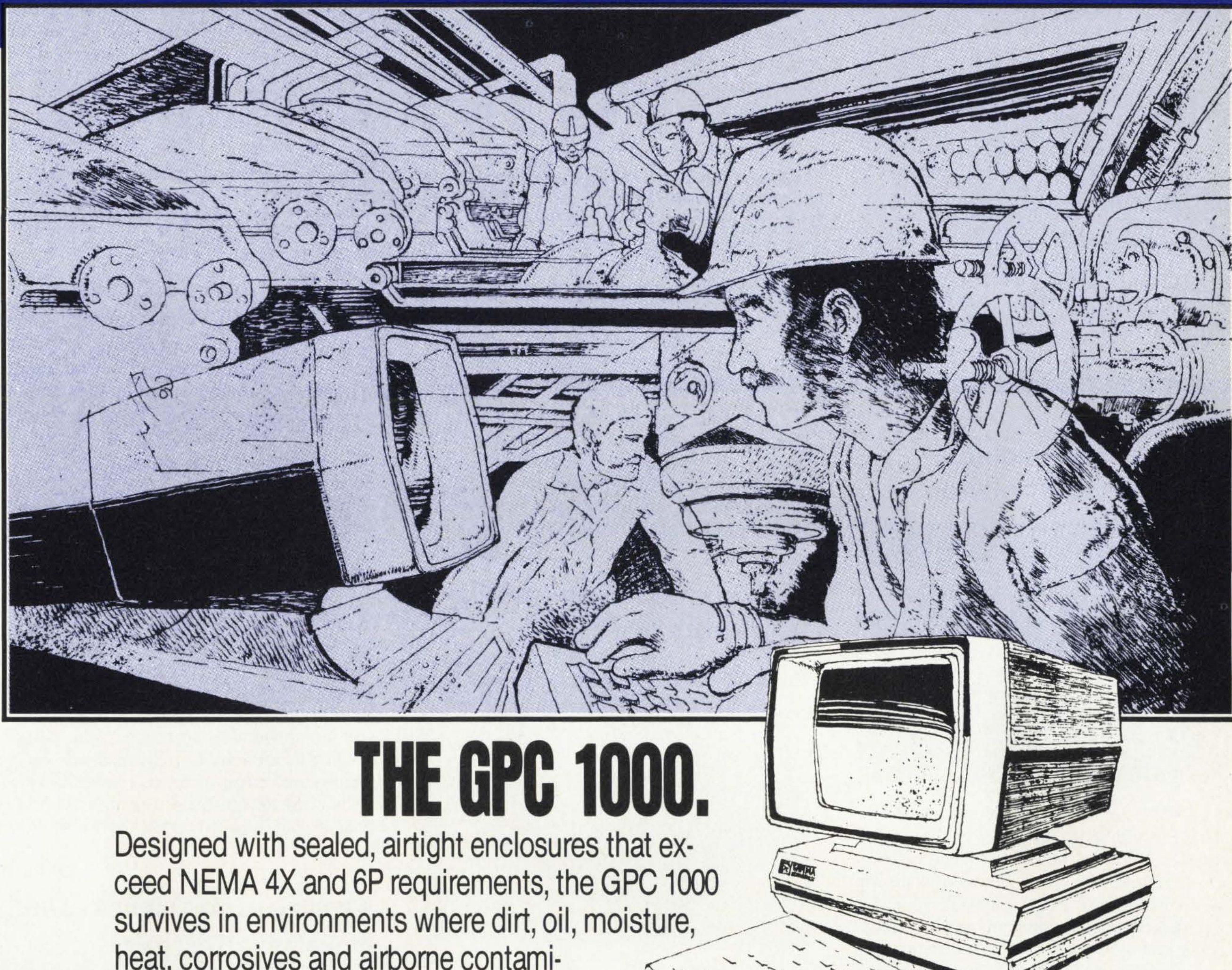
Shields Against RFI and EMI



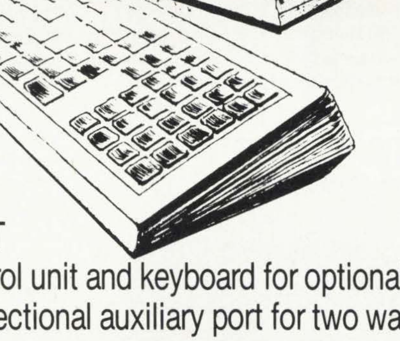
The KS-500E membrane keyboard is portable and rated at 20 million cycles. A metal back-plate provides shielding against RFI and EMI. Keys have a .140" nominal stroke, with a home-row height of 18.3mm. The KS-500E is available with a selection of two-shot keycaps, colors and finishes and in either low or ultra-low profile. The keyboard can also be customized. **Stackpole**, Farmville, VA

Write 170

THE SEVERE ENVIRONMENT VIDEO TERMINAL:



THE GPC 1000.



Designed with sealed, airtight enclosures that exceed NEMA 4X and 6P requirements, the GPC 1000 survives in environments where dirt, oil, moisture, heat, corrosives and airborne contaminants are the enemy. Its durable rugged design incorporates advanced technical specifications with smart ergonomics. DEC* compatible, the GPC 1000 outleagues all other video terminals in its ability to perform in severe environments with features like a sealed 14″ diagonal CRT with protective anti-glare filter; separate monitor, control unit and keyboard for optional bench top, wall, shelf or ceiling positioning; true bi-directional auxiliary port for two way communications—and much more—all backed with our one year warranty.

The Severe Environment Video Terminal Engineered To Work Where You Work.

GPC

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Shreveport, LA 71129 USA
(318) 686-1600 Telex 750469

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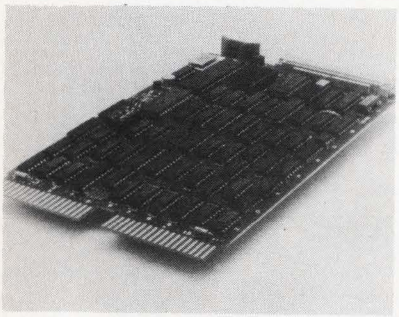
For more information concerning Gamma Products, contact Sharon Russell, Marketing Communications.

*reg. TM-Digital Equipment Corporation emulates VT100 with AVO

FLOPPY DISK CONTROLLER

Interfaces SA801/805 Drives To DEC Q-Bus Computers

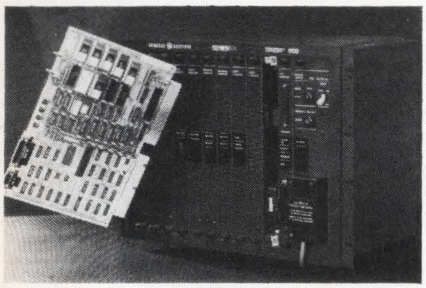


The model DQ419 is a 8" floppy disk controller, which emulates and has operating system compatibility for two SA801/850 drives to interface with LSI-II, 11/23 PLUS and MICRO PDP-11 computers. The DQ419 includes control and interface electronics for RX01/RX02 media compatibility and support of DEC RT-11, RSX-11 and RSTS operating systems, without software patches or modifications. Features include 18/22 bit addressing for 4 Mbytes of memory, on-board diagnostics, data buffer, media present monitor, 4 level interrupt jumper selectable, on-board bootstrap loader, and write precompensation. **Dilog**, Garden Grove, CA

Write 212

COMMUNICATIONS MODULE

For GE Programmable Controller

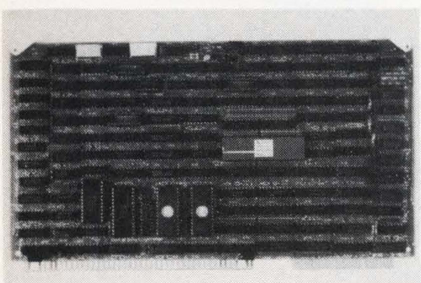


The CCM3 is a communications module for the General Electric Series Six line of programmable controllers. The CCM3 allows interfacing to Fisher Controls' PRoVOX instrumentation systems via Fisher's type DH6005 PCIU. Eight GE Series Six PCs can be connected to a programmable controller interface unit. A total of 64 registers of data can be communicated to the Fisher PCIU from the Series Six programmable controller. The Fisher system also can change values in the Series Six PCs. Price is $1,500. **General Electric**, Charlottesville, VA

Write 192

MULTIBUS PROCESSORS

Support Virtual Memory OS

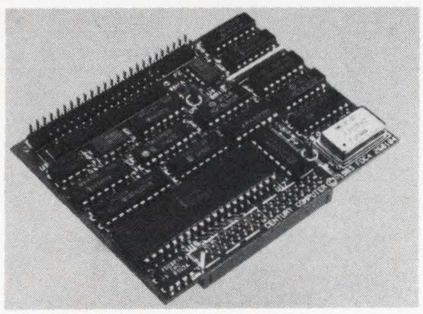


The 68010 and Z8003 are two processors for the Multibus and iLBX. Both boards feature an iLBX interface for the Multibus, providing a memory path for the boards, and support a virtual memory operating system. The 68010 is used as the processor for one board, while the Z8003 segmented virtual memory processor is used for the other. The Z8003 requires off-chip support circuitry, which is provided by the board. UNIX Version V is available for the 68000 board, and XENIX is available for the Z8000 board. **Central Data**, Champaign, IL

Write 194

MULTIBUS FLOPPY CONTROLLER

For 5¼" And 8" Drives



The model V8004 disk controller supports 5¼" and 8" disk drives. It is a single-wide iSBX module compatible with iSBX specifications which provides on-card data separation and double density write data precompensation. Clocks are provided under software control, and the motor on signal is set via software, allowing it to be independent of drive select, if necessary. Price is $450. **Century Computer**, Dallas, TX

Write 202

128K STATIC ROM

Replaces 128K EPROM

The MK23128 is a 128K static ROM that allows compatibility between EPROM, RAM and ROM devices with different densities, up to and including the Mostek MK38000 32K × 8 256K ROM. Suited for use with 8-bit microprocessors, the MK23128 ROM serves as a replacement for any 128K EPROM. The MK23128 is available with 200ns and 250ns access and cycle times. In 5,000-piece quantities, price is $7.65. **Mostek**, Carrollton, TX

Write 205

CONVERTER

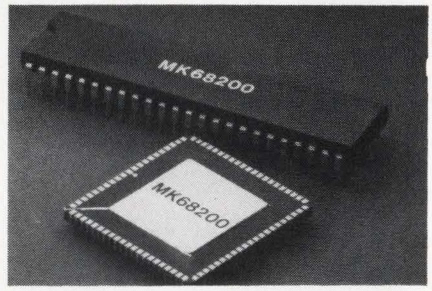
With Dual Rank I/O

The MIL-STD-1553 Manchester II Converter includes all functions for an interface between a MIL-STD-1553 serial MUX bus transciever and an 8- or 16-bit parallel tri-state highway. Features include an encoder/decoder, dual rank I/O registers, valid word, valid address, fault flags and wraparound built-in test. The devices operate over a temperature range of −55°C to +125°C and requires a power source of 5V ±10%. Priced at $450. **ILC Data Device**, Bohemia, NY

Write 199

16-BIT SINGLE-CHIP MICROCOMPUTER

For Robotics and Instrumentation

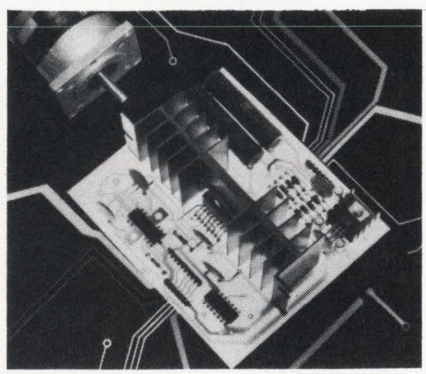


The MK68200 is a single chip microcomputer that can be configured as a stand-alone controller in a single-chip mode or as an intelligent peripheral controller in an expanded bus mode. The chip implements an architecture with a 16-bit instruction set which includes bit-manipulation, BCD arithmetic and multiply/divide operations. The device is designed for applications such as industrial controls, robotics and instrumentation. The MK68200 provides a USART capable of data rates of 1.5 Mbps. Price in quantities of 1,000 is $25. **Mostek**, Carrollton, TX

Write 195

STEPPER MOTOR DRIVER CARDS

For Testing and Prototyping



Models LR-BP-20-35 and PW-BP-50-45 are driver cards for prototyping and testing equipment designed with stepper motors. Model LR-BP-20-35 is a bipolar driver card used for basic drive applications. The card uses a 35V input and has a 2 A/phase output. Model PW-BP-50-45 uses a 45V power supply and has an output of 5 A/phase. Both stepper motor driver cards are TTL compatible and have full- and half-step capability. Inputs for direction, clock, inhibit, and reset are provided. **Clifton Precision**, Murphy, NC

Write 197

SOFTWARE

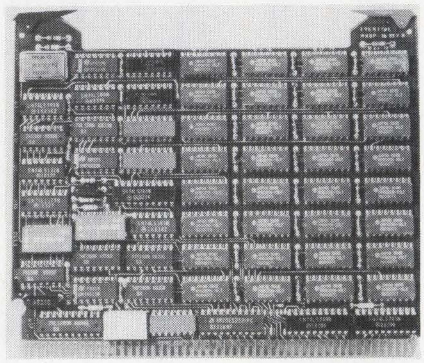
Converts PALs To CMOS Gate Arrays

ANGOP is a software package which converts PAL/HAL designs to CMOS gate arrays. ANGOP accepts as input the logic equations defining a PAL/HAL design, and produces as output a gate array netlist. This netlist is then processed on Matra Design System's GateMark workstation, which contains a library of structured cells, and uses 3μm CMOS technology. The ANGOP package is available for use on the GateMark CAE workstation and the MDS cell library software can be run on a VAX minicomputer. **Matra Design Systems**, Santa Clara, CA

Write 201

MEGABYTE MEMORY BOARD

For HP 9816, 9826 And 9836

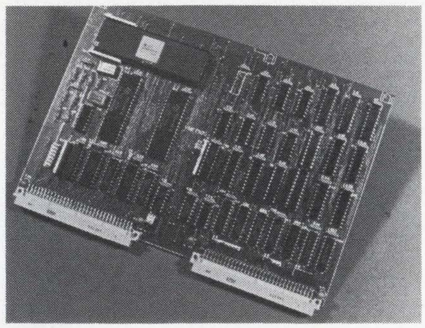


The WKBP-16 is a megabyte memory board for HP Series 200 desktop computers. 16H uses 256K RAM chips increasing the density of previously available boards. The WKBP-16 memory board provides a Mbyte of memory to the HP9816 with no expansion interface and no increase in power consumption. **Eventide**, Little Ferry, NJ

Write 193

DUAL GPIB CONTROLLER

VME Bus Compatible



The VME 7500 is a dual channel controller designed to be compatible with the published VME bus specification. The board implements the talker, listener, and controller functions for the GPIB and contains two independent channels with a separate DMA channel for each GPIB channel. A comparator is included to terminate DMA tranfers on a character match, which is controlled by software. The board can also perform memory to memory DMA transfers without affecting the GPIB functions. Price is $1200. **Mizar**, St. Paul, MN

Write 208

EPROM PROGRAMMER MODULE

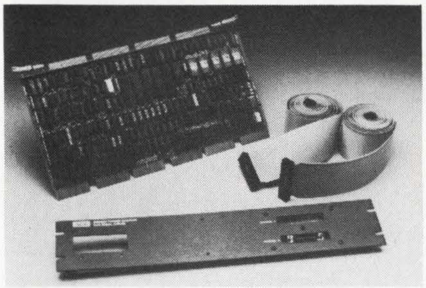
Accommodates Eight EPROMs

The MP-4598 EPROM programmer module is designed to load object code into non-volatile memory. The MP-4598 is software driven and accommodates eight 2716, 2732, 2732A, 2764 EPROM devices while accepting a Multibus chassis slot. The board is I/O mapped and the base address is set by a 4-bit dip switch. The program voltage is hardware selectable between 21.5v for 2732As and 2764s, and 25v for 2716s and 2732s. **Symbicon**, Amherst, NH

Write 211

COMMUNICATIONS PROCESSOR

Supports 131 Bytes Per Frame



The IF-11/HDLC is a single board communications processor which supports user-selectable frame sizes of 131 bytes per frame. The system includes a processor board, distribution panel, cabling, and device drivers for RSX, VMS, and IAS operating systems. The IF-11/HDLC interface allows DEC users to communicate with both DEC and non-DEC hosts. The IF-11/HDLC supports line speeds of 500 kbps, and data throughput rates of 400 kbps. Price is $7,500. **Advanced Computer Communications**, Santa Barbara, CA

Write 191

MULTIBUS TAPE CONTROLLER

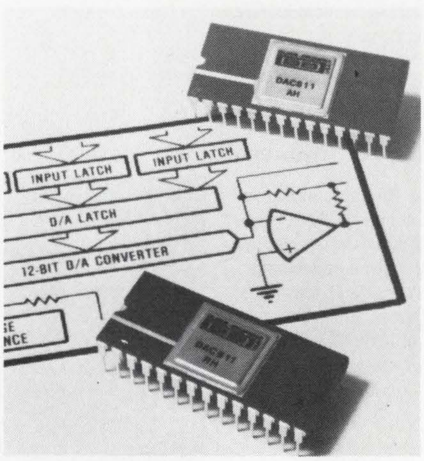
Supports GCR

The 472 GCR is a streaming tape controller which supports Group Coded Recording. Tape storage capacity is 180 Mbyte and the drives operate at 125 ips. The controller is suited to back up larger disk drives, such as the Fujitsu Eagle and CDC 515MB FSD devices. Price in quantities of 100, is $1,300. **Xylogics**, Burlington, MA

Write 207

12-BIT DAC

Available In Two Grades

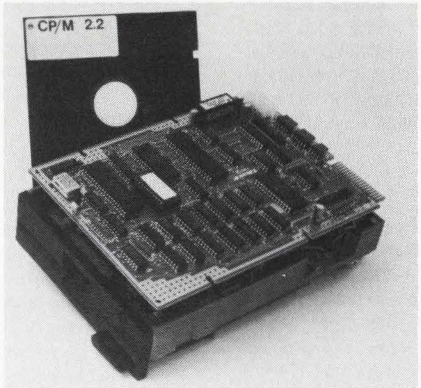


The DAC811 is a microprocessor-compatible 12-bit DAC. The 125 × 131 mil chip contains interface logic, double-buffered latches, DAC, voltage reference, resistors, and an output amplifier. The DAC811 is specified at both ±12 V and ±15V power supply voltages and is monotonic over the temperature range of −25°C to +85°C. Two performance grades are available: the AH grade offers ±1/2LBS max linearity error, and BH model is specified at ±1/4LBS max. Price is $14.95-$22.95. **Burr-Brown**, Tucson, AZ

Write 200

BUS INTERFACE

Parallel I/O To SASI

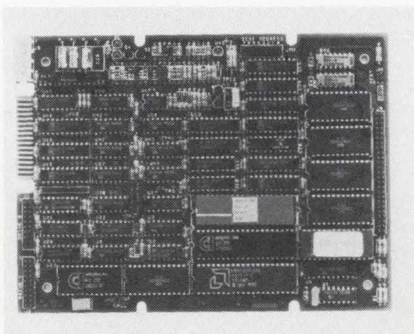


The SASI-100 board converts the 8255A parallel port on the MCPU-800 or MCPU-900 board to a SASI Bus compatible format. The SASI Bus gives the user access to hard disk, cartridge disk, and streaming tape controller boards manufactured by Xebec, Shugart, DTC, and Western Digital. The SASI-100 connects to the microcomputer parallel I/O with CBL-26 and to the desired controller board with CBL-50S. Power is transferred to the SASI-100 thru CBL-26. **Miller Technology**, Los Gatos, CA

Write 209

WINCHESTER DISK CONTROLLER

SCSI Compatible

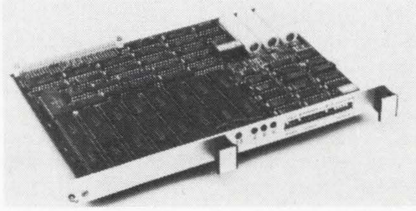


The SABER-AP controller connects to the host micro or mini computer via a (SCSI) bus. The SABER-AP is configured on a 5¼" form factor card and supports two ST506 Winchester disk drives. Standard features include SCSI bus parity and bus error recovery messages. Data protection on and off the disk media is provided by a 32-bit ECC polynomial. The ECC provides correction of errors on up to 8-bit single bursts of data. Price in quantities over 500 is $408. **Adaptive Data**, Pomona, CA

Write 210

VMEBUS MEMORY BOARD

Provides 128 Kbytes

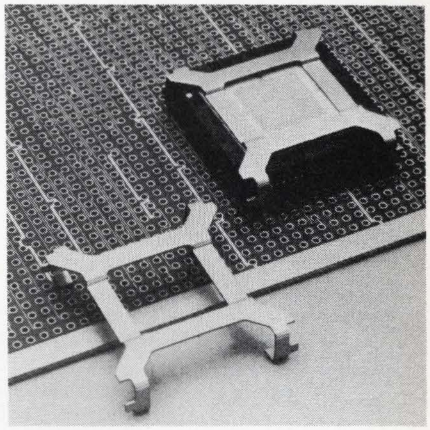


The MM-6500C provides 128K, 64K, or 32K bytes of memory and is compatible with 16-bit VMEbus microcomputers. It employs 8K × 8 or 2K × 8 CMOS static RAMS, which the user may mix with 2764 or 2716 EPROMs, respectively. Other features include 24-bit addressing of 16 Mbytes, module selection on 1000 boundaries using upper and lower address switches, and cycle and access time of 220 nsec. Price is $1175. **Micro Memory**, Chatsworth, CA

Write 190

CHIP CARRIER SOCKET

For Protection Of VLSI

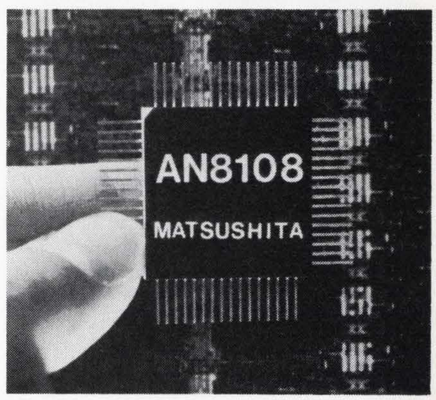


The chip carrier socket for JEDEC Type A leadless chip carriers has a low profile, one-piece spring cover. The stainless-steel cover assembly snaps onto the socket and accepts substrate mounted heat sinks. Sockets are available for thru-board or surface mount configurations. Thru-board footprint is .100" × .100" grid and contacts are located on .050" centerlines. Contacts are beryllium copper with tin or gold plating. The socket insulator is molded Ryton. **Methode Electronics**, Rolling Meadows, IL

Write 188

A/D CONVERTER

Image Processing Applications



The AN8018 8-bit image processing A/D converter, has a speed of 120 mega sample/second, with an input signal range of 40 MHz, making it suitable for high definition picture processing. The converter's three-stage comparator circuit decreases clock signal-talking into an analog signal at a ratio of 1:25. For video pictures, the S/N ratio of 40db is 30MHz input signal area. **Matsushita**, New York, NY

Write 203

BASYS Brochure. This 8-page color brochure from ADAC Corp. describes the BASYS family of real-time measurement and control systems. Included are DiskBASYS, a winchester or floppy disk support system; PromBASYS, a data acquisition and control system with all-solid-state storage media; and MicroBASYS, a remote data acquisition and control system for distributed applications. A proprietary I/OBASIC language, which all use, is described.
ADAC **Write 250**

Fiber-Optics Interface Brochure. This four-page brochure from Kaptron provides information on its line of fiber-optics interface devices. Specifications are included on wavelength division multiplexer/demultiplexer, fiber-optics splitter/directional couplers, fiber-optics switches, and coupler/monitor/bidirectional coupler. The brochure contains diagrams, photographs, and application notes.
Kaptron **Write 257**

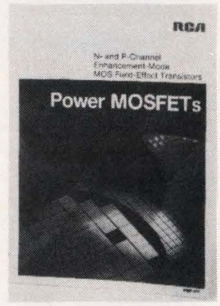
CAD Brochure. Summagraphics Corporation discusses its ICON 2000 Series CAD systems based on Data General's Desk Top Generation computers, for applications in the architectural, engineering and construction and printed circuit board markets. The literature provides a system overview, details software functions and hardware components and provides operating specifications.
Summagraphics **Write 253**

Direct Order Catalog. This catalog from Codex Corp. enables data communications users to order items, which they typically install themselves, without going through their sales representatives. The catalog features cable multiplexers, statistical multiplexers, limited distance modems, high speed modems, cable and Bell-compatible modems.
Codex **Write 265**

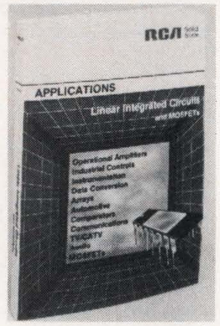
Touch Screen CRT Bulletin. This two-page illustrated bulletin from Reliance Electric describes how the Touch Screen CRT, when included as the total operator interface of an AutoMate Control System, complements the entire system by providing custom displays. The screen replaces the need for keyboard, pushbuttons, pilot lights and meters and can use graphics to display a list of figures or detailed instructions.
Reliance Electric **Write 267**

Converter Data Sheet. This 4-page data sheet from Natel Engineering Co. describes a 22-bit binary-to-BCD converter, designed to interface with high accuracy optical encoders, 2-speed synchro systems and high accuracy synchro instruments. The converter accepts the binary digital representation of an angle and provides a scaled BCD equivalent angle. Included are features, applications, description, specifications, pin designations, I/O interfacing and ordering information.
Natel **Write 255**

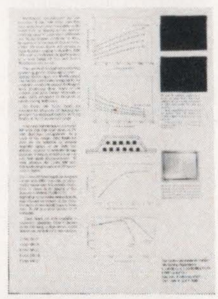
Encoder/Decoder Data Sheet. This 12-page data sheet from Standard Telecommunications describes its STI-5268 Convolution Encoder/Viterbi Decoder designed for digital communication links to aid in overcoming the effects of noise. Included are pin descriptions, electrical characteristics, timing diagrams and parameters, RAM specifications and application information.
Stamford **Write 256**



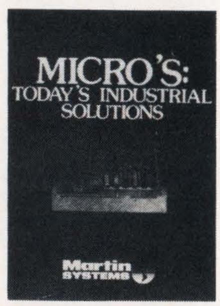
Power MOSFETs Catalog. This catalog from RCA Solid State provides ratings and characteristics data on currently available n- and p-channel enhancement-mode field-effect transistors with drain current (I_D) ratings of 1 to 45 amps and drain-to-source voltage (V_{DS}) ratings up to 500 volts. A cross reference to other industry types is also provided.
RCA



Linear IC Databook. This Databook, "Linear Integrated Circuits and MOSFETs–Applications," from RCA Solid State contains a selection of application notes. Products covered include operational amplifiers, power-control circuits, arrays, differential amplifiers, circuits for television, AM and FM radios and audio systems, data-conversion and special-function circuits, and MOSFETs. Also included is a classification chart.
RCA



Thin-film Heads Data Sheet. This 2-page data sheet from Cybernex Corp. describes its Cyber 100 Series of thin-film recording heads, developed for sub 5″ through 8″ Winchester disk drives and designed for operation on either thin-film or oxide-coated media. The data sheet includes five drawings that explain flying vs. velocity, stiffness vs. velocity, overwrite vs. write current and normalized amplitude vs. flux changes per inch. In addition, color photographs illustrate readback signals and electroplating technology.
Cybernex **Write 260**



Capabilities Brochure. This brochure from Martin Systems describes its approach to the design and development of microprocessing systems for complex manufacturing controls and monitoring processes. Services include R&D, feasibility studies, prototype development, and production of micro products and equipment, as well as the custom design of software packages.
Martin Systems **Write 259**

Dot Matrix Printer Data Sheets. These data sheets from Digital Matrix Corp. describe its Durawriter and Formwriter series of 80 and 132 column dot matrix printers. The Durawriter literature discusses bidirectional NLQ, slew rates to 5″ per second, and speeds to 180 cps in the draft mode. The Formwriter literature reviews the products' state-of-the-art in high speed printing of up to 6 part, continuous forms, without having to manually realign or waste the next form to be printed.
Digital Matrix Corp. **Write 261**

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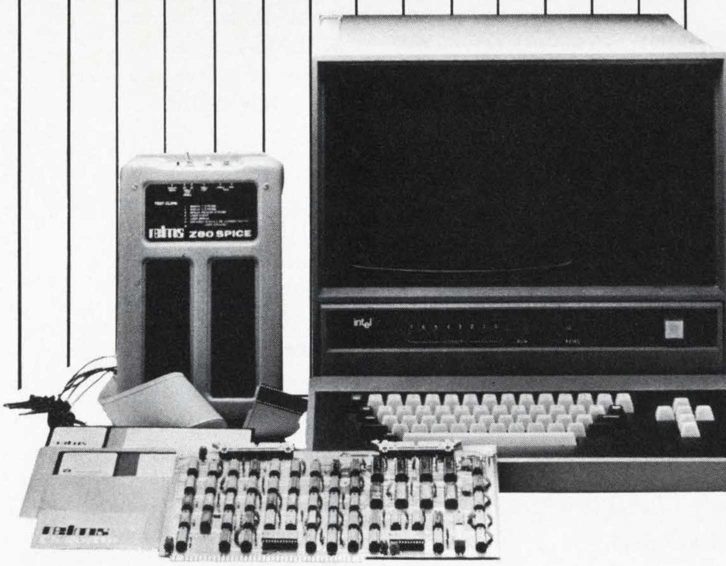
EMULATORS	●									●		●		●
ASSEMBLERS	●	●	●	●	●	●	●	●	●	●	●	●	●	●



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CALENDAR

June 4-7

Eleventh Annual International Symposium on Computer Architecture. Ann Arbor, MI. Contact: Keki B. Irani, Dept. of ECE, University of Michigan, Ann Arbor, MI 48109. (313) 764-8517.

June 5-7

Sixth IEEE Symposium on Mass Storage Systems. Vail, CO. Contact: Bernard T. O'Lear, NCAR, PO Box 3000, Boulder, CO 80307. (303) 494-5151.

June 6-8

ACM Sigcomm 84 Symposium on Communications Architectures and Protocols. Montréal, Canada. Contact: Gregor Bochmann, Dept. d'IRO, Université de Montréal, C.P. 6128, Succ. A. Montréal, PQ H3C 3J7, Canada.

June 14-17

The Byte Computer Shows. Los Angeles, CA. Contact: The Interface Group, Inc., 300 First Avenue, Needham, MA 02194. (617) 449-6600.

June 17-19

Computerized Slidemaking. Andover, MA. Contact: Richard Murray, Director of Conferences, Institute for Graphic Communication, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

June 19-22

Sixth International Conference on Analysis and Optimization of Systems. Nice, France. Contact: INRIA, Domaine de Voluceau, Rocquencourt 78153, Le Chesnay Cedex, France.

June 19-22

CLEO '84. Conference on Lasers and Electro-Optics. Anaheim, CA. Contact: Optical Society of America, 1816 Jefferson Place N.W., Washington, D.C. 20036.

June 19-22

State-of-the-Art Robot Systems Course. Washington, D.C. Contact: Nora Swerdloff, Integrated Computer Systems, 6305 Arizona Place, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

June 20-22

First International Conference on Computers and Applications. Beijing (Peking), China. Contact: Tse-yun Feng, 1604 Stormy Court, Xenia, OH 45385. (614) 422-1408.

June 20-22

FTCS-14, 14th Annual International Symposium on Fault Tolerant Computing. Orlando, FL. Contact: Richard M. Sedmak, Sperry Corp., MS C1SW12, PO Box 500, Blue Bell, PA 19424. (215) 542-3638.

June 24-27

ACM/IEEE Design Automation Conference. Albuquerque, NM. Contact: Design Automation, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

June 26-28

PCExpo. New York Coliseum. Contact: Jim O'Rourke, 333 Sylvan Ave., Englewood Cliffs, NJ 07632. (201) 569-8542.

June 26-29

Computer Graphics Course. Los Angeles, CA. Contact: Nora Swerdloff, Integrated Computer Systems, 6305 Arizona Place, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

June 26-29

MEDCOMP '84. New Orleans, LA. Contact: MEDCOMP '84, IEEE Computer Society, 1109 Spring St., Ste. 300, Silver Spring, MD 20910. (301) 589-8142.

June 26-29

Designing Effective Man/Machine Interfaces Course. Anaheim, CA. Contact: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Pl., PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

July 9-12

1984 National Computer Conference. Las Vegas, NV. Contact: American Federation of Information Processing Societies, Inc. 1899 Preston White Drive, Reston, VA 22091. (703) 528-0114.

July 10-13

Knowledge-Based Systems, AI and 5th Generation Computing. San Diego, CA. Contact: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Pl., PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

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