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JULY 1984

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- IBM PC COMPATIBILITY
- S-100 BUS
- DISPLAY PROCESSORS
- WORKSTATION VS. MAINFRAME ENVIRONMENT
- HARDCOPY

Beautiful Streamer

Kennedy proudly announces Model 9600, the first member of a new family of advanced low cost formatted tape drives. A few of its many features include; Autoload; 800/1600 CPI dual density; streaming capability of 100 ips; a capstan motor which provides an amazing 45 ips true start/stop mode; PC boards which may be moved or replaced in any order on a common bus for upgrading to higher performance levels or different interfaces — the list, fortunately, goes on and on. Write or call today.

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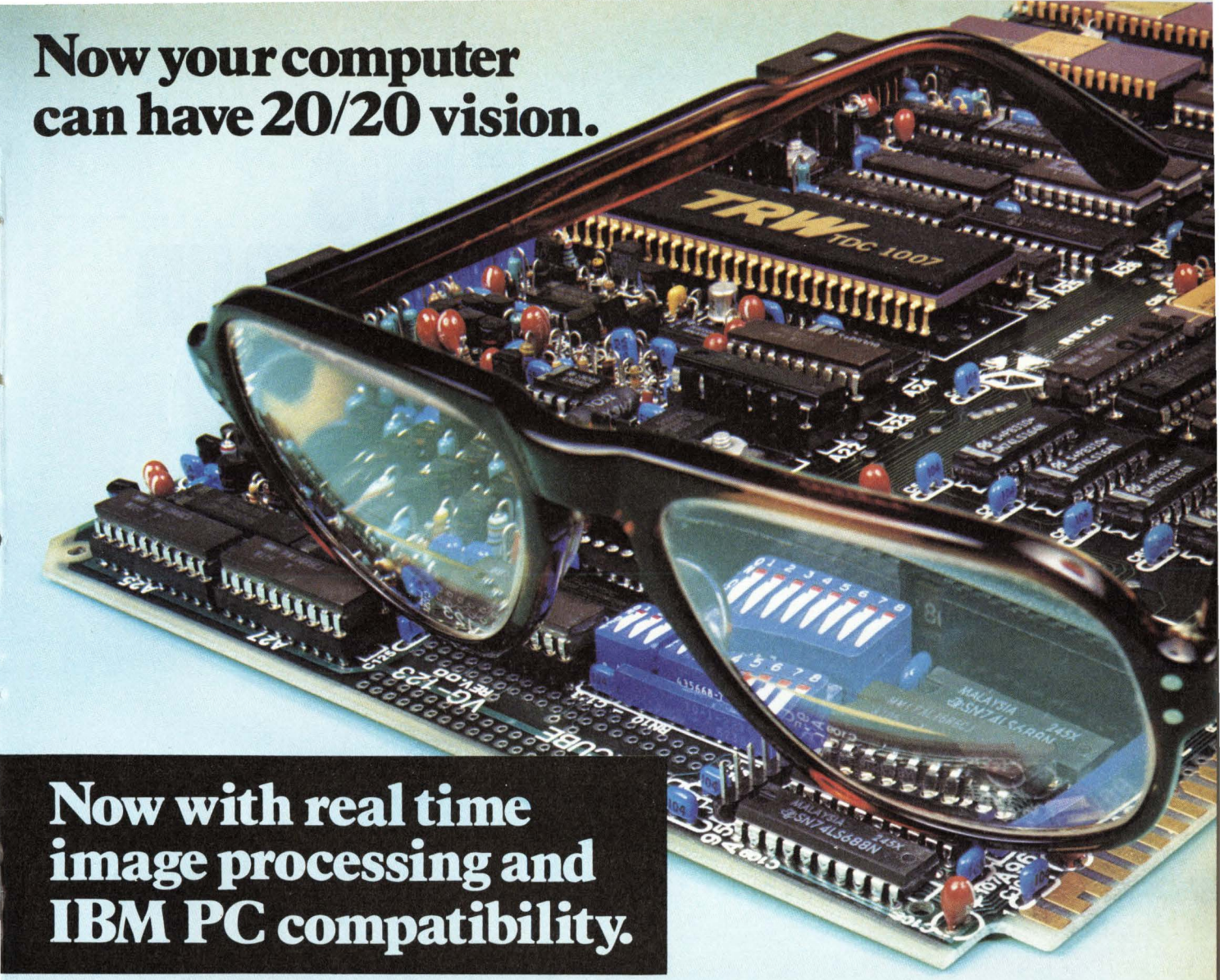
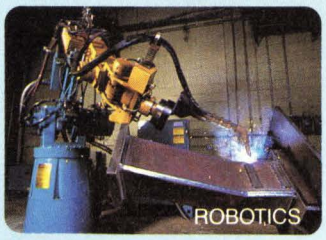
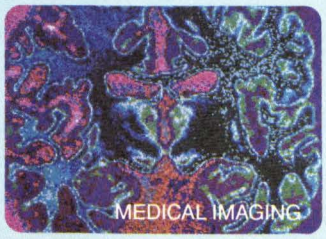


Now with real time image processing and IBM PC compatibility.





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The new IVG-128 is a complete video acquisition and display module on a single IBM PC compatible card. It features input & output look up tables, an 8-bit digitizer, and RGB 8-bit outputs.

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Call or write for our new Product Guide of Multibus, Q-Bus, and IBM PC compatible boards and systems. Datacube Incorporated, 4 Dearborn Road, Peabody, MA 01960, Telephone: (617) 535-6644.

Datacube

We'll look for you at **SIGGRAPH '84!**

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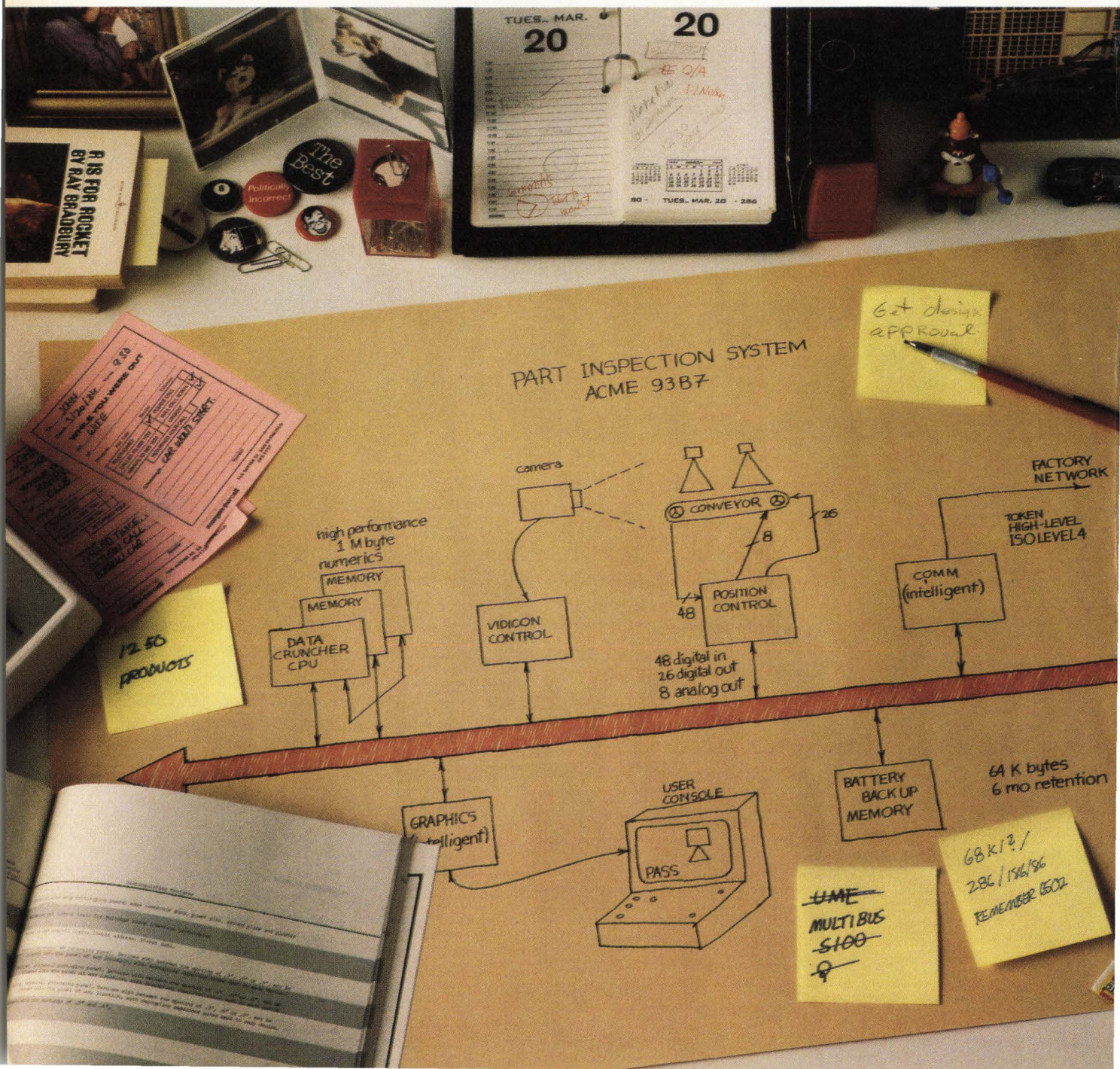

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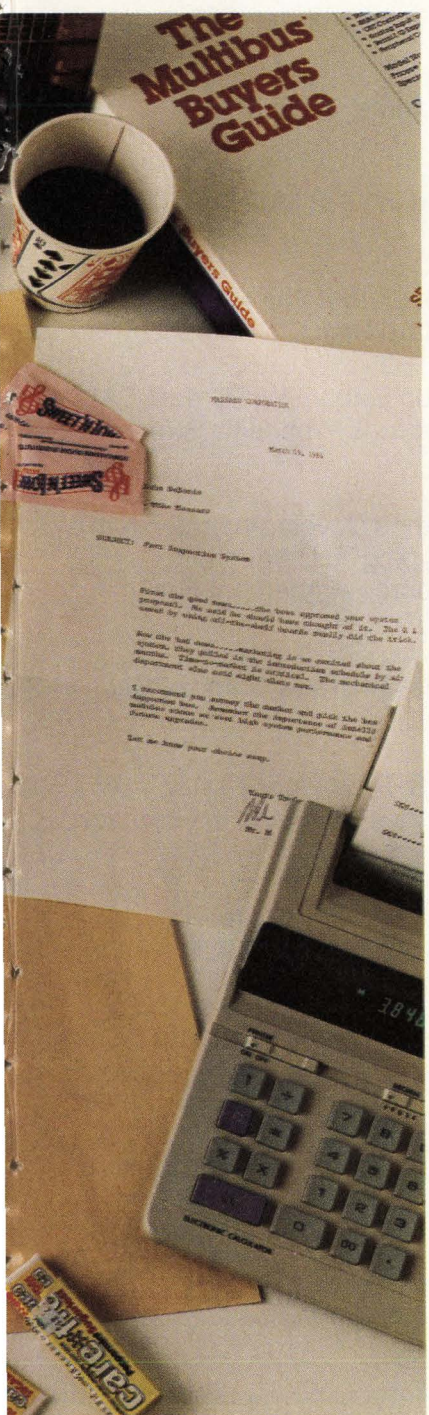

First, consider having a wide open road ahead. Only MULTIBUS supports more than 30 different operating systems. And all the major microprocessors. Seventeen, in fact. So you can drive your design right at the ultimate application. Even change your mind when the market changes its. And thoroughly profit from Intel's open systems approach.

It will also comfort you to know that MULTIBUS is the world's best supported architecture. Over 200* companies make and distribute MULTIBUS products. Giving you a selection of more than 1250* products.

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Next, consider that MULTIBUS supports all levels of integration. Chips. Boards. And boxes. From leading edge to commodity. So while you're custom-configuring your own product, you can count on getting exactly what you need. Hardware and software. And service along the way.

Finally, MULTIBUS keeps you fueled up for whatever's coming around the next bend. With a defined upgrade path to MULTIBUS II.® Which, by the way, is the most advanced bus architecture going. And which already has over 100 companies committed to its support.

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Because there's no good reason why you should find yourself up the road without a paddle.

intel®

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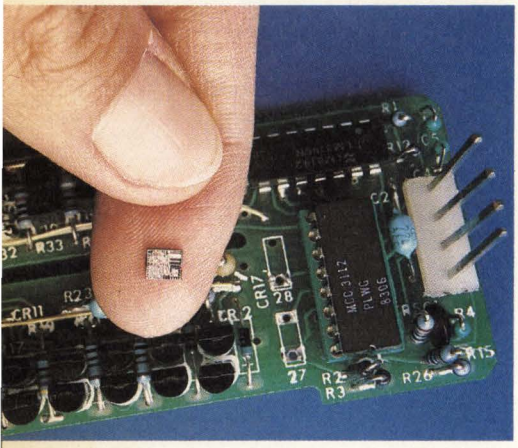
JULY 1984 VOL. 14 NO. 7



COURTESY GENERAL ELECTRIC

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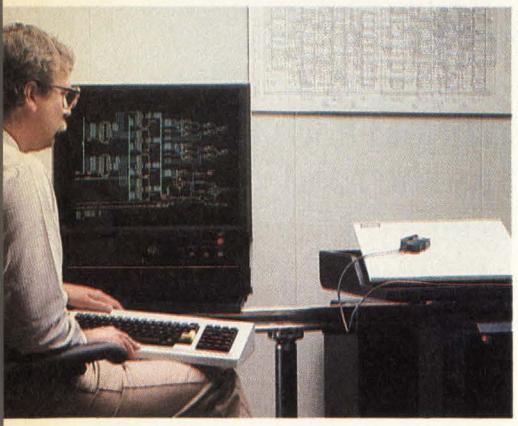
COURTESY XTAR ELECTRONICS, INC.

94 Display Processors



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100 Design Environment Issues

DEPARTMENTS

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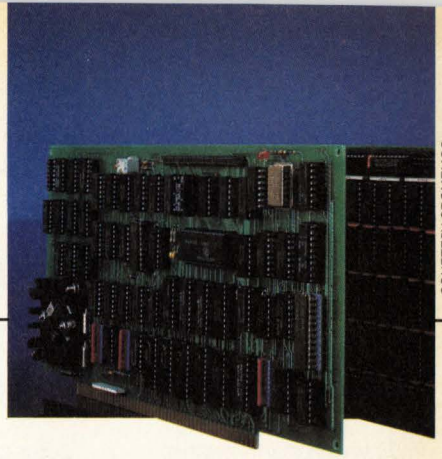


COURTESY CROMEMCO

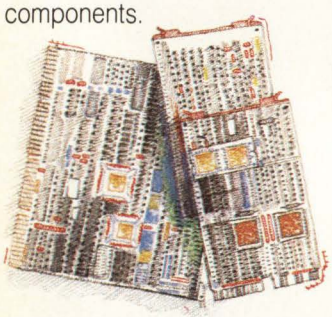
FEATURES

ON THE COVER

The 156A in-circuit programming system from Data I/O programs multiple circuit boards of EPROMs in one operation. Because parts are programmed on the board, physical limitations of conventional programming are eliminated. The designer can use flat packs, hybrids and leadless chip carriers for maximum board densities or vibration prone EPROMs can be soldered without sacrificing programming flexibility. Photo courtesy Data I/O. Concept by Paul Prentice. Photo by Michael Ramey.

NOTHING IN THE WORLD SUPPORTS OEMS LIKE Q-BUS.

Few companies could legitimately promise you either the experience or the insight into the OEM market that has helped make Digital the number one choice and world's leader in systems and 16-bit components.



With well over 25 years' experience behind us, we've learned quite a bit about what it takes to be a good OEM and how we – as a supplier – can help.

We're aware of your concern for reliability and dependability. With your name on the product, you're naturally the first one to get any calls.

We appreciate the deadlines you're forced to deal with. And your need for the thorough documentation and manufacturer's support that can help you beat your competition to market.

We also understand the commitment you make when you select an architecture. And your need for support of that architecture. Not just from the manufacturer, but from third party sources as well.

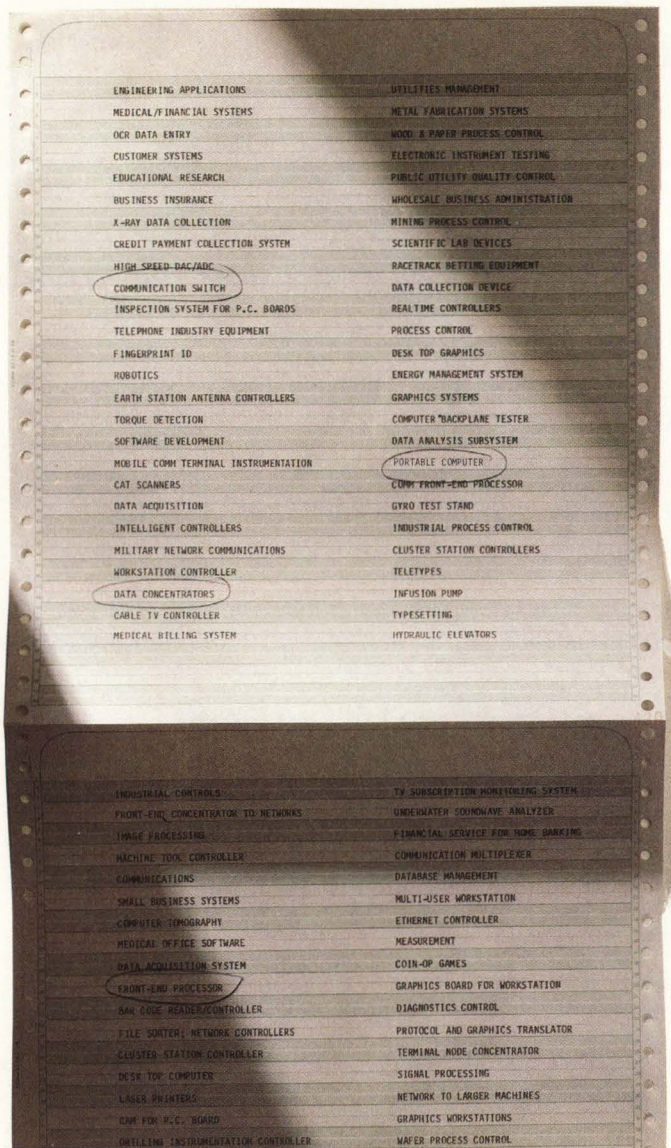
These are precisely the reasons to choose Digital's Q-Bus* architecture. Because only Q-Bus gives you the proven products and technologies, the flexibility, the commitment and support to help you reach your market. On time. And on target. With a minimum of risk.

CHOOSE THE INTEGRATION LEVEL THAT'S MOST PRACTICAL FOR YOU.

Q-Bus is nothing if not flexible. And that flexibility begins with the level of integration you choose. From chips to boards to boxes to complete systems.

You may, for instance, have the time and resources to develop your own system around one of our J11* microprocessors, thus helping to reduce your hardware costs.

On the other hand, if deadlines are tight, you might opt for one of our complete systems, like the standalone Pro 350* workstation, the multi-user MicroPDP-11,* or our powerful 32-bit desktop MicroVAX I.* By radically reducing development time, perhaps almost eliminating it altogether, you increase your chances of beating your competition to market, thus permitting you to earn the higher margins available at the beginning of a product life cycle.



If your needs fall somewhere in between, we recently introduced three board level CPU products to work with. Our LSI-11/73,* a new CMOS microcomputer that benchmark studies show exceeds the performance of a similarly configured MC68000 or NS 16032 in most applications. Our KXT11-C* peripheral processor, which for the first time allows you to place multiple PDP-11* processors on the Q-Bus, assigning separate tasks to each. And Falcon-PLUS,* one of the smallest 16-bit single-board computers for dedicated or limited RAM applications. In addition, you have two versions of Micropower/Pascal* system software available to you for use in VMS* or RSX* development environments.

Digital's new board-level products also take full advantage of the Q-Bus' block mode transmission, which effectively doubles previous throughput to nearly 3 megabytes per second. That means Q-Bus – along with these new products and future generations – will be running strong well into the future with the full commitment of Digital behind them.

And since all are based on the industry standard PDP-11,

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you get the best of both worlds. Advanced capabilities. With proven technologies. So you become more competitive with less risk.

COMPATIBILITY MEANS MORE FLEXIBILITY, LESS REDEVELOPMENT.

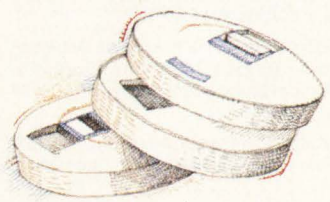
From the beginning, Digital has been dedicated to a single philosophy with its product families. Compatibility. Not just from product to product. But from generation to generation.

To the OEM, that's particularly important because it means you can upgrade your product at any time you like, with an absolute minimum of development.

Suppose, for instance, you designed around the world's first 16-bit microcomputer, our LSI-11*. And now you find that new demands on your product require a more powerful system. Upgrading your processor to our LSI-11/23* or LSI-11/73 is a simple matter. You don't need to learn a new operating system. And the changes to your software are absolutely minimal. With Q-Bus, instead of going back to the boards and starting over, you move your product to market. Faster. With far less expense.

MORE THIRD PARTY SUPPORT THAN ANY OTHER ARCHITECTURE IN THE WORLD.

Your advantages continue with the broad choice of peripherals available to you.



Q-Bus is not only supported by Digital's own line of processors and peripherals, but by those of any number of third party sources as well. From memories to mass storage to a complete range of I/O interfaces.

So chances are, you can design your custom system around existing hardware, rather than developing your own or working around someone else's limited product offering. And you may modify your product later with little concern over development costs or delays.

BEST ENGINEERED MEANS ENGINEERED TO A PLAN.

Digital's Q-Bus products, like all Digital hardware and software products, are engineered to conform to an overall computing strategy. This means that our systems are engineered to work together easily and expand economically. Only Digital provides you with a single, integrated computing strategy, from chips to 32-bit systems, and direct from desktop to data center.

For more information about Digital's OEM products, simply fill out and return the coupon below. Or contact one of Digital's Authorized Industrial Distributors. Or call 1-800-848-1400, ext. 139. In Canada, call 617-542-6283.

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For more information, write: Lundy Electronics & Systems, Inc., Glen Head, New York 11545, or call: (516) 671-9000.

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Mt. Everest, symbolic of aiming high, was generated on the Lundy T5680 raster. It offers 16 colors and 136 shades from a palette of 4,096 colors.

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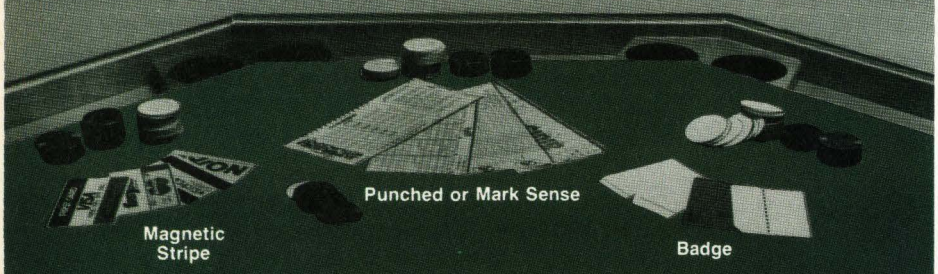

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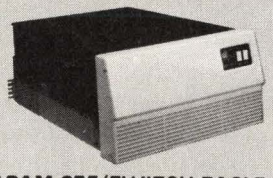


DATARAM S35/FUJITSU EAGLE

Fujitsu's Eagle, combined with Dataram's S35 controller, adds up to more than a high performance alternative to DEC's UDA50 subsystem. This package of peripheral performance conforms to DEC's MSC protocol and gives you 474 MB of storage at a data rate of 1.8 MB/sec. The S35/Eagle subsystem interfaces to the PDP or VAX UNIBUS and functions under all of DEC's current operating systems, including VMS.

DATARAM D30

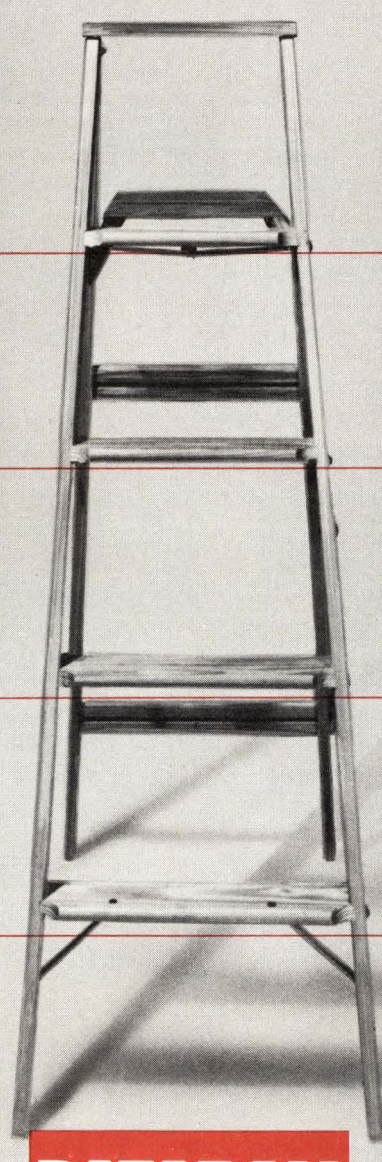
"Versatile" is the only word that can describe our 7" D30 subsystem. It combines a ¼" start-stop/streaming cartridge tape unit and an 8" Winchester. The D30 uses the 70 MB CDC Sentinel cartridge drive and emulates the TS11 or TSV05. The Winchester emulates RM02, RK06/07, or the new UDA50, and provides 80 or 160 MB. The D30 operates with all of DEC's minicomputers: LSI-11, PDP-11, VAX, and microVAX.

DATARAM D23

This RL02-emulating subsystem for the Q-Bus provides a 10.4 MB fixed/10.4 MB removable Winchester along with an additional 20 MB Winchester. Both 5¼" Winchesters are directed by a single dual-board controller which treats the total 40 MB capacity as four logical RL02s.

DATARAM FD-311

RX01/RX02/RX03 dual floppy subsystem packaged in a compact 5¼" chassis. Our FD-311 and larger-capacity FD-511 come with a dual-board controller for the LSI-11 Q-Bus or a quad-board controller for your PDP-11 and VAX UNIBUS.



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Computers can not only add and subtract. They can divide.

RACAL

To shorten your electronic design times, you can provide your project teams with Computer-aided Engineering, Design and Manufacturing systems. And those systems will do their individual jobs very well.

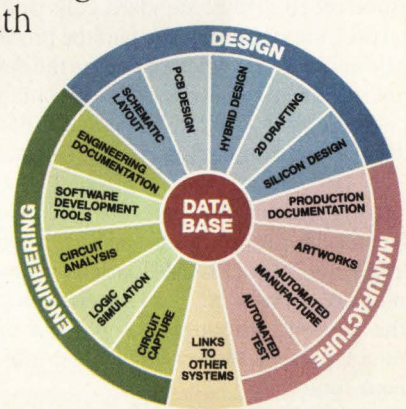
However.

As soon as you try to transfer the data generated by your engineers to the design stage (not to mention manufacturing) you'll find you have a problem. Because none of the systems are fully compatible with each other. Engineering can't get along with Design. Design can't get along with Manufacturing. And vice versa. Worse still, when the systems can't get along, neither can the people using them. So instead of state-of-the-art, you end up with something akin to a state of war.

The solution, of course, is to work with one company that can handle the entire project from beginning to end. A company with a full range of modular systems for every stage of every electronic design project. All fully integrated around a common data base.

That company is Racal-Redac.

With Racal-Redac, you can solve today's problems without creating new problems for yourself tomorrow. Because all the system modules were designed to work together, and grow with you as your needs grow.



Finally, a totally integrated capability for electronics.

Read that last paragraph again. We at Racal-Redac are talking about a range of complete, totally integrated systems which work for you through every stage of the design cycle.

Only unlike other companies, what we're talking about isn't a vague promise for the future. Racal-Redac systems are already hard at work right now in over 1,000 electronics companies around the world. Any one of which we will be happy to discuss in considerable detail.

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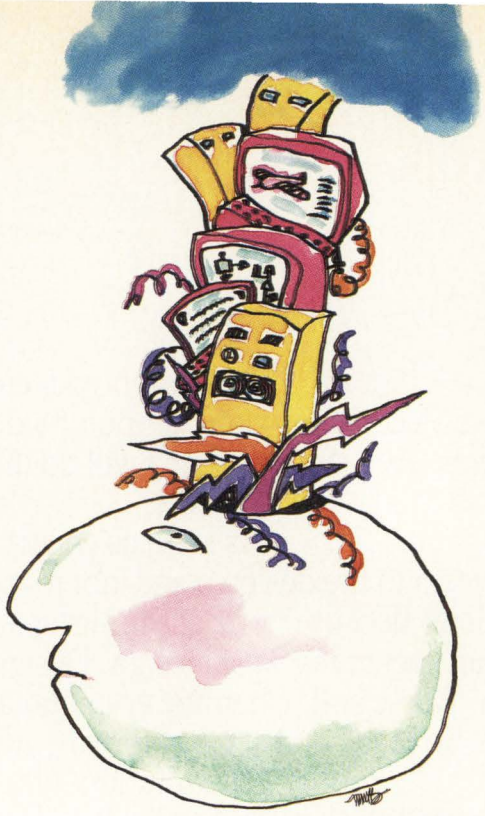
"The real question is whether to base the design environment on a mainframe or a network of self-contained workstations."

EDITOR'S COMMENT



Getting more performance out of a system design may in the past have meant evaluating newer off-the-shelf products. Today, however, a number of semi-custom and full-custom schemes exist that may provide more cost-effective, higher-performance solutions than previously available – throwing the ball back in the designer's court. Evaluating the differences between these schemes, which may include programmable logic, gate/macrocell arrays, standard cells and handpacked custom, however important, is only half the problem. The real question to be addressed is whether to base the design environment on a mainframe or a network of self-contained workstations. In this issue, Ron Collett, Technical Editor, will take a look at some of the options facing engineering management in the field.

Today's off-the-shelf catalog parts are not only getting more complex, but also more application specific in nature. With the Japanese producing 256K DRAMs like jelly beans, newer start-up companies are carving out very specific niches for themselves in the market. Although this is most evident in the memory arena at present, the trend is likely to affect other areas too in the near future.

One environment closely tied to the use of large amounts of memory is that of graphic system design. In this issue, Greg MacNicol, West Coast Technical Editor, not only looks at some of the newer memory devices specifically suited to graphics applications, but also examines the trend towards developments in VLSI to produce video control ICs, dedicated graphics engines and single chip controllers.

Until recently, the programming of EPROM memory has necessitated the removal of the EPROM device from the board. Many trends, however, in EPROM usage do not lend themselves to off-board programming, causing the designer to sometimes compromise design for manufacturability. An alternative approach, one described by Mike McGee in this issue, is the use of in-circuit programming techniques that allow the installation of blank EPROMs into the PCB and the programming and reprogramming of the devices without their removal.

Interestingly, to alleviate some of the problems associated with understanding these newer ICs, some companies are offering board-level solutions that may cut learning time and facilitate the integration of their product into systems. Board level solutions offer the system architect a reduction in design/production time of about half over the IC approach.

Although many new bus structures have recently emerged in the marketplace – VME, Multibus II and the NUBus, in this issue we have taken a look at one of the older bus structures – the S-100. Although the S-100 is a mature market, it still remains an alternative to the lower-cost STD bus and the high-end Multibus. Today, it has found its widest acceptance in the design of low-cost multi-user systems.

Perhaps the greatest challenge facing the OEM board market, particularly the S-100 bus, has come from the IBM PC. The IBM trademark, the integrated CPU-in-a-box approach, and a wide range of compatible vendors have given IBM 25% of the personal computer market, according to Andrea Coville, New Products Editor, who prepared this month's Industry Review, dealing with the issue of PC compatibility.

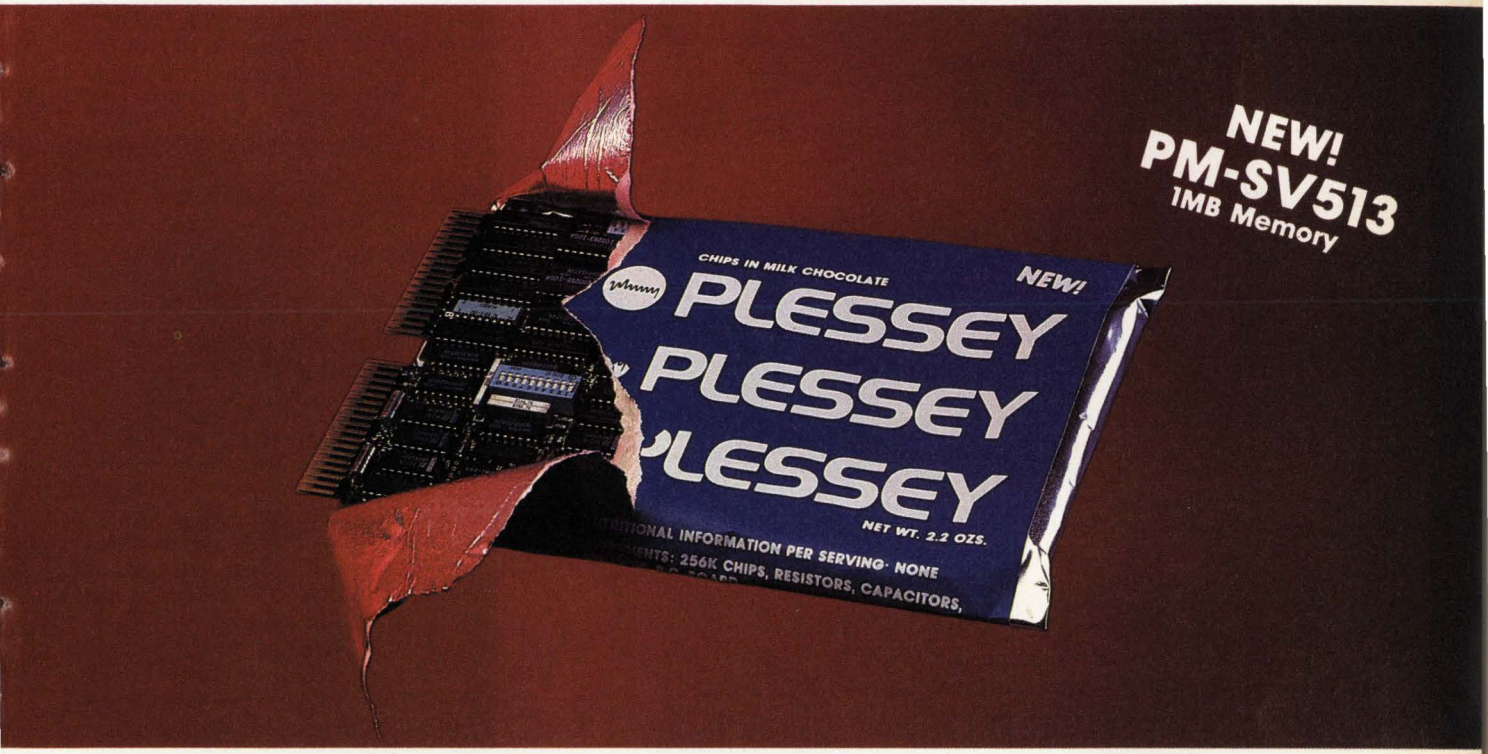
Manufacturers of third party products have saved IBM an enormous amount of research and really pushed the acceptance of the PC into a wide variety of markets. The market for the IBM PC is so large that it has attracted a number of manufacturers that traditionally built products solely for the OEM. These companies, including Interphase, Priam and Datacube, have by necessity changed their marketing philosophy to meet the new market. Interphase, for example, is placing a lot of emphasis on marketing its new 75 Mbyte PC disk subsystem through retailers and distributors. Similarly, Priam, with its DataTower storage products and interface cards for the IBM PC and Apple Computers, is selling through value-added resellers (VARs) as well as through its direct sales force and distributors.

According to Stanley Karandanis, President of Datacube, the IBM PC user is a less sophisticated customer who must be provided with a great deal of software support. Datacube will market its new single board real-time video acquisition and display board for the PC both directly and via distribution.

The choice of whether to base a design around ICs, boards, or system level products is a decision that requires the evaluation of many parameters, including market window and product cost. Only by covering all these subject areas can *Digital Design* make an effective contribution to the industry.

Dave Wilson, Executive Editor

Performance, Price, Plessey



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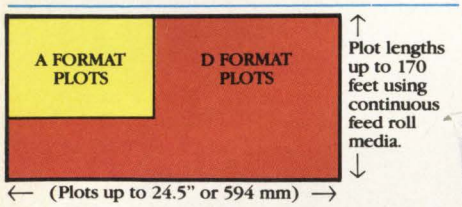
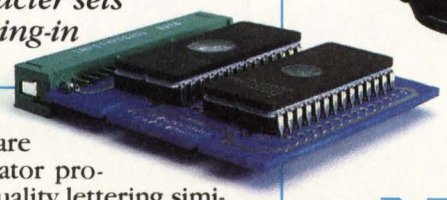


Now you can create virtually any size plots you want up to 24.5" wide, including ANSI sizes A-D and ISO sizes A4-A1, on cut sheet or roll media. Use standard bond paper, glossy bond, vellum, clear film or mylar.

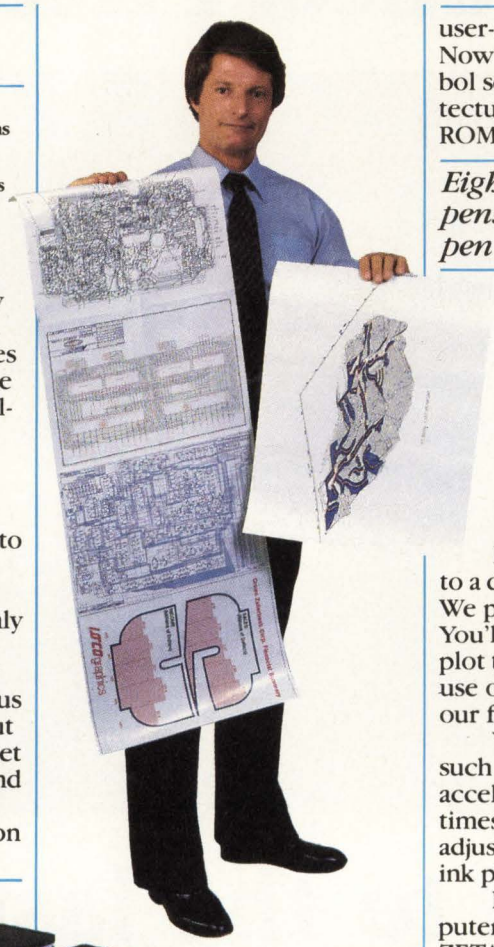
Run dozens of entirely different plots automatically thanks to a built-in microcomputer that can be pre-programmed to plot on roll media up to 170 feet. Then quickly switch to cut sheet plotting – great for your pre-printed forms. The ZETA 822 is the only plotter that can do both.

Best of all, we've got line quality and throughput at a price that makes us the cost-effective choice for just about anybody's plotter applications. You'll get vector independent speed of 25 ips. And 2 g acceleration insures the plotter reaches top speed fast. With resolution of one-one thousandth's of an inch.

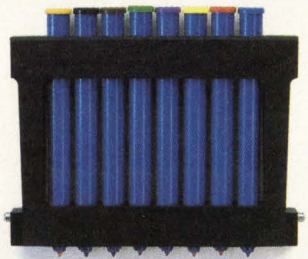
Change character sets just by plugging-in a ROM chip.



Our firmware character generator produces typeset quality lettering similar to the popular Helvetica font with user-controlled proportional spacing. Now you can add special character symbol sets for both engineering and architecture simply by plugging in a new ROM chip.



Eight color, carriage-mounted pens eliminate time-consuming pen changes.



Incredibly, some plotters still grind to a dead stop to change pens. Not ours. We put all eight pens on the carriage. You'll be amazed at what that does for plot throughput. And when you want to use our liquid ink option, just snap in our four-pen cartridge.

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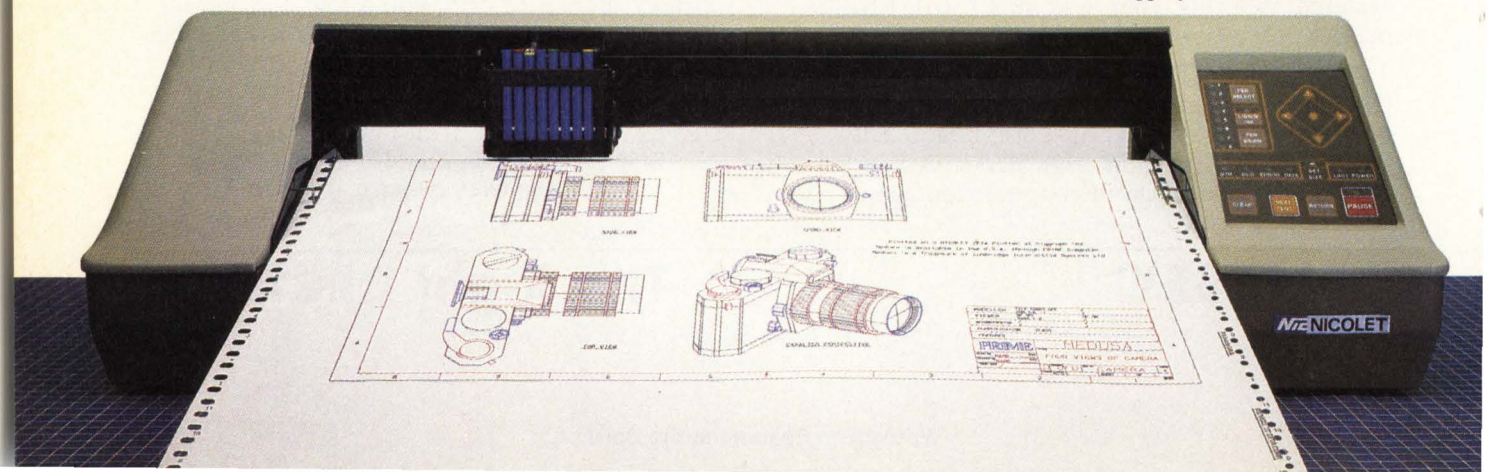

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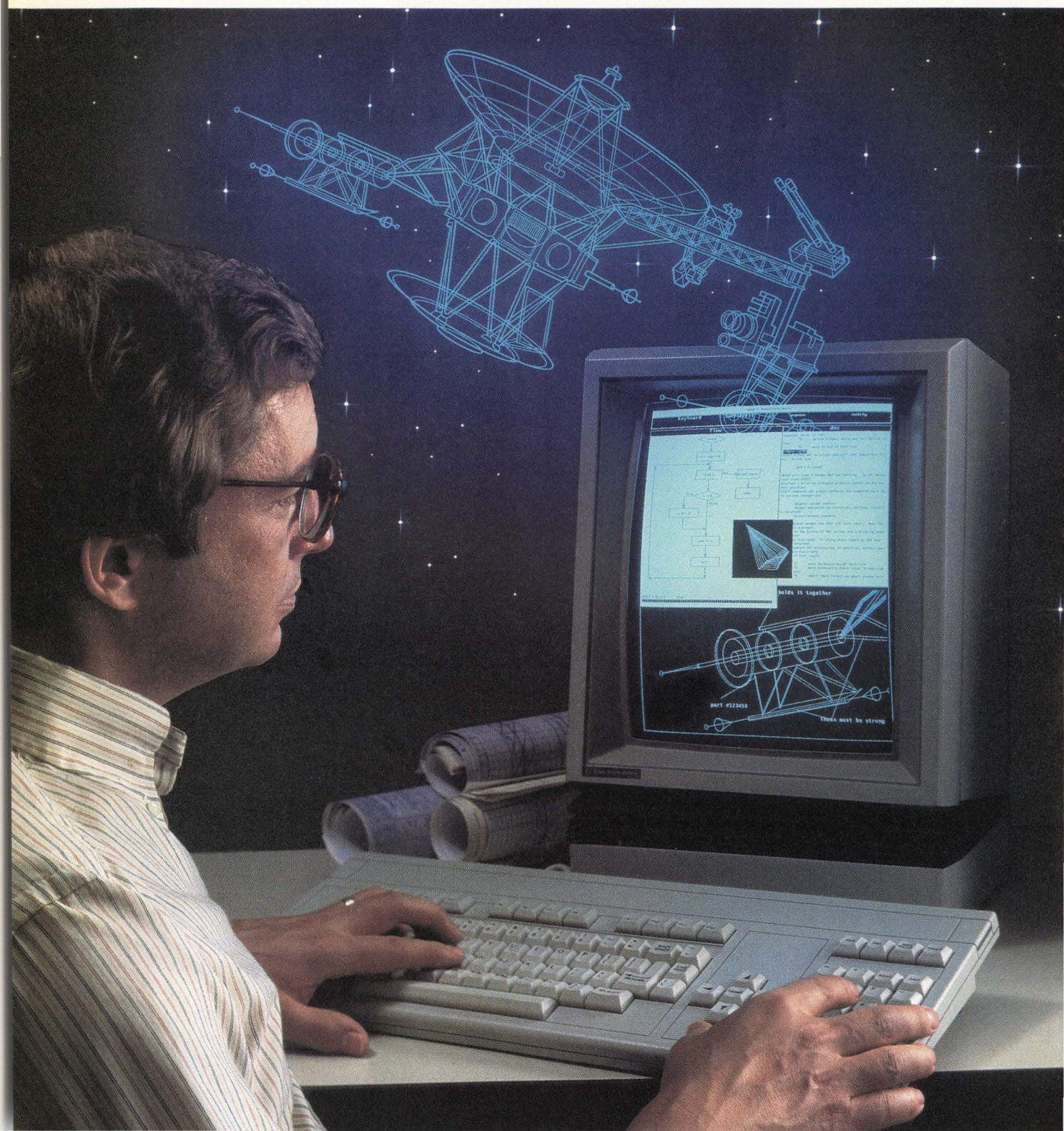
Introducing TI's Climb on the 32-



Nu Machine. bit NuBus now.

The Nu Machine™ Computer. The first system in the Texas Instruments Nu Generation Computer family. The only system now available built on a modern 32-bit bus. The processor-independent NuBus™ architecture helps meet your advanced-technology design requirements today. And tomorrow.

First high-performance 32-bit bus

The NuBus technology, designed at M.I.T., is optimized for 32-bit data and address transfers. Its 37.5-Mbyte/sec bandwidth combines with an elegant arbitration scheme to ensure fast and fair data flow.

Innovative, flexible architecture

The NuBus design was developed to support sophisticated system architectures and eliminates the built-in obsolescence of processor-dependent systems. It lets you concentrate on developing applications, not architecture. Your significant investments are protected as new technologies develop.

The Nu Machine's open architecture solves your make vs. buy dilemma. Multiple-processor configuration support combines with the NuBus high bandwidth, high-resolution graphic displays, cache memory, and high-speed disks to make the Nu Machine system attractive to sophisticated end-users, systems integrators, and OEMs in the engineering and scientific marketplace.

Anticipating industry trends, the power and expandability of TI's Nu Machine allow it to accept 32-bit processors of the future.

Open system supporting industry standards

TI's Nu Machine system is currently available with a 10-MHz 68010 processor supporting a UNIX™-based operating system with enhancements for windowing and high-resolution displays.

Those who want to design their own system processors and controllers can now license the NuBus design from Texas Instruments.

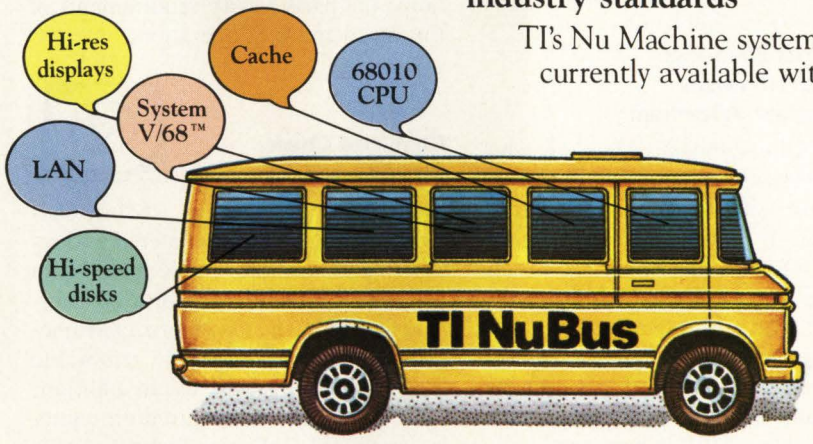
Also, a NuBus-to-Multibus™ converter allows the use of existing interface cards and peripherals from third parties.

The system you can build on from now on

Because its high performance and flexibility are designed for the long run, TI's Nu Machine can be updated when other systems are outdated.

And, Nu Machine computers are backed by TI's service and customer-support network and by TI's commitment to quality and reliability.

To climb on the NuBus bandwagon, call toll-free: 1-800-527-3500. Or write Texas Instruments Incorporated, P.O. Box 402430, Dept. DNA203DI, Dallas, Texas 75240.



Combining innovative NuBus architecture with advanced graphics, powerful peripherals, and UNIX-based software, TI's Nu Machine provides the outstanding performance and flexibility required by scientific and engineering systems designers.

Nu Machine and NuBus are trademarks of Texas Instruments Incorporated
Multibus is a trademark of Intel Corporation
System V/68 is a trademark of Motorola, Inc.
UNIX is a trademark of Bell Laboratories

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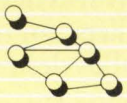
UPDATE

DEC Introduces OPS5

Digital Equipment Corp. announced its first commercially available Artificial Intelligence (AI) product, the OPS5 programming language for its VAX family of computers. OPS5 is targeted for companies with in-place AI departments, OEMs, and software houses wishing to build expert-system applications. The new language runs under the VAX/VMS operating system. It is intended for use by software engineers trained in AI methodology and technology for encoding knowledge from human experts in the form of production rules.



OEM Networking

Novell Inc. has reached an OEM agreement with Corvus Systems of San Jose, CA, under which Novell will offer NetWare/OMNINET, a complete hardware/software package to link (network) IBM-XTs, IBM PCs, and IBM compatibles, allowing OMNINET local area network (LAN) users to run applications software in a multiuser environment. The NetWare/OMNINET Starter Package contains two OMNINET Transporter cards, the NetWare/O file server operating system and documentation, and a thirty-foot cable and connectors. According to Novell, the package contains the NetWare operating system, a fully-functional file server, which enhances the performance of OMNINET, Corvus System's LAN.

Hughes Opens AI Facility

Officials of Hughes Aircraft Company recently participated in the official opening of a new facility that will house the company's efforts in artificial intelligence. The facility, Hughes' Artificial Intelligence Center (Calabasas, CA), will be operated by the company's Electro-Optical and Data Systems Group, headquartered in El Segundo, Calif. Existing artificial intelligence projects from other Hughes facilities will bring research and development efforts under one roof.

Hughes commitment to AI includes company-funded efforts that will involve USC, UCLA and major universities around the country. The Hughes effort will include projects in self-controlled systems and image understanding.

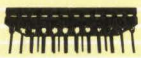
Western Digital Goes to Japan

Western Digital Corp. has announced plans to form a new company in Tokyo, Japan, to handle sales and distribution of the company's semiconductor components and digital subsystems in the Northern Pacific region. A regional sales office located in Japan will be opened in the near future.

Launch New Venture

Burr-Brown Corp. has concluded agreements with Intelligent Instrumentation, Inc., of Tucson, AZ, to jointly pursue the growing market for microcomputer-based instrumentation. Intelligent Instrumentation, Inc., is a newly-formed venture that is developing a broad line of hardware and software. These products will be used in instrumentation systems for data acquisition, test, measurement and control.

Intel Licenses Oki



Intel Corporation has licensed Oki Electric Industry, Ltd. to market CMOS versions of Intel microprocessors, microcomputers, and related peripheral devices. The agreement calls for Oki to develop CMOS products compatible with existing Intel devices. It establishes licenses for the worldwide manufacture and sales of devices made with the low-power, high-speed CMOS technology.

Siemens Enters Programmable Controller Market

Siemens-Allis Automation, Inc., a newly formed Siemens Company, will enter the growing market for Programmable Controllers (PCs). Aiming at factory automation requirements throughout the U.S., the Company will market a full line of industrial PCs and related equipment. These products are designed for both stand-alone and distributed operation in process and machine control applications. Siemens-Allis Automation will maintain full marketing, R&D, and manufacturing capabilities in the U.S., and products will be sold through a network of independent distributors, assisted by a direct field sales force.

Drivetec Second-Sourced By Six

Drivetec, Inc., a manufacturer of half-height, 5.25" high-capacity, high-performance disk drives, said that it has qualified six leading media manufacturers and concluded with them second source agreements on formatted disk for its 3.33 Mbyte SuperMiniFloppy disk drive. The companies are BASF Systems Corp., Bedford, MA; Brown Disk Manufacturing, Inc., Colorado Springs, CO; Dysan Corp., Santa Clara, CA; Maxell Corp., Conyers, GA; Memorex Corp., Santa Clara, CA; and Spin Physics, a division of Eastman Kodak Co., San Diego, CA. The suppliers will provide media formatted to the Drivetec drive on the open market to OEMs and users.

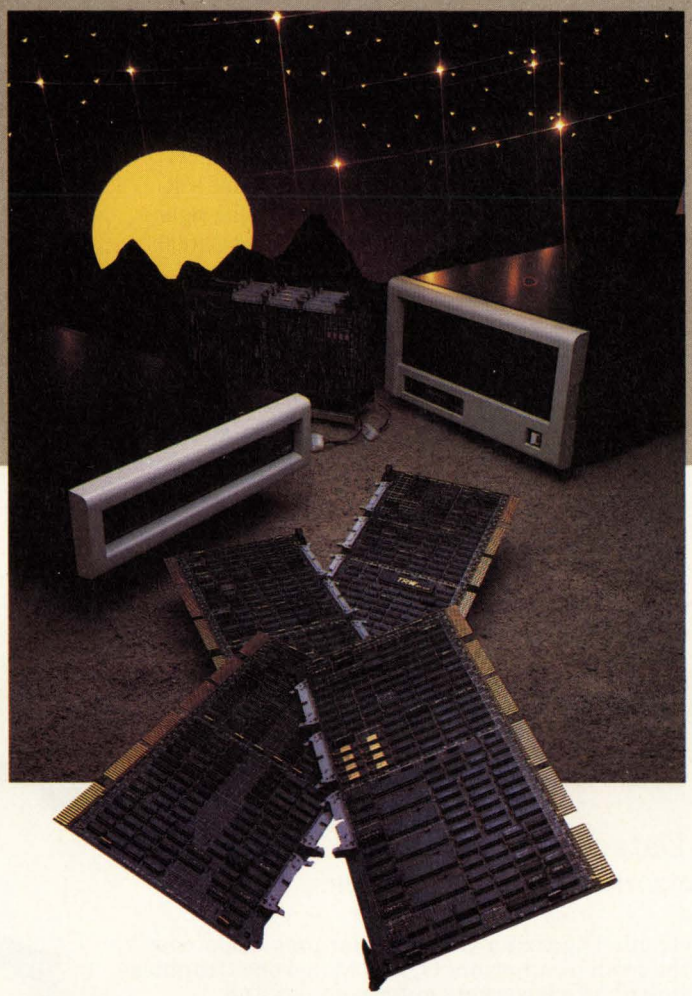
Gould Second Sources Hitachi

Gould AMI Semiconductors, and Hitachi, Ltd. (Tokyo), have signed an alternate-source agreement for the Hitachi family of codecs. By this agreement, Gould AMI becomes the first U.S. alternate source for the popular Hitachi HD44230 series of single-chip codecs. The HD44230 (S44230) series features preadjusted internal voltage reference and low operating and idle power consumption. The series also includes both asynchronous codecs for applications in transmission systems and synchronous codecs. Available in A-law and μ-law options, the parts satisfy requirements of European and U.S. operation.

Optical Disk Drives R&D

Information Storage Inc. (ISI) of Colorado Springs, CO, has entered into research and development contracts with Tallgrass Technologies Corp. of Overland Park, KA and CPT Corp. of Minneapolis, MI to develop 5¼" removable media optical disk drives. In addition, each company has acquired an equity interest in ISI. Tallgrass Technologies is a supplier of fixed-disk storage and cartridge-tape backup systems which are marketed nationwide as memory extensions to IBM and other personal computer manufacturer's products.

Because You need to run FORTRAN programs 10X to 100X faster...



Mini-MAP makes it practical to apply array processing to general-purpose scientific and engineering computing.

Practical in terms of use: Mini-MAP's compiler allows you to program the array processor directly in FORTRAN. An assembler, a linker, and a debugger are also part of the package. Plus you can use our library of over 250 highly optimized scientific subroutines.

Practical in terms of throughput: Because it is an array processor, Mini-MAP increases the computing speed of a mini or super-mini computer as much as 10 to 100 times. Where it takes a typical minicomputer minutes to perform tasks such as image rotation, Mini-MAP reduces interactive response times to seconds. Your computer may require hours to perform each step of a trial-and-error-process such as simulation, but Mini-MAP, can zip through in mere minutes.

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Practical in terms of cost: Mini-MAP is available as an economical, four-board set or as a packaged system. Now, with Mini-MAP, OEMs can offer their customers a better product at lower costs. Mini-MAP's low power demands, small size, and high reliability make the package extremely attractive. And end users will find our FORTRAN compiler and other software tools minimize program development costs.

Some practical things to know about Mini-MAP: 32-bit DEC™ floating point format ☐ Interfaces to DEC PDP-11, LSI-11, and VAX-11 series ☐ Up to 16 MBytes of data memory ☐ 1024 x 1024 2-D FFT in 8.8 seconds ☐ Extensive software tools plus dedicated applications assistance including training, convenient parts depots, and field service staff support our worldwide installations.
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UPDATE

U.S. Design Signs With Maxtor

U.S. Design Corp. has signed a contract with Maxtor Corp. for the purchase of 190 Mbyte disk drives, the most advanced 5¼" Winchester disk product available in the industry. USDC will use these new units in their recently introduced Virtual Information Processor/Extended (VIP/X), a 760 Mbyte subsystem with fast data access.

Sun Signs For $7.5 Million

Sun Microsystems, Inc., a $7.5 million OEM contract with Chromatics, Inc., (Tucker, GA), for integration of Sun's general purpose workstation into Chromatic's product line. Under the terms of the contract, Sun's Model 2/120 FS Deskside SunStation will be used by Chromatics and its customers in conjunction with the recently-announced CX 1500 Colorgraphic Engine. Chromatics will also use the SunStation in its new VLSI Designer II Workstation, currently being delivered to major semiconductor manufacturers.

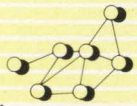
Series 32000 Development

National Semiconductor Corp. and Texas Instruments Inc. announced a long-term cooperative technical effort in the area of advanced 32-bit microprocessors and peripherals. In conjunction with this announcement National has renumbered its high-end microprocessor line as the Series 32000. National and TI will exchange specific technologies in the 32-bit field, including development, support and software. In addition, TI acquires the right to manufacture National's Series 32000 family of microprocessor products.

Cray Contracts IBIS

IBIS Systems, Inc. (Westlake Village, CA) has signed a two-year, multi-million dollar contract with Cray Research, Inc., (Chippewa Falls, WI) to supply its advanced, large-capacity disk drives to the super-computer manufacturer. IBIS designs and builds high-capacity 14-inch Winchester disk drives that provide 1.4 Gbytes of storage. With a 12 Mbyte per second data transfer rate and a track-to-track access time of 2.5 ms with an average access time of 16 ms.

PC/NOS For Fujitsu



Applied Intelligence, Inc., manufacturer of the network operating system PC/NOS, has signed $1 million OEM agreement with Fujitsu Microelectronics, allowing Fujitsu to distribute PC/NOS for use with the Fujitsu Micro 16s Personal Business Computer. Fujitsu has licensed PC/NOS modules capable of connecting Micro 16s computers that use CP/M, CP/M-86 and MS-DOS operating systems.

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QVT™ TERMINALS

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WASHINGTON REPORT

by Anne Armstrong

The Paperless Patent

Planning Research Corp. has been awarded a contract to automate the U.S. Patent and Trademark Office as part of a plan to achieve a paperless patent procedure by 1990. Under the terms of the contract – which has a potential value of more than $300 million over the 20-year life of the project – PRC will purchase and supply hardware according to government regulations. Software for the mammoth undertaking will be designed by the Chemical Abstracts Service, a division of the non-profit American Chemical Society.

PRC planners selected Chemical Abstracts for the software duties because a large number of patents include chemical data, and CAS has already developed a computerized identification and notation system for its own chemical database.

The PTO currently has on file some 25 million documents and expects that number to double by the end of the century. The addition of a computerized application, examination and issuing procedure is expected to reduce the time taken to process a patent from the present 27 months to 18 months.

The patent contract calls for the first six years to be devoted to the installation of hardware and the latter 14 years, for the maintenance of the system. PRC will receive $8 million for work in the first year of the award.

The PRC proposal reportedly beat out a competing bid from a team lead by Computer Sciences Corp. in partnership with Integrated Automation, Mead Data General, and Derwent.

Protection For Semiconductor Masks

Like a locomotive slowly gathering speed, Congress is finally showing signs of making headway on legislation. The House Judiciary Committee has unanimously approved H.R. 5525, a compromise bill that provides a new type of protection, similar to copyright, for the masks used to manufacturer semiconductor chips. Although this is just the first step, Hill observers expect the bill to easily clear the full House and be quickly enacted by the Senate.

The original plan to protect the interests of semiconductor and computer firms against unauthorized copying was introduced by Rep. Don Edwards and Norman Mineta of CA. However, the bill met with opposition from the Copyright Office and a number of computer interest groups. A revised version of the idea was introduced by Rep. Robert Kastenmeier and it was the modified plan which passed the House committee.

The bill will give 10 years of protection to masks used to make computer chips, but it permits legitimate reverse engineering, protects innocent design infringers by limiting their liability to reasonable royalties, and stipulates enforcement by civil, rather than criminal, procedures.

The registration process will be handled by the Copyright Office and will begin Jan. 1, 1985.

Spare Parts Scam

After much publicity about the cost of spare parts for many DOD projects, the House Armed Services Committee approved legislation that would require identification of the actual manufacturer of any items supplied to the government, the national stock number, and whatever technical data is available for the equipment. House committee staffers suggest that with such information, parts could be bought more competitively.

In addition, the legislation bars prime contractors from restricting subcontractor direct sales to the government. Before any requisitions are approved, agencies would also be required to identify other possible sources for an item.

NBS And ISO Encourage Data Communications Standards

In an effort to get computer manufacturers to adopt the International Standards Organization data communications standard that has been developed by 30 computer makers from around the world, the U.S. National Bureau of Standards has set up two demonstration projects to show the protocols work in a practical setting.

General Motors will set up the factory project that will connect a group of mini and microcomputers in a mini-assembly line for cars. Boeing Computer Services Co. will handle the office project and will link graphics terminals and minicomputers in a local-area network. Both projects will be displayed at the National Computer Conference in July.

After years of warring about which standard was going to be used, there are now indications that manufacturers may be willing to settle on the ISO proposal as a compromise. The industry heavyweights, by their support of the standard, will speed its adoption. General Motors, for example, will use the ISO standard in a new factory planned for Saginaw, MI. Any vendor that wants to supply GM with equipment also must follow suit. Digital Equipment Corp. is also committed to the gradual adoption of the ISO standard.

Martin-Marietta Wins $225 Million Navy Contract

Martin-Marietta Data Systems of Bethesda, MD has won a 10-year contract from the U.S. Navy to set up an automated personnel and payroll system for Navy enlisted and reserve forces.

Under the terms of the contract, Martin-Marietta will install some 60 Hewlett-Packard Series 3000 mainframe computers at 36 processing centers around the world. In addition, the contact calls for 3,600 Hewlett-Packard terminals to be located in 400 sites internationally. Linking the system will be 2,000 pieces of communications gear that will be supplied by Racal-Milgo, Inc., of Miami, FL.

The system is designed to handle the pay records and transfer schedules of 400,000 Navy personnel. Martin-Marietta's award is part of a government-wide effort to update and upgrade aging computer systems. Reportedly, Martin-Marietta was the only company to meet the Navy's benchmark requirements.

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Off-line development package includes macro-assembler, microcode diagnostics, and a unique utility for automatic microcode optimization.

AP Run Time Executive Support Package (AREX)
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Applications Libraries
Extensive applications libraries include math, signal processing, and image processing.

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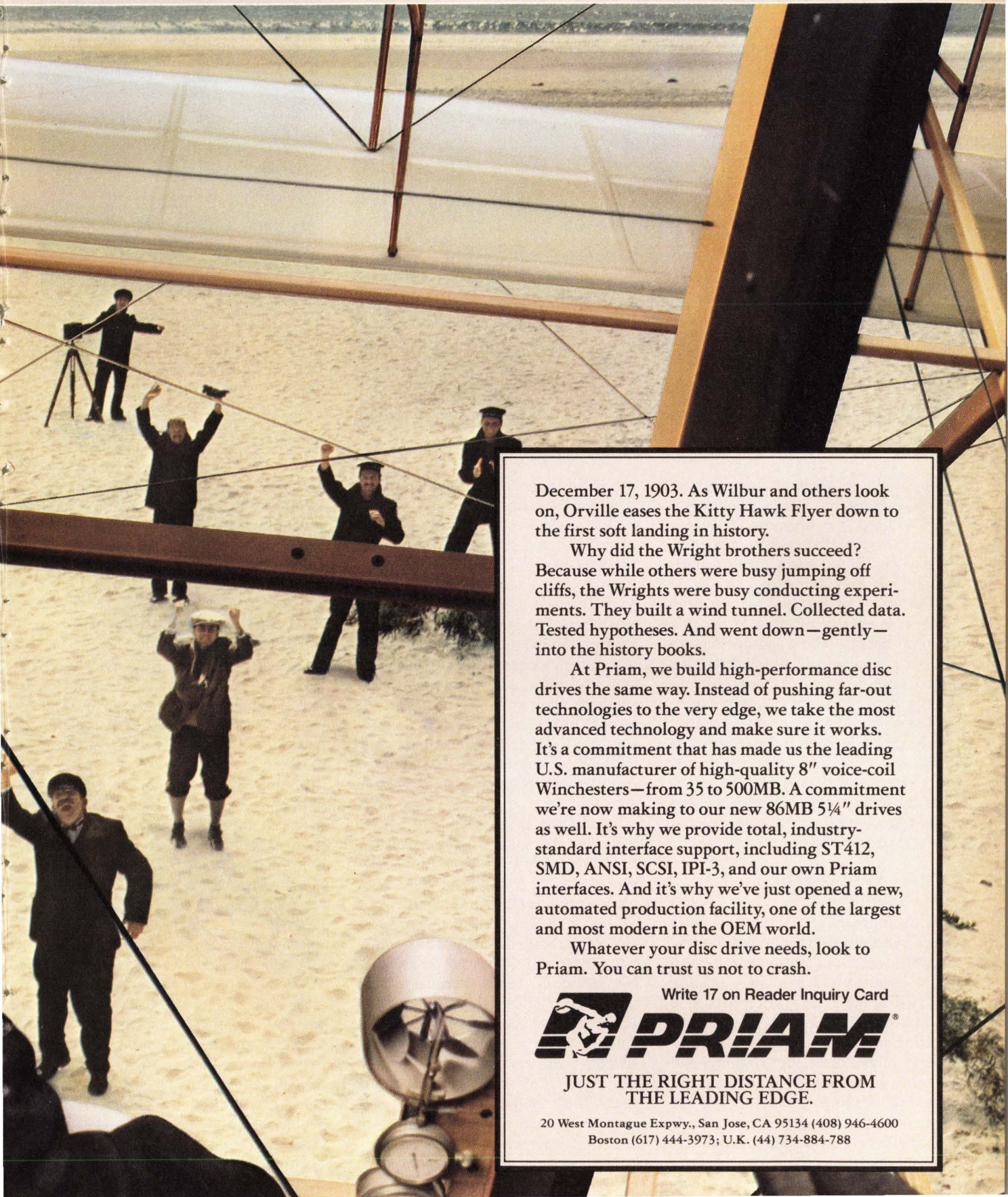

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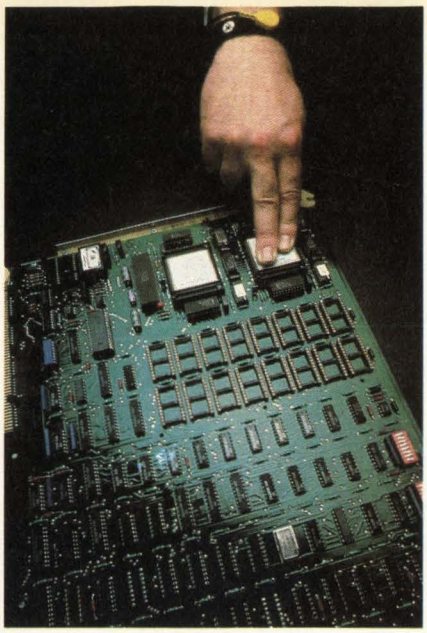
Bubble Memory Comes Out Of The Lab, Onto The Factory Floor



Above: Bubble memory chip on a processor board.

Left: The CLASSICMATE II system in an industrial environment.

Using a color graphics terminal as a man/machine interface in industrial applications enables the operator to achieve closer control of the process or manufacturing operation, thereby saving materials and labor and increasing efficiency. Nested levels of displays, ranging from general overview pictures to specific graphic details, allow the operator to view the process in detail and determine which level is critical at the moment.

As a manufacturer of man/machine interface systems for the industrial control marketplace, Industrial Data Terminals (IDT) has gained considerable experience in developing color graphics terminals for harsh industrial environments hostile to conventionally designed and built electronic equipment.

Coping With Harsh Environments

A color graphics system can encounter many potentially damaging environmental hazards while operating on a factory floor. Temperature extremes, ranging from 0°F to 120°F are possible in outside environments, such as steel mills and pipeline monitoring. Vibration (particularly in foundries, liquid sprays and aerosols, airborne dust, humidity, moisture, and electrical power outages are other potential dangers. These hazards can be disastrous to a color graphics terminal if it has not been specifically built to withstand them.

One of the most critical components of an industrial graphics system is the memory device. The terminal's memory must be rugged, fast and flexible, to serve a wide range of applications. These considerations led IDT to choose bubble memory for picture storage in its terminals. Bubble memory is an extremely rugged, read/write, non-volatile memory; a solid-state unit with no moving parts. It is much more durable than temperature-sensitive RAM and EPROM memories, and unlike RAM memory, data is not lost from bubble memory when the power goes off.

One of the chief benefits of bubble memory is the sheer volume of data that can be stored and its reliability as a storage device. The error rate for a 128K bubble memory device is low; chances of a user receiving an incorrect bit are 1 in 10^{15}. In real use, this translates roughly into one error in 100 years of normal bubble operation. Since potential system reliability in industrial applications was IDT's primary consideration, bubble memory became a very promising resource – and has been used for picture storage in IDT terminals for the past three years. The on-board bubble memory reduces the amount of data needed by IDT terminals, cuts data transmission time, and lowers power requirements for the terminal, thus increasing overall system reliability. All the host device really needs to do is send data on process variable changes, since the terminal can perform its own picture generation.

Storing Pictures in Bubble Memory

To store a picture in any memory type, IDT terminals actually store strings of ASCII character commands as a file. The terminal then interprets and executes these stored commands when the file is recalled.

Bubble memory, made on a chip of garnet, consists of small cylinders of magnetism. Each cylinder, or domain, is positive on one end and negative on the other, and is formed by a group of atoms in the garnet whose magnetic poles are aligned. Like the floppy disk, bubble memory uses a binary method to store information magnetically, with microscopically magnetized areas representing a 1 to the computer and unmagnetized areas representing a 0. The methods of communicating this information to a computer are vastly different, however. In disk storage, the information is magnetically embedded in disk and a mechanical head moved out to read it. With bubble memory, the magnetic domains (bubbles) are moved by a rotating electri-

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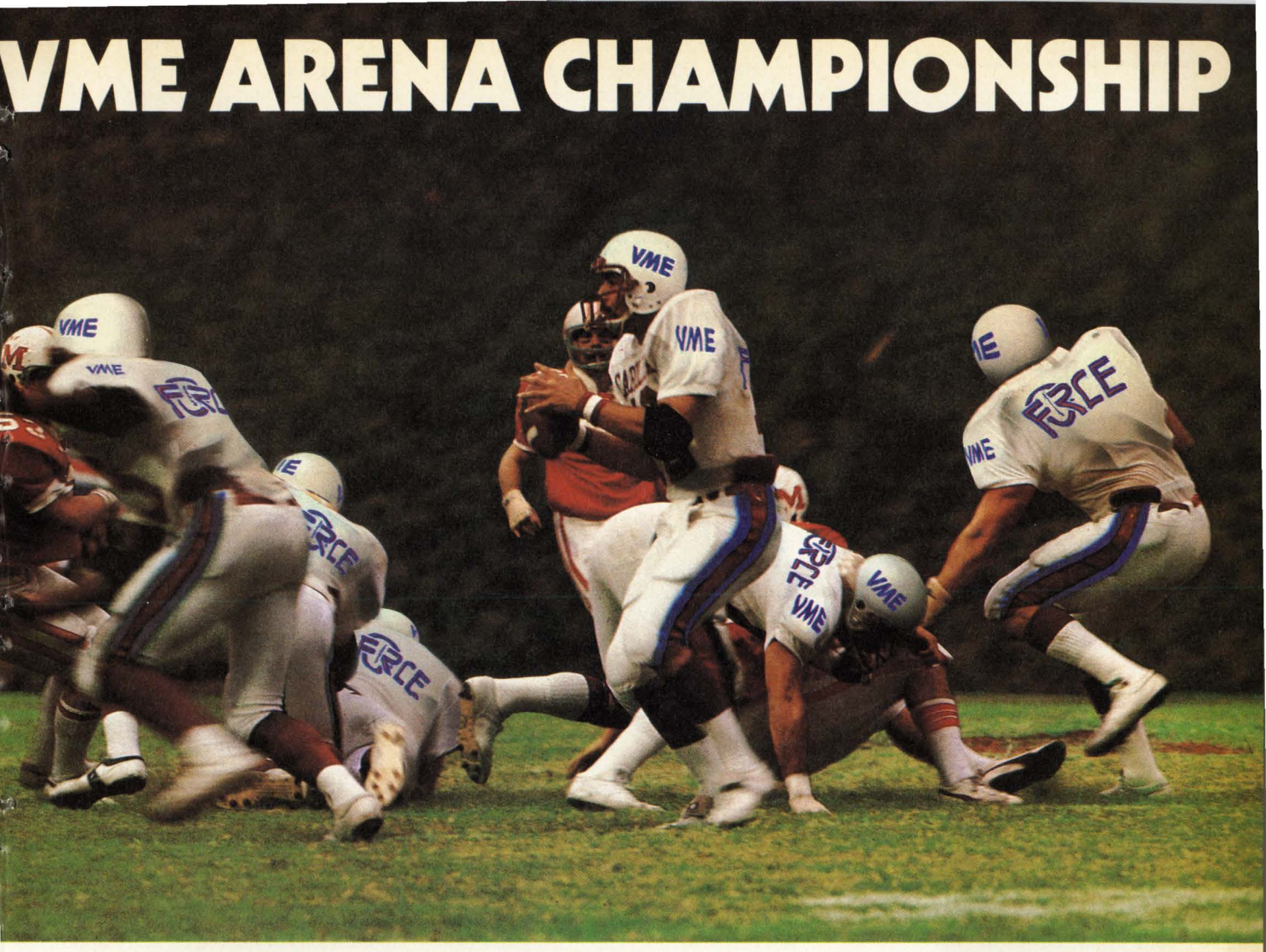

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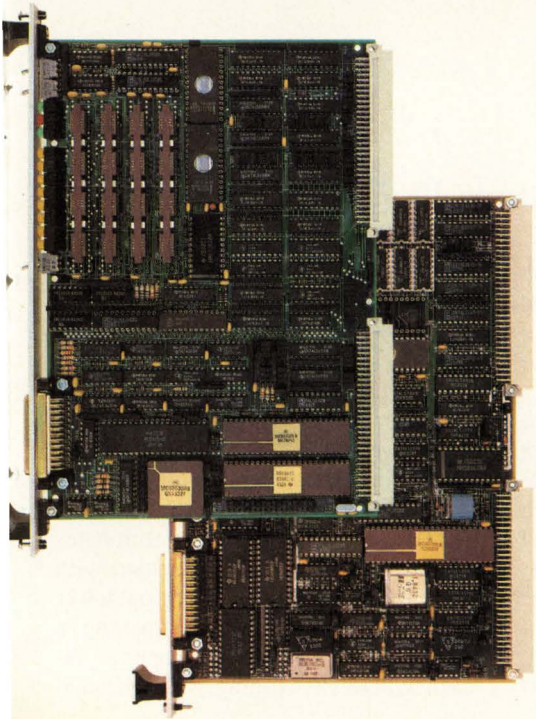

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cal field through the chip, like links in a chain, to a location where they can be read. The sequence of bubbles/no bubbles makes up the stored data.

Making Bubble "Look Like" A Disk

The development of a new IDT product, CLASSICMATE, presented challenges for both IDT engineers and bubble memory. CLASSICMATE represented a slight departure from IDT's product line, for it is a hardware and software color graphics package uniquely designed to provide a rugged industrial graphics system for programmable controllers. Initially, CLASSICMATE used bubble memory strictly for picture storage. The CP/M-80 based high-level language application software necessary for communication to programmable controllers was resident on a disk system. This was merely an intermediate solution, however, as disks were not suitable for industrial applications.

The challenge IDT engineers faced with bubble memory presented the task of structuring access to bubble memory so that high-level language software could be stored in and executed from the bubble – thus emulating a rotating disk medium with solid-state reliability. This would allow CLASSICMATE to use bubble memory instead of the rotating disks for communication to programmable controllers in harsh industrial environments. Operating Systems like CP/M are disk-based, or presume access to a disk-based system. In order to use bubble memory in place of a rotating disk device, its file structure has to be organized like a rotating disk. In order to allow bubble memory to be used for communication to PCs, IDT engineers needed to adapt the Basic I/O system (BIOS) to recognize and accept bubble as a memory resource, thus emulating a rotating disk system.

Over a six man-month period of time, IDT engineers customized BIOS and created a new processor board for the terminals, which contained an 8-bit microprocessor in addition to the bubble memories. The CP/M Operating System itself was installed within bubble memory. IDT engineers also had to locate a "generic" compiler for a particular high-level language, and make modifications for the bubble environment. The result for CLASSICMATE was that all picture storage takes place in bubble, and all CP/M-80 based application software for communication to programmable controllers also resides in a separate bubble. Thus, there is no need for disks or battery backup.

All picture development for CLASSICMATE now takes place on the IDT Mass Store Unit, which contains a 10 Mbyte, sealed Winchester hard disk drive, with a mini-floppy drive for file backup purposes. This Mass Store Unit is portable and can be used to support many IDT Online Systems during the initial picture development.

The CLASSICMATE Online System consists of three devices: a 19" high-resolution color monitor; a 105 key full-travel keyboard, and an IDT 220 Video Processor, which has total control of a matrix of 512 × 512 pixels (dots) on the monitor. Following the development stage, all animation and picture files are automatically transferred from the hard disk in the Graphics Development Package into the Video Processor's bubble memory – allowing both complex picture storage and communication to the programmable controllers without any type of rotating disk device.

New Uses For Bubble Memory

Recognizing the potential for bubble-based software running from CP/M, IDT expanded development efforts to CP/M-86. The resulting 16-bit microprocessor version of CP/M became another IDT product – the IPM-16 (Input Processing Module). The IPM-16 is a versatile single board microcomputer, designed for use within the IDT family of color graphics terminals. While the IPM-16 is running under CP/M-86, a user can write his own application programs, which can then also be stored in bubble memory.

IDT will continue to expand its line of bubble memory products and plans include potential applications for Intel's projected new 4 Mbit bubble memories. The possibilities for further industrial applications of bubble memory appear very promising.

Write 231

DEPARTMENTS/Systems

CMOS Dual Processor Eases Imbedded System Design

Imbedded computers generally provide real time control where multiple tasks may be performed and complex programming may be required. At the Electro '84 Conference and Exhibition, Mr. Gordon H. Smith of Rockwell International discussed a new concept of dual processors in a single chip aimed to simplify these applications and reduce both development and production costs.

The dual processor itself (**Figure 1**) is an enhanced version of the 6502 with ten additional instructions including hardware multiply. It contains 128 bytes of RAM, five 8-bit bidirectional input/output ports, one 8-bit output port, one 4-bit input port, two 16-bit counter timers and in the 65C00/21 version, 2048 bytes of ROM. The 65C29 version is identical except that it has no built-in ROM.

The dual processor behaves as if each processor is completely independent except that there are provisions for either processor to interrupt the other one. Each processor has its own set of reset and interrupt vectors, internal software accessible registers, and interrupt enable registers.

This arrangement simplifies programming and system design for applications that require the simultaneous control of two or more independent asynchronous control of two or more independent asynchronous processes. One CPU may control one process while the other controls the other one. Programming, either to interleave the control functions or to implement an interrupt driven system is simplified.

The use of the dual CPU eliminates many of the problems associated with establishing priorities, locking out lower priority options when performing a higher priority function and general concern with relative timing. Since the dual

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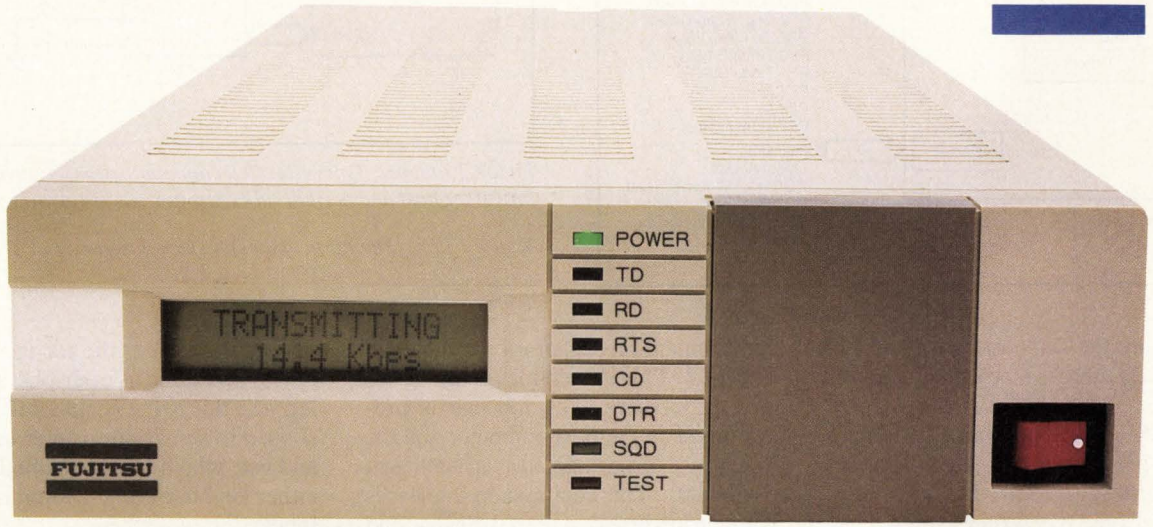

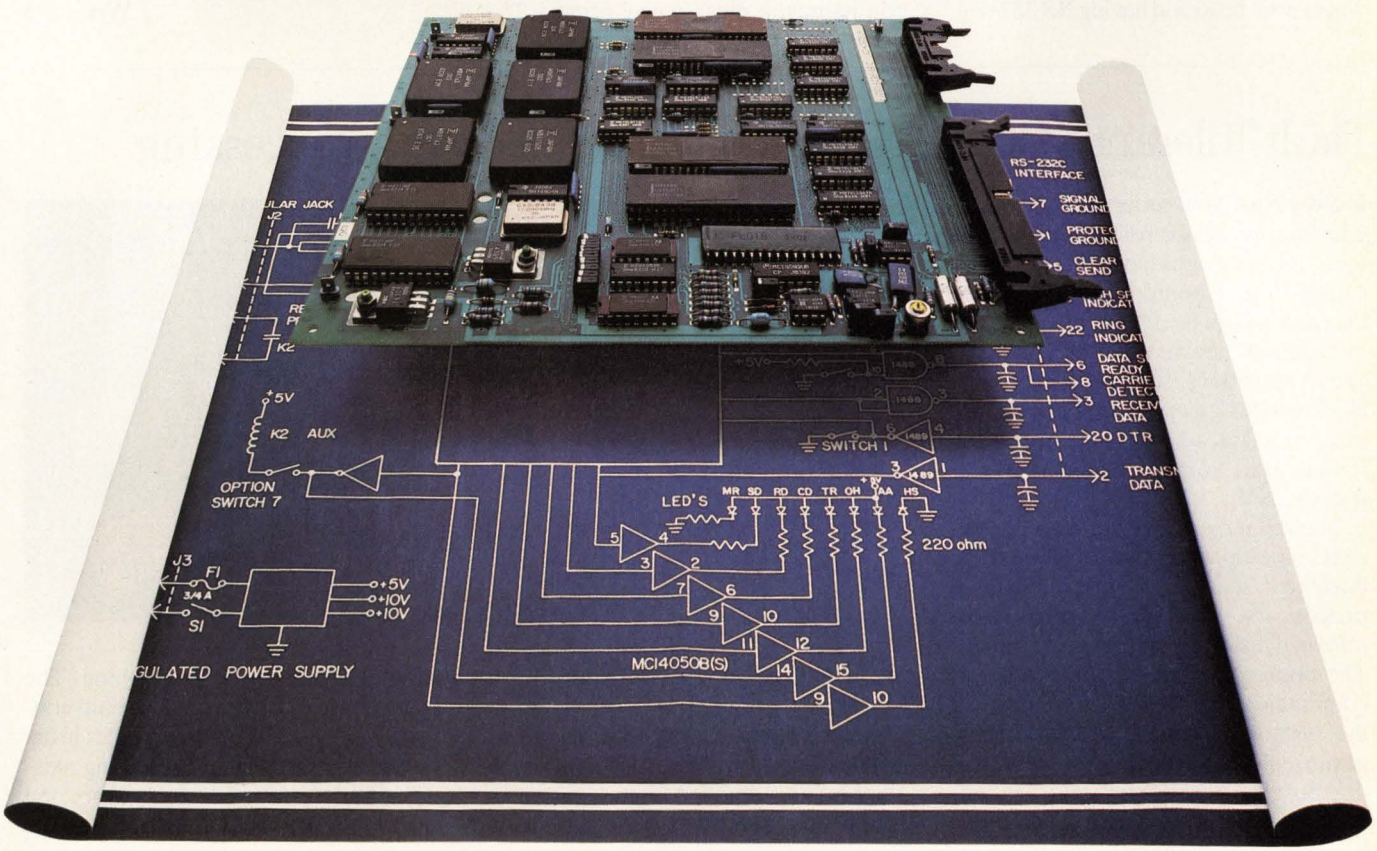

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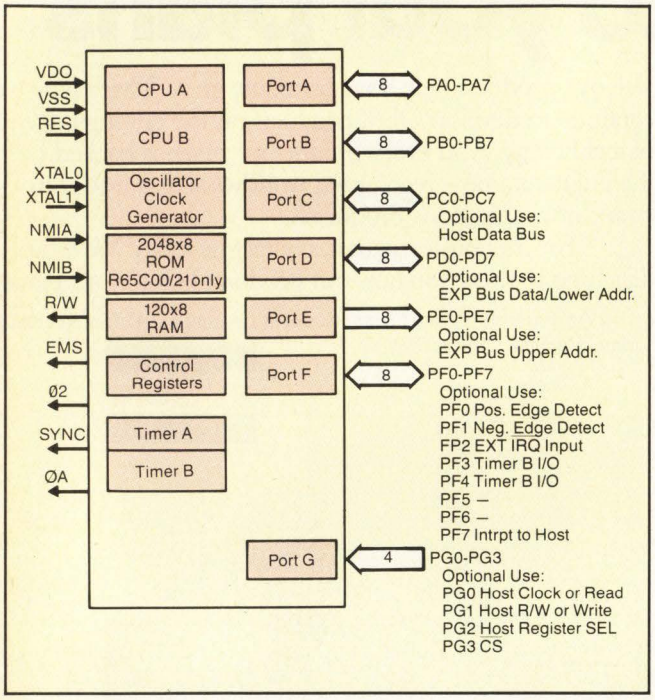


Figure 1 (left): Dual processor interface diagram.

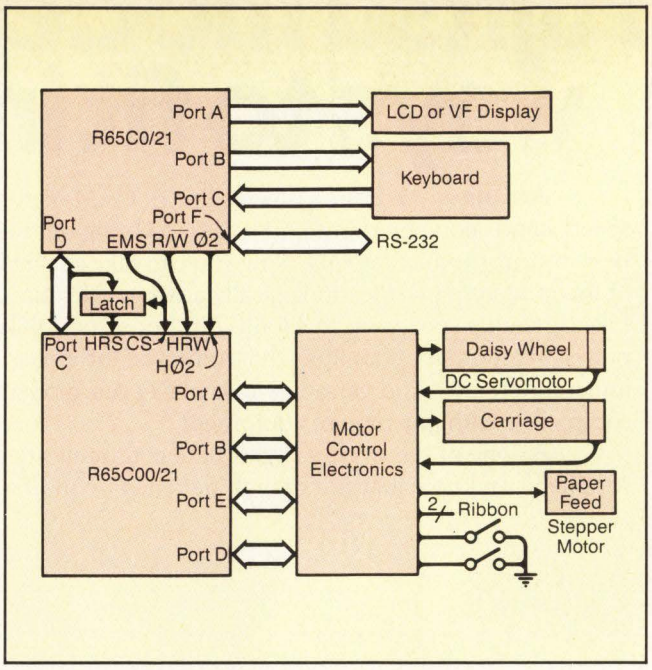


Figure 2 (above): Typewriter/Telecommunications system with dual processor host and peripheral controller.

CPUs share the same memory and I/O capabilities, there is no communications hardware required between the two processors. And since the dual CPUs share the same program memory, only one set of subroutines is required.

An electronic typewriter using a daisy wheel print head and having RS 232 telecommunications capability is shown in **Figure 2.** This system makes use of two dual processors. The top one is programmed as the host computer and the lower one is programmed as an intelligent peripheral. The host system interfaces with the keyboard, a digital display, and via its bus, a daisy wheel printer. The printer interface is the second dual processor operating as a peripheral controller. The bus to the peripheral controller is used to send both printer commands and text which has been obtained from either keyboard or telecommunications inputs.

– Wilson

Write 235

Fault-Tolerant Machine Handles Distributed Multiprocessing

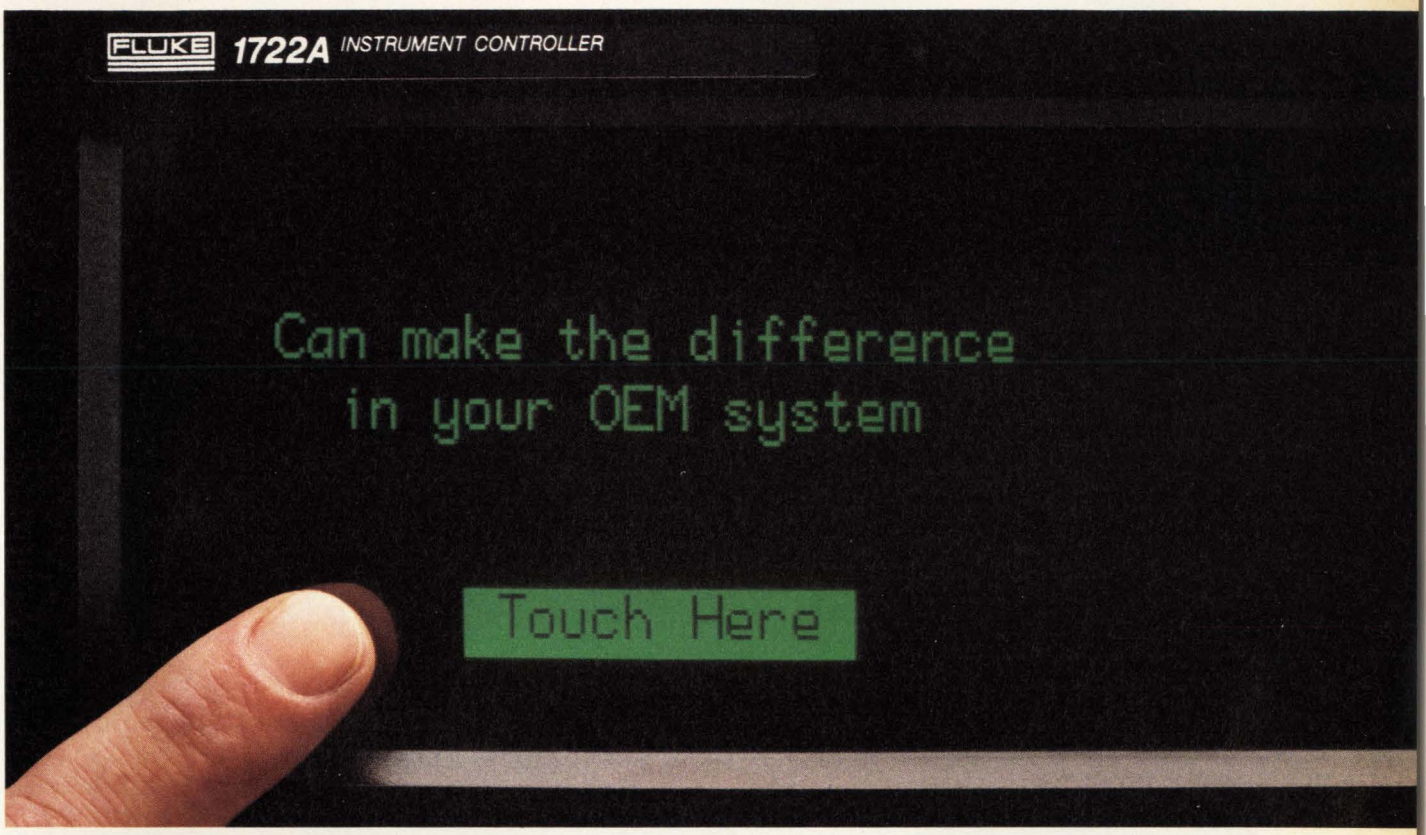
In order to get more performance from low-cost microprocessor-based computer systems, many designs have relied on dedicating a single board computer to each user and using a backplane bus as a communications network between the users and I/O functions, such as disk and tape. Now that design approach has been applied to a fault-tolerant machine – the Reliant from NoHalt Computers (Farmingdale, NY).

The Reliant fault-tolerant system uses a backplane bus as a communications network between users and I/O functions.

The Reliant's internal architecture consists of multiple application processors, dual high speed data buses, dual file processors, dual disk controllers, mirrored disks, and dual power supplies. The application processors handle all communications between the users and the system, while the file processors govern internal data transfer. The twin data buses, file processors and disk subsystems operate in parallel, performing real-time mirror images of each system operation.

Fault-tolerant operation is achieved on two levels by the computer. Level one is the System Activity Monitor, known as "SAM" and level two is the automated parallel operation of the machine. The System Activity Monitor Program constantly monitors all active modules in the system. By sending and receiving messages between the file processors and each of the application processors, the

Fingertip control



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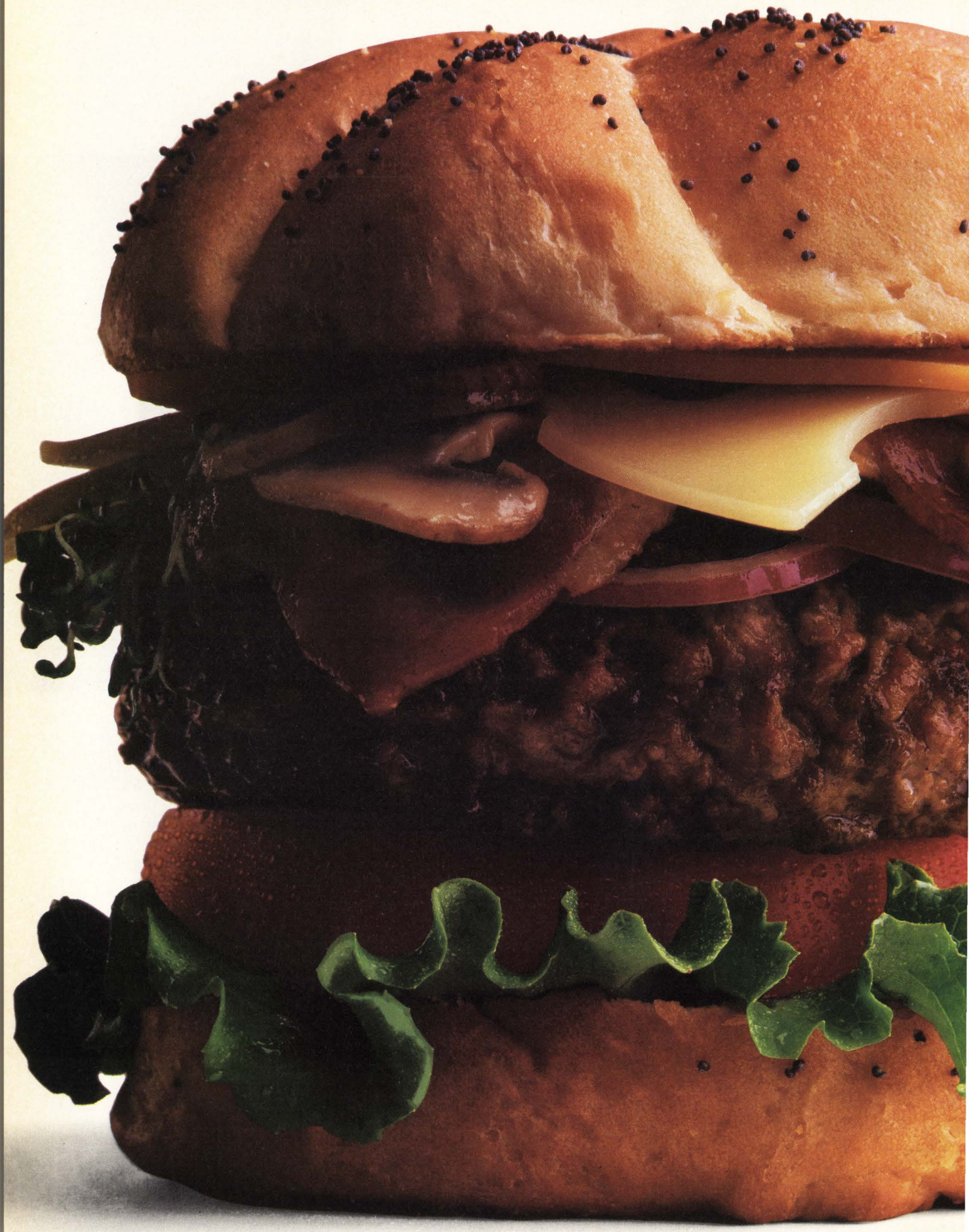

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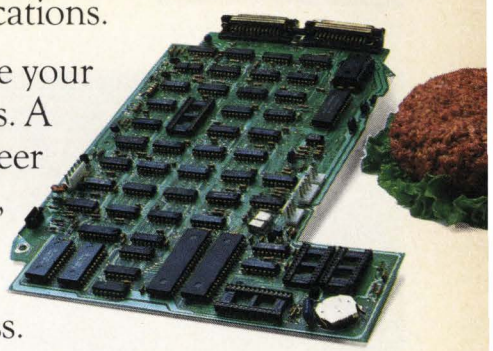

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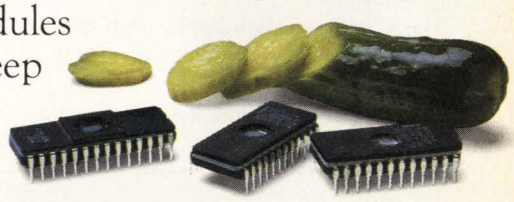

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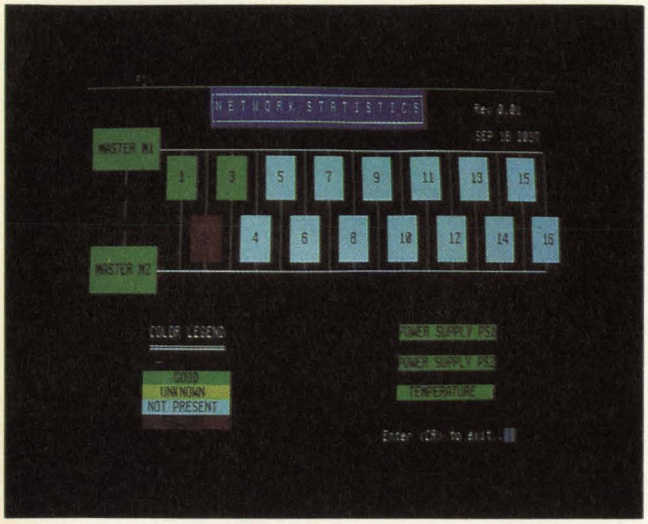

The file processors analyze messages from the application processors, determining the state of the system, and any special action required.

SAM determines if there are any faults and if any modules must be shut down to prevent corruption of data. This is accomplished by sending messages from the file processor to the application processor periodically during system operations. Each application processor receives these messages, checks the validity of these messages and records whether or not the associated file processor and its data bus is functional.

The results of each application processor's analysis is compiled and sent to each file processor. The file processors, upon receipt of the messages from all application processors, analyze them and determine the state of the system and any special action required.

For example, if one application processor fails such that data is written to one file processor and not another, then SAM shuts down the file processor that controls the disk.

If SAM fails to detect a message from an application processor or if the message is communicated incorrectly, then that application processor is removed from service. All files associated with that processor are closed and all locked records are released, and no other application processor is affected.

The parallel transfer of information between an application processor and both file processors is transparent to the application program. Each packet of information that is to be sent from an application processor to both file processors is duplicated in the mailbox. Both copies are compared and verified prior to release for transfer on the data buses. All information packets transmitted in the system have a CRC appended to them to guarantee the integrity of messages and data sent between modules. Failure of a module to receive a valid message (correct CRC) will cause the message to be disregarded, and SAM to remove that module from service. In the case of the file processors, records are unlocked and files closed for the application processor that has failed to communicate correctly.

The basic NoHalt Reliant configuration – a cabinet containing a single 16-bit application processor, mirrored system components with twin 20 Mbyte Winchester disk, NH DOS and utilities – costs $25,570 per system. A larger system for point-of-sale or other multiuser/multiprocessing tasks, with 16 application processors and 140 Mbytes disk storage, costs approximately $70,000 each. Optional add-on drives can double disk capacity to 280 Mbytes. – *Wilson*

Write 237

DEPARTMENTS/CAD

100% Autorouting For Manufacturable Board Designs

The increasing use of surface-mounted devices, chip carriers, ICs with multiple tracks between pads and manufacturing techniques that allow components on both sides of the board, have created board designs up to eight times as dense as older versions. Often these boards have irregular spacing. Automatic routing software for printed circuit board CAD systems, including 100% autorouters are now available. But to cope with very dense new designs, Racal-Redac (Westford, MA and Newtown, U.K.) have developed a proprietary algorithm to complement the VAX-based software for use with their range of CAD workstations. The 100% autorouter uses a gridless approach and new methods to achieve clean designs for fabrication.

Popular "Lee algorithm" autorouters that divide a board into cells according to a grid become extremely cumbersome with density increases. Though they are adequate for many boards, going to twice as fine a grid to route complex designs requires quadrupling the number of cells the routines must treat. This, of course, forces either increases in routing run time or limiting total board size.

Redac's gridless algorithm acts more as a human designer, viewing a picture and routing obstacles regardless of the spacing or units on the board. Finer tracking lines are allowed when needed, and operate in any increments necessary to route the design. The first pass connects up the board as completely as possible; errors will likely remain in complex designs. In subsequent routing iterations, the system goes back through to correct errors, changing routes completed on the first pass as needed to correct some errors.

Normal automatic routers also complete as many of the connections as possible on a first pass, come back and tell the designer how much it has completed. The designer must then either fix errors himself, interactively, or change

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the algorithm or parameters slightly for the portion remaining. Autoroute iterations work on only the connections not completed in the initial pass. For 100% automatic routing, the system must have enough intelligence to undo correct routes, fix errors and then determine a way to re-route around the correction.

The sophistication of the router requires that it be resident in a VAX to which any of the Redac Cadet or Maxi CAD workstations can be connected. Ian Yates of Redac estimates a minimum of about 1-1½ Mbytes of memory are needed for the autorouter, depending on the number of design stations and VAX model being supported.

Other 100% autorouting packages are available, but the effort to develop this system in-house was deemed worthwhile. Potential problems with buying a package from outside include manufacturing ease issues like interfaces and compatibility, support, and future development. In addition, Redac feel they have developed a technically superior router.

One element they feel is particularly strong is manufacturability of final board designs. The routine includes a final smoothing step that allows routes to be respaced and put on a grid, once the connections are complete. Since the original route uses no grid, any later interactive work on a design could prove difficult without the added grid and even spacing, and this clean-up step will leave designs cleaner for fabrication.

Though the router is not scheduled for shipment until October, initial 100% connections of customer-supplied designs are promising. A two-layer 35 IC equivalent board at 0.45 square inch per IC density was 100% routed in 42 minutes using eight mil signal tracks at 10 mil spacing. A larger two-layer board with surface-mounted components and 161 IC equivalents at a density of 0.35 square inches per IC at only 6 mil signal track and spacing was 100% automatically routed in less than a day. These feats of non-interactive PCB connection could account for much shorter design times for complex dense boards, and depend less on the skill of the designer using the CAD tools.

Still, the designer can stop the process as desired, or set grids, if needed. The package simply provides more complete routing capability without interaction, and increases ease of designing dense boards using two sides, surface mounts and special parts. As they point out, the 100% autorouter is an enhancement to Racal-Redac's current PCB design software system. As such, it may not be required by those designing relatively straightforward modules, but could vastly increase users' ability to incorporate new components and manufacture sophisticated printed circuit boards. Pricing of the router begins at $60,000. *—Pingry*

Write 234

DEPARTMENTS/Communications

802.3 Networking For Multibus UNIX Systems Integration

Designers using the Multibus have several options for networking. A new controller board to meet the IEEE 802.3 CSMA/CD specification and Xerox XNS protocol software are both specially tuned for use with the 68000 and UNIX. The NI 3210 Ethernet board from Interlan (Westford, MA) uses both a dual ported 8 Kbyte RAM and DMA (**Figure 1**). Its accompanying NS 4244/UNIX software has a device driver and XNS Internet Transport Protocols (ITP) for UNIX System V.

The addition of dual port memory combined with linked list buffer management is particularly powerful. With linked list buffering, short buffers can be used individually for short packets and chained together for storing longer packets. Since Ethernet frames can range from 64 to 1518 bytes long, with linked buffering, the 8 Kbytes of RAM can store many minimum size to several maximum size frames at once. Dual porting allows the host latency on incoming packets, so the CPU can determine where each will go in the Multibus system memory. The DMA offloads block moving of Ethernet packets between system memory and the dual ported memory.

Efficient memory and buffering on the network controller board is critical to system throughput, especially on CSMA/CD networks. If the flow of network packets becomes too fast for the host at the node to process, the CPU may drop some incoming packets. This is detected by the sending node, where the packet will be

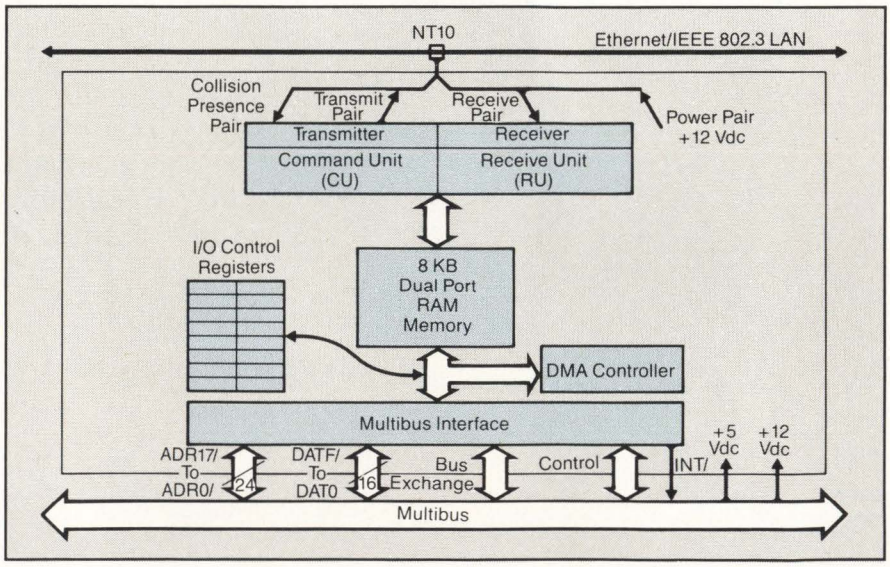

Figure 1: NI3210 functional block diagram illustrating command and receive units implemented with the Intel 80582 chip.

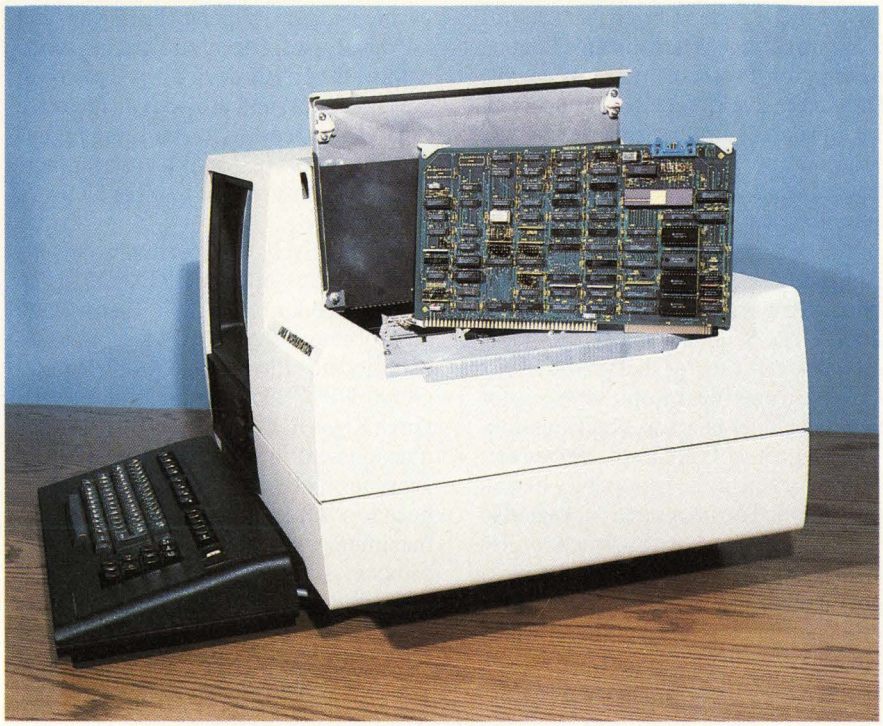

Figure 2: Interlan's NI3210 Multibus Ethernet Communications Controller.

re-transmitted until properly received. The overhead for errors, collisions and re-transmission can be cut back with adequate memory on the network controller.

Diagnostics on the board include two loopback modes, heartbeat detection and excess collision detection. Besides these basic functions, network service quality is monitored by transmit deference indication, collision counting, CRC, alignment and receive overrun error counting.

In tuning the board to a large OEM base, Interlan provides programmable byte-swapping so the Multibus can accommodate the format of a 68000 processor running XNS or TCP/IP network protocols. Otherwise, the host CPU would have to re-order bytes in every frame transmitted or received. Another feature added for use with the 68000 is 24-bit addressing.

The scarce Intel 80582 chip is used for Command and Receive Units (**Figure 1**), for transmitter turnaround of 9.6 microsec and even less for the receiver. Error detection is built into both functions, and the receiver is programmable to either save or discard faulty frames. A big advantage to using the chip is lower costs. The NI 3210 board costs $760 in quanti-

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ties of 100.

Network controller boards connected to transceivers and cable only provide the first two levels of the ISO OSI network model. For this board, Interlan has also developed a UNIX device driver and software for levels three (Network Layer) and four (Transport Layer) to the XNS ITP specs. Through third party agreements, higher level (closer to the user and application package) network software is available from Unisoft System (Berkeley, CA) and Network Research (Los Angeles, CA).

The Internet Transport Protocols written for UNIX System V are those Interlan has already developed under VMS in C, and the two types of systems can intercommunicate. This set of protocols is designed for either single-network or internetwork communication formatting.

The OSI Network or level three is called Internet Datagram Protocol (IDP) here, and there are five integrated packages at the transport layer that use this datagram service. These include Routing Information Protocol, which keeps the IDP's internetwork routing table updated; Error Protocol for reporting errors, with error numbers and parameters, Echo Protocol that verifies the existence and operation of a remote host and the communication path to it; and a Packet Exchange Protocol for request/reply in connectionless acknowledged communications. The Sequenced Packet Protocol is the powerful sector that provides virtual circuit and file transfer services, for successive internet packet transmission.

These protocols are implemented as a process, so the code is portable, like an application. The integrated package also includes a network management utility serving all of the levels through the package. Over 40 statistics from the network keep status checks on virtual circuit performance, flow control and congestion problems, and indicate buffering and overhead use. The entire package, including the UNIX device driver, starts at $200 per copy, and provides an interface to UNIX processes for building higher level protocols on, or as a base for, kernal protocols through Unisoft or Network Research.

This relatively low cost hardware/software package allows UNIX OEMs to provide standard IEEE 802.3 networking on Multibus systems. Byte-swapping accommodates the protocol ordering of a 68000 CPU. The combination of dual port 8 Kbyte RAM using linked list buffer management and DMA is designed to keep network error and collision overhead low while offloading the CPU, for maximum network throughput. Network protocol software designed for UNIX eases integration. — *Pingry*

Write 233

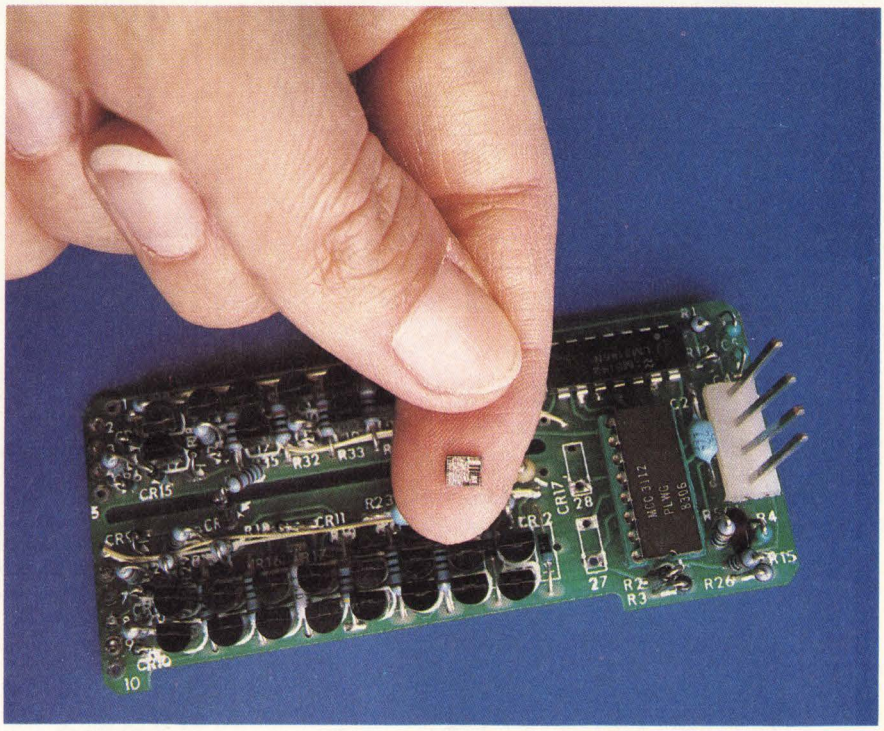
DEPARTMENTS/ICs

Chip Combines Logic With Output Power

A process designed to fabricate monolithic 500 volt junction-isolated High Voltage Integrated Circuits (HVICs) which use both bipolar and MOS technology in their fabrication was recently introduced by General Electric Co. The new technology puts on a single chip many functions now performed by discrete devices, logic circuitry and relays. Because it couples logic with drivers and high voltage output devices on one chip, improvements in cost, size and reliability are possible.

With the new HVIC, designers can fabricate unlatchable CMOS logic circuits, rated up to 20 volts, that operate properly and safely in noisy environments. Circuits can also be designed using other logic families such as NMOS, PMOS, MOS, TTL, RTL and ECL.

GE's goal was to develop a generic IC technology that addresses the most frequent circuit design needs found in power systems. Several functions require some logic capability the extent of which is highly application oriented. For those necessitating small to moderate amounts



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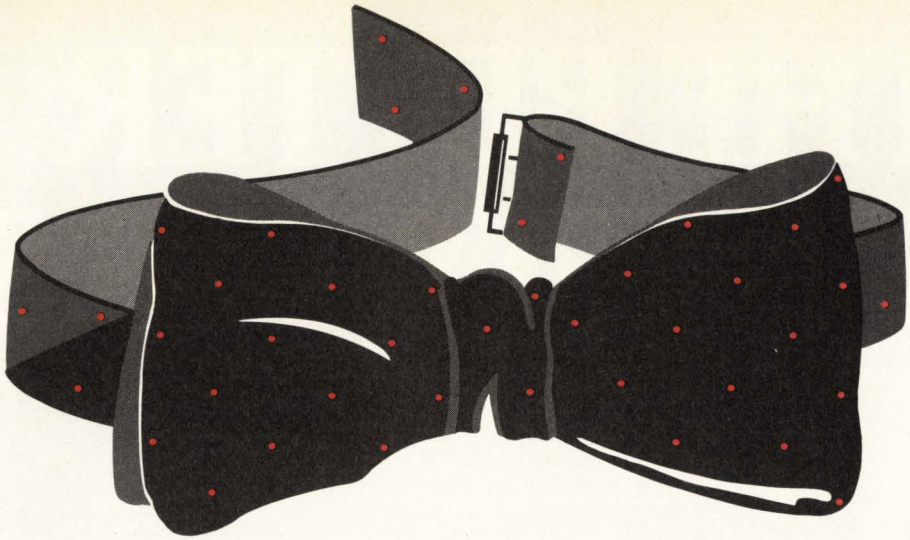

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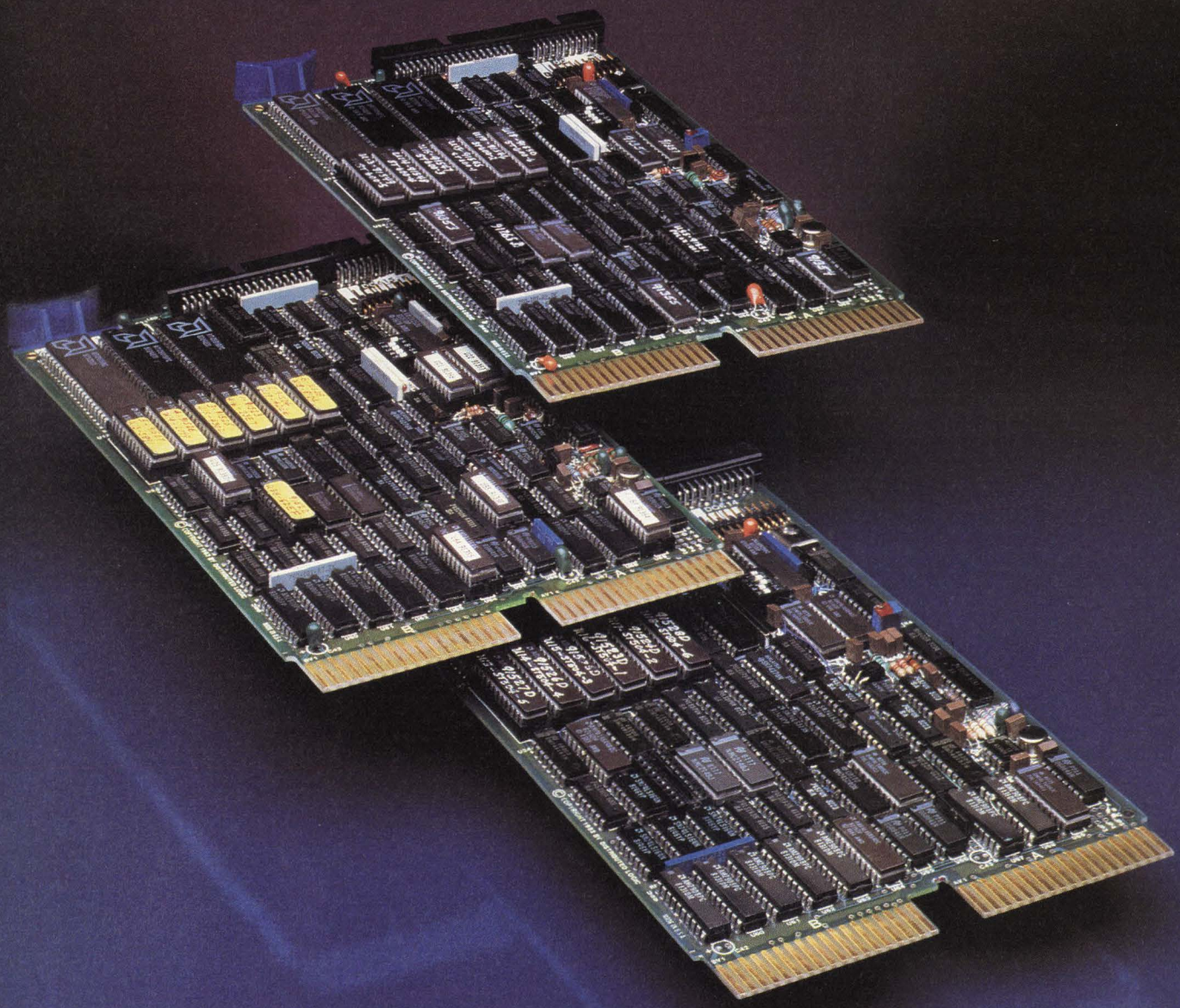

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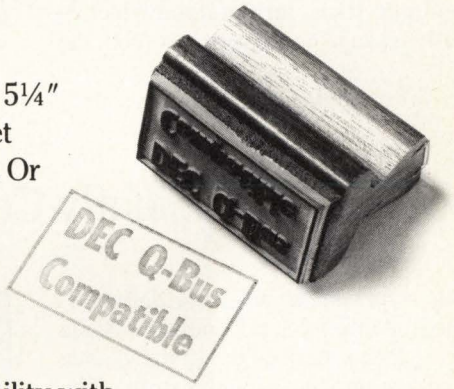

First, these controllers interface over 30 popular 5¼" drives. More 5¼" drive compatibility than you can get from any other independent controller manufacturer. Or from DEC.

At one end of the spectrum is the Model DQ615, that's RK06/07 compatible. It offers formatted drive capacities to 222.4-MB with two ST506 drives. Along with a maximum of eight logical units—two physical.

Next, the Model DQ614 offers RL01/02 compatibility with drive capacities to 41.6-MB for ST506 drives. It handles four logical units maximum—two physical.

Both these controllers offer DILOG's Universal Formatting™ that lets you mix or match drives, regardless of heads, parameters, capacity, etc. Or you can expand by simply unplugging one drive and plugging in another.

The third controller, The Model DQ634, is RL01 compatible with one fixed and removable 5¼" drive, such as DMA, and one ST412 drive. Formatted capacity is 20.8-MB.

All three controllers offer 22-bit addressing, enhanced 32-bit ECC and compatibility with RT-11, RSX-11, RSTS and TSX-11Plus.

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of digital control logic, it becomes attractive to implement the logic on the same chip where drivers and output devices reside. This lowers packaging costs, reduces function size and enhances overall reliability. A major factor in GE's selection of CMOS to handle these digital functions is its high noise immunity which roughly equals half of the bias supply voltage. This is desirable in power systems where the amount of noise generated is substantial.

A further attribute of CMOS is its negligible static current drain which is totally leakage dominated. As such, the power drain associated with the digital logic is very small and to first order scales linearly with the input frequency to which the logic is subjected.

A notorious problem with CMOS, is the relative ease with which it can latch-up. Such a failure mode is even more likely in the kind of environment GE is considering; therefore an important process requirement is the availability of latch-proof CMOS.

The HVIC drivers can deliver up to 2 amps peak, and can drive power devices such as bipolars, MOSFETS, Insulated Gate Transistors, SCR triggers and TRIACS. It can be used as a plasma display driver; in switching power supplies; for single bus wiring and in such applications as motor controls, robotic vision, welding, lighting, avionics, automobiles, major appliances, and in numerical and programmable controls.

Analog functions possible with the HVIC include timers, regulators, op amps, oscillators, comparators, temperature sensors and many other types of status and supervisory circuits.

The HVIC process was developed at General Electric's corporate Research and Development Center (Schenectady, NY) and will be used by its Power Electronics Semiconductor Department (Auburn, NY) to build and market a variety of devices.

– Hanrahan
Write 241

Chip Sets Efficiently Control Small Hard Disk Drives

With much fanfare and several design advances, National Semiconductor (Santa Clara, CA) produced the first disk data separator chip, the 8460 this spring. The 8460 is one of a four-chip set aimed at very sophisticated control of hard disk drives. Two of the four chips are already available.

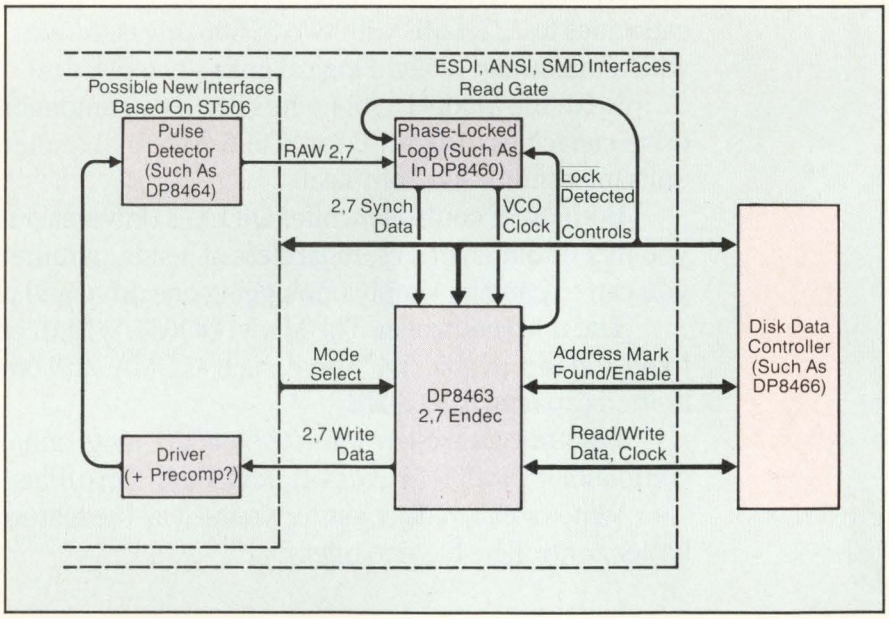
Western Digital (Irvine, CA) has long offered a disk controller chip, with several updated versions, and has plans to introduce a data separator chip later in the year. Adaptec (Milpitas, CA) has had a three chip set, developed through work on their controller boards, available for over a year. They are also scheduled to announce a separator chip before year's end to round out the set. Signetics and Advanced Micro Devices (both of Sunnyvale, CA) have two-chip sets due out before the end of the year, as well.

The drive for chip sets begins with the orders of magnitude increases in the amount of data now being put on 5¼" form factor drives. Discreet components for drive control can be squeezed into that size only with great difficulty. Interfaces like the ESDI (Enhanced Small Disk Interface) put data separation into the drive rather than the controller. Single drive control may migrate into the drive with several interfaces.

Each manufacturer has a different approach incorporating various functions, and which set will be best for a given design depends on many factors. One feature to be considered is data rate. Most of the 5¼" and 8" systems for which the space savings of a chip set are critical now operate at 5 Mbits/sec. All of the chip sets are optimized for at least this. National, Adaptec and Signetics offer rates up to 10 Mbits/sec, for SMD and ESDI higher performance interfaces and drives. National's specs promise a 15 MHz operation with the 8640 data separator. They are shooting at 1-25 Mbits/sec to accommodate 14", vertically recorded or optical disk drives.

The other chip already offered by National is the DP8464 Pulse Detector, a chip that always is built into the drive. It uses a comparator approach to sensing the peaks of the drive's amplifier signal. They suggest that this is better suited to plated media, thin form heads, vertical recording and run length limited coding (RLLC) than older methods. The other manufacturers do not include this device in the drive control chip set, as it really is part of the drive.

The next step in drive control is the separation of serial NRZ data from clock. This involved a voltage controller oscillator (VCO) and phase locked loop



Controller system block diagram using National's four-chip set for 2,7 RLLC encoded (DP8463 2,9 Endec chip) Winchester disk drives.

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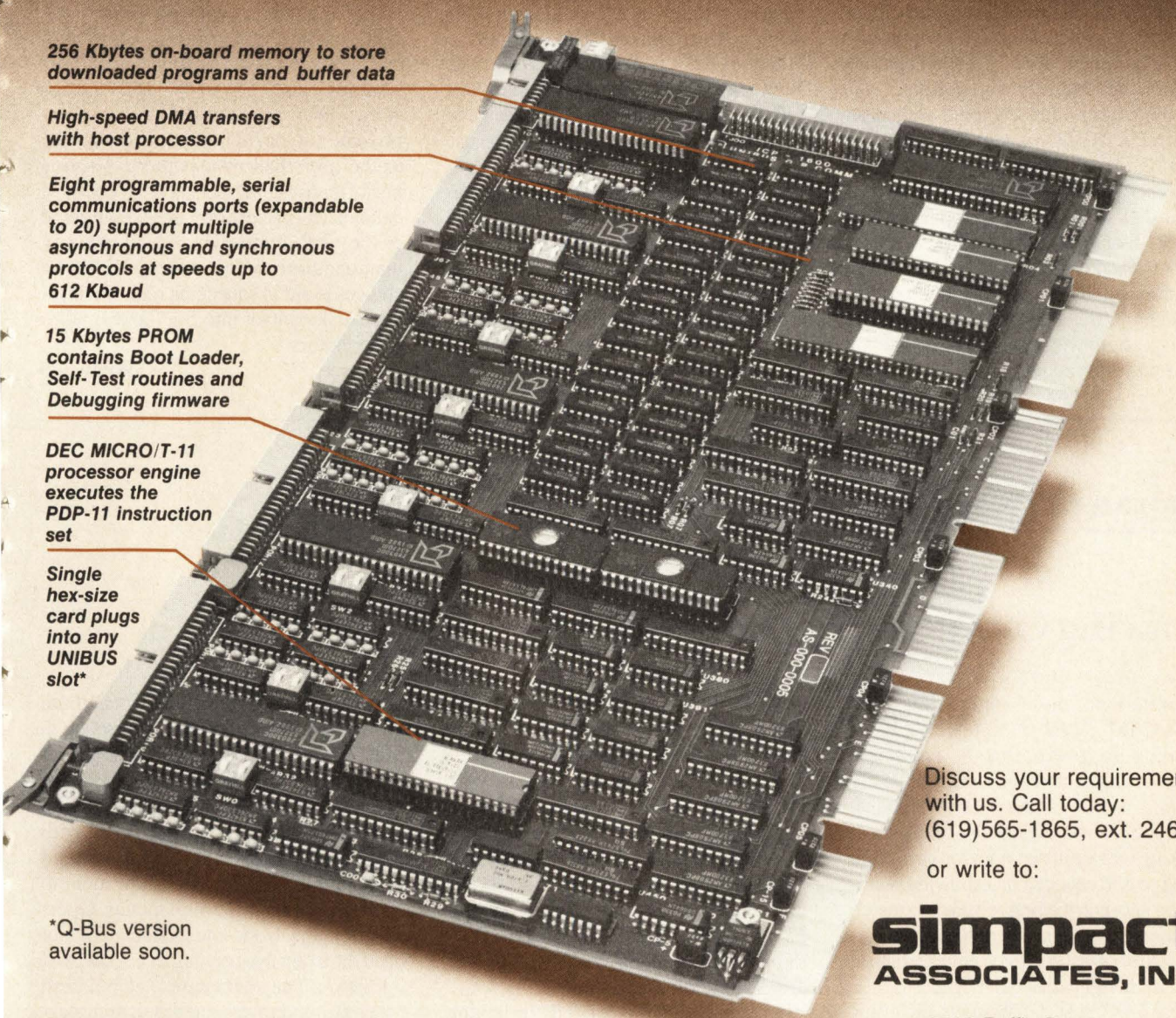

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(PLL). Though only National's is available, specs for Western Digital's 1011 separator show it at 4.34 or 5 Mbits/sec. Signetics' SCB 68459 Disk PLL spec sheet claims it includes the VCO, as well.

The National 8460 separator is very comprehensive, with three versions for varying pulse gates. The −2, at 2ns can accommodate very high data rates off the drive and contributes little error in the process. (A classic problem with data separation circuitry is that it adds errors in the process.) Versions at 4 and 8 ns are adequate for most 5 and 10 Mbits/sec rates. PLL filtering is off-chip, for user configurability.

Once the data is separated out, it must be decoded – or encoded, in the opposite direction. Most disk schemes have used MFM encoding, but RLLC is allowing up to 50% more data to be packed onto a disk with no added density. It's important, then, that these "endecs" are a separate chip to allow choice or upgrading.

Both Adaptec and National are working on 2,7 RLLC endecs for late year introduction. An MFM endec to translate and synchronize with the address marks on the disk is the AIC 250 from Adaptec, but for all of its advantages, 2,7 encoding has not yet taken great hold because of the complexity of the code and circuitry needed to translate it. These monolithic devices could well open up that code for more widespread use.

At the center of any chip set for drive control is the disk controller chip. Adaptec's AIC 100 10 MHz chip has been out for some time. The other contenders in the market are also planning controller chips at 10 MHz. Western Digital is the only exception, with a 5 MHz chip, that is also the only one without ECC. WD plans a separate Buffer Manager/ECC device.

Error control is always critical in disk drive use. These controller chips include sophisticated ECC to accommodate the higher performance drives now being produced. National boasts 32-bit and 48-bit ECC, programmable by the user. Computer Generated Codes' popularity has made the programmability useful; Mike Evans of National says that they have found that every drive OEM is using a different code. Signetics similarly has two levels of polynomial complexity for their ECC, 32-bit and 40-bit.

National calls their DP8466 a Disk Data Controller, as it "doesn't control the drive control signals," but the data. In other words, it is not interface-specific. Both chip and ECC are programmable, for use with floppies or Winchesters. This makes it a flexible chip, but its use requires more design work to accommodate the interface. AMD, for one, has voiced plans to include ST 506 or ST 412 control on their controller chip.

Both the Signetics and the National controller chips include DMA control. On-chip DMA control is as much as five times as fast as external circuitry. National has included a 32-byte FIFO buffer with two 16-bit DMA channels. The on-chip FIFO permits buffering of constant data off the disk with bursty output to the host. The two channels can either be used in serial for 32 bits, or as a local channel for controller to buffer and a remote channel between buffer and host.

As great as on-chip buffering may be, some contend that 32 bytes affords too little cushion for long sectors off a disk. Adaptec adds a buffer of up to 64,000 bytes to round out their control set. Two static RAMs become a dual-port buffer, for reading to a host and from a disk simultaneously. This buffering scheme permits them top handle non-interleaved (1:1 interleaved) disk formatting. Western Digital's 1014 will include up to 32K of buffer plus their 32- or 56-bit polynomial ECC.

The differences in number of chips, what functions are integrated and onto which chip draw clear definitions of different manufacturers' approaches. National is the first out with the most difficult of the chips, the separator. They claim that the sensitive phase lock loop sections caused about 95% of the design work. They are taking a high-end approach, but leaving more programming to the user than many others. Varying performances and specs will no doubt be balanced by price differences. By the end of the year, controller – and drive – manufacturers will have several chip set choices to aid in squeezing high performance disk control into 5¼" and smaller form factors. *– Pingry*

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DEPARTMENTS/Peripherals

Drawing Conversion System Will Create CAD Databases

Accurate input of design drawings into CAD/CAM systems is possible with scanning digitizers. But the notational data, such as dimensions and text on the drawing, is only captured. It is not understood and associated with the geometrical markings. In addition, notations are often added-to and changed on a drawing, without the geometry being redrawn to match it. This process creates a coherent, accurate picture of what is to be entered before the real design work can begin.

Creating CAD databases is the company motto and product capability goal at Metagraphics Inc. (Woburn, MA). They have begun to demonstrate a prototype drawing conversion system that uses a relational database as the software core for a CAD/CAM front-end, combining scanning digitizing, automatic character recognition and intelligence. It associates notational data of mechanical CAD drawings with vector and pixel geometry. Even the prototype has provided a five-to-one improvement in efficiency over direct input on a CAD system.

As a CAD/CAM front-end, the linking association of all markings on an engineering drawing is critical to accurate design data entry. This new approach to input takes much of the margin for error out of using existing drawings as a base for CAD work. The Metagraphics 2100 screen display is object-oriented, with icons accompanying text in stacked branching menus for easy movement to functions on any of several menus. Operation of this front-end system will not need the extensive training of CAD/CAM operators. The system uses symbols and terms familiar to designers and draughtspeople, and most data is input without

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operator interaction except for verification. Vocational school students are acting as operators in early tests of the system. A one-week training session will be offered to teach effective, efficient operation and full productivity should follow a week or two later. The interface is simple enough that some work can be done with no training.

The hardware base is Apollo (Chelmsford, MA), with their newest tilt and swivel screen and graphics processor attached to a large worksurface. A scan station with scanning digitizer to accommodate E size drawings and/or an aperture card scanner, monitor, communications and I/O, also incorporates an interface for output to the CAD system. The paper scanner is large, so the paper does not move, and the head consists of a single 4000-element CCD array, increasing reliability.

Several edit stations with similar color monitor, mouse/tablet or other input device, computer and mass storage may be attached to each scan station. Add-on modules of the same size and appearance as the processing box are available to add memory or other cards to both scan and edit stations.

The process involves first scanning either aperture cards or a drawing; the pixel representation scan file captures both geometry and notational markings. With a rough manual tracing, geometry is fixed, and the dimensions and associations from the system's knowledge base rectify even the crudest tracing of the part itself. The relational database cleans up vector information by notational override, often resulting in an improvement in the accuracy of design data.

Thus information automatically input with meaning can be verified on the monitor and then edited. Complete accurate parts definitions are output as IGES information. This spring, IGES was produced for a Computervision system; packages will be initially available for IBM, Calma, Applicon or Integraph front-end compatibility.

The automatic optical character recognition developed for the system can decipher machine or hand-written notations. Unlike most character recognition methods that match patterns, reading depends on attribute recognition. This allows a broader range of text to be read accurately and users can verify the capture.

Metagraphics has combined several advanced "fifth generation" approaches for a complete front-end to CAD/CAM. The icon/menu human interface with a language to match that of system users, automatic character recognition and "intelligence" in the associativity of the relational database software, along with at least one computer per user, provides efficiency and accuracy for even unskilled operators. Desktop-style display format with drawers and movable menu pads, along with the system's knowledge of what it needs to completely represent the design, are all carefully thought out.

Accurately inputting designs from aperture cards or engineering drawings has been a time-consuming chore for CAD users. If Arthur D. Little's estimates are accurate, about 40% of mechanical parts to be designed exist, and 40% can be modified from existing drawings, making this drawing conversion capability especially critical.

Systems are scheduled for delivery in the fourth quarter, with benchmarks underway now. Though initial configurations and beta sites are for front-ending mechanical CAD, the modular software will allow other applications to be written for the same basic system.

—Pingry
Write 240

Tape Backup Standards Proposals Stream Into ANSI

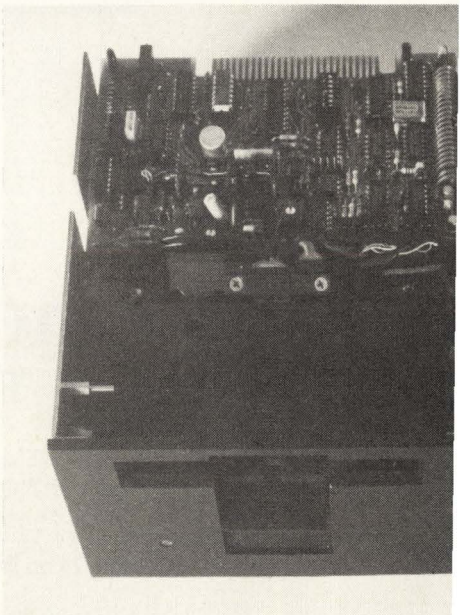
In a move indicative of the migration toward early standards setting, a group of tape and tape drive manufacturers has formed D/CAS, the Working Group for Data Cassette Drive Compatibility. Several proposals agreed on by the group are now under consideration by ANSI for data cassette Winchester backup standards. The documents suggest an intelligent QIC-24 compatible interface, a four-track recording format for 10 and 20 Mbytes per cassette and specs for unrecorded 0.150″ media. Another meeting was held to work out a basic-level drive interface proposal.

The D/CAS-5 intelligent interface proposal calls for QIC-24 compatibility. All drives made to the standard would be not only interchangeable with each other, but can plug into existing QIC-24 controllers. That interface is well suited to ¼″ tape, and was chosen as an existing standard to help this new product class get started.

The group's goal is "to promote widespread use of data cassette cartridge tape drives through the development of proposed standards that will encourage industry-wide compatibility." The initial proposals are for a 5¼″ form factor drive, since that is now the strongest market for Winchesters.

Ray Freeman of Freeman Associates (Santa Barbara, CA) suggests that this effort is really to establish a product type which can migrate to 3½″ size when the market for disk drives in that form factor is large enough to support a good backup tape business. The cassette probably will not be a serious competitor in the 5¼″ market where existing products serve well. But if a standard is set before the smaller market opens up, the product class could flourish.

A 3½″ tape drive to the standard would use the same controller, circuits and connector as the 5¼″ version, but LSI will be needed to shrink the electronics. There are several design challenges to producing the 3½″ form factor drive, but there



Tape drives to the D/CAS standards, like the Memtec Companion 500 Series, fit into a standard 5¼″ form factor and hold 10 or 20 Mbytes.

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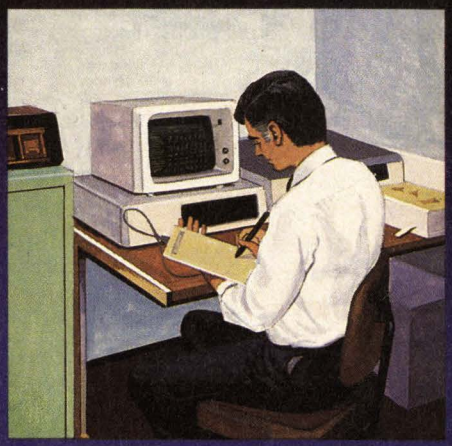

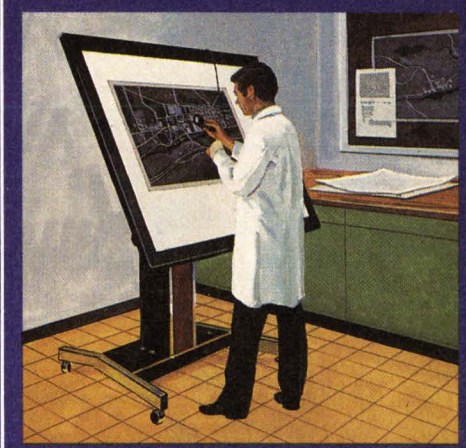

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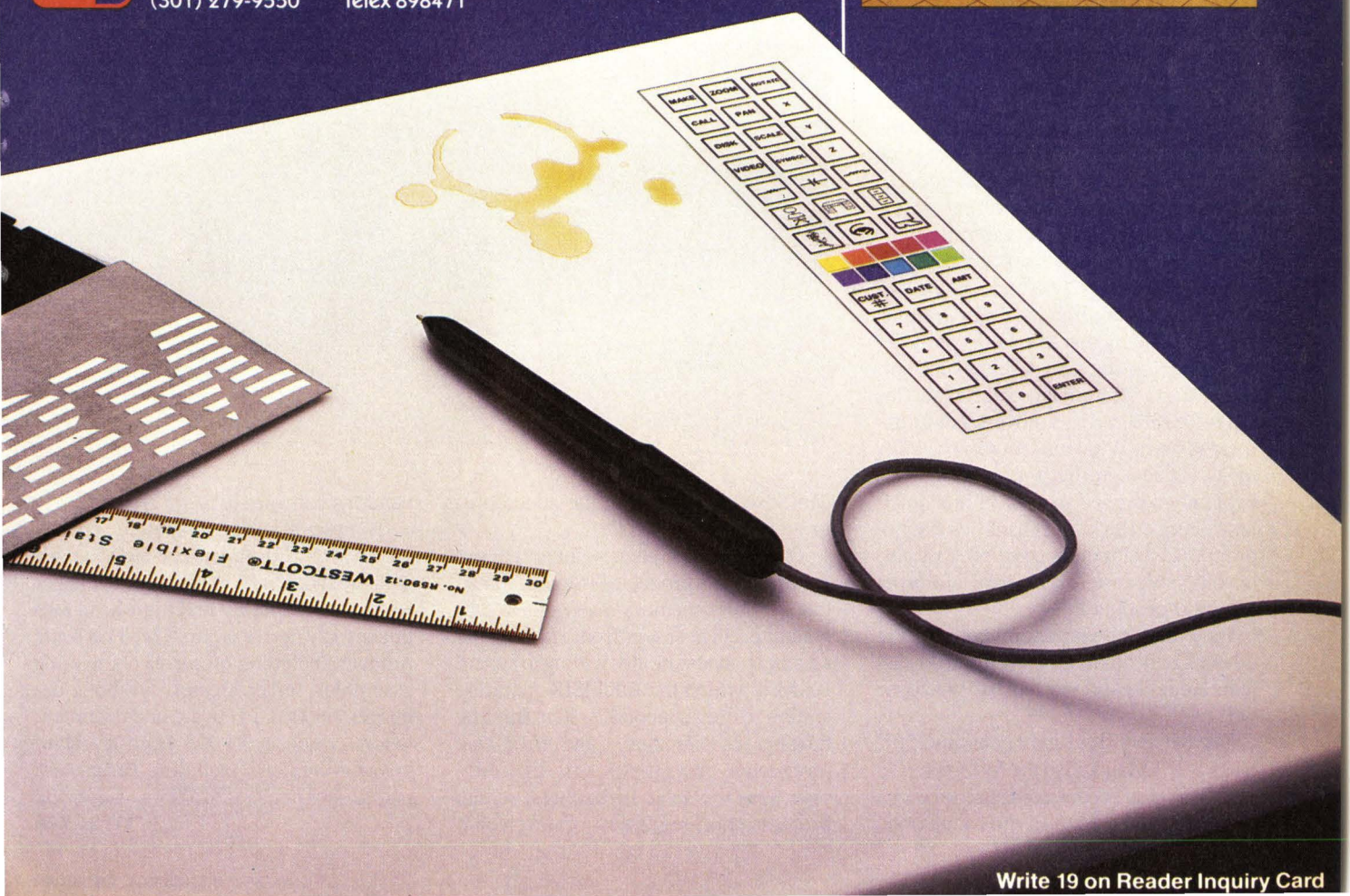


Write 19 on Reader Inquiry Card

is little doubt that the problems are being actively solved in the labs of several companies.

Another future goal for these backup cassettes is a standard at 40 Mbytes. The current recording proposal calls for 10,000 flux transitions per inch (ftpi) for the 20 Mbytes cassettes. The 6,400 ftpi used for the 10 Mbyte capacity could likely support even more data per cassette.

Members of D/CAS include Memtec (Salem, NH), Raymond Engineering (Middletown, CT), TEAC (Tokyo, Japan) and Verbatim (Sunnyvale, CA); several other companies have observed at the meetings. Memtec and Raymond, under license, offer full and half-high drives and TEAC, a half-height. Verbatim, as a media manufacturer, is responding to their needs. Such a grouping of companies formulating standards before the product type is truly active is a switch for the industry.

Current ½" tape cartridge working collaboratives include DEC (Hudson, NH) and 3M (St. Paul, MN). Each has submitted a proposal to ANSI for a 20 to 200 Mbyte CompacTape and recording format. Memorex (Santa Clara, CA) has licensed Electronic Processors' (Englewood, CO) ½" format even before the drive has hit the market. EPI suggests that several other large agreements will make them an even stronger force around which to standardize. These ½" tapes are of much higher capacity than the D/CAS proposal.

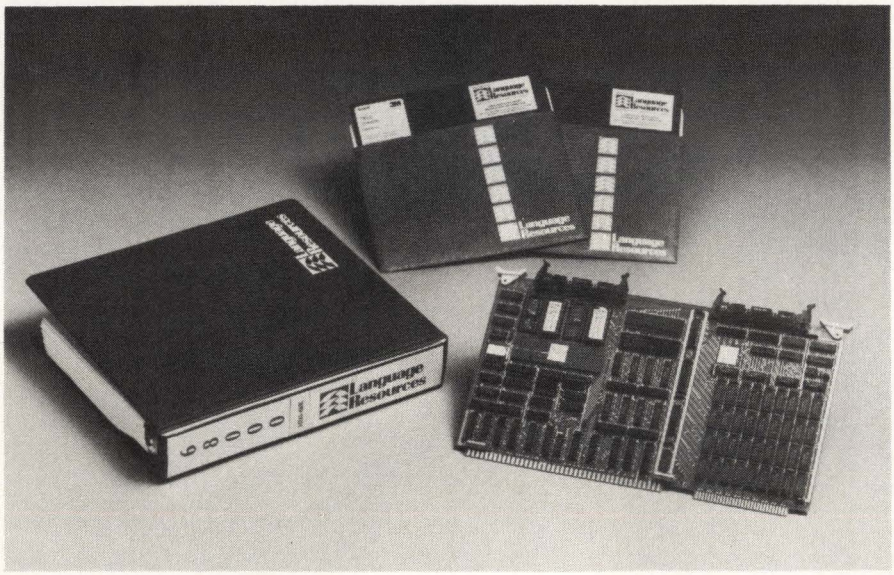
The two types of tape products will serve different markets, and for the high-end, the decision to go to a ½" format avoids pushing the limits of ¼" tape.

Write 242

DEPARTMENTS/Boards

Insertable Board Expands Development System For M68000 Use

The MD-68K is designed so users of Intellec systems may also develop software for M68000 products.



The proliferation of the microcomputer is affecting the programming development tools required to outfit these products for specific applications. Attempts have been made over the years to supply a universal development system, one that could be used to develop software for a variety of products. Virtually every one has fallen short of the universality goal due to the problems of supporting various vendors' evolving product lines.

The MDS-68K from Language Resources (Boulder, CO), is a more focused approach. Its the first hardware product from a company that has successfully developed cross-software development tools in the past. There is no claim made for the MDS-68K being a universal development system. What may prove to be a key to its success is that the MDS-68K is explicitly designed so users of Intel Intellec systems (the largest installed base of program development systems), may also develop software for the rival Motorola M68000 product line.

For emerging systems integrators, the advantage is obvious. Development systems aren't cheap; why buy two when one will do?

The MDS-68K's board contains 256K bytes of RAM linked to the M68000 CPU via a private bus. Additional memory boards can be added to the Intellec via Multibus slots and used for added program storage.

There are two other well thought out features of this product. First, it's claimed that the 68K's memory management subsystem prevents users from crashing the system by inadvertently writing to system RAM in which the Intel ISIS operating system resides. Second, system training time may be decreased – and operational productivity increased – since the developer uses the same procedures, screen prompts, etc., regardless of which chip vendor's software is being created.

Compilers available include Pascal, PL/M68 and Fortran; assemblers include MASM and AL/M. A symbolic debugger for use on assembly and high-level languages is offered separately. The basic product, including Motorola compatible assembler, linker/locator, symbolic debugger, 68000 CPU board and documentation is priced at $5,995. High-level language compilers, including Pascal, are priced separately at $1,995. – *Cashman*

Write 246

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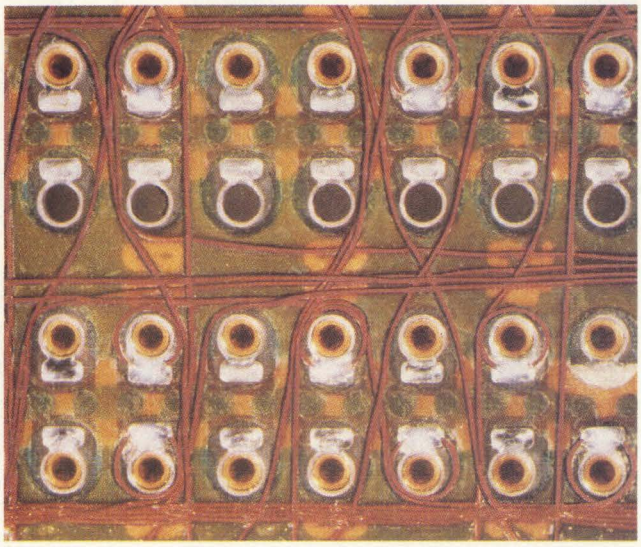
From Prototyping To Production – A Third Alternative

As semiconductor densities skyrocket, more complex printed wiring boards must be designed to accommodate them. The difficulty of designing and building these boards increases according to the complexity of the board.

Multilayer boards were developed over 20 years ago as an extension to double sided printed wiring boards, to accommodate increased interconnection densities. However, because of the complexity of circuit design in multilayer construction, the chance of having initial design errors is greatly increased. In addition, because several of the board interconnection layers are internal, circuit modifications cannot be made easily.

To overcome these obstacles, designers began to wire wrap boards. The problem of inaccessible layers is overcome because all wiring connections are now accessible. Designers can rework designs as they go along by unwrapping the wires and wrapping them around different pins. In many instances wire wrap is impractical for high volume production because the boards are too costly, and, in some applications, the profiles are too high to be placed in a final product. Final production requires a transition from wire wrap to multilayer boards which is difficult at best.

Unilayer 11 is an alternative design approach recently introduced by Augat Interconnection Systems Division (Attleboro, MA). The concept bridges the gap between wire wrap and multilayer printed circuit boards. Computer storage of design information used in conjunction with premanufactured board modules allows new designs to be started in wire wrap for prototyping and converted directly to Unilayer 11 wiring for production requirements, thus eliminating the cost and time normally associated with production redesigns.



Identical universal board modules are supplied with individual wire wrap sockets for prototyping.

Identical universal board modules are supplied with individual wire wrap sockets for prototyping and converted to Holtite zero profile sockets and Unilayer 11 wiring layers with soldered connections for production requirements. Circuit densities equal to multilayer designs, component pluggability and the ease of making wiring changes are maintained from prototyping through production. A variety of popular board sizes are stocked "on the shelf" ready for custom wiring and delivery in two to three weeks. Special designs require an initial six to eight weeks lead time prior to the start of the standard wiring cycle. – *Wilson*

Write 236

Second Source Agreement For VME Boards

Nine new VME modules (**Table 1**) including an Ethernet LAN controller and a 68010-based microcomputer were recently announced by the Microsystems Operation of Motorola. Three of the boards, the MVME 115MM, the MVME 320, and the MVME 025 are the results of a recent multisourcing agreement with Signetics/Philips.

The MVME115M microcomputer board can be used in applications ranging from standalone to dedicated control tasks. It can also be used in general purpose, disk based multiprogramming/multitasking environments including high speed data processing. The module features the

MVME101	VME module Monoboard Microcomputer with the MC 68000L8 MPU. Two serial ports and two parallel I/O ports.
MVME025	VME Module System Controllers with two mode bus arbiter, AC Power fail circuitry, watch-dog bus timer and system clock.
MVME115M	VME module Monoboard Microcomputer with 8MHz 68010 MPU, 68451 MMU one parallel and two serial I/O ports. Up to 64 Kbytes RAM/ROM.
MVME211	VME module Static RAM/ROM/EPROM Memory.
MVME315	VME module Floppy Disk Controller. SASI interface with DMA.
VME310	VME module for custom interfacing.
MVME330	VME module Ethernet LAN controller. Includes 128K of RAM, LANCE (7990) SIA (7991) 68000 MPU, Kernal Firmware and Power up self test.
MVME320	VME module Floppy Disk Controller. Supports DMA.
MVME202	512 Kbyte DRAM.

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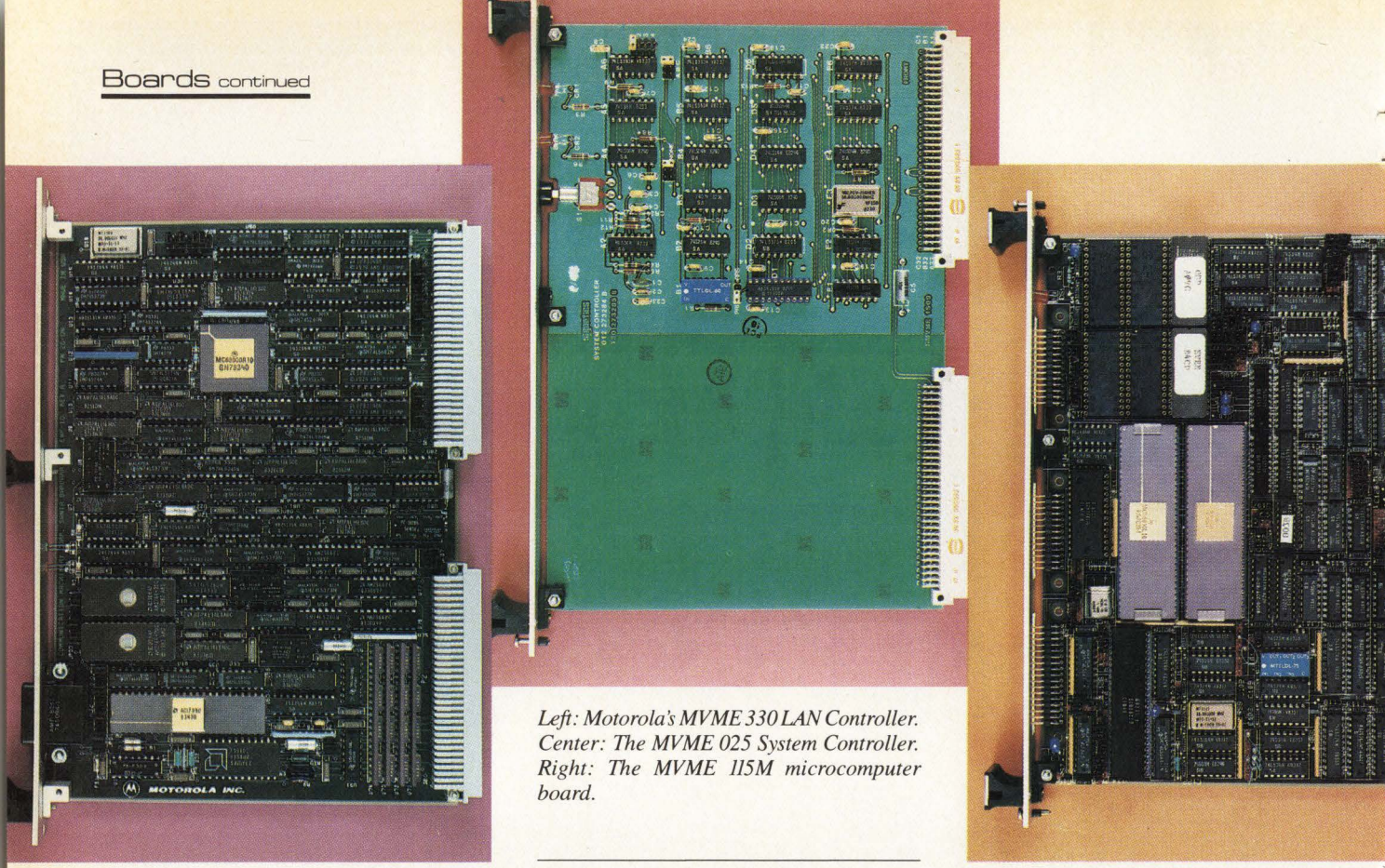

Left: Motorola's MVME 330 LAN Controller. Center: The MVME 025 System Controller. Right: The MVME 115M microcomputer board.

68010 and the 68541 MMU which provides access translation and protection over the entire 16 Mbyte range of the MPU. The MVME 320 disk controller provides high performance DMA data channels between system memory and either Winchester or floppy drives. The module is used in applications having intensive real-time disk I/O or multiprocessing structures to reduce VME bus traffic and increase system throughput. Floppy disk data transfer is done using two byte buffering. For hard disks, a 1024 byte local buffer is used. Automatic head switching and cylinder positioning is performed for operations requiring multiple sector read or write.

The MVME330 LAN controller provides the interface for 10 Mbits/sec Ethernet 2.0 implementation. The board frees the VME host from significant protocol burden through the use of a 68000 and the VLSI LANCE controller chip – the 7990. A communications executive runs on the LAN controller MPU supervising the LANCE chip in its execution of the Xerox Network System protocol package. A VLSI serial input/output adapter – the Am7991 provides Manchester encoding/decoding of the Ethernet interface.

Motorola projects that alternate-sourced supplies of the initial Signetics boards will be available in June. Signetics projects that alternate sourced samples of the Motorola designed 68010 MPU board will be available during the fourth quarter of 1984. *–Wilson*

Write 238

DEPARTMENTS/Graphics

Gate Array Co-Processor Draws 1 Mpixel/Sec In Low-Cost Graphics Terminal

Extremely high speed interlaced graphics displays have required bipolar bit-slice processors and their associated circuitry, driving up the cost of machines capable of drawing one million pixels per second, to about $6,000 to $10,000. Terminals for under $3,000 are widely available, but speeds several times slower than bipolar usually force screen interlacing or low resolution. In these lower priced terminals, many manufacturers have used the NEC 7220 chip as a graphics co-processor to offload graphics functions from the host microprocessor.

To build terminals inexpensively with the high quality fast drawing of more costly devices, Digital Engineering (Sacramento, CA) has developed a CMOS gate array for their new HiScan series to draw 1 Mpixel/sec, non-interlaced. Both color and monochrome HiScan terminals use this 2200-gate 3-micron technology array, dual ported for simultaneous access to the bit map and microprocessor.

The gate array co-processor and 4MHz Z8002 processor are in a pipelined architecture with read-modify-write hard-

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All of which means someone is going to be very happy. Visual cueing is better. And picture manipulation is localized. Which, of course, makes operators faster and more productive. And mainframes less burdened. Two cost-efficiencies every company can live with.

The 1104 will even support ANSI 3.64. And give you a VT100 keyboard (with 16 function keys). So there are no re-learning curves to finance.

What's more, the 1104 is Plot 10 compatible. Which means it can emulate the TEK 401X instruction set. And you can save a lot of time and money on software development.

Now for some impressive technology.

The 1104 uses four (not the usual one) graphic display controllers. So figures are drawn, filled and manipulated faster. There's no drag on the system caused by processor or memory overload.

Next, the video formatter is our own custom-LSI design. A gate array (2000 gates) that reduces power consumption and board space. And provides the video speed necessary for output to our high resolution display.

Which, we hasten to add, is beautiful. Especially with its .31mm pitch shadow mask. And contrast enhancement filter that eliminates screen glare and improves visual acuity.

You'll also be happy to note that the 1104 supports our Graphics Tablets (there are two) and Color Hard Copier (the one that's already taking the industry by storm).

One last item. Because we design, build, sell and service all of our products, you can count on getting the back-up you need. Direct service from 13 offices across the U.S.

So make life easy on yourself. Call today to get the full GR-1104 picture. It's easy. Just call your local Seiko Instruments sales person, or us at (408) 943-9100, or write 1623 Buckeye Drive, Milpitas, CA 95035.

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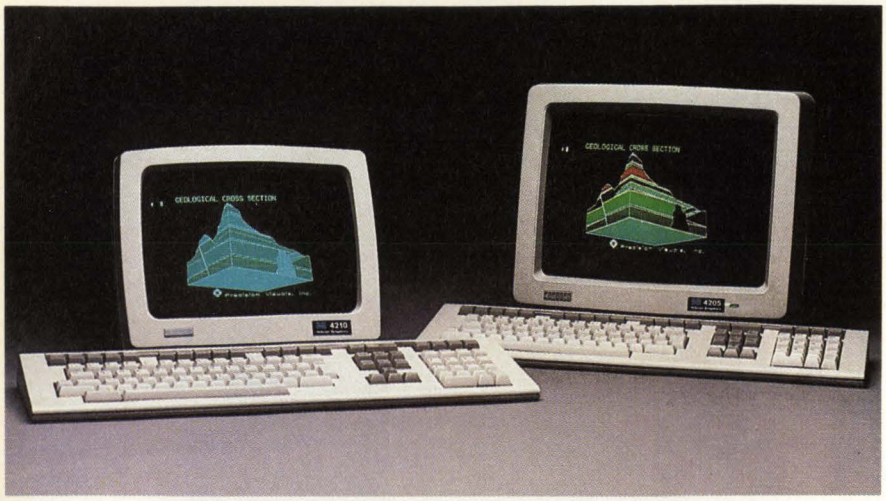


The custom VLSI architecture of HiScan Graphics terminals allow complex graphs to be drawn at 1 Mpixel/sec.

ware. While the read-modify-write element calculates the next address to modify, the graphics processor prepares its next instruction, and the microprocessor loads the next graphics software module. This pipelined speed is further increased during area fills to the screen, which can be 32 Mpixel/sec by parallel transfers.

In addition to the gate array for graphics, speed is improved and costs moderated with the use of 64K 16K × 4 RAMs instead of 16K × 1s, which are commonly used in high-end graphics terminals. With 4-bit data paths to the graphics memory, accesses are four times faster, and the bit map memory needs only one-quarter as many chips, at 64K per device.

All of the speed inherent in the 1 Mpixel/sec gate array plus 4-bit wide RAM paths and pipelined architecture have allowed Digital Engineering to eliminate the alphanumeric character generation and ROM. Both text and graphics use the same bit map, eliminating alphanumeric and mixing circuitry. A two memory plane bit map provides 16 simultaneous colors of 64 for the 4105. Only a few terminals bit map alphanumeric text because, for scrolling or blink, for example, each entire line must be redrawn and replotted to affect that simple attribute. And, unless drawing speeds are extremely fast, smearing and slow response make displays almost unusable.

Readability and ergonomics are further enhanced by the non-interlaced display. High line rate CRTs have been too expensive for terminals under $3,000, although costs have been dropping. Their speed brings the same non-flicker, non-smear graphics of high-end terminals. The 4210 monochrome HiScan terminal uses DEC's 800 × 600 pixel screen, and the 4105 uses the DEC 800 × 300 pixel color monitor. In creating their own terminal product line, Digital Engineering lowered costs in part simply by not replicating functions, as is common in add-on or retrofit products.

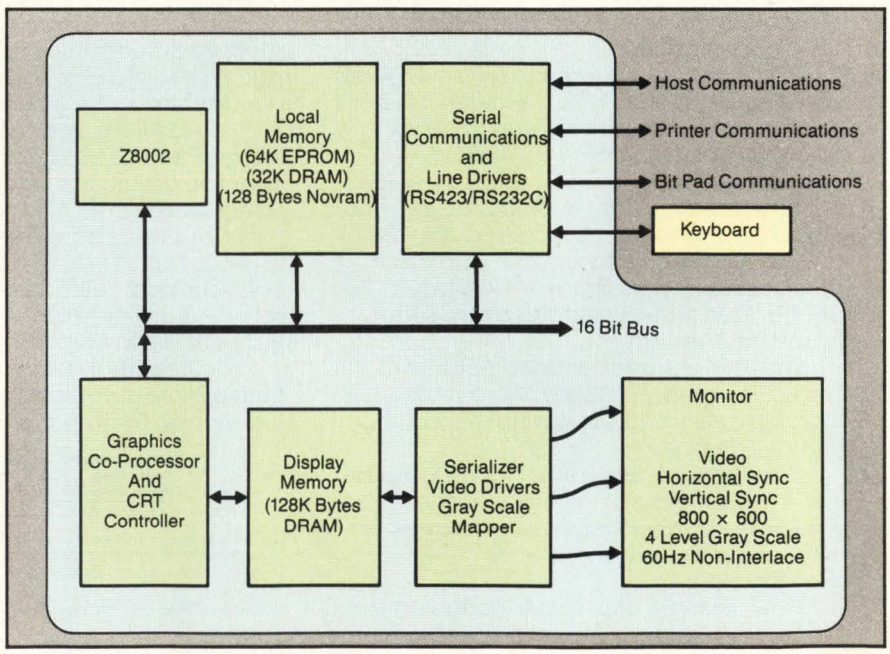
HiScan terminals can be specified for several popular emulations; Tek 4027 or 4105 or DEC ReGIS protocols as well as DEC VT220 text and Tek 4010/4014 graphics may be chosen. Digital Engineering claims this is the most emulations anyone offers at the price range. The monochrome 4210 terminal, available July 1, 1984, is $2195, and the color 4105, available in September 1984, will be priced at $2995.

Speed improvements over terminals in the same price range that use a single processor or even the 7220 off-the-shelf coprocessor are significant. Phil Grasso, President of Digital Engineering, points out that the 7220 was not built as a graphics processor. Though it runs at 1 Mpixel/sec like their proprietary gate array, the 7220 does not allow two port interleaved access to the bit map. It stands idle except during the blanking intervals, resulting in only a 10-15% duty cycle. Grasso also noted that as a standard part, the 7220's features are fixed. The gate array for HiScan does all of the set-up for vector processing, allows tilt and rotation of text, pixel multiplication and can adjust for dot pitch other than 1:1 (although the monochrome HiScan has 1:1 pitch).

The combination of sophisticated parts and pipelined architecture allows Digital Engineering to claim that they can offer the functionality of a $10,000 graphics terminal for far less. The main factor is the low-power CMOS gate array coprocessor, optimized for fast drawing on their system. The graphics speed, 64K RAMs, high line rate CRTs and non-interlaced displays have only recently become possible without great cost. With an architecture to combine all of those features, parts are eliminated and even greater cost reduction and efficiency results.

—Pingry

Write 239



Block diagram of HiScan Graphics Terminal.

Photo: Peter B. Kaplan

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Inspiring plans have been developed to restore the Statue and to create on Ellis Island a permanent museum celebrating the ethnic diversity of this country of immigrants. But unless restoration is begun now, these two landmarks in our nation's heritage could be closed at the very time America is celebrating their hundredth anniversaries. The 230 million dollars needed to carry out the work is needed now.

All of the money must come from private donations; the federal government is not raising the funds. This is consistent with the Statue's origins. The French people paid for its creation themselves. And America's businesses spearheaded the public contributions that were needed for its construction and for the pedestal.

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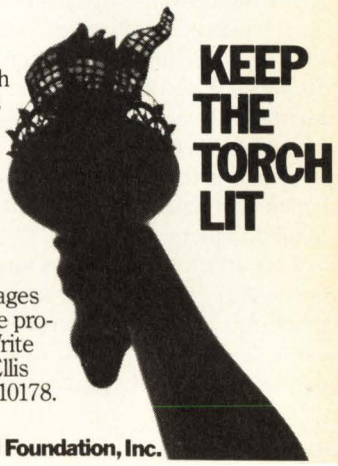

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The IBM PC Bus Remains The Standard For Hardware Compatibility

The IBM PC has an open architecture, a factor that has led to the third party development of boards and software.

by Andrea Coville,
New Products Editor

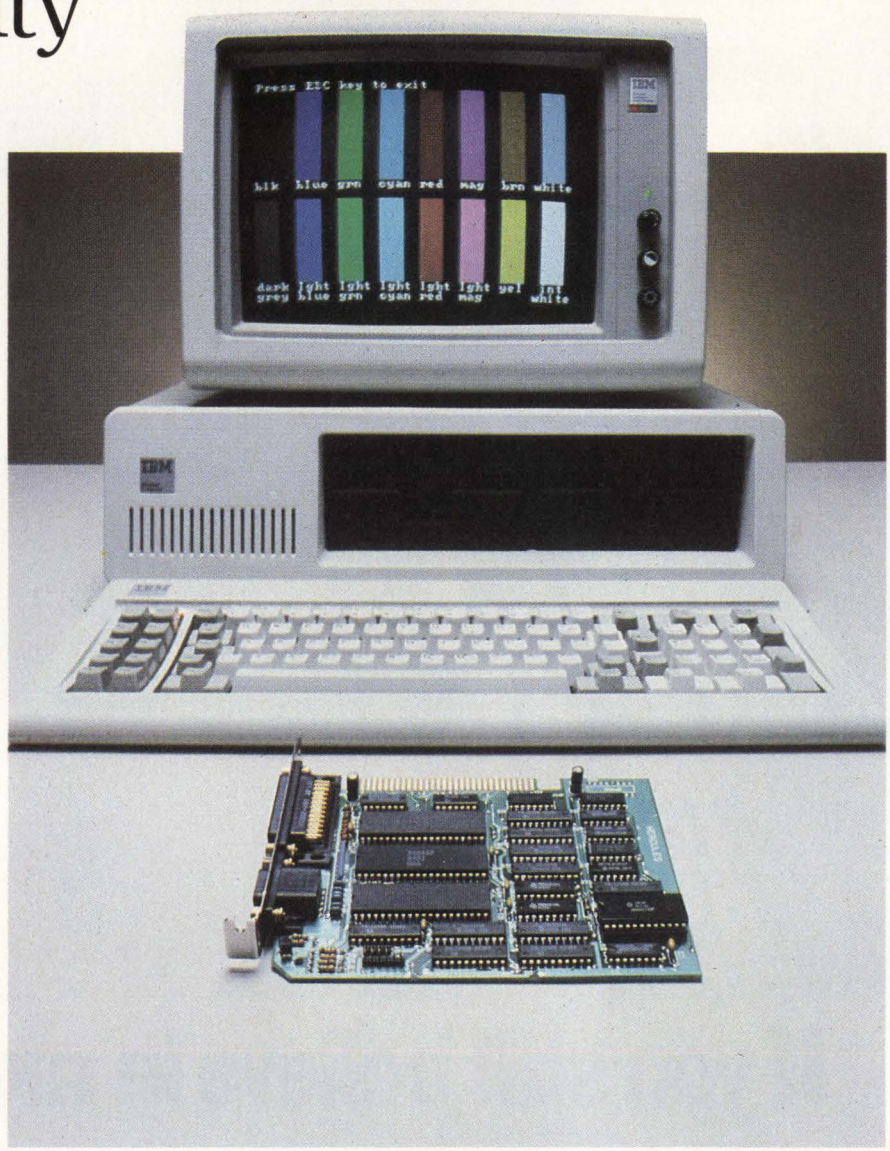

Figure 1: The Hercules color card from Hercules Computer fits into one of the IBM XT's short expansion slots.

Observing the current success of the IBM line of personal computers, manufacturers of compatible products should have a correspondingly bright future. IBM has captured 31.6% of the North American market for desktop and portable computers and is leading microcomputers into the scientific and industrial areas that were previously the realm of the minicomputer.

Defining compatibility proves to be a difficult task, for compatibility can refer to hardware, software or a whole system. But in a loose definition there are four levels of compatibility. Three are associated with software and the remaining one with hardware. Software compatibility includes machines which run between 50% and 95% of the software available for the PC. Disk compatible machines can neither run PC software nor read information from PC formatted disks, but can accept data from a PC if it is downloaded to them.

This article will address machine (or hardware) compatibility, specifically a machine's ability to accept accessory cards designed for the PC or XT. These cards must be pin for pin compatible with the PC's I/O channel, which is an extension of the bus on the system's microprocessor, the Intel 8088.

History

IBM announced the first product in its line of personal computers (which is now comprised of the IBM PC, PCjr, PCXT, XT/370, 3270PC and the CS9000 series), the IBM PC, on August 12, 1981 and made its initial delivery two months later. To date, IBM has 25% of the personal computer market and has shipped over one half-million units. In the process, an untold number of companies have created add-on hardware products. (Over 750 are

listed in Ironoak Company's "The IBM PC Buyers Guide.")

IBM took a unique corporate posture when developing the PC. They built on the progress made by the many successful small companies that were designing and marketing microcomputers. With their extended resources, they quickly became an industry standard. The hardware chips and the software used in the PC are manufactured by outside companies. Intel makes the machine's eight-bit processor, the 8088, and Microsoft wrote the PC-DOS operating system. Because the hardware and software were published, the PC has an open architecture. This factor has led to the third party development of boards and software. One part, however, of the PC's architecture is proprietary, the BIOS software which resides in ROM. Because of this, no manufacturer can claim to be 100% IBM PC compatible.

Figure 2: The Quadboard from Quadram is a multifunction board for the IBM PC which expands memory to 384K.

System Board Design

The system board for the PC (**Figure 4**) is a multilayer single land-per-channel design, with ground and power internal planes provided. DC power and a signal from the power supply enter the board through two six-pin connectors. Other board connectors are for attaching the keyboard, audio cassette and speaker. Five 62-pin card edge sockets are mounted on the system board. The system I/O channel is bused across these five slots.

The major elements of the board are divided into five areas. They are the processor subsystem and its support elements, the read only memory (ROM) subsystem, the read/write memory (RAM) subsystem, integrated I/O adapters and the I/O channel. The XT board is similar but has eight expansion slots as compared to five on the PC and one DIP switch instead of the PC's two.

I/O Channel

The PC's I/O channel is the key element to consider when determining the degree of compatibility of an add-on board. The description which follows (**Figure 6**) contains the specifications a hardware designer needs when building a PC compatible board.

The I/O channel is an extension of the 8088 microprocessor bus. It is demultiplexed, repowered and enhanced by the addition of interrupts and direct memory access (DMA) functions.

The channel contains an eight-bit bidirectional data bus, 20 address lines, six levels of interrupt, control lines for memory and I/O read/write, clock and timing lines, three channels of DMA control lines, a channel check line, and power and ground for the adaptors. These functions are provided in a 62-pin connector card with 100-mil card tab spacing.

A ready line is available on the I/O channel to allow operation with slow I/O or memory devices. If the channel's ready line is not activated by an addressed device, all processor-generated memory read and write cycles require five clocks for a cycle time of 1.05 μs/byte. DMA transfers similarly require five clocks for a cycle time of 1.05 μs/byte. Refresh cycles occur once every 72 clocks and require four clocks and approximately 7% of the bus bandwidth.

I/O devices are addressed using I/O mapped address space. The channel is designed so 512 I/O devices are available to the I/O channel cards. A channel check line exists for reporting error conditions to the processor. Activating this line results in a non-maskable interrupt (NMI) to the 8088 processor. Memory expansion options use this line to report parity errors.

The I/O channel is repowered to provide enough drive to power the five expansion slots, assuming two low-power Schottky loads per slot. The IBM I/O adaptors typically use one load.

Signal Lines

There are 18 types of signal lines on the I/O channel, all of which are TTL-compatible. There are two clocks, an oscillator (OSC) and a system clock (CLK) which have periods of 70 ns (14.31818 MHz) and 210 ns (4.77 MHz) respectively. The reset driver (reset DRV) is synchronized to the falling edge of the system clock and is used to reset or initialize system logic upon powerup or during a low-line voltage.

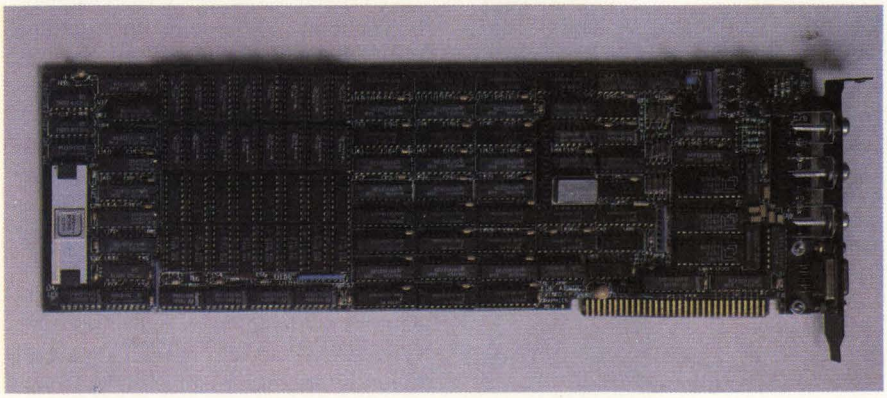

Figure 3: Featuring the NEC 7220 chip and 128K of memory, the IDEAgraph color graphics board from IDEAssociates allows the PC or XT to be used in CAD/CAM applications.

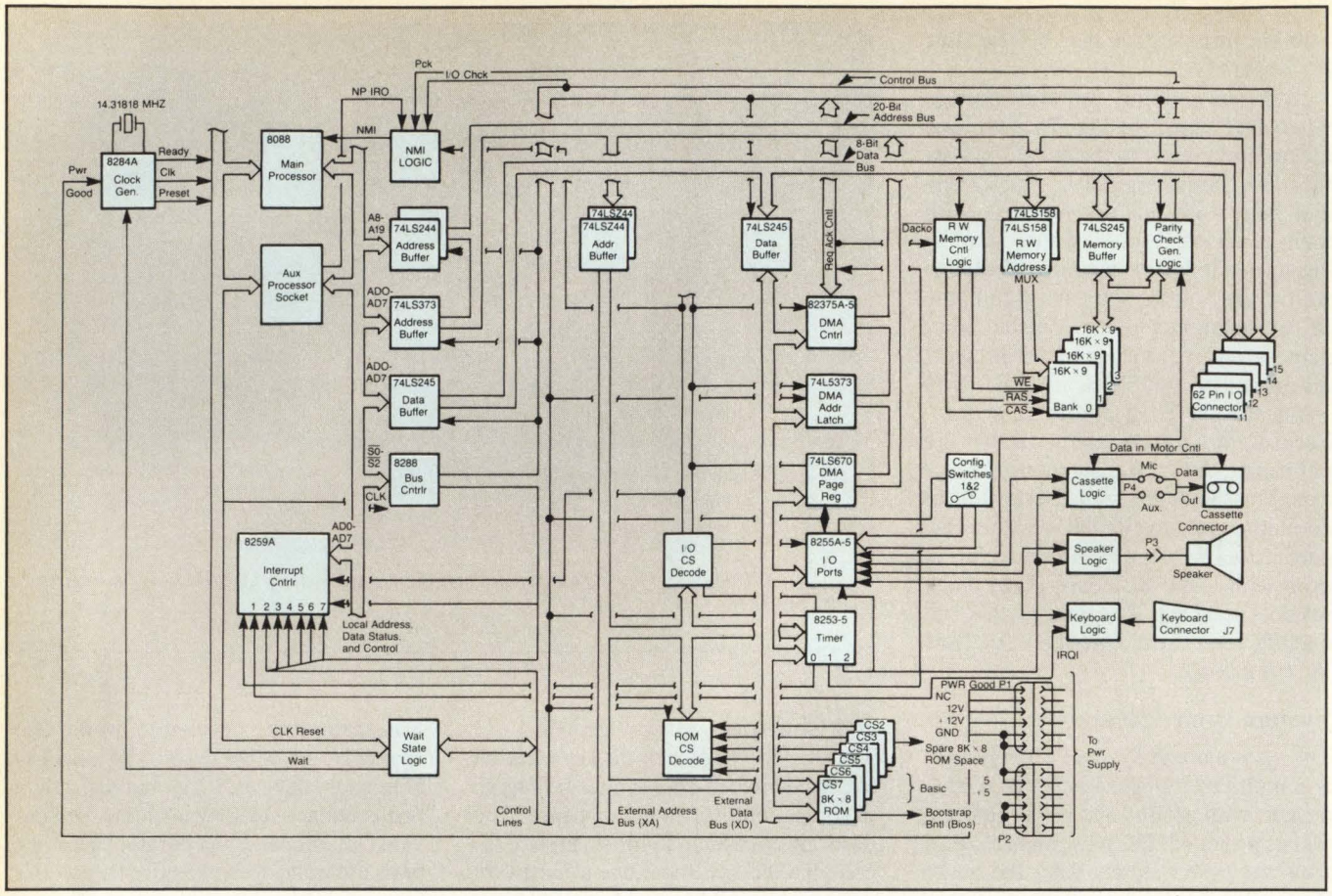

Figure 4: System board diagram of the IBM PC. The board can support either 16K to 64K or 64K to 256K of RAM.

The address bits located on lines A0-A19 are used to address memory and I/O devices within the system. The 20 address lines access up to one Mbyte of memory. A0 is the least significant bit (LSB) and A19 is the most significant bit (MSB). The address lines are active high and are generated by either the processor or the DMA controller.

Eight lines (D0-D7) are data bus bits for the processor, memory and I/O devices. D0 is the LSB and D7 is the MSB. These lines are also active high. The address latch enable (ALE) is used on the system board to latch valid addresses from the processor. It indicates to the I/O channel which processor addresses are valid.

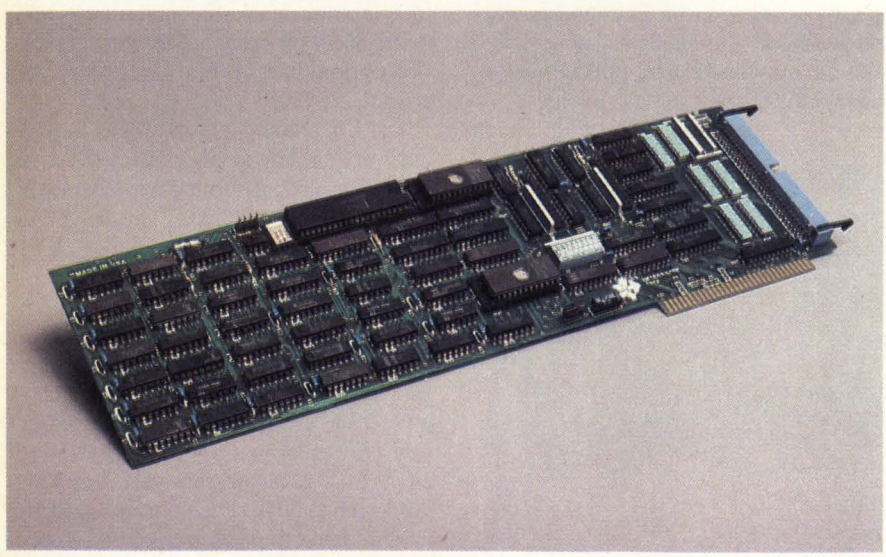

Figure 5: Interphase Corp.'s Maverick SMD PC-80 is a rigid disk controller which allows the PC to support the SMD interface.

Two lines are designated to provide the processor with information on memory or other devices in the I/O channel. The I/O channel check ($\overline{\text{I/O CH CK}}$) provides a signal which when active low, indicates a parity error. The I/O channel ready (I/O CH RDY) allows slower devices to attach to the channel. When this line is pulled low (it is normally high), it lengthens memory or I/O cycles, thus accommodating a slower processor time.

Interrupts are handled by lines IRQ2-IRQ7. They are used to signal a processor that an I/O device requires attention and are prioritized, IRQ2 being the highest and IRQ7, the lowest.

Read and write commands for I/O and memory are handled by four lines $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$. They are all driven by the processor or DMA controller. DMA requests are handled by lines DRQ1-DRQ3. These asynchronous

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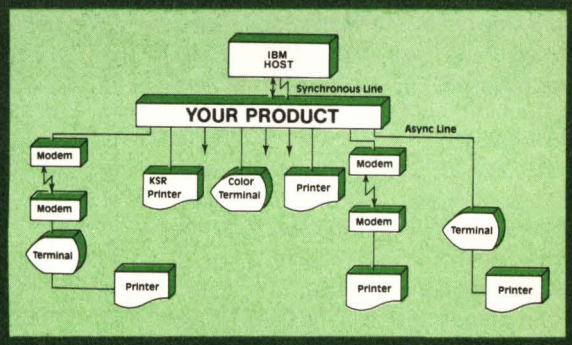

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lines are used by peripheral devices to gain DMA services and are prioritized with DRQ1 being the highest.

DMA acknowledge lines are represented by $\overline{\text{DACK0}}$-$\overline{\text{DACK3}}$. These lines refresh system memory and also acknowledge DMA requests. The remaining two lines AEN and TC are an address enable and terminal count. The address enable is used to degate the processor and other devices from the I/O channel and allows DMA transfers to take place. The terminal count provides a pulse when the terminal count for any DMA is reached. The following voltage lines available on the I/O channel are; +5 Vdc, −5Vdc, +12Vdc and −12 Vdc. GND signifies the ground line.

Applications

The Quadboard from Quadram Corp. (Norcross, GA) is one example of a multifunction board which plugs into the IBM expansion slot. The board is expandable to 384K RAM using 64K increments and includes a parallel port for attaching printers and a serial port which connects modems and other devices.

Baron Hall, Technical Support for Q3 and Quadram says, "The multifunction board plugs in through the 5150 data bus lines and utilizes DMA, IRQ-4 and IRQ-3. We looked at the way IBM addressed its parallel port and then used the same addressing and DMA. We make our DMA hex address the same as the standard set by IBM. With our chronograph, we had to find an open channel or address space at 310 (generally it's 210) but because the expansion chassis took up address space we had to fill it up. As far as any limitations with IBM's design, those reside with the limitations of DOS and other compatible software."

"Because PC-DOS will only allow one DOS partition per hard disk we had to fool the system by putting two 33 Mbyte partitions on."

IDEAssociates (Bedford, MA) makes a color graphics card for the IBM PC and XT. Their design incorporates the NEC 7220 chip, has 128K of memory and generates four color planes (16 colors) at the resolution of a standard PC monitor, 640 × 200 pixels. The board's functions are hardware driven and operate at 80 ns per pixel. The software that comes with the board is compatible with IBM BIOS, IDE-extended BIOS and the virtual device interface (VDI).

Paul Stephancyk, Software Engineer for IDEAssociates, says that hardware compatibility is a straightforward matter. "Any expansion board that fits into the PC bus has to use signals according to its definition. In order to interface our board to the bus structure, the graphics controller (NEC 7220) takes the contents of the display memory (256K) which resides on the graphics board, converts them to an analog signal, which is then sent to the PC monitor. This is called the raster scan process."

"The only thing that goes across the PC bus is commands to NEC chip, because our device's memory is not in the address space of the 8088. It is desirable, however, for a programmer to be able to address this space. What must happen, is that the programmer addresses the NEC chip by giving it a command saying, 'I want to address this byte in display

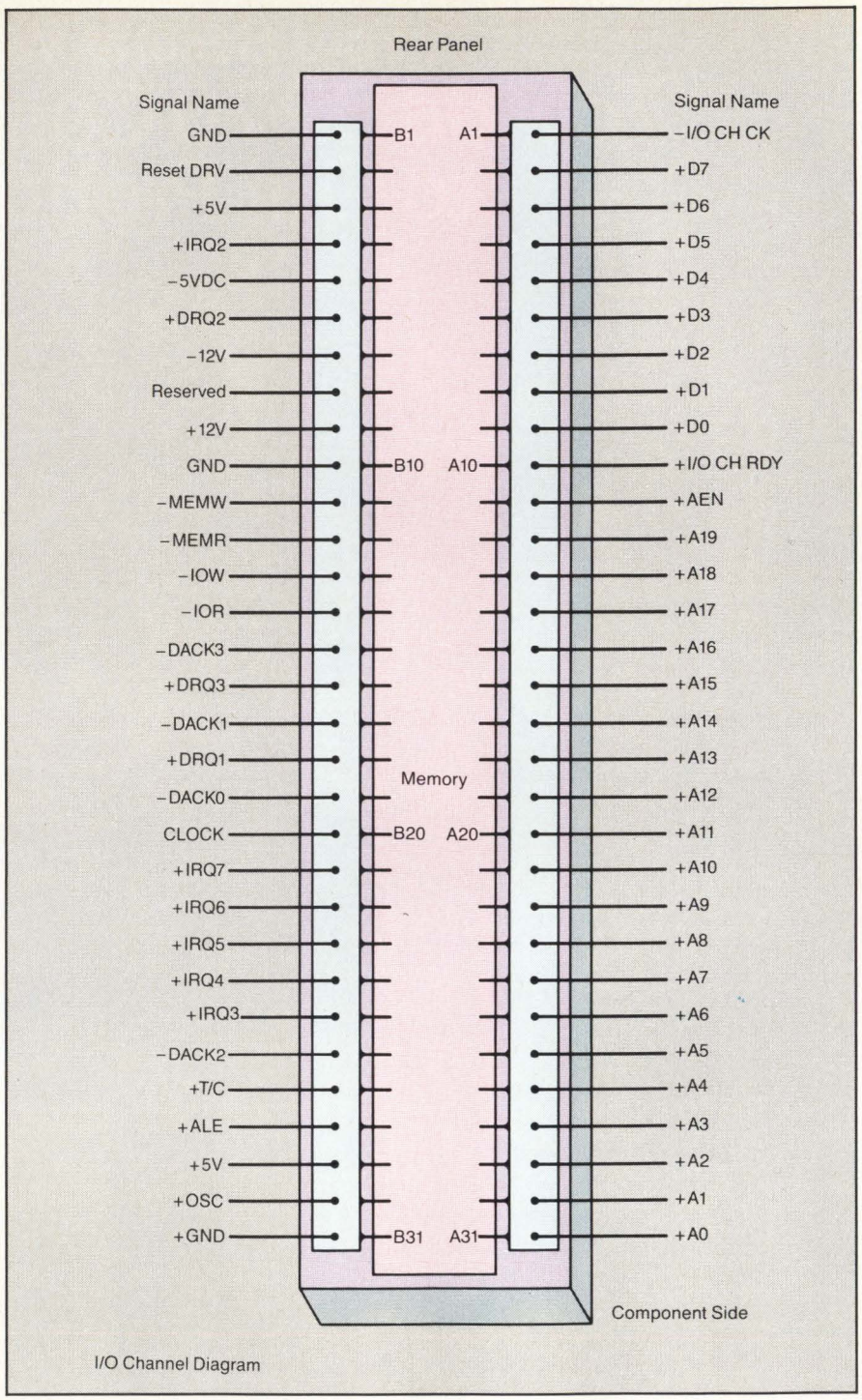

Figure 6: Diagram of the I/O channel which is an extension of the 8088 microprocessor bus. The I/O channel is bused across the system's five I/O slots.

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memory.' The programmer in effect has altered the contents of the display memory through the NEC chip, which can understand 20 commands."

Hercules Computer (Berkeley, CA) manufactures a color card which is one half the size of IBM's color card. It is inserted into one of the XT's short expansion slots, allowing the longer slots to be used for full-sized cards. The card has a parallel printer port and is compatible with all color graphics software for the IBM color card. It can be kept in the system at the same time as the full-size Hercules Graphics card which provides graphics capabilities for the monochrome display of the PC.

Votan's (Fremont, CA) voice card addresses another application area for the PC: voice input/output. Its printed circuit board plugs into any of the auxiliary system bus slots, and includes microphone, speaker and software. Voice input replaces keystroke combinations which activate applications. For each application program, the user defines as many as 64 words linked to the voice card which causes the keyboard to type the keystrokes linked to each command.

The 488 Controller from Ziatech (San Luis Obispo, CA) has found applications in the areas of measurement and instrumentation. It is a short slot card, the heart of which is Texas Instruments' TM39914 GPIB controller chip. According to Alan Beverly, Engineering Manager, one of the design problems Ziatech encountered was in deciphering the timing diagrams for the PC bus. "We went through the IBM schematics," says Beverly, "and literally made the timing diagrams. Since IBM is always pushing for third party support, they should provide this information, because without it, you can end up with a board that sometimes works and sometimes doesn't."

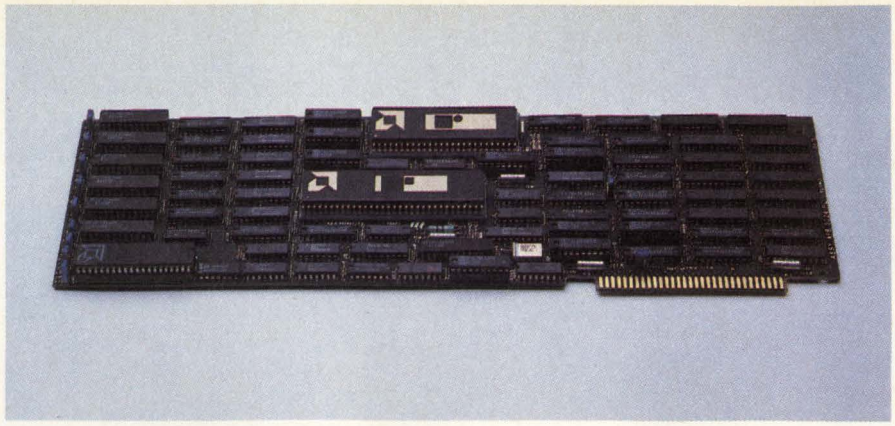


Figure 7: Utilizing a 16-bit AM29516 eight MHz parallel multiplier, the Marinco APB-3024 PC adds array processor functions to the IBM PC.

"As far as the bus structure, it is a very popular design and I have no problems with what IBM has done. Because we design for many 8088-based microcomputers, we are familiar with the 8088. The way that IBM implemented the I/O is a reasonable first shot. But for a second or third design it would have problems. For instance, future machines will need to share DMA channels and have more interrupts. With only one DMA channel, what happens if you have more than one I/O board? I would also like to see them address the area of real-time multitasking."

Ziatech considers the connector they developed for the I/O backplate one way in which they have enhanced the PC's design. According to Beverly, "The 488 connector is too big to fit into their backplate conveniently. Because of this you do not get a good mating connection with the other connector. With our back bracket, consisting of an integral connector, shielding and backplate, we get a great seating."

Applications for the PC are endless, as the designer of an accessory card has only to comply with the hardware specification mandated by the PC's I/O channel. Other application areas are represented by Interphase Corp. (disk controllers), Prentice (modems), Discortex (color transformers), Dilog (electronic disks) and Marinco (array processors).

Conclusion

Hardware compatibility has and will continue to develop alongside the standard set by IBM. As IBM incorporates enhancements into the PC, manufacturers of accessory cards will make adjustments accordingly.

Although the PC will change, the movement will neither be drastic nor unexpected as the PC's success relies heavily on the development of third party hardware and software. Manufacturers of compatible products have saved IBM a tremendous amount of research.

According to Hall, there is the factor of the 16-bit processor sometime in the future. "If IBM goes to a 16-bit processor all of the compatible boards will be obsolete. This will probably happen but when it does, it will be a trickle down effect."

Another general prediction for the PC is that IBM will incorporate the recently announced 256K RAM chips into the system board. If so, memory expansion boards will have to be redesigned to accommodate increased memory capacity and may necessitate three, four or five communication ports. But the bottom line for compatibility is, as one company spokesperson said, "We look at what IBM does and try to get as close as possible."□

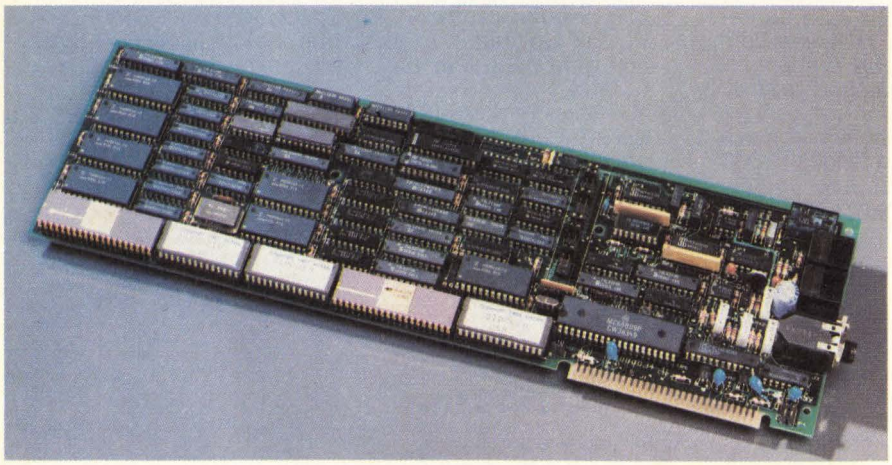
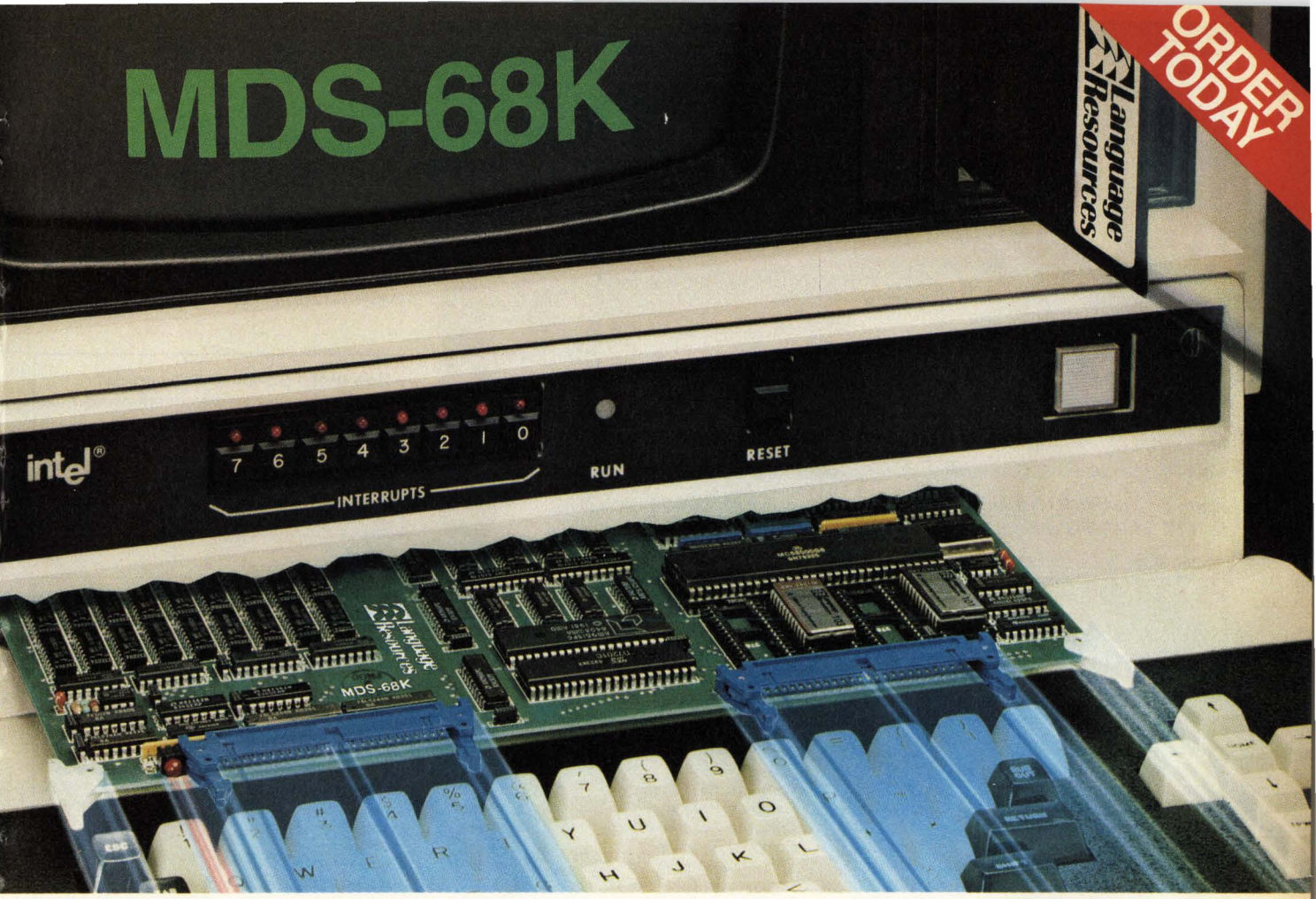


Figure 8: The VPC 2000 voice card from Votan brings voice I/O functions to the PC.



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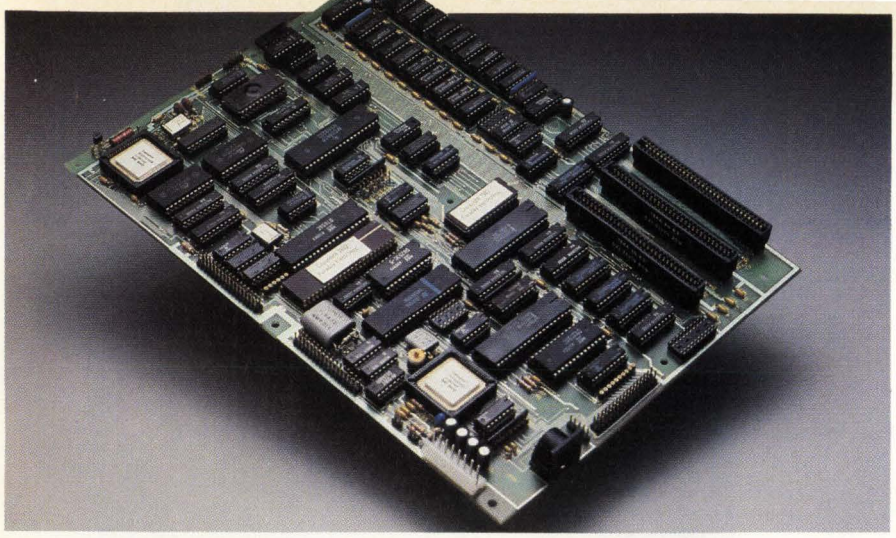

Figure 9: The FE6413 is a single board computer from Faraday Electronics compatible with the IBM PC which has either a floppy disk or monochrome display controller option.

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2.) *IBM Personal Computers.* Datapro Research Corp., Delran, NJ.
3.) *IBM PC Buyers Guide.* Ironoak Company, La Jolla, CA.

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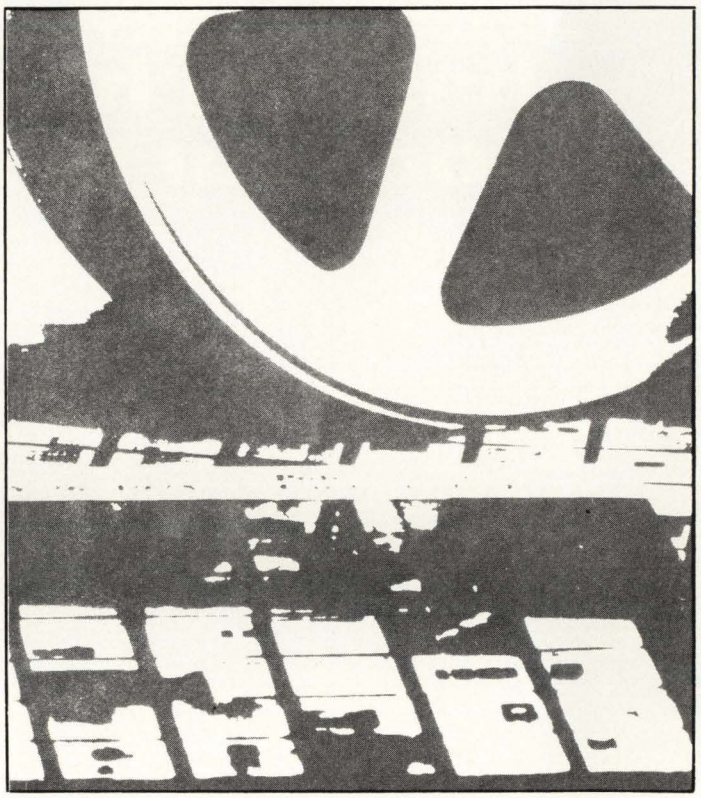

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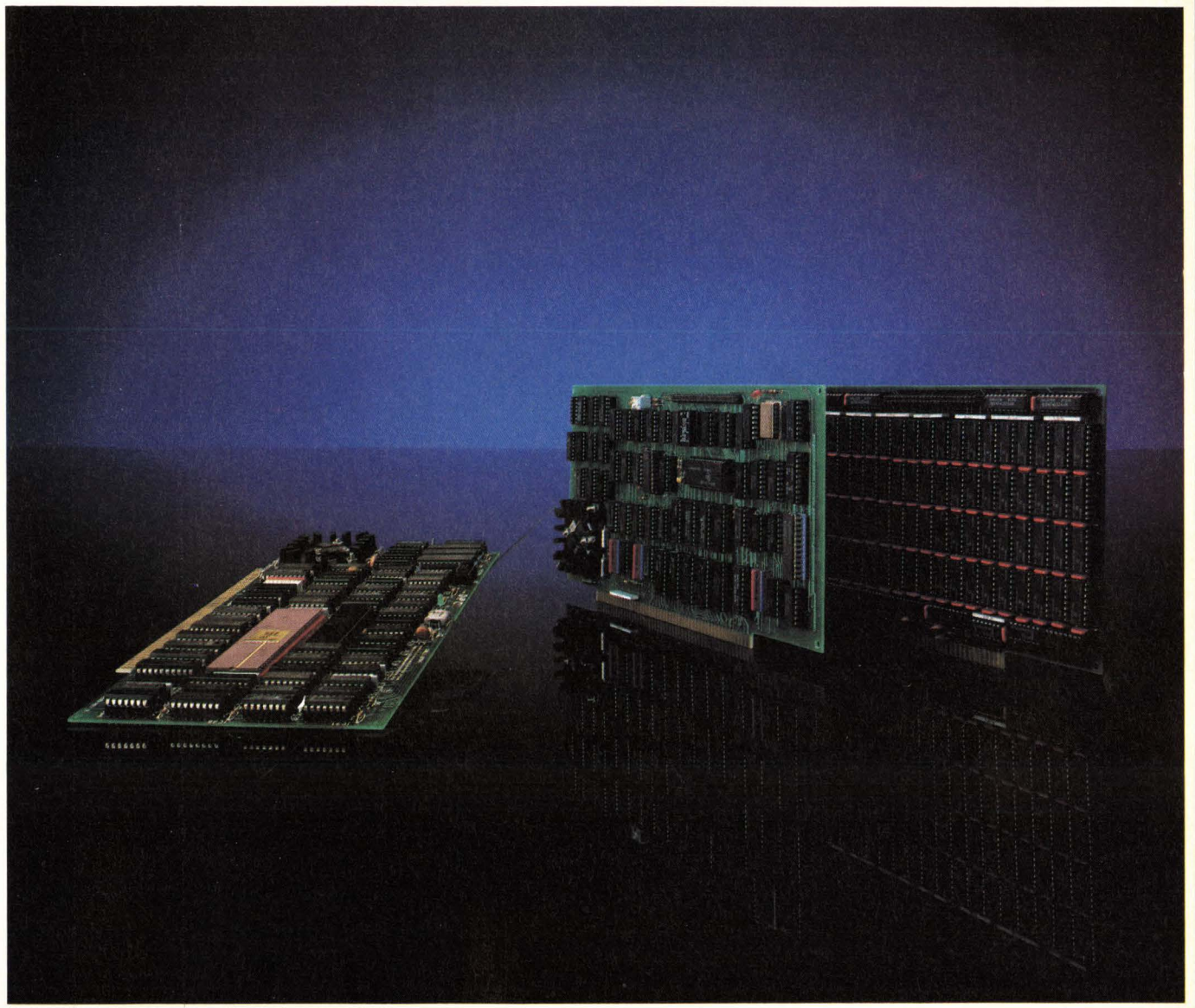

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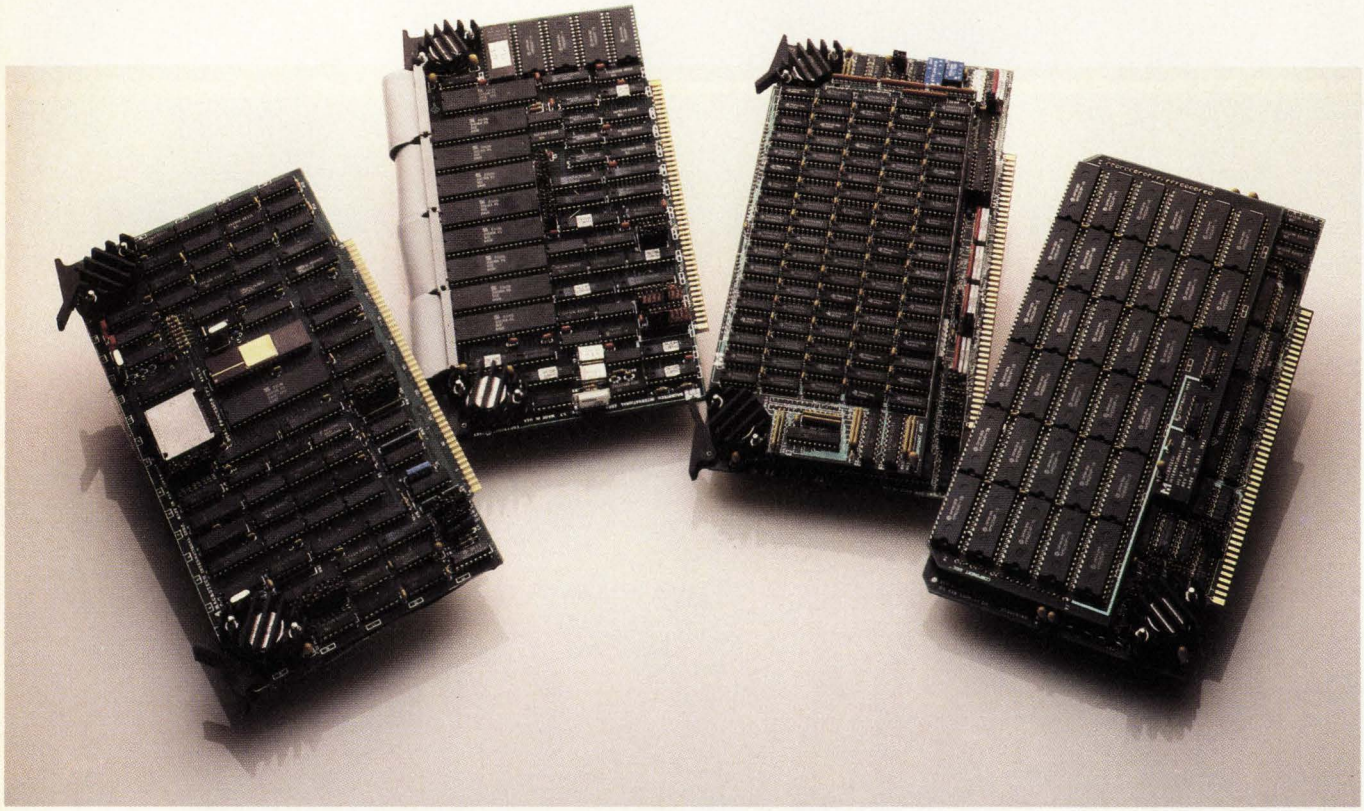


Designer's Guide To The S-100 Bus

by Dave Wilson, Executive Editor

At present, the single board computer market is more than $500 million and is growing at approximately 30% per year. By 1986, it will be at $1 billion. One of the latest studies to examine the marketplace is from Gnostic Concepts, commissioned by Intel Corporation. It shows the concentration of the market on a few key architectures – namely Q-bus and Multibus (**Figure 1**).

If the study is true, it would place other bus structures, such as the STD, IBM PC, CIMbus, and the S-100 bus in a narrow 9% of the market, worth about $53 million per year between them. Of course, if that percentage of market share even stays at a constant until 1986, those buses' market would double in value to $100 million by that time.

That scenario is, however, unlikely to be correct, and several indicators validate this. The newer bus structures that are emerging, such as Multibus II and VME bus at the high-end of the market as well as the imminent long-awaited BI bus, inevitably will make large inroads into the market pie. The simple fact is that these newer entries are supported by major players in the industry (Intel, Motorola and DEC). A good deal of thought has gone into the systems architecture, and not simply bus structure, and ease of design will be facilitated by IC support for bus interface functions from those vendors. These are only a few of the factors that will contribute to their success.

More importantly, the Multibus I may contribute heavily to the demise of earlier buses such as the S-100. Traditionally, the OEM has weighed many factors – such as product development cost, final product cost and time to market in deciding the bus around which he should build a system.

Low Cost

Possibly the most redeeming of these factors for the S-100 has been its low cost. Today, however, the increasing functionality and decreasing cost, increased reliability and better performance of Multibus boards poses the question of how long the S-100 can survive. As an example, Intel's latest 186/03 (*Digital*

Four S-100 add-in boards from Macrotech International include (left to right) the MI-286, a CPU that uses the 286 and Z80B, the ADIT (version 1.1) which can extend a CPU to as many as 16-terminals, modems or printers; the MAX-M, a 1 Mbyte RAM memory board and the 512-STATIC, a half Mbyte static memory board.

The S-100 is alive and well despite competition from the IBM PC and alternate bus structures.

Design, May 1984) with the ISBC 341 and SCSI drive costs a mere $2000, a $2475 cut from the previous solution (**Table 1**). Other vendors, such as Metacomp (San Diego, CA) with their MPA- 2000 are also following this trend claiming to be single board replacements for two, three or four board members in many applications. It appears that the Multibus is taking not only the low-end but also the high-end market by storm through the architectural enhancements that have been made to the bus in the form of the iSBX, iLBX, and Bitbus interfaces.

Unfortunately, the same cannot be said for the S-100 bus. Although it has heavy support from Cromemco and CompuPro, little has been done to enhance the architecture for high performance systems since its inception. Today, the S-100 marketplace is highly fragmented, with many garage and mail-order operations in the business. These may offer anything from complete systems to add-in boards for upgrading older hobbyist microcomputers to esoteric products like data encryptors and telephone answering devices.

Application Areas

One of the major differences between the Multibus and the S-100 lies in current application areas. Unlike the Multibus, the S-100 is a development/commercial systems bus. Many large companies may purchase off-the-shelf S-100 cards simply to evaluate newer microprocessors and disk/tape interfaces around which they will then develop their own system. This is how IBM developed the PC, ironically leaving some S-100 based personal computer vendors in a static market corner. Worse still for the S-100, the rampant success of the IBM machines has geared software houses toward that product and away from the S-100 bus. It may appear from the above discussion that gloom, doom and certain bankruptcy face the S-100 vendors and that competition from other bus structures and the IBM PC and its band of clones will inevitably obliterate the bus.

While most vendors appreciate that the S-100 is a mature market, many report that it is still a healthy one and not about to vanish overnight. This may be in part due to its rather unique market position and also to designers' familiarity with the bus' past as it emerged from the hobbyist environment.

Like the Multibus, earliest S-100 designs placed single functions on each PC board, allowing the integrator to select only those functions needed for a specific application. As on-chip functionality increased, the market demand for efficiency and cost-effectiveness directed many S-100 manufacturers to design multiple function SBCs that can be found on the market today. The most advanced offer a variety of CPU options, RAM, I/O with on-board drivers, and a floppy disk controller. If additional functions are required, the user may insert the required graphics, modem or other card to expand the capability of the system.

WITH SINGLE BOARDS	
Solution	**Price**
iSBC 86/05	$1500
iSBC428	$ 695
iSBC215G	$1500
iSBX218A	$ 540
iSBX 351	$ 240
TOTAL COST	**$4475**

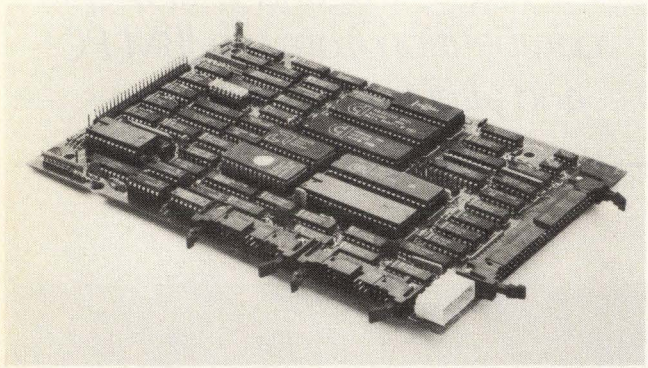
WITH SINGLE BOARD SYSTEM	
Solution	**Price**
iSBC 186/03	$1650
iSBC 341	$ 150
SCSI DRIVE PREMIUM	$ 200
TOTAL COST	**$2000**

Table 1: SBC 186/03 peripheral controller system integrates functions and lowers cost.

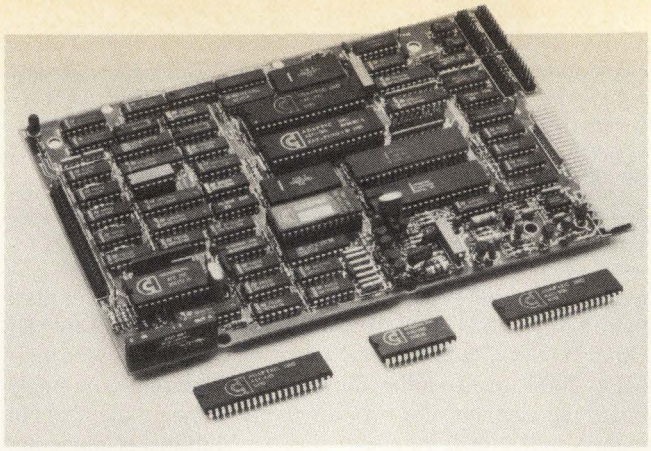
The CompuPro 8/16 microprocessor-based system set in a multi-user environment.

The trend is clearly toward multi-processing as well as multi-tasking. In even a modestly sized four to six user multi-tasking system, efficiency is seriously degraded if users must share a single processor. As hardware becomes less expensive, manufacturers are placing more and more intelligence on slave and peripheral controllers and enhancing the system capabilities through block mode and DMA schemes to reduce processing overhead on the master CPU.

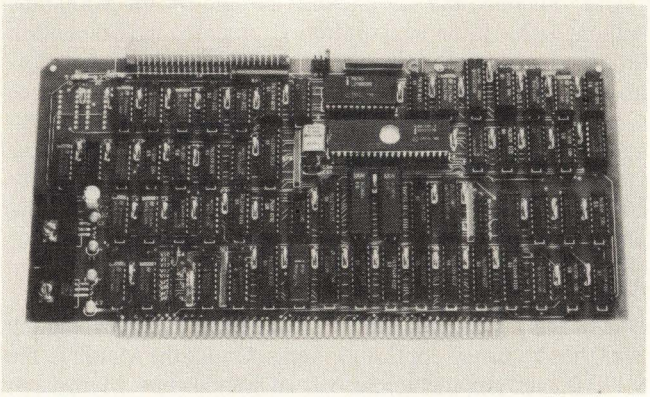
Enhancing systems performance through incorporating state-of-the art microprocessors onto CPU cards does, however, present some thorny problems for designers. This is due mainly to the fact that the S-100 was originally designed around the pin out of an Intel 8080 microprocessor, has its origins in the CP/M world and today market momentum is forcing it towards the 16-bit UNIX world.



Adaptec's ACB-5580 SMD rigid disk controller with SASI/ANSI SCSI support.



Adaptec's ACB-550 5¼" Winchester disk controller with SASI/ANSI SCSI support.



Adaptec's Intelligent host adapter, the AHA-1510, supports the S-100 bus.

Problem areas encountered when designing a 16-bit machine onto the S-100 include coordinating 8- and 16-bit data transfers, accommodating wait states, and generating status signals on the bus. Originally limited to a 64K address space, the S-100 bus now utilizes a 16 Mbyte addressing range. Under the new IEEE 696 standard, 24 lines on the S-100 are used for addresses, useful for accommodating newer microprocessors like Intel's 286 and National's 16032.

CompuPro's (Hayward, CA) latest CPU board based on the NS16032 includes the NS16082 memory management unit (MMU) to implement demand paged memory management. In a multi-user environment, each user has access to a 16 Mbyte virtual address space for his tasks.

Options such as the NS16081 floating point unit may make the board attractive to manufacturers of CAD/CAM equipment and multi-user software development houses. CompuPro has integrated the board into a multi-user system introduced at this year's NCC and will be offering the UNIX version 4 operating system, a C compiler, and Fortran.

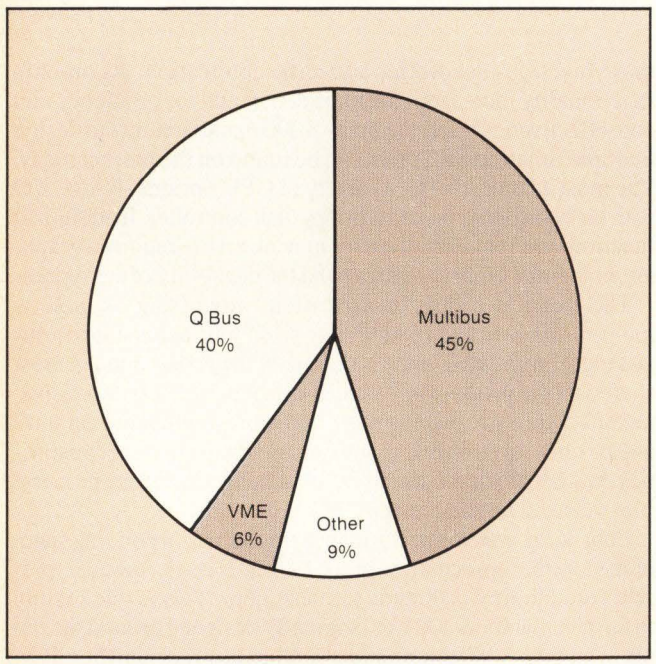


Figure 1: The 1983 Single Board Computer market shows how evident the concentration is on a few key architectures.

In the past, S-100 customers have included many people seeking a low-cost alternative to computer systems offered by Digital Equipment. As predicted, with DEC recently making the J-11 and T-11 microprocessors available to the market, many third parties are taking advantage of the large base of DEC software by introducing board level products based on the devices.

One of these, startup Abacus Technology Systems (Houston, TX) offers the PC11, an S-100 card based on the T-11 DEC microprocessor. Similar in performance to the PDP 11/03, the RT-11 operating system is provided as part of the package.

Rather than force the system integrator to choose one O/S standard or another, many manufacturers support both with unusual dual processor units (DPUs). Cromemco's (Mountain View, CA) DPU, for example, includes a 68000 for access to newer software and operating systems, plus a Z80 for compatibility with the large existing base of 8-bit software. In operation, the DPU switches back and forth between 8- and 16-bit data path widths according to the type of memory or I/O being accessed. Further, the full 16 Mbyte address space of the S-100 is supported directly by the 68000 and through a paging scheme, by the Z80A.

Designed as a replacement for systems using the MP/M 8/16 operating system, including CompuPro's CPU 8085/88, Macrotech's (Chatsworth, CA) new MI-286 CPU board features both the 286 and the Z80B processors.

The ability of the S-100 bus to support large amounts of main

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memory is one of its most important features. A number of reasons make this capability practical.

First, the bus is large enough (more than 21 slots) to hold the boards physically required for many Mbytes of RAM. Advanced processors are available that can handle multiple-Mbyte address spaces and operating systems, and languages are available that make use of the address space. Error correcting memory is available to make soft errors less worrisome.

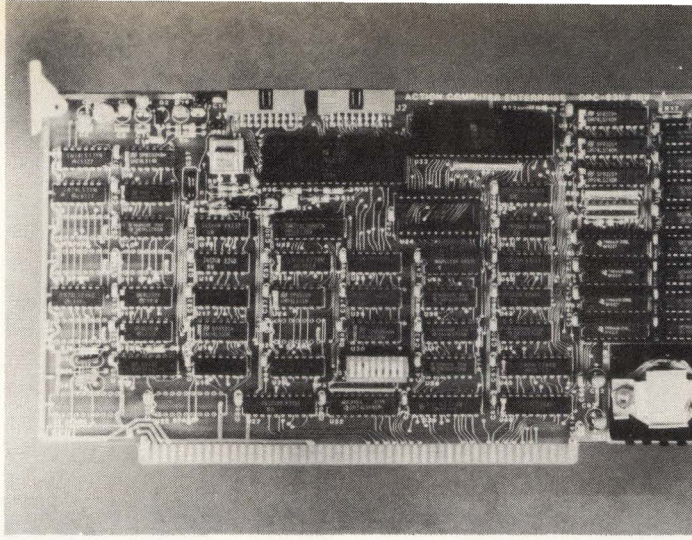
Dual processor units and large memory configurations are common features of S-100 multiuser systems. These commonly work in a master/slave relationship whereby each slave is dedicated to a single user and contains its own CPU and memory.

Such microcomputers are found in both conventional office and business environments and in other applications where the computer is part of a larger function, such as process control or scientific measurement. Although single-user desk top machines such as the IBM PC may be more economically designed using a "motherboard/expansion slot" approach, the S-100 bus still offers the ability to upgrade and enhance system performance more easily.

Operating Systems

In multiuser master/slave configurations, an operating system residing in the master manages system resources while each user has his own version of one of the popular operating systems, each as CP/M, Concurrent DOS, etc.

Action Computer Enterprises (Pasadena, CA), dpc/OS 3.0., for example, downloads CP/M Plus (or CP/M 2.2. or CP/M-86) to each of the user processors on the system. Any combination of the CP/M versions (8- or 16-bit) may run on the system concurrently. As the dpc/OS is transparent to the user, all the user sees is a pure CP/M environment. The processors supporting dpc/OS 3.0 and CP/M Plus are the dpc-183 and dpc-83u boards. The dpc-183 can serve as a user processor or, in conjunction with the dpc-100, as a service processor. The dpc-83 is a user only processor – a cost-effective alternative



The dpc-83u user processor from Action Computer Enterprise provides CP/M Plus in a multiuser multiprocessing environment.

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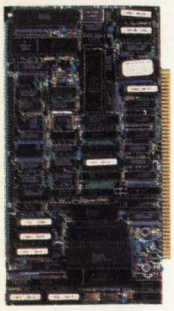
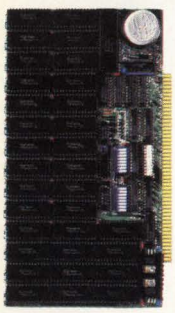


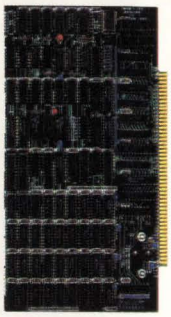
1 CPU 8/16

- Dual processors: 4MHz NSC800 (executes full Z80 instruction set) and 8MHz Intel 8088.
- Onboard floppy controller with 24-bit DMA. Runs up to four 5¼" or 8" floppies in any combination at the same time.
- 8K PROM monitor.
- 2 serial ports (software selectable up to 19.2K Baud.)
- Interrupt controller with 8 vectored interrupts.
- Real time clock interrupt.
- $895 (Manual only: $25)



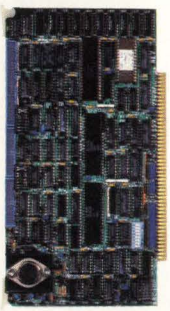
2 256K STATIC RAM/ TIME OF DAY

- Employs fully static CMOS memory chips.
- Accepts either 8-bit or 16-bit bus requests.
- Includes battery-backed-up time-of-day clock and calendar.
- IEEE-696/S-100 compatible.
- $1850 (Manual only: $25)



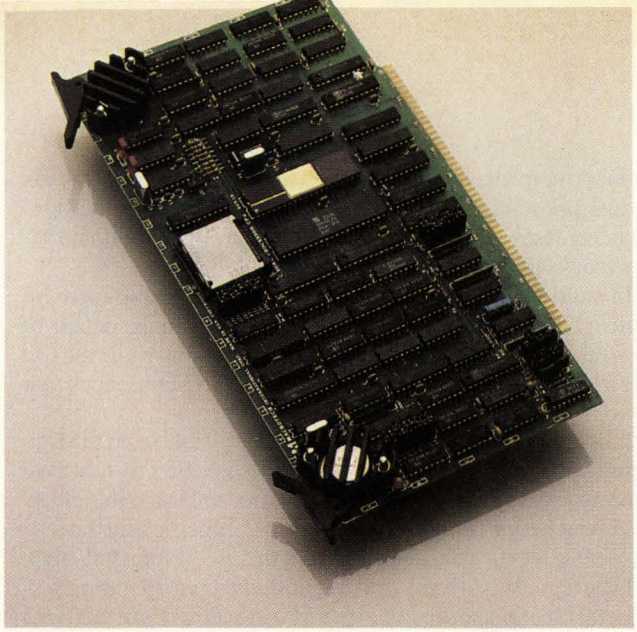
3 256K/512K/1MB/2MB DYNAMIC RAM

- Configurable as either dynamic RAM or as disk drive emulator.
- Accepts either 8-bit or 16-bit bus requests.
- Uses 256K chips for 1MB or 2MB configurations.
- 150ns. RAM chips.
- IEEE-696/S-100 compatible.
- Low as $850 (Manual only: $25)



4 SBC-300

- Single board computer able to perform as permanent bus master or slave processor.
- Z80* CPU: 4 or 6MHz.
- 64K of dual-ported RAM with parity.
- 2 to 16K bytes of PROM.
- System memory addressing to 16MB.
- Serial, parallel and counter/timer I/O.
- SASI port.
- Dual programmable serial full-duplex channels.
- Supports CP/M* Plus, MP/M* and TURBODOS.*
- $740 (Manual only: $25)



The MI-286 from Macrotech features the 286/10 and the Z80B.

to the dpc-183.

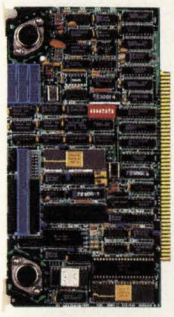
Another example, the MDZ/OS from Micro Mike's Inc. (Amarillo, TX) is a multi-user, multiprocessor operating system for use with Teletek's (Sacramento, CA) S-100 SBCs. This network supports as many as 16 users, each with an individual Z80A or Z80B processor, 64K of RAM, two serial ports, parallel ports, shared access to Winchester disks, printers and 5¼" or 8" floppy drives. Each user has in RAM an individual copy of CP/M-80 or MicroDOZ, a Northstar DOS-compatible operating system.

TurboDOS is yet another operating system that will allow 16 slaves per master to be interconnected on an S-100 bus. According to Intercontinental Microsystems (Anaheim, CA), TurboDOS will soon be CP/M, CP/M-86 and PC-DOS compatible. These sorts of systems do offer many advantages. Since all processors and peripheral controllers are normally mounted on the S-100 bus, all data transfers are parallel across the bus, rather than serial as with a network of PCs, enabling faster transfer rates.

Since all users can share common peripherals, the cost of a multi-user system is lowered. The common peripherals are usually connected to the master processor. Although a PC network can put a printer on each PC, the users cannot share these printers. On a TurboDOS network, however, printers can be put on the master as well as on the slaves, and all users can share all printers.

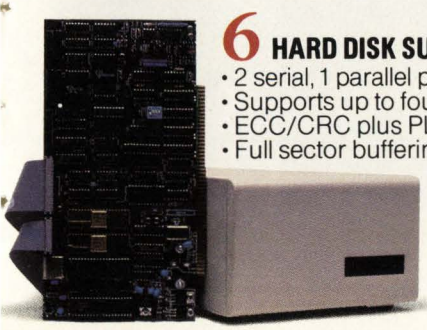
Furthermore, since all boards – master, slave, memory boards and peripheral controllers – are contained in a single chassis, each user only needs a terminal. Again, a less expensive approach than a personal computer at each workstation. Some slave boards on the market today will support more than one user, and some, like the Poly186 from Polymorphic Systems (Santa Barbara, CA), can function as either a stand-alone master card or a system slave board. The Poly-186 runs Concurrent

BOARDS



5 VFW-III

- Offers simultaneous control of up to three 5¼" Winchester drives (up to 16 heads) and four 5¼" and 8" floppy drives.
- Floppy drives may be single- or double-sided, single- or double-density.
- Data transfers under DMA or programmed I/O control.
- Phase lock loop data separator.
- 20-bit single and 4-bit double burst detection span on 256 byte sectors.
- $895 (Manual only: $25)



6 HARD DISK SUBSYSTEM

- 2 serial, 1 parallel port (IBM-PC* compatible).
- Supports up to four 5¼" Winchester drives.
- ECC/CRC plus PLL data separator.
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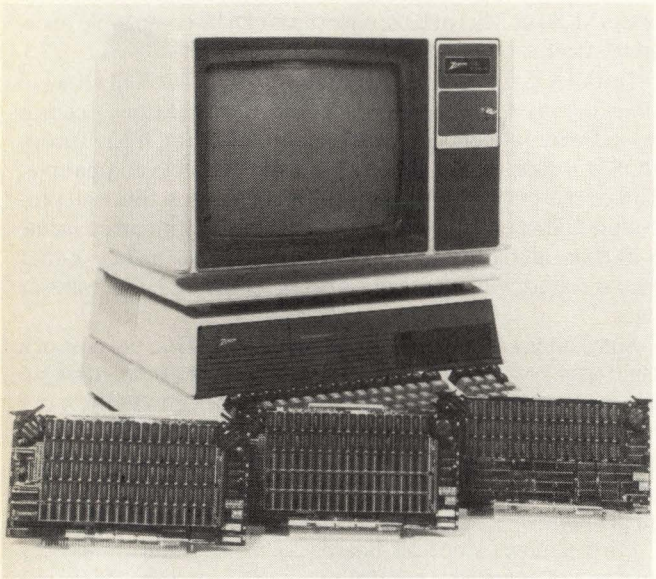


The Z-series from Macrotech International boosts the Zenith Z-100 microcomputer main memory up to a full Mbyte.

DOS, which is Digital Research Corporation's MS-DOS compatible operating system. Indeed, the S-100 vendors who can offer software compatibility with the PC may find themselves fighting back at IBM with a more flexible solution. Upcoming UNIX compatibility by the concurrent DOS operating system may give vendors even more clout in the marketplace.

Operating system support from a particular vendor is one vital factor to be given consideration when purchasing an S-100 board or system. The days when an assortment of cards could be purchased from a number of vendors and integrated by a design engineer appear to be limited, and today the purchase of an integrated subsystem appears to be a more common approach that takes a lot of the headaches out of the integration process.

Memory

Efforts to increase performance of disk and tape subsystems both in the single-user microcomputer and the multi-user computer systems arena has been the focus of large efforts by many manufacturers, primarily because it remains one area where system access times can still be dramatically improved.

New add-in memory boards from Macrotech (Chatsworth, CA), for example, are aimed to boost Zenith Z-100 microcomputers' 128K main memory to 1Mbyte, taking up only one slot in the Z-100's S-100 expansion bus. All the boards come with Macrocache, a software package on a 5¼" floppy that can provide both RAM disk emulation (virtual disk) and full cache memory capability. Through the Macrocache virtual disk feature, the Z-100 can address a user-specified portion of a Z-Series memory board as if it were a disk drive, enabling the add-on memory to stimulate a second or a third disk drive electronically. Virtual disk can speed up program execution significantly, especially where disk accesses are frequent.

Microcache software employs dynamic memory allocation in both virtual disk and cache memory modes. For example, the cache may act as an expanding and contracting buffer that responds automatically to changing virtual disk requirements. As virtual disk storage area increases, cache buffer size proportionally decreases, providing flexibility for programs with memory blocks of frequently varying sizes.

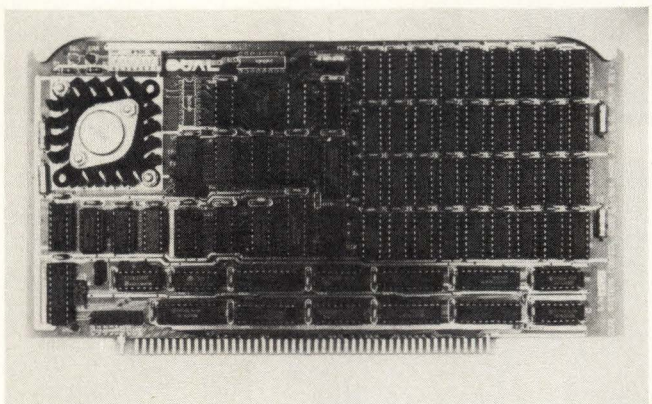
In multi-user systems, DMA is frequently used to increase system performance. The host CPU, freed from the details of disk access, may continue to execute instructions while the I/O operation is in progress, relieving the disk I/O bottleneck that constricts many multi-user systems.

In some cases, such as with the boards available from SD Systems (Dallas, TX), DMA transfers from disk directly to a slave processor can be accomplished. In addition to DMA, the STDC 5¼" Winchester Disk Controller from Cromemco further enhances system performance through the use of four full-track data buffers. When a sector is requested by the operating system, that sector and all other sectors on that track are read into one of the track buffers. The desired sector is then transferred to main memory, while the remaining sectors are retained inside the STDC until called for later by the operating system. When a new sector is requested, it can be delivered immediately. These "caches" of data appear to come from a very high speed disk drive. The STDC determines the degree of stagnation from the frequency with which each buffer has been accessed and the time interval since the last access.

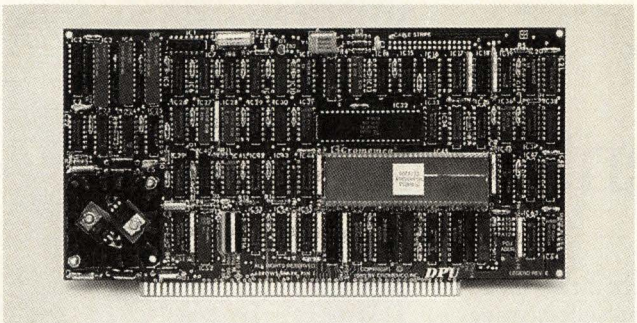
Disk Controllers

As virtual memory is finding its way onto microprocessors, disk capacity is increasing at a rapid rate and RAM prices continue to drop. The disk controller is becoming increasingly important with the push towards newer intelligent interfaces, such as the SCSI. Adaptec (Milpitas, CA) is one company that is spearheading the partitioning of intelligence at the disk subsystem.

Two boards currently available from the company function as a host adapter to the user's Multibus or S-100 bus system and an intelligent I/O controller. The ACB-5580 board is designed to support up to seven host CPUs through the SCSI bus and up to four SMD disk drives. It relieves the operating system from the task of managing shared disk functions in a networked system through a reserve/release command. This command maintains data integrity by merging multiple access to files. Moving these functions to the disk controller increases operating system speed and improves file sharing reliability, according to Adaptec.



Dual Systems (Berkeley, CA) 1 Mbyte RAM board makes use of 256 Kbit devices. Access time is 220 ns.



Cromemco's dual processor card features a 68000 and a Z80.

Two intelligent host adapters, the AHA-1510 (S-100) and ATTA-1530 (Multibus) may sit between the host bus and the SCSI and function as I/O processors working with the I/O supervisor of the operating system. Both support DMA access at 1-5 Mbytes/sec from the SCSI bus to the local memory of the host. These boards can handle up to eight concurrent I/O requests and increase the performance of multitasking computer systems by relieving the operating system of its I/O management duties.

Industrial Control

One of the problems most commonly encountered in the design of an industrial control system is the availability of boards suited for that function. The problem is compounded by the fact that most of these sorts of applications have very specific I/O requirements that may not be suited to general purpose off-the-shelf solutions. To make matters worse, most of the A/D converter houses such as Datel and Analog Devices have identified and built product for only the largest slice of the board market – the Multibus and the Q-bus. While analog and I/O board designs for newer buses such as the VME are taking off slowly, older bus structures such as the S-100 have been ignored by the larger companies. This has left many S-100 systems integrators with only two resorts – to build product themselves or to move to another bus structure. Some of those who chose the design approach, such as Kristoph Krug of Automated Control Systems (Somerville, MA) have even set up their own company to market the product after its completion.

Conclusion

Today, the incompatibility problems encountered in the early days of the S-100 bus appear to have been overcome, mainly due to the publication of the IEEE 69 specification. The market, however, remains a diverse product mix, with multi-user systems perhaps owning the largest chunk. Although the future of the bus itself may be short, many of those small systems companies currently basing products around the S-100 have enough flexibility and design expertise to maneuver around the problems encountered by the bus itself in their next generation designs.

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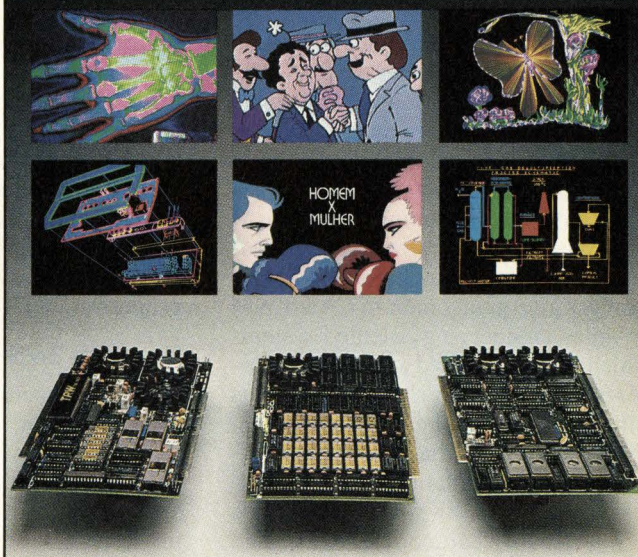

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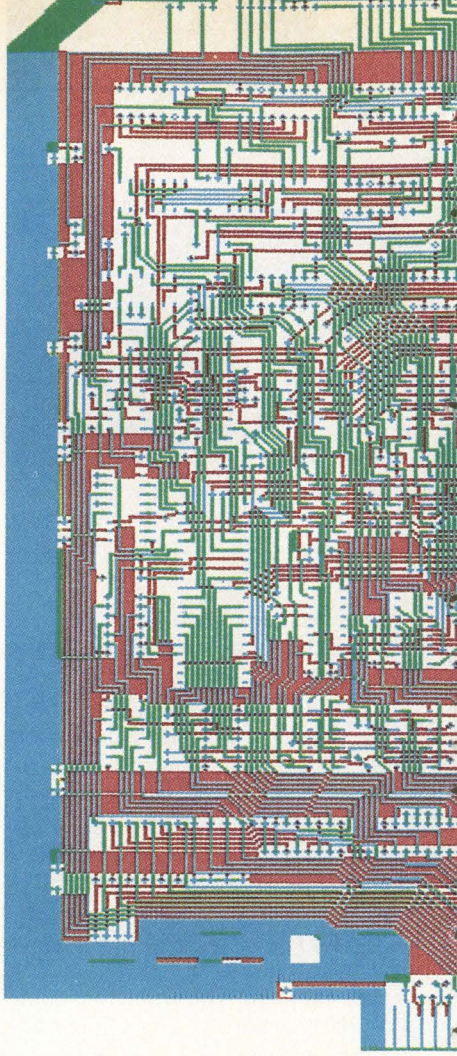
Color In Hardcopy Device Development



by Mike Cashman,
West Coast Technical Editor

Almost everyone who uses computers eventually wants and needs hardcopy, and hardcopy is almost always the final storage medium for information. This reliance on hardcopy is, in turn, helping to improve the medium through the use of color. The technique of using color to improve information communication isn't new. What is new, however, is its dramatic acceptance. Many hardcopy device vendors give great credit to CAD/CAM or other engineering oriented systems which were compelled to use color in order to make complex shapes and layouts (like printed circuit boards) intelligible. "There's no doubt that the dramatic increase in the installation of color monitors is paving the way for the acceptance of high-quality hardcopy devices," said Harry Watkins, Product Line Manager in Tektronix' Graphic Peripheral Products Division, (Wilsonville, OR) a thought echoed by Chuck Stires, Marketing Manager at Advanced Color Technology, Inc. (Chelmsford, MA). "Just recently, the installation rate of color terminals has overtaken that of monochrome displays. From now on, color will be the standard," added Watkins. Further underscoring this point is the prediction of the marketing research firm of International Resource Development (Norwalk, CT), that "color printer sales will rise to $4.1 billion in 1993, up from the 1984 figure of $750 million." These figures include plotters, which IRD predicts will account for the highest dollar volume share, but states that "honors in the units shipped category are expected to go to ink jet printers (35% of all shipments), and thermal transfer printers (32%)."

Products To Supply The Demand

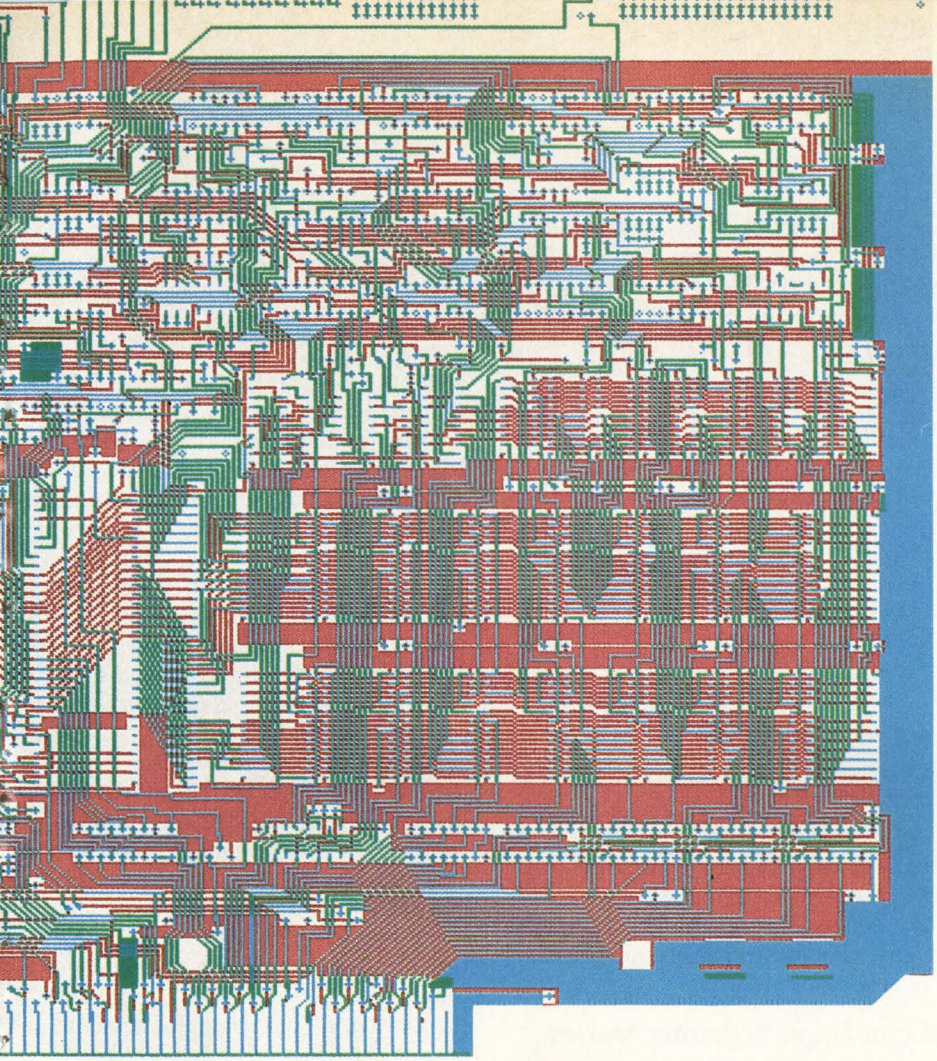
What most users or systems integrators are looking for is a low-cost, reliable, high-quality, easy-to-use hardcopy device. Ink jet and thermal transfer printing are the two major technologies manufacturers have settled on in an attempt to supply these somewhat mutually exclusive device attributes.

Ink jet technology has been around, by some estimates, as long as 30 years. One of the special allures of this technology all along was user friendliness, before that term became popular. Spraying ink doesn't make much noise, so here was a technology that would be very acceptable. Early ink jet technology was so primitive it created a built-in bias regarding its ultimate suitability among many systems integrators.

The two chronic problems over the years have been clogging and smearing problems. If too much (or too slow drying) ink is deposited on the paper, it smears. If smaller orifice jets are used to control the ink quantity, the printer tends to clog. Quicker drying water-based inks were good for copy quality, but tended to clog more than solvent-based inks.

Like so many technologies, however, designers have not give up on the problems. At the National Computer Graphics Association exposition in Anaheim, CA this May, a reasonable effort was made to smear the newly completed output of every ink jet printer at the show

Figure 1: Tektronix' 4510 color graphics rasterizer and the 4692, an ink jet plotter. The 4510 accepts images as high-level graphics commands and converts them to 4692 compatible data. The 4692 sprays more than 20,000 ink droplets per second by its four ink jet heads.



What most users or system's integrators are looking for is a low-cost, reliable, high-quality easy-to-use hardcopy device.

Figure 2: An example of output from the ACT[II] color printer from Advanced Color Technology.

Figure 3: The new model 8050 dot matrix printer from Dataproducts can print words, numbers and graphics with high resolution.

without success. (This was, in every case, when the ink jet product was writing on paper.) While this technology looked questionable for generating letters a decade ago, what it does routinely now in a wide variety of colors is remarkable.

An example of the refinement of the ink jet hardcopy device is the just announced 4692 by Tektronix. The pedigree of this system is interesting. Tektronix' Watkins claims that when the company decided to enter the terminal image hardcopy market, it did so with an open mind regarding suitable technologies. The field narrowed to ink jet and thermal transfer. Ink jet was selected after surveys of users in four markets; CAD/CAM, business graphics, cartography, and scientific data analysis. The results showed that the number one selection criterion was copy quality. Tektronix' research convinced them that ink jet technology had better quality output potential. Working together with Matsushita on a Japanese-developed design led to the Tektronix 4691. The 4692 is the next generation product and is an all Tektronix design which contains some interesting features. Foremost among them is a feature for which a patent is pending called the Ink Transient Suppressor. It uses a five micron mesh filter to trap any bubbles or particles which enter into the ink paths. A one-way valve prevents ink from flowing away from the ink jet heads, and a flexible diaphragm, balanced by air on one side and ink on the other, suppresses shocks when the copier is moved or jolted. This is all done in an effort to eliminate bubbles and head clogs.

Trend Toward Resource Sharing

A companion for the 4692 (and already installed 4691's) is also being announced; the 4510 color graphics rasterizer. The 4510 accepts images as high-level graphics commands across an RS 232 interface and converts them to 4692 compatible data. In its smallest of three configurations, it processes 12,000 vectors and costs $4,495 (the top-of-the-line system at $9,995 processes 200,000 vectors). While the 4510 is costly, it does make possible resource sharing among terminals.

It also seems to tie the rasterizer and the 4692 hardcopy output device to a relatively low-cost graphics terminal. In this way, the end-user of the system could in many, if not most cases, work up acceptable quality images, and then have the ink jet or other hardcopy device generate much higher quality output. Tektronix' Watkins says this is a real possibility, but ACT's Marketing Manager Chuck Stires states that even though his firm's Chromajet ink jet products are designed to be used in this fashion, they are typically being sold one to a terminal. "Maybe we'll see that in the future, but we're not seeing it now."

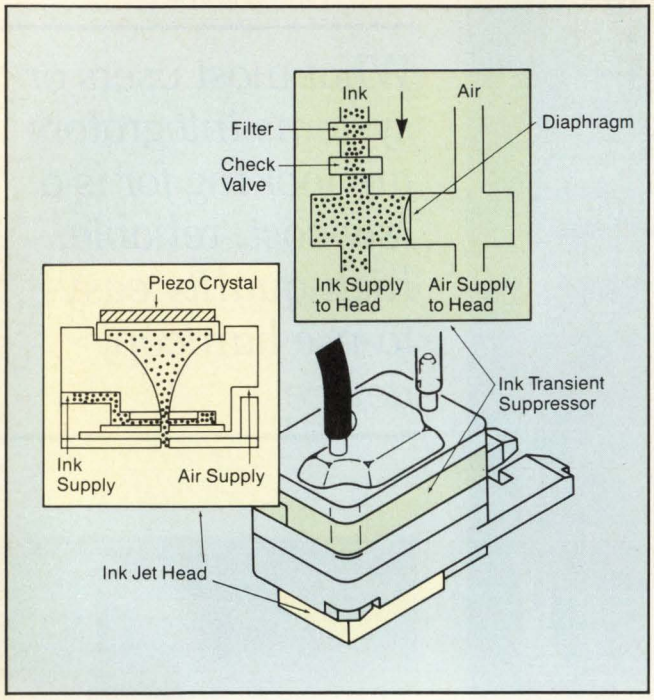


Figure 4: The ink transient suppressor from Tektronix uses a five micron mesh filter to trap bubbles and particles that may have worked their way into the ink system. A one-way valve prevents ink from flowing away from the ink jet heads, and a flexible diaphragm, exposed to air on one side and ink on the other, suppresses shock when the copier is jolted and moved.

Thermal Transfer

As much as any other, thermal transfer technology is related to electrostatic printer/plotters. A typical design is the CH5201 from Seiko Instruments. A dense row of print heads (150 per inch) is selectively addressed and raised to 70°C through a transfer sheet coated with dry ink. This approach does away with clogging concerns, but has a few of its own. Each transfer (or doner) sheet is good for one copy, regardless of the density of the image, and copies cost about $.30 for paper. (Transparencies can also be processed.) And doner sheets, with their images of the finished plot, could potentially be a disposal problem in an increasingly security conscious world. Still, the technology is proven, quiet, clean, and more reliable than ink jets have been until now.

Color Impacts Printer Market

So pervasive is the preference for color hardcopy that it has even affected the impact printer. "I can't quite believe that color printing is a strong need yet, but it is a strong want. And we're selling more of these than we ever thought we would," said a spokesman at Anadex (Camarillo, CA). This type of product, the high-performance, color capable, serial printer is seen as the new high-end for these devices. Anadex claims that the color dot-matrix printer is not often the first printer a company acquires for a system. "More often, it's the second printer, after the users find out how much they rely on hardcopy, and what color can do for their interpretation of information."

Anadex' DP9725B Color/Scribe uses a multiple pass and overlaying technique to achieve a variety of colors. Resolution approaches that of many of the thermal transfer and ink jet devices (at up to 144 dots per inch), but neither the quality nor the price ($1,625) compare. Still, for many users, even this level of graphics capability would more than suffice. One nice design feature is the 9725B's printing sequence. Software control always prints from light to dark colors to prevent (or at least minimize) color contamination of the ribbon.

For even higher performance, there's the Trilog COLORPLOT[II]. This is a 300 line per minute unit that uses a three-color ribbon and two rows of printheads to obtain color graphics output for many non-graphics critical applications. One interesting feature in the Trilog (Irvine, CA) printer/plotter is two rows of print heads. If one row should fail, a user can flip a switch which enables the device to operate at half-speed until help arrives.

Monochrome Printer Graphics

For low-cost hardcopy printer graphics, the approach taken by Analog Technology Corp. (Irwindale, CA) is to develop intelligent controllers that can be inserted into two familiar printer products, the Texas Instrument 810 and the C. Itoh matrix shuttle printer. The controller board makes these printers compatible with Tektronix Plot 10[R] compatible software. There are selectable raster sizes up to 1584 × 1024 dots, and resolution values from 72 to 240 dots per inch, still preserving the original functions of the TI 810 for less than $500.

One thing is clear. The continuing preference for color computer images and output will keep designers busy thinking of even more innovative products that are bound to arrive in the near future. □

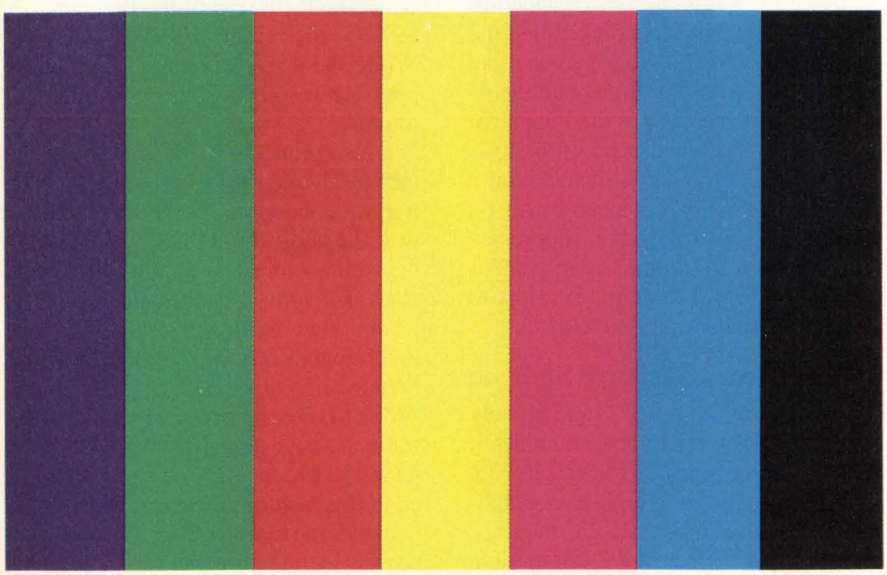


Figure 5: This test pattern was generated on the Tektronix 4692 color graphics copier.

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In-Circuit Programming: A Solution To Several Design Problems

by Michael McGee

Since the introduction of the PROM and EPROM, equipment optimized for programming these devices has evolved. When first introduced, the PROM and EPROM were primarily design tools used by the engineer in the development of ROMs, and the programming equipment was made for use in the engineering lab, and with the needs of the designer in mind. The first commercially-available PROM programmers introduced in 1971 allowed the programming of single devices. The PROM was inserted in a zero-insertion force socket, then programmed with software stored in punched paper tape. Next came units that programmed PROMs from other PROMs, or from a host computer, eliminating the need for libraries of paper tape, a fairly cumbersome storage medium. Improvements made to the earlier PROM programmers were intended to make the job of the design engineer easier.

As the cost of the PROM and EPROM dropped, it became cost-effective for manufacturers to install such devices in equipment shipped to the customer. Thus, the EPROM, while still an effective design tool, became a key ingredient in the manufacture of many high-technology products. The high volume of PROM and EPROM devices required by increasing manufacturing levels soon overburdened the standard programmer units and led to the invention and introduction of the "gang" programmers, a variation of the earlier models. The first of these units allowed the programming of eight devices in parallel. Later generations of programmers allow automated programming of devices so that entire tubes of PROMs and EPROMs can be programmed without the need to install each device in a socket on the programmer.

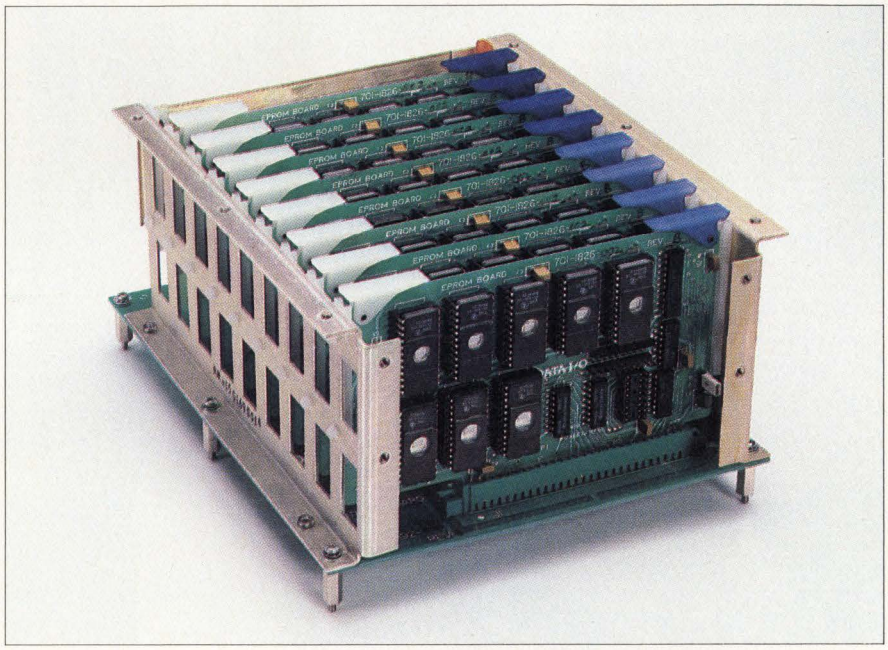

Figure 1: Data I/O's interface fixture holds up to eight circuit boards for simultaneous programming.

In-Circuit Programming

The introduction of the EPROM onto the manufacturing floor from the design lab was just the first stage of its evolution. The second stage resulted from new industry-wide trends in the use of EPROMs, three of which became immediately apparent. 1) As designers continue to move computerization into critical applications requiring high reliability, EPROMs have become a staple in all types of military and aviation equipment, with each device soldered-in to overcome vibration problems. 2) Space-saving packages such as flat packs and leadless chip carriers have become more popular for high-density circuits. 3) "Memory modules" – nonstandard, specially designed memory units containing multiple devices – are used in areas where standard EPROM packaging would be impractical.

Although today's market is filled with programmers of various sizes, capabilities, and prices, all of them program PROMs and EPROMs only prior to installation. However, many trends in EPROM usage do not lend themselves to off-the-board programming, causing the designer to sometimes compromise design for manufacturability.

The alternative to off-the-board programming is in-circuit programming. In this method of programming, though standard programming algorithms are used, but programming signals are not routed to discrete devices installed on the

Michael McGee, a free-lance technical writer, has spent 18 years documenting high-technology equipment for such manufacturers as Ampex Corporation, John Fluke, Bell & Howell, Qantel Corporation, and a host of others.

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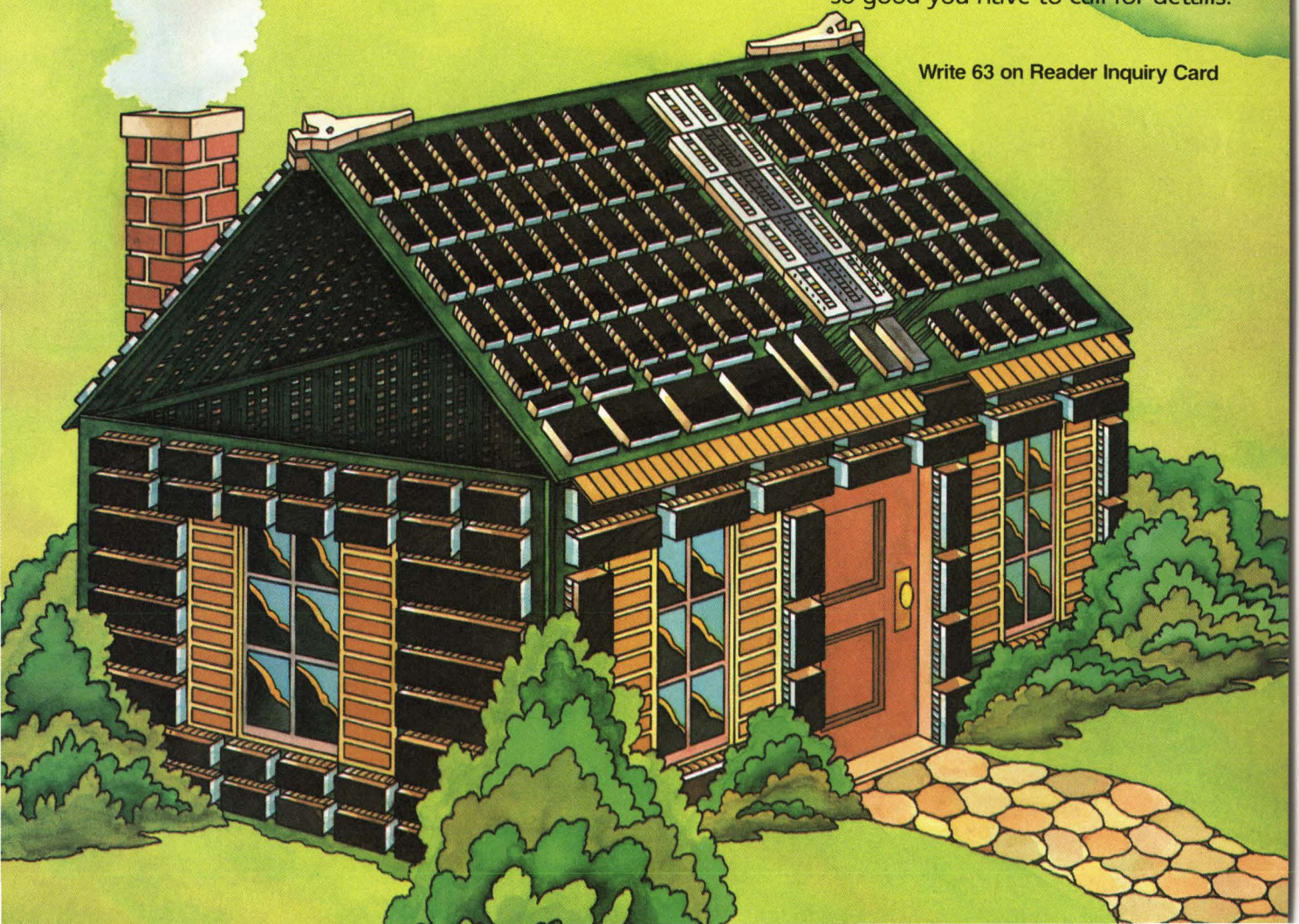

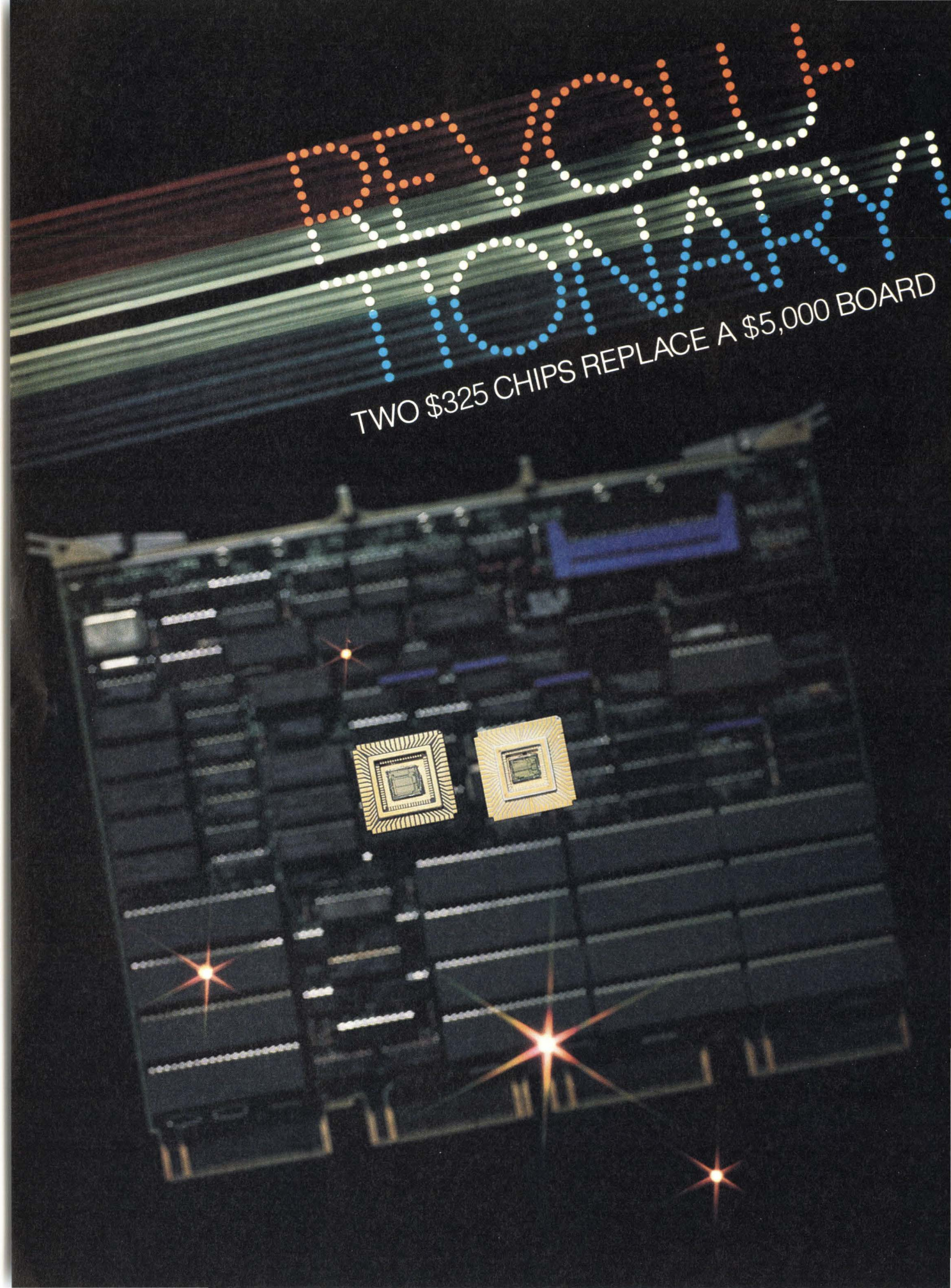
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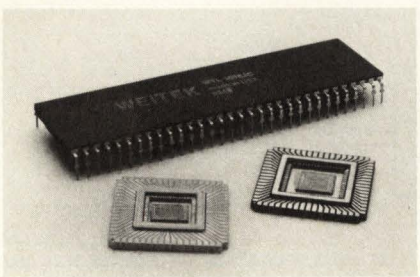

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Designers can now specify leadless chip carriers to solve lack-of-real-estate problems, hybrids for unusual packaging applications, and soldered-in parts for improved product reliability.

The new generation of in-circuit programmers makes changes between programmable boards as easy as changing adapter bases. (Photo courtesy Data I/O).

programmer, but to EPROMs and PROMs mounted on complete circuit boards. In-circuit programming allows the installation of blank EPROMs and PROMs on the printed circuit board. After complete assembly, the entire board is programmed so that each EPROM and PROM device, either soldered-in or installed in a socket, receives the appropriate program code. Electrical access to the board by the programming equipment is made via the circuit board connector and an interface fixture.

Thus far, two basic types of in-circuit programmers have been developed. Original systems provided a fixed interface that allowed the programming of a single type of board. These systems were usually a costly result of a manufacturing company's attempts to improve product reliability and manufacturability (and possibly test its design expertise) by fabricating a specially-configured piece of equipment. While the "customized" in-circuit programmer may have solved some of the manufacturing problems when it was finally engineered and built, its lack of flexibility prevented its use as an effective tool for programming a variety of circuit boards. Furthermore, this in-circuit programmer typically suffered from poor documentation and inadequate support in addition to the need for extensive modification to accommodate a change in boards to be programmed.

The second generation system is not custom-built, but is a production unit designed to program virtually any size and type of printed circuit board. This system is equipped with a flexible interface that allows the programming of such boards. With the second-generation system, the programmer manufacturer provides an interface connector. But since the programmer manufacturer does not specify the sizes and connector configurations of the user's boards, the user supplies the interface fixture that contains the boards to be programmed.

In a sense, the second-generation programmer is a "gang programmer" since it programs several whole boards in a single parallel operation. The user simply places up to eight boards in the interface fixture, mounts the interface fixture on the interface connector, calls up the appropriate "board profile," and initiates the programming operation. The in-circuit programmer proceeds to check the integrity of each EPROM and PROM device, and when all check okay, proceeds to program each device on each board simultaneously, in a single operation. While in-circuit programming itself does not involve the designer directly, it may allow the use of EPROMs, leadless chip carriers, and hybrid devices in the board design.

In-Circuit Programming Of Memory Boards

Until now, the basic idea behind building memory boards, or modules, has always been to dedicate personnel to the programming of the individual EPROMs, and then have other personnel stuff them individually into the circuit boards at some later point in the manufacturing process. In this manufacturing method, all programmed EPROMs must be kept in inventory awaiting use. Later, they are requisitioned from inventory for installation into the product, where they are subject to such common phenomena as bent pins, part number mix-up, destruction or damage due to static discharge, etc.

Consider programming a production run of memory boards, each containing eight EPROMs. Previously, each device had to be programmed as a discrete item then segregated into one of eight separate bins. Later, after much handling, each device had to be placed in its designated location on each board in the run, where it was either soldered in (to save the cost of a socket or increase reliability) or installed in a socket. In either case, each device had to be placed in its correct loca-

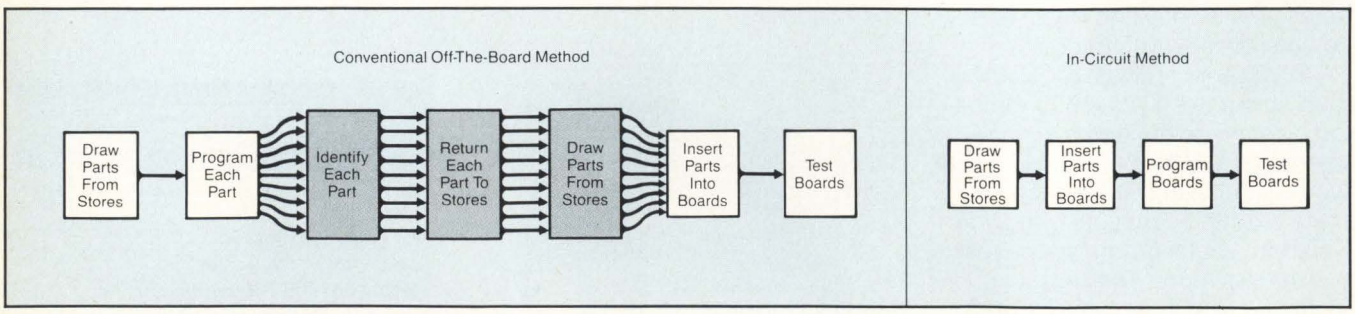

Figure 2: Comparing the manufacturing steps required for the off-the-board and in-circuit programming methods.

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Elements Of The In-Circuit Programmer

The second-generation in-circuit programmer is typified by the Data I/O Model 156A. The functional arrangement of this programmer, initially configured to program up to eight boards at a time, is shown in the accompanying block diagram.

The in-circuit programmer is essentially a computer system consisting of a CPU, a terminal, hard and floppy disk drives, programmable power supplies, a host computer port, 32-line address and data buses, and control/status line buses. Control of the programmer is a function of the CPU, which is in turn operated by means of the video terminal/keyboard. Sophisticated control software is maintained on the Winchester drive and is supplied by the manufacturer as part of the system.

The in-circuit programmer allows EPROM/PROM data to be loaded from any of four different sources: 1) A floppy diskette; 2) the Winchester drive; 3) a host computer; and 4) a pre-programmed board. Once loaded, the data can be saved on disk and recalled for future use. In addition, program data can be copied from any source to any other source as required to create and maintain data files.

To operate the in-circuit programmer, the boards to be programmed are installed in the interface fixture. This custom fixture is connected to the interface connector, a flexible interface that allows endless variations of circuit board architecture (up to 32 data lines, up to 32 address lines, and all required control signals). All signals are buffered within the interface connector, and additional space is provided on the buffer board for customizing signals.

Up to eight fully-loaded circuit boards are placed in the interface fixture and instructions appear on the video display. The operator keys in the name of the board profile to define the bus architecture, EPROM address and data assignments, EPROM type, and other necessary information regarding the board to be programmed. During every phase of operation, the system video display provides user-friendly prompting for the operator. After answering a few questions defining whether all, or just a part, of the boards are to be programmed, the operator can leave the in-circuit to operate unattended.

Figure 1: The Data I/O Model 156A In-Circuit Programming System.

Throughout the programming process, the programmer constantly checks for programming accuracy. Devices are given a blank check and illegal-bit check before they're programmed. Protection is provided from overcurrent, overvoltage, undervoltage and power line failures during programming. After programming, the programmer performs up to a three-pass verification of the programmed data with user selected Vcc levels. Finally, accurate programming is double-checked by both checksum and cyclic redundancy check calculations of the programmed data.

tion on each board, without error or damage, if the product was to function.

With the second-generation in-circuit programmer, this whole process is eliminated. All that is required when building a memory board using in-circuit programming techniques is to stuff blank devices into the board, insert the board (along with other boards of the same type) into the programmer interface fixture, and command the programmer to begin. The programmer checks and programs all specified programmable devices, and then checks each device to insure that all programming was completed correctly.

Reprogramming the EPROM

As designers turn more frequently to the soldered-in technique for mounting EPROMs, in order to gain reliability in more adverse environments, the problem of updating the EPROM becomes even more significant. Soldered-in devices are being used in increasing numbers in mili-

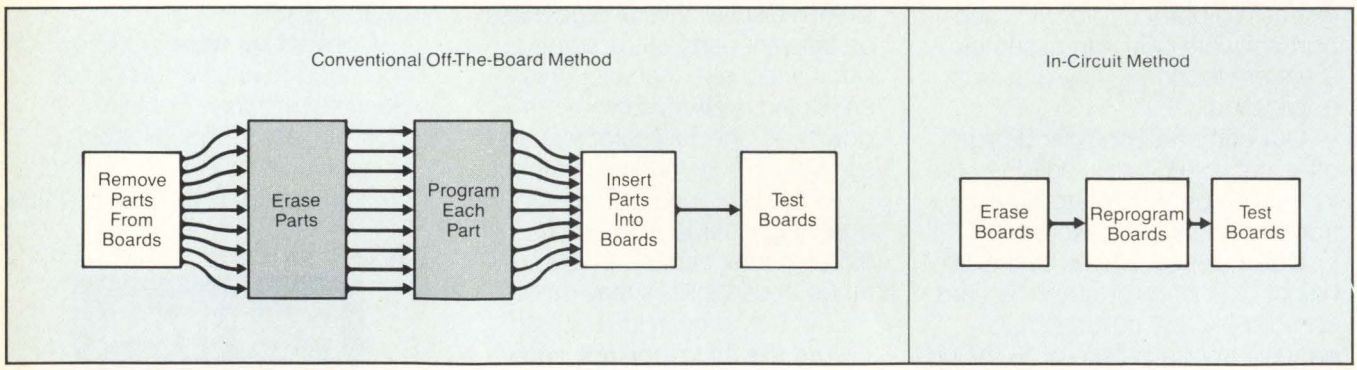

Figure 3: Reprogramming memory boards, comparing off-the-board method to in-circuit method.

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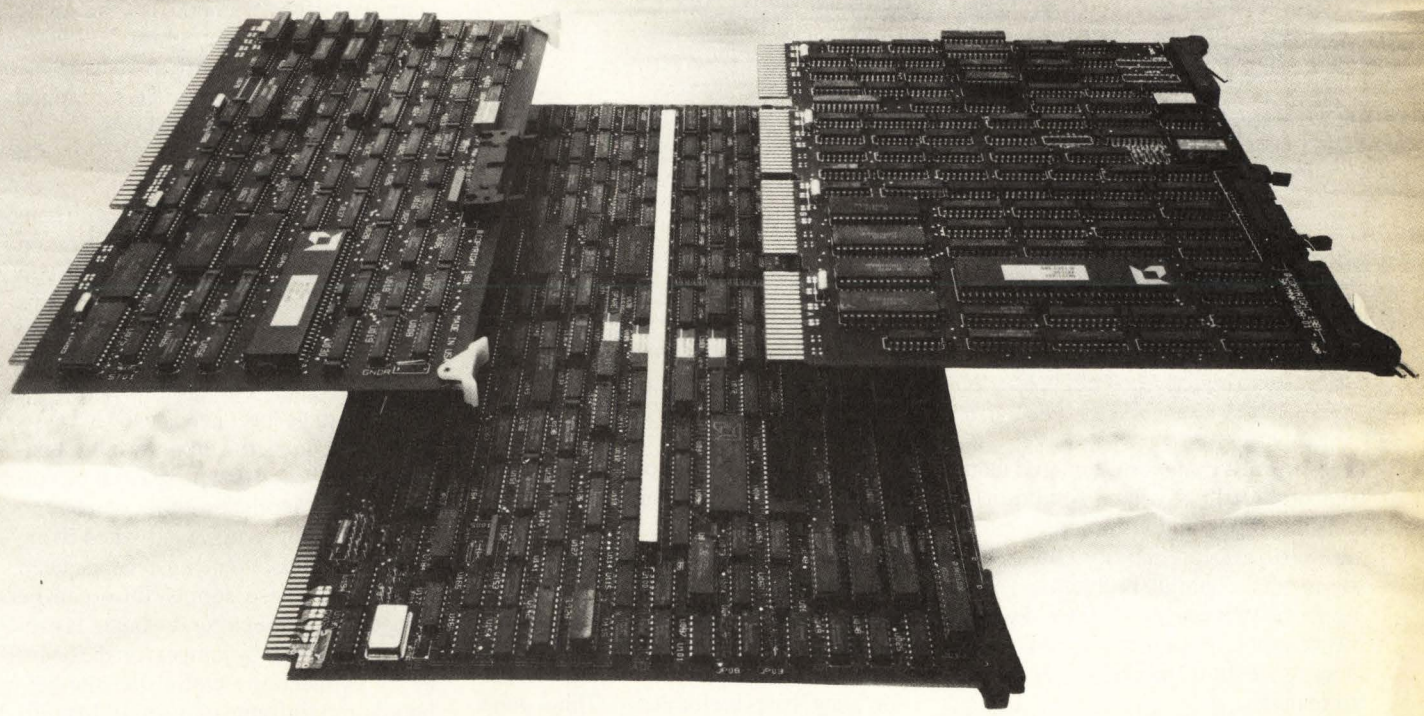

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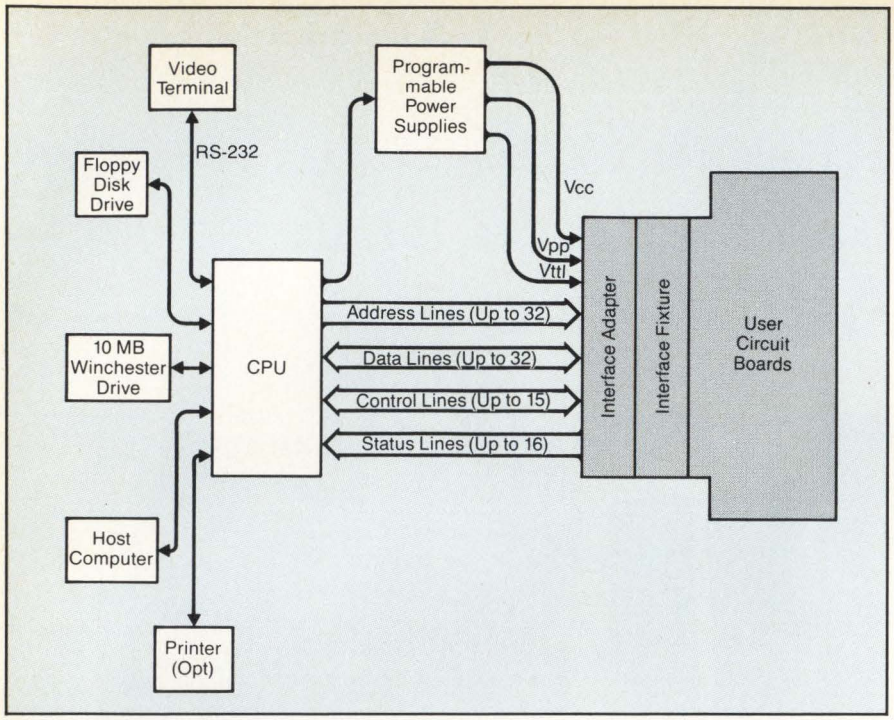

Figure 4: Block diagram illustrates the internal structure of the in-circuit programming system.

tary, aircraft, transportation, and industrial applications where conditions of constant shock and vibration cannot be allowed to affect reliability. Often, while solving the reliability problem by soldering-in the previously-socketed device, a problem of reprogramming the device to incorporate future product enhancements is created.

In the past, the way to reprogram a circuit board containing soldered-in EPROMs was to desolder each device and remove it from the circuit board. The next step was to discard or reprogram the obsolete device(s). In either case, each had to be resoldered back into its correct position on the board. Since desoldering and soldering requires an adequate amount of heat, damage to the board and the device can occur.

Side Benefits

Before the designer makes a decision between off-the-board and in-circuit programming for a particular board (or series of boards), some benefits of the in-circuit method should be considered. The labor required to program memory boards using the in-circuit technique is a fraction of that demanded by the conventional method where each device is individually or "gang" programmed. This time savings is primarily due to the elimination of man-hours spent programming EPROMs on an individual or "gang" basis prior to assembly in the product.

While labor savings are due in part to the fact that all devices on several boards are programmed simultaneously, they are also due to the elimination of several other common manufacturing problems. First, the need to handle each device as a separate part number in the assembly process is eliminated. Second, the need to program each device on an individual or "gang" basis is eliminated. Third, gone is the possibility of inserting EPROM and PROM devices in wrong sockets (all devices are blank when the board is stuffed), a major concern in critical applications such as guidance and control systems, avionics, transportation, etc. Incorrect insertion can mean increased cost due to the rework required to fix stuffing errors. In addition, the use of blank devices also eliminates the need for a large inventory of preprogrammed parts, that not only must be stored separately, but must also be properly identified. The latter usually means that someone has to take the time to write and affix small labels to each device to help insure that no mix-up occurs in the stores or parts departments.

For many manufacturing operations, the cost-effectiveness of in-circuit programming is evident. For the designer, the benefits may be less obvious. In-circuit programming lets the engineer base the design of memory boards on system considerations rather than on limitations imposed by off-the-board programming. For boards used in critical environments, EPROMs can be soldered-in for reliability without making reprogramming difficult. If maximum board density is the greatest consideration, leadless chip carrier packages can be installed during the manufacturing process and the entire board can be programmed. If the design is such that system software needs to be changed often, a board can be erased under ultraviolet light and then completely reprogrammed in one operation. With in-circuit programming, the only limitations to the design of memory boards are those imposed by the designer. Also, the ability to program and reprogram EPROMs right on the board is particularly valuable where unique packaging calls for limited access for removal of EPROMs.

Design Considerations

In-circuit programming is rich with benefits, but not without some consideration toward the design of the printed circuit boards. While the design considerations are real, they are neither expensive to implement nor mysterious to the experienced designer. For instance, each required voltage level needs to be accessible at the connector. Vpp must be separated from Vcc so that programming voltage can be applied without damage to sensitive components; and when using fast algorithms, Vcc must be isolated from Vttl. These supply lines can be jumpered together after the board is programmed, either by jumpers on the board or by connections within the motherboard or mainframe of the unit. In addition, the EPROM control lines, such as PGM, OE and CE need to be accessible at the connector during in-circuit programming.

Most EPROM manufacturers recommend the connection of decoupling capacitors to the Vpp input of each device. The value of this capacitor is determined from the manufacturer's specifications for the device. A typical value is 0.01 μF, which is sufficient to shunt the inductive spike that results from interrupting the current on the Vpp inputs.

Finally, any devices connected to the data bus should be placed in the high-impedance (tri-state) condition during in-circuit programming. The in-circuit programmer takes care of tri-stating the devices as long as the control inputs are accessible at the edge of the board. □

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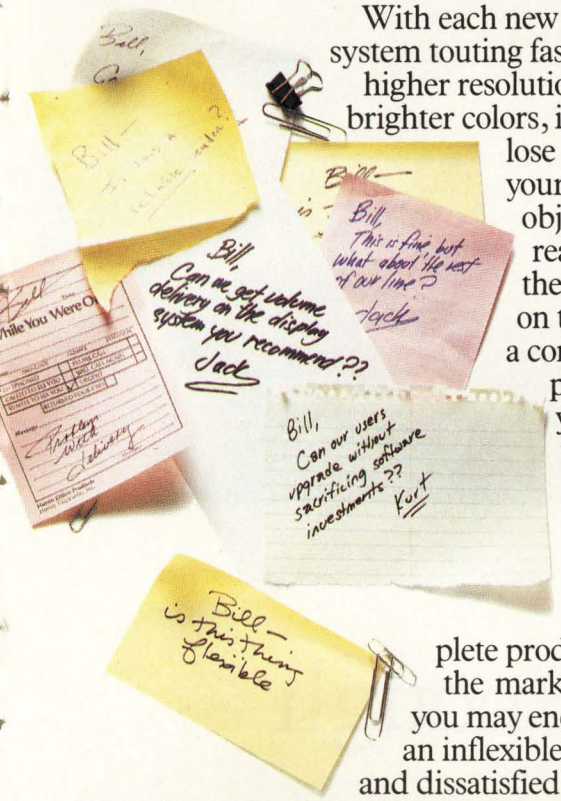
HOW THE LEX 90 TURNS PIXELS AND BITS INTO DOLLARS AND CENTS.



With each new display system touting faster speeds, higher resolutions and brighter colors, it's easy to lose sight of your primary objective—reaching the market on time with a competitive product. If you're late, you may lose valuable market share. Rush an incomplete product onto the market, and you may end up with an inflexible system and dissatisfied users.

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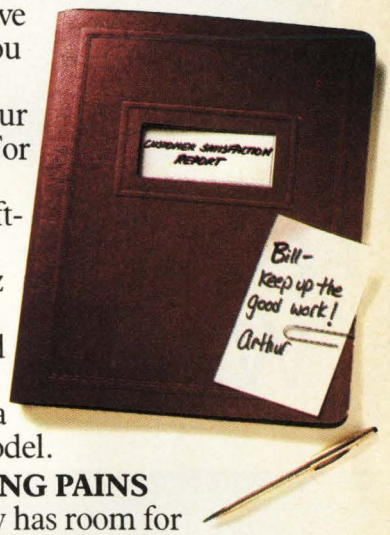

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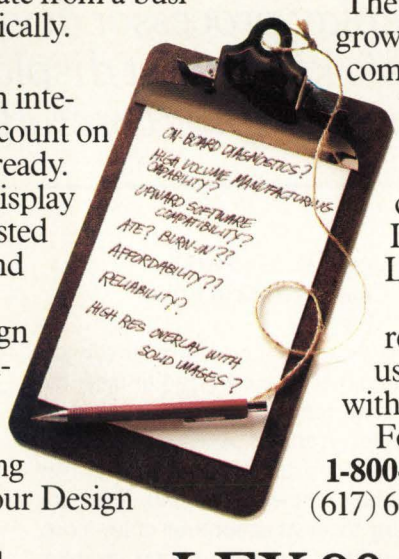

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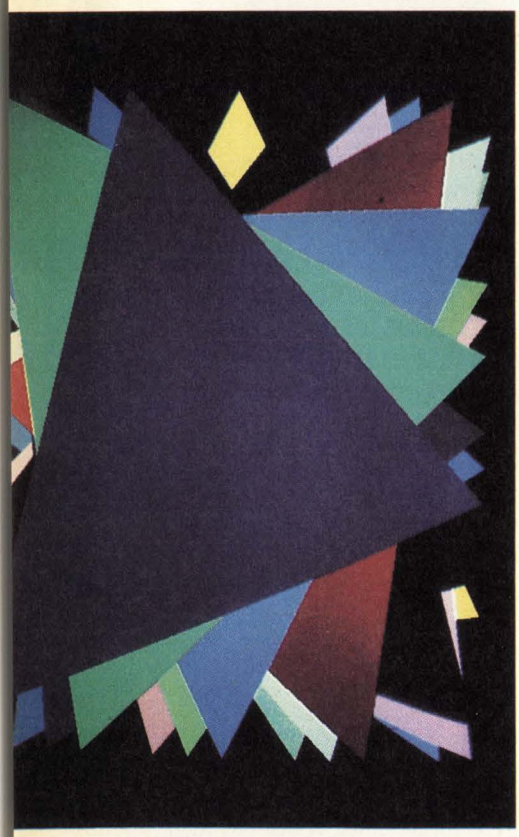
Display Processors — Where Fast Isn't Fast Enough



Display processor devices come in two basic kinds: fast display drivers and smart graphic controllers.

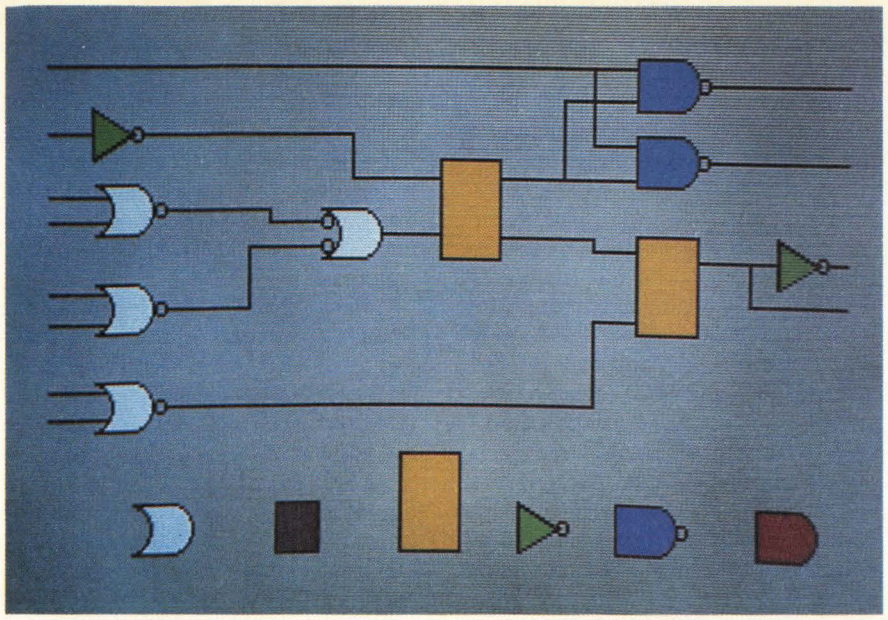
by Gregory E. MacNicol,
West Coast Technical Editor

Recently some new display processor technologies have emerged to meet the increasing demand for high performance computer graphics systems. These advances offer graphics designers an ever increasing choice of possibilities for creating the next generation of low cost, high performance computer graphic systems.

Some of the most powerful features now available in display processing include: use of array processors in boards and/or subsystems; Direct Memory Addressing of frame buffer memory; use of DACs and custom chips providing faster throughput; video-oriented memory with dual ports and wider width; onboard firmware functions providing callable functions from the host.

Bit-mapped raster graphic systems prevail as the most chosen method of high

Above: A single frame from a real-time (30 frames/second) flight simulation demonstrates XTAR Electronics, Inc.'s VLSI GMP chip set's applicability to simulation and animation systems. Left: Sixteen triangles, each equal to one-half the screen area, are drawn in less than one frame time at 60 frames/second, illustrating the drawing speed of XTAR's GMP based graphics systems.



The Motorola RMS chip set has been designed to work with the 6809 and 68000 microprocessors.

performance display processing. Vector graphics systems and raster scan conversion systems have to contend with many technical and economic problems.

Display processor devices come in two basic kinds: fast display drivers and smart graphics controllers.

Display drivers drive monitors very quickly, have few commands, and rely on the smarts of a host to execute their functions.

Intelligent display controllers, however, have large command sets, often over 100 words, with advanced graphics functions like polygon fill, pan, 3-D perspective control, smooth zoom, and video scan rate changing.

Some new systems combine the best of both worlds, having speed and intelligence. Parallax (Sunnyvale, CA), for example, makes a 16 color board that draws at 12 million pixels/second. Its 85 commands include sophisticated functions like run length encoding and smooth zoom and pan. The board comes in either Q-bus or Multibus configurations.

Though speed and intelligence are important in evaluating a display processor, they aren't the only benchmarks of performance. A designer or system integrator has a choice between a board or subsystem approach. Boards are powerful, offering easy expandability and freedom from the constraints of a particular microprocessor. Memory or special functions can also be easily added, creating greater power for a graphic system. But these added advantages increase software overhead – a costly factor.

The subsystem approach offers greater simplicity, where special display processor components are interfaced with a popular computer such as a VAX, PDP-11, NOVA or ECLIPSE by means of parallel and/or serial ports.

The trend in display processors is to introduce more and more features on graphics subsystems, creating greater performance rather than lower prices.

There is an increased demand for sophisticated display processing capabilities, but there have not been many significant improvements in the quality of important peripheral devices. The design of a high resolution color monitor for a reasonable cost is more than challenging. Problems in drive electronics, yoke design, convergence, CRT design, and electromagnetic interference are compounded by a shortage of analog designers.

Trends

The pressure for better display processors has stimulated the development of lower cost, higher performance units that are easier to use. These units use the latest in VLSI technology, including video display controllers, video memory chips, and multi-processor support.

Overall, three trends dominate the graphics processing arena: use of bit-slice devices or dedicated microprocessors, implementation of VLSI controllers, and better use of memory.

Architecture

The two most popular methods of graphics control, bit-slice processors and VLSI controllers, have advantages and disadvantages. While bit-slice processors have fast execution speed, programming time can be long. Graphics controller chips, on the other hand, offer simplicity in exchange for versatility.

A number of novel architecture schemes have recently been developed that offer surprising display processing power. The use of bit-slice processors, multiple processors or sophisticated hardware/software schemes have led to common drawing rates of 12 million pixels/second.

Memory

Graphics displays depend on memory. As a result, much attention is focused on graphics memory technology, where speed, control and cost are of primary importance. The demand is so great that memory manufacturers are responding to graphics designers with better chips and better support.

The single data refresh path of the 64K × 1 RAMs is a bottleneck for reading and writing to bit-mapped displays. One solution is the use of wide words or high granularity. When chips are organized as 16 × 4, memory can be expanded in 16 Kbyte increments (two chips) because of the 4-bit (½ byte) output. The wide word organization approach also saves power because a single byte can be obtained by enabling two chips, not eight as in the 64K × 1 organization scheme.

Another solution to the bottleneck is the use of 16K static RAMs. Their superior speed allows fast access time during wasted horizontal retrace periods. SRAMs also require less support circuitry and do not require "precharge." Although they remain expensive, new INMOS developments promise lower SRAM prices and better performance, as well as on-board 4-bit cache memory.

The great demand for graphics memory support has pressured chip manufacturers to produce dedicated video RAM devices. Texas Instruments (Houston, TX) introduced a 64K × 1 dynamic RAM with an on-chip 256-bit shift register and fast bulk data store designed specifically for video applications. The TMS 4161 multi-port memory provides two ports that eliminate memory contention problems while reducing hardware support circuitry.

While the 256-bit register of the TMS 4161 allows better bit plane performance, it does not allow for a convenient method

of cascading the shift register, nor does it provide proper shift control via the pixel clock. Systems that require hardware pan and zoom will not be able to utilize the TI component without forfeiting some performance.

8K × 8K iRAMs from Intel (Mountain View, CA) are yet another memory option. Unlike pseudo-static or quasi-static RAM devices, which only incorporate a portion of refresh circuitry on a chip, iRAMs integrate all the components of a dynamic RAM system on a single device. The 8- bit wide memory provides many advantages over single data paths. Interleaving of CPU cycles with video timing allows unrestricted access to the memory during both horizontal and vertical blanking periods, permitting real-time screen updating.

An interesting development is memory modules where four or eight 64K RAMs are piggybacked for dense, single board applications. Such configurations are appearing in single board plug-ins for desktop computers.

Inexpensive memory devices have also spawned new graphic techniques, like 'double buffering,' where one frame is displayed while another is being updated. A method of increasing memory plane transfer rates, one-bit plane contains the currently displayed image while its twin is used for writing to and updating. When finished with calculations, the two planes are swapped. This procedure alleviates the interference and time constraints normally incurred during the updating process. Memory, however, doubles.

Graphics design is not based solely on the price of RAM. Double buffering, static column decoding, nibble mode and integrated shift registers are attempts at creating "smarter" memory. The interactive dynamics of memory, architecture, cost and performance are paramount in the creation of display processors.

VLSI

As manufacturers scramble to make inexpensive, fast and available memories, impressive developments are happening in graphics VLSI, primarily in three areas: video control ICs, dedicated graphics engines, and single chip controllers.

Video control ICs provide memory control for graphics data prior to reaching the high speed digital to analog converters. Where speed is critical, these controller chips simplify design and retain fast data rates while reducing board space.

Intelligent engines are relatively new. Here, VLSI devices are used to control specific graphics functions such as shading or rotating an image. These powerful chips or chip sets are being offered as ICs or boards.

More impact on reducing graphics processor cost has been made by single chip graphics controllers, most notably the NEC 7220, second sourced by the Intel 82720.

The strength of the 7220 lies in its ability to handle three major graphic functions. It generates the basic video raster timing including all sync and blanking signals. It controls video display memory and data movement. Third, it calculates addresses in display memory, pixel by pixel, at 80ns per pixel, as drawing progresses in real-time.

Vectrix (Greensboro, NC) is one company using the 7220 with inexpensive 64K RAMs to create an inexpensive but powerful graphics processor. Combined with the processing power of an 8088, the VX 384 can display 512 colors at 480 × 672 resolution. It has a command list of 80 words. Vectrix has also introduced the Midas board for the IBM PC with all the features of the VX 384.

Other companies, like Genisco (Costa Mesa, CA), combine the bit-slice architecture of AMD's 2901 with two 7220s. With a cycle time of 150ns and 55 instructions, typical instruction time is between two and four cycles.

VLSI chips like the 7220 have their limitations, however. Memory writing can only be performed during retrace or blanking, putting a speed limit on display output. Primitives such as circle generation may be slow enough to warrant rewriting code. Nonetheless, the 7220 is a graphic milestone, and a sign of graphics chips to come.

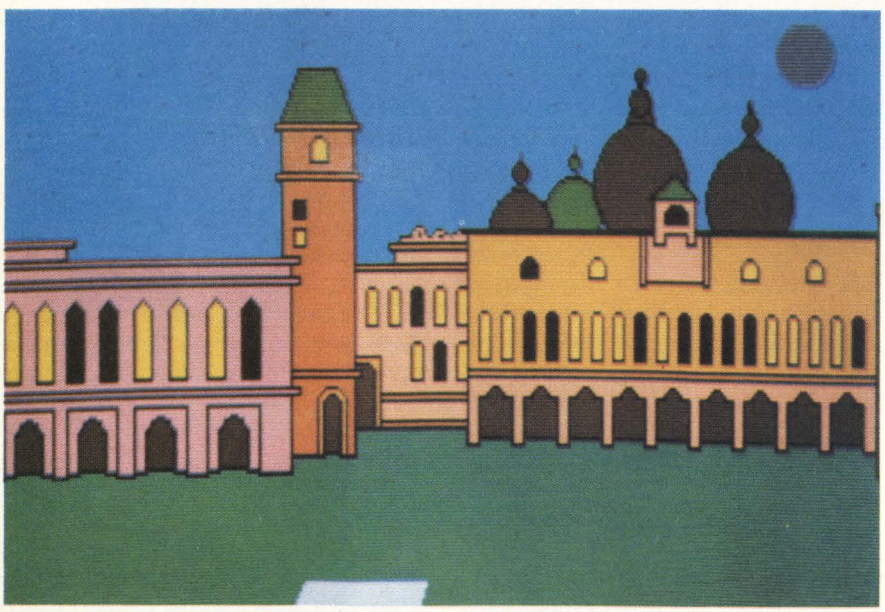
Another chip is the CF9367 graphics display processor from Thomson-CSF (Conoga Park, CA). Currently, over 15 companies have adopted the CF9367 over the NEC 7220. The chip is geared primarily for the video market, with the output interlaced at 525 vertical lines.

In addition, the 9367 is faster and less expensive than the 7220, has no limitation of memory planes, has an on-board character generator, and addresses twice the word size of the 7220.

Recently, two firms have introduced VLSI products that are significantly ahead of existing hardware. Weitek (Sunnyvale, CA) offers two new products, the WTE 7000 Graphics Engine and the WTE 6000 Tiling Engine. They are designed to augment the capability of minicomputers for real-time 3-D applications in the OEM market and are available in boards or chip format.

The Tiling Engine is capable of calculating and displaying a shaded object in 5-6 seconds. Three chips and three functions make this possible; a polygon to pixel converter, a function generator, and an address generator. So far, a handful of graphics processor companies are incorporating the Tiling Engine for CAD and solid modeling.

IGC (Hauppauge, NY) uses Weitek's chips for simulation of 3-D objects. A



The RMS chip set can simultaneously display up to 32 colors from a palette of 4096.

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Easy To Integrate

Parallax's high-performance series of graphics controllers let OEMs and system integrators add astonishing graphics power to standard microcomputers — Multibus and Q-bus controllers are available now.

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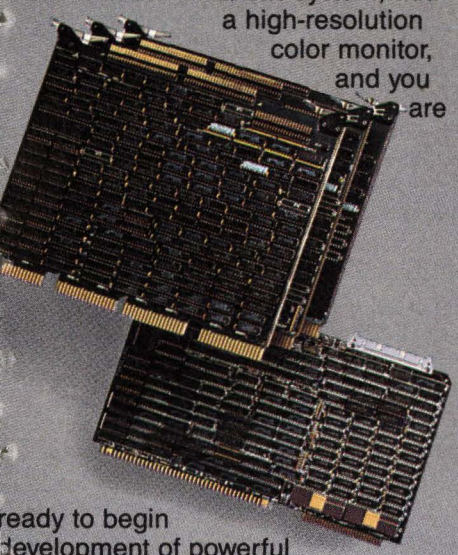

ready to begin development of powerful graphics applications.

The Parallax graphics controllers also give you the advantages of low power consumption, light weight — and with their advanced board-level designs, provide a price/performance ratio that is ideal for individual graphics workstations.

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With drawing speeds of up to 88 million pixels per second, you get more productive interactivity between the operator and your microcomputer graphics system.

- The Series 600 single-board controllers draw at 12 million pixels per second.
- The high performance Series 1000 board-set controllers draw at 88 million pixels per second, with Block Image Transfers (BLIT) at 14 million pixels per second.

"...drawing speeds of up to 88 million pixels per second."

With immediate interactivity, applications such as animation, CAD/CAM, on-screen page make-up, and business graphics are easier to work with, simply because images and graphics appear instantly on screen — and can be changed just as quickly.

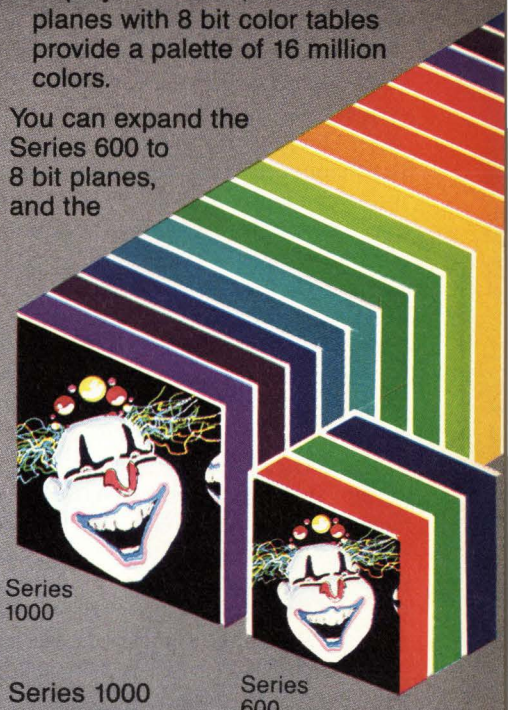
Parallax's rich instruction set provides single-instruction Polygon, Box, Circle and Vector drawing, Solid Fill, Outline, Stipple, Block Image Transfer, Opaque/Transparent, standard and user-defined Text modes, vector Dejagging — and the list goes on.

High Resolution

1024 x 1024, 60 Hz non-interlaced display is yours with Parallax's high-performance graphics controllers.

- The Series 600 provides 640 x 480 display resolution; standard 4 bit planes provide 16 colors from a palette of 4096 colors.
- The Series 1000 provides 1024 x 1024, 60 Hz non-interlaced display resolution; standard 4 bit planes with 8 bit color tables provide a palette of 16 million colors.

You can expand the Series 600 to 8 bit planes, and the



Series 1000

Series 600

Series 1000 is expandable to 24 bit planes. Other standard Parallax features include double buffering, smooth pan, and integer zoom along either axis — Parallax controllers have a long list of features that mean high performance graphics power for your microcomputer system.

Contact Parallax Graphics today. We'll be glad to draw a clear picture of all the advantages OEMs get with our graphics controllers.

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Calculating Clock Rate

A system's clock rate is an indication of the demand on hardware and software. Simple calculations give a designer a feeling for system requirements. Assuming a 60Hz rate, subtract 1.25ms for vertical blanking. That leaves 15.42ms for scanning 432 (visible) lines on the active portion of the display. Dividing 15.42ms by 432 lines gives 33.5μs/line, which is equivalent to a 28KHz horizontal scan rate. Horizontal retracing requires 7μs/line where the active portion of each line is 35.7μs. Subtract 7μs from 35.7μs leaves 28.7μs. 576 pixels are displayed during this time for a period of 28.7/576 or 49.8ns. This is equal to a 20.07 MHz system clock rate, fast for both memory and processor.

host computer downloads the matrix data and the chips enable fast rotation and image manipulation. The alternative would be for the host to pre-calculate the data for display.

XTAR Electronics, Inc., (Elk Grove, IL) announced a two-chip graphics controller capable of drawing filled-in polygons into a 1024 × 1024 frame buffer at an average speed of 136 million pixels per second. Called the GMP, or Graphics Microprocessor, the VLSI chip set executes specialized graphics instructions which are downloaded into a random access memory shared between the GMP and a host processor.

The GMP also draws points and lines at high speeds and can be interfaced to various size frame buffers from 256 × 256 × 1 to 2048 × 2048 × 32. The screen area that can be drawn in a given period of time remains relatively constant regardless of frame buffer size, so that no performance is lost when using high-resolution frame buffers. A programmable two-dimensional clipping window, automatic refresh of the shared display list memory and instructions which ease the drawing of polygonally-defined alphanumerics are additional features of the GMP.

Designed to ease the software overhead associated with high-performance graphics, the GMP instruction set allows the programmer to draw points, lines, and filled polygons merely by defining the screen coordinates of the point, line end points, or polygon vertices.

XTAR also announced a third chip called VSR, or Video Shift Register. An ancillary to the GMP, the VSR is used several times per system and interfaces the GMP to the frame buffer random access memory chips. In addition to reducing the chip count in a system, the VSR allows the host processor to read the frame buffer contents and provides features such as the filling of polygons with user-defined patterns and the ability to perform read-modify-write operations on the frame buffer memory.

A recent product from NEC will be a powerful entry in the graphics market. The μPD 7281D is a single chip non-Von Neumann processor with the image processing capability of a medium sized computer, about 5 million instructions per second. Among other functions, it will allow a graphics processor to rotate a 640 × 400 display in just 1.4 seconds.

The MC68487 and the MC 68486 from Motorola (Phoenix, AZ) make a two chip set for raster displays of 640 × 500. At 32 display colors from a palette of 4096, the raster memory system (RMS) allows virtual screen and display screen addressing as well as 160 characters in ROM. Designed to interface directly with the M6809 or M68000, it offers flexibility at low cost. Samples are due later this year.

Shadowed by single chip graphics controllers are a host of other video support chips. Signetics (Sunnyvale, CA) makes a programmable video timing controller (PVTC) and video attribute controller (VAC) that provides all the basic video control circuitry. This includes a 25 MHz shift register, control for the horizontal and vertical timing signals, and cursor format logic.

Innovative designers can mix some of these video control chips with high-resolution generators to make simplified, yet powerful graphics devices.

The capabilities of today's graphics processors are easily rivaling the performance of the more powerful image processors. As a result, system integrators have a large menu of choices when configuring a display processor. These choices, where each subsystem offers different specifications and capabilities, can be a confusing process. Here are some suggestions to keep in mind:

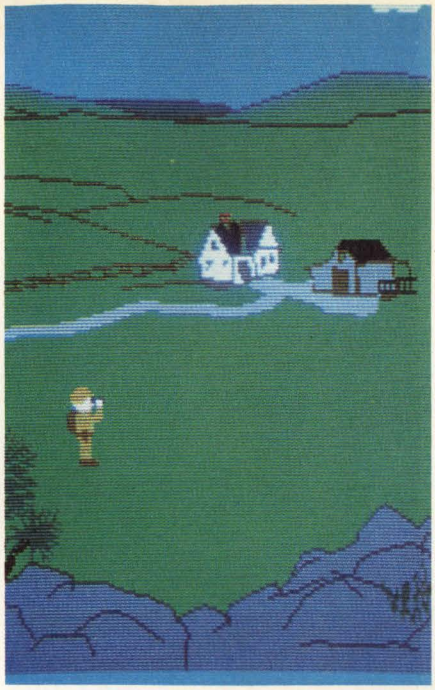
- Consider the interface to all units. "Standards" such as RS-170A are liberally interpreted. Sync may be separate, composite, on green or even inverted. A "black box" may be required.
- Determine the functional priorities. Do you need speed or smarts? And where do you need the speed; in processing or displaying the image? How many colors do you really need? Determine where the real bottleneck exists and resolve it with hardware or software.
- Look at expandability and upgradability. At some point it may be necessary to expand the capability of a board or box. Is this possible? At what cost in dollars and software time? Exactly how are cameras and peripherals added? Improper choice of a bus may preclude the specific expandability desired.
- Examine the software overhead in the total system. Sometimes savings in hardware becomes a burden in software. This may become expensive and lead to disaster. Find out what software is available and at what cost.
- Consider serviceability – Better systems offer on-board diagnostics. When a system is down, then what?
- Beware of demos. Demos are designed to amaze and delight, and to sell product. Stick with your original application and ask for a specific operational demo.

The Future

The latest VLSI developments include integrated functions, dedicated uses, ECL hybrids and floating-point devices. Anti-aliasing is being seen in hardware as well as software, and graphic primitives in addition to complex algorithms are being implemented on smaller systems. On-board data compaction techniques help with data transfer problems.

More impressive, though, is work being done on major graphics programs such as MOVIE.BYU on a chip. Research being conducted at North Carolina Microelectronics Center, for instance, is aiming at fast graphics processor chips that augment these smart functions.

Because software is becoming a major



Output from Motorola's MC68487 and MC68486.

investment to manufacturers, OEMs and end-users, a major standardization problem is surfacing.

An interface standard defining the way to use the capabilities of graphics peripherals allows an application program to drive a variety of devices. Interactive programming, such as dealing with graphics data over several layers, is another important focus for standardization.

Currently, few software standards are being followed. The lack of standards is also true with hardware, where different interpretations of I/O configurations, create problems for all users. Better peripherals such as monitors will be appearing soon, also as a result of dedicated linear CRT driver chips. In the land where fast isn't fast enough, each segment of display processing is improving dramatically. Regardless of architectures and processors used or what capabilities are implemented in firmware, graphics processors offer never-before-imagined performance and power. □

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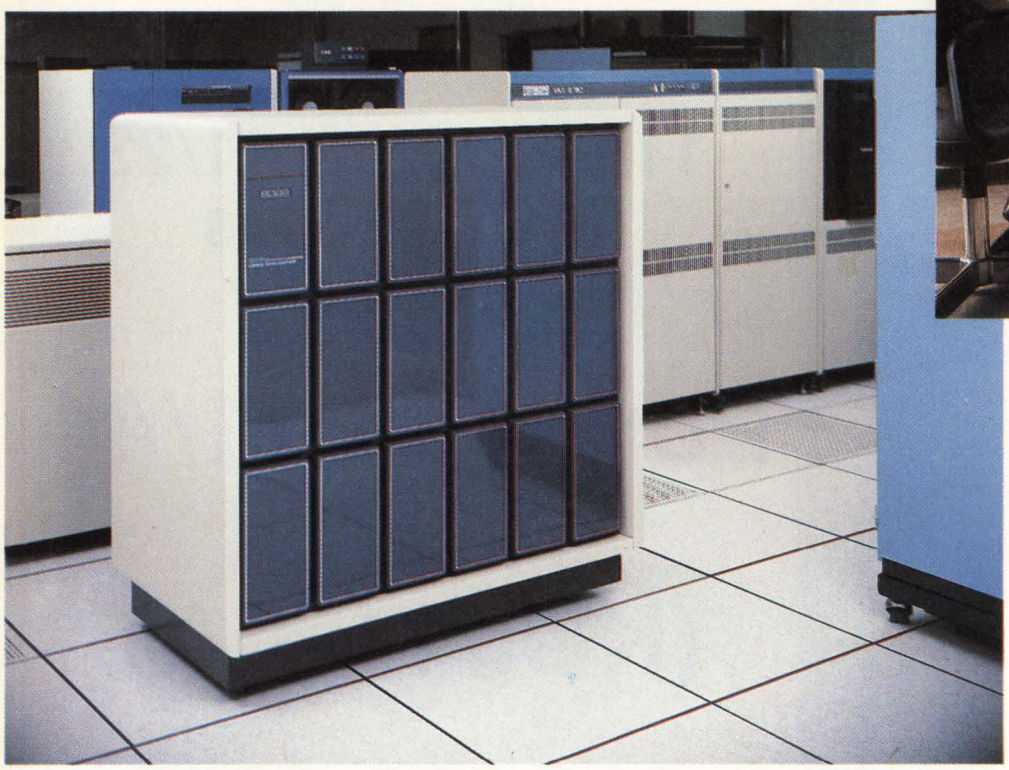
Tackling Design Environment Issues



Left: ZyCad's hardware simulator can perform logic simulations at speeds up to 16 million events/second. In comparison, the fastest software simulators (running on a mainframe) reach about 7000 events/second. Above: Daisy's Megalogician workstation includes a hardware simulator which can simulate logic at speeds up to 100,000 evaluations/second. Also shown, the physical modeling extension (PMX) allows actual VLSI chips to be plugged into the simulator so that software models of these larger components need not be developed.

Increasingly sophisticated workstations have sparked debate over whether to base the design environment on a mainframe or a network of self-contained workstations.

by Ronald Collett, Technical Editor

Over the next few years, most equipment manufacturers will be faced with the difficult chore of choosing a CAD/CAE environment to support system design. With the increasing density of VLSI devices and expanding system complexity, design tasks will undoubtedly require increased computer assistance. To remain competitive in the marketplace, OEMs must demand full utilization of both engineering manpower and design tools. If they are to achieve this goal, system architects must have the freedom to concentrate on design tasks as opposed to their CAD/CAE tools. While this may sound simple, the improved capabilities of self-contained workstations have created controversy over whether to base the CAD/CAE environment on: a large mainframe accessed by personal computers (equipped with some basic front end software such as schematic capture, netlist generation, etc.) or graphics terminals; a network of sophisticated workstations; or perhaps several intelligent workstations coupled to a mainframe. Equipping system architects with flexible CAD/CAE tools that can easily accommodate future needs is of primary importance when making the choice between the various design support systems.

As semi-custom, cell compiled and silicon compiled ICs replace off-the-shelf parts, greater design responsibility will be placed in the hands of the system architect. As an example, consider the differences between implementing a system with standard TTL parts and designing a system with semi-custom VLSI chips. With off-the-shelf parts, designers are absolved from responsibilities such as place-and-route tasks, design rule checks and mastering design nuances of a particular semi-custom IC vendor. Increasingly complex designs also force engineering teams to rely more heavily on both hardware and software design aids. With this in mind, the CAD system must provide engineers with a clear path to

designing chips, laying out boards and integrating systems.

Purchasing tools that will not be immediately outdated requires evaluation of both long and short term design support needs. It also demands that the OEM plan for future VLSI design techniques so that the tools will adequately support these new methodologies as they arrive. For instance, one may wish to consider whether the design environment should accommodate silicon compilation—the next generation of VLSI design techniques.

In short, system architects must ask several questions before making an investment in a CAD/CAE system. First, can the hardware perform the computationally intensive tasks (i.e. large simulations, automatic place and route for large circuits, etc.) in a timely manner? Alternatively, can the CAD/CAE system be easily linked to a larger host to perform these complex jobs? Is the system's hardware flexible enough to accommodate enhanced software for future upgrading? Given that the hardware is indeed flexible, can the CAD/CAE manufacturer provide the necessary software?

Most CAD/CAE suppliers will give a positive answer to these questions and in fact, they are usually quite honest. The issue, however, comes down to the degree of hardware flexibility, computational horsepower, software availability and the amount of effort a CAD/CAE vendor is putting into developing new software.

Unfortunately, vendors having the greatest marketing resources as opposed to the best product often end up the ultimate winners. Sorting through all the marketing hype is an important task when evaluating design support systems. The major CAD/CAE issues currently under debate concern which design tasks should be performed locally and which should be handled by the larger host computer.

Workstation Based Environments

Recently, some CAD/CAE workstation vendors have touted their 32-bit desktop computer systems as having computational capabilities commensurate with a DEC VAX or similar super minicomputer. Although some of the computational specifications are similar, these comparisons can be misleading since complete design solutions entail much more than brute computational horsepower (**Figure 1**).

Highly publicized MIPS (million instructions per second) values often cloud a lack of available software to carry a design from conception to prototype including project management. Some of the application software that potential workstation buyers should be concerned with includes: auto place and route; design management; executive management; testability assessment and fault grading (**Figure 2**).

The completely integrated nature of the workstation is one of its major strong-

Figure 1: A feature comparison of 32 bit computers.

Feature	DEC VAX-11/750	DEC VAX-11/780	Data General MV-8000	Apollo 660	HP 9030 (3 CPU's)
Maximum Physical Memory	8 Mbyte	32 Mbyte	4 Mbtye	4 Mbyte	2.5 Mbytes
Physical Address Range	512 Kbyte To 8 Mbyte	256 Kbyte To 8 Mbyte	256 Kbyte To 4 Mbyte	256 Kbyte To 4 Mbyte	128 Kbyte To 2.5 Mbytes
Logical Address Space	4.3 Gbyte	4.3 Gbyte	4.3 Gbyte	256 Mbyte	500 Mbytes
Maximum Program Size	2 Gbyte (32 Mbyte Supported)	2 Gbyte (32 Mbyte Supported)	512 Mbyte	256 Mbyte	500 Mbytes
Page Size	512 Bytes	512 Bytes	2 Kbyte Pages	1 Kbyte	1 Kbyte
Memory Access Time	800 ns	600 ns	440 ns	150 ns	550 ns
Memory Interleaving	No (One Controller)	Yes Two Way (Two Controllers)	Yes 4 Way	Separate Controllers	Separate Controllers
I/O Throughput	MI 5 Mbytes/Sec Massbus 2 Mbytes/Sec Unibus 1.5 Mbytes/Sec	SBI 13.3 Mbytes/Sec Massbus 2 MBytes/Sec Unibus 1.35 Mbytes/Sec	18.2 Mbytes/sec	10 Mbytes/Sec Multibus 1 Mbyte Burst Rate	5 Mbytes/Sec
Emulators	HASP 2780/3780 CPC 6000 20 Out	HASP 2780/3780 U1004 20 Out	HASP 2780 3780 3270	HASP 2780 3270 Domain	HASP 2780 3270
MIPS	.8	1.1	1.2	1.0	.8-2.3

Courtesy of Torric Corporation, Scottsdale, AZ

CAE Workstation	Computer	Hardware Configuration	Software Operating System	Communications Links To Other Computers	Local Application Programming	Hard Copy Support
Daisy	Intel 8086 And 8087 CPU Chips	Specially Designed Terminal Chassis And Peripheral Interfaces. Specific Hardware Additions Expand The System Capability Beyond Software Upgrades.	Specially Designed Disk Operating System Similar To Unix	RS232 ASCII Files	Fortran 77 Pascal PL-1	V80 Electrostatic Optional Plotter Support
Mentor	Apollo DN400	Each Terminal Supports A Motorola 68010 And Up To 4 Mbytes Memory And 300 Mbytes Disk. Terminals Are Connected In A 12 Mbytes/Sec Local Network.	Aegis Disk Operating System Similar To UNIX System III	HASP, 3270 Ethernet	Fortran 77 Pascal C	V80 Optional Plotter Support
Silvar Lisco	Apollo DN400	See Above	See Above	See Above	See Above	Optional Plotter Support
Metheus	Motorola 68000	Specially Designed Terminal. Chassis And Peripheral Interfaces.	UNIX	Ethernet	Fortran 77 Pascal C	Optional Plotter Support
Valid	Motorola 68000 Central Processor, 8086 Graphics Processor	Specially Designed Terminal Chassis And Peripheral Interfaces. 6 Mbytes Memory and 420 Mbytes Disk, IEEE 796 Multibus.	UNIX	RS449,RS232 Ethernet, Parallel	Fortran 77 Pascal C	Optional Plotter Support

Courtesy of Torric Corporation, Scottsdale, AZ

Figure 2: A comparison among these workstations indicates a trend toward UNIX and Ethernet.

points. Integrated systems reduce the chance of design errors and facilitate the design cycle while non-integrated CAD/CAE systems incorporating several vendor's equipment can increase the possibility of such errors. An integrated system allows the system architect to easily move data from one application program to another without being concerned with formatting the data. For example, moving from schematic capture to simulation to electrical rule checking would be transparent to the user on an integrated system. In contrast, if a schematic is captured using a non-integrated system, the user must be sure that the netlist is compatible with the logic simulator. Such non-transparent systems force the user to concentrate on the CAD/CAE tools as well as the design tasks.

Evaluating the workstation's operating system is a good place to start when choosing this type of design environment. The UNIX operating system seems to be emerging as a workstation de facto standard. The primary advantage of UNIX is the ease of software portability between machines and the increasing amount of software available. Since it runs on both workstations and larger computers, communications between the two is greatly facilitated when both are running under the same operating system. In addition, since design methodologies are usually organized in a hierarchical fashion, the hierarchical file structure of UNIX make it ideal for the design environment.

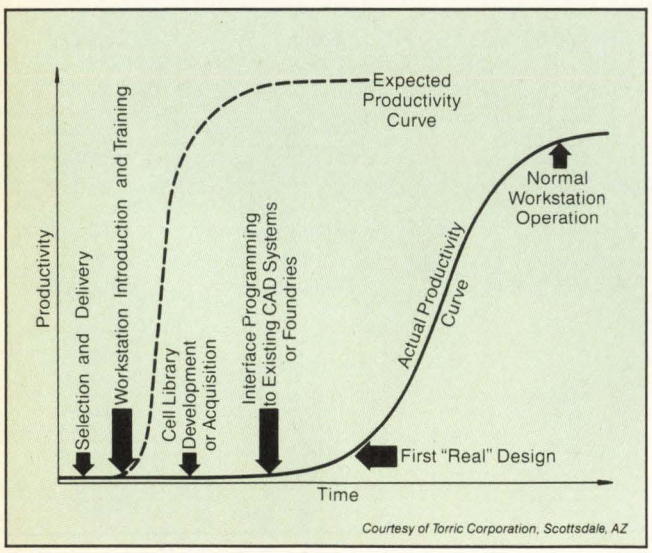


Figure 3: Workstation buyers should be aware that the time delay between the expected productivity and the actual curve can be as much as 12-14 months.

On the other hand, the processing inefficiency of UNIX makes it somewhat undesirable for I/O intensive tasks. Specifically, UNIX converts each bit of data to an equivalent 8-bit ASCII character. This means that the host computer needs eight times as much memory as well as eight times the bandwidth when compared to operating systems that handle data in a binary manner.

Most UNIX application programs are written under version 4.2 which supports virtual memory and networking. However, some programs are written under version V which supports neither of these. Unfortunately, once the UNIX V

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Universal Semiconductor's UNICAD I CAD system includes an IBM XT for schematic capture, netlist generation and local simulation. For larger simulation tasks, the PC can be linked to Universal's VAX.

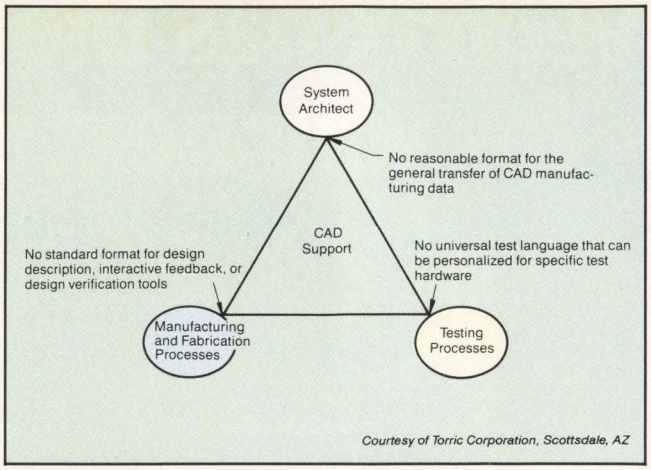

Figure 4: Three interfaces in the design environment that are presently lacking in definition.

kernel is altered to support virtual memory or networking, the operating system becomes hardware-dependent and incompatible with many computer systems. Consequently, the growing number of UNIX variations make it necessary to fully evaluate the feasibility of software portability between machines.

Presently, third party software is limited for workstations based on unique or less popular operating systems. As a result, users of such systems must rely primarily on the workstation vendor for software or be prepared to write their own.

Logic/analog simulation tasks are probably the most important functions performed by a CAD/CAE system. Unfortunately, most software simulators running on even the largest computers require excessive execution time and cannot adequately support system level simulations. Prompted by this inefficiency, some workstations include hardware dedicated to increasing the execution speed of simulation.

While there is little doubt as to the tremendous value of these hardware simulators, the real question is whether the cost of having one for each workstation can be justified when compared to purchasing one large dedicated hardware simulator which can be used as a central resource. For instance, a hardware simulator integrated with a workstation may sit idle when the engineer is not using the workstation for other design tasks. On the other hand, a simulator used as a central resource may be more efficient since all members of the design team can access it at anytime.

A solution to this inefficiency would be to allow the workstation's simulator to act as a central host, giving all members of the design team access. However, the local area network and all the necessary software supporting this configuration must be readily available from the workstation vendor. The decision of whether to use a distributed or centralized simulation environment should be based on the number of engineers performing logic/circuit simulation.

Workstation/Mainframe Environment

In a workstation/mainframe configuration, the user performs front-end tasks on the workstation and utilizes the host's resources for computationally intensive tasks. Although the cost of a mainframe is often prohibitive, leasing mainframe time via a time sharing network is a viable alternative. For most design projects, 80% to 90% of the computer costs will be attributed to simulation and fault grading. With this in mind, one can evaluate the magnitude of the design task and the associated cost-effectiveness of either buying or leasing a mainframe.

Although each design task requires a particular amount of computer horsepower, supporting the design cycle's front-end generally requires a workstation with a CPU speed around 1 MIPS coupled to a 40 Mbyte disk. Providing the user with a large amount of local storage reduces disk contention problems traditionally found in exclusively centralized storage environments. However, for larger design efforts that include several engineers, one should not neglect the importance of a centralized database as well as local storage capabilities.

As in any design environment, communications between resources is an absolute necessity. Without this basic function, it can be difficult to allocate design tasks to the proper resource. Consequently, to have an efficient workstation/mainframe environment, communication bottlenecks must be eliminated. If a particular design environment requires continuous interchange of data between nodes on the network, a file server may provide the best solution. Not only must the files be transferred, but to run on the mainframe, they must be in a format suitable for execution. Several committees have been established and are currently working towards developing a standard format for transporting design data (**Figure 4**).

To implement a workstation/mainframe environment, the buyer should carefully evaluate the communication link between the workstation and the host. First, the physical hardware supporting communication should be a commonly used network with a high bandwidth. It appears that Ethernet (10 Mbit/sec) is becoming a workstation network standard. However, unfamiliar users should not be deceived by the speed of this interface since effective throughput significantly drops (down to 1 Mbit/sec in some cases) when the higher level protocols are taken into account.

In most cases, the hardware of a network is well defined. However, standards are less defined for the higher level protocols. Higher level protocols should be scrutinized when the overall objective is to communicate with a host. These protocols should provide the ability to easily interface to the host you plan to use. If the workstation's protocols are not compati-

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ble with the host, a substantial programming effort may be necessary to simply move data back and forth.

A recent interview with a product manager of a large semiconductor supplier using several different workstations revealed that a major software development effort was required simply to transfer a circuit netlist between the workstations and the firm's host mainframe. This source also noted that although the manufacturers claimed to have communication capabilities, the software was not adequately tested.

Personal Computer/Mainframe Environment

A personal computer (PC) linked to a host mainframe is usually the least expensive CAD/CAE environment. A growing number of software vendors are supplying PC engineering application programs for tasks including schematic capture, logic simulation, printed circuit board layout and project management. The widespread use of the IBM PC has also spawned the development of communication standards between the IBM PC and larger host systems. As a result, using an IBM PC for engineering applications is a relatively safe investment.

Limited graphics capability is the major complaint among users of this design solution which is, of course, directly tied to the intrinsic limitations of a PC. As one would expect, computationally intensive design verification analysis cannot be performed on the PC. However, local simulation of smaller circuits is quite feasible. For larger simulations, the netlist would be transferred to the mainframe.

With the limited local processing power of the PC, the user is completely dependent on the host for computationally intensive tasks. In some instances, this design environment may put a strain on the host. Although this may not be the case in all situations, it should be taken into account if for large engineering efforts.

Conclusion

Obviously there is no single solution to implementing a CAD/CAE design environment. Each of the design environments discussed has tradeoffs and must be in evaluated in the context of the particular situation.

Supplying the engineer with as much local processing power as possible is a trend throughout the industry. This reflects improvements in CAD/CAE tools as well as the increased computational capabilities of 32-bit super microcomputers. Most industry experts agree that workstations are extremely useful tools, greatly facilitating the design of chips, boards and systems.

With the real-time graphics capability of many of today's workstations, they have become excellent user interfaces. As design standards for communicating between resources become more formalized, the workstation will likely evolve into an undisputed necessity. However, these standards are presently undefined and this fact tends to hinder the acceptance of workstations as cost effective tools. In addition, some industry experts contend that hardware and software advancements may lag the needs of tomorrow's complex designs. If this does not come to pass, networking will become the crucial element in the design environment. □

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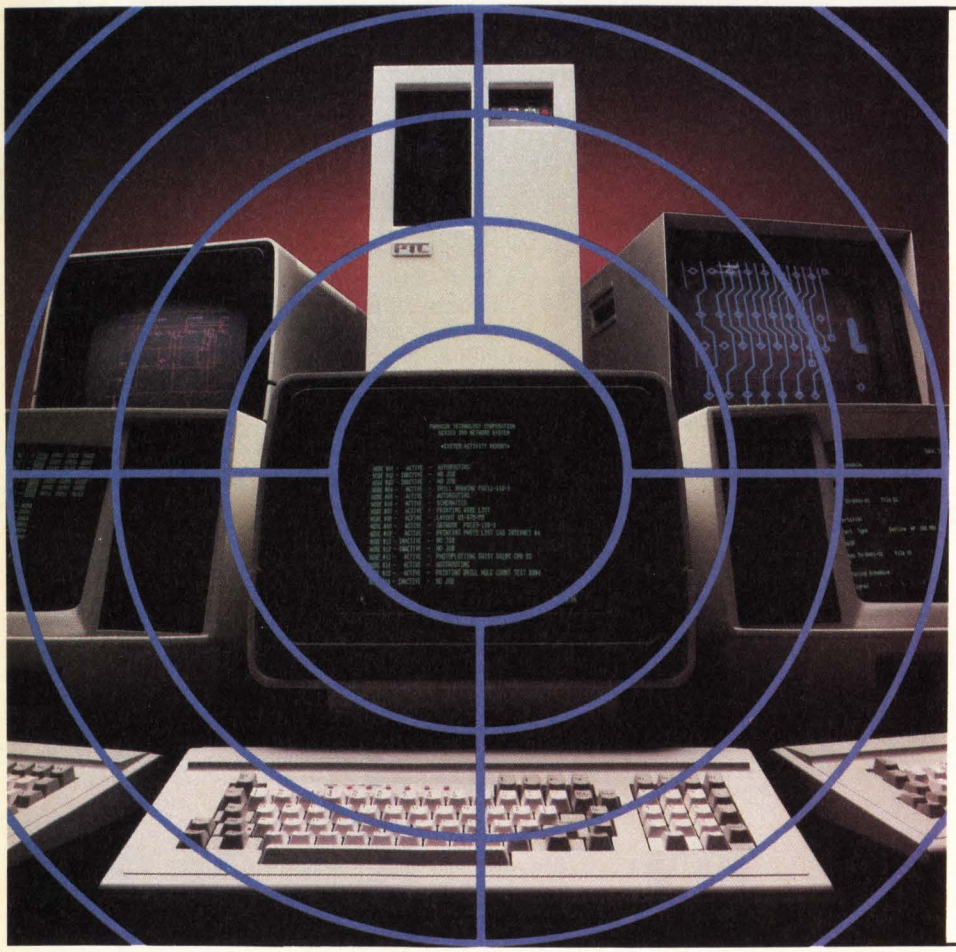

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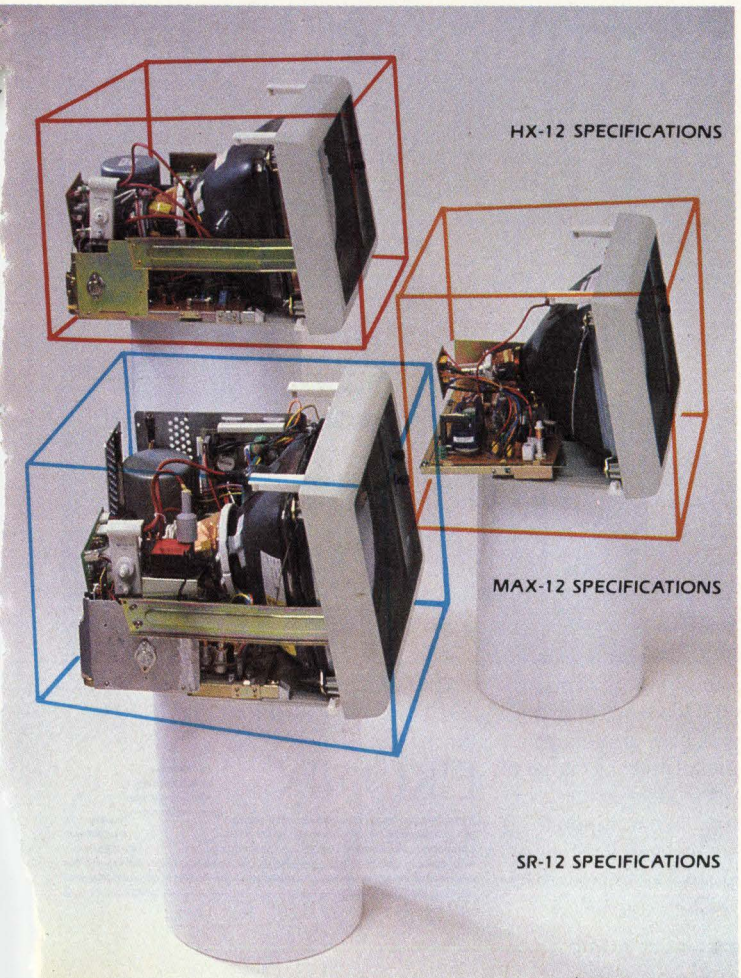

HX-12 SPECIFICATIONS

CRT	12" Diagonal, 76 degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface (NEC 320CGB22)
Input Signals	R, G, B, channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video Bandwidth	15 MHz
Scan Frequencies	Horizontal: 15.75 KHz Vertical: 60 Hz
Display Size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 240 lines (non-interlaced) 480 lines (interlaced)
Misconvergence	Center: .6mm max Corner: 1.1mm max
Display Colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows—8x8 dots)
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

MAX-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor)
Input Signals	Video signal, Horz Sync, Intensity—positive TTL levels, Vertical Sync—negative TTL levels
Video bandwidth	18 MHz
Scan frequencies	Horizontal: 18.432 KHz Vertical: 50 Hz
Display size	204mm x 135mm
Resolution	Horizontal: 900 dots Vertical: 350 lines
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

SR-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface
Input Signals	R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video bandwidth	25 MHz
Scan frequencies	Horizontal: 31.5 KHz Vertical: 60 Hz
Display size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 480 lines (non-interlaced)
Misconvergence	Center: .5mm max Corner: 1.0mm max
Display colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows)
Input Connector	9 Pin (DB9)—cable supplied

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Stanford's "MIPS" Prototypes Faster, Cheaper Systems

By the end of the 1980s, computers will be cheaper, faster, contain chips that will hold millions of transistors, and have memory capabilities that will outdistance by a factor of 10 systems presently used. "People will be able to buy machines for $3,000-$4,000 that will be faster than machines that now cost $200,000," predicts Associate Prof. John Hennessy of Stanford's Electrical Engineering Department. Personal computers will be considerably more powerful and able to perform many tasks that now are associated with minicomputers, and the bigger machines available to scientists and engineers will become significantly faster – "as fast as a Cray," Hennessy says.

Hennessy is project director for the recently announced 32-bit microprocessor that was completely designed and fabricated at Stanford. The microprocessor, named "MIPS," represents a new architecture, housing only 25,000 transistors as compared with the 100,000 or more transistors usually needed in 32-bit machines. Its real strength is that it outperforms commercially available microprocessors by about a factor of five. Efforts are now being made to increase the performance by a factor of five to 10 which would make it faster than any existing machine, excluding supercomputers.

The increased speed was achieved on MIPS by improving the compiler technology that translates languages such as FORTRAN or Pascal into computer instructions. The architecture was redesigned so that it became more compatible with the compiler and IC technology. It was also important to devise a chip which relies less on read-only memory (ROM), and instead uses as many transistors as possible to directly increase instruction, execution, and speed.

Some commercial chips now contain as many as 450,000 transistors, but 80% of those transistors are in ROM. MIPS has 25,000 transistors, but only 15% of them are in ROM; allowing for a much faster system, with more chip area devoted to active operation. The system is designed to let the compiler do most of the translation work, a feature most commercial systems do not have. Most current systems do the instruction interpretation as the program is executing.

In order to produce a new system that is faster again by a factor of five or 10, Hennessy is studying the current design of the system to see where the bottlenecks are, trying to develop a new architecture for the 32-bit microprocessor. The new chip will have 100,000 to 150,000 transistors, 50% of which may be in memory. The Stanford team is also trying to determine whether it should supply support for multiplication and floating point operations on or off the chip.

– *Hanrahan*

Write 247

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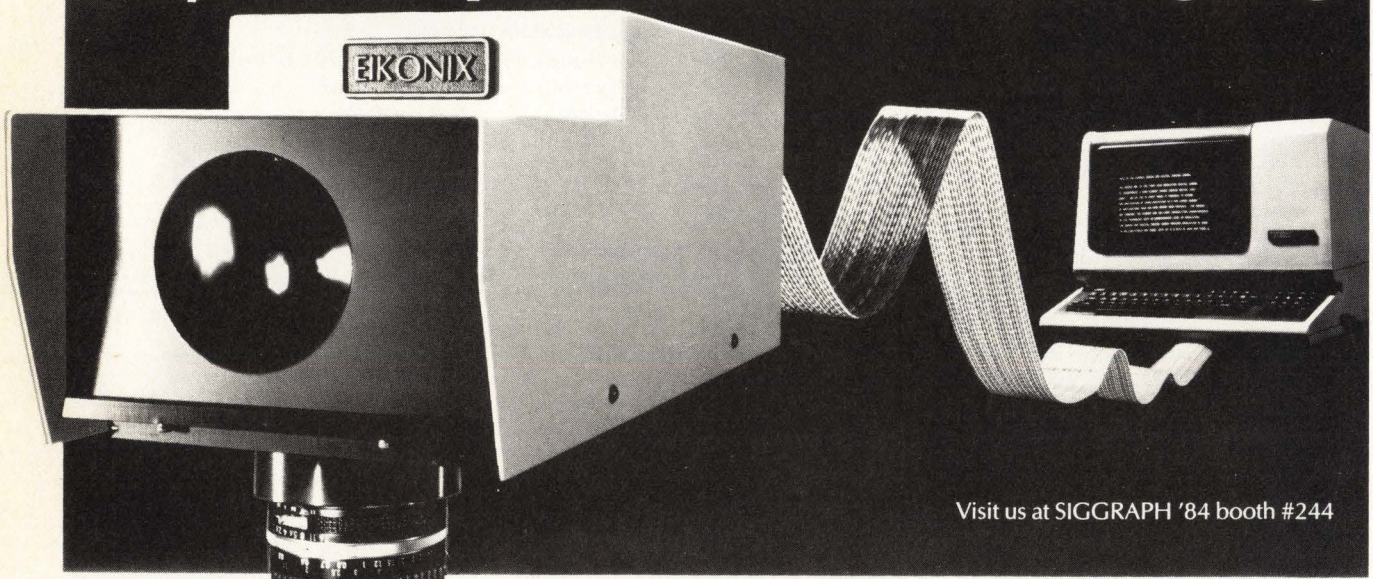

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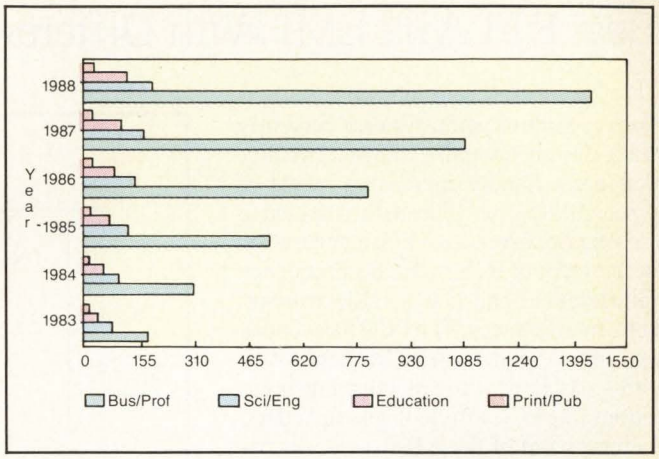
Major Changes Predicted In Graphics Hardcopy Market

The growth of the graphics printer market to 1.8 million units worth $4.6 billion in 1988 will be accompanied by dramatic shifts in the technologies used and the user base. The combination of declining costs and larger and more sophisticated markets is leading to an explosion of new graphics hardcopy devices in a variety of technologies, threatening any companies that fail to keep up. The most important change, however, is the shift to desktop business systems as the largest graphics market, both in units and dollars.

Strategic Incorporated's study, "Interactive Graphics Printers: Impact Of Emerging Technology," analyzes the interrelated development of technologies and products: graphics workstations and computers, graphics hardcopy peripherals, and graphics software. The study projects not only the number and value of future graphics printers, but also the types that will be needed. The accompanying chart shows unit sales by year for graphics systems.



Unit sales by year for graphics systems. (Source: Strategic, Inc.)

Given the variety of output technologies, and variability in resolution, image quality and support of color, there is a strong tension between device independence and complete control of graphics output, which has prevented the development of portable graphics software. Device independence would allow a variety of graphics displays and printers to be used with the same software without individual programming, but would increase the complexity of operating systems and fail to take maximum advantage of more capable devices. At the moment there is little standardization, but the development and marketing activities of key actors such as Digital Research, Microsoft, IBM and AT&T will lead to market standards after several years of intense competition.

Strategic predicts that the convergence of CP/M and UNIX, as well as the appearance of bit-map graphics hardware and software products will be major factors in the development of key industry standards. These standards will be independent not only of applications and graphics printers, but also of operating systems and computers as well. In the CP/M-MSDOS-UNIX fracas, each will come to run all other software. The current competition among Apple's Lisa and MacIntosh, VisiCorp's VisiON, and the bit-map graphics to be supported by Microsoft and Digital Research, will be equally confusing at first. Printer manufacturers will be equipped to support various incompatible hardware and software interfaces. Later, the problem will be resolved as each system is enhanced with emulations of the others, and as each operating system allows all the others to run as tasks in the manner of IBM's VM mainframe operating system.

The leading graphics printers will be well supported in each system, and new devices will either require special drivers for popular computers and operating systems or emulate existing devices. This coming conflict may offer good opportunities for graphics printer manufacturers.

—Hanrahan

Write 248

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Beat RFI And EMI With Differential Backplane Transceiver

Data communication systems currently being designed require compact circuitry that must handle increasing levels of power dissipation. This in turn has led to a rising occurrence of noise generation in the form of R.F.I. (Radio Frequency Interference) and E.M.I. (Electromagnetic Interference). The FCC has stepped up its crackdown on radio frequency standards violators while placing new regulations like FCC article 15 into full effect. Enforcement of these RF standards has forced many manufacturers to closely re-examine their degree of RFI/EMI compliance. Compliance testing helps ensure present equipment meets these standards but designing out these problems is the best long-term solution.

A new transceiver capable of providing users with a means to comply with FCC regulations is AMD's Am26LS38 Quad Differential Backplane Transceiver, designed to integrate Schottky TTL performance, high noise immunity and wired logic capability into low-cost differential backplane structure.

R.F.I. and E.M.I. noise can occur in many areas of a system but the principal source is backplane (or board-to-board interconnections) signaling. The Am26LS38's differential signaling provides two forms of helpful cancellation. First, radiated signal caused by the dv/dt in each signal lead is opposed by its equal and opposite compliment, thus cancelling the R.F.I. Second, terminating the cable pair correctly line to line in its characteristic impedance assures that current flowing in one signal lead is opposed equally by its mated pair, thus minimizing E.M.I. Correct termination is illustrated in **Figure 1.**

The Am26LS38's driver-receiver pair are capable of operating in a blanced differential mode without distortion. The receiver is designed with a low (±50mv) threshold that combines with its driver output of greater than 500mv to provide systems attenuation tolerance and margin for cable losses. A 25mv (typical) hysteresis minimizes the switching sensitivity caused by lines with slow transition times. The device will operate in the presence of up to 1.5v of Common Mode Voltage, thus eliminating the need for absolute ground references. To reduce radiated harmonic disturbances the

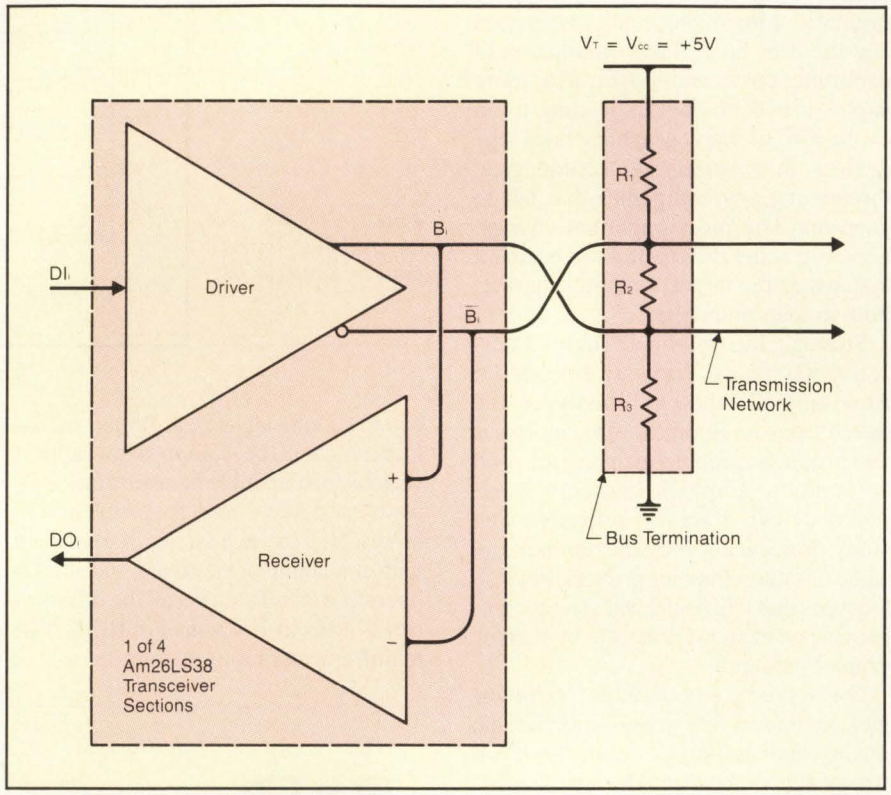

Figure 1: System connection diagram.

Am26LS38 features symmetrically controlled rise/fall times.

The Am26LS38's shared-bus digital balanced line transmission works especially well for the inter-element backplane communication within a processor complex. For such an application, the bus line is bi-directional and party lined, but the subsystem internal buses are unidirectional. While network dimensions vary with the types and size of cabling utilized, a typical network of up to 25 feet (and up to 25 transceivers per line) can be created with data rates in excess of 10MHz.

Two modes of bus operation are possible with the Am26LS38: registered transmit and latched receiver, or buffered transmit and latched receiver. With the

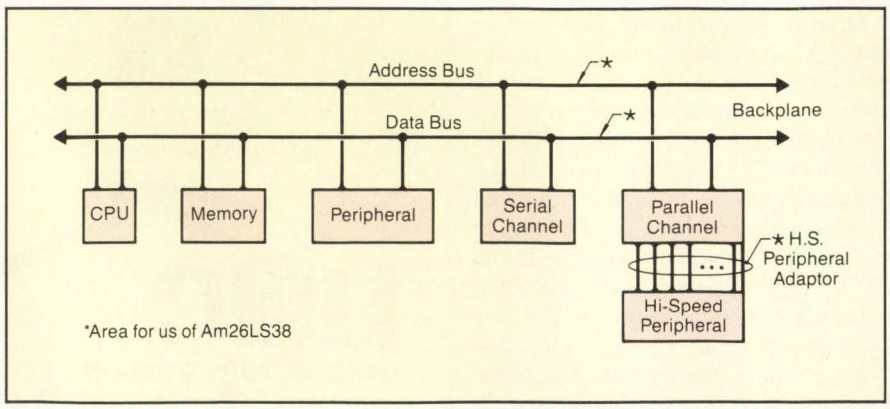

Figure 2: Am26LS38 utility in a processor complex.

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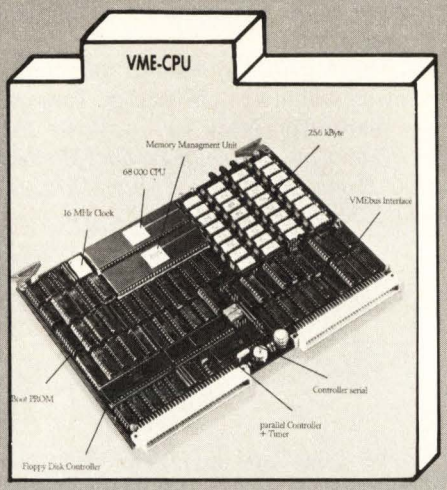

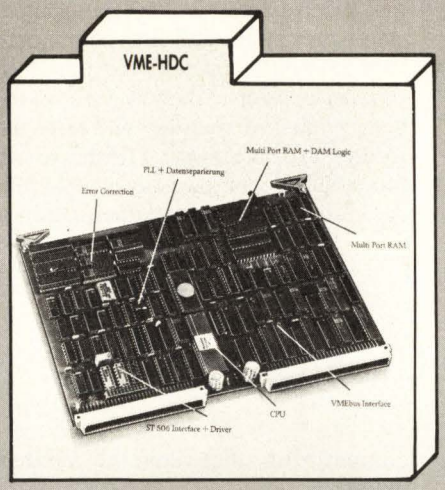

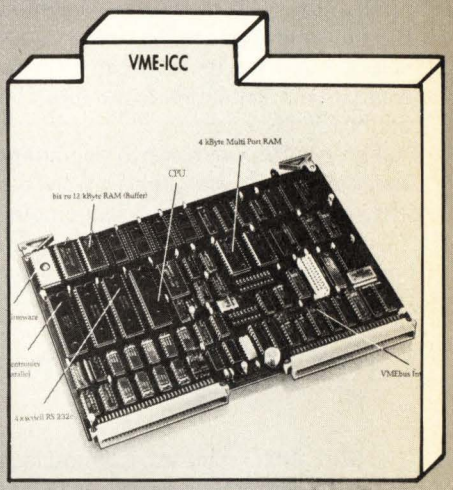

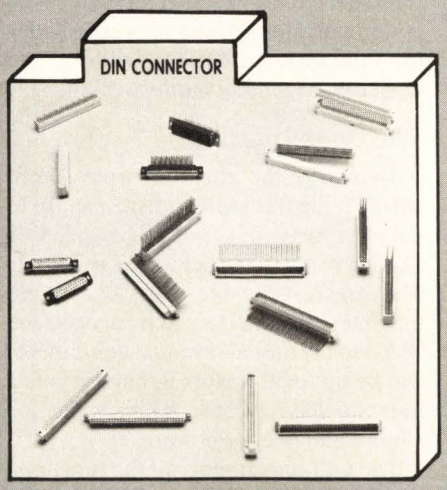

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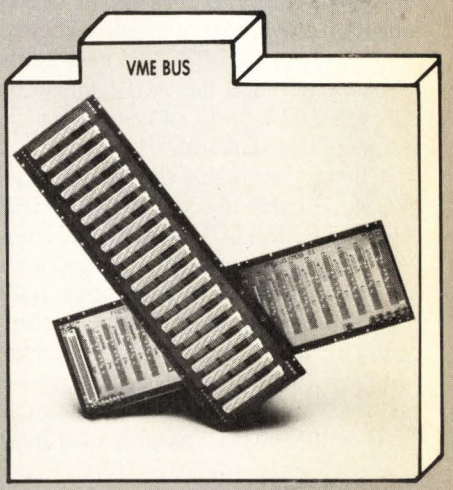

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Am26LS38's internal register and latch combination, a storage mode can be established for the output and input data ("Registered Mode" for synchronous bus applications). In the non-storage mode the buffered-input to the driver can be selected and the receiver can be wired transparent ("Buffer Mode" for direct bus applications).

The Am26LS38 has two operational states: active (driver outputs on) and passive (off). The two-state driver employs active pull-down (open collector) and active pull-up (open emitter) output stages that are simultaneously applied to a transmission line to form the driven signal. When a driver is active, both output stages turn on, establishing a minimum voltage differential of 0.5v on the bus. This driver reverses the voltage across the bus termination resistor and causes the receiver to detect a logic "1". In the passive mode both output stages are off, and voltage levels, observing polarities, return to the conditions set by the bias network, thus maintaining a logic "0" at the receiver input. Users may use this two-state (active/passive) operation for such wired logic functions as polling or prioritization.

The Am26LS38 features four transceivers within a 24-pin package. Parts are available from stock. **Write 232**

–Gary Connor, Senior Product Marketing Engineer, Advanced Micro Devices, Inc., Sunnyvale, CA

Chip Set For Ethernet/Cheapernet Node

The IEEE 802.3 standard, is almost identical to the Ethernet II as well as ECMA standards. Two important enhancements soon to be part of 802.3, namely the 'Cheapernet' and the 'AUI Compatible Broadband,' significantly broaden the scope of this standard.

Cheapernet uses the inexpensive RG58AU cable and is user installable. Hence it is ideal for low cost applications. The AUI Compatible Broadband standard allows the 802.3 compatible baseband equipment to be plugged directly into a broadband network, thus providing the user with the option of changing over to broadband at a later date. A single data rate of 10Mbits/sec assures total intercompatibility between the various options.

Success of the 10Mbit/sec CSMA/CD, however, depends heavily on the availability of ICs that implement the network node functions in a cost effective manner. National's solution (the DP8390 series) integrates all the electronics required for an IEEE 802.3/Ethernet node into three chips. Starting from the cable, these three chips perform the following functions: the DP8392 Coax Transceiver Interface (CTI) implements the driver, the receiver and the collision detection circuitry; the DP8391 Serial Network Interface (SNI) Manchester encodes and decodes the serial data and interfaces to the transceiver cable; and the DP8390 Network Interface Controller (NIC) executes the communications protocol and provides the host system interface with built-in buffer management hardware.

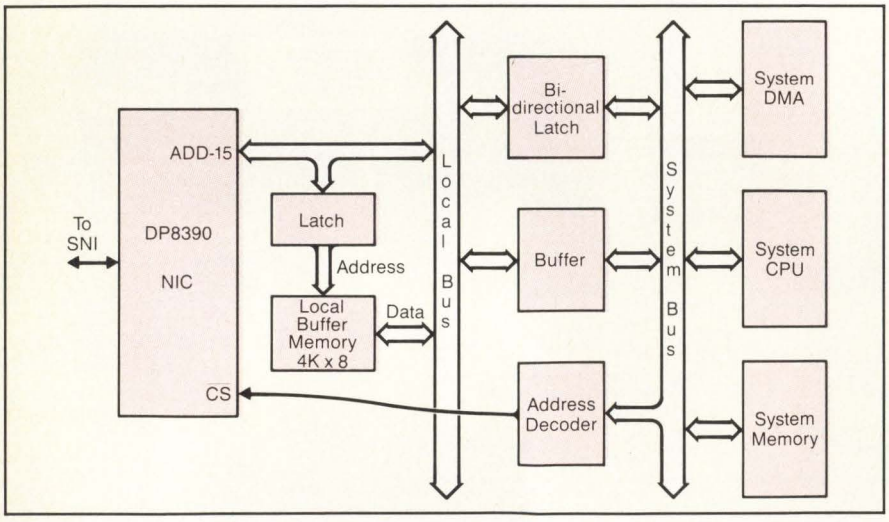

Figure 1: A few low cost external components is all that is needed to interface the NIC to the host system with local memory. Even the control signals for the buffers and the latches shown are provided by the NIC. A direct interface to the system bus (without a local memory) requires even fewer components.

The Coax Interface

Also called the medium access unit (MAU), the transceiver resides close to the coax medium to keep the capacitive loading on the cable below the 4pF limit. The transceiver cable or the attachment unit interface (AUI), which connects the MAU to the digital terminal equipment, can be up to 50 meters in length. It has four shielded twisted pairs, three for signals and one for power.

The CTI implements all the functions within the transceiver except for the signal and power isolation. Signal isolation may be accomplished with three pulse transformers that fit in a single 14 pin standard plastic DIP. The power isolation, however, requires switching and regulating circuitry in addition to a transformer. This part of the transceiver electronics is intentionally left out of the CTI because of the high power and isolation requirements.

In short, the CTI combines all the precision functions with high speed ECL, this chip meets the specifications of IEEE 802.3/Ethernet-II. For example, the coax driver must have controlled rise and fall times of 25+/−5ns matched to within a nanosecond with no more than a 2ns skew. To meet the tighter drive current tolerances recommended by IEEE 802.3, an external resistor is used in conjunction with an internal voltage reference. A

(continued on p. 119)

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PRODUCT INDEX

To help you find the products that you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

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(continued from p.112)

jabber that monitors the driver for faulty operation disables the output if it is active for more than 20ms. The output can also be physically disconnected from the network using a relay connected to the jabber output provided on the CTI.

For reliable detection of Receive Mode collision (i.e. collision between any two stations on the network), the CTI incorporates a 4 pole Bessel filter in combination with a trimmed on board reference. An on chip 10MHz oscillator is turned on to signal the presence of collision and to generate the Heartbeat at the end of a transmitted packet. The receiver circuit features an equalizer to reduce the distortion introduced by the cable. It also incorporates a squelch circuit that keeps the noise on the cable from triggering the receiver. The CTI connects to the pulse transformers that in turn connect to the transceiver cable. The receive and collision pair ECL drivers feature a zero output idle state to eliminate large idle currents through the transformers. The transmit pair input incorporates a squelch to reject transceiver cable noise.

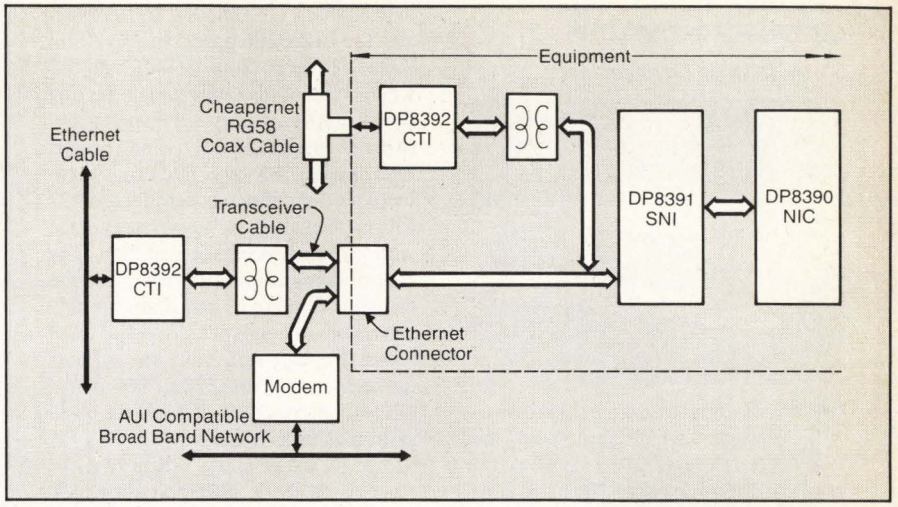


Figure 2: By incorporating the CTI along with the other two chips within the data terminal equipment, the user can be provided with the option of using either the Cheapernet or the Ethernet or the Broadband network.

Digital PLL Decoder

On the terminal end, the transceiver cable interfaces directly with the SNI without the need for any transformers. The differential driver and receivers have all the features of those in the CTI in addition to the breakdown and short circuit protection required to connect the cable directly to the chip. Eight TTL lines provide the interface to the network controller. Although designed for easy interface to the NIC, the SNI can be adopted to most other controllers with some extra logic.

The NRZ data from the controller and the transmit clock are encoded into Manchester data and sent down the transmit pair to the transceiver. The opposite process takes place on the receive path.

Apart from the encoder/decoder function, the SNI also generates the carrier sense signal from the receive pair and decodes the collision presence signal into a TTL level for the controller. It also features an internal loopback for diagnostic purposes.

Dual DMA

Packaged in a standard 48 pin DIP the DP8390 network interface controller is a VLSI chip that implements all the data link layer functions specified in IEEE 802.3/Ethernet II. It also provides an efficient on board buffer management scheme featuring a dual channel DMA that effectively dual ports an external local buffer RAM. Up to 64 Kbytes or words of buffer RAM is supported. One of the DMA channels (local) is used for data transfers between the local buffer memory and the NIC and the other (remote) for data transfers between the local buffer and the host. All RAM support and bus arbitration logic are provided on chip minimizing the external parts count for a typical system. The NIC is designed for easy interface to most of the popular 8- and 16-bit microprocessors.

To transmit a packet, the host processor assembles the packet in the local buffer and issues a transmit command to the NIC. The NIC then automatically handles the transmission of the packet according to the CSMA/CD protocol. That is, deferring to any carrier on the coax with a 9.6us interframe gap, it transmits the packet from the local buffer inserting the preamble and the CRC that are generated on board. When a collision occurs it stops transmission and backs off randomly in accordance with the binary exponential algorithm and retransmits the packet. If repeated collisions occur, the NIC quits after 16 attempts and alerts the host. It should be noted that all of the above activity is isolated from the host bus saving system bandwidth.

As a packet is received from the network the NIC checks the destination address and if it is valid, verifies the CRC with the one generated on board and stores the packet in the receive buffer queue area within the local memory. This area is a continuous list of 256 byte/word pages that is assigned by the host during initialization of the NIC chip. Both the location of the receive buffer queue within the local buffer and its length in number of pages are fully programmable. Any area outside of this queue can be used for assembly of transmit packets. The packets are always stored starting from the top of a page and as many pages as required to store a packet are used.

Cheapernet Options

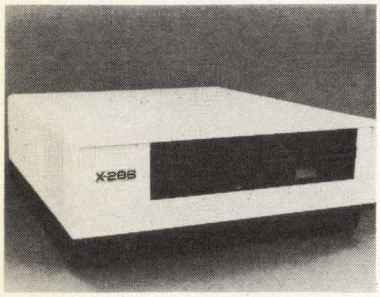
By providing the standard transceiver cable connector in addition to the BNC, the user now has option of using either the IEEE 802.3/Ethernet/AUI Compatible Broadband or the low cost Cheapernet. Using an off the shelf coax, the Cheapernet accommodates up to 30 nodes over a span of 200 meters. Furthermore, because it uses the same data rate and protocols as the Ethernet a Cheapernet cluster may be connected through a standard Ethernet repeater to the main Ethernet cable passing through the building.

National's three chip solution, that requires only a few external components, is expected to bring the manufacturer's cost of the standard LAN hook up to under $100(qty).

– R.V. Balakrishnan, Design Section Manager, Interface Design, National Semiconductor Corporation, Santa Clara, CA.

SUPERMICROCOMPUTER

5-User Desktop Configuration



The X-286 is a desktop supermicrocomputer which implements the XENIX operating system on Intel's 80286 processor. The basic configuration supports five users which is expandable to 16. The X-286 incorporates the iAPX 286 processor, an 80-bit 80287 numeric co-processor, and 512 Kbyte of error detecting and correcting RAM. RAM memory is dual ported between the system Multibus and a private high speed iLBX bus. The disk system includes a pipelined controller and 127 Mbyte (formatted) of Winchester storage with an average access time of 30ms. The controller has automatic error correction of 11-bit burst errors and performs disk subsystem diagnostics. A 5-1/4″ 320 Kbyte floppy, with software support for sector sizes from 128 to 1024, and a QIC-02 interface come with the basic system. The X-286 is expandable to 16 Mbyte of RAM and 1 Gbyte of disk. Price is $17,900. **BDS,** Sterling, VA

Write 128

TURNKEY CAD SYSTEM

For Parametric Design

BRAVO! is a family of turnkey CAD and manufacturing systems designed for applications such as parametric design, interactive solids modeling, online structural analysis, drafting and documentation, and numerical control programming. The systems feature the VAX/VMS operating system, and has a CODASYL-compliant database management which integrates design, analysis, drafting, documentation, and manufacturing applications in a single system. BRAVO! processors range from a VAX-11/730 GPF with 5 Mbyte memory option to a VAX-11/751 GPF with 8 Mbyte memory. BRAVO! can also run unbundled on VAX-11/780 systems with Applicon workstations. **Applicon,** Burlington, MA

Write 143

CROSS-DEVELOPMENT TOOLS

With Link Editor

Uniware is a system of cross-development tools that are written for any UNIX-based system and can accommodate most 16- and 32-bit host processors. The base module consists of a macro preprocessor, link editor and utilities, and a target module which consists of a cross-assembler specific to the target microprocessor. Release 3.0 has a link editor and object file format, which allows an unlimited size symbol table and preserves it for use in symbolic debugging. It supports multile overlays and uses a C-like specification language that allows users to define load maps in one central file, define and use symbols in arithmetic expressions, and create linkages between overlays. Price is $1,200 – $2,000. **Uniware,** Chicago, IL **Write 149**

COLOR CAD SOFTWARE

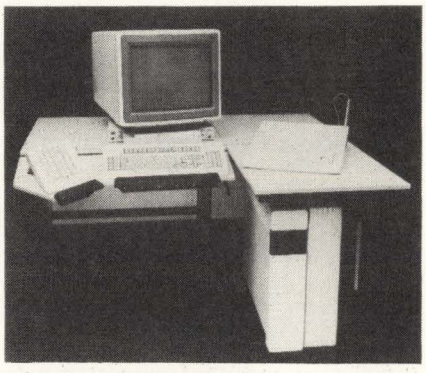
For IBM PC

Cad Master is a two-dimensional drafting software program from Datagraphic Systems which converts the IBM PC into a high resolution CAD workstation. Features include auto dimensioning, bill of materials, 130 assignable overlays, fillet radii generation, symbol tables and parts libraries, pattern fills and cross hatching. Engineering functions include area and volume computation, and section properties, like centers of gravity, and moments of inertia. Applications include mechanical, architectural, schematic drafting, control layout, process flow diagrams, electrical and electric circuit designs. **Datagraphic Systems,**, Milford, MI

Write 129

COLOR DISPLAY SYSTEM

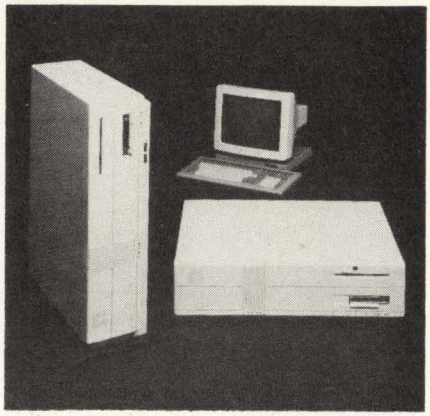
Uses Multidrop Communications



The VG 9250 display system is a high resolution 1024 × 1024 pixel raster system which can simultaneously display 256 colors from a 16-million-color palette. The system has a vector draw rate of 16 million pixels/sec and is designed for high-end CAD/CAM engineering functions. The VG 9250 uses a multi-drop communications network that integrates multiple display stations on a 15,000 ft. coaxial cable. Data transfer speeds are two million bits/sec. Price is $26,250. **VG Systems,** Woodland Hill, CA **Write 137**

SUPERMICRO COMPUTER

Dual Processor Architecture

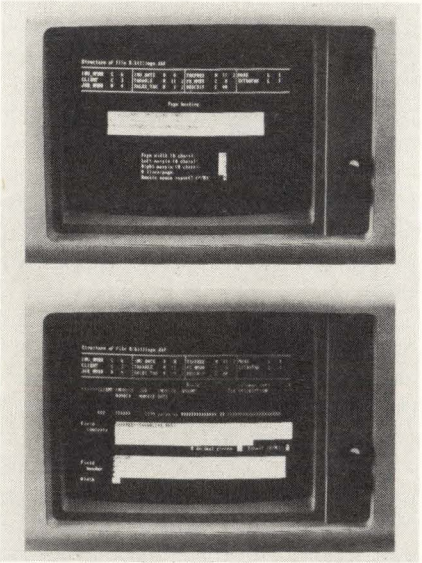


The SuperMicro computer is based on a dual processor architecture, combining the iAPX 286 and iAPX 287 microprocessors from Intel. The SuperMicro uses the iAPX 286 as an applications processor, and the iAPX 287 as a numeric co-processor. The peripheral bus conforms to SCSI requirements and supports arbitration and contention logic. It can be controlled via programmed access or DMA. Two 5.25″ Winchester hard disk drives have a capacity of 50 Mbytes. A 5.25″ streaming tape drive provides backup and a 5.25″ floppy disk drive provides program loading and low volume backup. The system has standard RS 232C serial ports and an IEEE 488 parallel bus. **Rair Computer,** Santa Clara, CA

Write 139

DATABASE MANAGEMENT SOFTWARE

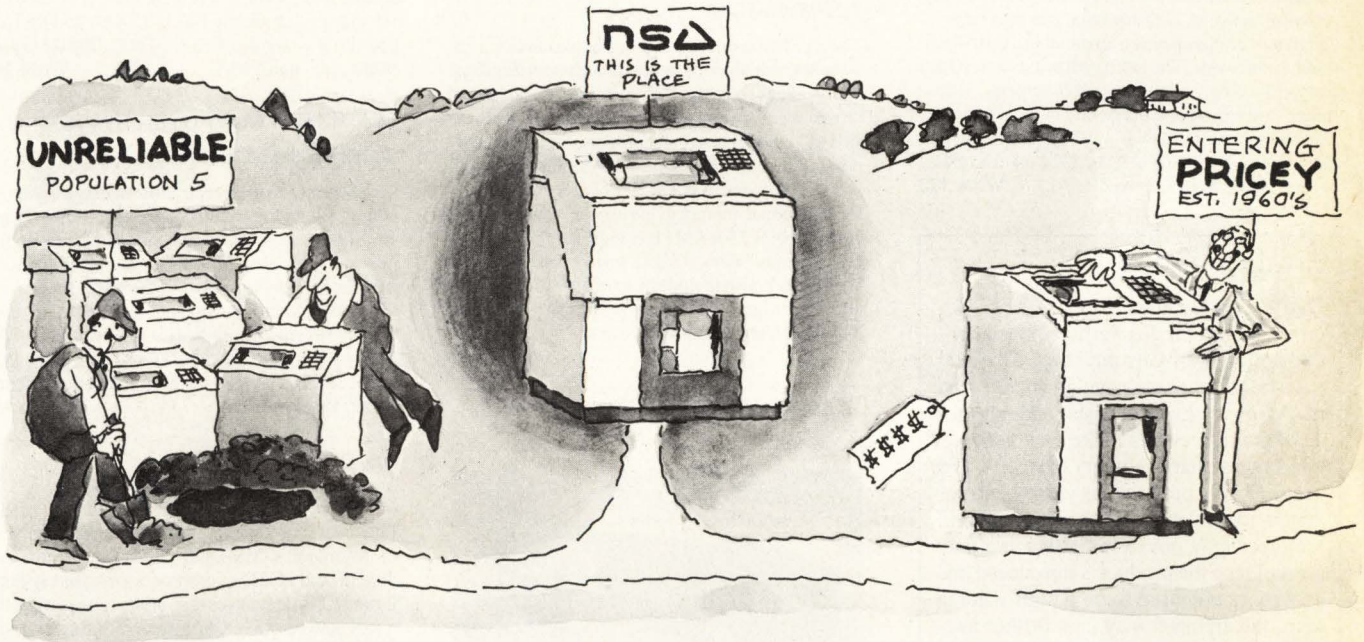
Uses 10 Database Files Simultaneously



DBASE III is a relational database management software program designed for 16-bit computers. The software has storage capabilities of two billion records per file, 128 fields per database and can use 10 database files simultaneously. The system features a command assistance mode for the first time user. System requirements include a minimum of 256K RAM, two 5¼″ 360K diskette drives or one fixed disk drive and one diskette drive, a monochrome or color display and PC-DOS 2.0 operating system. Price is $695. **Ashton-Tate,** Culver City, CA

Write 144

Finally, a 2,000 LPM band printer somewhere between unreliable and too much money.



Twice the reliability.

Compare Hitachi Koki's FP-2000 against any low-priced 2,000 LPM band printer. The differences are immediately apparent. Instead of a light-duty souped-up machine, you'll find heavy-duty 3,000 LPM technology that has actually been slowed down for unprecedented reliability at 2,000 LPM. You'll find a printer that's suited for continuous operation — not just transaction printing. That delivers consistent OCR scannable print quality. And most significantly, that delivers an honest 1,200 hours MTBF.

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Next compare the FP-2000 against the old industry standard for reliability. After evaluations, large OEMs have reported reliability every bit as good, print quality better, and the price almost half. They have also found comprehensive diagnostics, modular construction, IBM plug compatibility, and a quiet, compact design engineered for ease of use, ease of service and low-cost of ownership.

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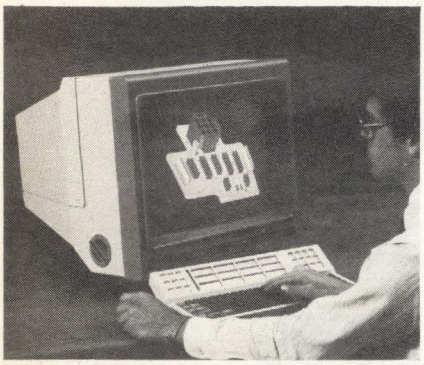
COLOR WORKSTATION

Desktop Configuration



The Interpro is a desktop color workstation which can simultaneously display 256 colors selected from a palette of 16 million hues and intensities. The Interpro communicates with any Integraph data processing system or operates as a terminal in a distributed graphics network. The Interpro has a second screen capability which simulates dual screens, whose images are stored independently in local memory. The color workstation has a 19″ raster screen, displaying graphics with 1280 by 1024 pixel addressability. **Integraph,** Huntsville, AL **Write 133**

Errata

Due to a typesetting error, a sentence was omitted from the June article "Designer's Guide To Semi-Custom ICs." The next to last paragraph on page 65 should read as follows: Lower costs and shorter development cycles make gate arrays a good risk management strategy. For example, if a product has yet to be introduced to the market, then the system architect may opt to initially use a gate array. Once the product is introduced and proves its potential to be a high volume item, the architect may then further integrate the system using standard cells. This risk managment plan minimizes financial losses if the product is not as successful as originally anticipated. If the product does turn out to be a market success, the initial gate array expenditure will be absorbed over the sheer volume of the product.

In the May issue of *Digital Design* the article entitled "Modular Architectures May Be The Next Array Processor Design" contained two errors. DSP Systems manufactures three products. Two are for the Multibus; the DSP-FFT-1B and the DSP-AP-4. Both units have 2K words, not 64K of on-board data memory as well as 2K of coefficient memory. Both modules have on-board DMA. The third product, the VAP-64, is for the VME bus. It does not have an on-board processor, but rather 64K RAM. The author apologizes for these mistakes.

UNIX-BASED COMPUTER SYSTEM

With Discrete Memory Management Unit

The MiniFrame is a UNIX-based computer system which supports eight users. Hardware is based on the Motorola 68010 10 MHz microprocessor, has 0.5 to 2 Mbytes of RAM (in a 4 Mbyte virtual address space), a discrete memory management unit and a Western Digital 1010 VLSI disk controller. Mass storage options include a fixed 5¼″ disk drive in 13, 26 and 50 Mbytes, unformatted capacities, and a removable 640 Kbyte 5¼″ floppy disk drive. The system has a Centronics parallel port for printer support, two to 10 RS-232 ports, a multidrop RS-422 port, and an Ethernet controller. In OEM quantities, price is $4,700. **Convergent Technologies,** Santa Clara, CA **Write 135**

MICROPROCESSOR-BASED DEVELOPMENT STATION

1.25 Mbyte RAM

The SYS16 is a microprocessor-based development system which supports the use of high-level languages and modular software. It implements demand paged virtual memory and supports Berkeley 4.1 bsd version of UNIX. The six slot processor module incorporates the complete family of NS16000 chips and has 1.25 Mbytes of RAM. Two slots are available for additional memory, giving the system a total capacity of 3.25 RAM. It is logic supporting with eight asynthronous RS 232 serial ports and FIFO buffering. It also includes a hard disk and streamer tape cartridge module and proprietary software. **National Semiconductor,** Santa Clara, CA **Write 134**

COMMUNICATIONS SYSTEMS

Handles 300 Lines

The System 75 communications system combines voice, high-speed data, and communications and system management features into an integrated system. It is designed for installations of 300 lines and can be upgraded. The system 75 can transmit voice and data simultaneously over one line at 64,000 bps. The system has a system management capability for customization in different applications such as diagnostics. **AT&T,** Morristown, NJ **Write 130**

¼″ CARTRIDGE SUBSYSTEM

60 Mbyte Capacity

The TK25 ¼″ tabletop streaming subsystem is backup for disk storage. It uses a DC600A cartridge and has a 60 Mbyte capacity, backing up miniWinchester disks without changing cartridges. The unit is supported under the RT-11, RSX-11, and RSTS/E operating systems. Price is $4,600. **Digital Equipment,** Maynard, MA **Write 142**

MULTIUSER COMPUTER SYSTEM

20 Mbyte Hard Disk Storage

The Series 9 multiuser, multiprocessor computer system allows the simultaneous operation of 8- and 16-bit processors and offers compatibility with five operating systems. The base model includes 20 Mbytes hard disk storage, a 320 Kbyte floppy disk drive, file processor card and accommodates up to nine application processors. Options include a 45 Mbyte streaming tape drive and 80 Mbytes of additional storage. Price is $7,995. **Molecular Computer,** San Jose, CA **Write 150**

MS-DOS SOFTWARE

For Intel 286/310 And 86/310 Systems

Release 1.0 of 310 MS-DOS is an implementation of Microsoft's MS-DOS Version 2.11 for Intel 286/310 and 86/310 microprocessor-based systems. It runs 1,300 languages and applications programs. Users have a choice of three operating systems, iRMX/MS-DOS, Xenix/MS-DOS, and MS-DOS. With the first two options, the 310 can be configured so that MS-DOS and the alternate operating system both reside with their file systems on the 310's Winchester disk drive. For users who run MS-DOS occasionally, 310 MS-DOS can also be operated from a floppy disk. Price is $285. **Intel Corp.,** Santa Clara, CA **Write 132**

SOFTWARE DEVELOPMENT STATION

Support Cross Development Projects

Source Tools is a computer-aided software development and management system which allows the host computer to assist in the application software development cycle. Source Tools can be used with software written in any computer language or text file. It is comprised of three program packages: SourceCon contains four programs that control the creation and modification of source code files; MAKE, automatically keeps programs up to date as components are changed; The third package contains two programs, which maintain parallel source files on different systems. Price is $4,500 for the RSX operating system, $4,500 for VMS running in RSX compatibility mode, and $3,600 for the RSTS operating system. **Oregon Software,** Portland, OR **Write 131**

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  - All Versions available for wide temperature (−40°C to +50°C) applications
- **Parallel 8 Bit Interface**
  - 110 V Operation
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  - All Versions available for wide temperature (−40°C to +50°C) applications
- **IEEE - 488 Interface**
  - 110 V Operation
  - 220 V Operation

All Models Feature -

- Complete Microprocessor compatible interface electronics
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- Quiet inkless thermal printing
- Built-in self test program
- Programmable controls
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  Front panel is 5.25" W × 2.81" H
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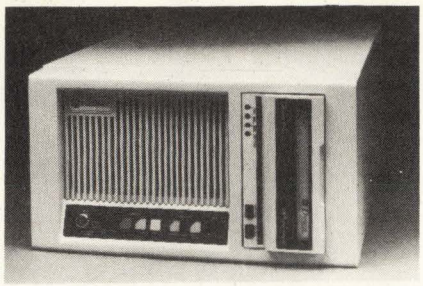
NEW PRODUCTS

COMPUTER SYSTEM

LSI-11/73



The Series 8600 incorporates the DEC KDJ11-AA-based LSI-11/73 processor into its operating systems. The system has a 41.6-Mbyte fixed/removable hard disk drive and 256 Kbytes RAM expandable to four Mbyte. Most current LSI-11 and PDP-11 operating systems and application software are compatible with the 8600. **Plessey**, Irvine, CA **Write 141**

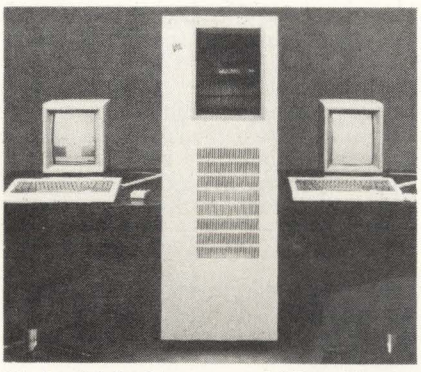
NEW SOFTWARE VERSIONS

PASCAL, FORTRAN and C

These software versions from Microsoft are programming languages for MS-DOS operating systems. Microsoft has added two math libraries to Pascal, supplementing the existing 8087 coprocessor and 8087 emulation support. The math package operates without an 8087 chip. The Pascal 3.2 includes MS-DOS 2.0 run-time support. The latest release of FORTRAN includes floating-point math and MS-DOS 2.0 file and overlay linking options, as well as support for large arrays and complex numbers. Other new features include parameter statement to assign symbolic names to constants, block data programs to set variable and array element values, and the Inquire statement to determine file or unit properties. Price is $300 to $500. **Microsoft Corp.**, Bellevue, WA **Write 145**

2-USER LISP MACHINE

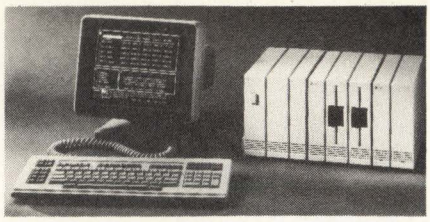
128 Mbyte Virtual Address Space



The Lambda 2×2 is a two-user LISP machine that features two concurrently executing LISP processors. The processors operate in the framework of a 37.5 Mbyte/sec multi-processor NuBus architecture, with 128 Mbyte of virtual address space per user. Each user has access to the Zetalisp-Plus environment, with individual AI keyboard and mouse, high-resolution display and display controller. The machine's 2 Mbyte physical memory, expandable in 2-Mbyte increments, is segmented between the processors, while other resources such as the 470-Mbyte Winchester disk drive, Multibus and Ethernet-II interface are shared. Price is $55,000. **LISP Machine**, Los Angeles, CA **Write 147**

DESKTOP MICROCOMPUTER SYSTEM

256K RAM



The B25 desktop microcomputer system supports clusters of up to 32 B20 and B25 workstations. The basic system includes a central processor with 256K RAM, 12″ display, keyboard and a dual floppy disk storage module. A 10-million byte floppy/hard disk peripheral is available as an option. The system can also be expanded to 40 Mbytes. Price is $4,000. **Burroughs Corp.**, Detroit, MI **Write 138**

NETWORK PROCESSOR

Support 114 Trunks

The System 375 network processor is based on DCA's Integrated Network Architecture. The 375 supports 114 trunks, has a 56K or 72K bps trunk capacity, a bus speed of 4.27 Mbits/sec and a standard floppy disk load subsystem. The 375 can function in a network with DCA Series/100 or 200 statistical multiplexors and the System 325 Netswitch, as well as with X.25 packet mode hosts or public data networks. Features include subnetting, port contention capability, trunk link multidrop multiplexing and a network console port. **DCA,** Norcross, GA **Write 136**

DEVELOPMENT WORKSTATION

For IBM PC

The Step PC7 is a development work station which links the Step-7 Firmware Integration Test Station with the IBM PC. The PC-7 takes heavily used disk files and puts them in the PC's RAM which results in a reduced file access time. Step's Macro Meta PC assembler can be installed on the PC chassis. Using the IBM PC as a host computer, it is possible to define bit-slice designs, assemble programs, format object code, and debug microcode. Price is $10,000-$25,000. **Step Engineering,** Sunnyvale, CA **Write 140**

GRAPHICS DESIGN SYSTEM

With Monochrome Or Color Screen

The System 25 is a CAD system with a 32-bit central processing unit, distributed processing and a modular building approach that enables system expansion. The system can be organized into single-user, stand-alone, multiuser or mainframe-based configurations. The main design station consists of two displays, a 12″ alphanumeric screen and a monochrome or color graphics screen. Price is $65,000. **Calcomp,** Anaheim, CA **Write 146**

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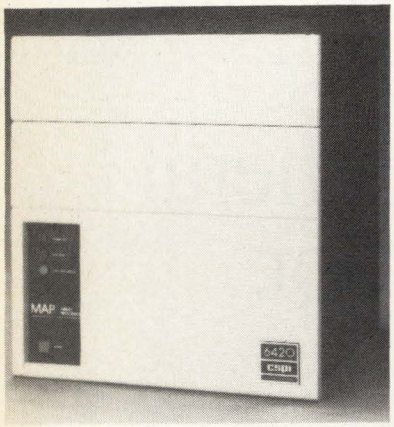
DD784

64-BIT ARRAY PROCESSOR

With Fortran Compiler



The MAP 6420 is a floating-point array processor system designed for scientific applications. The MAP-6420 is equipped with a FORTRAN compiler which enables development or conversion of applications programs. The MAP-6420 has a data memory capacity of 64 Mbytes, an address space of 1 Gbyte, an internal minicomputer, and an arithmetic processor comprised of a 64-bit floating point unit in parallel with a 32-bit integer unit. Price is $100,000 in a 4 Mbyte configuration. **CSPI**, Billerica, MA. **Write 217**

DATA MODEM

2400 Full-Duplex Operation

The UDS 224 data modem features an adaptive equalizer which allows high performance over marginal lines. The modem processes synchronous and asynchronous binary serial data at 2400 or 1200 bps. The data modem can tell if the calling modem is a Bell compatible unit and adapts its speed and modulation accordingly. The 224 provides a CCITT V.24 and EIA RS-232-C compatible interface for connection to DTE. **Universal Data Systems,** Huntsville, AL **Write 167**

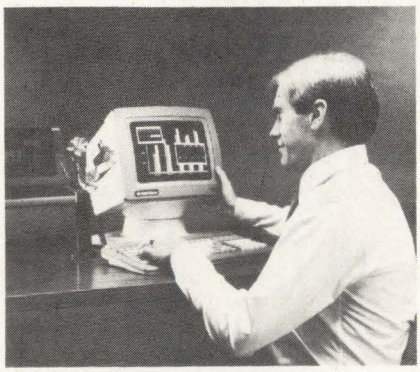
ETHERNET-BASED LAN

Integrated With PRIMENET

This local area network from Prime Computer is based on Ethernet technology and international standards. The LAN is integrated with PRIMENET, the company's distributed networking facility. PRIMENET users can execute existing applications on the LAN without changing their software. The network complies with protocols as defined by the IEEE, ISO, NBS and the ECMA. Using a layered architecture design, protocols follow the ISO Open Systems Interconnection Model recommendations. IEEE 802.3 standards are used for the physical and link level protocols at the lowest layers of the network. At the higher transport layer, draft specifications as set forth by the ISO and NBS will be used. **Prime Computer,** Natick, MA **Write 156**

TERMINAL

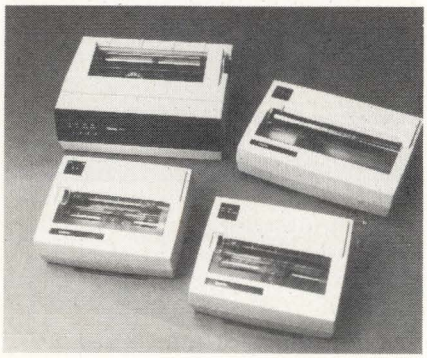
For Engineering And Word Processing Applications



The 925E terminal provides 925 compatibility. The 925E meets DIN standards, has a tilt and swivel screen, a buffered printer port and 16 function keys that can be shifted to 32. An optional graphics board is available. Price is $795. **TeleVideo Systems,** Sunnyvale, CA **Write 175**

GRAPHIC DOT MATRIX PRINTERS

IBM-Compatible



The models 12CQI and 32CQI are graphic matrix printers with speeds of 80 cps to 150 cps. They print 80 or 132 columns at 150 cps in draft mode and 60 cps in correspondence quality mode with a matrix of 16 x 36. With the paper handling capability, the printers can have simultaneous use of cut sheet and fanfold paper. The printers come with form tractor and cut sheet handling and bit map graphics. Price is $499-$995. **Diablo**, Fremont, CA **Write 174**

LINE PRINTER

Prints At 400 LPM

The Linewriter series of printers, which includes models 400 and 800 have a typical print rate of 400 to 800 LPM. The printers are available with 48, 64, 96, 128, and 192 character set capabilities. Available with multiple interfaces, all models have a 4-digit alphanumeric display. Features include cassette ribbon, length select switch, downline loadable VFU, auto configuration I.D. paper tray and eight diagnostic routines. **Centronics Data Computer Corp.**, Hudson, NH **Write 170**

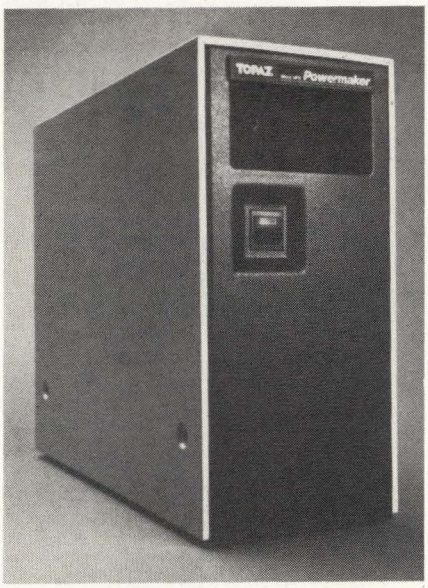
TEST SYSTEM

Announces Radiation of VLSI/VHSI

The Model 4100 Test System, tests for internal latch-up on CMOS VLSI and evaluates radiation hardness on individual VLSI/VHSI dies at the wafer stage of fabrication. Results correlate with LINAC testing procedures. The Model 4100 meets government defense procurement demands for total-dose hardness assurance using an x-ray source. Results correlate with cobalt-60 exposures. The Model 4100 is compatible with functional or parametric device testers. **Advanced Research and Applications Corp.**, Sunnyvale, CA **Write 215**

POWER SYSTEM

Features Line Loss Alarm



The Powermaker Micro UPS is an uninterruptable power system for microcomputers, PC's, and other computer-based equipment. The system provides 75 minutes of sine wave AC power in the event of a blackout. Features of the system include a line-loss alarm, pulse-width-modulation inverter design, and an electronic transfer switch. The system has an optional status monitor which produces a logic signal that interfaces with the user's software to initiate shutdown if primary power fails. **Topaz**, San Diego, CA **Write 216**

DATA COMMUNICATIONS DEVICE

Wrap Around Box Configuration

The WRB/1 is a remotely controlled, data communications device that tests communications lines and local or remote modems. The WRB/1 allows any modem not equipped with a network control capability to become part of, and be controlled by Digilog's Network Analysis and Management System (NAMS). It provides data monitoring, control and restoral capabilities and is designed to operate with a user's existing system. For four-wire, leased-line modems operating from 1200 to 4800 bps, the secondary channel operates at 150 bps. For 9600 bps modems, the secondary channel is set at 75 bps. Price is $950. **Digilog,** Montgomeryville, PA **Write 162**

5¼″ WINCHESTER DISK

With Cartridge Tape Backup

The Medley Subsystem is a high-performance 5¼″ Winchester disk combined with a CDC Sentinel ¼″ cartridge tape drive. Using the SCSI interface the Medley provides storage/backup for users of the DEC QBus and Unibus computers. Included in the system are a 5¼″ Winchester with 36 Mbytes or 110 Mbytes of formatted data storage, and a streaming cartridge tape drive with 70 Mbytes of ¼″ tape storage backup. Included in the subsystem package is the appropriate host adapter; the Emulex UC02 for the QBus applications, and the UC12 for the Unibus. Price is $9,795-$12,855. **Emulex,** Costa Mesa, CA **Write 166**

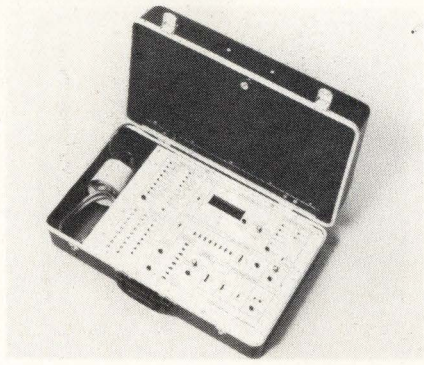
8″ WINCHESTER DISK DRIVE

165.9 Mbyte Unformatted Capacity

The model 73160 is a 8″ Winchester disk drive which employs composite heads and a rotary actuator to provide an unformatted capacity of 165.9 Mbytes with an average access time of 20msec. The disks have a density of 9980 bpi on the inner cylinder and 823 tps with a track density of 800 tpi. Heads fly 14 to 17 microinches above the recording surface with a loading of 9.5 grams. The unit employs Modified Frequency-Modulation techniques with 9.67 MHz data-transfer rates. The drive has six platters with 10 data surfaces and one servo surface. Price is $4,695. **Kennedy Corp.**, Monrovia, CA **Write 165**

¼″ STREAMING CARTRIDGE EXERCISER

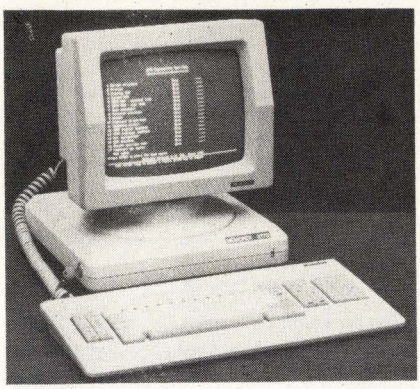
Has QIC-02 Interface



The TQX-500 test exerciser for streaming ¼″ cartridge tape drives is equipped with a QIC-02 interface. Programs in the exerciser command the drive to write and read, move tape and go into streaming mode, with error counts monitored and displayed. Other features allow testing of the drive's internal error and recovery modes. File length selections are one, eight, 1024, and 8192 data blocks. Single-command generation using any of 256 codes enables the testing of special functions, including cartridge lock and response to illegal commands. Price is $2,495. **Wilson Laboratories, Inc.**, Orange, CA **Write 169**

DISPLAY STATION

For IBM 3270 Terminals



The 2178 Display Station is designed for IBM 3270 terminal systems. The display logic, and keyboard module may be interchanged with other 2178s for diagnostics and maintenance. The unit includes a 12″ green phosphor screen, and a keyboard which is less than 2.2″ in height. The 2178 provides users with automatic screen dimming after 20 minutes of inactivity, has a non-glare screen, audible alarm, cursor position indicator and automatic diagnostics. Price is $1,485. **Memorex,** Santa Clara, CA **Write 157**

5¼″ FLOPPY DISK DRIVE

Available in 48 and 96 TPI

The FDA-5000 series is comprised of 48 and 96 TPI drives with single and double density formats and full-height or half-height face plates. The drives are pin for pin compatible with the industry standard interface, and include a direct drive DC servo spindle motor, head positioning via an alpha-winding steel belt, and a proprietary LSI controller chip. **Sumitomo Corp.**, Tokyo, Japan **Write 164**

DIGITAL TRANSMISSION MULTIPLEXER

Bell and CCITT-Compatible

The Codex 6240 Digital Transmission Multiplexer (DTMX) is a high speed time division multiplexer designed to integrate voice, data and digital image applications for transmission over a single link at rates from 56 Kbps to 2.048 Mbps. It accommodates 64 data channels or 64 voice channels, or any mix of these as required. The 6240 offers a programmable capability which permits network reconfiguration from a central site. The 6240 uses a bit interleaved time division multiplex technique and has Bell network (T1/DS1 1.544 Mbps) and CCITT compatibility (T1/G 732 2.048 Mbps). The multiplexer is modular and is available in four system sizes: 16, 32, 48 and 64 channel systems. Price starts at $14,000. **Codex,** Mansfield, MA **Write 173**

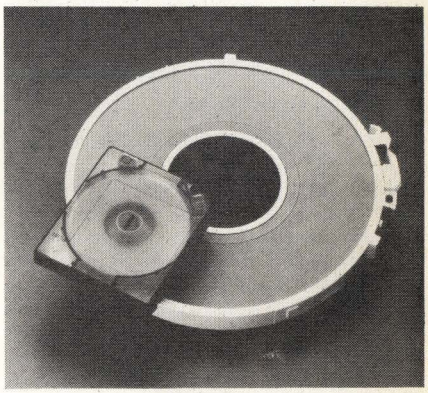
EPROM/EEPROM PROGRAMMER

Handles 512 Kbyte Logic Devices

The Model EP-824 portable programmer is capable of programming EPROMs, EEPROMs, and Intel single-chip microprocessors with a capacity of 512 Kbytes. Programming can be executed by either the membrane keyboard, or by remote control. Internal software for Model EP-824 is written in PL/M or 8085 Assembly Language, and is modular to the extent possible. Data transfer will operate in the interrupt mode and timing for programming pulses is generated by a hardware counter. The 8085A microprocessor operates at 3 MHz and RAM is 64 × 8. Dynamic RAM is used in an organization of 64 × 1. Price is $1,195. **Wavetek-Digelec,** Sunnyvale, CA **Write 179**

TAPE CARTRIDGES

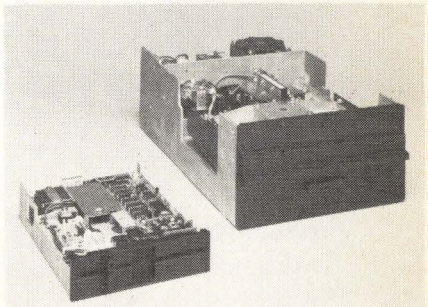
Records 18 Tracks of Data



These drives are part of the IBM 3480 magnetic tape subsystem, which replace reel tape with a cartridge format. The cartridge is one-fourth the size of a 10.5″ reel of magnetic tape and stores 200 million characters. The 4″-by-5″ cartridge is inserted into a slot in an IBM 3480 tape drive. Linear data recording density is 38,000 bpi and 18 tracks of data can be recorded and read. Price, in a typical configuration of one controller and eight drives is $237,910. **IBM,** Rye Brook, NY **Write 161**

HALF-HEIGHT 5.25″ MINIFLOPPY

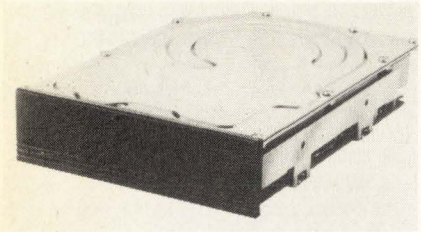
1.6 Mbyte Capacity



The 475 is a double-sided Minifloppy disk with a capacity of 1.6 Mbytes, a data transfer rate of 500 Kbits/sec., and a track-to-track access time of 3 msec. Not only is the performance the same as the 8″ floppy, the recording format is the same as well. The 475 is seen as a logical upgrade for OEMs from the vendor's 1 Mbyte 465. The bit density rises to 9,646 in the 475 which required 600 oersted media. The form factor for the 475 is a 1.63″ (h); 5.75″ (w); 8″ (d). **Shugart Corp.**, Sunnyvale, CA **Write 168**

5¼″ WINCHESTER DISK DRIVE

25.50 Unformatted Capacity



The MR522 5¼″ Winchester disk drive has 25.50 Mbytes of unformatted capacity, 6.37 Mbytes per surface and 10,416 bytes per track. The MR522 has an industry-standard transfer rate, recording format and controller interface requirements, and consumes 18 watts of power. The drive has two platters, four data surfaces and four magnetic data heads. Price is $875 in OEM quantities. **Mitsubishi,** Torrance, CA **Write 171**

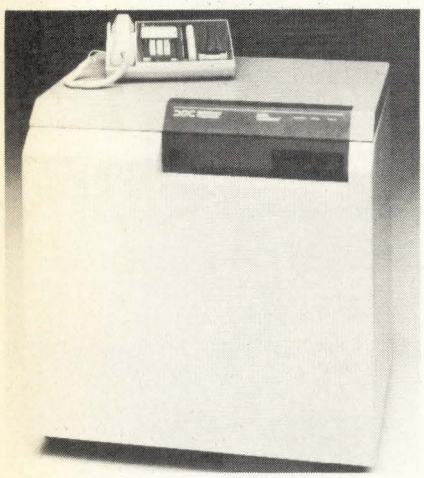
19,200 BPS MODEM

38,400 Aggregate Speed

The MP-192 SM is a voice grade 19,200 bps modem with an integral statistical multiplexer. It achieves aggregate speeds of 38,4000 bps over a 3002 line with D1 conditioning. The MP-192 SM provides 8 or 16 channels of statistical multiplexing with a 2:1 concentration ratio. For synchronous operation, the MP-192 SM supports BiSync, HDLC/SDLC, Honeywell VI 7700, Honeywell GRTS, CCITT X.25, CDC UT 2000, Univac U100, U200, U400, ICL C03, DEC DDCMP and a transparent RTS/CTS mode. Price is $16,900. **Paradyne,** Largo, FL **Write 160**

VOICE PROCESSING SYSTEM

UNIX and Multibus Compatible



The DSC-2000 Voice Server is a voice processing subsystem that reduces voice messages to standard microcomputer data rates by means of a proprietary compression technology. The DSC-2000 is UNIX and Multibus compatible and is designed for integration into existing office automation and PBX systems, for attachment to local area networks and for stand-alone applications. The architecture allows interfacing with two to 16 external voice ports, and permits a variety of Multibus cards to be plugged into a system to support protocols like Ethernet and X-25. OEM prices range from $13,000-$45,000. **Digital Sound Corp.,** Santa Barbara, CA **Write 163**

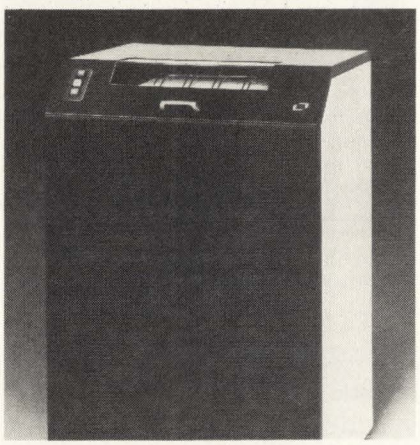
TOTALIZERS AND CONTROLS

For OEM Instrumentation Designers

The Design Mate family of totalizers, count, time and rate controls has been developed for OEM instrumentation designers. The units have 8mm high LCD displays, eight digits in the totalizers and six in the control units. Batteries provide non-volatile memory protection. The Design Mate line is offered with reset and non-reset totalizers and single or dual level, push-button preset controls, with or without serial communications. **Eaton Corp.** Watertown, WI **Write 159**

IBM EMULATOR

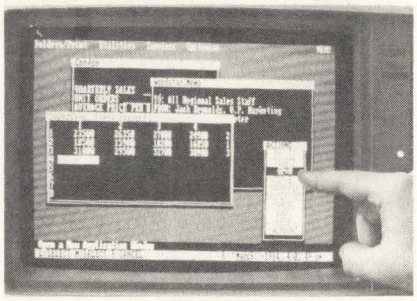
With Processor Interrupt Receptor



The Innovator 202-FC provides 2780/3780 emulation for the Innovator 300 LPM printer system. Features include space compression/expansion, processor interrupt reception, conversational mode, reception of EBCDIC transparent data, component selection, vertical format control, and horizontal format control. The hardware design also includes processor interrupt transmission, switch selectable 2780/3780 modes, switched network/leased line control, auto-answer, switch selectable ASCII/EBCDIC modes, diagnostics, and support of an ASCII terminal as a card reader/punch device. **Innovative Electronics,** Miami, FL **Write 177**

TOUCH SCREEN KIT

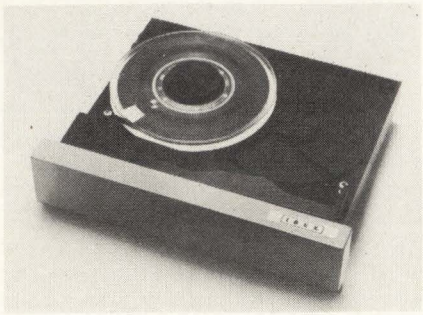
For IBM PC Color Monitor



The Point-1 Color Kit includes a 13″ diagonal touch screen, intelligent controller and an RS-232C serial interface. The screen, available for the IBM PC color monitor is fully programmable and supported by software development tools. With the screen, users can select from menus, position the cursor and create and manipulate graphics by touching the IBM Color Monitor with a fingertip. Price in OEM quantities is $650. **MicroTouch,** Woburn, MA **Write 178**

STREAMING TAPE DRIVES

Provides 138 Mbyte Backup



The PCT-1000 is a IBM-format compatible 9-track streaming tape drive, that provides backup of 138 Mbytes for Winchester hard disks, read/write access to archival data banks, and intercomputer data interchange. The PCT-1000 can handle formats including 800 NRZI, IBM and ANSI; 1600 cpi PE, IBM and ANSI; and dual-density, 3200/1600 cpi. Price is $2,256. **IBEX Computer Corp.,** North Hollywood, CA **Write 176**

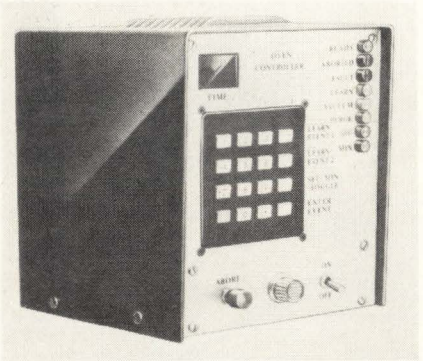
GRAPHICS EDITING PACKAGE

For IDT Color Terminals

Screenmax is a graphics editing package for the IDT family of industrial color graphics terminals. Screenmax operates on an IDT 2200 or IDT 2250 terminal by using the IDT Input Processing Module. The mass store unit, which contains a 10 Mbyte Winchester hard disk drive, is used for program and display storage. The package supports the IDT trackball as an input device. **IDT,** Westerville, OH **Write 172**

CYCLE MASTER SEQUENCER

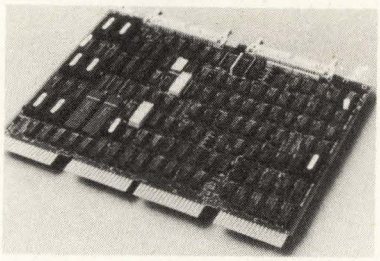
For Programming Electromechanical Processes



The Cycle Master I, is a microprocessor-controlled sequencer for controlling electromechanical processes. The unit allows the programming of two events, with individual time periods of 99 minutes. The events may be cycled in minutes on a continuous basis or up to 99 cycles on a limited basis. The Cycle Master I has a countdown display on a two-digit time indicator, plus light indicators for the operator. A sequence detector system activates a fault light and alarm, should the process be interrupted. **Polaris Electronics Corp.,** Olathe, KA **Write 158**

TAPE COUPLER

Transparent To Software And Diagnostics



The TC13 tape coupler connects industry-standard ½" tape drives to DEC PDP-11 and VAX-11 systems. Tape data rates of 781 Kbyte cps are permitted by the coupler which has a 3.5 Kbyte buffer. The TC13 handles start/stop, streaming and GCR tape drives and has an adaptive streaming capability. The coupler's microprocessor which has been programmed in firmware to detect sequences of operation which support streaming at high speeds and automatically switches to the streaming mode without operator intervention. The coupler executes self-test operations during power-up, and flags errors with a fault LED indicator. Data parity is generated and checked on transfers between the coupler and the tape drive, with errors reported by status bits. Price is $2,000. **Emulex Corp.,** Costa Mesa, CA **Write 197**

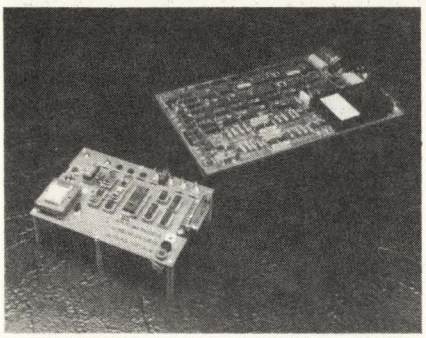
MODEM CHIP SETS

TTL-Compatible

The MSM6926/6927/6946/6947, are CMOS modems which transmit and receive serial, binary data over the switched telephone network using frequency shift keyed (FSK) modulation. The MSM6926 is compatible with CCITT V.21 series data sets. The MSM6927 is compatible with CCITT V.23, MSM6946 with Bell 103, and MSM6947 with Bell 202. The devices have features such as originate and answer modes, built-in and external delay timers, a crystal controlled oscillator on the chip, a TTL compatible digital interface and low power dissipation. Prices in quantities of 100 is $15 (MSM 6926) and $18 (MSM6927). **OKI Semiconductor,** Santa Clara, CA **Write 193**

SINGLE CHIP MODEM

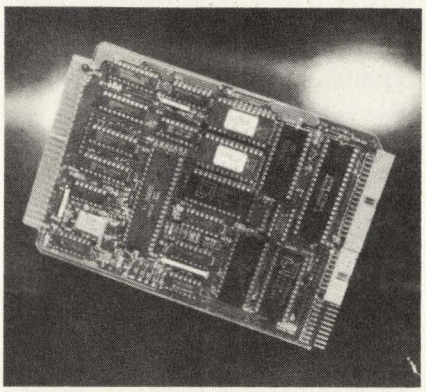
300 Baud Full Duplex FSK



The S3530 is a single-chip 300-baud full-duplex FSK modem. Compatible with the Bell 103/113, the device functions as a CCITT V.21 modem circuit for international applications. The modem is an on-chip RS-232-C control interface which has an automatic-abort function to prevent the S3530 from tying up a system should there be difficulty establishing a data link. Other chip features include transmit and receive filtering and an automatic answer/originate mode selection. The modem is designed for standalone applications and for integration into terminals and computers. It runs off the 3.58 MHz crystal, giving a 4.8-kHz output for UART interface applications. Price in quantities of 1000, is $14.50. **AMI,** Santa Clara, CA **Write 187**

SBC FOR STD BUS

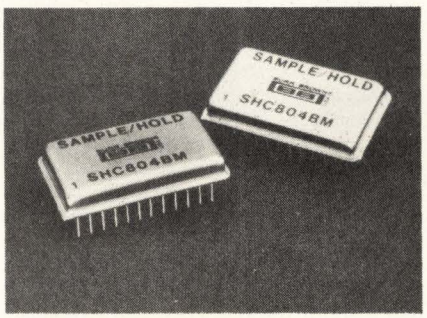
Z80A-Based



The MP6102 is a STD Bus compatible Z80A-based single board computer. Byte-wide memory is located in EPROM with 8K capacity. Three channels of user-definable counter/timer functions are provided by a Z80A-CTC. One channel is software programmable as the time base for the RS-232-C port to 9600 baud. Interrupt control is performed by an AM9519 universal interrupt controller for eight maskable interrupt inputs. An I8255A peripheral interface which supplies 24 bits of multiple mode input or output is responsible for parallel I/O. Price is $570. **Burr-Brown,** Tucson, AZ **Write 186**

SAMPLE/HOLD AMPLIFIERS

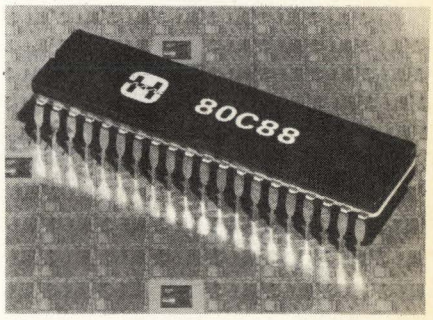
350ns Acquisition Time



The SHC803 and SHC804 are sample/hold amplifiers with an acquisition time of 350nsec within ±0.012% of 10V (±1.2mV) and a sample-to-hold settling time of 150nsec. The units are identical except that SHC803 has an uncommitted front-end buffer amplifier that is used as an impedance buffer for high source-impedance driving circuits. In the sample mode the amplifiers operate as unity-gain inverters. Their signal bandwidth is 15MHz and input voltage rant, ±10V. Outputs are short-circuited protected and provide ±50mA output drive current. Sample/hold input command signals are LSTTL compatible over the specified temperature ranged of −25°C to +85°C. Power supply requirements are ±15V and +5V. Price is $105-$117. **Burr-Brown,** Tucson, AZ **Write 194**

CMOS MICROPROCESSOR

8/16-Bit



The 80C88 CMOS, 8/16-bit microprocessor operates from DC to 5 MHz and is a companion to the 80C86 16-bit, CMOS microprocessor. The 80C88 CPU has a 16-bit internal architecture and interfaces with memories and peripherals via an 8-bit bus. Two operating modes, Minimum and Maximum, support development of systems ranging from dedicated, single processors to large, multiprocessor applications. Inputs and outputs are both TTL and CMOS-compatible. Price is $48.50-$252.76. **Harris,** Melbourne, FL **Write 192**

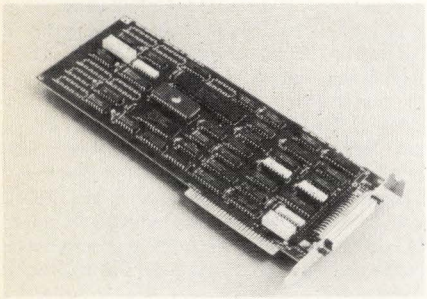
5¼" ESDI WINCHESTER SERIES

85-170 Mbyte Capacity

Models 1353, 1354, and 1355 are Winchester disk drives with capacities of 85, 127, and 170 Mbytes, respectively. The series is compatible with drive controllers available from major controller firms and average access times are less than 30 msec. Prices, respectively, are $1,469, $1,669, and $1,837 in OEM quantities. Evaluation units will ship in the fourth quarter of the year. **Micropolis Corp.,** Chatsworth, CA **Write 210**

SCSI BOARDS

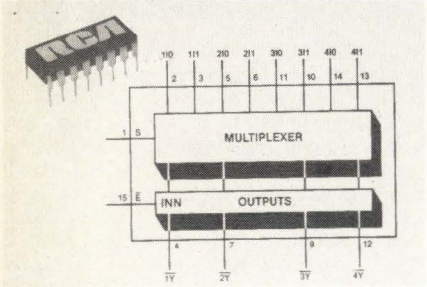
IBM PC Compatible



These two board products are designed for use with the SCSI standard. The first is an IBM PC-compatible host adapter, the IB01. It is a single printed circuit board which can add a Gbyte or more of memory. The second product is an SCSI-based tape controller intended for interfacing Cipher Data Products, Inc.'s model 540 ¼" streaming tape drive to a variety of CPUs. The product, called the Titleist, supports full SCSI arbitration for eight host and/or peripheral devices. The controller is a single PC board that is housed in the Cipher 540 transport. Prices are $345 (IB01) and $435. (Titleist). **Emulex Corp.,** Costa Mesa, CA **Write 209**

INVERTING MULTIPLEXERS

For CMOS Systems



The CD74HC158 and CD74HCT158 are a pair of Quad 2-Input Inverting Multiplexers. CD74HC158 types are intended for all-CMOS systems. The CD74HCT158 types are drop-in replacements for LSTTL (bipolar) logic. The CD74HC/HCT158 multiplexers select four bits of data from one of two sources under the control of a common select input line. Each bit in the selected word appears on an output line in complemented form. A typical application of HC/HCT158 devices is the movement of data from two 4-bit registers to four common output lines. Prices in quantities of 100, are $.74 (HC158) and $.81 (HCT158). **RCA/Solid State,** Somerville, NJ **Write 204**

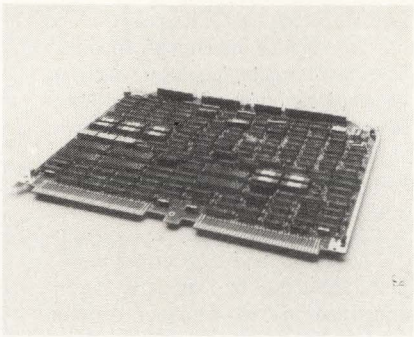
SINGLE BOARD COMPUTER

With 80188 Processor

The I-Bus R188 is designed as a central processing unit around which to build a PC bus based system. On board there are 64K of RAM, with parity, and a provision for 256K. ROM allows 8K to 32K of BIOS and from 8 K to 128K of user memory. The boards' RS-232C port operates at a fixed rate of 9600 baud and is used as a console I/O port to an asynch terminal. The processor is compatible with all PC expansion cards and complies with the IBM PC bus interface. **I-Bus Systems,** San Diego, CA **Write 198**

DISK/TAPE CONTROLLER

For T.I. 600/800 Series



The Spectra 126 is a disk/tape controller that supports TI's 990 and 600/800 computer series and emulates TI's CDI400, DS80/300 and WDMT disk and TI 979 tape subsystems. The single-board controller is fully compatible with TI's DX10 operating system and diagnostic software. The Spectra 126 attaches any combination of two SMD disks and four ½" tape drives, including GCR. It can support transfer rates of 2.0 Mbyte/sec disk and 800 Kbyte/sec tape. Drive mixing and mapping is switch selectable from 128 configurations located in one PROM. **Spectralogic,** Sunnyvale, CA **Write 191**

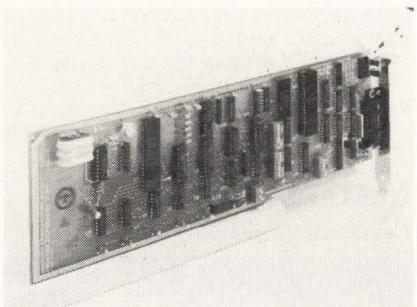
LOGIC ARRAYS

Supports ECL, TTL, ECL/TTL

The Q3500S, the initial array of AMCC's Q3500 series, operates at typical gate equivalent delays of 0.5ns with power consumption remaining at 3.5 W. Programmability at the macro level permits gate delays of 275 ps or power consumption of 0.7 mw/gate. I/O pair delay is 5.0 ns for TTL and 1.0 ns for ECL modes. The Q3500 series has been developed for military and commercial applications in computers, peripherals, tests, instrumentation and communications. The array has 120 programmable I/O cells for interface to TTL, ECL 10K, ECL 100K or 5 volts referenced ECL. The I/O's also support a 20 ma TTL output drive or an ECL output drive of 25 ohms. **AMCC,** San Diego, CA **Write 207**

COMMUNICATION CONTROLLER

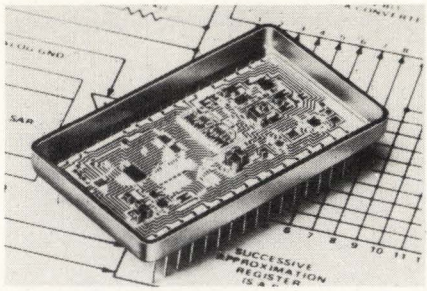
With Multiple Protocol Support



The Advanced Communication Controller allows communication with other computer systems using different protocols. The board allows communication rates of 19.2 K and optional features include, an IBM-PC compatible printer interface, and a real time clock. Design features include multiple protocol support, DMA interface and interrupts, intelligent communications controller chip (Z80 SIO), and a parallel port option. **Frontier Technologies Corp,** Milwaukee, WI **Write 201**

A/D CONVERTER HYBRID

12-Bit



The ADC-00403 is a militarized 12-bit 2 usec hybrid A/D converter. It is a successive approximation device in a 32 pin hermetic TDIP for military and industrial data conversion applications. The hybrid can be used as a pin-for-pin replacement for ADC85 and ADC 87 types. It has a precision internal reference and six pin programmable unipolar and bipolar input voltage ranges. Linearity, gain and offset errors are ±0.01% FSR, ±0.1% FSR, and ±0.05% FSR, respectively. Prices are $169 and $219 in quantities of 100. **ILC Data Device Corp.,** Bohemia, NY **Write 203**

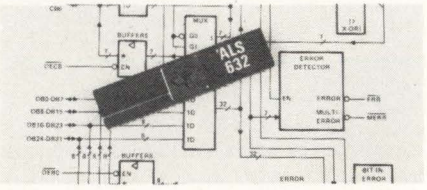
MULTIPLE DISK CONTROLLER

Supports Four Rigid or Floppy Disks

The SCN68454 and SCB68459 are two VLSI circuits which control four hard and floppy disk drives, in any combination. The two-chip set integrates the equivalent functions of 90 circuits for 8-, 16-, and 32-bit computer system disk control applications. The SCN 68454 is an IMDC chip and the SCB68459, a DPLL, both of which have programmable error correction codes, programmable soft and hard sectors, automatical bad sector handling, DMA and two interfaces. One is a host interface to 8- and 16-bit data buses, and the other a disk drive interface. The SCN68459 DPLL has an operating range of 100 KHz to 20MHz and a FIFO buffer of 128 bytes. The IMDC supports FM and MFM data formats with data rates of 10Mbits/sec for MFM and 2 Mbits/sec for FM. Price is $99.95 (IMDC) and $21.00 (DPLL). **Signetics,** Sunnyvale, CA **Write 190**

32-BIT PARALLEL EDAC

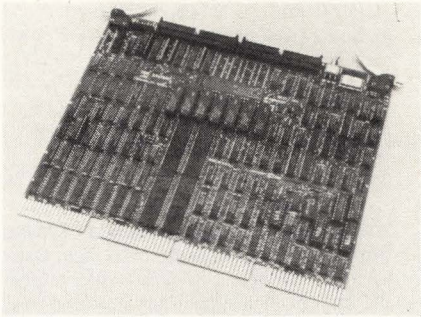
With Single Chip Error Correction



The SN74ALS632 is a stand-alone, 32-bit parallel error detection and correction (EDAC) circuit which drives buses directly without the need for external bus drivers. The products detect and correct single-bit errors and detect and flag dual-bit errors. They also flag gross-error conditions of all-high or all-low outputs. The 'ALS632 indicates a single-bit error in 40ns and a double-bit error in 60ns. Corrected output data appears on the bus 58ns after the data input has been processed. The SN54ALS' military-temperature-range versions will offer corresponding performance of 43 ns, 67 ns, and 65 ns. Price in quantities of 1,000 is $79.42. **Texas Instruments**, Dallas, TX **Write 195**

Q-BUS CONTROLLER

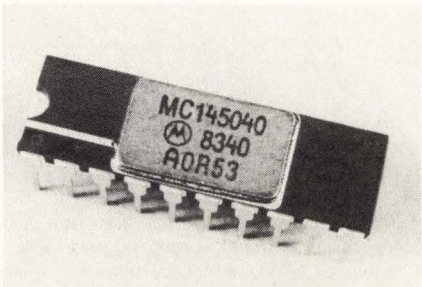
Handles 9 Track Drives



The TS11/TSV05 compatible tape controller/coupler for the Q-bus is designed for tape drives with embedded formatters. The controller handles 9 track magnetic tape drives from one quad board. Different operating modes and Q-bus address selection can be configured by the operator console input to nonvolatile static RAM as units are changed or added. Data density of an 800 CPI (NRZI), 1600 CPI (PE), 3200 CPI (Cipher) or 6250 CPI (GCR) is supported. The amount of buffer storage exceeds 16 Kbytes which effects transfers between the controller and tape drive to ensure continuous tape streaming. **MDB,** Orange, CA **Write 199**

A/D CONVERTERS

With Serial Interface



The MC145040/MC145041 are 8-bit A/D converters with serial interface ports that are compatible with SPI, Microwire and other similar interfaces. The MC145040 has an operating supply voltage range of 4.0V to 6.0V. Its operating temperature range is −55°C to +125°C and it has a conversion rate of 16ms for the standard part. The inputs are TTL-compatible and can be driven with CMOS parts as well. The 20 pin DIP packages provide for 11 analog channels. In quantities of 100 price is (MC145040) $2.89 and (MC145041) $2.99. **Motorola,** Austin, TX **Write 196**

12-BIT INTEGRATING A/D CONVERTER

With Microprocessor Interface

The ADC-7109 is an integrating A/D converter which can be interfaced to any 8- or 16-bit microprocessor data bus. The ADC-7109 includes a buffer amplifier, integrator, comparator, 12-bit binary counter and three-state outputs. Data outputs can be grouped in two 8-bit bytes, each activated by its own byte-enable signal, and a master chip-enable line. A UART handshake mode is provided to operate with industry-standard UART's in the serial data transmission mode. The ADC-7109 operates over a temperature range of 0°C to +70°C. Price in quantities of 100 is $11.25. **Datel,** Mansfield, MA **Write 189**

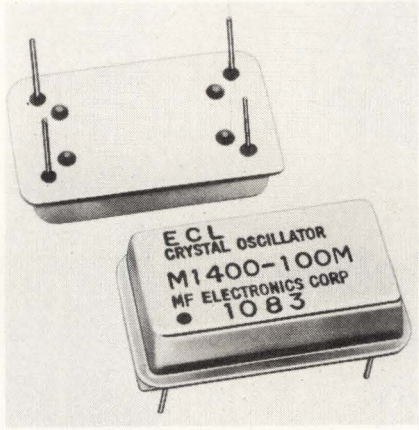
UNIVERSAL DISK CONTROLLER

For 5¼" or 8" Flexible Drives

The SECS 80/208 flexible disk controller is capable of controlling virtually any double or single-sided standard 8" or mini 5¼" flexible disk drive. The controller is programmable, enabling track-to-track access, head loading, and head unloading characteristics to be program specified for the drive model selected. The 80/208 is based on the Intel 8272 floppy disk controller, enabling it to read and write single and multiple sectors. Price is $4,495. **Electronic Memories & Magnetics Corp.,** Encino, CA **Write 208**

CRYSTAL CLOCK OSCILLATORS

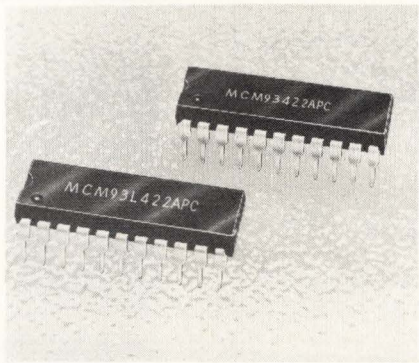
10 to 125 MHz



These Crystal Clock Oscillators are for commercial or industrial applications and are available in frequencies of 10 to 125 MHz. The metal package is hermetically sealed by resistance weld, with a glass-to-metal seal connector which may be soldered or plugged into a socket. The oscillators have monolythic ECL 10,000 outputs and come in fourteen models that cover .0025% thru 1.0%. **MF Electronics,** New Rochelle, NY **Write 200**

256 × 4-BIT TTL RAM SERIES

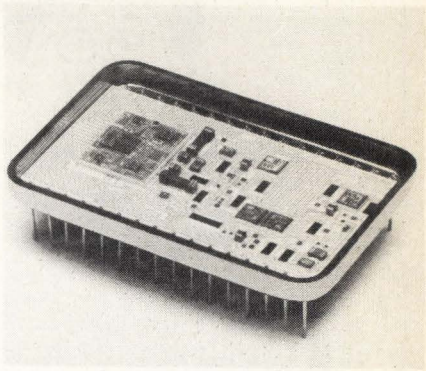
45ns Acquisition Time



The MCM93422A and MCM93L422A are 1024-bit bipolar RAMs with access times of 35ns and 45ns, respectively. The parts have a power dissipation of 0.26 m W/bit and provide 3-state outputs to drive bus-organized systems and/or highly capacitive loads. The series is TTL compatible and is offered in JEDEC standard 22-pin, 400 mil wide plastic or ceramic packages. Price in quantities of 100 is $9.50 (plastic), and $10.76 (ceramic). **Motorola,** Phoenix, AZ **Write 188**

16-BIT D/R CONVERTER

Double Buffered D/R Inputs



The HDR2116 is a 16-bit converter which has a power output of 2-VA. Packaged as a 32-pin hybrid, the converter has 1 arc-minute accuracy and 0.03% max scale factor variation. The HDR2116 has double-buffered inputs, is compatible with both 8- and 16-bit microprocessors and has protected analog sine and cosine outputs. Price is $345. **Natel Engineering,** Simi Valley, CA **Write 202**

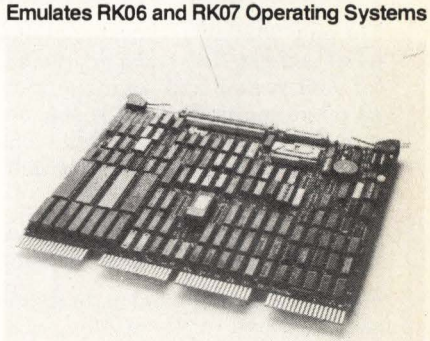
Q-BUS COMPUTER SYSTEM

250W Switching Power Supply

The VQ-11 family of Q-Bus computer system packages is intended for system integrators and OEMs who specialize in DEC Q-Bus hardware and compatible software. The modular package consists of a 250W switching power supply, an eight slot Q-Bus card cage, dual fans and front panel controls which allow 150 combinations of floppies, Winchesters and tape drives to be mounted within the box. The eight slot cage can accommodate DEC CPUs with additional room for several Mbytes of system memory and controllers. A typical configuration includes two RX02 emulating floppies, a RL02 emulating Winchester, an 11/23 CPU, 1/4 Mbyte RAM and 4 serial I/O ports. Price is $7,620. **Zoltech,** Van Nuys, CA **Write 205**

I/O DISK CONTROLLER

Emulates RK06 and RK07 Operating Systems



The Model DQ215 Winchester disk controller interfaces two 8" and/or 14" SMD I/O compatible drives to LSI-11 thru 11/73 and MICRO/PDP-11 computers. The quad module operates when it is plugged into one Q-Bus slot and connected to drive(s) by flat cables. The controller has universal formatting, 56-bit ECC, 22-bit addressing for 4 Mbyte data access and is compatible with RT-11, RSX-11 and RSTS operating systems. Price in quantities of 50 is $1,150. **Dilog,** Garden Grove, CA **Write 206**

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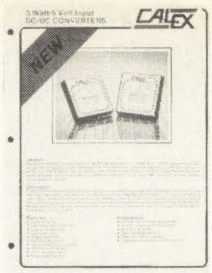
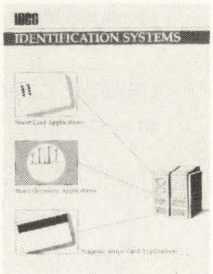
Write 76 on Reader Inquiry Card

NEW LITERATURE



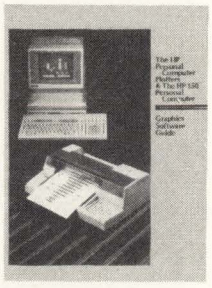
DC/DC Converter Data Sheet. This data sheet describes two power sources for converting computer power to low noise amplifier power. The 5D15.100 and 5D12.125 DC/DC converters operate from a 5 Volt computer power bus, and provide outputs of +/−15VDC at 100 mA and +/−12VDC at 125 mA respectively. They have 500 volts of isolation between input and output, input current noise of 40 mA, and 30 mV peak to peak output noise.
Calex **Write 260**



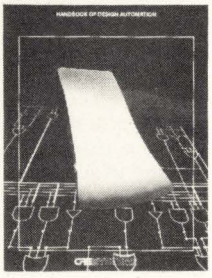
Voice Response and Identification Systems Brochures. Two brochures from Input Output Computer Services, Inc. discuss voice response and identification systems for large data bases. Voice Response Systems access a data base and vocalized output via telephones. Identification Systems integrate a microchip card, magnetic strip card, and hand geometry technologies.
Input Output Computer Services **Write 256**

Power Assemblies Brochure. This brochure from Sorenson Co. describes over 65 custom and semi-custom assemblies off-the-shelf for applications where programmable power supplies are required. The brochure gives specifications, schematic drawings and illustrations of 19″ rack assemblies.
Sorensen **Write 253**

Fiberoptics Brochure. This brochure from Ensign-Bickford Optics Co. describes their line of fiber optic cables designed for data communications and process control. The "hard-clad" silica fibers are incorporated into cable assemblies for short-haul (10- to 100-meter links), bulk cable in kilometer lengths and special cables for military applications.
Ensign-Bickford **Write 255**



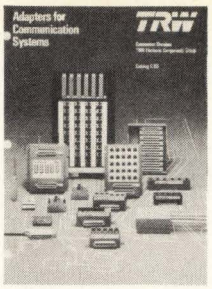
Graphics Software Guide. This guide from Hewlett-Packard includes six data sheets describing features of software packages for connecting its plotters to the HP 150. Each page consists of sample plots to illustrate the graphics capability and a list of hardware requirements. System configurations, connection instructions and communications verification are included.
Hewlett-Packard **Write 267**



Design Automated Handbook. This 148-page book from CAE Systems, Inc. provides information on CAE workstations and systems. The book studies the design process, surveys available CAE software tools as well as the systems that implement them. It also evaluates design automation systems. Appendixes include a glossary, bibliography, and a listing of 107 CAE hardware and software vendors with addresses and telephone numbers.
CAE Systems **Write 254**

NEW LITERATURE

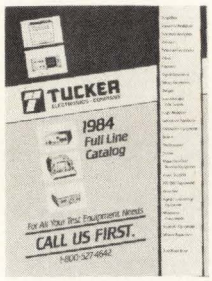
Adapter Products Catalog. This 32-page catalog from the Connector Div. of TRW Electronic Components Group details adapter products for data communications and telecommunications system applications. Using charts, illustrations, photos and diagrams, the catalog describes modular adapters and accessories.
TRW **Write 251**



Quality Statistics Brochure. This data sheet from Hewlett-Packard Co. on a cluster-based quality statistics describes how in-circuit board test and repair data are transformed into information. The three major classes of data collected are management, production and component. Also discussed is the transfer of data coming from a number of sources to other systems.
Hewlett-Packard **Write 250**

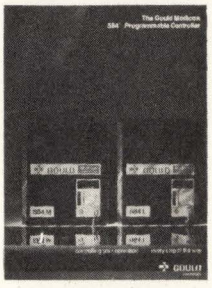
Test System Flyer. Borso's Engineering, Inc.'s Fleet-1 automated test system, designed to test bus-structured TTL circuit boards, is described in this flyer. Specifications, operational features and programming, fault detection and interconnection descriptions are provided.
Borso's Engineering **Write 257**

Test Equipment Catalog. This catalog from Tucker Electronics Co. contains over 250 pages of descriptions, specifications and prices on 4,000 new and reconditioned electronic test instruments. All equipment is for sale, and most items are also available for short-term rental.
Tucker **Write 269**



Fiber Optic Brochure. This four-page brochure from Welch Allyn, Inc., Industrial Products Div., discusses fiber optic solutions for a variety of problems such as transmitting data to inaccessible locations, channeling light to multiple stations, and ducting cold light into heat sensitive areas. Application information, color photos and illustrations are also provided.
Welch Allyn **Write 271**

Programmable Controllers Brochure. This eight-page brochure from Gould, Inc., Programmable Control Div., describes its mid-size Modicon 584M and Modicon 584L programmable controllers. The 584M, with as many as 2,048 control application points, performs functions such as data acquisition, numerical calculations, distributed control, supervisory control, reporting and monitoring. The 584L has as many as 8,192 control points and memory sizes up to 32K words.
Gould **Write 265**



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CALENDAR

July 31-August 3

Hands-On Microprocessor Troubleshooting. Boston, MA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

August 13-14

CAD/CAM: Concepts, Systems, and Applications. Worcester, MA. Contact: Kathy Shaw, Office of Continuing Education, Higgins House, Worcester Polytechnic Institute, Worcester, MA 01609. (617) 793-5517.

August 13-14

The SuperMicros. Washington, D.C. Contact: The George Washington University, School of Engineering and Applied Science, Washington, D.C. 20052. (202) 676-6106.

August 13-15

1984 ASME International Computers in Engineering Conference and Exhibit. Las Vegas, Nevada. Contact: Mary Benedict, The American Society of Mechanical Engineers, 345 East 47th Street, 13M, New York, NY 10017. (212) 705-7100.

August 15-17

Engineering Workstations. Andover, MA. Contact: Institute for Graphic Communication, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

September 10-13

10th Annual Advanced Control Conference. West Lafayette, IN. Contact: Control Engineering, PO Box 1030, Barrington, IL 60010. (312) 381-1840.

September 11-14

Computer Network Design and Protocols. San Diego, CA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

September 11-14

Computer Graphics. San Diego, CA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

September 12-14

Eurographics '84. Copenhagen-Denmark. Contact: Eurographics '84, Dis Congress Service, Linde Allé 48, DK-2720 Vanlose/Copenhagen, Denmark. Tele. 45 + 1 + 712244.

September 16-20

Compcon Fall '84. Arlington, VA. Contact: Compcon Fall 84, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

September 17-21

The 8th International Fiber Optic Communication and Local Area Networks Exposition. Las Vegas, NV. Contact: Michael O'Bryant, Information Gatekeepers, Inc., 138 Brighton Ave., Boston, MA 02134. (617) 787-1776.

September 18-20

Computers in Cardiology. Park City, Utah. Contact: Computers in Cardiology, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

September 18-21

Knowledge-Based Systems, AI and 5th Generation Computing. Boston, MA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

September 18-21

Computer Network Design and Protocols. Washington, D.C. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

September 25-28

Implementing Local Area Networks. Washington, D.C., Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

September 25-28

State-of-the-Art Robot Systems. Palo Alto, CA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

September 26-28

Eurocon '84, 6th Conference on Electrotechnics: Computers in Communication and Control (IEEE, et. al.) Brighton, England. Contact: Conference Secretariat, IEE, Savoy Place, London WC2R OBL, United Kingdom. Tele. 01-240 1871, ext. 337.

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