A CAHNERS PUBLICATION
MARCH 18, 1987

EDN

Breadboarding facilitates gate-array development

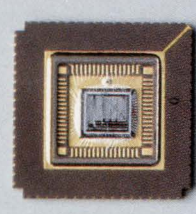
CMOS FIFO buffers employ memory architectures

Fast-settling op amps aid data-conversion tasks

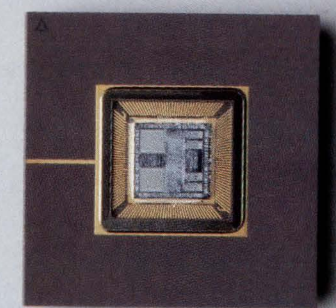
Electro '87 preview

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

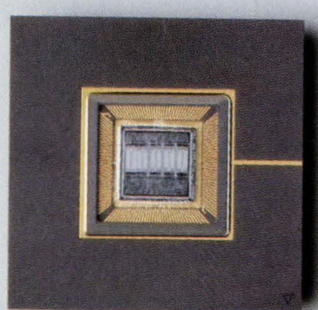
Complex layouts emerge from low-cost systems



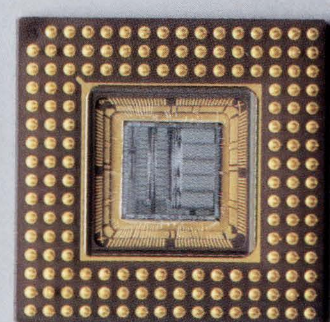
Our MACGEN silicon compiler developed the world's fastest 16-bit multiplier accumulator.



High Performance cell-based 1750 CPU combines logic, ROM and processors.

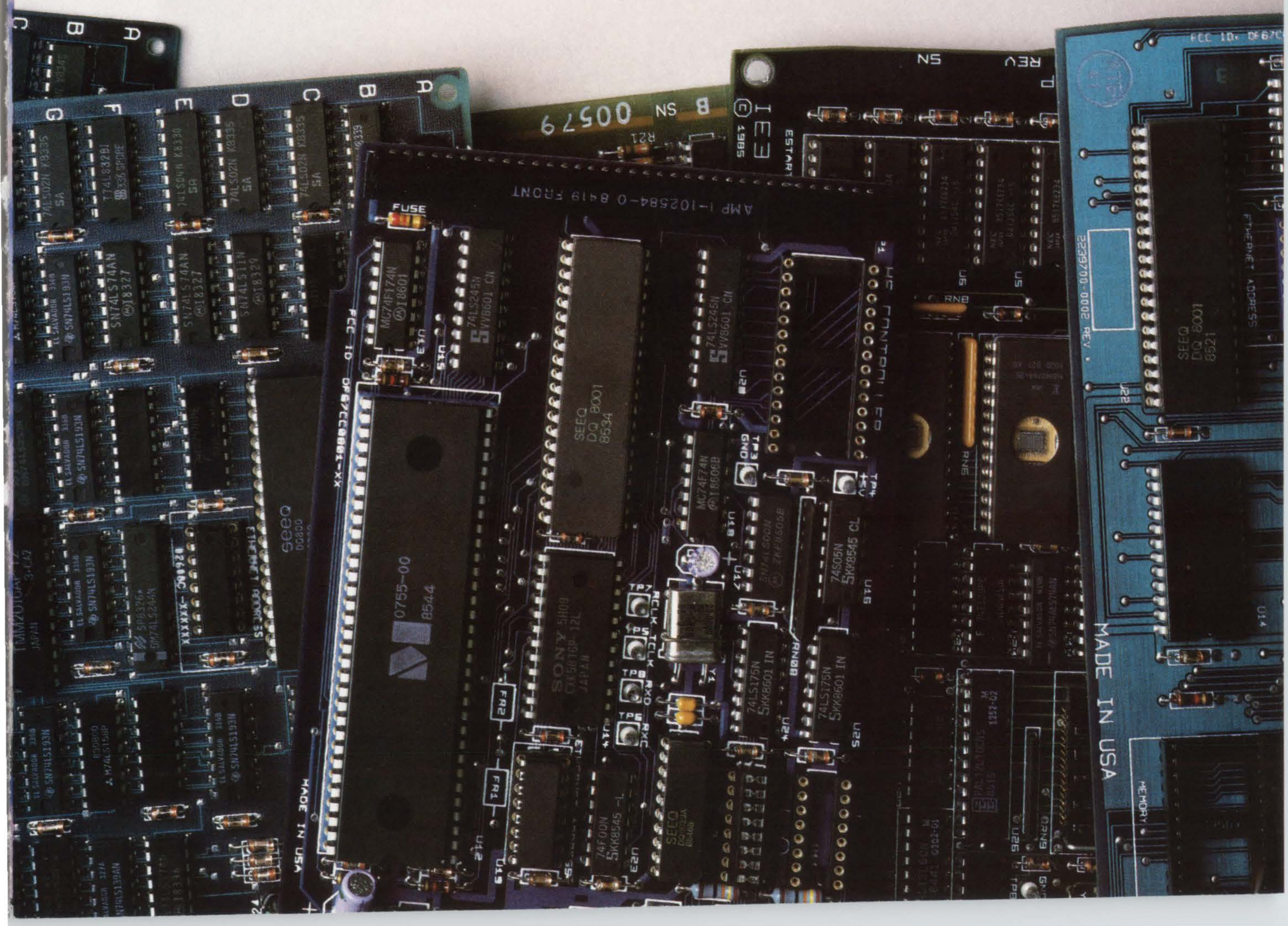


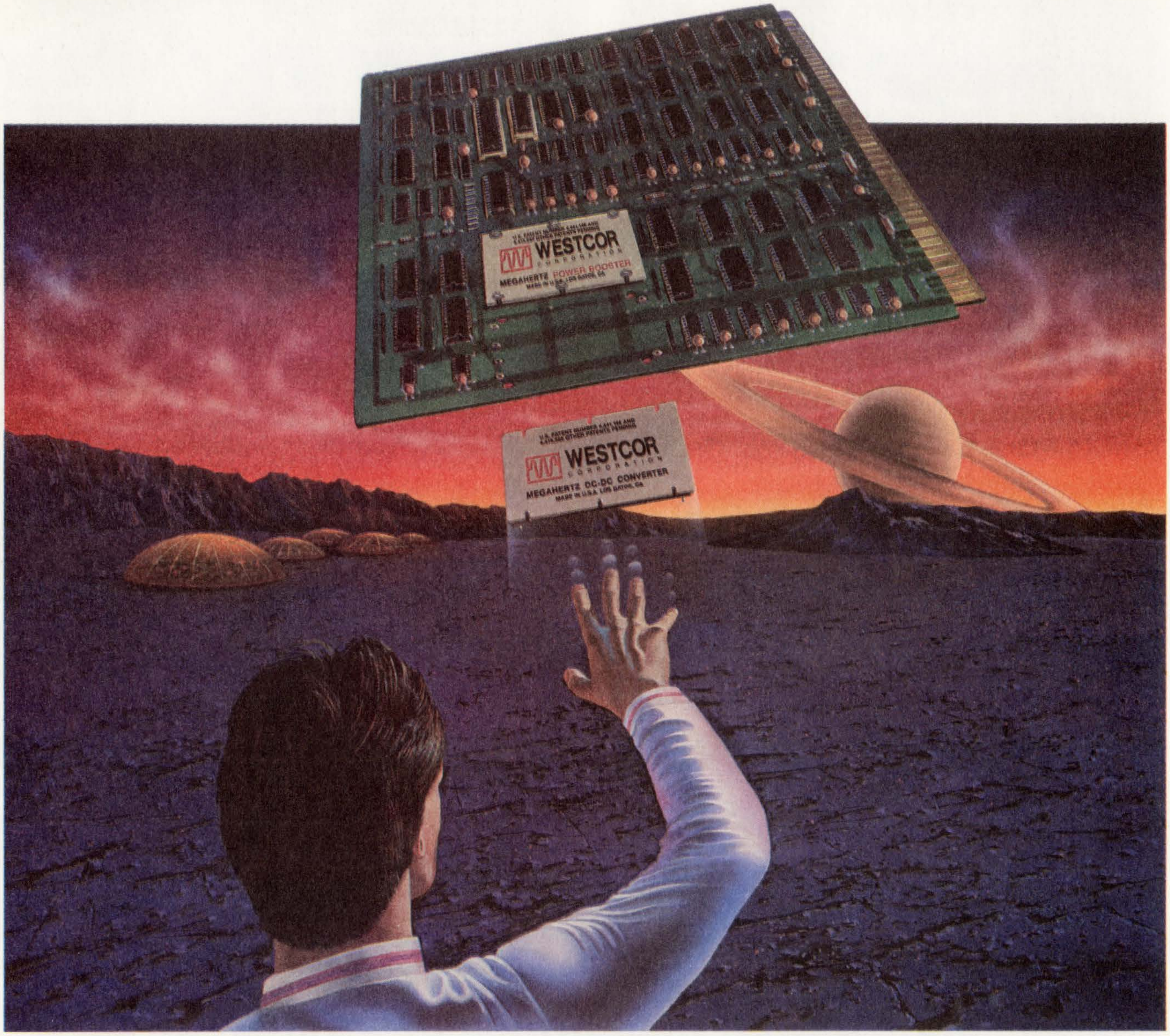
Structured Arrays combine high-density memories with up to 41,000 logic gates.



Channel-free Compacted Arrays combine logic and memory functions with up to 129,000 available (up to 70,000 utilized) gates.

HOW TO AVOID GOING OVERBOARD.

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MEGAHERTZ POWER BOOSTER
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WAVETEK®

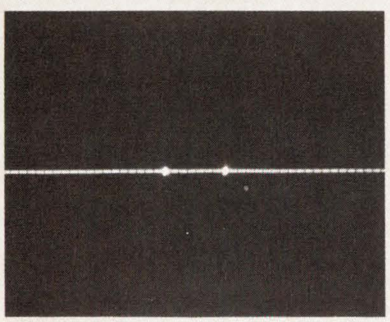
Make any waveform come to life.

Now you can create arbitrary waveforms in real time just by using your oscilloscope screen. Our new Model 75 Arbitrary Waveform Generator gives you the tools to quickly produce any arbitrary waveshape: insert standard waveform segments, adjust their offset and amplitude, and create non-standard waveforms with our "thumbtack and rubberband" editing system. You can program an entire function visually without ever entering an x/y coordinate.

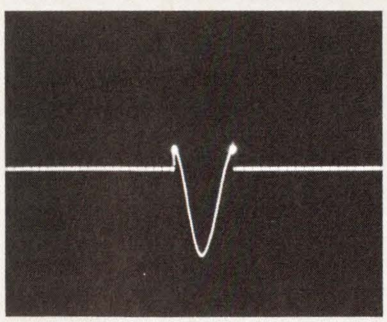
With more than 4,000 vertical and 8,000 horizontal points available, the most complex waveforms can be created and then stored in Model 75's nonvolatile memory. You can play the waveform back at any rate, then edit it point by point.

Since the Model 75 costs just $2,095, you might want to buy several. Then you could link two or more Model 75's together and use their internal counters to produce sequences of "normal" waveforms mixed with bursts of "abnormal" ones, or create multiples of a function with phase displacement. An optional IEEE-488 [GPIB] or RS232C interface is available for only $395.

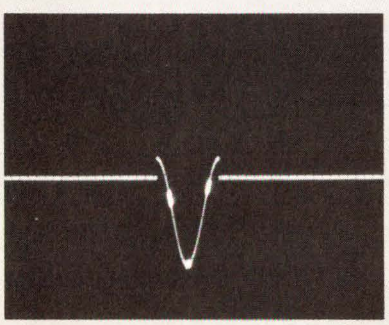
For more information call or write Wavetek San Diego, P.O. Box 85265, 9045 Balboa Ave., San Diego, CA 92138. Phone [619] 279-2200; TWX [910] 335-2007.



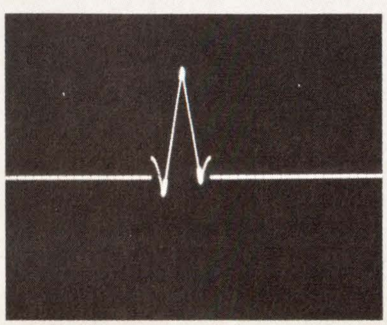
1. Place "thumbtack" markers.



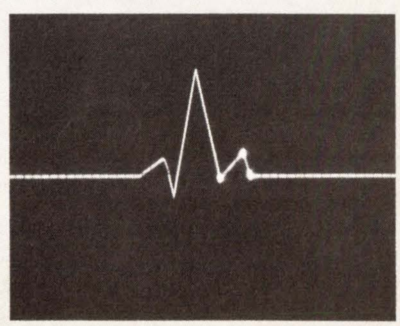
2. Insert standard waveform.



3. Reset "thumbtack" marker positions.



4. Stretch "rubberband" with edit cursor.



5. Move "thumbtacks" and complete waveform editing.

Circle 48 for demonstration

Circle 9 for literature

Volume 32, Number 6 EDN March 18, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

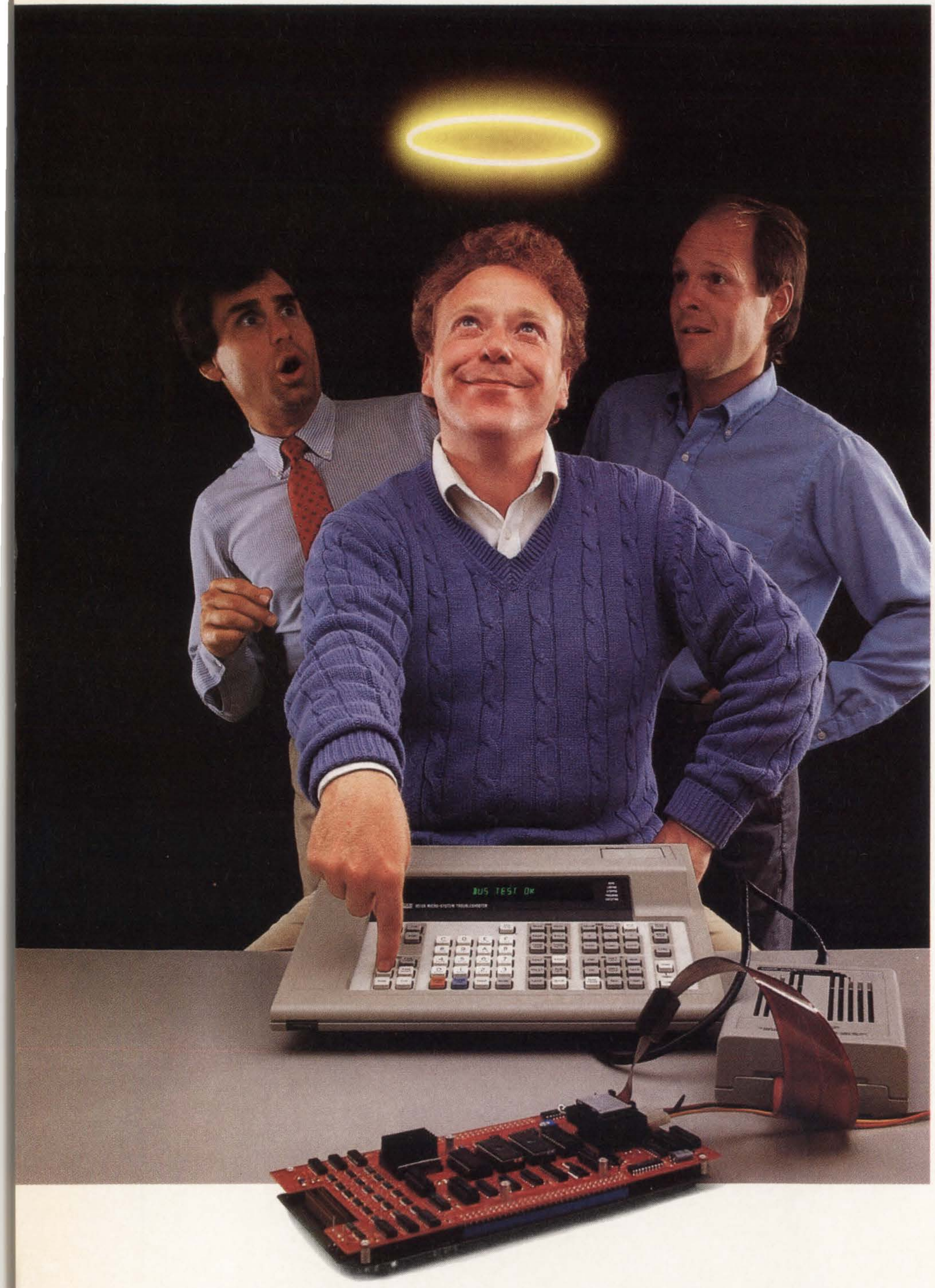
***On the cover:** Layout projects that once required a dedicated workstation or the use of a service bureau can now be accomplished on personal computers, thanks to high-performance software packages that cost less than $15,000. See pg 138. (Photo courtesy Racal-Redac)*

DESIGN FEATURES

Continued on page 7

EDN (ISSN 0012-7515) is published 45 times a year, biweekly with one additional issue in January, February, March, August, and December, two additional issues in April, June, July, September, and November, and three additional issues in May and October by Cahners Publishing Co, a Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158. William M Platt, President; Terrence M McDermott, Executive Vice President; Jerry D Neth, Vice President of Publishing Operations; J J Walsh, Financial Vice President/Magazine Division; Thomas J Dellamaria, Vice President Production & Manufacturing; Frank Sibley, Group Vice President. Copyright 1987 by Reed Publishing USA, a division of Reed Holdings Inc; Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer, Robert L Krakoff, Executive Vice President. Circulation records maintained at Cahners Publishing Co, 270 St Paul St, Denver, CO 80206. Second class postage paid at Denver, CO 80202 and additional mailing offices. Postmaster: Send address changes to EDN, 270 St Paul St, Denver, CO 80206.

How to be perfect to a fault.



Get your product to market faster. Save weeks debugging each prototype circuit board. Immediately.

What a faultless package: Fluke's 9000 Series of micro-based *hardware* debuggers. Plus the *free* troubleshooting training. And Fluke support when and where you need it.

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- Support for over 50 microprocessors.
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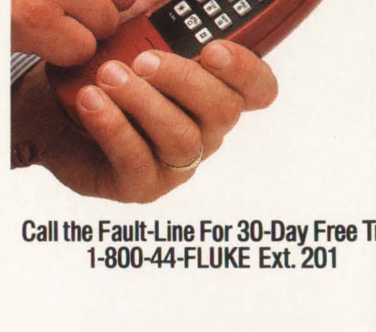
From the moment you plug the interface pod into the microprocessor socket, you'll save time, money and deadlines.

And become faultless in the eyes of man.



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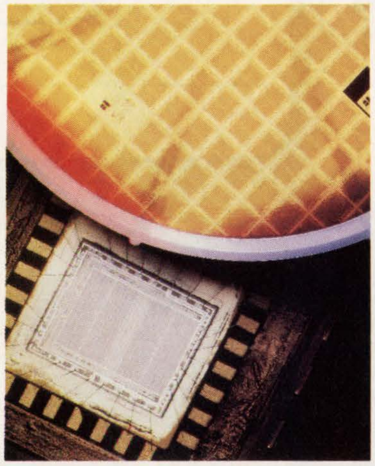
Continued from page 5



CMOS FIFO buffers are employing memory architectures to achieve high capacities and fast data rates. Furthermore, the devices don't exhibit the ripple-through delays that contribute to the input/output latency time inherent in shift-register versions (pg 65).

TECHNOLOGY UPDATE

PRODUCT UPDATE

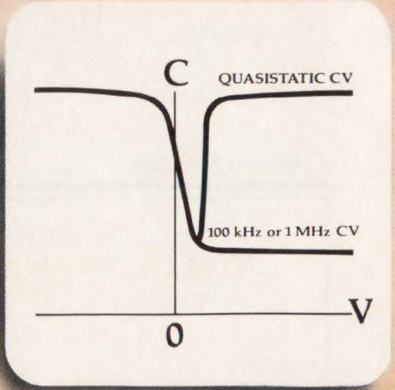
DESIGN IDEAS

Continued on page 9

Advertising and editorial offices: 275 Washington St, Newton, MA 02158. Phone (617) 964-3030. Subscription offices: 270 St Paul St, Denver, CO 80206. Phone (303) 388-4511. EDN is circulated without charge to those qualified. Subscription to others: US, $95/year, $6/copy; Canada and Mexico, $110/year, $8/copy; Europe Air Mail, $135/year, $10/copy; all other nations surface mail, $135/year, $10/copy; all other nations Air Mail, $200/year. Special issue prices may vary. Send requests for qualification forms and/or change of address to subscription office.

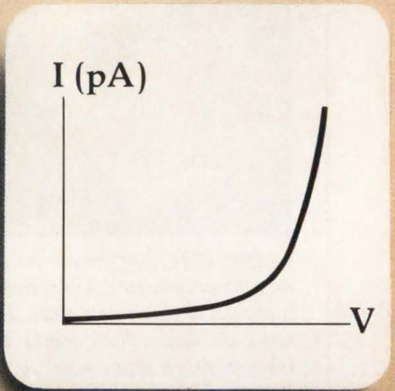
KEITHLEY ON SEMICONDUCTOR MEASUREMENTS:

PROVE IT.



For difficult semiconductor measurements, you need assurance that your instrumentation can correctly verify process, wafer, or device specifications. Not being sure can reduce confidence in your test results.

These difficult semiconductor measurements need a broad line of instruments specifically designed to solve semiconductor source, measure, and connect problems. Keithley has them. Our evidence:



SOURCING INSTRUMENTS

All our low-noise current, voltage and crossover sources have built-in memory so you can program a sequence of levels. Some also feature sensitivity to below 1 pA; others go to 1 A at 100 V, or 10 A at 10 V.

MEASURING INSTRUMENTS

Measure currents from 10 aA (10^{-17}) to 10 A, and voltages from 10 nV to 1 kV. Up to 6½ digit resolution and speeds up to 100 kHz at 16 bits. Measure resistances from 10 $\mu\Omega$ to 10 PΩ (10^{16} Ω). Our measuring instrument line also includes an IEEE-488 thermometer and 1.3-GHz counter/timer.

TWO NEW CV METERS

One is a 100 kHz/1 MHz CV analyzer with sensitivity better than 1 fF, an extended range option to 20 nF, powerful math functions and built-in cable correction and plotter drive. On-board features also include low 15 mV rms drive voltage, 4½ digit resolution and internal memory to store front panel setups. The other is a quasistatic CV meter using a new technique to directly correct for background currents and help you find the right sweep rate faster.

CONNECTING INSTRUMENTS

Programmable switches with 17 different cards to choose from, some specified to 500 MHz. Other capabilities include matrix, picoamp sensitivity, and up to 10^{15} Ω isolation.

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Not only do these products perform individually, they are designed to be used together in a variety of combinations. Evidence: we give you three ways to measure Hall effect. First, a plug-in card with all needed sensitive amplifiers, cables, and switching for use with our low-cost programmable switch. Second, an instrument package with instructions on how to make your own system; or third, a complete turnkey system.

All our products feature compatible hardware, are easy to set up, and use a language common to other Keithley instruments. That saves you from learning a new language for every new instrument. Further, the telephone assistance provided by the application engineers at our Information Center helps you find out specifically how to use Keithley instruments to solve your unique semiconductor measurement problems.

We've stated that Keithley has the ability to do semiconductor measurements. Now it's time to prove it.

Call the Information Center at (216) 248-0400, or write Keithley Instruments, 28775 Aurora Road, Cleveland, Ohio 44139.

The best proof of our leadership in sensitive instruments is the fact that we've specialized in them for the last 40 years. But the past is prologue. Today we make the total spectrum of semiconductor test instruments which SOURCE, MEASURE, and CONNECT signals in semiconductor research, design and test labs.

SOURCE • MEASURE • CONNECT

KEITHLEY

Continued from page 7

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Until now, printed circuit board layout was an isolated process: done on a special-purpose workstation at the "back end" of the design effort. But Mentor Graphics saw it a different way. Since PCB layout brings together all the elements created by "front end" CAE tools, it should be integrated with those tools.

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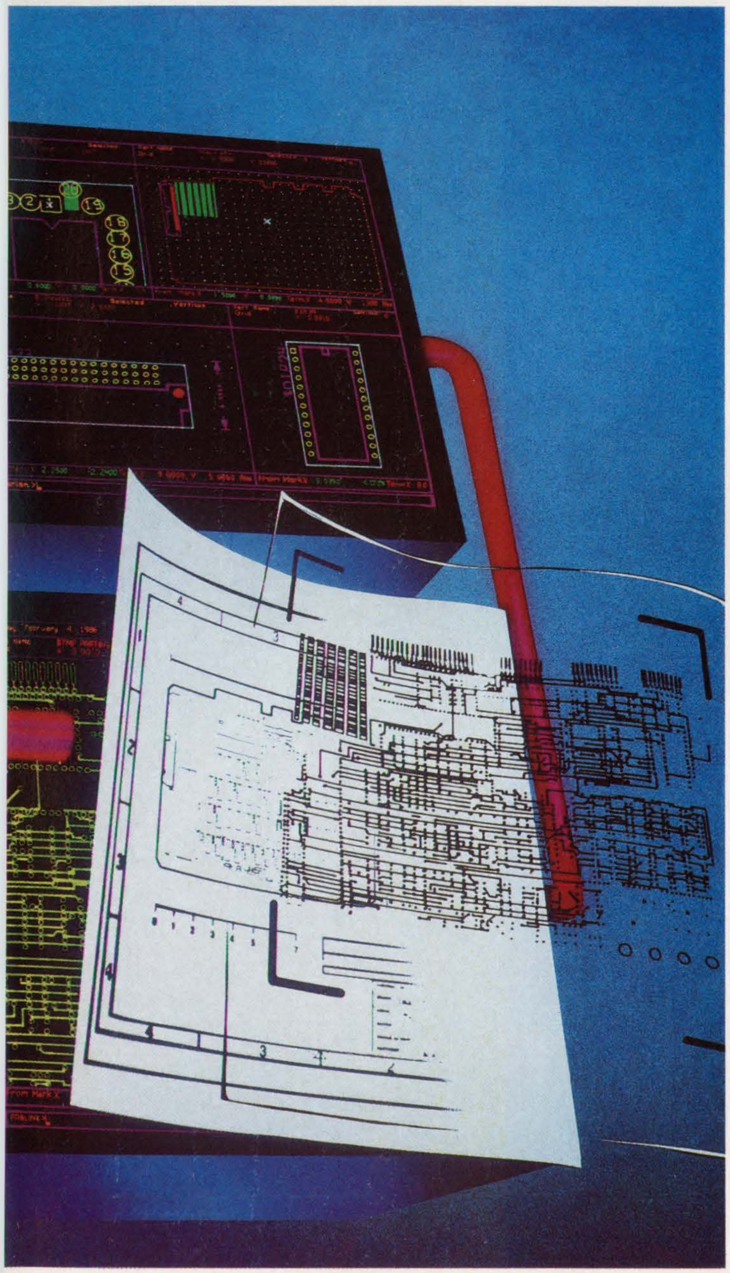
At last, PCB layout resides in a CAE network that also includes hierarchical schematic capture, as well as logic and analog simulation. All linked in an environment that permits fast, simple data sharing for greater productivity.



As for the tools themselves, a very fast and efficient routing system optimizes board usage and minimizes manufacturing overhead. Now you can do both automatic and interactive fine line routing on even the most complex multi-layer boards. A double-sided placement editor presents a complete view of components on either side of the board under design.

And you have the ability to work with almost any type of component package to optimize your design to meet current market requirements.

Also, our PACKAGE tool bridges, at long last, the gap between EE and PCB designers. Any electronic design is automatically translated into proper component packaging.

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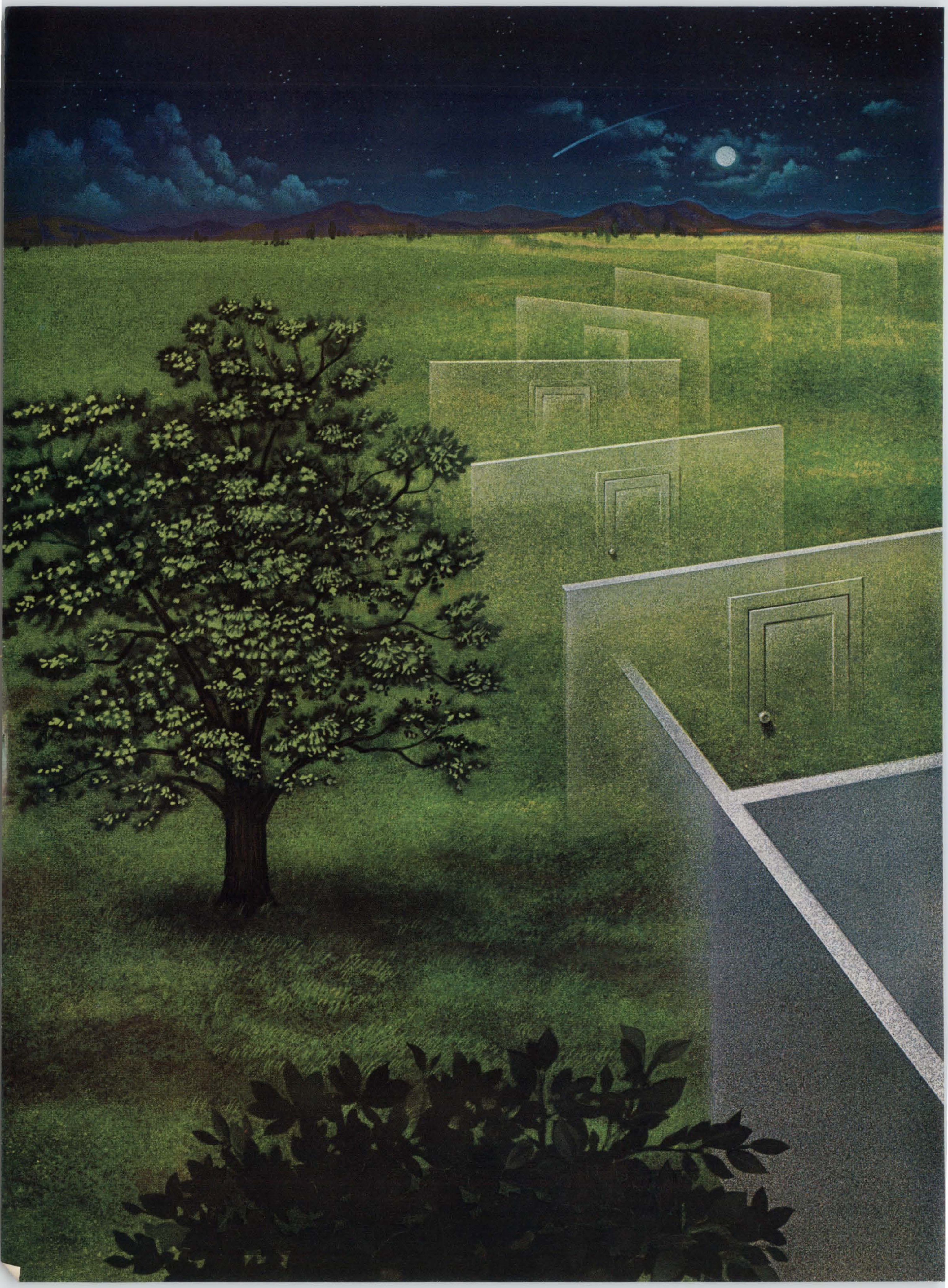

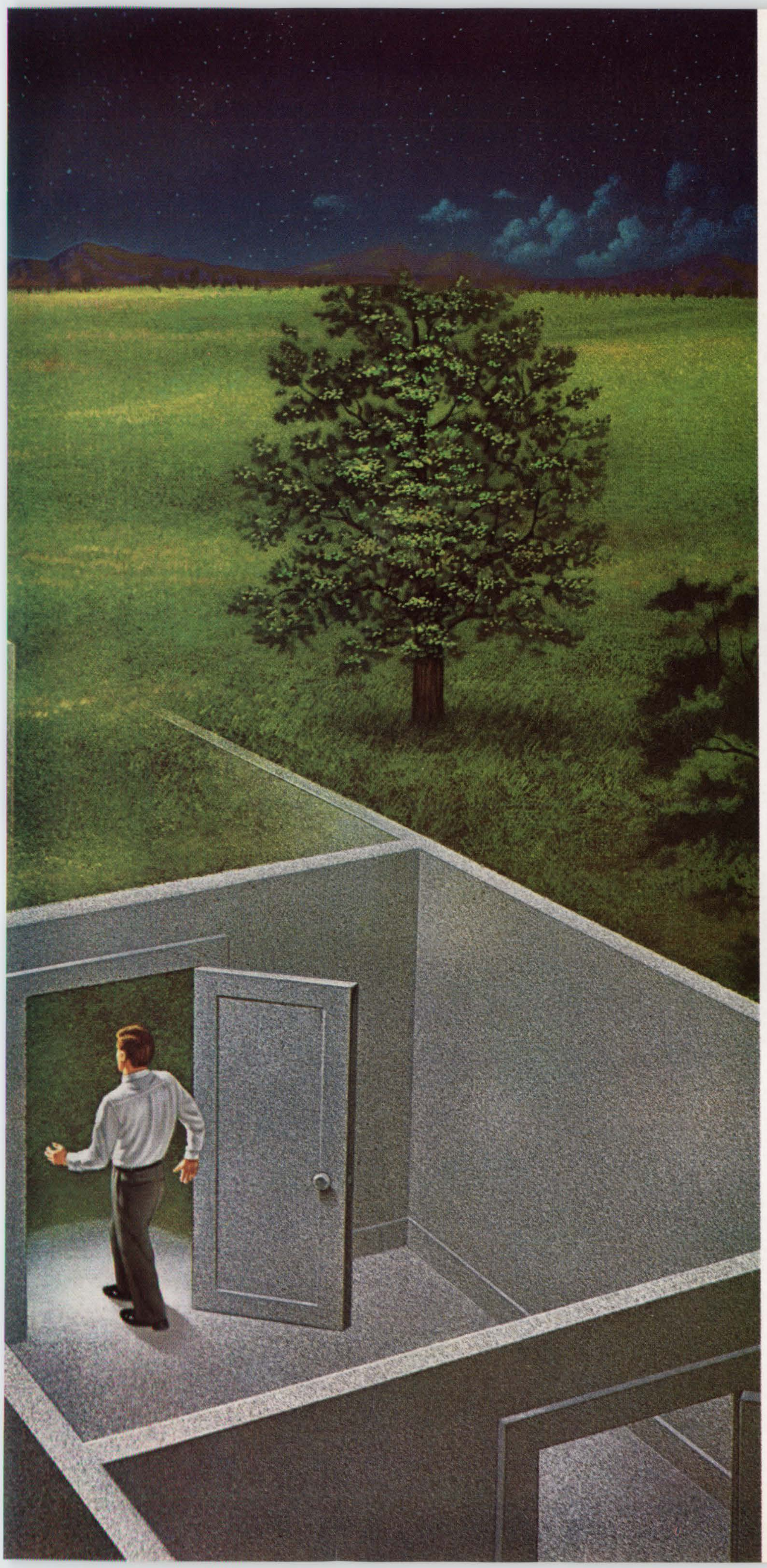

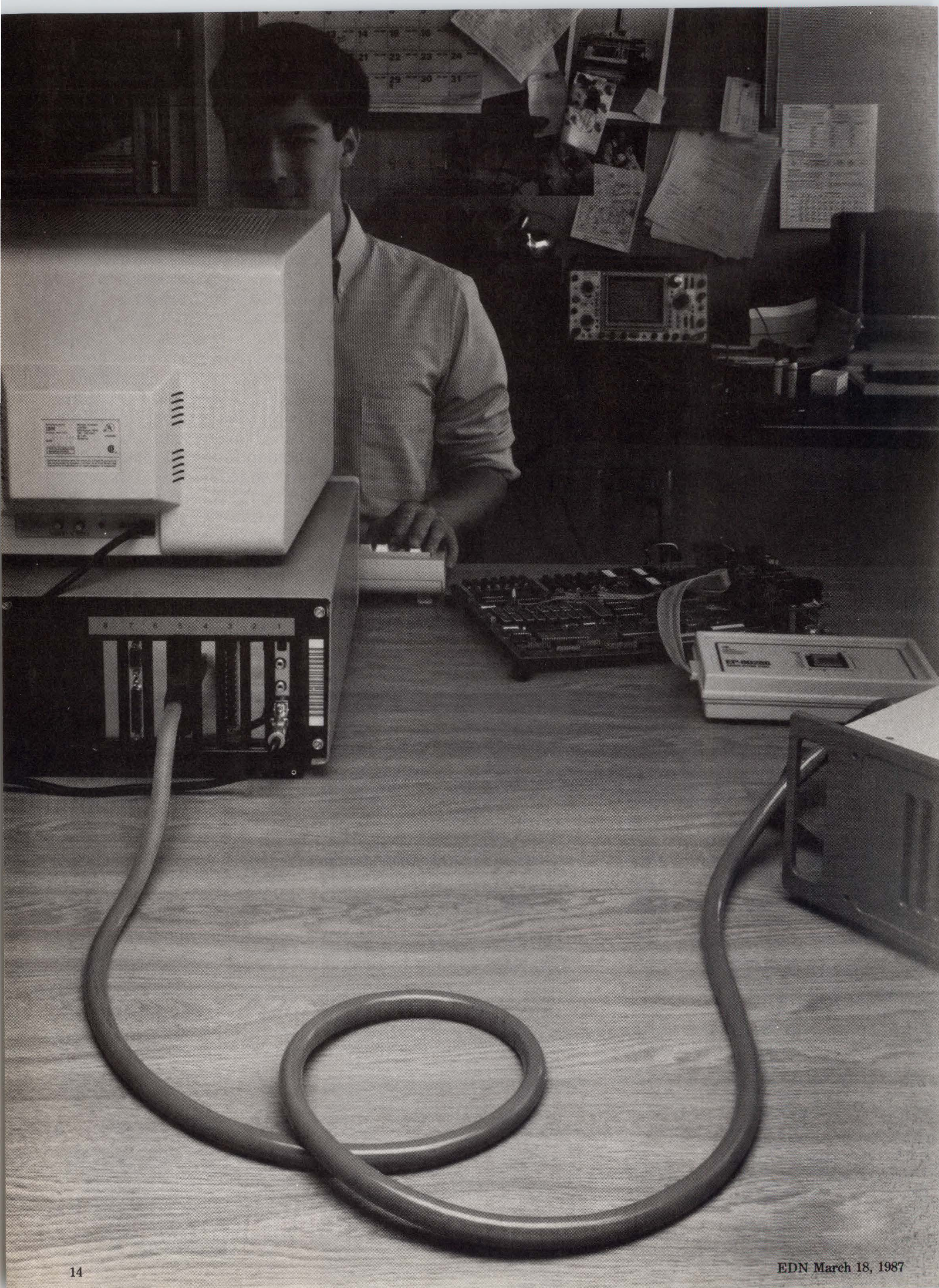

101 ways to hit a moving target.

PAL Family	Generic Part Number	Std MIL Drawing	Replacement JAN Specification Part #
Small 20 Combinatorial	PAL10H8MJ883B	8103501RA	M38510/50301BRXA
	PAL10H8ML883B	81035012C	M38510/50301B2XC
	PAL10H8MF883B	8103501SC	–
	PAL12H6MJ883B	8103502RA	M38510/50302BRXA
	PAL12H6ML883B	81035022C	M38510/50302B2XC
	PAL12H6MF883B	8103502SC	–
	PAL14H4MJ883B	8103503RA	M38510/50303BRX
	PAL14H4ML883B	81035032C	M38510/50303B2X
	PAL14H4MF883B	8103503SC	–
	PAL16H2MJ883B	8103504RA	M38510/50304BRX
	PAL16H2ML883B	81035042C	M38510/50304B2X
	PAL16H2MF883B	8103504SC	–
	PAL16C1MJ883B	8103505RA	M38510/50305BRX
	PAL16C1ML883B	81035052C	M38510/50305B2X
	PAL16C1MF883B	8103505SC	–
	PAL10L8MJ883B	8103506RA	M38510/50306BRX
	PAL10L8ML883B	81035062C	M38510/50306B2X
	PAL10L8MF883B	8103506SC	–
	PAL12L6MJ883B	8103507RA	M38510/50307BRX
	PAL12L6ML883B	81035072C	M38510/50307B2X
	PAL12L6MF883B	8103507SC	–
	PAL14L4MJ883B	8103508RA	M38510/50308BRX
	PAL14L4ML883B	81035082C	M38510/50308B2X
	PAL14L4MF883B	8103508SC	–
	PAL16L2MJ883B	8103509RA	M38510/50309BRX
	PAL16L2ML883B	81035092C	M38510/50309B2X
	PAL16L2MF883B	8103509SC	–
Medium 20A	PAL16L8AMJ883B	8103607RA	M38510/50401BRX
	PAL16L8AML883B	81036072C	M38510/50401B2X
	PAL16L8AMW883B	8103607SA	–
	PAL16R8AMJ883B	8103608RA	M38510/50402BRX
	PAL16R8AML883B	81036082C	M38510/50402B2X
	PAL16R8AMW883B	8103608SA	–
	PAL16R6AMJ883B	8103609RA	M38510/50403BRX
	PAL16R6AML883B	81036092C	M38510/50403B2X
	PAL16R6AMW883B	8103609SA	–
	PAL16R4AMJ883B	8103610RA	M38510/50404BRX
	PAL16R4AML883B	81036102C	M38510/50404B2X
	PAL16R4AMW883B	8103610SA	–
Medium 20A-2 ½ Power	PAL16L8A-2MJ883B	8103611RA	M38510/50407BRX
	PAL16L8A-2ML883B	81036112C	M38510/50407B2X
	PAL16L8A-2MW883B	8103611SA	–
	PAL16R8A-2MJ883B	8103612RA	M38510/50408BRX
	PAL16R8A-2ML883B	81036122C	M38510/50408B2X
	PAL16R8A-2MW883B	8103612SA	–
	PAL16R6A-2MJ883B	8103613RA	M38510/50409BRX
	PAL16R6A-2ML883B	81036132C	M38510/50409B2X
	PAL16R6A-2MW883B	8103613SA	–
	PAL16R4A-2MJ883B	8103614RA	M38510/50410BRX
	PAL16R4A-2ML883B	81036142C	M38510/50410B2X
	PAL16R4A-2MW883B	8103614SA	–

Military Package Designators:

R = 20 lead ¼ x 1 1/16 dual-in-line
S = 20 lead ¼ x ½ Flatpack
2 = 20 Terminal .350 x .350 Leadless Chip Carrier
K = 24 lead 3/8 x 5/8 Flatpack
L = 24 lead ¼ x 1¼ Dual-in-Line
3 = 28 Terminal .450 x .450 Leadless Chip Carrier

MMI Package Designators:

J = Ceramic DIP
F = Bottom Brazed Flatpack
L = Leadless Chip Carrier
W = Cerpak
JS = 24 pin Cerdip

Now that the DOD is rethinking the order of its mil spec standards, which one should you shoot for?

Well, when it comes to military PAL® devices, you can't miss. Simply set your sights on Monolithic Memories.

You see, we have more PAL devices qualified to the highest military standards, JAN38510 and the Standard Military Drawing Program, than anybody else. (See list below.)

Even our newest PAL devices, from high-speed ECL to low-power CMOS, are already slated for Standard Military Drawing release.

So whether the DOD moves its standards or leaves them right where they are, you'll be right on target.

For a copy of our new Military Products Short Form Catalog, call your local Monolithic Memories representative or qualified military distributor.

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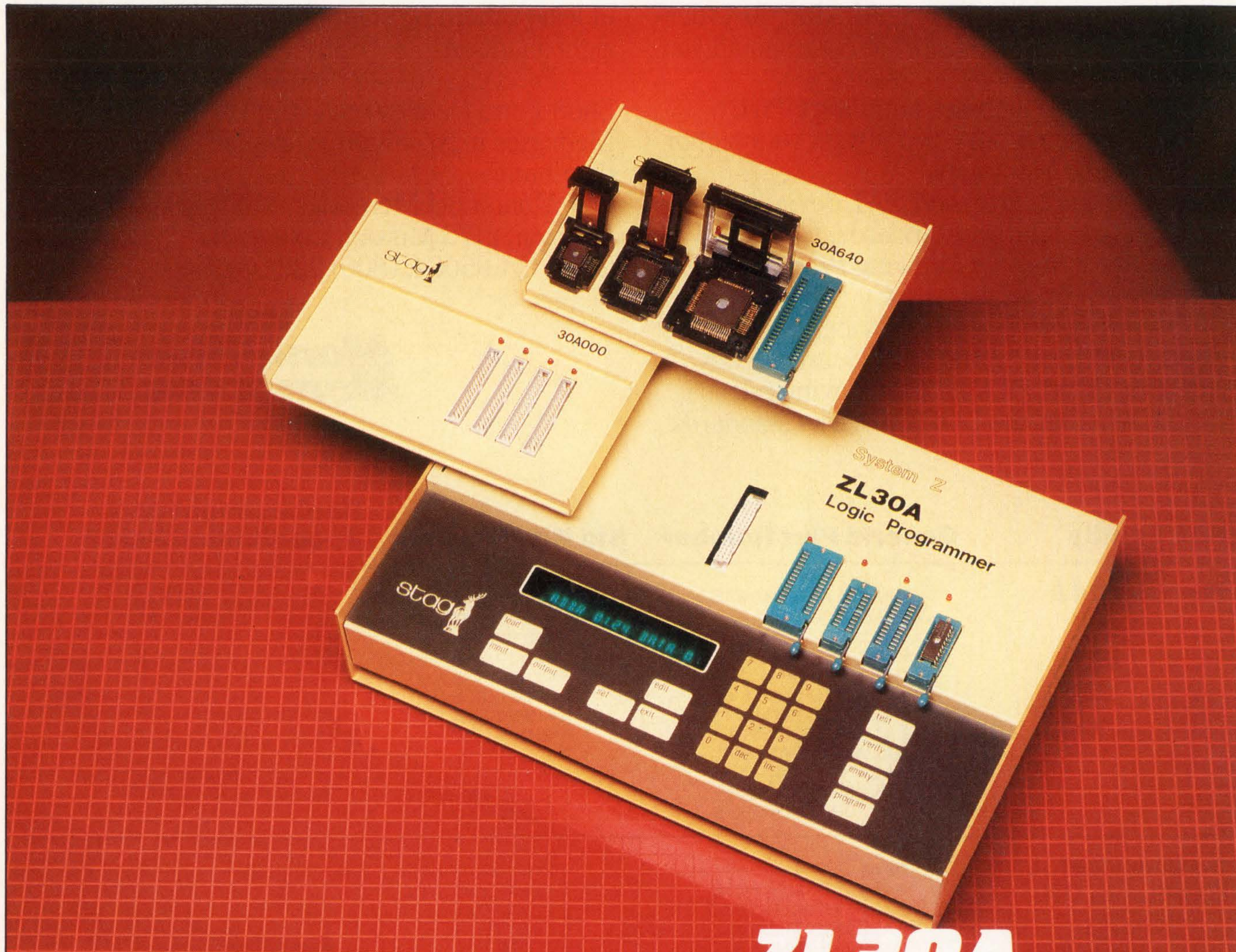
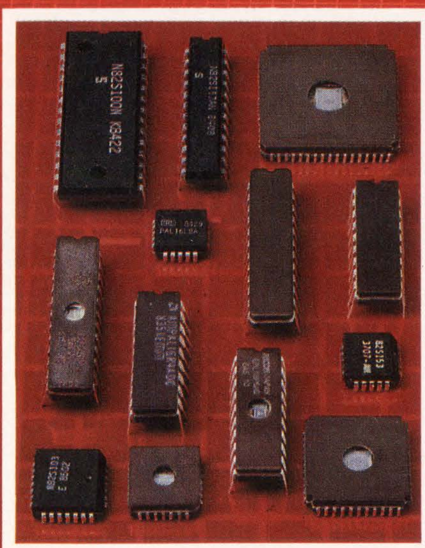
Monolithic Memories MMI

PAL Family	Generic Part Number	Std MIL Drawing	Replacement JAN Specification Part #
Medium 24A	PAL20L8AMJS883B	8412901LA	M38510/50501BJX
	PAL20L8AML883B	84129013C	M38510/50501B3X
	PAL20L8AMW883B	8412901KA	–
	PAL20R8AMJS883B	8412902LA	M38510/50502BJX
	PAL20R8AML883B	84129023C	M38510/50502B3X
	PAL20R8AMW883B	8412902KA	–
	PAL20R6AMJS883B	8412903LA	M38510/50503BJX
	PAL20R6AML883B	84129033C	M38510/50503B3X
	PAL20R6AMW883B	8412903KA	–
	PAL20R4AMJS883B	8412904LA	M38510/50504BJX
	PAL20R4AML883B	84129043C	M38510/50504B3X
	PAL20R4AMW883B	8412904KA	–
Medium 24XA Exclusive OR	PAL20L10AMJS883B	8412905LA	–
	PAL20L10AML883B	84129053C	–
	PAL20X8AMJS883B	8412906LA	–
	PAL20X8AML883B	84129063C	–
	PAL20X10AMJS883B	8412907LA	–
	PAL20X10AML883B	84129073C	–
	PAL20X4AMJ883B	8412908LA	–
	PAL20X4AML883B	84129083C	–
Medium 20A-4 ¼ Power	PAL16L8A-4MJ883B	8506501RA	–
	PAL16L8A-4ML883B	85065012C	–
	PAL16R8A-4MJ883B	8506502RA	–
	PAL16R8A-4ML883B	85065022C	–
	PAL16R6A-4MJ883B	8506503RA	–
	PAL16R6A-4ML883B	85065032C	–
	PAL16R4A-4MJ883B	8506504RA	–
	PAL16R4A-4ML883B	85065042C	–
Medium 20B	PAL16L8BMJ883B	8515501RA	–
	PAL16L8BML883B	85155012C	–
	PAL16R8BMJ883B	8515502RA	–
	PAL16R8BML883B	85155022C	–
	PAL16R6BMJ883B	8515503RA	–
	PAL16R6BML883B	85155032C	–
	PAL16R4BMJ883B	8515504RA	–
	PAL16R4BML883B	85155042C	–
Medium 20B-2 ½ Power	PAL16L8B-2MJ883B	8515505RA	–
	PAL16L8B-2ML883B	85155052C	–
	PAL16R8B-2MJ883B	8515506RA	–
	PAL16R8B-2ML883B	85155062C	–
	PAL16R6B-2MJ883B	8515507RA	–
	PAL16R6B-2ML883B	85155072C	–
	PAL16R4B-2MJ883B	8515508RA	–
	PAL16R4B-2ML883B	8515508SA	–
			–



ZL30A
Power in design
Speed in production



Stag's ZL30A offers total PLD programming support

Stag Microsystem's model ZL30A is the first dedicated Logic Programmer of its kind that not only supports programming of PLDs, EPLDs, and GALs*, in a variety of 20, 24, 28 and 40 pin DIP, but also supports programming of the latest surface mounted PLCC/LCC devices.

Stag's ZL30A contains features that have made it the industry standard in both engineering and production environments. Salient among these are: ● Powerful easy-to-use editing capability ● Super fast programming speed ● Stand alone or remote control operation ● Comprehensive device library ● Handler interface capability to support DIP or PLCC/LCC devices ● I/O formats include JEDEC, Signetics and X-Plot ● Compatible with CUPL* software compiler ● RS232C, IEEE-488 and handler control interface ports standard ● Expansion modules accommodate 40 pin DIP and a range of surface mounted devices ● Stringent in-program checks including continuity and connect tests are automatically performed to guarantee error free stand alone or handler operation ● Supports Test Vectors ● Turn-Key handler interface kits ● Worldwide sales and service support.

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CIRCLE NO 162

NEWS BREAKS

EDITED BY JOAN MORROW

SINGLE-CHIP DISK CONTROLLER SUPPORTS ESDI

The Am9590 from Advanced Micro Devices (Sunnyvale, CA, (408) 732-2400) is a single-chip hard-disk controller that supports the emerging Enhanced Small Disk Interface (ESDI) at data rates to 15 MHz. The device can control any combination of as many as four hard- or floppy-disk drives. The characteristics of each drive are independently user programmable. Two on-chip sector buffers, each with 512 bytes max, support zero-sector interleaving to increase system throughput. The Am9590 is packaged in a 68-pin leadless chip carrier and costs $69.95 (100).—David Shear

SOFTWARE TOOLS LET MACINTOSH CONTROL IBM PC I/O BOARDS

Now you can use your Macintosh Plus computer and MacBus expansion unit to control Analog Devices' RTI-800 Series analog and digital I/O expansion cards. The MacBus/RTI-800 Series software from National Instruments (Austin, TX, (512) 250-9119) lets you program RTI-800 cards using Microsoft Basic, Magamax C, or LabView. If you use C or Basic, the local MacBus μP interprets command strings to perform data-acquisition and -control I/O functions. Using LabView—National Instruments' graphical programming language for automatic test and measurement—the RTI-800 boards appear to be electronically wired into a LabView block diagram, and LabView performs all communication tasks. For $195, you get the software and application examples written in C and LabView.—J D Mosley

DIGITAL WORD GENERATOR OPERATES TO 250 MHz OVER 32 CHANNELS

Look for Interface Technology (Glendora, CA) to introduce a 128-channel, 62.5-MHz digital word generator next month. You can operate the generator in a 32-channel mode at data rates to 250 MHz. You can program output edges with 50-psec resolution and output amplitudes with 10-mV resolution.—Chris Everett

OPTICAL SCANNER AND LASER PRINTER SUIT DESKTOP PUBLISHING

Two new products from Hewlett-Packard Co (Palo Alto, CA) underscore the company's continued interest in desktop publishing. The $1495 ScanJet optical scanner features user-selectable 38- to 300-dots/in. resolution and three scanning modes: binary, dithered, and gray scale. You use binary image scanning on line art and text, dithered scanning (similar to half-tone representation) on photographs, and gray-scale scanning for high-quality photographic reproduction. The scanner recognizes 16 gray shades. A $495 interface-card and software package links ScanJet to IBM PC and compatibles. The $2495 LaserJet Series II laser printer includes all of the features of the company's earlier $3995 LaserJet Plus model, plus a few more. Based on the Canon LBP-SX print engine, the laser printer incorporates a new paper path that emits copies face down, enabling the printer to deliver multiple-page documents in the correct order. The base printer includes 512k bytes of memory. A $495 1M-byte expansion board allows the printer to create full-page, 300-dots/in. graphics.—Steven H Leibson

NEW 32-BIT CPU CHIP OFFERS RISC-LIKE ARCHITECTURE

By late 1987 or early '88, Advanced Micro Devices Inc (Sunnyvale, CA) hopes to be in the 32-bit μP market with its Am29000 CMOS CPU chip. The streamlined-instruction processor (SIP) will provide a set of simple instructions that take advantage of the chip's RISC-like architecture. AMD plans to offer chips that operate at 25 MHz, which would sustain a rate of 17 MIPS. The chip will contain 192 general-purpose registers, a 64-entry memory-management unit, and a 512-byte cache.—Jon Titus

NEWS BREAKS

65×100-mm FACSIMILE MODEM BOARD RUNS AT 14,400 BPS

The $255 HF144 facsimile modem from Emulex (Costa Mesa, CA, (714) 662-5600) is 50% faster than previous fax modems, yet fits in the same 65×100-mm form factor. It operates at 14,400, 12,000, 9600, 7200, 4800, 2400, and 300 bps, and it uses trellis-coded modulation at 14,400 and 12,000 bps in accordance with CCITT V.33. At 9600 bps, you can choose between V.29 and TC96 modes. V.29 does not specify trellis coding; TC96 implements it in accordance with V.32. Trellis-coded modulation results in improved signal quality and refers to the visual form the data takes in an eye-pattern display.—Margery S Conner

EVALUATION MODULE LETS YOU TEST M68HC05 PROTOTYPE DESIGNS

The $500 M68HC05 Evaluation Module from Motorola (Austin, TX, (512) 440-2035) is a board that emulates all of the essential timing and I/O circuitry of MC68HC05C4/C8 μCs. It allows you to design, debug, and evaluate hardware and software designs for use with those μCs and with future members of the M68HC05 family. Communicating via an RS-232C port, the module is compatible with IBM PCs, VAXs, PDP-11s, and any Motorola development system. The module includes jumper-selectable options such as IRQ sensitivity and clock input selection. An EEPROM μC programmer enables you to check, erase, program, verify, and copy the contents of DIP or PLCC μCs.—J D Mosley

CERTIFIED BEHAVIORAL MODELS SIMULATE 74AS8800 ICs PRECISELY

Texas Instruments (Dallas, TX) has certified Quadtree's (Bridgewater, NJ) behavioral models of the TI SN74AS8800 chip set. To certify the behavioral models, Texas Instruments verified that the models implement all functional and timing characteristics of the physical ICs.

The SN74AS8800 chip set consists of nine support chips for TI's 32-bit μP. You can use these models to design and debug, in software, a μP-based system or a single-board computer. The chip set includes such devices as a 32-bit multiplier/accumulator, a floating-point processor, and 32-bit shifters. The behavioral models cost $500 to $1500; a set of all nine models costs $7200.—Eva Freeman

DATA-ACQUISITION BOARD SPEEDS WAVEFORM DATA STORAGE

Functioning as either a stand-alone system or as an enhancement to the manufacturer's Soft500 data-acquisition and -control program, the Real Time Monitor and Direct Storage System (RTMDS) from Keithley Instruments (Cleveland, OH, (216) 248-0400) continuously sends data to your PC's floppy or hard disk at speeds as fast as 5000 samples/sec, while maintaining a real-time waveform display on your PC's monitor. By performing the plotting functions in hardware, the $1200 RTMDS frees your PC for other tasks. When used in conjunction with Soft500, the program runs as much as 10 times faster. The RTMDS provides as many as 16 channels of direct data storage, simultaneous display of as many as eight channels, smooth scrolling, and a triggered sweep-display mode. —J D Mosley

INDUSTRY-STANDARD FIFO MEMORY COMES IN LOW-POWER VERSION

A low-power FIFO memory that is pin-for-pin compatible with the IDT7201 and the MK4501 is available from Mosel (Sunnyvale, CA, (408) 733-4556). The MS7201 is a 512×9-bit FIFO memory that consumes 10 μA during data retention and 40 mA maximum while operating. The MS7201 comes in 50- to 120-nsec versions in 28-pin plastic DIPs for $13 to $26 (100).—David Shear

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Why fill your digital delay design with unnecessary components, when you can have all the capability you need in one small, low-cost IC?

TRW LSI Products Division, the industry leader in high performance digital signal processing products, gives designers an edge with the TDC1011. The TDC1011 is a high-speed, 8-bit wide shift register, programmable to any length between 3 and 18 stages. It operates at an 18MHz shift rate (56ns worst case), is TTL compatible, and dissipates a low 750mW.† The TDC1011 operates from a single +5V power supply and is available in a 24-lead DIP.

The beauty of the TDC1011 is that this single chip performs the same functions that would require as many as 18 alternative chips — instead of 18 shift registers, you can use just one in a variety of digital delay applications. This translates into lower component costs, less board space and reduced power dissipation. Built with TRW's OMICRON-B™ one-micron bipolar process, the TDC1011 provides the system designer with a unique variable delay capability at video speed.

You can use the TDC1011 for telecom, sonar, radar, CAT scanners, computer graphics, TV special effects, and a host of other digital delay applications. And, as with all of our products, the TDC1011 is backed by our extensive network of in-house and field applications engineers, application notes and our full line VLSI DATA BOOK.

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NEWS BREAKS: INTERNATIONAL

CPU CARD, SOFTWARE INTEGRATE REAL-TIME PROCESSING AND UNIX

Featuring a 68010 μP, math coprocessor, memory-management unit, SCSI bus interface, four RS-232C serial ports, and 2M or 4M bytes of RAM, the TSVME106 VME Bus CPU card from Thomson Semiconducteurs (Velizy, France, TLX 204780) provides a complete operating environment for Unix System V. Because Unix tasks don't need to access memory via the VME Bus, the bus is free for other CPUs to run real-time application programs. To link real-time programs running under pSOS-68K into Unix supervisory programs, the company's TSVME791 software, priced at Fr fr 12,000, provides a Unix-to-pSOS link. Communicating via shared memory on the VME Bus, this link allows you to route the output of Unix tasks to the input of pSOS tasks and vice versa. Depending on memory prices during the second quarter, the TSVME106 will cost approximately Fr fr 35,000.—Peter Harold

SILICON COMPILER USES TI/PHILIPS/ES2 AND MIETEC CELL LIBRARIES

Running on VAX-VMS computers, the ASA silicon compiler from Sagantec bv (Eindhoven, The Netherlands, TLX 59163) allows you to minimize the chip area required to implement digital ASIC designs. The compiler's front-end processing includes schematic capture and high-level simulation software; the layout generator handles standard-cell libraries from Texas Instruments, Philips, ES2, and Mietec. Databases of foundry-dependent parameters allow you to design to the requirements of Texas Instruments' and Mietec's bulk CMOS processes. The software license for the compiler costs $50,000 and $80,000. A version running under Unix is under development.—Peter Harold

LOW-COST WORKSTATION OFFERS 2.5- TO 4-MIPS PROCESSING POWER

Housed in a PC-style desktop package, the Vitesse graphics workstation from Cambridge Micro Computers Ltd (Cambridge, UK, TLX 817923) provides vector-drawing and area-fill speeds on its 1024×768-pixel resolution color monitor as high as 2.5 and 1 μsec/pixel, respectively. The workstation displays as many as 16 colors from a palette of 4096 colors. The hardware is based around a VME Bus system and runs a 16-, 20-, or 25-MHz 68020 μP and 68881 math coprocessor. It incorporates floppy- and Winchester-disk drives and includes five RS-232C interfaces and an Ethernet interface. The workstation, which starts at £9950, is supplied with a single-user Unix license. Two- and 3-dimensional graphics software packages are also available.—Peter Harold

IMAGE-ANALYSIS SYSTEM IS BASED ON IBM PC

The μMagiscan image-analysis system from Joyce-Loebl (Gateshead, UK, TLX 53257; in the US, (516) 222-0941) is built around an IBM PC with a color-graphics adapter board, a 10M-byte hard-disk drive, an Intel 8087 math coprocessor, a TI 320 coprocessor, and a video I/O pc-board frame grabber to provide 256×256×8-bit images. In addition to the IBM PC monitor, the system also has a separate color monitor for displaying the image-analysis operations. The custom-designed software is divided into three programs: Test, which gives you a quick method to check the system; Menu, which lets you perform all the basic image-analysis routines; and Results, which provides a rapid overview of the measurements. The system costs $25,000.—Joan Morrow

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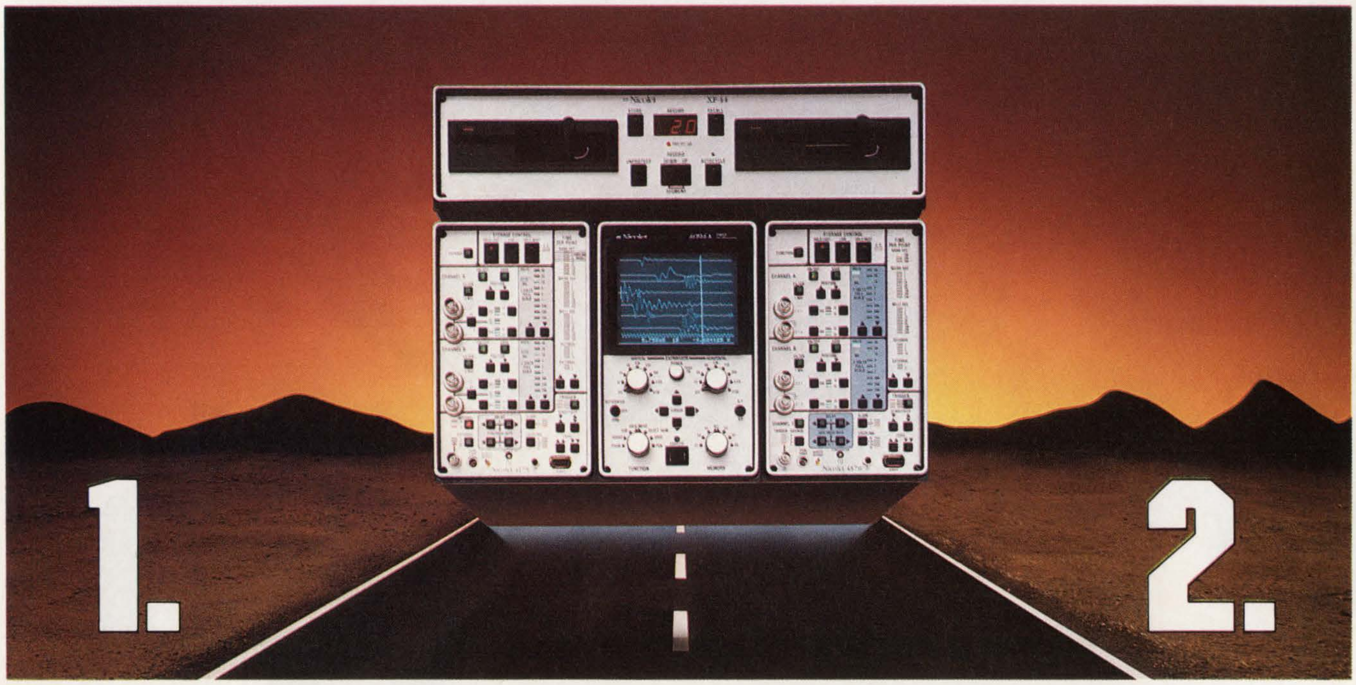
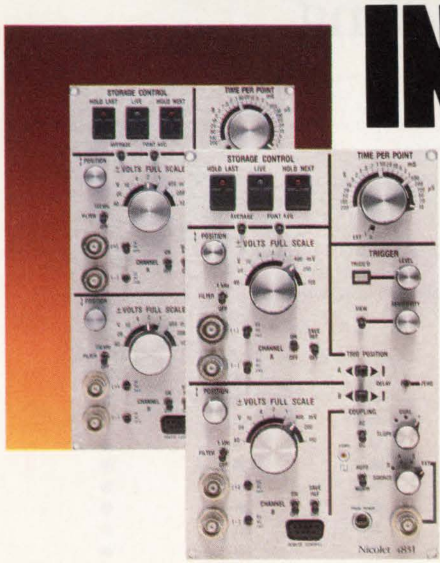


TWO DIGITAL SCOPES IN ONE.



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Expand and examine any waveform feature in detail. Use the dual cursors and numerics to measure the time or voltage of any point. Compare live or stored waveforms with each other or with pre-recorded references. Store signals on disk manually or automatically. Use pushbutton programs to manipulate the data or send it to your computer via GPIB or RS232 interface. Complete your report with a hardcopy plot using the XY/YT recorder or digital plotter outputs.

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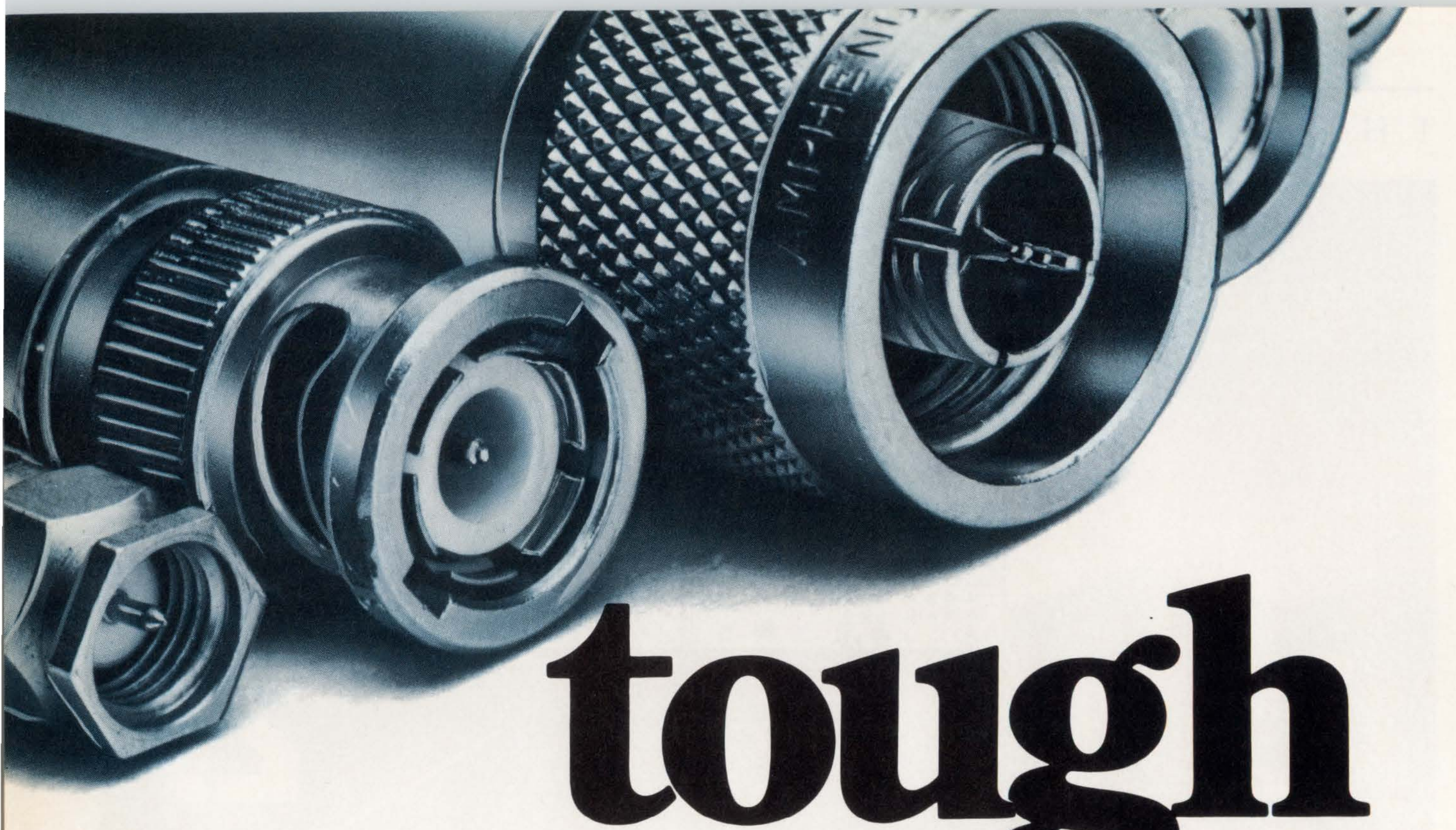

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		DC–1000	1000–1500	DC–1000 MHz	1000–1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

*DC–1000 MHz (all 75 ohm or 30 dB models) DC-500 MHz (all 40 dB models)

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■ denotes 75 ohms; add –75 to model no.
● denotes 50 ohms

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1	●	●	●	●
2	●	●	●	●
3	●	●■	●	●
4	●	●	●	●
5	●	●	●	●
6	●	●■	●	●
7	●	●	●	●
8	●	●	●	●
9	●	●	●	●
10	●	●■	●	●
12	●	●	●	●
15	●	●■	●	●
20	●	●■	●	●
30	●	●	●	●
40	●	●	●	●

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Max. 20dB Stop Frequency (MHz)	19	70	90	147	210	290	410	580	750	840	1000	1100	1340

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HIGH PASS Model *HP–		50	100	150	200	300	400	500	600	700	800	900	1000
Pass Band (MHz)	start, max.	41	90	133	185	290	395	500	600	700	780	910	1000
	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	190	290	365	460	520	570	660	720

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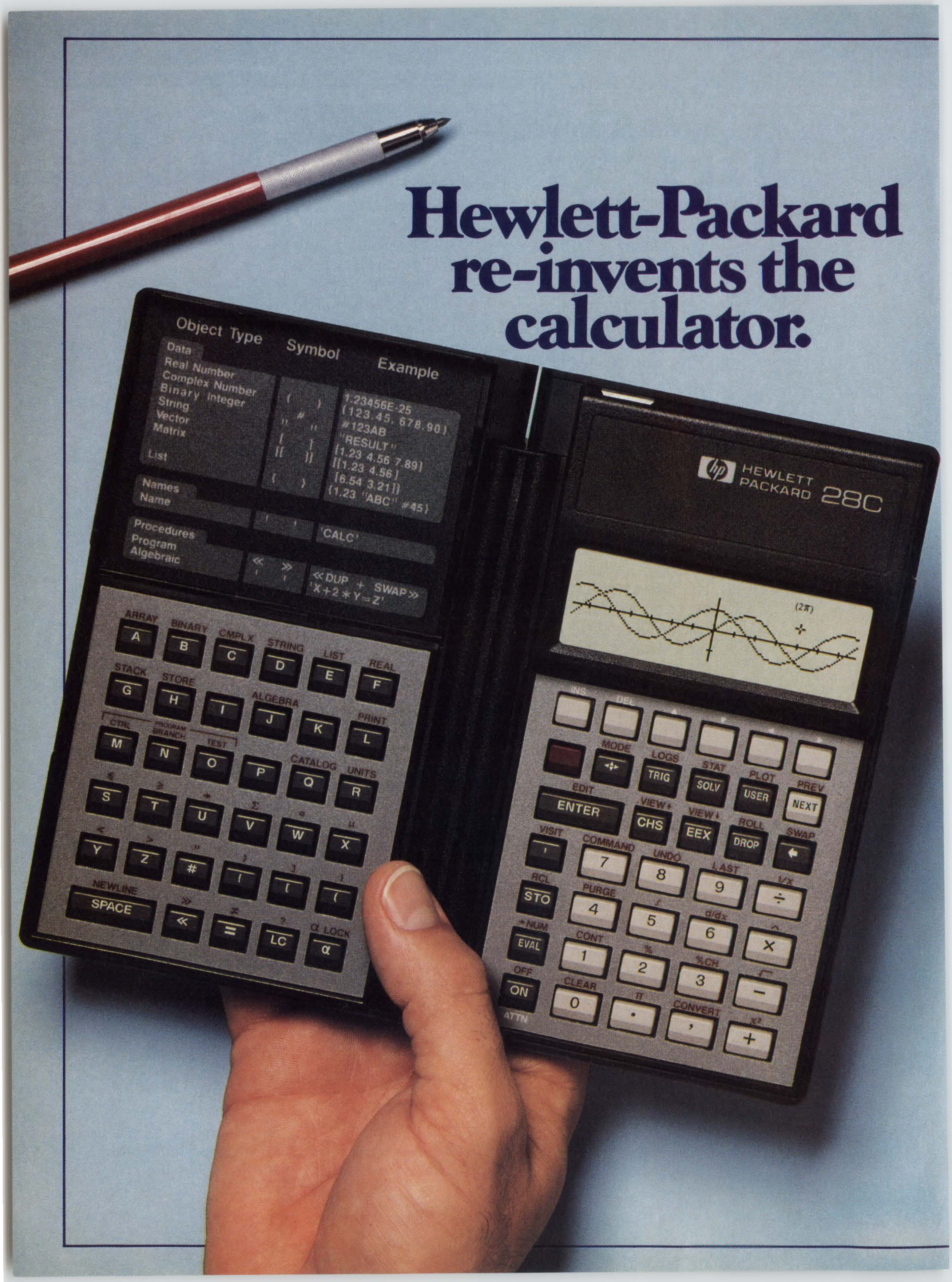
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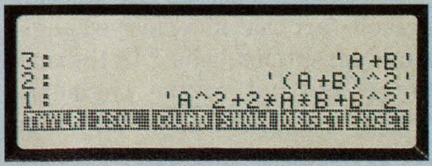

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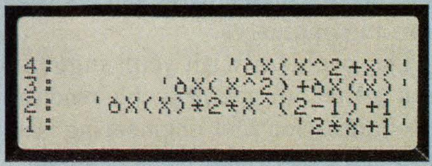

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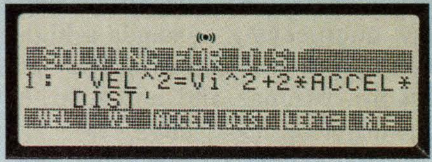

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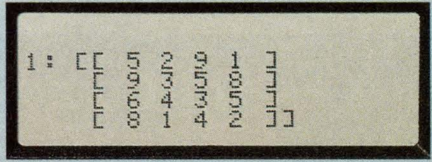

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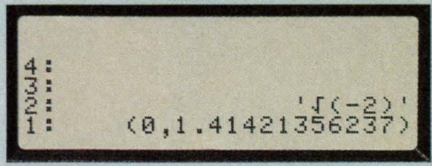

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00028-40001
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D-00028-40001-1

Career speakers ignore engineering's drawbacks

Dear Editor:

In your editorial "Youngsters deserve a look at engineering" (EDN, December 11, 1986, pg 51), you suggest that it is time to inform young people about careers in engineering so that they can be persuaded to enter the field. You suggest the time-honored approaches, whereby gullible high-school students are exposed to industry trade shows and to speakers from various local companies that employ engineers.

Without a doubt, the speakers supplied to the schools' Career Days are those that espouse the management viewpoint of the companies that furnish them. No mention will be made of the massive, ongoing layoffs. Nobody will point out that, according to the College Placement Council, the EEs in the class of 1986 received 36.5% *fewer* job offers than did those in the class of 1985. Nobody will breathe a word of the fact that this nation is in the midst of a worsening high-tech depression. Nobody will bring up the uncomfortable fact that an employed engineer's inventions belong to the employer and not to the engineer. Nobody will speak of the fact that the professional engineering societies represent the professors and the corporate executives and not the working engineers.

The problem with your suggestion is that our young people receive the impression that engineering is a fulfilling career and not a dead-end one, that engineering is a stable career and not an uncertain one, and that engineering demands a high level of technical skill on the part of the practitioner and not a large amount of clerical skill.

By all means, let us give our youngsters a look at engineering careers, but let's make certain that this look is an accurate one.

Incidentally, Mrs Feerst and I are both degreed engineers who have persuaded our two sons, under penalty of shattered kneecaps, to enter other careers.

Sincerely yours,
Irwin Feerst
Committee of Concerned EEs
Massapequa Park, NY

Engineers are considered a consumable resource

Dear Editor:

The December 11, 1986, issue of EDN presents an interesting dichotomy. On page 51, you extol the virtues and rewards of an engineering career, while on page 306 (in the Professional Issues section) we read how the father of the CEO of a small company in the South Bronx "was one of the thousands of engineers

Text continued on pg 34

TEK'S NEW EASY-TO-EXPERT LOGIC ANALYZER $3995.*

Introducing the Tek 1220 and 1225: the two newest members of the Tek 1200 Series of logic analyzers. Nothing else in their price range delivers so much and makes it all so easy to use. Consider:

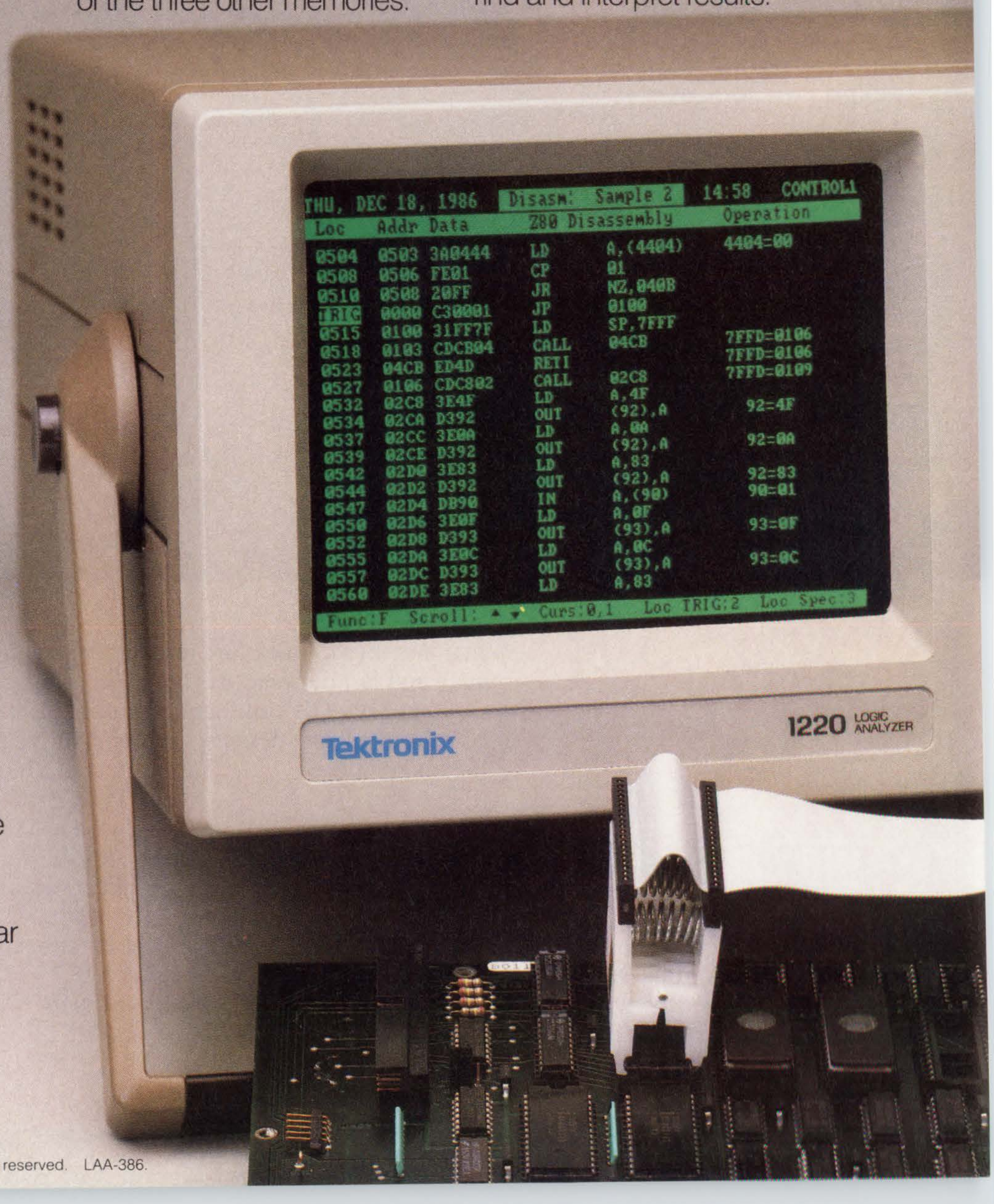
1 Powerful state, timing and disassembly analysis. The 1220 and 1225 provide 32 or 48 data channels, respectively, in groups of 16-channels, with channel groups clocked independently or linked together — so you can sample

data from as many as three circuit sections at once.

Tek currently provides support for the most popular microprocessors, with additional 8- and 16-bit personality modules to be introduced continually.

2 A total of four 2K nonvolatile memories support each channel. Acquire data in one memory and compare it to data in any of the three other memories.

Clock/calendar plus storage for up to eight test setups are also in battery-backed memory. Date and time of storage are included with each data memory, so it's easy to find and interpret results.



who lost their jobs during the 1960s."

During my 30 years as an engineer, I have seen layoffs, threats of layoffs, salaries that have lagged well behind the cost-of-living index, uncompensated overtime, and the feeling that engineers are considered by the management of most companies to be a consumable resource.

If high-school students were truly given the "realistic exposure to engineering and its rewards" that you call for in your editorial, far fewer high-school students would go on to pursue careers in engineering.

Sincerely yours,
Allan Koszyn
Yonkers, NY

"WE'VE TRIED, BUT IT STILL WON'T DO WINDOWS."

Few engineers reap the career's rewards

Dear Editor:

Yes, it is time to tell more young people about engineering careers. By failing to teach more students about engineering, we might lure more innocent minds into the career of engineering, whose college curriculum is one of the toughest and whose rewards are among the highest.

A small fraction of engineering students make it up through the ranks, some because they are exceptional, some because they know someone. The majority do not make it and are forever being pushed around (if they're lucky). Most of us are simply discarded.

We in our 50s buy our own computers, study to keep abreast, and develop much of our work at home. So what kind of reward do we get? Some young engineer becomes our supervisor; he or she decides we are surplus, and we land in the street.

Thousands of engineers are in that position. Because the Social Security retirement program is slowly going bankrupt, it's inevitable that the retirement age will be increased to 70. What is going to happen to the discarded engineer over 50? Will he or she have to tolerate this degrading treatment that much longer?

My advice to young people is this: Yes, engineering education is superior to most other kinds. If you must

Text continued on pg 38

YOU'VE READ A LOT LATELY ABOUT DSP.

NOW HERE'S THE LAST WORD.

With all the talk about digital signal processing these days, it's hard to know what to believe. At Zoran, we'd like to make it easy for you.

For us, DSP isn't just a sideline, as it is at other companies. It's the bottom line. Because it's all we do.

Which means we strive to achieve only one objective. Developing the high-performance DSP products you need for faster, easier system design.

As evidenced by the Zoran Vector Signal Processor (VSP)™ and Digital Filter Processor (DFP).

Two new signal processors that enable you to do something you've never done before. Like design your system from the top down.

With a systems perspective in mind, which enables you to focus on your application, instead of on your implementation.

Using single, highly integrated system-processor devices that use parallel processing to deliver all the speed of building blocks. Without all the hassles of discrete components and extensive programming.

What's more, you'll design your system in a lot less time. At a lower cost. And with greater ease and flexibility than you ever thought possible.

Best of all, we're shipping products now. Instead of simply announcing them. Which means you don't have to wait to get the jump on your competition.

High performance never looked so easy. We didn't think it was enough for the VSP and the DFP to be the fastest DSP devices. So we also made them the easiest to use.

We developed proprietary architectures and optimized them for faster, more efficient execution of embedded DSP algorithms, such as FFTs and FIRs.

And we slashed programming time with a high-level instruction set that shrinks hundreds of lines of code to a mere handful, speeding system design.

On top of that, we developed a modular design that lets you configure multiple VSPs and DFPs in parallel to achieve even higher performance.

And we utilized proven double-layer metal CMOS technology for lower power consumption and higher reliability.

VSP: Powerful vector processing capability. Until now, you needed the power of an array processor if you wanted to do vector processing. But that was before Zoran developed the Vector Signal Processor.

```
LD   MMPT:128    MBA:IN_DATA          ; LOAD 128 POINTS
FFT  MMBT:128    FPS:64    LPS:1      ; DO 128-PT FFT
ST   MMPT:128    MBA:OUT_DATA         ; STORE 128 POINTS
```

Three simple VSP instructions execute a 128-point complex FFT in 237 microseconds.

The world's most powerful DSP processor. And the first to process data in blocks, or vectors, instead of processing only one input at a time, as is the case with scalar processors.

Which means you can easily achieve bit-slice performance with a single component. And you can do it in a lot less time.

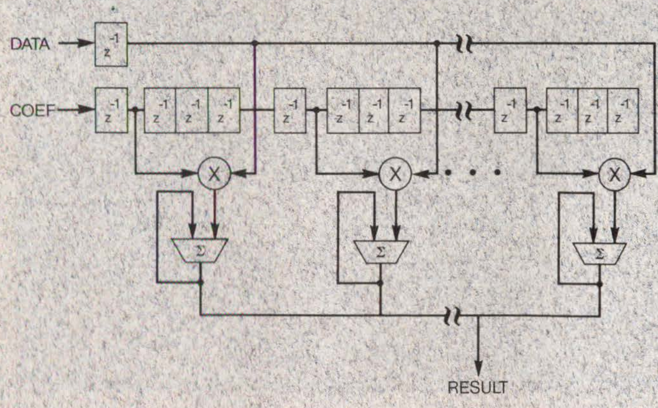
Because our embedded high-level instruction set eliminates the need to write lines and lines of code.

So you can concentrate on your end application, instead of getting bogged down in the details of software implementation.

And with our unique VSP architecture, multiple tasks, such as managing the bus interface and executing algorithms, are handled concurrently for even faster operation.

A 1024-point complex FFT, for example, takes just 2.6 ms with the VSP. Using only a kernel of three simple instructions.

The VSP also provides better dynamic range, thanks to the use of 16-bit block floating point arithmetic. Which retains the precision of the original signal during FFT operations.



DFP architecture utilizes parallel processing to deliver 320 million operations per second.

DFP: Faster FIR filtering with parallel processing. Designed for extremely high-speed FIR filtering and 2D real-time convolutions, the DFP family delivers the high performance of building blocks. But with the high integration of a single device.

Each DFP consists of four or eight filter cells configured as a unique parallel-processing system. Each cell contains an 8 x 8 or 9 x 9 bit multiplier, a 26-bit accumulator and three decimation registers.

And with each cell computing 20 million additions and 20 million multiplications per second, the DFP is capable of performing 320 million operations per second. At a blazing 20MHz throughput. So you can easily convolve images in real time.

Moreover, you can cascade multiple DFPs for higher-order filters, or implement them in parallel for even greater precision.

All the tools and support you'll ever need. Most DSP support doesn't give you much to lean on. So we decided to provide you with all the help you need to shorten your development cycle and get to market faster, ahead of the competition.

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All of which explains why the Digital Filter Processor and Vector Signal Processor are currently in use in such computation-intensive applications as image processing, instrumentation and high-speed communications.

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be an engineer, get at least three promotions in the first 10 years. If you don't, get out and use your superior training in another field; otherwise, you'll be in hell the rest of your life. The younger you are when you get your degree, be it bachelor's, master's, or doctorate, the higher the probability that you'll acquire pecking-order points.

Sincerely yours,
Miguel Melgar, PE
Sweetwater, FL

(Ed Note: We doubt that giving kids a chance to go to Electro or Wescon will flood engineering schools with new applicants. However, there is a good chance we will get applicants who really want to be engineers. Every profession has its good and bad points, and youngsters should know about them before they choose career paths. Kids aren't stupid. They'll hear from upperclassmen, friends, and relatives about the decline in engineering jobs, and we'll see a proportionate decline in engineering school enrollment. But if engineering is such a rotten profession, why are so many people still in it?)

Errata

An editing error crept into a February 5 news break (pg 19), which drastically affected the frequency range of the FS-30, a digitally programmable CMOS frequency synthesizer from Analytic Instruments (Dallas TX). The $195 device offers a 20-*mHz*- to 31-MHz range, not the 20- to 31-MHz range as printed.

Please note the following corrections to the November 13, 1986, issue of EDN. In the article "Use of check list prevents problems in TTL systems" (pg 253), item 25 cites an incorrect number (9052) for a monostable device. The correct number is 9602.

Further, a paragraph in the New Products section (pg 329) erroneously states that the SHM-91 dual S/H amplifier from Datel features an acquisition time of 2 msec. In fact, the device's acquisition time is 2 μsec.

Finally, the phone number given on pg 347 for Sprague Electric Co is incorrect. The correct number is (603) 224-2755.

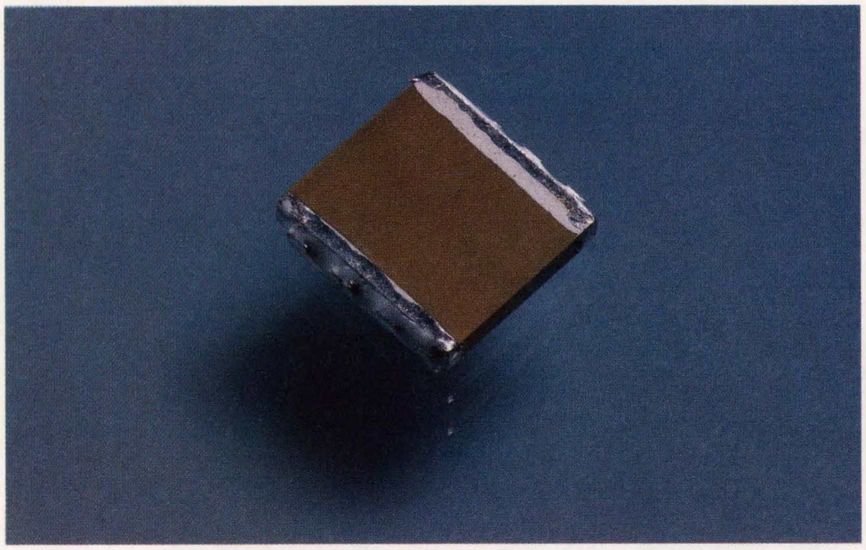
YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

Decoupling V

AVX TechFile Series

TECHNICAL INFORMATION FROM THE LEADER IN MLCs



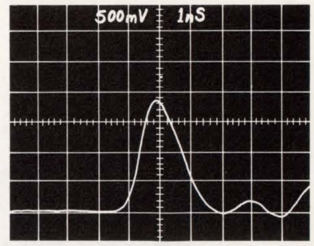


Figure 2. 5.6µF Tantalum

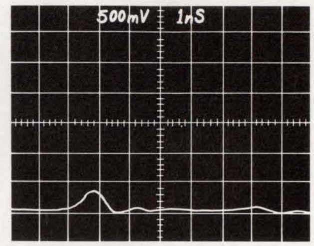


Figure 3. 7.5µF Ceramic MLC

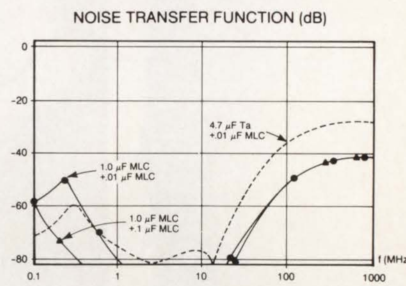


Figure 4. Noise transfer function from switched gates to power entry point (Ferrite bead used on power feed line in all cases)

Power-Entry Decoupling

Replacing Electrolytics in Surface Mount Applications

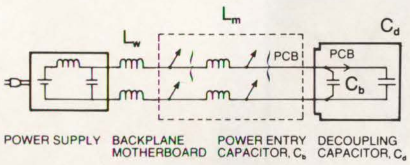


Figure 1. Power supply to printed circuit board (PCB)

In a typical power distribution system (Figure 1), the power-entry capacitor C_b is a relatively large-valued capacitor near the power-entry point on the PCB.

These board level decoupling applications or power-entry capacitors have been dominated by aluminum and tantalum electrolytic capacitors, but the push to surface mount configurations presents major problems in the use of these electrolytic capacitors.

Now, high value, small physical size MLCs offer an excellent alternative to electrolytics. MLCs are compatible with surface mount processing. This allows the designer to take advantage of the lower ESRs and ESLs of MLCs to prevent transmission of PCB-generated noise to the backplane/motherboard and power supply.

Test Results

Figures 2 and 3 compare the response of a tantalum capacitor with an MLC to a leading edge of 200 mA/nS. The tantalum shows an inductive voltage of 2.0V versus the MLC's 0.4V.

This reduction in the ESL of the power entry capacitors through the use of MLCs relative to the conventional approach of using tantalums results in greater than 15 dB noise reduction in the critical range of clock-harmonics falling between 50 MHz and 150 MHz (see Figure 4). This is the most troublesome frequency range in meeting FCC emission requirements, as that noise will eventually find its way to an "antenna" (I/O cables, etc.) and cause out-of-spec emissions problems.

Conclusion

The value of the power-entry capacitors can be reduced by using larger value circuit level decoupling capacitors (0.1µF). In effect, some of the total capacitance on the PCB is shifted from the power entry capacitor, C_b, to larger-valued decoupling capacitors, C_d.

☐ Please send me the AVX Technical paper "Improved Noise Suppression via MLCs in Power-Entry Decoupling."

☐ Please send me literature describing AVX MLCs.

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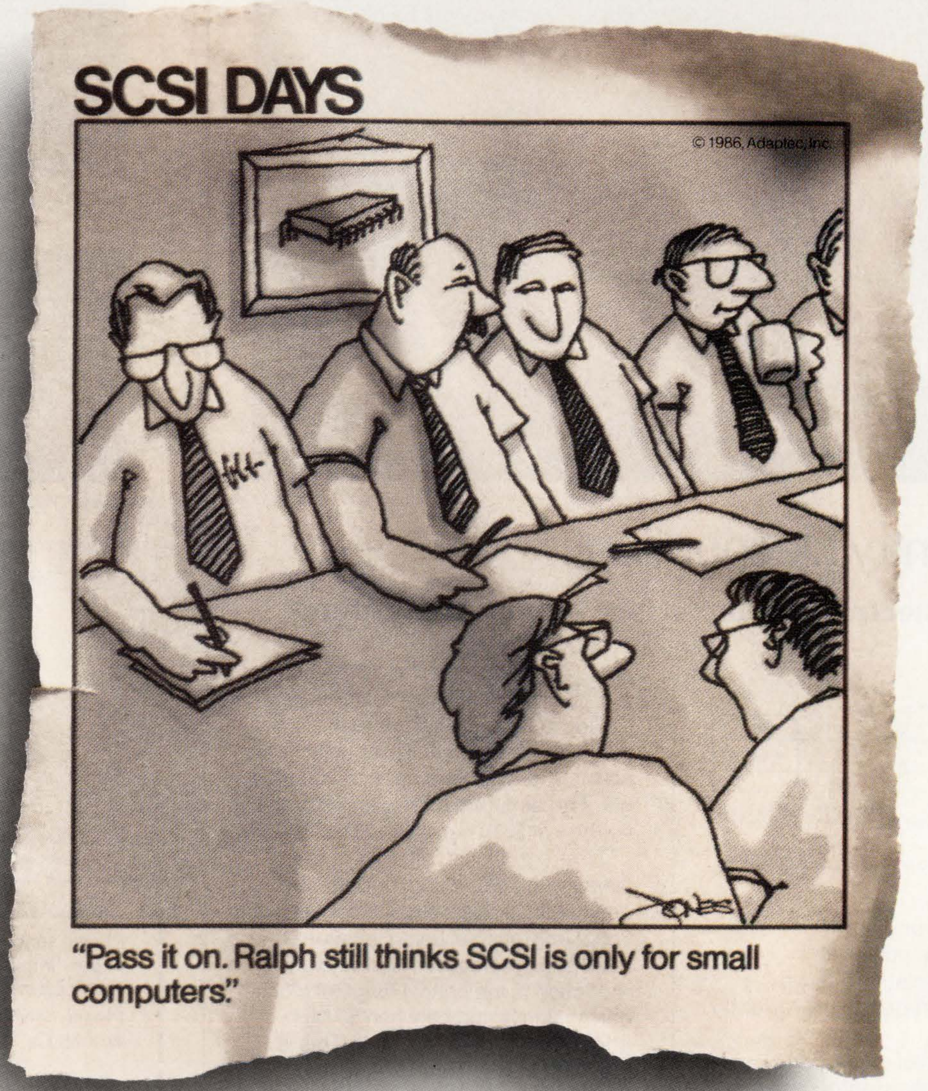

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CALENDAR

Hands-on Programming in C, San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 24 to 27.

Internepcon/Semiconductor Korea '87, Seoul, Korea. Cahners Exposition Group, Box 70007, Washington, DC 20088. (301) 657-3090. March 26 to 28.

Ninth Annual Rocky Mountain Inventors Congress Conference, Denver, CO. Don Margolis, (303) 443-3818. March 27 to 28.

Interface '87, Las Vegas, NV. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. March 30 to April 2.

ADEE West '87, Anaheim, CA. Cahners Exposition Group, 1350 E Touhy Ave, Des Plaines, IL 60017. (312) 299-9311. March 31 to April 2.

Hands-on Programming in C, Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 31 to April 3.

Real-time Operating Systems: A Hands-on Workshop, Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 31 to April 3.

Defense Communications Agency Forecast to Industry, White Oak, MD. Armed Forces Communications and Electronics Association NOVA Chapter, Computer Sciences Corp, 6565 Arlington Blvd, M/C DCA/AFCEA, Falls Church, VA 22046. April 1 to 2.

Microtronics '87, Hannover, West Germany. Hannover Fairs USA, Box 7066, Princeton, NJ 08540. (609) 987-1202. April 1 to 8.

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 CIRCLE NO 150

CALENDAR

Invitational Computer Conference, Nashua, NH. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. April 2.

Conference on Human Factors in Computing Systems and Graphics Interface, Toronto, Canada. Wendy Walker, Conference Coordinator, Computer Systems Research Office, University of Toronto, 10 Kings College Rd, Rm 2002, Toronto, Ontario, Canada M5S 1A4. (416) 978-5184. April 5 to 9.

Electro/Mini Micro Northeast, New York, NY. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (800) 421-6816; in CA, (800) 262-4208. April 7 to 9.

Nepcon Southeast, Orlando, FL. Cahners Exposition Group, Box 5060, Des Plaines, IL 60017. (312) 299-9311. April 7 to 9.

Annual Electrical Overstress Exposition, San Jose, CA. EOE, 2504 N Tamiami Trail, Nokomis, FL 33555. (813) 966-9521. April 21 to 23.

Modern Electronic Packaging, Washington, DC. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. April 21 to 23.

Real-time Operating Systems: A Hands-on Workshop, Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. April 21 to 24.

Invitational Computer Conference Computer Graphics Series, Munich, West Germany. BJ Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. April 23.

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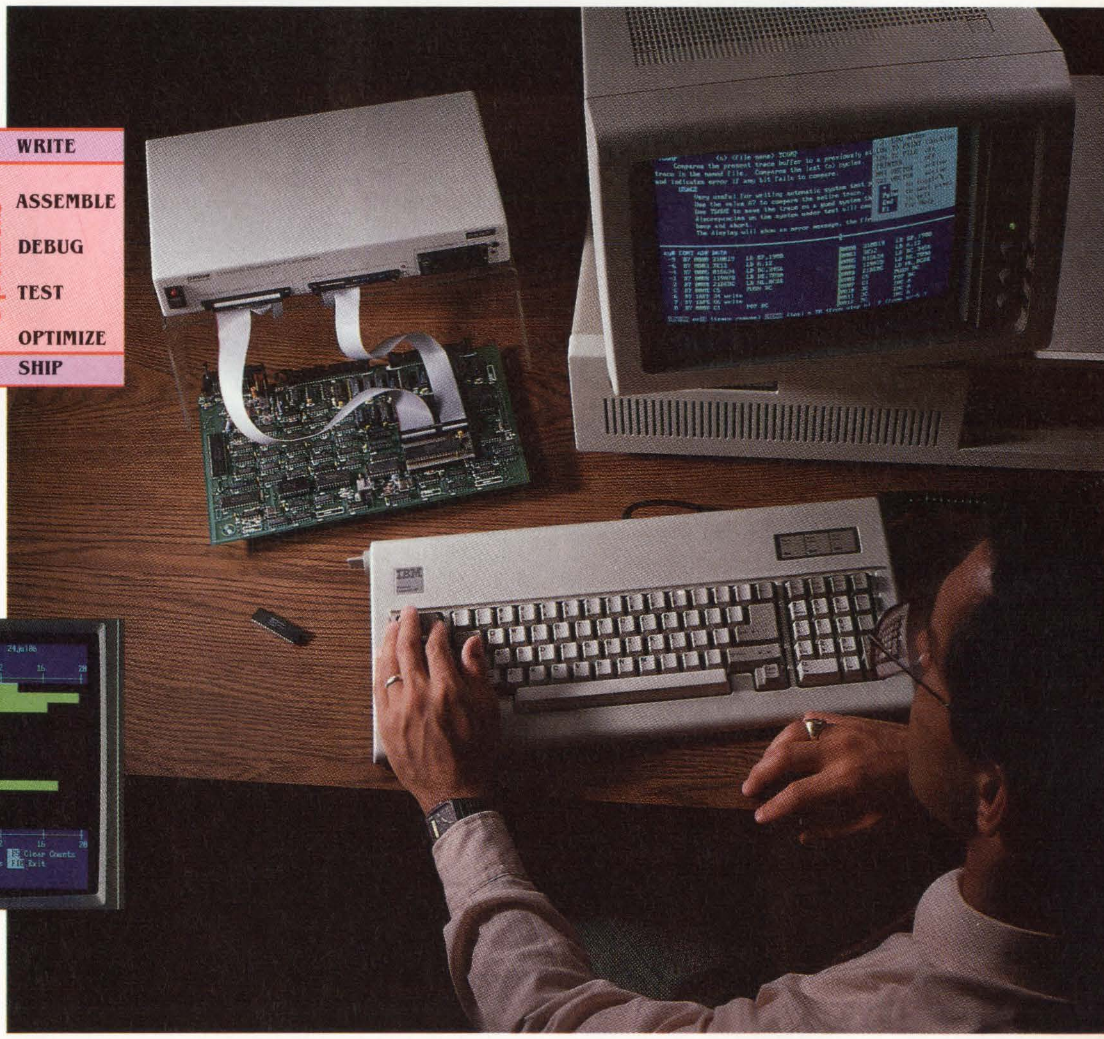

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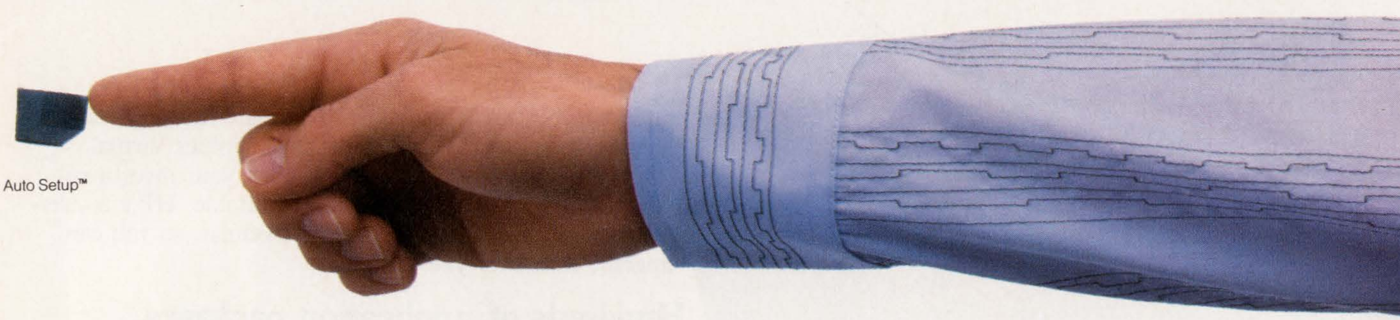

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EDITORIAL

Direct sales costs too much

The pc-board layout packages described in this issue's cover story (pg 138) cost $1000 to $15,000. Until recently, similar software could cost you $30,000 or more. We asked pc-board layout vendors how prices could come down so much, so quickly. Had purveyors of the high-priced models been raking in enormous profits before?

Whatever the earlier profits, vendors concede that profit margins are less for low-cost packages than for high-cost ones. But suppliers of the low-cost ones attribute their lower prices mostly to differences in sales practices. Instead of sending salespeople to prospective customers, vendors of low-cost layout packages use advertisements, distributors, and the mail to reach customers.

The main drawback to using salespeople is the cost incurred to keep them on the road. One company reported that it had spent about $150,000 per year to maintain one salesperson's job. Obviously, when you buy a product from a company that uses direct salespeople, you're indirectly paying for part of those high costs.

If a salesperson adds value to a product, then he or she is worth the extra cost. However, many electronics companies employ salespeople with no engineering training; those people don't understand their products well enough to add that extra value. Such salespeople can even lack the expertise to understand their companies' promotional literature.

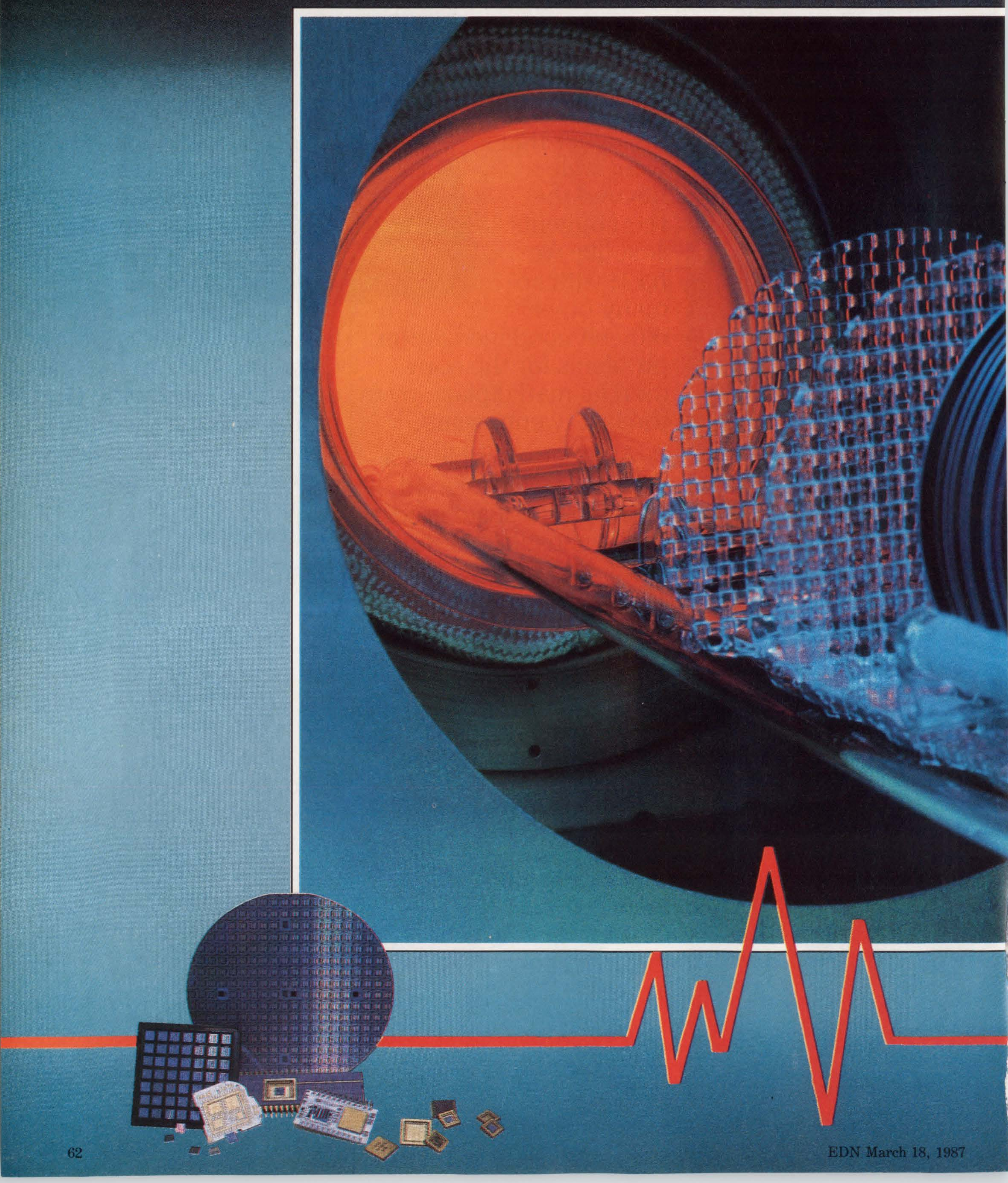
That's not to say you'll never talk to qualified salespeople. But you can learn at least as much as they know from other sources. First, you can read a company's literature and spec sheets. You can also test the product. Software vendors will often send out demonstration disks. Many vendors rely on distributors, who let you run programs in their offices. You'll learn more by trying a program than by listening to someone tell you how wonderful it is.

Alternative sales approaches can thus provide more results per sales dollar than direct sales. Many electronics firms, for example, are following a trend started by the garment industry: They're mailing videotapes that describe their products. The companies that apply such innovative marketing techniques and therefore offer products to you at the lowest cost will be the ones to survive.

Eva C. Freeman

Eva Freeman
Associate Editor

Five good



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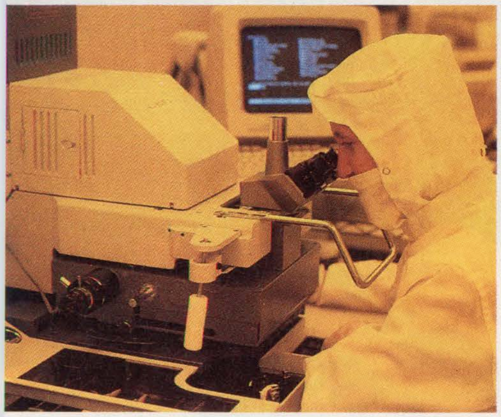

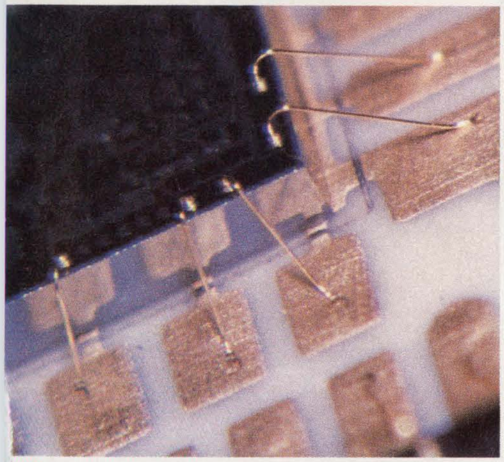

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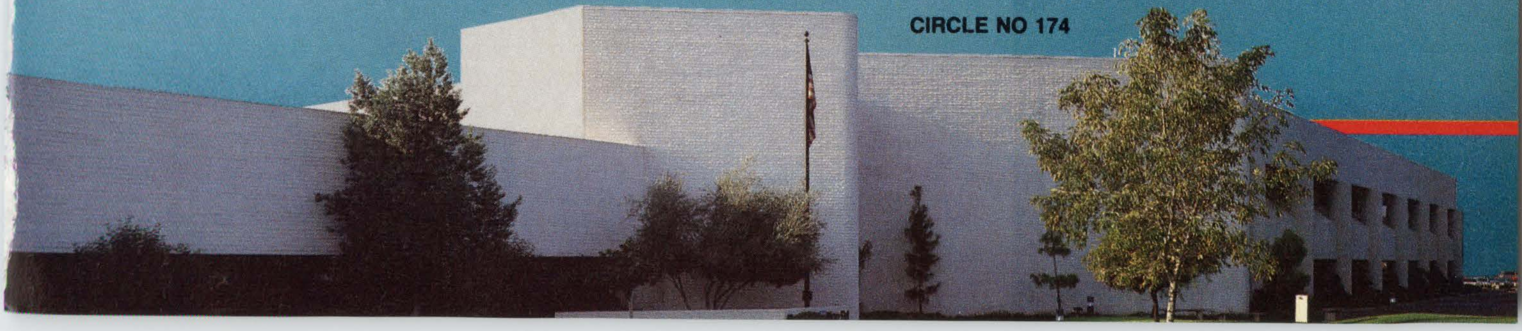

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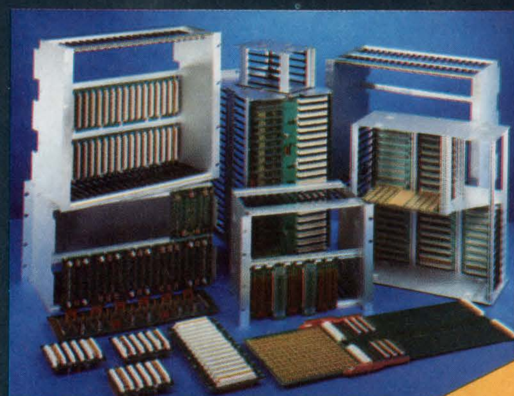

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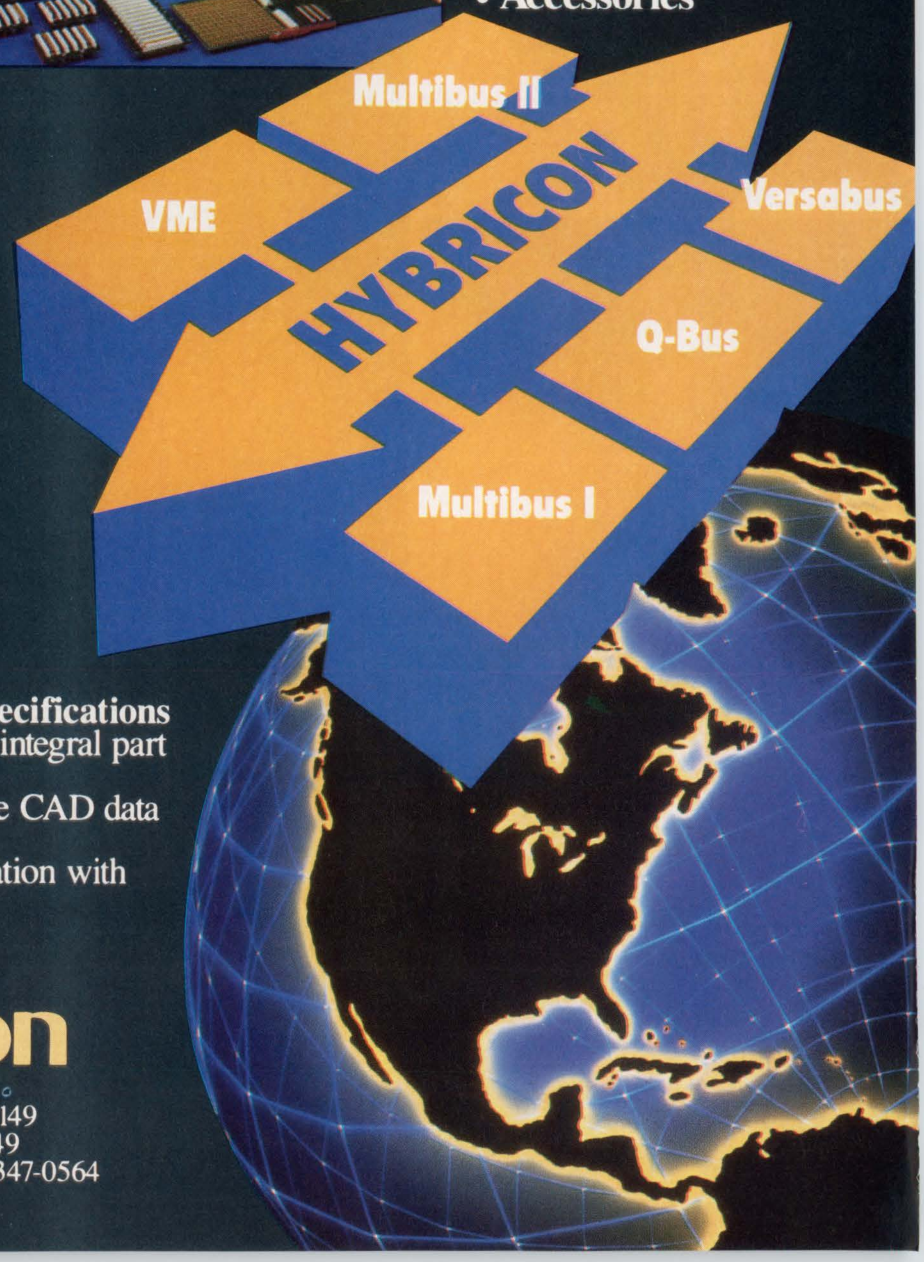

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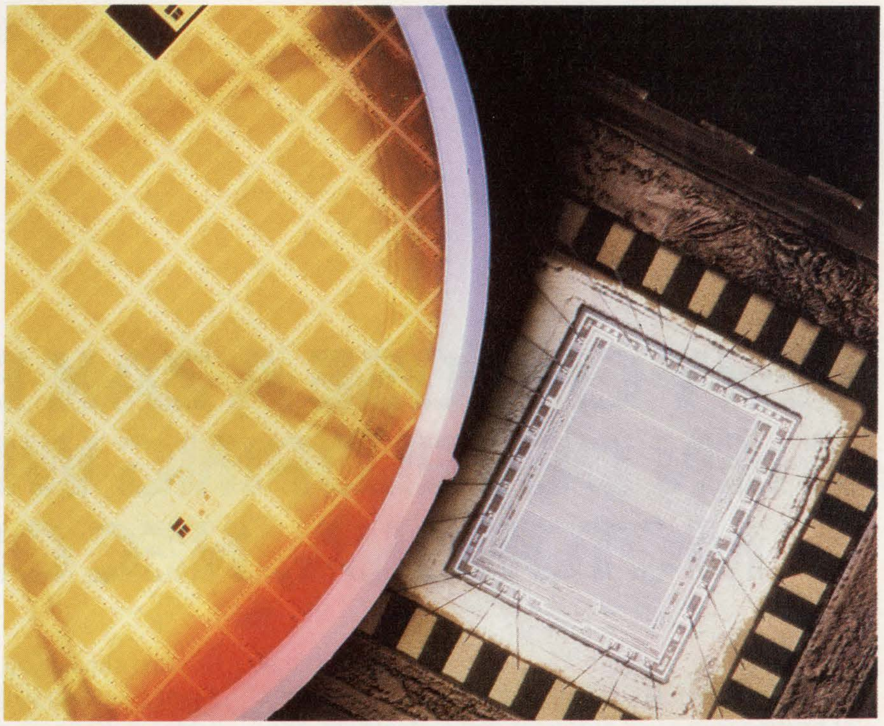
CIRCLE NO 154

TECHNOLOGY UPDATE

Memory-based CMOS FIFO buffers sport large capacities, rival the speed of bipolars

Peter Harold, *European Editor*



Fabricated in CMOS SOS technology, *the 512×9-bit MA7001 FIFO buffer from Marconi Electronic Devices is inherently free of latch-up problems. If there is sufficient demand, the company will manufacture the part to ESA radiation-hardness specifications.*

The latest generation of 9-bit-wide, memory-based FIFO buffers allows you to implement data-rate buffers or data-delay lines as deep as 4096 words with a single chip. With little or no glue logic, you can cascade the FIFO buffers to obtain greater depth, word width, and data rate. Because most of these FIFO buffers are based on an industry-standard pinout, many FIFO buffers with different depths maintain pin and functional compatibility with one another. Others depart from the norm to provide novel features—for example, serial I/O, programmable status flags, and parity generation/checking logic.

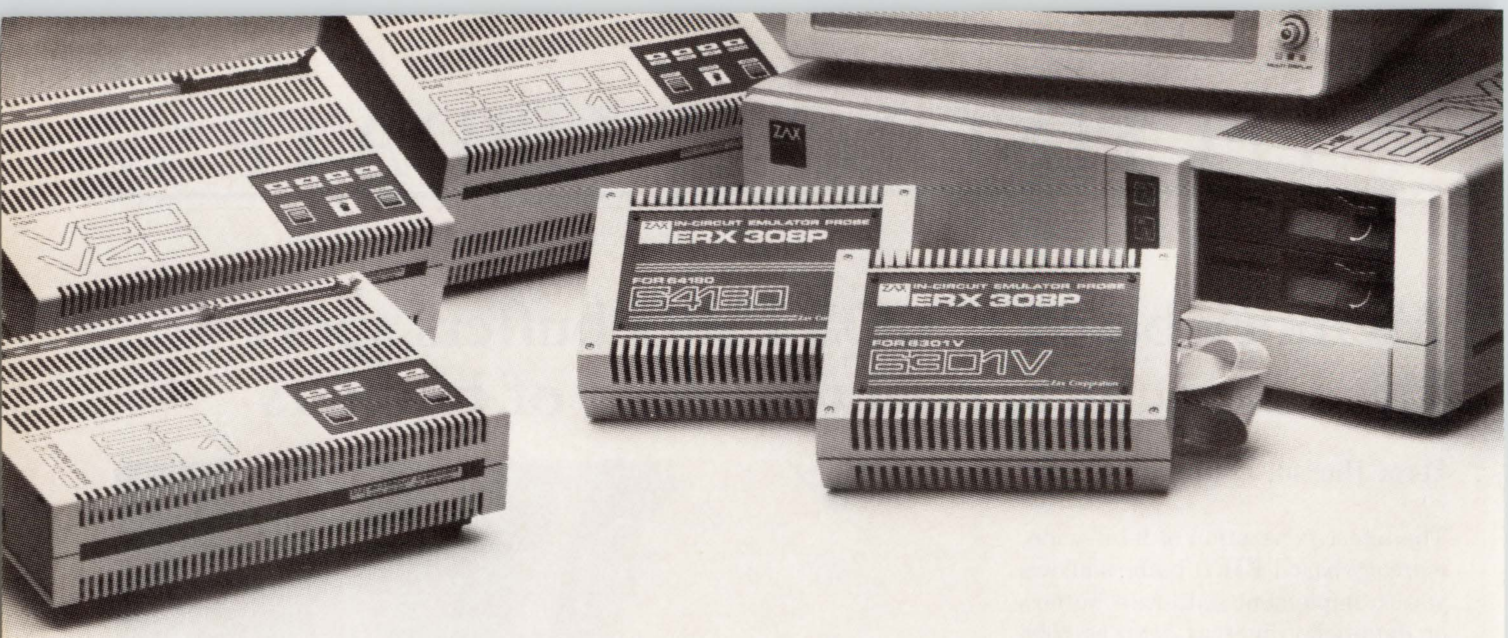
High-capacity FIFO buffers are based on memory architectures rather than on the shift-register technology often used to fabricate their smaller 64-word counterparts. By employing the latest CMOS biport memory-cell techniques, several manufacturers have created high-capacity FIFO buffers that are capable of sustaining input and output data rates of 15 or 20 MHz, rivaling the speed of smaller bipolar parts. In addition, the new buffers' memory architecture eliminates the ripple-through delays that contribute to the input-to-output latency time inherent in shift-register FIFO buffers.

A memory-based FIFO buffer has a static-RAM array to which input data is written and from which output data is read. The RAM is addressed by two ring counters, one containing an In pointer and one containing an Out pointer. The In pointer defines the next RAM location that input data is to be written to; the Out pointer defines the next location that output data is to be read from. Internal comparators, which keep track of the difference between the In pointer and the Out pointer, serve to activate status flags that tell you how full the FIFO buffer is. You could think of these FIFO buffers as a hardware implementation of the circular buffer often created in software to queue data into a μP-based system.

Because the data contained in a memory-based FIFO buffer remains static in a memory location, no shifting of data from one memory location to another is required as the FIFO buffer fills and empties. Hence, the input-to-output latency time is only the time taken to perform one write cycle and one read cycle on the RAM—it's typically on the order of 100 nsec or less for a memory-based FIFO buffer fabricated in CMOS technology.

One of the first memory-based FIFO buffers to become commercially available was the 512×9-bit MK4501 CMOS FIFO buffer, which was designed by Mostek before its takeover by Thomson Semiconductors. The buffer's pinout and I/O architecture have subsequently been adopted as an industry standard.

Because a memory-based FIFO buffer's memory array requires no external addressing (all read/write addressing is handled internally by the two ring counters), it's possible to make FIFO buffers of any capacity pin compatible with one another, as long as they have the same data width. As a result, several other manufacturers have announced, or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are about to announce, MK4501-compatible parts having capacities as great as 4096 words. This compatibility isn't confined to single-device operation either—the parts maintain compatibility even when you use multiple devices to expand FIFO-buffer depth or width. If you expand your FIFO buffer's depth by cascading devices as shown in **Fig 1,** you can use exactly the same interconnection scheme for 4096-word FIFO buffers that you'd use for 512-word FIFO buffers.

Manufacturers offer MK4501-compatible devices in a range of capacities and speed selections. **Table 1** gives salient specs for a number of these devices. You'll find that most of the parts listed in the table as MK4501 compatibles have a Half-Full flag output, which doesn't exist on the MK4501. Generating the Half-Full status flag is actually a second function of the expansion-out pin on most of these devices. You can use the pin as a Half-Full flag output only when you're using a single device to implement your system's FIFO buffer. When you configure multiple devices for depth expansion, the Half-Full output automatically reverts to the expansion-out pin function.

If you're concerned about CMOS latch-up problems—for example, if you're designing equipment for use in electrically harsh environments—consider using Marconi Electronic Devices' MA7001 512×9-bit FIFO buffer. The device, which is pin and function compatible with the Thomson Components-Mostek MK4501, is fabricated in CMOS SOS (silicon-on-sapphire) technology, so it's inherently free of latch-up problems. In addition, even the standard part has a degree of radiation hardness; it can withstand a total-dose radiation level of around 50k rads. If there is sufficient demand, Marconi says, it will produce the part with a radiation-hardness spec that meets the full ESA (European Space Agency) requirements.

Although Mostek took the early lead, it's Integrated Device Technology Inc that currently offers the largest range of commercially available memory-based FIFO buffers. To add to its 512×9-bit, 1024×9-bit, 2048×9-bit, and 4096×9-bit MK4501 pin-compatible FIFO buffers, the company has recently introduced the 2048×9-bit IDT72103 and 4096×9-bit IDT72104, which

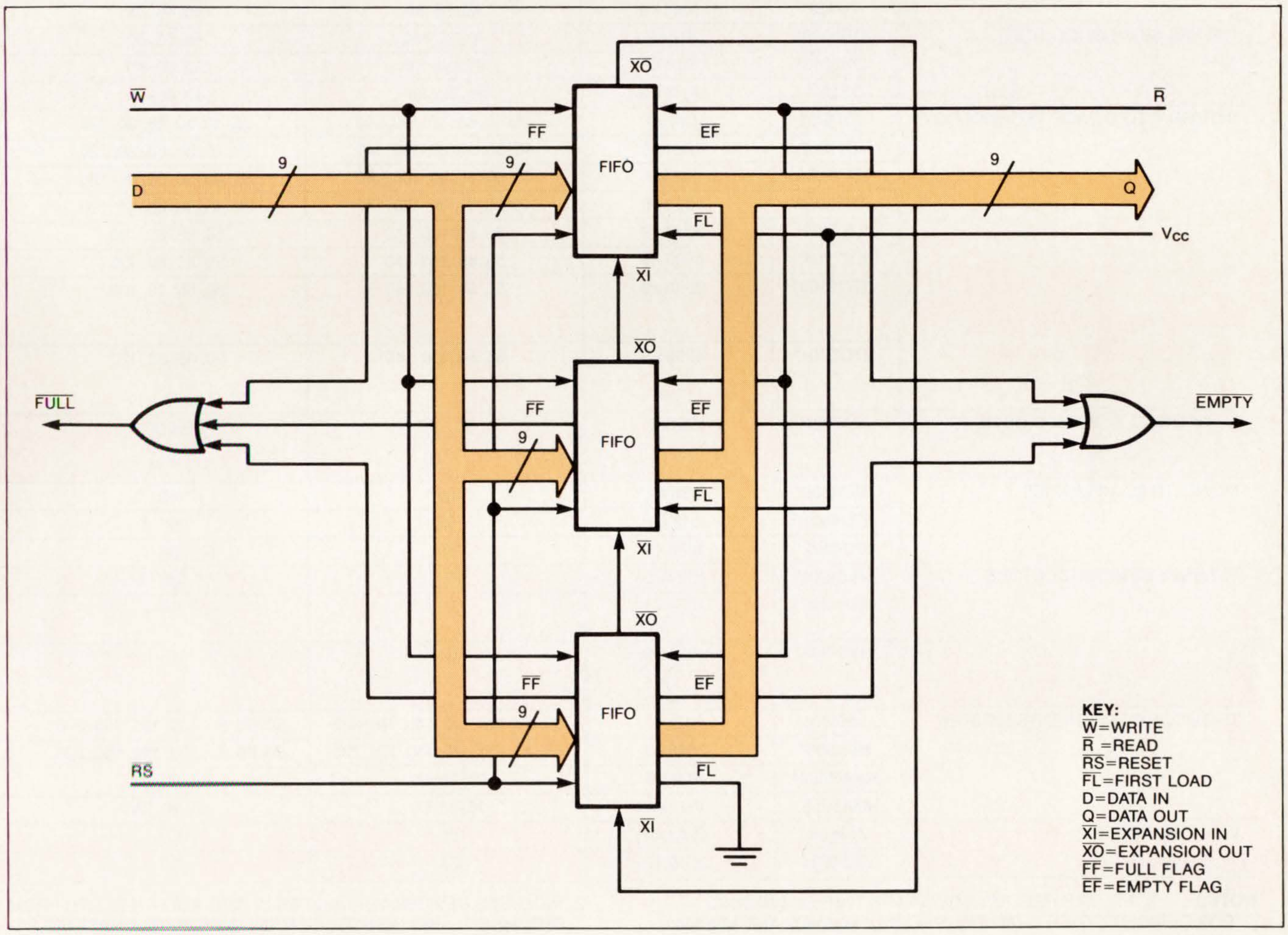


Fig 1—You can expand a FIFO buffer's depth *by using any MK4501-compatible FIFO buffer, irrespective of its capacity, in the above circuit. If your device implements pin 20 as a Half-Full flag output, this output automatically reverts to the expansion-out ($\overline{XO}$) signal when you connect multiple devices.*

feature serial and parallel data inputs and outputs. These FIFO buffers target applications in which the data source or destination is a bit-serial device, such as a magnetic disk drive, a video scan, or a communication link.

The IDT72103 and IDT72104 FIFO buffers incorporate a parallel or serially loaded input register and an output register with parallel and serial outputs. Independent serial/parallel mode controls on the input and output registers allow you to create a serial-to-serial, parallel-to-parallel, serial-to-parallel, or parallel-to-serial FIFO buffer. The part that specs a 65-nsec cycle time lets you load the input or unload the output at serial clock frequencies as high as 40 MHz.

Because serial data is often divided into word lengths other than nine bits, you can program the input register of the IDT72103 and IDT72104 to accept any word length greater than four bits. When you program the FIFO buffer to operate in the serial-input mode, the parallel data inputs become the outputs of an internal, clocked, digital delay line. You program the word length by routing a suitable delay-line output to the write-pulse input of the FIFO buffer. When that delay-line output becomes active, it initiates the parallel transfer of data from the input register to the FIFO buffer's RAM array, and it resets the input register and delay line so they're ready to receive the next serial data word. In addition, the serial-input register has its own expansion logic; you can use multiple devices to expand the word length

TABLE 1—REPRESENTATIVE HIGH-CAPACITY, HIGH-SPEED CMOS FIFO BUFFERS

MANUFACTURER	PART NUMBER	ORGANIZATION (BITS; DEPTH×WIDTH)	MINIMUM READ/WRITE CYCLE TIME (nSEC)	MAXIMUM READ-ACCESS TIME[1] (nSEC)
CYPRESS SEMICONDUCTOR	7C412*	512×9	40, 50, 80	30, 40, 65
	7C424*	1024×9	40, 50, 80	30, 40, 65
	7C429*	2048×9	40, 50, 80	30, 40, 65
DALLAS SEMICONDUCTOR	DS2009*	512×9	65, 80, 100	50, 65, 80
	DS2010*	1024×9	65, 80, 100	50, 65, 80
	DS2011*	2048×9	65, 80, 100	50, 65, 80
INTEGRATED DEVICE TECHNOLOGY	IDT7201	512×9	45, 50, 65, 80, 100, 140	35, 40, 50, 65, 80, 120
	IDT7202	1024×9	45, 50, 65, 80, 100, 140	35, 40, 50, 65, 80, 120
	IDT7201A	512×9	45, 50, 65, 80, 100, 140	35, 40, 50, 65, 80, 120
	IDT7202A	1024×9	45, 50, 65, 80, 100, 140	35, 40, 50, 65, 80, 120
	IDT7203*	2048×9	65, 80, 100, 140	50, 65, 80, 120
	IDT7204*	4096×9	65, 80, 100, 140	50, 65, 80, 120
	IDT72103*	2048×9	65, 80, 100, 140	50, 65, 80, 120
	IDT72104*	4096×9	65, 80, 100, 140	50, 65, 80, 120
MARCONI ELECTRONIC DEVICES	MA7001*	512×9	80, 100	65, 80
MONOLITHIC MEMORIES	67C4500*	256×9	65	50
	67C4501*	512×9	65	50
	67C4502*	1024×9	65	50
PLESSEY SEMICONDUCTORS	MV61901*	1024×9	60	45
	MV61902*	1024×9	60	15
	MV61903*	1024×9	60	15
THOMSON COMPONENTS-MOSTEK	MK4501	512×9	65, 80, 100, 120, 140, 175, 235	50, 65, 80, 100, 120, 150, 200
	MK4503*	2048×9	65, 80, 100, 120, 140, 175, 235	50, 65, 80, 100, 120, 150, 200
	MK4505M*	1024×5	25, 33, 50	15, 20, 25
	MK4505S*	1024×5	25, 33, 50	15, 20, 25
VLSI TECHNOLOGY	VT2KF9*	2048×9	65	50
	VT2KF91*	2048×9	65	50

NOTES: * DATA WAS PRELIMINARY AT THE TIME OF WRITING
1. FOR DEVICES OTHER THAN THE PLESSEY MV61902 AND MV61903 AND THE THOMSON COMPONENTS-MOSTEK MK4505M AND MK4505S, WHICH ARE EDGE-ACTIVATED, THESE FIGURES ALSO REPRESENT THE MINIMUM READ/WRITE PULSE WIDTHS.
2. INCLUDES DEVICES THAT DIFFER IN FIFO-BUFFER DEPTH FROM THE MK4501, AND DEVICES THAT INCORPORATE A HALF-FULL FLAG ON PIN 20 FOR USE IN SINGLE-DEVICE MODE.
3. USE ONLY AS A PRICE GUIDE. PRICE QUOTED IS GENERALLY FOR A LOW-SPEED, COMMERCIAL-GRADE DEVICE.

to greater than nine bits while maintaining the serial word-length programmability. Similar word-length-programmability and expansion facilities exist for the serial output.

The IDT72103 and IDT72104 also feature an impressive array of status flags. In addition to Full, Empty, and Half-Full flags, they have Full−1, Empty+1, Almost-Full, and Almost-Empty flags. The Empty+1 and Full−1 flags indicate that the FIFO buffer has only one filled or one vacant location, respectively. The Almost-Empty and Almost-Full flags are asserted when the FIFO buffer is less than ⅛ full or more than ⅞ full, respectively.

Plessey Semiconductors' MV-61902 and MV61903 FIFO buffers—both of which are organized as 1024×9 bits—are the only FIFO buffers that have user-programmable status flags. In addition to their conventional FIFO-Empty and FIFO-Full flags, these FIFO buffers have a third flag, which the manufacturer has trademarked as the "Dipstick flag."

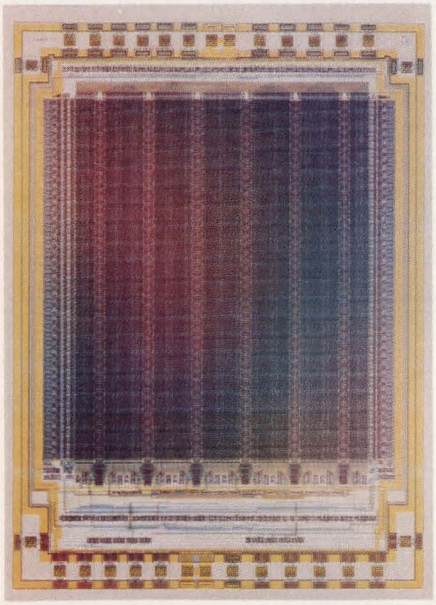
You can program a register within the FIFO buffer so that the Dipstick flag becomes active when a specified number of buffer locations is occupied by data. You specify this number of locations, which can be any number between 0 and 1023, by applying a 10-bit word to the FIFO buffer and by applying a shift-in clock pulse while holding the buffer's master-reset pin active. The nine most significant bits of the 10-bit word are applied to the device's data-input pins, while the least significant bit enters through

FLAGS	MK4501 PIN COMPATIBILITY	PACKAGE (NUMBER OF PINS)	PRICE[3]	REMARKS
E, HF, F	•	DIP (28), LCC (32)	SAMPLES Q2 '87	
E, HF, F	•	DIP (28), LCC (32)	SAMPLES Q2 '87	
E, HF, F	•	DIP (28), LCC (32)	SAMPLES Q2 '87	
E, HF, F	•	DIP (28)	$10.00 (100)	
E, HF, F	•	DIP (28)	$19.50 (100)	
E, HF, F	•	DIP (28)	$42.80 (100)	
E, F	•	DIP (28), PLCC (32), LCC (32)	$13 (100)	
E, F	•	DIP (28), PLCC (32), LCC (32)	$18 (100)	
E, HF, F	•	DIP (28), PLCC (32), LCC (32), TDIP (28), FP (28)	$13 (100)	
E, HF, F	•	DIP (28), PLCC (32), LCC (32), TDIP (28), FP (28)	$18 (100)	
E, HF, F	•	DIP (28), PLCC (32), LCC (32)	$27.00 (100)	
E, HF, F	•	DIP (28), PLCC (32), LCC (32)	$40.50 (100)	
E, E+1, AE, HF, AF, F−1, F		DIP (40), PLCC (44), LCC (44)	$37.00 (100)	DEVICES HAVE BOTH PARALLEL AND SERIAL I/O
E, E+1, AE, HF, AF, F−1, F		DIP (40), PLCC (44), LCC (44)	$55.50 (100)	DEVICES HAVE BOTH PARALLEL AND SERIAL I/O
E, F	•	DIP (28), LCC (28)	£12.74 (1000)	FABRICATED IN CMOS SOS TECHNOLOGY
E, HF, F	•	DIP (28), PLCC (28), LCC (28)	$15.95 (1000)	
E, HF, F	•	DIP (28), PLCC (28), LCC (28)	$18.15 (1000)	
E, HF, F	•	DIP (28), PLCC (28), LCC (28)	$25.40 (1000)	
E, HF, F	•	DIP (28)	£26.92 (1000)	
E, DS, F		DIP (28)	£37.96 (1000)	PROGRAMMABLE DIPSTICK FLAG
E, DS, F, PE		DIP (28)	£41.41 (1000)	PROGRAMMABLE DIPSTICK FLAG AND PARITY LOGIC
E, F	•	DIP (28), PLCC (32), LCC (32)	$13.43 (100)	
E, HF, F	•	DIP (28), PLCC (32)	AVAILABLE Q1 '87	
E, AE, HF, AF, F		TDIP (24)	AVAILABLE Q2 '87	
HF		TDIP (20)	AVAILABLE Q2 '87	
E, HF, F	•	DIP (28), PLCC (32)	$40.34 (1000)	
E, AE, AF, F		PLCC (32)	$41.50 (1000)	

KEY: AE=ALMOST EMPTY
AF=ALMOST FULL
DS=PROGRAMMABLE DIPSTICK FLAG
E=EMPTY
F=FULL
HF=HALF FULL
PE=PARITY ERROR
DIP=600-MIL DUAL-IN-LINE PACKAGE
FP=FLAT PACK
LCC=LEADLESS CHIP CARRIER
PLCC=PLASTIC LEADED CHIP CARRIER
TDIP=300-MIL DUAL-IN-LINE PACKAGE

the FIFO buffer's output-ready pin.

Because the output-ready pin normally functions as an output, when you're programming the Dipstick-flag value you'll have to drive the output-ready pin from 3-state logic or from a 0 to 5V logic source with a source impedance of 10 kΩ or more.



This micrograph of a 2k×9-bit FIFO buffer, VLSI Technology's VT2KF9, illustrates the regular array of memory cells typical of memory-based CMOS FIFO buffers.

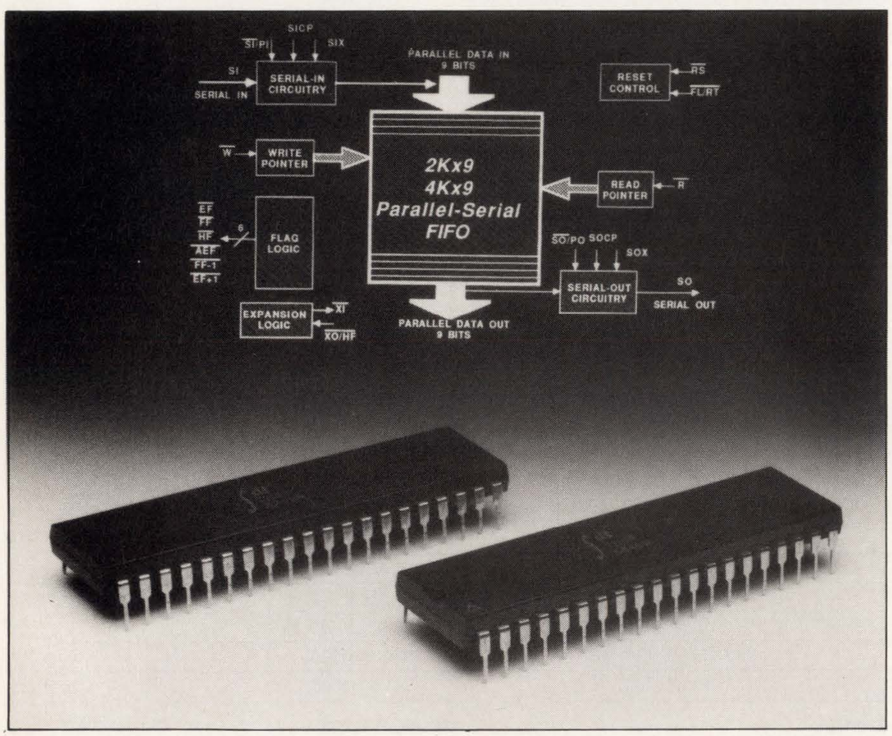
The dipstick value remains intact during subsequent reset periods, provided you don't issue a further shift-in pulse during these resets. If you don't program the dipstick value at all, it remains at its power-up value, which sets the dipstick function to act as a Half-Full flag.

In addition to offering the Dipstick function, the MV61903 FIFO buffer incorporates parity checking/generation logic. You can program the parity logic to check the even or odd parity of the eight least significant input bits against the ninth input bit; parity errors are indicated on a separate parity-error flag output. Alternatively, you can program the parity logic to generate an even or odd parity bit from the eight least significant input bits (after they have passed through the FIFO buffer); this bit is then substituted for the ninth bit in the output data. You program the parity logic during master-reset periods at the same time that you program the Dipstick flag, by using the parity-error and Dipstick-flag outputs as inputs into which you place a 2-bit code. This 2-bit code allows you to enable or disable parity generation and to select even or odd parity generation/checking. As with the output-ready pin, you'll have to drive the parity-error pin and Dipstick-flag pin from 3-state logic or from a 0 to 5V logic source with a source impedance of 10 kΩ or more.

The MV61902 and MV61903 aren't pin compatible with the MK4501. Because their input and output handshaking controls are different from those of the other FIFO buffers listed in **Table 1**, and because they each have an independent, 3-state, output-enable control line, their 28-pin package is short on pins. As a result, the MV61902 has only two outputs with which to indicate the FIFO-Full, FIFO-Empty, and Dipstick flags, and the MV61903 has room for only one capacity-flag output, which it uses to indicate the state of the Dipstick flag.

The MV61902 must, therefore, encode three flag conditions on its two flag-output lines. As a result, you'll need a few spare 2-input gates and inverters or a 2- to 4-line decoder chip to decode the two flag-output lines into single-line flag outputs. Similarly, with the MV61903 you'll require a couple of D-type flip-flops to decode the FIFO-Empty and FIFO-Full conditions from the input and output handshaking lines.

In some applications, however, the Dipstick flag can save you external logic. For example, if you want to delay data by a programmable number of clock periods—a common requirement in DSP applications—all you need to do is to AND the dipstick-flag output with the shift-in clock and connect the AND-gate output to the shift-out clock. When you start to clock the FIFO buffer, data will be placed in the FIFO buffer, but the AND-gate output



***Featuring parallel and serial I/O ports,** the 2k×9-bit IDT72103 and 4k×9-bit IDT72104 FIFO buffers from Integrated Device Technology provide data-rate buffering for serial devices such as disk drives. In addition, each device sports seven status flags that indicate the amount of data in the FIFO buffer.*

won't start to clock data out until the Dipstick flag becomes active. Because you can program the Dipstick to any value between 0 and 1023, you have full control over the input-to-output delay.

Although they don't have the fastest read/write cycle time, the MV61902 and MV61903 do possess the fastest read-access time (15 nsec) of any of the 9-bit FIFO buffers listed in **Table 1.** Further, the MV61902 and MV61903 each have a separate 3-state output control. Using these features, you can double a FIFO-buffer system's data rate by multiplexing data between two devices as shown in **Fig 2.**

The MV61902 and MV61903 FIFO buffers also feature a 0-nsec data-hold time relative to the active edge of the shift-in pulse. This spec could save you a 9-bit latch if you're interfacing to systems that don't guarantee they will hold data after the active clock edge.

Note that the unique features of the MV61902 and MV61903 are the Dipstick flag and parity logic. You could implement some applications that use these features—for example, the programmable digital delay line—by adding external logic to other, less-expensive FIFO buffers. Unless you're constrained by other factors, such as pc-board space or power-supply considerations, therefore, you should weigh the higher cost of the MV61902 and MV61903 against the cost of the external logic that you'd have to add to other FIFO buffers to achieve the same functionality.

Thomson Components-Mostek Corp should soon be able to lay claim to the fastest high-capacity, memory-based FIFO buffer around. One speed selection of its 1024×5-bit MK4505 FIFO buffer, which is currently under development, specs a read/write cycle time of 25 nsec, which allows the input and output of parallel data at clock frequencies as high as 40 MHz. The device has independent input and output clocks. It's designed for use in systems (such as digitized video or

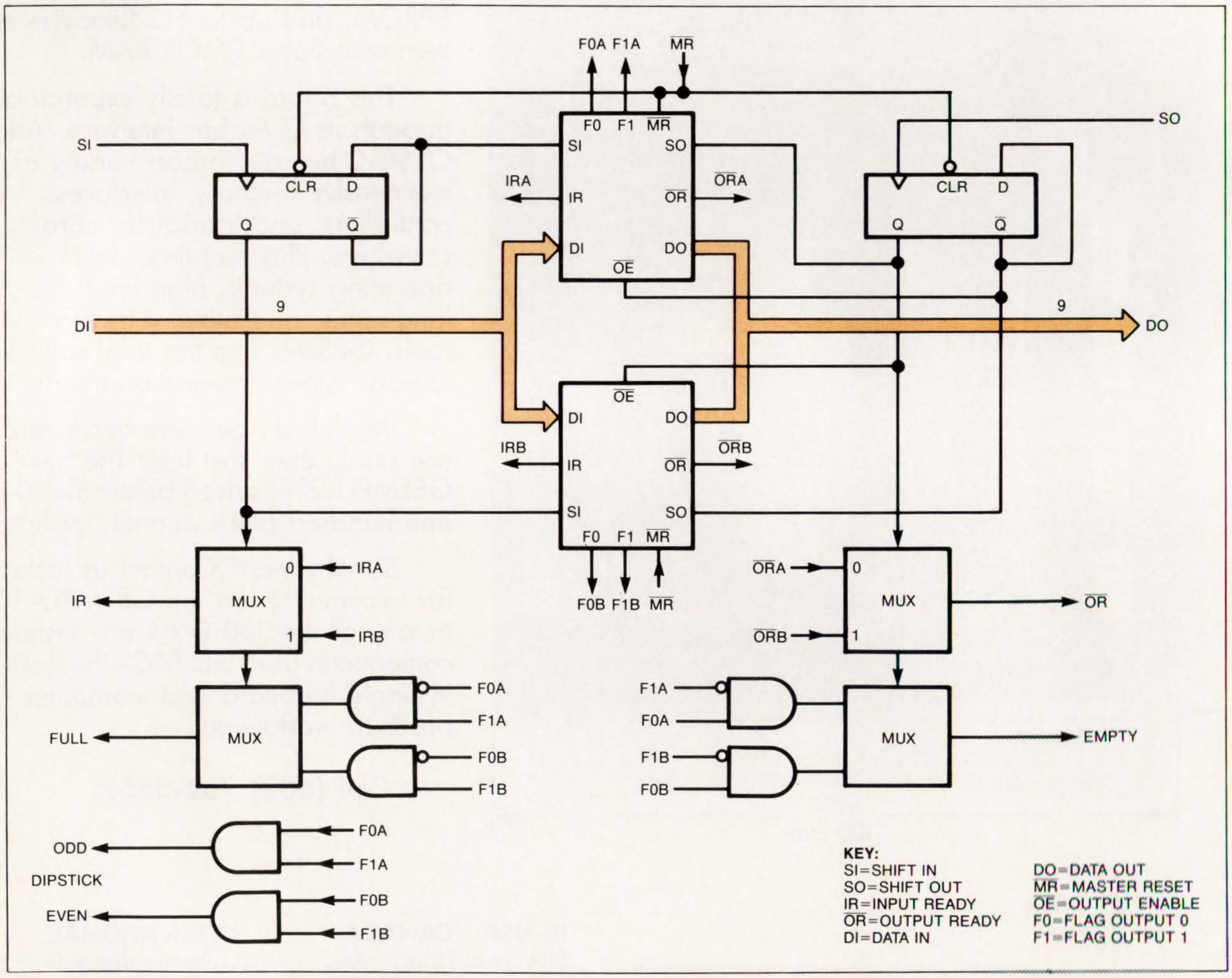


Fig 2—To double the speed of your FIFO-buffer system, *you can take advantage of the 15-nsec read-access time of Plessey Semiconductors' MV61902 by using this circuit, which multiplexes data between two FIFO buffers. Although you could apply this technique to other manufacturers' FIFO buffers, you'd require more complex external logic to do so.*

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TECHNOLOGY UPDATE

audio, image processing, or continuous A/D- or D/A-conversion systems) through which data moves continuously on a square-wave clock.

The MK4505 will be available as either a 24-pin master device (MK4505M) or a 20-pin slave device (MK4505S) in the second quarter of 1987. The master device provides all the control signals necessary to expand a FIFO buffer's width and depth, and it also includes Empty, Almost-Empty, Half-Full, Almost-Full, and Full flags, as well as Input-Ready and Output-Valid handshaking pins.

The slave device has only a Half-Full flag, but it has a second write-enable input, and it includes an additional read-enable input that acts as a 3-state output control. Unlike the master device, the slave device can be forced to write data to and read data from the RAM array irrespective of the FIFO buffer's Full or Empty status. In other words, when the FIFO buffer is full, you can overwrite its contents. When the FIFO buffer's status is set at Empty (after you've read the last word out of it), you can make it reread the entire contents of the FIFO buffer. Note that the ability to reread the entire contents of the FIFO buffer differs from the retransmit facility on MK4501-compatible devices; that facility resets the memory array's Out pointer to location 0. This feature allows you to implement such functions as data-tracing (continuous write) or message-retry (continuous read) operations. **EDN**

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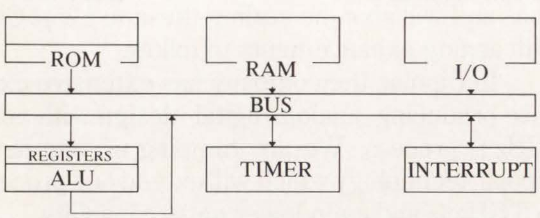
Low Voltage:	3 Volts
Low Power:	<1 mA Static Halt Mode



100% compatible with National's COP820C 8-bit microcontroller, this core processor features modifications on its pinout to make it more flexible. Because of its small size and versatile architecture, it can be combined—on a single chip—with digital, analog, EEPROM and peripheral megacells from our library, such as keyboard encoder, UART, RTC, LCD/LED driver, and Watch Dog timer. The net result is a dramatic savings in part cost and board area.

FEBRUARY

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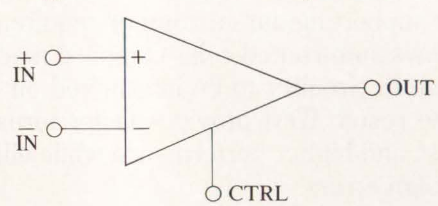
Key Features

Differential Input Pulse Width	20 ns (min)
Output Pulse Width	12 ns (min)
Internal Hysteresis	150 mV (typ)
Output Drive Current @ Vol = 0.5V	48 mA (min)
Operating Range	4.5 to 5.5 Volts 0 to 70° C
Technology	2μ CMOS



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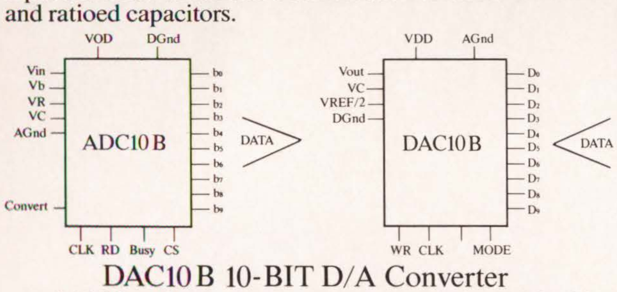
MARCH

ADC10B 10-BIT A/D Converter

Key Features (Both cells)

Accuracy	10-bit
Power consumption	5V ± 10%
Technology	2μ CMOS

A low-power, 10-bit successive approximation differential input converter which uses a combination of ratioed resistors and ratioed capacitors.



DAC10B 10-BIT D/A Converter

A 10-bit ratioed capacitor and resistor string DAC with a deglitched sampled-and-held buffered output. Like the ADC10, it also uses 2 micron technology. In CMOS. All of which makes us a tough act to follow. And gives you a good reason to watch this space in April.

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- large I/O family available in both pad limited and core limited layouts for smallest die
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TSSB SERIES / TSSC SERIES
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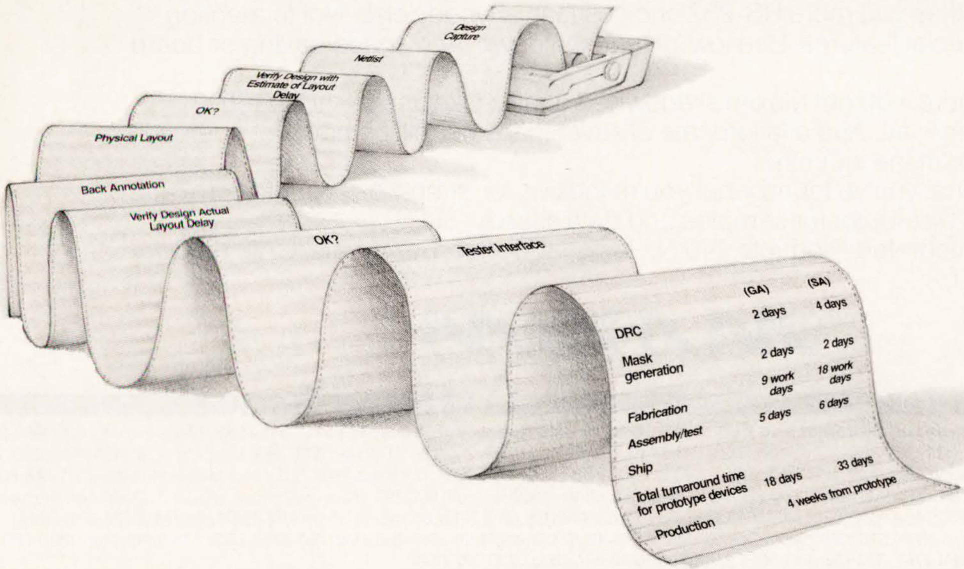
GATE ARRAY PRODUCTS

TSGB SERIES (2μ) **TSGC SERIES** ($1.2^*\mu/2\mu$) with 1K-10K densities

TSGB/GC No.	No. Gates	No. I/O	PWR	DIP Package	Pin Grid Arrays	Chip Carriers
01000	1120	56	12	28, 40, 48 (C/P)	68 (C/P)	44, 52, 68 (C/P)
02000	2128	76	12	28, 40, 48 (C/P)	68, 84 (C/P)	44, 51, 68 (C/P) 84 (C)
03000	3264	96	12		68, 84, 100 (C/P)	68, 84 (C/P) 100 (C)
04000	4256	108	12		68, 84, 100, 120 (C/P)	68, 84 (C/P) 100, 124 (C)
06000	5880	132	12		68, 84, 100, 120 (C/P) 144 (C)	68, 84 (C/P) 100, 124 (C)
08000	7872	168	16		84, 100, 120 (C/P) 144, 180 (C)	84 (C/P) 100, 124 (C)
10000	9776	192	16		84, 100, 120 (C/P) 144, 180, 208 (C)	84 (C/P) 100, 124 (C)

C = ceramic, P = plastic



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Peripheral Interface	MAX231*	2	2	No	No	14	2.52
General Purpose Interface	MAX232	2	2	No	No	16	3.60
Gen. Pur. Interface/ Space Saver	MAX233	2	2	No	Yes	20	6.75
+5V 1488 Replacement	MAX234	4	0	No	No	16	3.60
Synchronous Communications	MAX235	5	5	Yes	Yes	24	10.00
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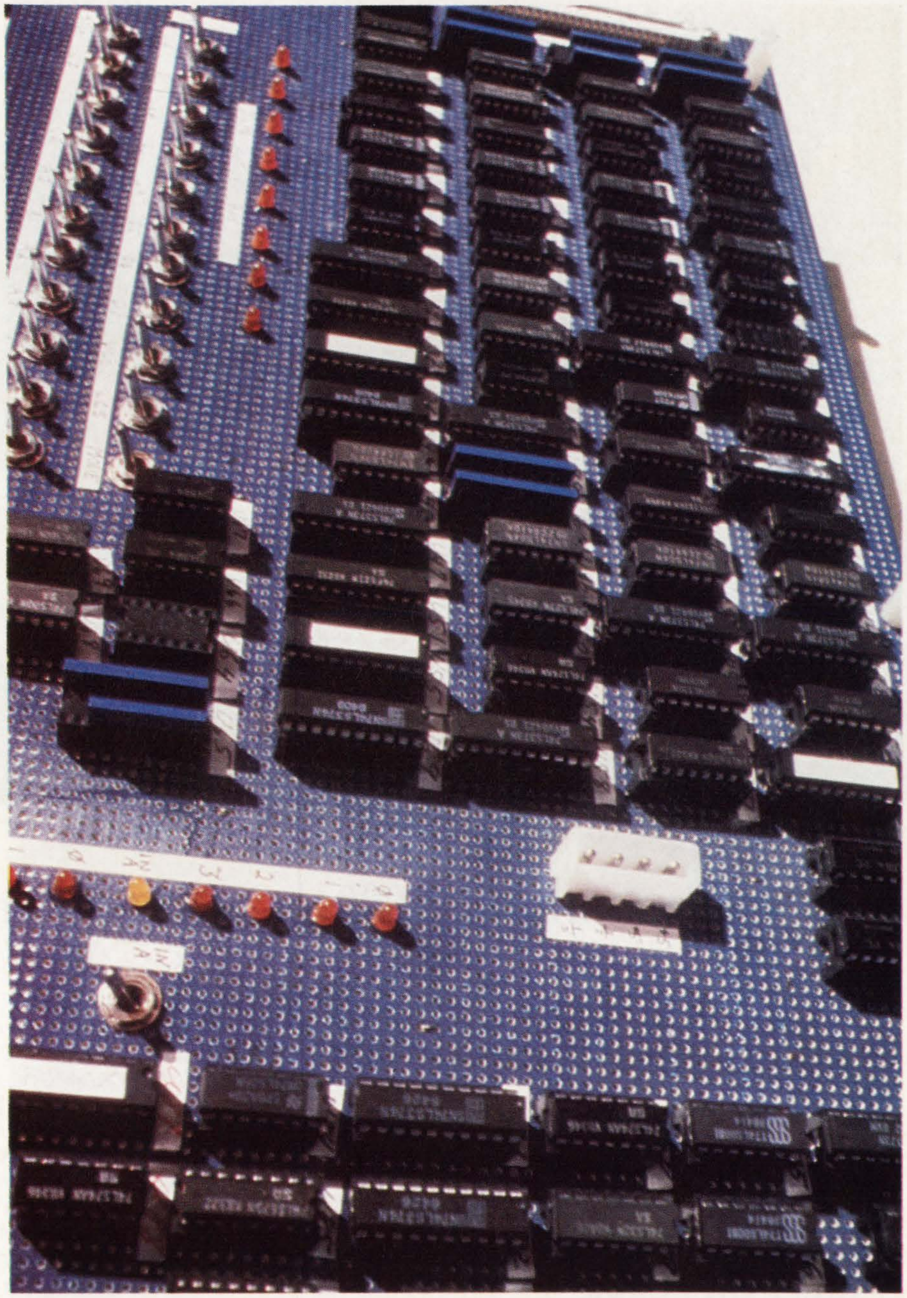
Tools help you retain the advantages of using breadboards in gate-array design

David Shear, *Regional Editor*

When you've considered the various approaches to developing a gate array, you may have deemed the use of a breadboard as impractical. Simulation has promised to make breadboards obsolete, and the effort to create the breadboard sometimes seems prohibitive. Now, however, with careful selection of device types and helpful design tools, you can reap the benefits that creating a breadboard still confers, whether you intend to build a gate-array design right away, or to convert from a design initially based on programmable devices to gate-array form at a later date. In the near future, you may be able to retain these benefits through the use of emulators that allow a thorough verification and simplify the process of modification.

The use of a breadboard enhances, rather than replaces, simulation, which remains an essential part of the design process. Simulation ensures that the gate array will perform the defined task properly, provided that the task is properly defined. Worst-case analysis and verification of critical timing paths require the use of simulation.

Simulation, however, has limitations of its own. It cannot yet thoroughly verify a design at the system level. This activity is still the domain of the engineer, and all engineers can make mistakes. What's more, simulation only answers what's asked of it, and it can only test a portion of a design. If you don't direct the simulation to look at the circuitry that contains an error, or that is malfunctioning because of an error elsewhere in the design, that error will go undetected. Also,



Because of schedule constraints, *the gate array in Data I/O's Unisite 40 universal programmer had to work the first time. Company engineers built this breadboard to prove the design of a gate array.*

the time required to test an entire design with a simulator is prohibitive, even with the accelerators now on the market. Finally, the simulation of multiple-feedback shift registers, such as pseudorandom binary sequencers and error-correction circuitry, is beyond the limits of to-

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day's computing power.

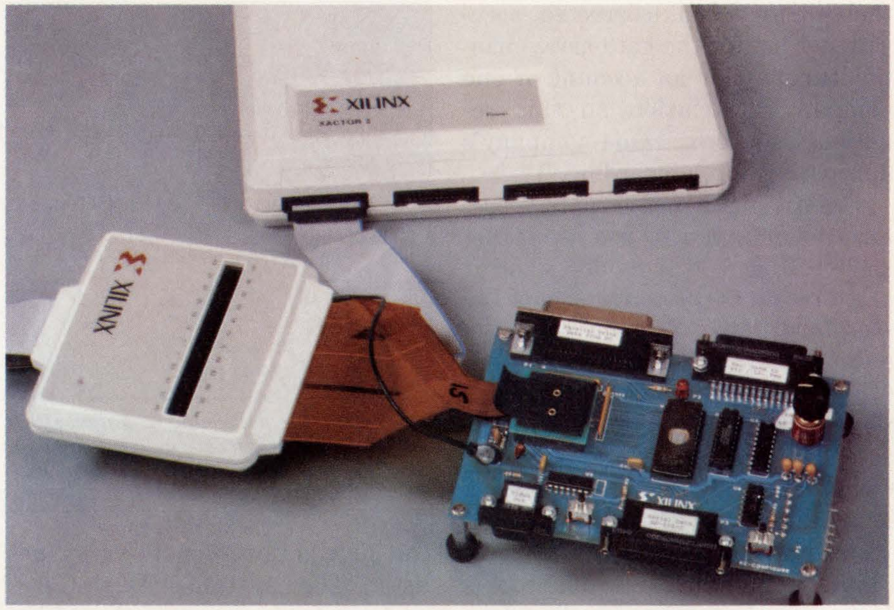
Some of the classic reasons for building a breadboard still apply, but there are also some very important benefits that did not exist in the past. The best known advantage to using a breadboard is the ability to test the design in the system and debug the logic in real time. If the board-level system that will incorporate your design must work with the unpredictable timing of asynchronous events, you can monitor its reaction to these stimuli. Another familiar advantage is the ability to test any existing software to ensure that the new design is compatible with a previous design.

When problems occur, you have access to all of the circuitry. Simple modifications take a very short time to effect, and then you can test the design again. Even if you must make major architectural changes, you can still use much of the breadboard.

A little known—but important—advantage to using a breadboard involves the generation of test vectors. The creation of test vectors is a time-consuming and tedious task, and it's very easy to make a simple error when you're dealing with ones and zeros. Yet without an accurate and comprehensive list of test vectors, it's difficult to verify the design with a simulator and test the resulting silicon samples from the first production run.

With the help of a logic analyzer and a word processor, you can use your breadboard to create your test vectors. The logic analyzer connects to the breadboard at the same places where the pins of the final gate array will be. As the system runs, the logic analyzer captures all of the generated patterns. You can then edit these test vectors with the word processor and render them into a form acceptable to the gate-array manufacturer. In effect, the system automatically, and accurately, creates the test vectors.

On a typical project you can't test the software until the hardware has



You can quickly test and modify a design *in an actual circuit, in real time, using Xilinx's XC-DS24 Xactor in-circuit emulator.*

been verified. If you don't build a breadboard, the software engineers will have to wait until the gate-array prototypes have returned from the foundry and have been tested in the system before they can exercise the software. If you do use a breadboard, the software engineers can begin their tests as soon as the breadboard is verified—significantly shortening the design-to-production schedule as a result. Obviously, test engineers also have access to the working system much sooner when you use a breadboard. You can even build more than one breadboard, so that all those needing the working system have simultaneous access to it.

You might also consider giving a system based on the breadboard to select customers for beta-site testing. Even though the system may not match the size or the speed of the production version of your design, you can derive valuable information by analyzing the response of the end user.

A breadboard will help streamline the process of iteration as well—a process whose importance is too frequently underestimated. Quite often management, the design community, and even engineers themselves expect to create a virtually perfect design at the start, but the reality couldn't be more different. A good design counts on the engineer's having an opportunity to test and optimize it repeatedly; a breadboard readily provides that opportunity.

The creation of a large breadboard is not an easy task. You should automate as much of the process as possible to minimize the possibility of human error. The use of PLDs or PROMs renders the number of components making up the breadboard more manageable, and available software packages help you gain mastery of breadboard-building techniques.

Most schematic-capture programs produce a net list that a number of companies can use to wire a breadboard automatically **(Ref 1).** You create the design and then send off the net list at the same time you purchase the necessary components. When you receive the completed wire-wrapped panel, you place the components on the panel. You then verify the design, and as you make changes, you update the schematic. Consequently, when you complete the testing, the final design already exists in a file. You then create a final, corrected, accurate net list for the gate-array manufacturer. (For an account of one company's variation on this sequence, see **box,** "One company's approach to breadboarding.")

The use of schematic-capture programs limits you to use of off-the-shelf SSI and MSI devices, and it often requires the conversion of the standard logic devices into the equivalent gate-array macros—another potential source of errors. Some gate-array vendors, however, are beginning to use standard TTL devices in their macro libraries, a practice which will smooth the conversion process.

One helpful breadboarding tool is FutureNet's Semicustom Development System, which runs on an IBM PC/AT with a 32-bit coprocessor board. The system helps you perform several tasks essential to the creation of digital circuitry, from design entry and simulation to the production of gate-array net lists. The system's Dash-Gates package lets you create the design using a functional description (the system allows schematic entry as well). After you've entered the design, you may either partition the design into multiple PLDs or send the net list directly to the gate-array manufacturer. If you're going to make a breadboard, you would elect the former alternative.

Form type: partition　　Form name: count

Partition: count
Inputs: 5　　Comb Outputs: 2 (2 w/feedback)　　Reg Outputs: 6 (6 w/feedback)
Total Pins Required: 13

Output Name:	Output Type:	Inputs Required:
count	Set	c0,c1,c2,c3,c_enable,clock, enable,up
up	Bidir	s0
c_enable	Bidir	s1
sreg	Set	c0,c1,c2,c3,clock,dir_up,enable, mode,pause,s0,s1

***Fig 1—When partitioning a design** with FutureNet's Dash-Gates, you enter the desired outputs, and the software automatically specifies the required inputs. The part required to perform this count function needs at least five inputs, two combinatorial outputs, six registered outputs, and 13 pins. A 16R6 or equivalent would work.*

The partitioning of the design is semiautomatic; you make many of the decisions. You survey the design and group sections that will most likely fit into a PLD, usually by separating pure logic from that which requires latches. Then you select outputs. Dash-Gates will determine the inputs required to create the selected outputs, and it will define the number of inputs and latches required **(Fig 1).** You then select the appropriate PLD and define the input and output pins. Dash-Gates then creates a file defining the PLD. This process repeats until you have converted as much of the design into PLDs as you desire.

Right now, the system will partition only functionally entered designs. In the near future, the system will be able to convert a schematic into a functional description and then partition that description. Also, the system does not yet provide a PLD interconnect diagram automatically, but the signal names on the PLDs will match. You can then make a net list for wire-wrapping the breadboard. Soon the interconnection of PLDs will be automated, and Dash-Gates will be able to create a net list that can be used to wire the breadboard.

Once you've proven the design information on the PLD-based

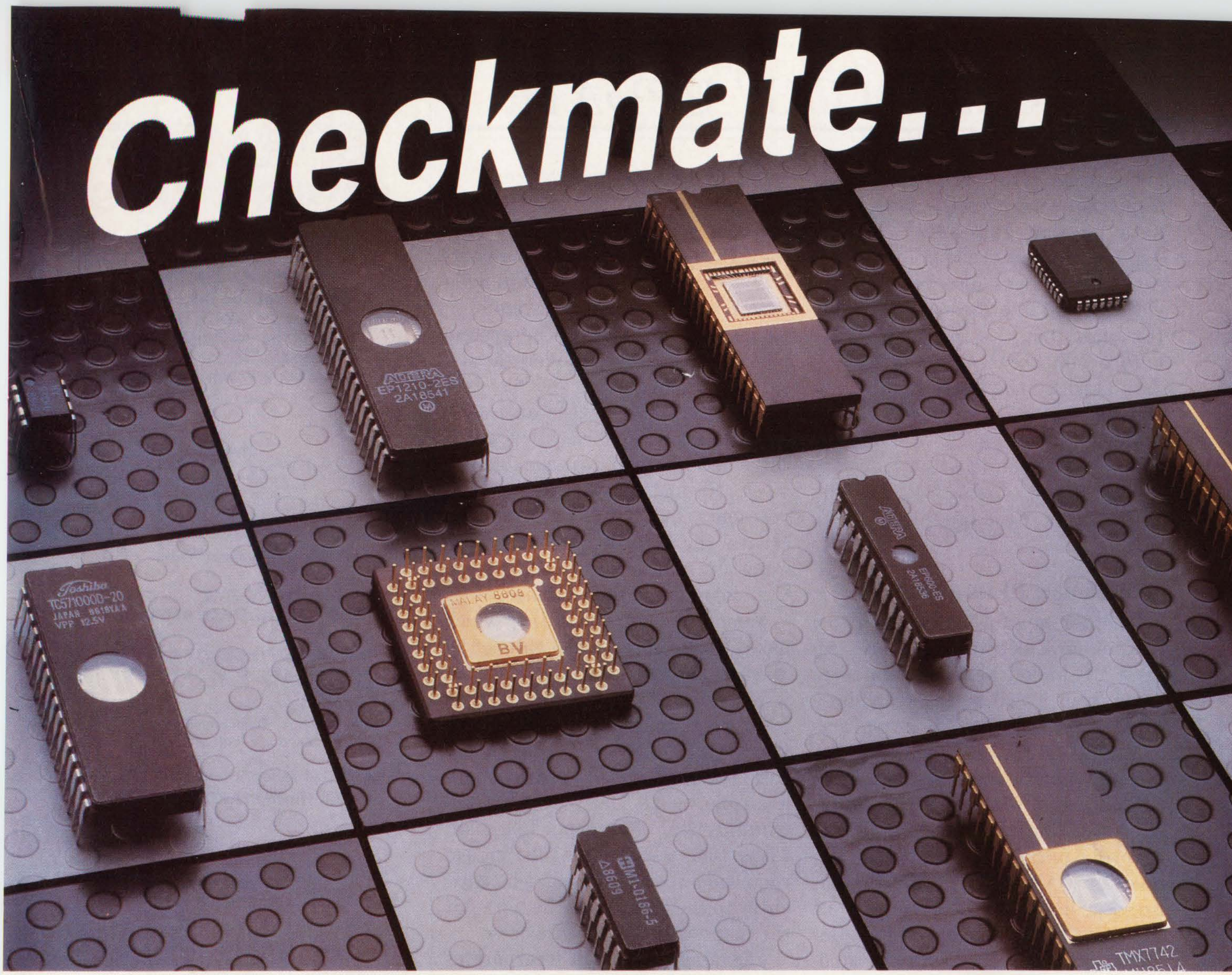
One company's approach to breadboarding

The approach to gate-array development used by Magnesys Inc (San Jose, CA), a producer of bubble-memory storage subsystems, is to use two breadboards for each gate-array design. This methodology requires a minimum of tools—an IBM PC, schematic-capture software, and a logic analyzer. It's not necessary to spend large sums of money on exotic equipment.

The engineers enter a design into a schematic-capture program, which creates a net list that an automated wire-wrapping service can use to build the first breadboard. The engineers then integrate this breadboard with the target system and debug the system until they're satisfied with its operation.

The updated schematics then undergo three types of treatment: They're sent to the wire-wrapping service, which creates the second breadboard; they're converted into the gate-array vendor's library; and they're given to someone else—another staff engineer, a consulting engineer, etc—for independent verification of the schematic translation. The design team then creates a vendor-compatible net list, as well as any other documentation the vendor requires.

When the second breadboard arrives, the design team again verifies the design in order to prove that the documentation is correct. A logic analyzer with an interface to a computer assists in the creation and editing of test patterns. The entire gate array is then simulated at the vendor's facility. The resulting documentation released to the gate-array vendor goes with a high degree of confidence on the part of the design team.



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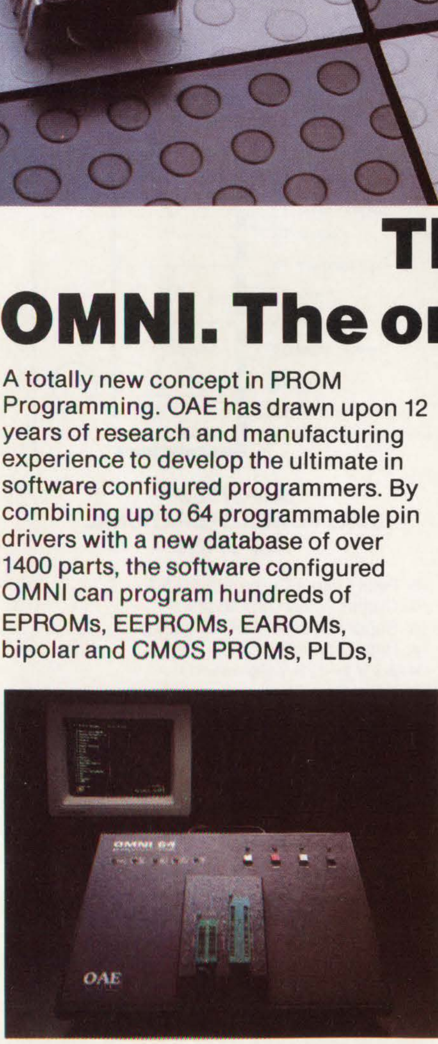

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breadboard, you use that same information to create the fabrication data for the gate-array vendor. Again, remember: If you incorporate any changes into your design, you must update the associated file. It's vital that the file be accurate before you create the fabrication data used by the gate-array manufacturer.

When purchased as a complete system, the Semicustom Development System costs $31,880. The Dash-Gates package alone costs $5500.

Your choice: PLDs or PROMs

Another helpful logic-design tool is Kontron Electronics' LOG/iC. An IBM PC-based version ranges in price from $3990 to $9280, while a VAX-based version costs as much as $23,280. LOG/iC lets you define the design with standard Boolean equations and truth tables; with a finite-state-machine syntax; or as one of several microprogrammable sequencers. After optimizing the entered design, you create an output file that defines registered PAL devices, gates for gate-array production, PLAs, or PROMs.

If you choose to use PAL devices, you initially place those designs that won't fit into a single device into a "hyper-PAL," which is a hypothetical device that has 32 inputs, 32 outputs, and 99 product terms. The information obtained from the description of the hyper-PAL will allow you to partition the design manually into multiple devices.

If you choose to use PLAs or PROMs, you enter the design into the LOG/iC system, which automatically converts the design into a file that will define the programming pattern of the device. The system will automatically partition the design into the devices you have selected. LOG/iC provides an extensive and growing library to simplify the selection of programmable devices. No matter what device type you use, the LOG/iC system will create the appropriate programming file and allow the file to be transferred to a programmer.

Monolithic Memories Inc, which has recently entered the gate-array market, has a software package that will convert multiple-PAL designs into gate arrays. MMI's $7500 Magik (MMI Advanced Gate Array Integration Kit) software tools are available on all Daisy systems, including the Personal Logician. These tools perform the full range of required functions, from schematic entry to the creation of the tapes for the manufacture of the devices.

The Magik package incorporates the PAL Integrator, which allows you to specify and include one or more devices into the gate array. Boolean equations used to design and program the devices are the input to the PAL Integrator. The program automatically converts the equations to an equivalent hierarchical macrocell and generates the associated schematic. Each device

For more information . . .

For more information on the hardware and software tools described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

FutureNet Corp
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Chatsworth, CA 91311
(818) 700-0691
Circle No 701

Kontron Electronics Inc
633 Clyde Ct
Mountain View, CA 94039
(415) 965-7020
Circle No 702

Monolithic Memories Inc
2175 Mission College Blvd
Santa Clara, CA 95050
(408) 970-9700
Circle No 703

Xilinx Inc
2069 Hamilton Ave
San Jose, CA 95125
(408) 559-7778
Circle No 704

has a separate schematic, which resides in a separate file. All of the devices to be used in a gate array are contained in a single directory that defines the entire gate array.

The PAL Integrator supports more than 60 of MMI's PAL device types. This measure of support allows you to create a design using PLDs and standard logic, test and verify the design in breadboard form, and then place the design into a gate array.

Emulators, superbreadboards

The ideal approach to gate-array development would be to retain the benefits of building a breadboard without actually building it: You would employ CAD tools to design the circuitry and simulate worst-case timing and racing conditions, monitor the operation of the gate array in the actual system in real time, and instantly modify the gate array where required. This approach would be possible if an available emulator could replicate the behavior of the gate array, allow the user to monitor all of the circuitry within the array, and facilitate modifications.

Coming very close to the ideal is Xilinx's development system for its logic-cell array **(Ref 2)**. The $3600 XC-DS21 design editor runs on an IBM PC/XT or PC/AT and provides a design environment for the development of an application using the logic-cell array. When you complete the design, you can download the data into the actual device directly from the PC, using the download cable provided and three pins of the device.

What gives the XC-DS21 its power and versatility, however, is the $6300 XC-DS24 Xactor in-circuit emulator, which allows you to test and modify a design quickly. You can evaluate the entire target system, including the logic-cell array's interaction with software and asynchronous events.

Once you've entered, simulated, and routed your design, you plug the Xactor into the target system and run the design in real time. At any time you can upload the internal state of the logic-cell array into the PC for analysis (by itself, the design editor does not allow uploading of files).

Depending on your design, you can use the editor and emulator to verify the target system and create a comprehensive list of test vectors by reading the internal state of the emulator after each step. Such a list proves useful when you want to place the design into a gate array and perform simulation and device testing.

Current Xilinx logic-cell arrays have 1200 or 1800 usable gates. An 8000-gate version should appear by the end of 1987.

Sometimes it's just not possible to build a breadboard. With many technologies, for example, there is a big difference between the speed of a discrete-IC version and that of its gate-array counterpart. At the upper limits of speed, the breadboard will be significantly slower than the final design. When the final system simply won't operate at a slower speed, the breadboard often isn't useful, because it can't keep up with the data coming in. Despite the existence of such cases, however, breadboarding remains viable for a sufficient number of designs to warrant your careful consideration.

EDN

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2. Wynn, Pardner, "In-Circuit Emulation for ASIC-Based Designs," *VLSI Systems Design*, October 1986, pg 38.
3. Crisafulli, Kelle, "A Pin-Logic Gate Array For a Programmable Logic Programmer," *VLSI Systems Design*, October 1986, pg. 30.

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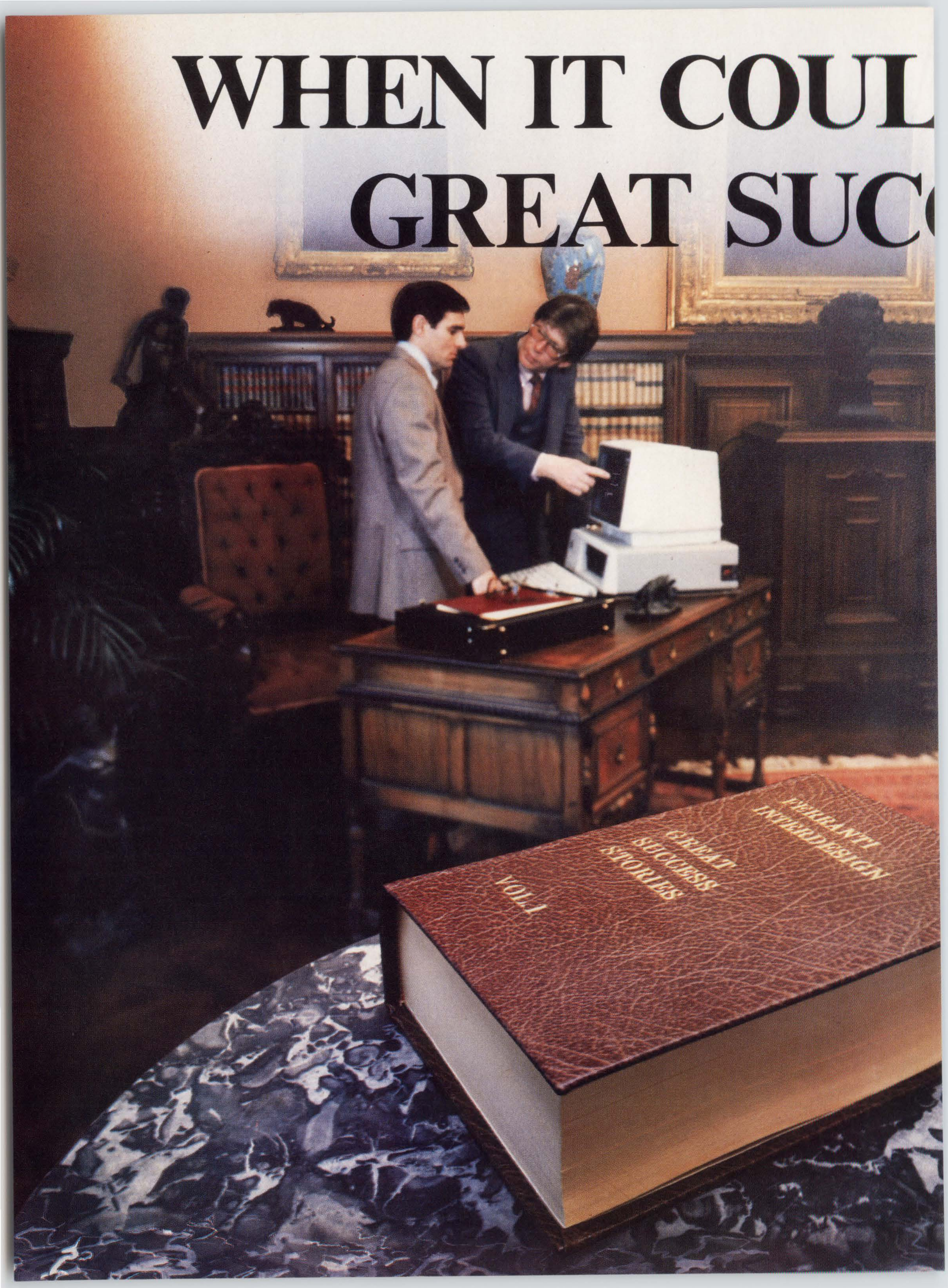

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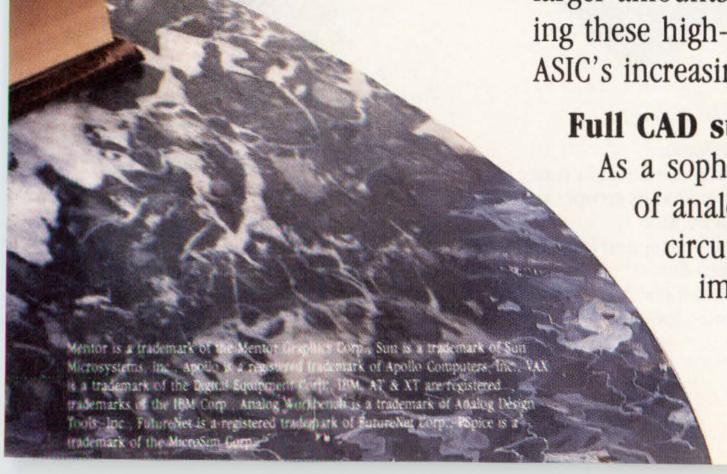

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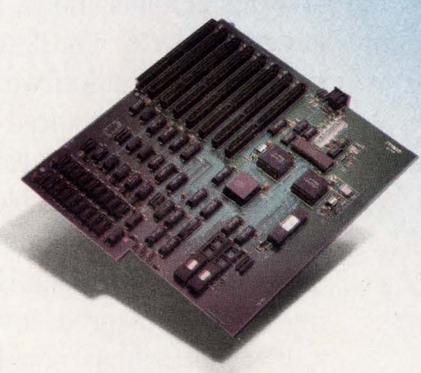

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8259A	Programmable Interrupt Controller
8284	Clock Generator
82284	Clock Generator and Ready Interface
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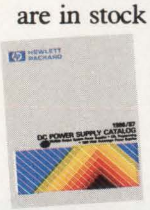

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CIRCLE NO 85

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Electro/87 and Mini/Micro Northeast programs will examine divergent topics

Tom Ormond, *Senior Editor*

The hallmark of this year's Electro and Mini/Micro Northeast conferences is its diversity. The theme of the professional programs is "Emerging Tools and Technologies for the Electronic Society of the Future"; you'll encounter numerous tutorials, sessions, and minitutorials pertaining to both. During the 36 sessions, speakers will present more than 150 papers (see **box**, "Information on programs and registration," pg 98).

Tutorials augment schedule

Electro/87 and Mini/Micro Northeast will run from April 7 to 9 at the Jacob Javits Convention Center in New York City. On Monday, the day preceding the formal start of the conferences, the IEEE Metropolitan Sections Activities Council and Electro/87 are co-sponsoring five tutorials. As of March 19, prices for the tutorials range from \$225 to \$355 (IEEE members) or \$280 to \$410 (nonmembers). These fees include course materials and lunch as well as show registration.

One tutorial, dealing with today's high-speed transmission systems, will discuss how telecommunications technology is moving metropolitan services into the digital realm in anticipation of the Integrated Digital Services Network (ISDN). This tutorial will have four speakers: One will talk about high-speed fiber-optic-based systems; another will discuss advances in fiber-optic technology; the third will identify how to use fiber-optic systems in LANs; and the fourth will offer specific applications as they relate to an end-user of high-speed services.

During the second tutorial, which will cover teleconferencing, you'll hear about the technical aspects of designing a teleconferencing system, including acoustics, echo cancellation, lighting, display technologies, equipment control, video-system design, audio-system design, and communication-system interfaces. Particular emphasis will be on image-data compression and satellite modem design.

The third tutorial will raise questions about monolithic microwave integrated circuits (MMICs), which are influencing traditional component-design techniques as they relate to communication, defense, and industrial applications. This session will address what MMICs mean to an engineer and how they might affect system designs.

The fourth tutorial will look at the history of radar, its present status, and its potential applications for the future. Equally applicable to new as well as experienced engineers, this tutorial will cover both technology and systems.

In the fifth tutorial, which is on μP architecture, you'll learn about ongoing research into reduced instruction set computers (RISCs). This meeting will analyze the prominent design issues pertaining to the RISC architecture.

Raise the Titanic

If you're planning to start off the conference at the keynote breakfast, scheduled from 9:00 to 10:30 AM on April 7 at the Marriott Marquis Hotel, you'll get a special treat: Dr Robert Ballard of the Woods Hole Oceanographic Institution in Massachusetts is the featured speaker. In addition to finding the Titanic, he has led or participated in over 50 deep-sea expeditions, and he has published 40 scientific articles.

Semicustom is on the agenda

Between April 7 and April 9, you'll have 36 professional programs from which to choose. Several sessions will concentrate on components such as gate arrays, PLDs, smart ICs, and LSI/VLSI parts. Other sessions will address advances in system architecture, logic, memory, processors, and number crunchers.

Still others will discuss custom and semicustom design centers, tools, and design-verification techniques, showing how they will have an impact on analog, digital, and communications systems. Sessions on computer languages, software-based systems, interface standards, manufacturing technologies (such as surface mounting), and the pros and cons of offshore vs domestic manufacturing and assembly are also scheduled.

One especially interesting session, on high-definition television, will include visual displays showing how to apply the technology to film, television, and printing. A minitutorial on computer-graphics video will present computer-generated 2- and 3-dimensional animated images as well as demonstrate shading and lighting effects.

Six additional minitutorials will deal with a variety of subjects. Some, for instance, will give broad overviews of emerging technologies such as computer graphics and optoelectronics. Others will review design guidelines for dealing with electromagnetic shielding and circuit stability.

Social issues on the docket

The professional programs at Electro and Mini/Micro Northeast won't neglect social issues, either. For example, you'll find sessions that will examine artificial intelligence and evaluate the chances of AI supporting (or supplanting) human thinking. A panel discussion will address ethical issues and ways to alleviate the conscientious engineer's susceptibility to criticism. You'll also have the chance to attend a session on the legal aspects of protectionism and another that addresses financial issues of interest to the new entrepreneur. **EDN**

Article Interest Quotient
(Circle One)
High 506 Medium 507 Low 508

Electro/87, Mini/Micro Northeast product highlights

More than 700 companies will be displaying their products at the Jacob Javits Convention Center. The brief product descriptions that follow hint at the diversity of the products you'll be able to see; for more detailed coverage, watch for EDN's March 31 issue.

Test and measurement instruments

The MW920A portable optical time-domain reflectometer from Anritsu (Oakland, NJ) features "EZ" keys that allow you to quickly select and set measurement conditions. The unit's 3-nsec pulse width virtually eliminates any dead zones, allowing you to locate fiber faults within 3m over distances of 40 km. You can store or recall as many as five sets of displayed data (including measurement conditions and fiber traces) in the MW920A's memory.

The SE 571 digital scope from BBC-Metrawatt/Goerz (Bloomfield, CO) simplifies the task of getting hard-copy output from a CRT: It has a built-in thermal printer that prints all the information from the CRT, complete with protocol of the information, within 10 sec. Equipped with two 25-MHz A/D converters, the SE 571 displays two signals (10 MHz max) via sine interpolation. For digital-circuit analysis, it provides as many as eight logic channels. Because of its almost-instantaneous printout capability, the scope also functions as an 8-channel logic recorder.

Keithley Instruments (Cleveland, OH) will introduce its Model 194, a programmable high-speed sampling voltmeter. Operating in the waveform-analyzer mode, it can digitize signals at sampling rates as high as 1 MHz with 8-bit resolution. Operating as a voltmeter, it has a high-resolution 16-bit (4½-digit) mode for sampling rates ranging to 100 kHz. It also has a wide dynamic range in the 16-bit mode: 10 μV to 200V. These capabilities reside in a full-rack system-voltmeter form factor.

Krohn-Hite Corp's (Avon, MA) Model 2100 synthesized-function pulse generator is an IEEE-488-compatible programmable instrument with a 0.01-Hz to 31.16-MHz frequency range, 0.00005% frequency accuracy, and 7-digit resolution. The 2100 includes nonvolatile memory that allows you to store and recall as many as 75 complete front-panel setups under either program or front-panel control.

The TA2000 from Gould (Cleveland, OH), an 8-channel thermal-array recorder, features a fixed array of thermal writing styluses that provides a recording width of 200 mm max with 8-dot/mm resolution. The unit's simple front panel provides immediate and convenient access to common recorder controls.

At its booth, Western Graphtec (Irvine, CA) will be displaying the TDA 3500, an 8-channel transient-data-acquisition system designed to capture and store high-frequency nonrepetitive data. The unit can operate in a stand-alone mode, in series with an oscillographic recorder, or in parallel with real-time recorders. Direct reading controls, conveniently grouped by function, eliminate the need to make calculations during setup and playback.

Integrated circuits

Amperex Electronic Corp's (Smithfield, RI) line of p-channel vertical DMOS FETs claim 4.5Ω drain-to-source on-resistance at a gate to source voltage of 10V, 4-nsec turn-on times, and maximum drain-to-source voltage ratings to −60V.

GE/RCA Solid State (Somerville, NJ) will present 8-bit R/2R ladder-type D/A converters for systems that run at video speeds. Two versions are available. The CA3338 specs integral and differential linearity errors of 1 and ¾ LSB, respectively, and the CA3338A guarantees ¾ and ½ LSB for the same parameters. Both types can operate at a typical digital-input update rate of 50 MHz.

Mitel Semiconductor's (Kanata, Ontario, Canada) MT8930, a complete S interface chip, conforms to CCITT I.430 recommendations for the ISDN's S and T reference points. The subscriber-network interface circuit operates from one 5V supply, is fabricated using low-power ISO^2 CMOS technology, and is available in a 28-pin DIP and PLCC.

Computers and peripherals

Applied Microsystems Corp (Redmond, WA) will display a high-speed SCSI interface option for its ES 1800 family of in-circuit emulators. The board will support the emulator-to-host interface electrically and logically in both the single-ended and differential modes. It'll also support bus arbitration, thereby allowing several initiators and targets to use the same physical bus.

The DVME-602R from GE/Datel (Mansfield, MA) is an intelligent analog input board specifically designed for RTD measurements in VME Bus-based systems. An internal RTD excitation current eliminates lead-resistance errors. The onboard μP linearizes and scales the digitized RTD values and outputs a binary quantity to the VME Bus host computer. You can select the binary value to directly represent a temperature value in either degrees Centigrade or Fahrenheit.

Information on programs and registration

Electro/87 will take place Tuesday, April 7 to Thursday, April 9, 1987, at the Jacob Javits Convention Center in New York City. Mini/Micro Northeast will run concurrently at the same location. This year, the Electro and Mini/Micro exhibits (and sessions) are under one roof. Over 700 exhibits will be on display from 10:00 AM to 6:00 PM on Tuesday and Wednesday and from 10:00 AM to 5:00 PM on Thursday.

If you register at the door, the cost for both conferences is $10 for IEEE members and $20 for nonmembers. This fee includes all Electro and Mini/Micro Northeast professional-program sessions and minitutorials, but not the tutorials held on Monday. Tickets to the keynote breakfast, which will be held Tuesday at 9:00 AM at the Marriott Marquis Hotel, are $20.

For more information, contact Electro-Mini/Micro Northeast, 8110 Airport Blvd, Los Angeles, CA 90045. Phone (213) 772-2965.

PROFESSIONAL-PROGRAM SESSIONS

DATE/TIME	ELECTRO	MINI/MICRO	MINITUTORIALS
APRIL 7 TUESDAY 10:00 AM TO 12:00 PM	SOCIAL IMPLICATIONS OF ARTIFICIAL INTELLIGENCE—SESSION 1	DESKTOP PUBLISHING BY ENGINEERS—SESSION 2	EVERYTHING YOU MIGHT NEED TO KNOW ABOUT METASTABILITY—SESSION 3
		MEMORY AND MEMORY SUPPORT—INNOVATIONS AND DEVELOPMENTS—SESSION 4	
1:30 PM TO 3:30 PM	SUPPORTING THE ETHICAL ENGINEER—SESSION 5	USING ADA IN REAL TIME APPLICATIONS—SESSION 6	GROUNDING AND SHIELDING ELECTRONIC INSTRUMENTATION—SESSION 8
		BUILDING NUMBER-CRUNCHERS WITH LSI DATA-PATH ELEMENTS I—SESSION 7	
4:30 PM TO 6:30 PM	TECHNOLOGY AND LAW—SESSION 9	RISCY BUSINESS—SESSION 10	
		BUILDING NUMBER-CRUNCHERS WITH LSI DATA-PATH ELEMENTS II—SESSION 11	
		CACHE MEMORY AND FIFO ARCHITECTURES FOR HIGH-PERFORMANCE COMPUTER SYSTEMS—SESSION 12	
APRIL 8 WEDNESDAY 10:00 AM TO 12:00 PM	AMERICAN MANUFACTURING: OUR COMPETITIVE EDGE—SESSION 13		FIBER OPTIC SENSOR TECHNOLOGY—SESSION 16
	ADVANTAGES OF ASIC DESIGN CENTERS—SESSION 14		
	ADVANCES IN CMOS STRUCTURAL SYSTEM DESIGN—SESSION 15		
1:30 PM TO 3:30 PM	OFFSHORE OPPORTUNITIES TO REDUCE COSTS AND EXPAND MARKETS INTERNATIONALLY—SESSION 17	NEW ALTERNATIVES IN USER PROGRAMMABLE LOGIC DEVICES—SESSION 19	CURRENT DIRECTIONS IN LIGHTWAVE COMPONENTS AND SYSTEMS—SESSION 20
	ANALOG DESIGN MADE EASY WITH CAE—SESSION 18		
4:30 PM TO 6:30 PM	ASSURING SUCCESS IN NEW VENTURES—SESSION 21	PROGRAMMABLE LOGIC FOR THE FUTURE—SESSION 23	OPTIMIZING SEMICUSTOM DESIGN—SESSION 22
	NEW APPLICATIONS FOR ELECTRO-OPTICAL COMPONENTS—SESSION 24		
APRIL 9 THURSDAY 10:00 AM TO 12:00 PM	DIGITAL SIGNAL PROCESSORS: PRODUCTS AND APPLICATIONS—SESSION 27	ADVANCES IN INNOVATIVE PLD ARCHITECTURE AND THEIR BENEFITS FOR SYSTEM DESIGN—SESSION 26	INTRODUCTION TO REALISTIC COMPUTER GRAPHICS—SESSION 25
		MULTIBUS II: THE MESSAGE PASSING COPROCESSOR (MPC) AND SYSTEM DESIGN—SESSION 28	
1:30 PM TO 3:30 PM	DESIGN AUTOMATION FOR INTEGRATED CIRCUITS—SESSION 30	NEW STANDARD DSP CHIPS ENHANCE TELECOMM DESIGN—SESSION 31	COMPUTER GRAPHICS FILM SHOW—SESSION 29
	SMART POWER IC's FOR MILITARY AND COMMERCIAL APPLICATIONS—SESSION 32		
4:30 PM TO 6:30 PM	HIGH DEFINITION TELEVISION APPLICATIONS—SESSION 33	COMPUTER AIDED TEST AND DESIGN VERIFICATION: A REVIEW OF CURRENT TECHNIQUES AND APPLICATIONS—SESSION 34	
	BEYOND SURFACE MOUNT: SILICON INTERCONNECT SYSTEM PROVIDES HIGHER DENSITIES AND IMPROVED PERFORMANCE—SESSION 36	HIGH SPEED PROGRAMMABLE LOGIC EASES NEXT GENERATION SYSTEM DESIGN—SESSION 35	

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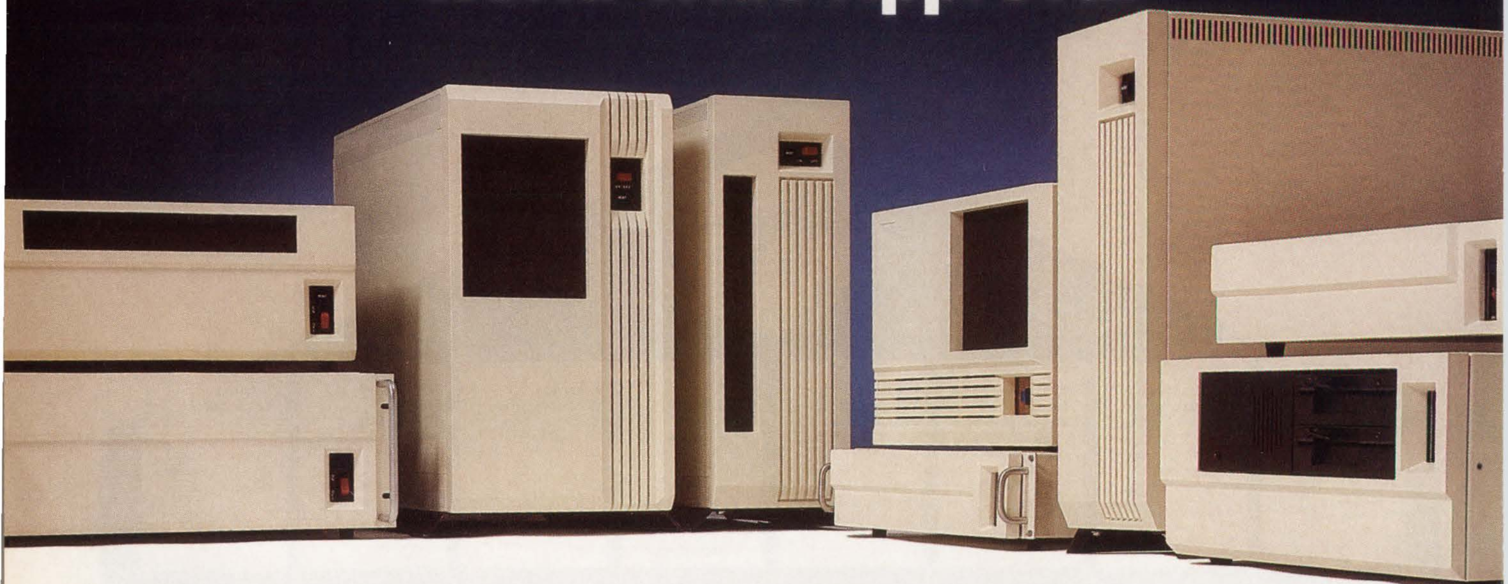

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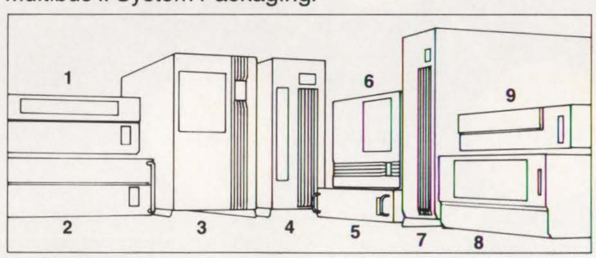

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   12 slots VME; 10 slots Multibus II; 15 slots Multibus I
4. Series 7 DeskMate
   5 slots VME, Multibus II; 7 slots Multibus I
5. Series 3 (shown with rack mounting)
   3 slots VME, Multibus II; 4 slots Multibus I
6. Series 10 with 4 full- /8 half-height peripherals
   12 slots VME; 10 slots Multibus II; 15 slots Multibus I
7. Series 7 DeskMate
   7 slots VME, Multibus II; 10 slots Multibus I
8. Series 7 with 2 full- /4 half-height peripherals
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CIRCLE NO 143

An 80386 µP and two operating systems enhance PC-compatible CAE workstation

CAE applications run two to three times as fast on the Personal Logician 386 as they do on the vendor's IBM PC/AT-based Personal Logician 286. As their names imply, the Personal Logician 286 uses Intel's 80286 µP in its CPU; the Personal Logician 386 uses the 80386 µP.

Although the Personal Logician 386 runs faster than a PC/AT, the 80386-based system provides PC compatibility. The workstation uses the IBM PC/AT bus and runs MS-DOS.

The system includes a 16-MHz 80386 µP; 2.5M bytes of RAM; a 44M-byte hard-disk drive; an 80287 coprocessor; Enhanced Graphics Adapter (EGA) graphics; and a 13-in., 640×350-pixel monitor. To improve your display, you can add either a 15-in. or a 19-in. color monitor to the Personal Logician 386. The optional monitors both spec 1024×824-pixel resolution.

The Personal Logician 386 isn't just a faster PC—it also runs the company's CAE and CAD software. Further, you can connect design-automation hardware, such as the PMX hardware modeler, to the personal computer.

Because MS-DOS can address only 640k bytes of memory, the company's CAE and CAD software doesn't run under MS-DOS. Instead, the design-automation programs run under the DNIX operating system, which is the company's implementation of Unix. This multitasking operating system features multiple display windows, expandable memory, and virtual memory.

The standard DNIX package includes a schematic editor, a design compiler, a text editor, and a net-list extraction program. You can add logic simulation, analog simulation, and test analysis to the package. Other software available for the workstation includes layout tools for gate arrays, pc boards, and custom ICs. Note, however, that the 386-based PC can't run all of the company's software. You must transfer IC-layout-verification and pc-board-routing tasks to a DEC VAX or to the company's Logician computer.

The Logician, which also now includes an 80386 µP, runs all of the company's CAE and CAD programs, but doesn't run MS-DOS software. The Logician features design and layout software; a 19-in., 1024×832-pixel color monitor; a graphics controller; 85M bytes of hard-disk memory; and 4M bytes of RAM. You can expand the RAM to 16M bytes and the hard-disk memory to 1.2G bytes. Including IC-layout software, the Logician 386 costs \$85,000. The Personal Logician starts at \$20,000.—***Eva Freeman***

Daisy Systems Corp, Box 7006, Mountain View, CA 94039. Phone (415) 960-0123. TLX 858262.

Circle No 729

To increase the speed of programs running under the DNIX and MS-DOS operating systems, *the Personal Logician 386 incorporates an 80386 µP. Electronic-design applications run on the workstation under DNIX; all other programs, including office-automation software, run on the system under MS-DOS.*

Single-chip data-acquisition system performs many of the tasks of a μP

The ML2200 low-power CMOS chip includes a 13-bit A/D converter (12 bits plus sign), a 4-channel differential multiplexer, a programmable-gain instrumentation amplifier, an S/H amplifier, a voltage reference, and a digital-control section that can perform many data-acquisition tasks.

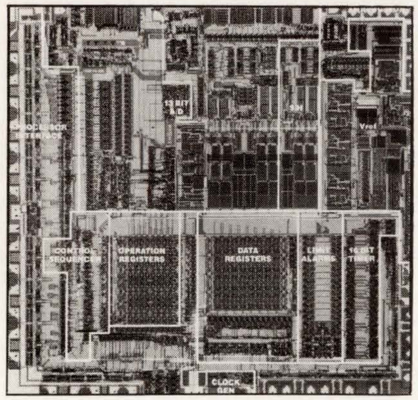
The 13-bit A/D converter is a self-calibrating design that doesn't require any external trimming devices. It converts 13 bits at 40 kHz max and eight bits at 50 kHz max. At a 13-bit resolution, the converter's integral and differential nonlinearity spec of ±½ LSB is guaranteed over temperature, power-supply range, and product aging.

Each of the four inputs is differential, providing high noise immunity. Any one of the channels can be used as a reference for an A/D conversion, so you can perform ratiometric measurements.

The programmable gain amplifier (PGA) is inherent in the A/D-conversion scheme. It allows a gain of 1, 2, 4, or 8. The instrumentation-amplifier offsets are nulled to less than ¼ LSB prior to the start of sampling.

The internal bandgap reference is accurate to 2.5V±2 mV. The temperature coefficient of the reference is 50 ppm/°C from 0 to 70°C. The reference also includes an output that is directly proportional to the temperature of the chip.

The digital-control section consists of a programmable sequencer, a double 8-word buffer, limit alarms, a 16-bit counter, and a μP interface. The ML2200 can easily handle certain tasks that are normally handled by the μP, so it can offload the μP of much of the overhead associated with data acquisition.



Because its 13-bit A/D converter takes up very little real estate, *the entire ML2200 can exist on a single chip.*

When initializing the system, the μP programs the sequencer by loading the on-chip instruction RAM and control registers. The 8-step sequencer contains eight words of 16 bits each. Each word is divided into seven different fields: reference selection, gain, 8- or 13-bit conversion, channel number, trigger source, limit-alarm activation, and an indicator that shows whether an operation is the last one in the sequence.

To see how the chip can benefit your system applications, consider a system with four sensors, each having different gain requirements. Three of the sensors are used as variables in a calculation for control of the system. The fourth sensor must be monitored continuously; if the measured value exceeds its preset limits, the system must shut down quickly.

In a conventional A/D system, the μP has to set the multiplexer, set the gain, start the conversion, and read the result for each channel. When the alarm channel is acquired, the value must be compared to a maximum value. If the maximum has been exceeded, the μP must execute the shutdown procedure.

In a similar system that uses an ML2200, however, the μP only needs to initialize the ML2200 and read the acquired data from the data buffer. If the alarm channel exceeds the preset limit, an interrupt can be generated, so the μP can handle the alarm condition quickly. The reduction in μP overhead is considerable, and the system using the ML2200 responds to the alarm condition much more quickly than would a system using the conventional approach.

The ML2200 Exerciser can aid you in using and understanding the ML2200. The Exerciser is an ML2200 on a pc board that interfaces to an IBM PC. This development system allows full access to all of the ML2200's registers and provides full-speed operation and full data-capture facilities. The software included in the package provides the means to control the ML2200. It allows you to store acquired data in a 20k-word buffer and to display the data either graphically or in table form.

The ML2200 costs $60 (1000). Samples are available now; the manufacturer expects to begin production in the third quarter of 1987.

— David Shear

Micro Linear, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 262-2095. TLX 275906.

Circle No 725

PC-board-manufacturing workstation integrates design, test, and fabrication

By transmitting the pc-board layout of a design to the CDX-60000S manufacturing workstation, you can adapt your design to fit your production requirements. Instead of stepping and repeating a photoplot, you step and repeat a layout on the workstation's screen.

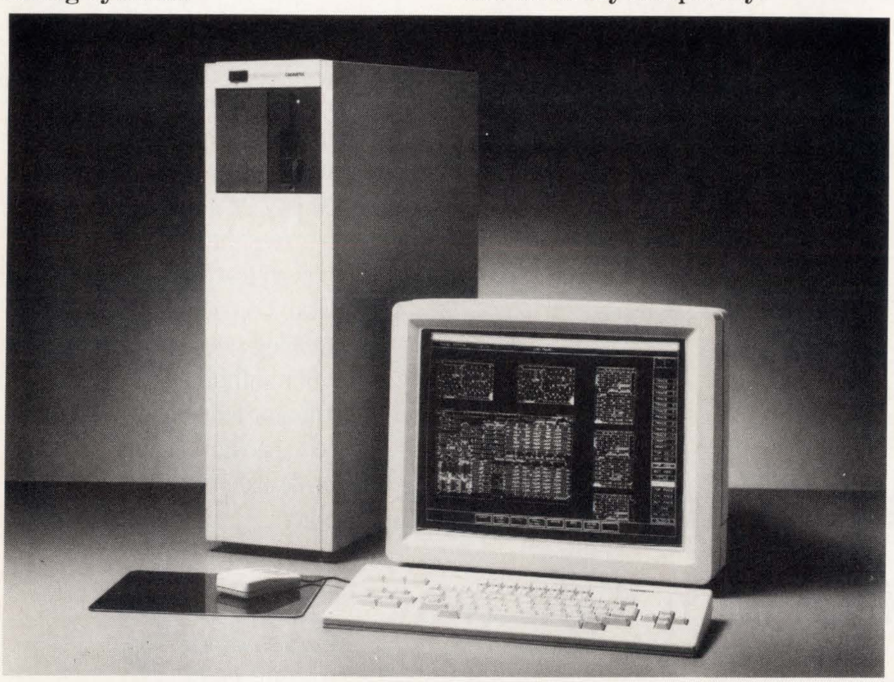
Because pc-board manufacturers make boards in large panels, which contain many copies of one board, you can't use just one copy of a layout for production. You must step and repeat the layout across the panel.

If all production equipment were perfect, stepping and repeating a photoplot would produce perfect pc boards. But stepping and repeating a photoplot requires accurate registration on all layers of a board. Furthermore, you can't make a photoplot compensate for the etching peculiarities of individual manufacturing systems.

The workstation's ability to process net-list data also lets it develop test vectors for production tests. Bare-board testers can use the files in the manufacturing workstation to simulate a complete panel.

When you're designing and assembling your boards at different sites, you can use the workstation's database to generate assembly instructions. The system also creates complete bills of materials for panels.

The CDX-60000S workstation improves the fabrication yield of pc boards because it lets you change manufacturing parameters interactively. You can, for example, shave pads, change trace widths, alter pad sizes, adjust drill-hole sizes, or add copper areas. The system has as many as 24 trace layers, 24 drafting layers, and 12 layers for silkscreen and outlines, so you can produce boards of any complexity.



This screen shot combines two pc-board layouts. *The CDX-60000S has placed one large design and several copies of a smaller design on a single panel.*

The manufacturing workstation can write fabrication instructions for most production equipment, such as photoplotters, N/C drillers, profile routers, autoinsertion tools, and pick-and-place systems. If the manufacturing workstation can't write an instruction set for a particular fabrication system, you can use the workstation's database query language to create an instruction file for that system. Using the database query language, you can specify drill, shape, pad, via, insertion, and test instructions. The workstation can then convert the instructions to any format.

You can enter design data from the vendor's CAD workstations or from Racal-Redac (Westford, MA), Scientific Calculations (Fishers, NY), and Computervision (Bedford, MA) systems. You can also enter photoplotter data, although you can't derive a net list from the graphical data that a photoplotter uses.

The CDX-60000S manufacturing workstation is a 68020-based color workstation. The system comes with 8M bytes of RAM (which you can increase to 12M bytes), the database query language, an asynchronous communications link, and a set of standard design postprocessors. $119,900.—***Eva Freeman***

Cadnetix Corp, 5757 Central Ave, Boulder, CO 80301. Phone (303) 444-8075.

Circle No 730

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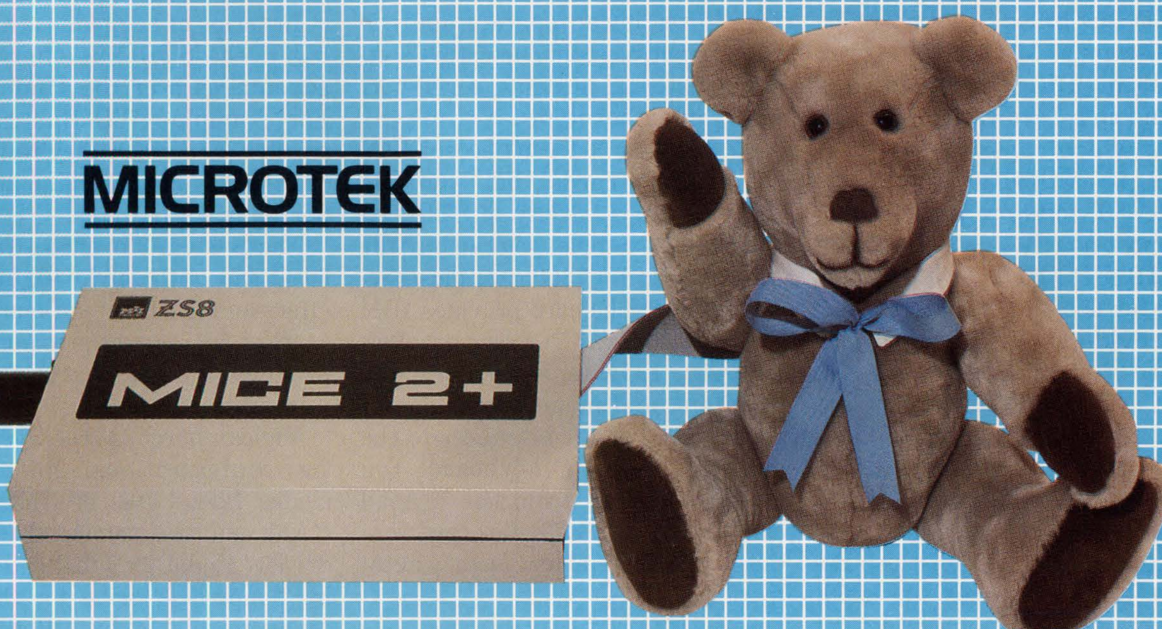

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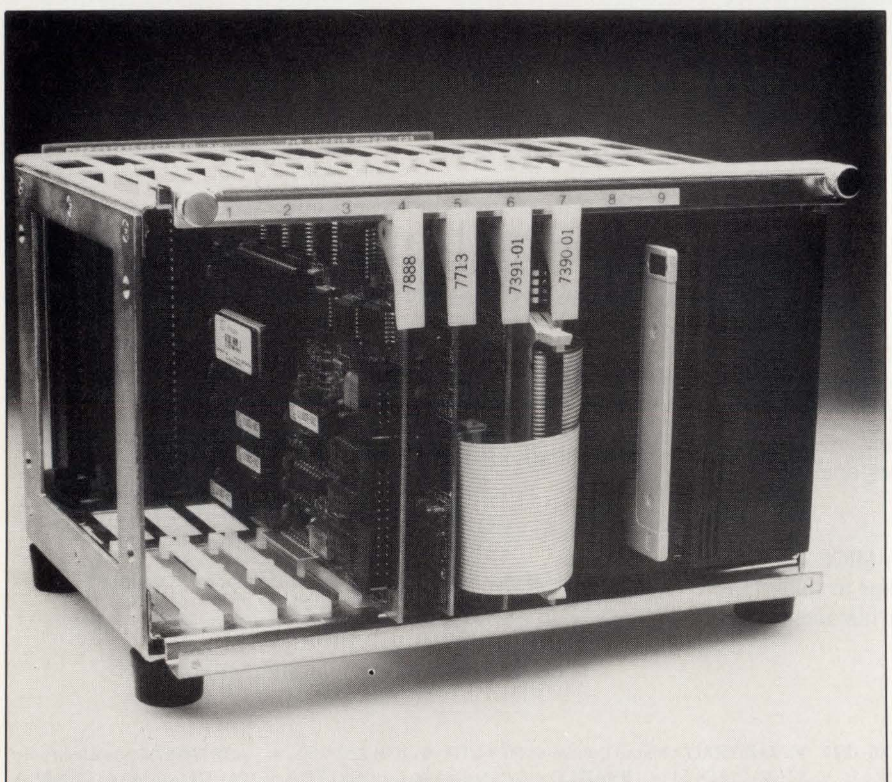
STD Bus-based IBM PC-compatible system suits industrial automation applications

The STD Bus-based System 2 offers IBM PC compatibility at the operating system, BIOS (basic I/O system), and chip-hardware levels. The system, which runs MS-DOS version 3.2, is as compatible with the IBM PC/XT software environment as are most non-IBM systems based on the IBM PC bus, yet it's rugged enough for use on the factory floor.

To provide extensive hardware/software compatibility with the IBM PC/XT, the System 2 employs a serial port implemented with an 8250 UART. Some communication software written for the IBM PC will work only with an 8250 UART or an exact compatible. Because the System 2 incorporates an 8250, therefore, it can operate all IBM PC-compatible communication software, external modems, serial-port mice, and other items.

The System 2 doesn't accept IBM PC plug-in cards, but you can choose from a variety of STD Bus cards. For example, you can buy the optional Model 7350 graphics/keyboard card. The card provides IBM PC-compatible CGA (color graphics adapter), EGA (enhanced graphics adapter), and monochrome operating modes, and it interfaces to the standard IBM PC keyboard. You can also choose from the myriad cards offered by STD Bus card vendors for industrial and factory automation.



Providing operating-system, BIOS, and chip-hardware-level compatibility *with the IBM PC/XT, the System 2 STD Bus-based computer runs almost all IBM PC/XT-compatible application software. The computer also accepts a card that emulates the IBM PC CGA, EGA, and monochrome display-adapter cards.*

In terms of ruggedness and reliability, the STD Bus offers several advantages over the IBM PC bus. For example, STD Bus cards are smaller, and when they're in a card cage, they're mechanically supported on three sides.

The System 2 operates from 0 to 60°C and withstands 10g shock. It offers an MTBF rate of more than 5 years at 55°C, and the manufacturer provides a 5-year parts and labor warranty.

You can purchase the System 2 in two configurations. Model 10 includes 128k bytes of CMOS static RAM and two semiconductor disk drives. Model 20 substitutes a 3½-in. floppy-disk drive for the semiconductor disk drives. Both models have 128k bytes of CMOS static RAM that's expandable to 640k bytes. You can add an additional floppy-disk drive or 20M-byte Winchester drive to both models. The systems employ an NEC V20 μP and include a clock/calendar chip.

For software support, you can purchase the vendor's STD-LIB 2.0 software library. The library provides initialization and driver routines for 22 STD Bus cards. The routines link to programs written in Microsoft C, Basic, or assembler languages. Other optional packages include software for prototyping and communications. Model 10 costs $1195, and Model 20 sells for $1595. The 7350 graphics/keyboard card is $565.—***Maury Wright***

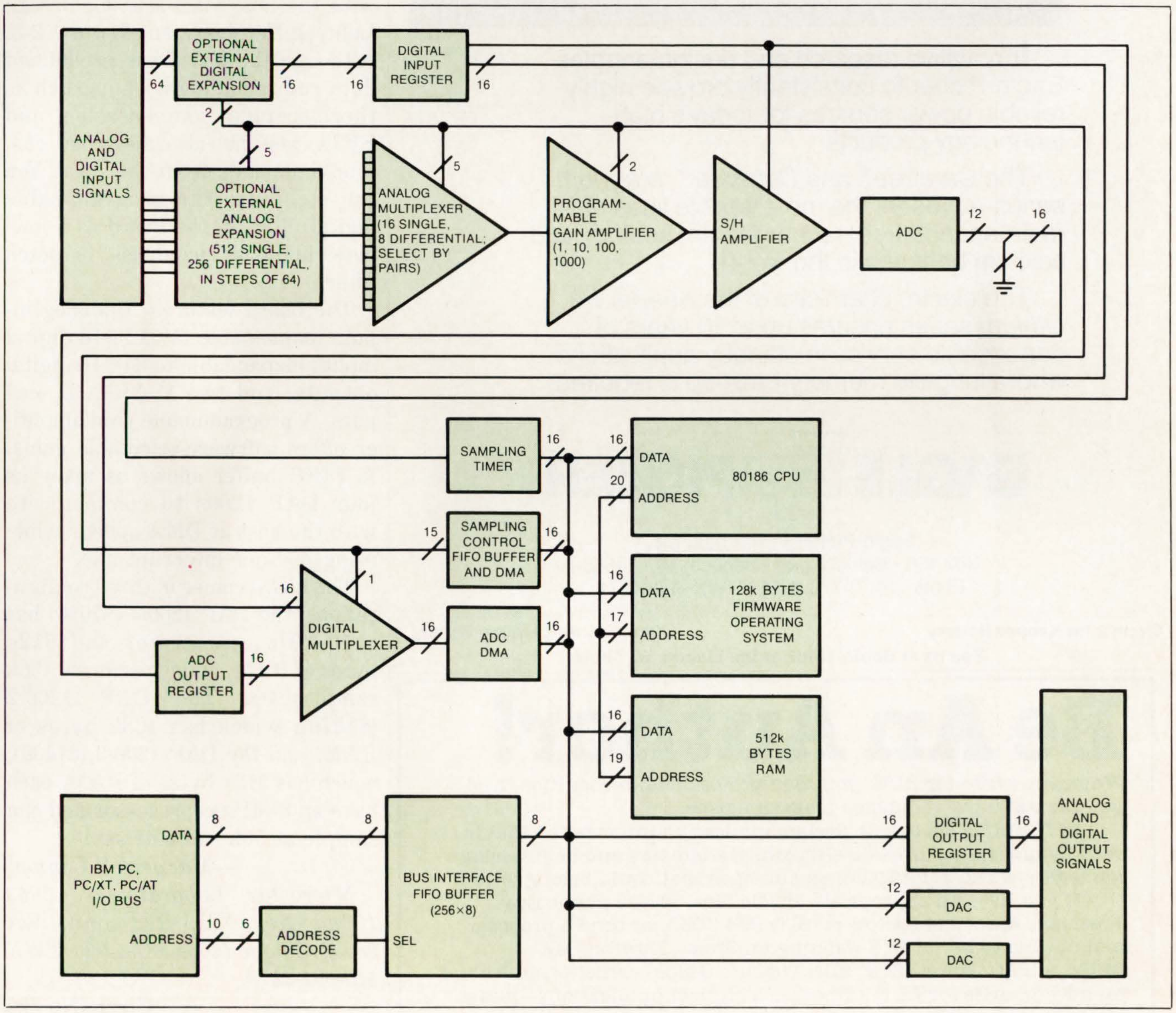
Pro-Log Corp, 2560 Garden Rd, Monterey, CA 93940. Phone (408) 372-4593. TWX 910-360-7082.

Circle No 731

80186-based data-acquisition board provides onboard signal processing

The DAP 1200 board can digitize and process analog signals in real time prior to passing them to a host IBM PC or compatible computer for storage or additional processing. Nonintelligent data-acquisition boards that pass large quantities of unrefined data to the host can exceed both the host's real-time processing capability and its storage capability. For example, acquiring 12 bits of data at 156 kHz for 64 sec will fill a 20M-byte disk. But because the DAP 1200 has an onboard 80186 coprocessor, it lets you perform calculations such as FFTs, cross-correlations, and signal averaging on the data before it goes to the host, so you can pass only reduced data to the host.

In addition, the coprocessor also supports both hardware and software triggering. Triggers are special events, observed or computed from acquired data, that signal the coprocessor when to begin processing. You use triggers to select



The ROM-resident multitasking operating system *of the DAP 1200/4 data-acquisition board allows tasks to communicate through Unix-like pipes. The board features 12-bit A/D conversion at rates as high as 156k samples/sec.*

the data that the board will process. Because the DAP 1200 buffers data after it's acquired, the board can both pretrigger and posttrigger on events.

The board has a ROM-resident, real-time, multitasking operating system that apportions local resources such as hardware, memory, and data buffers among the various tasks. The tasks communicate by passing data through Unix-like pipes. You configure the operating environment by means of the manufacturer's proprietary high-level language, DAPL.

The DAP 1200 communicates with the host via Basic, C, Pascal, Labtech Notebook, and Lotus 1-2-3. Although the board has predefined data-reduction algorithms such as thermocouple compensation and FFTs, you can also download custom commands from the host. You can configure the programmable digital filter on the board as a lowpass, highpass, bandpass, or notch filter.

The board features 16 analog inputs (expandable to 512), 16 digital inputs (expandable to 64), 16 digital outputs, and two 12-bit A/D outputs. A programmable gain amplifier offers software-selectable gains. A FIFO buffer allows as many as four DAP 1200s to communicate with the host at DMA speeds while using just one interrupt line.

The board comes in three configurations: the DAP 1200/4 ($1596) has a 10-MHz coprocessor and 512k bytes of RAM, and it performs 156k samples/sec. The DAP 1200/2 ($1276), which has 128k bytes of RAM, and the DAP 1200/3 ($1436), which has 512k bytes of RAM, each have an 8-MHz coprocessor and can sample at 50k samples/sec.

—Margery S Conner

Microstar Laboratories, 2863 152nd Ave NE, Redmond, WA 98052. Phone (206) 881-4286. TWX 510-601-3473.

Circle No 726

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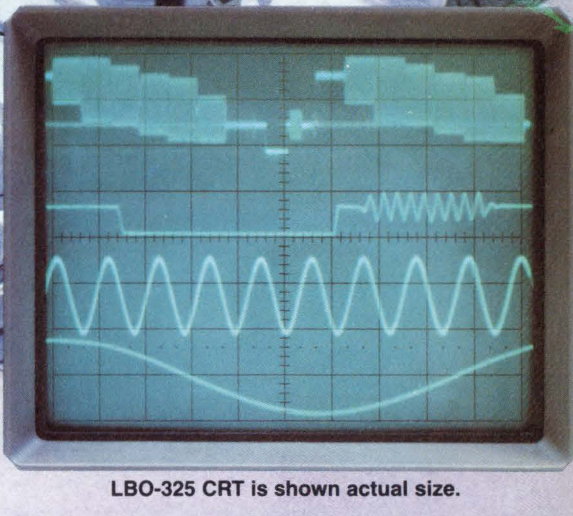

LBO-325 CRT is shown actual size.

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Circle 42 for product information

Circle 3 for product demonstration

Digital meter interfaces directly to thermocouples

The PM-5050 may change the way you think about and use digital panel meters (DPMs). The unit, which fits into a one-eighth-size DIN panel cutout, connects directly to thermocouple types B, E, J, K, N, R, S, and T. The meter's internal circuitry filters, amplifies, and converts the thermocouple's voltage to a direct temperature readout in units of °C or °F. You can choose a resolution of either 1° or 0.1° for the 5-digit display. The meter measures temperatures accurately over the entire ANSI-specified temperature range for each thermocouple type. It also provides cold-junction compensation.

Besides measuring temperature, the meter controls four independent setpoints, each of which activates a MOSFET. Each optically isolated MOSFET switches as much as 100 mA at as much as 300V. The setpoint outputs let you control alarms, heater relays, and other electrical devices. The setpoint switches are individually programmable for temperatures that go either above or below a limit you set. The setpoint hysteresis is selectable in 1° steps from 1° to as much as 25°.

Four front-panel membrane switches let you select options from an extensive menu that scrolls through the meter's alphanumeric display. Menu items let you establish setpoint temperatures, set a hysteresis value, test the meter, and control its RS-232C port. Internal nonvolatile RAM stores the menu selections when the meter is not powered.

The internal RS-232C port lets you connect the meter to a remote computer system. As many as 50 ASCII commands let you remotely control the meter's functions and acquire data from the meter. Because you can set each meter to respond to a 2-digit identification code, as many as 100 meters can connect to one RS-232C port on your computer. The meter provides three levels of security so that people have limited access to the meter's menus from the front panel. However, communications through the unit's RS-232C port give you control over all of the functions at all times.

The PM-5050 digital panel meter displays temperature readings *in °C or °F. The meter connects directly to thermocouples, and it provides internal cold-junction compensation.*

The meter measures 3.622×1.771×5.47 in. and weighs 567g. Available models operate on 115V, 230V, or 100V ac, or 5V dc. They consume less than 4W under normal operation. Options include an analog output that furnishes either a 4- to 20-mA or a 0 to 10V dc output. You can preset the temperature range that will correspond to the full-scale current or voltage output. The PM-5050 costs $395. The optional analog output costs $65; you must order it with the basic meter.—***Jon Titus***

GE Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. TLX 951340.

Circle No 732

Low-cost trackball offers 3-D I/O control for CAE

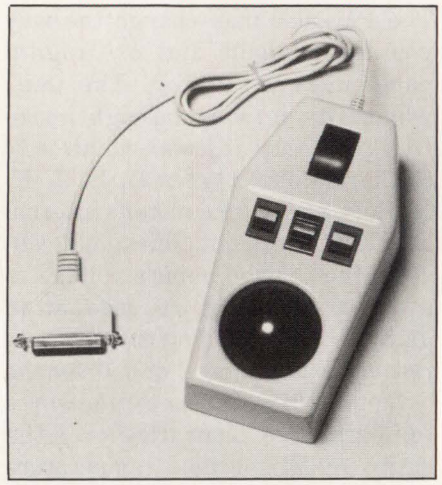
When you're working with 3-dimensional images on your CRT, you can use the FastTrap pointing device to inject X-, Y-, and Z-axis data directly into a variety of application programs. The FastTrap is a 3-axis I/O device that provides you with the stability and resolution of a trackball but costs only $149.

Unlike mice, which require a minimum of 60 in^2 of desk space to operate, FastTrap occupies only 18 in^2. In addition, FastTrap doesn't require a special work-surface texture and isn't as sensitive to dust as a mouse is. The pointing device also eliminates the jitter that mice often cause in high-resolution applications.

Each unit houses a 200-pulse/in. trackball for X- and Y-axis input and a 200-pulse/in. fingerwheel for Z-axis input. Most mice offer only half this resolution, and none provide Z-axis input. The FastTrap device emits pulses to indicate motion in each axis; your application software interprets the trackball movements to change the position of the screen cursor.

FastTrap plugs into the serial port of any IBM PC or compatible computer via its RS-232C interface. The device comes with an MS-DOS/PC-DOS software driver for ease of installation. To provide compatibility with existing software, FastTrap includes hardware emulation of mouse controllers. Three buttons enable you to make menu selections, and you can adjust the tracking drag to suit your application.

FastTrap's tracking surface provides a high degree of stability in high-resolution graphics applications. Certain CAE/CAD software packages, such as AutoCAD, currently offer 3-dimensional capability, but with an ordinary mouse or trackball you'd have to enter all Z-axis information from the keyboard. By integrating a FastTrap device in your CAE/CAD system, however, you can enter the Z-axis information with the pointing device, thus enhancing the functionality of your 3-dimensional software.



***Providing 3-dimensional cursor control** at a resolution of 200 pulses/in., the FastTrap pointing device plugs into the serial port of any IBM PC or compatible computer via its RS-232C interface.*

To aid software developers who want to use FastTrap's features in their programs, the manufacturer will furnish applications information, complete product data, and source code.—***J D Mosley***

MicroSpeed Inc, 5307 Randall Pl, Fremont, CA 94538. Phone (800) 232-7888 or (415) 490-1403.

Circle No 728

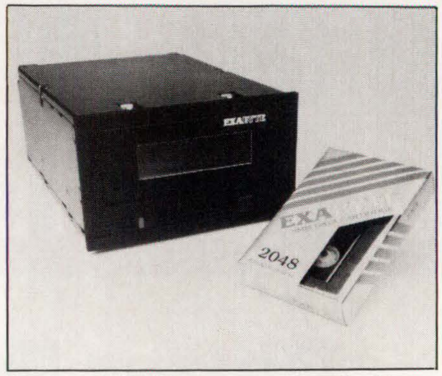
Tape drive stores 2G bytes in a 5¼-in. form factor

Employing high-volume, consumer videotape technology, the EXB-8200 cartridge-tape subsystem stores 2.332G bytes on a 360-ft, 8-mm videotape cartridge. The subsystem includes the tape drive, controller electronics, a 256k-byte data buffer, and an embedded SCSI interface in an industry-standard, full-height, 5¼-in. form factor.

Although the actual tape speed is a leisurely 0.429 ips (allowing for very gentle tape handling), the subsystem's helical-scan record-and-playback drum rotates at 1800 rpm, creating an effective head-to-tape speed of 150 ips. The recording head places tracks diagonally on the tape, storing 8k bytes per track at a density of 819 tpi. The drive achieves an area recording density of 35M bits/in^2.

Reed-Solomon product-code error correction and extensive error-recovery procedures give this storage peripheral a nonrecoverable error rate of less than one error per 10^{13} bits read. The subsystem's separate read and write heads allow for read-after-write verification. If a 1k-bit block within an 8k-bit track produces a verification failure, that block is rerecorded on a subsequent track; the subsystem handles recording errors on the fly, without stopping or reversing tape motion.

The subsystem sustains a continuous transfer rate of 246k bytes/sec over the SCSI interface, and the internal 256k-byte data buffer allows for a burst-transfer rate of 1.5M bytes/sec. The peripheral supports ANSI version 17B, conformance level 2, of the SCSI specification for sequential-access devices. It also provides full disconnect, arbitration, and reconnect functions. Because it includes the data buffer, the drive can simulate start/stop tape operation by fulfilling data requests directly from buffer storage instead of tape, as long as the desired information is in the buffer. The data-buffer-access time is 400 μsec.



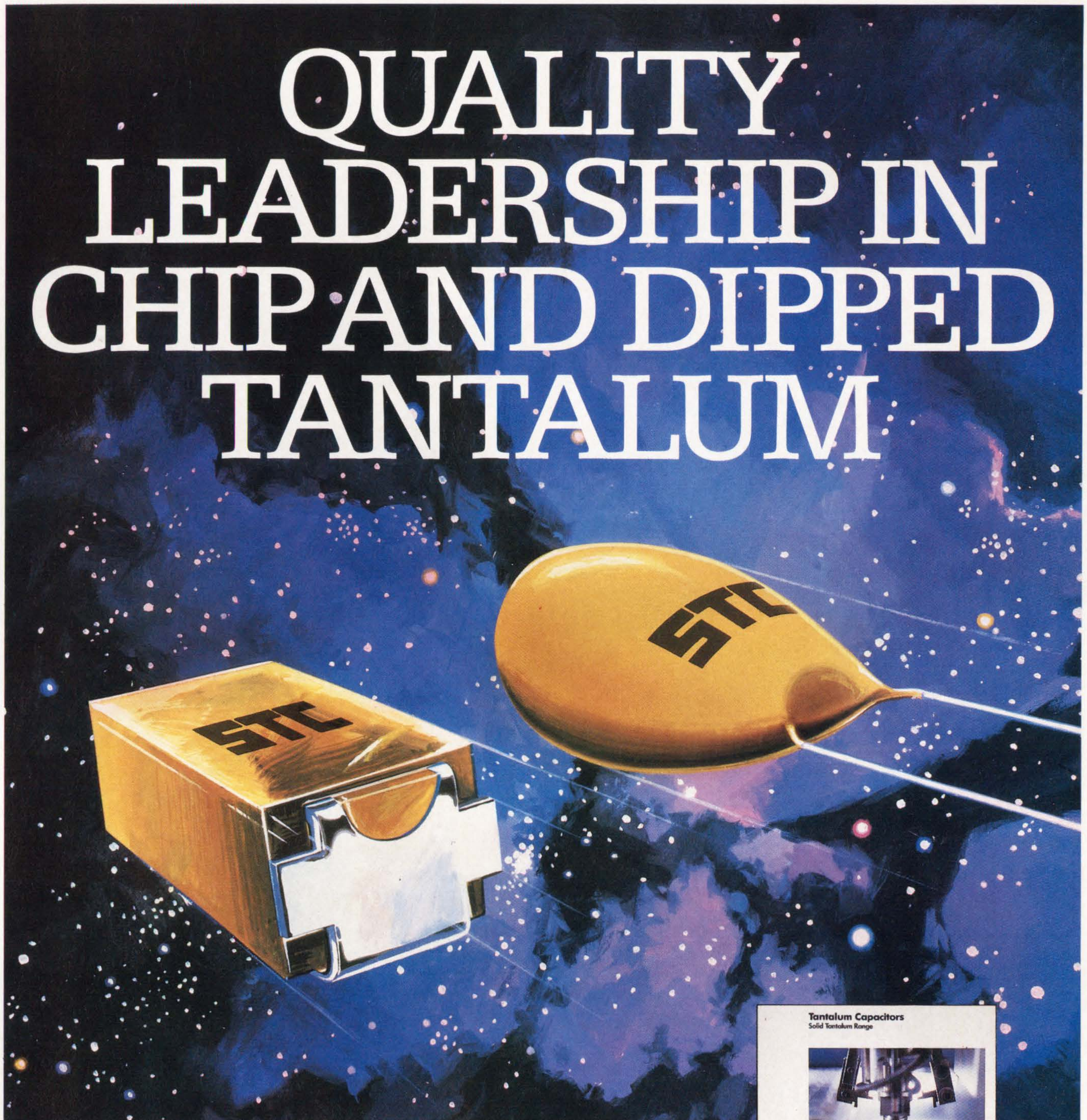
Packing 2.332G bytes onto a standard 8-mm videotape cartridge, *the EXB-8200 cartridge-tape subsystem fits into a 5¼-in. form factor. The peripheral's embedded SCSI interface supports continuous data-transfer rates of 246k bytes/sec and burst rates of 1.5M bytes/sec.*

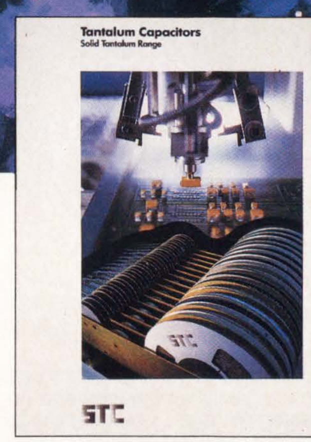
The environmental specifications for the drive include an operational temperature range of 5 to 45°C at a relative humidity of 20 to 80%. The subsystem's voltage requirements are 5 and 12V; it dissipates 15W. You can purchase off-the-shelf 8-mm video cartridges for use with this product at less than $20 per cartridge. The manufacturer plans to offer certified media as well. One evaluation unit costs $3500; the price drops to less than $1000 per unit for large OEM quantities.

—Steven H Leibson

Exabyte Corp, 4876 Sterling Dr, Boulder, CO 80301. Phone (303) 442-4333. TLX 361740.

Circle No 727





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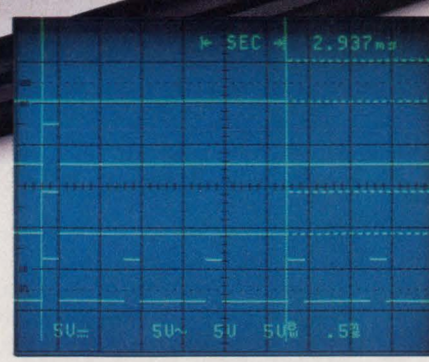

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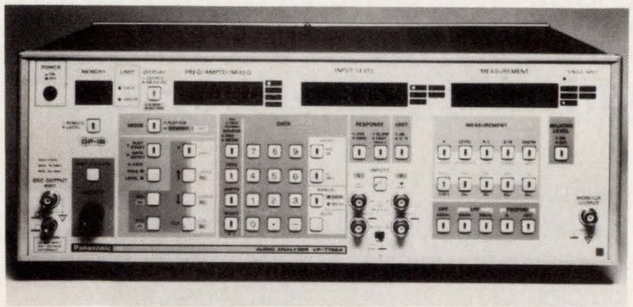
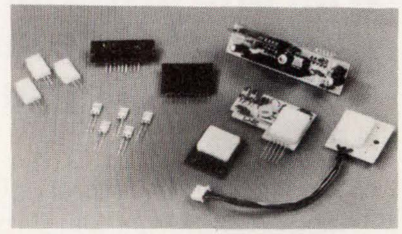
READERS' CHOICE

Of all the new products covered in EDN's **January 8, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **January 8, 1987,** issue.



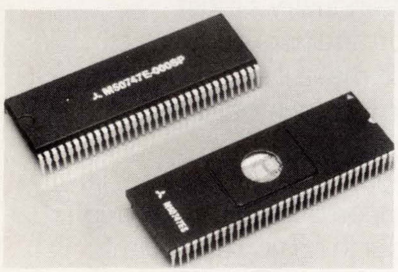
▲ AUDIO ANALYZER

The VP-7722P dual-channel audio analyzer has a 10-Hz to 110-kHz frequency range. It measures total harmonic distortion digitally (pg 283).
Panasonic Industrial Co.
Circle No 605



▲ HUMIDITY SENSOR

You can use the RH-8 bulk-resistance-polymer relative-humidity sensor and the SCMC-I and SCMC-V signal-conditioning microcircuits for constructing humidity transmitters (pg 247).
General Eastern Instruments Corp.
Circle No 601

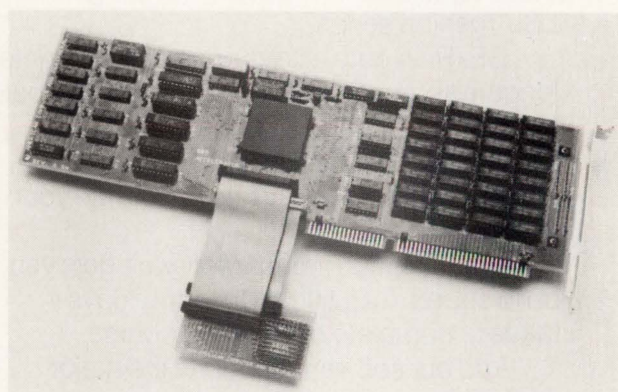


◀ MICROCONTROLLER

The Model M50747ES microcontroller contains 8k bytes of EPROM and 256 bytes of RAM and comes in a one-time-programmable version (pg 277).
Mitsubishi Electronics America Inc.
Circle No 604

C INTERPRETER

Instant-C 2.0 is an enhanced version of a C-language interpreter/compiler that runs on the IBM PC and compatibles. It has a full-screen, memory-resident editor for correcting source code (pg 272).
Rational Systems Inc.
Circle No 603



▲ ACCELERATOR

The 386 Turbo accelerator card has a 1M-byte cache memory with a 100% hit rate. It speeds software for the IBM PC/AT (pg 261).
American Computer & Peripheral Inc.
Circle No 602

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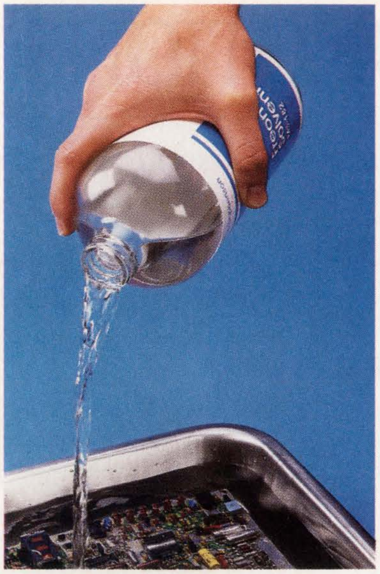

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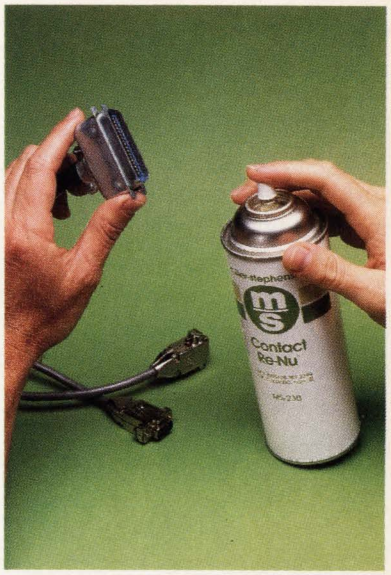

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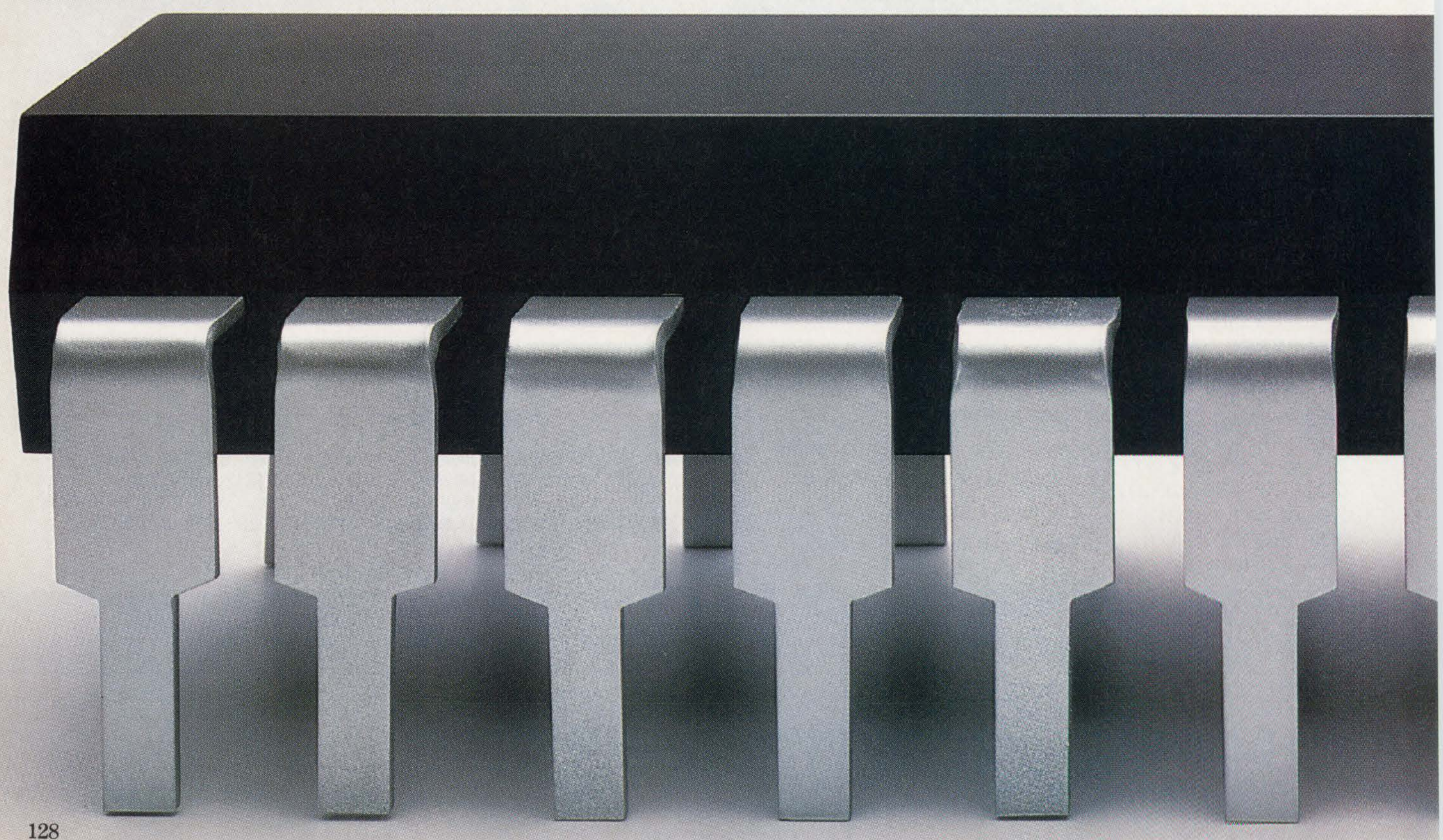


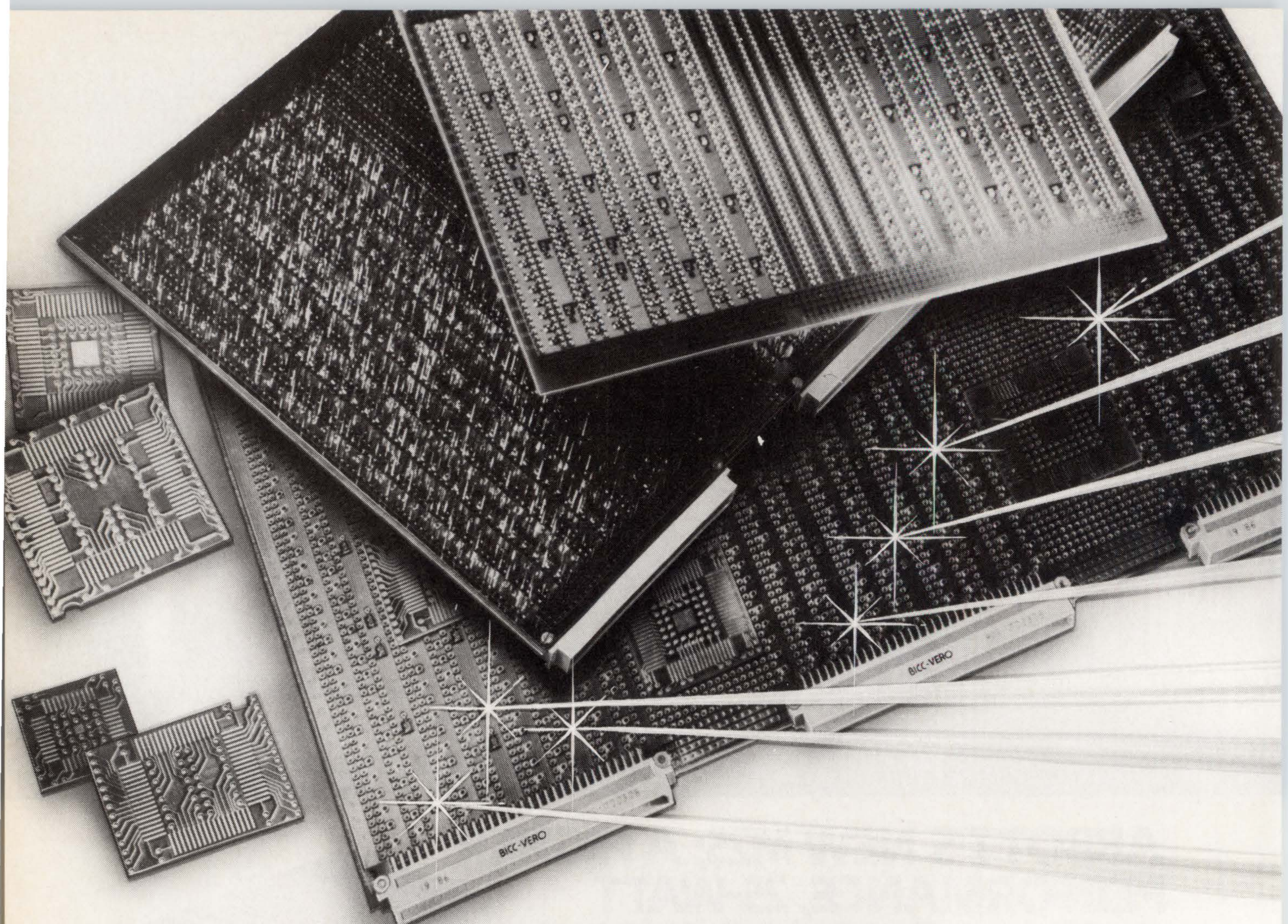
LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	9	45	46	0	0	11.0	8.8
Pot-Core	0	13	50	37	0	0	10.2	10.5
Laminate (power)	7	13	47	33	0	0	9.3	8.0
CONNECTORS								
Military panel	0	25	25	25	12	13	13.7	8.8
Flat/Cable	21	47	16	16	0	0	5.1	5.9
Multipin circular	0	27	33	13	13	14	13.1	9.6
PC	0	64	18	18	0	0	6.2	5.7
RF/Coaxial	21	29	36	7	7	0	6.6	5.4
Socket	20	40	27	13	0	0	5.4	4.4
Terminal blocks	12	41	35	12	0	0	5.9	5.6
Edge card	13	33	40	14	0	0	6.3	7.0
Subminiature	20	30	40	10	0	0	5.7	6.4
Rack & panel	0	29	57	14	0	0	7.6	6.2
Power	15	31	39	8	0	7	7.6	7.4
PRINTED CIRCUIT BOARDS								
Single-sided	0	55	40	5	0	0	5.6	4.8
Double-sided	0	38	58	4	0	0	6.4	6.5
Multilayer	0	23	62	15	0	0	8.0	8.9
Prototype	0	79	11	10	0	0	4.8	4.4
RESISTORS								
Carbon film	50	29	21	0	0	0	2.5	4.2
Carbon composition	43	29	10	19	0	0	4.9	3.9
Metal film	44	16	36	4	0	0	4.0	4.5
Metal oxide	30	39	31	0	0	0	3.6	4.3
Wirewound	16	28	56	0	0	0	5.3	2.4
Potentiometers	17	33	38	12	0	0	5.9	5.9
Networks	7	47	33	13	0	0	6.1	6.1
FUSES	29	29	35	7	0	0	4.8	2.4
SWITCHES								
Pushbutton	6	19	63	12	0	0	7.5	4.7
Rotary	5	18	65	12	0	0	7.5	5.7
Rocker	20	13	47	20	0	0	7.2	4.6
Thumbwheel	0	22	45	22	11	0	10.5	5.4
Snap action	20	20	30	20	10	0	8.7	3.5
Momentary	10	20	50	10	10	0	8.7	4.4
Dual in-line	17	33	17	17	16	0	9.2	4.2
WIRE AND CABLE								
Coaxial	43	28	29	0	0	0	3.1	1.8
Flat ribbon	47	20	33	0	0	0	3.3	1.7
Multiconductor	42	17	42	0	0	0	3.8	2.9
Hookup	61	30	9	0	0	0	1.6	1.5
Wire wrap	58	25	17	0	0	0	2.1	1.0
Power cords	36	23	36	5	0	0	4.3	4.3
Other	33	33	17	17	0	0	4.9	5.8
POWER SUPPLIES								
Switching	0	18	46	36	0	0	9.8	6.5
Linear	20	20	50	10	0	0	6.2	4.8
CIRCUIT BREAKERS	20	20	33	27	0	0	7.4	5.7
HEAT SINKS	27	20	47	6	0	0	5.4	3.9

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	28	22	39	11	0	0	5.5	5.2
PC board	0	25	58	17	0	0	8.0	8.1
Dry reed	25	25	37	13	0	0	5.7	6.9
Mercury	0	22	67	11	0	0	7.7	7.6
Solid state	21	36	29	14	0	0	5.6	8.9
DISCRETE SEMICONDUCTORS								
Diode	38	23	31	8	0	0	4.3	4.8
Zener	25	25	30	20	0	0	6.3	5.7
Thyristor	23	39	23	15	0	0	5.4	6.5
Small signal transistor	19	31	31	13	6	0	7.0	5.3
FET, MOS	24	23	18	35	0	0	7.6	7.6
Power, bipolar	25	8	33	34	0	0	8.1	4.8
INTEGRATED CIRCUITS, DIGITAL								
CMOS	10	26	32	32	0	0	8.2	6.4
TTL	31	19	38	12	0	0	5.5	6.5
LS	8	42	42	8	0	0	5.9	5.7
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	0	14	57	29	0	0	9.4	6.3
OP amplifier	10	20	40	30	0	0	8.5	6.5
Voltage regulator	11	33	39	17	0	0	6.7	6.6
MEMORY CIRCUITS								
RAM 16	37	18	27	18	0	0	5.5	4.0
RAM 64	20	40	30	10	0	0	5.2	4.2
RAM 256	20	20	40	20	0	0	6.9	5.0
ROM/PROM	22	22	45	11	0	0	5.9	5.3
EPROM	14	29	36	21	0	0	7.0	6.9
EEPROM	22	11	45	22	0	0	7.3	8.2
DISPLAYS								
Panel meters	11	45	33	11	0	0	5.7	6.4
Fluorescent	20	20	20	40	0	0	8.4	10.1
Incandescent	0	50	25	25	0	0	7.4	4.3
LED	17	33	33	17	0	0	6.3	5.6
Liquid crystal	0	31	46	23	0	0	8.2	7.2
MICROPROCESSOR ICs								
8-bit	27	9	37	27	0	0	7.4	4.2
16-bit	20	10	50	20	0	0	7.4	2.9
FUNCTION PACKAGES								
Amplifier	25	0	50	12	13	0	9.1	4.9
Converter, analog to digital	0	30	50	20	0	0	8.0	8.6
Converter, digital to analog	0	22	56	22	0	0	8.6	8.5
LINE FILTERS	11	33	34	22	0	0	7.1	6.4
CAPACITORS								
Ceramic	13	39	35	9	4	0	6.4	5.2
Ceramic monolithic	19	19	37	19	6	0	8.1	5.5
Ceramic disc	14	33	29	19	5	0	7.5	5.5
Film	10	30	35	20	5	0	8.1	5.9
Electrolytic	21	25	33	21	0	0	6.6	6.6
Tantalum	13	22	52	13	0	0	6.8	6.6
INDUCTORS	0	18	64	18	0	0	8.5	5.5

Source: *Electronics Purchasing* magazine's survey of buyers



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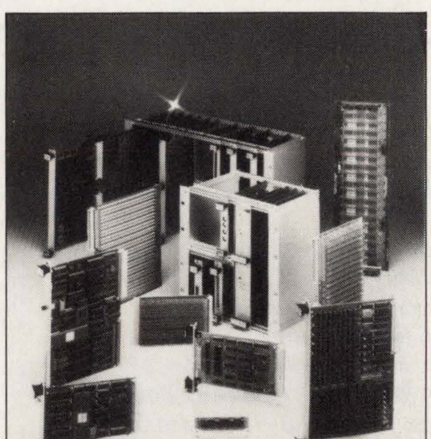

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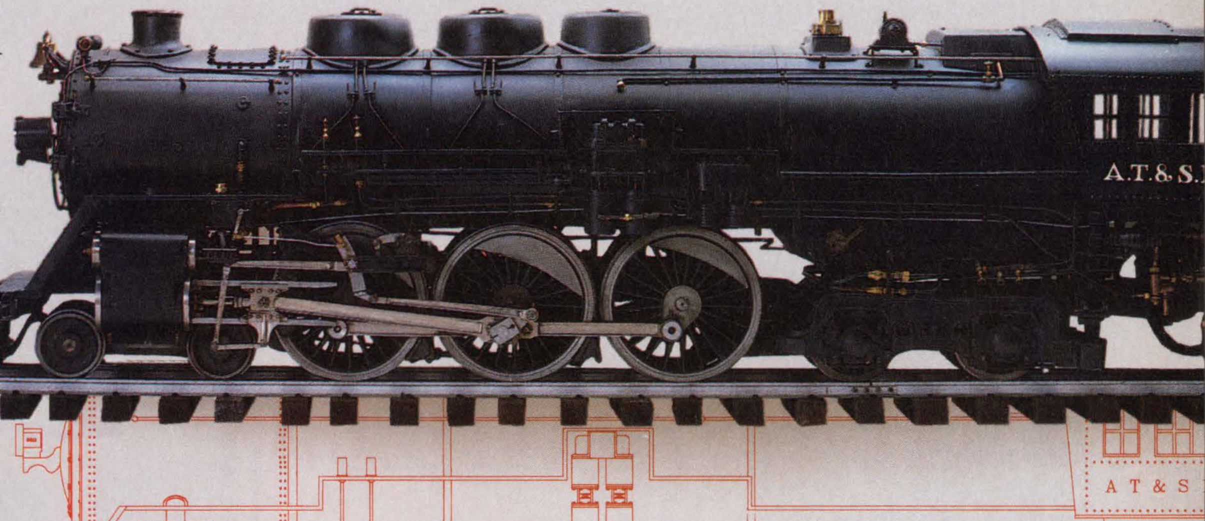

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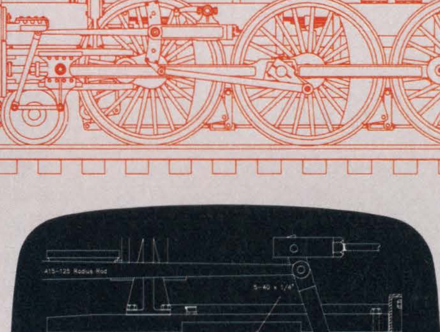

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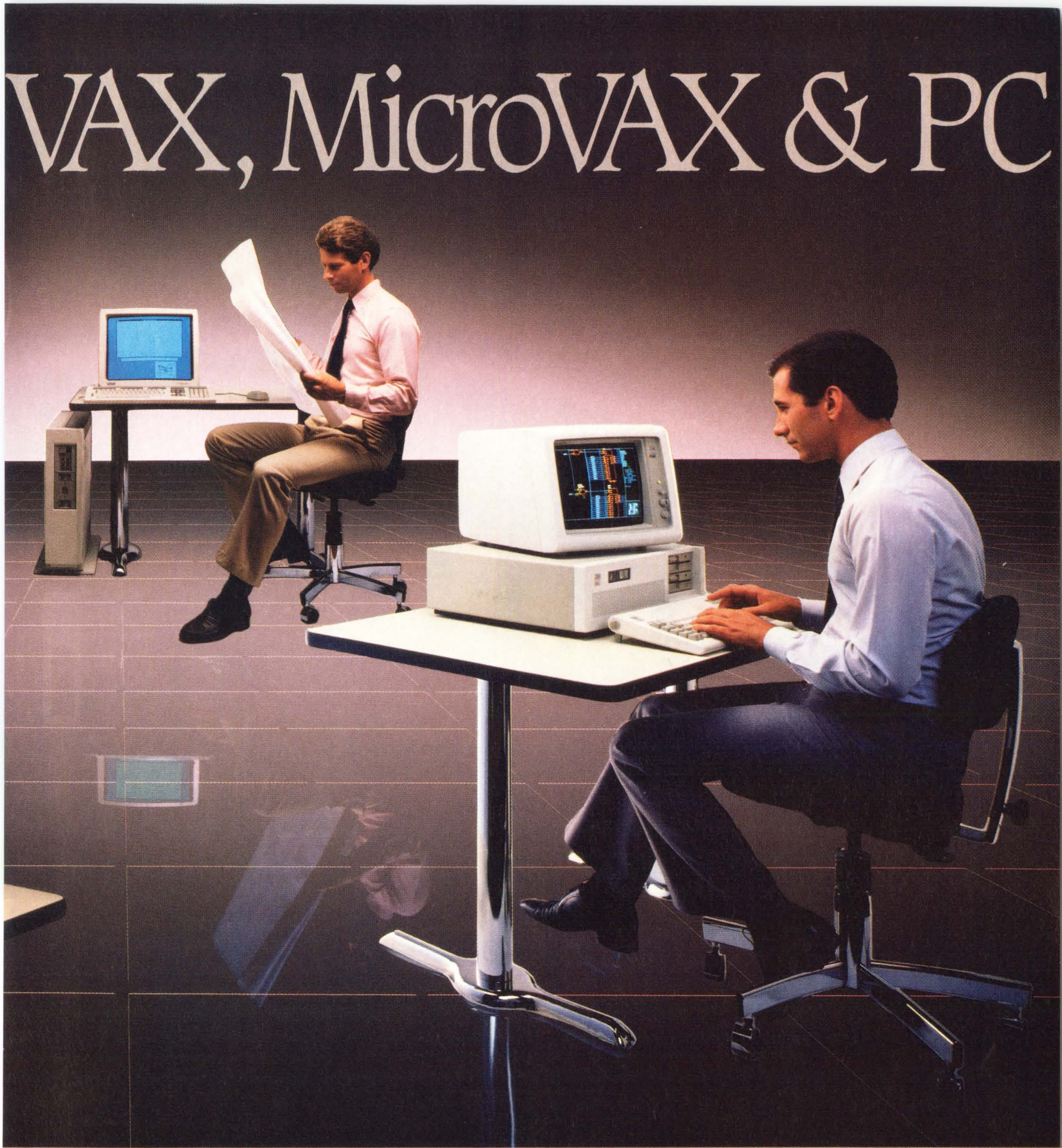
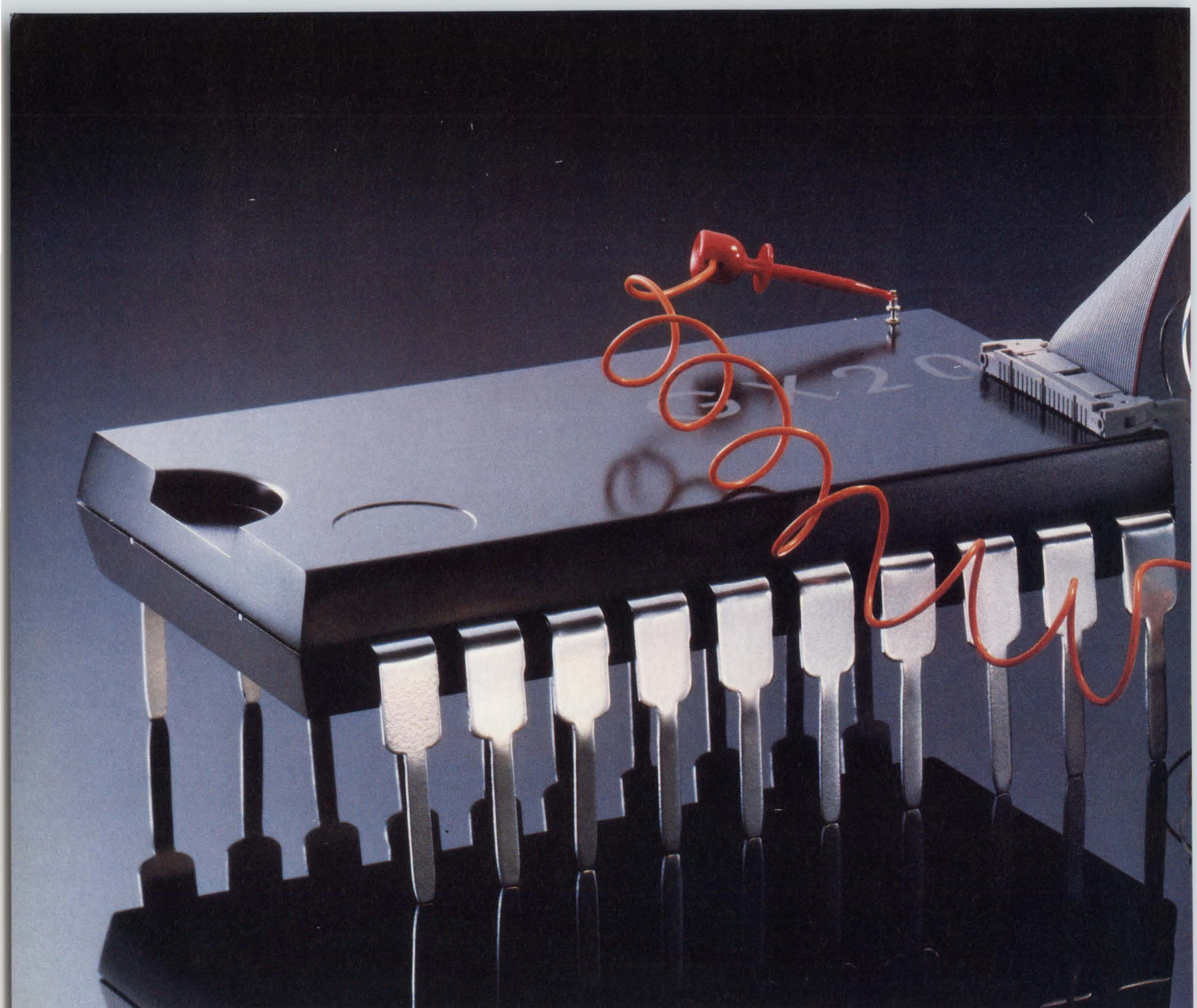
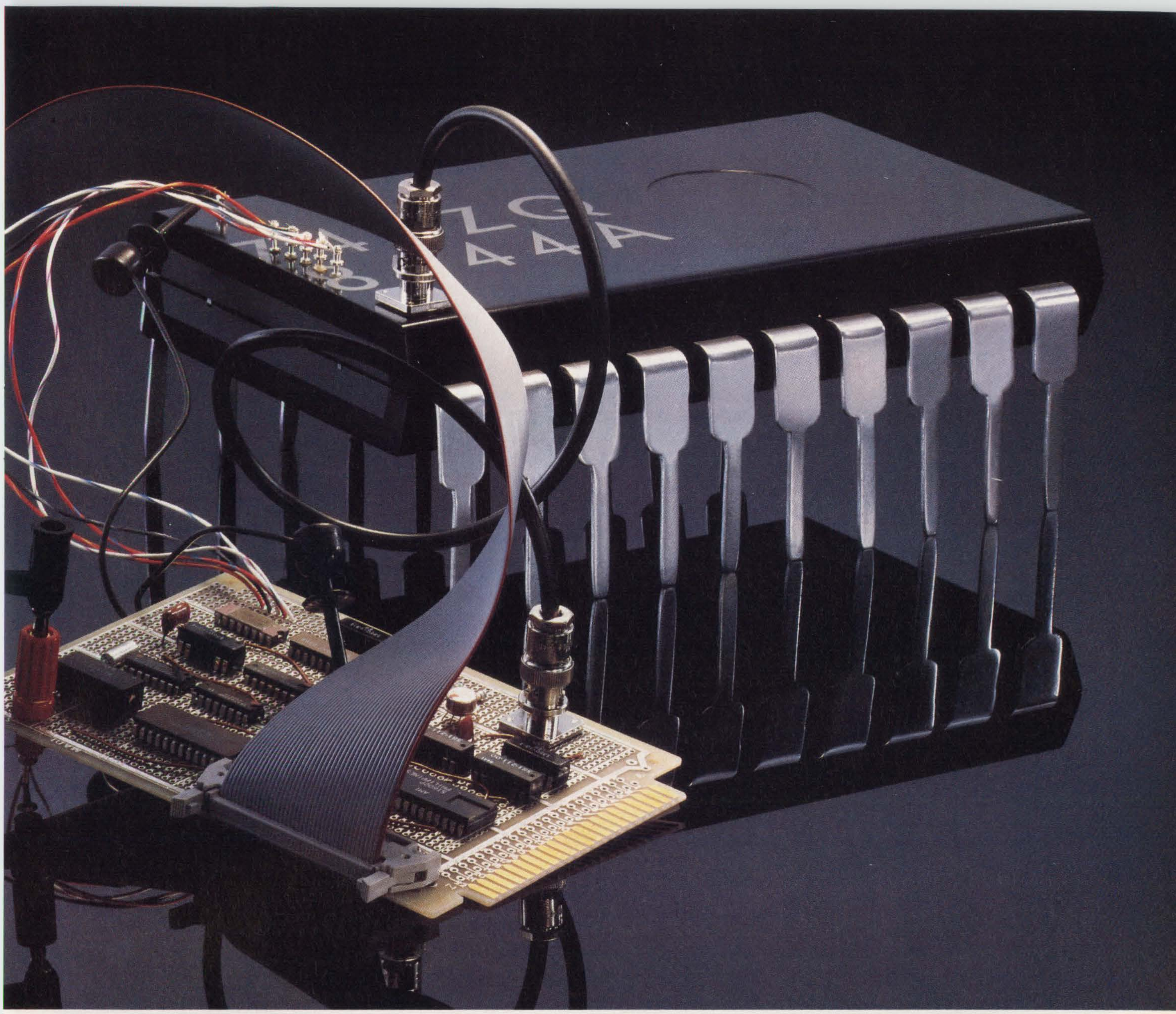
One Schematic is Worth a Thousand Netlists

The CASE system saves you hundreds of man-hours by allowing a bi-directional interface with other design


VAX, MicroVAX & PC





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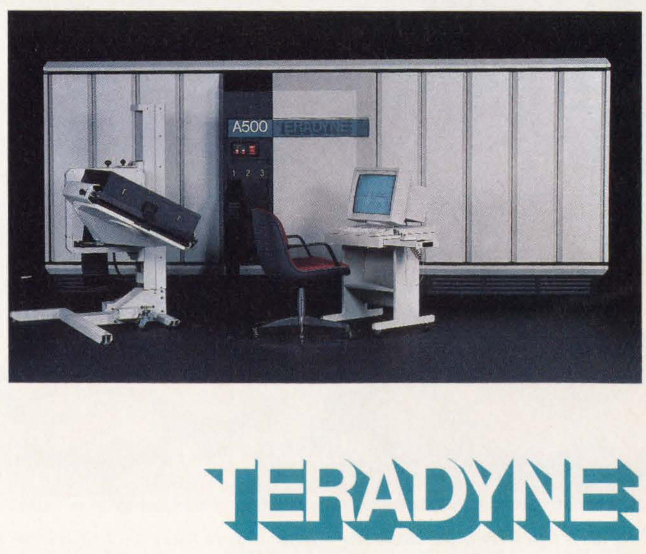

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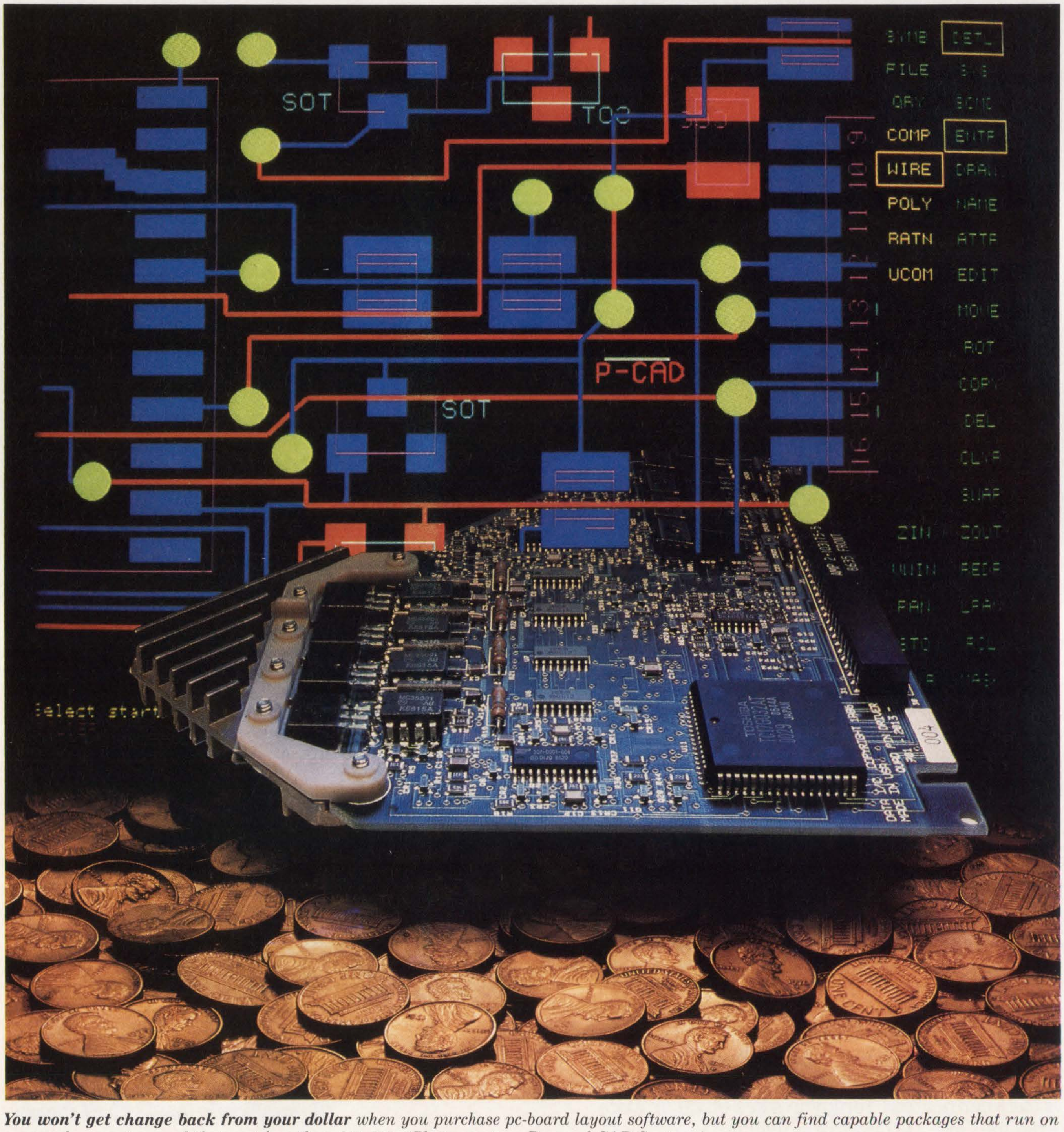
CIRCLE NO 106

Special Report

Low-cost pc-board



You won't get change back from your dollar *when you purchase pc-board layout software, but you can find capable packages that run on personal computers and that cost less than $15,000. (Photo courtesy Personal CAD Systems)*

Inexpensive programs can now complete pc-board layouts that once required mainframes or dedicated workstations. These programs, which typically run on personal computers, are automatic as well as interactive. You needn't use the packages often to become proficient with them—they're easy to learn and to use.

layout software

Eva Freeman, *Associate Editor*

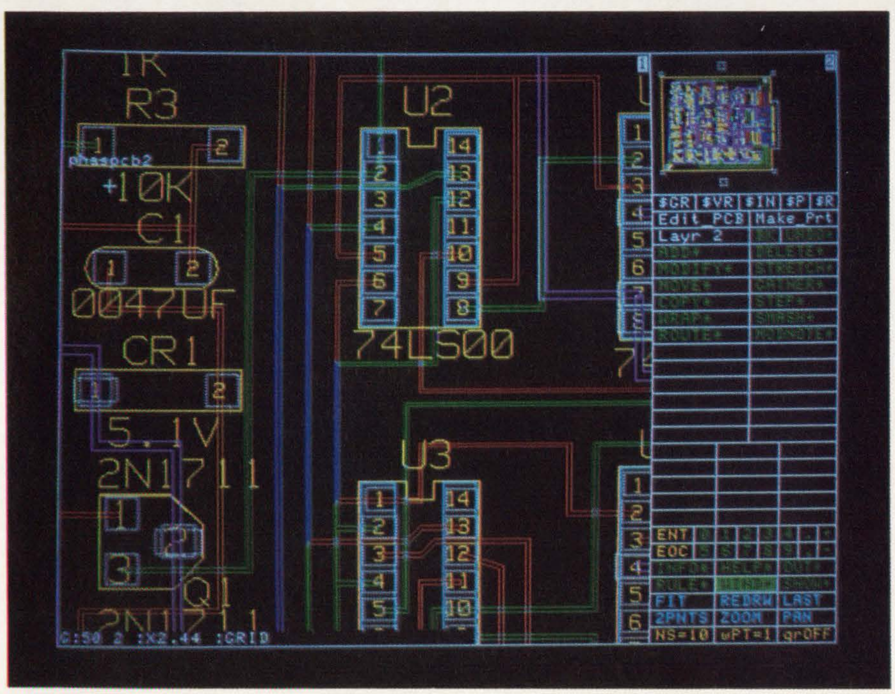
Advanced pc-board layout packages needn't be among the most expensive ones. In fact, for less than $15,000—in some cases much less—you can buy a layout package that can complete almost every pc-board design. Moreover, these programs are generally easy to use. Even if you have never laid out a pc board before, you can learn how to use a low-cost layout package quickly.

Until recently, you had to choose between sending your design to a pc-board service bureau or using a layout package that ran only on a dedicated workstation. CAD packages that cost less than $15,000 were drafting tools at best. However, today's low-cost pc-board layout software packages, most of which run on personal computers, generally provide the same features that workstation-based systems do. For example, most low-cost packages now offer optional autorouters. Because an autorouter draws interconnections automatically, you don't need layout experience to design your own board.

The autorouters in low-cost pc-board layout packages approach the sophistication of those in the most advanced workstation- or mainframe-based layout systems. For example, CAD Software's $750 Pads-Route autorouter provides three routers: power-and-ground, memory, and maze. The power-and-ground and memory routers specialize in power-supply and RAM interconnections; the maze router interconnects all other digital and analog components. However, the low-cost packages' autorouters don't match the speed of Calay's (Irvine, CA) V04 or Cadnetix's (Boulder, CO) CDX-75000 autorouters. Furthermore, low-cost autorouters can't consistently route all boards to 100% completion; the V04 and the CDX-75000 can.

Keep your expectations reasonable

Because the low-cost packages can't lay out boards as fast or as well as workstation- or mainframe-based software, you can't use a low-cost program for every design. Vendors of low-cost packages estimate that their programs can design about 80% of all pc boards. Therefore,



***Not all low-cost pc-board layout packages** run on general-purpose personal computers; Hewlett-Packard's Engineering Graphics System captures schematics and designs pc boards on the company's 32-bit workstation.*

Because an autorouter draws interconnections automatically, you don't need layout experience to design your own pc board.

before you commit your projects to a low-cost package, you must ascertain that such software is appropriate.

The low-cost packages' limitations are largely due to the limitations of the computers they run on. The MS-DOS operating system that the IBM PC uses, for example, can address only 640k bytes of memory. Thus, low-cost packages that run on IBM PCs and compatible computers can't handle databases of unlimited size.

You shouldn't expect, for example, to use a PC-based package to design an 8-layer, 500-IC board. Although several of the PC-based layout programs in **Table 1** (below) do permit eight layers and 500 components, the packages' autorouters can't route boards of such complexity. Furthermore, you'll usually find that the maximum number of traces limits your designs more than

TABLE 1—REPRESENTATIVE LOW-COST PC-BOARD LAYOUT PACKAGES

COMPANY	PRODUCT	BASE PRICE	REQUIRED HARDWARE	OPERATING SYSTEM	AUTO-ROUTER	AUTO-ROUTER PRICE
ABACUS SOFTWARE	PCBOARD DESIGNER	$195	ATARI 520ST OR 1040ST	GEM	•	
ACCEL TECHNOLOGIES	TANGO-PCB	$495	IBM PC/XT OR PC/AT	MS-DOS	•	
APTOS SYSTEMS	CRITERION II	$4000	ARTIST 1 CARD AND IBM PC/XT OR PC/AT	MS-DOS	•	$5000
AUTOMATED IMAGES	PERSONAL 870	$8000	IBM PC/XT OR PC/AT	MS-DOS		
B&C MICROSYSTEMS	PCB/DE	$395	IBM PC/XT OR PC/AT	MS-DOS (AND THE AUTOCAD DRAFTING PACKAGE)		
CAD SOFTWARE	PADS-PCB	$975	IBM PC/XT OR PC/AT	MS-DOS	•	$750
CASE TECHNOLOGY	VANGUARD PCB	$4250	IBM PC/AT, SUN-3, OR DEC MICROVAX	MS-DOS, UNIX, OR VMS	•	$5500
DAISY SYSTEMS	PERSONAL BOARDMASTER	$8000	IBM PC/AT OR DAISY PL386	DNIX		
DASOFT DESIGN	PROJECT: PCB	$950	IBM PC/XT OR PC/AT	MS-DOS	•	
DESIGN COMPUTATION	DRAFTSMAN-EE	$1147	IBM PC/XT OR PC/AT	MS-DOS	•	$2450
DOUGLAS ELECTRONICS	DOUGLAS CAD/CAM	$395	APPLE MACINTOSH	MACINTOSH		
ELECTRONIC DESIGN TOOLS	PROCAD	$2495	IBM PC/XT OR PC/AT AND 68000 COPROCESSOR	MS-DOS	•	$2495
ELECTRONIC INDUSTRIAL EQUIPMENT	EXECUTIVE CAD	$11,000	IBM PC/XT OR PC/AT	MS-DOS	•	
FUTURENET	DASH-PCB	$13,000	IBM PC/AT AND 32032 COPROCESSOR	UNIX	•	
HEWLETT-PACKARD	EGS	$7000	HP 9000	HP-UX		
KONTRON	KAD-286	$10,400	IBM PC/AT	MS-DOS		
PERSONAL CAD SYSTEMS	PCB-1	$6000	IBM PC/XT OR PC/AT	MS-DOS	•	$6000
RACAL-REDAC	REDBOARD	$12,000	IBM PC/XT OR PC/AT	MS-DOS	•	
SEETRAX (IN US, CIRCUITS AND SYSTEMS)	RANGER	$5000	IBM PC/AT	MS-DOS	•	$2000
SOFTCIRCUITS	PCLOPLUS	$1024	COMMODORE AMIGA 1000	AMIGADOS	•	
VAMP	McCAD	$395	APPLE MACINTOSH	MACINTOSH	•	$995
VISIONICS	EE DESIGNER II	$1875	IBM PC/XT OR PC/AT	MS-DOS	•	$1475
WINTEK	SMARTWORK	$895	IBM PC/XT OR PC/AT	MS-DOS	•	
ZIEGLER INSTRUMENTS (IN US, CADDY)	CADDY ELECTRONIC SYSTEM	$2495	IBM PC/XT OR PC/AT	MS-DOS	•	$2500

the maximum number of components or layers.

Table 1 lists the maximum number of traces that each package can handle, but note that vendors differ in the way they spec this capability: Some spec a maximum number of nets; others, a maximum number of lines. A net links all pins that are connected together; a line simply connects two points. (A line doesn't even necessarily connect two components; if a connection includes a 90° bend, some vendors consider the connection to be two lines.) A typical design contains roughly five lines per net. Thus, you can consider that a package that specs a 2000-net maximum is equivalent to one that specs a 10,000-line maximum.

The specs in **Table 1** can mislead you. Although a package might permit 1000 nets, 300 components, and 50 layers, you're better off avoiding the software limits.

AUTO-PLACEMENT	COMPATIBLE NET LISTS	MAXIMUM NUMBER OF COLORS	MAXIMUM NUMBER OF TRACES	MAXIMUM NUMBER OF COMPONENTS	MAXIMUM NUMBER OF LAYERS	PACKAGING TECHNOLOGIES
		2	1100 LINES	250	2	
	ACCEL, OMATION, ORCAD	16	26,000 LINES	1000	9	SMD
•	APTOS, FUTURENET, P-CAD	16	2000 NETS	1000	50	SMD, ECL, ANALOG
	APPLICON, FUTURENET, ORCAD	16			16	SMD, HYBRID
	B&C	16				
•	FUTURENET	16	4511 NETS	764	30	SMD, FINE-LINE
•	CASE	16	2000 NETS	1000	256	SMD
	DAISY	7	14,000 LINES	14,000	255	SMD
	DASOFT	6			4	SMD
•		16	4000 NETS	300	20	FINE-LINE
		2				SMD, ANALOG
•	ELECTRONIC DESIGN TOOLS	16	10,000 NETS	3000	56	SMD, CONSTANT-IMPEDANCE
•	ELECTRONIC INDUSTRIAL EQUIPMENT	16			4	SMD, ECL
	FUTURENET	4			10	FINE-LINE
	HP	15			255	HYBRID
	KONTRON	64	5300 LINES	3200	255	ECL, SMD, HYBRID
•	P-CAD, FUTURENET	16	1000 NETS	300	50	SMD
•	RACAL-REDAC	16	1900 NETS	511	16	SMD
•	SEETRAX	16	10,000 LINES	1400	16	SMD
		16				
•	VAMP	2	32,000 LINES	32,000	6	SMD, METRIC
•		16		999	26	SMD
	WINTEK	3			6	
	ZIEGLER	16			128	ANALOG

Vendors of low-cost packages estimate that their programs can design only about 80% of all pc boards, so you must ascertain that such software is appropriate.

As your design approaches the limits of the package, the software starts to run more slowly. Moreover, the autorouter generally fails to complete all the interconnections.

The 80386 μP will solve speed problems

You can accelerate most IBM PC-based layout packages simply by running them on an 80386-based personal computer. Most vendors of PC-based layout packages have written their software to run on generic PCs, and those programs can run on systems like the Compaq Deskpro 386. But even though a generic MS-DOS program runs faster on an 80386 μP than on a PC/XT or a PC/AT, a program that's written specifically for the 80386 could be even faster, deriving more benefit from the faster μP and the 32-bit bus.

The Personal Boardmaster 386, from Daisy Systems, is the first PC-based package that takes full advantage of the 80386. The system comprises pc-board layout software and a 386-based, $25,000 personal computer (made by Intel and available from Daisy). The computer includes a 16-MHz 80386 μP, a PC/AT bus, an 80287 math coprocessor, 4M bytes of RAM, and 53M bytes of hard-disk storage. A 17-in. monochrome display is standard, but you can select a 15- or a 19-in. color display.

The Personal Boardmaster 386 provides two operating systems: MS-DOS and DNIX. Because the $10,000 Personal Boardmaster 386 layout software doesn't run under MS-DOS, it isn't constrained by MS-DOS's memory limitations. Using this layout package, you can place as many as 14,000 components on your board. You can also draw as many as 14,000 lines and route a 255-layer design. You're obviously not going to place 14,000 components on a pc board or implement a 255-layer design, but you can be confident that the system won't slow down during any ordinary layout.

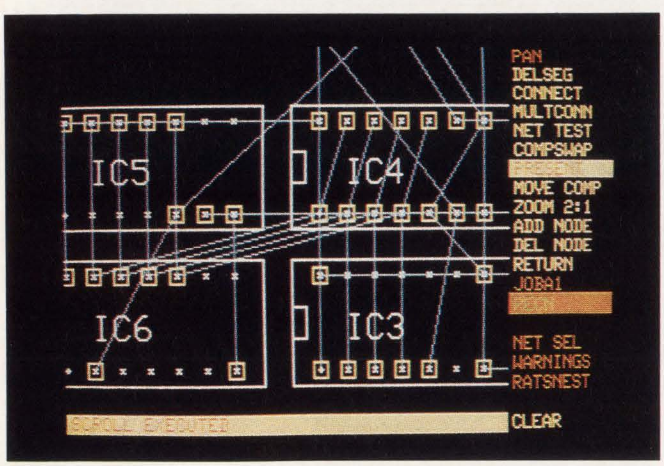
Daisy sells a PC/AT-based version of its pc-board layout software, Personal Boardmaster. This package runs at about half the speed of the 386-based system, but the slower package costs only $8000; the hardware starts at $20,000.

MS-DOS accepts extended-memory boards

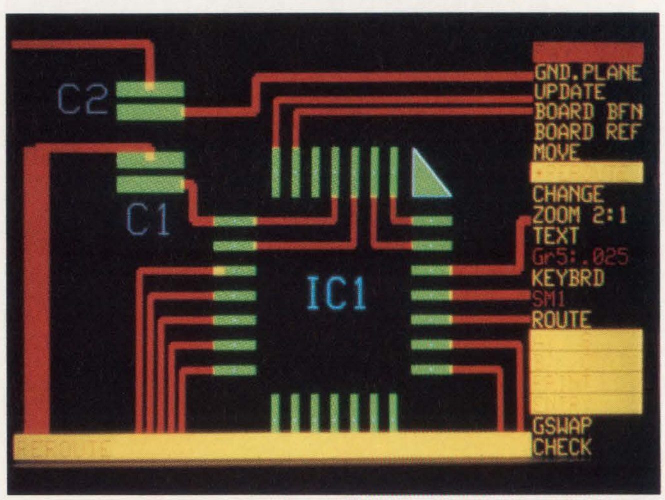
PC-board layout programs that run under MS-DOS usually cost less than software that runs under specialized operating systems. Furthermore, you can transfer data more easily among MS-DOS programs than among programs that run under incompatible operating systems. But if you want to run your software under MS-DOS, you must deal with MS-DOS's 640k-byte memory limitation.

To overcome this limitation, you might consider using an extended-memory board. Most PC-based layout packages can't yet take advantage of extended memory, but Case's and CAD Software's programs can use extended memory. CAD Software's $250 Pads-Large-SW option increases the maximum number of components from 539 to 764. This option also increases the number of connections from 2711 to 4511.

The addition of extended memory to Case's Vanguard program permits the system to complete pc boards that



A rat's-nest display, *such as the one provided by Electronic Industrial Equipment's Executive CAD package, can help you minimize the total length of interconnections in a layout.*



Even the most inexpensive packages *can handle sophisticated packaging techniques. Because the EE Designer II from Visionics can place components on both sides of a board, the package can lay out surface-mount designs.*

contain as many as 200 equivalent ICs. Without extended memory, the program can handle only as many as 125 equivalent ICs. In the next year, you'll be seeing many more layout packages using extended memory.

Plug-in cards accelerate PCs

You can also increase the speed and memory of a PC-based layout package by accelerating the PC. For example, Electronic Design Tools' Procad system includes a Motorola 68000-based coprocessor card. The 68000-based card, which includes 1M byte of RAM, costs $1595; the software starts at $2495.

Procad requires its own graphics card, which costs $1495 and features an 800×600-pixel resolution as well as a direct 68000 access port. In contrast to Procad's graphics card, a standard IBM Enhanced Graphics Adapter (EGA) card provides only 640×400 pixels. You'll find the increased resolution of the Procad card especially useful for fine-line or large designs.

The benefits of adding an accelerator card and a graphics controller to an IBM PC are obvious: Your calculations run faster, and you can read your display more easily. But don't forget that these features aren't free. In fact, the least expensive product that most vendors of low-cost layout packages sell is the basic program. As the **box**, "Watch out for the hidden extras," explains, optional programs and hardware dramatically increase the cost of pc-board layout.

The extra cost of an accelerator card can be a worthwhile investment. By adding a 32032-based coprocessor card to an IBM PC, FutureNet has been able to port a workstation-based layout program to the IBM PC/AT. Even on the PC/AT, though, the company's Dash-PCB program doesn't run under MS-DOS; the coprocessor card provides the PC with the Unix operating system.

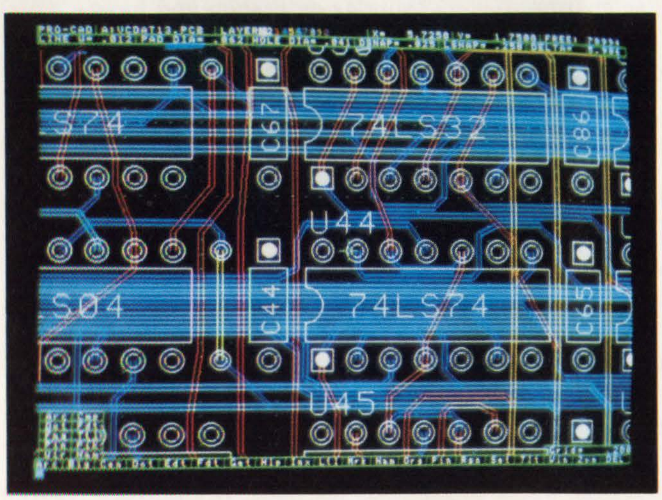
Dash-PCB layout software includes such features as 45° routing, fine-line layouts, and a multistrategy router. The package, which comprises software, the coprocessor card, and an 80M-byte hard disk, costs $13,000.

The best way to benefit from the memory-management features of Unix and the speed of a 32-bit bus is, of course, to run your software on a 32-bit workstation. But in general, workstation-based programs cost much more than PC-based programs. One exception to that rule is Hewlett-Packard's Engineering Graphics System. The package, which runs on Hewlett-Packard's 9000 Series 300 workstations, costs $7000. The workstations cost $15,000 to $25,000.

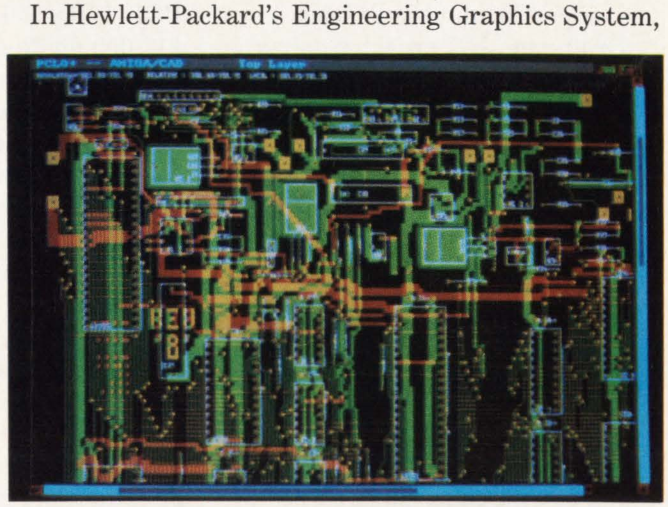
The architecture of the Engineering Graphics System lets you customize every module in the package. For example, you can adapt the bill-of-materials module to satisfy your company's purchasing requirements.

Bills of materials are a weak point in many pc-board layout packages. Although almost every program offers a bill-of-materials utility, these subroutines typically generate generic parts lists. Your purchasing department can't work with a request for a 10-kΩ resistor, however. You must also specify the wattage. Furthermore, many companies require internal part numbers in bills of materials, so a generic parts list might be useless.

In Hewlett-Packard's Engineering Graphics System,



By adding a 68000-based coprocessor card *from Electronic Design Tools to an IBM PC, you can run the company's Procad software as fast on the PC as you can on a 32-bit workstation.*



To encourage user improvements *to its pc-board layout package, Softcircuits provides the source code of its PCLOplus layout package. The program runs on Amiga computers.*

As your design approaches the limits of your package, the software starts to run more slowly, and the autorouter generally fails to complete all the interconnections.

you can associate design data and graphics data. Instead of just assigning a name to a part, you can link a symbol to as many design specifications as you need. The bill-of-materials program can handle as many as 20 specs, including part numbers and prices, for each part.

A $4000 option to the Engineering Graphics System lets you use the system for hybrid-circuit design. Using this program, you can generate thick-film resistors from resistor-paste curves and draw irregularly shaped conductors.

Such irregularly shaped conductors are important for analog circuits as well as for hybrids. Analog circuits require the irregular shapes for their ground planes. To create and fill polygons, you can use the Engineering Graphics System or even a lower-cost package like Aptos's IBM PC-based Criterion II.

Complex graphics for analog or dense digital circuits require greater resolution than an EGA card can generate. Therfore, Criterion II uses Control Systems' (St Paul, MN) Artist I card, which produces a 1024×768-pixel display. By controlling a 19-in. color monitor with this graphics card, your IBM PC's monitor can provide the graphics resolution of a CAD workstation. Criterion II costs $4000; the Artist I option lists for $1200.

Designs often require automatic layout

Good graphics are necessary to lay out a dense circuit, but graphics alone aren't sufficient. Unless you can boast of considerable experience in pc-board layout, you won't be able to route the interconnections on your

Watch out for the hidden extras

When you calculate the price of a pc-board layout package, don't forget to figure the options into your cost. Some vendors of low-cost pc-board layout software are like automobile manufacturers—they derive their profits from options, not from the basic package.

Unfortunately, you'll find that some optional programs really aren't optional. For example, Design Computation's basic Draftsman-EE provides only a graphics editor, a component library, and bill-of-materials and parts-list utilities. To generate a rat's-nest display and to check for design-rule violations, you must purchase the optional DC/Check program. The autorouter is yet another option. But you usually need these options for your pc-board layouts.

Draftsman-EE cost $749, DC/Check costs $398, and the autorouter lists for $2450. For $4000, you can purchase all of these tools, as well as 12 months of telephone assistance. Although $4000 certainly is a modest price for a complete pc-board layout system, it is more than five times the cost of the basic program.

Options can also cause sizable changes in the price of the more expensive of the low-cost packages. Compare, for example, the price of the PCB-1 and the Redboard pc-board layout packages. Personal CAD charges $6000 for PCB-1; Racal-Redac charges $12,000 for Redboard. Redboard includes autorouting and autoplacing software, however, and PCB-1 does not. P-CAD charges $6000 for its autorouting and autoplacing package. Thus, if you need an autorouter, you pay the same amount for either program.

(Racal-Redac's and Personal CAD's complete design packages, which combine automatic pc-board layout and schematic capture, also feature similar price tags. Personal CAD's PCB-3 costs $15,950; Racal-Redac's Redcad costs $14,900.)

You can buy a pc-board layout package for as little $95. This product, sold by Douglas Electronics as Douglas CAD/CAM and by Bishop Graphics as Quik Circuit, doesn't provide automatic-layout features or schematic capture. Furthermore, the program doesn't include interfaces to pen plotters or photoplotters. To use the $95 package, you must transmit your layout to Douglas or Bishop and have them fabricate your pc board, or you must buy the $300 pen-plotting option or the $500 combined pen-plotting and photoplotting option.

Options, especially for packages that list for less than $1000, greatly increase the total price of pc-board layout software. Nonetheless, the total cost is far less than the cost of a pc-board service bureau or a workstation-based layout system. Just remember the advice of the US Postal Service: "If an offer sounds too good to be true, it probably is."

The benefits of adding an accelerator card and a graphics controller to an IBM PC are obvious: Your calculations run faster and you can read your display more easily.

board without an autorouter **(Ref 1)**.

An automatically routed layout, however, can be only as good as the component placement permits. If you don't optimize the placement of components on your board, your board will have more vias and longer interconnections than should be necessary. In many cases, the autorouter will simply fail to route the board completely. And in all cases, pc-board fabrication costs will be higher and system speed will be lower than they could be.

Most pc-board layout systems include a rat's-nest utility that can help you optimize the component placement. A rat's nest displays straight-line connections between components. Using a rat's nest, you can shift components on your layout and minimize the average length of interconnections.

Unless your layout is comparatively simple or you are an experienced pc-board designer, you won't obtain the best possible layout just by optimizing a rat's nest. "Rat's nest" is an appropriate name—the tangle of lines can be difficult to unravel.

Several low-cost pc-board layout packages, such as Racal-Redac's Redboard, now provide an automatic alternative to manual placement. You'll find two automatic-placement routines in Redboard. The first minimizes the total length of interconnections by rearranging the components on the layout. The second minimizes interconnection lengths further by adjusting the position of all DIPs on a board. The package also optimizes component placement by swapping logically equivalent gates or pins. By minimizing the length of interconnections, the automatic-placement software simplifies the autorouter's task.

If, after Redboard has optimized the position of board components, you see a way to improve the placement, you can move or rotate components interactively. Including automatic placement and routing, Redboard costs $12,000. You can also add schematic capture to Redboard; the schematic-editor option costs $2900.

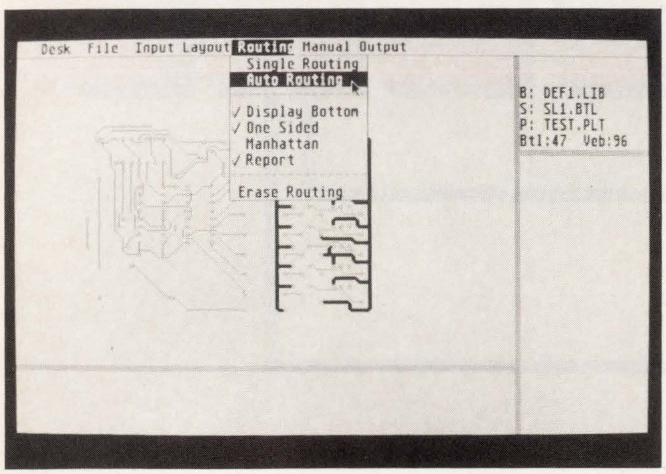
Feel free to include SMDs in your board

Automatic layout tools in low-cost packages enable you to implement advanced packaging technologies on your PC. For example, Personal CAD has just added features for SMD layout to its PCB-1 layout program. Because SMDs don't have leads that extend through a board, the program lets you place components on both sides of a board. The program also permits buried vias (vias that don't extend through all layers of a board).

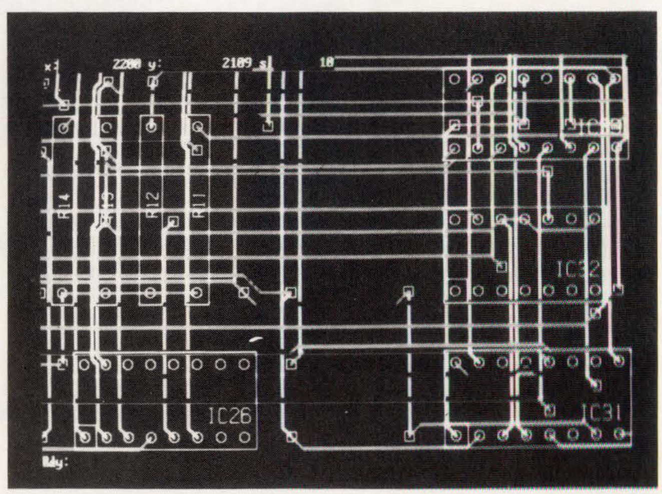
A library of SMDs rounds out PCB-1's tools for designing with surface-mount components. The SMD library features TTL, CMOS, discrete, and linear components. PCB-1 costs $6000. The company's PCB-3 package, which combines PCB-1, automatic placement and routing, and schematic capture, costs $15,950.

If you're a typical user of low-cost pc-board layout software, your design needn't accommodate advanced packaging technologies or implement sophisticated layout algorithms. All you need is an inexpensive package that's easy to use.

Several of the least expensive products run on per-



Interconnecting a design with 45° routing *can shorten many routing paths. Abacus Software's PCBoard Designer, which runs on Atari ST computers, features 45° routing in a low-cost package.*



Vias increase fabrication costs *and decrease production yields, so the via-minimization algorithms in Design Computation's Draftsman EE automatic-layout package will give you an immediate return on your investment.*

Bills of materials are a weak point in many pc-board layout packages; subroutines typically can generate only generic parts lists.

sonal computers that aren't compatible with IBM PCs. **Table 1** lists four such pc-board layout programs. The $195 PCBoard Designer from Abacus Software provides pc-board layout tools to Atari users. Softcircuits has brought pc-board layout to Commodore's Amiga; Softcircuits gives you the choice of the $500 entry-level PCLO program or the $1024 PCLOplus package, which runs faster than the less expensive version. Apple Macintosh users can choose between two programs: Vamp and Douglas Electronics both offer packages that start at $395.

Nevertheless, most low-cost pc-board layout pack-

Manufacturers of low-cost pc-board layout packages

For more information on pc-board layout packages, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Abacus Software
Box 7219
Grand Rapids, MI 49510
(616) 241-5510
Circle No 650

Accel Technologies Inc
7358 Trade St
San Diego, CA 92121
(619) 695-2000
Circle No 651

Advanced Microcomputer Systems Inc
2780 SW 14th St
Pompano Beach, FL 33069
(305) 975-9515
Circle No 652

Aptos Systems Corp
4113 Scotts Valley Dr
Scotts Valley, CA 95066
(408) 438-2199
Circle No 653

Augat Inc
Box 1037
Attleboro, MA 02703
(617) 222-2202
Circle No 654

Automated Images Inc
53 Cummings Park
Woburn, MA 01801
(617) 933-1731
Circle No 655

B&C Microsystems
6322 Mojave Dr
San Jose, CA 95120
(408) 997-7685
Circle No 656

Bishop Graphics Inc
5388 Sterling Center Dr
Westlake Village, CA 91359
(818) 991-2600
Circle No 657

CAD Software Inc
Box 1142
Littleton, MA 01460
(617) 486-9521
Circle No 658

Caddy Corp
3401 Algonquin Rd
Rolling Meadows, IL 60008
(312) 394-7755
Circle No 659

Case Technology Inc
2141 Landings Dr
Mountain View, CA 94043
(415) 962-1440
Circle No 660

Circuits and Systems
Foot of Second St
East Rockaway, NY 11518
(516) 593-4301
Circle No 661

Control Data Corp
Box 0
Minneapolis, MN 55440
Phone local office
Circle No 662

Daisy Systems Corp
700 Middlefield Rd
Mountain View, CA 94039
(415) 960-6593
Circle No 663

Dasoft Design Systems
1827B Fifth St
Berkeley, CA 94710
(415) 486-0822
Circle No 664

Design Computation Inc
10 Frederick Ave
Neptune, NJ 07753
(201) 922-4111
Circle No 665

Douglas Electronics
718 Marina Blvd
San Leandro, CA 94577
(415) 483-8770
Circle No 666

Electronic Design Tools Inc
1509 Falcon St
Suite 103
DeSoto, TX 75115
(214) 224-2472
Circle No 667

Electronic Industrial Equipment SA
15 rue Marziano
Box 140
1211 Geneva 24
Switzerland
(022) 423260
Circle No 668

FutureNet
9310 Topanga Canyon Blvd
Chatsworth, CA 91311
(818) 700-0691
Circle No 669

Great Softwestern Co Inc
270 W Hickory St
Denton, TX 76201
(817) 383-4434
Circle No 670

Hewlett-Packard Co
3404 E Harmony Rd
Fort Collins, CO 80525
(303) 229-3800
Circle No 671

Kontron Electronics Inc
630 Clyde Ave
Mountain View, CA 94039
(415) 965-3505
Circle No 672

Kontron Messtechnik GmbH
Oskar-von-Miller-Strasse 1
8057 Eching
West Germany
(08165) 77550
Circle No 673

Modula Corp
1673 W 820 N
Provo, UT 84601
(801) 375-7400
Circle No 674

Personal CAD Systems Inc
1290 Parkmoor Ave
San Jose, CA 95126
(408) 971-1300
Circle No 675

QTech Inc
256 E Hamilton Ave
Campbell, CA 95008
(408) 370-3910
Circle No 676

Racal-Redac Inc
4 Lyberty Way
Westford, MA 01886
(617) 692-4900
Circle No 677

Racal-Redac Ltd
Tewkesbury,
Gloucestershire GL20 8HE
United Kingdom
(0684) 294161
Circle No 678

Seetrax Ltd
Unit 10, Rodney Rd
Portsmouth, Hampshire PO4 8SS
United Kingdom
(0705) 754-320
Circle No 679

Softcircuits Inc
401 SW 75th Terrace
North Lauderdale, FL 33068
(305) 721-2707
Circle No 680

Vamp Inc
6753 Selma Ave
Los Angeles, CA 90028
(213) 466-5533
Circle No 681

Visionics Corp
1284 Geneva Dr
Sunnyvale, CA 94089
(408) 745-1551
Circle No 682

Wintek Corp
1801 South St
Lafayette, IN 47904
(317) 742-8428
Circle No 683

Wire Graphics
95 Sherwood Ave
Farmingdale, NY 11735
(516) 293-1525
Circle No 684

Ziegler Instruments GmbH
An der Waldesruh 17
D-4050 Monchengladbach 2
West Germany
Circle No 685

***A point-to-point router assists** interactive pc-board design with Wintek's Smartwork program; an autorouter completes sections of board designs that don't require manual intervention.*

ages run on the IBM PC. Two vendors have held down the cost of their IBM PC programs by linking their software to Autodesk's (Sausalito, CA) Autocad drafting package. Because Great Softwestern's Auto-Board and B&C Microsystems' PCB/DE use Autocad as a drafting tool, the creators of the programs could focus their code on pc-board layout. Auto-Board, which includes schematic capture and automatic routing, costs $2495; PCB/DE costs $395.

Most PC-based packages supply their own drafting software. Wintek's $895 Smartwork program, for example, includes all the graphics tools you need for pc-board layout. To aid you in pc-board design, Wintek has recently added an $895 schematic-capture program and is now introducing an automatic router.

Visionics has recently added an automatic router to its EE Designer II pc-board layout package. The basic software costs $1875; the autorouter option increases the price by $1100. Besides 2-layer boards, the autorouter can route SMD and multilayer boards.

Multilayer capabilities notwithstanding, low-cost pc-board layout packages still don't match the speed or provide the quality of layout algorithms that traditional layout systems offer. If you give your PC the kind of layout problem that would challenge a mainframe or a 32-bit workstation with custom autorouting hardware, you'll be sorely disappointed. But if your pc boards fall among the 80% of designs that low-cost packages can complete, you'll find that pc-board layout has never been so inexpensive and so easy. **EDN**

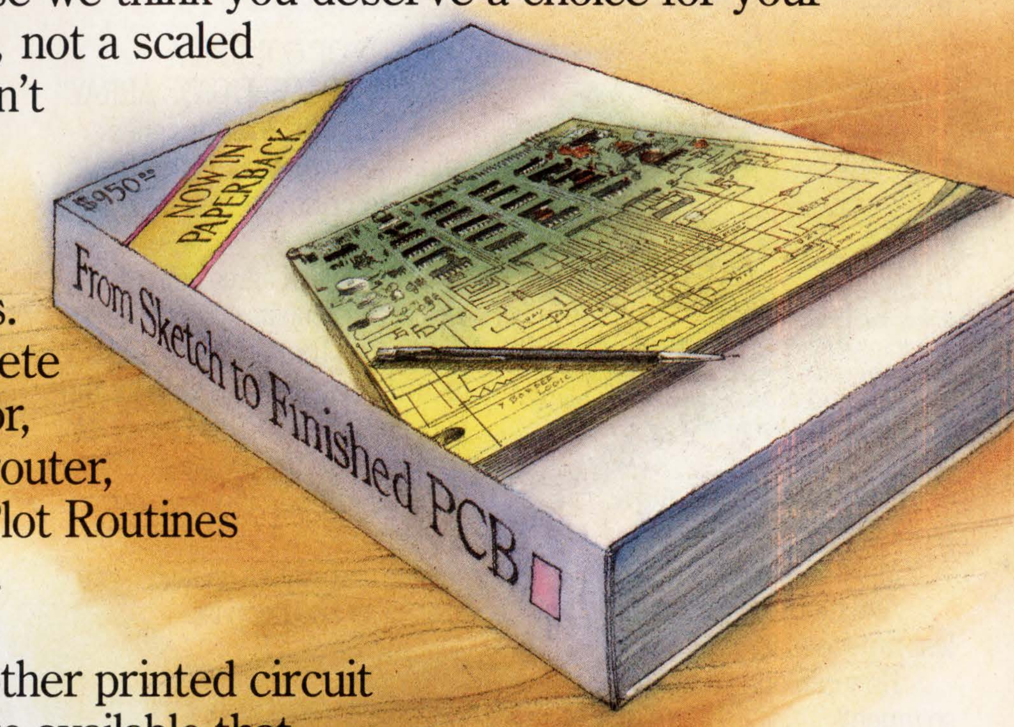
Reference

1. Freeman, Eva, "Autorouters use sophisticated algorithms to lay out complex, multilayer pc boards," *EDN*, August 7, 1986, pg 67.

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

PROJECT:
PCB
SOFTWARE FOR PRINTED CIRCUIT DESIGN

We like to think of it as our paperback edition. Project:PCB was developed by our engineers because we think you deserve a choice for your money; a real choice, not a scaled down version that can't quite handle the job.



Project:PCB specs speak for themselves. The system is complete with Schematic Editor, Layout Editor, Autorouter, Library Managers, Plot Routines and Listing Routines.

At $950, there's no other printed circuit board design software available that matches Project:PCB for performance, thoroughness and price. You get a package that does the job—from design concept to board artwork.

To review Project:PCB for yourself, ask about our demo disk. All purchases are backed by our 30-day money-back guarantee. So order your copy of Project:PCB now—it's destined to be a best-seller.

DASOFT
DESIGN SYSTEMS, INC.
PHONE (415) 486-0856
P.O. Box 8088, Berkeley, CA 94707-8088

Project:PCB *sells for $950, and can be shipped immediately from stock. Terms are prepay, COD, VISA or MasterCard. The Project:PCB system runs under MS-DOS™ on the IBM®XT/AT (640K RAM and a minimum 10Mb Hard Disk) and compatibles. Graphics options include Hercules™ Monochrome (or compatible), CGA or EGA with monochrome monitor, and EGA with color monitor (add $300 for full color). A system mouse is required and a wide variety of plotters are supported. All Project:PCB editors are menu-driven.*

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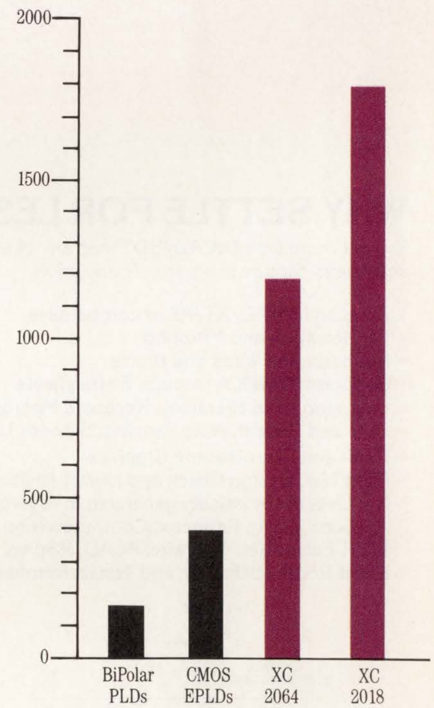

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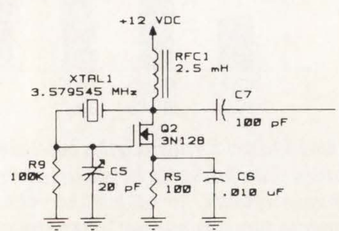

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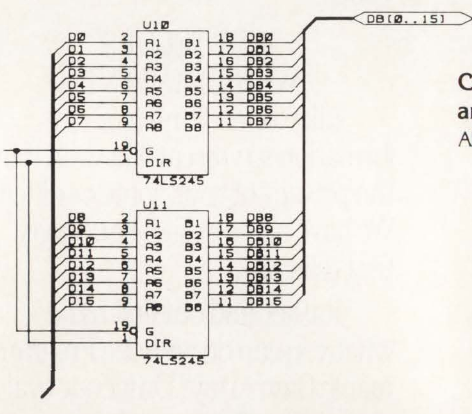

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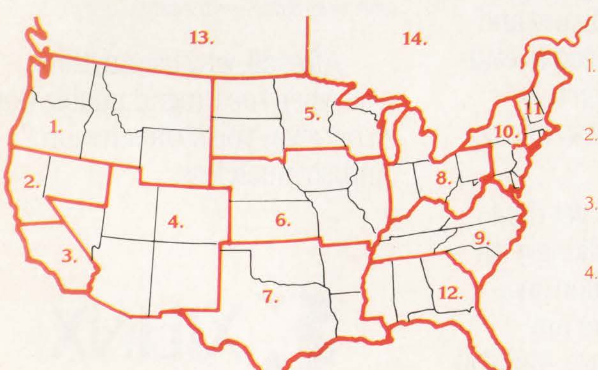

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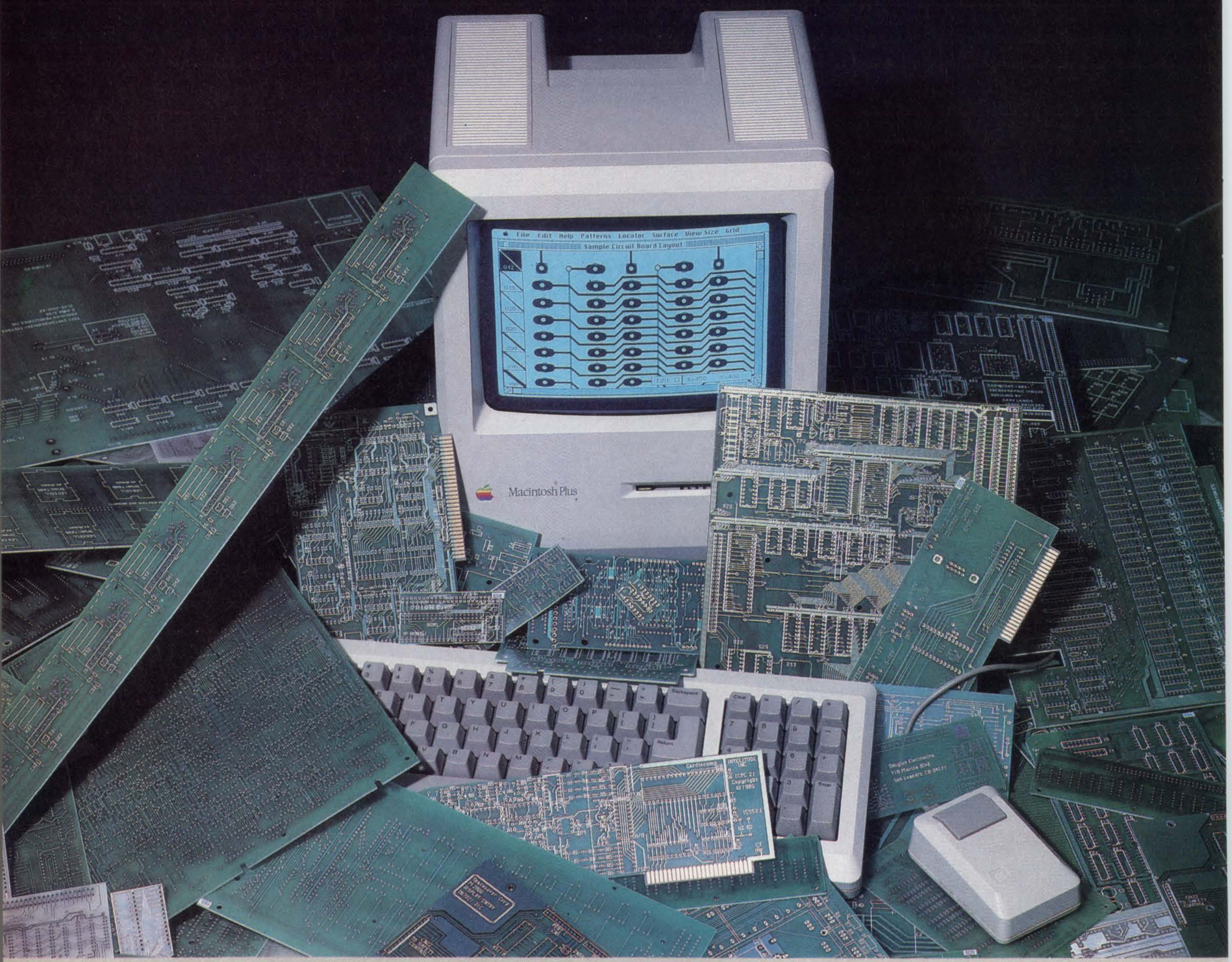

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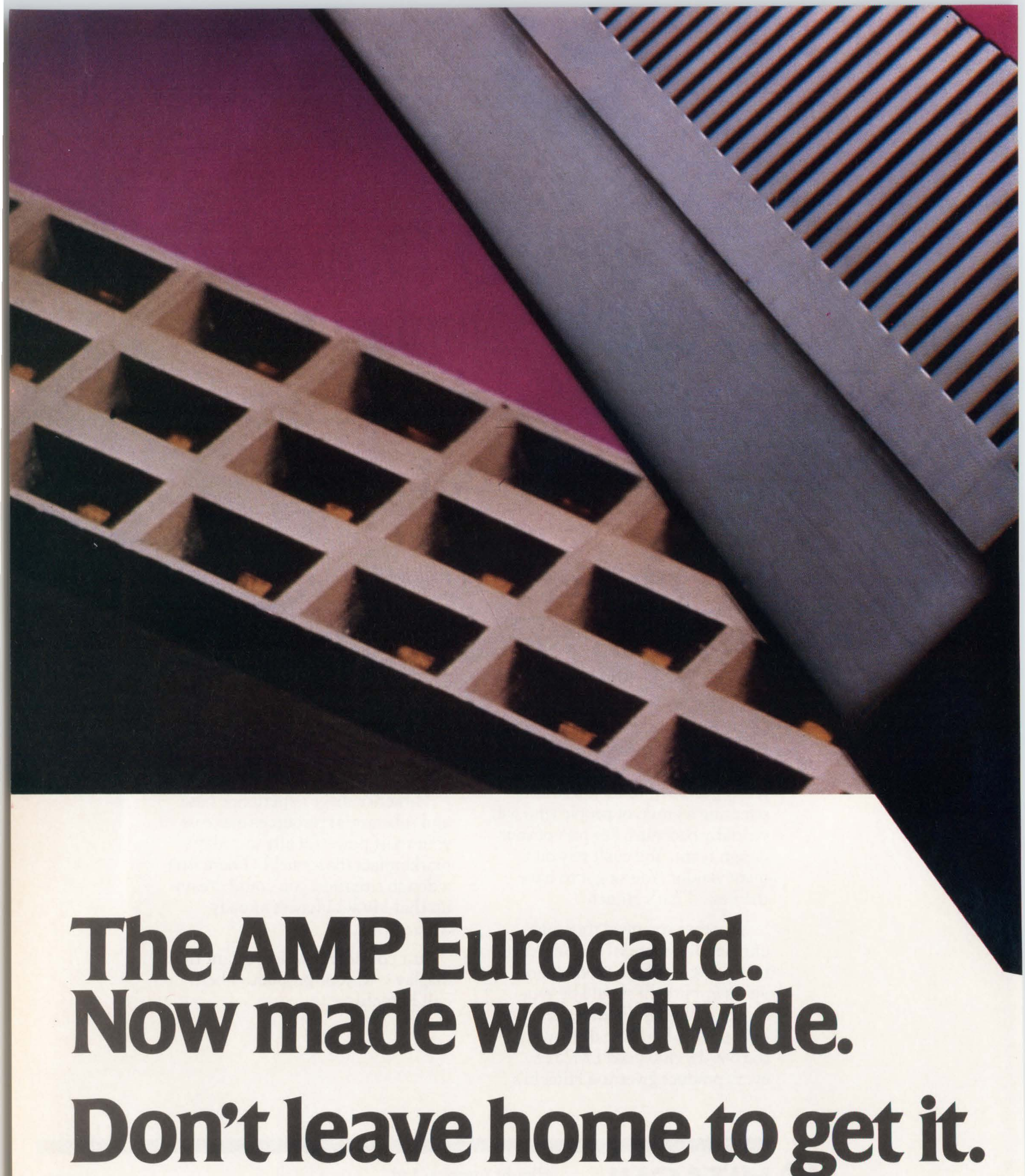
CIRCLE NO 115



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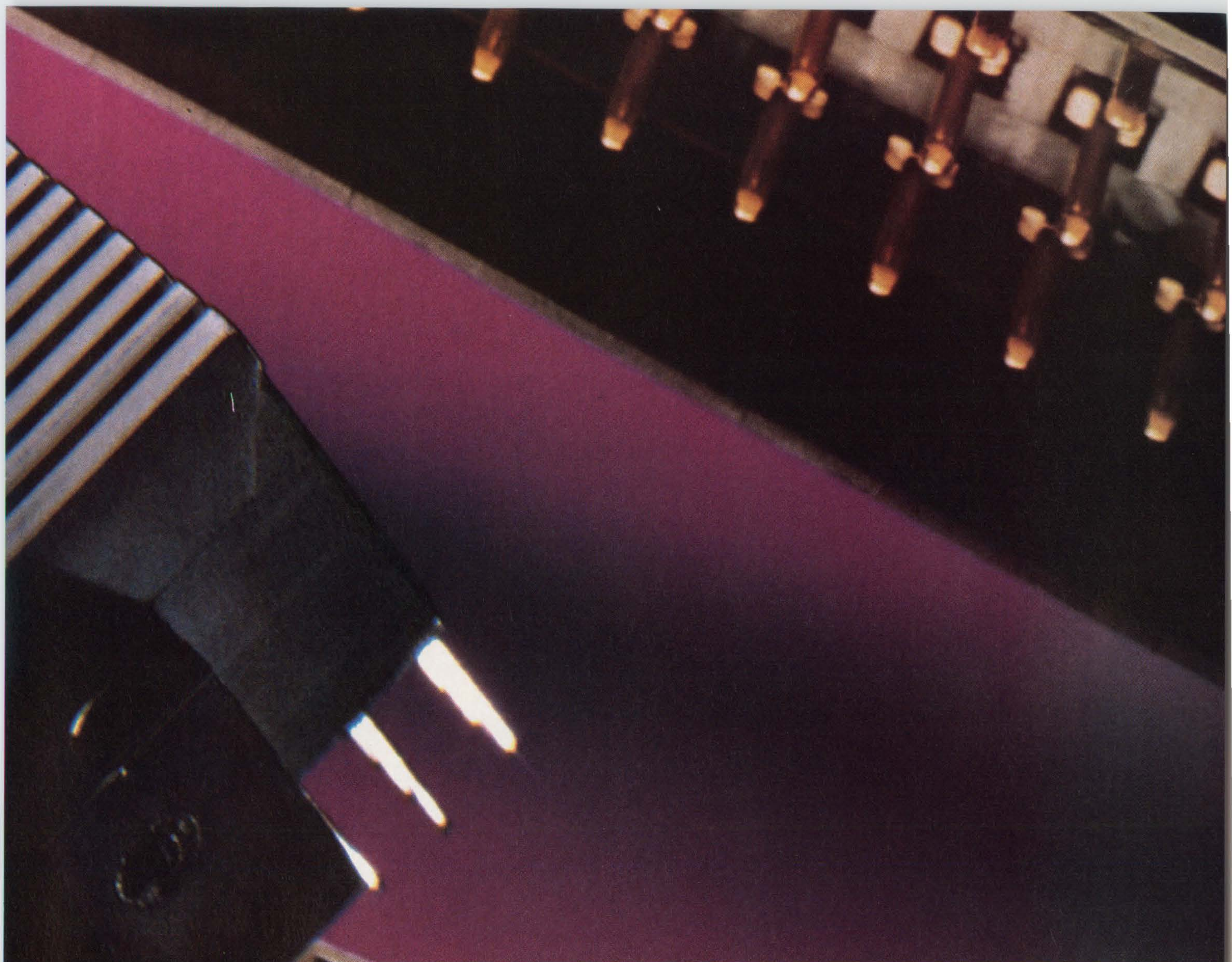

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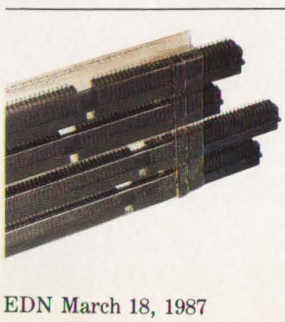

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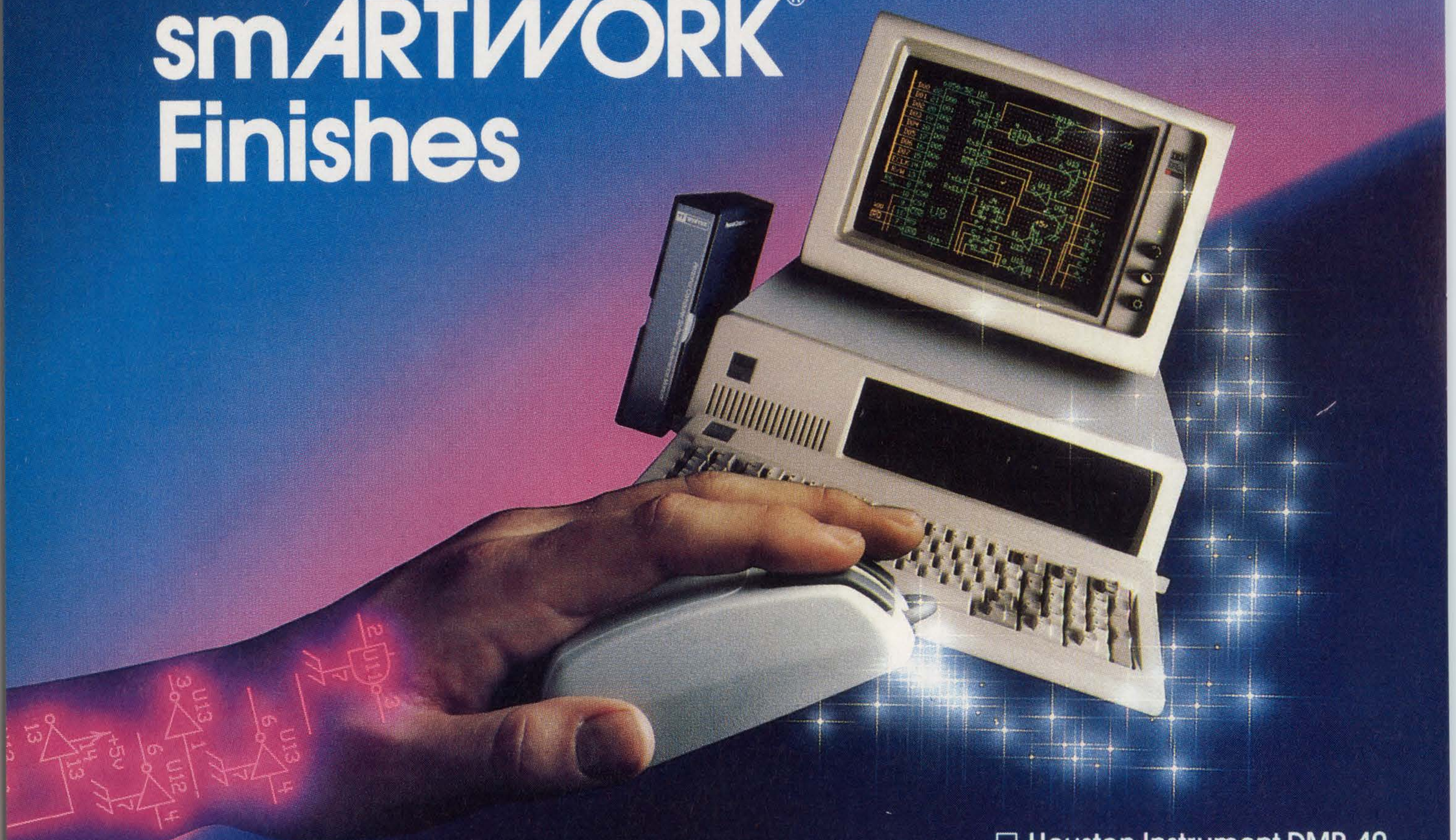

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CIRCLE NO 120

Optimize your graphics system for 2-D and 3-D

The design of a graphics system that's both 2-dimensional and 3-dimensional poses some conflicting requirements. You can reconcile some of these conflicts, however, through careful design of the frame-buffer structure, and you can achieve adequate speed for 3-D applications by using parallel processors for computation-intensive tasks.

Anoop S Khurana and Olivier Garbe,
Advanced Micro Devices Inc

A graphics system that will handle both 2- and 3-dimensional applications presents design requirements that are at odds with one another. These conflicts arise from the fundamental differences in the nature of the geometry-, pixel-, and display-processing tasks required by the two systems. A system with a microprogrammed architecture can help you avoid the difficulties you'd encounter in reconciling these differences.

You'd use a 2-D graphics system with such graphics editors as MacDraw, MacPaint, and Interleaf, or with CAE programs such as schematic-capture packages or layout editors for pc-board design. You'd need a 3-D system, on the other hand, to display 3-D wire-frame models, to model solids for mechanical design, or to produce visually pleasing 3-D pictures for animation.

One of the major differences lies in the size of the frame buffer needed, and the speed with which the host computer can obtain access to it. Most 2-D systems need only eight bits to define a pixel color as one of 256 simultaneously displayable colors. A 3-D system, on the other hand, needs eight bits each for red (R), green (G), and blue (B)—a total of 24 bits per pixel. Also, 2-D pixel-processing operations require fast access to multiple pixels during the same frame-buffer cycle. In a 3-D system, by contrast, pixel-processing operations (such as Gouraud shading) are computation-intensive but require access to only one pixel at a time.

Similarly, geometry-processing operations are more arithmetic-intensive in 3-D than in 2-D systems. Fixed-point, 32-bit arithmetic provides adequate computational power and speed for many 2-D applications, whereas 3-D applications need the speed and versatility of fast floating-point arithmetic.

Most of the graphics systems available today, including engineering workstations, are optimized for 2-D graphics operations; if they have 3-D capabilities, they perform the required processing mainly in software, which is slow. To obtain adequate speed, then, serious users of 3-D graphics find that they need a separate system that's optimized for 3-D graphics, resulting in an expensive duplication of hardware and software.

You can avoid these disadvantages by designing a single graphics system that provides all the features

A 2-dimensional graphics system can handle diagrams, but you need 3-dimensional capability for mechanical modeling.

necessary for both 2-D and 3-D graphics. You'll find a microprogrammed architecture ideal for such a system, because such an architecture lets you customize the data paths and computational resources to a particular application and to the performance level that you want. It also lets you integrate both fast integer and fast floating-point arithmetic capabilities, both of which are necessary for complex graphics operations, into a single system.

As an example of such a system, consider the design of a graphics peripheral for a conventional minicomputer. This peripheral can act as a bus master on the host's system bus, but it need not do so. The application program runs on the host computer and generates a display list, defining the image, which the CPU passes to the graphics peripheral via a DMA channel (or by any other appropriate means). The graphics peripheral processes this display list to generate the image. (The steps that convert a display list to an image on the screen are collectively referred to as the "graphics pipeline"; see **box,** "From object to image: the graphics pipeline.") The three main functional blocks of the system are the communications and display-list handler; an update processor that performs geometry and pixel processing; and a display controller **(Fig 1).**

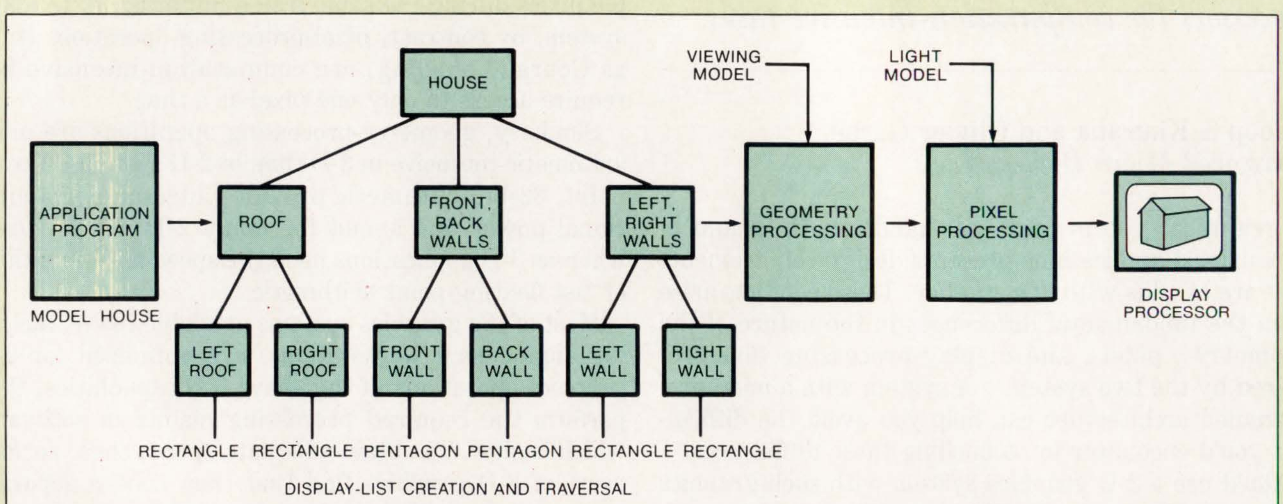
A conventional, general-purpose, 16- or 32-bit μP, which has its own memory and DMA channel, receives and executes commands issued by the host. This communications processor can directly execute some host commands, such as Load Display-List. Other commands, such as Render Display-List, involve the rest of the graphics system; the communications processor analyzes these commands and dispatches appropriate commands to the update processor, using a message-based protocol and a fast, dual-access memory block that serves as a mailbox.

From object to image: the graphics pipeline

The graphics pipeline is the sequence of operations that translates the user's description of a scene into a viewable image. The four stages in this process are display-list handling, geometry processing, pixel processing, and display control.

The display-list handler helps the user or the application program decompose objects to be depicted into a display list. The display list is usually hierarchical, and it embodies the structure inherent in the object being modeled. Leaf nodes in the hierarchy are drawing primitives provided by the graphics system.

The geometry processor performs viewing- and perspective-transformation operations on the display list, and it clips objects against the boundaries of the



The graphics pipeline consists of the processing steps *needed to convert a graphics object description, in digital form, into a viewable image on the screen.*

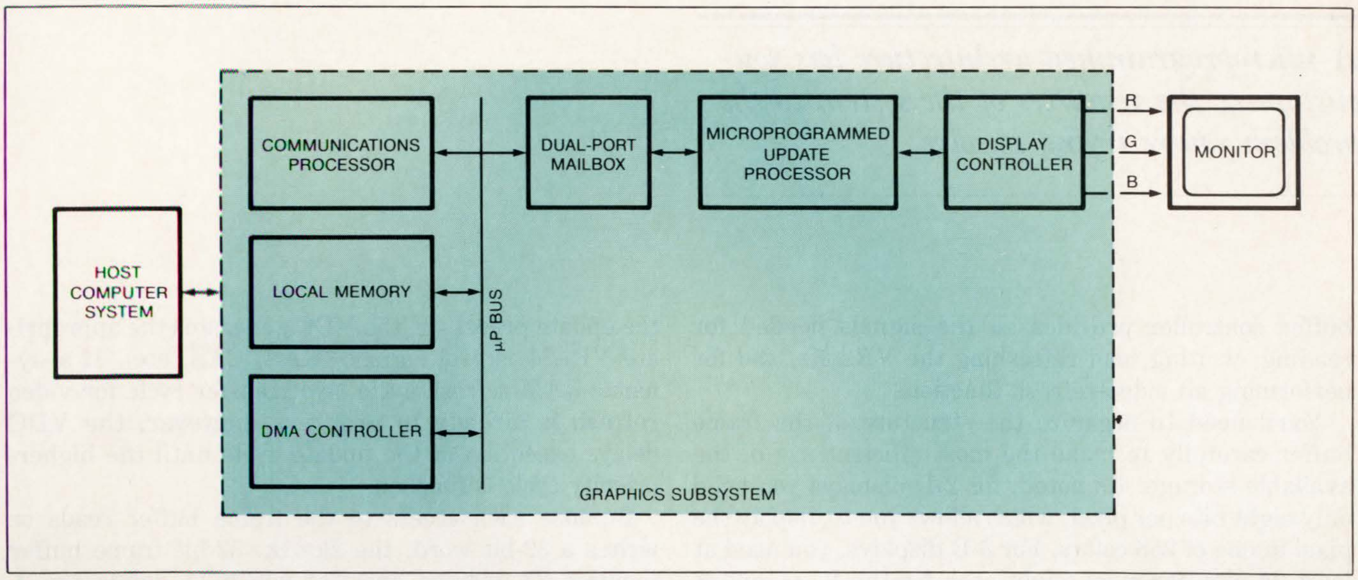


Fig 1—A graphics subsystem is ideally an intelligent peripheral *that accepts a display list from the host computer and converts the digital representation of an image into a standard video signal that creates a screen display.*

The dual ports of the mailbox allow the update processor to read a command while the communications processor is sending a subsequent command. Semaphores, also located in the mailbox RAM, govern both command chaining and the allocation of memory to message buffers.

The microprogrammed update processor executes all commands that are related to geometry or pixel processing. Such operations may update the pixel data in the frame buffer, or they may pass a message back to the communications processor.

The frame buffer uses video RAM (VRAM) ICs, both to maximize bandwidth and to minimize the quantity of hardware needed for refreshing the image. The frame-

viewing volume. You can decompose the complex primitives used by the geometry processor, such as patches or cubic curves, into simpler primitives, such as polygons or lines.

The pixel processor physically writes all the pixels affected by a primitive into their correct locations in the frame buffer. It also performs all operations, such as pixel-block transfers, that require pixels to be read from or written to the frame buffer.

The display controller converts the pixel values stored in the frame buffer into a standard video signal. This video signal, when transmitted to a suitable monitor, builds the desired image on the screen.

A single, general-purpose processor, such as the Intel 80286, along with the 80287 numeric coprocessor, can perform all the operations in the graphics pipeline sequentially. In such a system, the main processor writes the final value of each pixel to the frame buffer, which forms part of the address space of the main processor. This configuration is relatively slow, however, and the speed may be inadequate for 3-D applications.

You can achieve improved performance by using specialized VLSI peripheral devices, such as the Am95C60 Quad Pixel Dataflow Manager, to speed some of the operations in the graphics pipeline. Most current graphics peripherals relieve the main processor of most of the pixel-processing tasks. Typical functions performed by such peripherals are line drawing, polygon filling, and block transfer of pixels. Because these tasks are relatively standard and are well suited to implementation in high-performance silicon, graphics peripherals yield a substantial improvement in system performance. You can achieve a similar improvement by using high-performance floating-point processors to speed the computation-intensive geometry-processing tasks.

For even higher performance and functionality, you should consider the use of multiprocessing systems that provide one or more processors for each stage in the graphics pipeline. Two factors contribute to the improvement in performance that such systems yield. First, because most graphics operations are vector operations, the concurrent performance of several parts of a task can yield a speed increase that's proportional to the number of processors available. Second, you can fine-tune the system by customizing it for highest performance in just those operations that the applications require.

A microprogrammed architecture lets you customize the resources of the system to the problem you're trying to solve.

buffer controller provides all the signals needed for reading, writing, and refreshing the VRAMs, and for performing all video-refresh functions.

You'll need to organize the structure of the frame buffer carefully to make the most efficient use of the available storage. As noted, for 2-D displays you need only eight bits per pixel, which allows you to display the pixel in one of 256 colors. For 3-D displays, you need at least 24 bits per pixel (eight each for the R, G, and B channels); you may also need, for each pixel, an additional eight bits for the alpha channel and 16 or 32 bits for the Z buffer (a maximum of 64 bits/pixel).

You can reduce the total number of bits per pixel by mapping the Z buffer into a portion of the frame buffer. For example, in a 2k-pixel×1k-line buffer, you could map a 1k×1k-pixel screen into the first 1k pixels of each line and the Z buffer into the second 1k pixels. Consequently, you could access the Z value of a pixel by adding an offset of 1024 to the pixel address. You would need two memory cycles to access both the RGB and the Z values of the pixel. This structure, however, has the great advantage that no bits are irrevocably dedicated to the Z buffer. If you don't need a Z buffer, this memory becomes available for general use.

You'll still have to resolve the discrepancy between the eight bits/pixel needed for 2-D and the 24 bits/pixel needed for 3-D. Your first thought might be to allocate a 32-bit memory word for each pixel, but then you'd be wasting 24 bits in 2-D operations. A better solution is to allow each 32-bit word to be treated as four adjacent 8-bit pixels in 2-D. You could then reorganize a 2k×1k×32-bit memory as a frame buffer of 8k×1k×8 bits. This organization allows you to store one 3-D screen with a resolution of 1024 pixels×1024 lines×32 planes, or several 2-D screens at once.

The frame buffer in our example consists of 64k×4-bit VRAMs and uses the shifter port of each VRAM for video refreshing; the update processor therefore has virtually unlimited access to the frame buffer. It's possible to organize each VRAM as a 256×256×4-bit square area of memory; using this area as a building block, you can create a 2k×1k×4-bit memory array having four rows and eight columns **(Fig 2)**. If you want to extend the depth of the array to 32 bits/pixel, you'll need eight VRAMs in each element (called a bank) of the array.

The video display controller (VDC) provides complete control of the frame buffer, both for update operations and for video-refresh operations. In response to a read or write memory-cycle request from the update processor, the VDC generates the appropriate VRAM-control signals ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, etc). If a dynamic-RAM refresh cycle or a transfer cycle for video refresh is already in progress, however, the VDC delays execution of the update cycle until the higher-priority cycle is finished.

Because each access to the frame buffer reads or writes a 32-bit word, the 2k×1k×32-bit frame buffer requires 21 address lines, of which 11 define the X address and the other 10 define the Y address within the array. In the 3-D 32-bit/pixel mode, each 32-bit word in the frame buffer represents one pixel.

In the 2-D 8-bit/pixel mode, each 32-bit word represents four pixels. The 18 most significant address bits select the 8-bit row address, the 8-bit column address, and $\overline{\text{RAS}}$ strobe signals. Decoding the three least significant bits yields a decode signal that selects one of eight adjacent pixels.

The capacitive loading imposed by the VRAMs makes it necessary to buffer the address and control outputs of the display controller. To reduce skew between signals, and thereby achieve a shorter memory-cycle time, you can buffer the address, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and XF/G signals within a single IC package, such as the Am2976 11-bit dynamic memory driver used in this example.

Select one of eight pixels

Each of the eight rows in the frame memory receives a separate $\overline{\text{RAS}}$ signal. You can therefore connect to a common 32-bit bus the data ports of all four banks of VRAMs within a column. Each memory cycle now gives access to eight pixels, one from each column. The update processor operates on only 32 bits at a time, however, so you'll need a mechanism to select just one of the eight available words.

You can perform this 8:1 multiplexing quite simply by decoding the three least significant address bits to obtain the $\overline{\text{CAS}}$ signal. As a result, only one bank in memory receives both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Consequently, you can tie together the outputs of all 32 banks in memory, but only the selected bank will drive the bus. To access eight sequential pixels, then, you'd need eight memory cycles.

There's another way to perform the multiplexing, however—one that gives the update processor very rapid random access to any or all of the eight adjacent pixels addressed in a single memory cycle. This method requires eight 32-bit, bidirectional, bus-interface registers. You connect the eight 32-bit words, accessed in parallel from the memory, independently to one port of

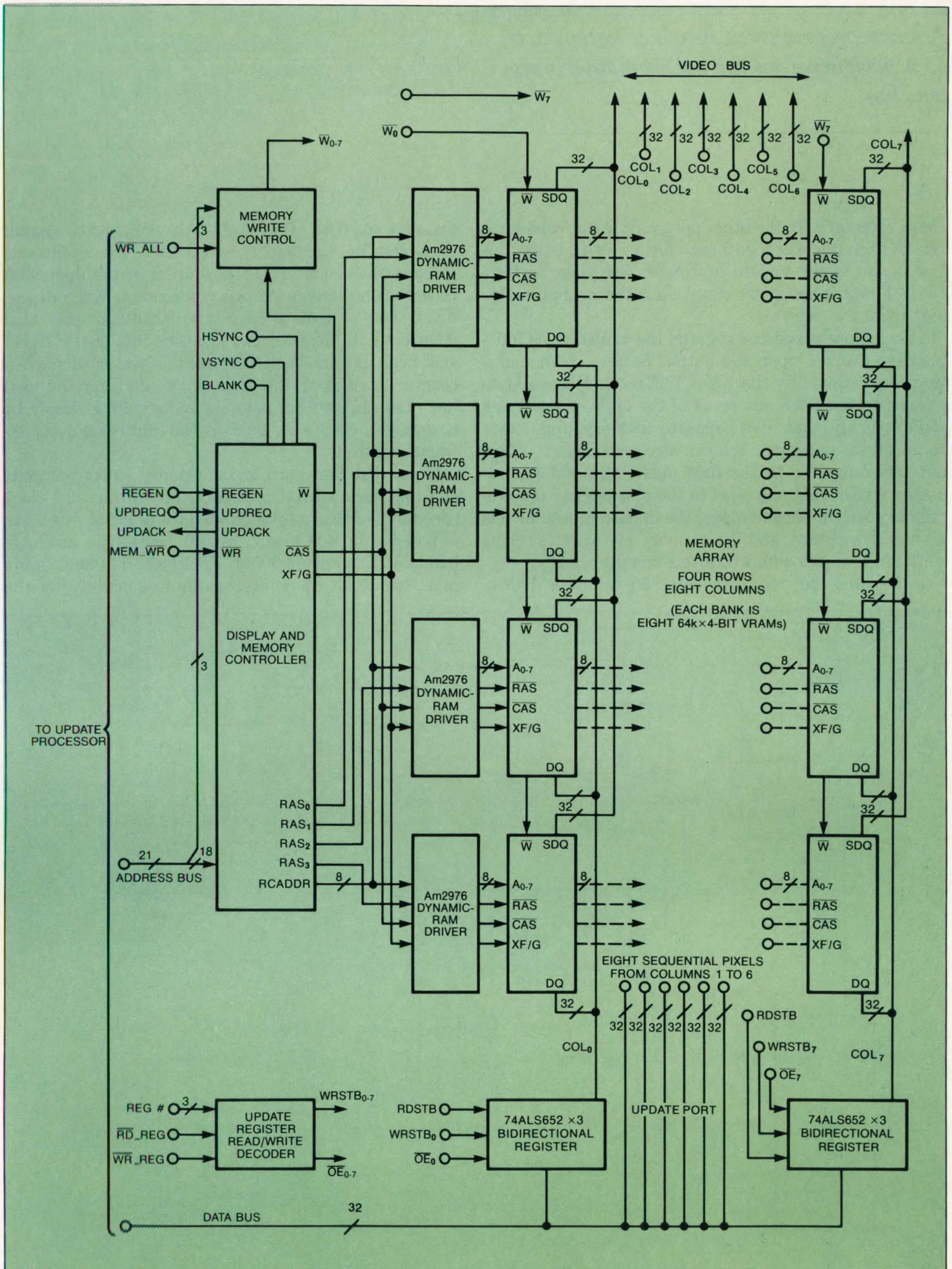


Fig 2—This frame buffer is organized as 2k pixels×1k lines×32 bits. *Three-dimensional applications can read or write eight adjacent pixels at one time. For 2-D applications, each 32-bit word represents four 8-bit pixels.*

A microprogrammed graphics system acts as a peripheral on the host computer's system bus.

these registers. To the other port you tie corresponding bits of each register together to form a single 32-bit bus that leads to the update processor. You then perform the 8:1 multiplexing by controlling the output-enable signals of the registers.

The update processor regards the registers as independent 8-pixel input and output buffers. A memory-read operation fills the input buffer, and the update processor can fetch any or all of the eight pixels much more quickly than if a separate memory cycle were required for each one. You can also provide two different write modes. In the first mode, the update processor writes just one pixel to the appropriate place in memory. In the second mode, the update processor fills all eight registers, and the memory cycle writes their contents to eight different pixels simultaneously.

Refreshing the video display is easy when the display memory consists of VRAMs. At every vertical-sync (Vsync) pulse, the display controller resets an internal video-refresh counter to the address of the upper-left corner of the screen. At every horizontal-sync (Hsync) pulse, the controller initiates a transfer cycle that transfers data for the next scan line into the VRAMs' shift registers and then increments its internal address counter to point to the start of the data for the next line. You can perform panning and scrolling simply by changing the address held in the controller's top-of-frame register.

Given that there are eight memory banks per row, and that each VRAM is capable of shifting at a clock speed of 25 MHz, a total bandwidth of 200M pixels/sec is possible in 3-D mode. In 2-D mode, the available bandwidth becomes 800M pixels/sec. The maximum pixel bandwidth is therefore limited mainly by the

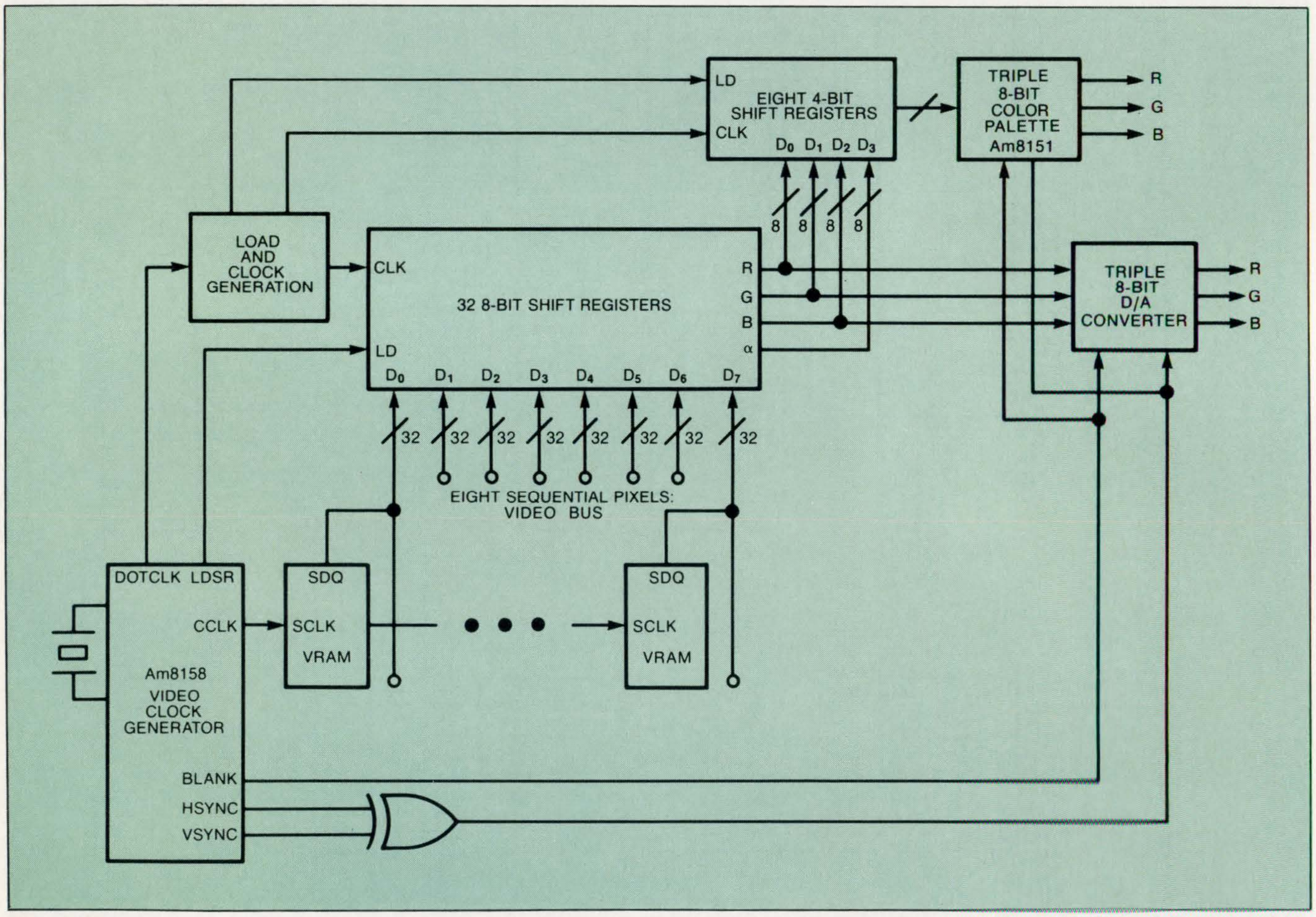


***Fig 3—You'll need two video shift registers** if you want to reconfigure the frame buffer from 32-bit, 3-D pixels to 8-bit, 2-D pixels or vice versa. The main register handles eight sequential 32-bit pixels; the secondary register reformats the RGB bit streams from the main register into RGB streams representing 8-bit pixels.*

characteristics of the shift registers and the associated D/A converter, not by those of the memory.

In 32-bit/pixel mode, strobe signals generated by the video clock generator—in this example, an Am8158—load into the video shift registers the eight sequential 32-bit pixels that are in parallel on the video bus (**Fig 3**). The video shift registers consist of 16 dual, 8-bit, parallel-in, serial-out ECL shift-register ICs. These ICs produce serial bit streams of the R, G, and B values of each pixel and forward these bit streams to a triple 8-bit D/A converter.

In 8-bit/pixel mode, the 32 bits that appear at the R, G, and B outputs of the shift registers actually represent four pixels. Four 4-bit ECL shift registers convert the 32-bit data into four 8-bit pixels for use by the Am8151 ECL color palette. To change from one mode to the other, you need only make the appropriate modifications to the Shift and Load signals to the shift registers.

The Am8158 generates the pixel clock pulse and some of the Shift and Load signals used by the shift registers. This IC also generates the Vsync, Hsync, and Blank pulses. The display controller uses these signals to initiate VRAM transfer cycles, and the D/A converters use them to force the video signals to the appropriate sync or blank levels. You can program all the important parameters of these signals using registers contained in the Am8158.

The update processor is microprogrammed

The update processor performs all pixel- and geometry-processing functions for both 2-D and 3-D graphics. These functions require powerful and versatile data-transfer capability coupled with fast integer and floating-point arithmetic. Implementing the update processor as a microprogrammed subsystem allows you to achieve the high performance that you need.

The major functional blocks and buses of the update processor are shown in **Fig 4.** The main data path in this example consists of the Am29332 integer ALU, the Am29323 integer multiplier, and the vector floating-point arithmetic unit, which consists of two Am29325 ICs. Each of these units accepts data from two common 32-bit input buses and places its results on one common 32-bit output bus (the main data bus).

An Am29334 register file provides storage for frequently accessed data. Its read ports supply data to the arithmetic unit's input buses. It also has two write ports, one of which accepts data from the main data bus, while the other transfers the result of an ALU operation back to the register file without using the main data bus. The system timing is such that the ALU can fetch two operands from the register file, process them, and write the result back to the register file within a single microcycle.

The update processor addresses 64k 32-bit words of high-speed local data memory, which consists of static RAM. An Am2131 dual-port message-buffer IC occupies 1k words of the 64k-word address space. To allow the main ALU to process video data at maximum efficiency, an auxiliary Am29C101 16-bit ALU performs all local-memory address computation; the outputs of this ALU are captured in a 16-bit address register. Random accesses to local memory therefore take two microcycles—one to compute and latch the address, and another to access the RAM. During consecutive memory accesses, however, next-word computation overlaps the current RAM access, so that the second and subsequent memory accesses are completed in a single microcycle.

The frame-buffer-address generator consists of presettable up/down counters (an 11-bit counter for the X address and a 10-bit counter for the Y address). The sequencer loads these counters via the main data bus. Although the main ALU is primarily responsible for generating frame-buffer addresses, use of the counters speeds the critical loops in curve drawing and other pixel-processing functions.

The update processor is configured with a single level of pipelining, so that next-address computation overlaps execution of the current microinstruction. The Am29331 sequencer computes the address of the next instruction in response to its instruction inputs, and it places the result on its Y output bus. For access to sequential microcode addresses, this result is simply the contents of the program counter. The sequencer uses an internal stack to store count values for nested loops and return addresses for calls to microcode subroutines.

To execute a jump to an address defined by the microcode, the sequencer connects the address section of the microinstruction word back into its program counter via the A bus. To allow the computation of jump addresses at run time, and to allow external examination of the sequencer's stack and stack pointer, the D bus connects to the main system bus.

An internal condition-code multiplexer, controlled by microcode, selects and enables one of the condition inputs of the sequencer; the sequencer can then test that condition and jump according to the state of the

The organization of the frame buffer is the key to resolving conflicts between 2-D and 3-D requirements.

selected input. For testing as many as four conditions simultaneously, a PAL device accepts all the signals that need to be tested simultaneously and encodes them into four fields of four bits each. A base address is assigned to each field, and the state of the field defines one of 16 sequential locations as an offset from the base address. The sequencer can then examine one of these fields and jump to the location defined by the state of that field. You can use this capability to advantage in a line-clipping algorithm.

In the 2-D mode, one of the most important pixel-processing operations is the movement of a rectangular block of pixels from one area of the frame buffer to another. This process, also known as BitBlt, may also require the execution of a logical operation during the transfer. The update processor transfers data one row at a time from the source block to the destination block. Within a row, the processor may transfer data either left to right or right to left. The sole reason for including the feature that provides fast access to eight pixels in the frame buffer is to speed block transfer. In the 32-bit/pixel mode, the algorithm that transfers one row of the source block to the corresponding row in the destination block has four steps, as illustrated in **Fig 5a** and described as follows:

- Read memory with X=24. This operation transfers pixels 24 through 31 into the frame buffer's read registers. Next, read pixels 31 and 32 into the register file. Then read memory again with X=32. Read five pixels (32 through 36) into the register buffer. You have now transferred the first seven pixels from the source region into the register file (there are only seven valid pixels in the first destination read cycle).
- Read memory with X=96. This operation trans-

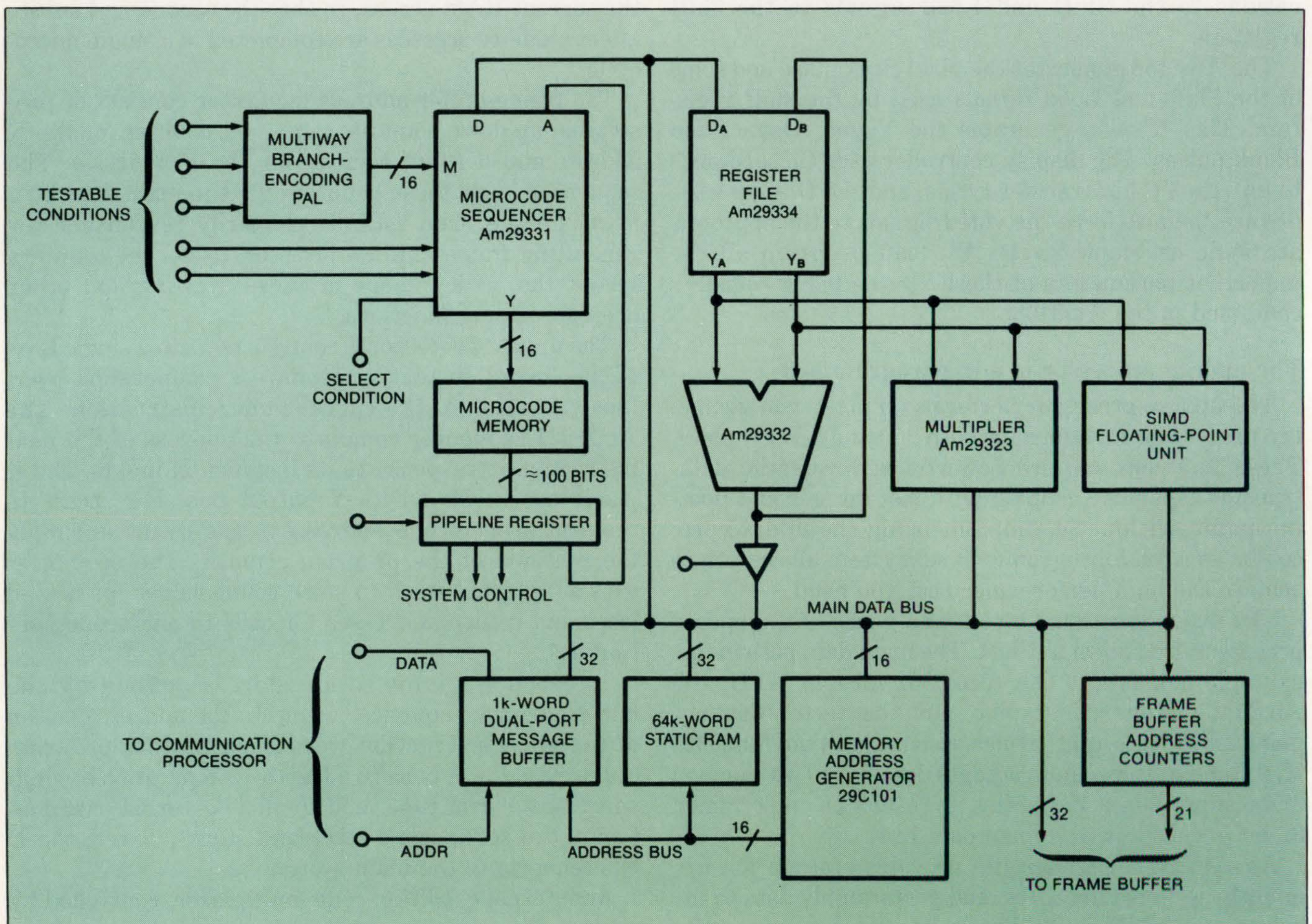


***Fig 4—This update processor,** which handles all geometry- and pixel-processing operations, uses a microprogrammed sequencer for control and parallel floating-point processors for vector operations.*

fers seven valid destination pixels into the frame buffer's registers.

- Read each valid destination pixel, one at a time, and perform any required logical operation with the corresponding source pixel in the register file. Write the resulting pixel back into the frame buffer's write registers. Copy each unread destination pixel from the input register to the output register.
- Write the eight destination pixels in the output registers back to memory. Repeat the sequence until you have transferred the entire row.

Assuming that a memory-read cycle takes 300 nsec and that each frame-buffer read or write operation takes 100 nsec, the total transfer time is 500 nsec/pixel. Using this algorithm, an average covering all possible alignments of source and destination turns out to be approximately 600 nsec/pixel. This time is a substantial improvement over the time of 1200 nsec/pixel for the case in which each memory cycle accesses a single pixel, and it's an acceptable data-transfer speed for 32-bit pixels.

In the 8-bit/pixel mode, the block-transfer algorithm must take into account different alignments of the source and destination within a 32-bit word, and it requires a modification of the procedure. The modified algorithm, illustrated in **Fig 5b,** is as follows:

- Read source words 1 and 2 simultaneously from both output ports of the register file. Using the Am29332 funnel shifter, extract four bytes aligned with the destination, and write this 32-bit word back to a temporary location in the register file. In the example shown, you need to extract the last three pixels of word 1 and pixel S2 from word 2.
- Read this aligned source location, using one register-file port. Read the destination pixel from the frame buffer via the main bus into the second register-file port.
- Perform the logical operation on the aligned-source and destination pixels, using the mask generated internally by the ALU; doing so leaves the first pixel unchanged by the logical operation. Write the result, which appears at the ALU's outputs, back to the frame buffer's input registers at the end of the cycle.

Step 3 of the algorithm now takes three microcycles per word instead of two, and it changes the average transfer time to just over 600 nsec per word. Because each word contains four pixels, the average pixel-transfer time is $600 \div 4 = 150$ nsec/pixel. This pixel-transfer rate allows an entire 1k×1k-pixel screen to be updated in 150 msec, or about 10 frame times, and is

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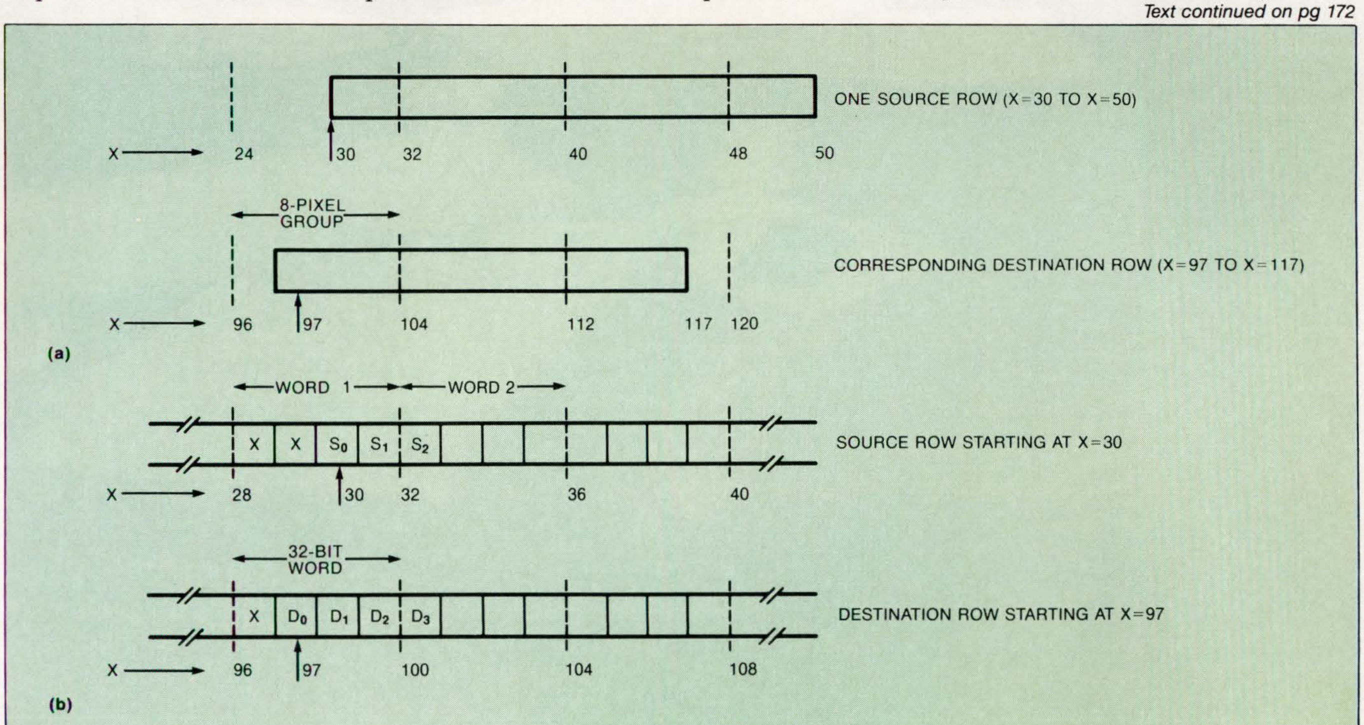

Fig 5—Pixel block-transfers need careful alignment *of the source and destination within a group of pixels. In 32-bit/pixel mode* ***(a)****, the group is eight pixels wide. In 8-bit/pixel mode* ***(b)****, the group is four pixels wide.*

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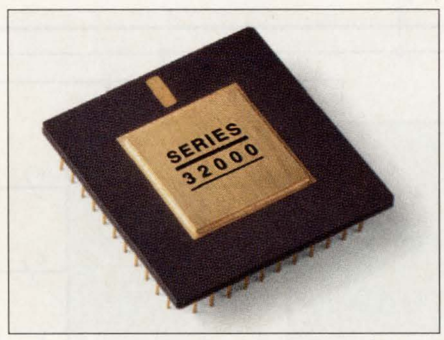

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The update processor needs fast access to several pixels at a time in the frame buffer.

sufficient for displaying text and manipulating windows.

It's not difficult to implement line- and circle-drawing algorithms, such as those of Bresenham, in microcode. The inner loop of Bresenham's line-drawing algorithm will require three microcycles. Because this time is equal to the time needed to access a pixel in the frame buffer, you can plot pixels at the pixel-access speed of the memory. However, because this algorithm does not profit from the fast access to sequential pixels, the plotting speed will be about the same in both the 32-bit/pixel and the 8-bit/pixel modes. The inner loop of Bresenham's circle-drawing algorithm will require four microcycles, and because each iteration through the loop generates eight points that must be plotted in separate memory cycles, circles too are drawn at the rate of about one pixel in every frame-buffer access time.

Typical pixel- and geometry-processing operations in a 3-D system are computation-intensive and require that you carefully consider the design of the arithmetic unit. Integer arithmetic, although fast, is unsuitable for these graphics operations. Fixed-point arithmetic has disadvantages as well. Although you can readily perform most pixel-processing functions using 32-bit fixed-point arithmetic, fixed-point geometry-processing operations require time-consuming pre- and postscaling operations. For this reason, floating-point operations are easier to develop and are more general in character. Furthermore, there are now many inexpensive floating-point chips, which are almost as fast as integer units and provide all the computation power you need.

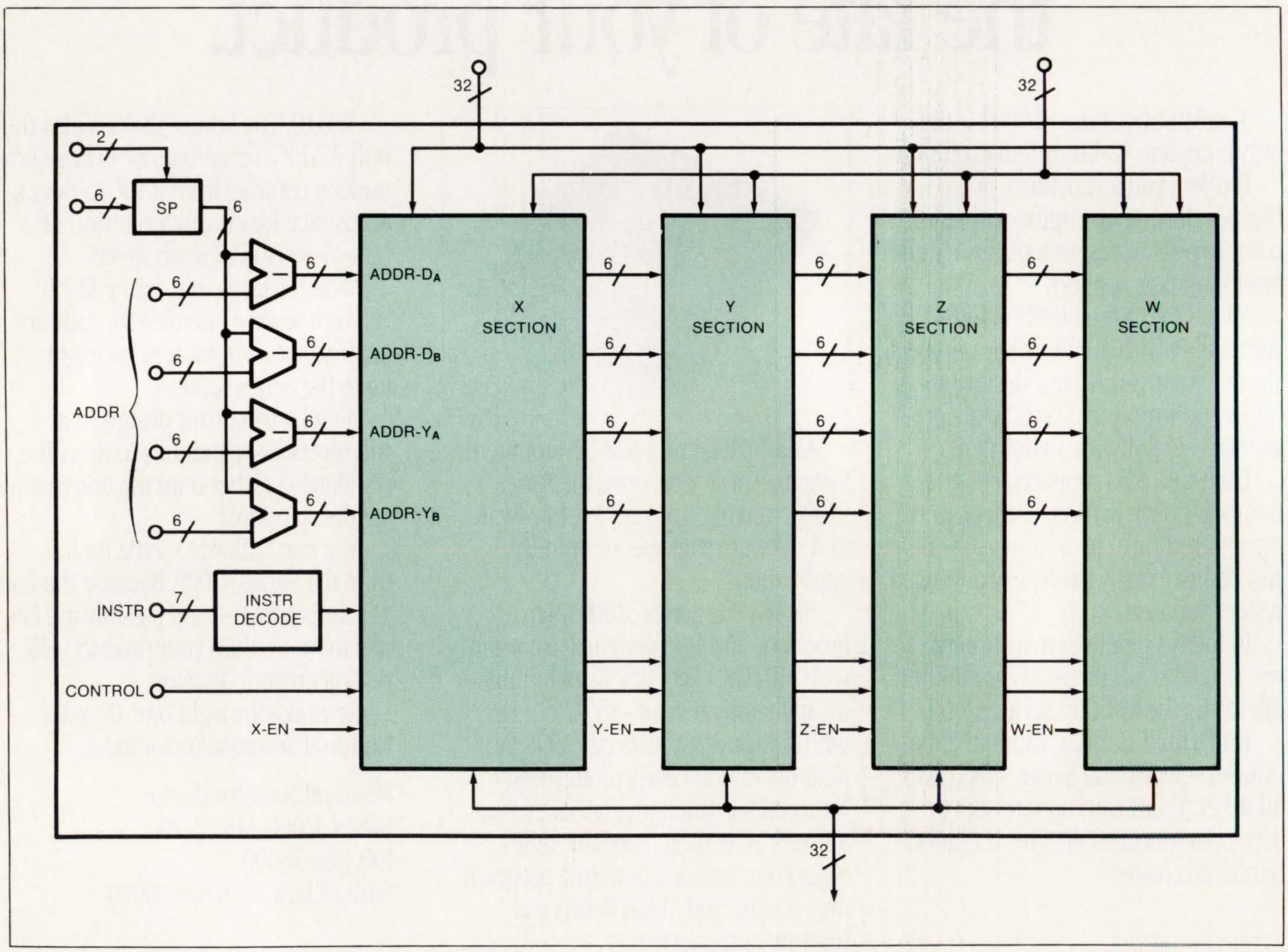

Fig 6—This SIMD floating-point unit has four sections *that share a common control bus. All four sections concurrently perform the same operation on different data.*

TABLE 1—TRANSFORMATION OF A 3-D POINT

CYCLE	EXECUTE	READ/WRITE
1		READ: Y_A=R=ST(0), Y_B=S=ST(4)
2	EXECUTE: F=R * S	READ: Y_A=R=ST(1), Y_B=S=ST(5)
3	EXECUTE: R=R * S	
4	EXECUTE: F=F+R	READ: Y_A=R=ST(2), Y_B=S=ST(6)
5	EXECUTE: R=R * S	
6	EXECUTE: F=F+R	READ: Y_A=R=ST(3), Y_B=S=ST(7)
7	EXECUTE: R=R * S	
8	EXECUTE: F=F+R	
9		WRITE: D_A=F, OUTPUT REGISTER=F (OPTIONAL)

In a graphics system, most of the arithmetic computations are vector operations, because points, plane-equations, transformation matrices, and other common data structures are all vectors. For example, you can represent a point in 3-D space, in homogeneous form, as the vector (x y z w). Although a single processor can perform vector operations sequentially, a multiple-processor system that uses four ICs (in this example, Am29325s) is much faster. If you can distribute the computation tasks among the four processors in such a way that you keep each processor busy all of the time, you can expect to achieve four times the performance of a single processor.

Fortunately, it's quite easy to distribute the simple vector operations that are useful in graphics. For example, perspective division on a point (x y w z) in homogeneous coordinates yields (x/w y/w z/w 1). Consequently, you can perform these divisions in parallel on four different processors, and you can arrange for algorithms that do not map onto such an architecture to run (though more slowly) on a single processor as a sequence of scalar operations. Furthermore, the fact that all processors perform the same operation (division, in this example) at the same time (but on different data) suggests that you should design the floating-point unit as a single-instruction, multiple-data (SIMD) machine, whose processors share a common instruction bus.

You can see the overall structure of a 4-processor SIMD floating-point unit in **Fig 6.** Each section consists of a floating-point processor, a register file, and a seed ROM **(Fig 7).** In each section, a 64-word area of the stack constitutes the register file, and you can address data in the register file with a 6-bit negative displacement from the stack pointer. The microcode word therefore contains four 6-bit fields to specify the addresses of the four ports on the register file. The stack-addressing capability allows microcode subroutines to be completely general in character, and if you first load the stack pointer with zero, you can use the microcode-word displacement fields to specify absolute addresses.

The seven instruction bits of the main microcode word, when decoded, provide all the output-enable and multiplexer-select signals needed to reflect all possible arithmetic-operation and source/destination combinations. Twenty-four bits specify the addresses for the four ports of the register file, two bits control write operations on the D_A and D_B ports of the register file, and one bit switches the source-select multiplexer located at the register file's D_A input. Two additional bits determine whether the stack pointer is to be left unchanged, incremented, decremented, or loaded from the data bus.

A data-access microcycle consists of three time slots. In the first slot, the address hardware computes register-file addresses by adding the displacement specified in the microcode word to the current contents of the stack pointer. In the second slot, data is written into the register file. In the last slot, data required for the next execution cycle is read from the register file.

The pipelined structure of the floating-point unit allows the overlapping of arithmetic operations with operations that access data from the register file. As a rule, the floating-point unit must access data from the register file one microcycle before using that data in an arithmetic operation. In many cases, however, the data needed for the next operation is already held in the Am29325's internal registers, so that a register-access cycle is unnecessary. Furthermore, most graphics operations allow execution cycles to overlap data-access cycles in a similar manner. Consequently, the effective throughput of the floating-point unit remains close to one operation per microcycle.

Guidelines for coding typical operations

As an example of how you can distribute portions of an operation among the four processors, consider the transformation of a 3-D point in homogeneous coordinates, using a ×4 matrix. The first step is to broadcast all four coordinates of the point to be transformed, and to write them into the register files of all four sections of the floating-point unit simultaneously. Because the register file also acts as the matrix stack, the transformation matrix is already established in the floating-point unit. You then distribute the transformation matrix among the four sections, storing only one column of the matrix in each section.

Assume that the point to be transformed is on top of the stack at [ST(0) ST(1) ST(2) ST(3)], and that the matrix column is at [ST(4) ST(5) ST(6) ST(7)], where ST(n) refers to the data n words down from the current stack pointer. You perform the transformation by computing the dot product of the point and a column of the transformation matrix. You can now compute, in parallel, the four dot products needed to transform each

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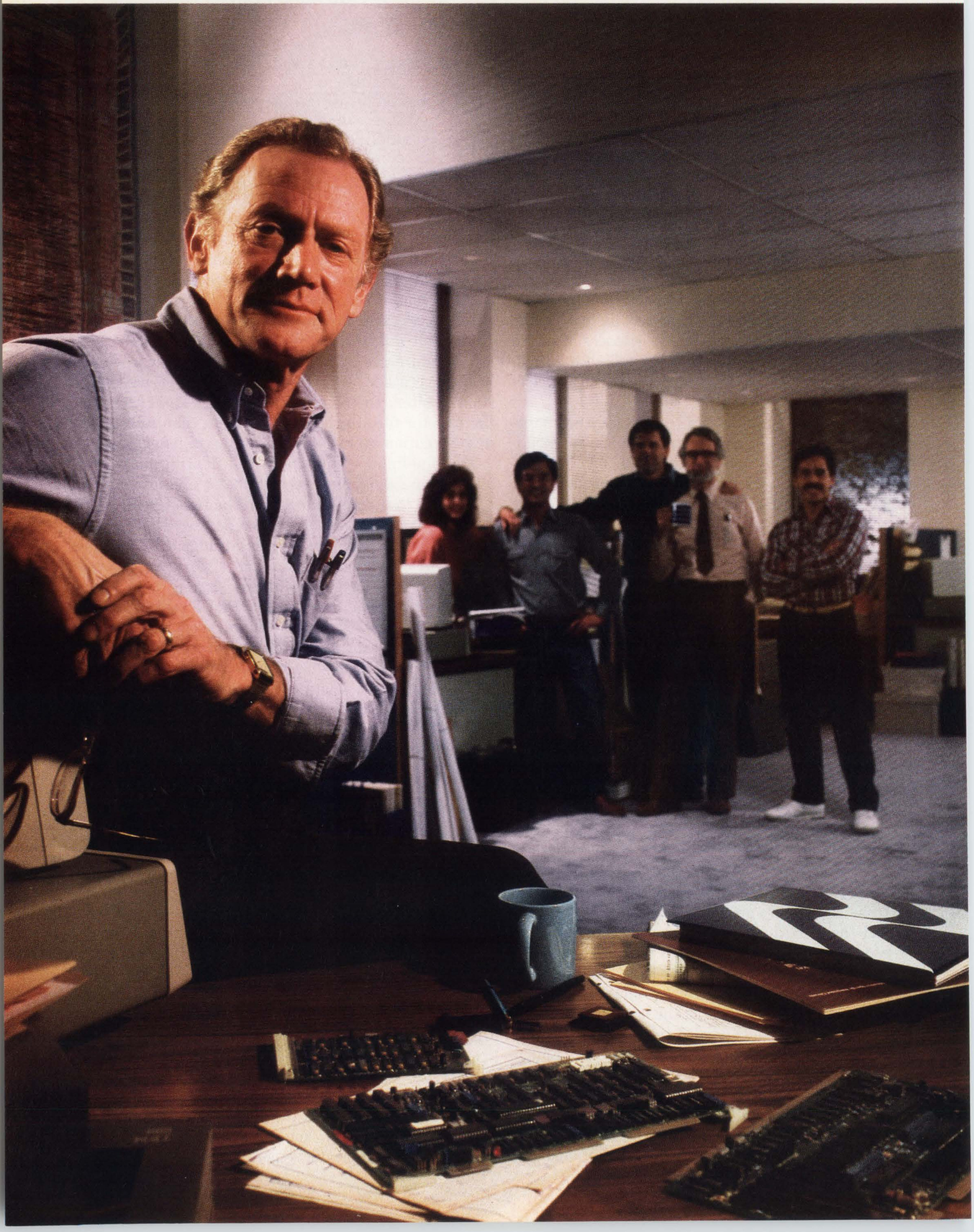

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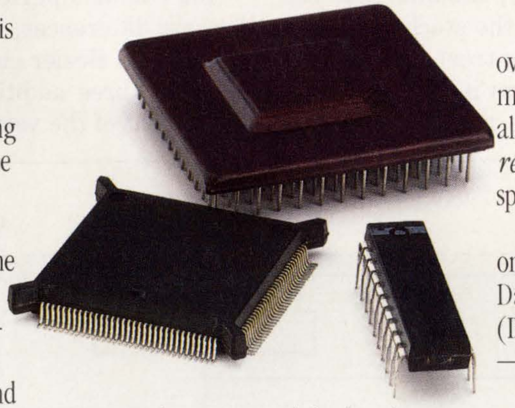

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The update processor is configured with a single level of pipelining, so that next-address computation overlaps execution of the current microinstruction.

component of the vector, one in each section of the floating-point unit. The entire transformation can complete within nine microcycles **(Table 1)**.

You can use the same approach to perform matrix-matrix multiplication. In this case, assume that the current transformation is on top of the stack, with one column in each section. You can now treat a row of the new matrix as a point and transform it by the matrix held on top of the stack to yield a row of the transformed matrix. You repeat this procedure four times (once for each row) to obtain the complete result. A matrix-matrix multiplication therefore takes 36 microcycles.

You can also perform parallel interpolation, using forward differences, when drawing cubic curves such as splines and Bezier curves. In this case, each iteration requires three addition operations, and because each component of the vector requires an identical computa-

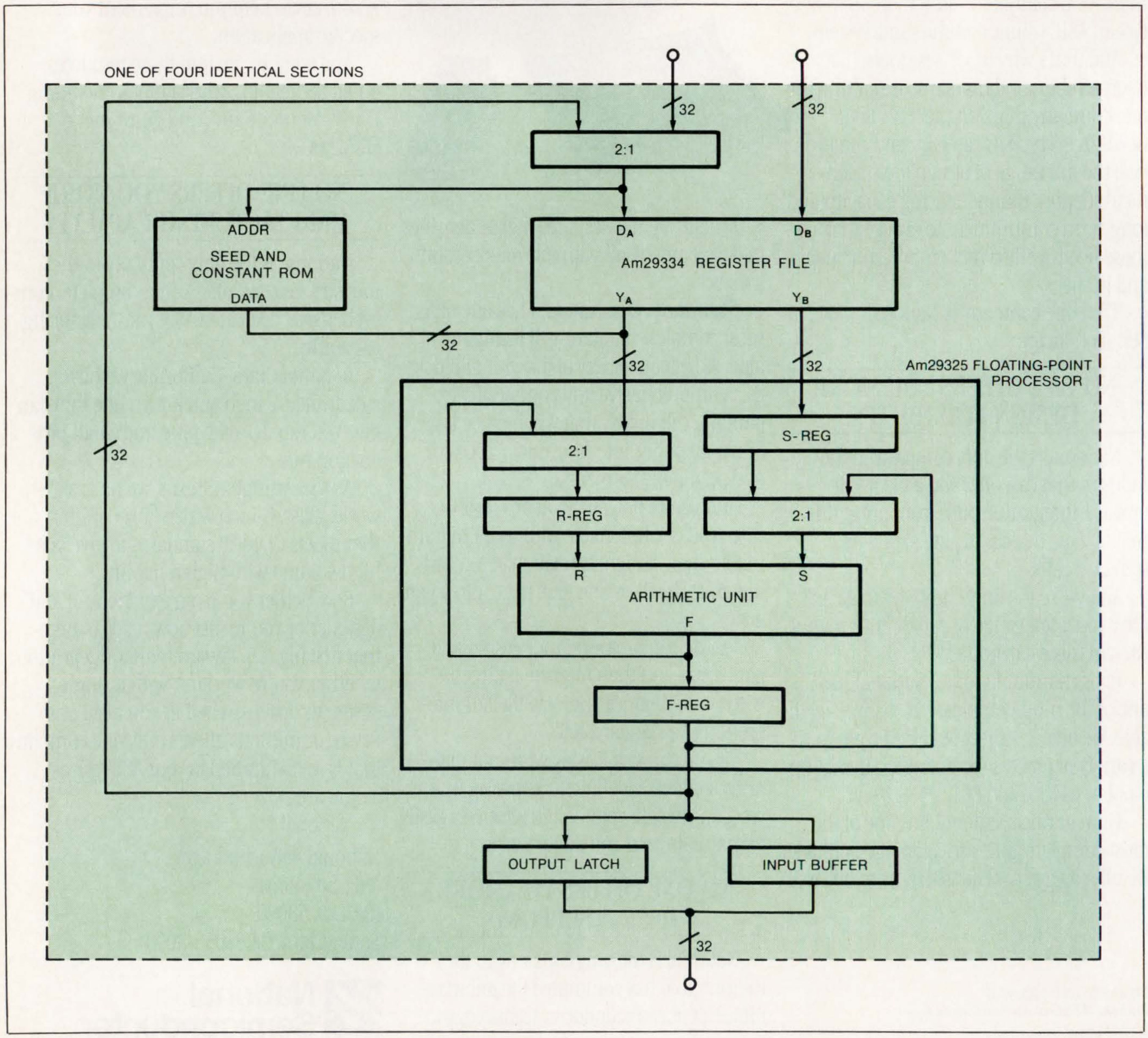

Fig 7—Each section of the SIMD floating-point unit is identical *with the others, and each has its own register file, seed and constant table, and floating-point processor.*

tion, you can perform the four computations in parallel in the four sections. Consequently, you can compute a new point every four microcycles. In the computation shown below, D_X, D_{2X}, and D_{3X} are the first-, second-, and third-order forward differences for the X coordinate:

$$[X\ D_X\ D_{2X}\ D_{3X}]=[X\ D_X\ D_{2X}\ D_{3X}]+[D_X\ D_{2X}\ D_{3X}\ 0]$$

$$[Y\ D_Y\ D_{2Y}\ D_{3Y}]=[Y\ D_Y\ D_{2Y}\ D_{3Y}]+[D_Y\ D_{2Y}\ D_{3Y}\ 0]$$

$$[X\ D_Z\ D_{2Z}\ D_{3Z}]=[Z\ D_Z\ D_{2Z}\ D_{3Z}]+[D_Z\ D_{2Z}\ D_{3Z}\ 0]$$

Perspective division requires a division operation, and the normalization of an interpolated vector, in the inner loop of Phong shading, requires square-root operations. The Am29325 does not perform division and square roots directly, however. Instead, it uses Newton-Raphson iteration to obtain the corresponding results. The seed ROM provides the seed (or first approximation) to start the iteration procedure. Each iteration requires three microcycles for division and five microcycles for square roots. Refining the seed to approximately single-precision accuracy requires another three microcycles. Consequently, each division operation requires a total of ten microcycles, and each square-root operation requires sixteen microcycles. Furthermore, because each processor in the floating-point unit has its own seed table, four such computations can proceed in parallel. **EDN**

Author's biography

Anoop S Khurana is a product planning engineer for advanced graphics at Advanced Micro Devices (Sunnyvale, CA). He's responsible for specifying architectures for peripheral graphics controllers. He holds a BSEE from the University of Roorkee in India and an MSEE from the University of Florida (Gainesville). His hobbies include squash, reading, and hiking.

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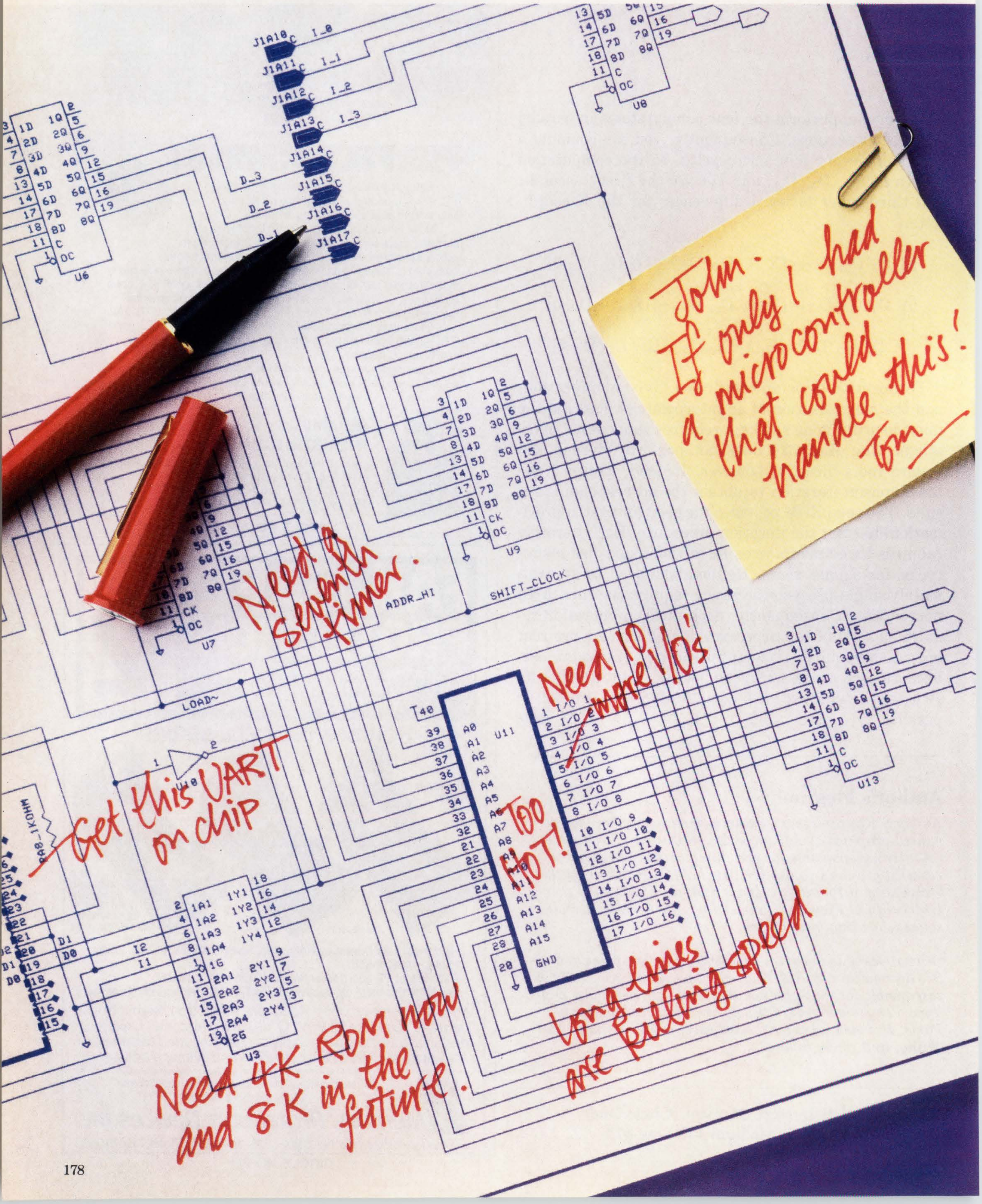

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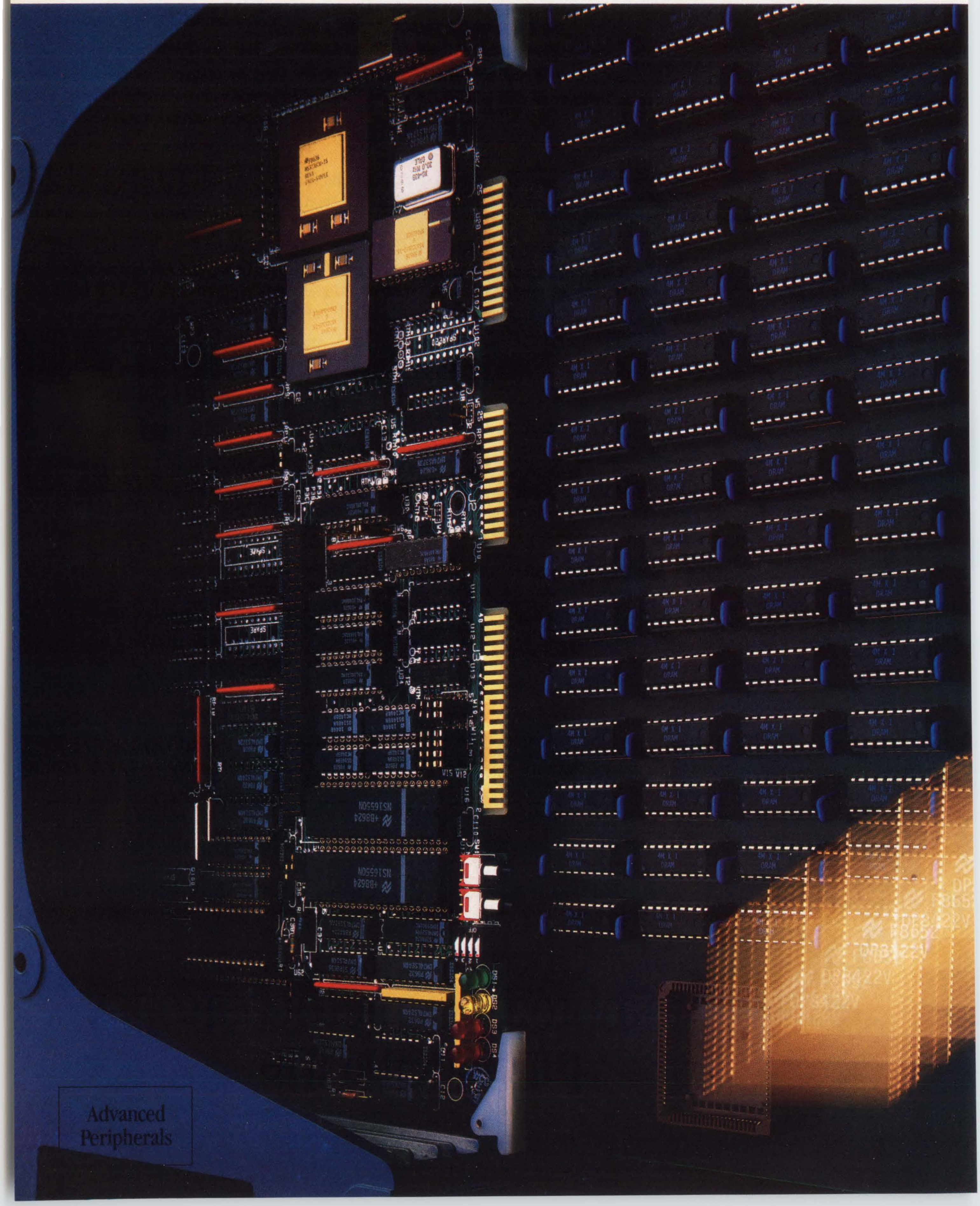

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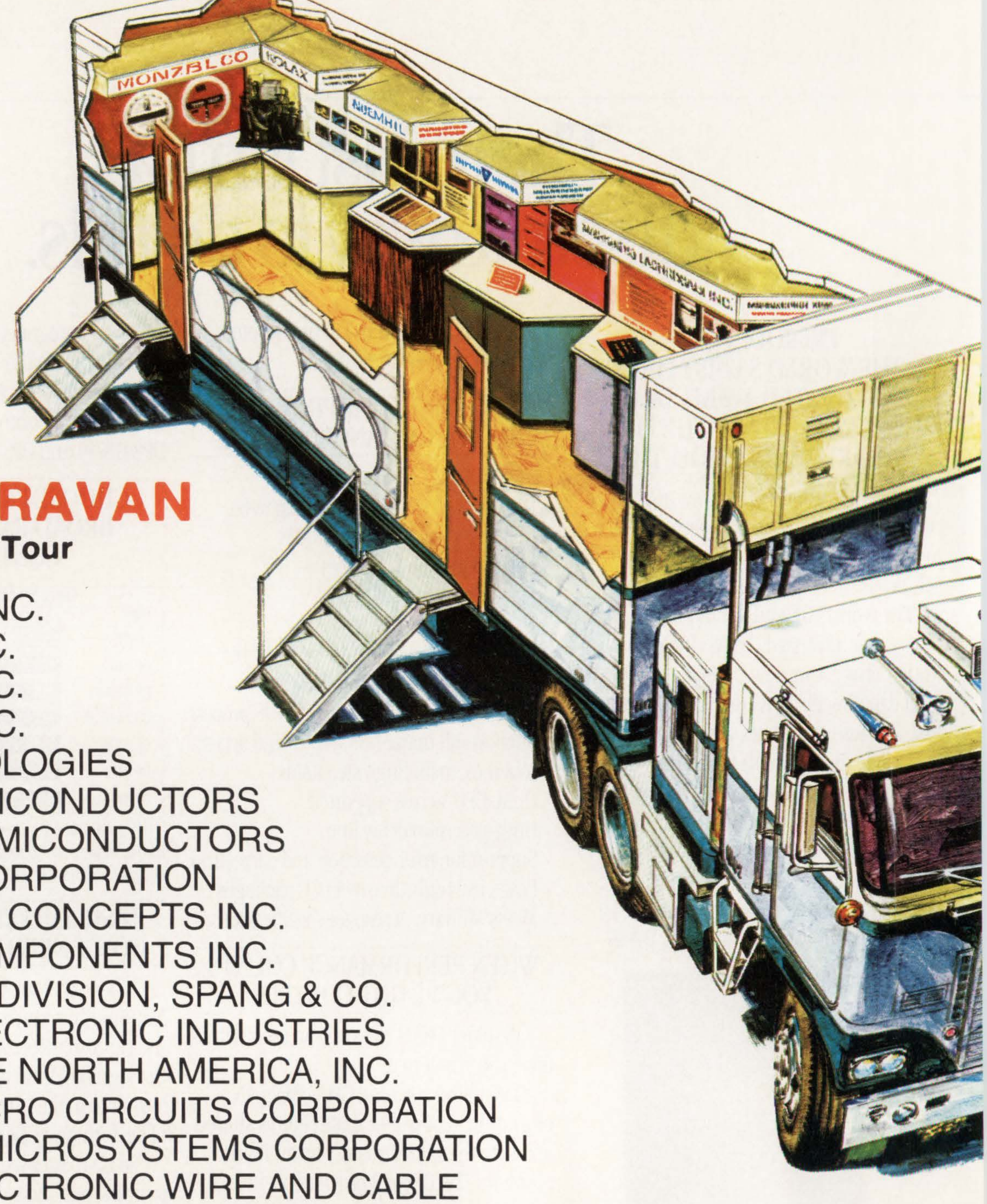

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1987 WESTERN EDN CARAVAN TRAVELING ELECTRONIC SHOW
March 23 to May 1 (last half)

DATE	TIME	SITE
3/23 Monday	9-11:30 AM	SPERRY FLIGHT SYSTEMS 2111 N. 19th Ave., Phoenix, AZ
3/23 Monday	1:30-3:30 PM	SIEMENS TRANSMISSION SYSTEMS 2500 W. Utopia Rd., Phoenix, AZ
3/24 Tuesday	9-12 AM	MOTOROLA GOVERNMENT ELECTRONICS 8201 E. McDowell Rd., Scottsdale, AZ
3/24 Tuesday	1-2:30 PM	MOTOROLA RADAR SYSTEMS 2100 E. Elliot Rd., Tempe, AZ
3/24 Tuesday	3-4:30 PM	MOTOROLA STRATEGIC ELECTRONICS 2501 S. Price Rd., Chandler, AZ
3/25 Wednesday	9-11 AM	IBM CORPORATION Rita Rd., Tucson, AZ
3/25 Wednesday	12:30-3:30 PM	HUGHES AEROSPACE COMPANY Negales Hwy., Tucson, AZ
3/27 Friday	9-12 AM	SANDIA NATIONAL LABS Kirtland AFB, Albuquerque, NM
3/27 Friday	1:30-4 PM	SPERRY AEROSPACE AND MARINE GROUP 9201 San Mateo Blvd. NE, Albuquerque, NM
3/30 Monday	9-11 AM	HEWLETT-PACKARD COMPANY 3404 E. Harmony Rd., FT. Collins, CO
3/30 Monday	1:30-3 PM	HEWLETT-PACKARD COMPANY 700 71st Ave., Greeley, CO
3/31 Tuesday	9-11 AM	HEWLETT-PACKARD COMPANY 815 14th SW, Loveland, CO
3/31 Tuesday	1-3 PM	BALL AEROSPACE SYSTEMS Boulder Industrial Park, Boulder, CO
4/1 Wednesday	9-11 AM	IBM CORPORATION 6300 Diagonal Hwy., Boulder, CO
4/1 Wednesday	1-3 PM	AT&T INFORMATION SYSTEMS LABS 11900 N. Pecos St., Denver, CO
4/2 Thursday	9-10:30 AM	MARTIN MARIETTA CORPORATION Hwy 470, Waterton, CO
4/3 Friday	9-11 AM	DIGITAL EQUIPMENT CORPORATION 301 Rockrimmon Blvd., Colorado Springs, CO
4/3 Friday	1-3 PM	HEWLETT-PACKARD COMPANY 1900 Garden of Gods, Colorado Springs, CO
4/6 Monday	8:30-11:30 AM	GENERAL DYNAMICS CORPORATION Grants Lane, Ft. Worth, TX
4/6 Monday	2-4 PM	E-SYSTEMS INCORPORATED 1200 Jupiter Rd., Garland, TX
4/7 Tuesday	8:30-10 AM	TEXAS INSTRUMENTS INCORPORATED Forest Lane, Dallas, TX
4/7 Tuesday	10:30-12 AM	TEXAS INSTRUMENTS INCORPORATED 13500 N. Central Exwy., Dallas, TX
4/7 Tuesday	2-4 PM	LTV AEROSPACE AND DEFENSE 1902 W. Freeway, Dallas, TX
4/8 Wednesday	8-9:30 AM	TEXAS INSTRUMENTS INCORPORATED 2501 S. Hwy. 121, Lewisville, TX
4/8 Wednesday	10:45-12 AM	TEXAS INSTRUMENTS INCORPORATED Central Expwy., McKinney, TX
4/8 Wednesday	2-4 PM	E-SYSTEMS INCORPORATED Farm Rd. 1570, Greenville, TX
4/9 Thursday	8:30-10 AM	ROCKWELL INTERNATIONAL CORPORATION 1200 N. Alma Rd., Richardson, TX
4/9 Thursday	10:45-12 AM	ROCKWELL INTERNATIONAL CORPORATION Shiloh Rd., Richardson, TX
4/10 Friday	9-12 AM	IBM CORPORATION 11400 Burnet Rd., Austin, TX
4/10 Friday	1-3 PM	TRACOR INCORPORATED 6500 Tracor Lane, Austin, TX
4/13 Monday	9-11:30 AM	BOEING MILITARY AIRPLANE COMPANY 3801 S. Oliver, Wichita, KS
4/13 Monday	1:30-3 PM	NCR CORPORATION 3718 N. Rock Rd., Wichita, KS
4/14 Tuesday	9-11 AM	KING RADIO CORPORATION 400 N. Rogers Rd., Olathe, KS
4/15 Wednesday	9-11:30 AM	ROCKWELL INTERNATIONAL CORPORATION 400 Collins Rd. NE, Cedar Rapids, IA
4/15 Wednesday	1-3 PM	ROCKWELL INTERNATIONAL CORPORATION 855 35th St. NE, Cedar Rapids, IA
4/16 Thursday	9-11:30 AM	IBM CORPORATION Hwy. 52 and NW 37th St., Rochester, MN
4/16 Thursday	2-3:30 PM	E. F. JOHNSON COMPANY 299 Johnson Ave. SW, Waseca, MN
4/17 Friday	9-11 AM	CONTROL DATA CORPORATION 3101 E. 80th St., Minneapolis, MN
4/20 Monday	8:30-10 AM	HONEYWELL DEFENSE SYSTEMS Country Rd. 18, Edina, MN
4/20 Monday	10:45-12 AM	MAGNETIC PERIPHERALS INCORPORATED 5950 Clearwater Dr., Minvetonka, MN
4/20 Monday	2-4 PM	HONEYWELL AVIONICS 2600 Ridgeway Pkwy., Minneapolis, MN
4/21 Tuesday	8:30-10 AM	HONEYWELL INCORPORATED 1625 Zarthan Ave., St. Louis Pk., MN
4/21 Tuesday	10:30-12 AM	HONEYWELL INCORPORATED Olson Memorial Hwy., St. Louis Pk., MN
4/21 Tuesday	2-4:30 PM	UNISYS CORPORATION Univac Park, St. Paul, MN
4/22 Wednesday	8:30-9:30 AM	UNISYS CORPORATION 2276 Highcrest Rd., Rosenville, MN
4/22 Wednesday	10:45-12 AM	CONTROL DATA CORPORATION 4201 N. Lexington Ave., St. Paul, MN
4/22 Wednesday	2-3:30 PM	3M COMPANY 3M Center, St. Paul, MN
4/23 Thursday	9-10:30 AM	NICOLET INSTRUMENT CORPORATION 5225 Verona Rd., Madison, WI
4/23 Thursday	1-2:30 PM	G. E. MEDICAL SYSTEMS 3000 N. Grandview Blvd., Wankesha, WI
4/23 Thursday	3:15-4:30 PM	G. E. MEDICAL SYSTEMS 16800 Ryerson Rd., New Berlin, WI
4/24 Friday	9:30-11 AM	JOHNSON CONTROLS INCORPORATED 507 E. Michigan Ave., Milwaukee, WI
4/24 Friday	1-3 PM	ALLEN BRADLEY COMPANY 1201 S. 2nd St., Milwaukee, WI
4/27 Monday	9-11 AM	SUNSTAND CORPORATION 4747 Harrison Ave., Rockford, IL
4/27 Monday	1-3 PM	BARBER COLMAN COMPANY 1354 Clifford Ave., Rockford, IL
4/28 Tuesday	9-11 AM	NORTHROP DEFENSE SYSTEMS 600 Hicks Rd., Rolling Meadows, IL
4/28 Tuesday	1-2:30 PM	MOTOROLA INCORPORATED 1500 W. Dundee Rd., Arlington Hts., IL
4/28 Tuesday	3:15-4:30 PM	NORTHROP DEFENSE SYSTEMS 2525 Buffe Rd., Elk Grove Village, IL
4/29 Wednesday	9-11:30 AM	ZENITH ELECTRONIC SYSTEMS 1000 Milwaukee Ave., Glenview, IL
4/29 Wednesday	1:30-4 PM	MOTOROLA INCORPORATED 1301 E. Algonquen Rd., Naperville, IL
5/1 Friday	8:30-10 AM	AT&T TECHNOLOGIES 2600 Warrensville Rd., Lisle, IL
5/1 Friday	10:30-12 AM	TELLABS INCORPORATED 4951 Indiana Ave., Lisle, IL
5/1 Friday	2-3:30 PM	ROCKWELL INTERNATIONAL WESCOM 8245 Lemont Rd., Downers Grove, IL

Fast-settling op amps aid in data conversion

When you use an op amp to buffer a high-speed data-conversion device, you must match the speed of the op amp to that of the D/A or A/D converter you're using. Unless your op amp's settling-time characteristics are comparable to those of the converter, the converter's fast performance will be wasted.

Charles Kitchin, Scott Wurcer, and Lew Counts,
Analog Devices Semiconductor

To take advantage of a fast DAC's speed and precision, you need to buffer it with an op amp that provides comparable performance. The op amp's dc noise characteristics mustn't bury the DAC's output, and the op amp must settle quickly, so that the voltage output you've created corresponds to the DAC's current output and is not just an artifact of the op amp's settling time.

You should pay equal attention to op-amp settling time when you're buffering the inputs of successive-approximation A/D converters. The op amp will require some finite portion of time to recover from the current switching that the A/D converter is performing at the op amp's output. If the recovery time is too long, the ADC will convert not the true buffered voltage, but a voltage that has been affected by the ADC itself.

Current-output, 12-bit D/A converters, such as the AD565A, which requires only 250 nsec to settle to within ½ LSB, have been available for several years. Very often, though, your system will require a voltage output rather than the current output that these devices provide, so you need to use an op amp to effect the necessary current-to-voltage conversion. However, many monolithic op amps require six times as long (1.5 μsec) to settle to 0.01% (½ LSB). Using one of these op amps would be counterproductive; you'd effectively waste the fast performance of the converter.

You can buffer the DAC without wasting its performance by matching the specifications of the buffer amplifier to those of your DAC. **Fig 1** shows an AD565A DAC using an AD711 op amp as an output buffer. The AD711's performance is comparable to that of the DAC (see **box**, "The AD711 family of op amps"). The DAC's output resistance is modeled by the 8-kΩ resistor connected between the DAC's output and the analog common terminals. The 10-pF capacitor connected between the summing junction and the output of the amplifier compensates for both the DAC's output capacitance and the amplifier's 5-pF input capacitance. Note, however, that although this schematic uses a 10-pF capacitor (a standard fixed value) for C_1, a 7.8-pF capacitor would provide the fastest settling.

The scope photo in **Fig 2** (pg 188) shows the output voltage of the AD711 for a transition from +10 to 0V. The vertical scale of the photo is 5 mV/div, which translates to 2 LSB/div. Note that the output settles to within ½ LSB of its final value in 1 μsec.

The 8-kΩ output resistance of the DAC is shunted by

An op amp used as a DAC buffer must settle quickly, so that its voltage output corresponds to the DAC's current output and isn't affected by the op amp's settling time.

the 9.95-kΩ bipolar offset resistor connected in series with the 100Ω trim resistor. This combination produces an effective output resistance of 4.4 kΩ. When you use the full 10-kΩ feedback resistance available in the DAC to obtain a 20V output span, the dc noise gain is 3.25 because the noise is modeled at the positive input of the op amp and is therefore amplified by the transfer function $1+(R_F/R_{OUT})$. The worst-case offset drift of the op amp, 10 μV/°C, will therefore contribute 32.5 μV/°C to the output of the amplifier. Over the full 0 to 70°C temperature range, offset drift will cause a 700-μV error voltage to appear at the amplifier's output. This error voltage amounts to less than 0.3 LSB for a 12-bit DAC with a 20V output swing.

The initial offset voltage of the op amp, specified at 0.5 mV, would contribute 1.65 mV to the output if it weren't trimmed out with the bipolar-offset-adjust resistor, R_1. The additive effects of offset drift and an initial, untrimmed, offset voltage could present as much as 2.35 mV at the output of the amplifier. This offset voltage is greater than ½ LSB, and it effectively negates the benefits of the fast-settling 12-bit converter. If you carefully trim out the initial offset voltage, however, you can take advantage of the DAC's 12 bits of accuracy.

Because the noise gain is greater than 2.0, you can reduce the settling time of the above circuit to 500 nsec by substituting an AD744 for the AD711. The AD744 features a 50V/μsec slew rate and a 12-MHz bandwidth. When you use the AD744, you may substitute a smaller feedback capacitor (between pins 2 and 6 of the op

Text continued on pg 188

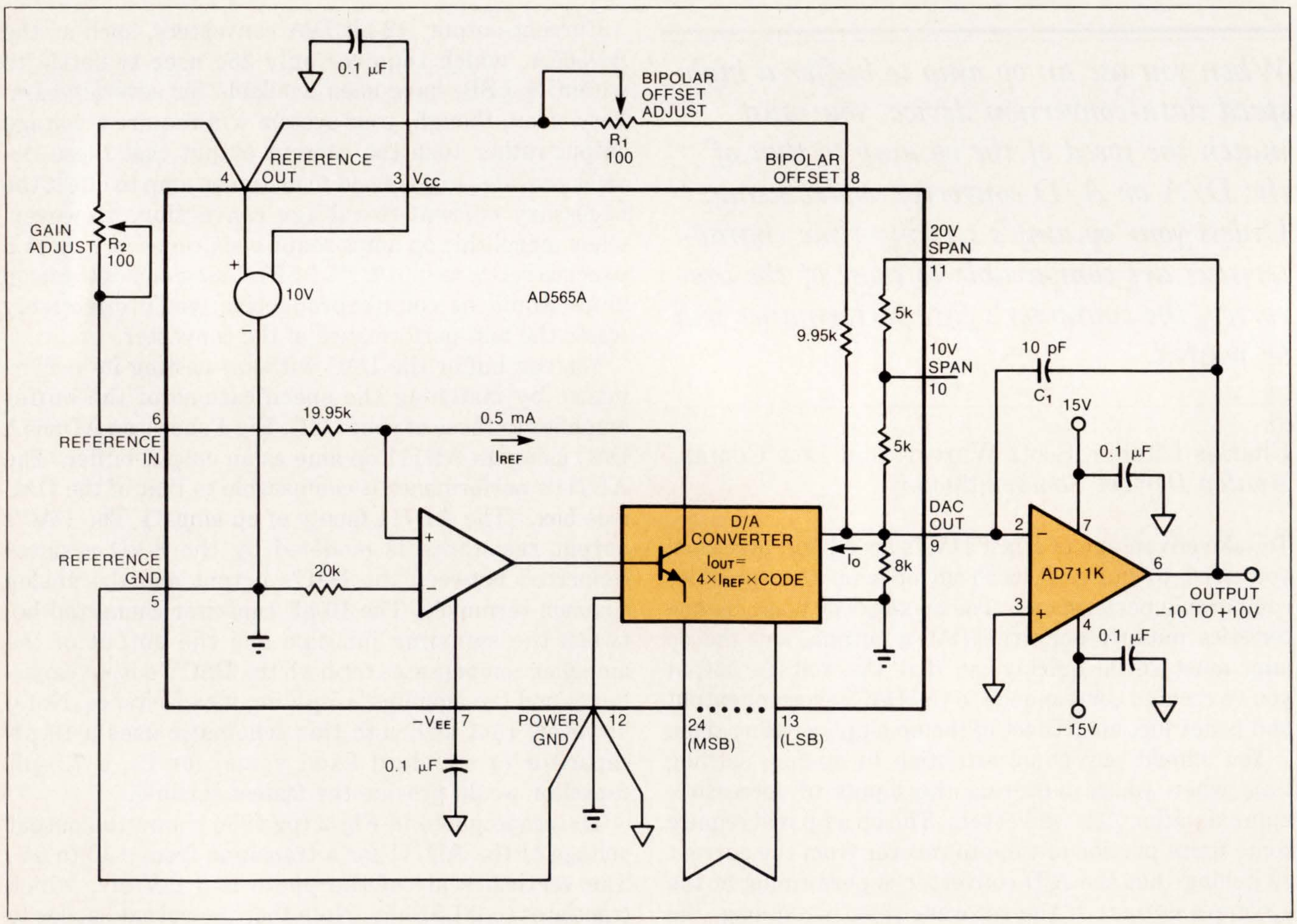


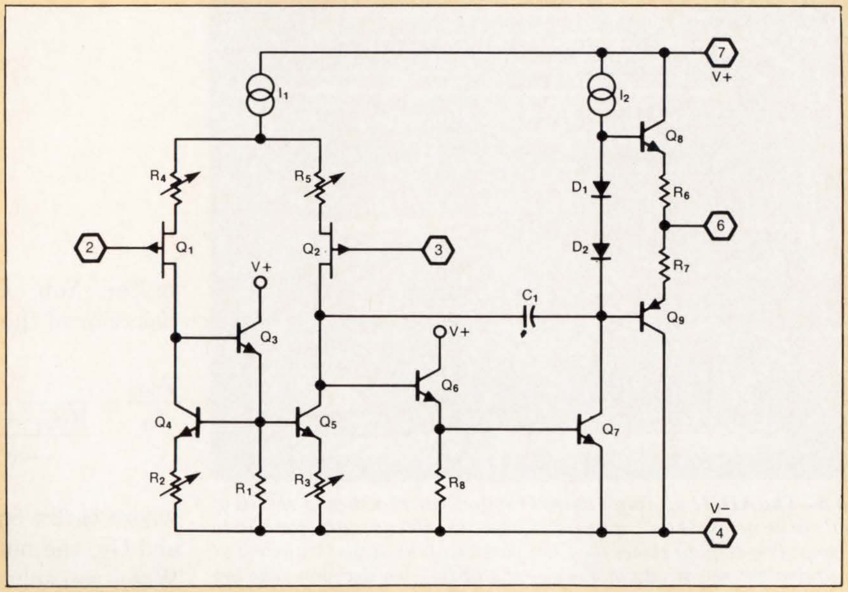
Fig 1—To take advantage of the speed of a fast D/A converter *(the AD565A), you can use an AD711 op amp to provide output buffering.*

The AD711 family

When operated as a follower or inverter that has a gain of unity or greater, the AD711 amplifier is compensated for stable operation. The device settles to within 0.01% of final value in 1 μsec typ, and it has a small-signal bandwidth of 4 MHz. The AD712, a dual version of the AD711, has similar specifications but also provides the sort of close parametric matching that results when you place two devices on the same die. The AD744 is internally compensated for noise gains of two or greater and settles in 0.5 μsec to within 0.01% of final value with a 10V step.

The amplifiers in the AD711 family are fabricated with a junction-isolated and JFET process. After initial processing, the manufacturer nulls the offset voltage and offset-voltage drift of each amplifier at the wafer level by laser-trimming several on-chip thin-film resistors. The manufacturer trims the input-stage operating current of each amplifier to reduce the effect of process variation on the op amps' ac performance. By using a standard linear process, the manufacturer avoids the potential problems associated with the dielectric-isolation process, which can cause dielectric absorption, thereby degrading settling characteristics.

The AD711 uses a 2-stage BiFET op-amp architecture. The first stage consists of a differential FET input section (Q_1 and Q_2), which operates with a total current of 400 μA and has a transconductance of approximately 400 μS. The combination of this current level and the input FETs provides both adequate transconductance and low noise. The manufacturer adjusts V_{OS} by laser-trimming small resistors in the source of the input-stage FETs.



A 2-stage BiFET op-amp architecture characterizes the AD711 family of op amps. The amplifiers are fabricated with a junction-isolated and JFET process.

KEY SPECS OF THE AD711 OP-AMP FAMILY

PARAMETER	AD711JN	AD711KN	AD744JN	AD744KN
0.01% SETTLING TIME (10V STEP, G=1) TYP (μSEC)	1	1	0.5	0.5
MAX (μSEC)	1.8	1.8	0.8	0.8
MIN SLEW RATE (V/μSEC)	16	18	45	50
MIN BANDWIDTH (MHz)	3.0	3.4	10	12
1-kHz VOLTAGE NOISE (nV/$\sqrt{Hz}$)	18	18	18	18
MAX OFFSET VOLTAGE (mV)	2.0	0.5	2.0	0.5
MAX OFFSET VOLTAGE DRIFT (μV/°C)	20	10	20	10
CMRR (dB MIN ±10V)	76	80	76	80
MAX SUPPLY CURRENT (mA)	3.4	3.0	4.5	4.0
STABLE AT MINIMUM GAIN OF	1.0	1.0	2.0	2.0
PRICE (100)	$0.80	$1.90	$1.90	$2.75

The bias current for the input stage is generated by a FET current source, I_1. Within I_1, current is multiplied by a split-collector pnp transistor that is cascoded by a second FET. This configuration provides a current source that is decoupled from power-supply and common-mode variations. The input stage operates directly into a current mirror, transistors Q_3 and Q_4.

The integrator-stage transistors, Q_6 and Q_7, run at 100 μA and 1 mA, respectively. All transistors in the signal path are striped-geometry devices. This geometry maximizes the gain-bandwidth product, F_T. Further, in this configuration, transistor Q_7 operates without degeneration. All these factors contribute to the creation of a tightly controlled integrator loop that has high bandwidth. The integrator loop reduces the phase shift through the amplifier.

Symmetrical current-limiting resistors on the class AB output stage combine with a 0.5-mA idle current to provide a harmonic-distortion figure of less than 0.0003% when the op amp's output is 3V rms, R_1 is 2 kΩ, and the test frequency is 1 kHz.

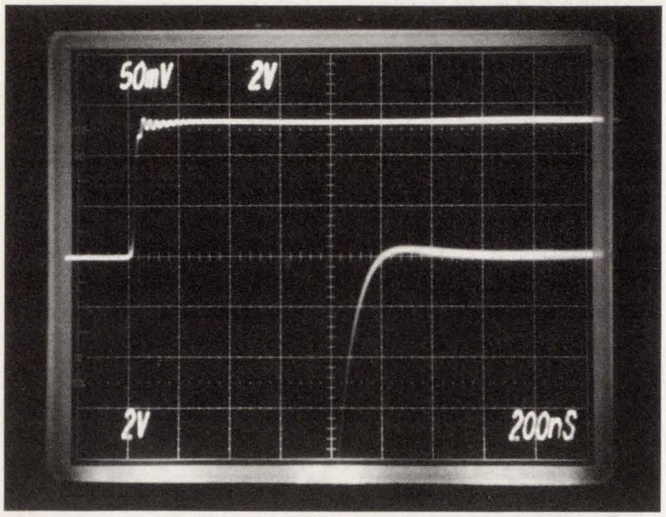


*Fig 2—**The AD711 op amp's output** (bottom trace) settles to ½ LSB of final value in less than 1 μsec (sweep speed is 200 nsec/div) for a 10 to 0V step. The display shows the final portion of the output transient at an equivalent sensitivity of 5 mV—or 2 LSBs—per division. The top trace is the logic transition that results in the amplifier's output excursion.*

amp), to provide the fastest possible settling time. A 1- to 10-pF air-variable trimmer capacitor is recommended for this purpose. Keep in mind that some ceramic trimmer capacitors exhibit very high dielectric absorption. Dielectric absorption causes the capacitor to exhibit a "memory effect." In a memory effect, although the voltage across the capacitor may change instantaneously to the value that you desire, the voltage will then tend to droop or relax to a voltage that's between the desired voltage and the previous voltage across the capacitor.

In general, you can represent the buffer amp as an ideal integrator. Using this model, you can determine the most suitable value for the feedback capacitor. **Fig 3** shows a Norton-equivalent simplified model in which the op amp is configured as a current-output-DAC buffer. You can accurately predict the small-signal behavior of the circuit with the equation

$$\frac{V_{OUT}}{I_O}=\frac{-R}{\dfrac{R(C_F+C_X)}{\omega_O}s^2+\left(\dfrac{G_N}{\omega_O}+RC_F\right)s+1}, \tag{1}$$

where $\omega_O/2\pi$ equals the op amp's unity-gain frequency and G_N, the noise gain of the circuit, equals $1+(R/R_O)$. When you solve **Eq 1** for C_F, you obtain

$$C_F=\frac{2-G_N}{R\omega_O}+\frac{2\sqrt{RC_X\omega_O}+(1-G_N)}{R\omega_O}. \tag{2}$$

In these equations, C_X is the total capacitance appearing at the inverting terminal of the op amp. In other words, C_X is the sum of the DAC's output capacitance and the op amp's input capacitance. **Eqs 1** and **2** describe the output of the system when the op amp's slew rate and other nonlinear effects are ignored.

When you replace R_O and I_O with their Thevenin equivalents, V_{IN} and R_{IN}, you obtain the general-purpose inverting amplifier shown in **Fig 4**. In this inverting amplifier, C_X is the op amp's input capacitance.

In either case, C_X changes the system response from a 1-pole to a 2-pole response. The additional pole increases settling time by introducing ringing in the op

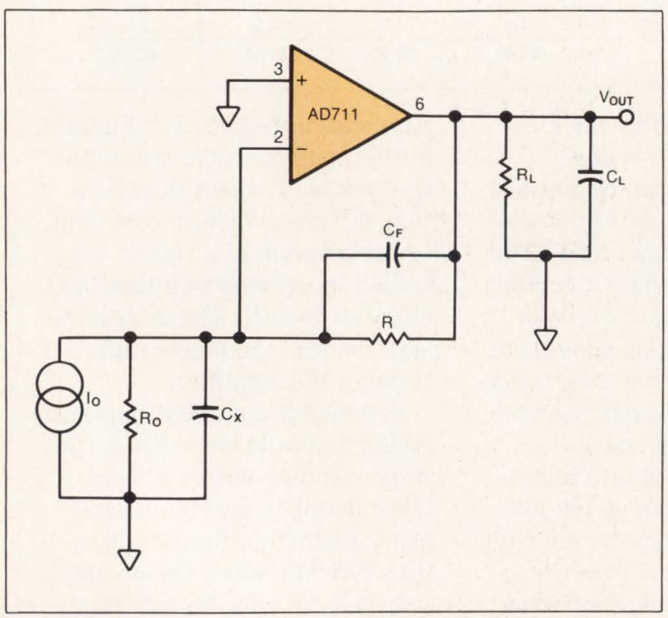


*Fig 3—**When you operate** the AD711 as a current-output DAC buffer, you can use this simplified model for circuit analysis.*

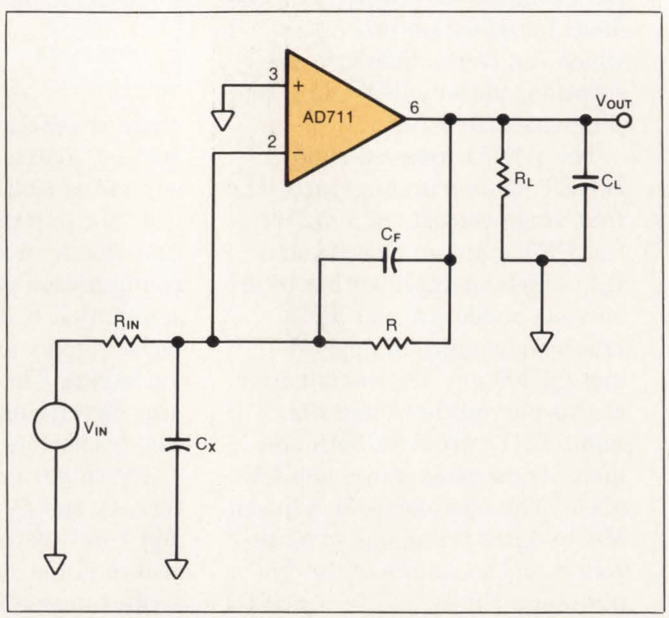


*Fig 4—**You can use this model for analysis** of an op amp that's operating as an inverting amplifier.*

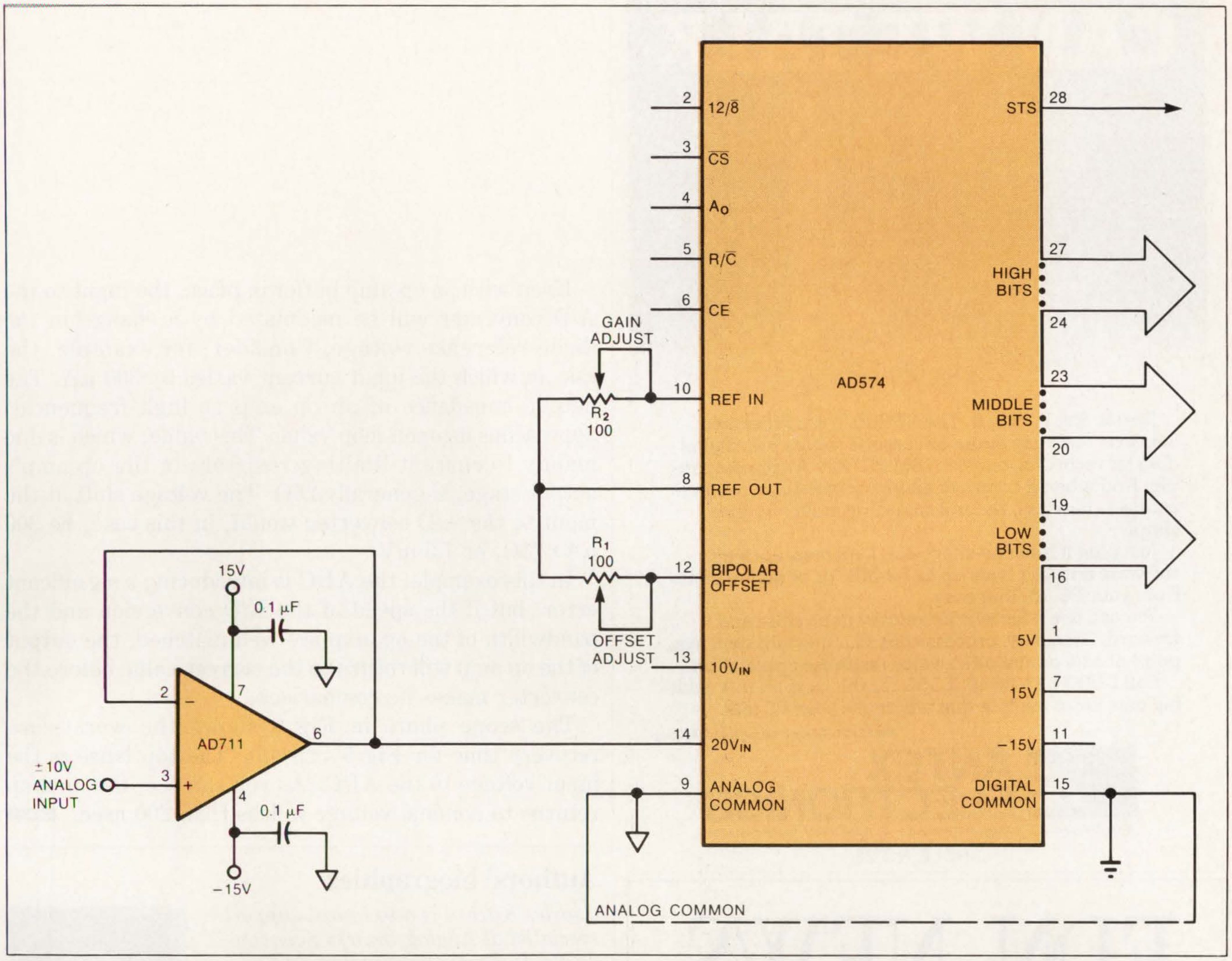
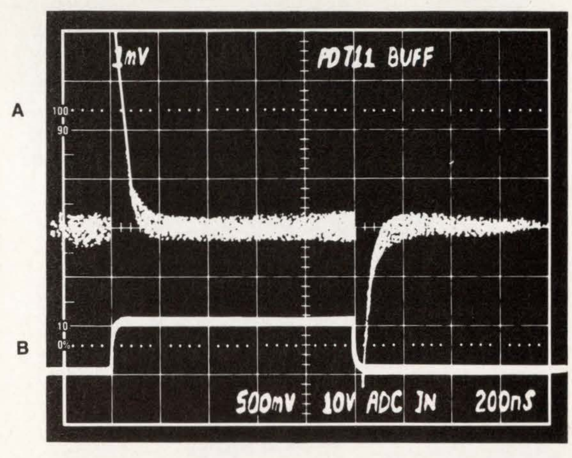


Fig 5—To buffer the input of a successive-approximation A/D converter, *you often need an op amp. In this circuit, an AD711 op amp acts as a unity-gain buffer on the input of an AD574 A/D converter.*

amp's output. Because you can estimate C_X with reasonable accuracy, you can use **Eq 2** to select a small capacitor, C_F, to cancel the input pole and minimize the amplifier's settling time.

Buffer amplifiers are also employed in data-acquisition systems, and one of the most demanding of these applications is that of buffering successive-approximation A/D converters. It's just as important for the op amp's performance to match that of the converter in this application as it is in the DAC-buffer application. **Fig 5,** for example, illustrates the connection of an AD711 as a unity-gain buffer at the input of an AD574 successive-approximation A/D converter.

A successive-approximation A/D converter compares an input current, which represents the signal being digitized, to a portion of the reference current. The reference current is developed with the use of a diode voltage reference. This voltage may deviate from its nominal value by several hundred millivolts; as a consequence, the A/D converter's input current is modulated. This input-current modulation occurs because the measuring device both effects and affects the measurement; to eliminate the modulation, you need to buffer the input to the converter.



TRACE	VERTICAL	HORIZONTAL
A	1 mV/DIV	200 nSEC/DIV
B	500 mV/DIV	200 nSEC/DIV

Fig 6—The AD711 op amp's output *(trace A) recovers in less than 200 nsec from a 2-mA source-current excursion. Trace B shows the logic transition that causes the current swing.*

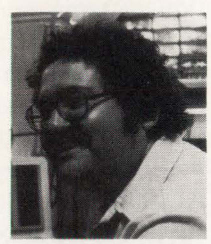
Even with an op-amp buffer in place, the input to the A/D converter will be modulated by a change in the diode reference voltage. Consider, for example, the case in which the input current varies by 300 μA. The output impedance of an op amp at high frequencies approaches its open-loop value. This value, which is due mainly to current-limiting resistors in the op amp's output stage, is generally 25Ω. The voltage shift at the input to the A/D converter would, in this case, be 300 $\mu A \times 25\Omega$, or 7.5 mV.

In this example, the ADC is introducing a significant error, but if the speed of the A/D conversion and the bandwidth of the op amp are well matched, the output of the op amp will return to the correct value before the converter makes its comparison.

The scope photo in **Fig 6** shows the worst-case recovery time for **Fig 5**'s circuit. The top trace is the input voltage to the ADC. As you can see, the op amp returns to nominal voltage in less than 200 nsec. **EDN**

Authors' biographies

Charles Kitchin is a technical-support specialist at Analog Devices Semiconductor Division (Wilmington, MA), where he has been employed for the last 10 years. He previously worked at KYBE Corp (Waltham, MA) and Boston radio stations WMEX and WCRB. Chuck graduated with an ASET from Wentworth Institute in Boston, and he now studies in the evening division at the University of Lowell in Lowell, MA. His spare-time activities include astronomy, jogging, and food and wine appreciation.



Scott Wurcer is a senior design engineer at Analog Devices Semiconductor, where he has worked for 12 years. He holds a BSEE degree from the Massachusetts Institute of Technology and is a member of IEEE and AES.

Lew Counts, manager of linear engineering and a Division Fellow at Analog Devices Semiconductor, has worked at the company for 15 years. A member of the IEEE, he holds a BSEE degree from the Massachusetts Institute of Technology. His hobbies are cycling and cross-country skiing.

Article Interest Quotient (Circle One)
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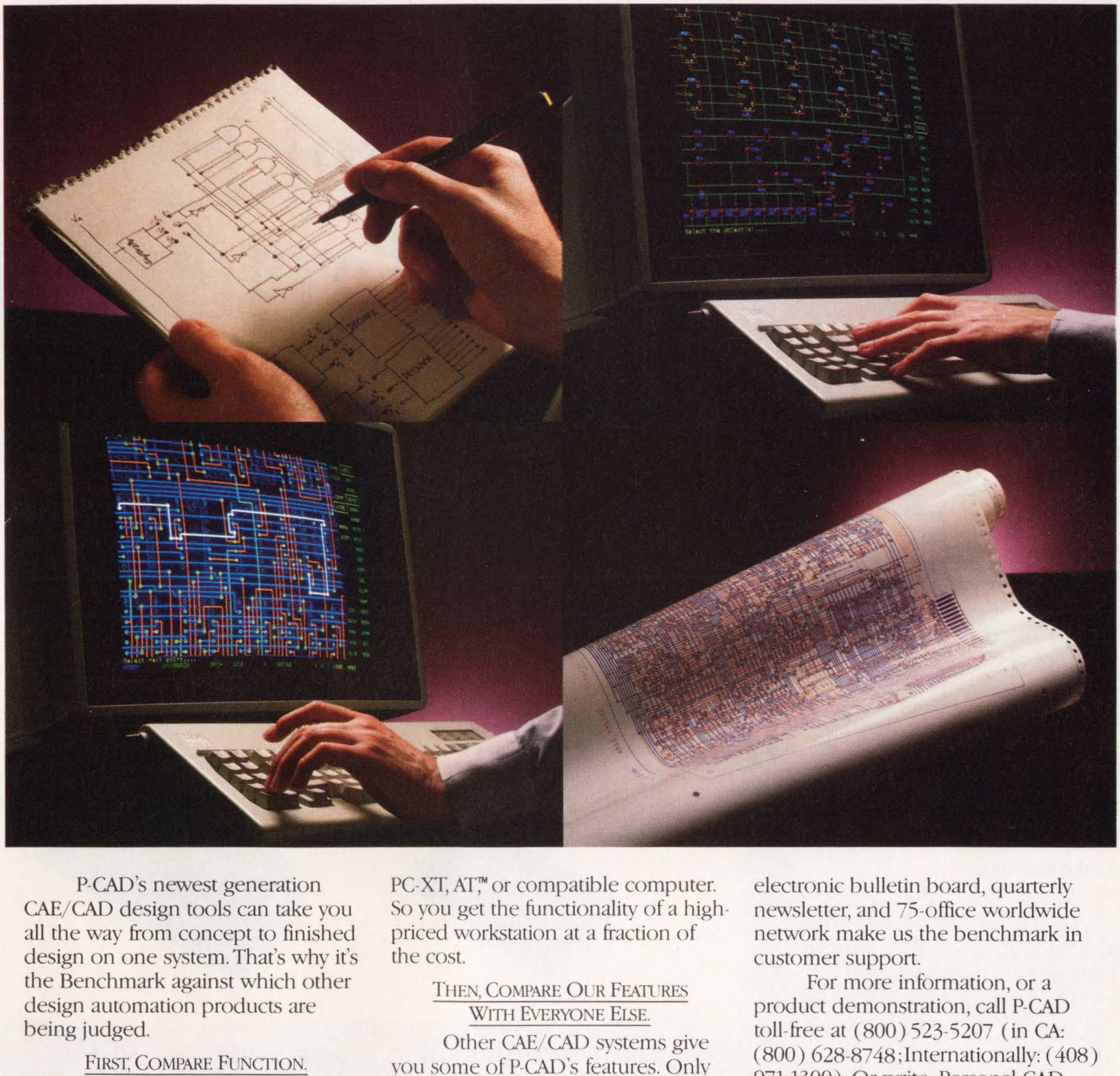

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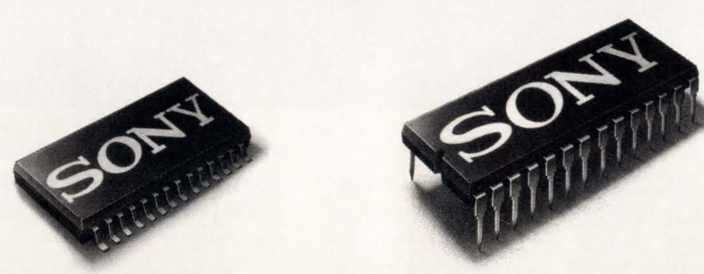

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CXK5816M—10L/12L	2K x 8	100/120	SOP*
CXK5416P—35L/45L/55L	4K x 4	35/45/55	300 mil DIP
CXK5864AP—70L/10L	8K x 8	70/100	600 mil DIP
CXK5864AM—70L/10L	8K x 8	70/100	SOP*
CXK5864PN—12L/15L	8K x 8	120/150	600 mil DIP
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CXK58256MF—10L/12L	MIX MOS	100/120	SOP	50 μA	0 to 70°C
CXK58256P—10LL/12LL	MIX MOS	100/120	600 mil DIP	10 μA	0 to 70°C
CXK58255P—45/55/70	FULL CMOS	45/55/70	600 mil DIP	5 μA	−30 to 85°C
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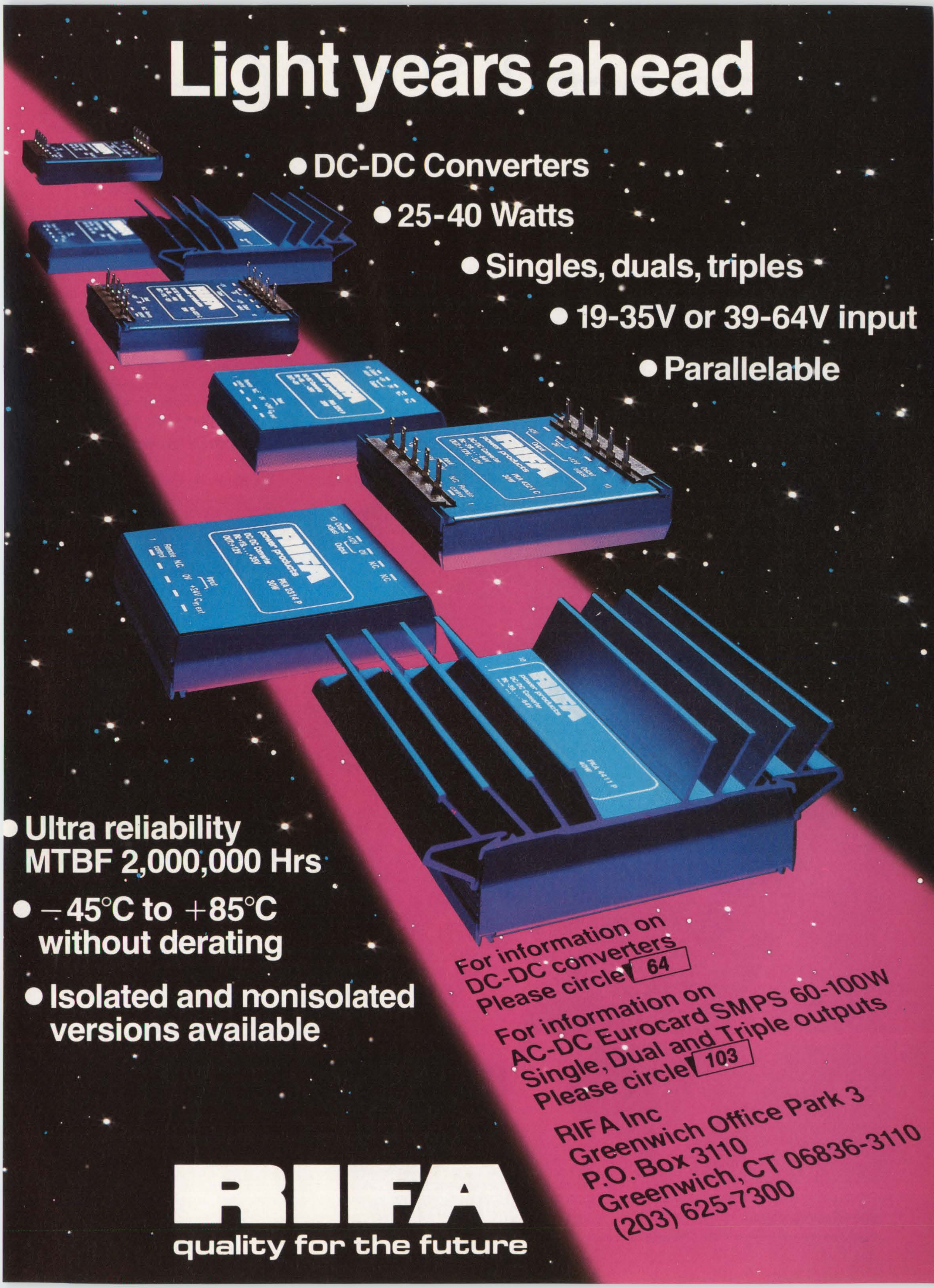
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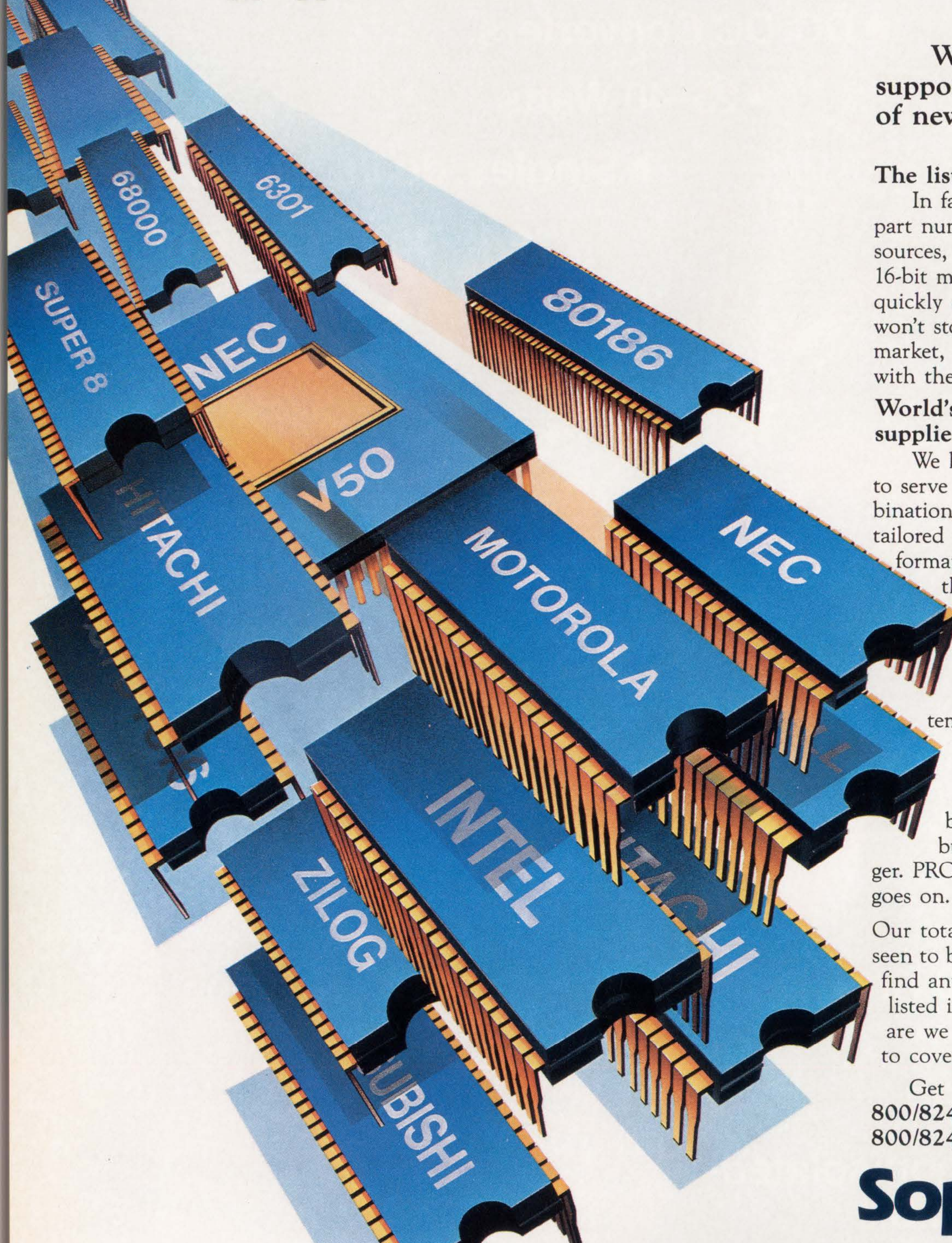

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CIRCLE NO 101

Combine C and assembly language for the 8086/88

You can write programs containing both C and assembly-language code for designs based on the 8086/88 µP. To write such programs, you must make your C and assembly-language routines compatible with each other.

William C Warner, *Consultant*

For designs incorporating an 8086/88, you may want to write all of a project's routines in a high-level language, such as C. However, some critical routines will invariably demand the speed and compactness of assembly language. To take advantage of the benefits of both languages, you can combine both types of code in your programs by writing assembly-language and C routines that are compatible. Your assembly-language routines must be able to call C routines, and your C routines must be able to call assembly-language routines.

To make C routines and assembly-language routines compatible, you must first know the conventions for the code your C compiler generates. Every compiler follows its own particular conventions for register usage, parameter passing, data returns, and routine calling. The assembly-language routines you write must follow those conventions.

In all C compilers, when a called routine returns control to a calling routine, certain registers must come back with their contents unaltered. These registers always include the code-segment (CS), stack-segment (SS), stack-pointer (SP), and base-pointer (BP) registers (**Fig 1**). When your C compiler calls an assembly-

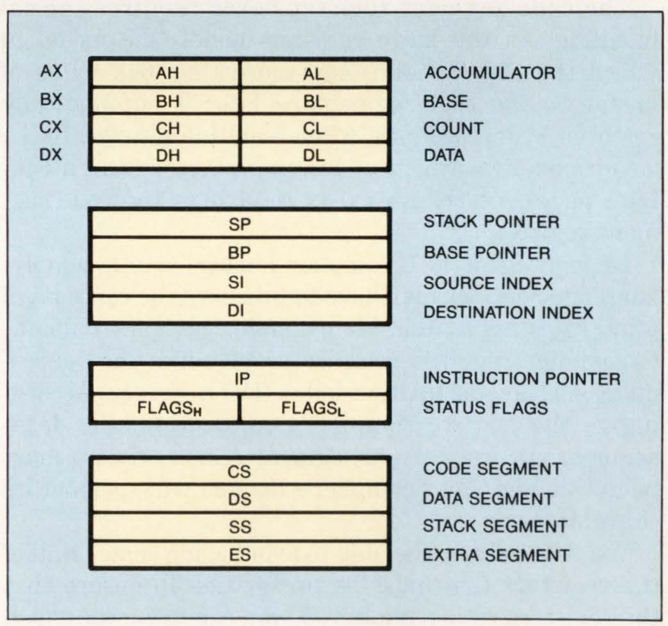

*Fig 1—**All C compilers require certain** registers to come back with their contents unaltered when a called routine returns control to a calling routine. Of all the 8086/88 registers (shown here), the code-segment (CS), stack-segment (SS), stack-pointer (SP), and base-pointer (BP) registers must always return unaltered.*

To write compatible assembly-language and C routines, you must first know your C compiler's conventions for the code it generates.

```
        ...

sum     DW      0                       ;reserve memory for integer sum
x       DW      0                       ;reserve memory for integer x
y       DW      0                       ;reserve memory for integer y
least   DW      0                       ;reserve memory for integer least

        ...

        MOV     AX, SEG sum             ;pass address of sum
        PUSH    AX                      ;    high word of addr
        MOV     AX, OFFSET sum
        PUSH    AX                      ;    low word of addr
        PUSH    WORD PTR y              ;pass contents of y
        PUSH    WORD PTR x              ;pass contents of x
        CALL    find_least              ;pass them to find_least
        ADD     SP, 8                   ;"remove" params from stack
        MOV     WORD PTR least, AX      ;store lesser of x and y
        ...
```

***Fig 2—This assembly-language code** follows the rules for a C compiler. The code passes parameters by pushing them (from right to left) onto the stack, calls the find_least() subroutine, removes the parameters from the stack, and stores the integer returned by find_least().*

language routine, therefore, that routine must return at least these four registers unaltered.

The code-segment register never requires special handling. In the large register model (the model in which the 8086/88 addresses more than 64k bytes of memory), the code-segment register is automatically restored, from the stack, when a routine returns. In the small model (in which addressing stays within a 64k-byte page), no reason exists to change the code-segment register.

Depending on the C compiler you use, your assembly-language routines may have to preserve the contents of other registers as well. For example, the Mark Williams C compiler requires routines to preserve the source-index (SI) and destination-index (DI) registers. According to the Lattice compiler's convention, the data-segment (DS) and extra-segment (ES) registers must be unchanged. Your compiler's manual will spell out its conventions.

You won't always be able to avoid using some or all of the registers that must be preserved. To ensure that the registers return unaltered, you can make the called routine save the registers on the stack immediately when it begins executing and then restore them just before it exits. Routinely saving all of the registers that must be preserved is a good idea, even if a particular routine does not employ them all, because during subsequent program modifications, you might change the registers that the routine uses. Always pushing the registers onto the stack in the same order is also a good practice.

When you have an assembly-language routine call a C routine, however, you don't have to modify your C code. You can always count on a C routine to return unaltered all the registers on the compiler's list of registers to be preserved.

Your assembly-language routines must also adopt the compiler's conventions for returning data. For each data type (character, short integer, long integer, floating-point number, pointer, etc), there is only one correct way to return a datum. A routine returns a datum by putting the datum in the appropriate register and executing a return. To date, most C compilers employ register AL for returning characters and register AX for returning short integers. For other data types, different compilers use different conventions. For example, the Mark Williams C compiler returns long integers, floating-point numbers, and pointers in DX:AX; DX holds the high word. The Lattice C compiler returns these data types in AX:BX with the high word in AX.

All code generated by C compilers for the 8086/88

```
; Routine: find_least
;
; This routine is callable from C as follows:
;
;    int least, x, y, sum;
;
;        least = find_least(x, y, &sum);
;
; This routine is passed two integers and the address of an
; integer.  It returns the lesser of the two integers and
; stores the sum of the two at the address passed in.
;
; This routine expects its parameters on the stack, just above
; the return address, and pushed in the order: &sum, y, x.  It
; returns the lesser of x and y in the AX register, and stores
; the sum of x and y at &sum.
;
; This routine is appropriate for use in large model only.

find_last:  PUSH  BP      ;preserve regs as required by compiler
            PUSH  DI
            PUSH  SI

            MOV   BP, SP

            MOV   CX, WORD PTR [BP+10]      ;get parameter x
            CMP   CX, WORD PTR [BP+12]      ;compare y
            JLE   find_last1                ;jmp if x <= y

            MOV   CX, WORD PTR [BP+12]      ;else, get y

find_last1: MOV   AX, WORD PTR [BP+10]      ;get x
            ADD   AX, WORD PTR [BP+12]      ;add y

            LDS   BX, DWORD PTR [BP+14]     ;get addr of sum
            MOV   WORD PTR [BX], AX         ;store x+y there

            MOV   AX, CX                    ;return lesser in AX

            POP   SI                        ;restore preserved regs
            POP   DI
            POP   BP
            RET
```

***Fig 3—The routine in Fig 2 can call** this routine, find_least(). This routine takes the two integers and the address of an integer from the stack, returns the lesser of the two integers, and stores the sum of the two integers at the address.*

When it begins executing, a called routine should save the registers on the stack immediately and restore them just before exiting.

passes parameters on the stack. The C routines push the parameters onto the stack in the order in which you've listed them in the parentheses immediately following a subroutine call. The parameters go on the stack starting with the right-hand parameter first, then proceeding in order to the left. The calling routine is responsible for removing parameters from the stack after the called routine returns. Consider this C program fragment:

```
int x, y, z, r;
char c;
...
r = demo(c, x, y, &z);
...
```

This fragment calls a routine named "demo()"; the fragment passes demo() a number of items: character c, integers x and y, and a pointer to integer z (as indicated by the prefix "&").

For this C statement, the compiler generates machine code that pushes the parameters onto the stack, starting with the pointer and ending with c. Then it calls the demo() routine, removes the parameters from the stack after demo() returns, and stores the data that demo() returns at the address of r. When the demo() routine is called, it finds its parameters on the stack, in the specified order, just above the return address for the calling routine.

When demo() begins to execute, the bytes on the stack are

```
high byte of high word of &z
low byte of high word of &z
high byte of low word of &z
low byte of low word of &z
high byte of y
low byte of y
high byte of x
low byte of x
high byte of c (on the stack,)
low byte of c (but meaningless)
high byte of high word of return address
low byte of high word of return address
high byte of low word of return address
low byte of low word of return address
```

Remember that words are pushed onto the stack high byte first, then low byte; double words are pushed onto the stack high word first, then low word. The stack grows downward in memory, and the stack pointer (SP) always points at the last byte on the stack (which is lowest in memory).

If you compile your C language routines in the small model instead of the large model, only one word of the return address, instead of two, will be on the stack, and only one word of pointer &z will be on the stack. Because the 8086/88 can't push less than a word onto the stack, character c—which is only a byte—will reside only in the low byte of the word devoted to it on the stack.

The following C program fragment provides an example of compatible assembly-language and C routines:

```
int least, x, y, sum;
...
least = find_least(x, y, &sum);
...
```

Imagine that find_least() is a C routine that will return the lesser of two integers, x and y, and store the sum of x and y at the address of the integer "sum." The assembly-language fragment in **Fig 2** can call find_least().

The assembly-language code in **Fig 2** follows C compiler rules. The code passes parameters by pushing them—right to left—onto the stack. It then calls find_least(), removes the parameters from the stack, and stores the integer returned by find_least(). **Fig 2**'s routine assumes that the compiler returns short integers in register AX.

Finally, suppose that after writing find_least() in C, you determine that this high-level-language routine is too slow, and you therefore decide to rewrite it in assembly language. **Fig 3** is an example of the find_least() routine written in assembly language. You can call this assembly-language version of find_least() from either a C routine or an assembly-language routine because it, too, follows the C compiler's conventions for register use and parameter passing. **EDN**

Author's biography

William C Warner is a self-employed consultant in Ann Arbor, MI. He specializes in the application of computers to instrumentation and automation. Will, who has worked for General Electric and Machine Vision International, has a BS in mathematics from Michigan State University.

Article Interest Quotient (Circle One)
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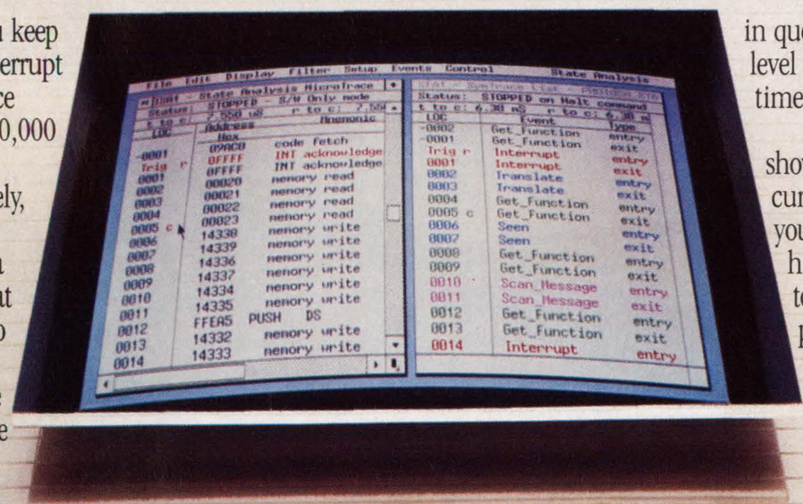
Spot a real-time problem that's 100,000 instructions old.



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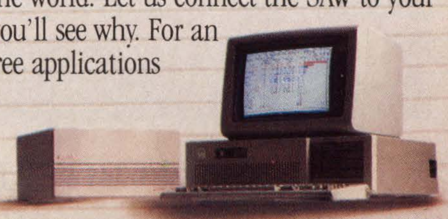

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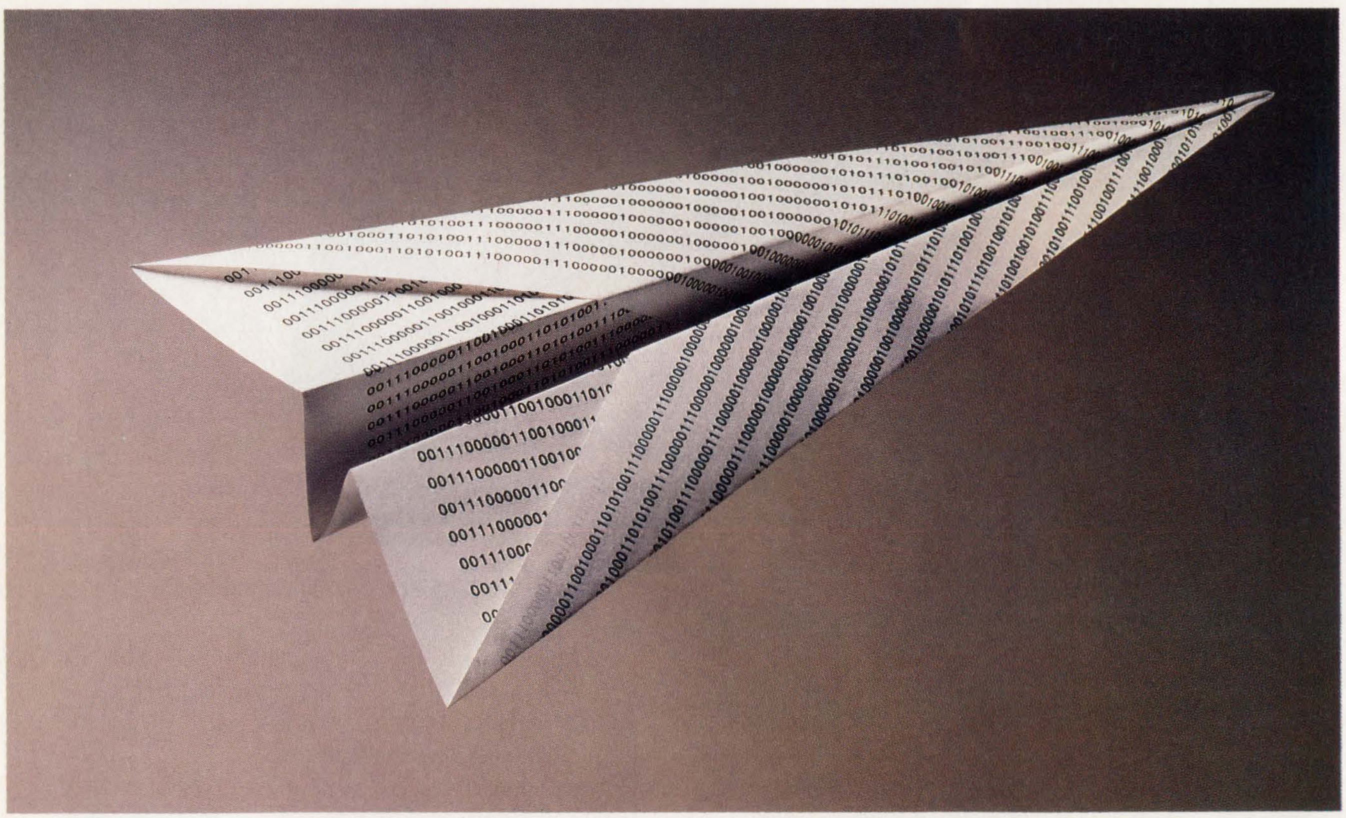

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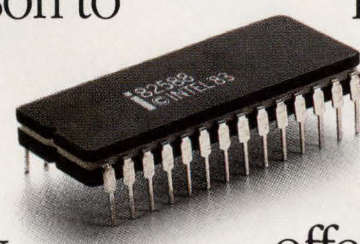

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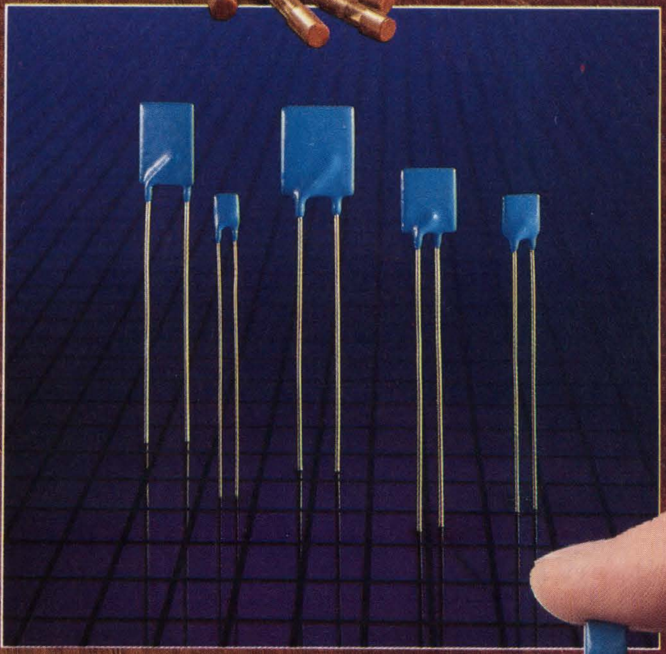

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VME system controller reduces parts count

Wade D Peterson
Mizar Inc, St Paul, MN

The VME Bus system controller **(Fig 1)** provides three essential functions: a reset circuit, a 16-MHz system clock driver, and a bus arbiter. Some systems will need additional functions, but this circuit minimizes pc-board area and cost.

The timing components R_1 and C_1 help generate a minimum 300-msec pulse ($\overline{\text{SYSRESET}}$). (The Schmitt-trigger input of IC_{1A} sources current, lowering the effective time constant.) The open-collector driver IC_2 issues this pulse following power-up or following a manual reset command, which you enter by pulsing the momentary-on switch S_1. IC_2 can sink 48 mA as required by the VME Bus specification. Resistor R_2 protects the switch and capacitor by limiting the discharge current to about 1A pk, and the Schottky diode (D_1) provides a capacitor-discharge path when you turn the power off and then back on again.

The TTL oscillator IC_3 offers adequate stability for the system clock (SYSCLK) because the 16-MHz signal has no relation to other signals on the bus. SYSCLK requires a 64-mA drive capability such as that provided by the totem-pole output of IC_4.

The system controller must provide an efficient method of bus arbitration to support the VME Bus's capability for multiprocessing. NAND gates IC_{5A} and IC_{5B} implement a single-level arbiter that can accommodate as many as 21 processors. When a bus master (CPU module) requests use of the bus (by asserting $\overline{\text{BR3}}$), the arbiter circuit asserts the bus-grant signal $\overline{\text{BG3IN}}$. This signal follows a daisy-chain path down the VME Bus backplane until it reaches the requesting module, which then asserts the bus-busy signal ($\overline{\text{BBSY}}$) until its transfers are complete.

The VME Bus specification requires that the system controller reside in slot 1, but the controller may operate as a subsystem in other slots as well. Accordingly, the enable/disable switch S_1 must be closed for operation in slot 1 and open for operation in the other slots. **EDN**

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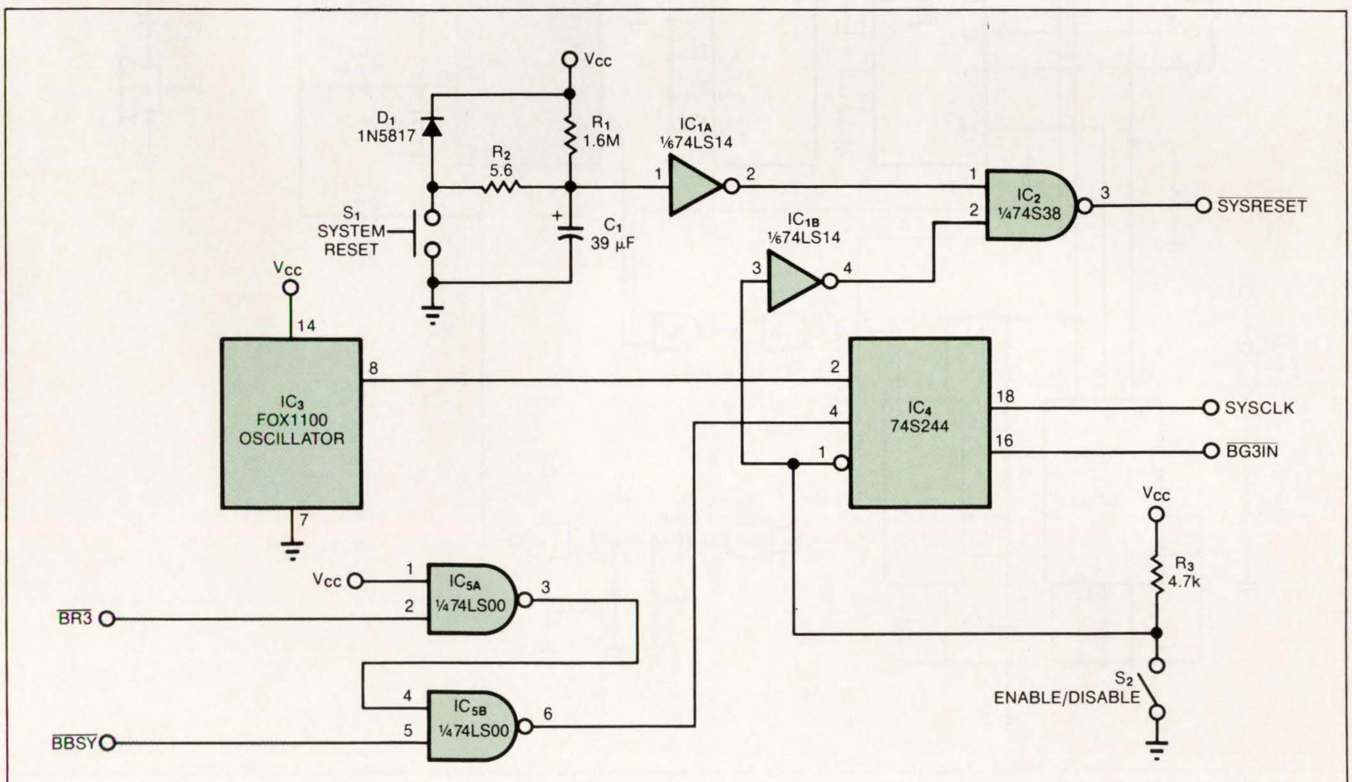

Fig 1—This inexpensive system controller *for the VME Bus provides a system reset, a 16-MHz clock, and a single-level bus arbiter.*

Circuit vocalizes hex code for 4-bit input

Ricardo G Jiménez
Mexicali Technological Institute, Calexico, CA

The **Fig 1** circuit is a general-purpose annunciator that interprets a 4-bit binary input code ABCD and vocalizes the corresponding hexadecimal word. The speaker gives an audible report each time you press the S_1 switch.

The contents of the EPROM (IC_4) drive a speech processor (IC_5), whose pulse-code-modulated output (pin 24) undergoes filtering and amplification before driving the speaker. By addressing the processor's 59

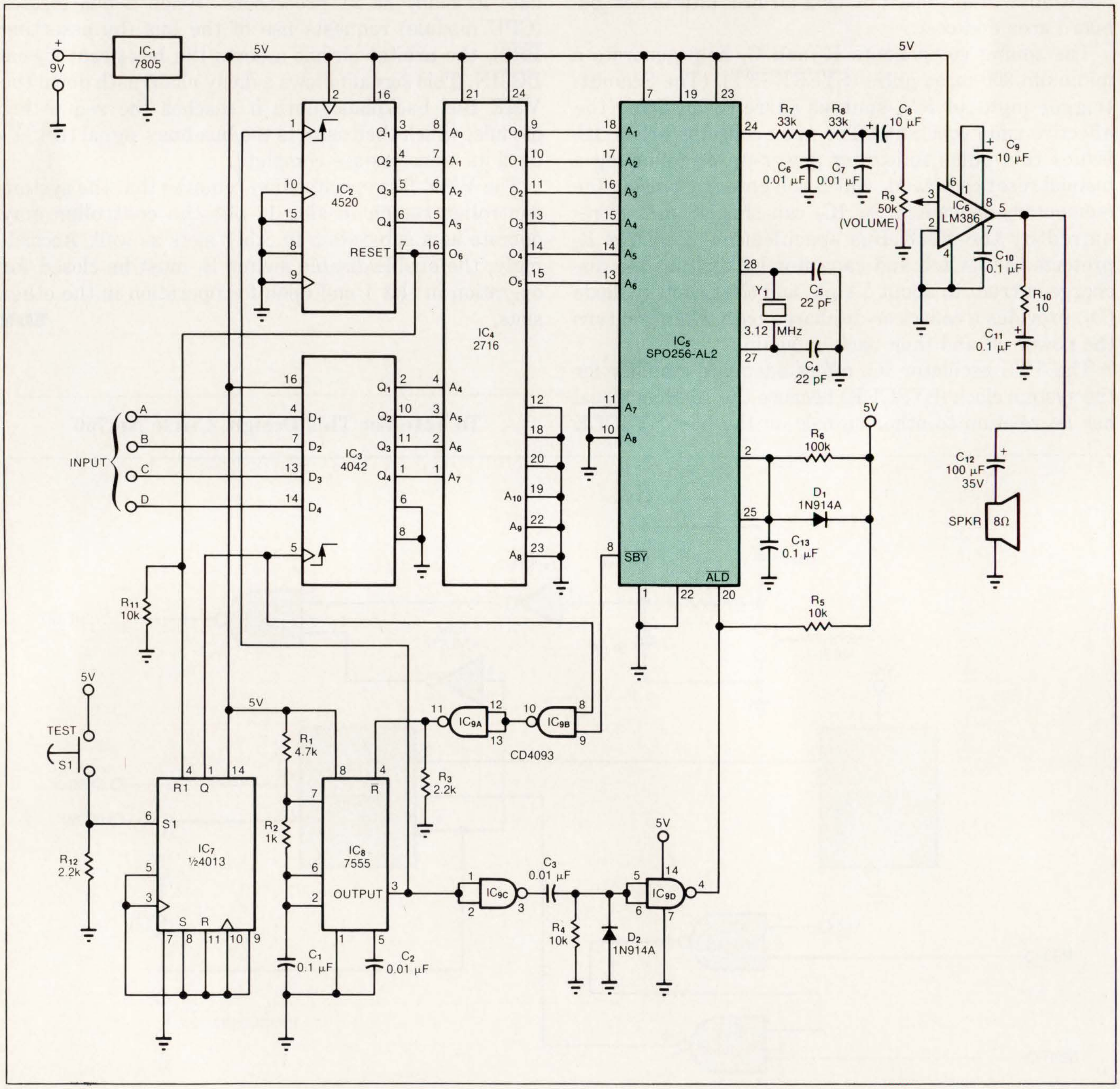

***Fig 1—This circuit's speech processor (IC_5)** synthesizes audible words for hexadecimal codes corresponding to the binary input on lines A, B, C, and D.*

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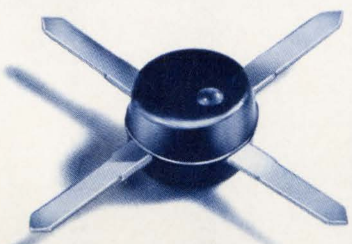

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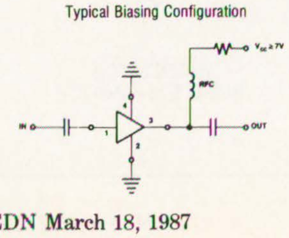

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allophones and five pauses in the proper sequence, you can synthesize the required hexadecimal word: one of the numbers "zero" through "nine," or one of the letters "A" through "F" **(Listing 1).**

Flip-flop IC_7's Q output latches high when you press S_1, causing IC_3 to latch the input data and apply it to the EPROM's upper address inputs A_4-A_7. This action selects a block of memory within the EPROM; counter IC_2 then scans those memory locations in sequence by driving the lower address bits A_0-A_3. As a result, the EPROM delivers a preprogrammed sequence of instructions to the speech processor.

Timer IC_8 and associated components form an astable, 2150-Hz oscillator that operates in 1-Hz bursts. Each positive transition at the timer's output (pin 3) advances counter IC_2 by one (starting with zero, following the closure of S_1). Each negative transition at pin 3 causes IC_{9C} and IC_{9D} to generate a negative pulse at the speech processor's address-load input ($\overline{ALD}$), which loads the current EPROM output and causes the processor to assert a low logic level at $\overline{SBY}$ (pin 8). This action resets the timer output to zero.

The processor chip holds $\overline{SBY}$ low for an interval appropriate to that particular allophone; when $\overline{SBY}$ returns high, the timer initiates the next allophone cycle. Each audible report requires one to seven allophones as shown in **Listing 1.** Following each report, the hex-data instructions 4 and 44 reset the speech processor (internally) and the corresponding counter and flip-flop (via output O_6). For the input ABCD=1010 (decimal 10), for example, the speaker will say the hexadecimal equivalent, "A." **EDN**

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LISTING 1—EPROM CONTENTS

DECIMAL ADDRESS	HEX ADDRESS	HEX DATA		DECIMAL ADDRESS	HEX ADDRESS	HEX DATA	
0	0	4		114	72	7	
1	1	2B		115	73	7	
2	2	3C	"ZERO"	116	74	23	
3	3	35		117	75	C	
4	4	4		118	76	B	
5	5	44		119	77	4	
16	10	39		120	78	44	
17	11	F		128	80	14	
18	12	F	"ONE"	129	81	C	"EIGHT"
19	13	B		130	82	D	
20	14	4		131	83	4	
21	15	44		132	84	44	
32	20	D		144	90	38	
33	21	1F	"TWO"	145	91	18	"NINE"
34	22	4		146	92	6	
35	23	44		147	93	B	
48	30	1D		148	94	4	
49	31	E	"THREE"	149	95	44	"A"
50	32	13		160	A0	14	
51	33	4		161	A1	4	
52	34	44		162	A2	44	
64	40	28		176	B0	3F	"B"
65	41	28	"FOUR"	177	B1	17	
66	42	3A		178	B2	4	
67	43	4		179	B3	44	
68	44	44		192	C0	37	
80	50	28		193	C1	37	"C"
81	51	28	"FIVE"	194	C2	17	
82	52	6		195	C3	4	
83	53	23		196	C4	44	
84	54	4		208	D0	21	
85	55	44		209	D1	17	"D"
96	60	37		210	D2	4	
97	61	37	"SIX"	211	D3	44	
98	62	C		224	E0	17	"E"
99	63	C		225	E1	4	
100	64	2		226	E2	44	
101	65	29		240	F0	7	
102	66	37		241	F1	7	"F"
103	67	4		242	F2	28	
104	68	44		243	F3	28	
112	70	37		244	F4	4	(RESETS IC_5)
113	71	37	"SEVEN"	245	F5	44	(RESETS IC_2 AND IC_7)

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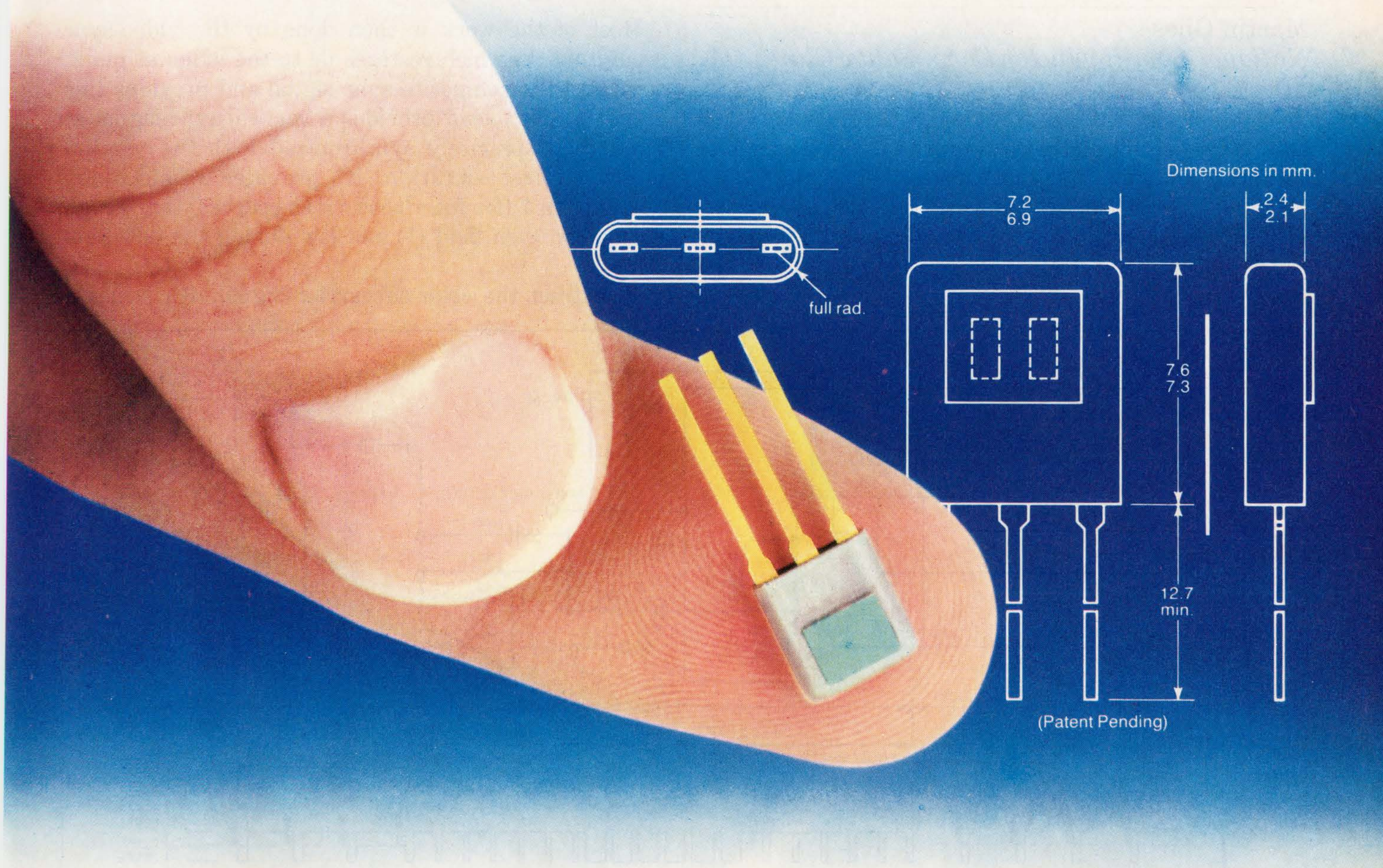

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Video IC extracts timing waveforms

Martin Giles
National Semiconductor Corp, Santa Clara, CA

To combine two video sources in one CRT display (such as a VCR signal and a computer-generated graphics overlay), you must first synchronize their timing waveforms. **Fig 1**'s circuit accomplishes this task by extracting timing information from one source for use in the other. You provide only a composite-video input to the circuit.

Most of the work is then done by the video-sync separator IC_1, which restores dc to the video at pin 2, separates the composite-sync signal and provides this output at pin 1, and provides a vertical-sync signal at pin 3 that's precisely synchronized with the vertical interval's first serration. IC_1 provides a field index pulse at pin 7 (for interlaced video sources) that's high during the even field (1) and low during the odd field (2).

To extract the color-subcarrier signal, IC_1 issues a

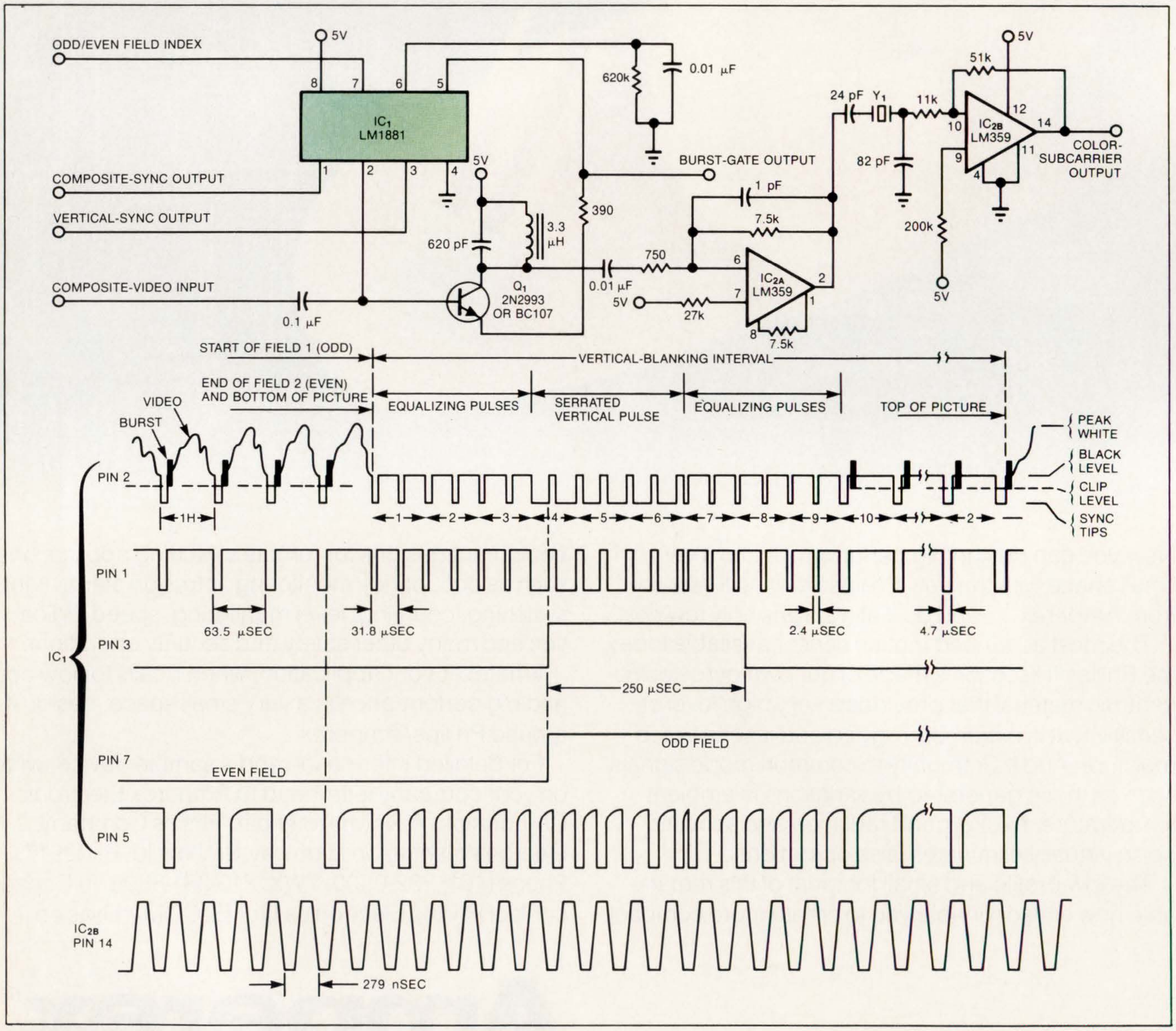


Fig 1—This circuit strips the timing information *from a composite-video signal for use in synchronizing the signal with another video source.*

burst-gate output (pin 5) that turns on the transistor amplifier, Q_1, only during the composite waveform's color-burst interval. Op amp IC_{2A} amplifies the frequency burst and applies it to the 3.579545-MHz crystal Y_1. Because the input resistance of op amp IC_{2B} sets a high Q for the crystal circuit (approximately 10k), the crystal continues to ring between bursts, providing a constant color-subcarrier output. **EDN**

To Vote For This Design, Circle No 748

Nested functions transform filter roots

David C Bidwell
Dowty-RFL Industries Inc, Boonton, NJ

The nested-function routine of **Fig 1a** transforms the roots of a lowpass transfer function to the roots of an equivalent bandpass transfer function. By including the routine in a filter program that solves for the roots of lowpass functions (for example, Butterworth, Chebyshev, and elliptical), you can obtain the equivalent bandpass roots for any desired Q. The usefulness of nested, user-defined functions for Basic programming has been discussed before **(Ref 1)**.

Written in Microsoft Basic for the IBM PC, the routine of **Fig 1a** exhibits the following characteristics:

- It uses no transcendental functions except the square root; this approach is simpler than the polar form based on trigonometric functions described in **Ref 2**.
- It uses no approximations, but instead solves the exact formulas given in **Ref 3**.
- It is highly accurate in single-precision arithmetic for any practical filter-circuit Q (QC), defined as $\sqrt{(f_1 f_2)}/(f_2-f_1)$, where f_1 and f_2 are the filter's lower and upper 3-dB frequencies, respectively.
- It converges on the simple linear transformation discussed in **Ref 3** for high QC.

EDN

```
PROGRAM BPFUNC (USER FUNCTIONS FOR BPXFRM)

10 INPUT "QC = ";Q
20 DEF FNT(A,B) = (B*B - A*A)/2/Q^2 + 2
30 DEF FNV(A,B) = SQR(FNT(A,B) + SQR(FNT(A,B)^2 + A*A*B*B/Q^4))
40 DEF FNU(A,B) = A*B/Q^2/FNV(A,B)
50 DEF FNR(A,B) = (A/Q + FNU(A,B))/2
60 DEF FNI(A,B) = (FNV(A,B) + B/Q)/2
70 DEF FNA(A,B) = (A/Q - FNU(A,B))/2
80 DEF FNB(A,B) = (FNV(A,B) - B/Q)/2
90 INPUT "ALPHA, BETA";A,B
100 PRINT USING "###.###### +/- J ###.######";FNR(A,B),FNI(A,B)
110 PRINT USING "###.###### +/- J ###.######";FNA(A,B),FNB(A,B)
120 PRINT
130 GOTO 90
```

(a)

```
RUN
QC = ? 1
ALPHA, BETA? 0,2.6003
   0.000000   +/- J  2.940391
   0.000000   +/- J  0.340091

ALPHA, BETA? .48307,0
   0.241535   +/- J  0.970392
   0.241535   +/- J  0.970392

ALPHA, BETA?
Break in 90
Ok
RUN
QC = ? 25
ALPHA, BETA? .2,.8
   0.004064   +/- J  1.016120
   0.003936   +/- J  0.984120

ALPHA, BETA? .7071067,.7071067
   0.014342   +/- J  1.014142
   0.013942   +/- J  0.985858

ALPHA, BETA?
Break in 90
Ok
```

(b)

***Fig 1—This routine of nested functions (a),** when embedded in a lowpass-filter program, calculates roots for the equivalent bandpass function. (QC is the desired filter Q; alpha and beta are the real and imaginary parts of the lowpass root.) Examples of the routine's output are shown in **b**.*

References

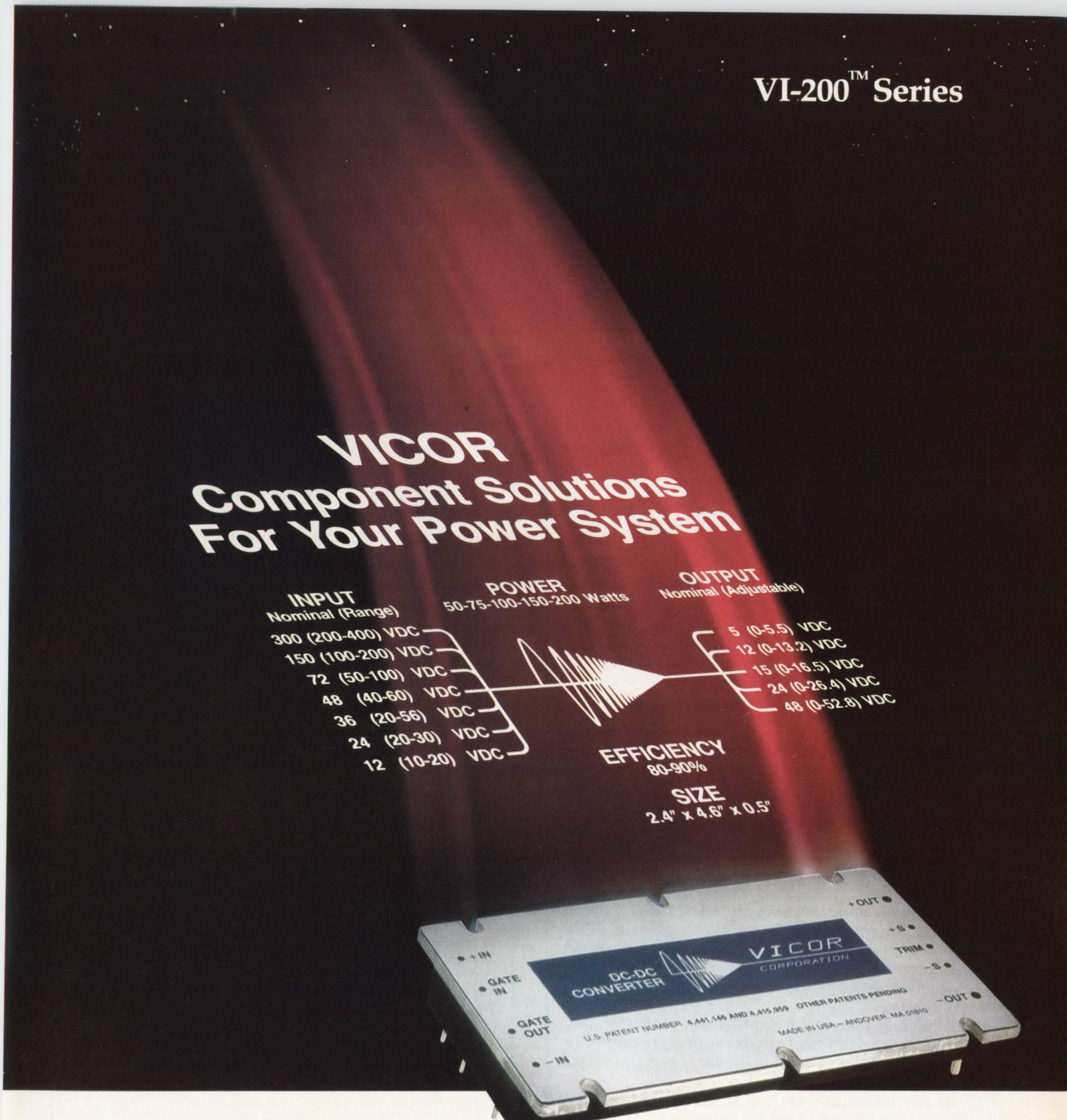
1. Bidwell, D, "Nested functions calculate standard Rs," *EDN*, June 28, 1984, pg 275.

2. Delagrange, A, and Douyon, R, "Pocket calculator eases filter design," *EDN*, January 24, 1985, pg 243.

3. Bidwell, D, "Filter transforms beat approximations," *EDN*, August 5, 1981, pg 141.

4. Knaell, K, "Lowpass/bandpass transform beats computers," *EDN*, March 4, 1981, pg 152.

To Vote For This Design, Circle No 746



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Circuit debounces pushbutton switch

Brian A Wittman
AT&T Consumer Products, Indianapolis, IN

Fig 1 is a simple alternative to the traditional debounce circuit based on a flip-flop. The inverters IC_{1A} and IC_{1B} form a bistable latch; closing the switch forces the latch to change and remain in the opposite state.

For most pushbuttons, 50 msec is a reasonable value for the product of R_2C_1. The interval must be short enough to register a rapid sequence of switch closures but long enough to avoid false signals caused by switch bounce. Resistor R_2's value should be at least 10 times that of R_1 to ensure proper operation despite the divider effect of these resistors. By substituting a NAND gate for either inverter and adding a power-on reset circuit at the other input, you can make the latch assume a desired state at power-up. **EDN**

To Vote For This Design, Circle No 749

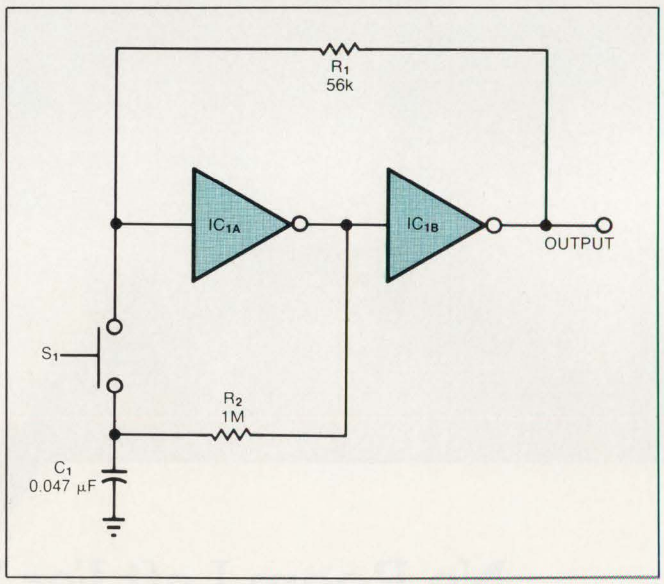

Fig 1—Inverters IC_{1A} and IC_{1B} form a bistable latch that debounces the pushbutton switch S_1.


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CIRCLE NO 93

Design Ideas Winners January through December 1986

January 9, 1986
Brian Koga, Wang Laboratories Inc, Lowell, MA. "68020 adapter upgrades 68000 systems."
January 23, 1986
Irwin Cohen, Hewlett-Packard Co, Rockaway, NJ. "Divider produces symmetrical output."

February 6, 1986
Richard Poindexter, Telex Computer Products, Tulsa, OK. "Use simple circuit to program EPROMs."
February 20, 1986
Edward W Rummel, Robin Baker Associates Inc, Short Hills, NJ. "Generate bipolar logic levels from a 5V supply."

Winning Idea is an adapter for upgrading 68000-based pc boards

Brian Koga has won EDN's $1500 grand prize for the best Design Idea of 1986. His January 9, 1986, entry, "68020 adapter upgrades 68000 systems," lets you enhance an existing 68000 board to take advantage of the 68020's larger instruction set. In some cases, the 68020's higher clock rate lets you speed up program execution as well. To use the adapter, you plug it into a 68000 socket and then plug a 68020 μP into a socket on the adapter board. Logic gates on the board derive the additional signals that the 68020 requires.

Mr Koga developed this adapter to allow software developers to begin debugging 68020 code without waiting for layout and fabrication of a 68020 board. He suggests that others could do the same. In addition, he has used the adapter to enhance the performance of a Commodore Amiga computer.

These activities reflect two of Mr Koga's interests: developing socket adapters and working with personal computers. Another interest is skiing, which he enjoys when time permits. Mr Koga holds a BSEE from Northrop University (Ingleside, CA) and is a principal hardware engineer with Wang Laboratories in Lowell, MA. Before coming to Wang in 1984, he was with IBM in Danbury, CT. Congratulations, Mr Koga, from all of us at EDN. —*Tarlton Fleming*

March 6, 1986
Christos S Koukourlis, Demokritos University of Thrace, Xanthi, Greece. "Test probe measures 4 to 220V."
March 20, 1986
Jeffrey Anthony, Corby Industries Inc, Whitehall, PA. "C function calls the IBM PC I/O system."

April 3, 1986
Michael Ellis, Scientific Atlanta, Norcross, GA. "Feedforward amplifier reduces distortion."
April 17, 1986
Robert D Grappel, MIT Lincoln Laboratory, Lexington, MA. "Square-root algorithm is fast and simple."

May 1, 1986
Robert J Zavrel, Signetics Inc, Sunnyvale, CA. "IF chip forms audio decibel-level detector."
May 15, 1986
John A Haase, Colorado State University, Fort Collins, CO. "Digital power controller handles 1 kW."
May 29, 1986
Mark D Braunstein, Contel Information Systems, Fairfax, VA. "Simple circuit tests twisted-pair cables."

June 12, 1986
Joseph G Vazach, Allen-Bradley Co, Highland Heights, OH. "Enlarge Z80 memory space to 512k bytes."
June 26, 1986
Steve Momii, University of Washington, Seattle, WA. "Circuit generates frequency difference."

July 10, 1986
Mark Walczak, Microcontrol Pty Ltd, Monterey, Australia. "Low-power RS-232C driver operates from 5V."

August 7, 1986
Thomas Hack, Master Designers Inc, Colorado Springs, CO. "Program computes log magnitude and phase."
August 21, 1986
H H Eck, Pulse Electronics Inc, Rockville, MD. "Circuit provides controllable resistance."

DESIGN IDEAS

September 4, 1986
Kurt W Christner, Carson City, NV. "IC emulates many types of logic gates."

September 18, 1986
Jerold R Thompson, Sperry Corp, Salt Lake City, UT. "Software provides rapid parity check."

October 2, 1986
Bobircă Florin Daniel, The Electronic Research Institute, Bucharest, Romania. "Circuit converts voltage ratio to frequency."

October 16, 1986
Damian G Bonicatto, Hibbing Electronics Co, Hibbing, MN. "Reset circuit solves brownout problems."

October 30, 1986
Doug Farrar, Apple Computer Inc, Cupertino, CA. "VCO generates frequencies above 40 MHz."

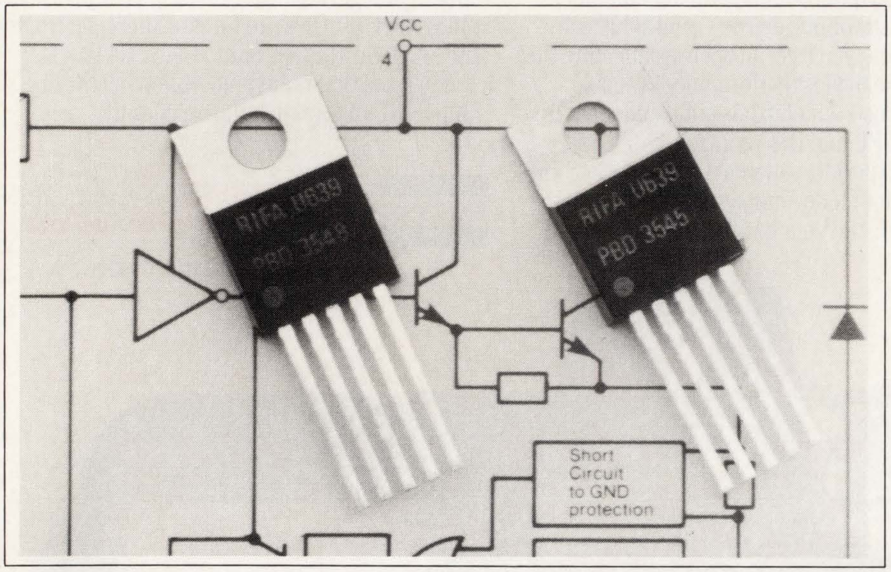
November 13, 1986
Mark Rumreich, RCA Corp, Indianapolis, IN. "Resistors provide nonlinear pot tapers."

November 27, 1986
Jim Wojcik, Allen-Bradley Co, Highland Heights, OH. "Arbiter lets two μPs use common RAM."

December 11, 1986
Andrew Dart, Trans-Texas Telegraph Co, Duncanville, TX, and **Richard Kihn,** KSDM TV, Beaumont, TX. "TV sync generator acts as clock timebase."

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES



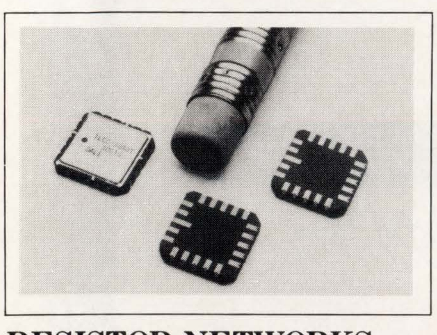
CURRENT DRIVERS

- *Protected for inductive loads*
- *Offer switching rates to 10 kHz*

The PBD 3545 and 3548 are 2A sink and source drivers, respectively. They feature short-circuit protection and a status output that indicates the load on an open circuit or a short circuit to either V_{CC} or ground. Internal protection diodes are provided to handle inductive-load switching. A temperature shutdown function limits the chip temperature to 130°C. During short-circuit load conditions, the output will be latched to zero at a speed fast enough to allow switching rates to 10 kHz. The supply voltage is 45V max. Operation spans 0 to 70°C for the PBD 3545, and −40 to +85°C for the 3548. PBD 3545, $3.25; PBD 3548, $3.75 (100).

Rifa Inc, Box 3110, Greenwich, CT 06836. Phone (203) 625-7300.

Circle No 351



RESISTOR NETWORKS

- *Three basic sizes available*
- *Package power ratings as high as 1.2W*

Model TLCC resistor networks come in hermetically sealed, chip-carrier-style packages that are compatible with automatic-assembly equipment. The networks are available in three basic sizes, each of which comes in a choice of three schematics. The 01 schematic provides a choice of 15, 19, or 23 resistors; each resistor connects to a common terminal. The 03 and 06 schematics provide eight, 10, or 12 isolated resistors. Resistance values range from 1 to 100 kΩ. Power ratings range as high as 1.2W per package for 24-terminal models. Individual resistors have 50-mW (01) and 100-mW (03 and 06) power ratings. Tolerances of ±2, ±1, ±0.5, and ±0.1% are standard, and the temperature coefficient equals ±25 ppm/°C. A typical 20-terminal, 03-schematic model with a ±2% tolerance, $9.53 (1000). Delivery, 12 weeks ARO.

Dale Electronics Inc, 2064 12th Ave, Columbus, NE 68601. Phone (402) 371-0080.

Circle No 352

THERMOMETERS

- *Dual-range capability*
- *Industrial-grade construction*

The industrial-grade construction of the Model 865 and Model 866 thermistor thermometers includes a high-impact ABS plastic case that can withstand a 6-ft drop. The 865 measures temperature from −70 to +300°F in two ranges. One range measures temperature from −70 to +300°F with a resolution of 1°F and an accuracy of ±(0.3%+1°F). The other range measures temperature from −70 to +199.9°F with a 0.1°F resolution. The accuracy equals ±(0.3%+1°F) from −70 to −40°F, and ±(0.3%+0.5°F) from −40 to +199.9°F. Model 866 measures temperature from −55 to +150°C with a 0.1°C resolution. The accuracy equals ±(0.3%+0.6°C) from −55 to −40.1°C, and ±(0.3%+0.3°C) from −40 to +150°C. The thermistor value at 25°C (77°F) equals 2252Ω. The instruments are powered by a 9V battery; an alkaline battery provides 350 hours of continuous operation. $159.

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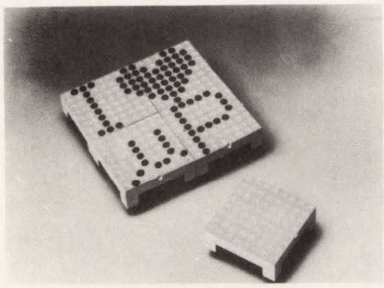
CIRCLE NO 57



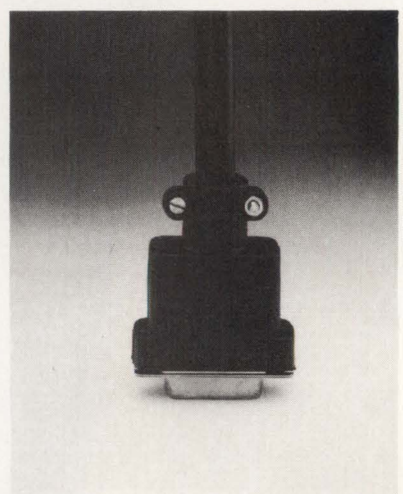
DISPLAYS

- *Readable from 35 ft*
- *Offers high alphanumeric flexibility*

The PD1165 (high-efficiency red) and PD1167 (green) programmable 8×8-dot matrix displays include built-in CMOS control circuitry that consists of LED drivers, multiplexers, RAM, and display-attribute features. Because of their 1.1-in. character height and 75° viewing angle, they are readable from 35 ft. They can display a variety of typefaces and alphabets, including script, Roman, Gothic, Japanese, Chinese, and Cyrillic characters. The units are XY stackable and cascadable (built-in synchronizing circuitry forms a display panel of any size). Specs include a 4.5 to 6V dc supply-voltage range, a −20 to +70°C operating range, and 1.6W power dissipation. PD1165, \$27.60; PD1167, \$30.35 (100).

Siemens Components Inc, Optoelectronics Div, 1900 Homestead Rd, Cupertino, CA 95014. Phone (408) 725-3548.

Circle No 354



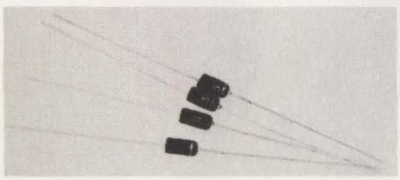
CONNECTOR SHELLS

- *Plastic shell matches die-cast shell for RFI/EMI shielding*
- *Side-lock construction permits easy cable termination*

Complying with IEEE-802.3 requirements and US and European RFI/EMI shielding standards, these plastic connector shells for Ethernet drop cables offer RFI/EMI shielding protection equivalent to die-cast covers. They accept 15-way subminiature D connectors and feature a side-lock construction with a cable ferrule that allows easy cable termination. They are available in a range of colors; you can have your company logo molded into the plastic shell—in most cases at no extra cost. Approximately $1.65.

Ossi Connectors Ltd, Unit C2, Priors Court, Priors Haw Rd, Corby, Northants NN17 1YG, UK. Phone (0536) 200963. TLX 265871.

Circle No 355



TUNING DIODE

- *14:1 min capacitance change*
- *Meets MIL-STD-19500 specs*

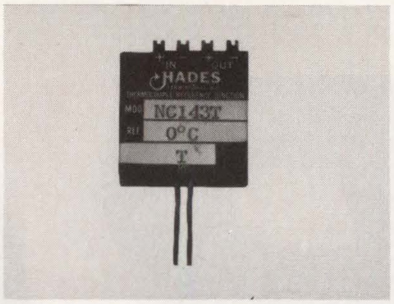
Over a 1 to 10V reverse-bias voltage range, the Type MV1401 tuning diode has more than a 14:1 change in capacitance. With its nominal 1V capacitance of 550 pF, the diode lends itself to broad tuning in the AM band and at somewhat higher frequencies. It has a reverse-voltage rating of 12V, and leakage at 10V measures less than 0.1 μA. Measured at a 2V reverse bias and a frequency of 1 MHz, the figure of merit (Q) equals 200 min. The diode comes in a DO-14-type glass package and meets MIL-STD-19500 environmental specifications. $5.85 (100).

MSI Electronics Inc, 34-32 57th St, Woodside, NY 11377. Phone (718) 672-6500. TLX 426407.

Circle No 356

REFERENCE JUNCTION

- *Operates over −65 to +125°C*
- *Handles all thermocouple materials and power sources*



The Model NC143 thermocouple reference junction is available with any reference temperature setting required, and it can accommodate all thermocouple materials and power sources. Because the module is a miniature full-bridge junction with two mounting holes and either solder terminals or leads, it eliminates the need for ice or electromechanical temperature-simulation devices. The unit is externally energized by 1, 1.35, 5, or 10V dc, as required. Power consumption is as low as 100 μW. Operation spans −65 to

+125°C, and stability is better than ±0.25° at any stabilized ambient temperature between −54 and +100°C. Compensation is available for all thermocouple materials. The output impedance equals 250Ω max for standard units, but other impedances are available on request. $53.10 (100).

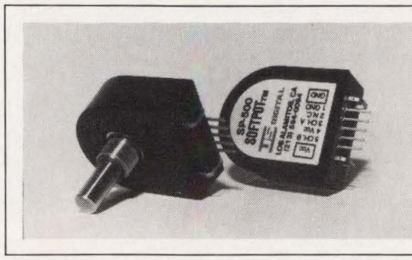
Hades Manufacturing Corp, 151 Verdi St, Farmingdale, NY 11735. Phone (516) 249-4244.

Circle No 357

OPTICAL ENCODERS

- *Draw less than 40 mA*
- *Performance unaffected by aging*

The SP-360, SP-500, and SP-512 optical encoders yield 360, 500, and 512 cycles/revolution, respectively. Their internal electronics, which draw less than 40 mA from a 5V supply, include the single LED, photodetector array, and signal pro-



cessors necessary to produce the devices' 2-channel quadrature TTL-compatible outputs. A rugged Mylar disk, a brass bushing, a stainless-steel shaft, and gold contacts complete the assembly. Each encoder is unaffected by aging or 10% voltage variations; they operate over −40 to +100°C. The torque-loaded shaft in each device simulates the feel of a potentiometer for front-panel applications. A free-spinning shaft is also available. $27 (100).

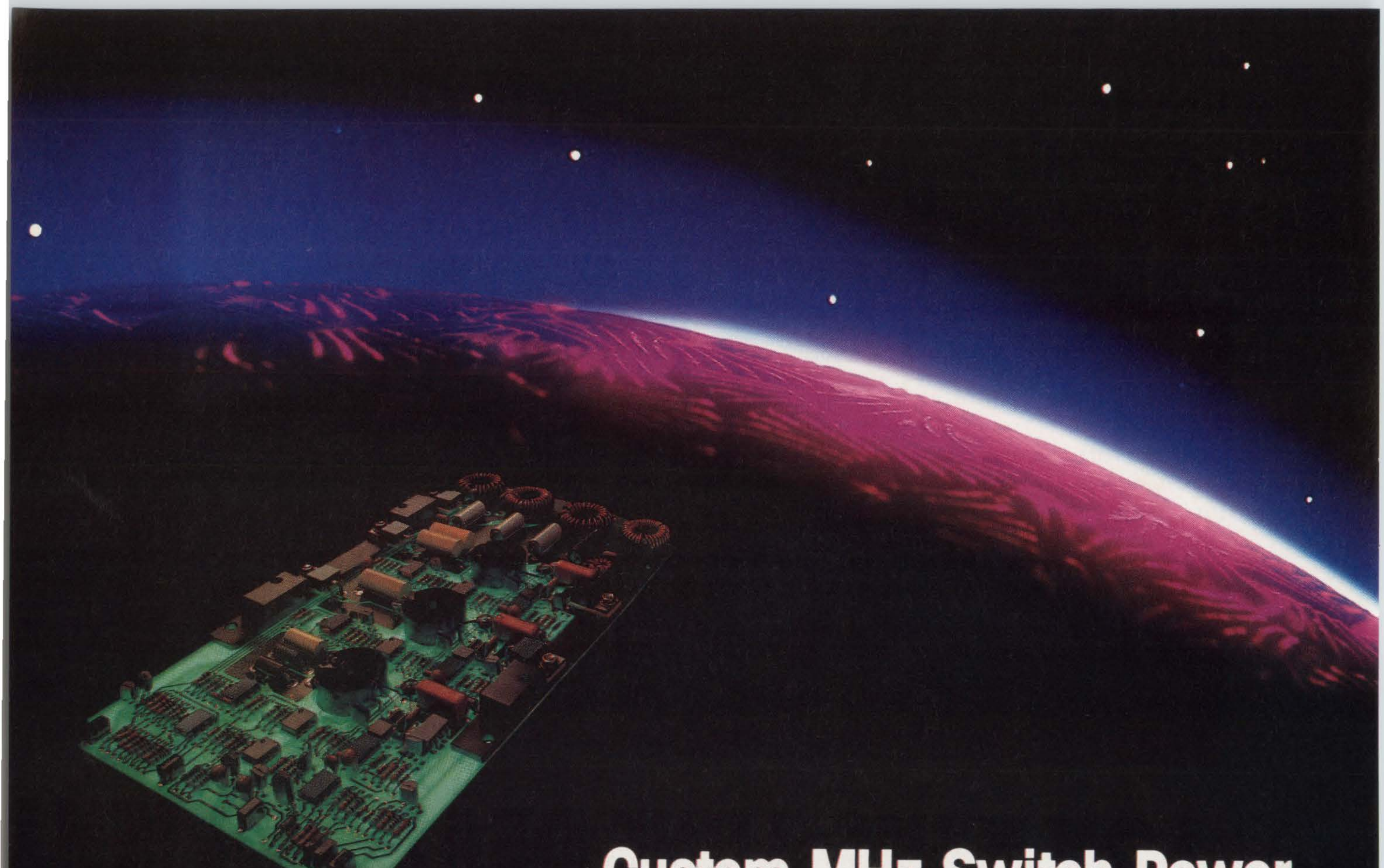
US Digital Corp, 12371 Kensington Rd, Los Alamitos, CA 90720. Phone (213) 594-0094.

Circle No 358

PANEL COUNTER

- *Provides eight input channels with programmable alarm levels*
- *μP controlled with battery backup*

The TC101 counter module allows you to count events on as many as eight inputs simultaneously, with a maximum count capacity of 9,999,999 on each input channel. The ability to preset step sizes on each channel suits the unit to batch-counting applications, and four alarm outputs allow you to generate alarms from any of the eight input channels. You set up the unit via a menu-driven procedure through



Custom MHz Switch Power from Standard Circuitry

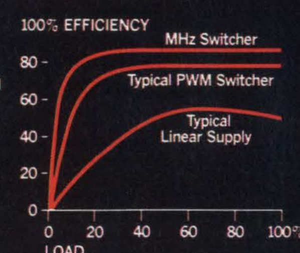
U.S. Pat. No. 4,441,146 and 4,415,959

New Zero Current Switching Technology
Saves Space • Reduces Heat • Increases Reliability

Lorain can put this high frequency converter technology to work for you. Compact, lightweight, multi-cell, zero current switching forward converters deliver up to 200 Watts per cell. All custom designed to your specific communications application from standard circuitry. And cost effective, too!

Over 30 Watts per Cubic Inch

Zero current switching provides the highest power densities available, compared to present day switch mode conversion technology.



80–88% Efficient

Zero current switching significantly reduces heat loss and stress on switching elements. Higher conversion frequencies result in increased life and reliability. Take advantage of Lorain's design and application expertise in high frequency power conversion. We will meet your specifications . . . customizing standard circuitry . . . including bells and whistles. Contact us for additional information, or send us your requirements.

Watts per Cubic Inch

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216-288-1122, Ext. 595

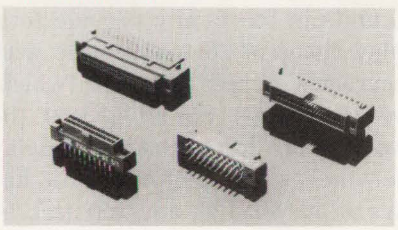
RELIANCE COMM/TEC

CIRCLE NO 88

four front-panel pushbuttons, and you can select any individual channel count for display. You can also display the sum total of events that have occurred on all eight inputs. A security feature limits operator access for viewing and clearing the display, and battery backup of the unit is also provided. The TC101 has panel dimensions of 160×50×110 mm. £120 (10).

Trace Technology Ltd, Swan Works, Box End Rd, Bromham, Beds MK43 8LT, UK. Phone (0836) 261643.

Circle No 359



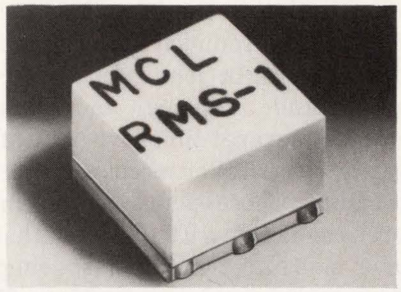
CONNECTORS

- *Handle high-density applications*
- *Contact pitch of 0.05 in.*

PICL Series 2-piece connectors are designed for board-to-board applications. They feature a mating-side contact pitch of 0.05 in.; contact tails have a 0.1-in. contact spacing with four staggered rows 0.075 in. apart. Combinations of straight and right-angle male and female connectors allow vertical, horizontal, and parallel board connections. Devices are available in 30-, 40-, 50-, and 60-contact layouts. Specs include a 0.5A current rating, a 1000V ac dielectric withstanding voltage, a $10^8\Omega$ min insulation resistance, a 25-mΩ max contact resistance, and a −40 to +80°C operating range. From $1.75 (1000). Delivery, stock to eight weeks ARO.

JAE Electronics Inc, 1901A E Carnegie Ave, Santa Ana, CA 92705. Phone (800) 523-7278; in CA and AK, (714) 250-7278. TLX 681438.

Circle No 360



MIXER

- *Spans 500 kHz to 500 MHz*
- *Measures 0.25×0.25 in.*

This surface-mount mixer, the RMS-1, spans a 500-kHz to 500-MHz frequency range and measures only 0.25×0.25 in. It's designed to work with a local-oscillator (LO) output of +7 dBm, but it can operate well at plus or minus several decibels from this level. Conversion loss is 8.5 dB min across the bandwidth. LO to RF isolation (+7 dBm LO power) is better than 44 dB at 62 MHz and greater than 24 dB at 531 MHz. You can attach the mixer to a pc board using conventional manual soldering or with automatic equipment. The mixer is also available in a tape-and-reel format to accommodate pick-and-place machines. $8.95 (100).

Mini Circuits, Box 166, Brooklyn, NY 11235. Phone (718) 934-4500.

Circle No 361

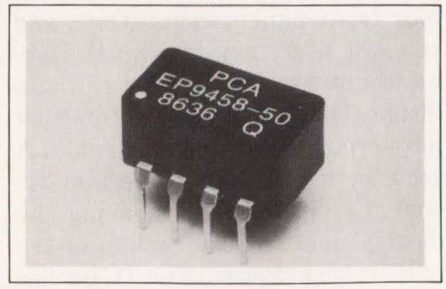
EDGE CONNECTORS

- *Eliminate need for soldering*
- *Offer 15 to 65 positions*

These compliant-pin card-edge connectors reduce assembly time and costs by eliminating the need for soldering. The flexible twin-beam construction in the compliant section and the rounded surfaces provide a gas-tight joint. You can remove and replace individual contacts several times without affecting electrical or mechanical performance. These connectors are interchangeable with devices that have a 0.1×0.2-in. grid spacing. They range in size from 15 to 65 positions and feature selective gold plating. The connectors are available in a number of configurations (including high and low profile) and a choice of card-slot depths, termination lengths, and open or closed ends. Contacts fit on 0.062-, 0.093-, and 0.125-in.-thick pc boards; the maximum insertion force equals 40 lbs, and the minimum retention force per contact is 10 lbs. $0.03 per contact (10,000).

Viking Connectors Co, Box 2379, Chatsworth, CA 91311. Phone (818) 341-4330.

Circle No 362



DELAY LINES

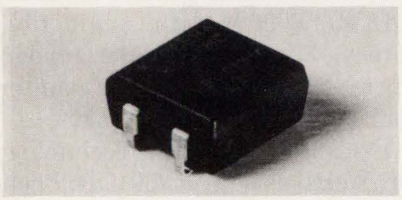
- *Designed for high-density applications*
- *Rise times equal 4 nsec*

Measuring 0.28×0.25 in., EP9458 5-tap, TTL-compatible delay lines are intended for applications where pc-board space is at a premium. The 15 units in the family provide total delay times of 25 to 250 nsec with accuracies of ±5% or 2 nsec (whichever is greater). For all devices, the five taps are located at equal delay increments; the 200-nsec unit has taps at 40, 80, 120, and 160 nsec. A Schottky TTL inverter buffers the

delay-line input and five output taps. Output buffers can drive TTL, low-power Schottky, or Schottky loads. The rise time is 4 nsec max. Operation spans 0 to 70°C. $2 (1000). Delivery, stock to six weeks ARO.

PCA Electronics Inc, 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761.

Circle No 363



OSCILLATOR

- *1- to 50-MHz frequency range*
- *Offers a 3-state output*

The Model KSO-HC surface-mount clock oscillator features a 1- to 50-MHz frequency range and can drive loads as high as 100 pF. It's compatible with TTL and CMOS loads and offers a 3-state output. The oscillator features an initial tolerance of ±100 ppm; an optional 45/55 duty-cycle ratio is available for tight-symmetry applications below 25 MHz. The operating range equals 0 to 70°C. The unit measures 12.45×11.45×5.5 mm. $3.85 (10,000).

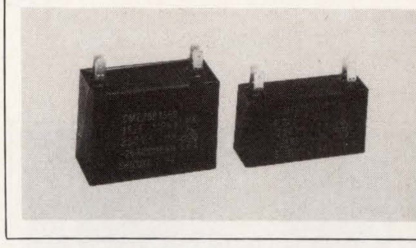
Kyocera Northwest Inc, Electronic Components Group, 11425 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 454-1800.

Circle No 364

CAPACITORS

- *Flame retardant to UL 94V-0*
- *Constructed of self-healing dielectric*

CME Series capacitors are constructed of metallized polyester die-

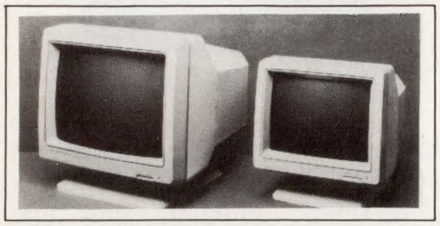


lectric, which is self healing and nonpolar. The capacitors feature a glass-fiber-reinforced, box-type plastic case that's flame retardant to UL specification 94V-0. Capacitance values range from 0.5 through 20 μF. Voltage ratings are 220, 250, 440, and 500V ac, and standard tolerances equal ±10, ±6, +10/−5, and +20/−5%. $0.932 (10,000) for a 5-μF, ±10%, 250V ac unit. Delivery, eight to 10 weeks ARO.

American Shizuki Corp, 21541 Blythe St, Canoga Park, CA 91304. Phone (818) 710-8555. TLX 662633.

Circle No 365

COMPUTERS & PERIPHERALS



GRAPHICS MONITORS

- *Has elliptical-aperture lens*
- *Model achieves 0.2- to 0.4-mm convergence*

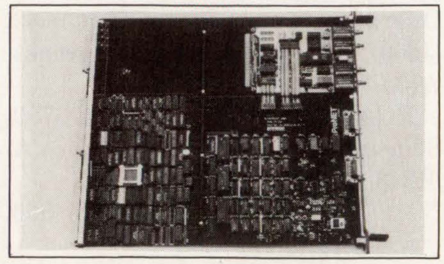
The HM-4119 and HM-4115 monitors feature the elliptical-aperture (EA) lens and HSA (Hitachi slit-winding with auxiliary coil) yoke technologies. Compared with conventional CRT lens techniques, the EA-type lens improves focus by 10%, the manufacturer claims. The HSA yoke achieves 0.3- to 0.5-mm convergence in the 19-in. HM-4119 and 0.2- to 0.4-mm convergence in the 15-in. HM-4115. Both monitors are 60-Hz noninterlaced color monitors with video bandwidths of 100 MHz. The deflection angle of each monitor is 90°, and the monitors use electrostatic focusing and electromagnetic deflection. The HM-4119 features 0.31-mm dot-trio pitch, and the HM-4115 has 0.28-mm dot-trio pitch. HM-4119, $3990; HM-4115, $2200.

Hitachi America Ltd, Office Automation Systems Div, 950 Elm Ave, Suite 170, San Bruno, CA 94066. Phone (415) 872-1902. TLX 176308. **Circle No 366**

NETWORK BOARDS

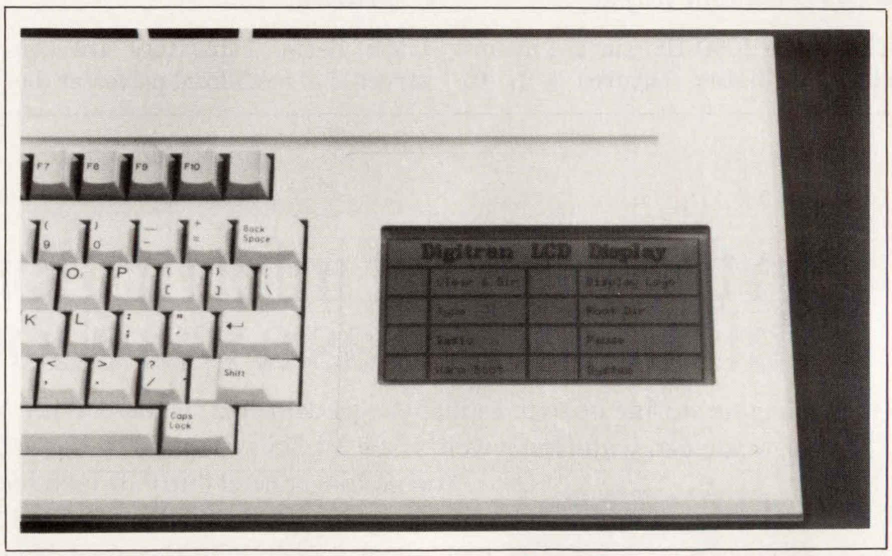
- *Boards for Sun VME Bus link workstations*
- *Direct fiber-optic interface option*

The interface boards of the p1500 Series tie Sun VME Bus workstations into the vendor's Pronet-10 and Pronet-80 local-area networks. The boards are available with a basic interface and a choice of three fiber-optic links that connect directly to the interface boards. Device-driver software is provided along with the boards (these packages complete the integration of the boards into the LAN). The interface boards plug directly into a Sun workstation's backplane. The three varieties of fiber-optic interface are single fiber, dual redundant, and counter rotating. The basic Sun VME Bus interface for Pronet-10 (p1503) costs $2700; with single fiber (p1504), $3800; with dual-redundant fiber (p1505), $4100; with counter-rotating fiber (p1506),



$4350. The basic Pronet-80 board (p1583), $6900; with single fiber (p1584), $9100; with dual-redundant fiber (p1585), $10,000; with counter-rotating fiber (p1586), $10,400.

Protean Inc, Two Technology Dr, Westborough, MA 01581. Phone (617) 898-2800. TLX 928124. **Circle No 367**



KEYBOARD

- *Programmable keyboard uses touchscreen LCD*
- *Comes in IBM PC/XT, PC/AT, ASCII, or custom formats*

The LCD Touch-Screen Keyboard combines an LCD touch panel with a main keyboard. The touch panel measures 5×2¾ in. You can use it as a cursor controller, a programmable keypad, or both. The keyboard is available in IBM PC/XT and PC/AT, ASCII, or custom formats. Using the keypad, you can incorporate macrokey words, short and long strings, or icons in programmed screen options. The bundled software allows you to develop screen formats directly from the keyboard, to increase the number of function keys without retooling, and to save menus or icons on multiple screens. A list of commands for custom menus is provided with the software. $395.

Xcel Corp, 3100 New York Dr, Pasadena, CA 91107. Phone (818) 791-5600.

Circle No 368

COMPUTERS & PERIPHERALS

IMAGE BOARD

- *Allows you to connect a video camera to an IBM PC*
- *Transfers image via modem*

The Professional Image Board allows you to connect a home video camera to an IBM PC. Using readily available components, you can capture, manipulate, and transmit images. The computer can enhance a captured frame on a feature-by-feature basis and store it on a floppy or hard disk. You can then transmit the frozen pictures to remote computers via modem. $595.

ATronics International Inc, 1830 McCandless Dr, Milpitas, CA 95035. Phone (408) 943-6629.

Circle No 369

VME BUS ANALYZER

- *Monitors 72 VME Bus signals*
- *Operates in conjunction with a CRT terminal*

The VME Bus Tracer, a double-Eurocard board, is a testing and debugging tool for VME Bus systems. It has most of the features of a logic-state analyzer; it plugs directly into the VME Bus and passively monitors VME Bus activity. It has an onboard μP and operates in conjunction with a CRT terminal for control and display purposes. In addition, it includes a Centronics-compatible interface for hard-copy output of the captured trace data. You can clock the data capture memory synchronously or asynchronously at frequencies to 16 MHz. The analyzer can capture 1024 states of 72 VME Bus signals, including address, 16-bit data, handshake, and control lines. Its trigger facilities include the capability to capture only those data-bus transfers occurring either inside or outside of a specified VME Bus address range. Approximately $4900.

Vmetro a/s, Box 122, Leirdal, 1008 Oslo 10, Norway. Phone (47) 6906271.

Circle No 370

COMPUTERS & PERIPHERALS

PORTABLE COMPUTER

- *Handheld computer with 8-bit μP*
- *Calculator functions included*

The Advanced Pocket Computer (APC) features an 8-bit μP, 64k bytes of internal memory, and expansion capability to 256k bytes of RAM and EPROM. It also has a full alphanumeric keyboard, an LCD organized as two lines of 16 characters each, and an RS-232C link, which operates at speeds from 50 to 9600 baud. The APC measures 5.6×3.1×1.1 in. and weighs 10 oz. The device uses a single 9V alkaline battery. In addition to computing and communications functions, the APC provides calculator and real-time date and time clocks. The computer's operating system and programming language reside in 32k bytes of ROM; 32k bytes of RAM are provided for data storage. The device's memory capacity may be expanded through the use of optional plug-in memory modules, which are available in capacities of 16k, 32k, 64k, or 128k bytes. $295. Delivery, four to six weeks ARO.

Hand Held Products, Box 2388, Charlotte, NC 28211. Phone (704) 541-1380.

Circle No 371

3-D DIGITIZER

- *Digitizes solids in a noncontact fashion*
- *Can digitize live subjects as well as inanimate objects*

The Rapid 3D Digitizer camera/computer digitizes any 3-D object regardless of its material composition, including live subjects. The camera circles the subject or object in 15 sec and obtains 500,000 points, which are reduced to 250,000 coordinates. You can then use the coordinates to reproduce the object for computer graphics or for solid modeling. You can also feed the information into a computer-controlled mill that cuts solid reproductions. Because the camera has no contact with the object being reproduced, the object is not deformed by the reproduction process. Resolution of the system is such that features as small as 0.028 in. can be captured in digital form on a 14-in.-diameter object. The system achieves an accuracy of 1% over the entire digitized surface. This figure means that any given feature will be within 1% of its actual position. $40,000. Delivery, 60 days ARO.

Cyberware Laboratory Inc, 2062 Sunset Dr, Pacific Grove, CA 93950. Phone (408) 373-6224.

Circle No 372

ESDI CONTROLLER

- *ESDI disk controller for the VME Bus*
- *Sustained data-transfer rates of 6M bytes/sec*

The Rimfire 3400 disk controller is an ESDI caching disk controller for the VME Bus. The device is capable of 20M-byte/sec burst-transfer rates from the controller to the bus by means of a short-burst FIFO gate array; it can transfer data at sustained rates of 6M bytes/sec. Disk access is enhanced through the use of a 512k-byte configurable cache memory and onboard firmware. The controller can review pending disk-access requests and optimizes seeks and caching by means of multiple circular-command queues in system memory. The controller runs four ESDI disk drives. $1995.

Ciprico Inc, 2955 Xenium Lane, Plymouth, MN 55441. Phone (612) 559-2034.

Circle No 373

DISPLAYS

- *Display terminals feature overscanned background*
- *Provide bit-mapped graphics*

The Visual 600 Integrated Image Display Station Series employs bit-mapped technology, which allows the display's internal 16-bit processor to address each pixel on the screen. (In contrast, purely text-based displays divide the screen into a matrix of character locations and do not permit the manipulation of individual pixels.) The 600 Series features a white-phosphor, dark-glass, nonglare flat screen that has a 70-Hz refresh rate with a horizontal frequency of 32 kHz. The screen has 1056×400-pixel resolution. From $695 to $725.

Visual Technology Inc, 1703 Middlesex St, Lowell, MA 01851. Phone (617) 459-4903.

Circle No 374

I/O FOR MAC

- *Links Macintosh to the STD bus*
- *Performs front-end I/O processing for the Mac*

The Model 3A SCSI/IOP adds an industrial I/O bus to the Macintosh Plus for industrial, scientific, and educational applications. The SCSI/IOP connects to the SCSI port of the

New Kepco/TDK 150KHz Switching Power Supply, SERIES RBX

This brand new product of advanced Kepco/TDK technology squeezes more power into less space than you'll find most anywhere else. It's a highly efficient, FET-based, fast-responding switcher operating at 150KHz.

The Kepco/TDK Series RBX gives you remote on/off, remote voltage control, remote error sensing, overvoltage and undervoltage protection, rectangular current limiting, an "output OK" LED, selectable 115/230V input, and a current balance circuit which lets you parallel up to three units and have them share the load.

Model	RBX 02-120K	RBX 05-120K	RBX 12-50K	RBX 24-25K	RBX 48-12.5K
Volts	2V	5V	12V	24V	48V
Adjustment	1.6-2.2V	4.0-5.5V	9.6-13.2V	19.0-26.5V	38.4-52.8V
Amps	0-120A	0-120A	0-50A	0-25A	0-12.5A
OVP	2.6-2.8V	6.0-6.5V	14-14.5V	27-27.5V	55-57V
Current limit	125-145A	125-145A	52-60A	26-30A	13-15A
Efficiency	65%	80%	80%	85%	85%
Dimensions	$3\frac{1}{4}$" x $7\frac{7}{8}$" x $8\frac{11}{16}$" plus $\frac{3}{4}$" for connectors				
Safety	UL478, CSA C22.2-154				
Prices	$675 (OEM quantity discounts available)				

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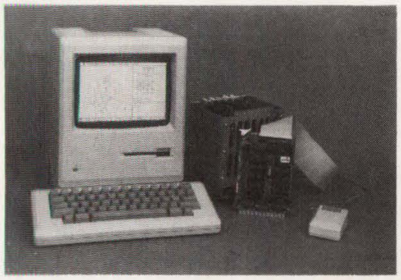
CIRCLE NO 122



MAC Plus by means of a ribbon cable and plugs directly into an STD Bus card cage and backplane. Using the SCSI/IOP, the Macintosh acts as an STD Bus CPU. The CPU, in turn, provides access to a wide variety of real-time data acquisition and control interfaces, such as analog I/O, digital I/O, and ac power control. Firmware on the SCSI/IOP includes reading and writing I/O ports and memory, as well as downloading and executing tasks. The product supports the STD Bus interrupt architecture and performs the role of a front-end processor for a Macintosh real-time I/O. $119.

Ampro Computers Inc, Box 390427, Mountain View, CA 94039. Phone (415) 962-0230. TLX 4940302.

Circle No 375

DISK DRIVES

- *20M-byte, 5¼-in., removable-cartridge disk drives*
- *Available with either SCSI or ST506/412 interface*

The RH5260 (ST-506) and RH5261 (SCSI) 20M-byte, 5¼-in., hard-disk drives offer unlimited storage capacity by using hard-media cartridges that you can remove, transport, and interchange with other compatible drives. A proprietary track-runout compensation technique lets you adjust the disk to ensure cartridge interchangeability between units. The drives can read 10M-byte, 5130 cartridges. RH5260, $1046; RH5261, $1126.

Ricoh Systems Inc, 2071 Concourse Dr, San Jose, CA 95131. Phone (408) 946-6200.

Circle No 376

DIGITIZER

- *Optical page scanner for the Macintosh*
- *Provides black-and-white or halftone modes*

The TurboScan optical page scanner converts color or black-and-white text, handwriting, artwork, and photographs into digitized bit information for processing by the Apple Macintosh. The scanner digitizes with a maximum resolution of 300×300 dpi. The interface between the scanner and the Macintosh is an RS-232C/RS-422 port. The scanner provides two basic scanning modes: line-art mode for black-and-white materials and halftone mode for documents with continuous shad-

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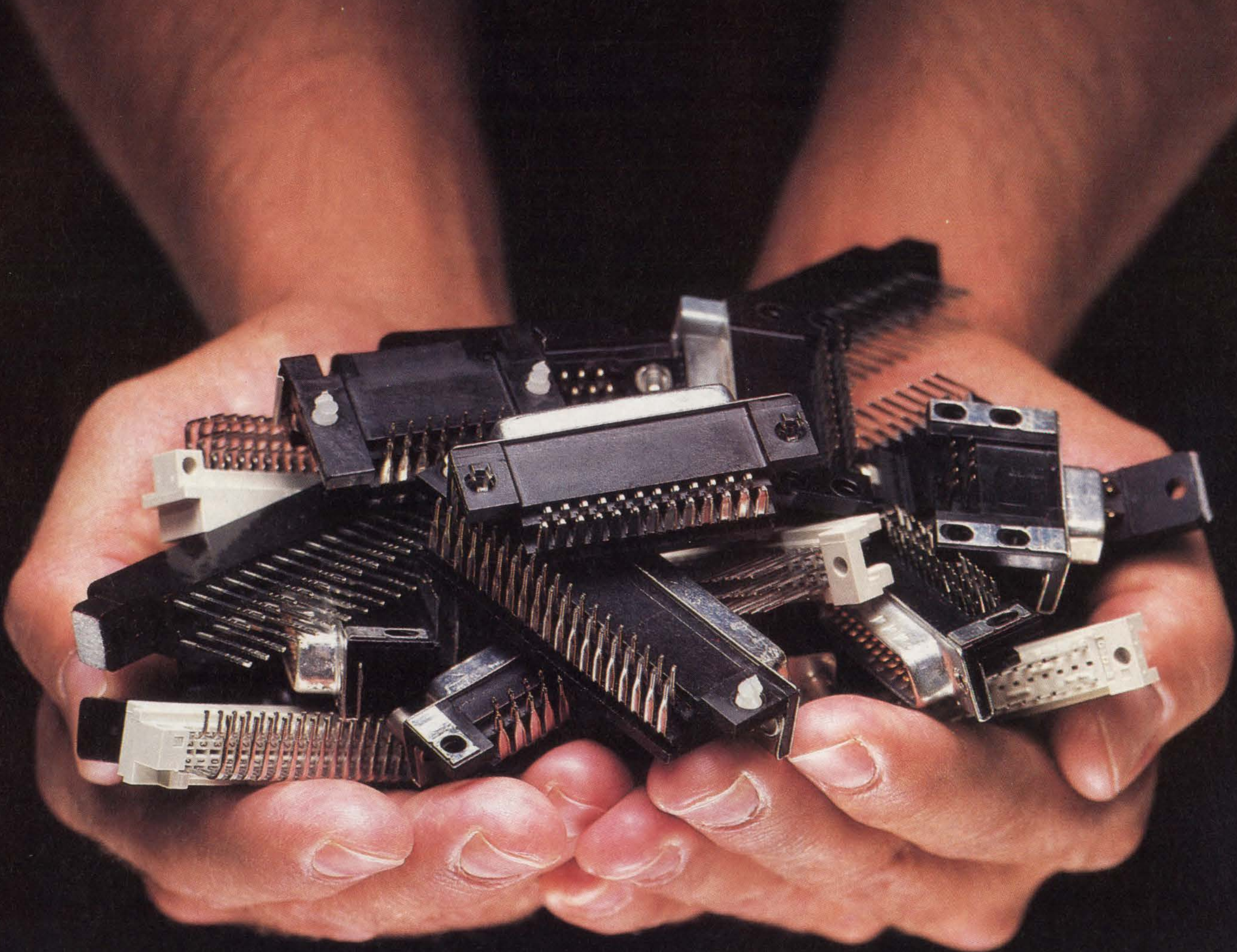

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- Surface mount
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Printed Circuit Card Edge
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Pin Headers
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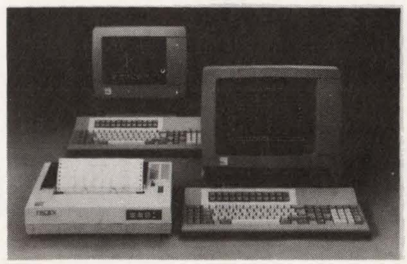
P.O. Box 37, Inman, SC 29349 • 803/472-4141 • Telex II 810/690-2302 • Fax No. 803/472-8568 ing. In the line-art mode, the scanner converts the scanned image, including any shades of gray, into a black-and-white image. In halftone mode, the scanner simulates the shades of the original image. $2395.

AST Research, 2121 Alton Ave, Irvine, CA 92714. Phone (714) 863-1333.

Circle No 377



COMM BOARD

- *Onboard 80186 processor operates at 8 MHz*
- *Board works with Unix and MS-DOS*

Smartport is an intelligent serial-communications board for the IBM PC/AT and 80386-based computers. It incorporates an onboard 80186 processor operating at 8 MHz, contains 64k bytes of dual-ported RAM, and offers a choice of either four or eight RS-232C ports. The board operates under MS-DOS, Unix, or other multitasking/multiuser operating systems. The onboard processor and dual-ported RAM offload the serial-communications tasks from the PC. The PC loads a block of data into the dual-ported RAM and indicates to Smartport that it should be transmitted. The board buffers incoming data in the dual-ported RAM, where the data resides until the PC reads it out. The board uses an onboard operating system known as Box (Basic Onboard eXecutive), which provides the basic functions, such as baud-rate changing and status checking that are needed to use the board. The vendor supplies a technical manual that lists all the Box function calls and examples of their use. Source code is also available for custom applications. Smart-4, $895; Smart-8, $1295; PC-DOS and Xenix drivers, $25 and $50, respectively.

Arnet Corp, 476 Woodycrest Ave, Nashville, TN 37210. Phone (615) 254-0646.

Circle No 378

TERMINALS

- *Display terminals include 122-key adjustable keyboards*
- *Printer terminals have speeds as high as 800 lines/minute*

The 3X Series includes four display and four printer terminals. Each of the display terminals displays as many as 1920 characters and has

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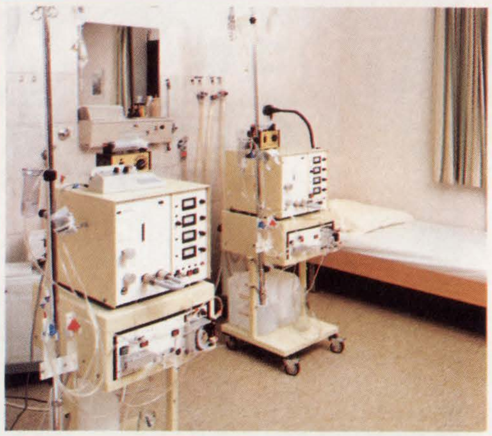

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Security/Fire alarm systems
Telecommunications

Primary Power–
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Robots
Wheelchairs
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CIRCLE NO 124

122-key adjustable keyboards. Each also buffers as many as 1500 keystrokes and has a printer port that allows you to attach a local screen printer. The monochrome display terminals are Models 078-2 and 180-2. The 078-2 has a 12-in. display and is available with green or amber phosphor; it costs $1295. The 15-in. 180-2 is plug compatible with IBM's 3180-2 and costs $1995. The color display terminals, Models 079-2 and 179-2, each display 7 colors. The 079-2, which sells for $1895, has a 12-in. display. The 179-2 has a 14-in. display and costs $2095. The four printer terminals are Models 201, 851, 214XP, and 225. The 201, a message printer, operates to 220 cps in draft mode and costs $545. The 851 ink-jet printer/terminal prints at as much as 220 cps in draft mode; it costs $775. The 214XP, which can reach 400 cps, sells for $5100. The 225, a plug-compatible replacement for the IBM 5225, prints 800 lines/minute in draft mode and costs $12,800.

Telex Computer Products, 6422 E 41st St, Tulsa, OK 74135. Phone (918) 627-1111.

Circle No 379

VOICE/DATA MUX

- *Simultaneously transmits voice and data*
- *Uses standard 2-wire, voice-grade cables*

The Linemate 96 Plus multiplexer transmits voice and data information simultaneously over twisted-pair phone lines between terminals and a central computer. The unit contains a full-duplex asynchronous FSK modem capable of operating at bit rates as high as 9600 bps. You can also use the modem at synchronous speeds of 2400, 4800, and 7200 bps by adding an optional interface card. The multiplexer can transmit data over distances as long as 8 mi on unloaded 2-wire cable, and data transfer is completely transparent during normal telephone operation, including dialing, supervisory, and ringing periods. The Linemate 96 Plus is available as a stand-alone desktop unit or as a board-level product. £233.

Trend Datalink Ltd, Knaves Beech Estate, Loudwater, High Wycombe, Bucks HP10 9QE, UK. Phone (06285) 28112. TLX 849408.

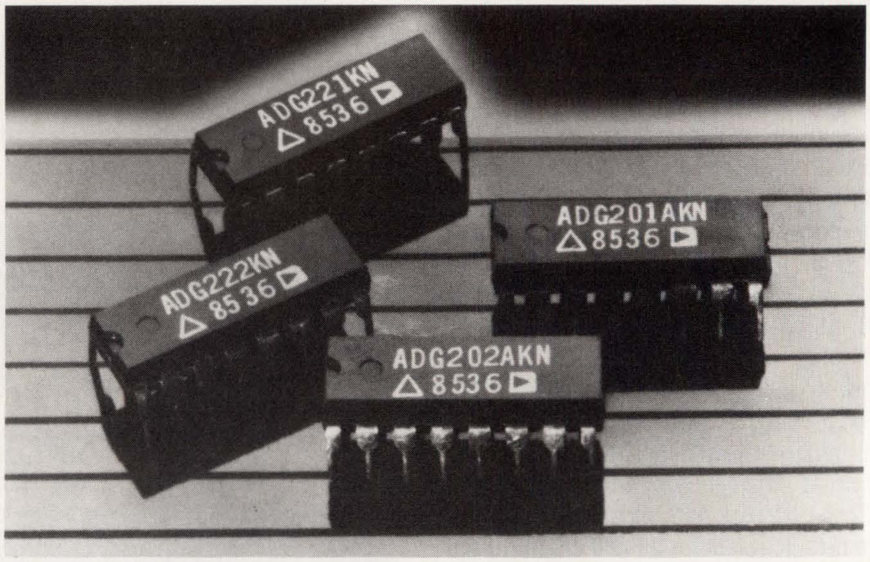
Circle No 380

NEW PRODUCTS

INTEGRATED CIRCUITS

CMOS SWITCHES

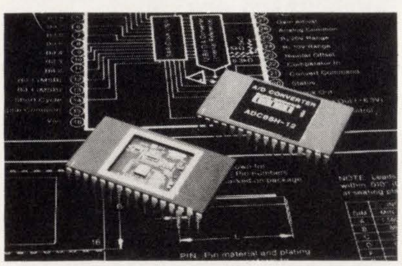
- *Onboard address latches available*
- *Feature a 44V max power-supply rating*



Models ADG201A and ADG202A are quad spst CMOS analog switches that feature a 44V max power-supply rating and typical current leakages of 500 pA. Models ADG221 and ADG222 offer the same leakage and power-supply ratings but also include onboard address latches that simplify the interface to μPs. According to the manufacturer, the ADG222 is the first CMOS switch that closes in response to a logic one at the address input. (The ADG221's switches close when the address level is low.) All switches offer a signal range of ±15V and single-supply (15V) operation. Fabricated with junction-isolated CMOS technology, the devices come in plastic or ceramic DIPs, LCCs, and PLCCs for the commercial, industrial, or military temperature ranges. ADG201A and ADG202A, from $3.15 and $2.95, respectively; ADG221 and ADG222, from $2.56 (100). Allow 12-week delivery for the military version.

Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577.

Circle No 381



A/D CONVERTERS

- *Improved versions of industry standards*
- *Offer monolithic D/A-converter chip*

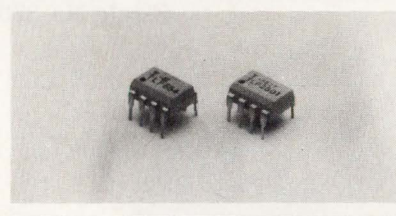
Improved versions of the company's industry-standard ADC84/85 A/D converters feature a monolithic D/A-converter chip and a CMOS gate array. These 12-bit converters offer 50% lower power dissipation (725 mW max) and 15 to 20% lower prices than the company's earlier models. The conversion time is 10 μsec for 12 bits and 6 μsec for 10 bits. Housed in 32-pin hermetic side-brazed DIPs, the converters specify monotonicity for the commercial, industrial, and military operating temperature ranges. The parts provide output data in parallel and serial form and operate from supply voltages of ±12 to ±15V, and 5V. From $62 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 382

OPTOCOUPLERS

- *Combine GaAlAs LEDs with high-gain photodetectors*
- *Have open-collector, Schottky-clamped transistor outputs*



The TLP554 and TLP2601 optocouplers combine GaAlAs (gallium aluminum arsenide) infrared LEDs with high-gain photodetectors. The outputs are open-collector, Schottky-clamped transistors. A Faraday shield integrated on the photodetector chip shunts capacitively coupled common-mode noise to ground; the shield provides a common-mode transient immunity of 1000V/μsec by reducing the effect of capacitive coupling between the input LED and the detector. The devices operate over −40 to +85°C. $4.37 (100). Delivery, eight to 10 weeks ARO.

Toshiba America Inc, ECBS, Semiconductor Products Div, 2692 Dow Ave, Tustin, CA 92680. Phone local office.

Circle No 383

A FULL DECK OF STATICS MAKES CENTS

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HYUNDAI CMOS SRAMs

Product	Part No.	Orgn.	Access Time (ns)	Packaging
16K SRAM	HY6116	2Kx8	100,120,150	24-pin DIP (600)
16K SRAM	HY61C16A	2Kx8	25,35,45,55,70	24-pin DIP (300/600)
16K SRAM	HY61C67	16Kx1	25,35,45,55,70	20-pin DIP (300)
16K SRAM	HY61C68	4Kx4	25,35,45,55,70	20-pin DIP (300)
16K SRAM	HY61C69	4Kx4	25,35,45,55,70	22-pin DIP (300)
64K SRAM	HY62C64	8Kx8	100,120,150	28-pin DIP (600)
64K SRAM	HY62C64A	8Kx8	35,45,55,70	28-pin DIP (600)
64K SRAM	HY62C87	64Kx1	35,45,55	22-pin DIP (300)
64K SRAM	HY62C88	16Kx4	35,45,55	22-pin DIP (300)
256K SRAM	HY62C256	32Kx8	55,70,90	28-pin DIP (600)

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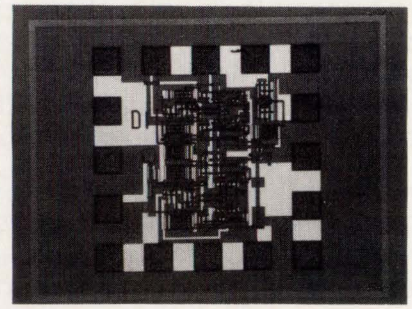
CIRCLE NO 132

INTEGRATED CIRCUITS



GaAs PRESCALER

- *3-GHz, divide-by-4 device*
- *Operates over military and commercial temperature ranges*

The monolithic ADV 3040 is a gallium arsenide, 3-GHz, divide-by-4 prescaler for microwave and high-frequency-synthesizer applications. The device provides ECL-compatible output levels over the range 0.8 to 3 GHz, and it operates over the military and commercial temperature ranges. Specifications include −130-dBc/Hz phase noise, 50Ω input impedance, and a 1.5:1 input VSWR. Single-sideband phase noise at 10 kHz does not contribute to the noise sidebands of a microwave source locked in a wideband phase-locked loop, nor does that phase noise add to the noise floor of a phase-locked signal source when that source uses a 10-MHz crystal as its reference. Commercial-grade version in an 8-pin flat pack, $77 (1000).

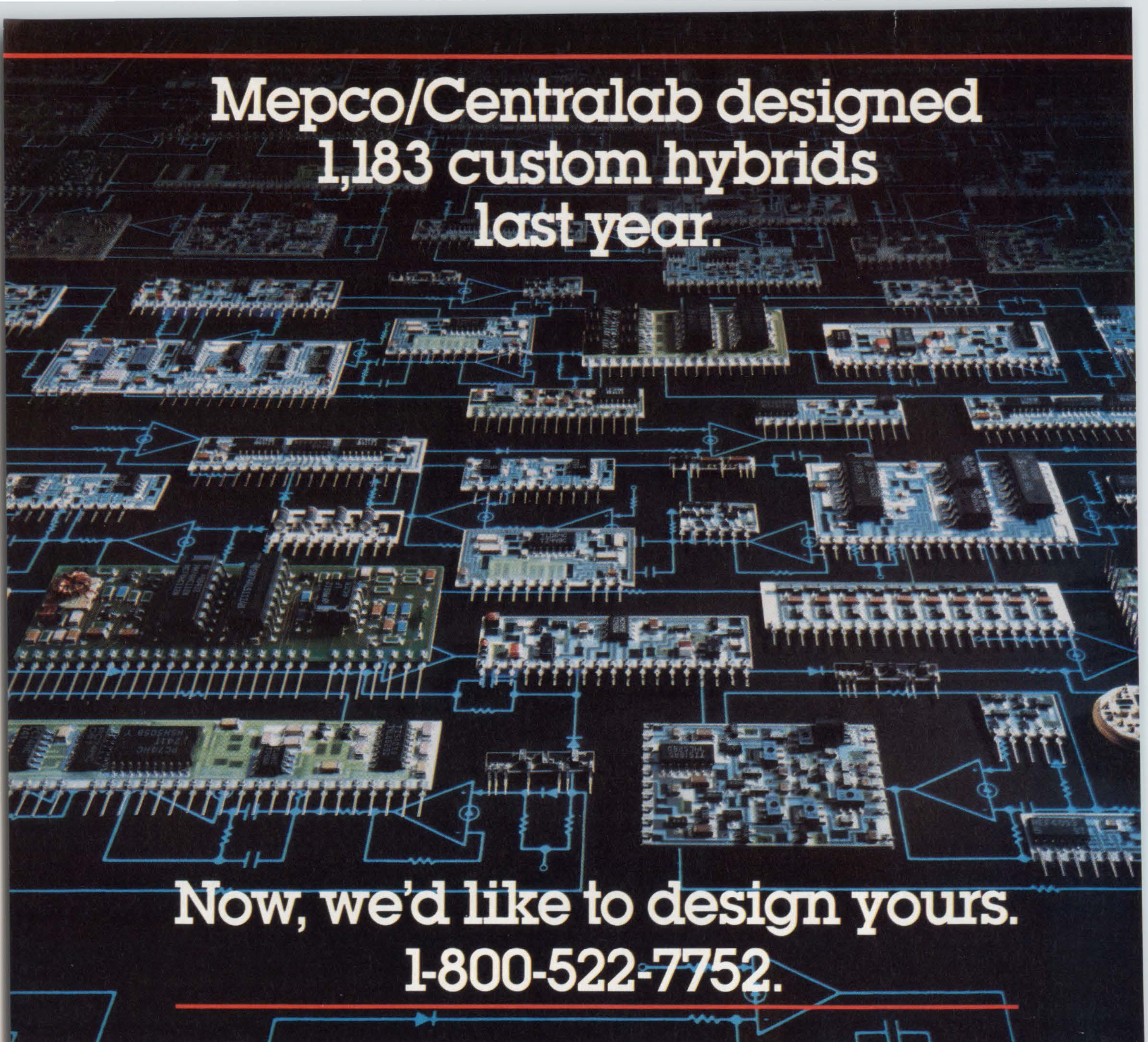
Anadigics Inc, 35 Technology Dr, Warren, NJ 07060. Phone (201) 668-5000. TLX 510-600-5741.

Circle No 384

MICROPROCESSOR

- *Accommodates Forth language slice*
- *Operates at clock frequencies to 10 MHz*

The NC6000 μP accommodates the Forth language slice using stack controllers that can access 512 words of external stack memory, and it has six bits of additional stack addressing to function as a process



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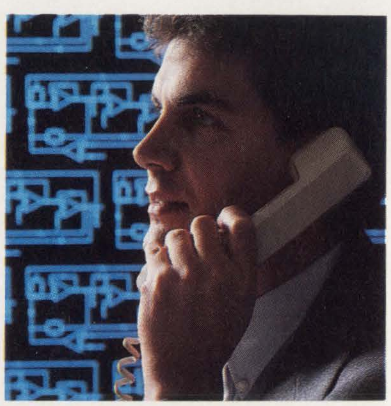

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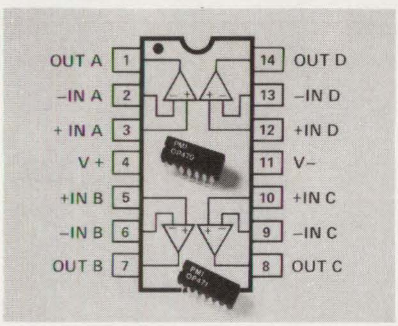
CIRCLE NO 131

identifier. The µP thus accommodates 64 pages of 512 words on its stacks. Incorporating 6000 gate arrays fabricated from a 2-µm CMOS process, the device operates at clock frequencies as high as 10 MHz. The chip contains no microcode and directly executes the Forth language. Throughput and cycle time are 13 to 16 MIPS and 100 nsec, respectively. Versions in a 121-lead (NC5000) and a 144-lead pin-grid array (NC6000) cost $270 and $340, respectively.

Novix Inc, 19925 Stevens Creek Blvd, Suite 280, Cupertino, CA 95014. Phone (408) 255-2750.

Circle No 385



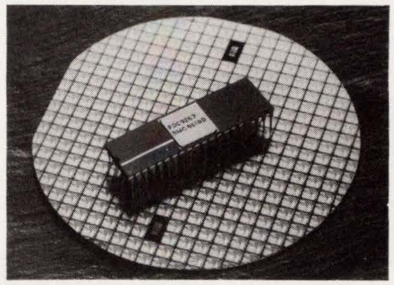
QUAD OP AMP

- *Has voltage noise of 5 nV/√Hz at 1 kHz max*
- *Has 25-nA bias current max*

The OP-470 quad op amp features a low voltage noise of 5 nV/√Hz at 1 kHz max, a 400-µV max input offset voltage, and less than 2-µV/°C input offset drift over the military and industrial temperature ranges. Other specs include a 25-nA max bias current, a 10^6 open-loop gain, 110-dB CMR, a 115-dB PSR, a 2V/µsec slew rate, a 6-MHz gain-bandwidth product, and unity-gain stability. Its 40-pin ceramic DIP conforms to the industry-standard pinout for quad op amps. Industrial grade, $6.50; military grade, $17.90 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 910-338-0218.

Circle No 386



DISK CONTROLLER IC

- *Comes in 40-pin DIP or 44-lead PLCC*
- *Suitable for use with IBM PC/AT*

The FDC9267 is a monolithic floppy-disk controller IC that's software-compatible with the industry-standard FDC765A. Housed in a 40-pin DIP or 44-lead plastic leaded chip carrier, the FDC9267 is suitable for use with the IBM PC/AT's 1.2M-byte drive, as well as with 3.5-in., 5.25-in., and 8-in. single- or double-sided drives that use single-density (FM) or double-density (MFM) encoding. The device includes all the logic necessary for write precompensation. It also has a self-tuning analog-data separator that eliminates tuning during operation, because an internally derived and filtered error signal controls the voltage-controlled oscillator's center frequency. Plastic-DIP version, $14.95 (100). Delivery, six to eight weeks ARO.

Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100. TWX 510-227-8898.

Circle No 387

DUAL DRIVER IC

- *Drives 2A with 0.6V dropout into resistive or inductive loads*
- *Incorporates alarm outputs to indicate overload conditions*

By incorporating a dc/dc converter to generate a base drive voltage greater than V_{CC}, the two independent emitter output drivers in the UAF1780 high-side switch deliver

as much as 2A into their loads with a dropout voltage of 0.6V typ (0.7V max). The dc/dc converter requires one inductor (typically 100 μH) and one capacitor (typically 47 μF or greater) to operate. Both output stages incorporate adjustable current limiting, thermal overload protection, and desaturation monitoring circuitry, which detects overloads and short circuits. The outputs turn off, and an open-collector alarm output is activated, in the event of prolonged output desaturation or excessive power dissipation. A reset input reactivates the drivers, and a strobe input simultaneously switches off both outputs. A reference-voltage input allows you to set the threshold voltage of the reset, strobe, and channel control inputs. The UAF1780 operates from 8 to 32V over −40 to +85°C. In a 16-pin plastic DIP, approximately $11; 15-pin Multiwatt SIP, approximately, $15 (100).

Thomson Semiconducteurs, 45 ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 240780.

Circle No 388

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, Texas 75006. Phone (214) 466-6000.

Circle No 389

CTCSS CODEC

- *Generates 38 programmable CTCSS subaudible tones*
- *Has parallel and serial interfaces for μP control*

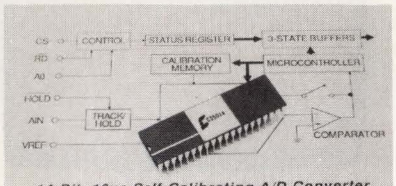
Targeted for use in radio-communication systems, the FX365 CTCSS (continuous tone controlled squelch system) encoder/decoder features a μP interface that allows you to generate, encode, and decode 38 subaudible tones between 67 and 250 Hz. In addition, the μP interface allows you to switch between transmit and receive modes, and to override the tone-decoding circuitry so that you can monitor a received audio signal. The μP interface operates in parallel or serial mode. In the parallel mode, a latch-enable input loads control data into an internal latch; in the serial mode, you can load control data via a serial port and clock inputs. The IC has an on-chip highpass filter with a 300-Hz cutoff frequency, which you can switch into the transmit or receive signal path, to provide audio prefiltering or rejection of the received CTCSS tones, respectively. The FX365 operates from a 5V supply and draws 3.5 mA typ. On-chip clock circuitry generates all frequency timing from a 1-MHz crystal or an external clock source. The device is available in a 24-pin DIP or in a 24- or 28-pin surface-mount package. Approximately £7.75 (1000).

Consumer Microcircuits Ltd, Wheaton Rd, Industrial Estate East, Witham, Essex CM8 3TD, UK. Phone (0376) 513833. TLX 99382.

Circle No 390

Mx-Com Inc, 4800 Bethania Station Rd, Winston-Salem, NC 27105. Phone (919) 744-5050.

Circle No 391



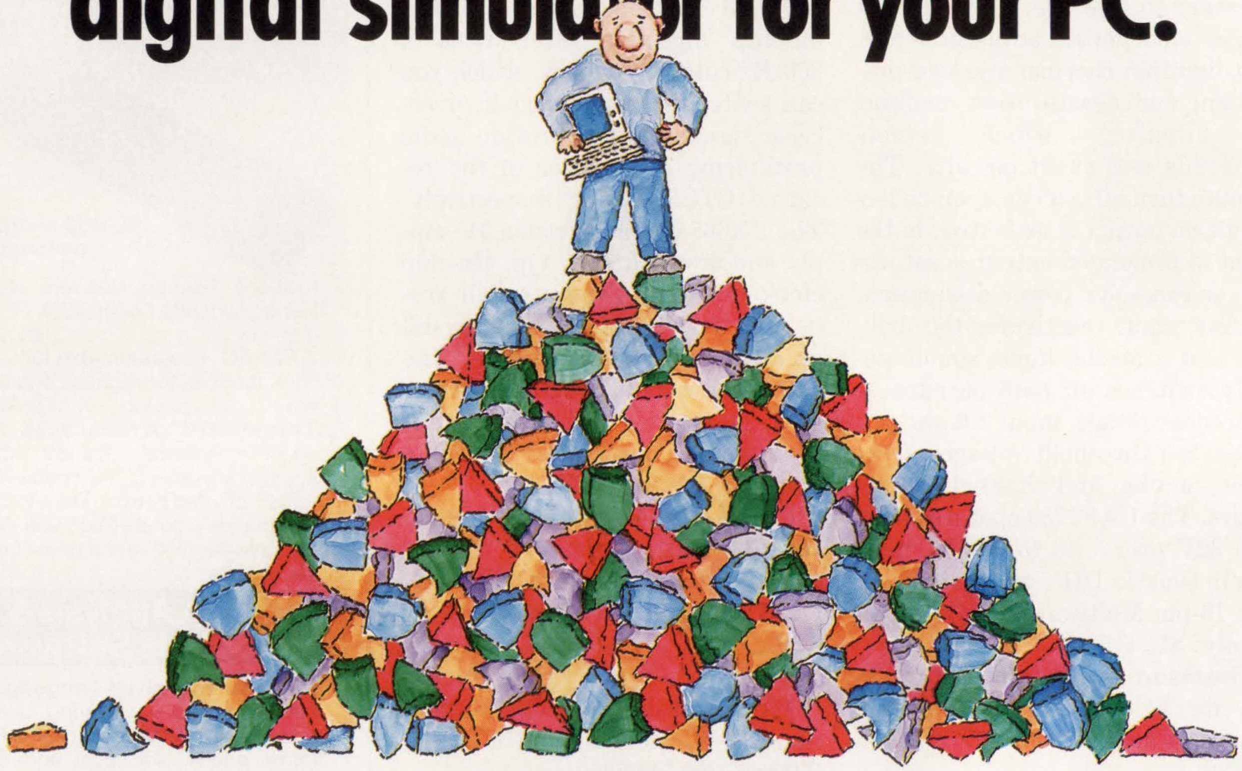
14-Bit, 16us Self-Calibrating A/D Converter

A/D CONVERTER

- *Self-calibrating device*
- *Offers 14-bit absolute accuracy*

The CS5014 is a self-calibrating, 14-bit A/D converter that maintains 14-bit absolute accuracy over time and temperature without external calibration—that is, the nonlinearity error remains within 0.5 LSB, with no missing output codes. The chip has a track-and-hold input, 3-state output buffers, digitally selectable unipolar and bipolar input ranges, and an 8-bit status register

MICRO-LOGIC II.™
The CAE tool with a 10,000-gate digital simulator for your PC.

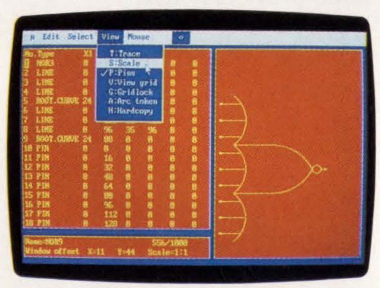


Spectrum Software's MICRO-LOGIC II® puts you on top of the most complex logic design problems. With a powerful total capacity of 10,000 gates, MICRO-LOGIC II helps engineers tackle tough design and simulation problems right at their PCs.

MICRO-LOGIC II, which is based on our original MICRO-LOGIC software, is a field-proven, second-generation program. It has a high-speed event-driven simulator which is significantly faster than the earlier version.

Timing Simulator

The program provides you with a top-notch interactive drawing and analysis environment. You can create logic diagrams of up to 64 pages with ease. The software features a sophisticated schematic editor with pan and zoom capabilities.



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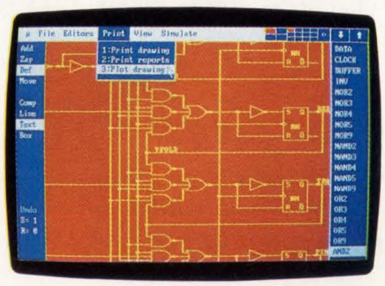
A 200-type library of standard parts is at your fingertips. And for a new high in flexibility, a built-in shape editor lets you create unique or custom shapes.

MICRO-LOGIC II is available for the IBM® PC. It is CGA, EGA, and Hercules® compatible and costs only $895 complete. An evaluation version is available for $100. Call or write today for our free brochure and demo disk. We'd like to put you in touch with a top digital solution.

- Total capacity of 10,000 gates
- Integrated schematic editor
- Fast assembly language routines
- Standard parts library of 200 types
- Event-driven timing simulator

CIRCLE NO 130

- Built-in shape editor
- Multiple delay models
- Printer and plotter hard copy



Schematic Editor

spectrum

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Sunnyvale, CA 94087
(408) 738-4387

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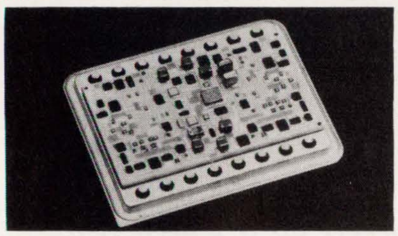
that contains conversion and calibration information. The typical power dissipation is 150 mW. The ADC comes in a 40-pin DIP and is available in 16- and 32-μsec conversion-time versions that are specified for the commercial, industrial, and military temperature ranges. CDB5014 evaluation board including socketed CS5014, $200. CS5014, from $45 (100).

Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222. TWX 910-874-1352.

Circle No 392



DUAL LINE DRIVER

- *Exceeds specs of MIL-STD-188-114A for Type III*
- *Available in a 16-pin, sealed DIP*

Model CSH-192 is a hybrid, dual-channel line driver that exceeds the enhanced performance requirements of MIL-STD-188-114A for Type III devices. The part, housed in a 16-pin, hermetically sealed DIP, includes 3-state, TTL- and ECL-compatible outputs, whose drive capability (25 mA min) is suitable for driving balanced lines such as twisted pairs, coaxial cable, or parallel-wire transmission lines. Output rise and fall times (10 nsec) and propagation delay (35 nsec) allow transmission rates to 10M bps. The driver requires ±5V, 1.76W max. MIL-STD-883B versions are also available. $195 (100). Delivery, 8 to 10 weeks ARO.

Leach Corp, Control Products Div, 6900 Orangethorpe Ave, Buena Park, CA 90620. Phone (714) 739-0770. TWX 910-596-2867.

Circle No 393

SATELLITE TV IC

- *Decodes D2-MAC/Packet standard satellite transmissions*
- *Handles multiple sound channels and data services*

When used in conjunction with other ICs in the Digit-2000 digital-TV chip set, the DMA 2270 D2-MAC decoder IC forms a high-quality, multistandard direct-broadcast-satellite (DBS) TV decoder. It also suits cable-TV applications. The DMA 2270 accepts a digitized baseband signal and includes circuitry for video clamping, automatic gain control, and phase locking of the system clock to the D2-MAC transmission. It also includes luma and chroma stores to regenerate a 13.5-MHz luminance signal and a 6.75-MHz color-difference signal; a contrast multiplier; a color-saturation multiplier; a sync and blanking pulse generator; and a sound decoder and demultiplexer. The device, which is housed in a 68-pin plastic LCC, also handles multiple sound channels and data services. It's software controlled via an IM Bus interface. The chip set, including the DMA 2270 and the four other Digit-2000 devices necessary to build a stand-alone D2-MAC decoder, costs approximately DM 200 (OEM qty).

ITT-Intermetall, Hans-Bunte-Strasse 19, 7800 Freiburg, West Germany. Phone (0761) 517337. TLX 772715.

Circle No 394

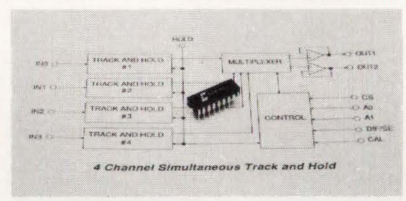
CMOS PALs

- *Have mask-programmable architecture*
- *Draw 100 μA max in standby mode*

The ZHAL20A and ZHAL24A Series programmable-logic circuits draw 100 μA max in standby mode and 3 mA/MHz while active. These 35 ZHAL (zero-power hard array logic) devices can implement most of the current 20- and 24-pin PAL/HAL (hand-wired array logic) circuits. The ZHAL option in the company's PALASM2 software can confirm whether a design specification will fit the ZHAL architecture. For a minimum of 5000 devices and a \$4000 nonrecurring engineering charge, unit prices are \$2.52 for ZHAL20A Series and \$4.25 for ZHAL24A Series. Production, eight to 10 weeks after design approval.

Monolithic Memories Inc, 2175 Mission College Blvd, Santa Clara, CA 95054. Phone (408) 970-9700. TWX 910-338-2376.

Circle No 395



QUAD TRACK/HOLD IC

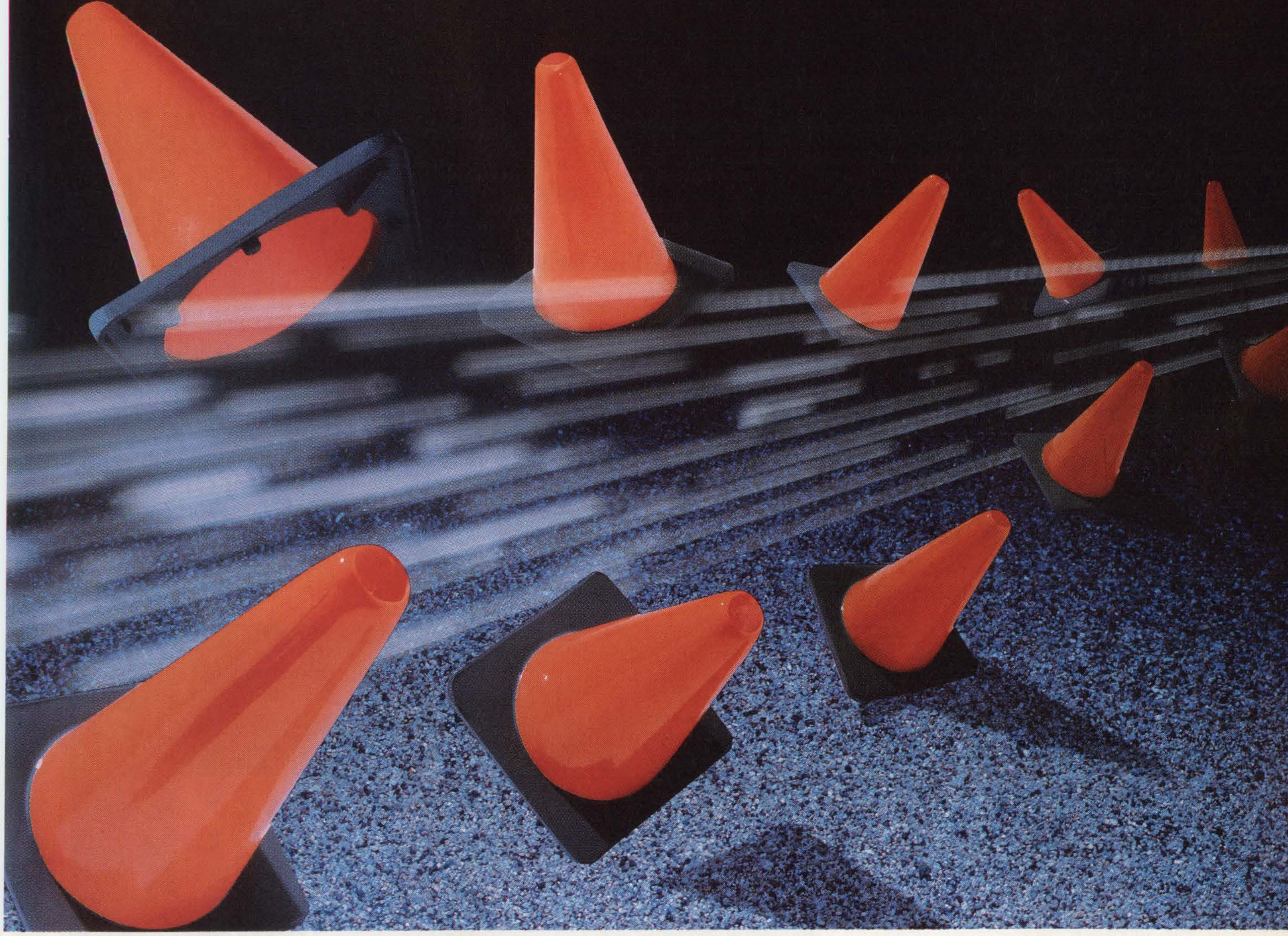
- *Has 12-bit accuracy*
- *Each track/hold amplifier includes a hold capacitor*

The Model CS31412 is a monolithic quad track/hold IC that offers 12-bit accuracy and a 1-μsec acquisition time. You can configure the input multiplexer to accept four single-ended signals or two differential signals. Each of the IC's four track/hold amplifiers includes a hold capacitor; the voltage droop is only 0.01 μV/μsec. The device also includes a RAM-based calibration scheme that reduces the total unadjusted error—including nonlinearity, gain error, and hold-pedestal error—to 700 μV max over time and temperature. The CS31412 comes in an 18-pin ceramic DIP, operates on ±5V supplies, and dissipates 250 mW. To simplify its evaluation, you can buy the CDB31412 demo board, including a socketed IC, for \$100. CS31412, from \$36 (100).

Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222.

Circle No 396

Introducing the Fastest Family of CMOS EPROMs on the Circuit



WSI EPROMs: Twice as fast as the Pack.

WSI's family of CMOS EPROMs keeps you in the fast lane with access times as low as 55 NS, leaving systems with wait states in the dust. That means you can now turbo charge your system. With EPROM architectures ranging from 8K x 8 to 16K x 16.

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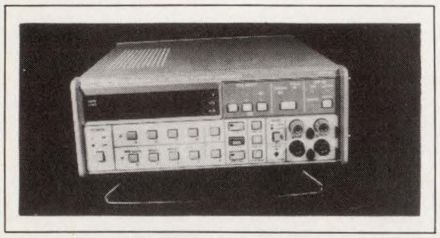
With this kind of speed and reliability, it makes sense to check out WSI's EPROMs and RPROMs.

So call us at **(800) 331-1030**, ext. 234, or in CA. **(800) 323-3939**, ext. 234. And we'll get you on the road to higher performance today.

Waferscale Integration, Inc.,
47280 Kato Road, Fremont,
CA 94538

Part No.	Speed	Type
WS57C191/291	40 ns.	2k x 8 CMOS RPROM
WS57C43	55 ns.	4k x 8 CMOS RPROM
WS57C49	55 ns.	8k x 8 CMOS RPROM
WS57C64F	55 ns.	8k X 8 CMOS EPROM
WS57C128F	70 ns.	16k x 8 CMOS EPROM
WS57C256F	70 ns.	32k x 8 CMOS EPROM
WS57C65	55 ns.	4k x 16 CMOS EPROM
WS57C257	70 ns.	16k x 16 CMOS EPROM

WaferScale
INTEGRATION, INC.



CALIBRATOR

- *Executes 160-step voltage-current program*
- *Sources 0 to ±12V at 0 to ±120 mA*

The 6142 programmable dc voltage-current generator can source 0 to ±11.999V at as much as ±119.99 mA in 0.1-μA steps. Its accuracy ratings are (±0.035%)+(±5 μV) and (±0.035%)+(±0.3 μA). The instrument has a 160-step nonvolatile program memory. The unit is completely programmable over the IEEE-488 bus. $3995.

PrimeLine, Box 670, San Fernando, CA 91341. Phone (800) 525-5554; in CA, (818) 764-5400. TLX 4943094.

Circle No 397

80386 EMULATOR

- *Runs at 16 MHz*
- *Lets you set breakpoints on task switches*

The Model ICE-386 emulator comes in an IBM PC/AT DOS-based version and a Xenix-based version. It contains a bond-out version of the 80386 μP that is not available on the open market. The emulator runs at clock speeds to 16 MHz. It has 128k bytes of emulation memory, which is mappable in 4k-byte increments. In addition to having the standard emulator breakpoints, the unit can break on task switches and illegal data accesses. It can store 2000 frames of program execution along with time tags. The company claims that its emulator's timing and electrical specs are exactly equivalent to those of the target μP. ICE-386, $15,000; Xenix-to-DOS field upgrade, $1100.

Intel Corp, Literature Dept W342, 3065 Bowers Ave, Santa Clara, CA 95051. Phone local office.

Circle No 398

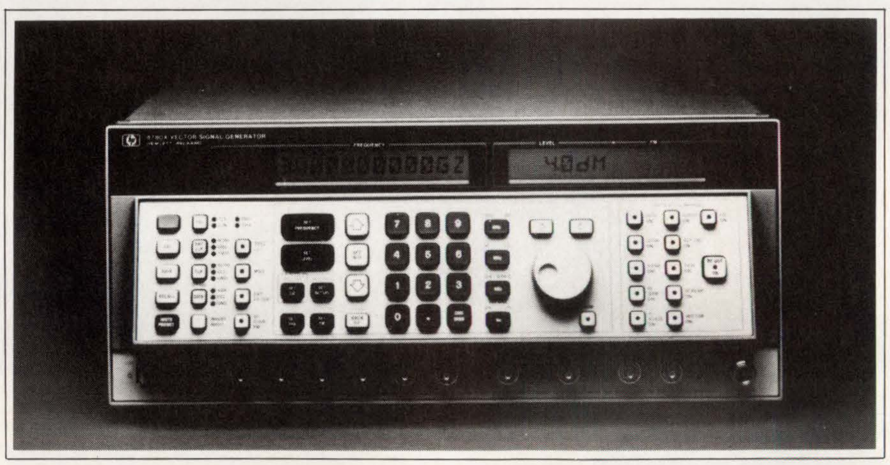
IEEE-488 EXTENDER

- *Extends possible length of cable by 18m*
- *Permits attachment of 14 extra devices*

The GPIB-120 IEEE-488 bus extender allows you to extend your total cable length from 20 to 38m. Furthermore, you can add 14 more devices to the bus. The extender has no switches for you to set; it detects the addresses of controllers, talkers, and listeners, and it configures itself. The unit operates transparently and requires no modifications to your software. $995.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737.

Circle No 399



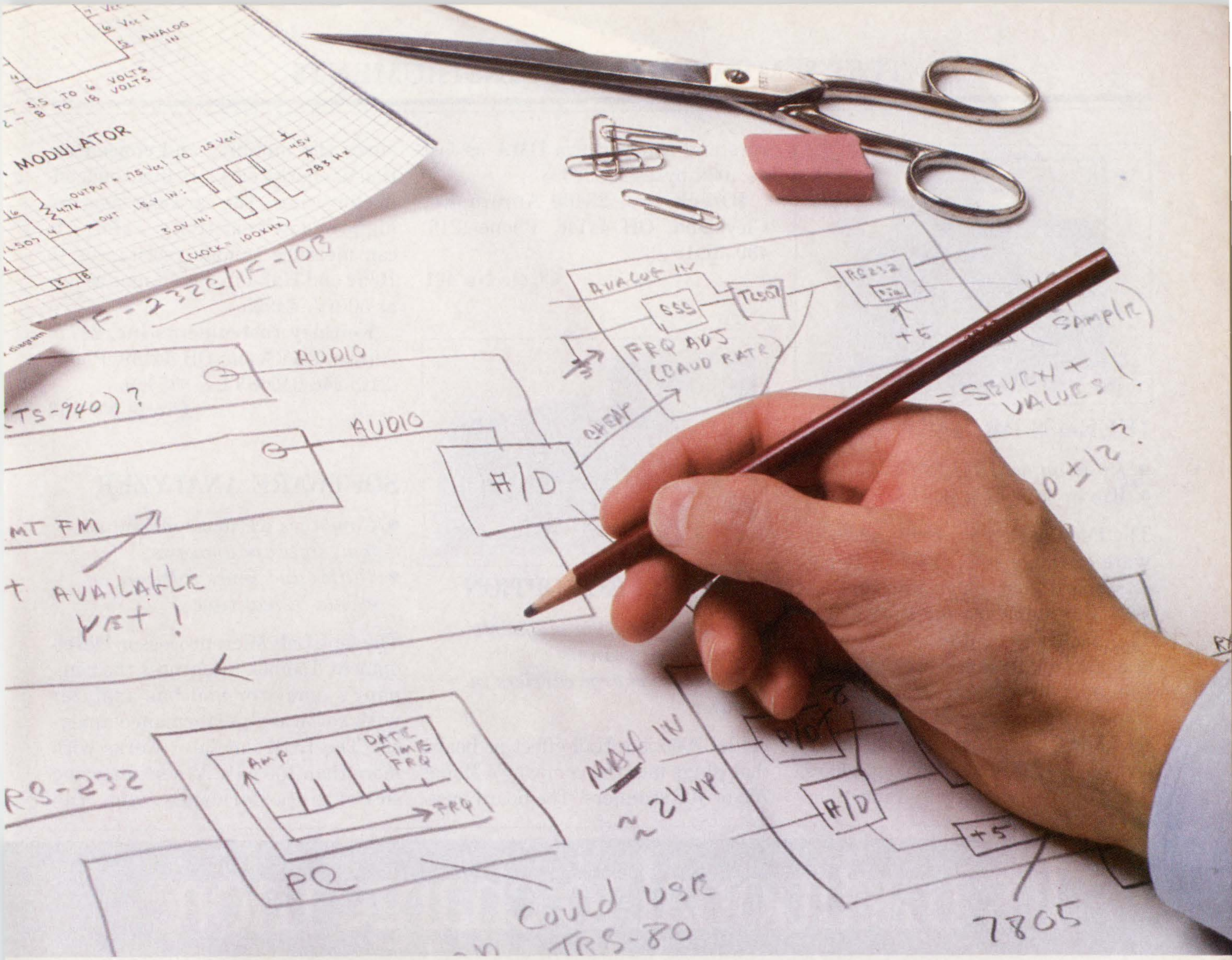
VECTOR GENERATOR

- *Uses both digital and analog modulation signals*
- *Processes in-phase and quadrature modulation inputs*

The Model HP 8780A vector signal generator accepts both digital bit streams and conventional analog signals as modulation inputs. Its clock rates range from dc to 150 MHz in clocked mode and from dc to 50 MHz in asynchronous mode. The instrument has a frequency range of 10 MHz to 3 GHz. The generator also processes in-phase and quadrature analog modulation signals ranging from dc to 350 MHz. In addition, you can amplitude-modulate the output with a scalar (nonvector), 500-kHz AM signal or a 50-MHz (p-p) FM signal. The generator's synthesized carrier has a resolution of 1 Hz. Its output spans +10 to −100 dBm. $55,000. Delivery, 12 weeks ARO.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 400



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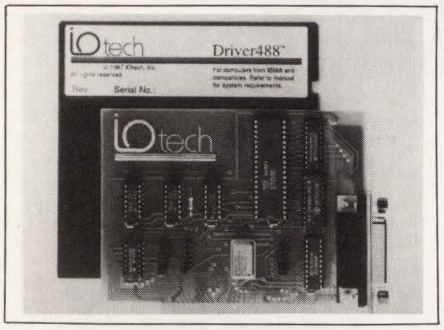


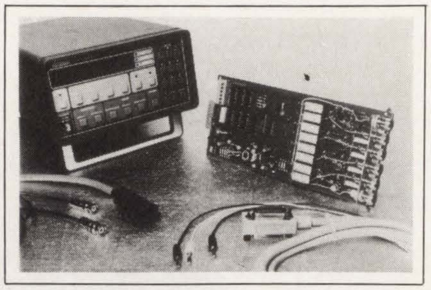
IEEE-488 PACKAGE

- *Runs on an IBM PC*
- *Works with high-level languages*

The Personal488 hardware and software package comprises an IEEE-488 board that plugs into an IBM PC, and software for that board. The package requires no language-specific device drivers or routines; the board's control software becomes part of the PC's DOS. The package's commands are similar to those of HP's Series 80 controllers. The board automatically reports errors and can perform DMA as fast as 400k bytes/sec. $395.

IOtech Inc, 23400 Aurora Rd, Cleveland, OH 44146. Phone (216) 439-4091.

Circle No 401



HALL-EFFECT OPTION

- *Hall-effect option plugs into company's scanner*
- *Measures charge carriers in wafer*

Model 7065 is a Hall-effect pc board that plugs into the company's Model 705 or 706 scanners. The board measures the mobility and concentration of charge carriers in a semiconductor wafer. The card can measure high- or low-resistivity wafers. It can measure sample resistances to $10^{12}\Omega$ and Hall-effect voltages as low as 50 nV. $4995.

Keithley Instruments Inc, 28775 Aurora Rd, Solon, OH 44139. Phone (216) 248-0400. TLX 985469.

Circle No 402

SOFTWARE ANALYZER

- *Combines μP development system, software analysis*
- *Tallies and times software events in real time*

The OptiLab Microprocessor Development Toolbox integrates the company's emulator and bus analyzer with software-performance analysis. The ROM emulator works with more than 150 μPs. When analyzing software performance, you can count and time-tag software events in real time at full speed. The software displays the results of the performance analysis on the screen of an IBM PC (you need a PC both to control the emulator and to run the software). The 32k-byte version costs $5980.

Orion Instruments Inc, 702 Marshall St, Redwood City, CA 94063. Phone (415) 361-8883. TLX 530942.

Circle No 403

SCSI ANALYZER

- *Records transactions in transitional-timing mode*
- *Options enable unit to emulate SCSI device*

The DSC-202 is a SCSI bus analyzer. It also offers the option of emulating a SCSI device. The analyzer requires a dumb terminal or an IBM PC for control. It stores as many as 8000 bus transactions in the transitional-timing mode. An optional time stamp provides 50-nsec timing resolution. In addition to 56 SCSI bus signals, the analyzer can record as many as eight additional inputs. The unit meets ANSI X3T9.2 specifications and can transfer data at rates as high as 1.5M bps. The unit has a 2k-byte EEPROM and 7k bytes of static RAM for setups and user programs. DSC-202, $4950; emulator and time-stamp option, $1900; if ordered together, $6500. Delivery, 60 days ARO.

D-Designs, Box 1141, Palo Alto, CA 94301. Phone (415) 327-1525.

Circle No 404

CURRENT SOURCES

- *Units provide 1 kW*
- *Have 50-μsec/V slew rate*

The C Series comprises three ac/dc current sources that supply 100A at 10V, 50A at 20V, or 20A at 50V. The 5¼-in., rack-mounted units require a 0 to 20V input stimulus. The units' slew rate is 50 μsec/V. Their input bandwidth is 10 kHz, and their basic output-current accuracy is 0.005%. The sources are IEEE-488 compatible. $4550. Delivery, stock to 60 days.

Shepherd Scientific Inc, 7918 Convoy Ct, San Diego, CA 92111. Phone (619) 268-9696.

Circle No 405

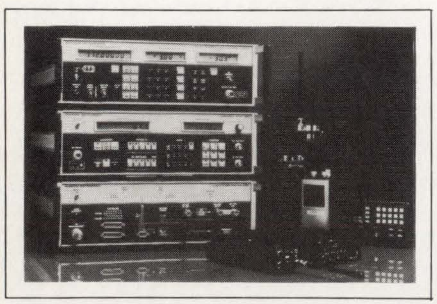
ANALYZER

- *Records line-to-line and line-to-neutral power disturbances*
- *Has built-in printer*

Model 646-3 is a 3-phase power-line-disturbance analyzer that reports voltage disturbances. It records voltage sags, voltage surges, impulses, and undervoltage and overvoltage conditions. It also recodes frequency variations. The unit monitors both line-to-line and line-to-neutral disturbances. Its built-in printer prints a record of each disturbance. The unit has a separate dc input. A temperature probe is optional. $3690.

Dranetz Technologies Inc, Box 4019, Edison, NJ 08818. Phone (201) 287-3680.

Circle No 406



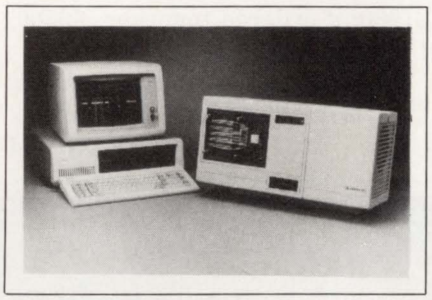
RADIO TESTERS

- *Check 2-way transceivers semiautomatically*
- *Controller software is written in Basic*

The MISATT semiautomatic test sets take routine measurements on AM or FM transceivers. The sets contain three IEEE-488 instruments: a 2019A or 2018A AM/FM signal generator, a 2305 automatic modulation meter, and a 2306 programmable interface unit. The software supplied with the sets is written in Basic, so you can expand or modify the test routines. The software runs on Hewlett-Packard controllers. The test routines include sensitivity, sinad ratio, power, frequency, and modulation tests. Adding a 2017 signal generator enables you to perform extended tests, such as adjacent-channel and image- and IF-rejection tests. Basic system (without controller), $25,000. Delivery, 60 to 90 days ARO.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401. Phone (800) 233-2955; in NJ, (201) 934-9050.

Circle No 407



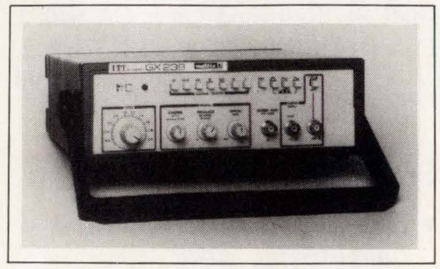
ASIC VERIFIER

- *Tester verifies 190-pin, 20-MHz ASICs*
- *Lets you program test patterns in 1-nsec increments*

The Logic Master ST is a modular benchtop tester for verifying ASICs. The unit can handle chips having as many as 190 pins. The unit can perform real-time pattern generation, data acquisition, and pattern matching at clock speeds as high as 20 MHz. You can program its pattern-generation channels' leading edges in 1-nsec increments in either NRZ or DNRZ formats. The pattern generator has branching, looping, and ASIC-initialization capabilities. The unit can use an IBM PC for control. You can download test patterns from common CAE systems and edit the patterns in real time on the PC. You wire replaceable front-panel cards to accommodate different devices. The 32-channel version is $16,800; a typical configuration for 100-pin devices costs around $40,000.

Integrated Measurement Systems Inc, 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117.

Circle No 408



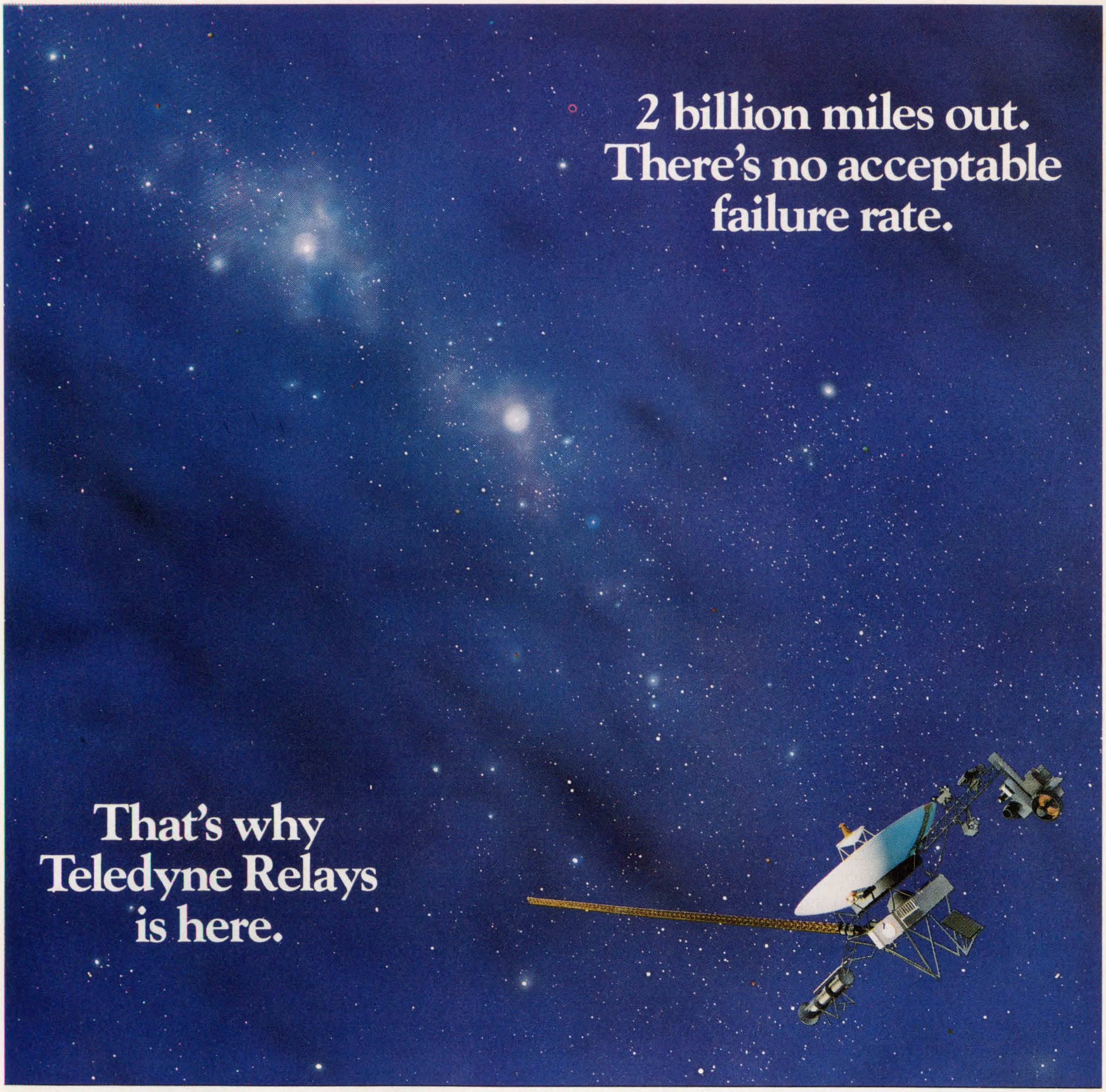
FUNCTION GENERATOR

- *Covers the frequency range of 0.2 Hz to 2 MHz*
- *Has external-sweep frequency control*

The GX239 function generator provides sine-, square-, and triangular-wave outputs, plus dc and pulsed TTL-level outputs. The instrument has seven decade-frequency ranges, which allow you to select output frequencies between 0.2 Hz and 2 MHz. Its frequency accuracy is ±5% of range, and its sine-wave distortion below 200 kHz is <1%. You can adjust the output waveform's duty cycle between 20 and 80%, and you can vary the output level into an open circuit from 0 to 20V p-p or from 0 to 10V p-p into a 50Ω load. A variable dc-offset facility allows you to offset the open-circuit output by more than ±10V, or by more than ±5V for a 50Ω load. You can also invert the square-wave or pulse outputs. External-sweep facilities permit you to vary the generator's frequency over a 1000:1 ratio from an external 0 to 10V source. The unit operates from 198 to 262V or 99 to 131V ac at 50 or 60 Hz. It measures 270×95×295 mm and weighs 1.8 kg. Fr fr 2500.

ITT Instruments, 346 Edinburgh Ave, Slough, Berkshire, SL1 4TU, UK. Phone 0753 824131.

Circle No 409



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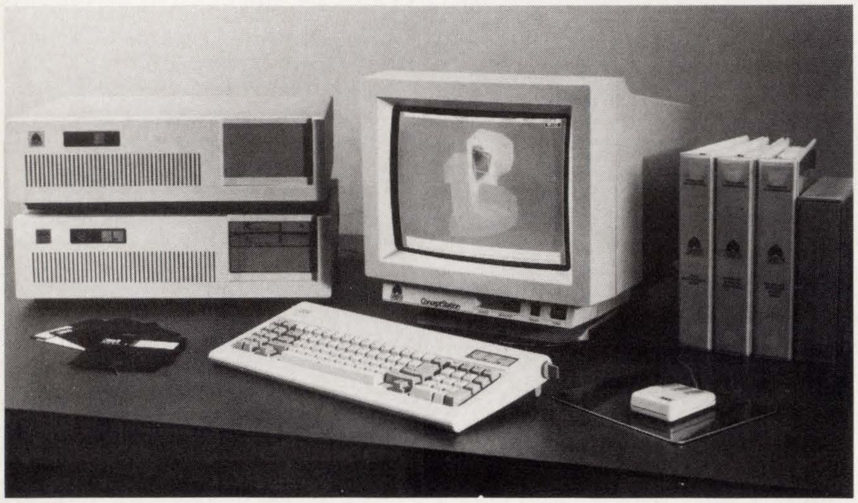
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS



CAE WORKSTATION

- *Uses IBM PC/AT and hardware applications accelerator*
- *Provides fast solid-modeling features*

The Conceptstation consists of an IBM PC/AT, enhanced by a proprietary 32-bit, 8M-flops accelerator coprocessor and graphics subsystem. You can run all MS-DOS software, such as productivity and software-development tools, on the PC/AT. The vendor's MCAE software, written in C, runs under the Xenix operating system and makes use of the accelerator coprocessor to achieve maximum analysis and display speed. The MCAE software includes a geometric modeler that can generate solid, surface, or wire-frame solid images; a finite-element modeler; a design-rule processor; a materials-property manager program; and a macro-design language. The workstation is available in two versions: The bundled version includes an IBM PC/AT; a 1.2M-byte floppy-disk drive; a 9.2M-byte RAM; a 60M-byte hard disk; an Intel 80287 math coprocessor; a 3-button optical mouse; a 256-color; 1024×770-pixel monitor; and the vendor's proprietary accelerator and graphics hardware, together with the MCAE software, Xenix, and MS-DOS. The unbundled version includes all of the proprietary items, but you have to provide your own PC/AT and 60M-byte hard disk. Bundled version, $49,000; unbundled version, $36,500.

Aries Technology Inc, 650 Suffolk St, Lowell, MA 01854. Phone (617) 453-5310.

Circle No 410

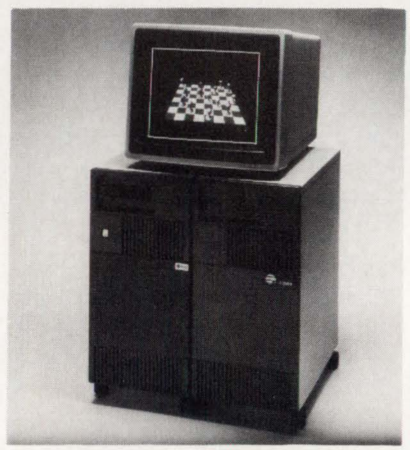
CAD GRAPHICS

- *Replaces PGA, EGA, and CGA boards in IBM PCs*
- *Provides resolution as high as 1024×768 pixels*

The Uni-Screen/PGA is a 2-board graphics set that plugs into one slot of an IBM PC, PC/XT, PC/AT, RT PC, or compatible computer. According to the manufacturer, the board is completely compatible with the IBM Professional Graphics Adapter, but the Uni-Screen/PGA runs PGA-compatible applications software four times faster than does the PGA. It offers resolution as high as 1024×768 pixels, and it can display 16 colors simultaneously from a palette of 4096. (The PGA's resolution is 640×480 pixels, and it can display 256 colors simultaneously.) The board set contains an 80186 μP, two I/O ports, as much as 512k bytes of RAM, and 128k bytes of ROM in which the firmware is resident. The board can drive most 36- and 48-kHz color monitors. According to the vendor, the board can run any PGA-compatible application, as well as applications that use the VDI, CGI, GKS, or DGIS graphics standards. With 800×600-pixel resolution, $2695; with 1024×768-pixel resolution, $2995.

TAT Graphics Group Inc, 1270 Lawrence Station Rd, Building E, Sunnyvale, CA 94089. Phone (408) 734-2202.

Circle No 411



GRAPHICS SUBSYSTEM

- *Provides 1280×1024-pixel resolution*
- *As many as 28 bit-planes of image memory*

The Satellite is a high-resolution color-graphics display subsystem for use with Sun Microsystems (Mountain View, CA) workstations. It's available in several configurations. All units in the line feature a resolution of 1280×1024 pixels and a palette of 16 million colors; the frame buffer can have as many as 28 bit-planes of image memory per pixel. Features include one to four

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independent color-display channels, programmable video-display formats, and a user-programmable, writable control store. The design of the frame buffer allows you to update it during display operations, and double buffering facilitates hidden-redraw operations. You can select from a variety of interlaced and noninterlaced display formats, including NTSC, CCIR, and the new HDTV television formats, or you can create your own custom format. The unit provides both 4-bit and 8-bit color-lookup tables, as well as 12- and 24-bit RGB modes of operation. The system comes with two libraries of graphics functions: The Basic Graphics Library (BGL) provides the basic machine-control functions and 2-D graphics functions defined in device coordinates; the High-Level Graphics Library (HGL) provides hierarchical display lists with 3-D functions in a world-coordinate space. The subsystem's image-processing capabilities include integer zoom factors from 1 to 16; separate pan and zoom control for each group of four bit-planes of image memory; and pixel-block transfers. The monitor screen can be 16 in. or 19 in.; both types have a scan rate of 65 kHz and a bandwidth of 110 MHz. From $15,000 to $30,000. Delivery, 30 to 45 days ARO.

Jupiter Systems, 1100 Marina Village Parkway, Alameda, CA 94501. Phone (415) 523-9000. TLX 6713004.

Circle No 412

MULTITASKING FOR PC

- *Multitasking kernel supplements PC-DOS*
- *Controls access to shared data areas*

PCMascot is a multitasking kernel for the IBM PC and compatibles. It allows you to develop real-time applications that use concurrently executing processes for process control or data acquisition. You can divide your application into processes that communicate with each other through a shared data area in memory. The package provides kernel primitives that control access to shared data areas and that can synchronize the execution of different processes. The kernel manages all interrupt-handling functions to simplify the writing of device drivers; however, in time-critical processes, you can include interrupt handling in the process. You implement tasks (processes) as sequential C programs that you compile and link in the usual manner. Because each task is a separate .EXE program, you can combine tasks that use different memory models or that were compiled with different compilers. $795.

Andyne Computing Ltd, 544 Princess St, Suite 202, Kingston, Ontario, Canada K7L 1C7. Phone (613) 548-4355.

Circle No 413

PC-BOARD DESIGN

- *Enhanced hardware speeds design, simulation, and routing*
- *Delivers more performance for less money*

Enhancement options for the Apollo DN3000 workstations now allow it to run this company's PCB Worksystem CAE software. These enhancements include an increase in main memory to 4M bytes and in disk storage to 155M bytes. The PCB Worksystem offers schematic capture, board layout, and, in conjunction with the Tektronix HILO-3 Logic Simulation System, simulation of large logic systems. The software offers both automatic and interactive placement of parts, either on the whole board or on specific areas. You can use a variety of routing strategies, singly or in combination, when making multiple passes to optimize board layout. A complete workstation, consisting of the Apollo DN3000, 4M bytes of memory, 155M bytes of disk storage, a keyboard, a mouse, dual operating systems (Unix 4.2BSD and Apollo Aegis), and Tektronix pc-board design and layout software configured for the DN3000, $49,900.

Tektronix Inc, CAE Systems Div, 5302 Betsy Ross Dr, Santa Clara, CA 95054. Phone (800) 547-1512; in OR, (800) 542-1877; in CA (408) 727-1234.

Circle No 414

MICROCODE TOOL

- *Microcode assembler runs on a variety of computers*
- *Facilities include pipeline macros and looping constructs*

Version 1.10 of the Hale Macro-Meta-Assembler for microcode includes substantial enhancements. The pipeline macros let you assign any microcode field; you can string together existing source macros to create microcode or to create a higher-level macro. You can operate as many as eight pipeline macros simultaneously. The software lets you define errors, so you can assert microprogram design rules; the assembler checks your code against these rules and warns you of any violations. You can insert nonassembling messages at any point in the source code to trace assembly-program flow or to indicate untested routines. The While and Endwhile looping directives allow the assembler to generate code from statements placed between these directives as long as a user-specified condition remains true. An ASCII code-conversion feature lets you

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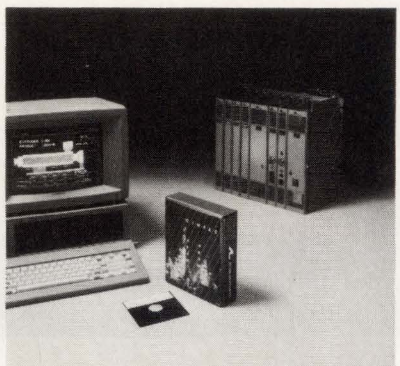
CIRCLE NO 168

code data in ASCII format. When you invoke the feature, it converts the data to binary form for embedding within the microcode. Thus, when you want to use the same message in different parts of your system, you need only enter it once in ASCII format and then invoke the converter at each occurrence of the message. Relocatable version for the IBM PC, $2300; relocatable versions for VAX, Sun, and Apollo computers, $3500.

Hilevel Technology Inc, 18902 Bardeen, Irvine, CA 92715. Phone (714) 752-5215.

Circle No 415



PROCESS CONTROL

- *Provides both analog and digital I/O*
- *Provides log of control and alarm events*

CIM-PAC is a process-measurement and -control software package that runs on IBM PC, PC/XT, PC/AT, and compatibles. To run the software, you need a math coprocessor, 640k bytes of RAM, an IBM Enhanced Graphics Adapter or equivalent graphics board, a hard disk, and appropriate analog or digital I/O boards. The display module lets you display the status of selected groups of I/O nodes (or of all nodes) in tabular form. Alternatively, you can create pictorial representations of the nodes and animate these by means of color changes and movement to indicate their current status. The event-processor module can automatically initiate tasks in response to monitored times, events, or instructions entered via the keyboard. You can define as many as 100 control loops for the system and independently select the update rate for each loop; you can vary the update interval from once per second to once every 255 seconds. The program provides several password levels to protect the database from unauthorized alterations. The software allows you to use as many as eight PCs in a network; the primary station requires a hard disk, but the secondary stations can be diskless units. $950.

Action Instruments Inc, 8601 Aero Dr, San Diego, CA 92123. Phone (619) 279-5726.

Circle No 416

COMMUNICATIONS

- *Links mini- and microcomputers to IBM mainframes*
- *Provides file transfers between disparate operating systems*

Blast-Host runs under IBM's VM/CMS and MVS/TSO operating systems and uses any of the asynchronous pathways typically found in the mainframe environment to provide file-transfer facilities between the mainframe and a minicomputer or a microcomputer such as an Apple Macintosh or an IBM PC or compatible. According to the vendor, the proprietary transmission protocol provides high-speed, error-free communication over such diverse media as X.25 packet-switched networks, satellite links, and noisy telephone lines. With the addition of a protocol converter, the program can emulate a 3270 terminal. Blast-Host for IBM mainframes, $5500; Blast for minicomputers, $495 to $1295; Blast for IBM PC or Macintosh, $250.

Communications Research Group, 5615 Corporate Blvd, Baton Rouge, LA 70808. Phone (504) 923-0888. TLX 759985.

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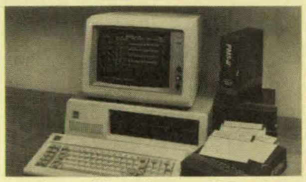

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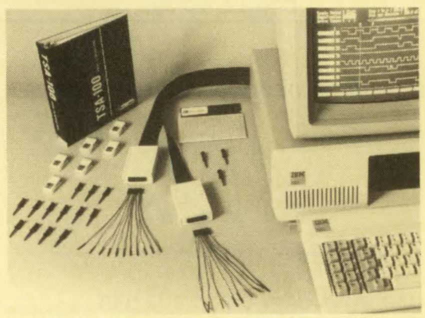

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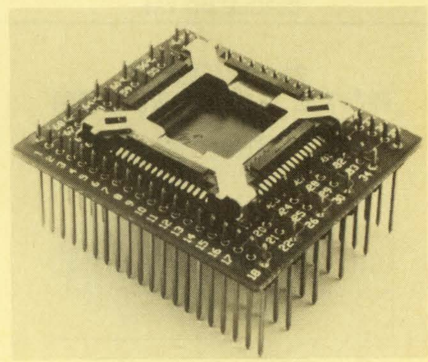

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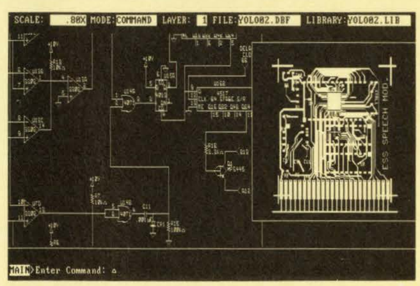

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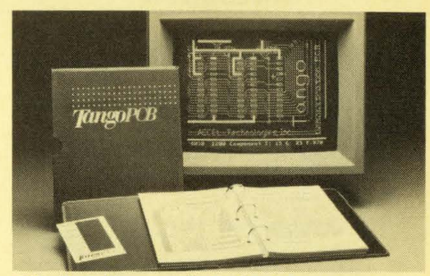

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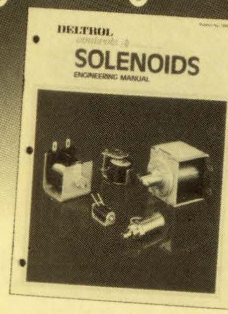

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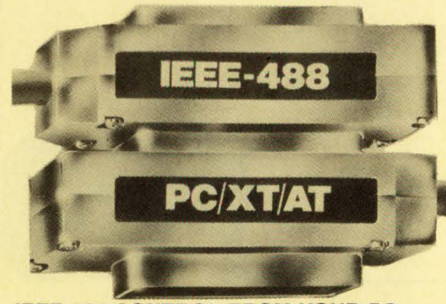

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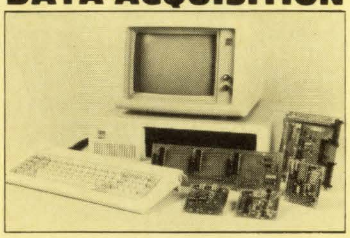

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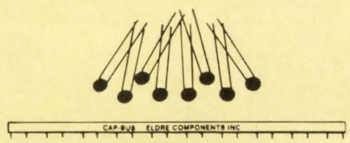

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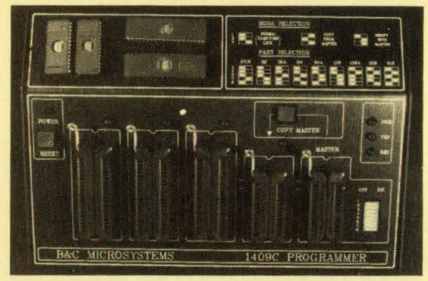

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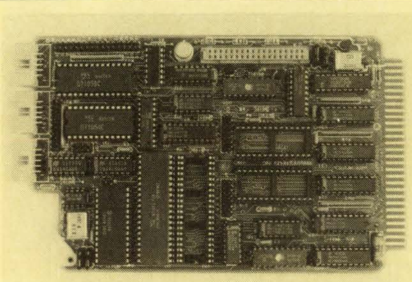

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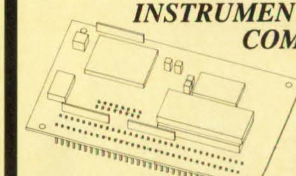

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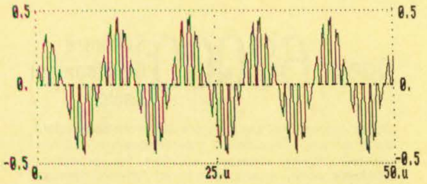

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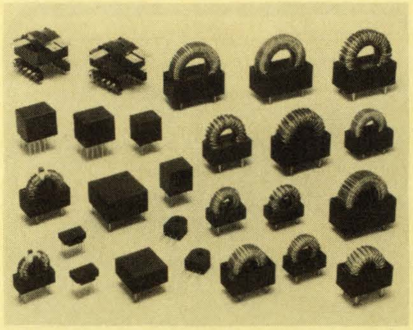

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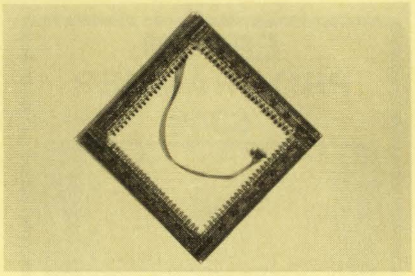

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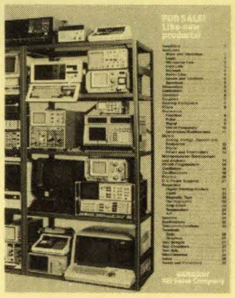

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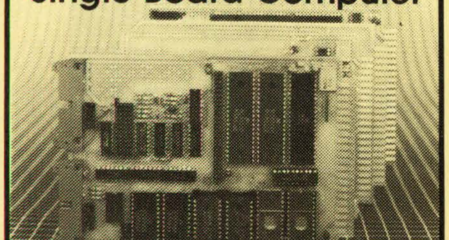

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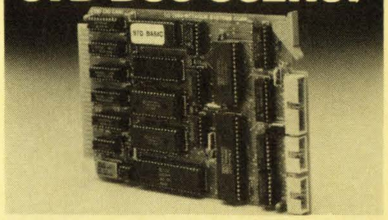

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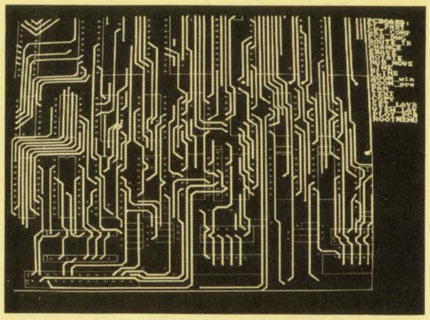

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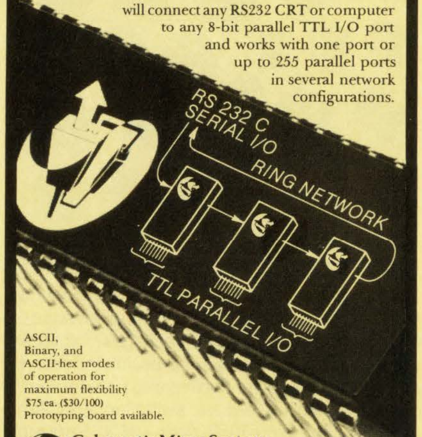

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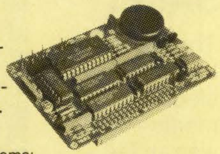

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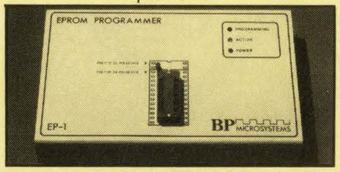

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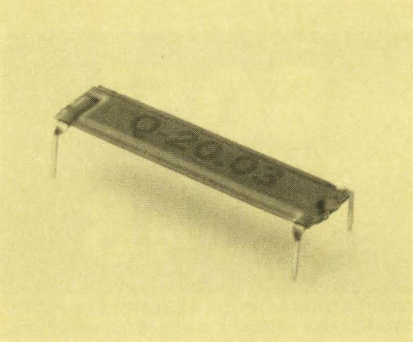

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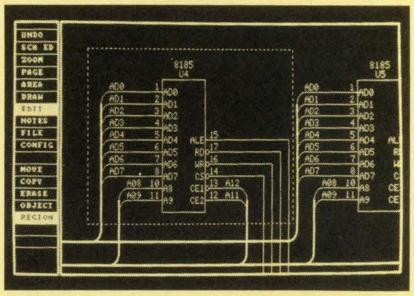

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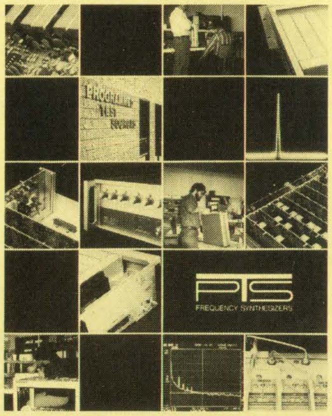

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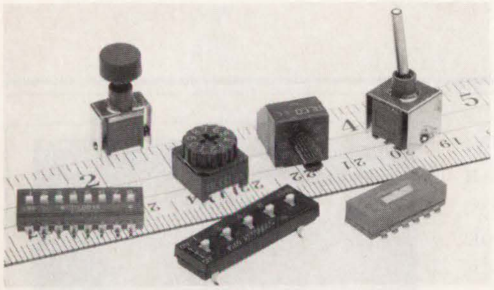

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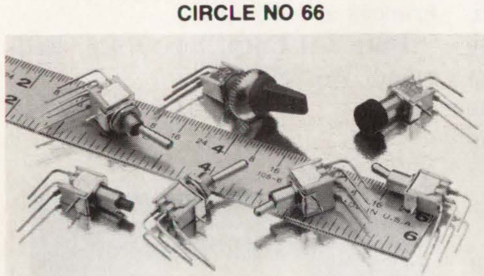

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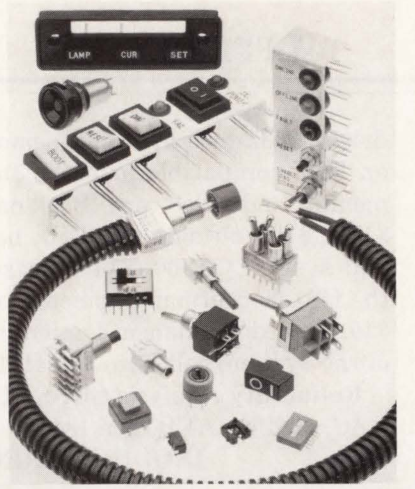

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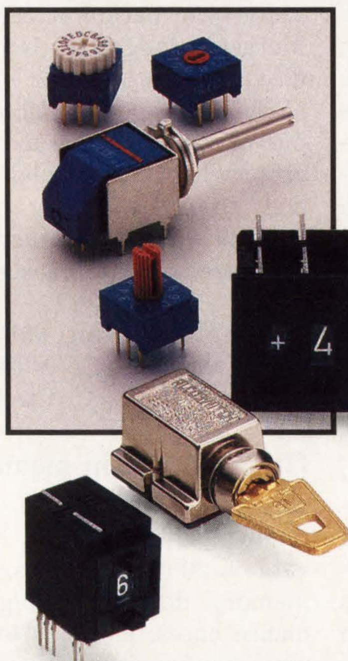

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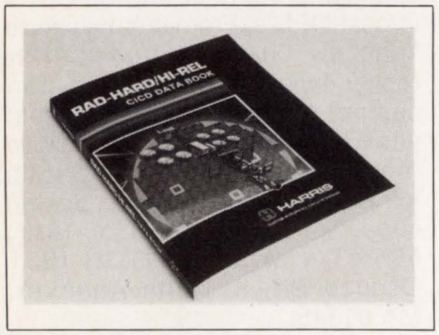

Data book details rad-hardened products

This book provides technical specifications on the company's rad-hardened products. Containing 496 pages, it features data sheets of such products as CMOS 16k-byte static RAMs, 80C85 and 80C86 microprocessors and peripherals, operational amplifiers, analog switches, comparators, multipliers, and data-communications interface devices. In addition, a section covers the manufacturer's CMOS/analog/digital standard-cell library, which includes 32 individual cells. The data book features other sections pertaining to microwave gallium arsenide products, secure-communication ICs, the effects of radiation on CMOS, and die sales and ordering information.

Harris Corp, Semiconductor Sector, Box 883, Melbourne, FL 32901.

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Report on reliability

If your target system is subject to extensive storage periods and relatively short operating times, you may find this data book and software system useful. According to the book, the disparity between these two time periods will cause most failures to occur during the nonoperating period. The book, *NONOP-1, Nonoperating Reliability Data-1986*, and the system, RAC-NRPS (nonoperating reliability prediction software), help in predicting the impact of nonoperating periods on system reliability. To use the software, you need an IBM PC, PC/XT, or PC/AT; one 10M-byte hard-disk drive or two floppy-disk drives; 348k-byte available memory; an IBM-compatible printer; and a monitor and video card. Book only, \$150 (\$160 outside the US); book and system, \$1400 (\$1450 outside the US). For airmail shipments, add \$15. To order a demonstration disk of the system, call (315) 330-4151.

Reliability Analysis Ctr, RADC/RAC, Griffiss AFB, NY 13441.

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Document discusses progamming, languages

This 39-pg document addresses the complexities of microprogramming and alternative microprogramming languages. In addition to examining the problems specific to microprogramming and offering traditional and unconventional ways to solve these problems, the publication provides information on the vendor's Metastep language. It includes a discussion of the major components of the language and detailed examples of representative and actual microprograms. Examples illustrate how to embed design-rule constraints within the structure of the language and within macro instructions.

Step Engineering, 661 E Arques Ave, Sunnyvale, CA 94086.

Circle No 420

Guide to add-in memory

This 80-pg booklet is a designer's guide to add-in memory. It contains data on 20 system buses, details of memory design for high-performance buses, elements to consider when configuring a system and selecting memory products, analyses of economic factors, and an industry overview. The final chapter of the guide describes the manufacturer's line of DEC-compatible memories and memories for high-performance microcomputers. A table of specifications completes the treatment.

Clearpoint Inc, 99 South St, Hopkinton, MA 01748.

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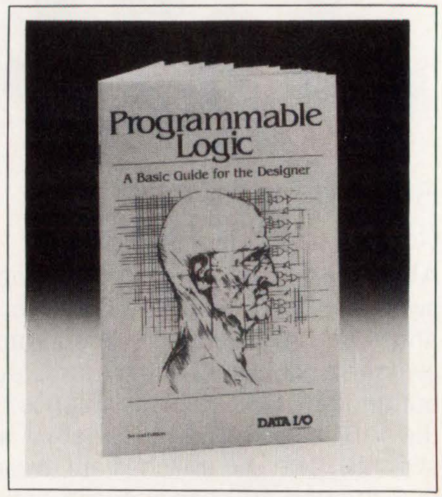

Booklet delves into programmable logic

This 30-pg booklet examines the topic of programmable logic. Sample chapters ask (and answer) such questions as "What is a programmable logic device?" and "Why was programmable logic developed?" The pamphlet also describes the different types of programmable logic devices, how to use the logic, and a design example. A glossary and references are included.

Data I/O Corp, Box 97046, Redmond, WA 98073.

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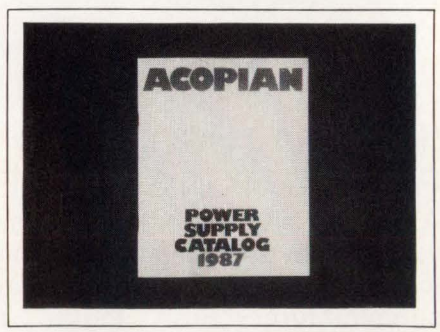

All about power supplies

This 1987 catalog of the manufacturer's power supplies, which are available with outputs of 1 to 200V (2A), lists standard features, options, prices, and ordering information. The 56-pg catalog contains photos and outline drawings, and it illustrates typical applications.

Acopian, Box 638, Easton, PA 18044.

Circle No 423

Tutorial helps to learn C

The C Trainer consists of a textbook and an interpreter. The book contains chapters on expressions, declarations, initializations, arrays and pointers, and macros. The interpreter runs on various systems and provides fine control of the execution and debugging of a C program or fragment. You may stop a program at any point, and you can inspect and change the values of active variables. Program modifications are effective immediately with no need to wait for compiling, assembling, and link editing. Also, you can trace function calls, statements, and expressions separately or together. The interpreter's programs range from introductory to advanced. For Macintosh, IBM PCs, PC/XTs, and PC/ATs, the interpreter costs $99. For other systems, the price is higher. The book costs $22.95. Shipping and handling is $5 extra.

Catalytix Corp, 55 Wheeler St, Cambridge, MA 02138.

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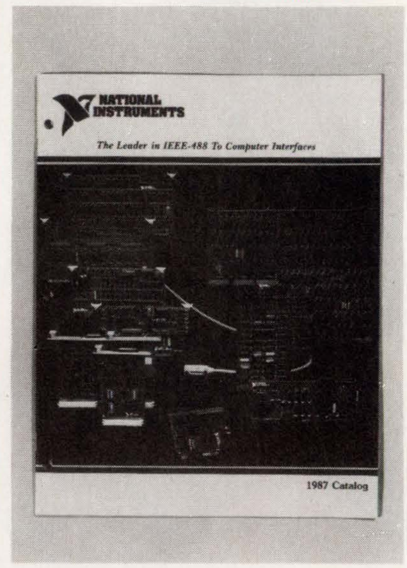

IEEE-488 bus interface products cataloged

This 1987 catalog covers the vendor's IEEE-488 bus interface products, which are available for IBM PCs, PC/XTs, PC/ATs, RT PCs, and compatibles; for Apple, AT&T, Tandy, Texas Instruments, Apollo, Sun, Compaq, Motorola, and NCR machines; and for the Q Bus, Unibus, VME Bus, Multibus, S-100 Bus, STD Bus, and SBX Bus. The 24-pg document includes the manufacturer's newest offerings, such as a family of intelligent interfaces that support AT&T 3B2 computers and TI Explorer workstations. In addition, it contains information about bus extenders, converters, and testers, as well as data on training for the IEEE-488 bus.

National Instruments, 12109 Technology Blvd, Austin, TX 78727.

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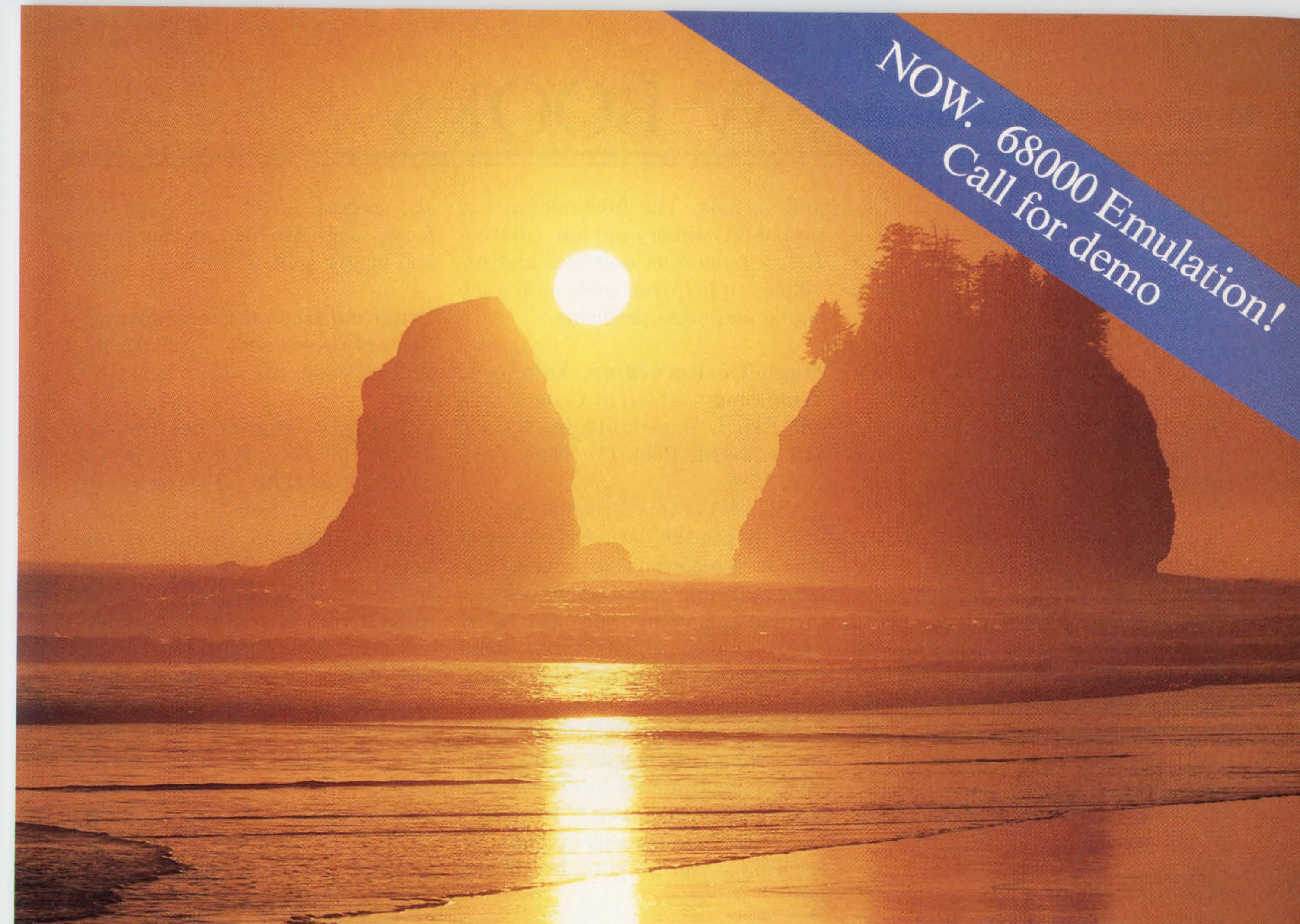

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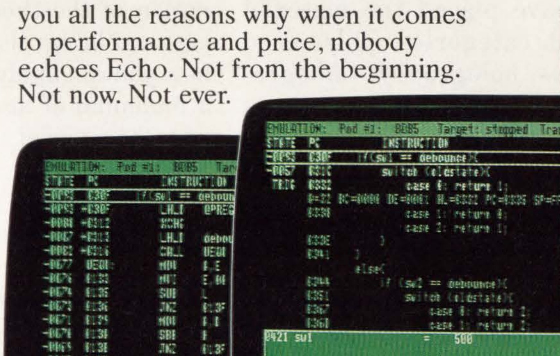

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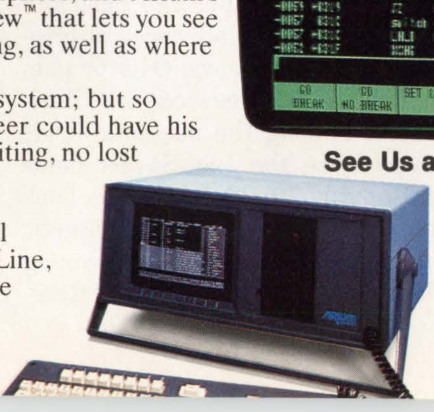

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NEW BOOKS

Electromagnetic Compatibility Handbook, by J L Norman Violette, Donald R J White, and Michael F Violette. 707 pgs; $68.95; Van Nostrand Reinhold, New York, NY, 1986.

This handbook approaches in a practical way the problems involved in achieving electromagnetic compatibility in electrical or electronic systems. It considers the fundamental electromagnetic concepts, explains the causes and effects of electromagnetic interference, and discusses current EMI problem-solving techniques. The work offers solutions to the problems of how to identify EMI sources, quantify resultant ambient electromagnetic fields when possible, identify EMI receptors and quantitatively determine their susceptibility, and develop the most cost-effective ways to eliminate EMI.

Modern Acoustical Imaging, edited by Hua Lee and Glen Wade. 433 pgs; $51.95; IEEE Press, New York, NY, 1986.

Divided into eight sections, this book reviews the various developments in acoustical imaging. The editors have placed the material into eight categories: pulse-echo techniques, holography, tomography, microscopy, imaging systems in general, seismic exploration, signal analysis and processing, and image understanding. The 35 reprinted papers describe how sound can produce images of objects that can't be obtained using light, x-rays, or other types of radiation.

Probability, Signals, Noise, by Jacques Dupraz. 344 pgs; $39.95; McGraw-Hill Book Co, New York, NY, 1986.

With an emphasis on practical applications, this work provides a comprehensive treatment of signal theory and probability. Written for use as a textbook, it takes you from the standard concept of a random variable to the ideas of random vectors and signals. The fundamentals of probability theory are also covered. It has numerous exercises and examples to help you solve on-the-job signal and noise problems.

Magnetic Recording, Volume I: Technology, edited by C Denis Mee and Eric D Daniel. 514 pgs; $34.50; McGraw-Hill Book Co, New York, NY, 1986.

Volume I of this 2-volume set covers in depth the basic technology of magnetic recording. It provides material on longitudinal versus perpendicular recording, physical tolerance, noise constraints, head geometries and materials, reproduction techniques, linear and nonlinear recording, storage formats, substrates, particulate media, film media, head-media interface, and more. Volume II, which will cover the varied applications of magnetic recording, will be published in the fall.

The Theory of Fourier Series and Integrals, by P L Walker. 192 pgs; $29.95, John Wiley & Sons Inc, New York, NY, 1986.

After presenting a concise explanation of the theory of Fourier series and integrals, this books shows how you can apply that theory, with a minimum of mathematical knowledge, to a variety of areas of science and engineering. Included are examples, exercises, a bibliography, and a guide to further reading.

Handbook of Magnetic Phenomena, by Harry E Burke. 423 pgs; $49.50; Van Nostrand Reinhold, New York, NY, 1986.

This book applies the basics of Ampere's Law to advanced electromagnetic-field theory. Over 60 phenomena are discussed and illustrated. Among the magnetic fields covered are the Biot-Savart fields and torroidal fields. Also, the book fully classifies the galvanomagnetic effects. The author covers spinning electric charges, magnetic hysteresis, thermal effects, mechanical effects, magnetic-field measurement, and magnetic resonance.

Practical Digital Electronics, by Pierre Pelloso. 219 pgs; $29.95; John Wiley & Sons Inc, New York, NY, 1986.

To explain digital electronics in depth, this book begins each of its six chapters with a theoretical discussion and follows that with some practical problems and their solutions. The book focuses the design and realization of digital circuits and subsystems using small-, medium-, and large-scale integrated circuits. The author places emphasis on the avoidance of timing problems by the correct use of signals; interconnections and associated noise margins are investigated in detail. All the devices discussed are well known and readily available.

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GP1006B	GP1006B04B	256X64	200	9.84X3.35X1.77
GP1009B	GP1009B03B	240X64	200	6.2X2.76X1.57
GP1010B	GP1010B01B	176X16	200	7.32X2.16X1.70
GP1002C	GP1002C02B	320X240	100*	7.10X6.30X1.60

*Different Versions Available

DOT MATRIX DISPLAYS/MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
20SD01Z	M20SD01CA	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42CA	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02CA	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42CA	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03CA	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04CA	40X2	5X7	0.200	10.43X2.56X.90
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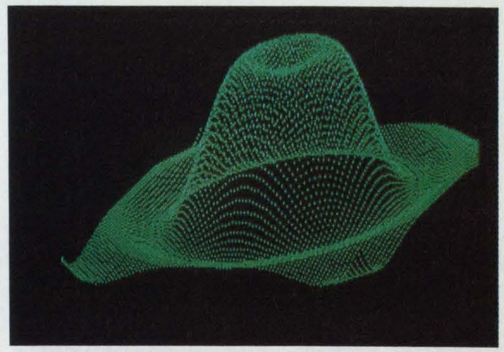

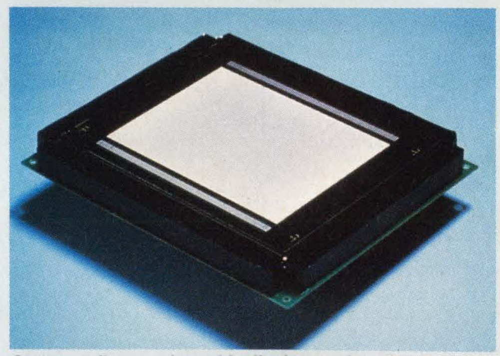

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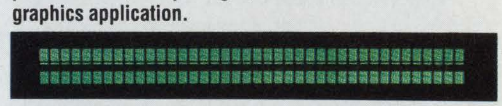

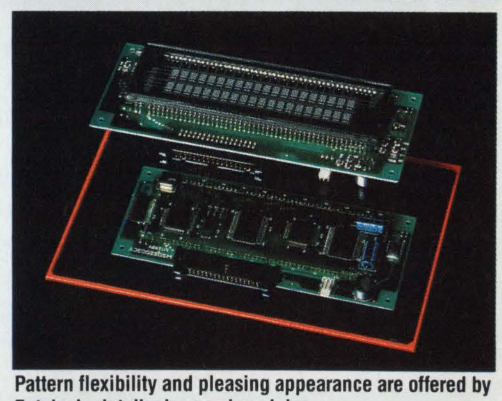

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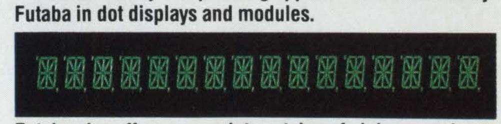

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Putting *Creativity* to work

Deborah Asbrand, *Associate Editor*

Author Betty Edwards is surprised that, although the subject of creativity is not a frequent topic of conversation, it's one of genuine importance to most people. "The question 'Am I creative?' is a burning one for many people," says Edwards, the author of *Drawing on the Right Side of the Brain* and *Drawing on the Artist Within.* "If I ask people if they want to be creative, the answer is overwhelmingly 'yes.' If I ask why, the answer is that being creative gives meaning to one's life."

> In the electronics sector, which prides itself as a bastion of innovation, the idea of using outsiders to assist in creative ventures has proved hard to sell.

Despite the high level of importance that people assign to creativity, however, many quickly dismiss their own potential for innovation, whether it's in the fine arts or in new-product design.

In fact, many people are scared away from even considering their creative potential because they believe some of the myths that have grown up around the creative process—for instance, that creativity is the exclusive province of people who are larger than life, that the mental pathways to creativity are neat and orderly, or that new products spring whole and finished from the creative mind. Other myths about the creative process have gone so far as to elevate it to the divine level.

A skill, not a gift

Yet many observers are now pointing out that the creative process isn't nearly as mysterious as it was once considered. Not only is creativity more of a skill than an innate gift, they say, but it's also a skill that most people can acquire. That idea has caught the interest of American business and has led to a rise in programs designed to stimulate latent creative potential, and, ultimately, spawn new and innovative products.

Moshe Rubenstein, professor of engineering and applied science at the University of California in Los Angeles and a speaker on the topic of creativity, scoffs at the veil of mystique that typically surrounds the creative process. Ideas, he says, are "nothing more than untested hypotheses." And the generation of ideas, particularly the creative problem solving in which engineers frequently engage, is often erratic. "The creative process in problem solving begins with chaos and then gives way to order," Rubenstein says. "Most ideas don't pan out at first. They need modification."

Rubenstein also discounts the theory that the best ideas are generated by individuals who are well versed in a particular subject. It's unnecessary to review large amounts of data on a problem before starting to hammer out ideas for solutions, he says, and companies with a penchant for doing so are actually restricting their employees' capacity for innovative thinking. Instead of letting their employees' imaginations fly based on a limited amount of information, the companies, by introducing voluminous reports and data, outline the parameters within which the employees' ideas must fall. "Ideas are generated based on fragments of information," Rubenstein says. "Sometimes too much information stifles the potential of surfacing ideas."

The freshest and least inhibited viewpoint probably produces the most novel solutions, Rubenstein says. At the conference "Fostering Creativity and Innovation," sponsored last December by the National Technological University, he demonstrated for the audience how restrictions in problem solving inhibit the generation of innovative ideas. Holding up a white page bearing a black inkblot, Rubenstein asked the audience to identify what they saw in the inkblot—their answers, though, he instructed, had to be three-letter words beginning with the letter "m."

"I'm putting a straitjacket on your creative thinking," Rubenstein explained. "Innovation begins with how you look at things. So not putting restraints on how you look at things is critical to creativity."

Research in creativity

The idea that creativity might be a skill anyone can learn rather than an innate gift has led to a surge of interest in learning more about the creative process. Although some individuals attribute their ideas or artistic expressions to divine inspiration, researchers say that most creative people simply exert greater control over their thought processes. As a result, they're able to direct their thoughts down innovative, imaginative paths.

Most information about creativity's organic origins is based on the groundbreaking research in the 1950s that found that each of the brain's hemispheres controls specific neural functions. The left hemisphere was discovered to control humans' logical and analytical thinking as well as their capacity for language; the right hemisphere controls visual and perceptual responses.

Thirty years later, scientific opinion on the brain's role in creativity falls into two camps: One group adheres to the conclusion that such functions as logic, analysis, and language reside in the left side of the brain and that visual and perceptual skills reside in the right side. The other group agrees that specific sections of the brain control specific neural functions, but believes that the brain is too complex an organ to divide its functions neatly by hemisphere.

What's clear is that creativity requires access to all of the brain's functions. Making the necessary neural transitions can be harder for some people than for others. Engineers, for example, depend largely on their talents for analysis and logical problem solving. They may be out of practice when it comes to tapping the abilities that lie in the portion of the brain that controls more artistic, less logical thinking. "Professionals need to think in a routine way 80 to 90% of the time," says Mark Sebell, a principal at Synectics, a Cambridge, MA, company that specializes in creativity and its management. "The glitch occurs when people try to use routine skills in an exploratory situation."

Synectics is one of a growing number of companies that work with corporations and their employees to improve their ability to open the stopper on imaginative thinking. The goal is to produce ideas for new ways of doing everything from designing new products to reorganizing the corporation.

Although client companies' first thoughts are usually to send their product manager, marketing manager, and marketing researchers to the sessions, Sebell says that Synectics has found the most productive groups to be ones whose members work at a variety of jobs. "You need to bring together a rich, diverse group of people who are going to look at problems in a new way." Often secretaries, sales people, accountants, and operations managers are included in the sessions.

> "Professionals need to think in a routine way 80 to 90% of the time. The glitch occurs when people try to use routine skills in an exploratory situation."

Program participants take mental "excursions," as Synectics calls them, in seemingly irrelevant directions that help those assembled make new associations. The interactions that occur among the group members are an important component of Synectics' version of the creative process. "One of the myths of creativity is that it's an individual thing," says Tom Crowe, the company's director of West Coast marketing. "But it comes out of group interaction." Once individuals become adept at connecting ideas and working together, they control their own creativity, Synectics' staff reasons.

Learning to "see"

Engineering students at California State University in Long Beach are learning a different kind of creative control from author Betty Edwards, who is a professor of art at the college. Edwards strongly supports the theory that tapping one's creative potential—whether it's in problem solving or in the fine arts—requires a shift of thinking from the left side of the brain to the right.

> "Ideas are generated based on fragments of information. Sometimes too much information stifles the potential of surfacing ideas."

In her drawing classes, Edwards teaches her students "how to control their own brain and develop perceptual skills through drawing." The class is more a lesson in "seeing" than in drawing, she says. To prove her point, Edwards shows drawings rendered by students before and after taking her class. Even those students whose preinstruction drawings were primitive and childlike improved after several weeks of instruction to the point where their drawings appeared to have been done by an artist of some skill.

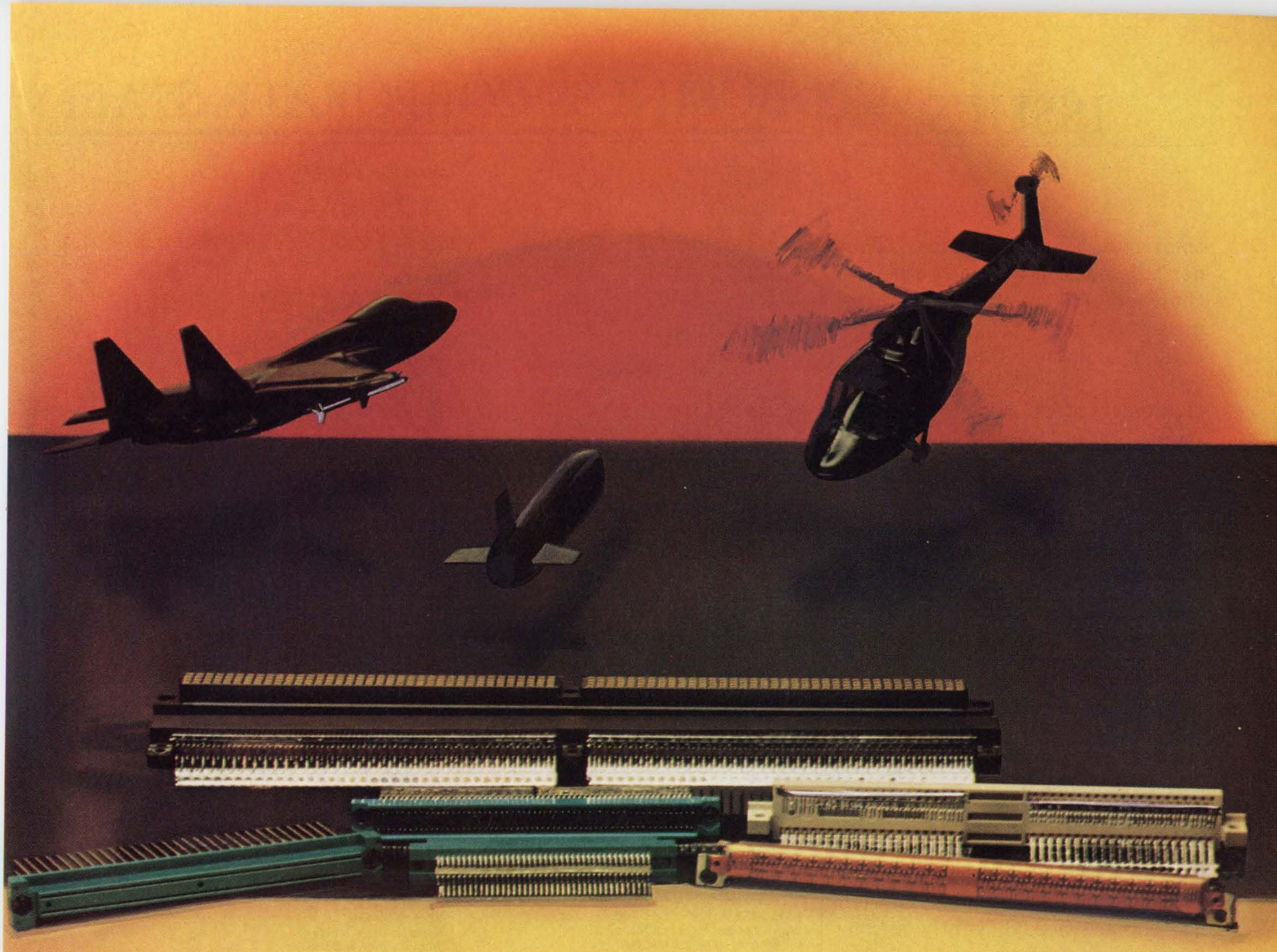
California State's engineering students aren't required to take Edwards' class, but advisers strongly recommend the course as a complement to the students' engineering classwork. About 40% of Edwards' students are engineering majors. Those that enroll "let it be known that this is soft stuff compared to what they're used to," she says. Called upon to use their visual and perceptual skills, however, the engineering students discover how different such skills are from those they're accustomed to using. "They go through a period of bafflement because the problems are ones they don't know how to solve," Edwards says.

Although some students drop the class in frustration, most complete the course, and some return to tell Edwards how the "sight" training has helped them in their engineering. "Students say that they can now visualize problems to a larger extent and they can scan solutions without calculating all of them. They feel their thinking is more flexible," Edwards says.

The business community's rising interest in acquiring the same kind of expansive vision is evident in the growth of companies like Synectics, which now employs a staff of 50 to serve its 150 clients. Often, it is companies' misconceptions about the generation of new ideas, and the subsequent poor results, that send them looking for assistance, Sebell says. For example, some companies, hoping to put innovative products on the market, think they can simply order a batch from their design staff. Nothing stifles employees' creativity more quickly, says Sebell. "Creativity is a function of quality thinking and climate. Too few companies really foster the climate of innovation that they claim to stand for."

Synectics lists a long string of successes in the consumer sector. The company credits itself with assisting in the development of General Electric's line of Space Saver appliances, Sunoco's dial-your-own-octane gas pumps, and vandal-resistant pay telephones for New York Telephone. But in the electronics sector, which prides itself as a bastion of innovation, the idea of using outsiders to assist in creative ventures has proved much harder to sell.

"High-technology companies say to us, 'We've got enough creativity in our business,'" says Sebell. In addition to making the same creativity-related mistakes that consumer companies make, he says, high-technology companies have



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their own set of problems. "They don't listen well—to each other, to their employees, to the marketplace." But more companies are beginning to warm to the idea of creativity consultants. AT&T, Digital Equipment Corp, General Electric, IBM, Lotus Development, Wang Laboratories, and Westinghouse Electric are all clients of Synectics.

As the number of creativity consultants grows, some consultants are beginning to question the quality and effectiveness of learning sessions. The lasting value of such workshops can be difficult to gauge, says Edwards, who is herself a part-time consultant and workshop leader. "They're interesting, and they expose people to new ideas, but they're equivalent to a weekend retreat. If you didn't know how to read, and you spent a weekend learning, you'd come away with some knowledge of reading. But unless you practiced diligently on your own, you'd soon forget most of what you learned."

In addition to an individual's commitment to becoming skilled at putting creative powers to use, commitment is needed at the corporate level. Edwards says that despite companies' vocal support of creativity workshops and the processes that go along with them, few firms provide employees with either the time or the space they need to develop ideas. Rubenstein agrees: "We preach creativity, but we don't support it."

No matter how well a company plans, or how skillfully it thinks it can predict the future, Rubenstein cautions, "no one's crystal ball is without error." Giving more time to the development of new ideas, he says, is key to a company's success. **EDN**

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CAREER OPPORTUNITIES

1987 Editorial Calendar and Planning Guide

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Apr. 15	Mar. 26	Microprocessor Technology; Software Development; Digital ICs	Closing: Apr. 2 Mailing: Apr. 23
Apr. 30	Apr. 9	Communications Special Issue; ASICs; Test & Measurement	
May 14	Apr. 23	Analog Technology Special Issue; ICs; Test & Measurement	Closing: Apr. 30 Mailing: May 21
May 28	May 7	Computer Peripherals; Software; Power Sources/Devices	
June 11	May 21	Math ICs; CAE; Computers	Closing: May 28 Mailing: June 18
June 25	June 4	ASIC (Semicustom ICs) Directory; Analog ICs; Surface-Mount Technology	
July 9	June 18	Product Showcase-Volume I; ICs & Semiconductors; Software	Closing: June 25 Mailing: July 16
July 23	July 2	Product Showcase-Volume II; Computers & Peripherals; Test & Measurement Instruments	
Aug. 6	July 16	Computer Boards; Digital Signal Processing; Test & Measurement; Top Ten Reader Vote Contest	Closing: July 23 Mailing: Aug. 13
Aug. 20	July 30	Military Electronics Special Issue; Fiberoptics; Software	

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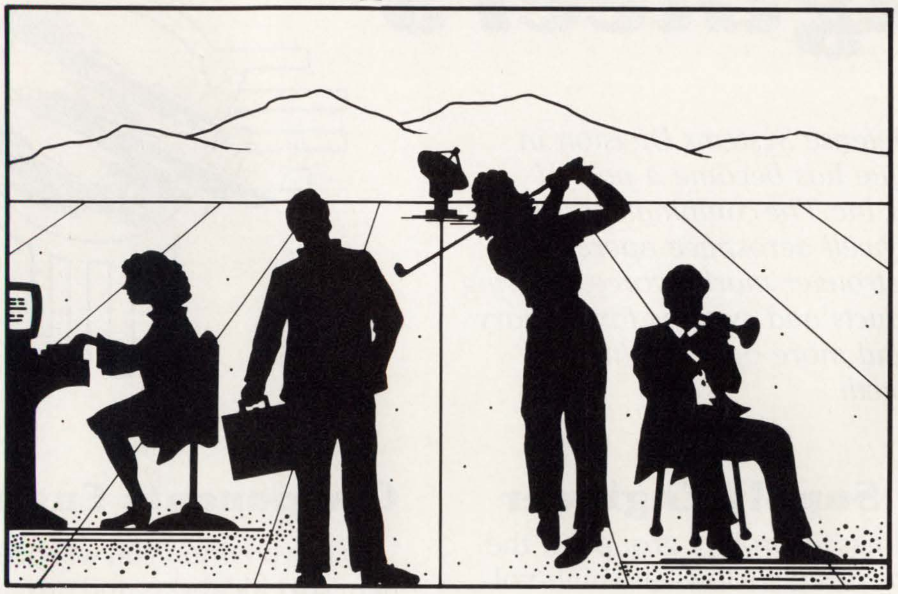

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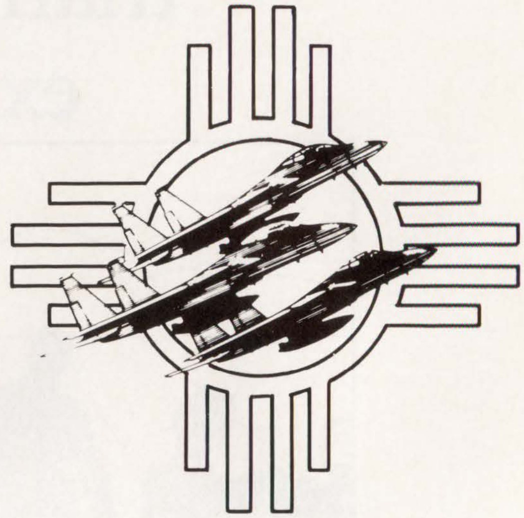

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In this position you will perform circuit stress analysis, reliability prediction and failure mode analysis and participate in reliability development testing. A BSEE degree and two or more year's experience is required.

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In this position you will prepare component specifications and provide technical liaison between Sperry Aerospace and component vendors. We need people who are specialists in electrical, electronic and mechanical components. A BS degree in engineering or one of the physical sciences is required.

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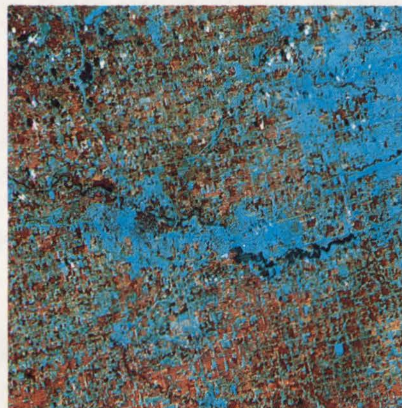


ERIM's Ann Arbor headquarters is home for a majority of our 700 staff members. This research and development facility contains electronic, measurement, and fabrication laboratories, computer facilities, workshops, and offices.

Our Flight Facility at Willow Run Airport houses two aircraft instrumented to pursue sensor research. It is equipped with everything necessary to operate, modify, and maintain the aircraft and to operate airborne sensor equipment.

The Institute operates a number of offices around the country, each with staff and programs customized for the sponsors in its area.

Los Angeles, California

Like the other ERIM offices, the Los Angeles facility was established to provide quick reaction and on-site technical support to sponsors on the West Coast. The office specializes in systems engineering, sensor applications analysis and development, digital signal processing, and systems performance analysis.

The backgrounds of staff members in Los Angeles span the engineering disciplines, with concentrations in electrical engineering, electro-optical and radar engineering, signal processing, and computer science.

Dayton, Ohio

Recently, ERIM established its newest office in Dayton, Ohio. This facility exists to support the Institute's programs with the Aeronautical Systems Division, the Air Force Wright Aeronautical Laboratories, and the Foreign Technology Division at Wright-Patterson Air Force Base.

Its mission is to provide sponsors with quick reaction in terms of technical expertise and support for programs dealing with synthetic aperture radar, electro-optics, and image and data processing systems. Staffing is currently in progress to support these technical areas.

Washington, DC

The largest of ERIM's branch locations is in Arlington, Virginia where about 40 staff members provide technical support to and liaison with sponsors in the Washington area. The office also offers general technical support to all Institute programs in addition to performing work on its own contracts.

While work at the facility covers the entire spectrum of Institute activities, there is a concentration on the interpretation and exploitation of synthetic aperture radar data with a special emphasis on human factors involved in information extraction.

Technical staff at the Washington office consists primarily of engineers and other physical scientists; other disciplines include mathematics, human factors engineering, and image and intelligence analysis.

Niceville, Florida

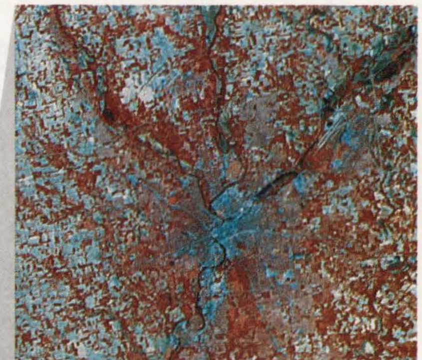
ERIM's Florida office was established in 1986 to help the Institute expand its customer base and technical horizons by moving into areas such as millimeter wave radar and imaging sonar. Intelligent weapons technology is a major focus, both in basic concepts and applications research, as well as systems development.

Staffing is currently underway. Areas of interest include millimeter wave radar, electro-optics, imaging sonar, and computer science/analysis.

Career Opportunities

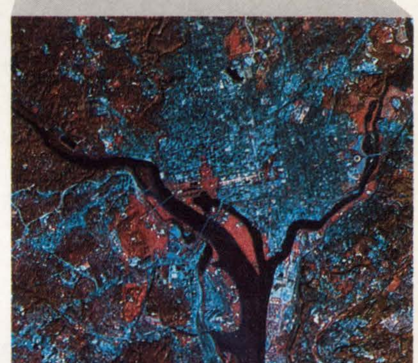
ERIM has research and management positions available at several levels in the following areas:

- **Radar System Design**
- **E-O/IR System Design and Analysis**
- **Computer Vision**
- **Optical Computer System**
- **Phase Retrieval/Signal Reconstruction**



- **Radar System Engineering and Analysis**
- **Signal and Image Processing**
- **Microwave Scattering and Measurement Engineering**
- **Diffractive Optics**

All positions require a BS, MS, or PhD in engineering, physics, mathematics, or statistics, along with appropriate work experience. Salary and benefits are highly competitive.



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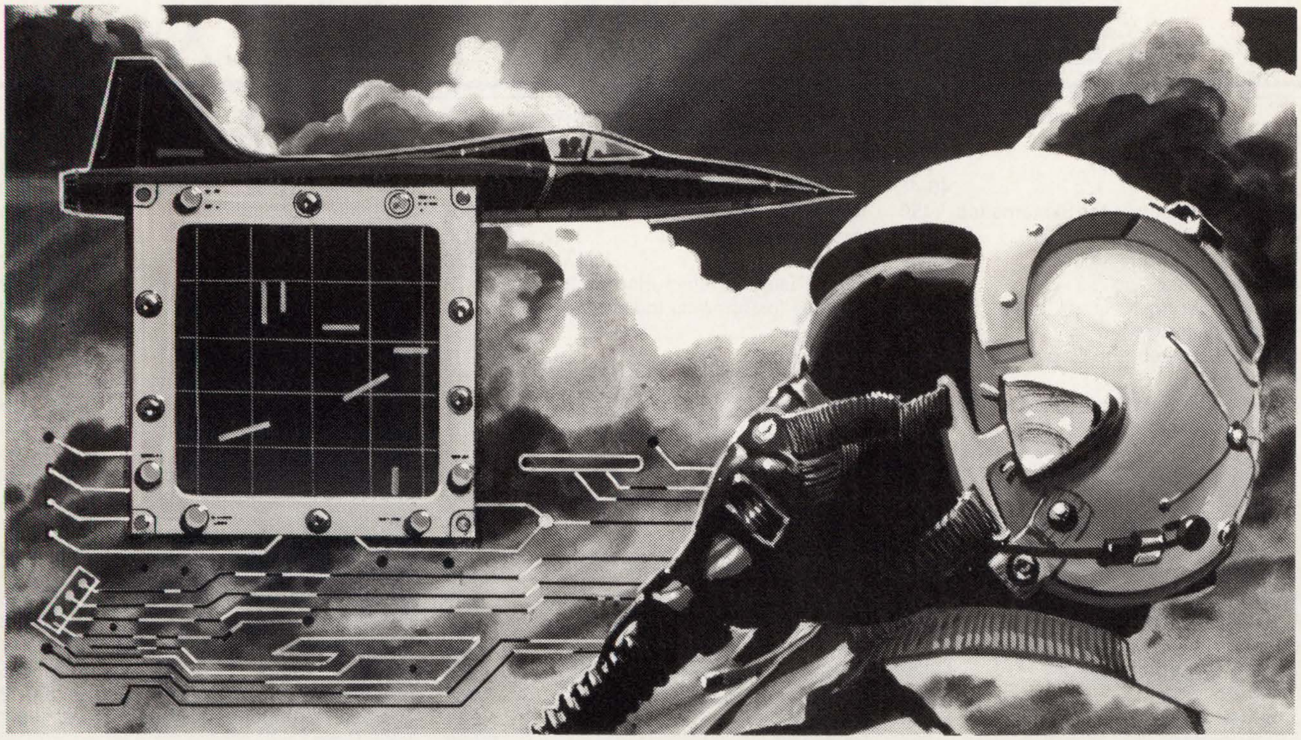

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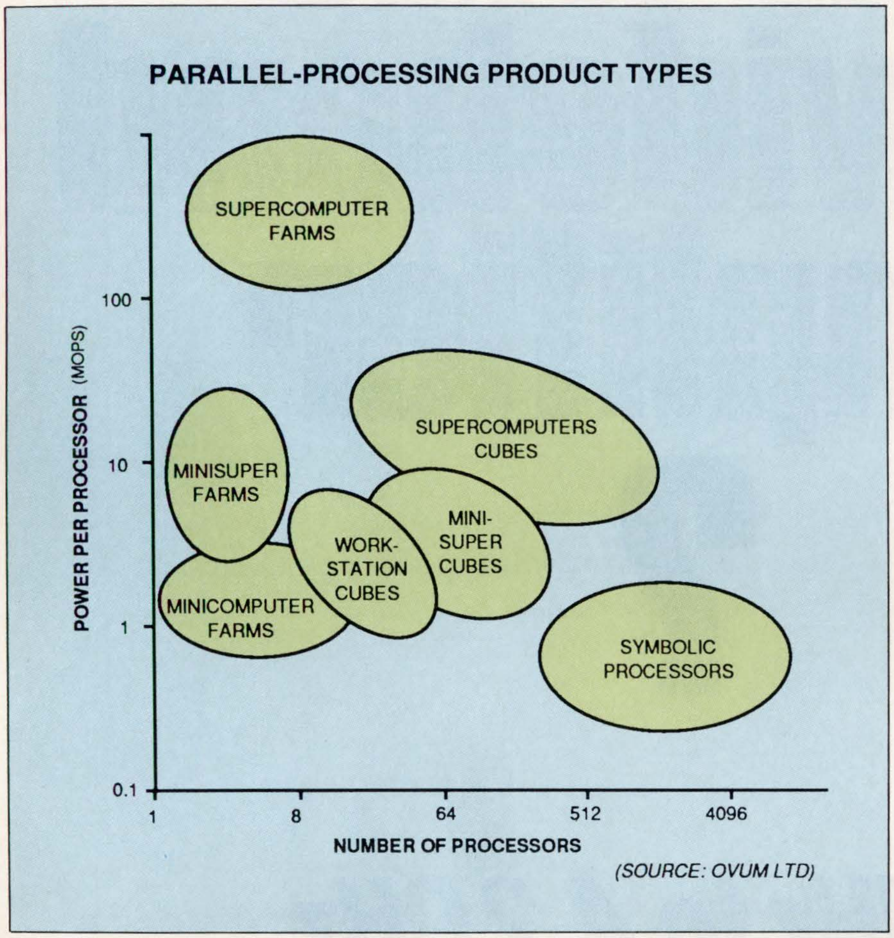

Future of supercomputers lies in parallel processing

The total market for supercomputers employing parallel-processing architectures will increase from $600 million in 1986 to $8.6 billion in 1992, reports the market-research company Ovum Ltd of London, UK. One development having a significant impact on the overall supercomputer market, says Ovum, will be the use of industry-standard microprocessors or semicustom components in parallel architectures that will improve price/performance ratios.

The comparative costs per one million operations per second (mops) speak highly for parallel processing, says Ovum. The cost per mops on a minicomputer ranges from $30,000 to $60,000; the cost per mops for a parallel-processing machine can range from $400 to $12,000, with many machines falling in the $3000 to $6000 range. Parallel computers built from large numbers of low-cost µPs have some drawbacks, however. They do not generally have, as yet, the I/O channels, the different levels of memory, the language compilers, the programming environments, and other facilities that users require to achieve large throughputs.

Indeed, parallel processors will not be an entirely transparent innovation as far as the user is concerned, reports the market-research company. At a minimum, there will be changes in software and operating methods, and the opportunities offered by parallel processing may be so great that some users will want to change the working methods at fundamental levels. (See "Industry needs design-automation experts to unleash the power of supercomputers," EDN, August 7, 1986, pg 259.)

For the purposes of analysis, Ovum distinguishes between two different types of parallel-processing products. A typical "farm" comprises a small number of processors—usually no more than eight. These processors communicate through some form of shared memory, which they access over a bus or network of direct processor-to-processor connections. A "cube" incorporates large numbers of processors—128, 1024, or even 65,536, in the case of the Connection Machine built by Thinking Machines Corp (Waltham, MA).

Power ICs: one hot hitter in US semiconductor slump

In the still depressed US semiconductor market, one segment remains profitable and will continue to show strong sales figures for the foreseeable future. According to the market-research concern Frost & Sullivan Inc (New York, NY), power semiconductors currently constitute a $1 billion market and will form a $2.25 billion market in 1991.

The relatively new power ICs known as "smart power" devices are already in high demand, and growth in their sales will be the fastest of all power semiconductor types. The average annual growth rate over the period 1985 to 1991 will be 100%, from $10 million to $600 million.

F&S reports that FET-type power semiconductors—and particularly those of the MOSFET variety—are also quickly gaining in popularity. F&S estimates US MOSFET sales at $140 million for 1985, and it expects sales of these devices to total $580 million in 1991. Meanwhile, the standard "workhorse" devices—zener diodes and rectifiers, bipolar transistors, and thyristors—will continue to show steady market growth.

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