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FEBRUARY 18, 1991

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report: Off-the-shelf adapters simplify SMT troubleshooting pg 146

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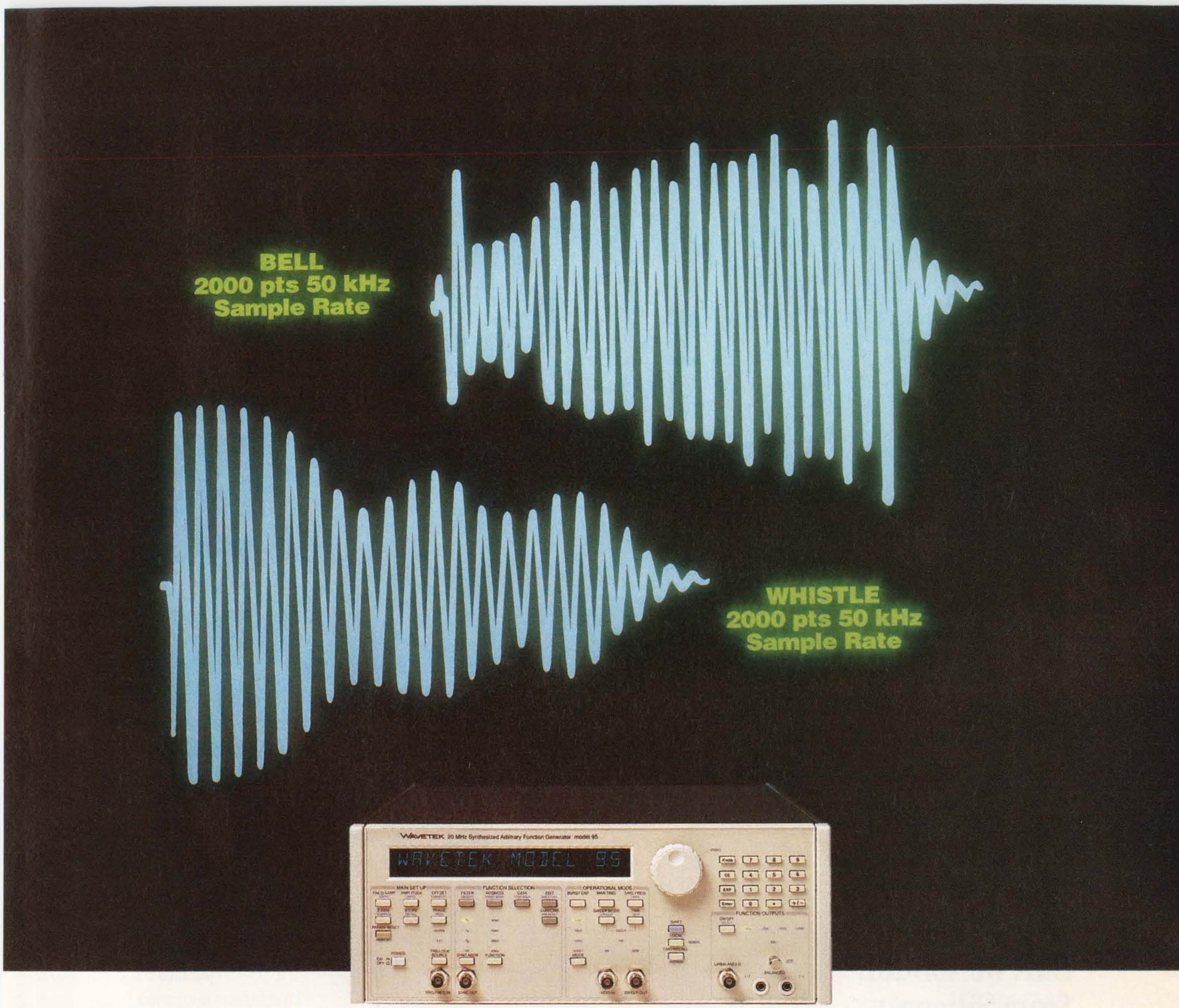

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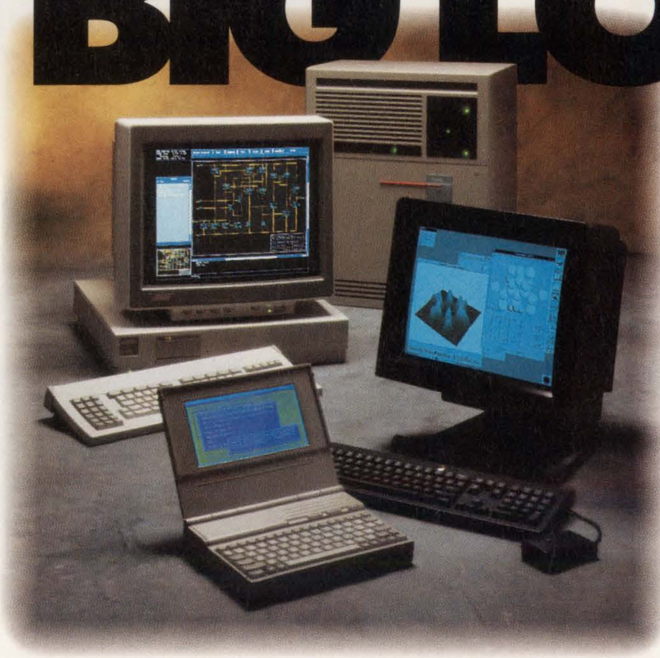

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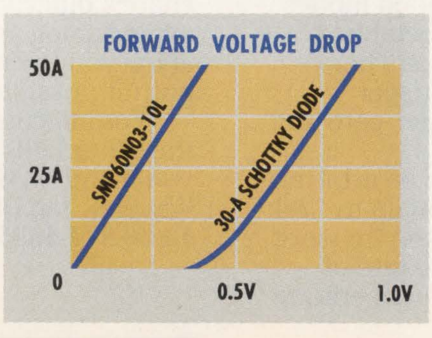

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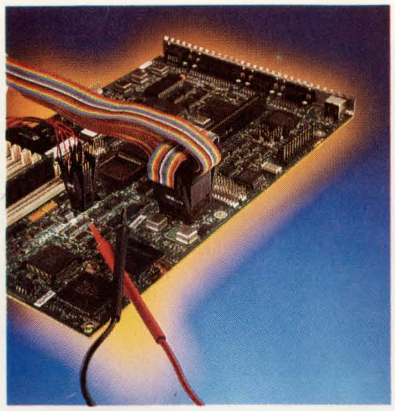
EDN® Magazine Edition

Volume 36, Number 4

February 18, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Off-the-shelf adapters let you concentrate on the benefits of surface-mount technology. They alleviate the inconveniences of testing and troubleshooting prototypes that contain high-level ICs. See the Special Report on pg 146. (Photo courtesy 3M, Electronics Div)*

Continued on page 7

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CIRCLE NO. 3

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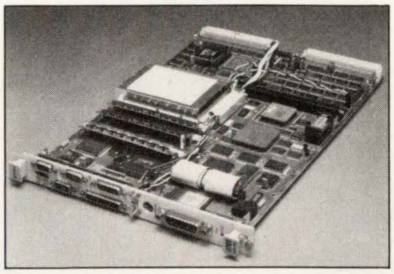

***Before selecting a VXI** (VME extensions for instrumentation) mainframe, explore the pros and cons of several system configurations (pg 89).*

Continued on page 9

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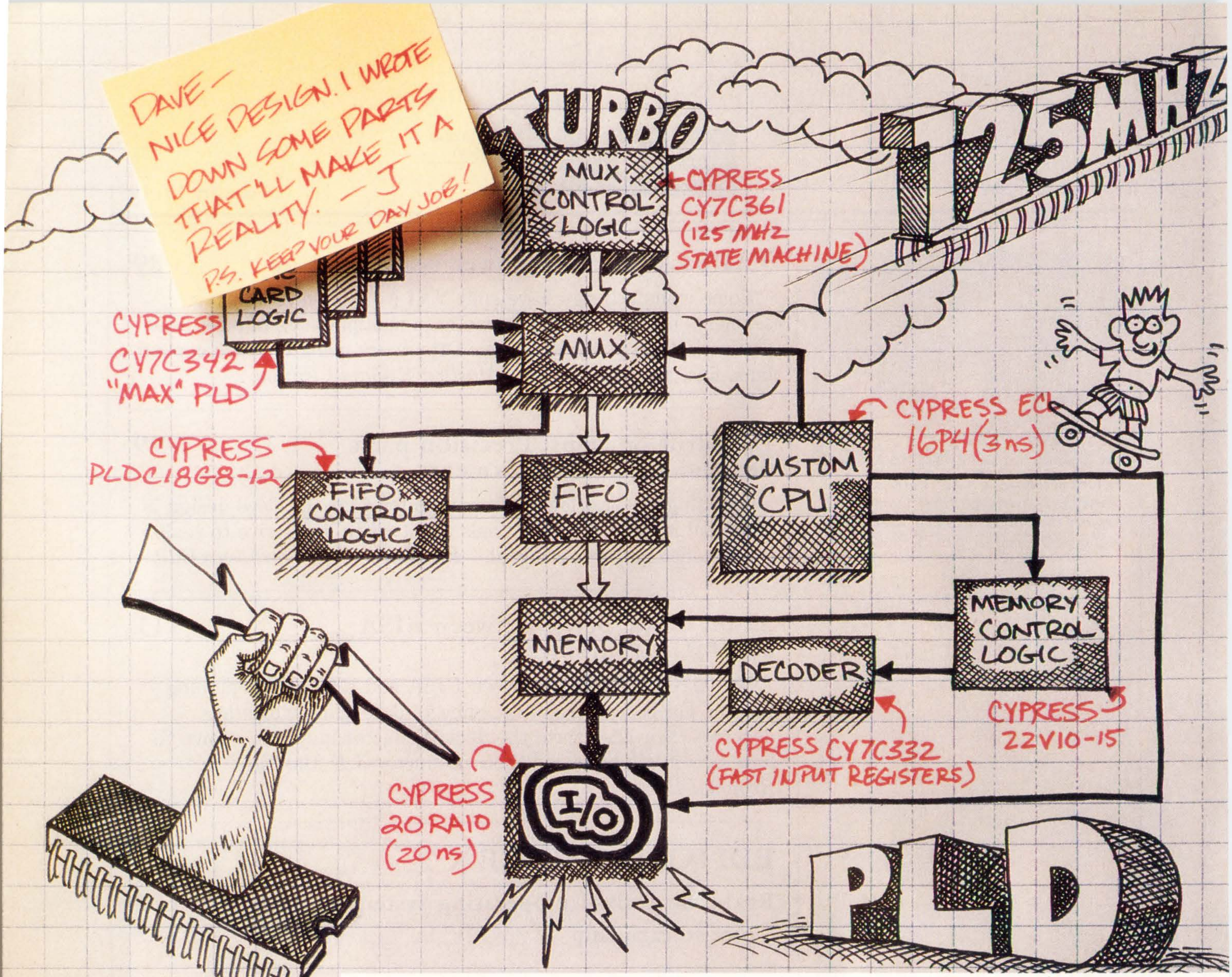

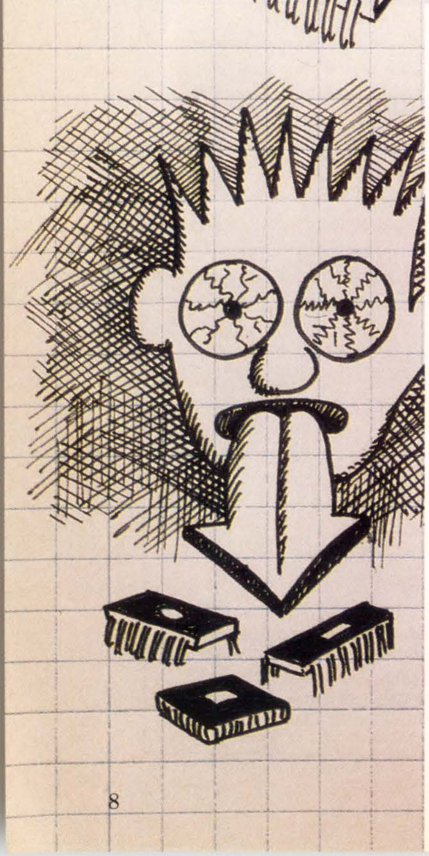

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Three new multi-function I/O controllers offer highly integrated solutions for all IBM PC/XT/AT systems. The MCCS16C462 is the industry's only "452" standard with an on-board crystal driven clock reference. This dual serial and single parallel port controller combines a 452 pinout with all the space and money savings of its own crystal oscillator. Motorola also makes two other controllers for use with a TTL clock reference—the single serial, single parallel MCCS16C451 and the dual serial, single parallel MCCS16C452.

New additions to the first family of EIA-232.

Two new families expand Motorola's industry-standard EIA-232 product lines—the MC145406/07 for notebook applications and the MC145403/4/5/8 for desktop applications.

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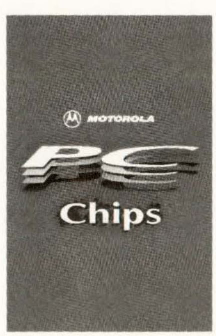

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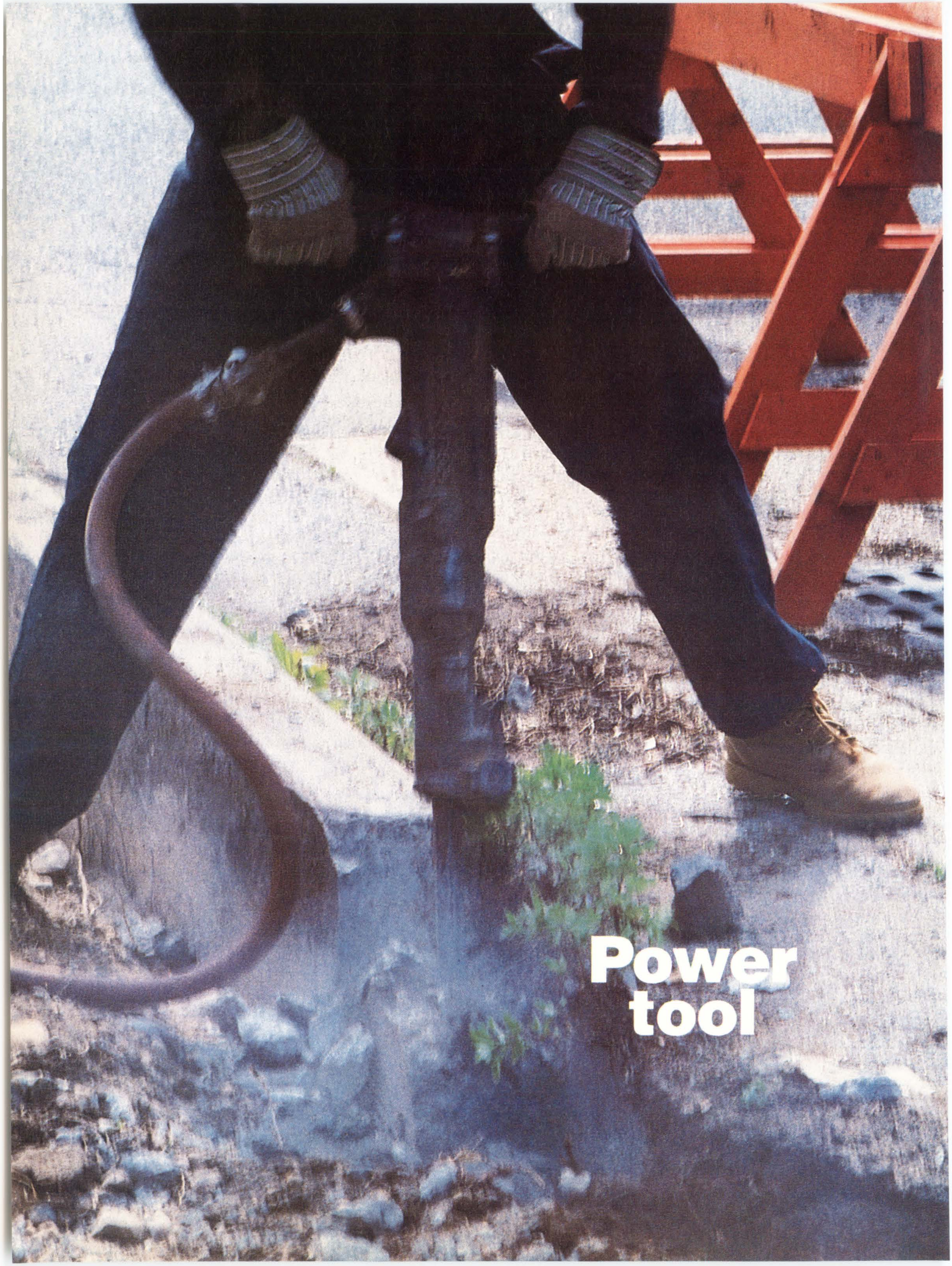
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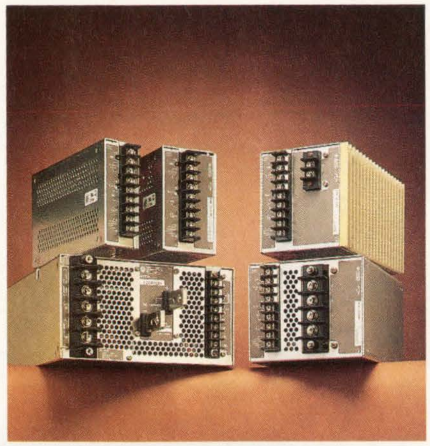

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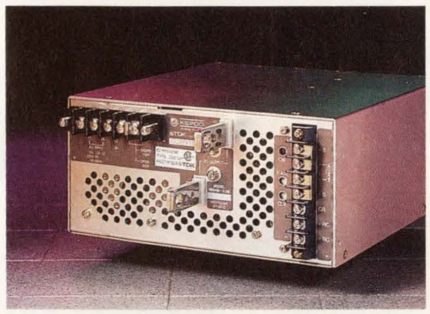

ac to dc power single output 600W

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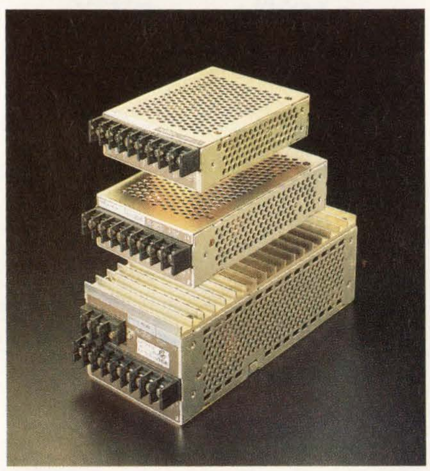

dc to dc power single output 30W, 60W, 150W

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- ☐ 24 and 48V input (60V available on some models)
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- ☐ Tested to MIL STD 810D

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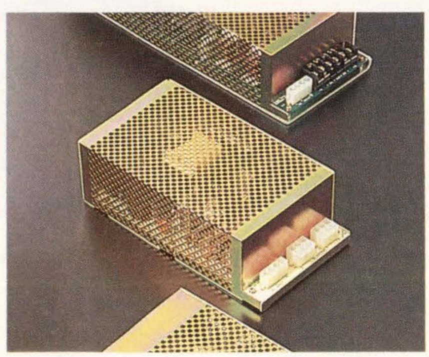

ac to dc power single output 30W, 60W, 120W, 240W

- ☐ 5V-24V dc output
- ☐ jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
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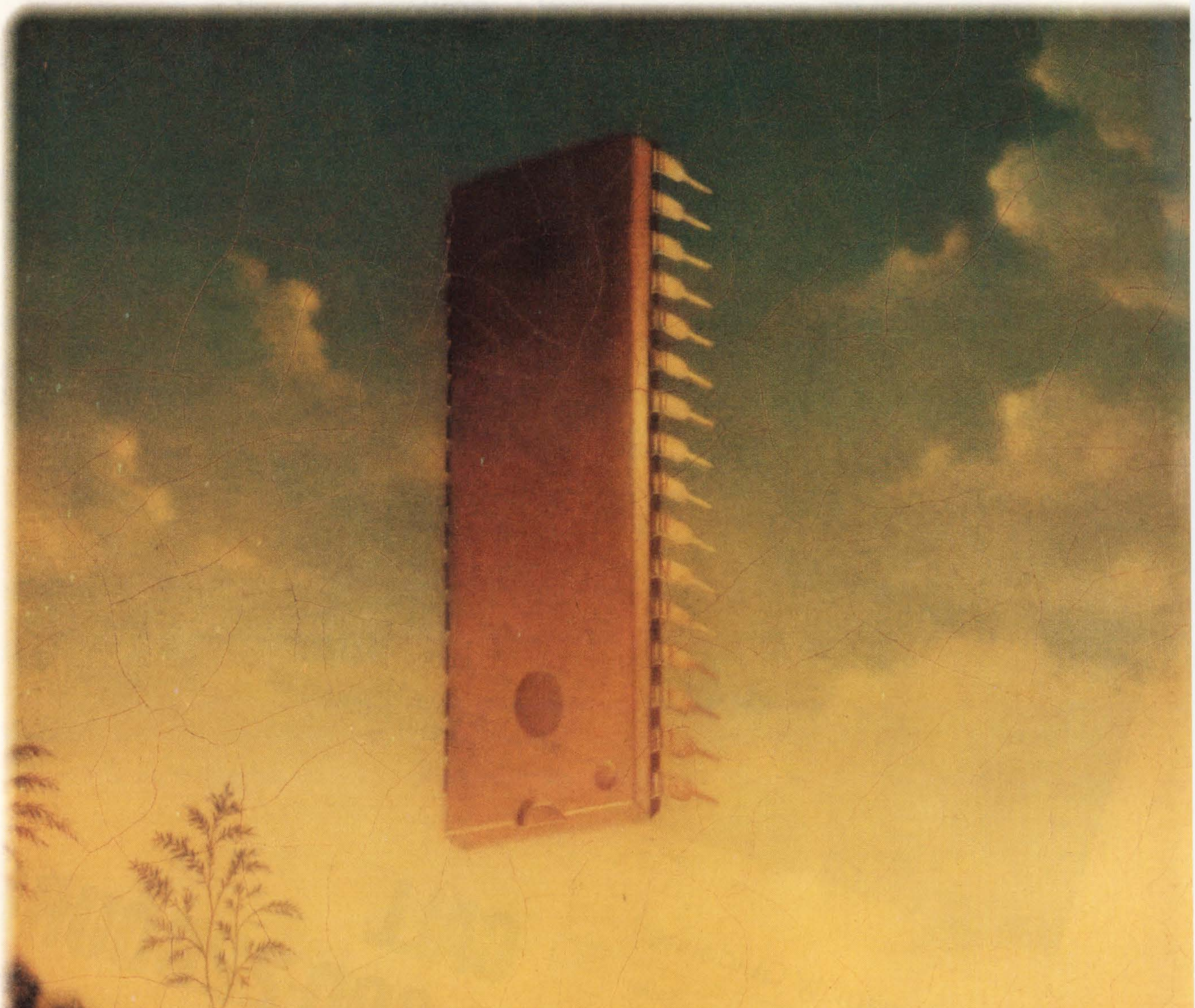

NEWS BREAKS

EDITED BY SUSAN ROSE

VMEBUS 68040-BASED BOARDS INTRODUCED AT BUSCON WEST

Several board vendors introduced VMEbus products based on the 68040 μP at Buscon West in Santa Clara, CA, Jan 29 to 31. Force Computers and Radstone Technology introduced 68040-based boards with 32-bit VMEbus implementations. Radstone's Model 68-42 includes a 68020 auxiliary processor that controls onboard I/O such as SCSI, Ethernet, and RS-232C. The board also includes as much as 2M bytes of dual-ported zero-wait-state static RAM. The 68-42 can accommodate 40-MHz μPs. A 25-MHz base configuration costs $6495. Base configurations of the Force CPU-40 with no dynamic RAM start at $3990. The board can hold as much as 16M bytes of dynamic RAM, and it includes the company's Eagle 32-bit daughter-board interface. Synergy Microsystems introduced a VME64 68040-based board, the SV430 (for additional information, see page 128). Force Computers, Campbell, CA, (408) 370-6300, FAX (408) 374-1146. Radstone Technology, Montvale, NJ, (201) 391-2700, FAX (201) 391-2899. Synergy Microsystems, Encinitas, CA, (619) 753-2191, FAX (619) 753-0903. —Maury Wright

OCTAL, 8-BIT DACs REPLACE EIGHT POTENTIOMETERS

You can replace as many as eight potentiometers with each DAC-8840 and DAC-8841 octal, 8-bit, multiplying DAC from Analog Devices. Serial commands set each converter's gain, and the devices handle analog signals from dc to 1 MHz. The DAC-8840 runs on ±5V and has 4-quadrant multiplication. The DAC-8841 runs on 5V and performs 2-quadrant multiplication. The ICs cost $9.95 (100). Analog Devices, Norwood, MA, (617) 329-4700, FAX (617) 326-8703, TLX 924491.—Steven H Leibson

CAE TOOL OPENS WINDOWS ON PLD DESIGN

Altera Corp's Max+Plus II PLD design tool runs under Microsoft Windows 3.0. The Windows-based version of the company's Max PLD family, like the DOS version, has hierarchical schematic capture, hardware-description-language logic entry, logic synthesis, and timing simulation. The tool also handles the company's EP Classic and 7000 series PLDs and multipart partitioning and waveform-logic-entry capabilities. It also has an integrated EDIF interface to other CAE tools.

The tool allows multiple windows on the same file, letting you simultaneously view your entire design and zoom in on a small section. You can also rapidly switch between design entry, compilation, and timing simulation. The memory management provided by Windows 3.0 lets the new version handle larger designs and simulate faster than the DOS version. The tool also has a degree of hardware independence—the Windows graphics interface handles the need for drivers for your graphics card. The design tool costs $9995 and will be available in April. Altera Corp, San Jose, CA, (408) 984-2800, FAX (408) 954-0348.—Richard A Quinnell

RF SIMULATOR PARTITIONS LINEAR AND NONLINEAR CIRCUITS

A harmonic-balance algorithm within jOmega from EEsof lets you simulate and optimize RF circuits operating at 30 to 3000 MHz. The algorithm allocates and manipulates your design between the software's linear and nonlinear simulators. The $24,500 package also includes a schematic editor; a statistical-analysis capability that lets you balance performance, cost, and yield constraints; and 50 RF package-level circuit and standard bipolar junction transistor models. A $5000 optional floor planner enhances your everyday pc-board software by working with the simulator to help you account for layout effects during simulation. EEsof, Westlake Village, CA, (818) 991-7530, FAX (818) 991-7109.—Michael C Markowitz

DRIVER-TRANSLATOR HAS 3.5-NSEC PROPAGATION DELAY

The 10G014 driver-translator from Gigabit Logic accepts four pairs of ECL inputs and multiplexes them to four differential TTL outputs. The propagation time is typically 3.5 nsec. The primary application for the chip is a dynamic RAM and static RAM driver for memories requiring multiplexed row and column addresses. The open-drain TTL outputs have 90-mA drive capability for large bused-memory architectures with high capacitive loads. The chip requires ±5V supplies and dissipates 500 mW typically. For compatibility with other ECL products, the negative supply also operates off −4.5 or −5.2V. The $13.90 (10,000) chip is available in a 44-pin plastic leaded chip carrier or a 40-pin leaded or leadless ceramic chip carrier. Gigabit Logic, Newbury Park, CA, (805) 498-9664, FAX (805) 499-2751.—Doug Conner

36-BIT-WIDE FIFO MEMORY CLOCKS AT 40 MHz

The LH5420 FIFO memory from Sharp provides two banks of 256×36-bit memory for bidirectional operation. The highest speed device clocks at 40 MHz and features a 15-nsec access time. You can also use the device as a data funnel because one of its two I/O ports will operate as a 9- or 18-bit port in addition to the full word width. Each I/O port has full, half-full, empty, and programmable almost-full and almost-empty flags. A bypass mode and two mailbox registers allow you to pass commands and status information through the device without sending them through the FIFO-memory section. Sample pricing is $130. Sharp Electronics Corp, Mahwah, NJ, (201) 529-8757, TLX 426903.—Steven H Leibson

CONFORMANCE SOFTWARE TESTS AT THE RIGHT PRICE

With a piece of software, you can test math coprocessors for 80386-based personal computers against the IEEE-754-1990 standard test suite for 80-bit computer arithmetic. Coprocessors that fail to meet the specification cause insidious errors because the computer does not give any indication that the data it is generating are incorrect. The coprocessor conformance software that catches these errors was developed at the University of California, Berkeley. Cyrix Corp is distributing it free of charge (limit one per customer). Ask for the IEEE test suite. Cyrix Corp, Richardson, TX, (214) 234-8387, FAX (214) 234-8397.—Michael C Markowitz

VXIBUS DIGITAL WORD GENERATOR OPERATES AT 50 MHz

The IT4620 digital word generator from Interface Technology provides 16 channels when operating at 50 MHz or 32 channels when operating at 25 MHz. If you need more channels you can add IT46E20 expansion cards, each providing an additional 32 channels at 50 MHz or 64 channels at 25 MHz. Memory depth is 16k words for 50-MHz operation or 8k words for 25-MHz operation. You can generate complex patterns with these word generators by organizing the data in nested-loop sequences. A timing-simulator mode lets you independently control the time duration of each word. The IT4620 costs $4950, and the IT46E20 costs $1950. Orders will be accepted in March; initial deliveries take eight weeks. Interface Technology, Glendora, CA, (818) 914-2741, FAX (818) 335-8346.—Doug Conner


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NEWS BREAKS

VOLTAGE REGULATOR HAS 1V DROPOUT VOLTAGE, AND MORE

The LT1185 from Linear Technology Corp is a low-dropout and negative voltage regulator with a user-adjustable current limit. The regulator has a guaranteed dropout voltage of 1V at 3A. At lower currents, the dropout voltage is lower. Most older 3A regulators feature a fixed 5A current limit. This current level permits overloads, which can potentially damage the input components, such as transformers and diodes. Being able to set the current limit precisely at a value just above the normal operating range reduces stress and eases design requirements of the input power circuitry that goes with the regulator. If you don't set a limit, the device's internal limit sets it for you. The output voltage range of the regulator is −2.5 to −25V. If the input voltage is floating and you ground its output, the device operates as a positive voltage regulator. The device comes in a 5-lead TO-3 metal can that operates over −55 to 150°C, and in a 5-lead TO-220 package that operates over 0 to 125°C. The TO-220 molded plastic package costs $3.70 (100). Linear Technology Corp, Milpitas, CA, (408) 432-1900, FAX (408) 434-0507.—Anne Watson Swager

TEST GENERATOR MODULES AND RF PRODUCTS FOR VXIBUS

Racal-Dana's VXIbus products include digital test modules, RF prototyping modules, and RF enclosures. The Model 6451 digital test module supports 48 bidirectional TTL-level channels at 20 MHz. You can synchronize multiple modules for a total of 576 channels. You can also configure the channels as 48 separate stimulus channels and 48 response channels. Channel-to-channel skew is ±5 nsec within a module and ±7.5 nsec across multiple modules. The C-size module is $14,995; delivery is 16 weeks.

For RF applications, the company manufactures the 1261E VXIbus chassis. The double-skin chassis provides typical shielding effectiveness of 100 dB. To reduce noise sources further, the chassis uses low-noise and low-ripple linear supplies. The chassis costs $11,995 and has a 16-week delivery. Also for RF applications is the Model 7065 prototyping module. The module includes message-based VXIbus interface circuitry, provides efficient heat dissipation, and maintains an EMI-shielded environment for the prototyping area. The chassis are available in single- and double-width C-size modules and prices start at $2495. Delivery is 16 weeks. Racal-Dana, Irvine, CA, (800) 722-3262, FAX (714) 859-2505.—Doug Conner

CONTROL IEEE-488 DEVICES WITH C++

The addition of Turbo C++ routines to the module library of the $495 HP 82335A IEEE-488 interface card expands the number of programming languages supported by the product to 12. Other language modules support Basic, Pascal, and C compilers and interpreters from several vendors. The card also includes printer and plotter drivers for serial- and parallel-interface peripherals. Hewlett-Packard Co, Palo Alto, CA, phone or FAX the local office.—Steven H Leibson

CONTRACT TEST ON A BUDGET

Integrated Measurement Systems has formed an engineering group to design custom test systems for low-volume-production test applications. The engineering group will focus on testing complex ICs and pc boards. These systems will cost much less than production test equipment. The group will specialize in applications that have stringent mixed analog-digital test requirements, including automotive, medical,

and telecommunications. It will provide design and test engineers with a range of services, including turnkey product development for a variety of test applications, third-party hardware/software integration services, and test consulting. Through a strategic-partnership program, the company can team up with leading test equipment manufacturers to develop fully integrated, off-the-shelf test stations. Integrated Measurement Systems Inc, Beaverton, OR, (503) 626-7117, FAX (503) 644-6969.—Anne Watson Swager

NEW DIVISION PROVIDES BOARD DESIGN AND MANUFACTURING

A new division of S-MOS Systems offers board-level design, manufacturing, test, and assembly. The company will produce custom boards and modules for laptop, portable, and notebook computers, and small communication products such as cellular phones and pagers. The company is the only US vendor that can offer surface mounting and pin-through holes in conjunction with chip-on-board, tape-automated bonding (TAB) and chip-on flex capabilities. Multilayer boards can have eight layers. You can incorporate ICs having 0.5-mm-pin pitch on a board which allows three traces between pins. The facility is also developing the capability to handle ICs with 0.25- to 0.30-mm-pin pitch, allowing three to four traces between pins.

TAB packages can accommodate 256-pin dies and will be able to handle 500-pin dies in the near future. In addition, the boards can accommodate 0.5-mm-pin pitch quad flatpacks with 256 pins. The company will accept volumes as low as 5000 units/year for large, complex designs and as many as 500,000 units/year for less integrated designs. S-MOS, Raleigh, NC, (919) 878-1120, FAX (919) 878-1125.
—John Gallant

5½-DIGIT ADC HAS 10-μV RESOLUTION

Harris Semiconductor's HI-7159 5½ digit ADC integrates ADCs with 10 μV—1 count in 200,000—resolution. The converter's dual-slope architecture provides this resolution with no other critical external components. The device uses ratiometric measurements for its 5½-digit precision, and autozeroing to eliminate zero drift over temperature. The converter's linearity has a maximum of ±3 counts and is typically ±1 count. The conversion rate for 5½-digit resolution is 15 conversions/sec. Speed increases to 60 conversions/sec when you switch the device to a 4½-digit, uncompensated mode. The converter has three interface options—two serial and one parallel. You can program the serial modes for one of four common baud rates. Samples of 28-pin DIPs are available now. Production quantities will be available by the end of March for $20 (100). Harris Semiconductor, Melbourne, FL, (800) 442-7747, FAX (407) 724-3111.—Anne Watson Swager

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Instrument-system designers working with the VXIbus can add two more choices to their rosters: the HP E1420A universal counter and the HP E1426A digitizing oscilloscope. The $3450 counter provides two 200-MHz input channels and can take more than 40 measurements/sec. The $6960 digitizing oscilloscope has four 500-MHz input channels, takes 8-bit measurements at 20M samples/sec, and occupies two C-sized bus slots. You can use a measurement-averaging feature to boost the scope's resolution to 10 bits. Hewlett-Packard Co, Palo Alto, CA, phone or FAX the local office.—Steven H Leibson

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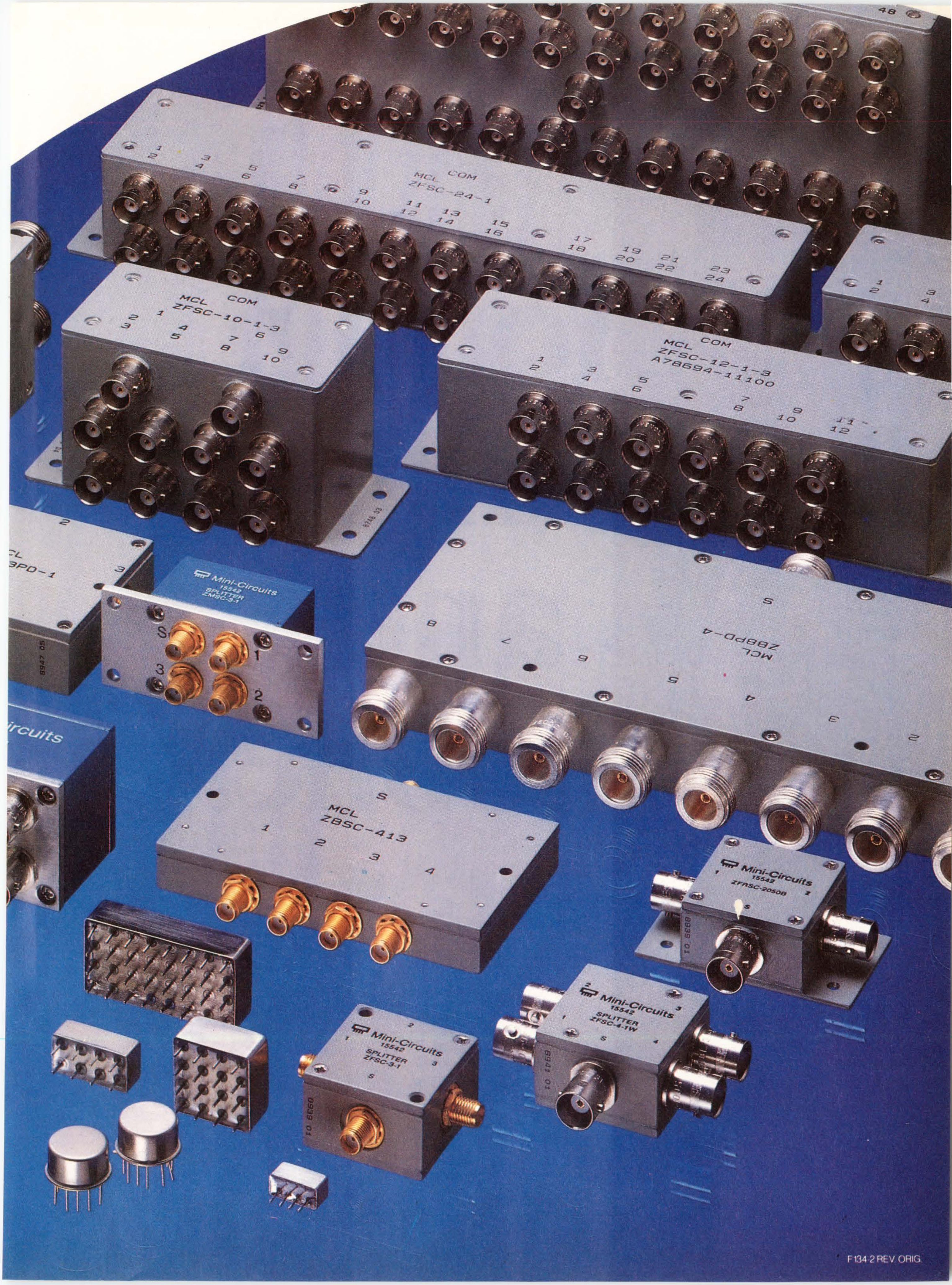

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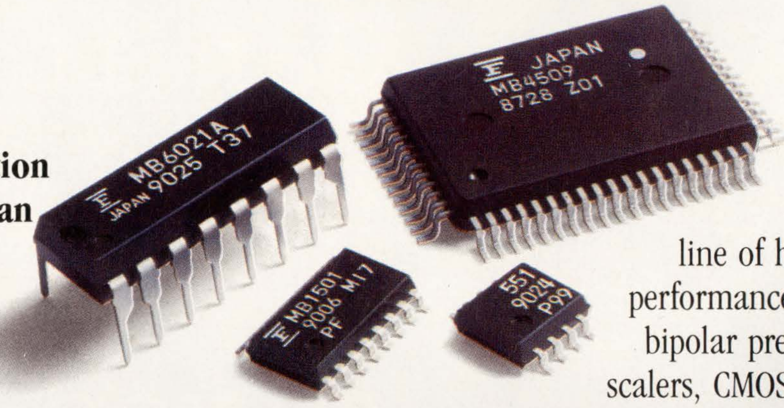

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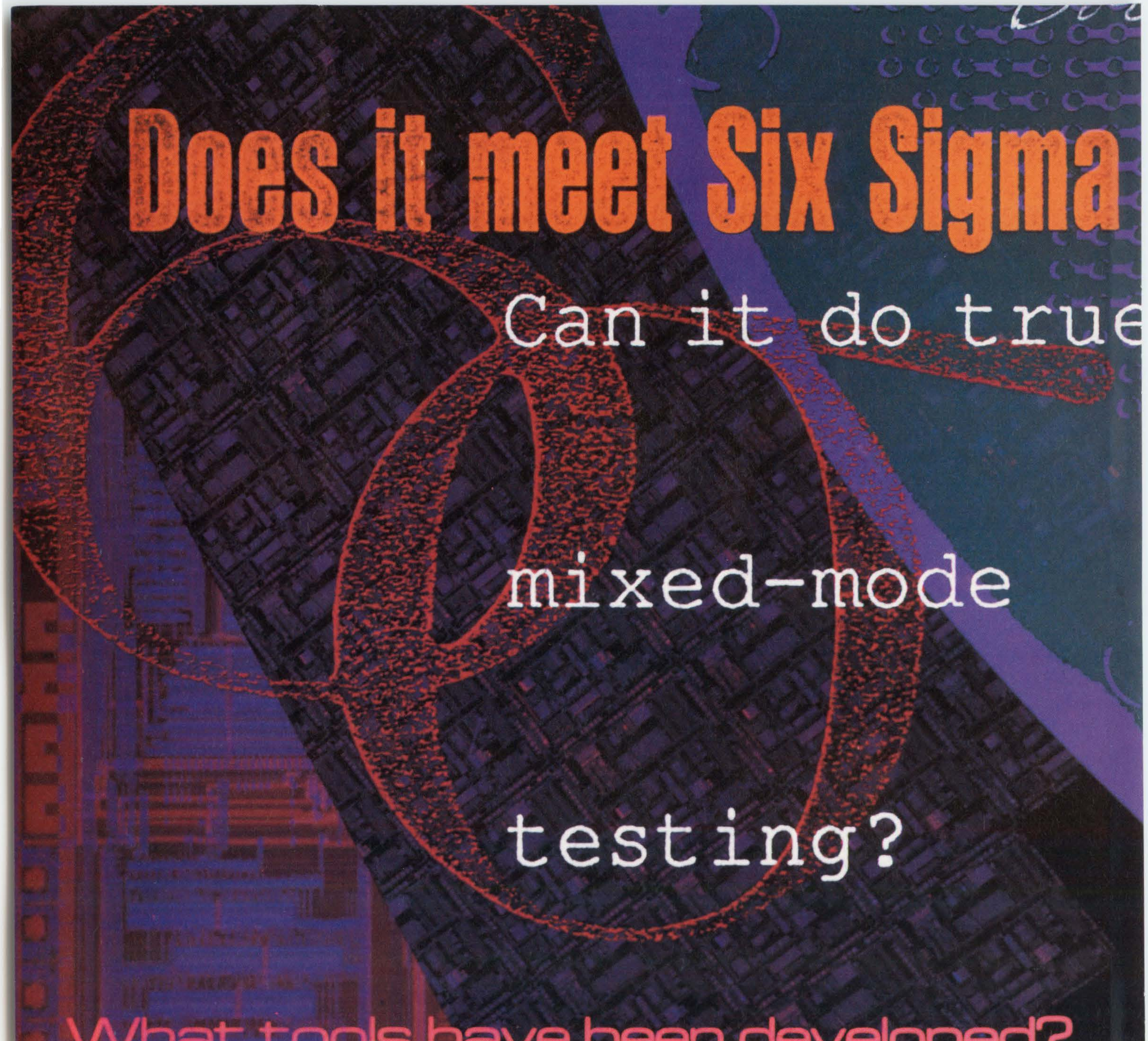

Before the A500 started testing Motorola's mixed-

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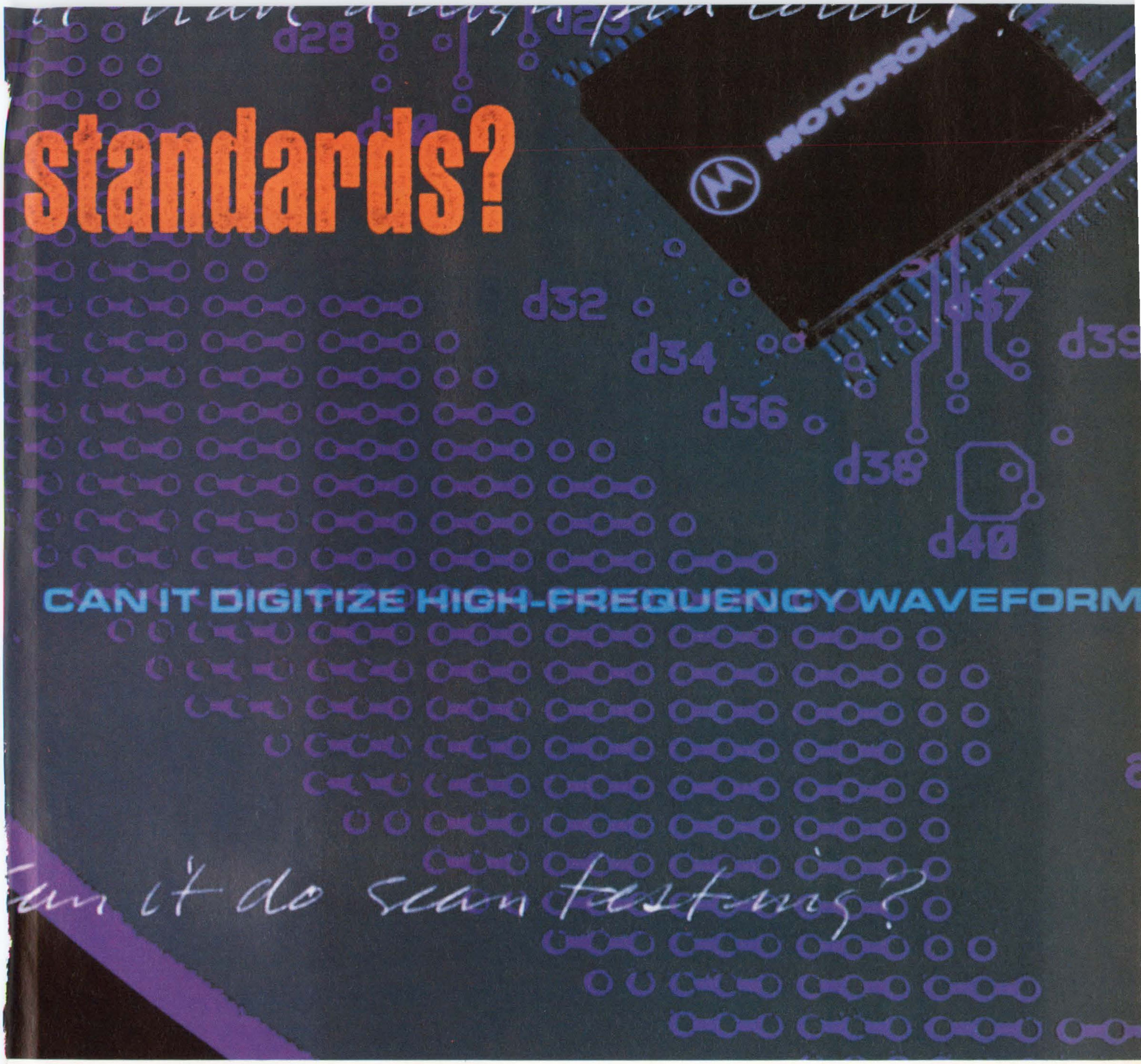

signal technology, Teradyne had to pass a few tests.

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SIGNALS & NOISE

How to obtain better performance

In Mark Stitt's article, "Boost instrument-amp CMR with common-mode-driven supplies" (EDN, October 25, 1990, pg 183), he illustrates the improvement possible by means of proper analog design, using composite amplifiers vs the limited specifications of modules.

Although Mark mentions the requirement that IC_4-IC_7 in Fig 2 have high speed to achieve the best results, capacitors C_1-C_2 cause a roll-off in the response of the $\pm 5V$ supply at 300 Hz. This action is also evident in Fig 4, where the CMR of the enhanced version is relatively flat at lower frequencies, has dropped -3 dB at 300 Hz, and begins rolling off at an initial -20 dB per decade. It would appear that even better performance could be obtained if the bandwidth of IC_6 and IC_7 were increased so as not to limit the bandwidth of IC_4 and IC_5.

Richard L Panosh
President
Vista Medical and Electronic Engineering
Lisle, IL

(The author's reply: In reply to Richard Panosh's letter, it is perhaps an unfortunate coincidence that the CMR of the boosted IA begins to roll off at about the same frequency that would be predicted by the RC time constant of C_1,R_7 and C_2,R_6 in the feedback of subregulator amplifiers, IC_6 and IC_7. Actually, the subregulator amplifiers are operating as unit-gain followers with feedback resistors to establish a $\pm 5V$ offset. The 0.01-μF capacitors, C_1 and C_2 in parallel with the 50 kΩ feedback resistors, are an arbitrary but adequate value to prevent gain peaking. Without C_1 and C_2, the feedback resistors would react with op-amp input capacitance and current-source output capacitance, causing excessive gain peaking. If anything, a larger value capacitor would improve high-frequency performance. The serious overdesigner might even be tempted to parallel the 0.01-μF ceramic capacitor with a 1-μF tantalum capacitor. Care must be exercised, however, to avoid excessive stray capacitance.

Richard is correct—faster is better for IC_6 and IC_7.)

Is garbage collection on Ada possible?

As an enthusiastic user of Ada and a consultant on Ada's use in real-time environments, I read Ben Brosgol's article on real-time Ada with great interest. Although Ada typically has a longer learning curve than more traditional approaches to real-time design, the use of Ada can pay off handsomely in more functional and reliable systems—especially in systems with a large amount of software.

I'm concerned, however, that Ben continues to perpetuate a view that was proven wrong 14 years ago. He contends (EDN, October 1, 1990, pg 107) that "automatic reclamation schemes suffer from unbounded execution times, which could cause your program to miss a critical deadline." I wrote a paper entitled "List Processing in Real Time on a Serial Computer" (*Communications of the Association of Computing Machinery*, April, 1978), which shows that it's possible to perform automatic garbage collection (reclamation) in such a way that the amount of time to allocate an object can be bounded by a time linearly proportional to the object's size, and that the constant of proportionality can be quite small. Because this scheme performs all of its work during allocation time, no additional time is required to reclaim storage outside of these allocation calls. Because the object must be initialized, and this initialization takes time at least proportional to the object's size, there's not much room for improvement in this algorithm.

This real-time garbage collector algorithm has received extensive testing as a result of its use in at least three commercial Lisp Machine products. Some file servers based on Lisp Machine technology have run 24 hours a day for months and years without garbage collection delays. Others have proposed substantial extensions to my work, including "generational garbage collection," which is currently the state of the art in garbage collection for Lisp, Smalltalk, and a number of other languages. Although not strictly real time, generational garbage collection is mostly incremental and is particularly well-suited to applications involving user interactions.

Garbage collection has therefore received a bad rap from those in the real-time and Ada communities. This obsolete view has severely hampered the widespread use of newer, highly productive software techniques, including object-oriented programming.

Henry G Baker, PhD
Nimble Computer Corp
Encino, CA

(The author's reply: I want to thank Henry Baker for calling attention to his algorithm for real-time garbage collection, because its bounded-time performance and its avoidance of heap fragmentation offer attractive benefits. His letter raises interesting questions: Can automatic garbage collection be implemented for Ada, and if so, would this be practical in real-time applications?

The answer to the first question is "Yes." Ada's strong typing enables the runtime executive to know the type, and thus the structure of each data object—an essential requirement for a garbage collector. Although compile implementors would need to consider interactions with tasking and exception handling, experience with previous languages such as Algol 68 has shown *the feasibility of garbage collection for languages with rich runtime semantics.*

The question, then, is not whether it's possible to implement garbage collection in an Ada runtime system, but whether such implementation will be applicable to real-time systems. Two principal issues arise, however:

1. How appropriate is the technique in programs where C-like or low-level features (address arithmetic, unchecked conversions, "hidden" pointers, representation clauses) are used? Real-time programs tend to require such features, but using them can render garbage collection unsafe or make it so conservative in its reclamation that its purpose is defeated.

2. What is the data space overhead? Henry's article in the CACM implies a doubling of the heap space requirements, in the absence of data compaction techniques that have a side effect of increasing execution time. In some environments this increase in space requirements may be tolerable, but in applications with tight storage constraints the overhead may be unacceptable.

In summary, although it was perhaps an oversimplification to state that "automatic reclamation schemes suffer from unbounded execution times," the applicability of garbage-collection strategies to real-time Ada programs remains an area where further work is needed. Meanwhile, programmers can reclaim storage via the various techniques described in the article—for example, explicit deallocation.)

Maintaining privacy of phone number

Joseph Gili (EDN, November 8, 1990) concisely sums up privacy rights in telephony as: (1) The right of one called to know who is calling; and (2) the right of a caller to keep his or her number private. He offers a good plan to protect both rights.

Another plan is: (1) Allow a caller to block transmission of his or her number to the one called; and (2) allow the one called to block incoming calls with the caller's number attached. With this plan, calls go through when both parties agree on the terms and are blocked when both parties don't agree. Simple, and elegant.

Quite frankly, I don't want anyone, friend or foe, to be able to access my number unless I can also access his or hers.

Wesley Mansfield
President
Tennsoft Inc
Dunlap, TN

Speaking Polish not an open door to closing deals

In his editorial (EDN, August 2, 1990, pg 47), Gary Legg is absolutely right in saying that "facts don't always tell the truth" when making comparisons about Poland.

As a Pole raised and educated in the US, returning to Poland twice this year has been eye opening. The quality of life is better in Poland today than it was 14 years ago when I worked there temporarily. Opportunities are enormous and widespread, yet enterprises are waiting to be rescued by Western businesses. The lifestyle, although cramped in many ways, is refreshing. As an international procurement and marketing manager, I find Poland an easily misunderstood quagmire.

I am working with Polish individuals and private, institutional, and public organizations of all sizes. A concerted effort has been made in the development of business within the electronics arena both in hardware and software. Making comparisons is fraught not only with the hazards of misconception but is usually misleading and downright erroneous. As an example, Gary cites simple wage rates and gives three examples of $75, $100,


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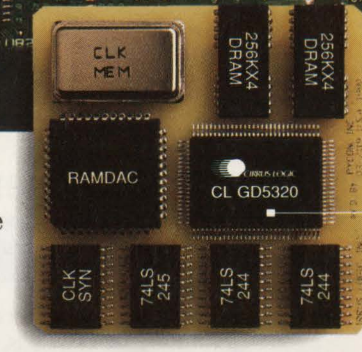
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SIGNALS & NOISE

and $125 a month; in fact, the American businessman should be prepared to pay upwards of $400 a month. Still inexpensive, but a big difference.

Even more important is the need for expertise on doing business with Polish individuals and companies. I have worked with the Japanese for 15 years and consider it much more difficult to deal with Poles, even though I'm a "near native" speaker of the Polish language. Determining who knows what and how to get something accomplished in Poland is an immense problem.

Having said all that, and with more to say about the problems of doing business in Poland, I remain very optimistic. I was involved in Japan and Taiwan in the mid 1970's and agree that Poland has more to offer in the 1990's than was available in Asia only 15 years ago.

Chris J Gniewosz
Chrisco Trading
Portland, OR

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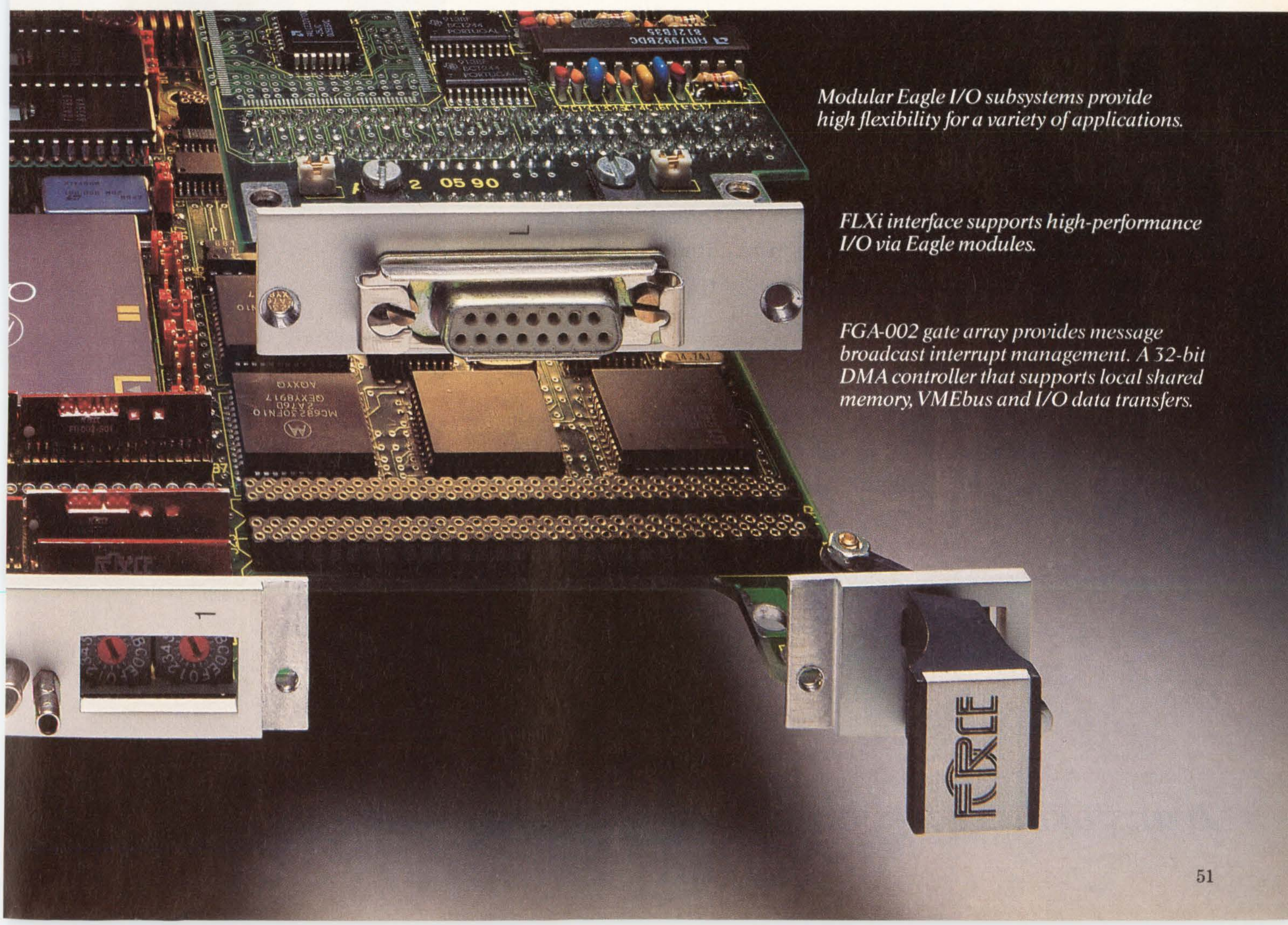

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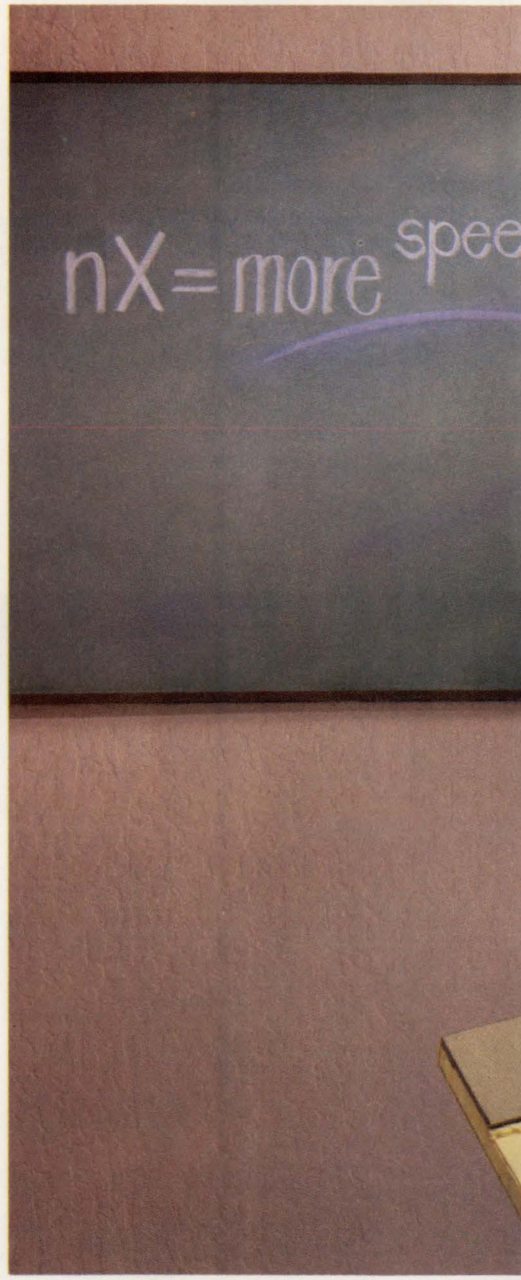

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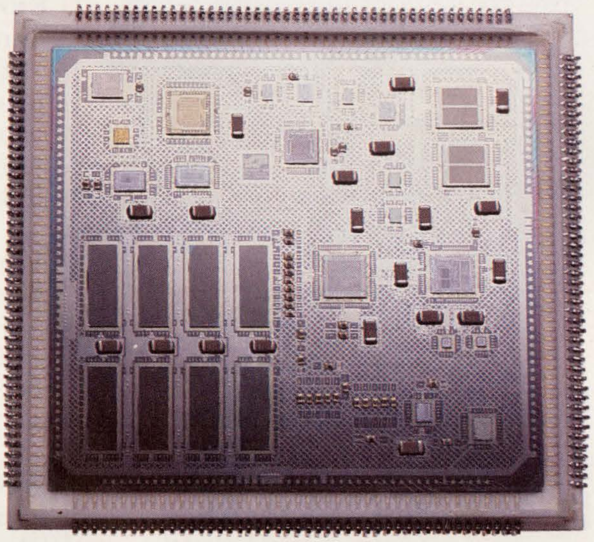

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Applications of UNIX Utilities (short course), Seattle, WA. Specialized Systems Consultants Inc (SSC), Box 55549, Seattle, WA 98155. (206) 527-3385. FAX (206) 527-2806. February 26.

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SQL (Structured Query Language): A Hands-On Workshop, Seattle, WA. Learning Tree International, Box 45028, Los Angeles, CA 90045. (800) 421-8166; in Canada, (800) 267-1824; in CA, (213) 417-9700. March 12 to 15.

Advanced Research in VLSI Conference, University of California, Santa Cruz, CA. Kevin Karplus or Jean McKnight, Computer Engineering, UCSC, Santa Cruz, CA 95064. (408) 459-2303. March 25 to 27.

National Telesystems Conference, Atlanta, GA. IEEE's Aerospace and Electronic Systems Section, Scott Wood, Scientific-Atlanta, 4388 Shackleford Rd, Norcross, GA 30093. (404) 925-6377. March 26 to 27.

VHDL Conference, Cincinnati, OH. VHDL User Group, Randy Harr, 3145 Geary Blvd, Suite 123, San Francisco, CA 94118. (408) 984-5952. FAX (408) 984-6723. April 8 to 10.

National Electronic Manufacturing and Design Expo, Chicago, IL. Amy Riemer, Cahners Exposition Group, Box 3833, Stamford, CT 06905. (203) 352-8292. April 8 to 11.

1991 International Reliability Physics Symposium, Las Vegas, NV. IEEE IRPS, SAR Associates, Box 308, Westmoreland, NY 13490. (315) 339-3971. FAX (315) 336-9134. April 8 to 11.

Electro/International, New York, NY. Electronic Conventions Management, Electro/International, 8110 Airport Blvd, Los Angeles, CA 90045. (800) 877-2668. FAX (213) 641-5117. April 16 to 18.

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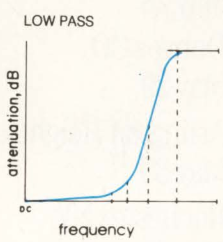
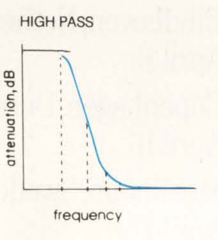


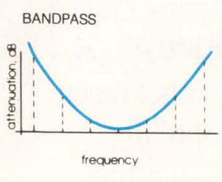
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



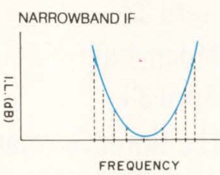
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz (loss <1dB) Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	STOP BAND, MHz (loss > 10 dB) Max. F4	STOP BAND, MHz (loss > 20 dB) Min. F5	STOP BAND, MHz (loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	STOP BAND, MHz I.L. > 20dB F6	STOP BAND, MHz I.L. > 35dB F7	STOP BAND, MHz I.L. > 35dB F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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F132-2 REV. ORIG.

Here's where the barricades start to come down in the mixed signal revolution.

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March 18

Cleveland, OH
March 19

Pittsburgh, PA
March 20

Atlanta, GA
March 25

Clearwater, FL
March 26

Orlando, FL
March 27

Huntsville, AL
March 28

Waltham, MA
April 1

Saddlebrook, NJ
April 2

Westchester, NY
April 3

Smithtown, NY
April 4

Cromwell, CT
April 5

Santa Clara, CA
April 8

Costa Mesa, CA
April 9

Los Angeles, CA
April 10

Woodland Hills, CA
April 11

San Diego, CA
April 12

McLean, VA
May 6

Baltimore, MD
May 7

Cherry Hill, NJ
May 8

Fort Washington, PA
May 9

Raleigh, NC
May 10

Toronto, Canada
May 13

Santa Clara, CA
May 14

Pleasanton, CA
May 15

Bellevue, WA
May 16

Beaverton, OR
May 17

Woburn, MA
May 20

Montreal, Canada
May 21

Bloomington, MN
May 22

Houston, TX
May 23

Dallas, TX
May 24

Phoenix, AZ
May 28

Denver, CO
May 29

Arlington Heights, IL
May 30

Rochester, NY
May 31

International Locations & Dates

Eindhoven, Netherlands
April 15

Copenhagen, Denmark
April 16

Stockholm, Sweden
April 17

Lyons, France
April 18

Paris, France
April 19

Rome, Italy
April 22

Milan, Italy
April 23

Hannover, Germany
April 24

Frankfurt, Germany
April 25

Munich, Germany
April 26

Birmingham, England
April 29

London, England
April 30

Vienna, Austria
May 2

Zurich, Switzerland
May 3

Seoul, Korea
June 3

Seoul, Korea
June 4

Taipei, Taiwan
June 5

Taipei, Taiwan
June 6

Hong Kong
June 7

Tokyo, Japan
June 10

Tokyo, Japan
June 11

Osaka, Japan
June 12

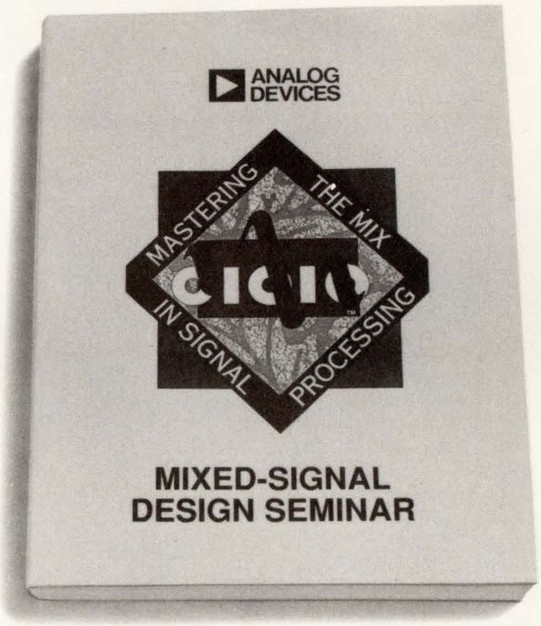
Osaka, Japan
June 13

Nagoya, Japan
June 14

Not too long ago, digital designers didn't need to know about analog. And the analog guys didn't need to worry about digital.

But with the revolution that's happening in mixed signal technology, that's far from true anymore.

You see, mixed signal technology is the only way to break down the barriers to higher levels of system integration, better performance, and faster time to market. And it accomplishes these difficult tasks by combining both signals on a single chip.



As the leader in mixed signal technology, Analog Devices has the most experience in assisting both analog and digital designers in applying it to their systems.

Which is why every designer from both camps should attend our Mixed Signal Design Seminar.

For example, in this comprehensive full-day seminar we'll cover such things as digital signal processing, interfacing converters to DSP, analog signal conditioning, digital and analog filtering, sigma delta converters, sampled data systems, and practical techniques for building a better board.

In short, you'll leave this seminar with a better idea of how to put mixed signal technology to work for you in a broader range of applications. And you'll leave with a design handbook, the industry's largest SPICE macromodel library, and more.

Admission is just $20, and includes all materials and lunch, but you must pre-register.

The mixed signal revolution has started, so make sure nothing stops you from attending this seminar. To reserve your space, return the coupon. For more information or to charge your ticket, call (617) 937-1430 or (800) 262-5643.

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ANALOG DEVICES

EDITORIAL

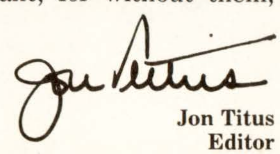
Save that technojunk!

Recently I looked through a local want-ad publication and was surprised at the old electronic and computer equipment that people are selling. Much of that equipment is obsolete and of little use, but some of it represents milestones in our technical past. It's sad to see it selling so cheaply and viewed as having so little value. I'm not talking about Nintendo games and citizen-band radios. At least in this part of the US, sellers offer older minicomputers, µP development systems, and test equipment.

It's easy to get caught up in the push for newer and better equipment and to declare older equipment obsolete. Most of the electronic companies I've dealt with have a shelf of such older equipment. The engineers can't decide whether to keep it for parts or to scrap it. Often when someone needs a power supply, a µP board, a display, or other component, they'll remove it from the old gear they have at hand. Slowly, more and more components are stripped out of the old equipment, leaving skeletons that end up in a dumpster. All too often we're destroying the history of electronics, perhaps because that "old" equipment is still too new to be viewed as historic. I don't know of anyone who would strip a hand-made brass microscope from the 1880s to get a brass tube, or anyone who would tear an old coil out of an antique Atwater-Kent radio. Unfortunately, that's what many of us are doing with our old electronic equipment.

Several years ago, a fellow I knew uncovered some old Philbrick operational amplifiers in his lab. To his dismay, he found they used vacuum tubes and high voltages, so they were of no use to him. These unused devices in brand-new boxes went into the trash. I salvaged all of them, saved a couple and gave others to friends who appreciated their historical significance. By casually throwing out old equipment and components, we start losing the artifacts of electrical and electronics history—I'm sure that many younger engineers think the 741 IC was the first op amp. Old devices, like the Philbrick op amps, are just the things that put today's technologies in perspective and relate them to past developments.

The Computer Museum in Boston and the Smithsonian Institution in Washington, DC have displays that provide a history of computers and information systems. They provide homes for some older equipment and a starting place for electronic history. But we need a broader display of electronic technology, its roots, its development, and the devices and products that embody the technology. Without such a repository for information and devices, we'll lose an appreciation for early developments, and we won't have a place where people can see what engineers have devised over the years. Although museums are slowly beginning to offer such exhibits, we may still be too close to the early days of electronics to provoke interest in a museum of electronic technology. So, in the meantime, take a look in your bin of old equipment. You may have some antiques that are worth preserving—even if they never reach a museum. You've got an Intel 8008 development system with a 1702A PROM programmer? Well, dust it off and keep the scroungers from snatching its toggle switches. Someday you'll be able to point to it and brag, "I remember the days when...." History and the artifacts that go with it are important, for without them, history becomes rumor.

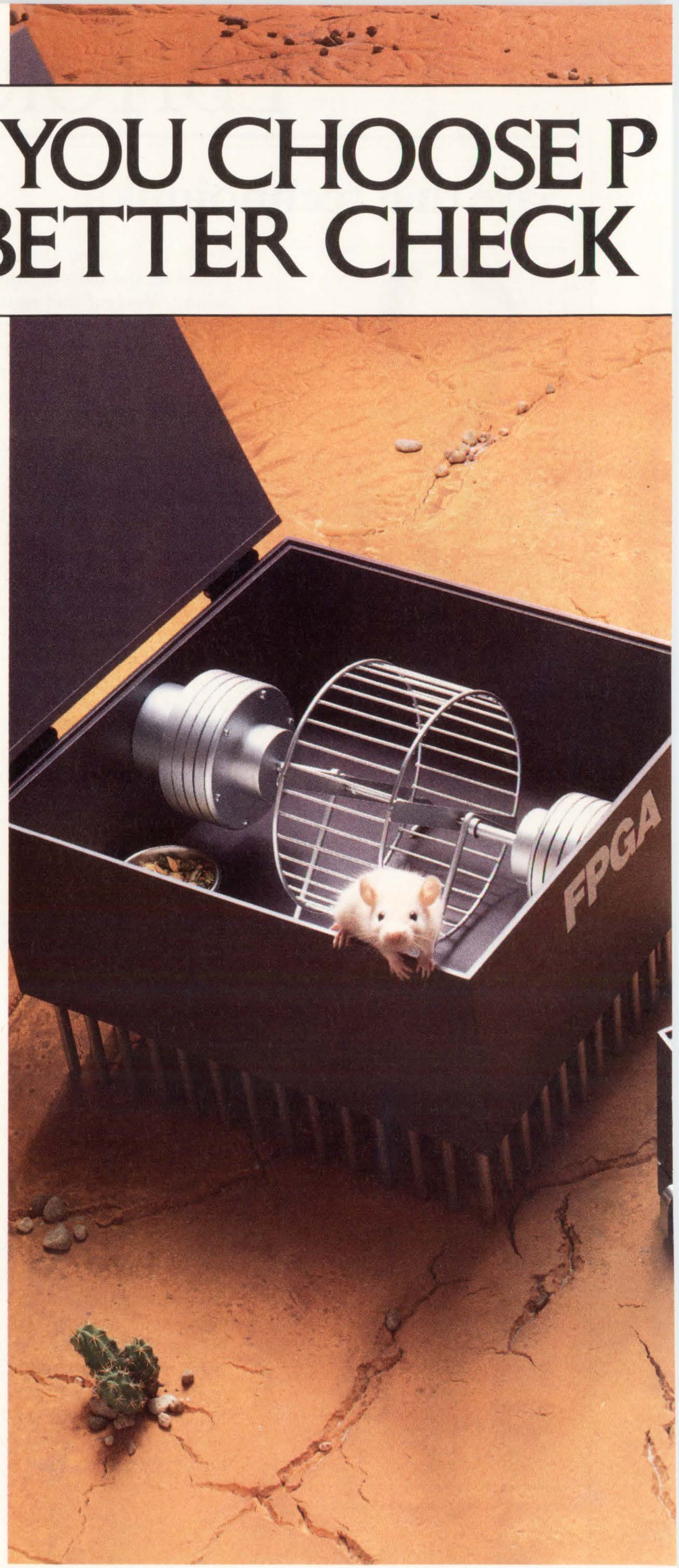


Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

BEFORE YOU CHOOSE P
BETTER CHECK



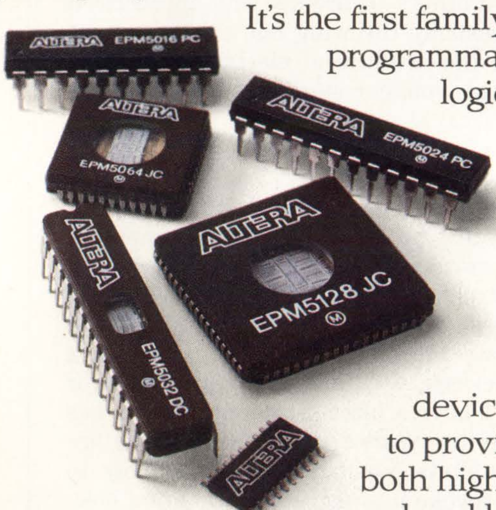
Things aren't always what they seem.

Some people would have you believe FPGAs are faster and denser than MAX™ EPLDs.

Funny how they never mention *in-system* performance, though. When they talk about speed, they quote 100MHz flip-flop toggle rates. When they talk about density, they recite raw gate counts.

Which could make your high-performance design highly disappointing.

But if you want to do more than just spin your wheels, consider MAX. It's the first family of programmable logic



devices to provide both high speed and high logic density where it counts. At the system level.

Which means MAX can handle just about all your logic needs. In fact, a single 64-macrocell EPM5064

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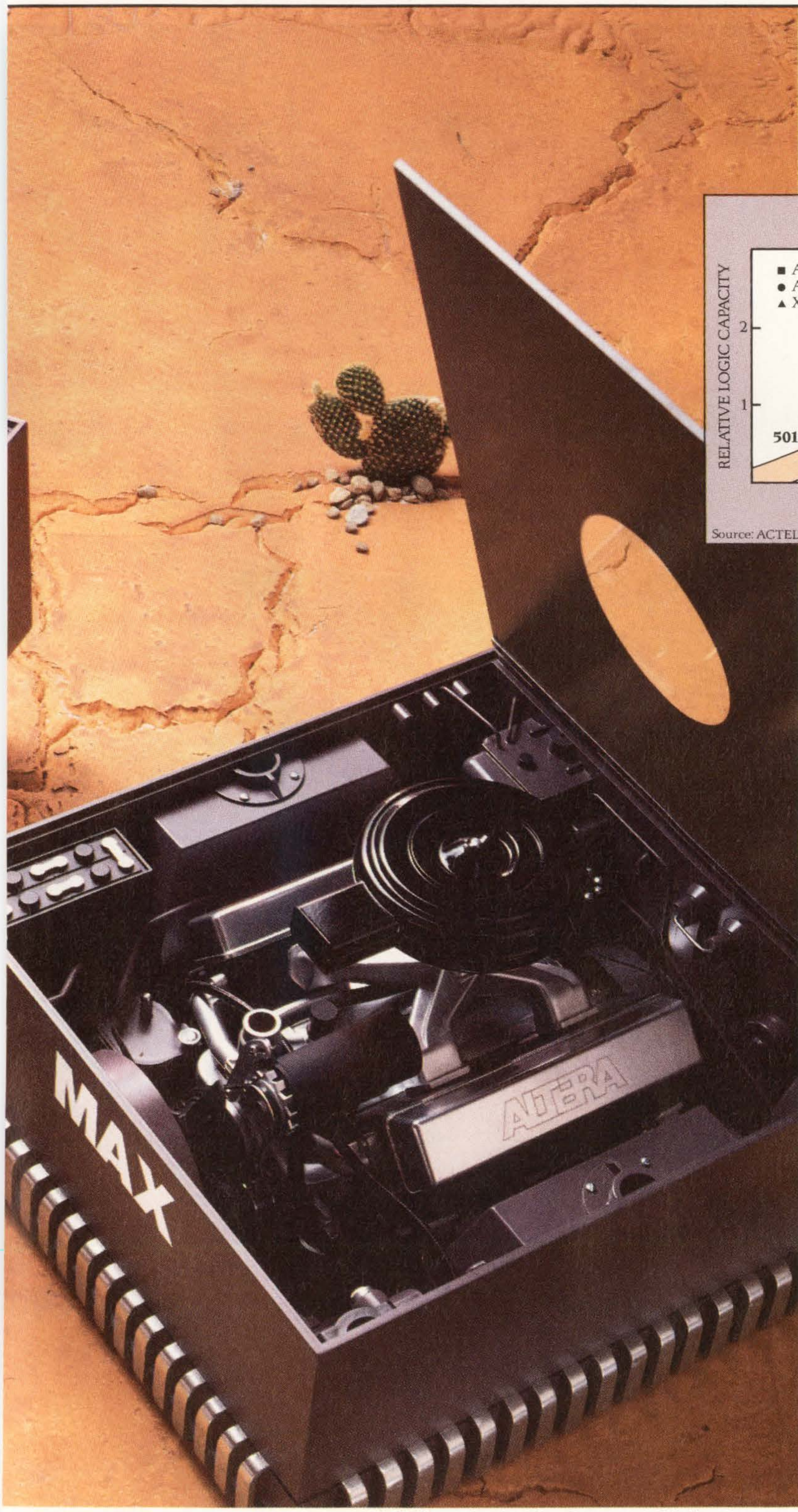
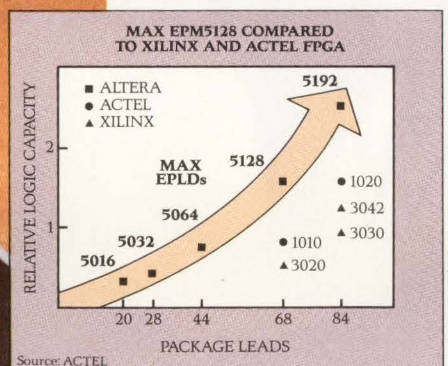


can integrate anything from simple system glue logic right up to complex graphics coprocessors and LAN and memory controllers.



Or take the 68-pin MAX EPM5128. It's up to 50% faster and 100% denser than comparable FPGAs, thanks to its high-performance architecture and superior logic routability. But don't take our word for it—just take a look at the competition's benchmarks.

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For years Seagate has been best-known as the volume producer of disc storage products. But our reputation as solely a manufacturing powerhouse is beginning to change.

H N O L O G Y

In the past several months Seagate has received three Disc Drive Supplier of the Year awards from some of our valued OEM customers. In every case, the commendations have been earned not just for supplying quality products, but for providing superior customer service.

ICL, Britain's leading information technology company, honored us with their Vendor Award Citation for being responsive to their flexibility of delivery and cost of ownership requirements. In addition, our Wren drives exceeded their stringent reliability and "plug-and-play" criteria.

Olivetti, the Italian computer company, awarded us their Quality Award for Customer Satisfaction for the same reasons. By meeting Just-in-Time delivery schedules, listening to the customer, exchanging data from the field and providing training and support, we have helped Olivetti provide superior products and service to their customers.

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So while Seagate is still the first name in disc drives, we're making quite a name for ourselves in quality and customer service, as well. To learn more about the benefits of a partnership with Seagate, call us at 800-468-DISC, or 408-438-6550.

And to our customers, we offer a couple of choice words of our own: Thank you.

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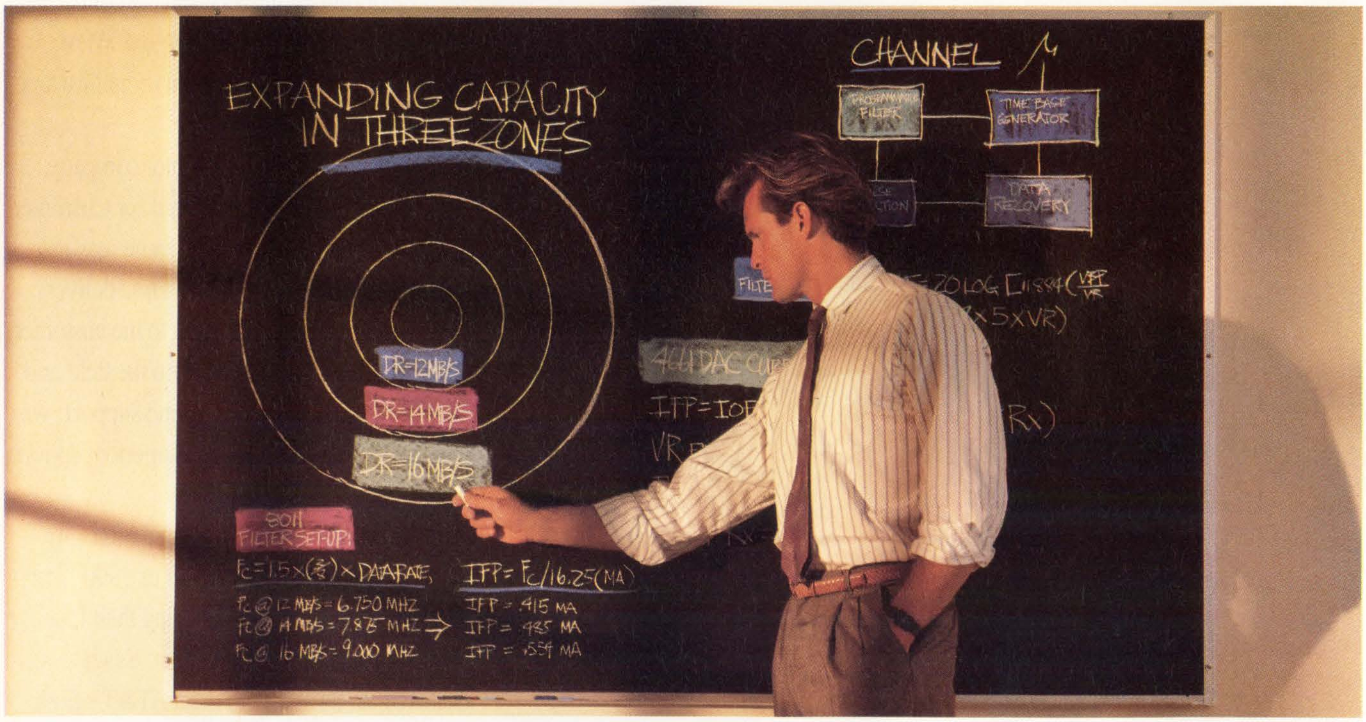
The first name in disc drives

The universe is expanding.



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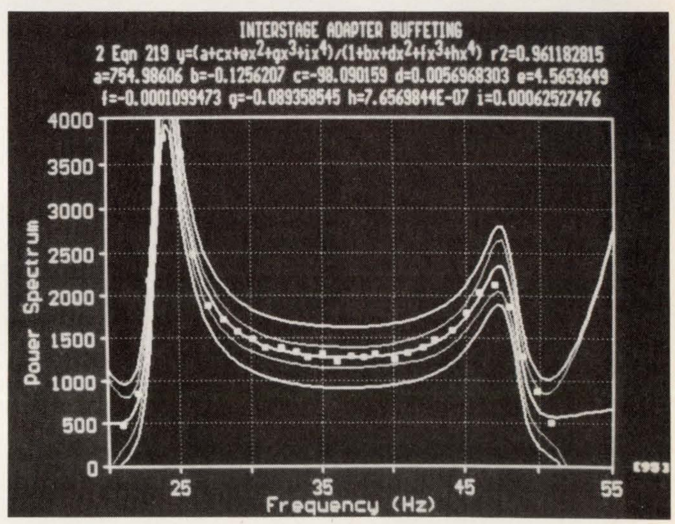
Dan Strassberg, Associate Editor

Like the ancient mariner surrounded by water with not a drop to drink, engineers often feel cast adrift in a sea of experimental data with not a point that makes sense. When such a situation leaves you feeling lost, a personal computer or workstation equipped with graphing software and a plotter or graphics-capable printer can act as your compass, your rudder, and your engine. By helping you make sense of the data you've gathered, these tools can empower you to set a true course toward solving your problem.

Graphs, 3-D displays, and contour plots are only the beginning of a long list of visualization aids that can show you relationships among variables that columns of figures never can. (In a family of contour plots, each contour line shows the combinations of a pair of variables for which a third variable achieves a specified value.)

Many of the software packages listed in **Table 1** perform such functions as automatic curve fitting, in which the software finds an equation that closely matches a set of experimental data points. Different equations can describe different regions of the data. Some packages, such as The Math Works's Spline Toolbox, perform "spline" fits. The software selects regional boundaries so that curves connect to one another without discontinuities. Often, the software will let you try different forms of equations, so you can see how closely you can get the curves to fit the data.

Animation is beginning to play a role in data interpretation. Personal computers, long a mainstay in data acquisition, are gaining in speed and power and in their ability to display pictures. Workstations, which are even more powerful than PCs, are finding increasing use in experiment control. Experimenters' use of this fast, powerful hardware is encouraging software designers to find new ways of processing experimental data to make it more meaningful. One result is a class of products called visualization packages, some of which produce animated high-resolution displays.



Color-plotting families of curves *in two dimensions on a single set of axes is a capability of many graphing packages, such as Jandel's Tablecurve. The middle curve results from discrete experimental data points. The software fitted a smooth curve to the data. The curve consists of several segments; a different equation describes each segment.*

Graphing and curve-fitting software

Temperature testing an automobile engine shows how you could use a visualization package. Thermocouples buried at many points in the engine block record temperatures. Data-acquisition software gathers the thermal data and puts it in a file on disk. Visualization software can present a 3-D picture of the engine block. It can read the file of temperature data and, through color or shading, depict isothermal (equal-temperature) surfaces within the block. These surfaces move as a function of engine speed, load, and time. Sequences of images presented in rapid succession show this movement. With such animated displays, experimental results take on an instant meaning that tables of readings and even 2-D plots cannot convey.

Visualization packages that can produce animated displays are not

Table 1—Representative graphing, curve-fitting, and visualization software packages

Vendor	Package	Computer system[1]	US list price	Key features, comments
Advanced Graphics Software	Slidewrite Plus V4.0	IBM PC	$445	Includes four custom scientific figure libraries.
Advanced Micro Solutions	Segs V2.0	IBM PC	$50 to $200	2-D plots. Reads ASCII and 1-2-3 files.
Amtec Engineering	Tecplot V4.0	IBM PC/AT	$649	Reads ASCII files. Displays multiple 2- and 3-D plots. Makes contour plots.
		Workstations	$1695	
BBN Software Products	RS/1 V4.2	IBM PC/AT (math coprocessor helpful)	$2000	Scatter plots, histograms, bar charts, X-Y and 3-D graphs. Data analysis, statistics, and curve fitting.
Binary Engineering	Tech*Graph*Pad V4.0	IBM PC, workstations	$395	Reads ASCII and 1-2-3 files. Makes eight plot types. Smoothes data. Fits curves.
BV Engineering	Grafmaker V1.0	IBM PC	$195	Reads ASCII files. Mixes graph types. Axes can be log or linear.
Caren Co	Mathgraph 11/90	IBM PC	$695	Reads ASCII files. Cracks unknown binary files. Makes 2- and 3-D plots, contour and surface plots. Smooths data. Fits curves.
		DEC 3100, 5000, VAX	$1400	
		Cray	$10,000	
Damaskos	Di-Graph V1.03	IBM PC	$144.95, $194.95 (with source code)	Makes 2- and 3-D plots, contour and polar plots, and Smith charts. Graphs algebraic and trig functions. Source code is in Quickbasic.
DSP Development	Dadisp	IBM PC, workstations	$895 to $6995	Post-acquisition data manipulation and display.
Dynacomp	PC Graphics	IBM PC	$49.95	3-D module, $19.95. Specializes in function graphing.
Golden Software	Grapher V1.79	IBM PC	$199	Makes 2-D plots. Reads ASCII files.
	Surfer V4.15	IBM PC	$499	Makes 3-D and contour plots. Reads ASCII and 1-2-3 files.
Heartland Software	Ugraph V3.00	IBM PC	$395	Handles many file formats. Makes 2- and 3-D plots.
Island Products	Nfit V1.1	IBM PC	$89.50	General-purpose nonlinear curve fitting.
Jandel Scientific	Sigmaplot V4.0	IBM PC	$495	Eight plot types. Smoothing curve fitting, regression, statistics. Imports ASCII, DIF, and 1-2-3 files.
	Tablecurve V2.11	IBM PC	$395	Automated curve fitting. Graphing. Reads binary, dBase, ASCII, and 1-2-3 files.
	Peakfit V2.0	IBM PC	$595	Separates and analyzes multiple peaks in data.
The Math Works	Spline Toolbox	IBM PC with math processor, workstations	$295	Requires Matlab (from $695, depending on computer). Fits curves to data using piecewise polynomials. Lets you build splines.
Micromath Scientific Software	Graph V2.02	IBM PC	$149	Scientific plotting, data transformation. Reads ASCII files. Simple curve fitting.
	Minsq V3.12	IBM PC	$249	Nonlinear curve fitting. Model development.

Notes: 1. As used here, the term IBM PC refers to personal computers based on any member of the 80x86 family of processors. These PCs are compatible with the original IBM PC. Software runs under MS-DOS. IBM PC/AT refers to computers based on 80286, i386 and i486 processors and that are compatible with the original IBM PC/AT. A listing of OS/2 indicates that the software runs under that operating system; obviously the computer must support OS/2.

2. Price is for single floating license. Academic discount lowers price. Licenses that permit multiple users on a network also lower the price per user.

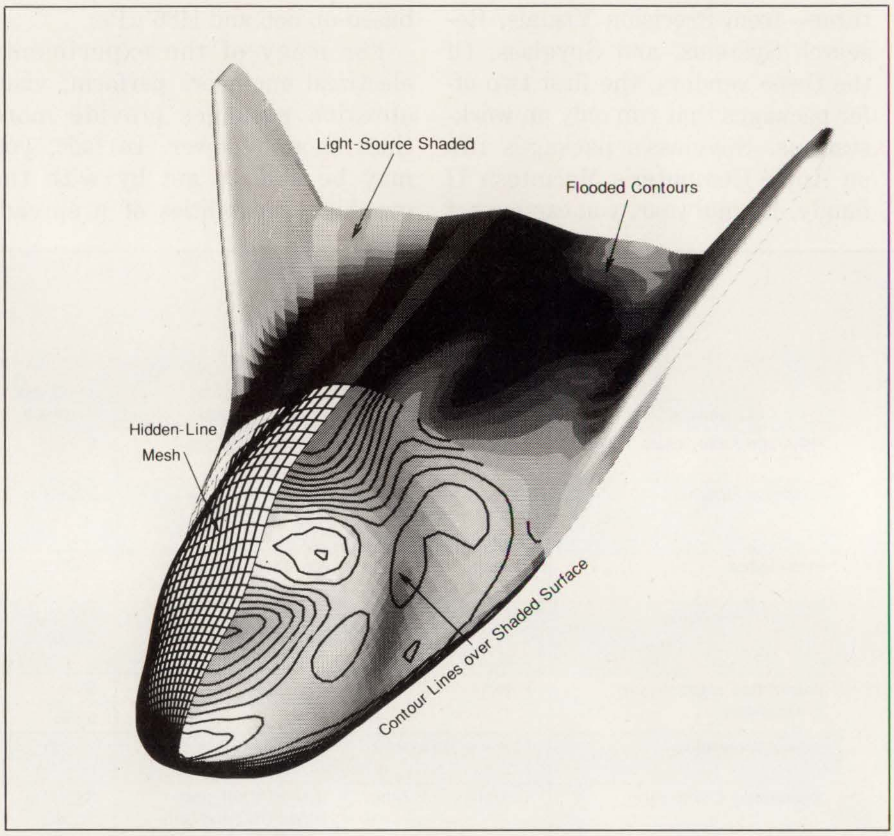
yet numerous. **Table 1** lists just three—from Precision Visuals, Research Systems, and Spyglass. Of the three vendors, the first two offer packages that run only on workstations. Spyglass's packages run on Apple Computer's Macintosh II family. By mid year, you can expect a visualization package for PCs based on 386 and i486 μPs.

For many of the experiments electrical engineers perform, visualization packages provide more than enough power. In fact, you may be able to get by with the graphing capabilities of a spreadsheet program. As **Ref 1** points out, though, most spreadsheets are tailored to business applications. They excel at producing bar and pie charts, but most can't create surface or contour plots. Few spreadsheets can show the limits of a range of data obtained from re-

Vendor	Package	Computer system[1]	US list price	Key features, comments
Mihalisin Associates	Temple-Graph V2.4	Sun workstations	$1290[2]	Graphing and data analysis. Templego, which does graphing only, costs $500.
Precision Visuals	PV-Wave (point-and-click version)	Sun workstations	$2500	2- and 3-D visualization and data analysis. Animated displays. Can read files in many formats without advance information about the format.
Prescience	Theorist V1.1	Macintosh (all types)	$399.95	Reads tab-and return-delimited ASCII files and anything from the clipboard.
Research Systems	IDL V2.0.11	Five vendors' workstations	$2200 to $9000	Generalized data reduction, analysis, visualization, and image processing. Reads binary and formatted data.
Scientific Programming Enterprises	Plot-It	IBM PC/AT	$195	2- and 3-D graphs (60 types). Linear and nonlinear regression analysis.
		OS/2	$295	
Signal Technology	N!Power Base V1.0	DEC and Sun workstations	$6000	Graphing and analysis. Reads ASCII and binary files and files from the vendor's ILS package.
Speakeasy Computing	Graph-easy V Zeta	IBM PS/2, RT, and RISC; DEC and Sun workstations	$2000 to $5000	Graphics component of numerical solution package called Speakeasy.
Spiral Software	Easyplot V II	IBM PC	$349	2- and 3-D plotting and data analysis. Zoom and scroll.
Spyglass	Spyglass Transform	Macintosh II	$395	Data visualization. Reads ASCII files. Creates color, interpolated, and polar images and line graphs.
	Spyglass View	Macintosh II	$395	Usable as companion to Spyglass Transform. Creates surface and contour plots and cross sections.
Statsoft	CSS: Graphics	IBM PC OS/2	$495	2-, 3-, and 4-D graphing; data analysis. Vendor has a statistical package (CSS/3, $595). CSS: Statistica combines the two ($795).
Synergy Software	Kaleido-Graph V2.1	Macintosh	$249	16 plot types. High-speed curve fitting.
Systat	Systat V5.0	IBM PC	$895	Includes all functions of Sygraph, a stand-alone graphing package: contour plots, nonlinear scatter-plot smoothing, and dimensional maps.
	Mac Systat V5.0	Macintosh		
Triakis	Dan V1.2	Sun SPARCstations	$395	Inputs and outputs in several file formats. Manipulates data tables in memory. Makes X-Y plots.
	Dan V2.0	Next		
TriMetrix	Axum V1.02	IBM PC	$495	Imports ASCII, 1-2-3, and dBase files. Creates 2- and 3-D plots, contour plots, and Smith charts.
Wavemetrics	Igor V1.24	Macintosh (all types)	$295	2-D graphing, curve fitting, data analysis. Macro language lets you automate functions such as peak analysis without additional software. Imports ASCII files (space, comma, and tab delimited); Excel and binary files.
3-D Visions	Graftool V3.3	IBM PC	$495	2- and 3-D graphing and data analysis. Reads ASCII, DIF and 1-2-3 (WKS and WK1) files.

peated trials of an experiment while plotting a single curve through the scattered points. Usually, curve fitting with a spreadsheet program involves entering equations and making repeated trials. You may not think of this exercise as programming, but it really is.

So, if you're serious about using a computer to produce plots and graphs of experimental data, you'll want one or more packages that perform the same functions as the graphing, curve-fitting, and visualization software packages in **Table 1**. Despite its length, the **table** probably omits more packages with graphing and plotting capabilities than it includes. For example, many data-acquisition packages contain graphing and plotting routines, some of which are quite advanced. Such software isn't included, nor are libraries of graphing and plotting routines that you can call from your own high-level-language programs.



Three-dimensional displays *take many forms, several of which appear in this illustration created with Amtec's Tecplot. Shown are a surface described by a mesh, shaded surfaces with and without contour lines, and a surface with flooded contours.*

Selection requires savvy

With such an array of choices, how do you select one package (or a small number of packages) well suited to your needs? The flippant answer, of course, is "very carefully." **Table 1** and the list of vendors in the **box**, "For more information . . . " are, at best, just starting points for your search. A few of the factors you should consider and questions you should ask are

☑ Are you going to use the software daily or only occasionally? User interfaces with pull-down menus can make occasional use of a package pleasant but may make frequent use exasperating. For this reason, some packages with pull-down menus have a "hidden" command-driven interface to speed operation for experienced users. If you do not use a mouse or pointing device, is the operation of the software acceptable without one?

☑ Create a list of the functions you want a package to perform. If possible, obtain a functional, interactive demonstration version of the software and spend enough time with it to assure yourself that it satisfies you in its performance of the functions you desire. Make sure the software operates fast enough on the computer you will actually use.

☑ Will the program read data from files in a format your data-acquisition software can produce? For example, most packages claim to read ASCII files, but ASCII is hardly a complete specification for a file containing a data table. What characters does the software accept as delimiters between entries—commas, carriage returns, tab characters? If you are plotting several dependent (Y) variables versus a single independent (X) variable, must the table repeat the X values for each set of Y values? If your X values are not always equally spaced, make sure the software still accepts them.

☑ Many packages read spreadsheet files in Lotus WKS or WK1 formats. A few packages claim to "crack" unknown ASCII and binary file formats. If you need this capability, test it by asking the software to read a file of the type you want it to accept.

☑ How large are the data sets the program can handle? If your data consists of more points than the program can read into memory at one time, you can prob-

Text continued on pg 76

For more information . . .

For more information on the graphing, curve-fitting, and visualization software packages discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

You can download a machine-readable version of this list from the EDN computer bulletin-board system (BBS). The downloadable list includes a larger number of companies than appear here. Some of the additional firms' products did not fit within the product category as defined in this article. Other companies failed to respond to our request for information. You can reach the EDN BBS at (617) 558-4241 (300, 1200, 2400, 8,N,1, 24 hours, 7 days). Look for file #TU260 in the /freeware SIG.

Advanced Graphics Software Inc
333 W Maude Ave
Suite 105
Sunnyvale, CA 94086
(408) 749-8620
FAX (408) 749-0511
Circle No. 700

Advanced Micro Solutions Inc
3817 Windover Dr
Edmond, OK 73013
(405) 340-0697
FAX (405) 749-0594
Circle No. 701

Amtec Engineering Inc
Box 3633
Bellevue, WA 98009
(206) 827-3304
FAX (206) 827-3989
Circle No. 702

BBN Software Products Corp
10 Fawcett St
Cambridge, MA 02138
(617) 873-6000
FAX (617) 873-3315
Circle No. 703

Binary Engineering Inc
400 Fifth Ave
Waltham, MA 02154
(617) 890-1812
FAX (617) 890-1340
Circle No. 704

BV Engineering
2023 Chicago Ave
Suite B-13
Riverside, CA 92057
(714) 781-0252
FAX (714) 781-0626
Circle No. 705

Caren Co
12137 Midway Dr
Tracy, CA 92507
(209) 835-0295
Circle No. 706

Damaskos Inc
Box 469
Concordville, PA 19331
(215) 358-0200
FAX (215) 558-1019
Circle No. 707

DSP Development Corp
1 Kendall Sq
Cambridge, MA 02139
(617) 577-1133
FAX (617) 577-8211
Circle No. 708

Dynacomp Inc
178 Philips Rd
Webster, NY 14580
(716) 265-4040
Circle No. 709

Golden Software Inc
Box 281
Golden, CO 80401
(800) 333-1021;
in CO, (303) 279-1021
FAX (303) 279-0909
Circle No. 710

Heartland Software Inc
234 S Franklin
Ames, IA 50010
(515) 292-8216
FAX (515) 292-8216
Circle No. 711

Island Products
Box 253, Station 1
Galveston, TX 77550
(800) 342-4681;
in TX, (409) 761-2463
FAX (409) 761-6424
Circle No. 712

Jandel Scientific
65 Koch Rd
Corte Madera, CA 94925
(800) 874-1888;
in CA, (415) 924-8640
FAX (415) 924-2850
Circle No. 713

The Math Works Inc
21 Eliot St
South Natick, MA 01760
(508) 653-1415
FAX (508) 653-2997
Circle No. 714

Micromath Scientific Software
2034 E Fort Union Blvd
Salt Lake City, UT 84121
(801) 943-0290
FAX (801) 943-0299
Circle No. 715

Mihalisin Associates
600 Honey Run Rd
Ambler, PA 19002
(215) 646-3814
FAX (215) 643-4896
Circle No. 716

Precision Visuals Inc
6260 Lookout Rd
Boulder, CO 80301
(303) 530-9000
FAX (303) 530-9329
Circle No. 717

Prescience Corp
814 Castro St, Suite 106
San Francisco, CA 94114
(415) 543-2252
FAX (415) 882-0530
Circle No. 718

Research Systems Inc
777 29th St, Suite 302
Boulder, CO 80303
(303) 786-9900
FAX (303) 786-9909
Circle No. 719

Scientific Programming Enterprises
Box 669
Haslett, MI 48840
(517) 339-9859
FAX (517) 339-4376
Circle No. 720

Signal Technology Inc
Box 1950
Goleta, CA 93116
(805) 968-3000
FAX (805) 967-0871
Circle No. 721

Speakeasy Computing Corp
224 S Michigan Ave
Chicago, IL 60604
(312) 427-2400
FAX (312) 427-4777
Circle No. 722

Spiral Software
6 Perry St, Suite 2
Brookline, MA 02146
(617) 739-1511
FAX (617) 739-4836
Circle No. 723

Spyglass Inc
701 Devonshire Dr, C-17
Champaign, IL 61820
(217) 355-1665
FAX (217) 398-0413
Circle No. 724

Statsoft Inc
2325 E 13th St
Tulsa, OK 74104
(918) 583-4149
FAX (918) 583-4376
Circle No. 725

Synergy Software
2457 Perkiomen Ave
Reading, PA 19606
(800) 876-8736;
in PA, (215) 779-0522
FAX (215) 370-0548
Circle No. 726

Systat Inc
1800 Sherman Ave
Evanston, IL 60201
(708) 864-5670
FAX (708) 492-3567
Circle No. 727

Triakis Inc
560 Bryce Ave
Los Alamos, NM 87544
(505) 672-3180
FAX (505) 662-2775
Circle No. 728

Trimetrix Inc
444 NE Ravenna Blvd
Suite 210
Seattle, WA 98115
(206) 527-1801
FAX (206) 522-9159
Circle No. 729

Wavemetrics
Box 2088
Lake Oswego, OR 97035
(503) 620-3001
FAX (503) 620-6754
Circle No. 730

3-D Visions Inc
412 S Pacific Coast Hwy
Redondo Beach, CA 90277
(213) 540-8818
FAX (213) 540-3492
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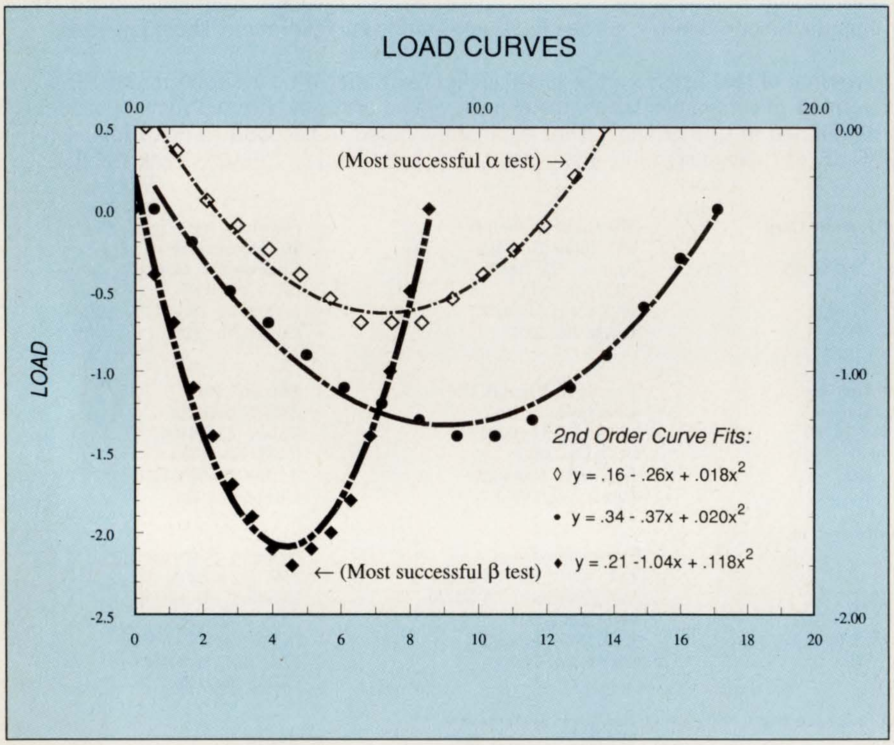
Graphing and curve-fitting software



***Fitting curves to data** is a useful way of perceiving relationships among variables. Next to these curves, which were created with Binary Engineering's Tech*Graph*Pad, are the equations the software created to fit the experimental data.*

ably break up the files into smaller ones. But doing so may require a lot of work, and the graphic output may not be acceptable. Some programs will read in every Nth set of Y values or every Nth set of Y values within a limited range of X values, where you can specify N and the boundaries of the X range. Such capabilities can be quite useful.

☑ Does the software support your printer or plotter? Most packages support large numbers of output devices, sometimes hundreds. Nevertheless, neglecting to check whether compatibility exists with your hard-copy device can result in unpleasant—and potentially costly—surprises.

☑ Similar caveats apply to checking for compatibility with your video-display hardware. You should make sure that packages that support the IBM VGA standard specifically suppor' your brand of VGA card at the resolution you hope to use. At resolutions greater than 640×480 pixels, little compatibility exists among supposedly equivalent VGA cards. If your graphics package supports resolutions such as 800×600 or 1024×768 pixels, you may have to rely on your VGA board vendor for video-driver software. Drivers for any but the most widely used packages are often difficult or impossible to obtain.

☑ Will the software save its graphical output to a file on disk? If so, what graphics file formats does it let you use? Once you've saved a file, can you produce the graphics on a printer or plotter without using the graphics package? With an appropriate hard-copy device, you can do so with files of certain standard types, such as Postscript and HPGL (Hewlett-Packard Graphics Language). Such a capability can be important if you plan to use the software on your PC at home but will be printing out your plots on a laser printer at work.

In addition to becoming an invaluable tool in your work, graphing, plotting, curve-fitting, and visualization software can also be a lot of fun to work with. One problem with selecting a technical graphics package, however, is the sheer number of products and their varied range of capabilities. Therefore, doing an intelligent job of selecting a package requires you to be clear about your needs. In addition, evaluating products will probably take more of your time than you'd like. If you take the trouble, though, your efforts will almost certainly be richly rewarded with time saved in interpreting data and good-looking reports and presentations. EDN

References

1. Stinson, Craig, "Who needs a graphics package anyway?" *PC Magazine*, December 11, 1990, pg 249.
2. Titus, Jon, "Draw your graphs on printers and plotters," *EDN*, April 13, 1989, pg 53.

Article Interest Quotient
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High 518 Medium 519 Low 520

WHAT'S NEXT

EDN's March 1, 1991, edition is our annual communications technology special issue. Leading off the coverage is associate editor Mike Markowitz's cover story on recent ISDN developments. Two other staff-written stories will look at CAE tools for transmission-line problems and transmitter and receiver modules for fiber-optic communications.

Discrete Products Division

CENTENNIAL 100 1891-1991

From Lights To Products That Enlighten... Our Century-Long Spirit Of Innovation Lives On.

Philips Components

PHILIPS

PHILIPS

A Look Back At A Company Built On Looking Ahead.

The first Philips carbon-filament lamp still burns symbolically today, inspiring us in the fundamental research that leads to better products.

CENTENNIAL 100 1891-1991

What a century! It started in 1891 with a young Dutch engineer deciding to produce incandescent lamps. Gerard Philips couldn't have dreamed that his tiny factory staffed with 10 would grow into a giant—the 22nd largest industrial corporation in the world.

He believed in the power of research. In 1908, he created a chemistry laboratory to help solve production issues with all types of lamps. Then six years later, he helped establish the Philips Physics Laboratory, which still today provides a broad range of research.

When suppliers proved unreliable during World War I, Philips opened its own plants to produce glass, hydrogen gas and cardboard. While others responded to the Depression by cutting back on research, Philips moved ahead with breakthroughs in gas-discharge lamps, X-ray equipment, gramophones, car radios, telecommunications equipment, welding rods and electric shavers.

Even vast destruction during World War II couldn't stop the momentum. Factories were rebuilt and production again reached pre-war levels by 1946.

After the war, science and technology made great advancements. Philips R&D laboratories contributed significantly with the invention of new magnetic materials that were used on a large scale. The knowledge obtained from this research formed the basis of later work on transistors, integrated circuits and charged coupled devices.

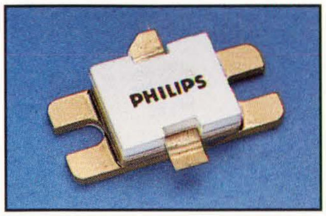
In recent years, Philips' work on lasers and microelectronics has achieved great advances in processing, storage and transmission of images, sound and data. Among the developments are the compact disc, LaserVision optical disc and new optical telecommunications systems.

Today in North America, Philips Components Discrete Products Division supplies the marketplace with thousands of quality electronic products. Passive components such as resistors, capacitors and trimmers. Discrete semiconductors including power, surface mount, MOSFET and small signal devices. Ferrite cores, beads, chokes, recording heads and other specialty products. And professional components such as camera tubes, photomultipliers and image intensifiers.

On front: Gerard Philips testing carbon filaments for lamps in 1890.

Our century-long spirit of innovation continues. Use the attached reply card to learn more about our products.

Microwave Transistor Offers Highest Output Power.



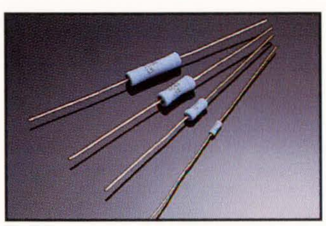
Philips' new PXB16050U microwave CW transistor provides the highest available output yet. Ideal for use in satellite links in INMARSAT and similar systems, the new transistor features input and output prematching circuits that simplify external circuit design and more evenly distribute power over its total active area. The result: no hot spots.

With its NPN silicon planar epitaxial design, the PXB16050U is geared for peak performance in common-base Class C narrow band amplifiers. Use it for voice and data communications on ships, aircraft and ground-based systems.

It provides 50W continuous wave power at 1.6GHz while operating from a 28V supply. Typical power gain is 9.5dB. Collector efficiency is as high as 52% with a low thermal resistance of 1.5K/W.

Gold metallization helps assure stability and extend device life, while use of diffused emitter ballasting resistors improve ruggedness and ensure excellent current sharing. Spec sheets available; delivery is 10 weeks ARO.

PPR5000 Film Resistors: Uncommon Stability, Power Handling.



Now you can specify a precision power film resistor with the stability and power handling ability you thought only wirewounds offered.

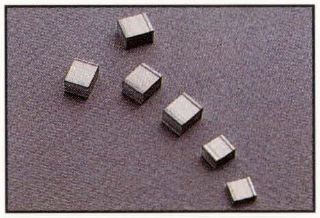
Replace your precision wirewound resistors with the new PPR5000 Series film resistors from Philips.

These resistors achieve the typically low inductance and reliability of metal film resistors and the power handling and stability of wirewounds—while maintaining comparably smaller size.

In power handling, the new series ranges from 1, 2, 3 and 5 watts at 25 °C with temperature coefficients to ±20 PPM. Tolerance levels are ±.05% to ±1% and maximum voltage ranges from 160 V at 1 watt to 500 V at 5 watts.

Ask for the PPR5000 resistors in bulk or on tape and reel. Delivery is 6 to 14 weeks.

Surface Mount Film Capacitors Keep Cost And Size Small.



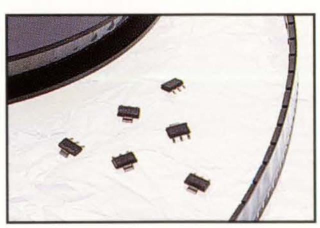
Thinking of ways to do away with encapsulation and shrink dimensions even more? Philips' new surface mount metallized film capacitors are what you need.

Made of high-temperature resistance dielectric polyphenylene sulphide (PPS) film in stacked construction, they're among the smallest capacitors on the market today. Three case sizes are available.

These new film capacitors feature solder-coated copper end-terminals to improve their solderability. They're ideal for all soldering processes—including wave soldering. Among other features: stability with temperature, voltage and frequency, high insulation resistance, low tan ESL/ESR, an open-circuit failure mode and high reliability.

Rated voltage is 25V DC with capacitance tolerances of ±5 and ±10%. Capacitors are available in blister tape on reel or in bulk.

First Schottky Rectifier In SOT-223 SMD® Package.



Philips has introduced the world's first Schottky power rectifiers in an industry-standard SOT-223 surface mount package. **PBYR235CT, PBYR240CT** and **PBYR245CT** feature a center-tapped pair of Schottky diodes. Each is capable of delivering an average output current of 1A and is perfectly matched through single monolithic substrate fabrication.

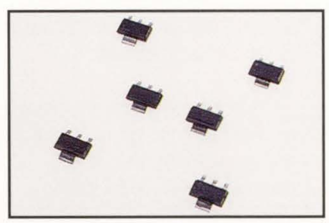
To assure highly efficient operation, the new rectifiers' forward voltage drop is less than 0.45V at a current of 1A. Leakage current at the diodes' maximum continuous reverse voltage is less than 100 μA.

Key features of the Schottky series include small size—just 6.5 x 3.5 x 1.8mm—a 2A current rating and surface mount capability.

The series offers reverse voltage ratings of 35, 40 and 45 volts that make it especially suited for low-voltage switch mode power supply applications such as 5V/2A units.

They're available on standard 12mm tape for SMD pick and place equipment. Samples and data sheets available. Production quantities delivered from 6 to 8 weeks ARO.

SOT-223 SMD® Package: Another Design First.



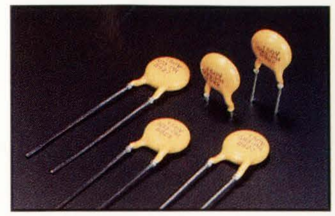
Few things have advanced medium-power surface mount design flexibility as much as Philips' introduction of its SOT-223 package.

A one-watt discrete semiconductor package when mounted on FR4 PCB, the SOT-223 allows you to achieve higher power dissipations and maximize board space without relying on conventional through-hole components. The new package dissipates 1 to 2 watts, and board mounting is possible with either reflow or wave soldering.

The SOT-223 is designed with flexibility of application in mind. The package can accommodate bipolar transistors, small signal MOSFETs, Schottky diodes, rectifier diodes, power MOSFETs, wide band/RF transistors, triacs and thyristors.

The surface mount package is especially suited to all applications where circuit board space is severely limited and power dissipations approaching 1W are required.

Flanged Varistors Improve Solderability.



An exclusive flanged design is key to the improved solderability of a new series of Philips zinc oxide disc varistors.

The new design also makes component insertion easier.

Available in 5mm and 7mm diameters, the new flanged varistors further expand Philips' line of straight-lead and kinked-lead devices.

By defining the mounting height of the varistor, the flanged lead minimizes stress on the component from automatic insertion equipment. The flange also improves solderability by allowing flux to escape through the PCB holes during soldering.

The new varistors offer maximum AC voltage ratings from 14V to 460V; maximum DC voltages from 18V to 615V. With maximum nonrepetitive transient current ratings from 100A to 1200A, and transient response times of less than 20 nsec.

Use them to suppress voltage transients in telecommunications, data processing, consumer and automotive electronics applications. They're available in bulk or tape and reel. Delivery 6-12 weeks.

Plumbicon® Camera Tube Geared To Medical, Industrial Use.

Medical X-ray imaging, military and industrial vision systems will get a boost from the new very high resolution Plumbicon camera tube.

High spatial resolution, improved contrast resolution and enhanced S/N are among the advantages of Philips' Type 88XQ tube.

DETACH HERE

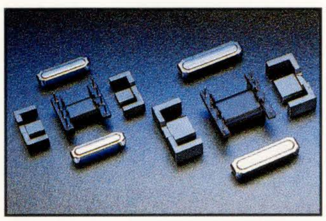
SMD® is a servicemark of North American Philips Corporation.

Electrostatic deflection reduces both the tube's length and overall "in-coil" diameters, making it an ideal fit for compact cameras. Its conical shape helps reduce operation scanning voltage. And because of the electrostatic deflection, corner and center resolution are better than that offered by magnetic deflection tubes.

The 88XQ is especially suited for medical imaging. It offers the highest modulation depth of all lead oxide tubes, resolving more than 2500 TV lines in the center and more than 1600 in the corner. Short response time is another advantage. And the camera tube's lag is tunable, a major design benefit for such dynamic applications as cardiac study.

Other 88XQ features: a low output capacitance (LOC) window, and a diode gun capable of handling 4 μA of peak signal with minimal loss of resolution and deterioration of lag characteristics.

Flat E-Cores Reduce Height In Transformers.



Making use of low-loss 3F3 material, Philips is introducing a series of flat E-cores designed to cut the height of transformers in DC/DC power modules.

The EFD (Economic Flat Design) cores come in four types:

- 15/8/5 for board areas 15 x 15mm and 500kHz operation
- 20/10/7 for board areas 20 x 20mm and 300kHz operation
- 25/13/9 for board areas 25 x 25mm and 100kHz operation
- 30/15/9 for board areas 30 x 30mm and 100kHz operation

All the new flat cores can be operated at up to 1MHz and can be used in transformers with power throughput densities as high as 20W/cm. That's possible because of the cores' high-frequency ferrite materials and computer-aided design.

EFD cores come with matching bobbins and clips suitable for automated production lines. Sample cores—with bobbins and clips—are now available from Philips.

SMD® Tantalum Chips Offer Extended Capacitance.

Philips is introducing a new line of conformally coated tantalum chip capacitors for use in high-reliability and medical applications.

The 49EC Series capacitors offer high capacitance density with low ESR values at 100 kHz and low DC leakage current. They're designed for operation from −55 °C to +85 °C with rated DC voltage applied. AT 67% of rated voltage, the temperature range can be extended to +125 °C.

The new capacitors, though non-military, are pad-compatible and interchangeable with established MIL-C-55365/4 CWR06 conformally coated and CWR09 molded tantalum chips.

Depending on the voltage rating, 49EC chips offer two to three times the capacitance values of CWR06 and CWR09 products in the same case size. Rated DC voltages of 4, 6, 10, 15, 20, 25 and 35 volts are available in each of eight case sizes. These sizes are identical to those of CWR06 devices. Gold-plated or hot solder-dipped terminals are available. Standard capacitance tolerances include ±20%, ±10% and ±5%. Delivery is 12 to 14 weeks ARO.

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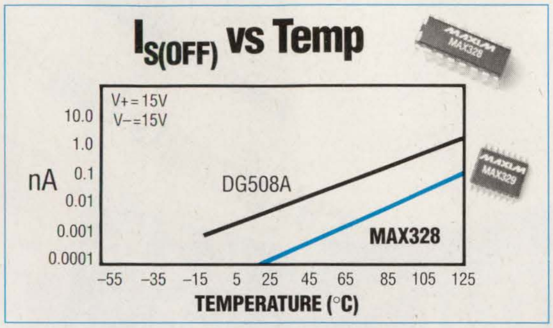

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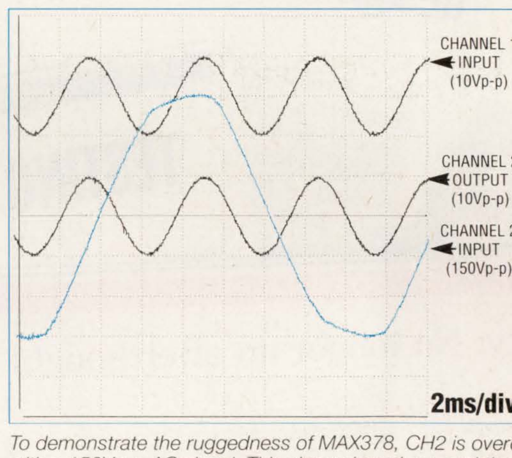

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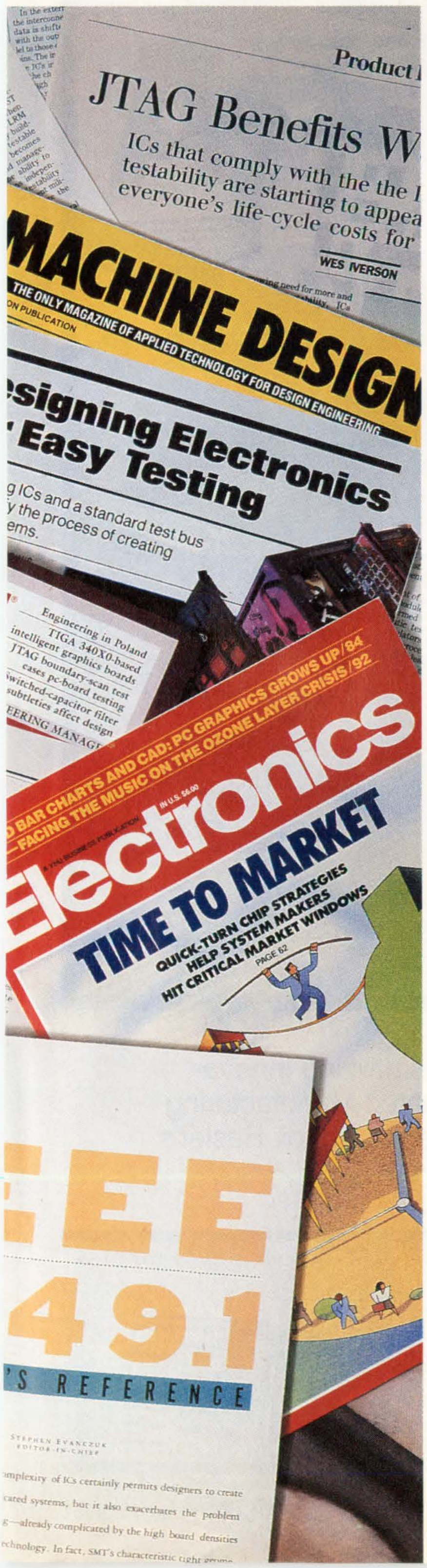

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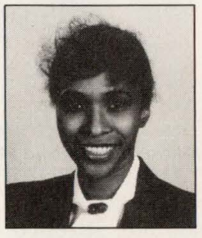
TEXAS INSTRUMENTS

VXI packaging and power issues heat up



Some manufacturers have split VXI instruments, locating segments outside the mainframe or in multiple slots, to meet heat dissipation and power demands. Others are using onboard cooling fans, fins, and towers.

J D Mosley,
Regional Editor

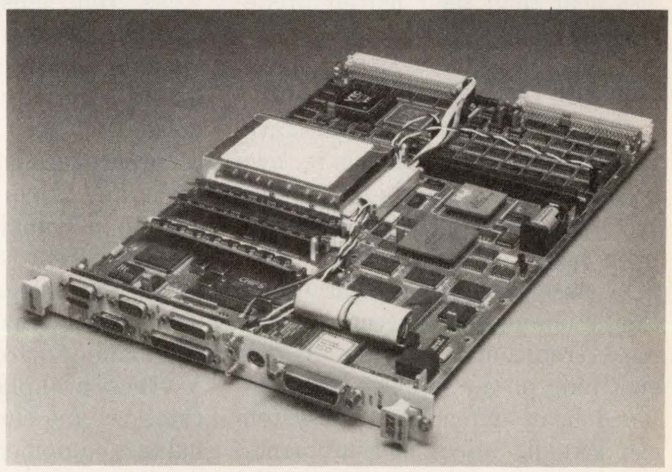
Many test engineers incorrectly assume that all VXI (VME extensions for instrumentation) mainframes are created equal. However, VXI enclosures and power ratings vary, and they are among the most important factors that designers of VXIbus test-and-measurement systems should investigate. The high performance that engineers demand from VXI instruments can translate into high power consumption, which in turn results in high heat dissipation. If you let such heat build up within the enclosure, you can jeopardize the integrity of your components' measurements.

Unfortunately, many manufacturers fail to publish specs for cooling capacity. So, when shopping for a mainframe, you should find out each box's cooling capacity per slot and identify which slot presents the worst case. You must also verify whether the manufacturer's per-slot power ratings are based on continuous or intermittent operation. Specs based on 30-sec operation cycles may not provide an adequate safety margin if the VXI module you plan to use functions continuously for longer periods of time.

Even if you don't have your mainframe loaded with modules, heat can produce problems if the air blown into the enclosure merely swirls through the empty slots, following the path of least resistance. Hewlett Packard combats this problem in its C-size E1400B mainframe by using a pressurized air-channel cooling system. This system forces air through each module, even when any or all of the enclosure's faceplates are open.

Other enclosure manufacturers equip their mainframes with *smart fans* that incorporate thermal resistors. These heat-sensitive resistors permit a fan to slow down or speed up in response to the temperature within the enclosure. However, a blocked vent can restrict airflow so severely that even the smartest fan wouldn't be able to dissipate sufficient heat to protect your instruments.

Augat solves the blocked-vent dilemma by equipping its enclosures with airflow sensors connected to audible

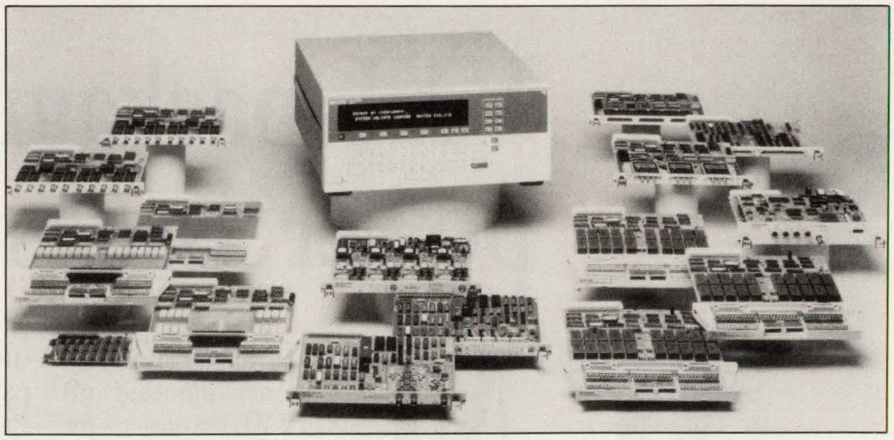


As manufacturers pack more components and functionality into a single VXI module, *heat and power considerations escalate. National Instruments used SMT components, custom ASICs, and advanced packaging technology to produce the VXIpc-386/1, the industry's first single-slot PC/AT-compatible embedded VXI controller.*

alarms. Besides alerting you to the problem of a blocked vent, the alarm also notifies you when to change air filters. Similarly, Augat enclosures monitor all seven power-supply outlets and provide visual and audible alarms that warn you of both intermittent glitches and terminal power failures.

In contrast, Racal-Dana markets a VXI module that cools itself. The company sells a 250-MHz time-interval analyzer that contains a number of high-performance custom ASICs. Instead of relying upon whatever air flow might be available in an enclosure, this module includes fans to ensure adequate ventilation. So, the board should perform to spec no matter how your mainframe controls cooling.

Not all methods of achieving maximum heat dissipation have met with acceptance. Tom Curfman, product marketing manager for ICS Electronics, noted that his company used to offer an enclosure with steel shields for optimum cooling capability. Customers objected so strongly to the weight of the box that ICS now only produces enclosures with aluminum shields. Unfortunately, these lightweight boxes dissipate less heat than their heftier predecessors.



Billed as an entry- level alternative to the more popular C-size modules, *Hewlett-Packard's 75000 B-size series of VXIbus products offers low-cost computer-aided test and measurement.*

Separate the hot from the cold

In traditional rack-and-stack systems, each instrument has its own power supply, and these supplies can generate a lot of heat. Aside from heat, switching power supplies also generate oscillations on the dc power line. Therefore, since most traditional instruments use switching power supplies, the combined heat and noise in a system can actually affect measurements. VXI systems attempt to avoid the heat and noise of a traditional configuration.

If your VXI system comprises only simple measurement instruments, they shouldn't create significant heat and noise problems. Unlike traditional rack-and-stack test systems, all the instruments in your VXIbus system will share a common enclosure and power supply. But, if your applications require you to use test equipment that consumes a lot of power, you shouldn't plan to locate that equipment inside the VXI enclosure. Instead, you should use Slot 0, or a VXIbus extender, and a separate backplane. High power consumption often produces high heat and noise, so you should segregate high-power devices from sensitive instruments. You may have to sacrifice the convenience of using a single enclosure for the security of avoiding heat and noise.

Intepro, a company that manufactures a VXIbus power-supply test system, eliminates noise and heat constraints by splitting their test instrument into two segments. A C-size, message-based, power-system commander card plugs into your VXIbus backplane and communicates via any slot 0 with the external test equipment. The commander card contains all the firmware needed to control the rack-mounted test equipment. That way, not only is the heat- and noise-generating equipment isolated from the VXI mainframe, but Intepro customers also can upgrade to a VXI interface without abandoning their existing hardware.

The key to successfully splitting such instruments lies in the way the two halves communicate with each other. As noted by Michael O'Connor, president of Intepro, you will achieve maximum system performance if you are careful not to create a hybrid architecture. Such a hybrid would occur if you mixed internal VXIbus and external IEEE bus operations. Although both buses appear to be well-matched according to their data transfer rates, the IEEE-488 transfer performance slows dramatically when your system frequently accesses one or more discrete addresses, as is the case in most test and measurement applications.

Larry Desjardin, HP's VXI program manager, maintains that splitting up an instrument into multiple slots inevitably reduces that instrument's performance. At the present time, that drop in performance makes VXI less suitable than other platforms for highly sensitive RF and microwave measurements. However, Desjardin theorizes that future technological advances may minimize this performance loss and allow the VXIbus to adequately ad-

Table 1—Representative VXIbus system components

Manufacturer	Model	Form factor	Description	Price	Features
BICC-Vero	Backplanes	C, D	Backplanes	$600 to $2500	10-layer stripling construction; 5- to 13-slot versions
Colorado Data	73A-021	C	13-slot mainframe	$6000	Includes power supply for maximum of 45W/slot; Block-mode high-speed data transfers
	73A-IBX	C	IEEE-488 VXIbus system	$8000	Access to individual VXIbus registers; Interface to IEEE-488 instruments via IEEE-488 bus
	73A-PCX	C	PC-compatible instrument system	$8500	Includes interface to PC-compatible computers via IEEE-488 bus
	73A-PRT	C	Prototyping system	$10,000	Mainframe with Slot 0 prototype modules; Message-based VXI interface
Elgar	VXP1000	C, D	Power supply controller card	$2495	Controls 4 power sources with as many as 16 dc channels and three phases of ac power
Elma	System 12	A, B, C, D	Backplanes & chassis	$4000 to $5500	Modular systems available from stock with power supplies ranging from 100W to 2000W
	69-A12VXIB	B	Backplane	$995	12-slot B-size backplane; 12-layer strip line construction; Separate TTL and ECL signal layers
	69-A13VXID	D	Backplane	$2395	13-slot D-size backplane; 12-layer strip line construction; Separate TTL and ECL signal layers
Hewlett-Packard	E1400B	C	13-slot mainframe	$6275	Jumperless backplane; Power supply; Pressurized air-channel cooling
	E1300A	B	7-slot mainframe	$2300	Built-in Slot 0 & Resource Manager; HP-IB and RS-232 interfaces; 80W power supply
	E1301A	B	7-slot mainframe	$2800	Similar to E1300A; Includes front panel & 2-line display
ICS Electronics	VXI-KIT 113-991	C	Shielded enclosure	$250	Single-wide; Includes front panel, RFI gasket, and side shields
	VXI-KIT 113-992	C	Shielded enclosure	$300	Double-wide; Includes front panel, RFI gasket, and side shields
Mac Panel	Series 120	A, B, C	Subrack assemblies	$2000 to $5000	Custom-configured mainframe rack assemblies and associated hardware
Mupac	GB12	B	Backplane	$895	Split ground-plane reduces ground loops
	213 Series	C	Wire-wrap board	$1395	Schottky design aids current distribution and capacitance
National Instruments	VXI-AT2000	C	MXI Interface kit for PC/AT	$3800	Lets a PC/AT function as a VXI commander and Resource Manager; Includes Labwindows
	VXI-MXI	C	VXIbus mainframe extender to MXIbus	$1995	Transparent 1-slot extension for VXIbus
	VXI-1000	C	5-slot mainframe	$3600	250W power supply; Carrying handle; Short-circuit protection; Rack mountable
Racal-Dana	1261	C	13-slot mainframe	$6450	12-layer backplane; Power supply; Cooling fans; Recessed cable tray
	1261E	C	RF chassis	$11,995	Double-skin construction attenuates external radiation; Shielded door for RFI sealing
	1262	C	13-slot mainframe	$9875	Similar to 1261, with hinged receiver mechanism and interconnect assembly
Radisys	VXI-B1	B	Portable 12-slot chassis	$9995	Includes embedded 80386SX-based computer and Slot 0 controller
	VXI-B2	B	Portable 12-slot chassis	$12,285	Includes embedded 25-MHz 80386-based computer and Slot 0 controller
Tektronix	VXI1500	D	13-slot mainframe	$9995	Includes power and cooling for maximum of 100W/slot
	VXI1505	D	6-slot mainframe	$7150	Includes power and cooling for maximum of 100W/slot
	VXI1400	C	13-slot mainframe	$7000	Includes power and cooling for maximum of 50W/slot
	VXI1405	C	5-slot mainframe	$3795	250W power supply; Carrying handle; Short-circuit protection; Rack mountable
Tracewell	System 23	C, D	13-slot mainframe	$5510, $6595	Mainframe comes with a 1000W power supply
	System 24	C	5-slot development system	$2445	Mainframe includes a 700W power supply
	System 90	C, D	13-slot mainframe	$6360, $7115	Microprocessor-controlled, monitors power supply voltages and airflow, visual and audible alarms

dress a full range of high- and low-frequency applications.

If you wish to sidestep the "split instrument" dilemma, consider using a VXIbus extender. The most popular is the MXIbus (multisystem Extensions interface bus), which lets you connect multiple VXI mainframes, stand-alone instruments, and IBM PC-compatible computers without the kind of performance degradation you'd experience in a VXI/IEEE-488 hybrid.

The MXIbus (pronounced MIX-ee bus) is a VXIbus enhancement that lets you daisy-chain and multidrop mainframes full of card-bound VXI instruments, as well as full-size physical instruments and PCs. It provides a 32-bit multimaster, frame-to-frame interface that lets a single VXIbus resource manager configure and control as many as 256 devices in a parallel-bus architecture.

Developed by National Instruments, MXIbus lets you tightly couple a VXIbus to computers and instruments that will never physically fit on a VXI module. MXIbus provides word-serial drivers and utilities that let the VXI resource manager identify all the devices in a system, manage self-testing, configure the A24 and A32 address maps, establish the initial system hierarchy for multimaster arbitration, and initialize normal system operation. MXIbus also defines a method for extending TTL triggers, VME interrupts, CLK10, and SYSFAIL across multiple frames.

Because MXIbus doesn't specify what you can attach to it, it is more of a general-purpose bus than the instrument-specific IEEE-488. Thus, you can tap the data flow from high-speed input devices such as optical scanners without facing the bottleneck posed by protocol-laden links.

In addition, although embedded PCs-on-a-board are currently available for the VXIbus, you may find the combination of your own PC and a $995 AT-MXI board from National Instruments to be a more cost-effective and versatile option for control and programming. And if you think that an embedded PC would, by definition, provide higher performance because it's located on the VXI backplane, remember that such functionality as memory caching and math coprocessing can actually make your external PC faster than its bare-bones, internal cousin.

A VXI Consortium technical subcommittee is currently using the

MXIbus as the basis for mainframe-extension standardization.

Determining the size of the boards you will use in your VXI system requires more than mere space considerations. A- and B-size modules have dimensions identical to their VMEbus counterparts—3.9×6.3 in. and 9.2×6.3 in., respectively, with 0.8-in. slot spacing. C-size modules measure 9.2×13.4 in. and D-size is 14.4×13.4 in., both with 1.2-in. slot spacing. **Fig 1** displays the relative size of the four form-factors and the signals available to the modules via the three defined VXIbus connectors.

A-size modules are scarce, mainly because of their limited board size and limited data-transfer capacity. D-size boards are the only boards that can access VXI's P3 connector, with its additional 24-pin local bus,

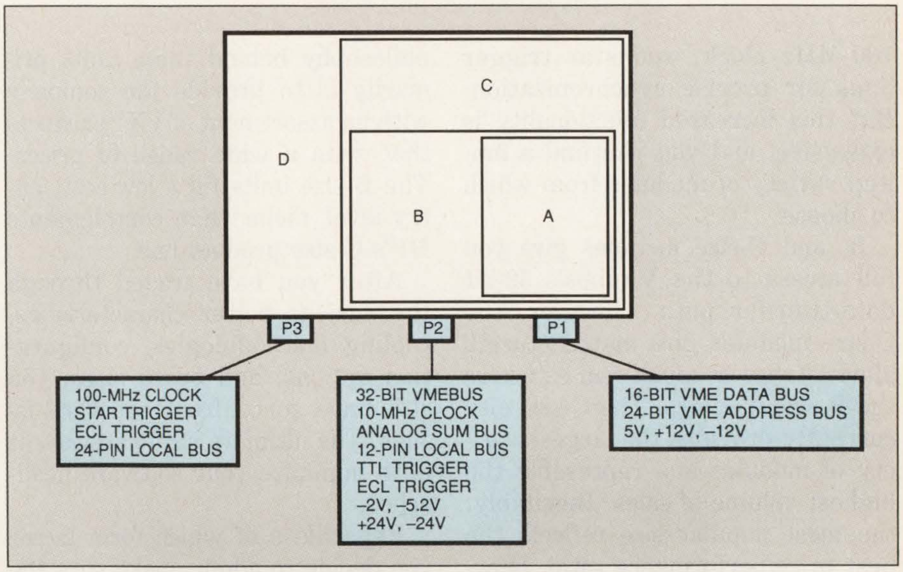


Fig 1—The VXIbus specifies three 96-pin DIN connectors. *In addition to three power pins and some interrupt buses, P1 includes a data-transfer bus that offers 24 address bits and 16 data bits. P2 expands the data-transfer bus to 32 bits and includes greater resources such as four additional power-supply voltages, a local bus, the module-identification bus, a current-summing bus, TTL and ECL trigger buses, and a 10-MHz clock. The D-size P3 connector offers 24 more local-bus lines, a 100-MHz clock, and more trigger lines.*

VXIbus power and packaging

100-MHz clock, and star trigger lines for precise synchronization. But this increased functionality is expensive, and you will find a limited variety of modules from which to choose.

B- and C-size modules give you full access to the VXIbus's 32-bit data-transfer path. However, the C-size modules give manufacturers almost twice as much real estate as the B-size modules. The C-size also currently provides the largest variety of modules and represents the highest volume of sales. Inevitably, the most popular size reflects the best price/performance ratio. However, if you face a limited budget or severe size constraints, you'll find HP promoting a comparable variety of B-size VXIbus products.

HP is fairly unique in touting B-size configurations. The marketing philosophy behind these units primarily is to provide the company with an assortment of VXI products that span a wide range of prices. The B-size units fill a low-cost, entry-level niche that complements HP's C-size product line.

After you have waded through the various power characteristics, cooling methodologies, configuration options, and board sizes, you still have to confront software issues. The ultimate hardware caveat is to minimize your software headaches.

Regardless of which form factor you decide to adopt, make sure the modules have a SCPI-compatible command-set interface. SCPI (Standard Commands for Programmable Instrumentation) provides a common command set that simplifies software development and maintenance, thereby reducing your overall system costs. Standardizing on SCPI (pronounced skippy) also provides you with a simple migration path to higher performance instruments that may become available in the future. EDN

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1. Bodie, Fred, *VXIbus Newsletter*, Vol 2, No 3, August 1990.
2. Kerridge, Brian, "Small products add big spark to test field," *EDN*, November 22, 1990, pg 43.

Article Interest Quotient
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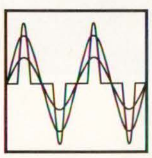

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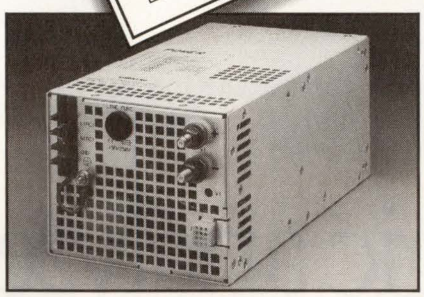

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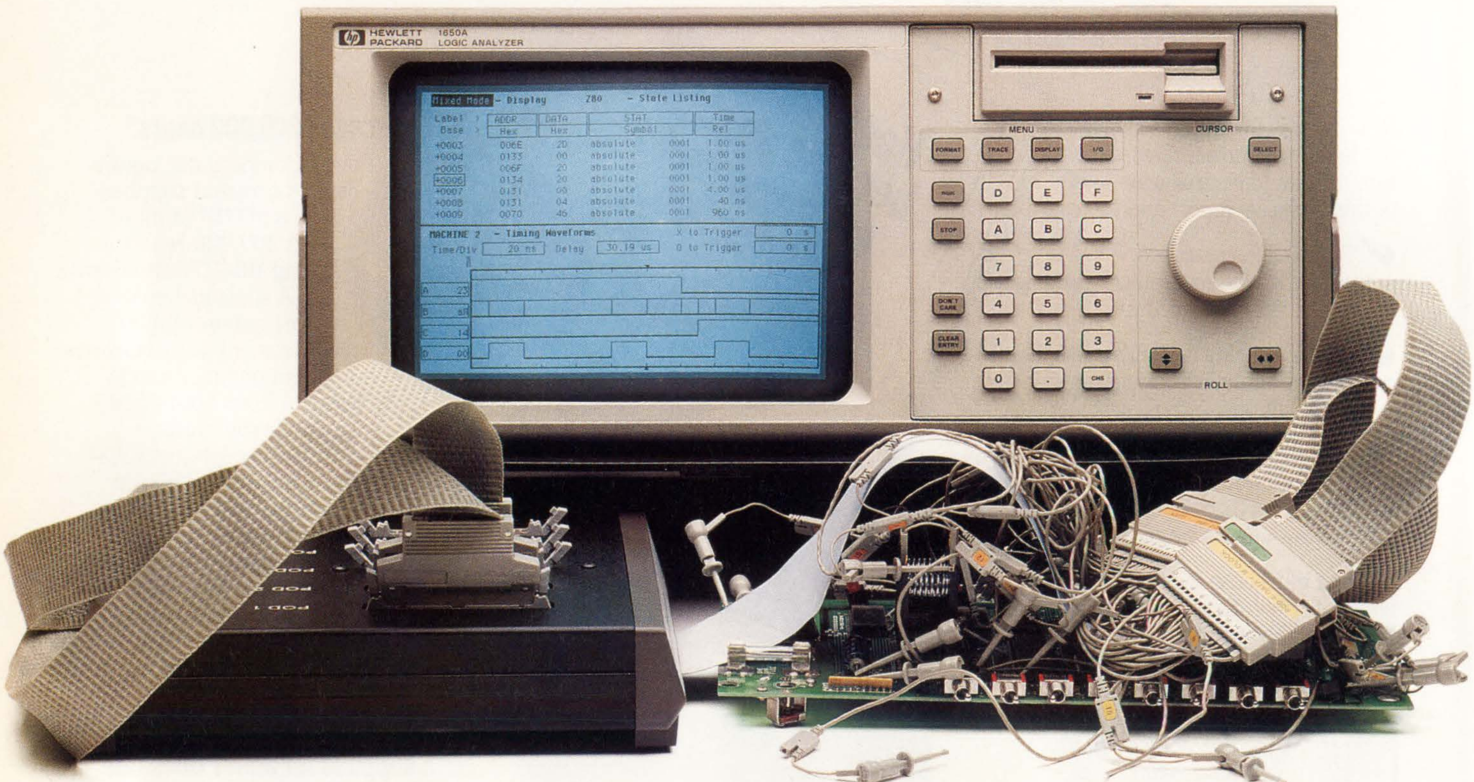

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Channels used	48[1]	48[2]	20
One connection	No	No	Yes
Setups	Two	Two+	One
Interfaces to learn	Two	Two+	One
Integrated state & timing triggering	No, only one arming condition	No, only indirect 4-bit Teklink	Yes, 8 levels
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Footnotes: 1) 8 channels lost to de-multiplexing
2) De-multiplexing requires double probing and only nine high-speed channels on basic unit

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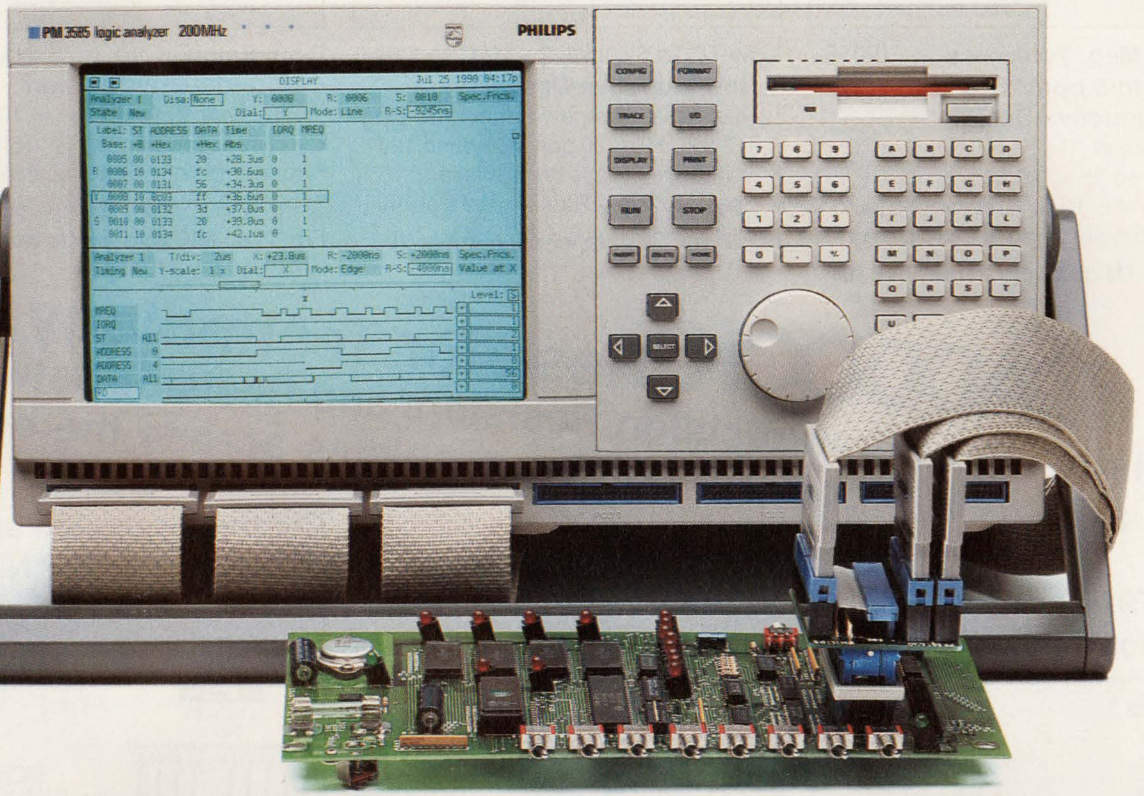

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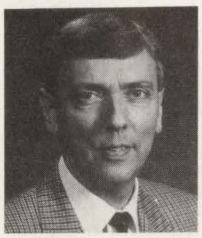
LOW-DRIFT OP AMPS

Precision parts demand kid-glove treatment



Selecting the best low-drift op amp for your sensitive design is an ordeal in itself. Further trials await when you strive to realize the specified performance goal.

Brian Kerridge, European Editor

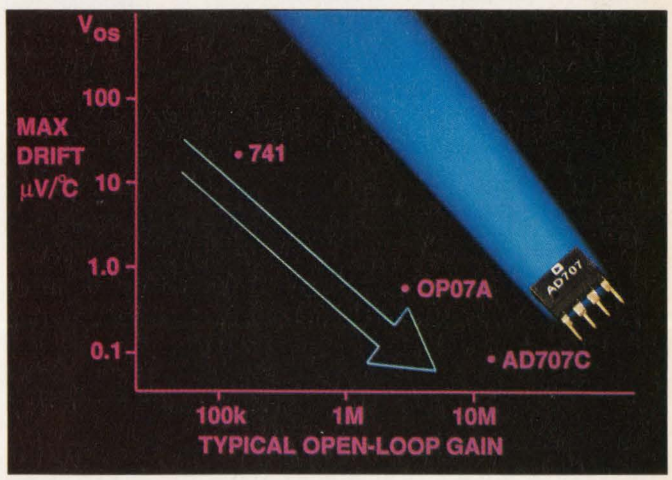
Achieving input offset voltage temperature coefficients (V_{io} TC) of less than 1 μV/°C in op amps is now commonplace. But, for precision circuits, this specification and other low-drift effects can still dog your design. Depending upon the application, V_{io}, V_{io} noise, and input bias current (I_B) all can prove troublesome. If you demand speed or low power consumption, then expect to trade off low-drift performance.

The problem op amp designers face is how to balance these key spec areas. It's possible to maximize any one parameter at the expense of others, and the designer's dilemma is choosing which parameter to maximize and by how much. The net result is a mishmash of devices, all justifiably claiming low drift. If you're designing temperature- or strain-gauge amplifiers, DMM front ends, log amps, low-noise audio circuits, low-frequency active filters, and reference buffers, you'll need time to sift out the optimal part for your application. Compound the list with dual and quad versions; mix in metal, ceramic, and plastic packages; and you could end up poring over data sheets for hours.

Although designers do an excellent job of minimizing drift within the op-amp package, effects of thermal EMF, current leakage, and extraneous noises persist. Simply thrusting a low-drift op amp into a socket or casually soldering it to an open pc board will ruin your overall design. Unless you consider the choice of materials and component layout along the op amp's signal path, external error sources will spoil its low-drift capability.

Table 1 shows just a small selection of the available low-drift op amps. Take care when comparing these parts—the table displays the breadth of what's available, rather than a collection of equivalent parts. Hence, the price column shows disproportionate differences.

Some vendors offer their best specs only in more expensive ceramic or metal packages. Lower-cost plastic packages are not preferred for low-drift designs. Ceramic and metal packages have hermetic seals and lower thermal resistance. Observe also, in **Table 1**, that although



***Analog Devices' bipolar AD707C performs far better** than the ancient 741 and the long-standing low-drift champion OP07A. It's expensive at $16, but with a V_{io} TC max of 0.1 μV/°C and an open-loop voltage gain of 138 dB min, the AD707C offers CMOS chopper drift performance without the noise penalty.*

Low-drift op amps

all noise specs appear for 0.1 to 10 Hz bandwidth, some manufacturers give only typical noise specs, notably for chopper input parts. In a design, you need to know the p-p noise, and that may be double the typical value supplied.

Making the choice for input

One of the key decisions you'll make in selecting a low-drift op amp will be between conventional bipolar or chopper input stages. Chopper input amps offer outstanding V_{io} low-drift performance over time and a range of temperatures. Using CMOS technology, the I_B and power-consumption specifications are also attractive. Additionally, some parts operate on ±15V supplies, overcoming the earlier ±7.5V limitation. But you pay the penalty of increased noise when you use choppers. Although improvements over the original 7650 chopper from Intersil are appreciable, bipolars still score higher in this one area.

At Precision Monolithics, Art Kapoor, product marketing manager, agrees: choppers have improved, but the best overall compromise of low-drift parameters comes from a bipolar design. The company's OP177E is an example of what is achievable. This part has a noise specification of 0.15 μV rms max for 1 to 100 Hz, and a V_{io} TC of 0.1 μV/°C max.

Linear Technology's Bob Dobkin, vice president of engineering, has a hard time believing that anyone has achieved a V_{io} TC of 0.1 μV/°C from a bipolar op amp. In his view, you can measure performance at this level five times and get five different answers. He maintains that 0.2 to 0.3 μV/°C is a more reasonable expectation. Linear Technology is the only company that offers bipolar and chopper low-drift op amps. Dobkin defends chopper op amps' noise performance but agrees they have shortcomings for designs handling ac signals, heavy loads, or requiring low wideband noise. Linear Technology publishes a useful guide to help you select chopper vs bipolar op amps (**Ref 1**).

Texas Instruments squeezes a neat combination of low-drift parameters from a nonchopping CMOS op amp with its TLC2201B. However, for a precision amp, it's a bit short on open-loop gain—at just 100 dB with a 10-kΩ load. Its common-mode and supply-voltage rejection ratio at 90 dB also requires attention.

Harris' 5221 shows a rare combination of low-drift parameters and speed. The amp slews at 25V/μsec, but the penalty is power consumption, with a max supply current requirement of 11 mA.

All op amps shown in **Table 1** are single-amplifier devices. In most cases, vendors offer dual and quad versions in a single package. For bipolar types, packaging multiple devices compromises drift specifications. You must consider the possibility of thermal crosstalk from one amplifier to another and accept the absence of nulling pins for finely adjusting input-offset voltage. Even where nulling pins exist, you need to take care not to use this facility to force large offsets into the op amp's input stage. If you attempt this in order to cancel a zero error from an earlier section of your design, you will simply degrade the V_{io} TC of the op amp. Typically, every 300 μV of offset you impose results in a 1 μV/°C TC.

When you've decided which op amp is best for your design, preserving that performance in practice is the next obstacle. The great-

For more information . . .

For more information on the low-drift op amps discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Table 1—Representative low drift op amps

Vendor	Model	Input type	Input offset-voltage vs temperature (μV/°C)	Input offset-voltage vs time (μV/month)	Input voltage-noise 0.1 to 10 Hz (μV p-p)	Input offset-voltage (μV)	Input bias-current	Package	Comments	Price (100s)
Analog Devices	AD707C	Bipolar	0.1	0.2 typ	0.35	15	1.0 nA	TO-99, 8-pin ceramic DIP		$16.00
	AD829A	Bipolar	0.3 typ	NS	0.05 typ	500	7 μA	8-pin ceramic DIP	Bandwidth 120 MHz (A_V=−1), slew-rate 230 V/μsec	$4.25
Harris	HA-5147A	Bipolar	0.6	NS	0.18	25	40 nA	TO-99, 8-pin ceramic DIP	Gain bandwidth product 120 MHz (A_V > 10), slew-rate 35 V/μsec typ	$8.78
	HA-5221	Bipolar	0.5 typ	NS	0.25 typ	750	100 nA	TO-99, 8-pin ceramic DIP	Gain bandwidth product 35 MHz (A_V=1), slew-rate 25 V/μsec typ	$6.68
Linear Technology	LT1037A	Bipolar	0.6	1.0	0.13	25	35 nA	TO-5, 8-pin ceramic & plastic DIP	Open-loop voltage gain 126 dB min with 600Ω load, slew-rate 11 V/μsec	$5.00
	LT1097C	Bipolar	1.0	0.3 typ	0.5 typ	50	250 pA	8-pin plastic DIP	Supply current 0.56 mA max	$1.05
	LTC1150C	Chopper	0.05	0.05/$\sqrt{\text{month}}$ typ	1.8 typ	5	50 pA	TO-5, 8 & 14-pin ceramic & plastic DIP, 8-pin SO	Supply voltage ±2.5 to ±18V, supply current adjustable 0.2 to 0.8 mA	$3.85
Maxim	MAX480C	Bipolar	1.5	NS	3.0 typ	70	3 nA	8-pin plastic DIP, 8-pin SO	Supply voltage ±0.8V to ±18V, supply current 20 μA max at 15V	$3.95
	MAX422E	Chopper	0.05	0.1/$\sqrt{\text{month}}$ typ	1.2 typ	5	30 pA	8-pin plastic DIP	Supply voltage ±2.5V to ±16.5 V	$3.77
	MAX425C	CMOS	0.05	NS	0.25	5.0	200 pA	8 & 16-pin ceramic & plastic DIP, and SO	Programmable zeroing facility, eg: auto-zero cycles at 1-minute intervals	$9.50
National Semiconductor	LM607C	Bipolar	0.3	0.2 typ	0.5	40	4.0 nA	TO-99, 8-pin ceramic & plastic DIP		$1.26
	LM627A	Bipolar	0.6	0.2	0.18	50	20 nA	TO-99, 8-pin ceramic & plastic DIP		$4.53
Precision Monolithics	OP-07A	Bipolar	0.6	1.0	0.6	25	2.0 nA	TO-99, 8-pin ceramic DIP	Former industry standard	$16.50
	OP-21E	Bipolar	1.0	NS	NS	100	100 nA	TO-99, 8-pin ceramic DIP	Supply voltage ±2.5 to ±15V, supply current 300 μA max	$3.25
	OP-50E	Bipolar	0.3	NS	0.12 typ	25	5.0 nA	14-pin ceramic DIP	Output current ±50 mA	$8.10
	OP-177E	Bipolar	0.1	0.2 typ	0.6	10	1.5 nA	8-pin ceramic DIP		$14.95
Teledyne Components	TSC911A	Chopper	0.15	NS	11 typ	15	70 pA	8-pin ceramic & plastic DIP, and SO	External capacitors not required	$2.14
	TSC9420E	Chopper	0.1	0.1/$\sqrt{\text{month}}$ typ	1.1 typ	5	30 pA	8 & 14-pin plastic and ceramic DIP	Supply voltage ±15V	$3.89
Texas Instruments	TLC2654A	Chopper	0.05	0.02	1.5 typ	10	50 pA typ	8 & 14-pin ceramic & plastic DIP, and SO		$3.01
	TLE2027A	Bipolar	1.0	1.0	0.13	25	35 nA	8-pin ceramic & plastic DIP, and SO		$5.26
	TLC2201B	CMOS	0.5 typ	0.005	0.7 typ	200	1 pA typ	8-pin ceramic & plastic DIP, and SO	Supply voltage ±8V; common-mode & supply-voltage rejection ration 90 dB min	$8.20

Notes: Maximum specifications at 25°C shown unless otherwise stated
NS=not specified
SO=small outline
A_V=open-loop voltage gain
Prices shown in order of availability, plastic, ceramic, or metal

est threat to low-drift performance comes from the presence of thermal EMFs external to your op amp. These irritating sources of voltage occur wherever a junction of differing metals produces a temperature gradient. A typical thermocouple intended for use as a temperature sensor develops around 10 to 50 μV/°C, depending on the type. When you compare that TC with an op amp's normal V_{io} TC of under 0.5 μV/°C, it's no surprise that stray EMFs in a signal path can ruin a design. A series of junctions exists

Digital bits invade analog part

Maxim offers an alternative to bipolars and choppers with a commutating autozero CMOS op amp. The recently announced MAX425 and MAX426 apply internal switching to null the input characteristics of CMOS amps in a similar fashion to choppers. Whereas choppers attempt to optimize all input drift errors, including 1/f noise, with one internal nulling loop, Maxim's design employs two independent and programmable on-chip nulling schemes. First is an autozero loop, and second is a commutating input switch. **Fig A** shows the essential parts of the design.

The autozero loop operates by shorting the input switch and nulling the first and second stages of the op amp. The loop operates until the voltage at the comparator equals the level immediately prior to commencement of the autozero cycle. Digital memory in the control logic stores the correction factor and maintains the null by controlling the analog input stages via DACs. One cycle of this autozero loop typically reduces an inherent 50 μV V_{io} to 0.5 μV. You can program the autozero loop to operate on command, or automatically once per minute. While the autozero loop is in action, the op amp's third stage operates as a sample-and-hold circuit and maintains the op amp's output at a constant voltage. The down side of this technique is the 50 msec it takes for one cycle of autozero, even on the faster MAX426. The merit is that if your design enjoys a stable environment, you may need only one cycle of autozero every few hours or days.

The commutating input switch runs at a default frequency of 300 Hz, although external frequency control is possible. When the switch operates, the op amp's V_{io} alternately adds to and subtracts from your real input signal. The resultant input is the real signal, amplitude modulated at 300 Hz by V_{io} and 1/f noise. Later averaging yields only the real input signal.

You can decide when either, neither, or both nulling schemes suit your application. In practice, the commutating switch operation is almost always beneficial, otherwise 1/f noise remains in the signal path. The autozero operation is optional, but normally necessary at least once following power-up. It removes a chunk of V_{io}, and minimizes the amplitude modulation at the commutating switch.

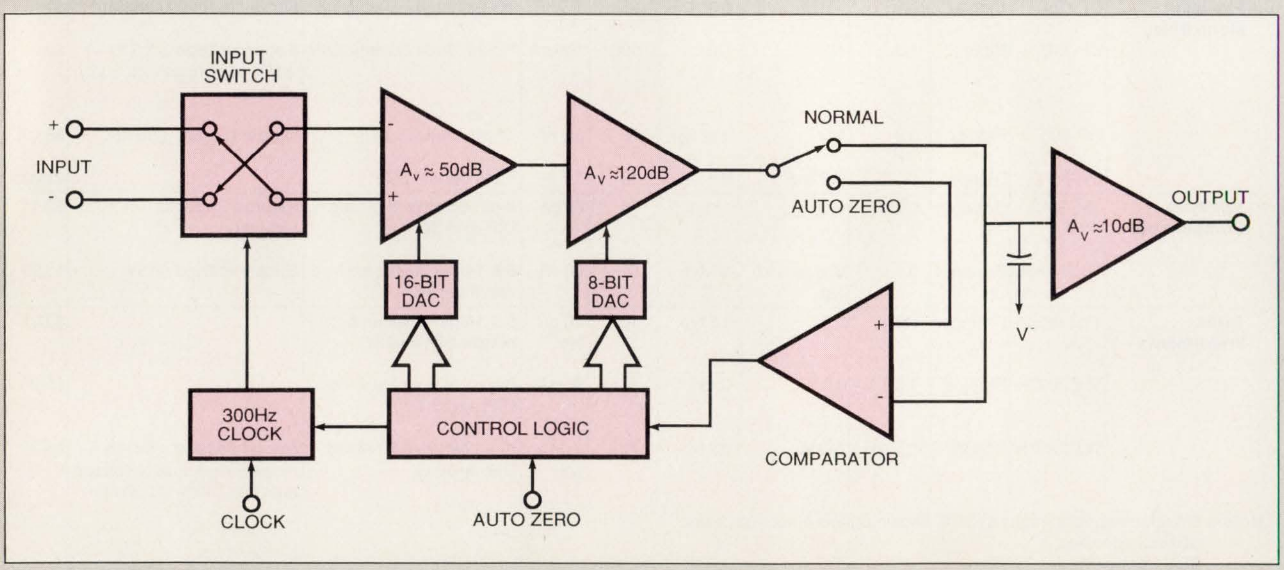
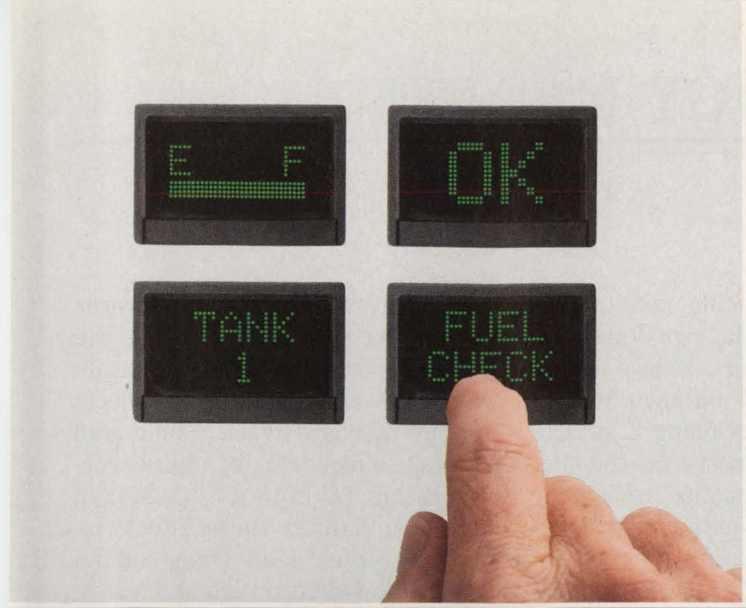


Fig A—The MAX425 or MAX426 from Maxim enables you to vary low-drift input specs, *using a programmable commutating input switch and digital autozero loop.*



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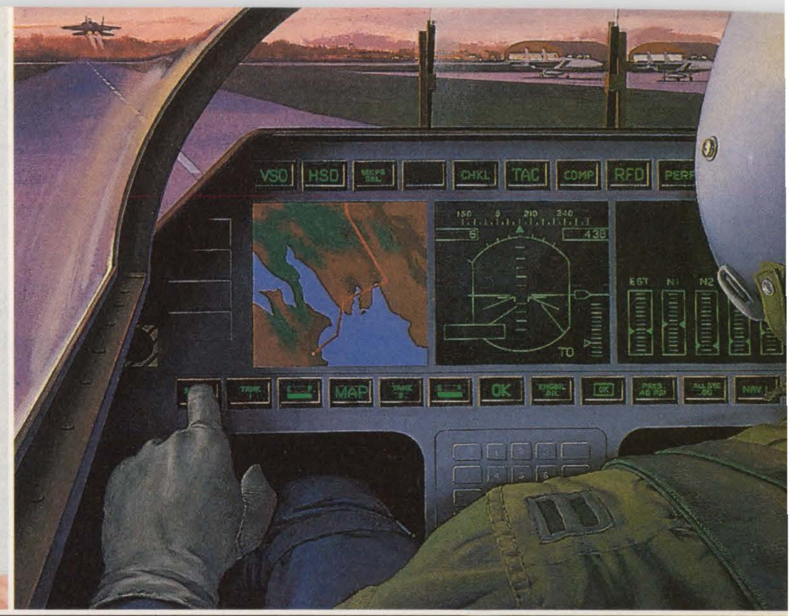

VSD
HSD
CHKL
TAC
COMP
RFD
MAP
OK

Low-drift op amps

all along a signal path from the op amp to the primary input signal. These junctions include every solder-joint, pin-to-socket and component-to-lead connection, relay contact, and any plug-in or screw termination. For example, the front-end dc amplifier circuitry of every bench DMM includes this series of parts.

Tot up the thermocouples

As a first objective in limiting thermal EMF effects, minimize the number of junctions and thermal gradients along the signal tracks. Balancing the number of junctions in series with the inverting and noninverting inputs of the op amp is another method. In some cases, this will mean designing in a few phantom components that have no use other than producing minute balancing EMFs in the signal path.

Op-amp designers achieve a high level of thermal balance within packages by maintaining a strictly symmetrical geometry on the die. Following this practice with your pc-board layout yields similar benefits. In most cases, in-series components conveniently develop opposing polarity EMFs at each end junction. But the orientation of the component is important in encouraging the EMF magnitude at each end to equate. Mount the part so that, wherever possible, heat generated within and around the part spreads uniformly throughout its body.

Junctions of different metals in the signal path are generally unavoidable. Most plastic-package op amps use Kovar, a copper alloy, for the lead-frame material. PMI warns you to expect 2 μV/°C from the Kovar-to-copper thermocouple where the op amp's lead connects to your pc-board track. Some lead frames use nickel alloy, and the corresponding TC is 18 μV/°C. Maxim helps you counter these effects by using a copper lead frame on its range of low-drift op amps.

Relay contacts are other notorious offenders, being housed in the comfort of warm energizing coils. Connecting two pairs of contacts in series and back to back is a useful technique for partially canceling EMF. Ideally, don't put relays in the signal path. If there's no other way, consider a latching relay.

If you mistrust Seebeck and his law of intermediate metals, then the composition of the solder you use is worthy of closer scrutiny. In most cases, the thermal gradient across a solder joint should be so low as to push any thermal EMF into the noise floor of your design. If you doubt this opinion, then follow advice from UK-based Multicore Solders Ltd and use a low-thermal solder. According to Multicore, changing from regular solder—60% tin and 40% lead—to a 70% tin and 30% cadmium solder limits thermal EMFs to 0.3 μV/°C—10% of the original value.

Whatever else you do to reduce thermal EMFs, eliminating temperature transients from the region of input circuitry is bound to yield dividends. Make sure your op amp doesn't drive heavy loads; in practice, just 7 mW dissipation in the op amp's output stages produces 1°C rise on the chip. Finally, surrounding the sensitive circuitry with draft screens gives any remaining thermal EMFs a chance to stabilize.

Tracing the rainbow's end

If you find yourself reduced to attempting to locate and measure invading thermal EMFs, then you may want to give up. This activity normally proves unrewarding and extremely time-consuming. Bear in mind each time you approach a junction with a measuring probe, you immediately alter the resident thermal EMF. Even if you manage to make a sensible measurement, you'll have to pretend that there are no additional EMFs at your probe tips. If you are going to exclude probes by soldering your measurement leads directly to the circuit, then do this just before coffee break, or, better still, before an extended luncheon. Once a hot iron has been anywhere near input tracks, thermal equilibrium takes at least 15 minutes to return. If, after all this rigmarole, you're still determined to have a go, then try using a simple analog readout microvoltmeter to make the measurements. The battery-powered Keithley 155 with a ±1-μV bottom scale is one of these.

Other evils threaten your low-drift design, especially if the signal's source resistance is high (for example, greater than 100 kΩ). In an instrumentation amplifier, or the front-end of a DMM, input current must be below 50 pA. A chopper op amp looks ideal, but the problem

Low-drift op amps

is to ensure that the op amp's input bias current flows from the signal input, and not from an undefined source elsewhere in the circuit.

Normally, one of the 15V power rails sits adjacent to the op amp's input pads. Any leakage inside, or across the surface of the pc board from the power rail to the high-impedance signal path, appears as voltage offset in series with the input signal. Dirty boards, or solder flux, encourage surface leakage. Even meticulously clean boards leak several hundred picoamperes, especially in damp conditions. The common answer is to surround pads for the sensitive input pins, top and bottom side, by an additional guard track on the pc board. To be effective, this guard must connect to a low impedance point that matches the voltage at the op amp's input pins. The guard rings divert stray leakage from the op amp's input. If a conformal layer of solder resist coats the pc board, then arranging to expose the guard track to air minimizes the chance of contaminants bridging the guard, especially in conditions of high humidity. Ideally, all component pads along the signal paths require guarding in this way. Alternatively, you can make all connections along the signal path off the pc board's surface by, for example, using high insulation standoffs. EDN

Reference

1. Linear Technology, George Erdi, "Design Notes, Number 42. Chopper vs Bipolar Op Amps—An Unbiased Comparison."

Article Interest Quotient
(Circle One)
High 485 Medium 486 Low 487

PSpice

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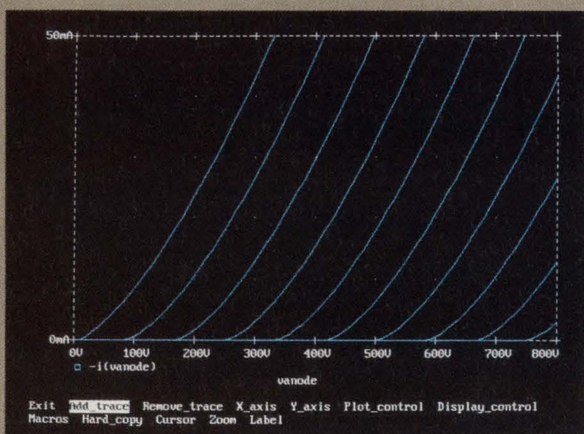

I-V curves of a triode vacuum tube

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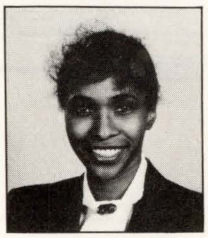
CIRCLE NO. 95

32-BIT BUSES

Battle between EISA and MCA continues



Technical differences between EISA and MCA are beginning to blur. For board designers trying to determine which bus deserves their allegiance, the deciding factor may come down to how easy it will be to sell their product.

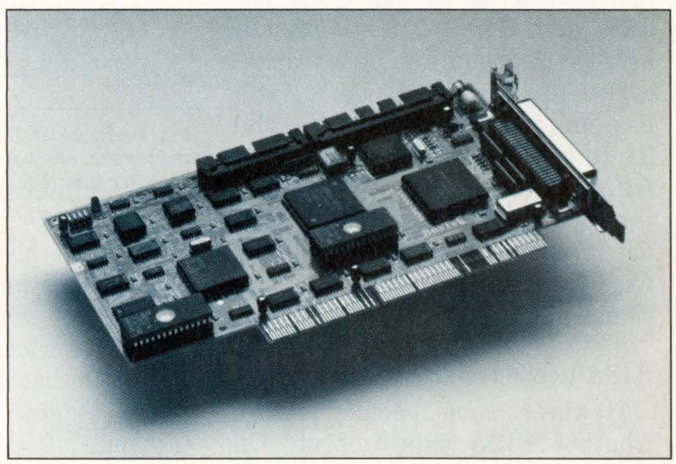
J D Mosley,
Regional Editor

As the smoke clears in the battle to establish 32-bit bus supremacy in the IBM PC arena, neither IBM's Micro Channel Architecture (MCA) nor the Extended Industry Standard Architecture (EISA) appear to provide board designers with any overwhelming arguments for pledging fidelity to either bus. The differences between the buses certainly are real, but the final evaluation reveals that the pros and cons offered by each bus give neither a discernibly superior technology.

Both architectures are suitable for combating the existing bandwidth bottleneck presented by the Industry Standard Architecture (ISA) found in IBM PC/AT and compatible computers. The 16-bit ISA bus limits data transfer to a maximum of 8M bytes/sec. EISA, the extended version of ISA, expands that to a 33M byte/sec data-transfer-rate under DMA control. MCA presently has a maximum bus-transfer-rate of 20M bytes/sec, but IBM can double that rate to 40M bytes/sec and has described future MCA modes that will permit data transfers of 80M and 160M bytes/sec.

Although at first glance MCA seems to offer data-transfer performance-potential that is superior to EISA, Richard Archuleta, Director of Advanced System Development for Hewlett-Packard, says the difference is minimal. The speed differential between the two buses exists because MCA uses a 10-MHz clock while EISA—for the sake of backward compatibility with ISA—uses an 8.33-MHz clock.

Currently available MCA-computers use an asynchronous 2-clock, 200-nsec address and data-transfer cycle that result in a 20M-byte/sec transfer rate. In contrast, the EISA spec has a 1-clock cycle that yields a maximum burst-mode data-transfer rate of 33 MHz, although normally the EISA bus also uses a 2-clock cycle that moves data at 16.6M bytes/sec.



You don't have to use a standard chip set to implement EISA or MCA. *Bustek Corp's BT-742A has a proprietary bus master ASIC for DMA and a SCSI-controller ASIC that reduces protocol overhead.*

The MCA performance upgrades announced in IBM's September 26, 1989 *Micro Channel Architecture Update* involve significant changes in the bus's components. IBM will execute the next-generation 40M-byte/sec transfer rate by reducing the number of necessary clock cycles with a streaming data-transfer. The address and first data-transfer will occupy a normal 200-nsec period, but subsequent data-transfers will happen in 100-nsec intervals, thereby making the transfer speed of the EISA and MCA buses roughly equivalent. **Fig 1** illustrates the anticipated improvements in MCA data-transfer.

To move data along at 80M and 160M bytes/sec by transferring 64 bits of data simultaneously, Archuleta says that IBM will have to abandon the TTL logic currently found in IBM PCs and switch over to the ECL family, which is much faster. However, he says, the high price of the technology is not practical for any IBM PC currently costing less than $20,000.

For 80M-byte/sec data transfers, IBM plans to multiplex MCA's 32-bit address bus so that it can also carry data. The 160M-byte/sec rate involves reducing the data-transfer cycles to 50 nsec. However, IBM has not yet demonstrated the ability to accomplish such rapid transfer rates. Archuleta is confident that when IBM can deliver these data-transfer rates, EISA will likewise improve its rates by using similar methods and components.

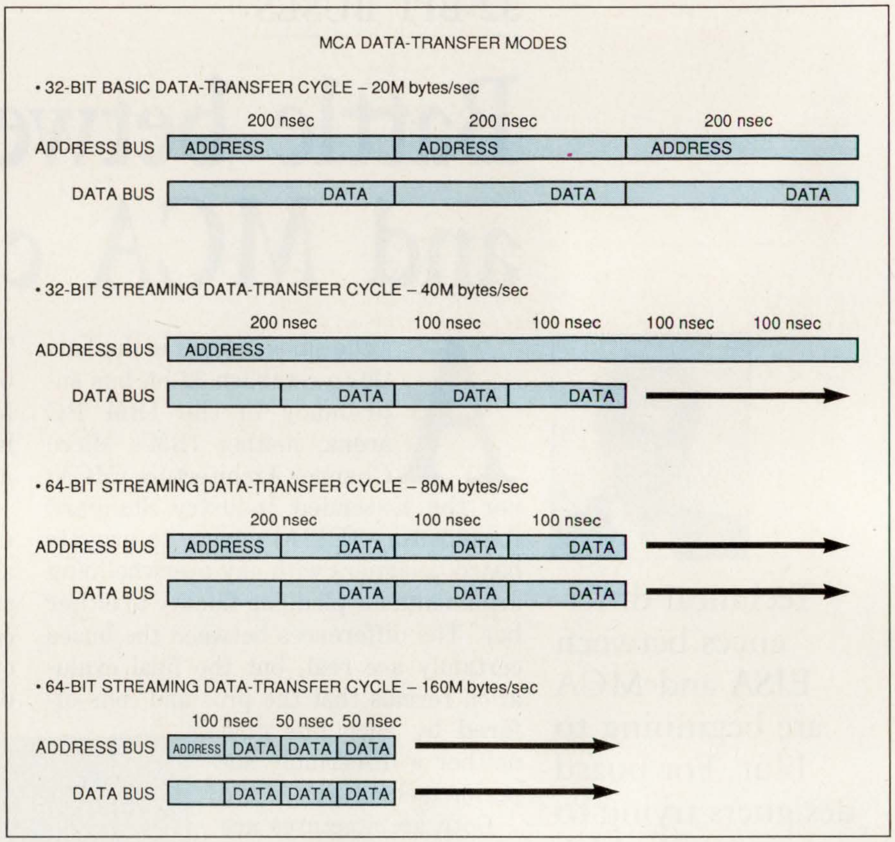


Fig 1—To boost MCA's data-transfer rate from its current 20M bytes/sec, *IBM plans to reduce the number of necessary clock cycles by using streaming data transfers for 40M bytes/sec and then multiplex the address bus for an effective 80M bytes/sec.*

EISA needs noise control

However, some people question whether EISA improvements will be so easily accomplished, citing the bus's inherent technological handicap of backward compatibility with ISA. Audrey Harvey, Engineering Manager for the Data Acquisition Division of National Instruments Corp, is concerned that at data-transfer rates exceeding 33 MHz, the EISA bus could produce unacceptably high levels of noise because of the relatively unsophisticated grounding scheme incorporated into the bus's ISA component.

Archuleta refutes that concern by noting the availability of currently unspecified EISA pins for future performance improvements and insisting that when the demand for more speed arises, the technology will meet that need.

Yet, amidst all this conjecture, the voice of reason points out that the real stumbling block to improved computational performance is not hardware constraints. Rather, it is the lack of proficient software.

Harvey is quick to note that DOS extensions are becoming de rigueur as software capabilities continue to exceed the restrictive boundary imposed by DOS's 640k-byte memory limit. The user expects to access much larger data buffers in an extended DOS environment, potentially causing interrupt latencies to increase to more than 100 μsec. This increase in interrupt latency occurs because many DOS system functions operate in real mode, and interrupts often require a mode switch. As a result, the 32-bit DMA control offered by EISA and MCA permits faster data-transfer throughput without an increased requirement for interrupt service.

However, Pete MacCormack, Texas Instruments' EISA Program Manager, notes that neither EISA nor MCA are "here" today: No software is available to fully exploit either bus's 32-bit capabilities. Furthermore, he says the bus advocates must prove their products are marketable—mere jousting with technical specs will not ensure either bus's longevity.

The "openness," or general availability, of each specification will

How MCA and EISA compare

Appreciating advancements in technology is often a simple matter of perspective. I remember sitting before my CP/M-based Osborne 1 computer in 1982, staring in amazement at an ad for a *5M-byte* hard-disk drive, and wondering why in the world would anyone want to shove that much (presumably valuable) data onto one (presumably fallible) storage device. Less than a decade later I'm chomping at the bit for a 200M-byte drive and wishing I could afford one with even greater storage capacity.

The same sort of performance scenario unfolded when ISA evolved from the 8-bit IBM PC/XT bus to the IBM PC/AT's longer 16-bit slot. Although 8-bit expansion boards still remain popular for such simple functions as modem communication or serial and parallel data I/O, a vast number of 16-bit cards currently provide the necessary high-performance data transfers required for complex graphics, number crunching, and LAN functions.

In 1987, IBM introduced a bus for its PS/2 line of computers—the Micro Channel Architecture, which promised workstation performance for desktop computers by specifying a 32-bit-wide data-transfer path, bus mastering, automatic system configuration, and 20M-byte/sec throughput. However, this architecture is completely incompatible with IBM's PC line of computers. And IBM PC users who make the MCA upgrade must abandon their existing investment in plug-in boards and software.

In response, a consortium of companies led by Compaq Computer Corp proposed EISA, an alternate 32-bit architecture that extended—rather than replaced—the 16-bit IBM PC/AT bus. Use the following table to compare and contrast the benefits offered by these two competing bus specifications.

MCA benefits

- Proposed technical advancements can provide data-transfer rates reaching 160M bytes/sec. MCA's current transfer rate is 20M bytes/sec.
- Completely redesigned pinouts in MCA connectors provide a ground for every four signals to minimize signal crosstalk.
- MCA has a 10-MHz bus clock.
- Micro Channel uses asynchronous transfer timing, thus simplifying timing considerations.
- MCA uses a distributed and prioritized arbitration scheme that operates in a serial fashion. Bus Master priority is dictated by the system, or you can optionally implement an "equal and fair" priority procedure.
- DMA transfers occur in a serial fetch-and-deposit manner.
- MCA plug-in-board configuration is strictly a programmable function with critical setup parameters stored on board in battery-backed RAM. IBM assigns unique ID numbers to each board manufacturer's plug-in card, thus permitting the system to correctly identify any board, regardless of its slot location.
- MCA's spec provides for options like video functions and sound or music.
- Within MCA, the CPU cannot even access its own memory when another device controls the bus. However, MCA's prioritized bus arbitration scheme provides CPU control.
- MCA implements a level-sensitive interrupt line that prevents the computer system from crashing, as can happen when edge-triggered peripherals or devices get hung up as a result of noise on the interrupt line, creating spurious signals.
- MCA expansion cards contain 36 in.^{2} of board space, 58 or 89 pins, and 1.6A per slot. However, these cards exhibit superior EMI characteristics due to their numerous power and ground planes.
- MCA is proprietary—IBM controls documentation, improvements, and enhancements centrally.

EISA benefits

- Current maximum data-transfer rate of 33M bytes/sec.
- EISA's connector pinout intersperses grounding between the existing ISA pins to maintain and improve upon backward compatibility.
- EISA's 8.33 MHz clock maintains backward compatibility with ISA.
- EISA employs synchronous transfer timing to maintain backward compatibility with ISA.
- EISA uses a centralized arbitration scheme that operates in a parallel fashion with a time-sliced, "equal and fair" priority procedure.
- DMA transfers occur in a parallel flyby manner.
- You can either configure EISA plug-in boards using physical jumper switches, or program them using software configuration files supplied by the board manufacturers. Each EISA expansion slot has an assigned address so that you can use multiple identical boards without I/O conflicts. Every EISA board manufacturer has a special 3-character code used as a prefix to create a unique identification code for each board.
- EISA has undesignated pins that can accommodate additional features in the future, as needed.
- EISA utilizes cache memory in such a way that the CPU can continue to work, even when another device controls the bus.
- EISA lets you program each interrupt individually for either edge- or level-sensitivity, which maintains compatibility with ISA's edge-triggered interrupts But you must be careful not to mix devices using different interrupt schemes on the same channel.
- EISA boards are 58 in^2 and provide 4.5A per slot.
- EISA is an open spec. Improvements and enhancements are contingent upon agreement by the EISA consortium. Anyone can obtain documentation describing every aspect of this architecture.

32-Bit Buses

have an impact on its broad acceptance among designers. Until the EISA spec was finalized, interested designers had to pay $2500 and sign a nondisclosure agreement before taking a peek at the proposed specification. Today, however, you can contact BCPR Services at (202) 371-5921 and pay $125 for a copy of the spec, or $450 for the spec, one year of updates, and access to the EISA Forum electronic bulletin board.

IBM provides copies of portions of the MCA spec free of charge. Anyone can obtain aspects of the spec not covered by IBM patents by calling the Software Publications Hotline at (800) 327-5711. You can also obtain a complete list of IBM PS/2 hardware publications by calling the Technical Directory at (800) 426-7282.

According to IBM's Mike Ryder, if you want to build computers for the MCA, you have to license the technology from IBM and pay a royalty fee of 2% for each mother board you sell. However, plug-in boards for the MCA are not constrained by any of IBM's patents, so manufacturers pay nothing to be added to IBM's list of preferred developers, thereby gaining access to the spec and any subsequent updates.

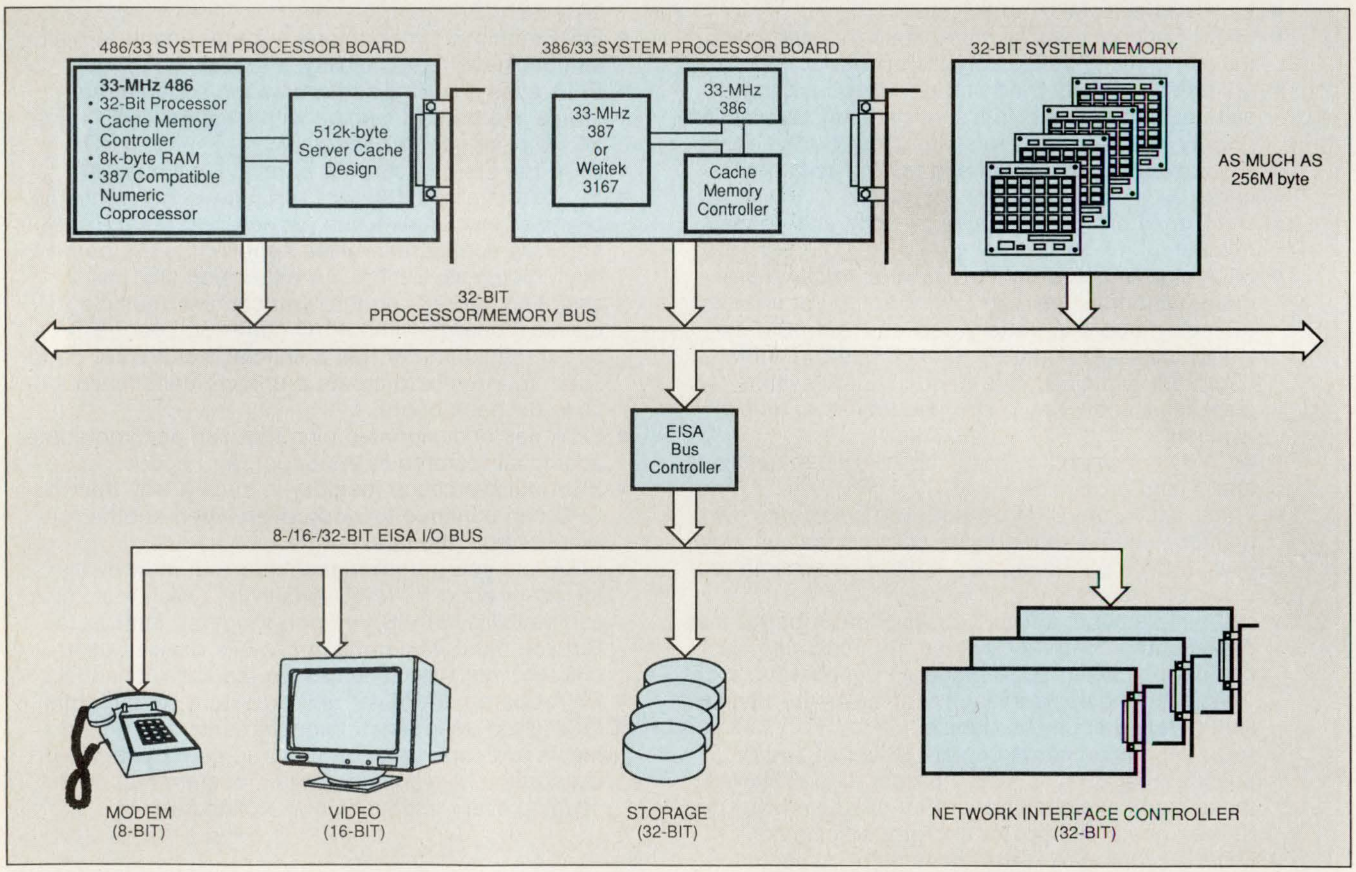
Chip sets simplify designs

From a plug-in board-designer's point of view, both EISA and MCA provide straightforward development paths because of the availability of chip sets for intelligent bus control, buffering, and DMA. Intel, the first chip manufacturer to introduce chips for EISA and MCA, also provides chip sets for these specs.

Intel's 82350 EISA chip set comes in a $90 (1000) 25-MHz and a $109 (1000) 33-MHz version, each of which includes the company's 82357 integrated system peripheral and 82358 EISA bus controller. You can also purchase an optional $16 (1000) 82352 EISA bus buffer that replaces 17 TTL glue-logic chips to further simplify your circuit.

Early this year Intel will announce a version of the 82350 EISA chip set that will reduce the number of chips necessary to manufacture a mother board from 90 to 100 chips down to about 40 chips. The chip set will not only lower the overall cost of producing a mother board, but will shrink the size of the board to a "baby AT" form factor.

Intel's $32.50 (1000) 82355 EISA



Complementing the EISA bus with a 32-bit processor/memory bus *called the Flex/MP, Compaq's Systempro Model 486/840 has two system processors that simultaneously operate from their memory caches.*

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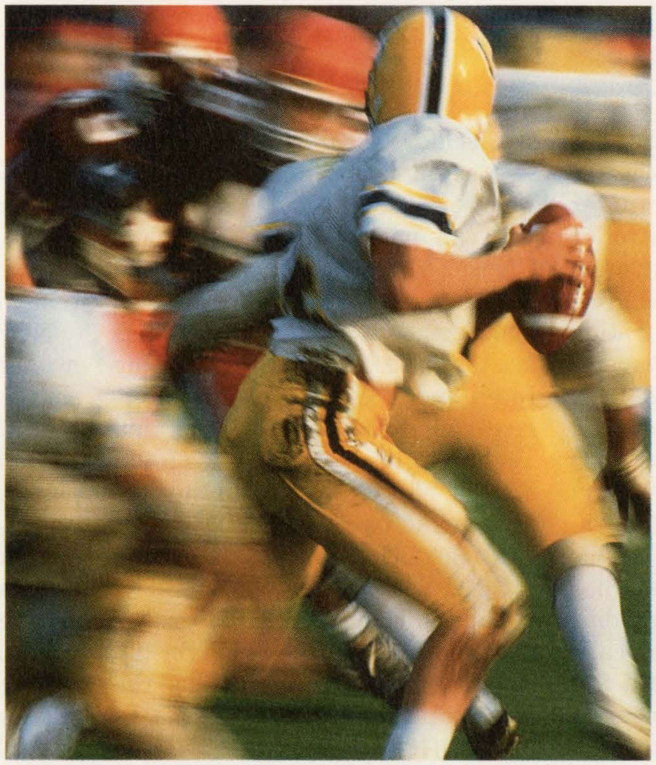

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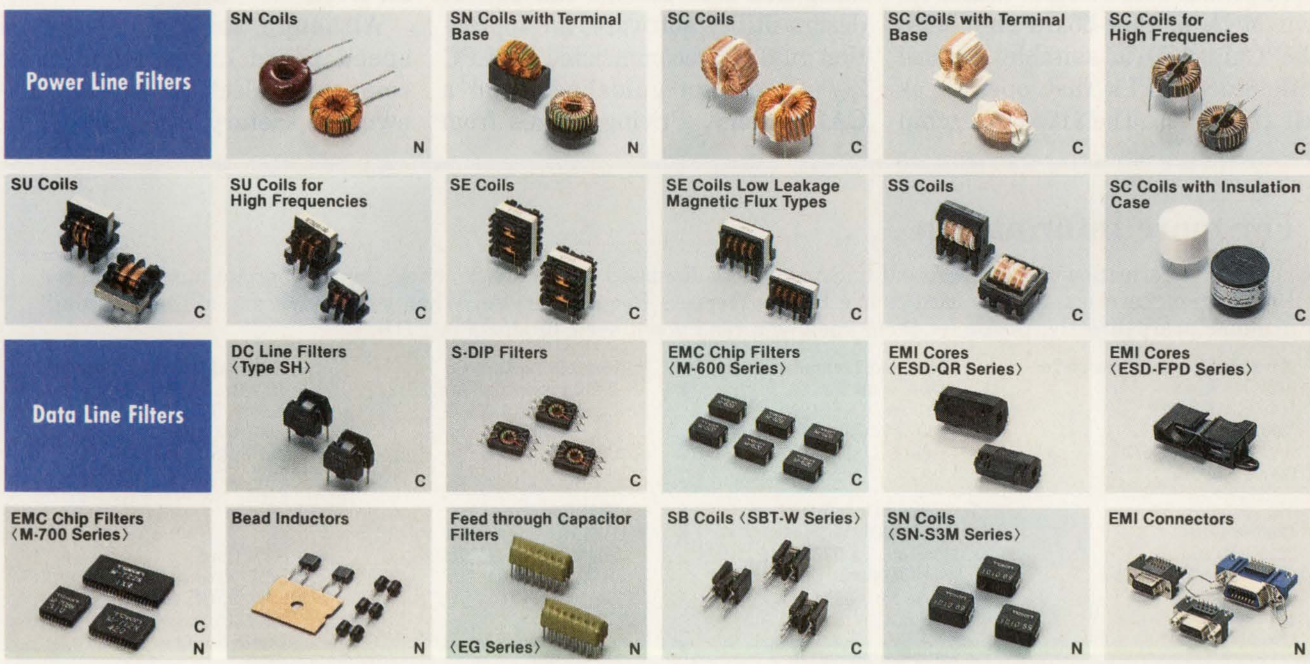

N: Normal mode C: Common-mode

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32-Bit Buses

bus master interface controller for designing plug-in boards integrates the EISA, CPU, and transfer buffer interfaces. The controller automatically administers such EISA bus master protocol as cycle timing and execution, arbitration and pre-emption, and byte alignment.

For MCA mother boards, Intel sells a chip set manufactured by IBM. The set includes two local I/O channel-support chips (82303 and 82304), a DMA controller and central arbiter (82307), an MCA bus controller (82308), an address bus controller (82309), and a floppy-disk controller (82077AA). Intel calls this set the 82311 and sells a $71 (1000) 16-MHz 80386SX version, an $89.50 (1000) version for the 20-MHz 80386, and a $133 (1000) 25-MHz set for 80386 and 80486 CPUs.

Chips and Technologies makes its own MCA mother-board chip sets. The Chips/280 is suitable for use with 80386 CPUs that operate as fast as 33 MHz. The $173 (1000) chip set includes BIOS, VGA graphics, two serial ports, and one parallel I/O. For 80386SX and 80286 CPUs, you can purchase the $94 (1000) Chips/250 chip set.

For plug-in boards, IBM also makes the $45 (1000) 82325 bus master interface, which is sold by Intel, and a $21 (1000) slave interface called the 82326. Chips and Technologies sells a $40 (1000) 82C614 Microchips bus master interface and two $20 (1000) slave interfaces: the 82C611 and the 82C612, with DMA.

Capital Equipment Corp makes its own MCA interface chip for designing expansion boards called the One Chip Plus (88C01), which sells for $34 (100) or $27.50 (1000). The company also offers development packages for I/O and memory card designers that include the 88C01, design-utility software, an application guide, a recommended IBM PC layout, design guidelines, and a CAD library. Pricing ranges from $495 for a basic I/O package (03000-50100) to $995 for a combined I/O and memory package (030000-50300) that includes background or foreground control for data acquisition and other I/O functions.

NCR offers a $36.25 (1000) bus mastering host-interface controller-chip, called the 86C05 Micro Channel/EISA/AT/Nubus. Plug-in board designers can use this chip to support multiple architectures without redesigning the host-interface logic, an effort that NCR officials estimate as 75% of the total hardware and firmware application-development task. The chip facilitates 20M-byte/sec data-transfer rates and includes a 32-word × 32-bit FIFO-buffer for 8-, 16-, or 32-bit transfers to host memory. The board also contains a programmable 8- or 16-bit DMA interface.

Although such chip sets can speed board development, some companies elect to develop their own proprietary circuits to inter-

For more information . . .

For more information on the MCA and EISA products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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face with the bus. For example, Bustek Corp makes a family of EISA and MCA bus master products that contain proprietary ASICs for SCSI peripheral control.

The company's BT-742A 32-bit EISA bus master SCSI-host-adapter includes a bus master ASIC that contains a 128-byte FIFO for 32-bit bursts of data at the maximum rate of 33M bytes/sec. The board's 32-bit addressing range allows direct access to more than 4G bytes of main memory in the host computer. In addition, the BT-742A's SCSI-controller ASIC reduces protocol overhead by performing common algorithms or sequences in response to SCSI-2 commands. The board sells for less than $500 in OEM quantities.

Data Technology uses a proprietary DMA controller and a 32-bit custom RISC μP in its DTC6290E EISA/ESDI disk-drive controller board. The board controls as many as four 15M-bps ESDI drives and as many as three floppy-disk drives. Performing most hard-disk access operations in less than 0.5 msec, this $895 bus master can also transfer data without using the host CPU.

It's a matter of volume

The infrastructure that will pave the way for your next 32-bit bus design is currently in place. However, which spec will emerge as the architecture of choice remains an unanswered question. Based on the volume of interest designers have shown, MacCormack predicts that EISA will be the dominant 32-bit architecture by 1992. Accordingly, Texas Instruments expects to introduce an EISA chip set this year, believing that demand for the chips will be sufficient to reduce the price enough to effectively compete with ISA. And as the price of the chip set falls, the cost of complete systems will follow.

A battle still rages between proponents of EISA and MCA over the merits of each bus despite the minimal differences between the two architectures.

Even now you can purchase an EISA computer from Advanced Logic Research for $1995. The company's Businessveisa model 101 has a 33-MHz 80386 CPU and 1M byte of RAM, and the company offers a 25-MHz 80486 CPU upgrade for $1995. The company makes an MCA-based 33-MHz 80386 computer called the Microflex 3300 that has a base price of $5795, but includes 2M bytes of RAM, a 70M-byte hard-disk drive, a 1.44M-byte 3½-in. floppy-disk drive, a parallel port, a mouse port, and a serial port.

IBM has announced the $16,695 Model 90 and $17,745 Model 95 PS/2 computers that use the MCA's 20M-byte/sec data-transfer rate. However, they boost system performance with a 33-MHz 80486 CPU nestled in an extendible processor "complex" that resides on a plug-in board, rather than on the motherboard. Therefore, you can upgrade the CPU to accommodate advances in future technologies. These computers also include a video bus master—the XGA Display Adapter/A, which is compatible with the existing 640×480 VGA video standard, but boosts screen resolution to 1024×768 in 256 colors.

There will always be a few individuals who insist that the EISA vs MCA debate is much ado about nothing—that IBM PC performance in excess of 40M bytes/sec will create more noise and data integrity problems than it could possibly resolve. Yet, enterprising designers have met and overcome every technical obstacle presented during the evolution of personal computing, and will presumably continue to do so.

Both EISA and MCA offer a logical 32-bit path, and neither seems to have a significant technological edge. Ultimately, MCA board manufacturers will find their fortunes inexorably tied to IBM's marketing clout, while EISA will most likely give board designers a more diverse, but also more cost-conscious, market. EDN

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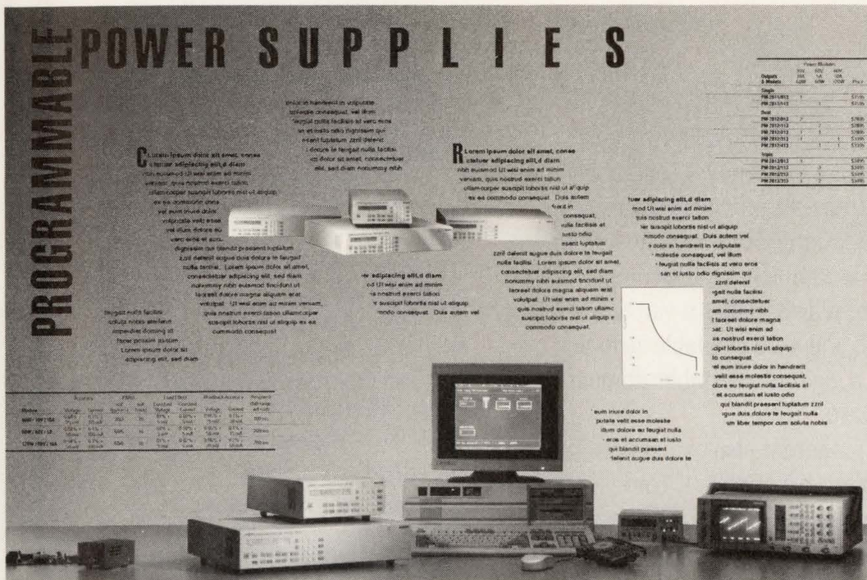

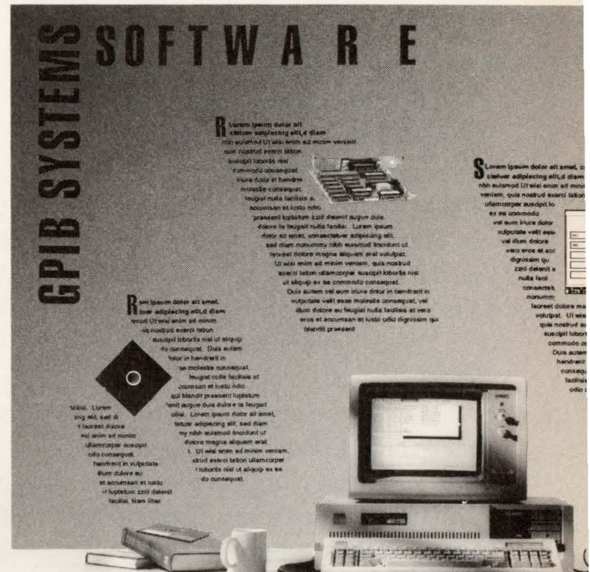

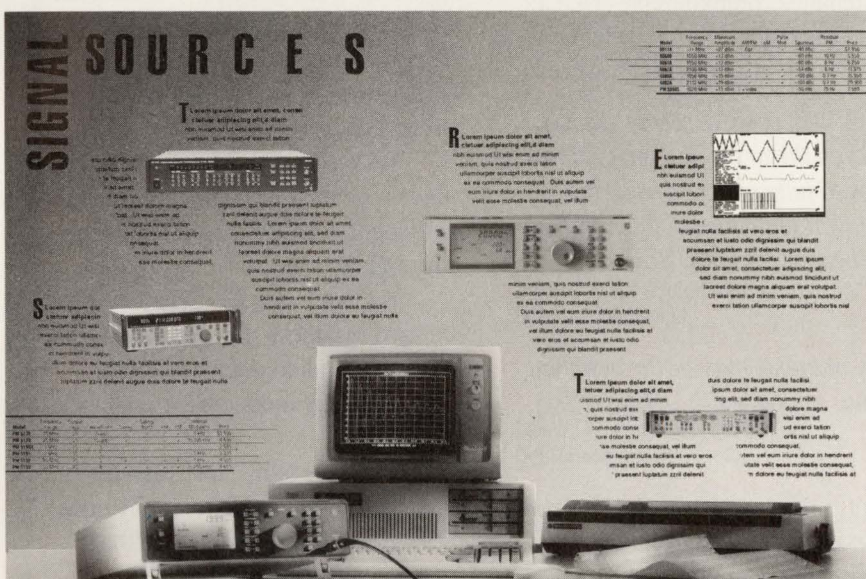

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EDN EDITORS' CHOICE INNOVATION

Real-time Unix-like operating system implements Posix 1003.4 extensions

Version 2.0 of the Unix-compatible Lynxos real-time operating system implements the complete set of real-time extensions specified in IEEE Posix 1003.4 (also called Posix.4). The Posix.4 standard makes possible real-time applications that can run on systems and processors from multiple vendors. Lynxos 2.0 also offers compatibility with threads, a form of lightweight tasks defined by Posix.4a.

Lynxos 2.0 provides the following features defined in Posix.4 extensions:

- Binary semaphores
- Process memory locking
- Shared memory
- Priority scheduling
- Asynchronous event notification
- High-resolution timers
- Interprocess communication
- Asynchronous I/O
- Synchronized I/O
- Contiguous real-time files.

The priority-scheduling facility provides several priority-driven scheduling policies including first in/first out. The timers in Lynxos go far beyond Unix timers and have nsec resolution for both absolute- and relative-timing operations.

Posix.4a defines the use of threads as a more efficient way to set up multiple concurrent execution paths within a task than the use of processes. Multiple threads within a process share address space and require less context information than a process. Thus, an operating system requires less CPU and memory resources to start, stop, or switch between threads. Lynxos 2.0 fully supports the Posix.4a threads concept and the thread model implied by Ada tasking.

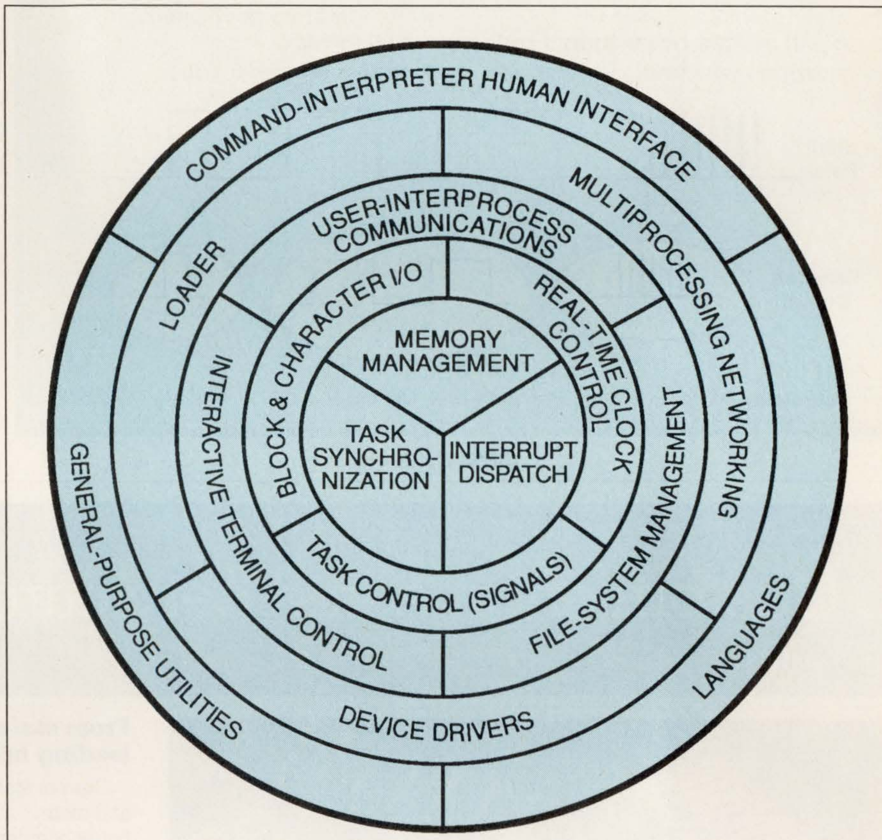

Fig 1—The task-control and scheduling capability *built into Lynxos 2.0 allows the real-time operating system to respond quickly to external events; yet the software maintains binary compatibility with System V Unix.*

Although compatible with Unix and Posix.4, Lynxos is a real-time operating system developed with no Unix System Laboratories (AT&T) code. **Figure 1** depicts the structure of Lynxos. The operating system can respond to an external event in <450 μsec, worst case, when running on a 20-MHz 80386-based system. The specified worst-case response time includes interrupt disable, dispatch, interrupt routine execution, pre-emption disable, scheduling, context switch, and return system call. The company also guarantees the specification on systems with disk drives and networks.

You can also place Lynxos in ROM for embedded applications, yet the operating system supports demand-paged virtual memory and offers compatibility with Unix Sys-

EDN EDITORS' CHOICE

tem V interprocess communications facilities. The operating system also offers binary compatibility with shrink-wrapped application software for Unix such as Wordperfect.

You can buy Lynxos for a number of popular μP families including the Intel 860, 80386, and 80486; the Motorola 680X0 and 88000; and the Mips R3000 and R6000. A version for IBM PC/AT compatibles costs \$1495. You can also buy a number of options such as X-window support, the Motif graphical user interface, and TCP/IP network support. An IBM PC-compatible development kit for ROM-based systems costs \$2995.—***Maury Wright***

Lynx Real-Time Systems Inc, 16780 Lark Ave, Los Gatos, CA 95050. Phone (408) 354-7770. FAX (408) 354-7085.

Circle No. 736

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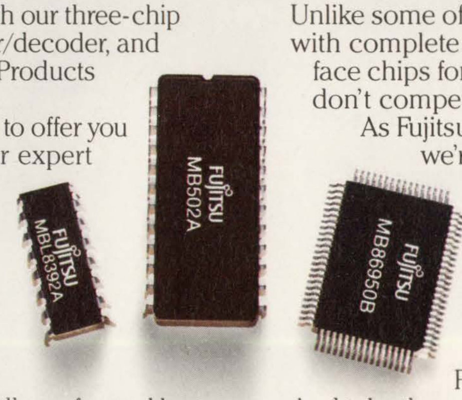

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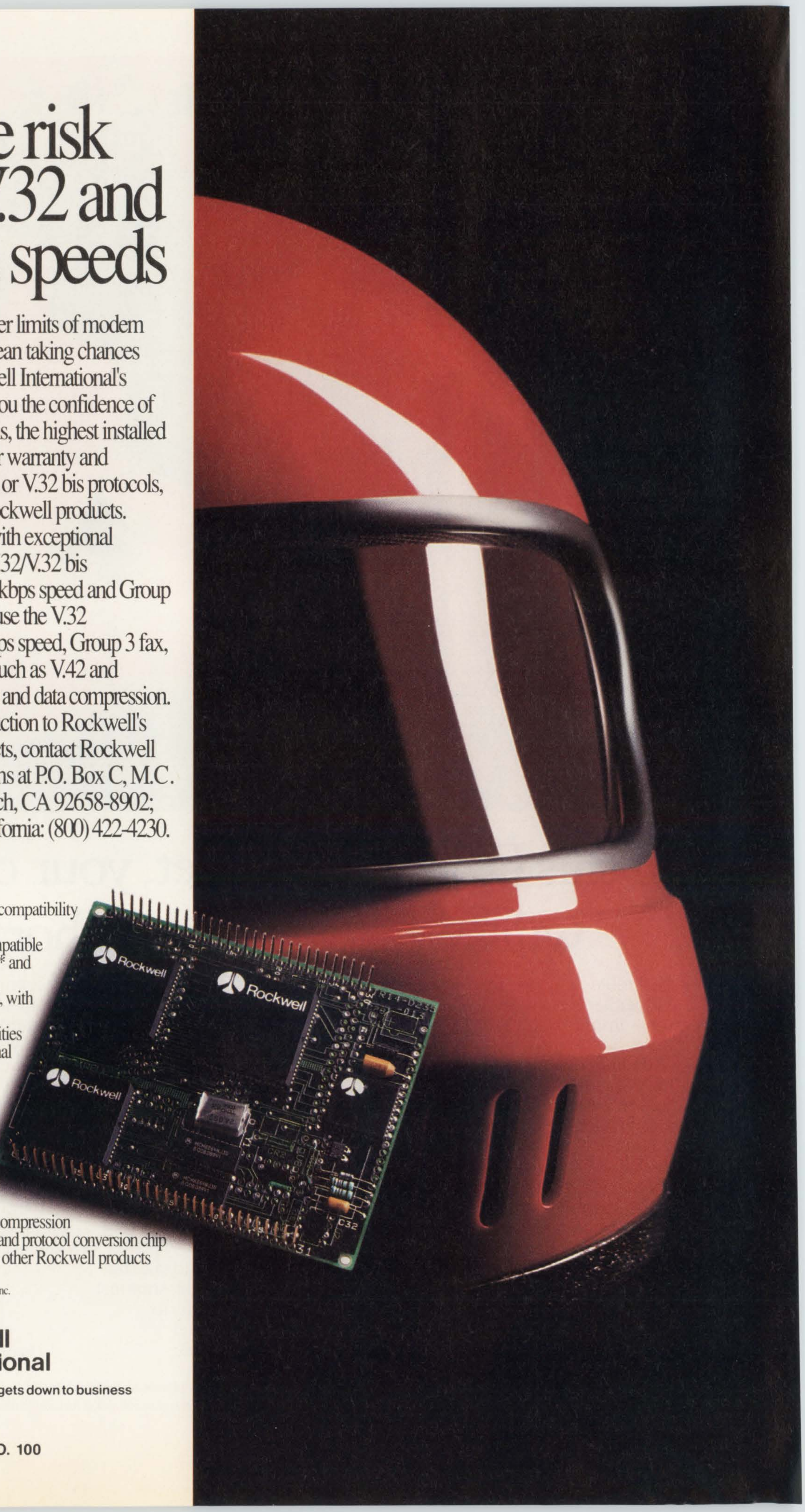
CIRCLE NO. 99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EDN EDITORS' CHOICE
INNOVATION

Voice-storage chip supplies nonvolatile analog memory

Today, voice-storage devices have become standard products. They're fairly easy to use and many manufacturers offer them, but the technology is basically the same—digitize a signal, store it, and play it back. Now, however, a small start-up company offers a voice-storage chip that requires neither an A/D nor a D/A converter. Instead, the ISD-1016 chip relies on analog memory.

Charge-coupled devices have supplied analog memory for years, but their ability to save information depends upon a constant source of power. However, this chip relies on nonvolatile memory cells that use a proprietary CMOS/EEPROM technology to store charges in a RAM arrangement. Thus, the chip requires no backup power supply to maintain its analog information—the chip draws 10 μA of standby current only because it contains other circuitry.

The device operates from a 5V power supply, and it requires few external passive components—resistors and capacitors that control filtering and automatic gain-control characteristics. Distortion is about 2%. The chip requires no external crystal or clock signal.

Applications are typical for voice-output products: phone-answering equipment, portable telephones, pagers, emergency equipment, and alarms. Because the chip's price is \$16 (1000), it should start to appear in such applications fairly soon. The chip can deal with all types of analog information, not just speech or music. For example, it can store test waveforms, sample analog signals, store correlation data, and hold filter coefficients. The company's CMOS/EEPROM technology may also find a use in neural-network chips in which the weighting values for individual neurons are stored analog values rather than binary (digital) values.

The chip stores as many as 16 sec of speech, and you can cascade as many of the chips as you need to extend a message's length. Because the chip uses a RAM structure, you can access portions of a message or divide the 16-sec interval into subintervals and several shorter messages. To record a message, a microphone connects directly to the chip. The chip's output also drives a small speaker directly, although you might use a small external audio-amplifier IC in some applications. You can order the voice-storage chip in a 28-pin DIP or in a 28-pin plastic leadless chip carrier.—***Jon Titus***

Information Storage Devices Inc, 2332B Walsh Ave, Bldg G, Santa Clara, CA 95051. Phone (408) 562-9550. FAX (408) 562-9559.

Circle No. 733

VME64 68040-based single-board computer supports 32M bytes of dynamic RAM

The SV430 CPU board's compliance with the VME64 bus spec and a 68040 host µP make this board well suited for high-performance Unix or real-time system applications. The board accommodates as much as 32M bytes of interleaved dynamic RAM. Also, its 68030 µP acts as an auxiliary processor that controls communication, disk, and other I/O operations.

The 68040 µP provides the SV430 board with 19 to 25 MIPS of power, depending on your choice of 25- or 33-MHz ICs. The processor includes dual 4k-byte instruction and data caches, a 68882-compatible floating-point unit, and an integrated memory-management unit. After more than a year's delay, Motorola has just begun to ship the chips in volume.

The CPU board can perform VMEbus block transfers as fast as 66M bytes/sec using the 64-bit wide data path described in the new revision D VMEbus spec (commonly called VME64). But the board maintains compatibility with standard 32-, 16-, and 8-bit VMEbus boards, and supports 33M-byte/sec block transfers at 32 bits. The board performs 10M-byte/sec VMEbus transfers during standard shared-

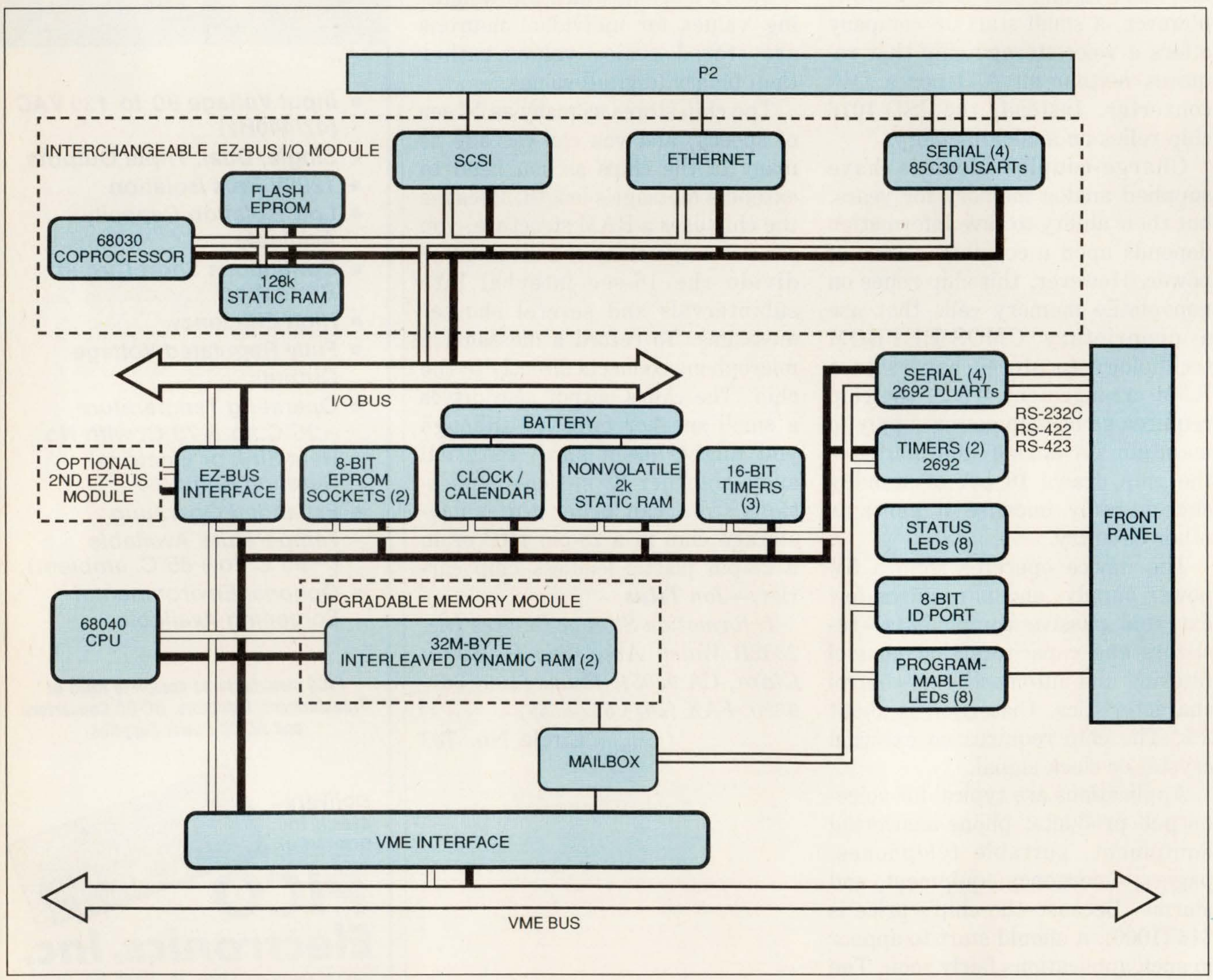
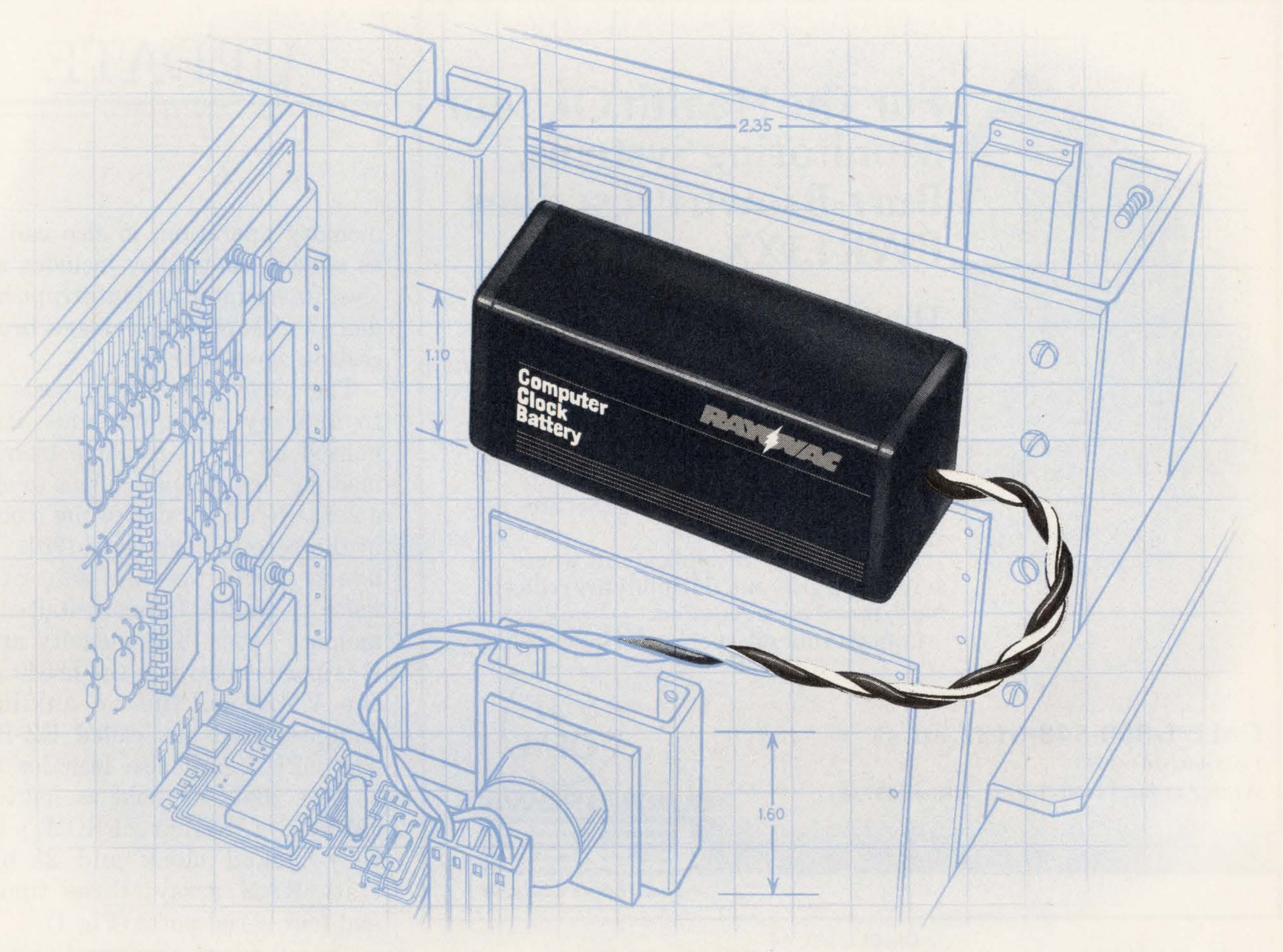


Fig 1—The 68040 µP and memory, *combined with the 68030-based EZ-Bus I/O modules, make the SV430 a true single-board computer. This computer allows eight users to run Unix via serial ports.*



WHY MORE COMPANIES ARE PLUGGING US INTO THEIR DESIGNS.

Today the Rayovac 844 computer clock battery is specified by 23 system architects worldwide. Its proven reliability safeguards the configuration file memory in 286/386/486 personal computer products, especially in power-down situations.

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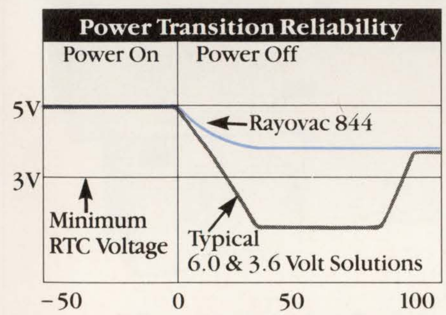

The 844 ensures IC voltage above the critical 3.0V level maintaining clock stability and configuration file memory.

The 844 is compatible with industry standard chip sets: Chips & Technology; VLSI Technology; Western Digital; Zymos and Intel. And it's made in the U.S.A., with on-time delivery available around the world.

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memory operation; it also can act as system controller, includes a 7-level interrupter and interrupt handler, and supports message broadcasting across the bus.

The basic CPU board hosts 2M to 32M bytes of dynamic RAM housed on an upgradable memory module. The company plans to offer a static-RAM version of the module in the second quarter of 1991. The board performs one-wait-state memory writes and zero-wait-state memory reads. The memory array is triported between the 68040 μP, the VMEbus, and an auxiliary daughter-card bus called EZ-Bus. The CPU board also includes two sockets that can hold as much as 1M-byte of ROM or EPROM, a battery-backed clock and 2k-byte static-RAM array, three timers, and four serial ports (**Fig 1**).

The standard configuration's single EZ-Bus daughter card handles I/O operations. A 68030 μP, operating as an auxiliary processor to the 68040, controls the I/O operations. The EZ-Bus module includes a SCSI bus, an Ethernet network connection, and four serial ports, all of which are connected to the VMEbus P2 connector. The module also includes buffer memory and 128k bytes of flash EPROM. You can also add a second EZ-Bus module; the company offers a number of daughter cards, such as cards for Arcnet networks or ESDI disk drives.

You can buy Unix System V release 4.3 for the board or choose from a number of real-time operating systems such as Ready Systems' VRTX, Microware's OS-9, and Wind River's Vxworks. The SV430, with a 25-MHz 68040, costs $4605.—***Maury Wright***

Synergy Microsystems Inc, 179 Calle Magdalena, Encinitas, CA 92024. Phone (619) 753-2191. FAX (619) 753-0903.

Circle No. 737

TAKE SOLDER PASTE AND DIPPING OUT OF CIRCUITS ASSEMBLY

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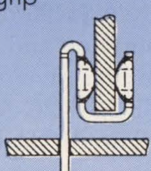
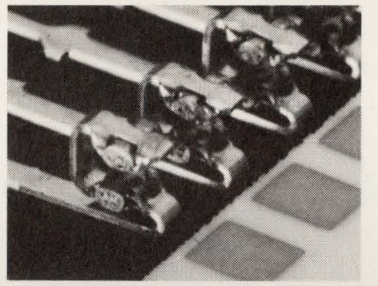
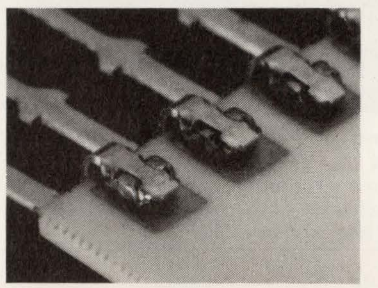


When you use NAS solder and flux bearing edge clips, expensive rework becomes virtually a a thing of the past.

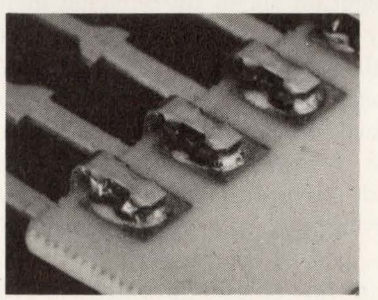
The simple, efficient method of applying NAS solder and flux bearing edge clips:



Direct contact between solder preforms and conductor pads produces a beneficial wiping action as clips are attached, either manually or with a lead attachment machine.



Interference fit holds clips firmly in position for reflow. Top and bottom preforms are reflowed in one operation using any method that raises temperatures to reflow levels.



Precise amounts of the right solder and the shape of the "Claw" grip provide control of solder flow without a solder stop. This assures perfect mechanical and electrical bonding without wicking or bridging.

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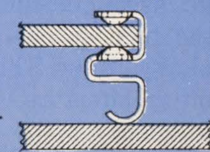
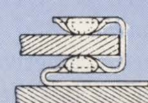


NAS offers a large selection of edge clips, including .100, .075 and .050 centerlines for both through-hole and surface mounting of SIP, DIP, Quad and Multi-chip devices. Our surface mount clips are the most effective solution to the problem of thermal mismatch, and are available in a variety of types. Ask about our Compliant "J" surface mount designs with .025 and 1mm centerlines.



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CIRCLE NO. 108

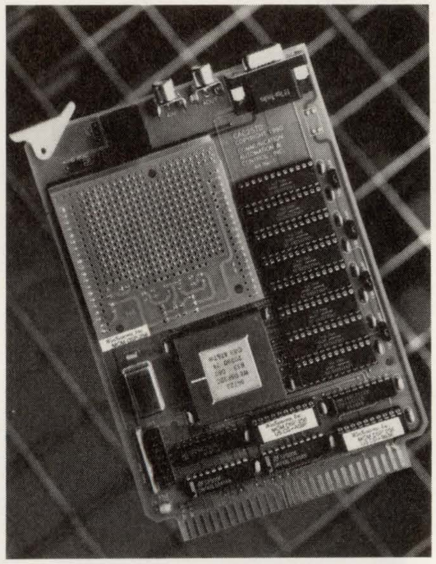
STD Bus DSP board delivers 25M flops and 3.5M-byte/sec data transfer

The MCM-DSP32C single-board processor can handle computation-intensive embedded applications at the high speed of a DSP chip. It plugs into an STD Bus, and its 32-bit architecture operates at a clock frequency of 50 MHz. This board can execute a 1024-point FFT in 3.3 msec, multiply two 4×4 matrices in 6.16 μsec, and compute the response of a complex adaptive FIR filter in real time at 80 nsec/tap.

The board contains AT&T's fastest floating-point processor, the 25M-flops DSP32C. Featuring four 40-bit accumulators, 22 general-purpose registers, and 6k bytes of internal RAM, the CMOS device is also compatible with IEEE's STD 754 floating-point format.

One of the chip's most attractive attributes, however, is its instruction set—all instructions execute in a single cycle. Conditional branching and conditional ALU operations simplify your programming task and permit efficient, compact coding. A data-stationary-coding feature enables parallel operation of arithmetic and logic functions and provides automatic pipeline control.

This DSP board provides a data-transfer rate of 3.5M bytes/sec due in part to its I/O-mapped interface, which transfers data to the STD Bus three times faster than a memory-mapped alternative could. The interface automatically senses and selects 8- or 16-bit data transfers, or you can slave the I/O so that on-board functions occur independently of the host STD Bus CPU. When you operate the board in this way, the DSP chip continues calculating even during the data-transfer process.



Based on AT&T's 50-MHz DSP32C processor, *the MCM-DSP32C single-board DSP chip accelerates your computation-intensive applications by operating independently of the host system's CPU.*

Using its ability to address 32 bits of memory at 4 times/cycle, the AT&T chip minimizes your code's execution speed by reducing memory-access bottlenecks. A byte-addressable address space provides storage for 8- and 16-bit data. The board interfaces to external devices and daughter boards via its serial and parallel ports. For optimal throughput, the chip performs 8-, 16-, and 24-bit integer conversions. And for telecommunications or speech applications, you can rely on this device to do μ-Law and A-Law conversion.

You can purchase a $395 source-level debugger called the D3EMU. Featuring a windowed user interface, this debugger lets you display and modify memory contents by scrolling or paging through your code. Windows display both the D3EMU's high-level, C-like language source code and the corresponding assembly-language instructions. You also receive a run-time function library, as well as a set of utilities and sample programs such as a hex converter and a voice-recording demonstration.

A $495 software-support library, dubbed the WEDSP32C-SL, has an assembler, a link editor, a simulator, and other utilities. You can also buy a $1495 optimizing C-language compiler and a $95 library of application routines called the WEDSP32C-AL.

The MCM-DSP32C DSP board with a maximum of 256k bytes of zero-wait-state RAM costs $1795. With 64k bytes of RAM, the board sells for $1495. An onboard adapter lets you plug in a daughter board, such as the $295 DBCS5339. The daughter board contains 16-bit, dual-channel, 48-kHz delta-sigma A/D and antialiasing filters for spectral-analysis and filtering applications.

Other daughter boards include the $195 DBT7525, which provides an 8-kHz, 16-bit, single-channel, pulse-code-modulating Codec for use in telecommunications applications. A $145 DBserial board offers an interface to the DSP32C's serial I/O channel. And a $95 DBproto board lets you design special-purpose interface electronics.

—J D Mosley

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Circle No. 735

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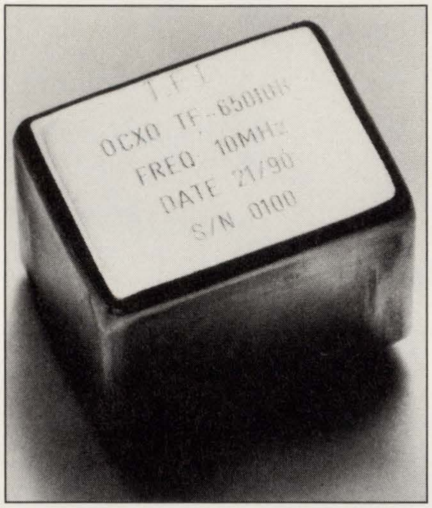
CIRCLE NO. 104

Compact crystal oscillator features 2×10^{-7} stability

The Model TF-65010-B crystal oscillator is available with a TTL-compatible, square-wave output anywhere in the frequency range of 1 to 20 MHz. Housed in a package measuring $1.38 \times 1.06 \times 1$ in., the unit utilizes oven-like compensation techniques to achieve a temperature stability of 0.2 ppm over a −20 to +70°C operating range. In addition, it reaches this stability level in 2 minutes, drawing 3W, which is far less power consumption than the typical oven-controlled oscillator would require. Thus, the oscillator opens up a number of high-stability applications that you would have previously avoided due to cost.



A ±0.2 ppm temperature stability is a key feature of the TF-65010-B crystal oscillator. The device achieves this stability performance without the use of oven control techniques. As a result, warm-up time measures 2 minutes, and power consumption is 3W.

Because the unit does not employ classical oven control for compensation, it reacts to temperature variations in real time, and it has no hysteresis characteristics. Phase noise at 10 kHz is specified at −140 dBc. Because you can adjust the output frequency over a maximum range of ±6 ppm, you can compensate for more than 10 years of aging. The oscillator operates with supply voltages of 5 and 12V.

In a classical oven-controlled crystal oscillator, a resistance wire heater controls the temperature of an oven that houses the crystal and associated electronics. The combined thermal mass of the oven and the crystal retards crystal heating, and it can take as long as 10 minutes to stabilize the oven-controlled crystal oscillator. The oscillator's design allows it to heat the crystal directly and position the temperature sensor inside the crystal case and in contact with the crystal. This scheme provides an accurate and real measurement of crystal temperature and significantly shortens warm-up time.

Because the resistance heating element acts directly on the unit's AT-cut crystal, the unit has no power requirement for oven heating. Thus, this direct-heating scheme reduces oscillator size and power consumption. The TF-65010 costs \$65 (10,000); allow 8 to 12 weeks ARO for delivery.

—Tom Ormond

Raltron Electronic Corp, 2315 NW 107th Ave, Miami, FL 33182. Phone (305) 593-6033. FAX (305) 594-3973.

Circle No. 732

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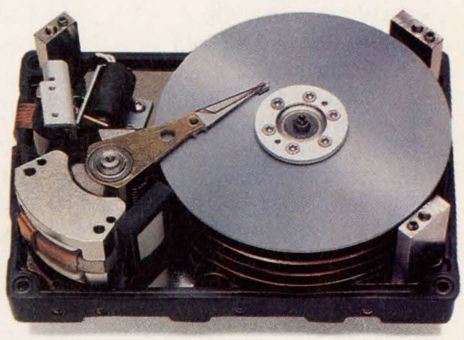

Maxtor LXT-340

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Shipping 300MB Class in Volume	Yes	No
Full Range of Capacities from 213MB to 535MB	Yes	No
Commonality in Family for Components and Manufacturing	Yes	No

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CIRCLE NO. 110

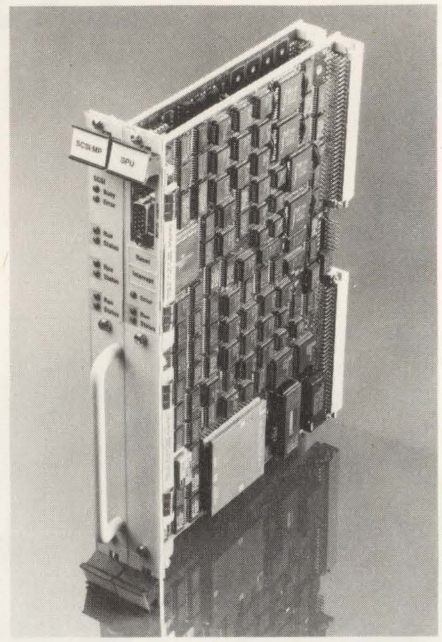
Real-time multiprocessor series occupies one board set

Series 7000 computers perform real-time multiprocessing without using multiple CPU board sets. Instead, the 2-board set that composes the computers' CPU can accept one, two, or three 68040 μPs (25- or 33-MHz versions). The two computers that make up the set run under the company's real-time version of the Unix operating system. Nonintrusive bus-snooping circuitry maintains coherency between the μPs' internal cache memories.

According to the manufacturer, the computers can accept raw data from VMEbus I/O boards across several channels, at aggregate rates as high 50M bytes/sec. The computers' I/O channels hew to the VME32 standard and the proposed VME64 standard for 32 and 64 bitblts, respectively. The VME32 transfers run at rates as high as 30M bytes/sec, and the VME64 transfers run at 37M bytes/sec.

An internal 48-bit clock having a 480-nsec period paces the computers' activity. In addition, the computers have three 32-bit interrupt timers that can measure intervals between pairs of external events or can count occurrences of external events. A 20-bit interrupt timer triggers pattern-based scheduling events, and a 32-bit square-wave generator provides a synchronizing signal for peripheral systems.

The computers can access from 8 to 112M bytes of parity memory. The memory can include as much as 5123k bytes of UV EPROM. Having this much EPROM may seem like overkill until you consider how long reloading a 5M-byte Unix system from disk would take. Having the operating system in ROM speeds recovery from outages. A 5M-byte/sec SCSI port accesses off-line storage. A 24M-byte/sec pk IPI-2 disk system is optional.



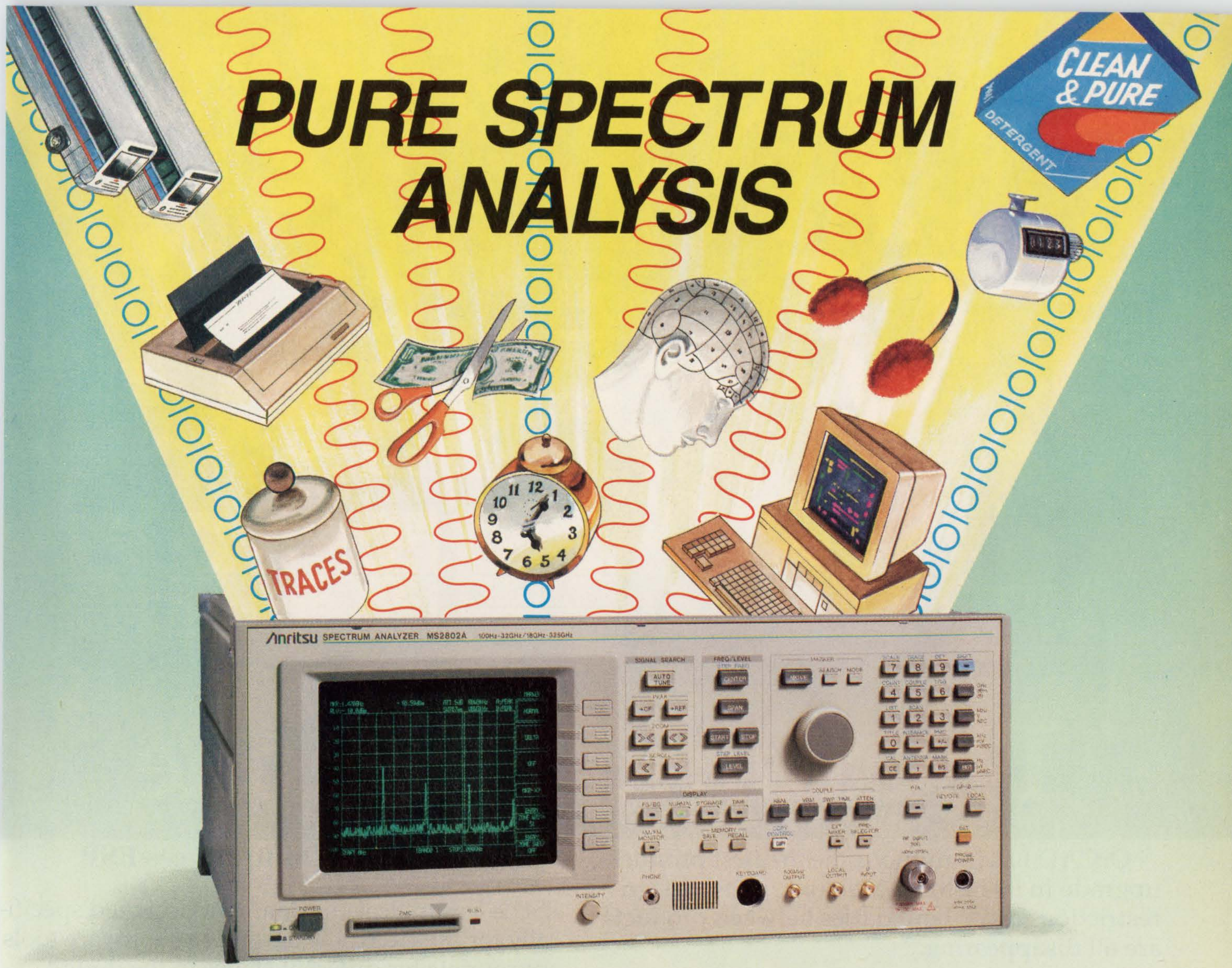
A 2-board VMEbus computer *performs real-time multiprocessing with one, two, or three onboard 68040 μPs.*

Packaged on 6U VMEbus boards, the CPU set fits into 5- or 21-slot enclosures. A 5-slot chassis with one μP and an 8M-byte memory costs $14,500. A 21-slot chassis with one μP and an 8M-byte memory costs $27,995. Additional μPs cost $3000. The company plans to sell the CPU board set but has not yet fixed a price for it.

—Charles H Small

Concurrent Computer Corp, 106 Apple St, Tinton Falls, NJ 07724. Phone (800) 631-2154 (US and Canada); in NJ, (201) 758-7000.

Circle No. 734



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CIRCLE NO. 113

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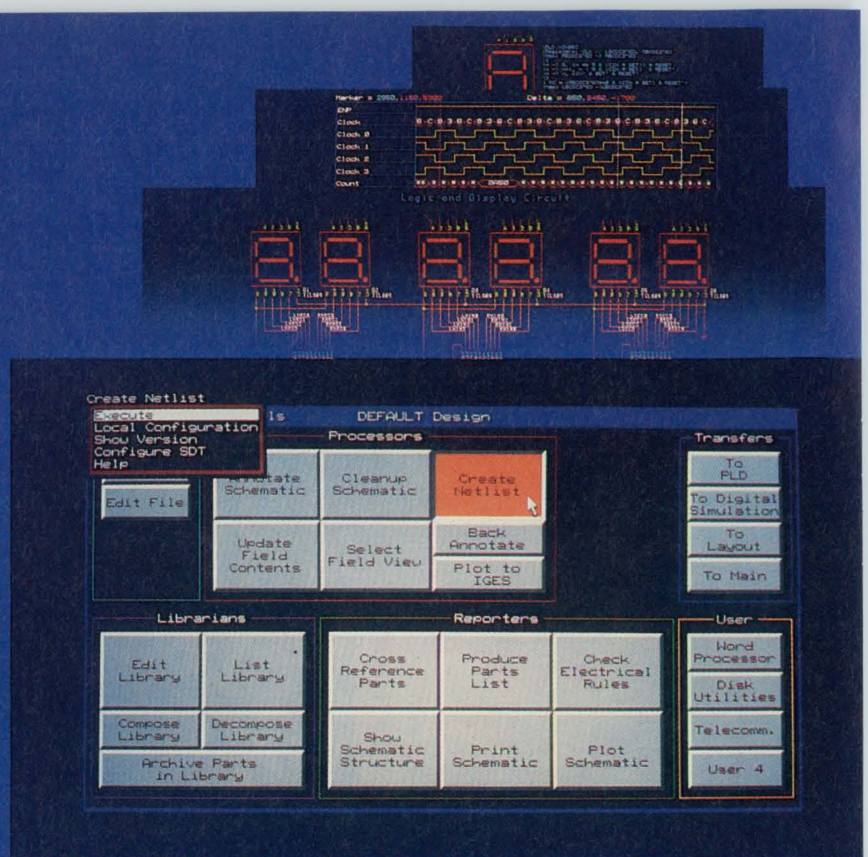
OrCAD presents

Release IV



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CIRCLE NO. 114

LEADTIME INDEX

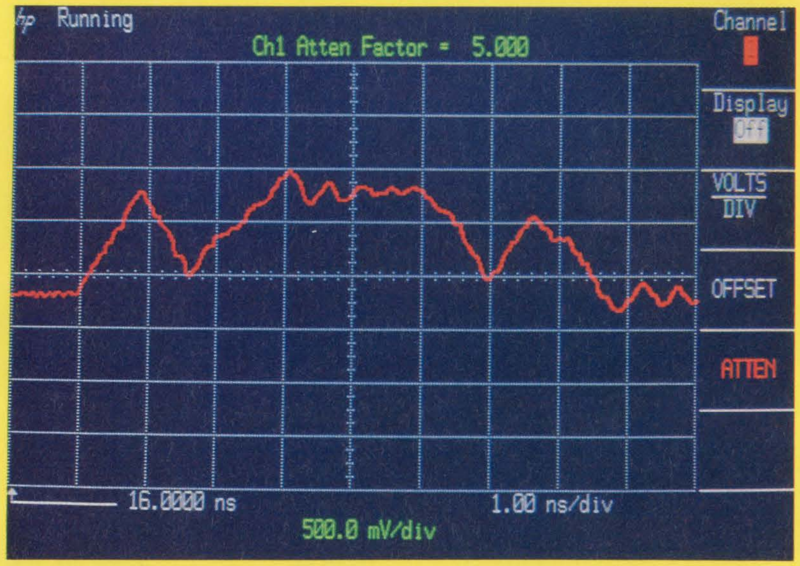
Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	62	13	25	0	0	6.7	7.3
Pot-Core	0	50	25	25	0	0	7.3	8.8
Laminate (power)	0	83	17	0	0	0	3.8	7.1
CONNECTORS								
Military panel	0	14	57	29	0	0	9.4	9.1
Flat/Cable	15	46	31	8	0	0	5.0	3.9
Multi-pin circular	0	78	22	0	0	0	4.0	9.0
PC (2-piece)	20	50	30	0	0	0	3.8	6.0
RF/Coaxial	11	56	33	0	0	0	4.3	4.1
Socket	42	50	8	0	0	0	2.1	4.3
Terminal blocks	33	50	17	0	0	0	2.8	4.3
Edge card	42	25	25	8	0	0	3.9	3.6
D-Subminiature	18	36	36	10	0	0	5.5	4.8
Rack & panel	14	57	29	0	0	0	4.0	5.0
Power	0	62	38	0	0	0	4.8	7.6
PRINTED CIRCUIT BOARDS								
Single sided	8	58	34	0	0	0	4.4	3.8
Double sided	0	60	33	7	0	0	5.5	4.7
Multi-layer	0	43	50	7	0	0	6.3	6.0
Prototype	9	73	18	0	0	0	3.6	3.6
RESISTORS								
Carbon film	44	39	17	0	0	0	2.5	2.7
Carbon composition	46	31	8	15	0	0	3.8	4.7
Metal film	40	60	0	0	0	0	1.7	4.3
Metal oxide	25	50	17	8	0	0	4.0	3.4
Wirewound	31	38	16	15	0	0	4.7	5.1
Potentiometers	27	40	20	13	0	0	4.8	5.2
Networks	43	21	15	21	0	0	5.0	4.6
FUSES	78	11	0	11	0	0	2.0	1.8
SWITCHES								
Pushbutton	42	25	25	8	0	0	3.9	5.2
Rotary	43	14	43	0	0	0	3.8	4.7
Rocker	33	34	33	0	0	0	3.6	4.5
Thumbwheel	38	13	49	0	0	0	4.3	7.0
Snap action	50	25	25	0	0	0	2.7	4.9
Momentary	25	50	25	0	0	0	3.4	4.9
Dual-in-line	44	23	33	0	0	0	3.3	5.3
WIRE AND CABLE								
Coaxial	31	46	23	0	0	0	3.2	2.2
Flat ribbon	45	55	0	0	0	0	1.6	3.0
Multiconductor	38	38	24	0	0	0	3.0	2.9
Hookup	47	53	0	0	0	0	1.5	1.6
Wirewrap	36	45	19	0	0	0	2.8	3.1
Power cords	18	55	27	0	0	0	3.8	4.7
POWER SUPPLIES								
Switcher	9	45	27	19	0	0	6.4	9.2
Linear	20	50	20	10	0	0	4.6	7.9
CIRCUIT BREAKERS	33	33	12	22	0	0	5.3	6.2
HEAT SINKS	45	36	19	0	0	0	2.5	3.1
BATTERIES								
Lithium coin cells	42	58	0	0	0	0	1.7	3.2
9V alkaline	60	40	0	0	0	0	1.1	4.9
Real-time clock back-up	29	71	0	0	0	0	2.1	3.7
RELAYS								
General purpose	17	50	25	8	0	0	4.7	4.8
PC board	21	36	36	7	0	0	5.0	4.5

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
Dry reed	38	25	37	0	0	0	3.7	6.0
Mercury	29	29	42	0	0	0	4.2	5.0
Solid state	22	34	44	0	0	0	4.5	7.5
DISCRETE SEMICONDUCTORS								
Diode	22	50	6	22	0	0	5.3	3.1
Zener	22	39	17	22	0	0	5.9	4.4
Thyristor	21	36	22	21	0	0	6.0	3.1
Small signal transistor	27	40	13	20	0	0	5.3	5.6
MOSFET	27	33	20	20	0	0	5.6	5.4
Power, bipolar	29	36	14	21	0	0	5.4	6.4
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	17	17	41	25	0	0	7.6	4.1
CMOS	33	22	33	12	0	0	5.1	3.5
TTL	33	27	27	13	0	0	4.9	2.8
LS	50	13	18	19	0	0	4.7	2.7
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	7	43	43	7	0	0	5.8	4.7
OP amplifier	27	27	39	7	0	0	5.0	3.9
Voltage regulator	31	15	46	8	0	0	5.3	3.9
MEMORY CIRCUITS								
DRAM 16K	0	66	17	17	0	0	5.9	3.6
DRAM 64K	14	57	15	14	0	0	5.0	3.6
DRAM 256K	22	56	22	0	0	0	3.4	4.4
DRAM 1M-bit	25	37	38	0	0	0	4.1	3.4
SRAM 4K × 4	0	33	50	17	0	0	7.6	4.9
SRAM 8K × 8	11	33	56	0	0	0	5.4	4.7
SRAM 2K × 8	14	29	43	14	0	0	6.4	4.1
ROM/PROM	0	50	33	17	0	0	6.7	4.7
EPROM 64K	0	42	50	8	0	0	6.4	4.7
EPROM 256K	8	33	50	9	0	0	6.3	4.2
EPROM 1M-bit	13	13	61	13	0	0	7.2	4.9
EEPROM 16K	0	38	49	13	0	0	7.0	5.9
EEPROM 64K	0	44	44	12	0	0	6.6	5.4
DISPLAYS								
Panel meters	33	34	33	0	0	0	3.6	4.3
Fluorescent	25	0	25	50	0	0	9.7	8.4
CRT 12-in. monochrome	25	0	25	50	0	0	9.7	7.6
LED	15	23	46	16	0	0	6.8	4.5
Liquid crystal	9	36	36	10	9	0	7.8	6.3
MICROPROCESSOR ICs								
8-bit	15	38	23	15	9	0	7.5	3.3
16-bit	15	46	39	0	0	0	4.4	4.3
32-bit	18	36	19	27	0	0	6.7	5.4
FUNCTION PACKAGES								
Amplifier	14	57	29	0	0	0	4.0	6.5
Converter, analog to digital	22	44	34	0	0	0	4.0	6.5
Converter, digital to analog	22	44	34	0	0	0	4.0	5.4
LINE FILTERS	14	43	43	0	0	0	4.7	7.2
CAPACITORS								
Ceramic monolithic	46	31	15	8	0	0	3.3	2.5
Ceramic disc	42	41	17	0	0	0	2.5	3.3
Film	45	27	18	10	0	0	3.7	4.5
Aluminum electrolytic	25	38	31	6	0	0	4.5	3.4
Tantalum	24	18	58	0	0	0	5.1	4.0
INDUCTORS	27	27	27	19	0	0	5.9	5.4

Source: Electronics Purchasing Magazine's survey of buyers.

REMEMBER WHEN SQUARE WAVES WERE SQUARE?



Typical Digital Waveform, circa 1990
Clock rate > 100 MHz
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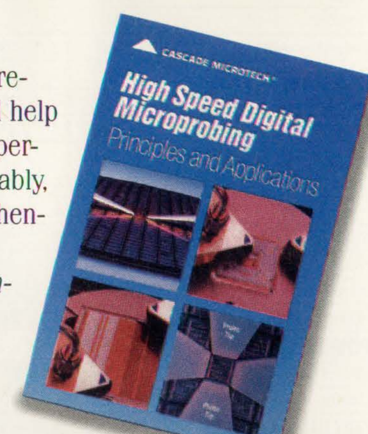

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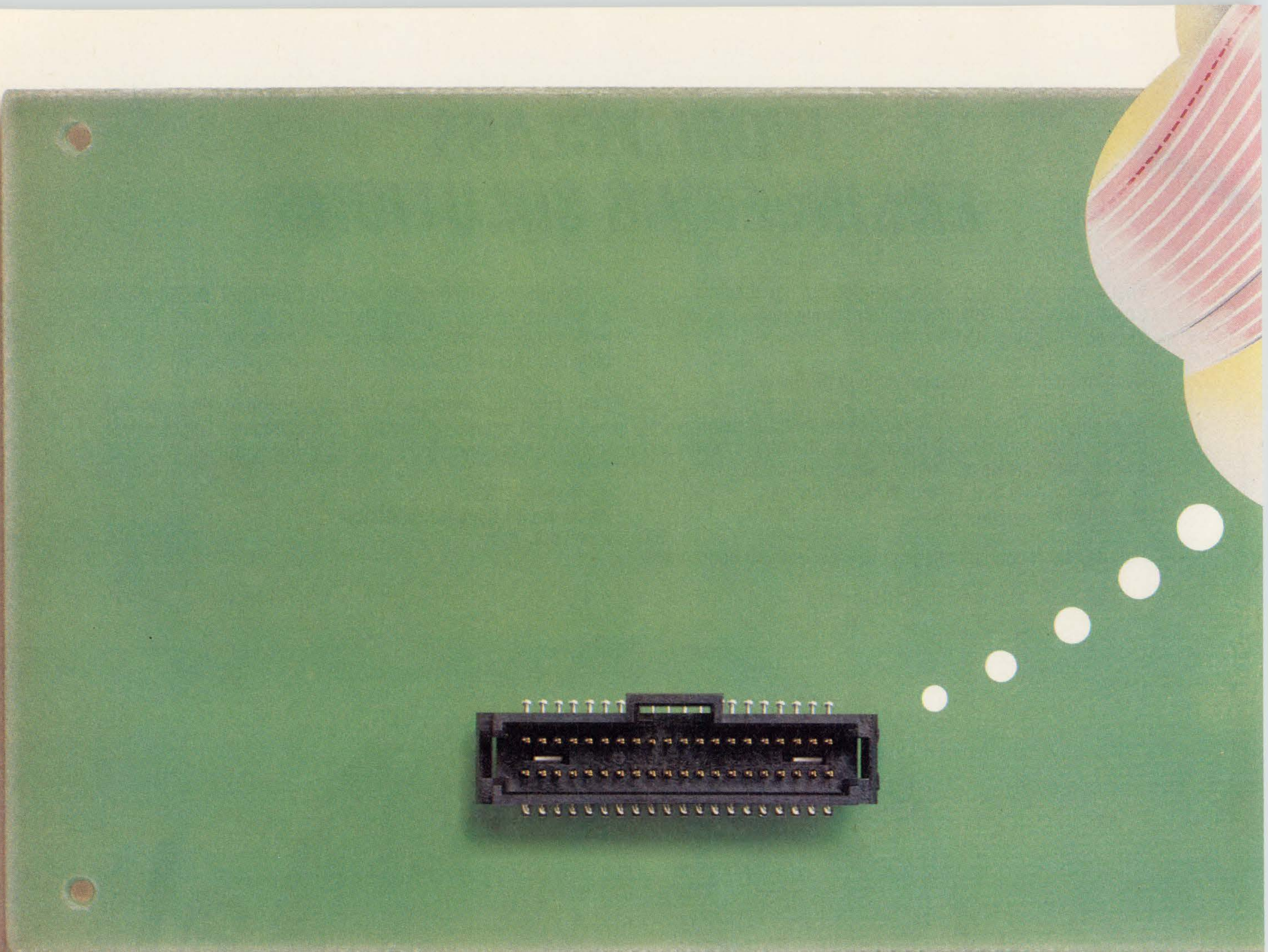

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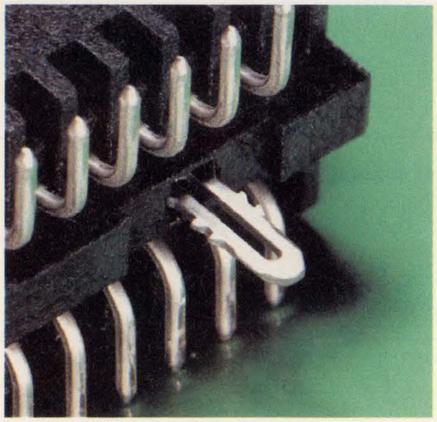
System 50 SMT receptacles and headers intermate with our complete .050" x .100" system, including cable-to-board types that expand your design thinking to include flat flex cable, .050" center flex etched circuitry, and .025" center ribbon cable.



Unique hold-down design requires only simple board support during placement. Design, materials are process-compatible.

Surface-mount versions are available in vertical, double-row versions, fully shrouded, in select sizes from 8 through 100 positions. Our compact design uses the same reliable System 50 interface, with dual-beam phosphor bronze receptacles plated gold-over-nickel on the mating end, tin-lead on the tail.

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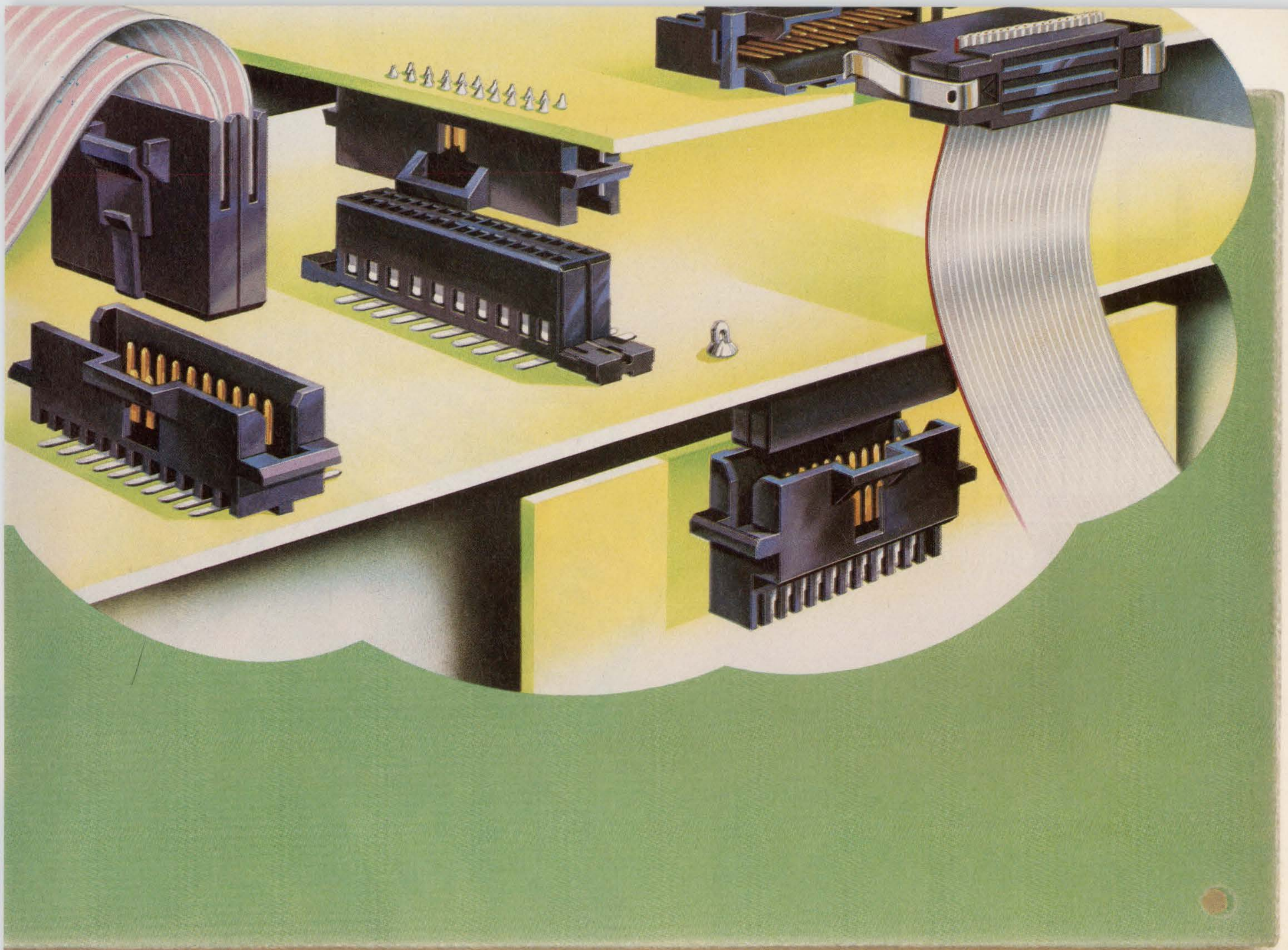


SMT TROUBLESHOOTING

Tom Ormond, *Senior Editor*

High packing density and high speed are two prime benefits of surface-mount technology (SMT). Yet the very packages that provide these benefits complicate the tasks of prototyping, testing, and troubleshooting surface-mount assemblies.

While today's IC packages can significantly reduce the size of electronic subassemblies, these same packages can be a problem when it comes to prototyping new designs and testing and troubleshooting completed assemblies. Increasing pin counts and finer lead pitches create a real challenge when it comes to probing a package terminal.

Wire wrapping has long been the primary technique used to fabricate prototypes of new circuit designs. Several breadboarding panels and IC sockets allow designers to easily fabricate a circuit prototype. In the surface-mount world, most high-level ICs are housed in one of three packages—LCC (leadless chip carrier), PLCC (plastic leaded chip carrier), or PQFP (plastic quad flatpack) (see **box**, "Sorting out some acronyms"). Unfortunately, few products allow designers to readily interface these packages to wire-wrap posts for prototyping. Most of the breadboarding panels are designed for through-hole components and typically have 0.100-in. pin spacings. Pin spacings on the PLCC and LCC packages are typically 0.050 in., whereas spacings for PQFP packages are only 0.025 in.

A second problem occurs during the troubleshooting and testing operations when you try to use test equipment probes at the chip pins. PLCC, LCC, and PQFP package pin counts can exceed 100. Locating a particular pin number on a package with so many leads, and then trying to hold the probe in place on the edge of a lead with center-to-center spacing as low as 0.025 in., proves to be a frustrating, and possibly dangerous, operation.

You could get around these problems by having a technician spend two to six hours hand-fabricating an adapter to convert a chip-carrier socket for wire wrapping. However, you would still have the problem of trying to locate a particular pin for test-probe attachment.

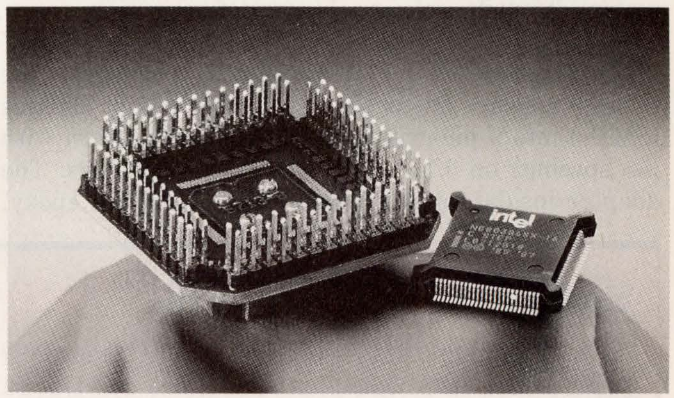
Fortunately, there is a more productive solution to the prototyping/troubleshooting problem—off-the-shelf adapters. Several vendors offer such products, and all are designed to ease the tasks of either prototyping new designs or troubleshooting production surface-mount assemblies. Antona, McKenzie Technology, Ironwood Electronics, and Global Specialties all offer prototyping adapters.

A μP test clip lets you take SMT troubleshooting into your own hands. (Photo courtesy ITT Pomona Electronics)

Easing the prototyping process

Antona offers several adapters designed to ease the prototyping tasks for a variety of surface-mount packages. The Model ANC-8068 adapter, for example, allows designers to readily wire-wrap prototypes of equipment that employs 68-pin PLCC or LCC type packages. The adapter, which is available with either 3-level wire-wrap pins or gold-plated machined pins, can accommodate PLD or erasable type devices that are installed and removed frequently during the system design cycle.

Occupying just less than 6 in.^{2} of board space, the ANC-8068 adapter features labeled test points for each of the 68 pins. The labeling makes it much easier for test personnel to attach oscilloscope or logic-analyzer probes properly. Adapter termination pins are on a 0.3-in. centered-row spacing, so the unit is compatible with a variety of off-the-shelf prototyping panels.



Designed specifically for the Intel 386SX, this test clip from Emulation Technology lets you test a chip that's already on board or bypass that chip with a known-good chip to test out the remainder of the board circuitry.

Adapter documentation includes a user's manual, which contains an adhesive-backed pin-numbering sheet. This sheet can serve as a guide during the wire-wrapping process of the prototype. The documentation also includes a template of the adapter, which designers can use as a signal-to-pin designation map. The ANC-8068 is available from stock and costs $135.

Handling higher pin-count devices

Antona also addresses the needs of designers working with PQFP-packaged devices. Their model ANC-9260 provides a simple means of wire-wrapping 160-pin PQFP devices. The clam-shell-type adapter is rated for 25,000 insertion/removal cycles. The unit occupies just over 8 in.^{2} of board space and includes test pins for each of the 160 pins that are designed to accommodate test probes.

The terminations on the ANC-9260 are spaced on 0.1-in. centers to minimize board real-estate needs and noise problems. These adapters are also available with either 3-level wire-wrapped pins or gold-plated machined pins. The ANC-9260 includes the same amount of documentation as the 8068 and is priced at $249. The company also offers adapters that accommodate devices housed in 84- and 100-pin PQFP packages.

Increasing pin counts and finer lead pitches create a real challenge when it comes to probing an IC package terminal.

McKenzie Technology's ADP Series device carriers are translator boards that have surface-mount pads on one side and through-hole pins on the other. The carriers allow a prototyper to install surface-mount packages into a wire-wrappable breadboard. You can also plug the carriers into another through-hole socket, making it much easier to change defective ICs.

The ADP carriers are available for both JEDEC standard PLCC and PQFP gull-wing packages. The devices convert 68- or 84-pin surface-mount devices (SMDs) into a pin-grid-array (PGA) grid pattern with pin spacings on 0.1-in. center-to-center spacings. The adapter insulators are copper-clad, FR4 glass epoxy, and contacts are tin-lead-plated phosphor bronze. Prices are $11.55 and $13.29 for a 68-pin PLCC and a 132-pin PQFP adapter, respectively.

In addition to a number of PLCC package adapters, Ironwood Electronics also offers prototyping adapters for both JEDEC and EIAJ PQFP packages. The JEDEC units range from 84 to 164 pins. All of the units are designed to have the smallest possible footprints. The units employ gold-plated pins and are available with either solder-tail or wire-wrappable terminations. Prices range from $145 to $200.

For the EIAJ packages, Ironwood offers both socketed and soldered versions. In the latter units, the IC is soldered directly to the adapter and connections are routed to wire-wrappable panel interconnects. The soldered versions have a low profile and are available in sizes that accommodate packages with 60 to 208 pins. These adapters also feature gold-plated pins and are available with either solder-tail or wire-wrappable pins. Prices range from $45 to $156.

Who needs to wire-wrap?

The Surfboard prototyping system from Global Specialties provides a simple and nondestructive vehicle for breadboarding circuitry that employs surface-mount chip-carrier packages. For the designer, the system eliminates the need to fabricate circuitry with permanent connections for testing, evaluating, and troubleshooting—a time-consuming and expensive process.

Each Surfboard consists of a chip-carrier socket mounted on a pc board containing two solderless breadboarding strips. Traces on the pc board connect the socket to the strips. Numbers on the pc board identify each pin location on the chip-carrier socket, making it

Sorting out some acronyms

The following glossary defines some of the more widely encountered surface-mount acronyms and specialized terms.

Chip carrier—a rectangular or square package that has I/O connections on all four sides of the package. On leadless versions, the I/O connections consist of metallized terminations. On leaded versions, I/O connections are attached to the side of the package.

EIAJ—Japanese equivalent of the Joint Electronic Device Engineering Council.

JEDEC—Joint Electronic Device Engineering Council. This group has developed two basic package styles for chip-carrier packages. One has a 0.050-in. pin spacing, and the second has a 0.040-in. pin spacing.

LCC—Leadless chip carrier. This is a chip package whose input and output pads sit right on the perimeter of the package. LCCs come in several versions.

PLCC—Plastic leaded chip carrier. This package can have from 18 to 100 pins. These devices are available with either J or gull-wing type leads.

PQFP—Plastic quad flatpack. This is the JEDEC-approved package for chips with 44 to 256 terminals. JEDEC PQFP carriers typically utilize a 0.025-in. pin spacing, and EIAJ units utilize either a 0.0256- or 0.0316-in. pin spacing.

Quad pack—term used by some manufacturers to designate a PLCC package.

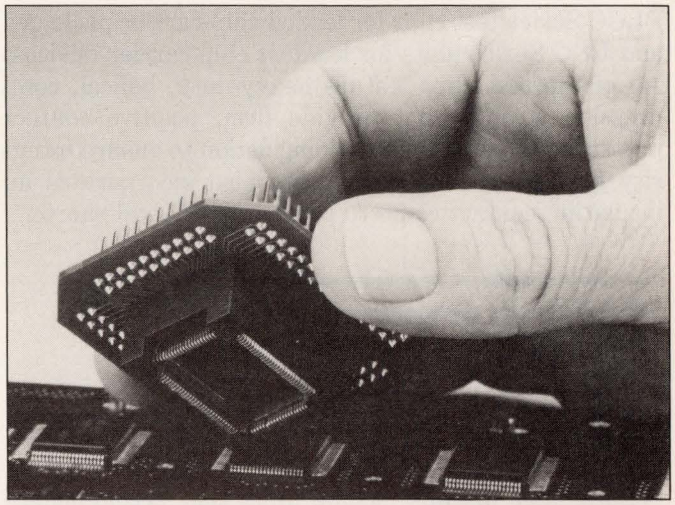
SOIC—Small-outline integrated circuit.—This carrier occupies an area about 30 to 50% less than an equivalent DIP. Typically, the SOIC package employs gull-wing leads spaced on 0.050-in. centers.

easy to identify which pin you're wiring. To make any design modifications, you simply move the wire in question from one location on the breadboarding strip to another.

The Surfboard line consists of five models that accommodate chip carriers with 20, 28, 44, 68, and 84 pins. All units accept JEDEC Type A devices and come with a lifetime warranty. Prices range from $34.95 to $49.95.

All of the adapters discussed up to this point are primarily designed for one-of-a-kind prototype service. You could, of course, use the devices for interim short runs of wire-wrap cards in end-user equipment. However, 3M, Pomona, Emulation Technology, and Ironwood all offer products that are designed primarily for troubleshooting and testing finalized-production circuit boards.

3M's line of test accessories includes two families of test clips designed for surface-mount assemblies:



Designed for PQFP packages, ITT Pomona's 5640 Series test clips feature a press-on design to fit directly over the surface-mounted ICs. Contact with the IC's gull-wing leads is via specially configured gold-plated beryllium copper pins.

Getting the whole picture

In today's electronics world, the design goal seems to be smaller and faster circuitry. Surface-mount technology, fine-pitch geometries, and large-scale integration are all attempts to pack more electronic functionality into less space. However, higher performance often translates into greater heat generation and smaller surface areas equate to less heat dissipation. This results in higher internal operating temperatures—a situation that can decrease system reliability.

Reliability problems are often compounded because today's electronic products are being used more and more in hostile environments. Today, many electronic system designs require users to customize them by selecting from an endless combination of add-on boards from a number of vendors. As a result, product design must frequently allow for a range of uncontrollable and unforeseeable environmental and intrinsic heat sources.

This heightened concern for reliability has increased the importance of thermal analysis in product design and development. Using sophisticated infrared scanning techniques to create thermal pictures or temperature maps (thermograms), the thermal imaging system is the thermal-analysis tool of choice. Although different systems vary in their resolution and scanning speeds, all can generate a complete thermogram of an operating circuit board in less than a minute. Displayed graphically, the data is easy to interpret quickly. Using these capabilities assures the design engineer that the final design will contain no hidden thermal flaws.

The Compix 6000 thermal imaging system from Compix Inc is an economical tool for analyzing the thermal characteristics of components, pc boards, and assemblies. The 2-part system (camera and controller) allows you to examine components and boards during verification, isolate potential thermal problems, and take corrective action. The 6000's high-resolution CRT display (greater than 47,000 pixels) offers a choice of six palettes in color or gray scale. The system will provide both isothermal (color band) temperature mapping and point-by-point temperature measurement with a cursor. The system measures temperatures ranging from 17 to 150°C and records variations as low as 0.2°C. Focus adjustments allow the system to accommodate circuit-board sizes from 3×4 in. to 36×36 in. Close-up adjustments show circuit details as small as 0.015 in.

By utilizing COM6 software with the 6000 system, you can leverage the power of a PC to store, retrieve, and compare images, zoom and pan on-screen, and convert temperature measurements from Fahrenheit to Celsius to milliwatts. COM6 features a menu-driven interface. The software also allows you to remotely control the 6000 system from the PC. A complete system (which includes a folding camera stand, COM6 software, and documentation for the 6000 and the software) costs $18,500.

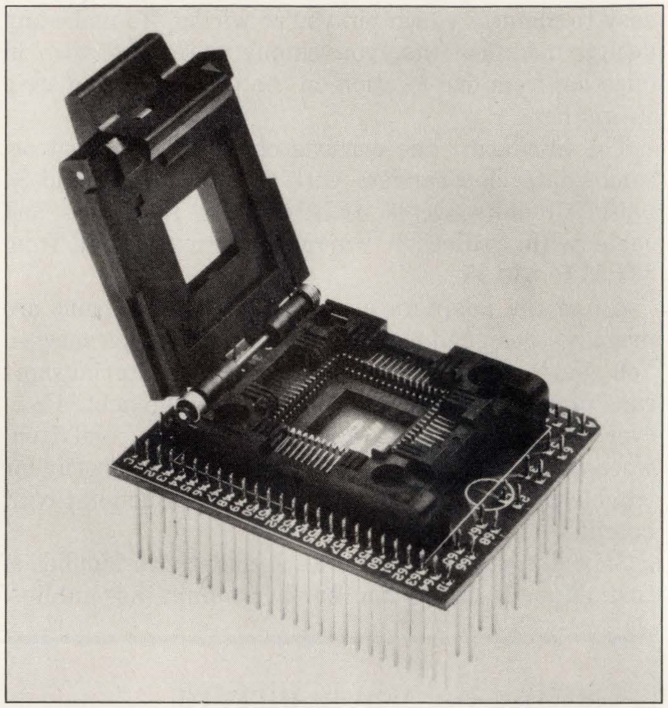
PLCC Series test clips for leaded chip-carrier packages and LCC Series units for leadless chip-carrier devices. All of the test clips feature heavy-duty, helical, compression springs that provide firm, positive contact pressure, and a patented wiping action to ensure integrity in testing. The clip design also incorporates an insulating contact comb to prevent accidental shorts.

Displayed graphically, the data obtained from a thermal-analysis system is interpreted easily.

Both lines of clips include units that accommodate 20-, 28-, 44-, and 68-pin chip-carrier packages with 0.050-in. center-to-center pin spacings. All four sides of the test clips open simultaneously to provide a 1-step attachment to the device under test. All probe access points are visible, providing fast and safe individual lead testing.

PLCC and LCC Series test clips handle high-density, surface-mount assemblies, readily testing ICs with as little as 0.200-in. row-to-row spacing between adjacent devices. The clip contacts are staggered in a 0.1-in. center-to-center pattern. This design facilitates probe attachment and helps prevent the accidental shorting of adjacent probes. These 0.25-in.-square contact pins readily accept single-row female socket connectors. The clips are available with alloy 764 or gold-plated leads and cost $15.95 to $39.95 for both lines.

ITT Pomona's 5640 Series test clips consists of three models that break out the high-density lead patterns of gull-wing type PQFP devices. Models 5643, 5644, and 5645 provide a readily accessible troubleshooting pattern for 100-, 120-, and 160-pin packages, respectively. The devices eliminate the need for handwiring test sockets and ease the task of accessing otherwise impossible-to-test device leads.



Available with 3-level wire-wrap pins, Antona's ANC-8068 adapters offer an efficient way to prototype equipment that employs 68-pin PLCC or LCC packages.

Manufacturers of SMT adapters

For more information on prototyping and troubleshooting devices such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Antona Corp
1643½ Westwood Blvd
West Los Angeles, CA 90024
(213) 473-8995
FAX (213) 473-7112
Circle No. 650

Compix Inc
16195 SW 72nd Ave
Tigard, OR 97224
(503) 639-8496
FAX (503) 639-1934
Circle No. 651

EDI Corp
Box 366
Patterson, CA 95363
(209) 892-3270
FAX (209) 892-3610
Circle No. 652

Emulation Technology
2344 Walsh Ave
Bldg F
Santa Clara, CA 95051
(408) 982-0660
FAX (408) 982-0664
Circle No. 653

Global Specialties
Box 1942
New Haven, CT 06509
(203) 624-3103
FAX (710) 465-1227
Circle No. 654

Ironwood Electronics Inc
Box 21151
St Paul, MN 55121
(612) 431-7025
FAX (612) 432-8616
Circle No. 655

ITT Pomona Electronics
Box 2767
Pomona, CA 91769
(714) 623-3463
FAX (714) 629-3317
Circle No. 656

McKenzie Technology
44370 Old Warm Springs Blvd
Fremont, CA 94538
(415) 651-2700
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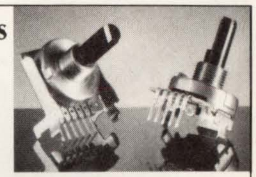

Noble SDB161 2-, 4- and 5-bit encoders are compact (21mm ø) with a low profile (under 10mm height). Built with a sturdy diecast and steel construction, these encoders offer long life and reliability.

SDB161 encoders are for relative (2-bit) and absolute (4-bit, 5-bit) reference applications. 2-bit switches offer 36 detented positions; 4-bit switches offer 12 or 16 detented positions; 5-bit switches offer 24 or 32 detented positions. All encoders feature continuous rotation. The 2-bit is available in gray code; the 4-and 5-bit versions offer either binary or gray code. Custom designs can be accommodated. For free samples, contact Noble at 708/364-6038.

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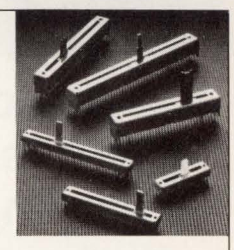
Slide Potentiometers



The VJ Series High and Low Profile Slide Potentiometers are lightweight, durable, and provide smooth operation. They function as volume, balance, brightness/contrast, temperature, lighting and graphic equalizer controls.

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Custom designs can be accommodated. Contact Noble at 708/364-6038 for a free sample.

CIRCLE NO. 166

SMT troubleshooting

Each test clip features a press-on design, which allows the unit to fit directly over the surface-mounted ICs. A built-in pin locater identifies pin 1 on the device under test to eliminate any chance of alignment error. The test clip makes contact with the PQFP's gull-wing leads via specially configured, gold-plated, beryllium copper pins. The clips have a black, molded liquid-crystal polymer housing covering multiple rows of 0.025-in.-square gold-plated, phosphor bronze pins. These pins are positioned on a 0.100-in. grid to accommodate commercially available headers. Model 5643, 5644, and 5645 test clips are priced at $317, $353, and $425, respectively.

Satisfying specific needs

Emulation Technology offers a line of prototyping/troubleshooting adapters that will accommodate LCC, PLCC, and PQFP (both EIAJ and JEDEC type) device packages with pin counts ranging from 20 to 160. One PQFP adapter is the 386SX test clip, designed specifically to facilitate testing of the 386SX chip from Intel—a device that is housed in a PQFP package with 100 pins spaced on 0.025-in. centers. The unit consists of a small pc board, which fits into the palm of your hand. A clip on the bottom of the unit's board covers the 386SX chip already soldered onto the pc board you're testing. A set of pins are located around the perimeter of the top of the unit's pc board. These pins are spaced on 0.1-in. centers—a spacing that makes it easy to attach test leads.

The 386SX test clip allows you to bypass the chip already soldered to the circuit board under test. The clip lets you disable the soldered chip and replace it with a chip that you plug into the test clip. The test clip also lets you use an emulator to imitate the chip already soldered onto the circuit board. In essence, the 386SX lets you simply test the chip already soldered onto the circuit board, disable that chip and test the circuit board, or test the board using an emulator in place of the chip under test. The test clip costs $875.

The Loclip from Ironwood Electronics is a specialty low-profile interconnect device for probing or interconnecting SMD packages. The units will accommodate 20-, 28-, 32-, 44-, 52-, 68-, and 84-pin PLCCs as well as 32-pin SOICs. You can clip the Loclip device onto the surface-mounted PLCC package. Because the mounted height of the Loclip ranges to as low as 0.450 in., you can then reinsert the board into a backplane mounted in a card cage. Prices range from $56 to $85.

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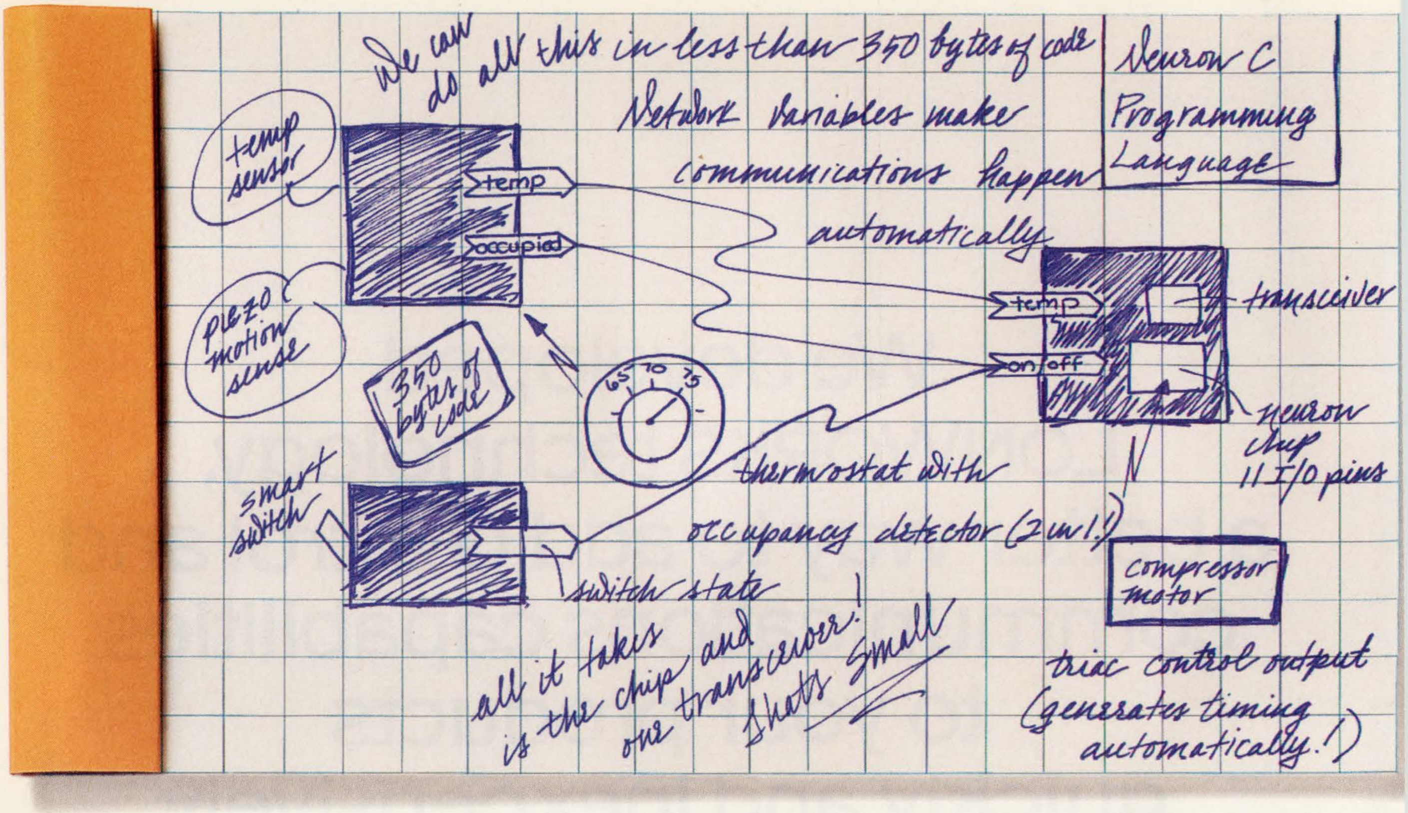
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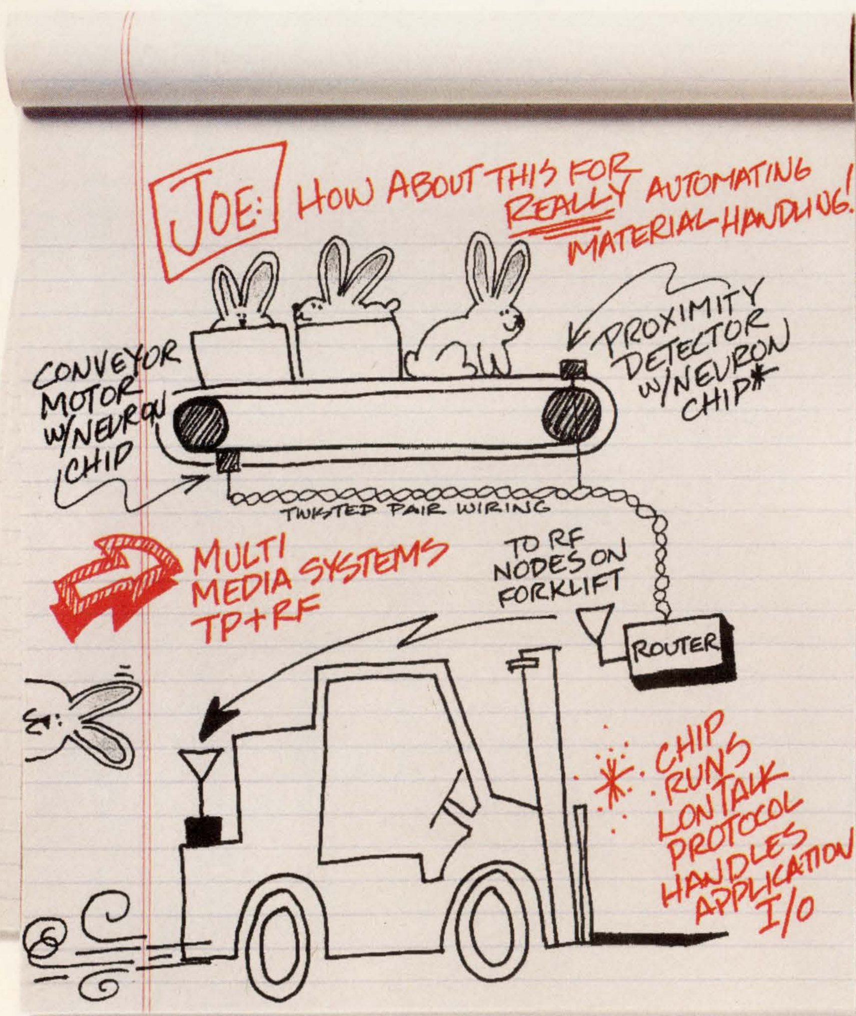
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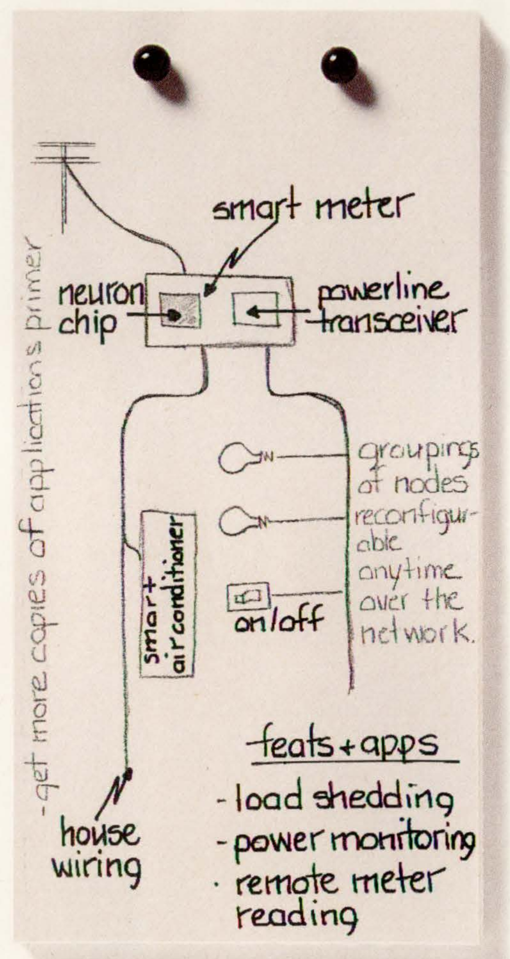
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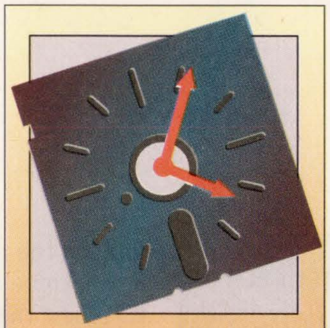

REAL-TIME PROGRAMMING PART 10

Task coordination and communication via signals

The major mechanisms for task-to-task interaction that have been described so far (event flags, messages, semaphores, and controlled shared variables) all use public objects that are accessible to all tasks. There is no sense of a private communication targeted to a specific task. Part 10 discusses signals, which fill this gap by permitting one task to send information to a designated recipient.

David L Ripps, *Industrial Programming Inc*

A signal is a software interrupt that may be handled at the task level. There are four modes of use:

- intratask coordination—A task may elect to have a signal sent to itself as the completion indicator for a requested service (coordination modes **CSIGn**).
- intertask coordination/communication—A task can send a signal to another task, or to a group of tasks, as a means of coordination or communication.
- error recovery—The OS automatically sends Signal 26 to a task when the task generates an error exception, such as an arithmetic overflow. For many processors, error exceptions are also caused by a reference to a nonexistent address and an attempt to execute an unimplemented instruction.
- debugging—A signal is sent after the execution of a breakpoint, which is often implemented as an illegal instruction or a software interrupt instruction. A different signal is sent after the execution of any instruction for which tracing or single-step operation has been enabled. Normally, these signals invoke the Debugger.

This part of the series concentrates on the coordination and communication aspects of signals.

MTOS-UX has 32 signals in total, but only 0 to 15 and 31 are available for task-to-task interaction. (The remaining 15 signals are reserved for error recovery and debugging.)

Signals differ from other coordination mechanisms in two ways. First, signal communication can be synchronous or asynchronous. In synchronous communication, the receiver chooses to ask for information. Waiting for an event flag or a message is synchronous. Signal communication can also be synchronous when the receiver issues a pause-until-signal-arrives request.

From the book, An Implementation Guide to Real-time Programming, by David L Ripps, ©1989. Excerpted by permission of Prentice-Hall Inc, Englewood Cliffs, NJ.

> Unlike most task-to-task interaction facilities, which use public objects accessible to all tasks, signals permit private communication to specific tasks.

However, signal communication can also be asynchronous. The sender transmits a signal to the receiver, thereby imposing the information on the recipient. As far as the receiver is concerned, the information arrives spontaneously and is not necessarily related to whatever ongoing activity the receiver happens to be doing. Thus, signals are the task-level analog of an external interrupt.

The second difference is that each task can decide how it will respond to each separate signal. The choices are: (1) ignore the signal, (2) perform a specified task-level procedure, (3) be blocked until continued by the Debugger, or (4) be forced to terminate. Signal 31 (the "kill" signal) is usually reserved for the forced termination. The response to intertask signals is commonly to perform a task-selected procedure (choice 2).

The signal mechanism is inherent within the operating system. Signal facilities may neither be created nor destroyed. All a task can do is change its response to a given signal.

Signaling as an end-of-service indicator

Previous sections have discussed two ways in which a task can determine that a requested service is completed:

- It can wait so that the request function does not return until the service is completed (mode **WAIFIN**).
- It can continue immediately and have a specified local event flag set upon completion of the service (mode **CLEFn**).

There is also a third mode, **CTUNOC**, in which the task continues without any coordination.

The fourth possibility is to have the task continue, with a signal in the range 0 to 15 sent when the service is completed. This mode is specified by the literals **CSIG0** to **CSIG15** in the coordination field of the service. The following word diagram illustrates how the signaling mechanism can be put to advantage:

1. Allocate a work area from a pool; save the address.
2. Build a message in the work area.
3. Set the response to, say, Signal 3 to be procedure *done3* ().
4. Send the message with **CSIG3** as coordination mode.
5. Continue with other work.
6. When the message is transferred, Signal 3 is sent to the task. The ongoing other work is interrupted and procedure *done3* is performed. The procedure deallocates the work area whose address was saved and then returns. This automatically resumes the interrupted other work.

Thus, the benefit of signal coordination is that it permits some task-level operations to be performed upon the completion of a service, without having to wait directly for that completion.

Set response to signal

When a task is first created, the default response is to ignore Signals 0 to 15 and terminate for Signal 31. (If the optional Debugger task has been installed, then the default for the error signals, 15 to 30, is to become blocked and start the Debugger to unblock it. If the Debugger is not present, the default is to print an error message on the System Console via the Error Logger task, if present, and then terminate the errant task.)

The function *setsig* resets the response to a prescribed list of signals. The C definition of the function is

```
int setsig (sigmsk,resp)
    long int sigmsk;
    int (*resp) 0;
```

The signals of interest are selected by *sigmsk*, using one bit per signal, left to right. A value of 0x80000000 selects only Signal 0. The literals **SIG0** to **SIG31** may be combined to select the appropriate bit or bits. **SIGALL** means all signals.

The desired response is indicated by *resp*. Four literals are recognized: **SIGIGN** (ignore), **SIGBLK** (become blocked if the Debugger is present; terminate if not), **SIGTRM** (terminate), and **SIGDFL** (reinstate the default). Any other value is assumed to be the address of a function to be executed upon receipt of the signal.

NOERR is returned for a successful call of *setsig*. **BADPRM** indicates that the change was rejected because the function was not executable (for example, started on an odd address for the 680xx family).

Some examples of the call are to reset the response of all signals to the default,

```
setsig (SIGALL,SIGDFL);
```

to set the response to Signal 3 to procedure *done3*,

```
int done3();          /* define done3 as a procedure */
    setsig (SIG3,done3);
```

and to set the response to Signals 1, 2, and 5 to ignore the signal.

```
setsig (SIG1+SIG2+SIG5,SIGIGN);
```

Signal response procedure

The structure of a signal response procedure is identical to that of a task: It is a procedure having a single argument. The argument is the address of a structure that is built by the OS when the signal is sent. The structure contains the signal number, plus the context of the task at the point of interruption. While the latter may not be of interest for communication and coordination signals, it is vital for error signals.

The signal response procedure executes at the task level and can issue any OS requests that the task could. The procedure acts completely as though it had been called by the task. It inherits the priority of the interrupted task and any task-level objects that the task had at that point. It can access any static data that the interrupted task could, but cannot see any local data. (This is generally true of a called procedure in C.) Correspondingly, any changes the procedure makes to the priority, task-level objects, or static data are the same as though the interrupt task itself had made them.

Normally, the procedure returns by reaching the last curly bracket of its code. In that case, the task continues from the point of interruption. Nevertheless, the procedure is free to terminate the task itself by issuing *exit* or *trmrst*.

Because the procedure acts as an extension of the task, the procedure may not execute immediately upon the arrival of the signal. For example, if the target task is blocked waiting for a previous service to be completed, the signal processing is postponed until the task becomes Active. Furthermore, while a task is executing a procedure invoked by a communication or coordination signal, the OS will not pre-empt that processing to handle another signal of the same type. The OS records any pending signals for a task and then processes them as soon as it is appropriate to do so.

Task-to-task communication via signals

One task can send a signal to another task, thus invoking whatever response the receiver currently has in force. The request specifies both the receiving task and the signal number.

```
sndsig (tskRid,15L);        /* send signal 15 to task R */
```

Normally, the first argument is the identifier of the target task. (It is not an error for a task to send a signal to itself.) For the special value 0, the signal is sent to all other application tasks in the system. This might be used to terminate all tasks prior to shutting down the computer.

```
sndsig (0L,31L);
```

One advantage of the signal for task-to-task communication is that the receiver can be interrupted to perform some signal-specific activity via a response procedure and then return to continue the interrupted "main" line of execution. This can be illustrated with a task (**HU**) that handles unusual conditions detected by a pair of scanning tasks (**SD** and **SM**). The individual scanning tasks have neither the time to evaluate the unusual conditions they find nor the overall information to take proper action. Thus, when a scanning task detects something that needs closer scrutiny, it sends a signal to **HU**.

For **SD**, the "somethings" are discrete events that

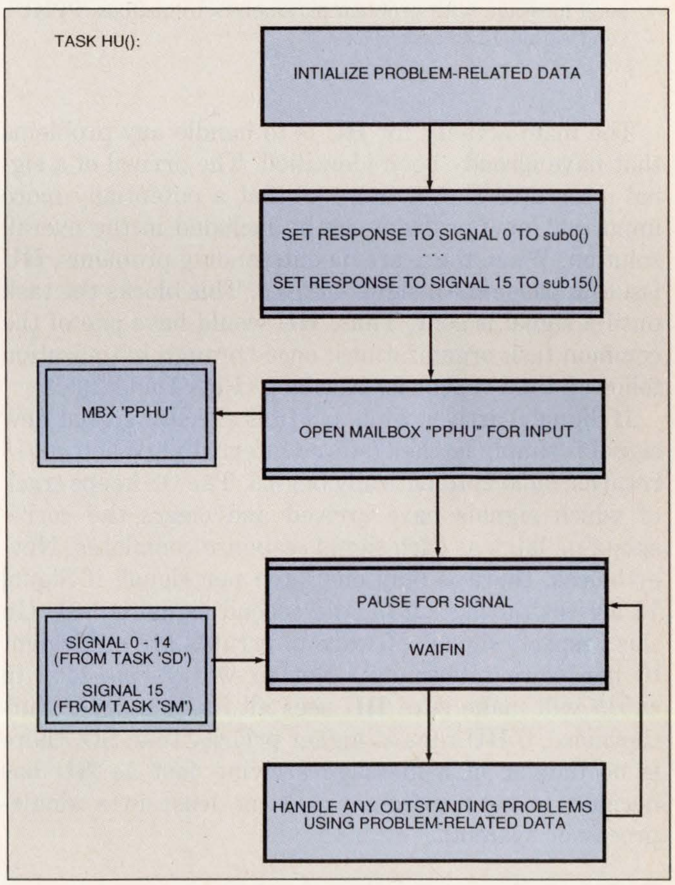

Fig 1—In a typical application of intertask communication via signals, one task handles unusual conditions detected by other tasks. In this example, problem-handling task HU receives signals from scanning tasks SD and SM.

> Each task can decide how it will respond to each separate signal: ignore it, perform a specified procedure, be blocked temporarily, or be forced to terminate.

can be represented by integers 0 to 14. Thus, **SD** just sends the corresponding signal

```
if problem "i" is suspected then send signal "i" to task HU;
```

The problems detected by **SM** are more complex so that further information must accompany the signal. **SM** transmits the auxiliary data in a mailbox message.

```
if problem is suspected then
  {
  send message with problem parameters to mailbox 'PPHU';
  send signal 15 to task HU;
  }
```

The main activity for **HU** is to handle any problems that have already been identified. The arrival of a signal interrupts that activity so that a potentially more important new problem can be included in the overall solution. When there are no outstanding problems, **HU** issues a pause-until-signal-arrives. This blocks the task until a signal is sent. Thus, **HU** would have one of the common task organizations: once-through initialization followed by a repeat-forever loop (**Figs 1** and **2**).

If Signal 0 arrives while *sub15* is executing, that new signal is simply latched (stored internally). When *sub15* returns, *sub0* automatically begins. The OS keeps track of which signals have arrived and clears the corresponding latch as each signal response completes. Nevertheless, there is only one latch per signal; if Signal 15 arrives during *sub15*, the second signal is lost. (In this respect, signal software interrupts are equivalent to hardware interrupts.) Not to worry, the loop in *sub15* will make sure **HU** sees all its messages. Furthermore, if **HU** runs at higher priority than **SD**, there is no danger of a message arriving just as **HU** has decided to return from *sub15* (at least in a single-processor system).

Task-to-task coordination via signals

Simple intertask coordination can be achieved by having one task (**TskT**) pause for a signal that is sent by another task (**TskC**) when **TskC** wants **TskT** to continue. This is closely related to the coordination pairs pause/cancel-pause and wait-for-local-event-flag/set-local-event-flag.

The pause-for-signal request specifies a maximum wait time. The time can be a specific interval

```
pausig (100+MS);
```

or can be "forever."

```
pausig (NOEND);
```

The first signal to arrive cancels the pause to continue the task, even if the response is to ignore the signal. Normally, *pausig* returns the signal number (0 to 31). However, if a signal does not arrive within the given interval, *pausig* returns with a value of **TIMOUT**. An invalid time interval is indicated by the value **BADPRM**.

Sending a signal after a given interval

A task can have a specified signal sent to itself after a given interval.

```
sgisig (3L,2+MIN);
```

The signal to be sent is specified by the first argument. Proper values are 0 to 15 and 31. The interval is given in the usual way.

Often, the response to a signal sent by *sgisig* is the execution of an asynchronous procedure. In this way,

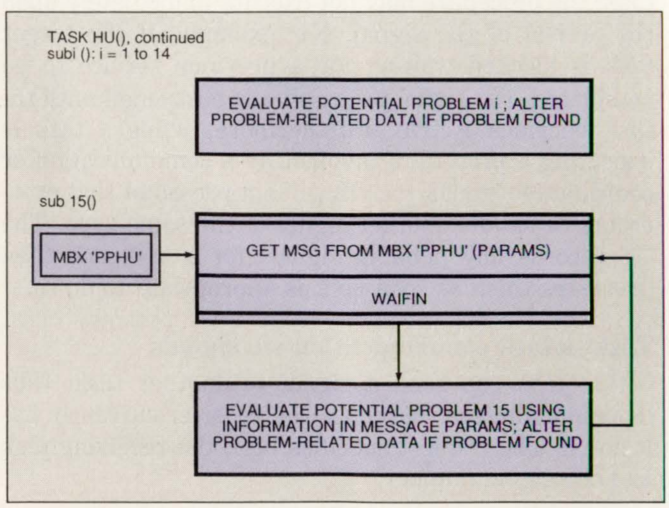

Fig 2—The problem-handling response of task HU depends on which signals the task receives. Signals 0 through 14 represent simple events that can be represented by integer numbers. The event represented by signal 15 is more complex, requiring further information to be sent to task HU via a mailbox.


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a single task can carry out a primary activity and periodically perform some auxiliary work (via the signal-invoked procedure).

As a simple example, suppose a task must perform a very long calculation, say one that takes about 5 minutes. It would be desirable to have the task show that the calculation is in progress by outputting a '>' every 10 seconds. This can be accomplished easily through *sgisig*.

```
int showp ();              /* define showp as a procedure */
setsig (SIG0,showp);       /* set response to signal 0 */
sgisig (0L,10+SEC);        /* send first signal 0 */

do long calculation

setsig (SIG0,SIGIGN);      /* reset response to signal 0 */
 ...
showp ()
  {
    putchar ('>');         /* output in-progress character */
    sgisig (0L,10+SEC);    /* send next signal 0 */
  }
```

To sum up, a signal is a software interrupt that may be handled at the task level. Signals provide a mechanism for asynchronous coordination and communication as well as for synchronous error recovery and debugging. (Synchronous or asynchronous indicates whether or not the arrival of the signal directly correlates with the current activities of the receiving task.)

There are 32 different signals. Each task may select its own response to each separate signal. The primary response is to perform a preselected, task-level procedure and then return to the ongoing task activity. Altternate responses are: (1) to ignore the signal, (2) to terminate the task, and (3) to halt the task and start the Debugger. A task can determine its current response to any signal and can dynamically change that response.

The OS automatically sends a corresponding signal when it detects a task error, such as an arithmetic fault or a bad parameter within a service call. A task may elect to have the OS send a signal when a requested service is completed or a given time interval has elapsed. A task can also send a selected signal to one given task, to a group of tasks, or to all of the application tasks. Finally, a task can pause until a signal arrives from any of the aforementioned sources.

The next installment, Part 11, will conclude this series with a wrap-up of the task coordination discussion.

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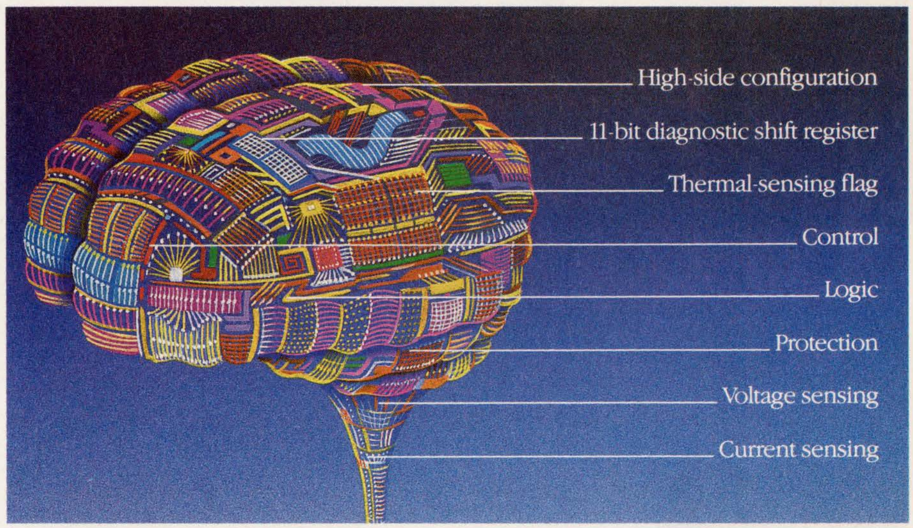

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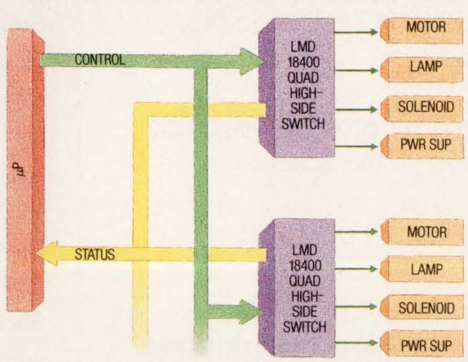

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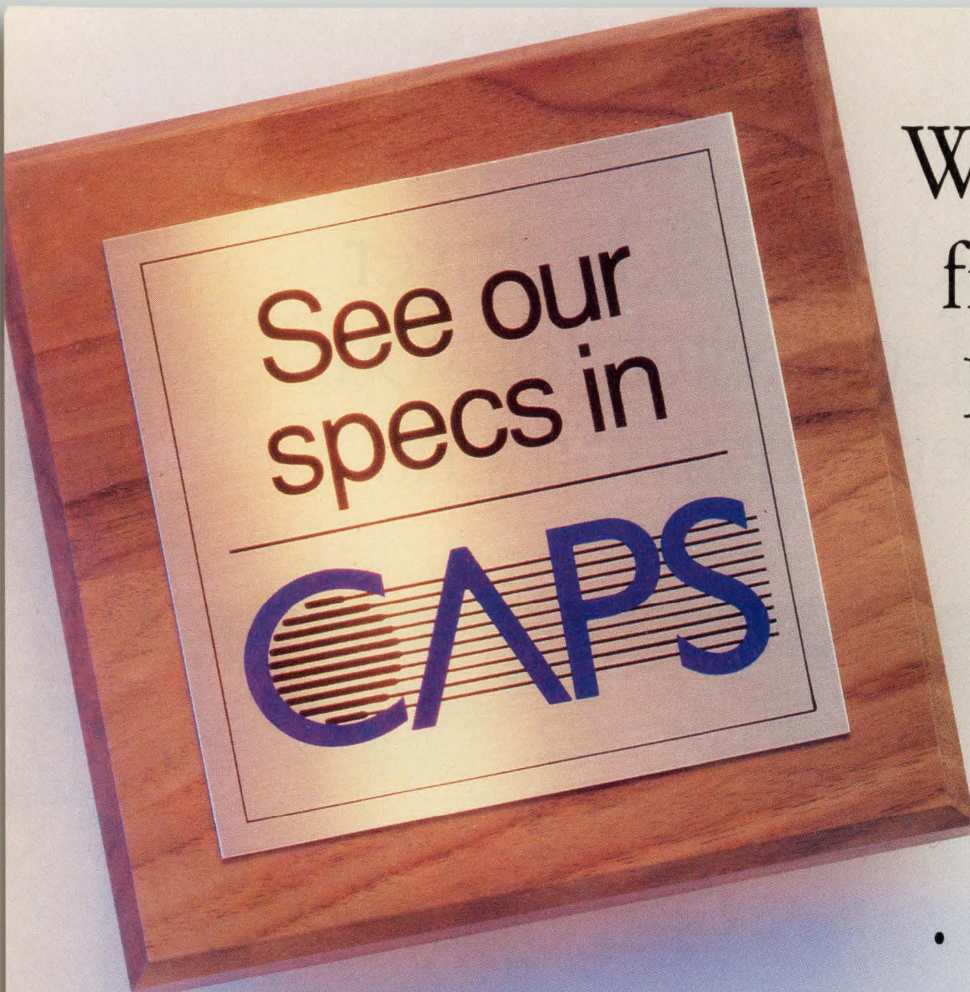

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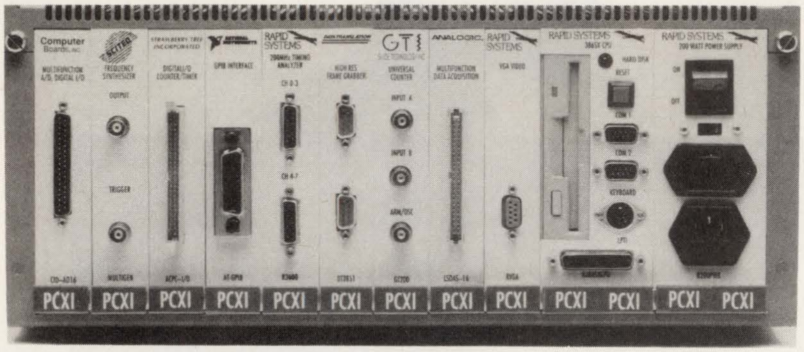

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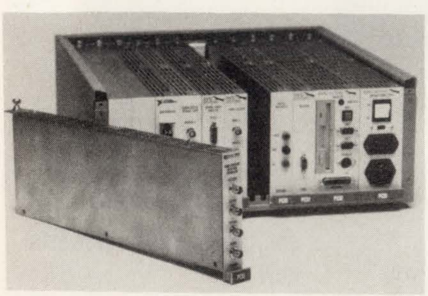

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CIRCLE NO. 128

Noninteger division synthesizes multiple clock frequencies

Generating multiple clock frequencies from a single reference often requires noninteger division. A basic algorithm provides an alternative to traditional division techniques by giving you some choice of the reference.

Sid Ghosh, *Design Assistance*

Designing frequency dividers that have noninteger division ratios is a problem that has long plagued the digital designer. The problem is particularly vexing when you must generate multiple clock frequencies synchronized to a single reference. One of the traditional methods for generating fractional division ratios is to use a frequency synthesizer that has a divide-by-M counter on the input to a phase-lock loop and a divide-by-N counter in the feedback path. Because the frequency synthesizer uses the ratio of N/M as the division ratio, however, this method loses accuracy when the synthesizer must generate a clock frequency that requires a non-rational divisor.

Another traditional method uses a very high frequency reference, which has a period equal to the least common multiple of all the desired clock periods. You then obtain the desired clock frequency using a counter that divides the reference by an integer. Often, however, this method requires a reference that is so high in frequency that it becomes difficult, if not impossible, to generate.

A typical application that requires a large number of clock frequencies synchronized to a single reference is the generation of fractional T1 clocks for private T1 networks. In these "customer-premise-equipment" applications the fractional T1-clock rates can be any frequency in the range of $N \times 64$ kHz (where $N = 1$ to 24) or 56 kHz. You must synchronize these clock rates to the 1544-kHz T1 transmission rate. A variation on the integer divider method lets you synthesize the fractional T1-clock rates using noninteger division. The noninteger divider gives you some flexibility in selecting the reference frequency and enables you to use standard fast-logic families.

As with all synthesis methods, the noninteger division technique produces a clock frequency that has phase jitter. You must evaluate the jitter to determine if the technique is applicable to your needs. A couple of examples illustrate the technique and the resultant p-p phase jitter. The examples use a reference frequency, called HICLK, which is a multiple of the 1544-kHz T1 transmission rate.

$$\text{HICLK} = 24 \times 1544 \text{ kHz} = 37.056 \text{ MHz}$$

The technique always generates a clock frequency, CLK', which is twice the desired frequency ($\text{CLK}' = 2 \times \text{CLK}$) so you can use a divide-by-2 counter to obtain the desired frequency having a precise 50%

The noninteger divider gives you more flexibility in selecting the reference frequency.

duty cycle. The first example synthesizes a 128-kHz clock frequency. In this example, the division ratio is

$$\text{DIV} = \text{HICLK/CLK'} = 24 \times 1544/256 = 144.75.$$

The technique employs an algorithm that produces a division ratio (DIV) that is a positive real number. The division ratio is given by

$$\text{DIV} = (\text{A} \times \text{d} + \text{B} \times (\text{d}+1))/(\text{A}+\text{B}),$$

where A and B are integers that are prime numbers and d is the integer value of the division ratio,

$$\text{d} = \text{INT(DIV)}.$$

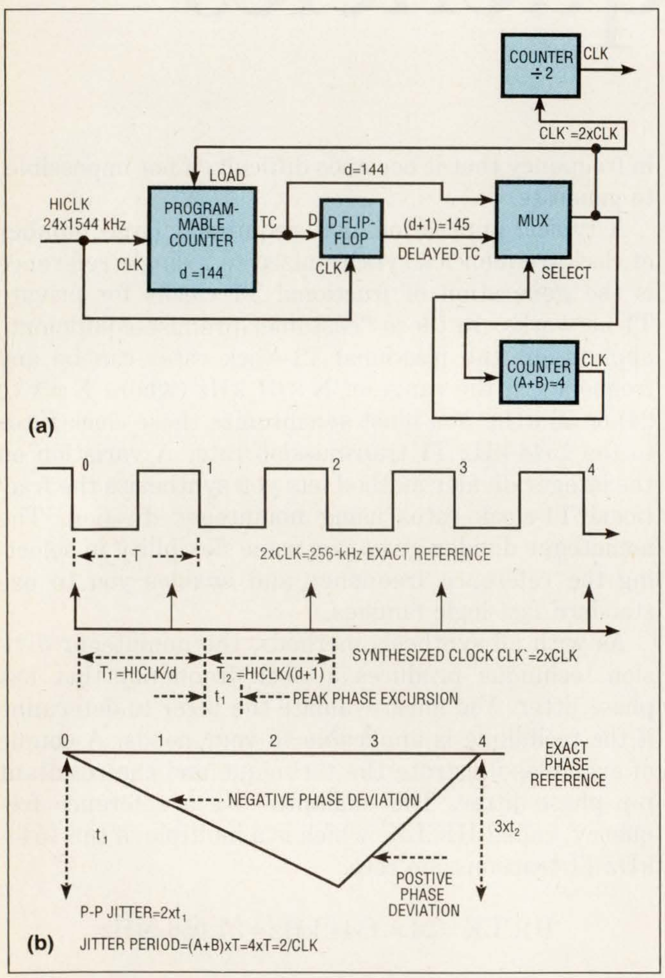

Fig 1—The block diagram shows an implementation to synthesize a 128-kHz clock (a). *You can analyze the jitter on the CLK' signal by comparing the time to divide the HICLK by d or d+1 with the period of an exact 256-kHz reference **(b)**.*

You must determine the values for A and B before you can apply the division algorithm. The method for computing A and B will be shown later in the text, but for this example let A = 1 and B = 3. Therefore,

$$\text{DIV} = (144 + 3 \times 145)/4.$$

This expression indicates that you can obtain CLK' by dividing the HICLK reference frequency once by 144 and then thrice by 145. Then repeat the cycle after the four indicated divisions. **Fig 1a** shows a block diagram of a possible implementation. A digital multiplexer selects either the terminal count (TC) from a programmable counter that divides the HICLK by d = 144 or a delayed TC from a D flip-flop that delays TC by one HICLK period. The delayed TC is a signal representing a division by d + 1 = 145.

Each output from the multiplexer loads a count number into the programmable counter and clocks a divide-by-4 (A + B) counter to control the multiplexer's selection. The control causes the multiplexer to select one TC signal and three-delayed TC signals before repeating the cycle. Another counter divides the output frequency of the multiplexer (CLK') by 2 to generate the desired clock frequency (CLK) having a 50% duty cycle.

Fig 1b illustrates the jitter on the synthesized CLK' period. The diagram compares the edge transitions of the synthesized 256-kHz clock with the edge transitions of an exact 256-kHz reference. You calculate the peak phase jitter using the following relationships:

$$\text{T} = \text{period of the exact reference},$$

$$\text{T} = 1/(256 \times 10^3) = 3.906\ \mu\text{sec},$$

$$\text{T}_\text{d} = \text{d} \times (\text{HICLK period}),$$

$$\text{T}_\text{d} = 144 \times (1/(24 \times 1544 \times 10^3)) = 3.886\ \mu\text{sec},$$

$$\text{T}_{\text{d}+1} = (\text{d}+1) \times (\text{HICLK period}),$$

$$\text{T}_{\text{d}+1} = 145 \times (1/24 \times 1544 \times 10^3) = 3.912\ \mu\text{sec},$$

$$\text{t}_1 = \text{T} - \text{T}_\text{d} = 20.2\ \text{nsec, and}$$

$$\text{t}_2 = \text{T}_{\text{d}+1} - \text{T} = 6.75\ \text{nsec}.$$

The synthesized CLK' period lags behind the period of an exact 256 kHz clock by $t_1 = 20.2$ nsec when the division ratio is 144 and leads the period of an exact

256-kHz clock by $t_2 = 6.75$ nsec when the division ratio is 145. Because 3×6.75 nsec $= 20.2$ nsec, the phase of the synthesized CLK' coincides with the phase of an exact 256-kHz clock at the start of each cycle. But within the cycle the p-p jitter is $2 \times 20.2 = 40.4$ nsec because the phase deviation can be either positive or negative. The jitter frequency is $256/4 = 64$ kHz (CLK'/(A + B)).

A second example synthesizes a 256-kHz clock from the HICLK. The CLK' frequency in this case is 512 kHz. Therefore,

$$DIV = 24 \times 1544/512 = 72.375, \text{ and}$$

$$d = INT(DIV) = 72.$$

Let $A = 5$ and $B = 3$ then

$$DIV = (5 \times 72 + 3 \times 73)/8.$$

Fig 2a shows a block diagram of the implementation. In this example, the multiplexer selects either five Tics from a programmable counter that divide the HICLK by 72, or three delayed TCs from the D flip-flop that divide the HICLK by 73. The output of the multiplexer clocks a divide-by-8 (A + B) counter that decodes the fifth and the eight count to control the multiplexer. A set-reset flip-flop uses the signals from the divide-by-8 counter to control the multiplexer. As in the first example, each output from the multiplexer loads the programmable counter with a count number and a counter divides the CLK' frequency by 2 to generate the 256-kHz clock with a 50% duty cycle.

In this example, t_1 and t_2 calculate to be 10.1 nsec and 16.9 nsec, respectively. **Fig 2b** shows that the p-p jitter is approximately 100 nsec ($10 \times t_1$). You can reduce the phase jitter by modifying the control to the multiplexer. For example, the control circuitry could alternate the selection of the TCs and the delayed TCs for the first six counts of the cycle followed by the selection of 2 TCs. This modification, or a similar selection scheme, maintains the same division ratios for the cycle but reduces the p-p jitter on the CLK' frequency.

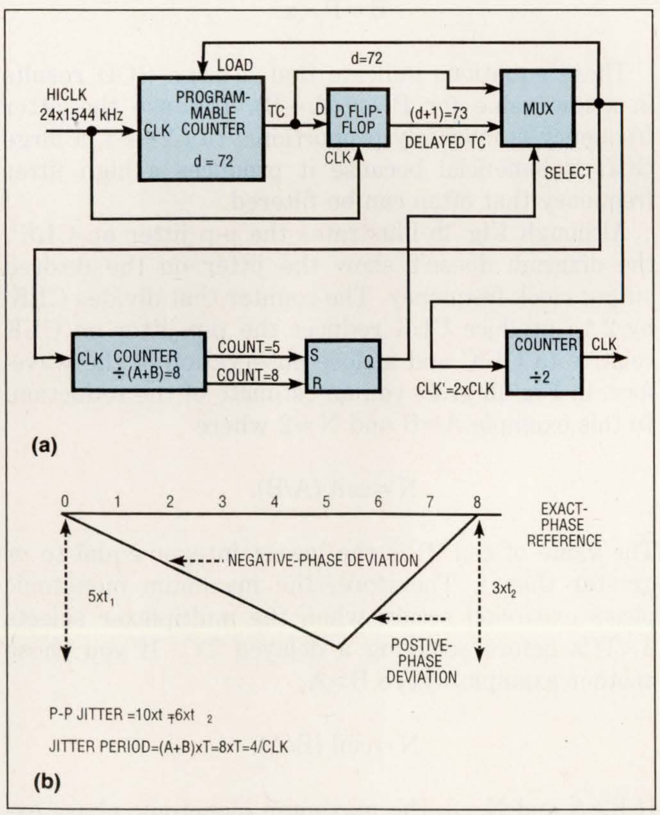

Fig 2—This implementation (a) is one possible way *to synthesize a 256-kHz clock. This implementation, however, results in a large p-p jitter **(b)** on the CLK' signal.*

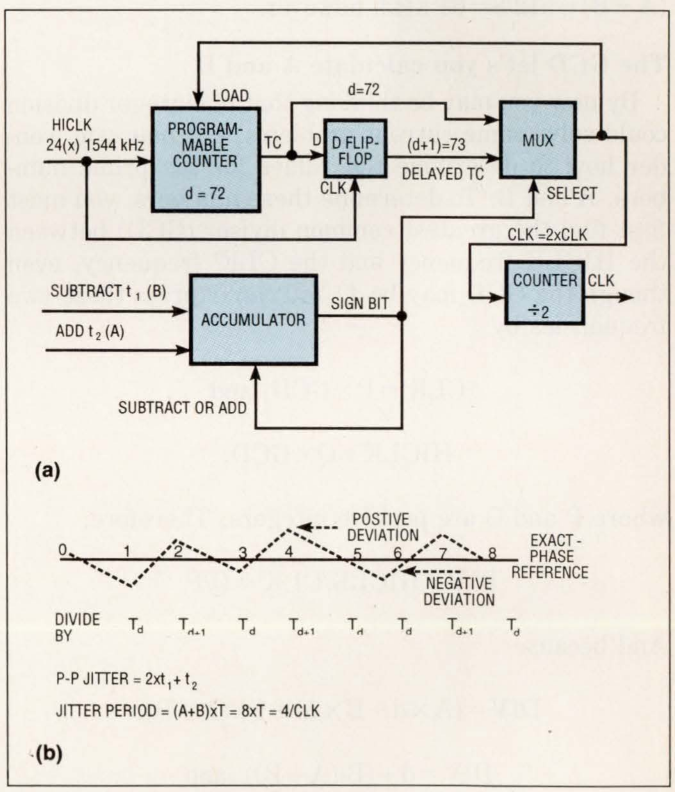

Fig 3—The block diagram shows a modification *that alters the selection of the terminal counts and the delayed terminal counts to synthesize the 256-kHz clock **(a)**. The modification produces less jitter **(b)** than the implementation shown in **Fig 2a**.*

You must evaluate the synthesized clock jitter to determine whether noninteger division is applicable to your needs.

The block diagram shown in **Fig 3a** implements this modification. The concept uses an accumulator, which accumulates the values for t_1 and t_2, to control the multiplexer. When the sign bit from the accumulator is positive, the multiplexer selects TC and the accumulator subtracts the value of t_1 from its contents. Similarly, when the sign bit is negative, the multiplexer selects delayed TC, and the accumulator adds t_2 to its contents. The accumulator's contents is initially 0, and the contents return to 0 after A + B divisions.

The noninteger division algorithm guarantees that the accumulator's content will converge to 0 after starting from any initial condition and that there will never be an overflow condition. In addition, because t_1 and t_2 are real numbers, you can replace their values with the integers for B and A, which are proportional to t_1 and t_2, respectively. **Table 1** tabulates the sequence of events for a cycle to synthesize the 256-kHz clock. Comparing **Fig 2b** with **Fig 3b** shows that the modification reduces the p-p jitter from 100 nsec to 36 nsec. The jitter frequency for both cases is CLK'/(A + B) = 512/8 = 64 kHz, however.

Table 1—Sequence of accumulator contents

Sign bit	t_1 and t_2 accumulator contents (n sec)	A and B accumulator contents
+	0	0
–	–10.1	–3
+	+6.8	+2
–	–3.3	–1
+	+13.6	+4
+	+3.4	+1
–	–6.7	–2
+	+10.2	+3
+	0	0

The GCD let's you calculate A and B

By now you may be thinking that noninteger division could solve some current problems, but now you wonder how to determine the values for the prime numbers, A and B. To determine these numbers, you must first find the greatest common divisor (GCD) between the HICLK frequency and the CLK' frequency, even though the GCD may be 1. You can express these two frequencies by

$$\text{CLK'} = P \times \text{GCD, and}$$

$$\text{HICLK} = Q \times \text{GCD},$$

where P and Q are positive integers. Therefore,

$$\text{DIV} = \text{HICLK/CLK'} = Q/P.$$

And because

$$\text{DIV} = (A \times d + B \times (d+1))/(A+B),$$

$$\text{DIV} = d + (B/(A+B)), \text{ and}$$

$$\text{DIV} = d + x,$$

where x is a positive number equal to or greater than 0 and less than 1, you can use a small amount of algebra on these equations, yielding

$$A + B = P,$$

$$A = P \times (1 - x), \text{ and}$$

$$B = P \times x.$$

These equations indicate that a large GCD results in a low value for P or (A + B). Because the jitter frequency is inversely proportional to (A + B), a large GCD is beneficial because it produces a high jitter frequency that often can be filtered.

Although **Fig 3b** illustrates the p-p jitter on CLK', the diagram doesn't show the jitter on the desired output clock frequency. The counter that divides CLK' by 2 to produce CLK reduces the p-p jitter on CLK relative to CLK' and a close observation of the waveform in **Fig 3b** gives you an estimate of the reduction. In this example A>B and N = 2 where

$$N = \text{ceil } (A/B).$$

The value of ceil (f) is the lowest integer equal to or greater than f. Therefore, the maximum monotonic phase excursion occurs when the multiplexer selects 2 × TCs before selecting a delayed TC. If you chose another example where B>A,

$$N = \text{ceil } (B/A).$$

If B>A and N = 2, the maximum monotonic phase excursion occurs when the multiplexer selects 2 × delayed TCs before selecting a TC.

In general, when A>B and N is even, there is a

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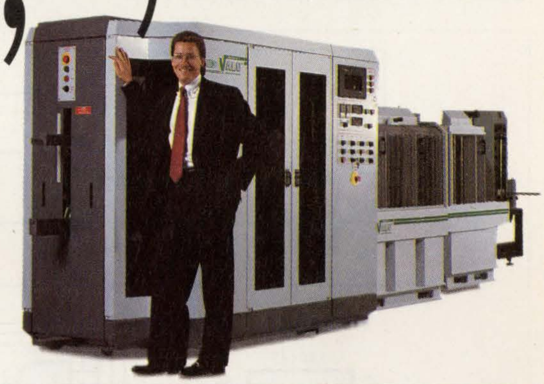

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The technique always synthesizes a clock that runs at twice the desired clock frequency, which you divide by 2 to obtain the desired clock having a 50% duty cycle.

maximum of $N \times$ TCs that produce a peak time lag of $N \times t_1$ sec from a theoretical exact period before one, and only one, delayed TC occurs. When N is odd, the peak time lag is $N-1 \times t_1$ from the theoretical exact period. In addition, because a period of the CLK signal is twice the period of the CLK' signal, 1 period of the CLK signal, which contains a time lead of t_2 due to the delayed TC period, always includes a time lag of t_1 due to the TC period either preceding or following the transition that causes the time lead. Therefore, the peak time lead of the CLK period relative to a theoretical exact period is t_2-t_1. To summarize,

If N = even, the p-p jitter $= N \times t_1 + (t_2 - t_1)$,

where p-p jitter $= (N-1) \times t_1 + t_2$.

If N = odd, the p-p jitter $= (N-1) \times t_1 + (t_2 - t_1)$,

where p-p jitter $= (N-2) \times t_1 + t_2$.

For those situations where B>A and N = ceil(B/A), you then swap t_1 and t_2. Because the p-p jitter of the CLK' signal is always $N \times t_1 + t_2$, the divide-by-2 counter reduces the p-p jitter, but the reduction is most pronounced when N is a small number. Also, the jitter frequency on the CLK sig nal is the same as the jitter frequency on the CLK' sig nal. You calculate the percentage of p-p output jitter by

% p-p jitter = p-p jitter × (CLK frequency in Hz) × 100.

Fig 4 shows a circuit that synthesizes all of the fractional T1 clocks used in private networks. The circuit employs a 9-stage programmable counter, comprising a JK flip-flop (IC_{1A}) and 2 binary counters (IC_2 and IC_3), which divide the HICLK frequency. The 9-stage counter requires a programmable number for each fractional T1 clock given by

PRE-LOAD = 511 − d.

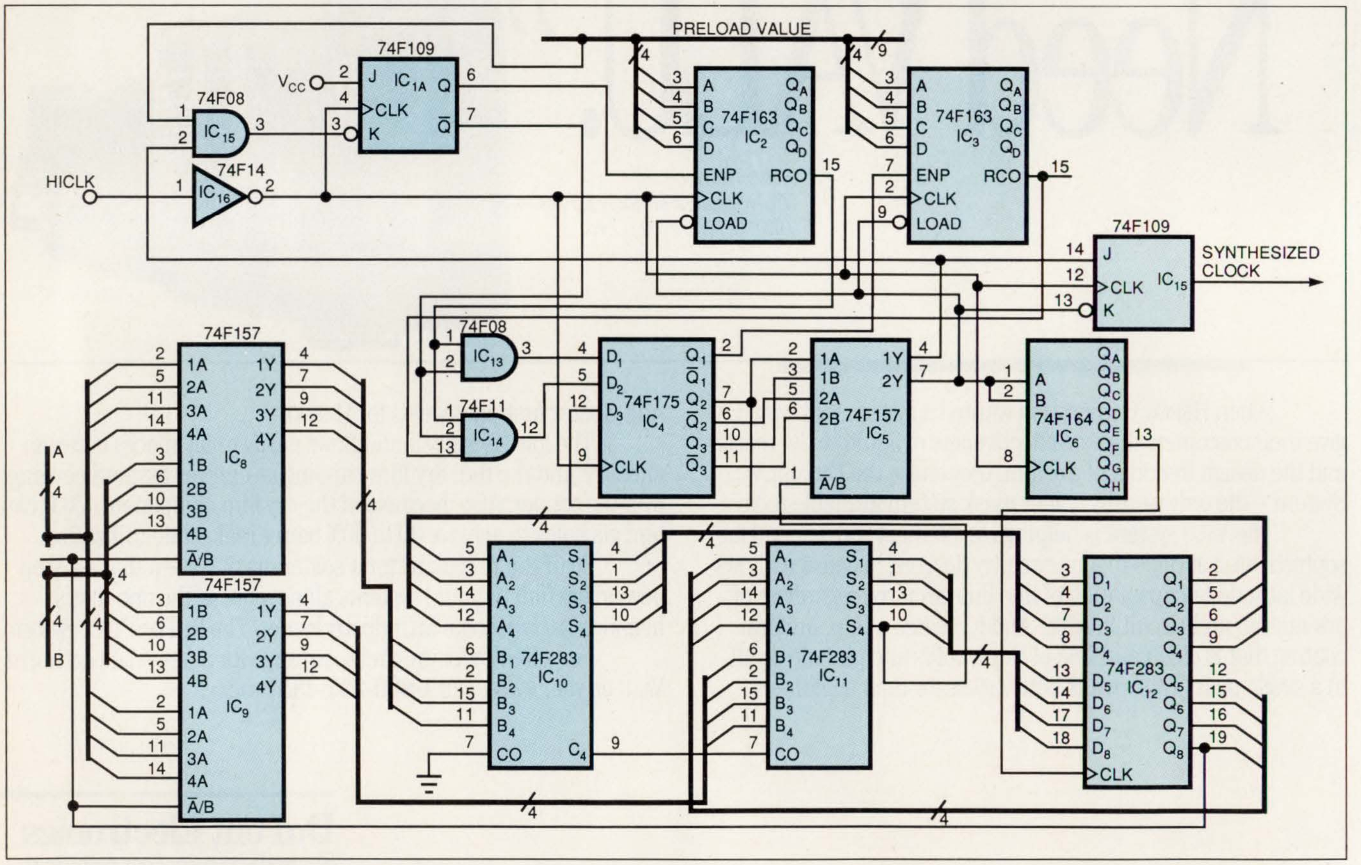

***Fig 4—The circuitry synthesizes all of the fractional T1 clock frequencies.** A µP or a PROM must interface to the circuit to supply the PRE-LOAD value, the A value, and the B value for each synthesized clock.*

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You can reduce the p-p phase jitter by altering the sequence that the multiplexer selects either the terminal count or the delayed terminal count.

Table 2—Fractional T1 clock parameters

Clk (kHz)	DIV	d	Pre-load value	GCD	P	A	B	p-p Jitter ns	% Jitter
56	330.86	330	181	16	7	1	6	42.41	0.24
64	289.50	289	222	64	2	1	1	0.00	0.00
128	144.75	144	367	64	4	1	3	26.99	0.35
192	96.50	96	415	192	2	1	1	0.00	0.00
256	72.38	72	439	64	8	5	3	26.99	0.69
320	57.90	57	454	64	10	1	9	43.18	1.38
384	48.25	48	463	192	4	3	1	26.99	1.04
448	41.36	41	470	64	14	9	5	26.99	1.21
512	36.19	36	475	64	16	13	3	37.11	1.90
576	32.17	32	479	192	6	5	1	35.98	2.07
640	28.95	28	483	64	20	1	19	48.58	3.11
704	26.32	26	485	64	22	15	7	26.99	1.90
768	24.13	24	487	192	8	7	1	40.48	3.11
832	22.27	22	489	64	26	19	7	26.99	2.25
896	20.68	20	491	64	28	9	19	26.99	2.42
960	19.30	19	492	192	10	7	3	26.99	2.59
1024	18.09	18	493	64	32	29	3	47.23	4.84
1088	17.03	17	494	64	34	33	1	50.80	5.53
1152	16.08	16	495	192	12	11	1	44.98	5.18
1216	15.24	15	496	64	38	29	9	39.77	4.84
1280	14.48	14	497	64	40	21	19	26.99	3.45
1344	13.79	13	498	192	14	3	11	38.55	5.18
1408	13.16	13	498	64	44	37	7	44.16	6.22
1472	12.59	12	499	64	46	19	27	26.99	3.97
1536	12.06	12	499	192	16	15	1	47.23	7.25

Note: HICLK = 24 × 1544 kHz

The gates at IC_{13} and IC_{14} select either the TC, to divide the HICLK by d, or the delayed TC to divide the HICLK by d+1. The D flip-flops at IC_4 synchronize the TC and the delayed TC to the HICLK. The multiplexer at IC_5 selects one of the synchronized signals from the divider. The selection depends on the MSB from an accumulator, comprising the 2 parallel adders at IC_{10} and IC_{11} along with the 8-bit latch at IC_{12}.

By entering the value for A as an input to the selector at IC_8 and the 2's compliment value for B as an input to the selector at IC_9, the parallel adders can either add A or subtract B from the accumulator contents. The output of the latch at IC_{11} selects either IC_8 or IC_9. In addition, each output from the multiplexer loads the PRE-LOAD value into the 9-stage programmable counter and the J-K flip-flop at IC_{1B} divides the multiplexer output by 2 to generate the fractional T1 clock. The HICLK signal also clocks the counter at IC_6 to delay the multiplexer's output by 8 HICLK periods before the latch at IC_{11} produces the control signal for IC_8 and IC_9.

The circuit must interface with either a µP or a PROM to provide the PRE-LOAD values for the 9-stage programmable counter, the value for A, and the 2's compliment value for B. These values are different for each synthesized clock. **Table 2** tabulates these values and the other parameters necessary for synthesizing all of the fractional T1 clock frequencies. Although the HICLK equals 24×1544 kHz to generate the tabulated clock frequencies, you could use another HICLK frequency, such as HICLK=32×1544 Hz, to improve the jitter performance. EDN

Author's biography

Sid Ghosh is a telecommunications consultant and has been president of Design Assistance in Crescent City, CA for two years. He has experience in the design of digital cross-connectors, digital loop carriers, multiplexers (T1, Sonet products, and Fiber), and channel banks. He is a senior member of the IEEE and holds BS degrees from Calcutta University and London University. In his spare time he enjoys jogging and hiking.

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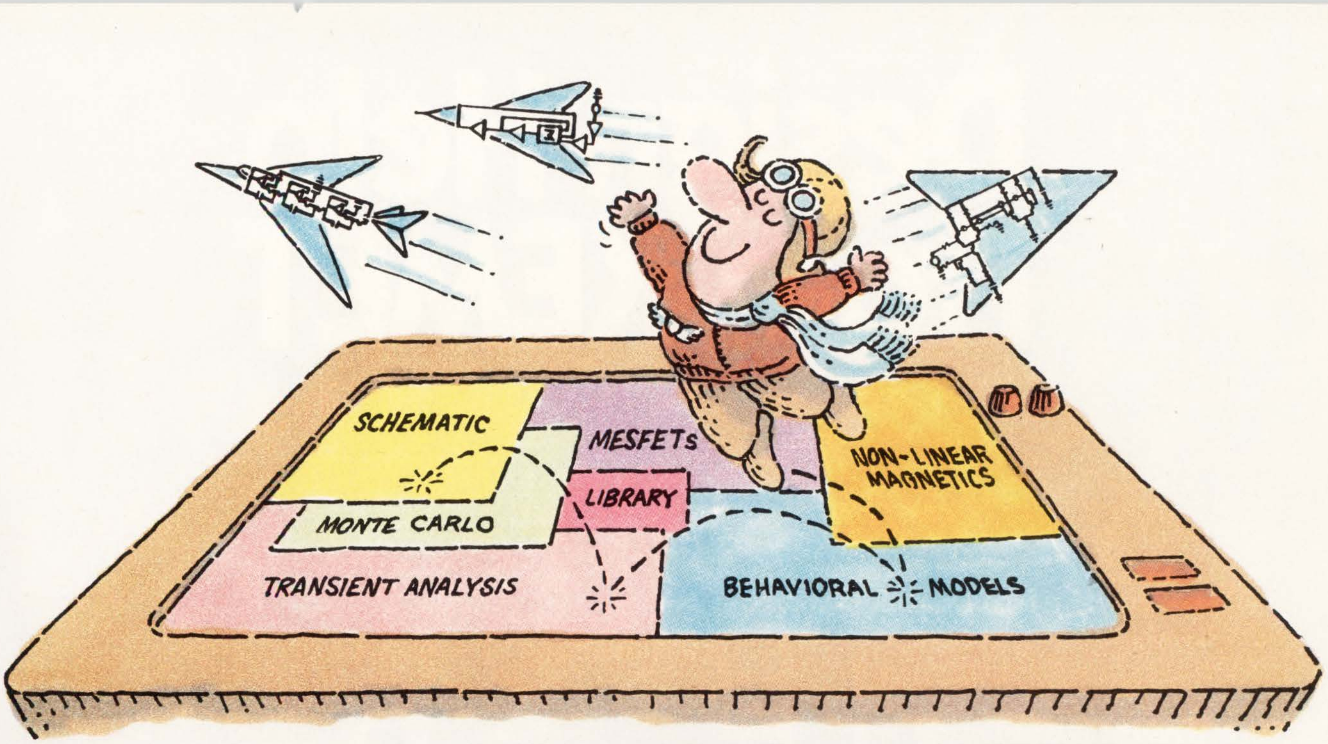

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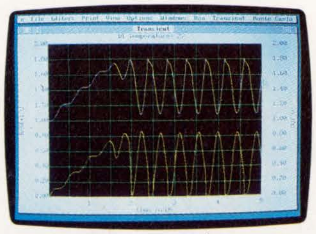

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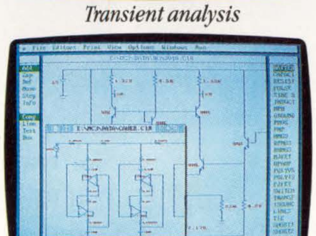

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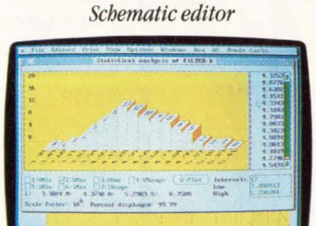

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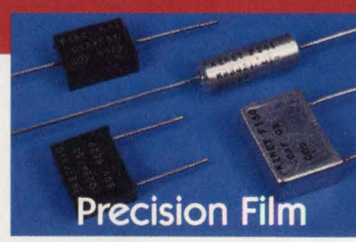

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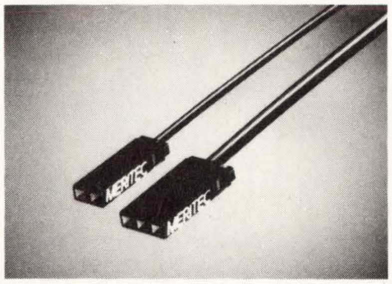

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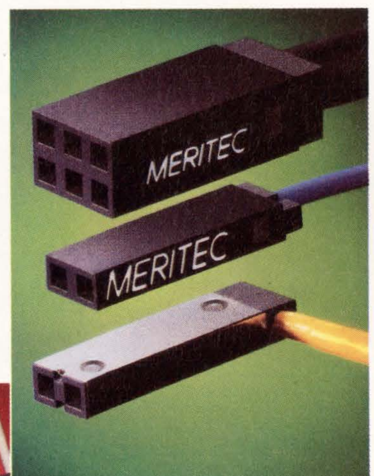

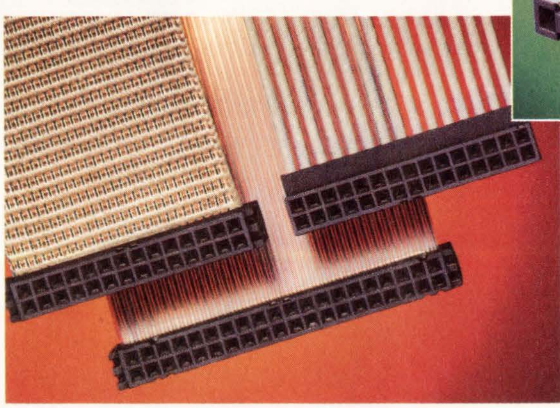

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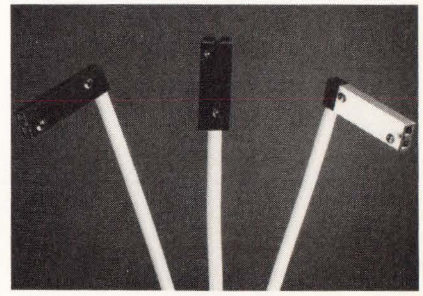

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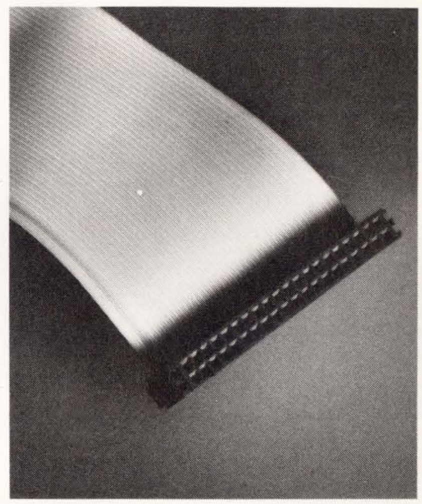

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CIRCLE NO. 131

DESIGN NOTES

Number 44 in a series from Linear Technology Corporation February, 1991

A Simple Ultra-Low Dropout Regulator

Jim Williams

Switching regulator post regulators, battery powered apparatus, and other applications frequently require low drop-out linear regulators. Often, battery life is significantly affected by the regulator's dropout performance. Figure 1's simple circuit offers lower dropout voltage than any monolithic regulator. Dropout is below 50mV at 1A, increasing to only 450mV at 5A. Line and load regulation are within 5mV, and initial output accuracy is inside 1%. Additionally, the regulator is fully short circuit protected, and has a no load quiescent current of 600µA.

Circuit operation is straightforward. The 3-pin LT1123 regulator (TO-92 package) servo controls Q1's base to maintain its feedback pin (FB) at 5V. The 10µF output capacitor provides frequency compensation. If the circuit is located more than six inches from the input source the optional 10µF capacitor should bypass the input. The optional 20Ω resistor limits LT1123 power dissipation and is selected based upon the maximum expected input voltage (see Figure 2).

Normally, configurations of this type offer unpredictable short circuit protection. Here, the MJE1123 transistor shown has been specially designed for use with the LT1123. Because of this, beta based current limiting is practical. Excessive output current causes the LT1123 to pull down harder on Q1 until beta limiting occurs. Under these conditions the controlled pull down current combines with Q1's beta and safe operating area characteristics to provide reliable short circuit limiting. Figure 3 details current limit characteristics for 30 randomly selected transistors.

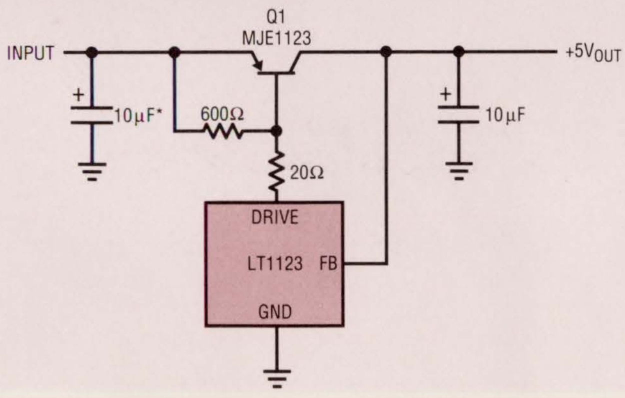

Figure 1. The Ultra-Low Dropout Regulator. LT1123 Combines with Specially Designed Transistor for Lowest Dropout and Short Circuit Profection.

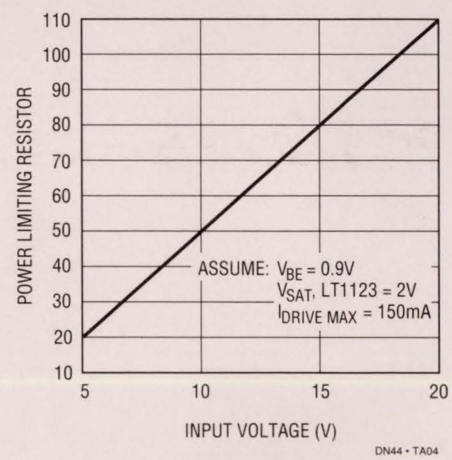

Figure 2. LT1123 Power Dissipation Limiting Resistor Value vs Input Voltage

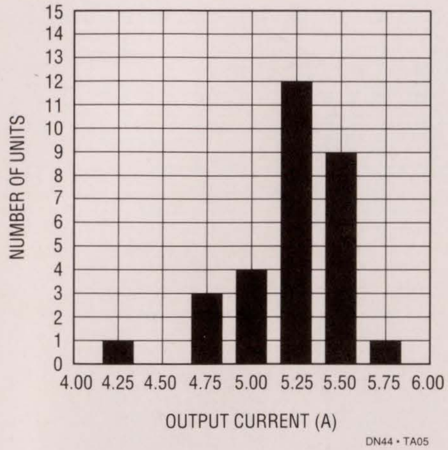

Figure 3. Short Circuit Current for 30 Randomly Selected MJE1123 Transistors at $V_{IN} = 7V$

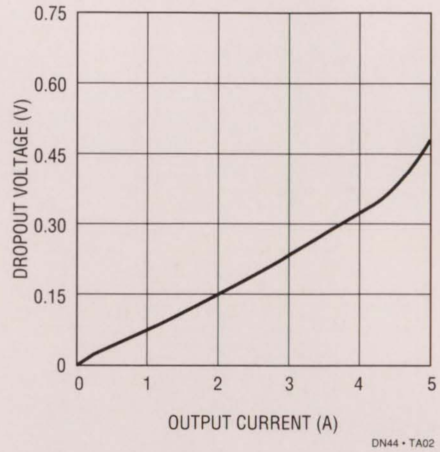

Figure 4. Dropout Voltage vs Output Current

Figure 4 shows dropout characteristics. Even at 5A, dropout is about 450mV, decreasing to only 50mV at 1A. Monolithic regulators cannot approach these figures, primarily because monolithic power transistors do not offer Q1's combination of high beta and excellent saturation. For comparison, Figure 5 compares the circuits performance against some popular monolithic regulators. Dropout is ten times better than 138 types, and significantly better than the other types shown. Because of Q1's high beta, base drive loss is only 1%-2% of output current, even at full 5A output. This maintains high efficiency under the low $V_{IN} - V_{OUT}$ conditions the circuit will typically operate at. As an exercise, the MJE1123 was replaced with a 2N4276, a Germanium device. This combination provided even lower dropout performance, although current limit characteristics cannot be guaranteed.

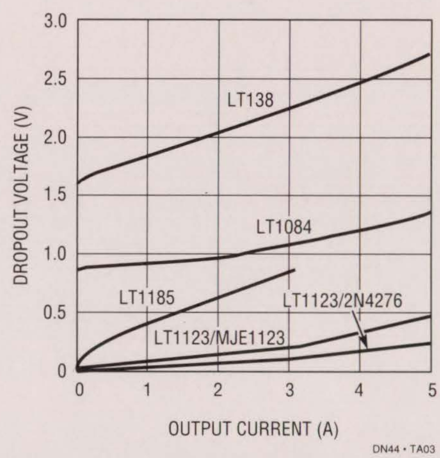

Figure 5. Dropout Voltage vs Output Current for Various Regulators

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EDITED BY CHARLES H SMALL

Power booster operates efficiently

A Simopoulos
Conversion Devices Inc, Brockton, MA

The power booster in **Fig 1** functions as either a high-efficiency "power multiplexer" or, if you supply an external signal-source, as a high-power linear amplifier.

If you want to drive a load with a high-power square wave, the circuit simply draws power from two external power sources, V_1 and V_2, alternately. In this mode, the circuit's power-handling devices function as switches, dissipating minimal power. The RC time constant of the integrator, IC_1, determines the circuit's oscillation period. The integrator's triangle-wave output drives a simple triangle-to-square-wave converter.

If you supply an external drive waveform, the circuit functions as a linear amplifier, and, consequently, inherently dissipates a varying portion of that power. The power amplifier is stable for gains ≥15.

Diodes D_1 and D_2 limit the FET's gate-voltage swing to less than 15V. D_3 is a dual Schottky diode that protects the FETs from short circuits between the two supplies, V_1 and V_2, through an FET's parasitic diode. With D_3 in place, you can choose either power channel for the higher voltage input.

To drive the FETs, Q_5 and Q_6, at switching frequencies greater than 1 kHz, you will have to employ gate drivers for them. **(EDN BBS /DI_SIG #922)** **EDN**

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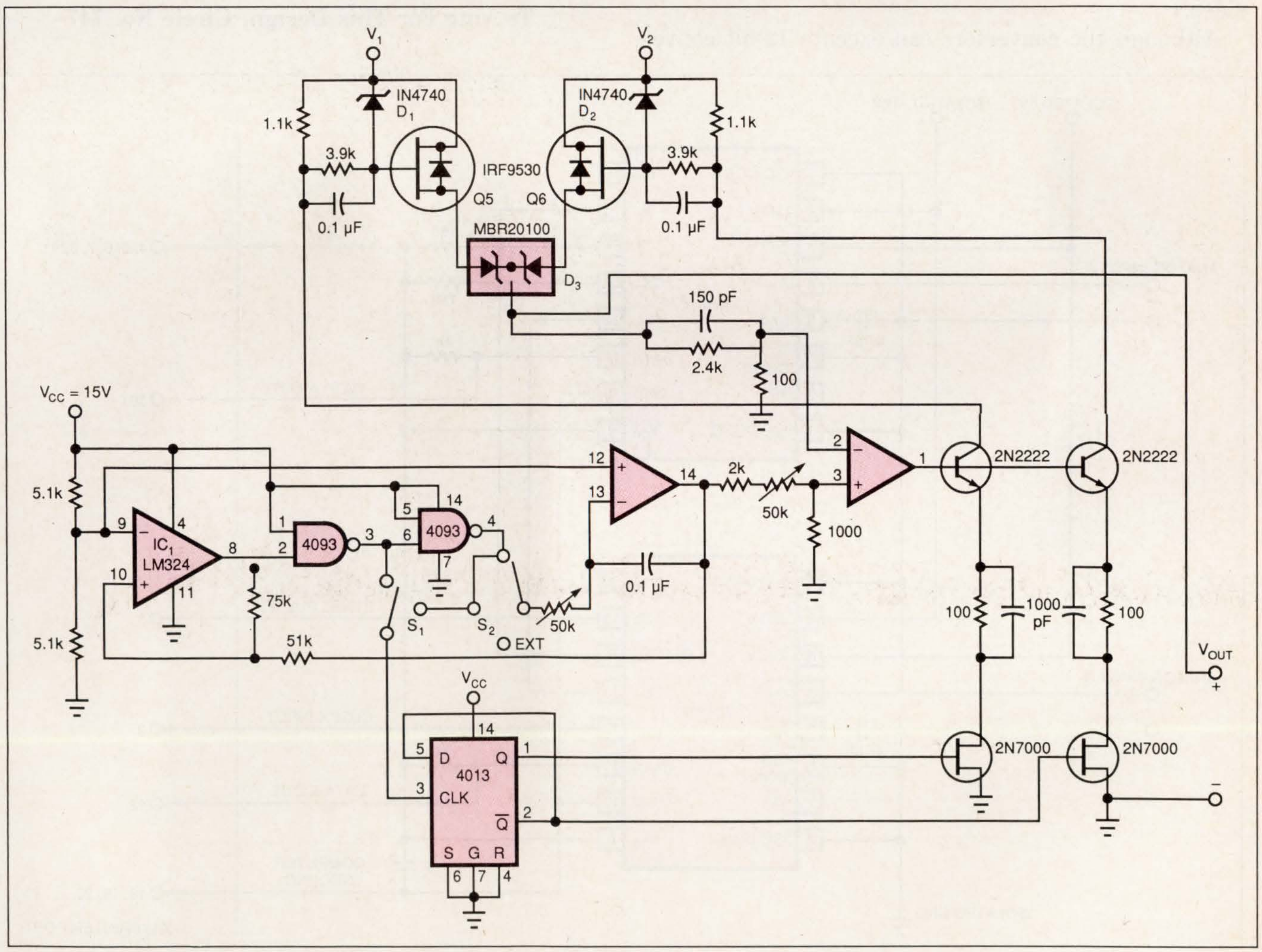

Fig 1—This power booster works as either a switch-mode power multiplexer or a linear amplifier.

A/D board hooks to IBM PC printer port

Bob Underwood
Maxim Integrated Products, Sunnyvale, CA and
Mark Underwood
Cupertino, CA

An IBM PC can operate the two 12-bit A/D converters in **Fig 1** via its printer port. The converters' serial outputs use only two of the printer port's eight data lines (DATA A OUT, DATA B OUT). Because the IBM PC's printer port supplies no power, interface software running on the PC programs the six unused data lines high. Busing these data lines provides power for the digital portion of the A/D converters. (The converters have internal optoisolators. Consequently, you must provide isolated supplies for their analog sides.)

Although the converters can execute 12-bit conversions in 6 μsec, the slow software-driven approach used in this Design Idea stretches conversion periods out to about 100 μsec (depending on your PC's clock speed).

The circuit takes advantage of the converters' optoisolator inputs to put their clock and start inputs in series. Therefore, the converters operate synchronously.

The accompanying software starts the conversions, issues clock pulses, reads the data bits as they become available, and stores them in memory. The **listing** is too long to reproduce here; you can obtain it from the EDN BBS (617-558-4241, 2400, 8, N, 1).
(EDN BBS /DI_SIG #924)

To Vote For This Design, Circle No. 747

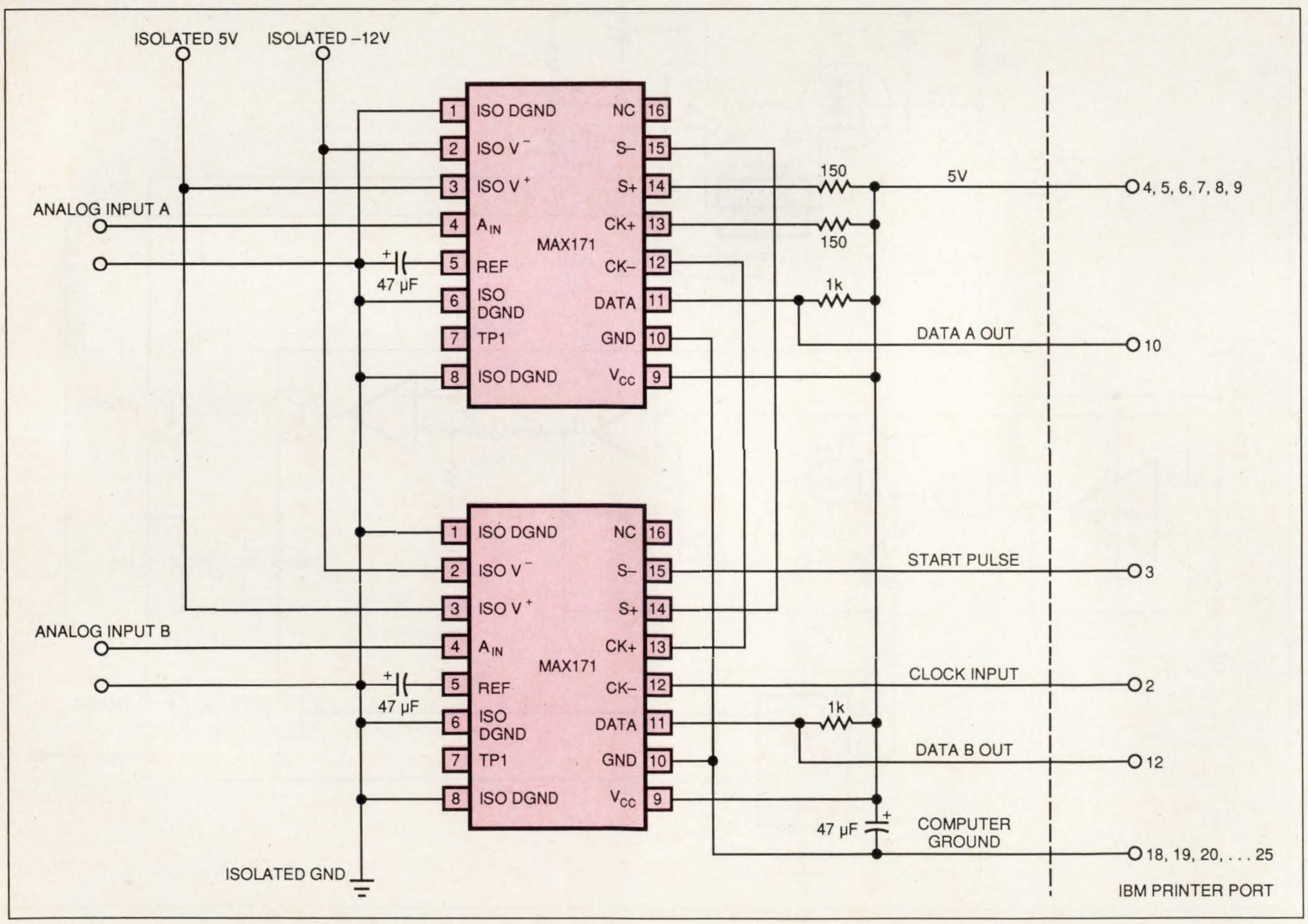

Fig 1—This IBM PC A/D converter board *derives computer-interface power from unused printer-port data lines.*

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RF input, max dBm (no damage)	22	22	26
VSWR (on), typ		1.4	
Video breakthrough to RF, typ (mV p-p)		30	
Rise/Fall time, typ (nsec)		3.0	

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CIRCLE NO. 132

F141 REV. ORIG.

Filter antialiases and sinc compensates

Gary Sellani
Maxim Integrated Products, Sunnyvale, CA

Two dual-biquad filter chips and some external components **(Fig 1)** form a multipurpose filter for reconstructing D/A converter signals. Connected to a converter's output, the filter provides antialiasing, reduces the D/A converter's quantization noise, and compensates for sin(πx)/(πx)—the "sinc" function—attenuation.

The sinc-function attenuation stems from the nature of the rectangular pulses that compose the converter's output. This attenuation reduces the output signal by almost −4 dB at frequencies corresponding to half the converter's sample rate.

The circuit incorporates an inverse-sinc function that operates to one-third of the converter's sample rate. Beyond one-third, the filter's response shifts to a stopband filter's, providing −70-dB attenuation. This attenuation conforms to the converter's inherent signal-to-noise ratio and quantization error.

To prevent aliasing, the stopband edge must be no

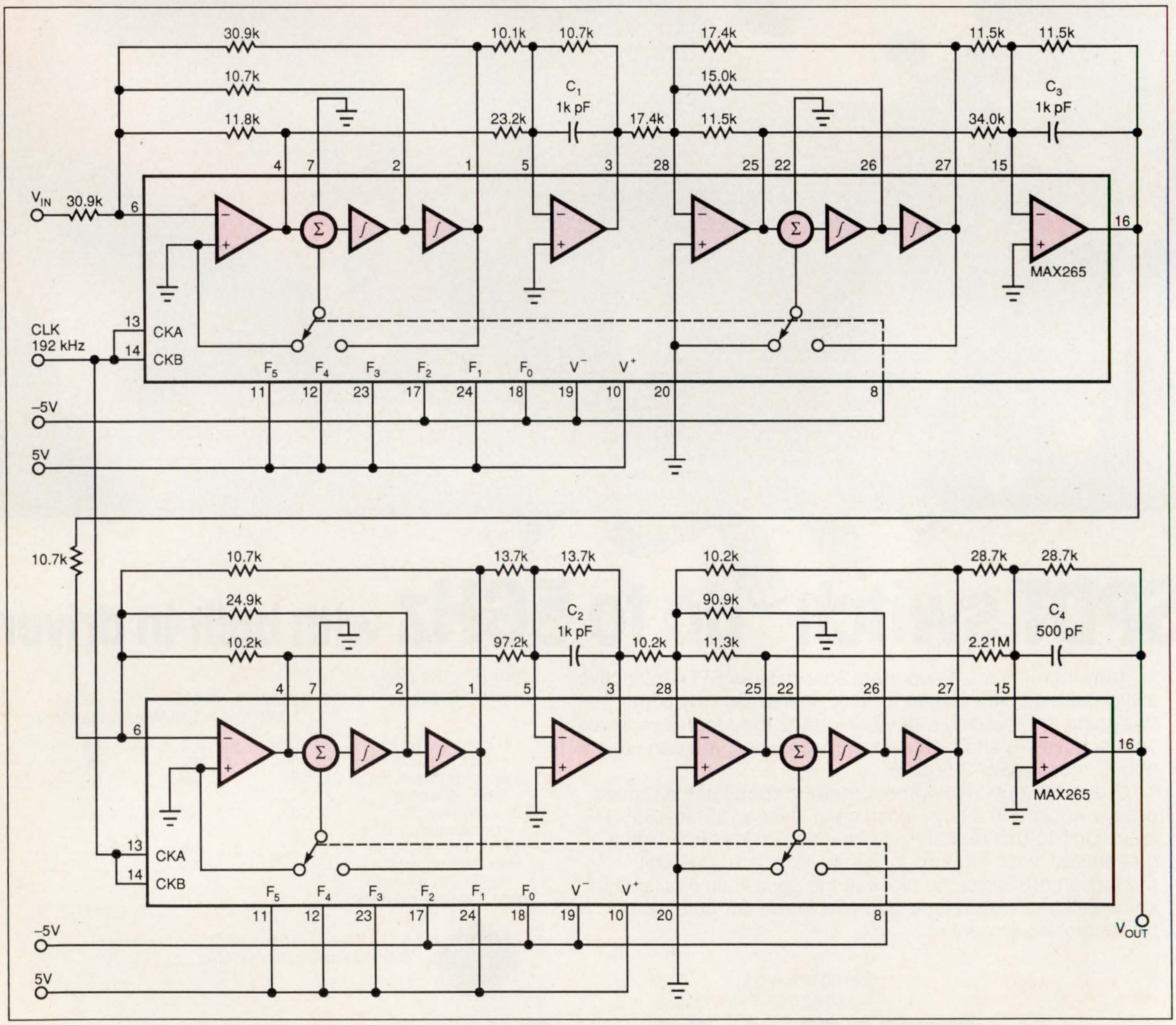

Fig 1—This circuit not only filters out high-frequency aliases and quantization noise, it provides sinc-function compensation.

higher than the Nyquist frequency ($f_S/2$). To achieve 70-dB stopband rejection with this eighth-order filter requires a transition ratio ($f_{STOPBAND}/f_{PASSBAND}$) of 1.5, which sets the passband's upper limit at $f_S/3$.

To ensure maximum dynamic range, the four filter sections exhibit increasing Q from input to output. The pole-zero pairs of each section also exhibit increasing frequency, minimizing the different component values required.

Note the feedback capacitors C_1 through C_4 across each filter chip's output op amps. These capacitors have two purposes: they improve the quality of transmission zeros, and they form 1-pole lowpass filters that help to smooth out the discrete-level steps which the filters' switched-capacitor action introduces. These 1-pole filters have little effect on the passband's shape because their high corner frequencies introduce only 0.1 dB of loss at 1 kHz.

Note also that you can apply a simple divide-by-64 circuit to the 192-kHz clock frequency to set the necessary 3× ratio between the converter's sample rate and the filter's 1-kHz corner frequency. The V^+, V^-, and the F_0 through F_5 connections program each filter chip for an f_{CLK}/f_0 ratio of 191.64.

(EDN BBS /DI_SIG #921) EDN

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FEEDBACK AND AMPLIFICATION

Numerous improvements suggested

I would like to suggest improvements for three of the Design Ideas presented in the October 1, 1990, issue of EDN.

First, for Francesco Ruggiero's "Scrambler disguises voice signals" on pg 127, note that the EP pin of the top 74HC161 is floating—a dangerous practice. And because the 74HC161 generates its CO (carry-out) asynchronously, runt pulses at its CO pin, arising from differences in propagation time, can cause problems for unclocked logic. I suggest readers first tie the EP pin to 5V. Then cut the CO connection to pin 3 of the 74HC74 flip-flop, and instead connect pin 11 of the top 74HC161 to the flip-flop.

Next, for Tarlton Fleming's "S/H circuit multiplexes op amp" on pg 128, I see problems with the drawing of the left-hand switch. R_1 should be inside the feedback loop for op amp stability; leakage and capacitance are less on the switched pin of the CMOS switch than

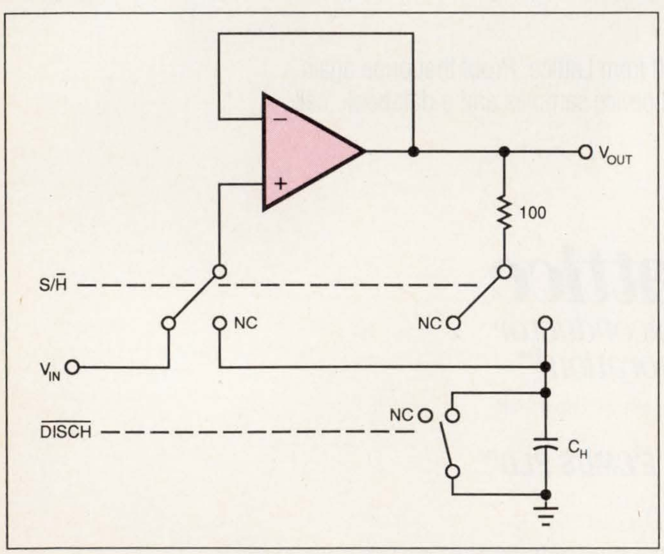

Fig 1—Revising the topology *of an S/H circuit improves its performance.*

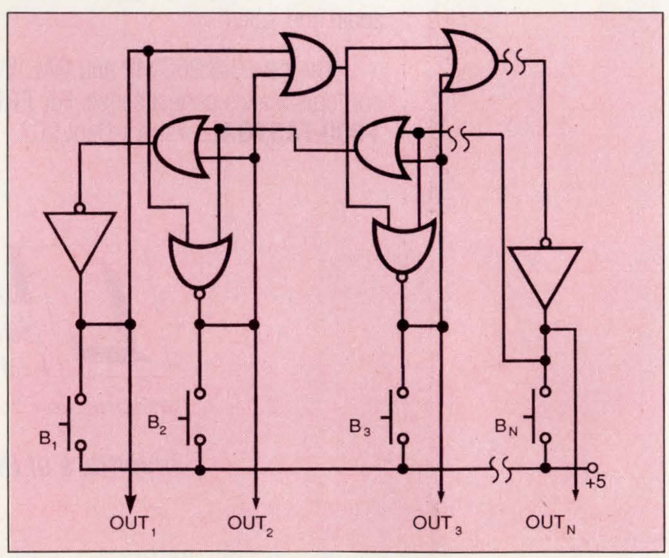

Fig 2—Stiffer drive current *and multiple-keypress lockout enhances the performance of an interlocked switch circuit.*

CIRCLE NO. 133

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FEEDBACK AND AMPLIFICATION

on the common pin. Also, parts cost drops from $3.50 (1000) to $1 (100) if you use a generic 74HC5043 triple dpst switch rather than a quad switch. **Fig 1** shows my suggested redesign.

Lastly, Tian Jin Qin's "Inverters mimic interlocked switches" on pg 132 also has problems. First, the circuit won't always switch. If you use CMOS logic, the worst-case current through B_1, C, R_3, S, and D_{1B} available to a switch, assuming a 5V ±10% supply, is 5.5 mA. For the circuit to work correctly, this current should be larger than the maximum inverter sink current, or at least 20 mA. Next, the circuit has an indeterminate state at power-on. Lastly, you could inadvertently turn on multiple outputs by pressing more than one button simultaneously. **Fig 2** shows my suggested revision.

Larry K Baxter, VP Engineering
Echolab Inc
175 Bedford Rd
Burlington, MA 01803
(617) 273-1512

Author corrects equations

The Design Idea I contributed, "Passive network is totally resistive" (EDN, August 2, 1990, pg 135), contains two errors. The equation for L should be

$$L=\frac{R}{\omega_0}=\frac{R}{2\pi F_0},$$

and the equation for C should be

$$C=\frac{1}{\omega_0 R}=\frac{1}{2\pi F_0 R}.$$

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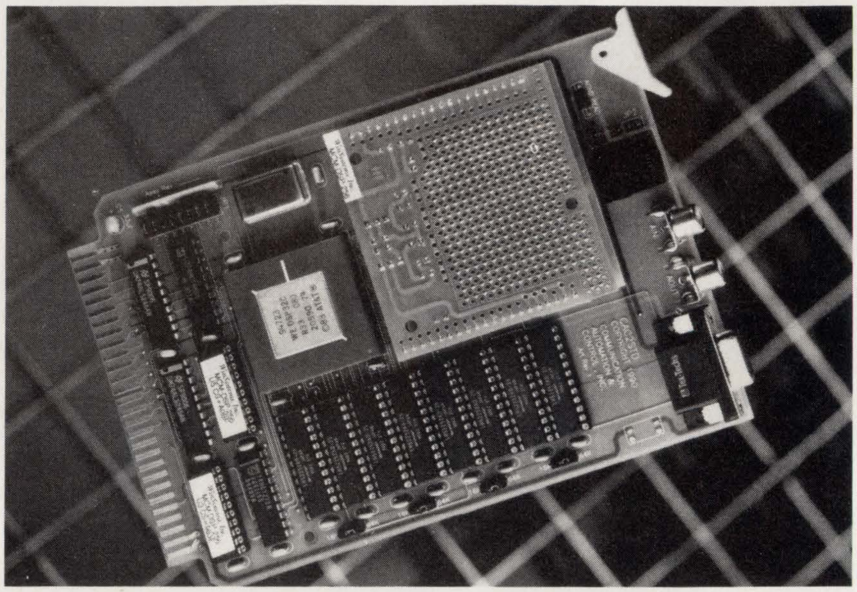

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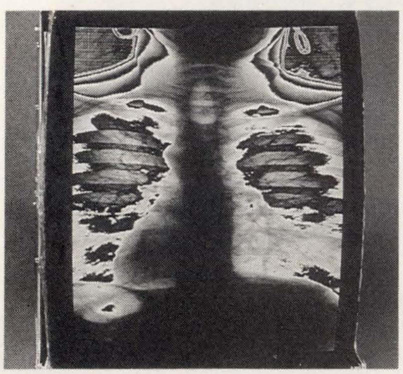

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The GMA212 19-in. gray-scale display, which is designed for medical imaging, has 1536×2048 pixels. The monochrome display's use of a P45 phosphor and a 31% transmission filter provides an ideal combination for soft-copy diagnostics on x-ray images. Other features include a 200-MHz video bandwidth, brightness and contrast controls, and enough dynamic range to display 256 shades of gray. The display uses a high-frequency switching power supply. It has a digitally correcting focus and astigmatism device, which displays well-focused images in the corners. The display weighs 55 lbs and measures 19.625×14.0×19.8 in. $7000.

Tektronix Display Products, Box 500, M/S 46-943, Beaverton, OR 97077. Phone (800) 835-9433, ext 2002; in OR, (503) 627-5000. FAX (503) 627-1070. TLX 192825. **Circle No. 365**

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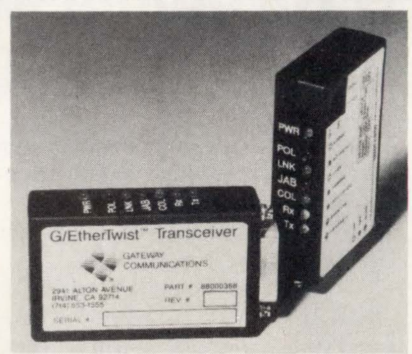
The G/Ethertwist transceiver for Ethernet networks can interconnect coaxial and unshielded twisted-



pair (UTP) networks. The transceiver, which complies with the IEEE-802.3 10Base-T Ethernet standard, allows adapters, fan-outs, and repeaters to operate using UTP wires. The unit's RJ-45 jack provides an interface for the UTP-wired section and a male attachment-unit-interface connector to interface with the coaxial section. The transceiver transmits and receives data, detects data collisions on the network, and performs heart-beat or signal-quality error tests. Seven

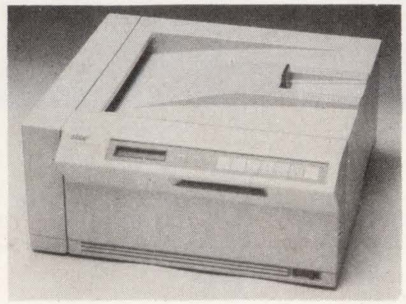
LEDs indicate power, polarity, link, transmit, receive, jabber, and collision. The unit measures 1.6 × 0.7 × 2.7 in. and weighs 2 oz. $150.

Gateway Communications Inc, 2941 Alton Ave, Irvine, CA 92714. Phone (800) 367-6555; in CA, (714) 553-1555. FAX (714) 553-1616.

Circle No. 366

Laser Printer

- *Uses an i960 μP to print at 4 pgs/minute*
- *Has 1M byte of RAM and 14 internal fonts*



The Star Laserprinter 4 uses Intel's i960 RISC μP. Its 1M byte of RAM ensures a maximum print speed of 4 pgs/minute when printing a full page of graphics at 300 dpi. You can expand the memory in 1M, 2M, or 4M increments to store downloaded fonts. The unit is software and hardware compatible with HP's Laserjet IIP; its 14 internal fonts are virtually identical to the LaserJet II Series fonts. In addition, the printer accepts LaserJet II Series font cartridges, toner cartridges, and a lower-level paper cassette. Other features are a Centronics parallel port and an RS-232C port. $1395.

Star Micronics America Inc, 420 Lexington Ave, Suite 2702, New York, NY 10170. Phone (800) 447-4700; in NY, (212) 986-6770. FAX (212) 286-9063. **Circle No. 367**

Development Board

- *Connects to a PC compatible for 80C51 μCs*
- *Has an 80C552 μC and a monitor program in 32k-byte EPROM*

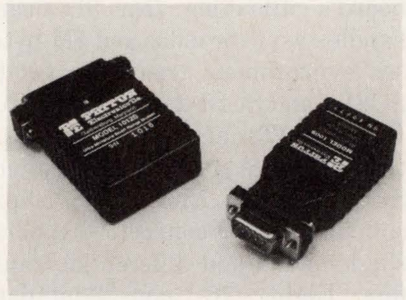
The DB-51 development board has sockets that accept any member of the 80C51 family of microcontrollers. An 80C552 microcontroller runs a monitor program in a 32k-byte EPROM, a programmed 87C751 microcontroller, 32k bytes of RAM, and a 1¼ × 7¼-in. prototyping area that gives you access to all of the microcontroller's signals. The board connects to an IBM PC or compatible running MS-DOS via an RS-232C link. The host must have a minimum of 512k bytes of RAM and a hard- or floppy-disk drive. Software for the host includes a symbolic debugger, an online assembler and disassembler, and upload and download utilities. You can write programs in assembly code or in C language or PLM, and you can display the contents of all the registers on the screen. Board for the 80C552 and software, $320.

Signetics Co, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-3445. **Circle No. 368**

Short-Range Modems

- *Have built-in surge protection for RS-232C links*
- *Operate over two twisted-pair lines*

Two asynchronous short-range modems are available with built-in surge protection. They use silicon avalanche diodes to protect internal circuits and external equipment. The Model 1009S can communicate at a distance of 17 miles and at data rates as fast as 19.2k bps. It receives its power by detecting the data. The unit measures 2.5 × 0.75 in. and has a DB-9 connector. The Model 1012S has transformer isolation for protection against signal disruptions. It operates in asynchronous networks having as many as 10 terminal drops. The 1012S also receives its power by detecting the data; it operates at a distance of 6 miles and at data rates as fast as 19.2k bps. Measuring 2.66 × 0.73 in., the 1012S has a DB-25 connector. Both models operate over two twisted-pair wires and handle peak surges of 600W/wire. Model 1009S, $75; Model 1012S, $120.



Patton Electronics Co, 7958 Cessna Ave, Gaithersburg, MD 20879. Phone (301) 975-1000. FAX (301) 869-9293. **Circle No. 369**

VMEbus SCSI-2 Adapter

- *Transfers data to SCSI-1 and SCSI-2 disk drives*
- *Handles 32-bit VMEbus transfer rates at 30M bytes/sec*

The RF3560, the latest member of the Rimfire family of intelligent SCSI host adapters, supports the SCSI-2 mandatory commands, command sets, and command queuing. It runs directly from a host operating-system's I/O command queue and controls data transfers independently. Tasks such as transferring SCSI messages, peripheral status, and error recovery between the host and as many as SCSI-2 peripherals take place during the board's offloading. The 6U board handles asynchronous and 5M-byte/sec synchronous transfer rates to SCSI-1 and SCSI-2 disk drives, CD-ROMs, DATs, and helical scan-tape transports. A face-plate mounted, SCSI-2, 50-pin ribbon or a 50-pin subminiature D connector supports single-ended and differential transfers. Eight-, 16-, and 32-bit data transfers on the VMEbus occur at rates as fast as 30M bytes/sec. $1495.

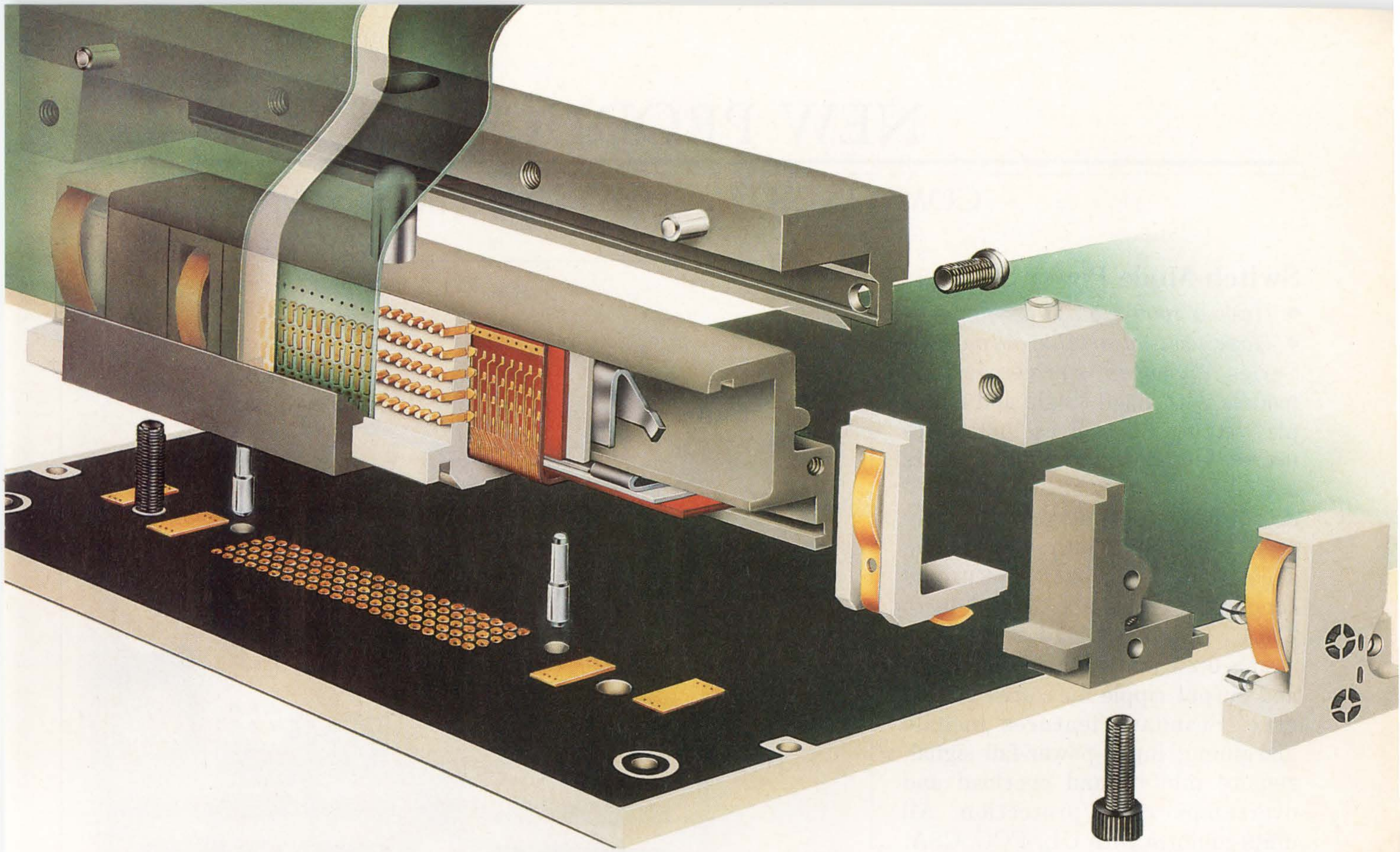
Ciprico Inc, 2955 Xenium Ln, Plymouth, MN 55441. Phone (612) 559-2034. **Circle No. 370**

VMEbus Single-Board Computer

- *Utilizes a RISC CPU based on MIPS chip set*
- *Contains a SCSI and an Ethernet controller*

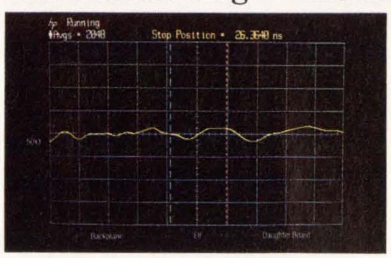
The Pacerunner/3400 is a VMEbus single-board computer (SBC) in a 6U form factor. It uses either a 25- or 33-MHz version of the company's PR3400A CPU. The CPU integrates the integer and floating-point unit of the MIPS RISC chip set. The board also utilizes the company's PR3100 chip. Some features are an 8-word write buffer, a programmable 32-word read buffer, and parity logic. The board provides 64k bytes of instruction cache and 64k bytes of data cache, both of which are expandable to 256k bytes. The SBC's 4M bytes of dynamic RAM is expandable to 16M bytes. The board's 53C700 SCSI controller and a 79C900 Ethernet controller both have on-chip DMA controllers. Two RS-232C ports, three 16-bit counter/timers, a watchdog timer with a time of day clock, and 50 bytes of nonvolatile RAM are also available. 25-MHz version, $9995; 33-MHz version, $10,995.

Performance Semiconductor Corp, 610 E Weddell Dr, Sunnyvale, CA 94089. Phone (408) 734-8200, ext 384. **Circle No. 371**



Out of sight performance!

Introducing the next generation interconnect, EII : transparent to high frequency signals, therefore eliminating connector induced signal distortion. Until now, the limiting factor for signal integrity in high speed electronic circuits has been the connector. The source may be matched to the load, but an impedance mismatch at the connector degrades performance. Signal integrity through EII is maintained because reflection, crosstalk, attenuation, signal skew, and rise-time degradation are reduced to absolute minimums.



EII achieves matched impedance of the connector to the backplane and daughter card.

This unprecedented performance is made possible by a unique flexible microstrip transmission line structure with a continuous ground-plane as the major signal path through EII. Augat, the company known for quality and innovation, is now setting a new standard of performance – EII. Outta' sight!

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Attleboro, MA 02703
(508) 222-2202
FAX:(508)222-0693

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

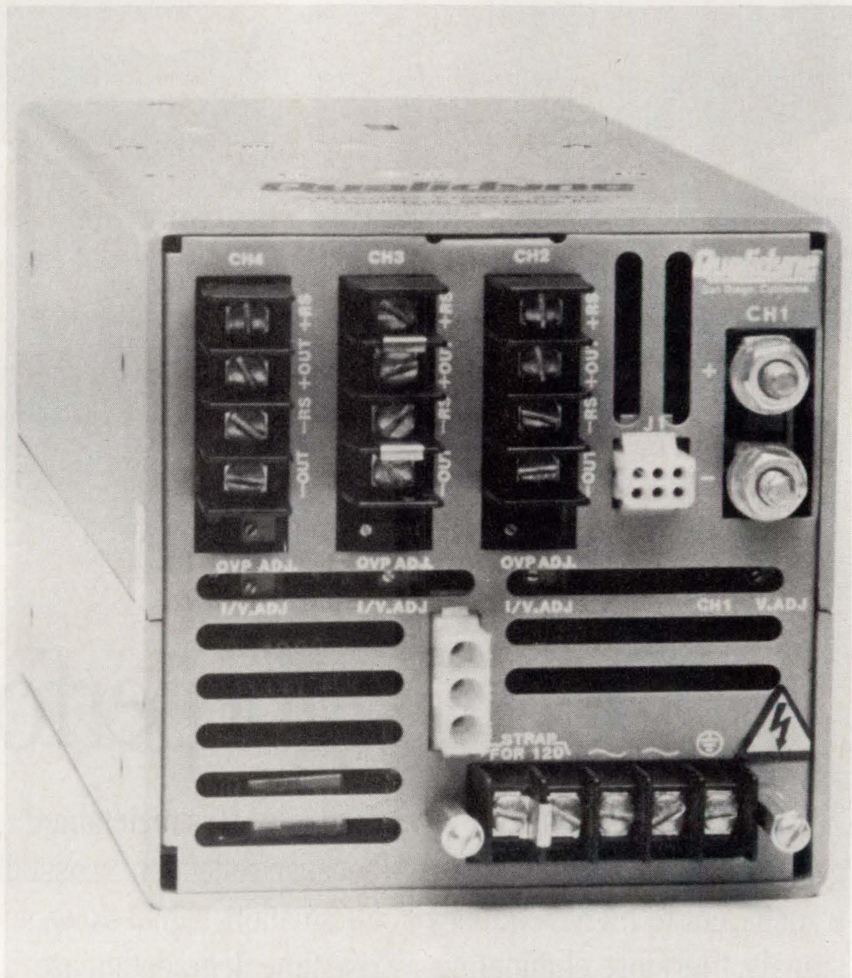
Switch-Mode Power Sources

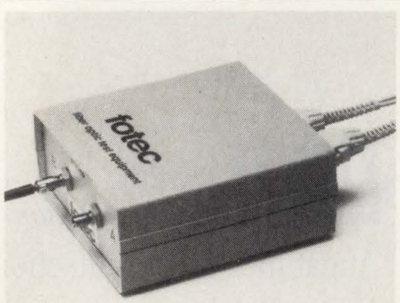
- *Have a 1000W output*
- *Have user-adjustable outputs*

Series 28 power sources include models with fixed single and multiple outputs as well as units with user-adjustable outputs. The units accept inputs of 120/240V ac or 48V dc. Multiple-output versions provide three or four outputs including a 5V/120A main output. Outputs range from 2 to 56V dc and 10 to 250A. Line and load regulation equals 0.2% and 0.8%, respectively, and output ripple measures 1% p-p max. Standard features include margining, input power-fail signal, remote inhibit, and overload and overtemperature protection. All units conform with UL, FCC, CSA, and VDE safety and EMI requirements. Standard options include output power-good signal and automatic current-sharing capability. Single-output models, $661 to $795; multiple-output versions, $717 to $1034.

Qualidyne Systems Inc, 3055 Del Sol Blvd, San Diego, CA 92154. Phone (619) 575-1100. FAX (619) 429-1011. TLX 709029.

Circle No. 383





Optical Tap

- *Tests operational networks*
- *Introduces 1.5-dB loss*

The A 175-FDDI Fotap optical tap plugs into FDDI networks and diverts a small amount of optical power to test equipment. The unit allows you to perform tests during network operation. The device looks like a bypassed station to an FDDI network. It introduces 1.5-dB link loss and provides a calibrated optical output, which is approximately 10 dB down from the actual FDDI ring level. You can then use this optical signal with appropriate test equipment to measure link power or convert the tap output to electrical signals for use with oscilloscopes or logic analyzers. $950.

Fotec Inc, Box 246, Boston, MA 02129. Phone (800) 537-8254; in MA, (617) 241-7810. FAX (617) 241-8616. TLX 501372. **Circle No. 384**

VXIbus Backplane

- *Features a 100-MHz clock line*
- *Includes separate TTL and ECL signal lines*

These D-sized backplanes are designed to revision 1.3 of the VXIbus specification. Developed for use with P1, P2, and P3, 96-pin press-fit connectors, the backplanes feature a 100-MHz clock line and synchronized signal lines for high speed applications. Four parallel ECL trigger lines provide inter module triggering at rates in excess of 100-MHz, and the ECL star lines offer precision timing. Separate TTL and ECL signal layers ensure controlled impedance for each logic family and

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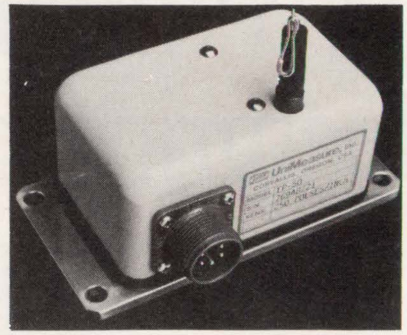
keep propagation delays within critical timing parameters. The backplanes feature a 12-layer stripline construction. Four ground and four power layers make up the distribution system for −5.2, −2, 5, ±12, and ±24V. Available in 5- and 13-slot versions, the units utilize 24 local bus lines for communication between adjacent modules. The units also feature protection that meets the SUMBUS revision. 13-slot model, from $2415; 5-slot version, $1015.

Augat Inc, Box 779, Attleboro, MA 02703. Phone (508) 222-2202. FAX (508) 222-0693.

Circle No. 385



Position Transducer

- *Available in metric versions*
- *Has a TTL-compatible output*

The EP Series of digital linear position transducers consists of four English versions and four metric models. Maximum measurement capability ranges from 10 to 500 in. All models have ±0.05% accuracy, and resolutions range to 0.002 in. The transducers operate from a 5V dc input and provide a 2-channel, TTL-compatible output signal with phase quadrature. A differential output is available as an option. The transducers are housed in an aluminum case and have an operating range of 0 to 70°C. From $495.

UniMeasure Inc, 7055 NW Grandview Dr, Corvallis, OR 97330. Phone (503) 757-3158. FAX (503) 757-0858. **Circle No. 386**

Neon Indicators

- *Are UL listed*
- *Rated for 105°C*

The 5/16-in. diameter neon indicators in the 2100 Series operate from 110 or 220V. UL and CSA listed, the 48 models are divided into three families. Model 2110 devices are supplied with raised nylon bezels and lenses; Model 2120 indicators feature flush, low-profile lenses with nylon bezels, and the Model 2150 group has stove-pipe lenses with chrome bezels. All units incorporate nylon housing and polycarbonate lenses and are rated for operation at 105°C. The indicators are available in a range of lens colors and come with prestripped wire

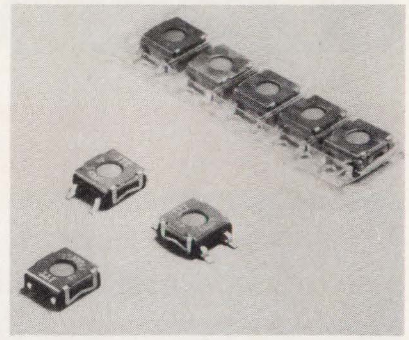
leads or tinned, male quick-connect terminals. Standard variations include a choice of lenses, leads, terminations, and body finishes. From $0.45 (OEM qty).

Industrial Devices Inc, 260 Railroad Ave, Hackensack, NJ 07601. Phone (201) 489-8989. FAX (201) 489-6911. **Circle No. 387**

Surface-Mount Keyswitches

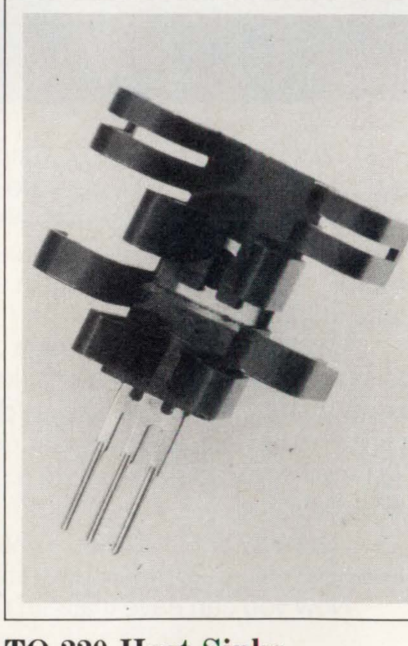
- *Available with or without actuators*
- *Have a sealed design*

KSC keyswitches are available with or without actuators. The units come with a choice of operating force—160, 300, or 500g. The switches are offered with either sil-



ver or gold contacts and a choice of either J-lead or gull-wing terminations. The units are totally sealed and will accommodate double-wave, infrared, and vapor-phase soldering techniques. To accommodate pick-and-place machines, the switches are supplied in thermoformed tape on reels of 500 pieces. $0.25 to $0.50. Delivery, stock to eight weeks ARO.

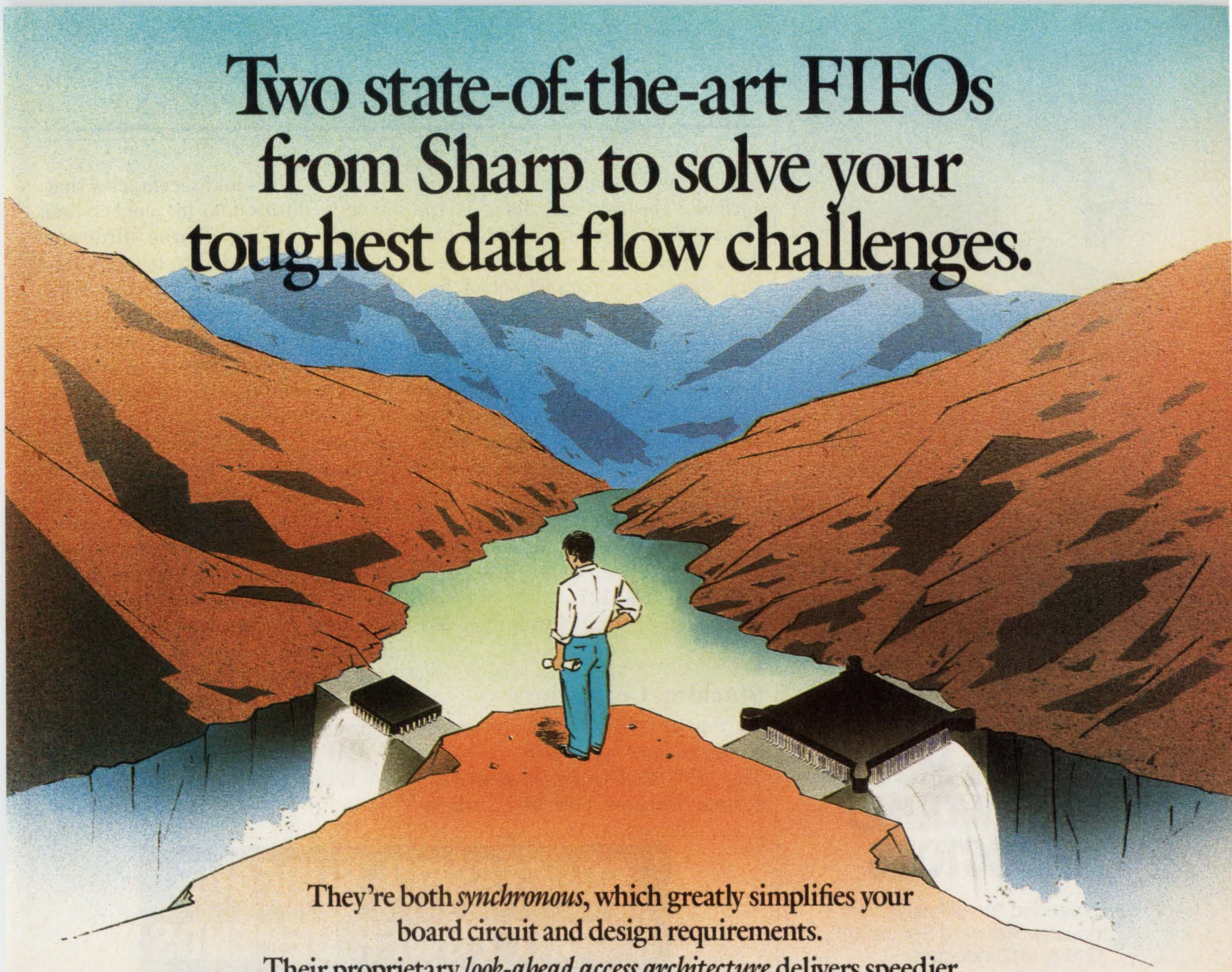
ITT Schadow Inc, 8081 Wallace Rd, Eden Prairie, MN 55344. Phone (612) 934-4400. TLX 290556. **Circle No. 388**



TO-220 Heat Sinks

- *Have a spring retainer*
- *Mount vertically or horizontally*

The Spider heat sinks have an integral spring retainer that holds the TO-220 semiconductor package



Their proprietary ***look-ahead access architecture*** delivers speedier access and cycle times while reducing power consumption.

Introducing: The LH5492 4K x 9 Clocked FIFO.

Sharp's new LH5492 is a dual-port clocked FIFO, with a 4K x 9 configuration. The clocked interface is a significant enhancement in FIFO design over previous asynchronous parts. The clocked enables on the LH5492 eliminate the requirement to shape waveforms, resulting in simpler design tasks, and lower parts count.

Its high-speed clocked interface can be used directly with the typical 40%/60% duty cycle system clock. And a separate $\overline{OE}$ control signal provides independent control over output buffers.

The second enable pin on each part can be directly tied to the flags to simplify external logic requirements.

The LH5492 4K x 9 clocked FIFO comes in a 32-pin PLCC. It is available with access times of 20 ns, 25 ns and 35 ns, and cycle times of 25 ns, 35 ns and 50 ns, respectively.

Introducing: The LH5420 256 x 36 x 2 Bidirectional FIFO.

Sharp's new LH5420 is actually two 256 x 36-bit FIFOs in one. Operating in parallel but opposite directions to provide bidirectional data buffering that would normally require multiple independent devices.

Its 36-bit word width is an industry first. And ideal for interfacing with new generation higher-speed 32/36-bit and 64/72-bit microprocessors and buses. Moreover, a choice of 9, 18, or 36-bit word widths on Port B means efficient word width matching.

Programmable Almost Empty and Almost Full status flags on each port—in addition to Full, Half Full and Empty flags—allow you to either leave the flags set at their initialized setting of 8, or program them over the entire FIFO depth.

The LH5420 comes in a 132-pin plastic QFP package. It is available with access times of 15 ns, 20 ns and 25 ns, and cycle times of 25 ns, 30 ns and 35 ns, respectively.

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Sharp Electronics Corporation

For more information call: 1-201-529-8757 FAX: 1-201-512-2020.

CIRCLE NO. 139

firmly to the heat-sink mounting surface. The retaining force is applied at four locations to ensure uniform mounting pressure. The heat sink employs a parallel set of fins to maximize thermal performance and minimize board-space and volume requirements. The units are available with or without solderable tinned tabs for either vertical or horizontal mounting. Heat sinks without tabs, \$0.24; heat sinks with tabs, \$0.33 (1000).

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400. FAX (603) 528-1478. TWX 510-298-1127.

Circle No. 389

Stacking Connectors

- *Come in 10- to 100-position sizes*
- *Are surface mountable*

The AMPMODU 50/50 connector system features polarized surface-mount headers and receptacles that have a 0.05×0.05-in. center-line contact spacing. Three different headers allow board-to-board stacking heights of 0.25, 0.32, or 0.39 in. Nonprotrusive metallic hold-downs allow you to mount the connectors on both sides of 0.062-in. pc boards. The connectors are available with 10 to 100 positions—in 10-position increments. Receptacles feature beryllium copper, redundant-beam contacts; the headers use 0.018-in.-diameter phosphor bronze posts. Both headers and receptacles are duplex plated to increase reliability on the mating end and to ease the soldering process on the tails. Built-in standoffs on both headers and receptacles ease board-cleaning operations. \$0.07 to \$0.09/mated line. Delivery, stock to 10 weeks ARO.

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752.

Circle No. 390

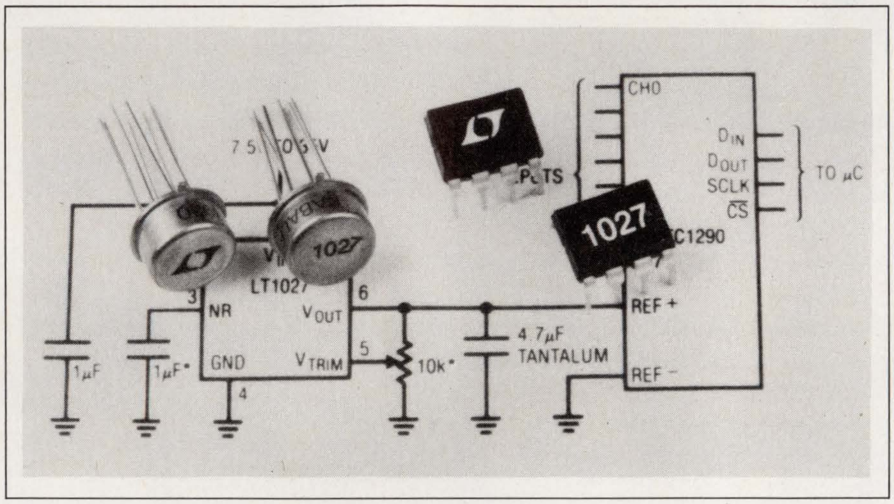
CIRCLE NO. 64

INTEGRATED CIRCUITS

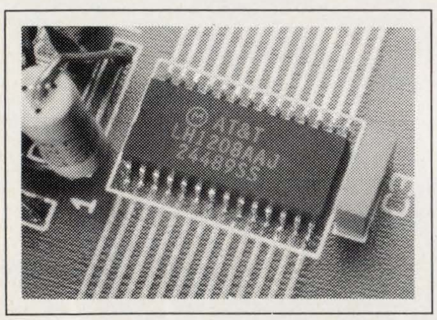
Precision 5V Reference

- *Less than 2-ppm/°C drift*
- *Needs no heated substrate*

Intended to reduce power requirements in 12- to 16-bit conversion applications, the LT1027 precision reference achieves high accuracy without need of a power-consuming heated substrate. Available in four grades of tolerance and drift, the highest grade LT1027A is pin compatible with the industry standard LT1021-5 and REF-02. Factory trimmed to an output voltage of 5.000V ±1 mV at 25°C, the A-grade device exhibits less than 2-ppm/°C drift. The lowest grade LT1027D has a ±5-mV output tolerance and 7.5-ppm/°C drift. The references settle within ±0.01% of final value in 2 μsec with no external load or when sourcing current. The output can sink or source currents as high as 10 mA. The low-noise references have a noise reduction pin for use with a low-leakage external capacitor; using the pin reduces wideband noise from 2 to 1.2 μV over the 10-Hz to 1-kHz range. The devices also have a trim pin for adjusting the output voltage over a ±30-mV range. All grades of the LT1027 are available in 8-pin, TO-39 metal cans. The B, C, and D grades also come in an 8-pin plastic DIP. $5.50 to $14.10 (100).



Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. FAX (408) 434-0507. **Circle No. 391**



PBX Switch-Set IC

- *Performs break and access functions*
- *Contains five high-voltage switches*

The LH1208 PBX switch-set IC replaces several PBX components. The device performs the break and access functions between the PBX line feed and the telephone loop. These functions cause the telephone to ring or the message-waiting lamp to light. The switch set's monolithic single-chip construction eliminates the problems normally associated with mechanical contacts. The chip's analog and digital circuitry includes five high-voltage switches, ring-trip/off-hook circuits, zero-crossing switching, and an auxiliary latch. The LH1208 comes in a 28-pin SO package and a plastic leaded chip carrier. $7.80 (100).

AT&T Microelectronics, Dept 52AL300240, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447; in Canada, (800) 553-2448. **Circle No. 392**

8-Bit Video DACs

- *Feature 40-MHz sampling*
- *Can drive a 75Ω cable*

Designed for high-speed conversion applications such as RGB graphics and high-resolution video, the MC10322 and MC10324 8-bit D/A converters can sample at rates as high as 40 MHz. Functionally identical, the MC10322 has TTL-compatible inputs, and the MC10324 has ECL-compatible inputs. The devices' input registers eliminate the need for external latches, unless the transparent mode is selected. Video controls (Force High, Blank, Bright, and Sync) permit an easy interface to standard video systems. The DACs have conversion (clock) inputs that can be either differential or single ended. The DACs also provide complementary outputs for use with custom displays or special effects. The devices come in 24-pin DIPs and cost $4.36 (250).

Motorola Inc, EL340, 2100 E Elliot Rd, Tempe, AZ 85284. Phone (602) 897-3615. **Circle No. 393**

Floating-Point Processors

- *Run at a 50-MHz clock rate*
- *Deliver 100M-flops performance*

Targeted at the workstation and massively parallel computer markets, the W4164 and W4364 floating-point processors can deliver a 100M-flops performance and run at

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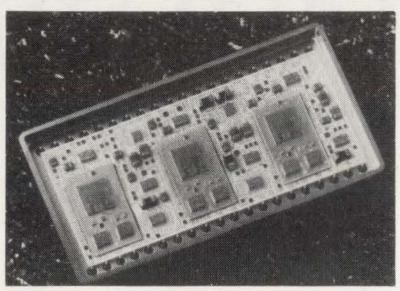
CIRCLE NO. 141

a clock rate of 50 MHz. The processors reduce board space by integrating several functions on a single chip, including a register file, a multiplier/divider unit, and an ALU. The register file eliminates the need for off-chip devices, and the independently controlled ALU and multiplier/divider unit enable the processors to perform two independent numeric operations simultaneously. The W4164 has an 8-port register file and a single 64-bit I/O port. The W4364 has a 9-port register file and three 64-bit I/O ports, which optimize the device for vector applications. The W4164 will be available in the second quarter of 1991, and the W4364 will be available in the fourth quarter of 1991. W4164, $575; W4364, $625 (1000).

Weitek Corp, 1060 Arques Ave, Sunnyvale, CA 94086. Phone (408) 738-8400. **Circle No. 394**



3-Channel, 16-Bit R/D Converter

- *Type-II servo-loop tracking*
- *Operates from a 5V supply*

The HRD1346 16-bit resolver-to-digital (R/D) converter contains three independent channels. Each channel is a Type-II tracking converter with zero velocity-lag error. The converter has an accuracy of 1.3 arc-minutes, which is maintained with signal-to-reference phase shifts to ±45°. Special anti-lock-up circuits ensure that the converter does not lock into an angle 180° from the true angle, when a step function of 180° is applied. A transparent latch, configured as two independently enabled 8-bit bytes, eases the transfer of data. The R/D converter, which is fully compatible with 8- and 16-bit microprocessors, operates from a single 5V supply and consumes 30 mA of current. HRD1346 in a 40-pin hybrid package, $1345. Delivery, 12 to 16 weeks ARO.

Natel Engineering Co Inc, 4550 Runway St, Simi Valley, CA 93063. Phone (805) 581-3950. FAX (805) 584-4357. **Circle No. 395**

Ethernet Transceiver

- *For use with 10Base-T LANs*
- *Low-power operation*

Designed for use with 10Base-T twisted-pair LAN media, the 92C03 Ethernet transceiver has all key analog and digital functions on chip and supports both embedded and external media-attachment-unit applications. The low-power device draws an idle current of less than 35 mA, compared with competitive types that draw as much as 350 mA. The chip also features a nonoperating mode that disables the internal clock and reduces current drain to <250 μA. This mode is useful for conserving power in laptop-computer and other power-sensitive applications. In addition to meeting the 10Base-T standard, the transceiver also supports pre-10Base-T designs by allowing for the disabling of the link test and the signal-quality-error test. The transceiver is available in 28-pin DIPs or plastic leaded chip carriers. DIP version, $9.75 (1000).

NCR Corp, 1700 S Patterson Blvd, Dayton, OH 45479. Phone (800) 334-5454; in OH, (513) 445-5000. **Circle No. 396**

Dual-Port Static RAMs

- *Have 25-nsec access times*
- *Organized as 1k×8 and 2k×8 bits*

Featuring access times of 25 nsec, an 8-member family of dual-port static RAMs (SRAMs) can work with processors running as fast as 40 MHz. Available in basic organizations of 1k×8 bits and 2k×8 bits, the CY7CXXX devices come in both master and slave configurations and in a choice of either 48- or 52-pin packages. Dual-port SRAMs that allow two processors to share a common memory provide two sets of address, data, and control signals; one for the "left" port and one for the "right" port. Usually, 8-bit applications require one master. You can use slave devices to expand word width. Because of pin limitations at the 2k×8-bit level, interrupt outputs are not available in the 48-pin DIP. In the 52-pin LCC and plastic leaded chip carriers, interrupt outputs are available from both master and slave devices. CY7C141 1k×8-bit slave, $32.20; CY7C136 2k×8-bit master, $47.20.

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600.

Circle No. 397

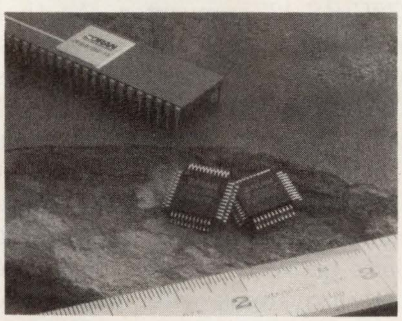


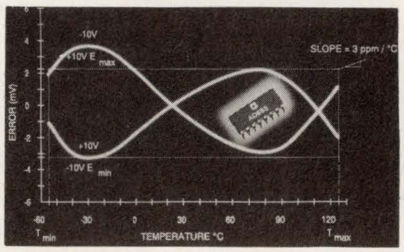
Image-Compression IC

- *Performs discrete cosine transforms*
- *Operates bidirectionally*

Designed for image-compression applications, the ZR36020 processor performs 2-D forward and inverse discrete cosine transforms (DCTs). By cascading the device with an image coder/decoder, the user can realize a JPEG-compliant image-compression system. Bidirectional operation facilitates dynamic compression and decompression switching. The processor performs an 8×8 DCT every 4.2 μsec (15-MHz data rate) and supports four different data formats. Power consumption is <625 mW, and a low-power standby mode reduces this figure to 10 mW. The DCT processor is available in a 44-pin quad flatpack or a 48-pin ceramic DIP. $79 (100).

Zoran, 1705 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 986-1314. FAX (408) 986-1240.

Circle No. 398



Precision ±10V Reference

- *Initial error is <2 mV*
- *Drift is <1.5-ppm/°C*

According to the company, the AD688 is the industry's first monolithic ±10V reference. The device features a maximum initial error of 2.0 mV, a maximum tracking error of 1.5 mV, and a maximum temperature drift of 1.5-ppm/°C. Designed for use in such applications as 12- to 16-bit data-acquisition systems, the reference offers 12-bit accuracy without any user adjustments. For greater levels of precision, you can use the gain and balance-adjust pins to calibrate the reference. In addition, Kelvin force- and sense-connections correct for the effects of voltage drops in circuit wires. Noise from the buffered voltage outputs is typically 0.6 μV pk-pk with a spectral density of 140 nV/$\sqrt{\text{Hz}}$. The AD688, in a 16-pin ceramic DIP, comes in three accuracy and temperature grades. From $12.75 (100).

Analog Devices, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. **Circle No. 399**

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

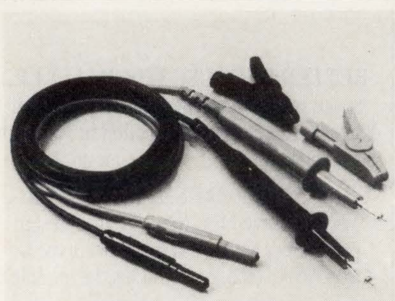
Digital Logic-Analyzer Probe

- *Includes bus simulation and logic analysis*
- *Accepts pods for specific 8-, 16-, and 32-bit µPs*

When equipped with appropriate pods and probes, the Model 5100 instrument performs bus simulation through 152 programmable I/O lines; operates as a 9-channel, 100-MHz logic timing analyzer; and aids in troubleshooting specific 8-, 16-, and 32-bit µPs. Among the processors supported are the 68020 and the i386. Among the buses supported are the VMEbus, Multibus, IBM PC/AT bus, and SCSI bus. In addition to logic analysis, the logic-analyzer probe supports signature analysis and measures frequency and other analog quantities. Unit equipped with logic analyzer probe, 152 I/O lines, and 32-bit µP pod, $21,195.

Talon Instruments, 150 E Arrow Hwy, San Dimas, CA 91773. Phone (714) 599-0690. FAX (714) 599-6529.

Circle No. 372



Multimeter Test Leads

- *Let you plug alligator clips onto banana-plug tips*
- *Accommodate many types of accessory tips*

The TL1000 silicone-rubber multimeter lead set includes right-angle or straight-shielded banana plugs and fully insulated alligator clips, with hard-plastic insulators. You can adapt the lead set to particular uses by pushing accessories onto banana plugs at the lead ends farthest from the meter. Such accessories include push-on hooks and spade lugs. Other accessories include adapters for meters with recessed male inputs and extended sleeves to link cables for greater length. You can use the 1.2m lead set for measuring voltages as high as 1 kV and currents as high as 10A. The straight plugs have spring-loaded, retractable safety sleeves; the right-angle plugs have fixed rubber sleeves. $14.

Test Probes Inc, 9178 Brown Deer Rd, San Diego, CA 92121. Phone (800) 368-5719.

Circle No. 373

Data-Acquisition Units For Next Workstations

- *For analog and digital I/O*
- *Driver software links to Objective-C*

The ADC488/16 16-bit A/D converter has 16 single-ended or 8 differential inputs and 100k-sample/sec throughput. The ADC488/8S ADC has eight differential inputs, each with its own S/H amplifier. The DAC is available with two or four channels. All DAC outputs are ohmically isolated from each other and from chassis ground. The Digital/488 is an 80-bit digital I/O interface. The Serial488/4 is a 4-channel bidirectional IEEE-488 to RS-232C/RS-422 converter. As their model numbers imply, all of these units connect to the IEEE-488 bus. The SCSI488/N interfaces the SCSI port of a Next workstation to the IEEE-488 bus. Driver488/N is software that lets you control the aforementioned units from the workstation's native Objective-C language. I/O subsystems with drivers and several modules, $2990 to $5780.

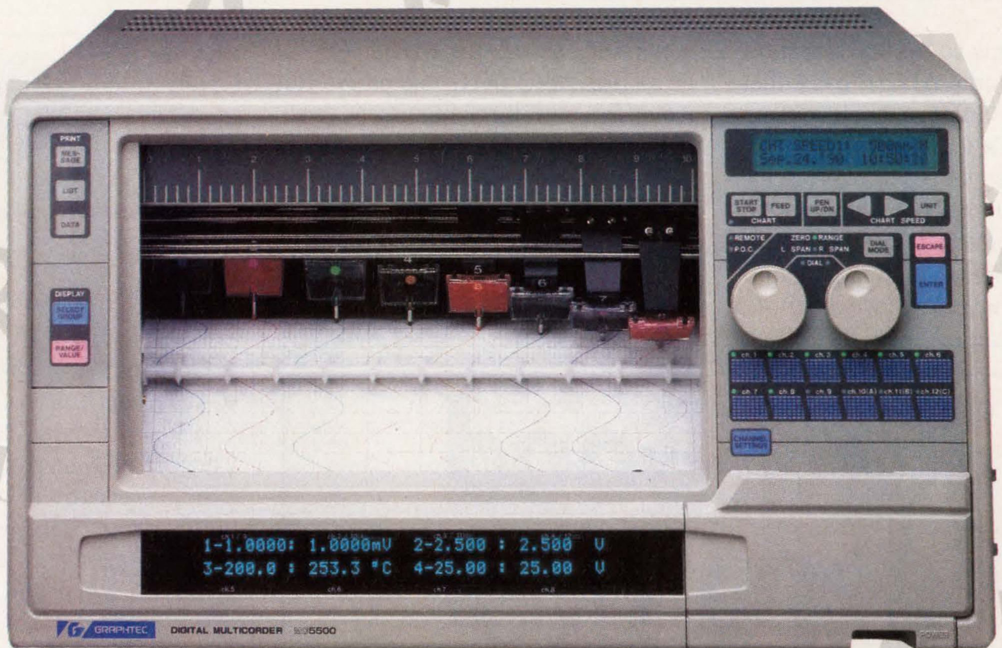
IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093.

Circle No. 374

Workstation-Based Test-Development Software

- *Lets you develop test programs by connecting icons*
- *You can define your own icons via C-language routines*

Real-time Integrator is software for the vendor's Unix and RISC-based workstations; it allows you to de-



THE WORLD'S SMARTEST 12-CHANNEL PEN RECORDER

More intelligent functions, and more channels—two key points that make the new Graphtec MC5500 Digital Multicorder a truly powerful package.

MORE INTELLIGENT FUNCTIONS—A smart machine means better efficiency. The MC5500 has a bright digital display that shows measured values and span, a 32 Kword memory card as standard equipment (256 Kword optional), and 5 different printed logging and report modes. You also get Auto Bias recording, Partial Enlargement/Reduction, Zone recording, remotely adjustable chart speed and a GPIB interface for control by the host computer.

MORE CHANNELS—If you need to record more than 8 channels of data, the choice is simple. You can either double up on hardware, bulk, and complexity, or simply buy the compact 12-channel version of the MC5500.

For more information on this truly SMART pen recorder, call, write or fax us today.

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(800) 624-8396 inside CA (800) 854-8385 outside CA
FAX: (714) 855-0895

CIRCLE NO. 142

velop programs to control and monitor test instruments and to reduce, display, and analyze their output. The package's icon-based graphical interface lets you create programs by interconnecting icons on the screen; no traditional programming is needed. The package supports instruments that interface with the workstations via an IEEE-488 bus or an RS-232C port. You can define icons for new instruments by writing routines in C. Development kit, $2700; runtime license, $600.

Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Phone (800) 344-4825; in MA, (508) 493-5111. **Circle No. 375**

IEEE-488-Controlled Power Supplies

- *Occupy 5¼ in. in EIA racks*
- *8V version produces noise of 7 mV p-p in a 20-MHz bandwidth*

The HP 6671A and 6674A power supplies occupy 5¼ in. of mounting height in a 19-in.-wide EIA equipment rack. The IEEE-488-programmable 8V and 60V units produce 1.96 and 2.1 kW of output power, respectively. The 8V unit produces 7 mV p-p in a 20-MHz bandwidth. A 5-pole common-mode current filter helps to lower the normal-mode noise, and the 8V unit offers common-mode noise of 5 mA p-p. The vendor claims that this current is from 1 to 10% of that produced by other switching supplies. The units respond to the SCPI syntax. HP 6671A 8V unit, $4450; HP 6674A 60V unit, $4300.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 376**

AC-Power-Quality Analyzer

- *Features DSO, rms voltmeter, and clamp-on ammeter*
- *Monitors harmonic distortion and power disturbances*

The Model 658 Power-Quality Analyzer electrical troubleshooting tool incorporates features of a digital storage oscilloscope, a true-rms clamp-on ammeter, a true-rms voltmeter, a harmonic-distortion analyzer, and a power-disturbance monitor. The 24-lb, 4-channel unit includes a 5-in. flat-panel display, a 3½-in. floppy-disk drive, and a graphics printer. You can view any voltage or current waveform and also see its peak and rms values up-

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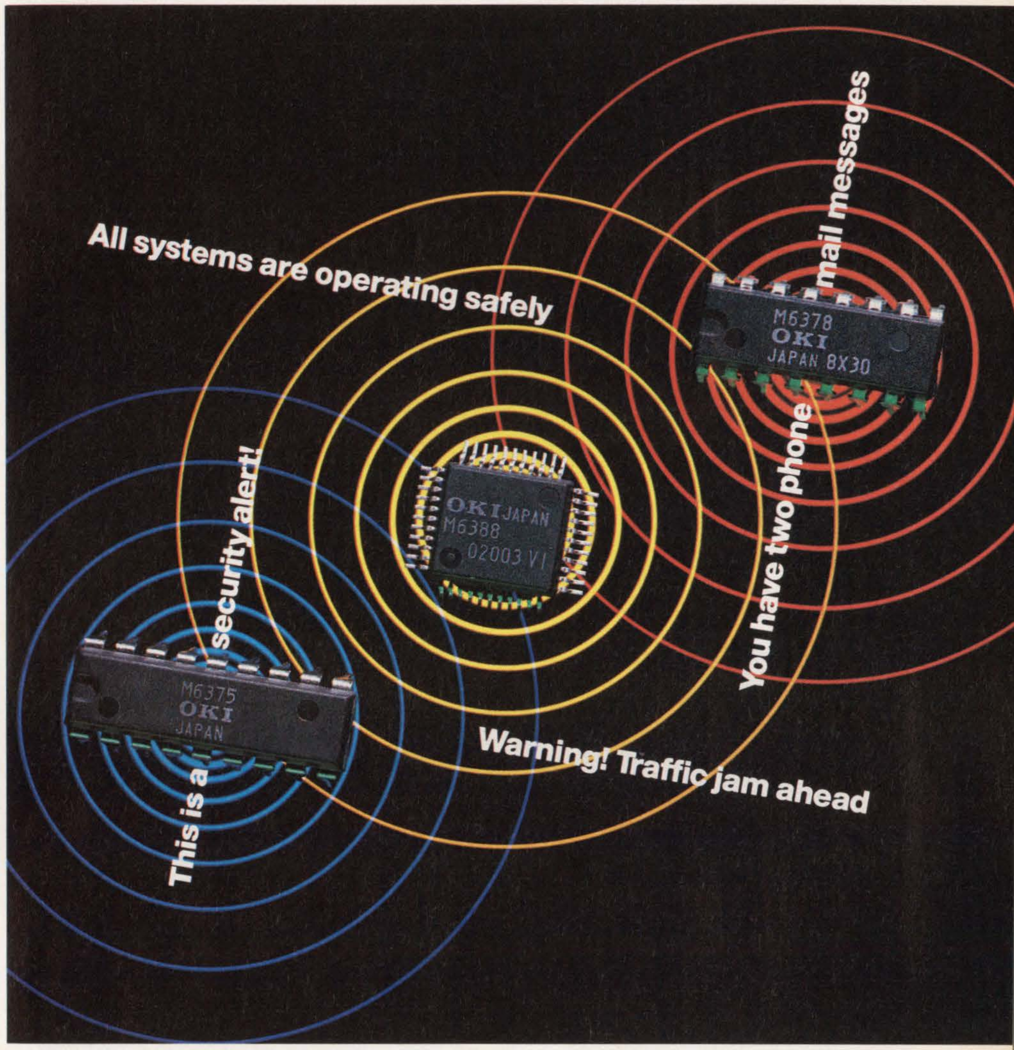

Oki's RealVoice™ Speech Synthesis Family

Part #	Description
MSM6295	4-channel speech synthesizer
MSM6322	Pitch control IC
MSM6372	Speech synthesizer with 128K ROM, 5 secs
MSM6373	Speech synthesizer with 256K ROM, 10 secs
MSM6374	Speech synthesizer with 512K ROM, 20 secs
MSM6375	Speech synthesizer with 1M ROM, 40 secs
MSM6376	Evaluation chip for MSM6372/73/74/75
MSM6378	Speech synthesizer with 256K OTP ROM
MSM6388	Solid-state recorder/1M serial register I/F

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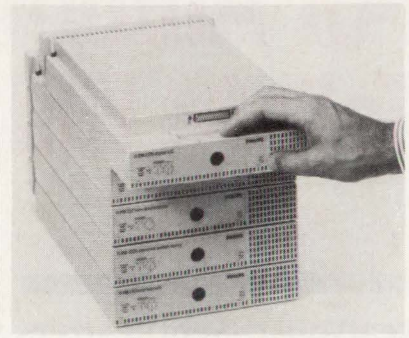
dated continuously in numeric form. You can also zoom in on waveform details. A monitor mode stores digitized records of disturbances in nonvolatile memory for later analysis. Approximately $13,000.

Dranetz Technologies Inc, Box 4019, Edison, NJ 08818. Phone (201) 287-3680. **Circle No. 377**

Switching Modules For Analog And Digital Signals

- *Accommodate low-level and high-frequency signals*
- *High-speed unit has 32k-word memory*

The System 23 family of modules plug together to form switching subsystems that route analog and



digital signals to and from test instruments. Each switching subsystem must include a master module that provides an interface to the IEEE-488 bus and can furnish power to 15 modules. The family has modules of seven types, including matrix switches, high-frequency switches, and switches with low thermal offsets. A 32-channel digital I/O module has a 32k-word buffer and can handle I/O operations at 2 MHz. Programming conforms to the SCPI syntax. Modules, $850 to $1650.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (800) 443-5853; in WA, (206) 347-6100. **Circle No. 378**

Philips Test and Measurement, Bldg TQIII-4, 5600 MD, Eindhoven, The Netherlands. Phone local office. **Circle No. 379**

2-MHz Sweep/Function Generator

- *Produces sine, square, triangular, and TTL waveforms*
- *Lets you vary sweep width to 100:1*

The FG-2000 2-MHz sweep/function generator produces five waveforms—sine, square, and triangular waves; ramps; and a TTL-compatible pulse train. The generator can operate as a frequency-modulated source or as a voltage-controlled generator using its internally synthesized ramp as the modulating source. The output is 10V p-p into 50Ω or 20V p-p into an open circuit. A switchable ×20 attenuator, vari-

CIRCLE NO. 125

able dc offset, and adjustable symmetry enhance the unit's flexibility. $349.

Ztest Electronics Inc, 290 Larkin St, Buffalo, NY 14220. Phone (416) 238-3543. FAX (416) 238-1377. **Circle No. 380**

VMEbus Data-Acquisition Module

- *Includes 12-bit 1-μsec or 14-bit 2-μsec ADC*
- *Has four input channels and plug-in ADC section*

The DVME-614 VMEbus data-acquisition module accepts very fast, accurate plug-in ADCs. The 4-channel unit accommodates a 12-bit ADC that makes a conversion in 1 μsec or a 14-bit ADC that converts in 2 μsec. The board contains a 4096-word FIFO buffer that permits nonstop acquisition during transfers of data blocks to the CPU's memory. In addition to transfers via the VMEbus, the board can send data from the buffer through its parallel port at 4M bps. You can trigger the ADC with analog or digital signals. The board includes counter/timers to divide a trigger signal's frequency. It also contains a comparator and threshold DAC for analog triggering. 12-bit, 1k-word buffer, $2395; 14-bit model, $2590.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. **Circle No. 381**

200k-Sample/Sec, 16-Channel ADC Board

- *Simultaneously samples all channels*
- *Includes four DACs and 24 digital I/O lines*

The PC-30DS data-acquisition boards plug into the IBM PC/AT bus. They include a 12-bit ADC that can take 200k samples/sec. The ADC is preceded by one to four multiplexed S/H circuits, each having four channels. These circuits can simultaneously sample all of the analog inputs. Also on the board are 24 digital I/O channels, two 12-bit DACs, and two 8-bit DACs. The board includes channel-list hardware that lets you scan channels in customized sequences. Once you've specified a scan, you can start it with a terse command. A block-scan mode and dual-channel DMA let you store long, gap-free data sequences in the computer's memory. The vendor supplies high-level-language drivers with source code. PD-30DS 16-channel unit, $1495; PD-30DS/4 4-channel unit, $1295.

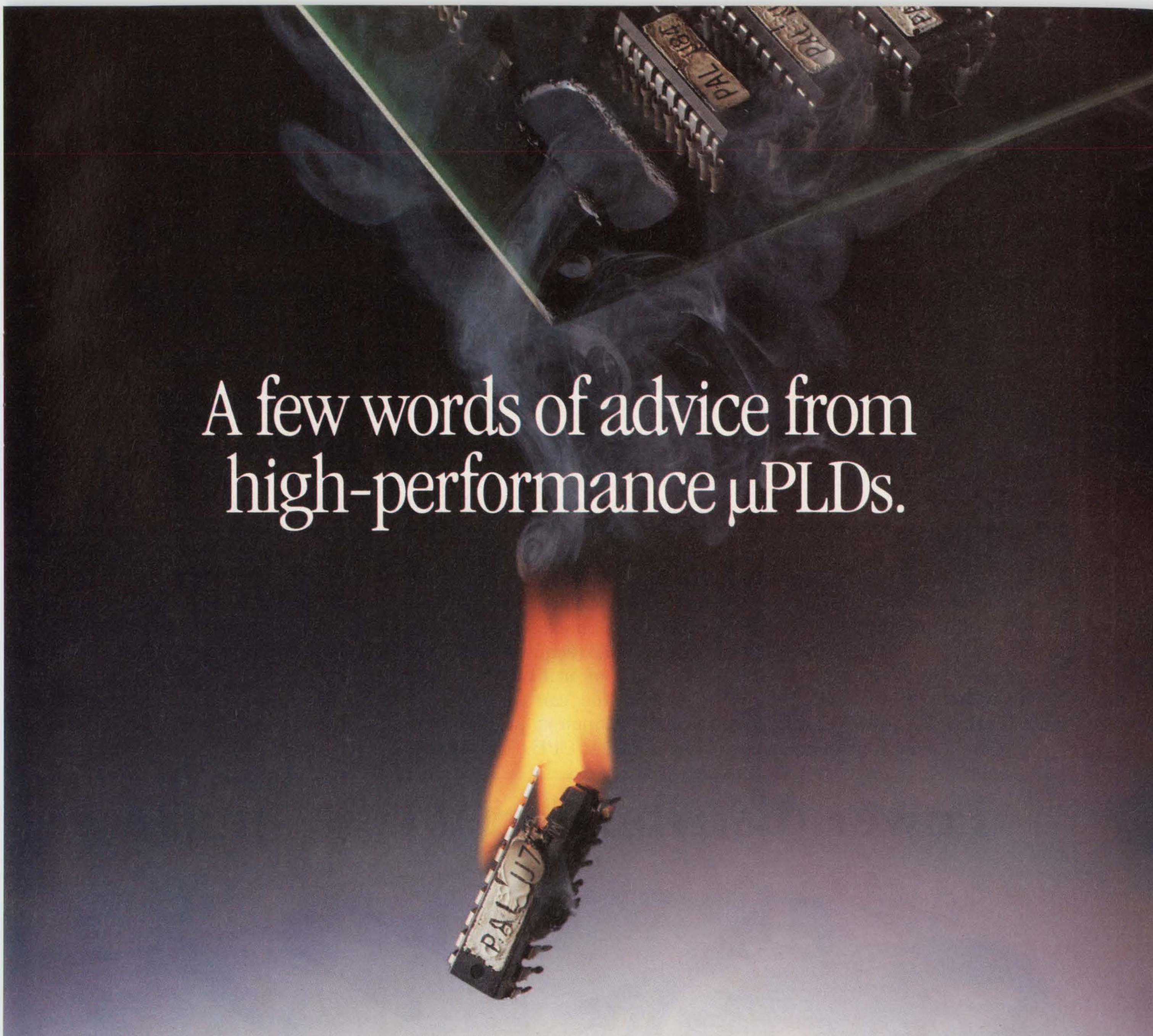
United Electronic Industries, 10 Dexter Ave, Watertown, MA 02172. Phone (617) 924-1155. FAX (617) 924-1441. **Circle No. 382**

CAE & SOFTWARE DEVELOPMENT TOOLS

PC-Hosted Cross-Development Tools for OS-9

- *Allow you to develop and debug applications in C on a PC*
- *Let you download your programs to 680X0-based system for OS-9*

PCBridge lets you develop and debug real-time applications in C on an IBM PC or compatible. You can cross-compile the programs, download them via a serial link to a remote 680X0-based system that runs the OS-9 operating system, and link your application modules to existing libraries and drivers. PCBridge comes with a C cross-compiler, an assembler, a linker, a state debugger, an OS-9 memory-module loader, and other development aids. If you're designing the entire OS-9 target system, you can use the



Chill out, PAL.

Many designers have hot, high-performance designs. Literally.

Fortunately, Intel has a simple way to reduce system heat and still get incredible performance. The μPLD Family of programmable logic devices.

Take, for example, the 85C220 and 85C224. They operate at 80MHz (100 MHz internally) with only a 10ns total propagation delay.

And since μPLDs are manufactured using Intel's CHMOS* technology, they require just 1/4 the power of their pin-compatible bipolar PAL* alternatives. Which means they can lower system heat by 35 percent and help reduce board-level failures, too. So they're certain to give your high-performance system a boost. And send chills up the spine of your motherboard.

Learn more about Intel μPLDs and receive a μPLD/PAL heat comparison. Call (800) 548-4725 and ask for Literature Packet #IA28.

Otherwise, you could take some heat over your system design.

intel®

CIRCLE NO. 146

Portpak tool set, which includes sample source code for I/O device descriptors and device drivers, as well as for boot ROMs. Portpak's Make utility helps you keep track of the proper versions of each module. $1400.

Microware Systems Corp, 1900 NW 114th St, Des Moines, IA 50325. Phone (515) 224-1929. FAX (515) 224-1352. **Circle No. 351**

Software Development System

- *Target CPU may be any 8- or 16-bit μP from Intel or Motorola*
- *Host system may be IBM PC/AT or compatible*

Ez-pro development systems consist of an IBM PC/AT or compatible for software development, C cross-compilers and cross-assemblers for most Intel and Motorola 8- and 16-bit μPs and microcontrollers, and an in-circuit emulator (ICE) configured for the target CPU. The C cross-compilers conform to the draft ANSI standard and will be revised to comply with the final standard. The C cross-compilers produce assembly-language for the target CPU, and a cross-assembler and linker generate the executable code for downloading to the ICE via a 56k-bps serial link. The Emulation Executive is a source-level debugger that runs on the host computer and controls execution of the program under test by means of the ICE. A deep-trace hardware option allows you to capture all address-bus and data-bus information during execution and to set hardware breakpoints on external probe data or on complex sequences of events. A variety of utility programs is available. You can also rent complete development stations for a specific target CPU. Emulator, depending on the target CPU, from $1995; cross-assemblers with linker, $595; C cross-compilers (with cross-assembler and linker), $895.

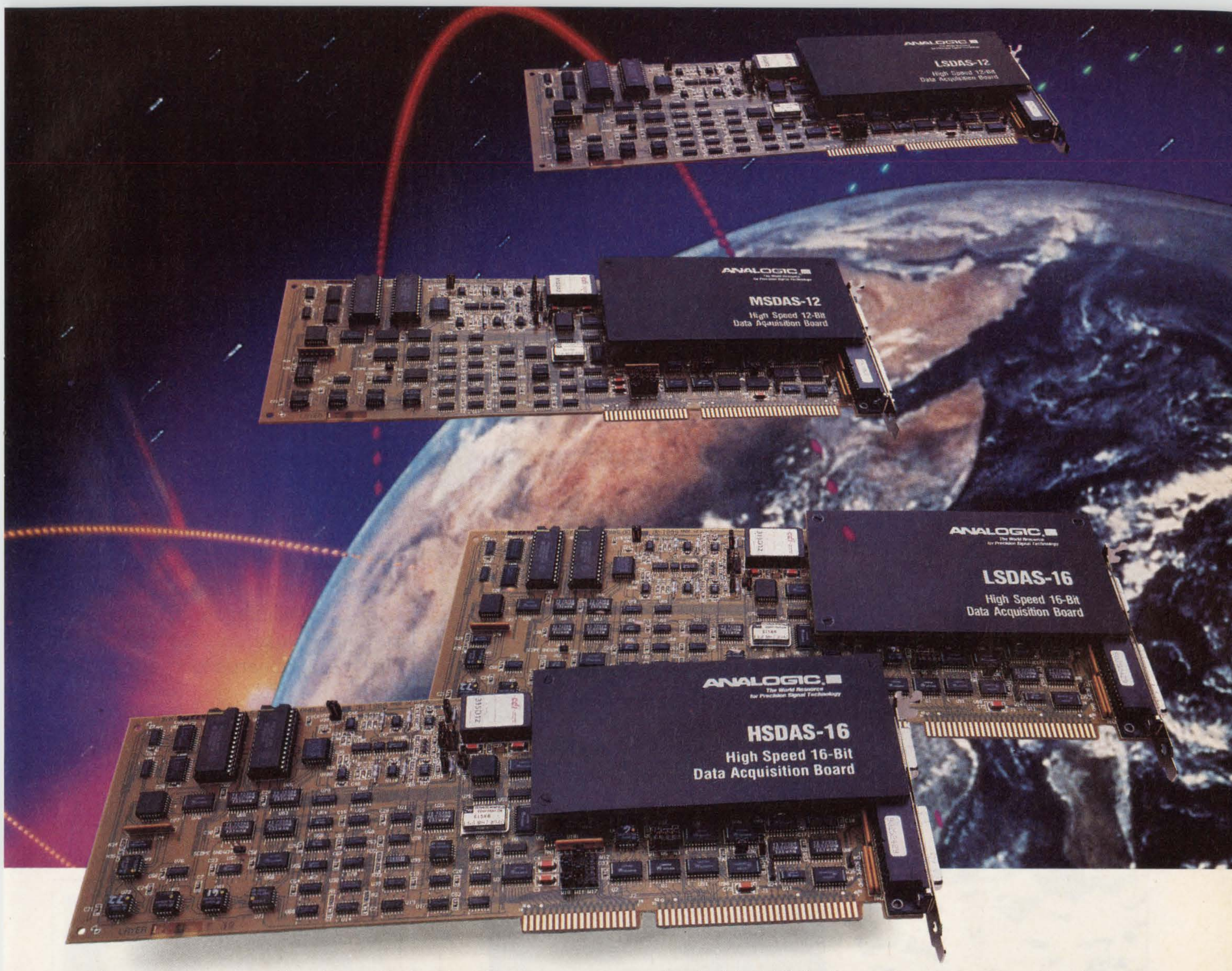
American Automation, 2651 Dow Ave, Tustin, CA 92680. Phone (714) 731-1661. FAX (714) 731-6344. **Circle No. 352**

Neural-Network Development Tool

- *Explains how the neural network arrived at a decision*
- *Interprets back-propagation networks*

Neuralworks Professional II/Plus is a design tool that allows you to develop neural networks for a variety of host computers. To facilitate development of embedded systems, the Flashcode feature can interpret back-propagation networks and their variations created by Neuralworks; and, from them it generates

 CIRCLE NO. 71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MSDAS-12
High Speed 12-Bit
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ANALOGIC
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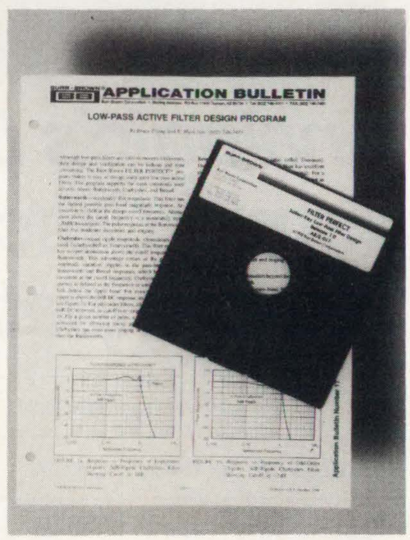
Data Acquisition Board

C source code. After compiling this source code, you can embed the resulting stand-alone program into application programs or DSP boards. The Explainnet feature lets the network explain how it arrived at a particular decision and which input has the greatest effect. The program also allows you to create neural networks for embedding into Digital Neural Network Architecture ICs from Neural Semiconductor (San Diego, CA). Other enhancements to this version of Neuralworks include a back-propagation builder that lets you create more than 8000 variations of back-propagation networks from a single menu; 40 new commands that help you to create special configurations; and seven new network types. The new types are Kohonen self-organizing map, learning vector quantization I and II, extended learning vector quantization, delta bar delta, extended delta bar delta, and directed random search, all of which can improve the performance of certain types of applications. Neuralworks Professional II/plus, for IBM PC/ATs under DOS or OS/2, and Macintosh SE and II computers running MAC OS, $1895; for Sun workstations running Unix and for the Meiko and Alacron Transputer boards, $3995; for the IBM RS-6000 running Unix, and for i860-based coprocessor boards from Myriad Solutions, $4995.

Neuralware Inc, Penn Center W, Bldg IV, Suite 227, Pittsburgh, PA 15276. Phone (412) 787-8222. FAX (412) 787-8220.

Circle No. 353



Design Tool For Active Lowpass Filters

- *Selects standard capacitor values*
- *Specifies exact resistor values or nearest 1% value*

Filter Perfect is a free software package that runs on IBM PCs and compatibles and helps you design active lowpass filters. The menu-

C&C Computers and Communications

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NEC Supercaps offer out-of-this-world performance.

Creating large capacitance in small cases has been an NEC specialty for decades. The three new Supercaps in our FM series are an extraordinary example.

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Supercaps are the ideal replacement for backup batteries. They feature fast charging, semipermanent life and excellent safety factors.

Supercaps come in eight series. They cover a wide range of backup needs from CMOS RAMs and microcomputers to large-current applications. For more information, contact NEC today.

Series	Application	Capacitance (F)	Feature
FYD	RAM/microcomputer backup	0.022 – 2.2	Space saving
FYH		0.022 – 1.0	Low profile
FYL		0.01 – 0.047	Extra low profile
FM		0.022 – 0.1	Auto insertion/soldering
FR		0.022 – 1.0	Wide operating temperature (–40°C to +85°C)
FS	Medium backup current	0.022 – 1.0	
FA	Large backup current	0.047 – 1.0	5.5V
		0.022 – 0.47	11.0V
FE		0.047 – 1.5	Low ESR

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NEC

CIRCLE NO. 148

driven program lets you select Butterworth, Chebyshev, and Bessel filters, guides you in choosing the number of poles, and calculates capacitor and resistor values. Even-ordered filters consist of cascaded sections of Sallen-Key complex pole-pairs. The program selects standard capacitor values and then calculates exact resistor values for the filter you have selected. If you select the 1% option, the program selects the closest 1% value for one resistor in each pole-pair; then it recalculates the exact value for the second resistor (using the 1% value for the first resistor as an exact value) before selecting the closest 1% value for the second resistor. This procedure produces the most accurate design you can implement with 1% resistors. The 5¼-in. disk comes with an application note (AB-017) that describes how the program works, gives further guidance on the design of lowpass filters, and shows the measured results of some actual filters designed with the aid of the program. You can obtain the package at no charge from your nearest Burr-Brown sales office.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510.

Circle No. 354

Simulator Predicts Transmission-Line Behavior

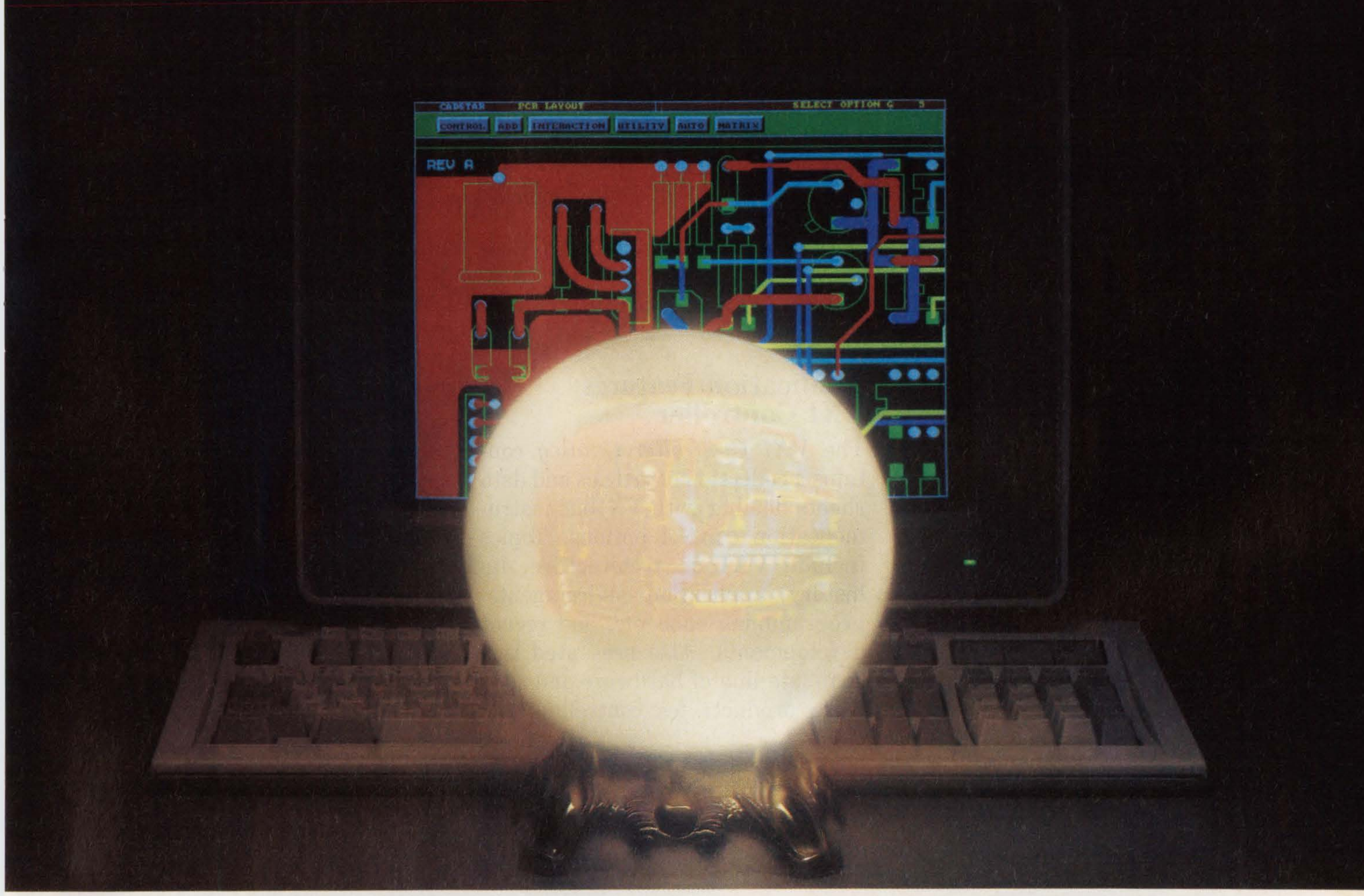
- *Lets you design critical traces before layout begins*
- *Handles buried microstrip and asymmetric stripline*

Linesim is a program that runs on an IBM PC/AT or compatible and predicts the transmission-line behavior of critical traces before layout begins. You specify the circuit elements (drivers, receivers, transmission lines, resistors, and capacitors) by clicking on library models with a mouse; the simulation appears in the form of an oscilloscope display. The program is completely interactive; to resimulate after a parameter change, you merely modify the schematic and replot. Thus, you can quickly determine the proper strategies and component values for line terminations. The program comes with an extensive model library that includes devices in the 74FCT, 74BCT, 74AC, 74HC, 74F, 74AS, 74ALS, and 74LS logic families, as well as programmable logic devices. $595.

Hyperlynx, Box 3578, Redmond, WA 98073. Phone (206) 869-2320. FAX (206) 881-1008.

Circle No. 355

Introducing The New CADSTAR...



IT ALMOST READS YOUR MIND.

CADSTAR's revolutionary new user interface almost reads your mind, anticipating your next move and intelligently defaulting to the most likely action. For example, if you pick a part, CADSTAR lets you move it without selecting an action from a menu. If you pick a connection, you can manually route it instantly.

CADSTAR's new Motif style graphical interface has clear, logical menus integrated across all functions. The best part is, you'll rarely need to use those menus! Imagine software so smart, it knows what you want to do next. CADSTAR is easy to learn, and it drastically reduces keystrokes, saving you hours.

The Power Remains

CADSTAR remains the most powerful design software you can run on a PC. Unique features like comprehensive, automatic/interactive routines for placement, gate and pin swapping, and routing give you remarkable design flexibility. Racal-Redac continues to enhance the design technology used by thousands of engineers worldwide. CADSTAR includes:

- Integrated Schematic Capture, PCB Layout, Autorouting, Manufacturing Outputs
- 5,000 part library
- Double sided SMDs
- Curved tracks & copper, teardrop pads
- Copper maximization
- Blind & buried vias
- Toll Free hotline support

CADSTAR works with Racal-Redac's 386 Advanced Router, the most powerful PC based router available. It features 32 bit, gridless, shove aside, rip up and retry technology for 100% routing completion.

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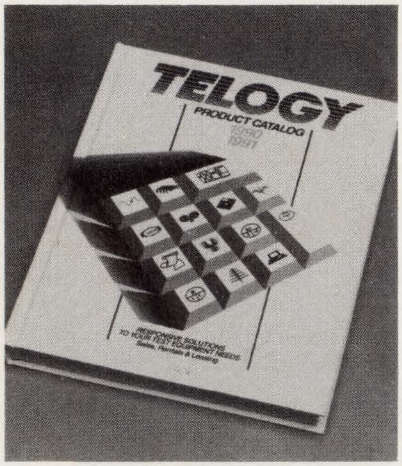


Guide Provides Listing Of Test Equipment

This 300-pg catalog is actually a reference guide, describing 3000 electronic test instruments, which are available for rental, lease, or purchase. You can easily find the 24 product categories; they are marked with individual icons. A helpful feature is the book's index arranged by product type, manufacturer name, and model number. An additional equipment-substitution index suggests alternative product selections. The publication provides photographs of the most popular instruments.

Telogy, 150 Shoreline Dr, Redwood City, CA 94065.

Circle No. 356

Publication Features VXI Controller

The *VXI Controller Catalog* contains a collection of articles and data sheets dealing with VXIbus instrumentation control options. Topics include VXIbus architecture, its history, application environments, programming concepts, and recent developments. Also presented is a complete line of hardware and software products for controlling the VXIbus systems, such as an external IEEE-488 controller, an external computer with an MXIbus interface, or an embedded PC controller.

National Instruments, 6504 Bridge Point Pkwy, Austin, TX 78730. **Circle No. 357**

Booklet Features Switching Power Supplies

This 4-color catalog describes a full line of switching power supplies. The 20-pg publication includes switching mode regulators, dc/dc converters, off-line switch power supplies, and electronic load devices with ratings of 1 to 720W output. Also discussed are selection tables, device descriptions, features and benefits, block diagrams, and specification charts.

Melcher Inc, 200 Butterfield Dr, Ashland, MA 01721.

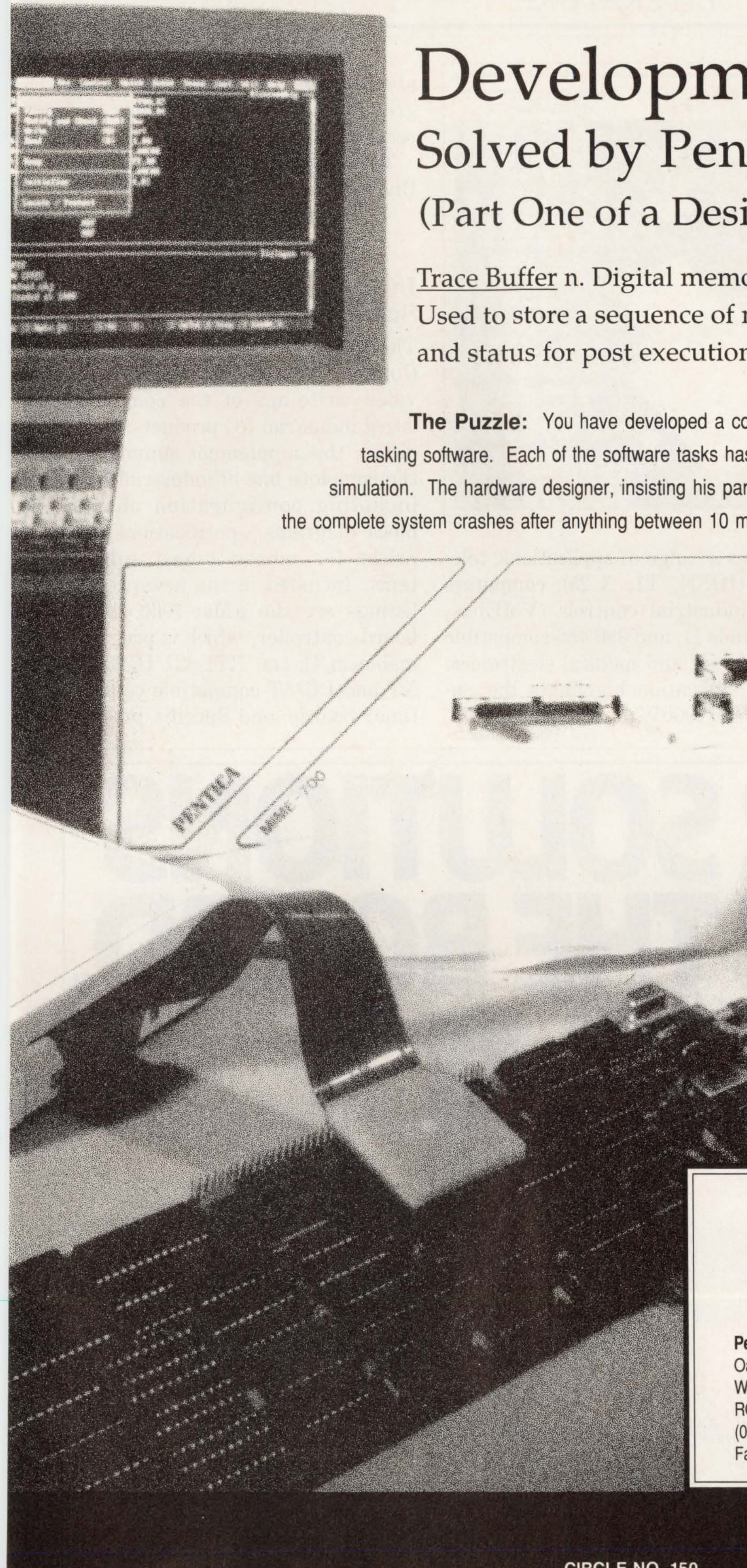
Circle No. 358

Development Puzzles

Solved by Pentica

(Part One of a Design Dictionary)

Trace Buffer n. Digital memory part of in-circuit emulator. Used to store a sequence of microprocessor addresses, data and status for post execution analysis.



The Puzzle: You have developed a complex real time system with interrupt driven multi-tasking software. Each of the software tasks has been debugged. No problems show up under simulation. The hardware designer, insisting his part works great, has gone on vacation. However, the complete system crashes after anything between 10 minutes and 3 hours.

The Solution: Use an ICE with a trace buffer large enough to capture the events which lead to the crash. Complex and sequential triggering of the trace may be required to stop tracing events which occur after the crash--an 8k word trace buffer could overflow in under 2ms. Pre-filtering of trace cycles can be used to extend the capture time. The ability to re-trigger the trace allows critical areas to be traced and then disregarded if the crash does not happen. Comprehensive search facilities are needed to analyse large amounts of data.

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CIRCLE NO. 150

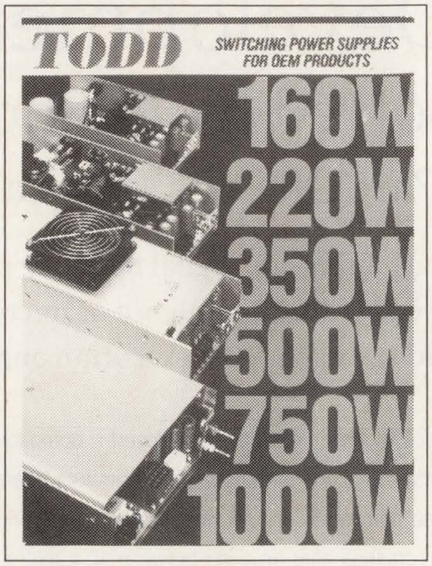
Measuring-Equipment Catalog

This 572-pg catalog details automatic test equipment/process controllers, signal generators, radio test sets, spectrum and network analyzers, and logic test equipment/recorders. The publication is divided into 13 sections. A choice of peripheral measurement devices appears in the appendix.

Rohde & Schwarz, 8000 Munchen 80, Muhldorfstr 15, Germany. **Circle No. 359**

Booklet Features Switching Power Supplies

The 1991 switching power-supply catalog discusses more than 100 standard switching power supplies. The publication also notes that the vendor produces modified, repackaged, and custom switching power supplies. The 32-pg booklet de-



scribes a range of applications: telecom (IDSN, T1, X.25); computers and industrial controls (VMEbus, Multibus II, and 386/486-compatible machines); and medical electronics. The publication highlights the Supermax 1000W series power supplies, a switcher designed from the ground up with power-factor correction.

Todd Products Corp, 50 Emjay Blvd, Brentwood, NY 11717.

Circle No. 360

I/O Products Catalog Supplement

The *1990 Data Acquisition and Control Catalog Supplement* provides write-ups of the company's latest industrial I/O products. In addition, the supplement summarizes the complete line of industrial I/Os, including configuration charts, block diagrams, specifications, and prices for sensor-to-host subsystems. Included in the new-product listings are the μMac-1060 single-board controller, which is programmable in C; the RTI-827 IBM PC/XT and PC/AT-compatible counter/timer boards; and Specifix process-

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Z84C90		✓				✓			✓		✓	✓
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Z80280	✓	✓	✓	✓	✓		✓			✓		
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control software and DOS drivers. A 9-section selection and configuration guide helps you determine the optimal configuration for specific applications. Product sections cover computer plug-in I/O boards; distributed I/O subsystems; modular signal conditions; analog signal-conditioning panels; digital subsystems, and software. Following these product sections are the product reference, listing each product's description and price, and an index, directing you to more detailed information in the main catalog.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. **Circle No. 361**

Comprehensive Listing Of STD Buses

The 480-pg STD Bus Technical Databook describes STD Bus and CMOS STD Bus products. The 10 tabbed sections make it easy to find the product you are looking for. The publication highlights the full STD Bus 8-bit and 16-bit Specification and STD Bus Practice and discusses more than 200 STD Bus devices for embedded and DOS-compatible systems. You will find technical specifications, photographs, and dimensional drawings for the full line of non-DOS single-board computers. Other products include 8088, 80286, and 80386 CPUs; memory; Ethernet and Arcnet networks; industrial I/O devices; card cages with power supplies; video controllers; and software for use in harsh industrial environments. The book features a section on the vendor's STD-AT, a true 80286 and 80386SX-based industrial computer that's compatible with the IBM PC/AT and PC/XT. An STD Bus Product Second Source/Cross Reference of more than 100 of the vendor's cards is included for such STD Bus manufacturers as Analog Devices, Prolog, Datricon, Data Translation, and Mostek.

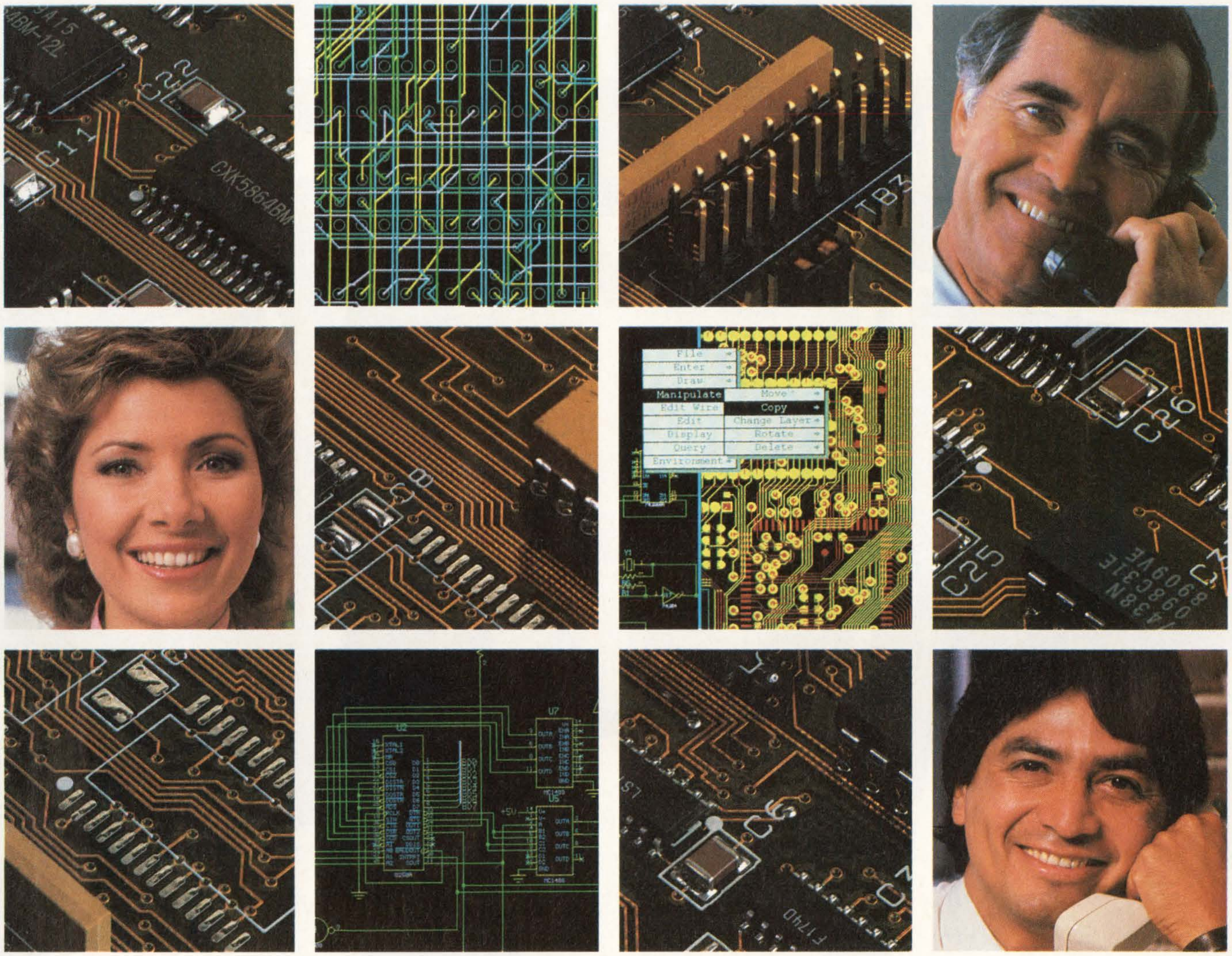
WinSystems Inc, Box 121361, Arlington, TX 76012.

Circle No. 362

App Note Explains Emulation System

This application brief examines the vendor's installation and utilization of the RPM Emulation System; its title is *Rockwell NTSD: ASIC Design Productivity Improvements.* The focus is on ASIC hardware emulation. "Sneakernet," an excerpted version of this study, is also available.

Quickturn Systems Inc, 325 E Middlefield Rd, Mountain View, CA 94043. **Circle No. 363**



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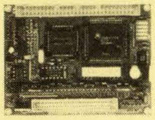

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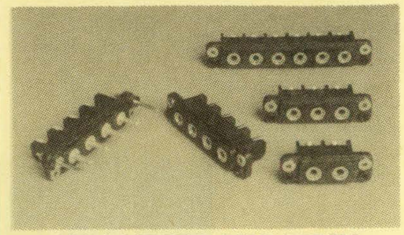

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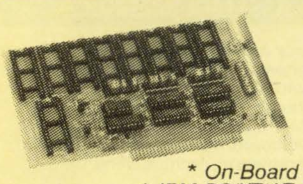

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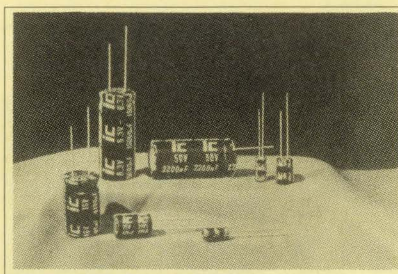

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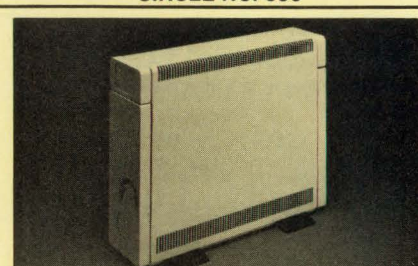

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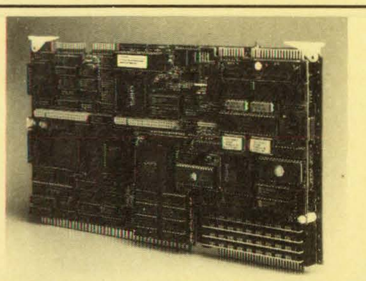

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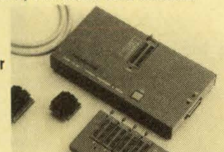

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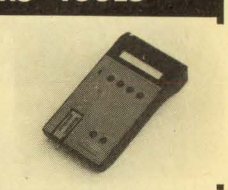

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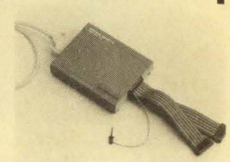

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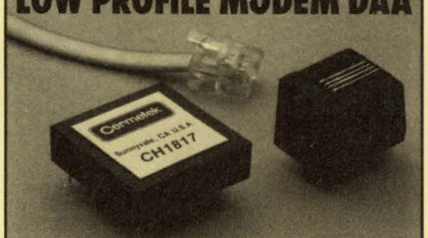

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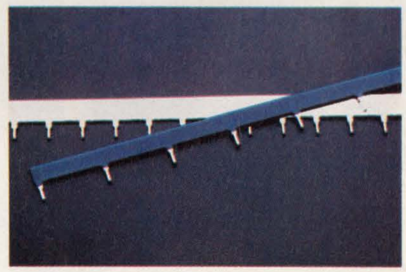

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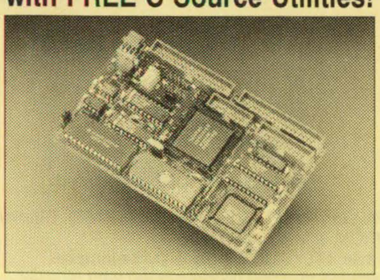

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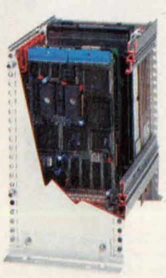

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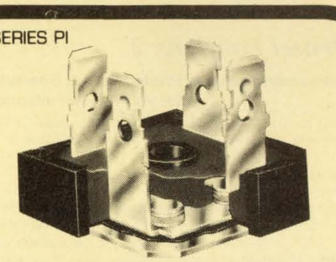

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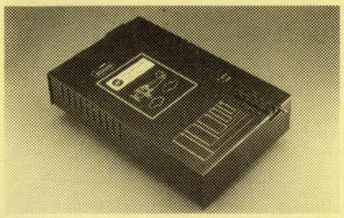

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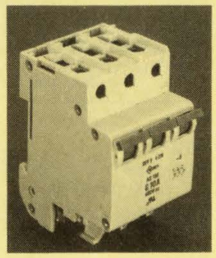

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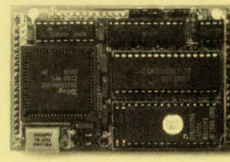

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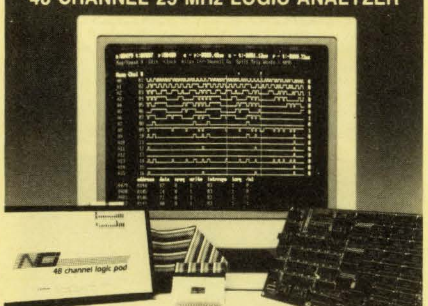

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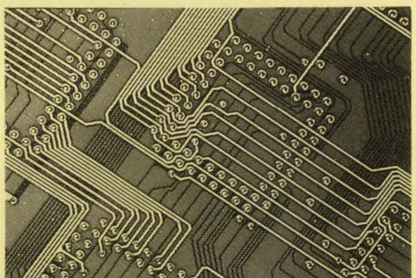

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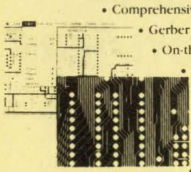

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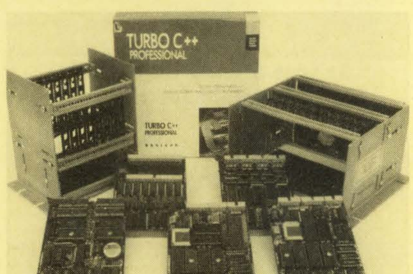

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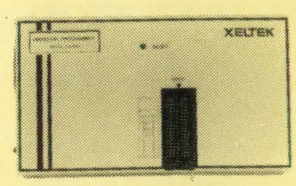

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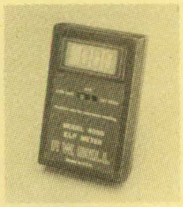

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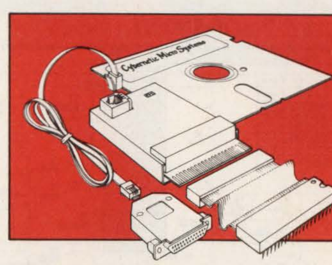

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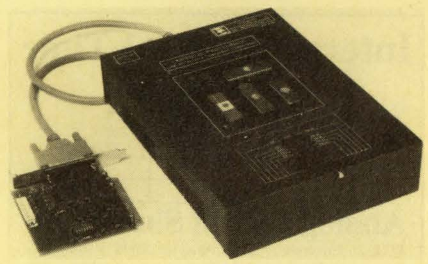

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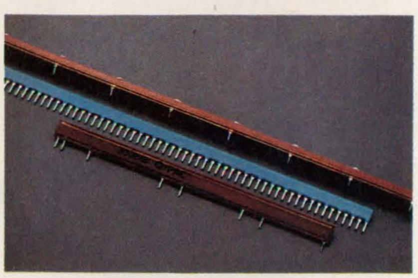

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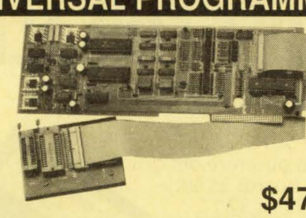

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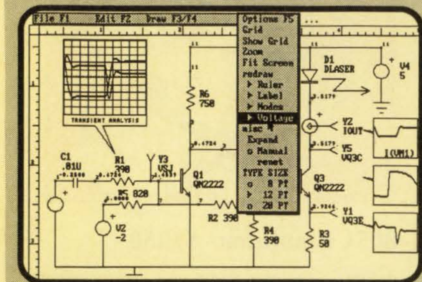

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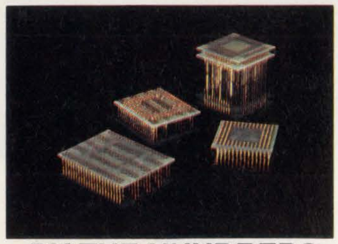

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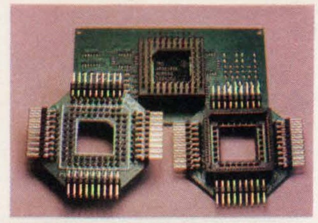

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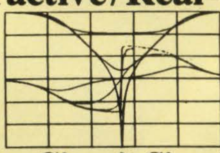

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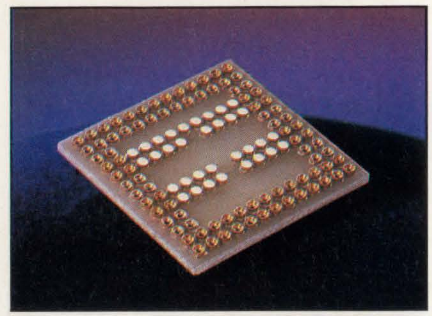

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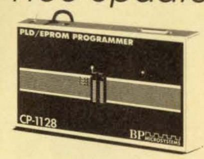

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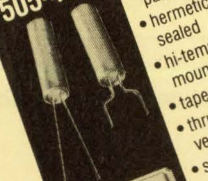

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CIRCLE NO. 156

Will you be the victim of age discrimination?

The answer is probably yes. Here's what you can do about it.

Jay Fraser,
Associate Editor

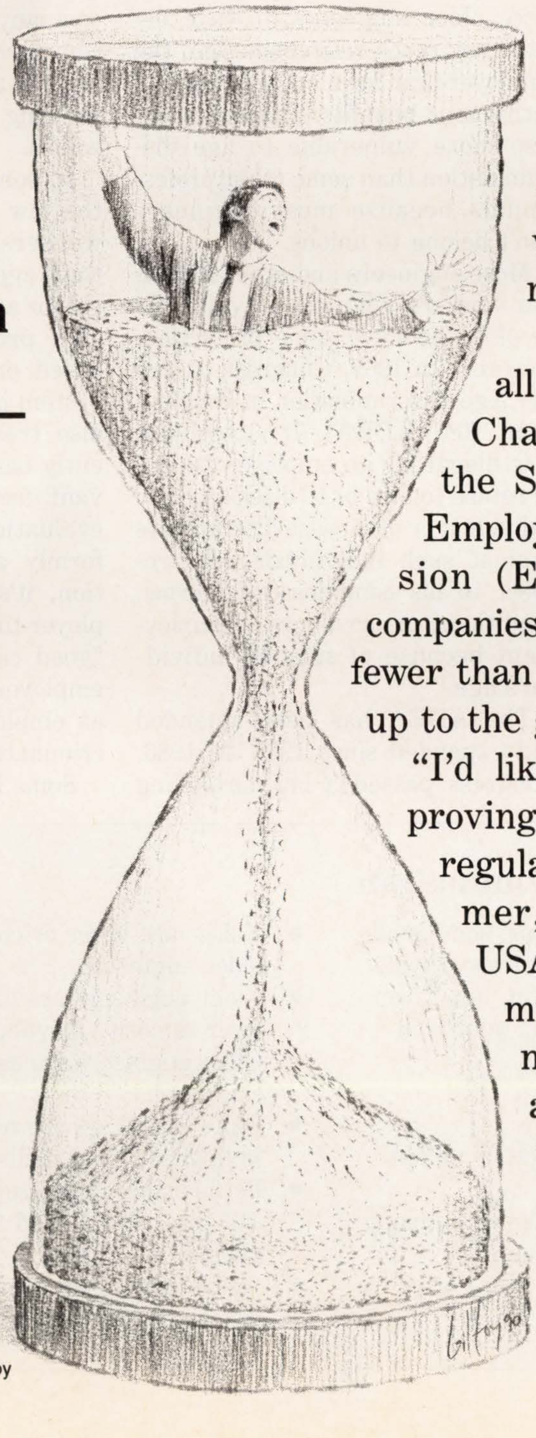

Illustration by Bruce Gilfoy

If you stay in the engineering profession after age 40, chances are that you will encounter age discrimination.

"Discrimination occurs on all levels of employment," says Charles Carattini, director of the San Jose office of the Equal Employment Opportunity Commission (EEOC), "and it occurs in companies that are small—those with fewer than 100 employees—all the way up to the giants."

"I'd like to believe things are improving due to the new laws and regulations," says Richard Plummer, Chairman of the IEEE-USA Anti-Discrimination Committee, "but in the past the majority of engineers faced age discrimination at some time in their careers."

Determining how many serious incidents of age discrimination occur each year is difficult. The federal government doesn't keep separate statistics on age-discrimination complaints. They're included in a single category along with complaints about racial, gender, and religious discrimination. Exact figures are also hard to come by because many age-discrimination cases are quietly settled out of court. However, the EEOC and state agencies receive about 25,000 complaints about all types of discrimination every year.

"I can tell you in the last five years or so, throughout the whole country there has been an increase in age-discrimination charges filed with the commissions," says Carattini. "I think it has to do with people living longer, being more active, and not seeing themselves at age 60 the way they used to."

Engineers face special problems

In some professions, such as medicine and law, age is equated with knowledge and experience. Older doctors and lawyers are sought after for their expertise. In engineering, employers all too often consider older engineers less valuable than their younger counterparts. Engineers fresh out of school supposedly bring with them a knowledge of the latest technologies and an energy that older engineers just can't match.

"Cases are settled out of court only about 33% of the time."

Another reason older engineers are often targets of age discrimination is purely financial. Younger engineers will sometimes accept jobs for low salaries just to get some experience. And if employers can force older engineers to leave before they reach retirement age, the employers can save on pensions and retirement benefits. Engineers are also more vulnerable to age discrimination than some other professionals because most engineers don't belong to unions.

Most engineers and other American workers who are 40 years old or older do have some protection, however. In 1967, Congress passed the Age Discrimination in Employment Act (ADEA). It states that it is illegal for an employer "to fail or refuse to hire or to discharge any individual or otherwise discriminate against such individuals with respect to his compensation, terms, conditions, or privileges of employment because of such an individual's age."

The ADEA has been amended and expanded since 1967. In 1986, Congress passed a law forbidding mandatory retirement and requiring employers to continue to pay into health-insurance and pension plans for workers who stay on after age 65. Last October, Congress passed the Older Workers Benefit Protection Act, which bars employers from cutting off extended benefits such as disability payments.

Not everyone comes under the protection of the ADEA, however. To qualify, you must work for a company in an industry that affects commerce, and the company must employ at least 20 people for every working day in each of 20 or more weeks.

In some circumstances, however, the law allows employers to treat workers differently according to their age. For example, it's not illegal for a company to establish a pension program or a benefit plan based on seniority as long as the system is equitable. Companies can also treat their employees differently based on reasonable and relevant factors such as performance evaluations that are applied uniformly and consistently. In addition, it's not unlawful for an employer to discharge an employee for "good cause." Of course, what an employer may consider good cause, an employee may consider age discrimination.

Some large judgments have been

Warning signs of age discrimination

Age discrimination can take many forms, some more subtle than others. Don't assume that every layoff or reassignment involves discrimination, but if you notice a recurring pattern of incidents, your company may be violating the law.

Here are some signs to watch for:

- Older engineers are often induced or forced into early retirement.
- Older engineers are laid off while the company continues to hire younger engineers.
- Lack-of-work notices are issued more often to older engineers than to younger ones.
- Raises are lower or come less frequently for older engineers.
- Older engineers are often demoted or have their seniority privileges taken away.
- Older engineers are assigned tasks below their skill level.
- Older engineers are not given opportunities to upgrade their skills.
- Performance appraisals are highly subjective and the criteria used for them are not explained.
- Age is stated—or implied—as a reason for demotion or termination.

won under the ADEA. In 1987, a court ordered Pan American Airlines to pay $17.2 million to 100 of its former pilots who had been forced to retire when they reached age 60. And in 1988, Westinghouse agreed to pay a record $35 million to a group of its former employees. The employees had sued the company because when they retired they had to choose between pensions and severance pay. Younger workers who left Westinghouse received both.

The IEEE-USA Anti-Discrimination Committee investigates age-discrimination complaints from engineers and advises them on how to deal with their companies. "It's much better if the complaint can be resolved amicably out of court," says Plummer. "The problem is most companies don't want to give away the store in out-of-court settlements. What they try to do is either talk employees into accepting marginal settlements or coerce them. In some cases they actually make veiled threats against employees."

Cathy Ventrell-Monsees is the manager of the Worker Equity Department of the American Association of Retired People (AARP) and its senior attorney. "I look at age discrimination as divorce in the workplace," she says, "and it can be just as dirty as a divorce proceeding."

If you feel you have been the victim of age discrimination and are

"Age discrimination is divorce in the workplace, and it can be just as dirty as a divorce proceeding."

considering filing a complaint, you should gather your evidence carefully. Your first step should be to begin keeping a journal or diary. "Start recording events that transpire—any statements that are made, any actions taken by the company," says Plummer. "Jot down all statements made by management regarding [your] employment or performance." Hearings and trials can drag on for months or even years. Don't depend on your memory. Keep careful records.

Make sure you have copies of your performance evaluations and any awards or letters of commendation you may have received. Once you leave a company, getting access to your files may be difficult. If you go to trial, the defense attorney may cross-examine you and call into question your record at work. Proof of a long history of solid achievement will outweigh a small mistake or two.

Also, ask your manager for a clear statement of company policies with regard to age. For example, ask for the criteria the company uses to decide who goes first in case of a layoff and who is included in training programs.

Talk to people in other areas of the company. Find out if they're facing the same problems you are and if older workers have been treated differently than younger workers in their departments. See if a pattern of discrimination emerges. If other engineers in your firm believe they have been discriminated against, you may want to join together and file a class-action lawsuit.

When you feel certain you can prove you have been the victim of age discrimination, make a complaint to the EEOC. It will investigate your complaint and, if it determines that your former employer has violated the law, take legal action for you.

Inflexible time limits

There are strict time limits on filing an age-discrimination charge. You must file within 180 days of the date of your termination or the date of the alleged discriminatory act. If you don't file within that time period, you cannot bring a lawsuit against your company. If the state you live in has a law prohibiting age discrimination and you also want to file a state charge, you must file within 300 days.

Some companies give employees notice that they will be laid off in two or three months. The time limit for filing a charge begins on the day you receive that notice, *not* on the day you eventually leave the company. Some companies lay people

Know your rights

If you think you have been discriminated against because of your age, make sure you know your rights. The IEEE publishes a booklet entitled "Age Discrimination in Employment: What Are Your Rights and Protections?" It's free upon request to both members and nonmembers. Write or phone:
IEEE-USA Anti-Discrimination Committee
1828 L Street NW, Suite 1202
Washington, DC 20036
(202) 785-0017

The US Equal Employment Opportunity Commission also publishes booklets that explain your rights and how to pursue legal action. You can visit one of its 50 local offices around the country, or write or phone its headquarters:
US Equal Employment Opportunity Commission
2401 E Street NW
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off but tell them there's a good chance they will be recalled soon. Don't let the time limit expire while you're waiting to be recalled. File as soon as you're laid off.

Once you have filed a complaint against your company, it may choose to settle with you out of court. "There's a procedure within the EEOC to deal with these cases through settlement agreements, and we use that procedure when the respondent companies or agencies wish to settle," says Carattini. "We require that [the employees] get full relief under the law, but cases are settled out of court only about 33% of the time."

If your company doesn't wish to settle, you may be in for a rough time even before you get to court. It's illegal for a firm to retaliate against a person who files a charge of age discrimination, participates in an investigation, or opposes an unlawful practice. However, that doesn't stop some companies from harassing people or trying to scare them into dropping the charge.

"They'll say they're going to prove that the charge was unjustified, that it was a frivolous lawsuit," says Plummer. "In that case, they can force the plaintiffs to pay the court costs. And any large company can generate hundreds of thousands of dollars of court costs in any given case."

"In litigation, it's not uncommon for a big company to try to paper the other side to death, filing lots of motions and taking depositions of the employee that lasts for days and days—sort of an interrogation under the lights," says Ventrell-Monsees.

Engineers who filed lawsuits against their former employers have had their pension checks stopped or their health-care benefits suspended. Any retirement perks you have earned can also disappear.

The EEOC may investigate your complaint and decide not to take legal action. If that happens, it will issue you a "right-to-sue" letter, which means it's up to you to pursue the case on you own.

"In the last five years there has been an increase in age-discrimination charges filed."

Bringing a private lawsuit

You might be better off hiring your own lawyer and bringing a civil lawsuit against your company. First of all, the EEOC has only a few hundred investigators nationwide. It may take a year or more for the EEOC to complete an investigation. Second, the EEOC receives thousands of complaints about all types of discrimination each year, but very few of them ever end up as court cases. For example, in 1986 the EEOC initiated just 118 lawsuits.

A third reason for pursuing a case on your own is that with an EEOC lawsuit, the amount of money you can recover is limited to your loss of earnings or benefits. If you win a private lawsuit, you can also collect punitive damages and damages for pain and suffering. In addition, if you can prove that there was willful discrimination against you, the court can triple the award.

Two of the drawbacks of going ahead with your own lawsuit are that hiring a lawyer may be expensive and juries are not always sympathetic to engineers.

"Juries have proved to be sympathetic in blue-collar discrimination cases, more so than in white-collar cases," says Plummer. "I suspect that many jurors look at engineers and think, 'They've got a degree in engineering and they're highly paid, and they've earned all this money all their lives. They certainly should have saved enough to get along without a job for a while, and in all probability they'll be able to obtain another high-paying job. Why should I give them a big bundle?' "

Be sure your case is sound and you're ready for a long haul before you plunge in. "You're going to have to find a lawyer who will give you an accurate and open assessment of how things stand," says Ventrell-Monsees. "You have to make an emotional commitment to proceed with the litigation. It's going to take up a lot of energy. You're making a commitment that will consume your life for a while."

Preventive measures

You and your company don't have to end up in court. You can take some measures to protect yourself from age discrimination.

Make sure you take part in your company's training programs. Firms sometimes cite an engineer's lack of knowledge of current technology as a reason for termination. You should also take outside courses to keep your knowledge up-to-date and your skills sharp.

Ask your manager for more challenging projects or volunteer for extra assignments. It's widely believed that older workers aren't as productive as younger ones. Continually doing the same type of work and never stretching yourself will only reinforce that myth.

Don't make obvious mistakes such as constantly arriving at work late, taking extended lunch hours, or missing deadlines. Companies have used all of these reasons to get rid of workers.

Ventrell-Monsees says employees can defend themselves against age discrimination by taking two basic steps: "They should know their rights and not be afraid to speak up about what they see as unfair treatment." EDN

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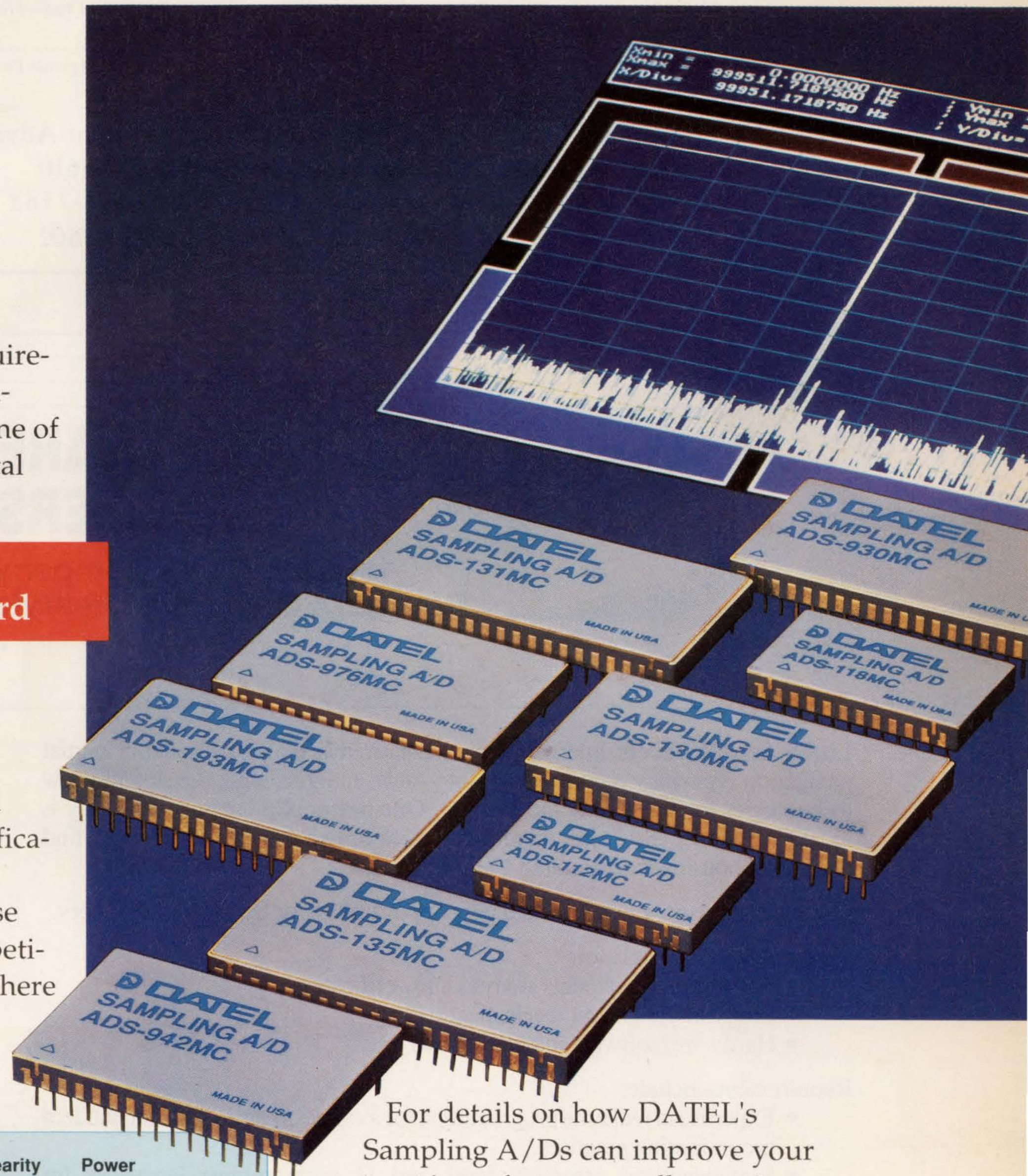

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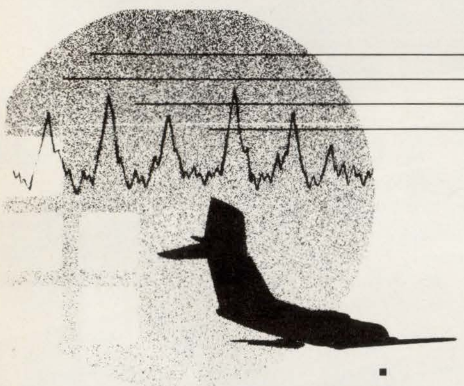

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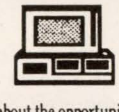

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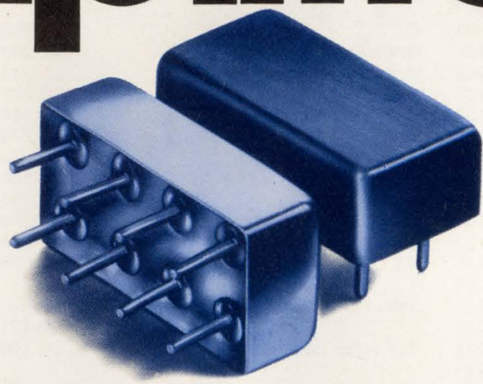

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