A CAHNERS PUBLICATION INTERNATIONAL EDITION OCTOBER 24, 1991

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report: Existing networks reach new age with ISDN ICs

pg 112

A Promise For Both Of Us To Keep.

Promises only count when they're kept. This one is no exception.

In the coming months, you will see a number of corporate advertisements from AVX. Each is different by virtue of its subject matter – our diverse product line, our advanced manufacturing capability, quality assurance, to name but a few. Yet all give voice to a single, steadfast goal. *AVX will do whatever it takes to surpass customer expectations, in every area of the company, every working day.*

AVX is so determined to hold to this promise, we'd like you to hold it as well. So we invite you to tear out this page and place it on the wall beside your desk. From that moment forward, call any AVX location anywhere in the world whenever you need our assistance, whether it's finding the right component or solving a special requirement. And call us on it if we ever fail to measure up to your expectations.

At AVX, we believe nothing is more important than the trust between you – the customer – and us. So this promise is not one we make lightly. We intend to keep it. We must keep it. We hope you will, too.

Thank you.

Marshall D. Butler
Chief Executive Officer
AVX Corporation

Ask the World of Us.

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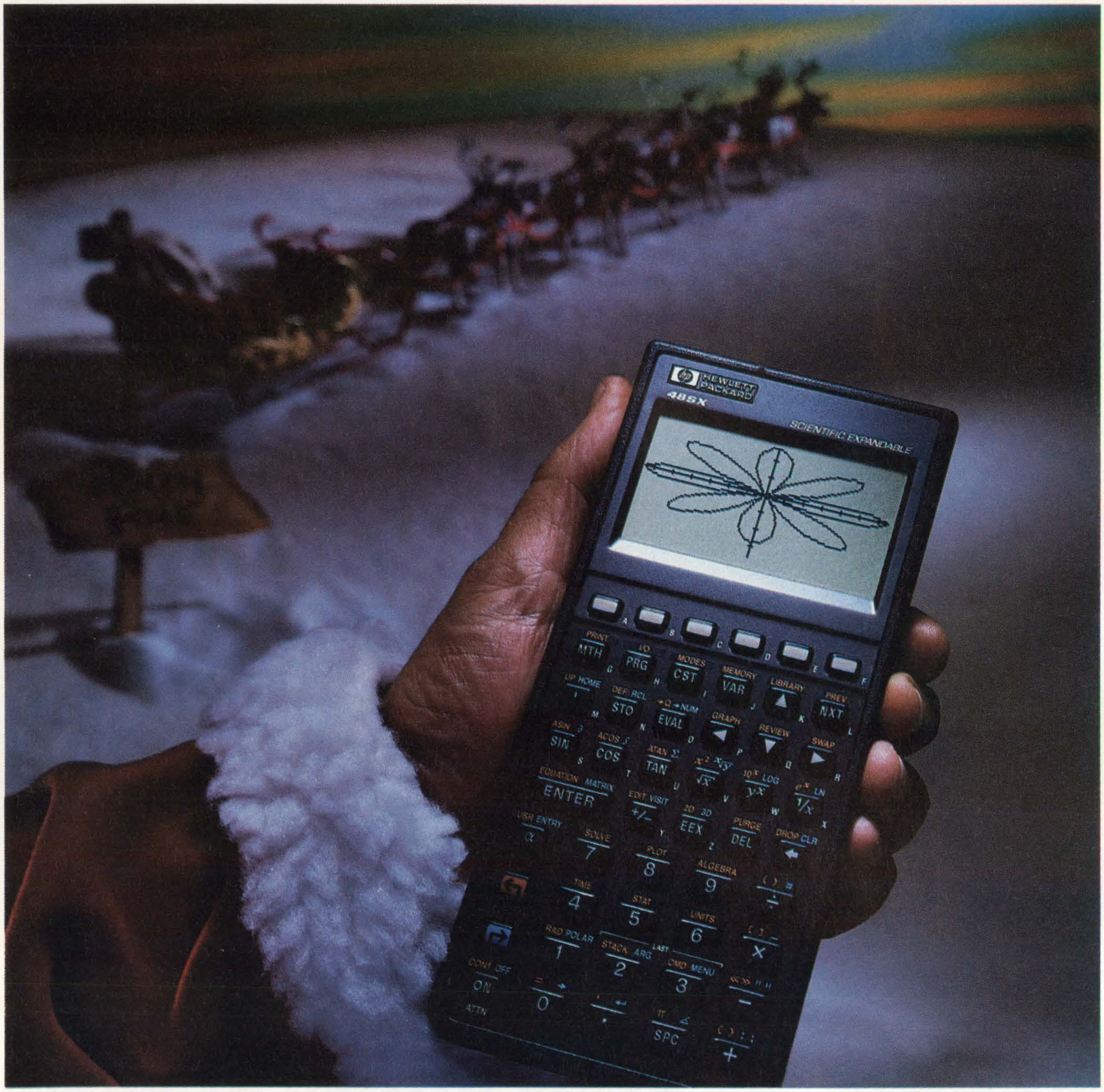

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No wonder the revolutionary HP 48SX is on so many wish lists this year. It's the only scientific calculator that has over 2100 built-in functions and custom capabilities.

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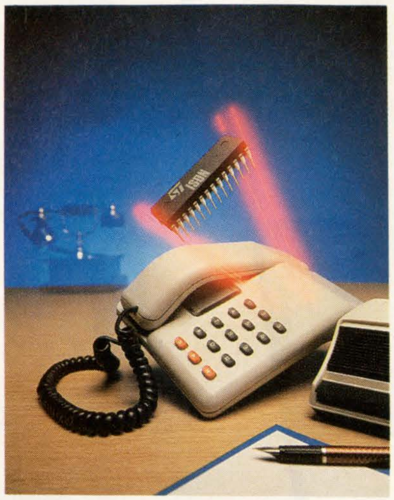
HEWLETT PACKARD

EDN Magazine Edition

Volume 36, Number 22 October 24, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Although twisted-pair phone wires are inadequate for digital-data relay, basic-rate ISDN ICs modernize these existing networks for voice and data communications. See our Special Report on pg 112. (Photo courtesy SGS-Thomson Microelectronics)*

Continued on page 7

EDN® (ISSN 0012-7515, GST Reg. #123397457) is published 48 times a year (biweekly with 2 additional issues a month, except for February, which has 3 additional issues and July and December which have 1 additional issue) by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President; Frank Sibley, Executive Vice President; Jerry D Neth, Senior Vice President/Publishing Operations; J J Walsh, Senior Vice President/Finance; Thomas J Dellamaria, Senior Vice President/Production and Manufacturing; Ralph Knupp, Vice President/Human Resources. EDN® is a registered trademark of Reed Properties Inc., used under license. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. **POSTMASTER: Send address corrections to EDN®, PO Box 173377, Denver, CO 80217-3377.** EDN® copyright 1991 by Reed Publishing USA; Ronald G Segel, Chairman and Chief Executive Officer; Robert L Krakoff, President and Chief Operating Officer; William M Platt, Senior Vice President. Annual subscription rates for nonqualified people: USA, $119.95/year; Mexico, $169.95/year; Canada, $181.85/year; all other nations, $209.95/year for surface mail and $329.95/year for air mail. Single copies are available for $15. Please address all subscription mail to Ellen Porter, 44 Cook Street, Denver, CO 80206-5800.

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EDN Magazine Edition

October 24, 1991

TECHNOLOGY UPDATES *(CONTINUED)*

EDITORS' CHOICES

PRODUCT UPDATES

DESIGN IDEAS

NEW PRODUCTS

DEPARTMENTS

Cahners Publishing Company, A Division of Reed Publishing USA ☐ Specialized Business Magazines for Building & Construction ☐ Research ☐ Technology ☐ Electronics ☐ Computing ☐ Printing ☐ Publishing ☐ Health Care ☐ Foodservice ☐ Packaging ☐ Environmental Engineering ☐ Manufacturing ☐ Entertainment ☐ Media ☐ Home Furnishings ☐ Interior Design ☐ and Lodging. Specialized Consumer Magazines for Child Care ☐ Boating ☐ and Wedding Planning.

It's Also More Power

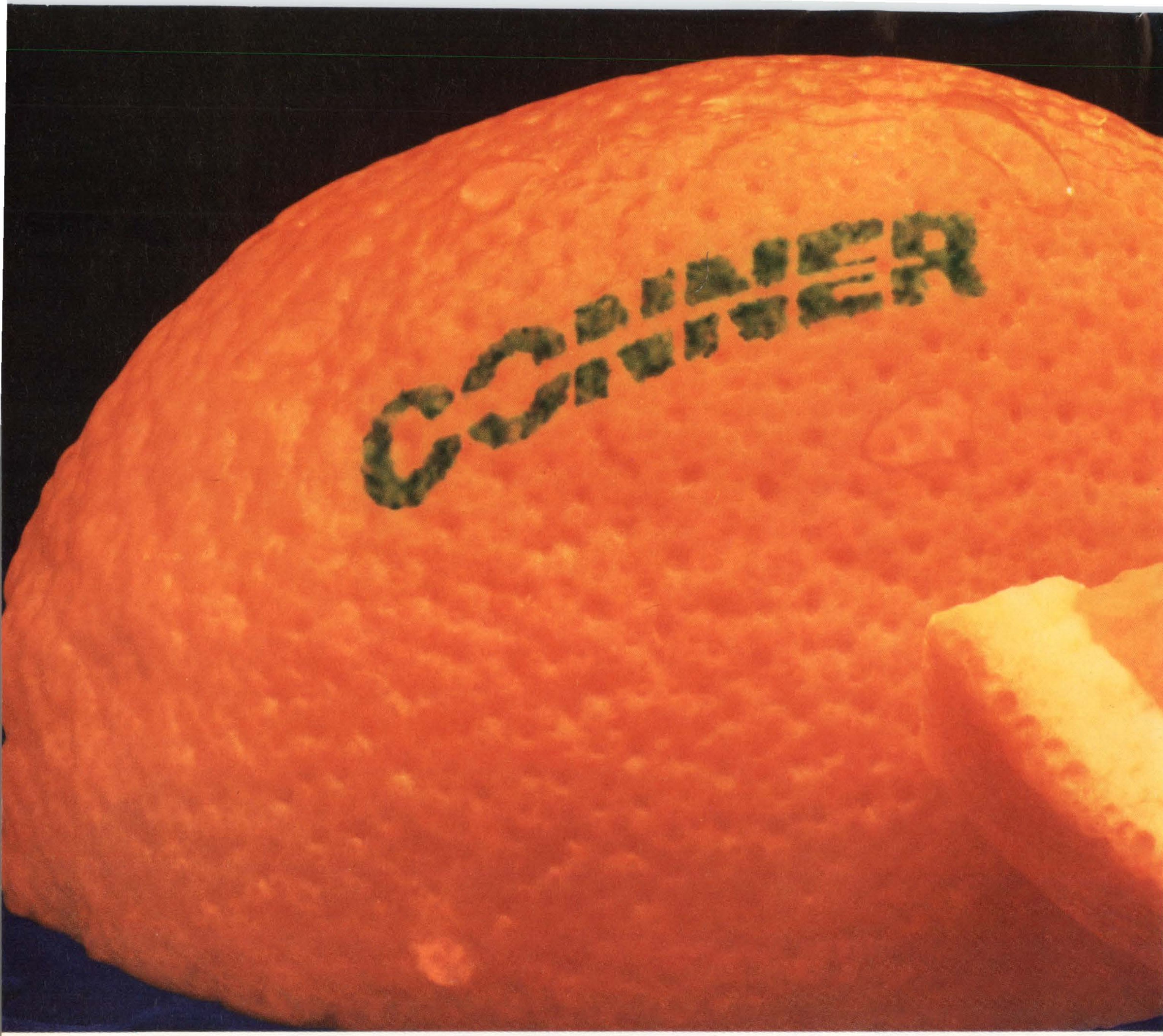
Introducing The 40MHz Am386™ Microprocessor— The Speediest 386 On The Planet.

It looks like a mild mannered 386. In fact, it is: A genuine, plug-in replacement for the i386. Except it's faster. Burns less power. Costs no more. And it's available now.

The Am386DX-40 microprocessor can transform any ordinary 33MHz system into an invincible, 25% faster, 40MHz Am386 system. So you can easily offer the world's fastest 386 performance.

PQFP packaging

It's not only super-fast, it's also super-efficient, thanks to its truly static

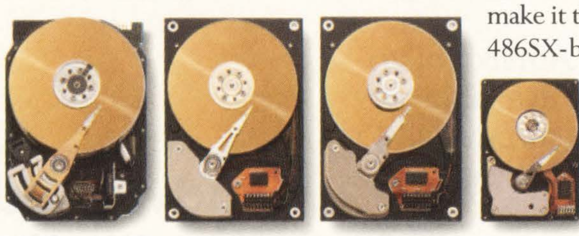


ANY WAY YOU SLICE IT, GENERATION COVERS EVERY

The squeeze is on. Today the PC market is rapidly concentrating into three segments: Notebooks, Desktops and Workstations. And once again, Conner has anticipated these changes.

Which is why we're introducing our newest wave of high-performance 2.5-inch and 3.5-inch drives to meet the needs of each of these evolving market segments.

For the notebook market, take our newest Pancho drive.



Summit 540MB · *Cougar 210MB* · *Jaguar 85/170MB* · *Pancho 85MB*

With 85 Mbytes, it offers the highest capacity available in a light weight, patented 2.5-inch form factor. Low power consumption, rugged packaging and a compact form factor make it the ultimate choice for 386SX and 486SX-based notebook computers.

Then there's our new Jaguar Series for the desktop market—3.5-inch drives offering 85 and 170 Mbytes. A 17 msec. average seek time and a light weight, patented 1-inch

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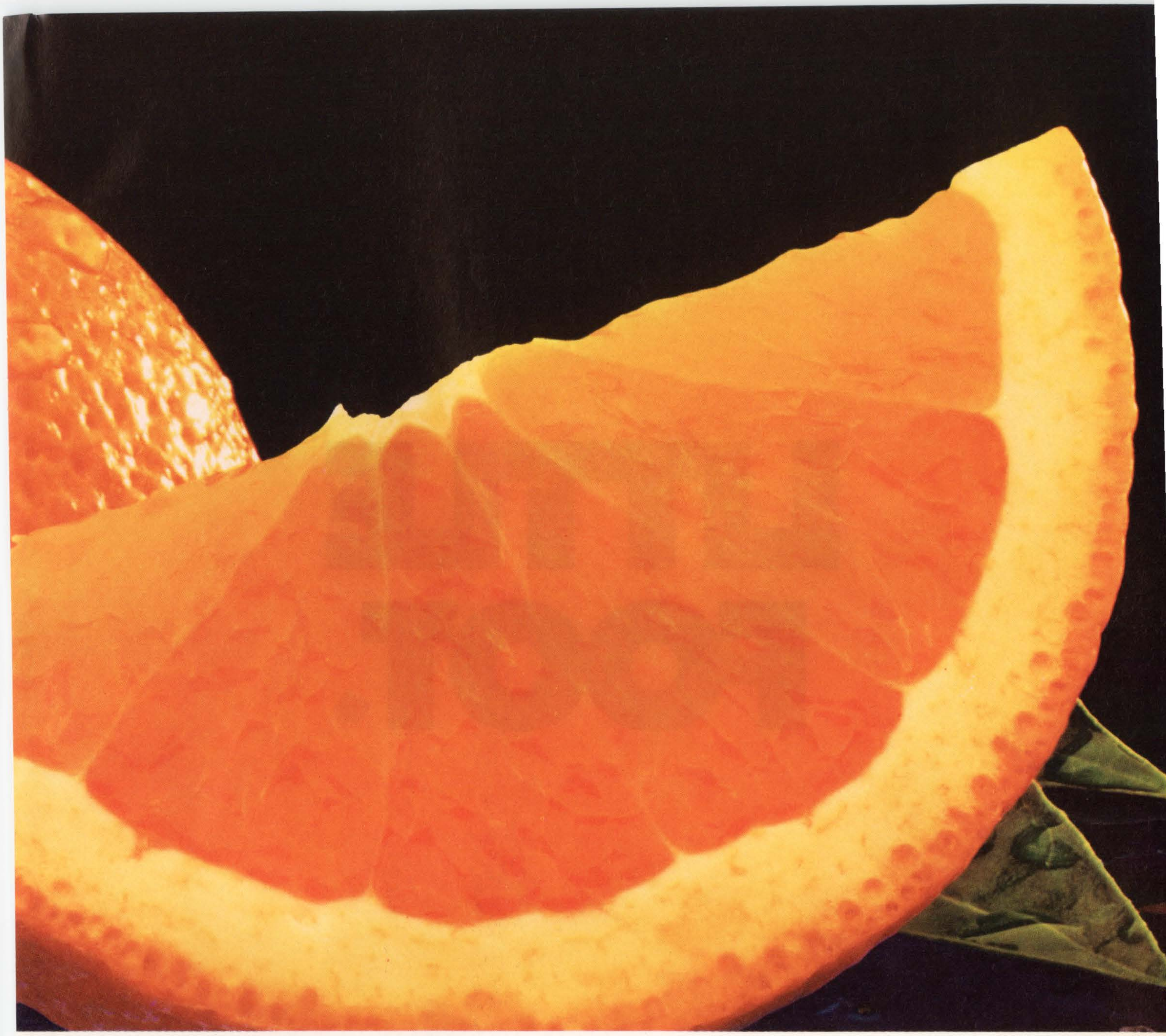

CONNER'S NEWEST SEGMENT OF THE MARKET.

high form factor make them ideal for a full range of desktop computers.

For workstations, we're introducing two new 3.5-inch drives—the 210 Mbyte Cougar and 540 Mbyte Summit. Cougar is the highest performance low-profile drive on the market today. While Summit delivers the greatest capacity and performance of any 3.5-inch drive. Both provide a fast average seek time of 12 msec., a 2.5 Mbyte per second sustained transfer rate and a SCSI-2 interface.

It's all a part of our innovative sell-design-build business philosophy. To identify our customer's needs sooner. Then fill them faster with the most advanced products. In fact, we're the technological leader with nine patents issued and 27 pending. Which is why more and more PC users are asking for systems with Conner drives.

So if the changing market segments are putting the squeeze on your systems, call us today. We'll guarantee you the most refreshing results.

CONNER

Delivering A Generation Ahead

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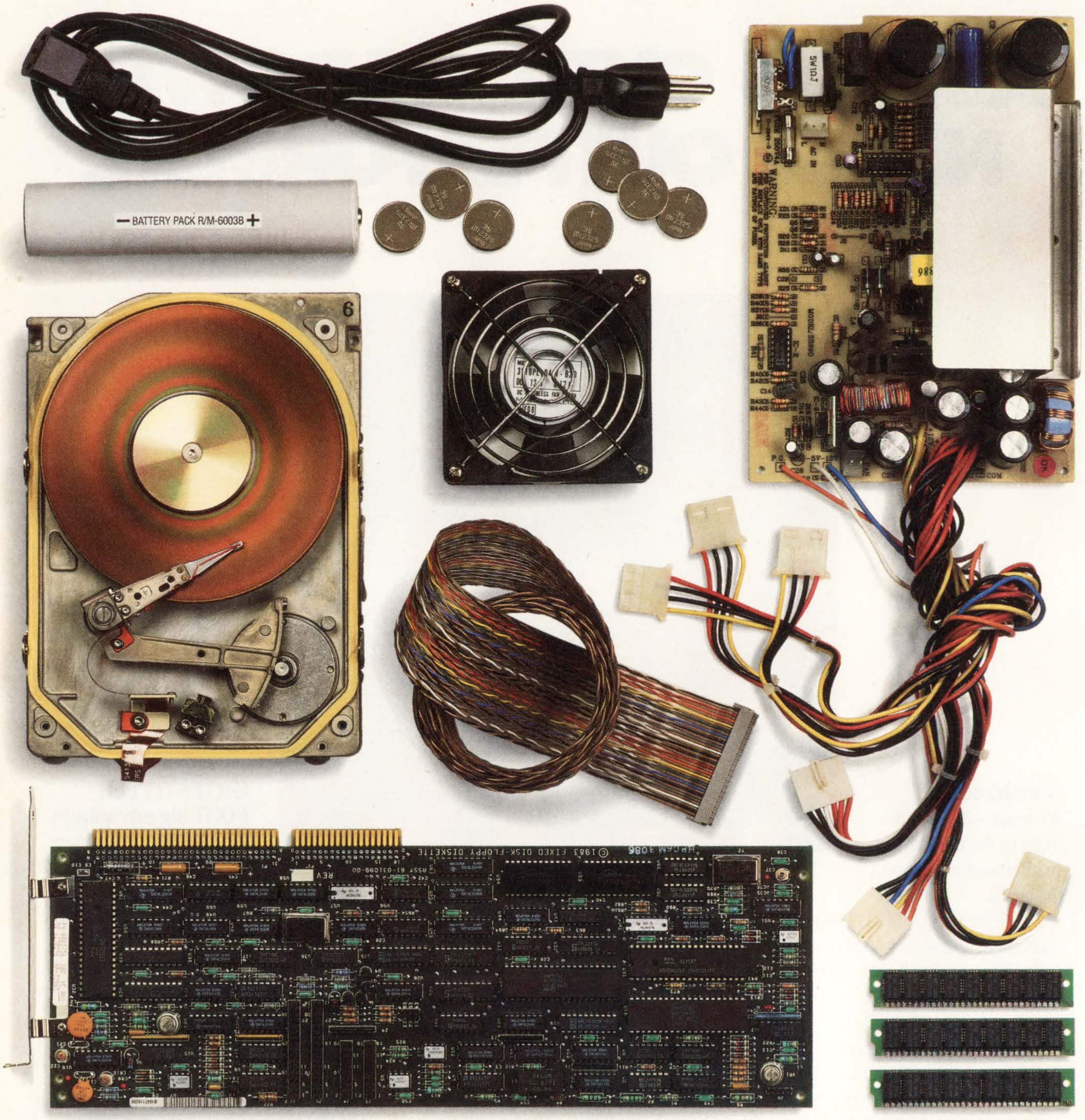


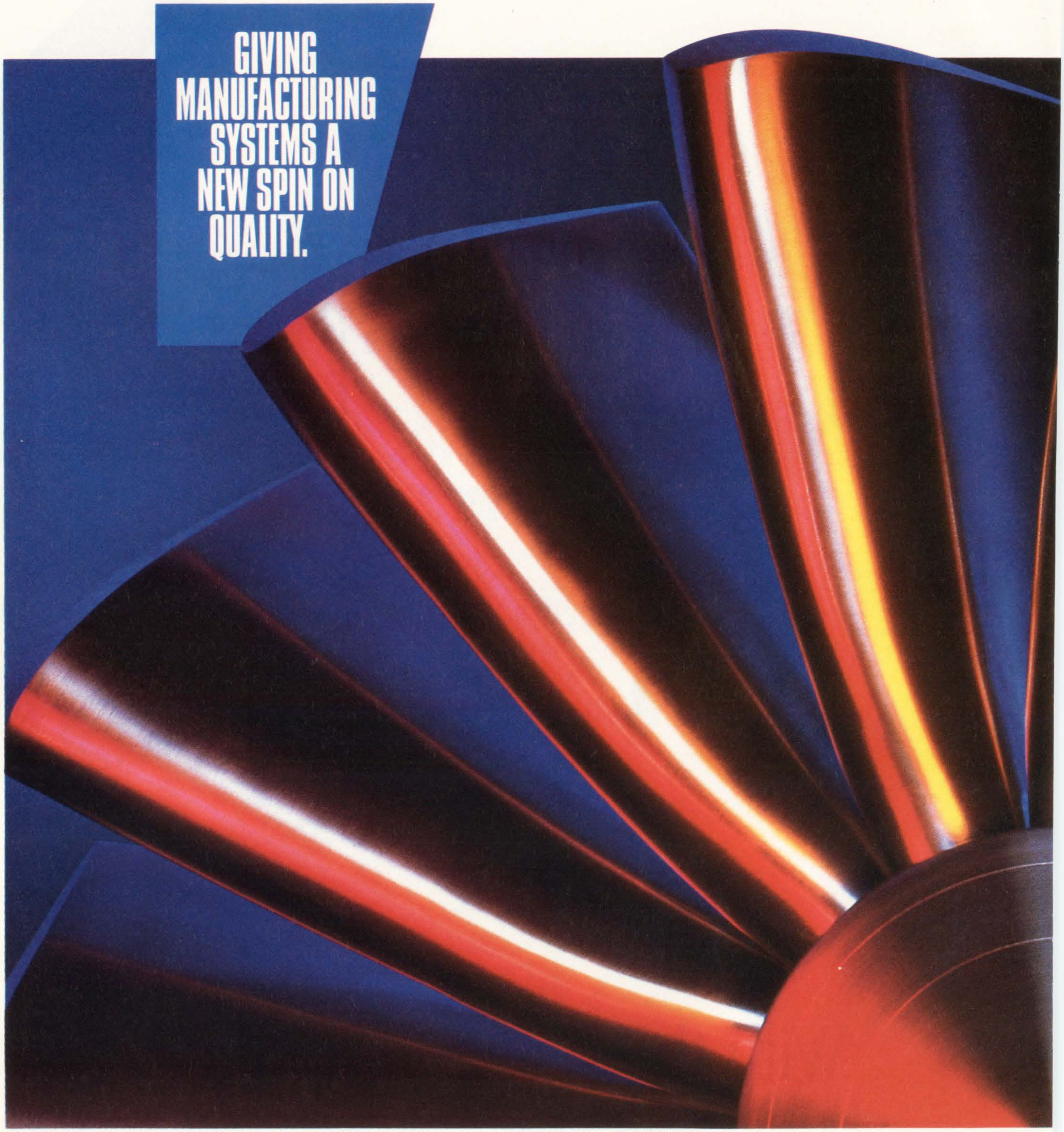
Make all these disappear.

Poof, they're gone. Bulky battery packs, slow hard disks and more. You see, where memory cards make sense, the new Intel 4MB Flash Memory Card provides a high-density, read/write, truly nonvolatile portable storage solution.

The real trick, of course, is that it allows you to store large amounts of code or accumulate data in a small, rugged card that uses less power than traditional memory technologies. So now you can design products that are faster, lighter, tougher and more energy efficient.

Not tomorrow, but today. Thanks to our System Developer's Kit. A DOS-compatible package that includes a 1MB Flash Memory Card, an add-in board as well as design information. In addition, it includes an evaluation copy of Microsoft's Flash File System software. All the stuff to get you started—now!

Plus, Intel's Flash Memory Card is the first to comply with the 68-pin PCMCIA/JEIDA standard. This allows the card and its data to be interchangeable between a host of



SIGNAL PROCESSING AND

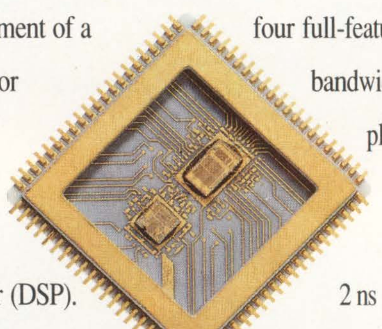
You have to build a
to build just

The new Tek TDS Series

More than a million Tektronix oscilloscopes have all been leading up to this: the most powerful, versatile, and intuitive instruments ever developed for the mainstream of test and measurement.

The new TDS 500 Series is the culmination of everything Tek has learned in the design, manufacture and use of digitizing oscilloscopes. It's an achievement made possible only by the unique integration of acquisition functions and combinational trigger logic onto a single board.

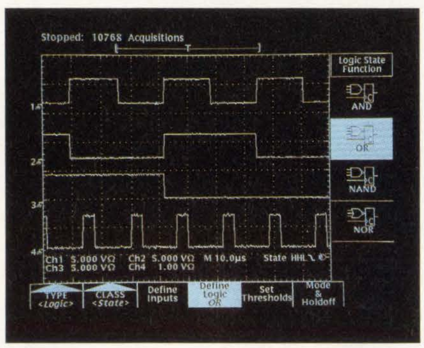
Only by the development of a milestone multiprocessor architecture.



Only by the addition of Tek's TriStar™ Digital Signal Processor (DSP).

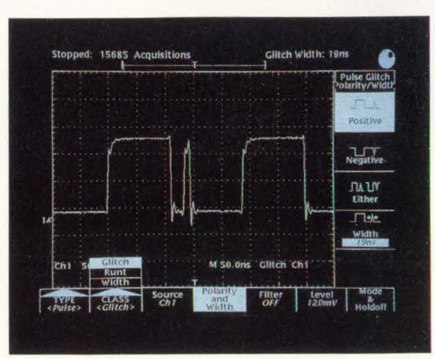
Only by Tek's capacity for taking the hard work out of high performance.

The TDS Series performs, *live,* updates and measurements that inhibit most other digitizing scopes. Its real-

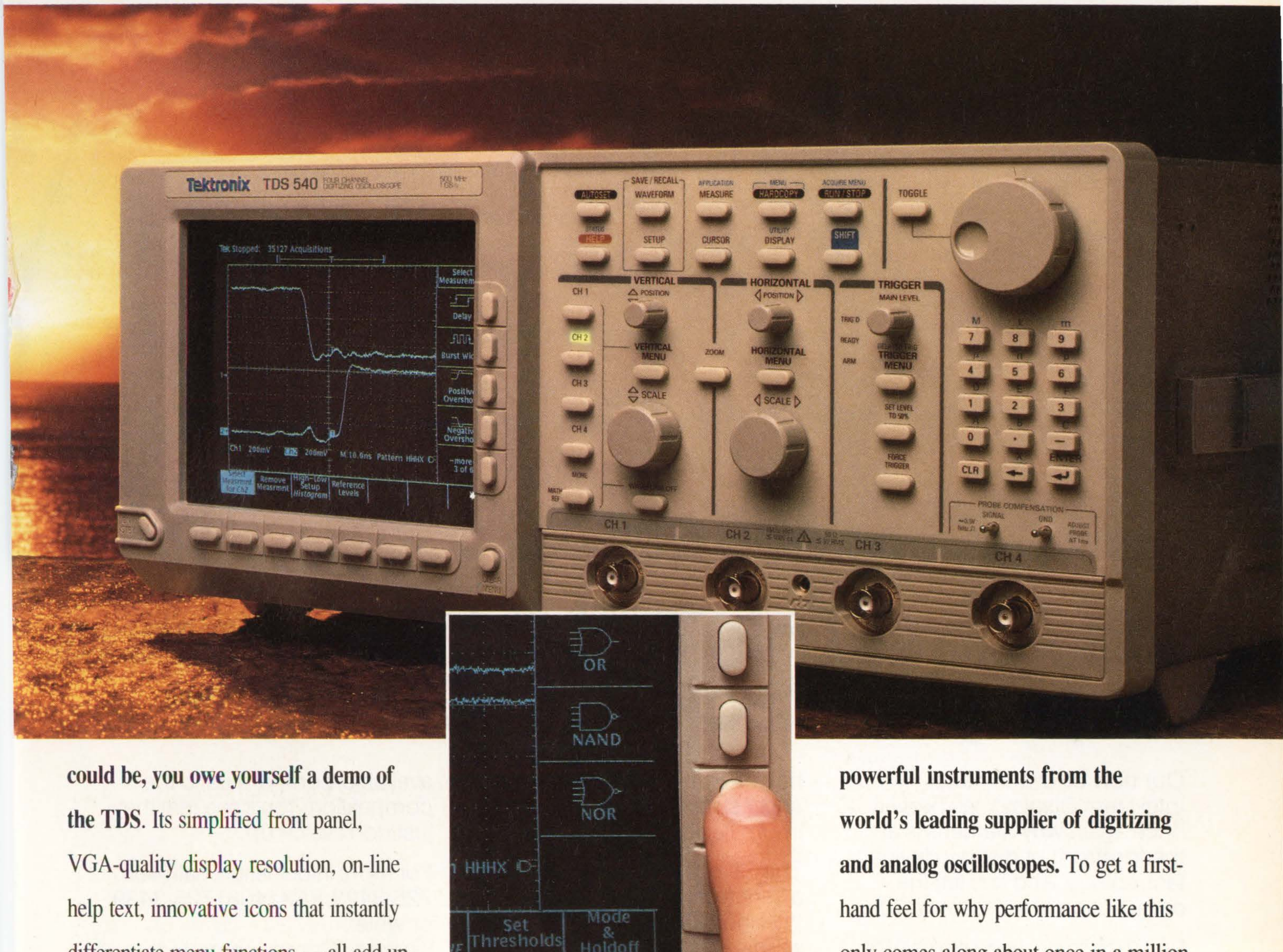


time DSP lets you perform single-shot averaging and extend resolution to 12 bits. The TDS Series arms you with up to four full-featured channels. 500 MHz bandwidth. Up to 1 GS/s sampling and 4 ns peak detect. Up to 50K record lengths. Time interval, 2 ns glitch, runt, pattern and state triggers. With acquisition sensitivity and fast overdrive recovery bringing greater waveform detail within your grasp.

And if you think oscilloscopes aren't as easy to use and comprehend as they



million oscilloscopes one like this.



could be, you owe yourself a demo of the TDS. Its simplified front panel, VGA-quality display resolution, on-line help text, innovative icons that instantly differentiate menu functions — all add up to a scope that makes the user's manual more a formality than a necessity.

The TDS Series signals the start of a new generation of friendlier, more powerful instruments from the world's leading supplier of digitizing and analog oscilloscopes. To get a first-hand feel for why performance like this only comes along about once in a million scopes, contact your Tek sales engineer or call **1-800-426-2200.**

One company measures up.

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NEWS BREAKS

EDITED BY SUSAN ROSE

TELECOM PC-BOARD TESTER TAPS VXI TECHNOLOGY

The GR9000 telecommunications test-and-measurement system from GenRad Inc uses the largest VXI boards (the so-called D size) to minimize cabling and to accommodate very large amounts of computing power. The test system suits complex mixed-signal pc boards used in large numbers in telephone central offices and private-branch exchanges. The system achieves some of its capabilities by harnessing a feature of the VXIbus modular-instrument standard that until now has attracted only limited interest. Because the VXI modules mount in the system's test head and contain connectors not found on smaller VXI boards, the system needs a minimum of cabling to connect to a unit under test—regardless of whether the connections are made by pogo pins or edge connectors. Moreover, the large VXIbus boards permit each system to include multiple-array processors, thus enabling high-speed number crunching. Adapters let the system hold smaller VXI units needed in specific applications. To provide users with a flexible set of test-program development tools, the vendor based its software on Labwindows from National Instruments (Austin, TX). The system costs $120,000, and a typical configuration costs $225,000. GenRad Inc, Concord, MA, (508) 369-4400.—Dan Strassberg

STATIC 80186 MINIMIZES POWER AND UPS PERIPHERALS

Intel has shifted its 80186 to a static core, adding a 3-level power-management control for low power applications. There are three new power modes: Idle (freezes CPU, keeps peripherals active), Powerdown (freezes internal clocks), and Powersave (a programmable internal clock divider to run at slower rates). With Idle and Powerdown, power consumption is less than 100 μA typ. There are three new microcontrollers: The 80C186EC has four DMA channels, two interrupt controllers, 22 I/O pins, four timers, and standard peripherals; the 80C186EA combines the power management modes with 5 and 3V operation and a static core; and the 80C186XL is compatible with the existing processor, but adds a static core and a 20-MHz clock. Prices start at $17.70, $11.80, and $11.80 (1000), respectively. Intel Corp, Santa Clara, CA, (408) 987-8080.—Ray Weiss

MAC LINE EXPANDS BY SIX, INCLUDING LAPTOPS

Apple Computer is adding six new machines to its Macintosh line of personal computers: three desktops and three laptops. The 68030-based Mac Classic II, an extended version of the Mac Classic, executes applications programs at approximately twice the speed of its predecessor and rivals the performance of the Mac SE30, which will be phased out of production. You can upgrade your computer for $699.

The company has also started two new product lines. The Macintosh Quadra computers use 25-MHz 68040 CPUs and feature built-in support for all of the company's monochrome and color monitors, offering as many as 32 bits/pixel for graphics. Both the $6499 700 and $8699 900 include SCSI and Ethernet ports as well as Appletalk and the company's Desktop Bus. They also offer Nubus expansion slots; two and five, respectively. Owners of the Mac IIfx can upgrade to a 700 for $3500.

The other new line, the Powerbook series, brings the company into the laptop-computer market. All three units, the 100 ($2500), 140 ($3200), and 170 ($4600), feature 640×400 displays, a built-in trackball, and internal hard-disk drives. The 140 and 170 also have built-in floppy drives. The three units use different CPUs: 68000s, 16-MHz 68030s, and 25-MHz 68030 with a coprocessor, respectively. Apple Computer Inc, Cupertino, CA, (408) 996-1010, TLX 171576.—Richard A Quinnell

NEWS BREAKS

VXIBUS CONSORTIUM MEMBER UNVEILS TEST PRODUCTS

Brüel & Kjaer's range of VXIbus products form the basis of the model 3538 modular test system. The system includes a size C, 13-slot cardframe controller, slot-0 modules, a signal processor, a configurable switch, a memory module, and a development card. Software support includes an object-oriented operating system, Pascal, system device drivers, and generic device-driver development software. Three versions of controller and slot-0 modules offer interfacing via IEEE-488 (model 7513, $6800), Ethernet (model 7514, $7300), or both (model 7527, $8900). The multitasking DSP module, model 3152 ($9500), handles signal-analysis and waveform-generation tasks with 32-bit floating-point accuracy. Switch module, model 3153 ($3350), lets you connect twelve 6-MHz signals in a variety of multiplex or matrix configurations. Memory module, model 7403 ($2350), expands storage of the 3538 system from 4 to 128 Mbytes by adding single in-line memory modules. The 7630 multiuser Felix operating system ($5400) lets you develop system software on a Unix workstation connected to the system via Ethernet. Multiuser capabilities of Unix and Felix, combined with LAN support, enable remote users to work on program development and production test simultaneously. You can use C or FelixPascal program languages for embedded control. FelixPascal (7602, $3800), is an extension of standard Pascal to suit the operating system and enable parallel programming. Brüel & Kjaer, Naerum, Denmark, 4280-0500, FAX 4280-1405. In US, (508) 481-7000, FAX (508) 485-0519.—Brian Kerridge

SOFTWARE ROUTES MULTIPLE FPGA ARCHITECTURES

NeoCAD is developing a tool suite to route field-programmable gate arrays (FPGAs) from several vendors. The product includes place-and-route algorithms tailored to specific FPGAs, unlike current tools from Data I/O, Exemplar Logic, and Viewlogic Systems that provide FPGA-device independence via individual FPGA mapping routines. The software will accept timing constraints that ensure that layouts meet design specifications. The initial release will include place-and-route algorithms for at least Actel and Xilinx FPGAs. The software will accept data in EDIF (Electronic Design Interchange Format), LPM (Library of Parametrized Models), and Xilinx and Actel proprietary formats. Scheduled for January availability, the software runs on 386 or 486 PCs and Unix workstations under X-Windows and Motif. The software is expected to cost less than $20,000. NeoCAD, Boulder, CO, (303) 442-9121, FAX (303) 442-9124. Xilinx, San Jose, CA, (408) 559-7778. —Michael C Markowitz

GYROSCOPE-BASED POINTING DEVICE HANDLES 3-D

The Gyropoint pointing device from Gyration Inc looks like a mouse, but it's a mouse with wings. The gyroscope-based device isn't confined to a table top. In its mouse-compatible mode, you can move the pointer in free space to control the cursor on your computer monitor. In the pointer's 3-D mode, it provides an additional degree of freedom, giving you your choice of XYZ position or roll, pitch, and yaw.

The pointer is a demonstration vehicle for the company's core technology, a miniature gyroscope. This device, called the Gyroengine, uses optical sensing and a built-in microcontroller to provide angular position measurements directly to a computer in RS-232C and serial-data formats. The device measures 1.75 × 1.25 in., runs on 3V, and consumes 0.1W while running. A developer's kit for the engine, comprising a pointer, interface schematics, and technical data, is available for $1000. Gyration Inc, Saratoga, CA, (408) 255-3016. Contact Laurie Schuler.—Richard A Quinnell

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Let MicroSim Corporation help you achieve your circuit engineering goals with our family of CAE packages— Genesis, Circuit Analysis, and Circuit Synthesis.

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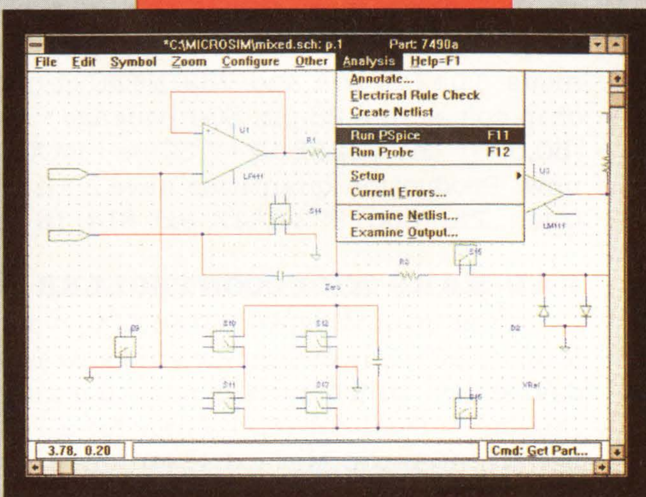
Our new Genesis package includes Schematics, a versatile schematic capture front-end to our popular Circuit Analysis programs, PSpice and Probe. Circuit definition is simple and flexible with Schematics' graphical circuit and symbol editors. Iterative adjustment of PSpice analysis parameters and invocation of PSpice simulations is convenient and direct through Schematics' pull-down menus and dialog boxes. Visual inspection of simulation results is just as straightforward since Probe is run directly from Schematics.



Schematics as a Windows 3.0 application

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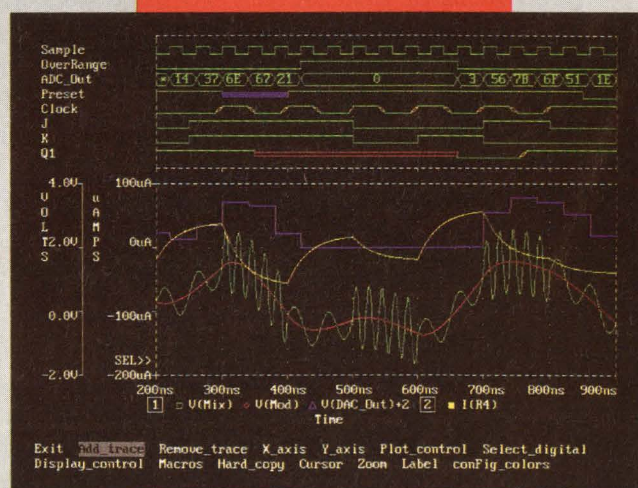
In-depth examination and processing of PSpice simulation results is more powerful than ever with Probe's new Performance Analysis and multiple Y axes features. Together with Probe's high resolution plotting, simultaneous display of analog and digital waveforms, and all of the other features that have made Probe so popular, the power is at your fingertips.



Analog and digital waveforms with multiple Y axes in Probe

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CIRCLE NO. 28

LOW-POWER MODEM CHIP SET HAS V.32BIS/FAX CAPABILITY

Available in two versions, a 3-chip set from AT&T Microelectronics targets low-power, high-speed applications in laptop computers and pocket modems. Consuming 450 mW of power, the chip sets support either V.32 + fax (9600-bps data and send/receive fax) or V.32bis + fax (14,400-bps data and 9600-bps send/receive fax). Each chip set contains a ROM-coded DSP16A to handle modem protocol processing, a T7525 coder/decoder serving as the analog front-end, and a V32INTFC data-pump interface that integrates peripheral circuitry. Needing no extra memory, the chip sets minimize power consumption and board space—important considerations in laptop computers.

The chip sets are downward-compatible with other modem standards, such as V.22bis, V.22, V.23, V.21, and Bell 212A and 103. Both chip sets also support fax-modem standards V.29, V.27ter, and V.21. They also feature a voice pass-through mode. The DSP16A and V32INTFC chips come in 84-pin quad flatpacks, and the T7525 chip comes in a 28-pin SOJ package. The V32F-LT (V.32 + FAX) chip set costs $75 (50,000); the V32FB-LT (V.32bis + FAX) chip set costs $85. Samples are available now. Production quantities have a 12-week lead time. AT&T Microelectronics, Allentown, PA, (800) 372-2447, ext 814; in Canada, (800) 553-2448, ext 814.—Dave Pryce

RAD-HARD MICROCONTROLLER EXECUTES 8 MIPS PEAK

United Technologies' UT69R000 is a 16-bit, 16-MHz, Rad-hard CMOS microcontroller (μC). The controller guarantees single-event upset of less than 25.6E-6 errors/device-day, which corresponds to a minimum linear-energy threshold of 40 MeV (mg/cm^2). Total dose immunity for all static and dynamic specifications is 1 Mrads(Si) per MIL-STD-883 Method 1019. The fully static design consumes less than 500 mW at 16 MHz. The μC features a 64k × 16-bit address space for data and a 1M × 16-bit address space for instructions. Embedded peripherals include a 9600 baud UART, two 16-bit interval timers, and nine hardware interrupts. The controller executes 35 instructions, most of which execute within two clock cycles, using a 32-bit accumulator and twenty 16-bit data registers that you can concatenate to 32 bits. The processor supports multiprocessor operation, DMA, and bus arbitration through bus handshaking. In a 144-pin PGA, tested to level S screening, the part costs $4744 (100); delivery is 26 weeks ARO. United Technologies Microelectronics Center, Colorado Springs, CO, (719) 594-8000.—Michael C Markowitz

CHAIRMAN AND CHIEF EXECUTIVE OF CAHNERS DIES

Ronald Segel, chairman and chief executive of Cahners Publishing Co, which publishes EDN, and deputy chief executive of parent-company Reed International PLC, died on August 31. Mr Segel died at the age of 56, after a year-long bout with cancer. A native of Boston, MA, he was a graduate of Harvard University and the Harvard Business School. Mr Segel was a quiet and private man who spoke most eloquently through his vision for Cahners and his dedication to its employees. His vision and judgment ensures that Cahners' publications will continue to increase their value to readers and advertisers for many years.

When Mr Segel joined the company as vice president of finance in 1971, Cahners was a trade-magazine company with annual revenues of $50 million. Twenty years later, Cahners is the core of a $1.3 billion communications company. Cahners, under Mr Segel's guidance, grew to a company with 84 publications, and is the leading trade publisher in the US and a growing force in consumer publishing.—EDN staff

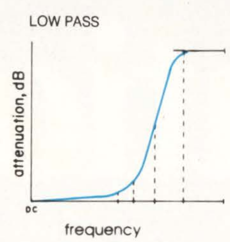
CIRCLE NO. 29

FILTERS

dc to 3GHz from $11^{45}

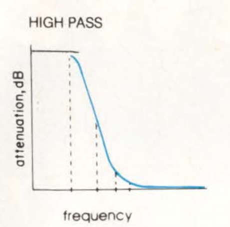
lowpass, highpass, bandpass, narrowband IF

- less than 1dB insertion loss • greater than 40dB stopband rejection
- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests
- rugged hermetically-sealed pin models • BNC, Type N; SMA available
- surface-mount • over 100 off-the-shelf models • immediate delivery



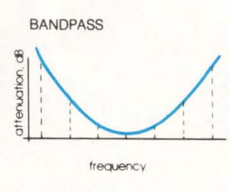
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



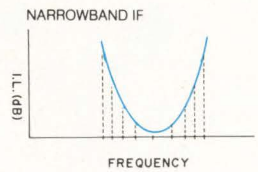
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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In fact, Fujitsu pioneered the 68-pin memory card and was the driving force in making it an international standard.

And if that's not big enough news, Fujitsu is the first to offer a complete family of 68-pin products including Flash EPROMs, Mask ROMs, EPROMs, and OTPROMs. As well as a full line of connectors, card drives, and interface chips.

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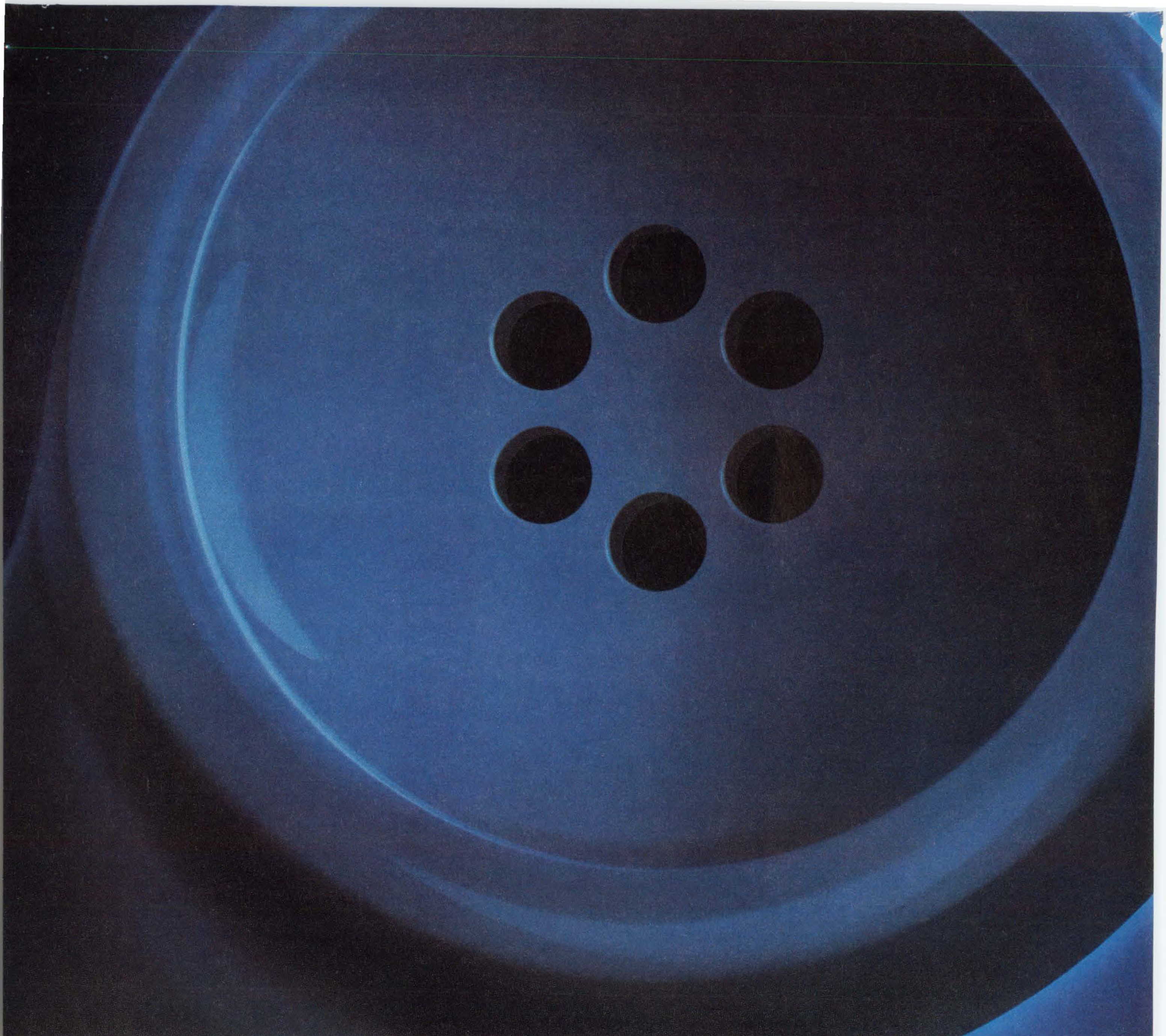
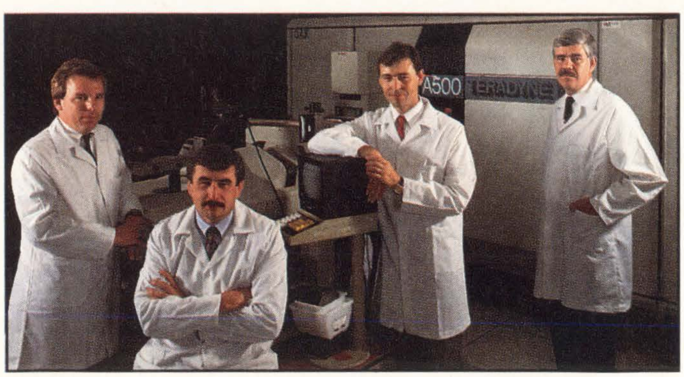


How Teradyne helps Northern Telecom



John Haydon, Ken Bradley, Gary Hobin, Terry Caves of Northern Telecom Electronics, Ottawa.

"To us, time is a strategic tool, a way of getting the edge it takes to gain a leadership role in world markets. With Teradyne testers, test development and manufacturing setup times are shorter, and actual test performance is far superior."

KEN BRADLEY, General Manager

Northern Telecom believes a quality message begins with a commitment: to deliver the highest performance products at the lowest cost – quickly and on time.

That's why Northern Telecom Electronics chose the Teradyne A500 Family of systems to test its most advanced mixed-signal chips. Pushing the performance envelope can be risky, but Teradyne is helping Northern Telecom avoid the pitfalls.

"Our Norstar key system is extremely silicon intensive. The A500 provided virtually unlimited test capability and reduced test time.

send the world a quality message.

I believe without it, the entire project would not be nearly as successful as it is."

GARY HOBIN, Manager,
Test & Product Engineering

Because the A500 Family's IMAGE™ programming environment permits full tester simulation at off-line workstations, test program development parallels design. That cuts product development times dramatically. And because test data is fed back quickly and early in the process, Northern Telecom engineers can eliminate bottlenecks, enhance manufacturability, and accelerate time-to-market.

"Teradyne helps us meet our high-volume production goals – on time. And they perform beyond our expectations in terms of operating costs; tester maintenance cost is 80% lower than budget – and tester uptime measures in the 98%-plus range."

JOHN HAYDON, Business Unit Manager,
Test Operations

Teradyne's A500 Family testers run reliably, producing the accurate, repeatable results that let Northern Telecom engineers ramp up fast to high-yield, high-volume production. So when a customer needs devices, Northern Telecom Electronics is ready to deliver quantity as well as quality.

"Teradyne's service continues after the sale. It's as if they take our priorities as their own. That's helped us achieve the quality it takes to succeed in such highly competitive markets as the U.S., U.K., Germany, and Japan."

TERRY CAVES, Director of Operations

Teradyne's A500 Family of Test Systems. Helping companies like Northern Telecom send their customers the right message. To see how we can help you, call Beth Sulak at (617) 422-2746. Or write today to:
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CIRCLE NO. 32

Introducing a revolutionary new idea in a 1000-watt, "shoe box" power supply.

It's TODD SUPERMAX 1000, an extraordinary OEM power supply of revolutionary proportions. *And those proportions are small.* Smaller than anything in its class. At just 3.38″H × 8″W × 12″L, its compact size allows for great flexibility in a system's mechanical design. In fact, three SUPERMAX 1000 units can be mounted where two standard shoe box units fit before.

SUPERMAX 1000 is the 1000-watt power supply designed right from scratch with Power Factor Correction built in for maximum performance and economy.

Long recognized as the leading innovator in the power supply industry, TODD now brings its advanced open frame switching power supply technology to the high-power shoe box world. SUPERMAX 1000 requires fewer components, so reliability, efficiency—even "no-fan" cooling—are greatly enhanced.

For a smaller, more reliable, lower cost 1000-watt power supply that meets every US and international requirement, evaluate the TODD SUPERMAX 1000. When it comes to quality and innovation, no one can fill our shoes.

To receive a catalog showing our broad line of switching power supplies, for an evaluation unit, or to speak with an engineer who can supply immediate response and immediate solutions to your power supply problems, call the TODD Power-Phone:

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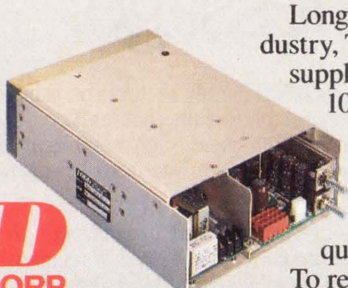

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Circle #16 for product info

Circle #17 for evaluation unit

SIGNALS & NOISE

Company increasing, not ceasing, LED production

In the September 2, 1991, Ask EDN, EDN stated that Rohm is phasing out its LED product lines. This statement is completely false; the reality is quite the opposite.

Rohm has no plans whatsoever to curtail the availability of its LED product offerings. There has been an international, industry-wide increase in demand for LED lamps for the past 12 months, and Rohm has made significant progress to comply with this demand, both for existing and prospective customers.

Other manufacturers may choose to discontinue LED products, but Rohm has exhibited an increased commitment to fulfilling customer requirements in this important product line.

Ray Ponkey, Product Manager, Optoelectronics
Rohm Corp
Antioch, TN

Government's role doesn't end with defense

I must take exception to the last statement by L Alan Kudravy (EDN, March 1, 1991, pg 27) where he asserts that the only obligation of the government is to provide defense. I fear this is a common perception, especially among us defense contractors. However, the Constitution spells out federal obligations in its preamble:

"WE THE PEOPLE of the United States, in order to form a more perfect Union, establish Justice, insure domestic Tranquility, provide for the common Defence, promote the general Welfare, and secure the Blessings of Liberty to ourselves and our Posterity, do ordain and establish this Constitution for the United States of America."

You can see for yourself the numerous obligations listed, including "Defence." Many additional powers and obligations are spelled out in ARTICLE I, SECTION B. These facts are more than 200 years old, and I think we'd all do better to become more familiar with them.

David Telford
Abilene, TX

Updated phone number

An outdated phone number for Circuit Search, Breslau, Ontario, was inadvertently published in the Product Showcase CAE Section (EDN, July 18, 1991, pg 126). The new number is (519) 241-1252.

Mea culpa

EDN made a typo in the Innovation writeup of the Gates Energy Products Genesis battery (EDN, August 5, 1991, pg 68). Readers can call (904) 462-3911 for more information.

Also, we inadvertently printed the fax number instead of the phone number in the Benchmarq Innovation writeups (pg 52). Readers should contact the company at (214) 407-0011, which is the correct phone number.

Correction

In the fourth line down, first column, (EDN, July 18, 1991, pg 92) the package name should read SO-8 packages, not TO-8 packages. General Semiconductor Industries Inc of Tempe, AZ, manufactures the SO-8 packages.

HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158, or leave a note via MCI mail at EDNBOS. Or use EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/SOAPBOX, then W to write us a letter. You'll need a 2400-bps or less modem and a communications program set for 8,N,1.

News Flash

SPORTS

The 90 Nanosecond Workout
An Exhaustive Look At High Tech Training Equipment — PAGE 2B

SCIENCE AND TECHNOLOGY

Virtual Reality
Close But No Cigar — PAGE 8H

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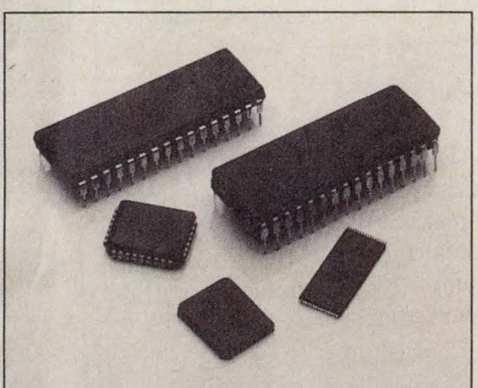
AMD Ships 2
PLCC Flash



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash — hence the name.

Standard, But With A Little More Flash

AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Meeting

Vice Pr
At L

From AMD.

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the *de facto* industry standard.

Our standards, however, are a bit higher. And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323.** And start making some headlines of your own.

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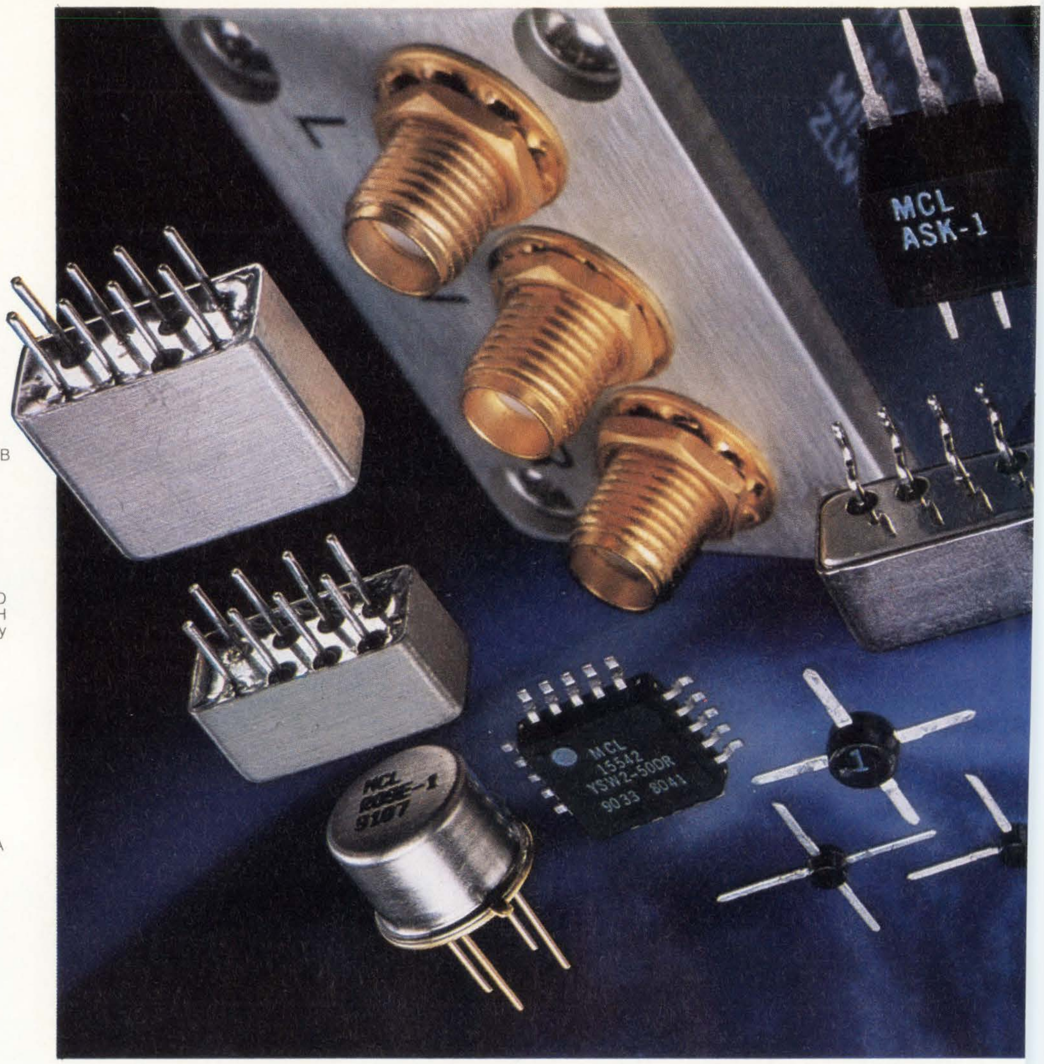

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We wholeheartedly encourage you to place your orders with your local distributor. But let's be realistic. Although our distributors stock our products, not every distributor will carry every single catalog item, especially in substantial quantities. In such instances, when the need for components is urgent, contact a Mini-Circuits' Distribution Center listed and you will be covered by our shipment guarantee.

F144 REV. A

CIRCLE NO. 36

F144 REV. A

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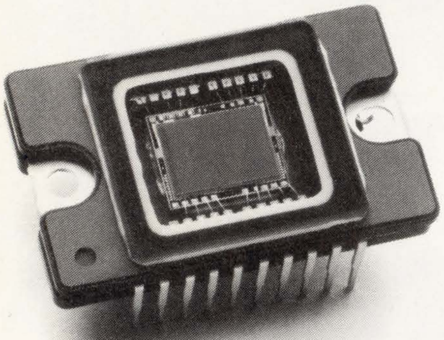

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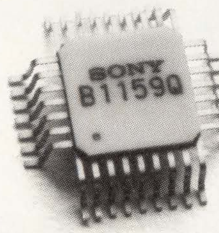

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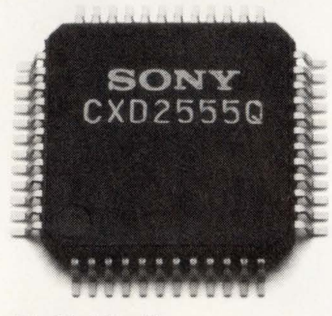

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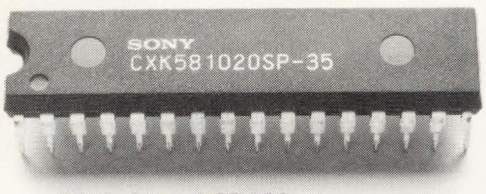

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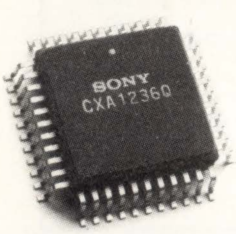

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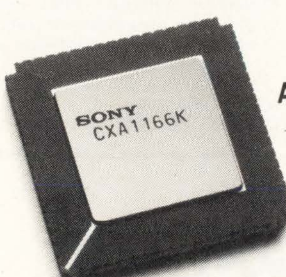

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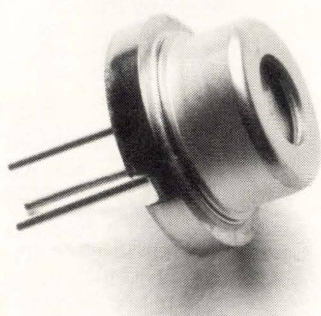

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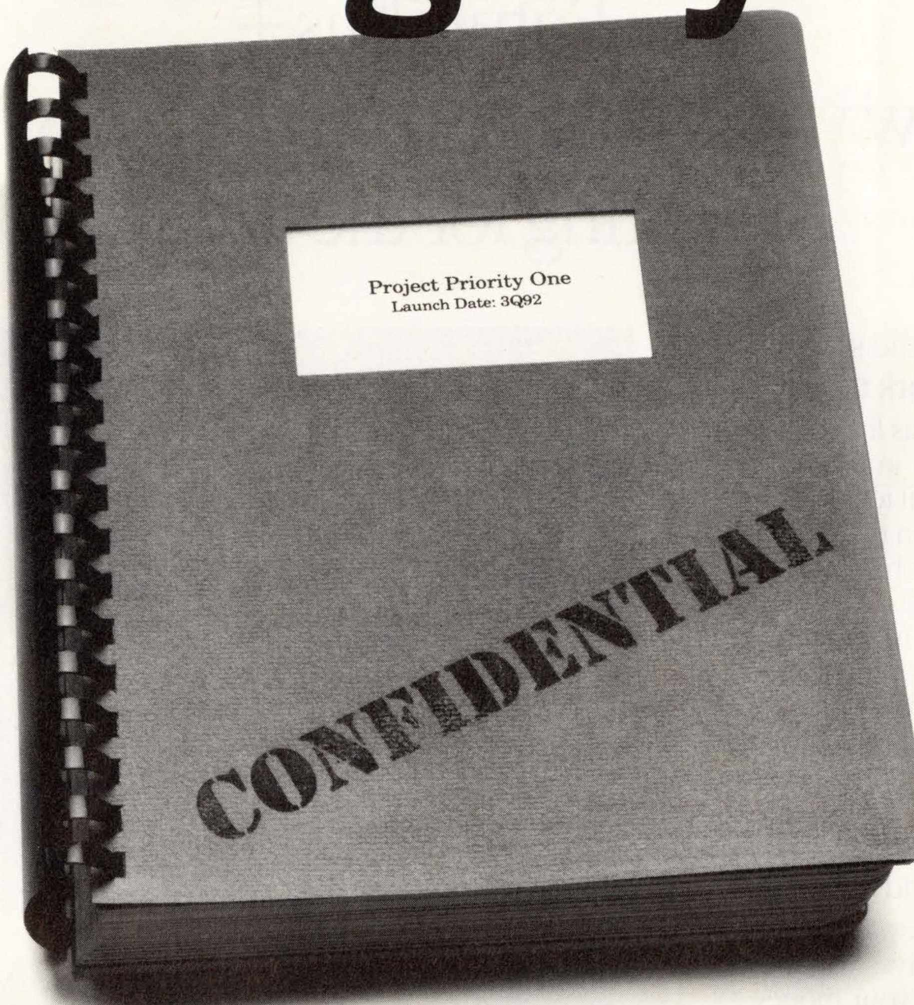

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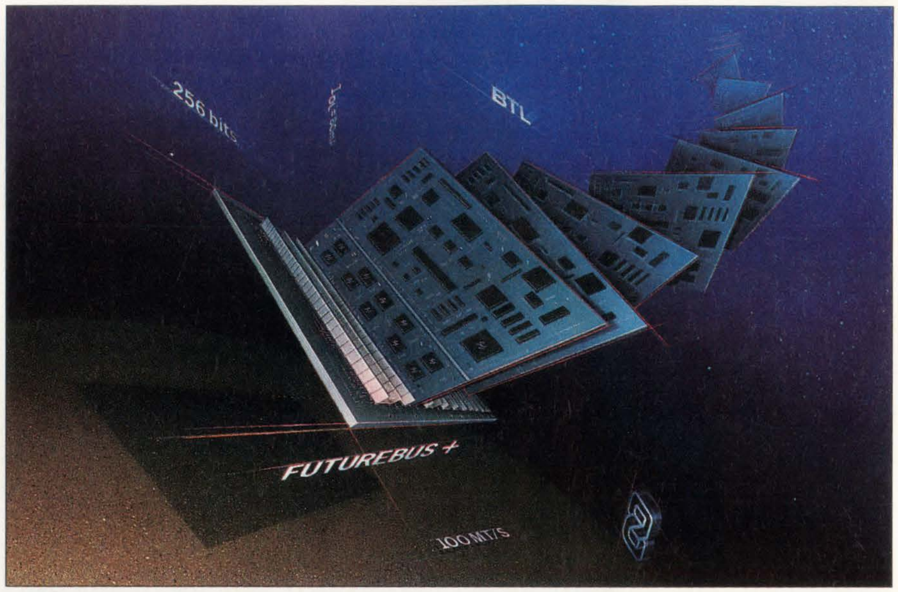

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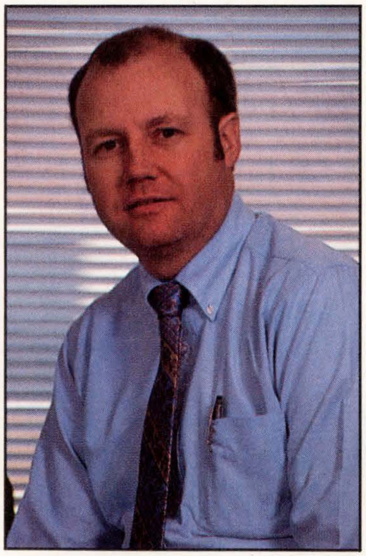
EDITORIAL

CDI technology: It's ready now



During a trip to the Midwest last week, I stopped by Microware (Des Moines, IA) to talk with the people there about their work on real-time operating systems and to learn more about the company's efforts in compact-disk interactive (CDI) products. Unlike audio compact disks, interactive disks also store images that you can display on a television screen. But, more important, CDI programs give you the opportunity to control what happens on the screen.

CDI products will go far beyond entertainment. In fact, the biggest promise for CDI products is in education and information. For example, I saw a Sesame Street disk that lets children select activities such as counting, saying alphabet letters, and matching colors. Even though the starting point of the CDI program looks the same each time you start the disk, the letters, numbers, and colors start at random each time you run through an activity. Thus, the potential for boring youngsters is low.

Another CDI program puts an interactive photography course on your TV. In the sample lesson I tried, I learned how to shoot pictures by candlelight. I pointed the light meter—a pointer on the TV screen—at various places on the TV image and then "shot" the photograph. The CDI program showed me what the resulting photograph would look like, and it let me reshoot the picture until I learned how to take light readings properly for low-light photographs. I could take as many photographs as I wanted.

That's the great potential for CDI technology—interactive products that let students "play" with information. You can structure lessons and complete courses around CDI products so that students can see what happens when they try different approaches to solving problems. It won't be long before we find engineering students trying different circuits and playing "what-if" games with complex formulas on CDI systems. Sure, many computer-based programs can do similar things, but compared with CDI programs, they're inflexible, slow, and difficult to learn to use.

CDI players cost about $1000 and disks cost upwards of $20 each, so the technology won't appeal to everyone—at least not right away. However, when you compare the cost of a CDI player and a set of disks with the cost of a technical college course, CDI is competitive now. It won't be too long before the costs of CDI equipment and disks come down, and soon creative and enterprising people will start developing many of the technical "what-if" courses that go on CDI disks. There are many opportunities here, and CDI technology could be the next killer application the electronics industry has been waiting for.

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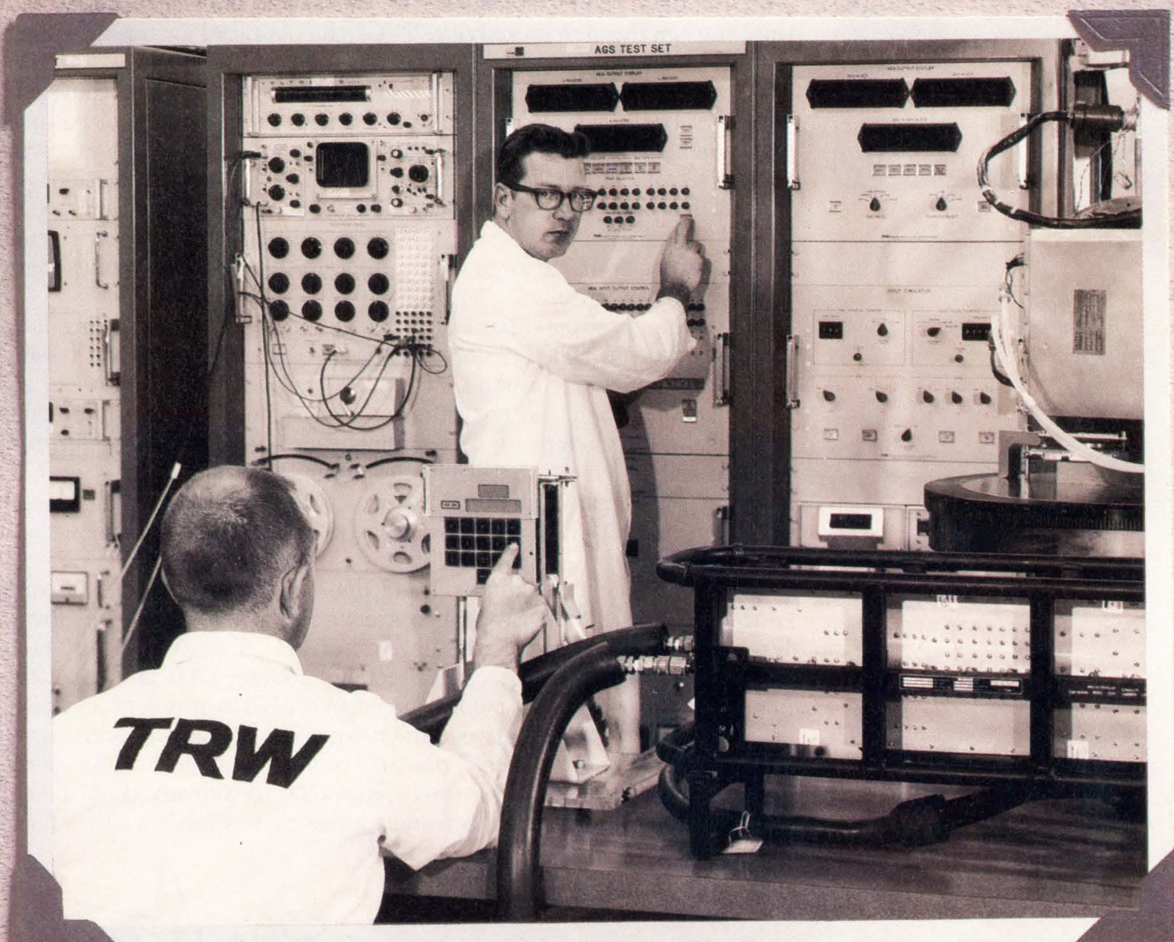

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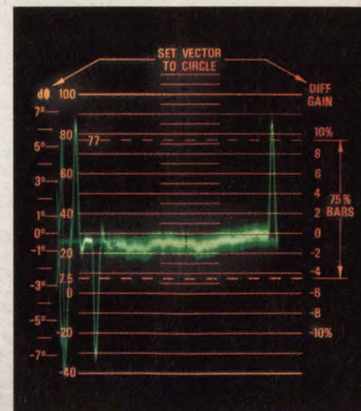

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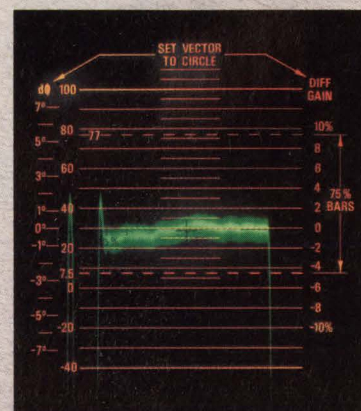

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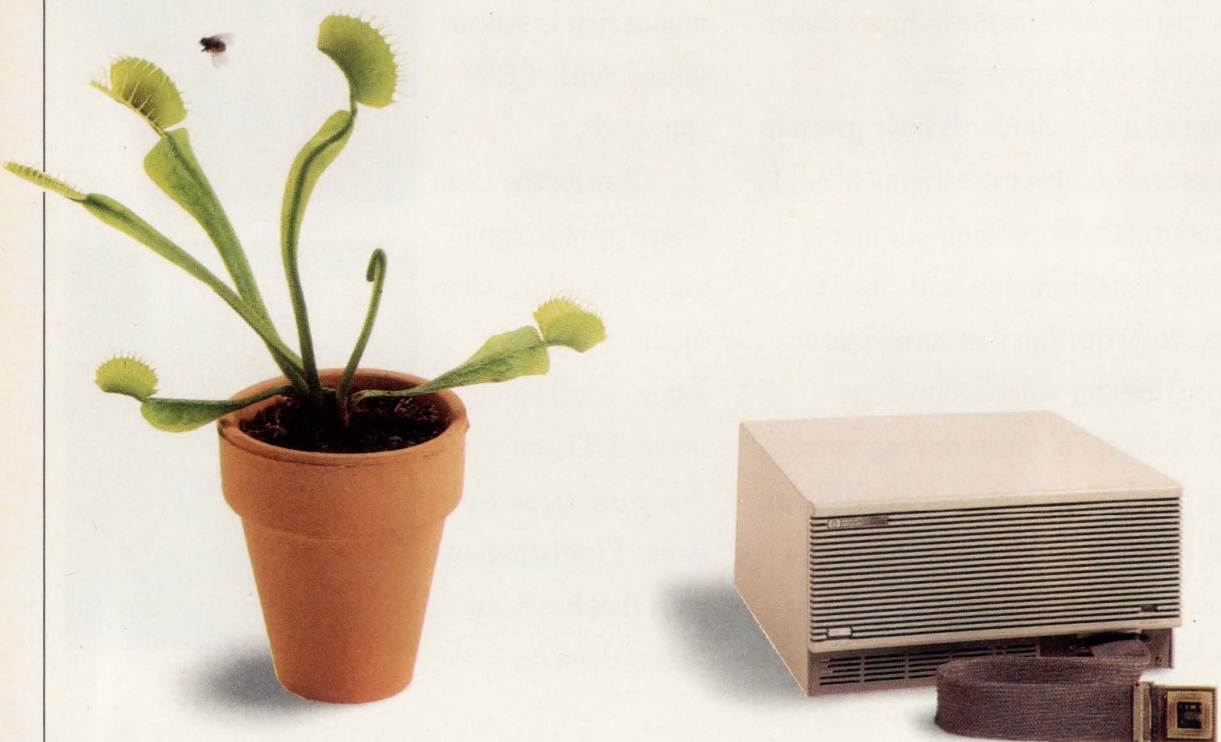

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HEWLETT PACKARD

Smart cards gear up for belated success

Computer chips packaged as credit cards have not become, as once predicted, a ubiquitous medium for electronic money. But, finally, smart cards are finding new applications and wider acceptance.

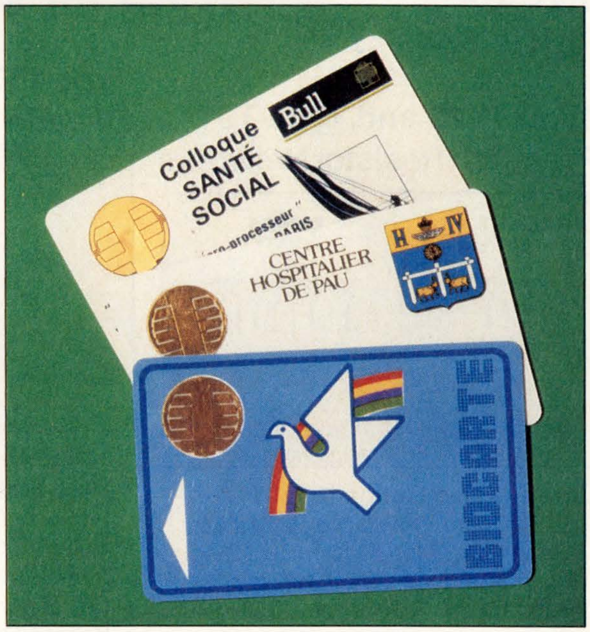
Gary Legg,
Senior Editor

Inquiring minds might want to know why smart cards, if they're so smart, haven't been more successful. Only a few years ago, the credit card containing a computer chip seemed destined to affect the daily lives of practically everyone in the industrialized world. The predicted proliferation of smart cards in financial applications never materialized, however, and other applications have been slow to develop. Only in Europe, where government monopolies and subsidies have encouraged or mandated smart-card use in communications and banking, have smart cards found any kind of widespread use.

There are signs, however, that smart cards might finally be nearing a critical mass of viability for new applications. Over the last few years, evolving standards have contributed to a gradually growing infrastructure of smart-card applications and equipment. At the same time, advances in semiconductor-manufacturing technology have lowered smart cards' prices. More important, application developers have learned to target areas where cheaper magnetic-stripe cards can't compete.

Ironically, the smart card's lofty potential may have been the biggest detriment to its early success. Because smart cards are relatively cheap and are ideal for numerous applications, it was easy to overlook some basic factors that worked against them. One factor, paradoxically, was cost. At less than a dollar, a simple (memory-only) smart card seems cheap. However, compared to 20 cents for a magnetic-stripe card, the smart card is very expensive. Never mind that the smart card can do so much more; the magnetic-stripe card already did what customers wanted. Magnetic-stripe cards also had a large installed base of card terminals and development equipment; smart cards had none at all.

But smart cards have, nevertheless, made notable progress. The biggest success story so far involves a memory-only card, which some people don't consider to be a smart card (see **box**, "What is—or isn't—a smart card?"). Some 50 million or more credit-card-sized memory cards, most containing only a small amount of EPROM, were sold last year in France alone, mainly for use as prepaid telephone cards. Phone cards are



Applications of smart cards in Europe have far outpaced applications elsewhere. *The initial impetus came from governments that encouraged or mandated use in telecommunications and banking. (Photo courtesy Motorola)*

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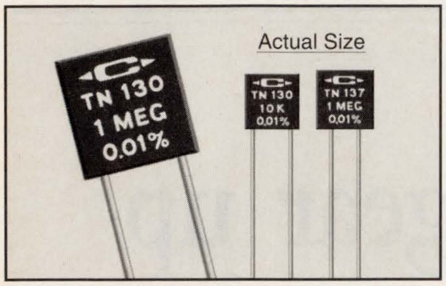

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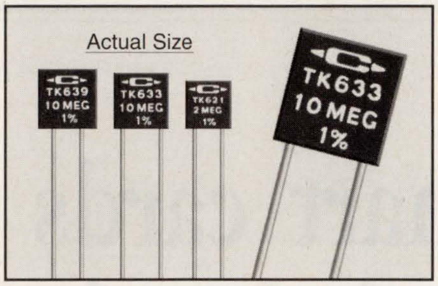

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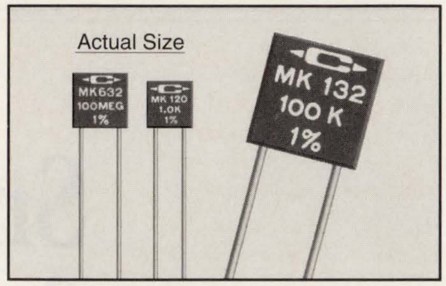

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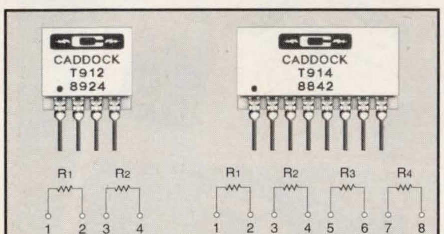

T912 Schematic 1:1, 9:1 or 10:1

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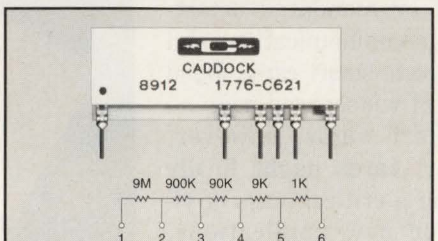

1776-C621 Schematic

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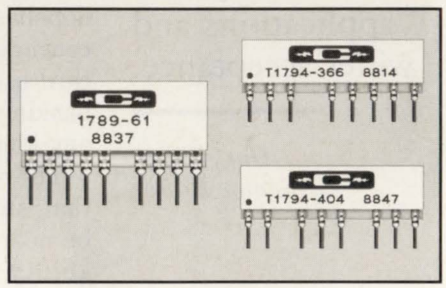

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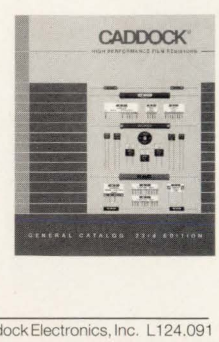

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in use in other European countries, too, but France has the highest volume of cards in use because of its early involvement with smart cards.

A telephone smart card comes "charged" with a certain monetary value; as a customer uses a card for pay-phone services, the telephone's card terminal subtracts a monetary value by altering EPROM cells. When the card's monetary value reaches zero, the customer has to buy another card. Each card costs the French phone company (a government-supported monopoly) about a dollar. However, the company recovers most of the cost by selling advertising space on the back of the card.

Other smart-card applications won't match the high-volume usage of phone cards anytime soon, but some markets seem to have good potential (see **box**, "What smart cards are doing"). Memory cards are finding use as portable data carriers and as "electronic purses;" cards with microcontrollers find use in applications requiring tight security, such as controlling access to buildings, computers, or funds.

Security, in fact, is high-end smart cards' best selling point. Motorola claims "zero break-ins" of 25 million cards produced with its chips, and SGS-Thomson last year introduced the ST16 family of smart-card microcontrollers with security features not previously available. The ST16 chips guard against hacking techniques ranging from the downloading of memory-dump routines to physically opening the chip.

For example, to prevent someone from downloading a memory-dump routine into RAM or EEPROM and then running the routine, a customer-defined access matrix (implemented at the time of chip manufacture and thereafter unalterable) determines whether an instruction executed in one memory area can access data in another. The ST16 device performs the access check on every instruction fetch.

Several sensors in an ST16 chip guard against other security breaches. A clock-frequency sensor, for example, detects attempts to operate the device at any frequency below 250 kHz, thus foiling attempts to analyze operation by single stepping. Other sensors detect the presence of light, indicating that someone has physically altered the chip.

Another security feature involves scrambling the chip's supply current. Otherwise, someone could conceivably observe the current during read cycles and gain information about the number of bits set or cleared in a particular ROM or EEPROM byte. ST16 devices even make it difficult to read ROM contents should someone go to the extreme of chemically removing the chip passivation layer and examining the mask layer with a microscope. At the time of manufacture, SGS-Thomson creates a 512-bit matrix that scrambles physical and logical ROM addresses.

In Motorola's 68HC05-based smart-card chips, memory contents are accessible only from application software in on-chip mask ROM; once customer software has been manufactured in ROM, fusible links can be blown to prohibit any future ROM access except via processor instruction fetches. And, like other manufacturers, Motorola points to the ability of a single-chip microcontroller to run encryption and decryption algorithms that reside in internal ROM. On-chip encryption

What is—or isn't—a smart card?

By some definitions, a smart card must have onboard intelligence in the form of a microcontroller. By other accounts, a card containing any form of electronics is a smart card.

The disagreement stems from the semiconductor manufacturers who supply the chips that go into cards. Motorola, long noted for its microcontroller prowess, insists that only a card with a microcontroller has intelligence, and is therefore "smart." SGS-Thomson, the leading supplier of memory-only cards, makes no such distinction, lumping memory cards and controller cards together. A spokesperson for Catalyst Semiconductor concurs, claiming that "a card that can remember information is smart, right?" Hitachi says its memory-only cards are smart, and its cards with microcontrollers are "super smart."

There's even disagreement about the physical configuration of smart cards. Credit-card-sized memory modules for computers **(Ref 1)** sometimes get dubbed as smart cards, even though they have 68 pins on one end rather than eight contacts on the side as recommended by the ISO smart-card standard. Some people even say a smart card can take forms completely different from that of the standard-sized credit card. Electronic keys, buttons, and dog tags, for example, would qualify as smart "cards."

and decryption eliminate the need to transmit unprotected data between a smart card and a card terminal, thus removing a potential security vulnerability.

Indeed, security is only as strong as its weakest link, so chip suppliers concentrate not only on what's in their chips, but on what happens to the chips during and after manufacture. Motorola and SGS-Thomson, for example, track and account for all wafers and use only secure areas for manufacture and test. Both companies even document the destruction of unused wafers and will arrange for secure shipping to customers.

Security requires a controller

Your most sophisticated smart-card applications, and especially those that have strict requirements for security, will need to use a card that contains a microcontroller.

Motorola, with chips based on the familiar 6805 core, sells more controller-based smart-card chips than anyone else, but both SGS-Thomson and Hitachi America note that sales of controller-based chips are looking up. SGS-Thomson claims that the ST16 family, which it introduced early in 1990, sold more than a million chips last year. Hitachi's H8/310, which began shipping in 1987, finally began selling in enough volume that the company "introduced" it as a product in April of this year. The 310 has more mask ROM (10 kbytes) than any other smart-card chip, and ties with Catalyst's CAT62C780 for the most EEPROM (8 kbytes) (**Table 1**).

Table 1—Microcontroller-based smart-card chips

Supplier	Device	RAM (bytes)	ROM (bytes)	EPROM (bytes)	EEPROM (bytes)	Clock rate (ext/int)
Catalyst	CAT62C580	128	3k	N/A	2k	5 MHz/5 MHz
	CAT62C780	192	6k	N/A	8k	5 MHz/5 MHz
Hitachi	H8/310	256	10k	N/A	8k	10 MHz/5 MHz
Motorola	MC6805SC01	36	1600	1k	N/A	4 MHz/1 MHz
	MC6805SC03	52	1904	2k	N/A	4 MHz/1 MHz
	MC68HC05SC11	128	6k	8k	N/A	5 MHz/2.5 MHz
	MC68HC05SC21	128	6k	N/A	3008	5 MHz/2.5 MHz
SGS-Thomson	ST1821	44	2k	1k	N/A	333 kHz/333 kHz
	ST1834	76	3k	4k	N/A	333 kHz/333 kHz
	ST16301	128	3k	N/A	1k	5 MHz/5 MHz
	ST16612	160	6k	N/A	2k	5 MHz/5 MHz
	ST16623	224	6k	N/A	3k	5 MHz/5 MHz

Note: N/A = Not applicable.

Even the simplest EPROM-based smart cards offer security features that magnetic-stripe cards don't. SGS-Thomson's ST1200 256×1-bit EPROM chip, for example, has a polysilicon fuse that protects 96 bits of memory from write operations. A smart-card developer can program application-specific in-

What smart cards are doing

Smart cards are succeeding mostly in new application areas, where they offer convenience and value without running up against entrenched competition. Perhaps the most widespread use is as an "electronic purse."

An electronic purse (an EPROM- or EEPROM-based card) holds electronic money that you buy with real money. You spend the electronic money by using the card in some sort of terminal. The prepaid telephone card is an electronic purse of sorts, although the money it contains can be spent in only one way—on phone calls. A racetrack in Ohio uses the same idea for a prepaid betting card, and certain ski resorts in Austria and Switzerland let you use a prepaid card for any expenses you incur during your stay.

Some European hotels take the concept further, using an EEPROM-based card to store transaction records while tracking your expenses. You can use the card for any hotel expenses, including purchases at restaurants and gift shops; at checkout, you plug your card into a reader and get an itemized bill. In the US, smart-card companies are targeting universities for a similar application. The goal is to give each student a personal EEPROM-based smart card that can be used for identification, tuition and fees, on-campus purchases, and even access to dormitories and labs.

Optical-disk technology is going into cards, too. At West London Hospital, British Telecomm is conducting a pilot program in which each obstetric patient's medical record is stored on a card. Each card, from Drexler Technology Corp (Mountain View, CA), holds 2.8 Mbytes of data, or about 1000 pages of typed text.

Smart cards

formation in the 96 bits and then blow the fuse to prevent code or data modifications by unscrupulous parties. The ST1301A 416×1-bit EEPROM chip takes memory-card security a step further. It contains logic circuitry that verifies a personal identification number (PIN) and "locks" the card if someone presents four consecutive PINs that don't match the one stored in the card.

You do pay for security, though. A typical magnetic-stripe card costs between $0.17 and $0.25; the cost of a smart card can range from less than a dollar for an EPROM card to ten dollars or more for a card containing a microcontroller. Prices vary widely with the quantity purchased.

For EEPROM, you have more options. In addition to the previously mentioned 416-bit ST1301A from SGS-Thomson, you can also get 2-kbit (256×8-bit) chips from Motorola and 4-kbit (512×8-bit or 256×16-bit) chips from Catalyst Semiconductor. Note that chips for smart cards have serial data access; smart cards' limited number of contacts precludes parallel transfers.

Acronyms used in this article

EEPROM—Electrically erasable programmable ROM
EPROM—Erasable programmable ROM
ISO—International Standards Organization
PIN—Personal identification number
RAM—Random access memory
ROM—Read only memory

Start with the chip makers

If you're interested in developing a smart-card application, perhaps the best way to start is by contacting the semiconductor manufacturers that produce the cards' electronics. These companies can give you information about their devices' operation and about available development systems. You may, in fact, want to choose a smart-card vendor based on that vendor's semiconductor supplier, especially if you want a microcontroller-based card and have a particular controller in mind.

The semiconductor companies can, in turn, put you in touch with companies that make the actual smart cards and supporting equipment, such as card readers. The US has a handful of smart-card companies, and Europe has scores, perhaps a hundred or more. Little information about smart cards comes out of Japan, although sources in the US and Europe say there is a lot of Japanese smart-card activity. Hitachi America has recently been pushing its smart-card chips, and Oki Semiconductor has long been the supplier of smart-card chips for California-based Catalyst Semiconductor.

Smart-card devices usually come in wafers or in micromodules with the bond-out pattern specified by ISO standard 7816. Manufacturers' delivery can take anywhere from 8 to 16 weeks after you provide the ROM-based application code. And bear in mind that getting the chip is only the first step for most application developers; in most cases, you'll want a second company to put the chips in cards. Also, some chips may just be approaching volume production, so you should be wary of delays. A spokesperson for Motorola's smart-card operation suggests verifying that a device is already in volume production before placing an order.

Development systems for smart-card chips are available from the

For more information . . .

For more information on the smart-card products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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semiconductor manufacturers; development occurs much as it would for any microcontroller-based application except for the differences resulting from the limit of six pins per chip. (ISO specifies eight contacts, but two are reserved for future use.) Some special equipment is available, both from semiconductor manufacturers and card manufacturers, for use after the chips are in cards.

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Near-term enhancements to smart cards probably will not be dramatic. Eight-bit processors appear to be adequate for now, although memory capacity—both in controller-based cards and memory-only cards—will undoubtedly increase. Flash memory, occupying less space than conventional EEPROM, will allow die sizes to remain small and keep the chips from breaking as the cards flex.

In the longer term, perhaps five years, more significant changes will occur. Until then, however, smart-card applications of existing products will need to prove as successful as glowing forecasts once predicted.

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Reference

1. Small, Charles H, "Small memories take on wider applications," *EDN*, June 20, 1991, pg 67.

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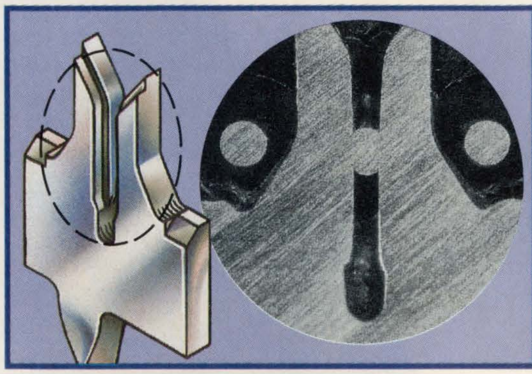

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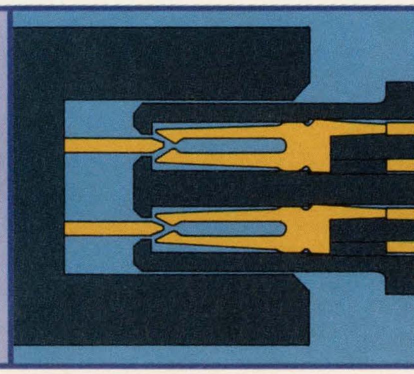

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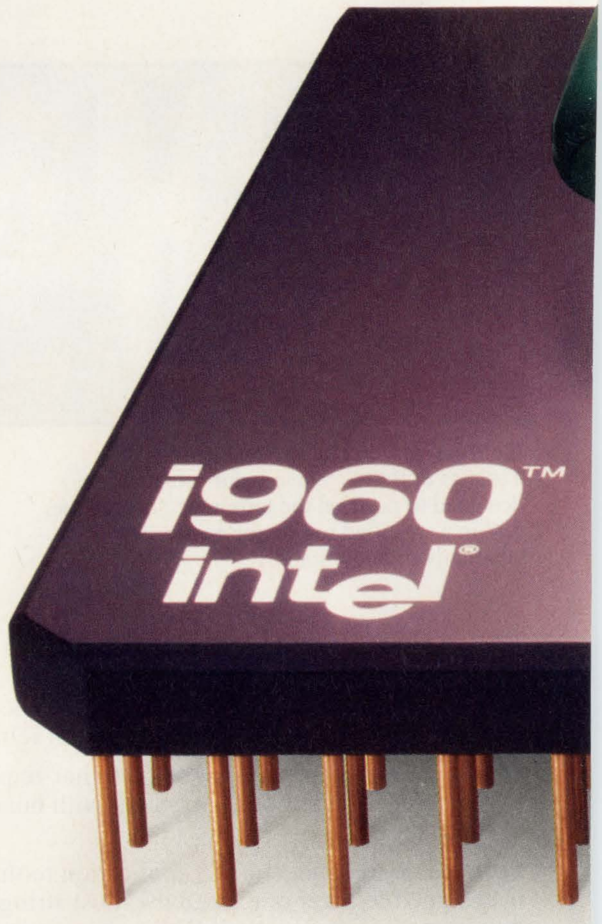

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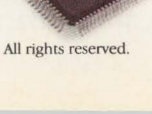

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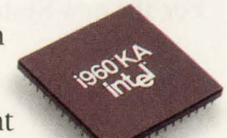

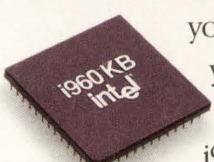

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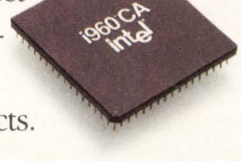

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CIRCLE NO. 46

VIDEO-COMPRESSION CHIPS

Monolithic circuits expedite desktop video

Dedicated ICs can ease the burden of implementing existing and emerging image-compression standards for video systems.

Dave Pryce,
Associate Editor

Although advances in processing speed, memory density, and mass-storage capacities have made the desktop computer a viable platform for video applications, these advances don't provide the power and capacity to handle the enormous amounts of data in video images. The person that said "a picture is worth a thousand words" would probably have said "a few million words," given knowledge of today's computer-based image demands. For desktop computers to deal with the millions—actually billions of bytes—they need some help from video-compression chips.

A *single* 24-bit color image with a resolution of 1024×768 pixels consumes about 2.3 Mbytes of storage. The capacity problem worsens if your application requires storing 15 minutes of such images in full-motion video running at 30 frames/sec. Such applications boost storage requirements to about 60 Gbytes. If you've got two-hundred 300-Mbyte drives lying around, you're home free. If not, you're in serious trouble.

Transferring such images is an equally daunting problem. A fast hard disk transfers about 1 Mbyte/sec, and an Ethernet LAN is typically even slower. Forget about modem transfer, you might not live long enough to receive the transmission.

Storing and transmitting video information—particularly full-color, full-motion images—has inherent limitations. Recognizing these limitations,

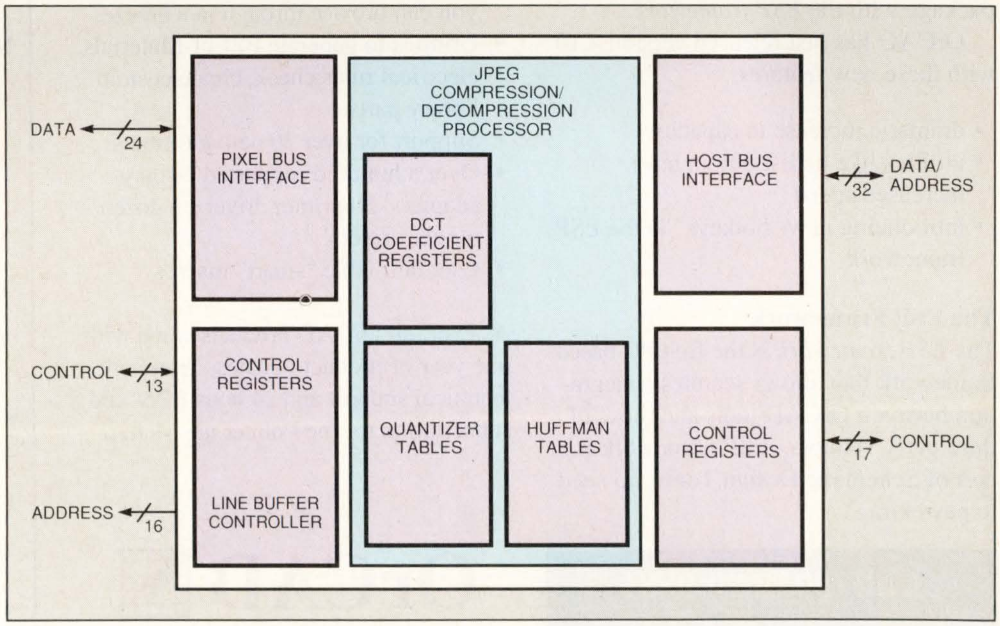


Fig 1—Shown here in block-diagram form, *the CL550 JPEG chip from C-Cube Microsystems can handle compression ratios from 8:1 to 100:1. The chip supports 8-bit gray-scale, RGB, CMYK, and YUV color-space representations.*

Video-compression chips

several vendors of integrated circuits have recently introduced dedicated ICs (**Table 1**) that can compress video data by factors ranging from about 15:1 to well over 250:1, depending on the application. These devices incorporate special circuit architectures and use algorithms tailored to the intended application.

Most of these compression chips use the discrete cosine transform (DCT), an algorithm that has become popular for image coding. Although most use the same algorithm, different image-compression chips are targeted for specific applications and fall under different standards generated by the International Standards Organization (ISO) or the International Consultative Committee for Telephony and Telegraph (CCITT).

The ISO has its Joint Photographic Experts Group (JPEG) and Motion Picture Experts Group (MPEG) standards. The JPEG standard primarily applies to still images and supports compression ratios to about 25:1 without any visible degradation in image quality. The MPEG standard applies to full-motion video and achieves compression ratios of 50:1 or more. The CCITT has its Px64 standard, which applies to full-motion video and to real-time video applications such as teleconferencing. Systems using the Px64 standard achieve typical compression ratios of 200:1 to 500:1. **Table 2** summarizes the standards in use for various applications and the features they offer. For a more complete discussion of these standards, see the **box,** "Video compression techniques and standards." For a more in-depth treatment of compression and decompression approaches, see **Ref 1.**

Table 2—Image-compression standards

Feature	JPEG	Px64	MPEG I	MPEG II
Full color still images	✓	✓	✓	✓
Full-motion video		✓	✓	✓
Real-time video capture/playback	✓	✓		
Broadcast-quality full-motion				✓
Compression ratios	10:1 to 80:1	100:1 to 2000:1	up to 200:1	up to 100:1
Bandwidth		64 kbps to 2 Mbps	1.5 Mbps	5 to 10 Mbps

Table 1—Representative video-compression chips

Company	Part no.	Standard	Speed rating	Package(s) available	Price (qty)
C-Cube Microsystems	CL550	JPEG	10, 30, or 35 MHz	144-pin PGA[1] 144-pin quad flatpack	\$95 to \$165 (10,000)
Integrated Information Technology	VP	JPEG MPEG Px64	N/S	144-pin quad flatpack	\$150 (10,000)
Intel Corp	i750 (2-chip set): 82750PB 82750DB	—	25 MHz 28 MHz	132-pin quad flatpacks	\$39 \$46 (10,000)
LSI Logic	3-chip set: L64735, L64745, L64765	JPEG	20 or 27 MHz	68- and 84-pin PGA 100-pin quad flatpack	\$220 to \$287 (1000) (set) \$149 (10,000) (set)
SGS-Thomson	STV3200	JPEG MPEG	N/S	40-pin DIP 44-pin PLCC[2]	\$91
	STV3208	JPEG MPEG		40-pin DIP	\$52
	STI3220	MPEG Px64		68-pin PLCC 68-pin CLCC[3]	\$78 \$140 (1000)

Note: 1. PGA=pin-grid array
2. PLCC=plastic leaded chip carrier
3. CLCC=ceramic leadless chip carrier
N/S=Not specified

JPEG chips are popular

The first monolithic image-compression processor based on the JPEG standard, the CL550 from C-Cube Microsystems, received almost instant acceptance by satisfying video systems manufacturers' needs. The CL550 speeds overall performance, reduces storage requirements, and minimizes transmission times. The device can shrink high-resolution, full-color images by a 25:1 ratio. But it can handle compression ratios from 8:1 to 100:1, depending on the application's quality, storage, and bandwidth requirements. Compression ratios are controlled by on-chip quantization tables. The device also works in the reverse mode to decompress images.

The CL550 (**Fig 1**) has on-chip video- and host-bus interfaces. The video (pixel) interface supports 8-bit gray scale, RGB (red, green, blue), CMYK (cyan, magenta, yellow, black), and YUV (luminance, chrominance) color-space representations. In the compression mode, the device takes pixels from the pixel bus, compresses them, and makes the compressed data available on the host bus. In the decompression mode, the device acquires host-bus compressed data, decodes it, and makes pixel data available on the pixel bus.

Video-compression techniques and standards

Most video compression techniques use a set of four basic processing functions: spatial-to-frequency domain translation, quantization, entropy (Huffman) coding, and motion compensation.

Spatial-to-frequency translation converts the red, green, and blue (RGB) pixels into YUV form, where Y represents an intensity value, and U and V represent color values. A discrete cosine transform (DCT) then converts the block of YUV pixels into a set of coefficients that represent the frequency components of the intensities and colors in the block. The DCT outputs a 2-D matrix that can be inversely transformed back into pixel values.

Quantization—a lossy, approximation function that is similar to division—compresses the overall range of the frequency matrix. For example, a data set comprised of integers from 0 to 255 needs 256 discrete values (8-bit numbers) to represent it. By dividing each value by 8, it's possible to represent the entire set using only 32 values, albeit with some loss of definition. Varying the quantization applied to the DCT-generated frequency matrix changes the compression ratio—and the quality of the decompressed image. Because human vision is less sensi-

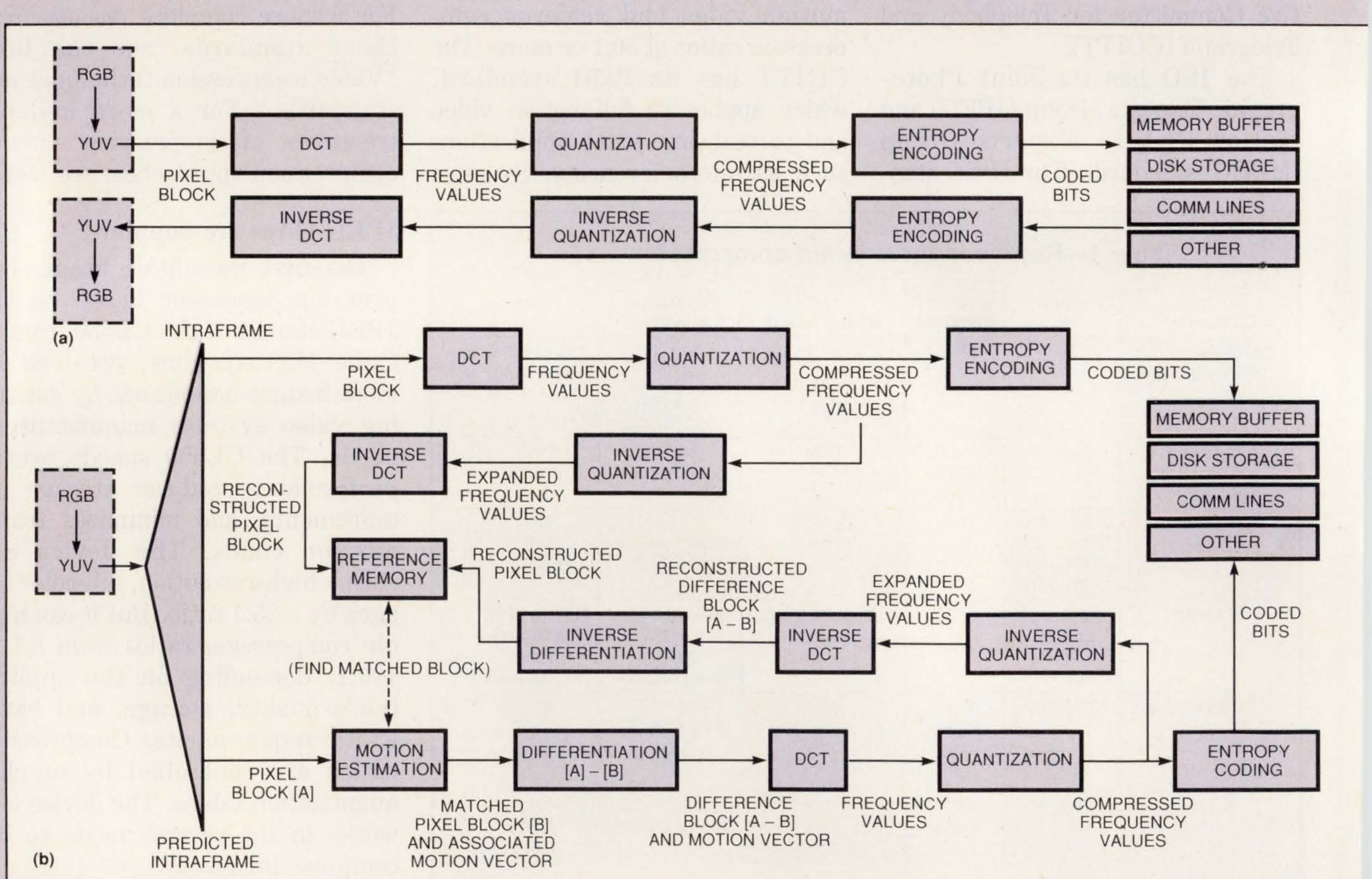


*Fig A—**Three standards currently govern** the compression and decompression of still and full-motion video. The block diagrams show implementations of these standards in increasing order of complexity: JPEG encoding and decoding **(a)**, Px64 encoding **(b)**, and MPEG encoding **(c)**.*

JPEG-standard compression operates on 8×8-pixel blocks. Because many applications work with raster graphics instead of pixel blocks, the CL550 provides address and control for an external line-buffer RAM. The chip can use this RAM to organize raster images into blocks of 8×8 pixels for compression, or to organize 8×8-pixel blocks after decompression into a raster pixel stream.

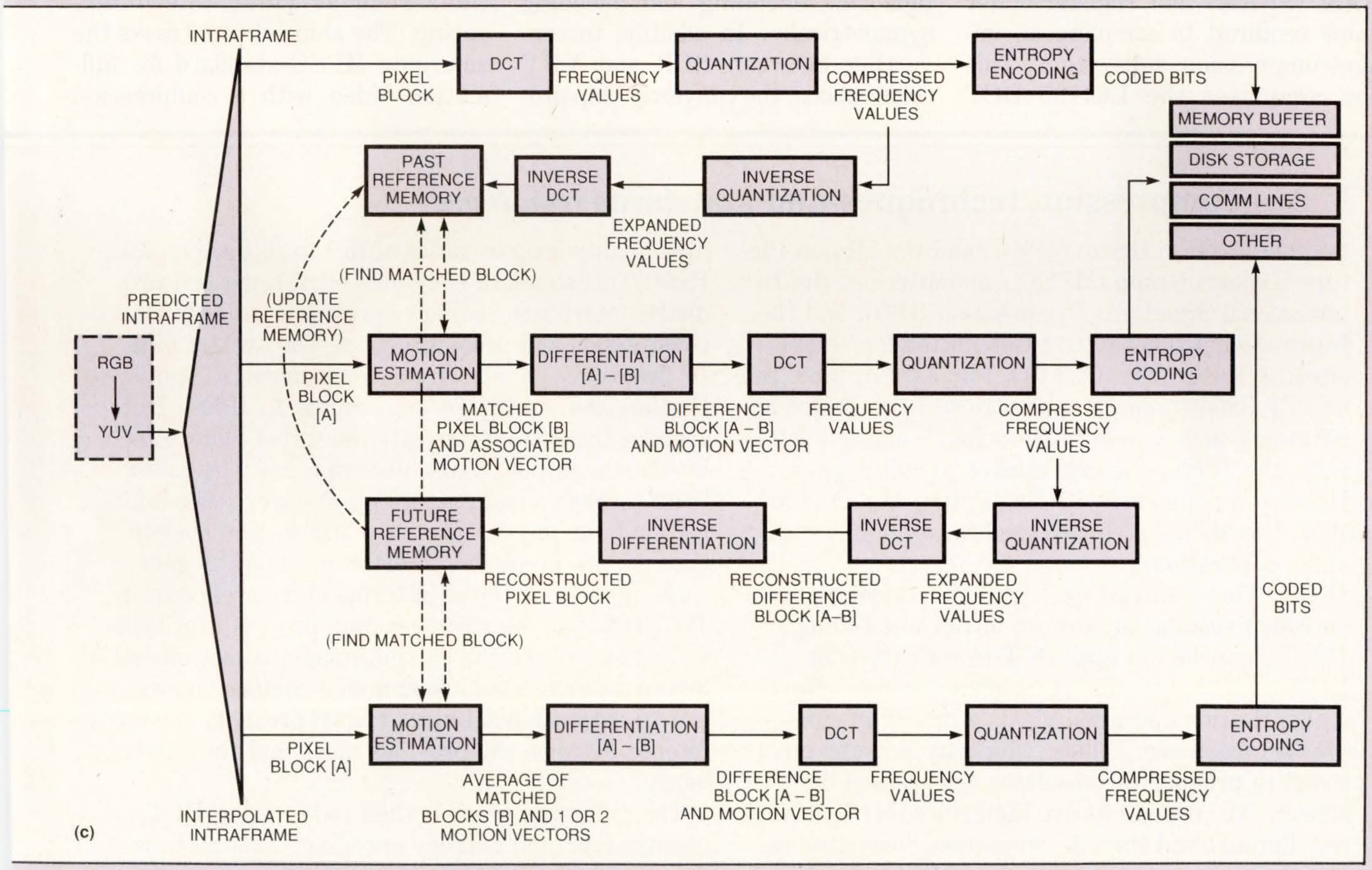
tive to high-frequency details than to low-frequency details, the relative quantization can be greater for high frequencies without sacrificing perceived image quality.

Entropy (Huffman) coding is a variable-length coding technique that assigns bit patterns of varying length to data codes, depending on the statistical occurrence of those codes. Frequently occurring patterns receive short codes; infrequent patterns receive longer codes. For example, because quantized video frequency matrices tend to contain many zeros, the entropy encoding operation generally assigns very short bit strings to represent the various run lengths of zeros.

Motion compensation compares the frame-to-frame variation in a video sequence and attempts to reduce the amount of information needed to describe one frame, given some information about one or more related frames. This process is called *interframe* coding. Initially, however, an *intraframe* (single frame) establishes the reference.

Driving the efforts to establish standardized methods for video compression are the Joint Photo-

Text continued on pg 72



As an example of the increased speed provided by the CL550, it can compress a 30-Mbyte, 24-bit/pixel color image in 1 sec. By comparison, a 68030 microprocessor would take 5 minutes to compress the same image.

Chip sets simplify circuitry

One thing you need to keep in mind when dealing with image-compression systems is that no single chip can provide all of the functions necessary to support JPEG, or any other standard. All compression systems require numerous support chips to accomplish the task. In an effort to reduce the total chip count, LSI Logic offers a 3-chip set that reduces the number of static RAM (SRAM) and register-buffer chips required to complete an image-compression subsystem. This set comprises the L64735 DCT processor, the L64745 JPEG coder, and the L64765 color and raster-block converter. The chip set is targeted for desktop publishing systems, color copiers, laser printers, medical imaging equipment, and other applications that need to compress still-image data.

Although some image-compression chips break down at high speed and low compression ratios, the pipeline architecture of the LSI Logic chip set can continuously code and decode any data stream, regardless of the amount of data or its compression ratio. The DCT processor and the JPEG coder chips perform the cosine transfer, quantization, and variable-length (Huffman) coding functions. The bidirectional chip set performs encoding and decoding symmetrically. In addition to converting between RGB and YUV color spaces, the converter chip provides the control logic to convert pixel data between a raster-ordered signal and a JPEG block-ordered signal. The chip set supports both color and gray-scale images.

The L64745 JPEG coder chip includes a lossless mode as an extension to baseline JPEG. The simpler design of a lossless system requires only the L64745 chip, bypassing quantization and run-code circuitry. The chip codes or decodes data using one of two internally stored code tables. A statistics mode lets the user collect image statistics in a first pass to optimize the Huffman code tables.

LSI Logic also offers a 7-chip set for implementing the CCITT Px64 standard for full-motion applications such as video teleconferencing. The chip set also tracks the emerging MPEG standard for full-motion video with a compression

Video-compression techniques and standards *(continued)*

graphic Experts Group (JPEG) and the Motion Picture Experts Group (MPEG) committees of the International Standards Organization (ISO), and the International Consultative Committee for Telephony and Telegraphy (CCITT). Finalized in 1989, the CCITT Px64 standard applies to real-time video applications such as teleconferencing. Finalized this year, the JPEG standard applies to still images. Under development, with finalization expected in 1992, the MPEG standard applies to full-motion video applications.

JPEG: This standard uses DCT, quantization, and entropy encoding to perform intraframe coding. JPEG compression uses DCT to convert each YUV pixel to a matrix of frequency values. Next, a quantization operation yields a matrix of compressed frequency values, which are entropy encoded to produce the resultant compressed bit stream. The coded bits are then stored, or transmitted digitally and then decompressed through a reverse process, regenerating the pixel image. **Fig A** illustrates the basic process. JPEG coding can achieve compression ratios from 10:1 to 80:1. For high-quality images, ratios of 15:1 to 25:1 are typical.

Px64: This standard combines intraframe and predictive interframe coding to provide on-the-fly video compression and decompression. The system **(Fig B)** first codes an intraframe block using DCT, quantization, and entropy coding, similar to JPEG. However, as the system converts the coded block to a bit-stream output, it also decompresses the coded block through a reverse process and stores the information in an internal memory buffer. The system then applies predictive interframe coding to code each subsequent frame in terms of its predecessor. The predictive interframe-coding process first loads a pixel block from the current image. A motion estimator then executes a search-and-compare operation to output a pixel block that represents the difference between the previous block and the current block.

The difference block is then coded using DCT, quantization, and entropy encoding. This block is output as coded bits, along with an encoding of the associated motion vector needed to reconstruct the original block upon decompression. That block is also bit-stream of 1 Mbps. The set contains an error-correcting codec, a motion-estimation processor, a DCT processor, a quantization processor, a Huffman encoder, a Huffman decoder, and an intra-/inter-frame decision processor. The price of the complete set in plastic packages is under $700 (1000). As a subset of the complete system, the company also offers a 3-chip set for a full-motion video playback system on a computer platform for $250.

Designed for multimedia applications, Intel's i750 2-chip video processor lets you combine text, graphics, and video images in a computer display. The chip set contains the 82750PB, a programmable pixel processor for manipulating image data, and the 82750DB display processor, which handles the video interface. **Fig 2** is a block diagram of a basic system using these two de-

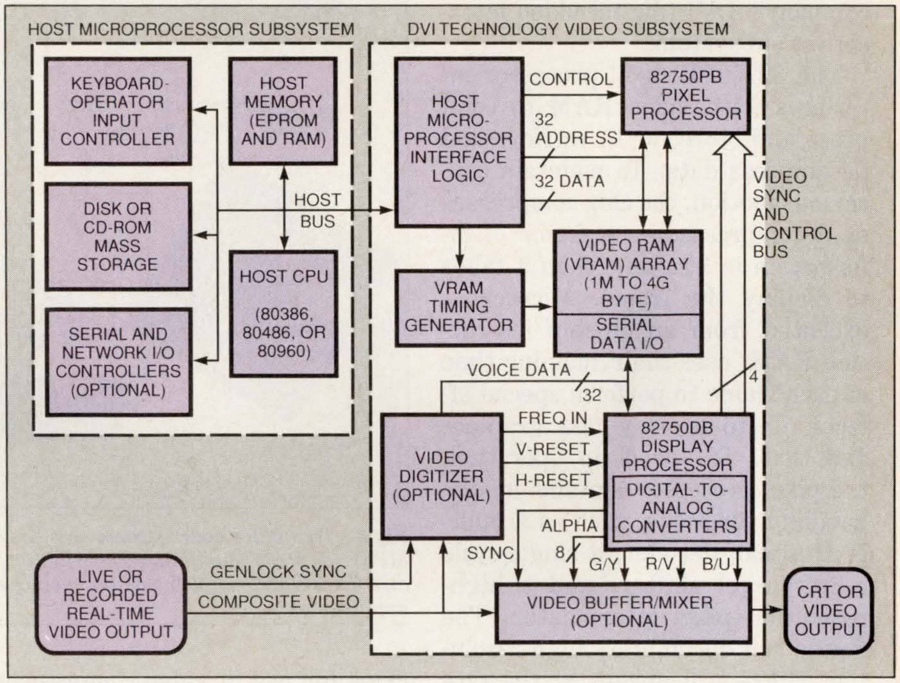


***Fig 2—Providing the basis for a video subsystem,** the 82750PB pixel processor and the 82750DB display processor from Intel interface with other components and the host microprocessor subsystem.*

decompressed internally and stored in the memory buffer as the new reference for the next block. Optimized for video-based telecommunications and other real-time applications that are not motion intensive, the Px64 algorithm incorporates limited motion-search and estimation capabilities to achieve compression ratios of 100:1 to 2000:1, depending on the desired image quality.

MPEG: This method **(Fig C)** uses all of the basic intraframe compression functions and also combines predictive interframe and interpolative interframe coding for motion compensation. The MPEG algorithm first compresses an initial intraframe block using DCT, quantization, and entropy encoding. The coded block is also decompressed and stored in an internal past-memory buffer. The system then uses predictive interframe coding similar to that used in Px64 to code a non-adjacent future frame. This future-frame block is decompressed and stored in the internal future-memory buffer. Then, interpolated interframe coding estimates and codes the intervening frames between subsequent intraframes or interframes.

The interpolated interframe coding used in MPEG is very similar to the predictive interframe, except that the motion estimation involves a comparison and search with respect to both images in the past- and future-frame buffers. Differentiation produces a new pixel block that represents the difference between the current block and the *average* of the past and future blocks. DCT, quantization, and entropy encoding are then applied to the difference block, and the coded bit-stream is stored or transmitted, along with the associated motion vectors needed to reconstruct the original pixel block. The system then moves the image data in the future memory buffer to the past memory buffer and codes a new future frame. Optimized for motion-intensive video applications, MPEG can achieve compression ratios as high as 200:1 but needs high bit rates for transmission.

Note: The preceding summary of compression techniques and standards is an edited version of selected material from "Video Compression Technology Overview," a 27-page report available from Integrated Information Technology of Santa Clara, CA.

vices as the core elements in the company's DVI (digital video interactive) subsystem.

The 82750PB pixel processor interfaces with video RAM to compress and store, or to retrieve and decompress data. To maintain continuous motion, the chip compresses or decompresses each frame of information in less time than it takes to display the frame. Microcode, executed from an on-chip instruction RAM, uses the remaining time of each frame to perform special effects, or to overlay fast graphics and text. To speed up operation, the pixel processor contains image-handling functions, such as a built-in Huffman decoder, a single-cycle n-bit barrel shifter, and a high-resolution pixel interpolator. The device can decompress high-resolution JPEG still images at the rate of 30 images/sec.

The 82750DB display processor retrieves bit-map image data from video RAM, performs post-processing operations (such as 2-D UV interpolation), translates the data from YUV digital video format to RGB analog format, and generates CRT synchronization and control signals. The device delivers the output from the pixel processor to a wide range of video displays, including VGA, NTSC, PAL and SECAM. You can also synchronize the chip with an external video source.

SGS-Thomson offers several chips for use in video compression/decompression applications. Notable are its STV3200 and STV3208 DCT processors, which perform both forward and inverse transforms. The circuit architecture for these chips is fully bidirectional with a 9-bit pixel-data bus and a 12-bit coefficient-data bus. You can program each bus as either the input or the output, depending on the selection of either a forward or an inverse DCT.

The 3200 can handle seven different pixel-block sizes, including 8×8 and 16×16. An 8×8 block is typically used in JPEG applications to convert 64 values to a single value. The 16×16 block is typically used in high-compression video conferencing applications to convert 256 values to a single value. The chip handles pixel rates to 15 MHz.

The 3208 chip performs a DCT only on 8×8 pixel blocks. The chip handles pixel rates to 27 MHz in the single-precision mode, and to 20 MHz in the double-precision mode.

SGS-Thomson's latest chip, the STI3220 motion-estimation processor, is designed for full-motion video applications such as those using MPEG or Px64 standards. **Fig 3** is a block diagram of a video coder

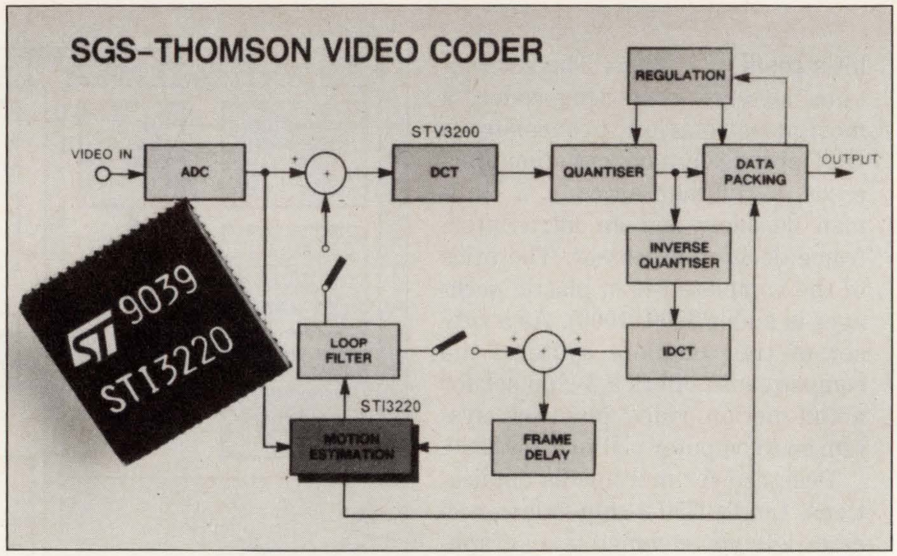


Fig 3—This video coder system *uses two dedicated chips from SGS-Thomson to implement MPEG or Px64 standards. The STV3200 provides DCT compression and decompression, and the STI3220 implements the motion-estimation circuitry needed for full-motion video applications.*

Acronyms used in this article

CCITT—International Consultative Committee for Telegraphy and Telephony
CMYK—Cyan-magenta-yellow-black
DCT—Discrete cosine transform
DIP—Dual in-line package
DMA—Direct memory access
DSP—Digital signal processing
DVI—Digital video interactive
ISO—International Standards Organization
JPEG—Joint Photographic Experts Group
LAN—Local area network
MPEG—Motion Picture Experts Group
NTSC—National Television Standard Committee
PAL—Phase-alternation line
PGA—Pin-grid array
PLCC—Plastic leaded chip carrier
RAM—Random access memory
RGB—Red-green-blue
ROM—Read-only memory
SECAM—Sequential couleur à memorie
SRAM—Static random-access memory
VGA—Video graphics array
VP—Vision processor
YUV—Luminance, chrominance

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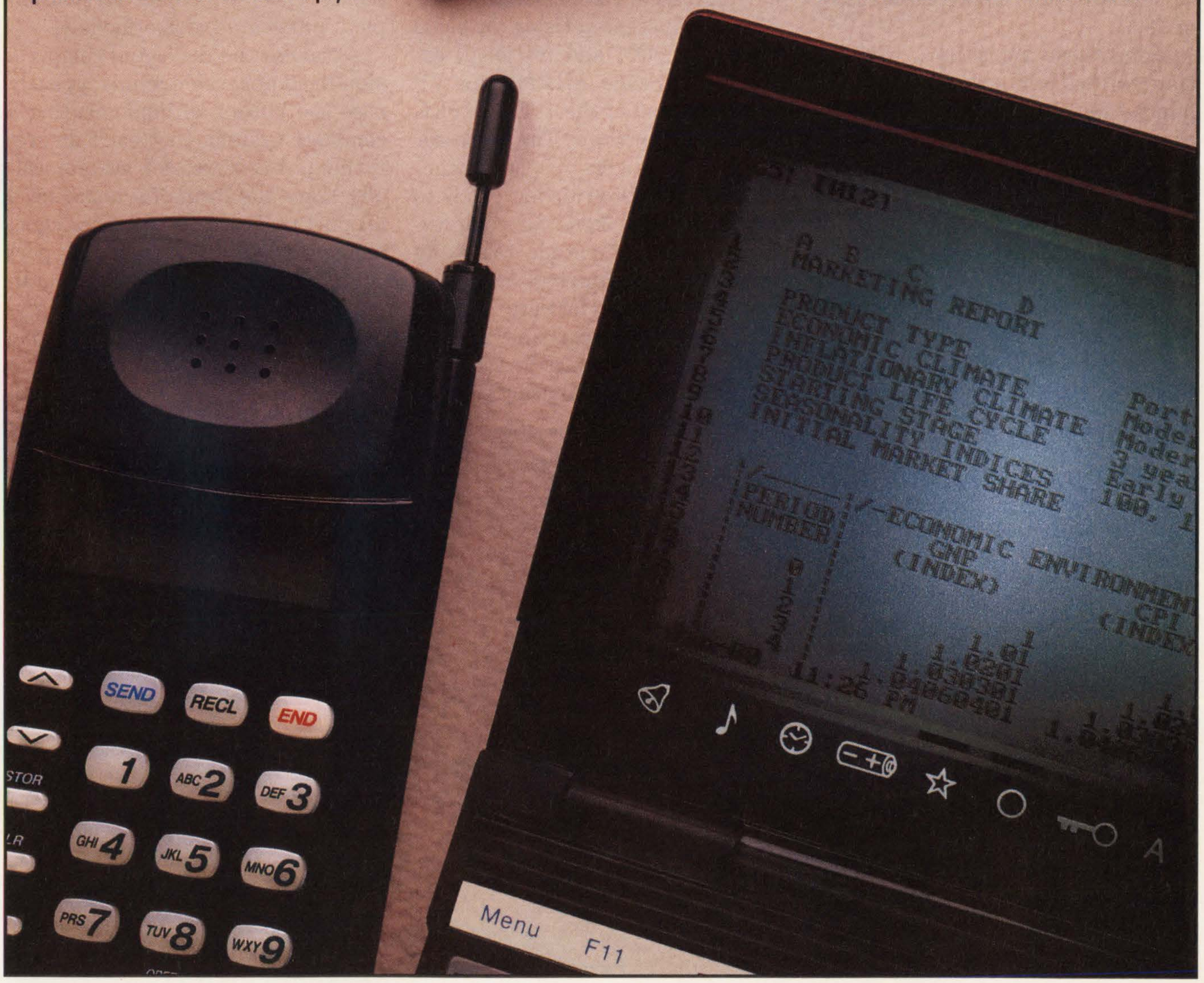

Video-compression chips

using the STV3200 DCT chip and the STI3220 processor.

Motion-estimation circuitry greatly reduces the amount of data required to store or transmit a video signal. Motion estimation exploits the fact that successive images are often similar and consist of the same elements in slightly different positions. Rather than transmit every pixel in every frame, the coder identifies these movements and transmits only the information required to reproduce the same movements at the decoder. In most algorithms, motion estimation is combined with DCT compression to achieve overall compression ratios of 200:1.

Using these algorithms, the motion-estimation processor determines the motion of pixel blocks by comparing each block with all of the surrounding blocks while looking for the best match. The processor then outputs a motion vector (indicating direction) and a distortion factor (indicating the degree of matching). This procedure requires enormous computational power. As an array of 256 processors, the STI3220 can achieve 14 billion operations per second. The chip supports operations on pixel blocks to 16×16 in a search window with a maximum displacement of $+7$ or -8 pixels, corresponding to 256 vectors. Random access to the distortion factors calculated by the chip allows the use of more elaborate algorithms such as half-pixel interpolation.

Chip handles JPEG/MPEG/Px64

Integrated Information Technology (IIT) offers a versatile chip called the Vision Processor (VP). The VP is a highly parallel, microcode-based video processor for use in DCT-based compression/decompression systems. Using internal microcode ROM and (optional) external microcode SRAM, the VP can execute all of the JPEG, MPEG and Px64 algorithms. The processor handles all stages of these algorithms such as converting pixels to run/amplitude tokens for compression, and run/amplitude tokens to pixels for decompression. Other functions include forward and inverse DCT, forward and inverse quantization, motion estimation and compensation, and filtering.

The company provides the microcode for use with JPEG, MPEG, and Px64 standards, thus relieving the system designer from the burden of writing the microcode. Algorithm parameters such as quantization values are customer programmable. The VP's 64-bit parallel architecture performs more than 1.9 billion operations per second. A high-speed DMA port transfers pixel or run/amplitude data to the chip. A command port allows an external processor to initialize the VP, execute microcode subroutines, and control the DMA port. In Q1 1992, IIT plans to introduce a companion vision controller and a complete integrated vision module.

Although the dedicated compression/decompression chips greatly ease the burden of implementing a complete system, they can't do everything. A compression system usually takes the form of a board-level product that also incorporates logic, memory, and other types of support chips. Both dedicated and general-purpose DSP chips are also beginning to play a more important role in compression applications and, in many cases, software is used to implement a specific algorithm. Whatever the final form of the complete system, however, dedicated compresssion chips will play an increasingly important role as manufacturers strive to simplify and reduce the cost of end products. EDN

For more information . . .

For more information on the image-compression products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

C-Cube Microsystems
339-A W Trimble Rd
San Jose, CA 95131
(408) 944-6300
FAX (408) 944-6314
Circle No. 706

Integrated Information Technology
2445 Mission College Blvd
Santa Clara, CA 95054
(408) 727-1885
FAX (408) 980-0432
Circle No. 707

Intel Corp
Box 58130
Santa Clara, CA 95052
(800) 548-4725
Circle No. 708

LSI Logic Corp
1551 McCarthy Blvd
Milpitas, CA 95035
(408) 433-8000
FAX (408) 434-6457
Circle No. 709

SGS-Thomson Microelectronics Inc
1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6228
FAX (602) 867-6102
Circle No. 710

Reference

1. Swager, Anne Watson, "Image compression lightens storage and transport burdens," *EDN*, July 18, 1991.

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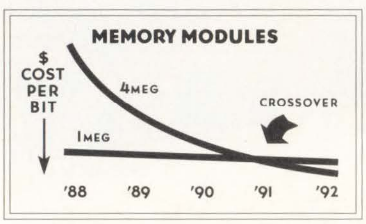
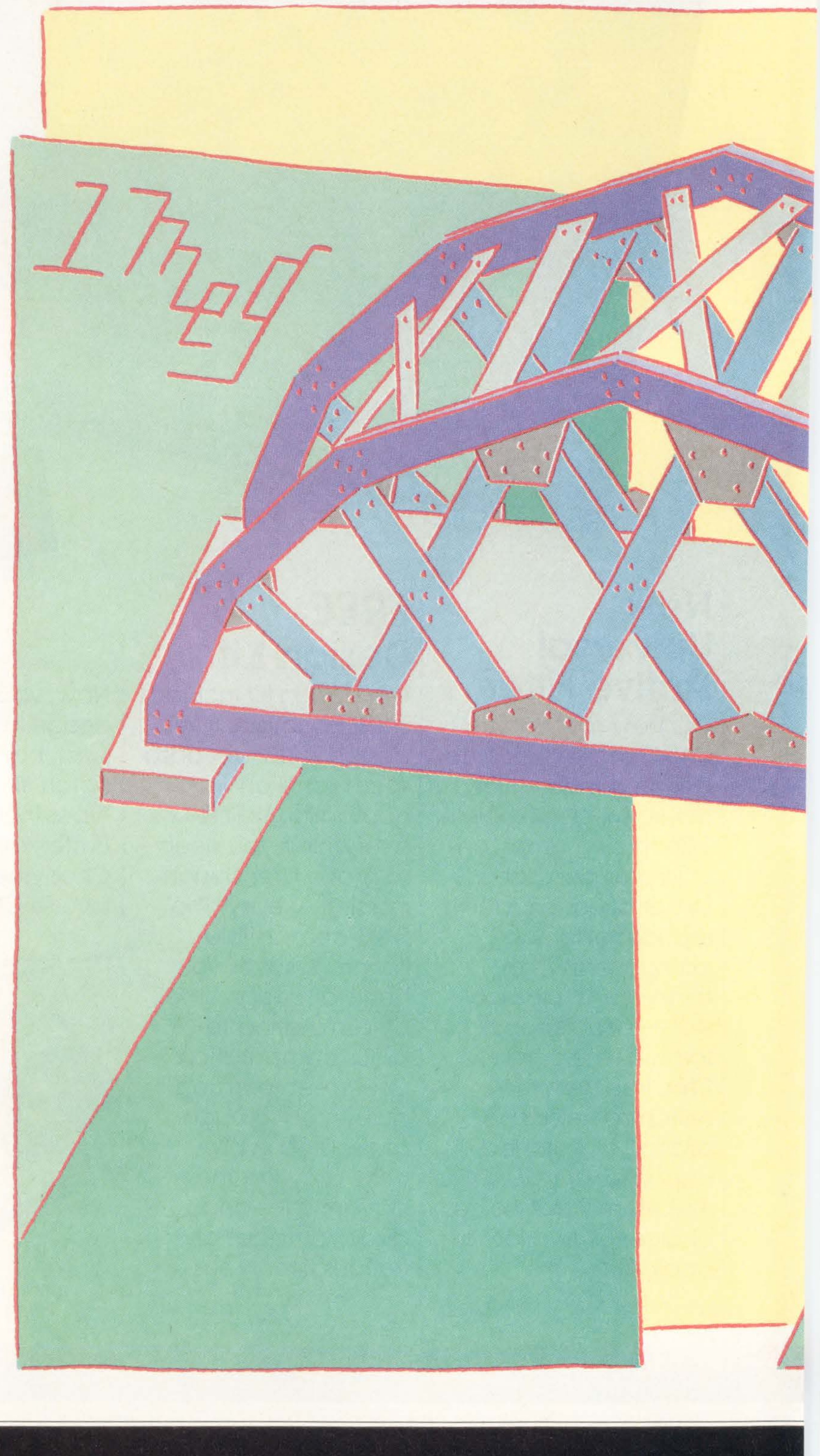


People are lining up to take advantage of it.

One specific advantage is in memory modules. Samsung 4-meg-based modules are actually more cost-effective today than their 1-meg-based counterparts.

All the modules listed here have reliability specs based on 600 temperature cycles (0-125°C) and 500 hours (85°C, 85% RH). Available features include 70, 80, and 100 ns access



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4	KMM5321000A	1M x 32
4	KMM5331000A	1M x 33
4	KMM5361000A	1M x 36
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SAMSUNG

Technology that works for life.

CIRCLE NO. 50

Wescon '91 offers a treasury of technology

November will find Moscone Convention Center in San Francisco opening its doors for the West Coast's annual sampling of electronic engineering's state of the art.

Carl Quesnel, *Associate Editor*

San Francisco will be swarming with engineers from November 19 to 21 for Wescon '91. High-speed logic design, memory systems, and PC applications and architectures are only a few of the topics that will be covered in 30 technical sessions. Nine technical courses will give engineers access to technology at the forefront of electronic design and manufacturing. And more companies than you can count will field representatives on the show floor.

Conference sessions will treat different engineering disciplines each day (**Table 1**). Tuesday, November 19, will feature sessions on neural networks and robotics, FPGAs, high-speed logic design, memory systems, and flat-panel displays. The Wednesday sessions will address networks, PLDs, sensors, image compression, and virtual reality. Thursday will round out the conference with sessions on embedded controls, PCs, ASICs and multichip modules, and design for testability and manufacturability. Among many other participants, companies organizing these sessions will include VLSI Technology, Xilinx, Integrated Device Technology, Viewlogic, National Semiconductor, Chips and Technologies, Texas Instruments, Advanced Micro Devices, and Hitachi.

San Francisco Convention & Visitors Bureau photo by Kerrick James.

Session 3, "Next-generation FPGAs accelerate system design," will present four papers describing how next-generation FPGAs have overcome limitations that previously held these devices behind masked ASICs in performance, density, and flexibility. A few hours later, participants in **session 4** will discuss the features and benefits of recently introduced CAE tools for creating FPGAs. Thursday morning, ASIC supporters will have their chance to rebut in **session 27**, "ASIC directions for the '90s." Session participants will examine technology trends that will soon make it possible to integrate an entire system on a single chip.

PCs vs workstations

Although workstations remain more powerful, PCs enjoy a much larger installed base and thus present a tempting opportunity for engineering-software vendors. Many design engineers remain convinced, however, that a PC just cannot perform CAD, CAM, CAE, and CASE functions well enough to justify the cost savings. A special session on Tuesday afternoon will feature a panel discussion on the assertion of EDA (electronic design automation) companies that it is the applications software rather than the hardware that drives EDA productivity. Panel members, representing both computer manufacturers and EDA companies, will go head to head over this issue.

In addition to technical sessions, Wescon '91 offers nine technical courses for engineers (**Table 1**). Topics will include concurrent engineering, surface-mount technology, optical-based sensors, design for testability, FPGA design, data storage, and high-performance packaging. Those interested in engineering management have three management seminars to choose from. Most sessions are day long—the half-day sessions are on Thursday—and require an extra fee. The fee for day-long seminars is $250 to $300; for half-day seminars, the fee is $150 to $200.

Concurrent engineering and design for testability will get their share of attention in **short course T1** on Tuesday and **short course T4** on Wednesday, respectively. "Concurrent engineering: Tying it all together" will provide attendees with the knowledge they need to produce high-quality products quickly through the simultaneous design of products and their associated manufacturing and test processes and support services. "Design for testability" will present testable designs of actual products and have attendees remedy untestable configurations of the same products. Attendees will also learn how to use this basic knowledge to work effectively within a team.

Come and see the show

When you're tired of sitting down, you can stretch your legs on the show floor and pick up some product literature from your favorite companies. This year, the show floor will feature three focus areas. These areas—for semiconductors, EDA tools, and test and measurement equipment—will group companies by field to make it easier for

Table 1—Wescon '91 technical conferences and courses schedule

Tuesday November 19, 1991	**Neural networks and robotics**	**Advances in FPGAs**	**High-speed logic design**	**Memory systems**	**Image display**	**Technical courses (9:00 am to 5:00 pm)**
9:00 am to 11:00 am	**Session 1** The "new wave" in computing: Advanced technologies facilitate today's neural-network applications	**Session 3** Next-generation FPGAs accelerate system design	**Session 5** Solving clock distribution problems in high-speed systems	**Session 7** Specialty memories: A rapidly evolving set of tools for the designer of high-performance products	**Session 9** Implementation of flat-panel displays	**Short course T1** Concurrent engineering: Tying it all together **Short course T2** Surface-mount technology: Principles and practices **Short course T3** An introduction to optical-based sensors
2:00 pm to 4:00 pm	**Session 2** Machine-vision systems	**Session 4** Advanced CAE tools for FPGA design	**Special session** PCs vs workstations: The software implications	**Session 8** Design advances of memory cards for portable systems		
Wednesday November 20, 1991	**Communication networks**	**Advances in PLDs**	**High-speed logic design**	**Memory systems and sensors**	**Image display**	**Technical courses (9:00 am to 5:00 pm)**
9:00 am to 11:00 am	**Session 11** The framework of an OSI network management system	**Session 14** Innovative, high-density PLD architectures	**Session 17** High-speed logic to the rescue...	**Session 20** Hassle-free cache design (without compromising performance)	**Session 10** Image compression: A key enabler of multimedia	**Short course T4** Design for testability **Short course T5** Surface-mount/fine-pitch technology **Short course T6** Short-run statistical process control for electronics manufacturing **Short course T7** 3000-series FPGA design
11:30 am to 1:30 pm	**Session 12** FDDI design issues		**Session 18** Interconnect issues for high-speed electronic systems	**Session 21** Recent trends in embedded control memory		
2:00 pm to 4:00 pm	**Session 13** The emerging 10BaseT standard: Trends in silicon and software	**Session 16** New PLD design tools enable flexible and efficient systems-level design	**Session 19** Combating EMI in high-speed electronic systems	**Session 20** Enabling sensor technologies—markets, trends, and applications	**Special session** Virtual reality	
Thursday November 21, 1991	**Embedded controls**	**PC applications and architectures**	**ASICs and multichip modules**	**Design for testability and manufacturability**		**Technical courses (9:00 am to 1:00 pm)**
9:00 am to 11:00 am	**Session 23** Real-time and embedded systems development and deployment	**Session 25** Portable applications for PC-compatible chip sets	**Session 27** ASIC directions for the '90s	**Session 29** Electronic product design for manufacturability and testability		**Short course T8** Data storage; magnetic, optical, and systems **Short course T9** From DIPs to multichips: An introduction to high-performance packaging
11:30 am to 1:30 pm	**Session 24** High-performance embedded control devices	**Session 26** PC bus architectures: Beyond the standard AT bus performance	**Session 28** The impact of multichip modules in the '90s	**Session 30** Using the IEEE boundary-scan and test-access port (JTAG)		

Acronyms used in this article

ASIC—Application-specific integrated circuit
CAD—Computer-aided design
CAE—Computer-aided engineering
CAM—Computer-aided manufacturing
CASE—Computer-aided software engineering
EDA—Electronic design automation
FPGA—Field-programmable gate array
PC—Personal computer
PLD—Programmable logic device

you to gather information. In addition, companies will present information on components, hardware, subsystems, manufacturing materials, and engineering and manufacturing services.

EDN will be at Wescon to celebrate advances in electronics at its annual Innovation Dinner and Awards Ceremony during the show. The event will take place at the Mark Hopkins Hotel on Tuesday, November 19. If you want to attend and show your support for innovative work in electronic design, get a reservation order form by faxing Pam Winch at (617) 558-4470.

The show will be open from 9:00 am to 5:00 pm Tuesday and Wednesday and 9:00 am to 4:00 pm on Thursday. General admission is $15 at the door. For more information, write Wescon '91, 8110 Airport Blvd, Los Angeles, CA 90045, call (800) 877-2668, or fax (213) 641-5117. EDN

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MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120*	1200	48	15ns	50 MHz	68	MASC 120
MACH 220*	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230*	3600	128	15ns	50 MHz	84	MASC 230

* Available Q4 1991.

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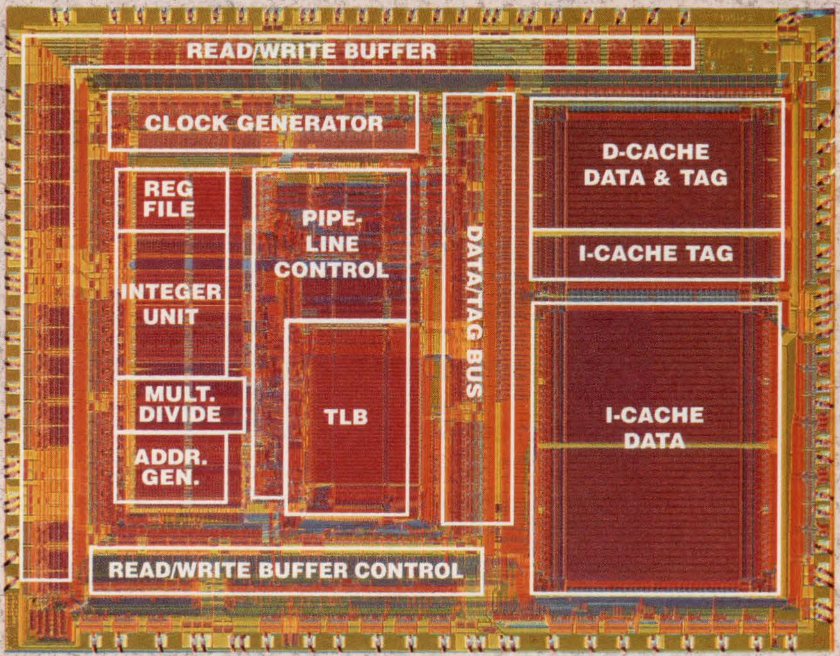

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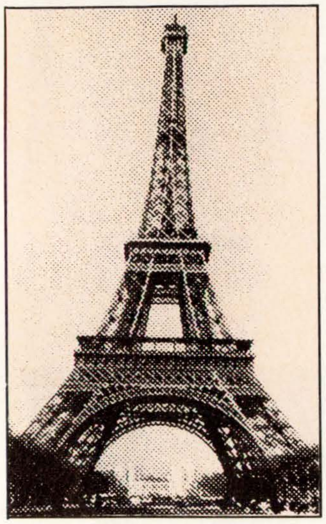
Componic '91



Raymond Boult

Componic '91, one of the dominant European electronics exhibitions, will run from November 18 to 22 at the Paris-Nord Exposition Center ("Parc des Expositions"). The Center is located on the express subway line, which links Charles de Gaulle Airport to Paris. Manufacturers will exhibit their products in 70,000 square meters of allotted space. Semiconductors, printed circuits, electromechanical components, test and measurement instruments, and commercial-distribution products will be on display for attendees.

In addition to taking in the show, you will be able to participate in a series of roundtable discussions on various topics, which will bring together key people in the appropriate fields. Componic is being organized by SDSA (part of the Paris Exposition Commission on behalf of SYCEP (Syndicat des Industries de Composants Electroniques Passifs), the French passive-electronics-components trade federation. Five sections of SYCEP are each sponsoring a roundtable debate, and each topic corresponds to each section's specialty.

At press time, four of the five sections had been finalized. They will cover

- printed circuits (roundtable topic is "Better buying for constant improvements in customer service at optimal cost")
- magnetic components (topic is "Magnetic components for SMT")
- connectors (topic is "Trends in the use of the metric system")
- hybrid circuits (topic is "Miniaturization with optimization of costs and services").

To give you an idea of what the Componic show has in store, EDN asked Europe's "Big Three" electronics component manufacturers—Philips (The Netherlands), Siemens (Germany), and SGS-Thomson Microelectronics (a Franco-Italian concern)—to provide a preview of the main attractions on display at their booths. (The addresses given are for these companies' French subsidiaries, which are the respective booth organizers.)

Philips, for instance, is introducing the Euro-90 switchers, a range of compact power supplies for 19-in. rack mounting for the DIN 41494 standard. Rated at 40, 50, and 60W (higher power models are already under development), these supplies are suitable for powering a range of applications in the general electronic equipment and computer sectors, particularly process control, medical, and automation systems, as well as industrial PCs. Philips's use of SMDs and hybrids on compact boards allows a creepage distance of 8 mm as required by the SELV (safety extra low voltage) circuit VDE 0806 standard. MTBF is guaranteed at more than 180,000 hours. (Philips Composants, 117 quai du President Roosevelt, BP 75, 92134 Issy-Les-Moulineaux Cedex, France.)

Siemens's booth at Componic will feature the SAB-R4000 family of 64-bit RISC microprocessors, as well as the Arcofi-SP audio ringing codec filter with speakerphone function. The R4000 family is suitable for wide-ranging applications including embedded controllers, desktop systems, workstations, and departmental servers and for such high-end applications as multiprocessing and fault-tolerant systems. Features include compatibility with earlier 32-bit devices, 64-bit integer and floating-point operations, registers and virtual addresses, a 50-MHz clock frequency, and a 5V power supply. On-chip features include

8-kbyte instruction and data caches, a memory-management unit whose variable page size ranges from 4 kbytes to 16 Mbytes, and an ANSI/IEEE-754-standard floating-point unit.

The Arcofi-SP codec filter is designed for digital terminal-equipment applications requiring voice functions. Codec functions are performed using digital signal processing, in accordance with the CCITT G.714 specification. Siemens recommends use of the IOM-2 serial data interface, rather than the SLD interface; although implemented in the Arcofi-SP, the SLD is not guaranteed. Dual analog inputs for the microphone in the handset and the speakerphone, plus an auxiliary differential analog input, are combined with two differential outputs for a handset earpiece and a loudspeaker, for which the drive capability is 100 mW (sine wave). (Siemens SA, 39/47 boulevard Ornano, 93527 St Denis Cedex, France.)

Pact leads to video chips

SGS-Thomson Microelectronics' UK subsidiary, Inmos, announced an agreement with IBM to manufacture and market chip sets for the US firm's Extended Graphics Array (XGA) PC video standard. Currently manufactured by IBM, the chips will be known as the IMS G200 display controller and the IMS G190 serializer palette DAC. Prototypes will be on display at the copany's booth. The European firm will immediately begin work on porting XGA technology to AT-compatible versions of the chip set, which will be manufactured at Inmos's production site at Newport, UK, and at SGS-Thomson's site at Carrollton, TX.

The G200 contains three major on-chip elements: a system bus interface, a CRT and memory controller, and a graphics coprocessor. The bus interface is designed to provide a 16- or 32-bit bus-master facility for IBM's Micro Channel Architecture; the controller manages pixel transfers to the G190 chip. The G200's graphics coprocessor supports user environments such as Microsoft's Windows or OS/2 Presentation Manager. The G190 serializer palette DAC features a pixel serializer, a color palette, three DACs, and a sprite and VGA font/attribute controller. The device delivers a stream of pixels from the video memory to the color palette, which is then transmitted to the DACs for on-screen display. Finally, the sprite and VGA font/attribute controller determines the position of a 64×64-pixel overlay image ("sprite" or "cursor") on the display, which is often used for graphics windowing. The controller also determines the attributes such as underlining and highlighting and the position and color of displayed texts.

The agreement with Inmos follows similar technology-exchange deals made earlier this summer by IBM with Germany's Siemens covering 16-Mbit dynamic RAMs, and with US-based Apple (and indirectly with Motorola) covering RISC microprocessors. (SGS-Thomson Microelectronics, 7 avenue Gallieni—BP 93, 94253 Gentilly Cedex, France.)

These major European manufacturers' offerings are just but a glimpse of the products that will be on display at Componic. You'll be able to see and hear about a lot more—that is, if you're lucky enough to get to Paris in November.

EDN

Raymond Boult is an independent journalist based in Paris, France.

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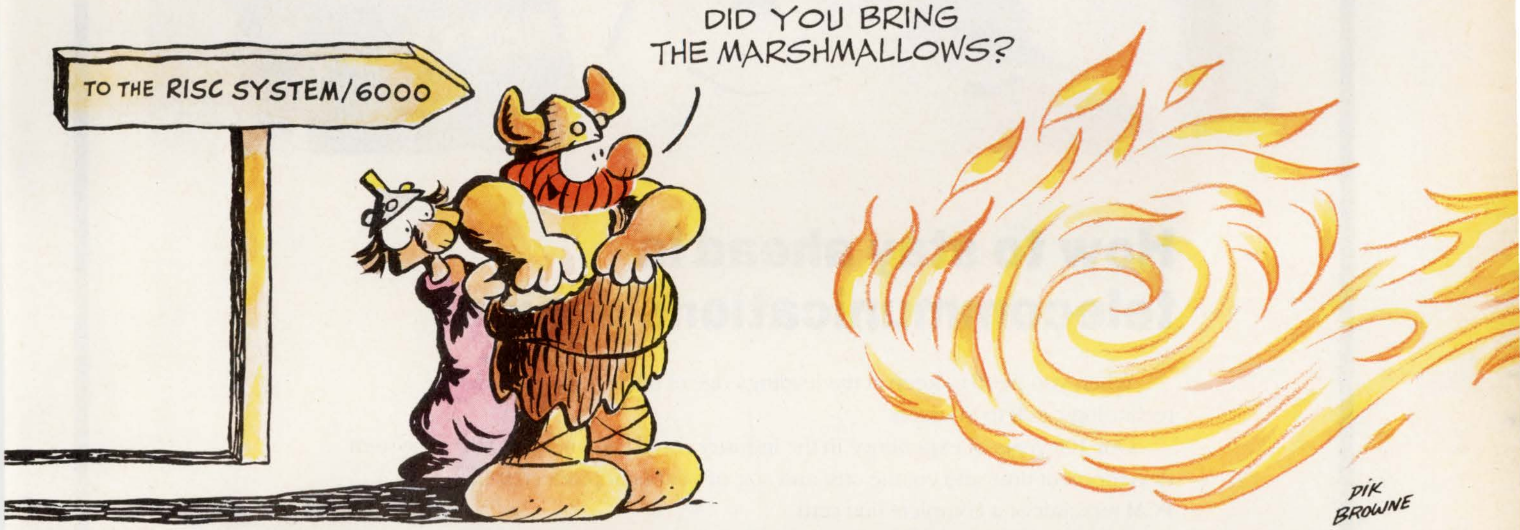

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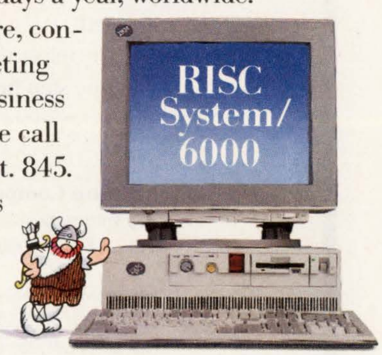

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CIRCLE NO. 60

EDN EDITORS' CHOICE

INNOVATION

Signal processor implements analog and digital functions in real time

Combining the Sproc 1400's multiprocessing architecture with the company's development tools *allows you to design analog and digital signal-processing functions at the block-diagram level. Without your having to write any code, software then automatically allocates execution tasks to each processor for the fastest runtime.*

Representing a major departure from the architecture and programming methods of other digital signal processors, the Sproc 1400 and future members of the 1000 family consist of a central memory unit shared by as many as four 24-bit, fixed-point processors. Programming the IC requires no manual coding—you can enter your entire design graphically at the block-diagram level using the company's development-system software. That block diagram can include both analog and digital functions resident in the software's cell library.

The processor incorporates all processor units, interprocessor communications circuitry, and memory required to implement signal-processing functions. A single stand-alone processor can replace analog circuits in applications that don't require a host µP or can work in conjunction with a host in a more complex system.

Unlike other DSP architectures, which base real-time operation on allocating processing power as interrupts occur, this processor time-division-multiplexes its central memory to provide concurrency between the various processors. The central multiported memory consists of 1k×24 bits of program RAM and 1k×24 bits of data RAM. A patented memory multiplexing scheme simplifies the programming and coordination of multiple processors that together run a single application. The four processors work individually or collectively, depending on the requirements of your application. Development software informs you how many processors the chip actually uses for each design.

Input and output data-flow managers handle the switching between concurrent tasks. These managers communicate with the processors and other on-chip elements through a 12-bit address and 24-bit data bus, and with off-chip data converters and digital data streams through programmable serial ports.

The processor includes two types of I/O interfaces that are compatible with most existing µPs' memories and peripherals. Four completely independent serial ports, two input and two output, each can operate with their own internal or external clocks, I/O word widths, and bit ordering. The parallel port is a single 24-bit, asynchronous bidirectional interface. Users can select word width to 24-bits and byte ordering for data transferred over the parallel port. Through the parallel port, you can program the IC dynamically using a host processor by operating in slave mode.

Despite the fact that the IC is purely digital, its architecture makes it possible for the IC to perform digital- *and* analog-type functions in real time. The analog nature of any digital device is initially difficult to fathom. However, if you consider that most analog components, such as amplifiers and integrators, are performing a mathematical function, the chip is simply computing these functions digitally. Just as digital filtering offers certain advantages over analog filtering, digital computation also offers higher precision, stability, and noise immunity than the corresponding analog approaches. One limitation is the processor's 250-kHz bandwidth. The 24-bit internal data bus theoretically offers a dynamic range of 144 dB and provides enough head room for processing of 16-bit analog signals.

Designing and programming the device requires four steps: creating a signal-flow diagram, compiling and linking processor-executable code, downloading code to the chip, and system calibrating, debugging and refining. The MS DOS-based Sproclab development system ($8950) consists of software and hardware that perform each of these steps. The system automatically allocates execution tasks to available processors and schedules those tasks during compile time for the fastest possible operation.

The software tools include a signal-flow editor, a cell library, custom filter-design software, an automatic compiler, and loading and debugging tools. Hardware tools include a μP-based interface from the processor's target system to the development system, and an evaluation/prototyping board that contains one Sproc 1400, interface converters, and logic. The development system's cell library currently includes 50 basic building blocks, including such traditional analog functions as filters, amplifiers, summing junctions, integrators, rectifiers, multipliers, and phase-locked loops.

A probe feature makes the system particularly useful during debugging by allowing you to observe and control system functions and performance under various conditions. An access port links the processor through the company-designed interface box to the development system. While the system is running, you can select and direct a signal from anywhere in the processing chain to this port. You can then view this signal on a scope. While observing the signal, you can change various parameters of your function blocks to view the effects.

The processor comes in a 132-pin ceramic pin-grid array and runs off 5V. The company is now selling a 20-MHz version of the 1400 through distributors at the suggested price of $495 (25). Sometime in the first quarter of 1992, the company will upgrade the chip to 50 MHz. Prices for 10,000-piece quantities will be $80. Sometime in the second quarter, 1- and 2-processor versions of the IC will also be available for $32 and $38 (10,000), respectively.

—*Anne Watson Swager*

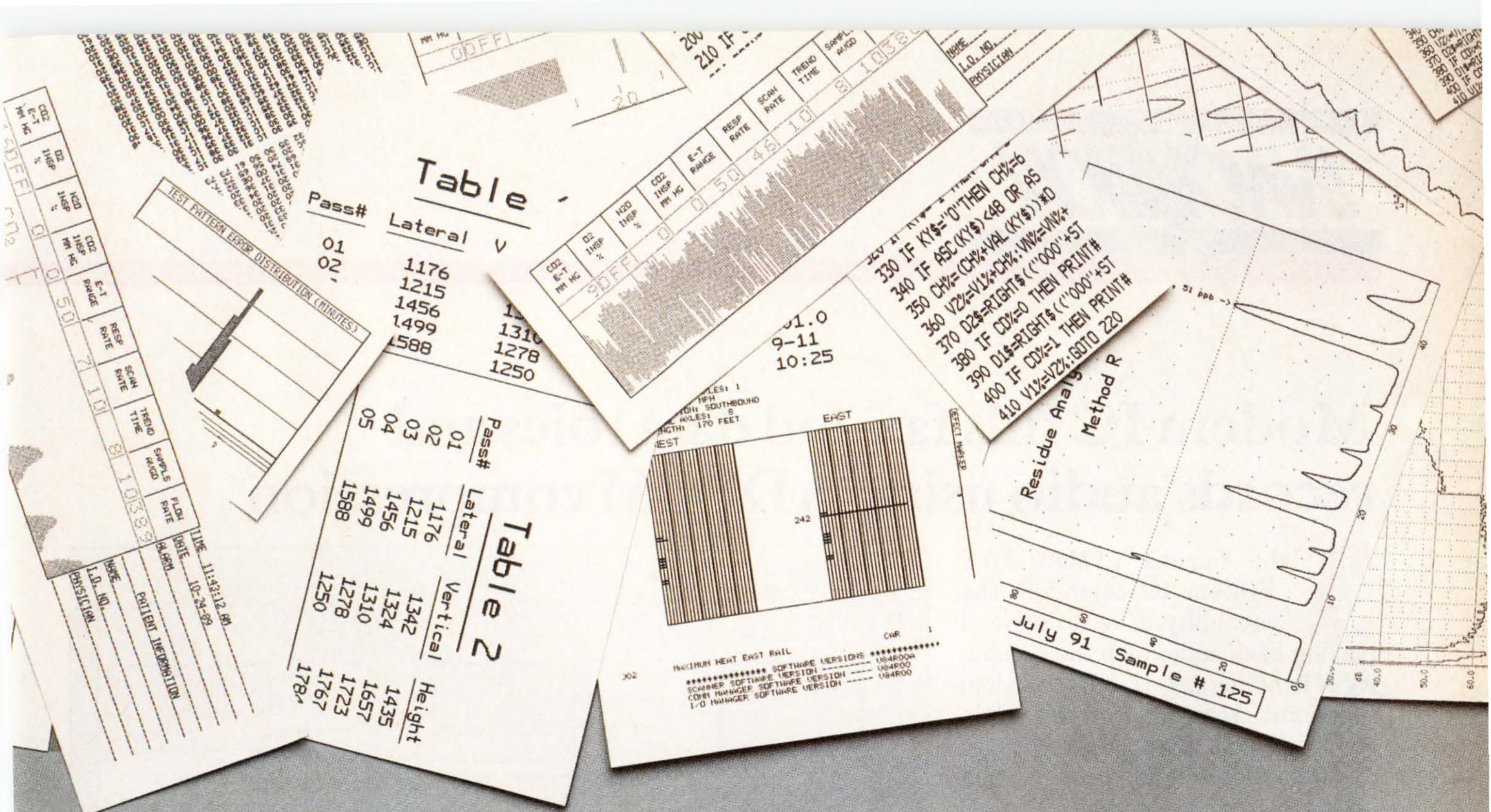
Star Semiconductor Corp, 25 Independence Blvd, Warren, NJ 07059. Phone (908) 647-9400. FAX (908) 647-4755.

Circle No. 730

EDN's Editors' Choice

On occasion, a new product will show a great deal of innovation and thus appear as an EDN Editors' Choice selection. To qualify for special coverage by our editors, an innovative product must:

- Offer significantly higher levels of performance in ways not previously available
- Solve a continuing problem much more effectively than its predecessor
- Exhibit a marked degree of cleverness, which differentiates it from earlier products
- Embody new technology that advances the state of the art or use older technology in a unique and innovative way.



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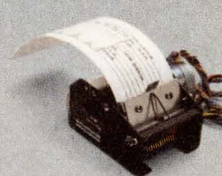
PM1224	2.6 inches	18 to 37	100	224	$311
PM1320	2.6 inches	23 to 53	150	320	$296
PM1416	4.5 inches	29 to 69	100	416	$443

1 This is the 300-piece OEM price. It is subject to change without notice.

2 The maximum number of columns depends on the font and size selected. The higher number is for 5 x 7 characters, approximately 16 characters/in.



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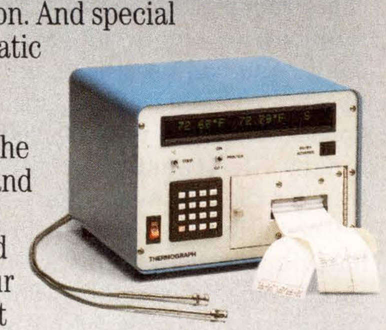

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B-G INSTRUMENTS

EDN EDITORS' CHOICE INNOVATION

Modem IC fills fax and data roles and records audio using ADPCM compression

The Yamaha YTM403 FAX VOdem IC combines the capability of recording and playing back audio with the capability of handling fax- and data-modem functions. You can use the IC in board designs that transmit faxes and data files and fill voice-mail and answering-machine roles. The IC can also automatically identify the phone number on incoming calls. The company offers a companion controller IC and firmware that simplify the product design, using the modem IC.

The modem IC uses a DSP core to implement the modem and voice capabilities. **Fig 1** depicts the chip architecture and illustrates the minimum amount of analog circuitry used in the modem. The IC has an HDLC (high-level data-link control) framing USART that performs the bit stripping and cyclic redundancy check required for Group 3 fax communications in error-correction mode. You can use the IC in 9600-bps fax communications, including applications that use the 9600-bps binary-file-transfer protocol to transfer files between PCs.

Compatibility with synchronous half-duplex communications at speeds ranging from 300 to 9600 bps ensures that boards based on the modem IC will work with older fax products. The IC supports full-duplex asynchronous data communications at speeds ranging from 300 to 2400 bps. It's also compatible with a number of international communications standards, such as Bell 212A and 103, CCITT V.29, V.27 ter, V.26 bis, V.23, V.22 bis, and V.21.

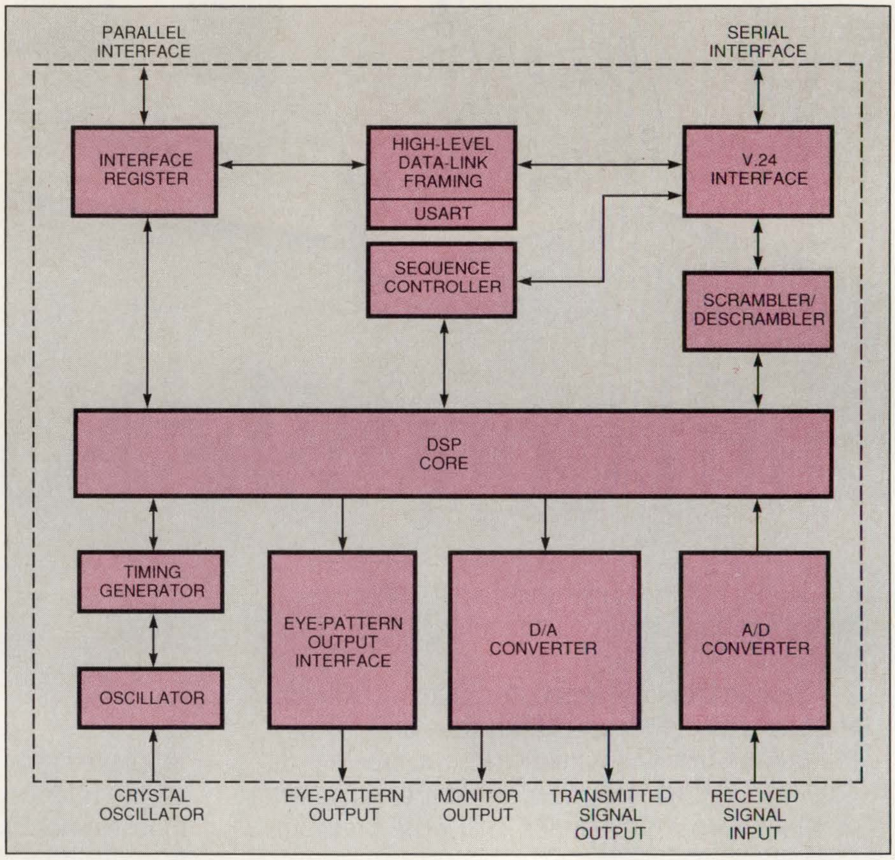


*Fig 1—**The DSP-based modem IC** provides fax and data capabilities and can record and play back voice transmissions using ADPCM compression and decompression.*

Other features of the modem chip include a programmable tone generator and DTMF tone detection. In fact, the DTMF detection can remain active during voice operations to interrupt messages during voice-mail operations. The caller-identification feature implements a database program that automatically accesses data of an incoming phone number before the user answers the call.

The IC can detect whether incoming calls are voice, data, or fax calls. Therefore, a user of a YTM403-based board could use the board with a single phone line. The IC's serial and parallel interfaces perform equally well in board designs for PCs and stand-alone modem devices.

You can use the modem chip to perform ADPCM (adaptive differential pulse-code-modulation) compression and decompression of audio. The IC can perform 8- to 4-bit 2:1 compression as most ADPCM-compatible devices do. Its enhanced compression mode offers 12- to 4-bit 3:1 compression, providing better audio quality.

The GTM407 companion controller IC features an 8051-µP-compatible core. The company's firmware makes a modem that's based on the pair of ICs compatible with the industry-standard Hayes AT command set. The controller IC can address as much as 128 kbytes of external EPROM or RAM. You can use the external memory to customize the controller firmware for your applications. The controller IC's serial interface connects with nonvolatile RAMs.

The standard controller-IC firmware supports voice and modem functions and implements automatic baud detection. The controller firmware is also compatible with V.42 and MNP-1-4 (Microcom Networking Protocol) error-correction code, and V.42 bis and MNP-5 data compression.

The 0.8-µm CMOS chip dissipates 300 mW from a single 5V supply, and a standby mode critical to applications in notebook computers requires only 1 mW. The 64-pin IC comes in shrink-DIPs and quad flatpacks and costs $40 (1000). The 80-pin GTM407 controller IC costs $15 (1000) and includes power-down circuitry that minimizes power consumption on both chips.

—Maury Wright

Yamaha Corp of America, 981 Ridder Park Dr, San Jose, CA 95131. Phone (408) 437-3133. FAX (408) 437-8791.

Circle No. 734

DACs offer programmable output range and single- or dual-supply operation

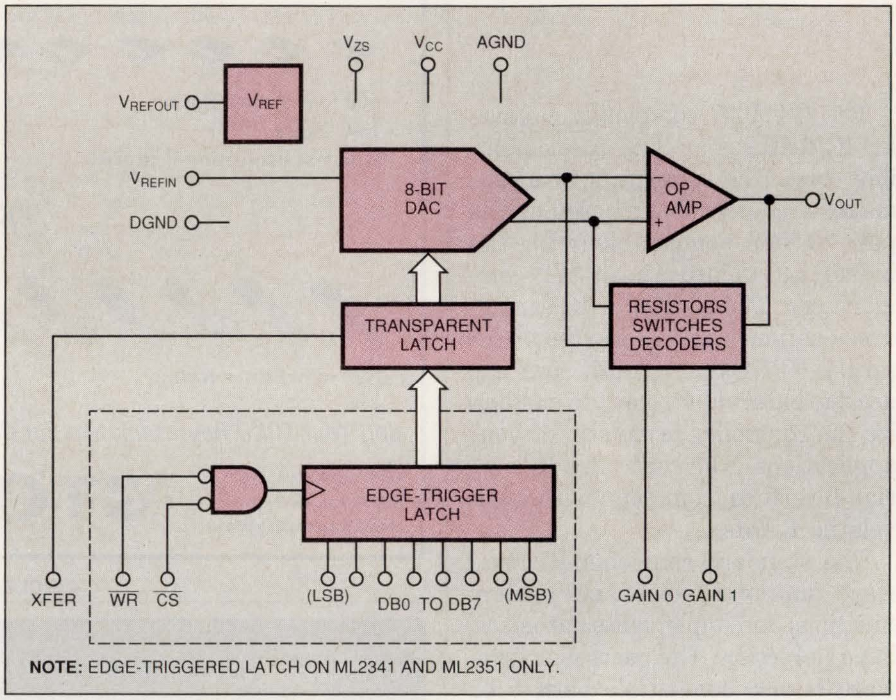
The ML2340/41/50/51 D/A converter (DAC) family gives you a lot of freedom in choosing supply and output voltages. The devices can operate from a single or dual supply while working in either bipolar or unipolar mode. They also offer a programmable output swing and provide a reference output voltage that adapts to reflect the available supply.

At each device's core is a CMOS 8-bit DAC that operates with a 4.5 to 13.2V single supply or a ±2.25 to ±6.6V dual supply, drawing a maximum of 5 mA at 5V. Two reference signals control both the DAC's output signal range and its operating mode.

The zero-scale voltage (V_{ZS}) determines what output the DAC will provide for an all-zero digital input. It also determines the device's operating mode. If V_{ZS} is <1.0V, the DAC will operate as a unipolar device with an output signal that swings from V_{ZS} to full scale. If V_{ZS} is >1.5V, the DAC will operate as a bipolar device and produce a signal with a symmetric range centered on V_{ZS}. In bipolar mode the DAC treats its digital inputs as 2's-complement binary numbers.

The input reference voltage (V_{REFIN}) controls the DAC's full-scale output range. This range also depends on the DAC's programmable output buffer. The buffer converts the DAC's current-based output signal to a voltage base. Two gain programming pins determine the output voltage swing. The swing can be ¼, ½, 1×, or 2× the reference voltage.

This programmable output capability is especially useful in servo applications where the steady-state condition is near the DAC's zero output. You can use the high-gain condition for coarse adjustments over the DAC's greatest possible range. As your system approaches its steady-state condition, you can then switch to a lower gain, effectively increasing the resolution of your DAC.



Flexibility is the hallmark of this DAC family, *offering you a variety of operating modes, output voltages, and digital interfaces.*

To simplify the provision of an input reference voltage, the DACs offer an on-chip reference voltage source with a 1% tolerance. The reference voltage assumes a low value if the supply voltage is <7V and assumes a high value if the supply exceeds 8V. The exact voltage varies with the specific family member. The ML2340 and ML2350 offer 2.25 and 4.5V, respectively; the ML2341 and ML2351 offer 2.5 and 5.0V, respectively.

The nature of the digital interface also varies with each family member. The ML2340 and ML2350 have 8-bit transparent latches, activated by a single control line. The ML2341 and ML2351 have an additional buffer between the input pins and the latch. This second buffer acts like an addressable register, requiring both a chip-select signal and a write strobe in order to accept data. Both interfaces have a power-on reset feature that sets the latches to zero if the supply voltage reaches 2V.

Both devices are available in DIP and SOIC packages. The ML2340 and ML2350 cost $3.75; the ML2341 and ML2351 cost $3.85 (100) and are also available in plastic leaded chip carriers.—***Richard A Quinnell***

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Circle No. 731


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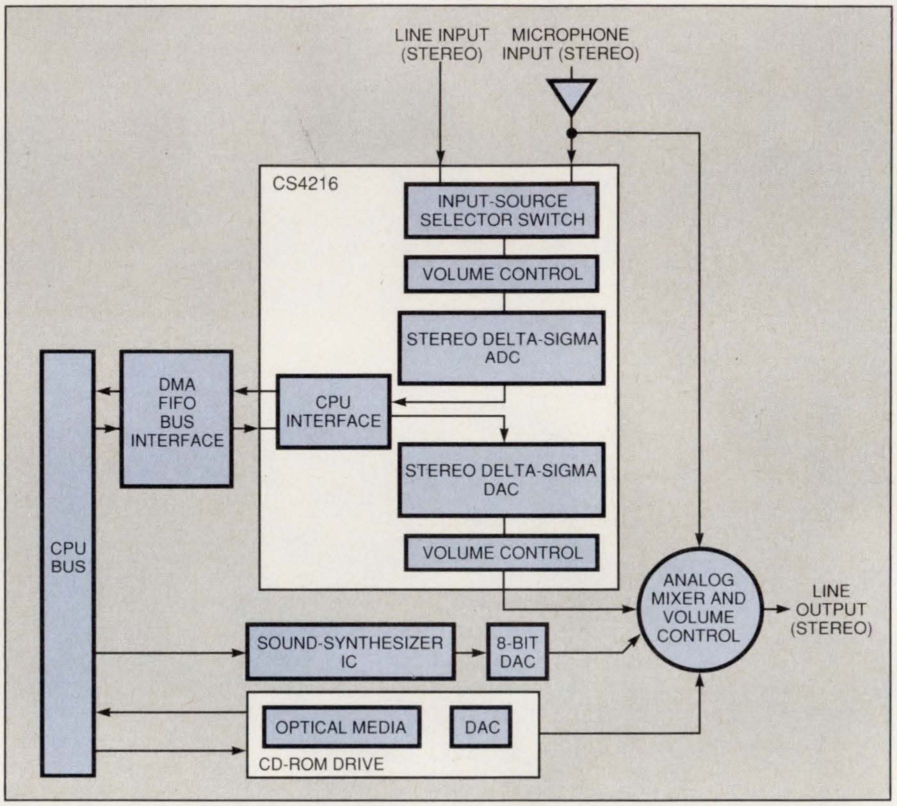
CIRCLE NO. 48

CD-quality audio ICs let PC mother boards meet multimedia specs

As the PC industry continues to herald the approaching era of multimedia, system developers can now select from two ICs that simplify the problem of upgrading computer hardware. In a straightforward and cost-effective manner, the CS4215 and CS4216 stereo-audio codecs provide monolithic CMOS alternatives for adding CD-quality sound on a PC mother board.

Both of these ICs perform 16-bit A/D and D/A conversion and operate from a single 5V power supply. Both provide a S/N ratio of >80 dB and contain antialiasing and output-smoothing filters. However, the CS4216 is the simpler of the two chips, acting strictly as an audio data-conversion device with internal delta-sigma modulation and 64× oversampling. The CS4215 adds a microphone input, a headphone driver, a 32Ω monophonic speaker drive, and on-chip crystal oscillators that grant you 10 software-programmable conversion rates ranging from 8 to 48 kHz.



***By incorporating CPU interface circuitry, stereo A/D and D/A converters, volume controls, and** input selection in a single chip, the CS4216 simplifies your development task and makes a PC compatible with Microsoft's Multimedia PC specification.*

You can attach as many as four CS4216 codecs to a single hardware bus. The CPU communicates with this device via a serial port that has separate pins for input and output data. You can control the sample rate by changing the serial-port bit rate. The chips' filters and converters operate over a sample-rate range of 1 to 48 kHz. You can also adjust the input gain and output attenuation from 0 to 22.5 dB in 1.5-dB steps.

A soft power-down mode occurs when the chip's serial-clock frequency drops to less than one-twelfth the master-clock frequency. In this mode, power dissipation drops from a normal 50 mA to 100 μA, making this IC useful for portable and battery-powered designs. And although the chip's parallel-bit I/O continues to function, its serial-data output will indicate invalid data and present the appropriate error code.

In contrast, the CS4215 has additional circuitry that lets it drive a 32Ω loudspeaker and a 20Ω set of headphones. On-chip controls let you mute these outputs, if you wish. An internal multiplexer toggles between line-level inputs and microphone-level inputs. To monitor the input audio signal, the chip routes the output of its A/D converters though a monitor-path attenuator. An internal calibration cycle minimizes both output offset voltage and input offset error. The CS4215's I/O capabilities suit it for applications that include CD-quality music, FM radio-quality music, telephone-quality speech, and modems.

Both ICs are packaged in 44-pin plastic leaded chip carriers. The CS4215 sells for $30; the CS4216 costs $23 (1000).—***JD Mosley***

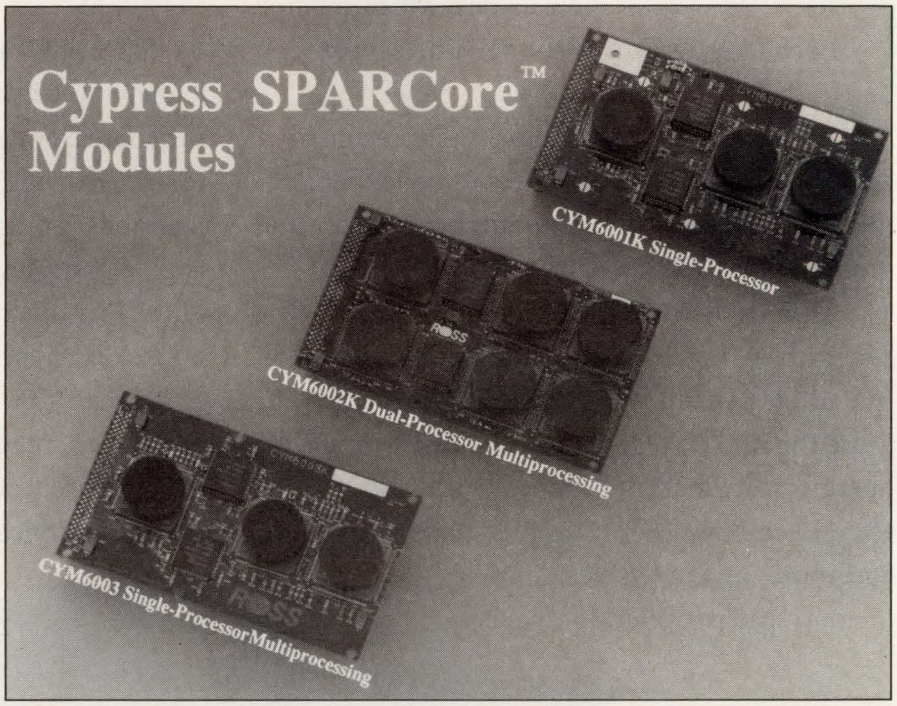
Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222. FAX (512) 445-7581.

Circle No. 732

SPARC CPU module offers easy upgrade path from single to multiprocessing

System designers can now tap the 40-MHz, 29-MIPS power of SPARC processors and skip the nonrecurring engineering (NRE) costs normally associated with designing a multiprocessing compute engine for a new product. Just select from any of three SPARCore modules that offer one or two onboard processors and built-in single or multiprocessing capability. By using these modules, system upgrades become a simple matter of changing daughter boards and loading a multiprocessing operating system.

The $1450 (1000) CYM6001K module contains one SPARC CPU and works in a single-processing environment. The other two modules are suitable for multiprocessing: The $3200 (1000) CYM6002K has two onboard SPARC processors; and the $1675 (1000) CYM6003K, which contains only a single SPARC, includes a multiprocessing cache-controller and memory-management unit that lets you plug multiple modules into your chassis.



Providing a selection of plug-in SPARC CPU modules, *the SPARCore boards ease multiprocessing system design by providing factory-tested processing in a field-upgradeable format.*

All three modules use the manufacturer's SPARC chip set, which includes a CY7C601 integer unit; a CY7C602 floating-point unit; either a CY7C604 or CY7C605 cache controller/memory-management unit; and CY7C157 16k×16-bit cache static RAMs. The modules come in a selection of 25-, 33-, and 40-MHz speeds and add a 4-kbyte page of virtual-memory management.

The 3.3×5.78-in. modules each have two power and two ground planes. Each board was designed using Spice simulation of critical paths for shorter interconnect delays. All components are surface mounted, and clamping diodes terminate the clock lines. Performance ranges from 32 to 59 MIPS and from 5 to 13 Mflops. Each of the modules plugs into a standard SPARC Mbus backplane.

The Mbus offers fully synchronous operation at 40 MHz with multiple-master and overlapped-arbitration capabilities. With 64-bit, multiplexed address and data paths, the Mbus facilitates shared-memory multiprocessor signals and transactions. The bus also provides for as much as 64 Gbytes of physical-address space and supports a write-invalidate, cache-consistency protocol.

By using this modular method for system design, the SPARCore boards reduce your design-cycle time. They also improve system quality and reliability because each module is tested by the vendor. Furthermore, the ease of upgrading lets you lengthen your product's life cycle by advancing to multiprocessing capability.—***JD Mosley***

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. FAX (408) 943-2796.

Circle No. 733

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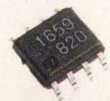

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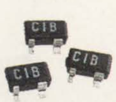

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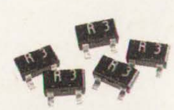

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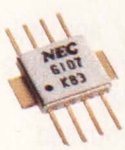

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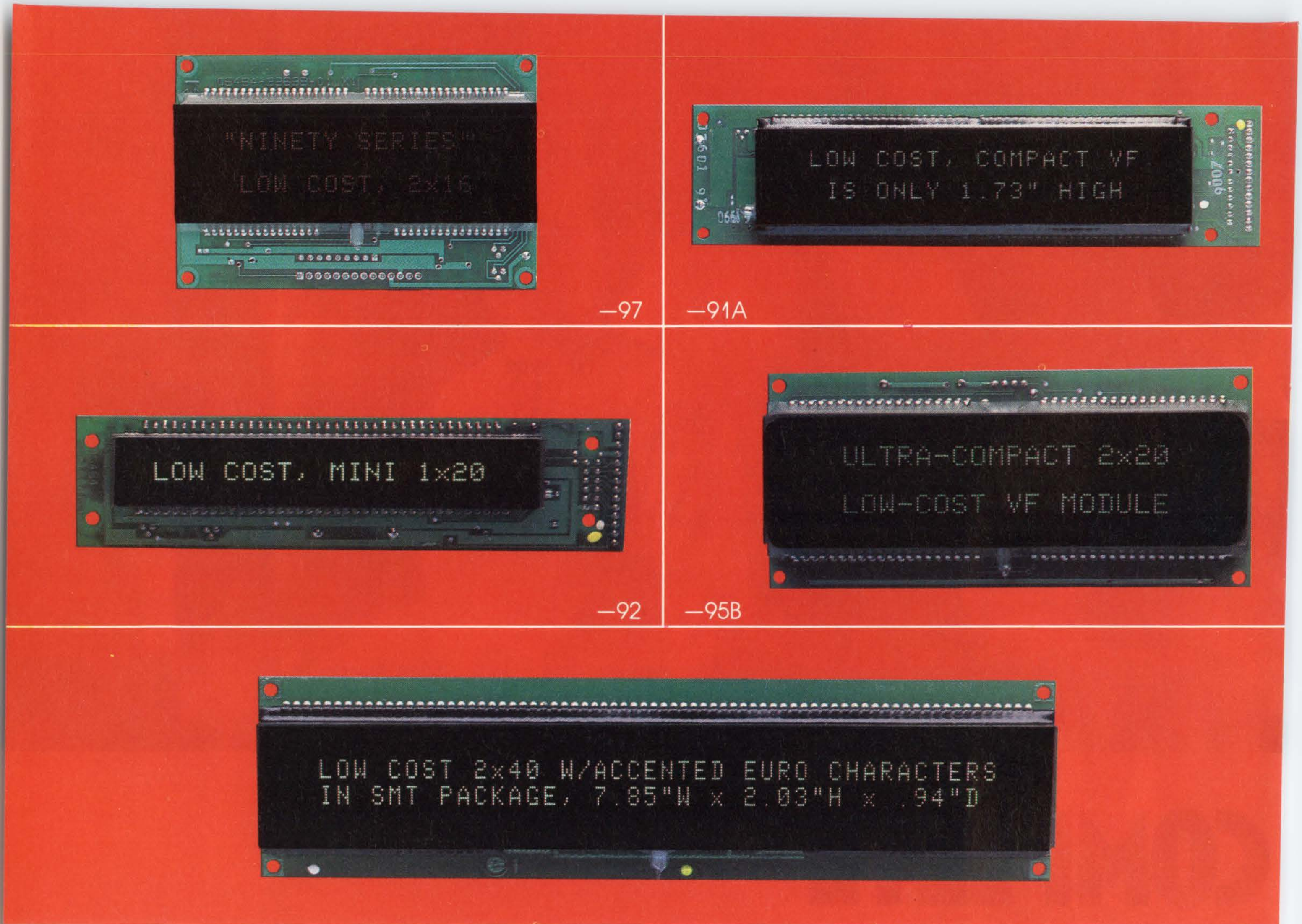

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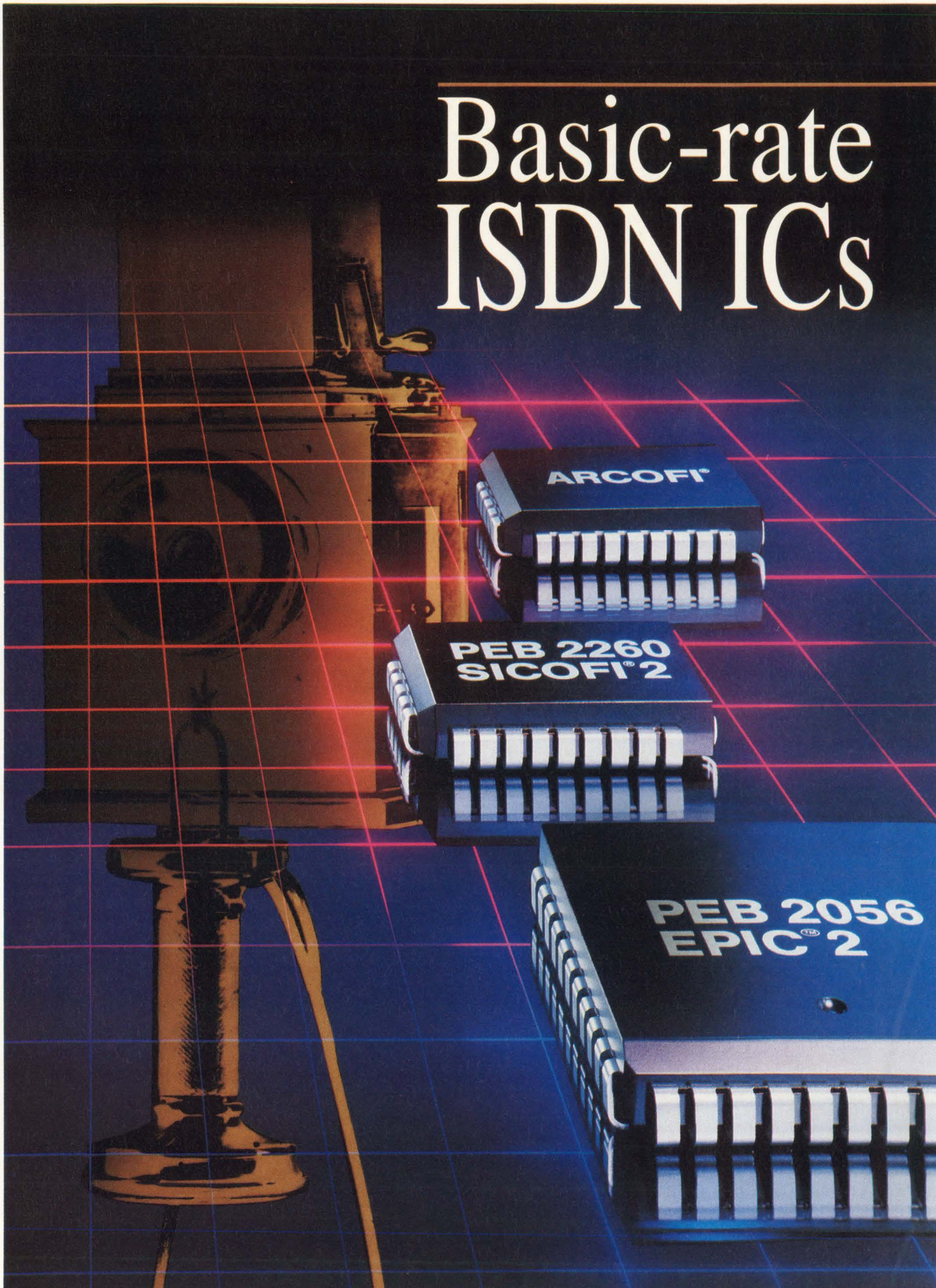
CIRCLE NO. 70

Basic-rate ISDN ICs



EDN Special Report

Brian Kerridge, *European Editor*

One objective of the Integrated Services Digital Network (ISDN) is to bring multiple channels of voice and data to small business and domestic users along a single twisted-pair wire.

Until recently, this part of the service, known as "basic-rate ISDN," failed to materialize. One of the reasons has been difficulty in designing vital ICs that reliably overcome transmission deficiencies of all twisted-pair configurations.

Now, a wider range of vendors offers these important ICs. Known as U- and S-interface ICs, some have a performance certified to operate over worst-case, twisted-pair wires. Vendors have reset prices too, down 5 to 10 times, to further attract the interest of telecommunications-equipment designers.

ISDN ICs have successfully developed past the laboratory and field-test phase, and now the commercial phase begins, says Flavio Benetti, network system manager with SGS-Thomson in Milan. Benetti reports a big increase in demand for ISDN ICs over the last 6 to 12 months.

The 160-kbps basic-rate service contains separate channels of two 64 kbps and one 16 kbps, called "bearer" and "data" channels, respectively (and known as 2B+D). Basic-rate service uses single twisted-pair wiring originally installed for phone communications in a 4-kHz baseband. The gross inadequacy of these wires for transmitting digital data limits the speed, capacity, and reach of ISDN. A key factor in realization of ISDN is the way IC designers exploit silicon to exploit copper. U- and S-interface ICs are prime examples of this ingenuity and combine VLSI, mixed-mode ASIC, and DSP technologies. For background on the difficulties of transmitting digital data along twisted pairs and an outline of the compensation techniques today's ICs employ, see **box**, "Straightening out twisted pairs."

Considering the ambitious objectives of ISDN, it's no surprise the system did not develop overnight. Jim Pickard, ISDN marketing manager with British Telecom, cites earlier absence of solid standards and lack of approved equipment as the main reasons for the general delay in launching an ISDN system. British Telecom launched basic-rate

> The network of twisted-pair wires running along our walls and streets is an unsuitable transmission medium for digital data. But with millions of miles of copper already in place, overcoming the gross deficiencies of this widest of wide-area networks presents IC designers with an alluring and supreme challenge.

ISDN in January this year, and around 700 towns and cities in the UK offer access. At present, equipment approved by the British Approvals Board for Telecommunications is available for fax, teleconferencing, and PC communications. Several ISDN telephones are in the approval pipeline and should be available later this year. Pickard expects ISDN to attract mainly business users, who show an increasing demand for data services. ISDN telephones will appear though, almost by default, and in time he expects phone communications to be the main ISDN service. In his view, there is a major requirement now for stand-alone terminal-adapter equipment

Basic-rate ISDN ICs let you use old single twisted-pair lines for multiple channels of voice and data communications. (Photo courtesy Siemens)

The 2B1Q line code is mandatory in the US, and likely to supersede other line codes in use elsewhere.

as users realize the possibilities of connecting existing products to ISDN. This requirement will eventually disappear as more products include ISDN interfaces as standard. Pickard emphasizes that ISDN is now set to become the preferred customer interface into British Telecom's network, and most definitely has a long-term future.

ISDN communication within national boundaries is a reality, but international ISDN is still to be completely implemented. Even in Europe, ISDN services between European Economic Community (EEC) member countries is not straightforward. The main difficulty results from a lack of common approval procedures for ISDN equipment, leading to noncompatibility at detail level. For example, some approvals in Germany conform to the CCITT Red Book, while in the UK it's the later issue Blue Book. In France, users can operate five equipments on one line; in the UK the number is eight.

The EEC's harmonization program addresses issues such as compatibility. But, with 26 phone companies in 18 countries operating at different stages of development, progress is slow. Member countries place great faith in a future "memo of understanding" agreement, known as Net 3, which promises to normalize principal differences by 1993.

ISDN products for basic-rate operation fall into generic categories with mundane titles of NT1 (network terminator), TE1 (terminal equipment), and TA (terminal adapter). A typical arrangement appears in **Fig 1**.

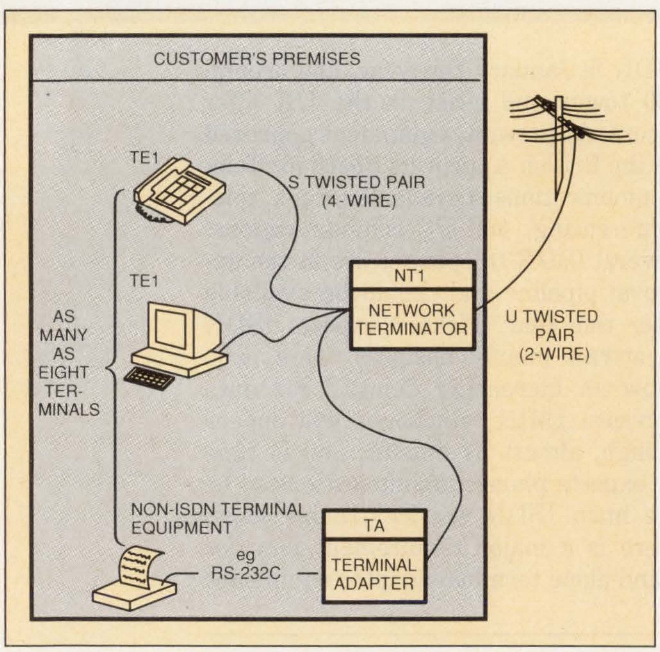
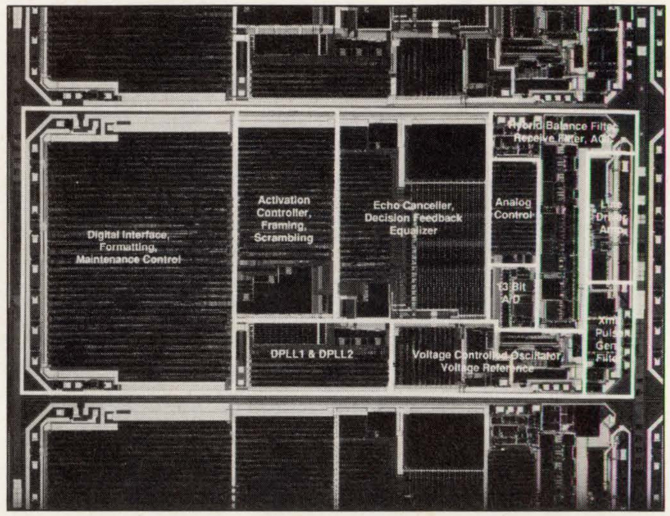


Fig 1—This diagram shows a typical arrangement of the main functional blocks for basic-rate ISDN.

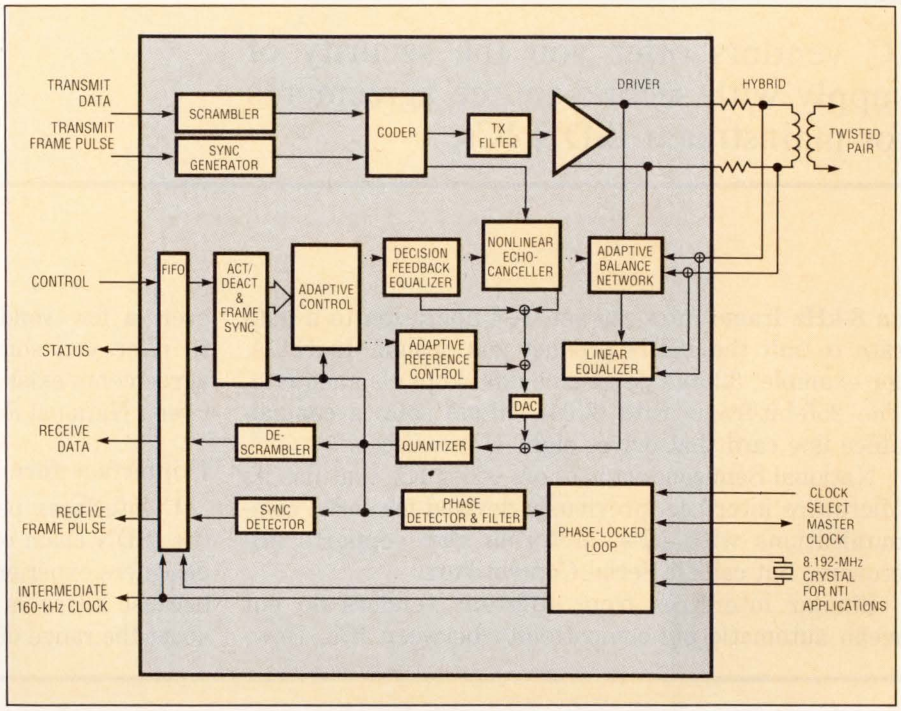


A single-chip U-interface IC is very complex. National Semiconductor's TP3410 is typical of the apportionment of silicon in these chips.

NT1 describes a wall box that forms a transition point between twisted-pair wires inside and outside your premises. NT1s contain the important U- and S-interface ICs, which together convert 2-wire 160-kbps data to 4-wire 192-kbps data. The U-interface IC also contains the circuit blocks to compensate for twisted-pair wire characteristics. An additional power-controller IC resides in an NT1 to convert incoming twisted-pair voltage to a 5V power-rail for the ICs.

TE1 describes the range of telephones, video phones, faxes, and computers that you may connect to ISDN. You can connect as many as eight TE1s to the same NT1. CCITT recommendations cater to an assortment of wiring configurations, ranging from 1 km to 200m between one to eight TE1s, respectively. Each TE1 requires at least another S-interface IC in its internal ISDN section, together with dedicated-controller ICs for protocol handling and microcontroller interfacing. If the TE1 is an audio terminal, then a codec IC is an additional requirement.

In theory, it's possible for terminal equipment to house a U interface, enabling direct connection to street wiring. This arrangement obviates the need for an NT1 terminal box. In practice, European phone companies do not permit this arrangement, as NT1s are phone-company property and are a mandatory requirement. Other countries, such as the US, have less



The complexity of a single-chip U interface is illustrated by Level One's LTX500. This interface includes an on-chip adaptive-balance network (ABN), which optimizes performance of the hybrid and reduces the need for accurate components external to the IC.

stringent views on NT1s, and the temptation exists to eliminate the cost of this item for small-scale users. ISDN PC plug-in interfaces that also contain phone links seem likely products to fill this application.

The last category of basic-rate ISDN products specifies a TA for linking non-ISDN telecommunications products into ISDN. A TA includes ICs used in TE1s. In addition, a bit-rate adapter IC translates bit-rates of other data-service standards, such as RS-232C, V.24, X.21, and X.25, into ISDN format. **Tables 1** and **2** show examples of ICs suitable for basic-rate designs.

ICs use different serial links

Distinctions between ICs from different vendors are not only in their ability to meet drive and sense requirements of twisted-pair wires, but also in different methods of interfacing the ICs themselves.

Vendors adopt a variety of methods for communicating between ICs at the pc-board level. All methods use some form of serial bus communication, synchronized to ISDN data rates. Typically, the interface employs two data lines and two control lines. Selecting a proprietary interfacing method does not necessarily lock you to one vendor. A serial interfacing technique for ISDN ICs described as General Circuit Interface (GCI), was devised by European manufacturers Alcatel, Italtel, Plessey, and Siemens to avoid this situation. Currently, ICs from Mietec, National Semiconductor, Siemens, and SGS-Thomson support the GCI. (Siemens calls the GCI IOM-2 (ISDN-oriented modular) and Mietec calls it V*). The GCI uses a message-based serial system that packs 32, 90, or 256 bits into

Table 1—Representative U-interface ISDN ICs

Manufacturer	Part number	Line-code	Features	Price
Advanced Micro Devices	Am2091	2B1Q	GCI compatible, 340 mW typ, 44-pin PLCC[1]	$45 (1000)
AT&T	T7262A T7263	2B1Q	Dual chip set, K2 serial interface, both in 44-pin PLCC	$18.50 (10,000)
	T7264	2B1Q	K2 serial interface, 275 mW typ, 44-pin PLCC	$27 (10,000)
Level One Communications	LXT500	2B1Q	Next margin 3 dB on ANSI loops 1 to 3, 6 dB on loops 4 to 15; adaptive hybrid-balance network; 300 mW typ; 28-pin DIP or PLCC	$35 (10,000)
Mietec	MTC2071	4B3T	GCI compatible, 250 mW max, 28-pin DIP or PLCC	$20 (10,000)
Mitel	MT8910	2B1Q	250 mW typ, 28-pin DIP or 44-pin PLCC	$55 (1000)
Motorola	MC145472	2B1Q	Next margin 1 dB on ANSI loop 1, 6 dB on loop 2, 5 dB on loop 3; 68-pin ceramic quad flatpack	$49.59 (1000)
National Semiconductor	TP3410	2B1Q	GCI or Microwire interface selectable, adaptive hybrid balance network	$60 (1000)
Philips	PCD2392HP PCD2393T	2B1Q	Dual chip set, GCI compatible, 300 mW typ, samples end 1991	$20 (10,000)
SGS-Thomson	ST5110	2B1Q	GCI or Microwire interface selectable, adaptive hybrid balance network	$35 (10,000)
Siemens	PEB2091	2B1Q	GCI compatible, 300 mW max, 44-pin PLCC	$35 (10,000)

Note: 1. PLCC=plastic leaded chip carrier.

IC vendors offer you the security of supply with second-source agreements for mainstream ISDN ICs.

an 8-kHz frame. You can set GCI operation to a data rate to suit the ISDN product you design. In NT1s, for example, 32 bits per frame (256 kbps) is adequate. The 256-bit/frame rate (2.048 Mbps) suits a central-office line card that drives eight U interfaces.

National Semiconductor offers other ICs that use its Microwire interface, previously devised for serial communications with μPs. Motorola also supports Microwire, but calls it Serial Control Port.

Similar interfaces from different vendors do not mean automatic pin compatibility between ICs. However, a few vendors have second-source agreements to offer you some assurance of supply. Currently, agreements exist between AMD and Siemens, and between National Semiconductor and SGS-Thomson.

U interface forms vital link

U interfaces perform the most critical functions in the ISDN chain of communication. It is here where IC designers experience the greatest challenge, especially, because there is a shortage of detailed information about the range of twisted-pair characteristics. The Am-

Straightening out twisted pairs

The twisted-pair line from your premises to the central office (in Europe, the exchange) presents a variety of obstacles to the smooth transmission of 160-kbps data streams. Principal difficulties arise from attenuation, crosstalk, and variations in characteristic impedance.

At ISDN (Integrated Services Digital Network) basic-rate frequencies, attenuation is not severe. Around 8 dB/km of attenuation at 100 kHz is typical, depending on wire gauge. The average distance a twisted pair carries data along the street is 5 km, giving rise to an end-to-end attenuation of 40 dB.

Crosstalk results from signals coupling your line to a bunch of adjacent lines in the network. As your line nears the central office, more and more lines come close, and cross-coupling becomes a limiting factor governing the maximum transmission distance. The length of the line becomes critical when the magnitude of your attenuated signal matches the magnitude of a stray cross-coupled signal.

Both attenuation and crosstalk effects increase with the frequency content of the digital data stream. Although basic-rate ISDN must transport a 160-kbps data rate, designers play tricks with line coding to reduce the baud-rate bandwidth and frequency of the signal.

Techniques for line coding involve translating sequential sets of bits in the data stream into discrete signal-amplitude levels. Both U and S lines in an ISDN utilize line coding, but the effects are more beneficial on the longer U lines. CCITT (Consultative Committee on International Telegraphy and Telephony) standards specify line codes for S interfaces, with the objective of making customer-premise equipment globally compatible. U interfaces are country specific, and as yet, only ANSI in the US has specified the line interface (2B1Q).

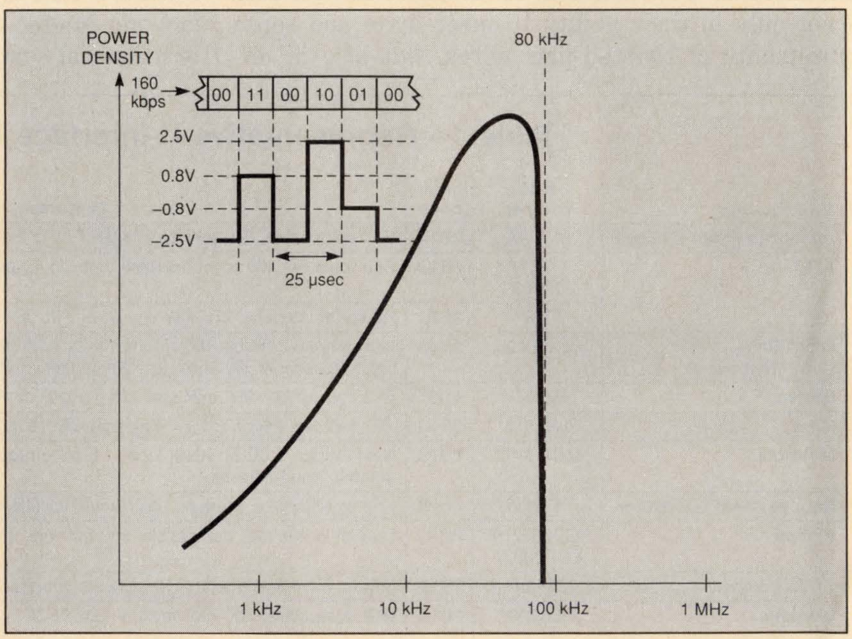


Fig A—The 2B1Q line code restricts frequency components of 160-kbps data to below 80 kHz.

erican National Standards Institute (ANSI) has specified 15 typical twisted-pair configurations—ANSI TI.601/1991. These configurations represent the toughest loops any U-interface is likely to connect to in the US. In the absence of specifications elsewhere, the ANSI requirement is currently accepted as an international guideline. The European Telecommunications Standards Institution (ETSI), is working on an equivalent specification for typical European loops. Publication of the specification is expected before the end of 1991.

Several vendors frankly admit difficulties in meeting ANSI-specified performance for all loops in early versions of U interfaces. Even in new-generation ICs, vendors disagree over some aspects of U interface design. The main differences of opinion relate to single-chip vs 2-chip examples, and to the merits of on-chip vs off-chip hybrid components.

So-called U-interface, single-chip solutions means integration of analog circuits that interface to the twisted pair, with digital blocks for communicating serially with other ICs in the chain. The basic disagreement is whether proximity of digital signals to highly sensi-

Experts generally agree 2B1Q line coding offers the best compromises, but other line codes operate satisfactorily elsewhere. Essentially, a 2B1Q waveshape offers the best compromise between crosstalk limit and circuit complexity when driving a typical twisted-pair wire.

The 2B1Q line code involves translating sequential pairs of bits into four voltage levels (+2.5, +0.8, −0.8, and −2.5V) at the transmitting end of the twisted-pair wire. The net effect of this line code is to limit frequency components in the transmitted waveform to well below 80 kHz (**Fig A**). Compressing the frequency components in this way reduces attenuation and crosstalk, thereby increasing the range of a twisted-pair wire.

An undesirable by-product of using a line code such as 2B1Q is the distortion experienced by the pulse, because of the presence of more low-frequency components. The distortion shows up particularly as long trailing edges to the pulses. Distortion is sufficiently acute that one pulse can run into another, an effect usually described as intersymbol interference (ISI).

To combat ISI, all U interfaces include equalization filtering in the receive path to restore pulse shape. The equalization filter often takes the form of an FIR-adaptive digital filter having around 25 taps. A key feature of the filter is its adaptive nature to modify its response with variations of cable characteristics, often referred to as a decision feedback equalizer (DFE).

As if this level of complexity were not enough, other characteristics of twisted-pair transmission cause a need for compensation. A major requirement of the U interface is that it operates in full-duplex mode. This requirement means that the receiver must be kept clear of transmissions from the same end of the line in order to detect what may be a heavily attenuated signal from the far end. The transmit and receive ports of the U-interface IC are isolated by a balanced hybrid, consisting of a transformer and resistive network. The hybrid is only partially effective in keeping the two paths separate because variations in characteristic impedance of the line destroys the balance. In practice, the hybrid inserts around 15 dB of isolation, although a worst-case figure may be as low as 6 dB. In consequence, a large chunk of transmitted signal bridges the hybrid, and must be canceled out in order to sustain duplex operation. In addition, echoes of transmission data reflect back to the receiver from discontinuities along the line. One of the main functions of a U-interface IC is to neutralize effects of hybrid unbalance and reflections. This function is called echo cancellation.

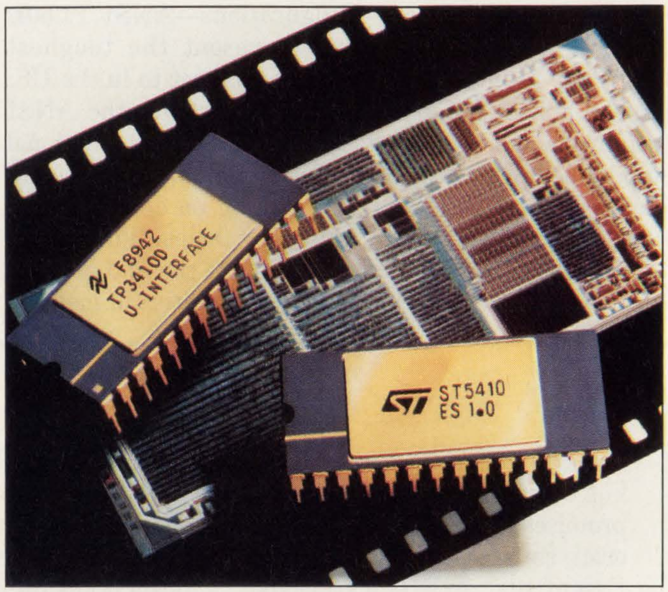
A second FIR filter handles echo cancellation. For optimal effect, the filter needs 60 dB of cancellation. An FIR adaptive filter similar to a DFE filter provides this function. An additional nonlinear adaptive filter helps to reduce the linearity required in the ADC and transmitter.

Acknowledgment

Thanks go to Simon Cox, group leader in Copper Access Systems with British Telecom, for suggesting many of the points in this box.

tive receiver circuitry degrades S/N ratio performance. Yves Durieux, telecommunications IC marketing manager with Philips, has no doubt that 2-chip versions are superior. He says Philips' measurements show consistently better results in loop tests using a 2-chip interface. He maintains IC users also benefit from different production-test methods associated with 2-chip designs. This approach leads to optimal yield and cost figures for the complete U-interface function. He claims that additional pc-board area taken up by two chips is relatively small in comparison to area needed for more complex hybrids and additional microcontrollers in other designs.

According to Jerrell Hein, marketing manager for ISDN basic-rate ICs with AT&T, the company's newly released T7264 single-chip U interface shows better margin against ANSI loop-test specifications than its earlier 2-chip alternative. Hein points to other single-chip advantages, such as lower power consumption. The T7264's typical power consumption is 275 mW as compared with around 800 mW for a dual-chip version.



Several vendors have second-source agreements to supply single-chip U interfaces, such as National Semiconductor, SGS-Thomson, AMD, and Siemens.

Hybrid design may be important

The term hybrid refers to a network of passive components that connects separate transmit and receive channels of a U interface to a single twisted-pair line.

National Semiconductor's TP3410 and SGS-Thomson's ST5410 single-chip U interfaces include some hybrid line-balance components on chip. You still need to mount seven resistors and the line interface transformer externally to the chip. Three of the resistors currently specify 0.1% tolerance, although SGS-Thomson intends to relax this requirement. The TP3410 and ST5410 also include two PLL circuits, instead of the single PLL offered by most vendors. When you design an NT1, you need two PLLs; one to synchronize with the incoming clock signal, and the other to measure frame-signal delay.

Table 2—Representative S-interface ISDN ICs

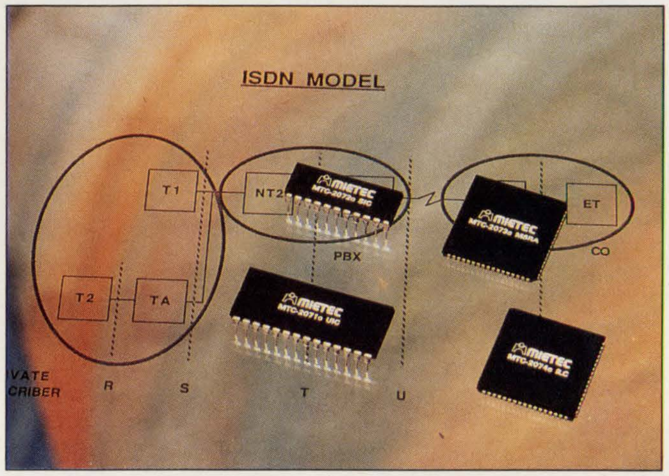
Manufacturer	Part number	Features	Price
Advanced Micro Devices	Am2080	GCI compatible, 60 mW max, 28-pin PLCC[1]	$8.45 (1000)
	Am2081	GCI compatible, adaptive equalizer, 80 mW max	$10.65 (1000)
AT&T	T7250B	Optimized for TE applications, 44-pin PLCC	$7.87 (10,000)
	T7252A	Optimized for NT applications, 44-pin PLCC	$8.83 (10,000)
Mietec	MTC2072	GCI compatible, 22-pin DIP or PLCC	$4.95 (10,000)
Mitel	MT8930	High-level digital link control, Intel and Motorola μP-compatible 8-bit port	$12.60 (1000)
Motorola	MC145474	2.5-km point-to-point range, 22-pin DIP	$7.42 (1000)
National Semiconductor	TP3420	Microwire interface, 1.5-km point-to-point range, adaptive equalizer receiver, 75 mW typ	$12.50 (1000)
SGS-Thomson	ST5420	Microwire interface, 1.5-km point-to-point range, adaptive equalizer receiver, 75 mW typ	$8 (10,000)
	ST5421	GCI compatible, 1.5-km point-to-point range, adaptive equalizer receiver, 75 mW typ	$8 (10,000)
Siemens	PEB2085	GCI compatible, includes link-access-protocol on D-channel, 44-pin PLCC	$11 (10,000)

Note: 1. PLCC=plastic leaded chip carrier.

Manfred Omenzetter, ISDN IC specialist with Siemens in Munich, believes strongly that all components of a hybrid should be external to the U-interface chip. In his view, totally external components offer you the opportunity to optimize performance to a wider range of loops. This arrangement also means that the highest tolerance resistor becomes 1%, as in the case of the hybrid for the company's PEB2091 single-chip interface. Omenzetter stresses though that all hybrid circuits need careful design. The line-balance transformer is particularly important and often troublesome to manufacture. He explains that using 2B1Q line code, a transformer must operate linearly with dc current to 80 mA. The pc-board layout in the region of the hybrid is another factor affecting performance. You must adopt methods normally associated with much higher-frequency designs, such as symmetrical layout, maximum separation from clock and other digital lines, and meticulous attention to decoupling and grounding.

Not all U-interface ICs demand such high precision for hybrid components. AT&T's T7264 uses just two external 1% resistors with a line-balance transformer. This design anticipates low-balance performance of only 3 dBs from the hybrid, but relies on enhancements in the echo-cancellation loop to restore overall performance.

Andrew Sorowka, product marketing manager at Level One Communications, explains how the company's LTX500 U interface gets away with a transformer and two 5% resistors for its hybrid arrangement. The IC design uses a dedicated compensation arrangement for first-order echo precancellation. Called adaptive-balance network, the on-chip hybrid achieves around 25-dB cancellation for cables of different characteristic impedance. Sorowka believes single-chip U interfaces exemplify a steady trend to further functional integration in ISDN circuits. He says next-generation ICs will see integrated versions of complete ISDN functions such as an NT1. Level One Communications already has an integrated NT1 at design phase and expects first samples in late 1992.



Many basic-rate ISDN ICs use general circuit interface (GCI) for interchip communication. Mietec calls the interface V*.

Essential for the development of any product using a U interface is a vendor's pc-board evaluation kit. Boards contain peripheral components needed to make up a product and provide an example of pc-board layout. Most evaluation kits come as a PC plug-in board with chip drivers and development software. Cost ranges from $500 to $2000, although AT&T will lend you its kit free of charge.

S lines cause less fuss

Communicating along 4-wire lines, S twisted pairs that make up the internal wiring of your premises are much less of a design headache than using 2-wire U lines. In the first place, the 4-wire arrangement keeps

Acronyms used in this article

ABN—Adaptive-balance network
ADC—Analog-to-digital converter
AMI—Alternate-mark inversion
ANSI—American National Standards Institute
ASIC—Application-specific integrated circuit
CCITT—Consultative Committee on International Telegraphy and Telephony
Codec—Coder/decoder
DSP—Digital signal processing
DFE—Decision feedback equalizer
EEC—European Economic Community
ETSI—European Telecommunications Standards Institution
FIR—Finite impulse response
GCI—General circuit interface
ISDN—Integrated Services Digital Network
ISI—Intersymbol interference
Net 3—"Memo of understanding" agreement between EEC member countries for ISDN compatibility
NT1—Network termination 1
PC—Personal computer
PLL—Phase-locked loop
S interface—Communicates over internal twisted pairs
S/N ratio—Signal-to-noise ratio
TA—Terminal adapter
TE1—Terminal equipment 1
TE2—Terminal equipment 2
U interface—Communicates over external twisted pairs
VLSI—Very large-scale integration

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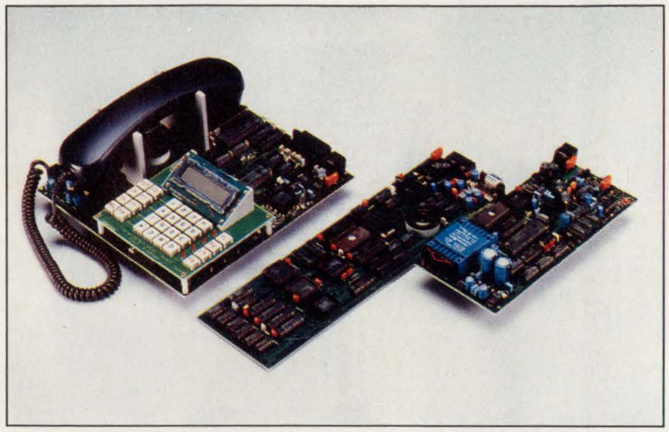
transmit and receive lines separate, obviating the need for a hybrid, and limiting line lengths to around 1 km. ISDN objectives require Sbus equipment to be compatible internationally. Therefore, all S-interface ICs conform to the same line code, called alternate-mark inversion (AMI). CCITT recommendation I.430 covers typical Sbus configurations and noise sources.

Despite less severe line conditions, National Semiconductor's TP3420 and SGS-Thomson's 5420 S interface still includes an adaptive equalizer to counteract pulse distortion on the line. This feature extends performance to 1.5-km point to point.

Normally, vendors offer you the same S-interface IC for all your ISDN applications, although this arrangement leaves you with redundant protocol logic associated with one or the other end of an Sbus. AT&T avoids this situation by optimizing the use of silicon



You can build an integrated services terminal (IST) bus as an extension to the ISDN Sbus using Philips' PBC2310 interface IC. The IST bus lets you concurrently communicate locally and externally without the need for a local exchange.

Manufacturers of ISDN ICs

For more information on basic-rate ISDN ICs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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in two different versions of S interface. The design of ICs T7252A and T7250B match precisely the requirements of NT1s and TE1s, respectively.

As an adjunct to an ISDN Sbus, Philips offers a PBC2310 IC to let you build an alternative local communications network between end-user terminals. Philips calls this network integrated-services terminal (IST) bus. The network carries nine 64-kbps channels, in contrast to ISDN's two 64-kbps B-channels, and one 16-kbps D-channel. This structure lets you operate 31 terminals on IST, instead of the normal eight on ISDN. Also, you can communicate locally and externally simultaneously—not possible with ISDN without a local exchange. Another advantage is that four separate data transfers run concurrently before further access is blocked. With ISDN, just one internal phone-to-phone conversation per Sbus blocks the system. Another significant difference is that IST operates in duplex mode along 300m of a single twisted pair, instead of the normal 1-km, 4-wire arrangement for ISDN. Philips intends IST to complement rather than compete with ISDN. The PCB2310 ($15 (10,000)) IST bus interface IC lets you build a gateway from IST to an ISDN Sbus, or to an existing analog phone system. EDN

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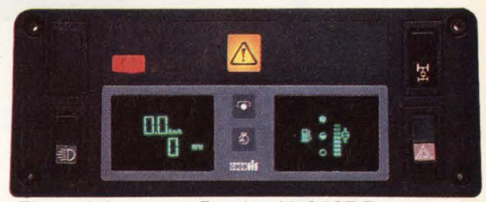

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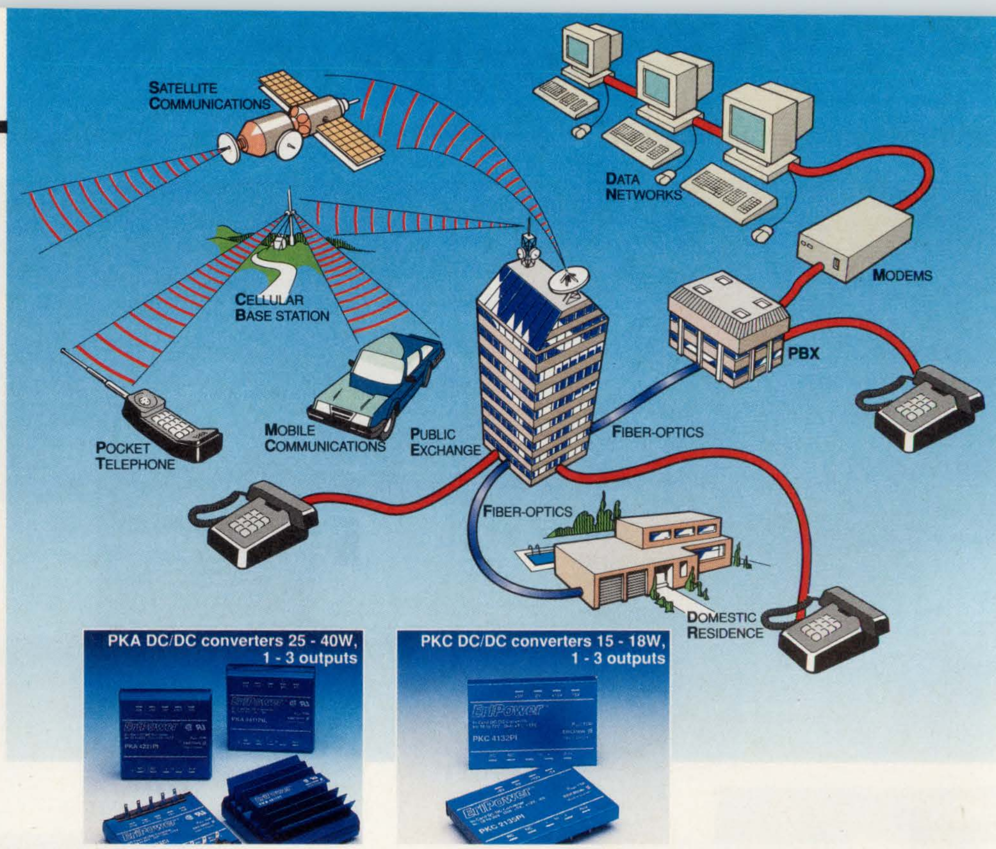

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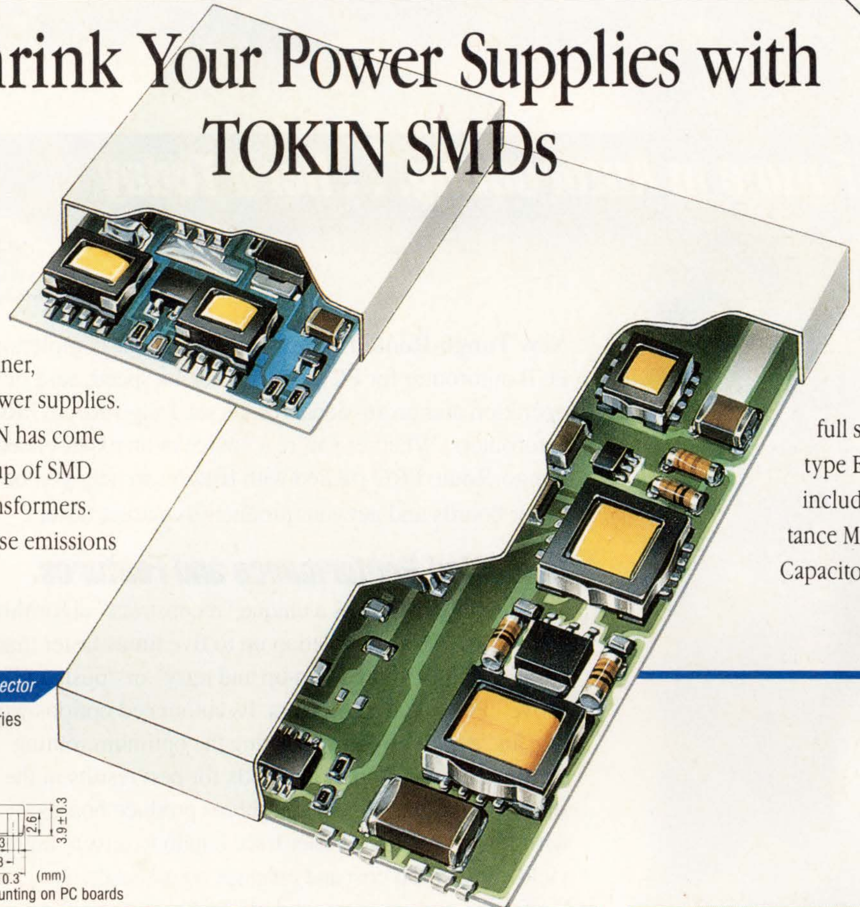

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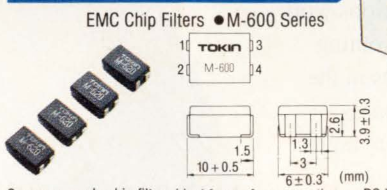

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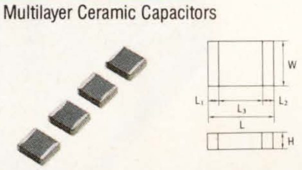

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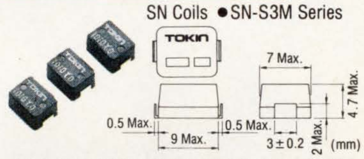

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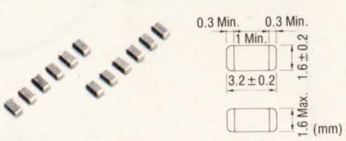

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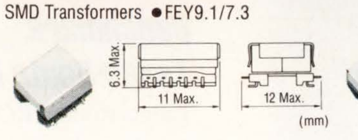

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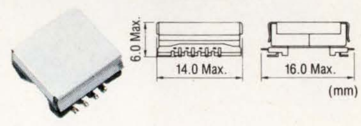

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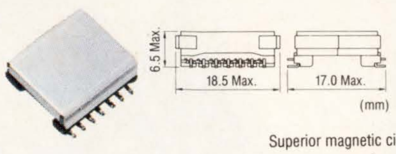

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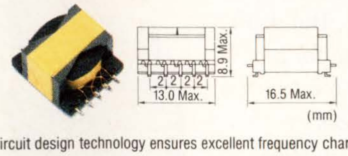

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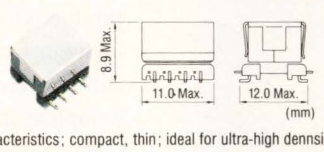

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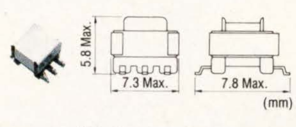

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THE

JIM WILLIAMS

PAPERS

Subduing high-speed op-amp problems

The application of high-speed op amps requires special attention to a multitude of potential problems. You need to guard against noise intrusion, capacitance-loading effects, and parasitic conductive paths—without neglecting the compromises you may have to make between compensation and gain.

Jim Williams, *Linear Technology Corp*

Compared with their low-speed siblings, high-speed op amps are subject to many problems, many of which can result in oscillation. The forte of the operational amplifier is negative feedback, which stabilizes the operating point and fixes the gain. However, positive feedback or delayed negative feedback can cause oscillation. Thus, even a properly functioning amplifier constantly lives in the shadow of oscillation.

When oscillation occurs, several major candidates for blame are present. If the power supply is unbypassed, the impedance the amplifier sees at its power terminals is high, particularly at high frequency. This impedance forms a voltage divider with the amplifier, letting the supply vary as internal conditions in the amplifier change. This variation can cause local feedback, resulting in oscillation. The obvious cure is to bypass the amplifier. Power-supply impedance must be low to ensure stable operation.

A second common cause of oscillation is positive feedback. In most amplifier circuits feedback is negative, although the circuit may also use controlled amounts of positive feedback. In a circuit that normally has only negative feedback, unintended positive feedback may occur with poor layout. Check for possible parasitic feedback paths and unwanted or overlooked feedback action. To the extent possible, minimize the impedances seen by the amplifier inputs. A low impedance helps to attenuate the effects of parasitic feedback paths to the inputs. Similarly, minimize exposed input-trace area. Route the amplifier outputs and other signals well away from sensitive nodes. Sometimes no amount of layout finesse will work, and shielding is required. Use shielding only when required—extensive shielding is a sloppy substitute for good layout practice.

Watch out for time delays

A third cause of oscillation is negative feedback that arrives significantly delayed in time. Under these conditions, the amplifier hopelessly tries to servo-control a feedback signal that consistently arrives "too late." The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point. The most common causes of this problem are reactive loading of the amplifier (most notably capacitive loads such as cable) and circuitry (such as power amplifiers) within the amplifier's feedback path. In many cases, isolating the reactive load from the amplifier's output (and feedback path) with a resistor will solve the problem. Sometimes rolling off the amplifier's frequency response will fix the problem, but in high-speed circuits this may not be an option.

Placing power-gain or other types of stages within the amplifier's feedback path adds time delay to the stabilizing feedback. If the delay is significant, oscillation commences. Stages operating within the amplifier's loop should have a minimum time lag compared with the amplifier's speed capability. At lower speeds, this is not too difficult, but a stage within a 100-MHz amplifier's loop must be fast. As mentioned before, rolling off the amplifier's frequency response eases the job, but is usually undesirable in a wideband circuit. You should make every effort to maximize the bandwidth of the added stages before resorting to amplifier roll-off. In this way, you can achieve the fastest overall bandwidth while maintaining stability. (See the **box,** "The oscillation problem and frequency compensation," which discusses power-gain stages and other types of stages operating within amplifier loops.)

In certain cases, it may appear that there is an oscillation problem when there really isn't. For example, the low-level, square-wave output in **Fig 1** appears to suffer from parasitic oscillation. In actuality, the disturbance is typical of that caused by fast digital clocking or switching-regulator noise getting into critical circuit nodes. Plan for parasitic radiative or conductive paths and eliminate them with appropriate layout and shielding.

The **Fig 2** display underscores the previous statement. The scope trace shows the output from a gain-often inverter with a 1-kΩ input resistance. The output exhibits severe peaking induced by only 1-pF of parasitic capacitance across the 1-kΩ resistor. The 50Ω-terminated input source provides only 20 mV of drive, but that's more than enough to cause problems, even with only 1 pF of stray coupling. In this case the solution was a ground-referred shield at a right angle to, and encircling, the 1-kΩ resistor. Plan for parasitic radiative paths and eliminate them with appropriate shielding.

Too low a gain can cause problems

A decompensated amplifier running at too low a gain produced the oscillation shown in **Fig 3**. The penalty for a decompensated amplifier's increased speed is a restriction on the minimum allowable gain. Decompensated amplifiers are simply not stable below some (specified) minimum gain, and no amount of wishful thinking will change this. Such oversight is common with these devices, although the amplifier never fails to remind the user. Observe gain restrictions when using decompensated amplifiers.

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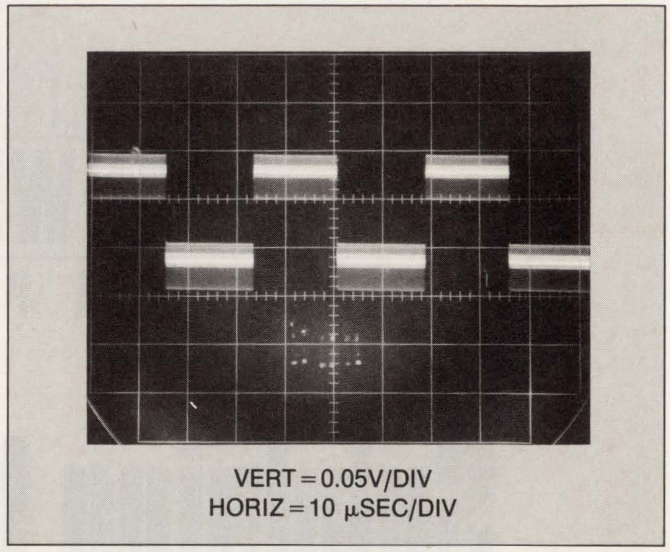

Fig 1—This square-wave output disturbance *is typical of switching-regulator noise at critical circuit nodes. Poor layout is the culprit.*

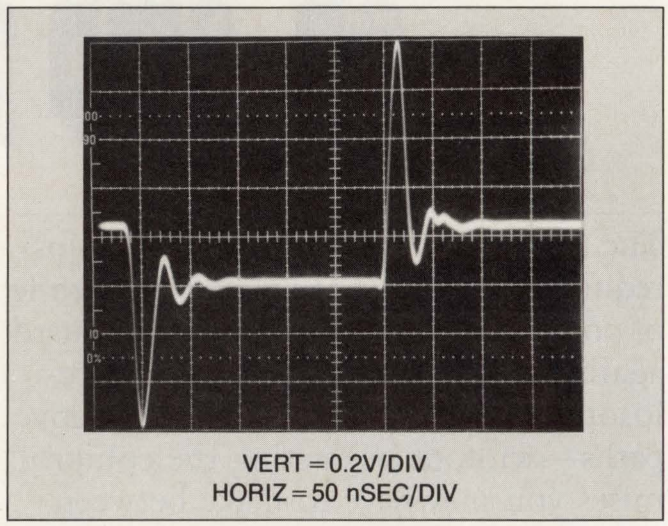

Fig 2—The peaking and ringing at the output of a 10× amplifier *is the result of only 1 pF of stray capacitance across a 1-kΩ input resistor.*

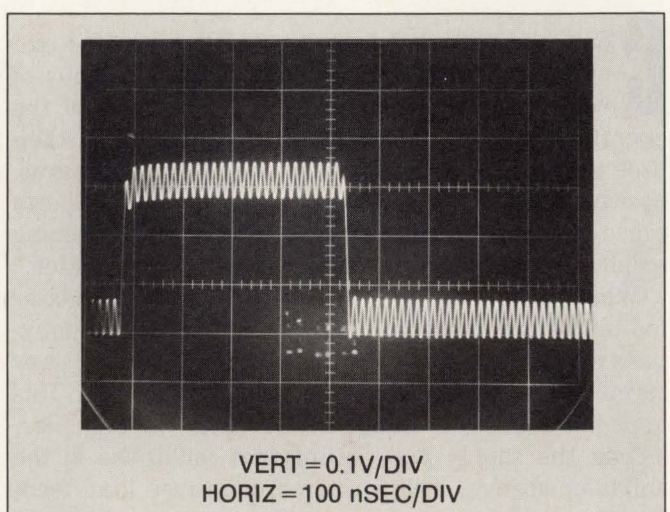

Fig 3—A decompensated amplifier running at low gain *produced this oscillation. Such amplifiers are not stable below a specified minimum gain.*

The oscillation problem and frequency compensation

All feedback systems have the propensity to oscillate. Basic theory tells us that an oscillator requires both gain and phase shift. Unfortunately, feedback systems, such as operational amplifiers, also have gain and phase shift. The close relationship between oscillators and operational amplifiers requires careful attention when designing op-amp circuits. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when you apply feedback. Furthermore, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This phase shift is why feedback-loop-enclosed stages can cause oscillation.

A large body of complex mathematics describing stability criteria is available, and is useful in predicting the stability characteristics of feedback amplifiers. For sophisticated applications, this complex approach is essential for optimum performance. However, comparatively little information is available that discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. The following is a practical approach to stabilizing various combinations of amplifier and power-gain stages, although the considerations are also useful to other feedback systems.

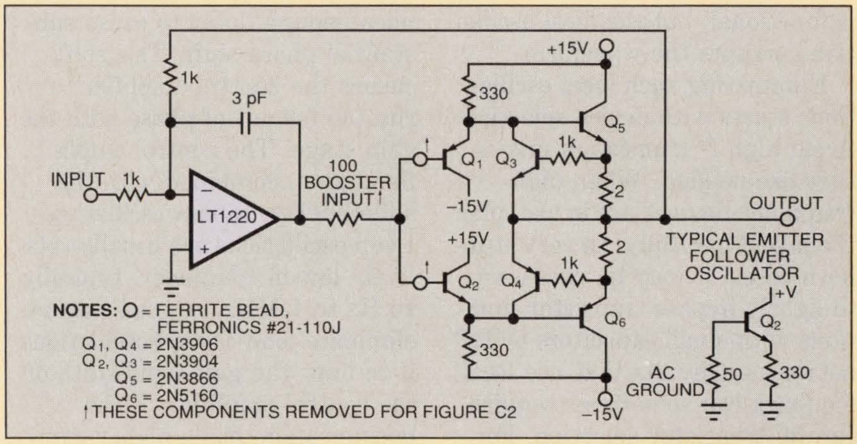

*Fig A—**In this booster circuit,** the 100Ω resistor and the ferrite beads at the inputs of Q_1 and Q_2 play a critical role in maintaining stability.*

Two categories exist

Oscillation problems in amplifier/power-booster combinations fall into two broad categories: local and loop oscillations. *Local* oscillations can occur in the booster stage, but should not appear in the IC op amp, which presumably was debugged prior to sale. These oscillations are the result of transistor parasitics, layout problems, or circuit-configuration instabilities. The oscillations are usually relatively high in frequency, typically in the 0.5- to 100-MHz range. Usually, local booster-stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation.

Fig A furnishes an instructive example. The Q_1 and Q_2 emitter-follower pair has a reasonably high f_T. These devices will oscillate if driven from a low-impedance source (**Refs 1** and **2**). To prevent problems, the 100Ω resistor and the ferrite beads are included to make the op amp's output look like a higher impedance. Q_5 and Q_6, also emitter followers, have an even higher f_T, but 330Ω sources drive them, eliminating the oscillation problem. The **Fig B** photo shows the action of the **Fig A** circuit without the 100Ω resistor and the ferrite beads. Trace A is the input, and Trace B is the output. The resultant high-frequency oscillation is typical of locally caused disturbances. Note that the major loop

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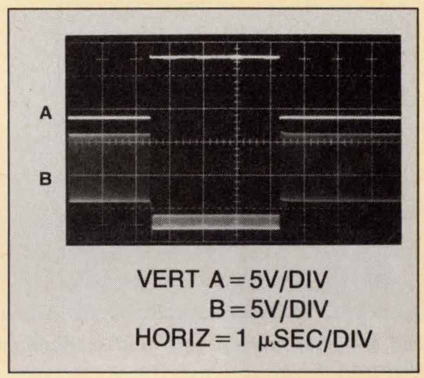


***Fig B—Removing the 100Ω resistor and the ferrite beads** from the **Fig A** circuit results in local oscillations, such as those shown here.*

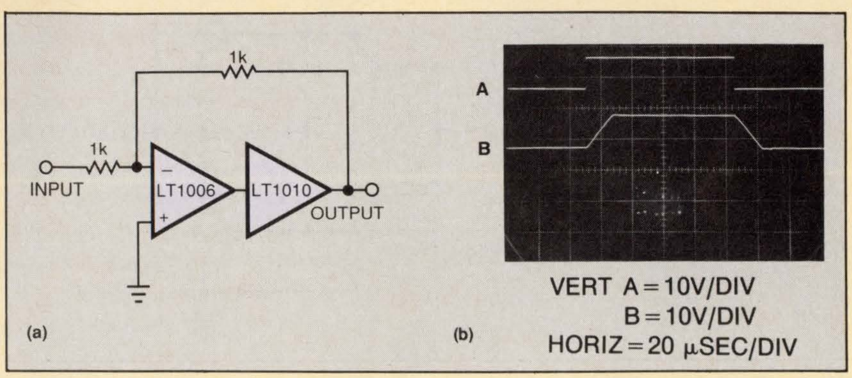


*Fig C—**This slow op amp and medium-speed booster (a)** produced the stable output shown in **b**.*

The oscillation problem and frequency compensation *(continued)*

is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high f_T transistors unless they are needed. When high-frequency devices are in use, plan the layout carefully. In very stubborn cases, it may be necessary to lightly bypass transistor junctions with small capacitors or RC networks. Circuits that use local feedback can sometimes require careful transistor selection. For example, transistors operating in a local loop may require different f_Ts to achieve stability. Emitter followers are notorious sources of oscillation, and should never be directly driven from low-impedance sources.

Loop oscillations are caused when the added gain stage supplies enough delay to cause substantial phase shift. This shift causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain, combined with the added delay, causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10 Hz to 1 MHz. A good way to eliminate loop-caused oscillations is to limit the gain-bandwidth of the control amplifier. If the booster stage has a higher gain-bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When the control amplifier's gain-bandwidth dominates, oscillation is ensured. Under these conditions, the control amplifier hopelessly tries to servo-control a feedback signal that consistently arrives too late, and the oscillation centers around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations, it is preferable to brutally force the compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling-off the control amplifier's gain-bandwidth. The feedback capacitor serves to trim only the step response; do not rely on it to stop outright oscillation.

Fig C illustrates these issues. The LT1006 amplifier used with the LT1010 current buffer produces the output shown in **Fig Cb**. As before, trace A is the input, and trace B is the output. The LT1006 has less than 1-MHz gain-bandwidth. The LT1010's 20-MHz gain-bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1006's internal roll-off is well below that of the output stage, and stability is achieved with no external compensation components. **Fig Da** uses the LT1223, which has a 100-MHz bandwidth, as the control amplifier. **Fig Db** shows the results. Here, the control amplifier's roll-off is well beyond the output stages, causing problems. The phase shift through the LT1010

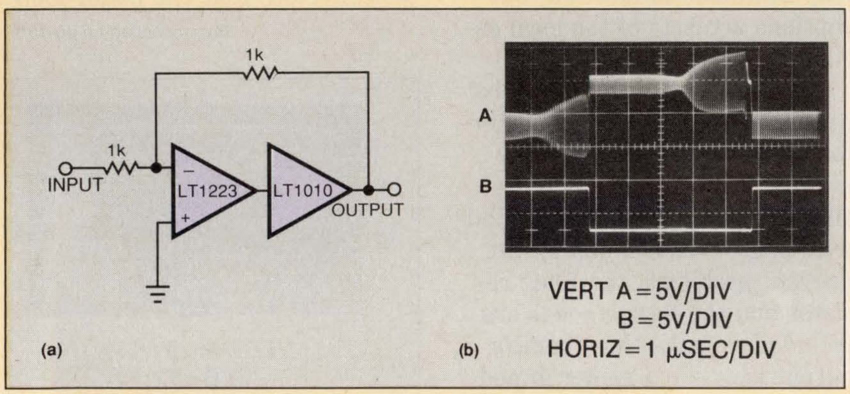


***Fig D—This fast op amp and medium-speed booster (a)** produced the oscillations shown in **b**.*

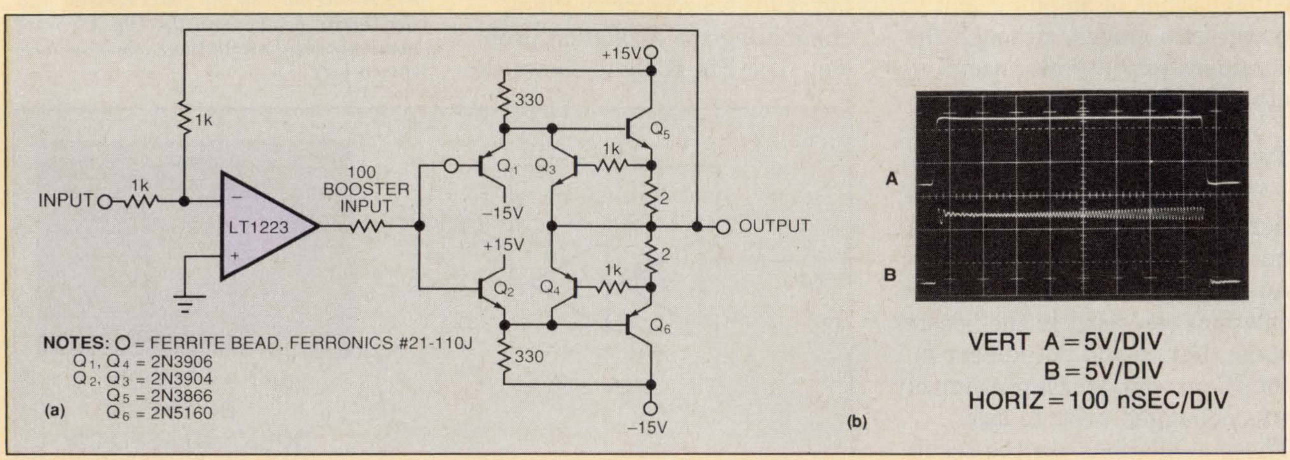


***Fig E—The fast amplifier and fast booster combination in a** attempts to correct the problems in the **Fig Da** circuit. Although the result is an improvement, the 100-MHz oscillation indicates that the booster stage is still too slow for the op amp **b**.*

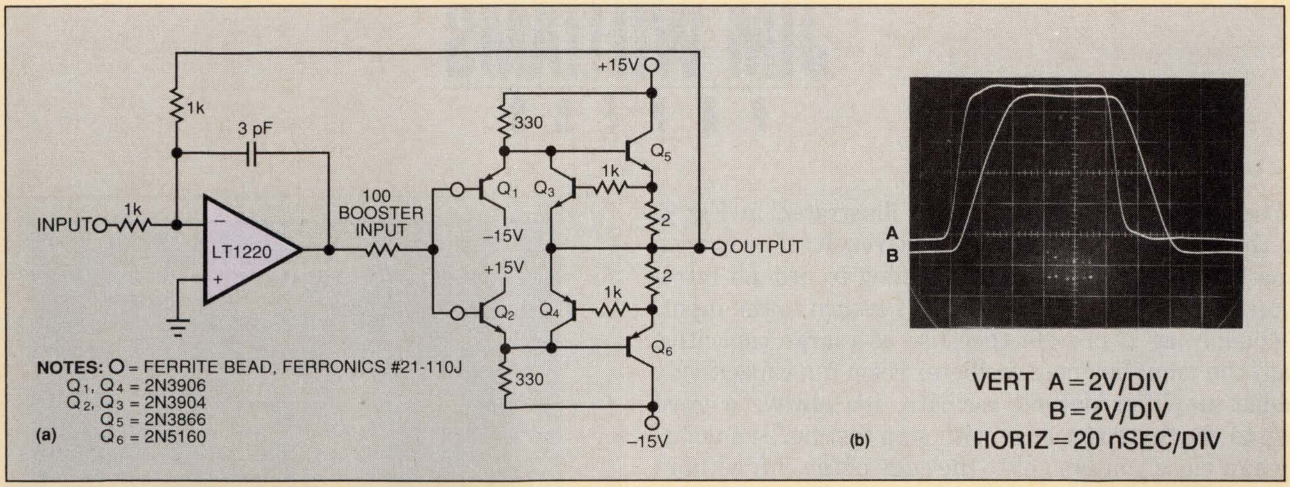


*Fig F—This circuit (a) produces more pleasing results than Fig Ea's circuit. The 45-MHz LT1220 replaces the 100-MHz LT1223. The slower amplifier now works well with the booster stage in its loop. The circuit is well controlled, with no sign of oscillation (**b**).*

is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the control amplifier's gain-bandwidth.

The fact that the slower op-amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is free. The faster amplifier requires roll-off components for stability. Practically, the LT1223's speed is simply too fast for the LT1010. A somewhat slower amplifier is the way to go. Alternatively, you could use a faster booster. The circuit of **Fig Ea** attempts using this faster booster, but doesn't quite make it. Although the result (**Fig Eb**) is less corrupted than before, the 100-MHz oscillation indicates that the booster stage is still too slow for the LT1223.

Nearly identical to **Fig Ea**, the **Fig Fa** circuit produces more pleasant results. Here, the 45-MHz LT1220 replaces the 100-MHz LT1223. The slower amplifier, combined with minimum (3 pF) local compensation, works well with the booster stage in its loop. The result (**Fig Fb**) is a high-speed output that is well controlled, with no sign of oscillations.

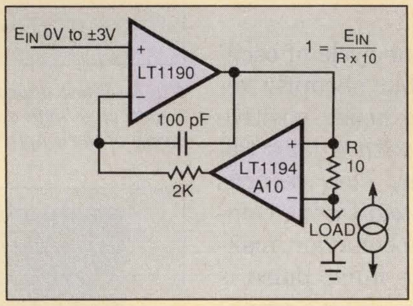


*Fig G—**This current source** uses a 40-MHz LT1194 with a gain of 10 and a 50-MHz LT1190. The 100-pF feedback capacitor ensures a fast, stable loop.*

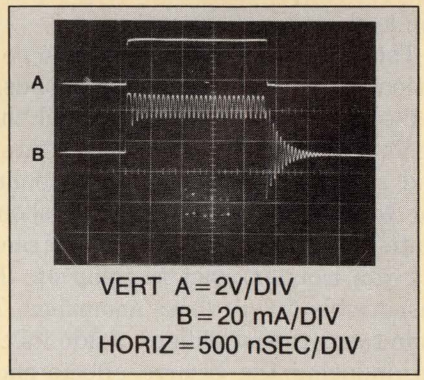


*Fig H—**Removing the 100-pF feedback capacitor** from the **Fig G** circuit subjects the op amp to phase-shifted feedback, causing the oscillation shown here. Put that capacitor back in.*

Power boosters are not the only things you can place within an amplifier's feedback loop. The **Fig G** current source is an interesting variation. There is no power booster in the loop, but rather a 40-MHz differential amplifier with a gain of 10. For stability, the circuit uses the 50-MHz LT1190. The local 100-pF feedback slows it down a bit more, and the loop is fast and stable. What happens if you remove the 100-pF feedback path? **Fig H** shows that the loop is no longer stable, because the LT1190 control amplifier cannot servo-control the phase-shifted feedback at the higher frequency. So, put that 100-pF capacitor back in.

Even if you broke the output-input connection between the LT1190 and the LT1194 and inserted a booster stage, the circuit would still be stable—if you retained the 100-pF feedback capacitor. This tells us that the control amplifier doesn't care what generates the causal feedback between its input and output, as long as there isn't excessive delay.

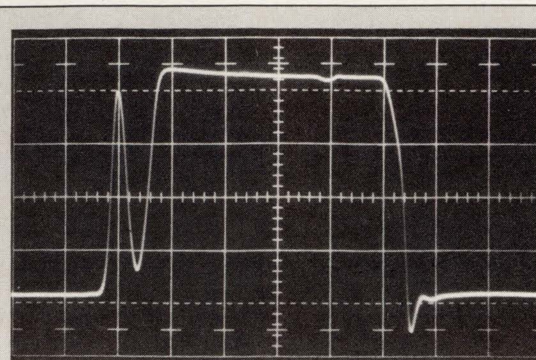
When compensating loops like these, remember to investigate the effects of various loads and operating conditions. Sometimes a compensation scheme that appears to be proper gives bad results for some conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

Oscillation is also the problem illustrated in **Fig 4**. In this case, the oscillation is a result of excessive capacitive loading. Capacitive loading to ground introduces a lag in the feedback signal's return to the input. If enough lag is present (because of a large capacitive load) the amplifier may oscillate. Even if a capacitively loaded amplifier doesn't oscillate, it's always a good idea to check its response with step testing. It's amazing how close you can get to the edge of the cliff without falling off, except when you build 10,000 production units. Avoid capacitive loading. If such loading is necessary, check performance margins, and isolate or buffer the load.

The **Fig 5** waveform appears to be one cycle of oscillation. The output initially responds, but abruptly reverses direction, overshoots, and then heads positive again. Some overshoot again occurs, with a long tail and a small dip well before a nonlinear slew returns the waveform to zero. Ugly overshoot and tailing complete the cycle. This is certainly strange behavior, making you wonder what is going on. The input pulse is responsible for all these anomalies. The pulse's amplitude takes the amplifier outside its common-mode limits, inducing the bizarre effects shown. Keep inputs within the specified common-mode limits at all times.

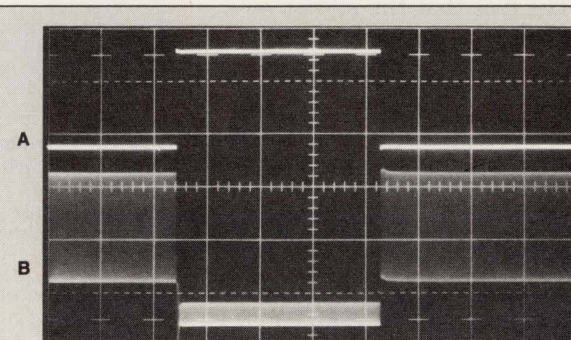
Fig 6 shows an oscillation-laden output (trace B) trying to unity-gain invert the input (trace A). The input's form is distinguishable in the output, but corrupted with very high-frequency oscillation and overshoot. In this case, the amplifier includes a booster within its loop to provide increased output current. The disturbances noted are traceable to local instabilities within the booster circuit. When using output booster stages, make sure they are inherently stable before placing them inside an amplifier's feedback loop. Wideband booster stages are particularly prone to device-level parasitic, high-frequency oscillation.

The booster-augmented, unity-gain inverting op amp in **Fig 7** also oscillates, but at a much lower frequency. Overshoot and nonlinear recovery dominate the waveform's envelope. Unlike the previous example, this behavior is not caused by local oscillations within the booster stage. Instead, the booster is simply too slow for the op-amp's feedback loop. The booster introduces enough lag to force oscillation, even as it hopelessly tries to maintain loop closure. Make sure that booster



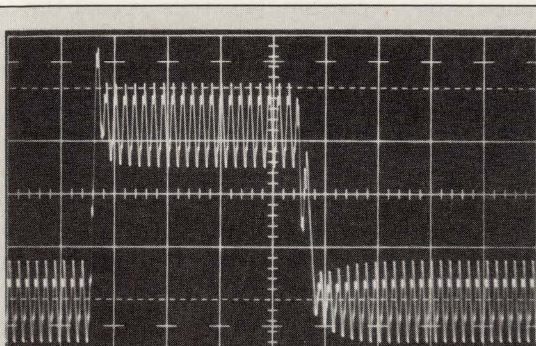
VERT = 1V/DIV
HORIZ = 50 nSEC/DIV

Fig 5—What appears to be one cycle of oscillation *is actually the result of a high-amplitude pulse that exceeds the common-mode range of the amplifier.*



VERT A = 5V/DIV
B = 5V/DIV
HORIZ = 1 μSEC/DIV

Fig 6—Local oscillation in a booster stage *produced this result. Wideband booster stages are prone to high-frequency parasitic oscillation.*



VERT = 0.5V/DIV
HORIZ = 500 μSEC/DIV

Fig 4—The oscillation shown here *is the result of excessive capacitive loading, which causes a lag in the feedback to the input of the amplifier.*

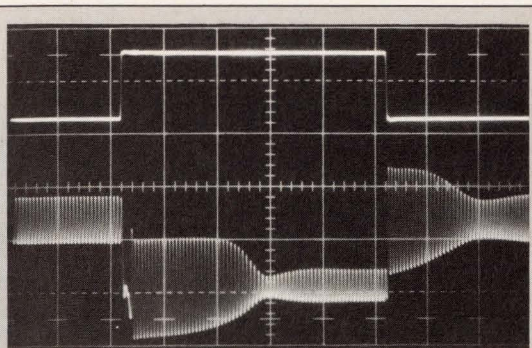


***Fig 7—Loop oscillation in a booster stage** produced this result. Note the lower frequency of oscillation compared with the local oscillation shown in **Fig 6**.*

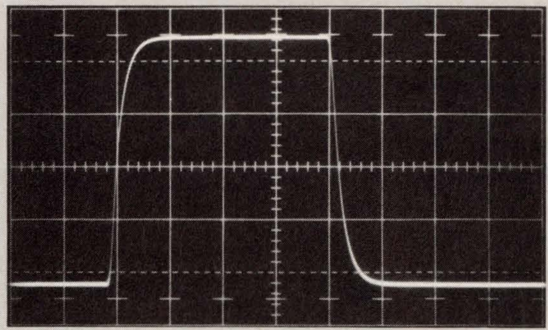


***Fig 8—Excessive source impedance** produced this serene—but undesired—result.*

stages are fast enough to maintain stability when placed in the amplifier's feedback loop.

The serene rise and fall of the **Fig 8** trace's pulse is a welcome relief from the oscillatory screaming of the previous examples. Unfortunately, such tranquilized behavior is simply too slow. This waveform is the result of excessive source impedance. The high impedance combines with the amplifier's input capacitance to band-limit the input, and the output reflects this action. Reduce the source impedance to a level that maintains the desired bandwidth, and minimize stray input capacitance. EDN

Acronyms used in this article

ac—Alternating current
DAC—Digital-to-analog converter
FET—Field-effect transistor
UHF—Ultrahigh frequency

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Author's biography

For more information on this article's author, turn to page 163 in the October 10, 1991, issue.

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

Measuring amplifier settling time

High-resolution measurement of an amplifier's settling time is often necessary. Frequently, a DAC drives the amplifier. Of particular importance is the time required for the DAC-amplifier combination to settle to its final value after an input step. This specification lets you set a circuit's timing margins with confidence that the data produced is accurate. The settling time is the total length of time from the input-step application until the amplifier's output remains within a specified error-band around the final value.

Fig A shows one way to measure DAC-amplifier settling time. The circuit uses the false-sum-node technique. The resistors and amplifier form a summing network. The amplifier output will step positive when the DAC moves. During amplifier slewing, the diodes limit the voltage excursion at the oscilloscope probe. The summing node is arranged so that, when settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half the actual settled voltage.

In theory, the **Fig A** circuit lets

Text continued on pg 142

you observe settling to small amplitudes. In practice, you can't rely on this circuit to produce useful measurements. Several flaws exist, including the oscilloscope connection. As probe capacitance rises, ac loading of the resistor junction will influence observed settling waveforms. The 20-pF probe alleviates this problem, but its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An active 1× FET probe might work, but another issue remains.

The clamp diodes at the probe point are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive-recovery characteristics vary among different types and are not usually specified. The 600-mV drop across the diodes means the oscilloscope may see an unacceptable overload, bringing displayed results into question. With the oscilloscope set at 1-mV per division, the diode voltage allows a 600:1 overdrive. Schottky diodes can cut this in half, but this is still much more than any real-time vertical amplifier can accommodate (**Ref 3**). The oscilloscope's

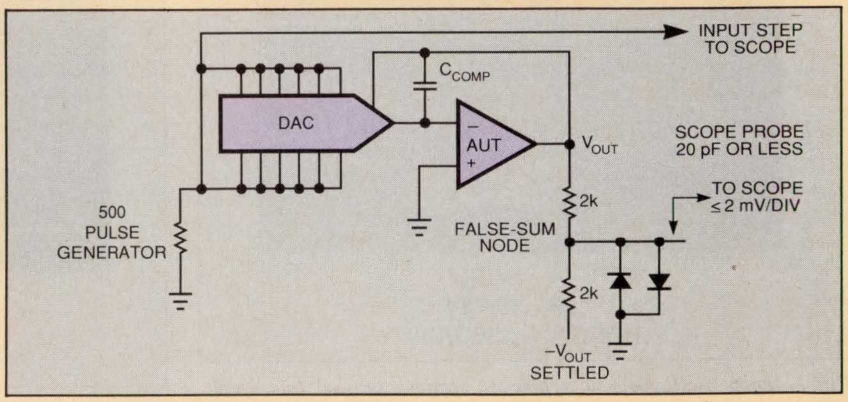


***Fig A—Using the false-sum-node technique**, this circuit has limitations in its ability to measure DAC-amplifier settling time.*

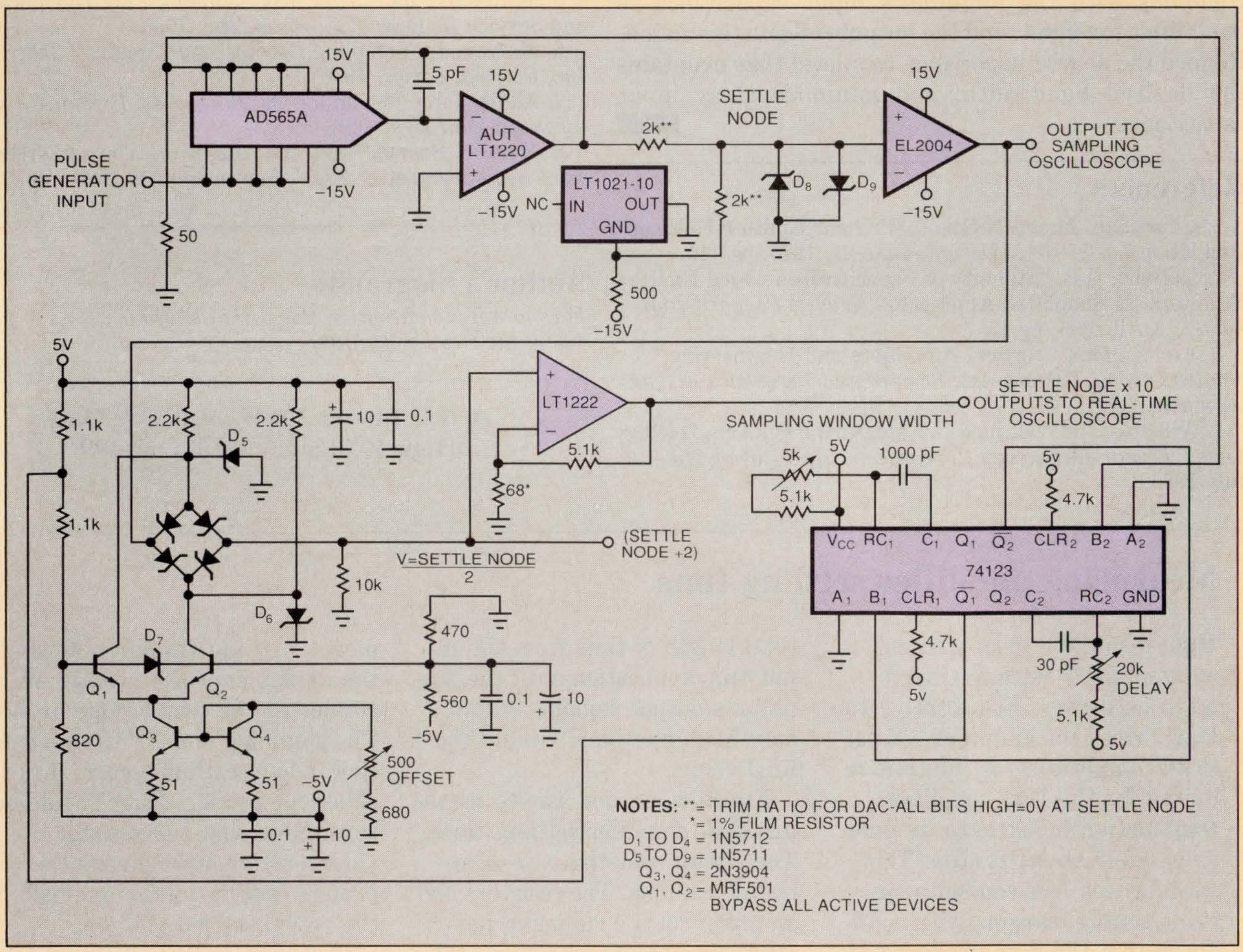


***Fig B—This settling-time test circuit** uses a sampling bridge to eliminate the oscilloscope overdrive problem of the previous circuit.*

overload recovery will completely dominate the observed waveform, and all measurements will be meaningless.

One way to achieve reliable settling-time measurements is to clip the incoming waveform in *time*, as well as amplitude. If you prevent the oscilloscope from seeing the waveform until settling is nearly complete, you can avoid overload problems. Doing this requires placing a switch at the settle circuit's output and controlling it with an input-triggered, variable delay. FET switches are not suitable because of their gate-source capacitance. This capacitance lets gate-drive artifacts corrupt the oscilloscope display, producing confusing readings. In the worst case, gate-drive transients will be large enough to induce overload, defeating the switch's purpose.

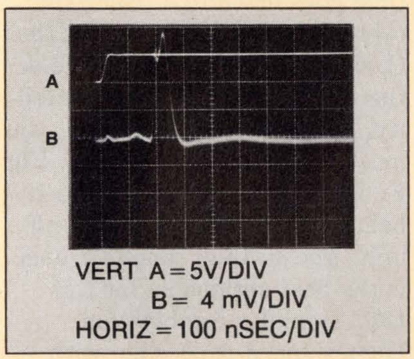


Fig C—The 280-nsec settling time shown here *was measured using the* ***Fig B*** *circuit. The sampling switch closes just before the third vertical division, which lets you observe the settling detail without overdriving the oscilloscope.*

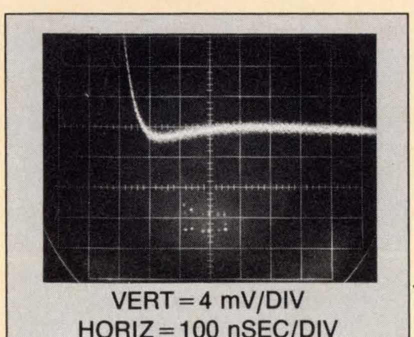


Fig D—This 280-nsec settling-time measurement *was obtained using a sampling scope at* ***Fig B*****'s** *sampling-scope output. The settling time and waveform is identical to that of* ***Fig C****.*

Fig B shows a way to implement a switch that largely eliminates these problems. This circuit lets you observe settling within 1 mV. The Schottky sampling bridge is the actual switch. The bridge's inherent balance, combined with matched diodes and very high-speed complementary bridge switching, yields a clean, switched output. An output-buffer stage unloads the settle node and drives the diode bridge.

The operation of the DAC-amplifier is as before. The additional circuitry provides the delayed switching function, eliminating oscilloscope overdrive. Buffering the settle node and driving the Schottky bridge is the EL2004, a unity-gain broadband FET-input buffer that has a 3-pF input capacitance and a 350-MHz bandwidth. The pulse generator's output fires the 74123 1-shot circuit. The arrangement of the 74123 produces a delayed pulse whose width sets the on-time of the diode bridge. The 20-kΩ potentiometer controls the pulse delay; the 5-kΩ potentiometer controls the pulse width. If you set the delay appropriately, the scope will not see any input until settling is nearly complete, eliminating overdrive. You adjust the width of the sample window so that all remaining settling activity is observable. In this way, the oscilloscope's output is reliable, and you can take meaningful data. Q_1 through Q_4 shift the level of the 1-shot's output, providing complementary switching drive to the bridge. The actual switching transistors, Q_1 and Q_2, are UHF types, permitting true differential bridge-switching with less than 1 nsec of time skew (**Ref 4**).

Using an oscilloscope having adequate sensitivity, you can observe the output of the bridge directly or you can look at the output of the LT1222, which provides a 10× amplified version. A third output, taken directly from the EL2004, is also available. This output, which bypasses the entire switching circuitry, provides a monitoring point for a sampling oscilloscope. Because of their operating nature, sampling oscilloscopes are inherently immune to overload (**Refs 5**, **6**, and 7). A good test of this settling-time test fixture (and the above statement) is to compare the signals displayed by the sampling scope and the Schottky-bridge-aided real-time scope.

As an additional test, you can employ a completely different (albeit considerably more complex) method of measuring settling time, described by Barry Harvey (**Ref 8**). All three approaches represent good measurement techniques, and if you use proper construction, the results should be identical. That is, the data produced by the three methods has a high probability of being valid.

Figs C, **D**, and **E** illustrate settling time details of an AD565A DAC and an LT1220 op amp. The photos represent the sampling bridge, sampling scope, and "Harvey" methods, respectively. Photos **Figs C** and **E** display the input step for convenience in ascertaining the elapsed time. Photo **Fig D**, taken with a single-trace sampling oscilloscope (Tektronix 1S1 with a P6032 cathode-follower probe in a 556 mainframe), uses the left-most vertical graticule line as its zero-time reference. All methods agree on a 280-nsec settling time to 0.01% (1 mV on a 10V step). Note that Harvey's method inherently adds 30 nsec, which you must subtract from the displayed 310-nsec to get the real number. Note also that the shape of the settling waveform—in every detail—is

Text continued on pg 144

Measuring amplifier settling time *(continued)*

identical in all three photographs. This kind of agreement provides a high degree of credibility for the measured results.

Some poorly designed amplifiers exhibit a substantial "thermal tail" after responding to an input step. This phenomenon, caused by die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking the settling at high speed, it is always a good idea to slow down the oscilloscope sweep and look for thermal tails. Often, you can accentuate the thermal tail's effect by loading the amplifier's output. Such a tail can make an amplifier appear to have settled in a much shorter time than it actually has.

Select the feedback capacitor

To get the best possible settling time from any amplifier, you should choose the feedback capacitor, C_F, carefully. The purpose of C_F is to roll off the amplifier gain at the frequency that permits the best dynamic response. The optimum value for C_F will depend on the feedback resistor's value and the characteristics of the source. DACs are one of the most common sources and also one of the most difficult. Usually, you must convert a

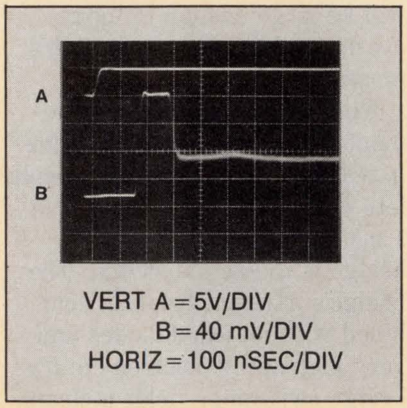


Fig E—Harvey's method was used to obtain *this 280-nsec settling-time measurement. After subtracting this method's inherent 30-nsec delay, the settling time and waveform are identical to that of* ***Figs C*** *and* ***D****.*

DAC's current output to a voltage. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200 nsec or less, but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the circuit unloads the DAC's current output directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase-shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling.

Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, which varies with code. Bipolar DACs typically have 20- to 30-pF of capacitance, which is stable over all codes. Because of their output capacitance, DACs furnish an instructive example in amplifier compensation.

Fig Fa shows the response of an industry-standard DAC-80 type and a relatively slow op amp. Trace A is the input, and traces B and C are the amplifier and settle outputs, respectively. In this example, there is no feedback capacitor (C_F), and the amplifier rings badly before settling. In **Fig Fb**, an 82-pF unit stops the ringing and settling time goes down to 4 μsec. The overdamped response means that C_F dominates the capacitance at the AUT's input, assuring stability. For the fastest response, you must reduce the value of C_F. **Fig Fc** shows the critically damped behavior obtained with a 22-pF unit. The settling time of 2 μsec is the best obtainable for this DAC-amplifier combination. Higher speed is possible with faster amplifiers and DACs, but the compensation issues remain the same.

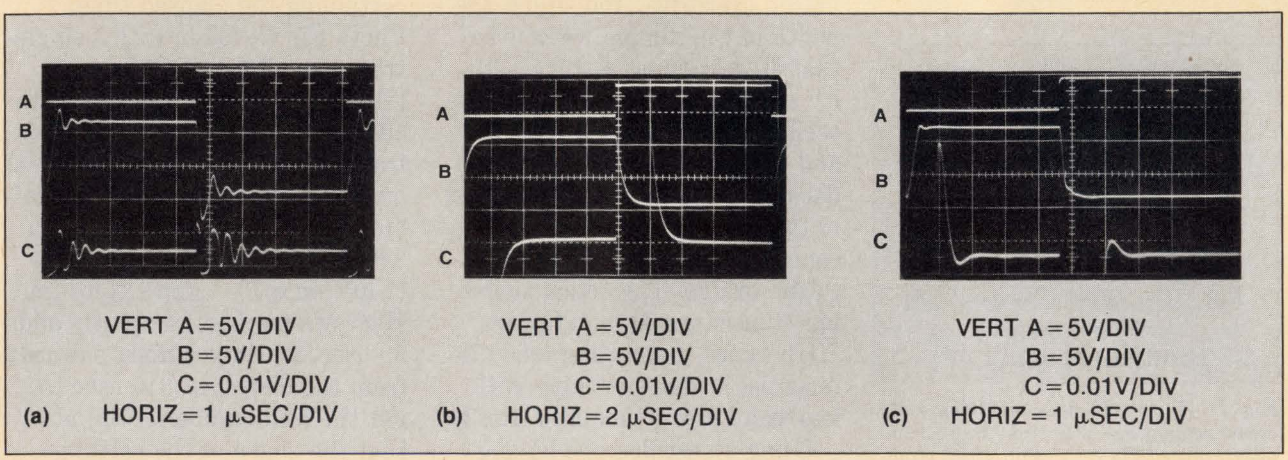
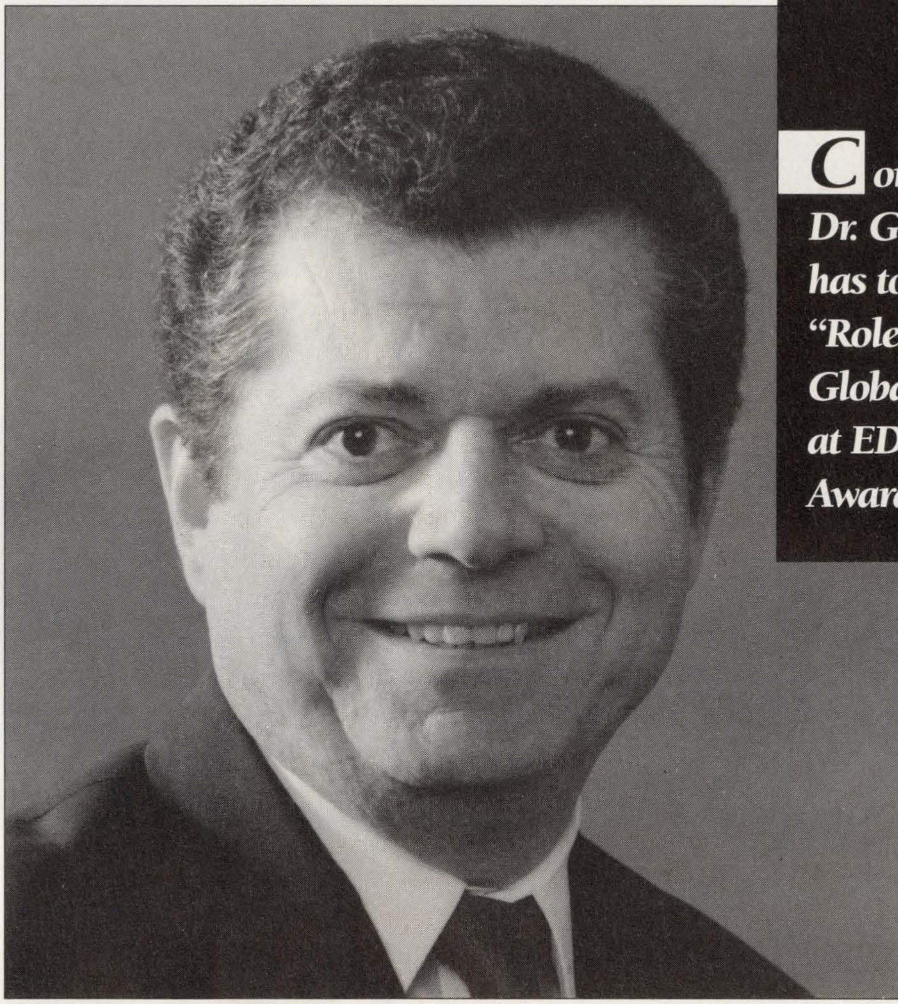


Fig F—These three scope traces show the effects of different values of feedback capacitors *on DAC-amplifier combinations. The values for the three photos are no capacitance (****a****), 82 pF (****b****), and 22 pF (****c****).*



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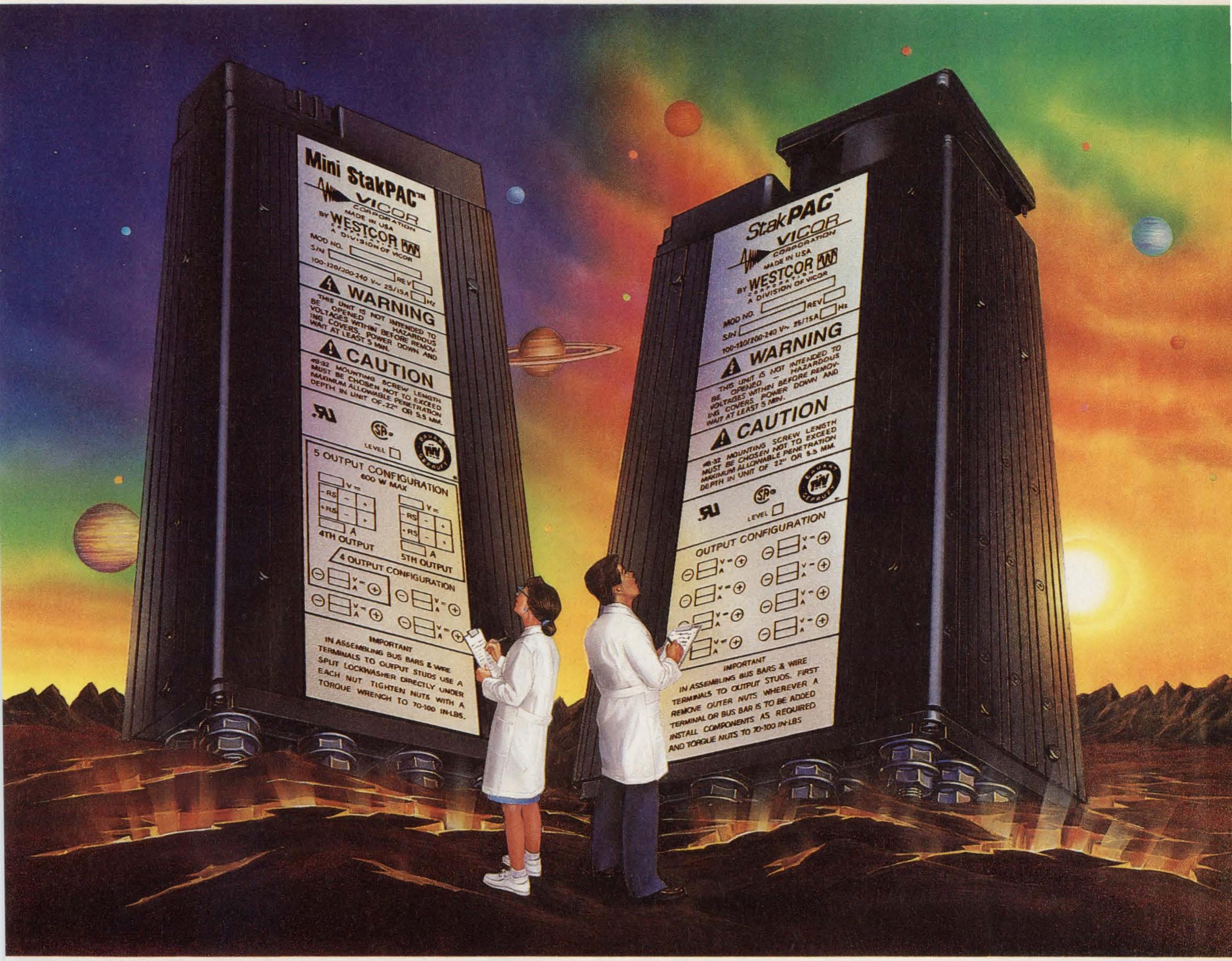

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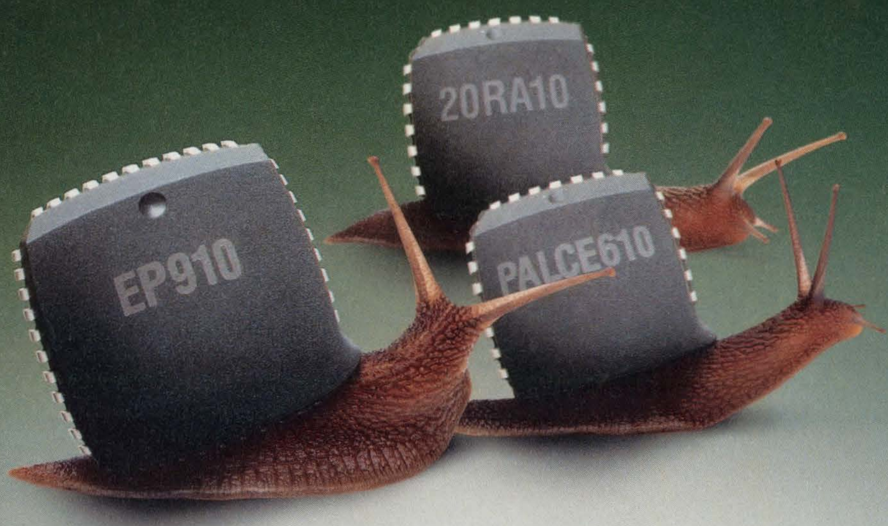

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THE JIM WILLIAMS PAPERS

High-speed amplifiers with low offset and drift

Amplifiers designed for wide bandwidth or fast settling often exhibit inferior characteristics at dc—that is, high voltage, current offset, and drift. Used with care, the techniques described here let you build circuits that exhibit exemplary performance from dc to MHz.

Jim Williams, *Linear Technology Corp*

Often, you must produce an amplifier circuit that has both the low offset of a dc amplifier and the wide bandwidth of a fast device. A number of techniques let you achieve such a result. Which method is best depends heavily on your application. Several circuits follow that you can study, build, and compare to determine what's best for you.

Fig 1 shows a composite amplifier that consists of an LT1097 low-drift device (IC_1) and an LT1191 high-speed amplifier (IC_2). The overall circuit is a unity-gain inverter that has its summing node at the junction of the two 1-kΩ resistors. IC_1 monitors this summing node, compares it to ground, and drives IC_2's positive input to complete a dc-stabilizing loop around IC_2. The 100-kΩ·0.01-μF time constant at IC_1 limits the amplifier's response to low-frequency signals. IC_2 handles high-frequency inputs, whereas IC_1 stabilizes the dc operating point. The 4.7-kΩ/220Ω divider at IC_2's input prevents excessive overdrive during startup. This circuit combines IC_1's 35-μV offset and 1.5-μV/°C drift with IC_2's 450V/μsec slew rate and 90-MHz bandwidth. Bias current, dominated by IC_2, is about 500 nA.

Fig 2 is similar, except that the sensing is differential, preserving access to both of the fast amplifier's inputs. IC_1 measures the dc error at IC_2's input terminals and biases IC_2's offset pin to force the offset to within 50 μV. IC_2's offset-pin biasing arrangement always lets IC_1 find the servo point. The 0.01-μF capacitor rolls off IC_1's gain at low frequencies, and IC_2 han-

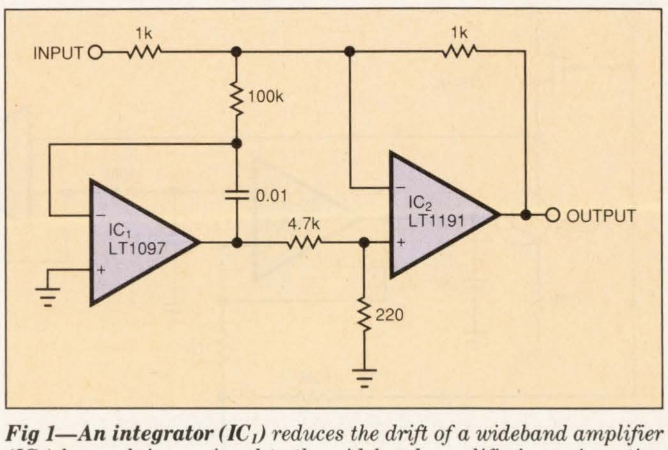


***Fig 1—An integrator (IC_1)** reduces the drift of a wideband amplifier (IC_2) by applying a signal to the wideband amplifier's noninverting input. That signal holds the wideband amplifier's summing junction at ground.*

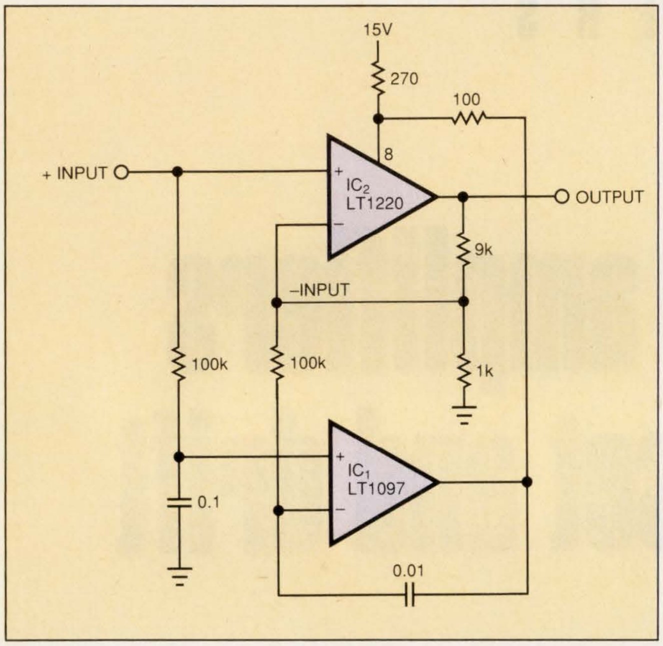


***Fig 2—You can also stabilize the offset** of a wideband amplifier (IC_2, in this case) by using a precision dc amplifier (IC_1) to apply correcting signals to the wideband amplifier's offset-trim adjustment pin.*

dles high-frequency signals. The combined characteristics of these amplifiers yield an offset voltage of 50 μV, an offset drift of 1 μV/°C, a slew rate of 250 V/μsec, and a gain bandwidth of 45 MHz.

Fig 3 shows wideband, highly stable gain-of-10 amplifier with high input impedance. The input capacitance is about 3 pF. Because of its low input capacitance and low (100 pA) bias current, the circuit is well suited for use in probing IC wafers or as a pin amplifier in automatic-test systems.

Q_1 and Q_2 constitute a simple, high-speed FET-input buffer. Q_1 functions as a source follower, and the Q_2 current-source load sets the drain-to-source channel current. IC_2 provides a gain of 10 with 100-MHz bandwidth. Normally, this open-loop configuration would drift unacceptably because there is no dc feedback. IC_1, by comparing the filtered circuit output to a similarly filtered version of the input signal, provides the feedback to stabilize the circuit. The amplified difference between these signals sets Q_2's bias—and hence Q_1's channel current—thereby forcing Q_1's V_{GS} to match the circuit's input and output potentials. The capacitor around IC_1 provides stable loop compensation. The R-C network in IC_1's output prevents that output from seeing high-speed edges coupled through Q_2's collector-base junction.

Fig 4a shows a way to combine wide bandwidth with true differential inputs and dc stabilization. IC_1 and IC_2 sense the input differentially at gains of 10. Wideband amplifier IC_1 feeds high-frequency signals to output amplifier IC_3 via a highpass network. Low-frequency and dc information get to IC_3 via the slower IC_2. The 2-kΩ/200-pF lowpass networks remove the input signal's high-frequency components, so only lower frequencies reach IC_2. Because the gain and bandwidth of the high- and low-frequency paths complement each other, IC_3's output is an undistorted, amplified version of the input (see **Fig 4b**, trace D.)

Fig 4b, trace A is one side of a differential input signal applied to the circuit. Trace B is IC_1's output

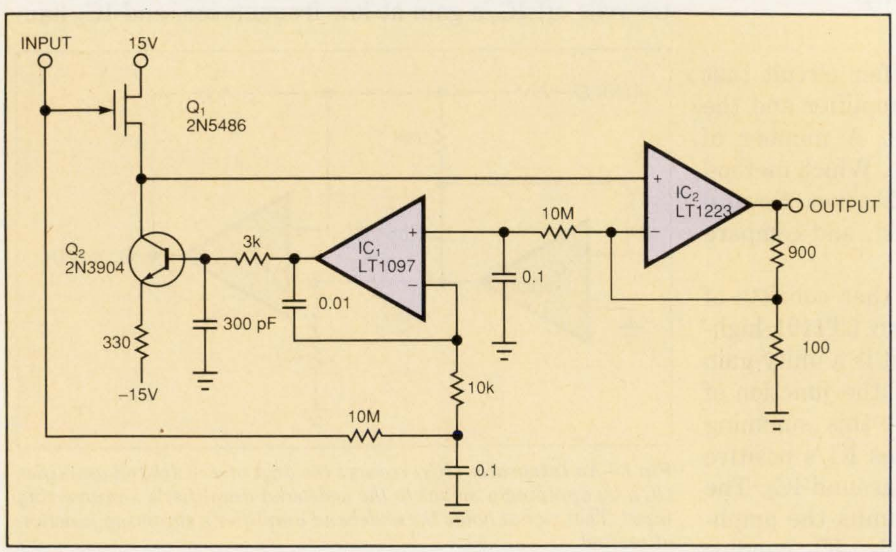


***Fig 3—An integrator (IC_1)** drives a current source (Q_2), which biases a FET (Q_1) that completes a dc feedback loop around IC_2 to stabilize the amplifier's operation at dc.*

taken at the junction of the 500Ω potentiometer and 0.001-μF capacitor. Trace C is IC_2's output. With the "ac-gain" and "dc-gain-match" trims properly adjusted, the two paths' contributions match up and trace D is clean, with no residual artifacts. You can optimize the adjustments by trimming the ac gain for the squarest corners and the dc-gain match for a flat top. Bandwidth for this circuit exceeds 35 MHz; slew rate is 450V/μsec; and dc offset is about 200 μV.

Parallel paths yield the best of two worlds

Fig 5a shows a very powerful extension of the previous circuit. The circuits operate similarly, but this one has a gain of 1000; its bandwidth is about 35 MHz; its rise time is 7 nsec; and its delay is less than 7.5 nsec. Full-power response is available to 10 MHz, and broadband input noise is about 15 μV. This kind of speed, coupled with true differential inputs, a gain of 1000, high dc stability, and low cost make the circuit broadly applicable in wideband instrumentation.

As before, two differential amplifiers, IC_1 and IC_2, simultaneously sense the inputs. In this case, IC_1 is a 592-733 type operating at a gain of 100. Its differential outputs feed output amplifier IC_3 via 1-μF/1-kΩ high-pass networks that strip out the dc content of IC_1's output. IC_2, a precision dc differential amplifier, operates in similar fashion to its counterpart in the previous circuit, supplying dc and low-frequency information to IC_3 at a trimmed gain of 100.

In this case, the output amplifier, IC_3, is not a follower but a differential-input/single-ended-output gain block whose nominal gain is 10. This change is necessary because IC_1's differential output must become a single-ended signal to provide the circuit's final output. Consequently, IC_2 does not directly apply its low-frequency information to IC_3 as it did before. Instead, IC_4 measures the difference between IC_2's output and a fraction of IC_3's output. IC_4's output, biasing IC_3's positive input via the 1-kΩ resistor, closes a loop around the circuit's dc and low-frequency path. To make the circuit's dc gain equal to its ac gain, you adjust the divider that feeds IC_4's negative input.

Fig 5b shows the circuit's response to a 60-nsec, 2.5-mV pulse, trace A. The ×1000 output, trace B, responds cleanly, with both delay and rise time in the 5- to 7-nsec range. Some small amount of overshoot is evident, but you can trim the overshoot with the peaking adjustment at IC_1. **Fig 5c** plots the circuit's gain vs frequency. The gain is flat within 0.5 dB to 20 MHz, with the −3 dB point at 40 MHz. The overshoot of **Fig 5b** shows up here as a very slight gain increase starting around 1 MHz and continuing to about 15 MHz. The peaking adjustment eliminates this effect.

To use this circuit, apply a low-frequency or dc signal of known amplitude and adjust the low-frequency gain to ×1000 after the output has settled. Next, adjust the high-frequency gain so that the signal's leading and trailing corners have amplitudes identical to those

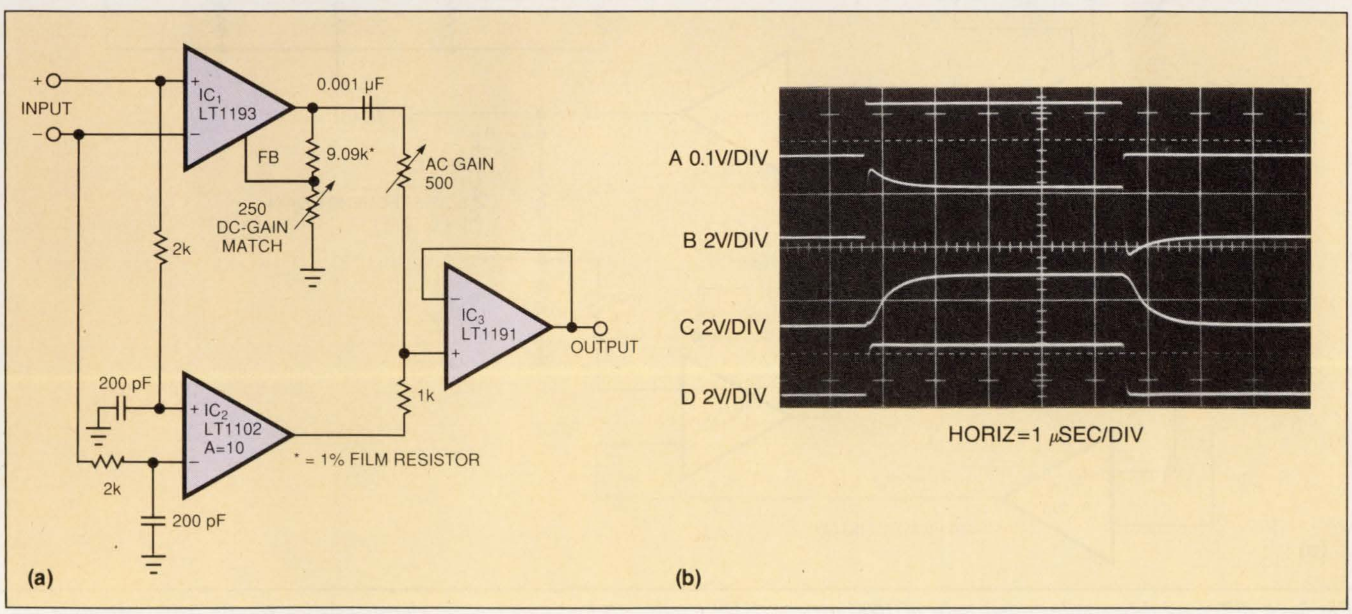


***Fig 4—Parallel paths** for ac and dc signals **(a)** provide low offset and good dynamic response—if you correctly adjust the trims (**b**, trace D).*

of the settled portion. Finally, trim the peaking adjustment for the best settling of the output pulse's corners.

Fig 5d shows the input (trace A) and output (trace B) waveforms with all adjustments properly set. The fidelity is excellent, with no aberrations or other artifacts of the parallel-path operation evident. **Fig 5e** shows the effects of too much ac gain; excessive peaking on the edges, with proper amplitude achieved only after the dc channel takes control of the output. Similarly, excessive dc gain produces **Fig 5f**'s traces. The ac-gain path provides proper initial response, but too much dc gain forces a long, tailing response that finally settles at an incorrect amplitude.

The use of parallel-path schemes to simultaneously achieve wide bandwidth and outstanding dc performance isn't new. In fact, it predates the use of low-drift bipolar differential gain stages. The first parallel-path amplifiers achieved dc stability by using electromechanical choppers to convert dc to ac. Gain stages consisting first of vacuum tubes and later of Germanium transistors amplified the chopped dc. Synchronous rectifiers converted the ac back to dc. AC-coupled amplifi-

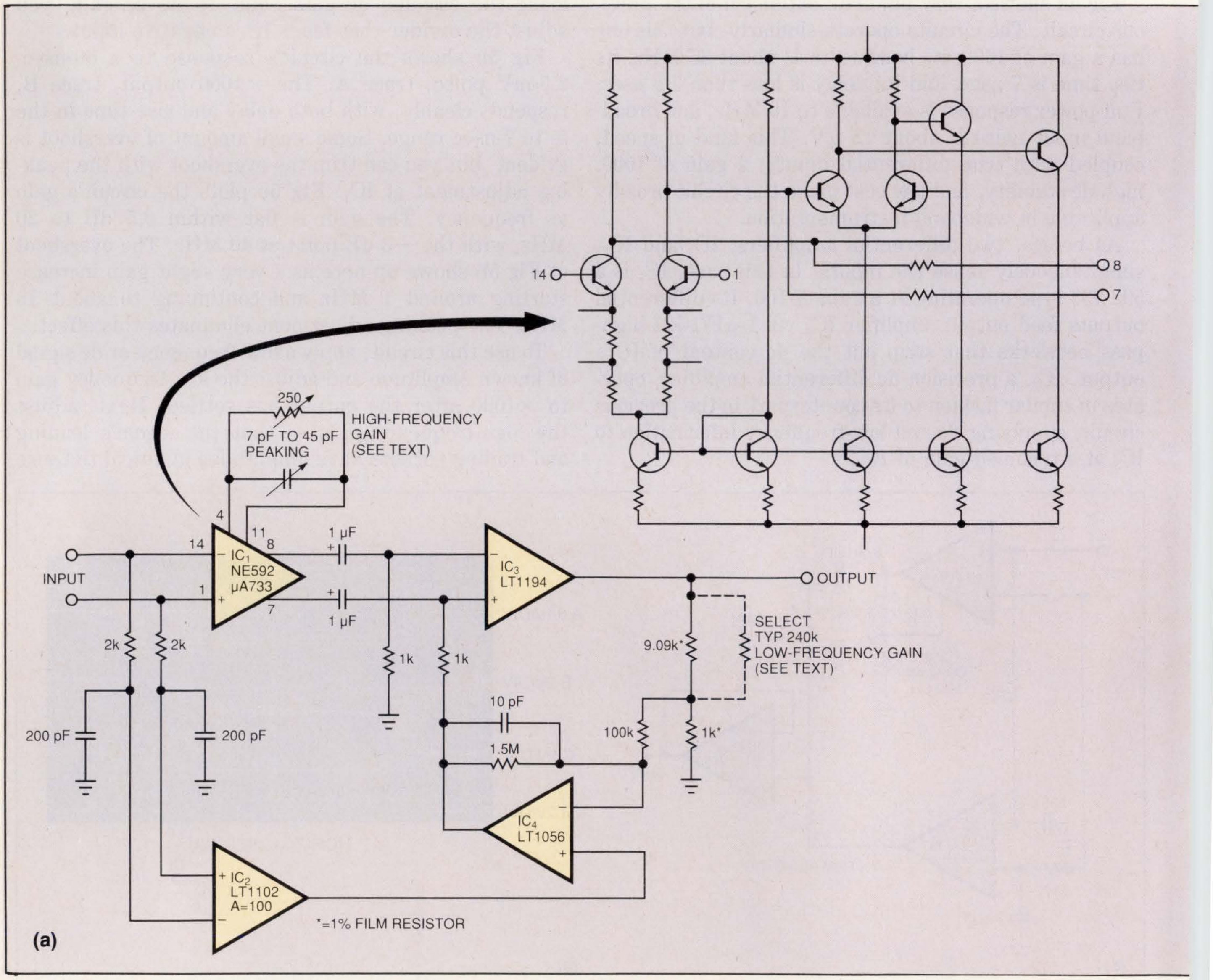


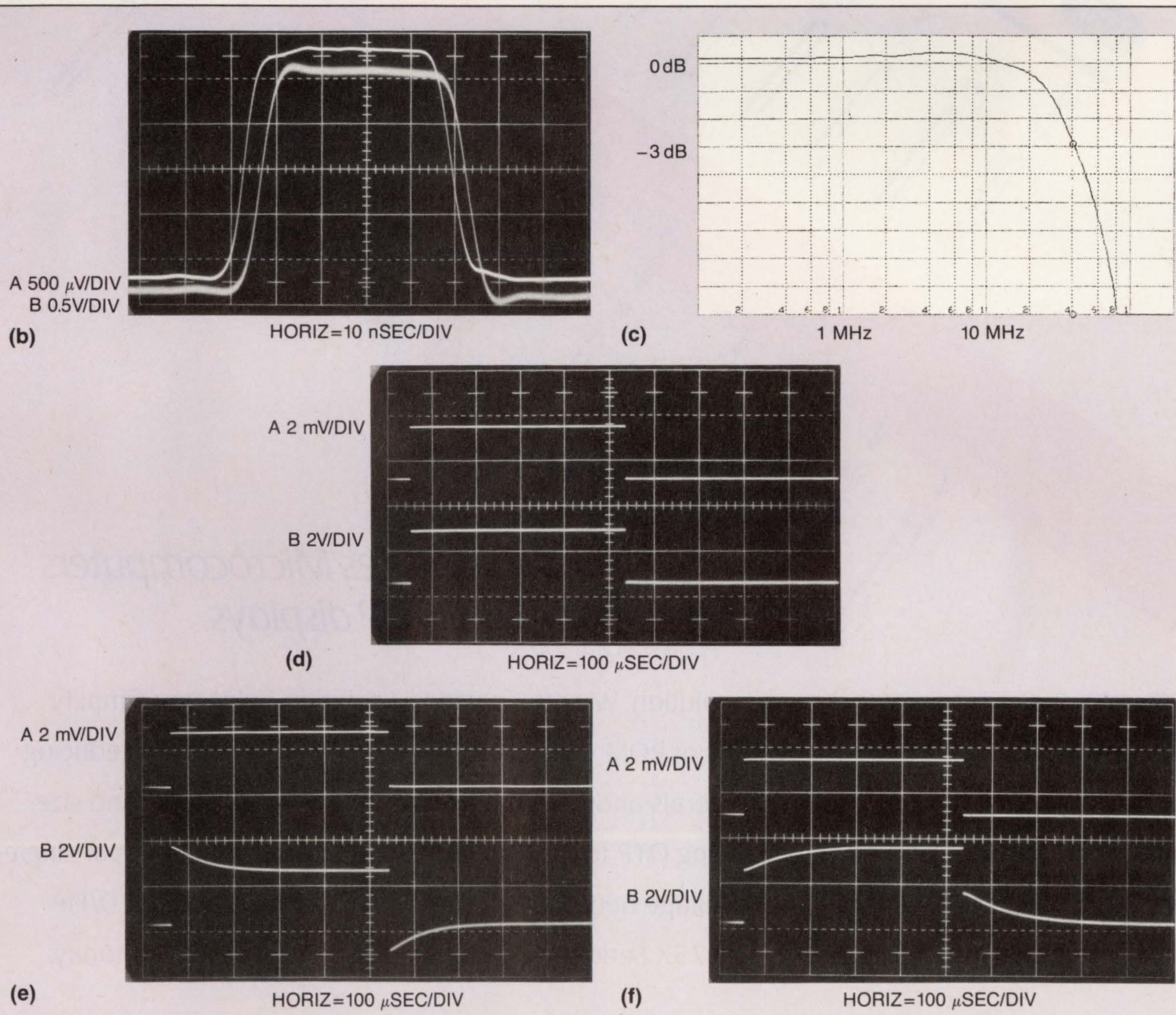
***Fig 5—A differential-to-single-ended gain of 1000** with 38-MHz bandwidth and excellent dc characteristics results from extending the parallel-path architecture, **(a)**. The pulse response (**b**, trace B) shows a minimum of overshoot, which is reflected in the frequency response*

ers in parallel with the chopper amplifiers provided good bandwidth. As **Figs 5e** and **5f** illustrate, these schemes have historically had a problem in many applications that demand the best at both dc and high frequencies: Unless you carefully match the dc and ac gains, the amplifiers' response to an input voltage step exhibits a long "tail." Keeping the response free of such tails over wide temperature ranges and long periods of time has always presented a challenge. Modern components make meeting that challenge easier, but the challenge still exists. **EDN**

Author's biography

For more information on this article's author, *turn to page 163 in the October 10, 1991, issue.*

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475



***(c)** as a slight peak near 6 MHz. In the other three photos, **(d, e, and f)**, you see, respectively, the effects of correctly matching the ac and dc gains, setting the ac gain too high, and setting the dc gain too high.*

THE JIM WILLIAMS PAPERS

High-speed amplifiers in application circuits

Once you acquire some familiarity with high-speed amplifiers and a respect for their design requirements, you can use these devices' speed to design a variety of application circuits. These circuits include DAC current-to-voltage converters, video amplifiers, and power boosters.

Jim Williams, *Linear Technology Corp*

Recent processing and design advances have made inexpensive, precision wideband amplifiers practical. They are less prone to oscillation and other variations than some much slower amplifiers. High-speed amplifiers' raw speed capabilities, combined with their inherent flexibility as op amps, permit a range of applications. These amplifiers let you create fast linear circuits that are difficult or impractical to create using other approaches. You can use these application circuits to capitalize on the amplifier's speed to improve on a standard circuit. Or you can utilize speed to implement a traditional function in a nontraditional way, with attendant advantages. You can even design completely new, start-of-the-art circuit functions that were previously impractical to implement at the board level. Simply put, these amplifiers make implementing high-speed functions easier.

One of the most common applications for a high-speed amplifier, transforming a 12-bit DAC's current output into a voltage, is also one of the most difficult. Although an op amp can easily perform the required current-to-voltage conversion, obtaining good dynamic performance requires careful design. A fast DAC can settle to 0.01% in 200 nsec or less, but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's output directly drives an amplifier's summing junction, placing the parasitic capacitance between ground and the amplifier's input. This capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to ring about the final value before settling.

Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance—in the 100- to 150-pF range, which varies with the input code. Bipolar DACs typically have 20 to 30 pF of capacitance, which is constant over all codes. As such, bipolar DACs are almost always better to use where high speed is required. **Fig 1a** shows the AD565A 12-bit DAC with an LT1220 output op amp. **Fig 1b** shows clean 0.01% settling in 280 nsec (trace B) to a full-scale input step (trace A). The requirements for obtaining trace B's display are not trivial **(Ref 1)**.

Another application area requiring good dynamic stability is video amplifiers driving cables. **Fig 2** shows a simple way to multiplex two video amplifiers onto a single 7Ω cable. The level of the input-select line determines which of the two amplifiers is active in accordance with the truth table in the figure. Amplifier performance includes 0.02% differential gain error and 0.1° differential phase error. The cable's 75Ω back termination means that the amplifiers must swing $2V_{p\text{-}p}$ to produce $1V_{p\text{-}p}$ at the cable output, but most amplifiers can easily handle this output swing.

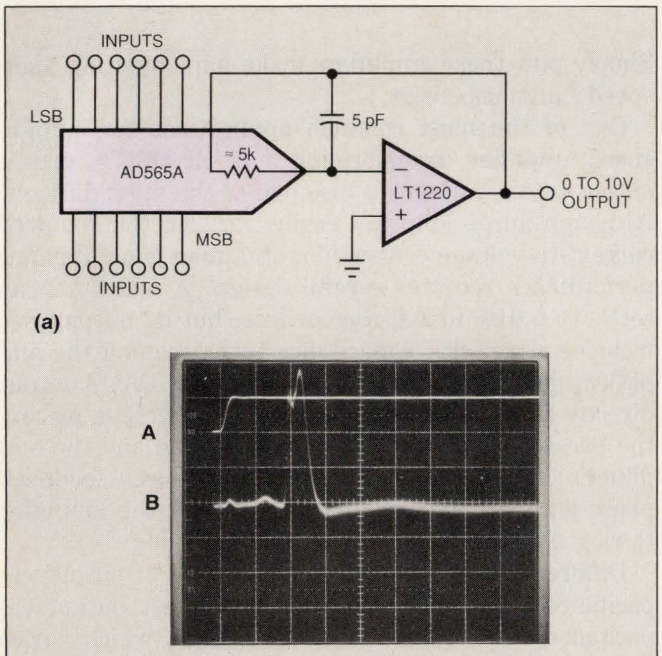
Simple video amp

Fig 3 is a simpler version of **Fig 2**. This circuit is a single-channel video amplifier, and it provides for a gain of 10. The circuit retains the double-cable termination of **Fig 2**, and the circuit has a 55-MHz bandwidth.

Fig 4 is another cable-related circuit. Here, the differential amplifier simply hangs across a distribution cable, extracting the signal. The amplifier's true differential inputs reject common-mode signals. As in the previous circuit, differential-gain and phase errors measure 0.02% and 0.1°, respectively. A separate input permits for adjustment of the dc level.

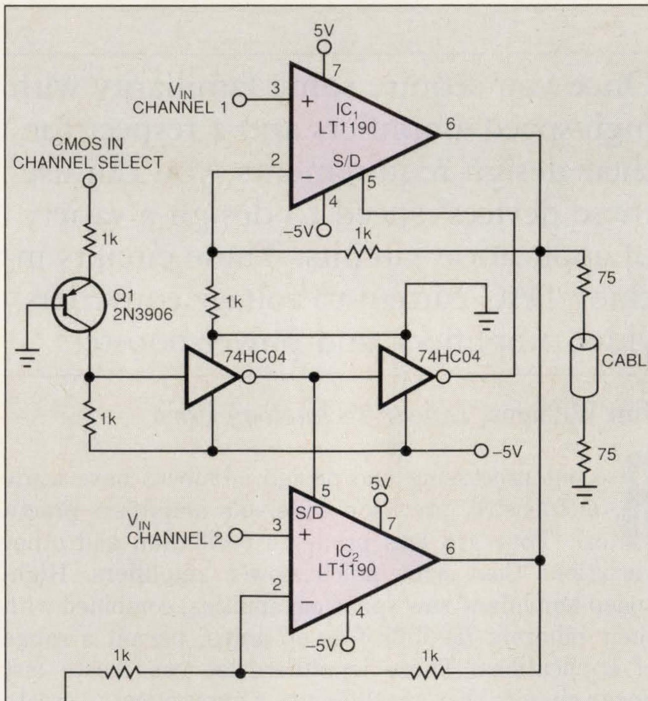
High-speed analog signals transmitted on a line often pick up substantial common-mode noise. **Fig 5a** shows a simple, fast, differential line receiver using the LT1194 gain-of-10 differential amplifier (IC_1). The differential line is fed to IC_1. The resistor-diode networks prevent overload and ensure sufficient input bias for IC_1 under all conditions. IC_1's output represents the difference of the 2-line input, times a gain of 10. In theory, the circuit should reject all common-mode noise.

The test-circuit **(Fig 5b)** waveforms **(Fig 5c)** confirm this noise rejection. The sine-wave oscillator drives T_1 **(Fig 5c**, trace A), producing a differential line output at its secondary. T_1's secondary returns to ground through a broadband noise generator, flooding the line inputs with common-mode noise (traces B and C are



TRACE	VERTICAL SCALE
A	5V/DIV
B	4 mV/DIV

***Fig 1—Achieving good dynamic performance while** converting a DAC's output current to voltage is a difficult job for many op amps. The output of the circuit in **a** responds to a full-scale step (**b**, trace A) by fully settling in 280 nsec (**b**, trace B).*



INPUT SELECT	IC_1 OUTPUT	IC_2 OUTPUT
5V	ACTIVE	INACTIVE
0V	INACTIVE	ACTIVE

***Fig 2—This 2-channel video amplifier features** 0.02% differential-gain error and 0.1° differential-phase error.*

IC_1's inputs). Trace D, IC_1's multiplied-by-10 version of the differential signal at its inputs, shows no visible noise or disturbances. This circuit provides a clean output, even in the presence of noise that dominates the signal by a 100:1 ratio from dc to 5 MHz.

Fig 6a shows another way to achieve high common-mode rejection. Additionally, this circuit has the advantage of true 3-port isolation. That is, the input, gain stage, and output are all galvanically isolated from each other. This configuration is useful where large common-mode differences exist or where ground integrity is uncertain. The circuit configures IC_1 for a simple gain of 11. T_1 feeds IC_1's positive input, and the output passes through T_2. **Fig 6b** shows the circuit's response to a 4-MHz input, with all transformer leads designated "•" referred to ground. The input (**Fig 6b**, trace A) drives T_1, whose output (trace B) feeds IC_1. IC_1 amplifies the signal, and its output (trace C) feeds T_2. T_2's output (trace D) is the circuit's output. Phase shift is evident, although tolerable. T_1 and T_2 are very wideband devices, with low phase shift. Note the negligible phase difference between the A-B and C-D trace pairs. IC_1 contributes the entire phase error. Using the transformers specified, the circuit's low frequency cut-off is about 10 kHz.

It is often desirable to examine or amplify one particular portion of a signal while rejecting all others.

Text continued on pg 162

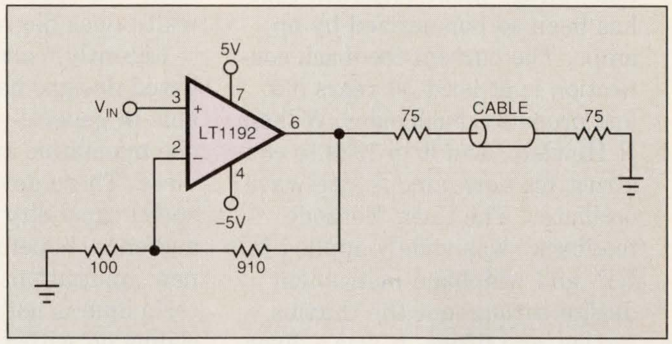


*Fig 3—**This double-terminated cable driver** features a bandwidth of 55 MHz.*

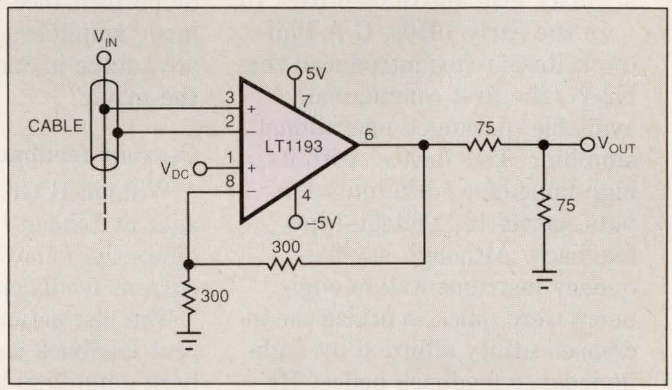


*Fig 4—**To extract video signals,** this cable-sense amplifier features a loop-through connection.*

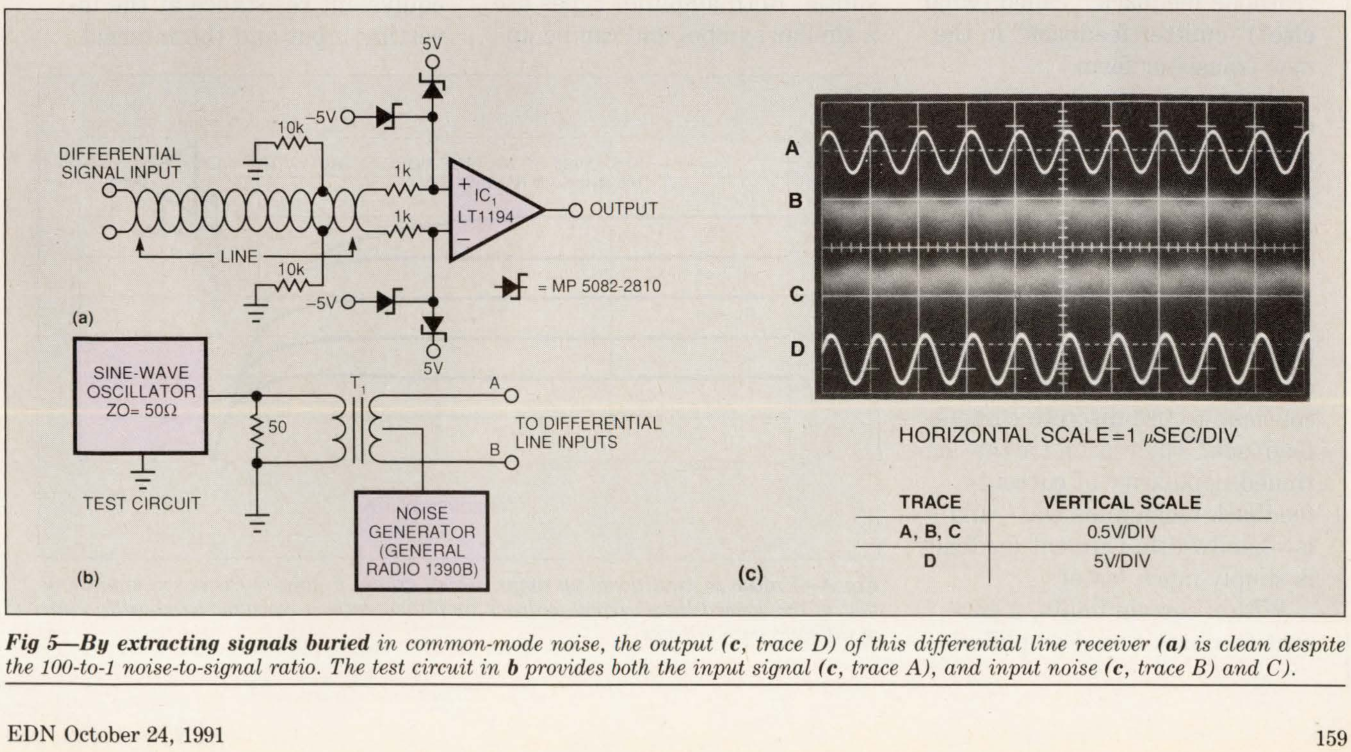


*Fig 5—**By extracting signals buried** in common-mode noise, the output (**c**, trace D) of this differential line receiver (**a**) is clean despite the 100-to-1 noise-to-signal ratio. The test circuit in **b** provides both the input signal (**c**, trace A), and input noise (**c**, trace B) and C).*

About "current-mode" feedback

Contrary to some enthusiastic marketing claims, so-called current-mode feedback isn't new. In fact, it is much older than the normal voltage-mode feedback that has been so popularized by op amps. The current-feedback connection is at least 50 years old, and probably much older. William R Hewlett used it in 1939 to construct his now-famous sine-wave oscillator. The term "cathode feedback" was widely applied in RF- and wideband-instrument design throughout the thirties, forties, and fifties. It was a favorite form of feedback, if for no other reason than there wasn't anyplace else left to feed back to.

In the early 1950s, G A Philbrick Researches introduced the K2-W, the first commercially available, packaged operational amplifier. This device, with its high-impedance differential inputs, permitted voltage-type feedback. Although low-frequency instrumentation engineers were quick to utilize the increased utility afforded by high-impedance feedback nodes, RF and wideband designers hardly noticed. They continued to use "cathode feedback," called (what else?) "emitter feedback" in the new transistor form.

Numerous examples of the continued use of "current-mode" feedback in RF and wideband instruments are found in designs dating from the 1950s to the present. Ostensibly easier-to-use voltage-type feedback was readily usable during this period, particularly as monolithic devices became cheap. Why did designers continue to use discrete current feedback? The reason for the continued popularity of current-feedback techniques was—and is—bandwidth. Current feedback is simply much faster.

Within certain limits, a current-feedback-based amplifier's bandwidth does not degrade as the closed-loop gain increases. This feature is a significant advantage over voltage-mode feedback amplifiers, whose bandwidth does degrade.

Recently, current-feedback-based designs have become available in general-purpose, easy-to-use monolithic and hybrid devices. These devices bring high-speed capability to a much wider audience, hopefully opening up new applications. So, while the technique is not new, marketing claims notwithstanding, the opportunity is. Although current-mode-based designs have poorer dc performance than voltage mode amplifiers, their bandwidth advantage is undeniable. What's the magic?

Current feedback basics

William H Gross, Design Manager at Linear Technology Corp, offers the following insight into current feedback.

The distinctions between current-feedback and voltage-feedback amplifiers are not obvious at first because, viewed from the outside, the differences can be subtle. Both amplifier types use a similar symbol and can be applied on a first-order basis using the same equations. However, their behavior in terms of the gain-bandwidth tradeoff and large-signal response is another story.

Unlike in voltage-feedback amplifiers, small-signal bandwidth in a current-feedback amplifier isn't a straight inverse function of closed-loop gain, and large-signal response is closer to ideal. Both benefits stem from the fact that the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor, R_F, from output to inverting input, works with internal junction capacitances to set the closed-loop bandwidth. Even though the gain-set resistor, R_G, from inverting input to ground, works with R_F to set the voltage gain, just as in a voltage feedback op amp, the closed-loop bandwidth does not change.

The explanation of these effects is fairly straightforward. The equivalent gain-bandwidth product of the current-feedback amplifier is set by the Thevenin equivalent resistance at the inverting input and the internal

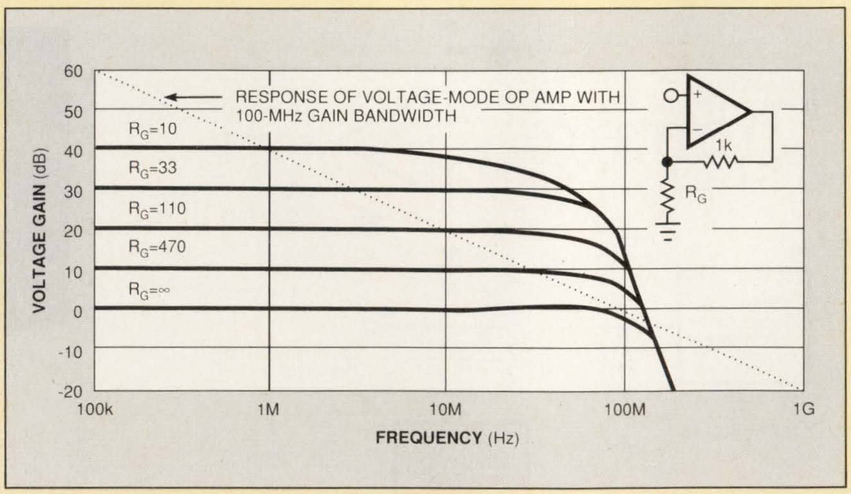


Fig A—Unlike in traditional op amps, *which exhibit a gain-vs-frequency similar to that of the dashed line, current-feedback amplifiers have a constant bandwidth, even at different gain settings.*

compensation capacitor. If R_F is held constant and gain changed with R_G, the Thevenin resistance changes by the same amount as the gain. From an overall loop standpoint, this change in feedback attenuation will produce a change in noise gain and a proportionate reduction of open-loop bandwidth, as in a conventional op amp.

With current feedback, however, the key point is that changes in Thevenin resistance also produce a compensatory change in open-loop bandwidth, unlike in a conventional fixed-gain bandwidth amplifier. As a result, the net closed-loop bandwidth of a current-feedback amplifier remains the same for various closed-loop gains.

Bandwidth is the key advantage

Fig A shows a plot of voltage gain vs frequency for a representative current-feedback amplifier, the LT1223, for five gain settings, driving 100Ω. For comparison, the figure also shows a plot of the fixed 100-MHz gain-bandwidth limitation that a voltage-feedback amplifier would have. It is obvious that for gains greater than one, the current-feedback amplifier provides 3 to 20× more bandwidth. The general shape of this bandwidth profile is common to all current-feedback amplifiers.

Because the feedback resistor determines the compensation of the amplifier, you can optimize bandwidth and transient response for almost every application. When operating from ±15V supplies, R_F should be 1 kΩ or more for stability. When operating from ±5V supplies, the minimum value is 680Ω because the junction capacitors increase with lower voltage. For either case, larger feedback resistors can also be used but will slow down the amplifier—which may be desirable in some applications.

The difference in operating characteristics between voltage- and current-feedback op amps results in slight differences in common circuit configurations. **Fig B** summarizes some popular circuit types, showing differences between each op-amp type. Gain can be set with either R_{IN} or R_F in a voltage-feedback op amp, but the R_F used with a current-feedback op amp is fixed.

You can control a voltage-mode op amp's bandwidth using a feedback capacitor. However, when using current-feedback op amps, bandwidth must be limited at the input. A feedback capacitor is never used. In an integrator, the 1-kΩ resistor must be included in the current-feedback amplifier's feedback path so its negative input sees the optimal impedance.

There is no correlation between bias currents of a current-feedback amplifier's inputs. Thus, source impedance matching will not improve dc accuracy. Matching input source impedances aids offset performance only in op amps that do not have internal bias-current cancellation.

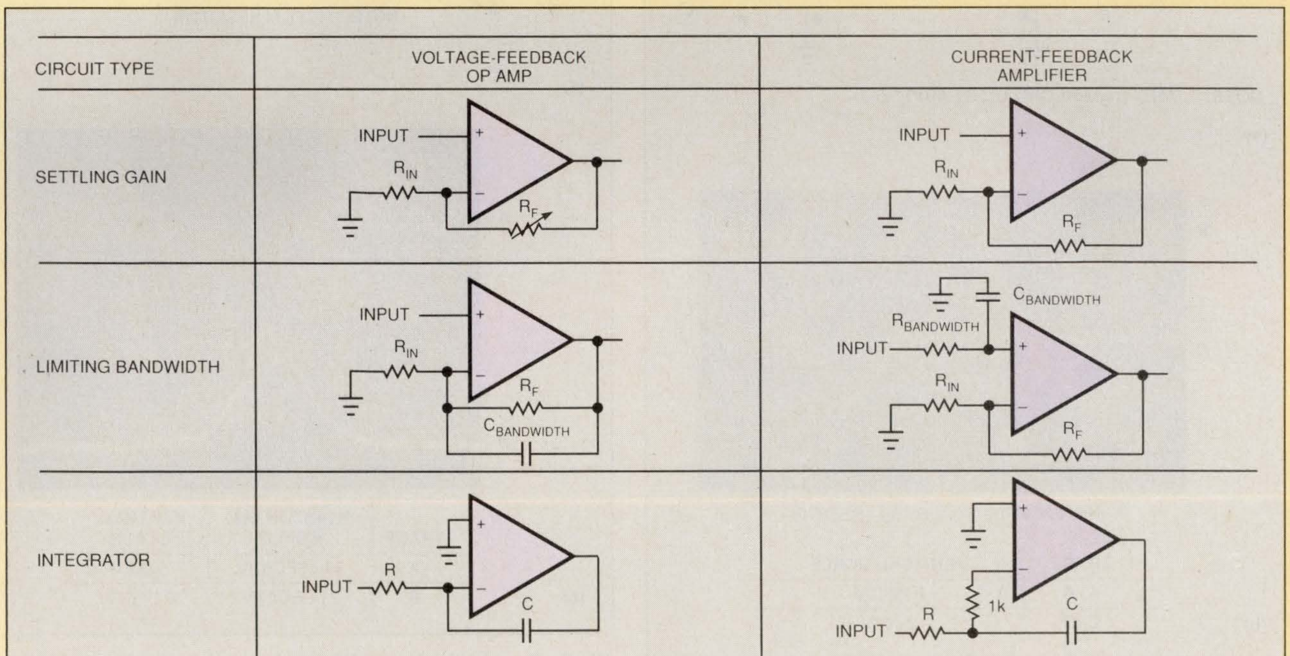
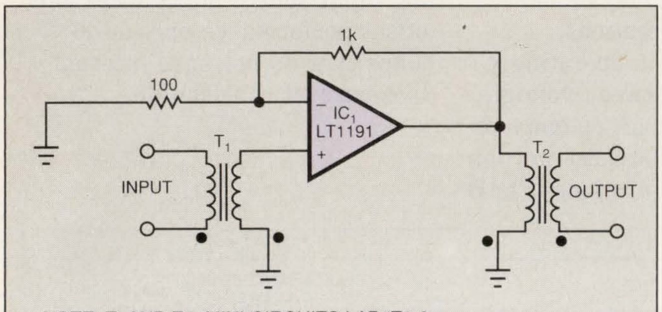


Fig B—Although voltage-mode and current-feedback op amps look alike *when viewed from the outside, their internal architectural differences require that you use slightly different circuit topologies when applying them.*

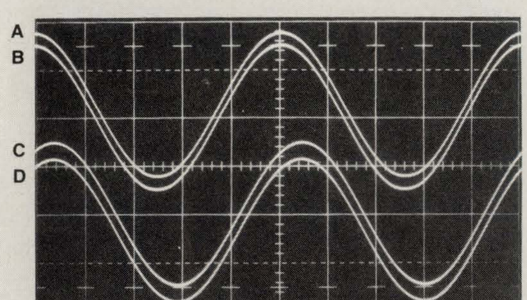
At high speed, this can be difficult because the amplifier may see fast, large common-mode voltage swings. Recovery from such activity usually is dominated by saturation effects, making the quality of the amplifier's output questionable. Differential amplifiers with fast overload recovery can perform this function while maintaining output fidelity to the input signal. The circuit in **Fig 7a** allows you to set the input level at which amplifying begins, allowing any amplitude-defined point to be selected. In **Fig 7a**, IC_1, the LT1019 reference, and associated components form an adjustable, bipolar voltage source that is coupled to differential amplifier IC_2's negative input. The input signal biases IC_2's positive input; R_1 and R_2 set IC_2's gain.

Input signals below IC_2's negative input levels keep IC_2's output in saturation, and no signal appears at the output. When the positive input rises above the negative input's bias point, IC_2 becomes active, providing an amplified version of the instantaneous difference between its inputs. **Fig 7b** shows what happens when you apply the output of a triangle wave generator (trace A) to the circuit. Setting the bias level just below the triangle peak permits high gain and detailed operation of the turnaround at the peak. Trace B clearly shows the switching residue in the generator's output. Appropriate variations in the voltage-source setting would permit more of the triangle slopes to be observed, with attendant loss of resolution due to oscilloscope overload limitations. Similarly, increasing IC_2's gain allows more amplitude detail while placing restrictions on how much of the waveform you can display.



NOTE: T_1 AND T_2 =MINI-CIRCUITS LAB#T1-6.

(a)

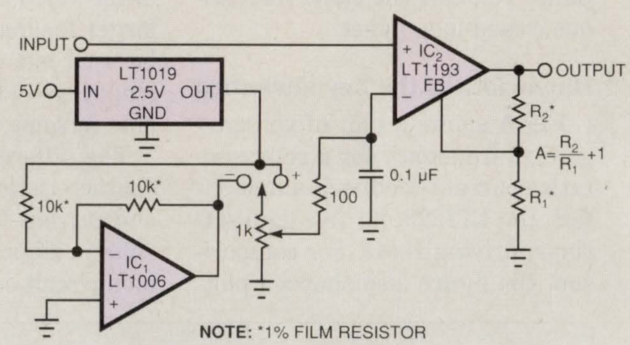


HORIZONTAL SCALE=50 nSEC/DIV

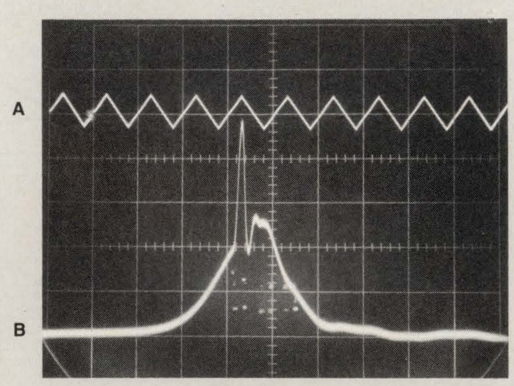
TRACE	VERTICAL SCALE
A, B	0.2V/DIV
C, D	2V/DIV

(b)

Fig 6—Methods to achieve high common-mode rejection include *transformer coupling. The amplifier in* ***a*** *responds to an input (****b****, trace A) with a slightly phase-shifted output (trace D). Traces B and C are T_1's secondary and T_2's primary, respectively.*



(a)



TRACE	HORIZONTAL SCALE	VERTICAL SCALE
A	20 μSEC/DIV	5V/DIV
B	2 μSEC/DIV	0.1V/DIV

(b)

Fig 7—By selectively amplifying *the portion of the signal you select, this differential-comparator amplifier* ***(a)*** *enables you to extract signal detail from a triangle waveform (****b****, trace A). At the triangle wave's peak (****b****, trace B), the triangle-wave generator's switching artifacts are clearly evident.*

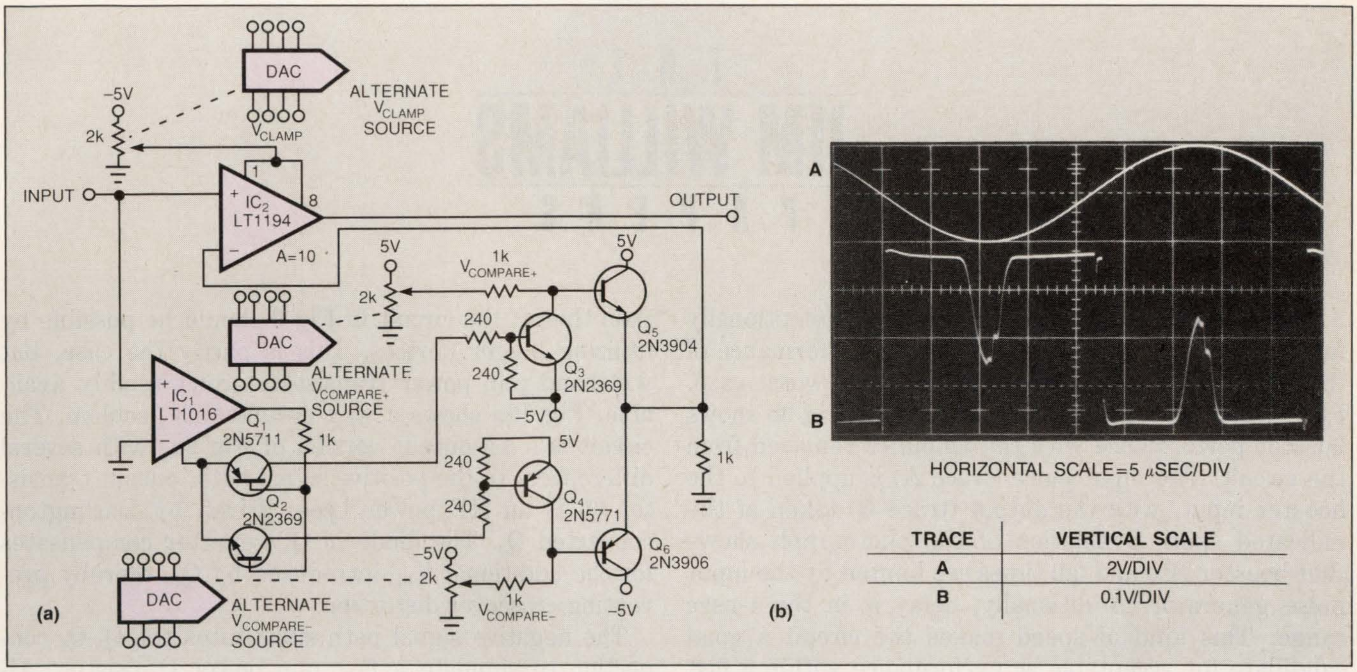


***Fig 8—A differential-comparator amplifier (a) allows** you to observe signals between two amplitude-defined points that you can set. The amplifier detects switching residuals (**b**, trace B) in the sine-wave generator's input (**b**, trace A).*

It is worth noting that this circuit performs the same function as differential plug-in units for oscilloscopes. This circuit's output is accurate and settles to 0.1% within 100 nsec after entering its linear region.

Window a waveform

Fig 8a extends the previous circuit's operation, allowing amplified observation of information between two amplitude-defined points that you can set. You can choose both the magnitude and sign of the amplitude setpoints. In this circuit, comparator IC_1's output state determines the polarity of the offset applied to IC_2's negative input. IC_1 compares the circuit's input to ground, generating polarity information at its outputs. Two level shifters, consisting of Q_1 and Q_3 and Q_2 and Q_4, bias followers Q_5 and Q_6. Positive circuit inputs result in Q_5 supplying the $V_{COMPARE+}$ potential to IC_2, whereas negative inputs route $V_{COMPARE-}$ to IC_2.

This additional circuitry eliminates the previous circuit's manual polarity switch, permitting automatic selection of the difference polarity and amplitude. Additionally, this circuit takes advantage of IC_2's input-clamp feature. This feature limits the dynamic range of the input, clamping the amplifier's input operating range. Signals inside the clamp limit are processed normally, while signals outside the limit are precluded from influencing the amplifier. This combination of circuit controls allows you to select very tightly defined "windows" on a waveform for accurate amplification without overload restrictions.

Fig 8b shows the circuit output for a sine-wave input (trace A) from the same function generator used to test the previous circuit. The V_+ and V_- compare voltages are set just below the sine-wave peaks, with V_{CLAMP} programmed to restrict amplification to the peaks' excursion. Trace B, the circuit's output, simultaneously shows amplitude detail of both peaks of the sine wave. The observed distortion is directly traceable to this generator's imperfect internal triangle waveform **(Fig 7b)**, as well as its sine-wave shaper characteristics.

Occasionally, it is necessary to supply larger output currents than an amplifier is capable of delivering. The power gain stage, sometimes called a booster, is usually placed within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics.

Because the output stage resides in the amplifier's feedback path, loop stability is a concern. This is particularly the case with high-speed amplifiers. You must consider the output stage's gain and ac characteristics to achieve good dynamic performance. Overall circuit phase-shift, frequency-response, and dynamic-load-handling capabilities are issues that you can't ignore when designing a power gain stage for a monolithic amplifier. The output stage's added gain and phase shift can cause poor ac response or outright oscillation. Judicious application of frequency-compensation methods is needed for good results. (See **Ref 1** for discussion and details on compensation methods.)

Fig 9a shows a 200-mA power booster used with a high-speed amplifier. Complementary emitter followers Q_1 and Q_5 provide current gain for positive signals, while Q_2 and Q_6 handle negative excursions. Q_3 and Q_4 are V_{BE}-based current limiters, turning on and thereby robbing drive from the appropriate output transistor when current exceeds about 300 mA. The diodes prevent reverse V_{BE} at Q_1 and Q_2 during current limiting. The 100Ω resistor and ferrite beads prevent the low-impedance amplifier output from causing Q_1 and Q_2 to oscillate **(Ref 1)**.

To be effective, the booster must be exceptionally fast. A slow design will obviate the ac performance of the amplifier by controlling it, or in the worst case, by causing oscillation (again, see **Ref 1**). **Fig 9b** shows booster performance with the amplifier removed from the circuit. The input pulse (trace A) is applied to the booster input, with the output (trace B) taken at the indicated spot. Evaluation of the photograph shows that booster rise and fall times are limited by the input pulse generator. Additionally, delay is in the 1-nsec range. This kind of speed makes the circuit a good candidate for acceptable ac performance within a fast amplifier's loop.

Fig 9c shows the pulse response with the LT1220 installed in the circuit driving a 50Ω load. The booster's high speed contributes negligible delay, and overall response is clean and predictable. The local 3-pF compensation across the amplifier optimizes response but is not absolutely necessary in this circuit. The input (trace A) produces a nicely shaped slew-limited output (trace B).

In theory, achieving higher power-booster stages than that of the circuit in **Fig 9** should be possible by utilizing bigger devices. This is partly the case, but wideband pnp power transistors aren't readily available. **Fig 10a** shows a way around this problem. The circuit is a 1A-output version of **Fig 9a**, with several differences. In the positive signal path, output transistor Q_4 is an RF power type, driven by Darlington-connected Q_3. The diode in Q_1's emitter compensates for the additional V_{BE} introduced by Q_3, thereby preventing crossover distortion.

The negative signal path substitutes the Q_5-Q_6 connection to simulate a fast pnp power transistor. Although this configuration acts like a fast pnp follower, it has voltage gain and tends to oscillate. The 2-pF feedback capacitor across Q_5's collector and base suppresses these parasitic oscillations and stabilizes the composite transistor. This circuit also includes a feedback-capacitor trim to optimize ac response. This trim capacitor, which is not included in the previous circuit, is necessary because of this circuit's slightly slower characteristics and much heavier loading. Current-limit

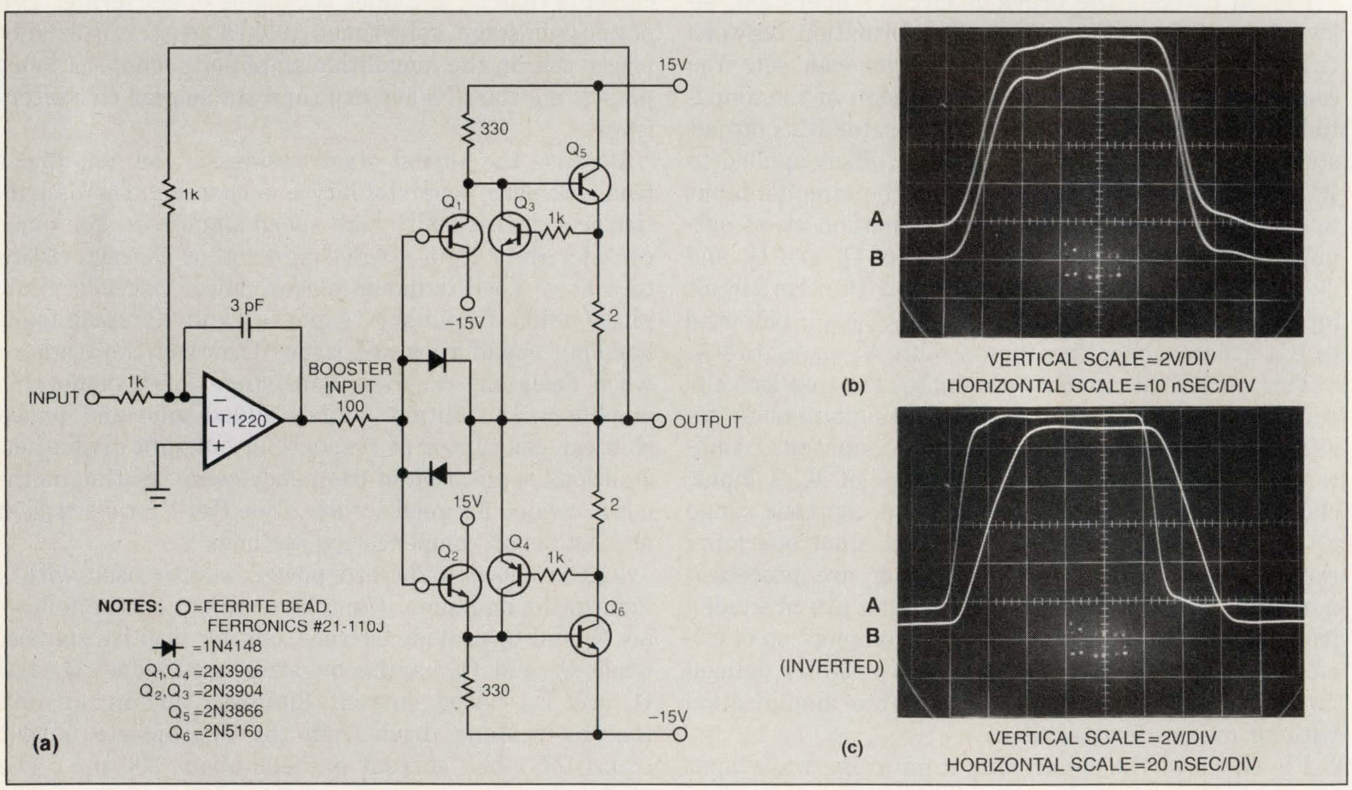
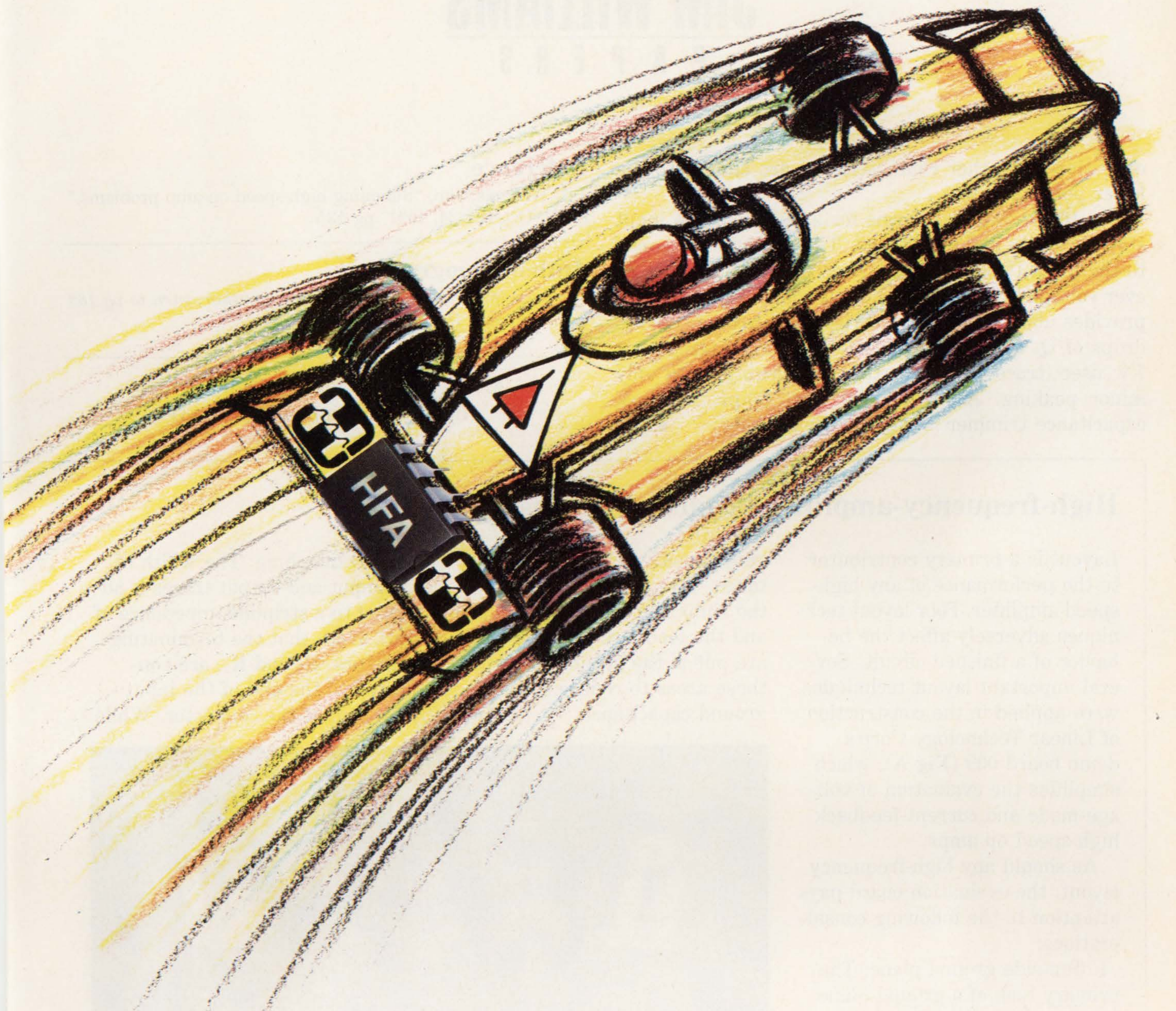


Fig 9—An additional booster stage increases *the output of this circuit's wideband amplifier to 200 mA* ***(a)****. The response of the booster* ***(b****, trace B) alone to a pulse input* ***(b****, trace A) must be sufficiently fast not to limit the high-speed amplifier. The delay between trace A and B of* ***b*** *is approximately 1 nsec, and the pulse generator's rise and fall times limit those of the boost circuit. When included in the amplifier's feedback loop, the booster's high speed contributes negligible delay, and overall circuit response* ***(c****, trace B) is clean and predictable.*



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operation and other characteristics are similar to the lower power circuit.

Fig 10b shows waveforms for a 10V negative input step (trace A) and a 10Ω load. The amplifier responds to the input (trace B), and drives the booster to whatever voltage is required to close the loop. The amplifier provides about 1.5V of overdrive to overcome the V_{BE} drops of Q_3 and Q_4. The booster output, lagging by a few nsec (trace C), drives the load cleanly, with only minor peaking. Adjusting the 5- to 30-pF feedback capacitance trimmer minimizes the peaking. EDN

Reference

1. Williams, Jim, "Subduing high-speed op-amp problems," *EDN*, October 24, 1991, pg 135.

Author's biography

For more information on this article's author, turn to pg 163 in the October 10, 1991, issue.

High-frequency-amplifier layout guidelines

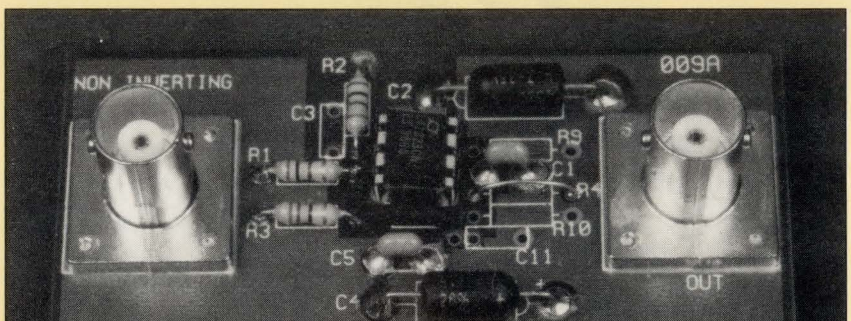
Layout is a primary contributor to the performance of any high-speed amplifier. Poor layout techniques adversely affect the behavior of a finished circuit. Several important layout techniques were applied in the construction of Linear Technology Corp's demo board 009 **(Fig A)**, which simplifies the evaluation of voltage-mode and current-feedback high-speed op amps.

As should any high-frequency layout, the evaluation board pays attention to the following considerations:

1. Top-side ground plane: The primary task of a ground plane is to lower the impedance of ground connections. The inductance between any two points on a uniform sheet of copper is less than the inductance of a thin, straight trace of copper connecting the same two points. The ground plane approximates the characteristics of a copper sheet and lowers the impedance at key points in the circuit, such as the grounds of connectors and supply bypass capacitors.

2. Ground-plane voids: Certain components and circuit nodes are very sensitive to stray capacitance. Two good examples are the summing node of the op amp and the feedback resistor. Voids are put in the ground plane in these areas to reduce stray ground capacitance.

3. I/O matching: The width of the input and output traces is adjusted to a stripline impedance of 50Ω. Note that the terminating resistors, R_3 and R_7, are connected to the end of the input lines, not at the connector. While



***This demo board embodies** a number of layout techniques crucial to the performance of high-speed amplifiers: top-side ground plane, ground-plane voids around critical nodes, and proper bypassing.*

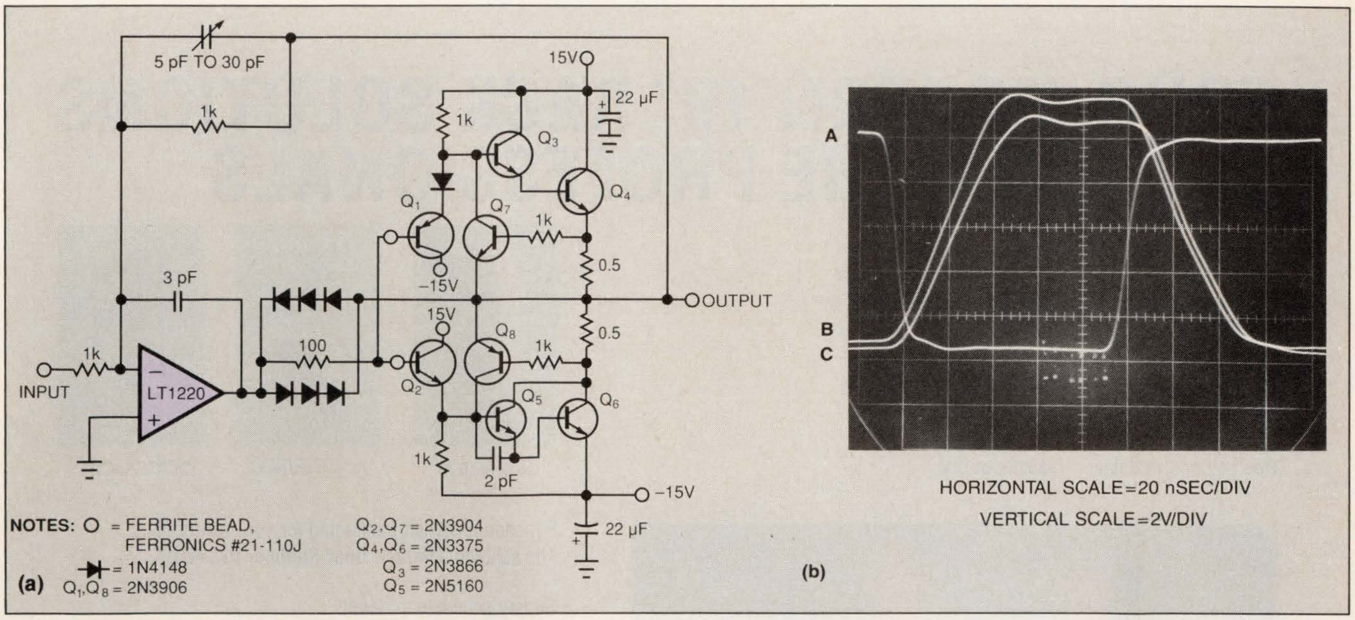


***Fig 10—Q₅ and Q₆ simulate** a fast pnp power transistor for this power booster **(a)**. The boosted op amp can drive a 1A load to 10V in 50 nsec. Trace A **(b)** is the 10V input, B is the op amp's output, C is the final circuit output.*

stripline techniques aren't absolutely necessary for the demo board, they are important on larger layouts where line lengths are longer. The short lines on the demo board can be terminated with 50, 75, or 93Ω without adversely affecting performance.

4. Separation of input and output grounds: Even though the ground plane exhibits a low impedance, input and output grounds are still separated. For example, the termination resistors, R_3 and R_7, and the gain-setting resistor, R_1, are grounded in the vicinity of the input connector. Supply bypass capacitors C_1, C_2, C_4, C_5, C_7, C_8, C_9, and C_{10} are returned to ground in the vicinity of the output connectors.

5. Proper bypassing: High-speed op amps work best when you bypass their supply pins with RF-quality capacitors. For example, C_1, C_5, C_8, and C_{10} should be 10-nF disc ceramic or other capacitors with self-resonant frequencies greater than 10 MHz. The polarized capacitors, C_2, C_4, C_7, and C_9, should be 1- to 10-µF tantalums. Most 10-nF ceramics are self-resonant well above 10 MHz, and 4.7-µF solid tantalums with axial leads are self-resonant at 1 MHz or below. Lead lengths are critical: The self-resonant frequency of a 4.7-µF tantalum drops by a factor of 2 when measured through 2-in. leads. Although a capacitor may become inductive at high frequencies, it is still an effective bypass component above resonance because the impedance is low.

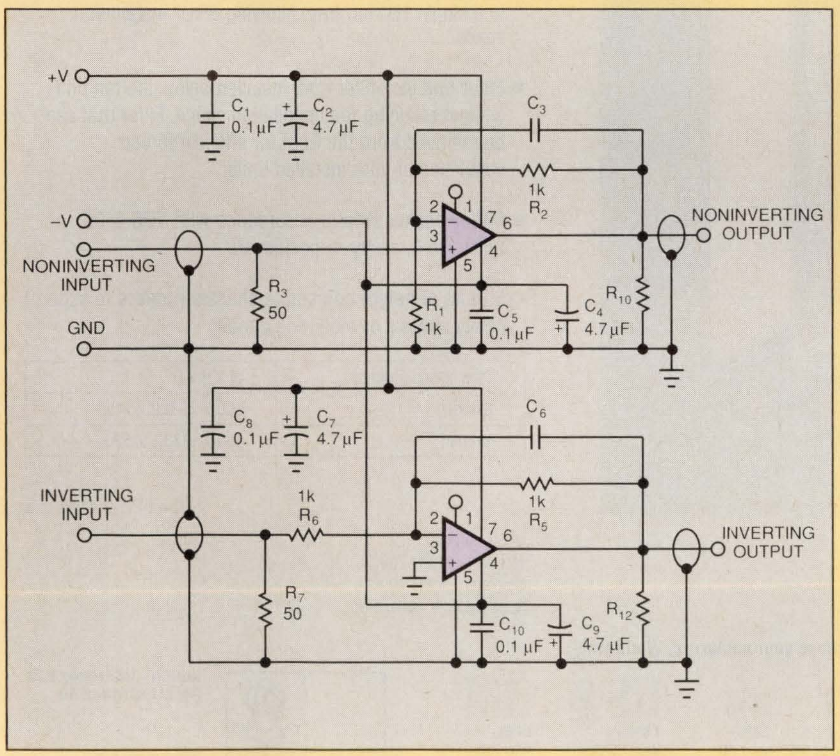


***Fig A—Mating the components of this schematic** to their placement on the demo board helps you visualize some high-frequency layout techniques and will help you transfer these techniques to your own high-speed boards.*

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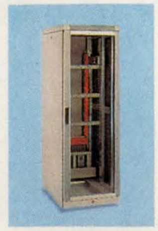
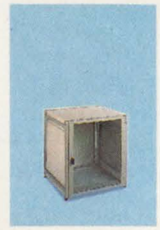
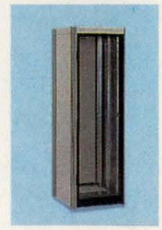

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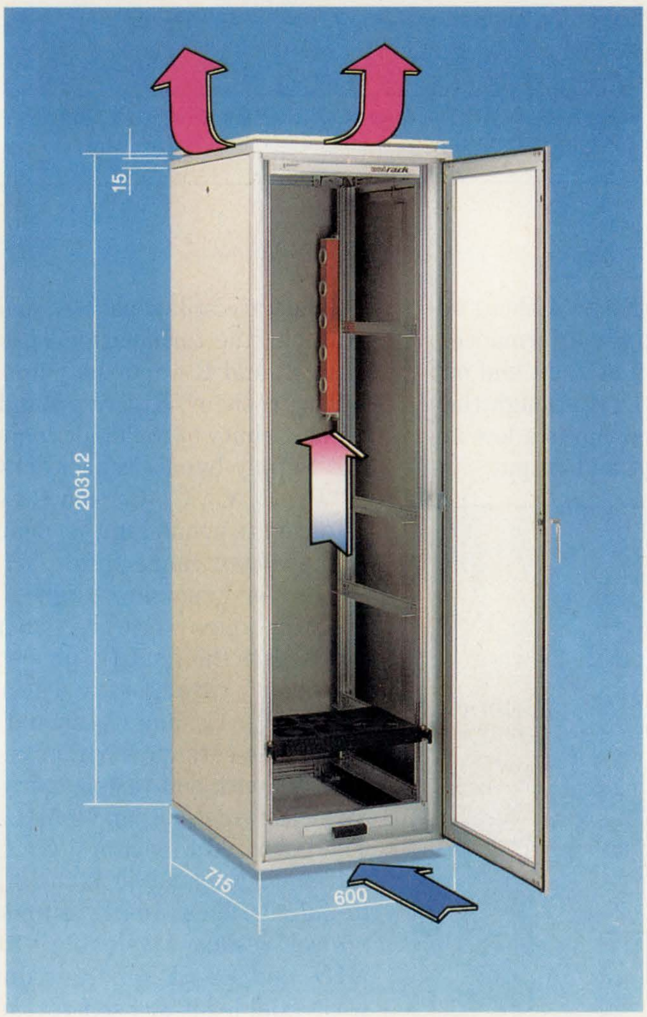

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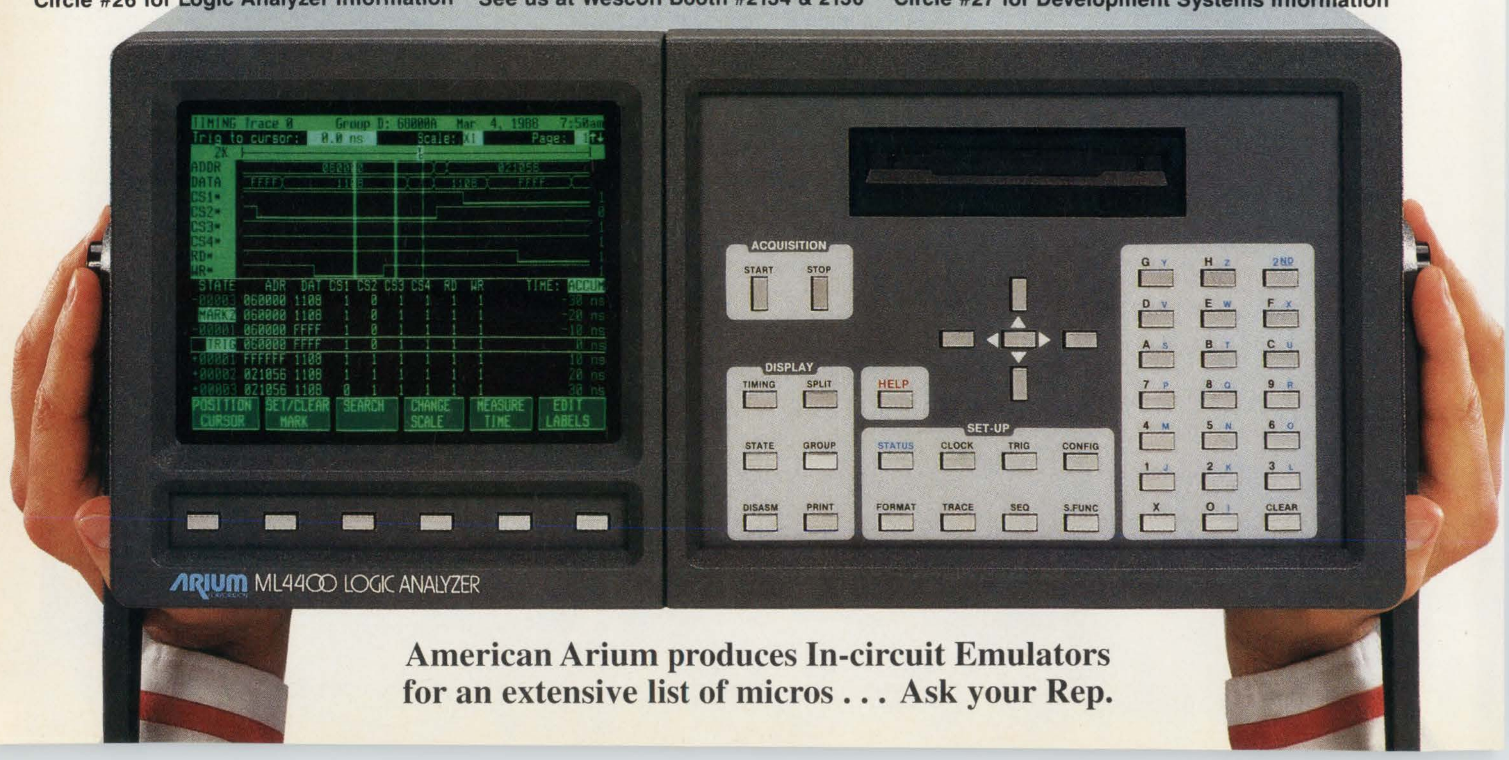

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Optical interrupter detects tiny parts

Leonard Schupak
Irvine, CA

Optical interrupters provide a reliable digital signal when the test part is larger than the interrupter's aperture. For smaller parts, however, the signal output becomes a function of the part size and the degree of saturation of the detector, especially if that detector uses a phototransistor or Darlington transistor. Detection may be missed entirely if the LED saturates the photodetector. Even if the detector doesn't saturate, detection is strongly dependent on temperature and optical-coupling efficiency. To overcome these difficulties, the circuit in **Fig 1** provides a controlled detection threshold and automatic, feedback-controlled adjustment of the LED output.

LED D_2 provides a reference level of about 1V at the input to IC_{1A}, which in turn controls D_1's current by comparing the photodetector's output with the voltage on C_1. The feedback-controlled amplifier maintains the LED current at the proper level and maintains the frequency response because of the large amount of feedback. The LED current is monitored by the peak detector composed of IC_{1B}, D_3, and C_2. This detector tracks very slow variations because of the presence of R_3. As long as D_3 is conducting, the Schmitt-trigger output at IC_{2A} remains high. When a small object interrupts the light beam, the LED current increases to maintain Q_1's output at the reference level. The peak detector goes negative at this point, disconnecting D_3 and switching IC_{2A}'s output low.

This closed-loop control system can accept varied part sizes. In fact, if the aperture is completely obscured, the LED current will saturate, but the detector current will continue to request a higher illumination. At the instant the obscured aperture begins to open, the circuit recovers rapidly because the illumination is already at its maximum level. Minimum part size is less than 1% of the aperture area.

The component values shown in **Fig 1** are representative of a typical interrupter. You can adjust R_1 and R_2 to suit a given mechanical configuration. Using the TLC272 for IC_1, the maximum LED current is about 6 mA. You can increase this current by adding a pnp emitter-follower stage and reducing the value of R_1. Because of the peak detector's very high sensitivity, the circuit may respond to background illumination at 60 or 120 Hz. You can reduce this sensitivity by simply eliminating the peak detector altogether—remove C_2 and R_3 and short out D_3. **EDN BBS /DI_SIG #1042**

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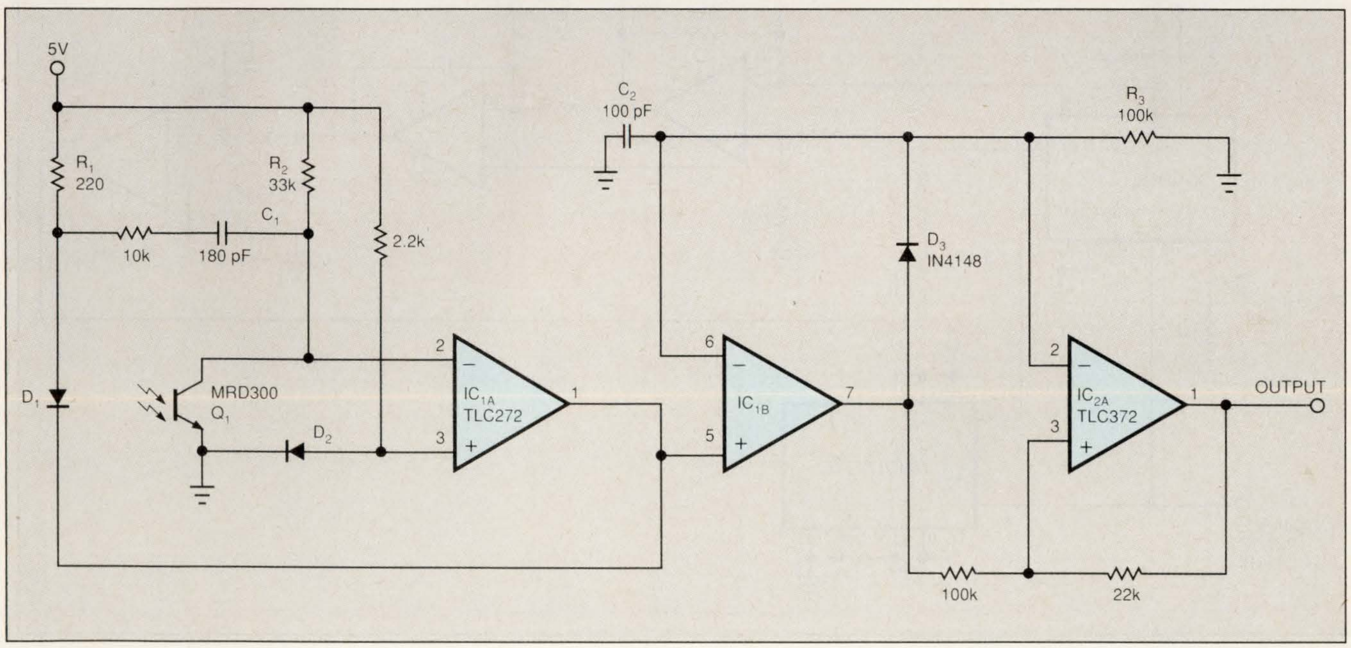

__Fig 1—By controlling LED output and detecting__ changes in LED current, this detection circuit won't overlook small objects.

Offset varies PLL's phase shift

Donald G Stefani
LeRoy, NY

By deliberately introducing a dc offset into the error-signal path of a phase-locked loop (PLL), you can add phase shift between the input reference and the feedback signal that drives the phase detector. The circuit in **Fig 1** has a phase-shift range of ±160° over a reference-signal range of 1 to 10 kHz. Because the loop uses an integrator, once set, the phase shift remains constant over the entire frequency range.

The positive-edge-triggered frequency/phase detector inside the CD4046B compares the frequency and phase of the input reference signal with the feedback signal from the 74HC193 counter. Since this phase detector is edge triggered, the duty cycle of the reference can be arbitrary. IC_{1A} level shifts the 3-state output of the phase detector. When in lock, if the positive edge of the reference leads the positive edge of the feedback signal, the output of IC_{1A} swings to its lower rail for the time interval between the two edges. IC_{1A}'s output then returns to 2.5V until the next positive edge of the reference occurs. If the positive edge of the reference lags the positive edge of the feedback, the output of IC_{1A} remains at the upper rail for the time interval between the two edges. It then returns to 2.5V until the next positive edge of the feedback occurs.

Using the quad LMC660C CMOS op amp for IC_{1A} permits dynamic-loop, error-voltage variations over almost the entire range of 0 to 5V. Adjusting the 20-kΩ potentiometer causes the phase shift to change because the average voltage of the pulses at IC_{1A}'s output must change to maintain the constant-feedback-forced value of 2.5V at IC_{1B}'s inverting input. A unity-dc-gain lead network stabilizes the loop. This design divides the output of the VCO by 16 before applying it to the phase-detector input. **EDN BBS /DI_SIG #1043**

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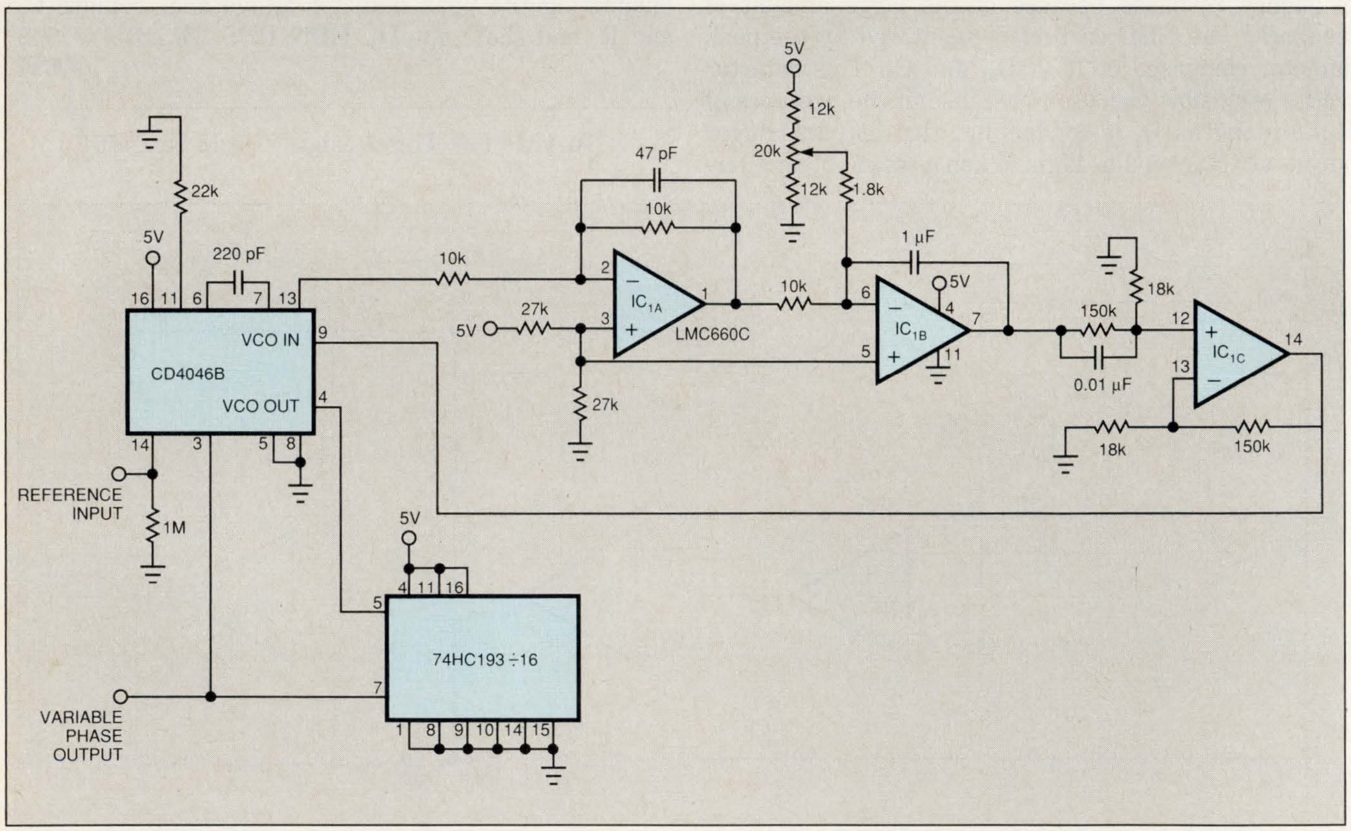

Fig 1—By introducing dc offset into this PLL's feedback, *you can vary the phase shift between its input and output by ±160 degrees.*

Backup time-out saves battery

Simha Pilot
Tadiran Electronic Industries, Rehovot, Israel

A single backup battery can provide power for multiple, limited-time backup periods. The circuit in **Fig 1** provides power for a time determined by an RC time constant without completely using up the battery. During regular operation, Q_1 is on and Q_3 is off. The load (R_L) connects to the main power through Q_1. When V_{CC} disappears, however, Q_1 turns off, and the positive pulse generated by Q_2 activates timer IC_1 for a predetermined period. During this period, Q_3 turns on the load current supplied by the backup battery.

The predetermined backup period, which can last from a few seconds to a few hours, is set by the values of R_1 and C_1 and equals $128 \times R_1 \times C_1$. If, during the backup period, the main power resumes, a reset pulse through R_2 and C_2 disconnects the backup battery from the load. When the main power source is active, the backup circuit draws less than 50 μA.

EDN BBS /DI_SIG #1045 EDN

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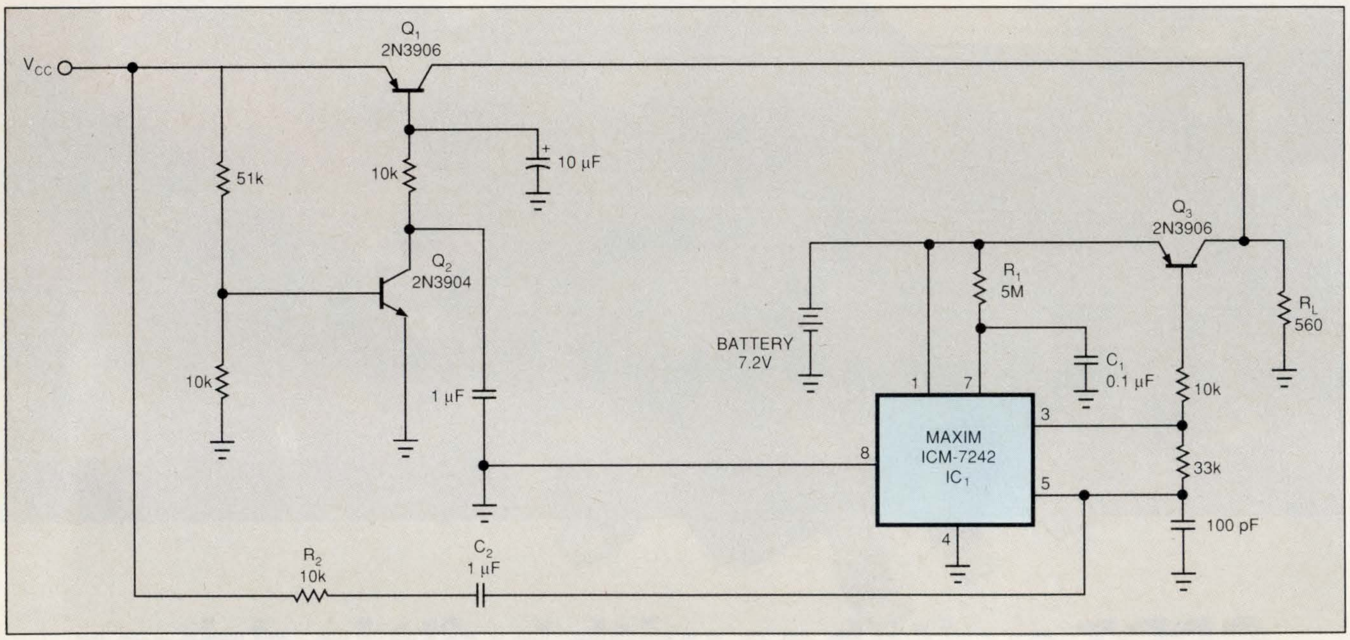

Fig 1—This limited-time battery-backup circuit conserves *your battery in those cases where only short main-power failures are expected.*

Isolation barrier preserves bandwidth

Giovanni Stochino
Arision-Ericsson FATME S p A, Rome, Italy

The interface circuit in **Fig 1** provides high isolation while maintaining wide bandwidth and low distortion. The circuit's bandwidth is 2.7 MHz when driving a 50Ω load. Its isolation is greater than 2.5 kV ac for 1 sec and greater than 1.4 kV ac for 1 minute. The circuit incorporates a suitable dc/dc converter to power those parts of the interface that need to be insulated from the output.

The circuit implements the isolation barrier that breaks the ohmic continuity between the input and output ports by optically coupling the signal path and

by using magnetic coupling within the converter. A pair of optocouplers form the core of the interface. The HCPL-4562 couplers are ideal for wide-bandwidth isolation because of their inherent high speed and linearity. This circuit uses local feedback through resistors R_1 through R_4 and collector-voltage bootstrapping via Q_1 through Q_4 and D_2 to increase the bandwidth and simplify the frequency compensation of the output amplifier.

Fig 1's input circuitry consists of an input amplifier, IC_1, that is referred to a floating common ground (note the schematic's two different ground symbols). The signal $-V_{REF1}$ biases IC_2's LED to ensure good linearity and dynamic range. The input circuit provides a high-impedance interface to the signal source and converts V_{IN} into a proportional current (I_1) that flows through IC_2's LED. The output circuit is a composite feedback amplifier whose input stage comprises the light-receiving diodes and respective transistors of IC_2 and IC_3. IC_4, D_1, and R_5 stabilize these transistors' collector currents at about 3 mA; their collector-emitter voltages are at an approximately 5.6V constant. These levels keep the amplifier frequency response and output offset voltage stable regardless of temperature and supply-voltage variations.

IC_6 establishes a linear relationship between V_{OUT} and the current I_2 flowing through IC_3's LED. This linear relationship is essential for achieving low distortion. The circuit in **Fig 1** also establishes a feedback loop around the output amplifier. Due to the feedback action and the high gain of IC_5, the circuit reaches a stable output state only when collector currents I_3 and I_4 are equal, that is, when the differential input stage is balanced. This technique of driving the LEDs with well-defined currents cancels out any influence in the input/output relationship if their forward voltages mismatch. R_6 and C_1 govern the frequency-response flatness of the entire isolation interface.

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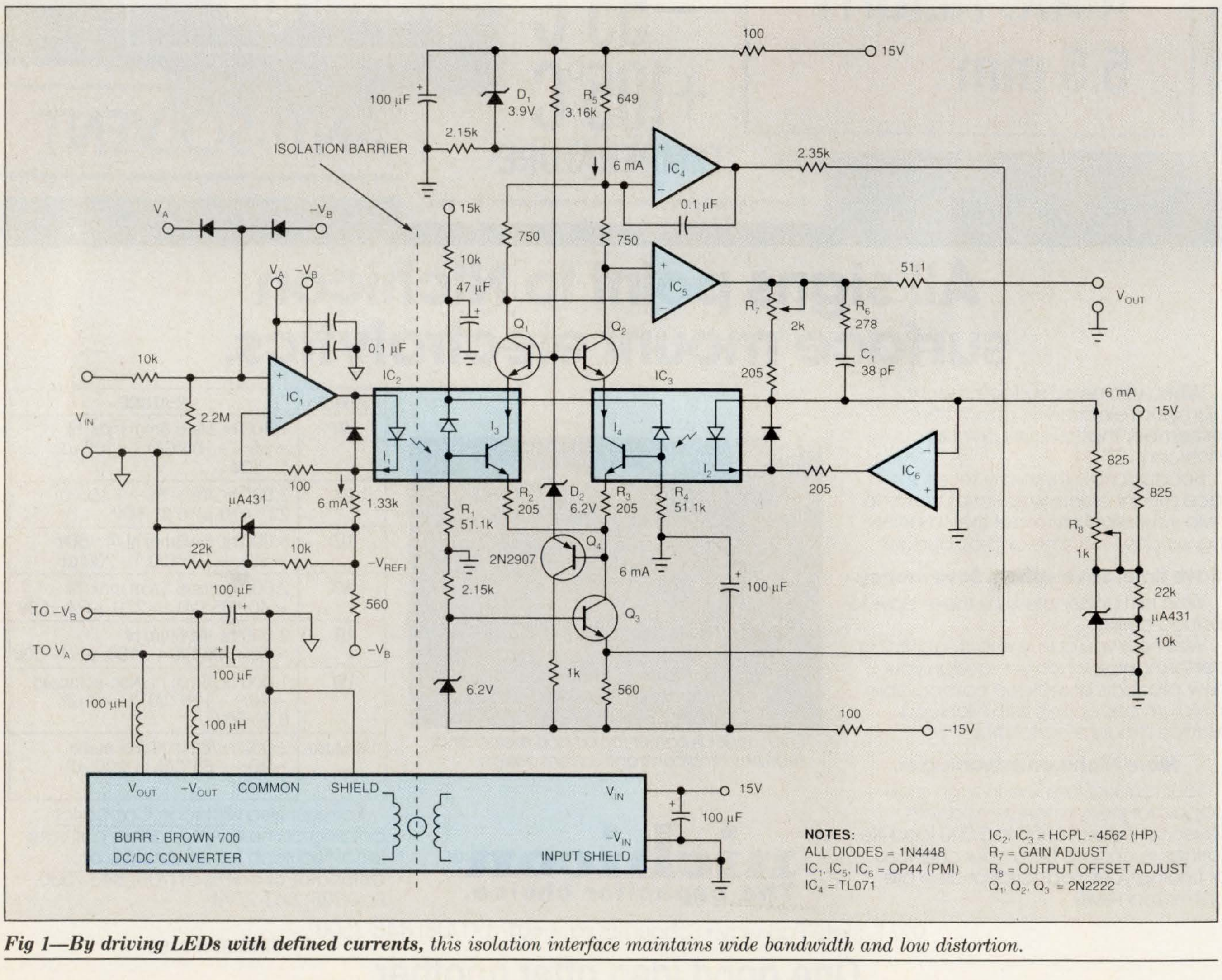


Fig 1—By driving LEDs with defined currents, *this isolation interface maintains wide bandwidth and low distortion.*

DESIGN NOTES

High Performance Frequency Compensation Gives DC-to-DC Converter 75µs Response With High Stability — Design Note 53

Ron Vinsant

This Design Note describes four high performance, low cost, 1.75A step-down converter circuits based on the LT1076 five terminal switching regulator. All four circuits have exceptional transient response; indeed, it is superior to most three terminal linear regulators. Transient response is important to loads that are switched on and off or that require high peak currents. Examples are digital circuits that are turned on and off, disk drive motors, stepper motors and linear amplifiers. The frequency compensation schemes shown in this Design Note, when compared to the usual R and C technique, allow greater variation in output capacitor ESR without causing stability problems. This is important in applications where wide temperature variations occur (which changes capacitor ESR) such as industrial control, automotive and military, and when the use of multiple capacitor vendors with different capacitor specifications is required.

Phase margin is always more than 50° and gain margin is a minimum of 18dB. Bode plots are available from the factory upon request.

The efficiency of these circuits is typically 80% with output ripple less than 50mV. Input voltages can be as high as 45V. Input ripple rejection is an exceptional 60dB due to the feedforward architecture of the LT1076. These circuits use a small number of external parts that are available off-the-shelf.

Many of the problems associated with five terminal switching regulators have been addressed by these circuits. Start-up overshoot is less than 5% with the optional soft start circuit. On recovery from a short circuit, a 10% overshoot is realized.

For a 15V output, line regulation is typically 0.06% (10mV) for a 20V to 40V input voltage change. Load regulation is difficult to measure; in fact, it is only 1mV to 2mV at the point of regulation. This applies to all output voltages.

Each circuit has been built in our lab and evaluated for stability, temperature, component life and tolerance. Two circuit options are shown: a simple soft start circuit and an output voltage adjustment (see Figure 1).

Inductors

The inductors shown in Table 3 are designed around two different core materials. The first is powered iron based for low cost. The second is tape wound steel for smaller size and higher efficiency but greater cost. For rapid evaluation of these circuits, powered iron cores are available in sample quantities from Micrometals at 1-800-356-5977. Completed inductors are available from Coiltronics at 305-781-8900.

Capacitors

Ripple current in the output capacitor is 150mA maximum with the input voltage at 40V and maximum load. At 35°C ambient estimated life-time with the specified capacitor and full load is 28 years.

The input capacitor, which undergoes higher stress, has a ripple current of 830mA maximum at 14V input and maximum load. The life-time of this capacitor is 14 years at 35°C. If the ambient temperature is higher, the life of the capacitor will be cut in half for every 10°C increase. The ESR specification affects the output ripple as well as frequency compensation. Its value of capacitance is not critical.

The capacitors in the frequency compensation network should be at least X7R ceramic, never Z5U, and, if broad temperature operation is expected, polyester or polycarbonate film caps should be used.

Manufacturing technologies must also be taken into account. If an IR furnace is used for soldering, use only ceramic capacitors. A wave or hand soldering operation is suggested for both film and electrolytic capacitors.

This is an area of continuing development so be sure to contact the capacitor manufacturers for temperature profiles.

Layout

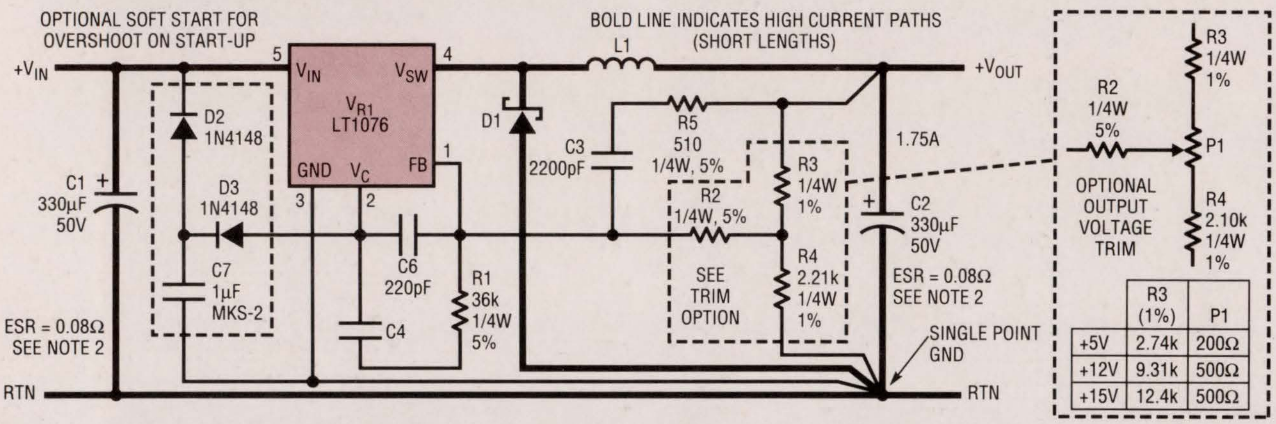
In order to achieve proper performance it is important to lay out the circuit as the schematic indicates. Use a single point ground at the output of the converter as shown. The term "short" indicates that the trace should be as short as possible between the two points shown. These traces should have a minimum width of 0.2 inches in 2oz. copper for a length of less than 1.5 inches. Traces longer than this should be avoided on the heavily shaded portions of the schematic.

Output Adjustment

A potentiometer can be added to the output divider string, provided the string does not change its overall resistance value. A table showing resistance values is shown with the schematic.

Heatsinking

Any heatsink of 30°C/W (~2 square inches) or lower will keep the LT1076 at an acceptable temperature up to a 70°C ambient. See LT1076 data sheet for further information.



NOTE 1: DO NOT SUBSITTUTE COMPONENTS WITHOUT COMPLETE EVALUATION.
NOTE 2: C1 AND C2 MUST BE 0.07Ω MIN ESR AT ROOM TEMPERATURE (25°C). UNITED CHEMICON SXE50VB331M10X30LL, SPRAGUE 672D337F020DM4D.
NOTE 3: ALL CAPS EXCEPT C1 AND C2 ARE WIMA FKC-2 OR X7R CERAMIC, ±10% TOLERANCE. WIMA 914-347-2474

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Figure 1. High Performance DC-to-DC Converter

Table 1. Components

#	V_{IN}	V_{OUT}	e (%) @ V_{IN}	L (μH)	D1	R2 (5%)	R3 (1%)	C4 (10%)
1	8V-20V	+5V	83% @ 10	75	MBR330P	1.5k	2.80k	0.0068μF
2	8V-40V	+5V	76% @ 24	91	MBR350	1.5k	2.80k	0.0068μF
3	15V-40V	+12V	86% @ 24	180	MUR415	1.2k	9.79k	0.01μF
4	18V-40V	+15V	86% @ 24	240	MUR415	1.2k	12.7k	0.01μF

Table 2. Performance

#	V_{OUT}	MIN LOAD	REGULATION (MIN TO MAX) LOAD	LINE	RIPPLE REJECTION 50Hz-400Hz	OUTPUT RIPPLE
1	+5V	0.200	0.1%	15mV	60dB	50mV
2	+5V	0.175	0.1%	15mV	60dB	50mV
3	+12V	0.175	0.1%	15mV	60dB	50mV
4	+15V	0.175	0.1%	15mV	60dB	50mV

Note 1: V_{IN} = 24V except #1 at 14V.
Note 2: Temperature = 25°C.
Note 3: Periodic and random deviation (P.A.R.D.).
With optional adjustment = ±2.5%.
Without optional adjustment = ±4.5%.

Table 3. Inductor

L (μH)	NUMBER TURNS	CORE	COILTRONICS P/N	SMALLER TOROID
75	37 #18	T68-52A	CTX75-2-52	CTX75-2-KM
91	38 #18	T80-52B	CTX91-2-52	CTX91-2-KM
180	53 #18	T80-52B	CTX180-2-52	CTX180-2-KM
240	61 #18	T80-52B	CTX240-2-52	CTX240-2-KM

Note 1: ΔL with DC current is 20% max.

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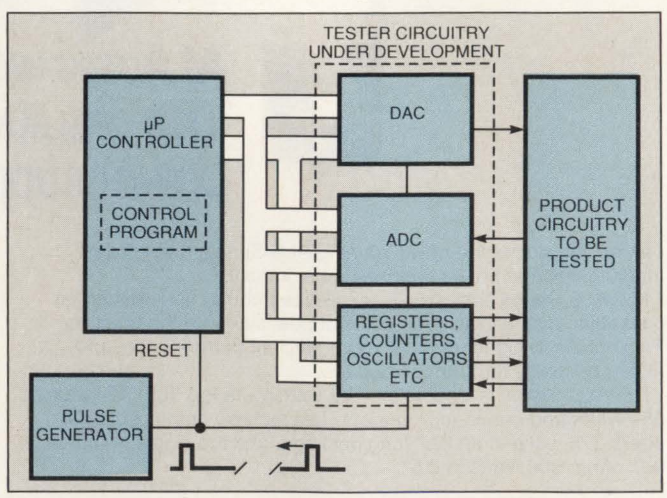

***Fig 1—By connecting a pulse generator to your system's** software and hardware reset points, you can manipulate reset pulses to coincide with failures, and thereby more easily find design errors.*

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Entry blank must accompany all entries. Design entered must be submitted exclusively to EDN, must not be patented, and must have no patent pending. Design must be original with author(s), must not have been previously published (limited-distribution house organs excepted), and must have been constructed and tested. Fully annotate all circuit diagrams. Please submit software listings and all other computer-readable documentation on a 5¼-in. IBM PC disk.

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In submitting my entry, I agree to abide by the rules of the Design Ideas Program.

Signed ______________________________

Date ______________________________

ISSUE WINNER

The winning Design Idea for the June 20, 1991, issue is entitled "Low-battery detector polls threshold," submitted by Yongping Xia of Department of Electrical and Computer Engineering, West Virginia University (Morgantown, WV).

ISSUE WINNER

The winning Design Idea for the July 4, 1991, issue is entitled "Ordinary DMM measures high resistances," submitted by Alfred E Hess of Boulder, CO.

FEEDBACK AND AMPLIFICATION

Hardware change saves cycles

I have just received a letter from Design Ideas Editor Charles H Small suggesting a change to my Design Idea, "Z80 acquires extra interrupt lines," in the August 19, 1991, issue. The suggested change is to connect the 8259's D_0, D_1, and D_2 lines to the Z80's D_1, D_2, D_3 lines. The purpose of the change is to multiply the interrupt vector by 2, thus simplifying the interrupt-vector jump table.

You are right! If you pay special attention to writing command words and reading status words (which will also be shifted), it is an ingenious solution.

András Pomozi
H-1025. Budapest
Tömörkény út 15/d.
Hungary

Contributor writes from China

I was delighted to hear from EDN. I didn't receive the letter you sent on March 27, by air mail, until June 17. By the end of June, I received your second letter and the check for my Design Idea. It took almost a month.

Though the post office delayed your letters much too long, I was very happy. I thank you for your encouragement and help. Without your appreciation, I might never have been published in a foreign country. This is a great success for me. I don't know how to express my thankful feelings so, as my workmates suggested, I am sending some Chinese paper cuttings to you.

The large one is an eagle, which symbolizes EDN's power, wisdom, and bright future. The others are little animals which symbolize that EDN has great glamour for the world's readers. We all love her. I hope you enjoy them.

Shu Zheng Ping
Computer Center
Central South University of Technology
Shangsha City, Hunan Province, PRC

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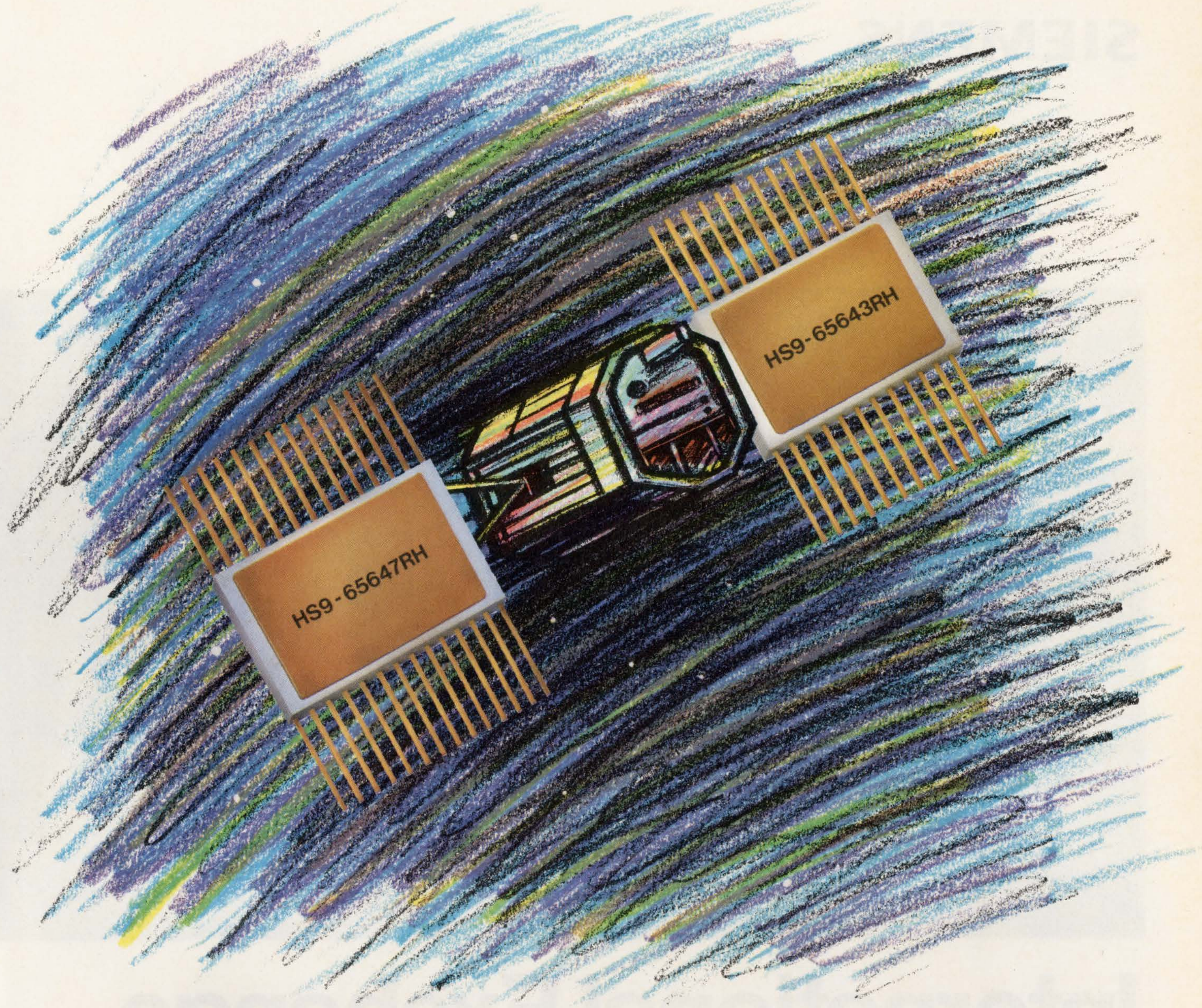

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CIRCLE NO. 97

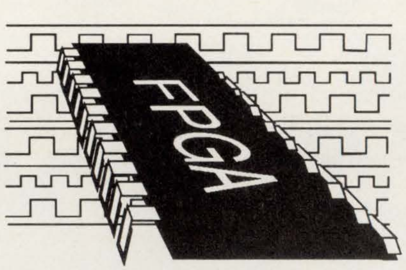
CAE Technology Report

Multiple FPGAs

Growing circuit size and complexity, coupled with board real estate constraints, are today, forcing more and more designs into FPGAs. This trend has caused many designers to use multiple FPGAs in a single design and even multi-vendor FPGAs in the same circuit. However, CAE tools have not kept pace with this development, and most simulators today can support only a single FPGA in a design. ALDEC Inc., Newbury Park, CA., has responded to this challenge with a new release of its SUSIE logic simulator which now supports simulation of circuits containing multiple same-vendor FPGAs and even multiple-vendor FPGAs. This development means shorter verification cycles, since multiple simulation passes for the same design is now unnecessary.

"Design Viewing Aperture" Technology

Today, designs are becoming increasingly larger and more complex. It is not uncommon to routinely have circuits over 300,000 gate-equivalents. However, during the logical verification phase of the design process, designers are usually interested in only a small part of the design at any given time. Because of their "batch" orientation, traditional simulators have forced the engineer to compile and simulate the entire design. The SUSIE logic simulator, release 6.0 from ALDEC Inc., solves this problem by supporting partial simulation. This feature allows the designer to choose the portion of the design on which he/she wishes to focus and to simulate just those components. The result is more manageable simulation results and shorter deisign cycles.



Modelling Made Simple

With the emphasis today, on system level design in general and VHDL capability in particular, device modelling has taken on much more significance, and many suppliers have stepped in to fill this void. However, most designers are still discovering that some of their more esoteric parts are unavailable in model form. VHDL has gone a long way in curing this ill, but has a rather steep learning curve. Now ALDEC Inc. Newbury Park, CA has taken this one step further by introducing MOBIC 6.0, the new modelling capability that makes device modelling a cinch. MOBIC lets modellers build models by using Boolean equations and also by specifying a model by its output waveforms. This form of behavioral modelling negates the need for detailed knowledge of the internal architecture of a device, thereby facilitating quick-turn models for simulation.

Xilinx 4000 FPGAs Support

By announcing support of the new XC4000 FPGAs from Xilinx by SUSIE 6.0 simulator, ALDEC Inc. has cemented its position as a leader in the CAE market place. This development means that designers can continue to simulate their entire designs even if they contain the latest Xilinx technology. ALDEC also recently released SUSIE/XNF, which simulates single FPGA designs in any of XC2000, XC3000 or XC4000 technologies. The XNF/VT library is also available for SUSIE-CD board level simulator to verify multiple Xilinx FPGAs at the board level. Interest in designs using XC4000 technology is now shifting from research departments into mainstream design organizations. SUSIE 6.0, by supporting this new FPGAs family is helping to support this trend.

New Simulation Alternatives

ALDEC Inc. has introduced a new family of dedicated simulation products targeted at the FPGA market. These stand-alone simulation engines are meant to support a variety of FPGAs from different vendors. There is the SUSIE/ACT which is the dedicated engine for ACTEL ACT and ACT2 parts, SUSIE/MAX, a similar product for Altera MAX parts and SUSIE/XNF for Xilinx parts. Because each product offers full timing and functional capability, designers who need to simulate only a single device are able to purchase simulation capability for a fraction of the cost of the full-board simulator, SUSIE-CD. In addition, since each of these stand-alone units is fully compatible with SUSIE-CD, single-chip simualtions can be modified to the full-board level with complete data integrity.

Selective Simulation

In the traditional approach to logic simulation, it was imperative that models be available for all devices in a design BEFORE a simulation run could be started. This was due to the compilation requirements of "batch-oriented" simulators. What this meant was that even if a single model was missing, simulation could not proceed. But now, with the release of SUSIE 6.0 from ALDEC, the designer is not hamstrung by the lack of models. Simulation can be performed with missing or incomplete (FPGA) models. No longer does the designer have to "design" the entire circuit before starting simulation. This new feature facilitates true incremental design and results in shorter design cycles and greater design flexibility.

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Conversion-Function IC For Projection TV

- *Generates complex waveforms*
- *Capable of multistandard operation*

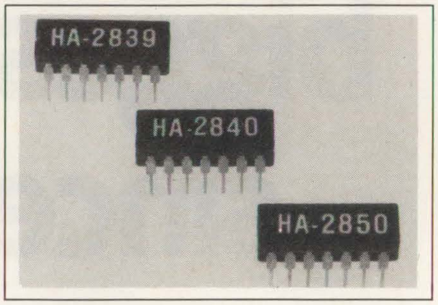
The MC44615 waveform generator provides the necessary ramps, parabolas, and cubic and combination waveforms for application to the convergence control circuitry in projection TVs. The device provides a total of 18 waveforms, 9 positive and 9 negative, which are of constant amplitude and independent of frequency. The waveforms are synchronized to horizontal frequencies to 64 Hz, and to vertical frequencies of 50 to 120 Hz. Other key features and specifications include complementary outputs, phase-locking of the internal horizontal oscillator to the external sync signal, blanking control of output waveforms, and adjustable horizontal time delay from the sync input to the waveform output. The IC, which operates from a ±5V supply, comes in a 40-pin DIP. \$3.66 (10,000).

Motorola Inc, Analog IC Div, EL340, 2100 E Elliot Rd, Tempe, AZ 85284. Phone (602) 897-3615. FAX (602) 897-4193. **Circle No. 355**

Wideband Op-Amp Family

- *Bandwidths to 600 MHz*
- *Slew rates to 625V/µsec*

Optimized for high-speed signal processing, the HA-2839, HA-2840, and HA-2850 op amps compete in price and performance with the EL2039, EL2040, and AD840. The HA-2839 and HA-2840 feature 625V/µsec slew rates and 600-MHz gain-bandwidth products. The HA-2850 offers a 340V/µsec slew rate and a 470-MHz gain-bandwidth product. All three devices also feature an input noise voltage of only 6 $nV/\sqrt{Hz}$. An input-offset voltage of 0.6 mV provides input precision, eliminating the need for a precision front-end amplifier. The full-power band-



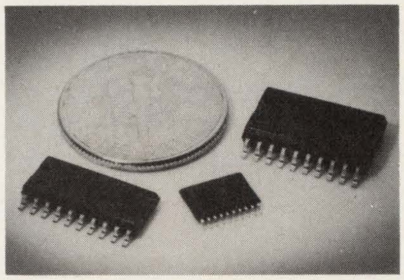
width of 10 MHz (10V step) for the 2839 and 2840, and 5.4 MHz for the 2850 satisfy high-resolution video applications. A complementary bipolar dielectric-isolation process keeps maximum supply currents to 15 mA for the 2839 and 2840, and only 8 mA for the 2850. The op amps are available in 8- and 14-pin plastic DIPs. $3.55 to $3.95 (100).

Harris Semiconductor, Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1132. **Circle No. 356**

Dual-Channel Read/Write IC

- *For 2-terminal MIG heads*
- *Comes in a 20-pin thin SO package*

The HA166102T read/write circuit is encapsulated in a 20-pin plastic, thin small-outline package. It measures 4.4×6.7×1.1 mm. The small size aids the miniaturization efforts critical in 1.8- and 2.5-in. drives. In larger 3.5-in. drives, the device's small size allows placement directly on the actuator arm. Special circuitry optimizes the chip for use with the newer 2-terminal MIG (metal in gap) read/write magnetic heads. The chip's write driver has a detection circuit that inhibits write operations at low supply voltages, and its read amplifier features a differential gain of 250 and low noise. The circuit operates from a 5V supply, and a standby function limits current drain to 1 mA typ in the idle mode. $3.45 (1000).



Hitachi America, Semiconductor Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (415) 589-8300. **Circle No. 357**

High-Speed FET Op Amp

- *Bandwidth is 35 MHz*
- *Typical input bias current is 5 pA*

The OPA671 FET-input op amp is fabricated in the company's Difet process. It features a gain-bandwidth product of 35 MHz, a 100V/µsec slew rate, and a 0.01% settling time of 240 nsec. Complementing the ac performance is a typical input bias current of only 5 pA, approximately one-millionth that of most bipolar-input wideband op amps. Output voltage-swing capability is ±10.5V with a 200Ω load. The op amp operates from ±4.5 to ±18V supplies and is specified for the industrial temperature range. 8-pin plastic DIP, $5.95 (100).

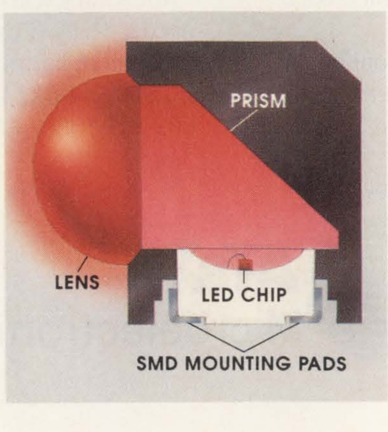
Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510.

Circle No. 358

INTRODUCING PRISM CBI℠
THE FIRST TRUE SURFACE MOUNTABLE LED INDICATOR.

The new surface mount CBI from Dialight is another breakthrough idea whose time has come. Instead of bending the leads on a through-hole version to make it look like a surface mount device, Dialight uses a patented high transmission prism and clear lens to bend the light from an upwards-facing surface mount LED. This approach offers a uniform illumination of the lens over a wide viewing angle. Finally, a truly leadless indicator developed for reflow-soldering and compatible with a wide variety of pick and place equipment.

The PRISM CBI is available in T-3/4 (1mm), T-1 (3mm) and T-1 3/4 (5mm) lens sizes. This unique product is offered in package sizes of 0.130 x 0.098 x 0.138 for the T-3/4, 0.240 x 0.185 x 0.200 for the T-1 and 0.250 x 0.245 x 0.282 for the T-1 3/4 size.



The introduction of the PRISM CBI means there is one less component on the board that has to be through-hole mounted because now a reliable surface mount version exists. Using this approach, an extremely high "post-process" reliability rate can be achieved.

Available in red, yellow or green, packaged in ESD-shielded tape on EIA standard 7" or 13" reels, the PRISM CBI is ready for a whole spectrum of demanding SMD applications.

For more information, contact:
Dialight Corp., 1913 Atlantic Ave., Manasquan, NJ 08736; Tel.: (908) 223-9400 Fax: (908) 223-8788.

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- *Totally sealed construction*
- *Available in 4-pole versions*

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Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600. **Circle No. 359**

Touchscreen Display

- *Displays 6 lines of 48 characters*
- *Includes a message memory*

Model PEP 4283-AX combines a 6-line × 40-character, vacuum fluorescent display with an optoelectronic touch input system. The unit features a RAM message memory that can accommodate as many as 127 240-character messages. The unit operates on 5V and has RS-232C (with CTS and DTR) and RS-422 interfaces. A switch border around the display area can be used for fixed function switches defined by custom artwork as specified by the user. Error-checking routines protect RAM data integrity and monitor software execution. PEP-WARE programming software allows designers to use a PC to compose display messages utilizing standard keyboard functions. Messages can be stored in the PC or the display's memory and recalled for editing. The programming software allows the programmer to determine the HEX coordinates of any location on the screen simply by touching that area. The unit will operate over a −40 to +85°C range. $800 (100).

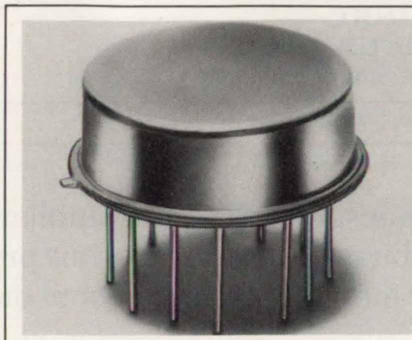
IEE Inc, Industrial Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311, ext 418. FAX (818) 901-9046.

Circle No. 360

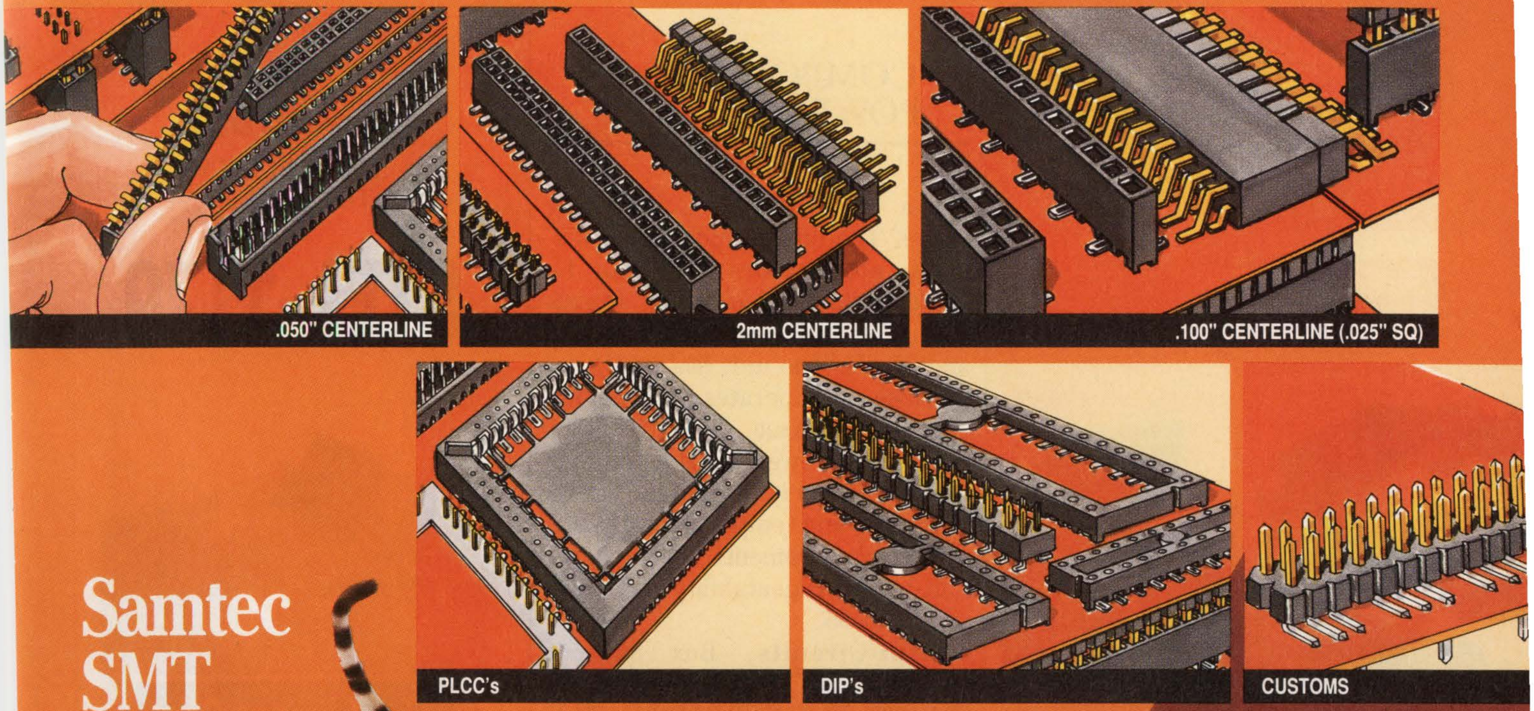
TTL-Controlled Attenuator

- *Housed in a hermetically sealed TO-8 package*
- *Operates to 1000 MHz*

The TOAT-51020 TTL-controlled precision attenuator is housed in a



hermetically sealed TO-8 package. It provides accurate attenuation over a 10- to 1000-MHz span and



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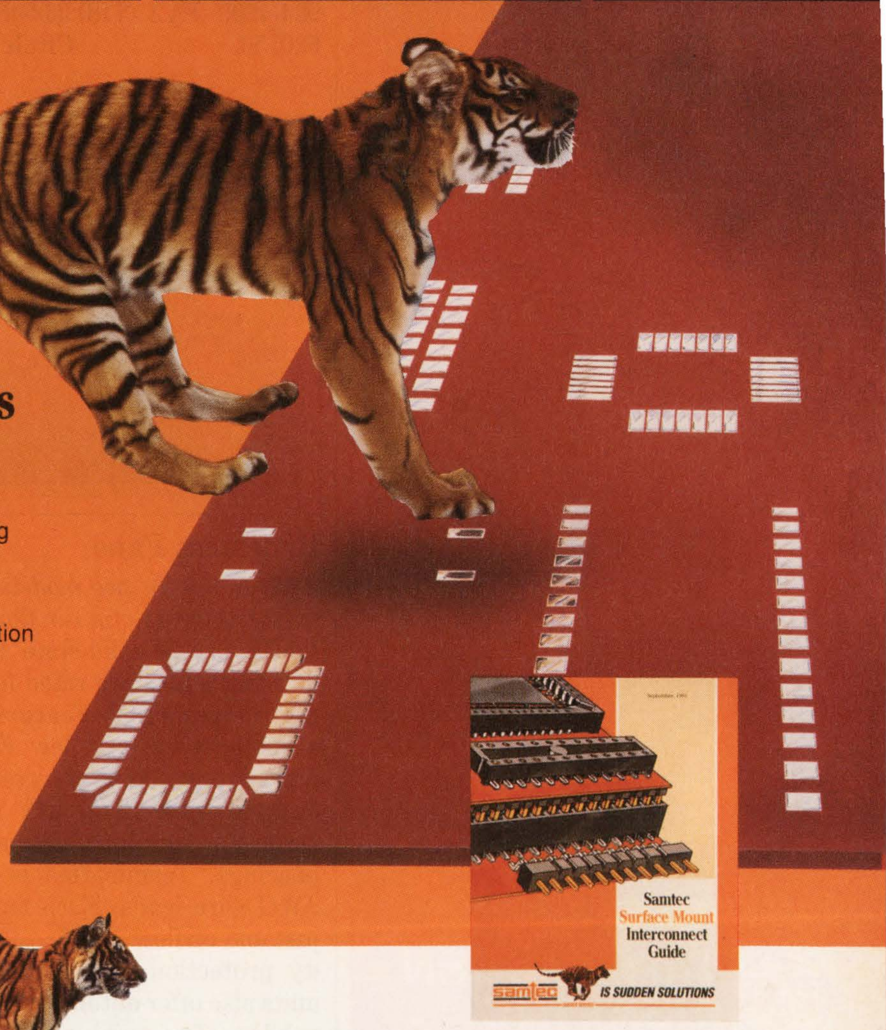

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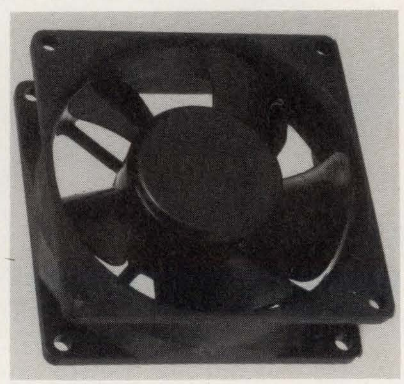
CIRCLE NO. 118

has a −55 to +100°C operating range. The unit includes three discrete attenuators that can be switched to produce seven attenuation levels—5, 10, 15, 20, 25, 30, and 35 dB. The unit has a 50Ω impedance and operates at switching speeds of 6 μsec. The attenuator can handle power levels as high as 0 dBm and can withstand the shock, vibration, and temperature stresses of MIL requirements. Three-sigma unit-to-unit repeatability is guaranteed. $55.95.

Mini-Circuits, Box 350166, Brooklyn, NY 11235. Phone (718) 934-4500. FAX (718) 332-4661. TLX 620156. **Circle No. 361**



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- *Rated for 53-cfm air flow*

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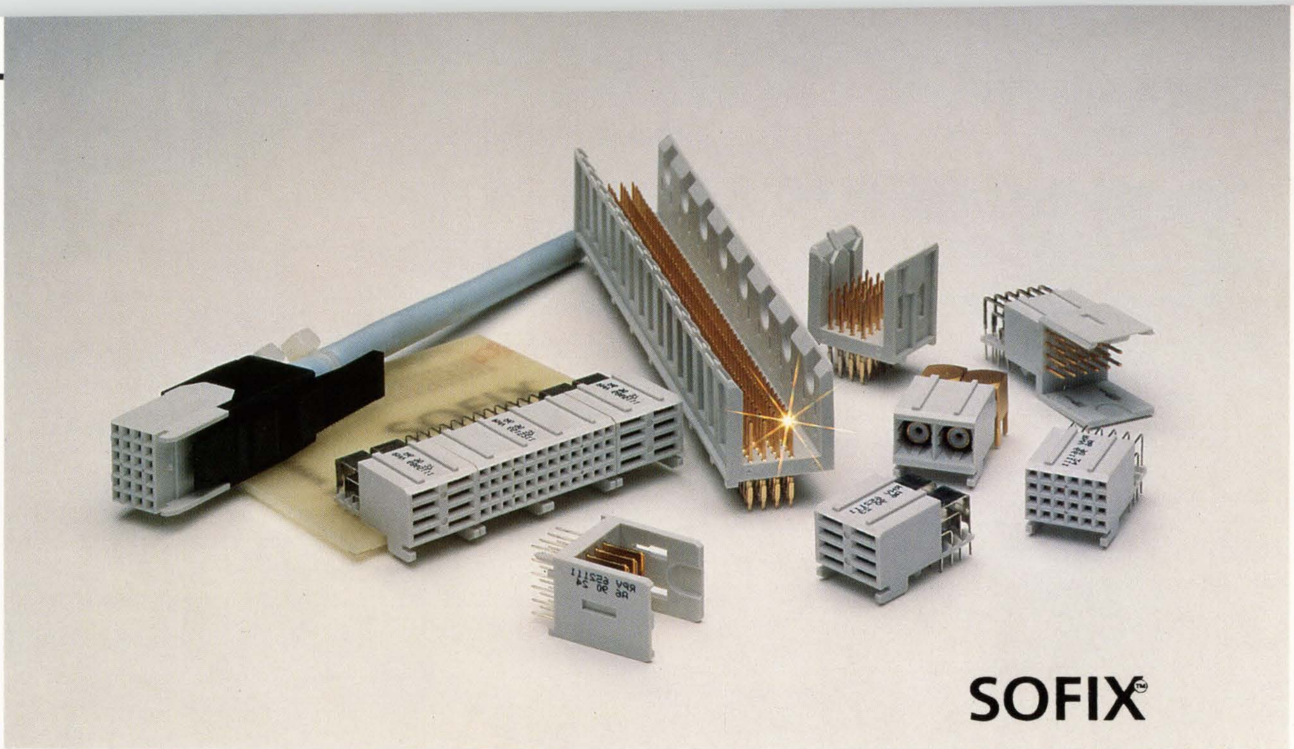
Interfan, Box 4188, Burlingame, CA 94011. Phone (415) 347-1203. FAX (415) 340-1670.

Circle No. 362



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* Standardization

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* Easy-to-assemble w/Hot Riveting tool.
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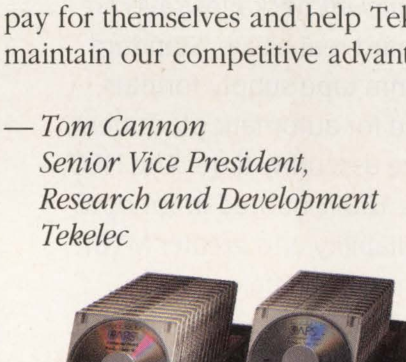

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CIRCLE NO. 116

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μF / VDC	2.5	4	6.3	10	16	20	25	35	50
0.047								A	
0.068								A	
0.10						A_2		A	A
0.15						A_2		A	A
0.22						A_2		A	B_2
0.33						A_2		A	B_2
0.47						A_2	A	A·B_2·B	B_2
0.68					A_2	A_2·A		A·B_2·B	C
1.0				A_2	A_2·A		A	B_2·B	C
1.5			A_2	A_2·A	A	A	B_2·B	B_2·B·C	
2.2		A_2	A_2·A	A	A	B_2·B	B_2	B_2·B·C	D
3.3		A_2·A	A	A	A·B_2·B	B_2	B_2·B·C	C·D	
4.7	A_2	A	A	A·B_2·B	B_2	B_2·B·C	C	D_2·D	
6.8		A	A·B_2·B	B_2	B_2·B·C	C	D_2·D	D_2·D	
10		A·B_2·B	B_2	B_2·B·C	C	C·D_2	D_2·D		
15	A	B_2	B_2·B·C	C	C·D_2	D_2·D			
22		B_2·B·C	C	C·D_2·D	D_2·D	D_2·D			
33		C	C·D_2·D	D_2·D	D_2·D				
47		C·D_2·D	D_2·D	D_2·D					
68		D_2·D	D_2·D						
100		D_2·D							

	W	L	H
A_2 case	1.6 (.063)	3.2 (.126)	1.2 (.039)
A case	1.6 (.063)	3.2 (.126)	1.6 (.063)
B_2 case	2.8 (.110)	3.5 (.138)	1.9 (.075)
B case	2.6 (.102)	4.7 (.185)	2.1 (.083)
C case	3.2 (.126)	6.0 (.236)	2.5 (.098)
D case	4.3 (.169)	7.3 (.287)	2.8 (.110)
D_2 case	4.6 (.181)	5.8 (.228)	3.2 (.126)

mm (inch)

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NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

Analysis Tool For Routing Ability

- *Provides a quick estimate of routing ability*
- *Analyzes as many as 48 signal layers*

The Allegro Placement Evaluator is a module within the Allegro Design System. It analyzes component placement on pc boards, multiwire boards, hybrids, and multichip modules to determine whether they can be manufactured. You can constrain the analysis by the number of signal layers and for feature sizes and spacings. The software, because it understands the routing algorithms of its companion tool, evaluates and predicts likely areas of congestion. Analysis output consists of a color map representing density and overflow areas. A trace map identifies the particular nets likely to try to traverse the congested areas. The Placement Evaluator is included as part of the Allegro 5.0 release and is free to users on software support. Allegro 5.0, $12,500 to $50,000.

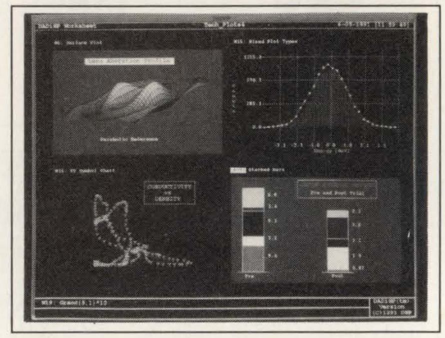
Valid, 2820 Orchard Pkwy, San Jose, CA 95134. Phone (408) 432-9400. FAX (408) 432-9430.

Circle No. 363

Graphical Spreadsheet

- *Permits as many as 100 windows*
- *Allows zooming, scrolling, and overlaying graphs*

Dadisp (Data Analysis and Display) 3.0 is an analysis tool that operates as a graphical spreadsheet. The software allows you to input data in several formats from numerous sources, including ASCII, 8-bit byte, 16-bit integer, IEEE floating point, binary files, or most data-acquisition systems. The software can perform matrix math functions



such as invert, balance, and rotate. Such 3-D graphics as contour plotting, depth- or height-density plots, XYZ surface plots, and spectral plots are supported as are a range of 3-D manipulation functions. As

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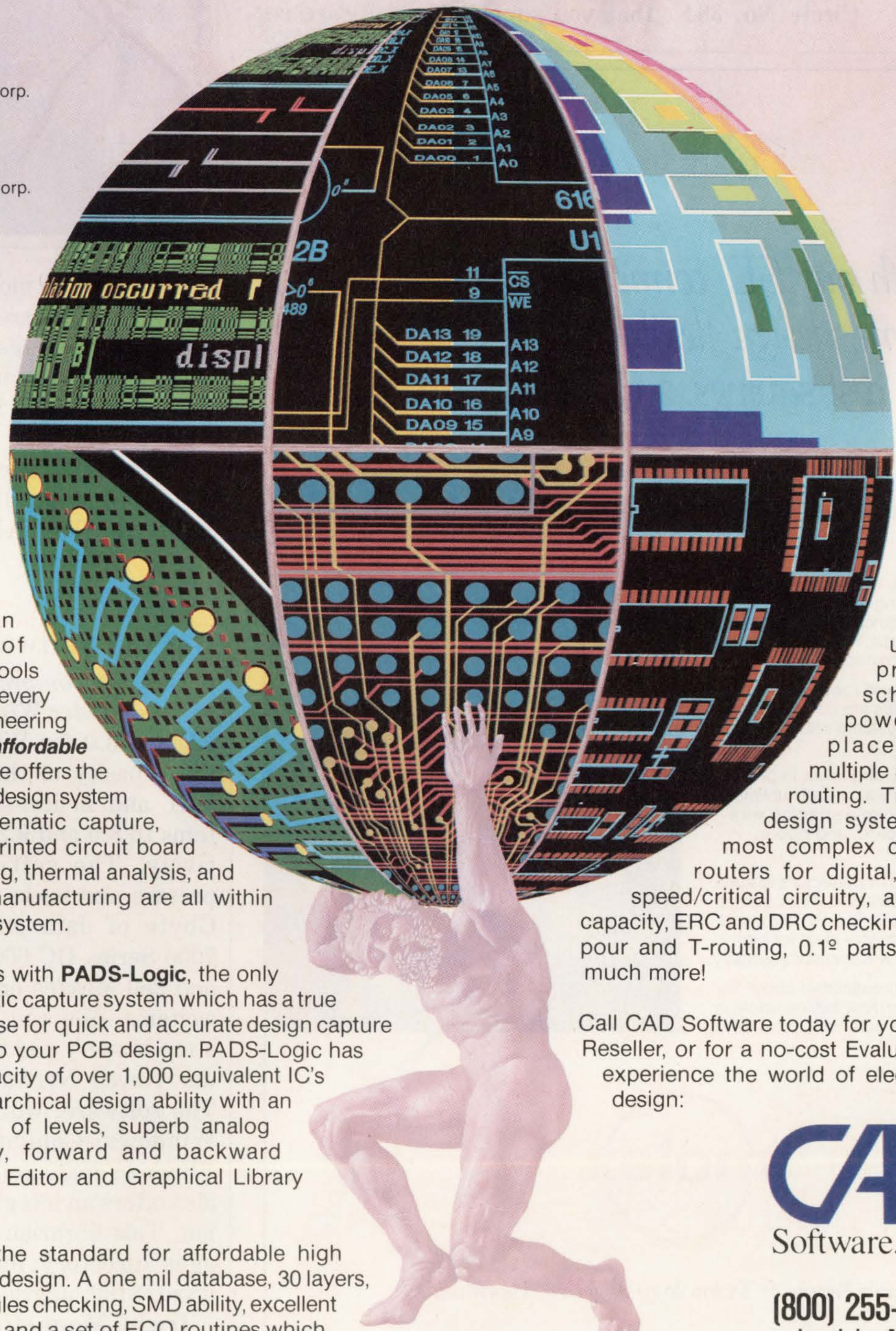

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You asked for an integrated set of CAE/CAD design tools which could deliver every aspect of your engineering design needs ***at an affordable price.*** CAD Software offers the highest performing design system for your PC. Schematic capture, logic simulation, printed circuit board design, auto-routing, thermal analysis, and computer aided manufacturing are all within the PADS Design system.

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CIRCLE NO. 111

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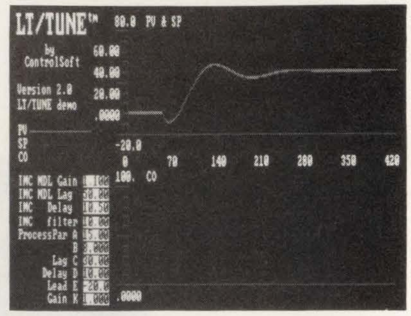
with a spreadsheet, the software allows you to manipulate data in one window before it recalculates all dependent data in other windows. From $895.

DSP Development Corp, 1 Kendall Sq, Cambridge, MA 02139. Phone (617) 577-1133. FAX (617) 577-8211. **Circle No. 364**

Loop-Tuning Software

- *Accommodates as many as 1000 data points*
- *Operates in batch mode*

LT/Tune 2.0 provides for tuning, testing, and simulation of process control loops. Using plant input/output data or model parameters that you supply, the software recommends PI (proportional integral) and PID (proportional, integral, and derivative) settings. The simulator provides both open- and closed-loop responses for combina-



tions of process models and controllers. The software displays model parameter values and measures model prediction error and correlation coefficients. It runs on PCs. $995.

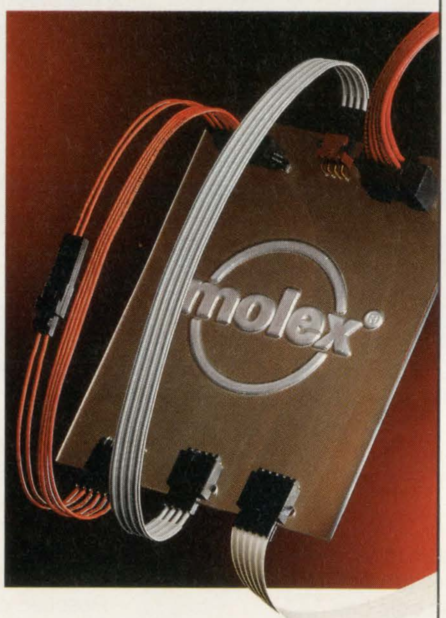
Controlsoft Inc, 4122 Wyncote Rd, Cleveland, OH 44121. Phone (216) 234-5759. FAX (216) 381-5001. **Circle No. 365**

Backup Software

- *Includes compression algorithms*
- *Runs under Windows 3.0*

EZtape 3.0 for Windows increases the capacity of the vendor's 4-mm DAT and helical-scan backup systems to 8.0 and 9.2 Gbytes, respectively. The software also compresses and backs up as much as 1 Gbyte of data onto the vendor's 7000 Series DC 600 data cartridges and 250 Mbytes onto minicartridge systems. You can back up and restore bindery and trustee rights under Novell Netware 2.2 and 3.11. The software, which complies with Windows' Common User Access Windows-management guidelines, also offers an integrated tape librarian. This librarian stores and manages directory information. Software, $169; upgrades, $59.

Irwin Magnetic Systems Inc, 2101 Commonwealth Blvd, Ann Arbor, MI 48105. Phone (313) 930-9000. **Circle No. 366**



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CIRCLE NO. 126

COMPUTERS & PERIPHERALS

Desktop Workstation

- *Has a custom SPARC CPU that delivers 28 MIPS*
- *Contains as much as 128 Mbytes of RAM*

The S4000DX desktop workstation contains a custom SPARC CPU that delivers 28.3 MIPS, 2.3 double-precision Mflops, and 18.3 Specmarks. The workstation also has a 256-kbyte second-level cache that supports the CPU's on-chip 8-kbyte cache. You can install as much as 128 Mbytes of RAM and 1 Gbyte of internal hard-disk-drive memory. Error-correction code protects against single-bit RAM errors. Other standard features include an Ethernet controller, two RS-423A ports, a SCSI-2 port, an audio port, an OS/MP Unix operating system, and a C-language compiler. Sunview, X-Window System, OI Library, PDB debugger, and the company's X-Window Manager are also standard features. Configuration with 19-in. monitor, 16 Mbytes of RAM, and a 200-Mbyte hard-disk drive, $12,495.

Solbourne Computer Inc, 1900 Pike Rd, Longmont, CO 80501. Phone (303) 772-3400. **Circle No. 351**

Laser Printer

- *Has 14 bit-mapped resident fonts*
- *Measures 14.3×15.9×7.7 in. and prints at 4 ppm*

The CI-4 laser printer prints at 4 pages/minute and measures 14.3×15.9×7.7 in. It weighs 28.7 lbs. You can select from 14 bit-mapped resident fonts, including Courier, Courier Bold, Courier Italic, and Line Printer. The printer specifies a 46-dBA sound level during normal operation and 35-dBA in standby mode. It provides HP Laserjet IIP emulation, and it prints at 300 dpi. You load paper by raising a guide-release lever and adjusting the paper guides. The paper bin holds 100

sheets. You can expand the standard 512-kbyte RAM buffer by installing one or two 1-Mbyte memory modules. An optional page-description-language (PDL) cartridge makes the printer Postscript compatible. Laser printer, $1245; 300-sheet paper bin, $175; 1-Mbyte memory module, $230; PDL cartridge, $450.

C-Tech Electronics Inc, Box 19673, Irvine, CA 92713. Phone (714) 833-1165. **Circle No. 352**

Bubble Jet Printer

- *360 dpi on plain bond paper*
- *Character pitch is 10, 12, or 17 cpi*

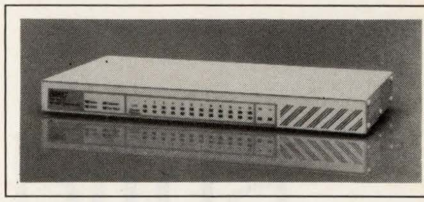
The BJ-10ex bubble-jet printer emulates an Epson LQ-510 and IBM Proprinter X24E printer. It can print with 360-dpi resolution on plain bond paper, envelopes, or transparencies. You can select the following character pitches when printing in high-quality mode—10 cpi (83 cps), 12 cpi (100 cps), or 17 cpi (142 cps). The printer also accepts graphic images from a scanner. You set DIP switches to control such functions as image density, automatic sheet-feeder mode, automatic line feed, page length, character set, emulation mode, and alternate-graphics mode. The printer operates at a noise level of 45 dBA. Printer, $499; 30-sheet paper feeder, $90; print-head and ink-supply cartridge, $25.

Canon USA, Printer Div, 1 Canon Plaza, Lake Success, NY 11042. Phone (516) 488-6700. **Circle No. 353**

Ethernet Concentrators

- *Have 12 10Base-T ports and network management*
- *Dual AUI ports accommodate fiber-optic communication*

These two Ethernet concentrators in the Elite line have 12 10Base-T ports. The 3512TPi concentrator comes with an installed network-management module; using an optional module, you can upgrade the 3512TP concentrator in the field. The module implements the Simple



Network Management Protocol (SNMP). A 16-MHz 80C186 µP provides the intelligence to communicate with SNMP-compliant stations, and you can load the latest protocol firmware over the cable into an on-board 128-kbyte flash PROM. The concentrators also have a fixed attachment-unit-interface (AUI) connector and switch-selectable AUI to BNC connector. Dual AUI ports accommodate fiber-optic communication. Concentrators, $1095; network-management module, $699.

Standard Microsystems Corp, 80 Arkay Dr, Hauppauge, NY 11788. Phone (516) 273-3100. **Circle No. 354**

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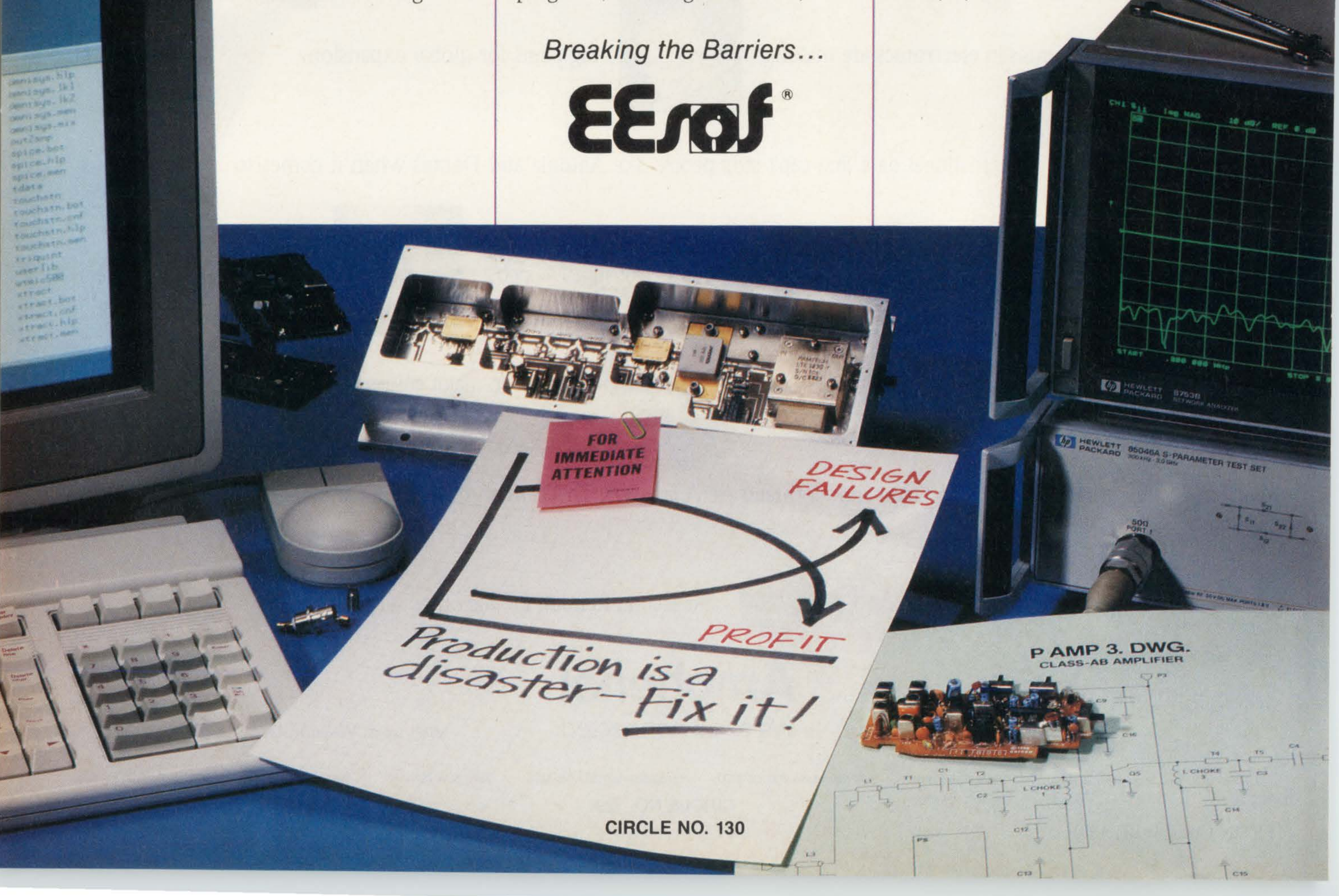
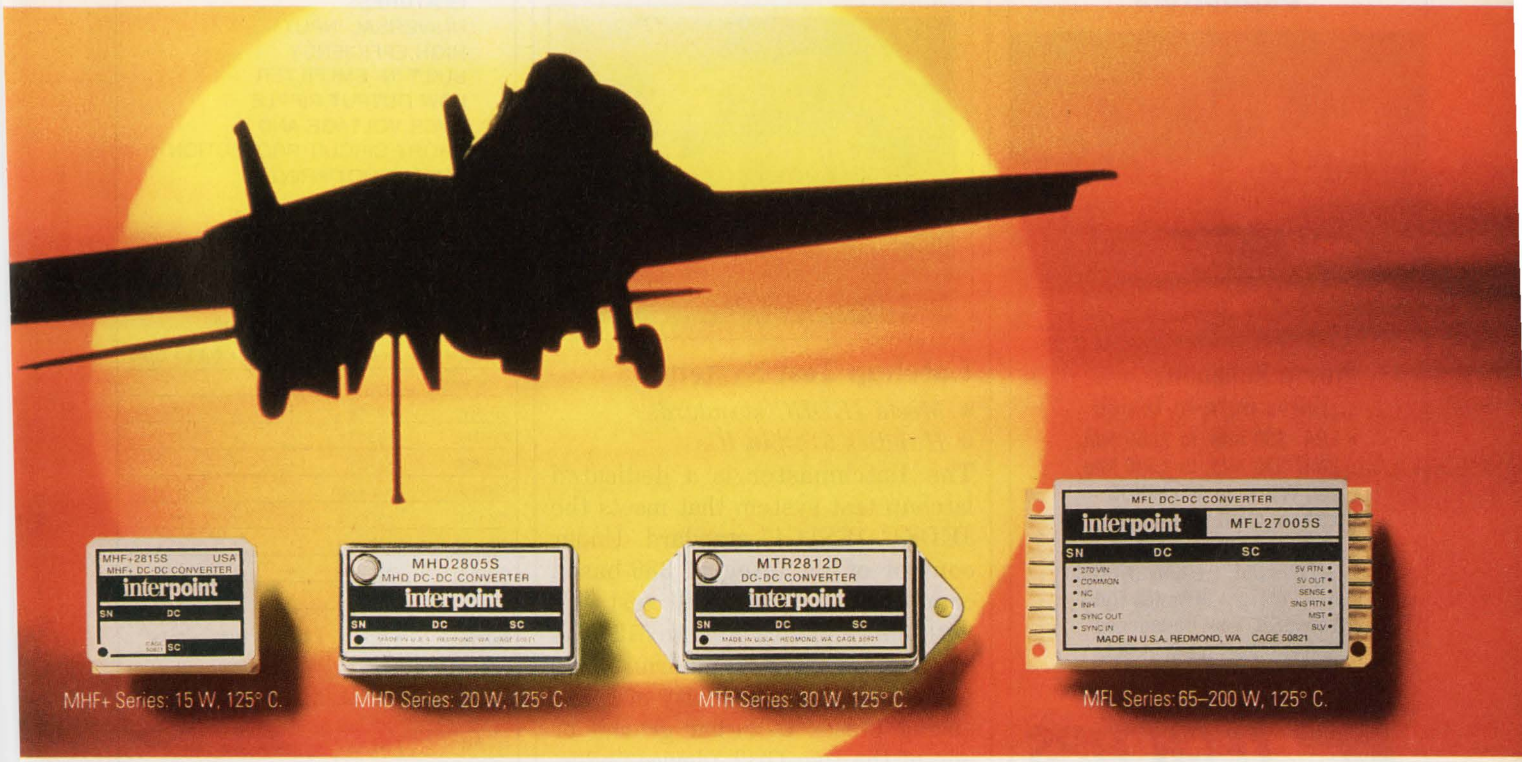


CIRCLE NO. 130

Our newest line of defense against heat.



Insist on Interpoint.

A full line of high-temperature DC-DC converters from the industry leader.

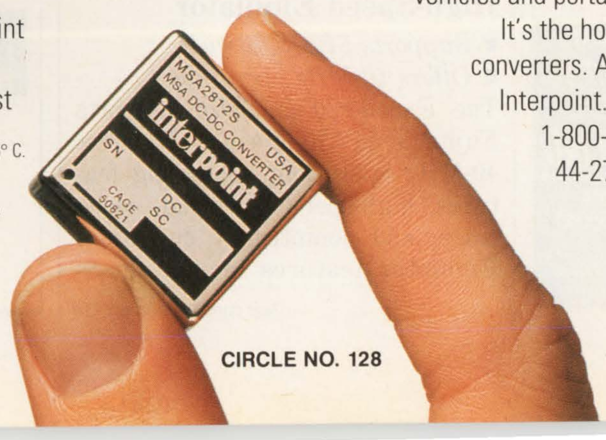
Get the hottest technology in board-mounted power supplies. Full military temperature range. Unsurpassed reliability. The lowest profiles. You can get it all with Interpoint's new line of DC-DC converters.

From arctic blasts to desert storms, Interpoint's new generation DC-DC converters stand up to the toughest military environments. They deliver full power over the entire -55° to +125° C. temperature range. And over an unprecedented power range, too. Interpoint can now offer you an off-the-shelf hybrid power supply for any power level from 2 to 200 watts.

For more than a decade, Interpoint DC-DC converters have proven their reliability in many of the world's most advanced weapons systems — including mission-critical electronics on the Patriot and Tomahawk missiles, the Bradley Fighting Vehicle and F/A-18 aircraft. Our new generation converters are the most reliable yet. Each of them was designed with the specific intent of being qualified to the full performance and reliability standards of MIL-STD-883C.

And Interpoint continues to lead the way in power supply miniaturization. With power densities as high as 40 watts per cubic inch and package heights as low as .270 inch, this new generation of converters is built for the tightly packed boards in today's military and commercial avionics, ground vehicles and portables.

It's the hottest new technology in DC-DC converters. And it's available only from Interpoint. For more information, call 1-800-822-8782. In Europe, 44-276-26832.



MSA Series: 5 W, 125° C.

Interpoint's new line of DC-DC converters features constant PWM switching frequencies from 500 to 700kHz. Built-in sync. Parallel operation. Up to 50 dB audio rejection. Line and load regulation as low as 0.1%. And full MIL-STD-704 input for 28- and 270-volt systems.

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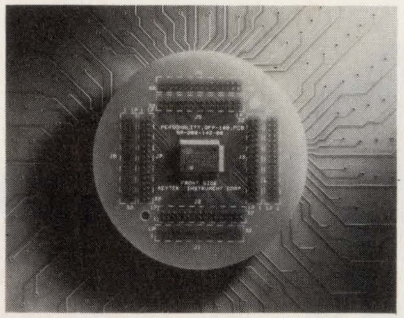
CIRCLE NO. 128

NEW PRODUCTS

INSTRUMENTS



Latchup Test System

- *Meets JEDEC standards*
- *Handles 512-pin ICs*

The Latchmaster is a dedicated latchup test system that meets the JEDEC JESD 17 standard. Under control of an integral 386-based computer, the unit will test ICs with pin counts ranging to 512. The system includes 4-quadrant test pulses with the capability of referencing pulses to either ground or one of the two DUT (device-under-test) power buses. The system also includes fundamental preconditioning to let users define the state of output. Bidirectional pins ensure testing under fully controlled and repeatable conditions. Test-pulse parameters under full software control include pulse voltage amplitude, pulse-current amplitude, rise and fall times, and selection of either logic ground or one of the V_{CC} power supplies as the pulse reference. From $70,000.

Keytek Instrument Corp, 260 Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880. **Circle No. 367**

High-Speed Emulator

- *Supports SPARClite μP*
- *Offers 40-MHz operation*

The Excell-930 emulator supports Fujitsu's SPARClite μP. It offers 40-MHz operation, debugging features, high-speed download, cache trace, and nonintrusive operation. Emulator features include an 8-

Text continued on pg 214

Heard the news about Keithley's new switching system?

It's on all 80 channels.

Introducing the Keithley Model 7001 High-Density Switching System.

Now, get up to 80 channels of two-wire switching from just one half-rack mainframe and two high-density cards.

Monitor all channels at once, too. The unique vacuum fluorescent display shows the open/close status of *all* channels simultaneously. Program, modify, or debug your test systems with remarkable ease.

Plus, have the capability to switch a variety of signals. From femtoamps to amps. Nanovolts to kilovolts. And DC to 500MHz. It's the kind of measurement integrity that has made Keithley switches a preferred choice for nearly two decades.

Call 1-800-348-3735. Or return the card. An applications engineer will provide details, arrange a demonstration, even help you design your test system.

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KEITHLEY INSTRUMENTS

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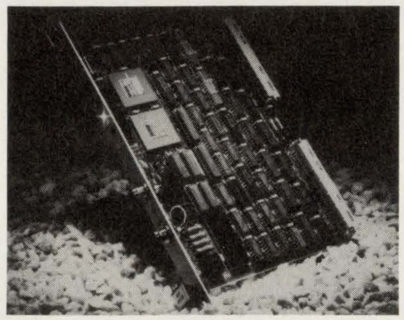
CIRCLE NO. 41

kbyte trace buffer, hardware and software breakpoints, 32 user-defined external inputs, and a logic-analyzer interface. Other features include a Microtec Research Xray source-level-debugger interface, remote debugging from the Sun-4, and a system-expansion bus. $15,875. Delivery, eight weeks ARO.

Step Engineering, Box 3166, Sunnyvale, CA 94088. Phone (408) 733-7837. **Circle No. 368**



VME/VXI Interface

- *Interface to MIL-STD-1553B*
- *Features software controls*

The BUS-65522II provides an interface between the serial MIL-STD-1553B data bus and the parallel VME/VXI bus. Software controls allow the unit to operate as either a 1553B bus controller (BC), remote terminal (RT), or bus monitor (MT). The card has an onboard dual-access RAM, which is double buffered. This prevents partially updated data from being read by the VME/VXI host or transmitted to the 1553B data bus. All MIL-STD-1553 functions are provided without host intervention. The board includes 11 registers that allow the VME/VXI host to configure its operation under software control. The interface supports four groups of vectored interrupts and a custom interrupt, which can be programmed by an onboard PROM interrupt enable/disable. From $4995. Delivery, five to 12 weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 545. **Circle No. 369**

COMPLETE FLASH MEMORY PROGRAMMER IN 1/2 SQ. INCH!

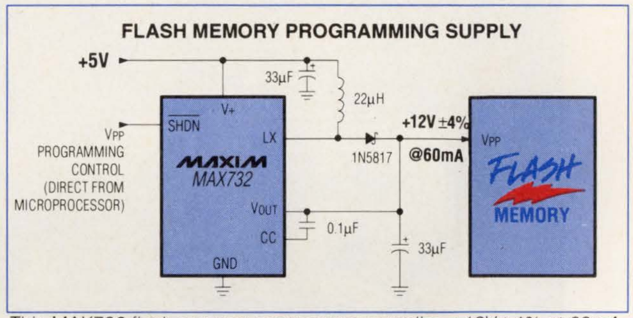
Step-Up From +5V to +12V ±4% at 200mA with 88% Efficiency

The new MAX732 200mA step-up regulator is a simple, compact flash memory programming supply that has direct microprocessor-controlled shutdown.

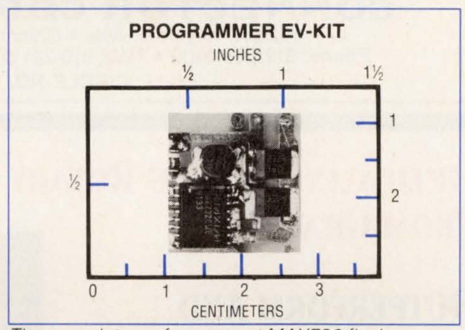
The most basic application needs only four external components and a miniature 22μH inductor to deliver 60mA with 88% efficiency — with a footprint of less than 1/2 in^2 (3.2 cm^2).

To ease design, a pre-assembled surface mount evaluation board is available.*

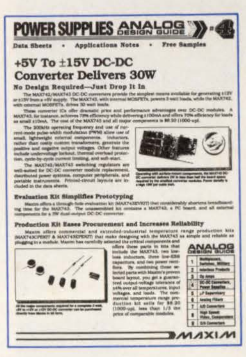
- **Completely Assembled Programmer EV-Kit in Surface Mount**
- **Small 22μH Inductor**
- **Direct Microprocessor Control**
- **Space-Saving Footprints: 16-Pin SOIC and 8-Pin DIP Packages**
- **Pre-Trimmed +12V Output with ±4% Accuracy**
- **Wide Input Range: +4.0V to +9.3V**
- **Guaranteed Output Currents up to 200mA**
- **Low-Noise Operation and Excellent Transient Responses**
- **Short-Circuit and Soft-Start Protection**



This MAX732 flash memory programmer supplies +12V ±4% at 60mA with 88% efficiency from a +5V source. The shutdown current for this entire circuit is 75μA.



The complete surface mount MAX732 flash memory programmer fits into less than 1/2 in^2 (3.2 cm^2). Additional capacitors can be added for higher current operation — up to 200mA.



FREE Power Supply Design Guide

Includes: Application Notes ♦ Data Sheets ♦ Cards For Free Samples

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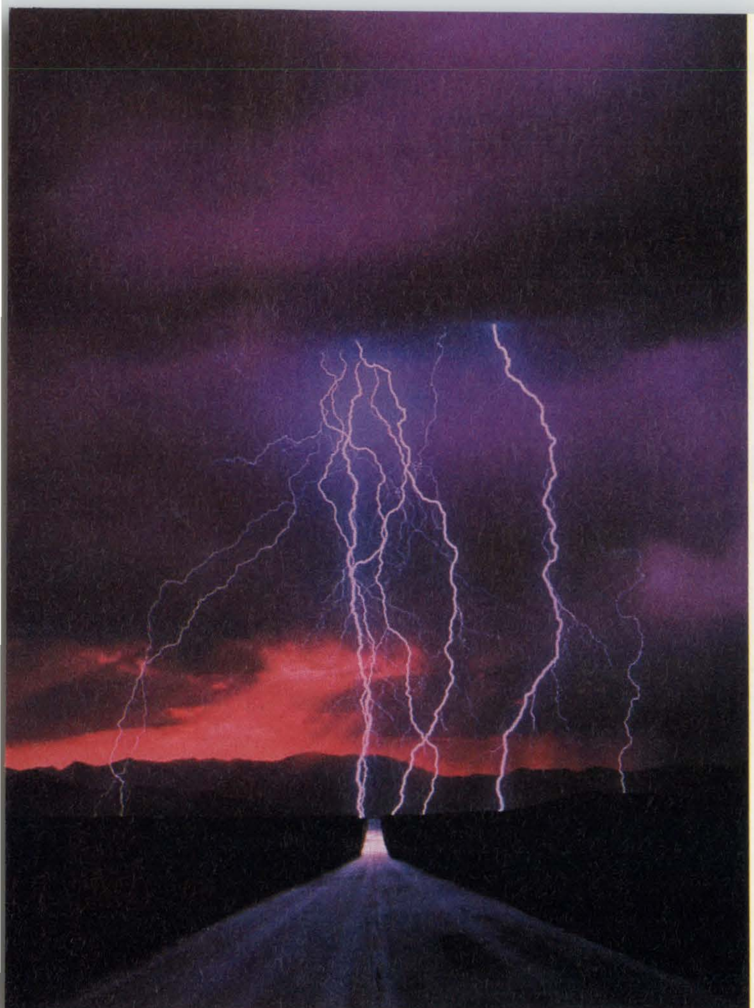
* Order "MAX732EVKIT"

Frequency Synthesizer

- *Covers to 310 MHz*
- *Has 1-Hz resolution*

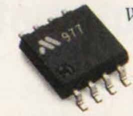
The PTS 310 frequency synthesizer covers a 0.1- to 310-MHz range with a standard resolution of 1 Hz. Resolution to 0.1 Hz is available as an option. Spurious suppression equals 60 or 65 dB, and switching speed ranges from 1 to 20 µsec. The unit is a direct synthesizer, combining direct analog with direct digital technologies. The synthesizer is available in two configurations: a standard model (type 1) and a less expensive version with reduced spurious performance for applications where spurious performance isn't critical. Both models occupy 3.5 in. of rack space. $6000.

Programmed Test Sources Inc, Box 517, Littleton, MA 01460. Phone (508) 486-3008. FAX (508) 486-4495. **Circle No. 370**

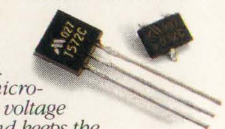


Whatever strikes your microprocessor, you'll be ready.

Mitsumi safeguards more microprocessors than any other company in the world. Not so surprising when you realize that our power guarding ICs are more reliable at half the cost of any others. It's helped us become the number one OEM supplier of quality peripherals over the last 38 years, with more than $1 billion in sales and over 14,000 employees in 27 facilities worldwide, manufacturing more than 100 million IC pieces each year. If you have high volume IC needs, call today, (214) 550-7300, and discover how, with Mitsumi power guarding ICs, you're protected and ready for anything.



WATCHDOG TIMER. Protects microprocessor from external noise and electric current.



SYSTEM RESET IC. Detects microprocessor voltage supply and keeps the microprocessor under control.

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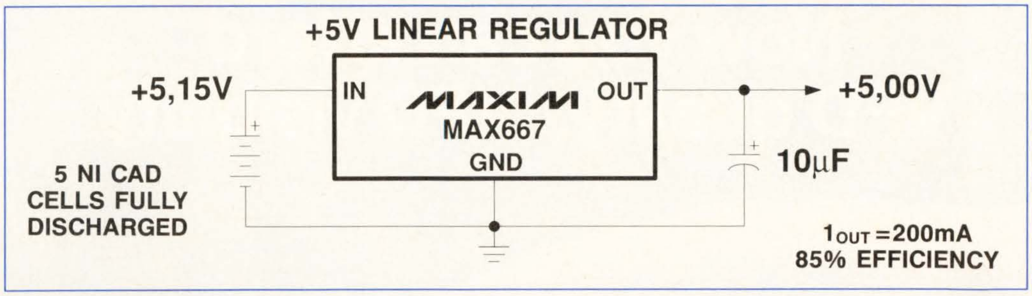

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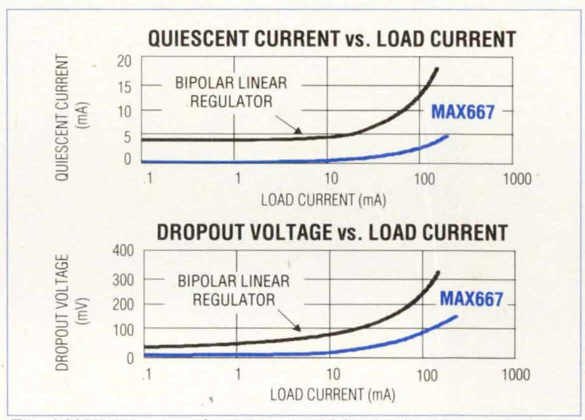

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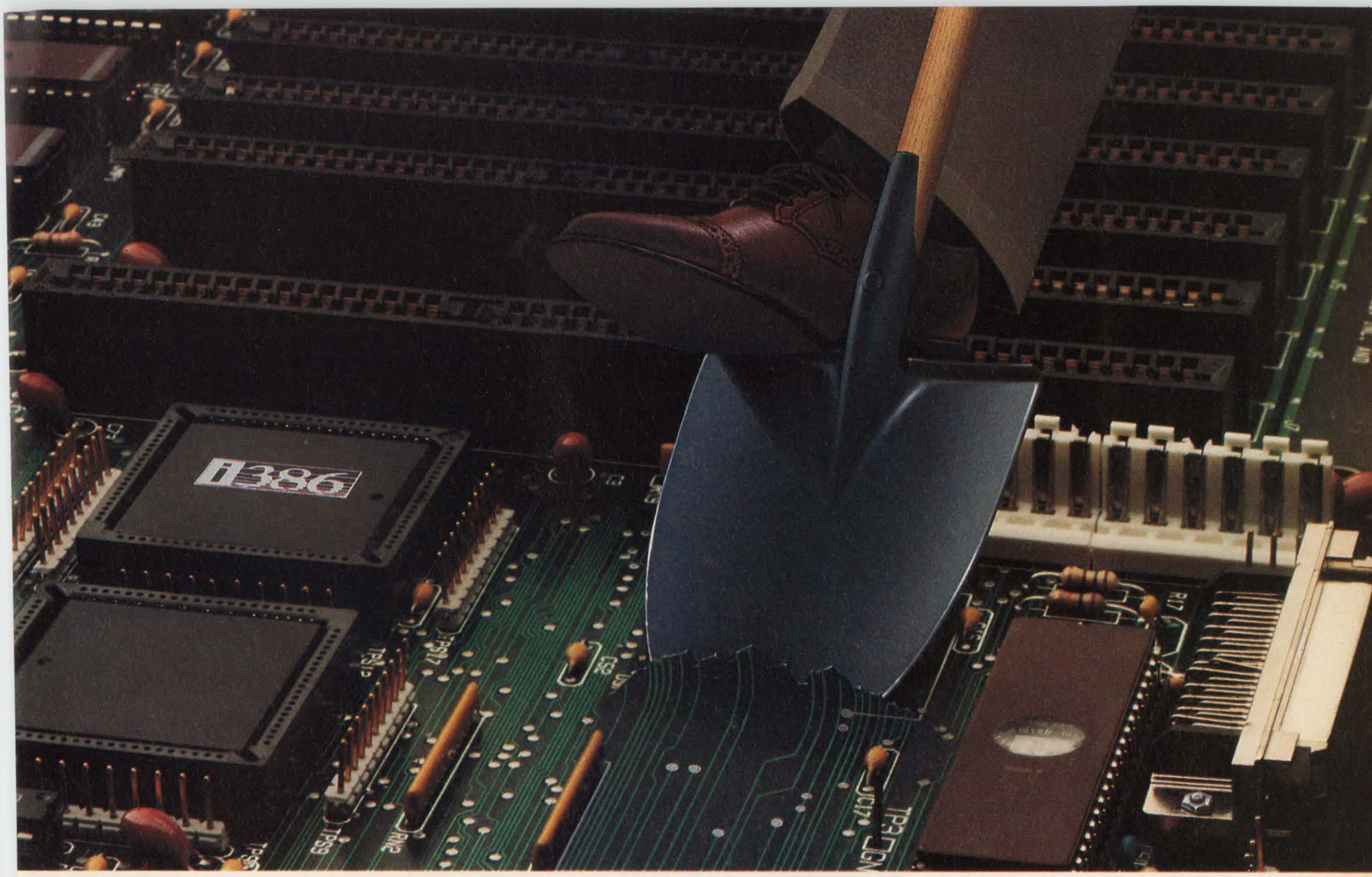

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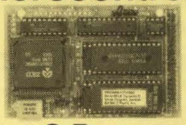

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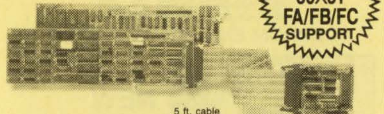

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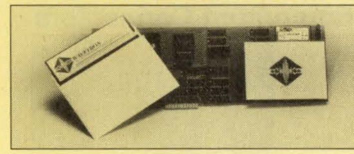

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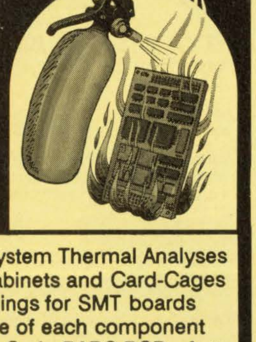

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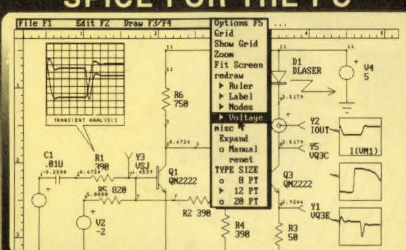

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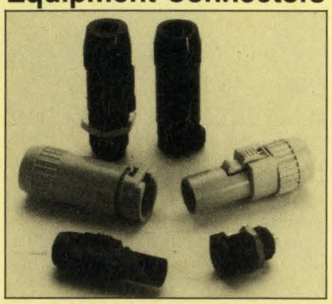

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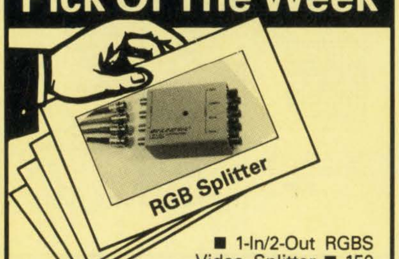

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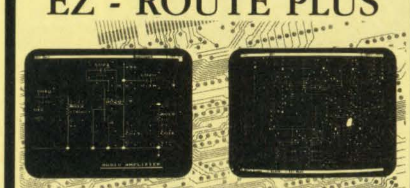

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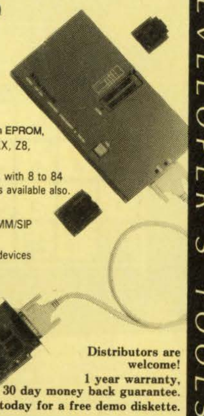

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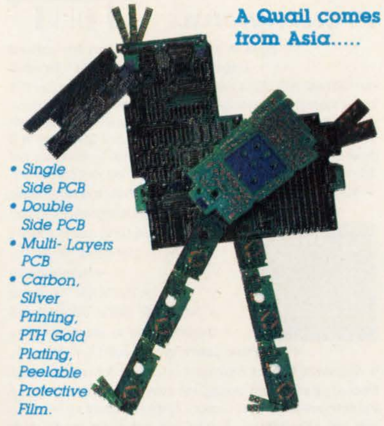

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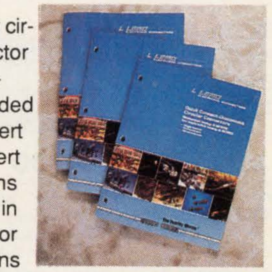

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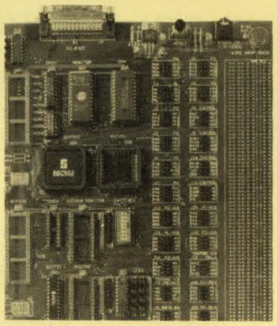

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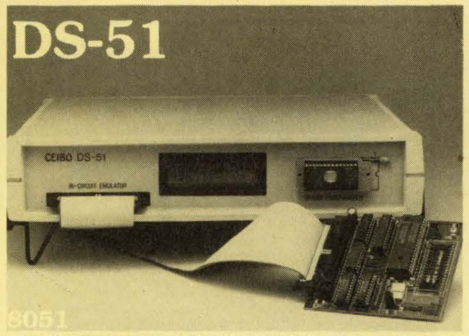

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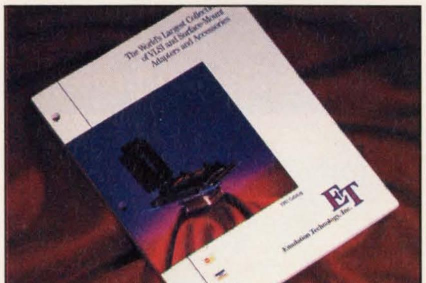

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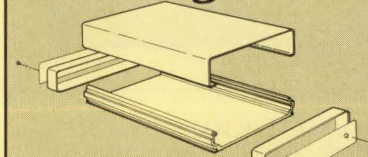

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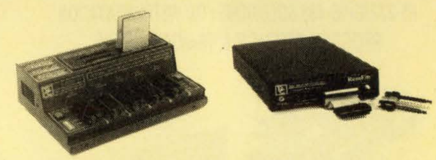

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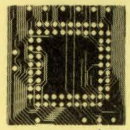

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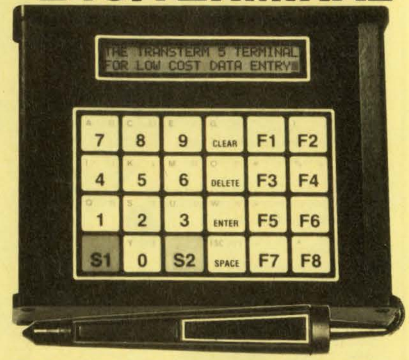

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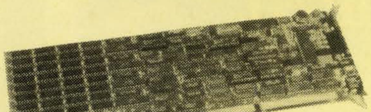

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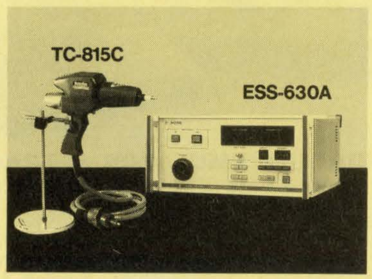

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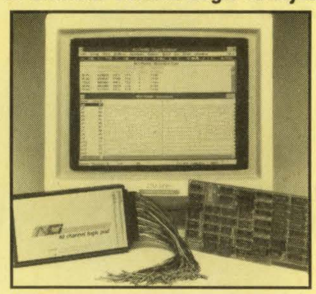

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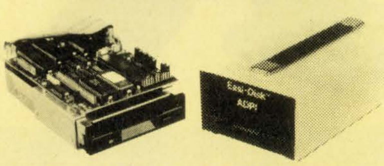

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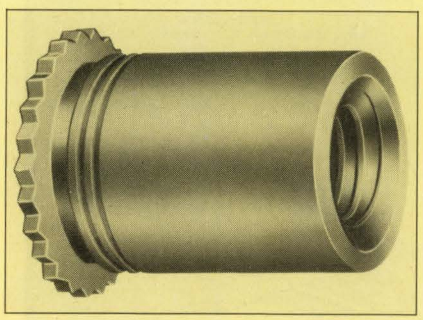

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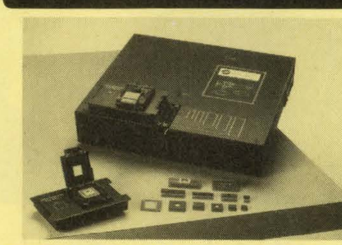

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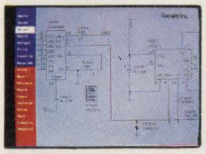

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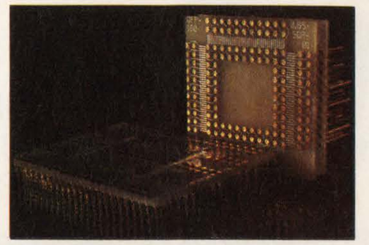

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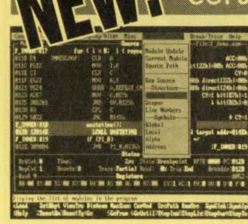

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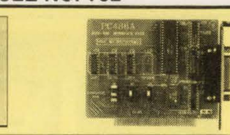

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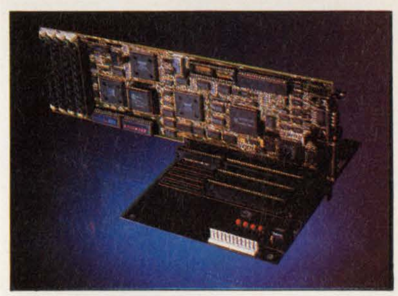

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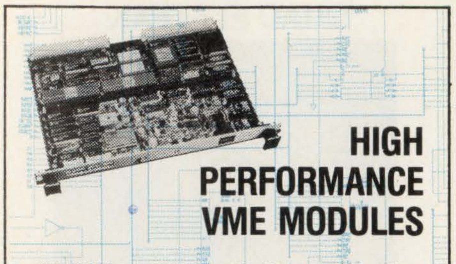

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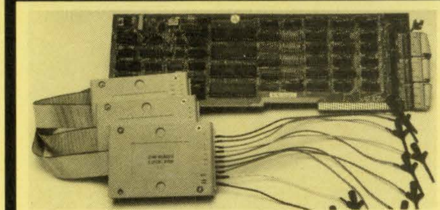

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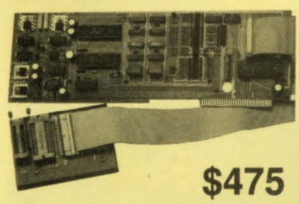

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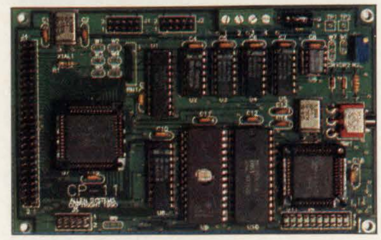

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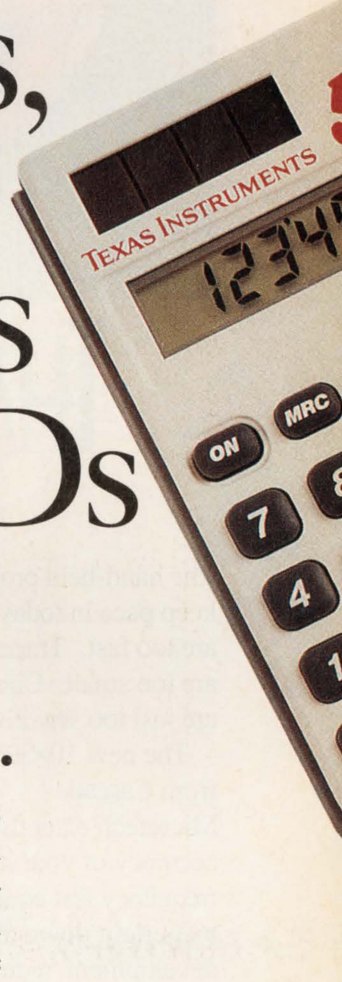

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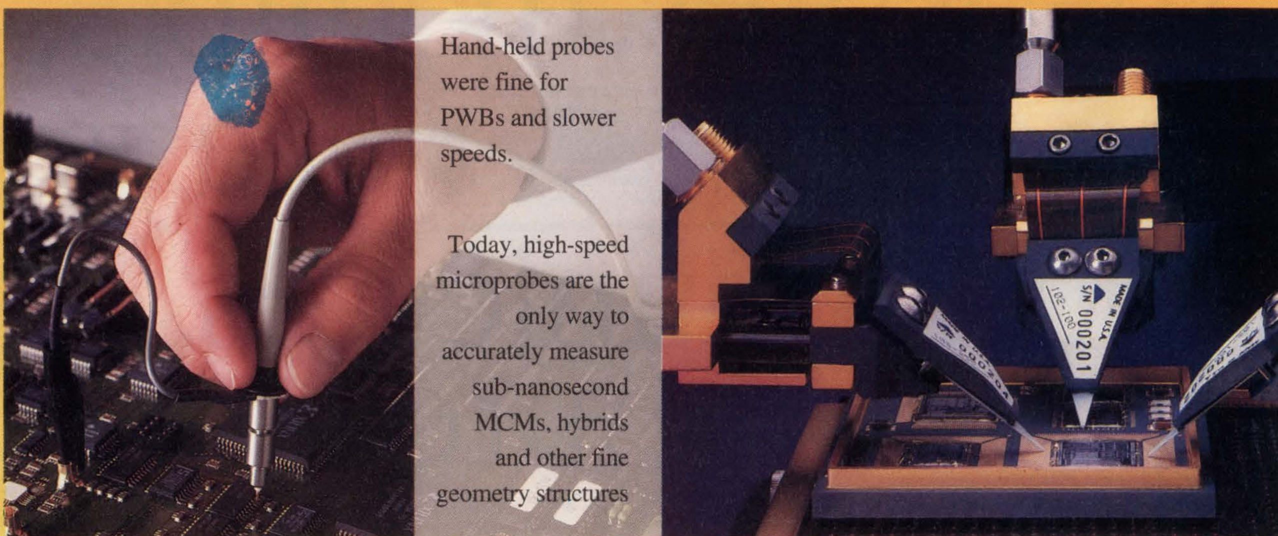

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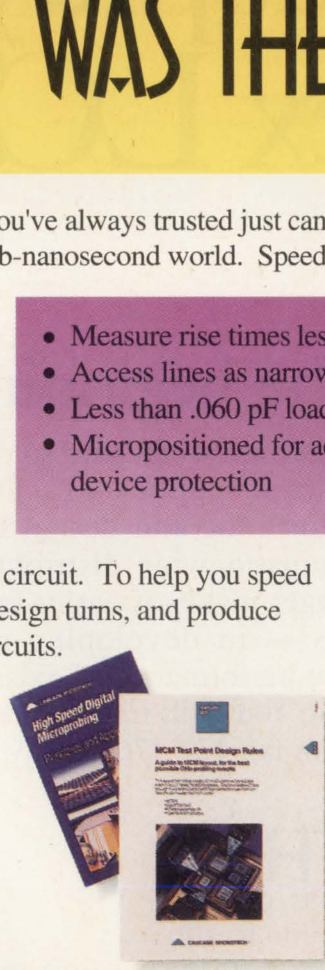

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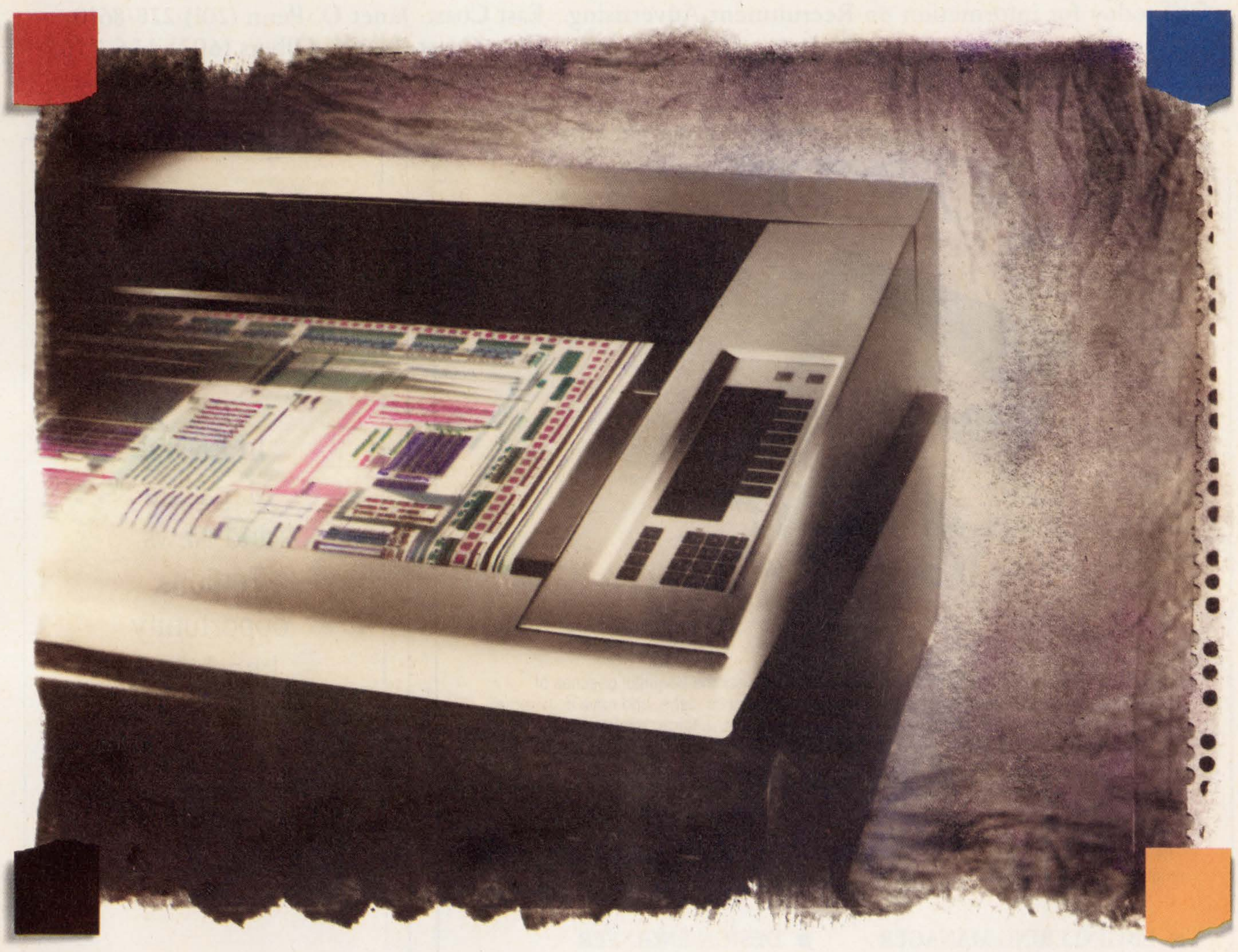

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1991 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	Nov. 21	Oct. 31	18th Annual Microprocessor Directory • Test & Measurement, CAE/ASICs, ICs & Semiconductors
News Edition	Nov. 28	Nov. 8	PC Cards, Board Level**, Regional Profile: Wisconsin, Illinois, Michigan**, EDN's Innovator/Innovation Awards Coverage •

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EMBEDDED COMPUTING INSTITUTE NAVAL WEAPONS CENTER, CHINA LAKE, CALIFORNIA

The Naval Weapons Center invites applications for the position of Director, Embedded Computing Institute. The Institute is being organized to provide research, development, technology insertion, and training in real-time embedded computing systems on board tactical missiles and aircraft. It is a cooperative venture between industry, academy and the Naval Weapons Center. Areas of interest include but are not limited to:

- **Increasing computational density (mips/watt/cu-in/lb)**
- **Shortening system design and implementation time**
- **Modeling and simulation of embedded computer systems**
- **Incorporating new technology into the acquisition process**

The Naval Weapons Center is located at China Lake, California, in the Indian Wells Valley, approximately 150 miles north of Los Angeles. Characterized as high desert, the Indian Wells Valley averages 2500 feet in elevation and lies in the northernmost corner of the Mojave Desert, adjacent to the eastern slopes fo the Sierra Nevada Mountain Range. Comprised of over 5000 employees, and over a million acres of land for both Laboratories and test facilities, this full spectrum center researches, develops and tests tactical air launched systems for the Navy and other services. The city of Ridgecrest is located outside the main gate. Cost of living is moderate, and the surrounding area offers a variety of outdoor activities. The Center intends to fill this position through the Intergovernmental personnel act (IPA). An assignment under the IPA may be made for up to two years and may be extended for up to two more years. Personnel from federal, state, or local government, institutions of higher education, federally funded research centers, and certain other organizations may apply. Applicants should send an SF-171 to K. Berry, Code 226, Naval Weapons Center, China Lake, CA 93555. Questions maybe directed to Ms. Berry at 619-939-2577.

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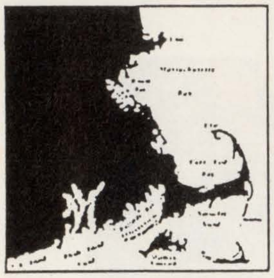

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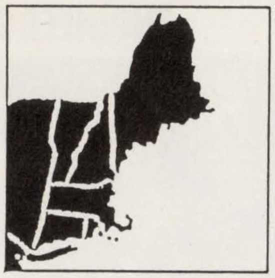

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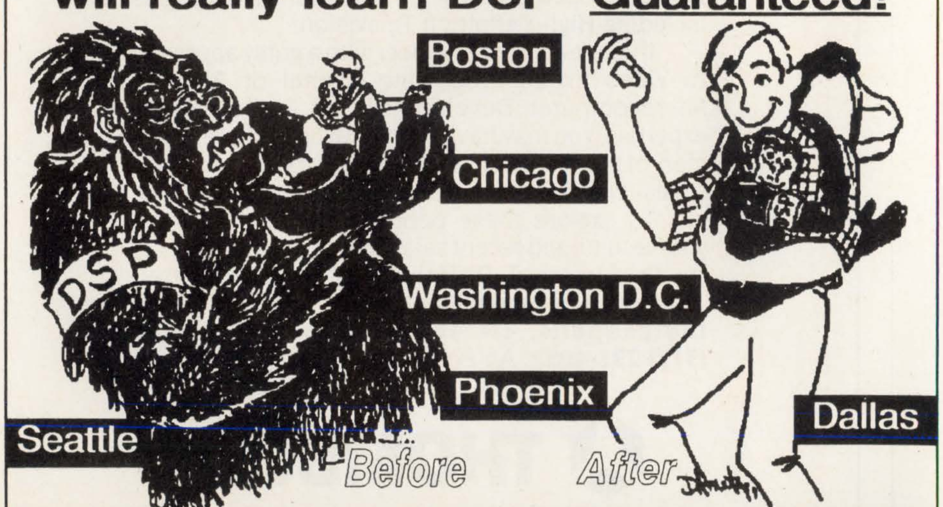

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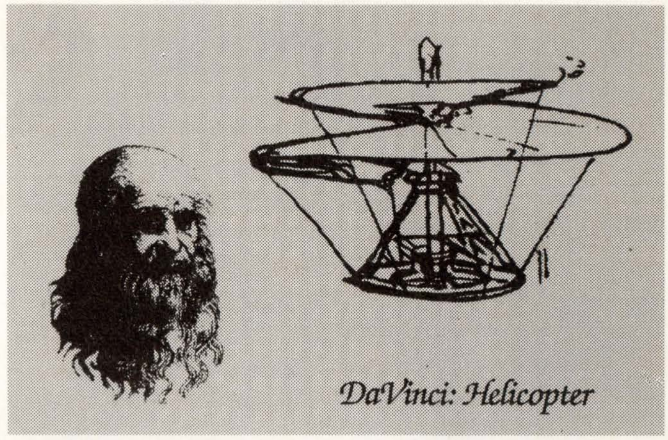
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You will design mixed signal ASIC and standard products using cell-based and semicustom array methodologies. Requires BS/MS in EE and 5+ years of IC design experience with emphasis on high-speed Phase-Locked Loop and/or data conversion circuits. Knowledge of high-speed analog/digital circuit techniques such as high-speed data conversion, clock and data recovery or transmitter and receiver circuits is highly desirable.

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You will develop code for interface program to be internally used by physical design tool, as well as generate command files to run physical design verification. Requires BSEE (MSEE preferred) and 5+ years experience, including solid experience in one of the following: PCs; Sun platform; place and route tools; or verification tools.

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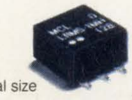

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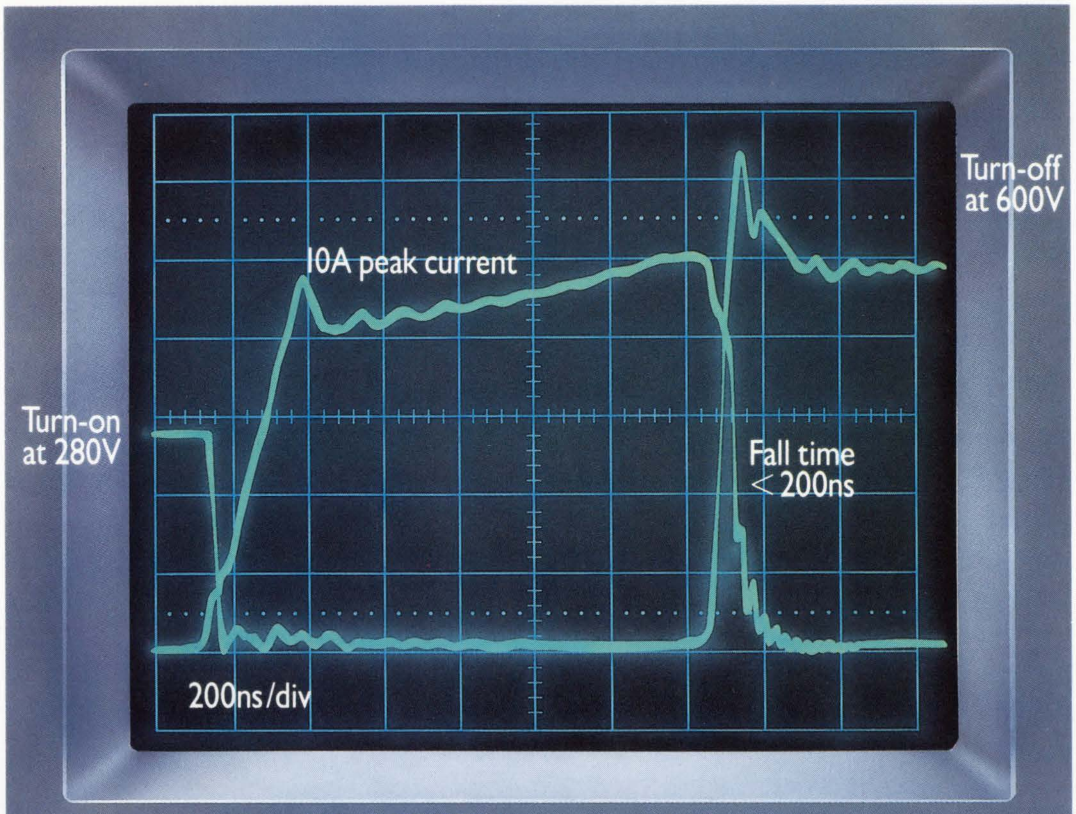

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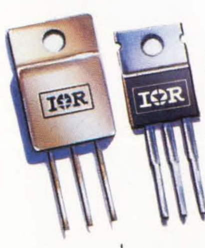

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