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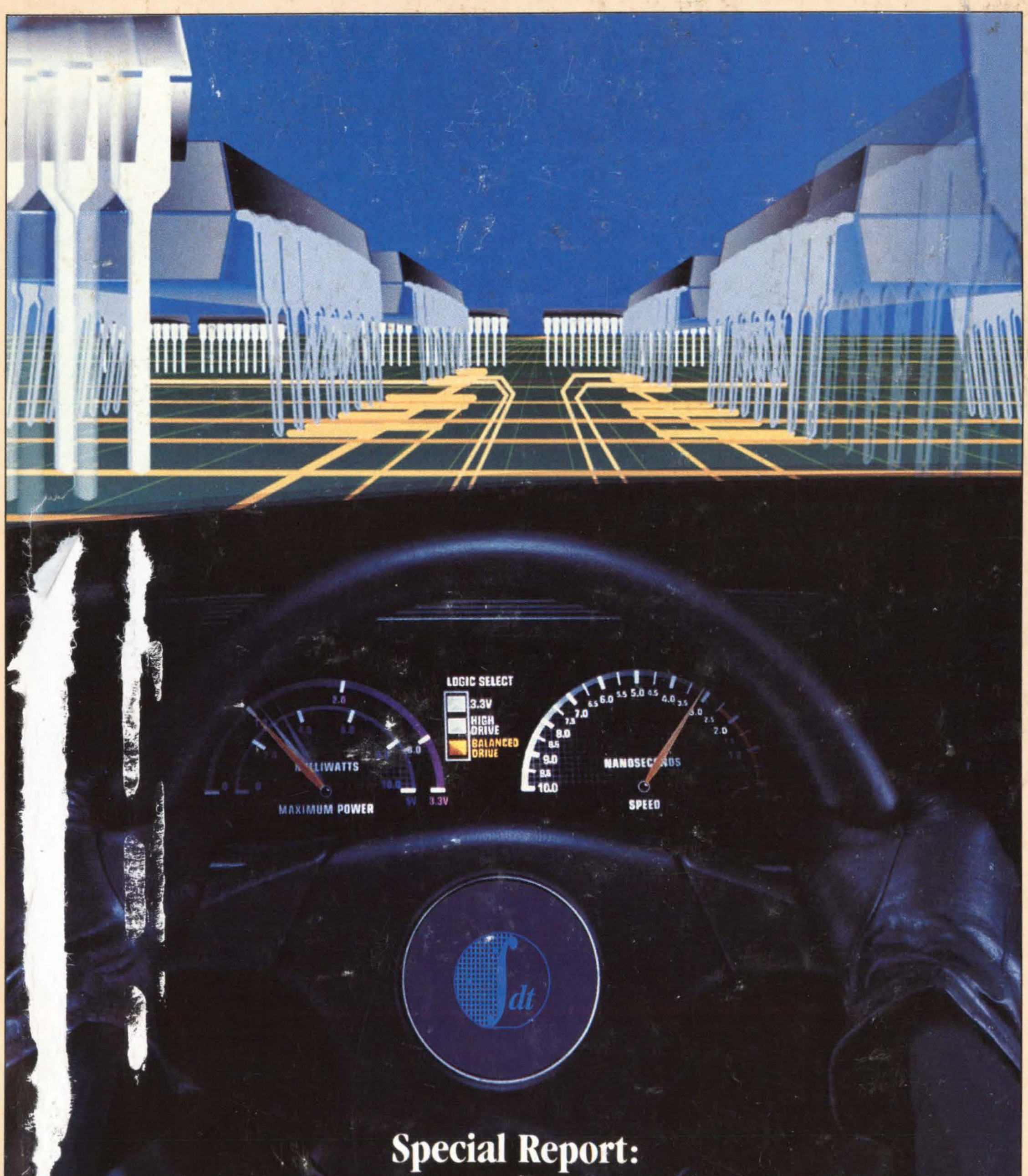
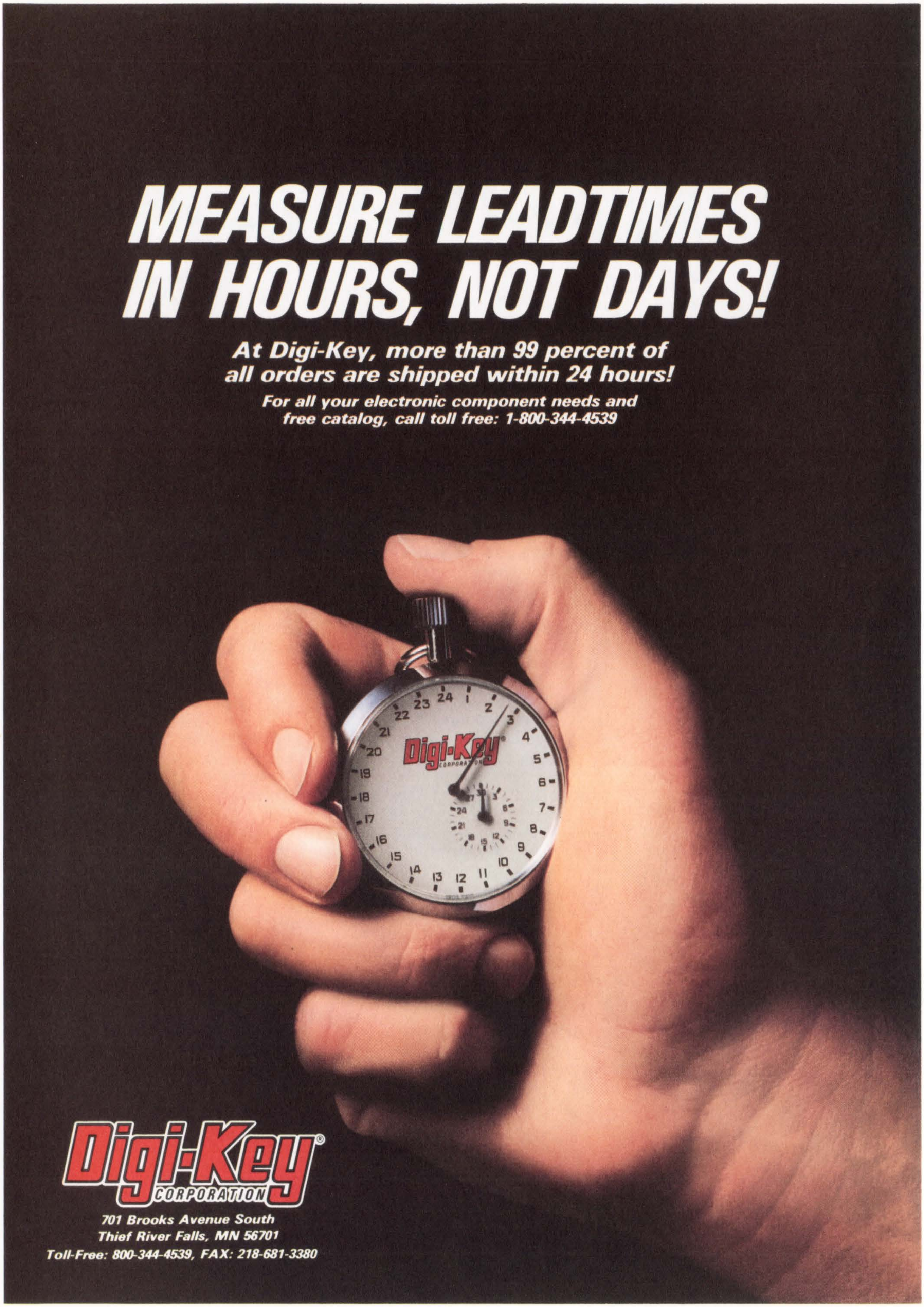
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

A CAHNERS PUBLICATION

February 3, 1992

BBS Update PG 7

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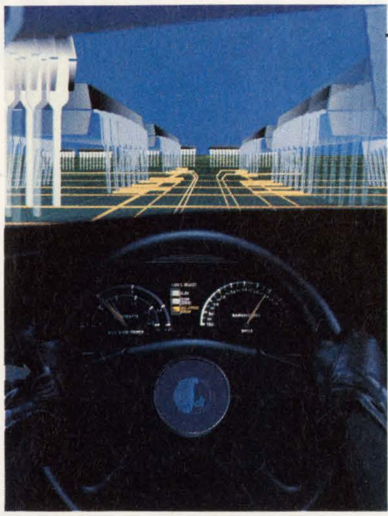
MAGAZINE EDITION

FEBRUARY 3, 1992 VOLUME 37, NUMBER 3

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE



On the cover: Bus-driver manufacturers have successfully maneuvered ground-bounce problems to turn out ICs that are faster, quieter, and have more drive than those previously available. (Photo courtesy Integrated Device Technology)
PAGE 78

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MAGAZINE EDITION

FEBRUARY 3, 1992

Continued from page 5

PRODUCT UPDATES

NEW PRODUCTS

DEPARTMENTS

EDN BBS Update

EDN continues to upgrade the Bulletin Board System (BBS) to make it easier for you to access the information you need, when you need it. The BBS ((617) 558-4241) now has a 220-Mbyte drive, courtesy of Quantum. The additional disk space accommodates 1000 public-domain and shareware postings as well as more than 50 computerized tutorials, covering all popular programming languages and other topics. The BBS also features an expanded FORTH section and a free 32-bit 80386/486 compiler for use on IBM PCs. You can access the expanded scientific-calculator program library on the /sci_calc Special Interest Group or the new math-software library on the /math Special Interest Group. Stay tuned for more.

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A summary and analysis of articles in this issue.

Just a year or two ago, it seemed that the notorious ground-bounce problem threatened to overcome further advances in bus speeds. However, as Technical Editor Richard A Quinnell discovered while researching bus drivers for this issue's cover story, IC vendors have effectively kicked ground bounce off of the bus. At the same time, vendors are enhancing bus drivers by adding logic, such as internal latches, test logic, and power-up-disable circuits, which permits boards using these drivers to be inserted into live systems.

If you're looking for more creative ways to use bus drivers, software, and other components in your designs, take a look at Senior Technical Editor Charles H Small's unusual article on innovation software. He reviews several products that help you use guided problem solving and brainstorming to overcome mental blocks. He also takes a look at the dark side of creative design, reviewing stress-management software and programs for overcoming depression. Small's venture into the untrodden territory of self-help software may seem unusual for a design publication like EDN, but such topics are interwoven into the design engineering occupation as into any other.

Also in this issue, you'll find the second part of Technical Editor Ray Weiss' review of μC evaluation boards. This time, Weiss looks at boards for the 16 bitters. As in the first part, he explains how these products can help you pick the right processor and get up to speed quickly.

Steven H Leibson,
Executive Editor

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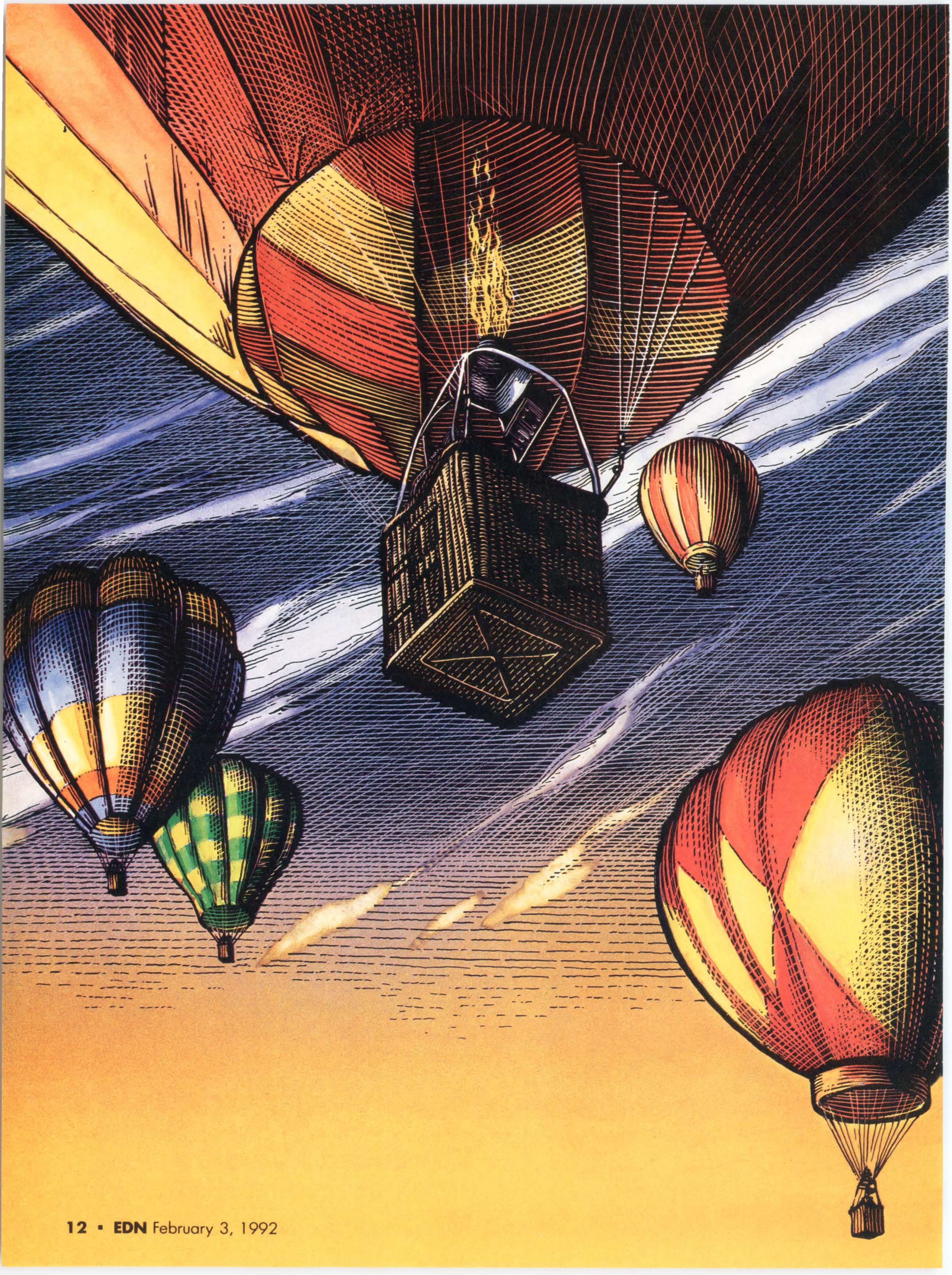

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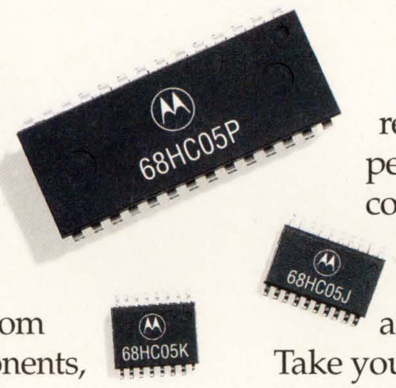

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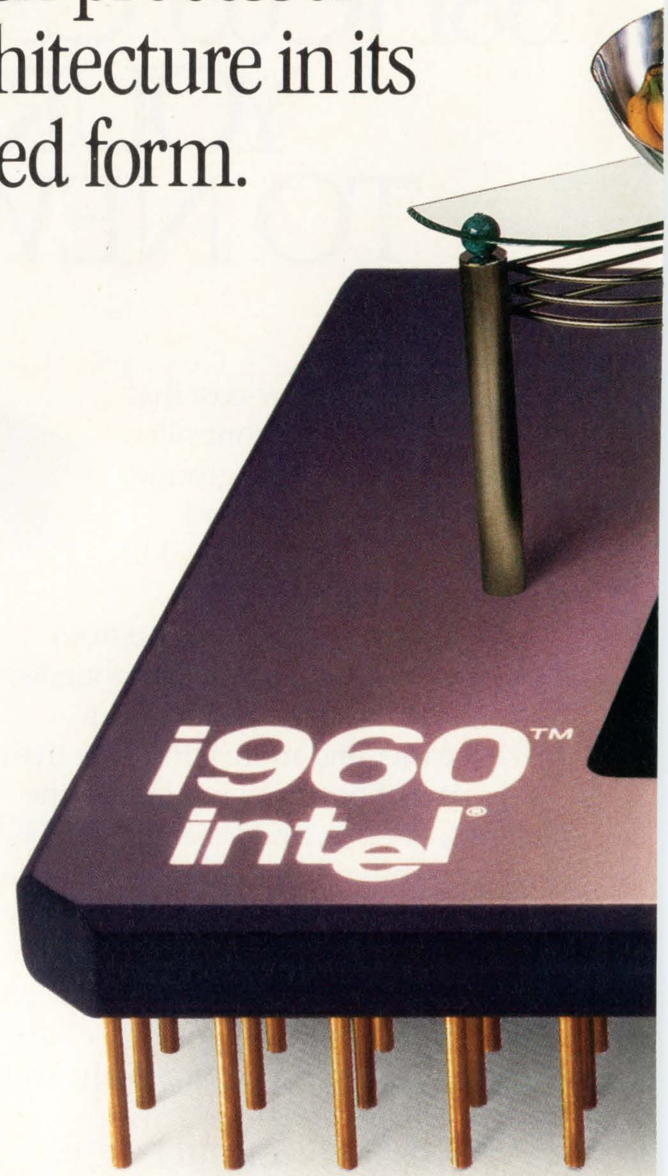

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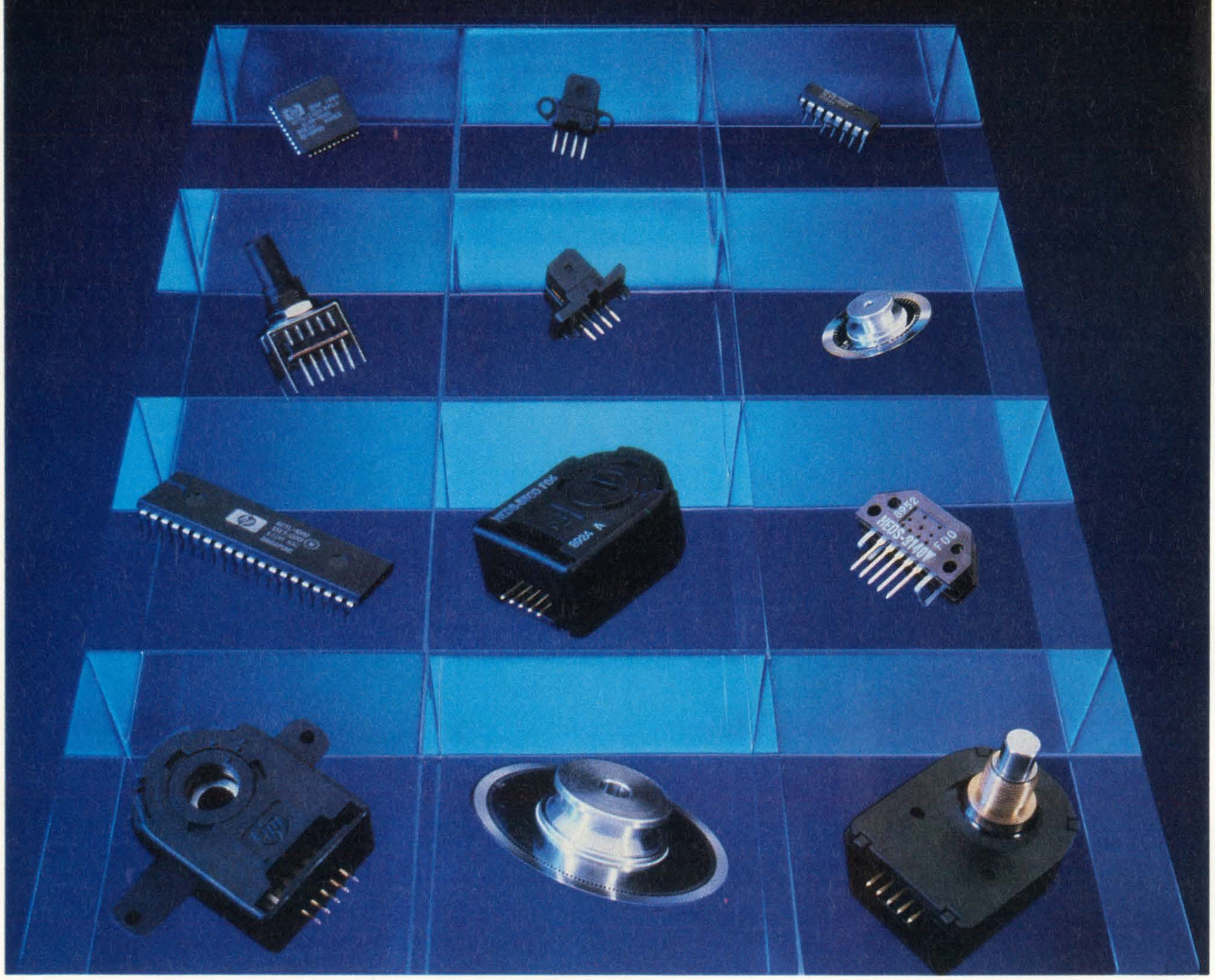

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Graphics IC quintuples Windows performance

Graphics performance has been one of the key limitations of the Microsoft Windows environment for PCs. Existing graphics-coprocessor boards provide the necessary performance boost but at a price that relatively few people are willing to pay. The OTI-087 super VGA controller IC offers a less expensive way for system designers to solve this problem. The $31 (1000) chip boosts the display speed of Windows by a claimed factor of five through a high-speed bus interface and hard-wired graphics functions. In addition, the device supports 1280×768-pixel noninterlaced and 1280×1024-pixel interlaced displays, both with 256 colors. It can also control 24-bit display memories for full-color applications with a 640×480-pixel resolution.

The IC's bus interface is designed to couple closely to the host processor bus and operates at speeds to 40 MHz. Most VGA controllers interface to a PC's 8- or 16-bit expansion bus operating at 8 or 10 MHz. The chip also incorporates a write cache memory to further speed bus transactions, a read cache memory for zero-wait-state bitblt (bit-block-transfer) operations, and a 64×64-pixel hardware cursor with 2 bits/pixel.

Systems based on this controller can immediately take advantage of the higher bus speed. To make use of the hard-wired graphics functions, you must add software drivers. The company plans to offer drivers for Microsoft Windows in February and an evaluation board in March. Oak Technology Inc, Sunnyvale, CA, (408) 737-0888, FAX (408) 737-3838.
—Steven H Leibson

Test-method availability to exceed 50%

With the addition of NEC Corp as a licensee for its embedded test matrix, Crosscheck Technology's approach to testability soon will be available on ASICs from vendors who collectively deliver more than half of the world's CMOS gate arrays. The license grants NEC the right to include Crosscheck's on-chip test electronics in a variety of semiconductors and to use Crosscheck's fault simulation, test-pattern generation, and device diagnostics software. A by-product of the test electronics is high observability of internal nodes. This observability ensures fault coverage exceeding 98% and reduces test-pattern, test-development, and device-debug times.
—Michael Markowitz

Windows-based data-acquistion software standards posed

With the announcement of open standards for applications- and systems-programming interfaces, collectively named DT-Open Layers for MS-Windows, Data Translation Inc has addressed problems that have plagued PC-based data acquisition since its inception: lack of a standard interface between applications programs and commonly used functions, and lack of standards for interfacing hardware to software.

MS-Windows, with its provision for dynamic-link libraries (DLLs), handles communications among applications programs, function libraries, drivers, and standard I/O devices. Because of its broad acceptance, MS-Windows has become the environment of choice for new PC-based real-time software. By using function libraries and drivers that conform to the new programming interface standards, software engineers and even end users will, without rewriting or recompiling their applications code, be able to use new hardware and extend the functional capabilities of their software.

Actually, the new standards apply to a field wider than data acquisition. The company has made image-processing boards for several years; the new standards apply to such boards. The standards also apply to hardware accelerators such as DSP boards. Indeed, there is nothing in the standards that limits their applicability to boards that plug into the ISA and EISA buses.

Data Translation is now distributing copies of the standards free of charge. It is also shipping 1.0 versions of the data-acquisition and signal-processing libraries for its $1495 Global Lab Data Acquisition and $1995 Global Lab Image applications software. The data acquisition library is free with a purchase of the firm's data-acquisition hardware ($95 without such a purchase). The image library costs $1995. Users of Global Lab V2.1, which does not support Windows, will receive a $500 credit when they upgrade to the MS-Windows-compliant version.

Three firms are announcing their support of the new hardware hardware programming interfaces: Ariel Corp, IOtech, and Optivision. Data Translation Inc, Marlborough, MA, (508) 481-3700, FAX (508) 481-8620.—Dan Strassberg

Interconnect succumbs to software programmability

Although ASIC designers have been able to reprogram the connections between gates for several years, system designers haven't had the same flexibility with their building blocks. An interconnect technology from Aptix Corp provides the ability to change, via software, the connections among board-level components.

The capability, like a huge digital crosspoint switch, lets you connect any input to any output or outputs. The device is packaged in a proprietary 1024-pin land-grid array—a multilayer ceramic package. The architecture, FPIC (field-programmable interconnect components), is being developed in two components; static RAM-based reprogrammable andone-time-programmable versions. Typical pin-to-pin delays are less than 10 nsec. The technology will be commercially available in the second quarter of this year. Aptix Corp, San Jose, CA, (408) 428-6200. —Michael Markowitz

Busless single-board computer is still flexible

RLC Enterprises' SBXC-186EB offers the simplicity of a single-board computer without the expense of a card cage and backplane for embedded applications. What gives the board flexibility are four SBX expansion connectors that let you add special functions to the card with industry-standard SBX modules. Hundreds of SBX cards from multiple manufacturers offer a variety of functions, including A/D and D/A conversion and speech synthesis. The SBX cards also have video controllers, LAN controllers, and SCSI adapters. The single-board computer is built around the Intel 80C186EB 16-bit CPU and the 80C187 coprocessor running at speeds as high as 16 MHz. The computer supports as much as 512 kbytes of battery-backed static RAM and 512 kbytes of EPROM or flash memory. The board provides a 32-bit parallel I/O port, a real-time clock, watchdog reset, and two communications ports that support RS-232C, RS-422, and RS-485 drivers. An 8-MHz board without the math coprocessor costs \$319 (100). RLC Enterprises, Atascadero, CA, (805) 466-9717, FAX (805) 466-9736.—Doug Conner

QIC Technical Committee Adopts New Standards

The Quarter-Inch Cartridge (QIC) technical committee recently adopted recording format standards for 385- and 410-Mbyte minicartridges. In addition, the committee defined standards for the magnetic heads in each device. The standards permit vendors to create QIC drives that have more capacity than QIC-40 and QIC-80 3½-in. drives.

QIC Drive Standards Inc is an international trade association. The group provides a forum for identifying and evaluating user needs and for technical discussions leading to the adoption of standards. The QIC technical committee comprises 10 member companies and 34 associate companies. The members are Archive Corp, Costa Mesa, CA; Carlisle Memory Products Group Inc, Bedford, TX; Colorado Memory Systems Inc, Loveland, CO; Gigatek Memory Systems, La Costa, CA; Summit Memory Systems Inc, Scotts Valley, CA; Sony Corp, Park Ridge, NJ; Tandberk Data Inc, Oslo, Norway; Teac Corp, Tokyo, Japan; 3M, St Paul, MN; and Wangtek Inc, Simi Valley, CA. QIC Drive Standards Inc, Santa Barbara, CA, (714) 497-8138, contact Tony Miller. —John Gallant

US firm continues emphasis on memory-IC testers

Even though most of the ICs the systems test come from Japan and Korea, memory testers don't have to be products of the Orient. A US firm willing to devote significant resources to developing memory-test systems can sell its products to the Asian firms that dominate the memory field. So goes the thinking at Teradyne Inc's Semiconductor Test Div. The firm feels that existing testers from either side of the Pacific won't test the new generations of memory chips as economically as necessary. And, the shift toward using application-specific chips demands testers that can readily adapt to testing many more device types than earlier testers could.

To overcome these problems, the J997, optimized for use in engineering and for wafer probing, runs at speeds to 200 MHz and exhibits an overall timing inaccuracy of 300 psec. It can test as many as 32 devices in parallel on two test stations. The corresponding specs for the J994, a model optimized for final test of packaged ICs, are 120 MHz, 500 psec, and 64 devices. Both models accommodate devices that store as much as 1 Gbit each. Pricing begins at \$1 million. Teradyne Inc, Semiconductor Test Div, Agoura Hills, CA, (818) 991-2900, FAX (818) 707-2805.—Dan Strassberg

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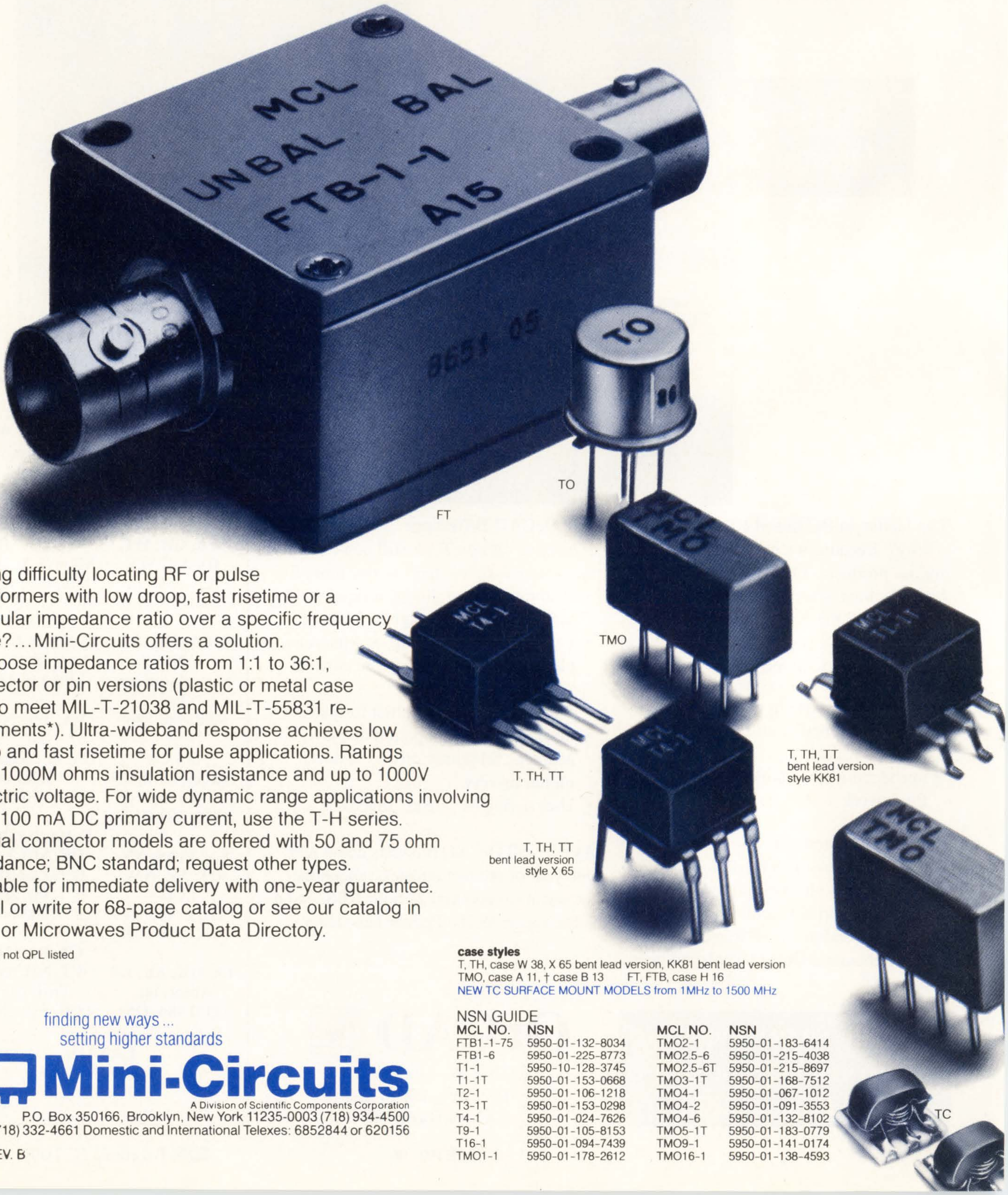

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FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
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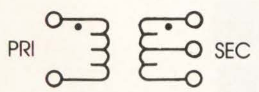

	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
	T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
	T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
	T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
	T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
	T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
	T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
	T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
	T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
	T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
	T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
	TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
	†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
	†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
	TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
	TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
	TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45

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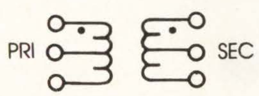

	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
	TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
	TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
	TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
	TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
	TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
	TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
	TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95

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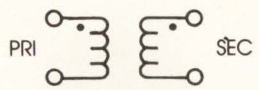

	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
	T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
	T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
	T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
	T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
	T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
	T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
	T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
	T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
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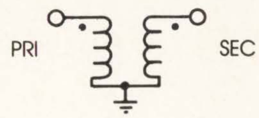
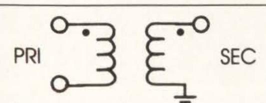
TO	TO-75	1	10-500	—	10-500	40-250	6.95
TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
	T9-1H	9	2-90	2-90	3-75	6-50	6.45
	T16-H	16	7-85	7-85	10-65	15-40	6.45
TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
	TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
	TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
	†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
	†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
	TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
	TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
	TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95

D



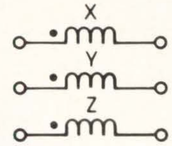
	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
	T3-1	3	.5-800	.5-800	2-400	—	4.45
	T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
	T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
	T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
	TMO3-1	3	.5-800	.5-800	2-400	—	8.45
	TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
	TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
	TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
	FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95

E

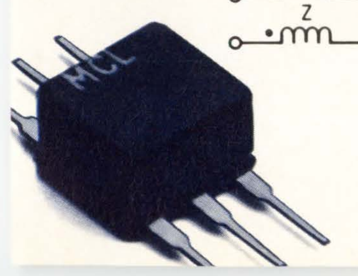


	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
	FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
	■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95

F



	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
	T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

* FOR A AND B CONFIGURATIONS

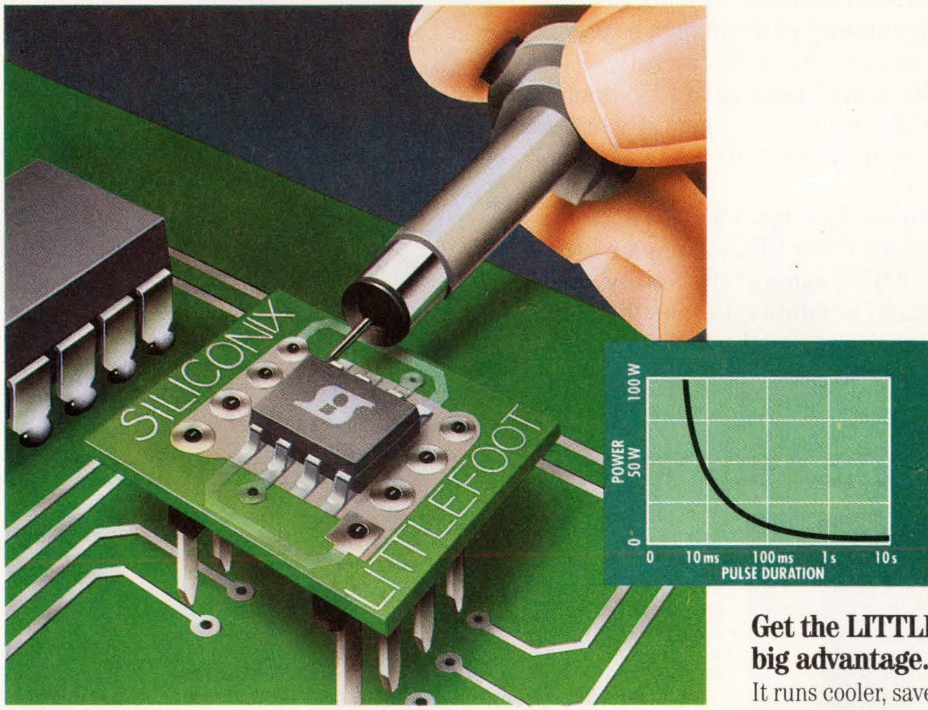
Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range

CIRCLE NO. 58

C72-2 REV. B

"SIZE IS POWER" DEBUNKING THE MYTH



The myth of mass.

Many say, "Size is power." We say different, but understand a few of you may have doubts. Sometimes it's just hard to believe a device so small can dissipate so much power. A full 2 watts.

But LITTLE FOOT™ does.

It also delivers the highest current rating available, up to 3.5 amps, in a tiny SOIC-8 package. This results from a combination of our unique copper lead-frame design that conducts heat directly from the backside of the die to optimize thermal performance, and our SiMOS 2.5 (2.5 million cells/sq.in.) technology that creates the industry's highest power density and lowest on-resistance. Just what you need for motor control, load switching, and DC/DC conversion in applications where space and heat are critical constraints.

How else can you design one or two powerful MOSFETs into your system in less than five one hundredths (0.05) of a single square inch?

Use the world's smallest evaluation board... and see for yourself.

Siliconix simplifies circuit testing by providing you with a mini-evaluation board. It's only ½" x ½". Just solder LITTLE FOOT to the mini-board and drop it into your socket. It takes only a few minutes to prove to yourself that 2 watts can be dissipated easily by this remarkable SOIC-8 packaging technology.

LITTLE FOOT is designed for manufacturability.

LITTLE FOOT simplifies your assembly process because Siliconix's SOIC packaging is compatible with the digital devices on your board. And its two-MOSFET capability means you use fewer components and get higher system reliability.

LITTLE FOOT cuts your costs and reduces set-up time. And there are no solder voids, no lead trimming, and no tube jamming. It can also eliminate steps in your production cycle to get your product to market faster.

Get the LITTLE FOOT big advantage.

It runs cooler, saves space, improves reliability, increases efficiency, simplifies design, extends battery life, reduces costs, and cuts time to market. With this kind of designed-in performance it's not surprising that LITTLE FOOT sales have surpassed 20 million devices.

And that's fact — not myth.

LITTLE FOOT comes in different versions that are ideal for motor control, load switching, and DC/DC conversion.

- N-ch MOSFETs (duals & singles)
- P-ch MOSFETs (duals & singles)
- N- & P-ch MOSFETs

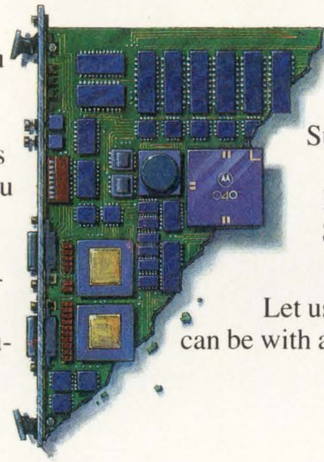
Voltage:	20-50 V (200 V coming)
On-resistance:	50-300 mΩ
Current Rating:	4.5 A
Power Dissipation:	2 W

Call our toll-free hot line now! **1-800-554-5565, ext 964.** Ask for your LITTLE FOOT design kit and evaluation board. And remember at Siliconix we're bringing a seamless power interface to the digital world.

Siliconix

2201 Laurelwood Rd, Santa Clara CA 95056

Why Settle for ½ an '040 Board?



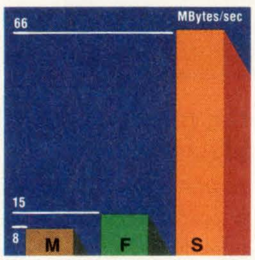
You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

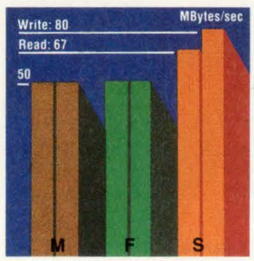
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



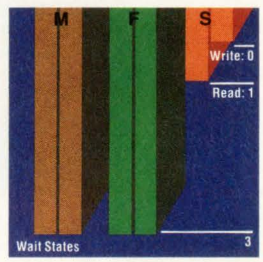
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



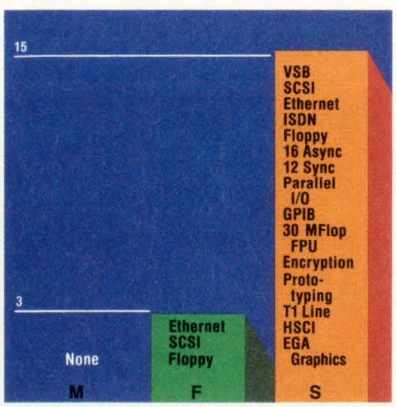
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



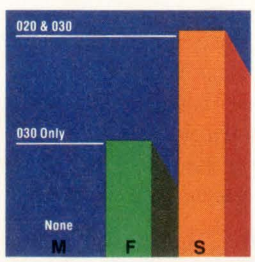
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



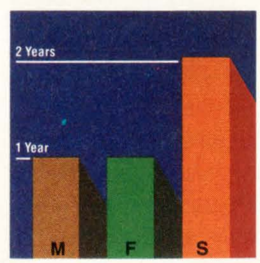
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



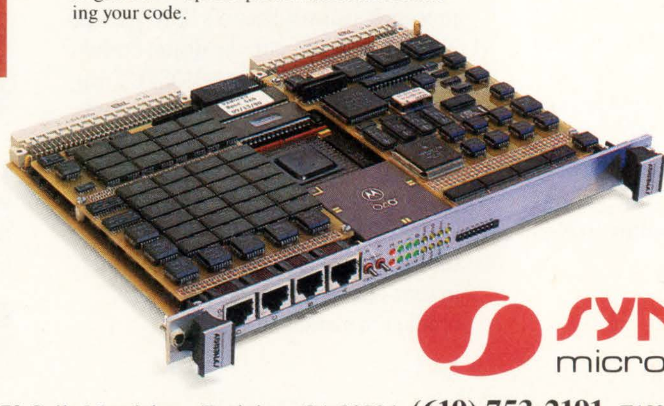
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 **(619) 753-2191** FAX: 619-753-0903

CIRCLE NO. 60

EDITED BY JULIE ANNE SCHOFIELD

Readers help themselves via EDN BBS

My question is in reference to D Fletcher's design idea "PC printer port performs I/O" in the October 10, 1991, issue of EDN. The Turbo C listing does not include the definition of the function outportb(). Does anyone know what the definition could be?
Jim DeFilipps
Boeing Computer Services
Seattle, WA

Reader Phil Hartman (KABL Radio, San Francisco, CA) replies via the EDN BBS: *outportb()* is included in dos.h in Turbo C. The function outputs a byte to argument "port". Another Turbo C function, *outport()*, outputs a whole word. I think this second function is similar to the Microsoft C function *outp()*.

Use the following C construct:

*void outportb(int port, unsigned char byte); /*int port=port address, unsigned char=byte to be written out*/*

Good luck.

Achieving electromagnetic compatibility with Europe

Where may we obtain copies of the CISPR and IEC standards, specifically CISPR-15, IEC-555, and IEC-801? The CISPR and IEC standards were mentioned in your excellent article "European EMC Regulations: Europe lays down EMC law" in the September 16, 1991, issue of EDN.
J Ned Chatham
The Ripley Corp
Ripley, OH

European Technical Editor Brian Kerridge wrote the article you allude to and supplied the following UK and US sources for the EMC (Electromagnetic Compatibility) standards:

BSI Sales
Linford Wood
Milton Keynes MK14 6LE, UK
(908) 221166
FAX (908) 322484

American National Standards Institute
11 W 42nd St
New York, NY 10036
(212) 642-4400
FAX (212) 302-1286

See **Table 1** for expanded information about the CISPR (International Special Committee on Radio Interference (from its title in French)) and IEC (International Electrotechnical Commission) standards you seek.

Readers come through

About half a dozen readers wrote or faxed in response to the "Orphaned meter needs new LCD" question in the November 7, 1991, issue of EDN. The LCD in question was and still is manufactured by LXD Inc, which makes standard and custom LCDs.

LXD Inc
7650 First Pl
Oakwood Village, OH 44146
(216) 786-8700
FAX (216) 786-8711

Thanks also go to David Hadaway (D B Systems, Ringe Center, NH), who offered his manual for the ECD 100 meter, which is the predecessor of Mr Edester's Doric 130A, and to A Tony Maluta, who has a complete Doric 130A for Mr Edester.

And last but not least, Jan Piet de Vries (Hydra-Electronic, Emmen, The Netherlands) dug up hundreds of the NE544 servo decoder drivers that Keith Gutierrez requested in the July 18, 1991, issue.

Justify this calculation

For tolerance stack-up analysis, we usually do a root-mean-square calculation using the maximum possible error of each component. In talking to engineers at other companies, we find that this seems to be a common way of doing an analysis. Unfortunately, no one has been able to supply the theoretical justification. We would appreciate any references that would let us defend this technique or that would provide a better method.
Gary Altman
Project Director
Sea MED Corp
Bothell, WA

We think you are referring to root-sum-squared (the square root of the sum of the squares), not root-mean-square, calculations. Regardless, we do not in fact know the theoretical justification of the technique or whether a better technique exists. If any reader has such information, let us know.

Scan EDN BBS for FFTs

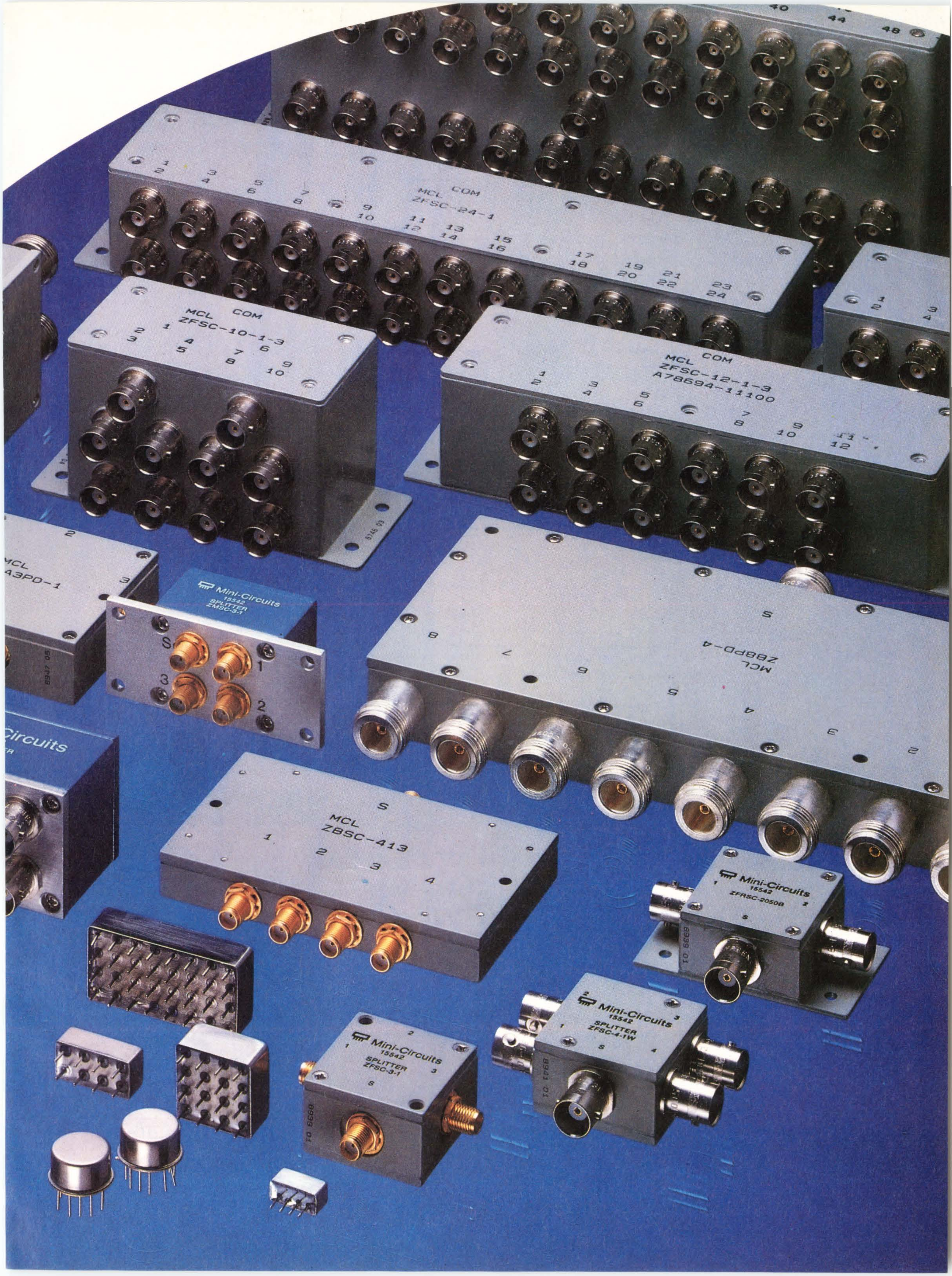
I'm looking for a fast Fourier transformation written in Quick Basic. Are you aware of a such a program listing or shareware version?
W Schwartz
Brissard, France

Log onto the EDN Bulletin Board System ((617) 558-4241, 300/1200/2400/9600, 8,N,1) and check out the /DSP and /misc Special Interest Groups. We have a variety of Basic and C FFTs.

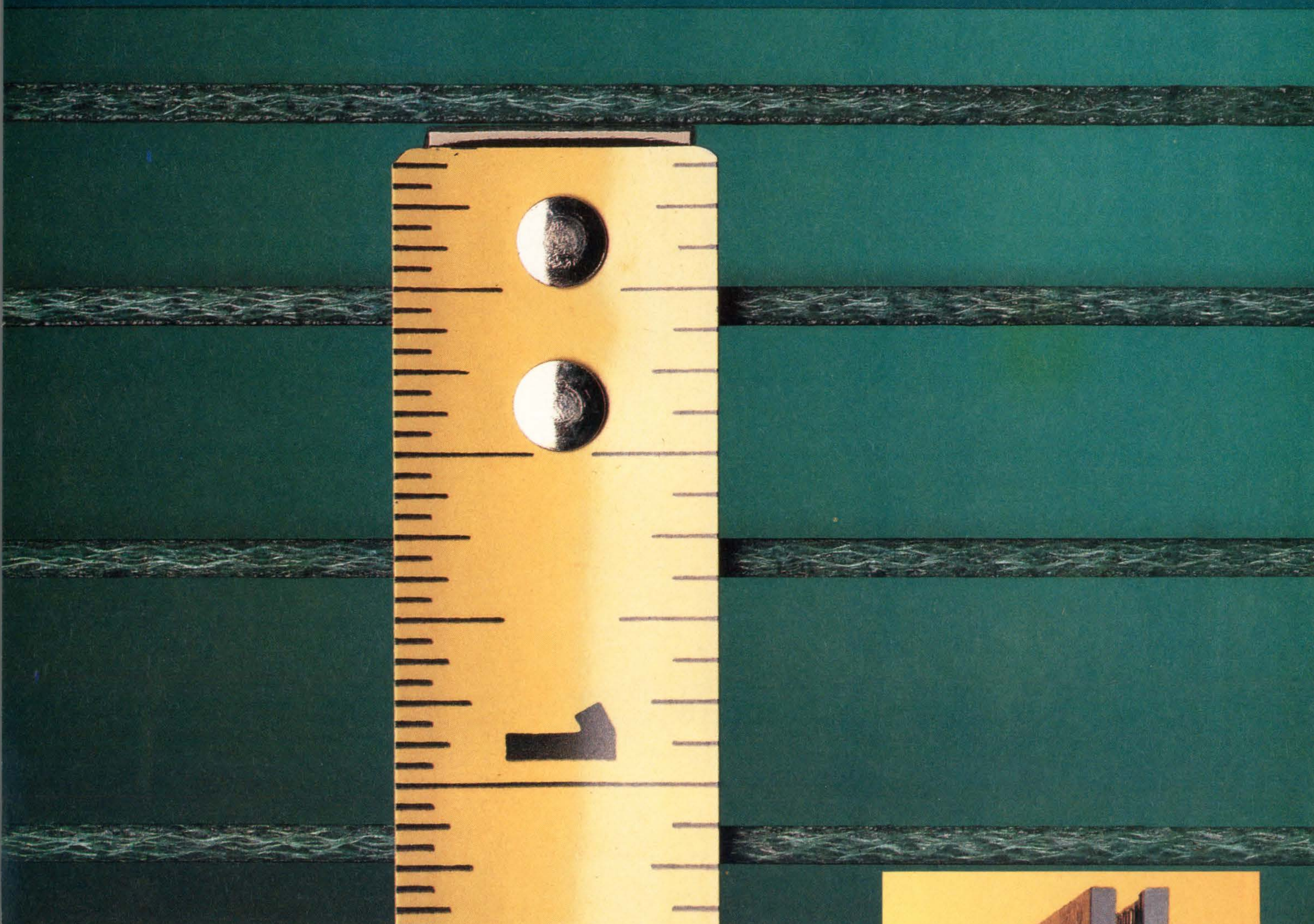
Table 1—Selected European EMC standards

Standard		Subject	Price	
CISPR 15		Lighting equipment	£62.43	$50
IEC 555	Part 1	Definitions	£29.38	$32
	Part 2	Harmonics	£39.10	$58
	Part 3	Voltage fluctuations	£81.16	$58
IEC 801	Part 1	General introduction	£14.68	$18
	Part 2	Electrostatic discharge	£71.71	$66
	Part 3	Radiated electromagnetic field	£51.84	$58
	Part 4	Fast transients	£51.81	$63
(draft)	Part 5	Surges	£8	$28
(draft)	Part 6	Conducted >9 kHz	£8	$32

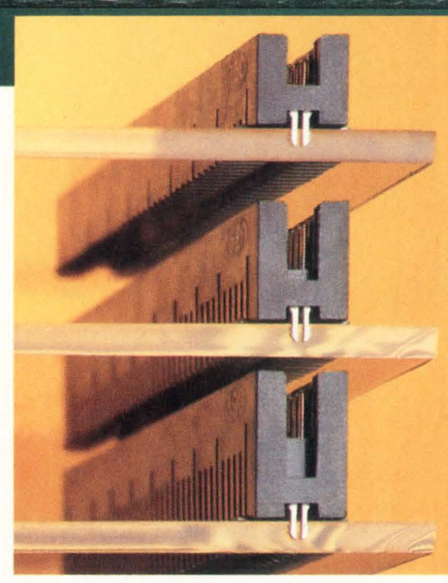
Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.


MCL COM
ZFSC-24-1
MCL COM
ZFSC-10-1-3
MCL COM
ZFSC-12-1-3
A78694-11100
Mini-Circuits
15542
SPLITTER
ZMSC-3-1
MCL
ZB8PD-4
MCL
ZBSC-413
Mini-Circuits
15542
ZFRSC-2050B
Mini-Circuits
15542
SPLITTER
ZFSC-4-1W
Mini-Circuits
15542
SPLITTER
ZFSC-3-1

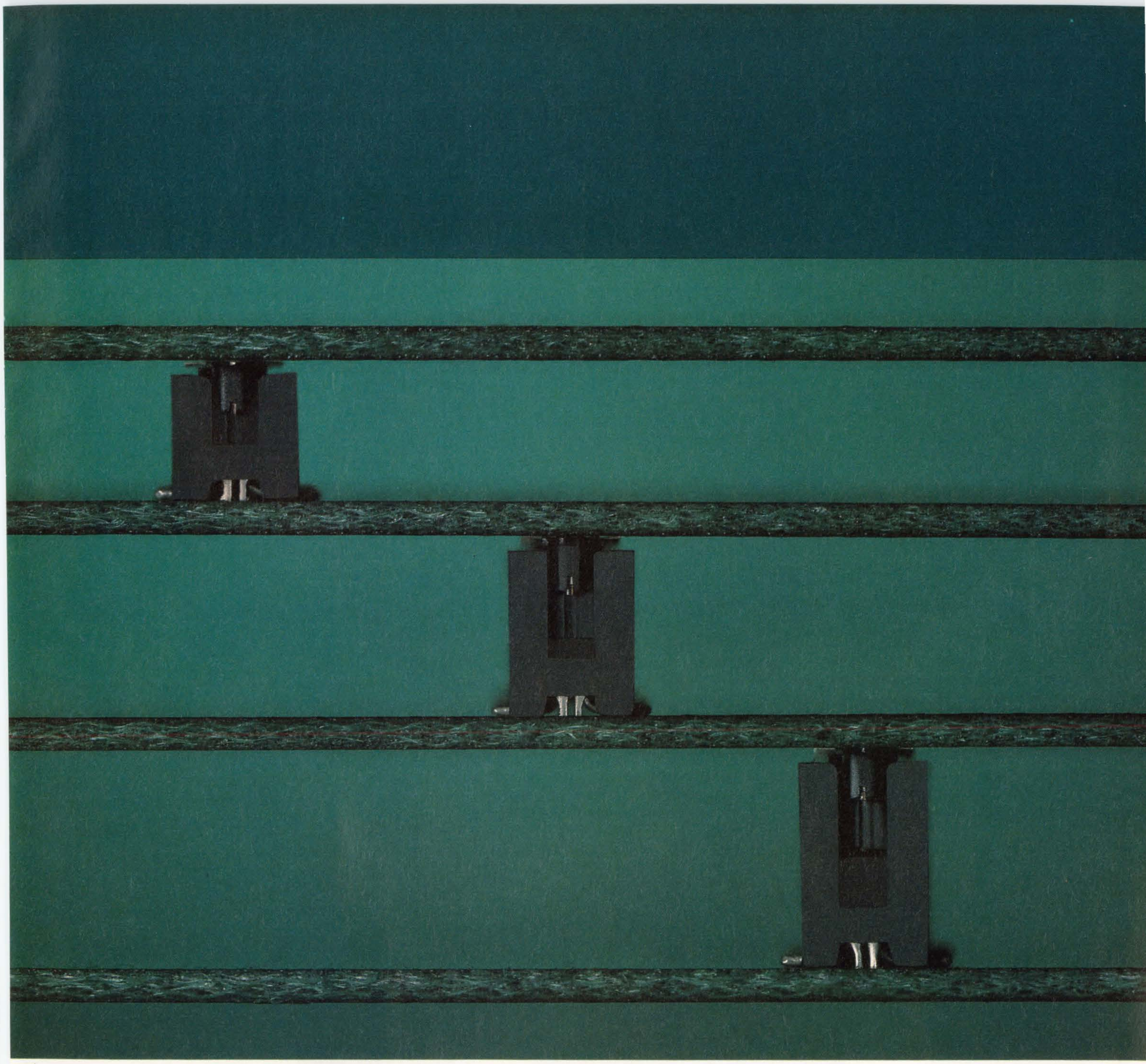
.050 centerline stackers. Close, closer, closest.



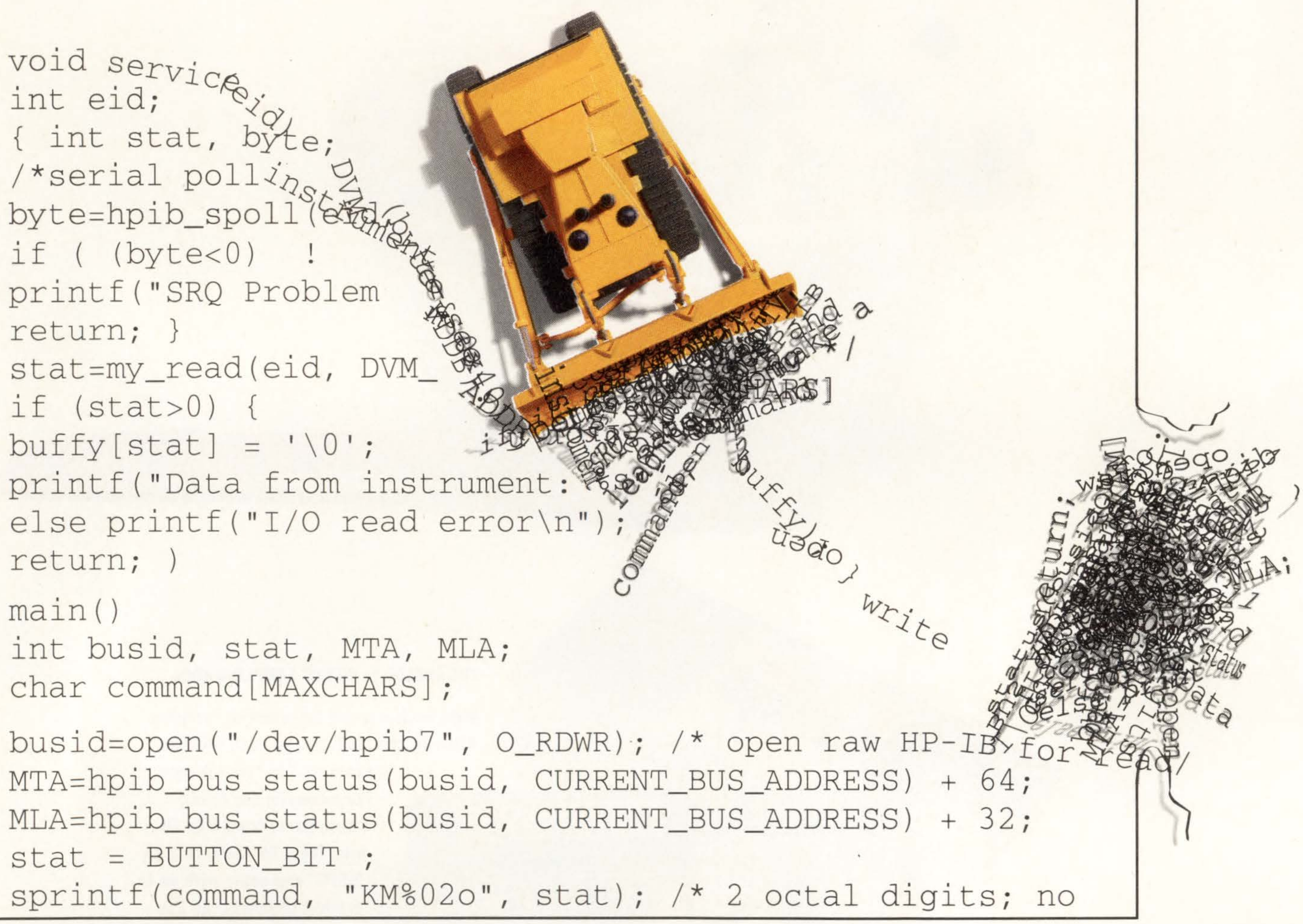
THIS IS AMP TODAY.

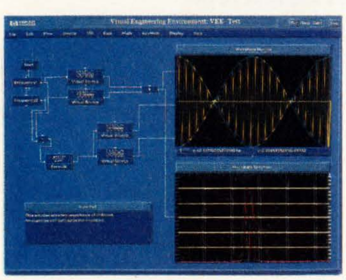


Surface-mount stack heights: .250"/.320"/.390"



Finally, engineering software that clears the way to problem solving without programming.





With HP VEE, you simply link the icons.

Computers are great for problem solving, if only programming didn't get in the way and slow you down. And now, it doesn't have to. Because the HP visual engineering environment (HP VEE) lets you solve problems without programming.

With HP VEE, you explore solutions visually by arranging and linking icons on the CRT. Each icon represents and executes a specific function for data collection, analysis—from simple mathematics to complex algorithms—and presentation. You don't have to write a single line of code.

There are two HP VEE software packages for prototyping, experimentation, and problem modeling. HP VEE-Engine, at $995*, is a general-purpose tool for analysis and presentation of existing data. HP VEE-Test includes HP VEE-Engine and adds extensive I/O capability, including soft panels and device I/O objects for $5,000*.

So, if programming is keeping you from solutions, call **1-800-452-4844.**** Ask for **Ext. 2380**, and we'll send you a brochure on clearing the way with HP VEE.

There is a better way.

HEWLETT PACKARD

* U.S. list prices.
** In Canada call 1-800-387-3867, Dept. 430.

CIRCLE NO. 26

You've got to have fun

When my brother Chris was a youngster, Mom or Dad would prod him to break away from his hobbies and other interests so he could do homework or chores. Chris would reply, "Gee, a guy's got to have a little fun around here." Even though the electronics industry is still in the doldrums, that's pretty good advice for today, too. With companies fighting for survival, it's not easy for many of us to have a little—or any—fun. Also, with many engineers out of work, life can be a lot less than fun. But fun remains an important goal for most of us.

I've always thought that without some fun, a job just isn't worth having. I'm not saying that all jobs should be a laugh a minute. Many seemingly dull and boring jobs still offer a measure of fun, and that's why people keep doing them. Perhaps that fun comes from the people we meet and know on the job, or even from some of the small things we do—things that aren't part of our main job.

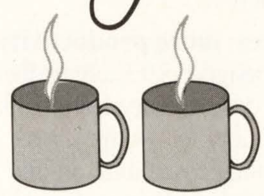
Some people I know seem to have a great deal of fun with their jobs. Jim Williams at Linear Technology sent me a copy of his company's Application Note 45 (June 1991), "Measurement and control circuit collection." The note starts off, "During my wife's pregnancy, I wondered what life would really be like when the baby was finally born." If that sentence didn't make readers do a double take, the circuits inside the app note must have.

Symbols of baby bottles accompany each circuit diagram. It seems that Jim and his newborn son Michael did circuit design in the middle of the night while Michael was guzzling bottles of baby formula. Jim assigned the circuits "bottles of merit" according to how many feedings it took to complete a circuit. The circuits range from a 1-bottle current source to a 48-bottle fluorescent-lamp power supply. There's even a picture on the app note's back page showing Michael propped up on his Dad's ancient oscilloscope. It sounds like Jim is having fun, although I don't envy him those midnight feedings.

Not everyone can have Jim's type of fun, and many people take and keep jobs simply because they have to. No fun there. Nonetheless, looking for the fun in a job and striving to get enjoyment out of what we do should be on everyone's list of goals. Without a little fun at work, we'd all go insane—or look for new jobs.

Some people think that being a magazine editor is fun. After all, we get to meet interesting people, write about neat things, and hear from readers. We also get to be among the first to know about new products and technologies. Sometimes we even get to try out new products before they reach the market. But to me, the most fun is working with interesting colleagues and coworkers. Coming up with ideas for editorials isn't always fun, but you can mark this one with two cups of black coffee.

Jon Titus
Editor



Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

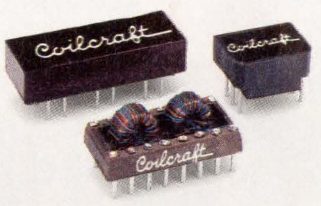
American Society of
Business Press Editors Award
1991, 1990, 1988, 1983, 1981

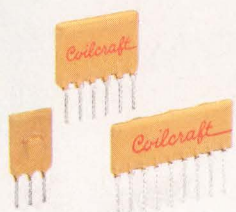
Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.

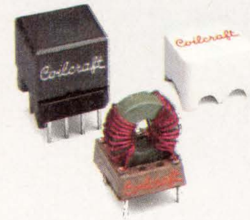
CIRCLE NO. 27

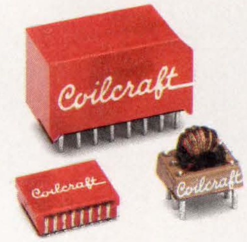
Coilcraft Data Line Magnetics

Precision components for signal filtering, network interface and EMI reduction









LAN Transformers

We can provide everything from complete sets of 10BaseT interface magnetics to individual isolation transformers for Token Ring, StarLAN, Arcnet, Ethernet or compatibles. All have fast rise times, excellent common mode rejection and meet international safety requirements.

Call for free evaluation samples.

LC Filter Networks

Choose from low, high, and bandpass filters in a variety of alignments. We offer 3, 5, or 7 pole filters in SIP, DIP or surface mount configurations. Plus our tight-tolerance chip inductors permit easy customization of cutoff frequency, rolloff, insertion loss, passband impedance, and delay.

Designer's Kit D102 contains 4 each of our 3, 5 and 7 pole low pass filters (18 MHz cutoff). $50.

Telecom Magnetics

Our family of telecommunications products includes transformers for T1, T3/DS-3, ISDN S and U Interface and impedance matching. They're compatible with most chip sets or we can customize to meet your specifications. We also offer common mode filters for "tip and ring" circuits.

Call for free evaluation samples.

EMI Filters

These board-mount filters virtually eliminate the problem of conducted EMI in data lines. They provide both differential and common mode noise attenuation from 1 MHz to over 500 MHz in a compact, easy to install package. Choose from 2, 3, 4 or 8-line versions, or we'll custom design parts to meet your specific EMC requirements.

Designer's Kit D101 contains 4 samples each of 2, 3, 4 and 8-line filters. $65.

Coilcraft

eem/electronic engineers master See our catalog in Vol. A, Section 1800

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CIRCLE NO. 84

Power tool

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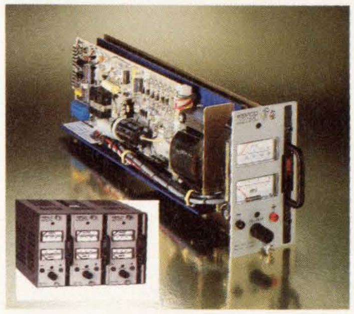

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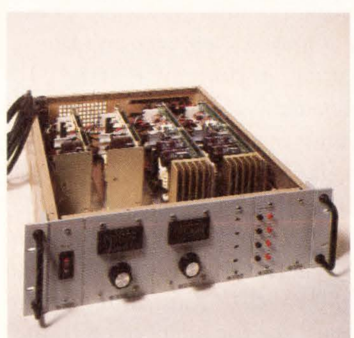

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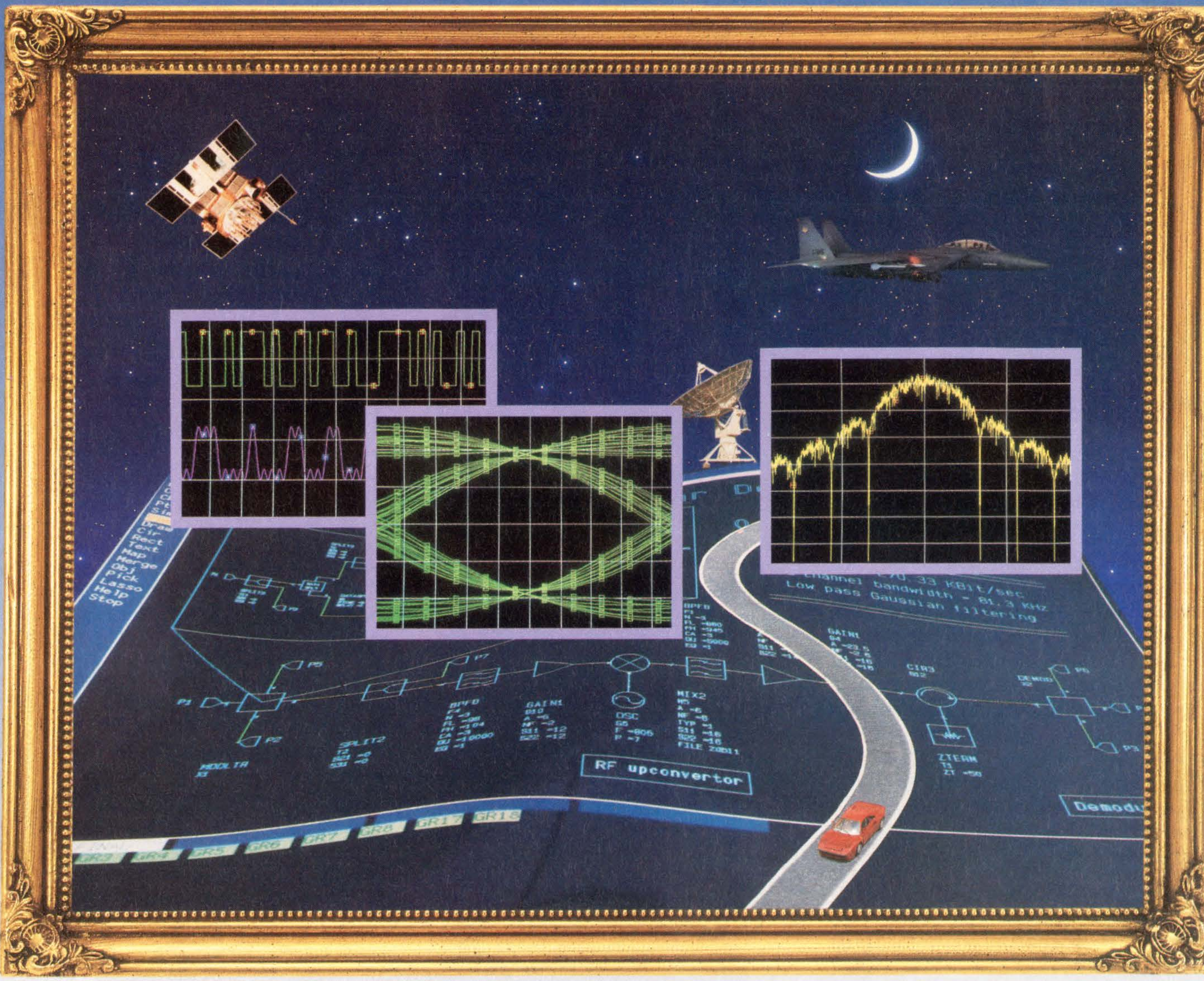

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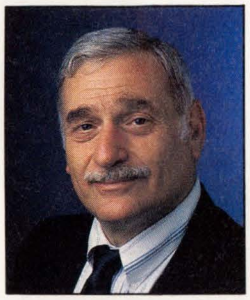
16-BIT-μC EVALUATION BOARDS

Boards let you try out μC architectures

RAY WEISS, Technical Editor



The processor selection stakes are high. Even the odds: Get an evaluation system, run some code, fool around with the software tools, and try out the on-chip peripherals.

The good news is that today's 16-bit microcontrollers (μCs) are affordable for a wide range of embedded applications. The bad news is that it's easy to choose the wrong part. One way to stack the odds in your favor is to get real, hands-on experience with actual 16-bit μC hardware and software.

Evaluation systems—boards and development software—provide a quick means to try out and match a μC architecture and tool set against your application needs (**Fig 1**). These systems let you get a feel for a μC's instruction set and peripherals. You can write trial code to time key algorithms, test out on-chip timers, and judge the μC's overall effectiveness.

Many 8-bit-system designers are reluctant to make the move to 16-bit systems. Sixteen bits bring higher processing power, more memory addressing, and the ability to handle more complex or integrated applications. But these benefits come at the expense of adapting a new architecture and development tools. Evaluation systems help ease this transition by giving developers a chance to get acquainted early with the μC and its tools.

A diverse 16-bit world

The 16-bit-microcontroller world is diverse. Some μC families suit low-end applications; others suit larger, more complex applications. Some microcontrollers have as much as 62 kbytes of program ROM and can work in single-chip applications. Others take advantage of low-cost, high-density off-chip memory. Many of these μCs have 64-kbyte banks and use bank switching to address 1 to 16 Mbytes of external memory.

First-generation 16-bit microcontrollers tend to be accumulator oriented;

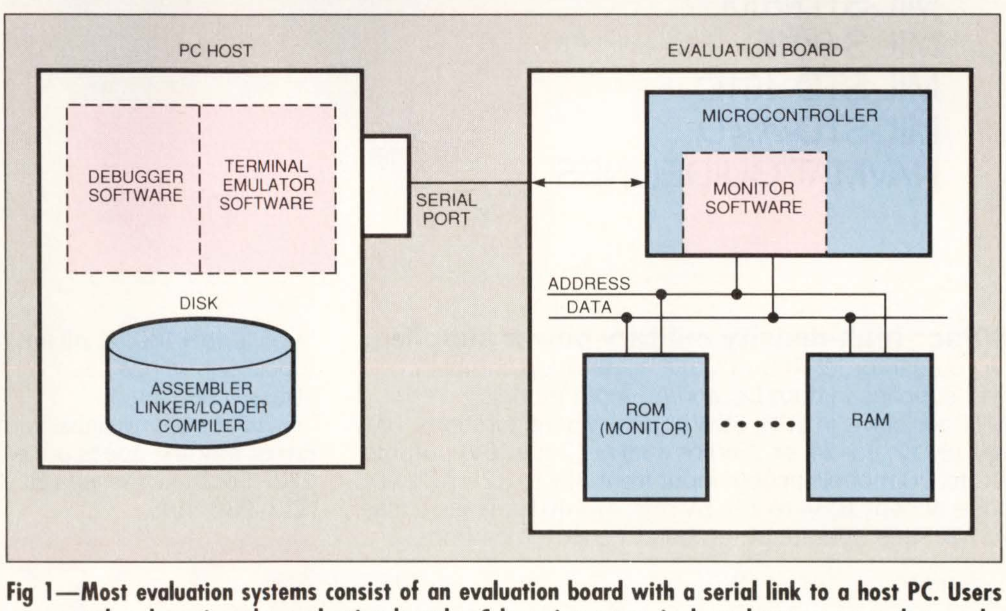
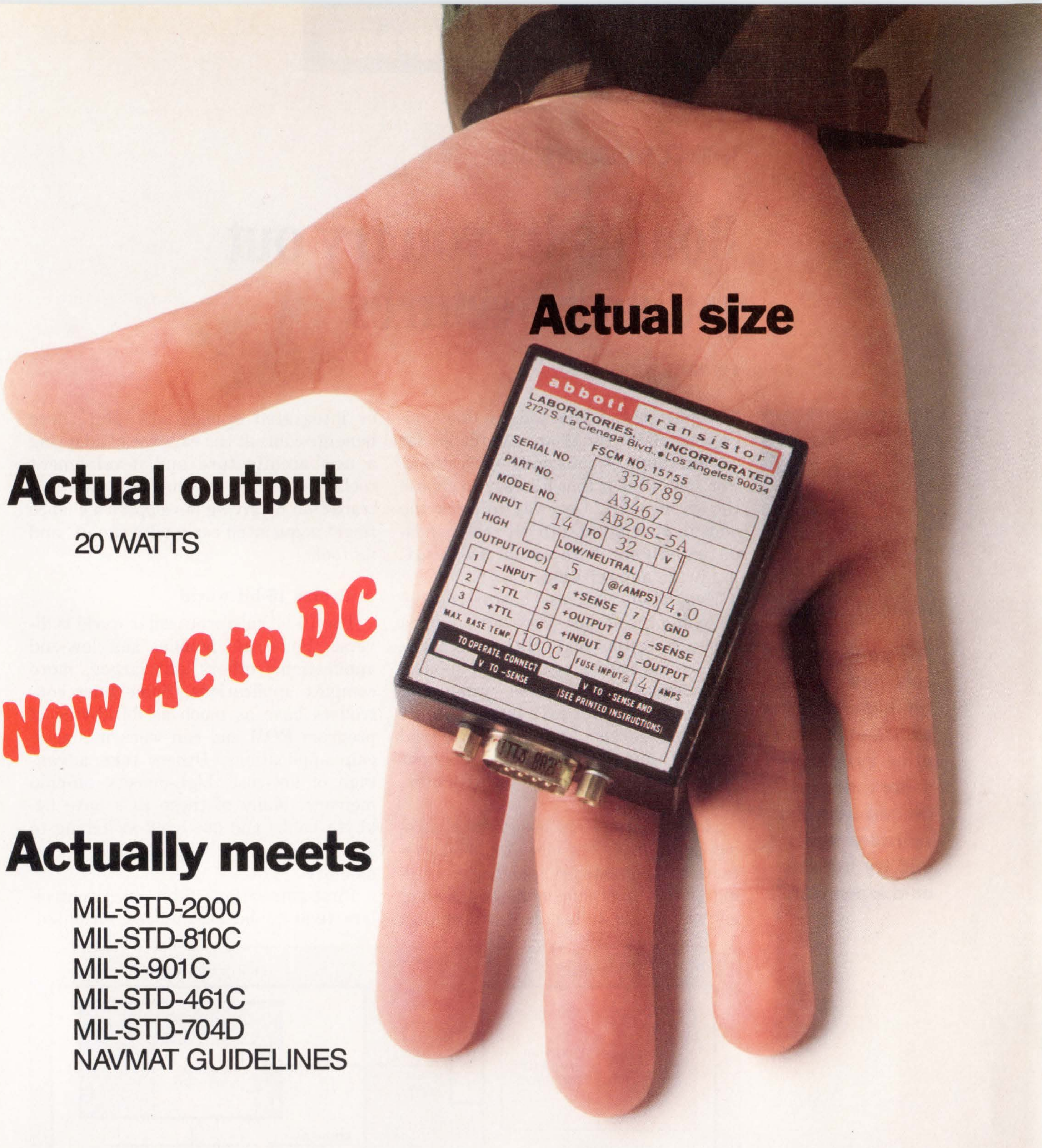


Fig 1—Most evaluation systems consist of an evaluation board with a serial link to a host PC. Users can control and monitor the evaluation-board μC by using a terminal-emulator program that works through a ROM monitor running in the μC.

Actual size



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that is, they're designed around a small set of specific registers. In many of these chips, most I/O and data-movement operations must move through the accumulator, indexed by other registers. Second-generation 16-bit μCs tend toward a set of general-purpose registers arranged in one or more register banks. Second-generation designs give users the advantage of more, easier-to-use registers and fast context switching between register banks.

Don't discount first-generation μCs: Some are quite fast, and their minimal architectures keep die sizes and costs down. However, second-generation μCs tend to be faster due to better real-estate usage and relatively recent design techniques such as pipelining.

This article covers seven 16-bit microcontroller architectures and their evaluation systems. Many of these systems were run and tested for this report. Although not quite as inexpensive as 8-bit-μC evaluation systems, most 16-bit-μC systems are fairly low cost. All but three of the systems in **Table 1** cost less than $1000.

Intel's 80C186 follows the PC

Many engineers have designed the 80186, the embedded version of the 8086, into their applications. A key advantage of the 80186 is the large software-tool and application base for Intel 808xx architectures.

The 80186 is half microcontroller and half microprocessor. Like a microprocessor, it relies on external memory and peripherals. But like a microcontroller, it has a timer, I/O port lines, and serial channels. Intel added programmable power management to the chip for low-power applications. The 186 is based on the classic 16-bit 80x86 architecture, which has a fixed register set of four general/index, four segment, and four pointer registers. A 20-bit address serves the 1-Mbyte segmented address space.

You can develop and debug application code on a PC host and then download it to an embedded μC. A simulator is not needed to test code: The PC host's CPU core is the same as the 80186 core—a 386, for example, will execute 8086 code (in real mode). Thus, you can simply code for a PC. Additionally, a trend is emerging to embed the PC itself. Embedded DOS is available, and Microsoft's Flash Memory system can serve as a substitute for disk storage. Both products are available from Annabooks.

Intel 80C186EC

Clock speed	13, 16* MHz
Instruction cycle	240 nsec min
Multiply/divide	7.3/6.7 μsec
Registers	4 data, 4 index/pointer, 4 segment, IP, status
Program memory	none
Data memory	none
Bus	multiplexed 20-/16-bit or 20-/8-bit address/data, 4-cycle read/write
Address space	1 Mbyte (segmented)
Interrupts	1 external
Serial ports	2 channel
I/O	22 lines
Timers	watchdog
Miscellaneous	4 DMA channels, clock generator, refresh controller
Package†	100-lead PLCC, PQFP
Price	$17.70 (1000)

*Ratings at selected clock rate.
†PLCC = plastic leaded chip carrier; PQFP = plas tic quad flatpack.

Intel's EV80C186EB is a compact evaluation board that includes a ROM-monitor and PC-host software. The monitor source code is supplied for you to modify. The package comes with runtime libraries for Microsoft C.

You can get PC-like interactivity by using Paradigm Systems' Locate and Debug packages for the evaluation board. These packages let you run PC C, C++, Pascal, and assembler code. You can debug the code using Paradigm's version of Borland's Turbo Debugger. Using this software, you can interactively debug at the source-code level, as you would native PC code using Borland tools—the user environment is the same.

Adding DSP to 16-bit μCs

National Semiconductor's HPC1600 is a 16-bit μC for high-speed applications. The register-based chip has an SP and a PC register and four 16-bit registers: A, B, X, and K (address boundary). Peripherals are memory mapped, and all transfers pass through the chip's main 16-bit bus. The μC has a 64-kbyte address space. On-chip program memory ranges from 0 to 8 kbytes of ROM and as much as 256 bytes of SRAM (static RAM).

Although a first-generation μC with a small set of registers, the HPC1600 delivers 100-nsec instruction cycles with a 40-MHz clock. The chip achieves that speed through the automatic extension of 8-bit values for 16-bit processing and an automatic increment/decrement for index registers speed the chip's performance. Also, instead of branch-and-test operators, many instructions have a built-in skip. When a data-move instruction's index passes a boundary condition, control skips the next instruction, thus providing a fast mechanism to terminate a loop.

National Semiconductor engineers further upped power by adding a DSP-like MAC (multiply-and-accumulate) unit to the μC. The MAC unit hangs on the main bus. It loads two 16-bit numbers, multiplies them, and accumulates the 32-bit signed result in nine clock cycles (450 nsec).

National Semiconductor's evaluation systems for the HPC1600 start with the HPC Designer Kit. The kit is built around an evaluation

Text continued on pg 46

Table 1—Representative 16-bit-μC evaluation boards

Board vendor	Microcontroller	Board: Hardware	Board: Software	Price	Comments	Circle number
AT&T Microelectronics 555 Union Blvd Allentown, PA 18103 (800) 372-2447	DSP16A 30 MHz 8-kbyte ROM 4-kbyte RAM	DSP16A-BD-EVAL: PC/XT plug-in board 32-kbyte program RAM sigma-delta codec 8-kbyte dual-port RAM, 128-kbyte RAM	Assembler linker/loader windowed debugger	$2200	Board runs on PC/AT bus. Window-based debugger; utilities link host C code to DSP board.	659
Forth Systeme Box 1103 D-7814 Breisach AM Rhein Germany	**Siemens** SAB80C166 20 MHz 1-kbyte SRAM 32-kbyte ROM	Modunorm 80C166: As much as 192-kbyte EPROM wrapped-wire area 64-kbyte RAM real-time clock battery backup	Assembler (from Siemens) Swiss-Forth ($2950)	$399	Surface-mount evaluation and application board. Requires simple breadboard circuit to link to PC host. EPROM set costs $100.	660
Hitachi America Ltd Semiconductor & IC Div 2000 Sierra Point Pkwy Brisbane, CA 94005 (415) 589-8300 FAX (415) 583-4207	H8/325 10 MHz 32-kbyte PROM/ROM 1-kbyte SRAM	H8/325 EVB: 64-kbyte EPROM 32-kbyte SRAM dual UART 6-LED display EPROM program adapter	Line assembler/ disassembler ROM monitor terminal emulator C compiler optional linker/loader assembler available X-ray debugger interface	$415	Has a 28-pin programming adapter (can program μC as EPROM). Can interface to both terminal and host CPU. Uses Microtek X-ray debugger and Motorola S file format.	661
Intel Corp Embedded Processor Group 5000 W Chandler Blvd Chandler, AZ 85226 (602) 554-2649	87C196KR 16 MHz 16-kbyte EPROM 744-byte RAM UART port	EV80C196: Uses on-chip EPROM precision ADC configurable board (EPLD)	Line assembler/ disassembler ROM-monitor host interface assembler, C compiler available	$390	Has software for peripherals and porting 8051 assembly code for the 196. Has 2 single-step modes and flexible memory configuration to match application (8, 16 bits, multiple wait states).	662
	80C186EA 16 MHz 2 DMA channels	EV80C186EA/XL: 32-kbyte EPROM (with monitor) 32-kbyte SRAM 512-kbyte DRAM (expansion) configurable board (EPLD) socketed for 80C187	ROM-monitor host interface C assemblers available can use PC software	$400	Can add as much as 512 kbytes of DRAM using an expansion bus. Board has digital I/O: status port, LED block, 4-bit port to define board parameters.	663
International Microsystems Inc 621 Valley Way Milpitas, CA 95035 (408) 942-1001 FAX (408) 942-1051	**Toshiba** TMP68303F 16 MHz	SBC303: 128 kbytes to 2 Mbytes EPROM 256 to 512 kbytes SRAM 512 kbytes to 8 Mbytes DRAM 3 serial, 1 parallel ports clock/calendar flash-EPROM programmer	monitor line assembler disassembler	$495	Has memory-expansion connector with sample code. Emulator board for ICE optional.	664
Motorola Microprocessor Products Group 6501 William Cannon Dr W Austin, TX 78735 (512) 440-2000	68HC16Z1 16 MHz 1-kbyte SRAM	M68HC16Z1 EVB: 64-kbyte SRAM (or EPROM) 64-kbyte SRAM (not populated) UART sockets for μP ports wrapped-wire area	Assembler/disassembler monitor symbolic debugger real-time kernel filter-design package floating-point software	$168 (1st quarter of 1992)	Has integrated assembler, monitor, debugger. Windowed development tools. Full set of software including a Quickstart set of application routines. Each port has its own easy-to-use header.	665
	68302 20 MHz	M68302ADS: 256-kbyte EPROM 500-kbyte DRAM 2-kbyte EEPROM (socket for 500-kbyte DRAM) optional emulation cable	Uses existing 68000 tools event-driven OS chip driver communications software monitor	$2800 board, $500 interface card, $700 cable, $4000 total	Comes with software support package for developing communications software. Has protocol modules for OSI layer 2 (LAPB/D), 3 (X.25) protocols.	666

Board vendor	Microcontroller	Board: Hardware	Board: Software	Price	Comments	Circle number
Motorola *continued*	DSP56156 40 MHz 4-kbyte ROM 4-kbyte SRAM	DSP5615 ADS	Assembler linker/loader monitor terminal emulator disassembler assembler/linker/ simulator	$3000	Has 2-board development system: interface board (PCs, Macintoshes, Sun workstations) and standalone evaluation board. ICE-like debugger uses on-chip emulation features. Assembler/linker/simulator option ($495).	**667**
National Semiconductor Corp 2900 Semiconductor Dr Santa Clara, CA 95051 (408) 721-5000 FAX (408) 730-0764	HPC16003/83 30 MHz 8-kbyte ROM 256-byte RAM	HPC Designer Kit 8-kbyte overlay RAM 32-kbyte ROM monitor as much as 64-kbyte RAM target emulation cable	Assembler linker/loader monitor host interface C compiler (limited) function library	$950	Board comes with C compiler limited to 3 kbytes of code; full C compiler optional. Board can be used to emulate target μC. System handles as many as 1000 lines of code. Board has emulation plug for 32-pin EPROM socket.	**668**
	HPC46100 40 MHz 1-kbyte RAM	HPC+ Development Kit 64-kbyte RAM on logic-analyzer-interface board, 64-kbyte RAM on evaluation board	Assembler linker/loader monitor host interface disassembler library	$950	16-bit μC with DSP capabilities. Kit includes target board, test board, and ROM emulator. Logic-analyzer interface for real-time trace.	**669**
NEC Electronics Inc 401 Ellis St Mountain View, CA 94039 (415) 960-6000 FAX (800) 729-9288	μPD78334 16 MHz 32-kbyte EPROM 768-byte SRAM	EB-78K334-PC 32-kbyte SRAM 32-kbyte EPROM ROM programmer	Assembler linker/loader monitor terminal emulator source debugger C compiler	$595	The evaluation board can be used as an ICE for applications using on-chip memory. An optional emulation plug plugs into target socket.	**670**
Oki Semiconductor Inc 650 N Mary Ave Sunnyvale, CA 94086 (408) 720-1900	67620	EVA67K 64-kbyte SRAM 512-kbyte video RAM	Assembler linker/loader librarian debugger (C and assembly) C compiler available	$450	The 67620 is a 200-nsec, 16-bit, second-generation μC and has two 8-bit and three 16-bit timers and a 64-kbyte address space.	**671**
Siemens Components Inc Semiconductor Group 2191 Laurelwood Rd Santa Clara, CA 95054	SAB80C166 20 MHz 32-kbyte ROM 1-kbyte SRAM	EVA-166 4-kbyte EPROM (with monitor) 64-kbyte RAM wrapped-wire area	Line assembler terminal emulator monitor	$450	All chip pins to DIN connector. Can add expansion board, to 256 kbytes.	**672**
Signetics (Philips Components) 811 E Arques Ave Sunnyvale, CA 94088 (408) 991-2000 FAX (408) 991-2311	SCC6870 10 MHz 4-kbyte ROM 256-byte RAM SCC66470B	SM68070 SK 256-kbyte ROM/EPROM 512-kbyte RAM I²C serial port color-monitor interface video-system controller wrapped-wire area	Assembler/disassembler loader monitor symbolic debugger	$695	This board is a complete video-frame-grabber system. It handles 640×240-pixel screens with 16 colors/pixel and drives TV/monitor RGB signals.	**673**
Texas Instruments Inc Box 1443 MS 719 Houston, TX 77251 (713) 274-2000 FAX (713) 274-2445	TMS320C16 35 MHz 16-kbyte ROM 512-byte RAM	TMS320C16 EVM 128-kbyte RAM PC/AT half card analog interface optional	Assembler disassembler linker/loader symbolic debugger	$995	PC/AT plug-in board. Acts as coprocessor to PC host.	**674**

Notes: 1. DRAM=dynamic RAM; ICE=in-circuit emulator; SRAM=static RAM.
2. For more information on the 16-bit-μC evaluation boards listed in this table, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service.

module that has an HPC1600 μC and 62 kbytes of EPROM for program test. The kit includes a cable for emulating target μCs, a monitor, host-interface software, an assembler, and a limited C compiler. (A full C compiler is an option.)

National Semiconductor HPC46100

Clock speed	20, 30, 40* MHz
Instruction cycle	100 nsec typ
Multiply/divide	4 1.5/1.5 μsec, 450-ns MAC cycle
Registers	A, B, X, K, SP, PC
Program memory	off chip
Data memory	1-kbyte SRAM (banks, stack), 128-byte EEPROM
Bus	16-/16-bit or 16-/8-bit address/data
Address space	64-kbyte instructions/data
Special feature	32-/16-bit DSP MAC unit
Interrupts	3 external
Serial ports	3 UARTS, Microwire+ (serial network bus)
I/O	51 lines
Timers	seven 16-bit (with watchdog)
Miscellaneous	8-channel, 8-bit ADC; PWM
Package†	80-pin QFP
Price	$16.44 (10,000)

*Ratings at selected clock rate.
†QFP = quad flatpack.

The HPC+ Development Kit includes an evaluation module and an emulation board. The board plugs directly into a target system's EPROM socket and emulates the target-board ROM with easy-to-change SRAM. The kit also has an interface for the Hewlett-Packard 1650/16500 logic analyzer for solving hard-to-test problems.

K3 bridges 8- and 16-bit worlds

The NEC K3 μC bridges the gap between the 8- and 16-bit worlds. The μC has a 16-bit ALU, but relies on an 8-bit, 8085-like external bus. The chip is organized around banks of 16 general-purpose 8-bit registers or eight 16-bit registers. Programs can address as much as 64 kbytes of instructions and data in a single address space. The μC holds 32 kbytes of instructions and 1 kbyte of data on chip.

The K3 provides three interrupt handling methods: the standard vectored-interrupt method, context switching, and Macroservice. In the first method, interrupt processing transfers to the code the interrupt-vector-table entry references for that interrupt. In the second, the active register bank changes to the bank specified by the interrupt-table entry; each bank includes a program-counter value. And in the third method, hardware performs programmed functions on a cycle-stealing basis. The hardware moves data blocks and checks and modifies data without interrupting or using the CPU.

NEC K3 μPD78334

Clock speed	12, 16* MHz
Instruction cycle	250 nsec min
Multiply/divide	1.2/4.8 μsec
Registers	eight 16 bit (8 banks)
Program memory	8-/32-kbyte EPROM/ ROM
Data memory	768-byte SRAM
Bus	16-/8-bit address/data (8085)
Address space	64 kbytes
Interrupts	3 hardware (0.4 μsec)
Serial ports	46
I/O	48 lines
Timers	watchdog, two 16 bit, two 16-bit up/down counters
Miscellaneous	8-channel, 10-bit ADC; dedicated memory-expansion chip
Package†	84-/94-pin PLCC/QFP
Price	$15.15 (10,000) with ROM

*Ratings at selected clock rate.
†PLCC = plastic leaded chip carrier; QFP = quad flatpack.

NEC has simplified assembly-language processing for its microcontrollers, which have a structured assembler. Essentially, a preprocessor enables programmers to use higher-level control structures for looping, case select (switch), incrementing, and decrementing. The preprocessor converts these higher-level statements to assembly language prior to assembly.

The NEC EB-78330 evaluation board holds 32 kbytes of SRAM for program and data. The board comes with a monitor and a symbolic debugger. A terminal emulator lets users download, query, and control application code running in the board's K3 μC under the monitor. The monitor lets you set up as many as four parallel, complex-instruction breakpoints. An optional emulation pod plugs into a target board for single-chip applications. The pod functions as an ICE (in-circuit emulator) by controlling target execution.

Motorola adds DSP to 16-bit μC

Motorola's new 16-bit μC, the 68HC16, provides an easy upgrade path for 16-bit processing: The chip is upwardly compatible with the company's popular 68HC11 8-bit microcontroller. The 16-bit chip follows the older accumulator-based architecture, but it has two accumulators and three index registers, compared with the 68HC11's single accumulator and two index registers. Unlike the earlier 8-bit μC, the initial 68HC16Z1 chip isn't for single-chip applications: It has only 1 kbyte of SRAM. Future releases will have on-chip ROM or EEPROM.

The 68HC16 is more than just a 16-bit extension to the 68HC11: It includes a DSP MAC unit as well as two 16-bit multiply registers and a 35-bit result register. Additionally, the 68HC16 uses peripherals Motorola developed for its 683xx family of 16- and 32-bit μCs. These peripherals include a serial controller, a general-purpose timer, and a system-integration module for I/O. The peripherals are linked to the CPU via an intermodule bus.

The 68HC16Z1 evaluation module is a compact, well-designed board. It has a prototyping area and headers for each of the μC's ports. This module stands out in the amount and range of software bundled with it. The board has an integrated assembler, editor, windowed debugger (MASM); a ROM

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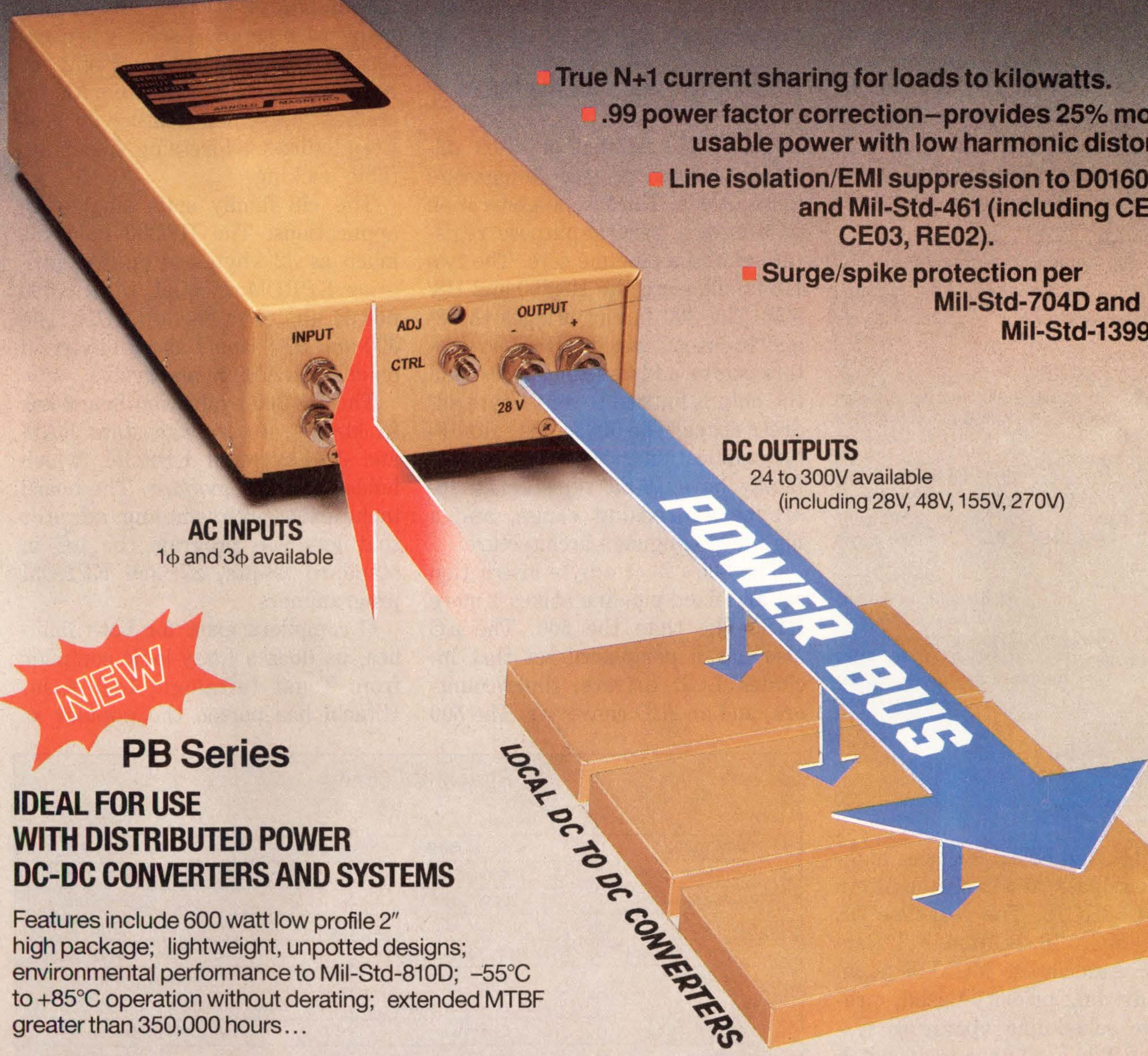

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monitor; a real-time kernel, and a DSP filter-design package. The Quickstart package gets the board up and running with a minimum of fumbling around.

P&E Microsystems developed MASM, which provides the same interactive, windowed interface used for other Motorola µCs. Momentum Data Systems Inc supplies the filter-design package, which is a subset of Momentum's QEDesign Series. The package lets you build IIR, FIR, and EFIR lowpass, highpass, bandpass, and bandstop filters for the 68HC16. The real-time OS kernel, MCX-16, is from A T Barrett & Associates. MCX-16 is an event-driven, priority-based, preemptive scheduling operating system and has a 20-µsec task-switch time. The OS takes up 2 kbytes of memory and can dynamically create and schedule tasks.

Motorola 68HC16Z1

Clock speed	16.78* MHz
Instruction cycle	360 nsec typ (120 nsec min)
Multiply/divide	0.48/2.3 µsec, 720-nsec MAC cycle
Registers	16 bit: 2 accumulate, 3 index, SP, PC, 4 multiply/accumulate
Program memory	off chip
Data memory	1-kbyte SRAM
Bus	20-/16-bit address/data (byte sizable), 2-cycle access
Address space	1-Mbyte instruction, 1-Mbyte data, sixteen 64-kbyte banks
Interrupts	7 hardware (3.3 µsec), 256 sources
Serial ports	queued serial module
I/O	50 lines
Timers	general-purpose timer, watchdog
Miscellaneous	8-channel, 10-bit ADC; hardware background debug
Package†	132-pin PQFP
Price	$20 (1000)

*Ratings at selected clock rate.
†PQFP=plastic quad flatpack.

Motorola is developing a low-cost test alternative to evaluation boards and ICEs for the 68HC16. This test alternative, which will be announced in the first quarter, takes advantage of the µC's background debug mode. This mode lets you do host-controlled debugging without an ICE. You must design in a small 10-pin header on the target board to provide the host access to the µC's background-control mode.

H8 family covers all the bases

Hitachi's H8 families of 16-bit microcontrollers suit mid- to high-end applications. The second-generation µCs have a general-purpose register set and a pipeline core. The two H8 families are the H8/300 and H8/500. The 300 family bridges the 8- and 16-bit-µC worlds. H8/300 registers can be addressed as bytes, and the chip is limited to a 64-kbyte address space. The 500 series suits 16-bit applications. Members of this family have 16-bit registers, a 16-Mbyte addressing range, and a high-level-language architecture.

The 300's 2- or 4-byte instruction set and fixed pipeline makes it more RISC-like than the 500. The µC also has a peripheral set that includes LCD drivers, timer/counters, and an A/D converter. The 500 is an upgrade of the 300 and suits high-level languages like C. It has an orthogonal instruction set (all instructions can use all addressing options) with automated stack and frame pointers. The 500 has as many as nine I/O ports, seven external interrupts, and a PWM for real-time control. An automatic increment/decrement feature for register indirect addressing speeds up table walking.

The H8 family suits single-chip applications: The H8/300 holds as much as 32 kbytes of on-chip program EPROM or ROM; the H8/500 has 64 kbytes of on-chip ROM. The 300 and 500 have 1 and 2 kbytes of on-chip SRAM, respectively.

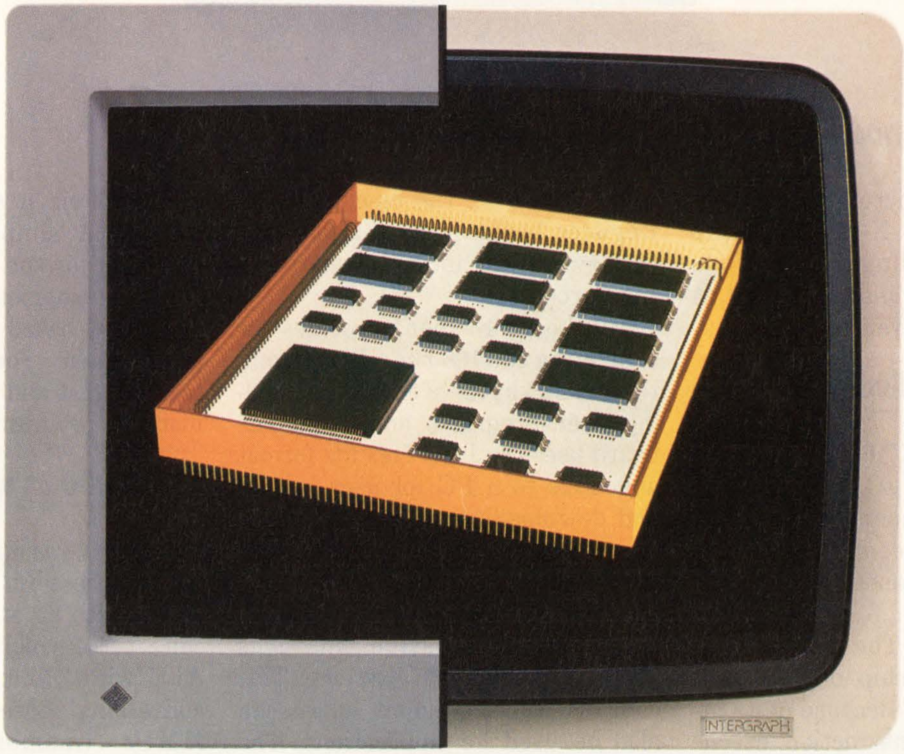
The H8/300 evaluation board has 32 kbytes of zero-wait-state RAM and 32 kbytes of EPROM, which holds the ROM monitor. The board includes a programming adapter that lets you program the µC in standard 28-pin, 27C256 EPROM programmers.

C compilers exist for both families, as does a fuzzy-logic compiler from Togai Infralogic Inc. Also, Hitachi has ported the popular x-

Hitachi H8 family

	Hitachi H8/330	H8/536
Clock speed	6, 8, 10* MHz	6, 8, 10 MHz
Instruction cycle	200 nsec min	200 nsec min
Multiply/divide	10/100 µsec	2.3/2.6 µsec
Registers	8 16 bit or 16 8 bit	8 16 bit
Program memory	8-/32-kbyte EPROM/ROM	64-kbyte ROM
Data memory	512 bytes	2-kbyte SRAM
Bus	16-/8-bit address/data	24-/16-bit or 24-/8-bit address/data
Address space	64 kbytes	16 Mbytes (64-kbyte banks)
Interrupts	9 external (2 to 3 µsec)	7 external
Serial ports	1 channel	2 channels
I/O	58 lines (16 LCD drivers)	57 lines (16 LCD drivers)
Timers	watchdog, two 8 bit, one 16 bit	watchdog, one 16-bit counter, one 8-bit, 1 PWM
Miscellaneous	8-channel, 8-bit ADC	8-channel, 10-bit ADC
Package†	80-/84-pin PQFP/PLCC	80-/84-pin PQFP/PLCC
Price	$16 (1000)	$34.10 (1000)

*Ratings at selected clock rate.
†PLCC=plastic leaded chip carrier; PQFP=plastic quad flatpack.



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ray debugger (Microtec Research) to the H8 family. X-ray lets users interactively debug target code running on the evaluation board at the source-code level.

Siemens 166 delivers

Siemens's SAB80C166 is a second-generation 16-bit μC built for high performance. Its compact execution unit has a 4-stage pipeline and is built around sixteen 16-bit general-purpose registers, 8 of which are byte addressable. The μC can function as a single chip or run with external memory. Because of its internal pipeline, instruction execution takes one 100-nsec machine cycle; 16-bit multiplies and 32-bit divides execute in 0.5 and 1.0 μsec, respectively. Jumps are sped from 200 to 100 nsec by using a branch target cache to hold recent jump addresses.

The 166 has a 256-kbyte address space organized as four 64-kbyte segments. The μC has three off-chip memory modes for an 18-bit address: 16-bit data, 16-bit data multiplexed with address, and 8-bit multiplexed data. The 166's general-purpose registers function as a bank for easy relocation via a context pointer in the on-chip RAM. Register banks provide a fast context switch for interrupt and real-time processing.

The board Siemens provides for evaluating the 166 has a ROM monitor and 32 kbytes of SRAM for holding user programs and data. The board uses the Intel Hex file format and links to a PC for user control and downloading. A line assembler and terminal emulator come with the board. An assembler and C compiler are optional.

Another evaluation board is available form Forth Systeme. This compact surface-mount board can also be used for applications. The board has 64 kbytes of RAM and provisions for as much as 256 kbytes of EPROM. It has two headers (128 pins total) for interfacing and links to a PC via a simple breadboard circuit. A simple ROM Forth is available for the board as is SwissForth—a sophisticated Forth with a window-based host development environment. Forth provides an extremely fast and interactive mechanism for program development.

Siemens SAB80C166

Clock speed	20 MHz
Instruction cycle	100 nsec min
Multiply/divide	0.5/1.0 μsec
Registers	16 (banks)
Program memory	8-/32-kbyte EPROM/ROM
Data memory	1-kbyte SRAM, 128-byte EEPROM
Bus	16-/8-bit or 16-/16-bit address/data
Address space	256 kbytes, 64-kbyte segments
Interrupts	3 hardware (0.5 μsec)
Serial ports	2 UARTs
I/O	76 lines
Timers	watchdog, seven 16-bit
Miscellaneous	10-bit ADC (9.75 μsec), peripheral service, 16 PWM channels
Package†	100-pin PQFP
Price	$46 (1000)

†PQFP = plastic quad flatpack.

The 68000 as a microcontroller

The 68000 was one of the first 16-bit microprocessors. It made its reputation with its straight-forward architecture, which combines a 16-bit ALU with 32-bit registers for easy addressing. Later, Motorola added MMUs (memory management units) to ease managing large address spaces and to introduce a level of indirection and memory mapping.

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16-BIT-μC EVALUATION BOARDS

68XXXX μCs

	Signetics 68070	Toshiba 68301	Motorola 68302
Clock speed	10, 12.5, 15* MHz	12, 16* MHz	16.77, 20 MHz
Instruction cycle	0.9 μsec typ	1.0 μsec	1.0 μsec
Multiply/divide	5/10.7 μsec	4.7/9.5 μsec	3.0/7.8 μsec
Registers	32-bit, 16-bit ALU; 8 data, 7 address, 2 stack pointers, 1 program counter	32-bit, 16-bit ALU; 8 data, 7 address, 2 stack pointers, 1 program counter	32-bit, 16-bit ALU; 8 data, 7 address, 2 stack pointers, 1 program counter
Program memory	none	none	none
Data memory	none	none	1152-byte RAM
Bus	24-/16-bit address/data	24-/16-bit address/data	24-/16-bit address/data
Address space	8-segment MMU, 16 Mbytes	8-segment MMU	8-segment MMU
Interrupts	6 hardware (0.4 μsec)	3	7
Serial ports	UART, I²C	3 UARTs	3 communications channels
I/O	none	16 lines	28 lines
Timers	one 16 bit	one 16 bit	three 16 bit
Package†	84-/120-pin PLCC/PQFP	100-pin PQFP	132-pin CQFP/PGA
Price	$15.25 (1000)	$24.55 (100)	$35.16 (1000)

*Ratings at selected clock rate.
†CQFP=ceramic quad flatpack; PGA=pin-grid array; PLCC=plastic leaded chip carrier; PQFP=plastic quad flatpack.

Today, there are μCs that use the 68000 as a core. Motorola's 68302 is built around the 68000. The chip suits communications processing and includes an on-chip RISC CPU for processing on-line data. Both Signetics and Toshiba also have versions of the 68000 μC. These chips are beefed up for embedded systems with I/O lines, serial ports, and 16-bit timers. All of these 68000 μCs have an MMU and run existing 68000 code.

Motorola's 68302 Application Development System (ADS) helps users develop embedded communications applications. The system includes communications protocols, an event-driven operating system, and an evaluation board that has as much as 1 Mbyte of DRAM (dynamic RAM) and 256 kbytes of program EPROM. The board has hooks for a logic analyzer.

Signetics' Microcore board integrates the company's SCC68070 μC with a video-system controller. The board can be used to drive a color video display as well as check out the SCC68070. Microware has ported its OS/9 real-time operating-system kernel and C development tools to the Microcore board. Additionally, Microtec Research has a C compiler, assembler, and version of its x-ray debugger for the board.

International Microsystems Inc makes an evaluation board, the SBC303, for the Toshiba TMP68303 μC. This board has as much as 2 Mbytes of EPROM, 512 kbytes of SRAM, and 8 Mbytes of DRAM. It includes a clock/calendar and parallel and serial ports as well as a ROM monitor and boot and I/O drivers. The board works with Software Development Systems' Freeform C source-level debugger and US Software's Multitask real-time operating system. EDN

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Config				
12	#1 M5			
24	#1 M4	#2 K		
26	#1 M4	#2 L		
30	#1 M3	#2 L	#3 K	
36	#1 M3	#2 K	#3 K	
48	#1 M3	#2 K	#3 K	#4 K
56	#1 M3	#2 K	#3 K	#5 J / #4 J
64	#1 M3	#2 K	#6 J / #3 J	#5 J / #4 J
72	#1 M3	#7 J / #2 J	#6 J / #3 J	#5 J / #4 J

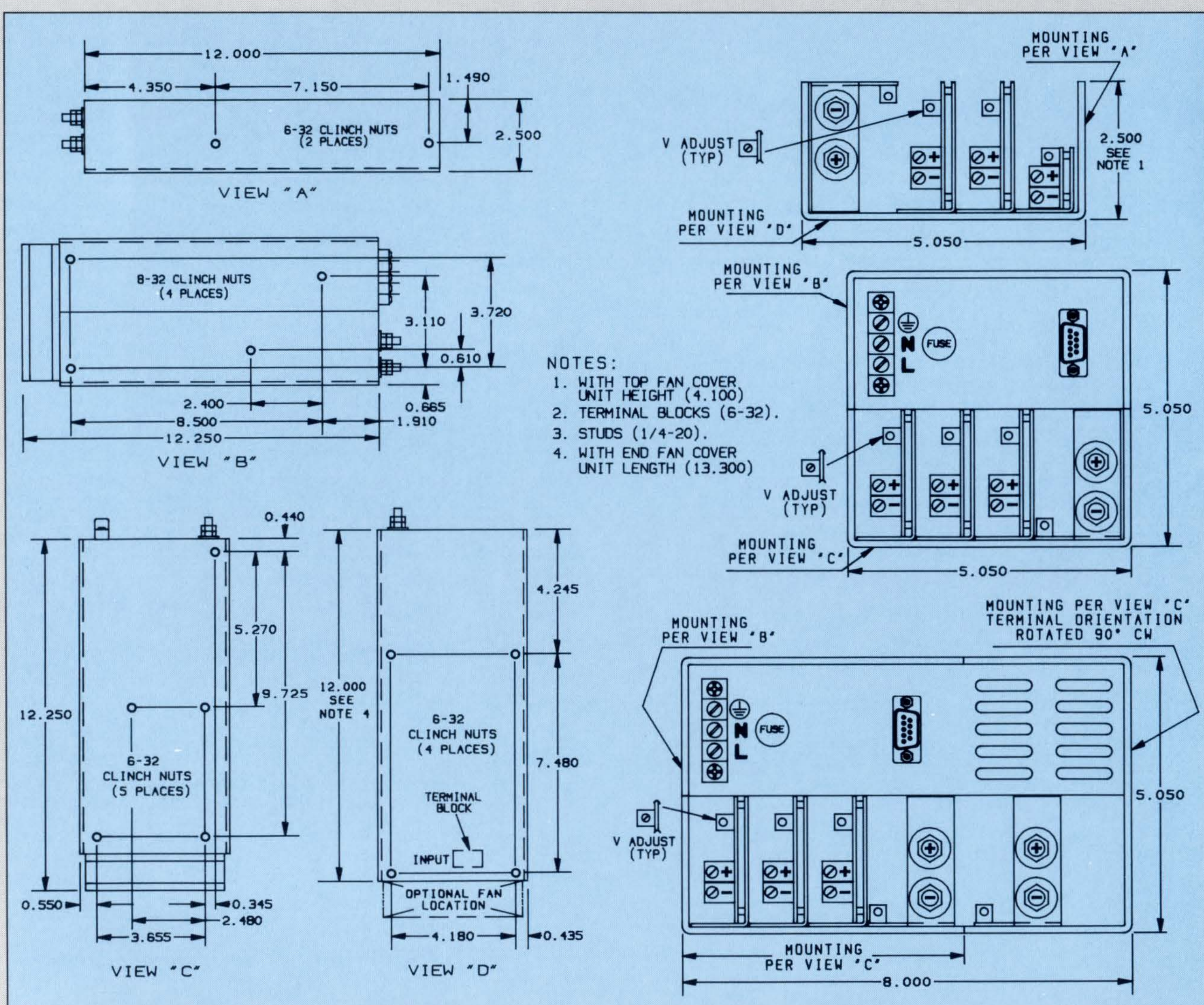
1000 Watt FM Configurations

Config	Top				
11	AC	#1 M7			
21	AC			#2 L	#1 M6
31	AC		#3 L	#2 L	#1 M6
41	AC	#4 G	#3 G	#2 G	#1 M6
43	AC	#4 K	#3 G	#2 G	#1 M6
51	AC	#5 J / #4 J	#3 G	#2 G	#1 M6
61	AC	#5 J / #4 J	#6 J / #3 J	#2 G	#1 M6
71	AC	#5 J / #4 J	#6 J / #3 J	#7 J / #2 J	#1 M6

2000 Watt FM Configurations

Config	Top					
13	AC	#1 M9				
23	AC				#2 M7	#1 M7
33	AC			#3 L	#2 M6	#1 M7
45	AC		#4 L	#3 L	#2 M6	#1 M7
53	AC	#5 G	#4 G	#3 G	#2 M6	#1 M7
55	AC	#5 K	#4 G	#3 G	#2 M6	#1 M7
63	AC	#6 J / #5 J	#4 G	#3 G	#2 M6	#1 M7
73	AC	#6 J / #5 J	#7 J / #4 J	#3 G	#2 M6	#1 M7

FM SERIES DIMENSIONS



DESCRIPTION

Moduflex switchers form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. These subunits and assembly hardware are pre-approved by safety agencies so that certifications can automatically apply to custom models. Additional advantages include first piece delivery within two weeks and the elimination of engineering costs for qualified "OEM" requirements using stock modules.

FM Series are corrected to produce a 0.99 power factor. The resultant input current waveform is nearly a perfect sine wave compliant to the harmonic requirements of IEC 555-2.

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FEATURES

- 0.99 power factor.
- 5 watts per cubic inch.
- 600-2000 watts output.
- 120 kilohertz design.
- TUV/VDE, UL, CSA.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit proof*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*

MODEL SELECTION

Input modules are available in ratings of 600, 1000, and 2000 watts with corresponding code letters of C, E and G. Refer to Power Code Table.

Output modules are available in ten types ranging in nominal power from 75 to 2000 watts. Refer to Output Code Table for codes and nominal power output.

Input Power Codes	
Codes	Watts
C	600
E	1000
G	2000

Output Codes	
Codes	Nominal Power
J	75
K	150
G	300
L	300
M3	400
M4	500
M5	600
M6	750
M7	1000
M9	2000

The Table of Ratings for the various types of output modules lists the maximum current for each type as a function of corresponding voltage rating.

Ratings in the shaded area are Preferred and are stocked for fast delivery.

Note: When computing output load power, multiply the fraction of actual current to max. rated current by the nominal power rating of the output module.

RATINGS OF OUTPUT MODULES

Nominal Power		75W	150W	300W	300W	400W	500W	600W	750W	1000W	2000W
Code	Volts	J	K	G	L	M3	M4	M5	M6	M7	M9
0	2	10	20	20	30	80	100	120	150	200	400
1	3.3	10	20	20	30	80	100	120	150	200	400
2	5	10	20	30	30	80	100	120	150	200	400
3	12	6	12	20	24	34	42	50	62	84	168
4	15	5	10	20	20	26	33	40	50	67	134
5	18	4	8	16	16	22	28	33	42	56	112
6	24	3	6	12	12	17	21	25	31	42	84
7	28	2.5	5	10	10	14	18	21	27	36	72
8	36	2	4	8	8	11	14	17	21	28	56
9	48	1.5	3	6	6	8	10	12	16	21	42

HOW TO ORDER

Select the letter F for power factor correction, then select the letter M to designate the series. Choose the desired configuration of output modules and list the configuration code. Insert the power code letter and follow with the output code numbers for each individual output. Enter a dash and from the option table insert the sum of the option codes. See example below.

F M 41 E 2 3 3 6 – Y

- F — P. F. Corrected
- M — Series
- 41 — Configuration
- E — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- Y — Sum of Option Codes

	OPTIONS
Option Code	Function
1	Power Fail Monitor
2	Cover (600W only)
4	End Fan Cover (600W only)
8	Top Fan Cover (600W only)

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.
190-264 for 2000W units.

POWER FACTOR
0.99 at full load.

HARMONIC CURRENTS
Compliant to IEC 555-2.

INPUT SURGE
230 VAC – 75A max.
115 VAC – 40A max.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table.

ADJUSTABILITY
±5% trim adjustment.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Main output is #1 on 600W and 1000W units and #2 on 2000W units.

REMOTE SENSING
On all outputs except type J modules.

RIPPLE & NOISE
1% or 100mV pk-pk, 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C.- Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS cooling air directed on cooling surfaces over the 600W units for full rating. Two test locations on chassis rated for max. temperature of 90°C. 1000W and 2000W models have built-in ball bearing fan.

TEMPERATURE COEFFICIENT
±0.02%/°C.

EFFICIENCY
70% to 80%.

SAFETY
Units meet UL 1950, CSA 22.2 No. 234, IEC 950, EN 60 950, VDE 0804, VDE 0805, VDE 0806. Certifications in process.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm primary to grounded circuits.

LEAKAGE CURRENT
3.5mA max.

EMISSIONS
Units meet FCC 20780 Part 15 Class A and VDE 0871 Class A for conducted emissions. Compliance with Class B limits by use of additional external filter.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%.
M3, M4, M5, M6, M7, and M9 modules – 200 microseconds.
J, K, G, and L modules – 500 microseconds.

UNDERVOLTAGE
Protects against damage for undervoltage operation.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Auxiliaries have additional backup fuse protection.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

SOFT START
Units have soft start feature to protect critical components.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided.

SHOCK
MIL-STD 810-D Method 516.3, Procedure III.

VIBRATION
MIL-STD 810-D Method 514.3, Category 1, Procedure I.

MECHANICAL
600W – Case 1. – 2.5 x 5.05 x 12
1000W – Case 2. – 5.05 x 5.05 x 12
2000W – Case 3. – 5.05 x 8 x 12

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME compatible power fail signal providing 4 milliseconds warning before main output drops by 5% after an input failure.

FAN COVER
Optional covers with brushless DC ball bearing fan which provides the required air flow for full rating of 600W units. Choice of low profile or top mounted types.

Specifications subject to change without notice.

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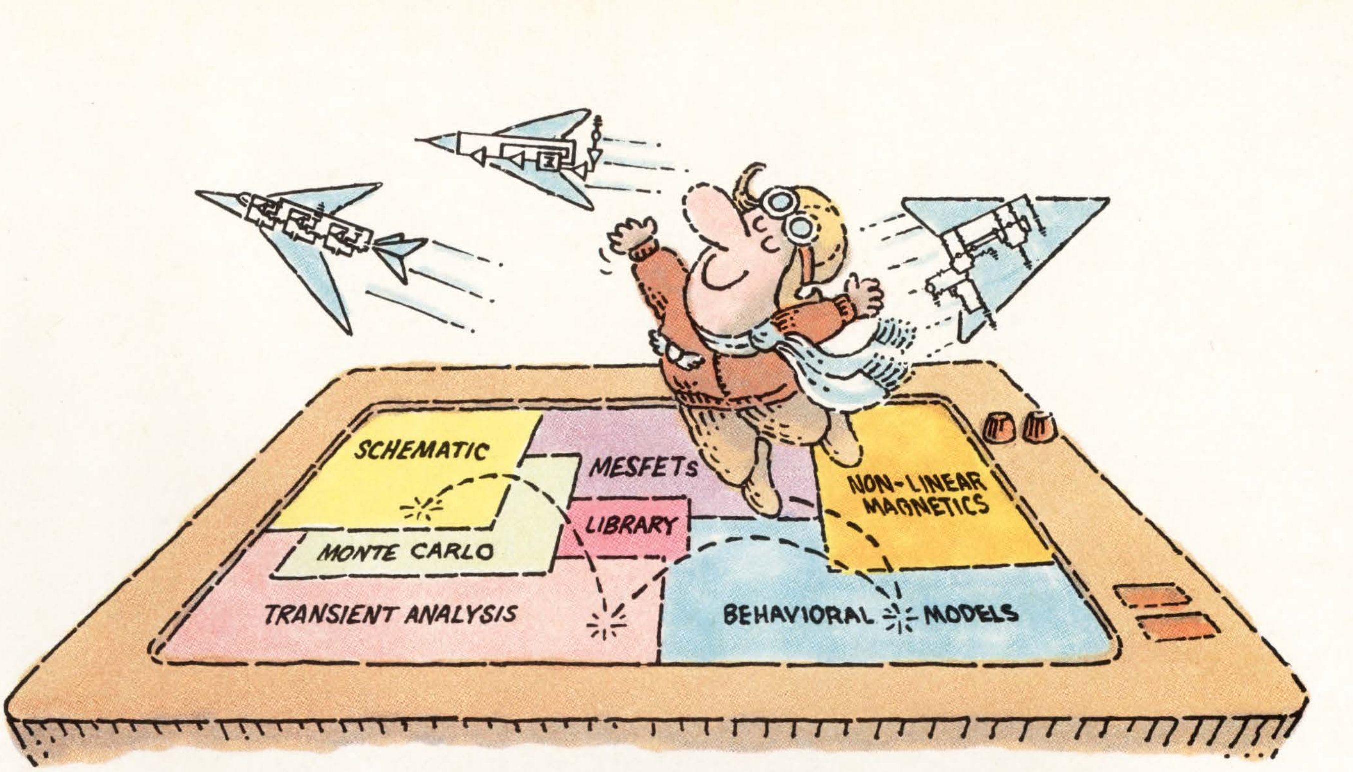

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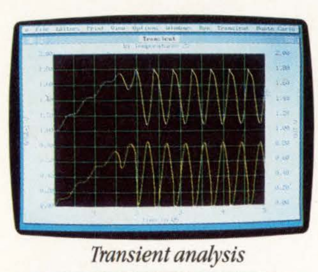
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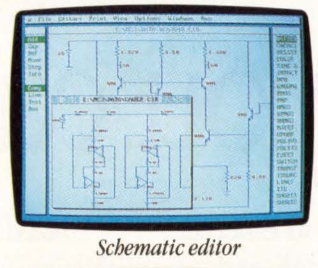
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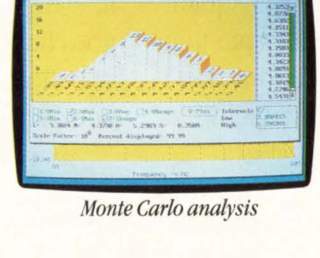
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For unmatched desktop performance, we offer


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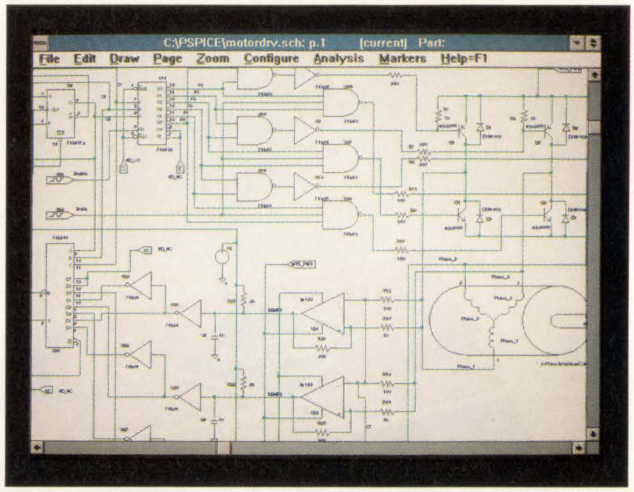
Where would you go to answer all of your analog and digital circuit design questions?



A sensorless brushless DC motor control system is graphically defined using part symbols from our analog and digital libraries, as well as symbols customized for the application.

We brought you PSpice — the world's most popular mixed analog and digital circuit simulator. Now we bring you the **Design Center** — the universal analog and digital circuit design environment! Offering integrated schematic capture, mixed-mode simulation, and graphical waveform analysis, the **Design Center** will take you and your circuit design from conception to realization with ease and efficiency.

Graphically Capture Your Circuit Design

Using the **Design Center**, circuit drawings are simple to create and edit. Select from over 5,700 analog and digital components maintained in our continually expanding device and symbol libraries. Or create your own devices and symbols to suit your individual application.

Run PSpice Simulations Directly from Your Schematic

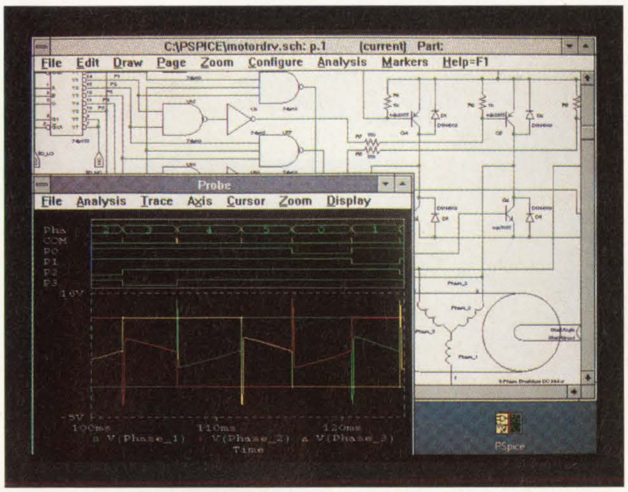
When your circuit drawing is complete, you can initiate PSpice analyses from choices on the pull-down menus. Netlists are generated automatically and can be examined on the screen. The electrical rule checker inspects the electrical connections on your schematic for integrity, before the simulation is run.

Maintain the PSpice Mixed-Mode Simulation Advantage

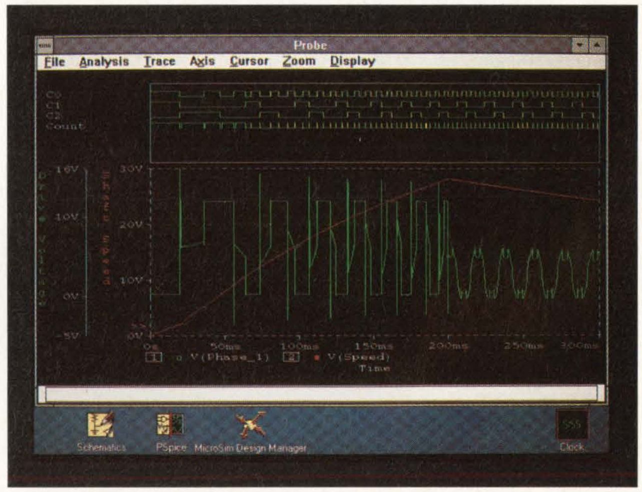
The **Design Center** provides analog-only, mixed analog/digital, and digital-only electrical circuit simulation by integrating the capabilities of our well-known PSpice simulator. With the **Design Center**, these features are standard:

- analog behavioral modeling,
- Monte Carlo and sensitivity/worst-case statistical analyses,
- fully integrated, event-driven digital simulation supporting state, strength, and timing modeling, as well as worst-case timing simulation,
- extensive device libraries containing over 4,000 analog and 1,700 digital devices,
- analog and digital stimulus generation,
- analog device characterization, and
- graphical waveform analysis of simulation results.

THE DESIGN CENTER™!



Using analog behavioral models for the motor, and devices from our analog and digital libraries, the Design Center simulates the closed-loop control system.



The Design Center displays PSpice simulation results for both analog and digital waveforms together on the same plot.

View Waveforms Directly from Your Schematic

Analog waveforms and digital signals can be displayed simultaneously along a common time axis, while remaining within your circuit drawing environment. Simulation results can be interactively viewed in a variety of ways including fast Fourier transforms, derivatives, integrals, user-defined functions, and buses, as well as analog and digital waveform expressions. Performance analysis, multiple Y axes, and flexible plot control are a few of the additional reasons why you'll benefit from graphical waveform analysis.

Choose from Several Configurations

Whether you run on a windows platform, or not, there is a configuration of the **Design Center** for you. Choose our full-featured system with schematic capture, available under Windows 3.0 or OpenWindows. Or choose one of our reduced configurations without schematic capture, available on a variety of platforms; you'll continue to benefit from the **Design Center**'s powerful simulation and analysis features. Whichever configuration you choose, we feel that the **Design Center** provides the most comprehensive system for circuit design available today.

We're Making Mixed Analog and Digital Circuit Design the Standard!

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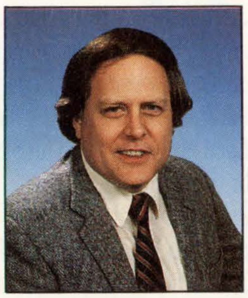
THE MAKERS OF PSPICE

CIRCLE NO. 38

Innovation software stimulates engineering creativity

CHARLES H SMALL, Senior Technical Editor



Personal-computer software can help you hatch new ideas and overcome creative blocks.

A gaggle of inexpensive personal-computer programs is available to help you be more innovative and deal with the stress of today's short design cycles. Some of these programs deliberately force you to think in nonlinear, nonlogical, playful ways. The idea behind them is to divert your thinking from the channels that day-to-day work has forced it into, sparking new ideas and new ways of thinking. Others focus your attention on the psychological aspects of overwork, such as motivation, stress, and depression. These programs are poles apart from logical, mathematical, engineering programs.

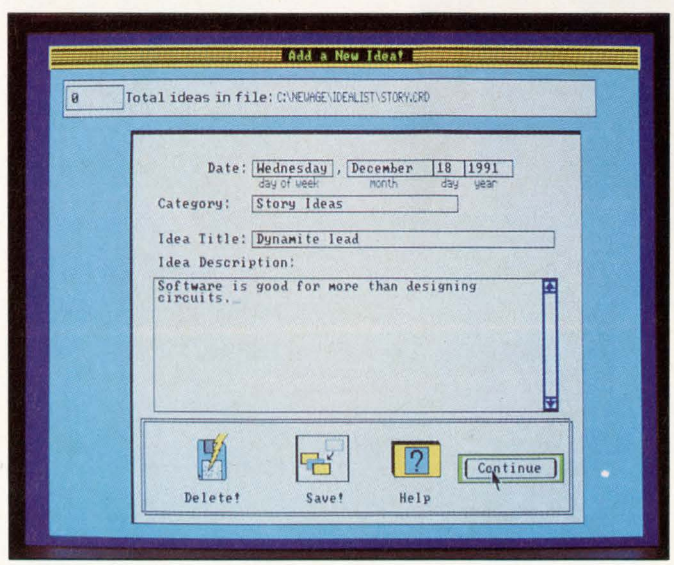
Bold, speculative, even outrageous thinking is the mainspring of innovation. Because logic begins with assumptions, when solutions depend on connections yet to be made, logic must fail. Therefore, activities such as brainstorming can be an important first step in finding new and easier ways to deal with today's crushing workloads. Of course, after brainstorming, you, as a working engineer, must convert your speculation into multiple, affordable experiments.

Speculative innovation and the resulting experiments are worthwhile endeavors even if you do not develop saleable products. As Buckminster Fuller pointed out, "There is no such thing as a failed experiment. Because the outcome is unexpected, the experiment is rich in potential learning. Too often, in the business environment, it is viewed as a 'failure,' to be covered up, swept under the carpet and forgotten as quickly as possible instead of being applauded for its courage and imagination and studied for the new insights it must contain."

Innovational and motivational programs draw on the techniques of itinerant seminar-givers. Instead of paying these folks lots of money to come to your site to conduct their workshops, the following programs let you engage in their drills and use their methods at your convenience.

Innovational programs use one or two general techniques: guided problem-solving and brainstorming. Guided problem-solving supplies frameworks into which you plug your ideas. The main advantage of computerized, guided problem-solving is that the programs will prompt you for your ideas in a thorough manner.

Mountain House Publishing's Ideatree (shareware) is a simple graphics editor for organizing your thoughts into



By providing a database that simulates a stack of 3x5-in. cards, Idealist lets you first capture, and then arrange, your thoughts.

Seagate's Low-Profile 3.5" Drives

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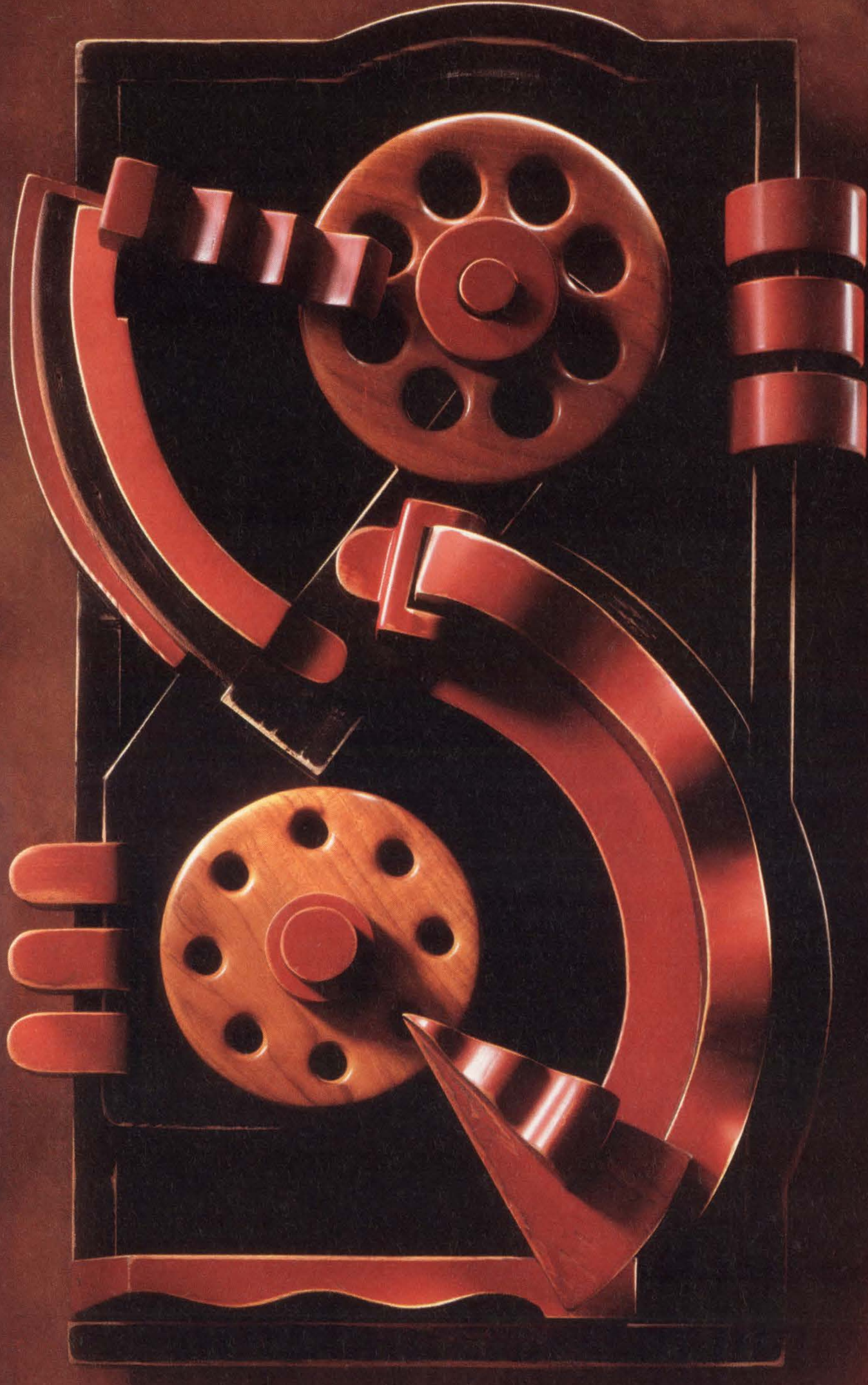

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Seagate's 1" high, 3.5"-inch disc drives—the ST3120, ST3144, ST3283, ST3500 and ST3600—offer performance levels unusual even in full-form-factor drives. These advanced drives are ideal for performance-oriented applications where size, weight and power must be kept to a minimum, such as high-end laptops and portable workstations.

Available in AT, SCSI-2 and Fast SCSI-2 interfaces, the drives combine a 3,600 RPM or 4,500 RPM spindle motor with Zone Bit Recording (ZBR) to offer access times as low as 9.9 msec. Power consumption is from 3.5 to 5 watts, and capacities range from 106 to 525 formatted megabytes.

When creativity and craftsmanship combine, the result is art. For complete product specifications, contact your authorized Seagate distributor or call Seagate directly at 800-468-DISC or 408-438-6550.

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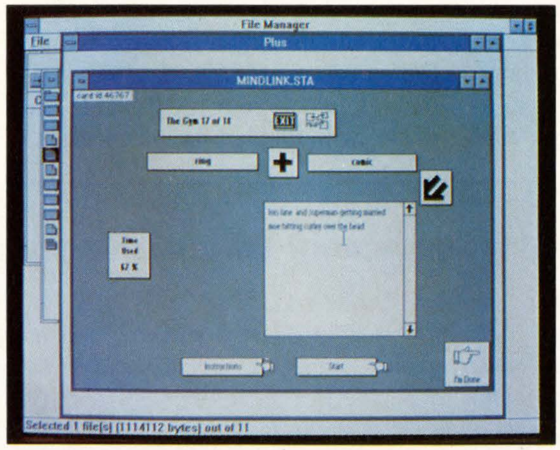
INNOVATION SOFTWARE

little boxes hung from the branches of descending trees. The program lets you build extensive organization charts—ones that are bigger than a single computer screen. Uses range from simply outlining a project to performing a complete top-down decomposition of a design or process.

Michael R Sleeter's Idealist (shareware) is a simple database that you use like a stack of 3×5-in. cards to jot down and sort your ideas. In fact, each database field is fixed in size and will hold about one 3×5-in. card's worth of free-formatted information. After recording all your thoughts, in no particular order, you can search through your "cards," ordering and printing them as you choose. The program has on-line help, a graphical user interface (GUI), and only a few simple commands, trading off the power, flexibility, and complexity of full-blown database programs for ease-of-use. You should be able to operate the program now and then without recourse to a manual.

David L Salahi's Dynamind (shareware) is one of several programs that purport to help you clarify and focus your thinking. It prompts you to fill in screens that identify and prioritize your goals. Once you have clearly defined your situation and your goals, the program helps you generate ideas through a variety of techniques that stimulate creativity and imagination. Finally, it directs you to evaluate your alternatives and choose the best one.



By encouraging you to think in nonlinear, nonlogical, playful ways, innovation programs such as Mindlink divert your thinking from the channels that day-to-day work has forced it into, sparking new ideas and new ways of thinking.

Rosemary West's Creativity Package (shareware) contains, among other things, the Think Thunder brainstorming system. The package also contains a program that randomly assembles "poetry" from lists of words, phrases, and sentence fragments you have previously entered. The brainstorming program proceeds in a similar fashion. In response to prompts from the program, you enter spontaneous thoughts about your design problem. The program then mixes up your responses, hoping that juxtaposing unrelated thoughts will kindle new ideas.

Mindlink's Mindlink ($299) is the most elaborate brainstorming and guided problem-solving program listed here. The program runs under Windows 3.0 or Macintosh and requires 4 Mbytes of memory; the others will all run under DOS. The program combines brainstorming and guided problem-solving.

The program's "gym" gives your creative powers a workout using game-like exercises developed for participants in creativity seminars. In a similar vein, it has an extensive series of screens for guided problem-solving and brainstorming. The program also comes with a copy of Vincent Nolan's "The Innovator's Handbook: The Skills of Innovative Management."

And, in case you find your motivation flagging, Lightning Creative Software's lighthearted Mind Strategies ($129.95) program will

Try program to multiply options

You can get free trial copies of the programs noted as "shareware" from the EDN Electronic Bulletin Board ((617)558-4241,300-9600,N,E,1) or from shareware distributors such as The Software Labs. You can try the shareware out for free, paying a fee only if you like the program. Trying out all the different approaches these programs embody is a good idea because creative people typically have many strategies that they employ when innovating, trying one after the other until they reach their goals.

EDN supports the shareware concept and encourages readers to pay for shareware they adopt; using shareware beyond a reasonable trial period without paying is unethical. The programs noted with a dollar amount, and other creativity software along the lines of the shareware listed, are available from Mindware or directly from the listed programs' authors.

INNOVATION SOFTWARE

juice you up again. Following the precepts of motivational speakers, the program lets you set up short- and long-term goals for personal as well as public success. If you find you are too stressed out, the program will display a relaxing picture for you to contemplate. If you have lost sight of your goals, the program will display an inspirational picture to help you remember just why you are working so hard (a Porsche is one option).

If your motivation is flagging, perhaps your spirits are too. No

Production-oriented management stifles innovation

Think about these two facts for a minute: Engineers are under tremendous pressure to become more "productive." And, according to IEEE salary surveys, engineering salaries have dropped slightly over the last two decades (after adjustment for inflation). In other words, your boss wants you to do more work for less money.

Further, creative engineers, more and more, suffer under management practices developed for rote production work. Shortsightedly, in pursuit of ever-shorter time-to-market intervals, management deprives engineers of the chance to learn new techniques, experiment, play, or—most important—fail.

An engineering manager interviewed for an EDN Special Report on field-programmable gate arrays (FPGAs) exemplified this attitude when he said, "I don't want my engineers using any design software that takes more than an afternoon to learn."

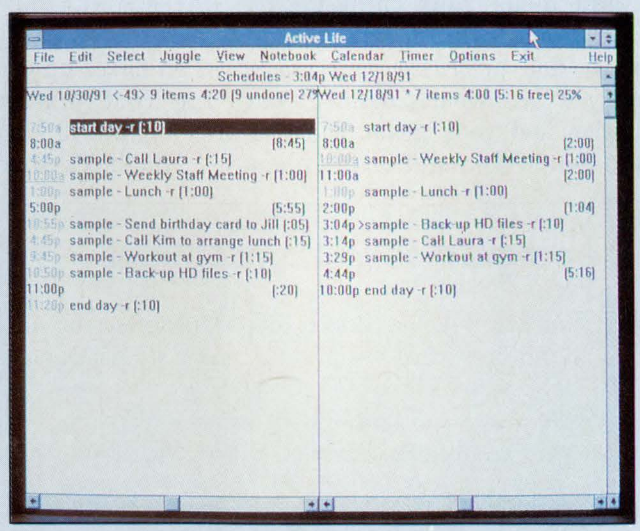
No wonder, then, that engineers express high levels of dissatisfaction with their jobs. Tellingly, in one EDN News survey, one in five engineers would choose another profession if he or she could start over. In another survey, a significant percentage of engineers said that they would not want their children to become engineers. Perhaps these engineers would feel better if their management followed the principle of Apple's John Sculley. "If innovation is our only chance, then only a respect for individual creativity will lead to innovation. We desperately need new tools to help us become more creative."

Software that will help you squeeze every spare second out of your schedule does exist, making your days more like living on a production line. For example, 1Soft, a company specializing in "high-achievement" software, offers scheduling programs for individuals and design teams: Active Life (shareware) and 1 Team ($295). The software not only generates schedules for every minute of every day, it can also warn you that a due date is nigh.

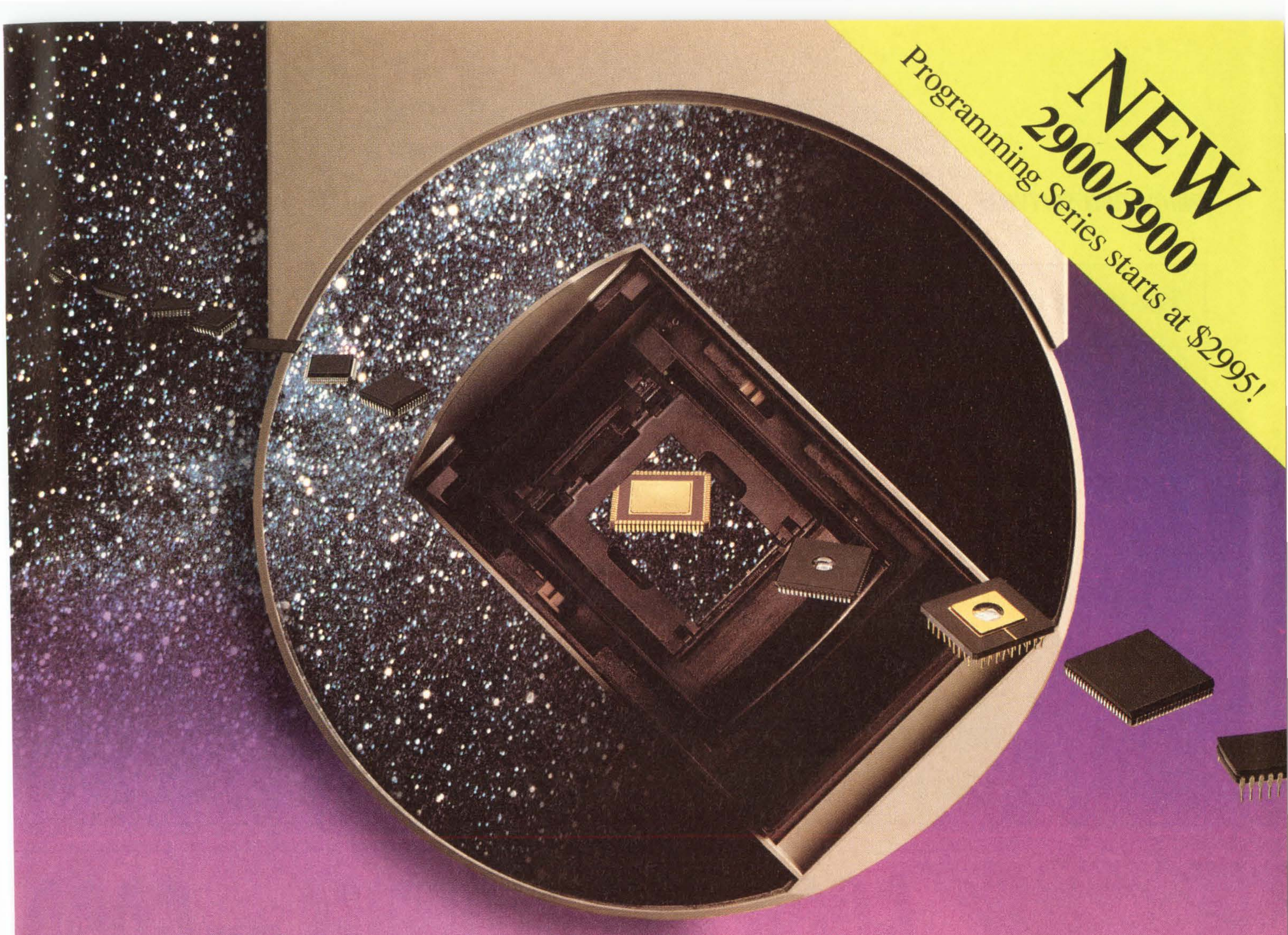
The team version provides the same features for groups. For example, your boss can set up or rearrange your schedule. And secretaries can enter phone messages into your to-do lists for you to follow up on.

Now, if you have to lug a laptop computer around with you 24 hours per day to keep track of your life, you have as much as admitted that you are overworked. To the clamor of your boss's orders, your family's demands, your parents' half-remembered admonitions, and your unfulfilled dreams, you can add constant nagging from your computer. Computerizing this nightmare does offer one advantage: You will have a minute-by-minute record of your descent into burnout. You can while away your spare time, as you recuperate in the rest home, extracting charts and graphs of your accelerating overwork for your therapist's perusal.

Applying the assembly-line philosophy to engineering development yields illusory results in the short run, but proves disastrous to both the company and its engineers in the long run. Simply honing and computerizing existing design methods forces engineers into a production-line-like rut, channelizing their thought processes. Thus, the company that is logical, analytical, orderly, decisive, aggressively single-minded, and *always right the first time*, paradoxically is taking the biggest risk of all: being blindsided by innovators. As Honda's Sichiro Honda said, "There is no success for those who cannot tolerate failure."



With the aid of a computerized appointment book, you can juggle every second of your public and private life, making sure that you are never inactive.



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For more information . . .

For more information on the programs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

1Soft Corp
Box 1320
Middletown, CA 95461
Circle No. 715

Lightning Creative Software Inc
16885 Via Del Campo Ct, Suite 220
San Diego, CA 92127
Circle No. 716

Malibu Artificial Intelligence Works
25307 Malibu Rd
Malibu, CA 90265
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Mindlink Inc
The King's Hwy
Box 247
North Pomfret, VT 05053
(802) 457-2025
Circle No. 718

Mindware
1803 Mission St, Suite 414
Santa Cruz, CA 95060
(800) 447-0477
FAX (408) 429-5302
Circle No. 719

Mountain House Publishing
Ideatree
RR 1, Box 205-8
Waitsfield, VT 05673
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David L Salahi
Dynamind
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Irvine, CA 92720
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doubt about it, today's short design cycles place engineers under terrible stress. Engineers—who would otherwise seek counseling or hire itinerant seminar-givers—could use personal-computer, self-help programs to overcome stress and depression to become more innovative.

One advantage of these personal-computer programs is that you can use them at home without leaving any record in your personnel or medical files. In fact, if your work involves a personal computer, you could engage in surreptitious, self-inflicted brainstorming or therapy on the job, fooling others into thinking you are actually working.

The 6-Step Stress Management System is a program from Self-Health Systems (shareware). The program guides you through assessing your stress levels, identifying the "stressors" in your life, learning relaxation skills, and charting your progress (or lack thereof) in overcoming stress. The program also assists you in preparing your own audio cassette tapes for relaxation.

Long periods of unremitting stress, among many other causes, can lead to depression. Figures from the National Institute of Health indicate that one-quarter of all people experience a significant bout of depression in their lives. In any given month, more than 1 in 20 of us are depressed.

Overcoming Depression, a program from the Malibu Artificial Intelligence Works ($195), is an artificial-intelligence program tailored to personal computers that simulates interactions between you and your therapist. The program is the result of a collaboration between programmers and therapists. The program records your sessions with the "therapist" so that you can study them later. It also provides constructive advice on psychology, antidepression drugs, and suicide prevention. EDN

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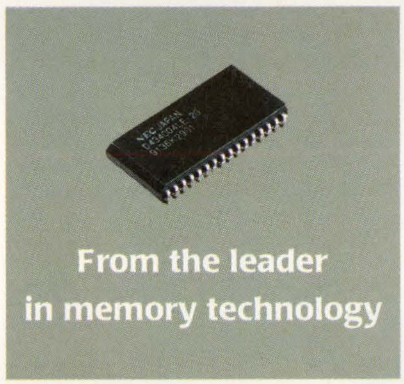

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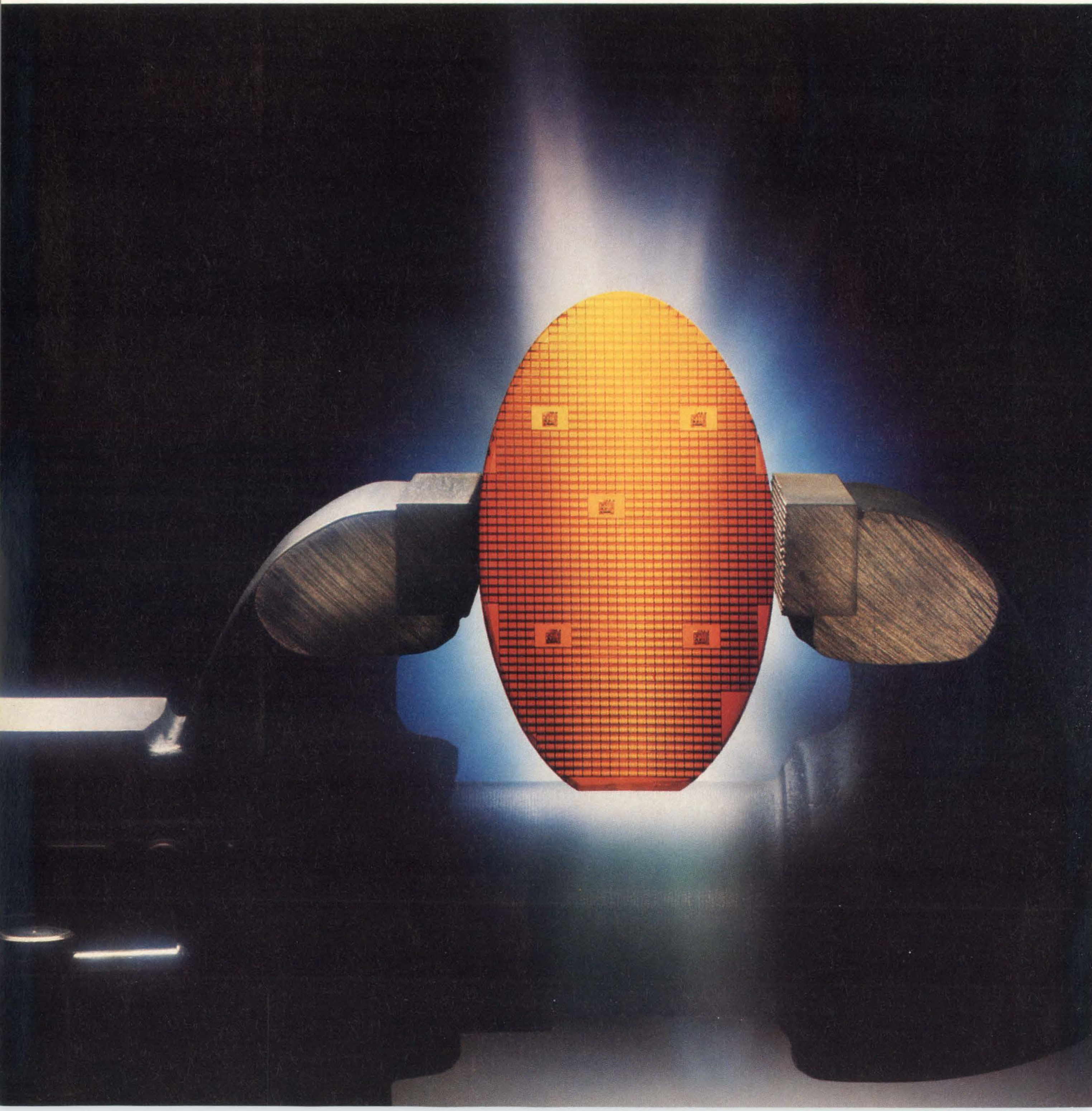

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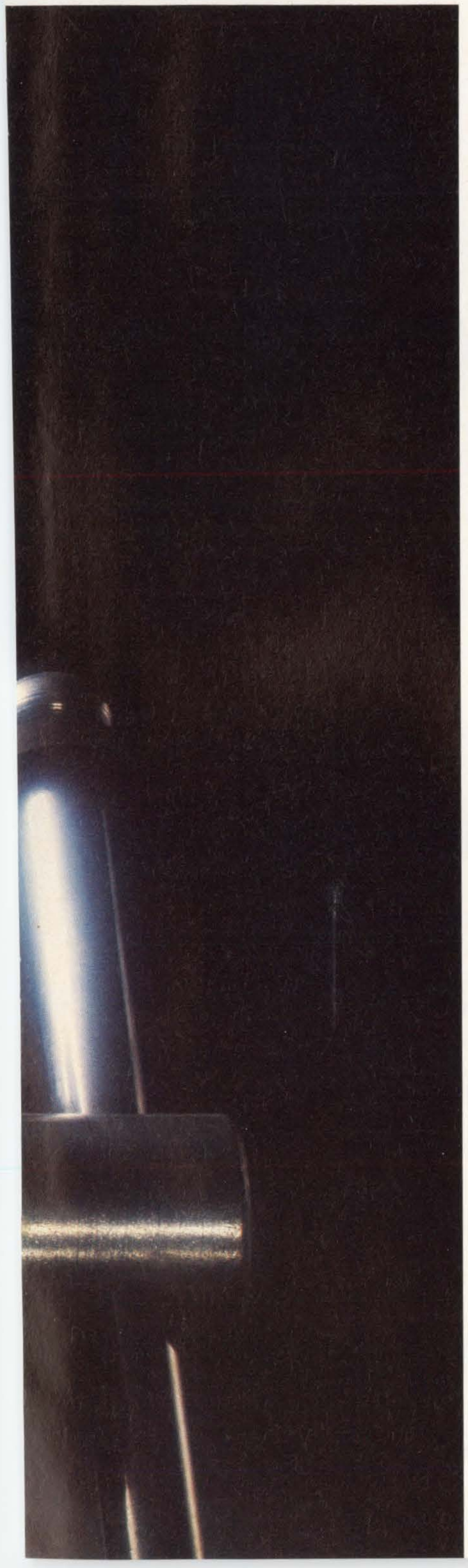

With our new Advanced BiCMOS interface logic (ABT) family, you get the speed, drive and low power you need to optimize the performance of processors operating at 33 MHz and above.

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As in our successful Advanced CMOS Logic (ACL) Widebus family, these devices come in our leadership surface-mount shrink small-outline package (SSOP) that gives you twice the number of I/Os as a standard small-outline package in the same space.

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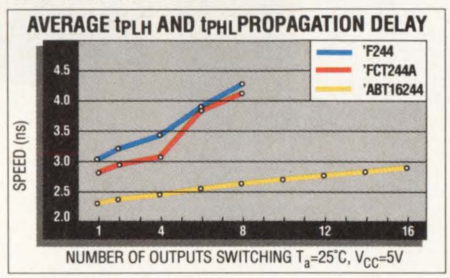

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To complement our full line of Widebus products, our ABT family will include at least 39 octal buffers/drivers, flip-flops, transceivers and registered transceivers.

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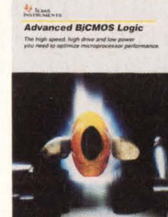
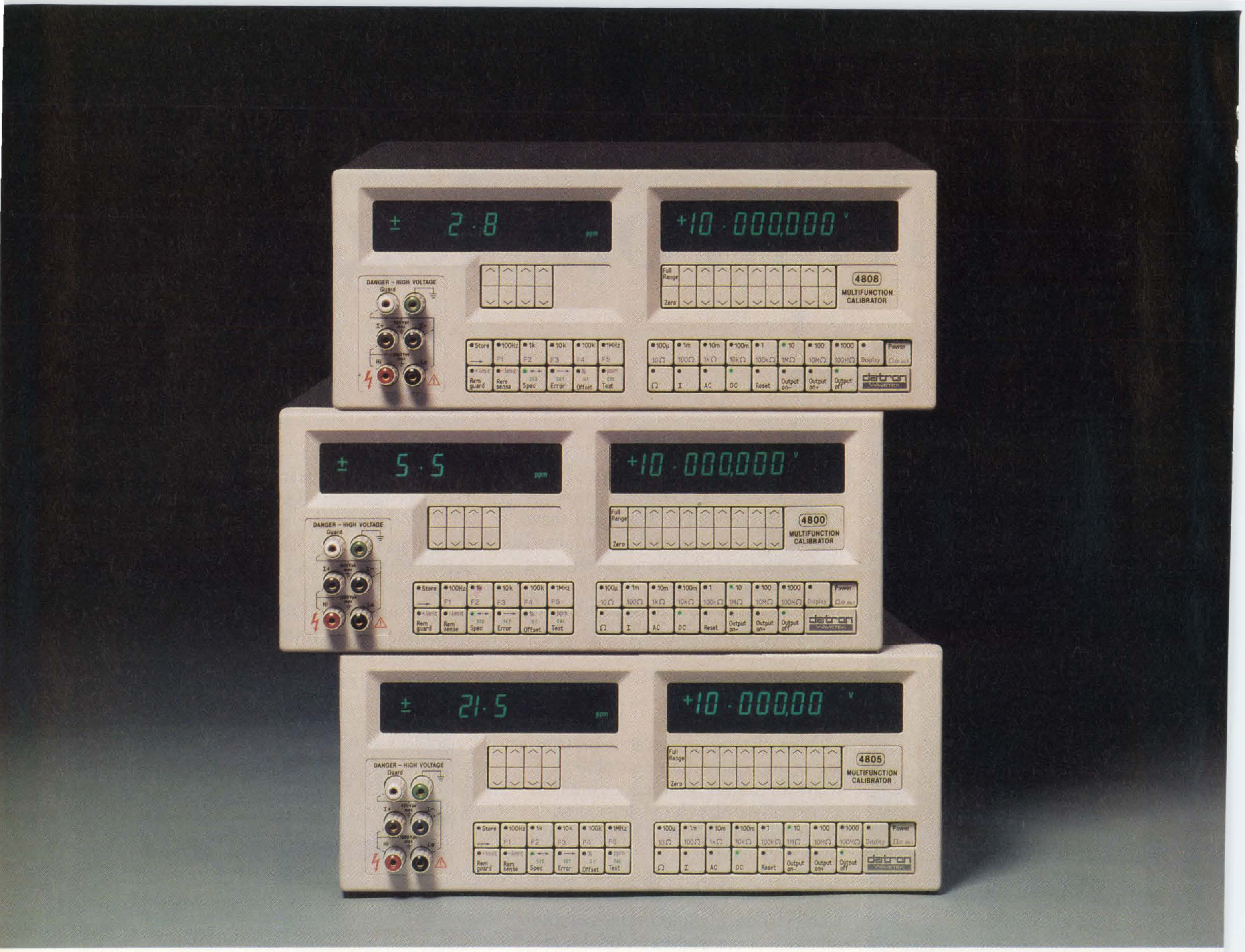
To learn firsthand how our new ABT family can boost the performance of your bus-interface designs, get a free 'ABT16500A transceiver and data sheet. Just complete and mail the return card or call the number above.



TEXAS INSTRUMENTS



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datron WAVETEK

Trio of software tools tailors MS-Windows to test applications

If you use an MS-DOS PC to develop and run test applications, Hewlett-Packard figures that sooner or later—probably sooner—you're going to be doing your development and running your programs under MS-Windows V3.0 or higher. Therefore, the firm is announcing a trio of Windows-based test-development packages.

Of the three latest offerings, Instrument Basic for Windows provides the best place for neophyte test programmers to get started. The language is designed for engineers and scientists who want to write their own test software to run under Windows. (Despite Basic's reputation as a beginner's language—Basic stands for *Beginners'* all-purpose symbolic instruction code—HP claims that test engineers still program as many test applications in Basic as in all other languages combined.)

Graphics displays that appear in windows while you develop and debug your test program are just one of the features of Instrument Basic for Windows. The language is one of three packages the vendor is targeting at test engineers who use MS-DOS-based PCs to develop and run test applications.

This Basic is interpreted, preserving the language's interactive flavor, and is much more test oriented than other Windows languages. Unlike earlier versions of HP Instrument Basic, the Windows version runs on 80x86-based PCs *without* a 680x0-based coprocessor board.

ITG II is a tool for programmers looking for assistance in creating Windows-based test programs. It doesn't allow you to program solely by creating, interconnecting, and manipulating icons. (Last year, for people totally averse to text-based programming, the vendor introduced a workstation-based package called VEE that lets you control instruments and data solely by working with icons.)

ITG II targets test engineers with programming experience who will find the graphics-based features handy for generating code segments in several languages. But text-based code will still be needed for linking the segments, which themselves are text based, into working applications. ITG II is the successor to the vendor's earlier ITG/DOS, a package that does not support MS-Windows.

One of ITG II's new features is a driver-writing tool. Although you cannot use the tool for writing complex instrument drivers, you can use it to rapidly write drivers that control an instrument's most-often-used functions. You write the drivers by following a structured question-and-answer process that is embedded in the tool.

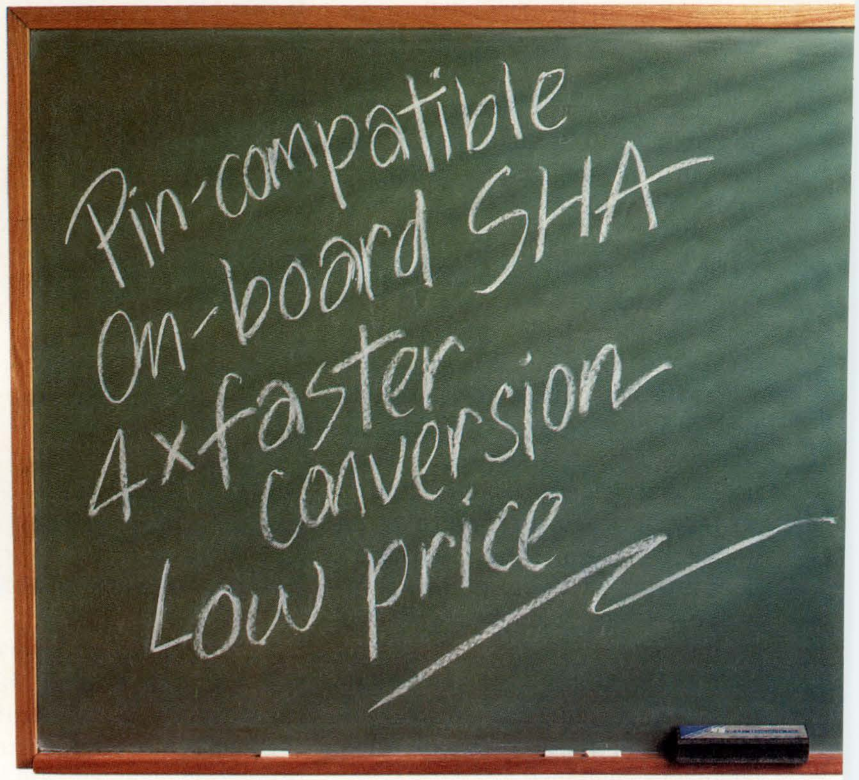
The vendor characterizes the third package, HP-IB for Windows and DOS, as a safety net for DOS/Windows programmers who are working with Windows-compatible languages and applications and want to control IEEE-488 instruments. In other words, if you are using a language that doesn't handle instrument control, you can enhance this language with the instrument-control functions you need by using HP-IB for Windows and DOS. If, instead of a language, you are using a Windows application, such as Excel, and you want to do instrument control and data acquisition from your spreadsheet, this Windows and DOS package will allow you to do the job.

HP E2200A, Instrument Basic for Windows, costs \$395; HP E2020B, ITG II, including a library of 220 instrument drivers, costs \$1495. HP 82335B, HP-IB for Windows and DOS, including an ISA bus IEEE-488 interface card, costs \$525.—**Dan Strassberg**

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900 for information; (800) 452-4844 for orders.

Circle No. 730

For everyone who's tried to copy our AD574, here's your assignment for the next ten years.



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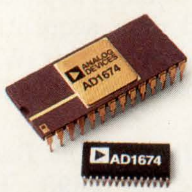
As a member of our AD574 family, the pin-compatible AD1674 offers designers unparalleled performance and integration. With the added benefits of an on-chip sample/hold amplifier, DC and AC guaranteed specs, faster throughput, and a list of other features too long to mention here.



The AD1674 retains the pinout and functionality of the AD574, AD674 and AD774, while integrating a high-bandwidth sample/hold circuit, higher speed, lower power, and lower price – from $14.15 (suggested, 100s). The AD1674 accepts input signals of ±5V, ±10V, 0–10V or 0–20V, while operating from its standard 10V on-chip voltage reference (available for driving external loads).

In other words, the AD1674 redefines 'industry standard' the same way the AD574 did ten years ago.

Why wait for an imitation when you can have the real thing now? Get more information today on the AD1674, AD574, AD674 or AD774 converter family by writing to us at the address below. Or by calling 1-800-262-5643.

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CIRCLE NO. 46

EPLD combines 80-MHz counter rate with 256 logic cells and 164 I/Os

Logic designers carve out their creations under tight constraints, limited by logic delays, interconnection costs, and available I/O pins. They can, however, use the Altera MAX 7000 series EPLDs (erasable programmable logic devices) to gain some sorely needed design elbow room. The top-of-the-line EPM7032 brings together an 83.3-MHz (f_{CNT}) counter clock rate, with 256 logic macrocells, special shared logic-expander terms, a fixed cell-to-cell signal delay of 3 nsec, and 164 I/O pins. Logic delay for a signal, coming on chip through a gate to a flip-flop, is 12 nsec (t_{PD}).

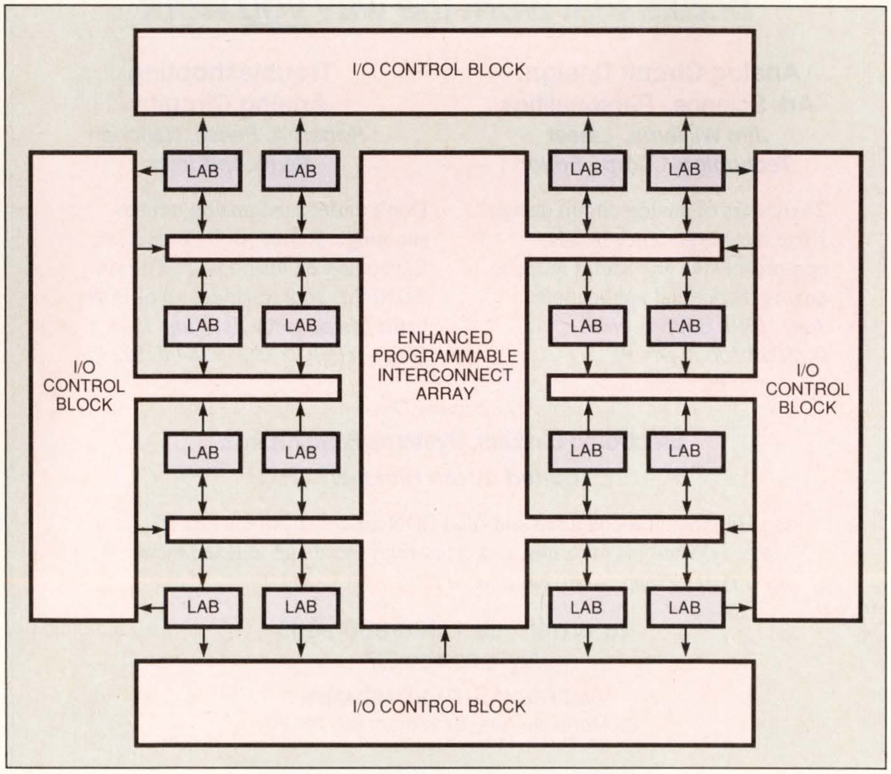
Engineers can build designs from the logic macrocells using expander terms to widen logic product terms. The company furnishes a comprehensive macro design library of SSI and MSI parts that are mapped onto the MAX macrocells from the earlier MAX 5000 line. The MAX 7000 series supports faster clocks, a minimized intercell delay to 3 nsec, and higher I/O pin counts. In addition, for the first time the MAX programmable logic is available in an electrically erasable PLD (EEPLD).

The first two members of the MAX 7000 family are the EPM7256GC192, a 10,000-gate EPLD with 192 I/Os; and the EPM7032LC44, a 1250-gate EEPLD with 36 I/Os (4 dedicated inputs). Most applications can use approximately 50% of these gates. Future chips will push to 300 pins and 20,000 usable gates.

The MAX family sits in the middle of the large-scale programmable logic world. On one hand, RAM-based FPGAs (field-programmable gate arrays), like Xilinx's, have an array of logic cells that are programmed by setting underlying RAM control bits. This RAM controls each cell as well as on-chip interconnects. On the other hand, antifuse FPGAs modeled after gate arrays have an array of cells with one-time-programmable interconnects. Vendors such as Actel, Quicklogic, and Crosspoint use low-impedance antifuses to program macrocell interconnects. MAX EPLDs are reprogrammable, but they must be taken out of the system to do so.

Altera's approach to complex FPGAs is to build fixed hierarchies of macrocells. For example, the EMP7032 has 256 macro or logic cells. These cells are ordered into logic array blocks. An EPM7256 has 16 logic blocks, each with 16 macrocells. Each logic block is like a mini PAL—the macrocells share a logic array or bus of signals. These signals are routed to an individual cell input term by programming its EPROM connection bit, just like a PAL. Each macrocell logic input acts as an implicit AND gate with multiple product terms. Thus, you can build fairly complex logic using a simple macrocell.

However, the MAX EPLDs differ from PALs in that Altera engineers added a programmable interconnect array for linking signals between logic blocks. This array is



With this EPLD architecture, intercell signal delays are held to 3 nsec. Using the MAX 7000 series, you can build complex logic without worrying about unconstrained routing delays.

laid out so routing delays between any two logic-block signals remain constant at 3 nsec. This tactic eliminates the routing problems that many designers experience with other FPGAs, where timing depends on efficient routing. MAX timing delays are fixed, with perhaps higher delays than an efficiently routed FPGA layout.

To increase potential logic complexity, Altera engineers added expander product terms to the logic blocks. These are unallocated AND gates that can be programmed and shared by the logic-block macrocells. With expanders, designers can fit as many as 76 product terms into a single macrocell using one additional logic level of delay.

The MAX7000 macrocell is a simple logic block. It consists of a product term-select matrix (5 PAL-like AND gates) with simple logic ORed and the result fed to a flip-flop or directly out. Without expanders, a macrocell takes as many as 32 product terms. The logic handles D, T, JK, and SR flip-flops. Global clocks, clears, and output enables are also provided.

The company's development software, MAX+PLUS II, is for the MAX programmable logic and runs on a PC under Windows 3.0. This tool set includes a graphic schematic editor, a text editor, a waveform editor, and a logic simulator for testing designs. It includes Altera's Hardware Description Language for textually defining designs such as state machines. The system also provides a tool for partitioning large designs into multiple chips.

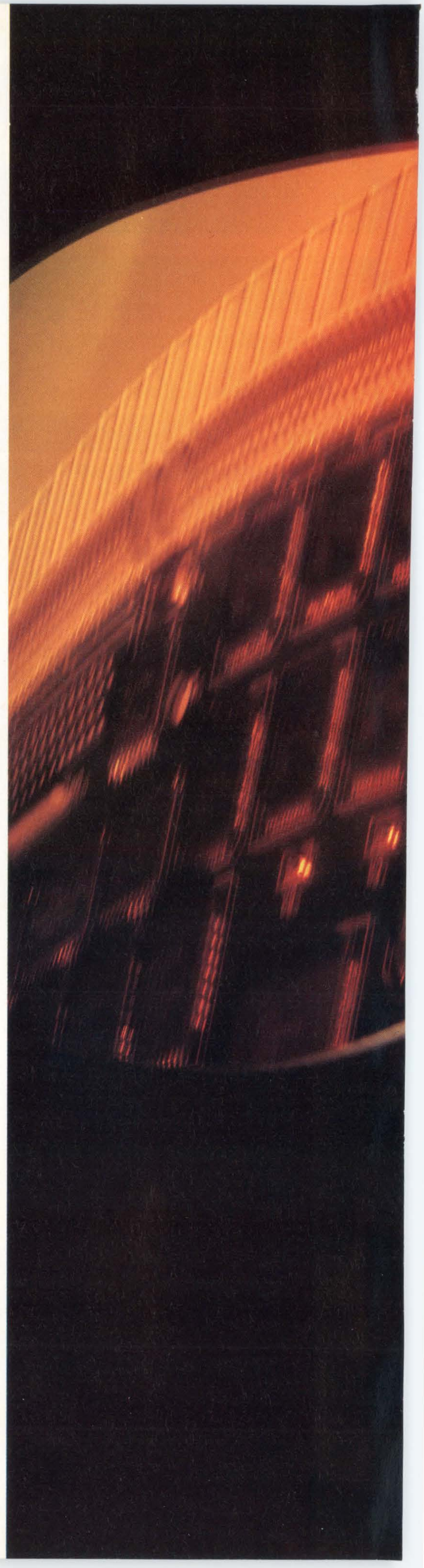
The 192-pin pin-grid-array EPM-7256GC192 costs $395 (single qty). The 44-lead plastic-leaded-chip-carrier EPM7032LC44 costs $14.75 (100).—**Ray Weiss**

Altera Corp, 2610 Orchard Pkwy, San Jose, CA 95134. Phone (408) 984-2800. FAX (408) 248-7097.

Circle No. 731

Bus-driver ICs

Richard A Quinnell, Technical Editor



As ASICs and programmable logic sweep up most discrete logic, bus-driver ICs are becoming the bulk of standard logic products and the focus of manufacturers' attention. Manufacturers have tamed ground bounce and are now boosting bus-driver performance and adding capabilities such as built-in logic.

Bus-driver ICs are so common in circuit design they tend to get ignored, so you probably haven't noticed that they've gotten a lot quieter lately. Bus-driver manufacturers have successfully attacked the problem of device-generated noise with a combination of circuit-design and packaging techniques. The knowledge gained, together with process-technology advances, has let manufacturers broaden their range of bus-driver products and make bus drivers that are faster, quieter, and have more drive than those available three years ago.

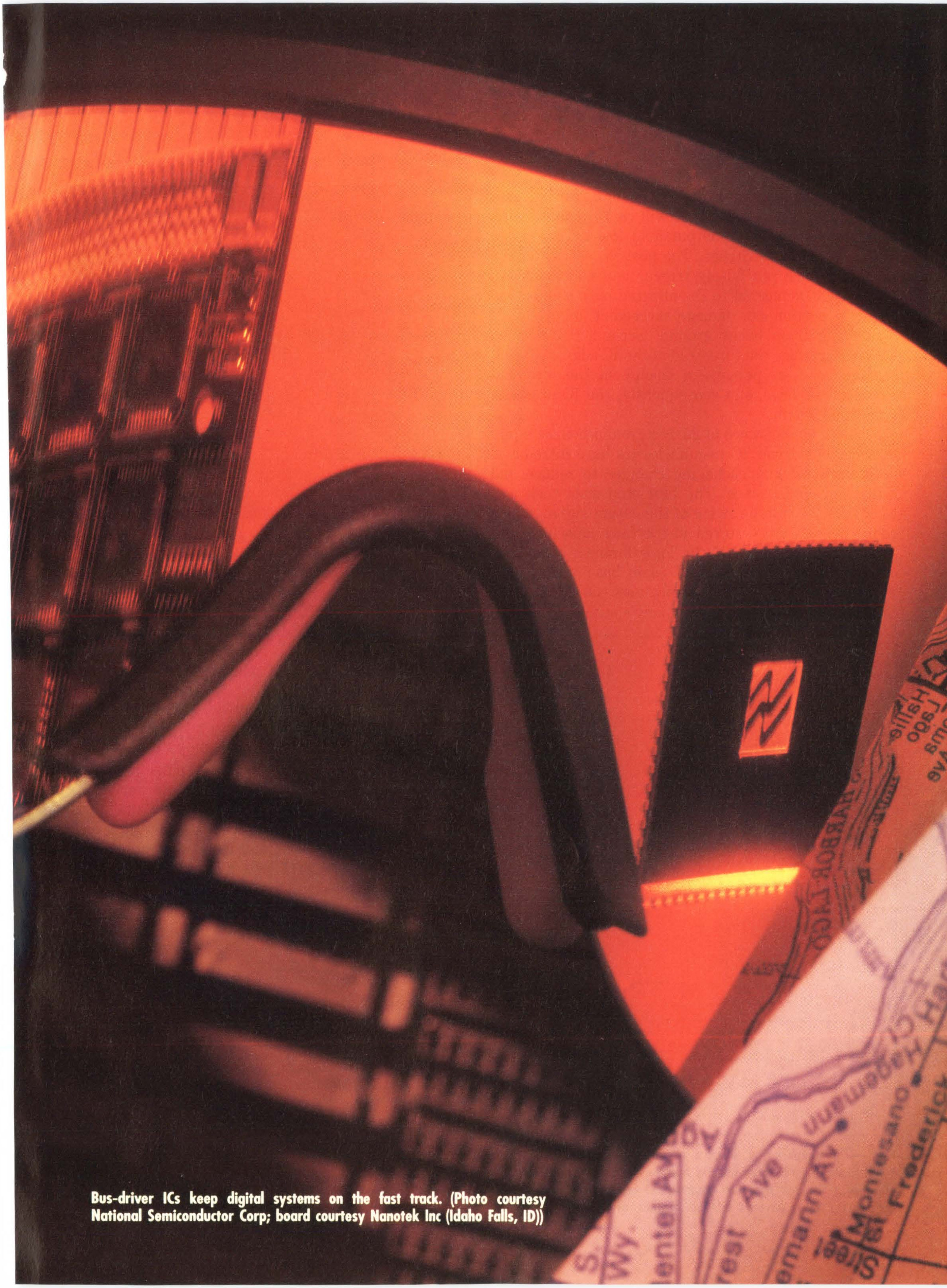
Device-induced noise first became a major bus-driver issue with the introduction of high-speed CMOS logic in the mid 80s. IC families such as Harris Semiconductors' and National Semiconductors' ACT, Integrated Device Technology's FCT, and Texas Instruments' AC series suffered to such a degree that EDN devoted several articles to addressing the problem (**Refs** 1 to 3), culminating in its own testing program (**Ref** 4).

The noise source of greatest concern was ground bounce, also known as simultaneous switching noise. **Fig 1** shows a simplified output-circuit model that helps explain ground bounce. The model is too simple for circuit simulation; fortunately, most manufacturers provide Spice models of their ICs for ground-bounce prediction.

As the model shows, when an output stage switches to logic low, it discharges load capacitance C_L through the lead inductance of the IC's ground pin. The induced voltage, in this model given by

$$V_L = -LC \times d^2V/dt^2,$$

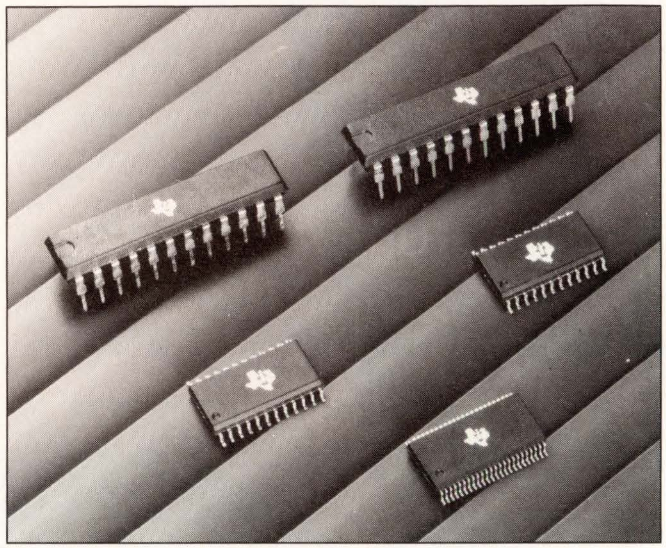
shifts the reference voltage seen by the IC's transistors relative to system ground.



Bus-driver ICs keep digital systems on the fast track. (Photo courtesy National Semiconductor Corp; board courtesy Nanotek Inc (Idaho Falls, ID))

The induced voltage, if great enough, can affect a circuit in two ways. First, it will cause a fluctuation (ground bounce) in an output held low by one stage as another stage switches. The positive portion of the ground bounce can falsely trigger any edge-sensitive input stage connected to the affected output line. The negative portion can damage succeeding input stages by driving them below ground. Second, the induced voltage can raise the threshold of the IC's input stages, causing them to perceive a change in the incoming signal's logic level, and consequently, the IC produces an output glitch.

Since the appearance of EDN's ground-bounce study in 1989, bus-driver IC manufacturers have introduced several circuit and packaging changes to reduce and control ground bounce. The first step most took was to reduce the voltage swing of the output signal, which reduces the energy stored in the load capacitors. As **Table 1** shows, most of the logic families have TTL output swings regardless of their base technology. IDT's FCT-T family, for example, uses the same CMOS process technology as the company's earlier FCT family but doesn't have the rail-to-rail swing usually characteristic of CMOS logic. By limiting the V_{OH}, IDT was able to reduce FCT-T ground-bounce noise as much as 40% from the FCT family's levels.



Bus-driver ICs are becoming denser and are migrating to smaller packages. Both trends combine to reduce ground bounce and increase the number of available channels per IC.

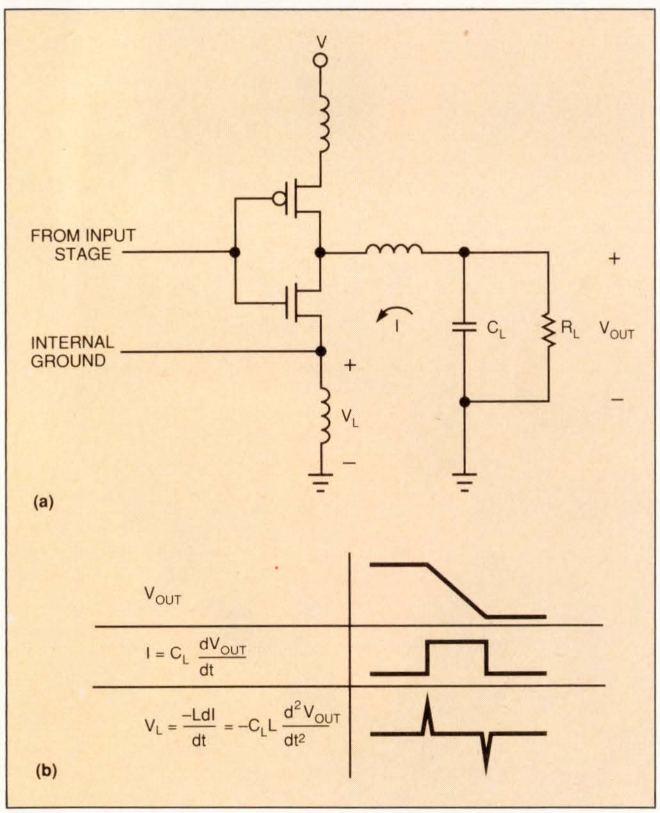


Fig 1—This simplified model of a bus-driver output stage (a) gives insight into the cause of ground bounce. As the load capacitance discharges through the IC's ground-lead inductance, the induced voltage shifts the device's internal ground reference (b).

Controlling turn-on reduces noise

Another step many bus-driver-IC manufacturers have taken is to control the output stage's turn-on rate. The magnitude of the ground-bounce pulse is proportional to the output signal's second time derivative. Implementing a gradual turn-on reduces the initial ground-bounce pulse, which is the one that adversely affects logic levels. Manufacturers accomplish this gradual turn-on in CMOS logic by using the circuit in **Fig 2.** The control-signal line first activates Q_1, a rela-

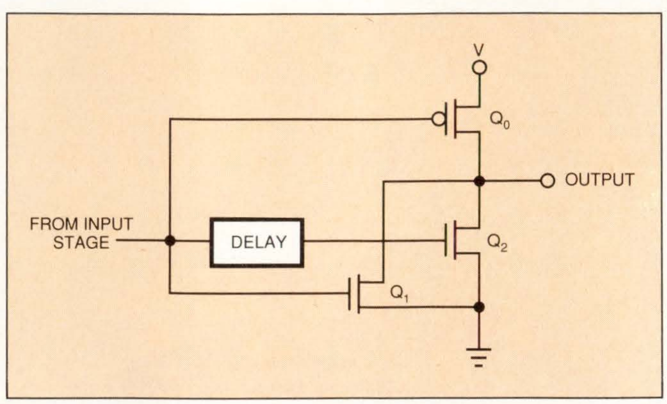


Fig 2—Controlling the output stage's turn-on rate is one technique for reducing ground bounce. For CMOS circuits, activating two transistors in succession yields a gradual turn-on.

tively small transistor with limited current-handling capability. Following a brief delay, the control signal activates the larger Q_2, which provides most of the output stage's current-handling capability.

In addition to circuit changes, manufacturers have reduced ground bounce by making packaging changes. The most obvious change has been a move to surface-mount packages. Surface-mount packages exhibit lower lead inductance than DIP packages, hence less ground bounce. Another change is that manufacturers have added ground pins to DIPs. The Texas Instruments 74ACT16xxx parts, for example, have eight ground and four power leads. Some DIPs also have a redesigned lead frame. Both National Semiconductor and Philips/Signetics have altered the IC's internal lead-frame construction as **Fig 3** shows. The additional ground finger lets the companies reduce chip-to-lead inductance by using two ground bond wires in parallel.

National Semiconductor provides separate ground references for the input and output stages of ACTQ series parts (**Fig 4**). Because the chip-to-lead inductance on the input side's ground helps isolate the input reference from the output reference, the input stage sees reduced ground bounce. National Semiconductor uses the input ground as a quiet on-chip reference. This reference lets the IC detect ground bounce and

Table 1—Bus-driver-IC families

Manufacturer	Family	Number of channels	Propagation delay (nsec)	I_{OL} (mA) (sink)	I_{OH} (mA) (source)	V_{OH} (min)	V_{OL} (max)	I_{CC} (mA) (high Z)	Package styles	Price (100)	Notes
Harris Semiconductor	CD74FCTxxx	8	6.5	64	15	2.4	0.55	0.08	DIP, SOP	$0.95	No I/O clamp diode to V_{CC}.
	CD74FCTxxxAT	8	5.3	64	15	2.4	0.55	0.08	DIP, SOP	$1.55	No I/O clamp diode to V_{CC}.
Hitachi America Ltd	HD74ACQxxx	8	5.0	24	24	4.4	0.1	0.08	DIP, QFP	$0.72	
	HD74ACTQxxx	8	5.0	24	24	4.4	0.1	0.08	DIP, QFP	$0.73	
	HD74BCxxx	8	4.5	64	0.5	2.4	0.6	0.5	DIP, QFP	$0.80	
Integrated Device Technology	74FCTxxxCT	8	4.1	64	15	2.4	0.55	1.5	DIP, SOIC, SSOP, LCC	$4	
	FCT16xxxCT	16	4.1	64	32	2.4	0.55	0.1	SSOP	$8	
	162xxxCT	16	4.1	24	24	2.4	0.55	0.1	SSOP	$8	25Ω series resistor.
	163xxx	16	4.8	24	8	2.4	0.5	0.1	SSOP	$3	3.3V supply.
National Semiconductor Corp	74ACTQxxx	8	7.0	24	24	3.76	0.44	0.08	DIP, SOIC	$1.62	
	74BCTxxx	8	5.5	64	15	2.4	0.55	9	DIP, SOIC	$1.62	
	74BCT2xxx	8	6.7	15	15	2.4	0.55	9	DIP, SOIC	$2.07	25Ω series resistor.
	74FRxxx	8	3.9	64	15	2.4	0.55	50	DIP, SOIC	$2.36	
	74FR16xxx	16	4.3	64	15	2.4	0.55	50	PLCC, SSOP	$4.71	
Philips Components/ Signetics	74ABTxxx	8	2.9	64	32	2.5	0.55	0.05	DIP, SOL	$1.83	
	MB2xxx	16	2.9	64	32	2.5	0.55	0.1	PQFP	$5.63	
Quality Semiconductor Inc	QSFCTxxxT	8	3.8	64	15	2.4	0.8	1.5	DIP, ZIP, SOIC, QSOP	$5.21	
	QSFCT2xxxT	8	4.1	12	15	2.4	0.8	1.5	DIP, ZIP, SOIC, QSOP	$3.37	25Ω series resistor.
Texas Instruments	SN74ABTxxx	8	4.6	64	32	2.0	0.55	0.05	DIP, SOIC, SSOP	$1.80	
	SN74ABT2xxx	8	5.5	12	12	2.0	0.55	0.05	DIP, SOIC, SSOP, TSOP	$2.20	26Ω series resistor.
	SN74ABT16xxx	16	9.5	24	24	3.7	0.44	2	SSOP	$3.50	
	SN74ABT16500	18	4.6	64	32	2.0	0.55	3	SSOP	$10.80	Universal bus-transceiver design.
	SN74ABT32500	36	5.0	64	32	2.0	0.55	4	SQFP	$19.80	Similar to 16500. Holds last output when bus goes to high impedance.
	SN74ACT16xxx	16	4.1	64	32	2.0	0.55	0.08	SSOP	$4.50	Demand-based power-reduction circuitry.
	SN74BCT25xxx	8	6.0	188	80	2.0	0.55	11	DIP, SOIC	$3.75	
Toshiba America Electronic Components Inc	74ABTxxx	8	3.0	64	15	2.4	0.55	0.05	SOIC	$2.20	
	74BCxxx	8	4.2	48	15	2.7	0.55	0.05	DIP, SOIC	$1.87	

Notes: 1. Parameters listed are for –244 type buffer in each family.
2. PLCC=plastic leadless chip carrier, PQFP=plastic quad flatpack, QFP=quad flatpack, SOP=small-outline package, SQFP=shrink quad flatpack, SSOP=shrink small-outline package, TSOP=thin small-outline package, ZIP=zig-zag in-line package.

take corrective action. In the ACTQ series, the chip's response is to inject current into the affected output circuits to reduce the negative ground-bounce pulse.

Forgotten but not gone

Given all the techniques manufacturers have devised to reduce ground bounce, you might be tempted to conclude that ground bounce is no longer a concern for bus-driver ICs. However, manufacturers have only controlled ground bounce, not eliminated it. Such noise will continue to exist in high-speed systems and has joined propagation delay and power consumption as factors bus-driver IC manufacturers must trade off in their designs.

What each manufacturer has done is chosen a voltage limit for ground bounce in its parts—a value it feels will relieve designers from the need to address ground bounce specifically in their designs. With today's parts, then, using ground planes and power-supply decoupling should keep ground bounce from affecting your system's operation. If your system has noise sources that might gang up with ground bounce, you may want to consider some of the design options described in the **box,** "A little more margin, please." You might also want to consider alternatives to using a bus driver in your design. The **box,** "Bus-driver alternatives" describes some options for common bus-driver applications.

Developing an array of ground-bounce reduction techniques, together with increasing IC transistor density, has enabled manufacturers to broaden their range of bus-driver products. Several manufacturers are offering bus-driver ICs that can handle 16 or more signals while still controlling ground bounce. Such manufacturers include Texas Instruments, National Semiconductor, and IDT. Early 1992 should see the introduction of 18- and 20-bit-wide parts from Motorola and a 36-bit-wide part, the SN74ABT32500, from Texas Instruments.

Ground-bounce control lets conventional 8-channel bus drivers quietly handle more current and greater

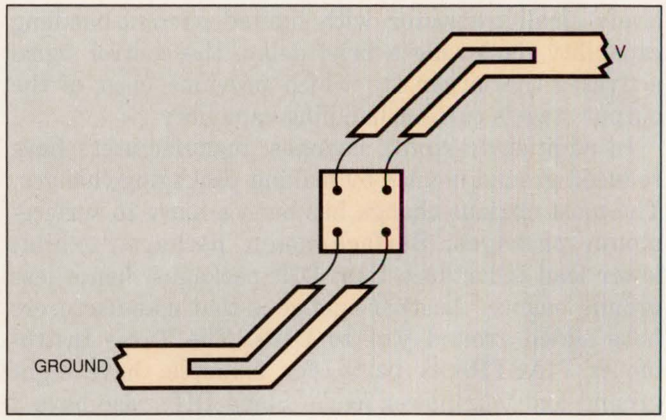


Fig 3—Using a split lead frame reduces ground bounce by letting two bond wires in parallel carry the ground signal, thus lowering the ground lead's inductance.

A little more margin, please

Manufacturers have made progress in removing ground bounce from their ICs, but you can give yourself an extra margin of safety through careful circuit design. The first step is to use synchronous design techniques wherever possible. Because ground bounce occurs only when outputs switch, a synchronous design may never see any ill effects from ground bounce occurring on data lines. The noise generated when output data changes on one clock edge will decay before the clock edge that latches that data into the next stage occurs.

If you're concerned about ground bounce affecting a clock line or if your design uses asynchronous logic, you can reduce the occurrence of problems by carefully assigning signals to ICs. Ground bounce increases with the number of signals switching simultaneously, so avoid running edge-triggering or clock signals through the same bus-driver ICs you use for data buses. An IC with four simultaneously switching output lines has less than 70% the ground bounce of one switching eight signal lines at once.

Even if you're stuck routing a sensitive signal through a noisy IC, you can still minimize potential problems with pin assignment. Because the lead inductance of an IC varies for each pin, the pins will see differing amounts of ground bounce. The pin closest to the IC's ground will be the quietest, exhibiting as little as half the noise of other pins.

Finally, you can use a series termination resistor in your critical signal path if you don't need a high drive current. The resistor will reduce the magnitude of a ground-bounce pulse. Several logic families have such resistors (generally 25Ω) built in, including the National Semiconductor 74BCT2xxx, Texas Instruments 74ABT2xxx, and Quality Semiconductor 74FCT2xxxT series.

load capacitance. Devices sinking at least 48 mA are the norm, and 64-mA capability is common. Texas Instruments' SN74BCT25xxx series can sink a whopping 188 mA, or source 80 mA, and suit designs with low-impedance (25Ω) buses and backplanes. Some families offer lower, but balanced drive capability, such as 24 mA; these parts sink and source current with equal facility.

Bus drivers acquire more logic

The additional die space that shrinking transistor sizes make available has let manufacturers add functions to the basic bus driver. Many of the device families listed in **Table 1** include parts with logic as well as bus-driver functions. **Table 2** (pg 86) lists commonly available combined-function parts.

Manufacturers are also combining several bus-driver functions within a single package. Texas Instruments, for example, offers the SN74ABT16500 18-bit bus transceiver. This device incorporates both D-type latches and D flip-flops into the basic transceiver design. By using the appropriate control logic you can operate the device in transparent, latched, or registered modes, thus emulating a variety of the devices in **Table 2**.

Another chip that has combined bus functions is the IDT 49FCT804 3-port bus multiplexer ($10). This device provides three 10-bit bidirectional ports that have 48-mA current-sinking ability. The part can connect any two of the three ports. Each port has a latch that also works in transparent mode, so you can use the part in both synchronous and asynchronous systems.

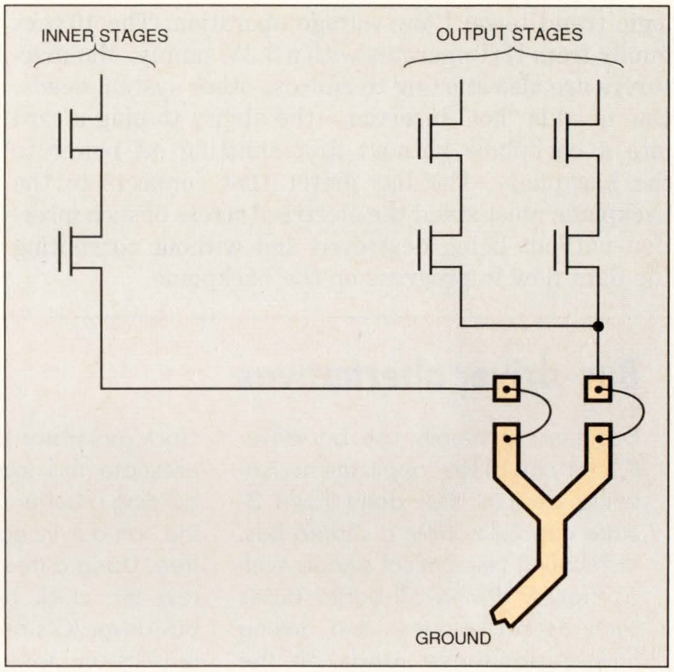


Fig 4—Splitting the on-chip ground among several pins isolates the IC's input stages from the output stage's ground bounce.

Bus-driver-IC manufacturers are evolving their products in other ways as well. Some are following the

Manufacturers of bus-driver ICs

For more information on bus-driver ICs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Harris Semiconductor
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Semiconductor & IC Div
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Brisbane, CA 94005
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BUS-DRIVER ICs

logic trend toward low-voltage operation. The 163xxx family from IDT operates with a 3.3V supply. Manufacturers are also starting to address other system needs. One need is "hot" insertion—the ability to plug a card into a backplane without first shutting off power to the backplane. The bus driver that connects to the backplane must stand the electrical stress of such insertion without being destroyed and without corrupting the data flow in progress on the backplane.

Several product families address hot insertion by providing power-up disable circuits. These bus drivers hold their output lines in a disabled state while the drivers are powering up. During the disabled state, logic elsewhere on the card can begin functioning and take control of the bus interface. Toshiba's 74ABTxxx family goes a step further by providing an I/O structure that prevents the IC from powering itself with current drawn from the bus.

Bus-driver alternatives

Designers generally use bus-driver ICs for one of four applications: isolating devices that don't have 3-state capability from a shared bus, distributing time-critical signals such as clocks, driving off-board buses such as backplanes, and driving high-capacitance loads on the same pc board. For many of these applications, bus drivers are not the only solution.

You can accomplish bus isolation, for example, by using a logic switch instead of a bus driver. The 74QST3384 ($3.55) from Quality Semiconductor is one such device. Its on-resistance of 5Ω lets it pass currents as great as 64 mA in either direction. The switch's current leakage when off is less than 1 μA. Using the switch for isolation instead of a noninverting driver has the advantage of letting you build a faster system. The switch adds no more than 250 psec of propagation delay to signals.

Avoid planting clock trees

If you're using a bus driver to distribute a clock signal on a pc board, you're probably minimizing onboard skew by replicating the clock using multiple output lines, then routing separate clock lines to various parts of the board. However, the combined input capacitance of the parallel driver lines may be too great a load for the clock generator to handle. You can eliminate this loading problem by building a buffer tree and restricting the fan-out in each branch of the tree. Using a tree, though, can narrow the clock pulse because the bus-driver IC's rise and fall characteristics are not symmetric.

An alternative to bus drivers for this type of clock distribution is a phase-locked-loop device such as the GA1110 ($35) from Triquint Semiconductor (Beaverton, OR). This device replicates the incoming clock via a programmable phase shift at the output lines. Each output can have a different shift. Thus, you can pre-skew the clock before distribution so the clocks are in sync when they reach their respective destinations.

For driving an off-board load, such as a backplane, you have a variety of choices. You can use high-capacity TTL-level drivers, such as the 188-mA 74BCT25xxx family from Texas instruments, or you can use non-TTL levels on the backplane.

Using a bus-translator IC, such as the Cypress Semiconductor (San Jose, CA) CY101E383 dual 10-channel ECL/TTL translator, simplifies the use of ECL in your system. Using ECL lets you run the backplane with a reduced voltage swing, thus easing noise and EMI problems. As an alternative to ECL, you can use the backplane translators National Semiconductor and Philips Components/Signetics developed for Futurebus+ systems. These devices can drive a backplane impedance as low as 12Ω.

Try altering backplane

You might even want to reconsider the nature of your backplane. If your system can support one, a star topology offers several advantages over a bus-oriented backplane. Star topologies place less of a burden on bus drivers because they limit bus connections to a single, fixed load. This limitation lets you use less drive current to maintain system speeds, which reduces both power-supply and cooling-capacity needs. The star topology also gives you more control over load impedances by letting you tune termination networks to control EMI and other electrical noise.

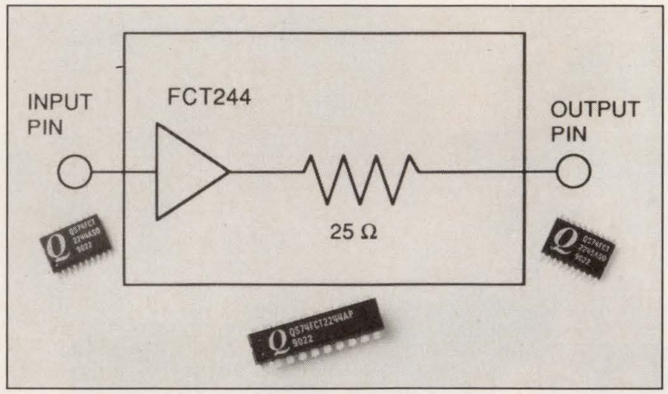
For driving high-capacitance loads on the same pc board, you'll probably need a bus-driver IC. First, check the drive capability of your other logic to see if it can handle the job without a driver. In some families, such as the Philips Components/Signetics and Texas Instruments 74ABTxxx series, all members have the same output drive capability—in this case, 64 mA.

BUS-DRIVER ICs

Table 2—Bus-driver functions

Functional description	Part designator
Inverting buffer	240, 540
Buffer	241, 244, 541
D flip-flop	273, 374, 534, 574
Transparent D latch	373, 533, 573
Transceiver	245
Latched transceiver	543
Inverting latched transceiver	544
Transceiver with storage register	646

Bus-driver manufacturers are also addressing board testability. Traditional bed-of-nails testing techniques are often unsuitable for surface-mount pc boards, which therefore need some form of built-in test. Bus-driver ICs are beginning to supply testability in the form of boundary scan. Parts emerging from Texas Instruments, Motorola, and National Semiconductor incorporate boundary-scan cells and control logic that meet the JTAG test specification IEEE 1149.1.



Series termination resistors help control ground bounce and other noise sources. Parts such as the QSFCT2xxx from Quality Semiconductor have such resistors built in.

The evolution of bus-driver ICs will continue throughout the decade. Because including bus-driver circuits in an ASIC would consume die area and could increase heat production beyond the capacity of plastic packaging, bus-driver ICs are likely to remain discrete products. And as long as discrete devices can pay for themselves in reduced ASIC silicon and packaging costs, designers will continue to leave the driving to them. EDN

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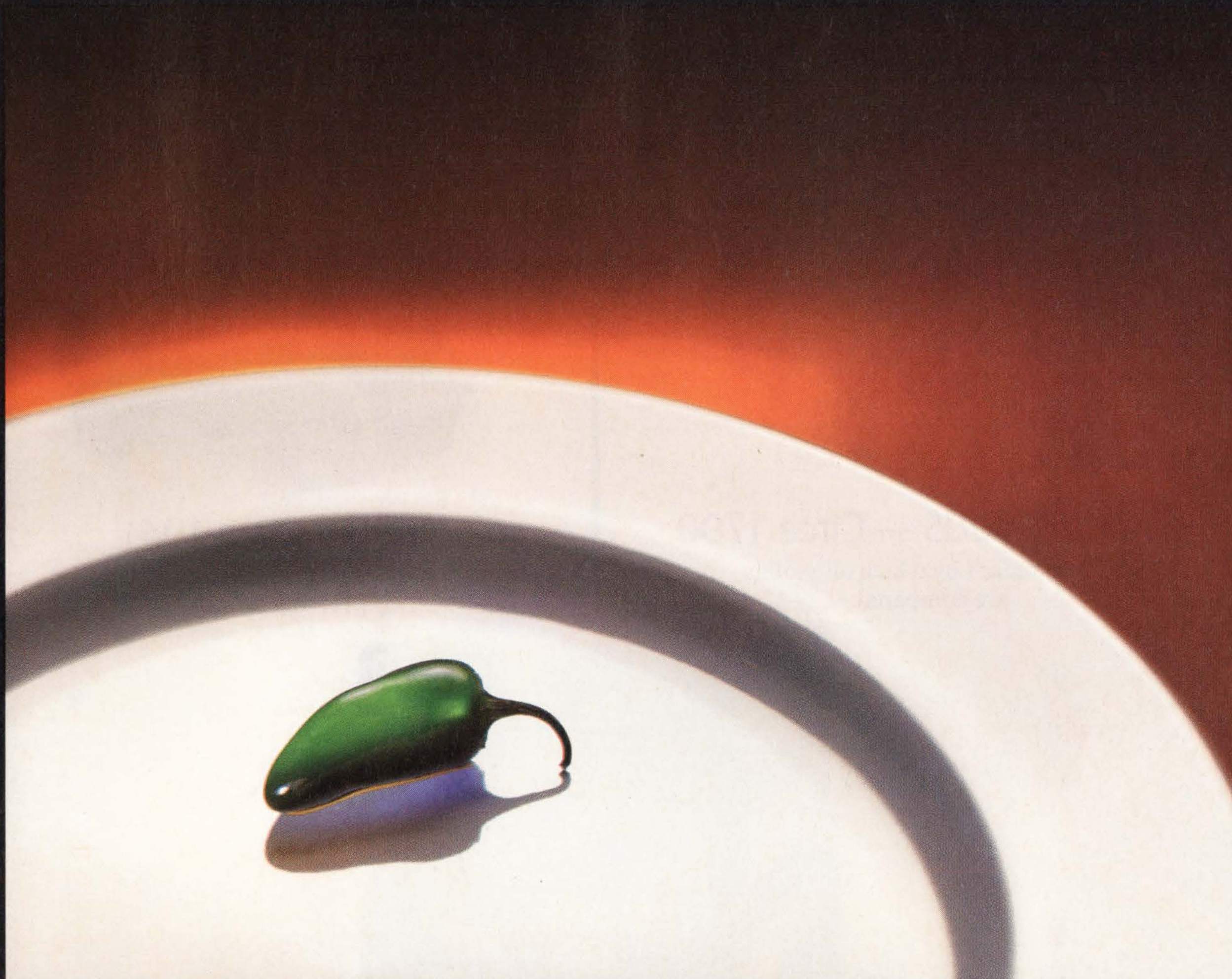

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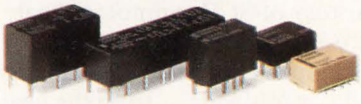

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Human-interface rules reduce test-program operator errors

John A Dinan, Raytheon Corp

The way a program displays data and interacts with its operator can either invite human error or minimize it. Following some simple rules can make all the difference, especially in a complicated test program.

You can design the human-interface part of a test program to minimize the number of errors an operator makes when using the program. In most cases, properly formatting your test data and giving the operator suitable guidance will help you avoid many known sources of human error.

For example, suppose you're running tests on a series of chips and displaying the results as follows:

```
                A B C D E F G H I J K
Test 1          P F F P P P F P P F P
     2          P P P P P P P P P P P
     3          P P F P F P P F P P P
     4          P F P F P F P P F P P
     5          P P P P P P P P P P P
     6          P F P P P P P P P P P
     7          F P F P F P P F P P F
```

You can expect an error rate of about 5% when a test operator reads these results. The similarity of the characters P (pass) and F (fail) invites error, as does the large number of characters in the display. Another contributor to error is the lack of spacing every few lines of data. (It's a good idea to insert a blank line for every five printed lines.)

You could reduce the error rate somewhat by displaying failures in a different color, such as red. But in so doing, you might introduce another error source: 9% of men are red-green color blind.

Instead, consider displaying failures only:

```
Test 1   B,C,G
     3   C,E,H
     4   B,D,F,I
     7   A,C,E,G,K
```

The error rate for reading this format approaches zero.

A display should present useful data in a way that isn't contrary to cultural experiences and thus operator expectations. We are all conditioned, for example, to read from left to right and from top to bottom.

Consider the following display format:

```
        Input                          Output
Frequency    Pulse length   Pulse length     Frequency
```

This layout has a pair of problems that could contribute to operator error. First of all, units of measurement are missing for frequency and pulse length. Second, and more important, the input and output subcolumns are in reverse order. This reverse order will result in confusion at best and possibly operator error. The psychological phenomenon known as perseveration—the tendency to continue a learned behavioral pattern—is responsible; the operator tends to read the output table as if its format is the same as that of the input table.

In displays of data, justify columns for rapid scanning. Compare the following layouts for ease of reading, first unjustified:

```
Channel number: NN
Frequency error: 10 Hz
Output: 1V
Self-test faults: none
Calibration faults: none
```

and then justified:

```
Channel number:          NN
Frequency error:         10 Hz
Output:                  1V
Self-test faults:        none
Calibration faults:      none
```

Also, always justify numeric data about the decimal point. It's much harder to scan this column of numbers:

```
26.53
106.21
50.25
87.50
1007.20
46.39
153.63
1365.60
```

than this one:

```
  26.53
 106.21
  50.25
  87.50
1007.20
  46.39
 153.63
1365.60.
```

A simple and effective guideline for displaying data is to lay out the data for smooth visual scanning in both the horizontal and vertical directions. The more complex the patterns, the greater the potential for error. Simple is better.

The following guidelines can also help you create user-friendly data displays:

- Display input data to the left of or above output data.
- When displays take more than one page, identify the page numbers (1 of 4, 2 of 4, and so forth).
- Place the data-entry area at the bottom of the screen just over the keyboard. It should be just under the error-message area and within the operator's immediate visual field.
- Display a symbol to indicate when tests are running and the keyboard is locked out.
- On each page of each display, indicate a key that will allow the operator to return to "home base" on a master menu with a single keystroke.

The layout in **Fig 1** illustrates some of these guidelines. This scheme won't be appropriate for every situation, but it is simple and free of any obvious sources of error.

A well-designed display can also minimize data-entry error. Perseveration again illustrates the point. An operator who has to put data into a certain spot on one data form may automatically (and erroneously) put similar data into the same spot in the next form. You can avoid this type of error by clearly defining data-entry fields and by making your forms' layouts consistent.

You can reduce other types of data-entry errors, too. You can't prevent simple keystroke errors or errors of short-term memory (trying to remember a long string of characters while keying them), but you can prevent many of the errors that result from operator confusion.

For example, an operator who is unsure that a program has accepted data or a command is likely to make errors in succeeding steps. You can minimize these errors in two ways—first by letting the user confirm data or commands before the program accepts them and then by informing the operator of their acceptance. By confirming data before accepting it, a program gives an operator an additional opportunity to correct keystroke errors before they result in corrupted data. Similarly, for commands such as "delete" that can result in the loss of data, your program can warn that

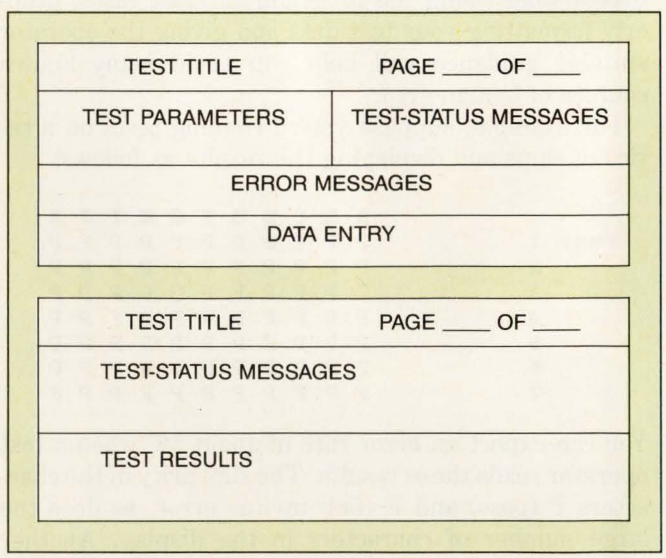

Fig 1—A test program's display should reduce the likelihood of error by the operator. This format for a 2-page display follows guidelines to achieve that objective.

data will be destroyed and ask if that is the operator's actual intent.

If your program detects an operator error, it should respond with a message that specifies how to recover from the error. For example, instead of simply saying that a specified test parameter is invalid, tell the operator that only a 4-digit entry is acceptable.

Military displays

Test programs to be used by the military will probably have to meet the requirements of MIL-STD-1472 **(Ref 1)**. By referring to the user-computer-interface information in Section 5.15, you can easily make a design checklist.

In some cases, your system specification will require the more complete guidelines of ESD-TR-86-278 **(Ref 2)**. This document is perhaps the most comprehensive user-interface design source available. Note, however, that it contains guidelines, not requirements. You should tailor the guidelines to your specific application.

Ease of learning reduces errors

At the heart of a user interface is the human/computer dialog. In general, dialogs that are easy to learn lead to fewer user errors. As **Table 1** shows, dialogs that use menu selections or questions and answers are your best bets.

A good way to see if your program is easy to learn is to conduct a "naive user" test. Select someone unfamiliar with your program and explain how to use the program to work a single-thread problem (a problem that exercises all the program's features). Then have the user work a typical problem while you watch for errors and confusion. Ask for comments and suggestions during and after the test. Repeat the process until the user is comfortable with the program and the user interface seems free of obvious sources of error and confusion.

The most common error source in a user interface is the "smart" shortcut. By building smart shortcuts into an interface, you give knowledgeable users more freedom, but you abandon design consistency. Beware: Smart shortcuts depend on users having perfect memory. You should not abandon consistent control procedures if you want to minimize user error.

Sequence control in a program, as described in **Ref 2**, "governs the transition from one transaction to the next." Because the potential for user error is at its highest at these transitions, you need to design sequence control carefully. To design a good sequence-control portion of a user interface,

- Give the user control in starting and stopping test sequences.
- Give feedback for all user actions and for all computer activities that affect the user.
- Consider function keys for frequently used or critical commands.
- Indicate the status of processing and control lockout.
- Allow user override of lockout with a function key or with a double action on a key.
- Display error messages that tell how to recover from the error conditions.
- Provide a "help" function that supplies increased detail when needed.
- Prompt users at points in the control sequence that appear confusing or complex—especially those that confused your naive user.
- Provide an easy way for a user to correct entries before the program acts on them.

Another part of a user interface that deserves extra attention is user guidelines—error messages, alarms, prompts, and labels, and other instructional material. Some helpful rules for creating user guidelines are

- Use affirmative statements ("Clear screen before entering data") rather than negative wording ("Do not enter data before clearing screen").
- Use the active voice ("Clear screen by pressing reset") rather than the passive ("The screen is cleared by pressing reset").
- Provide a list of valid options in each display.
- When the user selects an item from a display, highlight that item.
- If a fault can set off an alarm, provide an alarm-reset function that turns off the alarm but still leaves a visual reminder than the fault needs tending to.

Table 1—User training for computer interfaces

Dialog type	Required user training
Menu selections	Little/none
Q & A	Little/none
Form filling	Moderate/little
Function keys	Moderate/little
Natural language	Moderate/little
Query language	High/moderate
Command language	High
Graphic interaction	High

HUMAN-INTERFACE ROLES

- Write error messages that provide instruction ("Test ID # requires three digits"), not just a simple error indication ("Invalid input").
- Cue users when and where to enter data (by displaying a colon followed by an underscored data field, for example).
- Write your program so that at startup it briefly explains what the user needs to do and tells how to get help at any time.

If you follow all these rules when you design a user interface and then test the interface with a naive user, you should uncover most of the pitfalls that can cause user errors. Your displays will never eliminate user error, but they can minimize it. EDN

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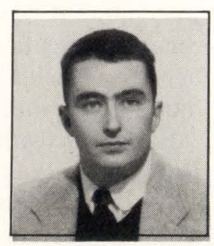
Author's biography



John Dinan, a senior engineer at Raytheon Corp in Wayland, MA, specializes in human-factor and safety engineering on large ground-based radar systems. John has a BA degree from Salem State College (Salem, MA) and an MA from Boston University (Boston, MA). He has done additional graduate work at George Washington University (Washington, DC). John's hobbies include collecting, researching, and writing about old popular literature such as dime novels and pulp magazines.

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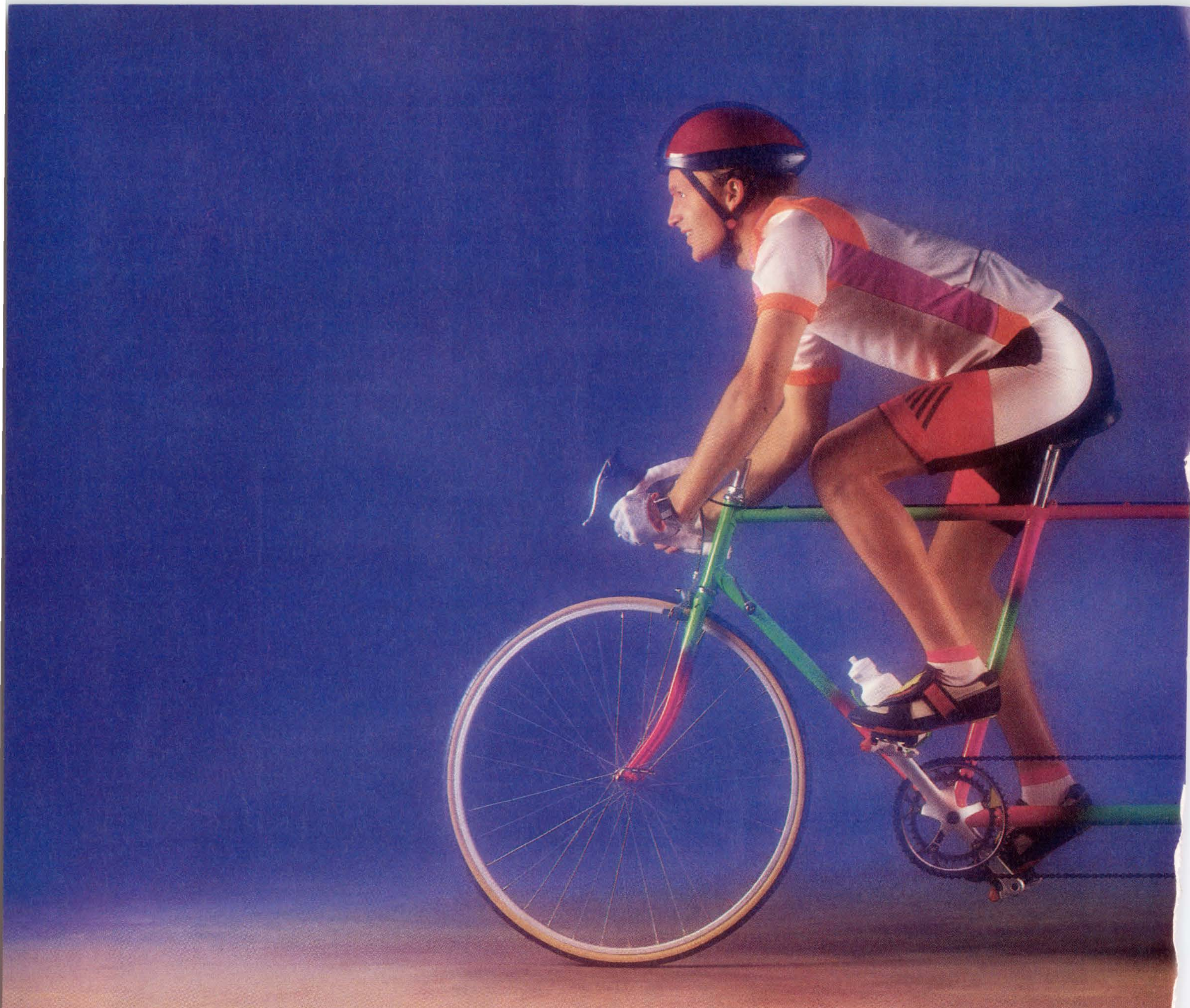

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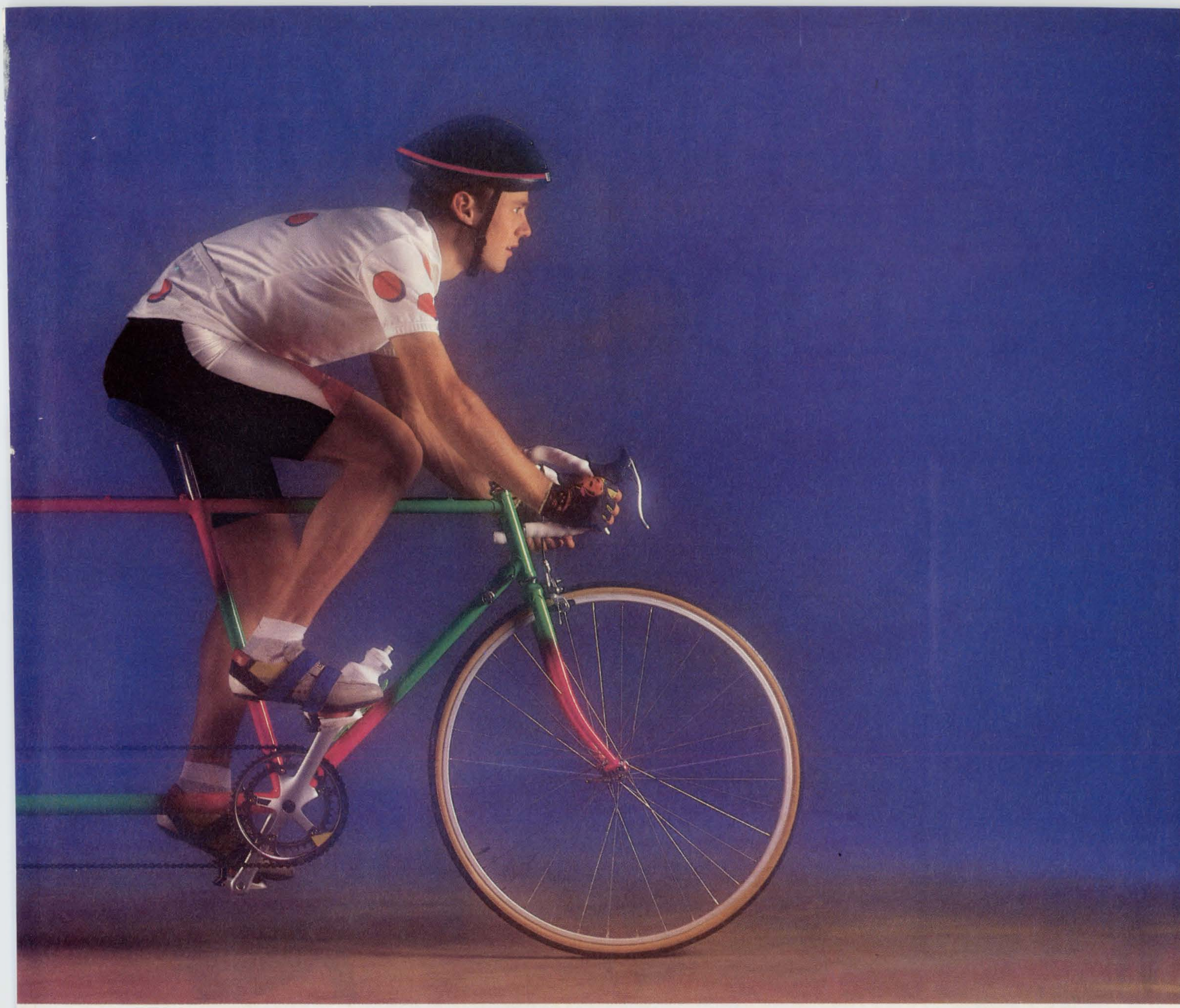

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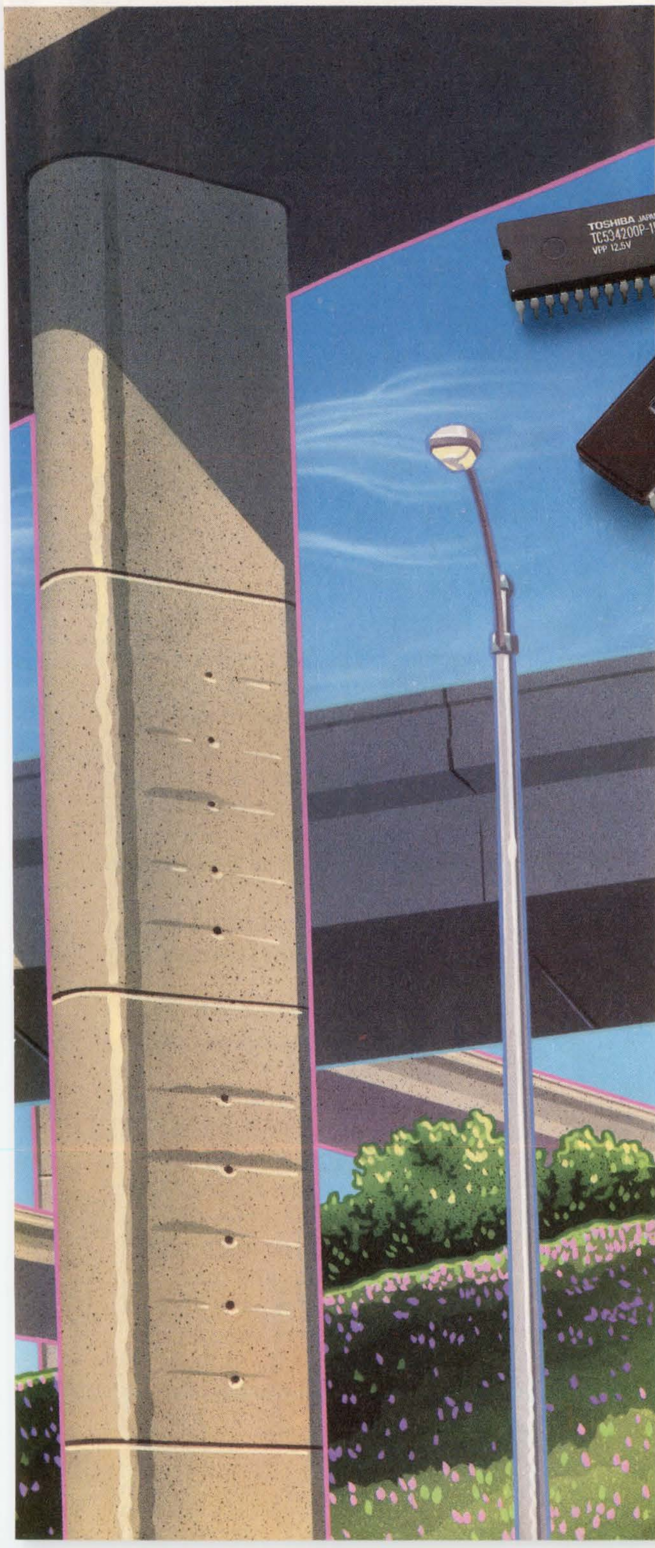

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Circular RAM buffer generates long delays

Yongping Xia, West Virginia University, Morgantown, WV

The circuit in **Fig 1** provides a delay interval for streams of 8-bit numbers. The delay for each number is equal to the RAM's total number of memory locations, divided by the clock frequency ($T=2^L/f_C$). For the components in the **figure**, delays range from 8.2 msec to 0.82 sec, depending on clock speed. The 6264's 300-nsec access time limits clock frequencies to under 2 MHz. Because the 6264 is a static device, the circuit has no low-frequency limit.

This 8k×8-bit static RAM functions as a circular buffer. The 74HC14s generate an adjustable clock for the 74HC4040 address counter. The address counter continuously cycles through the RAM's addresses. The 2-phase clock also coordinates the input and output buffers. The RC-delay networks in the RAM's $\overline{WE}$ line and the 74HC374 input-data buffer's OC line cause the circuit to first read out the contents of a particular memory location via the 74HC273 data-out buffer and then write the contents of the input buffer into that memory location. This process repeats for each memory location. Thus, the circuit holds a given datum only until the counter makes one complete cycle. **EDN BBS /DI_SIG #1080**

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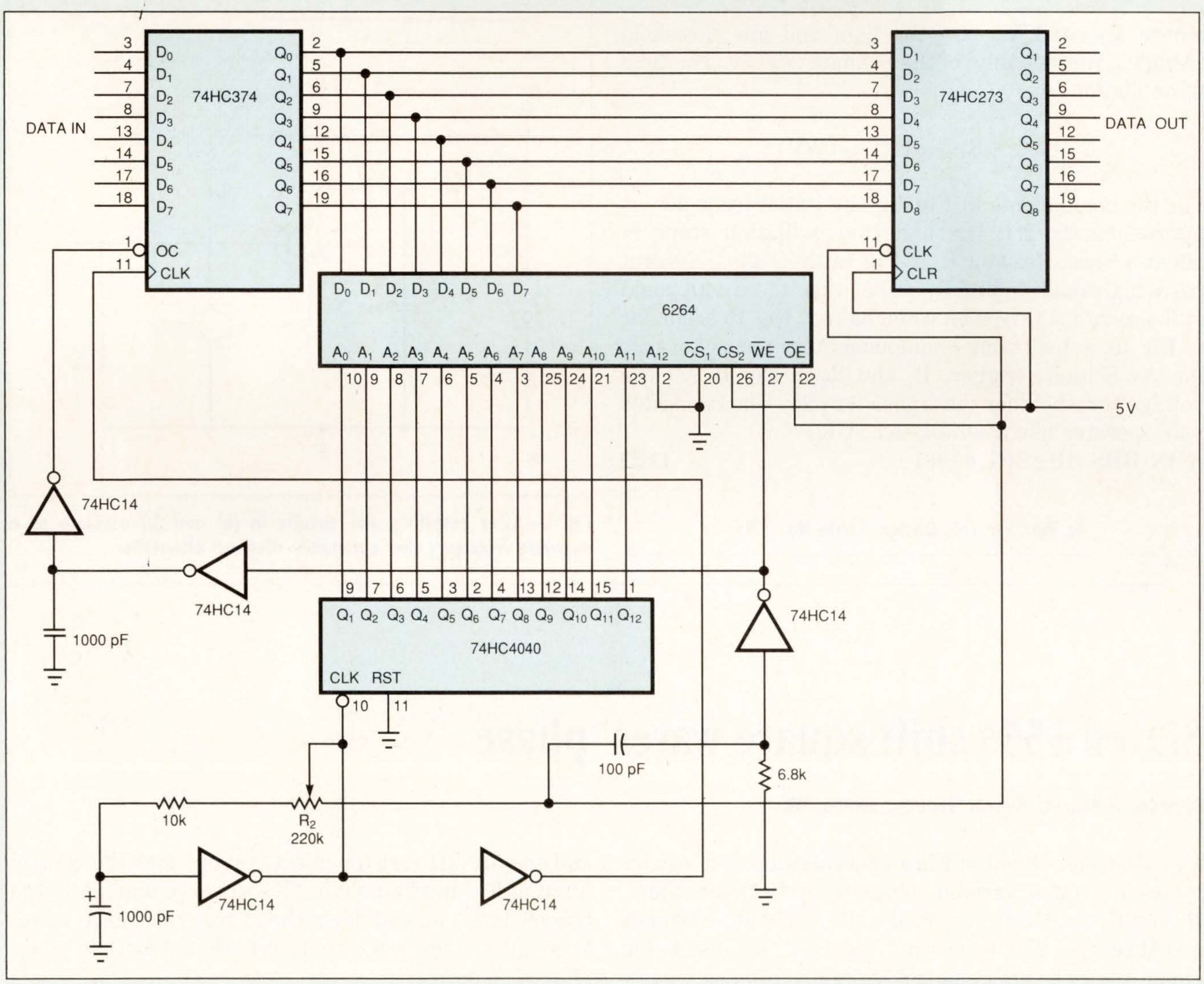

Fig 1—Functioning as a circular buffer, the 6264 static RAM provides a variable delay for streams of 8-bit data.

Decaying oscillator dies out

Gregor Said Jackson, Azad International, Hamburg, Germany

After resetting, the output frequency of the circuits in **Fig 1** decays exponentially, eventually dying out altogether. In **Fig 1a**, the voltage on capacitor C_1 determines the rate at which transistor Q_1 charges capacitor C_2. After resetting, C_1's low voltage causes Q_1 to charge C_2 quickly. When C_2's voltage exceeds the Schmitt trigger's (IC_1's) threshold, the Schmitt trigger changes state, discharging C_2. As C_1 charges up, C_2 takes longer to charge up, lengthening the period of the output. The time-dependent equation for the circuit's frequency is

$$f=((V_{DD}/\exp(t/R_1C_1))-0.7V)/((V_{TH}-V_{TL})/R_2C_2),$$

where V_{TH} and V_{TL} are the high and low threshold voltages, respectively, of the Schmitt trigger. The time of oscillation is

$$t_{OSC}=R_1C_1\times\ln(V_{DD}/0.7V).$$

For the components in **Fig 1a**, the initial frequency is approximately 280 Hz, and the oscillation stops in about 3.9 sec. Resistor R_4 in **Fig 1a** sinks any quiescent current through Q_1 and D_1. Otherwise, the circuit could still oscillate slowly even when halted. **Fig 1b** is similar to **Fig 1a**, substituting a complementary transistor pair for the Schmitt trigger. R_1 and R_2 in **Fig 1b** set the voltage threshold for the transistor pair. The transistor pair operates like a self-biased SCR.

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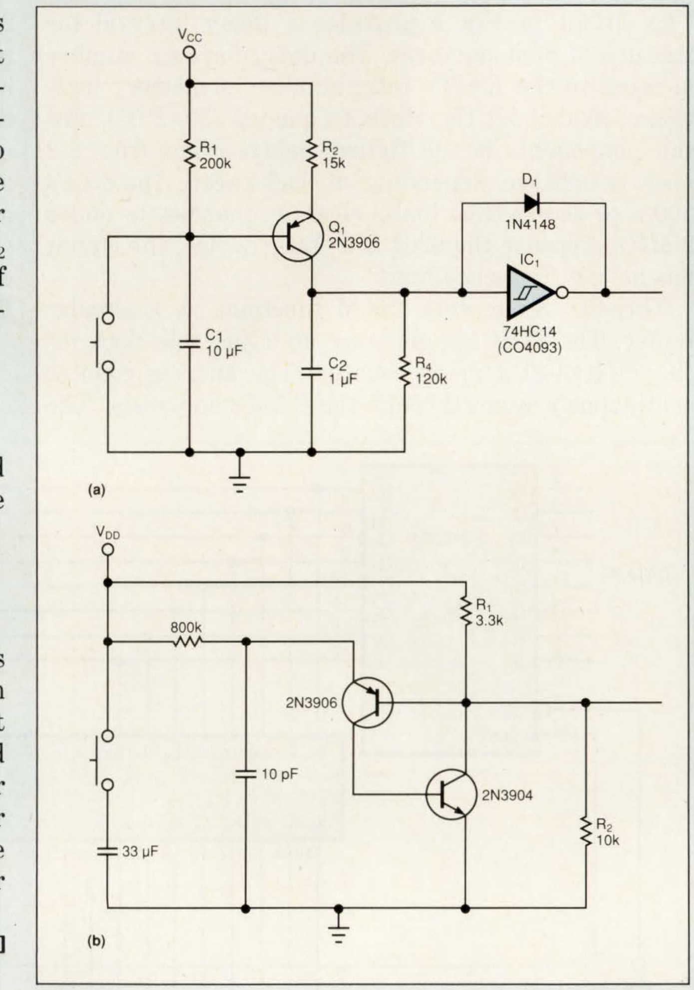

Fig 1—After resetting, the circuits in (a) and (b) oscillate at a decaying frequency that eventually dies out altogether.

Slaved 555s shift square waves' phase

Raymond N Bennett, Remote Security, Seattle, WA

The 555-timer circuit in **Fig 1** generates a pair of square waves having a variable phase shift between them. R_1 and C_1 set the timing of IC_1. IC_1's and IC_2's trigger and threshold pins are slaved together. All else being equal, the two timers should therefore produce nearly identical square waves. However, potentiometer R_2 and the 510-kΩ resistor inject current into the control input of IC_2, in effect sliding IC_2's charge and discharge trigger levels up and down the charge-discharge waveform of C_1, shifting IC_2's output back and forth in phase with IC_1's output.

The circuit is not perfect. Because the 555s' charge

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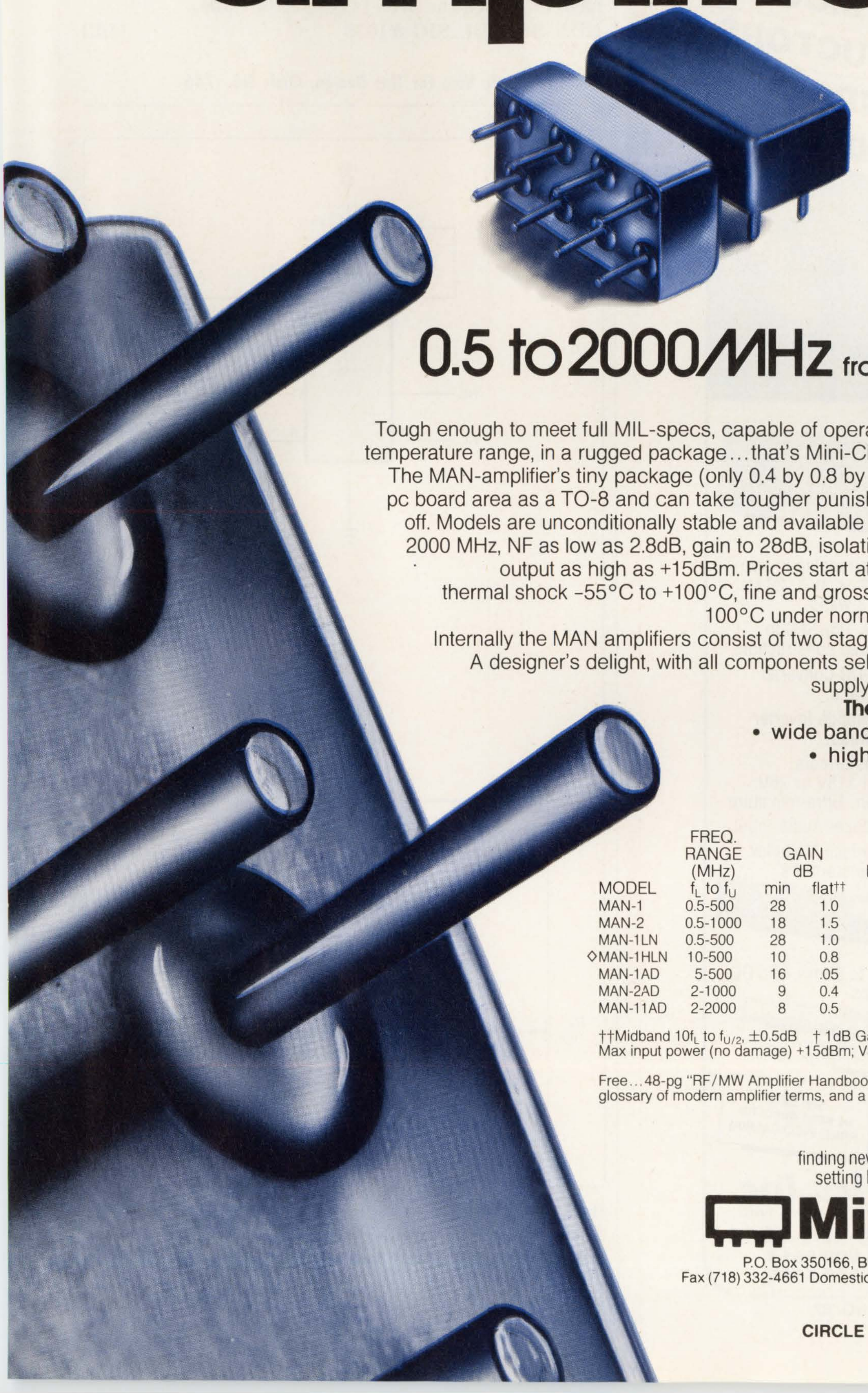

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MODEL	FREQ. RANGE (MHz) f_L to f_U	GAIN dB min	GAIN dB flat††	MAX PWR† dBm	NF dB (typ)	ISOL. dB (typ)	DC PWR V/ma	PRICE $ ea. (10-24)
MAN-1	0.5-500	28	1.0	+8	4.5	40	12/60	13.95
MAN-2	0.5-1000	18	1.5	+7	6.0	34	12/85	15.95
MAN-1LN	0.5-500	28	1.0	+8	2.8	39	12/60	15.95
◇MAN-1HLN	10-500	10	0.8	+15	3.7	14	12/70	15.95
MAN-1AD	5-500	16	.05	+6	7.2	41	12/85	24.95
MAN-2AD	2-1000	9	0.4	-2	6.5	28	15/22	22.50
MAN-11AD	2-2000	8	0.5	-3.5	6.5	22	15/22	29.95

††Midband $10f_L$ to $f_{U/2}$, ±0.5dB † 1dB Gain Compression ◇Case Height 0.3 in.
Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.

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CIRCLE NO. 66

C118 REV. F

and discharge slopes are not linear, the duty cycle of IC_2 changes with phase changes. In the worst case, if either threshold moves outside the limits of the charge-discharge waveform, IC_2 will stop oscillating. If you use NMOS timers instead of CMOS devices, you will have to reduce the 510k-Ω resistor's value.

EDN BBS /DI_SIG #1078

To Vote For This Design, Circle No. 746

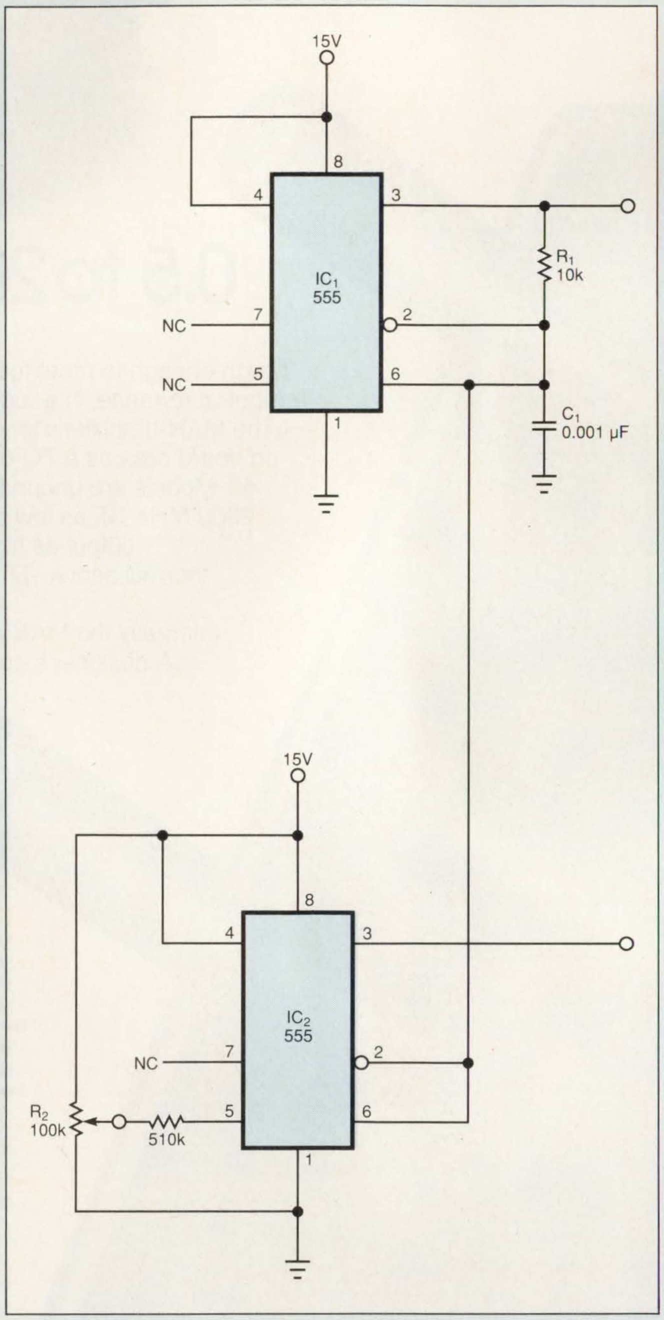
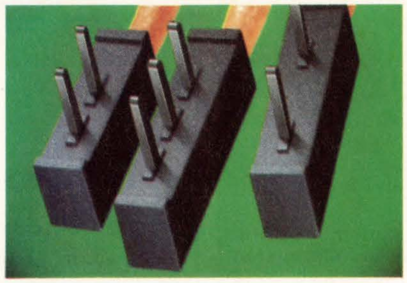


Fig 1—In this circuit, the bottom 555 timer is slaved to the top timer. However, the potentiometer and resistor at pin 5 of the bottom 555 injects current that slews the phase relationship of the two timers' outputs.

Impedance matched PCB Solderable Interconnects

- *Solders directly to the PCB*
- *Low profile*

Meritec's PCB Solderable Interconnects can be soldered directly to the PCB for a permanent connection. Pin lengths of .110″ and .160″ are available for different board thicknesses. The impedance matched connectors feature precision, high strength molded terminations for reliability in critical applications. Available in 1×2 and 1×3 configurations, the connectors are side-to-side stackable and feature heights as low as .150″ from the PCB, making



them ideal for dense package applications. The connectors can be terminated to a variety of different cable styles.

CIRCLE NO. 68

96 Position DIN Cable Assembly

- *Impedance matched*
- *Programmed grounds and signals*

Meritec's impedance matched 96 Position DIN Cable Assemblies feature an internal PCB which allows programming of grounds and signals to customer specifications. The high speed, low noise controlled impedance assemblies are designed for TTL fast, fast CMOS and ECL logic. Standard impedances are available from 50 to 120 ohms using low dielectric FEP cable to ensure less propagation delay. EMI/RFI electrical shielding is optional. Signal and ground wires are mass solder terminated to the PCB. Insert molded strain relief provides high reliability in critical applications.

CIRCLE NO. 69

Digital and analog interconnect systems that maximize board density and budget.

If you need speed and performance in a digital or analog interconnect system but have a limited budget, turn to Meritec. Meritec digital and analog interconnect systems are designed to meet the requirements of electrically sensitive applications using high speed CMOS, ECL or GaAs logic. Our systems are engineered to provide controlled impedance and propagation delay while minimizing crosstalk. You get ship to stock quality, backed up with technical service and applications support. All at a cost that's well in line with tight project budgets.

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CIRCLE NO. 71

BNC Cable Assemblies for critical applications

- *Impedance matched*
- *High strength molded terminations*

Meritec's impedance matched BNS cable assemblies feature precision, high strength molded terminations for high reliability in critical applications. The assemblies are available in a variety of configurations, including cable end plug, cable end jack, front panel mount jack, front panel mount jack with isolated ground and rear panel mount jack. The connectors are terminated using subminiature coax cable and feature standard BNC and cable impedances of 50 and 75 ohms. The assemblies may be terminated with Meritec's SSI™, SSC™ or PCB Solderable interconnects on the opposite end.

CIRCLE NO. 70

Software Shorts

8051 moves blocks 100% faster

Peter Kielbasiewicz, Hewlett-Packard, Böblingen, Germany

The listing in **EDN BBS /DI_SIG #1063** doubles the speed of an 8051 microcontroller's block move by using a page-addressing algorithm.

To Vote For This Design, Circle No. 747

Spreadsheet aids PLL design

Bruce Acker, Engineering Solutions, Tarzana, CA

Two Excel spreadsheets in **EDN BBS /DI_SIG #1066** calculate the open-loop frequency response and the compensation stage's R and C values for phase-locked-loop (PLL) designs.

To Vote For This Design, Circle No. 748

22V10 handles 680xx DMA and interrupts

Sean Powers, Stratus Computer, Marlboro, MA

The Boolean equations in **EDN BBS /DI_SIG #1059** program a 22V10 to handle three functions for 680xx μPs: 7-level interrupt prioritizing, generating a μP-halt signal, and managing DMA-controller retries.

To Vote For This Design, Circle No. 749

DSP program determines μP type

Jerzy R Chrząszcz
Warsaw University of Technology, Warsaw, Poland

EDN BBS /DI_SIG #1072 contains a compressed, concatenated file consisting of an extensive discussion of compatibility among various Texas Instruments DSP μPs. The file also includes an assembly-code listing that lets a program test for the TI DSP μP it is running on.

To Vote For This Design, Circle No. 750

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on EDN's bulletin-board system (BBS): (617) 558-4241,300/1200/2400,8,N,1. From Main Menu, enter ss/DI_SIG, then rk*nnnn*, where *nnnn* is the number referenced above.

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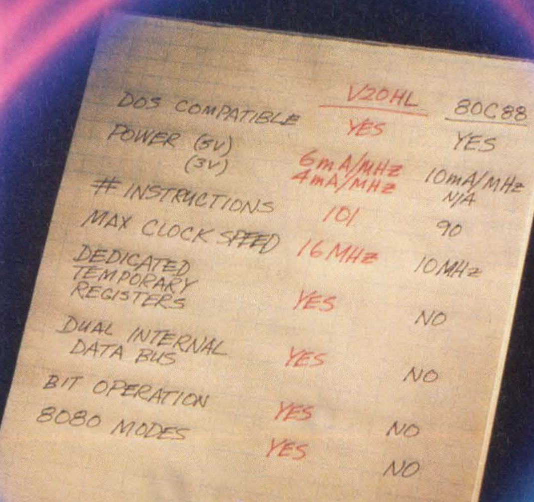

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CIRCLE NO. 74

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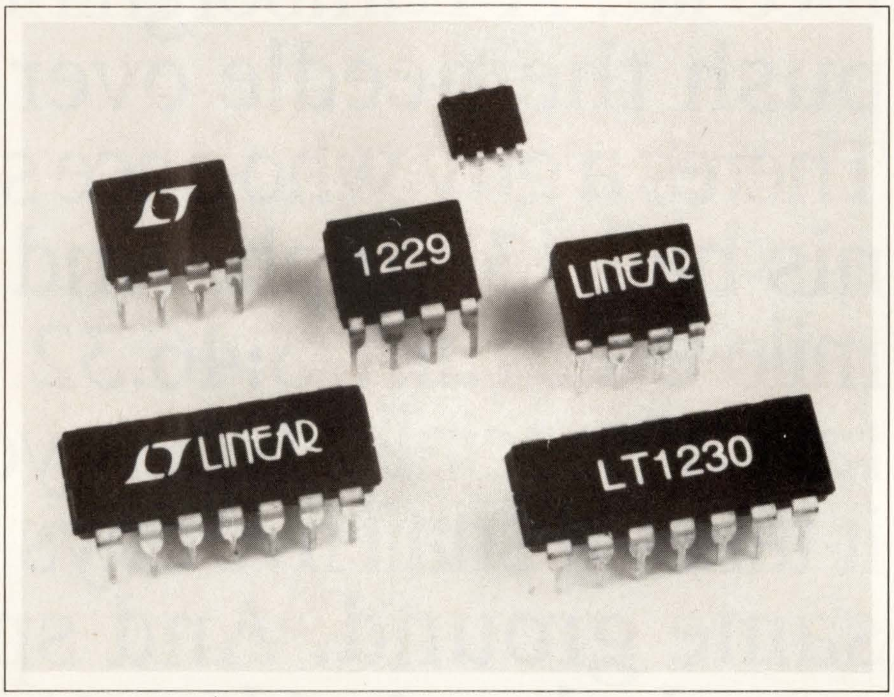
They're big. They're fast. They're everything you've asked for. Want to know more? Speed dial 1-800-800-7256. MAX7000

CIRCLE NO. 76

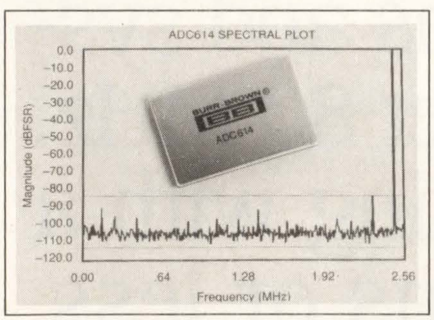
Current-Feedback Op Amps With 100-MHz Bandwidth

- *Slew rate is 1000V/μsec*
- *15-MΩ input impedance*



The LT1229 (dual) and LT1230 (quad) are current-feedback op amps whose 100-MHz bandwidth and 1000V/μsec slew rate remain fairly constant over a range of closed-loop gains. The dc-coupled amplifiers have only 6-nV/$\sqrt{\text{Hz}}$ of noise and an impedance of 15 MΩ at the noninverting inputs. The op amps are specified for operation at supply voltages from ±2 to ±18V. The maximum supply current (each amplifier) is 9.5 mA. When operating at a gain of two and driving a 75Ω cable, the differential gain and phase of the op amps are 0.04% and 0.1°, respectively. In RGB (red, green, blue) video systems, the fast rise time of 3.5 nsec eliminates smearing. The amplifiers also have an output-drive capability of 30 mA, which allows them to drive low-impedance loads. The 8-pin LT1229 and 14-pin LT1230 are available in DIP and SO packages. $3.95 and $7.25, respectively, (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; (408) 432-1900. **Circle No. 351**



14-Bit subranging A/D-converter system. The ADC614 hybrid IC, a subranging ADC subsystem, contains a 14-bit A/D converter, a sample/hold amplifier, a voltage reference, and timing circuitry. The IC, which comes in a 46-pin ceramic and metal package, features a sampling capability from dc to 5.12 MHz and a Nyquist spurious-free dynamic range of −88 dB. Other key specifications include no missing codes, an analog-input bandwidth of 40 MHz, and a S/N ratio of 74 dB at 2.3 MHz. $990 (100). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 352**

32-bit microcontroller. The 68F333 32-bit microcontroller contains 64 kbytes of flash EEPROM, allowing you to alter or update electronic modules by reprogramming the software. Other features include an 8-channel 10-bit A/D converter, 512 bytes of standby RAM, 3.5 kbytes of general RAM, a 16-bit timer, and a serial peripheral interface. The 68F333, in a 160-pin quad flatpack, $199.95. Sample quantities will be available in the second quarter of 1992. **Motorola Inc,** 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-3465. **Circle No. 353**

Color coprocessor chip. The Render-Ready Graphics Array (RRGA) compresses 24-bit pixel data for use with an 8-bit graphics frame buffer. Suiting CRT or flat-panel display controllers, the RRGA uses a linear 256-color RGB (red, green, blue) palette to provide photo-quality images. The chip features a 25-MHz conversion throughput, which is fast enough to process 30 1024×768 frames/sec. In a 68-pin plastic leaded chip carrier, $25. **Vermont Microsystems,** 11 Tigan St, Winooski, VT 05404. Phone (802) 655-2860. FAX (802) 655-9058. **Circle No. 354**

High-speed RAMDAC. A 150-MHz version of the Bt459 triple 8-bit RAMDAC complements the company's 80-, 110-, and 135-MHz speed grades. Designed for workstation applications, the device supports resolutions to 1280×1024 pixels. The RAMDAC also handles European refresh standards of 76 and 77 Hz. Available in 132-pin, pin grid arrays and plastic quad flatpacks, $120 and $107, respectively, (100). **Brooktree Corp,** 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. FAX (619) 452-1249. TLX 383596. **Circle No. 355**

High-density programmable logic. The 84-pin CY7C341 erasable programmable logic device (EPLD) features 7500 equivalent gates and runs to 50 MHz. Consolidating approximately 30 22V10s, the 192-macrocell EPLD is the fourth and highest-density

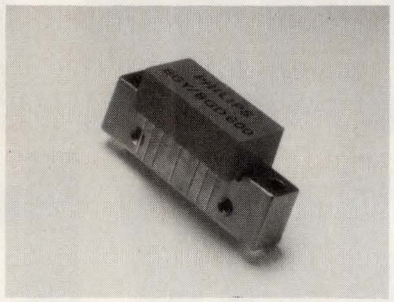
member of the company's MAX family. In plastic-leaded-chip-carrier and pin-grid-array packages, the CY7C341, \$337 (100). **Cypress Semiconductor,** 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600.
Circle No. 356

Dual-port video RAMs. Designed to speed system performance by off-loading screen refresh from the data bus, these video RAMs are available in two versions. The 24-pin KM424C64, a 256-kbit device organized as 64k×4 bits, is available in access times of 100 and 120 nsec. The 28-pin KM424C256, a 1-Mbit device organized as 256k×4 bits, is available in access times of 80, 100, or 120 nsec. In 100-nsec versions, the KM424C64 and KM424C256 are \$3.10 and \$8, respectively, (1000). **Samsung Semiconductor,** 3725 N First St, San Jose, CA 95134. Phone (800) 423-7364; (408) 954-7000. **Circle No. 357**

Video switch and amplifier. The CA3256 video switch and amplifier provides five channels of CMOS multiplex switching and a bipolar output amplifier on a single chip. Channels 1 through 4 are digitally selected and include LED output drivers to indicate the "on" channel. Channel 5 is independent and can function as a monitoring output for signal information on the other channels. The CA3256, in 18-pin DIPs and 20-pin SOICs, \$4 (100). **Harris Semiconductor,** Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1042; (407) 724-3704. **Circle No. 358**

Analog multiplexer. Able to switch in 17 nsec, the CLC532 2:1 analog multiplexer can pass either of its inputs to the output with better than 0.01% accuracy. Other key specifications include channel isolation of −80 dB, harmonic suppression of −80 dBc, and differential gain and phase of 0.05 dB and 0.01°, respectively. CLC532, in 14-pin DIPs or SOICs, \$9.49 (1000). **Comlinear Corp,** 4800 Wheaton Dr, Fort Collins, CO 80525. Phone (303) 226-0500.
Circle No. 359

12-bit multiplying DACs. The MAX501 and MAX502 are 12-bit, 4-quadrant, voltage-output multiplying D/A converters. They combine a BiCMOS amplifier having a ±10V drive capability with a laser-trimmed, thin-film resistor DAC on a single chip. The DACs accept a dc or ac reference and have buffered input latches. The MAX501 acquires data in an 8+4-bit format, and the MAX502 in a 12-bit format. In 24-pin DIP and SO packages, from \$5.65 (1000). **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. **Circle No. 360**



Wide-bandwidth CATV modules. Designed for use as repeater amplifiers in CATV networks, the BGY600 series of amplifier modules and the BGD600 series of power-doubler modules feature a bandwidth of 40 to 600 MHz. The BGY series amplifiers offer six different power gains from 12.5 to 27 dB. The BGD series power doublers have a power gain of 12.5 or 18.5 dB. Both series feature low noise figures. The modules utilize thin-film technology and are housed in SOT-115 packages, which suits them for upgrades to existing equipment. The 18.5-dB BGY685A amplifier, \$29.16; the BGD602 power doubler, \$38.88 (500). Delivery, 8 to 10 weeks ARO. **Philips Components,** Literature Center, 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762; (407) 881-3308. Outside the US: Philips Components, Marketing Communications Dept, Bldg BA, 5600 MD, Eindhoven, The Netherlands.
Circle No. 361

PC/AT chip set. The DXBB chip set adds a local bus to the ISA bus and uses EISA connectors. The local bus transfers data at 66 Mbytes/sec. The chip set consists of the 82C496 CPU block-interleave dynamic RAM and AT bus controller, the 82C206 peripheral controller, and the 82C497 write-back caching controller. The chips work with 80386/486 CPUs from Intel and AMD. The 82C496 and 82C206 pair, \$27.50; the 82C497, \$17.50 (10,000/quarter). **Opti Inc,** 2525 Walsh Ave, Santa Clara, CA 95051. Phone (408) 980-8178. FAX (408) 980-8860. **Circle No. 362**

Frequency Synthesizer. The MC-145191, a phase-locked-loop (PLL) frequency synthesizer, runs to 1.1 GHz. A byte-oriented interface can operate at 4 Mbps. Tuning is via a 3-byte serial transfer to the 24-bit A register. The R, N, and A counters are fully programmable, and the C register configures the part to meet various applications. The C register can also shut off unused outputs to minimize system noise. In a 20-pin SO package, \$5.50 (500). **Motorola Inc,** Box 6000, Austin, TX 78762. Phone (800) 521-8274. **Circle No. 363**

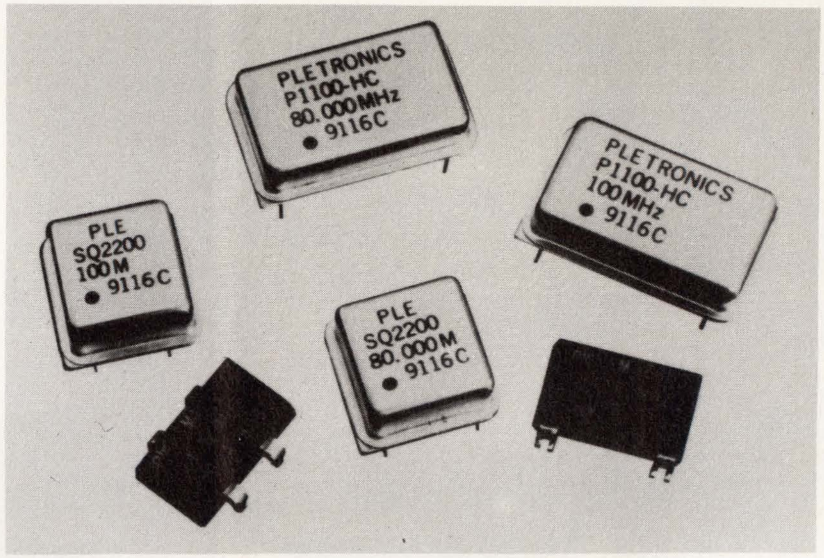
SCSI controller. Designed for 32-bit CPU-based systems, the μPD72611 SCSI controller supports data-transfer rates to 10 Mbytes/sec over an 8-bit SCSI bus. The device also provides a selectable host bus, supporting 32-, 16-, and 8-bit widths. Other features include a 24-bit transfer counter, single-ended SCSI bus drivers, and Schmitt-type receivers. In a 100-pin quad flatpack, \$17.50 (10,000). **NEC Electronics Inc,** 401 Ellis St, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985. **Circle No. 364**

Opto-isolated 12-bit ADC. MAX171 is a 5.8-μsec, 12-bit A/D converter that provides over 1500V-rms isolation between its analog input and the digital interface pins. The device combines a serial-output ADC, three optocouplers, and a low-drift buried-zener reference in a standard 16-pin DIP. You can drive the 2.5-MHz clock input from an external source. The MAX171 operates from 5V and −12 to −15V supplies. From \$20.25 (1000). **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.
Circle No. 365

16-bit D/A converter. The AD669 DACport integrates on a single chip a 16-bit DAC, a reference, a span-programmable output amplifier, and double-buffered latches. The output amplifier is pin-programmable for unipolar or bipolar spans of 0 to 10V or −10 to +10V. Specifications include 15-bit monotonicity over the operating temperature range, ±1-LSB differential and integral nonlinearity, THD+N of 0.0009% (max), and a S/N ratio of 84 dB. In 28-pin DIP and SO packages, from \$16 (100). **Analog Devices,** 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. FAX (617) 821-4273. **Circle No. 366**

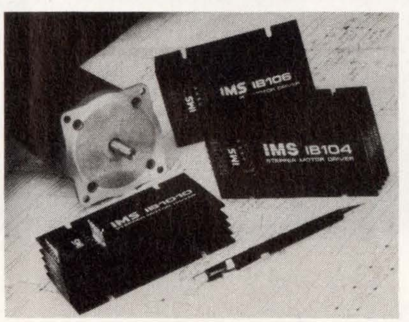
Clock Oscillators

- *Operate to 120 MHz*
- *Provide a CMOS output*



These clock oscillators develop outputs in the 50- to 120-MHz-range standard frequencies of 50, 60, 64, 66, 66.667, 80, and 100 MHz and are available from stock. The output is High-speed CMOS compatible and can drive 15 standard TTL loads. The units are available in a choice of package styles: a 4-pin model in a 14-pin metal DIP; a 4-pin model in an 8-pin miniature DIP; a 0.3×0.5-in. surface-mount package with J leads; and a 0.3×0.5-in. surface-mount package with gull-wing leads. The crystal operates in the fundamental mode at all outputs, minimizing mode-shift problems. Oscillator outputs are 3-state types and are short-circuit protected. Inputs and outputs are also ESD protected. \$3 to \$8 (1000).

Pletronics Inc, 19015 36th Ave W, Suite H, Lynwood, WA 98036. Phone (206) 776-1880. **Circle No. 367**



Stepping motor drives. Models IB104, 106, and 1010 bipolar stepping motor drives utilize MOSFET technology to develop 1800W of power. Housed in a package measuring 6 in.^{3}, the units operate from a supply voltage of 24 to 100V dc. The 104 develops 4A/phase, and the 106 and 1010 develop 6 and 9A/phase, respectively. With optically isolated inputs and onboard logic for full- and half-step operation, these drives are suitable for pc-board mounting, direct-frame, or chassis mounting. IB104, \$138 (100). **Intelligent Motion Systems Inc,** 511 Norwich Ave, Taftville, CT 06380. Phone (203) 889-8353. FAX (203) 889-8720. **Circle No. 368**

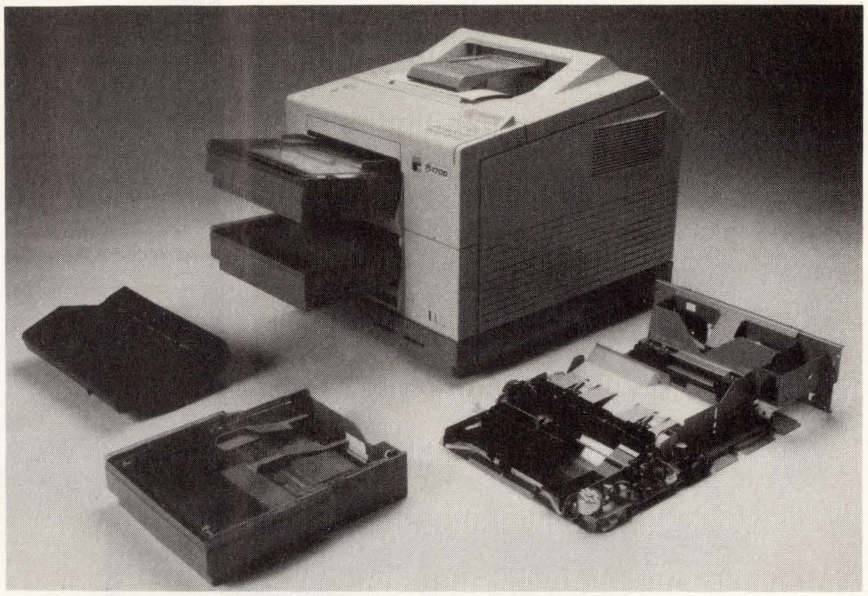
Signal conditioner. The Model 161MK strain-gauge signal-conditioner system operates with a ±15V supply. A DIP-switch selection chart printed on the card shows you how to select corner frequency (10, 100, 1000 Hz). The unit is designed for use with metal-foil gauges. The unit's excitation regulator can supply from 0 to 100 mA. A trimmer mounted on the card selects bridge excitation levels between 4 and 12V dc. **Calex Mfg Co Inc,** 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (800) 542-3355; (510) 932-3911. FAX (510) 932-6017. **Circle No. 369**

Plastic connectors. ABC solderless, plastic connectors are capable of bidirectional operation because each mated half of the unit can contain both pin and socket contacts. The rectangular connector shells are available in either 1- or 2-in. sizes. Standard plugs mate with three types of receptacles—in-line stack mount, flange mount, and pc-board mount. EMI/RFI shielded back shells are also available. Approximately \$65 (100). Delivery, four to six weeks ARO. **Deutsch Co,** Municipal Airport, Banning CA 92220. Phone (714) 849-7822. FAX (714) 922-1544. **Circle No. 370**

Image sensor. The E3W2 programmable-line-array, image-sensor system consists of a light source, a sensing head, and a controller. The system has a sensing accuracy of 0.5 mm through a 25- to 500-mm field of vision. The system controller features a 100-step programmable memory that can store as many as four independent programs. The controller provides three relay outputs and also accepts two gate inputs. It features a built-in power supply for external sensors. \$1500. **Omron Electronics Inc,** 1 E Commerce Dr, Schaumburg, IL 60173. Phone (800) 826-6766; (708) 843-7900. FAX (708) 843-7787. **Circle No. 371**

Power transistors. MRF10070, 10150, 10350, and 10500 microwave power transistors operate in the 1025- to 1150-MHz frequency band. Output power capability for the four devices equals 70, 150, 370, and 500W, respectively. Each transistor operates from a 50V supply and has a typical gain ranging from 9 to 10 dB. All four parts are supplied in hermetic, metal-ceramic packages and are internally matched for broadband operation. \$185 to \$435 (25). **Motorola Inc,** E-114, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-3818. FAX (602) 244-4597. **Circle No. 372**


LabWindows Instrumentation System
TRG
Signal
Source
Signal Spectrum
LabWindows
LabWindows



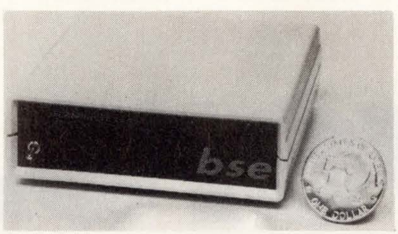
Laser Printer

- *Connects to Ethernet or Token Ring networks*
- *25-MHz 80960 μP produces 600 × 600 dpi resolution*

The QMS-PS 1700 laser printer connects directly to an Ethernet or Token Ring network when you install optional interface cards. The printer also includes standard RS232C serial, Centronics parallel, and Localtalk ports. An 80960 μP and 8 Mbytes of RAM, which is expandable to 16 Mbytes, produce 600 × 600-dpi or 300 × 300-dpi resolution. The printer serves as many as 20 users on Netware, Ethertalk, TCP/IP, or DECnet networks. The printer employs a proprietary Crown operating system that permits selectable printer resolutions and automatic sensing of Postscript, HP PCL, HP-GL, or optional LN03 Plus printer languages. Job spooling permits each of the printer's four ports to receive print jobs while a job from another port is printing. For 20 users, less than $10,000; optional TCP/IP or DECnet Ethernet card, $1995.

QMS Inc, 1 Magnum Pass, Mobile, AL 36689. Phone (205) 633-4300. FAX (205) 633-0013.

Circle No. 373



Portable hard-disk drives. The Flashdrive comprises portable hard-disk drives for laptop and notebook computers. They are tested and approved by Atari, NEC, Poqet, and Toshiba. The drives add from 20 to 750 Mbytes of external storage to the host's internal capacity. For example a 40-Mbyte drive increases the total capacity of a computer having a 20-Mbyte internal drive to 60 Mbytes. The drives' software occupies 1.5 kbytes of the host's main memory. The model 25 is 1.5-in high and comes with 20-, 40-, 60-, and 80-Mbyte capacities. The Model 35 is 2.5-in. high and has capacities ranging to 750 Mbytes. 20-Mbyte Model 25, $399; 40-Mbyte Model 35, $499. **BSE Co,** 1622 Edinger Ave, Suite F, Tustin, CA 92680. Phone (714) 258-8722. FAX (714) 258-8815. **Circle No. 374**

I²C bus adapter. With the ICA-90 I²C serial-bus adapter for the ISA bus, you can select one of eight I/O addresses and one of four interrupts for the half-length card. The card employs the Philips PCD8584 bus-controller chip and supports the 2-wire I²C protocol. The board operates as a master or slave in receiver and transmitter modes. Popular languages can either poll or interrupt the board. The board interfaces to the bidirectional serial-data and serial-clock lines through a 9-pin D-style connector. $299. **The Saelig Co,** 1193 Moseley Rd, Victor, NY 14564. Phone (716) 425-3753. FAX (716) 425-3835.

Circle No. 375

80386 single-board computer. The CAT990 single-board computer for passive ISA or EISA bus backplanes employs a 25-MHz or 33-MHz 80386 μP and 1M to 32 Mbytes of dynamic RAM. The board achieves a Landmark v1.14 speed rating of 41.0 when operating at 25 MHz and 54.1 when operating at 33 MHz. An onboard cache controller manages 64 or 128 kbytes of cache RAM. Peripheral controllers interface to IDE/AT hard-disk and floppy-disk drives. 25-MHz version without RAM, $1345; 33-MHz version without RAM, $1495. **Diversified Technology Inc,** Box 748, Ridgeland, MS 39158. Phone (800) 443-2667; (601) 856-4121. FAX (601) 856-2888. TLX 585326. **Circle No. 376**

Frame grabber. The HI*DEF II HS frame-grabber-board 2-board set has an effective sampling rate of 55 MHz in single-pass and 110 MHz in dual-pass mode. The boards can simultaneously accommodate data from one digital and four independent analog video sources. You can program the sampling rate from 2 to 110 MHz to capture analog video signals at various resolutions. $5490. **Imagraph Corp,** 11 Elizabeth Dr, Chelmsford, MA 01824. Phone (508) 256-4624. FAX (508) 250-9155. TLX 4946300. **Circle No. 377**

Stepper motor controller. The nuStep stepper-motor-controller board for the NuBus permits a Macintosh II computer to control 3 axes of motion at programmable step rates as fast 750,000 steps/sec. A 68000 μP controls unipolar and bipolar motor drivers in

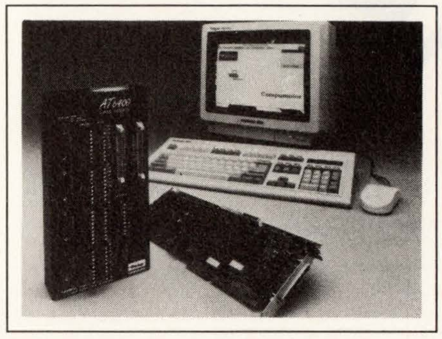
real-time open- or closed-loop systems. $1595. **nuLogic Inc**, 475 Hillside Ave, Needham Heights, MA 02194. Phone (617) 444-7680. FAX (617) 444-2803.
Circle No. 378

Token Ring bridge. The Plexbridge 8039 bridge connects to 4-Mbps or 16-Mbps Token Ring networks. The bridge employs the Simple Network Management Protocol (SNMP) to manage compliant network-management stations. The bridge implements the Spanning Tree algorithm, which automatically determines the most efficient network route, and it accommodates multiple parallel paths and hops. $4495. **Plexcom Inc**, 65 Moreland Rd, Simi Valley, CA 93065. Phone (805) 522-3333. FAX (805) 583-4764. **Circle No. 379**

Console-to-computer switch. The SC-6X3-15V6M matrix switch connects six consoles to three computers. The consoles can consist of VGA monitors and keyboards having 6-pin miniDIN connectors. A remote switch-control unit, the RMT-3C, can be located 500 feet away. Switch, $2700; remote control, with 25-ft cable, $105. **Network Technologies Inc**, 7322 Pettibone Rd, Chagrin Falls, OH 44022. Phone (800) 742-8324; (216) 543-1646. FAX (216) 543-5423. **Circle No. 380**

Media attachment unit. The 2100 ultraminiature MiniMAU allows an attachment-unit interface on data-terminal equipment to transmit and receive data on a 10Base-T, twisted-pair, Ethernet network. It doesn't require ac or battery power and conforms to the IEEE-802.3 and FCC Class A standards. The unit measures $2 \times 1.68 \times 0.79$ in. and comes in a plastic case with LED status indicators. $89. **Patton Electronics Co**, 7958 Cessna Ave, Gaithersburg, MD 20879. Phone (301) 975-1000.
Circle No. 381

Ethernet adapter. The Pocket Print Server enables a printer to connect directly to a 10Base-T Ethernet network. The unit attaches to the printer's parallel port and transfers data at 60 kbytes/sec. The adapter is compatible with Novell's Print Server standard software and supports Novel Netware 2.15 and Netware 386 protocols. $495. **Extended Systems,** 6123 N Meeker Ave, Boise, ID 83704. Phone (208) 322-7575. FAX (208) 377-1906. **Circle No. 382**



Stepper motor controller. The AT6400 stepper motor controller for ISA bus computers can synchronize 2, 3, or 4 axes of motion and accept incremental-encoder-feedback signals on all four axes. The controller has 24 programmable I/O ports. Its software command language features feed-rate override, 2-axis contouring, conditional programming, unit scaling, registration, and mathematical functions. $2275. **Parker Hannifin Corp**, Compumotor Div, 5500 Business Park Dr, Rohnert Park, CA 94928. Phone (800) 358-9070; (707) 584-7558. FAX (800) 328-8087.
Circle No. 383

386DX single-board computer. The TEK-AT3 contains a 33-MHz 80386 µP; 1, 4, or 16 Mbytes of dynamic RAM; 2 Mbytes of solid-state disk RAM; 1 Mbyte of flash EPROM; and 1 Mbyte of static RAM with battery backup. In addition, the board has hard- and floppy-disk-drive controllers; two serial ports; and 1 parallel port. The board plugs into a passive 16-bit ISA bus backplane, and its all-CMOS design consumes 6W typ. $1495. **Teknor Microsystems Inc**, CP 455, Sainte-Therese, Quebec, Canada J7E FJ8. Phone (514) 437-5682. FAX (514) 437-8053.
Circle No. 384

Signal-conditioning board. The VMIVME-3413 conditions signals from 32 low-level analog sources. The conditioned signals are compatible with the company's VMIVME-3112 and VMIVME-3118 scanning A/D boards. Each channel accepts differential or single-ended inputs and has jumper-selectable gain adjustments of $\times 1$, $\times 10$, $\times 100$, or $\times 1000$. Each channel also has a 3-pole lowpass filter, which is adjustable from 4 Hz to 10 kHz. $1695 to $2375. **VME Microsystems International Corp,** 12090 S Memorial Pkwy, Huntsville, AL 35803. Phone (800) 322-3616; (205) 880-0444. FAX (205) 882-0859.
Circle No. 385

i960CA Emulator

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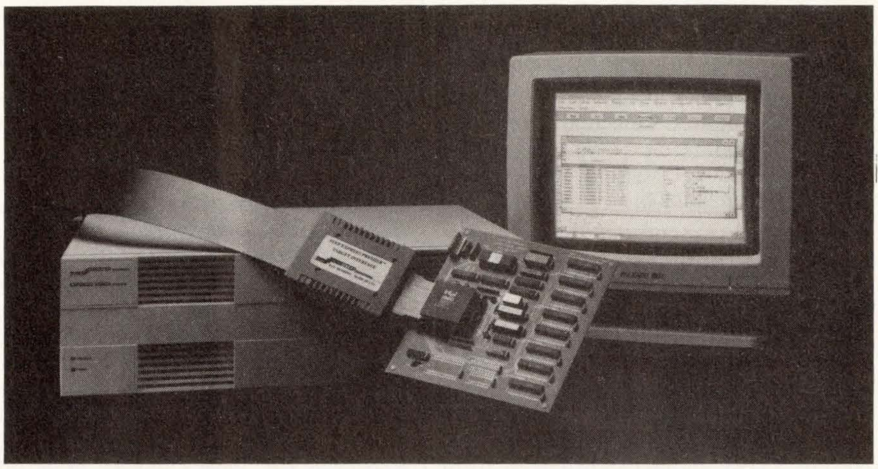

The Express III emulator for the i960CA µP performs more complete cache analysis than did earlier instruments. In addition, it couples its logic-analyzer-style triggering to the µP's cache and uses the IC's on-chip debugging facilities to detect trigger conditions and to control program execution from cache. Among the emulator's features are a 32k×256-bit trace buffer with passive trace and time stamping; multilevel hardware and software triggering that includes store-control facilities; 71 hardware-range matchwords and breakpoints; performance-analysis capabilities; and an integrated MS-Windows-based debugger with a graphical user interface. $35,000.

Step Engineering Inc, Box 3166, Sunnyvale, CA 94088. Phone (800) 538-1750; (408) 733-7837. FAX (408) 773-1073. TWX 910-339-9506.

Circle No. 386

Analog signature-comparison tester. The Pro-line 5300 autotracer is an analog signature-comparison tester that—without applying dc power—isolates failed components on pc boards containing analog, digital, and mixed-signal devices. The unit also works with diodes, transistors, resistors, inductors, capacitors, regulators, and ICs not mounted on boards. An MS-DOS PC stores signatures measured at various nodes of a known-good board. The tester measures as many as eight signatures at a node (four impedance levels, two frequencies). An autoranging feature then selects the most meaningful of these signatures for permanent storage. From $4500. **Maxtec International Corp,** 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448.

Circle No. 387

6-slot VXIbus chassis. The 1246U has a hinged front panel and a removable outer shell. It has a 450W power supply and cooling that removes 55W per slot. $3875. Delivery, four to six weeks ARO. **Racal-Dana Instruments Inc,** 4 Goodyear St, Irvine, CA 92718. Phone (800) 722-3262. FAX (714) 859-2505. **Circle No. 388**

ISA bus IEEE-488.2 interface. The KPC-488.2 transfers data as fast as 1.5 Mbytes/sec. A built-in bus analyzer lets you track down bus problems without special instruments. Software support is provided for MS-DOS, MS Windows 3.0, SCO Unix, and OS/2, and for several Microsoft and Borland languages. $495. **Keithley Metrabyte,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 389**

ISA bus data-acquisition board. Model 30 has 24 lines of TTL I/O, an 8-channel multiplexer, an 8-bit ADC, and a 12-bit counter. It comes with sample programs on a 5¼-in. floppy disk. You can get it with open-collector TTL drivers that handle 30V and 0.5A. $79. **Prairie Digital Inc,** 846 17th St, Prairie du Sac, WI 53578. Phone or FAX (608) 643-8599. **Circle No. 390**

PC-based in-circuit emulator. The Emul16/300PC consists of an ISA bus emulator board containing 1 Mbyte of shadow RAM, a 5-ft twisted-pair ribbon cable, a pod board containing 1 Mbyte of breakpoint RAM, and an optional trace board. You can display the contents of the shadow RAM while the emulator continues to run at full speed. $1995; pod $1995. **Nohau Corp,** 51 E Campbell Ave, Campbell, CA 95008. Phone (408) 866-1820. FAX (408) 378-7869. **Circle No. 391**

L-C-R meter. The HP 4263A LCR meter measures inductance (L), capacitance (C), and resistance (R) from 100 Hz to 100 kHz. Inaccuracy is 0.1% and resolution is five digits. Using option 001 transfer-measurement function, the unit quickly displays parameters of low-frequency transformers. LCR meter, $3800; transformer test fixture, $540; option 001, $660. Delivery, six weeks ARO. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 392**

Capacitance meter. The JAC-380123 measures 0.1 pF to 20,000 µF in nine ranges. The 7.3×3.4×1.5-in. unit is bright yellow and weighs 10 oz; its LCD has 0.7-in.-high characters. $99. **Extech Instruments Corp,** 335 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. FAX (617) 890-7864. **Circle No. 393**

350-MHz PQFP probe adapter. This adapter for testing high-speed devices comes in 100-pin plastic quad flatpacks. It fits over the device under test and provides a 100-pin pin-grid-array socket for connecting probes. Removable pins let you connect to retractable probe tips or to a logic analyzer's square-pin adapters. $260. **Tektronix Inc,** Box 1520, Pittsfield, MA 01201. Phone (800) 426-2200. **Circle No. 394**

4-channel thermal-array chart recorder. The 31-lb Easygraf 4-channel recorder has a printhead with a dot pitch of 4 dots/mm. Chart speeds range from 0.01 to 125 mm/sec. Frequency response extends to 500 Hz. The unit accepts plug-in signal conditioners. Recorder, $5495; signal conditioners, from $315/channel. **Gould Inc,** 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7000. FAX (216) 328-7400. **Circle No. 395**

Visual-inspection system. The AV-560 benchtop system inspects pc boards produced in moderate volume and contains surface-mount components. It handles boards as large as 12-in. square and includes a high-resolution color video display. $23,500. **Benchmark Industries Inc,** 215 St Anselm's Dr, Goffstown, NH 03045. Phone (603) 627-8484. FAX (603) 627-6788. TLX 881404. **Circle No. 396**

VMEbus digitizers. The Comet 6U-size VMEbus board holds four ADCs. You can select converters that digitize to 12 bits at 1, 2, or 5 Msamples/sec. A board with four 5-Msamples/sec ADCs can acquire single-channel data at 20 Msamples/sec. Each converter has 64k words of acquisition memory. Board with four 5-Msamples/sec ADCs, $2444 (100). **Omnibyte Corp,** 245 W Roosevelt Rd, West Chicago, IL 60185. Phone (708) 231-6880. FAX (708) 231-7042. **Circle No. 397**

Data-acquisition software. DAQware runs with the vendor's ISA bus, EISA bus, and data-acquisition boards for the Micro Channel bus, and is included in the price of these boards. Besides displaying data in strip-chart format and producing arbitrary waveforms, it stores data on disk in binary, ASCII, and Lotus 1-2-3 formats. The vendor will supply the source code on request at no extra charge. LabWindows package, $695. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in USA and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 398**

100-MHz logic-analysis card set. The combination of an HP 16540D and one to four 16541Ds equip the vendor's 16500 logic-analysis systems to do 100-

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Test set for European cellular phones. The HP 8922G test set performs protocol, signaling, and bit-error-rate tests on European digital cellular telephones that conform with the GSM (Group Speciale Mobile) standard. \$79,000. Delivery, eight weeks ARO. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 400**

Frequency synthesizer. The SI-102 frequency synthesizer provides 5½-digit resolution from 0.1 Hz to 16 MHz. From 0 to 50°C, the output frequency is stable to ±10 ppm (±1 ppm optional). The output will drive a 50Ω load. \$779. **Syntest Corp,** 40 Locke Dr, Marlboro, MA 01752. Phone (508) 481-7827. FAX (508) 481-5769. **Circle No. 401**

Drivers for Turbo C and Pascal. NI-DAQ DOS and NI-DAQ Windows help you write Turbo C and Turbo Pascal programs that control and acquire data with 20 types of the vendor's ISA bus and Micro Channel Architecture bus data-acquisition boards. The driver packages accompany the boards at no extra charge. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in USA and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 402**

Analog-output boards for 16-bit ISA bus. The AT-AO-6 analog-output board has six multiplying DACs, and the AT-AO-10 analog-output board contains ten multiplying DACs; both boards accept 200,000 updates/sec. They boards also have voltage references for the DACs. Each channel has a 4-to-20-mA current output and a voltage output that can be either unipolar or bipolar. AT-AO-6, \$895; AT-AO-10, \$1295. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in USA and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 403**

Data-logger software. The Hydra data-logger application software package works with the vendors' data-acquisition instruments and runs under MS Windows. The package allows you to create custom interfaces using a spreadsheet such as Excel or 1-2-3 for Windows. \$350. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. **Circle No. 404**
Philips Test and Measurement, Bldg TQIII-4, 5600 MD Eindhoven, The Netherlands. **Circle No. 405**

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Datalight, 17455 68th Ave NE, Suite 304, Bothell, WA 98011. Phone (800) 221-6630; (206) 486-8086. **Circle No. 407**

Unix for 386/486. Version 3.0 is a new release of the Interactive Unix System V Release 3.2 for Intel's 80386 and 80486 processors. Enhancements allow easier use and also include support for additional hardware, including the EISA architecture and foreign languages. The user interface features pull-down menus and pop-up dialogue boxes and forms that guide you through operations such as system installation, kernel configuration, copying disks, configuring printers, adding users, and installing applications. Single-user system, $495; multiuser extension, $400. **Interactive Systems Corp,** 2401 Colorado Ave, Santa Monica, CA 90404. Phone (800) 346-7111; (213) 453-8649, ext 3130. FAX (213) 828-6453. TWX 910-343-6255. TLX 182030. **Circle No. 408**

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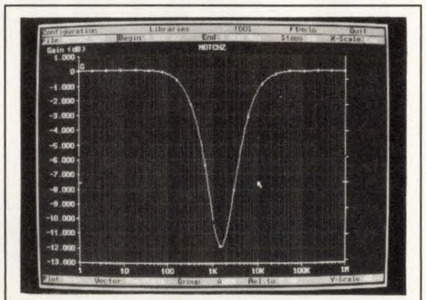

Unix for 68040 VME. A version of Unix System V Release 4 is now available for the supplier's 68040-based VMEbus single-board computers. The software conforms to the IEEE 1003.1 specification developed by the Posix standards committee. $3000. **Radstone Technology,** 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; (201) 391-2700. FAX (201) 391-2899.

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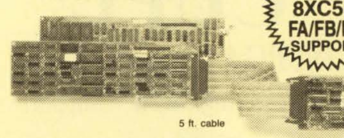

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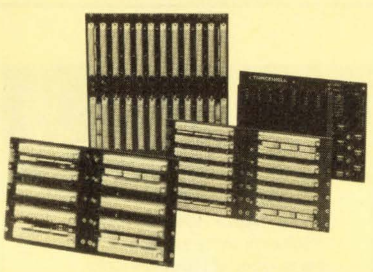

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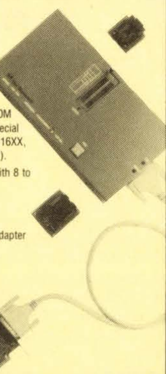

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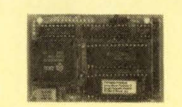

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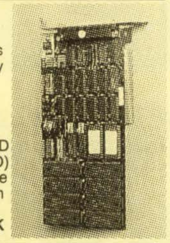

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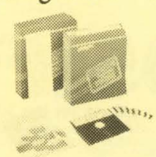

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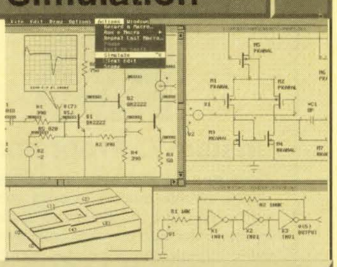

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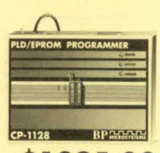

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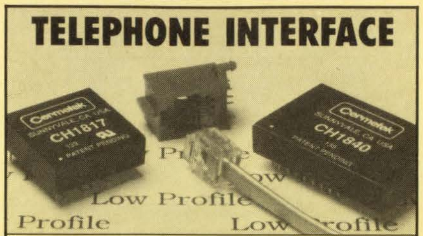

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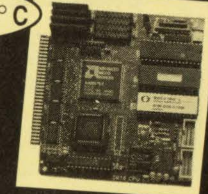

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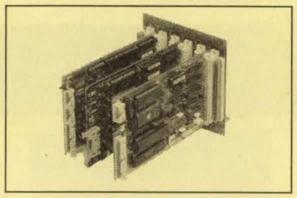

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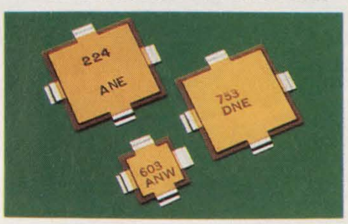

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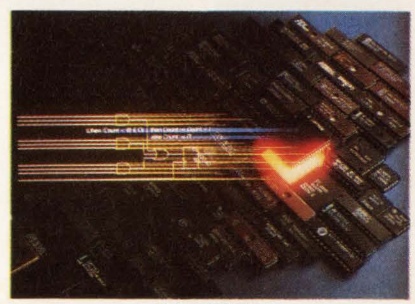

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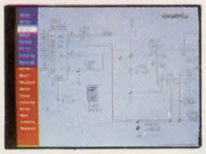

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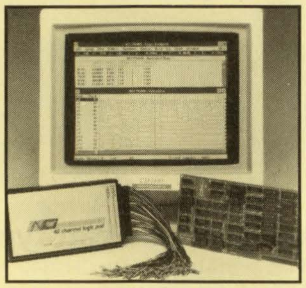

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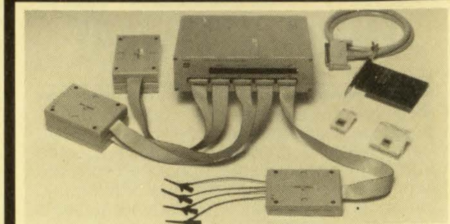

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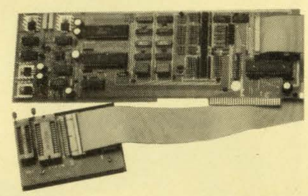

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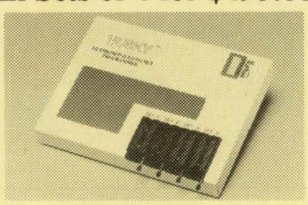

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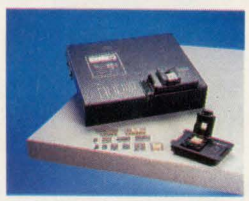

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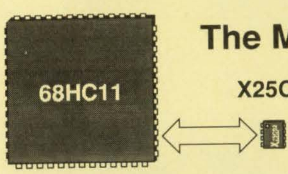

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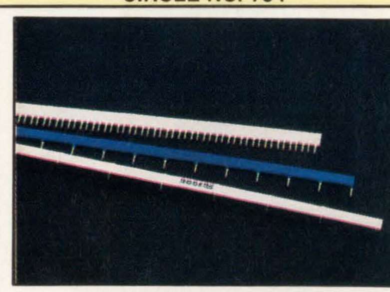

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Issue	Issue Date	Ad Deadline	Editorial Emphasis
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Magazine Edition	Mar. 2	Feb. 6	COMMUNICATIONS SPECIAL ISSUE • Test & Measurement • Local-area Networks • Microprocessors Memory Technology
News Edition	Mar. 5	Feb. 20	Memory Technology • CPU Boards • Computers & Peripherals • Diversity Special Series
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DESIGN DRAFTSMAN/PCB DESIGNER

A minimum of five years experience with electronic equipment design and packaging is mandatory. Familiarity with castings, PCBs, schematics, wire lists, assembly drawing, parts lists, component parts, SCDs and detail drawings. Familiarity with the following specifications is required: ANSI Y14.5M-1982, DOD-D-1000, DOD-STD-100, MIL-STD-275, MIL-STD-2000, and MIL-STD-2175. Extensive experience in documentation of military drawings utilizing Computervision Cadds 4x with 3-D modeling as well as a Scicards cad station for circuit card assembly design and documentation is required. Tasks will include updating and creating mechanical drawings and parts lists as well as PCB layout and documentation.

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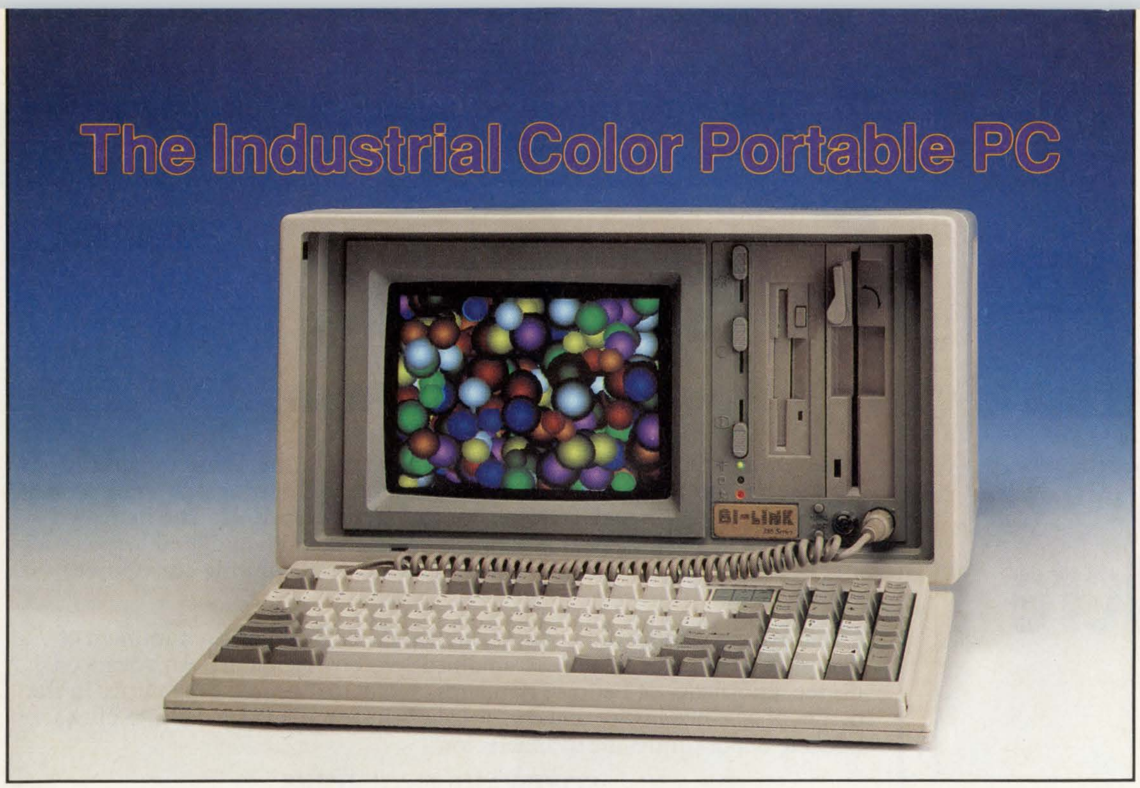

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EDN·ACRONYMS & ABBREVIATIONS

ADC—analog-to-digital converter
ALU—arithmetic logic unit
ASIC—application-specific integrated circuit
BiCMOS—bipolar and complementary metal-oxide semiconductor. An integrated-circuit process technology that combines bipolar and metal-oxide transistor types.
CMOS—complementary metal-oxide semiconductor. An integrated-circuit technology that uses two metal-oxide transistors of differing polarities in pairs as the basic design element. Logic circuits built from such elements have a logic threshold midway between the device's power and ground voltages.
CPU—central processing unit
CQFP—ceramic quad flatpack
DIP—dual in-line package
DMA—direct memory access
DRAM—dynamic random-access memory
DSP—digital signal processing
ECL—emitter-coupled logic
EEPROM—electrically erasable programmable read-only memory
EFIR—equiripple finite-impulse-response filter
EMI—electromagnetic interference
EPLD—erasable programmable logic device
EPROM—erasable programmable read-only memory
FIR—finite-impulse-response filter
FPGA—field-programmable gate array
GUI—graphical user interface
I/O—input/output
IC—integrated circuit
ICE—in-circuit emulator
IEEE—Institute of Electrical and Electronics Engineers
IIR—infinite-impulse-response filter
JTAG—Joint Test Action Group. A subcommittee of the IEEE with the charter to develop standards for embedding test circuits into integrated circuits.
LCC—leadless chip carrier
LCD—liquid-crystal display
LED—light-emitting diode
MAC—multiply and accumulate unit
MMU—memory-management unit
OS—operating system
pc board—printed-circuit board
PGA—pin-grid array
PLCC—plastic leaded chip carrier
PQFP—plastic quad flatpack
PROM—programmable read-only memory
PWM—pulse-width modulator
QFP—quad flatpack
RAM—random-access memory
RGB—red, green, blue—analog color signals to a cathode-ray tube
RISC—reduced-instruction-set computer
ROM—read-only memory
SOIC—small-outline integrated circuit
SOP—small-outline package
SQFP—shrink quad flatpack
SRAM—static random-access memory
SSOP—shrink small-outline package
TSOP—thin small-outline package
TTL—transistor-transistor logic. A design technique that uses bipolar transistors. Logic circuits designed using this technique have a static threshold of 1.5V.
UART—universal asynchronous receiver transmitter
ZIP—zig-zag in-line package

EDN·INTERNATIONAL ADVERTISERS INDEX

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Put this PLD text on your library shelf

Here is a book that gives an excellent introduction to programmable logic devices (PLDs). Although the authors of *Practical Design Using Programmable Logic* claim to be industry "insiders," they write thoughtfully for engineers and for managers who might know little about PLDs. You won't get lost in complex device descriptions or in examples that only experts could fathom.

The authors start with an overview of the origins of PLDs, a nice touch that sets the stage for an introduction to device technologies and simple devices and architectures. The book includes chapters on design and development tools and on high-level design techniques. You'll also learn about field-programmable gate arrays (FPGAs), which are becoming more and more popular. Appendices list acronyms and device and design-tool manufacturers.

If you need a detailed and technical understanding of PLDs, you won't find it here, but that isn't what the authors had in mind when they wrote the book. Instead, you'll get a thorough overview of what PLDs can do, what you need to think about before deciding to use them, and design implications of various architectures. I recommend this book to engineering or project managers who need to know what their engineers are talking about, and to engineers who are approaching a PLD project for the first time. Engineers who are using simple PLDs such as the 16L8, 16R8, or derivatives, and who want to move on to more complex devices, will find much useful information in this book, which is worth having in your library.—**Jon Titus**

Practical Design Using Programmable Logic, David Pellerin and Michael Holly, Prentice Hall, Englewood Cliffs, NJ 07632, USA, 1991, 385 pgs, $43.

Real-world wisdom for setting up data-acquisition PCs

The book, *Data Acquisition Techniques Using Personal Computers* by Howard Austerlitz, is a mix of tutorial and reference information for engineers setting up or using a PC-based data-acquisition system. Spanning many disciplines, this well-illustrated book gives readers enough information to build a system from scratch or to simply piece together appropriate commercial hardware and software products.

The book, broken into 14 chapters, contains diverse information rarely found in a single source. It begins with an introduction to data acquisition and describes why a PC is such a useful tool for acquiring, analyzing, and displaying data. The major topics cover transducers, analog signal conditioning, analog/digital conversions, personal-computer hardware and software, programming languages, and signal-processing techniques. In addition, the book discusses standard interfaces, such as RS-232C, Centronics, and IEEE-488, as well as special topics such as data-compression techniques.

This text contains detailed information on the IBM PC/XT/AT family of computers and their clones, including reference tables of memory maps, I/O address maps, and BIOS functions. The book discusses the PC/XT and PC/AT (ISA) buses in great detail and presents timing diagrams and sample circuit diagrams of hardware interfaces.

One chapter in the book covers other personal-computer families suitable for data acquisition: IBM's MCA-based PS/2 machines and Apple's NuBus-based Macintosh II computers.

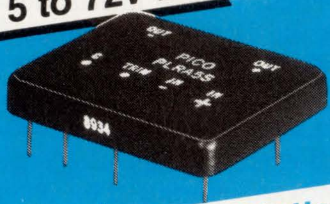
In line with stressing IBM-compatible hardware, the author discusses the MS-DOS software environment in great detail. This book contains tutorial information on using MS-DOS for those unfamiliar with PCs, but it also covers more advanced topics, such as disk and file structures. Program listings and examples support the author's software-interfacing techniques.

For engineers who don't want to design their own hardware or software, the book contains descriptions of commercially available hardware and software products from several major vendors, such as Keithley Metrabyte and Laboratory Technologies. The author includes guidelines on how to choose the appropriate hardware or software product for your application, and he gives specific examples. The appendices contain listings of commercial data-acquisition product manufacturers.

The final chapter provides examples of real-world applications for PC-based data acquisition. One application is an ultrasonic measurement system as an example of high data rates. Another is an electrocardiogram measurement system, which uses low data rates.

The author provides frequent examples to explain topics. The subject matter can vary from following a sigma-delta ADC's conversion process cycle by cycle to an example of Huffman encoding, which illustrates how to design a code tree and calculate the data-compression ratio.

A large number of figures and tables supplement the wide-ranging contents of this book, which also contains many illustrative program listings, mostly in C, assembler, and Basic. *Data Acquisition Tech-*



niques Using Personal Computers is a useful book for anyone who wants to use their PC to acquire, analyze, or display data.

—**Charles H Small**

Data Acquisition Techniques Using Personal Computers, Howard Austerlitz, Academic Press, Harcourt Brace Jovanovich, Department #11029, 1250 Sixth Ave, San Diego, CA 92101, (800) 321-5068, 306 pages, ISBN: 0-12-068370-9, Hardcover, $59.95.

Taking this bus isn't worth the trip

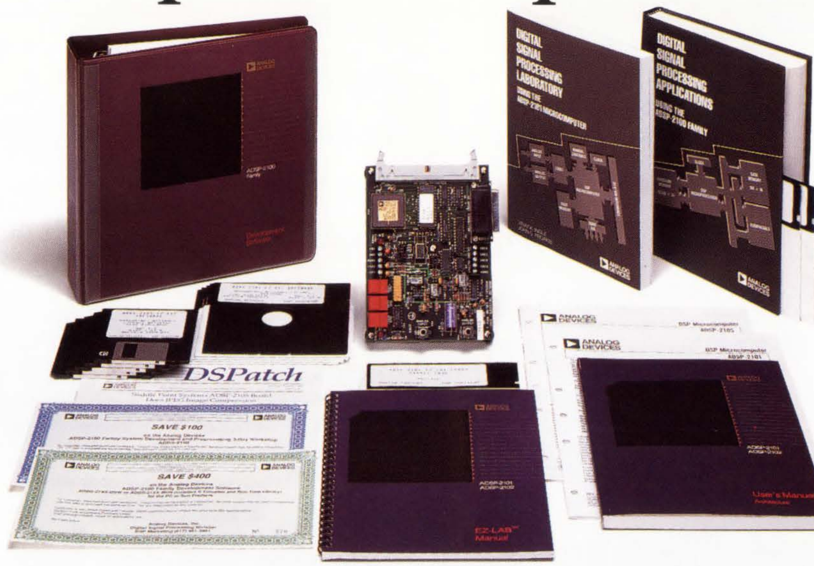
When it comes time to learn about computer buses, steer clear of *Microcomputer Buses* by R M Cram. Although the book promises information on popular computer buses, all you get is a quick overview and few of the necessary details of bus design.

For example, the book spends only six pages on VMEbus arbitration. In fact, the book devotes only 126 pages to describing real bus architectures. Although the book includes quite a bit of introductory information and two chapters on programmable logic devices (PLDs) and field-programmable gate arrays (FPGAs), you can find that information elsewhere and in much more detail. Two final chapters cover real examples of bus-interface circuits, but instead of describing how to design such circuits, the author simply dissects commercial designs. You'll learn how those specific designs work, but little more.

To learn more about computer buses, look for another book. You can also contact bus-product manufacturers for application notes and talk with industry groups that support bus standards.—**Jon Titus**

Microcomputer Buses, R M Cram, Academic Press, San Diego, CA, 1991, 246 pgs, $49.95.

Our DSP development tool kit hammers the competition on performance.



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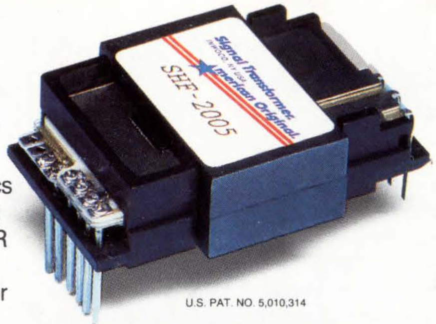

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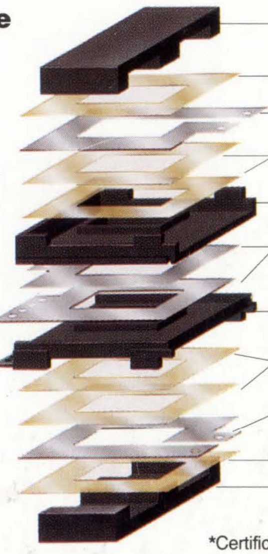

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