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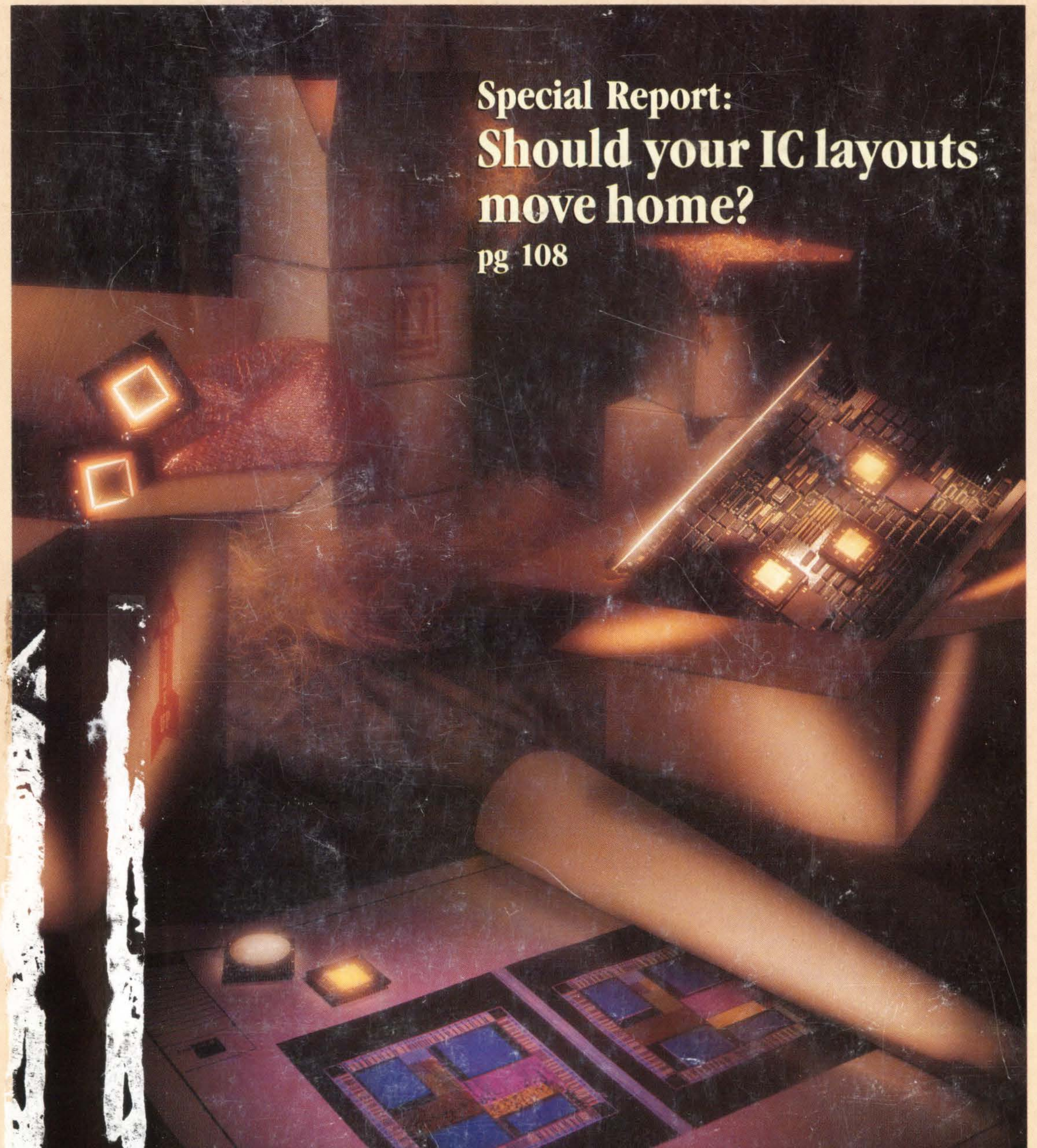
September 3, 1992

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

PROCESSOR UPDATES PG 97



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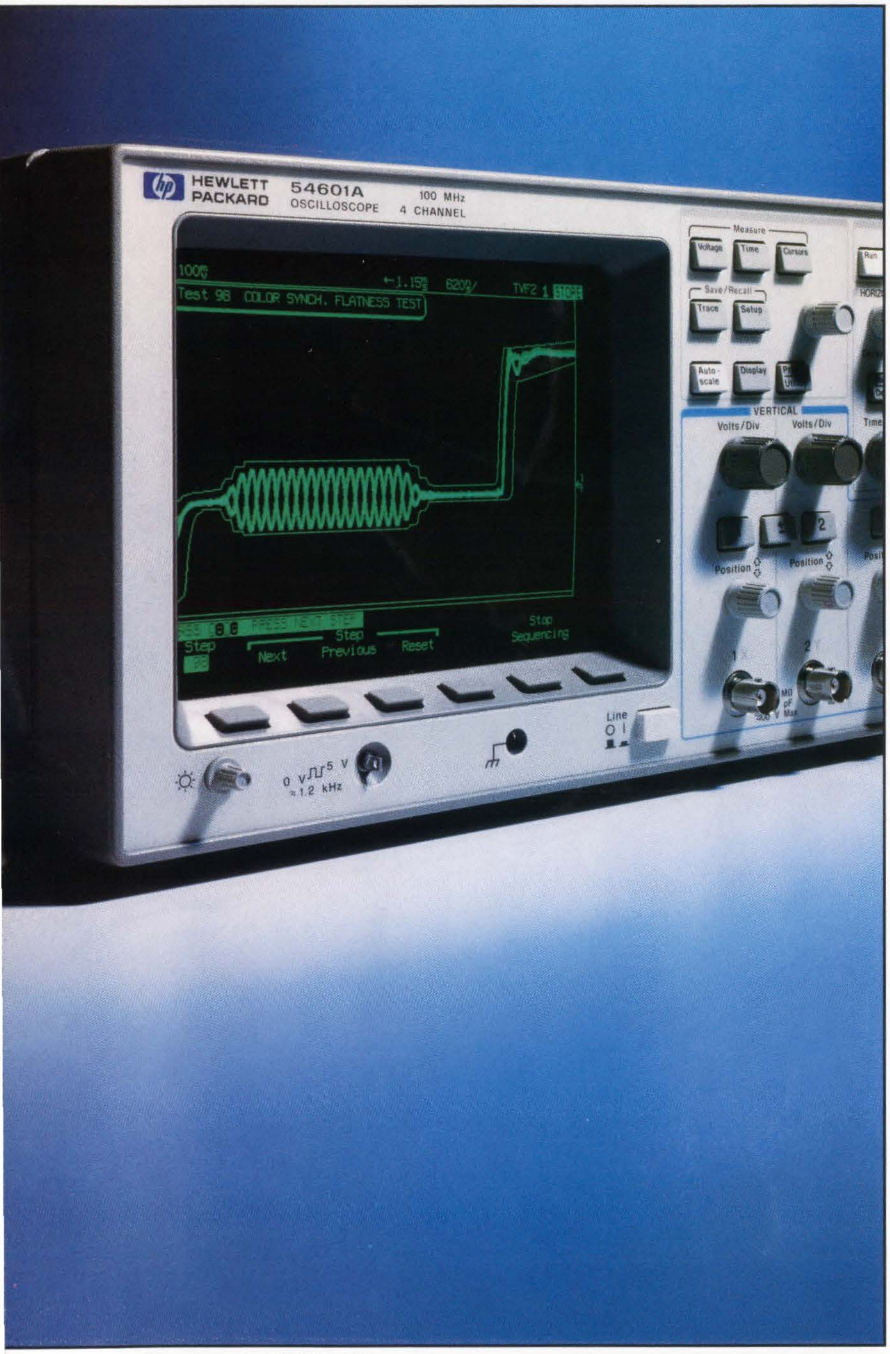

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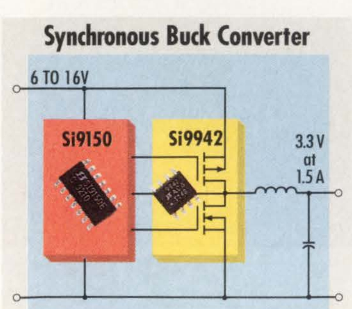

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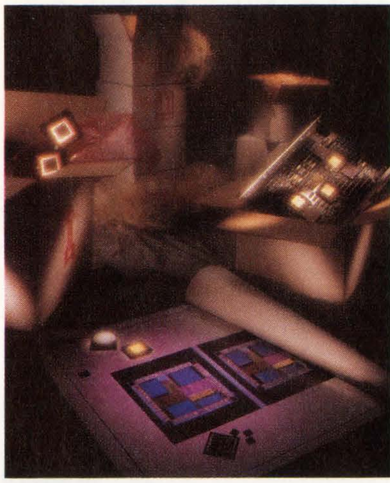
SEPTEMBER 3, 1992 VOLUME 37, NUMBER 18

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE



On the cover: Bringing IC layout in house could save you both time and money. Maybe it's time for you to buy your own place-and-route tools and move your IC layout back home. Photo courtesy LSI Logic; concept and photography by Imagination; accelerator board provided by Zycad . . . . **PAGE 108**

ASIC TECHNOLOGY SPECIAL ISSUE

Continued on page 7

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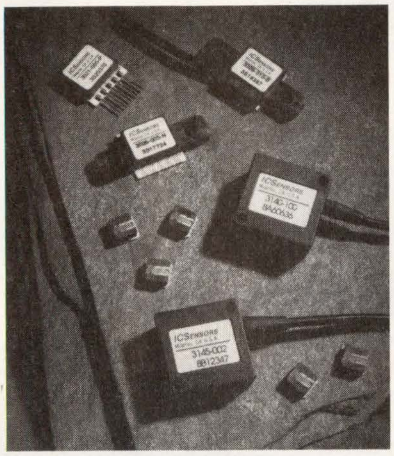

Low-cost precision accelerometers are now available that stem from adaptations of silicon-processing techniques used in the semiconductor industry. You can read more about these accelerometers on . . . . **PAGE 69**

TECHNOLOGY UPDATES

PRODUCT UPDATES

Continued on page 9

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PROCESSOR UPDATES

NEW PRODUCTS

DEPARTMENTS

INSIDE EDN

A summary and analysis of articles in this issue

Technical Editor John Napier introduces our ASIC Special Issue with his Special Report on doing **IC layout in house** rather than leaving it to a semiconductor fab. For fast, complex ICs, having a third party lay out your IC after you've finished the logical design can result in timing problems or other layout effects that might require you to rework the logic, thus delaying time to market. John explores the decision to invest in place-and-route tools to take full control of physical design and design verification.

Doing these tasks in house isn't cheap: Most place-and-route tools cost more than $50,000. But if an IC design has 50,000 gates or more, a 40-MHz or faster clock, submicron feature sizes, or high-performance compiled cells, doing the physical layout in house can shorten the design cycle. "Doing a large, high-speed design in a competitive length of time practically demands that you do IC layout in house," says John.

The future is now for Futurebus+ products, reports John Gallant in his **Futurebus+ update.** In response to the US Navy's prodding, the IEEE Futurebus+ committee approved and adopted five critical hardware documents in September 1991. The finalized documents spurred more than 20 manufacturers to finally introduce commercial products including chips, boards, backplanes, connectors, enclosures, and systems. Manufacturers demonstrated many of these products at Buscon West. At Buscon East, John says you can expect to see more Futurebus+ products including protocol chip sets.

IEEE working groups have developed several Futurebus+ spinoff technologies such as BTL (backplane-transceiver logic), the MESI cache-coherency protocol, the live-insertion mode, and processor-independent data-transfer protocols. John says that these tech-

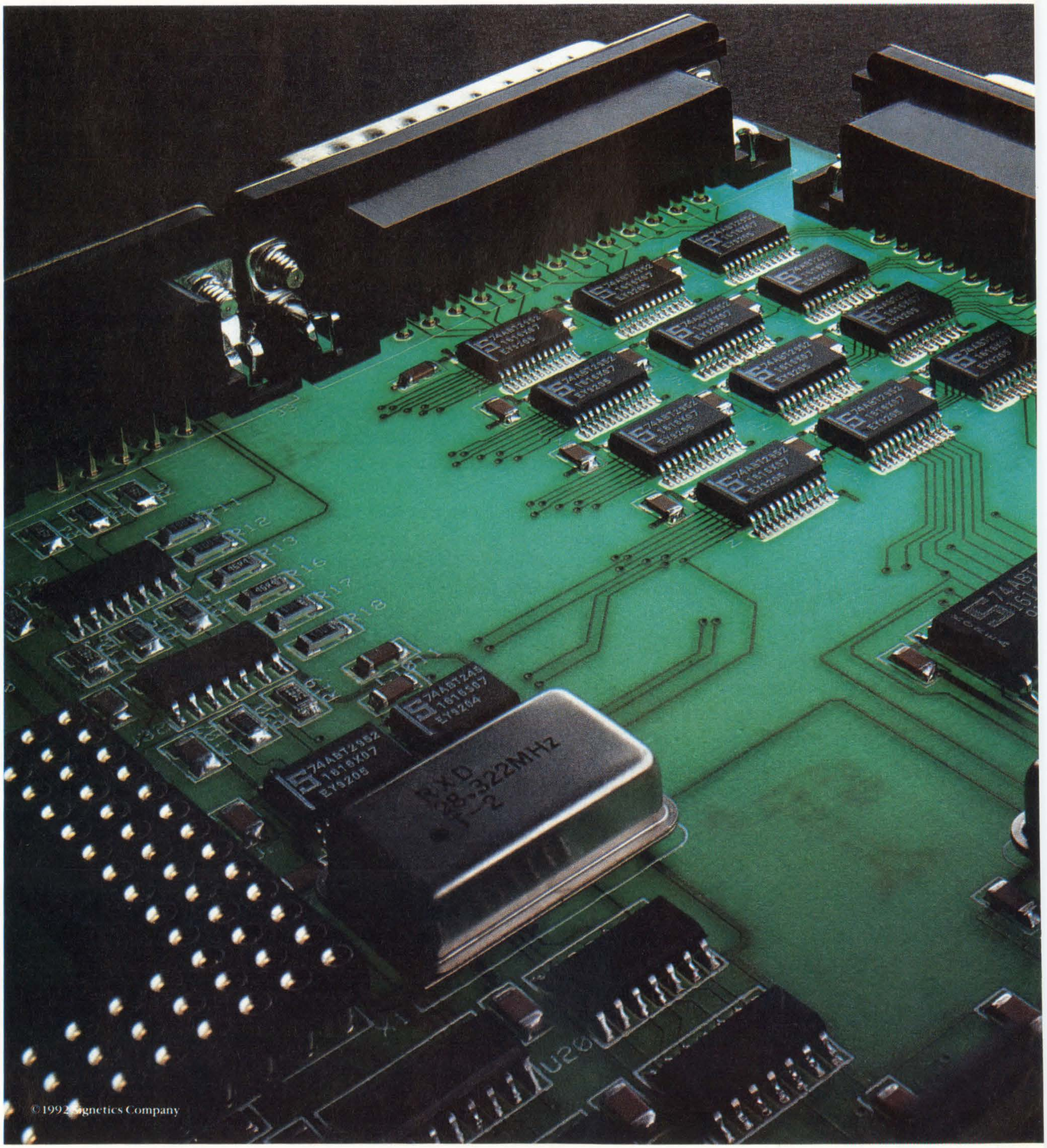
This issue's Special Report will help you decide whether to bring IC layout in house.

nologies will be the first fruits of more than a decade of design effort. "Because Futurebus+ is an open standard architecture, an independent designer can pay $20 to $35 to get one of the 25 or so current Futurebus+ documents and then implement the technology into custom designs," says John. "There are no fees, royalties, or licenses required. The system is wide open. That's the beauty of it."

Designers can also find a bargain on **silicon accelerometers.** In his Technology Update, Technical Editor Richard Quinnell says that these silicon sensors are tough, accurate, and newly affordable—prices range from $23 to $295. He also notes that the automotive industry is now a high-volume market for accelerometers. The sensors are used for deploying air bags and monitoring vibration in active suspension systems. Rich says this market is fueling accelerometer R&D and will likely lead to improved performance and still lower costs for all silicon accelerometers.

And after nearly a decade as a technical editor at EDN, Maury Wright has decided to call it quits and pursue other interests. His swan song is the Technology Update on **minicartridge tape drives**. Maury's expertise in computer drives of all sorts and his presence at EDN's annual editorial meetings will be missed.

Julie Anne Schofield
Senior Associate Editor


74ABT2952
1616X07
EY9205
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28.322MHz
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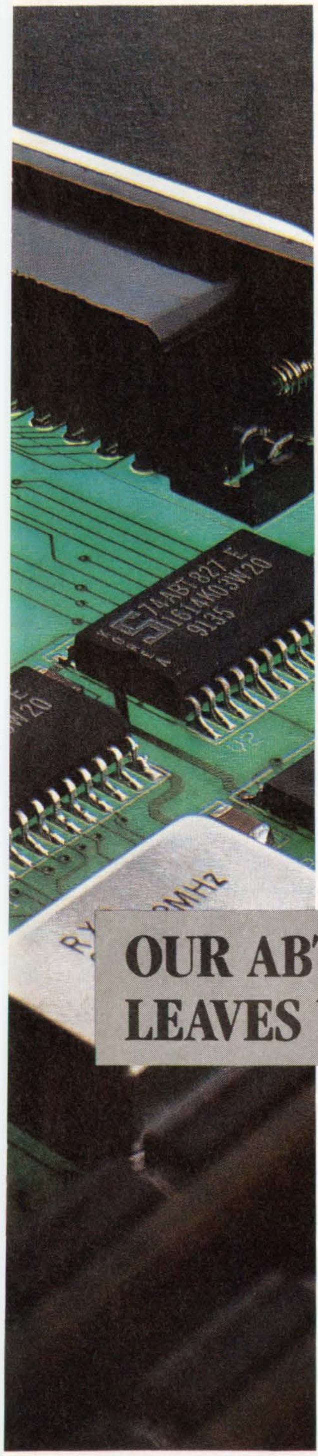

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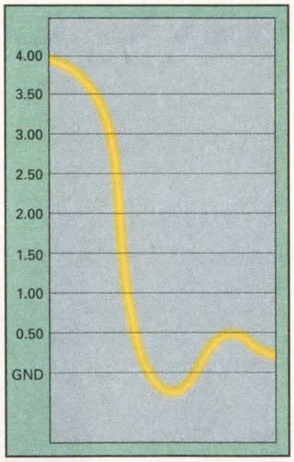
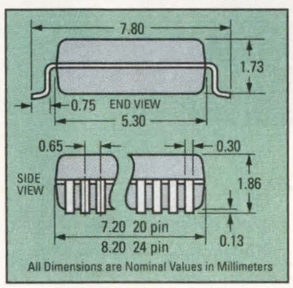


ABT in SSOP offers the highest performance while improving noise characteristics.



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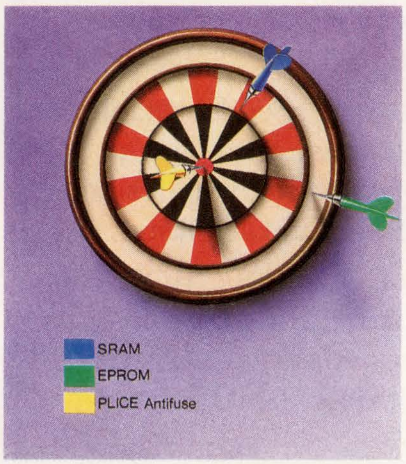

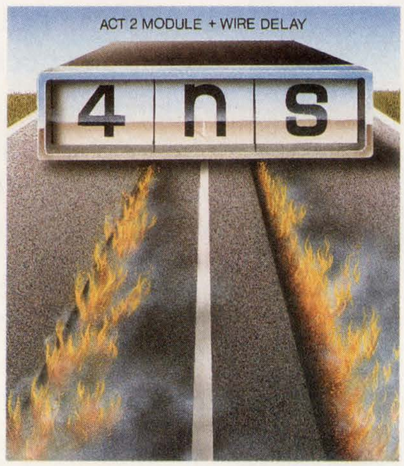

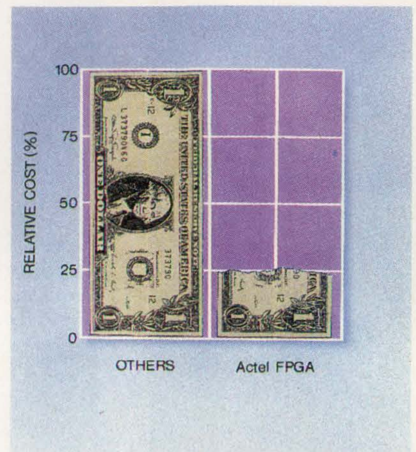

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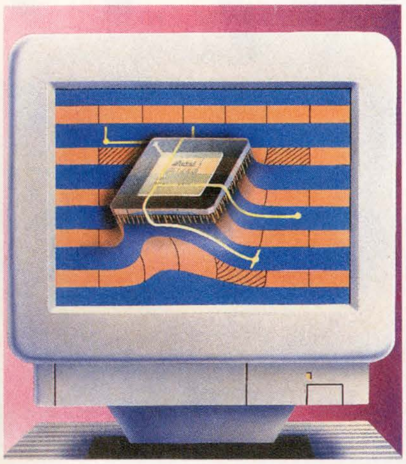

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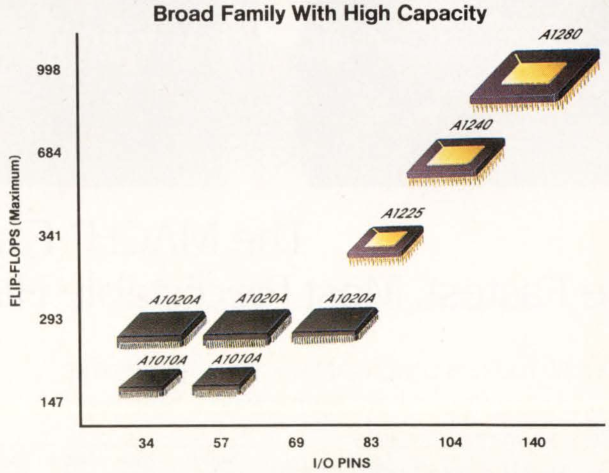

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Model Number	Equiv. Gates	Macro Cells	Max. Delay	System Speed	I/O Pins	Hard-Wired Option
MACH 110	900	32	12ns	66.7 MHz	44	MASC 110
MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120	1200	48	15ns	50 MHz	68	MASC 120
MACH 220	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230	3600	128	15ns	50 MHz	84	MASC 230

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Advanced Micro Devices

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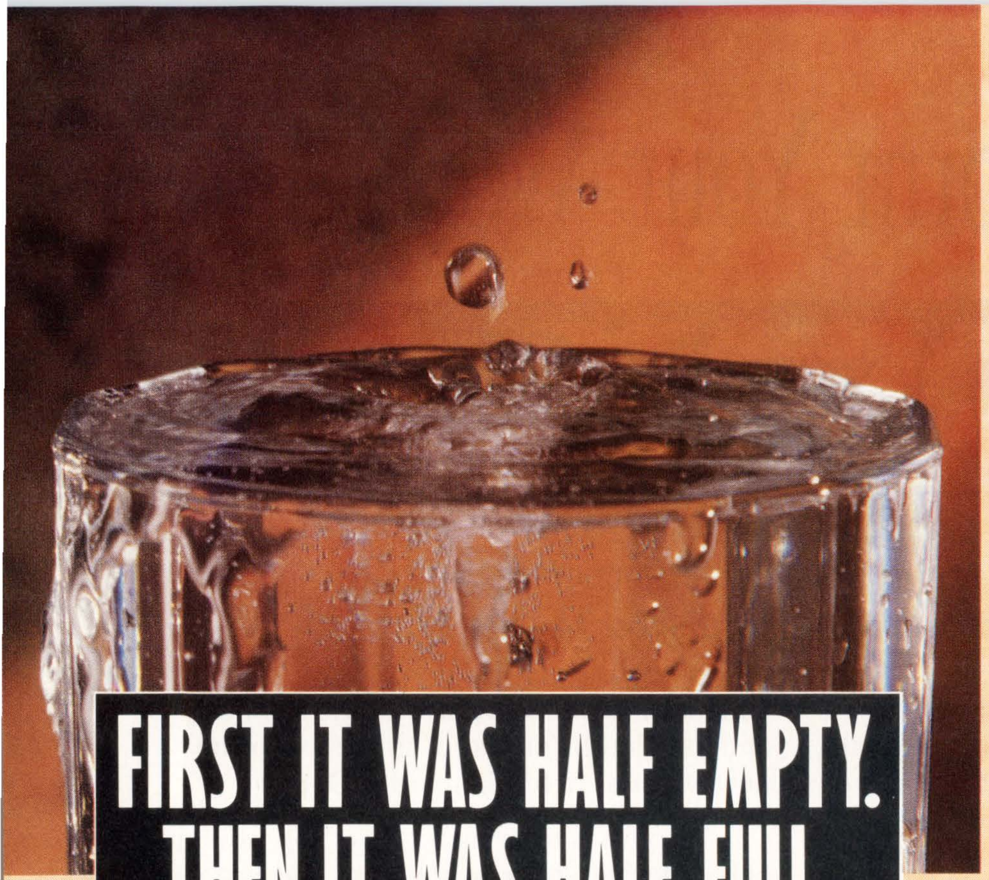

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THE REST IS HISTORY

CIRCLE NO. 20

EDITED BY SUSAN ROSE

Tool set automates software chores for C users

Ensemble from Cadre Technologies is a modular tool suite that automates software development, maintenance, and testing for C professionals. It gives you a common graphical user interface through which you access a range of functions for understanding, constructing, testing, and documenting your code. The tools let you rebuild complete, original code, including comments, in original files at any stage of processing. You can also call one module from another, without exiting, through incremental links.

The tool set includes six modules that you can purchase bundled for $23,000 or separately for the following prices per seat: System Understanding, $5500; Function Understanding, $3000; Construction, $5000; Test Case Generation, $6000; Test Verification, $3000 (shipping first quarter 1993); and Documentation, $3000.

The System Understanding tool creates structure charts and a data dictionary. The Function Understanding tool creates control flow graphs that diagram how the program uses functions. It also calculates complexity metrics for both data and control. The Construction module synchronizes design and code, letting you apply structured design to existing code. The Test-Case-Generation module automatically builds test cases at the function, unit, or subsystem level. The Test Verification module measures test coverage at the design, branch, and statement levels. It also graphically annotates control flow diagrams created by the Function Understanding Module. The Documentation module creates documents from the shared database, leveraging information stored by the other modules. Available now on Sun SPARC FCS. Available in the fourth quarter of 1992 on IBM, HP, and DEC workstations. Cadre Technologies Inc, Providence, RI, (401) 351-2273, FAX (401) 351-7380.

Units speed gang and set programming of ICs

Three moderately priced programmers, the PSX family, handle parallel programming of groups of ICs at speeds that the vendor claims come within a few percentage points of the theoretical maximum. Moreover, according to the vendor, the units' speed is from 2× to as much as 10× that of competitive units.

A major reason for the programmers' speed is their design. The sockets into which you insert the ICs to be programmed are part of "rails" that also include the output stage of the driver for each pin. Reducing the distance between the output stages and the ICs cuts the inductance of high-current leads and reduces delays and ringing that can slow programming. Careful attention to layout has also minimized the time operators need to load and unload ICs. Three types of rails accommodate memory devices and microcontrollers in a variety of through-hole and surface-mount packages. Each rail accommodates as many as ten ICs, depending on the package. The programmers, which accept one or two rails and as much as 16 Mbytes of data memory, cost from $2950 to $4950 (with 1 Mbyte). The rails cost from $3500 to $5500 each. Data I/O Corp, Redmond, WA, (206) 881-6444, FAX (206) 881-6856.

Testers let you learn causes of EMI failures

A soon-to-be-announced series of modular test systems will significantly reduce the effort required to find the exact causes of equipment's susceptibility to electromagnetic interference (EMI). With the systems, you'll be able to investigate the causes of susceptibility to electrostatic discharge (ESD), electrical fast transients (EFTs), surges, and power-line disturbances. The ECAT systems let you connect optically isolated μP-based data-acquisition modules to circuit nodes within the equipment under test; you can then gather data—even low-level analog signals—while other modules apply simulated threats: for example, pulses with kilovolt peak voltages and kiloampere peak currents. System pricing begins at $22,630. Keytek Instrument Corp, Wilmington, MA, (508) 658-0880, FAX (508) 657-4803.

Digital-analysis system runs on networks

Tektronix has updated its DAS 9200 digital-analysis system, a top-end logic analyzer. Among the enhancements are deeper memory (to 2 Mbits/channel), performance analysis with 5000 symbolic ranges, and improved networking, which lets users of Sun workstations open a DAS window and control a system miles away as if it were inches away.

The large number of software-development tools that are compatible with Sun workstations gives users of the networked analyzers a long list of options for code development and debugging. The company's LA-Connect software, which extracts information from many vendors' compilers, and the workstations' windowed user interface let developers use their high-level-language source code as a guide in setting complex hardware breakpoints and tracing program execution. System pricing begins at $29,950. Owners of older systems can add all new capabilities. Tektronix Inc, Beaverton, OR, (800) 426-2200.

System combines tools for pc boards and multichip modules

The System Workbench combines existing tools for design entry, PLD and field-programmable-gate-array (FPGA) design, simulation, physical design, and board- and system-level analysis. The tool set includes Cadence front-end tools such as Composer design entry software, the Verilog-XL simulator, and Allegro Correct-by-Design physical-design and analysis tools from Valid. The Communications Manager, a component of Cadence's Design Framework II, provides flexible communication among the various tools. It includes a default, technology-independent design flow. The user may also customize the design flow to manage tool encapsulation, tool sequencing, and methodology automation.

The software also includes a common-constraints editor for setting electrical, physical, and timing constraints across all tools at once. You can retarget the Valid tool's technology files to your specific manufacturing process or multichip-module fabrication technology. Optional libraries include standard parts from Cadence and hardware and software models from Logic Modeling Corp. You can use a single symbol to represent any of these three models and optional development tools to add new parts or to customize existing ones. Analysis options let you conduct pre- or post-layout reliability analysis, perform critical placement and routing, and execute informed design optimizations using on-line thermal- and signal-integrity analysis.

Available in October, a minimum tool set for design entry, packaging, and physical design starts at $58,000. The complete tool set starts at $145,000. Cadence Design Systems Inc, San Jose, CA, (408) 943-1234.

Real-time BIOS makes DOS real for 80186 μC

The 80186 is a microcontroller (μC) with peripherals and setups that differ from the standard PC 80x86-CPU μP. The Embedded BIOS from General Software provides a configurable DOS BIOS that runs on the μC. The BIOS is compatible with the IBM PC BIOS and includes video, keyboard, serial, parallel, disk, time/date, info, disk (remote, ROM, high memory ROM), and an integrated debugger. The company is supplying utilities for burning applications into ROM.

The Embedded BIOS comes with full source code, so you can modify it as you need. The BIOS image size runs between 32 and 64 kbytes. The BIOS supports 80186 chip select, 80186 timers, and the watchdog timer. The BIOS is the low-level part of I/O drivers and peripheral interfaces. Interrupt latency is held at 5 to 10 instructions. Embedded BIOS sells for $350; there are no royalties. General Software, Redmond, WA, (206) 391-4285, contact Steve Jones.

Operating system fits palmtops and portables

Digital Research/Novell's PalmDOS is a DOS-based operating system tailored for handheld equipment and palmtop PCs. The operating system is a stripped-down version of Digital Research's DR DOS, with built-in support for small equipment. The OS supports the PCMCIA (PC Memory Card International Association) 2.0 specification for small memory and peripheral pop-in cards. In addition, OS suits ROM-based systems and subsystems with OS-directed, hardware-based power management. To save power, you can power down parts of the system when not in use.

The operating system connects to Novell's Netware communications packages, which are an industry standard. This connectivity includes Netware client support and standard Netware communications device drivers. The OS also provides password protection to files and subdirectories. The system handles flash memory and battery-backed static-RAM storage. It also supplies utilities in ROM and is MS-DOS compatible. The system's minimum RAM requirement (assuming the OS is in ROM) is 128 kbytes. Minimum space requirement is 58 kbytes without a shell/user interface; with the full COMMAND.COM, the OS uses 95 kbytes. In OEM quantities, prices must be negotiated. The system comes as a Re-Distribution Kit (RDK). System and software developers can buy the Netware PalmDOS Software Developers kit (#884-0000030-001) for $2995. Novell/Digital Research, Monterey, CA, (408) 649-3896.

Alliance provides measurement and control systems

An alliance formed by Sun, Tektronix, and National Instruments will provide workstation-based measurement and control systems in a product line called Open Measurement Solutions (OMS). The heart of these systems will be Sun workstations, Tektronix instruments, and National Instruments' new SunOS version of its Labview virtual-instrument software. National Instruments will also supply certain hardware, such as IEEE-488 and VXIbus interfaces and VXI Slot-0 controllers.

Customers can act as their own system integrators: They will buy what they need from each company. Tektronix will offer standard systems; customers who do not want to do system integration will be able to order everything they need from Tek, which will purchase sys-

Text continued on pg 26

Controller board tackles PLLCs with C

Z-World's Little PLC (program logic controller) provides an alternative to traditional PLLCs (program ladder-logic controllers). Instead of using bulky PLLCs, engineers can drop a 4.33×2.85-in. board into the system that draws only 0.8W (0.4W in low power). The company provides a C compiler, Dynamic C, for programming the board for complex control applications.

The controller is a self-contained device. It has a built-in switching power supply, watchdog timer, a time/date clock, a power-fail detector, two RS-485 serial communications lines, eight optically isolated inputs, and eight relay-driver outputs. Built around a 9.26-MHz Zilog Z80181 µP, the board holds up to 512 kbytes of battery-backed static RAM and as much as 512 kbytes of EPROM ROM. In addition, the board holds 512 bytes of EEPROM for nonvolatile storage of key parameters or security IDs. The board has a 26-pin connector for expansion and peripherals. Expansion boards available include a board with eight DIP relays and an expansion board with six power relays (10A at 24 Vdc and 5A at 120 Vdc). The relays are software controllable.

The C programming system is tailored for embedded control. It supports PC-host code development with a communications link to the target board for downloading and debugging. The system comes with a multitasking kernel (with source code), a C compiler (to handle ROMable code), a library of drivers and application programs, and a C/Assembly-language source debugger. The C compiler generates in-line Assembly code. The board and software sell for $195 each. The relay expansion boards cost $95. Z-World Engineering, Davis, CA, (916) 757-3737, contact Carrie Evanoff.

Text continued from pg 24

tem components that it doesn't make. The alliance will also support value-added resellers who will supply custom systems tailored to specific applications. The companies have worked out a support plan so that, should problems arise, customers won't have to worry about finger pointing among the vendors. For more information, contact Tektronix, Beaverton, OR, (800) 426-2200, ext 111.

SPARC chip and board set integrates with PC/AT cards

SPARC-clone designers can easily integrate SPARC processors with low-cost PC/AT ISA cards and PC peripherals. Nimbus Technology has extended its Nimbus SPARC chip-and-board set to drive one or two PC/AT add-in cards. (See "SPARC board set uses MBus modules," EDN, June 18, 1992, pg 24.) AT expansion slots open up SPARC clone boxes for standard, low-cost PC peripherals. In addition to features shared with the previous product, the set also incorporates the SBus, a 64-bit mezzanine bus for specialized peripherals. The set costs $400 (2000). Nimbus Technology Inc, Santa Clara, CA, (408) 727-5445.

Companies field CAN chip

Intel, in a joint development with Robert Bosch GmbH, has developed a controller chip for the Controller Area Network (CAN) protocol. CAN is an embedded-system, multiprocessing LAN that is used by European car manufacturers. The 82527 chip implements CAN Protocol Specification 2.0, which provides a single bus to link embedded components.

CAN 2.0 defines both 11- and 29-bit message identifiers and can drive data at rates up to 1 Mbps. CAN has built-in error-checking and message security. The controller chip handles communications processing, including error detection, correction, and confinement. In a 44-pin plastic leaded chip carrier, the chip meets automotive temperature grade (−40 to +125°C). The chip will be available in October in sample qty, with production in March 1993. The production price is $5.30 (250,000). Intel Corp, Santa Clara, CA, (800) 548-4725.

Multiprocessor architecture gains speed and memory

Corollary has enhanced its multiprocessor PC architecture by improving its C-bus multiprocessor bus design and adding Intel's new 66-MHz 80486DX2 µP to the mix. The enhanced multiprocessor bus, formerly called the Enhanced C-bus, can now address 256 Mbytes of memory, which is four times greater than the original C-bus spec. The company's boards let you build multiprocessor PCs that can efficiently run the Unix OS. You get linear-performance improvements in multitasking performance when you add processor boards. The advantage of the PC architecture in this application is the large number of add-in cards available for the PC.

A $12,500 base configuration consists of a 13-slot backplane with both EISA and Extended C-bus connectors; the company's 486/smp XM EISA Bridge processor card with 1 Mbyte of cache RAM; the 486/smp XM I/O card with SCSI, floppy-disk-drive, serial, and parallel interface ports; and the smp Memory/256 memory board with 256 Mbytes of RAM. The RAM card uses error detection and correction. Performance tests indicate that these new cards perform 50% faster than the company's earlier products. Corollary Inc, Irvine, CA, (714) 250-4040, FAX (714) 250-4043.

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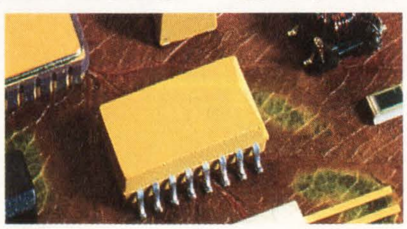

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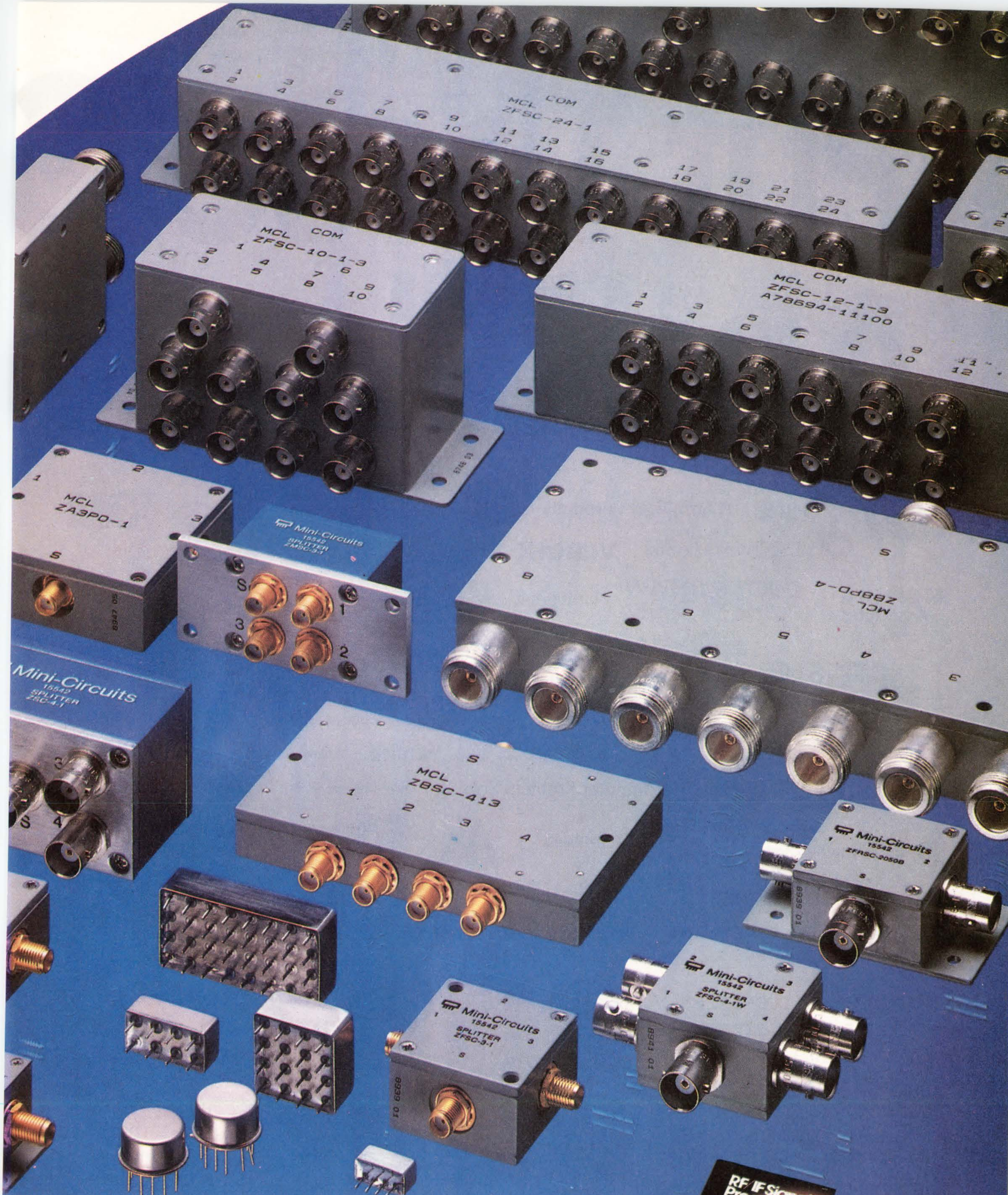

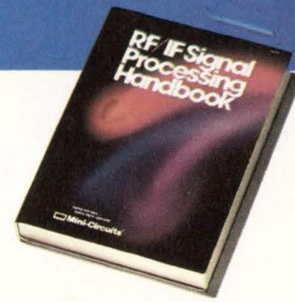

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For more information on the 29K Family of embedded RISC processors and Fusion29K support, call AMD today: **1-800-292-9263 Ext. 3.**

With this much support, you may be able to take some time off for yourself.

CIRCLE NO. 24

Advanced Micro Devices

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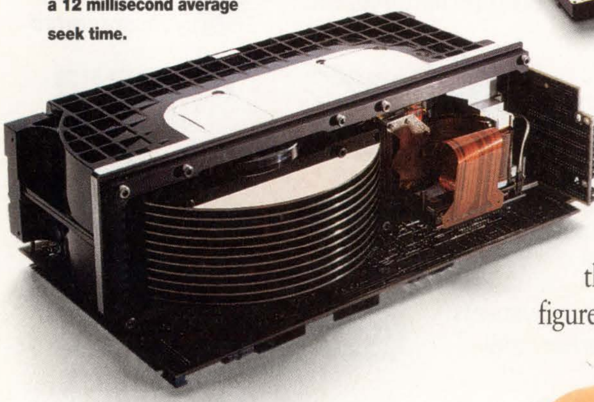
The first name in disc drives is now the first name in performance, too.

For years, Seagate has set disc drive industry standards for availability, reliability and product range. But you may

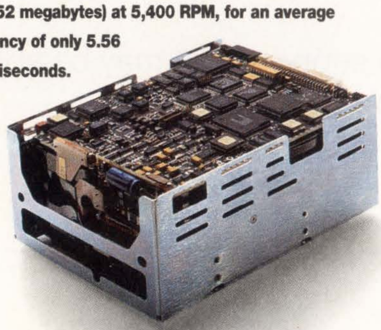
This 2 head parallel Sabre-7 (ST83050K) gives you 3 gigabytes of storage in an 8" form factor, with a transfer rate of 9.34 megabytes per second and a 12 millisecond average seek time.



be surprised to learn that we're consistently leading the industry in performance as well.

The drives featured here are available now—setting performance standards in systems like yours all over the world.

The 5.25" Elite 1 offers gigabyte-plus capacity (1352 megabytes) at 5,400 RPM, for an average latency of only 5.56 milliseconds.



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At 2.5", the ST9235 offers 209 formatted megabytes with the AT interface and an average seek time of only 16 milliseconds.

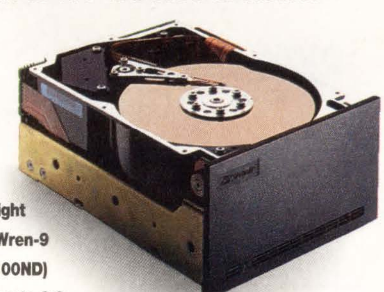
drives like these. Because when you take a few milliseconds' performance advantage and multiply it by thousands of transactions a day… well, the results translate into some figures that might surprise you.

The ST3283 family of 1" high 3.5" drives holds more than 245 formatted megabytes, with a 4,500 RPM spindle which reduces latency to 6.67 milliseconds.

In fact, depending on the amount and nature of processing you do, high-performance drives like these can save you enough to pay back your disc drive investment within weeks — or days. For help in selecting the

The digital servo on this ST3600 family of low-profile 3.5" drives reduces average seek time to 10.5 milliseconds, with capacities up to 525 formatted megabytes.

drive you need, or for more information about any Seagate drive, call Seagate at 408-438-6550 or contact



This full-height 5.25" Wren-9 (ST42100ND) offers up to 2.2 gigabytes of storage and a synchronous data transfer rate of up to 20 megabytes per second.

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The 3.5", half-height ST11200 family, with up to 1.2 gigabytes of storage, boasts a 256 kilobyte multi-segmented cache buffer and an average seek time of 10.5 milliseconds.

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Reader finds schools that "measure up"

I enjoyed Jon Titus's editorial "Don't blame the kids" (EDN, April 23, 1992, pg 41). I have long had similar views and would love to see teachers held accountable. Even so, the responsibility for a child's education is squarely on the shoulders of the parents and the community. When parents are involved, and the school system accepts and encourages their participation, and the community stands behind the importance of education, then you have all the ingredients for world-class instruction.

I don't have much faith in testing as a means of correcting a problem. All you end up with is teachers who are good test-takers, and you still have not solved the problem.

Our solution to the problem was to move to a place where a child's education is of utmost importance. The school system here in Corvallis is impressive. With Oregon State University and Hewlett-Packard as the major employers in town, it's easy to see why education is so important.

Our oldest son will be starting school in September. Recently, my wife and I went to his orientation. I talked with other parents who already have kids in the school and was impressed by how much they have been able to contribute to their child's education. The teachers seem to be genuinely interested in including the parents in the education process.

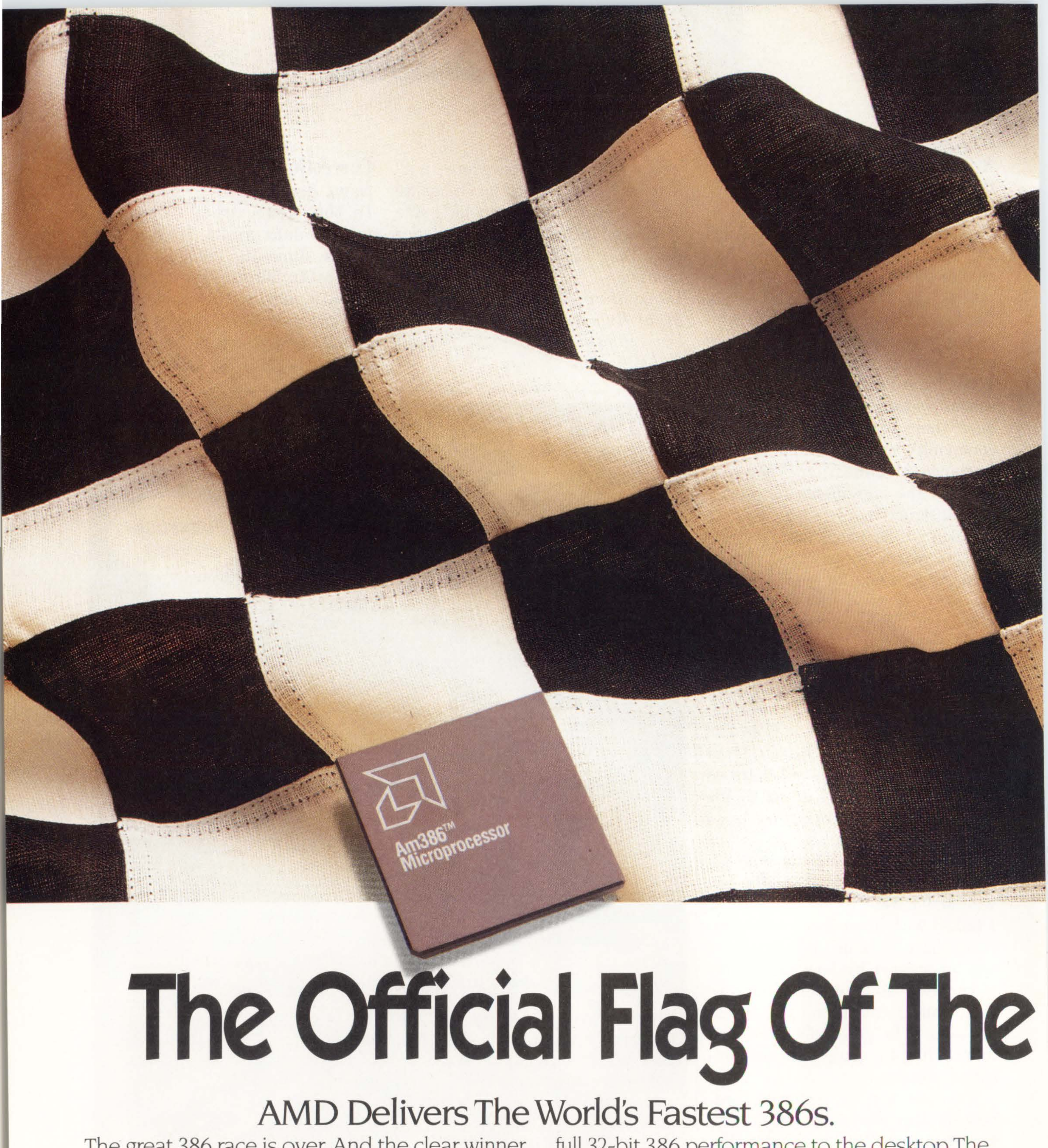
Our solution to America's education slip obviously can't work for everyone. We are, essentially, just looking out for our own. The difficulty of trying to change other parents and an entire community were beyond our ability. By moving to Corvallis, we have found a place where there are many parents with attitudes similar to ours.

We are not concerned about which side of the "have/have not" fence our children end up. What we are concerned about is which side of the educated/uneducated fence they fall. With education comes freedom.

David Shear
Shear Engineering and Development
Corvallis, OR

Correction for Simulex News Break

In the News Break "Controller pumps data at 24 Mbytes/sec," (EDN, June 18, 1992, pg 21), the disk controllers are the SX1615 and SX1610, not SC1615 and SC1610; the price is $172 (1000), not $72 (1000); and the company's phone number is (714) 730-1500.



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AMD Delivers The World's Fastest 386s.

The great 386 race is over. And the clear winner is the Am386 microprocessor family.

The fact is, no other 386 microprocessors available today can rival the sheer speed and performance of the Am386 microprocessors. The Am386DXL-40 CPU brings 40MHz, full 32-bit 386 performance to the desktop. The Am386SXL-33 CPU makes 33MHz the standard for 386SX machines both at the desktop and for battery powered applications.

The 40MHz DXL-40 and the 33MHz SXL-33 are available in low-cost PQFP packaging.

In either case, they're over 20% faster than those run-of-the-mill 386s.

EDITED BY JULIE ANNE SCHOFIELD

Be on the lookout for self-powered, adjustable resettable fuse

I am looking for a simple circuit that is in effect an adjustable, resettable electronic fuse. I have seen such circuits before, but they have all required an external power source. In my circuit, I want to have the fuse self-powered—that is, line-powered—by the very piece of equipment being tested.

Basically, I am searching for a device to temporarily replace a given fuse in a piece of equipment undergoing testing. The device's break current must be adjustable; the range I'm looking for is something on the order of 200 mA to 6A. I also want this device to test both ac and dc. It would be nice if special home-brew wound transformers or coils could be avoided. Also, I'd prefer solid-state relays to mechanical ones.

I realize that mechanical circuit breakers would suffice, but a wide variety of trip currents would be needed and the response time of circuit breakers is generally a lot longer than that of fast-blow fuses.
Michael Danish
Aberdeen Proving Ground, MD

We were unable to locate an adjustable electronic fuse. If anyone has come across such a device, we urge them to contact Ask EDN.

We did run across Inresco (Manasquan, NJ, (201) 223-6330), a company that makes small board-mountable devices called circuit savers. The devices function like current limiters. They are very fast and reset themselves. However, they are not variable—you must specify specific trip points.

One IC won't do

I want to use one serial port on a notebook-style computer to address, send, and receive data with two RS-232C ports on a piece of test equipment. I want to be able to address an individual port on the test equipment, read data from that port, address the other port, read data from that port, and so on as necessary. Can you suggest any ICs that would fit the bill?
Gordon Sargent
General Electric Mobile Communications Inc
Lynchburg, VA

Executive Editor Steve Leibson replies: I know of no single-IC solution to this problem, and believe me, I've been watching. Essentially, what you need are three UARTs, a μP, and some memory. I know of no IC vendor currently offering all of these functions on one chip. Thus, to build this circuit, you'll need to design a board with the above parts plus assorted buffer chips, resistors, capacitors, and an oscillator. You must also write the software to make it all work, and you'll need to invent the command protocol for telling the circuit when to switch.

If you don't want to design, build, and debug the circuit yourself, you can get the product ready made. It's called the Logical Connection from Logical Connection Inc. This box has four serial ports, two parallel input ports, and two parallel output ports. You can connect any port to any other port with a command sequence. The box costs $449 with a 256-kbyte buffer memory. You can configure the box with as much as 1 Mbyte of buffer memory.

Logical Connection Inc
4660 Portland Rd NE, #108
Salem, OR 97305
(800) 238-9415

Reader needs book to start evaluating μCs

In the January 20, 1992, issue of EDN, the Special Report on 8-bit-μC evaluation boards has a box titled "Getting started easily." This box refers to a book called *The 8051 Microcontroller* by Kenneth J Ayala and published by West Publishing in Minneapolis, MN.

I have been trying to contact West Publishing, but all I get is a message that the phone has been disconnected. Possibly the company has moved or gone out of business. From Australia, I am having trouble finding what has happened to this company. Would it be possible for you to ask the author of the article whether that book is available from another source?
Peter Baxter
Cochlear Pty Ltd
Lane Cove, NSW, Australia

The publisher has relocated. The new address is

West Publishing Co
Box 64526
St Paul, MN 55164
(800) 328-9352
(612) 687-7000.

The book sells for $49 plus $2 shipping and handling and your local sales tax.

Readers respond to part request

We'd like to thank the following readers who responded to Ariel Spivakovsky's request for SN76477s and SN76488s in the May 7, 1992 issue: Richard N Sterns (Pensacola, FL), William M Wren (Rapidprint Inc, Middletown, CT), Vineet Dujari (Fremont, CA), Mac Cody (Sunair Electronics, Fort Lauderdale, FL), and Leonard Jacobs (Dynamic Signal Systems, Eden Prairie, MN).

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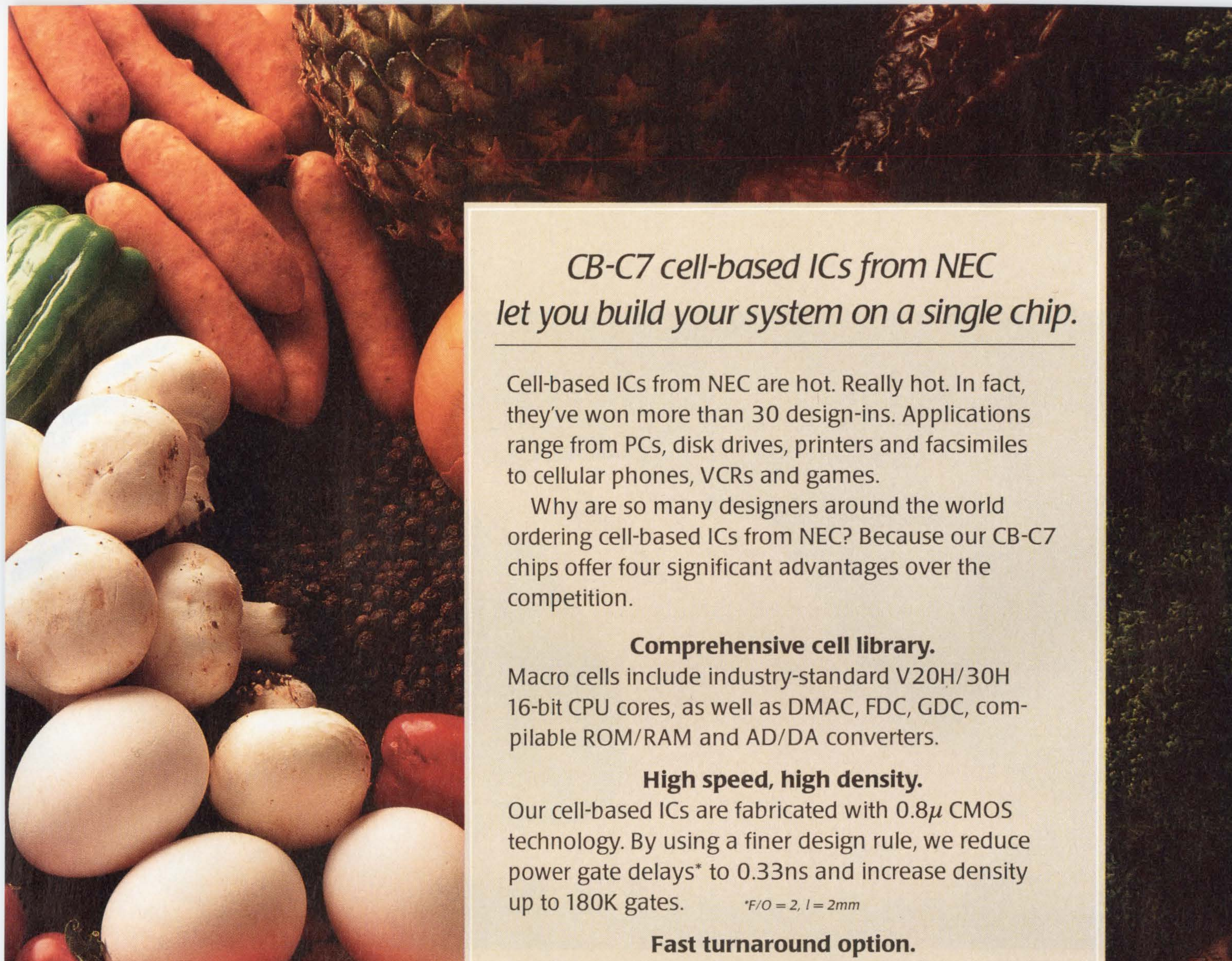
WHO'S GOT THE POWER TO KEEP NEW GENERATION DISC DRIVES RIGHT ON TRACK?


CB-C7 cell-based ICs from NEC let you build your system on a single chip.
Cell-based ICs from NEC are hot. Really hot. In fact, they've won more than 30 design-ins. Applications range from PCs, disk drives, printers and facsimiles to cellular phones, VCRs and games.
Why are so many designers around the world ordering cell-based ICs from NEC? Because our CB-C7 chips offer four significant advantages over the competition.
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Macro cells include industry-standard V20H/30H 16-bit CPU cores, as well as DMAC, FDC, GDC, compilable ROM/RAM and AD/DA converters.
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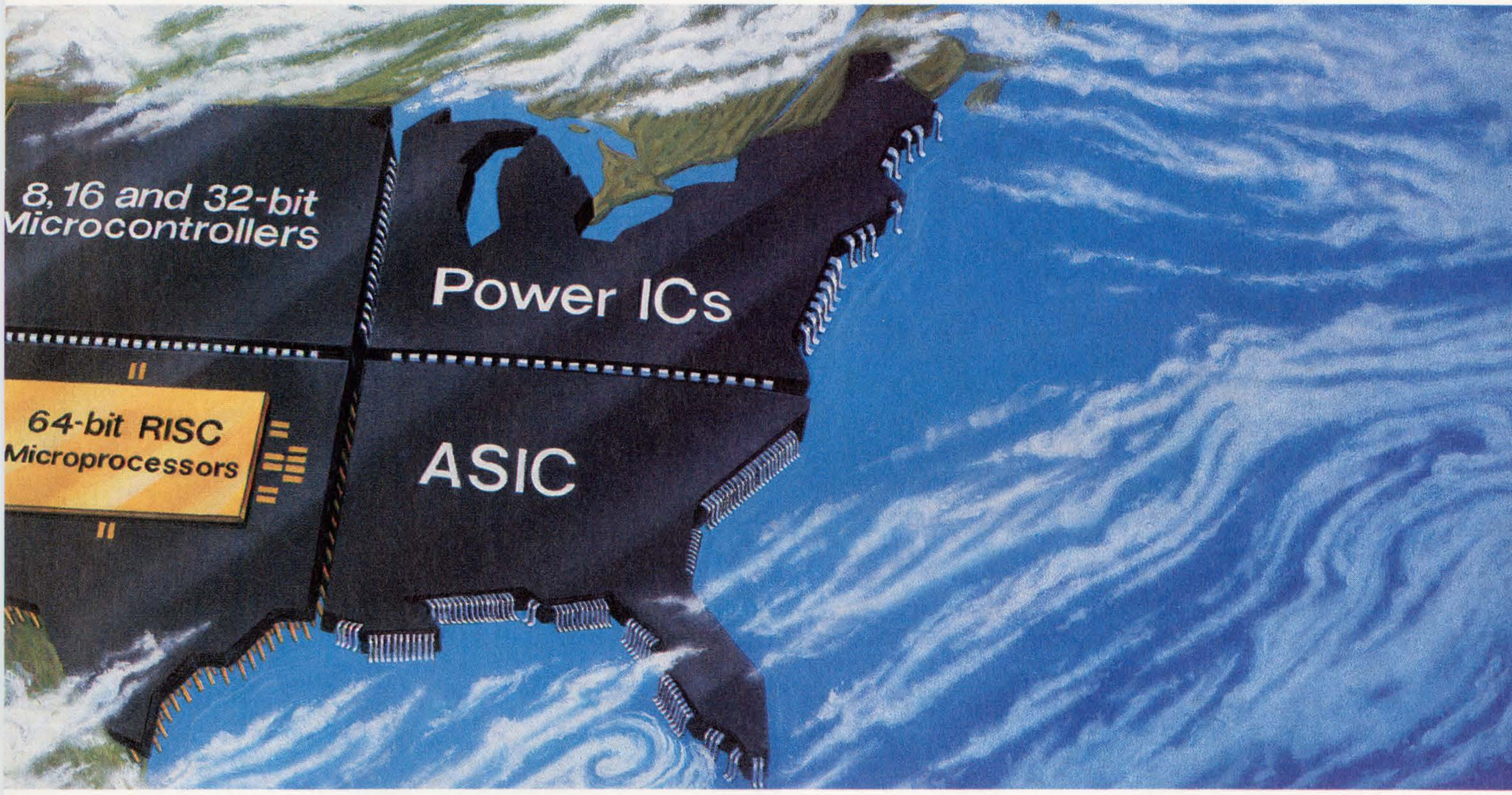
Designers appreciate the convenience of working with CB-C7 ICs. NEC's OpenCAD Design System™ lets you use industry-standard design tools on popular workstations.
People have been talking about a system on silicon for years. If you want to see the reality, call NEC. We've got a hot product and we deliver it fast.


8, 16 and 32-bit
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Power ICs
64-bit RISC
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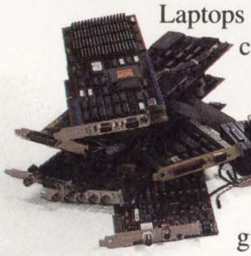
Try stuffing these into a laptop.



Laptops have their place, but for mission-critical applications requiring serious expansion, workstation power, CRT-quality screens or toolbox ruggedness, get a P.A.C.™ (Portable Add-In Computer). **■ MASSIVE EXPANSION.** Nobody gives you more expansion possibilities then Dolch. In an 18 pound package a Dolch P.A.C. has room for up to five full-size EISA/ISA add-in cards. You can add up to 32 MB RAM, 1 GB HDD, and any combination of drives, CD-ROM, removable HD, streaming tape, and more. **■ EXTREME POWER.** Dolch P.A.C. systems have been rated "the fastest portables on the market" since 1987, and have won more Editor's Choice awards then any other product in its category. *Computer Reseller News* calls the 486-50E "a dream machine . . . one of the most powerful PCs of any kind." P.A.C. systems are based on 386SX and DX, and 486 CPUs up to 50MHz, delivering as much as 22 MIPs. **■ DAZZLING DISPLAYS.** "Breathtaking . . . Dolch's heart-stopping TFT Color Display produces vibrant colors and sharp images virtually on par with those seen on desktop VGA monitors," reports *PC Computing*. **■ MIL RUGGEDNESS.** Every P.A.C. is as tough as it is powerful. Certified under MIL Std. 810C Dolch provides true mission critical reliability. ". . . it simply outclasses its competitors and it is sturdy and solid . . ." says *PC Magazine*. **■ GET THE FULL STORY.** Call **1.800.538.7506**. In Canada 1.800.561.4527.

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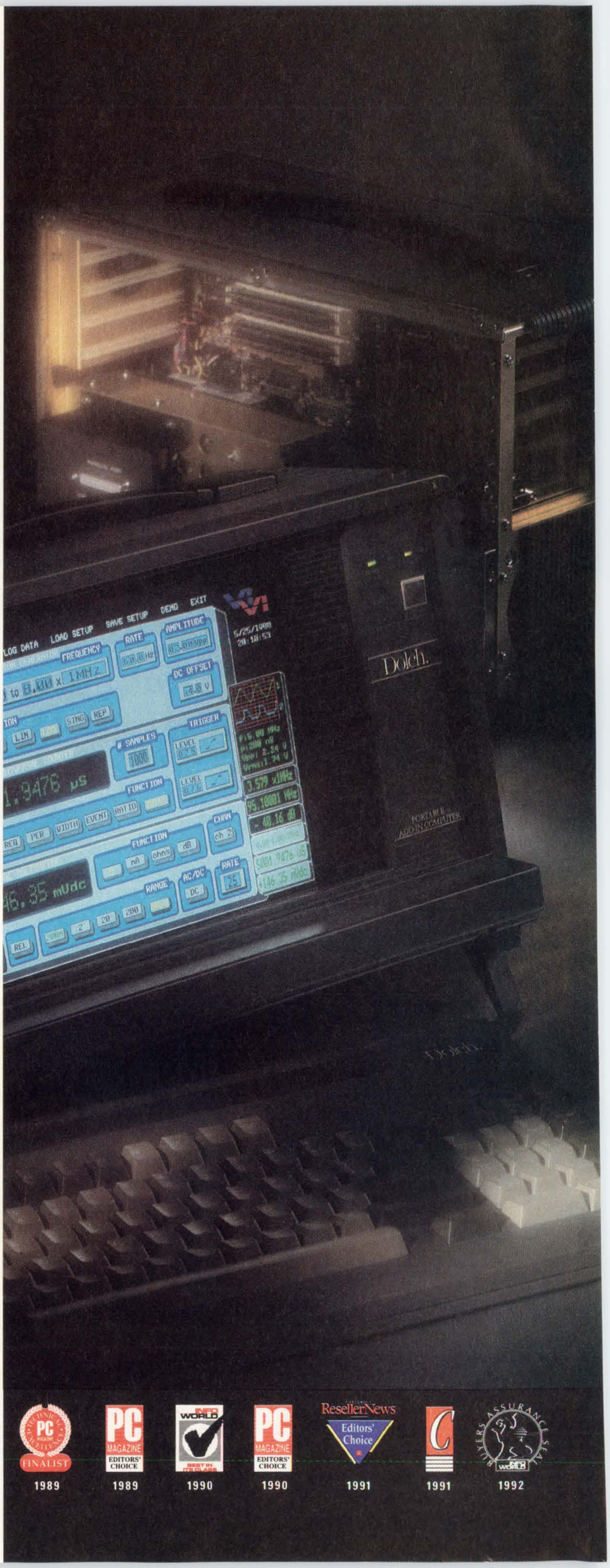
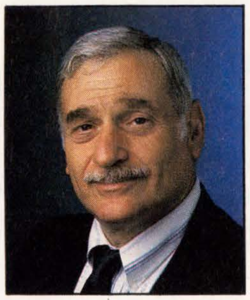


Break some rules



The debate about ends and means is endless. Do good ends justify bad means? To achieve a noble end should we do ignoble things? World War II is a classic case: with civilization at stake, could we afford to act the gentleman or lady?

In engineering, we aim for both profitable ends and efficient means. Engineers and engineering managers pride themselves on pragmatism—finding effective means to solve problems, delivering desirable ends. This approach sounds good. So why do we have so many organizational and people problems? Why do we float products out the door on a sea of ineffectual paper? Why can't we get the sand out of our organizational gears? And how come we spend much of our time struggling with our own internal systems?

I suspect it's due to a number of things that contribute to corporate rigidity. One culprit is a gradual buildup of corporate rules. Originally deployed to ensure corporate consistency, rules often get out of hand, eventually clogging the corporate arteries.

I'm not saying that rules are bad. Actually rules are good things. Our brains evolved to detect a pattern and react, that's what we humans do best. It's a bit like learning to drive or make coffee; we're slow at first, but when we learn the behavior pattern, it becomes almost automatic.

Rules are just organizational patterns with attached actions that provide quick solutions for given situations. However, rules can outlive the problems that required them, and go on to develop a life of their own. With enough such rules unchained from ends, you get a system without corrective feedback—a world in which means define ends. In short, the rules define results.

How come? Well, as a rule is accepted, it just becomes part of the operational culture, or the way things are done. At that point, rational discussion flees, usually replaced by rote, unyielding justifications. Thus the rules we created to solve problems can metastasize, and pollute the body corporate.

Here's a modest proposal for swiftly regaining sanity. I call it the "Reasonable Person Test." It's simple. Take each suspect rule and ask, "What would an average customer or user think of this rule?" Would users think it's silly or useless? If so, check the rule. It may be one that consumes resources, without aiding profits or performance. If so, junk it.

Means and ends *are* connected. To be effective, ends must dictate means. So if you're frustrated in trying to get things done and find much of your day spent in satisfying pointless rules, then do some rule weed-whacking. Not only will it make your day, but it will raise your firm's competitiveness. Good luck.

Ray Weiss

Ray Weiss
Technical Editor

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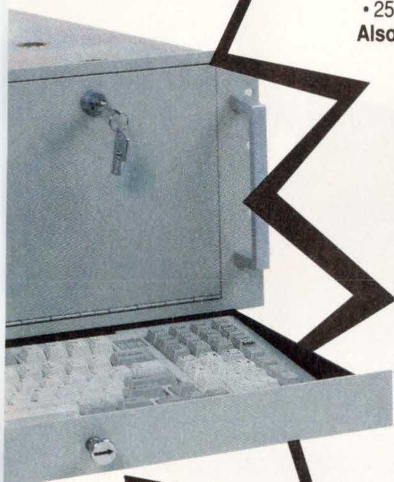

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CVC560 ***Versatile Low-Cost 16-Bit VGA***
- 256Kb to 512Kb video memory

CVC550 ***High Performance 16-Bit VRAM/VGA***
- 512Kb to 1Mb video memory

CVC530 ***16-Bit Flat Panel/VGA Support***
- 256Kb video memory

Also: Paradise 16-Bit
ATI VGA Wonder
CGA Compatible Video Card
Monochrome Compatible Video Card

Multi-Function Utility Cards

CIO703 - Dual Serial Ports
CIO704 - IDE, Floppy, 2 Serial/1 Parallel
CEX541 - IDE, Floppy, 2 Serial/ 1Parallel, CGA
CEX543 - IDE, Floppy, 2 Serial/ 1Parallel, SCSI, CGA
CEX561 - IDE, Floppy, 2 Serial/ 1Parallel, SCSI
CEX571 - IDE, Floppy, 2 Serial/ 1Parallel, SCSI, VGA
CEX591 - IDE, Floppy, 2 Serial/ 1Parallel, SCSI, Flat Panel VGA
CEX575 - IDE, Floppy, 2 Serial/ 1Parallel, Super VGA

Disk Controller Cards

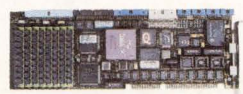
Adaptec 1542A - ISA Bus SCSI Controller
Adaptec 1542B - ISA Bus SCSI Controller w/ Floppy Port
WD7000FASST - ISA Bus SCSI Controller w/Floppy Port
CEX Series - IDE and SCSI Controllers (see above)
Bustek BT742A - EISA Bus SCSI Controller
DPT Smart Cache Plus - EISA Bus SCSI Controller w/Cache
Adaptec 1740 - EISA Bus SCSI Controller

Network Adapter Cards

Mylex LNE390A - EISA EtherNet Adapter
Mylex LN390 - ISA EtherNet Adapter
Proteon ProNET 4/16 - ISA or EISA Token Ring N/C

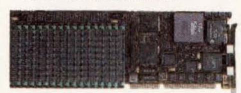
ISA or EISA CPU CARDS

CAT1011/CAT1010



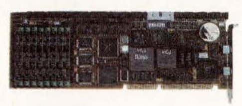
20-66MHz 80486SX/DX/DX2
- 8Kb 80486 internal cache
- Up to 32Mb onboard DRAM
- Up to 512Kb user PROM disk
- Embedded Peripherals

CAT1001/CAT1000



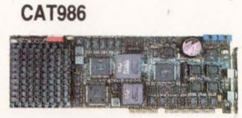
20-66MHz 80486SX/DX/DX2
- 8Kb internal cache
- Up to 32Mb onboard DRAM
- CAT1001-Serial/Parallel

CAT990



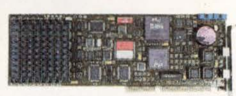
25 or 33MHz 80386DX/486DLC
- Up to 32Mb onboard DRAM
- Up to 128Kb cache
- Embedded Peripherals

CAT986



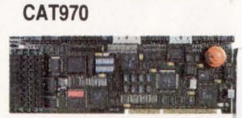
33 or 40MHz 80386DX/486DLC
- Up to 32Mb onboard DRAM
- 128Kb cache onboard
- Up to 1Mb user PROM/FLASH

CAT985



25 or 33MHz 80386DX/486DLC
- Up to 32Mb onboard DRAM
- Up to 512Kb user PROM/FLASH

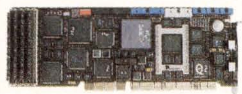
CAT970



16-33MHz 80386SX/486SLC
- Up to 16Mb onboard DRAM
- VGA interface (flat panel)
- Embedded Peripherals

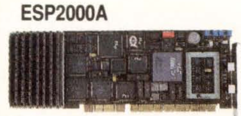
486 EISA

ESP2001



EISA 33-66MHz 80486 DX/DX2
- 8Kb 80486 internal cache
- Supports opt. INTEL turbo-cache
- Up to 32Mb onboard DRAM
- 128 bit DRAM Subsystem
- Embedded Peripherals

ESP2000A



EISA 33-66MHz 80486 DX/DX2
- 8Kb 80486 internal cache
- Supports opt. INTEL turbo-cache
- Up to 64Mb onboard DRAM
- 128 bit DRAM Subsystem

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CIRCLE NO. 36

Cached DRAM. It Screams!

Matching low-cost DRAM technology with today's high-speed CPUs can be a design engineer's nightmare. Until now. **Introducing the 100MHz 4Mb Cached DRAM from Mitsubishi.**

FIRST SYNCHRONOUS DRAM

Mitsubishi combined a fast, 4K x 4 SRAM and a 1M x 4 DRAM with a wide, 16 x 4 bit internal bus and a synchronous clock design, all into one tiny TSOP IC. The result is the industry's first synchronous DRAM with on-board cache.

100MHz OPERATION

The Cached DRAM's large, 16 x 4 bit internal data path can transfer a 16-line data block in just one cycle, allowing the small on-chip cache to perform like a much larger external cache. The result is fast, 100MHz performance at a much lower cost than separate cache configurations. Plus, the Cached DRAM's fast copy-back scheme significantly reduces the miss cycle penalty time.

COST-EFFICIENT, SMALL SIZE

The Cached DRAM die and package are only 7% larger than those of a standard 1M x 4 DRAM. And, since they are manufactured with the same process and on the same production line as Mitsubishi's standard 4Mb DRAMs, Cached DRAMs are highly cost-efficient to manufacture.

LOW POWER OPERATION

With a clock that can be stopped to reduce power consumption to as low as 1mW, the Cached DRAM is ideal for portable and highly integrated applications where low power consumption, compact size and fast operation are essential.

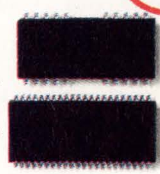
MITSUBISHI'S CACHED DRAM PERFORMANCE

Part Number	Cache Hit Access/Cycle	Cache Miss Access/Cycle	Direct Array Access/Cycle	Package
M5M44409TP-10	10ns/10ns	70ns/280ns*	70ns/140ns	TSOP**
M5M44409TP-15	15ns/15ns	75ns/300ns*	75ns/150ns	TSOP**
M5M44409TP-20	20ns/20ns	80ns/320ns*	80ns/160ns	TSOP**

*Cache hit cycles can resume after one miss access time, while the copy-back completes in the background.

**TSOP Type II. Also available in reverse pin-out TSOP.

Samples Available June 1992



Standard 4Mb DRAM.

Actual size.

4Mb Cached DRAM is only 7% larger than a standard 4Mb DRAM.

Not your ordinary next-generation DRAM, Mitsubishi's 4Mb synchronous Cached DRAM sets a totally new standard for cost-effective, high performance memory. For more information and technical specifications, please call **(408) 730-5900, ext. 2106 or 2226.**

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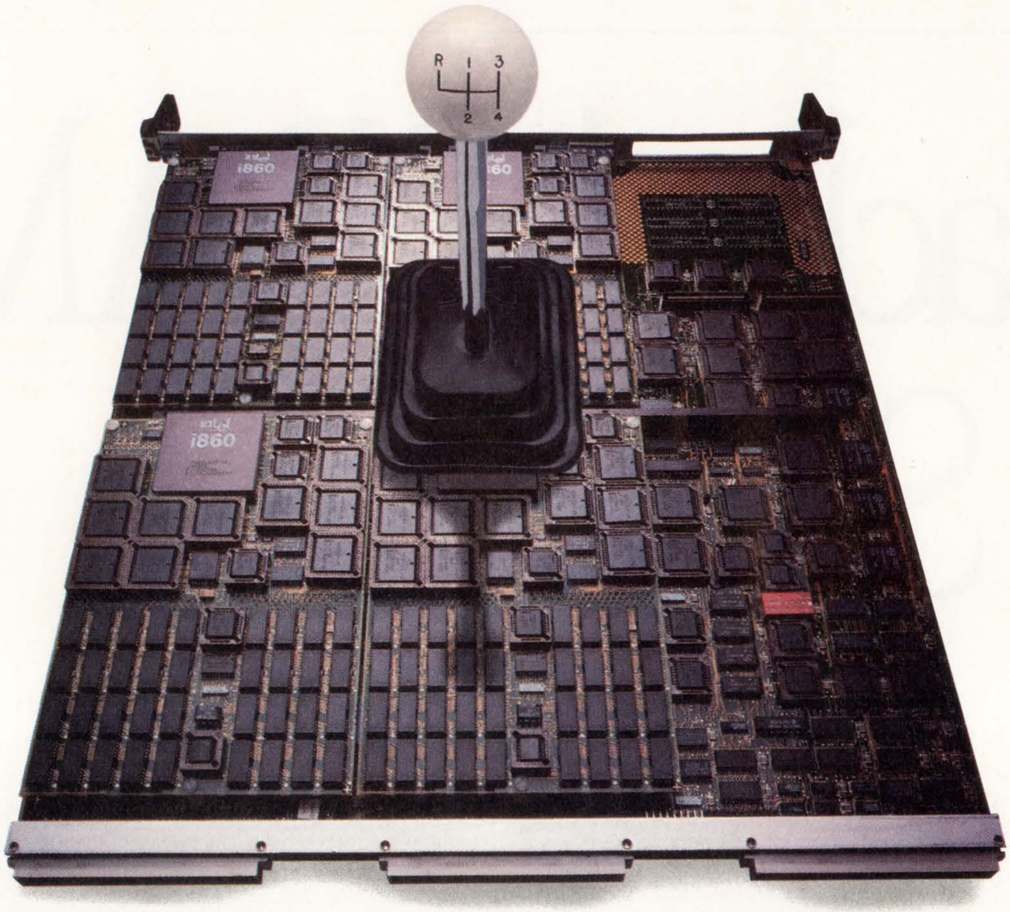
CIRCLE NO. 37



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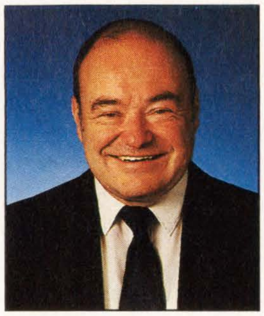
CIRCLE NO. 38

Futurebus+ standards spur commercial products

JOHN GALLANT, Technical Editor



Futurebus+ fans should be happy to learn that real-live products are beginning to proliferate. Finalized documents are providing the impetus to move this sauntering architecture off the drawing board.

According to Yogi Berra, "The future ain't what it used to be." Perhaps the great soothsayer would say the same for Futurebus+ if he counted the number of available products for this long-unsettled bus architecture. In response to firm Futurebus+ standards, over 20 manufacturers displayed chips, boards, backplanes, connectors, enclosures, and systems at Buscon '92 West in Long Beach, CA, in February. Buscon '92 East, in Boston, MA, from September 15 to 17, promises to feature more of the same.

Much of the momentum change, since our last look at Futurebus+ (**Ref 1**), is due to the fallout from the US Navy's Next Generation Computer Resources (NGCR) program. In 1989, the Navy's Space and Naval Warfare Systems Command (SPAWAR) decided to extend proof-of-concept contracts worth $2 million apiece to three primary contractors: Cable and Computer Technology (CCT); Litton Data Systems (Pascagoula, MS); and Raytheon.

The intent of the NGCR program is to develop interoperability standards for a single, universal computer standard to which all future Navy computer systems must adhere. The Navy focused on the Futurebus+ scalable open-system architecture to conform with future industry standards. By conforming to industry standards, the DoD can upgrade systems quickly at minimal cost.

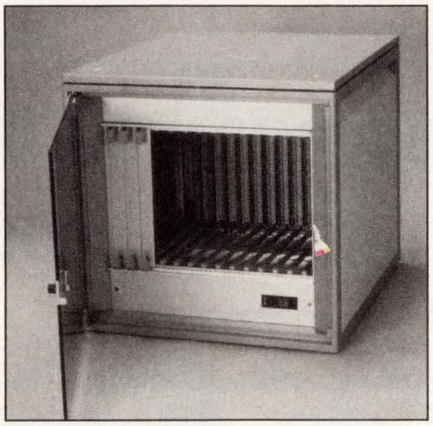
Because the pundits hail Futurebus+ as processor independent, the Navy commissioned the three contractors and their subcontractors to build systems having different CPUs. Currently, the Navy is evaluating conformance and interoperability tests on systems delivered by the prime contractors. CCT delivered systems based on the AMD 29000 and Motorola 68030 µPs; Litton Data Systems delivered systems based on the Intel 80486 and Motorola 88000 µPs; and Raytheon's Equipment Division delivered systems based on the MIL-VAX and Mips R3000 µPs.

The final NGCR standards probably

The fallout from the NGCR program is beginning to have commercial repercussions. CCT, one of the prime contractors, offers a variety of CPU, memory, I/O, and communication boards as well as complete Futurebus+ systems.

won't be completely defined for another four years. But the IEEE Futurebus+ committee has already benefited from the Navy's program and has finalized some of the Futurebus+ standards. As usual in computer-system development, hardware standards are progressing faster than software standards. An operating-system specification still remains entirely up in the air, and don't expect a working specification before 1995.

The IEEE approved and adopted five critical hardware documents in September 1991. The documents are IEEE 896.1—Futurebus+ Logical Layer; IEEE 896.2—Futurebus+ Physical Layer & Profiles A, B, & F; IEEE 1194 & 1194.1—Backplane Transceiver Logic (BTL); IEEE 1301—Guide to Metric Mechanicals; and IEEE 1301.1—Metric Mechanicals for 2-mm Connectors. The final approval of these documents has solidified what hitherto were wavering specifications and allowed vendors to commit to concrete designs.



The height of a 12SU Futurebus+ subrack (300 mm) is slightly larger than a standard VMEbus 6U subrack (266 mm). Therefore, 12SU enclosures, such as the Minirack cabinet from Schroff, can house a 6U subrack to accommodate a bridge to the VMEbus.

The suite of documents that completely defines the Futurebus+ standard is staggering (**Fig 1**). Such a collection is a departure from the single document that defines the bus standard for VMEbus or Multibus. The IEEE design goal is to create a pool of specifications, called Profiles, that allow vendors to produce products for different bus architectures. A Profile is a compilation of IEEE standards that defines a range of products that will interoperate. Each Profile targets different applications.

Display your best Profile

Having a finalized IEEE 896.2 specification, vendors can now offer a range of products that conform to Profiles A, B, or F. Profile A is a general bus architecture that specifies a 64-bit and a subset 32-bit address and data-path backplane for compelled- and packet-mode transactions. A 128-bit superset path and 192 or 80 I/O pins on the backplane are optional. Multiple cache memories on the backplane maintain cache coherency using the Modified Exclusive Shared Invalid (MESI) model (**Ref 2**).

Profile B is an I/O architecture that attaches to a host system via a host-to-Futurebus+ bridge. The major difference between Profiles B

Competition is the spice of life

Although Futurebus+ offers many alluring attractions to electrical practitioners, mature buses aren't giving up without a struggle. Some of these oldsters are getting a midlife booster to help them compete with the young upstart. Consider the VMEbus, for example. Gerry Gipper, director of marketing at Motorola, cites several reasons why the VMEbus will maintain its vitality for a number of years to come.

High on-board integration is one reason. According to Gerry, it wasn't very long ago when marketing would make a list of wished-for functions to be included on a single-board computer, which engineering would summarily discard due to lack of board real estate. Today when marketing makes a similar wish list, engineering generally answers "Is that all? What are we going to do with the rest of the board space?" Because many functions are integrated onto a single module, the VMEbus simply becomes an I/O bus to support burst mode or message passing between modules.

Another reason is added bus performance. To enhance the speed of burst-mode transfers on the VMEbus, the IEEE committee opened up the IEEE 1014 specification to consider adding three high-speed data-transfer modes. The Multiple Block Transfer mode, formerly called VME 64, promises to increase the DMA transfer capability from 40 Mbytes/sec to 80 Mbytes/sec. The Source Synchronous Block Transfer mode makes the VMEbus a synchronous bus and promises 160 Mbyte/sec DMA transfers. The Autobahn transfer mode will extend the burst-mode transfer rate to 400 Mbytes/sec.

Motorola also feels that the multifarious Futurebus+ form factors and profiles offer too many confusing options. Therefore, the company believes that market demand for Futurebus+ will be weak as long as the VMEbus can fill the bill. Motorola also is cognizant of the capabilities of Futurebus+, however, and is maintaining a wait-and-see position. Notwithstanding their added push, the VMEbus boosters fall far short of the 3.2-Gbyte/sec theoretical maximum transfer rate offered by Futurebus+.

and A is Profile B's inability to implement cache-coherent transactions. Profile F is a high-performance workstation architecture that specifies a 128-bit address and datapath backplane. For real-time operations, Profile F places specific time-response restrictions on cached and noncached transactions.

Other Profiles actively under development include Profiles M and T. The US Navy is developing the 896.5 document to define Profile M for a variety of military applications. Profile M must have live insertion, which is optional for Profiles A, B, and F. Another difference is Profile M's connector size. The other Profiles employ a 2×2-mm grid connector specified in the finalized IEEE 1301.1 standard and based on Du Pont's Metral connector.

The Navy doesn't believe that the 2-mm connector is dense enough for its applications, or that it will meet environmental requirements. In-

Text continued on pg 56

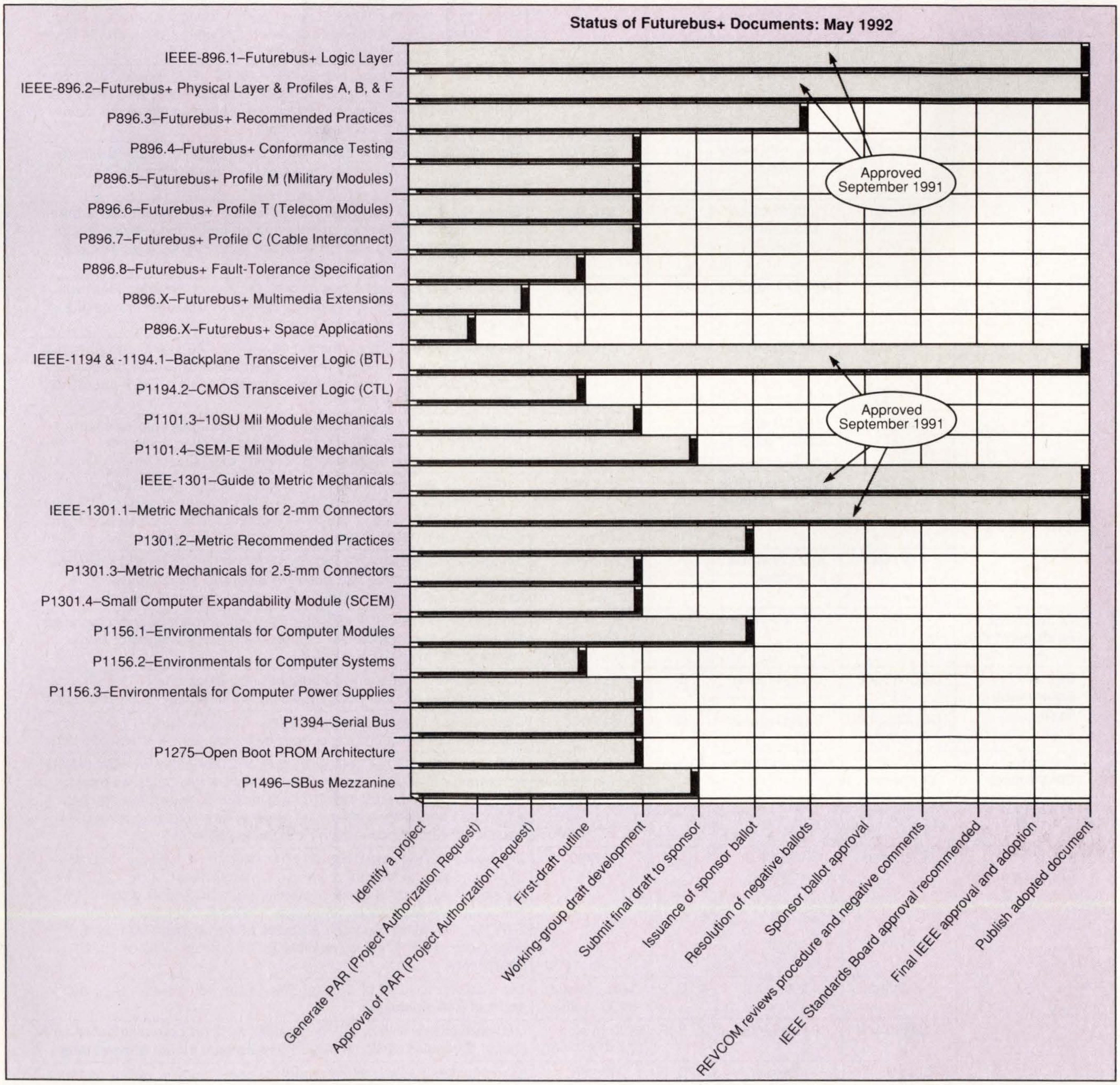


Fig 1—The bewildering set of Futurebus+ documents permits the definition of a variety of subsets called profiles. The chart shows the status of the IEEE documents effective May 1992.

Table 1—Current Futurebus+ products

Company	Model	Product type	Profile	Price	Description
BICC—VERO Electronics	KM25	Microrack	F	$8000 to $13,000	Multilayer backplane has 13 slots that conform to IEEE 1301.1 specifications. Power-conversion module delivers a maximum of 1800W. Thermal-management system has intelligent fan control. "System on" and "system off" switches control power sequencing.
	819-306xxxx	Backplanes	A, B, F	$1700 to $2500	16-layer design accepts 12 SU boards conforming to IEEE 1301.1 standards. A maximum of 13 slots are on 6SP (30-mm) pitch. SMT resistor and capacitor networks match signal trace lengths. Employs the company's LOMET low-impedance power connectors. Profile F backplanes can be used in Profile A but not vice versa.
Cable and Computer Technology Inc	FBC-030	68030 CPU module	A	$11,000	Single-slot, 12 SU board has 33-MHz 68030 μP; optional 6881 FPU; 2 Mbytes of dynamic RAM; 2 serial ports; debugger; monitor ROM; and optional OS-9 software. Supports distributed arbitration. 64-kbyte local cache provides cache-coherency logic.
	FBC-029	29000 CPU module	A	$13,000	Single-slot, 12 SU board has 25-MHz 29000 μP; optional 29027 coprocessor; 2 Mbytes of dynamic RAM; 2 serial ports; and debugger and monitor ROM. Supports distributed arbitration. 64-kbyte local cache provides cache-coherency logic.
	FBC-860	Array processor module	B	$16,000	Two-slot, 12 SU module has 40-MHz i860 μP; 2, 4, 8, or 16 Mbytes of dynamic RAM; 1k×64-bit burst-transfer data buffers; i860 subroutine library.
	FBT-001	Central arbiter and analyzer module	A	$12,000	Single-slot, 12 SU board has central arbiter with default bus arbitration. Supports 14 levels of priority and preempt and priority receipt. Four connectors plug into HP1650 and 16500-series logic-analyzer pods.
	FBM-001	Memory module	A	$8000	Single-slot, 12 SU board has 4 or 16 Mbytes of dynamic RAM with single-bit correction and double-bit detection. Provides cache-line buffers and cache-coherency logic.
	FBP-30	I/O processor module	A	$12,000	Single-slot, 12 SU board connects to FDDI, SAFENET, and Ethernet networks. A 33-MHz 68030 μP executes communication protocols. Contains two serial ports. PROM contains real-time OS-9 operating system.
	FBI-003	SCSI and adapter module	A	$3000	Single-slot, 12 SU board contains an NCR53C90A chip to control SCSI port. Two A32:D32 VMEbus expansion slots accept 6U VMEbus slave boards. Supports 7 levels of VMEbus interrupts.
	FBI-002	NTDS and 1553 adapter module	A	$10,000	Two-slot, 12 SU module controls a Navy Tactical Data System (NTDS) interface. Controls a MIL-STD-1553 serial data bus. Contains a 25-MHz 29000 CPU, 1 Mbyte of dynamic RAM, 2 serial ports, and 64-kbyte cache RAM having cache-coherency logic.
	FBI-004	A/D converter module	A	$12,000	Single-slot, 12 SU board contains an 8-channel 12-bit A/D converter. Programmable sample rate between 52k- and 1M-samples/sec. A 2k×64-bit FIFO buffer accommodates DMA transfers on Futurebus+.
Component Equipment Co	FX-2	2-mm connector	A	$0.08 per mated pair (press-fit OEM)	Right-angle, press-fit, contacts can be installed after board component assembly to eliminate solder bridges. One-piece connector body comes in 12- to 252-mm sizes.
Digital Equipment Corp	DECNIS600 -EP	Bridge-router	B	$15,000	Contains two T1 leased-line interfaces. Contains one N1 leased-line interface housed in a chassis containing 9 Futurebus+ expansion slots.
	DECNIS500 -EP	Bridge-router	B	$10,000	Contains two T1 leased-line interfaces. Contains one N1 leased-line interface housed in a chassis containing 4 Futurebus+ expansion slots.
DuPont Electronics	Metral Connector	2-mm connector	A, B, F	$0.05 to $0.10 per mated pair (OEM)	Complies with IEC 917 connector grid of 2.00×2.00 mm. Has blades for power connection. Family contains right angle solder-to-board; straight solder-to-board; hybrid power solder-to-board; hybrid coax; and coded connector systems. Modularity lets you concatenate different connector types in single-connector systems.
Force Computers Inc	FCPU-486	i486 CPU module	A, B	$9950	Single-slot, 12 SU board has 33-MHz i486 μP, 16 Mbytes of local dynamic RAM, 16 Mbytes of shared dynamic RAM, 2 or 4 EISA expansion slots, 2 serial ports, 1 parallel port, SCSI port, Ethernet port, graphics accelerator, 256-kbyte EPROM, 512-kbyte Flash EPROM, five 16-bit counters, 8 kbytes of nonvolatile RAM, and time-of-day clock. A PC-compatible BIOS permits DOS or Unix applications.
	F Subrack	Subracks	A, B, F	$495 (14-slot) $195 (5-slot)	Two versions have 14 or 5 slots. The 14-slot version fits 19-in. racks and has EMI shielding.
	F Backplane	Backplanes	A, B, F	$920 (4-slot) to $2130 (14-slot)	Models available with 4, 5, 7, or 14 slots. Support both distributed and central arbitration. ESD protection and surface-mount terminations.
	F Chassis-4/5	Chassis	A, B, F	$4995	Accommodates 4 or 5 64-bit modules, power supply, wiring harness, and fans. Comes with 750W power supply. Measures 550×600×210 mm. A hinged top provides access to disk-drive bay.

Company	Model	Product type	Profile	Price	Description
Future+ Systems	Futurebus+ preprocessors	Logic analyzer adapter	A, B, F	\$5500 (FS16564) to \$8800 (FS16528CA)	Single-slot, 12 SU boards adapt BTL Futurebus+ backplane signals to HP logic analyzer signals. Four versions consist of the FS16564 64-bit preprocessor, FS16564CA 64-bit preprocessor with central arbiter, FS16528 128-bit preprocessor, and FS16528CA 128-bit preprocessor with central arbiter. Any bus strobe signal can clock data into the analyzer.
Hybricon Corp	Series 222	System enclosure	A, B, F	\$9500	14-slot backplane has 128-bit data path and central arbitration. Hard metric enclosure has hard metric card guide and fits in a 19-in. rack. Contains a 1000W power supply and meets UL, CSA, VDE, and TUV requirements. Card guide accommodates board thickness from 1.4 to 2.57 mm. Measures 24×19.25×17-in. (609.6×488.95×431.8 mm) and weighs 85 lbs (39 kg).
	Series 224	Backplane	A, B, F	\$3000	14-layer backplane has 14 slots and bus bars for 5V, 3.3V, and G_{ND}. Supports 128-bit data path and distributed and central arbitration. Surface-mount terminations accommodate incident wave switching. Employs press-fit Metral connectors.
	Series 231	Wire-wrap boards	A, B, F	\$1900	12 SU×300-mm boards have 8 layers and handle 64- or 128-bit transfers. Contains National Semiconductor's arbitration, latching-data, and handshake BTL transceivers. Boards accommodate 230 16-pin DIPs or equivalent. 80 pins available for I/O on the E connector and 276 holes for front-panel I/O.
ITT Cannon	Tempus	2-mm connector	A, B, F	\$0.06 to 0.08 per mated pair	Connector modules come in 12-, 24-, 48-, and 96-mm lengths. Monoblocks come in 132-mm lengths and can be stacked lengthwise or side by side.
Mupac Corp	FJxx and FKxx	Backplane	A, B, F	FJ07, \$1543 (7-slot); FK09, \$2818 (9-slot)	FJxx family supports 64-bit data transfers. FKxx family supports 128-bit data transfers. 14-layer design has matched-signal trace lengths. Backplanes available having 5 to 14 slots.
	277 Series	Wire-wrap boards	A, B, F	\$1995	12 SU×300-mm boards have 8 layers. Boards have National Semiconductor's 64-bit BTL data transceivers.
	512 Series	Subracks	A, B, F	\$9700 (14-slot, 1200W power supply)	Available with 5 to 14 slots. Fits in 19-in. rack. Available with 1000W or 1200W power supply.
	529/539 Series	System enclosures	A, B, F	\$10,900 (14-slot, 1200W power supply)	529/539 Series mounts 12 SU boards vertically (5 to 14 slots). Desktop or 19-in. rack styles. Available with 1000W or 1200W power supply.
Nanotek Inc	NR3000-1	R3000 CPU module	A, B, F	\$5000	Single-slot 12 SU board has 25-MHz Mips R3000 CPU, R3010 coprocessor, 2-Mbyte secondary instruction and data cache, 2-Mbyte local RAM, 2-Mbyte global RAM, 1-Mbyte flash RAM, timer, real-time clock with battery-backed RAM, 2 serial ports, and programmable cache-coherency logic.
	NCA-1	Arbiter module	A, F	\$3500	Provides priority and fairness arbitration for 13 modules. Single-slot 12 SU board provides 64 priority levels. Sends power-fail arbitration message. Can send backplane length message on power up or system reset. System reset interface for front panel or power-system control.
	NFBIM-1	Interface module	A, F	\$12,000	Provides a Futurebus+ interface for custom designs. Single-slot 12 SU board has 32- or 64-bit data path, 32-bit address, split-transaction capability, compelled transaction, message passing, central arbitration support, and backplane I/O.
	NMEM-1	Memory module	A, B, F	\$5000 (16-Mbyte) \$11,500 (64-Mbyte)	Single-slot 12 SU board contains 16 or 64 Mbytes of dynamic RAM. Starting address is configurable through control and status registers (CSRs) on 1-Mbyte boundaries. Reports parity errors through status register. Supports 32- and 64-bit compelled transactions.
National Semiconductor Corp	DS38xx	Futurebus+ and BTL chip set	A, B, F	Transceivers, \$7.20 to \$14.40; arbitration controller, \$36.80	DS3875 Futurebus+ arbitration controller implements IEEE P896.1 arbitration. DS3883 BTL 9-bit data transceiver features controlled rise and fall times. DS3884 BTL 6-bit handshake transceiver features wired-OR glitch filters. DS3885 BTL arbitration transceiver incorporates competition logic. DS3886 BTL 9-bit latching data transceiver has an edge-triggered latch. DS3890 BTL 8-bit trapezoidal driver has open collector outputs with 6-nsec rise-and-fall times. DS3896/97 BTL trapezoidal transceivers have 6-nsec rise-and-fall times.
Schroff Inc	Metrix 2000	Enclosures and subracks	A, B, F	\$300 (6 SU×405-mm subrack)	Family of cabinets, cases, subracks, and plug-in units. Subracks have electromagnetic shielding. SU-compatible subracks accept 6U boards.
	Futurebus+ backplanes	Backplanes	A, B, F	\$829 (3 slots)	Backplanes have 3 or 14 slots and surface-mount terminations. Features distributed and central arbitration. Backplanes have 64-bit data paths and 192 I/O pins.

Table continued

FUTUREBUS + UPDATE

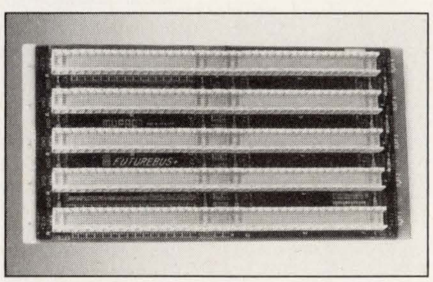
Table 1—(continued)

Company	Model	Product type	Profile	Price	Description
Schroff Inc (continued)	Minirack system	Development system	A, B, F	\$6000 (assembled, wired, and tested)	System is 355.6m high and 600 mm deep. Contains a 14-slot, 12-layer backplane. Features distributed and central arbitration.
Signetics Co	FB20xx	Futurebus+ chip set	A, B, F	\$7.50 (FB2040) to \$77 (FB2000)	FB2040 BTL 8-bit inverting transceiver has 100-mA drive and controlled transition times. FB2032 BTL 9-bit competition transceiver provides competition logic (4th qtr). FB2031 BTL 9-bit latched/registered transceiver has 100-mA drive. FB2030 BTL 9-bit address/data transceiver has controlled transition times. FB2012 BTL central arbitration controller has 14 bus grant lines, 14 request lines, and priority preemption. FB2000 protocol controller features parallel protocol transactions, asynchronous operation, queued packet mode, and programmable glitch filters.
Tektronix Inc	92DM911	Logic analyzer adapter	A, B, F	\$9950	Adapts a Futurebus+ backplane to the company's DAS9200 logic analyzer equipped with two Centurion cards. Package consists of adapter card, setup/display software, and manual. Features 100-MHz synchronous or asynchronous clocking and triggering. Memory depth is 128 kbits on each channel.
Teradyne Connection Systems	VHSICon	Connectors	M	\$0.75 per mated contact pair (OEM)	Conforms to the Standard Electronic Module-E (SEM-E) format for the P1101.4 specification. Connectors measure 5.44×0.58 in. Connectors come with 396 contacts on an 8-row 0.1×0.05-in. staggered grid.
Texas Instruments	TFB20xx	Futurebus+ chip set	A, B, F	\$26 (TFB2010) \$292 (TBF2022) \$81 (TFB2002)	TFB2010 arbitration bus controller features distributed arbitration, 256 priority levels, and 4-level incoming-message FIFO buffer. Handles messages for event-driver interrupts in control-arbiter systems. TFB2022 data path unit provides a 64-bit data interface to Futurebus+. Provides 32-bit dynamic addressing, compelled and packet mode, and a 32-transfer buffer. TFB2002 I/O controller controls host-to-Futurebus+ reads and writes. Contains JTAG test port.

stead, the Navy has opted for the Standard Electronics Module (SEM-E) connector specified in the incomplete P1101.4 document. The archetype for the SEM-E connector is Teradyne's VHSICon UHD interconnection system.

Telecommunications companies are working on Profile T for use in central-office switching units. The high-performance capabilities of Futurebus+ are only secondary features, however. The prime concerns in this application are fault tolerance, live insertion, and ease of maintenance, which are part of the Futurebus+ attractions. Currently, the greatest debate is over Profile T's acceptable level of tolerance to glitches when modules are inserted or removed in a live system. Profile T is scheduled to be circulated for working-group ballot in November 1992.

Because Digital Equipment Corp (DEC) has been a long-time advocate of Profile B as a high-speed backplane I/O bus, it isn't surprising that many of the initial and soon-to-be systems conform to this profile. DEC demonstrated an operational computer system having a Profile B I/O backplane at Buscon '92 West. DEC also demonstrated a Profile B multiprotocol network router, a communications controller, backplanes, and card cages at



The Futurebus+ backplane employs a metric connector that has pins on a 2×2-mm grid. This 5-slot backplane from Mupac is compatible with a 64-bit Profile A or B data path and accommodates central arbitration.

the show. Volume shipments of Profile B products are scheduled for later this year.

Raytheon also demonstrated a complete working Futurebus+ computer system at Buscon '92 West. The Raytheon workstation conforms to Profile A or F standards and has either a 14-slot 12SU hard-metric or a 6U soft-metric backplane. The system contains either a Motorola 68040 or a Mips R4000 or R3000 μP; 100-Mbps Safenet II and Ethernet LAN adapters; an NTDS Fast adapter; a 1553-B adapter; 16 Mbytes of global RAM; a central arbiter; and a bridge to a Silicon Graphics graphics subsystem.

Raytheon made significant contributions to the electrical specifications of the IEEE 896.2 profiles. The company created Spice models of all transmission-line, transceiver, crosstalk, and parasitic effects for the 12SU backplane. Raytheon de-

FUTUREBUS+ UPDATE

veloped over 300 Spice simulation studies to model worst-case loading scenarios. The IEEE working committee adopted the resulting recommendations to guarantee interoperability of products. Raytheon is currently accepting custom Futurebus+ workstation designs for DoD and NASA vendors. (For further information, contact Joe Cooper at (508) 440-3655.)

Chip sets make the bus

Possibly the greatest boon resulting from document approval is the availability of chip sets to implement the Futurebus+ protocols. In 1990, Nanotek, one of Raytheon's subcontractors, introduced the first commercially available CPU board for Profile A. At that time, uncertain specifications and consequently unavailable silicon forced the company to execute the suite of protocols using 50 PLDs on a single 6U board. Nanotek president, Joe George, estimates that the protocol chips scheduled to be announced at Buscon '92 East, could eliminate 30 of these PLDs.

Both National Semiconductor and Texas Instruments plan to introduce Futurebus+ protocol silicon at Buscon '92 East. National Semiconductor will announce the DS3805 Futurebus+ Protocol Controller, which is compliant with Profile B specifications. The chip's TTL-compatible I/O ports interface with the company's DS3875 arbitration controller chip, the company's broad range of BTL transceivers, and a host-processor local bus.

Newbridge Microsystems cooperated with National Semiconductor to develop the DS3805 protocol controller. Newbridge, which is a fabless semiconductor facility, has a foundry agreement to second source National's Futurebus+ chips. Newbridge designates the protocol con-

A Futurebus+ primer

Even though the history of Futurebus+ dates from the mid-1980's, many engineers are unfamiliar with this architecture because of the absence of real products. Futurebus+ derives its name from its ability to incorporate any future processor into an existing multiprocessor system. To meet this objective, Futurebus+ offers the following features:

1. An open standard architecture that is independent of processor and technology
2. An asynchronous data-transfer protocol, called compelled mode, that provides handshake flow control for each word transfer
3. An optional source-synchronous burst transfer protocol, called packet mode, that provides flow control over each block transfer
4. A split-transaction protocol, which allows a master to relinquish the bus when requesting data from a slow slave
5. Upper performance limits based on physics rather than technology
6. Parity protection on all lines
7. Multiple priority levels and fairness arbitration for real-time applications; either central or distributed arbitration
8. Fault tolerance, live insertion and withdrawal of modules, and fault detection and isolation
9. A snooping cache-coherent shared-memory system that utilizes the MESI model
10. Message passing between modules that uses control and status registers (CSRs).

Futurebus+ defines a 64-bit address and data path that you can implement using any logic family that meets skew and incident-wave switching requirements. The Backplane Transceiver Logic (BTL) family is recommended. In addition, Futurebus+ defines an optional 32-bit subset and 128- and 256-bit supersets of the address and data path. Current technology permits 25 M transfers/sec, which provides 100-Mbyte/sec transfers for low-end systems having a 32-bit data path. Backplane physics limits the upper transfer rate to 100 M transfers/sec. Therefore, the theoretical maximum transfer rate for a 256-bit data path is 3.2 Gbytes/sec

Although Futurebus+ specifies a variety of options, interoperability is guaranteed by defining specific profiles that products should conform to. The IEEE 896.2 document finalizes Profiles A, B, and F. These profiles employ a metric mechanical form factor, defined in IEEE 1301, that has subrack dimensions based on a 25-mm standard unit (SU). A 12SU card, which measures 265× 160 mm, is slightly taller than a 6U (233×160mm) VMEbus board. Therefore, subrack vendors can offer enclosures containing both backplanes to accommodate a VMEbus-to-Futurebus+ bridge. To obtain more detailed information on Futurebus+ specifications, you can purchase related documents from:

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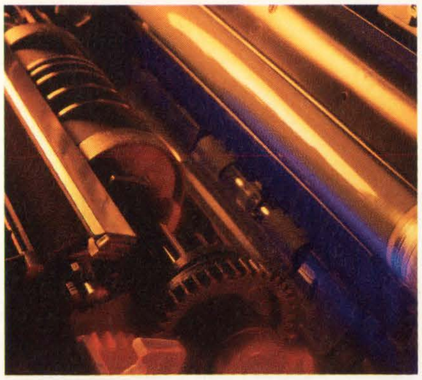

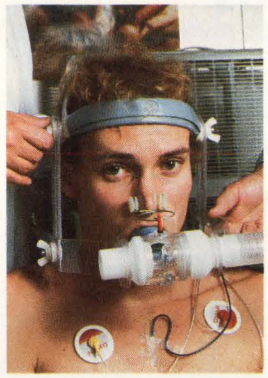

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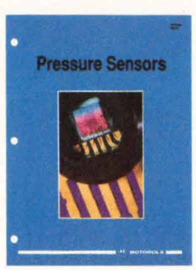

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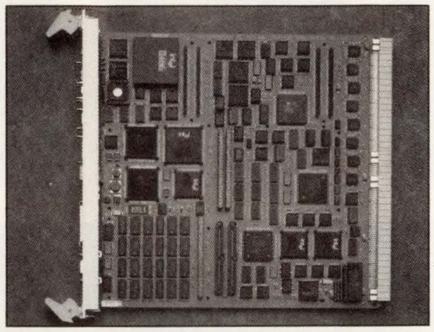
troller chip as CA91C899. The chip will support compelled-, packet-, and split-mode transactions. Burst-transfer register length is selectable from 1 to 64 transfers, and the chip supports 32- and 64-bit data and address paths.

Initial offerings of the protocol controller will handle 10 to 15 M transfers/sec or 80 to 120 Mbytes/sec in a 64-bit system. A subsequent version will handle 25 M transfers/sec. The chip can reinitiate transactions, if a slave is busy, and it includes address-decoding logic for Profile B's control and status registers (CSRs). The chip supports both central and distributed arbitration but doesn't implement the MESI suite of protocols for cache coherency.

Texas Instruments plans to announce a 3-chip chip set at Buscon '92 East. Force Computers, which is one of Litton Data Systems' subcontractors, provided system-level consulting for the development of the chip set. The TFB2010 arbitration bus controller implements a distributed arbiter for Profiles A and B and handles event-driven interrupts in central arbiter sys-



The FCPU module conforms to Profile A or B specifications. The 12SU board from Force Computers Inc employs an Intel 486 µP, 16 Mbytes of RAM, and 2 or 4 EISA expansion slots. A PC-compatible BIOS lets the board run DOS or Unix applications.

For more information . . .

For more information on the Futurebus+ products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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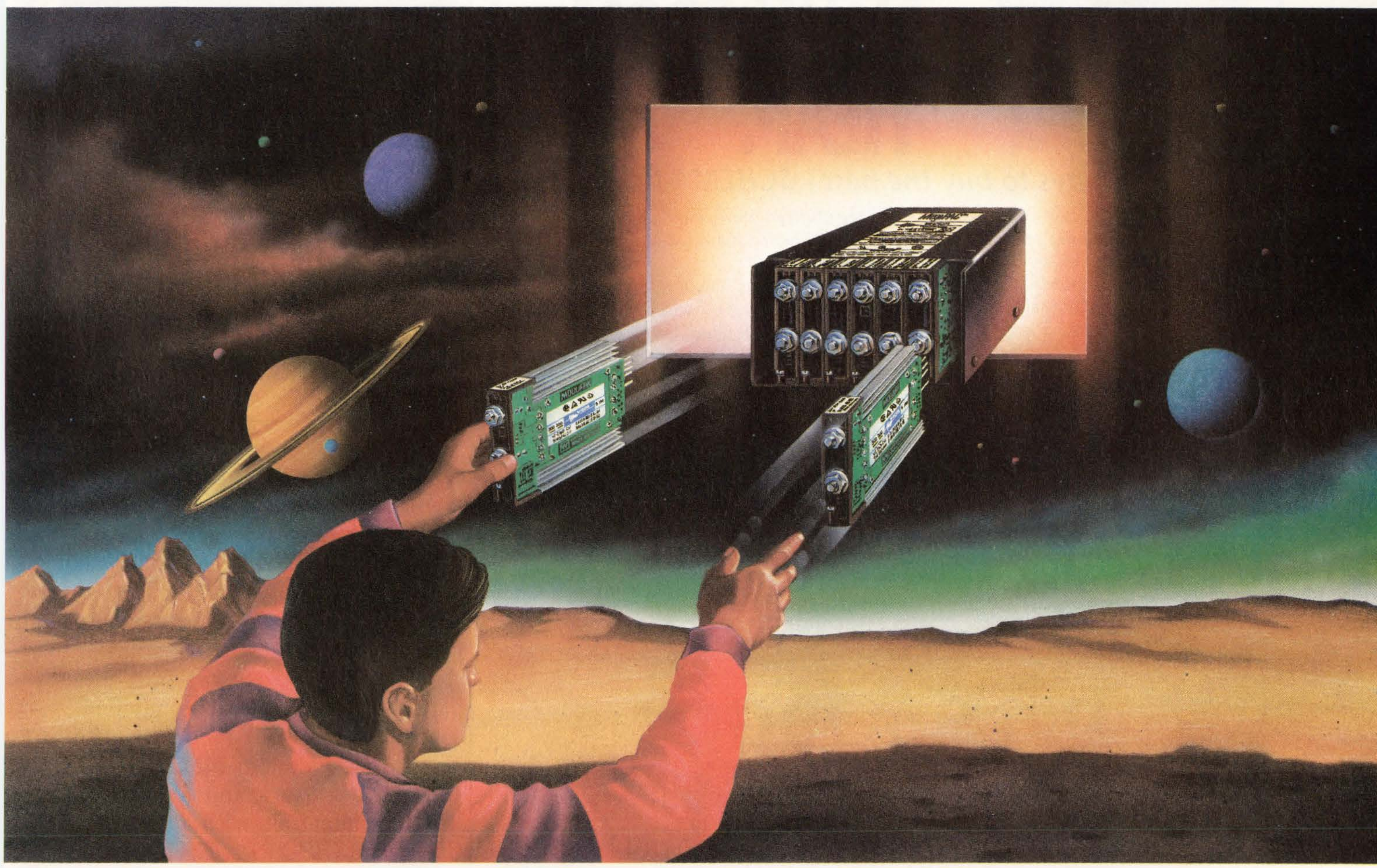

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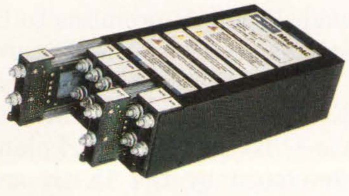

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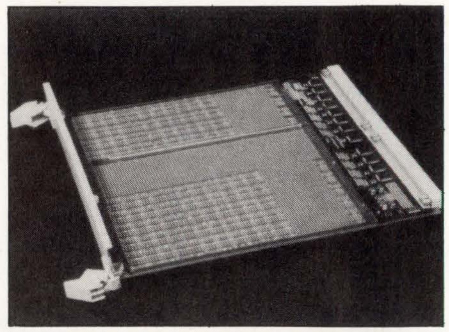

To facilitate the development of Futurebus+ prototype boards, Hybricon offers a 12SU, 8-layer, wire-wrap board having 9-bit BTL transceivers and stub matching to meet incident-wave switching requirements.

tems. The device maintains a round-robin bit for fairness and provides 256 priority levels.

The TFB2002 I/O controller and the TFB2022 data-path unit are optimized for Profile B transactions and decode addresses for transfers to memory, mailboxes, or CSRs. The chips implement compelled-, packet-, and split-mode transactions. The chip set interfaces with BTL transceivers and a local bus that is compatible with a variety of RISC and CISC μPs. Each chip has a JTAG test port. The chip set does not implement the MESI model for cache coherency. Signetics has an alternate-source agreement with TI to second source these parts and an extensive line of BTL transceivers.

Turning the ¼ pole

Though Profile B promises to be the early flag bearer of the Futurebus+ banner, other spin-offs from the IEEE effort are apparent. Futurebus+ is the first backplane ever developed by the IEEE and as such is an open standard and requires no licenses or fees. Consequently, many system designers are employing some Futurebus+ features in custom designs. Michael Thompson, technical manager at Schroff, says that the majority of the current orders for high-per-

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formance backplanes are for custom configurations employing BTL transceivers.

Interest in Futurebus+ is high in Japan also. The VME member association in Japan, which consists of 50 vendors, is promoting Futurebus+ for use in high-performance computing applications. The VME member association is similar to the VME International Trade Association (VITA) group in the US. Both groups advocate the Futurebus+ backplane for performance exceeding the VMEbus capability (see **box 2**).

European interest depends on who you talk with. While most vendors detect a cool reception to Futurebus+ in Europe, DEC indicates it has received a number of proposals from the continent for systems that hinge on the soon-to-be-available Profile B silicon. Although Futurebus+ must still make the familiar transition of high cost for a few new systems to moderate cost for more volume, the curve of real output versus development time is beginning to bend. EDN

References

1. Gallant, John, "Futurebus+," *EDN*, October 1, 1990, pgs 86-98.
2. Gallant John, "Protocols keep data consistent," *EDN*, March 14, 1991, pgs 41-50.

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CIRCLE NO. 48

Silicon accelerometers tackle cost-sensitive applications

RICHARD A QUINNELL, Technical Editor

Tough, accurate, and affordable, silicon sensors are entering high-volume markets. And, entry into these markets promises to spur further improvements.

High-powered DSP chips and powerful microcontrollers are still indebted to the lowly sensor for their ability to take on innovative real-world applications. For applications involving motion, that sensor is the accelerometer. In recent years a variety of low-cost precision accelerometers have become available that stem from adaptations of silicon-processing techniques used in the semiconductor industry.

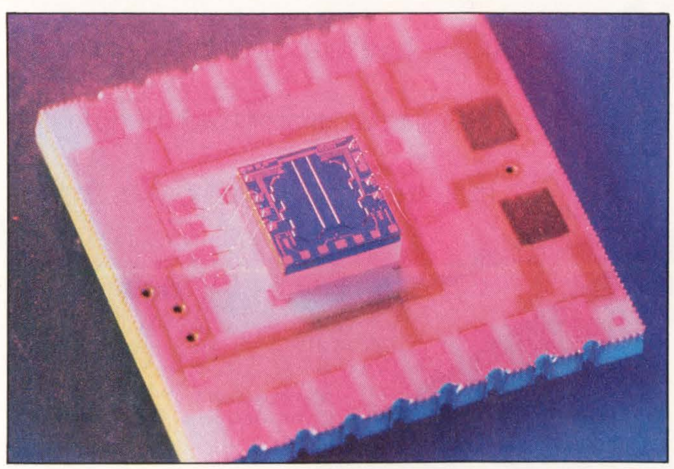
Micromachining, the ability to shape silicon, is the genesis of silicon accelerometers. There are two types of micromachining: bulk and surface. Bulk micromachining uses acids, which naturally etch faster along one lattice direction than another, to cut well-defined channels in crystalline silicon. Such channels typically cut all the way through the wafer, creating stencil-like shapes. Surface micromachining confines the action of acids to thin layers, which are created by diffusion and other surface treatments. Both allow the shaping of silicon into a basic accelerometer.

The basic accelerometer is nothing more than a mass suspended from a spring (**Fig 1**) within a frame. If the frame undergoes an acceleration along the spring's axis, the mass (called a seismic mass) remains unaffected until the spring exerts the necessary force. By equating Newton's law, F=ma, with the spring force-displacement relationship, F=kx, you obtain a relationship between the acceleration and the seismic mass' displacement.

Even the simple model gives some insights into the concerns that arise when using this measuring technique. One problem is that an impulse to the mass will set up an oscillation unless the system's motion is damped. Another concern is that the system can falsely report acceleration along the spring axis when none exists. Any transverse force on the mass, for example, will still stretch the spring, resulting in a false reading. Vibration rectification can also distort the reading. If the displacement sensor exhibits nonlinearities, it can produce frequency mixing when subjected to random vibration and thus report low-frequency motion that doesn't exist. You cannot filter out such erroneous signals.

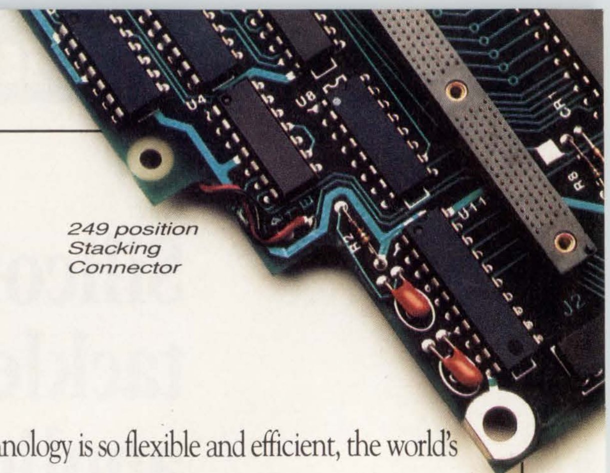
Complex shapes solve problems

Several improvements in silicon-processing technology have helped sensor manufacturers address these concerns.



Many silicon accelerometers, such as this device from Lucas Nova Sensor, come in surface-mount configurations with additional circuitry on the ceramic base.

1,156 position
LGA Socket



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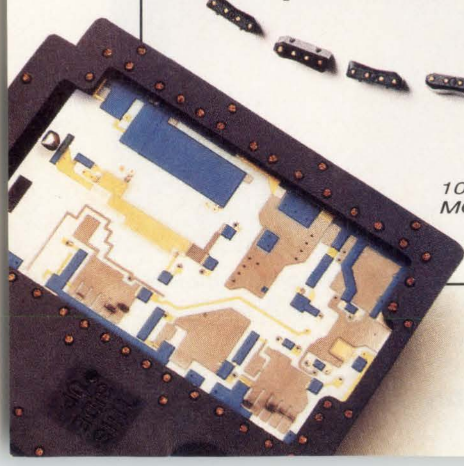

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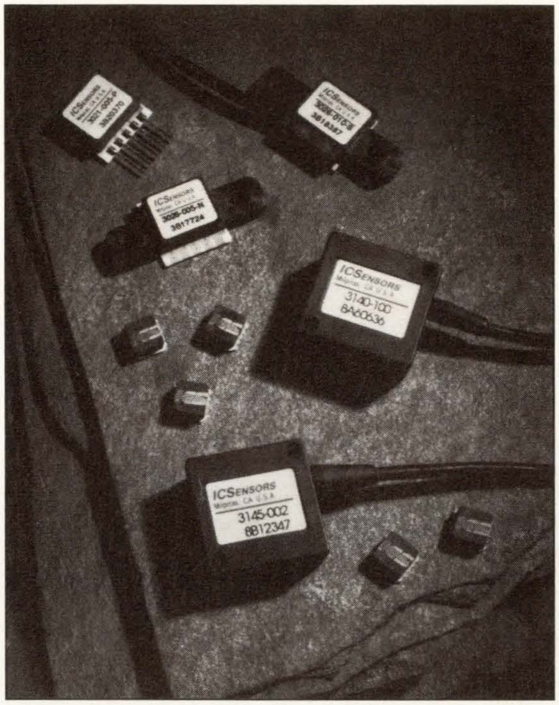
CIRCLE NO. 49

SILICON ACCELEROMETERS

One such improvement is the advent of silicon fusion bonding, first applied to sensors four years ago. This technique allows the bonding of two wafers while preserving the crystalline structure of the silicon crystal across the boundary. Fusion bonding permits the creation of complex 3-D structures without introducing mechanical discontinuities or thermal-dependent stresses.

This structuring ability lets accelerometer manufacturers capture the seismic mass within a sealed cavity by bonding a cap and a base plate to the frame. By controlling the space between the mass and cavity, vendors are able to use the air sealed inside the cavity to serve as a viscous damping fluid for the system's motion.

Prior to fusion bonding, either the frame was captured between layers of glass, or oil was used as the damping fluid. Both techniques contributed to temperature-dependent error, either because of a mismatch in expansion coefficient causing distortion in the springs or because the viscosity of oil changes with temperature.



Accelerometers come in a variety of packaging options, from surface-mount sensor-only devices to encapsulated sensors with built-in signal conditioning.

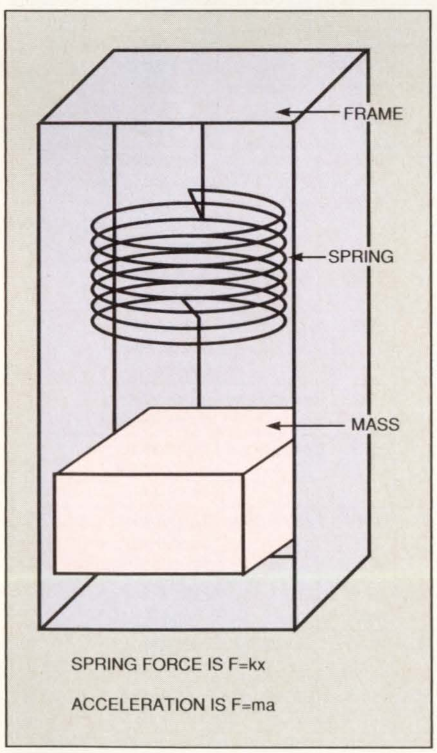


Fig 1—The mass suspended from a spring serves as a basic accelerometer. By relating force equations, you can use the spring's displacement as the measure of acceleration.

Shock resistance built in

Silicon fusion bonding has also provided an answer to another limitation on earlier silicon accelerometers: shock resistance. Simply falling off of a desk can produce a 200g shock when the sensor hits the floor. Even though silicon is a tough and flexible material, that kind of shock is able to break the springs in an accelerometer unless you limit the seismic mass' motion. Silicon fusion bonding has allowed the placement of bumbers and other mechanical stops that make the accelerometer much more shock resistant. Devices now routinely handle shocks as great as 2000g.

The remaining concerns vendors address with their design approach. The various approaches make different tradeoffs between error sources. One choice to make is how to sense the displacement. Another is how to connect the spring and mass. The variations available include having a single- or double-cantilevered or a membrane support as the spring, with either piezoresistive or capacitive displacement sensors. The combination you choose will determine the interface circuitry you will need, although some devices have that circuitry built in. **Table 1** gives an overview of representative devices.

Fig 2a is a diagram of a single-cantilevered design. Thin beams support one edge of a seismic mass, which is free to move within a cavity created by fusion-bonding two additional wafers to the one containing the mass. Piezoelectric resistors fabricated at the beams measure the displacement by changing resistance as the beams bend. The double-cantilevered approach, shown in **Fig 2b**, supports the mass from two sides.

Single-sided support is simpler

The single-cantilevered configuration has several advantages. Because the mass is supported by fewer beams, for example, the beams in a single-cantilevered structure see more stress for a given-sized mass. This makes the structure more sensitive than the double-cantilevered structure, resulting in smaller devices for a given sense range.

The single-cantilevered devices are also the simplest electrical circuit to interface with. Because piezoelectric resistors are highly temperature sensitive, you must provide temperature compensation to maintain accuracy. The single-cantilevered devices are the easiest to compensate.

They do have drawbacks, however. For one, the spring action that the single-cantilevered structure supplies is not normal to the surface of the chip but is angled by as much as 9°. Unless accounted for when the device is mounted, this mismatch between the spring and acceleration forces can result in reduced accuracy.

Table 1—Representative silicon accelerometers[1]

Company	Model	Dynamic range (±g)	Shock protection (g)	Linearity (% full scale)	Upper frequency (Hz)	Sensitivity (mV/g)	Transverse sensitivity (%)	Temperature range (C)	Weight (grams)	Price (100)	Sensor type	Special features
Analog Devices	ADXL50	50	2000	0.5	1000	20	2	−55 to +125	0.98	$23	Capacitive	On-chip signal conditioning and self-test. Costs $5 (100,000+).
Endevco	7264A	2000	10,000	1	5000	0.20	3	−54 to +121	1	$550	Piezoresistive	
	7290A-2	2	5000	0.2	50	1000	2	−54 to +121	10	$1095	Capacitive	
	7290A-10	10		0.2	500	200				$995		
	7290A-30	30		0.2	800	66				$995		
	7290A-100	100		1	1000	20				$995		
IC Sensors	3021/26-002	2	400	1	250	8 to 20	3	−40 to +125	1.4	$108	Piezoresistive	Available in 2, 5, 10, 20, 50, 100, 200, and 500g ranges.
	3021/26-050	50	1000	1	1000	1.5	3	−40 to +125	1.4	$108		
	3031-002	2	400	1	350	1.7 to 3	3	−40 to +125	0.3	$74	Piezoresistive	Available in 2, 5, 10, 20, 50, 100, 200, and 500g ranges.
	3031-050	50	1000	1	2000	0.6 to 1.5	3	−40 to +125	0.3	$74		
	3140-002	2	400	<1	250	1000	3	−20 to +85	13	$295	Piezoresistive	Temperature compensated to 1% accuracy, 2, 5, 10, 20, 50, and 100g ranges available.
	3140-050	50	1000	<1	1600	40	3	−20 to +85	13	$295		
	3145-002	2	400	<1	250	1000	3	−20 to +85	13	$230	Piezoresistive	Temperature compensated to 1% accuracy, 2, 5, 10, 20, 50, and 100g ranges available.
	3145-050	50	1000	<1	1600	40	3	−20 to +85	13	$230		
Lucas Nova Sensor	NAC-103	2	2000	0.5	200	6	3	−30 to +85	1	$68	Piezoresistive	Temperature compensated
	NAC-203	50	2000	0.5	500	0.8	3	−30 to +85	1	$76	Piezoresistive	Temperature compensated, self-test.
	NAH-5-02	2	2000	0.5	200	6	3	0 to 70	1	$68	Piezoresistive	Temperature compensated
	NAH-5-050	50	2000	0.5	500	0.8	3	0 to 70	1	$68	Piezoresistive	Temperature compensated, self-test.
	NAS-002	2	2000	1	200	1250	3	0 to 70	5	$169	Piezoresistive	Temperature compensated with signal conditioning.
Silicon Designs	1000-010	10	100	1	800	0.08 (Note 2)	3	−55 to +125	0.75	$119 (1000)	Capacitive	Pulse-density TTL output signal.
	1000-025	25	250	1	1000	0.20 (Note 2)	3	−55 to +125	0.75	$119 (1000)	Capacitive	Pulse-density TTL output signal.
	1000-050	50	500	1	1600	0.40 (Note 2)	3	−55 to +125	0.75	$119 (1000)	Capacitive	Pulse-density TTL output signal.
	1000-100	100	1000	1	2000	0.80 (Note 2)	3	−55 to +125	0.75	$119 (1000)	Capacitive	Pulse-density TTL output signal.

Notes:

1. Values given are maximum ratings unless noted.
2. Sensitivity is measured in milligrams per pulse per second.

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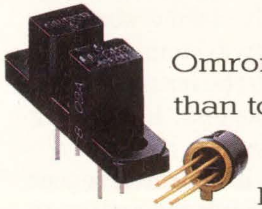

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CIRCLE NO. 51

SILICON ACCELEROMETERS

Double-cantilevered structures have no such mismatch. They also have the advantage of lowered transverse sensitivity. Because the seismic mass' center of mass lies below the plane of the support beams, as shown in **Fig 3**, a transverse force will tend to twist the mass, causing a false reading. By having resistors on both sets of beams, the double-cantilevered device can distinguish between normal acceleration, which bends both beams the same way, and a transverse acceleration. Proper design of the resistor network can make it self-compensating for transverse forces.

Supporting the mass on all four sides will reduce transverse sensitivity still further. Such structures, however, typically use capacitive sensing of the seismic mass' displacement. **Fig 4** shows a typical capacitive-sensing device. These devices have the advantage of being relatively insensitive to temperature variations, but require much more complex and sensitive interface circuitry than piezoresistive sensors.

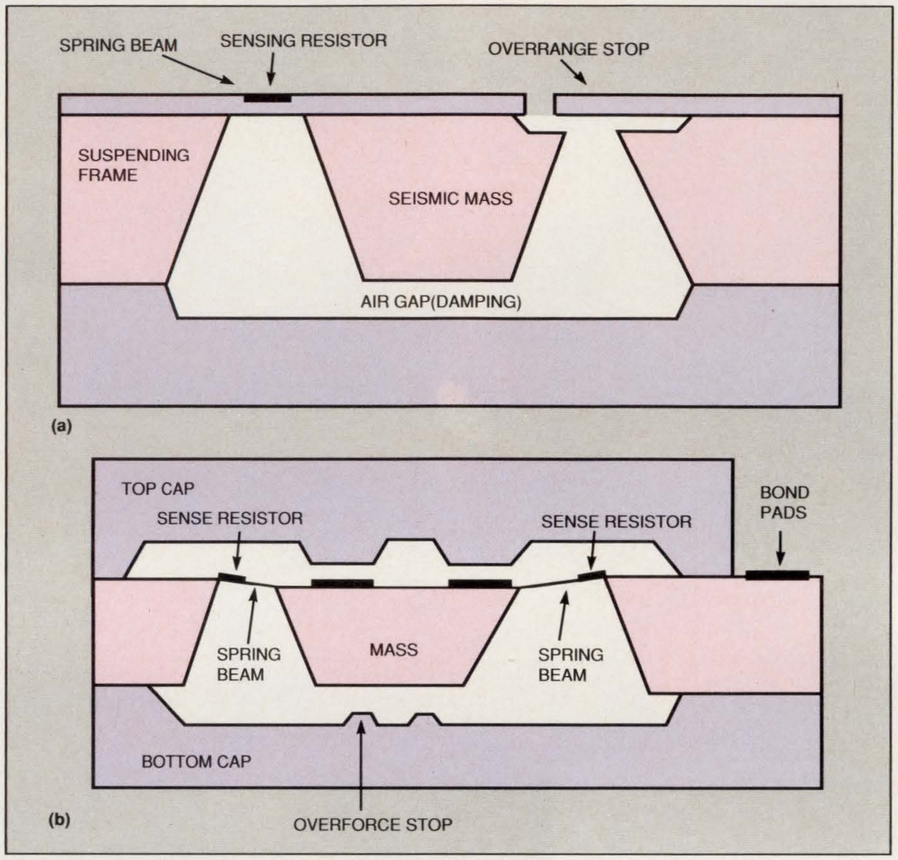

Fig 2—Silicon accelerometers make a mass and spring by suspending a block from a set of beams. Single cantilevered (a) and double cantilevered (b) are common configurations.

Capacitive sensors add circuits

As a result, many capacitive sensors have the necessary circuitry built in. Most put both sensor and circuits into a ceramic module, as with the Silicon Designs devices. Analog Devices takes a unique approach with its ADXL-50; it integrates everything onto the same piece of silicon.

The ADXL-50 is unique in another way, as well. Its seismic mass is not a single block but a series of interdigitated fingers fabricated using surface micromachining (**Fig 5**). These fingers stand on posts above the chip's surface and are sensitive to acceleration in the plane of the chip. All other accelerometers respond to acceleration normal to the surface. The ADXL-50 also has an extremely low cost for this type of device, dipping to as low as $5 in large volumes.

The drawback of complicated interface circuitry in a capacitive sensor is compensated for by an additional ability inherent in the capacitor structure. The presence of charge-carrying plates in the sensors gives them a built-in means for applying an electrostatic force on the seismic mass. This capability lets the sensor be used in a closed-loop configuration.

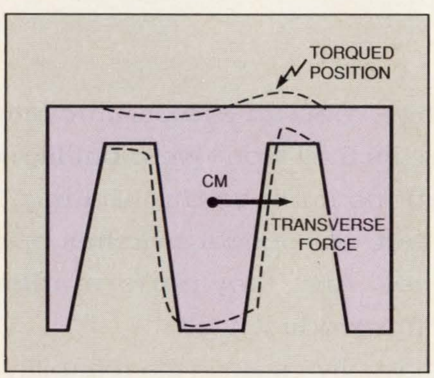

Fig 3—An off-axis acceleration can show up as a spring displacement for a double-cantilevered mass because of torquing. If the mass's center were in line with the beams there would be no effect.

Closed loop improves linearity

Instead of letting the seismic mass move freely during acceleration, a closed-loop system applies a restoring force to the mass, keeping it relatively motionless. Restricting the mass' movement has two advantages. First, it improves sensor linearity by confining the motion to the linear region of the spring's restoring force. Second, it extends the range of a sensor beyond the limits imposed by its housing on the seismic mass' movement. In such force-feedback systems the restoring force, not the actual movement, serves as the measure of acceleration.

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SILICON ACCELEROMETERS

The ability to apply a force to the proof mass has an additional advantage; it gives the sensor a self-test capability. This capability is particularly important in systems such as automotive airbags, where you cannot test the system by actually accelerating it, yet testing is necessary for safety or reliability.

Electrostatic deflection capability can be added to piezoresistive devices. The problem is that it requires as much as 100V to run the test even though the sensor itself needs only 5 to 12V. Lucas Nova Sensor has developed a novel self-test mechanism for its piezoresistive sensors that does not require such high voltages. In its 50g NAC and NAH sensors, the company has added a support beam that has heating resistors built in. By heating the beam, you can make it expand more than the surrounding silicon, causing it to buckle and push down the seismic mass.

Such innovation as this novel self-test scheme and the fully integrated ADXL-50 sensor is part of a wave of new ideas likely to appear in silicon accelerometers in the near future. The emergence of a high-volume market for accelerometers in the automotive industry, where they are used to trigger the deployment of airbags in accidents and to monitor vibration for active suspension systems, has fueled research and development. The payoff is likely to be continually improving performance and lowered costs of silicon accelerometers for all applications.

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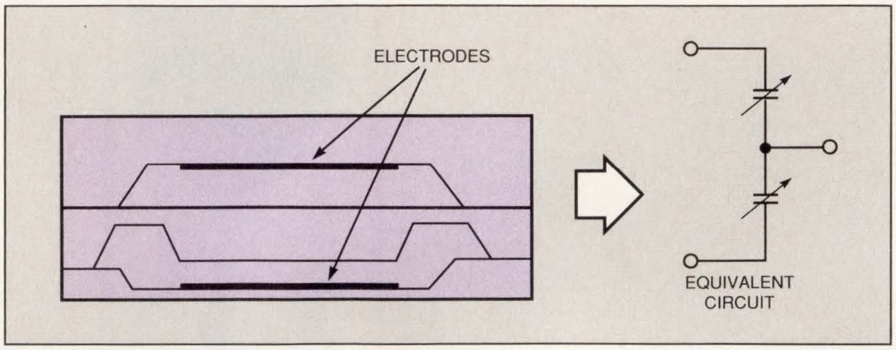

Fig 4—Capacitive sensors use top and bottom plates to form a capacitor divider with the seismic mass that is temperature insensitive. Sensing the change in capacitance requires relatively complex circuitry, however.

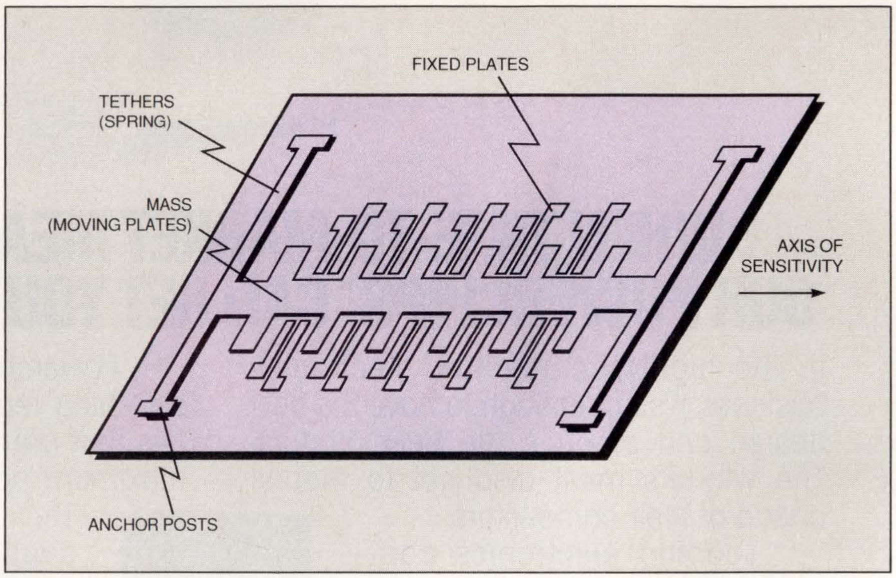

Fig 5—The seismic mass of the AXDL-50 from Analog Devices is a unique interdigitated comb supported by four posts. Its sensitivity is along the surface, not normal to it as with other sensors.

Reference

1. Allen, Henry V, Stephen C Terry, and James W Knutti, "Understanding Silicon Accelerometers," *Sensors*, September 1989, pgs 17 to 31.

Article Interest Quotient
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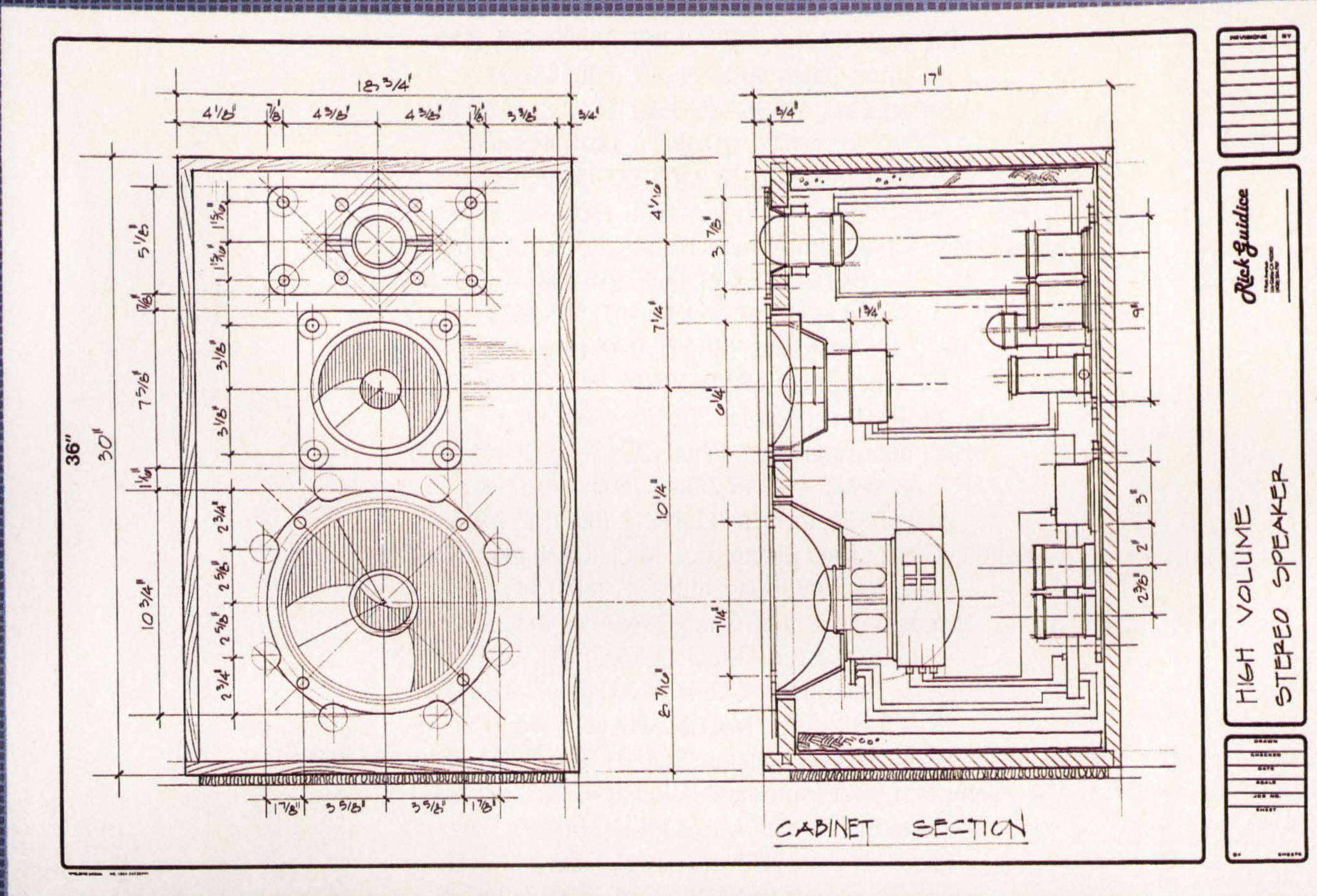

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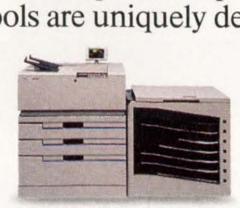

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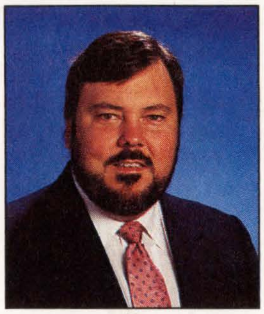
CIRCLE NO. 53

Tape drives proliferate despite format diversity

MAURY WRIGHT, Contributing Editor



Floppy-interface minicartridge tape drives dominate the PC market. New SCSI models with gigabyte storage capacities will move this low-cost drive class into workstation and midrange computing applications.

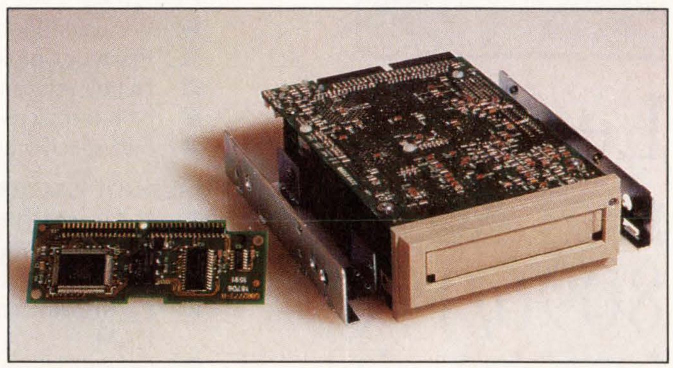
Minicartridge tape drives haven't been receiving the headlines allotted to DAT and other cartridge drives, but the 3½-in., low-cost units make up the fastest growing segment of the tape industry. This success comes despite the lack of industry-wide agreement on a single recording format—typically a requirement for removable mass-storage devices to succeed. Most sales of the minicartridge drives to date have been in the PC market, but manufacturers are primed to offer new gigabyte-class drives that will suit applications ranging from power PCs and workstations to LAN servers and midrange business systems.

Whether you're designing or buying computers, you're likely to encounter DC-2000-class minicartridge tape drives in the near future. Ever increasing hard-disk capacities are making tape backup a virtual system requirement—even in PCs. And the minicartridge drive class includes models having combinations of capacity, performance, and price specs that satisfy a wide range of applications.

Small size an advantage

Drive size will be key to the proliferation of minicartridge drives. The computer industry has adopted 3½-in. hard-disk drives as the most popular drive size, and 3½-in. floppy-disk drives far outnumber 5¼-in. drives in new computers. As 5¼-in. slots rapidly disappear from computer cases, the smaller tape drives are becoming more desirable.

Minicartridge drives are one of three available types of tape drives that fit the 3½-in. form factor. Data-cassette drives also fit this form factor, but they have never attained significant market share and only Teac still offers such drives. DAT (digital-audio-tape) drives also fit in 3½-in. slots, are growing in popularity, and provide the only real alternative to minicartridge drives. Currently, DAT drives store substantially more data but cost substantially more than minicartridge drives. Exabyte (Boulder, CO) has indicated that it will eventually offer a 3½-in. version of its 8-mm helical-scan drives, but the company hasn't announced when such drives will be available.



A storage capacity of 450 Mbytes and a SCSI interface are features of the Archive Adder minicartridge drive. The unit uses a format that is an extension of the Accutrak format, which Irwin Magnetics developed.

Minicartridge drives range in storage capacity from 40 to 566 Mbytes. Late this year or early next year, expect announcements of drives that store at least 875 Mbytes as well as more new drives that offer capacities in the 500-Mbyte range. **Table 1** summarizes both available minicartridge drives and those that should be available within the next year.

Universal 8051/52 Family	
Intel 8031	32 MHz
Intel 8032	24 MHz
Intel 80C31	32 MHz
Intel 80C32	24 MHz
Intel 80C51FA	16 MHz
Intel 80C152	16 MHz
Intel 8048/49/50	11 MHz
AMD/Siemens 80515	16 MHz
AMD/Siemens 80535	16 MHz
AMD/Siemens 80C535	16 MHz
Siemens 80537	16 MHz
Siemens 80C537	12 MHz
Siemens 80C517	16 MHz
Signetics/Philips 80C451	16 MHz
Signetics/Philips 83C451	16 MHz
Signetics/Philips 87C451	16 MHz
Signetics/Philips 80C552	16 MHz
Signetics/Philips 8XC552	16 MHz
Signetics/Philips 83C751	16 MHz
Signetics/Philips 87C751	16 MHz
AMD 80C321	16 MHz
AMD 80C325	16 MHz
AMD 80C525	16 MHz
AMD 87C525	16 MHz
Intel 8096/196 (KB, KC, KR, KQ, JR, JQ)	
8096/80196	16 MHz
8098/80198	12 MHz
Zilog Z8, Super-8	
Z8	20 MHz
86C94	30 MHz
Super-8	20 MHz
Texas Instruments DSP's	
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320C16	35 MHz
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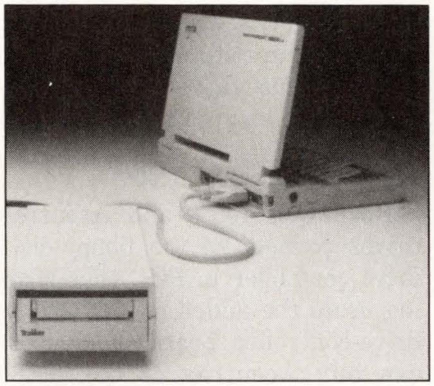
* System capable of 32 MHz; actual emulation speeds limited by currrent device speeds.

CIRCLE NO. 55

MINICARTRIDGE TAPE DRIVES

Two drive types make up the minicartridge industry: drives whose formats conform to standards set by the QIC (quarter-inch cartridge) industry trade group and drives that use proprietary formats and were developed by individual companies. Given such a diverse group of drives having incompatible formats, the minicartridge industry has succeeded amazingly well. Traditionally, computer users haven't accepted new classes of removable mass-storage products until an industry-standard format emerges. Diverse media and formats have significantly hurt the optical-disk industry.

Format incompatibility has hampered growth in every segment of the tape-drive industry except the minicartridge drives. For example, competing formats for DAT drives delayed real market acceptance of this product class for more than two years. System designers incorporating 5¼-in. DC-600-style data-cartridge drives demanded that manufacturers agree on a single QIC format for each new drive that raised a cartridge's storage capacity. These designers also demanded that higher-capacity products be able to read tapes recorded with older drives.



The parallel-port interface of Colorado Memory Systems' Tracker drives lets users back up notebook computers and share a tape drive among several desktop systems.

Low cost suits PC users

Drive cost—not competing formats—has proved to be the biggest barrier to the widespread use of any of the three tape-drive types in PCs. Users either didn't backup their hard drive because it was too much trouble and tape drives cost too much, or they used floppy disks for system backup because their hard drives held only 20 to 40 Mbytes of data.

Two trends spurred PC users to adopt minicartridge tape drives. First, manufacturers led by Archive's Irwin OEM Div and then by

Table 1—Minicartridge drives and manufacturers

Drive type	Capacity (300-ft tape, Mbytes)	Transfer rate (kbytes/sec)	Tracks	Recording density	Interface	Read compatibility	Vendors	Price	Availability
QIC-40	60[1]	31 to 62	20	10,000 bpi	Floppy-disk controller	N/A	Colorado Memory, Everex, Summit, Wangtek	$250	Now
QIC-80	120[1]	31 to 62	28	14,700 bpi	Floppy-disk controller	QIC-40	Aiwa, Archive-Irwin, Colorado Memory, Everex, Iomega, Summit, Wangtek	$200 to $400	Now
QIC-100	60	42	24	10,000 bpi	SCSI	N/A	Georgens	$800	Now
QIC-128	128	98	32	16,000 bpi	SCSI	QIC-100	Georgens	$916	Now
QIC-410M	410[1]	200 to 300	32	38,750 ftpi	SCSI	N/A	Teac[2]	N/A	Early 1993
QIC-500M	500[1]	125 to 250	40	42,000 bpi	Floppy-disk controller, IDE	QIC-40,80	Archive-Irwin[2], Colorado Memory[2]	N/A	Early 1993
QIC-875M	875[1]	300 to 800	38	50,800 ftpi	SCSI	QIC-40,80	Archive[2], Wangtek[2]	N/A	Mid-1993
Accutrak 120	60[1]	62	24	10,700 bpi	Floppy-disk controller	N/A	Archive-Irwin	$199	Now
Accutrak 250	125[1]	62 to 125	32	14,700 bpi	Floppy-disk controller	Accutrak 120	Archive-Irwin	$249	Now
Adder	450[1]	217	40	34,000 bpi	SCSI	Accutrak 120,250 QIC-40,80	Archive	$540 sample	Now
Excel 1G	566[1]	567	40	51,667 bpi	SCSI	N/A	Everex	$1679[3]	Now
Micro streamer	155	122.5	29	14,440 bpi	SCSI	N/A	Teac	$390	Now
SE305	152[1]	125	28	14,700 bpi	IDE	QIC-40,80	Summit	$449	Now

Notes: bpi=bits per inch, ftpi=flux transitions per inch, IDE=Integrated Drive Electronics—an industry-standard high-disk interface, N/A=not applicable, QIC=quarter-inch cartridge, SCSI=Small Computer System Interface—a general-purpose I/O interface.
1. Data-compression options for these drives essentially double-specified capacity.
2. Expected manufacturers for new classes of drives.
3. Price includes an Adaptec 1510 SCSI host adapter.

MINICARTRIDGE TAPE DRIVES

Colorado Memory Systems found ways to substantially reduce the drives' price. Second, PC hard-drive capacities surged drastically. This increase was due to the needs of graphics-intensive programs and the fact that corporate users started storing large databases and other data on PCs rather than on larger systems. Computer users realized that tape was the only effective way to make sure they regularly backed up their data.

Two types of minicartridge tape drives vie for space in IBM PCs and compatibles. The first, Archive-Irwin's Accutrak drives, use the proprietary format Irwin Magnetics originally developed. QIC-40,80 drives are the second type of PC minicartridge drive. (QIC-40 and QIC-80 are actually two separate but closely related specs.) QIC members, who produced the larger DC-600-style drives, developed the QIC-40,80 specs so they could offer standard drives to compete with the Accutrak family.

Colorado Memory designed a QIC-40,80 drive that mechanically snaps together using few fasteners. The design resulted in a reliable drive that the company could produce and sell at low prices. In fact, the company's aggressive pricing spurred competitors to find ways to further reduce drive prices and ultimately kick-started the industry.

Prices drop below $200

Both QIC-40,80 and Accutrak drives connect to the floppy-disk-drive controller in PCs, thus sparing users the added cost of a tape-drive-controller board. End users can buy Accutrak or QIC-40,80 drives for as little as $200 at discount houses now. Both drive types can store 250 Mbytes using data compression.

The low prices of floppy-interface minicartridge drives make the products almost a commodity item, like a floppy-disk drive. In fact, Bill Beierwaltes, Colorado Memory chairman, says that capacity-hungry phenomena such as Windows will make a tape drive necessary for every system. He predicts that manufacturers will drive the price down so low that system manufacturers will be able to include a tape drive in 80386 and faster systems. Dell Computer (Austin, TX) has already started including a tape drive as a standard feature in its high-end 80486 systems.

The floppy interface of QIC-40,80 and Accutrak drives is certainly partially responsible for the drives' low cost. The interface also makes the drives simple to install, but simplicity and low cost come at the expense of data-transfer rate and, therefore, backup performance. The importance of backup speed varies with users. Many users set backups to occur automatically at night and therefore consider speed unimportant.

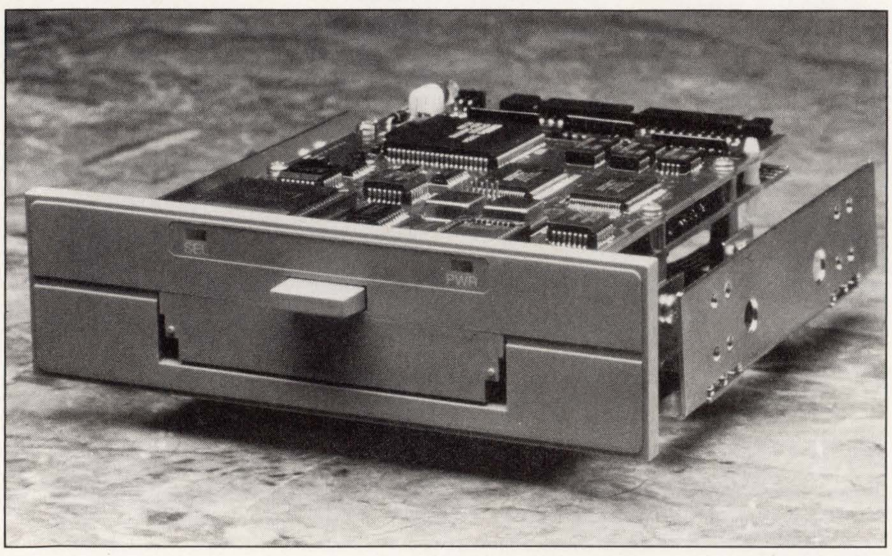
Floppy-disk interfaces operate at 31 to 62 kbytes/sec. Most manufacturers of floppy-interface drives offer accelerator boards that boost the data rate to 125 kbytes/sec, but users who buy the board lose an expansion slot and end up paying almost double for their tape drive.

IDE improves data rate

The QIC group added an option to its QIC-40,80 spec that enables manufacturers to offer drives that connect to the IDE (integrated device electronics) hard-disk interface found in many PCs. The IDE interface can operate several orders of magnitude faster than a floppy-disk-drive interface—in fact, much faster than any tape drive can operate.

IDE speeds sound appealing, but consider two facts before buying an IDE tape drive or designing one into a new system. First, the IDE interface supports only two drives, so a system with one hard disk and one IDE tape drive will require another controller board for future disk expansion. Second, the IDE interface is single threaded. A system can't operate the disk and tape drive concurrently, which limits the true data throughput.

So far, Summit Memory Systems is the only company offering an IDE-interface tape drive. The company's SE305 drive costs $449 and has a 125-kbyte/sec transfer rate—the same speed floppy-interface drives with accelerator boards achieve. Company benchmarks suggest that 386- and 486-based sys-



The 567-kbyte/sec data-transfer rate of the Everex Excel 1G suits the 566-Mbyte drive for high-end-PC and workstation applications.

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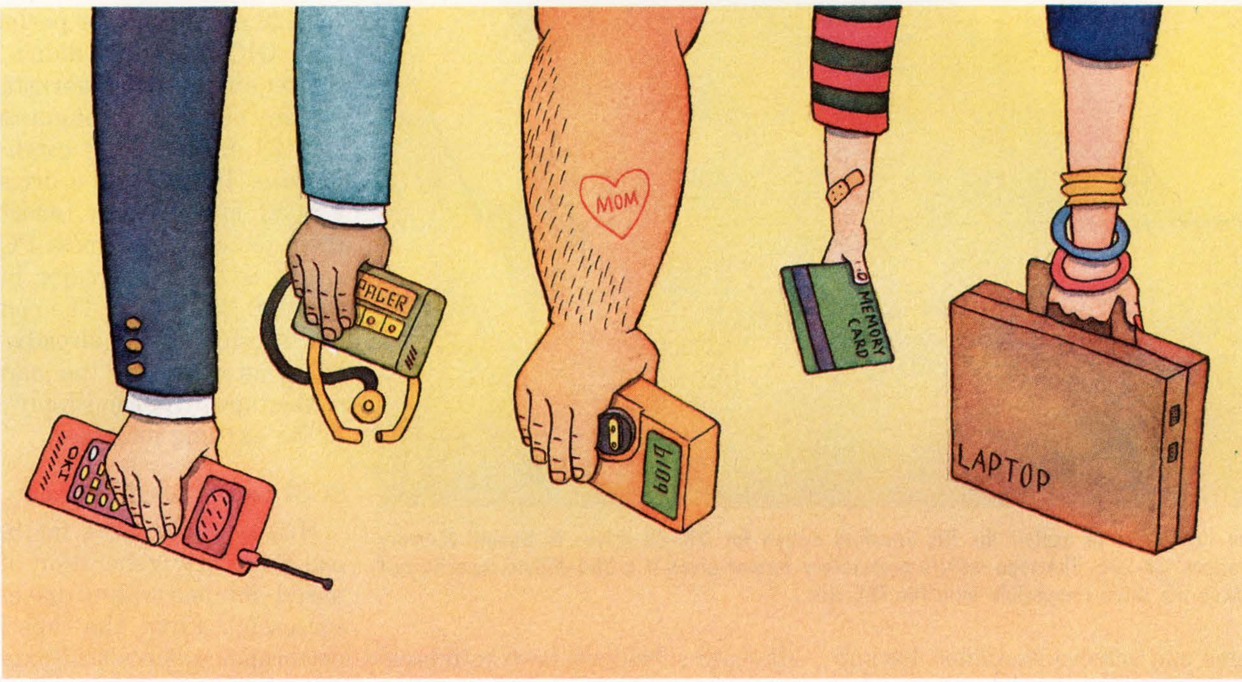

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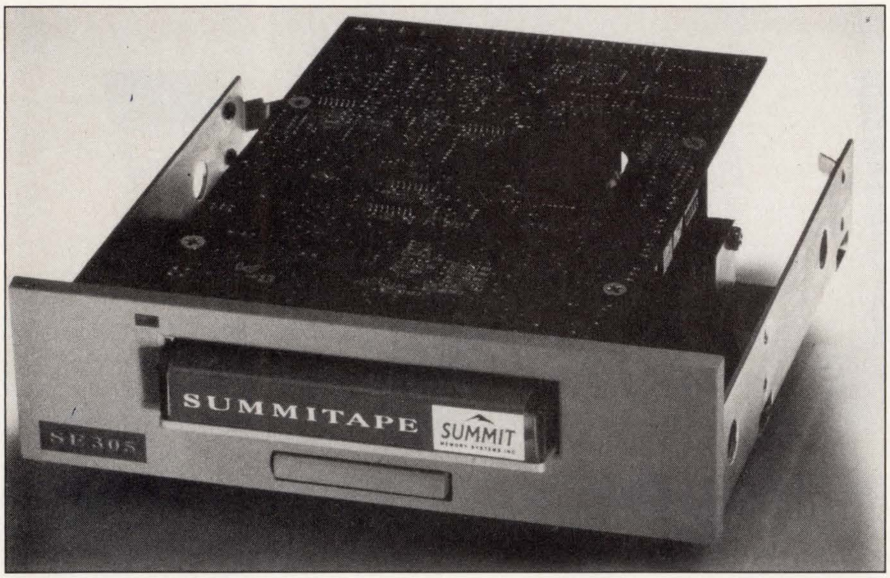
MINICARTRIDGE TAPE DRIVES



The first drive to exploit the IDE-interface option for QIC-80 drives is Summit Memory Systems' SE 305. The tape drive's proprietary format gives it a 305-Mbyte capacity and makes the drive compatible with the QIC spec.

tems can achieve sustained backup rates as fast as 166 kbytes/sec due to the drive's 64-kbyte buffer. The drive's IDE interface can handle burst transfers as fast as 5 Mbytes/sec. The drive can operate in standard QIC-80 mode or use a proprietary format to extend a minicartridge's capacity to 152 Mbytes—305 Mbytes using data compression.

Drives stand 1 in. high

Manufacturers of QIC-40,80 drives are trying to differentiate their products as sales take off. For example, Archive-Irwin's Superhornet drives and Iomega's Tape250 products stand 1-in. high; most other minicartridge drives are 1.6-in. high. The smaller tape drives exactly fit the profile of 1-in.-high floppy-disk drives. The low-profile units will make designing a tape drive into small desktop systems easier. Iomega also differentiates its Tape250 drive by making it read-compatible with Archive-Irwin's Accutrak drives.

Manufacturers also differentiate their products by the way the drive connects to a computer. For example, Colorado Memory and Archive's Maynard subsidiary have both packaged QIC-80 floppy-interface drives in external cases. An interface board lets users connect the external drives to a parallel port. The parallel-port interface reduces data-transfer rates but lets users back up notebook computers and easily move the drives between systems.

Later this fall, expect the announcement of a 500-Mbyte class of floppy-interface minicartridge drives. The QIC group has already published the QIC-500M spec, which defines such drives, and the products' storage capacity will exceed 1 Gbyte when using data compression. Colorado Memory should be the first to introduce a 500-Mbyte drive. Given the company's history of low-cost drives, expect the 500-Mbyte drive to cost less than $200 more than QIC-80 drives.

While floppy-interface drives for PCs continue to prosper, minicartridge-drive manufacturers have also been busy developing higher-performance products for workstations and midrange business systems. At about the same time the QIC group specified QIC-40, it also defined the 40-Mbyte QIC-100 spec. The group later followed up with the 128-Mbyte QIC-128 spec. QIC-100,128 offered better performance than QIC-40,80 but didn't satisfy the requirements of workstations.

Many observers thought the QIC-100,128 drives would catch on for PC use. However, the drives need a SCSI host adapter, which made them too costly for most PC users. Apple is the only major buyer of QIC-100,128 drives. The company's Macintosh systems already have a SCSI interface for the hard disk, so the tape drive can simply connect to the existing interface.

SCSI boosts performance

However, several factors will make the new generation of SCSI-based minicartridge drives more successful. First, the capacity and performance specs will extend the drives' application range far beyond PCs. Second, SCSI will finally become a standard interface in high-end PCs, even if the interface doesn't connect to the hard-disk drive. SCSI will come to the PC mother board because of the demand for CD-ROM and other optical drives and because SCSI offers a high-speed interface for printers and scanners. Finally, SCSI is the interface of choice in workstations and midrange business systems.

Teac started the parade of new SCSI-based products when it announced the 155-Mbyte Micro Streamer last year, which was also the industry's first 1-in.-high minicartridge tape drive. Mike Helsel, Teac manager of tape and optical products, predicts that the 1-in.-high form factor will quickly become the size of choice for minicartridge drives in PCs and workstations. Lately, the company has backed the new QIC-410M spec and figures to be the first company to announce one of the 410-Mbyte drives having a data-transfer rate of 300 kbytes/sec.

Archive Technology has an-

MINICARTRIDGE TAPE DRIVES

nounced a 450-Mbyte SCSI-based drive whose format is an extension of the Archive-Irwin Accutrak format. In fact, the Adder drive can read tapes recorded on both Accutrak and QIC-40,80 drives. Everex has broken the 500-Mbyte level with its Excel 1G drive. The 566-Mbyte unit uses a proprietary format and has a data-transfer rate of 567 kbytes/sec.

The announced SCSI-based products along with the QIC-875M 875-Mbyte drives expected next year have the performance and capacity to compete at the low end of the DC-600, DAT, and 8-mm tape markets. Remember that data compression can double the capacity of all minicartridge drives. And the emerging minicartridge drives actually offer better performance than DAT drives do.

Also, cost should again ensure the success of the SCSI-based minicartridge product class. The new high-capacity drives share many mechanical features with the high-volume, low-cost, floppy-interface drives. The manufacturers well understand the minicartridge drive manufacturing requirements. Therefore, expect newly introduced 1-Gbyte-class minicartridge drives to sell for substantially less than DAT drives.

Lack of standards could yet stymie the success of minicartridge drives, however. The format diversity never mattered in the PC market, but workstation and enterprise-level business users will want to buy multisourced tape products that offer compatible formats and therefore data interchange. Whether led by the QIC group or a de facto standard, the industry needs a single upgradable technology path to follow.

Road map passes 3 Gbytes

The QIC group has defined an upgrade path that extends the QIC-875M technology to a 3-Gbyte drive that could be available as early as 1994. Privately, some minicartridge manufacturers claim they could develop a 10-Gbyte cartridge in the same time frame.

And depending on your viewpoint, a completely new type of minicartridge drive could either fuel your enthusiasm for the product class or dilute your interest in a product class already full of diversity. Conner Peripherals (San Jose, CA), a leader in the disk-drive business, announced this past summer that it plans to enter the tape-drive business. The company plans to develop a multigigabyte minicartridge tape drive using technology that it obtained through a licensing agreement with 3M (Minneapolis, MN)—the inventor and leading supplier of data cartridges and minicartridges.

Conner and 3M disclosed little about the technology when they announced the licensing deal. However, Bob Abraham, vice president of Santa Barbara, CA, market-research firm Freeman Associates, speculates that the drive will use a recording technology significantly different from the longitudinal recording QIC drives use and the helical-scan recording DAT and 8-mm-tape drives use.

Conner and 3M refuse to reveal more details, but industry gossip suggests that Conner may make a Fall Comdex product announcement this November. The whispers also indicate that the drive could carry a low price and have a storage capacity as high as 3 Gbytes, which would be an immediate, serious challenge to DAT drives. EDN

Article Interest Quotient
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For more information . . .

For more information on the tape-drive products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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Colorado Memory Systems Inc
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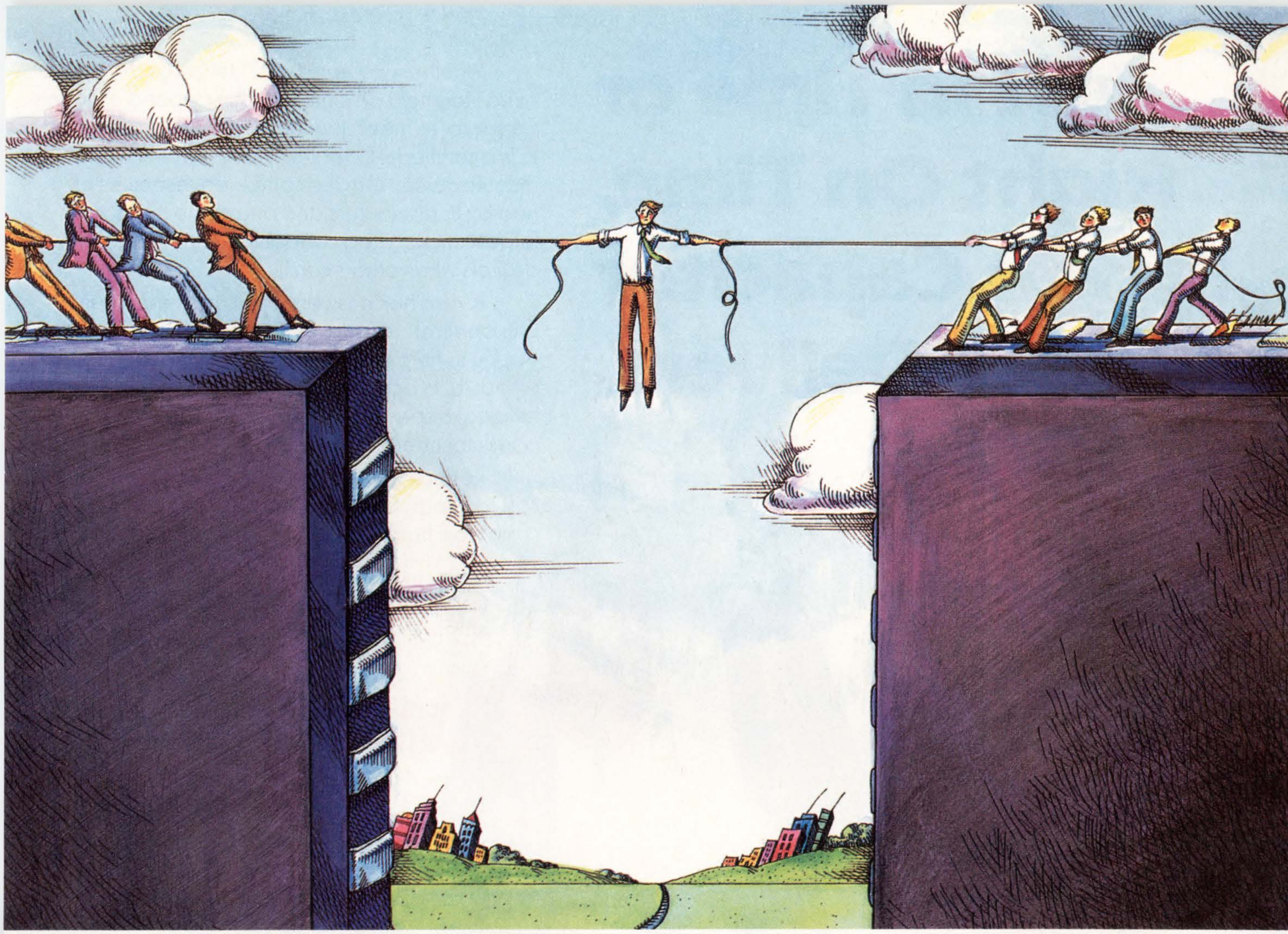

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CIRCLE NO. 58

Logic analyzers offer many tools and perform 1-GHz timing analysis

Tektronix likens today's system developers to a kid in a candy store who wants eight candy bars but can afford just one. With bus speeds on the fastest μPs well over 50 MHz, developers need faster logic-analysis tools, and they need many other tools as well. The problem is that their budgets barely allow the purchase of a logic analyzer. Moreover, if these developers had to pay last year's prices, the analyzer they could buy wouldn't meet this year's needs.

Enter the GPX series, a family of high-speed analyzers that perform functions that previously required multiple instruments. These units cost no more than lower-performance, single-function instruments with the same number of channels cost earlier this year.

From the outside, the GPX units look like members of the Prism family that the vendor introduced in 1989, and, indeed, Prism owners can upgrade their units. The analyzers have two package configurations: One is a portable benchtop version with an integral 9-in. monochrome CRT; the other is an enclosure that resembles the system unit of a desktop PC. With the second package, you choose either a high-resolution color CRT or a flat-panel electroluminescent monochrome display. Picking the flat display results in a portable system. To either package, you can add an expansion housing that looks almost identical to the "PC" package. The benchtop unit has 80 channels, the "PC" holds 160, and the expansion housing holds 160 more.

All channels can perform 200-MHz transitional timing analysis and 80-MHz state analysis. When the timing-analysis speed is 100 MHz or less, any channel can do both state and timing analysis simultaneously through a single probe. In this mode, each channel provides 8 kbits of memory. The units will perform 1-GHz timing analysis if you reduce the channel count by a factor of five. In this mode, each channel has 40 kbits of memory.

The analyzer's probing system is new; the probes are passive hybrid circuits that plug onto pins spaced as closely as 0.1×0.1 in. in a grid pattern on your target board. The vendor supplies adapters that accept specific μPs. These adapters plug into target boards in place of the μP and let you neatly plug in the probes. At present, the units accommodate 17 μPs from four IC vendors; support for more μPs is on the way.

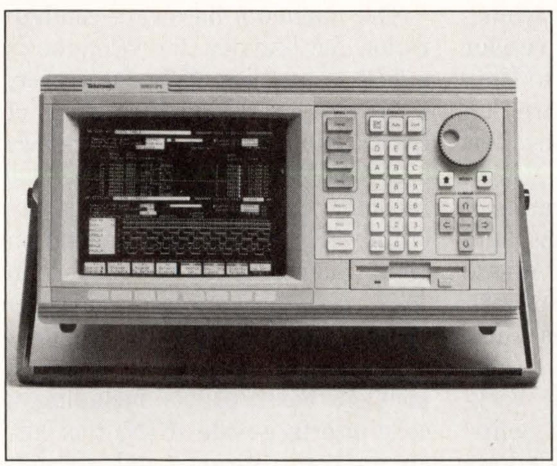
Besides state and timing analysis, the analyzers let you add real-time performance analysis and ROM emulation. According to the vendor, some competitive instruments' so-called real-time performance-analysis functions operate in real time only for the first sample. Because performance analysis is meaningful only when you acquire data for an extended period, an analyzer that can't present data at the time of acquisition is likely to mislead you.

The 3001 GPX—the 80-channel benchtop version, which includes a 3½-in. MS-DOS-compatible floppy-disk drive—costs $8995. A 40-Mbyte hard disk and a QWERTY keyboard with a knob and keypad are optional. The 3002 GPX—the "PC" version—costs $13,995, with 80 channels and your choice of display. In this model, the keyboard and both the floppy- and hard-disk drives are standard. The expansion housing costs $2000, and 80-channel expansion modules cost $7995. Delivery is six weeks ARO. For the large number of troubleshooters who use a logic analyzer with a scope, the vendor recommends the TDS 520 DSO, which stacks nicely atop the 3001 GPX. You can buy both products for $16,500.

—Dan Strassberg

Tektronix Inc, Test and Measurement Group, Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200.

Circle No. 731



A look at its front panel leaves the impression that the Tektronix 3001 GPX is a full-featured logic analyzer. What is not obvious is the number of functions the unit can perform, its high level of performance, or that it does 80-MHz state and 100-MHz timing analysis simultaneously on all channels through one set of probes.

Virtual-instrument ware migrates to MS-Windows

Since 1986, National Instruments' Labview virtual-instrument software has captivated engineers and scientists who use Apple Macintosh PCs to control the acquisition of data from laboratory instruments and to process and display that data. Using Labview, instead of writing conventional, text-based programs, you connect and manipulate icons on the PC's screen.

Although National Instruments has for years offered a data-acquisition package called Labwindows, which offers a text-based interface for MS-DOS PCs, a large user group of those PCs and of Unix workstations has continued to ask when Labview's simple, intuitive, icon-based interface would be available to them. The answer, finally, is right now.

The colorful, intuitive, icon-based interface of National Instruments' Labview, a mainstay for data acquisition and analysis on Apple Macintosh PCs since 1986, is now available to users of well-equipped PCs running MS-Windows 3.1 and MS-DOS 5.0, as well as to users of Sun SPARCstations.

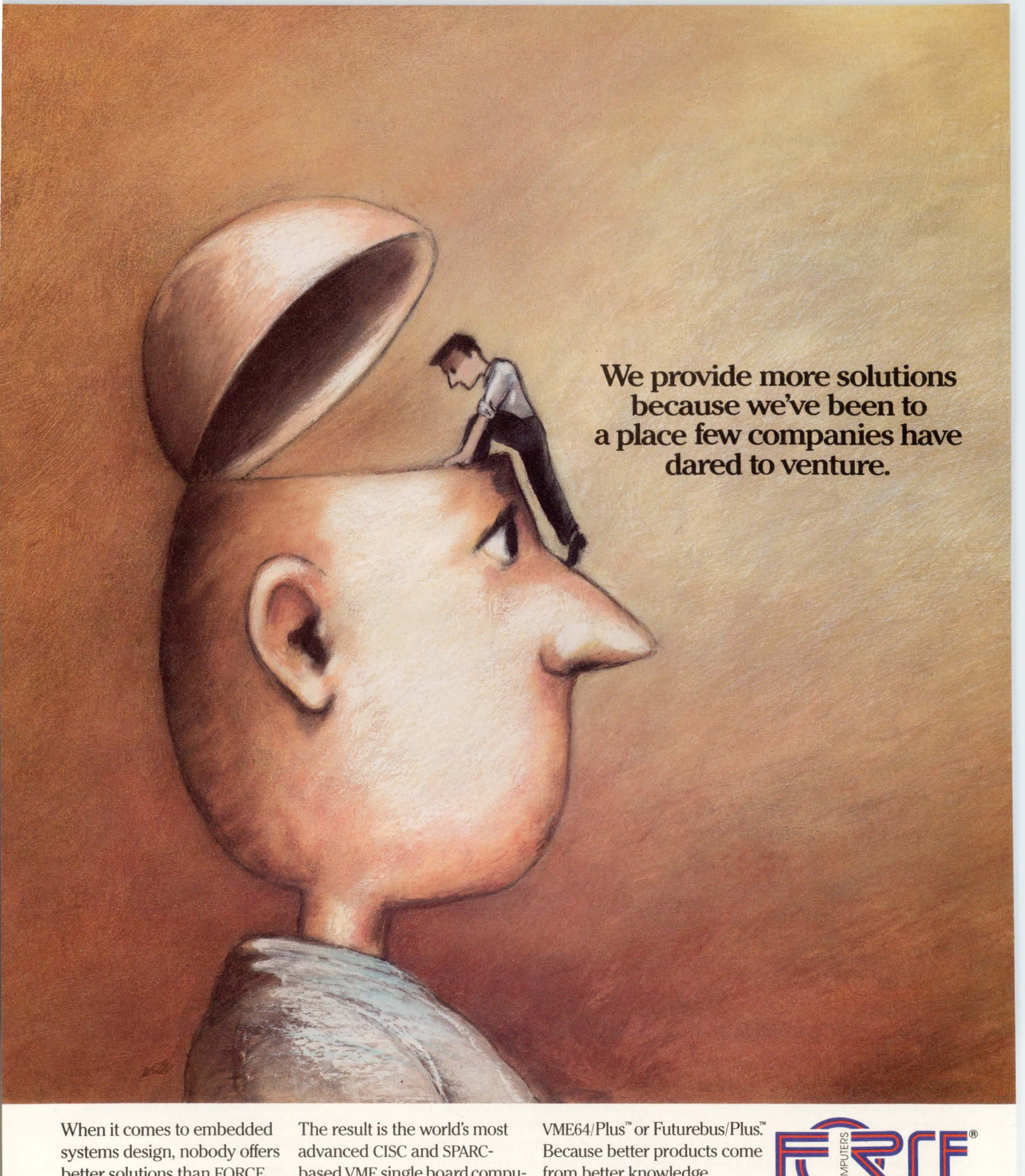
It was the advent of MS-Windows V3.1, with its graphical interface and management of extended memory that made possible the Windows version of Labview. Also required was a herculean effort by National Instruments' programmers to rewrite Labview's internal code, creating a core version not specific to a particular computer or operating system. With a machine-independent version, the vendor could also port the package to Unix systems. The first of these are Sun Microsystems SPARCstations that run under SunOS.

Both versions include libraries of ready-to-use controls, graphs, and strip charts you can use to create custom virtual-instrument panels. In addition, driver libraries allow you to connect more than 100 instruments to the host PC or workstation via National Instruments' interface hardware. The Windows version also works with the vendor's IEEE-488 DSP and data-acquisition boards. Because the analysis libraries make use of the DSP boards when they are present, the result is a powerful, DSP-based data-acquisition and analysis system with a virtual-instrument interface. Users of Labview for the Macintosh should feel right at home with the new packages because the functions and user interface are nearly identical.

The minimum hardware configuration for Labview for Windows is a '386 PC with a '387 coprocessor, 8 Mbytes of RAM, 10 Mbytes of free hard-disk space, MS-Windows 3.1, and MS-DOS 5.0. The vendor recommends a super-VGA display (1024×768 pixels recommended on 19-in. monitors; 800×600 pixels on 14-in. monitors) and a graphics accelerator compatible with Windows 3.1. The full Labview for Windows package costs \$1995, including a code-interface-node (CIN) tool kit, an analysis library, and virtual-instrument libraries for data-acquisition and DSP boards, IEEE-488 instruments, and RS-232C instruments. A version lacking the analysis library and CIN tool kit costs \$995. A virtual-instrument library for VXI modules sells separately for \$495.

Labview for Sun, which costs \$3995, requires a SPARCstation with 24 Mbytes of main memory, 10 Mbytes of disk space for the application and associated files, 32 Mbytes of disk swap space, and MIT's X-Window system V11, release 4 or 5, or Open Windows V3. Motif or Open Look are not required. This package includes a CIN tool kit, a library for VXI modules, and equivalents of all libraries in the full Windows package, except the one for ISA bus data-acquisition boards.—**Dan Strassberg**

National Instruments Corp, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. TLX 756737. **Circle No. 730**



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CIRCLE NO. 60

EDITORS' CHOICE EDN

Hitachi H8/338 μC crams 48-kbyte EPROM/ROM and 2-kbyte RAM into one IC

On-chip memory is always in short supply for embedded microcontrollers (μCs). Hitachi's H8/338 is a move in the right direction; it crams 48 kbytes of program memory, ROM, or EPROM into a single chip along with 2 kbytes of data RAM. This combination gives designers enough space for complex applications—including C applications—that require more program and data memory.

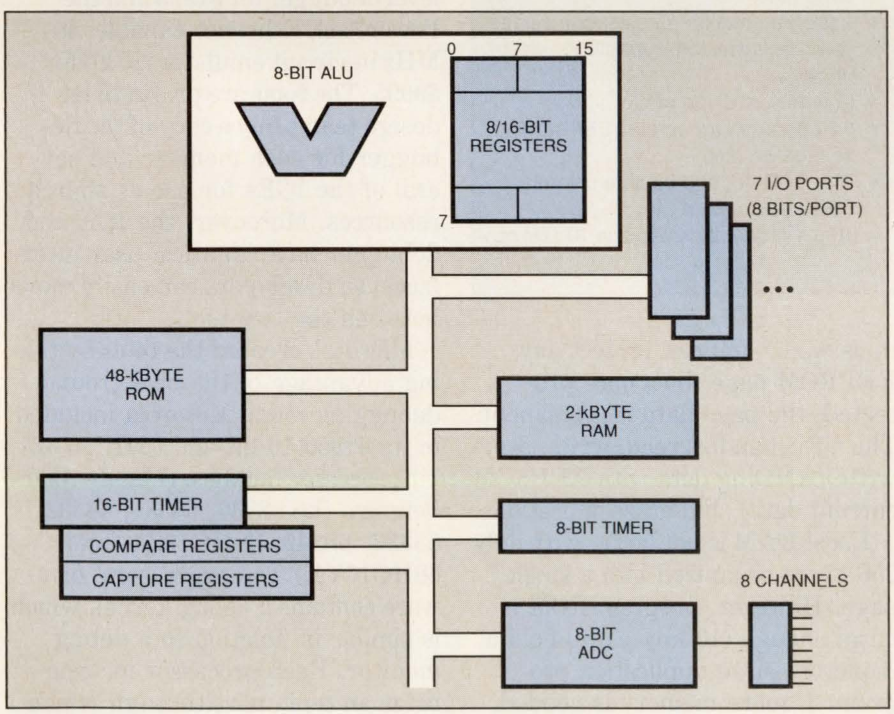
The H8/300 architecture is hard to classify. The instruction and data paths are 16 bits wide, and the adder is 8 bits wide. Registers are addressed and manipulated as either 8 or 16 bits. Many engineers classify the H8/300 as an 8/16-bit μC.

The 16-bit registers make it easy to handle 16-bit values, especially pointers and addresses, which is a major difficulty with most 8-bit devices. And, the 16-bit instruction path speeds instruction processing. Instructions are two or four bytes long, so some instructions will take two word accesses, slowing execution. Execution from external memory is slower, because the CPU has an 8-bit data path.

A second-generation μC, the H8/300 series is built around an 8-bit ALU with a set of 16 8-bit registers. These registers can alternatively be treated as eight 16-bit registers. Like a RISC (reduced-instruction-set-computer) processor, the H8/300 is a load/store architecture: All data-manipulation operations are register to register. The μCs have a single 64-kbyte address space that includes both code and data. The CPU has a simple instruction set with 57 basic operations and eight addressing modes. These modes include register-indirect and register-indirect-with-postincrement and -preincrement options, which save code.

Hitachi H8/338

- 10-MHz clock, 5 MHz for 3V operation
- 57 instruction types; load/store architecture
- R-to-R add; NOP (not operational)=200 nsec; 8-bit MPY/DIV=1.4 μsec
- 8 16-bit or 16 8-bit registers
- 16-bit data path, instruction path; 8-bit ALU
- 48 kbytes of EPROM/ROM/OTP
- 2-kbyte RAM
- 64-kbyte address space
- 3 power-down modes: sleep, hardware standby, and software standby
- 8 channels; 8-bit A/D and D/C converters
- Interrupts: 9 external, 22 internal
- 55 I/O pins, 8 input-only pins
- In 84-pin PLCCs; 80-pin QFPs
- $26.75 (100)



Hitachi's H8/338 integrates an 8-bit ALU with a set of 8/16-bit general-purpose registers and 48 kbytes of program ROM and 2 kbytes of RAM.

The H8/33x is well set up for I/O: It has 63 I/O pins and nine external interrupts. In addition, the μC's peripherals include A/D and D/A converters, three timers (one is a 16-bit general-purpose timer with compare and capture functions), and two serial I/O ports.

Hitachi is also adding more members to the H8/300 family. The H8/329, 328, 327, 326 use 8, 16, 24, or 32 kbytes of on-chip ROM with 256-byte to 1-kbyte RAM. They run at 6, 8, and 10 MHz at 5V and can run up to 5 MHz with 3V operation. Zero-turnaround-time (ZTAT) and one-time-programmable (OTP) versions are available for prototyping. The chips come in 64-pin DIPs and quad flatpacks. On-chip peripherals include an 8-channel, 8-bit A/D converter, a 16-bit free-running timer with two input-compare and four output-capture registers, an 8-bit timer, and a 2-Mbps serial I/O channel. As many as four processors can team up on a serial line.

These additional μCs have 22 interrupt sources (four external) and

48 general-purpose I/O lines, with eight input-only lines, as well. Prices for 5V H8/329s (32-kbyte OTP version) or H8/327s (24-kbyte OTP version) are $18.25 and $15.75, respectively (100).

Hitachi is introducing an ICE for the H8/300 series. The E3000 supports all H8/300 μCs, including 10-MHz operation. A 6×8.5×2-in. box, the ICE includes 64 kbytes of emulation memory. It features four complex breakpoints with up to 64 pass counts. It has a 2k×54-bit trace buffer. The ICE links to a PC development host with one of three interfaces: a command line, Microtek Research Inc's Xray debugger, or a Windows 3.0 graphical interface. The ICE costs $5000.

—Ray Weiss

Hitachi America Ltd, Semiconductor and IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (800) 245-1601, ext 21; (415) 589-8300. **Circle No. 732**

H8/3101 smart-card μC provides 8-kbyte EEPROM nonvolatile memory

Many embedded applications require more than volatile RAM or fixed ROM/EPROM program memory. These applications demand dynamic, but nonvolatile, memory to hold critical data such as encryption or security keys, identifiers, and complex sets of passwords. Hitachi's H8/3101 offers the best of both worlds: 10 kbytes of program ROM and 8 kbytes of modifiable, nonvolatile EEPROM memory with built-in security. Fit in a 10-pin package, this microcontroller (μC) has enough program and RAM memory to support complex encryption algorithms.

The H8/3101 μC's EEPROM furnishes a nonvolatile mechanism for dynamic storage of key data. Using this chip, designers can tackle embedded applications that require encryption, changeable codes, or secure embedded storage with a single-chip μC. Board and program design are simplified because off-chip nonvolatile storage is not required. EEPROM data is protected with a special security feature.

Organized in 256 pages of 32 bytes each, the EEPROM is written to from RAM. An EEPROM instruction moves a block of 1 to 32 bytes from RAM to EEPROM. (Write and erase protection is built in as well.) You can protect any EEPROM page, but, once protected, the page data is permanent. The CPU handles read, write, overwrite (ANDing data with EEPROM current data), and erase operations.

Hitachi H8/3101 smart-card μC

- See previous processor update for description of general H8/338 architecture
- 10-MHz clock (5-MHz internal)
- 8-kbyte EEPROM organized into 256 32-byte pages; written as a block of 1 to 32 bytes; programmable erase/write protection per page
- 10-kbyte program ROM
- 256 bytes of data RAM
- 5V operation; on-chip charge pump generates EEPROM erase/write voltage
- 10-year EEPROM data-retention time; 10^4-page rewrite cycles; 15-msec rewrite time
- 2 programmable I/O pins; one serves as an external interrupt pin for sleep mode
- Low-power sleep mode
- 5V operation (generates EEPROM voltage on chip)
- Die, SOP-10, and custom chip-on-board packaging
- 10-pin small-outline package, $7 (1M qty)

Local RAM is not large, with only 256 bytes organized into a single page. However, program ROM is large enough (10 kbytes) to hold a moderate-sized application program. If more memory is needed, the chip has off-chip memory for both data or code (the CPU has a single address space, addressing up to 1 Mbyte of off-chip memory). A multiplexed external bus presents a 16-bit address and an 8-bit data path.

The H8/3101 operates on 5V. The higher voltage needed for EEPROM writes is generated on the chip, simplifying chip power requirements.

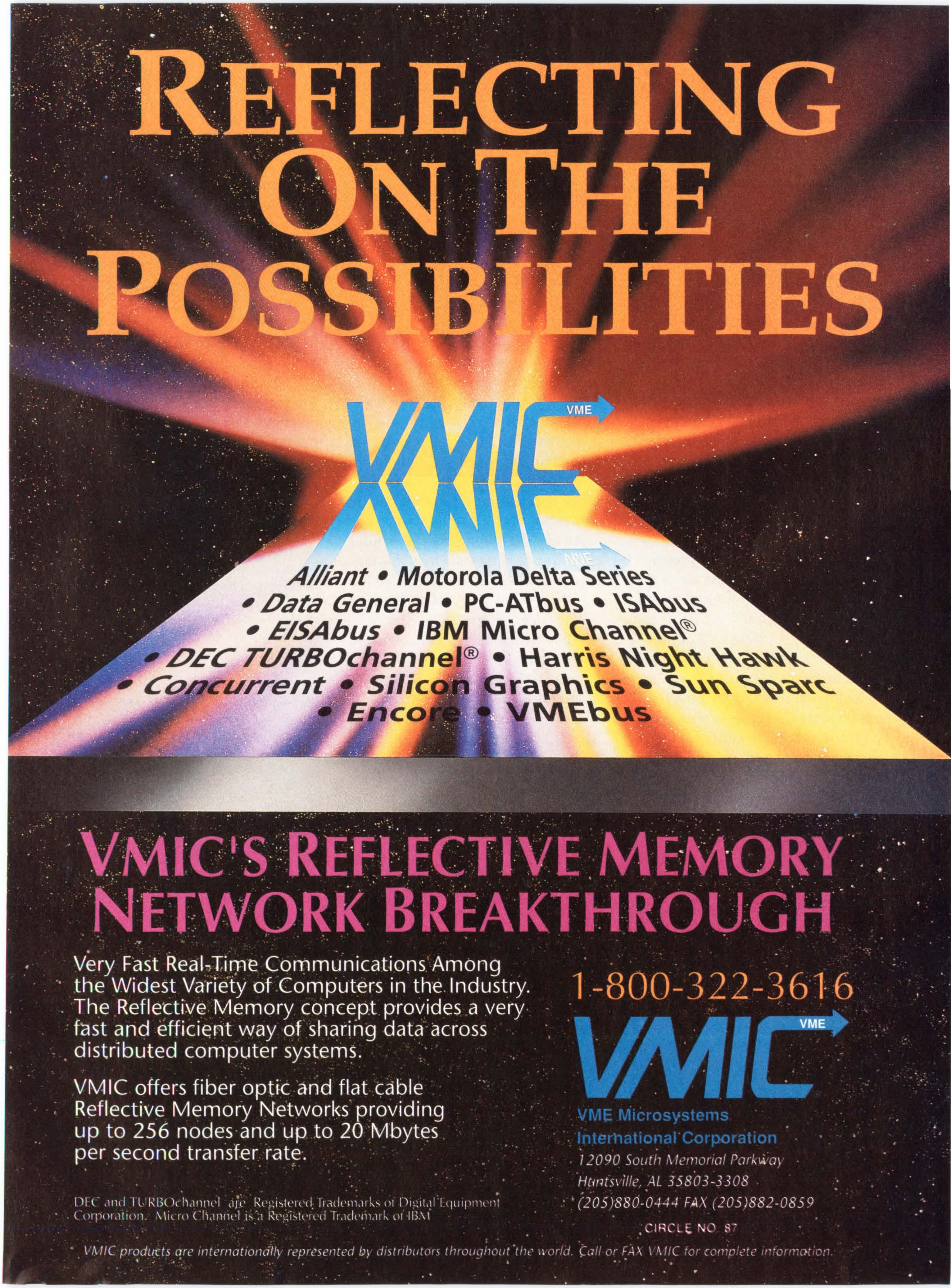
—Ray Weiss

Hitachi America Ltd, IC & Semiconductor Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (800) 245-1601, ext 21; (415) 589-8300. **Circle No. 733**

$9995 ICE handles Motorola 16- and 32-bit μPs

As embedded-system design teams add more members and the majority of the work shifts to software development, the cost per development seat continues to increase. Responding to this trend, Microtek has introduced the Powerscope MS-Windows-based source-level debugger for $1995 and the PowerPack Ethernet-capable, 40-MHz in-circuit emulator (ICE) for $9995. The tools are priced to let design teams buy a copy of the debugger for each member and several of the ICEs for use as shared resources. Moreover, the ICE and debugger have identical user interfaces, so developers can easily move between the two tools.

Microtek created the tools by taking advantage of the background debugging mode Motorola included in its 68300 16-bit and 68HC16 32-bit processor families. (Family members are the 68330, 68331, 68332, 68333, 68340, 68HC16Z1, and 68HC16Y1.) The processors' firmware contains a debug kernel, which is similar in function to a debug monitor. Each processor incorporates an 8-pin port through which you can access internal nodes for debugging.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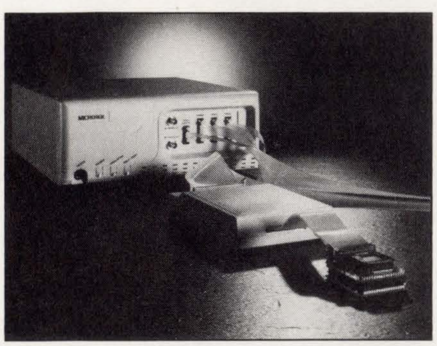
Because of the debug port, the debugger or ICE can operate transparently without usurping an interrupt line to gain control of the processor. In addition, communicating with the target does not usurp an RS-232C port, so you don't need to create RS-232C device drivers for debugging applications that use the port. The presence of the kernel on the µP chip also eliminates the need for creating ROMs that contain debugger code linked to your application code.

The emulator has 256 kbytes of overlay memory (1 Mbyte optional) and 128k frames of trace memory (256k frames optional). Compared with industry norms, the emulator's standard trace memory is large. You can subdivide this memory into multiple trace buffers—for example, 256 512-frame buffers, each with the trigger point at its center.

The multiple buffers and the emulator's acquisition of trace data on clock cycles (rather than bus cycles) help you obtain a quick answer to debugging's toughest question: "Which code module wrote this incorrect data?" By separately qualifying the trigger conditions for traces saved in separate buffers, you can obtain data in a single run that, with other emulators, might require hundreds of runs.

Another notable feature of the ICE is its construction. Ever since the clock rates of embedded-system



Using ECL for communication between the pod and the chassis lets the Powerpack in-circuit emulator include an unusually long cable. The cable gives you much more flexibility in locating the chassis than you have with most emulators.

µPs passed 8 MHz, cable-length limitations have constrained the placement of the emulator chassis. These constraints have been a major annoyance to system developers. By using ECL to communicate between the pod and the emulator chassis, Microtek was able to make the Powerpack connecting cable several times as long as the cables on some competitive products. The long cable will also work with 40-MHz versions of the processors when they become available.

Rather than adapting third-party tools, Microtek created its software in house. The MS-Windows-based tools provide hypertext help and allow multitasking with other Windows applications. In addition, by controlling both the hardware and software development, the vendor can offer features such as linking traces to their associated C code.

—Dan Strassberg

Microtek International Inc, Development Systems Div, 3300 NW 211th Terrace, Hillsboro, OR 97124. Phone (800) 886-7333; (503) 645-7333. FAX (503) 629-8460.

Circle No. 734

IC builds real-time histogram and saves hardware

Image and contrast enhancement—recovering and enhancing hard-to-see or hard-to-use images—has always been a tough problem. Software solutions are time consuming, and dedicated-hardware solutions are expensive and complex. The Harris HSP48410 chip neatly reduces the problem to one that's easily handled by hardware. This single chip provides histogram-accumulate and histogram-equalization functions for applications such as medical imaging, scanners, vision systems, infrared image or signal analyzers, and target-recognition systems.

The HSP48410 acts as a histogrammer: It analyzes an image pixel by pixel and keeps an accumulated total, or "bin," for the occurrence of each pixel value across the gray scale (a 10-bit pixel can have 1024 different values). This histogram is built in on-chip RAM. The chip can generate a histogram equalization table from the histogram, which is then used to enhance the image. The equalization table indicates how to change each pixel value for a sharper, clearer image.

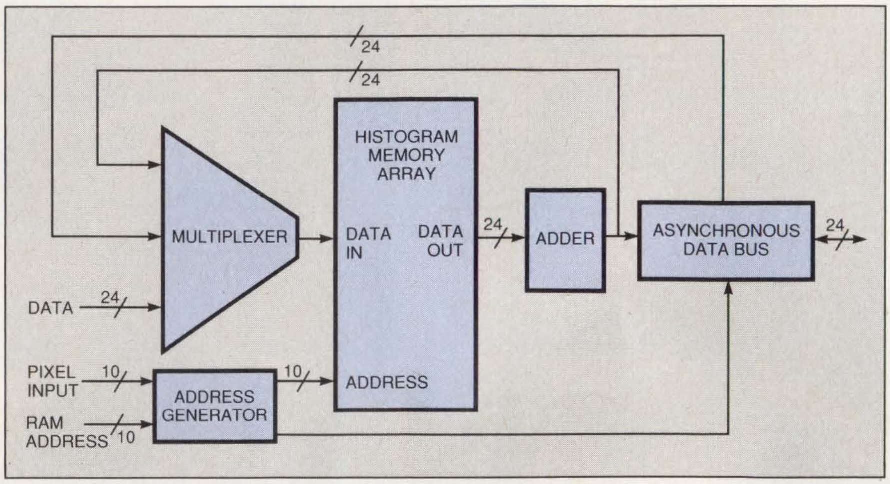
The chip maintains an accumulator in RAM for each discrete pixel or gray-scale value. Thus, after an image is run through the histogrammer, the accumulator supplies an accumulated total for each possible value over the whole range. For each image pixel with a value of say 0, the 0 accumulator increments by one. When the image is processed, the chip holds a histogram of the image that represents the cumulative intensities of the image pixels. To build a histogram, pixel image values stream into the HSP48410 on a 40-MHz system clock.

When done, the histogram can be converted to an equalization table. It uses a built-in algorithm that does integral-like summing on each pixel table value or "bin" by adding

Harris HSP48410 Histogrammer/Accumulator

- DC to 33- or 40-MHz clock
- 10-pixel resolution
- Builds histogram for image
- Converts histogram to equalization table
- Look-up-table mode reads out equalization table value for image enhancement
- Asynchronous host interface
- 1024×24-bit RAM (4k×4k image)
- Random access to RAM array
- 16- or 24-bit 3-state I/O bus
- Flash clear (single-cycle memory and internal data paths)
- 2.4W maximum power dissipation (70°C)
- 84-pin PGA; PLCC in development
- $52.01 (33-MHz version); $65.03 (40-MHz version) (1000)


BUSS



The Harris HSP48410 histogrammer/accumulating buffer IC builds histograms in real time in its 3-kbyte memory array for on-line image enhancement.

the data from the previous items (starting from 0) to each item. To build the new equalization table, the chip must be clocked 1024 times, once for each table item.

The equalization table now holds values that can be used to shift pixel gray values for an enhanced image. The surrounding hardware sends the chip a pixel value, and the chip returns the equalized value for enhancing the image. Two chips can do real-time adaptive equalization; one builds a histogram for the current image, and the other provides the equalization values to enhance the last image frame.

The chip is designed to be accessed asynchronously by a μP for easy interfacing and synchronous processing of data. It has a flash clear to reset the entire RAM array in a single clock cycle. The RAM array is loaded from the synchronous or asynchronous interfaces or from the on-chip adder.

In the Bin Accumulate mode, the item/bin value is added to the incoming data (DIN) value, instead of incrementing the bin by 1 as in the Histogram Accumulate mode. Thus, the bins increment by a constant, which can be varied. The Delay and Subtract mode is similar, except that the input value is subtracted from the item or bin value. The RAM can be accessed directly, as well as in synchronous 16- or 24-bit modes.—**Ray Weiss**

Harris Semiconductor, Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1040; (407) 727-9207.
Circle No. 735

Windows-based tool eases programming of μC family

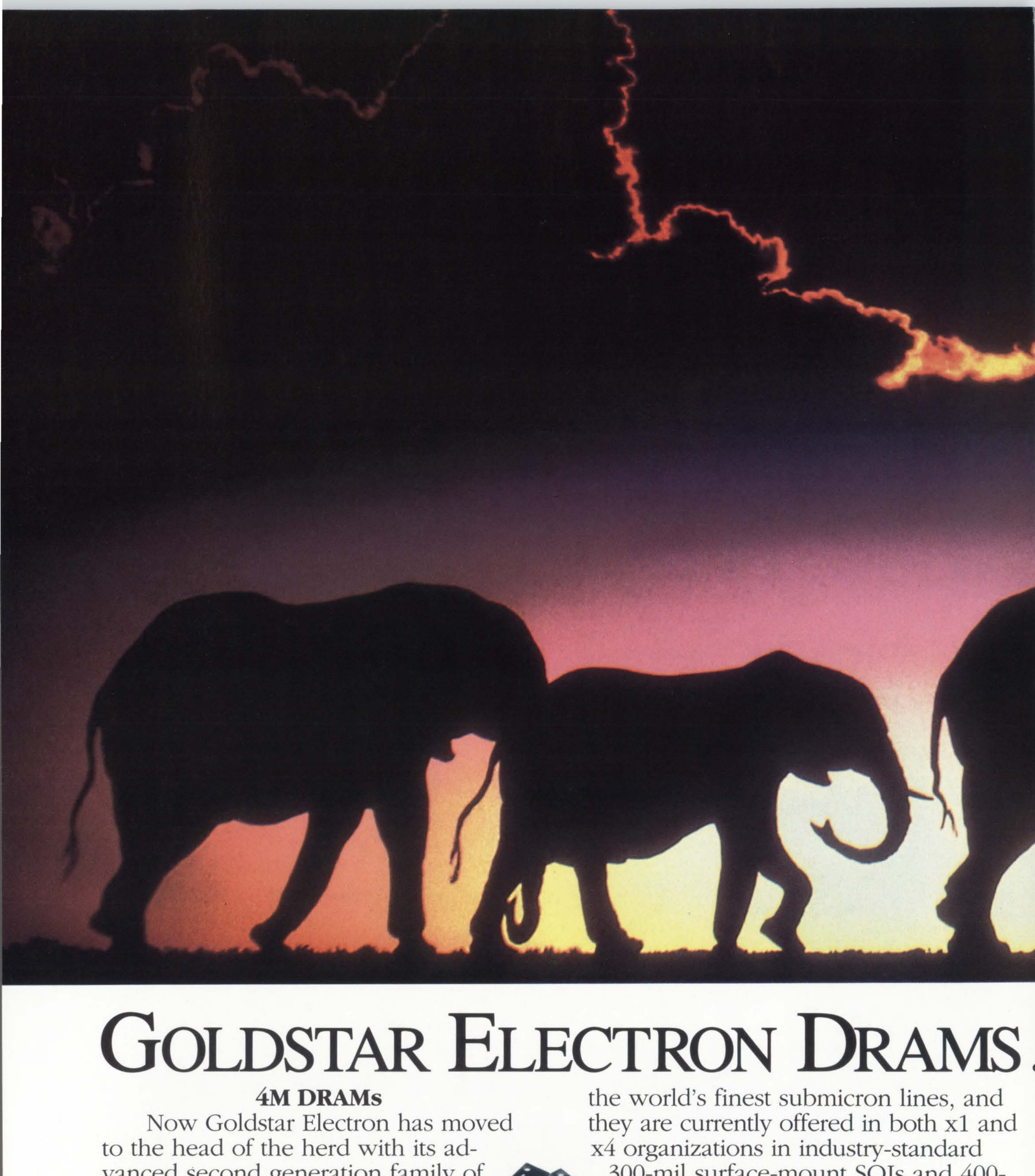
Intel's ApBuilder provides a graphical on-line reference and code-generation package for understanding and programming peripherals for the new 80C196 family of 16-bit microcontrollers (μCs). Running on Windows, the tool makes setting up and controlling peripherals easy. You can graphically define peripheral operations, and the software automatically generates assembly-language or C code. ApBuilder is free.

The Editors' Choice in EDN's April 23, 1992, issue (pg 107) dealt with the 80C186 family of μCs that are also used with ApBuilder.

—**Ray Weiss**

Intel Literature Center, Box 7641, Mt Prospect, IL 60056. Phone in US and Canada, (800) 468-8118; others, call local office. **Circle No. 736**

NOW WHO'S LEADING THE HERD IN DRAMs?



GOLDSTAR ELECTRON DRAMS.

4M DRAMs

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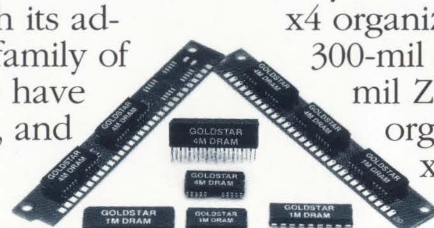

1M DRAMs

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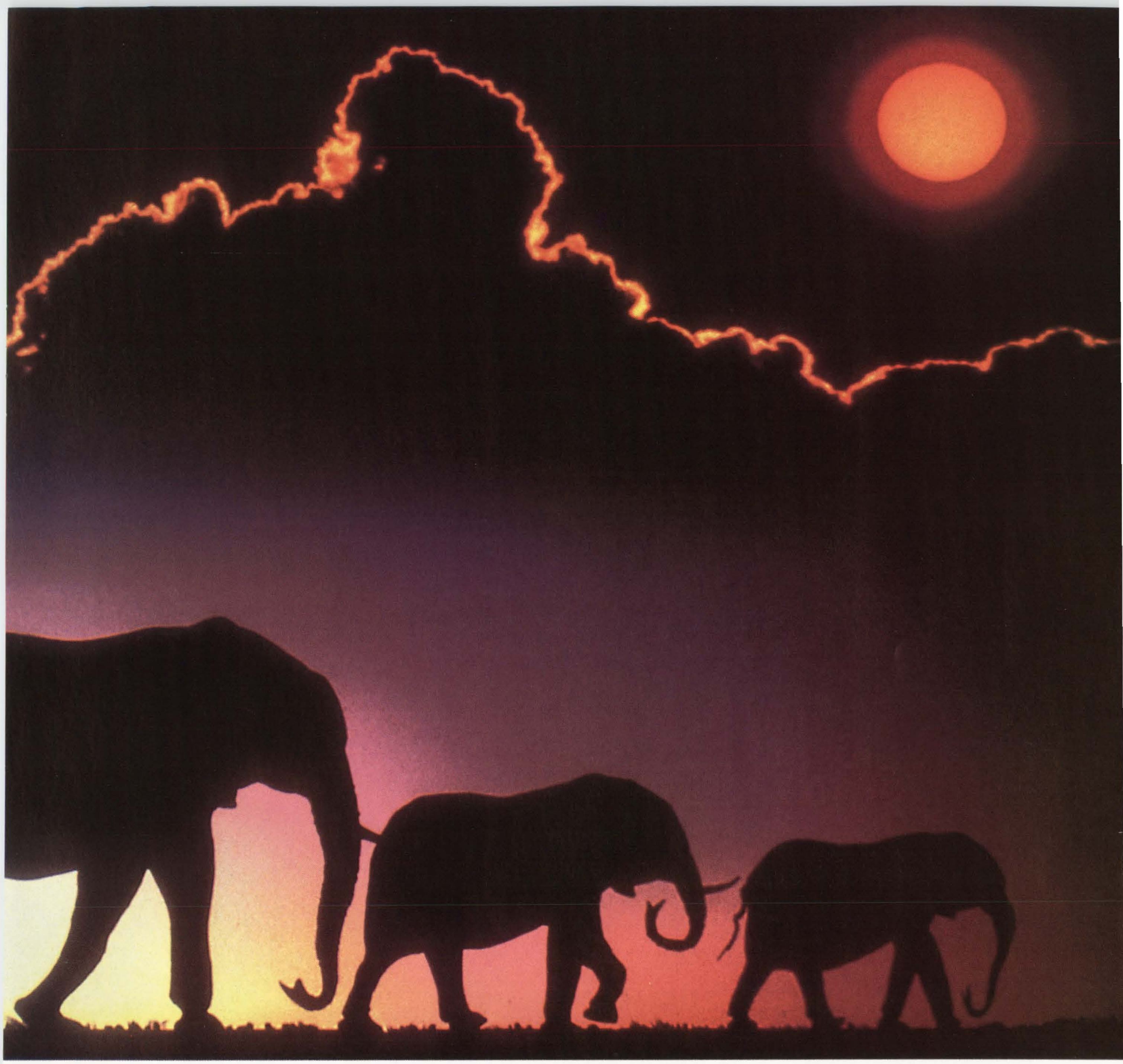

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THE GOLDSTAR DRAM FAMILY

CMOS DYNAMIC RAMs

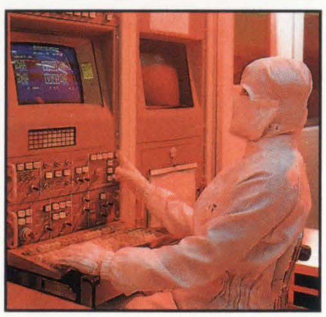
ORG.	PART NUMBER	ACCESS TIME (MAX) (ns)	CURRENT (mA) ACTIVE	S/B (L)	FEATURE	PACKAGE MIL
4M x 1	GM71C4100A/AL - 60 - 70 - 80	60 70 80	110 100 90	1 (0.2)	FAST PAGE MODE L-POWER	20 SOJ (300) 20 ZIP (400)
1M x 4	GM71C4400A/AL - 60 - 70 - 80	60 70 80	110 100 90	1 (0.2)	FAST PAGE MODE L-POWER	20 SOJ (300) 20 ZIP (400)
1M x 1	GM71C1000/L - 60 - 70 - 80	60 70 80	90 80 70	1 (0.2)	FAST PAGE MODE L-POWER	20 SOJ, 18 DIP (300) (300) 20 ZIP (400)
256K x 4	GM71C4256A/AL - 60 - 70 - 80	60 70 80	90 80 70	1 (0.2)	FAST PAGE MODE L-POWER	20 SOJ, 20 DIP (300) (300) 20 ZIP (400)
512K x 8	GM71C4800/L - 70 - 80	70 80	110 100	1 (0.2)	FAST PAGE MODE L-POWER	28 SOJ (400)
512K x 9	GM71C4900/L - 70 - 80	70 80	110 100	1 (0.2)	FAST PAGE MODE L-POWER	28 SOJ (400)
256K x 16	GM71C4260/L - 70 - 80	70 80	170 150	1 (0.2)	FAST PAGE MODE L-POWER	28 SOJ (400)

DRAM MODULES

ORG.	PART NUMBER	ACCESS TIME (MAX) (ns)	CURRENT (mA) ACTIVE	S/B	FEATURE	PACKAGE MIL
1M x 8	GMM781000NS - 60 - 70 - 80	60 70 80	220 200 180	2	FAST PAGE MODE	30 PIN SOCKET
1M x 9	GMM791000NS - 60 - 70 - 80	60 70 80	310 280 250	3	FAST PAGE MODE	30 PIN SOCKET
4M x 8	GMM784000S - 60 - 70 - 80	60 70 80	880 800 720	8	FAST PAGE MODE	30 PIN SOCKET
4M x 9	GMM794000S - 60 - 70 - 80	60 70 80	990 900 810	9	FAST PAGE MODE	30 PIN SOCKET
1M x 36	GMM7361000SG/SGS- 60 - 70 - 80	60 70 80	1240 1120 1000	12	FAST PAGE MODE	72 PIN SOCKET (DBL/SNG)
1M x 32	GMM7321000SG - 60 - 70 - 80	60 70 80	880 800 720	8	FAST PAGE MODE	72 PIN SOCKET
2M x 32	GMM7322000SG - 60 - 70 - 80	60 70 80	896 816 736	16	FAST PAGE MODE	72 PIN SOCKET
2M x 36	GMM7362000SG - 60 - 70 - 80	60 70 80	1264 1144 1024	24	FAST PAGE MODE	72 PIN SOCKET
1M x 40	GMM7401000SG - 60 - 70 - 80	60 70 80	1110 1000 950	10	FAST PAGE MODE	72 PIN SOCKET
2M x 40	GMM7402000SG - 60 - 70 - 80	60 70 80	2220 2000 1800	20	FAST PAGE MODE	72 PIN SOCKET

The combination of high performance with high density in Goldstar's 1M and 4M devices has been achieved by the use of submicron design rules, an advanced triple-poly, double-metal CMOS process technology, and the use of state-of-the-art manufacturing equipment and facilities. For complete products specs, send for data sheets.

A WORD ABOUT GOLDSTAR QUALITY



Goldstar's Quality Assurance System and Reliability Testing covers all phases of design and manufacturing. In the development stage, we *design* reliability into our products. During manufacturing, we *build* reliability into our products. And in the test stages, our quality assurance inspection *verifies* that the required quality and reliability have been achieved.

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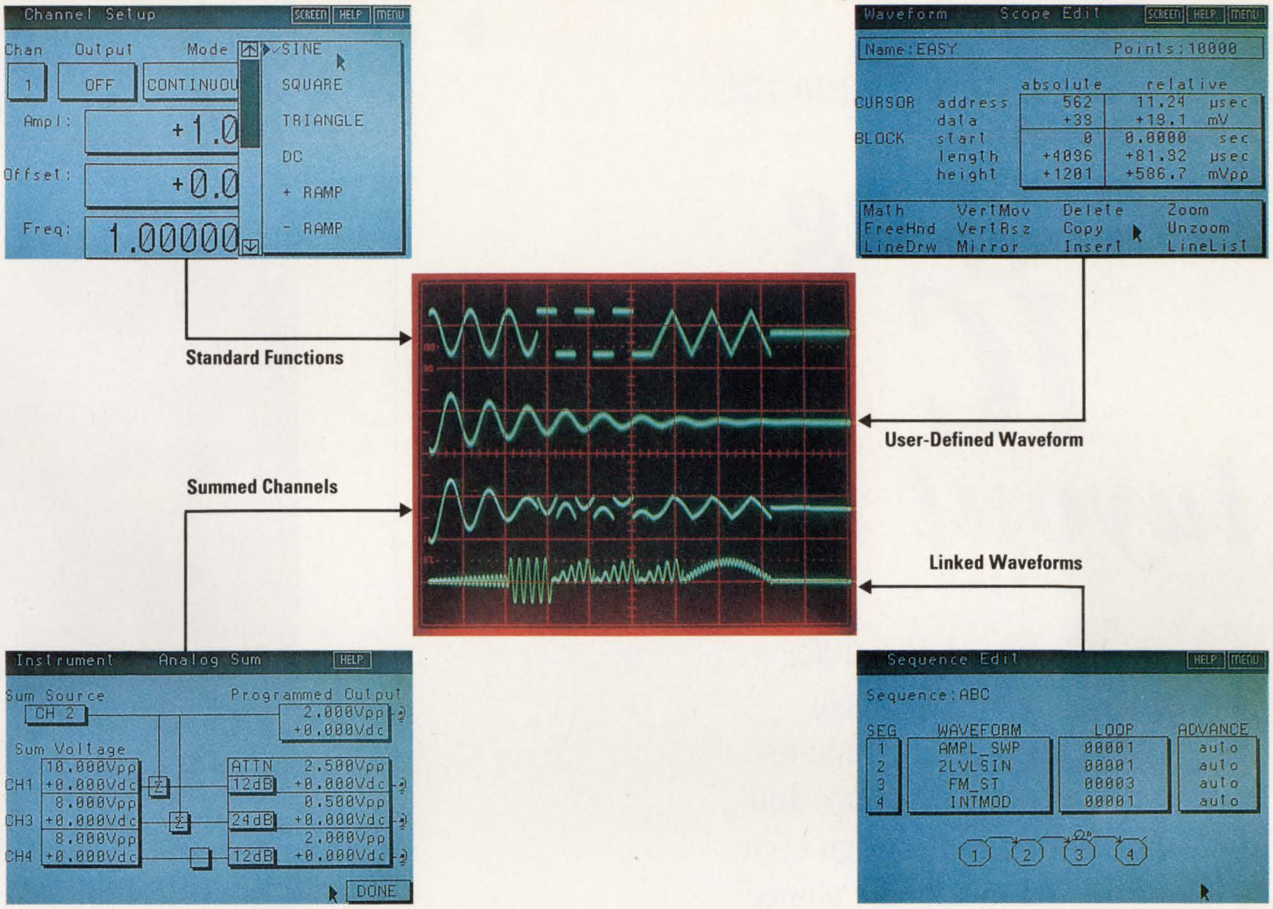

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Circle #111 Literature

Bringing IC layout in house

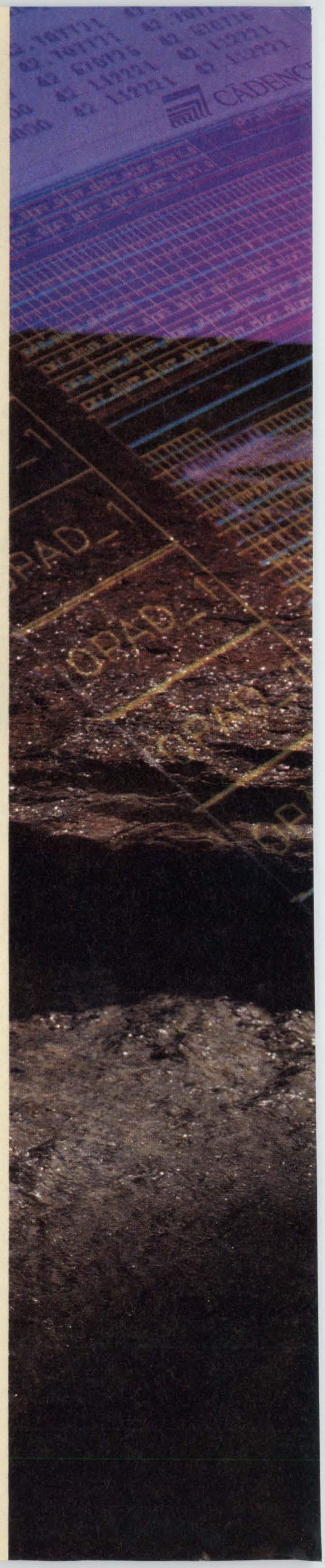
For large, high-speed digital ICs, physical layout can upset logic design goals, lengthening time-to-market. Doing your own place and route can shorten your design cycle. Is it time for you to take the plunge?

John C Napier, Technical Editor

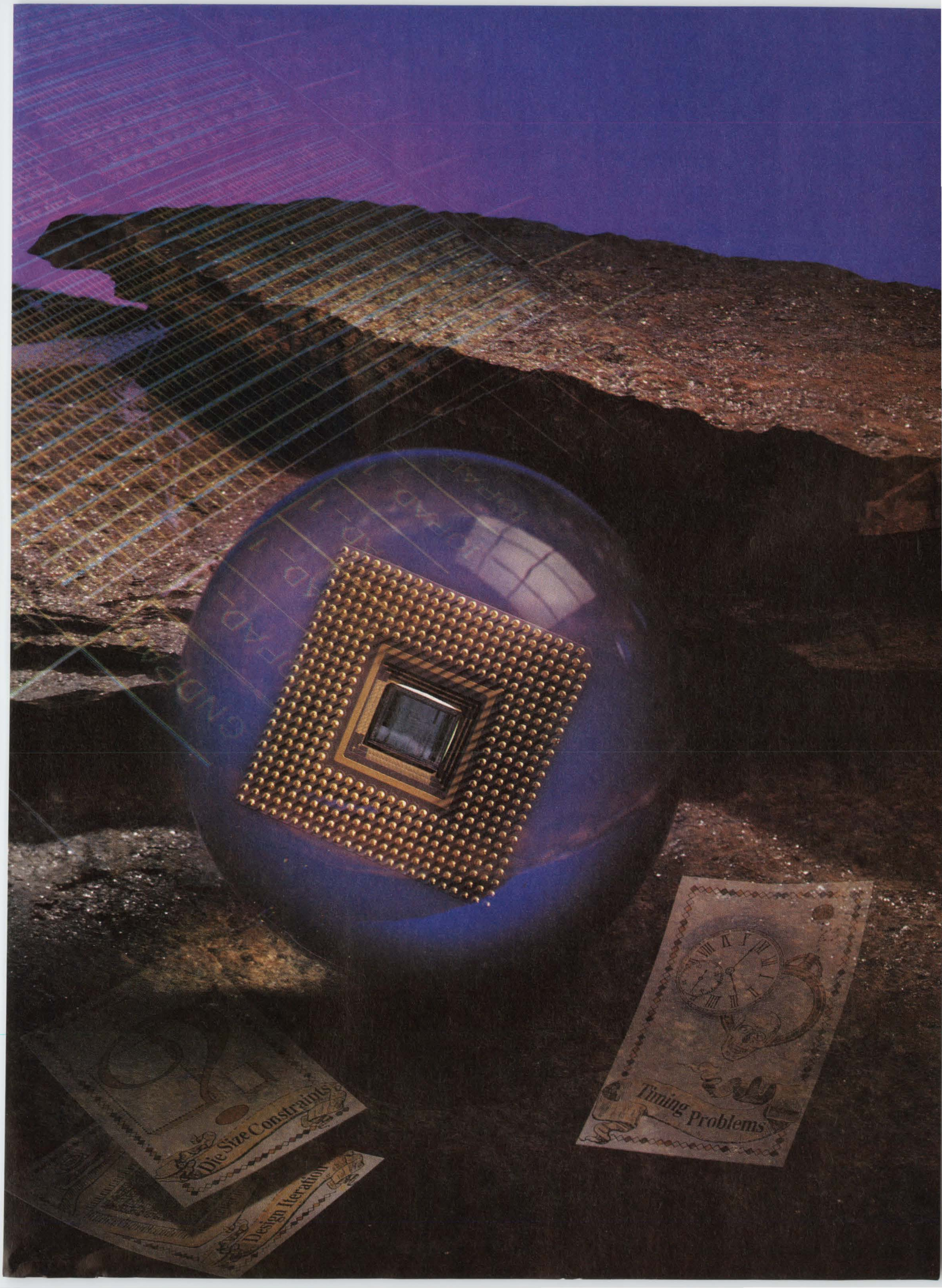
Fast, submicron designs have made it costly to postpone place and route until you complete logical design—too often, the design comes back from layout with unforeseen timing problems and other layout effects that require major rework of the logic. You can begin to control physical design by using a floorplanner (see "Floorplanning: layout comes to the logic designer," EDN, July 20, 1992, pg 154). In some situations, however, you may want to go all the way to buying your own place-and-route tools and bringing full control over physical design in house (**Fig 1**).

When deciding whether to bring layout in house or leave it to your fab, you should consider your business niche, the products you design, and your design methodology. Short time-to-market, high-volume and high-performance products, designs having more than 100,000 transistors, and fast clock rates all argue for doing your own layout with your own layout tools. Gate arrays, structured-custom designs (cell-based or "semicustom"), and full-custom designs each present their own twist on the general problems with bringing IC layout in house.

Designers leave layout of most array-based ASICs to the fabs. Because the distance between gates in a gate array is fixed



When you leave layout to your fab, you may get back a design that exceeds your die size or doesn't meet timing constraints. Having layout in house ensures that whatever happens, even multiple iterations won't leave your time to market on the rocks. (Photo courtesy Cadence Design Systems; photography, Dave Monley; art direction, Lisa Tollner)


Die Size Constraints
Design Iteration
Timing Problems

("frame" size), the system designer can only optimize the interconnect. Most often that procedure gives only small performance gains and does not justify a designer's involvement in physical layout. ASIC supplier LSI Logic reports that less than 10% of their customers have in-house layout tools. For most ASIC designs, low manufacturing volume does not justify designers' optimizing their own physical designs.

For large, full-custom designs, such as those done by Motorola's High Performance MPU Division (Austin, TX), layout in house may be the only way to go. "We could not do our 2M-gate designs without layout in house—we could not afford the place-and-route iterations," says David Leitch, CAD/CAE manager. Similarly, designers at Intergraph's Advanced Processor Division (Huntsville, AL) did their own layout for two custom microprocessors for the C4 workstation, according to Jennifer Smith, product marketing manager.

Cell-based design

In between gate arrays and full-custom designs lies semicustom design in its various flavors—structured-custom, embedded-array, and cell-based design. Such designs combine gate-array technology with prerouted

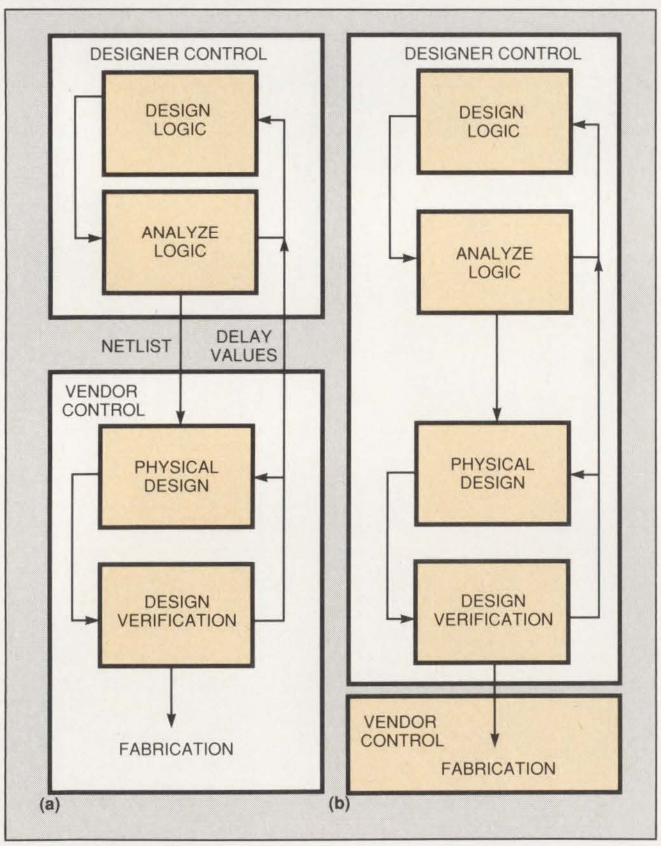
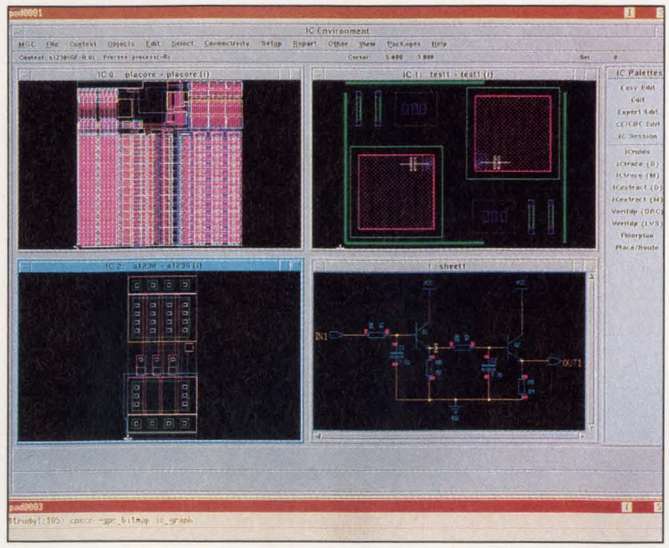


Fig 1—Traditional design methods leave physical design and design verification to the semiconductor vendor (a). Bringing layout in house puts physical design and design verification under control of the system designer (b).



IC Station, from Mentor Graphics, gives layout specialists the tools to handle both full-custom and cell-based designs. The windows show (clockwise from lower left), polygon editing, place and route, symbolic editing, and schematic-driven layout.

cells, logic or layout from module generators, and custom logic. The designer juggles blocks that come in many sizes and from a number of sources. He or she works with units of circuitry that range from single gates to complete microprocessor cores, dealing with many more variables than gate arrays present. "Semicustom is the prime market for in-house tools," says James Ulatowski, general manager for Dazix Intergraph.

In cell-based design, the systems house obtains libraries of "black-box" functional cells, usually from the semiconductor vendor. The systems engineer's "layout" job involves placing the cells and wiring their terminals together. Transistor-level designers who create cell libraries also refer to their work as "layout." One way to avoid confusion is to think of transistor-level design as "mask layout" and call the tools for that task mask-layout editors.

State of the art

The place-and-route tool market is still in its infancy. Available tools do the job but are few in number and therefore target very large, generally defined groups of users. The tools address unique sets of needs and do not compete head-on for the same customers.

Layout has an unwarranted reputation for being difficult to do, according to Donald Brandshaft, president of IC Editors. He contends that laying out an IC is actually easier than laying out pc boards, and that poor place-and-route software limits the progress of the ongoing trend toward consolidating board-level designs on chips. The chip-level designer works with only three layers of interconnect, compared with six or more for pc boards. In chip design there are fewer idiosyncrasies such as odd-sized packages to deal with.

Layout may be easy to do, but it is not widely done outside fabs. "Sociology, not engineering, is the bottleneck," says Brandshaft, referring to the weak showing that IC layout presents in engineering-school course work. "Most faculty cannot do layout themselves. Teachers are behind the times, and therefore give students the impression that this is an arcane subject." If most engineering students did laboratory work involving chip layout instead of just breadboarding discrete components or wire-wrapping pc boards, many more systems designers would be doing their own layout by now.

Even so, a systems house may design only one to four chips a year, compared with the layout designer working for a semiconductor vendor who may route several chips a week. The lower rate of design "turns" makes it hard for the systems house to keep an engineer current with the considerable volume of detail that is unique to physical design (**Fig 2**). To address this situation, most place-and-route tools offer the user a high degree of automation.

You may have the impression that layout is an exotic, specialized skill that is owned by the "polygon-pusher." In the old days (early 1980s), layout tools were simple graphics CAD systems that allowed the designer to put almost anything on screen, whether or not it made sense electrically and could be fabricated. Since then, layout tools have incorporated more and more rule checks and increasing levels of automation. Automated place and route appears in tools from Mentor Graphics, Compass Design Automation, Cadence Design Systems, Dazix Intergraph, Silvar-Lisco, Cascade Design Automation, and Tanner Research. For cell-based designs, Cascade Design Automation's tools can even give you pushbutton packaging design (see **Table 1**).

List prices for IC layout tools run the gamut from \$1000 for an introductory PC-based mask editor to \$180,000-plus for Cadence Gate Ensemble. List price for a minimal layout tool set runs in the \$50,000 to \$100,000 range for most packages (see **Table 1**). Yet purchase price represents a small fraction of the cost of software—most of the cost comes in the form of time spent learning to use it.

For your first foray into physical design, a low-end package minimizes your investment and takes less time to learn. For developing prototypes or for making modifications to existing designs, such a package may be all you need. PC-based ICED-32 from IC Editors

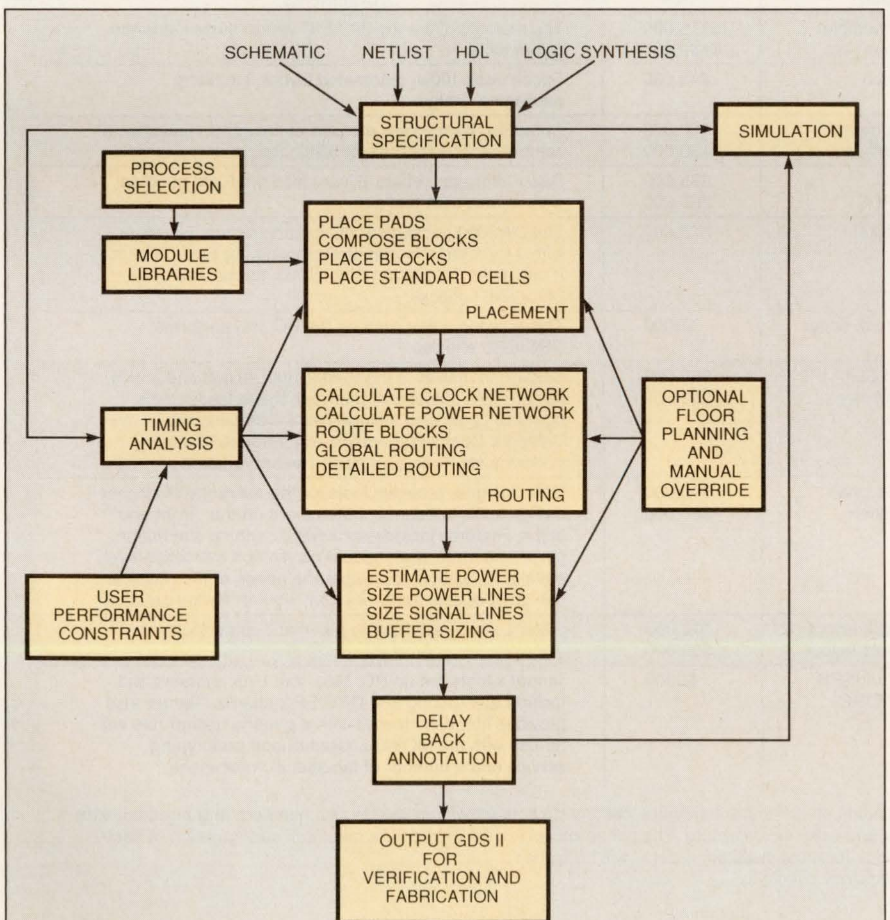


Fig 2—Automatic layout tools perform all the typical design tasks that follow structural specification and simulation.

gives you mask editing and design rule checking for $5000. You can unpack ICED-32 and learn to use it in one day, according to the manufacturer. At the high end, Mentor offers formal week-long training routinely with its products and puts an applications engineer on the customer site one day a week for several weeks thereafter. Ed Fischer, product marketing manager in Mentor's IC Group, describes the learning curve for Mentor's place-and-route tools as "a few weeks" for someone with an ASIC logic-design background.

Use your existing resources

For many organizations, bringing IC layout in house will not be a start-from-ground-zero proposition. Compass Design Automation reports that about 90% of its customers already have one person doing physical design in house. On the hardware side, most of those considering place and route already have networked workstations and so need only minor upgrades to bring layout in house, according to Bob Alessi, vice president of engineering for Cascade Design Automation. Upgrading may require as little as some additional memory or an add-in board.

Your first thought may be to buy a layout tool from your fab. You may be surprised to find that they go to an outside software house for their tools. Craig Silver, manager of product marketing in Toshiba Corp's (Sunnyvale, CA) System IC Division says, "At any given time, probably all major layout tools offered are either in use or being evaluated for purchase within Toshiba." Among the fabs that do not offer place-and-route tools to their customers are AMI, AT&T Microelectronics, Fujitsu, Motorola, NCR, NEC, TI, Toshiba, and UTMC (United Technologies Microelectronics Center). LSI Logic stands out as a fab that does offer place-and-route tools, including Smart Cell now and Smart Array during the fourth quarter of this year.

If most of your software already comes from one of the major electronic-design-automation (EDA) vendors, you can avoid some integration headaches by going back to them for place-and-route tools. Cadence,

Table 1—Representative place-and-route tools

Manufacturer	Product	Price[1]	Comments
Cadence Design Systems	Cell3 Ensemble Gate Ensemble	$115,000 $180,000	The majority of the top 30 ASIC vendors use Cadence layout tools.
Cascade Design Automation	Epoch	$49,000	Epoch does 100% automated layout, including packaging design.
Compass Design Automation	Chip Compiler Gate Compiler	$50,000 $50,000	Compass' layout tools are part of the ASIC Navigator, a comprehensive tool set for ASIC design.
Dazix Intergraph	SC GARDS	$35,000 $65,000	Dazix Intergraph offers Silvar-Lisco products bundled with its own EDA tool set.
Design Workshop	DW2000	$12,500	The DW2000 package is PC based and lets you work within the Calma Graphics Programming Environment. It translates Calma format to GDSII format and does DRC/ERC[2] checks.
IC Editors	ICED-32 mask editor	$5000	This polygon editor runs on the PC and performs DRC/ERC checks.
LSI Logic	Smart Cell Smart Array	$60,000 $60,000	Coming to market in the third (Smart Array) and fourth (Smart Cell) quarters of this year, these layout tools from LSI Logic also include Block Compiler and Datapath Compiler modules and produce optimum performance from LSI's silicon technologies.
Mentor Graphics	GDT Designer IC Station	$90,000 $90,000	GDT Designer provides tools for the full range of system-design tasks but concentrates more on the "front end" steps. Features include schematic capture, simulation, place and route, and module generation transistor-level editing. IC Station addresses the needs of the physical design specialist for full-custom work or library creation.
Silvar-Lisco	SC cell/block layout GARDS array layout	$30,000 $60,000	Silvar-Lisco specializes in place-and-route tools.
Tanner Research	L-Edit, L-Edit/SPR, L-EDIT/DRC	$9000	Tanner's tools run on PC, Mac, and Unix systems and include autorouting and DRC/ERC checks. Tanner also provides libraries created with a generic design rule set for use with the MOSIS shared-silicon prototyping service and a number of fab-specific processes.

Notes: 1. Prices for CAE software vary greatly depending on computer hardware, options such as maximum design size handled, and bundled extra tools such as simulators, module libraries, and schematic capture. The prices shown are list prices for a minimum configuration of each product to perform place and route. List price for most installed systems will be higher.
2. ERC/DRC=Electrical rules checking/design rules checking.

Mentor, and Dazix Intergraph all offer tools for physical design of gate arrays and structured custom ICs. These vendors give you place-and-route tools that are well-integrated into software for schematic capture, design rule checking, layout verification, synthesis, and other design functions.

The "point tool" approach may be more useful if you have specialized needs such as very fast place and route or want to closely integrate place and route with in-house tools. Point tools SC and GARDS are available directly from the manufacturer, Silvar-Lisco. Dazix Intergraph sells the tools under the same name and has integrated them with its EDA tool set. Viewlogic (Marlborough, MA) and Silvar-Lisco demonstrated the ease of connecting these tools by integrating SC and Viewlogic's Powerview in just three days. The demonstration at this year's Design Automation Conference showed interactive cross-probing between views of the cell-based layout and the corresponding logical schematics (**Fig 3**).

Why bring layout in house?

Many high-end microprocessor designers have always had layout in house because they needed to control timing. A high-end customer produces designs with some combination of advanced features such as clock rates above 40 MHz, gate count above 50,000 utilized gates, submicron feature size, or high-performance compiled cells such as data path or memory. As clock rates rise, more customers will be in the high-end category. Gate count alone may make your design high end. According to Steve Crain of Motorola's ASIC Division, "Ninety-five percent of our gate-array designs are laid out by Motorola, but large (100k-gate) designs

Algorithms

Barry Roitblat, Cascade Design Automation

Placement software commonly uses two algorithms, mincut and simulated annealing. Routing software commonly uses two other algorithms: maze and channel-based. Most current packages guarantee 100% completion, meaning that they come guaranteed to route your design. They very likely *do not* guarantee die size, however. You may wind up with a die size that yields unrealistic area, such as a 10×10-in. die.

Placement algorithms

Mincut for placement divides the set of cells into some number of groups such that the number of nets connecting any cell in one group to any cell in another group is minimized. This division tends to group highly connected cells closer together and thereby minimize overall route length on the chip. The algorithm may run recursively to partition the design to the desired level of resolution.

Simulated annealing is a general algorithm for solving combinatorial optimization problems. It finds the minimum (or maximum) of a function of many parameters, although, as a statistical technique, it does not guarantee an optimal solution. The algorithm proceeds with exploring the solution space by making pseudorandom moves within it and evaluating the results.

For VLSI placement, "moves" may be changes to placement, orientation, aspect ratio, etc. The evaluation function may include criteria such as total delay, total net length, chip area, or combinations of these variables. The algorithm maintains a "best result" as it searches the solution space. The algorithm may pass over a best result, although this probability decreases as the algorithm runs.

Routing algorithms

The regions between blocks of cells on a chip layout are called channels. Using two or more layers, the channel-routing algorithm makes connections between rows of terminals on opposite sides of a channel. The algorithm considers terminal location to be fixed along a channel on two opposing sides. The other two sides may also have terminals, but the algorithm considers them to be movable. These requirements limit the order in which the algorithm routes the channels, and also impose some restrictions on placement. Such restrictions avoid circular constraints, which would lead the algorithm to deadlock. The benefit of working within these restrictions is that the algorithm can guarantee fast, 100% completion of all routes in a channel with a predictable amount of space.

The maze-routing algorithm makes connections among terminals with arbitrary placement, using one or more layers. The algorithm does not use the concept of a channel. The terminals have fixed locations along both horizontal and vertical axes. The maze router searches for a path around obstacles from terminal to terminal. Maze routers usually use a fixed-spacing grid to reduce the complexity of the problem. Even with the restriction to a grid, time-to-complete may be substantial for maze routing. The time is proportional to the square of the distance between points, and the algorithm cannot guarantee a solution, even where one exists.

The author is director of marketing at Cascade Design Automation, Bellevue, WA.

are starting to be placed and routed by customers in house. We expect to see all high-end customers having layout in house by the year 2000."

Instead of doing complete layout themselves, most systems houses purchase layout tools so that they can tweak layouts done by their fab. "We keep the tools so we can do quick changes," says Jan Fandrianto, manager of IC research and development for Integrated Information Technology (Santa Clara, CA). IIT has had layout in house since its start-up in 1987. Because the staff had full-custom-design background, the learning curve on physical layout was moderate.

Two developing technologies that may spur more systems designers to bring IC layout in house are mixed-signal design and 3V power. Guido Arnout, VP of engineering for Silvar-Lisco reports, "Mixed analog/digital design users have always had place and route close to them due to the need to control interaction of the two on the physical level." An increase in mixed-signal design starts would presumably lead to more in-house layout. Nitin Deo, manager of ASIC applications engineering for Fujitsu (Sunnyvale, CA), expects 3V power to become a layout issue late in 1992 and early 1993. Mixed-voltage designs require more careful control of power-bus routing and metal migration. In addition, gate-array frame sizes differ for the two voltage levels. You will need to pay extra attention to these issues when you place and route mixed-voltage designs. If you do so, you can compensate for other penalties imposed by having two voltage levels.

"Semiconductor vendors are going to cell-based design to boost profit and value-added over that available from gate arrays," says Daniel Skilken, director of worldwide marketing for Compass Design Automation. "Overhead for the silicon vendor to place and route a gate array is fairly low due to its constrained, defined structure. Cell-based designs have more variables to juggle.... But design flow using cells is less automated, [actually] increasing overhead for the ASIC vendor. Pushing place and route out to the customer is one way to reduce this overhead."

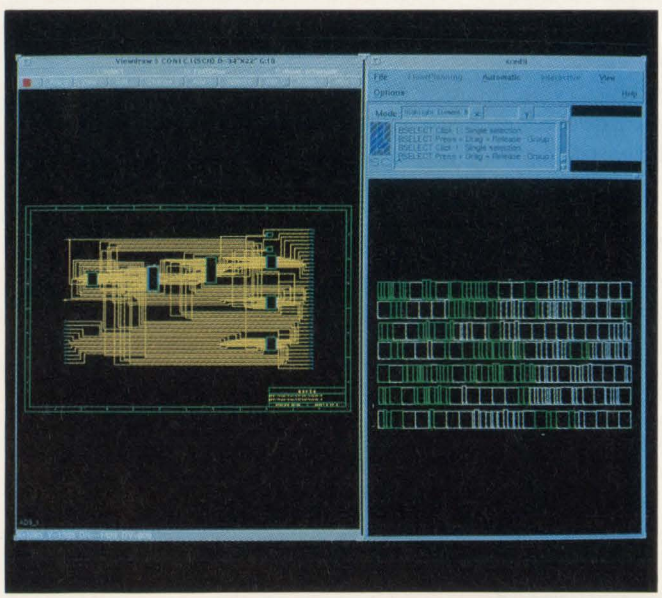
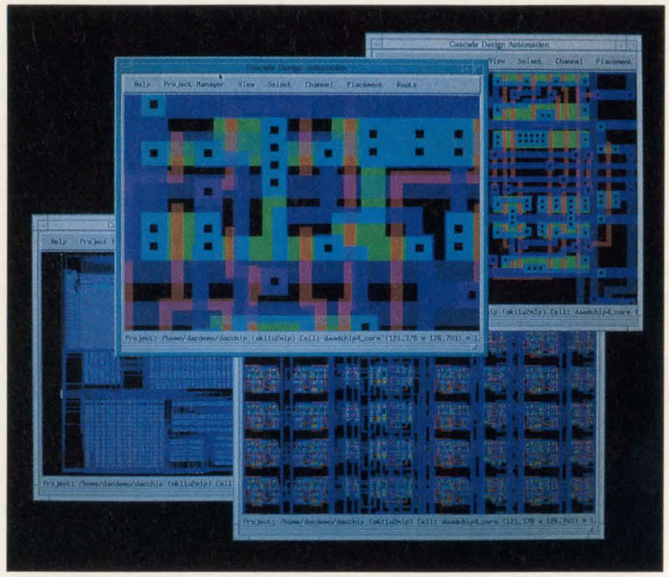


Fig 3—Selecting the logic symbol from a schematic in the left window (from Viewlogic's Viewdraw environment) highlights the corresponding cells in the right window (from Silvar-Lisco's SC cell/block layout system), in this demonstration of "cross-probing" and integration of point tools.



Several views show progressive detail of a data-path layout automatically produced by Epoch from Cascade Design Automation. The tool exploits the regularity of bus-oriented structures for efficient layout and can also handle arbitrary (irregular) netlists.

Despite that prediction, a survey of 10 US fabs for this article turned up only one that offers layout tools for place and route to its systems-house customers. "ASIC vendors are cautious in giving out their place-and-route tools," says Jackquie Taylor, product marketing manager in Cadence's IC design division. "The vendors risk being blamed for the chip not working after a layout done by a systems house. Very large-volume business from a systems house may justify letting out the tools."

Liabilities of the library

Doing your own layout requires that you use physical design libraries supplied by your semiconductor vendor within a design environment supplied by your EDA vendor. That can leave you in the middle, holding an error list from your software or failing silicon prototypes. When you do your own layout, you will be totally responsible for the success or failure of your design.

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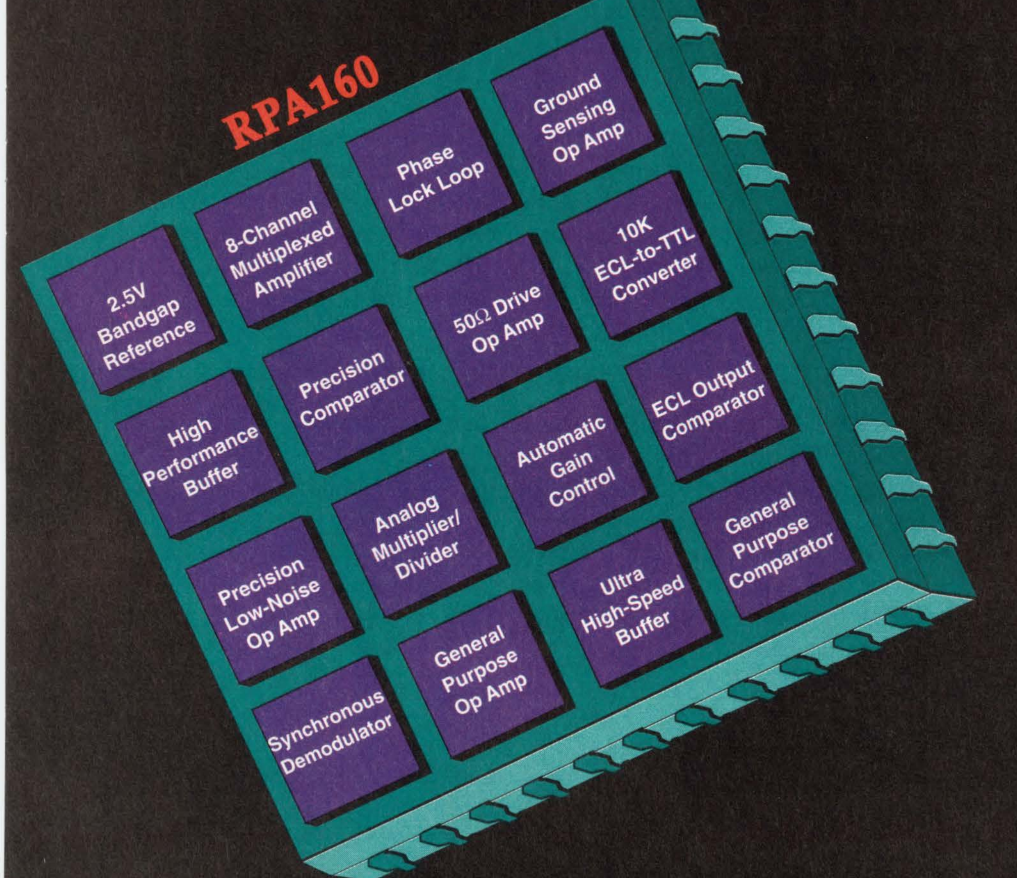

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with their libraries. As a new user of layout tools, you will probably start with cell-based designs. You will most likely get the cell libraries from your fab in "black-box" format and assume that they work. In that case, you will have to verify only the interconnect of your design.

If you want to do transistor-level design, you will need the full GDSII description of all cells and modules. Foundries readily give their customers the timing characterization of their silicon families and the logic description for functional cells implemented with them. But the next level down the information hierarchy, the GDSII description, gives information that describes the geometry of the physical layout. This level reveals physical line widths, diffusion area, oxide thickness, etc—information that is proprietary to the vendor. Semiconductor houses are reluctant to distribute GDSII files for all cells and modules.

Compass offers one easy route to library certification. It has prequalified the library it sells with eight semiconductor vendors. Tanner Research also offers standard cell libraries that have been certified by a number of fabs. Cascade Design Automation uses over 150 design rules to characterize physical layout. Its Epoch tool uses these rules to calibrate its functional module generators to libraries of a number of fabs.

Design steps in automated layout

Barry Roitblat, Cascade Design Automation

Layout tools from leading vendors all offer high automation with optional manual override. As a new user, you may begin doing place and route with "pushbutton layout." Among the most automated tools is Epoch from Cascade Design Automation. This tool's design sequence gives you an idea of the steps involved in automated layout.

The software accepts a netlist and user constraints and begins placement. If the user specified a pinout, the tool places pads to satisfy that pinout and the bonding and packaging constraints. The pad placement then becomes a constraint for placing the core. If the user did not specify a pinout, the tool places pads after the core using signal exports and package constraints.

To place the core, the tool first composes blocks for data paths and analog sections of the chip. A chip can have any number of data paths or analog blocks. The software then assembles the blocks with any other generated blocks (such as RAM, ROM, macrocells, etc) and divides the standard cells into groups to fill the gaps left by the blocks. It then performs an optimization step on the block placement and separately within the standard cell groups. Placement optimization takes into account path criticality, net length, area, and user-assignable weights.

You can invoke interactive optimization at this stage by calling the Epoch Floorplanner. Within that tool, you can modify the placement, orientation, or aspect ratio for the cells as well as other physical parameters.

Getting to the route

The layout tool proceeds next with global routing (which you can also perform interactively) followed by detailed routing. Global routing assigns a sequence of channels that each net will pass through. The tool routes as many nets as possible over cells. It routes power lines and clocks first, then sizes and segments power-line networks based on load and clock frequency, optimizing voltage drop and current density. The software then calculates clock trees for each of the clocks to minimize skew between them and between the nodes for each clock.

Detail routing first completes the over-cell portions using a maze-routing algorithm. The tool keeps track of over-cell blockage areas (portions of a cell that block over-cell routing). The software spills any routes that it cannot complete over cell into adjacent channels for routing by a channel router. Channel routing guarantees predictable results, and each channel includes just enough space to complete the routes.

The software uses a gridless contour router. Gridless means that ports or nets are not limited to fixed spacing or locations by the tool itself. Contour routing means that the tool follows the edges of obstructions to leave the maximum amount of open space in the middle. The over-cell and channel routers include optimizations that take advantage of the regularity of bus-oriented data-path structures. Routing also segregates noisy nets from sensitive ones.

After 100% completion of routing, the tool sizes buffers. It optimizes buffer drive and, hence, the delay along the critical path. You may also change the size of noncritical elements at this stage or set up module generators to size buffers automatically. Since buffer sizing may change the physical size of the cell, the tool performs an incremental reroute to adjust the layout accordingly.

The author is director of marketing at Cascade Design Automation, Bellevue, WA.


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Cascade does not act as a broker or packager of silicon libraries themselves, however.

A place-and-route tool is more than an interface to a semiconductor vendor's libraries—it accepts input in a variety of design entry formats. EDIF is the standard format used to transfer design descriptions to layout tools, whether the design originates as a schematic, uses a hardware description language, or comes from a synthesis package. GDSII stream format is used for both library definition (foundry sends to customer) and IC definition (customer sends to foundry). The foundry "fractures" the GDSII shape definitions into smaller polygons that mask generation devices can handle.

Performance issues

At $50,000 to $100,000, place-and-route tools are not commodity items, so it is understandable that there are no commonly used benchmarks for them. Your best approach for evaluating a layout tool will most likely be to make up your own benchmark. Take one of your representative designs to the software vendor and have it placed and routed while you watch. Use any automated layout and interactive layout editing features. Try out any alternative design-entry methods, such as VHDL or synthesis packages. Keep track of such performance measures as gate utilization (for gate arrays), meeting timing constraints, runtime, wire length, die size, and number of vias.

As you evaluate, you should find that full-featured layout software offers most of the following: 3-layer routing; 100% automatic routing with option for manual, interactive overrides; hierarchical, symbolic editing of layout with option to edit the design in "flat" or gate-level, form; timing-driven placement and routing; ERC/DRC (electrical rules checking/design rules checking), or interface to an ERC/DRC tool; RC tree modeling of net delays; floorplanning; module generation; and clock-tree synthesis.

Layout tools use a variety of algorithms for placement and routing. See the **box**, "Algorithms," for descriptions of two of the more common methods. Beyond placement and routing, automated layout tools must work within a host of constraints that the user defines or the tool selects as defaults. See the **box**, "Design steps in automated layout," for a description of one product's design flow. EDN

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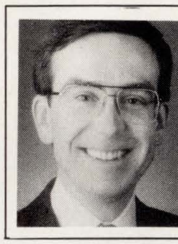

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Manufacturers of place-and-route tools

For more information on place-and-route tools such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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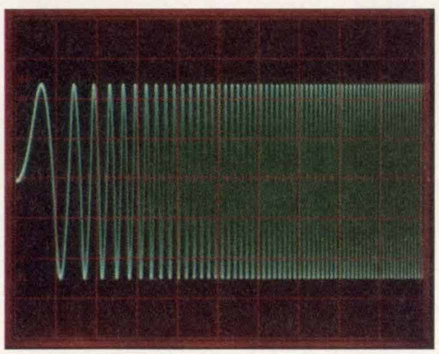

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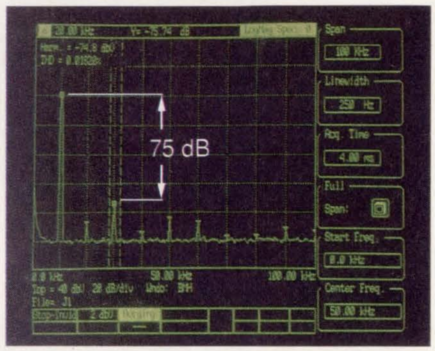
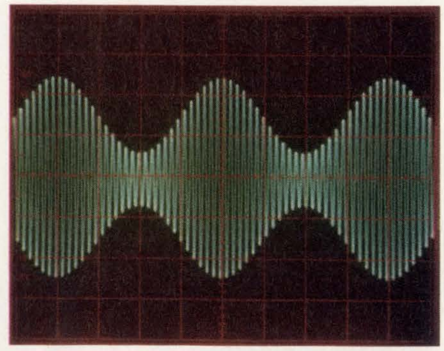


DS335's clean output spectra

The DS340 is similar to the DS335, with a frequency range which extends to 15.1 MHz, and arbitrary waveforms. Arbs may be programmed with 12 bits of vertical resolution, record lengths to 16k points, and sample rates to 40 MHz. A linear phase filter provides smooth outputs with a 10 MHz bandwidth.



DS345 offers AM, FM, PM and Burst modulation

The DS345 has all of the features of the DS340 with frequencies up to 30.2 MHz, and a rich set of modulation capabilities. Any of the standard waveforms may be amplitude, frequency, or phase modulated by sines, squares, ramps, triangles or arbitrary modulation patterns. Several DS345's may be slaved together via an external clock input, and the phases between their outputs may be adjusted with millidegree resolution.

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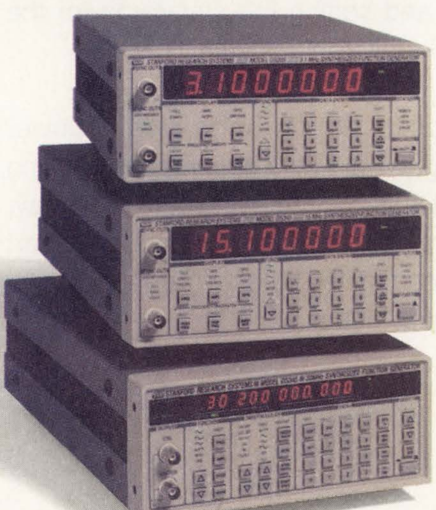

	DS335	DS340	DS345
Max Freq (Sine/Sq)	3.1 MHz	15.1 MHz	30.2 MHz
Freq Resolution	1μHz	1μHz	1μHz
Standard Timebase	±5 ppm	±5 ppm	±5 ppm
THD (f_0=10 kHz)	< 0.05%	< 0.05%	< 0.10%
Spurs (f_0=1 MHz)	<-65 dBc	<-65 dBc	<-55 dBc
Level Accuracy	±0.1dB	±0.1dB	±0.2dB
Modulation	FSK	FSK	AM,FM,PM, FSK,Burst
Arbitrary Waveforms	none	12 bits to 16k points and 40 Msamples/s	
GPIB/RS232	$395	$495	$495
Price	**$995**	**$1595**	**$2195**

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CIRCLE NO. 77

Understanding synthesis begins with knowing the terminology

Steve Carlson and Emil Girczyc, Synopsys Inc

Jargon and buzzwords make synthesis confusing. You can cut through much of the confusion by sticking to a vocabulary that has gained wide acceptance.

To understand synthesis, you need to know the language of synthesis. Unfortunately, the language is unclear; many synthesis terms have different meanings to different people. Nearly everyone agrees on certain terms, however, and understanding those terms can help you understand the issues of synthesis.

Synthesis is actually a continuum, but its practical application includes discrete tasks associated with behavioral synthesis, RTL (register-transfer level) synthesis, and logic synthesis (**Fig 1**). Although you will sometimes encounter references to other kinds of synthesis—architectural synthesis and system-level synthesis, for example—those terms don't have precise definitions.

Behavioral descriptions are at the most abstract level of synthesis. These descriptions describe what modules do, but not how they do it or how many clock cycles they need to do it. For example, a behavioral description of a CPU contains no notion of an ALU or that the ALU might be pipelined. Rather, the behavioral CPU description contains many specifications that may be realized on (or mapped onto) a single ALU in almost any circuit technology, and in one or many clock cycles.

Note that the use of behavioral constructs, such as *case*, *if-then*, and *for* loops, does not necessarily imply that the model in which they are contained is behavioral. The larger context, or the model style, determines the model classification to a much larger degree than the individual constructs do.

RTL descriptions, also known as data-flow descriptions, are at the next abstract level below behavioral descriptions. They define a system in terms of registers, switches (multiplexers), and operations. They're different from behavioral descriptions in that they have a notion of an architecture and a clocking scheme. Like behavioral descriptions, RTL descriptions are technology independent.

Logic descriptions are the lowest-level nonphysical representation of a design. At this level of abstraction, a Boolean network or netlist describes a design implementation. These descriptions not only retain the

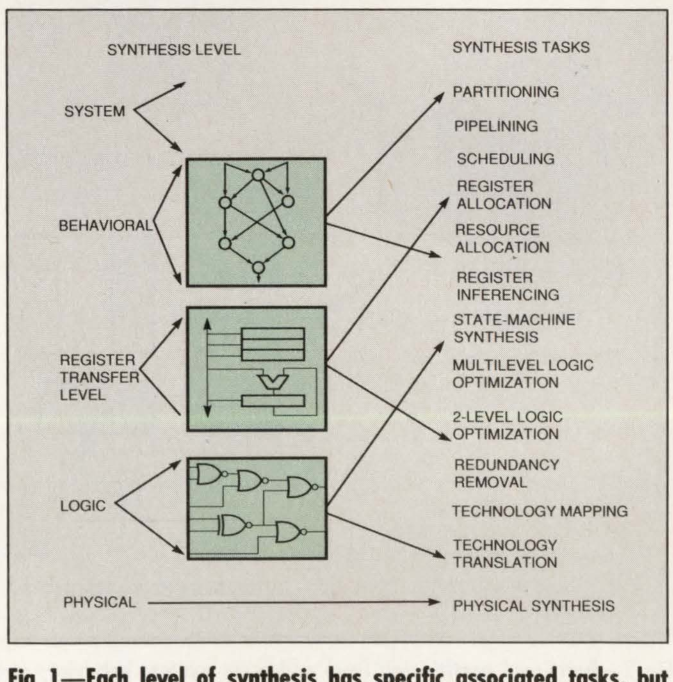


Fig 1—Each level of synthesis has specific associated tasks, but some tasks overlap levels.

architecture derived at the RTL level, but also show the local Boolean architecture or the logical implementation of the function. Although it is possible to represent such designs in a generic technology, such descriptions typically depend on a particular technology.

The task of designing electronic systems is a process of refining to successively more detailed, and thus more complex, design descriptions. The design-synthesis tasks associated with adding detail to the design description are shown in the right column of **Fig 1**. Each of these tasks represents a major area of research in the field of automated design synthesis.

Partitioning

The first synthesis task, partitioning, divides a design into smaller pieces to be implemented as separate modules, ICs, or boards. Partitioning may accommodate hard constraints, such as die size or package-pinout limitations, or it may decrease circuit cost or signal delays by simplifying connections. Partitioning can be functional (applied to system behavior) or structural (applied to circuits). **Fig 2** illustrates both types.

Fig 2's top branch depicts the partitioning of a behavior into a module-level description. This type of partitioning is purely functional; mapping the functional partitions onto physical partitions occurs later in the implementation process. **Fig 2**'s lower branch depicts an initial structural partitioning, in which the mapping of behavior onto hardware units occurs early in the design process. Note that the two partitionings of **Fig 2** yield different hardware implementations. The design hierarchy that you specify using a hardware description language (HDL) not only helps manage design complexity, but also specifies partitioning, thus affecting your design's eventual hardware implementation.

Pipelining

Pipelining partitions an algorithm's execution flow into a number of sequential stages that execute simultaneously, enabling a circuit to process data at a higher rate by working on different portions of the algorithm in parallel. A pipelined instruction may actually take longer to execute than the same instruction implemented without pipelining. Overall program speed increases, however, because several pipelined instructions can execute at once.

Fig 3 illustrates the pipelining of a floating-point addition instruction into three stages. To see how throughput increases, suppose that a complete single-cycle (not pipelined) floating-point addition occurs in 18 nsec.

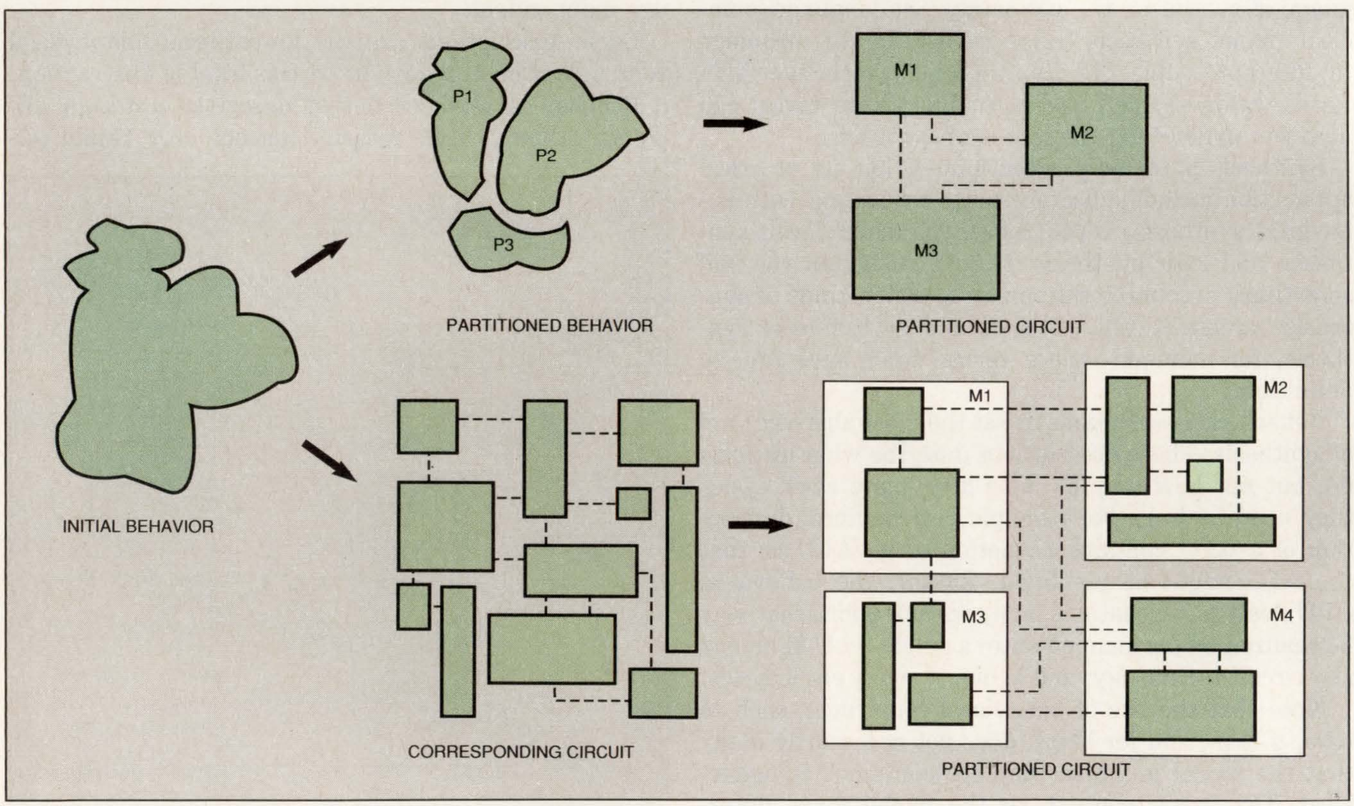


Fig 2—Functional partitioning (top) addresses system behavior; structural partitioning (bottom) deals with devices for implementation. The two approaches yield different results.

Now, suppose that an identical floating-point addition occurs in three 6-nsec stages. In this pipelined implementation, the overall calculation for a single addition increases by 2 nsec because the registers between stages each provide a 1-nsec delay. However, a new addition can now begin every 7 nsec, so effective throughput increases by a factor of more than 2.5.

Functional pipelining, which partitions an algorithm's data flow into stages, results in a circuit in which the different stages share hardware resources (multipliers, for example). Generalized pipelining tries to balance path lengths between pipeline registers to maximize throughput.

Scheduling

Scheduling assigns the operations in a behavioral description to a sequence of control states or clock cycles. **Fig 4a**, which illustrates an algorithm before scheduling, shows an arithmetic formula in the form of a dataflow graph. This description is behavioral; it defines the transformation of a set of inputs into a set of outputs, but it does not give any information on how to implement this formula in hardware. The scheduling problem is to take this behavioral description and partition it into a number of control steps, or clock cycles (Fig

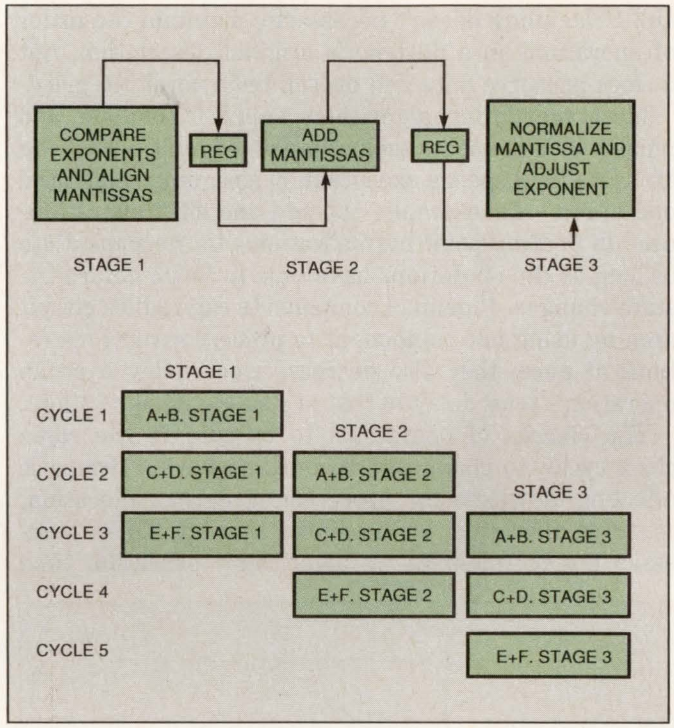


Fig 3—Pipelining partitions an algorithm's execution flow into a number of stages that execute simultaneously.

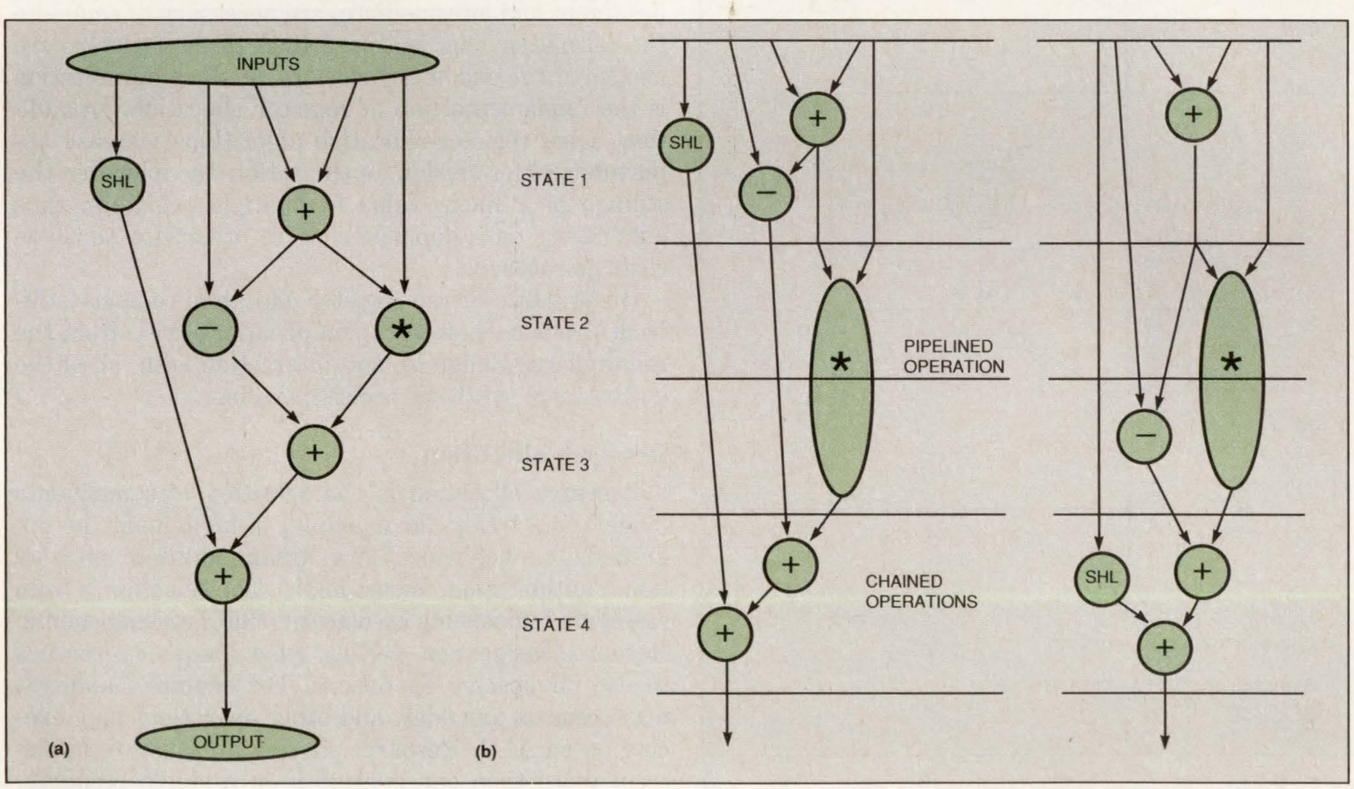


Fig 4—The description of an algorithm before scheduling (a) shows the transformation of inputs to outputs, but not the hardware implementation. Scheduling (b) places the algorithm's operations in different clock cycles. Which operations are chained or pipelined affects both execution time and required hardware resources.

4b). Scheduling doesn't necessarily maintain the order of operations in a designer's original description, but it does preserve data and overall behavioral integrity.

Most scheduling algorithms support chaining and pipelined components such as pipelined multipliers (**Fig 4b**). Chaining speeds execution by assigning sequential operations—for example, the add and shift operations used in floating-point normalization—to the same state as long as the operations have time to finish before the state changes. Pipelined components can reduce circuit area by using one component to process several operations at once; they also decrease clock delay from an operation's total delay to that of a single pipeline stage.

The choices of operations to execute in the same clock cycle, to chain, and to pipeline have a dramatic effect on "downstream" processes of register allocation, resource allocation, and resource sharing. These processes try to minimize an algorithm's execution time (cycle period × number of clock cycles) or minimize the resources needed by an algorithm to execute within a given time.

Fig 4b shows **Fig 4a**'s algorithm with two different possible schedules. Algorithm behavior is the same for both cases, but implications on downstream implementation are quite different. The SHL (shift-left) and subtract operations, for example, can go into different clock cycles to optimize either throughput or resource requirements.

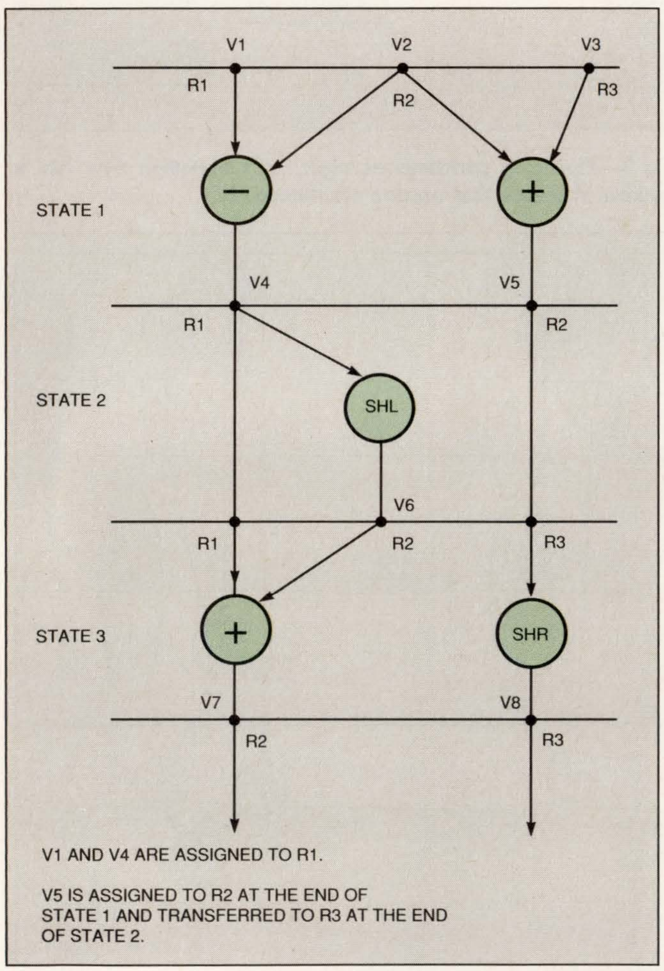


Fig 5—Register allocation selects registers for storing values that get generated in one clock cycle and used in a later cycle. To minimize the number of required registers, the process assigns only "live" values—not variables—to registers.

Register allocation

Still within the realm of behavioral synthesis, but also overlapping with RTL synthesis, is register allocation. Register allocation (also called register assignment) selects registers for storing values that get generated in one clock cycle and accessed in later cycles. To minimize circuit area, each user variable does not get a dedicated register. Instead, registers are for live values only; each assignment of each variable is a separate value to be stored. Thus, different values of a variable may be in different registers. That is, the binding of a variable to a register is dynamic.

Fig 5 illustrates register allocation using a chain calculation scheduled into three clock cycles. Eight values (input and intermediate) are necessary to complete the calculation, but no more than three registers are needed at the end of any clock cycle. Such optimization is the fundamental job of register allocation. In addition, some register-allocation algorithms increase opportunities for design optimization by allowing the storage of a single value in multiple registers, thus eliminating data dependencies in otherwise separate chain calculations.

Performance-driven register allocation remains a difficult problem, however. Complications arise from the required knowledge of, and interaction with, all of the downstream synthesis tools' operation.

Resource allocation

Resource allocation is the selection of components (adders and ALUs, for example) to implement the operations of a behavioral description (addition, subtraction, multiplication, and so forth). The selection is from candidate components in some set of library components. Resource assignment decides what kinds of resources to use for specific operations. For example, addition may occur on an adder, and other operations may execute on an ALU. Resource sharing attempts to implement more than one operation on a single resource. The constraint is that the operations must not need to execute at the same time (in the same clock cycle).

Module binding (or implementation selection) selects a specific component from a parts library for each resource and translates constraints on the resource into parameters of the component. For example, the selection of an adder could involve a choice between a ripple-carry adder and a carry-select adder.

Fig 6a shows a scheduled arithmetic computation, and **Fig 6b** shows the computation's implementation after resource allocation and sharing. A label next to each operation in **Fig 6a**'s data-flow diagram indicates the type of resource needed (ALU or adder) to perform each operation. Only two hardware resources are necessary for the five operations.

In synthesis systems, much interaction is necessary between resource allocation and resource sharing, and between those operations and higher-level synthesis operations (pipelining and scheduling) and lower-level synthesis tasks.

Register inferencing

Register inferencing determines which values must be preserved across cycle boundaries and under what conditions those values must be preserved. The process instantiates a register (or a latch, if appropriate) to store each value and then connects the appropriate clocking, asynchronous-reset, and/or load-enable pins.

An illustration of register inferencing appears in **Fig 7**, in which the VHDL wait statement of process P1 indicates clock dependencies. Variable *a*, which gets read before it gets written, needs a register; variable *b*, which gets written before reading, does not. In process P2, signal *f* gets gated by the signal level of *L* and thus needs a latch.

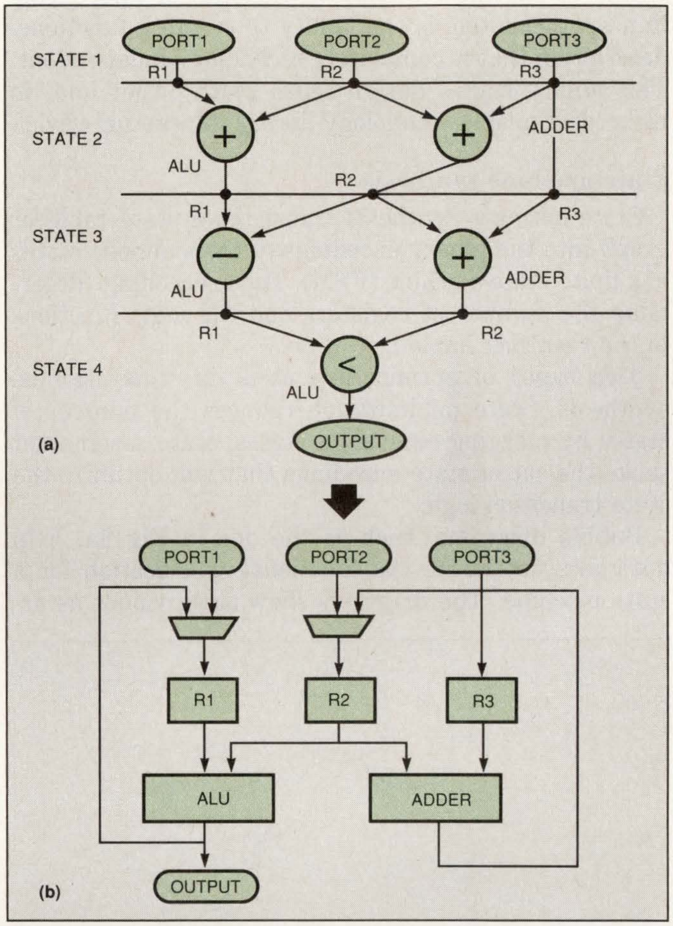


Fig 6—Resource sharing allows multiple operations on a single resource in different clock cycles (a). As (b) shows, one ALU and one adder perform the five arithmetic operations.

VHDL source code

```
P1 : process begin
      wait until clk'event and clk='1'
      b := a or c;
      a <= b and e;
end;

P2 : process(L,e) begin
     if    L then
              f <= e;
     end  if;

end;
```

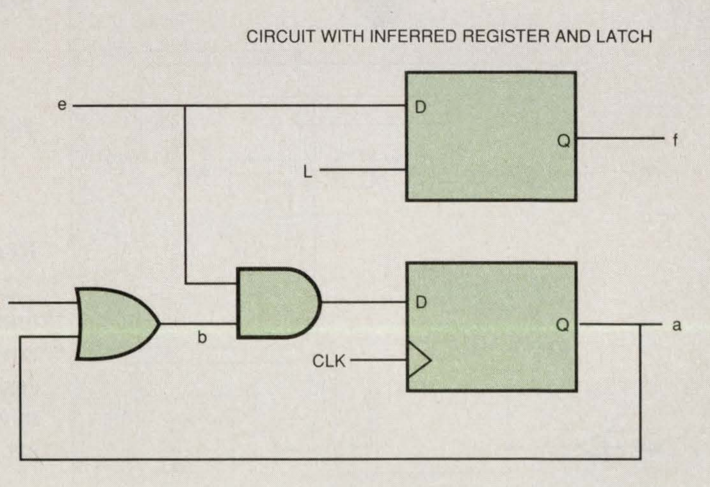


Fig 7—Register inferencing determines which values must be preserved across clock-cycle boundaries. In this example, value a needs a register, because process P1 reads a before writing it; value b needs no register, because the process writes it before reading it. Process P2's signal f needs a latch.

One of the most important benefits of inferencing in a synthesis tool is the ability to create a functional description that is completely technology independent. This ability makes design reuse much easier and, in most cases, makes technology-library retargeting trivial.

State-machine synthesis

State-machine synthesis translates a state table or graph into the binary encodings of the symbolic states of a finite-state machine (FSM). These encodings determine the number of registers and the logic functions in the resulting implementation.

Two types of optimization occur in state-machine synthesis. State minimization reduces the number of states by merging equivalent states; state assignment seeks the set of state encodings that will optimize the state-transition logic.

Bubble diagrams, such as the one in **Fig 8a**, help designers determine the functional specification for a state machine. The diagrams show state values as ordered pairs of input values and output values. **Fig 8b** shows an FSM synthesized from **Fig 8a**'s diagram. The synthesized FSM has one flip-flop for each state in the FSM diagram, implying that the FSM's designer may have chosen one-hot encoding (only one state-vector bit high for any given state) to maximize the state machine's speed.

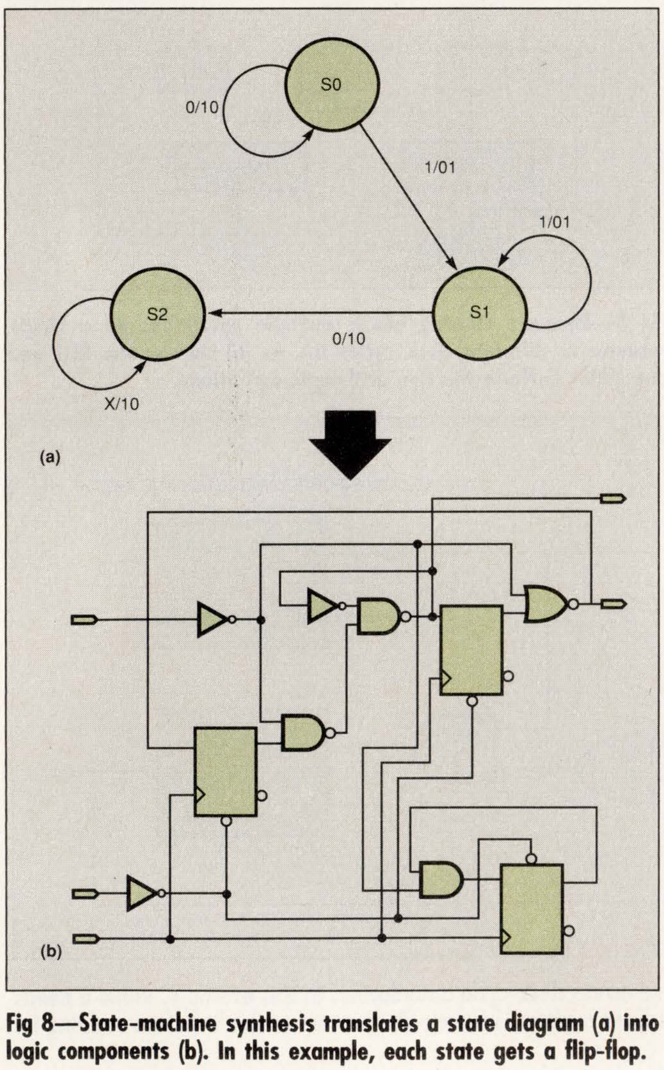


Fig 8—State-machine synthesis translates a state diagram (a) into logic components (b). In this example, each state gets a flip-flop.

Multilevel logic optimization

Multilevel logic optimization takes a netlist of gates that describes a combinational-logic circuit and creates a new description that results in faster circuit operation, less circuit area, or both. The improvements typically occur through a series of transformations called restructuring and simplification.

Restructuring finds logic that multiple equations can share, which typically results in a smaller logic network but can also increase path delay by increasing the fanout of shared terms.

Simplification finds simpler logic equations with the same behavior as the original input. Such reductions often decrease both the number of gates and critical-path length.

Two-level logic optimization

A 2-level logic representation, also known as a PLA or AND-OR representation, is a specialized form of multilevel logic. For designs representable as 2-level logic, special algorithms and heuristics can determine a near minimal implementation in a practical amount of time. For example, Espresso, a tool from the University of California at Berkeley, uses such rules and algorithms. The following equations illustrate the optimization of a Boolean equation to a 2-level AND-OR Boolean equation:

$$f = xyz + xy'z' + xy'z + x'yz + xyy'z$$

yields

$$f = xy' + yz.$$

Redundancy removal

Redundancy removal is the process of identifying and removing redundant logic. Redundancies waste circuit area, may affect performance (because of unnecessary fanout), and can make test-pattern generation more difficult (because redundant portions of the circuit are untestable).

Technology mapping

Although logic optimization minimizes a Boolean network, it is still possible to implement the network in different ways through the choice and connection of logic elements from a library. Technology mapping, however, transforms a technology-independent Boolean network into a netlist that is specific to a particular ASIC vendor. The goal of technology mapping is to find the combination of elements that best achieves the designer's goals for circuit performance, circuit area, or power consumption. **Fig 9** shows technology-independent logic functions implemented with 2-input NAND gates and inverters.

Technology translation

Technology translation, a specific application of technology mapping, converts a design from one technology-specific implementation to another. It allows reimplementing older ASICs, fabricated in obsolete technologies, in new technologies. Technology translation takes two different approaches:

- For each gate in an original design, find the cell in the new ASIC library that most closely matches.
- Translate a technology-specific netlist into a technology-independent Boolean network; then optimize the network and map it to a new ASIC library.

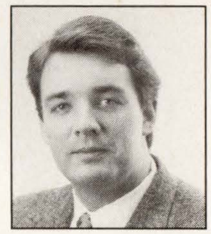
The first approach executes much faster because it occurs through a simple library-linking mechanism. The second approach can yield a better implementation, however, because gate selection occurs under the design constraints and analysis for the new target library.

Physical synthesis

Physical synthesis includes many different capabilities with one common theme: the results are tied to a particular ASIC vendor and silicon process. Logic synthesis produces optimized instantiations and connections of devices; physical synthesis creates the mask-level design that implements this structural description. In conjunction with the aspects of synthesis already discussed, physical synthesis encompasses all the design steps for translating a gate-level netlist to the physical design of an ASIC at the polygon level (including floor planning, placement, and routing).

Some capabilities normally considered part of physical synthesis include silicon compilation and technology-specific layout generators (also called module generators) for blocks such as RAMs and ROMs.

Authors' biographies



Steve Carlson is manager of methodology at Synopsys Inc, where he has worked for the last four years. His work has included the design of compilers (including a VHDL compiler) and timing analyzers. Steve holds MSEE, BSCS, and BSEE degrees from the University of Colorado at Boulder and is a member of the IEEE and the ACM. In his spare time, Steve enjoys playing golf.

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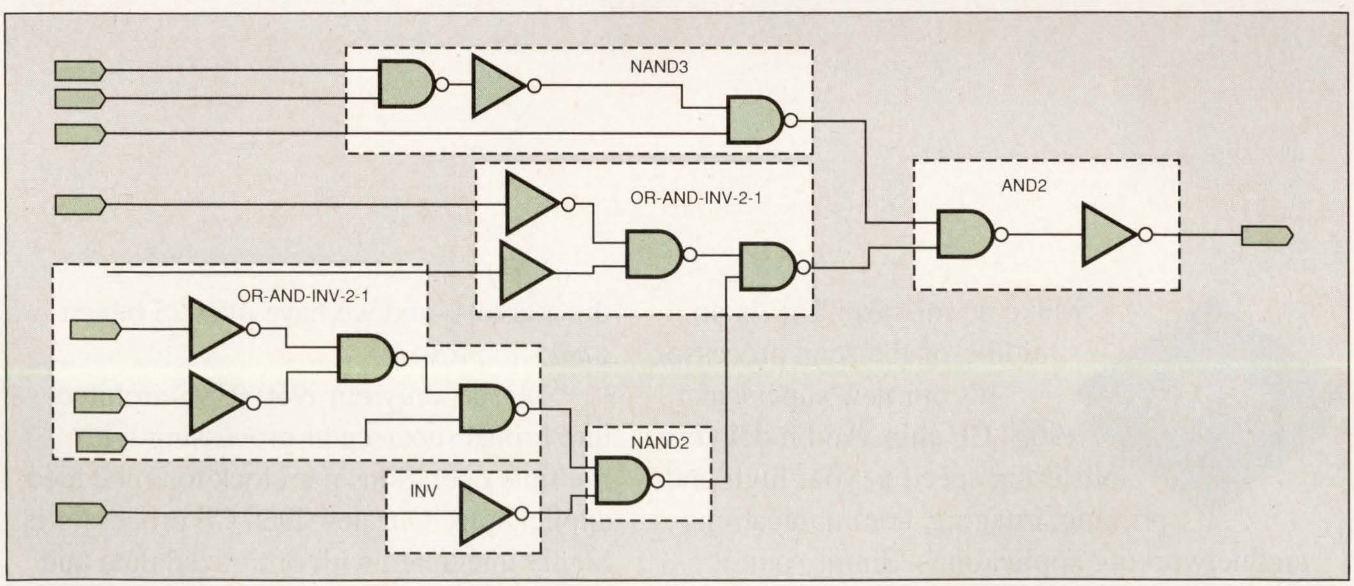

Fig 9—Technology mapping transforms a technology-independent Boolean network into a vendor-specific netlist. In the example shown here, technology mapping has implemented various logic functions (indicated by labels) with 2-input NAND gates and inverters.

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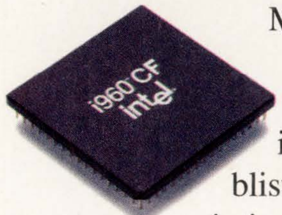

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CIRCLE NO. 118

Designer's guide to sampling A/D converters Part 1

Basic characteristics distinguish sampling A/D converters

Walt Kester, Analog Devices

The characteristics of sampling A/D converters are often quite different from those of nonsampling converters. Part 1 of this 3-part series discusses static and dynamic characteristics; minimizing switching transients, which are inherent to sampling ADCs; and protecting the analog input. Part 2 will consider the input amplifier, antialiasing filters, references, and clock. Part 3 will describe how to interface the ADC to a system and will provide guidelines for grounding and power-supply filtering.

You can find monolithic sampling ADCs having resolutions of 16 and 18 bits and sampling rates greater than 50 ksamples/sec. Examples include such devices as the AD676, AD1879, and AD7884. Hybrid devices such as the AD1332 can achieve sampling frequencies of 500 ksamples/sec and higher at 16-bit resolution. Sampling converters—by definition—contain a built-in sample-and-hold (S/H) circuit. S/H circuits make these devices much easier to use than earlier ADCs that used several discrete components to implement sampling. However, sampling ADCs still require critical external support circuits, and you must use precision and high-speed techniques to achieve data-sheet performance levels.

For example, a drive amplifier conditions the ADC's input signal by providing gain and offset. You need to make sure that this amplifier is compatible with the ADC's dc and ac characteristics, and the dc and ac specifications of sampling A/D converters often differ from those of traditional nonsampling converters. You'll also need to know techniques for minimizing the effects of switching transients on the ADC's analog input. Finally, you'll have to know how to protect the sensitive analog inputs of sampling ADCs by using clamping and other protection circuits.

Key dc performance characteristics

Sampling ADCs generally have a set of dc specifications that includes gain and its temperature coefficient, offset and its temperature coefficient, differential linearity, and integral linearity. To ensure initial calibration accuracy, most sampling ADCs incorporate thin-film resistors that vendors trim to the appropriate value during manufacture.

Some 16-bit and higher-resolution sampling ADCs are self-calibrating (autocalibrating), a feature that eliminates the need for thin-film resistors. Although laser trimming thin-film resistors works well and yields economical devices having resolutions as high as 14 bits, maintaining absolute resistor accuracy after packaging is a real challenge at resolutions of 16 bits and higher. Two disadvantages of autocalibrating ADCs are their large chip area and the need for periodic calibration routines. When using autocalibrating converters, however, always check the data sheet to see if temperature-related specifications are valid after the initial autocalibrating routine or if you need to perform the routine periodically as the temperature changes. You must also provide the necessary timing signals to perform the routine.

Although dc specifications are fairly well standardized, precision 16-bit sampling ADCs may behave differently from their 12-bit counterparts. Ideally, a fixed dc input to an ADC should result in the same output code for repeated conversions. Historically, designers have analyzed ADCs for code-transition noise by using a DAC to reconstruct the analog input signal. They applied a slow ramp voltage to the ADC and observed each code transition. With a precision 16-bit sampling ADC, however, this test will probably produce some unexpected results. For a given input voltage you're likely to have a range of output codes. This behavior is due to unavoidable circuit noise within the wideband circuits in the ADC. The noise is equivalent to summing the broadband noise with the input of a noiseless AD converter.

If you apply a dc signal to the precision sampling ADC and record several thousand outputs, the result will be a distribution of codes such as the **Fig 1** histogram for the AD7884 16-bit, 166-ksample/sec ADC. The correct code appears 50% of the time, but adjacent codes also appear. If you fit a Gaussian probability distribution to the histogram, the standard deviation is approximately equivalent to the rms input noise of the ADC. The actual specification on the ADC's data sheet may be in the form of a histogram similar to **Fig 1**, or the spec may appear as an equivalent rms input-noise voltage.

This noise may come from several sources. For example, a 1-MΩ resistor generates 158 μV rms of Johnson, or thermal, noise over a 1-MHz single-pole bandwidth. The equivalent noise bandwidth is 1.57 MHz. Comparing this 158 μV of noise with a 16-bit ADC having a 10V input-voltage range and an LSB of 153 μV illustrates the importance of keeping the ADC's driving impedance low. Note also that the wideband S/H amplifier generates some of the internal ADC noise.

Sampling ADCs have input bandwidths that usually far exceed the Nyquist frequency, which is half the sampling rate. For example, the 16-bit, 100-ksample/sec AD676 ADC has an input bandwidth that exceeds 1 MHz. ADCs require such wide bandwidths to minimize gain and phase distortion at the signal frequencies of interest. As a result, the S/H circuit and other wideband circuits within the ADC will generate a certain amount of unavoidable noise, which causes the sample-to-sample variation in output code for dc inputs. Good layout, grounding, and decoupling techniques are mandatory to prevent additional external noise from coupling into the ADC and adding to the inherent input noise.

One way to reduce the input noise of the ADC is to use oversampling and digital filtering. The input noise is uniformly spread over the Nyquist bandwidth, $f_S/2$.

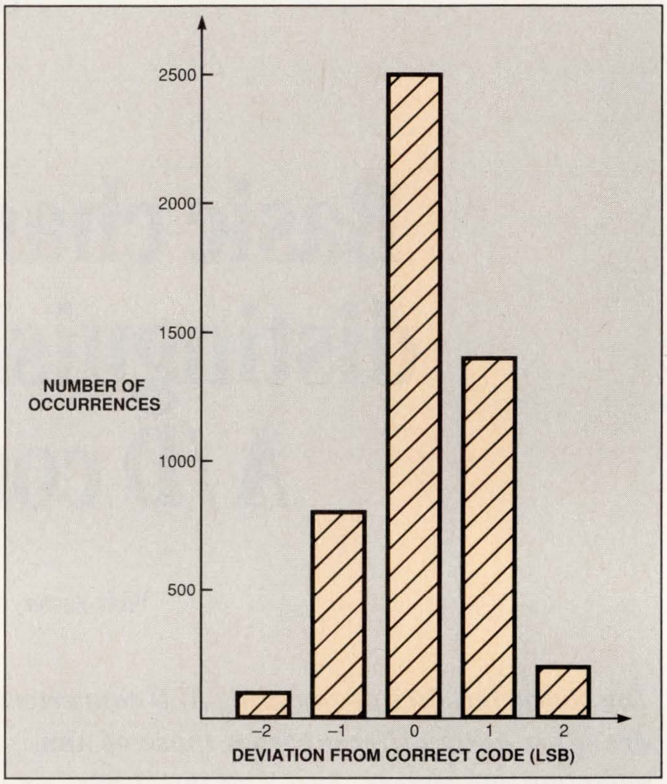

Fig 1—Because of inherent circuit noise in wideband high-resolution ADCs, a range of output codes may occur for a given input voltage. This histogram shows the distribution of codes relative to the correct code for 5000 conversions using the AD7884, a 16-bit 166-ksample/sec ADC. Fitting a Gaussian probability distribution to the histogram yields a standard deviation approximately equivalent to the input rms noise voltage.

By increasing the sampling rate to $2f_S$ (2× oversampling) and inserting a digital filter having a cutoff frequency of $f_S/2$ following the ADC, you can remove the noise between $f_S/2$ and f_S. This arrangement, which improves the ADC's signal-to-noise (S/N) ratio by 3 dB, is a fundamental concept in sigma-delta ADCs that use noise-shaping to achieve extremely high resolutions with single-bit quantizers.

Key ac performance characteristics

Although sampling ADCs can usually handle ac input signals as high as the Nyquist frequency, all will exhibit some degraded dynamic performance as you increase the input-signal slew rate. For higher-frequency inputs (usually those greater than the Nyquist frequency), linearity tends to degrade and bandwidth rolls off. Aperture jitter and other errors associated with timing also contribute to this degradation. The most common method for quantifying these dynamic errors is applying a pure sine-wave signal to the ADC and performing an FFT on the output data. This test yields a spectral output from which you can calculate the S/N ratio, harmonic distortion, S/N ratio including distortion (S/(N+D), total harmonic distortion (THD), and bandwidth.

A perfect n-bit ADC with no errors will yield a theoretical quantization noise of $q/\sqrt{12}$, where q is the weight of the LSB. This relationship leads to the well-known equation for theoretical full-scale rms sine-wave signal-to-noise-plus-distortion level of S/(N+D) = 6.02n + 1.76 dB, where n is the bit resolution. An actual ADC, however, will yield a measured S/(N+D) less than the theoretical value. Solving this equation for n using the measured S/(N+D) value yields the equation for the effective number of bits (ENOB):

$$\mathrm{ENOB} = \frac{\left[\mathrm{S}/(\mathrm{N}+\mathrm{D})\right]_{\mathrm{ACTUAL}} - 1.76\,\mathrm{dB}}{6.02}.$$

Fig 2 shows S/(N+D) as a function of input frequency for the AD676 16-bit, 100-ksample/sec ADC. Notice that, for a full-scale input, the ADC maintains an S/(N+D) of 88 dB (14.3 ENOB) up to an input frequency of approximately 60 kHz. The ENOB equation applies only for a full-scale input signal. In many cases, signals are less than full scale, especially at higher frequencies. **Fig 2** also shows the S/(N+D) for signals at −20 dB and −60 dB. You can calculate the effective number of bits for these less-than-full-scale signals by adding the appropriate correction factor:

$$\mathrm{ENOB} = \frac{\left[\mathrm{S}/(\mathrm{N}+\mathrm{D})\right]_{\mathrm{ACTUAL}} - 1.76\,\mathrm{dB} + \text{level of input below full scale}}{6.02}.$$

For example, for a 1-MHz, −20-dB input signal, the actual S/(N+D) is 54 dB. Using the above formula, this corresponds to an ENOB of approximately (54 − 1.76 + 20)/6.02, or 12.

Another important ac specification is the full-power bandwidth. Somewhat analogous to that of an op amp, the full-power bandwidth of an ADC is the frequency at which the fundamental component in the FFT output is down 3 dB for a full-scale input. The AD676 has a full-power bandwidth of 1 MHz, but because of the large level of harmonic distortion, it has a S/(N+D) of 40 dB (6.4 ENOB) for a full-scale 1-MHz input signal. For this reason, you should always consider the full-power bandwidth in conjunction with the S/(N+D) and ENOB values to determine whether the converter has sufficient dynamic performance at the full-power-bandwidth frequency.

In addition to ac and dc characteristics, sampling ADCs have other traits you should be aware of. Just because a sampling ADC has a sample-and-hold function doesn't mean that the analog input is benign and well behaved. Different ADC architectures present different loads to the drive amplifier. During conversion, many sampling ADCs inject transient load currents into the output of the drive amplifier. These currents develop corresponding voltages across the closed-loop output impedance of the drive amplifier. Such transient voltages must settle to the required accuracy before correct conversions are possible.

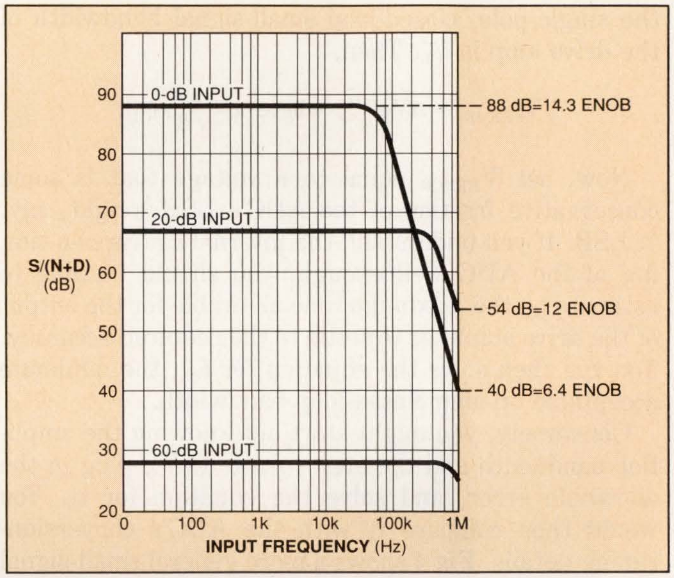

Fig 2—This plot for the 16-bit, 100-ksample/sec AD676 shows the S/(N+D) (S/N ratio including distortion) and the ENOB (the effective number of bits) as a function of frequency. Note that, for a full-scale (0 dB) input, the ADC maintains a 14.3 ENOB to an input frequency of approximately 60 kHz.

Consider the simple model of a classical closed-loop S/H circuit in **Fig 3**. When switching from sample to hold, or vice versa, assume that the circuit develops a 1V step voltage (ΔV) across the clamping diodes. This step voltage produces a corresponding high-frequency transient load current of about 0.3 mA to the output of the ADC drive amplifier. If you know the rise time (t_R) of the step voltage, you can calculate the corresponding signal bandwidth using the approximation, bandwidth = $0.35/t_R$.

You next estimate the closed-loop output impedance of the drive amplifier at this frequency using the manufacturer's data-sheet information. Because of the inductive nature of the op amp's emitter-follower outputs, the closed-loop output impedance of the drive amplifier (Z_O) could easily be 100Ω at 100 MHz. This impedance would develop an error voltage (V_{ERROR}) of 30 mV. This small error voltage is not large enough to cause the amplifier to become nonlinear, so you can use a simple first-order exponential-decay model to calculate the error voltage as a function of time t. Assume that the single-pole, closed-loop small-signal bandwidth of the drive amp is f_{CL}. Then,

$$V_{ERROR}{}^{t} \approx \Delta V e^{-t/\tau}, \text{ where } \tau = \frac{1}{2}\pi f_{CL}.$$

Now, set V_{ERROR} equal to a voltage that is some conservative fraction of the ADC's LSB weight, say, ¼ LSB. If you understand the internal conversion timing of the ADC well enough, you should be able to estimate t_S, the maximum time allowable for the output of the drive amplifier to settle to the required accuracy. You can then solve the equation for f_{CL}, the minimum acceptable op-amp closed-loop bandwidth.

Conversely, you might start out knowing the amplifier bandwidth and the step voltage (ΔV), plug in the allowable error, and solve the equation for t_S. You would then compare t_S with the ADC's conversion-timing details. **Fig 4** shows a more general small-signal model, which you can use for any amplifier subjected to transient load currents.

Transient load currents are very much a function of the ADC's architecture. For example, ADCs that use charge-redistribution techniques sequentially switch the analog input through several states, as **Fig 5** shows. During the coarse-charge interval, the input drives the storage capacitor through a low-accuracy internal buffer amplifier. During the fine-charge interval, the analog input switches to connect directly to the storage capacitor. Finally, the analog input disconnects from the storage capacitor, and the internal conversion takes place. Each time the analog input switches between modes, transient currents are injected into the ADC's analog input.

At this point you might well ask why manufacturers don't include on all ADC chips an input buffer amplifier that would make the analog inputs truly benign. The answer is that in many cases the manufacturing process the ADC manufacturer uses can't produce a buffer that must have not only precision dc performance, but also low noise, low distortion, and high bandwidth. Although the ultimate goal is to create ADCs with high-impedance, glitch-free inputs, the reality is that many precision sampling converters place transient load requirements on the drive amplifier.

You should also be aware that ADCs having switched-capacitor inputs, such as the AD1879 18-bit, sigma-delta stereo audio ADC in **Fig 6,** may generate signal-dependent transient load currents. This signal dependence is the result of the nonlinear nature of the capacitance associated with the CMOS switches in the differential sigma-delta modulators.

The **Fig 6** circuit can properly drive the differential inputs of the AD1879 at THD levels exceeding −100 dB. The differentially connected 0.0047-μF capacitor

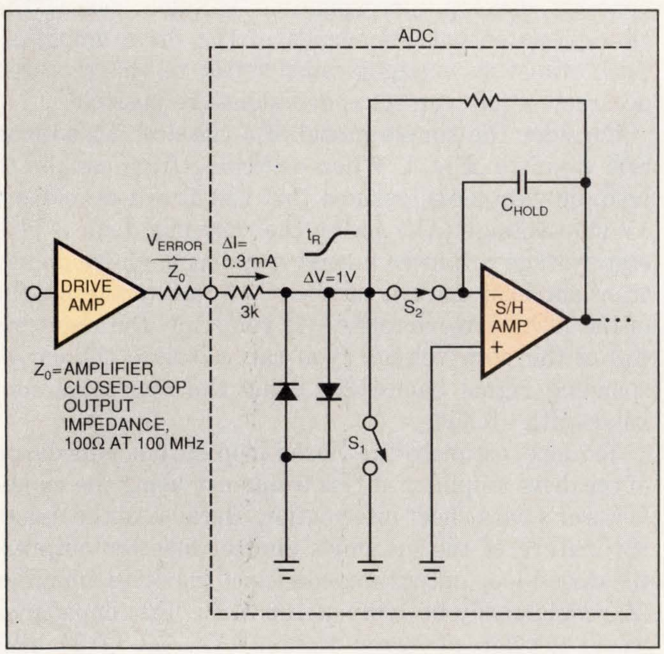

Fig 3—This diagram of a closed-loop S/H circuit illustrates how a sampling ADC generates transient load currents. A 1V step voltage across the clamp diodes generates a load current of approximately 0.3 mA to the output of the ADC's drive amplifier.

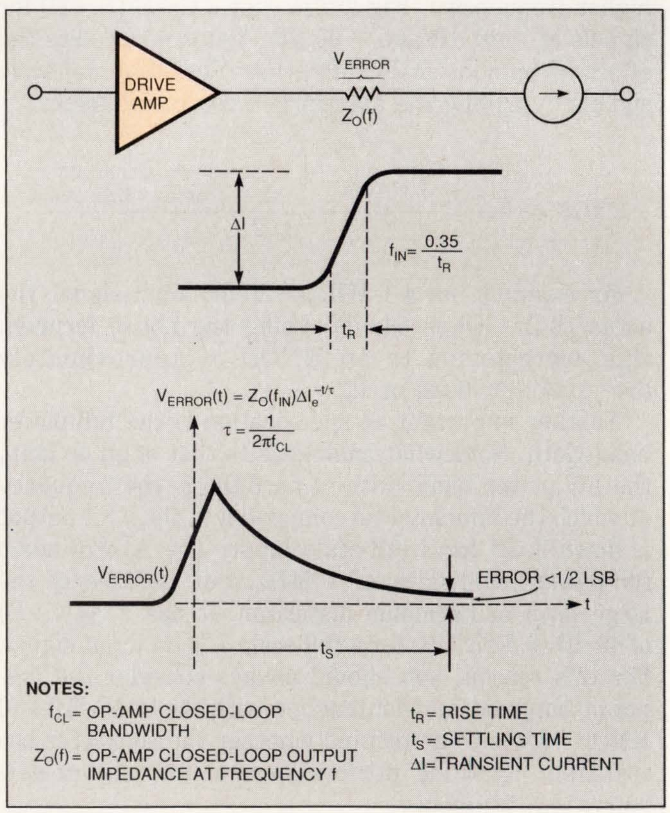

Fig 4—You can use this general small-signal model to estimate the drive amplifier's settling time as a function of the transient load current.

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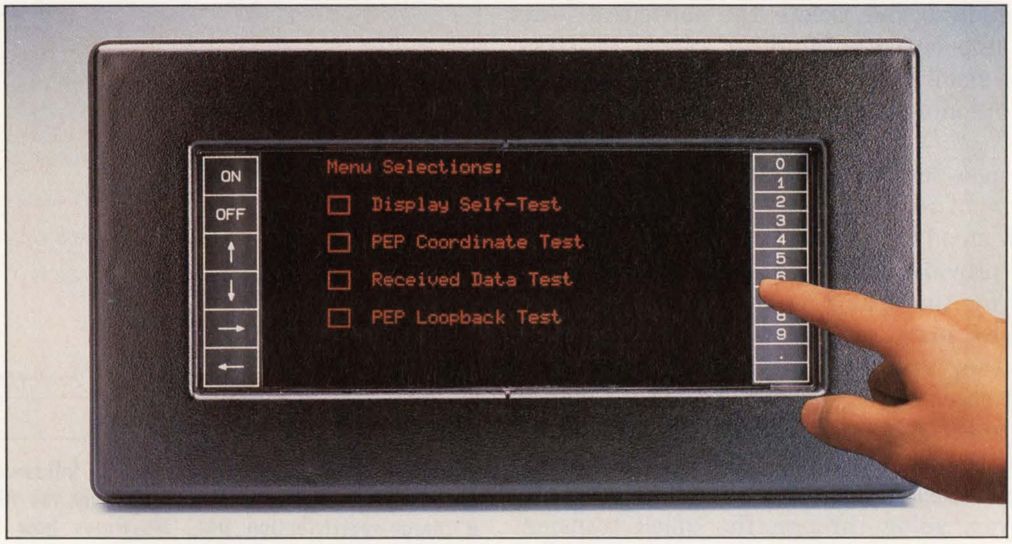

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supplies most of the differential-mode transient currents; the 0.01-µF capacitors connected to ground absorb common-mode spike currents. The 51Ω series resistors isolate the remaining transient currents from the drive amplifiers and isolate the capacitive loads from the op-amp outputs. However, these resistors' value must be small to avoid distortion resulting from the signal-dependent transients charge injection causes.

These examples serve to illustrate the fact that most ADC analog-input impedances are quite complex and comprise both steady-state and transient components. Rather than provide detailed amplitude and timing specifications for the analog-input transient load currents, most ADC manufacturers recommend drive amplifiers that they know work with their particular ADC. In most cases, if you select an amplifier properly with respect to the ADC's signal bandwidth and THD requirements, the settling time will be short enough to handle the transient load currents the ADC produces. However, going through the quick transient analysis described previously is a good idea, especially if you're using an amplifier the ADC manufacturer did not recommend.

Most ADCs will tolerate moderate out-of-range signals without damage to the input circuit. However, you might want to clamp the ADC input so that the signal is limited to small over-range values. This step is especially smart if you expect large out-of-range

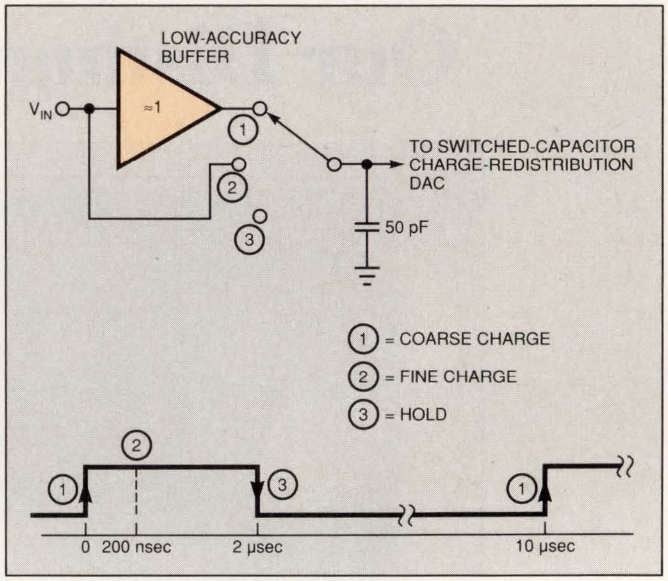

Fig 5—An ADC's architecture greatly influences transient load currents. This equivalent input circuit for the AD676, which uses a charge-redistribution DAC, illustrates how the analog input switches through several states.

transient signals to be routine. Clamping not only protects the ADC input but is also likely to reduce the time required for the ADC to recover from an overvoltage condition.

In the **Fig 7** circuit, low-capacitance Schottky diodes perform the clamping. The value of series resistor R_S

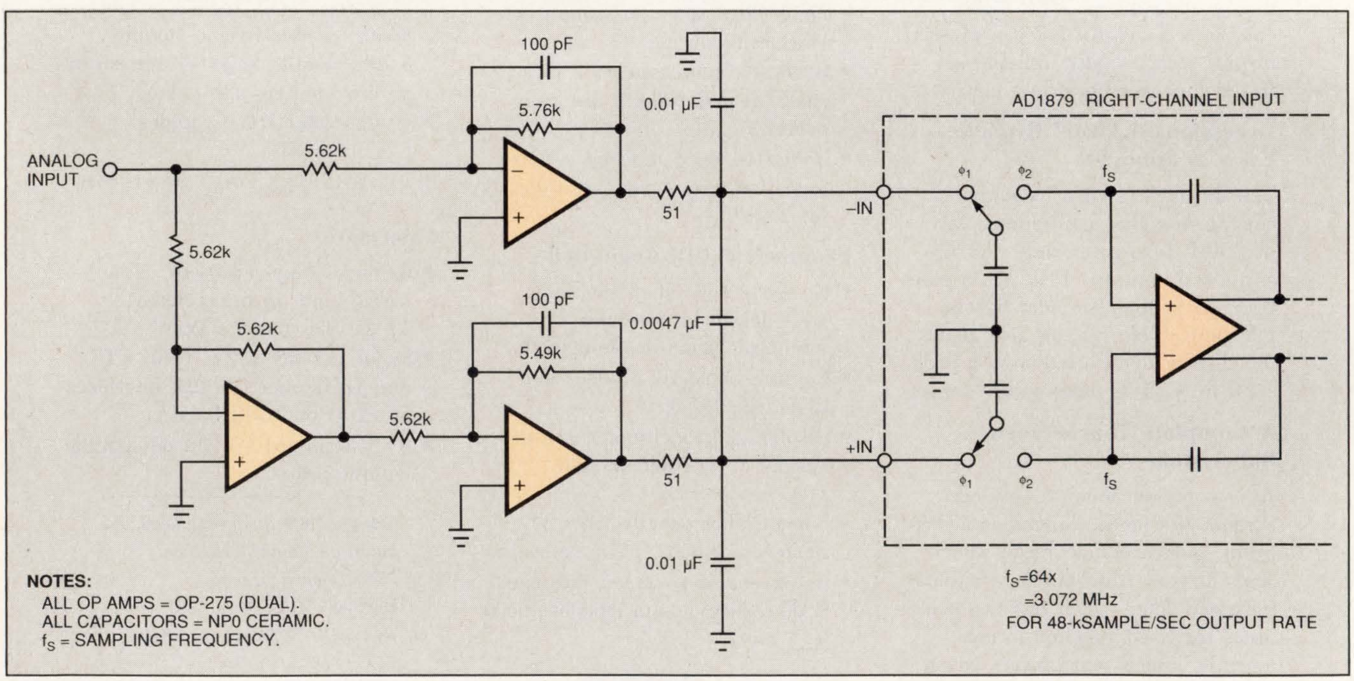

Fig 6—ADCs with switched-capacitor inputs, such as this 18-bit sigma-delta converter, can generate signal-dependent transient load currents. This signal dependence primarily results from the nonlinear nature of the capacitance associated with the CMOS switches, which are in the differential sigma-delta modulators.

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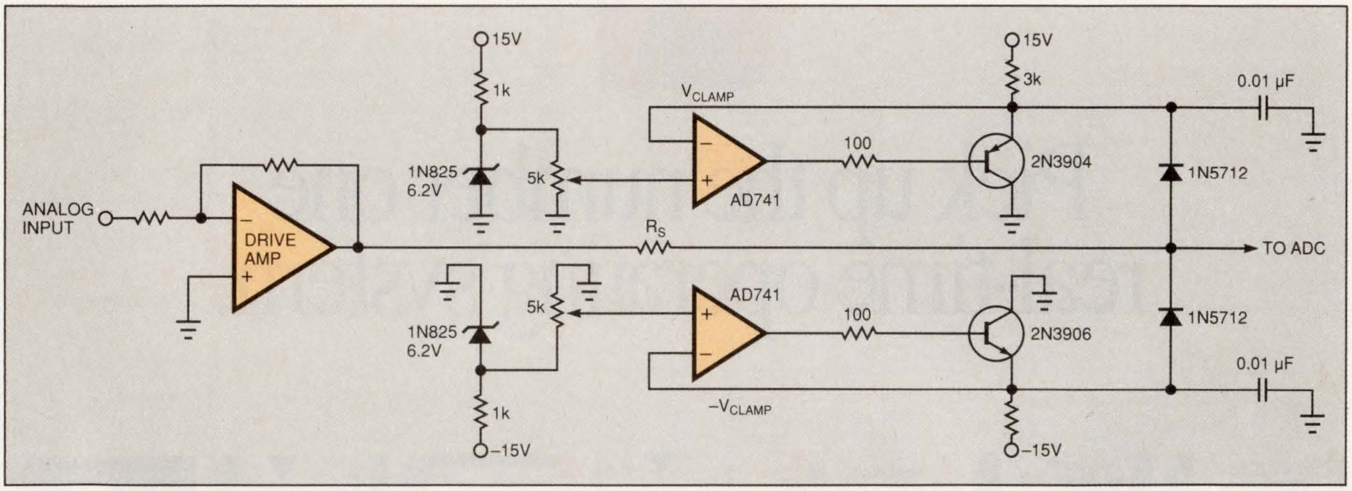

Fig 7—This circuit uses low-capacitance Schottky diodes to provide both positive and negative adjustable clamping. Such circuits protect the input of an ADC by limiting large out-of-range signals. An additional benefit is the reduction in the time an ADC needs to recover from an overvoltage condition.

should be only large enough to limit the op-amp output current. Larger values may limit bandwidth and cause distortion products because of the impedance nonlinearities of the ADC input.

Some op amps have an external-compensation pin connected to the internal high-impedance node in the op amp immediately preceding the output-buffer stage. Although normally meant for externally compensating the frequency response, you can use this pin as a connection point for the diode clamping circuit. This approach eliminates the need for an external current-limiting resistor but may introduce distortion because of the high-impedance node's sensitivity to the diode's nonlinear capacitance. The compensation pins on some op amps are not connected to a point in the circuit suitable for clamping, so always check the data-sheet schematic diagram before proceeding with this approach.

Other conditions of temporary overvoltage may occur because of power-supply sequencing. For instance, if an op amp powered by ±15V supplies drives an ADC powered by ±5V supplies, the ADC may be damaged if the op amp supplies turn on first. Also, some CMOS ADCs may go into latch-up if the analog input voltage exceeds the ADC supply voltage. One common way to prevent these problems is to connect diodes between the analog input of the ADC and each ADC supply voltage. Manufacturers often design these diodes into ADC chips.

Another preventative measure is selecting an amplifier that will operate from ±5V supplies and powering both the op amp and the ADC from the same supplies. In fact, many recently introduced op amps are specified for both ±15 and ±5V operation. Unfortunately, their output-voltage swing when operating from ±5V supplies may not be sufficient to drive the input of the ADC. A more realistic alternative is to use a ±15V op amp and derive the ±5V for the ADC from the ±15V supply using standard 3-terminal regulators. This scheme is fairly efficient when using CMOS ADCs because of their relatively low power dissipation. Moreover, such a scheme has the advantage of isolating the ADC from noise that may exist on the ±5V supplies if the supplies also power digital circuits.

Regardless of the ADC, you should strictly observe the absolute maximum supply-voltage ratings on the data sheet to prevent damage or latch-up. EDN

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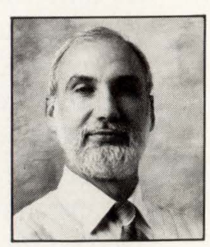
Author's biography



Walt Kester is a corporate staff applications engineer with Analog Devices and has been with the company for 23 years. His principal responsibility is applications support for linear and converter products. A member of IEEE, Walt has a BSEE from North Carolina State University (Raleigh, NC) and a MSEE from Duke University (Durham, NC). In his leisure time, Walt enjoys travel and carpentry.

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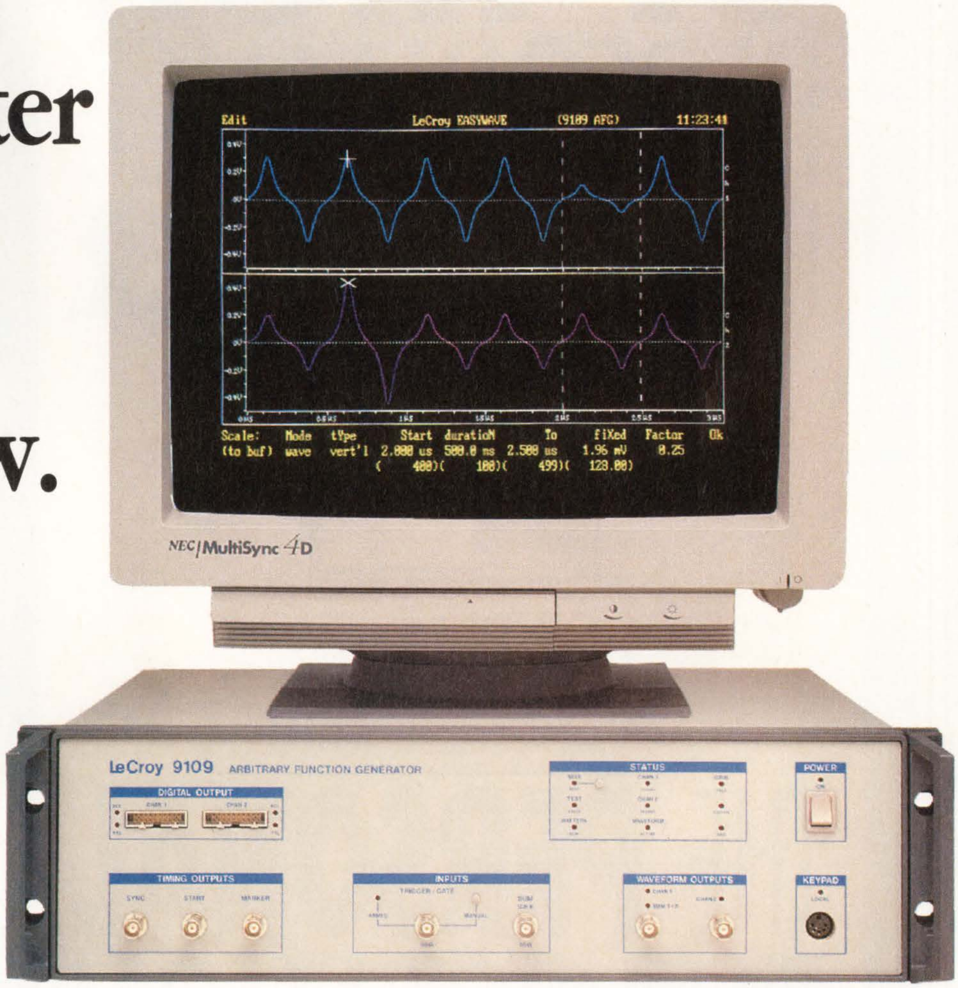

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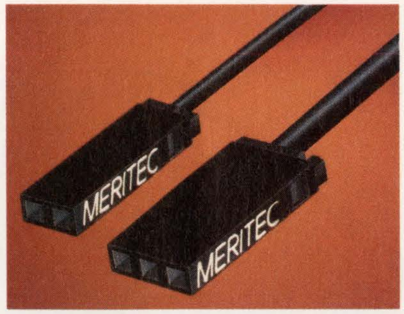

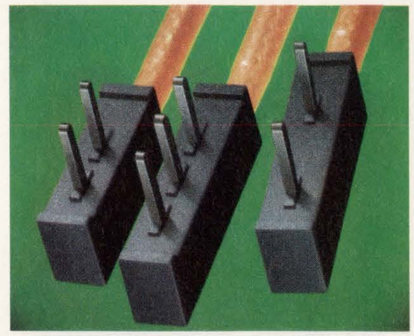

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Series resonators widen FM demodulation

Tom Hajjar, Hajjar & Associates Inc, Satellite Beach, FL

A pair of series resonators (**Fig 1**) allows the CA3189 FM audio demodulator to handle wideband FM and still achieve low distortion. The recommended tuned-LC circuit for the chip's quadrature detector is either a simple single-tuned tank circuit or a double-tuned circuit teamed with a quad coil. Both standard circuits require variable inductors or tuned IF transformers.

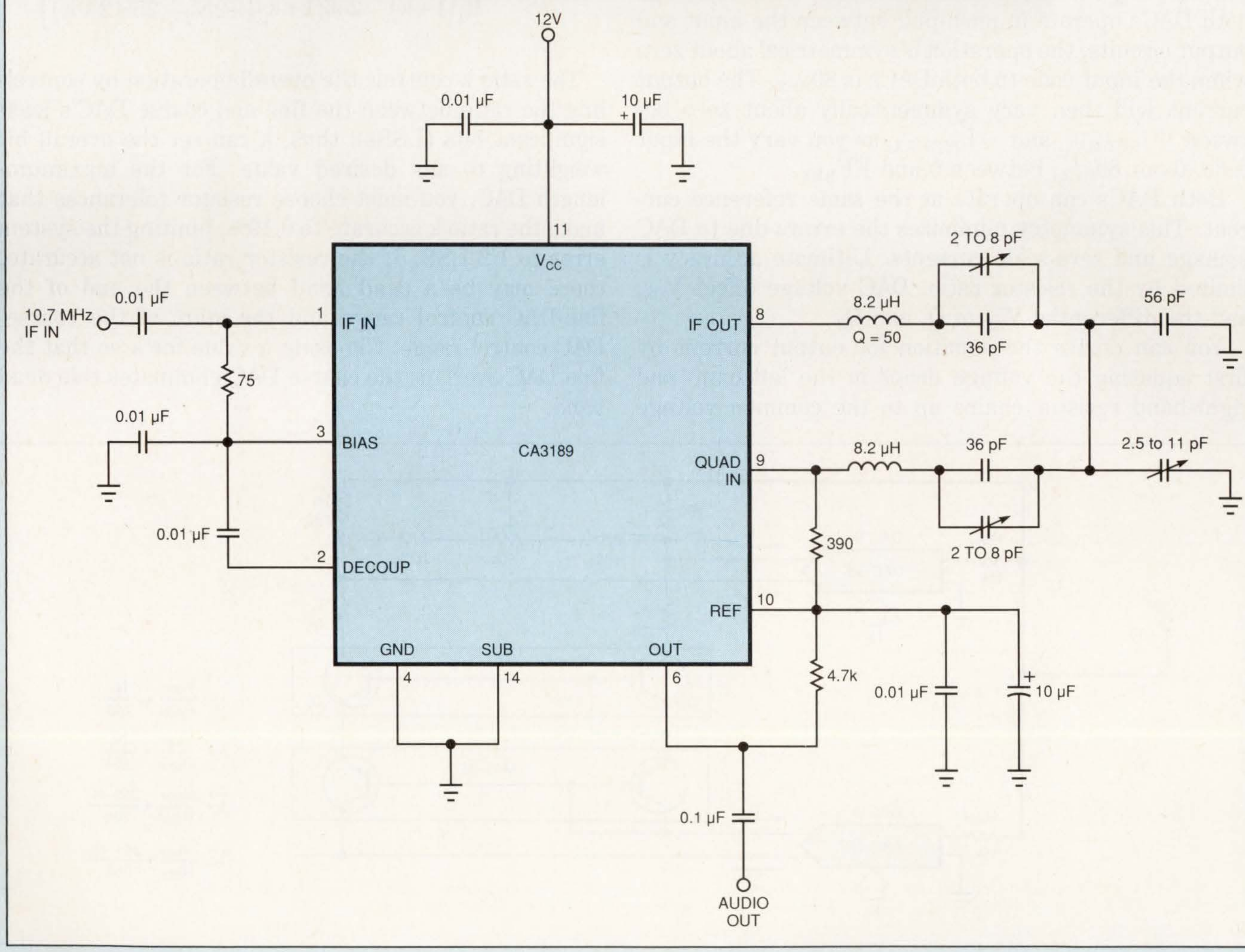
The premise that linear phase means flat group delay leads to the filter in **Fig 1**. The filter is the dual of a top L-coupled, 2-resonator bandpass filter. The series resonators are weakly coupled for a Bessel-like response, achieving a flat group delay. The filter also has a 90° phase shift at its center frequency, which eliminates the quad coil.

You can design similar filters for most FM demodulators by first using standard filter tables for top C-coupled parallel-resonator bandpass filters. Then change the capacitive coupling to inductive coupling, making the appropriate component changes. Finally, using duality, convert the filter to the topology in the **figure**.

The values in **Fig 1** demodulate a 10.7-MHz signal having 450-kHz peak deviation. The filter has a 390Ω impedance, which matches the chip's.

EDN BBS /DI_SIG #1169

To Vote For This Design, Circle No. 746



High-resolution DAC uses coarse/fine control

Terence S Finnegan, Carlisle, UK

The circuit in **Fig 1** is a high-resolution DAC that provides symmetrical bipolar output current. The resolution can extend to 21 bits with the appropriate components. The design uses two DACs that operate from a common reference in a simple coarse/fine control arrangement. The circuit resistively divides the output current from the fine DAC and then adds this current to the coarse DAC. The circuit's accuracy and resolution are therefore controlled by passive resistors and are independent of the active elements.

The two DACs provide the coarse and fine control through a 4-transistor Wilson current mirror. DAC A provides the coarse control, and its current mirrors connect directly to the output. DAC B provides fine control, and this DAC's output current affects the output only by the resistor ratio $R_1/(R_1+R_2)$. Because both DACs operate in push-pull between the input and output circuits, the operation is symmetrical about zero when the input code to both DACs is 80_{HEX}. The output current will then vary symmetrically about zero between $+I_{OUT(MAX)}$ and $-I_{OUT(MAX)}$ as you vary the input code about 80_{HEX}, between 0 and FF_{HEX}.

Both DACs can operate at the same reference current. This symmetry minimizes the errors due to DAC leakage and zero-scale currents. Ultimate accuracy is limited by the resistor ratio, DAC voltage offset V_{OS}, and the differential V_{BE} of Q_1 and Q_2.

You can derive the equation for output current by first equating the voltage drops in the left-hand and right-hand resistor chains up to the common voltage point, V_C. Substituting the right-hand side of the equations shown in **Fig 1** for I_1, $\overline{I_1}$, I_2, and $\overline{I_2}$, yields the equation

$$I_{OUT} = V_{OS} + \frac{I_{REF}}{256}\left[\begin{array}{l} N_1(R_1+R_2+R_3+R_4) \\ +N_2(R_1+R_3) - 255(2R_3+R_4) \end{array}\right],$$

where N_1 and N_2 are the decimal input codes for the coarse and fine DACs. If you let $R_3 = R_1$, $R_4 = R_2$, and set $R_2/R_1 = k$ and $V_{REF}/R_{REF} = I_{REF}$, the expression becomes

$$I_{OUT} = \frac{V_{OS}}{R_1(1+k)} + \frac{I_{REF}}{256(1+k)}\left[\begin{array}{l} 2N_1(1+k) \\ +2N_2 - 255(2+k) \end{array}\right].$$

The ratio k controls the overall operation by controlling the ratio between the fine and coarse DAC's least significant bits (LSBs); thus, k can set the overall bit weighting to any desired value. For the maximum-length DAC, you must choose resistor tolerances that make the ratio k accurate to 0.19%, limiting the system error to 1/2 LSB. If the resistor ratio is not accurate, there may be a dead band between the end of the fine-DAC control range and the start of the coarse-DAC control range. Choosing a value for k so that the fine DAC overlaps the coarse DAC eliminates this dead band.

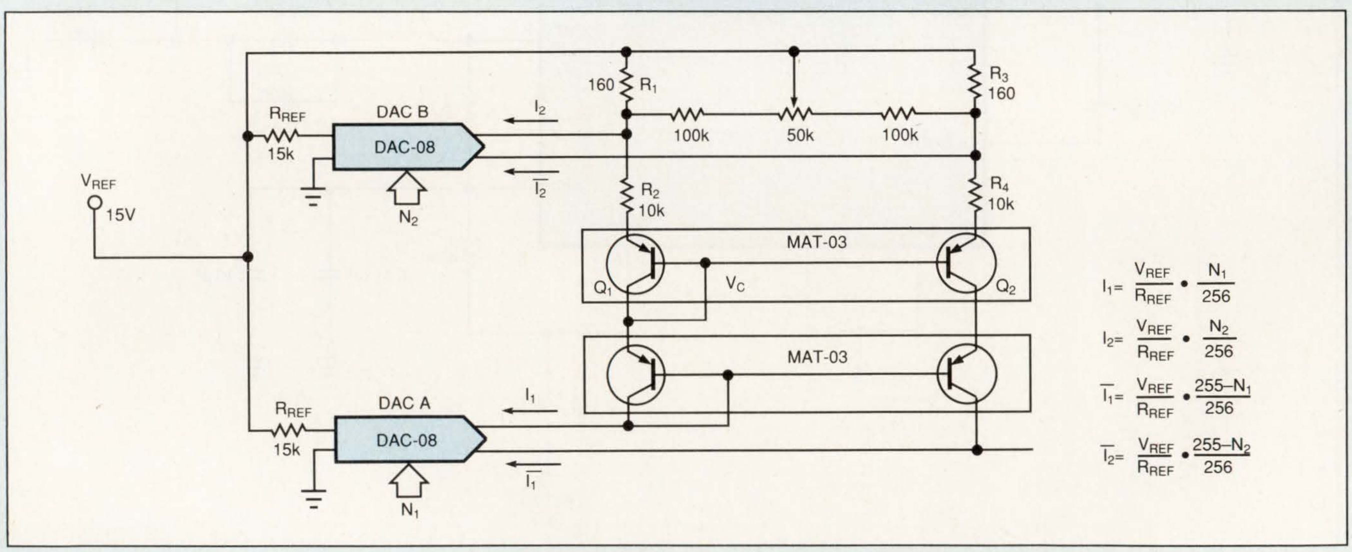


Fig 1—DACs A and B provide coarse and fine control through a Wilson current mirror to implement an overall DAC with 14 bits of resolution. The design's maximum possible resolution is 21 bits.

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For instance, setting k to 126.49 makes the combined system act like a bipolar 15-bit DAC with a total range of 32,765 bits. The fine DAC overlaps the coarse DAC by 1 bit, allowing the use of less accurate resistors and ensuring that the circuit generates all output states without any missing codes. You can set other ranges and overlaps as you like by choosing k appropriately. **Fig 1** implements a 14-bit DAC with k = 62.25.

If you need more resolution, you can expand this circuit to include combinations for 8- and 12-bit DACs, which will increase the control range.

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To Vote For This Design, Circle No. 747

Servo loop controls oscillator amplitude

Thomas P Hack, Comlinear Corp, Fort Collins, CO

The high-performance, fundamental-mode crystal oscillator in **Fig 1** uses an AGC amplifier and a crystal to form a very-narrow-band filter at the crystal's series-resonant frequency. The design exhibits reasonably low phase noise and jitter because it places the crystal between two low-impedance points of the CLC520 AGC amplifier (IC_1). The oscillator can drive a 50Ω load easily and has a well-controlled output impedance. The design exhibits low distortion and is adaptable to a variety of fundamental-mode crystals.

Unlike most oscillators, which use limiting to set the amplitude, this design uses a servo loop to control amplitude. D_1 and C_1 are the key components of a clamping circuit that produces an average voltage proportional to the peak-to-peak oscillator amplitude. The larger the amplitude, the more positive the dc component.

The design configures an LF356 (IC_2) as an integrator that compares the dc signal against the reference voltage of D_2. If the oscillator's amplitude is too high, the integrator's output voltage drops, as does IC_1's gain and the oscillator's loop gain. When the loop gain drops below unity, the oscillator output amplitude begins to drop until it reaches the loop's desired amplitude. If the amplitude is too low, the integrator output voltage increases, thereby increasing the loop gain and increasing the amplitude to the loop's desired value.

When the oscillator amplitude is stable, the average current flowing into the integrator capacitor (C_2) is zero. The average current through R_3 is equal in magnitude and opposite in sign to the current flowing

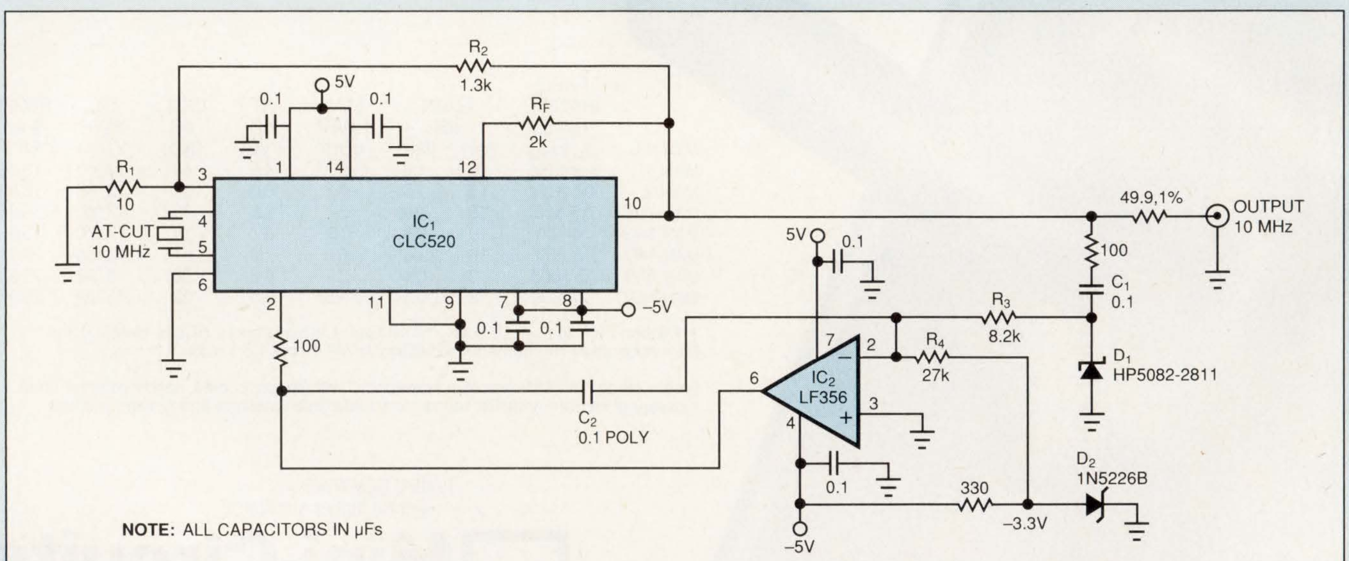


Fig 1—Unlike most oscillators, which use limiting to set the amplitude, this 10-MHz oscillator uses a servo loop to control amplitude. Six steps are necessary to tailor the design to your requirements.

through R_4 (assuming that IC_2's bias currents are negligible). And the oscillator loop gain is exactly equal to one. Because a leveling loop, and not circuit limiting, sets this oscillator design's amplitude, distortion is low. The amount of distortion is mostly set by IC_1. Because IC_1's bandwidth (typically 140 MHz for large signals) is approximately four to five times higher than the highest oscillation frequency of most fundamental-mode AT-cut crystals, the effect of IC_1's bandwidth is negligible.

Designing this oscillator requires six major steps. The first step is to determine the range of the crystal's equivalent series resistance. You should use a range consistent with the distribution of crystals that you use. If you'll be tuning the range, find the equivalent resistance of the crystal combined with the tuning network at the new series-resonant frequency. In the case of a crystal and a tuning capacitor in series, the highest overall series resistance exists at the lowest tuning capacitance and highest crystal series resistance.

The second step is to choose the output amplitude. To determine the output voltage at pin 10 of IC_1, first convert from dBm to watts as follows:

$$P_{OUT} = 10^{(0.1\,dBm-3)},$$

where P_{OUT} is the power delivered to the load in watts, and dBm is the power delivered to the load in dBm. The rms voltage delivered to the load is

$$V_{OL} = (R_{LOAD} \times P_{out})^{0.5}.$$

To account for a doubly terminated load, use the following equation:

$$V_{OP\ AMP} = 2 \times V_{OL} = (4R_{LOAD} \times P_{out})^{0.5},$$

where V_{OP} is in volts rms.

The third step is to select the crystal drive level. Drive levels should lie between 1 and 20 μW for good long-term stability and between 100 and 500 μW for good short-term stability. Because the equivalent series resistance of the crystal affects the drive level, be sure that the drive level is reasonable for all expected values of this resistance. One way to start is to choose the maximum crystal drive level (D_{MAX}) and see if the minimum drive level is acceptable using the following equation:

$$D_{MIN} = D_{MAX}\left(\frac{R_{S(MAX)}}{R_{S(MIN)}}\right)\left[\frac{R_{S(MIN)}+3}{R_{S(MAX)}+3}\right]^2,$$

where $R_{S(MAX)}$ and $R_{S(MIN)}$ are the maximum and minimum series resistances, respectively. If this calculated value of D_{MIN} is acceptable, you need to determine whether or not IC_1 can deliver D_{MAX}. IC_1 will be most limited at the minimum series resistance, as follows:

$$D_{LIMIT} = (0.9113 \times 10^{-6})R_{S(MIN)},$$

where D_{LIMIT} is the maximum drive available from IC_1 in watts, and $R_{S(MIN)}$ is the minimum crystal series resistance in ohms. If D_{LIMIT} is greater than D_{MAX}, IC_1 can deliver the targeted maximum drive level. If not, substitute D_{LIMIT} in place of D_{MAX} in **Eq 4** to determine the lowest drive that will occur. D_{LIMIT} and the new D_{MIN} set the new drive-level range.

The fourth step is setting the forward gain of the oscillator. First determine the input voltage to IC_1's pin 3 at the maximum series resistance as follows, with D_{MIN} in watts and V_{IN} in volts rms:

$$V_{IN} = (R_{S(MAX)}+3)\left(\frac{D_{MIN}}{R_{S(MAX)}}\right)^{0.5}.$$

This equation accounts for the crystal's loading of IC_1's buffers (pins 4 and 5). You can now determine the voltage gain of IC_1 at the highest series resistance and highest gain-control voltage (A_V) as follows:

$$A_V = \frac{V_{OP\ AMP}}{V_{IN}}.$$

To achieve this gain, set R_F as follows:

$$R_F = \frac{A_V(R_{S(MAX)}+3)}{1.85}.$$

In general, the value of R_F should be between 1 and 2 kΩ. Somewhat higher values are acceptable if the oscillator is running below 10 MHz. If R_F needs to be lower than 1 kΩ, refer to IC_1's data sheet for the output-amplifier loop-gain reduction techniques.

Fifth, you need to calculate the values of the feedback network comprising R_1 and R_2. To keep the noise low at IC_1's input and provide reasonable resistor values, you should make $R_1 \geq 10\Omega$ and ≤ 1 kΩ. You should set the loss in the network equal to $B = 1/A_V$, which means that

$$R_2 = R_1(A_V - 1).$$

The sixth and final step requires setting up the level-

ing loop. The average voltage from the clamping circuit is as follows, where V_{PK} is the peak output voltage of IC_1, and V_D is the forward voltage drop for D_1:

$$V_{DC} = V_{PK} - V_D = 1.414V_{OP\ AMP} - V_D.$$

Once the amplitude of the oscillator is stable, the current flowing through R_3 and R_4 must cancel at C_2. For this condition to be met,

$$R_4 = R_3\left(\frac{V_{D2}}{V_{DC}}\right),$$

where V_{D2} is the zener voltage of D_2. To ensure the stability of the amplitude-control loop, make C_2 equal to $0.01 \times F$, where C_2 is in µF and F is in MHz.

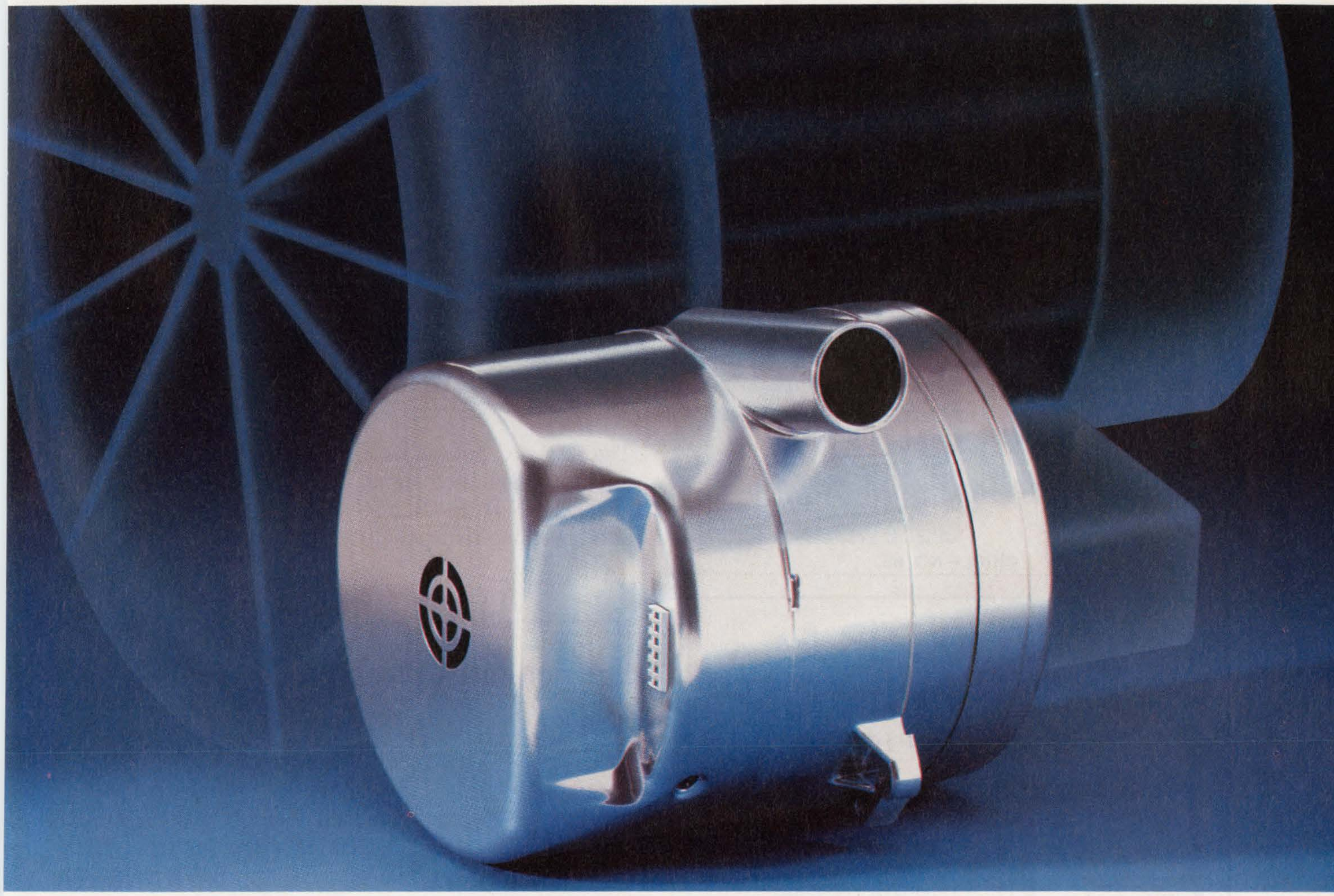
For the values in **Fig 1**'s design, the results of the six steps are as follows:

1. The crystal has a measured equivalent series resistance of approximately 7.3Ω. The range of R_S is 5 to 25Ω.
2. The design's output-power requirement is 7 dBm into 50Ω so that the oscillator can drive a double-balanced mixer directly. This requirement translates into an output voltage at the op amp of approximately 1V rms.
3. For a 5Ω minimum equivalent series resistance, IC_1 limits crystal drive level to 4.56 µW. At R_S of 25Ω, the drive level falls to 1.86 µW. These numbers produce good long-term stability.
4. The input voltage at IC_1's pin 3 is 7.64 mV rms. The voltage gain is 131. Thus, R_F must equal 1.98 kΩ (use 2 kΩ).
5. R_1 is set to 10Ω. Thus, R_2 must equal 1.301 kΩ.
6. Assuming a forward drop of 0.4V for D_1 yields approximately 1V dc from the clamping circuit. R_3 must then be approximately 8.3 kΩ (use 8.2 kΩ). C_1 is set to 0.1 µF because this design is for a 10-MHz oscillator.

EDN BBS /DI_SIG #1154 EDN

To Vote For This Design, Circle No. 748

Here's technology that delivers regenerative blower performance in a fraction of the space



High air flows, high pressure capability and variable speed in a compact package

Just 5.7″ (145 mm) in diameter by 5.2 to 7.2″ (132 to 183 mm) long, these Windjammer® blowers combine brushless motor drives that provide high speed, high torque and controllability with high performance fan systems. They're much smaller, weigh only 10% as much and are 25% more efficient than a regenerative blower with comparable performance. The result is a compact, cost-effective blower for demanding applications such as medical equipment, business machines and materials handling.

Application matched performance

Windjammer blowers are available with 1-, 2- or 3-stage fan systems. These blowers can be optimized for high air flow

of up to 125 cfm (212 m^3/hr) free flow or high pressure/vacuum capability of up to 75″ H_2O (185 mbar) sealed.

Models for worldwide AC operation

These Windjammers feature integral power conversion with models available for operation from any standard AC input power. With one version, a 0 to 10 VDC signal from a sensor or other device will control motor speed and adjust air performance from 0 to 100%. Or, a second model provides manual speed control by means of a potentiometer located in the blower housing.

Windjammer blowers are UL component recognized, CSA and TÜV certified. AMETEK, Technical Motor Division, 627 Lake Street, Kent, OH 44240. Tel: 216-673-3452. Fax: 216-678-8227. In Europe, Friedrichstrasse 24, D6200 Wiesbaden, Germany. Tel: 0611-370031. Fax: 0611-370033.

AMETEK
TECHNICAL MOTOR DIVISION

CIRCLE NO. 61

Software Shorts

Korn-shell functions enable directory stack

John Fenwick, Hewlett-Packard Co
Cupertino, CA

The Korn-shell functions in **EDN BBS /DI_SIG #1145** define push, pop, and display operations for a directory stack, bringing handy functions of older shells to the more modern Korn shell.

To Vote For This Design, Circle No. 670

PAL generates 8031 fetch signal

Predrag Kezele and Milan Radovanovic,
Lola Institute, Beograd, Yugoslavia

The 8031 μC generates no external signal to indicate an instruction-fetch signal. The complete design package in **EDN BBS /DI_SIG #1057** details a PLD-based state machine that generates the signal.

To Vote For This Design, Circle No. 671

Program locks checksum in EPROM

Raymond D Kade and Preyas S Shah, Ametek
Sellersville, PA

The Qbasic program attached to **EDN BBS /DI_SIG #1178** accepts a 27256 EPROM's file (in Intel HEX format) and generates a new file that has a checksum appended. The checksum will match checksums generated by standard EPROM programmers.

To Vote For This Design, Circle No. 672

Program finds parallel resistors quickly

John Dunn
Merrick, NY

The GWbasic program in message **EDN BBS /DI_SIG #1179** finds resistor combinations quickly by restricting the possible values it tries. You specify the parallel or total resistance, and the program finds what combinations of standard resistors will produce it.

To Vote For This Design, Circle No. 673

LINEAR TECHNOLOGY DESIGN NOTES

No Design Offline Power Supply – Design Note 62

Anthony Bonte and Ron Vinsant

Offline Switcher Eliminates Optocoupler Feedback. Low Cost, Simple, 50W, Universal Input Power Supply.

Linear Technology has broken through the "buy-vs-build" barrier for offline power supplies. The new LT1105[1] current-mode PWM control IC is used to make a simple, triple output power supply (Figure1). The circuit features low cost, high reliability and customizable footprint. It accepts a universal input of 85VAC-270VAC while providing isolated and regulated output voltages of 5V at 5A, 12V at 1.5A and –12V at 0.5A. MTBF is calculated at >100k hours for full load at 25°C ambient. The power supply contains all necessary components including an input EMI filter. All outputs have continuous short-circuit protection. Figure 2 indicates 5V load regulation performance as a function of input line voltage.

The LT1105 eliminates optocoupler feedback by regulating the flyback voltage of the bootstrap bias winding. This reduces the number of components crossing the isolation barrier to one: the transformer. The transformer is designed to meet international safety standards and is subject to a set of compromises involving efficiency, maximum power output, size, coupling, leakage inductance, interwinding capacitance and ultimately cost. A unique sampling error amplifier incorporated into the LT1105 allows operation in spite of the resultant transformer limitations. The error amplifier provides a feedback term allowing load regulation performance to be set with one external resistor. Thus, ±1% line and load regulation performance is achievable for single output voltage power supplies operating in either continuous or discontinuous mode[2].

LTC has simplified the magnetics design task by creating a series of off-the-shelf transformers for a variety of applications. New transformer design continues as an area of development. Transformers in power levels of 50W and 100W are presently available and meet international safety standards UL1950 and IEC950. Completed transformers are available from Coiltronics at 305-781-8900.

The LT1105's totem-pole output drives the gate of external high-voltage FET switch Q1. R10 controls switching transition speed. Transition speed is a trade-off between minimizing switch dV/dt common mode current contributions vs minimizing switching losses. FET conduction losses are set by the values of switch "on" resistance and primary current. The FET voltage rating must exceed the sum of the maximum rectified DC input voltage plus the leakage inductance spike. Finally, the external FET is protected from insufficient or excessive gate drive voltage with a drive protection circuit built into the LT1105.

Short-circuit protection is provided by bootstrap operation of the LT1105. Shorting an output results in switch duty cycle "on" time being limited to 500ns. The transformer cannot store sufficient energy to maintain a regulated bias winding voltage. The LT1105 senses this condition and shuts down the power supply. The power supply then returns to start-up mode. Trickle resistor R11 charges input bypass capacitor C8 to the LT1105 start threshold voltage. If the output remains shorted, the LT1105 starts and stops again. This "burp" mode protects the power supply from overload or indicates an incomplete power loop. Sense resistor R22 sets the maximum switch current available. To guarantee "burp" mode operation under fault conditions, C8 must be prevented from peak-detecting the large leakage inductance spike during maximum switch current cycles. Otherwise, the bootstrapped supply voltage would increase under a fault condition thereby leading to catastrophic failure. Resistor R3 along with C8 forms an R-C filter which prevents the diode D2/C8 combination from peak detection. This ensures well defined start cycles.

1. Data Sheet, LT1103/LT1105 Offline Switching Regulator, Linear Technology Corporation, Milpitas, CA., March 1992

2. Bonte, A. and Vinsant R., "Offline Switching Regulators Achieve ±1% Regulation in a Flux-Sensed Converter", Seventh Annual Applied Power Electronics Conference, IEEE-7803-0485-392, p 513-516, 1992

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

WARNING!

DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN OFFLINE CIRCUITS!

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF OFFLINE CIRCUITS. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THESE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. REPEAT: OFFLINE CIRCUITS CONTAIN DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

ALL TESTING PERFORMED ON AN OFFLINE CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE OFFLINE CIRCUIT'S INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF OFFLINE CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN THE CIRCUIT INPUT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.

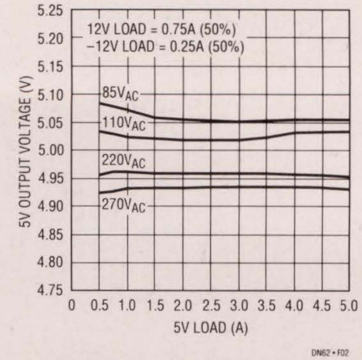
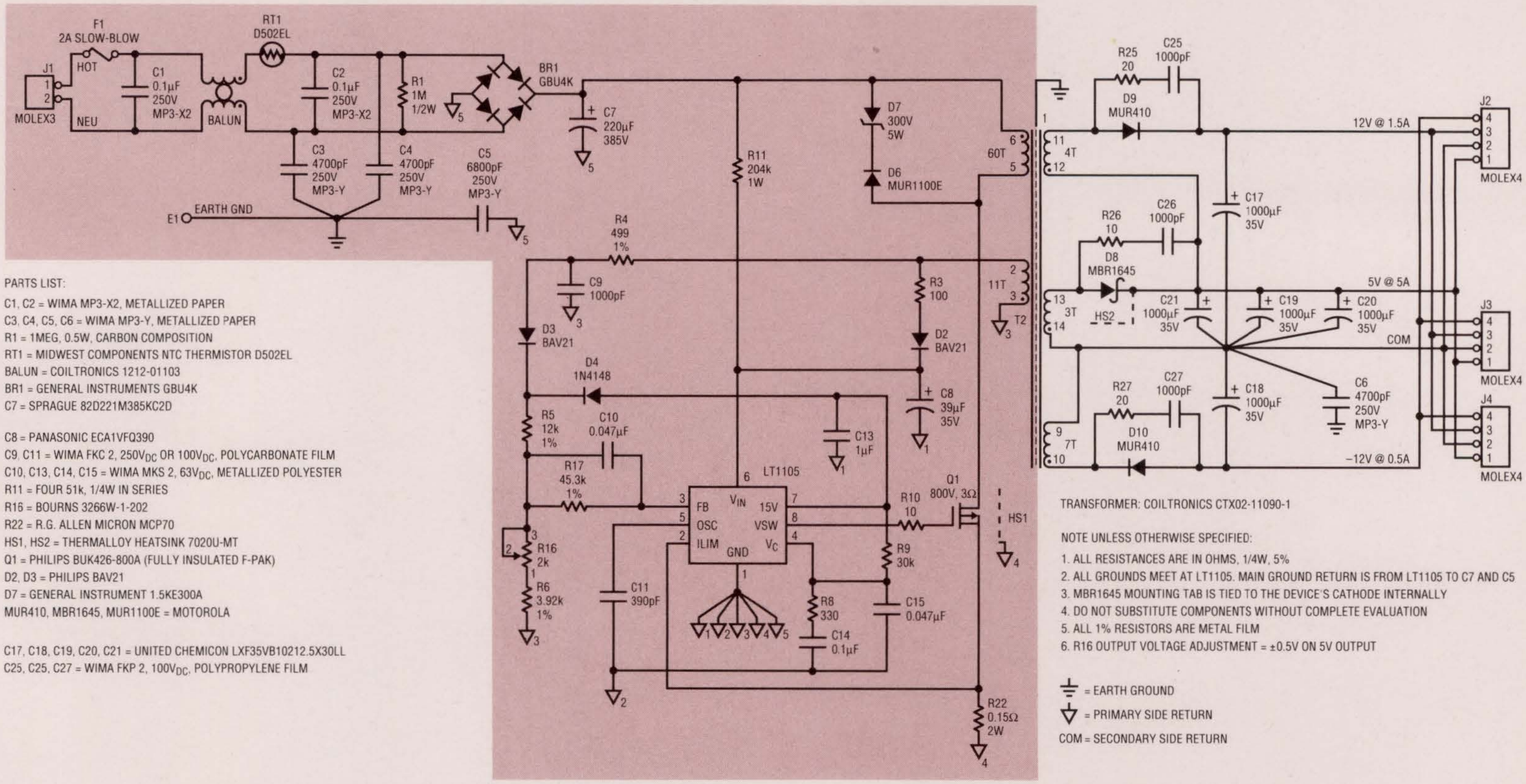


Figure 2. 5V Load Regulation vs Line Voltage



PARTS LIST:

C1, C2 = WIMA MP3-X2, METALLIZED PAPER
C3, C4, C5, C6 = WIMA MP3-Y, METALLIZED PAPER
R1 = 1MEG, 0.5W, CARBON COMPOSITION
RT1 = MIDWEST COMPONENTS NTC THERMISTOR D502EL
BALUN = COILTRONICS 1212-01103
BR1 = GENERAL INSTRUMENTS GBU4K
C7 = SPRAGUE 82D221M385KC2D

C8 = PANASONIC ECA1VFQ390
C9, C11 = WIMA FKC 2, $250V_{DC}$ OR $100V_{DC}$, POLYCARBONATE FILM
C10, C13, C14, C15 = WIMA MKS 2, $63V_{DC}$, METALLIZED POLYESTER
R11 = FOUR 51k, 1/4W IN SERIES
R16 = BOURNS 3266W-1-202
R22 = R.G. ALLEN MICRON MCP70
HS1, HS2 = THERMALLOY HEATSINK 7020U-MT
Q1 = PHILIPS BUK426-800A (FULLY INSULATED F-PAK)
D2, D3 = PHILIPS BAV21
D7 = GENERAL INSTRUMENT 1.5KE300A
MUR410, MBR1645, MUR1100E = MOTOROLA

C17, C18, C19, C20, C21 = UNITED CHEMICON LXF35VB10212.5X30LL
C25, C25, C27 = WIMA FKP 2, $100V_{DC}$, POLYPROPYLENE FILM

TRANSFORMER: COILTRONICS CTX02-11090-1

NOTE UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCES ARE IN OHMS, 1/4W, 5%
2. ALL GROUNDS MEET AT LT1105. MAIN GROUND RETURN IS FROM LT1105 TO C7 AND C5
3. MBR1645 MOUNTING TAB IS TIED TO THE DEVICE'S CATHODE INTERNALLY
4. DO NOT SUBSTITUTE COMPONENTS WITHOUT COMPLETE EVALUATION
5. ALL 1% RESISTORS ARE METAL FILM
6. R16 OUTPUT VOLTAGE ADJUSTMENT = ±0.5V ON 5V OUTPUT

= EARTH GROUND
= PRIMARY SIDE RETURN
COM = SECONDARY SIDE RETURN

Figure 1. LT1105 Fully Isolated, Offline Flyback, 100kHz, 50W Converter with Load Regulation Compensation

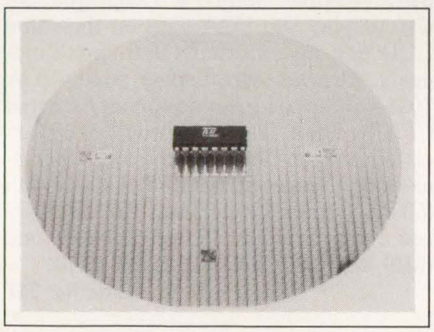
For literature on our DC to DC Converters, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

LT/GP 0992 190K

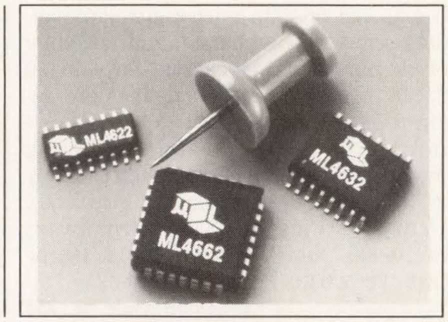
Integrated Circuits

Data-acquisition module. The μSM1601 processor combines a CMOS 8051 microcontroller, 4k×8-bit ROM, 2k×8-bit RAM, 8k×8-bit EEPROM, and a 16-bit A/D converter into a 1.85×1.14×0.6-in. 68-pin module. Firmware residing in the internal ROM includes a floating-point math package and routines for downloading programs to EEPROM via a serial port. The module also contains a programmable gain amplifier and programmable filters. $315 (100). **The Fidelis Group Inc,** Cyborg Div, 94 Bridge St, Newton, MA 02158. Phone (617) 964-9020. FAX (617) 332-8819. **Circle No. 351**

Sampling 12-bit A/D converter. The HI5812 contains an onboard track-and-hold circuit that digitizes 50,000 analog samples/sec. The 12-bit A/D converter operates from 5V and consumes 10 mW. It has a 20-μsec conversion time, which includes a 4-μsec acquisition time. The integral-linearity specification for a K-grade version is ±1 LSB, and there are no missing codes over the temperature range of −40 to +85°C. K-grade version in 24-pin SOIC packages and narrow DIPs, $8.95 (1000). **Harris Semiconductor,** Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 7015; (407) 724-3704. **Circle No. 352**



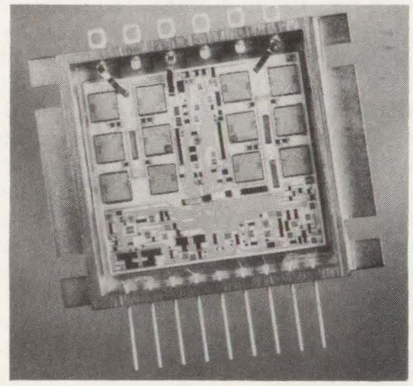
Sensor-to-μP interface. The SSC 8830 accepts low-voltage inputs from a sensing device, amplifies and digitizes the input, and sends a serial digital pulse stream to a μP. It multiplies a differential or single-end input by an external sampling input signal to eliminate amplifier offsets. The amplified signal is then converted back to dc for A/D conversion by a sigma/delta A/D converter. A feedback signal from the μP passes through a lowpass filter to generate a dc voltage to close a feedback loop around the A/D converter. In plastic DIP or SOIC package, $2.40 (2500). **Telephonics Corp,** 815 Broad Hollow Rd, Farmingdale, NY 11735. Phone (516) 755-7000. **Circle No. 353**



10Base-FL Ethernet chip set. The ML4622 fiber-optic data quantizer and the ML4662 10Base-FL transceiver provide a chip set for fiber-optic Ethernet communications. The quantizer receives signals as small as 2 mV from a fiber-optic receiver and generates clean digital waveforms for the transceiver. The transceiver detects collisions and directly drives signals from the attachment unit interface to the Ethernet controller. The transceiver also filters the

1-MHz idle signal on the cable. Quantizer, \$7; transceiver, \$19.50 (1000). **Micro Linear Corp,** 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. **Circle No. 354**

Keyboard encoder. The K25C8 Keycoder provides two bidirectional channels to communicate with an ISA bus or Micro Channel Architecture computer and an 83 or 101 IBM-style keyboard. An on-chip microcontroller handles scanning, debounce, and encoding of as many as 144 custom keys in an 8×18 matrix. You can define key assignments on the matrix for 2-key-inhibit or N-key matrix scanning modes. The encoder can buffer as many as 122 keycodes. From \$12.95 (2000). **Usar Systems Inc,** 568 Broadway, Suite 405, New York, NY 10012. Phone (212) 226-2042. FAX (212) 226-3215. **Circle No. 355**



High-power op amp. The PA30 can deliver 2000W rms continuous output power from dc to 40 kHz. The $2.8 \times 2.2 \times 0.422$-in. hybrid uses power MOSFET output stages to ensure there is no secondary breakdown. The module also uses on-chip temperature sensors for thermal protection. Operating from a 200V supply, the module can deliver a 100A output pulse. \$1585 (100). **Apex μTech Corp,** 5980 N Shannon Rd, Tucson, AZ 85741. Phone (602) 690-8603. FAX (602) 888-3329. **Circle No. 356**

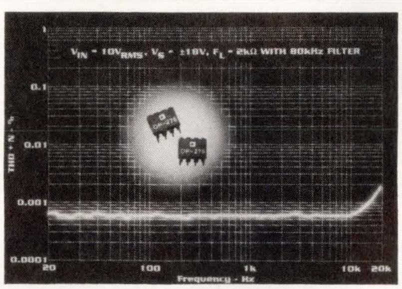
Graphics controller. The CL-GD6420 displays data in three ways. You can display data on a VGA-compatible 640×480-pixel notebook LCD. You can also display the VGA data on the same LCD and an external CRT simultaneously. Or, you can display super-VGA 1024×768-pixel graphics on an external CRT by itself. The chip provides 64 levels of gray on monochrome and 256 colors on active-matrix TFT LCDs. \$45 (5000). **Cirrus Logic Inc,** 3100 W Warren Ave, Fremont, CA 94538. Phone (510) 623-8300. FAX (510) 226-2240. **Circle No. 357**

3.3V read/write preamplifier. The VM3200 is a read/write amplifier for 2.5- and 1.8-in. disk drives. The chip has an input noise voltage of 0.55 nV/$\sqrt{Hz}$ and a 5V differential p-p write voltage. When deactivated, a sleep mode consumes 1.5 mW. The chip operates from 3.3V and can coexist with 5V logic. \$7 (1000). **VTC Inc,** 2800 E Old Shakopee Rd, Bloomington, IN 55425. Phone (612) 853-3323. **Circle No. 358**

8-bit CMOS μC. The first devices in K0 family of 8-bit microcontrollers are the 7800x and 7801x. Both devices contain 8- and 16-bit timers, a watchdog timer, two serial interfaces, and parallel

I/O ports. The 7801x contains an 8-bit A/D converter. The K0 family operates from 2.7 to 6V and an 8.38-MHz internal oscillator. You can program the CPU's instruction cycle time to range from 0.48 to 7.63 μsec. The chip draws 7.5 mA when operating and 50 nA in power-down mode. 7800x, $4 to $6; 7801x, $5 to $8 (5000). **NEC Electronics Inc,** Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. FAX (415) 965-6130.
Circle No. 359

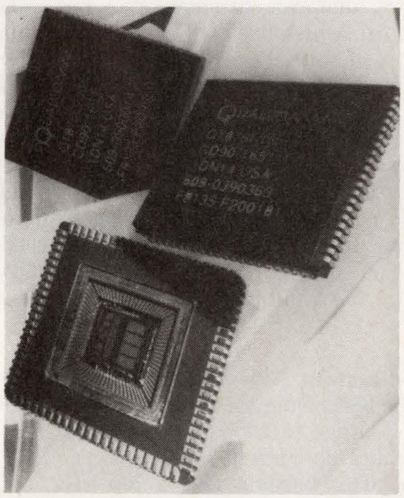
Video-processing chip set. The Videoview chip set provides scalable full-motion video windows using Microsoft's Windows or DOS software. It also provides multiple frame capture, VGA or XGA graphics and text overlay, special effects, chroma and linear keying, and a palette of as many as 16.7 million colors. The set also lets you deliver the output to a VGA monitor, projection TV, or video tape. The chip set can combine VGA or XGA graphics and text with inputs from one or more selectable sources. $120 (100). **Trident Microsystems Inc,** 205 Ravendale Dr, Mountain View, CA 94043. Phone (415) 691-9211. FAX (415) 691-9260. **Circle No. 360**



Dual op amp. The OP-275 dual op amp features a Butler input stage consisting of both JFET and bipolar transistors. The feature permits 0.0006% typical total harmonic distortion and a 6-nV/$\sqrt{\text{Hz}}$ input-voltage-noise specification. The input current noise is 1.5 pA/$\sqrt{\text{Hz}}$, and the maximum input offset current is 10 nA. Maximum input offset voltage is 1 mV; the device has a 9-MHz gain-bandwidth product and a 22V/μsec slew rate. $0.99 (100). **Analog Devices Inc,** 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. FAX (617) 821-4273. **Circle No. 361**

Antialiasing filters. The D70 family consists of fixed-frequency antialiasing filters in 14-pin, double-width DIPs. The chips are available in 4-, 6-, and

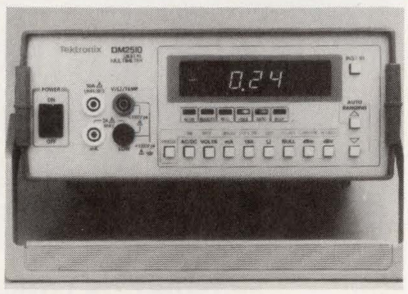
8-pole configurations having Butterworth or Bessel transfer functions. The Butterworth filter attenuation rate is −6n dB/octave, where n is the number of poles. The minimum input impedance is 10 kΩ, and the maximum output impedance is 1Ω. Filters come with 3-dB corner frequencies ranging from 500 Hz to 50 kHz. The 8-pole filter, from $49. Delivery, four to six weeks ARO. **Frequency Devices,** 25 Locust St, Haverhill, MA 01832. Phone (508) 374-0761. FAX (508) 521-1839. **Circle No. 362**



Full-duplex trellis codec. The Q1875 is a full-duplex codec for Pragmatic Trellis coded modulation. The 84-pin IC can achieve 60-Mbps rates and 3-bps/Hz bandwidth efficiency. The codec lets you implement a 64-state, ⅔ encoding and decoding rate for 8-ary modulation (for example, phase-shift keying (PSK)) and ¾ encoding and decoding rate for 16-ary modulation. The chip set is also backward compatible with the company's Q1650 family of Viterbi decoders. From $62. **Qualcomm,** 10555 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 597-5005. FAX (619) 452-9096. **Circle No. 363**

Low-voltage μCs. Five low-voltage versions of the 8-bit 68HC11 microcontroller family operate from 3 to 5.5V. The A8, D3, E9, and L6 versions operate at 2 MHz, and the K4 version operates at 3 MHz. The parts are available in plastic-leaded-chip-carrier packages and operate within a −20 to +70°C range. $7.94 to $15.86, (10,000). **Motorola Inc,** Microprocessor and Memory Technologies Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-3465. **Circle No. 364**

Test & Measurement Instruments



Economical benchtop instruments. The TM2500 series currently includes the following members: the $595 DM2510, a 4½-digit autoranging DMM, and the $695 DM2510G, which is similar to the DM2510 but includes an IEEE-488.1 interface. The vendor has also announced other low-cost instruments: the $545 CMC251, a 1.3-GHz multifunction counter with ±1-ppm timebase accuracy; the $995 CFG280, a 0.1-Hz to 11-MHz sweep/function generator that includes a 100-MHz counter; and the $345 PS281 and PS282 power supplies. The first supply delivers 0 to 30V at 3A max; the second delivers 0 to 18V at 5A max. Delivery, stock to six weeks ARO. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200.

Circle No. 365

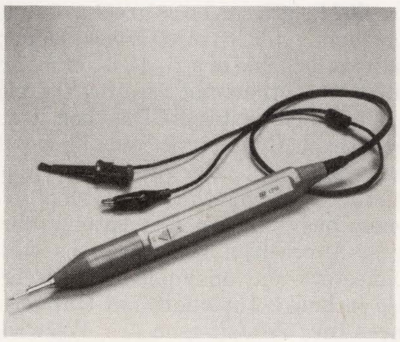
VMEbus analyzer. The VME310, a 6U VMEbus board, samples eight bus signals at 200 MHz. It supports 8-, 16-, and 32-bit transfers, can act as a bus master on both the P_1 and P_2 connectors, and can stimulate the bus. The board, which has a 100-bit-wide (96 bus signals plus 4 external signals), 50-MHz, 32k-frame trace buffer (128k frames optional), constructs histograms for signals and address ranges in real time. The front panel includes a reset button and an LED that monitors the 5V power line. $8995. **Silicon Control Inc,** 1020 Milwaukee Ave, Suite 305, Deerfield, IL 60015. Phone (708) 634-9313. FAX (708) 808-9090. **Circle No. 366**

9-function, 4½-digit, true-rms DMM. The 380285 digital multimeter measures dc voltage to 1 kV, ac voltage to 750V, ac and dc current to 10A, capacitance to 40 μF, frequency to 200 kHz, and temperature to 1370°C. Basic dc accuracy is 0.5%. The 7.25×3.25×1.136-in. unit, which receives power from a 9V battery, includes a 42-segment analog bar-graph display. Features include data hold, recall of minimum and maximum readings, readings relative to a programmable offset, averaging of readings, and calculation of % deviation from a reference value. $189. **Extech Instruments Corp,** 335 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. FAX (617) 890-7864. **Circle No. 367**

Battery-powered, portable, bit-error-rate testers. Two versions of the 76B operate from battery power. A $2295 unit includes an internal rechargeable battery. A $1450 handheld unit works with the vendor's $395 model 45 rechargeable battery pack and case. The testers operate with data at rates from 50 bps in asynchronous mode to 10 Mbps in synchronous mode. Plug-in interface modules (from $340) enable the testers to conform to a variety of standards. **International Data Sciences Inc,** 501 Jefferson Ave, Warwick, RI 02886. Phone (800) 437-3282; (401) 737-9900. FAX (401) 737-9911.

Circle No. 368

0.5-to-15-Gbit/sec digital pattern generator. The MP1755A, which produces a serial bit stream using internal or external clocks, can create pseudorandom binary sequences with lengths from 2^7-1 to $2^{31}-1$. You can also define your own patterns, with lengths to 512 bits. The output is differential. You can vary the offset from -2 to $+2$V (open circuit) and the amplitude from 0.5 to 2V. You can adjust the data and data outputs separately, or the adjustments can track. Four parallel outputs each operate at ¼ the rate of the main output. $255,900. **Anritsu Wiltron Sales Co,** 685 Jarvis Dr, Morgan Hill, CA 95037. Phone (408) 776-8300. FAX (408) 776-1744. **Circle No. 369**

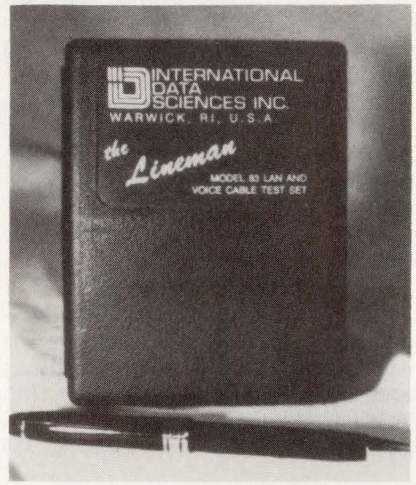


50-MHz pen-size logic probe. The LP50, which receives power from the circuit under test, measures signals from TTL and other 5V logic families at frequencies to 50 MHz. It detects pulses as narrow as 10 nsec and provides simultaneous LED and tone indications. $45. **Beckman Industrial Corp,** 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 495-3200. FAX (619) 268-0172. TLX 249031. **Circle No. 370**

In-circuit emulator for 68332. The PC-based Emul16/300-PC with the $1995 Pod 332 works with the 68330, 68331, and 68332 at their full 16.78-MHz clock rate. The emulator consists of an ISA bus board, which connects to the pod board using a twisted-pair ribbon cable. A trace board is optional. The accompanying software runs under MS-Windows V3.x. **Nohau Corp,** 51 E Campbell Ave, Campbell, CA 95008. Phone (408) 866-1820. FAX (408) 378-7869. **Circle No. 371**

In-circuit emulator for 8-MHz 68HC05. You can purchase the Icemaster-68HC05 in two versions. The basic model 200 costs $1499; the model 400 costs $2299 and adds a 4k-frame trace buffer, full watchdog-timer support, and two real-time performance analyzers. Both models include 32 kbytes of emulation memory, 32,000 hardware breakpoints, 32,000 trace on/off triggers, and 32,000 write-access triggers. The units communicate with the host MS-DOS PC via a 115.2-kbps RS-232C link. The user interface lets you open windows to observe memory, source code, watch points, the stack, the system status, and registers. Probe card, from $499. **MetaLink Corp,** Box 1329, Chandler, AZ 85244. Phone (602) 926-0797. FAX (602) 926-1198. TLX 4998050. **Circle No. 372**

LAN- and voice-cable test set. A $395 pair of handheld model 83 Lineman test sets lets you verify shielded and unshielded twisted-pair circuits used in LANs and voice communications. The



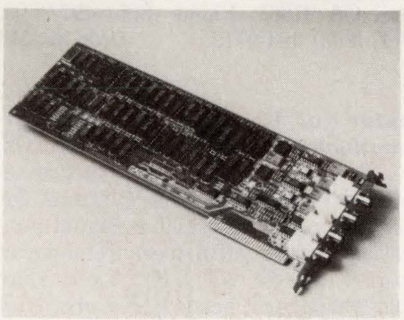
circuits' length can be as great as 1 mile. One unit applies tracer tones sequentially to each line of a 2-, 4-, 6-, or 8-wire cable. The other unit receives the signals and illuminates LEDs when it detects them. By observing the light pattern, you can identify shorted and open conductors. The tones override dial tones, busy signals, and battery voltages. A breakout box that uses RJ45 connectors and an audio monitor are also included. **International Data Sciences Inc,** 501 Jefferson Ave, Warwick, RI 02886. Phone (800) 437-3282; (401) 737-9900. FAX (401) 737-9911. **Circle No. 373**

Interface adapter for bit-error-rate tester. A $295 adapter allows the vendor's $595 72/62 pocket bit-error-rate tester to test modems at both their RS-232C and CCITT V.24 or V.35 interfaces. A line-powered breakout box with two LEDs per line monitors all 25 signals and lets you interrupt or patch any line. **International Data Sciences Inc,** 501 Jefferson Ave, Warwick, RI 02886. Phone (800) 437-3282; (401) 737-9900. FAX (401) 737-9911. **Circle No. 374**

100-kHz-to-2.7-GHz synthesized signal generator. The 3221 offers 10-Hz resolution (20 Hz above 1.35 GHz) and 0.05-ppm frequency accuracy. Modulation capabilities include seven modes and 14 combination modes. Output levels range from +13 to −133 dBm, variable over a ±5-dB range in 0.1-dB steps. The unit stores 100 setups. $12,300. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; (516) 231-6900. **Circle No. 375**

Digital sync/test generator. The 411D provides video test signals and serial digital audio in the Audio Engineering Society/European Broadcast Union format. You can program a 20-character source-identification signal from the front panel. The generator provides further identification via an integral clock/calendar. Signals include ones specified by the Society of Motion-Picture and Television Engineers and the Electronics Industry Association. $5600. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; (516) 231-6900. **Circle No. 376**

Frame-relay test software for WAN protocol analyzers. The 18258A frame-relay-decode and statistical-analysis software package and the 18278A frame-relay post-processing software package work with the vendor's 4957A, 4957PC, and 4952A wide-area-network (WAN) protocol analyzers. The packages, which monitor 13 network-performance parameters and decode congestion-notification bits, provide user-definable frame-element displays and allow you to tune the network. $790 each. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 377**

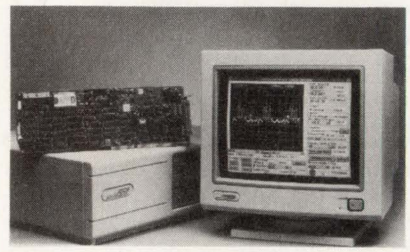


$995, 40-Msample/sec ISA bus DSO board. The Compuscope Lite 64K can sample two channels at 20 Msamples/sec each or one channel at 40 Msamples/sec. Resolution is 8 bits and memory depth is 32 kbytes per channel. The vendor supplies DSO software and drivers for popular MS-DOS languages. **Gage Applied Sciences Inc,** 5465 Vanden Abeele, Montreal, PQ H4S 1S1, Canada. Phone (514) 337-6893. FAX (514) 337-8411. **Circle No. 378**

RGB generator. The 1605 lets you evaluate high-resolution color monitors, such as those in workstations. The unit's maximum pixel-clock frequency is

300 MHz. The generator, which provides a palette of 256 colors drawn from a repertoire of 16.7 million, stores 100 programs in RAM, 100 more in ROM, and 1800 more on a floppy disk. An EPROM programmer is built in. The graphics user interface features menu displays from which you make selections with a mouse. $18,500. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; (516) 231-6900. **Circle No. 379**

Environmental compensator for laser-interferometer. The 10866A, an ISA bus board, provides environmental compensation for laser-interferometer positioning systems that use the vendor's 10885A axis board (also an ISA bus board). The positioning systems use the wavelength of light as their fundamental measurement unit. This wavelength can vary by ±10 ppm as ambient temperature, humidity, and atmospheric pressure change. Compensation reduces the variation to ±1.5 ppm. $1330; air sensor, $4250. A material-temperature sensor, which compensates for the temperature-dependent expansion of the object whose length you are measuring, costs $1060. Delivery, four to six weeks ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 380**

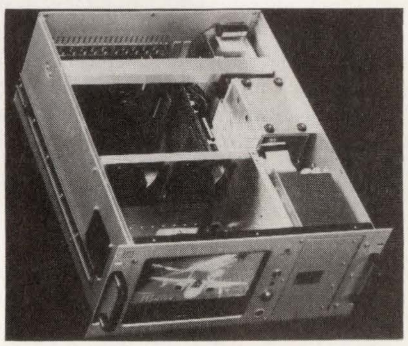


DSO software for data-acquisition boards. Besides software, the SWI-DAQ200 Daqscope package includes a National Instruments AT-MIO-16F-5 data-acquisition board, which collects 12-bit-resolution analog data from eight differential or 16 single-ended channels at speeds to 200 ksamples/sec. The package lets the computer system function as an oscilloscope. $2090; software alone, $495. **SystemWare Inc,** 660 Hampshire Rd, Suite 100, Westlake Village, CA 91361. Phone (805) 497-9603. FAX (805) 494-9719. **Circle No. 381**

Tester for ICs used in personal-communications products. The RF02, an option for the vendor's Synchro series of production test systems for mixed-signal ICs, provides signal generation and sensitive measurements at frequencies to 2.7 GHz. Less than $300,000 per test head. **LTX Corp,** LTX Park at University Ave, Westwood, MA 02090. Phone (617) 461-1000. FAX (617) 326-5895. **Circle No. 382**

Vertical-coupling plane for ESD testing. The 0.5m × 0.5m VCP-1 works with the vendor's Minizap electrostatic-discharge (ESD) simulator to meet the requirements of the recently revised International Electrotechnical Commission standard, IEC 801-2. The European community will soon require most electronic equipment sold in Europe to comply with the standard. $1475. Delivery, 60 to 90 days ARO. **Keytek Instrument Corp,** 260 Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880. FAX (508) 657-4803. **Circle No. 383**

486DX embedded PC module. The Little Board/486 member of the company's PC/104 family of embedded modules contains a 33-MHz 486DX or 20-MHz 486SX μP. In addition, the module has as much as 32 kbytes of secondary cache and 16 Mbytes of dynamic RAM. Other functions include two serial ports, a parallel port, SCSI port, bootable solid-state disk, and an IDE controller. $1995 (100). **Ampro Computers Inc,** 990 Almanor Ave, Sunnyvale, CA 94086. Phone (408) 522-2100. FAX (408) 720-1305. **Circle No. 408**



Rack-mount PC with flat-panel display. The ST-3000-EL has a flat-panel electroluminescent display. The amber display allows room in the 19×8.8×22-in. chassis for 12 expansion slots and as much as 520 Mbytes of storage. Processor options range from a 10-MHz 286 to a 50-MHz 486 microprocessor. $3950 to $6950. **IBI Systems Inc,** 6842 NW 20th Ave, Fort Lauderdale, FL 33309. Phone (305) 978-9225. FAX (305) 978-9226. **Circle No. 409**

VMEbus 3U memory board with 4-Mbyte static RAM. The two RAM-ROM boards have as much as 4 Mbytes of battery-backed static RAM and two flash-EPROM sockets. The extended-temperature 3U VMEbus board operates at temperatures from −40° to +85°C. The industrial-quality version operates at 0 to 70°C. MSX-RAMROM and MS-RAMROM, from $550 and $950, respectively. **Matrix Corp,** 1203 New Hope Rd, Raleigh, NC 27610. Phone (800) 848-2330; (919) 231-8000. FAX (919) 231-8001. **Circle No. 410**

IBM PS/1 printer. The IBM 2390 PS/1 Printer is a 24-wire, narrow-carriage dot-matrix printer with print speeds as high as 200 cps in draft and 60 cps in letter-quality modes. The printer's resolution is 360×360 dpi; it has eight resident fonts and a 32-kbyte buffer. $499. **Lexmark International Inc,** 740 New Circle Rd NW, Lexington, KY 40511. Phone (800) 358-5835; (606) 232-6906. **Circle No. 411**

16-Mbyte flash-memory card. The 16-Mbyte flash-memory card uses Intel's 8-Mbit flash chips and meets PCMCIA 2.0 and JEIDA 4.1 standards. $580 (OEM qty). **Epson America,** OEM Components Group, 20770 Madrona Ave, Torrance, CA 90509. Phone (310) 787-6300. **Circle No. 412**

6U VMEbus board with dual FDDI nodes. The FDDI-1 employs the SPARClite embedded processor to implement two FDDI nodes on a single VMEbus board. The board achieves PMD sublayer compliance using combined Data Link transceivers and integrated Media Interface Connectors. The board employs AMD's Supernet-2 chip set; 8 Mbytes of dynamic RAM; 1 Mbyte of flash EPROM; and a 128-kbyte FDDI buffer static RAM. $9500. Delivery, 90 days ARO. **Radstone Technology,** 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; (201) 391-2700. FAX (201) 391-2899. **Circle No. 413**

DSP interface board. This ISA bus board provides a bridge between the company's DSP-Link and Data Translation's DT-Connect high-speed buses. High-speed FIFO buffers maximize data transfers between the buses. The board operates as a slave for a DT-Connect I/O board. From $795. **Spectrum Signal Processing Inc,** Westborough Office Park, 1500 W Park Dr, Westborough, MA 01581. Phone (800) 323-1842; (508) 366-7355. **Circle No. 414**

Laser-based bar-code verifier. The LC 2912 laser-based bar-code verifier reads Postnet, the proprietary bar code of the United States Postal Service. The scanner can display or transmit data to a host via an RS-232C link. Mass mailers receive an incentive from the postal service of 5 cents/letter for using Postnet. $2995. **Symbol Technologies Inc,** 116 Wilbur Pl, Bohemia, NY 11716. Phone (516) 563-2400, ext 4215. **Circle No. 415**

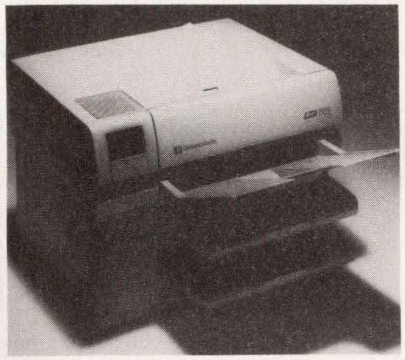
Graphics workstation. In its basic configuration, the ME 486-Local Bus graphics workstation comes with a 486-SX/25 processor, 4 Mbytes of RAM, a 170-Mbyte hard-disk drive, 3½- and 5¼-in. high-density floppy-disk drives, a Super-VGA color monitor, mouse, DOS 2.0, and Windows 3.1. Local-bus graphics on the mother board employ a Tseng Labs ET4000G graphics chip set. The computer, with five disk-drive bays, measures 6.5×14.5×16.5 in. $2175. **Micro Express,** 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (800) 989-9900; (714) 852-1400. FAX (714) 852-1225. **Circle No. 416**

Rack-mount computer system. The standard mother board on the BGW U86 rack-mount microcomputer comes with a 40-MHz 80386DX microprocessor (μP), 4 Mbytes of RAM, and a configurable secondary cache of 64 kbytes. The computer has a 120-Mbyte Maxtor IDE drive with a 15-msec access time, 64-kbyte look-ahead cache, and DOS 5.0. You can optionally upgrade to a 50-MHz 486 μP and 64 Mbytes of RAM. $2995; optional rack-mount keyboard drawer, $89. **BGW Systems Inc,** 13130 Yukon Ave, Hawthorne, CA 90251. Phone (310) 973-8090. FAX (310) 676-6713. **Circle No. 417**

6-Gbyte ½-in. tape drive. Based on digital-linear-tape (DLT) hardware, the T860 records data at a density of 224 tracks/in. and can reach data-transfer rates as fast as 800 kbytes/sec. The company claims the 6-Gbyte ½-in. drive has a 20% increase in capacity and data throughput 2× faster than comparable 8-mm products. \$3500 (OEM qty). **Cipher Data Products Inc,** 10101 Old Grove Rd, San Diego, CA 92131. Phone (619) 693-7111. **Circle No. 418**

25-MHz 386SX single-board computer. An industrial-grade 386SX single-board computer, the CAT975 operates at 16, 20, or 25 MHz. The computer has up to 16 Mbytes of dynamic RAM and four sockets for an onboard PROM/flash disk. It also has an IDE controller, two serial ports, a parallel port, and a VGA controller that supports 1024×768×16-bit color modes. The 25-MHz CAT975 with VGA, \$810; without VGA, \$755. **Diversified Technology Inc,** 112 E State St, Ridgeland, MS 39158. Phone (800) 443-2667; (601) 856-4121. FAX (601) 856-2888. TLX 585326. **Circle No. 419**

Laser printers/plotters. The LZR 1555 series uses HPGL and PCL5 page-description languages and accommo-



dates paper as large as 11×17 in. The printers have a resolution of 400×400 dpi, a speed of 15 pages/minute, and 4 Mbytes of RAM (expandable to 16 Mbytes). \$5995 to \$6995. **Dataproducts Corp,** 6219 De Soto Ave, Woodland Hills, CA 91365. Phone (800) 334-3174; (818) 887-8000. **Circle No. 420**

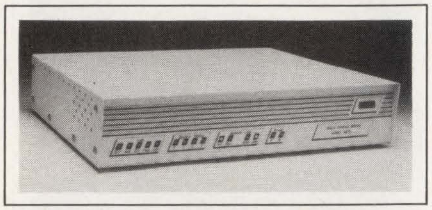
Ethernet adapter for HP printers. The H1000 adapter card plugs into the Modular I/O slot of HP's Laserjet IIISi or Designjet to let DEC computers use these printers on an Ethernet network. The adapter has a standard and a thin interface. A twisted-pair interface is optional. \$1095. Delivery, 60 days ARO. **XCD Inc,** 2172 Dupont Dr #204, Irvine, CA 92715. Phone (714) 476-7855. FAX (714) 752-0609. **Circle No. 421**

Color X terminal for open network. TX800C Open Network Terminal can interpret X commands at a rate of 104,000 Xstones. The terminal can also download other terminal services via an SBus expansion slot. The base unit contains a 25-MHz 68040 microprocessor, 4 Mbytes of RAM (expandable to 16 Mbytes), and two custom-graphics ASICs. Base unit, \$3495; with 19-in. monitor, keyboard, and mouse, \$5495. **Visual,** 120 Flanders Rd, Westborough, MA 01581. Phone (508) 836-4400. FAX (508) 366-4337. **Circle No. 422**

Video graphics adapter. The Evolution VGA Super-VGA adapter has resolutions of 1280×1024 pixels in 16 colors, 1024×768 pixels in 256 colors, 800×600 pixels in 65,536 colors, and 640×480 pixels in up to 16.7 million simultaneous colors. The ISAbus adapter comes with drivers for Windows applications, CAD/CAM rendering, and DOS-based imaging software. $199. **STB Systems Inc,** 1651 N Glenville, Suite 210, Richardson, TX 75081. Phone (214) 234-8750. **Circle No. 423**

VMEbus SCSI-2 host adapter. The MVS/200 single 6U VMEbus module works with SCSI-1 or SCSI-2 devices. The adapter has an aggregate synchronous SCSI data rate of 20 Mbytes/sec. Dual RISC processors control all SCSI functions. From $1990 (single qty). **Macrolink Inc,** 1500 N Kellogg Dr, Anaheim, CA 92807. Phone (714) 777-8800. FAX (714) 777-8807. **Circle No. 424**

33-MHz Mac PC. The Macintosh Quadra 950 computer is the latest member of the Quadra family. The computer employs a 33-MHz 68040 microprocessor. The computer has an Ethernet port, 8 Mbytes of RAM (expandable to 64 Mbytes), and options for floppy-, 230-Mbyte, or 400-Mbyte hard-disk drives. $7199 to $10,208. Logic-board upgrade kit, $1499. **Apple Computer Inc,** 20525 Mariani Ave, Cupertino, CA 95014. Phone (408) 996-1010. **Circle No. 425**



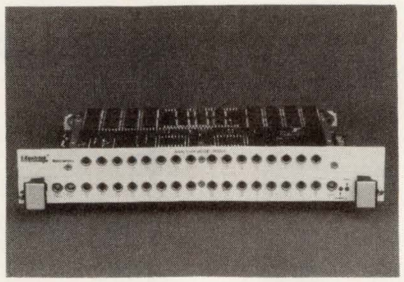
Ethernet bridge. The 8870 Campus Ethernet Bridge connects LAN segments at distances as far as 25 km. The bridge operates at the Data Link Layer of the OSI model, and it filters 12,000 packets/sec and forwards 10,000 packets/sec. Network interfaces include 10Base-5, 10Base-2, 10Base-T, and FOIRL connectors. $5698. **Canoga Perkins,** 21012 Lassen St, Chatsworth, CA 91311. Phone (818) 718-6300. **Circle No. 426**

64-Mflops scientific workstation. The Visualization Solution handles 64-Mflops and has a software-selectable display resolution from 1 to 32 bits/pixel. The unit includes real-time full-color image and motion compression and decompression using an image digitizer. Workstation with 8-Mbyte video RAM, 32-Mbyte dynamic RAM, image digitizer, 200-Mbyte hard-disk drive, and monitor, $20,000. **Lazerus,** Box 13249, Oakland, CA 94661. Phone/FAX (510) 339-6263. **Circle No. 427**

HP Laserjet IIISi print server. As many as seven users can connect to an HP Laserjet IIISi printer—through six serial and one parallel port—without a LAN. The user-installable board emulates HP's MIO interface and is available with 1 to 4 Mbytes of buffer memory. From $795. **ASP Computer Products Inc,** 160 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 746-2965. FAX (408) 746-2803. **Circle No. 428**

Novell-network print servers. Pocket Print Servers install on a printer's parallel port to construct a network printer. With the server, you can attach the printer directly to a Novell

network, utilizing Novell's standard print services. Three connections are available: 10Base-T or 10Base-2 Ethernet, $495; 9-pin Token Ring, $995. **Extended Systems,** 6123 N Meeker Ave, Boise, ID 83704. Phone (208) 322-7575. FAX (208) 377-1906. **Circle No. 429**



32-channel VME transient recorder card. The 2032LC can simultaneously capture and record transients on as many as 32 channels. The 6U VMEbus board has 32 differential inputs having a jumper-selectable sensitivity of 0 to 10V or ±5V. The board can capture 10,000 samples/sec for all channels using the onboard 12-bit Analog Sampling Array. The sampling rate increases to 200,000 samples/sec for a single channel. With 1M word of memory, $9295; with 2M words of memory, $9995. Delivery, 10 weeks ARO. **Analytek Ltd,** 365 San Aleso Ave, Sunnyvale, CA 94086. Phone (408) 745-1114. FAX (408) 745-1894. **Circle No. 430**

Inverse multiplexer. The RCP-BMM (bandwidth-management module) serves seldom-used high-bandwidth applications such as video conferencing, LAN-internetworking, and disaster backup of high-speed trunks. The unit can automatically demand more bandwidth from the network provider on an as-needed basis. The module has from 2 to 8 input ports and multiple network connections. From $10,000. **Racal-Datacom Inc,** Box 407044, Fort Lauderdale, FL 33340. Phone (305) 846-1601. FAX (305) 846-3935. **Circle No. 431**

ISA bus DSP board. Banshee II, an enhanced version of the Banshee System Board, uses a 40-MHz TMS320C30 DSP chip and as much as 4 Mbytes of static RAM. The board communicates with the host via an 8-bit dual-port RAM. A software option, called Ashell, creates a DPS-board development system. Board with 256-kbyte static RAM, $3895; development systems, from $7395. Delivery, third quarter 1992. **Atlanta Signal Processors Inc,** 770 Spring St, Atlanta, GA 30308. Phone (404) 892-7265. FAX (404) 892-2512. **Circle No. 432**

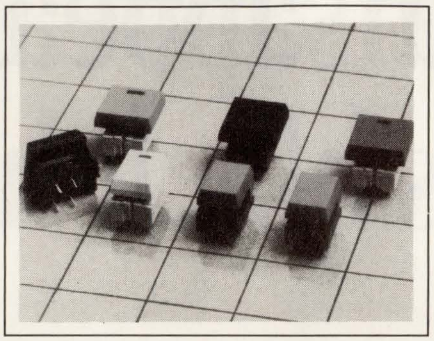
Interface board. The PM5512 SAPP board can provide OC-12 interfaces for connecting local ATM switches and SONET-based public networks. It simplifies the task of developing broadband trials and test beds to evaluate SONET/ATM technology. The board provides a 622-Mbps SONET STS-12 electrical interface, facilities to access payload, and an optional OC-12 optical interface. $7995. **Pacific Microelectronics Centre,** 8999 Nelson Way, Burnaby, BC V5A 4B5, Canada. Phone (604) 293-5755. FAX (604) 293-5787. **Circle No. 433**

Components & Power Supplies

Green LEDs. These units operate at 550 nm and are available in all popular shapes. The units have a 0.2% max quantum efficiency and a 1.36 l/W visual efficiency. $0.10 to $0.50. **Lumex Opto/Components Inc,** 292 E Hellen Rd, Palatine, IL 60067. Phone (708) 359-2790. FAX (708) 359-8904. **Circle No. 384**

Surface-mount LEDs. Series 6250F right-angle T-1 LEDs have a high-profile lens designed for through-panel mounting. Viewing angle measures 90°. Units are available in red, amber, green, yellow, blue, and bicolor red-green. The line includes units that operate on currents of 2 mA, as well as models with built-in resistors for 5 and 12V operation. From $0.59 (1000). **Industrial Devices Inc,** 260 Railroad Ave, Hackensack, NJ 07601. Phone (201) 489-8989. FAX (201) 489-6911. **Circle No. 385**

Keyswitches. SRKFL and STKFL switches have an overmolded LED lens that provides as much as 16-kV ESD protection. The illuminated units have flat switch caps to give a dead-front appearance. The LEDs are available in red, yellow, or green. Two cap sizes and a choice of momentary or alternate switching actions are available. $2.25 to $3.70. **ITT Schadow Inc,** 8081 Wallace Rd, Eden Prairie, MN 55344. Phone (612) 934-4400. **Circle No. 386**



Board connector. ZIP X-50 board-to-board connectors are based on the FLXibus specification. They feature a 3-row interstitial array of either 25 or 30 pins per row. Both the plug and receptacle are polarized to ensure correct mating. Two mounting heights are available: 0.295 and 0.433 in. $0.12/mated line (1000). **McKenzie Technology,** 44370 Old Warm Springs Blvd, Fremont, CA 94538. Phone (510) 651-2700. FAX (510) 651-1020. TWX 910-240-6355. **Circle No. 387**

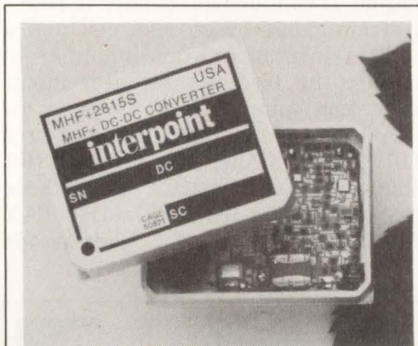
Interface module. The PE-65425 surface-mount 10Base-T interface module has two channels and consists of low-pass filters, isolation transformers, and a common-mode choke on the TX channel. The module meets IEEE 802.3 standards and FCC/VDE emissions requirements. $6 (1000). **Pulse Engineering Inc,** Box 12235, San Diego, CA 92112. Phone (619) 674-8100; (619) 674-8224. FAX (619) 674-8262. **Circle No. 388**

Breadboard modules. PRL-950 modules come with a connector and pc board with 138 to 231 plated-through holes on a 0.1-in. grid. The board has a ground plane on one side for noise suppression. $32. **Pulse Research Lab,** 1536 W 25th St, San Pedro, CA 90732. Phone (310) 515-5199. FAX (310) 515-0068. **Circle No. 389**

Panel meters. The Versameter line includes three models—Model G920DV, which has a 200-mV to 1000V dc range; Model G921DA, with a 200-μA to 2A capability; and G922DA, which suits 4- to 20-mA applications. All models feature rear-panel terminal pins, automatic zero adjust, and a 3½-digit LED display. From $79. **Extech Instruments Corp,** 335 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. FAX (617) 890-7864. **Circle No. 390**

Crystal oscillator. Model 2890080 operates over a 30- to 110-MHz range. The ovenized unit has a frequency stability of ±0.001 ppm over a −40 to +70°C range. Phase noise at 100 MHz equals −95 dBc/Hz at 10 Hz and −125 dBc/Hz at 100 Hz. $500 to $600 (500). **Piezo Crystal Co,** 100 K St, Carlisle, PA 17013. Phone (717) 249-2151. FAX (717) 249-7861. TWX 510-650-2280. **Circle No. 391**

Test clip. Model 5830 Maxigrabber test clip features a double-gripping pincer that can be rotated for easy installation. An extended shaft makes inaccessible test points easier to reach. The clip comes with a socket for a standard 4-mm banana plug connection and a screw for direct wire termination. $6.30. **ITT Pomona Electronics,** 1500 E Ninth St, Pomona, CA 91769. Phone (714) 469-2900. FAX (714) 629-3317. **Circle No. 392**

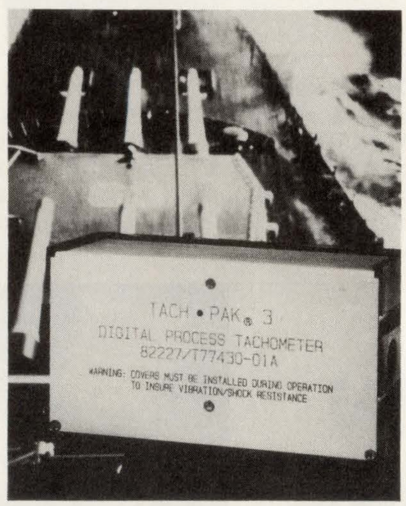


DC-DC converter. MHF+ Series converters are MIL-STD-883 compliant. The 15W units have single or dual outputs of 5, 12, 15, ±12, or ±15V. Input range spans 16 to 40V. Efficiency is as high as 82%, and line and load regulation equal 15 mV. $296 (100). Delivery, eight weeks ARO. **Interpoint Corp,** 10301 Willows Rd, Redmond, WA 98073. Phone (206) 882-3100. FAX (206) 882-1990. **Circle No. 393**

Isolator. Model 281 opto isolator provides full-duplex data and control link for RS-422 signals and eliminates any electrical connections between the ports. The unit provides two optically isolated signal paths for data, TD, RD, and a control signal pair that can support RTS/CTS or DTR/DCD. Internal jumpers select the signal pair. $158. **Telebyte Technology Inc,** 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 835-3298; (516) 423-3232. FAX (516) 385-8184. **Circle No. 394**

Low-profile IC sockets. These surface-mount sockets have a 0.2-in. mounted height. The sockets are available with 6 to 64 pins in single- or dual-row configurations. The sockets can withstand vapor-phase and infrared-soldering techniques and are available with either gold or tin plating on the contacts. $0.50 for a 20-pin model. **Socket Express Inc,** 100 Jersey Ave, Bldg B-202, New Brunswick, NJ 08903. Phone (908) 247-9500. FAX (908) 247-9816. **Circle No. 395**

Signal conditioner. Model 165 offers an alarm output as well as an analog output. It contains a regulator to power a strain-gauge-based load cell and a built-in instrumentation amplifier to amplify the bridge transducer input. Excitation supply-voltage range spans 4 to 10V dc, and regulation measures 0.01%. $155. **Calex Mfg Co Inc,** 2401 Stanwell Dr, Concord, CA 94520. Phone (800) 542-3355; (510) 687-4411. FAX (510) 687-3333. **Circle No. 396**



Process transducer. The Tach Pak 3 digital tachometer is a microcontroller-based instrument that features a scheme of adaptive period averaging. Response time above 100 Hz equals 50 msec; below 100 Hz, response time is governed by the input frequency. Measurement range spans 0.625 Hz to 30 kHz. The unit will accept input from magnetic sensors, TTL-output sensors, or almost any frequency-output device. $805. **Philips Technologies,** Cheshire Industrial Park, Cheshire, CT 06410. Phone (203) 271-6000. FAX (203) 271-6100. **Circle No. 397**

Storage cases. Models 235 and 285 are designed to store, transport, and protect as many as six 3½-in. disks. The devices are held firmly in place by a press-fit, capacity-detent action in two inside-cover trays. An open, nonpartitioned rear cover will hold any size IC. The rear tray is lined with polyethylene

foam. The 235 and 285, from $16.95 and $18.95, respectively. **Itoi Enterprises,** Box 59, Newton Highlands, MA 02161. Phone (617) 332-1010. **Circle No. 398**

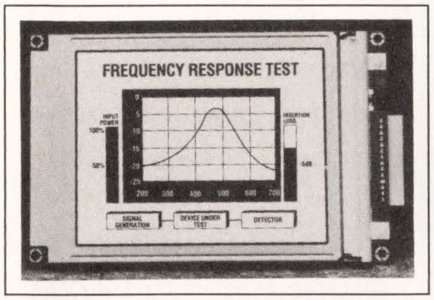
S/D converters. HSDC614 10- to 16-bit converters can be programmed on the fly and can track input rates as high as 600 readings/sec. Output accuracy equals 2 minutes of arc. A velocity output with a 1% linearity is standard. The units operate with reference inputs of 26V dc or 115V ac, and supply requirements equal 5V at 30 mA. $250 (OEM qty). **Computer Conversions Corp,** 6 Dunton Ct, E Northport, NY 11731. Phone (516) 261-3300. FAX (516) 261-3308. **Circle No. 399**

Fault indicators. MC25 and MC26 built-in, test-equipment nonvolatile indicators feature a slanted face and a sealed display that's highly visible in ambient light conditions. Once triggered by a 20-msec pulse to set the display, the units require no power. You reset the indicators by pulsing the reset coil. Operating range spans 0 to 71°C, and lifetime is specified at 4×10^6 transfers min. From $9.10 (1000). **Minelco Inc,** Box 459, Thomaston, CT 06787. Phone (203) 283-8261. FAX (203) 283-6527. **Circle No. 400**

Inductor kit. Series 32 surface-mount inductors come in a kit that contains 6 samples of 49 available inductors, which have values ranging from 0.1 to 100 μH. Tolerance equals ±10%. All units have modified J leads. Packages are epoxy molded and feature an inductance value marking. Kit, $120. **Gowanda Electronics Corp,** 1 Industrial Pl, Gowanda, NY 14070. Phone (716) 532-2234. **Circle No. 401**

Chip capacitors. The MCH 18 comes in values from 0.5 to 560 pF for NPO dielectrics, as well as 200 to 6800 pF for X7R dielectrics. Tolerances for NPO and X7R devices equal 5 and 10%, respectively. Operating range spans −55 to +125°C. The chips are supplied in 8-mm tape-and-reel format. $0.025 to $0.035 (4000). **ROHM Corp,** Electronics Div, 3034 Owen Dr, Antioch, TN 37013. Phone (615) 641-2020, ext 117. **Circle No. 402**

Components & Power Supplies

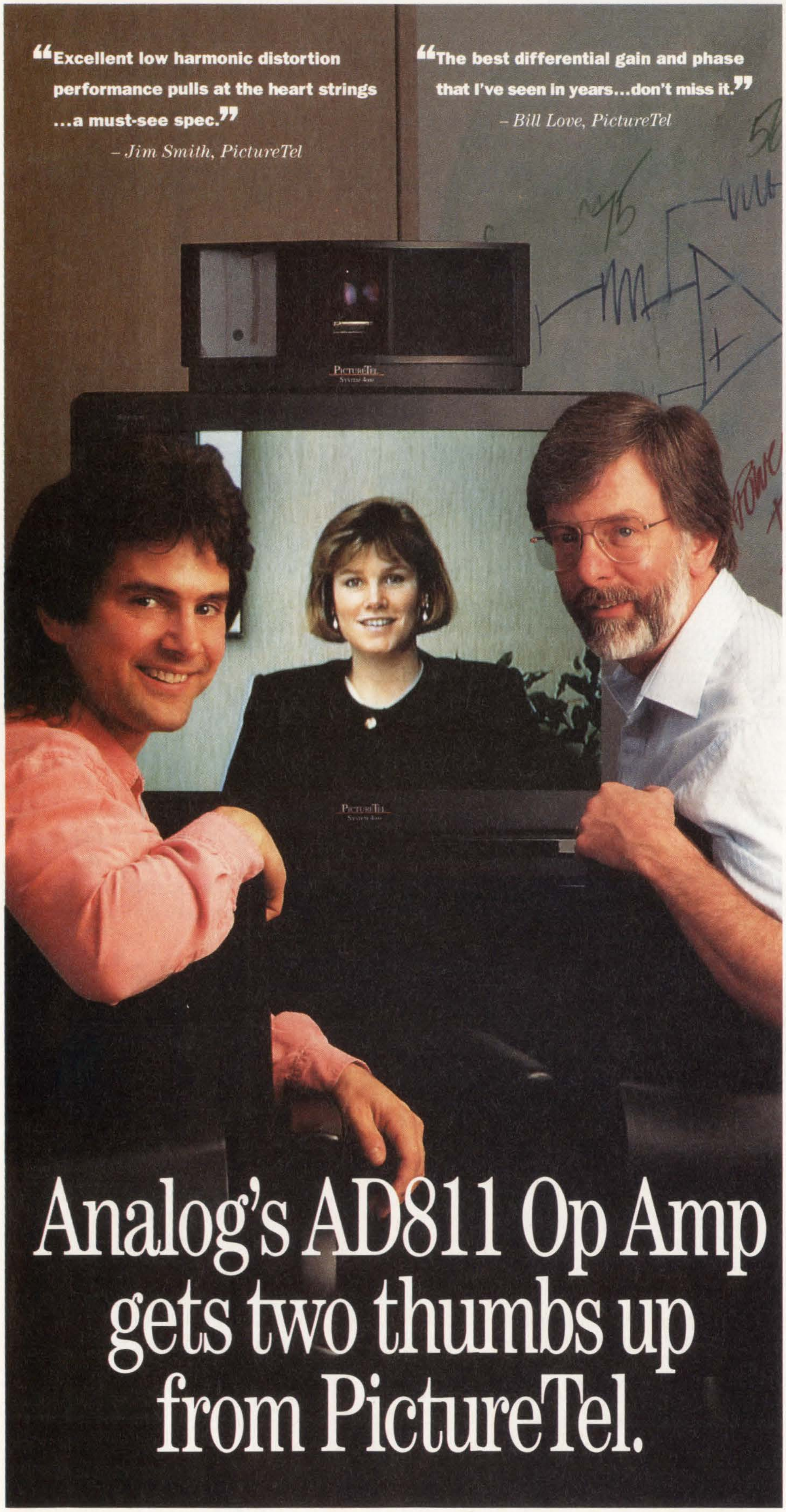


LCD module. The G321E has a 320× 240 dot-matrix format and features edge lighting. The module has an 8:1 contrast, a 100-cd/m² brightness, and operates on 5 and −22V supplies. The module measures 150×96×14 mm overall and weighs 195g. Operating range spans 0 to 50°C. $166 (100). **Seiko Instruments USA Inc,** LCD Dept, 2990 W Lomita Blvd, Torrance, CA 90505. Phone (310) 517-7829. **Circle No. 403**

Keyboard. Model MF-87 keyboards are IBM compatible. The 87-key unit employs membrane technology and has an IP rating of 54. The keycaps are mounted on 0.75-in. centers and have an operating life of 20×10^6 operations. $257. **Preh Electronic Industries Inc,** 470 E Main St, Lake Zurich, IL 60047. Phone (708) 438-4000. **Circle No. 404**

Power-supply input. The stand-alone Model PFC-555 features a 0.99 power factor and reduces harmonics in accordance with IEC 555-2 specifications. It handles inputs as high as 1300W for voltages of 90 to 264V ac and 2600W from 187 to 264V. Line and load regulation equal 0.3%, and efficiency measures 93% typ. $760. **Deltron Inc,** Box 1369, North Wales, PA 19454. Phone (215) 699-9261. **Circle No. 405**

MOSFETs. The FR406x line of rad-hardened MOSFETs includes four high-voltage types (FRL430, FRM440, FRF450, and FRK460) and four low-voltage units (FRS9130, FRS9230, FRS130, and FRS230). The high-voltage units have a $500V_{DS}$ specification and on-resistance values in the 0.4Ω range. $175 to $470 (50). **Harris Semiconductor,** Box 883, Melbourne, FL 32901. Phone (800) 442-7747. **Circle No. 407**



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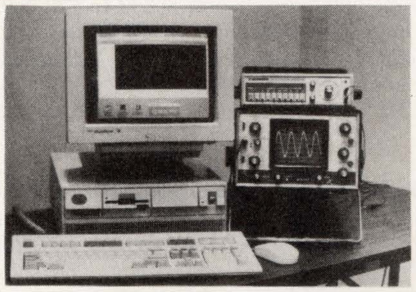
CIRCLE NO. 79

CAE & Software Development Tools



Real-time multitasking for Windows. Notebook and Notebook/XE achieve real-time sampling at rates to 1 kHz with no gaps in the 386-enhanced mode of Windows. The software lets you collect data, display the data in real time, simultaneously log the data to disk, and perform triggering and control decisions based on the input data. $4495; upgrade from Windows, $500; from DOS versions, $600. **Labtech,** 400 Research Dr, Wilmington, MA 01887. Phone (800) 769-5227; (508) 657-5400. FAX (508) 658-9972. TLX 989695.
Circle No. 434

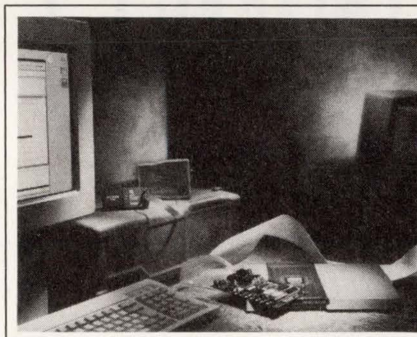
FPGA-design tool. Timing Wizard, a timing-driven design tool, automates the process of achieving operating frequencies for FPGA designs. The tool operates with the company's FPGA Foundry system to place and route FPGA designs automatically. As an option combined with FPGA Foundry, approximately $5000. **NeoCAD Inc,** 2585 Central Ave, Boulder, CO 80301. Phone (303) 442-9121. FAX (303) 442-9124.
Circle No. 435

Statistical fault-grading tool. Quickgrade II allows the user to measure and obtain test coverage of large, complex ASICs and pc boards. The software, used in conjunction with the company's Falcon Framework for Concurrent Design and Simview, graphically locates undetected faults. From $14,900. **Mentor Graphics,** 8005 SW Boeckman Rd, Wilsonville, OR 97070. Phone (503) 685-7000. **Circle No. 436**

Software library for HP-UX. The 1992 HP-UX Contributed Software Library contains 47 programs (23 directly from HP). Programs include an electronic-mail interface, an AGP to Starbase library, information mail server, X11 revision 5, system security audit tool, and Perl 4.0 language and utilities. The library is available in 1600- or 6250-bpi magnetic tape, Linus cartridge tape (CS-80), and 4-mm digital audio tape. Annual fee for HP-UX members with site-level service, $495. **Interex,** Box 3439, Sunnyvale, CA 94088. Phone (800) 468-3739; (408) 738-4848. FAX (408) 736-2156. TLX 4971527 **Circle No. 437**

Source-level debugger. Freeform/Simulator, a new version of Freeform, allows you to embed code for the Motorola 68000 family processors before the target hardware is available. Software for MS-DOS workstations, $2300; for Unix workstations, $3600. **Software Development Systems Inc,** 1211 W 22nd St, Suite 610, Oak Brook, IL 60521. Phone (708) 990-4640. FAX (708) 990-4640. **Circle No. 438**

Applications-development software. Smalltalk/V for Windows 3.1 allows you to write programs in Windows. In addition to standard features, this version of the software provides Windows multiple-document interface; Toolpane; Statuspane, which displays the status of applications; and Objectfiler for sharing objects with other applications and developers. For Windows version 2.0, $499.95; user upgrade, $195. **Digitalk Inc,** 9841 Airport Blvd, Los Angeles, CA 90045. Phone (310) 645-1082. **Circle No. 439**



Microprocessor development tools. A set of development tools for Intel's 80C186/188 and 80C186/188EB microprocessors includes Validate/XEL integrated debugger interface, an optional optimized C compiler, an instruction set simulator, Codetap (an in-circuit tool for debugging embedded code), and EL 1600 emulator. The tools are based on the company's emulation-link architecture, which provides network accessibility and a high-level-debugging capability. $2000 to $18,400. **Applied Microsystems Corp,** Box 97002, Redmond, WA 98073. Phone (800) 426-3925; (206) 882-2000. **Circle No. 440**

Tool kit. You can use the Mips R3000 RISC (reduced-instruction-set-computer) Software Development Toolkit for embedded development. It has an ANSI C cross-compiler, an assembler, a locating linker, a software floating point, downloadable format generation, and a multiwindow high-level-language debugger. PC-DOS package without debugger, $3495; PC-DOS remote-debugger package, $3495; Unix versions, $4700 to $7000; multiuser systems and file servers, $6300 to $28,000. **Boston Systems Office/Tasking,** Norfolk Pl, 333 Elm St, Dedham, MA 02026. Phone (617) 320-9400. FAX (617) 320-9212. **Circle No. 441**

Software development tools. The Intertools C cross-compiler tool kit is a third-party product for the 77220, 77230, and 77240 processors. The software provides an ANSI C cross-compiler, an NEC-compatible cross-assembler, runtime libraries, and programming utilities. The tools are available for Sun workstations and IBM PCs. From $2500; XDB source-level cross-debugger, $2300. **Intermetrics Microsystems Software Inc,** 733 Concord Ave, Cambridge, MA 02138. Phone (800) 356-3594; (617) 661-0072. FAX (617) 868-2843. **Circle No. 442**

Ada source-code management. ADC/Adascan, an option for Aide-De-Camp, lets you identify and track relationships between the components of Ada programs. Platforms include IBM RS/6000, DEC RISC Ultrix, Sun-SPARC, HP, Silicon Graphix Unix, Intel 386/486-based Unix, 88open Unix, and Mips Unix. $2195. **Software Maintenance and Development Systems Inc,** Box 555, Concord, MA 01742. Phone (508) 369-7398. FAX (508) 369-8272. **Circle No. 443**

ISDN system adapter. The ISDN (Integrated Services Digital Network) System Adapter version 1.1 now comes with a Macintosh configuration program to accompany the DOS configuration program. The adapter is an external multimedia adapter with voice and data capabilities for AT&T and Northern Telecom ISDN switches and uses the company's standard AT command set of ISDN and Autostream. $1599. **Hayes Microcomputer Products Inc,** Box 105203, Atlanta, GA 30348. Phone (404) 441-1617. FAX (404) 441-1238. **Circle No. 444**

Analog interface kit. Analog Interface Kit integrates Mentor's Falcon Framework with Anacad's Eldo circuit simulator to provide high-performance electrical-circuit and analog-behavioral simulation. Anacad license fee, $5000; Mentor license fee, $11,900. **Mentor Graphics,** 8005 SW Boeckman Rd, Wilsonville, OR 97070. Phone (408) 451-5649. **Circle No. 445**

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CIRCLE NO. 100

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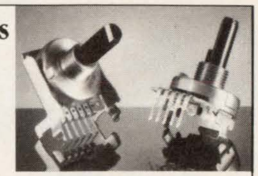

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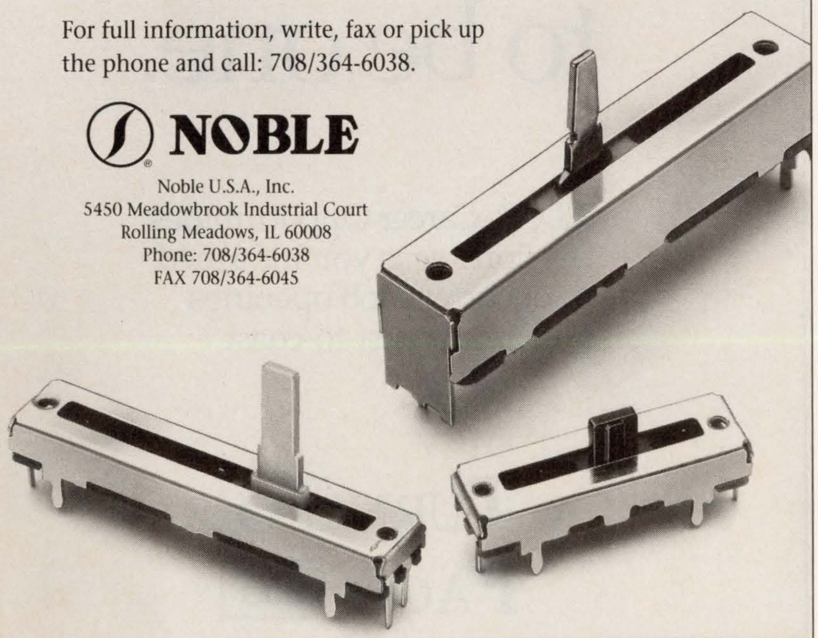
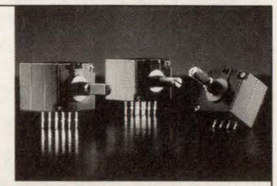


CIRCLE NO. 104



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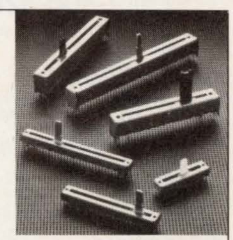

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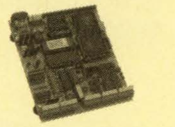

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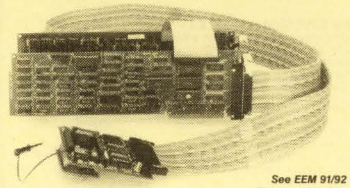

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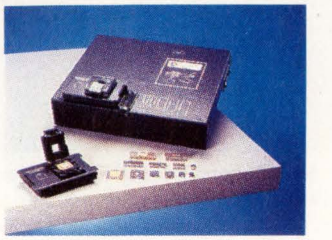

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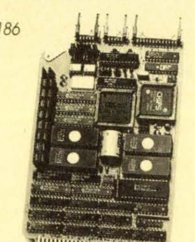

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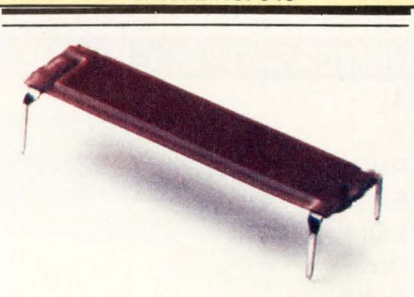

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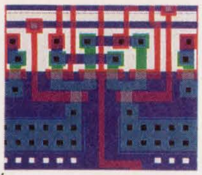

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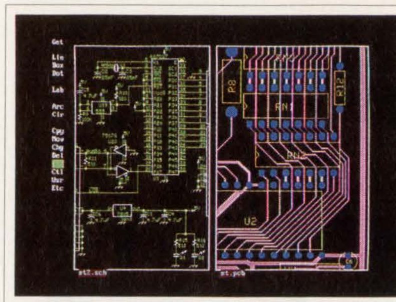

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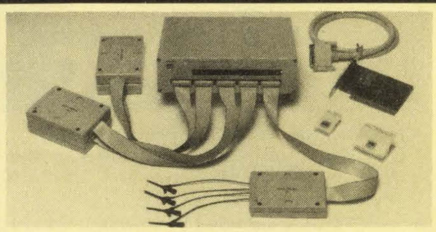

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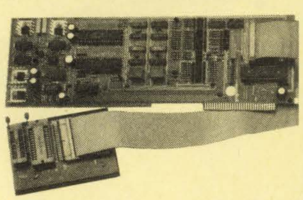

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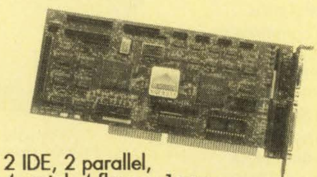

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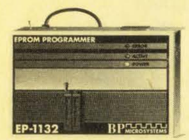

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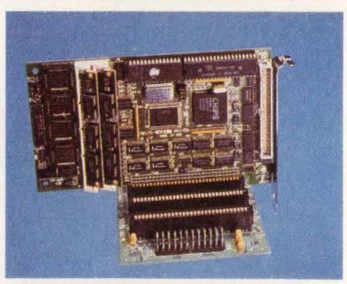

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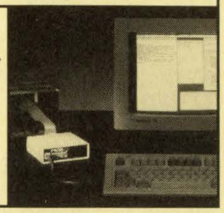

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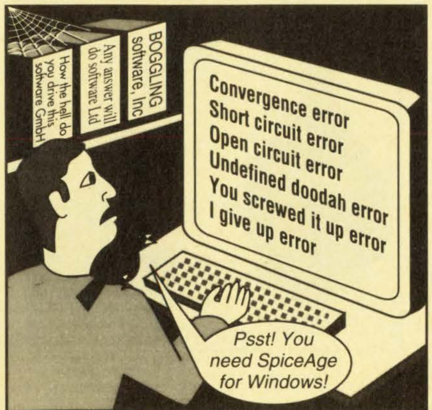

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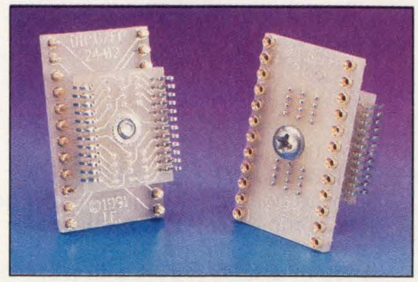

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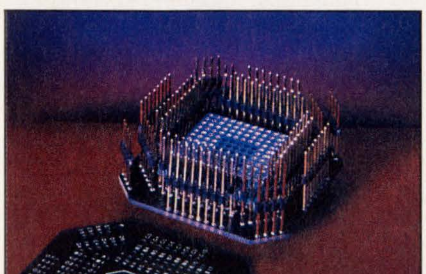

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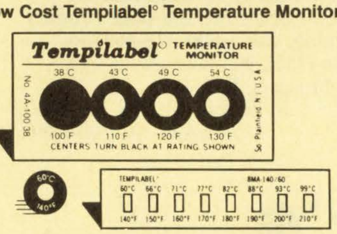

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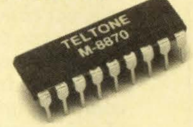

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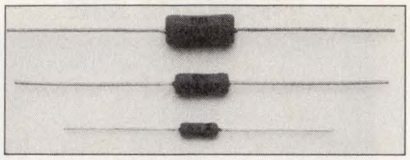

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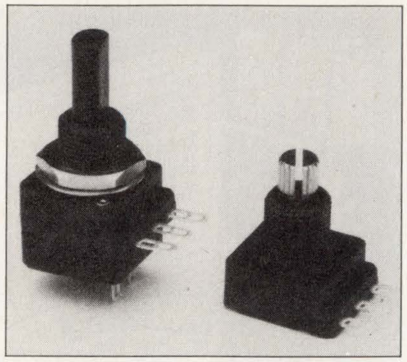

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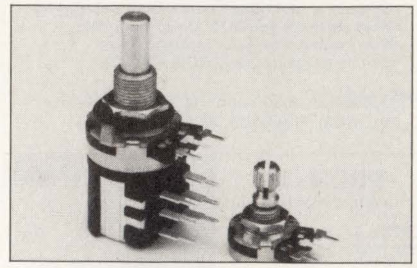

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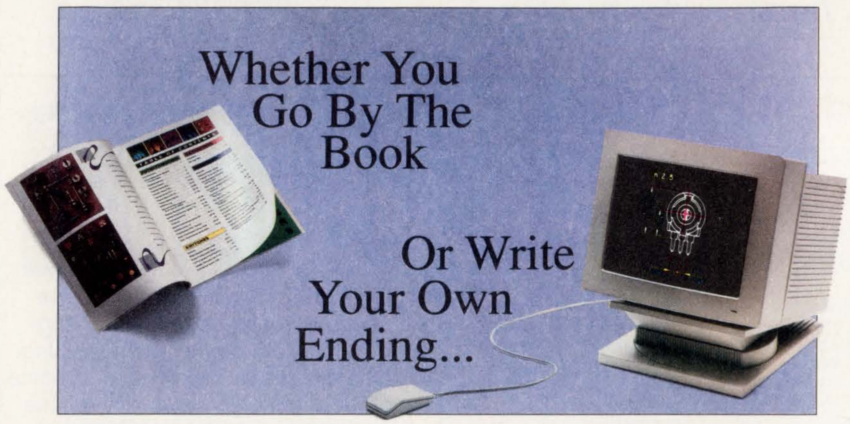

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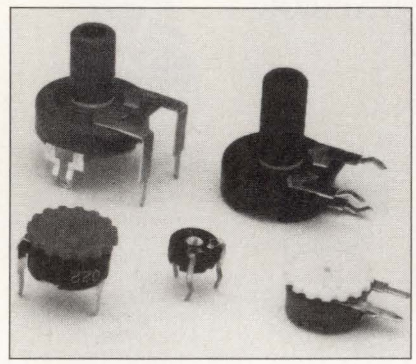

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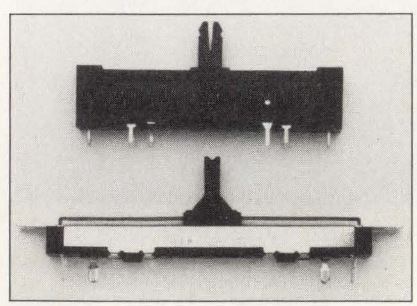

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Magazine Edition	Oct. 29	Oct. 8	ELECTRONICA SHOW ISSUE • Object-oriented Programming • Chipsets for PCs Design it Right Series—Part III Wescon Preview Issue
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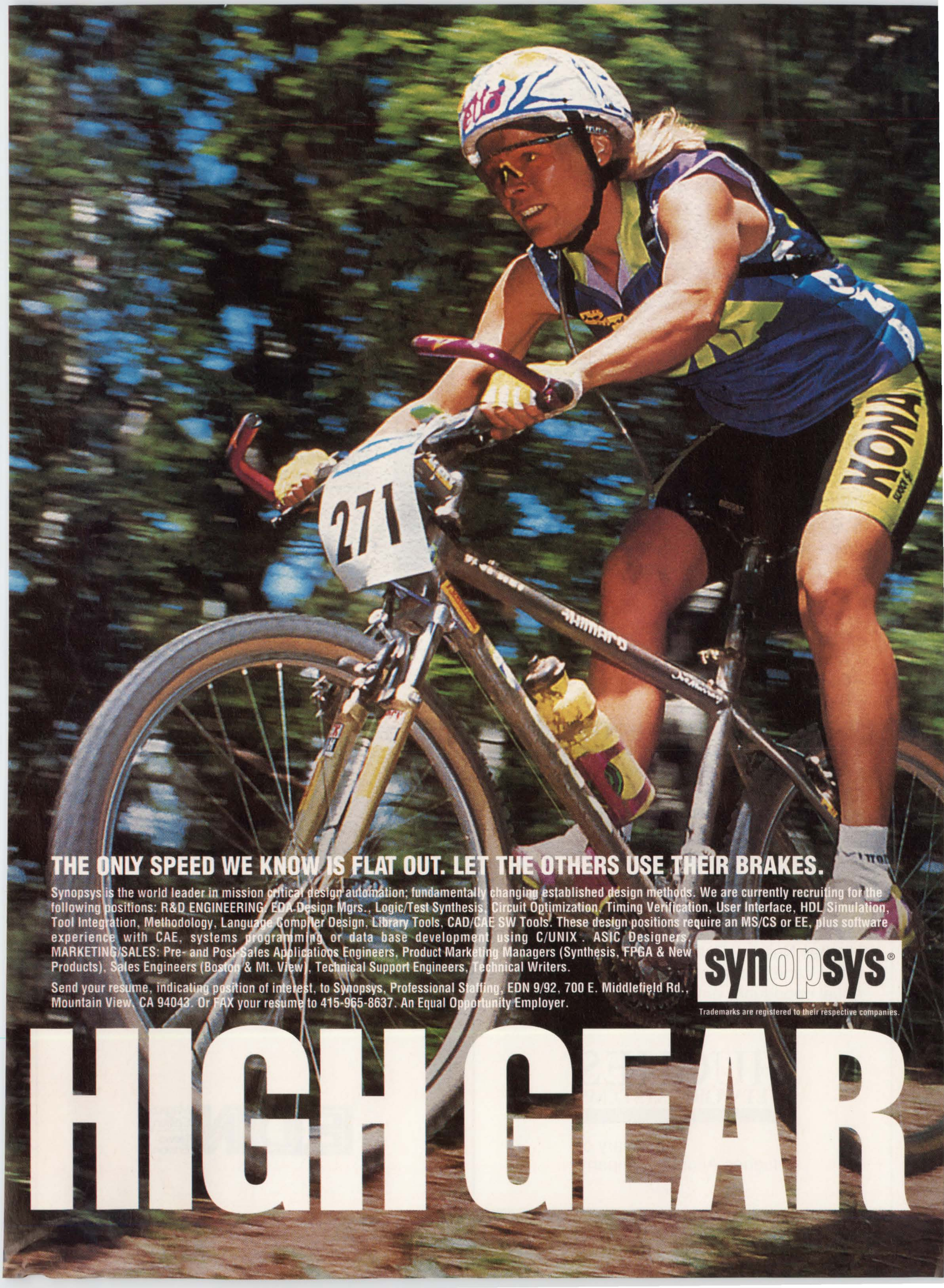
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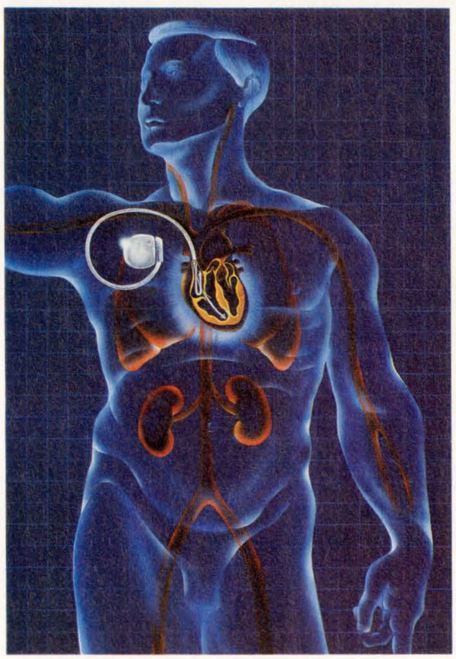

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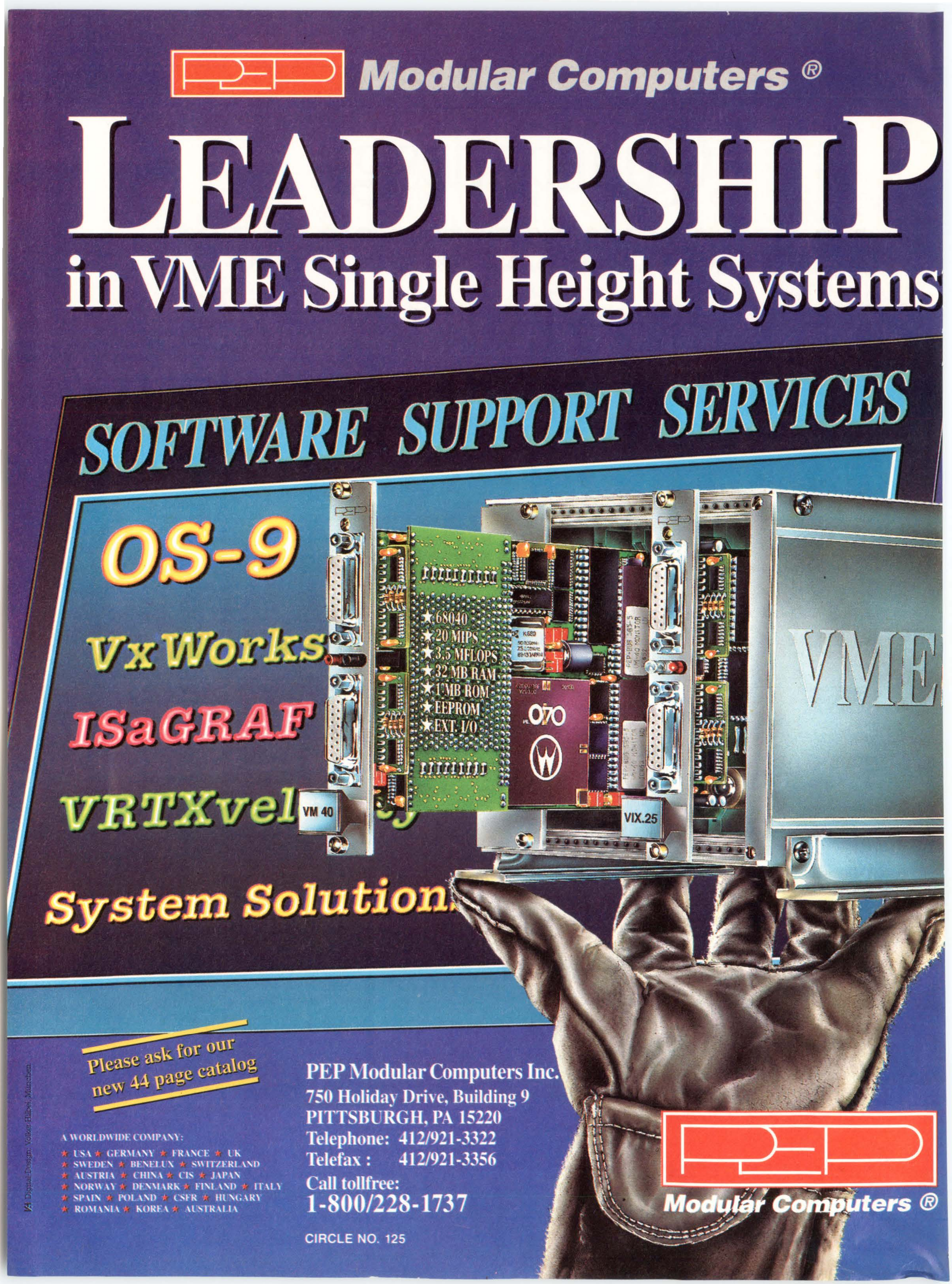
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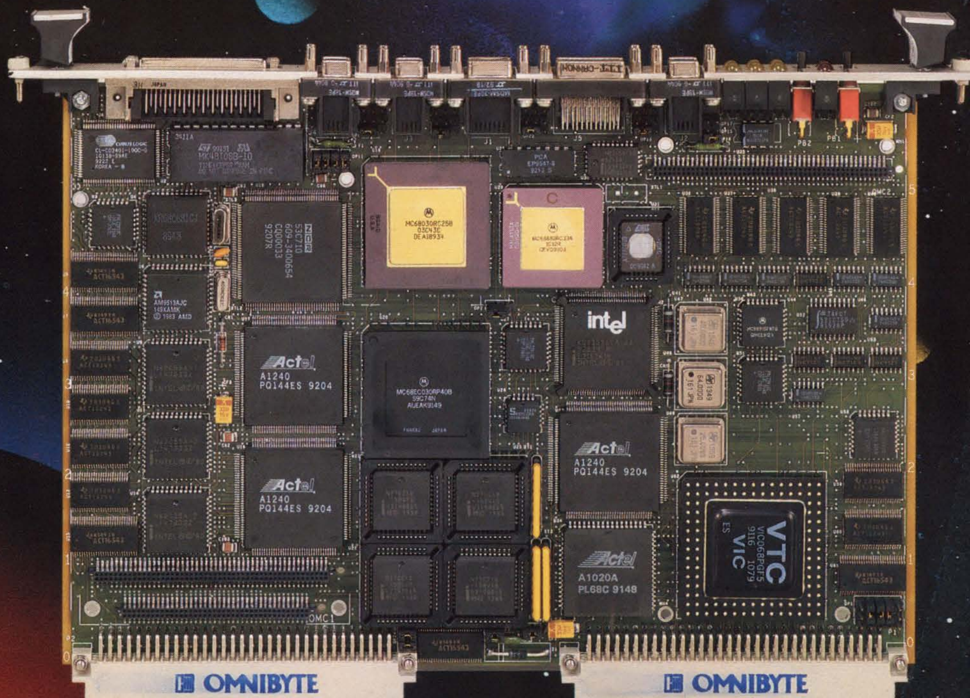

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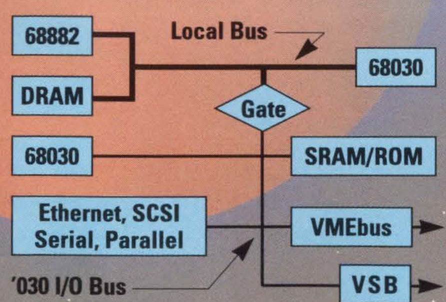

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Software	VxWorks[1], UNIX[2], OS-9[3], CrossCodeC, FreeForm[4]

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A/D—analog to digital
ADC—analog-to-digital converter
ALU—arithmetic and logic unit
ASIC—application-specific integrated circuit
BTL—backplane transceiver logic
CD-ROM—compact-disc, read-only memory
CISC—complex-instruction-set computer
CMOS—complementary metal-oxide semiconductor
CPU—central processing unit
CSR—control and status register
DAC—digital-to-analog converter
DAT—digital audio tape
DoD—Department of Defense
ENOB—effective number of bits
FSM—finite state machine
HDL—hardware-description language
IC—integrated circuit
IDE—integrated device electronics
IEEE—Institute of Electrical and Electronics Engineers
JTAG—Joint Test Action Group
LAN—local-area network
LSB—least significant bit
MESI—Modified Exclusive Shared Invalid
MIPS—million instructions per second
MSB—most significant bit
NAND—not AND
NASA—National Aeronautics and Space Administration
NGCR—Next-Generation Computer Resources
NOR—not OR
NTDS—Navy Tactical Data Systems
OEM—original equipment manufacturer
PC—personal computer
PLA—programmable logic array
PLD—programmable logic device
QIC—quarter-inch cartridge; also the name of a minicartridge-tape-drive industry group
RAM—random-access memory
RISC—reduced-instruction-set computer
rms—root-mean-square
ROM—read-only memory
RTL—register-transfer level
SCSI—Small Computer System Interface
SEM-E—Standard Electronics Module
S/H—sample and hold
SHL—shift left
S/N—signal to noise
SPAWAR—Space and Naval Warfare Systems Command
SPICE—simulation program with integrated-circuit emphasis
SU—standard unit (25 mm)
THD—total harmonic distortion
TTL—transistor-transistor logic
U—Eurocard (1.75 in.)
VHDL—VHSIC hardware-description language
VHSIC—very high-speed integrated circuit

ASIC development book skimps on the meat and confuses the facts

Surviving the ASIC experience by John Schroeter attempts to cover a broad topic: integrated circuits "designed by the end user, *specifically for his proprietary application*" (author's emphasis). The topic is both the book's strength and weakness. The result is a quick tour of the entire spectrum, from ASIC design methodologies, processes, and packaging to verification and production testing. Any one of these areas is worthy of its own book.

I had hoped, based on the book's title and the highlights printed on the cover, that this book would give me insight into how others viewed the risk-management process in ASIC development. I wanted to recommend the book to prospective customers as a reference to help educate them as to the risks involved in ASIC development.

There is a clear need for risk management education in the customer base. The Quality Director in my organization has commented to me that several large, technically sophisticated customers have asked him, "Why didn't anyone tell us about the risks involved?" Although it does explain some of the risks, this book spends more time describing ASIC process options than it devotes to explaining how to manage the development risks proactively.

The material covered in this book is inconsistent with what I presume to be the information needed by the target reader. For a prospective ASIC designer, the material about technically sophisticated packaging options, such as TAB (tape automated bonding) or COB (chip on board) in chapter 4, conflicts with the book's title theme, which is survival. Let someone who's done a few ASIC designs tackle tough packaging and production options. Spare the novice. Surprisingly, beryllium-oxide packages are mentioned for their superior thermal conductivity, but the book fails to mention toxicity or potential regulatory problems associated with that packaging material.

Material in this book is sometimes presented out of sequence. The discussion in chapter 10 of ASIC cost determination should appear in the front of the book because the choice to proceed with ASIC development is always economic, whether for reducing costs or as an enabling technology. In either case, the benefits of using an ASIC must be compelling and must be understood at the beginning of a design project. Woe to the engineer who doesn't understand the economics of ASIC development.

The discussion of time-to-market issues in chapter 7, "Design Guidelines and Issues," should be expanded and brought forward in the book as well. Understanding the impact of schedule slippages deserves more than the one example given. The example states that if a product has a lifetime of 18 months and an anticipated revenue of $10M, an 8-week slip costs 10% of the revenue (linear with time). Actually, this lost-revenue figure is wrong—it will be much worse—and the book should explain why in the beginning.

Graphics could have been used for better clarity in several places. For example, I think a flowchart of the IC manufacturing cycle that points out where each customization option takes place for gate arrays, custom designs, and FPGAs would have been helpful in explaining the tradeoffs among these products. A graphic presentation would also have helped the discussion of analog simulation by showing the hierarchy of simulation methods: behavioral, cell-based, schematic-level, and polygon-level. Such a graphic could also show the need for interaction and verification among these methods.

Unfortunately, Chapter 2, "Selecting the ASIC Methodology," mentions back annotation but doesn't explain it. Chapter 5, "Selecting the ASIC Design Tools," also mentions back annotation but doesn't really explain the rationale for using it. Back annotation is a part of ASIC design that deserves more explanation because there are potential risks and pitfalls in the extraction of parasitic capacitance and resistance from the design's polygon level for resimulation at the schematic level.

Also, I think the author's attention to detail could be better. The directory of ASIC vendors in Appendix B mentions only US suppliers. It should also mention Seiko, Hyundai, and TSMC (Taiwan Semiconductor Manufacturing Co). My firm also was not mentioned (obviously, I have some work to do). Harris and Orbit are also missing. The directory of CAE vendors in Appendix D omits Synopsys, which is unfortunate because that company supplied Figure 5.3, even though the credit misspells the name.

In several cases, I disagree with the author's statements of fact. For example, on page 64 the book states that most vendors specify a maximum T_j (junction temperature) of 125°C. I know of no vendor specifying this maximum junction temperature, and it directly conflicts with military specifications that call for a maximum ambient operating temperature of 125°C. It's not possible for the ambient and junction temperatures to be the same. Most silicon processes specify a maximum T_j of 150°C, although operating chips at such a high temperature isn't recommended.

On page 172, the author states: "There is a substantial learning curve for ASIC manufacturing. This learning curve is complicated further by the small production runs typically associated with ASICs. The process flow must be stopped, started, and restarted for every unique production lot on the line."

This statement directly contradicts my experience. The point of wafer fabrication is to run the same process, or minor variants, at all times so that each wafer lot gets the same processing. No self-respecting fab manager would set up and tear down process flows on a lot-by-lot basis. Added costs associated with small lot sizes might occur further down the production line where small lot sizes, package diversity, and test options result in complexity, hence increased cost.

I do like the book's breadth of coverage. For someone who has not spent much time in the industry or is completely new to ASICs, this book provides a quick overview, especially for digital ASICs and some of the buzzwords. After a quick reading, a prospective ASIC designer should then find reputable vendors and deal with the specifics of his or her project. ASIC vendors survive only if their customers survive.—**Dave FitzGerald**

Surviving the ASIC Experience, John Schroeter, Prentice Hall, Englewood Cliffs, NJ, 1992, 205 pg.

Dave FitzGerald is a mixed-signal marketing manager at Analog Devices, Inc. He has many years of technical marketing experience, especially to the Japanese market, and previously was a design engineer.

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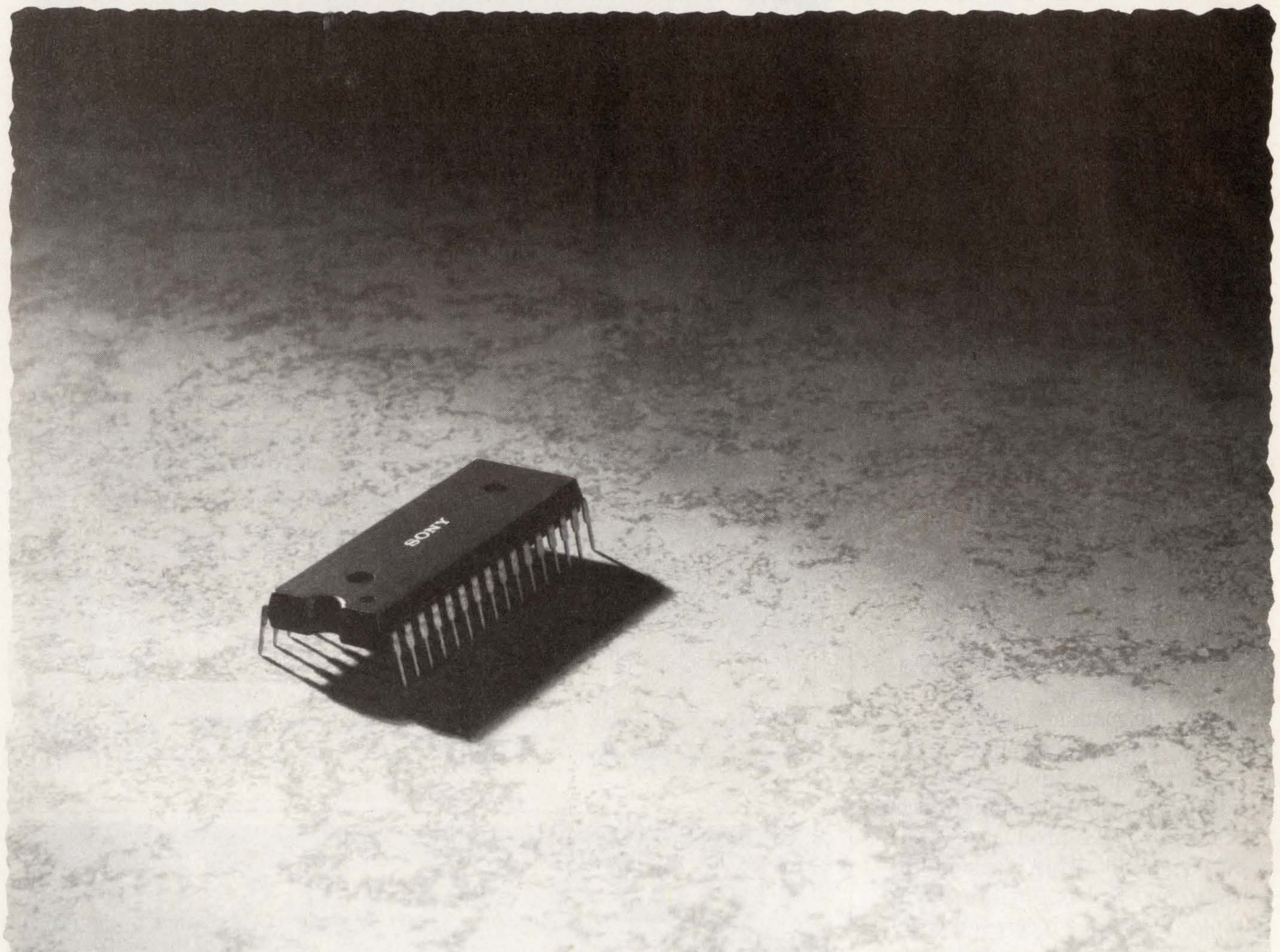

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Model	Speed (ns)	Package	Standby Current (µA)	Special Features
CXK581000P	100/120	DIP 600 mil	12/50	-25° - +85°C
CXK581000M	100/120	SOP 525 mil	12/50	-25° - +85°C
				-40° - +85°C
CXK581100TM	100/120	TSOP	12/50	
CXK581100YM	100/120	TSOP (rev.)	12/50	
CXK581001P	70/85	DIP 600 mil	12/50	
CXK581001M	70/85	SOP 525 mil	12/50	
CXK581020SP	35/45/55	DIP 400 mil		
CXK581020J	35/45/55	SOJ 400 mil		
CXK581021J	47	SOJ 400 mil		
CXK581120J	15/17/20	SOJ 400 mil		
CXK77910J	20	SOJ 400 mil		Sync., 128K x 9

Note: All packages 5V, 32 pin, 128K x 8, unless otherwise noted.

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CIRCLE NO. 130

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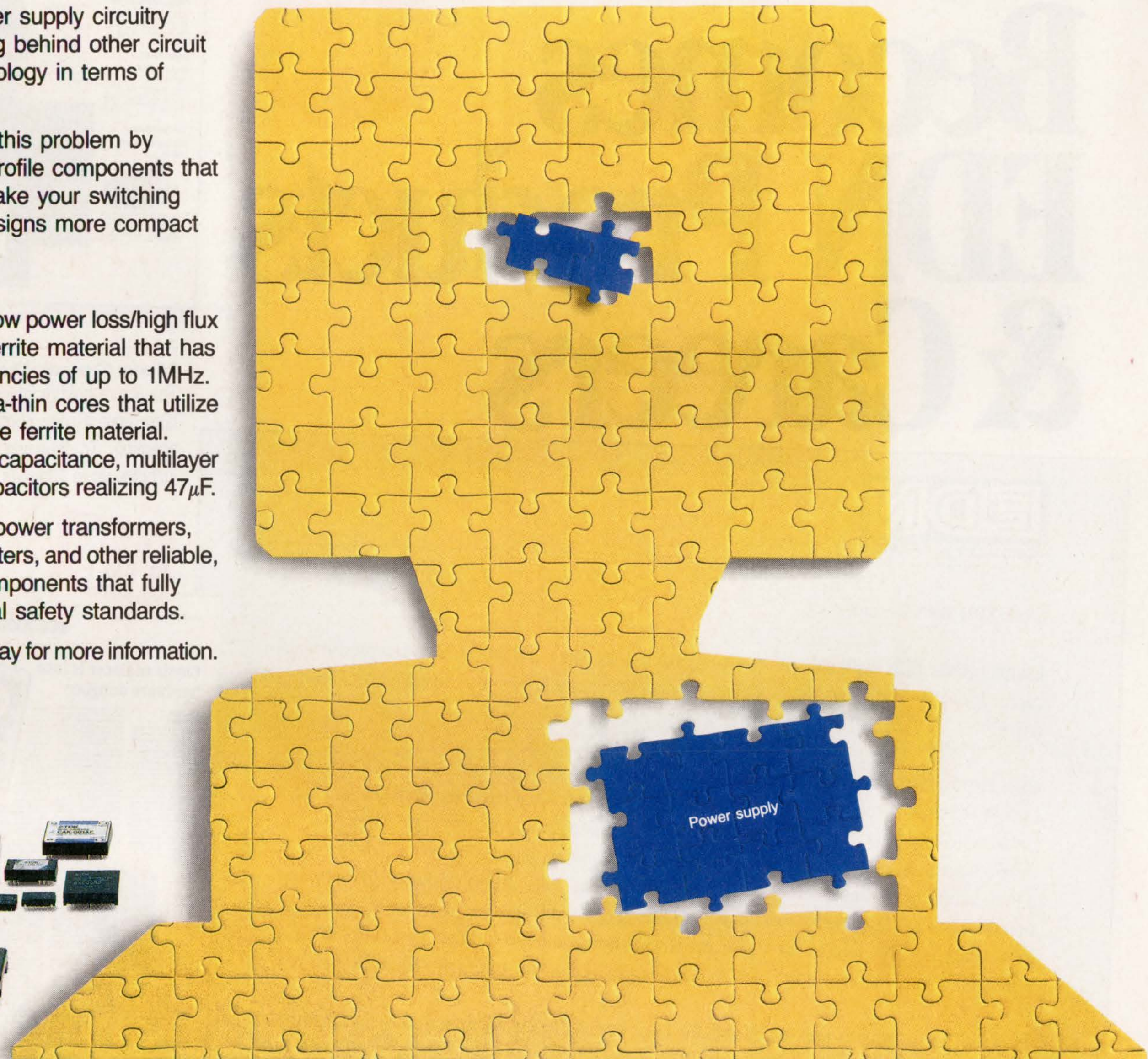
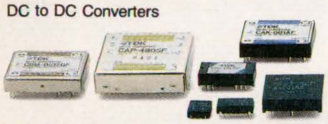
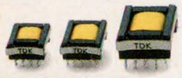


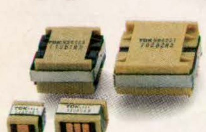
DC to DC Converters



Power Transformers



Current Transformers



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CIRCLE NO. 131

On October 8 EDN News Becomes EDN Products & Careers

Take a look!! →

New Cover Design:

The use of bold graphics, an enhanced typeface and large scale 4-color photography will grab your attention. To draw you inside the issue, the cover includes up to 13 starts or story pointers.

Executive Engineer:

A regular personality profile of a successful engineering executive. They'll tell how they devised their own roadmap for success—and how others can do the same.

EDN
PRODUCTS & CAREERS

JOHN C. WHITMARSH
Editor

Dear EDN News Reader,

Exciting News! EDN's tabloid edition is going back to its roots--a publication with a product and career focus. Beginning with our October 8 issue, EDN News Edition will become EDN Products & Careers.

EDN Products & Careers will belong to you.
EDN Products & Careers matches your professional and personal interests. We'll give you the "what with" and "by whom" information you need by identifying products and professional developments. And, we'll deliver this information in a unique, interactive format. For example, take a look at our new Snapshot Surveys. These regular reader polls give you a chance to state your opinion on important management and technical issues of the day. And… notice the new Product Preference Surveys-- here's where your peers who use certain products evaluate them. No other publication allows its readers to have so much say in its content. And there's more--lots more.

Take the time to get pre-acquainted with the issue by reading the editorial feature explanations on the next page. You'll see that EDN Products & Careers has a lot to offer. Features such as the Buyer's Guides and the Technical Product Sections as well as the expanded Career Section are sure to interest you. And of course, it will complement the important design application information you'll continue to receive in EDN Magazine.

I know you'll be as excited as we are when the premiere issue hits your desk on October 8th. Tell us what you think about your new publication. Your comments and suggestions are always welcome.

Sincerely,

John Whitmarsh
Editor, EDN Products & Careers

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