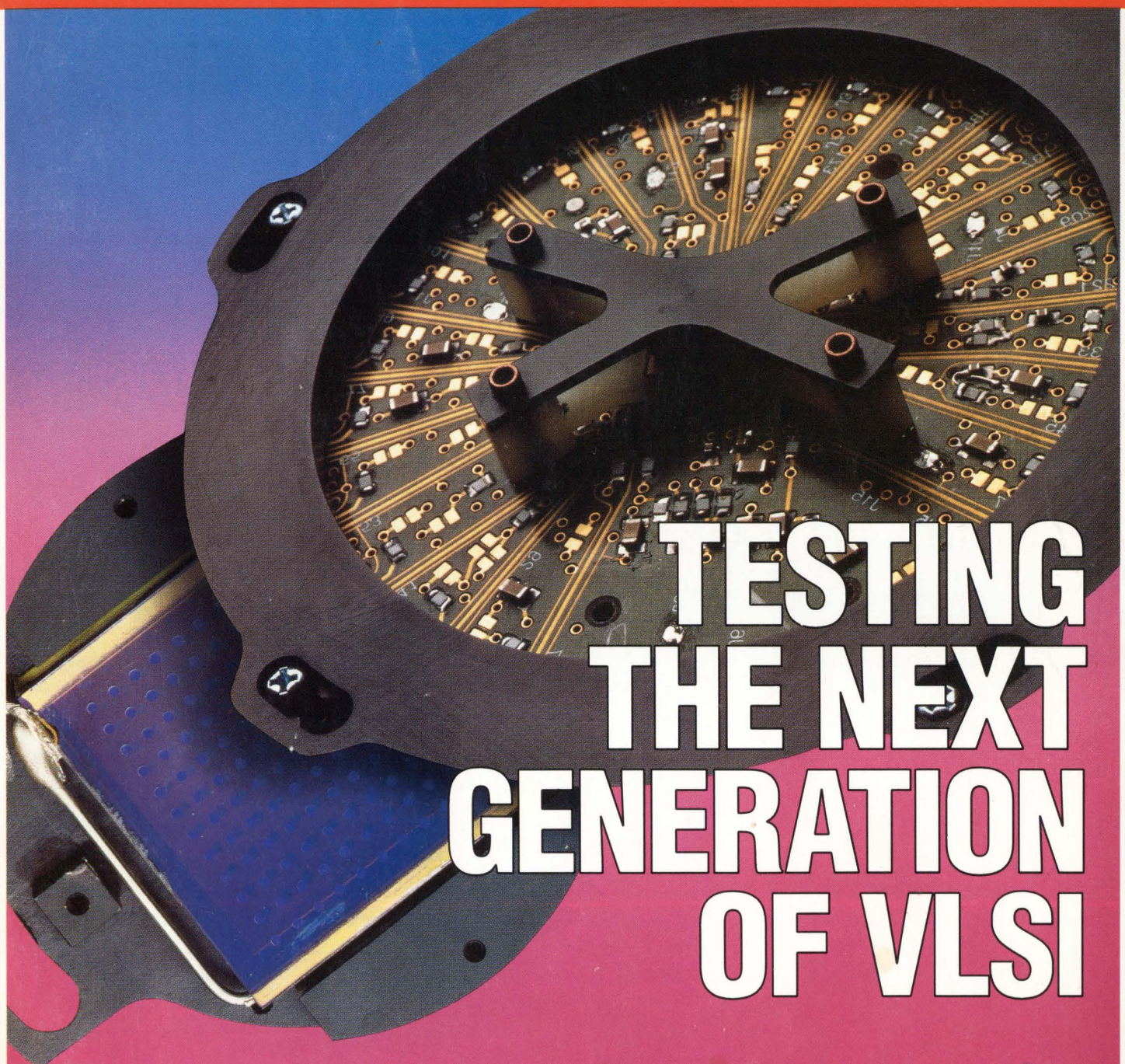
PROCESSOR DOES 1024-POINT FFTs IN 0.5 MS

BUILD AN ETHERNET PORT ON THE SCSI BUS

ELECTRONIC DESIGN

A VNU BUSINESS PUBLICATION

SEPTEMBER 8, 1988



TESTING THE NEXT GENERATION OF VLSI

- ELECTRO-OPTICS GIVE GHz MEASUREMENTS
- SPECIAL REPORT ON ASIC VERIFIERS
- DESIGNING OCTAL DACs INTO HIGH PIN-COUNT ATE

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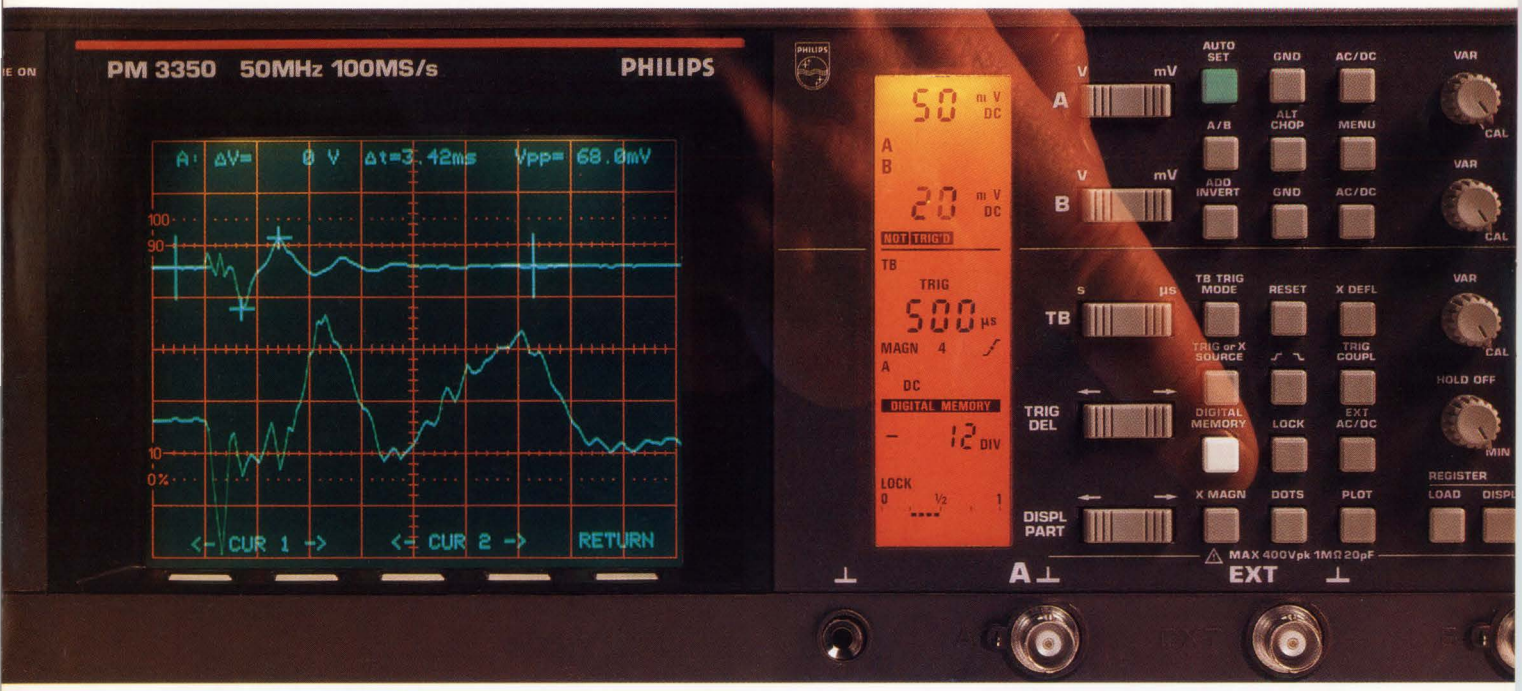

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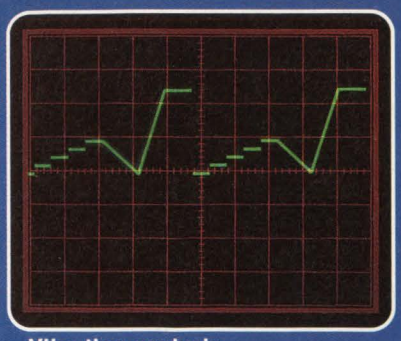
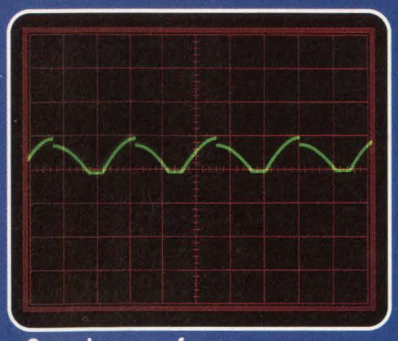
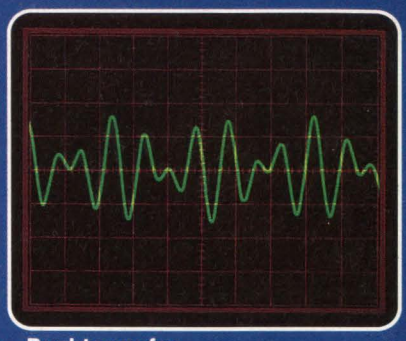
CIRCLE 131



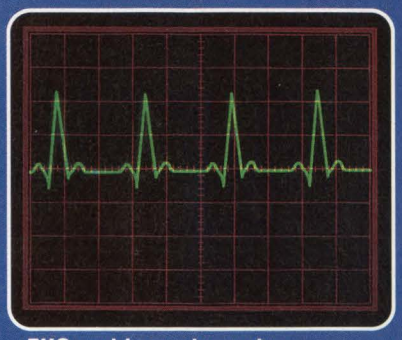
Vibration analysis with stop and hold.



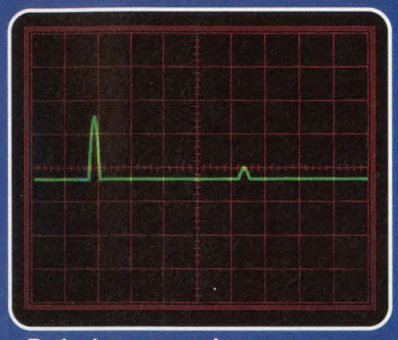
Complex waveforms for servo drives.



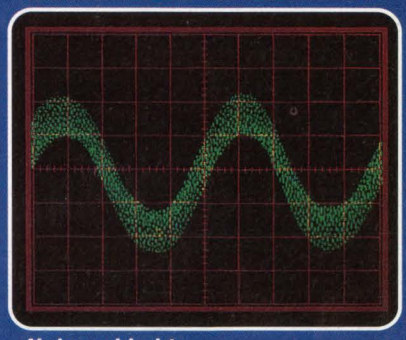
Dual tones for telephone testing.



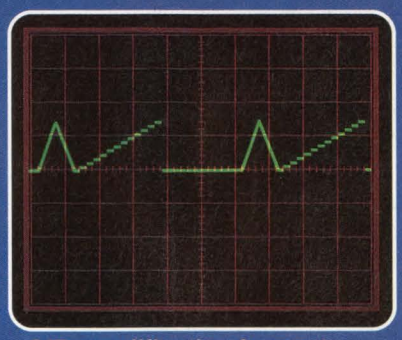
EKG and hemodynamic waveforms.



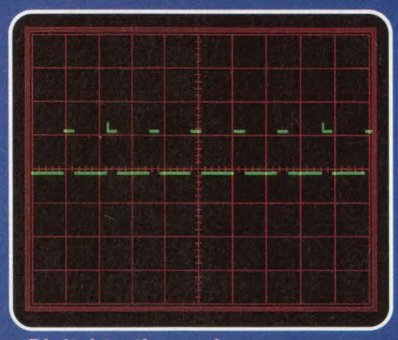
Radar/sonar envelope simulation.



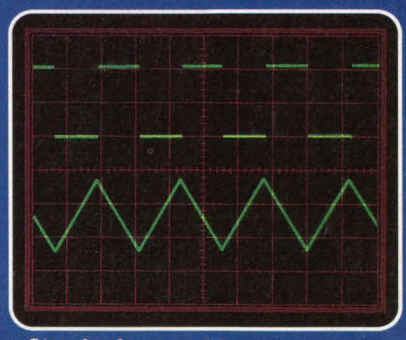
Noise added to any waveform.



A/D, amplifier development and calibration.



Digital testing and troubleshooting.



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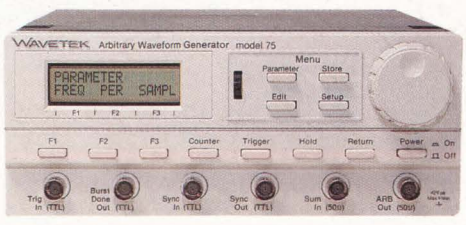

Waveforms are stored in nonvolatile memory, with more than 4,000 vertical points and 8,000 horizontal points of resolution. They can be played back at any rate, up to 500ns per point.

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CIRCLE 3 FOR DEMONSTRATION

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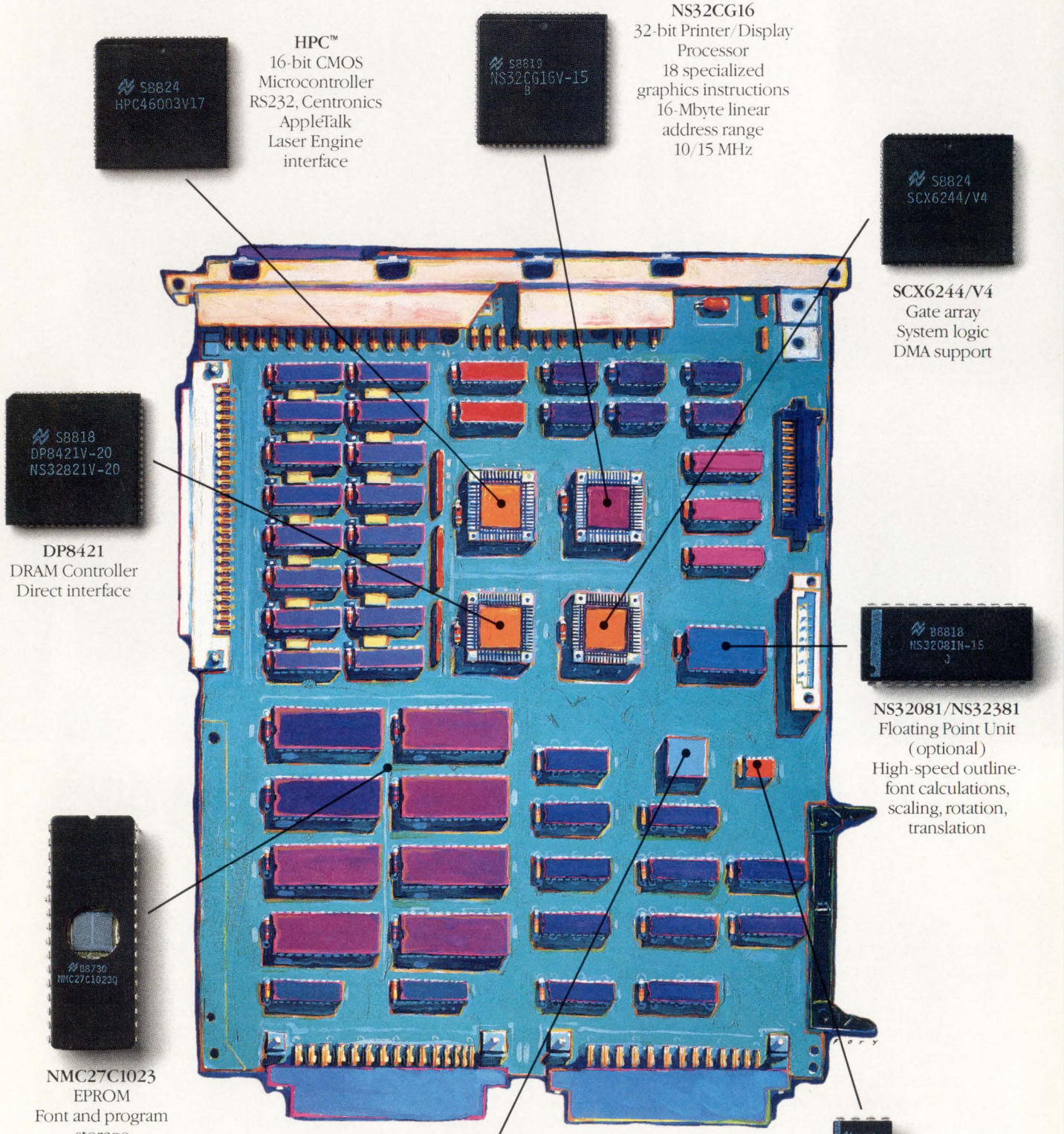

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AppleTalk
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graphics instructions
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address range
10/15 MHz

SCX6244/V4
Gate array
System logic
DMA support

DP8421
DRAM Controller
Direct interface

NS32081/NS32381
Floating Point Unit
(optional)
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font calculations,
scaling, rotation,
translation

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EPROM
Font and program
storage
Printer diagnostics

DP8510/11
BitBLT
Processing Unit
(Accelerator)
(optional)
Very fast bit-aligned
block transfers

NMC9346
EEPROM
Printer set-up
Page-volume data

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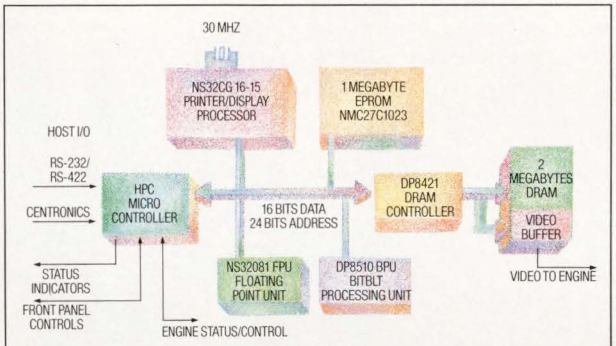
The only fully programmable 32-bit, CMOS microprocessor tuned for graphics applications.

And the heart of the most cost-effective systems solution for a full range of imaging designs.



The NS32CG16 is the heart of a high-performance, cost-effective systems solution for applications like this page-printer controller.

ALL TOGETHER: THE CHIP

The NS32CG16 combines the programmability of a high-performance 32-bit microprocessor with the power of a specialized graphics coprocessor. It includes 18 dedicated graphics instructions for:

- bit-aligned block transfers (BitBLT) with 16 logical operations for high-speed character moves and windowing
- line drawing (9 Mbits/sec)
- pattern drawing, replication, and filling (60 Mbits/sec)
- pattern magnification to support Epson and HP LaserJet™ emulations (1X, 2X, 3X, 4X)
- binary data compression/expansion for compact font storage under run-length-limited (RLL) encoding
- supports CCITT Group III and IV protocols for facsimile transmission
- on-chip clock generator
- programmable power-down modes
- on-chip DMA support circuitry.

A true 2-address machine (for direct memory-to-memory graphics operations), the NS32CG16 has a 16-Mbyte linear address space to support large font storages, high-dpi (dots-per-inch) page buffers, and memory-intensive page-description languages (PDLs).

ALL TOGETHER: THE PERIPHERALS

The NS32CG16 is supported by a full range of peripheral devices, available now:

- hardware floating-point coprocessors for high-speed outline-font calculations in PDLs like PostScript™ and PCL™
- DRAM controllers
- single-chip I/O support for RS232 Serial, Centronics Parallel, and AppleTalk® interfaces
- LAN support, including Ethernet, Thin Ethernet, StarLAN, and IBM® 3270/5250 protocols
- interrupt controllers with timers and parallel I/O ports.

ALL TOGETHER: THE TOOLS

The NS32CG16 is also supported by a full range of development tools, available now:

- add-in cards to turn your PC/AT® or compatible into a powerful, multiuser development host
- a full set of language tools, including
  - —assemblers, linkers, debuggers
  - —optimizing compilers for C, Pascal, FORTRAN 77, and Ada®
- MicroCASE (formerly Northwest Instrument Systems) Software Analysis Workstation for performance-tuning your code
- National's In-System Emulator (ISE™) for complete hardware/software integration
- the NS32CG16 Evaluation/Development Board to reduce development time and costs, and bring your design to market faster (*in development*).

ALL TOGETHER: THE PROOF

The NS32CG16 has already been designed-in by a number of major office peripherals manufacturers, such as Canon and Olivetti, and is now being evaluated by over 100 companies around the world.

But find out for yourself what the NS32CG16 can do in *your* design.

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CIRCLE 4

SEPTEMBER 8, 1988 VOL. 36, NO. 20

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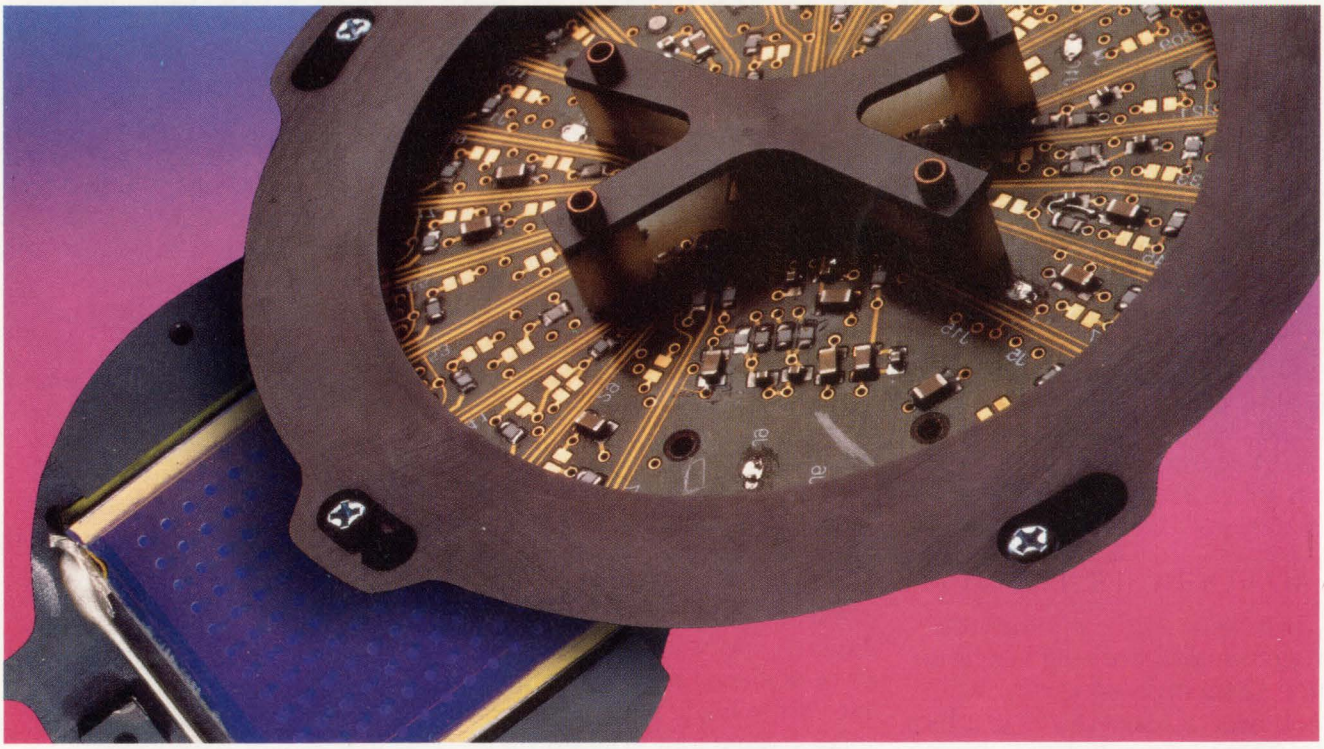

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Improving on the best of two worlds, a digital spectrum analyzer employs a new conversion algorithm to top the speed of conventional spectrum analyzers; it also surpasses the bandwidth of real-time FFT analyzers.

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A 20-MHz CMOS chip speeds FFT algorithms by executing real or complex butterfly kernels in just 100 ns per point.

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ZFL-500LN	0.1-500	24	+5	2.9	79.95	1-24
ZFL-750	0.2-750	18	+9	6.0	74.95	1-24
ZFL-1000	0.1-1000	17	+9	6.0	79.95	1-24
ZFL-1000G*	10-1000	17	+3	12.0	199.00	1-9
ZFL-1000H	10-1000	28	+20	5.0	219.00	1-9
ZFL-500HLN	10-500	19	+16	3.8	99.95	1-24
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ZFL-1000VH	10-1000	20	+25	4.5	229.00	1-9
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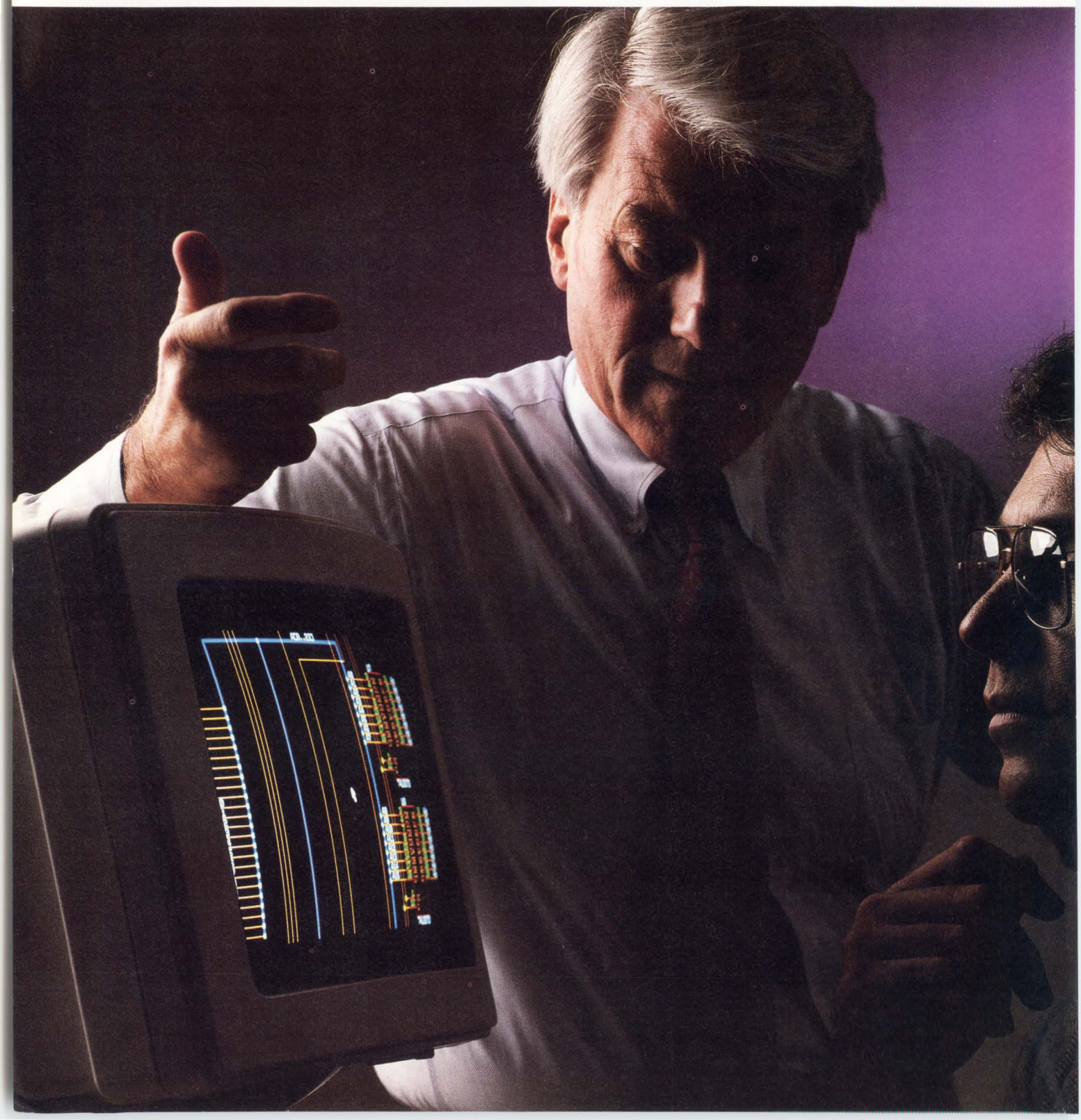
AND WE NEED IT AT EVERY S



T PROGRAMING. REALLY NEED. TAGE IN THE PROCESS."

WE COULDN'T AGREE MORE.

Testing ASIC devices creates a whole new set of problems. Developing test programs, characterizing, verifying and debugging are, at best, unwelcome and time-consuming for ASIC designers. ASIC vendors can test the silicon, but not the custom functionality of the ASIC prototype. Traditional test approaches and traditional ATE merely compound the problem.

At ASIX Systems our focus has always been exclusively on ASICs. From the start we took an entirely different approach to solving the unique ASIC test problems. We saw immediately that adapting existing ATE to try to fit to needs of ASICs didn't make sense. Designing a totally new, focused ASIC test system did. Not only did programs need to be automated, they needed to be developed from the design data base and menu-driven, so changes would be simple to make. And the test system itself had to be easy to use, designed for its particular environment, and a cost-effective alternative to the huge, expensive, complicated ATE.

TEST SOLUTIONS FOR THE WHOLE ASIC COMMUNITY.

Our unique perspective allowed us to understand that the ASIC world is not so much Design Engineers, Test Engineers and Quality Engineers working independently. It's more a "community" of specialists whose tasks are intrinsically linked. So we made sure that we could provide another crucial element. Communication. In order to capture the vital time-to-market edge, what ASIC end users and vendors really need is the opportunity to use the same test programs and the same tester. That's what gives both environments a common frame of reference and the chance to generate test programs automatically from the design data base. That's the ASIX-1 family of test systems.

ASIX-1: ASIC TEST SYSTEMS THAT MAKE SENSE.

We don't have the room here to tell you everything the ASIX-1 family has to offer. But here are a few things to think about: automatic, menu-guided programming; data base management; ATE architecture and flexibility at an affordable cost; 256 true I/O pins; "zero footprint"; fully integrated PMU; automatic calibration; simple fixturing; no cabling; high MTBF. That's enough. If you're testing ASICs you know you have to see for yourself what the ASIX-1 can do. And the sooner the better. ASIX Systems Corporation • 47338 Fremont Blvd • Fremont, CA 94538.

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CIRCLE 53

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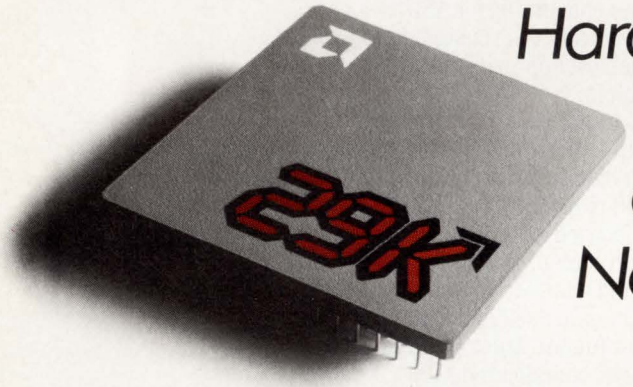

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CIRCLE 8

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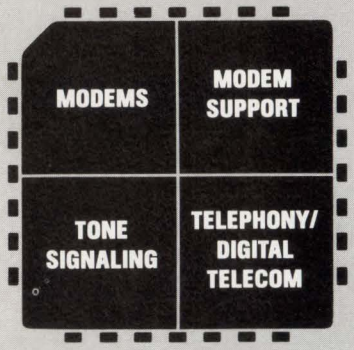
IN A SERIES



Silicon Systems has developed the following families of advanced telecommunication chips.

MODEMS: Silicon Systems offers the industry's most advanced designs in single-chip modem IC's. All members of the SSI K-Series family of one-chip modems are designed to the same footprint, with total hardware and software compatibility, allowing easy product upgrading over the entire Bell and CCITT range of full-duplex, split-band standards at data transfer speeds from 300 to 2400 BPS.

MODEM SUPPORT: SSI has designed a line of high performance filters, special purpose FSK modems, and high speed modem analog processors, which make possible efficient modem designs for custom applications.

TONE SIGNALING: Since pioneering the DTMF receiver, SSI has not only developed a whole family of DTMF receivers but has also introduced DTMF transceivers that can both generate and detect all 16 standard Touch-Tone digits. This Tone Signaling Family of products also includes a group of telephone-band call progress detector chips, which simplify design of automatic calling systems.

TELEPHONY / DIGITAL TELECOM: This family is comprised of standard integrated circuits for use in T1 transmitters and receivers, as well as chips for DS-1 line interfacing, central office MF tone detection, and 4-wire loopbacks for use in low-cost maintenance termination units.

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silicon systems
INNOVATORS IN INTEGRATION
CIRCLE 9

WEAVING AN INTERNATIONAL WEB

An interesting international situation could be facing Sematech, the U.S.-government-sponsored consortium of American semiconductor makers whose aim is to improve the U.S. industry's production capabilities for next-generation VLSI. Although Sematech is supposed to be strictly American, taking financial support from public coffers filled by U.S. taxpayers, what if a Japanese-owned semiconductor manufacturer with extensive U.S. production facilities wants to join? NEC Electronics, Inc., for example, which employs hundreds of American worker-taxpayers in Roseville and Mountain View, Calif., has been reported as looking into membership. Sematech leaders are, however, opposed to taking any Japanese-owned competitor into its ranks.

We hope that Sematech can and will strengthen the American semiconductor industry. However, American semiconductor makers do not operate in a vacuum (no pun intended). The whole electronics industry is becoming more international every day. The many technology partnership agreements between American semiconductor makers and Far Eastern and European companies call into question just how Sematech-developed technology will be maintained as exclusively American. Already, many American semiconductor companies have extensive international operations, with overseas manufacturing sites and chip designs generated at centers across the globe.

What's more, it seems inevitable that national technology boundaries will continue to fade as new design technologies take hold. With worldwide communication facilities to transmit massive amounts of design data from CAE workstations anywhere in the world, the distance between, say, a design team's hardware and software groups can span contintents.

There's plenty of information to fill the pipeline, to keep design engineers, both here and abroad, on their toes. That's where ELECTRONIC DESIGN comes in. As you read through this issue, you'll notice changes in graphic design and in the lineup of departments. This sprucing up makes us a better vehicle for the critical design engineering information you've always expected from us.

Stephen E. Scrupski
Editor-in-Chief

tiny SPDT switches

absorptive... reflective

dc to 4.6GHz from $32.95 (1-24)

Tough enough to pass stringent MIL-STD-883 tests, useable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model	KSW-2-46		KSWA-2-46	
Connector Version	ZFSW-2-46		ZFSWA-2-46	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	−5V on, OV off		−5V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (1-24)	**$32.95**		**$48.95**	
	$72.95		**$88.95**	

finding new ways...
setting higher standards

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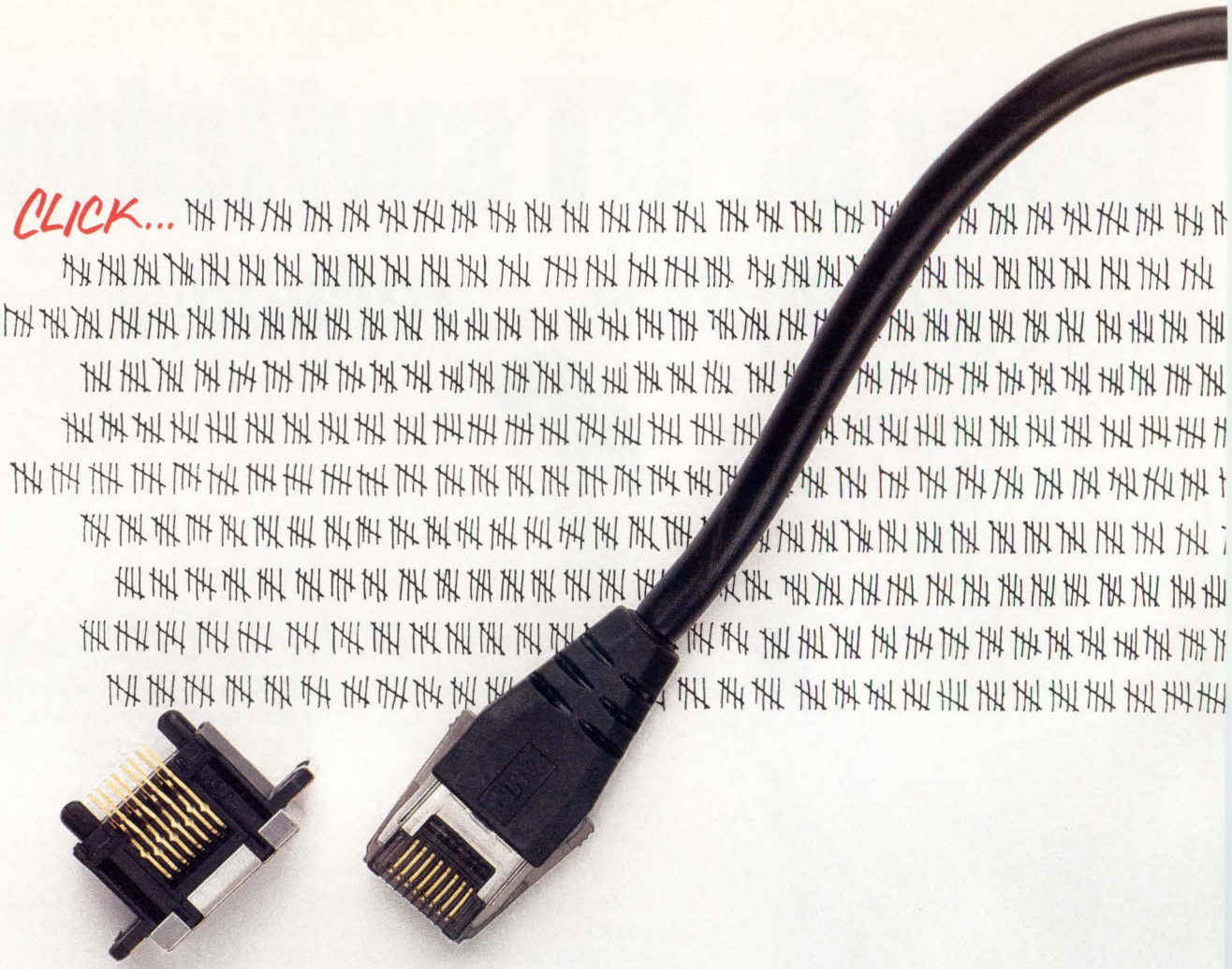
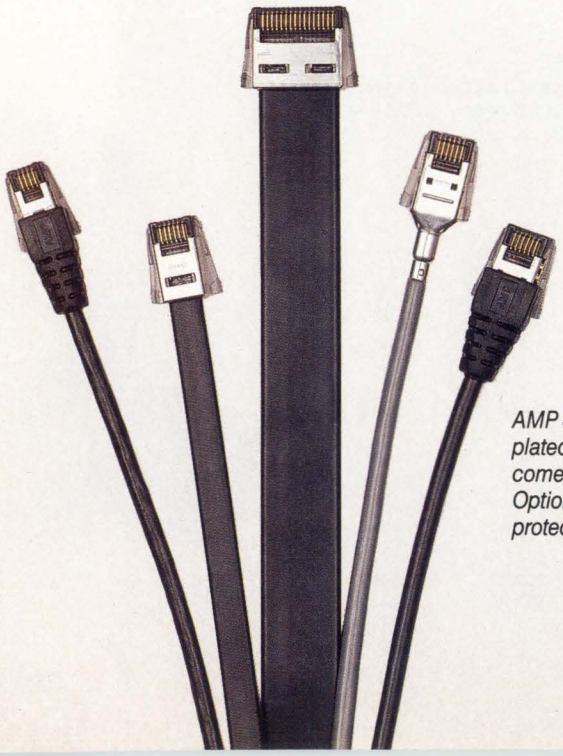
C 117 REVD

CIRCLE 10



Great ideas tend



They're simple. They're shielded. They go in with a solid click, and release with a gentle squeeze. Keying and polarization are implicit.

And they're very, *very* durable. In fact, our Shielded Data Link (SDL) connectors are rated at 3000 cycles. They owe their toughness to design and engineering, and attention to such details as selective gold plating. Dependability is the essence of friendliness.

But good-looking and hard-working start well before the user sees this connector. The highly effective shield is designed in, so our SDL connector comes as a no-hassle, one-

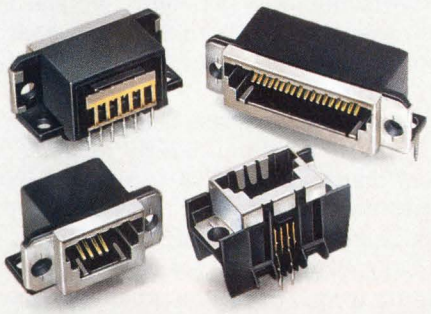
AMP SDL connectors—selectively gold plated for reliability and durability—come in 4, 6, 8, and 16 positions. Optional boot for round cable version protects against electro-static discharge.

Offset flange receptacle makes good use of real estate.

to hang in there.

piece assembly. It terminates to flat shielded cable in a single step—conductors and shield, plus two-point strain relief. Round cable takes only two steps.

AMP SDL connectors are a cost-effective alternative to crimp-snap type products, whether you do-it-yourself or order custom cables from us in flat, round, or coiled styles. Either way, you benefit from the same ease of application, the same well-thought-out design. And you walk away with the reliability and durability you need.



Receptacle options: top and side entry, and shunted side entry versions for network applications.

For technical information and literature on SDL connectors, call 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

CIRCLE 75

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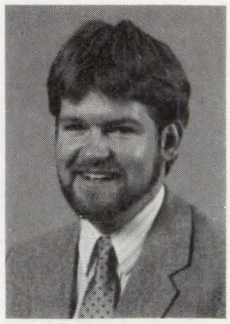
CIRCLE 12

IPI-2 Starts To Roll


BARRY W. PHILLIPS

The data-transfer rate of the disk interface is of paramount importance in such applications as relational database machines, graphics workstations, and imaging. With the standard storage module drive (SMD) interface running out of steam, system integrators must determine whether they can live with the transfer-rate performance that will be offered by the buffered, logical-level SCSI-2, or whether they should upgrade to the timing critical, device-level Intelligent Peripheral Interface, IPI-2.

Many users have already pushed the SMD interface to its limit of 3 Mbytes/s by tweaking the cable (50 meters maximum) with costly ECL transceivers and balanced transmission lines. Meanwhile, the completed SCSI-2 specification is gaining momentum, with its promise of 5- 6-Mbyte/s transfer rates (although, over the full 25-m length of the SCSI cable, a maximum of 4 Mbytes/s has been attainable). A fast differential transceiver option (10 Mbytes/s) and a dual-cable option for wide transfers are both on the drawing board for SCSI-2.

If the transfer rate is of significant important, IPI shines. IPI-2 promises 10-Mbyte/s transfers at up to 60 meters. The enhanced IPI (presently being standardized) runs at 25 Mbyte/s with fast differential transceivers and optimized cables. With ECL, this data rate is boosted to 50 Mbyte/s. A 100-pin enhanced IPI can transfer data at 100 Mbyte/s. The next generation of IPI drives will cash in on its promise. For example, by upping bit density, both Fujitsu and NEC are planning IPI-2 drives that transfer data at 4 to 4.5 Mbyte/s for mid-to-late 1989.

An advantage of IPI, which is not offered in SCSI, is a dual channel option. This provides a redundant path for each drive, which is key in fault tolerant systems. IPI will handle parallel processes, multiple channels of access to one subsystem, and addressability to an unlimited number of drives. At first, the interface was used to connect multiple-spindle disk farms to large mainframes with IPI-2 to IPI-3 bridge controllers from Control Data, Fujitsu, Hitachi, IBM, and Siemens. Quantities are high; IBM alone has shipped over 125,000 disks on its mid-range systems.

This fall's design season opened with a series of fireworks that will surely give IPI-2 a boost. Working largely to coincide with announcements from the IPI drive community, two controller board vendors are readying IPI-2 adaptors for the VMEbus. With these new boards available, IPI-2 has become an attractive option in the mini supercomputer and high-end workstation file server market.

Dallas-based Interphase Corp. just released the first IPI-2 host adapter for the VMEbus. Based on a 16-MHz 68020 CPU, the board features a large cache memory that consists of 256 to 512 kbytes of dual-port RAM.

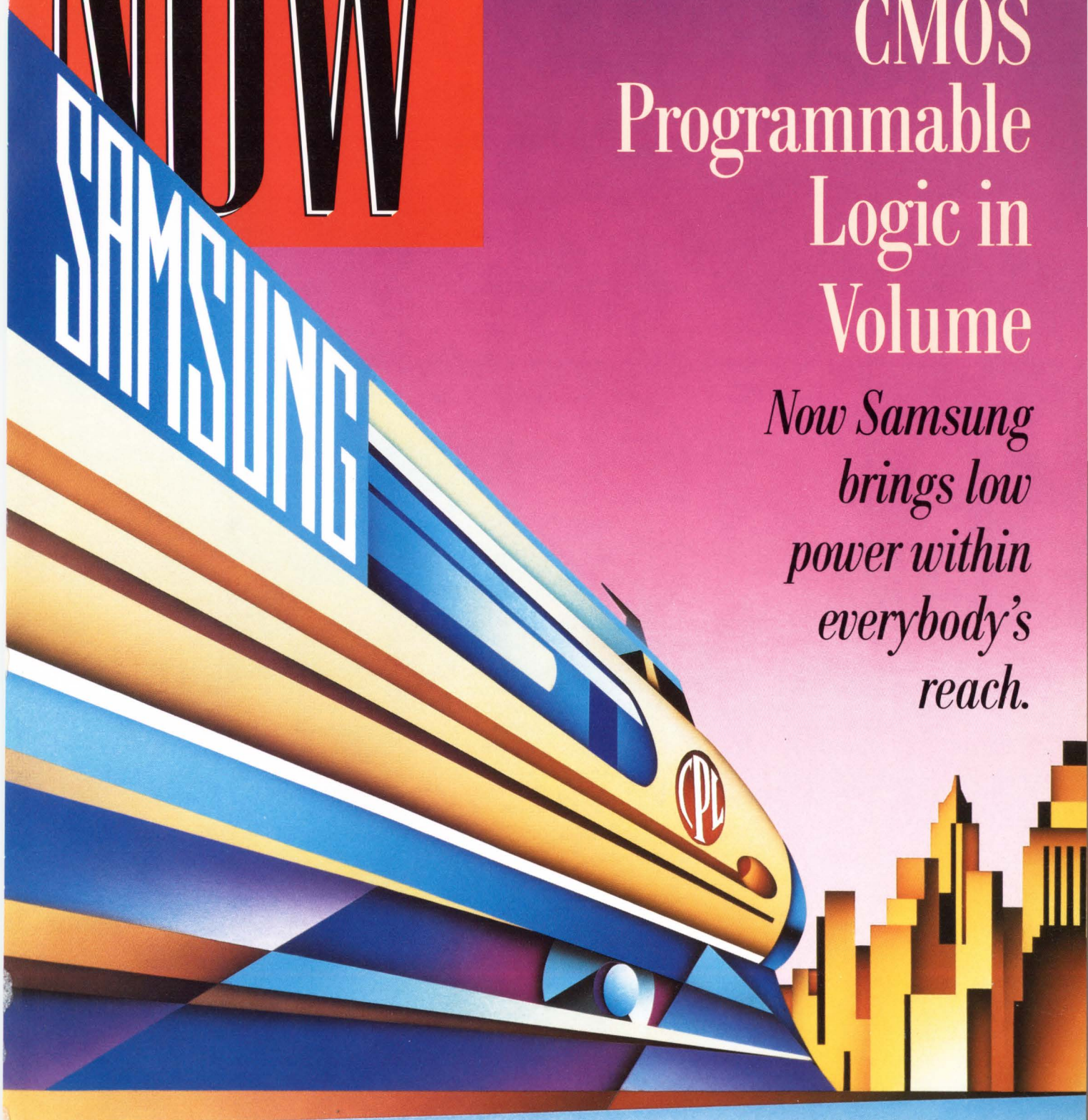
In addition, Xylogics Inc., of Burlington, Mass., plans a fall introduction for a high-end, IPI-2-to-VMEbus adapter. According to company president Chap Cory, "Once users see controllers available for IPI-2, many will start migrating from SMD. Although the IPI-2 drives shipping are at current SMD data rates, new drive technology is coming along fast. With our upcoming controller, data rates two times greater than SMD are no problem."

Those disk-drive improvements are underway. By reading two heads in parallel, Control Data Corp. doubled their IPI data rate. According to Amyl Ahola, vice president of marketing, CDC will announce a 6-Mbyte/s version of its 1-Gbyte IPI-2 Saber drive by next month. Evaluation units will be out by year's end, and volume shipments will occur in early 1989. Hitachi also expects to debut a two-head, parallel-transfer drive by the middle of next year. Ultimately, the multihead technique will expand to five or more heads, yielding 15-Mbyte/s IPI-2 transfers by the end of 1989.

SAMSUNG

NOW

Number I



CMOS Programmable Logic in Volume

Now Samsung brings low power within everybody's reach.

We Introduce an Exceptionally Reliable New EEPROM in CMOS
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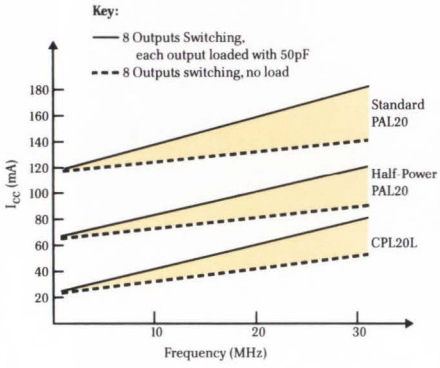
CMOS PROGRAMMABLE LOGIC

INTRODUCING CPL™ Samsung Moves

Harnessing our manufacturing strength, we become the first to produce this demanding technology in volume.

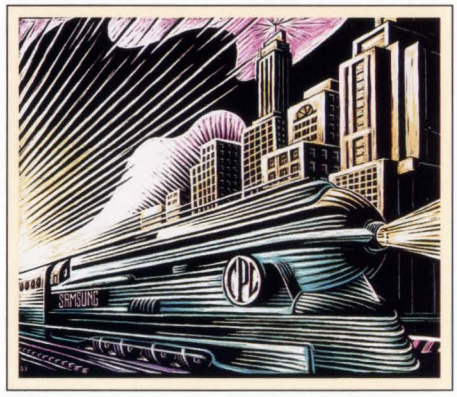


CPL reduces power dissipation up to 70% compared to bipolar PALs.

Since the beginning, Samsung Semiconductor has been known for its manufacturing expertise.

Samsung's commitment to CMOS technology is also long-standing.

Today, our new CPL (CMOS Programmable Logic) product line draws on both of those strengths.



It is a product line at the cutting edge of technology, and we are uniquely positioned to manufacture it–and manufacture it in volume.

What the introduction of CPL means is that, for the first time, there is a viable low-power alternative to bipolar PALs.®

It's viable both because we are offering CPL in volume. And because we're making it affordable–comparable in cost to bipolar parts.

In short, we're taking CMOS Programmable Logic, once and for all, out of its high-priced niche. To make low power a reality. And make compact systems more feasible than ever.

What will CPL do for you as a designer?

It will let you cut your power consumption 70% by directly replacing the bipolar PALs in your existing design. With no new development tools. And with no redesign.

In new designs, you'll have a head start on reducing power consumption.

And there's another critical advantage. Unlike bipolar PALs, Samsung's UV-erasable CPL devices are reprogrammable. Which means that we're in a position to ship 100% tested parts. We subject every CPL device, in fact, to programming, AC, and functional testing.

CPL–low in power, 100% tested, and produced in volume by a manufacturing giant–is here to stay. Request a databook and samples today, and get started with this winning technology now. NOW

Samsung: A leader in CMOS

Samsung Semiconductor is among the world's leaders in manufacturing products that use leading-edge CMOS processes. Our 6-inch wafer-fabrication lines are some of the most advanced in existence. Our technology has evolved from 2.5 micron to 0.8 micron in just four years. And we have invested more than $600 million in new product development. Throughout our growth, we have continued to manufacture products that meet the very highest quality standards.

The CPL Parts

CPL 20	CPL 24
CPL16L8	CPL20L10
CPL16R4	CPL20L8
CPL16R6	CPL20R4
CPL16R8	CPL20R6
	CPL20R8

Speed options: 25 nsecs, 35 nsecs.
Power options (Icc max.) 45 mA, 70 mA

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To The Forefront.

You can develop a CPL design with existing tools. Or you can use our Starter Kit and start prototyping immediately.

Developing new, low-power designs with Samsung CPL is easy. And to make it that much easier, we're offering a low-priced CPL Starter Kit.

The Starter Kit includes a software package developed by Personal CAD Systems and based on CUPL,™ the most powerful high-level language for designing programmable logic. And it also includes samples of Samsung CPL20 and CPL24 devices, which are supported by the Starter Kit.

Since CPL devices are reprogrammable, this means the Starter Kit includes everything you'll need to prototype and debug your design.

And you'll be doing that in short order. The CUPL software runs on any IBM PC/XT/AT or compatible system, and it lets you choose from a variety of options for entering your design–including truth tables; state diagrams and ASM flow charts (for describing sequential designs); and high-level equations.

CUPL power tools provide logic minimization, available in three algorithms for improved optimization; DeMorganization (helpful when negating complex expressions); and simulation, to help you verify your design.

Comprehensive documentation includes a logic "template" file for design ease; a fuse map and expanded product-term information; a chip diagram illustrating pin assignments; and a symbol table of all variables. In addition to the CUPL software, Samsung's CPL Starter Kit includes:

- CPL20 and CPL24 samples.
- A CPL data book.
- A manual for the CUPL software.
- A Programmable Logic User Guide (PLUG) diskette, which lets you browse interactively through the workings of programmable logic.
- "My First PAL Design," a booklet that leads you step by step through programmable logic design.

At just $220, Samsung's CPL Starter Kit is a bargain. Request ordering information today and get started designing–in low power. NOW

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ADVANCED CMOS LOGIC FAMILY

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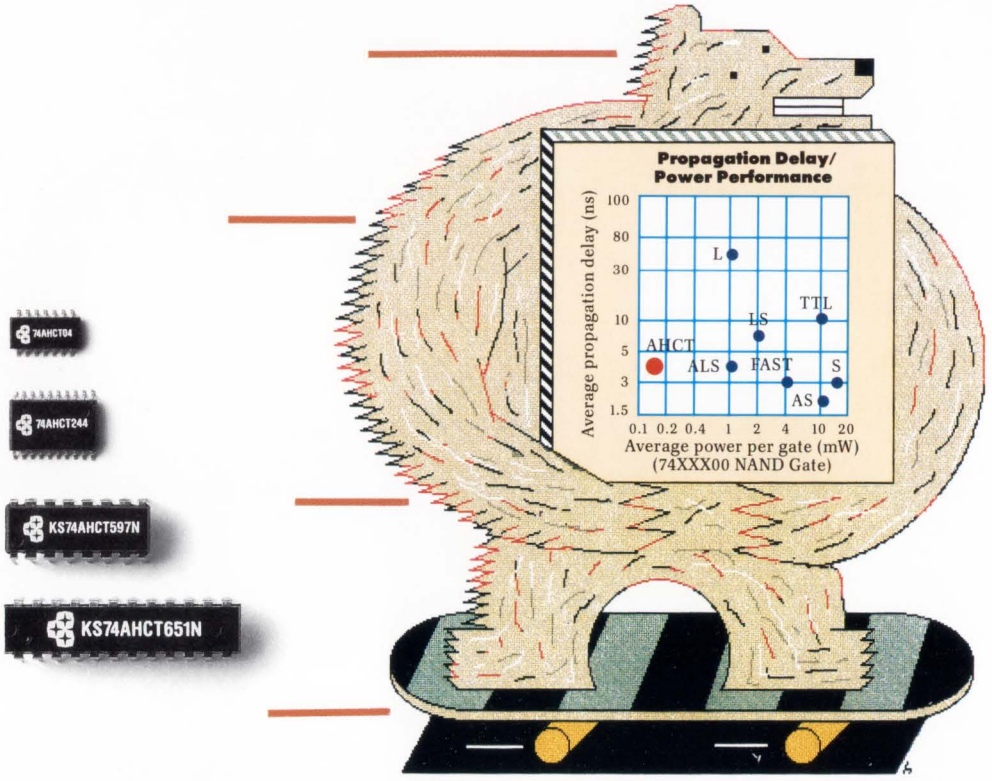
that are Exceptionally Fast *and* Very Available.

The entire Samsung AHCT CMOS advanced logic family is in stock, available, ready, and waiting to be shipped—right now. All fast, all very very cool.



When you look at both speed and power, you see that Samsung's AHCT family is, simply, unsurpassed.

And unlike other advanced logic families, these are parts that are available today, from stock.

All 157* of the AHCT CMOS logic family parts are direct plug-in replacements for ALS and FAST™-parts that provide the most comprehensive selection of standard logic functions available. Which means that no matter which ALS or FAST part you're using, you can replace it with an AHCT CMOS part–and cut your power–right away.

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We have free samples available for you today. Or, as an additional way to learn just how good these parts are, use the coupon at the back of this insert to request information on our AHCT tool box. It keeps 100 of the most popular advanced CMOS logic device types at your fingertips, whenever you need them. NOW

Of the 157 parts in the family, 125 are available from stock today; the remaining 32 will be available by the end of 1988.

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KS74AHCT Parts

Gates and Inverters

00	08	20	51
01	09	21	58
02	10	22	86
03	11	27	132
04	12	30	133
05	14	32	266

Buffers and Line Drivers

125	241	367	467
126	244	368	468*
210	365	465*	540
240	366	466	541

Flip-Flops

73	173	534	823
74	174	564	824*
76	175	574	825*
78	273	670	826*
107	374	794	
109	377	821*	
112	399	822*	

Latches

75*	533	841*	845
77*	563	842*	846
259	573	843*	
373	793	844*	

Transceivers/ Registered Transceivers

242*	643	651	664
243*	645	652	665*
245	646	658*	
640	648	659*	

Counters

160	168	192	590*
161	169	193	591*
162	190	390*	592
163	191	393	593*

Decoders/Encoders

42	139	154	238
138	148	155	239

Multivibrators

121*	123*	423*

Logic Level Converters

4049	4050*

Multiplexers

151	158	257	353
153	251	258	
157	253	352	

Shift Registers

164	194	299	596*
165	195	595	597
166			

Arithmetic Circuits

181	518	522	684*
182*	519	679	686*
183	520*	680	688
280	521	682	689*

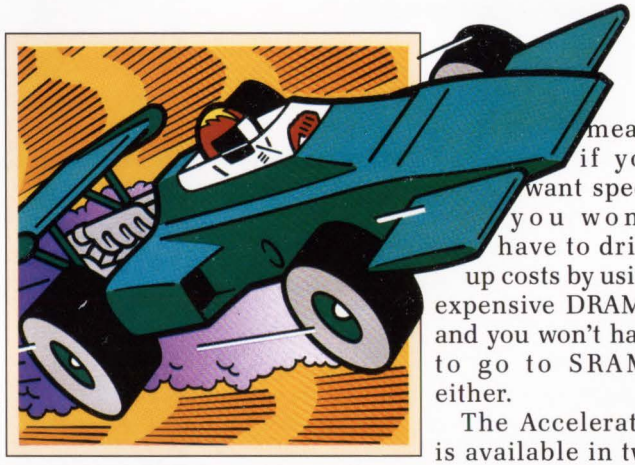
All parts are available in plastic DIP. For SOIC availability, contact the factory.
**Available by end of 1988.*

DRAM CONTROLLER

Our new 1- and 4-meg DRAM Controller is also a system accelerator. It can give you

80ns *Performance* *from* 120ns *DRAMs.*

Our new 1- and 4-meg DRAM Controller does so much for system speed that we've named it *The Accelerator.*



If you're a designer attracted to speed, you're going to want to design it in.

The KS84C21/22 DRAM Controller supports interleaving, and it supports the fastest access modes of the newest DRAMs.

It radically reduces parts count and engineering effort compared to PAL-based designs and interfaces to all major microprocessors.

But above all, it effectively increases the speed of your memory array–giving you performance exceeding 80ns from 120ns DRAMs.* Which means if you want speed, you won't have to drive up costs by using expensive DRAMs, and you won't have to go to SRAMs either.

The Accelerator is available in two versions. One has an externally programmable register, for prototyping and moderate-volume applications. The other version is the first and only mask-programmed DRAM controller ever developed anywhere, and it eliminates still more logic parts.

To make it easier to get started with The Accelerator, we've made up a sample kit.

Request yours today and start designing-in speed! NOW

Samsung's DRAM Controller.

Part	RAMs Supported	Package
KS84C21-25CL	256K, 1 MB	68-pin PLCC
KS84C22-25CL	256K, 1 MB, 4 MB	84-pin PLCC

*System dependent.

TURN
to coupon on back page to request free DRAM controller sample kit and specifications.

Samsung: Building on our leadership in DRAMs
As one of the world's leading producers of DRAMs, Samsung Semiconductor has been able to compete in one of the most demanding technologies of all. And we will continue to do so as our 4- and even 16-megabit products emerge. We're making additional use of this manufacturing know-how to deliver an extremely broad range of semiconductor products that are remarkable for their high performance, their cost-effectiveness, and their reliability.

EEPROMS

Our CMOS 64K EEPROM Is an Entirely New Breed.

Feature by feature it's as good or better. But besides using less power, it also consumes less money.

When you stack it up against the leading competitors, our new CMOS 64K EEPROM is, in a word, better.

It uses less power (100 μA vs. 150 μA standby current, 30 mA vs. 50 mA active current). It's exceptionally fast.

And it's available at much lower cost.

The part is available in volume right now.

In reliability, it's superb–far more reliable than requirements call for. In 1000 hours of testing in the key areas of endurance, WHTS, HOPL, and WHOPL–with industry-standard testing procedures–there were *zero* failures experienced.

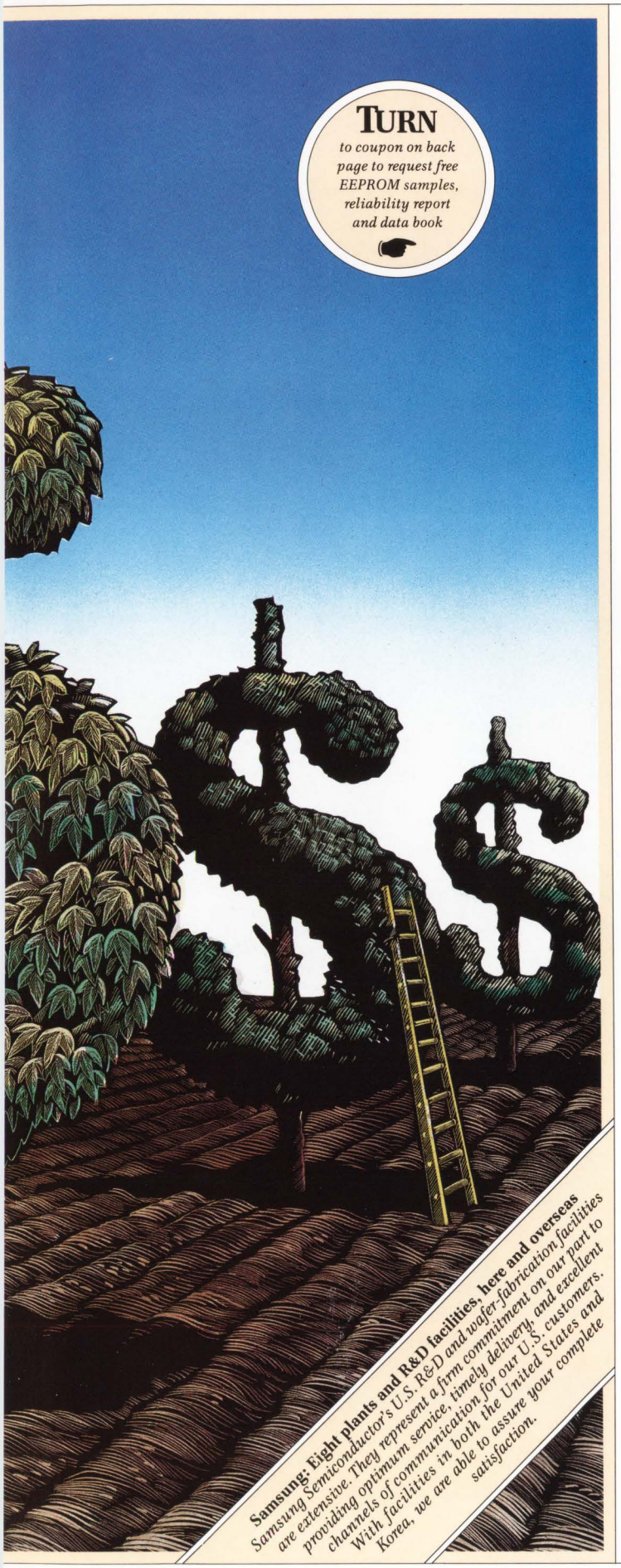
We think what all this means is that our new CMOS 64K EEPROM is simply the most sensible choice on the market.

But don't take our word for it. Request our reliability report, data sheet, and samples today. Then compare it for yourself. NOW

Product Specification	Samsung 28C64 8K x 8 CMOS EEPROM	Leading Competitor's 64K CMOS EEPROM
ISB (standby current)	100 μA	150 μA
ICC (active current)	30 mA	50 mA
TAA (address access time)	200 ns	200 ns
TRC (read cycle time)	200 ns	200 ns
TWC (write cycle time)	2-5 ms/byte	2-5 ms/byte
VCC	5V ± 10%	5V ± 10%
Page mode	Yes	Yes
Endurance (write cycle)	10,000	10,000
Data retention	10 years	10 years
Packaging	DIP, PLCC	DIP, PLCC

The KM28C64/65 at a glance.

8K x 8 CMOS EEPROM ■ 28-pin JEDEC byte-wide memory pinout (DIP, PLCC) ■ Single 5V ± 10% Vcc supply ■ Performance: 200/250ns ■ Current: standby (max) 100μA; active (max) 30mA ■ 32 byte page write: 5ms ■ 4-cell bridge for enhanced reliability ■ Write completion indicator: Data polling, Rdy/busy (for KM28C65) ■ Endurance 10,000 cycles ■ Data retention 10 years



The Most Reliable Battery-Backed SRAMs Aren't SRAMs at All.

They're EEPROMs from Samsung.

Since EEPROMs don't require batteries to retain data during power loss, they are, of course, inherently more reliable than devices that do–such as SRAMs.

Because of the relative costs, however, it wouldn't occur to most designers to use an EEPROM where conventional thinking calls for an SRAM–even *with* the improvement in reliability that there'd be.

But those relative costs are changing.

Today, SRAMs cost more than they once did. And Samsung's EEPROMs, in fact, now compare favorably in price.

Which means that if you want reliability, there's every reason to start using these EEPROMs–and making your next battery-backed SRAMs, Samsung EEPROMs.

There are, of course, additional applications at which we excel. Our entire EEPROM family–including our new 64K CMOS part–is also superbly suited to rugged applications such as communications, instrumentation, robotics, and industrial control.

All Samsung EEPROMs are guaranteed to provide endurance in excess of 10,000 write cycles and data retention of 10 years. And they meet or surpass all other industry standards for performance, reliability, and quality.

Most important of all, our EEPROMs are available in large quantities *from stock*–so you avoid escalating lead times as well as high prices.

EEPROM performance, reliability, and availability–all at low cost. To start taking advantage of them, request samples, a data sheet, and a reliability report today. NOW

Samsung CMOS and NMOS EEPROMs.

Part Type	Organization	Speed	Features	Technology	Pinout	Availability
KM28C64P	8K x 8	200,250	Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time	CMOS	28 pin	From Stock
KM28C65P	8K x 8	200,250	Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time	CMOS	28 pin	From Stock
KM2816AP	2K x 8	250,300,350	10ms (max) write time	NMOS	24 pin	From Stock
KM2817AP	2K x 8	250,300,350	Ready/Busy, 10ms (max) write time	NMOS	28 pin	From Stock

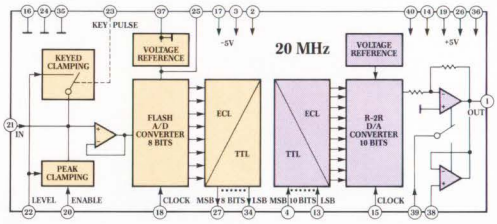
In linear, what Samsung gives you can be stated easily.

MORE.

A Data Converter That Does More.

Samsung's new KSV3110 data converter is a technological feat that we're rather proud of.

On a single chip, it offers independent 8-bit flash A/D and 10-bit D/A functions. And with an operating range of DC to 20MHz, it's faster than any other part available that does both. Also unique, it gives you an auxiliary circuit, which can be used to do impedance matching within the chip.



What's good about having all this on one chip, of course, is that it saves you real estate and money–and also cuts power drain. And, at the same time, boosts system reliability.

In short, the KSV3110 doesn't just do more. It does *way* more.

TURN
to coupon on back page to request linear data books and specifications.

Samsung's 3110 Series Combination A/D-D/A Converters.

Part Type	Resolution		Linearity		Conversion Speed	Industry Part
	A/D	D/A	A/D	D/A		
KSV3110N-10	8 bits	10 bits	±1/2 LSB	±1/2 LSB	20 MSPS	
KSV3110N-9	8 bits	10 bits	±1/2 LSB	±1 LSB	20 MSPS	
KSV3110N-8	8 bits	10 bits	±1/2 LSB	±2 LSB	20 MSPS	
KSV3110N-7	8 bits	10 bits	±1/2 LSB	±4 LSB	20 MSPS	
KSV3100AN-8	8 bits	10 bits	±1/2 LSB	±2 LSB	20 MSPS	UVC3101
KSV3100AN-7	8 bits	10 bits	±1/2 LSB	±4 LSB	20 MSPS	UVC3101

Volume Leadership In Conventional A/D And D/A...

As a company that does remarkable things in the manufacturing arena, Samsung is in a superb position to produce high-quality conventional data converters cost effectively and in volume.

And that's just what we do.

Which means that if you use data converters in large quantities, you simply won't find anyone it makes better sense to do business with.

Samsung: Some of the world's most advanced fabrication lines. Among our fabrication lines, a particular showpiece is our new Class 1 6" wafer facility in Kiheung, Korea, dedicated to DRAM technology and set to open in October of this year. It utilizes advanced stepper technology and automated manufacturing and is among the largest in the world.

The Samsung A/D and D/A Lines.

Part Type	Resolution		Linearity		Conversion Speed	Industry Part
	A/D	D/A	A/D	D/A		
KSV3208N	8 bits		±1/2 LSB		20 MSPS	
KAD0820ACN	8 bits		±1/2 LSB		1.5 μsec	ADC0820BCN
KAD0820AIN	8 bits		±1/2 LSB		1.5 μsec	ADC0820BCJ
KAD0820BCN	8 bits		±1 LSB		1.5 μsec	ADC0820CCN
KAD0820BIN	8 bits		±1 LSB		1.5 μsec	ADC0820CCJ
KAD0808IN	8 bits		±1/2 LSB		100 μsec	ADC0808CCN
KAD0809IN	8 bits		±1 LSB		100 μsec	ADC0809CCN
KDA0800CN		8 bits		±1/2 LSB	*100 nsec	DAC0800LCN
KDA0801CN		8 bits		±1 LSB	*100 nsec	DAC0801LCN
KDA0802CN		8 bits		±1/4 LSB	*100 nsec	DAC0802LCN
KDA0806CN		8 bits		±2 LSB	*150 nsec	DAC0806LCN
KDA0807CN		8 bits		±1 LSB	*150 nsec	DAC0807LCN
KDA0808CN		8 bits		±1/2 LSB	*150 nsec	DAC0808LCN
KS7126CN	3-1/2 digit		±1/2 LSB		333 msec	TSC7126
KS25C02	CMOS 8-bit successive approx. register					DM2502
KS25C03	CMOS 8-bit successive approx. register					DM2503
KS25C04	CMOS 12-bit successive approx. register					DM2504

**Settling Time*

And In Op Amps, Regulators, Comparators, Timers, And More.

Across the entire spectrum of high-volume linear devices, in fact, Samsung–being a manufacturing leader–offers a combination of reliability and competitiveness in price that has given these devices tremendous acceptance in the marketplace.

It's a market we're strongly committed to, and we have more than 250 industry-standard ICs available for immediate delivery now.

If by chance you *aren't* buying linear devices from Samsung, it will make sense for you to look into us.

Solutions Tailored To Specific High-Volume Needs. For Those Who Simply Need More.

A particular specialty that Samsung offers in linear is in the area of specific, rather simple solutions tailored to certain very high-volume applications.

We have developed devices for use in such high-volume areas as telephones, car stereo, and household appliances–among many others.

If you have a need for a high-volume, tailored linear device on this order, we may have the device you need–and if we don't, we'd like to talk about making it for you.

Our line of simple speech synthesis chips–designed for use primarily in electronic toys and answering machines–is one particular example of the kind of low-cost solution we can offer.

To learn about others, please contact us.

Our Speech Synthesizers.

Part	Function	Application
KS5901A	Voice synthesizer (external ROM)	Sound information answering machines
KS5902XX	Voice synthesizer (internal ROM)	Toys; simple sound generation
KS5911	Voice recording and reproducing (talking back type)	Talk-back answering machines
KS5912XX	Natural sound generation	Toys; natural sound effect

Major Linear ICs

Regulators

3T Positive

KA78TXXCF	3 Amp
KA78TXXCT	3 Amp
LM317T	1.5 Amp
MC78XXCT	1 Amp
MC78MXXCT	0.5 Amp
MC78LXXACZ	0.1 Amp
LM723CN	0.1 Amp

3T Negative

KA337T	1.5 Amp
MC79XXCT	1 Amp
MC79MXXCT	0.5 Amp
MC79LXXACZ	0.1 Amp

Switching

KA78S40CN	KA3524N

REF Voltage

KA431CZ (TL431CLP)	KA336Z-2.5,5
KA431N (TL431CP)	KA385Z-1.2

Comparators

KA319N (LM319N)	LM2903N
KA361N (LM361N)	LM311N*
KA710CN (LM710N)	LM3302N
KS374N (TLC374N)	LM339N/AN*
LM2901N	LM393N/AN*

Op Amplifiers

KA301N/AN (LM301N)*	LM348N*
KA733CN (LM733CN)	LM358N/AN*
KA9256 (POWER AMP)	LM741CN*
KF351N (LF351N)	MC1458N*
LM2902N	MC3303N
LM2904N	MC3403N*
LM324N/AN*	MC4558N*

Telecommunication ICs

KA2410N	Tone Ringer
KA2411N	Tone Ringer
KA2418N	Tone Ringer/bridge diode
KA2412FN	Speech Network
KA2413N	DTMF
KS5808N	DTMF (MK5089)
KS5805AN	Pulse (MK50992)
KS5805BN	Pulse (MK50993)
KS55820N	DTMF/Pulse
KT3040J	CODEC Filter
KT5116J	CODEC
LM567N*	Tone Decoder
LM567LN	Tone Decoder (Low Power)
KS5812N	Quad UART

Timers

KS555N (CMOS)*	NE555CN*
KS555HN (CMOS)*	NE556CN*
KS556N (CMOS)*	NE558CN

RS-232 Interfaces

MC1488N*	MC1489/AN*

Audio ICs

LM386N	0.5 Watt Power Amp
KA2201N	1.2 Watt Power Amp
KA2206	2.3 Watt Dual Power Amp
KA22062	4.6 Watt Dual Power Amp
KA2210	5.8 Watt Dual Power Amp
KA22101	23 Watt Power Amp
KA2243	AM/FM IF & DET
KA22441	FM IF & DET
KA22495	FM Front End
KA2263	FM MPX

45 other audio ICs available

Video ICs

KA2914A	ColorTV VIF/SIF
KA2153	NTSC Chroma & Deflection
KA6101	Video R.G.B. Interface
KA6102	Video R.G.B. Interface

40 other video ICs available

Others

KA2580AN	(UDN2580AN)
KA2588AN	(UDN2588AN)
KA2651N	(UCN5815AN)
KA2615	LED/Lamp Driver
KA2616	LED/Lamp Driver
KA2284	5 Dot LED Meter Driver
KA2286	5 Dot LED Meter Driver
KA2288	7 Dot LED Meter Driver
KA2181	Infrared Amp
KA8301	Motor Driver IC
KS5803AN	Infrared Transmitter
MC3361N	FM IF Amp

**Also available in surface mount package (SOIC)*

TRANSISTORS

We Launch a New 1500 volt Power *Transistor*

With over 500 transistors, Samsung is among the world's largest producers. Our 1500-volt parts break ground even for us.

As a producer of transistors, Samsung sits squarely among the very largest in the world.

There is virtually no transistor need we can't fill–with a high-quality part, and at an advantageous price.

Our entire line of more than 500 transistors, in fact, is in full production and available from stock.

You can order anything from our list *now,* and get immediate delivery.

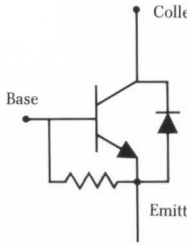
At present, we are introducing state-of-the-art, 1500-volt power transistors–transistors so difficult to produce that only one other company makes them.

We also provide 100 types of SOT-23s, ideal for both hybrid and surface-mount applications, plus TIP Series, MJE Series, and TO-92 transistors.

Many are listed here, but for a complete list of Samsung transistors, please turn to the back of this issue and request it.

NOW

The new 1500-volt transistors at a glance.



Internal circuit of damper diode built-in TR.

Designed for high-voltage switching systems and industrial motor controls, the eight new Samsung 1500-volt power transistors utilize the TO-3PF fully isolated plastic package.

Samsung: One of the world's largest corporations

As a unit of one of the world's largest corporations, Samsung Semiconductor is here to stay. Last year, the Samsung Group employed revenues of $24 billion–which would put us in 15th place on the list of the Forbes 500. We have the resources to make things happen technologically, and we have the strength to be a partner in whom you may have absolute confidence.

TURN *to coupon on back page to request complete list of Samsung transistors and data book.*

Transistors From Samsung

1500-Volt Power TR

2.5 amps	5 amps	6 amps
KSD5010*	KSD5012*	KSD5013*
KSD5014	KSD5016	KSD5017

3.5 amps
KSD5011*
KSD5015
**Damper diode built-in transistor*

SOT-23

BCX70G	MMBT4403	MMBTA43
BCX71G	MMBT5087	MMBTA55
MMBR5179	MMBT5088	MMBTA56
MMBT2222A	MMBT5089	MMBTA63
MMBT2484	MMBT5401	MMBTA64
MMBT2907A	MMBT5550	MMBTA70
MMBT3904	MMBT6428	MMBTA92
MMBT3906	MMBTA05	MMBTA93
MMBT4123	MMBTA06	MMBTH10
MMBT4124	MMBTA13	MMBTH17
MMBT4125	MMBTA14	MMBTH24
MMBT4126	MMBTA20	
MMBT4401	MMBTA42	

66 other types also available.

TIP SERIES

TIP29 Family	TIP106	TIP140F
TIP30 Family	TIP107	TIP140T
TIP31 Family	TIP110	TIP141F
TIP32 Family	TIP111	TIP141T
TIP41 Family	TIP112	TIP142F
TIP42 Family	TIP115	TIP142T
TIP47	TIP116	TIP145F
TIP48	TIP117	TIP145T
TIP59	TIP120	TIP146F
TIP50	TIP121	TIP146T
TIP100	TIP122	TIP147F
TIP101	TIP125	TIP147T
TIP102	TIP126	
TIP105	TIP127	

MJE SERIES

MJE170	MJE210	MJE800
MJE171	MJE340	MJE801
MJE172	MJE350	MJE802
MJE180	MJE700	MJE803
MJE181	MJE701	MJE2955T
MJE182	MJE702	MJE3055T
MJE200	MJE703	

TO-92

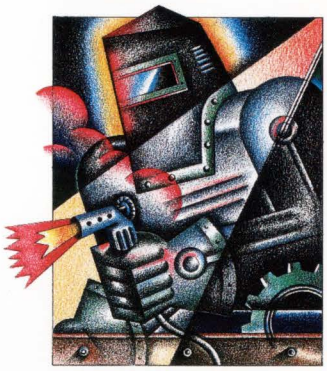
2N3904	2N5210	MPSA42
2N3906	2N5400	MPSA43
2N4123	2N5401	MPSA55
2N4124	2N5550	MPSA56
2N4125	2N5551	MPSA70
2N4126	2N6427	MPSA92
2N4400	2N6428	MPSA93
2N4401	2N6515	MPSH10
2N4402	2N6517	MPSH17
2N4403	2N6520	MPSH20
2N5086	MPSA05	MPSH24
2N5087	MPSA06	PN2222A
2N5088	MPSA14	PN2907A
2N5089	MPSA20	

200 other types also available.

MOSFETS

THE WORD IS Rugged

Power MOSFETs just don't come any more rugged than ours.



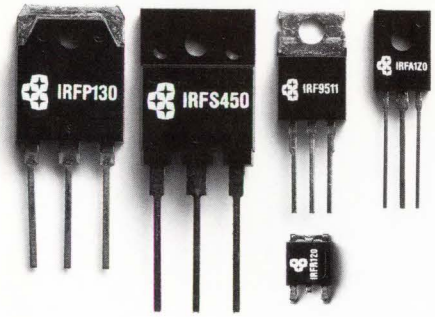
Exhaustive testing has proven Samsung's line of over 400 industry-standard power MOSFETs to be unsurpassed anywhere in ruggedness. They've been shown to withstand 2J at 500V, and in addition, each part has been screened to MIL-STD-750 specifications.

Our recently published ruggedness application note thoroughly documents the superior ruggedness of these parts, and we invite you to complete the coupon at the back of this insert to request a copy. We'll rush it to you.

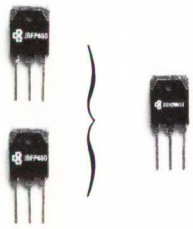
In the past several months, our MOSFETs have been qualified at an exceptionally large number of major accounts. We continue to offer the entire line with competitive pricing.

Samsung MOSFETs directly replace parts from IR and Motorola.® And since they are one of the broadest lines on the market, you can get just about anything you need. Both N and P channel parts are available, as are a variety of packages–including lead-formed TO-220s, state-of-the-art TO-247 FULL PACK and DPAK.

What more could you ask? NOW



The single MOSFET that does the job of two.



Samsung's SSH20N50–available only from us–improves reliability, simplifies assembly, and minimizes mounting hardware, because it's a direct replacement for two IRFP450's. There's less to go wrong, and less to mount.

TURN *to coupon on back page to request MOSFET samples and ruggedness application note.*

Samsung Power MOSFETs

TO-247 Full Pack N-Channel Types

IRFS130	IRFS450
IRFS140	SSS4N70
IRFS150	SSS6N70
IRFS230	SSS10N70
IRFS240	SSS4N60
IRFS250	SSS6N60
IRFS330	SSS8N60
IRFS340	SSS15N60
IRFS350	SSS20N50
IRFS430	SSS25N40
IRFS440	

TO-3P Package N-Channel Types

IRFP120	IRFP422
IRFP121	IRFP423
IRFP122	IRFP430
IRFP123	IRFP431
IRFP130	IRFP432
IRFP131	IRFP433
IRFP132	IRFP440
IRFP133	IRFP441
IRFP140	IRFP442
IRFP141	IRFP443
IRFP142	IRFP450
IRFP143	IRFP451
IRFP150	IRFP452
IRFP151	IRFP453
IRFP152	SSH3N70
IRFP153	SSH4N70
IRFP220	SSH6N70
IRFP221	SSH10N70
IRFP222	SSH4N60
IRFP223	SSH6N60
IRFP230	SSH8N60
IRFP231	SSH15N60
IRFP232	SSH4N55
IRFP233	SSH6N55
IRFP240	SSH8N55
IRFP241	SSH15N55
IRFP242	SSH4N50
IRFP243	SSH20N50
IRFP250	SSH4N45
IRFP251	SSH20N45
IRFP252	SSH5N40
IRFP253	SSH25N40
IRFP320	SSH5N35
IRFP321	SSH25N35
IRFP322	SSH7N20
IRFP323	SSH8N20
IRFP330	SSH7N18
IRFP331	SSH8N18
IRFP332	SSH7N15
IRFP333	SSH8N15
IRFP340	SSH7N12
IRFP341	SSH8N12
IRFP342	SSH12N10
IRFP343	SSH10N10
IRFP350	SSH12N08
IRFP351	SSH10N08
IRFP352	SSH12N06
IRFP353	SSH10N06
IRFP420	SSH12N05
IRFP421	SSH10N05

TO-3P Package P-Channel Types

IRFP9120	IRFP9220
IRFP9121	IRFP9221
IRFP9122	IRFP9222
IRFP9123	IRFP9223
IRFP9130	IRFP9230
IRFP9131	IRFP9231
IRFP9132	IRFP9232
IRFP9133	IRFP9233
IRFP9140	IRFP9240
IRFP9141	IRFP9241
IRFP9142	IRFP9242
IRFP9143	IRFP9243

TO-3 Package N-Channel Types

IRF120	IRF242
IRF121	IRF243
IRF122	IRF250
IRF123	IRF251
IRF130	IRF252
IRF131	IRF253
IRF132	IRF320
IRF133	IRF321
IRF140	IRF322
IRF141	IRF323
IRF142	IRF330
IRF143	IRF331
IRF150	IRF332
IRF151	IRF333
IRF152	IRF340
IRF153	IRF341
IRF220	IRF342
IRF221	IRF343
IRF222	IRF350
IRF223	IRF351
IRF230	IRF352
IRF231	IRF353
IRF232	IRF420
IRF233	IRF421
IRF240	IRF422
IRF241	IRF423
IRF430	SSM4N50
IRF431	SSM20N50
IRF432	SSM4N45
IRF433	SSM20N45
IRF440	SSM5N40
IRF441	SSM25N40
IRF442	SSM5N35
IRF443	SSM25N35
IRF450	SSM7N20
IRF451	SSM8N20
IRF452	SSM7N18
IRF453	SSM8N18
SSM3N70	SSM7N15
SSM4N70	SSM8N15
SSM6N70	SSM7N12
SSM10N70	SSM8N12
SSM4N60	SSM12N10
SSM6N60	SSM10N10
SSM8N60	SSM12N08
SSM15N60	SSM10N08
SSM4N55	SSM12N06
SSM6N55	SSM10N06
SSM8N55	SSM12N05
SSM15N55	SSM10N05

TO-3 Package P-Channel Types

IRF9120	IRF9220
IRF9121	IRF9221
IRF9122	IRF9222
IRF9123	IRF9223
IRF9130	IRF9230
IRF9131	IRF9231
IRF9132	IRF9232
IRF9133	IRF9233
IRF9140	IRF9240
IRF9141	IRF9241
IRF9142	IRF9242
IRF9143	IRF9243

TO-220 Package N-Channel Types

IRF510	IRF741
IRF511	IRF742
IRF512	IRF743
IRF513	IRF820
IRF520	IRF821
IRF521	IRF822
IRF522	IRF823
IRF523	IRF830
IRF530	IRF831
IRF531	IRF832
IRF532	IRF833
IRF533	IRF840
IRF540	IRF841
IRF541	IRF842
IRF542	IRF843
IRF543	SSP3N70
IRF610	SSP4N70
IRF611	SSP4N60
IRF612	SSP6N70
IRF613	SSP6N60
IRF620	SSP6N55
IRF621	SSP4N60
IRF622	SSP4N55
IRF623	SSP4N50
IRF630	SSP4N45
IRF631	SSP5N40
IRF632	SSP5N35
IRF633	SSP7N20
IRF640	SSP8N20
IRF641	SSP7N18
IRF642	SSP8N18
IRF643	SSP7N15
IRF710	SSP8N15
IRF711	SSP7N12
IRF712	SSP8N12
IRF713	SSP12N10
IRF720	SSP10N10
IRF721	SSP12N08
IRF722	SSP10N08
IRF723	SSP12N06
IRF730	SSP40N06
IRF731	SSP10N06
IRF732	SSP12N05
IRF733	SSP10N05
IRF740	

TO-220 Package P-Channel Types

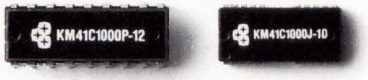
IRF9510	IRF9610
IRF9511	IRF9611
IRF9512	IRF9612
IRF9513	IRF9613
IRF9520	IRF9620
IRF9521	IRF9621
IRF9522	IRF9622
IRF9523	IRF9623
IRF9530	IRF9630
IRF9531	IRF9631
IRF9532	IRF9632
IRF9533	IRF9633
IRF9540	IRF9640
IRF9541	IRF9641
IRF9542	IRF9642
IRF9543	IRF9643

TO-126 Package N-Channel Types

IRFA1Z0	IRFA1Z3

DRAMS

1Mb DRAMs!



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KM44C256	256K x 4	Fast Page mode	100,120	DIP,ZIP,SOJ	3Q '88
KM44C258	256K x 4	Static Column mode	100,120	DIP,ZIP,SOJ	3Q '89
KM41256	256K x 1	Page mode	120,150	DIP,ZIP,PLCC	Now
KM41257	256 x 1	Nibble mode	120,150	DIP,ZIP,PLCC	Now
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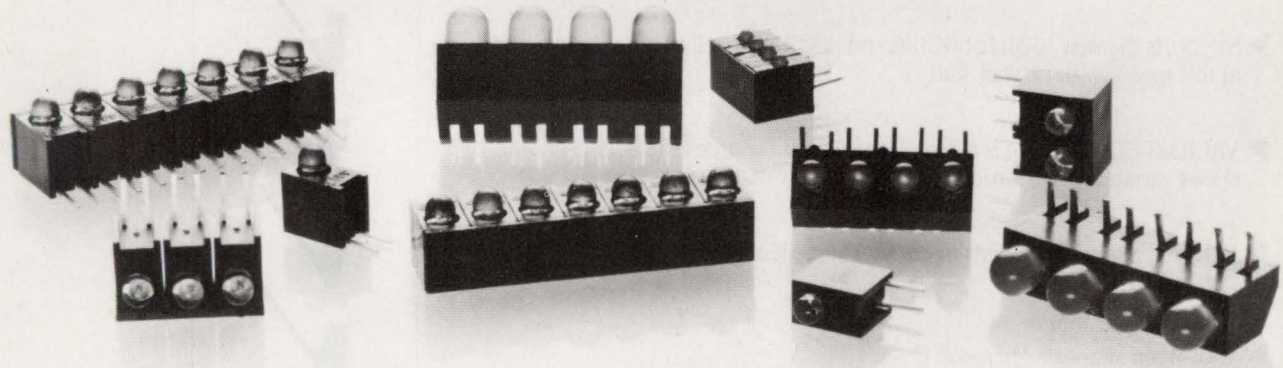

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CIRCLE 13

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▶ Tool chain supports Microsoft C (Also other versions of C and Pascal, FORTRAN, PL/M, Assembler, Jovial)	✓	
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CIRCLE 14

X-RAY LITHOGRAPHY USES CONVENTIONAL RESISTS

Combining a high-power, laser-based X-ray source with advanced mask-reticle technology, Hampshire Instruments Inc.'s new X-ray stepper system delivers submicron geometries using conventional photoresists. The Marlboro, Mass. startup company recently demonstrated a prototype of its Series 5000P stepper, which the company says especially suits such leading-edge designs as 4- and 16-Mbit dynamic RAMs. Company officials claim that the stepper is two years ahead of optical steppers in its ability to resolve device geometries and spacings of less than 0.5 μm. Hampshire uses a patented neodymium-glass pulsed laser source that's extremely intense to generate soft X-rays in the 0.8- to 2.2-nm range—the short wavelengths required for submicron lithography. First production systems of the $2 million stepper are scheduled for delivery next July.LC

CODE GENERATOR PROGRAMS AT&T DSP CHIP

A PC-based, high-level development system is the first code generator to automatically convert high-level "FlowGrams" into an application. A FlowGram is a block diagram created with function blocks (such as FFTs), signal generators, filters, and arithmetic and trigonometric functions, as well as the block interconnects. Until now, writing an application for a signal processor required programming in assembly or C. However, the DSPlay XL/32, a $1495 software package from Tucson, Arizona-based Burr-Brown Corp., converts the user-created FlowGrams into code, which can be downloaded and executed on the AT&T DSP32 chip that resides on the company's DSPeed processor board ($995). AT&T is also currently beta-siting its own DSP32 C compiler, which is expected in October.

There are two ways to execute Burr Brown's FlowGrams: Continuous or block. Continuous-mode programs run in a loop where analog data can be input, processed, and put out in real time. To harness the power of optional analog I/O boards, users can add serial input and output blocks to their FlowGrams. In block mode, the functions are executed one at a time, so the results of each block can be viewed and analyzed. The software includes a filter design package, and an assembler and debugging environment.BP

ECL LOGIC FAMILIES RUN WITH 3-GHz CLOCKS

A pair of bipolar processes developed at Tokyo's Fujitsu Ltd. has spawned a trio of ECL logic families that will soon arrive in the U.S. through Fujitsu Microelectronics Inc., of San Jose. These families offer a choice of functions optimized for speed, power, or pin compatibility. Aimed at the highest performance applications, the MB880 series is built with a 0.5-μm polysilicon emitter structure and operates at clock rates of 3 GHz. The speed has its cost, though—each logic function (gate, flip-flop, multiplexer, demultiplexer, and so forth) consumes 250 to 1200 mW. To minimize signal propagation delays and crosstalk, the chips come housed in the company's proprietary button-size "hockey-puck" packages, which have radial leads.

A more relaxed process with 1-μm emitters is used to build the power-optimized MB810 family and the pin-compatible 10KHL series. The initial MB810 series will have a lower peak operating frequency of 1.5 GHz, dissipate less power—from 50 to 150 mW—and come in the more familiar DIP and flat-package options. The 10KHL series drops into sockets already established for Motorola's 10KHL ECL logic family. The difference: Fujitsu's bipolar process cuts power dissipation to half that of the 10KH series—just 13 mW/gate.DB

COMING UP: VARIATIONS ON ASPECT PARTS

National Semiconductor Corp. is readying advanced bipolar, CMOS, and biCMOS processes for use in high-density gate arrays and standard cell systems. In making a variation of the second-generation Aspect (advanced single-polysilicon emitter-coupled technology) process, which adds more metal layers, the Santa Clara, Calif. company expects to employ 1.5-μm emitter dimensions and four levels of metal interconnections for a high-density ECL gate array that it should release by year's end. The array will offer about 30,000 gates—double that of currently available arrays—and gate propagation delays of 100 to 120 ps. A next-generation version of the process with 0.8-μm emitters—Aspect III—is expected to be in place by late 1989 or early 1990.

Channel-free CMOS logic arrays with 50,000 to 150,000 usable gates and more than 400 I/O pads are also in development. A 1-μm drawn channel length will be used to make some of the arrays in 1989, and the company expects to shrink the dimensions by 20% in 1990 for the most complex chips. High-density biCMOS arrays, with up to 20,000 gates and 64 kbits of static RAM, are also in development with a 1-μm process.DB

DSP Development Now On The MAC II

Spectral Innovations of Sunnyvale, Calif. has released MacDSP for the Macintosh II—a DSP32-based accelerator with 64 kbytes of program and data memory. With the addition of an optional, programmable, 16-bit, 125-kHz analog input, and an output card ($486), users can interactively operate on data and observe the effect of the function they are applying. Harnessing the power of the Macintosh's graphics, the MacDSP renders a 256-line, 62-kHz bandwidth spectrogram with full color in real-time.

MacDSP comes with a wide range of signal-processing functions. AT&T's DSP32 assembler and simulator for the Macintosh is expected this month, and the C Compiler is two months away. The MacDSP is priced at $2249 for the 8-MFLOPS version; $2745 for the 12-MFLOPS version. When AT&T releases the enhanced CMOS version of the DSP32 (expected this month), Spectral Innovations will ship a 25-MFLOPS board ($3241). The company also plans to ship a speedy 1-MHz data acquisition card (at about $600) based on Datel's ADC508 analog-to-digital converter.BP

ULSI RISC Chip Makes Sun Clones Possible

An ultra-large-scale RISC CPU that integrates about 1 million transistors is on the way from Solbourne Computer Inc., of Longmont, Colo. The circuit will form the basis for a superworkstation that's planned for a second-half 1989 introduction. On a single piece of silicon, this chip will combine four different functions: the integer CPU, floating-point processor, instruction and data caches, and a memory management unit. These functions require several chips in current RISC designs. Featuring full 64-bit-wide data paths, the RISC chip is built in a submicron CMOS process. More than $50 million in funding from Matsushita Electric Industrial Co., Ltd. is being pumped into the circuit's development.

The future workstation will be compatible with the Scaleable Processor Architecture and Application Binary Interface proposed as RISC standards by Sun Microsystems and AT&T. The Sun clone will feature a multiprocessor architecture that can handle up to eight of the ULSI processors working together. Smaller machines will be field-upgradeable by plugging in additional ULSI-based processor boards. Though the focus of the development effort is on the workstation, Matsushita has indicated that it may later offer the ULSI chips on the merchant market.WRI

IBM Announces Fastest 64-kbit CMOS RAMs Yet

Two 64-kbit CMOS memory chips—touted as the fastest in the world—were just introduced by IBM at the 1988 VLSI Circuits Symposium in Tokyo (August 22–24). Designed to run at liquid nitrogen temperature (77K), the first chip boasts an access time of only 3.5 ns—the fastest reported for any technology at 64 kbits. This ultra-fast speed comes from extremely low temperatures and small-signal ECL interfaces. The RAM is built in a dual 0.5-μm-gate polysilicon process to optimize the low operating-temperature advantages, which doubles room-temperature speed and cuts the power-delay product.

The second chip, which runs at room temperature, has an access time of 6.2 ns and is currently the only sub-10-ns CMOS RAM with an ECL interface. High performance comes from selectively scaled processing and an innovative circuit design that employs fully clocked CMOS amplifiers instead of simple, tapered inverters. Using optical lithography to obtain a 0.5-μm channel length, the CMOS processing offers speeds that are more than twice those of the previous 1.1-μm TTL designs. Simulation results have shown that access times of 4.8 ns are possible if the large diffusion areas that are caused by selective scaling can be reduced.LG

Germanium Returns For Rad-Hard ICs

Researchers at the Electro-Optical and Data Systems Group of Hughes Aircraft Co., in El Segundo, Calif., have crafted what they believe to be the first large-scale IC with germanium-junction FETs. The IC runs at cryogenic temperatures and should withstand a nuclear detonation in space. The circuit performs the readout function required by high-sensitivity, infrared, focal-plane arrays—and it can do so at lower power-consumption levels than silicon-based technologies. Developed as part of a project funded by the Strategic Defense Initiative Organization, the readout circuit operates with a silicon detector array, and combines the information received from all the detectors. By basing such a combination of circuits in an observation satellite, defense systems will perform surveillance, acquisition, tracking, and even assess the kill capability of a ballistic missile during the weapon's midcourse flight outside the earth's atmosphere.DB

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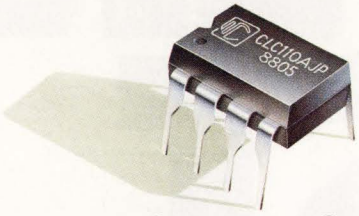
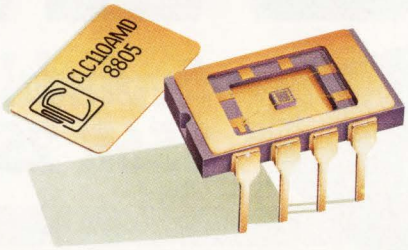


400ps rise time and −60dBc distortion at 50MHz. Suddenly, the buffer gets interesting!



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The CLC110 is ideal for high-speed line driving and video distribution. It's also a great choice for driving capacitive loads, especially in the newest 100 to 200MSPS flash A/D converters; its fast 750ps group delay, 800V/μs slew rate and 400ps rise time make it excellent for op amp feedback loops as well.

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CIRCLE 15

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MT5C2565	64K X 4 $\overline{OE}$	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C6404	16K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C6405	16K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 S. I/O	**15ns**	PDIP, CDIP, SOJ
MT5C6408	8K X 8	**15ns**	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C1604	4K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 S. I/O	**15ns**	PDIP, CDIP, SOJ
MT5C1608	2K X 8	**15ns**	PDIP, CDIP, SOJ

*Slower speeds also available.

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CIRCLE 16

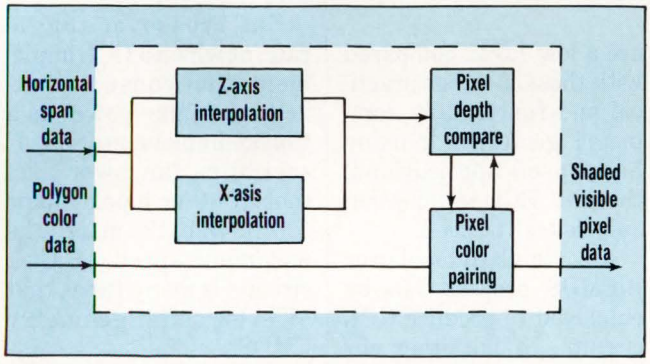
FAST GRAPHICS ALGORITHM REMOVES HIDDEN SURFACES

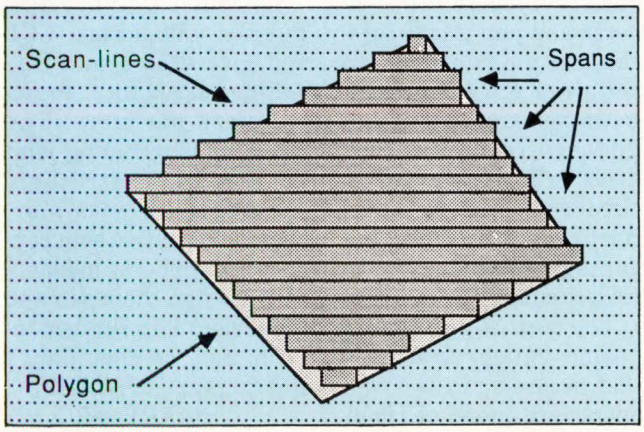
A pixel-processing algorithm that takes out hidden-surface coordinates on-the-fly—without using a Z-buffer—was developed and patented by San Diego-based Megatek Corp. Named Xpan, the algorithm was demonstrated at Siggraph this summer.

Traditionally, a real-time graphics simulator is engineered with a Z-buffer. Here, a computational engine calculates all hidden surfaces for objects on a screen, and stores these coordinates for future Z-buffer use (for an example, see ELECTRONIC DESIGN, July 23, 1987, p. 143). Consequently, hidden surfaces—such as the far side of a mountain—are revealed to the graphics system operator just by pulling the data from the Z-buffer.

There's several problems with Z-buffer architectures, though: They're expensive and slower than they need be for a simulator that must compute and render more than 3D million pixels/s. Many Z-buffers are constructed with 20-ns static RAMs, and because the graphics engine must invariably calculate the coordinates for something which may never be shown, it wastes valuable clock cycles.

As implemented on the company's Model 928 display system (a simulator employed by the U.S. Navy as part of its Tower Operating Training System program), Xpan can supply a 5X speedup over systems using a Z-buffer.





According to Todd Heckel, principle architect of the 928 hardware, the key to fast hidden-surface removal is identifying all visible elements of a picture just before it must be portrayed on a screen. Using the Xpan algorithm, the displayed polygons are first scan-converted vertically into horizontal segments, called "spans." In the second step, the horizontal scan conversion transforms the spans into pixels.

This two-step process depends on the use of a span processor and a link list buffer. For each polygon portrayed on the screen, the span processor extracts span information; that is, the intersection of each polygon with the scan lines of the raster display device. The span information includes the horizontal location of the scan line, its color, and the intensity (or Z-depth)—not for the whole span, but just left and right end points of the span. A multiple linked-list buffer stores the span information, ordering it according to the vertical screen location.

While the Xpan algorithm requires a span processor and linked-list buffer, besides normal frame buffers, it uses less hardware and software than traditional frame buffer architectures. "Each scan-line buffer is cleared as the data is transferred to the frame buffer," says Heckel. "Thus there is none of the overhead of a traditional full-sized Z-buffer." On a 1280-by-1024-pixel screen, a Z-buffer could take a full 8 ms—25% of the frame time at 30-Hz refresh rates—just to clear the screen.

STEPHAN OHR

BIPOLAR PROCESS BUILDS DUAL 1.5-GHZ FLASH ADC

Aimed at building the ultimate high-speed analog and digital ICs, Tektronix's latest bipolar process incorporates virtually every technique of the process engineer's art. Called simply the GST-1, its 15.5-GHz f_t npn transistors make possible two identical 4-bit flash analog-to-digital converters on one chip, capable of sampling 750-MHz sinewaves at 1.5 GHz. The 750-MHz Nyquist frequency is the highest reported for a monolithic a-d converter.

The double-polysilicon process uses 1-μm patterns, trench isolation, and self-aligning methods to build devices, which mate their speed with a current gain of 100. Contactless resistors and a single interconnect layer of emitter-collector polysilicon creates a dense layout with minimum interconnection parasitics and delays.

Rather than the usual use of interconnect metal, a stripe of silicided polysilicon forms the untrimmed reference divider. The two a-d converters contain 1700 active devices, which take up about 2600 mils^2 of silicon area.

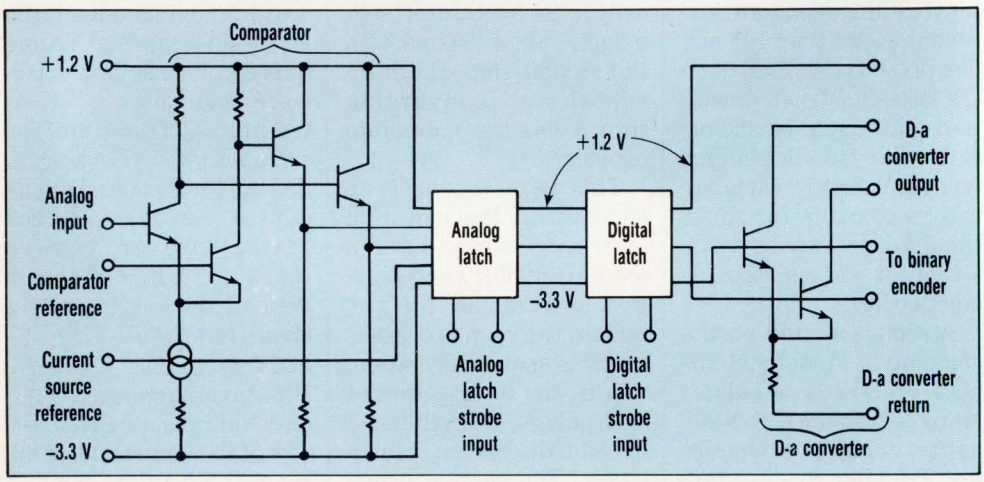
The basic design of both converters is typical of the flash genre: 15 comparator-latch chains, followed by a thermometer-code-to-binary encoder. Each flash converter also contains its own 4-bit digital-to-analog

converter on its output. Formed from current switches connected to the output of the comparator-latch chains, in parallel with the input to the encoder, the d-a converters make possible easy and detailed testing and evaluation of the chip's critical front end.

The chip's two converters operate independently on two separate signals. They alternately sample a single input, in a ping-pong mode, to double the sampling rate. The chips are either cascaded to form a 5-bit converter, or pipelined with extra components to form a higher-resolution multistep converter.

The chip operates from a 5-V nominal power supply and dissipates 1.5 W. It accepts an input signal of 1 V pk-pk. The process and chip will be described at the upcoming Third Annual IEEE Bipolar Circuits and Technology Meeting, September 12-13, Minneapolis.

FRANK GOODENOUGH



NEW NONSATURATING LOGIC OUTRUNS ECL AND DISSIPATES LESS POWER

A fundamentally new form of nonsaturating, high-performance logic—trademarked Current Coupled Logic or CCL—works faster than comparable ECL circuits produced with the same process. What's more, the technology, developed by Computer Circuit Laboratories Inc., of Spokane, Wash., consumes only about one-sixth the power of ECL. Simulated using published parameters from Motorola's Mosaic III bipolar production process, the worst-case CCL NOR gate delay—with a fan-out of three—is 197 ps.

CCL technology has the potential to deliver important gains in circuit performance, even at military temperatures. Numbers for logic delay, packing density, power thriftiness, and manufacturing costs could substantially improve, the company says. And these gains need not be mutually exclusive. Depending on the design context, several might be achieved simultaneously.

The technology owes its speed and power thriftiness to its simplicity and to nonsaturating transistor circuits. A CCL design uses roughly half the transistors needed by a functionally equivalent ECL design. CCL circuits, the company claims, make use of a more sophisticated metal pattern for power distribution than other technologies offer. Also, CCL power-supply levels are a low 1.5 V, compared with those of other practical and functionally complete logic forms. In many high-speed applications, the –2-V ECL termination supplies can be used.

Any standard bipolar or BiCMOS process can be employed to produce CCL circuits. Unlike other circuits, which require inverse and pnp transistors, the new implementation requires only forward-mode npn transistors and diffused resistors. Produced in any process, CCL circuits maintain the same relative performance advantage, compared with ECL circuits.

The new logic boasts unique gating structures that, according to its developers, are more efficient and versatile than ECL series gating. CCL technology mandates no sacrifice in the ability to route signals, as do other low-voltage logic forms, such as I^2L.

Computer Circuit Laboratories' defined cell library includes all essential logic functions, along with both TTL- and ECL-compatible input/output cells. Accordingly, designers can use the library to implement the core logic of upgraded replacements for industry-standard TTL and ECL parts.

The company claims that CCL technology outperforms CMOS for dense, high-performance digital VLSI circuits. Because CCL circuits, like ECL chips, have little dynamic power consumption, they consume less power than equivalent CMOS circuits at toggle rates greater than about 10 MHz, depending on the relative feature size.

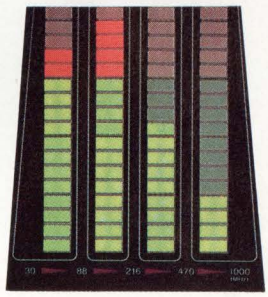
The crossover toggle rate, at which a CCL implementation consumes exactly the same power as a CMOS implementation, is said to be far lower than that of other bipolar logic forms. What's more, the maximum speed of CCL circuits is many times that of even small-geometry CMOS.

Computer Circuit Laboratories will license CCL and give design and consulting assistance to its business partners. The company is pursuing joint ventures and strategic partnerships with merchant and captive semiconductor suppliers, independent design houses, and foundries. For further information, contact Chuck Hastings at (509) 455-8216.

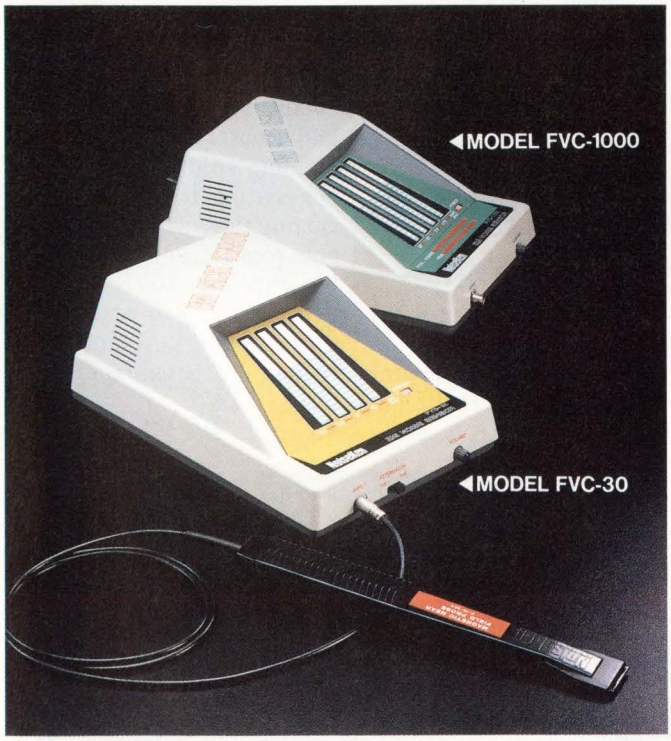
BARRY PHILLIPS

NoiseKen

FCC
VDE
VCCI
CISPR



Three points on the display is a criterion for your success in the protective measures to reduce emissions.
Our wide experience in EMI solutions has proven that even products with long wiring or flat cable of high efficiency of radiation are almost sure to clear FCC Class B limits for radiated emissions, if the reading on the FVC-1000 display is not higher than three points.



The FVC series locates sources of EMI

EMI Noise Sensor

Model FVC-1000 Model FVC-30

Features

1. The FVC-1000 can detect and locate sources of radiated interference in electronic equipment.
   The FVC-30 can detect and locate sources of conducted interference in electronic equipment.
2. The user can readily evaluate the effectiveness of protective measures to reduce emissions.
3. For each classified frequency band based on the FCC, VDE, VCCI and CISPR standards, the FVC series measures electric field strength and magnetic field strength individually, which are potential sources of EMI.
4. An electric near field probe and a magnetic near field probe of high sensitivity are furnished as standard accessories.

Equipment summary

	FVC-1000	FVC-30
Frequency range	30MHz～ 88MHz 88MHz～ 216MHz 216MHz～ 470MHz 470MHz～1000MHz ※Simultaneous 4 spectra measurement	100KHz～500KHz 500KHz～ 3MHz 3MHz～ 10MHz 10MHz～ 30MHz ※Simultaneous 4 spectra measurement
Display	20-point LED bar graph display for each frequency band.	20-point LED bar graph display for each frequency band.

NOISE LABORATORY CO., LTD.
2662-1, NOBORITO, TAMA-KU, KAWASAKI CITY, KANAGAWA PREF, 214 JAPAN
TEL(044)933-4311 FAX(044)932-4511

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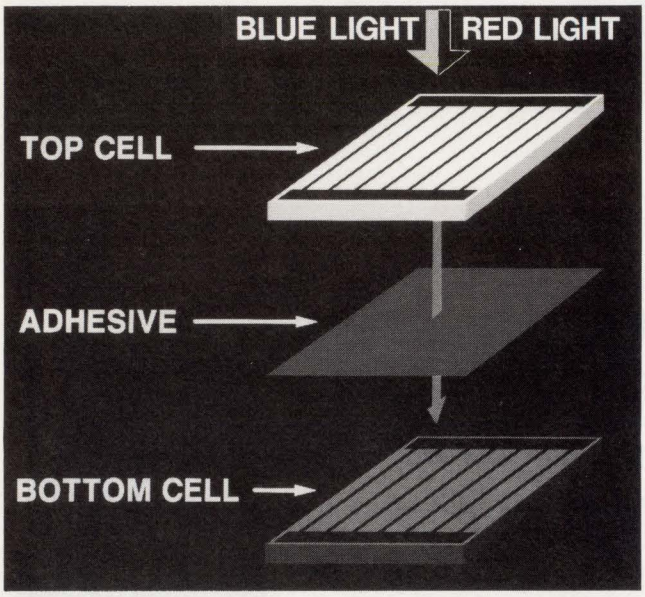
CIRCLE 17

PHOTOVOLTAIC SOLAR CELL SETS EFFICIENCY RECORD



Searching for an alternative to conventional power generation for the Department of Energy (DOE), scientists at Sandia National Laboratories, in Albuquerque, N.M., reached a 31% solar-to-electric conversion rate with a new photovoltaic cell design. By comparison, commercially available photovoltaic concentrator cells are now only 18% to 20% efficient.

The new cell is a layered arrangement of gallium arsenide and silicon crystalline cells, and it's based on contributions to solid-state technology from Varian Associates Inc., Stanford University, and Sandia's Photovoltaic Cell Research Div. The record efficiency is reached with a concentrated light intensity of 35 to 50 W/cm^2—the equivalent of 350 to 500 suns.

Sandia's multijunction solar cell consists of two stacked cells, each with different light-acceptance characteristics (bandgaps) for absorbing more of the electromagnet spectrum than one cell. Optical concentrators focus energy from the sun onto the cells, grouped into modules to generate significant electrical current.

Developed under contract with Sandia by Varian Associates, the gallium-arsenide top cell converts light from the blue end of the light spectrum to electricity with a 27.2% efficiency. The crystalline silicon bottom cell, developed by Stanford, contributes a 3.8% conversion efficiency for the red end of the light spectrum. Because of light frequencies reflected or absorbed by the upper cell, the bottom cell has lower efficiency.

To reach an expected efficiency limit of 40%, the next step in the DOE's program calls for installing groups of cells in a high-efficiency module for field testing. The DOE's ultimate goals are expected to be reached by combing cell elements with higher efficiencies and using improved optical technology for concentrating up to 1000 suns onto one cell.

MILT LEONARD

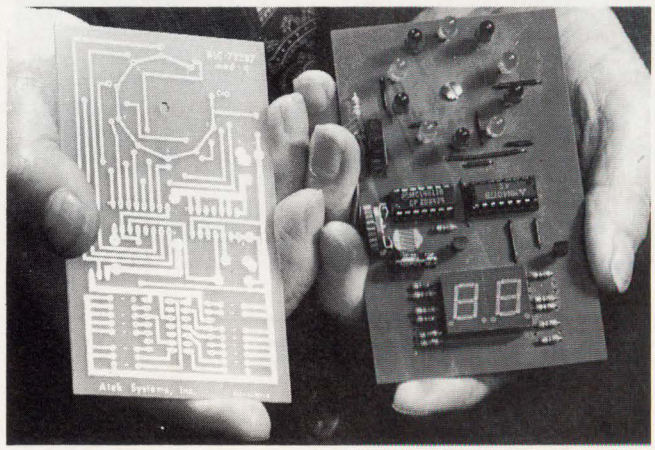
PC-BOARD MINIATURIZATION PROCESS REDUCES TIME, COST

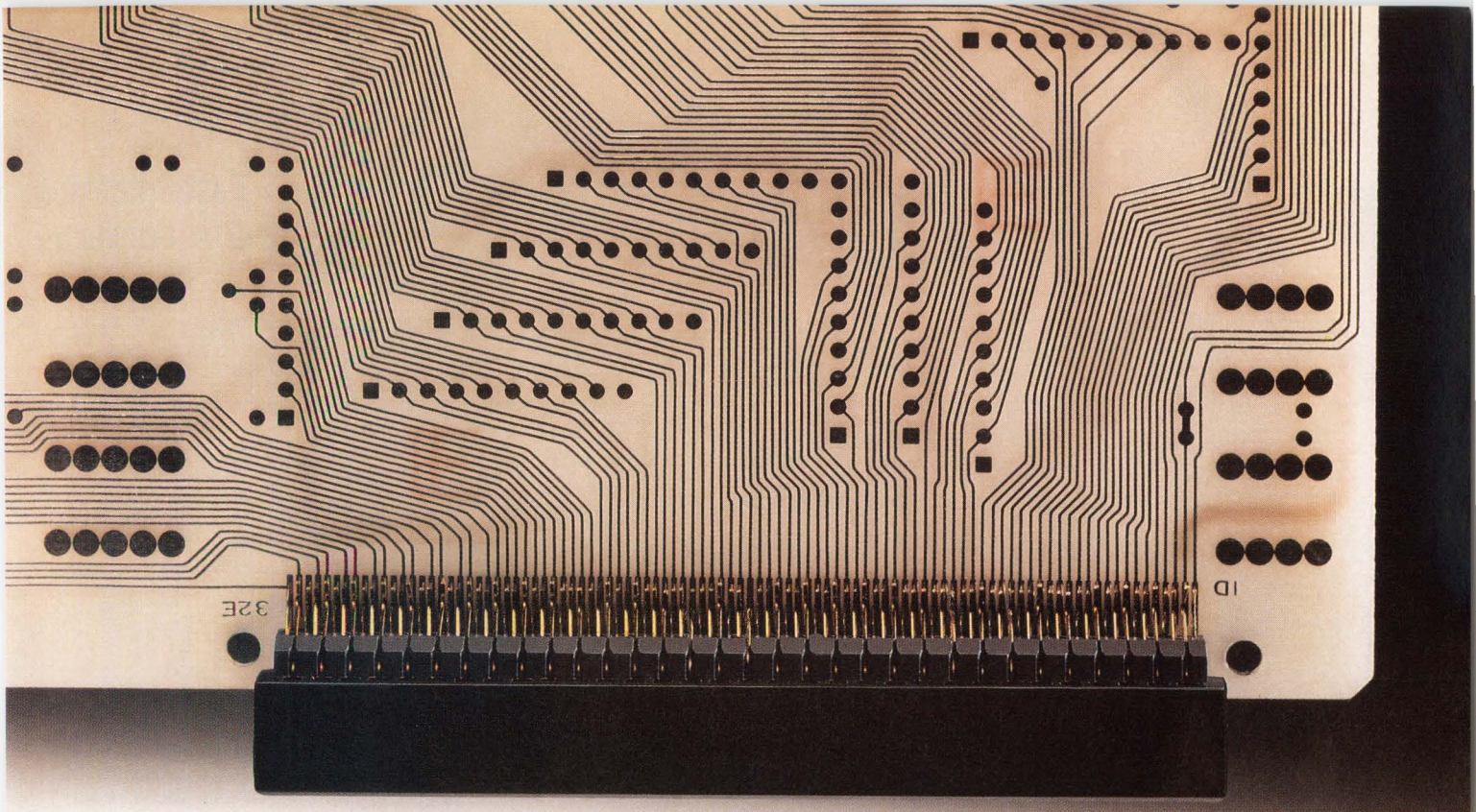
With its new system of manufacturing polymer-based pc boards, PrinTron Inc., of Scotch Plains, N.J., can reduce board size by up to 70%. Production speed is increased 50 to 100 times over conventional methods. Designated the PrinTron Process, the system results in savings up to 70% for board manufacturers.

Components can be directly soldered to the pc boards, which are being produced with 3-mil lines and spaces, and the company says are 100% error-free. Boards with 2-mil lines and spaces are still in experimental stages. In comparison, Conventional pc boards have line spacings of 7 to 10 mils. The process employs a metallic-graphic ink with a resistance rating of 1.8 to 2.0 $\mu\Omega$/cm, depending on the specific alloy used (the alloy used is determined by the board's application). The ink, which is non-conductive in its printed state, goes through a high-energy radiative-curing process to become a continuous alloy. This, in turn, makes the alloy electrically conductive. PrinTron doesn't etch the boards—it passes a brushing-detergent solution over the board to create the lines and spaces.

These procedures makes it possible for the PrinTron Process to condense the five steps of traditional pc-board manufacturing into one process. The five basic steps are: laminating the substrate with a copper foil; adhering a polymer and making a photo-image of the desired circuit; chemically developing the photo-polymer; etching away the unused copper and neutralizing the remaining solution; and solder-coating the board. By cutting these steps down to one, considerable time and labor are saved by the manufacturer. Eventually, these savings should be reaped by consumers as well.

RICHARD NASS

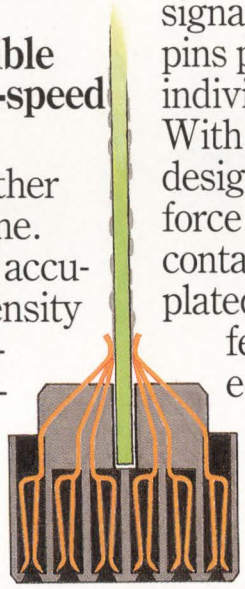




Mother and daughter have never been this close.

Augat introduces electrically compatible connectors for high-speed applications.

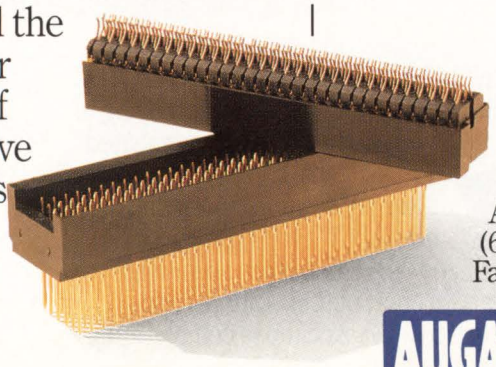
It's as though mother and daughter were one. That's how fast, how accurately, Augat high-density connectors speed signal processing, eliminate data loss and substantially reduce board space.



Now just one connector processes both power and signal. Hot-air-soldered to the PCB for stability via our simple, bench-top turnkey system.

Modular end caps for design flexibility. Up to 264 signal pins and 16 power pins per connector—individually replaceable. With patented press-fit design for an insertion force of just 1.8 oz. per contact. Selectively gold-plated on both male and female contacts for economy.

To find out more about our new 4- and 6-row high-density connectors—or about all the ways our family of innovative products can improve yours—call Bernard Gudaitis direct at (214) 221-8776. Or send for a detailed brochure.



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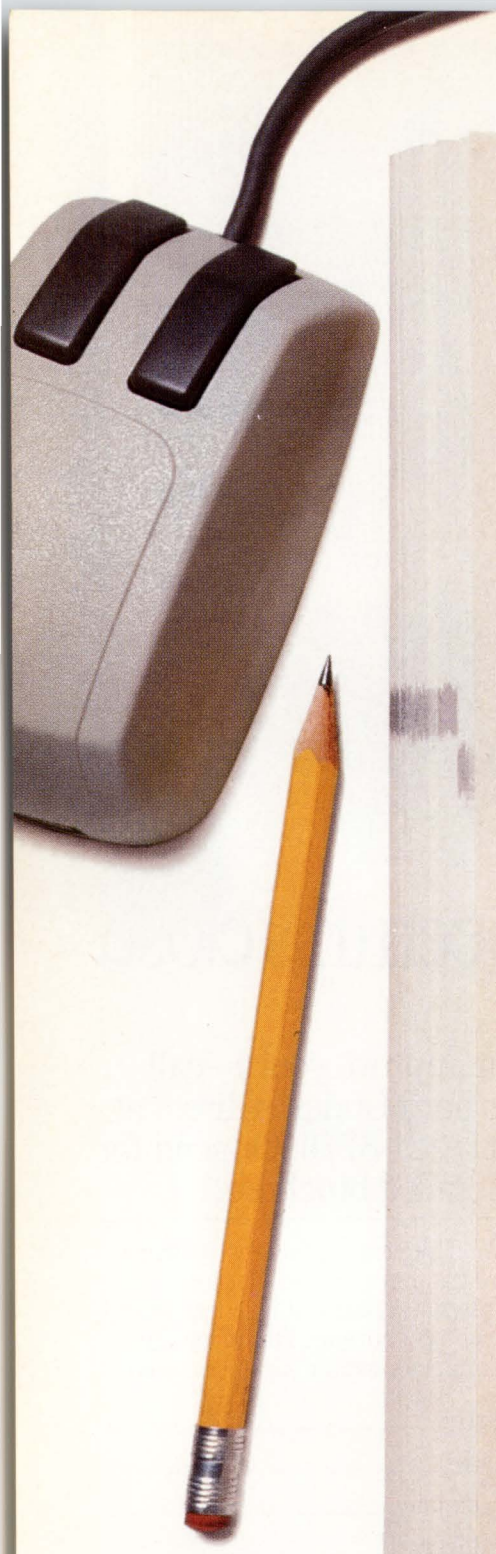
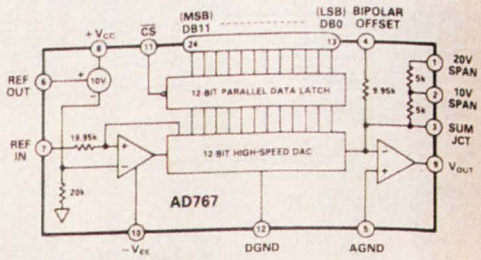


ANALOG DEVICES

Fast Interface 12-Bit D/A Converter

AD767

FEATURES
- **Complete 12-Bit D/A Function**
  - **On-Chip Output Amplifier**
  - **High Stability Buried Zener Reference**
- **Fast 40ns Write Pulse**
- **Guaranteed for Operation with ±12V or ±15V Supplies**
- **0.3" Skinny DIP Package**



AD767 Functional Block Diagram

PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried zener reference and input latch on a single chip. The converter uses 12 precision high-speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high-speed bipolar manufacturing process, and proven laser wafer-trimming (LWT) technology.

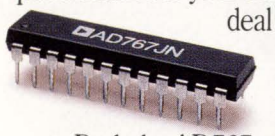
The subsurface (buried) zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5ppm/°C. The AD767 is packaged in a small, 0.3" wide, 24-pin DIP.

PRODUCT HIGHLIGHTS

1. Complete 12-bit DACPORT™:
   The AD767 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The input latch responds to write pulse widths as short as 40ns assuring direct interface with the industry's fastest microprocessors.
3. The internal buried zener reference is laser trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full-scale and bipolar offset errors.
5. The precision high-speed current steering switches and on-board high-speed output amplifier settle within 1/2LSB for a 10V full-scale transition in 3.0μs when properly compensated.

DACPORT is a trademark of Analog Devices, Inc.

Bringing complete 12-bit DAC functionality and performance to your designs no longer requires having to deal with all the problems associated with external components. Instead, it simply requires specifying our new AD767 or AD7245.



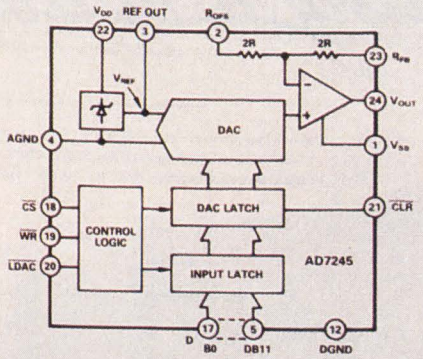
Both the AD767 and AD7245 feature an on-chip stable buried Zener reference, output amplifier and microprocessor interface logic. And these complete functions come packed into skinny 0.3" DIPs. All this means you no longer have to deal with error budgets, product characterizations, or space constraints related to external components.

If digital interface speed is what you're after, the AD767 responds to pulse widths as short as 40ns, allowing it to be used with today's fastest processors. On the other hand, if low power dissipation is critical to your application, the LC²MOS AD7245 consumes only 65mW. There's also

Low Power 12-Bit D/A Converter

AD7245

FEATURES
- Complete 12-Bit D/A Function
  - On-Chip Output Amplifier
  - High Stability Buried Zener Reference
- Low Power (65mW typ)
- Single or Dual Supply Operation
- 0.3", Skinny DIP Package
- 8-Bit Bus Version Available: AD7248



AD7245 Functional Block Diagram

PRODUCT DESCRIPTION

The AD7245 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The part features double-buffered interface logic with a 12-bit input register and 12-bit DAC register. The data held in the DAC register determines the analog output of the converter. The input register data is latched on the rising edge of $\overline{CS}$ and $\overline{WR}$ and data is transferred to the DAC register under control of $\overline{LDAC}$. An asynchronous $\overline{CLR}$ signal on the DAC register allows features such as power-on reset to be implemented. All logic inputs are level triggered and are TTL and CMOS (5V) level compatible, while the control logic is speed compatible with most microprocessors.

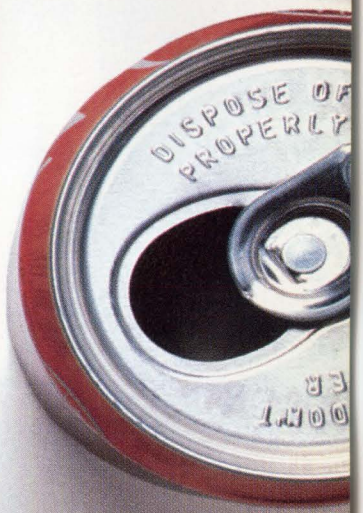
The on-chip 5V buried zener diode provides a low-noise, temperature compensated reference for the DAC. The gain setting resistors allow a number of ranges at the output: 0 to +5V, 0 to +10V when using single supply and −5V to +5V when operated with dual supplies The output amplifier is capable of developing +10V across a 2kΩ load.

The AD7245 is fabricated in an all ion-implanted high-speed linear compatible CMOS (LC^2MOS) process and is packaged in a small, 0.3" wide, 24-pin DIP.

PRODUCT HIGHLIGHTS

1. Complete 12-bit DACPORT™:
   The AD7245 is a complete voltage output 12-bit DAC on one chip. This single-chip design of the DAC, reference and output amplifier is inherently more reliable than multi-chip designs.
2. Single or Dual Supply Operation:
   The voltage-mode configuration of the AD7245 allows operation from a single power supply rail. The part can also be operated from dual supplies to allow a bipolar output range.
3. Low Power Consumption:
   CMOS fabrication results in very low power consumption (65mW typical in single supply). This low power allows the part to be packaged in a small 0.3" wide 24-pin DIP.
4. Versatile Interface Logic:
   The high speed logic allows direct interfacing to most 16-bit microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7245 in multiple DAC systems. The part also features an asynchronous $\overline{CLR}$ input.

DACPORT is a trademark of Analog Devices, Inc.



FINALLY, THE COMPLETE STORY ON COMPLETE 12-BIT DACs.

an 8-bit bus version of the AD7245 (the AD7248) that loads in two bytes.

Whether your need is determined by speed or power dissipation, it doesn't have to be limited by price. Our DACs come complete for as little as $8.40 (1000s).

To find out how the AD767 and AD7245 can tend to your complete 12-bit DAC needs, call Applications Engineering at (617) 935-5565 Ext. 2628 or 2629. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

ANALOG DEVICES

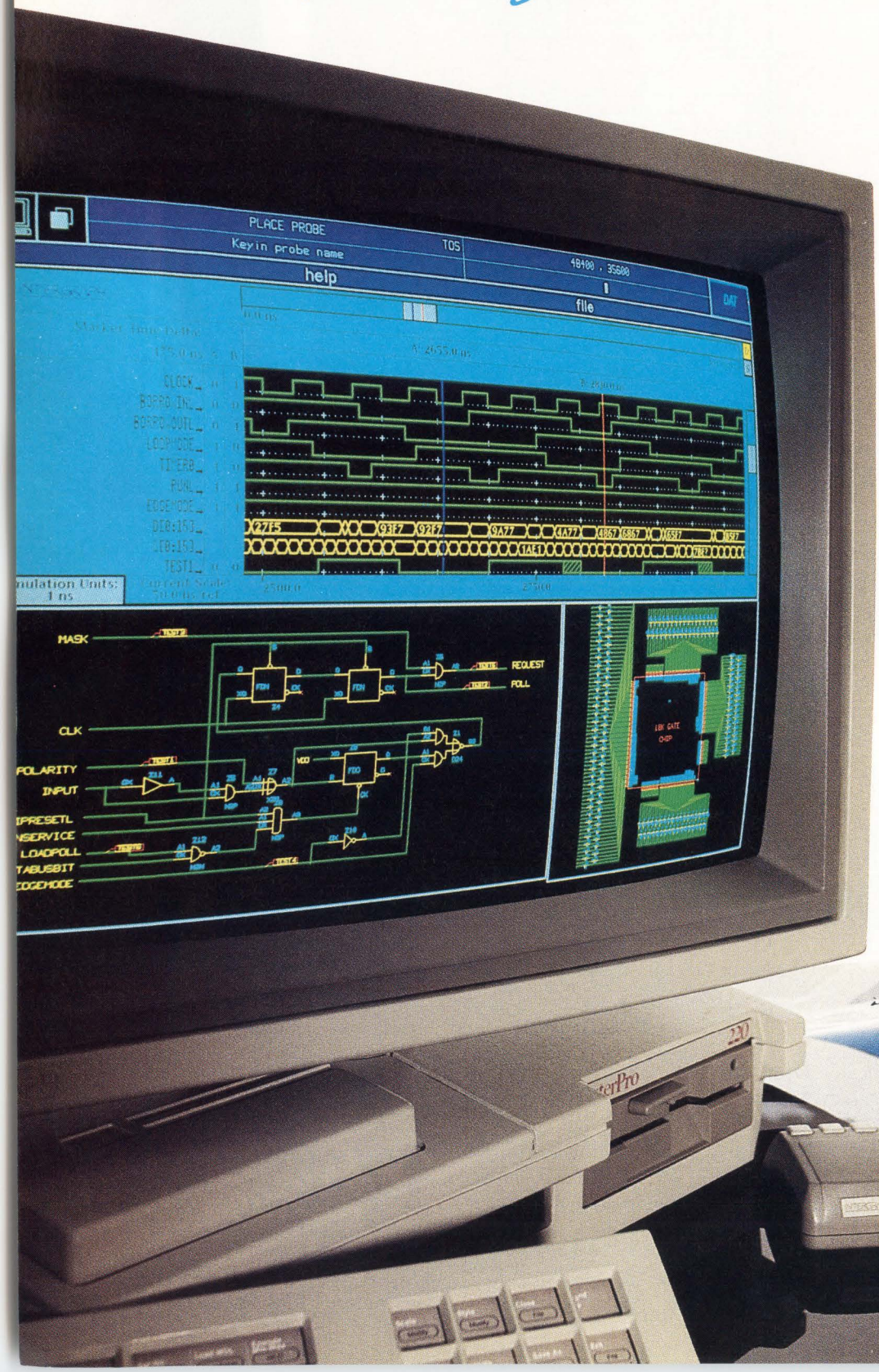
Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 559-2037; Colorado: (719) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 251-9550; Austria: (222) 885504; Belgium: (3) 237 1672; Denmark: (2) 845800; France: (1) 4687-34-11; Holland: (1620) 81500; Israel: (052) 911415; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050

CIRCLE 19

Simple as...

pushing a button

DESIGN ENGINEER	ASIC
CSPICE	PLD
HILO	LAYOUT



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CIRCLE 20

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INTERGRAPH

CAE ACCELERATORS RACE TO KEEP UP WITH GATE COUNTS

WITH ASIC GATE COUNTS REACHING 100,000, ONLY DEDICATED ACCELERATORS—THE ULTIMATE RISC MACHINES—KEEP SIMULATION RUN TIME IN CHECK.

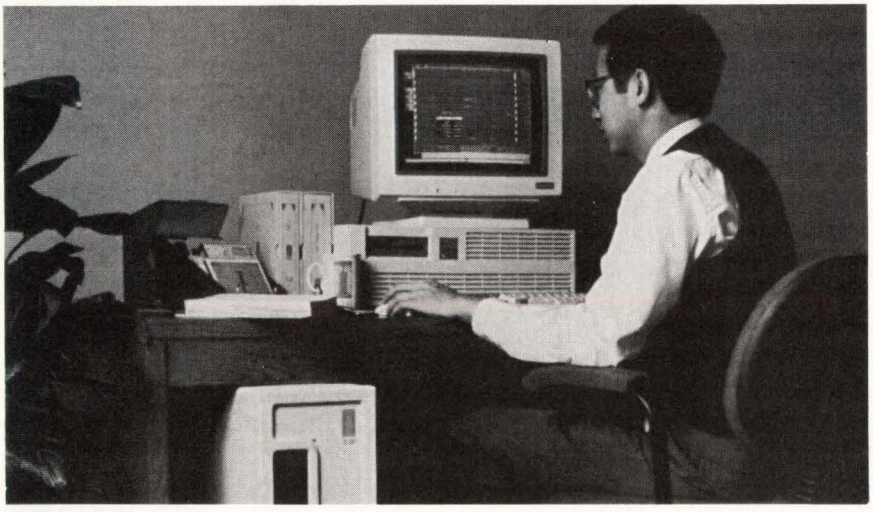
JOHN BOND

Engineering workstations and larger computers have changed the way electrical engineers design circuits. But simulating gate-level designs strains the resources of most computers. With the growth of higher-density ICs—several with up to 100,000 gates on one array—logic simulation and testing inevitably requires more computing power than is available from general-purpose computers.

Dedicated hardware CAE accelerators offer a solution. By reducing the number of instructions to only those needed to simulate a logic gate, the simulation runs much faster—often 10 to 100 times faster—than even the largest computers available.

Accelerators are needed because logic simulation is essentially an "unbounded task." The more you do it, the better the design, although it's impossible to attain 100% certainty.

But the amount of time a computer runs a simulation program doesn't grow linearly with the number of gates being simulated. It's an *n*-squared problem. That is, if the number of gates in a circuit is doubled, it requires four times the computer power, in MIPS and memory, to simulate the circuit at the same speed as before. This is because the computer



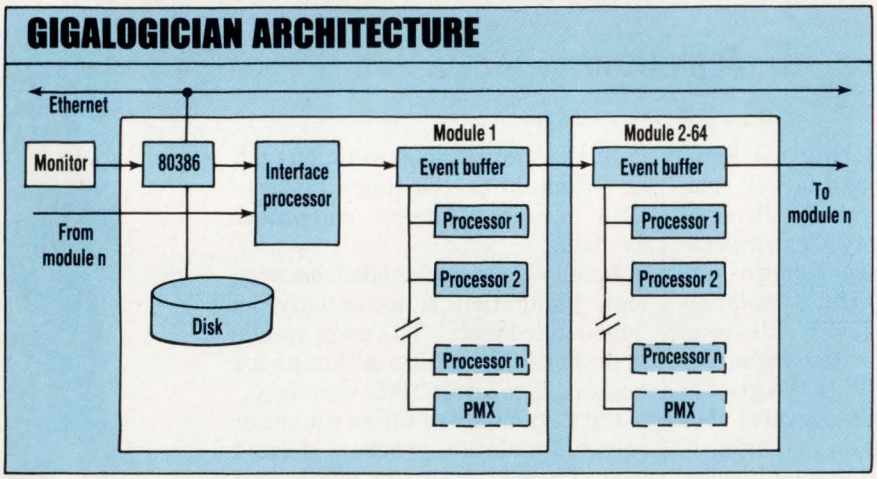
1. THE IKOS SIMULATION System links with most major platforms and CAE environments to furnish accurate, fast ASIC simulation. The Ikos 1900 processes 15 million events/s.

must run the simulation program over and over again to depict every possible output pattern. The simulation of a two-gate circuit, for example, must be run four times (n^2) to depict all combinations of outputs.

Fault simulation, similarly, is an n-cubed problem, since the entire combination of outputs is considered once with inputs "stuck at 1" and again with inputs "stuck at zero." When circuit size is doubled, it takes eight times as much power to accomplish the same job.

performs an output operation. The result is a logic output that simulates the gate's activity. By using only logic functions that can be expressed as AND, OR, NAND and NOR gates, the instruction set shrunk.

With ASIC gate densities increasing, to accurately simulate the behavior of a circuit, many test cases must be run through each gate, requiring many events—outputs of gates that are changing state—to be generated. It's in these numbers—events per second—that CAE accelerators strut their stuff: A typical software simulator running on a fast workstation or a mainframe runs around 10,000 events/s. A basic Ikos simulation accelerator, in contrast, might run from 500,000 to 1 million events/s in full timing mode or 10 million events/s for a functional check. This is only one example.



2. THE ARCHITECTURE of the Daisy Gigalogician, optimized for mixed-level simulation, is tightly coupled into the Daisy design environment.

Accelerators do their work by running simulation software algorithms in hardware, and that takes a special kind of computer. Computers exist within a spectrum from general-purpose, very flexible, highly programmable machines to special-purpose, nonprogrammable ones. On that spectrum a RISC processor, for example, has a simpler architecture and can therefore run faster than the most general-purpose CISC machines. If that concept is carried even further in the direction of much more simplified instructions, you eventually arrive at the position that the accelerator holds on the spectrum.

A simulation accelerator such as Zycad's Logic Evaluator (LE), for example, specifies only in Boolean logic. It has very simple instructions that represent all gate-level activity with three input states and one output state. When data comes in—that is, when an input changes—the accelerator refers to a truth table or

The Ikos architecture uses a table of primitives stored in high-speed RAM to mimic the function of gates. The basic primitive used by Ikos is a four-input, one-output device. The output can be programmed to be any Boolean combination of the four inputs. It's designed to quickly perform a narrow set of tasks.

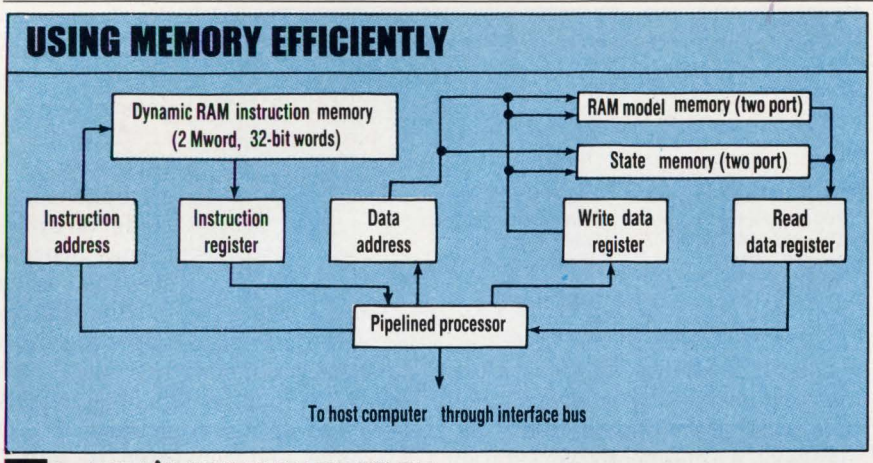
Ikos focuses on verification and takes inputs from virtually all design systems—CASE, Daisy, Futurenet, Mentor, P-Cad, Valid, and so on. Ikos systems do some board-level simulation, primarily of multiple ASICs and memory. Ikos is also working on accelerated behavioral simulation.

An Ikos system consists of software that runs on the host and a hardware simulator module that comes in two sizes. The current Ikos product module is a special-purpose card cage designed specifically to do fast simulation. It comes with attachments for three platforms—Apollo, PC AT, and Sun—and it will soon be available for Intergraph workstations. Each card simulates up to 20,000-gate circuits at 1 million events/s *(Fig. 1)*. For larger circuits, designers can add evaluator cards to achieve a type of parallel processing.

The simulator's software includes a waveform-capture package that lets designers use a mouse to draw out all the waveforms to be employed as test vectors. A new board-level product, expected shortly, allows behavioral programs that run concurrently on a workstation host to communicate with gate-level simulations running on the accelerator card.

Whereas the typical computer is programmed with high-level languages and instructions, a Zycad accelerator is programmed with a net list in binary form, which front-end software makes transparent to the user. The interface reads a standard text language like HILO and translates the gate descriptions into the correct format for the accelerator. Or it can read the diagrams on a workstation and translate that to the accelerator.

Although accelerator performance is often measured in events/s or evaluations/s, the key to performance is a shorter design cycle. For that you need library models and a good debugging environment. Daisy Systems Corp. maintains that net-list driven accelerators don't supply tight enough coupling between tools. Daisy's accelerators are tightly integrated into the complete CAE environment, from schematic entry through layout. While running a simulation, users can open a schematic and probe a node on that schematic. The company's accelerators furnish a full history—the results of the simulation up to that point for the node—making it easier to track down problems.



3. AIDA'S COSIM HARDWARE accelerator is suited to large-scale synchronous design, especially level-sensitive scan design. With a capacity of up to 8 million gates, it models memory and performs up to 10 million gate evaluations/s.

By contrast, most standalone accelerators take in net lists from a variety of environments and are optimized for gate-level simulation. They translate the inputs into three-input NAND gates or a fixed set of primitives. Most accelerators don't support behavioral modeling, although some do support it on the host computer. The Daisy accelerator, however, is one of the few mixed-level simulators. It can perform simulation at the gate, switch, functional, behavioral, and physical levels.

Daisy has two architectures in its family line: the Megalogician, with a microcoded architecture, and the Gigalogician *(Fig. 2)*, an expandable parallel computer. The Gigalogician has two kinds of processors in parallel. Hardwired (dedicated-function) processors implement the simulation algorithm in silicon, and microcoded (reprogrammable) processors handle behavioral modeling and memory components. Fault simulation, which runs on the Megalogician, is being developed for the Gigalogician. The low-end Personal Megalogician is targeted toward ASIC design but can also be used for system-level simulation because it does full mixed-level simulation.

The Aida COSIM accelerator board plugs into Apollo and Sun systems *(Fig. 3)*. A subsidiary of Teradyne Inc., the company focuses on the relationship between simulation and testing. Its products are geared to designers of large, complex systems who favor synchronous design. Such designers often implement scan design to ensure testability.

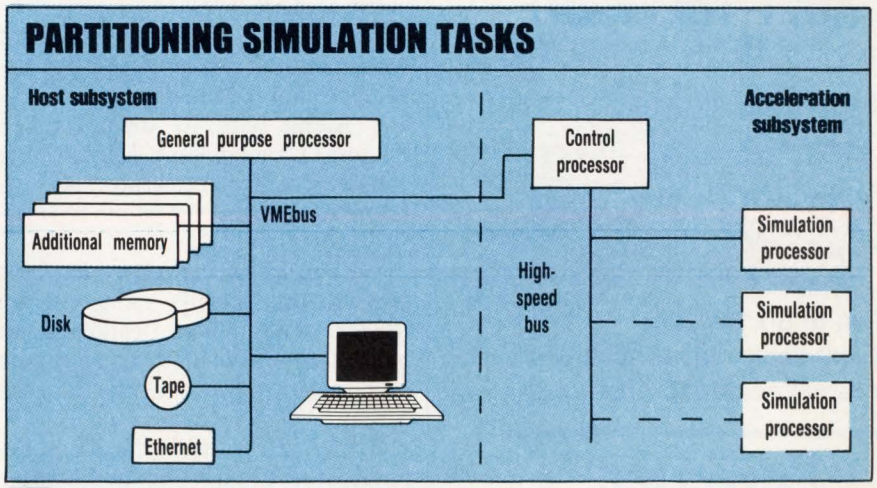
In scan design, a control circuit permits flip-flops, latches, or registers to be set to the desired state for a particular test pattern. The control circuit runs the machine for one cycle, then reads out the contents of the flip-flops downstream of the combinational logic that has just been exercised. In boundary scan design, a set of latches or flip-flops are placed around the periphery of every chip so that the inputs can be set and the outputs read. One result of this technique: The chip can be turned off and exercised to see whether the interconnections between chips are correct. The output scan elements of a chip are loaded, and the inputs are read downstream.

The Aida simulator was specially designed to build synchronous, well-clocked systems. The narrower focus yields a substantial gain in speed. A preprocessing step walks through the circuit's topology and does "levelizing," or compilation, which ranks the gates for evaluation. Gates are subsequently evaluated at level one, level two, and so on, down through multiple levels. They are evaluated by their topology rather than by tracing events.

Systems that evaluate events typically evaluate a gate only if one of the inputs changes. The Aida approach is to evaluate only the dc values of the combinational gates. Every gate is evaluated, but just once, at its stable state.

Aida's hardware component is a computer, called a levelized compiled-code simulator, that executes the linear list of gate models without branching. This approach lends itself to pipelining because future instructions can be anticipated. Most other systems use an event-driven, event-queue, or selective-trace type of algorithm, which causes inefficient pipelining. The Aida accelerator has a capacity of up to 8 million gates. A new version will add a modeling cache.

According to Aida, among the trade-offs the accelerator designer must consider, the most important is



4. PARTICULARLY ADEPT at modeling MOS circuits, the Mach 1000 from Zycad subsidiary Silicon Solutions accelerates logic simulation and performs mixed-level as well as concurrent fault simulation.

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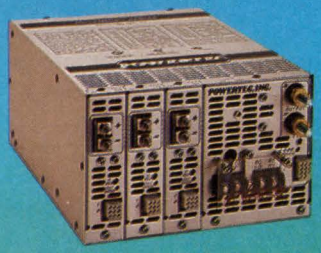
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SOME ACCELERATOR MANUFACTURERS

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Santa Clara, CA 95054
(408) 980-5200
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Daisy Systems Corp.
700 Middlefield Rd.
Mountain View, CA 94039
(415) 960-0123
CIRCLE 460

Ikos Systems Inc.
145 N. Wolfe Rd.
Sunnyvale, CA 94086
(408) 245-1900
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Silicon Solutions (Subsidiary of Zycad)
1380 Willow Rd.
Menlo Park, CA 94025
(415) 321-8574
CIRCLE 462

Zycad Corp.
3900 Northwoods Dr.
Ste. 200
St. Paul, MN 55112
(612) 490-2500
CIRCLE 463

Consider this to be a guide rather than a definitive list.

speed vs. flexibility. The most flexible computers process logic simulation, word processing, and accounting tasks. An engineer's workstation should be this type. His accelerator, on the other hand, should be fast but needn't be very flexible.

There are other trade-offs. For example, a difference between Zycad's LE and Mach 1000 lines is that the Mach 1000, from the company's Silicon Solutions subsidiary, works with an algorithm that's much better for doing MOS designs. It handles more "strength," letting the designer use many sizes of transistors and capacitors—an important consideration for switch-level design *(Fig. 4)*.

While Ikos refers to its system as a hardware simulator, Zycad calls its processors hardware accelerators. Zycad built a hardware engine to speed up existing simulation software. Ikos chose to design its own simulator to execute in the company's hardware. Ikos interfaces to standard CAE systems at the schematic-capture level.

Zycad, in fact, introduced the first commercial accelerator and has developed some of the fastest and largest. Along with its top-of-the-line System Development Engine, the company offers accelerators at lower price-performance points to satisfy different needs.

All Zycad accelerators do fault simulation. Prices range from $38,000 to $3 million. Designers can purchase software to convert the text or pictures of the net list into the machine's binary format.

ZyCad offers two ways to do behavioral-level modeling. In the Logic Evaluator and the System Development Engine (SDE), an event link allows behavioral modeling to run on the host computer and interact with the gate-level model. The Mach 1000 can run a behavioral model on an internal processor that talks to the simulation processor. Another method Zycad uses with HILO 3 is to have high-level models described in the functional HILO language and converted to gates. This approach works well if the high-level language is fairly structured and everything can be run in the accelerator. If the language is unstructured and difficult to convert into gates, it must be processed on the host.

In comparing accelerators, two figures of merit are frequently used: events/s and evaluations/s. An evaluation occurs when the input of a gate changes; an event happens when an output changes. An evaluation may or may not result in an event.

The level at which a design is modeled also affects performance. If it takes two primitives to model something on one accelerator and fifty primitives to model it on another and you measure evaluations/s, you're not measuring the same thing.

According to Aida, there are two useful measures of performance. One is the number of clock cycles of the entire design that you can simulate in a second. The other is the time it takes to examine simulation results, make a change in the design, perform preprocessing steps, measure the run time of the execution, and examine simulation results again. The total turnaround time to get a bug out—discover the bug, make the change, and verify that it's out—is the most useful measure for the user.□

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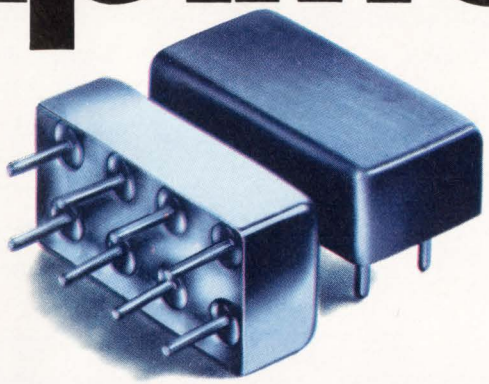

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◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
★MAN-1AD	5-500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ± 0.5dB † 1dB Gain Compression ◇Case Height 0.3 In.
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Access Time Range	15-25ns	55-70ns	65-200ns	65-200ns
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Width Expandable	x	x	x	x
Packaging	300 mil 24/20 Pin DIP	300 mil 24 Pin DIP	600 mil 28 Pin DIP	600 mil 28 Pin DIP 32 PLCC
Status Flag E, Empty. F, Full. HF Half Full. AF, Almost Full. AE, Almost Empty.	E, F HF, AF AE	E, F AF AE	E F HF	E F
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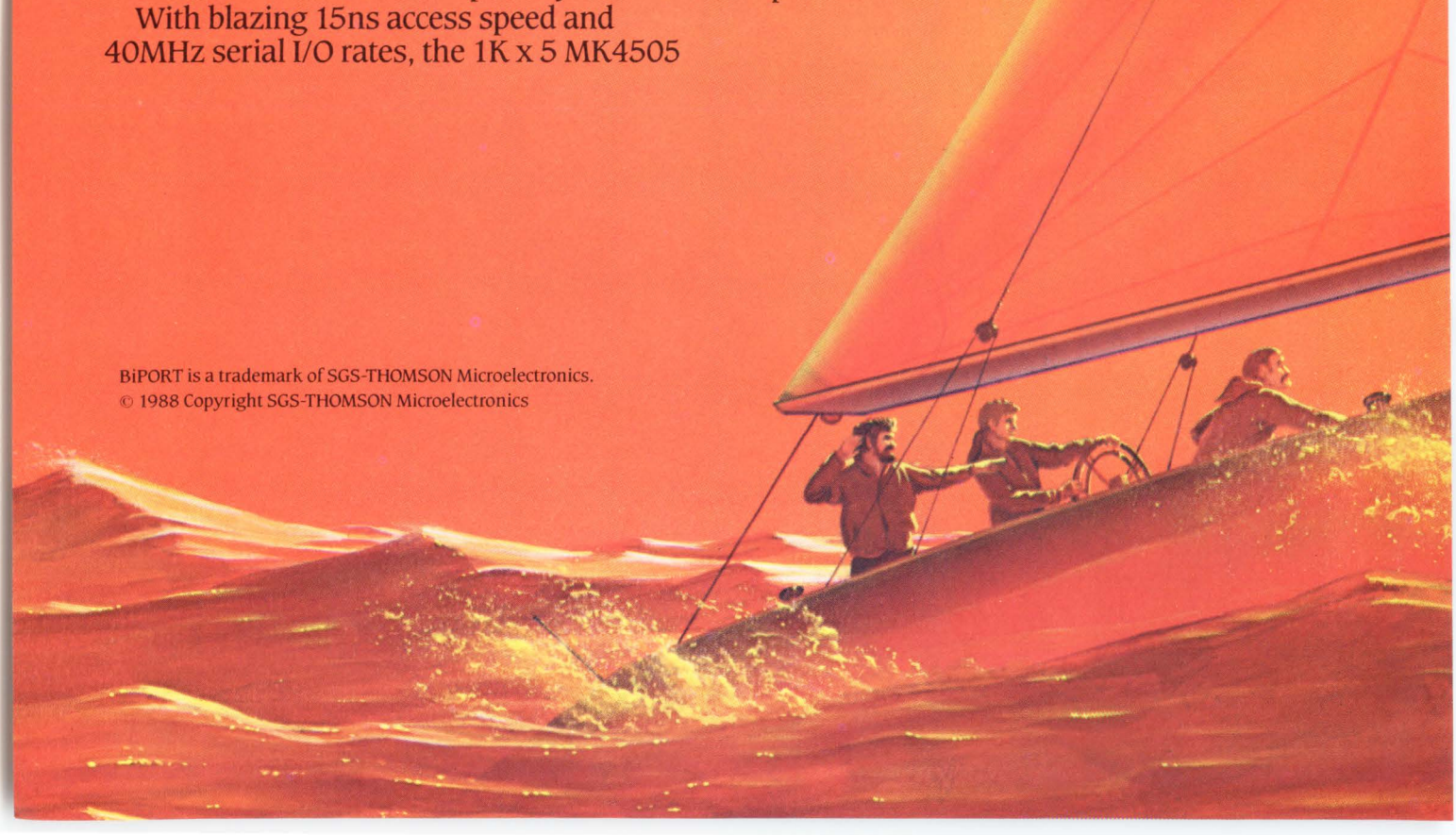

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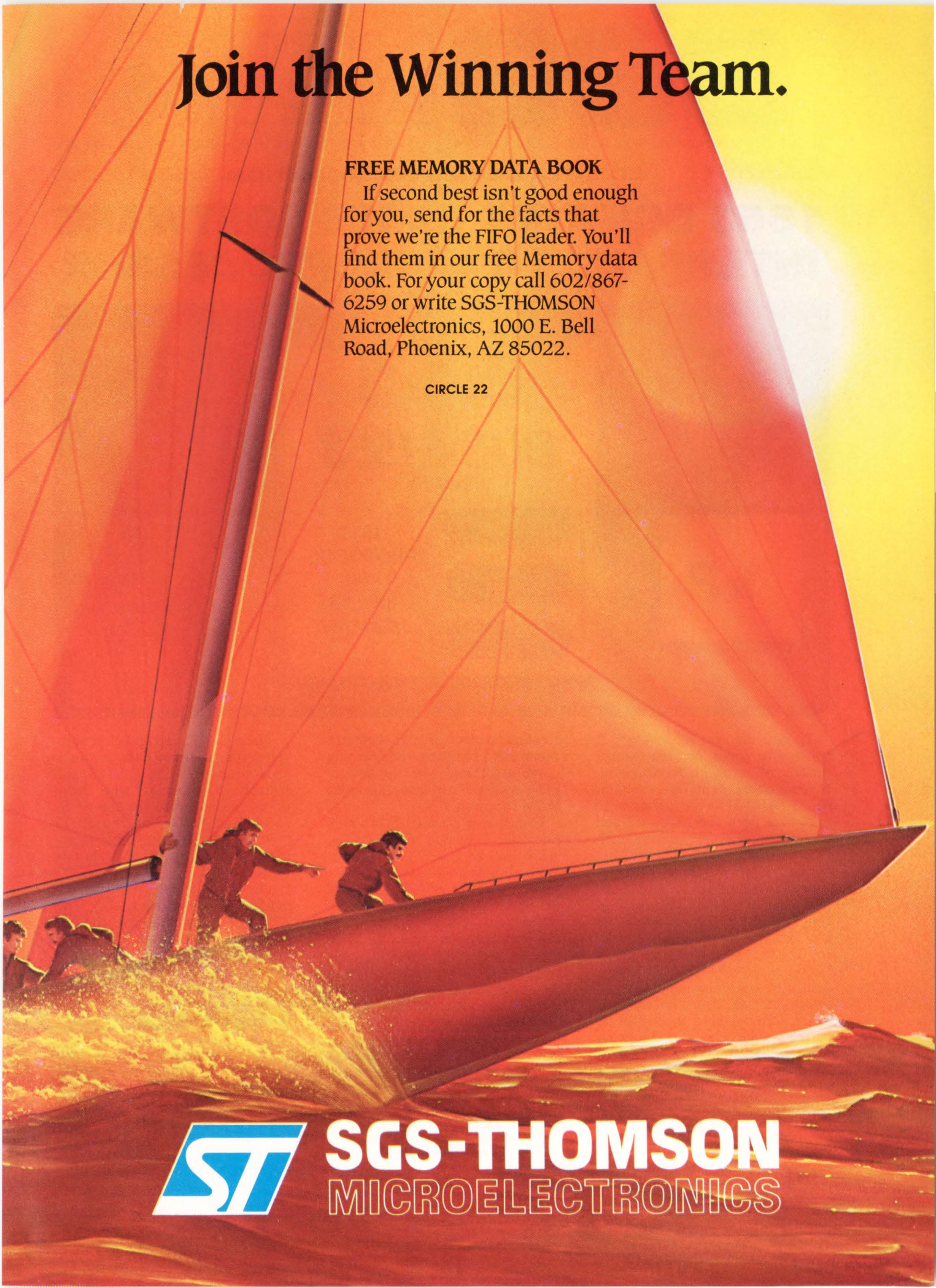
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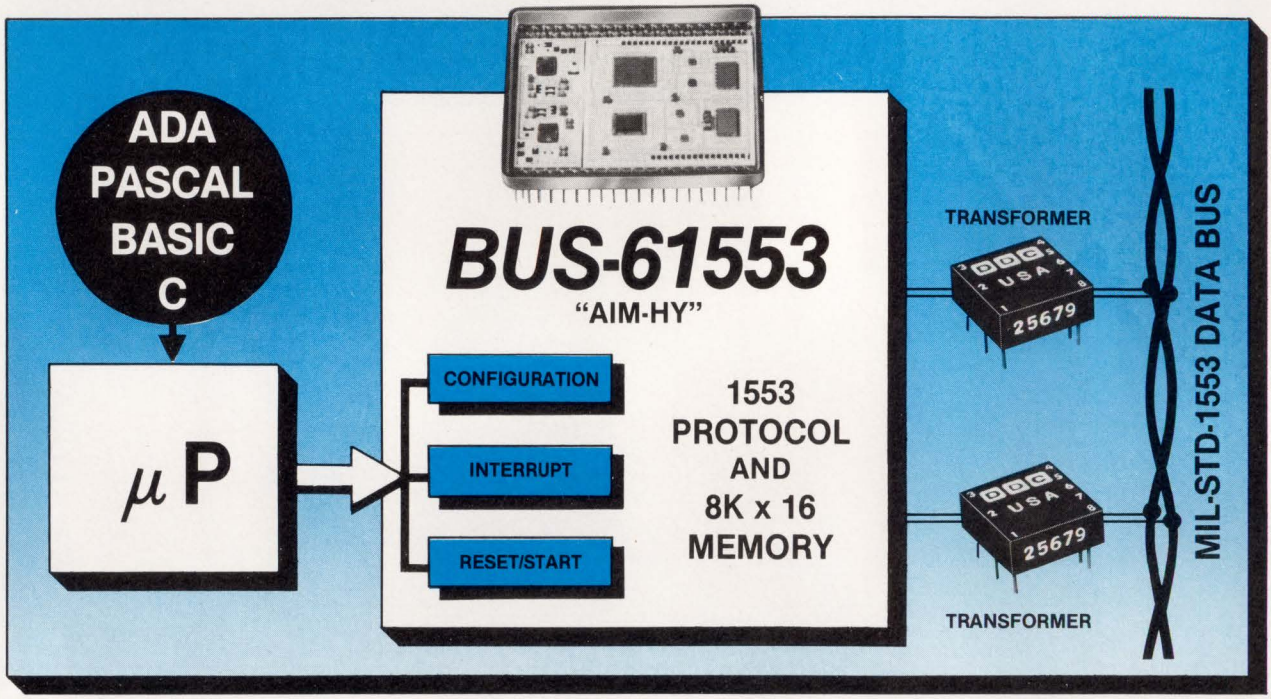
DDC NEWS

ABOUT SYNCHRO-CONVERSION • A/D & D/A CONVERSION • 1553 BUS DEVICES • POWER & CUSTOM HYBRIDS

PUBLISHED BY ILC DATA DEVICE CORPORATION SEPTEMBER 1988

1553 BC/RT/MT EASES SOFTWARE INTERFACE TO MICROPROCESSOR



Today, the cost of software is starting to equal, or even exceed, the cost of hardware development. In recognition of this fact, the BUS-61553 (AIM-HY) was designed to minimize both the hardware and software development costs associated with MIL-STD-1553.

The AIM-HY's unique architecture allows the MIL-STD-1553 bus to appear to the microprocessor as simply a block of RAM (NOT an I/O port!). This allows the user to control the interface DIRECTLY from Pascal, BASIC, ADA, "C", or any programming language—no low level I/O driver is required. The internal shared RAM can be defined to be array containing 8K words. Programming is just a matter of defining the individual values of the array. The number of registers and header words was kept to a minimum, reducing the learning curve associated with the device. (The registers can also appear as RAM locations.)

Control of the MIL-STD-1553 messages is accomplished via a stack, rather than a Linked List. With a linked list it is possible that a single, incorrect entry could cause the device to go off into "Never-Never Land", and never returning to normal program execution. The use of a stack reduces this possibility. (Even if one stack entry is incorrect, program control will return to the next entry in the stack.) The use of a stack also reduces debugging time, by eliminating the need to trace through large, scattered areas of RAM to follow program execution.

The AIM-HY is completely software compatible with the previous generation of DDC MIL-STD-1553 hybrids. Companies who have developed software for the BUS-65600/BUS-66300, or the BUS-65515 IBM PC compatible interface card can use these programs DIRECTLY!!!

The user does NOT trade performance for software flexibility. The AIM-HY fully supports the requirements for BC, RT and MT operation. Differences in the data structures used in the three modes has been minimized, making it possible to economically develop a single circuit to meet all MIL-STD-1553 applications.

For more information on the AIM-HY call toll-free (outside N.Y. state): 800-DDC-1772. □

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LOGIC SYNTHESIS: A BREAK POINT IN IC DESIGN

IN THE FUTURE, HDLS AND LOGIC SYNTHESIS WILL SIMPLIFY ASIC DESIGN

Due to increasing chip complexity, by 1992 most ASIC designers will abandon gate-level design for register transfer level (RTL) circuit descriptions. Rather than gate-level logic transformations, RTL describes the data movement from large circuit blocks, and includes both structural and behavioral descriptions. New design tools, particularly logic synthesis, will substantially aid the transition.

The present trend to hardware-description languages (HDL) resembles the 1970s migration from physical layout to the more abstract netlist description *(see the figure)*. Automatic placement and routing algorithms not only made complex ASICs possible, but also allowed designers to become more productive. RTL can reduce design turnaround times by a factor of 3 to 5.

What's more, the quality of RTL design results can increase compared with that of the present methods. Designers can explore multiple design alternatives and make higher-level trade-off decisions based on accurate area and timing information derived from the synthesized gate-level implementations.

The VHSIC hardware description language (VHDL) is likely to become a standard in the next two years, as efficient simulation becomes available. A number of other specialized synthesis languages will emerge to satisfy the needs of such specialty fields as digital signal processing or filter design.

AART J. DE GEUS
SYNOPSYS INC.

Logic synthesis is causing a breakpoint effect in IC design methodology. Within the next two years, leading ASIC designers will be effectively synthesizing 100,000 to 1,000,000 gate circuits. "Systems on a chip," touted as the impetus of ASICs, is now more possible than ever because of logic synthesis.

Tough new challenges will arise, however, from automatically synthesizing circuits with over 100,000 gates. Because most HDLs were designed for use in simulation, employing these languages in circuit synthesis will be the first challenge.

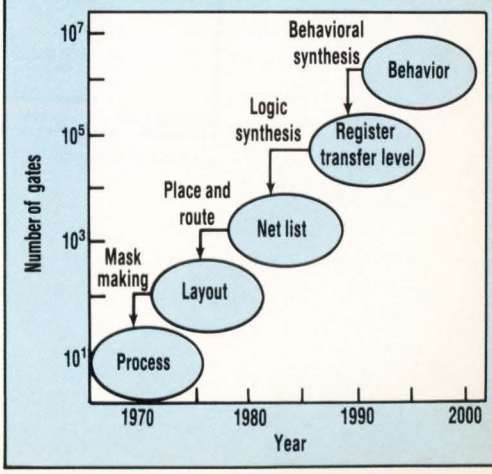
Chip testing poses another difficulty. Although in the past, designers could get by with ad-hoc test approaches, increasing design complexity prohibits this type of testing in the future. As a result, two trends will emerge: the rapid adoption of disciplined scan-based techniques and the use of built-in self-test (BIST) mechanisms, created automatically as part of the synthesis process. The testability of a design will then become part of its specification, and designers will control synthesis for testing directly from the HDL description.

The premise behind the success of ASICs is that designers are insulated from low-level technology details. Designers will build ASICs only if they can use such familiar descriptions as TTL functions and standard parts like RAMs and ROMs. Synthesis not only matches this appeal, but also frees the designer to concentrate on functionality rather than on implementation.

ASIC vendors realize that synthesis will be the differentiating component in the next generation of ASIC design. As the design process occurs at a higher level, less "traditional" electrical engineering content is involved, opening opportunities to a broader generation of designers. Based on practicality alone, RTL descriptions will be the main level of representation in the early 1990s. With synthesis, the behavioral description will become the source from which all other design representations are automatically derived. Consequently, in addition to gate libraries, ASIC vendors will ultimately provide functional subroutines that designers use in HDL descriptions.□

AART J. DE GEUS is vice president of engineering at Synopsys Inc. He holds a PhD in electrical engineering. As a CAE manager for General Electric, he led the team that developed the Socrates synthesis system at Research Triangle Park, North Carolina.

DESIGN FOCUS



	MODEL	DESCRIPTION	ANALOG INPUTS			ANALOG OUTPUTS			
			Channels	Resolution (bits)	Throughput (kHz)	Channels	Resolution (bits)	Throughput (kHz)	I/O Lines
LOW COST	DT2811-PGH	Low Cost A/D, D/A, Interrupt	16SE/8DI	12	20	2	12	50	8 In, 8 Out
	DT2811-PGL	Low Cost, Low-Level A/D, D/A; Interrupt	16SE/8DI	12	20	2	12	50	8 In, 8 Out
	DT2814	Low Cost A/D, Int.	16SE	12	25	–	–	–	–
	DT2815	Low Cost D/A	–	–	–	8	12	3.3	–
	DT2817	Low Cost DIO	–	–	–	–	–	–	32
GENERAL PURPOSE	DT2808	Low Cost, DMA	16SE	10	3.3	2	8	10	16
	DT2801	General Purpose, DMA	16SE/8DI	12	13.7	2	12	14.8	16
	DT2801-A	Higher Throughput, DMA	16SE/8DI	12	27.5	2	12	29.5	16
	DT2801/5716A	High Resolution, DMA	8DI	16	20	2	12	14.8	16
	DT2805	Low Level, DMA	8DI	12	13.7	2	12	14.8	16
	DT2805/5716A	Low Level, DMA	8DI	16	20	2	12	14.8	16
	DT2818	Simultaneous Sample & Hold, DMA	4SE, SS&H	12	27.5	2	12	29.5	16
HIGH SPEED	DT2824-PGH	High Throughput, Low Cost A/D; DMA, Ints.	16SE/8DI	12	50	–	–	–	16
	DT2824-PGL	Low Level, Low Cost, High Throughput A/D	16SE/8DI	12	50	–	–	–	16
	DT2821	High Throughput, DMA, Interrupts	16SE/8DI	12	40	2, De-glitched	12	130	16
	DT2821-F-16SE, DT2821-F-8DI	Very High Throughput, DMA, Interrupts	16SE or 8DI	12	150	2, De-glitched	12	130	16
	DT2821-G-16SE, DT2821-G-8DI	Ultra High Throughput, DMA, Interrupts	16SE or 8DI	12	250	2, De-glitched	12	130	16
	DT2823	High Throughput, High Res., DMA, Ints.	4DI	16	100	2, De-glitched	16	100	16
	DT2825	High Throughput, Low Level, DMA, Ints.	16SE/8DI	12	40	2, De-glitched	12	130	16
	DT2827	High Resolution, High Throughput, DMA, Int.	4DI	16	100	2, De-glitched	12	130	16
	DT2828	High Throughput, SS&H, DMA, Interrupts	4SE, SS&H	12	100	2, De-glitched	12	130	16
DT-*Connect*™	DT2841	High Throughput, **DT-*Connect*™** Transfer	16SE/8DI	12	40	2, De-glitched	12	130	16
	DT2841-F-16SE, DT2841-F-8DI	150kHz Throughput, **DT-*Connect*™** Transfer	16SE or 8DI	12	150	2, De-glitched	12	130	16
	DT2841-G-16SE, DT2841-G-8DI	250kHz Throughput, **DT-*Connect*™** Transfer	16SE or 8DI	12	250	2, De-glitched	12	130	16
	DT2841-L	750kHz Throughput, **DT-*Connect*™** Transfer	4DI	12	750	2, De-glitched	12	130	16
	DT2847	16-bit Resolution, **DT-*Connect*™** Transfer	4DI	16	100	2, De-glitched	12	130	16
	DT2848	High Throughput, SS&H, **DT-*Connect*™** Transfer	4SE	12	100	2, De-glitched	12	130	16
FLEXIBLE I/O	DT2806	iSBX A/D	Up to 80	12	20	Up to 24	12	5	Up to 72

Subroutine libraries and/or application–specific software packages are available with all boards.

–Fred "Atlas" Molinari, President

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L FUNCTIONS			SCREW TERMINAL PANELS		
	Counter/ Timer	Programmable Clock	Low Cost	Signal Conditioning	PRICE
	–	√	DT707	DT709-Y, DT756-Y, DT760	$ 745
	–	√	DT707	DT709-Y, DT756-Y, DT760(-T), DT707-T	$ 845
	–	√	DT757	DT709-Y, DT756-Y, DT760	$ 395
	–	–	(2)DT757	–	$ 499
	–	–	DT758-C	–	$ 199
	–	√	DT707	DT709-Y, DT756-Y, DT760	$ 495
	–	√	DT707	DT709-Y, DT756-Y, DT760	$ 995
	–	√	DT707	DT709-Y, DT756-Y, DT760	$1,095
	–	√	DT707	–	$1,970
	–	√	DT707	DT707-T	$1,095
	–	√	DT707	DT707-T	$2,070
	–	√	DT707	–	$1,695
	–	√	DT707	DT709-Y, DT756-Y, DT760	$ 995
	–	√	DT707	DT709-Y, DT756-Y, DT760	$ 995
	–	√	DT707	DT709-Y, DT756-Y, DT760	$1,345
	–	√	DT707	DT709-Y, DT756-Y, DT760 (SE)	$1,995
	–	√	DT707	DT709-Y, DT756-Y, DT760 (SE)	$2,995
	–	√	DT707	–	$2,795
	–	√	DT707	DT707-T, DT760	$1,445
	–	√	DT707	–	$2,495
	–	√	DT707	–	$1,995
	–	2	DT707	DT709-Y, DT756-Y, DT760 (SE)	$1,450
	–	2	DT707	DT709-Y, DT756-Y, DT760 (SE)	$2,095
	–	2	DT707	DT709-Y, DT756-Y, DT760 (SE)	$2,695
	–	2	DT707	–	$2,995
	–	2	DT707	–	$2,495
	–	2	DT707	–	$2,095
	(3) 16-bit, cascadable	–	DT757, DT758-E	DT709-Y, DT756-Y, DT756-D, DT760	$295 to $1,530

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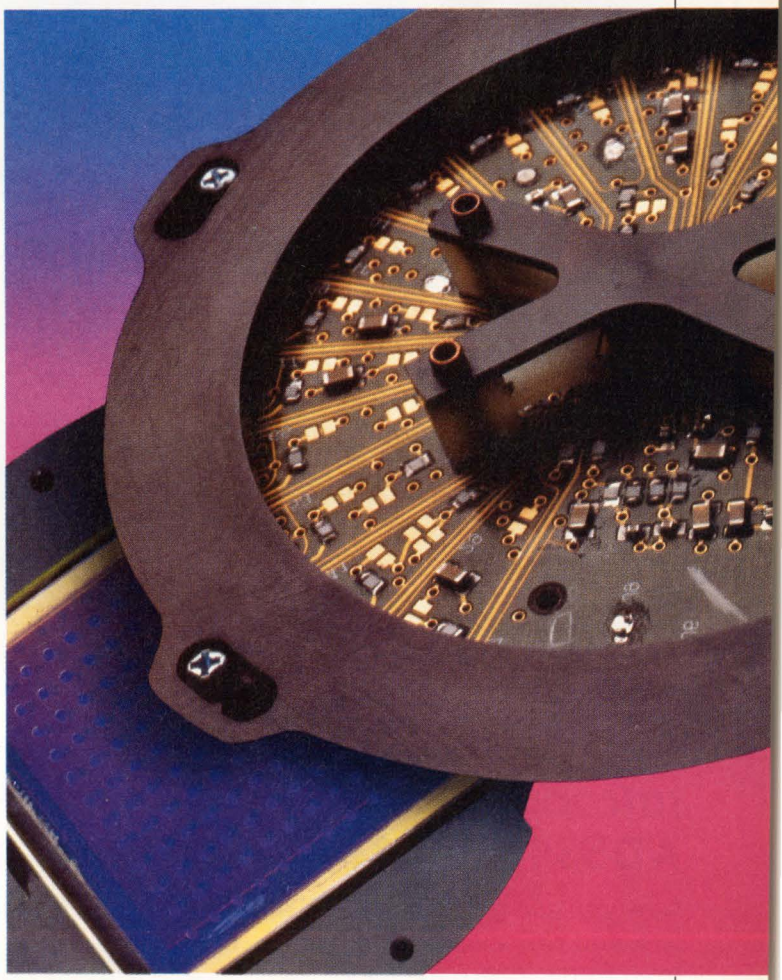
CIRCLE 26 FOR LITERATURE

CIRCLE 27 FOR DEMONSTRATION

LASER BEAMS AND A CRYSTAL'S ABILITY TO CHANGE LIGHT POLARIZATION AS VOLTAGE VARIES CARRY A DEVICE TESTER TO NEW HEIGHTS IN PERFORMANCE.

ELECTRO-OPTIC DEVICE TESTER TOPS 1-GHz

JOHN NOVELLINO



Sometimes an old technology just runs out of steam. After years of tweaking, nudging, and coaxing the tried-and-true techniques—working harder for each performance improvement—designers reach a dead end. Take conventional semiconductor test methods, for instance. Though manufacturers did a fine job of reducing such critical parameters as device pin loading and pin-to-receiver distance, the basic characteristics of hard-wired electrical testers may prevent them from going much further.

That's certainly the philosophy at Photon Dynamics, a two-year-old company whose first product supports its claim that electro-optical systems are the future of digital device testing. The System E/O One, which replaces electrical signals and copper wires with a laser-scanned optical sensor, tests devices at data rates up to 1.2 GHz, with clock rates twice that figure. The production tester for VLSI devices features a timing accuracy of ±25 ps and timing resolution of 10 ps. In comparison, the fastest conventional testers supply digital data at up to 200 MHz, with timing accuracies of about ±250 ps and resolutions to about 20 ps.

Although the concept of measuring device characteristics with a noninvasive light beam is new, the System E/O One is based on long-standing principles. Laser and optical systems have been around for some time. The breakthrough technology that made it possible for them to be used in a device tester is based on Pockel's effect, which dates back to the 19th Century. Pockel's effect—a fundamental physical interaction between light and an electrical field inside an appropriate crystal—is the basis of the systems's voltage measurement. The optical techniques offered by this phenomenon reduced pin loading to less than 1 pF and cut the distance from

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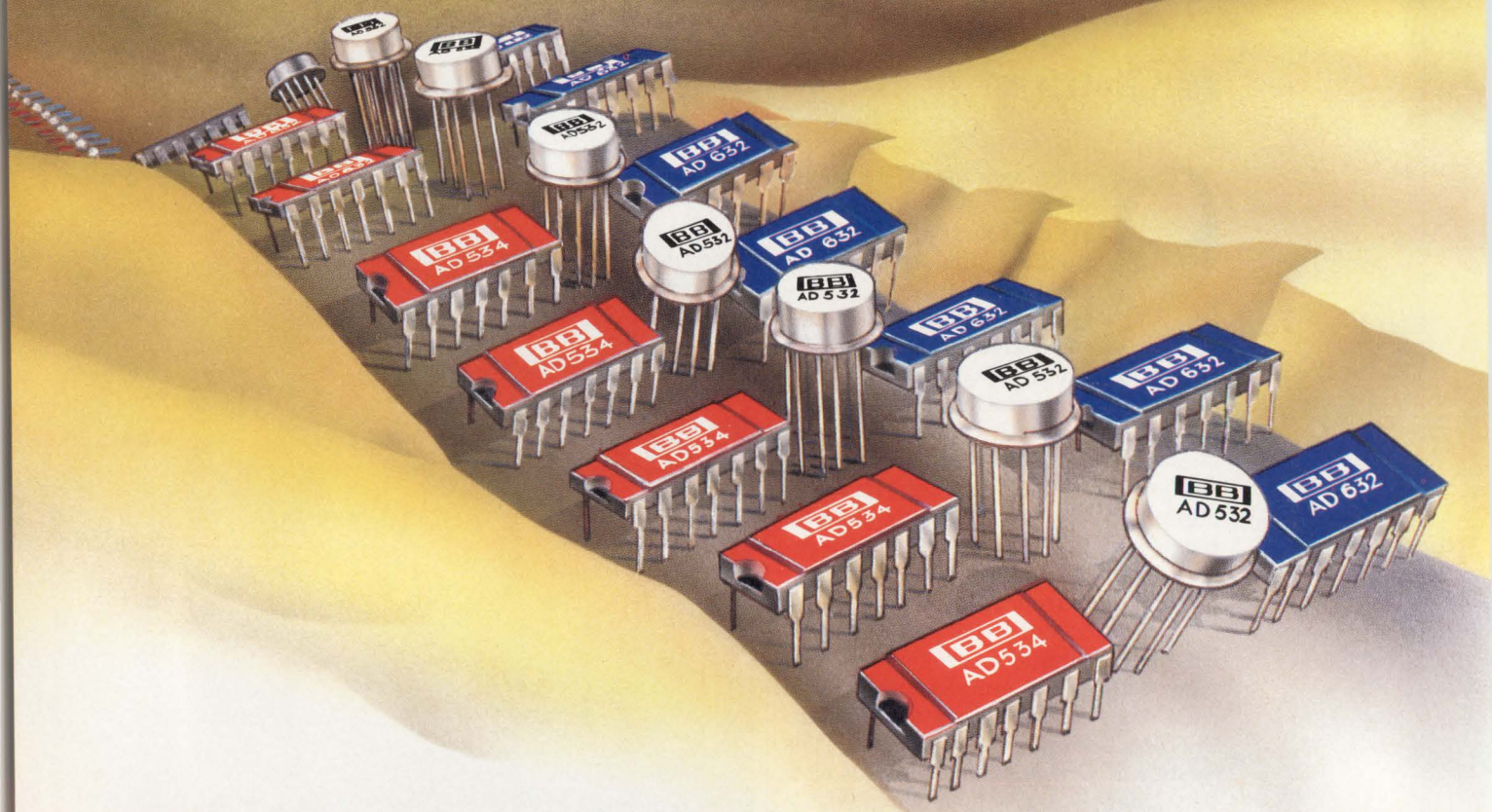

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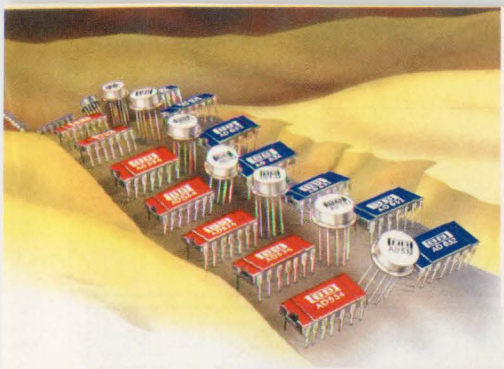

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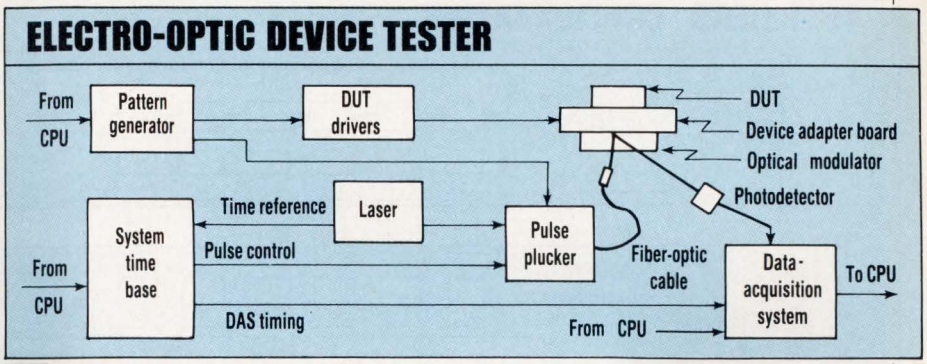
COVER: ELECTRO-OPTIC DEVICE TESTER



1. PHOTON DYNAMICS' SYSTEM E/O One uses a fast beam of very short laser light pulses to measure the performance of digital devices. A Sun Microsystems 3/160 CPU controls the tester.

PRICE AND AVAILABILITY

Prices for the System E/O One VLSI production tester range from $750,000 to $1 million, depending on the number of pins, driver power supplies, and so forth. Availability is 90 days, with first shipments expected by the end of December.

Photon Dynamics Inc., 645 River Oaks Pkwy., San Jose, CA 95134; Bob Ackerman, (408) 433-3922. **CIRCLE 514**

the device under test (DUT) to the receiver to 0.5 cm. Combining these technologies in the first commercial laser-based semiconductor test system was the work of Francois J. Henley, vice president of engineering research and development and cofounder of Photon Dynamics, of San Jose, Calif.

The resulting system uses sampling techniques to process more than 50 pins per second. Though it's currently limited to 1.2 GHz, systems based on lightwave technology have worked at hundreds of gigahertz in laboratory tests. Consequently, Photon Dynamics doesn't expect the basic techniques to soon be obsolete.

The system's extremely low capacitance prevents DUT loading, which would affect timing performance. Furthermore, this low capacitance makes possible sharper signal edges, which helps locate the signal switches between logic 1 and logic 0. As a result, slew rate is better than 3.3 V/ns, compared with about 1.5 V/ns on conventional testers.

Controlled by a Sun Microsystems computer, running under AT&T's Unix, System E/O One offers complete functional testing for both wafers and packaged circuits *(Fig. 1)*. The test language is based on C, and the system includes a C compiler and linker to help build the final test program. A vector editor creates and modifies the vector patterns sent to the DUT.

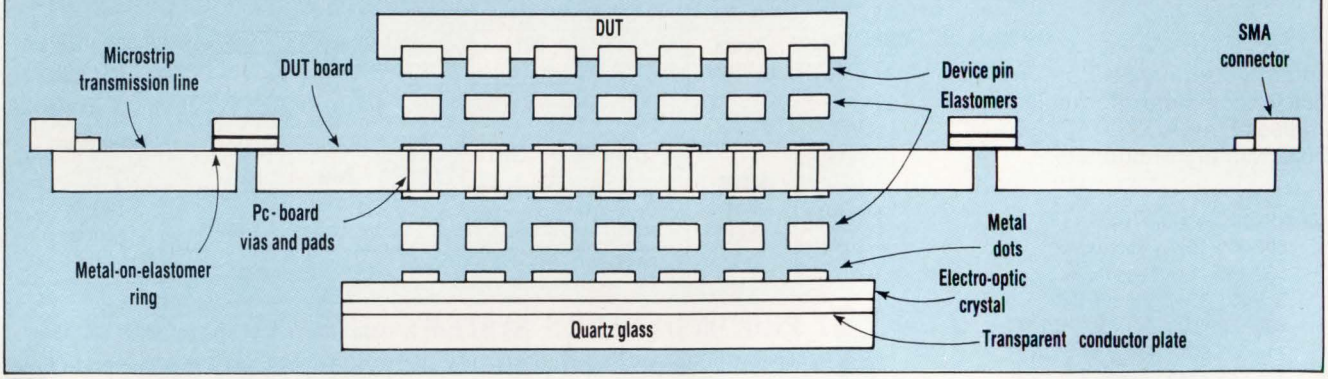
Unlike single-shot pass recording, typical of electronic measurement systems, System E/O One captures fast events with sampling. A very short light pulse, precisely synchronized with the device waveform, samples the voltage point. By accurately controlling the relative time position of the light pulse, the tester can trace the device's waveform.

Drive signals are supplied by 20 high-speed drivers (75 Mbits/s to 1.2 Gbits/s) and 20 low-speed drivers (5 to 75 Mbits/s), each backed by 32 kbits of vector-pattern storage. The system also stores 32 kbits of sampled output data. The interface between the tester and the DUT has up to 144 positions, offering users a wide selection of measurement test points *(Fig. 2)*. These points connect to the drive signals, which are checked before measurements are made to eliminate skew (timing differences) between test signals.

A Sun Microsystems 3/160 computer controls the pattern generator, eight driver power supplies, the system time base, and the data-acquisition system. The test vectors are stored in the pattern generator,

COVER: ELECTRO-OPTIC DEVICE TESTER

TEST-HEAD CONFIGURATION



2. THOUGH THE SYSTEM is initially rated at 1.2 GHz, its test head maintains a tightly controlled electrical environment. As a result, it works at up to 5 GHz.

which incorporates ECL circuitry. From there, the vectors go through gallium arsenide DUT drivers to the device adapter board.

A mode-locked Nd:YAG continuous-wave laser delivers precise time references, not only for the measurement system but also for the pattern generator and the data-acquisition system. The measurement system receives 100-ps light pulses at 1 MHz. Because the laser emits pulses, an optical pulse-selection scheme is needed to select the pulses used for sampling. The "pulse plucker" does this under control of the DAS and system timebase. Both random and sequential sampling are possible.

As a result of Pockel's effect, the voltage on each of the 144 gold dots that form the interface with the DUT changes the lightwave's polarization. In the System E/O One, the Pockel cell crystal is about 1-in. square and 1-mm thick *(Fig. 3)*. A transparent electrode is deposited on the bottom of the crystal, and the top holds the 12-by-12 dot array.

A field lens and a set of scanning mirrors aim the laser light beam at the dot selected by the test program. Because wires don't connect the DUT to the measurement system, the capacitance is between the metal dot and the ground plane. The dot is tiny, and the crystal has a high dielectric. As a result, capacitance is less than 1 pF.

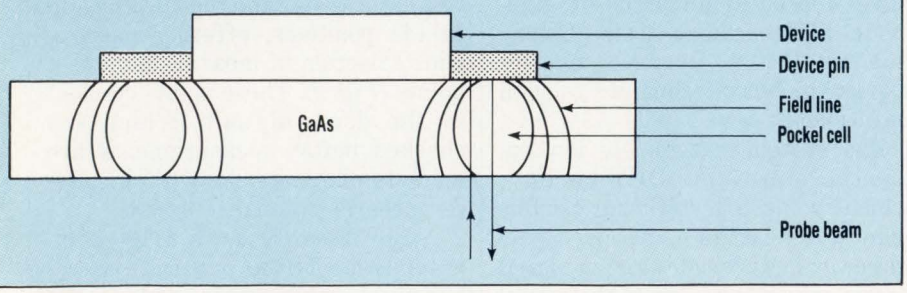
The return beam is split and analyzed with a Wollaston analyzer and two photodetectors, which measure the polarization changes differentially. After amplification and analog-to-digital conversion, the information goes to the data-acquisition system. This measurement technique is linear and can handle levels from millivolts to hundreds of volts at frequencies from dc to terahertz.

A tightly controlled electrical environment in the test head minimizes its effects on the measurement. In fact, the head is good for operation to 5 GHz. Microstrip transmission lines terminate beyond the DUT, so that loading is kept constant. A metal-on-elastomer ring forms the connection between the DUT board and the fixed test-head board. Elastomeric connectors also link the DUT board, which may have up to nine layers, to the metal dots on the electro-optic crystal.

Several important measurement tools are built into the System E/O One: a sampling oscilloscope, a logic analyzer, and a timing analyzer. All three can work as independent instruments, though they are fully integrated into the system and operate on tester-generated data.

Users can interact with the tester and DUT controls through the oscilloscope's controls. In this way, the tester can run a programmed test and then the operator can vary the test parameters with the oscilloscope's controls and avoid rewriting or recompiling the program. In addition, the system can capture the new or edited test setups and incorporate them into the program with the EasyTest program generator.□

POCKEL'S EFFECT



3. A POCKEL CELL is the optical modulator that makes the System E/O One possible. The polarization of the light beam reflected off the pin contact changes according to the voltage at that point.

HOW VALUABLE?	CIRCLE
HIGHLY	565
MODERATELY	566
SLIGHTLY	567

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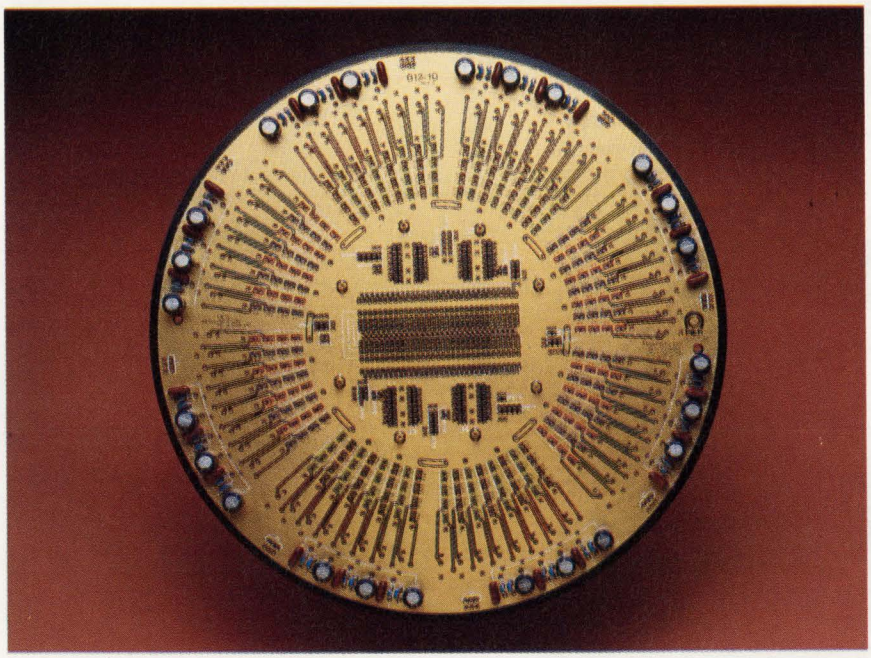


ASIC VERIFICATION SYSTEMS FIGHT TO MEASURE UP

BOB MILNE

SHRINKING IC GEOMETRIES DEMAND MORE TESTING POWER AND BETTER ANALYSIS TOOLS

ASIC verification systems have sought the same goal since their 1984 introduction—to give designers cost-effective test systems that can wring out their prototype parts confidently. But the growing complexity of application-specific ICs has made meeting that goal a tall order.

From the start, designers employed these systems to perform functional verification on their first silicon. Now, these testers are called on to perform more than mere functional verification. Some users add dc parametric measurements. Others seek also to fully characterize ASICs intended for multiple design projects. In effect, the ideal is a "do-it-all" tester for developing data sheets that can be used by future designers. What's crucial here is accurate ac parametric measurements of items such as setup and hold times or propagation delays.

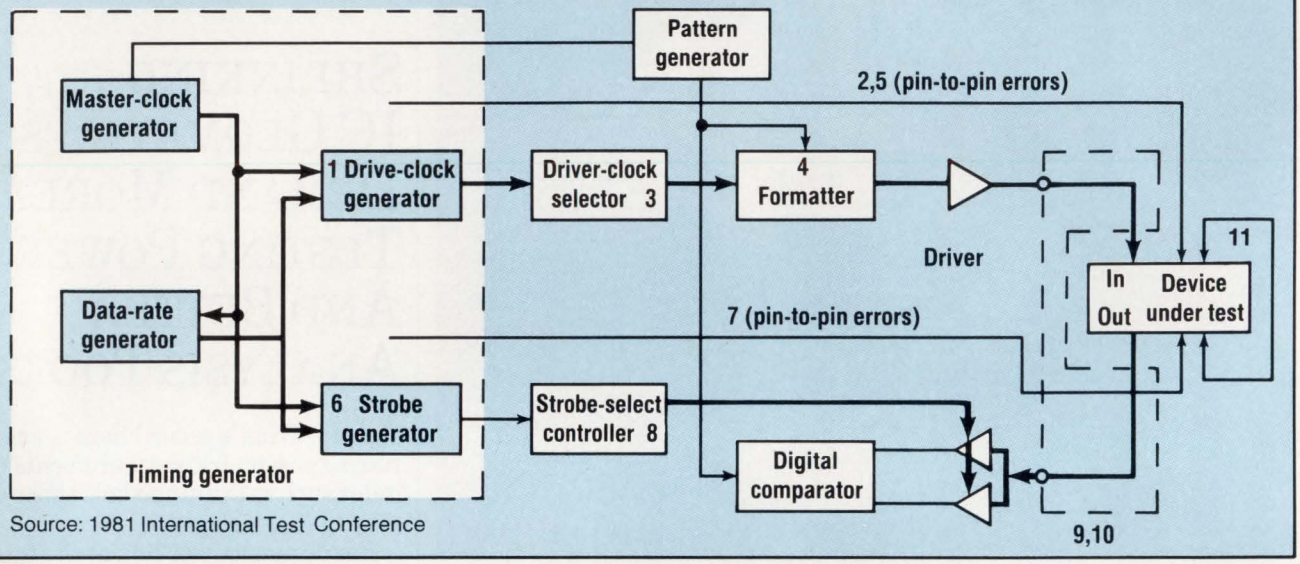
For designers working at the forefront of technology, the real obstacles are the basic testing challenges imposed by today's ASICs. Shrinking device geometries add up to more densely packed chips operating at ever higher speeds. This means that more than anything else, designers working with leading-edge ASICs need more raw testing power and better accuracy. The latest testers offer just that. Indeed, if there's insufficient testing power, the other bells and whistles a system sports become meaningless. And as performance rises, designers must know more about the conclusions they draw from reading tester data sheets. Speed is neat, but with testing, accuracy is what counts.

Furthermore, designers are getting better software tools to help them analyze and interpret test results. Links to CAE systems and user interfaces are improving, too. Also, the verification needs of engineers working with structured design methodologies, such as scan-path techniques, are now being addressed.

To meet the testing challenges, verification systems are responding to the traditional faster-wider-deeper syndrome so well known in the automatic-test-equipment community. But as pin counts and performance rise, so the does the yardstick by which cost effectiveness is

ASIC VERIFICATION SYSTEMS

ERROR SOURCES



1. MANY SOURCES OF error affect a VLSI test system's overall accuracy: 1) clock positioning linearity; 2) driver pin-to-pin skew; 3) driver clock-to-driver-clock skew; 4) format-to-format skew; 5) jitter; 6) strobe-positioning linearity; 7) comparator pin-to-pin skew; 8) strobe-to-strobe skew; 9) high-to-low comparator skew; 10) ambiguous time; 11) driver-to-comparator skew; and 12) dual thresholds.

judged. A low pin-count system can be had for under $20,000. However, some newer systems, configured for maximum pin count, can easily hit $500,000. Is that cost effective? To those working with high-pin-count devices, it's better than the alternative: a $2 million production-type VLSI test system.

To get the right perspective on verification systems, compare them with VLSI test systems intended for production. The most expensive production testers obviously have the best performance specifications money can buy, but these testers are geared for high-throughput, pass-fail testing—not prototype evaluation. Although production testers can check out ASIC prototypes (many semiconductor houses do just that), their user interfaces and software tools aren't optimized for an ASIC designer's needs.

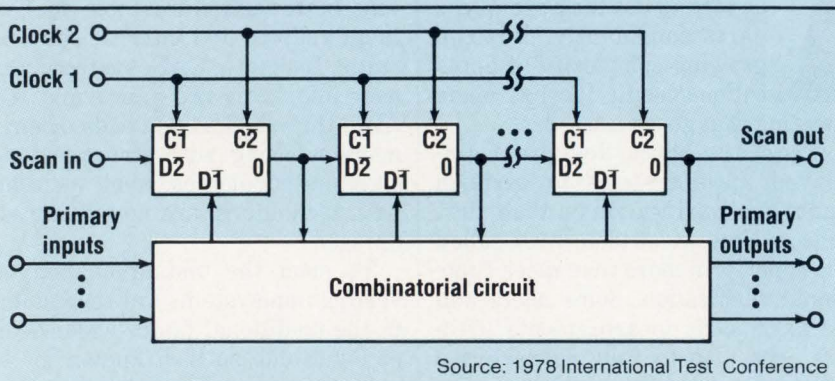
Consequently, from a designer's standpoint, ASIC verification systems are actually better for evaluating prototypes than production testers. They're more affordable; some fit on a desktop; and their toolsets are ideal for the kinds of analysis designers perform. Some even sport user interfaces patterned after the ones designers are used to on CAE systems. But how does a designer determine whether he has enough testing power for the job at hand?

Determining whether a verification system has enough measurement power is difficult. Data sheets bristle with specifications and though some are relatively straightforward and readily compared between machines, others are more obscure and may not be measured under identical conditions.

Edge-placement resolution, for example, means roughly the same thing to everyone. So does clock rate. But designers must still look closely. Are all the data formats available at the highest clock rate? Is the highest clock rate reached by multiplexing pins?

There's also accuracy: What's most important to designers is the overall worst-case system accuracy across all the tester pins. When performing ac parametric measure-

SCAN-PATH DESIGN



2. TO MAXIMIZE "controllability" and "observability" of a complex circuit, the scan-path design technique uses sequential elements that can be configured into shift registers for testing. Test patterns are scanned in and response data is scanned out.

ASIC VERIFICATION SYSTEMS

ments, for example, the worse the accuracy, the bigger the guard band must be around the measurements. This shrinks the window of acceptable measurement results.

It's a safe bet that a data sheet will have a specification for skew across all pins. But is the skew specified for any driver pin to any other driver pin? Or is the tougher specification given: any driver pin to any comparator pin? What's more, skew isn't worst-case timing error—it's only a component of it.

Accounting For Errors

A superb analysis of the error sources in a VLSI test system was presented at the 1981 International Test Conference by the Takeda Riken Industry Co. (now the Advantest Corp.), of Saitama, Japan, and the Musashino Communication Lab., NT&T, of Tokyo. In analyzing the functional blocks that make up a typical VLSI test system (pattern generator, timing generator, clock selector, formatter, driver, strobe selector, and comparator), no less than 12 sources of timing errors were found *(Fig. 1)*.

Boldface lines indicate the paths along which timing errors may be determined, and the locations of error sources are numbered 1–12. In this study, actual analysis revealed that timing errors in test results could reach ± 7 ns or more.

As if keeping track of the effects of a dozen error sources isn't tough enough, the real complexity comes in maintaining acceptable timing accuracy across all of a tester's pins. Many verification systems state overall timing-accuracy specifications. What's unknown, though, is how many error sources were taken into account.

Also, a system's accuracy, whatever level, must be maintained. Consequently, it's important to look into a tester's calibration process. Is it automated to some degree? How hard is it to perform the calibration? How long does it take? Is other equipment needed?

Noting these considerations, a look at the most recent verification systems reveals significant advances over earlier systems with test rates limited to about 20 MHz. Late last year, for example, Integrated Measurement Systems introduced the XL 100 verification system, which has 100-MHz clock and data rates, along with 224 bidirectional

ADVANCING THE STATE OF THE ART

Why do ASIC designers feel as if the walls are closing in on them? On one hand, they must thoroughly evaluate their first silicon before releasing the design to production. On the other hand, they're continually pressured to shorten design times.

The goal of Hewlett-Packard's HP 82000 IC evaluation system is to take some of that heat off the designer. For starters, its performance specifications set a new standard for verification systems. Moreover, the system has automatic setup tools that reduce the time it takes to prepare tests.

The system sports a 200-MHz vector rate, and up to 384 channels with 64 kvectors behind each pin. Edge-placement accuracy is ±250 ps, with a resolution of 50 ps. System skew is a low ±250 ps.

The unit's tester-per-pin architecture results in bidirectional-timing and level capabilities on each pin without sharing tester resources. This also avoids the need for pin wiring, which is time-consuming and error-prone.

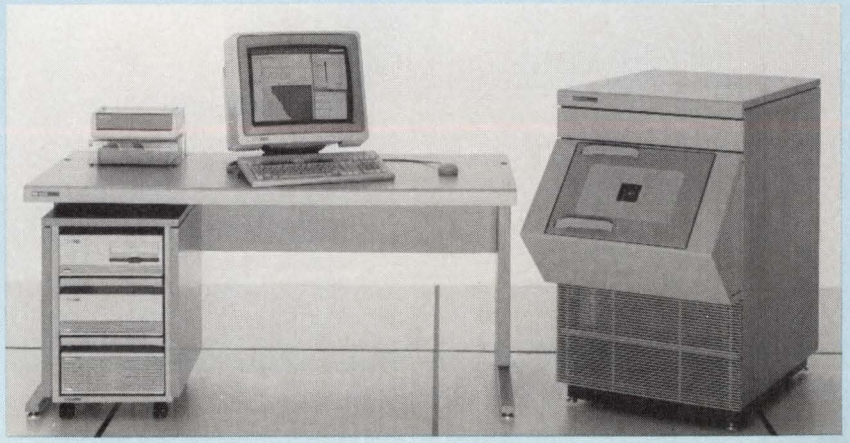
Functional tests are automatically generated with data from a CAE workstation. Unlike other test systems, which only translate test vectors, the HP system's automatic process also handles timing waveforms and pin assignments. The result: The HP 82000 can be set up to check a new design in minutes or hours, as opposed to days or weeks.

Such ac and dc parameters as propagation delay and leakage current can be measured with ready-to-use test routines. After completing the testing, users can display the results as 3D plots, high-resolution timing diagrams, state lists, and error maps.

An HP 9000 technical workstation drives the tester, and the system software operates under the HP-UX multitasking operating system, HP's version of AT & T's Unix. Custom test routines can be written in C or HP Basic.

The HP 82000 can be configured in a benchtop cabinet that accommodates up to 80 I/O channels, or a system rack that holds 384 I/O channels. Because only the mechanical housing must be changed, upgrading is simple.

A typical system containing 64 I/O channels, including the computer hardware and all operating and measurement software, is $193,000. Delivery is scheduled for the first quarter of next year.



ASIC VERIFICATION SYSTEMS

I/O channels (ELECTRONIC DESIGN, Nov. 27, 1987, p. 49).

These channels can split into separate stimulus and data-acquisition functions to yield a 448-pin system. What's more, the unit has an edge-placement and sampling resolution of 100 ps.

This year, Hilevel Technology brought out its latest verification system, the Topaz V (ELECTRONIC DESIGN, July 28, p. 155). This system, which expands to 544 I/O channels, has several operating modes depending on the test rate required. In the direct mode, which has a maximum test rate of 55 MHz, all of the system's six data formats are available.

For higher speed testing, the Topaz V has a shared mode, which yields a 110-MHz test rate with two data formats, NRZ and DNRZ. Besides that, stimulus pins can be designated as high-speed clocks that operate up to 220 MHz. Resolution for this system is 100 ps.

Per-Pin Architectures

Both testers are based on what the verification-system industry calls a "per-pin" architecture. Pioneered by Cadic in its STM 5100 and 5200 verification systems, this architecture shouldn't be confused with what the ATE industry regards as a "tester-per-pin" architecture.

In a true tester-per-pin architecture, all tester resources, including the timing generator, are duplicated for each tester pin. But this approach is quite costly. With the per-pin architecture, a verification system has a fixed number of resources—such as timing generators, driver rails, and threshold rails—that can be distributed to any pin. Cost is kept down while retaining independent control of timing, formatting, and masking on each pin.

This per-pin approach also leads to "wireless fixturing." Instead of wiring a device-under-test board to connect the DUT to the proper tester channels, pins can be assigned with software. To complete the fixturing, the user names the pins and assigns them the proper tester resources.

More Power

Two new products continue the quest for more tester power. The XL2 from Integrated Measurement Systems seeks to handle high-pin-count devices without making performance tradeoffs *(see p. 72, this issue)*.

Supporting 896 individual pattern-generation and acquisition channels, the XL2 can also be configured with 448 bidirectional I/O channels. It supports 100-MHz clock rates and 80-MHz data rates while retaining all of its nine data formats. Even at 80 MHz, the system drives into, and samples the output from, a bidirectional bus all in the same cycle.

The other introduction earns bragging rights to the highest performance specifications achieved in a verification system using conventional measurement techniques. Hewlett Packard's HP 82000 IC evaluation system *(see "Advancing the state of the art," p. 65)*. Unlike HP's previous 81810S system, which was built around rack-and-stack instrumentation, the HP 82000 was built from the ground up as an integrated system and it's based on a true tester-per-pin architecture for ac measurements.

System specifications rival those found on expensive production testers. The highest data rate, for example, is 200 MHz. Edge-placement resolution is specified at 50 ps with an accuracy of ±250 ps. The system skew also checks in at a low ±250 ps.

One test system, the E/O One from Photon Dynamics, can also verify ASICs—but it's not cut from the same mold as the other units. Its mission is to test those ICs too fast for conventional measurement methods. Based on an electro-optic measurement technique, the E/O One handles low pin-count devices operating as fast as 1-GHz *(see p. 55, this issue)*.

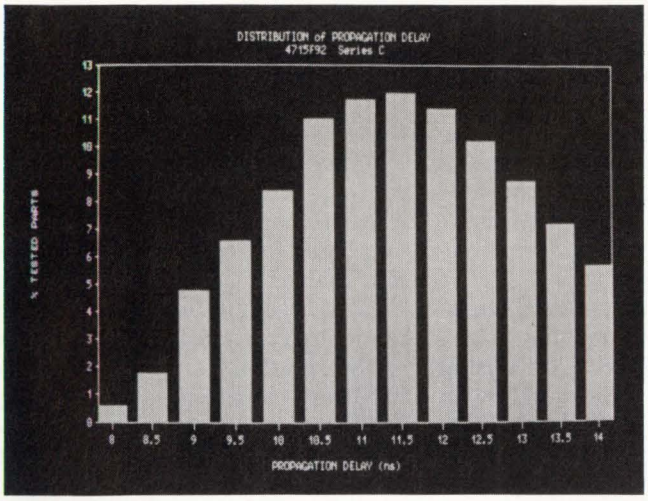
Because it's unlike any other currently available, one last system deserves mention: The ScanMaster DV-6005 from Gillytron is aimed specifically at ASICs based on scan design techniques. The system was introduced in June at the Design Automation Conference.

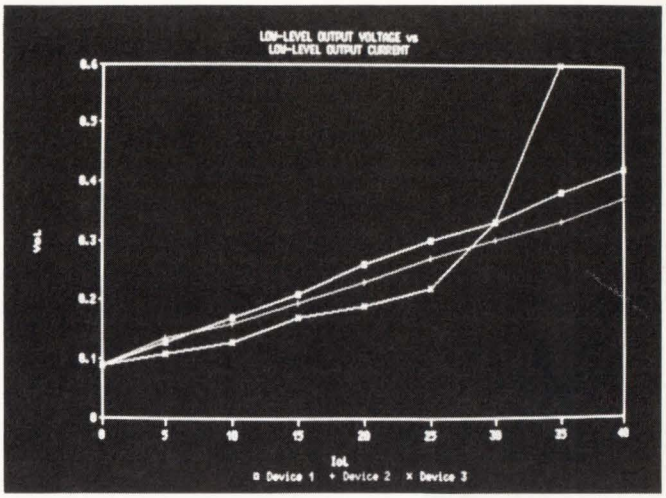
Although scan techniques have varied implementations—such as LSSD (level-sensitive scan design), scan path, and scan set—each shares a common approach to designing testable circuits. The basic idea is that for testing purposes, a circuit's sequential elements are reconfigured as a shift register.

This opens up access to the remaining portions of the circuit that are blocks of combinatorial logic. The complex problem of testing sequential logic is reduced to the easier task of testing shift registers and

3. WITH HEWLETT-PACKARD'S HP82000 verification system, designers can work with multiple windows. Going clockwise from the upper left, the display indicates vector setup, test control, report, and timing diagram functions.

ASIC VERIFICATION SYSTEMS





4. WITH INTEGRATED Measurement Systems' characterization and timing analysis (CTA) software, designers work with test results in a Lotus 1-2-3 environment. After analysis, information is graphically displayed. Among the graphs that can be displayed are those that depict propagation delay distribution (left) and the results of a failure analysis (right).

combinational logic.

Consider the scan-path approach *(Fig. 2)*. A test vector is applied to the primary inputs, then an input vector is scanned into the internal memory elements forming the shift register by Clock 2. At this point, the test results are checked on the primary outputs and one cycle of Clock 1 occurs. Next, test results from the internal memory elements are scanned out using Clock 2. Such scan techniques as this have proven successful in achieving fault coverage greater than 99%.

AC Performance Tests

The DV-6005 also handles dc parametric and ac performance tests. For ac performance, the conventional testing approach puts the burden on the verification system to stimulate the ASIC and acquire response data at the device's operating speed. As noted, this pushes verification systems to 100-MHz data rates and subnanosecond timing resolution. Gillytron's approach, though, doesn't rely on measuring edge rates and propagation delays. Instead, gate speeds are measured indirectly with the scan paths built into the chip.

A test signal introduced onto the scan circuits is allowed to couple back on itself in a repetitive fashion, or as a ring oscillator. Clocks and test inputs to the chip are set at dc levels. As a result, the scan string oscillates at a natural frequency that depends on the length of the scan circuit. Next, the period of this oscillation is measured. By considering the number of scannable latches in each scan path, it's possible to calculate the average of the gate delays in the scan loop or the overall ac performance.

The heart of the DV-6005 is a scan module that includes a scan generator with an interface for up to 25 pins—23 clock/control lines along with scan-in and scan-out data lines. Also housed in the scan module is the frequency counter used for the ring oscillator measurements. It covers a frequency range of 2 kHz to 100 MHz with 0.1% accuracy.

Each scan module comes equipped with 4 Mbytes of pattern memory and also includes a programmable device power supply and a voltage/current reference card for dc parametric measurements. By adding function modules in increments of 128 pins, the system can expanded to 1792 pins. Each scan module can be equipped with up to four scan generators and memory is expandable to 256 Mbytes.

Coping With Scan Designs

Conventional verification systems can also handle some scan testing, though none offer the ring-oscillator test. In some cases scan requirements are handled on a case-by-case basis. With Hilevel's Topaz V, the data sheet states that scan testing is an integral part of the system. Any pin or pins can be designated as scan pins during any part of a test.

Vector memory is also getting its share of attention. As devices get more complex, more test patterns are required to thoroughly exercise them. Early verification systems got by with 4, 8, or 16 kvectors behind each tester pin. Many of today's systems can expand to 64 kvectors.

Hilevel Technology takes its own approach to the memory problem: virtual vector memory. In the Topaz V, the memory is a 16-Mbyte RAM array that's connected to the pin electronics by a very fast interface. This results in a virtual vector depth of 28 million vectors divided by the number of pins. An optional 64-Mbyte array yields 112 million vectors/no. pins. For example, a device with 200 signal pins could have up to 560 kvectors active.

Testing throughput is also boosted substantially. With the conventional approach to vector memory, a verification system might require several minutes to run a 560-kvector set. With the Topaz V, it takes less than 5 seconds.

Of course, it's easy to get wrapped up in the leading-edge verification systems and forget that most engineers designing with ASICs are not working with the fastest, highest-pin-count devices. For these users, a 20-MHz verification system may be all that's needed.

The Cadic STM 5200, for instance,

ASIC VERIFICATION SYSTEMS

is a relatively small desktop unit with a fully integrated test head. Data rates can reach 25 MHz, and the system can expand to 352 bidirectional I/O pins. With a double return format, the system generates 50-MHz clock signals. Recently, Cadic upgraded the system with an executive command language (XCL) for its parametric measuring unit and a voltage-level sensitivity measurement (VLSM) package.

XCL is a high-level language that includes straightforward system commands for user constructed batch-mode testing, peripheral-interface control, and flexible test sequencing. The language also gives users control of the system's communication interfaces, including RS-232, IEEE-488, and Cadic's GIA (general-purpose interface adapter).

The VLSM package automatically measures threshold, noise-margin voltages, and other performance-related voltage levels with respect to a DUT. These tests may be performed while varying the ASIC's power-supply voltage, with the results displayed as a Schmoo plot.

Tektronix addresses ASIC prototype verification by building a system around its DAS 9200 Digital Analysis System. The verification system is created by complementing the 9200 pattern-generation and logic-analysis functions with a test fixture and the DAS 92DV software. The software package holds the key to optimizing the system for prototype verification. Test vectors from a CAE workstation can be downloaded to the system, which has various translators for popular logic simulators.

After completing the translation process, the software's resource-allocation menu maps the simulation database to the DAS 9200's stimulation and data-acquisition channels. This is accomplished automatically or manually. Then, a sampler matches the simulator output data to the hardware capabilities. By sampling the data at the test rate, checks are made for patterns that produce set-up and hold violations in the tester hardware. The user is notified if any violations are found, and the expected response data is modified to a

ASIC PROTOTYPE VERIFICATION TESTERS

Manufacturer	Model	Maximum I/O pins	Test rate (MHz)	Vector depth (kvectors)	Edge-placement resolution	Skew	Price range ($)
Asix Systems Corp. 47338 Fremont Blvd. Fremont, CA 94538 (415) 656-8664 **CIRCLE 451**	Asix-1	256	25/50	16	100 ps	±1.5 ns	80,000-300,000
Cadic Inc. 1725 S.W. 167th Pl. Beaverton, OR 97006 (503) 645-2222 **CIRCLE 452**	STM5100 STM5200	256 352	10 25	64 64	1 ns 1 ns	±2 ns ±2 ns	17,000-99,000 42,000-199,000
Gillytron Inc. 2150 Bering Dr. San Jose, CA 95131 (408) 435-3043 **CIRCLE 453**	DV-6005 (for scan designs)	1792 (ring frequency 2 kHz-100 MHz; pattern memory 256 Mbytes)					125,000-1,700,000
Hewlett-Packard Co. 1820 Embarcadero Rd. Palo Alto, CA 94303 contact local sales office **CIRCLE 454**	HP82000	384	100/200	64	50 ps	±250 ps	65,000-1,000,000
Hilevel Technology Inc. 31 Technology Dr. Irvine, CA 92718 (714) 727-2100 **CIRCLE 455**	Topaz FX Topaz 50 Topaz II Topaz V	224 256 256 544	30 50 50 55/110	16 64 64 *	500 ps 500 ps 100 ps 100 ps	±1 ns ±1 ns ±1 ns ±500 ps	20,000-85,000 30,000-200,000 40,000-250,000 70,000-450,000
Integrated Measurement Systems Inc. 9525 S.W. Gemini Dr. Beaverton, OR 97005 (503) 626-7117 **CIRCLE 456**	Logic Master ST Logic Master XL 60 Logic Master XL HS Logic Master XL 100 Logic Master XL2	112 224 256 224 448	20 60 20 100 80	16 64 64 64 64	1 ns 100 ps 100 ps 100 ps 100 ps	±2.5 ns ±1 ns ±1.5 ns ±1 ns ±1 ns	17,000-76,000 55,000-255,000 36,000-360,000 75,000-400,000 470,000-800,000
Photon Dynamics Inc. 645 River Oaks Pkwy. San Jose, CA 95134 (408) 433-3922 **CIRCLE 457**	E/O One (for fast, low-pin-count devices)	**	1.2 GHz	32	10 ps	< 10 ps	750,000-1,000,000
Tektronix Inc. P.O. Box 12132 Beaverton, OR 97212 In Ore. (503) 231-1220 **CIRCLE 458**	DAS9260 DAS9262 DAS9264	64 96 128	50 50 50	8 8 8	1 ns 1 ns 1 ns	±1.5 ns ±1.5 ns ±1.5 ns	67,110 105,350 134,000

* 112 Mvectors/number of pins
**40 input, 144 output

ASIC VERIFICATION SYSTEMS

don't-care condition. Once alerted, the designer reduces the test rate or modifies the test patterns to eliminate the violations.

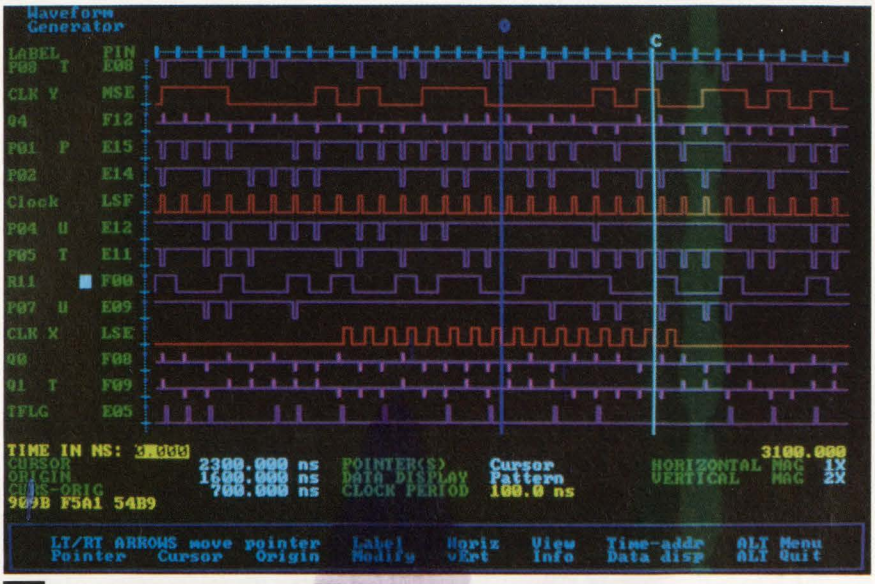
When the proper data acquisition modules are installed, they can run asynchronously with the functional test. This arrangement yields timing analysis at speeds of 200 MHz or a blazing 2 GHz.

Another verification system aimed at mainstream designers is the Asix-1 from Asix Systems Corp. Accommodating up to 256 I/O pins, this system has data rates up to 25 MHz, or 50 MHz with multiplexing. Moreover, 100-MHz clocks are supported. Asix focuses on the link between the CAE and test worlds. The problem they address is that ASICs force designers to wear a test-engineer's hat, too—an uncomfortable situation. Verification systems typically have some form of vector translator for accepting simulation vectors. But there's more to building a test program than just applying test vectors to a device.

For example, a test sequence must be developed. At the start, up to four different power supplies may have to be brought up in a timed sequence. There may be a check for opens and shorts and, following that, functional test vectors would be applied, dc parametrics might be run, and so forth. With the Asix system, designers can program these operations with a few keystrokes.

At this year's Design Automation Conference, Asix demonstrated an automatic test program generator called ASIXtest linked to LSI Logic design tools. Designers using LSI Logic's software tools to develop ASICs can now recreate simulation input files and employ the resulting files to produce a test program automatically.

A shortcoming of most CAE links is that they are generally one-way paths—from the CAE system to the verification system. But that's changing. Daisy Systems Corp., for example, worked with Integrated Measurement Systems to develop a two-way link between their respective systems. As a result, the actual test vectors run on an IMS system can be transferred back to a Daisy



5. LOOKING JUST LIKE A logic-analyzer presentation, a display from Hilevel Technology's Topaz V system makes it possible for designers to edit test vectors graphically. In some situations, this is a welcome alternative to looking at test vectors displayed as a list of ones and zeros. This type of display also makes interpreting response data easier because test results can be displayed with failures highlighted. The vector display is, in fact, as easy to interpret as a logic analyzer.

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CIRCLE 31

ASIC VERIFICATION SYSTEMS

workstation and used to, say, run another fault simulation to gauge their effectiveness.

There's good news for user interfaces: Verification system software is adopting much of the look and feel designers are used to on CAE systems. For instance, take the HP82000 with windows, color, and graphical timing displays just like a workstation's *(Fig. 3)*.

Besides making a tester easier to set up, a good user interface is essential for designers analyzing test results. With the right set of software tools, a wealth of information can be derived from test data.

An interesting approach to harvesting tester data is the CTA characterization and timing analysis software from Integrated Measurement Systems. Based on Lotus 1-2-3, the package helps designers in several key areas: Any measurement that can be performed with an IMS verification system can be automated. With preprogrammed routines, designers fill out a menu, push "start," and the system automatically measures such parameters as setup time, hold time, and propagation delay.

Once test data is acquired, the results can be collected and compiled in a spreadsheet environment. Data, for example, can be organized and statistically analyzed. If required, more tests can be performed on the device directly from the spreadsheet. To make test data easier to interpret, results can be displayed to indicate, say, propagation-delay distribution or failure-analysis curves *(Fig. 4)*.

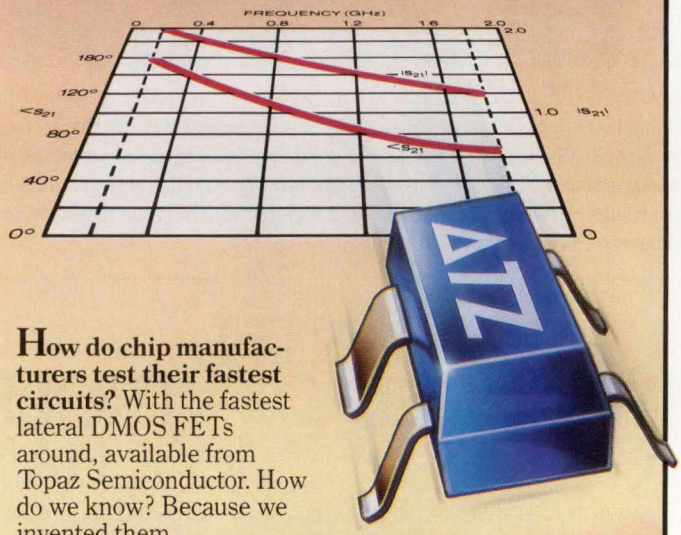
GRAPHIC EDITING

Graphic tools also help designers in editing test vectors. With Hilevel's Topaz V, for example, users can display and edit a vector set in a timing diagram format like it would appear on a logic analyzer *(Fig. 5)*. Test results can also be displayed in this manner with the failures highlighted.

As demanding as ASIC testing is now, it's going to get even tougher as more devices mix analog and digital circuitry with asynchronous clock rates on the same chip creating verification problems. These systems must resolve even more complicated dc and ac parametric data. For production testing of mixed-signal devices, it takes costly testers with huge equipment bays to do the job. Perhaps verification-system designers will come up with an affordable approach to this problem as they have for purely digital ASICs.□

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

Full Speed Ahead



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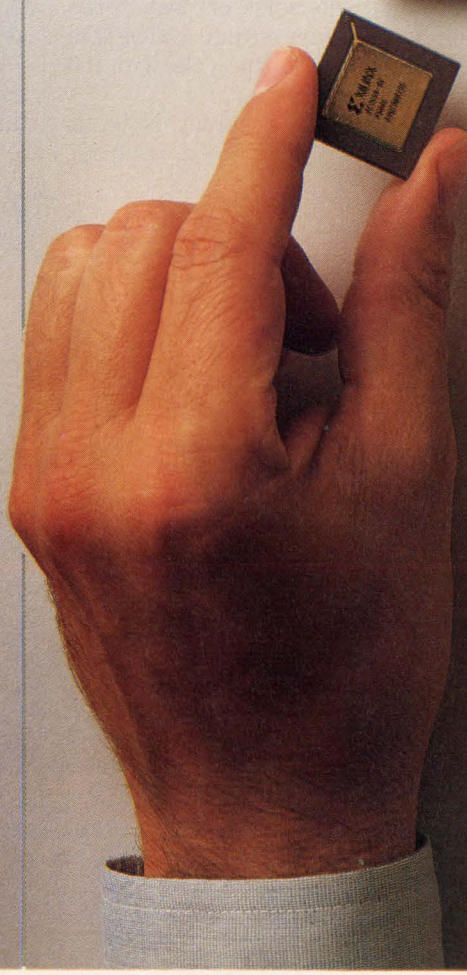
CIRCLE 32

XILINX PROGRAMMABLE GATE ARRAYS from HAMILTON/AVNET

PERFECT DESIGNS ALL THE WAY DOWN THE LINE



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CIRCLE 33

ASIC VERIFICATION SYSTEM BOOSTS PIN COUNT WHILE MAINTAINING PERFORMANCE

BOB MILNE

It would be bad enough if makers of ASIC verification systems only worried about making high-speed systems. But they must also satisfy the needs of designers working with high pin-count devices. "Device pin counts are more limited by packaging technology than by silicon technology," notes Barry Baril, vice president of engineering, IMS, Beaverton, Ore. "But the lure of capturing a complex system in silicon will drive the development of advanced packaging technologies, making 400-plus pin devices economically feasible. Many of our customers already push these bounds."

With its latest Logic Master system, the XL2, Integrated Measurement Systems Inc. anticipates such a future. Beefed up with 896 individual pattern-generation and data-acquisition channels, or up to 448 bidirectional I/O channels, the XL2 is ready to take on devices with more than 600 pins. What's more, the system doesn't sacrifice performance. It features 100-MHz clock rates and 80-MHz data rates, extensive data formatting, and lots of memory behind each pin.

TIMING IS IMPORTANT

Maintaining full performance across that many pins is important. As entire systems migrate onto one ASIC device, a verification system's timing resources must handle multiple input buses, control lines, multiphase clocks, address lines, and output buses.

Similarly, setup, hold times, and propagation delays must be stressed when analyzing worst-case timing conditions. In many cases, system performance may have to be evaluated under varying temperature or V_{CC} conditions.

Baril explains, "Although a 5,000-gate design may require only a few timing edges for input buses, control pins, and a clock, larger designs may consume dozens of edges merely to create the correct timing relationships needed to run a functional test."

In light of this, the XL2 supplies 48 timing edges, with 24 edges available to each pin. Timing is assigned on a per-pin basis. Consequently, measurements can be made for individual device pins.

The leading driver edge for an input pin can be placed anywhere in the cycle—from zero delay to cycle-end—with no holes or dead zones. Similarly, device outputs can be sampled anywhere in the cycle, with 100-ps resolution.

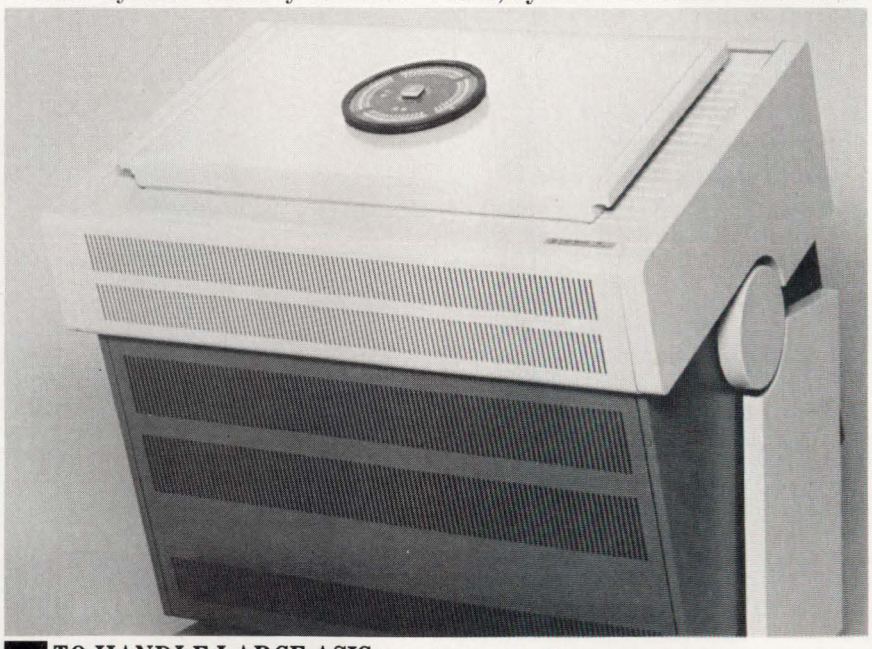
Total system accuracy is better than ± 1.75 ns across all 896 channels. An automatic calibration feature maintains this accuracy by calibrating individual driver edges to match the threshold level of corresponding device pins.

Of course, high-performance drivers are needed to deliver clean, symmetrical edges to a device's input pins. In the XL2, the drivers' rapid slew rate enables them to deliver a 5-V swing in well under 5 ns. This affords accurate timing measurements.

FIXTURING IS CRITICAL

Other factors help determine performance. For example, the quality of the device fixturing critically effects driver edge delivery and acquired response data. Like other Logic Master family members, the XL2 eliminates the need to hand-wire signal pins through an automatic wiring scheme that uses a 50-Ω transmission line from the device pin to the XL2 pin electronics. For large devices, the system supports a 512-pin circular socket card *(see the figure)*. Custom socket cards can be developed for up to 896 signal pins.

As noted, with the system's distributed resource per-pin architecture, system resources can be inde-



TO HANDLE LARGE ASICs, the IMS XL2 verification system supports a 512-pin circular socket card. The system runs 50-Ω signal paths from the system's pin electronics to the socket card.

ASIC VERIFICATION SYSTEMS

pendently assigned to device pins. Besides accessing 24 of the 48 available timing edges, each pin has access to four of the system's eight pairs of drive rails. Three-stating, formatting, and masking are also assigned on a per-pin basis. With this flexibility, complex devices—especially those with mixed technologies—are easily verified.

ALTHOUGH A 5000-GATE DESIGN MAY REQUIRE ONLY A FEW TIMING EDGES FOR INPUT BUSES, CONTROL PINS, AND A CLOCK, LARGER DESIGNS MAY CONSUME DOZENS OF EDGES MERELY TO CREATE THE CORRECT TIMING RELATIONSHIPS NEEDED TO RUN A FUNCTIONAL TEST.

Even at full speed, the XL2 doesn't compromise full programmability of data formatting and timing. Nine data formats are available, including NRZ, DNRZ, RZ, RZI, R1, RC, RI, 2xRZ, and 2xR1. At 80 MHz, the system can drive inputs into a bidirectional data bus and sample its output, all in the same cycle.

Each I/O pin is backed by 5 bits of memory, allocated individually for pattern generation and data, three-state, expect memory, acquire memory, and mask memory. Up to 64 kpatterns are available behind each bit. Furthermore, if the designer calls upon the system's built-in pattern compression, even deeper patterns can be stored.

With the pattern compression, any vector can be repeated up to 4096 times. Moreover, additional pattern compression comes from embedding repeating patterns within loops. If a pattern still exceeds available memory after the compression techniques are applied, the pattern can be segmented into 64 k sections and downloaded at DMA speeds.

Any pin can serve as a "keep-alive" clock for a dynamic device while the pattern memory is reloaded. In effect, this yields a sort of infinite memory without sacrificing any system performance characteristics.

Just three display screens can completely program the tester. As with other Logic Master systems, the screens are completely interactive and any parameter can be changed with the results immediately displayed.

All measurements can be automated, reported, summarized, and graphed with IMS' optional CTA (characterization and timing analysis) software. The software gives designers a spreadsheet environment from which they can completely control the XL2.□

PRICE AND AVAILABILITY

Prices for the Logic Master XL2 configured for 480 channels start at $470,000. The system will be available in October.

Integrated Measurement Systems Inc., 9525 S. W. Gemini Dr., Beaverton, OR 97005; (503) 626-7117. **CIRCLE 511**

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HIGHLY	544
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SLIGHTLY	546

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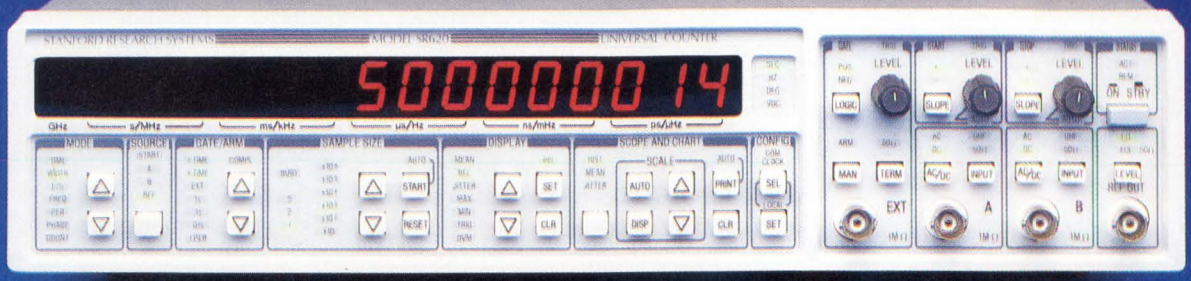

4 ps single-shot resolution
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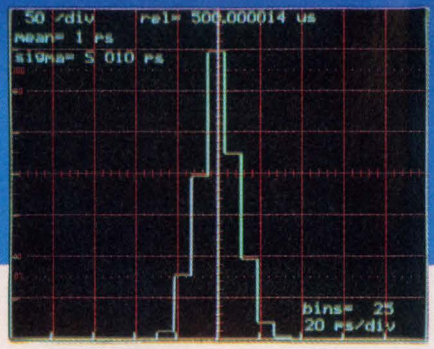
Statistics, analysis, and graphics



The SR620 provides graphic display of histograms and strip charts on any X-Y oscilloscope. With Autoscale and Zoom, graphics can be easily scaled. Attach a dot matrix printer or an HP-GL plotter and obtain hardcopy of any graph.

Finally, high resolution time interval measurement at an affordable price. The SR620 Universal Time Interval Counter offers 4 ps single-shot LSD on time intervals, and 11 digits of frequency resolution in one second. With powerful arming, gating, and triggering modes, the SR620 can measure time interval, frequency, period, pulse width, and phase, as well as rise and fall times.

The SR620 has built-in statistical functions, including mean, min, max, standard deviation, and Allan variance for up to 1 million samples. Results may be displayed on the front panel, and graphed in histogram or strip chart form on an X-Y oscilloscope. Hardcopy is directly available on a plotter, printer, or chart recorder.

With both RS-232 and GPIB interfaces standard, the SR620 is also ideal for ATE applications.

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SR620	**$3850**
Single-shot resolution	4 ps
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Maximum time interval	1000 s
Maximum frequency	1.3 GHz
Frequency resolution	10^{-9} Hz
Phase resolution	0.001°
Statistics	Mean, Min, Max, Std. Dev, and Allan Var.
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CIRCLE 35

PROGRAM ADJUSTABLE ATE VALUES WITH AN OCTAL DAC

WITH THE HELP OF EIGHT ON-CHIP D-A CONVERTERS, TEST ROUTINE SOFTWARE EASILY SETS ADJUSTABLE ATE PARAMETERS.

MIKE BYRNE AND PASCHAL MINOGUE
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It's only natural that the problems of designing automatic test equipment (ATE) have kept pace with the sophistication of the electronic equipment to be tested. The increased complexity of IC design demands that testing equipment itself becomes faster to accommodate more test points. Add size and cost restraints, and the need for inexpensive, compact test pin electronics becomes obvious.

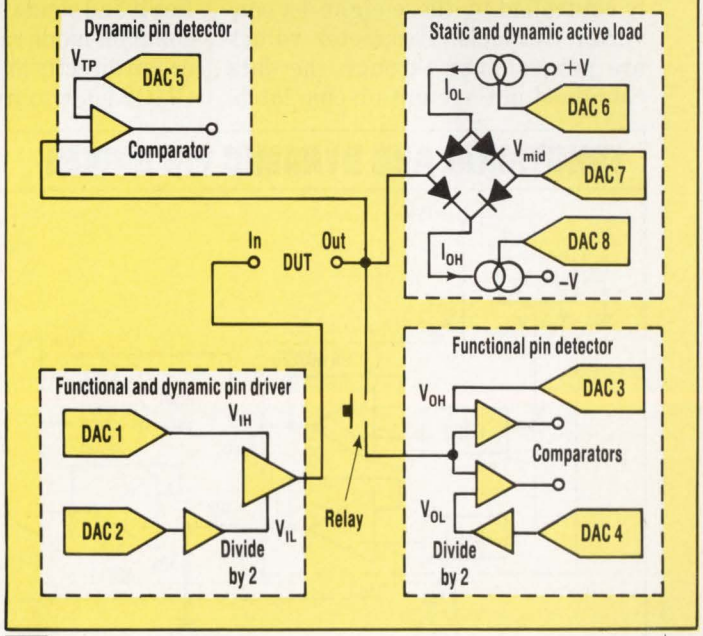
The trend in ATE design is moving toward a "pin-slice" architecture, meaning that each pin is a complete tester with programmable stimulus and measurement capabilities. Consequently, any device that packs significant functional density into a small package is a welcome addition to the ATE designer's toolkit.

A test-head pin driver and detector calls for this increased functional density. VLSI package pin counts of more than 100 are now commonplace, and each pin must be checked for both dc and ac functionality.

Ideally, each adjustable quantity involved in the basic pin-tester functions should be programmable from the test-routine software. Analog Devices' AD7228 octal digital-to-analog converter, which integrates eight V-mode d-a converters, eight output buffers, and fast interface logic on one chip, offers a way to achieve this programmability.

The AD7228 chip is built with Analog Devices' linear-compatible CMOS (LC^2MOS) process, which combines precision bipolar components with low-power CMOS logic. Low power is important in systems with a high density of active components. Bipolar drivers are necessary for

TEST-HEAD PIN DRIVER AND DETECTOR



1. THE EIGHT D-A converters on the AD7228 chip are split among the tester's four basic sections. On-chip latches supply the data necessary to program the d-a converters with correct parameter values for a particular DUT.

PROGRAMMABLE ATE

speed and current. Separate on-chip latches are supplied for each of the eight d-a converters, and a 3-bit address input (A_1, A_2, A_3) determines which latch is loaded when the Write signal (WR) goes low.

Basically, one digital-pin tester card has four distinct sections: a functional/dynamic pin driver, a functional pin detector, a dynamic pin detector, and a static/dynamic active load *(Fig. 1)*. The pin driver employs two d-a converter-generated voltages (V_{IH}, V_{IL}) to supply an input signal to the device under test. The DUT's output is then supplied to both pin detectors to test output levels and dynamic parameters. The functional pin detector uses two d-a converters to generate reference voltages (V_{OH}, V_{OL}) and two comparators to determine the DUT's voltage swing (high/low). To perform timing tests, the dynamic pin detector uses one d-a converter (generating V_{TP}) and a trip comparator. The active load supplies an adjustable current source or sink on the DUT using three d-a converters and a diode bridge.

The tester's eight adjustable voltage parameters (V_{IH}, V_{IL}, V_{OH}, V_{OL}, V_{TP}, I_{OH}, I_{OL}, and V_{mid}) are individually controlled by these eight d-a converter channels. Parameter values are programmed through the data contained in the eight on-chip latches. Data is transferred into the latches through a common 8-bit TTL/CMOS (5-V) compatible input port.

The functional and dynamic pin-driver section of the tester modifies an input waveform to supply the voltage levels and signals required by the DUT. This section consists of a pin driver, a precision voltage reference, an op amp, and two of the eight d-a converters *(Fig. 2)*. The input waveform is applied to the high-speed differential inputs of the AD1322 pin-driver chip, which modifies it and sends it to the DUT. With a common-mode range of 5 V, the driver can directly link with ECL, TTL, or CMOS logic sources.

THE TESTER'S PARAMETERS ARE INDIVIDUALLY CONTROLLED BY THE EIGHT D-A CONVERTER CHANNELS.

The pin driver must also supply the DUT with a high slew-rate input source for fast timing tests. The AD1322 driver in this example has an output slew rate of 2000 V/μs. Because of space constraints, both static and dynamic performance tests are excited by the same high-speed pin driver.

The AD1322 pin driver's output high and output low voltage levels are determined by the chip's V_{high} and V_{low} inputs, respectively. Data held in the first on-chip latch programs its d-a converter to directly drive the V_{high} input with the correct voltage. The output of the second d-a converter, which is programmed by data contained in the second latch, is divided by two and then applied to the V_{low} input.

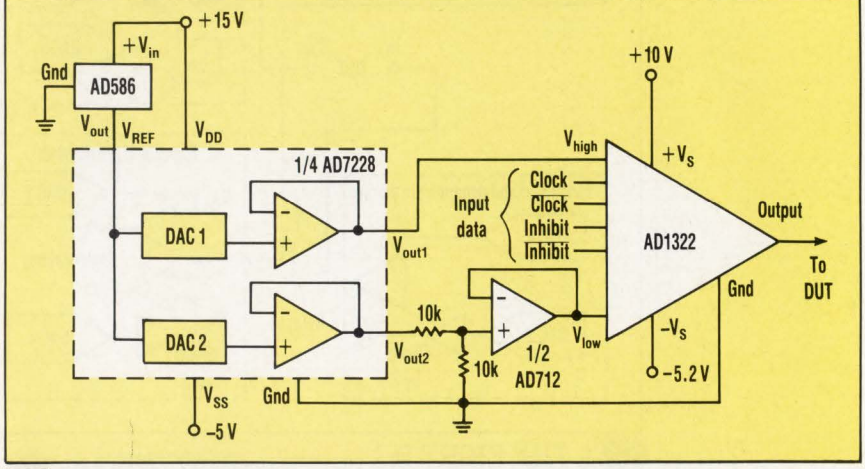
The 5-V reference voltage to the d-a converters, supplied by an AD586 precision voltage reference, limits the V_{out1} (and subsequently V_{IH}) voltage to between 0 and 5 V. Although this is sufficient for testing most bipolar and MOS devices, the range can easily be changed with an alternative reference source. With the reference set at 5 V, a total output voltage error of ±20 mV with a resolution of 20 mV means that the input high level to the DUT can be set with an accuracy of ±0.4%.

The V_{out2} voltage range, also 0 to 5 V, is adequate for the DUT input low level. If the V_{out2} signal is applied directly to the V_{low} input of the pin driver, only a limited input code range of the octal d-a converter can be utilized. Therefore, the output voltage from V_{out2} is applied to two 10-kΩ resistors and an AD712 dual precision op amp to halve the input voltage to the V_{low} input pin. The result: The error on the input low voltage level to the DUT is also halved, and more of the input code range is used.

DEVICE TESTING

After receiving an input signal, the DUT's outputs are tested by the functional or dynamic pin detector. The functional pin detector tests the DUT's digital outputs by comparing them with correct high and low output voltage levels. Two more d-a converters from the AD7228 chip, as

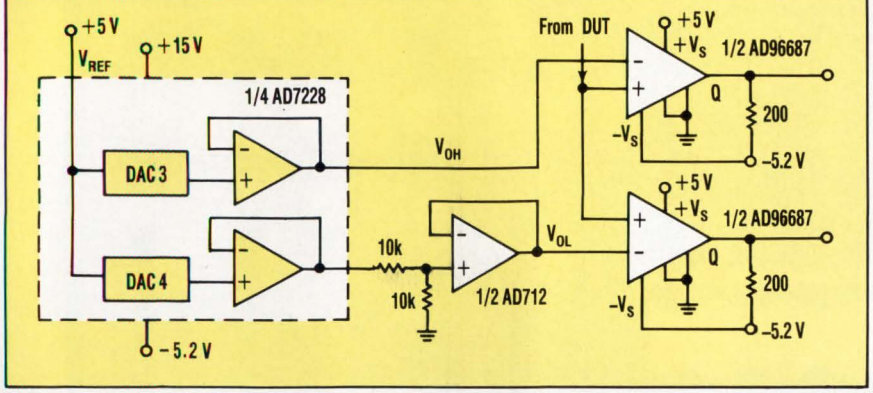
FUNCTIONAL AND DYNAMIC PIN DRIVER



2. BOTH THE HIGH- and low-input voltage levels to the device under test (DUT) are programmed by the user within ±0.4% accuracy. The precision voltage reference determines the input level range.

PROGRAMMABLE ATE

FUNCTIONAL PIN DETECTOR



3. AN AD96687 DUAL op amp tests the DUT's output voltage levels by comparing them with the expected values programmed into the third and fourth d-a converters.

well as a AD96687 dual comparator and AD712 high-speed op amp, are employed in the functional pin-detector circuit *(Fig. 3)*.

The output high (V_{OH}) and output low (V_{OL}) threshold voltage levels are programmed by the third and fourth d-a converters, respectively. As with the functional pin-driver circuit, the V_{OH} level is applied directly to the comparators, while the V_{OL} level is first divided by two to give greater resolution and use more of the digital-to-analog converter code range.

When an output-high voltage level is expected from the DUT, both comparator Q outputs should be high. Similarly, both Q outputs should be low when an output-low level is expected. Any combination of outputs from the comparators, other than those expected, indicates a functional failure of the DUT.

An added feature is the circuit's detection of high-impedance output states from the DUT. High output impedance forces the output voltage levels to the V_{mid} value found in the active-load circuit. This mid-value usually sits between the V_{OL} and V_{OH} thresholds. If a high-impedance state is expected, a high Q output from the V_{OL} comparator and a high $\overline{Q}$ output from the V_{OH} comparator indicate that the DUT is operating correctly.

The Q outputs from the AD96687 dual comparator are open emitter and fully ECL compatible. Consequently, they need a 200-Ω pull-down resistor, which brings down the voltage level to –5.2 V. The common-mode range for the differential input stage of the comparators is –2.5 to +5 V. If the output voltage from the DUT can exceed this range, it should be attenuated before being applied to the comparators. Also, the V_{OH} and V_{OL} voltages from the d-a converters should be adjusted accordingly.

The dynamic pin detector compares a DUT output waveform with a trip-point voltage for the measurement of parameters, such as propagation-delay time, setup time, hold time, pulse width, and rise and fall times. The pin detector consists of one d-a converter and a comparator *(Fig. 4)*. High-speed timing tests demand a fast, high bandwidth comparator. This example uses the AD96685 with a maximum propagation delay of 3.5 ns.

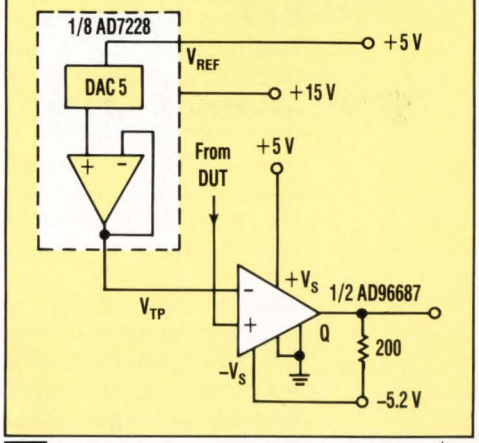
The third d-a converter channel sets the threshold-detector trip point (V_{TP}). As with both the pin driver and functional pin-detector circuits, parameters can be set with a resolution of 20 mV over a 0 to 5 V range. For pulse-width measurements, the comparator trip point is typically set to some midpoint value of the output levels, like $V_{TP}=(V_{OH}+V_{OL})/2$. For measuring propagation delay and rise and fall times, it is programmed to the 10% and 90% level of the DUT output.

To minimize capacitance and impedance problems, the dynamic pin detector should be separate from the functional pin detector. Pc board layout influences the pin-to-pin waveform skew of each input and output signal. Unequal track lengths cause differences in skew, and unless these differences can be calibrated, all the tracks leading to and returning from the DUT must be as close as possible in electrical length. The latter restriction usually dictates a radial form of track layout.

Both the functional and dynamic pin tests must be performed under loaded conditions (meaning that the device outputs are required to source or sink specified currents). A static and dynamic active load is constructed with the final three d-a converters, a dual high-speed op amp, a buffer, a diode bridge, and two transistors *(Fig. 5)*. Resistor values R_1 and R_2 are selected to convert the 0- to 5-V output voltage span of the d-a converter channel to a current source range of 0 to 20 mA and a current sink range of 0 to 1 mA.

The three d-a converter channels supply programmable I_{OH}, I_{OL}, and V_{mid} values. High-level output current (I_{OH}) is the current flowing into an output when the input conditions establish an output high. The 7400-series logic I_{OH} of –0.4 mA indicates current flowing out of the output pin, and therefore I_{OH} in the active

DYNAMIC PIN DETECTOR



4. TIMING MEASUREMENTS are performed by a high-speed comparator with a trip-point voltage applied at the inverting terminal.

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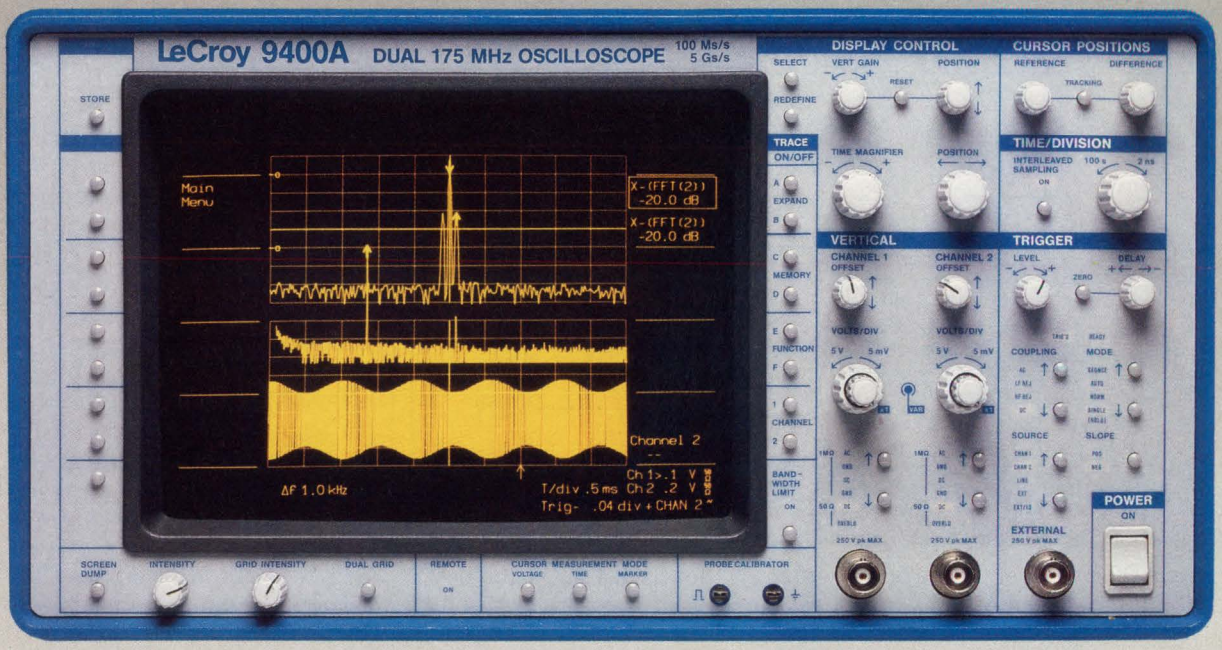

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load is a current sink. Low-level output current (I_{OL}) is the current flowing into an output when the input conditions establish an output low. The same logic produces an I_{OL} of 16 mA, indicating current flowing into the output pin and, thus, I_{OL} in the active load is a current source.

The V_{mid} value digitally determines when the currents I_{OH} and I_{OL} are directed into or steered from the digital output under test. V_{mid} is usually set to $(V_{OH}+V_{OL})/2$. I_{OH} is steered from the output pin if V_{out} is greater than V_{mid}. Also, I_{OL} is directed into the digital output pin if V_{out} is less than V_{mid}. As noted, the V_{mid} value is also used in timing measurements with high-output impedance states. The seventh d-a converter channel sets the mid-point voltage with 20-mV resolution over a range of 0 to 5 V.

An intermediate buffer amplifier between V_{out7} and the diode bridge is needed to sink I_{OL} and source I_{OH} when they aren't applied to the DUT's output. The buffer may have to supply a differential current (the difference between I_{OH} and I_{OL}) of up to 20 mA. This example uses an AD845 buffer, which settles to within 0.1% of its final value in 250 ns.

The buffer amplifier driving the diode bridge can be replaced with a complementary (npn-pnp) transistor pair, which would also source and sink the excess currents. To maintain a balanced arrangement, though, two extra diode-connected transistors must be added to the diode bridge, doubling the V_{BE} matching requirement.□

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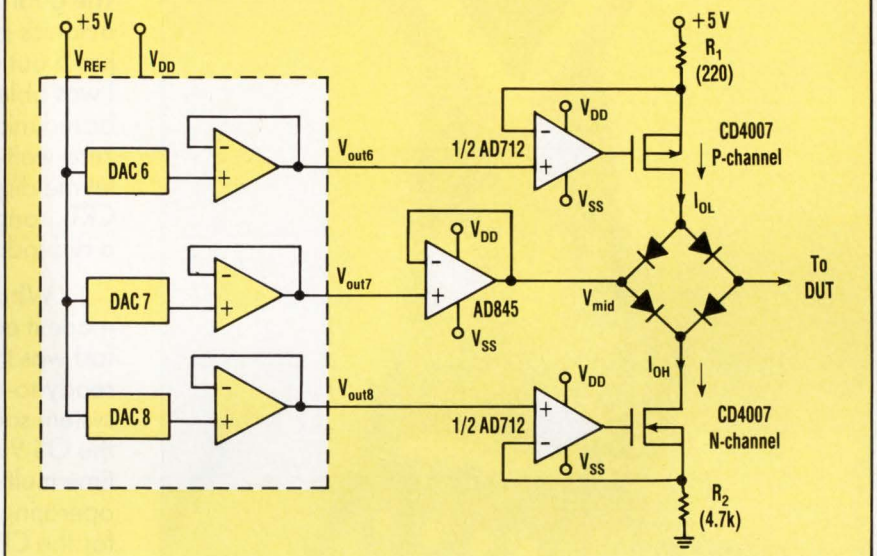
Paschal Minogue, a senior design engineer at Analog Devices BV, has a BSEE from University College, in Dublin, Ireland.

HOW VALUABLE?	CIRCLE
HIGHLY	556
MODERATELY	557
SLIGHTLY	558

STATIC AND DYNAMIC ACTIVE LOAD



5. THE CHIP'S LAST three d-a converters supply the parameter values that establish necessary load conditions. The value of V_{mid} determines when the tester will source or sink load current.

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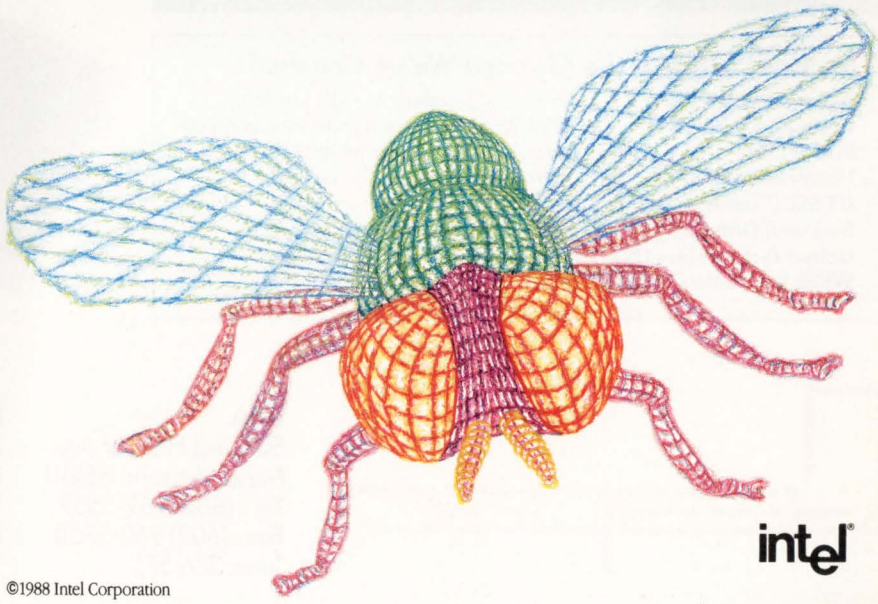

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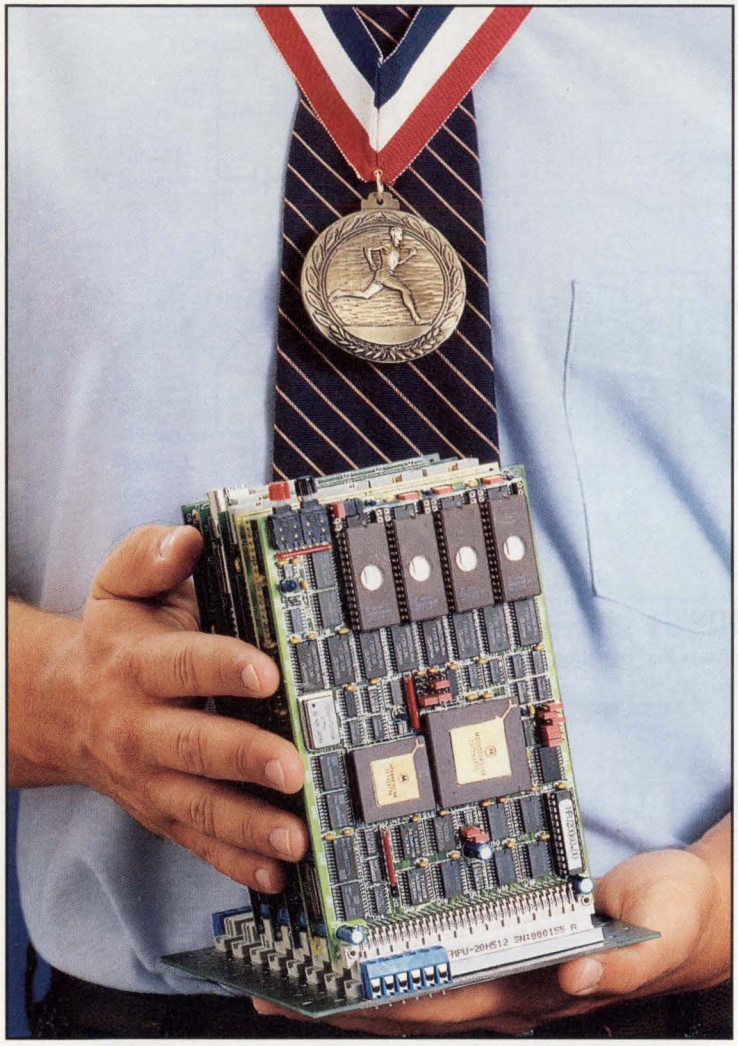

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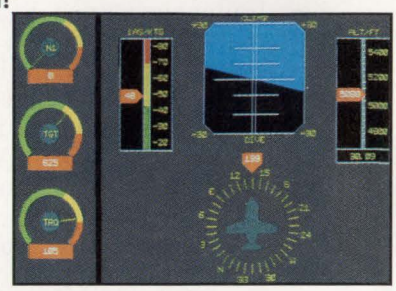

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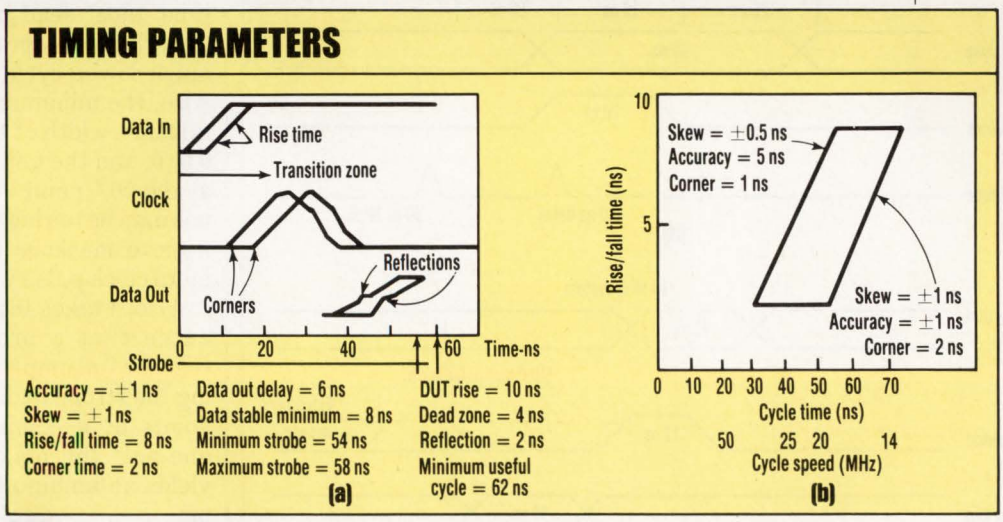
CYCLE SPEED ISN'T NECESSARILY THE BEST WAY TO RATE DEVICE TESTERS. MULTIPLE EDGE AND STROBE FORMATTING PERMIT LOW CYCLE RATE TESTING.

TEST DEVICES EASIER AT LOW CYCLE RATES

Now that devices are regularly breaking speed records, fast cycle rate testing is grabbing a lot of attention. Indeed, cycle rate often is key to defining a test system's ability. But cycle rate alone has little value, and other tester characteristics—such as rise time, dead zone, and skew—can limit the useful cycle rate of a test system to a value far below that of its specified speed.

Moreover, often device timing sensitivities can be determined independently from cycle rate testing. A tester can isolate critical timing parameters and fully characterize a device under test (DUT) at very low cycle rates. This approach alleviates problems caused by test system characteristics at high cycle rates.



1. TIMING DIAGRAMS SHOW some of the factors that can make a tester's useful cycle rate much lower than its specified cycle speed (a). A simple graph of tester characteristics helps determine the unit's useful cycle time (b).

DICK GOMEZ
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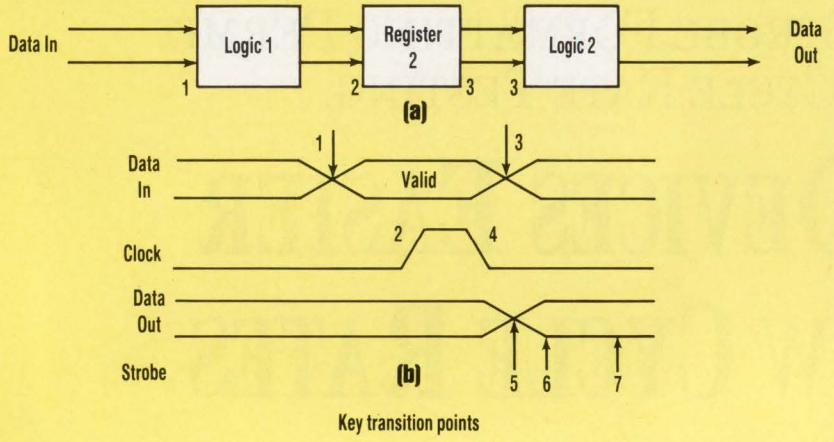
TESTING DEVICES

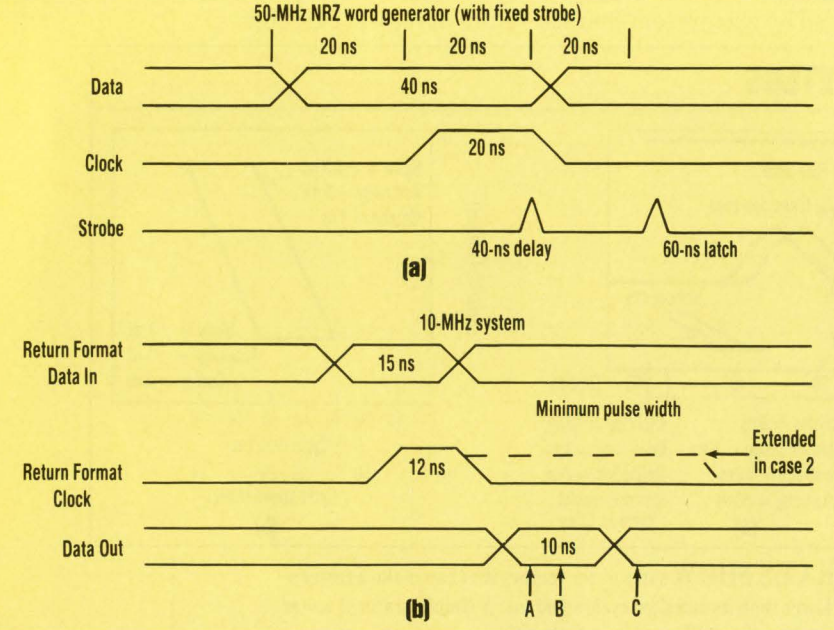
TEST EXAMPLE



1. Input data changes.
2. The leading clock edge allows the input data change results to propagate through Register 2 and into Logic 3.
3. The point at which the input data no longer has to be valid for proper latching to take place.
4. The latching edge of the clock. Data in the register will be held until the next clock leading edge.
5. The change of output data resulting form the input data change.
6. Minimum output strobe determines where output data first reaches its final value.
7. Latching the output data strobe ensures that the data is present on the output after an input data change has had time to propagate to the output.

2. EVEN A SIMPLE LOGIC CIRCUIT exhibits critical timing relationships (a), but a test engineer can isolate these relationships and stress them independently at low cycle rates (b).

COMPARING TESTERS



3. A 50-MHZ NONRETURN-TO-ZERO word generator (a) is limited in its ability to characterize the circuit of Fig. 2. A slower, 10-MHz tester with 1-ns resolution and multiple formatted edges does a better job (b).

Unless design and test methods are carefully planned to accommodate the conditions in which the device and tester operate, results can be ambiguous. Ideally, the tester should isolate and stress the device's timing sensitivities while holding other time-related signals in a nominal, nonstressed condition.

This is important for diagnostic purposes and to account for issues such as test system dead zones, skew, and accuracy; variations in the rise and fall times of the DUT and the tester; and reflections on the DUT output waveforms. An examination of these issues highlights the problems in testing a DUT at full cyclic rate with all transitions (time-oriented signals) stressed.

A set of typical timing diagrams demonstrates how the timing parameters noted affect the useful cycle rate *(Fig. 1a)*. These diagrams further point out the potential difficulties in fitting all transitions into a limited cycle time. To evaluate the diagrams, a number of timing parameters must be defined *(see "A glossary of timing terms," p. 90)*.

The timing diagrams show the limits faced by the test engineer. The minimum cycle time to which the tester can be programmed for this simple case is 62 ns (minimum strobe time plus dead zone time), even though the device could operate at a much lower cycle time on a board. Also, the minimum programmed total pulse width of this tester is 26 ns, 0 to 0, and the minimum pulse width at the 50% point is 14 ns. These values may be too high to allow the engineer to measure the device's minimum clock pulse width.

Also, it takes 16 ns from T_0 to guarantee that a programmed pulse reaches full amplitude. Finally, moving the strobe to determine pass/fail points at a compare amplitude of one-half the maximum amplitude yields an ambiguity of 2 ns on each pin.

A tester with these characteristics could have a data rate specified at 40 MHz (a 25-ns cycle time). In a real, very simple test environment, however, the tester's useful cycle rate is more likely to be about 16 MHz (a 62-

ns minimum cycle time). To precisely characterize this device with this tester, the engineer must manually set up the system with a scope and external delays. This assumes that the enginer can control pin skew, preferably with software rather than hardware. But the tester could never test the device at its full cycle rate, even though the cycle rate specification may imply that capability.

To achieve a useful cycle time of under 40 ns with the example waveforms, the rise and fall times should be less than 5 ns; skew and accuracy combined should be ±1 ns; and corner time should be under 1 ns *(Fig. 1b)*. This assumes a 5-ns dead zone, a 5-ns device delay, and three nonoverlapping transitions per cycle.

Of course, it could be argued that the data transition zone and the leading edge of the clock could overlap, thus gaining a few nanoseconds. But in most practical situations the overall device delay and rise time is likely to exceed 5 ns. In any event, the example offers a useful estimate for minimum cycle time and emphasizes the need to examine all aspects of timing.

Fortunately, by using multiple timing setups, a test engineer can stress most timing sensitivities without cycle rate testing—that is, without trying to compact all transitions into a minimum cycle time. If the tests are properly designed, they will accurately predict the device's cycle rate capability. Setting up the timing for the tests is easier at low cyclic rates than at high rates and the procedure is less susceptible to tester-DUT interaction problems. Tester and DUT rise and fall times need not be as stringent, and the engineer need not work around tester dead zones.

The tester can place transitions anywhere in a test cycle and move noncritical transitions to noncritical times, eliminating ambiguity. Overall accuracy, of course, still depends on the test system's placement accuracy and skew.

An explanation of VLSI timing helps in understanding low cycle rate testing. Basically, transitions occur in a VLSI logic device for three reasons: changes of input data, clocking of signals to move data internally, and changes of output data. An unlimited variety of transition combinations is possible, but a basic sequence of events is usually established for any given part or family of parts. Typically, this sequence is:

Instruction (change of data input)
Execution (internal data movement and operation on data)
Results (observation of outputs and feedback data)

The relationships between these transitions at the device pins, as well as internally generated transitions not directly controlled from an external pin, cause timing sensitivities. To uncover these timing sensitivities, test engineers performing design verification must be able to create and place transitions and strobes with great accuracy and resolution.

For internally generated transitions, test pins should permit key transitions to be controlled externally, at least in the early stages of development. With this control, the engineer can debug the part even if a timing problem exists with the internally generated transition circuitry. Also needed are the ability to independently move the transitions presented to the DUT and to note the times at which the DUT creates output transitions.

A simple circuit containing two logic elements and a register illustrates this testing method *(Fig. 2a)*. While maintaining the time from transition 1 to transition 3 at a nonstressing value, the tester reduces the width of the clock pulse until errors occur *(Fig. 2b)*. The data strobe should be set to verify latching (strobe position 7). The smallest width at which no errors occur is the minimum clock pulse width.

Next, the tester moves the clock

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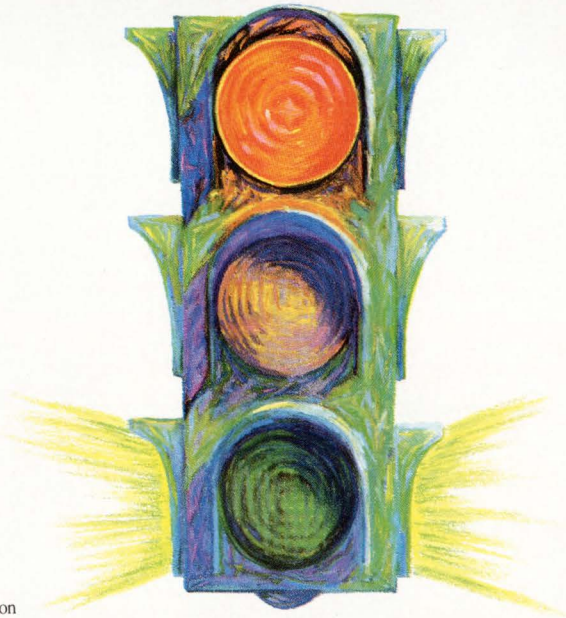

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pulse back toward transition 1 while maintaining clock width (the relation between transitions 2 and 4) at its minimum value. Errors occur when transitions 1 and 4 are too close to allow the input data to propagate through the latching circuits before latching edge 4 occurs. This point defines the maximum data rate at which latching occurs.

While holding transitions 1 and 4 at the point noted, the tester then moves back transition 3 until a failure occurs. This minimum time between transitions 3 and 1 defines the maximum data change rate.

Finally, the time between transition 1 and strobe 6 under the preceding conditions is the turn-on delay time, determined by moving the tester data strobe to the pass/fail point.

If the tester had simply reduced the cycle time and scaled the transition placements accordingly, the conditions under which errors started to occur would still have to be reviewed. The engineer would also have to vary the test setup to determine that the transition combination represented minimum cycle time rather than a violation of a transition relationship (for example, minimum clock pulse width).

This circuit can be completely tested with a slow cycle rate tester (10 MHz) with multiple edges and full formatting. However, a 50-MHz non-return-to-zero (NRZ) pattern generator would be of little value in trying to test the timing relationships, since edges and pulse widths could occur only in 20-ns increments.

Timing diagrams for two such typical systems point out that characterization with the 50-MHz NRZ word generator with fixed strobe is very limited *(Fig. 3a)*. The word generator can create a 40- or 60-ns cycle time but cannot determine setup and hold times, transit delays, and the DUT's minimum cycle time. However, the 10-MHz tester with 1-ns resolution and multiple formatted edges creates transition relationships and strobe positions that fully characterize the device *(Fig. 3b)*.

With the strobe at B, case 1 employs minimum clock and data widths to determine the minimum

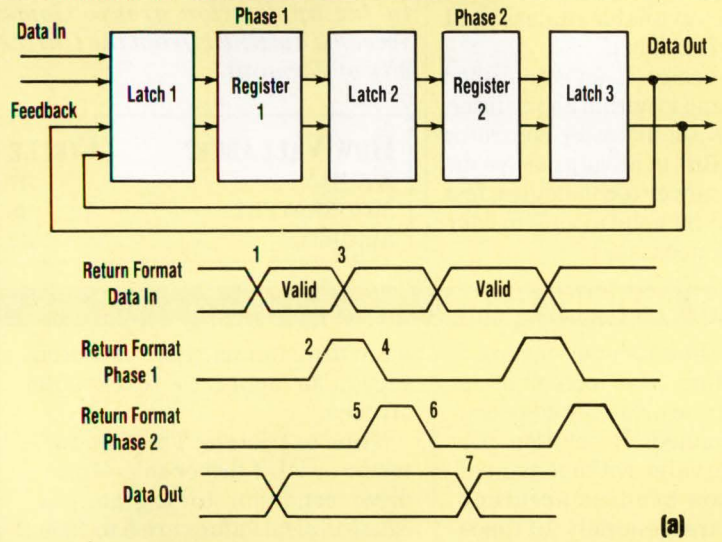
propagation time (at A) and the register's setup-and-hold time. In case 2 the tester extends the clock pulse to allow data transitions to propagate through the register to the output. Time A is verified to correlate the results from case 1, and time C establishes when a subsequent input data change propagates to the output. In this example, the test system's key feature is that it can create minimum pulses and multiple timing transitions with fine resolution, tight tolerance, accuracy, and very low skew.

This comparison represents two extremes in system capability. Today's testers offer a wide variety of waveform-creation and data-sampling capabilities.

Another important point is that for most complex parts clock rate, not data rate, becomes a figure of merit for speed. Since devices usually include two or more clock intervals between the data in transitions, the part's cycle rate (as presented to a tester) may be one-half or less that of the clock rate. As a result, if a system creates double clock pulses in one cycle, it needs a cycle rate of only one-half the DUT's clock rate.

For example, consider a part in which two clocks must each make two transitions within every data cycle. Data from a feedback path must combine with input data to yield the

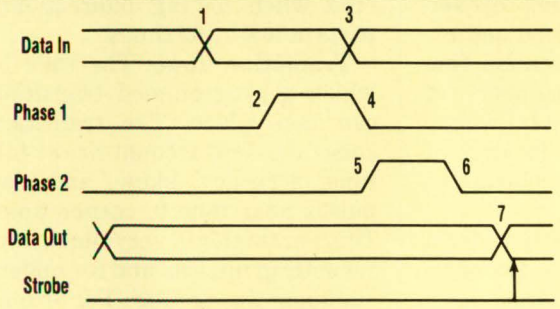
EFFECT OF CLOCK RATE



(a)

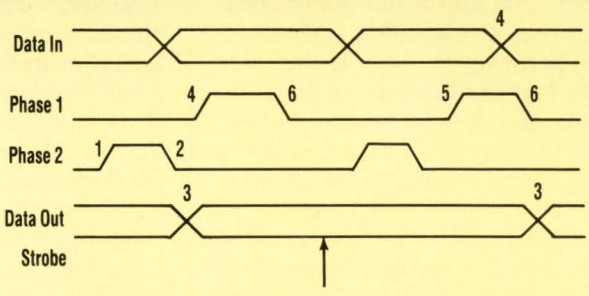
Key Transition points

1. Data In becomes valid and propagates through Logic 1.
2. Enable edge of Phase 1 allows results of Data In and feedback to propagate through Register 1 and Logic 2.
3. Data In becomes invalid.
4. Latching edge of Phase 1 holds Data In and feedback data at output of Register 1.
5. Enable edge of Phase 2 allows the results of Data In as stored in Register 1 to propagate through Register 2 and output Logic 3 and to feed back results to Logic 1.
6. Latching edge of Phase 2 allows feedback and Data Out to remain constant while new data is combined with feedback data and stored in Register 1.



Transition	Relationship
1-3	Minimum data width.
2-4	Minimum Phase 1 clock width.
5-6	Minimum Phase 2 clock width.
1-4	Setup and hold for Register 1 through Logic 1 for Data In changes.
2-6	Setup and hold for Register 2 through Logic 2.
5-7	Propagation delay through Register 1 and Logic 3.
1-7	Delay from Data In to Data Out after feedback has been established in Logic 1.

(b)



Transition	Relationship
1-6	Establishes the minimum time for feedback to be latched into Register 1 while data is stable.
1-2	Nominal setup to ensure that results aren't affected.
4-6	Minimum pulse width for Phase 1.
5	Data In transition placed to ensure no affect on the results.
Strobe	Placed to ensure correct logic state is achieved. Noncritical.

(c)

4. WHEN FEEDBACK and input data must combine for correct results, the device needs multiple clocks in each cycle (a). In this case, data must change at one-half the clock rate. This can be characterized by varying the relationships between the transitions. In case 1 (b) the tester moves edges and strobes to create minimum pulse widths and spacings. In case 2 (c) propagation delay of the feedback through logic 1 is determined by the relationship between the leading edge of Phase 2 and the trailing edge of Phase 1.

proper results *(Fig. 4a)*. Consequently, the data must change at one-half the clock rate. As in the first example, the test engineer can determine timing sensitivities by varying the relationships of the transitions at a relaxed cycle rate.

Two main cases apply. Starting with minimum clock pulse widths, the first case develops relationships that derive the minimum time needed for input transitions to propagate to the outputs *(Fig. 4b)*. The minimum time for Data In changes latched into Register 1 can also be found. Case 2 examines the minimum time that feedback transitions require for latching into Register 1 *(Fig. 4c)*.

In this circuit, the minimum cycle time is the shortest period between the time the combined data and feedback reach the input and the time the next results successfully propagate through the device. This figure includes the minimum transition relationships established in cases 1 and 2.

If this second part had internal timing circuits and the relationship of Phase 1 and Phase 2 couldn't be controlled externally, the tester could verify worst-case delay by relating the data in transition to the timing circuit transition. The only way to determine the feedback delay, however, would be to operate at the rated cycle time or by double-pulsing the clock pin in one cycle. Other information on sensitivities wouldn't be available unless test points were furnished.

So, if the design is an established technology and is within limits, internal timing without tester control is acceptable. But in an aggressive design or with newer technologies, test points would be helpful and, in complex circuits, necessary.

Note that although most timing sensitivities can be determined with the techniques described, the power and temperature effects for CMOS circuits depend on cycle time or clock rate. The temperature change created by a change in cycle time affects a device's timing characteristics. This offset can be duplicated at low cycle rates by testing at an elevated temperature.□

Richard Gomez, Cadic's vice president of engineering, oversees product development and engineering in the application group. Gomez received his BSEE from the University of Vermont.

How Valuable?	Circle
Highly	547
Moderately	548
Slightly	549

A GLOSSARY OF TIMING TERMS

Accuracy: How close to a programmed value a tester can position transitions. In this discussion, accuracy doesn't include skew. For example, consider a bus transition programmed to occur at 20 ns from time 0. If measurements show that all the bus edges occur between 18 and 20 ns, skew is ±1 ns; accuracy is –1 ns. If the same bus is programmed to a different time, and skew is the same but distributed around a time 1 ns above the programmed value, general accuracy would be ±1 ns.

Corner time: The time from the beginning or end of a transition to the level at which the rise or fall time begins or ends. For low amplitude pulses (such as ECL) and with certain types of drivers, the corner times can exceed the rise and fall times.

DUT waveform reflections: A step in a DUT's output. In effect, reflections create a flat, constant voltage point in a rising or falling transition. These voltage plateaus can cause ambiguous time readings if the waveform is strobed for the reflection amplitude when the reflection occurs.

Resolution: The increment in which a strobe or driver edge can be programmed. Resolution per se is of little value without manual intervention because accuracy and skew are generally 10 times the resolution. It is important, however, for fine-tuning test setups with an oscilloscope and external standards, because fine resolution lets test engineers set clock pulses precisely where they're needed. The linearity of resolution can be as important as the increment.

Rise/fall time: The time for a transition to go between two specified points on a waveform.

Test system dead zone: A period of the tester cycle where edges and strobes cannot be programmed. Because the dead zone may have to be added to the cycle, it can slash the test-system's useful cycle rate.

Test system skew: The difference in the time for different tester drivers programmed to the same time value to reach 50% of full amplitude as they go from minimum to maximum or maximum to minimum. Skew and accuracy also apply to test-system strobes.

Time to tristate: The time for a tester or DUT driver to go from a drive condition to tristate. Because typical values are 5 to 10 ns, time to tristate must be considered when testing bidirectional parts at low cycle times.

Transition zone: The time in which a programmed transition can take place. The transition zone takes into account rise or fall time, accuracy, skew, and, for pulses near time 0, corner time. This parameter is very important for setting up tests and for understanding the results. For example, the relationship between bus data and a clock edge may require data to be present at least 10 ns before the clock transition reaches 50% of amplitude. The slowest bus driver (defined by the bus-transition zone) must be 10 ns from the fastest possible clock edge (defined by the clock edge's transition zone). This could require up to 30 ns or more of cycle time, depending on the test system and the device requirements.

ETHERNET CONTROLLER ADDS COMMUNICATIONS TO SCSI BUS

ORIGINALLY A DISK-CONTROL PROTOCOL, THE SCSI BUS STANDARD OFFERS SEVERAL ADVANTAGES TO USERS OF LOCAL AREA NETWORKS.

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Putting an Ethernet controller on the Small Computer System Interface (SCSI) bus offers some powerful advantages. For one, it lets a user connect an Ethernet node to any computer that supports SCSI, which today means almost all of them—from PCs to VAXs. It also reduces cost by integrating the transceiver on the same card with the controller. And because the SCSI bus can extend 6 m (18 ft) with a single-ended drive and 25 m (75 ft) with a differential drive, the controller can be outside the computer cabinet, directly connected to the Ethernet coaxial cable through the 50-conductor SCSI cable.

Also, the bus accommodates local intelligence and multithreaded logical connections. These features benefit software designers because they let the Ethernet controller pick up some of the higher levels in the ISO/OSI model, at least up to the transport layer. This ability not only offloads the host, but also avoids the inherently useless process of copying packets from one place to another until the proper program can interpret them.

Some computers, such as the Macintosh, have SCSI capability built in. For systems that already have SCSI-based storage devices, a user just adds the Ethernet controller at the end of the bus. Those without this head start must add a SCSI host adapter.

The controller's simple hardware design, using 17 DIP devices and several passive components, keeps the 8-bit processing that's natural for Ethernet and SCSI throughout the board. Three main ICs—a SCSI controller, an Ethernet controller, and a high-integration 8-bit processor—are at the heart of the design. A shared local bus lets the memory access all three chips *(Fig. 1)*.

Even though billed as a general-purpose interface, the SCSI standard shows its origins as a disk-controller protocol as soon as designers try to use it for something else.[1] The bus's inherent master/slave architecture implies that the host computer always "knows" what the peripheral is doing. As a result, the asynchronous events typically found in communication controllers are difficult to flag.

A good example is the sequence of events in an elementary read command initiated by the host computer. If the peripheral is a disk drive, sooner or later the correct track and sector are found, and the information is retrieved and delivered to the host. This read operation is completed in a known period, normally the disk-access time.

This is not the case when the SCSI target is a communication controller. In the example noted, if the host requests a read from the Ethernet controller, it won't get its data back until the packet arrives, which can well be a very long time (imagine a computer waiting for a remote user to press a key on a terminal). In the meantime, if the same host wants to write a packet through the Ethernet, it has no way, short of a full-blown reset, to break the previous connection on the read.

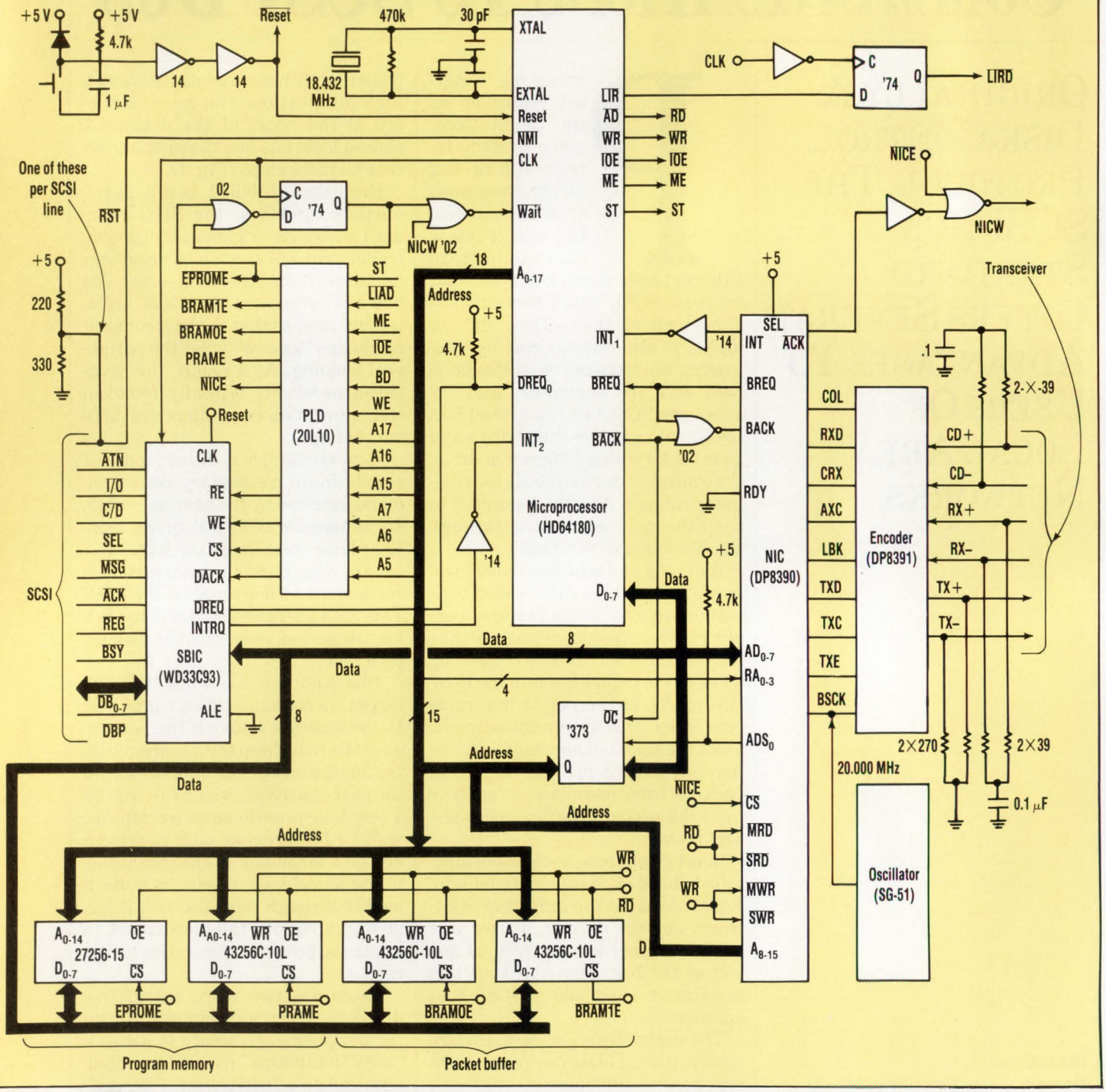
There are two ways out of this deadlock. First, a designer can give the peripheral the ability to act as a "host" ("initiator" in SCSI terminology) and give "peripheral" ("target" in SCSI) capability to the host. Then the system can flag asynchronous events from the controller to the host

ETHERNET CONTROLLER

computer without a previous request. The problem with this scheme is that the host operating system must incorporate special drivers that make the host computer appear to be a target.

The preferred solution to the "wait for read" syndrome is to take advantage of SCSI's ability to maintain multiple logical connections through one physical path—that is, multithreading. With multithread-

ETHERNET CONTROLLER CIRCUIT



1. THE ETHERNET CONTROLLER section maintains the 8-bit architecture natural to both Ethernet and SCSI. A shared local bus offers memory access to the circuit's three main ICs: a SCSI controller (WD33C93), an Ethernet controller (DP8390), and a highly integrated 8-bit processor (HD64180).

ETHERNET CONTROLLER

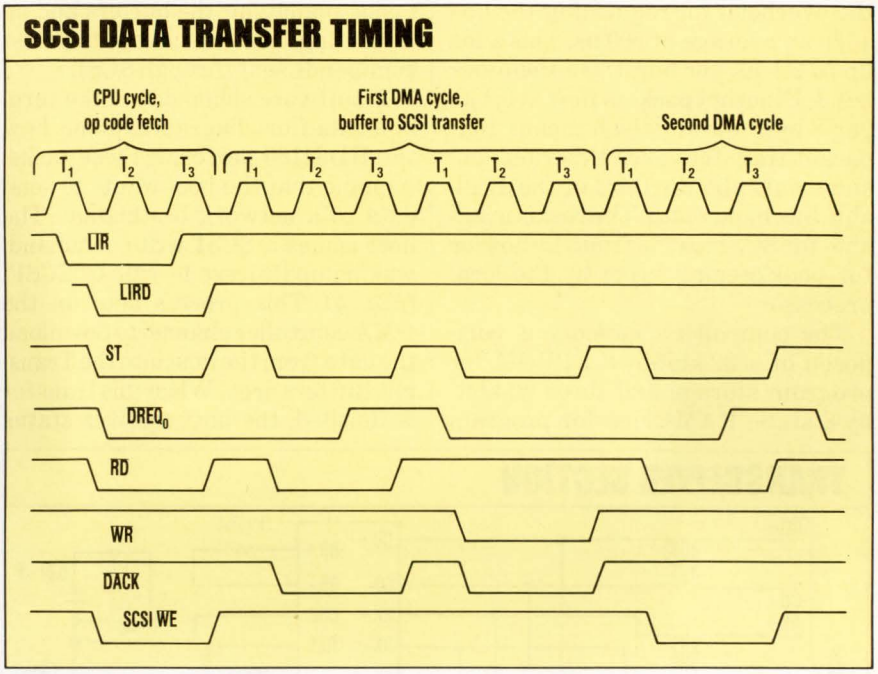
ing, the host (SCSI initiator) connects to a peripheral (target) and requests a certain transaction. If the peripheral isn't ready for the request, the physical path between the two devices is freed up, leaving the bus available for other transactions.

SCSI devices achieve multithreading with the logical unit number (LUN) concept. The controller accepts up to eight simultaneous host connections, called LUNs 0 to 7 (more could be employed through the SCSI extended identify mechanism). LUN 0 is a write and control channel (all such transactions execute in a limited time). LUNs 1 and up are read channels. As a result, a read request to LUN 1 can disconnect if no packet is waiting on the controller's receive buffer, so that write and control requests can proceed. LUNs 2 and up allow the controller to handle higher layer software. Consequently, each LUN represents an open socket or channel between the host and the outside world.

A total of 64 kbytes of static memory is used for buffering, and another 64 kbytes for program code and data. Two DMA channels, one in the processor and another in the Ethernet controller chip, speed data transfer. Careful priority analysis avoids lost data when more than one device wants control of the bus. One programmable logic device (PLD) supplies all decoding and DMA transaction timing.

At the SCSI end, the WD33C93 SCSI bus interface controller (SBIC) chip manages the traffic between the SCSI bus and the controller buffer memory.[2] This chip implements all low-level SCSI protocols in firmware, so very little work is left for the local microprocessor (HD64180). In a typical case, the designer programs the SCSI chip to wait for an initiator to select it and send a SCSI command. Only then is the processor alerted (through INT_2) for further action.

Owing to the low byte count involved, SCSI commands are processed using programmed I/O access to the WD33C93. SCSI data, however, is transferred by a DMA controller in the HD64180. Because this DMA controller doesn't recognize the typical REQ/ACK handshake, the PLD is programmed to identify the DMA cycle and automatically generate the ACK signal for the SCSI chip. A SCSI DMA transaction from controller to host takes six clock cycles/byte (651 ns); a host-to-controller transfer takes seven cycles/byte, or 760 ns *(Fig. 2)*.



2. THE PLD GENERATES the DACK and WR signals to the SCSI bus interface controller while the processor is still in the first read cycle. The second write cycle, to a nonexisting destination, is ignored, but it gives the SBIC time to lower its DREQ line and to obtain the next DMA cycle without releasing the bus. The PLD uses the Delayed Load Instruction Request (LIRD) and ST lines to tell between DMA and regular CPU cycles.

At the Ethernet end, the DP8390 Network Interface Controller (NIC) manages the Ethernet traffic and packet encapsulation/decapsulation.[3] The chip supplies automatic address recognition and check sum insertion, which are normal in all Ethernet chip controllers, as well as buffer management.

Typically, the network interface controller raises the BREQ line to the HD64180 anytime the controller wants to retrieve a packet from or place a packet into the buffer memory. Once the bus is granted, the NIC uses its own DMA controller to effect the data transaction. The bus grant signal from the processor, $\overline{BACK}$, enables the 74ACT373 latch. The latch picks the DMA controller's low-byte address information, which is generated at the NIC's $AD_{0\text{-}7}$ lines when the Address Strobe (ADS0) line is toggled.

The high-byte address information is generated independently on the NIC's $A_{8\text{-}15}$ lines. When the operation is complete, the controller releases the bus and interrupts the processor for further action. Since the NIC has its own buffer manager for received packets, overhead is minimal. Each received packet is preceded by a NIC-generated header with the status, length, and a link pointer to the next received packet.

Because the NIC has higher priority for bus use than the processor does, the controller can never be denied access to the buffers when an Ethernet packet arrives and SCSI transactions are taking place. The bus is released in a maximum of five and a half processor clock cycles, or 600 ns, so the NIC's 16-byte FIFO buffer cannot be overrun.

Data transfers between the buffer memory and the NIC occur in 8-byte bursts. Each byte transfer takes 200 ns (four 20-MHz clock cycles), and

ETHERNET CONTROLLER

the overhead for requesting the bus adds an average of 500 ns. This adds up to 2.1 μs per burst. On the other hand, Ethernet packets flow at 6.4 μs per 8-byte burst, which means that packet transfers over Ethernet consume only about a third of the available bus bandwidth. The rest is available for SCSI traffic from the host or for bookkeeping tasks by the local processor.

The controller's memory is composed of a 32-kbit-by-8 EPROM for program storage and three 32-kbit-by-8 static RAMs, one for program data and two for packet buffering. One wait state is inserted on an EPROM access, owing to its longer access time and the shortened read cycle on the processor's op code fetch. Half of a 74ACT74 section and a NOR gate create the wait state.

From the NIC, packets are sent and received through the DP8391 Manchester encoder and the DP8392 transceiver chip *(Fig. 3)*. A dc-dc converter and a transformer furnish galvanic isolation between the transceiver and controller sections.

As noted, the HD64180 processor, running at 9.2 MHz, has relatively little work to do. Once the SBIC and NIC are correctly programmed, the processor waits for interrupt calls from those two controller chips. But the processor does have two major tasks: managing the buffers and interpreting and executing the host commands sent through SCSI.[4]

A software schematic in the form of a data-flow diagram explains how the HD64180 performs these tasks. Assume that the host wants to send data to a network destination. The host issues a SCSI write command, waking up Process 1—called "SCSI" *(Fig. 4)*. This process sets up the DMA controller channel to download the data from the host into the Transmit Buffers area. When this transfer is finished, the host receives status information signaling the successful completion.

Process 1 then signals Process 2, "Ether," which adds the corresponding headers to the packet and transmits it. How much header information is added depends on the number of protocol layers implemented. Normally, the data link addresses (source and destination) are pulled from the Address/Protocol Tables and incorporated in the packet. Also, the corresponding protocol identification is added to the Ethernet Type field for recognition by the receiving counterpart. Similarly, TCP and upper layer headers can be added to the packet.

When the packet is assembled and checked, the processor sends the NIC a set of pointers indicating where the packet is stored and asks the controller to send it. Ether then goes to sleep until the transmission is completed and an interrupt generated by the NIC reawakens the process. Depending on the protocol implemented, the packet just sent is either discarded or saved for a Receipt Acknowledge by the receiving end. Either way, the SCSI status sense area is updated to show success or failure.

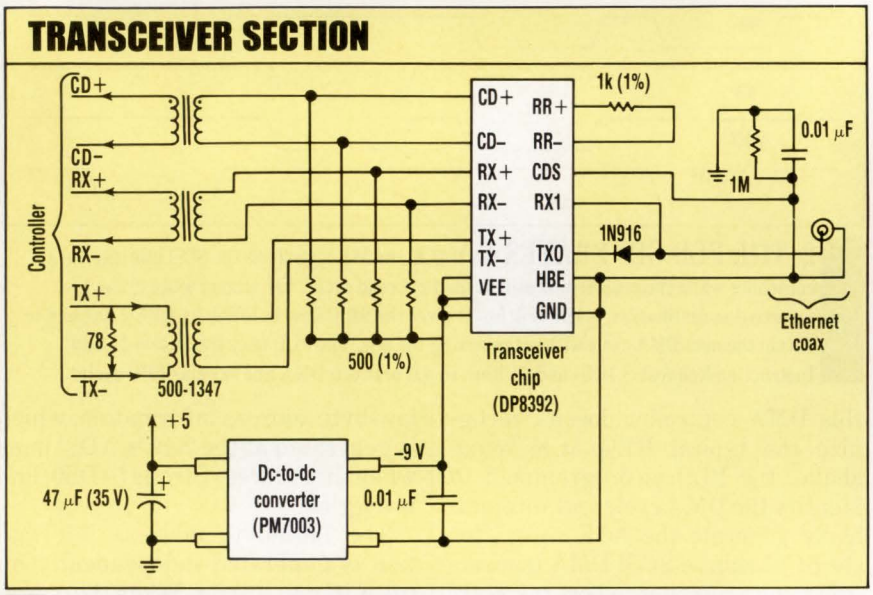
The transmit and receive buffers are organized as logical rings. Pointers are moved around by the processor and NIC after each transaction is concluded.

When it receives a multicast packet, the processor analyzes the packet's address and checks for a match with its own table of multicast addresses. This software check is needed because the NIC multicast filter matches only the hashing code. If higher level protocols are implemented, the processor must make sure other headers within the received packets have a proper destination and an outstanding read request from the host.

The operations noted, including the SCSI bus protocol, typically take about 1 to 2 ms per transaction. To this the designer adds the time the data takes to move between the host and controller (at up to 1.4 Mbytes/s, depending on how fast the host responds). This overhead determines how much network traffic can be supported. It also limits the number of higher level protocols that can be incorporated in the controller. Of course, this limit also depends on how much computing power the host has.

The SCSI standard doesn't include specific commands for communication controllers. When the host computer boots up, it usually sends an Inquiry command to all possible SCSI addresses to find out who is on the line. The Ethernet controller responds—and will continue to until the SCSI standard recognizes a specific category—with a "vendor unique" code, 80 hex and up. After that, only the mandatory commands need be followed and supported.

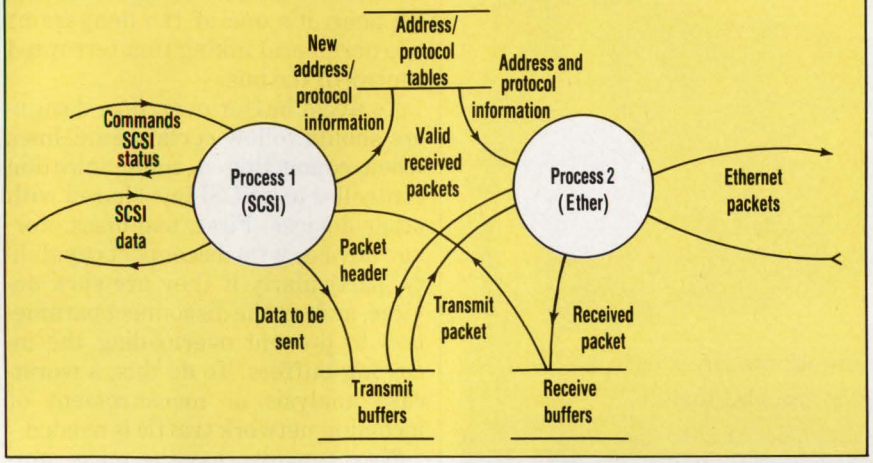
For instance, the basic read and



3. THE TRANSCEIVER STAGE needs only one IC. The entire controller-transceiver fits on a 6-by-4.5-in. circuit board.

ETHERNET CONTROLLER

DATA FLOW DIAGRAM



4. THE SOFTWARE'S top-level data-flow diagram includes two processes that handle SCSI and Ethernet requests. Interrupt signals from the respective controller chips activate the processes.

write commands work the same as in any other SCSI device, though some bit fields are added to accommodate special conditions. In one common operation, for example, the host reads the packet header before deciding what to do with the received data. As a result, the basic read command includes a "keep" bit that lets the host read part of a packet without throwing the rest away. The "offset" field points to the first byte of data to be read after the headers have been stripped.

The write command includes a bit that signals the host to add the packet header (Hdr) and a "no write" bit (NoW) that tells it to load the packet in the buffer but do not send it. Only LUN 0 is valid for the write command; for the read command, LUN 0 is invalid. Logical destination addresses are correlated with physical addresses by the controller Tables.

The control commands are implemented as a SCSI mode select. Several page descriptors place the controller on-line or off-line, download higher-layer protocol information, and define other SCSI-related parameters. The SCSI format command downloads Ethernet multicast and physical addresses and higher level CPU addresses. These commands can also be mode select descriptors. The mode sense command and the traditional SCSI check sense command convey status information.

An important consideration in designing an Ethernet controller for the SCSI is the bus's bandwidth. In its slower, asynchronous mode, SCSI handles transactions only 20% faster than Ethernet's 10 Mbits/s. But since average Ethernet traffic to and from a particular node is not that high, adequate buffering on the controller keeps traffic on the SCSI bus at reasonably low levels. As a result, users can simultaneously run other peripherals on the SCSI bus.

Connecting certain devices to the bus, however, creates a problem. The reason is that once a transaction on the SCSI bus has started, there is no graceful way of interrupting it until either it's finished or the target decides to disconnect. So if a "dumb" disk drive—one that doesn't offer disconnect—is sitting on the SCSI bus trying to access some physical sector, the bus could be easily tied up for 40 ms or more. That 40 ms represents about 50 kbyte's worth of Ethernet packets, assuming they come

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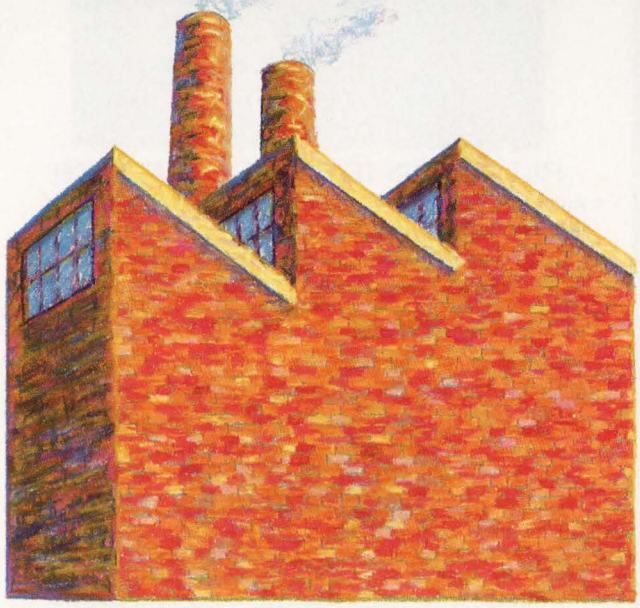

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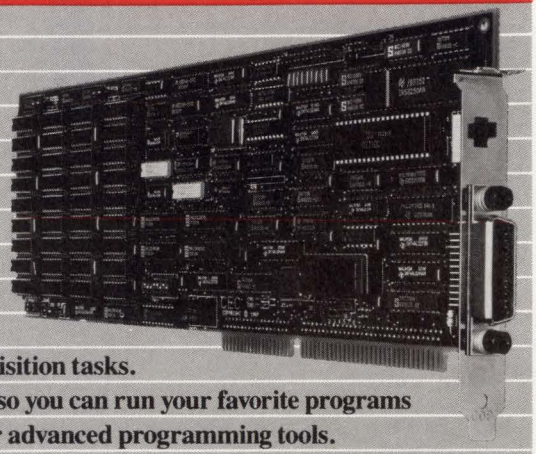

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ETHERNET CONTROLLER

one after the other, and the controller's buffers would overflow. Although such an overflow seldom happens, it's one of the dangers of one peripheral taking uninterrupted control of the bus.

To avoid buffer overruns, designers should follow certain guidelines when connecting a communication controller to a SCSI bus shared with other devices. First, use mass storage devices with disconnect capability, particularly if they are slow devices, and set the disconnect parameters to prevent overloading the incoming buffers. To do this, a worst-case analysis or measurement of incoming network traffic is needed.

Next, ensure that the mass storage device's usage time is below the Ethernet controller's maximum buffering capacity. This is easily done by limiting the number of consecutive blocks transferred between the host and mass storage devices in one SCSI transaction.

Finally, designers should give the controller's SCSI address a higher priority than other peripherals with no direct latency problems. Usually, mass storage units can wait to be serviced without losing data, although some devices, such as streamer tapes, become inefficient.□

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1. ANSI, Small Computer System Interface (SCSI), X3.131-1986.
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Tomas Russ is the electrical engineering group leader at the Bates Linear Accelerator Center, within the Massachusetts Institute of Technology Laboratory for Nuclear Science. His group is responsible for the controls, instrumentation, and ac/dc power developments for the center's 1-GeV electron linear accelerator. Russ received his engineering degree from the University of Buenos Aires, Argentina.

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

FOR LAMBDA, CIRCLE 57 →

THE MATH BEHIND THE MIPS: DSP BASICS

THE SECRET TO DIGITAL SIGNAL PROCESSING IS REDUCING COMPLEX ANALOG FUNCTIONS—LIKE FILTERS—TO SIMPLE HIGH-SPEED COMPUTATIONS.

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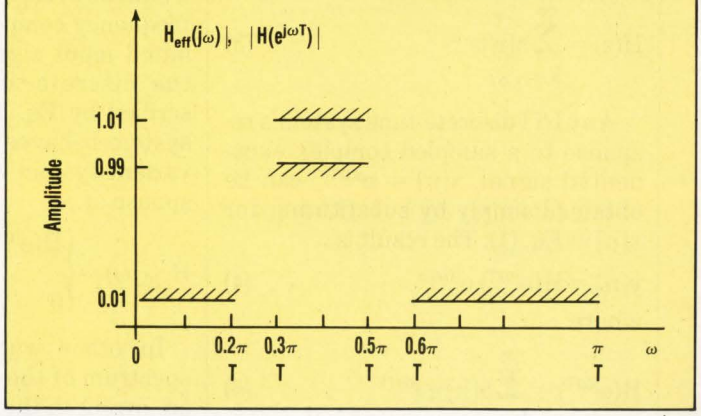
Digital signal processing is rapidly making the transition from the research lab to applications. In fact, almost any case in which an analog signal must be stored or manipulated is fair game for DSP. For all the glamour of ultrafast computation and programmability, digital signal processing techniques are based upon mathematical concepts that are familiar to most engineers. From these basic ideas spring the myriad applications of DSP, including fast Fourier transforms, linear prediction, nonlinear filtering, decimation and interpolation, and many more.

One of the most common signal-processing functions is linear filtering. High-pass, low-pass, and bandpass filters—traditionally analog designs—can all be constructed with DSP techniques. To build a linear filter with digital methods, a continuous-time input signal, $x_c(t)$, is sampled to produce a sequence of numbers, $x[n]=x_c(nT)$. This sequence is transformed by a discrete-time system—that is, a computational algorithm—into an output sequence of numbers, y[n]. Finally, a continuous-time output signal, $y_c(t)$, is reconstructed from the sequence y[n] *(see Fourier transforms, bandlimited signals, and sampling, p. 107).*

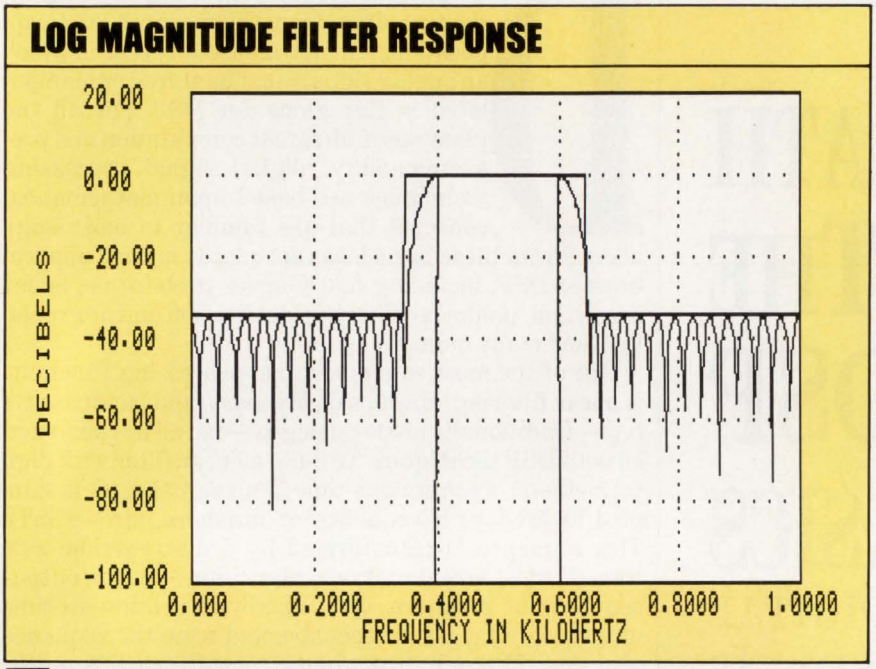
If the input signal is bandlimited so that the sampling frequency $\omega_s=2\pi/T$ is at least twice the highest frequency in the input spectrum, and if the discrete-time system is linear and time-invariant (LTI), then the overall system behaves as a linear time-invariant system. To change the overall system response, only the computational algorithm of the discrete-time system must be changed, so this approach to linear filtering is extremely flexible.

LTI discrete-time systems, as well as LTI continuous-time systems, obey the principle of superposition. Also, time-invariance implies that if the system's input is shifted in time, the output is correspondingly shifted. It follows that the inputs and outputs of all LTI discrete-time systems are related by the convolution sum expression:

SPECIFICATIONS FOR A BANDPASS FILTER



1. THE SPECIFICATIONS for a bandpass filter are for zero gain in the stopbands and unity gain in the passband, with a maximum approximation error of .01.



2. THE BANDPASS FILTER can be constructed from an elliptical infinite-impulse-response filter.

$$y[n] = \sum_{k=-\infty}^{\infty} h[k]x[n-k] \quad (1)$$

where the sequence h[n] is the system's impulse response—that is, the response of the discrete-time system to the unit impulse input sequence:

$$\delta[n] = \begin{cases} 1 & n = 0 \\ 0 & n \neq 0 \end{cases} \quad (2)$$

Another characterization of an LTI discrete-time system is its system function, H(z), the z-transform of the impulse response:

$$H(z) = \sum_{k=-\infty}^{\infty} h[n]z^{-n} \quad (3)$$

Any LTI discrete-time system's response to a sampled complex exponential signal, $x[n] = e^{j\omega Tn}$, can be obtained simply by substituting for x[n] in Eq. (1). The result is

$$y[n] = H(e^{j\omega T})\, e^{j\omega Tn}, \quad (4)$$

where

$$H(e^{j\omega T}) = \sum_{k=-\infty}^{\infty} h[k]\, e^{-j\omega Tk} \quad (5)$$

is the system's frequency response. Comparing Equations (3) and (5) shows that the frequency response equals the system function evaluated for values of z on the unit circle of the z-plane, that is, for $z=e^{j\omega T}$.

If the input signal is bandlimited so that the sampling frequency $2\pi/T$ is at least twice the highest frequency in the input spectrum, then the Fourier transform of the sequence x[n] is periodic in ω with period $2\pi/T$. Each period is an exact copy of the bandlimited Fourier transform of the input signal, $x_c(t)$. Also, from Eq. 5 it's clear that $H(e^{j\omega T})$ is periodic in ω with period $2\pi T$. Consequently, if a discrete-time system is LTI, with a frequency response of $H(e^{j\omega T})$, each frequency component of the bandlimited input signal is processed by the discrete-time system as described by Eq. 4. Thus, the overall system behaves as a linear time-invariant system with a frequency response of:

$$H_{eff}(j\omega) = \begin{cases} H(e^{j\omega T}) & [\omega] < \pi/T \\ 0 & [\omega] > \pi/T \end{cases} \quad (6)$$

In other words, the frequency spectrum of the output is bandlimited, owing to the reconstruction system, and is shaped in the band $|\omega| < \pi/T$ by the frequency response of the discrete-time system. The frequency response of the discrete-time system thus determines the system's overall frequency response.

In an important class of continuous-time systems—including RLC circuits and RC-active filters—the input and output satisfy a linear differential equation with constant coefficients. The corresponding system function is therefore a rational function of the Laplace transform complex frequency variable *s*. Practically realizable LTI discrete-time systems also have rational system functions of the form:

$$H(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{1 + \sum_{k=1}^{N} a_k z^{-k}} \quad (7)$$

The input and output satisfy linear difference equations with constant coefficients:

$$y[n] = -\sum_{k=1}^{N} a_k y[n-k] + \sum_{k=0}^{M} b_k x[n-k] \quad (8)$$

By using Eq. 8 as a recurrence formula, the output can be computed from the input and previously computed output values.

IIR AND FIR SYSTEMS

Discrete-time LTI systems are often classified according to the length of their impulse-response sequences. Finite-impulse-response (FIR) systems have finite-length impulse responses, and infinite-impulse-response (IIR) systems have infinite-length impulse responses. Although the rational function in Eq. 7 is the most general form for an LTI system function, FIR systems have system functions of the special form:

$$H(z) = \sum_{k=0}^{M} b_k z^{-k} \quad (9)$$

that is, the denominator in Eq. 7 is unity (all the a_k's are zero). The difference equation for a direct form realization of an FIR system also results from setting all the a_k's in Eq. 8

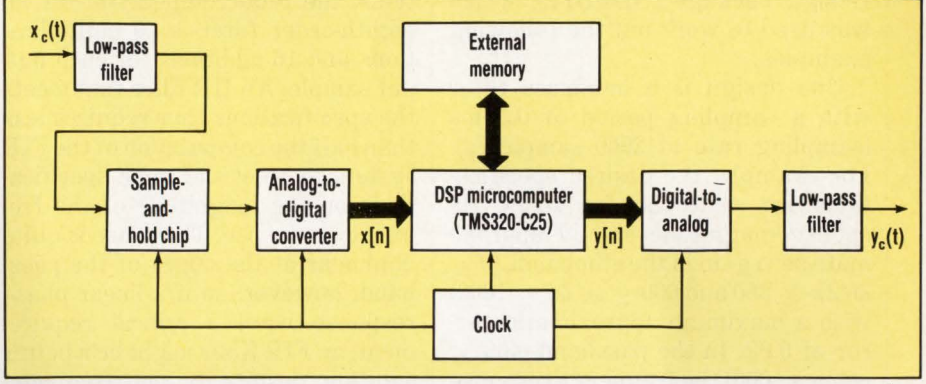
to zero. In this case, the impulse response of the system is:

$$h[n] = \begin{cases} b_n & 0 \le n \le M \\ 0 & \text{otherwise} \end{cases} \quad (10)$$

FIR systems are always stable, and if the impulse response satisfies the symmetry condition h[n]=h[M-n], the phase is exactly linear, corresponding to a delay of M/2 samples at all frequencies. An FIR filter's linear phase is often an attractive design feature. However, an FIR system may require more computation than an IIR system to achieve a given desired response.

If the denominator of the system function in Eq. 7 is not unity, meaning that some of the a_k's are nonzero, then the system has an infinite length impulse response. The reason for this is clear from Eq. 8, which shows that previous output samples are fed back to compute the next output sample. When an IIR system is excited by the impulse sequence of Eq. 2, the feedback paths in the system can potentially keep the output nonzero, even though the input returns to zero for $n > 0$. If the impulse response decays with time, the system is stable. Depending on the values of the feedback coefficients a_k, however, the input could also grow or oscillate without decaying. Realizable IIR systems can't have exactly linear phase, but they're often more efficient to implement than comparable FIR systems.

HARDWARE FOR REAL-TIME DSP SYSTEMS



3. CONSTRUCTING A DSP-based filter requires only converters, memory, and a clock, as well as the DSP microcomputer. The analog filters bandlimit the input and output signals.

Filter designers must first determine a set of specifications on the response of the discrete-time system. Next, they must obtain either the coefficients of a rational system function, as in Eq. 7, for an IIR system or the coefficients of a polynomial system function, as in Eq. 9, for the FIR case. To explore the trade-offs inherent in choosing a design structure, a

FOURIER TRANSFORMS, BANDLIMITED SIGNALS, AND SAMPLING

The relationship between continuous-time (analog) signals and discrete-time signals is most evident in Fourier transforms of the signals. The Fourier transform of a continuous-time signal $x_c(t)$ is defined as

$$X_c(\omega) = \int_{-\infty}^{\infty} x_c(t)e^{-j\omega t}\,dt$$

The Fourier transform describes the frequency content of the signal $x_c(t)$ in terms of complex exponential signals $e^{j\omega t}$. If $X_c(\omega) = 0$ for $|\omega| \ge \omega_N$, the signal is bandlimited and can be represented by periodic samples:

$$X(e^{j\omega T}) = \sum_{n=-\infty}^{\infty} x[n]e^{-j\omega Tn}$$

$$= \frac{1}{T}\sum_{k=-\infty}^{\infty} X_c\left(\omega + \left(\frac{2\pi k}{T}\right)\right)$$

where $x[n]=x_c(nT)$, $-\infty < n < i$ is a sequence of samples taken at intervals of T seconds; T is the sampling period; and $2\pi/T$ is the sampling frequency (in radians/s). A sample-and-hold circuit followed by an analog-to-digital converter approximate ideal sampling. The quantity:

$$X(e^{j\omega T}) = \sum_{n=-\infty}^{\infty} x[n]e^{-j\omega Tn}$$

is the Fourier transform of the discrete-time sequence x[n]. An idealized—bandlimited—Fourier transform is nonperiodic, while the individual terms in the right-hand sum of Eq. A are periodic.

Aliasing—the result of high frequencies taking on the identity of low frequencies, thereby creating confusion in the overlap region—occurs when $2\pi/T < 20_N$. When $2\pi/T > 20_N$, the Fourier transform is periodic, with each period a perfect replica of the bandlimited Fourier transform of the continuous-time signal. The original bandlimited signal can be recovered by constructing a continuous-time output of the form:

$$y_c(t) = \sum_{n=-\infty}^{\infty} x[n]h_r(t - nT)$$

To see this, note that the Fourier transform of $y_c(t)$ is

$$Y_c(\omega) = \sum_{n=-\infty}^{\infty} x[n]H_r(\omega)e^{-j\omega nT}$$

$$= H_r(\omega)X(e^{j\omega T})$$

Accordingly, if $H_r(\omega)$ is an ideal low-pass filter with gain T and cutoff frequency π/T, then $Y_c(\omega)=X_c(\omega)$, so $y_c(t)=x_c(t)$.

Such a signal as $y_c(t)$ could be the output of a system that emits a pulse of amplitude proportional to x[n] at each sample time nT. Ideally, the pulse shape is: $h_r = (\sin(\pi t/T)/(\pi t/T)$.

DSP DESIGN TECHNIQUES

flexible filter-design tool is essential. An example is ASPI's Digital Filter Design Package-2 (DFDP2), which was used to work out the following examples.

One design is a bandpass filter with a sampling period of 0.5 ms (sampling rate of 2000 samples/s). For example, the desired specifications are that the frequency response magnitude should approximate zero gain in the stopbands ($0 \leq \omega/2\pi \leq 350$ and $600 \leq \omega/2\pi \leq 1000$) with a maximum approximation error of 0.02. In the passband ($400 \leq \omega/2\pi \leq 600$) the frequency response magnitude should approximate unity gain with a maximum error of 0.02. Above $\omega/2\pi = 1000$, the overall system response will be zero, due to the output reconstruction filter.

An IIR design meeting the specifications could also be built *(Fig. 1)*. For frequency-selective filters such as bandpass filters, the most widely used approach is the method of bilinear transformation. In this method, a discrete-time filter is obtained by algebraic transformations of analog system functions resulting from the Butterworth, Chebyshev, or elliptic approximation methods. The design program determined that a 24th-order Butterworth, a 12th-order Chebyshev, or an 8th-order elliptic filter would meet the specifications.

Construct An FIR Filter

Standard techniques for FIR filter design are the window method and the Parks-McClellan method. In the window method, the impulse response of an ideal filter is truncated to produce a realizable FIR impulse response. The Parks-McClellan method produces optimum (in the minimum maximum-error sense) FIR approximations *(Fig. 2)*. According to the Parks-McClellan design module of DFDP2, the impulse response length needs to be $(M + 1) = 69$ to meet the design specifications. The delay of this system is exactly 34 samples, and constructing this filter with a direct form structure requires 69 multiplications and 68 additions to compute each output sample.

The elliptic filter requires the least computation. Since each second-order section in the cascade form requires 5 multiplications and 4 additions, the total computation for an eighth-order filter is 20 multiplications and 16 additions for each output sample. An IIR filter that meets the specifications thus requires less than half the computation of the FIR system to meet the same specifications on the magnitude of the frequency response. The phase is quite nonlinear at the edges of the passband, however, so if a linear phase response were a critical requirement, an FIR filter might be a better solution, despite its increased complexity. Also, counting multiplications and additions can be misleading.

System Hardware

After the filter coefficients have been obtained, the next step is constructing the filter. The necessary hardware consists of a DSP microcomputer, a sampling system, a signal-reconstruction system, a clock, and external memory *(Fig. 3)*. In this design, the microcomputer is a Texas Instruments TMS320C25, but many other possibilities exist, such as other chips in TI's TMS320 family, AT & T's WE-DSP-16, Motorola's 56000, and Analog Devices ADSP-2101. To prevent aliasing, the input signal is bandlimited by a low-pass filter. The input sequence x[n] is obtained from the sample-and-hold circuit followed by an analog-to-digital converter. The discrete-time system is a program running on the TMS320C25 that converts the input sequence into the output sequence. Finally, the continuous-time signal is reconstructed by a d-a converter, followed by a low-pass analog filter.

The sampling rate at the input and output of the filter system and the microcomputer arithmetic unit's speed constrain the complexity of the filtering algorithm. For real-time operation, each output sample must be computed within one sample period T. The total time required to get an input sample from the a-d converter, output a sample to the d-a converter, and compute a new sample of the output must be less than or equal to T. For this reason, it's important to use the minimum-order system possible.

In the case of the TMS320C25 microcomputer, the basic instruction cycle is 100 ns. If the sampling period is T, the total number of cycles available in one sample period is $T \times 10^7$. For a sampling period of 5×10^{-4}, 5000 cycles are available to compute each output sample.

Filter Code

The complete program for the FIR bandpass filter was generated automatically by the code-generation module of DFDP2. It involves a filter subroutine *(Fig. 4)* and six more instructions for looping, obtaining an input sample from the a-d converter, and sending an output sample to the d-a converter. Eleven more instructions initialize the filter coefficient memory; 69 memory locations store the filter coefficients; and 68 locations store the delayed values of the input signal. The program, impulse response coefficients, and delay memory reside in the microcomputer's internal RAM for fast operation.

In the filtering subroutine, the filter coefficients are stored in the data memory, and the delayed input values are stored in program memory. Consequently, instead of testing and branching to create a loop, the instruction RPTK 68 causes the next instruction, MACD FDATA + > FD00, *-, to be executed 68 times. As a result of that instruction, a data memory value (specified by the address FDATA+>FD00) is multiplied by a program memory value (specified by the indirect address *-); the previously computed product is added to the 32-bit accumulator; and the indirect address register is decremented. The other subroutine instructions set up for the multiply/accumulate operation that is the essence of the FIR filter. The two instructions RPTK 44 and MACD FDATA+>FD00,*- require a total of 71 cycles if both the filter coefficients and delay memory are in the on-chip RAM. The total number of cycles required to execute the subroutine is 84. This, added to the 12 cycles for a-d and d-a converters, gives a total of 9600 ns. Since the

DSP DESIGN TECHNIQUES

TMS320 DIGITAL FILTER PROGRAM

```
DELAR     EQU     1              *DELAY AR REGISTER
*
FILTER
          LARP    DELAR          *POINT TO THE DELAY INDEX REGISTER
          LRLK    DELAR,Z000     *INDEX POINTS TO Z-0 (INPUT)
          LAC     VSAMPL,15      *GET & SCALE INPUT
          SACH    *              *SAVE SCALED INPUT

          MPYK    0              *P = 0
          ZAC                    *AC = 0
          LRLK    DELAR,ZLAST    *INDEX POINTS TO Z-N
          RPTK    68
          MACD    FDATA+>FD00,*- *MULTIPLY, ACCUM. and DELAY
          APAC                   *FORM RESULT
          SACH    VSAMPL,0       *SAVE OUTPUT
          RET                    *RETURN
*
          PEND
          END
```

4. THE CORE OF THE filtering program is a short segment of code. The key instruction is MACD FDATA + > FD00,*-, which performs the multiply, accumulate, and delay operations.

sampling period was 10^{-4} s, the bandpass filter requires only 1.9% of the microcomputer's computational power.

The automatic code-generation module of DFDP2 was also used to obtain an implementation of the elliptic IIR filter that meets the specifications. In this case, the number of memory registers for coefficients is 20, and the number of delay registers is 8, only about one-fifth the number required for the FIR filter. Surprisingly, the IIR system doesn't enjoy a similiar advantage in speed. Whereas 84 cycles were required to implement the 69 multiplies and 68 adds of the FIR filter, 73 cycles are required to implement the 20 multiplies and 16 adds of the IIR filter. Thus the total time to compute one output sample is 9.6 μs for the FIR filter and 8.5 μs for the IIR filter.□

Ronald W. Schafer is Regents' Professor and John O. McCarty/Audichron Chair Professor of Electrical Engineering at the Georgia Institute of Technology. He has done research in many areas of digital signal processing and is coauthor of three textbooks on the subject. Schafer is a founder of Atlanta Signal Processors Inc., a company that supplies design tools for DSP applications.

FOR MORE INFORMATION

The following books furnish more detailed information on the topics discussed in this article and on digital signal processing in general:

Lin, K-S. *Digital Signal Processing Applications with the TMS320 Family*, Vol. I. Englewood Cliffs, NJ: Prentice-Hall, 1987.

Oppenheim, A.V. and Schafer, R.W. *Digital Signal Processing.* Englewood Cliffs, NJ: Prentice-Hall, 1975.

Oppenheim, A.V. and Schafer, R.W. *Discrete-Time Signal Processing.* Englewood Cliffs, NJ: Prentice-Hall, 1989.

Oppenheim, A.V. and Willsky, A.S. *Signals and Systems.* Englewood Cliffs, NJ: Prentice-Hall, 1983.

Parks, T.W. and Burrus, C.S. Digital Filter Design. New York: John Wiley & Sons, 1987.

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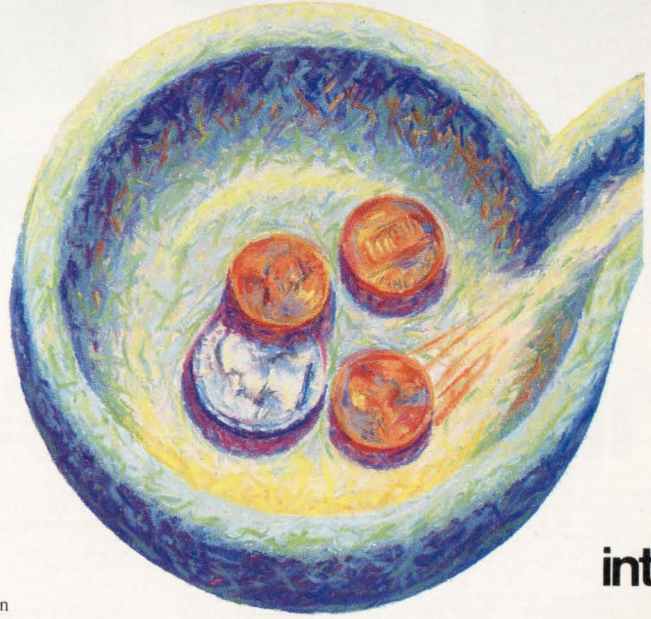

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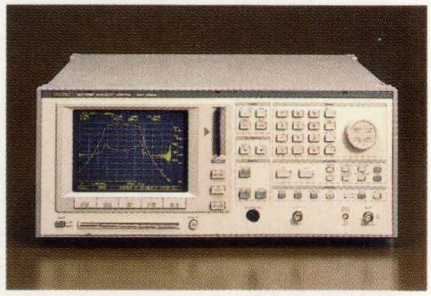

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CIRCLE 44

CIRCLE 521

GET START-AND-RUN VOLTAGES FOR MOTORS

CARL SPEAROW
Sundstrand Corp., 4747 Harrison Ave., Rockford, IL 61125; (815) 394-3263.

Here's a timed two-voltage circuit that can start and run a small dc motor or solenoid. The circuit is simpler than a previously published circuit that performs the same function—it uses one regulator instead of two and fewer other functions (ELECTRONIC DESIGN, April 28, p. 122). The input voltage to the LM317 three-terminal regulator ranges from 5 to 40 V, and the output voltage can range from 2 to 36 V *(see the figure)*.

With an input voltage (V_{in}) initially applied to the input, and the capacitor C_1 in a discharged state, the LM393 comparator's open-collector output circuit is open circuited. Then, the higher start-up output voltage is

$$V_{out1} = 1.25[1 + (R_3/240)]$$

At a time t after start-up, when

$$t = -R_1C_1Ln[R_4/(R_4 + R_5)]$$

or

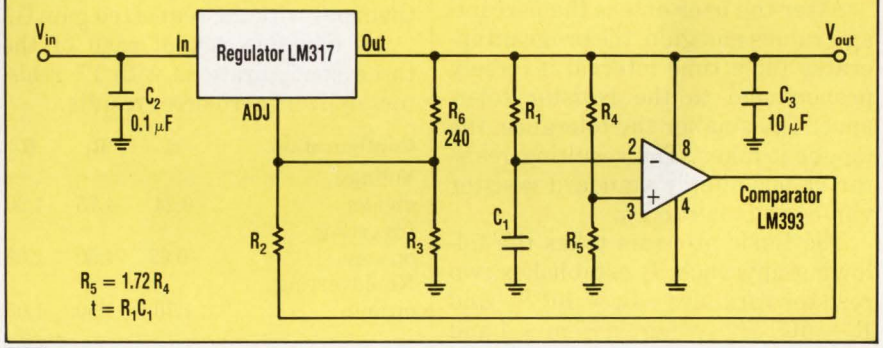
$$t = R_1C_1, \text{ if } R_5 = 1.72R_4$$

the comparator output goes low. At that time, the output voltage switches to a lower value

$$V_{out2} = 1.25\{1 + [R_2R_3/240(R_2 + R_3)]\}$$

for running the device at its proper operating level.□

START AND RUN POWER SOURCE



IN THIS TIMED, two-voltage circuit, the input voltage can range from about 5 to 40 V, and the output voltage can range from about 2 to 36 V at 1.5 A. The circuit is useful for starting dc motors or solenoids. In these applications, one voltage is required to start the device; a different voltage is required to run it.

CIRCLE 522

STANDARD RESISTORS GIVE ACCURATE RATIOS

ROBERT BOYD
Hughes Aircraft Co., 1901 Malvern St., Fullerton, CA 92634; (714) 732-8058.

A simple program written in standard Basic quickly calculates feedback resistors to get accurate gain values for inverting and noninverting op amps and resistors *(see the program listing)*. It also gets accurate ratios for voltage dividers, when using standard resistor values. In fact, a table of resistor ratios was calculated with this program (ELECTRONIC DESIGN, May 12, p. 154). With no restrictions on the number of decimal places in gain between the limits, the program supplies the most accurate resistor value combinations for the following configurations:

Configuration	Gain (G)	Limits for G (volt/volt)
Voltage divider	$1/(1+R_1/R_2)$	0.01 to 0.99
Inverting op-amp	$-R_2/R_1$	−100 to −0.01
Noninverting op-amp	$1+R_2/R_1$	1 to 100

In operation, the program begins by asking the user for the percent tolerance of the resistors to be

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PROGRAM LISTING

```
10 REM Accurate gain ratios – dividers/op-amps
20 F5=0:REM Swap R1 & R2 if F5=1
30 DEF FNA(X)=.01*INT(X*100+.5)
40 DEF FNB(X)=.1*INT(X*10+.5)
50 DEF FNC(X)=INT(X+.5)
60 REM Roundoff routines
70 INPUT "2, 1, or 0.5% ";B
80 INPUT "Gain ? ";G
90 IF G=-1 THEN R1=1:R2=1:GOTO 350
100 IF G=1 THEN R1=1:R2=0:GOTO 350
110 IF G<0 THEN A=-1/G:GOTO 150
120 IF G<1 THEN A=1/G-1:GOTO 150
130 IF G<2 THEN A=1/(G-1):GOTO 150
140 A=G-1:F5=1
150 B=96/B
160 REM B=No. of discrete resistor values, 48, 96 or 192
170 E=B
180 REM Initialize error E
190 IF A<1 THEN A=1/A:F5=1
200 L=FNC(B*LOG10(A))
210 FOR M=1 TO B
220 N=L+M-1
230 R8=10^(N/B)
240 REM R8 = trial value of R1
250 IF N<=B THEN R8 = FNA (R8)
260 IF N>B AND N<=2*B THEN R8=FNB(R8)
270 IF N>2*B THEN R8=FNC(R8)
280 REM Insures just 3 significant figures
290 R9=FNA(10^((M-1)/B)):E1=ABS(R8/R9-A)
300 REM R9 = trial value of R2
310 IF E1<E THEN E=E1:R1=R8:R2=R9
320 REM Find smallest error E
330 NEXT M
340 IF F5=1 THEN S=R1:R1=R2:R2=S
350 PRINT G; R1;R2
360 END
```

used—2%, 1%, or 0.5%—with the 0.5% tolerance supplying the same accuracy as 0.1% resistors would. Next, the program asks for the gain G in volt/volt. The requested gain determines the program branching to one of the three circuit configurations:

Gain	Branches to
$G < 0$	Inverting op-amp
$0 < G < 1$	Voltage divider
$G > 1$	Non-inverting op-amp

After the user enters the percentage values and gain, the program operates for a time interval inversely proportional to the resistor tolerance: The smaller the tolerance, the longer it takes. The resulting resistor values supply standard resistor values and tolerances.

The Basic program takes the following approach: It establishes two resistor variables—$R_x = 10^{(n-1)/B}$ and $R_y = 10^{(m-1)/B}$—where $n > m > 1$ and $B = 48$ for 2%, 96 for 1%, and 192 for 0.5% tolerance. Then, where $A = R_x/R_y$, $B \bullet \text{Log } A = n - m$. Because the standard resistor values require that n and m must be integers, the result difference—INT(n-m) = N – M—only approximately equals B•Log A.

Accordingly, the program calculates discrete trial values of R_1 and R_2 for integer M and N values during iterations of M from 1 to B. Using these trial values of R_1 and R_2, the program makes a comparison of their ratio R_1/R_2 with the ideal continuous ratio A. The program saves the trial values of R_1/R_2 that minimize the error $(R_1/R_2) - A$ and prints them out with the requested gain G.

An example run of each of the three configurations with 1% resistors delivers zero-error results.

Configuration	G	R_1	R_2
Voltage divider	0.24	4.75	1.50
Inverting op amp	–0.68	1.50	1.02
Noninverting op amp	1.70	1.50	1.05

Of course, the user must supply the appropriate decade value for each resistor, such as 475Ω, 4.75k, or 475k, in the actual circuit.□

CIRCLE 523

MEASURE BREATHING RATE WITH SENSOR

RICARDO JIMENEZ-GARCIA
Mexicali Technological Institute, 233 Paulin Ave., Box 7953, Calexico, CA 92231; (619) 357-0974.

To a seriously injured patient or one undergoing surgery, respiratory rate is critical to immediate survival. With a $12 respiratory sensor placed under an oxygen mask, medical workers can monitor respirations per minute on a liquid crystal display. An audible tone warns of respiratory failure *(see the figure)*.

The sensor is a circuit that detects air pressure. Because the pressure of expired air is higher than that of inhaled air, the sensor, placed in the airway at the bottom of an oxygen mask, can monitor the patient's respiratory flow. The circuit then converts these air-pressure signals to respirations-per-minute readings.

Edmund Scientific sells the device, an ultrasensitive 0.004-psi air-pressure switch (Catalog No. E36,839). Single-pole, normally open switch contacts on the sensor are rated to handle 20 mA. The sensor's input port accepts 1/8-in. inside-diameter tubing (Catalog No. E35,918), which connects to the airway in the oxygen mask.

A 7555 timer IC1, configured as a monostable multivibrator, gives a 0.1-s positive, square output pulse each time a monitored person exhales and the sensor switch closes. This positive pulse enables timer IC2, a 5-kHz oscillator that drives a piezoelectric buzzer, to produce an audible tone for every pulse received. The positive pulse also triggers flip-flop IC4 to change its state for every pulse received.

The Q output signals from IC4 turn on AND gate IC7d to pass bursts of crystal-controlled 100-Hz signals from the MM5369EST oscillator chip IC5. The output of IC7d feeds to a 12-stage binary counter IC9, a CD4040. Since the maximum period of the low-frequency signal is 6 s, the circuit must use 10 bits of the counter to count to 600 (2^{10} equals

PROGRAM FOR THE EPROM

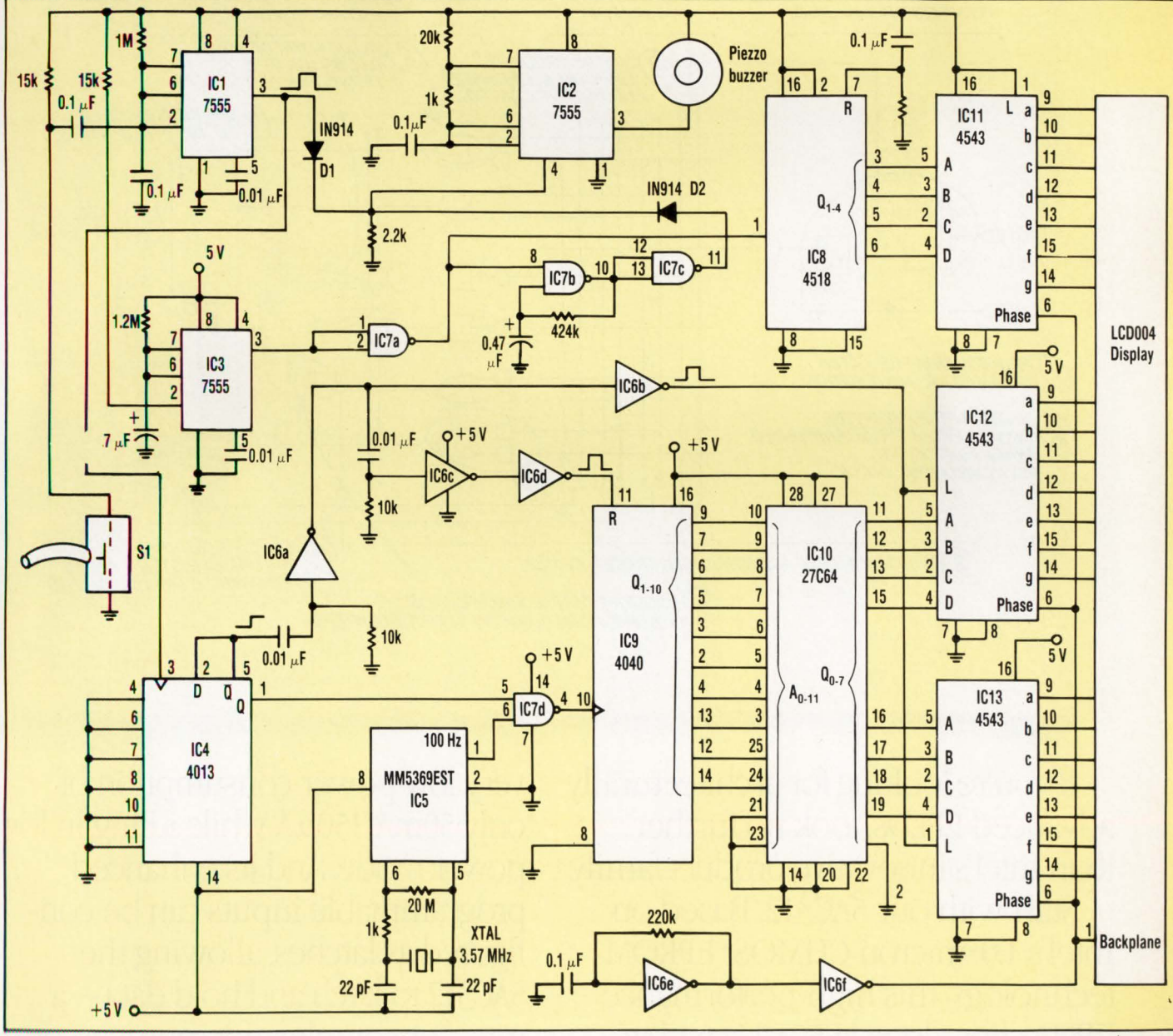
Hexadecimal Address	Hexadecimal Data	Hexadecimal Address	Hexadecimal Data
4B	80	80	47
4C	79	81	47
4D	78	82	46
4E	77	83	46
4F	76	84	46
50	75	85	45
51	74	86	45
52	73	87	45
53	72	88	44
54	72	88	44
55	71	8A	44
56	70	8B	44
57	69	8C	43
58	68	8D	43
59	68	8E	43
5A	67	8F	42
5B	66	90	42
5C	65	91	42
5D	65	92	41
5E	64	93	41
5F	63	94	41
60	63	95	41
61	62	96	40
62	61	97-9A	39
63	61	9B-9E	38
64	60	9F-A2	37
65	60	A3-A7	36
66	59	A8-AB	35
67	58	AC-B0	34
68	58	B1-B5	33
69	57	B6-BB	32
6A	57	BC-C1	31
6B	56	C2-C7	30
6C	56	C8-CE	29
6D	55	CF-D6	28
6E	55	D7-DA	27
6F	54	DB-DC	06
70	54	DD-F0	25
71	53	F1-FA	24
72	53	FB-104	23
73	52	105-110	22
74	52	111-11D	21
75	52	11E-12C	20
76	51	12D-13B	19
77	51	13C-14D	18
78	50	14E-160	17
79	50	161-177	16
7A	49	178-190	15
7B	49	191-1AC	14
7C	49	1AD-1CD	13
7D	48	1CF-1F4	12
7E	48	1F5-221	11
7F	48	222-258	10

1024, and 2^9 is merely 512). For a period between two respiratory signals of 6 s, IC9 would record the number 600 (six bursts of 100 each) in binary code.

Accordingly, for 20 respirations per minute, the interval between consecutive pulses is 3 s, and IC9 will register the number 300 in binary code. To display the number 20 on the LCD, the circuit must convert the binary number 300 into the decimal number 20. The circuit does the conversion with a translation table programmed into a 27C64 EPROM (IC10) that relates the IC9 count to respirations/min *(see the table)*. The information stored in the EPROM is in hexadecimal code, ranging from values of 10 to 80.

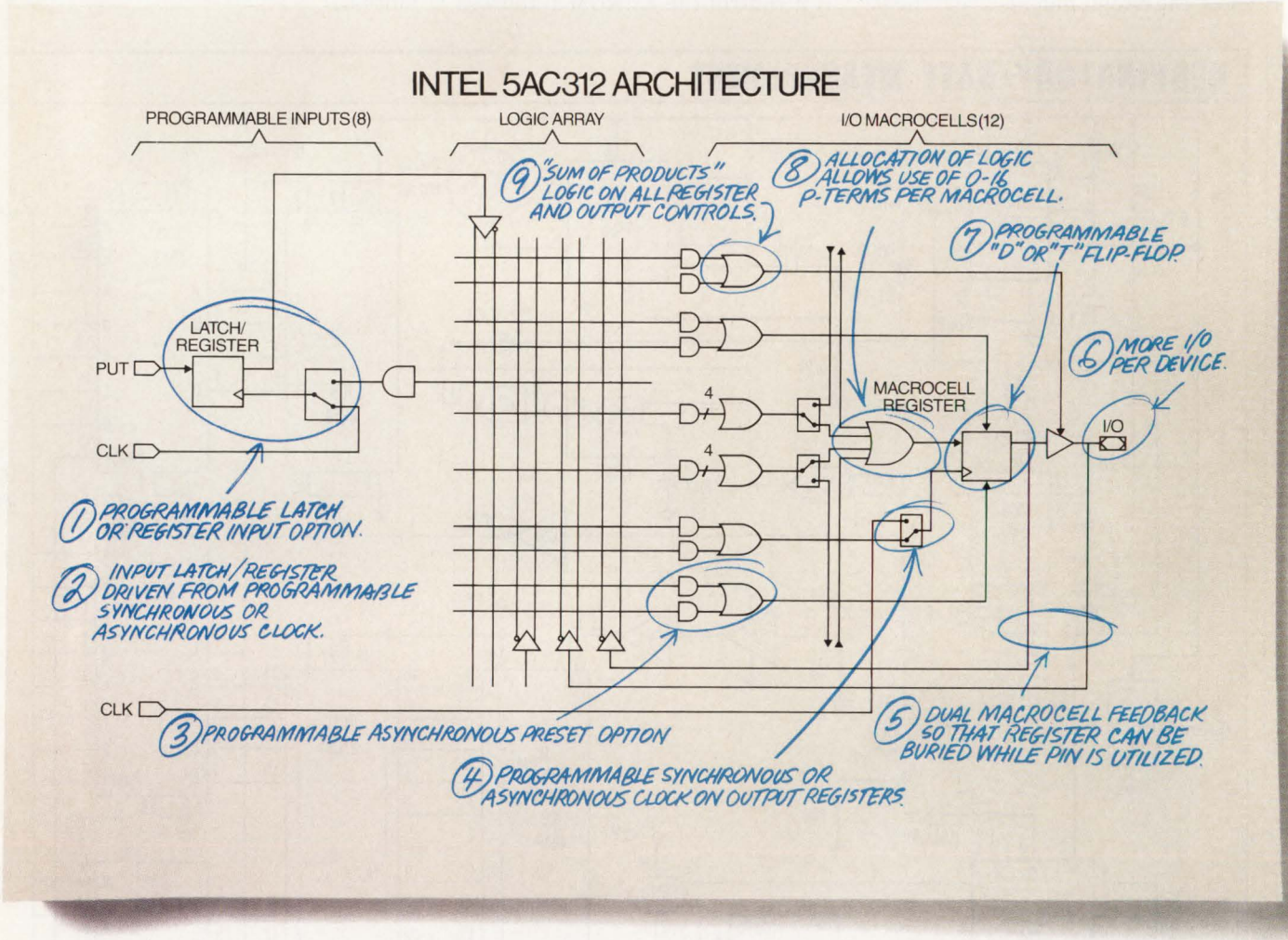
The 10 bits of the binary counter IC9 control the EPROM's address. The 4543 decoders are latched by the inverters IC6a and IC6b. This EPROM drives two 4543 BCD-to-seven-segment decoder-drivers, IC12 and IC13, which, in turn, drive the units and tens making up the two lower digits in the LCD display. The upper LCD digit shows the number of times (respiratory failures) the patient doesn't exhale for 6 seconds or more.□

RESPIRATORY-RATE MEASUREMENT



AN AIR-PRESSURE SENSOR placed in the airway at the bottom of an oxygen mask detects respiratory flow. A circuit within the sensor converts the signals to respirations-per-minute readings on an LCD and a tone that warns of respiratory failure.

9 REASONS TO CHOOSE INTEL FOR YOUR EPLD DESIGN.



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AND 12 MORE.

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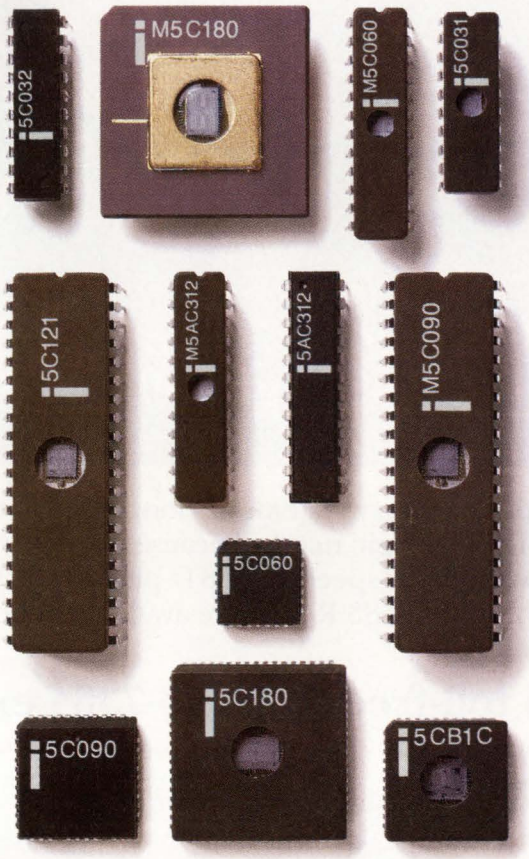

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CIRCLE 45

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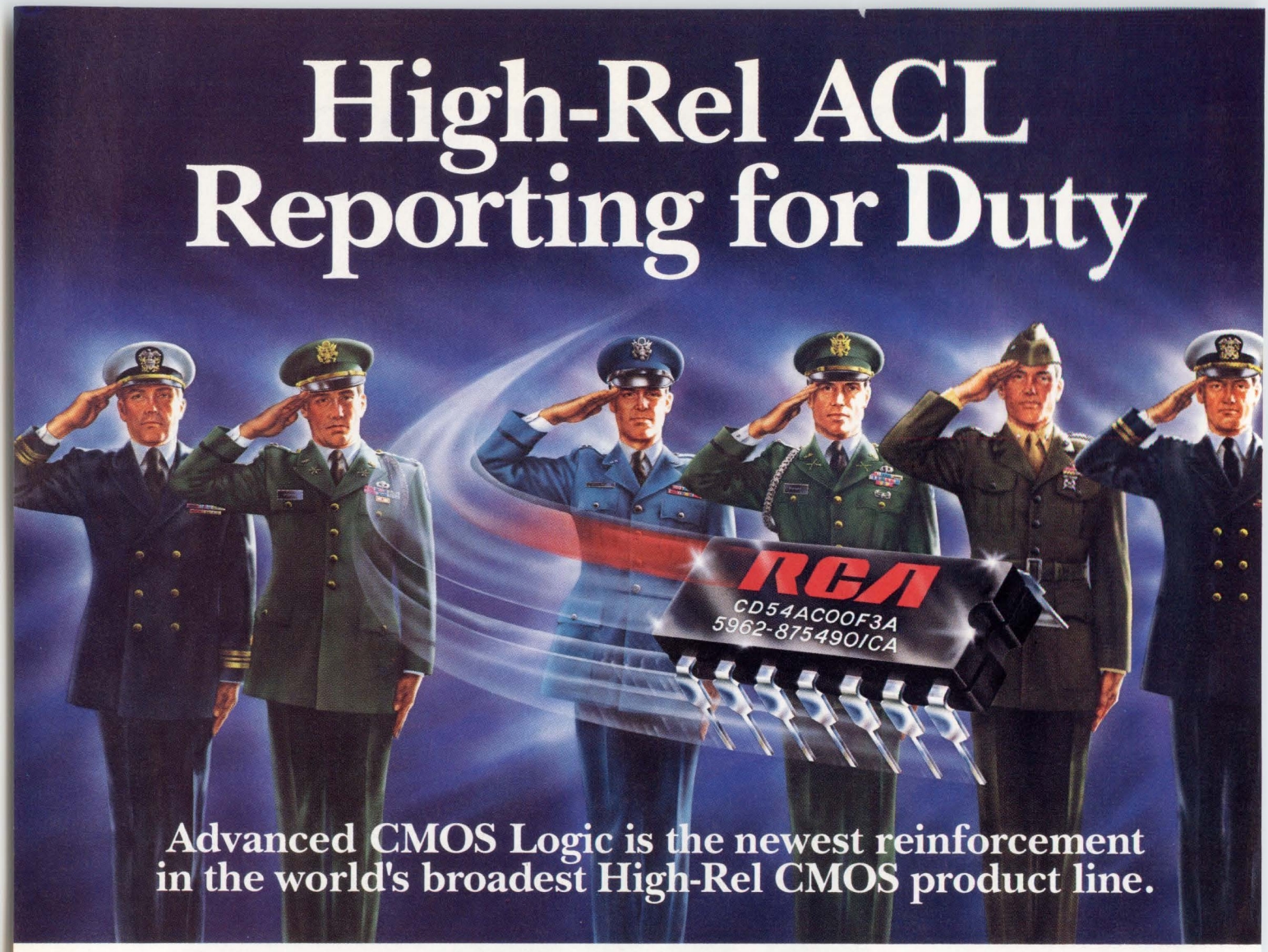

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Two 3- to 8- Line Decoder Demultiplexers*	Two Octal Buffer Line Driver 3-State*	One Octal D-Type Flip-Flop 3-State*
	Two Octal BUS Transceiver 3-State*	One Octal Transparent Latch 3-State(Inverting)
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*Standard Military Drawings available

† FAST is a trademark of National Semiconductor Corp.

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FAST EDC CIRCUIT SEALS MEMORY INTEGRITY

With the Am29C660 error detection and correction circuit, from Sunnyvale, Calif.-based Advanced Micro Devices, memory errors that corrupt dynamic RAM can now be detected at speeds 36% faster than other solutions in volume production. Then, the part corrects the errors 20% faster and with 32% lower power consumption than competitive circuits. The high-speed CMOS device detects all single-, double-, and some triple-bit errors in each word in memory. The circuit rapidly corrects all single-bit errors, including hard errors caused by permanent physical device failure. In addition, by using a modified Hamming-code algorithm and generated check bits, it corrects soft, transient errors. The highest-performance version has a 16-ns maximum delay for error detection and a 24-ns delay for error correction. The part comes in a 68-pin plastic leaded chip carrier for $60, and in a pin-grid array package for $63. Both prices are for quantities of 100.DM **CIRCLE 301**

ALDEC TEAMS WITH ACCEL; ENHANCES SUSIE SIMULATOR

Newbury-Park, Calif.-based Aldec Co.—developer of the Susie logic simulator—signed an OEM agreement with Accel Technologies, of San Diego. Effective immediately, Accel will resell the Susie simulator, which is compatible with the company's Tango schematic-capture package. This joint effort will yield a fully interactive, PC-based, design entry and verification environment for engineers. Based on an incremental compiler, the Susie simulator was upgraded to automatically identify all design timing problems. To save time, a design can be partitioned on-the-fly and any section with a known problem can be independently simulated. Aldec also released a PLD library for Susie that includes parts from AMD, Cypress, Intel, Lattice, and others. When teamed with the PLD library, Susie performs board-level simulations with PLDs working in concert with microprocessors, memories, and glue logic.BM **CIRCLE 302**

ANALOG-INPUT BOARD HITS 50-KHz THROUGHPUT

Reaching a price-performance milestone, Data Translation's DT2824 analog input and digital-I/O board for the IBM PC AT packs 50-kHz throughput, a RAM channel-gain list that permits scans of any channel sequence at any available gain, and 16 lines of digital I/O—all for $995. Thanks to the Marlboro, Mass., company's continuous-performance architecture, the board assures gap-free data transfers to system memory by combining dual-DMA-channel support, interrupts, and a selective error-flagging system. Because the board is software-compatible with the company's DT2821 series of boards, it already has an extensive subroutine library to draw from, as well as application-software support. The DT2824 is available for five-day delivery.DM **CIRCLE 303**

USERS PROGRAM DIE SIZE WITH MIXED ARRAY

Representing a major breakthrough in semicustom design, the Delta Series flexible linear array from Exar Corp., of San Jose, Calif., features programmable die size and programmable multifunction components for analog, mixed a-d, and pure-digital design. The result: a semicustom approach that can match the densities, silicon efficiency, and low per-unit cost of custom approaches. Not only that, the series retains the traditional semicustom benefits of quick turnaround, low non-recurring-engineering costs, and high design flexibility. The series is built with a 1-GHz, 3-μm design-rule process and consists of two arrays for different component counts. The Delta 2000 and 4000 pack up to 1310 and 4900 components each. Typical NRE charges range from $20,000 to $25,000, with a turnaround of 3 to 8 weeks. In high volumes, smaller arrays will be under $1.DM **CIRCLE 304**

11-BIT DIGITIZER HITS 1.35 GSAMPLES/S

Capturing high-speed waveforms accurately just got easier with the introduction of the 6880B/6010 waveform-digitizing system from LeCroy Corp., of Chestnut Ridge, N.Y. Combining a 1.35-Gsample/s sampling rate with an unprecedented 11 bits of single-shot resolution, the system features a 500-MHz bandwidth and a 10,000-point waveform memory. Running at full speed, the system records transient waveforms with an accuracy of 9.6 effective bits. For repetitive waveforms, averaging techniques increase the resolution to 14 bits.BM **CIRCLE 305**

VT100 TERMINAL RECEIVES GREYSCALE PICTURES

A VT100-compatible terminal from Image Data Corp., of San Antonio, Texas, receives high-quality greyscale video images from a computer database. The ImageTerminal displays the equivalent of an 8-by-10-in. glossy photograph. Users can store pictures together with text, so a hospital database, for instance, could include X-rays with a patient's file. The pictures require as little as 12 kbytes of storage memory, thanks to a data-compression algorithm. Compressed data from the host system is prefaced by a control sequence that tells the terminal to decompress the data. Because ordinary text

doesn't contain the control sequence, it's displayed normally. Images are created with a video camera and the ImageTerminal, using application software that's developed by the systems integrator. In OEM quantities, the terminal costs $2495 to $3995.JT **CIRCLE 306**

MAC & PC USERS CAN NOW SHARE DATA FILES

With its Bernoulli Box II, Iomega Corp., of Roy, Utah, made it possible for Macintosh users to share stored data files from IBM PCs and compatibles. The removable data-storage system enables Mac users to share the more than 2 million Bernoulli cartridges currently in use with PCs and with PS/2 machines. A file that was formatted by a PC or compatible is inserted into the Bernoulli Box II connected to a Macintosh, and the data on the cartridge will appear to the Mac user along with his other data as standard files and file folders. The system uses 5-1/4-in. removable disk cartridges to store up to 20 Mbytes of data per cartridge. Designed to fit on top of the computer and under the monitor, the box has a low profile. Suggested retail prices are $2550 and $1650 for dual- and single-drive boxes, respectively.DM **CIRCLE 307**

MULTIFUNCTION ROM PACKS SRAM, I/O LINES

Many microprocessor-controlled products, such as printers and typewriters, will benefit from the new, highly integrated M6M72561J CMOS multifunction ROM device from Mitsubishi Electric Corp., of Itami, Japan. In addition to its 256-kbits of one-time-programmable ROM for system programs, the device packs 16-kbits of static RAM for data. For further flexibility, the chip can be configured with either an 8- or 16-bit data bus for use with 8- or 16-bit processors. A presettable 8-bit counter is included, as are 14 input lines, eight output lines, and eight programmable lines. Although the device needs only 16 address lines for its on-chip memory, two more address lines are tacked on to supply four selects for other chips or peripheral units. The chip, in a 68-lead plastic leaded chip carrier, will start at $22.50 when sampling begins in October.CC **CIRCLE 308**

VIEWLOGIC EXPANDS TO SUN CAE PLATFORMS

With an eye toward broadening its CAE horizons, Marlboro, Mass.-based Viewlogic Systems Inc. ported its entire suite of CAE software to Sun Microsystems' Sun-3 platforms. Until now, only the computation-intensive and non-graphical portions of Viewlogic's Workview product line ran on Sun machines. With the addition of the Sun-supported software, Viewlogic's full line of CAE tools now run on a variety of platforms including PCs running MS-DOS, VAX computers running VMS, and Sun platforms operating under AT&T's Unix. A common user interface and database is maintained across all platforms.BM **CIRCLE 309**

PROTOCOL CONTROLLER LINKS TO NETWORKS

The key building blocks needed to interface with packet data-communication networks are bundled in the Am79C401 integrated data-protocol controller (IDPC) from Advanced Micro Devices, of Sunnyvale, Calif. The chip, which is finally in volume production, contains an HDLC data-link controller, a USART, and a dual-port memory controller. With the 68-pin device, designers can build communication processors and terminal adaptors for HDLC-based packet networks, such as ISDN, X.25, SNA, DMI, and proprietary networks. AMD also offers system software packages for the controller, such as the Am79LLD401 low-level driver, which creates a common interface to higher levels of software. The IDPC comes in PLCC or LCC packages and costs $20.52 in lots of 100.DM **CIRCLE 310**

EXTERNAL MODEM RECOVERS SERIAL PORT

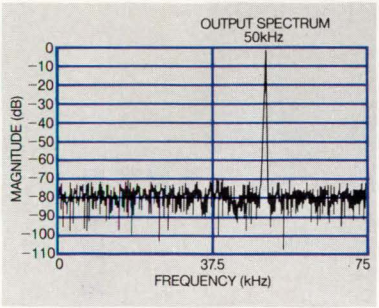
The XE2400FT, a feedthrough modem from Xecom, Inc., of Milpitas, Calif., plugs into the lone serial port in many compact PCs and laptops. But instead of hogging that port, the modem makes it available to a mouse, serial printer, or other serial device when the modem is not in use. With its full V.22 bis compatibility, the modem communicates at data rates of 2400, 1200, and 300 bits/s and responds to the Hayes 'AT' command strings. Because the modem has two RJ-11 phone jacks, two-way voice or data communications can be carried out. Also, two RS-232 connectors are on the unit: one ties into the host PC's serial port, and the other serves as the feedthrough and can attach to the serial peripheral. The feedthrough feature does away with the need for an A-B switch box and the headache of switching cables. The feedthrough modem sells for $349 each, and tosses in the Mirror II communications software and adapter cables. A $449 version comes bundled with an optical mouse, Mirror II, and two drawing packages.DB **CIRCLE 311**

New 8-bit A/D converters with sample and hold maintain accuracy at 50KHz.

The new ML2258 and ML2281 series from Micro Linear maintain true 8-bit accuracy while digitizing a 0V to 5V, 50KHz sine wave. This gives you near ideal signal-to-noise of 47dB. All devices come with either a double buffered parallel or serial digital interface. Yet, these devices are superior for interfacing to temperature, pressure and position transducers due to low cost and ease of use.

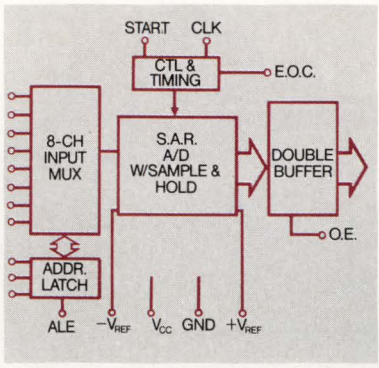
Dynamic Performance and 8-bit Guaranteed Accuracy

Dynamic performance and 6 microsecond conversion time make the ML2258 and ML2281 series ideal for signal processing as well as for digitizing sensors.



The FFT Plot of the ML2258 Converting a 50 KHz, 0 to 5V, Low Distortion Sine Wave Input.

Total unadjusted error in the ML2258 and ML2281 series is ±½ or ±1 LSB, which includes the sum of nonlinearity, full scale and zero scale errors. It is important to note that no full scale or zero adjust is required.



ML2258 Block Diagram

Designed for Ease of Use with a Choice of Analog Inputs

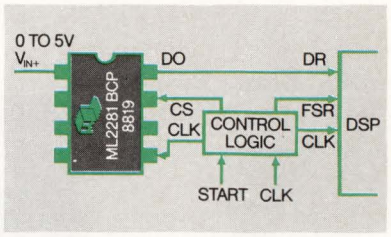
With all parameters guaranteed over the entire ambient temperature range, as well as ±10% tolerance of the single 5V power supply, the ML2258 and ML2281 series are designed for ease of use. Stable and repeatable conversions result from a digital code uncertainty of 1 mV.

Greater design flexibility is allowed by the 0V to 5V analog input range operating either ratiometrically or with a voltage reference up to 5V. The inputs are protected for up to 25mA maximum per input.

Power dissipation overall is extremely low—less than 3mA.

Digital inputs and outputs are both TTL and CMOS compatible.

The ML2258 microprocessor-compatible 8-bit A/D converter with 8 analog inputs has a



ML2281 Serial DSP Interface

double-buffered three state output and latched and decoded multiplexer address inputs. It is available in both 28-pin DIP or PCC.

The ML2281 series 8-bit serial I/O A/D converters provide a serial address of the 2, 4, or 8 analog inputs. ML2281 series DIP packages are 8, 14 or 20-pin configurations. In addition, the 8-input channel ML2288 is available in a 20-pin PCC. Prices start at only $2.95 each in 100 unit quantities.

Call or Write for More Information

If you would like more information on the ML2258 or ML2281 series A/D converters, or on Micro Linear's complete range of linear devices, please call (408) 433-5200, extension 912, or write:

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CIRCLE 46

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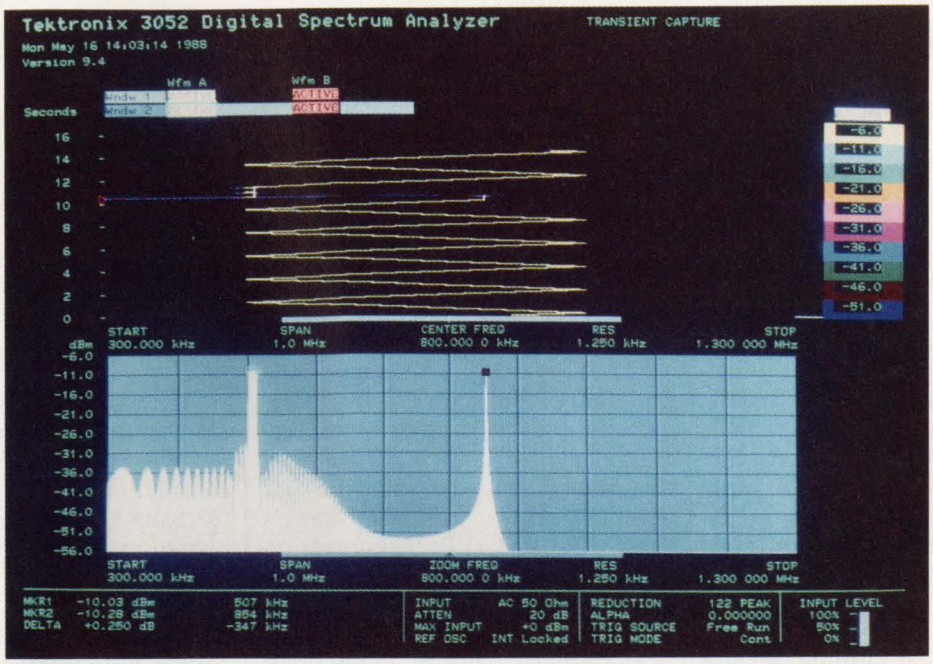


1. IN TEKTRONIX'S 3052 digital spectrum analyzer, the bottom window displays a band-splatter spectrum created by introducing a discontinuity in the triangle signal shown in the upper window. Such measurements are particularly important to designers trying to clean up the output spectrum of radar and frequency-hopping communication systems.

SPECTRUM ANALYZER COVERS 2 MHZ AT REAL-TIME SPEEDS

JOHN NOVELLINO

Designers who must analyze signals in the frequency domain often face a dilemma. Conventional spectrum analyzers do a good job displaying broad bandwidths, but their swept-frequency techniques are too slow to be considered real time in many applications. Covering wide bandwidths in relatively long sweep times, they heterodyne the input signal during which time they can miss transient phenomena or modulation effects.

For their part, fast-Fourier transform analyzers can display real-time signal variations because they measure frequencies across the entire bandwidth simultaneously, rather than one at a time. The FFT instrument's digital sampling and processing methods, however, limit bandwidths to less than 100 kHz. And the real-time bandwidth of an FFT instrument is limited by its block-processing rate—how fast it can digitize the signal and transform it.

Many of these engineers will now find what they're looking for—wide-spectrum real-time analysis—in the Tektronix 3052 digital spectrum analyzer, whose 2-MHz real-time bandwidth outstrips FFT analyzers by nearly two orders of magnitude. At 2 MHz, the 3052 updates its spectral output every 200 μs, compared with the 15 to 20 ms for an FFT analyzer. Also, the unit's digital architecture lets a user store up to 500 spectral outputs in the block-capture mode. The outputs can then be ex-

amined individually, frame by frame.

Tektronix aimed the 3052 at engineers working in telecommunications and radar applications, where both speed and bandwidth are important *(Fig. 1)*. The instrument overcomes the 80-kHz real-time ceiling of conventional FFT analyzers—far too low for many applications.

Key to the 3052's performance are a bank of 1024 identical digital finite-impulse-response filters and a new algorithm for converting the input signal from the time domain to the frequency domain. The filter bank breaks down the input signal into its constituent frequencies. Each filter outputs its real and imaginary components into a frequency "bin" or hardware storage location. The combined 1024 parallel outputs constitute a spectral frame, although only the central 800 bins are displayed.

The arrangement of the terms in the transformation algorithm, different than that in the conventional FFT, allows fast parallel processing in calculating the spectrum. Designers of the 3052 didn't rely on the common assumption that the number of points in the frequency domain must equal that in the time domain.

A benchmark parameter for comparing analyzers is the time to do 1024 conversions. The 3052 performs that task, for both magnitude and phase, in 200 μs. FFT analyzers can take 15 to 20 ms.

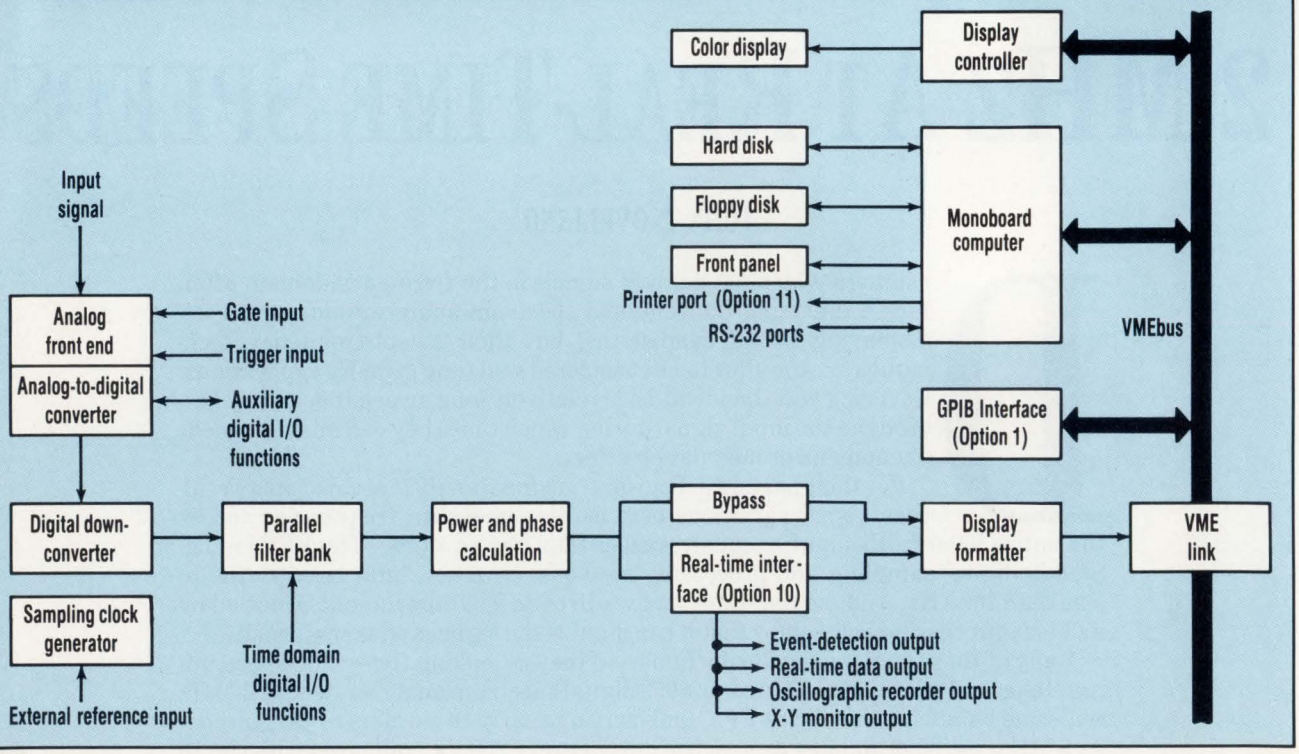
The FIR filters also enhances several analyzer specifications, including amplitude accuracy, spectral resolution, dynamic range, and sensitivity. Each filter's passband is flat within 0.05 dB, and the entire bank's span is flat to 0.5 dB. The filter's 80-dB rolloff 1.5 bins from center lets the 3052 easily separate closely spaced frequency components.

Amplitude accuracy (with error correction) is ±0.5 dB across all frequencies and ±0.2 dB at 12.5 kHz. The display dynamic range is 110 dBm and the maximum input range is 33 to −57 dBm. Sensitivity at 100 kHz is −150 dBm/Hz. For a signal 6 dB below the maximum input, harmonic distortion is 65 dBc up to 1 MHz and 58 dBc from 1 to 10 MHz. Also, the filter's shape and the rate at which the spectrum's samples are output satisfy the Nyquist criteria, so the output spectrum contains no aliased frequencies.

The analyzer's marker resolution is the selected span divided by 800, or 1.25 Hz to 2.5 kHz at spans from 1 kHz to 2 MHz. Bandwidths of 5 and 10 MHz are also available, but the frame output interval remains at 200 μs; consequently, Tektronix doesn't consider them real-time. Since the filter bank's center frequency is tunable, any frequency within the 10-MHz range can be viewed at a narrow span.

To display as much of the filter bank's output as possible at wide spans, the analyzer offers several data-processing formats: average, peak, min/max, and Rth, where every Rth output frame is displayed. For greater flexibility, the user can manually set R to 1 to 1024 in the av-

SYSTEM BLOCK DIAGRAM



2. THE ANALYZER DRAWS its real-time conversion speed from the parallel bank of 1024 digital FIR filters and an improved algorithm for transforming the input signal from the time domain to the frequency domain.

2-MHz SPECTRUM ANALYZER

eraging mode, and from 1 to 65,535 for the other three modes.

The 3052 consists of separate display and control units, both rack-mounted. The 16-in., 1024-by-768-pixel monitor displays power vs. frequency, phase vs. frequency, and spectragram and waterfall modes. A spectragram places frequency on the horizontal axis and time on the vertical axis and uses color as a third variable to help illustrate how the spectrum is changing with time. A combination of pushbuttons and knobs (for amplitude, span, and frequency) control the analyzer's functions. An LCD panel (16 characters by 25 lines) presents the analyzer's function menus and prompts users to enter parameters. A 70-Mbyte hard drive and a floppy-disk-drive are built into the control unit.

The VMEbus serves as the basis for the analyzer's system architecture. Cards performing the main instrument functions are pipelined to an interface that links them to the bus *(Fig. 2)*. After passing through an analog front end, the input is digitized by a 25.6-Msample/second 10-bit analog-to-digital converter. The signal then goes through the filter bank before power and phase calculations are made.

The 3052 operates under the System V/68 version of AT&T's Unix, with instrument controls and functions performed in C language and firmware on the cards. With selected Unix utilities and C libraries, users can develop their own application programs via an RS-232 port.

Besides an optional GPIB interface, the instrument is available with a real-time interface (Option 10) that supplies 32-bit spectral data. Option 10 also lets users detect spectral events by setting up maximum and minimum limits for the output. The option includes analog outputs to drive an oscillographic recorder, X-Y monitor, or oscilloscope. A third option offers an output for the Tektronix 4696 color ink-jet printer.□

PRICE AND AVAILABILITY

The base price of the 3052 digital spectrum analyzer is $75,000. Delivery takes 12 weeks. Option 1 (GPIB) costs $1995; option 10 (real-time interface), $9500; and option 11 (color copier interface), $1495.

Tektronix Inc., Frequency Domain Instruments Div., P.O. Box 500, MS 38-386, Beaverton, OR 97077; Douglas L. Goodman, (503) 627-7794. **CIRCLE 512**

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MODERATELY	560
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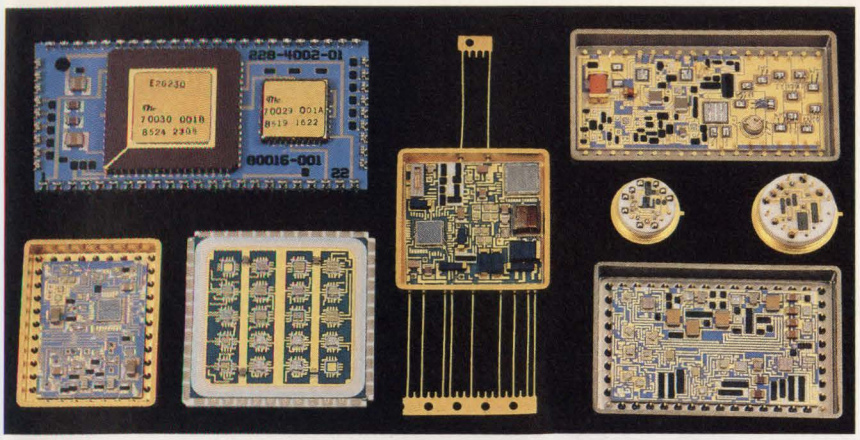

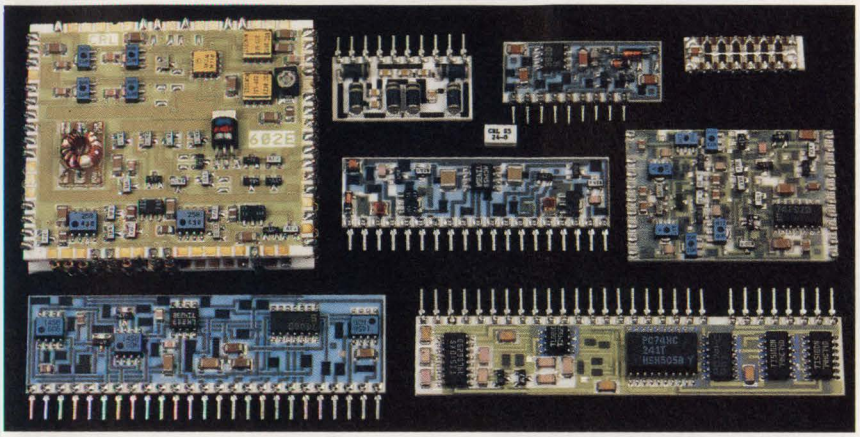

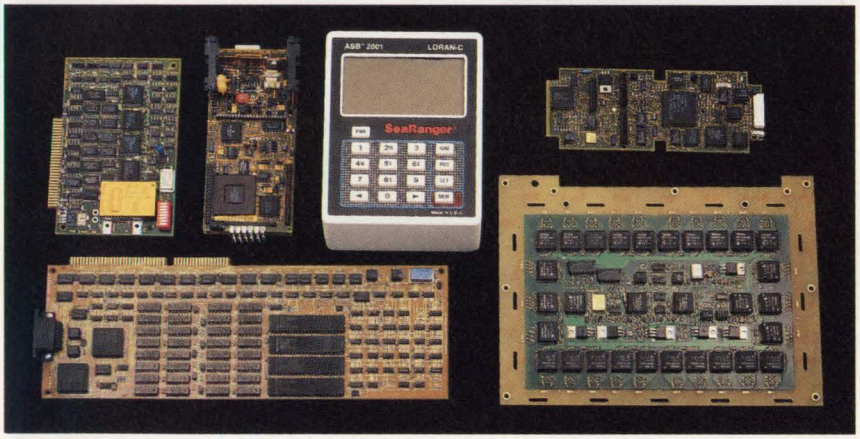

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CIRCLE 49

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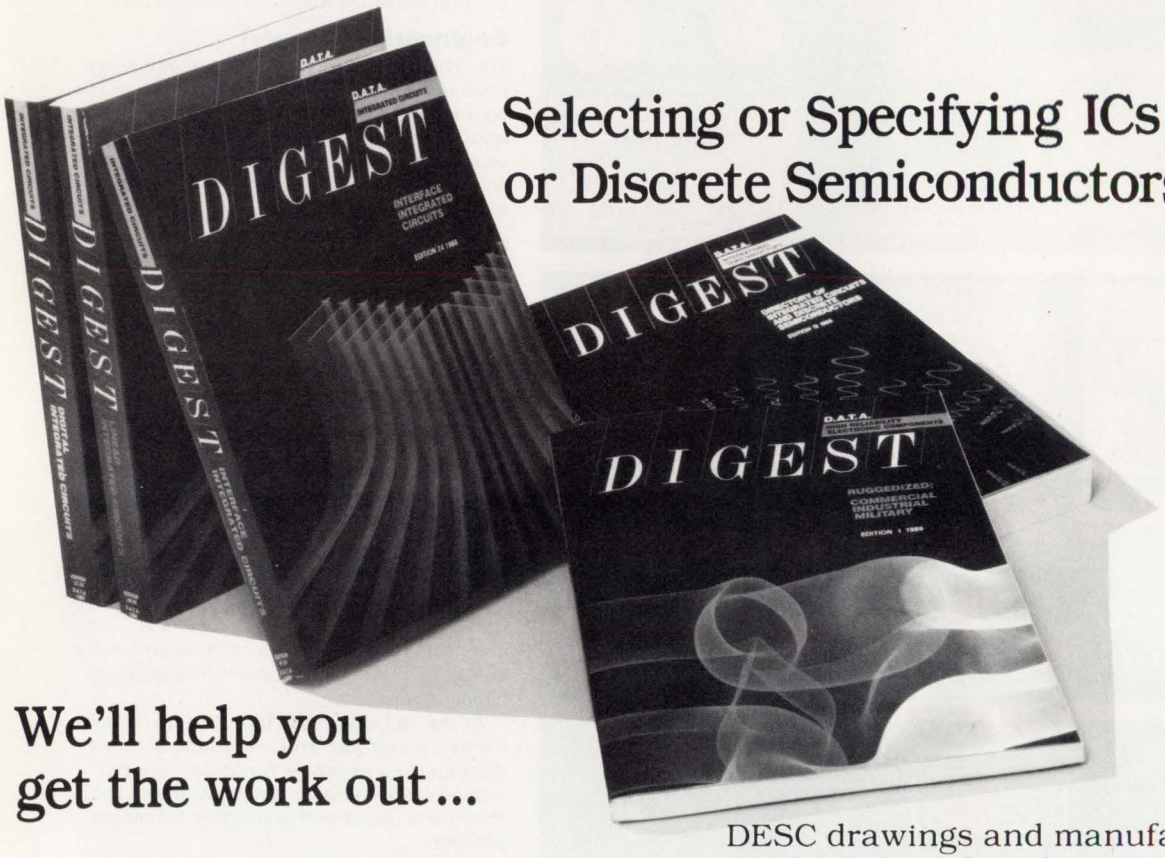

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CIRCLE 74

SPORTING DUAL 16-BIT MULTIPLIER-ACCUMULATORS, TWIN ADDERS, AND ON-CHIP ADDRESS SEQUENCING, CMOS IC EXECUTES 1024-POINT FFTS IN 0.5 MS.

ONE-CHIP FFT PROCESSOR RIPS THROUGH SIGNAL DATA

DAVE BURSKY

Whether signal data will be processed in the time or frequency domain, swift algorithm execution depends on speedy arithmetic elements such as multiplier-accumulators (MACs). By integrating fast 16-bit MACs on one CMOS chip, along with an extra adder for each, an address generator, and a coefficient/microprogram ROM, TRW LSI Products has created a signal-processor chip that executes fast-Fourier transforms and other algorithms in just 100 ns per complex radix-2 butterfly.

The butterfly's swift execution lets the TMC2310 signal-processor chip rip through 16, 32, 64, 128, 256, 512, or 1024 complex- or real-point fast Fourier-transform (FFT) algorithms in 8 to 514 μs, respectively, at its 20-MHz maximum clock rate. These speeds are 4 to 10 times faster than general-purpose and most dedicated digital-signal-processing (DSP) chips. Users can also program the chip to perform multiple equal-length transforms on up to 1024 data points. As a result, the chip executes up to 64 FFTs with 16 data points, 32 FFTs with 32 data points, and so forth, all the way to one FFT with 1024 data points. What's more, multiple TMC2310s can be orchestrated to process data in parallel and further accelerate computations. System performance is limited only by the maximum clock rate or the memory access time, which is 15 ns at the 20-MHz maximum clock rate.

ROM routines let the circuit execute forward or reverse transforms, with or without data windowing. Designers can select automatic block-floating-point rescaling, or, if necessary, they can program their own algorithm for the chip to execute.

Besides performing the FFT algorithms, the processor can implement in-place, memory-based finite-impulse-response (FIR) filters that employ an external window coefficient memory to store the filter coefficients.

Fixed coefficient or adaptive FIR filters can be set up with tap lengths of 16 to 1024. Real and complex vector arithmetic functions—multiplication, multiplication-accumulation, and magnitude-squared—are also embedded in the 2310's on-chip ROM. By combining these functions with the filtering and FFT routines, designers can perform various signal-processing algorithms, including frequency-domain filtering, signal analysis, and signal synthesis.

SIMPLE ARCHITECTURE

The two key blocks in the processor's basic architecture are the twin arithmetic elements that execute the multiplications, accumulations, and additions for the algorithms *(see the figure)*. A state-machine block controls the arithmetic blocks, keeps track of the scaling—sometimes called the equivalent exponent—and generates the external memory control signals. An address generator supplies the addresses for the off-chip memory and for the transform and coefficient ROM. Although the algorithms execute with a 16-bit, fixed-point

data format, the intermediate results are carried to 19 bits to minimize arithmetically generated noise. Also, both arithmetic elements can transfer the 19-bit data out to or in from the registered, 19-line bidirectional data buses.

Two other registered ports on the arithmetic elements accept the external 17-bit window coefficient and the internal 17-bit ROM coefficient—sine or cosine twiddle factors. Because the 17th bit allows +1.0 to be represented exactly, round-off error is minimized. To move data between the arithmetic elements, two unidirectional 18-bit ports cross-couple the math units so that one can feed its result directly into the other element's incoming data port. Programmable shifters in the arithmetic elements scale the data by up to 3 bits rightward to compensate for word growth during multiplication and accumulation cycles. Each arithmetic block also contains an 18-by-18-bit fixed-point multiplier-accumulator (which delivers a 36-bit product and a 36-bit accumulation result) a separate 19-bit adder, and some registers and shifters.

Flexible Arithmetic

The arithmetic elements must be flexible, because the calculations must be done on both positive and negative coefficients and because of the additions and subtractions inherent in the butterfly algorithm. It can compute the sum or difference of each pair of products and can add or subtract each sum of products from the unmultiplied incoming data term. The 19-bit postadder takes the accumulator's most significant 18 or 19 bits.

The processor accepts 16-bit data and transfers 19-bit intermediate results. Either automatic pass-by-pass block-floating point or manual rescaling can be performed on the data to deal with word growth as multiplications and accumulations increase word length. Incoming data, though, is rescaled to 16-bit two's-complement fractions, based on the maximum overflow detected during the last pass (automatic scaling) or on a figure the designer presets (manual scaling).

External fast static RAMs or nonvolatile memories store the complex data points and the window or filter coefficients. Twin bidirectional data ports allow the circuit to send back the results from the computations so that designers can build in-place or ping-ponged memory architectures with either single or dual memory banks.

With the multibank approach, users can overlap I/O and arithmetic operations and minimize time lost in performing overhead tasks. To reduce the memory bandwidth requirements by up to 50%, the processor performs the FFT radix-2 butterflies in groups of four and is completely self-sequencing.

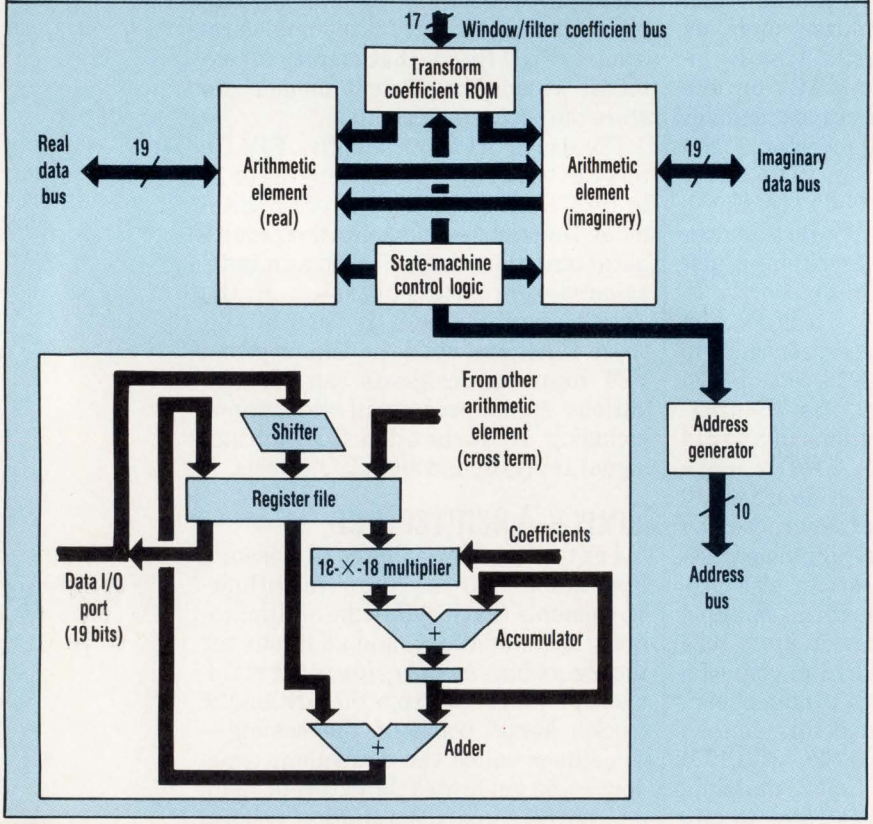
Memory Saver

Although the processor transfers 19-bit-wide data, designers can configure systems for 16-bit-wide memory arrays and for user-controlled 3-bit data scaling. Such systems will help trim the memory-component count but will result in a slightly higher round-off error in the calculations.

The twin 19-bit data buses, a 17-bit coefficient bus, and a 10-bit address bus occupy 65 of the 84 or 88 leads in the packaged chip. Various signal lines—RAM Write Enable, RAM Read/Write, RAM Select, Clock, Done Flag, and a few others—take up 8 of the remaining pins; power and ground lines account for the 11 or 15 still unoccupied.

Since the chip typically consumes about 800 mW operating at 20 MHz, TRW will offer it in either an 84-lead flatpack with 25-mil lead spacing or in an 88-lead pin-grid-array package. For military customers, full MIL-STD-883C screened versions of the

BLOCK DIAGRAM OF THE TRW TMC2310



TWIN ARITHMETIC ELEMENTS, each packing a full 18-bit multiplier-accumulator and an extra 19-bit adder, are the key blocks on TRW's TMC2310 FFT signal processing chip. Another block containing some state machines controls the math elements, the address generator, and a microcode and coefficient ROM.

FAST FFT PROCESSOR

PRICE AND AVAILABILITY

The CMOS TMC2310 is available in either an 84-lead flat pack or an 88-lead pin-grid array package. In quantities of 1000 units the PGA-housed commercial version will sell for $120. A military version is also planned. Samples will be available in the middle of the fourth quarter.

TRW LSI Products Inc., P. O. Box 2472, La Jolla, CA 92038; Rich Wegner, (619) 457-1000.

CIRCLE 513

device will be available.

Designed to operate as a peripheral to a microprocessor, the signal processor can be initialized for one of its embedded algorithms with just two internal, 16-bit control words and three simple commands—Load, Start, and Reset. The two control words set the algorithm parameters—the operating mode, transform size, data addressing modes, single (strict in-place) or bank-switching memory architecture, as well as other options. Once initialized, with the source data and window coefficients loaded into external memory, a simple Start command triggers execution. The chip generates data and window memory addresses, plus control signals. When the algorithm is executed, the circuit alerts the host processor with a Done signal.

With the transform completed, the host system can read the 19-bit data output and a 6-bit scaling factor generated by the internal shift-rescale circuitry during the transform execution. The 6-bit value is divided into a 4-bit "total scaler" value and a 2-bit maximum overflow. The scalar value equals the number of shifts performed on the data. The 2 overflow bits show the maximum overflow during the final data pass, or how many of the upper 3 bits contain valid information.□

HOW VALUABLE?	CIRCLE
HIGHLY	562
MODERATELY	563
SLIGHTLY	564

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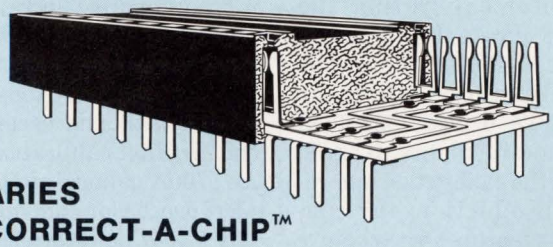

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CIRCLE 51

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CIRCLE 52

MULTIFUNCTION CALIBRATOR TAKES ON HIGH-ACCURACY DMMs

DAVID MALINIAK

Capable of calibrating the most accurate digital multimeters (DMMs), the 5700A multifunction calibrator from John Fluke brings expanded performance and flexibility to applications both in the calibration laboratory and in production environments. The unit features an absolute uncertainty specification (including stability, temperature coefficient, linearity, line and load regulation, and standards traceability) of dc volts to 5 ppm, ac volts to 80 ppm, direct current to 50 ppm, alternating current to 150 ppm, and resistance to 12 ppm. These accuracy specifications are for 90 days, ±5°C of calibration temperature.

The instrument offers direct voltages to 1100 V and alternating voltage from 220 μV to 1100 V at frequencies from 10 Hz to 1 MHz. Cardinal point resistances range from 1 Ω to 100 MΩ, including a short, in X1 and X1.9 decades. Direct and alternating currents are supplied to 2.2 A, and frequencies for alternating current range from 10 Hz to 10 kHz.

The calibrator performs many functions automatically, so that less experienced technicians can calibrate instruments that normally require the attention of highly trained personnel. Support costs are significantly reduced because calibration adjustments of all 5700A ranges and functions are made using only three artifact standards.

Traditionally, high-accuracy multifunction calibrators have required costly support equipment and frequent calibration to ensure that they operate within necessary tolerances. The artifact-calibration process of the 5700A calibrator operates under microprocessor control and requires only a 10-V dc reference and 1-Ω and 10-kΩ resistance references to maintain the accuracy that is traceable to legal standards on all ranges and functions.

The temperature stability of the 5700A calibrator permits it to be used and calibrated in production environments, reducing down time and eliminating the need for backup instrumentation. The unit can be calibrated on-site at any temperature from 15 to 35°C, with specified accuracy available over a 10° range spanning those temperatures.

A wideband voltage option delivers a flat, low-noise alternating-voltage output from 10 Hz to 30 MHz, extending coverage to include rf voltmeters. The companion 5725A amplifier increases the calibrator's maximum direct- and alternating-current capability to 11 A for calibrating the high-current ranges of most popular low-cost and handheld DMMs. In addition, the amplifier meets the needs of many high-accuracy bench and systems meters by extending the calibrator's volt-hertz product to 1100 V at 30 kHz and 750 V at 100 kHz. The 5700A calibrator has built-in support for the company's existing voltage and current amplifiers.

Many of the instrument's features make it easy to use, even for inexperienced operators. Values are entered on a simple numeric keyboard, displayed on the front panel, and then confirmed with the Enter key. To verify the accuracy of the unit under test, the operator simply adjusts the output knob and the error is displayed directly in parts-per-million or a percentage. With the Offset and Scale keys, the 5700A calibrator compensates for meter zero-offset and scale errors and directly displays linearity errors at any scale level. To simplify work on meters requiring calibration levels in even-decade steps, the operator just touches the multiply-by-10 or divide-by-10 keys.

Calibrating the 5700A itself on-site is an easy process taking less than one hour. The operator simply follows prompts displayed in plain English on the front panel to make various connections and inputs. Because the calibration process is automated, more reliable results can be obtained in less time by an operator with minimal experience.

Between artifact calibrations, the instrument's performance can be checked against its internal standards in an automated procedure called Cal Check. Results can be sent to a computer for processing or printed by means of the IEEE-488 or RS-232-C ports, and used to develop control charts for predicting the calibrator's performance over a long period of time.

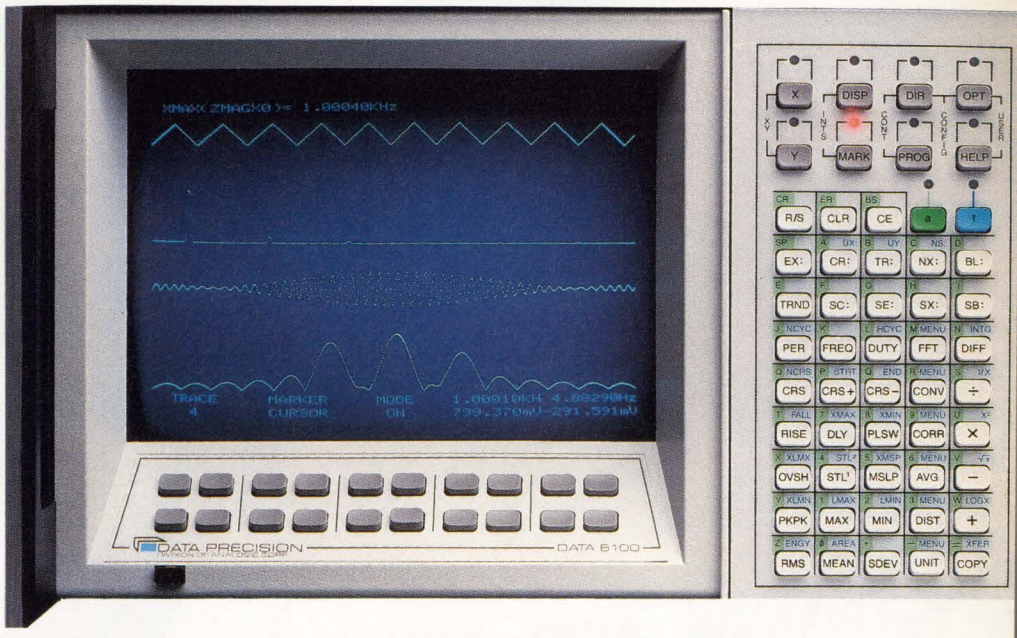
The 5700A calibrator costs $19,950. The 732A 10-V dc reference, 742A-1 1-Ω resistor reference, and 742A-10K 10-kΩ resistor reference cost $3300, $795, and $695, respectively. The 5700A-03 wideband voltage option costs $3995 and the 5725A amplifier goes for $7950. Delivery is in 4 months.

John Fluke Mfg. Co. Inc., P.O. Box C9090, Everett, WA 98206; (800) 443-5853. **CIRCLE 353**

FIND THE SOLUTION TO YOUR CHALLENGING SIGNAL ANALYSIS PROBLEM HERE. *(Or challenge us to come up with a solution for you).*

THE INSTRUMENTS:

The DATA 6100 permits complex signal analysis with or without computers. You get simple one-key access to 50+ processing functions, settling time to within 0.01% of final value in less than 10 ns, rise times as fast as 350 ps and resolution to 16 bits at 100 GHz effective sampling rate. **The MODEL 2020** generates waveforms in real time, lets you add noise, glitches, simulate phase shifts or degraded rise times with front panel entry, and features a 512K output memory.



THE SUB SOLUTION:

With the 650-1 Plug-In Digitizer's true 16-bit/1 MHz resolution, the DATA 6100 can determine "Who goes there?" in the undersea environment, easily differentiating seemingly identical screw and engine noises. With more than 50 resident functions and 32,000 data point storage, analysis and retrieval of key sensor data are greatly simplified.

THE BIOMEDICAL SOLUTION:

Studies of the effect of psychotropic drugs on brain electrical activity may lead to greater understanding of the etiology of mental disorders. The DATA 6100 acquires signals from 0.5 to 100 mV with durations of fractions of a millisecond in this advanced research program. In other applications, the Model 2020's direct entry, real-time waveform generation and modification enhances analysis.

THE VIBRATION SOLUTION:

The DATA 6100's extensive frequency and time-domain capabilities excel in industrial vibration analysis, such as the automatic testing of transmissions, alternators, and fuel pumps. For example, 6 FFT input types and 18 result options speed electric fuel pump fault detection through signature analysis.

THE DISK DRIVE SOLUTION:

Disk drive performance parameters such as position error signal (PES) symmetry and seek-time errors can be rapidly and cost-effectively tested with the DATA 6100 and the 620-1 plug-in. Testing PES resonance and PES spike is equally fast and efficient. The 6100's programmability and powerful algorithms provide single-key results.

Sub photo/General Dynamics

CIRCLE 72

YOUR SOLUTION:

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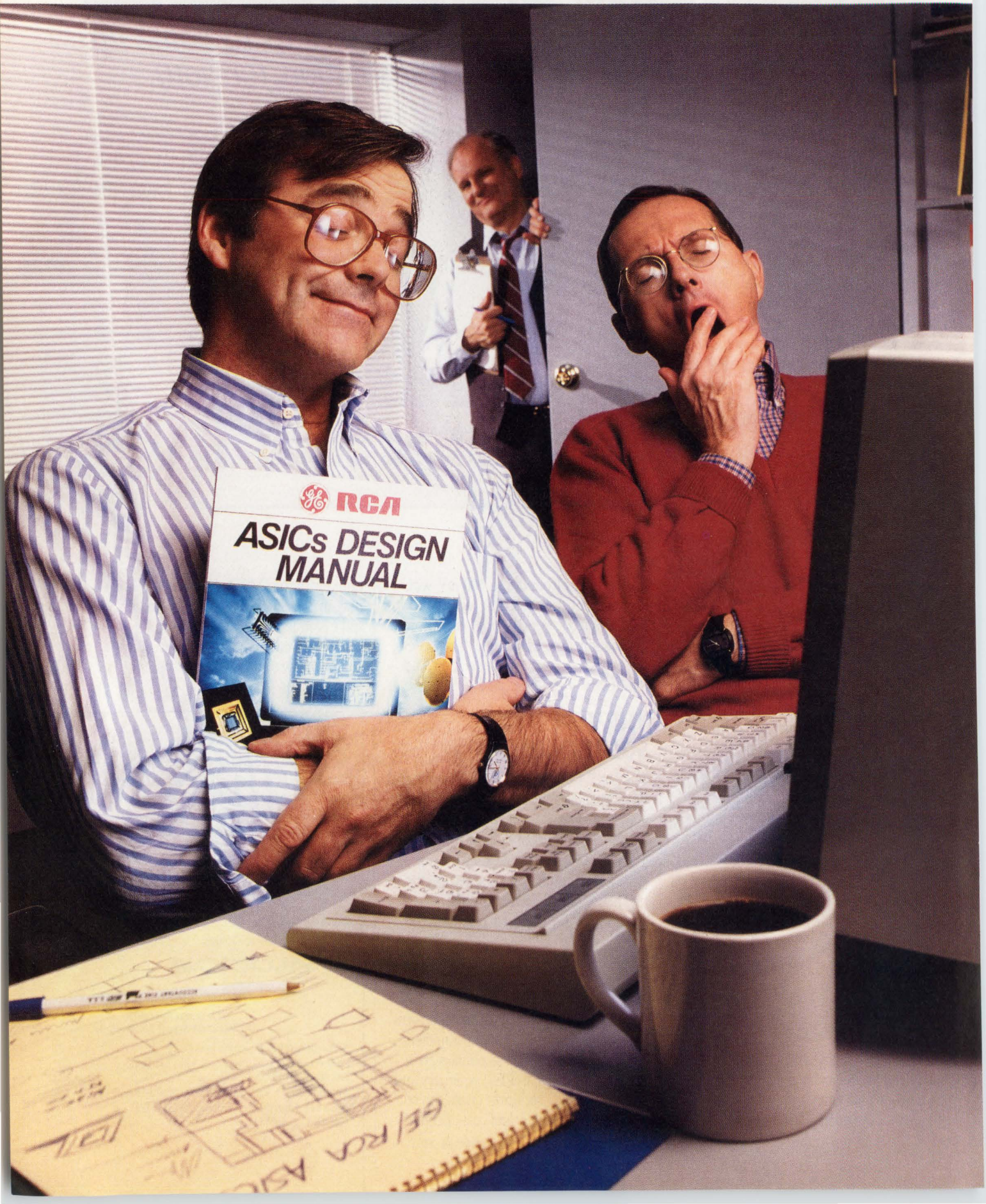

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You've heard all about the excitement of ASICs.

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But, unfortunately, you've probably also heard about one big potential problem: while many ASICs pass the tests specified by the designer, they don't always work in the real world. And that causes excitement you can do without.

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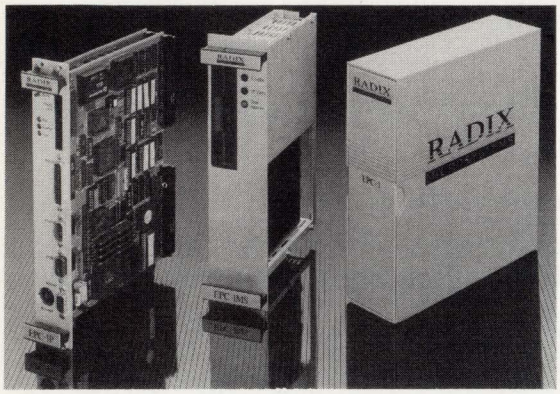
80386-Based Embedded PC Packs 32-Bit VMEbus Link

Intended to help systems integrators and OEMs cut costs and shorten the system-development process, the EPC-1 80386-based embedded computer from Radix Microsystems features a full 32-bit VMEbus interface.

The PC AT-compatible two-module set lets designers take advantage of the full spectrum of operating systems and application and development-tool software already available for the PC while opening a path to over 1000 memory, I/O, and auxiliary-processor products offered by VMEbus vendors. In addition, the EPC-1 processor offers direct support for the VXI modular instrumentation-bus standard.



By directly embedding the EPC-1 computer in systems, costs are lowered and performance and reliability improved by elimination of duplicate hardware and by taking advantage of the speed and ruggedness of the VMEbus. Also, the large available software base makes a PC AT-compatible modular processor a desirable alternative to traditional single-board computers, particularly in terms of the cost and time required to develop system and application software.

The EPC-1 includes a processor module with a 16- or 20-MHz 80386 microprocessor and up to 4 Mbytes of dual-ported 32-bit, zero-wait-state RAM. Built into the module are an EGA graphics controller (with full support of 640-by-480-pixel super EGA), floppy and SCSI hard-disk controllers, two RS-232 serial ports, a parallel printer port, and a PC AT-compatible keyboard port. The EPC-1 disk module contains a 1.4-Mbyte, 3-1/2-in. floppy-disk drive and a ruggedized 40-Mbyte hard disk. Both modules comply fully with VMEbus specifications.

For users of the VXI extension to the VMEbus, the EPC-1 processor supplies hardware support for geographical addressing, module configuration, and description; and message passing. The company implements the VXI and VMEbus interface functions with proprietary gate arrays.

A major component of the EPC-1 computer that simplifies and shortens the system-development process is the EPConnect software package. The software enhances the computer's capability as a full-fledged system controller on a backplane bus by serving as an interface between application software and the VMEbus. It also supplies a direct device driver for commonly used VMEbus I/O cards.

Included within the EPConnect software is the auxiliary processor interface package, which can run on other processors on the VMEbus and allows those processors to communicate with the EPC and share its disk-storage module. The interface enables addition of the EPC-1 to existing VME systems as PC coprocessors.

To simplify system prototyping, the company offers its EPC-1000 package, which includes the EPC-1 module pair combined with DOS 3.3, Microsoft Windows 2.0, or Windows 386; a keyboard; a PC-to-EPC-1 migration link; and complete documentation. The package costs $7950. Delivery is from stock.

Radix Microsystems Inc., 19545 Von Neumann Dr., Beaverton, OR 97006; (503) 690-1229. **CIRCLE 354**

512-Pin Tester Handles High-Pin-Count CMOS ASICs, VLSI Parts

Designed to test CMOS ASICs and a wide range of other VLSI devices, including ECL and GaAs types that require very high pin counts and pattern rates are a pair of semiconductor test systems from Tektronix. The LT-1100 and LT-1100+ Vista Series testers are 512-pin systems that augment the company's lineup of high-performance testers.

The LT-1100+ generates stimulus signals at 100 MHz without multiplexing and has an overall placement accuracy of ±275 ps across all pins, including driver and comparator skew. The tester also has a maximum pattern data rate of 200 Mbits/s. The 50-MHz LT-1100 supports pattern data rates up to 100 MHz and has an accuracy of ±500 ps. Both systems feature per-pin timing resources, 39-ps resolution, 256 kwords by 4 bits of pattern memory per pin, and 64 parametric (dc) measurement units.

Like other members of the Vista Series of testers, the LT-1000 uses highly integrated CMOS ASICs to reduce the size, power requirements, and cost of the all-important pin-electronics function. As a result, the 512-pin LT-1100 test head is only 4 in. larger than the earlier 256-pin LT-1000 version. In addition, the LT-1100 head is air-cooled, allowing easy manipulation for overhead wafer sorting. The lower component count and low heat dissipation result in high reliability and repeatability.

Featured in the LT-1100 system is a fully scalable architecture that combines tester-per-pin and shared-resource technologies. The tester's 512 I/O channels are partitioned in 64-pin modules.

The LT-1100 system is priced at about $1.6 million while the LT-1100+, with its higher accuracy and pattern data rate, is priced at about $1.9 million. Shipments begin June 1, 1989.

Tektronix Inc., P.O. Box 4600, Beaverton, OR 97075; (503) 629-1035. **CIRCLE 364**

VXIbus Development Tools Get Designs Going

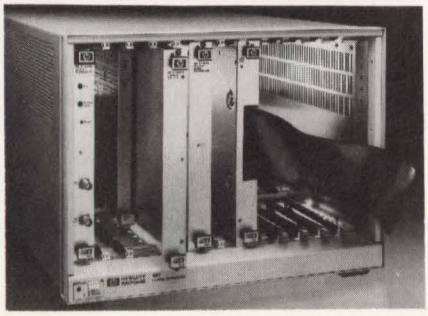
Early adopters of the VXIbus, the VMEbus extension for instrumentation, can get a head start on their designs with a VXIbus mainframe and a set of development tools from Hewlett-Packard. The tools help VMEbus users develop VXIbus custom instruments on a card faster and with less extensive resources.

Because the VXIbus is an open-standard instrumentation system, test developers can build their own modules. This task is made easier and faster with the development tools. VXIbus manufacturers can also use the tools to speed product development and minimize the time it takes to bring those products to market.

The tools are designed for product development of C-size and smaller VXIbus modules. The C-size carriers permit development of A- and B-size modules within the C-size mainframe. A positive-pressure airflow system ensures a flow of clean air to all modules, eliminating the need to install front panels on unused slots. Variable-speed fans keep modules cool without excessive noise.

In addition to the mainframe, the tool kit includes a slot 0 translator module, a register-based breadboard module (with schematics), a module carrier, a chassis shield for rfi reduction between modules, and development software for use with the company's HP 9000 Series 300 controllers.

The HP E1400A C-size VXIbus mainframe costs $6600. The HPE1404A slot 0 translator module, HP E1490A breadboard module, and HP E1408A module carrier cost $850, $500, and $170, respectively. The HP E1409A chassis shield goes for $150, while the HP 98646A VMEbus interface for the 9000 Series 300 controllers costs $1295. Pricing is not yet set for the VMEbus preprocessor. Delivery is in 4 weeks.



Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, CA 94303; call local Hewlett-Packard sales office. **CIRCLE 355**

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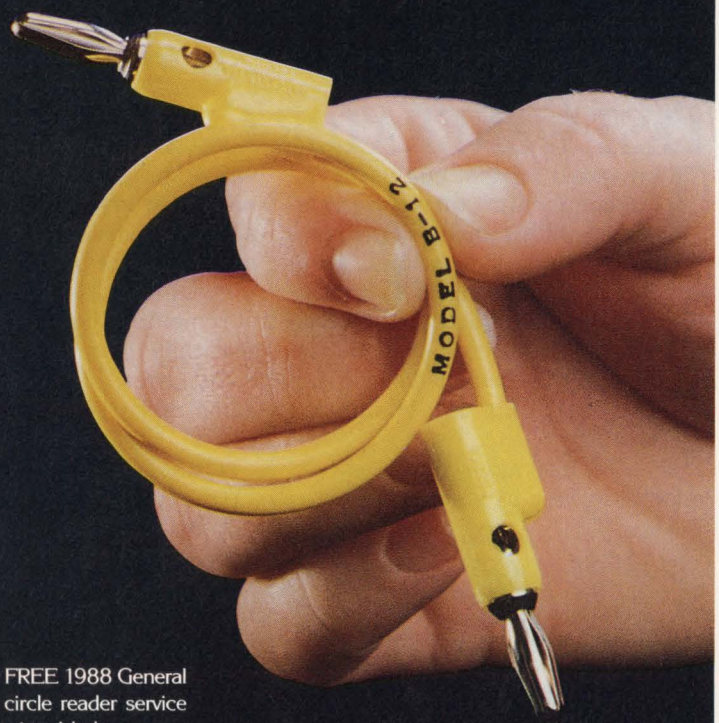

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CIRCLE 58

RECORDER TAKES 1 MSAMPLE/S/CHANNEL

Capture of eight analog and eight event data channels per mainframe with true master-slave expansion capability up to eight systems (128 channels) is possible with the 5300 series programmable waveform-recording system from Gould. The fully programmable, 68000-based system performs simultaneous sampling from 1 Msample/s to days at 12-bit resolution.

Thanks to the company's Event Manager triggering system, users can capture only data of interest. The Event Manager features a 21-input, dual-trigger tree system, using logical AND and OR functions to enable discrimination of over 500,000 unique transient events. This allows virtually any trigger event from single contact closure to complex Boolean definitions involving all acquisition parameters.

Individual channel trigger criteria is adjustable using above/below level or inside/outside a user-defined asymmetrical window. This flexibility permits triggering when the signal exceeds a threshold, crosses through zero, or breaks a boundary condition.

The recorder features two independent clock functions that correlate real-world signals to time. The real-time clock is programmable to begin an acquisition at a specific data and time.

The Memory Manager feature optimizes memory utilization. Users can define memory allocation with channel depth ranging from 256 to over 2 million samples per acquisition in increments of 256 samples. Options include a digital-to-analog converter for hard-copy output to standard oscillographic recorders, a choice of three analog-to-digital converters, and an intelligent front panel with an electroluminescent display that has menu-driven setup and waveform-display software.

The system is designed around an internal architecture that supports up to 20-bit data words with over 2 Msamples/s of system acquisition throughput. Also available is the ACQ5300 setup and acquisition software, which lets users without any programming experience set-up the system quickly. The software runs on IBM PC AT and PS/2 computers as well as Compaq machines.

The 5300 waveform recording system starts at $15,000. Delivery is in 45 days.

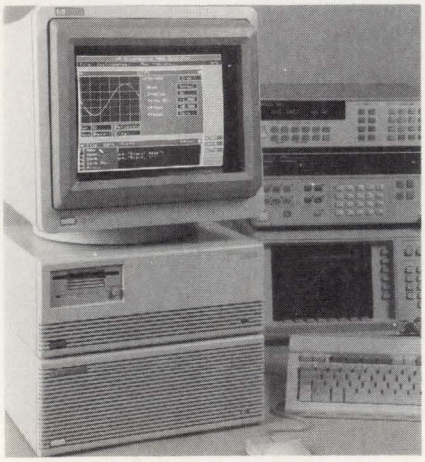
Gould Inc., Test & Measurement Division, 3631 Perkins Ave., Cleveland, OH 44114; (216) 361-3315.

CIRCLE 358

TEST GENERATOR CUTS DEVELOPMENT TIME

Targeted for test engineers, independent of their programming skill, is an interactive test generator software package from Hewlett-Packard. The HP ITG package accelerates HP Basic test development with a windowed, mouse-driven interface designed specifically for controlling HP-IB instruments.

The ITG package reduces test-development time by supporting interactive program development with on-screen instrument panels. Menu selections made with the click of a mouse prescribe settings of instruments and initiate and display measurements. The software also automatically generates the HP Basic code necessary to perform these same tasks in the user's test program.



Thanks to the friendliness of the ITG software combined with HP Basic, test engineers are better able to focus on their test task, rather than on software development. It is no longer necessary to write code that requires knowledge of instrument-specific HP-IB mnemonics or to search through volumes of manuals for the right command string. Automatic code generation guarantees consistent, structured, error-free programming, even by inexperienced software developers.

With the ITG software, incorrect instrument settings and data-entry errors that lengthen test development are virtually eliminated through the use of the mouse and menu selections. To avoid setting controls one by one, complete instrument states are stored and recalled with user-defined names. A library of states is quickly generated, and states can be browsed and reused to build new applications with even less effort.

Traditionally, striking a balance between ease of use and performance has been difficult. The HP ITG package makes inroads in this area with automatic incremental state programming. The software tracks the current instrument state and sends only the commands needed to reach the next state.

The HP ITG software runs on all HP 9000 Series 300 computers with HP Basic/UX and on all Series 200 and 300 computers with HP Basic Rev. 5.11. The software costs $995 and delivery is in 4 weeks.

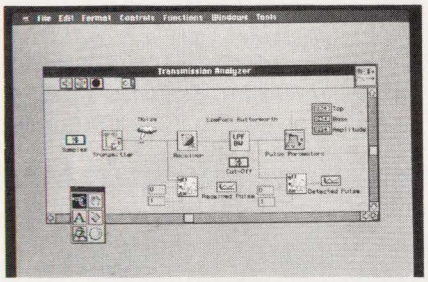
Hewlett-Packard Co., 1920 Embarcadero Rd., Palo Alto, CA 94303; call local Hewlett-Packard sales office.

CIRCLE 359

ICON-BASED SYSTEM EASES MAC PROGRAMMING

Engineering and scientific programming on the Macintosh Plus, SE, and II personal computers is made simpler by version 2.0 of LabView, National Instruments' graphical programming system. Various enhancements to the original product fulfill its promise of graphical automation of data acquisition, analysis, and presentation.

In the LabView system, software programs are called virtual instruments (VIs). VIs have graphical front panels for the user interface, and the program code itself is developed by drawing block diagrams rather than writing sequential lines of conventional program code.



With the inclusion of a compiler and support for multiple numeric formats, version 2.0 of LabView boasts the performance of a conventional compiled language along with the user accessibility of a graphical language. Thanks to the compiler, the new version of LabView runs about 10 times faster than did version 1.2. In version 2.0, the compiler generates machine code from the block diagram, so that when LabView runs a VI, it no longer has to interpret the block diagram, but instead executes the generated machine code.

Other major enhancements, such as diagram rubberbanding, complete clipboard cut-and-paste capabilities, multiple object selection, and dragging objects between windows make rapid prototyping faster than ever. Graphics controls with interactive pan and zoom and cursors have been added to increase flexibility in evaluating graphical results. The package also takes advantage of the Macintosh's color capabilities.

LabView version 2.0 retains the version 1.2 price of $1995. Version 1.2 owners can upgrade at no charge. Beta copies of version 2.0 are scheduled for release by the end of this month, with production copies shipping in November.

National Instruments, 12109 Technology Blvd., Austin, TX 78727-6204; (512) 250-9119.

CIRCLE 363

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CIRCLE 59

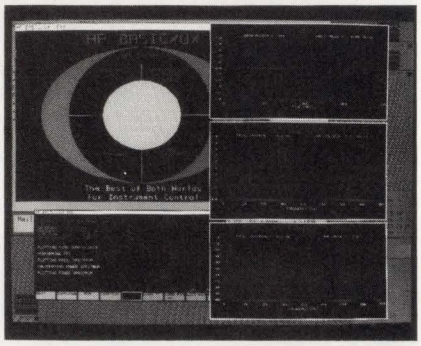
LANGUAGE WEDS BEST OF UNIX, BASIC

Retaining the friendly, high-performance instrument-control capabilities of HP Basic is Hewlett-Packard's Basic/UX, an environment that reduces the development and execution time for instrument-control applications. The language is optimized for running under HP-UX, the company's implementation of the standard Unix System V operating system.

The language and development environment of Basic/UX are the same as that used by most Series 200/300 HP Basic customers. But by wedding HP Basic to HP/UX, users gain such features as networking, multitasking, and windowing, which can be put to work in test applications.

Generic Basic, although easy to use, does not have the necessary functionality for serious instrument-control applications. With its instrumentation background, H-P designed HP Basic to deliver superior instrument-control capabilities without sacrificing friendliness.

By merging with the HP/UX operating system, HP Basic/UX can access IEEE 802.3 networks using ARPA, Berkeley, or the company's Network Services (NS9000) to perform such functions as logging in to remote systems and transferring files. Also, because HP/UX is multitasking, Basic/UX users can partition their complex instrument-control applications into separate processes.



The HP Basic/UX operating system can access IEEE 802.3 networks using ARPA, Berkeley, or the company's Network Services (NS9000) to perform such functions as logging in to remote systems, and transferring files. Products are available to supply access to HyperChannel and IBM's SNA networks by means of gateways.

Licenses to use HP Basic/UX cost $995. Media and documentation cost $305. Delivery is in 8 weeks.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, CA 94303; call local Hewlett-Packard sales office. **CIRCLE 361**

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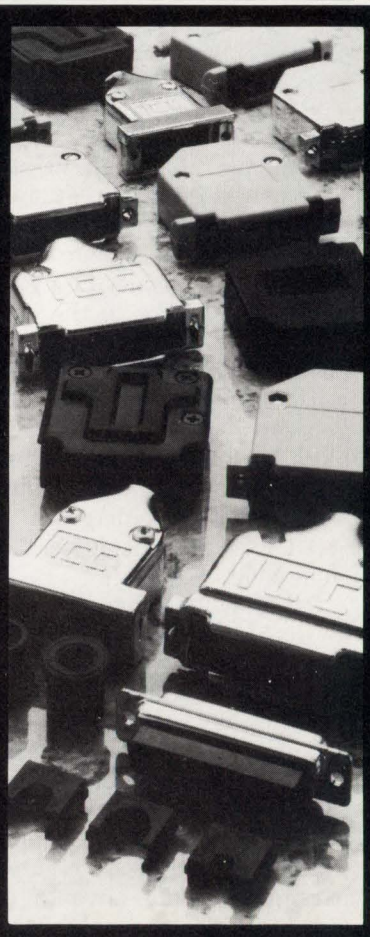


CIRCLE 61

SOFTWARE MODULE MASSAGES ANALOG DATA UNDER WINDOWS

Display, manipulation, analysis, and reporting of acquired analog data are among the capabilities of the View II software module from Gould. Written to run under Microsoft Windows, the module is designed to perform flexible display functions that enhance the visual interpretation of waveforms.

Special editing and annotation functions are used to identify, segment, and define data of interest while basic math and calculus functions complement the visual interpretation of data.

With the module's graphic functions, users can view from one to 16 channels of data derived from either single- or multiple-device channels, and from different devices and/or tests. With support for over 1 Gsample per channel, the software can handle up to 16 Gsamples of data.

The X and Y axes can be expanded or compressed. A window of X- and Y-axis information can be displayed for each channel, using a cursor as a reference point. Data includes the axis values at cursor and axis spans, as well as the time and the date of trigger (acquisition).

The color of each displayable item may be specified, as well as per-channel definition of display size and position. Also, a set of horizontal and vertical graticules with from one to 99 divisions can be set up.

Default settings can be defined for the basic math and calculus functions, annotation, plotter settings, and the data segmenting. Sine, triangle, and square waves can be generated for reference and comparison. Displays can be output to printers, plotters, or any device with an MS-Windows driver. This is accomplished while taking advantage of the full resolution of the output device.

The View II software module costs $2000. Delivery is in 90 days.

Gould Inc., Test and Measurement Division, 3631 Perkins Ave., Cleveland, OH 44114; (216) 361-3315. **CIRCLE 311**

BOARD-LEVEL INSTRUMENTS PLUG INTO PC SLOTS, BYPASS PROGRAMMING

Plugging directly into any IBM PC, PC XT, PC AT, or compatible's I/O slot, a series of board-level instruments from Metrabyte offer bench-top/rack-mounted features, functions, and performance without the programming hassles of an IEEE-488-based system, and at a fraction of the cost. The PCIP-DMM, a 4-1/2-digit multimeter, and the PCIP-SST, a 5-MHz function generator, eliminate the communication interface, display circuitry, cabling, and power supply required for dedicated IEEE-488 systems.

The PCIP-DMM multimeter offers users five functions in 19 ranges: dc and ac volts, dc and ac amps, and resistance measurements. Features include ±0.03% accuracy, fully isolated inputs, overload protection, 10-MΩ input impedance, and a built-in data-logging capability.

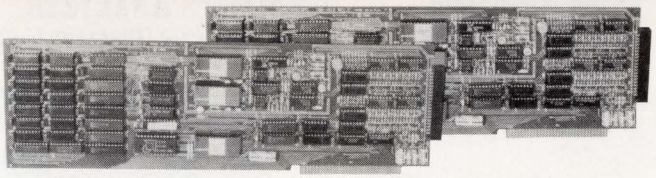
Sine, square, and triangular output waveforms are among the capabilities of the PCIP-SST 5-MHz function-generator board. Other features include 20-V pk-pk amplitude capability, a 50-Ω output impedance, and ±0.5% frequency accuracy. Connections are made through three standard BNC connectors.

These instruments operate in either of two modes: bench emulation or programmed, which simulate IEEE-488 local and remote operation, respectively.

The PCIP-DMM digital-multimeter board and PCIP-SST function-generator board cost $699 and $999, respectively, in quantities from 1 to 9. Delivery is from stock.

Metrabyte Corp., 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3000. **CIRCLE 312**

12 bit, 1 Mhz
Waveform Digitizer
16 bit, 250 Khz
Waveform Synthesizer



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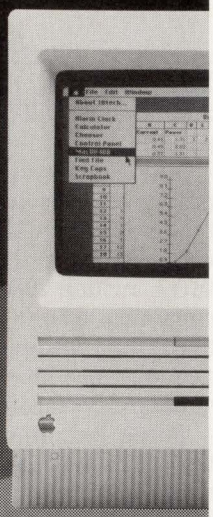

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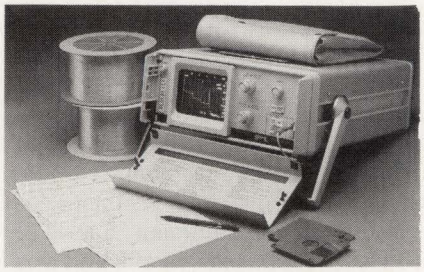
CIRCLE 64

OTDR Has A Range To 28 dB At 1300 nm

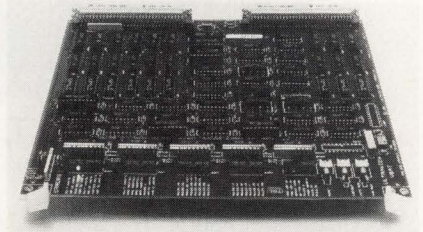


Equipped for single-mode, multimode, and dual-wavelength capabilities, the 3100X optical time-domain reflectometer (OTDR) has a range of up to 28 dB at the 1300-nm wavelength with less than one minute of averaging. The ability to see splices and faults as close as 150 meters is the result of a shorter dead zone. Pulse widths of 25, 50, 100, 250, and 1000 meters optimize measurement accuracy. Applications include the installation, restoration, and maintenance of public and private telecommunications networks. An optional data logging and signature-analysis package is available.

Photon Kinetics Inc., 9350 Southwest Gemini Dr., Beaverton, OR 97005; (503) 644-1960. From $24,250. Delivery is in four weeks.

CIRCLE 313

VMEbus Analyzer Diagnoses Timing Faults

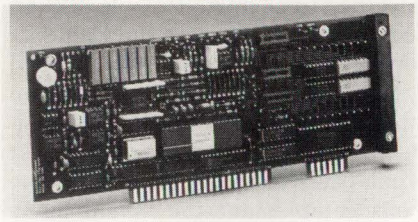


Designed to determine the presence of VMEbus timing faults, the A14591 VME Bus Analyzer identifies 104 different faults in 27 classes. When a fault is observed by the analyzer, an LED is lit. When the board is used in conjunction with a logic analyzer, the bus analyzer triggers the logic analyzer to determine the source of the fault. Once triggered, the logic analyzer can display the bus signals with 5-ns resolution. The analyzer board can be plugged directly into any available slot of the VME bus.

Gould Inc., Test and Measurement, 3631 Perkins Ave., Cleveland, OH 44114; (800) 538-9320. $2000. Avail. is eight weeks.

CIRCLE 314

Card Offers 50-kHz Throughput



Offering 50-kHz throughput and 16-bit resolution, the AMM2 analog-measurement module performs analog input, signal conditioning, and analog-to-digital data conversion. Its features include 16 single-ended or eight differential analog inputs, a crystal-controlled oscillator, and an external trigger capability. Programmable operating parameters include gain, input filter, and input configuration, and a programmable input filter with cutoff frequencies of 2 kHz or 100 kHz that improves low-level measurements by minimizing the effects of external noise.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (216) 248-0400. $1125. Availability is two weeks. **CIRCLE 315**

SMD Adapter Simplifies LCR Testing

The PM 9542 surface-mount device (SMD) test adapter, used in conjunction with the PM 6303 automatic LCR meter, allows for simplified testing of components that range from 2 to 10 mm in length. With its spring-loaded fixture clips, proper alignment is made easy for measurements of inductance, capacitance, and resistance of individual passive components. The adapter comes complete with the cable which is needed to connect it to the meter.

John Fluke Mfg. Co. Inc., P.O. Box C-9090, Everett, WA 98206. (800) 443-5853 ext. 77. $90. Available immediately. **CIRCLE 316**

500-V MOSFET HANDLES 50 USABLE AMPS

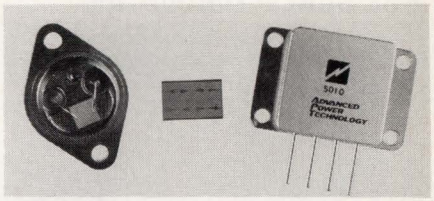
A record 50 A of usable current and an on-resistance of 0.1 Ω make the APT5010FN 500-V MOSFET from Advanced Power Technology a likely candidate for power-supply and motor-control circuits in military and commercial systems. The part supplies twice the usable current that is available from conventional MOSFETs with comparable voltages.

Based on the company's Power MOS IV technology, the device combines its high power with exceptional switching speed. Input capacitance is just 6000 pF, about half the drive requirement of conventional MOSFETs configured for comparable currents.

The company is also introducing a 450-V version of the part, the APT4510FN, with all other specifications remaining similar to those of the APT5010FN. The pair expand power MOSFETs into the realm of bipolar, high-power transistors and thyristors. With these 50-A MOSFETs, users can build simpler, more reliable power-supply and motor-control circuits than has been possible with either bipolar power transistors, thyristors, or MOSFETs in parallel configurations.

Both the 500-V APT5010FN and the 450-V APT4510FN are built on a 388-by-588-mil die in a hermetically sealed package. The parts are 0.330 in. tall, 1.125 in. wide, and 1.625 in. long packaged, and are also available in die form. The package can be mounted directly to a heat sink without the usual isolation practices needed with nonisolated packages.

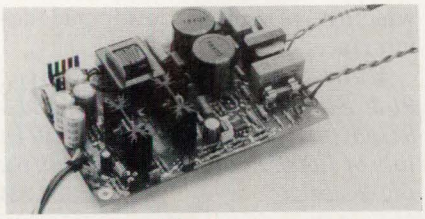
If used in place of bipolar power transistors, the 500-V and 450-V MOSFETs permit designers to simplify control schemes. When used in place of thyristors, these fourth-generation devices free designers from the complexities of commutation circuits in their systems. With their higher current-handling capabilities, the MOSFETs simplify the task of paralleling several devices to control high currents, because it takes fewer to do the same job.



The APT5010FN costs $149.88 and the APT4510FN goes for $115.83, both in quantities of 1000 and with full military screening. Delivery is in 4 to 6 weeks in either packaged or die forms.

Advanced Power Technology, 405 S.W. Columbia St., Bend, OR 97702; (503) 382-8028. **CIRCLE 362**

UNIT POWERS HALF-HEIGHT DRIVES

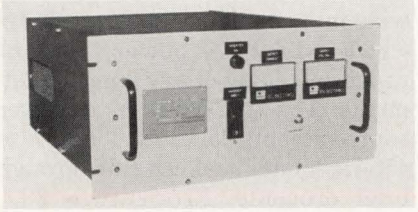


Equipped with dual outputs, an open-frame power supply features an exceptionally low profile, making it an ideal candidate for powering half-height tape and disk drives. The 9M23 delivers sufficient peak power to drive a $3\frac{1}{2}$-in. or $5\frac{1}{4}$-in. floppy- or hard-disk drive, or it can be used with a $\frac{1}{4}$-in. tape drive. It is rated for +12 V at 1.6 A continuous and 3 A peak, while the fully regulated second output handles +5 V at 0.7 A. Overvoltage and overload protection are standard on each output, with a minimum hold-up time of 16 ms. The supply has a footprint of only 1.1 by 3.75 by 5.75 in.

Valor Electronics Inc., 6275 Nancy Ridge Dr., San Diego, CA 92121; (619) 458-1471. $60 for single units, dropping to $25 in OEM quantities. **CIRCLE 317**

INVERTER OPERATES FROM 48-V BATTERY

The model G2K60-48 inverter employs sine pulse-width modulation and is designed to operate from a battery or generator over an input range of 42 to 54 V dc. It produces 120 V ac output at 60 Hz with a low distortion sine wave output. It is designed for applications where ac power is unavailable or with an existing battery supply to provide uninterrupted power to critical loads. Output voltage regulation is ±1%

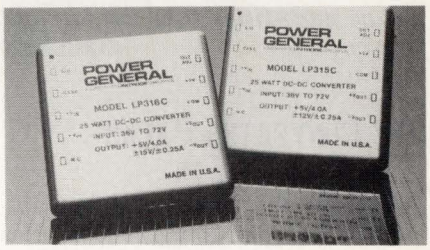


from no load to full load. Frequency regulation is ±0.5%. It can supply loads with a power factor of 0.7 lead to 0.7 lag. An optional electro-mechanical or solid transfer switch is available.

Nova Electric Inc., 263 Hillside Ave., Nutley, NJ 07110; (201) 661-3434. $4,140. Delivery is four weeks from date of order. **CIRCLE 318**

CONVERTERS BOAST LOW-PROFILE DESIGN

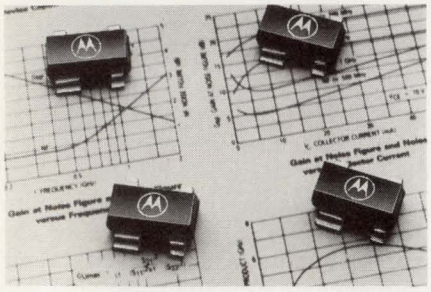
A series of low-profile, wide-input-range, 25-watt dc-dc converters feature 0.375-in. maximum height, 7.7 watts/in.^{3}, 2 to 1 input voltage range,



and 25 watts at the output. Applications of the LP-315/316 series converters include telecommunication equipment, portable battery-operated equipment, and computer peripherals. Its surface-mount design reduces the overall thermal operation of the unit, resulting in a mean time between failures of 300 khours. It is packaged in a 3-in. by 3-in. by 0.375-in fully shielded metal case which allows single-card slot mounting.

Power General, 152 Will Dr., P.O. Box 189, Canton, MA 02021; (617) 828-6216. $219. Availability is stock to four weeks. **CIRCLE 319**

TRANSISTOR PACKAGED FOR SURFACE-MOUNTING



Designed primarily for use in high-gain, low-noise small-signal amplifiers, the MRF0211 RF transistor is manufactured in a four-lead surface-mount package for improved gain and automated assembly. The transistor, which can operate at frequencies up to 3.5 GHz, features a high current gain bandwidth of 5.5 GHz, a collector-base capacitance of 0.7 pF, a collector-emitter breakdown voltage of 15 V minimum, and a maximum collector current rating of 70 mA. It is available in both standard and low profile configurations and tape and reel options.

Motorola Inc., Semiconductor Products Sector, P.O. Box 52073, Phoenix, AZ 85072; (602) 244-3818. $0.88 for quantities over 100. Small quantities available from stock. Large quantities take six to eight weeks. **CIRCLE 320**

DC CONVERTER PACKS 2 W IN 1 BY 2 IN.

Available with single- and dual-outputs of 5, 12, and 15 V, the ITS series of 2-W isolated dc-dc converters comes in a package that is only 1 by 2 by 0.4 in. It also provides a wide input voltage range of 18 to 70 V dc to cover 24-, 36-, 48-, and 60-V batteries or compensate for long input line drops in telecommunication applications. Each unit in the series is equipped with 500 V of isolation, as well as protection against continuous short circuits and output overvoltage. Typical operating efficiency is rated at 80%.

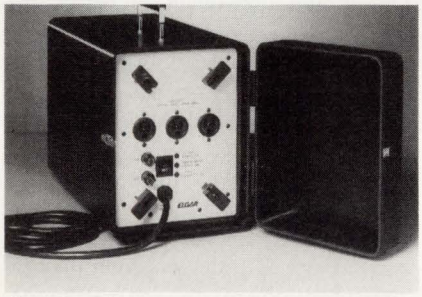
Melcher Inc., 10 Cochituate St., Natick, MA 01760; (617) 653-9979. $68.50 (100 units); small quantities are from stock. **CIRCLE 321**

SWITCHER DESIGNED FOR USE IN OFFICE

The MAX-704 is a multioutput, self-cooled, high-performance switching power supply designed for high-end, computer-based office products. Housed in a low-profile package, it incorporates a heat-transfer technique that enables it to use the host system's air-flow cooling. This feature can significantly reduce audible noise by eliminating integral fan noise. The switcher delivers 700 W of power and provides 100 A of +5 V for logic and memory. Up to three auxiliary outputs provide high-efficiency, tightly regulated 12 V or -5.2 V at up to 20 A. Overload protection is provided on all outputs as is +5-V overvoltage protection.

Todd Products Corp., 50 Emjay Blvd., Brentwood, NY 11717; (516) 231-3366. $549 in quantities of 100. Delivery is stock to six weeks. **CIRCLE 322**

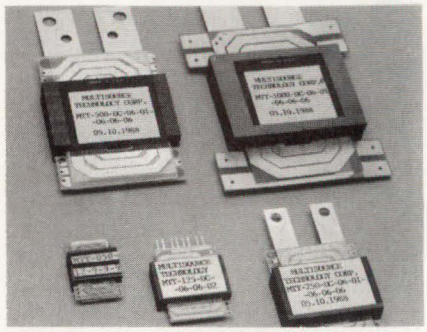
PORTABLE SOURCE PROVIDES 117 V AC



A portable ac power source converts unstable ac power anywhere world-wide into regulated 117-V ac, 60-Hz (±2%) sinewave power, without range switching or any other adjustments. The GPS 1000 W ac power source accepts 85- to 280-V ac, 47- to 450-Hz inputs, and can ride through brief dropouts. Efficiency is 80%. Three outlets are included. Optional input adapter cables for outlets used world-wide are available. Applications include powering of data processing, communications, or other sensitive electronic equipment at any remote locaion.

Elgar, 9250 Brown Deer Road, San Diego, CA 92121; (619) 458-0235. $2695. **CIRCLE 323**

TRANSFORMERS CUT SIZE, ADD EFFICIENCY



A new line of low-profile planar transformers and inductors shrink power supply size while providing high efficiency. Designated the Plan-R series, the transformers and inductors have a maximum height of 0.575 in. over the 50- to 1000-W range. Standard core material is a low-loss ferrite capable of 100-kHz to 300-kHz operation. High frequency units operate from 300 kHz to 1 MHz. Total power losses are typically less than 2% of rated power. The units, which are also ideal for resonant converters, can accomodate up to five windings, providing a low impedence interface.

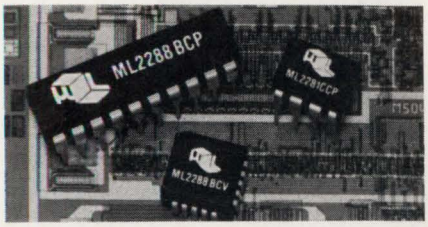
Multisource Technology Corp., 91-3 Staniford St., Newton, MA 02166; (617) 965-8668. From $7.50 in lots of 1,000. Prototype availability is 1-2 weeks. **CIRCLE 324**

AC POWER SOURCE SPANS 1.2 TO 15 kVA

Intended for powering motors and other high current-consuming loads, a line of frequency-changing, sinewave ac power sources supplies from 1.2 to 15 kVA in single-, two-, and three-phase configurations. Output voltage and frequency can be fixed or variable from 0 to 260 V ac and from 47 to 500 Hz. Harmonic distortion for units in the EL series is less than 2% at full load, and power factors of zero to unity have no effect on the sources. All models feature an efficiency rating of 80%.

Elgar Corp., 9250 Brown Deer Rd., San Diego, CA 92121; (619) 450-0085. Prices start at $2595. **CIRCLE 325**

8-Bit Serial-I/O ADC Easily Links With Microprocessors



Sampling an analog input signal at over 100 kHz and interfacing with a microprocessor at 1.33 MHz is within the reach of the ML2281 family of 8-bit serial-I/O analog-to-digital converter from Micro Linear. The successive-approximation converters boast a conversion time of 6 μs for efficient interfacing with DSP chips. Total unadjusted error is ±1/2 LSB or ±1 LSB, and an on-chip sample-and-hold features a 375-ns acquisition time.

The ML2281 family is an enhanced, double-polysilicon CMOS pin-compatible replacement for the ADC0831, ADC0832, ADC0834, and ADC0838 a-d converters. Four basic versions—the ML2281, ML2282, ML2284, and ML2288—differ by the number of input channels, which is indicated by the last digit of the model numbers. Enhancements include faster conversion times, true sample-and-hold function, superior power-supply rejection, improved ac common-mode rejection, and lower power dissipation.

Features include a zero-to-5-V analog input range with a single 5-V power supply and a maximum power dissipation of 12.5 mW. The converters can be operated ratiometrically, or witn an external voltage reference in systems that require absolute accuracy. The reference can be externally set to any value between ground and 5 V.

The ML2281 and ML2282 come in an 8-pin DIP, the ML2284 in a 14-pin DIP, and the ML2288 in both a 20-pin DIP and a 20-lead plastic chip carrier. Prices range from $2.95 to $4.65 in units of 100. Delivery is from stock.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; (408) 433-5200. **CIRCLE 326**

Fast, Accurate Op Amp Smooths Applications With Ease Of Use

Exceptional ac and dc characteristics are par for the course in the MSK 738 operational amplifier from M.S. Kennedy Corp. Features include a slew rate of 3500 V/μs and 20-MHz full-power bandwidth. Within the same TO-8 package, however, the MSK 738 amplifier exhibits high dc precision—on the order of an OP-07 device.

An input offset voltage of just 75 μV maximum (25 μV typical), a 1.0-μV/°C maximum drift coefficient (0.5 μV/°C typical), and an input noise voltage of 0.15 μV pk-pk (typical from 0.1 to 10 Hz) make the device a standout performer. The amplifier's settling time is 30 ns to 1%, 40 ns to 0.1% (guaranteed), and 200 ns to 0.01% (typical) for a full 10-V step.

The amplifier is distinguished by its ease of use, because of its unity-gain stability and compensation scheme consisting of a single capacitor whose value is independent of the gain setting.

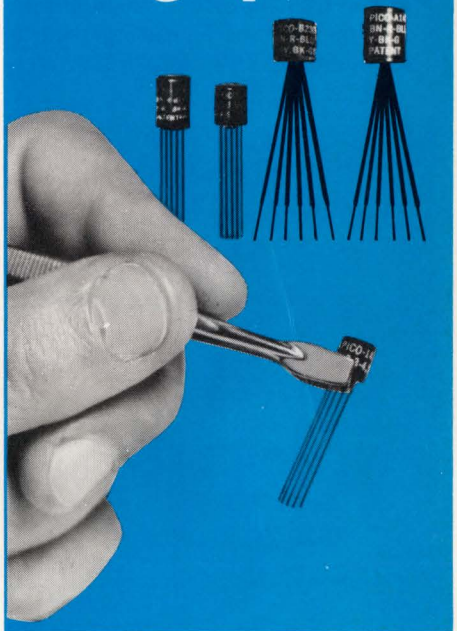
The slew rate and bandwidth specifications are both guaranteed minimums under the device's full rated output of ±10 V into 100 Ω. That translates into 100 mA of continuous high-speed output for driving a capacitive load.

Because of the op amp's extremely low initial input-offset voltage and ultra-low offset-voltage drift, the MSK 738 can be used at very large gains without ac coupling. Trim potentiometers can be eliminated from most applications and the user need not worry about system-performance changes with respect to temperature. With its continuous ±100-mA output capability and fast guaranteed settling time, the part is suited for high-performance data-acquisition circuits.

Prices start at $140 for the full military version and $85 for the industrial version. In quantities of 5000, the commercial version costs $25. Small quantities are delivered from stock.

M.S. Kennedy Corp., 8170 Thompson Rd., Clay, NY 13041; (315) 699-9201. **CIRCLE 327**

PICO transformers ... small size ...big specs



- size variations of .25" dia. x .25" to .75" dia. x 82" ht.
- MIL-T-27E (PICO is QPL source)
- 20Hz —250KHz
- pulse applications .05μs to 100μs
- prim. and sec. impedances 2 ohms to 250K ohms
- power to 3 watts
- inductors to 80 henries
- plug-in construction, surface mount, or flying leads
- extreme resistance to thermal shock MIL-STD-202F, method 107(25 cycles). Special designs for 300 cycles.

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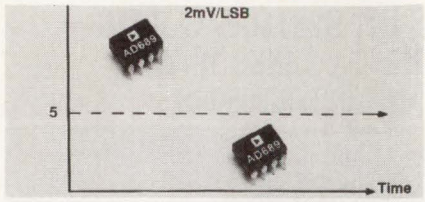
CIRCLE 66

VOLTAGE REFERENCE MAXIMIZES RESOLUTION FROM 12-V SUPPLY

The highest effective resolution for systems operating from a nominal 12-V supply is provided by the AD689 +8.192-V reference from Analog Devices. Unlike +10-V references that cannot operate reliably at the lower limit of a 12-V, ±10% supply, the AD689 is guaranteed to operate with supplies as low as 10.8 V.



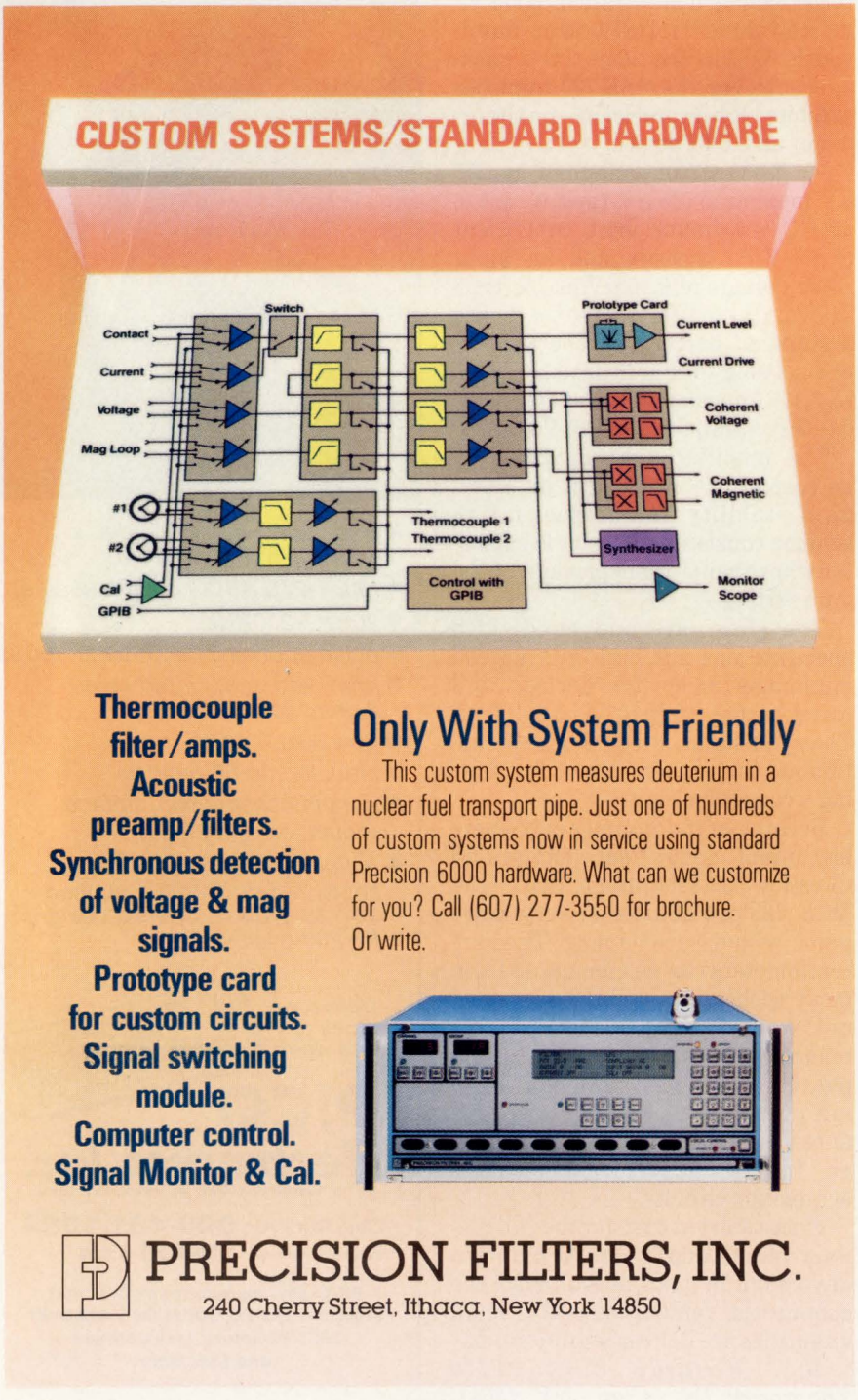
The AD689 reference delivers 2-mV/LSB resolution for 12-bit converters, which is about 164% of the 1.2207-mV/LSB resolution of a 5-V reference. Force and Sense connections on the monolithic device permit remote sensing of the load and ground voltage to maintain accuracy of the reference value at the load. The Force and Sense connections can also be used to conveniently boost output current with a high-current transistor connected inside the loop at the reference output or at the load. The chip is designed for operation as a complete buffer-amplifier reference; no additional components are required for operation. This considerably reduces board-space requirements and improves the reliability of the entire system.

Initial accuracy is laser-trimmed to within ±4 mV to ±16 mV, depending on the grade. An optional fine-trim connection enables the output voltage to be adjusted +8%, –3%, for higher accuracy or a precise 8.000-V reference value. Peak-to-peak noise is typically below 2 μV from 0.1 to 10 Hz; wideband noise (to 1 MHz) is typically less than 400 μV pk-pk and can be cut to less than 200 μV with an external capacitor.

Maximum temperature drift is from 5 ppm/°C to 25 ppm/°C, with the smallest drift in the highest-accuracy grade. A 15-ppm/1000-hour typical long-term drift assures stability over time. This reference, available for temperature ranges of zero to +70°C and –55 to +125°C, is packaged in an 8-pin hermetic ceramic DIP.

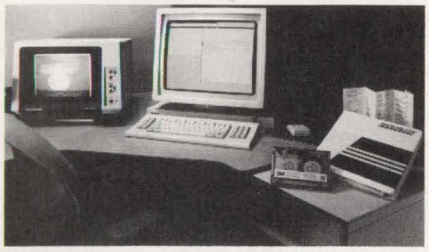
In quantities of 100, prices for the AD689 voltage reference start at $2.95 and range to $6.50 for the highest non-military grade. Delivery is from stock.

Analog Devices Semiconductor, 804 Woburn St., Wilmington, MA 01887; (617) 935-5565. **CIRCLE 328**



CIRCLE 67

UNIX SOFTWARE PROCESSES IMAGES IN REAL TIME ON SUN WORKSTATIONS



A Unix-compatible software package from Data Translation gives C, Pascal, and Fortran programmers powerful image-processing tools and complete software support for the company's frame-grabber and frame-processor boards. The DT-IRIS package, which is designed for use on Sun-3 workstations, includes subroutines that can perform real-time medical imaging, machine inspection, document image editing, and various other scientific, industrial, and graphics applications.

With the package, users can acquire images into the Sun workstation from a video source, such as a video camera, VCR, or even a CAT scanner, for storage, processing, and display. Most operations execute at a real-time rate of 30 frames/s. Simple operations involve just digitizing, storing, and displaying images, from one video source or from several at a time.

Images can be zoomed into for close-up examination, or hard-to-see regions in an image can be displayed with false color for emphasis. The software also supplies graphics capabilities to create text labels, box windows in an image, or mix boxes, circles, and lines with video images. For sophisticated image processing, there are several predefined convolutions that implement a number of image-enhancement filters.

The software supplies an interface to the workstation's Unix operating system and to the company's DT1451 high-resolution frame-grabber and DT1458 auxiliary frame-processor boards. The package takes control of system service calls and memory mapping, as well as management of virtual-memory operations.

The DT-IRIS package for the Sun-3 workstation costs $1995 for the initial license, with subsequent licenses costing $695 each. Delivery is within 5 days.

Data Translation, 100 Locke Dr., Marlboro, MA 01752; (617) 481-3700. **CIRCLE 329**

MULTIBUS SOFTWARE PROVIDES X.25 LINK

Including an application interface library and an interactive utility program, a software package permits the interconnection of systems based on the Multibus I to X.25 packet-switched communication networks. It offers user-configurable baud rates (0.3 to 64 kbaud) with support for up to four physical links and 255 configurable virtual circuits. The software routines provide flexibility in accessing packet-switched networks, allowing host computer access as a DTE or DCE device. The Multibus I X.25 software runs on a Multibus system equipped with an iSBC 188/56 board and running the iRMX real-time operating system.

Intel Corp., Literature Department #W420, P.O. Box 58065, Santa Clara, CA 95052; (800) 548-4725. $1300. **CIRCLE 330**

TOOLKIT OPTIMIZES 80386 DEVELOPMENT

A family of native and cross development tools is designed for use with the 80386 microprocessor. The integrated toolkit, based on Green Hills C, Pascal, and Fortran compilers and complementary assembler-linker options, is available on VAX (VMS or Ultrix), Sun, and other 68000-based systems, as well as IBM PC, Compaq Deskpro 386, and 80386-based workstations. Compilers in the Oasys 80386 development kit use global optimization techniques and employ superior register allocation in generating code. Full support is provided for two floating-point units, the Intel 80387 and Weitek 1167.

Oasys, a division of XEL Inc., 230 Second Ave., Waltham, MA 02154; (617) 890-7889. **CIRCLE 331**

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DC-DC CONVERTERS
Wide Input Range
5 to 60V DC

Regulated
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- 230 Standard Models
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- All Units Shielded
- 500V DC Isolation Input to Output

OPTIONS AVAILABLE
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CIRCLE 66

MACINTOSH TOOL DESIGNS ICs ON DESKTOPS

The interactive design of ICs and hybrids, from initial concept to documentation, is now available to Macintosh users thanks to DKL Technology's MacGDS design system. The software runs on a standard Macintosh with a minimum of 512 kbytes of RAM, making it a cost-effective CAD workstation.

With its menu-driven design format and editing functions, MacGDS users can create layouts intuitively for optimum throughput. Keyboard equivalents for menu commands are supplied for maximum productivity as the user becomes familiar with the program. By adhering to established Macintosh data formats, compatibility of files with word processing, graphics, and page-layout programs for documentation needs is guaranteed.

The program offers 99 hierarchical levels for virtually unlimited structure nesting. It supports basic metric and imperial units of measurement from microns to miles, with further subdivision for resolution of less than 10 angstroms. Large-screen color or monochrome displays are supported up to 19 in. with up to 1664 by 1200 pixels of resolution.

A palette command gives complete flexibility to design and set a contour/fill pattern, line width, and color combinations on a layer-by-layer basis. Two different sets of choices can be created and saved along with the file library. Pattern interference permits accurate display of multiple layers on a monochrome monitor without sacrificing clarity.

Also, a continuously variable zoom capability from one to 1200 times is coupled with comprehensive view commands and panning, layer selection, and multiple windowing capabilities to let users focus precisely on the item being worked with. Symbolic versus physical representation is supported, along with a mask function for edit locking and visibility selection by layer.

The software automatically calculates the area, perimeter, and length of selected paths and boundaries. Because square, octagonal, vector, and arc digitizing modes can be used in any combinations, designers can create any desired shape.

In single quantities, the MacGDS design tool costs $8200. The price decreases to $5100 for ten users. Availability is from stock.

DKL Technologies Inc., 11 Donex St., Pointe-Claire, Quebec, Canada H9R 4Z3; (514) 694-9773. **CIRCLE 335**

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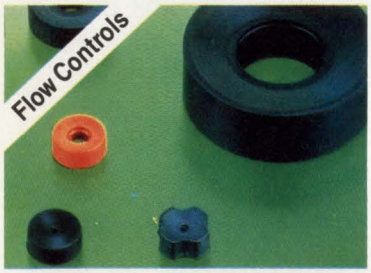

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CIRCLE 68

CMOS EEPLD Substitutes For Popular Earlier Device

The first CMOS EEPLD version of the 20RA10 architecture has emerged, yielding a low-power alternative to Advanced Micro Devices' PAL20RA10. The PALC20RA10Z, which is a product of a joint effort between AMD and Seeq Technology, boasts a zero-power standby mode with a maximum current draw of 150 μA. With an operating current of only 5 mA/MHz, the part is suited for battery-operated applications and battery-backup systems, portable computers, and handheld devices. It will also find applications in military, industrial, and telecommunication systems.

The CMOS chip features 10 registered asynchronous macrocells, each of which can be clocked, set, reset, or bypassed individually, which gives users the maximum flexibility that is needed in system design. Also, two speed versions are available containing propagation delays of 40 and 45 ns.

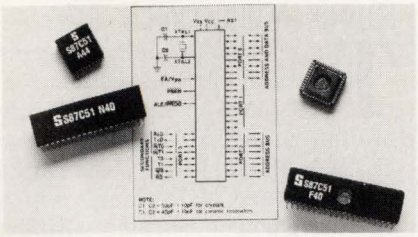
The part owes its extremely low standby current to a grounded substrate. Also, the electrically erasable CMOS technology eliminates the need for windowed packages, which reduces cost. Reprogrammability not only reduces development and field-retrofitting costs, but also guarantees 100% testability and field programmability.

Both speed versions come in 300-mil-wide plastic and ceramic DIPs, and will be available in plastic leaded chip carriers later this year. The AMD PALC20RA10Z goes for $13.45 for the 40-ns version and $9.90 for the 45-ns version. The Seeq Technology PQ20RA10Z costs $15.40 and $11.90 for 40- and 45-ns versions, respectively. All prices are for quantities of 100, and small quantities are available from stock.

Advanced Micro Devices Inc., 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088-3453; (408) 732-2400 **CIRCLE 332**

Seeq Technology Inc., 1849 Fortune Dr., San Jose, CA 95131; (408) 432-9550. **CIRCLE 352**

8-Bit Microcontroller Sources 87C51



The S87C51 is an 8-bit CMOS microcontroller that has applications in a broad range of fields, including data processing, consumer electronics, industrial tasks, telecommunications, and automotive systems. Features include a 4-kbyte-by-8-bit EPROM, a 128-by-8-bit RAM, two 16-bit counter-timers, a full-duplex serial channel, and a Boolean processor. Dual 64-kbyte address spaces let the programmer separate the program memory from the data and I/O addresses. The controller, which is fully TTL compatible, offers 32 I/O lines, two 16-bit counter-timers, and a five-source, two-priority-level, nested interrupt structure, and also contains an on-chip oscillator and clock circuits.

Signetics Corp., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088; (408) 991-2000. $45 in quantities of 100. Availability is from stock. **CIRCLE 333**

SRAM Modules Combine Speed And Compactness

Featuring thinner profiles and denser form factors, a family of static RAM modules is designed for use in super-minicomputers, RISC-based systems, high-end personal computers, workstations, test equipment, and embedded controllers. Offering access speeds as low as 20 ns and densities as high as 512 kbits, the SSMM91000 family requires only 25% of the board space normally needed. The module is packaged in a 28-pin plastic DIP, a 38-pin ZIP, or a 60-pin ZIP.

Saratoga Semiconductor, 10500 Ridgeview Court, Cupertino, CA 95014; (408) 864-0500. From $171 in quantities of 100. Available immediately. **CIRCLE 334**

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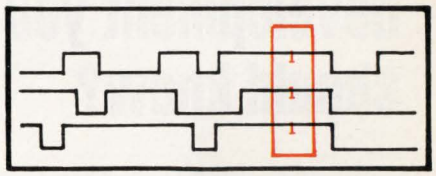

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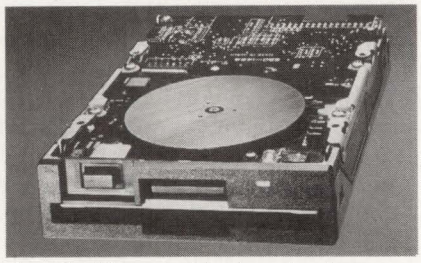
CIRCLE 70

2.0-MBYTE, 3.5-IN. FLOPPY DRIVE HANDLES SEVERE SHOCK, VIBRATION

The only 3.5-in. microfloppy disk drive available specified for a 60-G non-operating shock/vibration rating for 11 ms is Canon U.S.A.'s MD3611 drive. The rugged unit relies on CMOS circuits with an operating power consumption of just 1 W typical and 20 mW typical in stand-by mode.

Applications for the drive include portable and laptop computers as well as desktop models. The dual-mode 1.0/2.0-Mbyte drive, which combines phase-correction circuitry with a wide gap-length head, is guaranteed to be fully compatible with conventional 1-Mbyte drives. An oil-damping mechanism performs hydraulic-like cushioning to improve head reliability and data integrity.



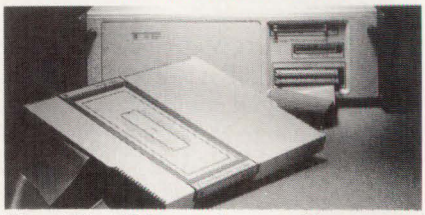
Key specifications include a track-to-track access time of 3 ms and a seek settling time of 15 ms maximum. Average access time is 94 ms. The drive transfers 500 kbits/s in the 2-Mbyte mode and 250 kbits/s in the 1-Mbyte mode. Disk rotational speed is 300 rpm with a latency of 100 ms. The dual-head drive offers a track density of 135 tracks/in.

Other features of the drive include a dust shutter, automatic disk ejection, and a dual-color LED to indicate which density mode is in operation. An optional dust cover for portable uses is also available. The drive stands 1 in. high and weighs about 15 ozs.

Evaluation samples of the MD3611 disk drive with a documentation kit are available immediately for $100 each.

Canon U.S.A. Inc., Components Division, One Canon Plaza, Lake Success, NY 11042; (516) 488-6700. **CIRCLE 336**

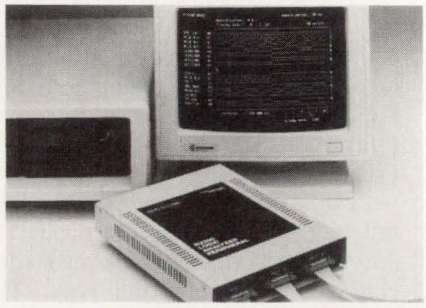
ZERO-WAIT EMULATION PROVIDED AT 16.7 MHZ



The ES 1800 emulator offers zero-wait state in-circuit 16.7 MHz emulation for the 68000 microprocessor. This easy-to-use unit operates with such computers as Sun, Apollo, VAX, IBM PCs, and compatibles. The emulator features an advanced event monitoring system that allows for easier control engineering by breaking on any combination of address, data status, pass counter, and logic state fields. Also included is a low profile tip that supports the DIP and PLCC packages. An optional computer-systems interface provides a faster data transfer rate.

Applied Microsystems Corp., 5020 148th Ave. N.E., P.O. Box 97002, Redmond, WA 98073; (206) 882-2000. **CIRCLE 337**

PC LOGIC ANALYZER RUNS AT 100 MHZ



Designed to provide flexibility, the R3200 PC-based logic analyzer can be used with 8 channels at 100 MHz, 16 channels at 50 MHz, or 24 channels at 25 MHz. Features include store, retrieve, and print waveforms, waveform zooming, timing and state analysis, internal sampling, and advanced triggering. Applications include logic simulation, automatic test equipment use, software development, and logic analysis.

Rapid Systems Inc., 433 N. 34th St., Seattle, WA 98103; (206) 547-8311. $1995. **CIRCLE 338**

CABINET, CASE, AND ENCLOSURE CATALOG

The 1988 standard products catalog from Zero Corp. includes the company's broad range of deep-drawn aluminum boxes and covers, carrying cases, instrument enclosures, military cases and cabinets, card files, chassis slides and accessories, commercial and industrial electronic cabinets and consoles, shock-mounted instrument cases, blowers and cooling systems, refrigerated air conditioners and heat exchangers, and more. A complete generic and trade name product reference is also included.

Zero Corp., 777 Front St., Burbank, CA 91503; (818) 846-4191.

CIRCLE 339

COOLING-FAN PRODUCTS CATALOG

Included in this detailed technical catalog are cooling fan products for a wide variety of applications, ranging from office copiers and microcomputers, to laboratory instrumentation and industrial control cabinets. Detailed performance specifications, dimensional data, specific product features, and available product options are featured in the publication.

Globe Motors, 2275 Stanley Ave., Dayton, OH 45404; (513) 228-3171. **CIRCLE 340**

CHIPS FOR POWER APPLICATIONS

P.T.C. has issued a power semiconductor-device catalog covering their full line of transistors, Darlingtons, and power diodes. Three categories are covered: high-voltage NPN transistors with current ratings of 2.5 to 15 A and voltage ratings from 200 to 1500 V; high-voltage NPN Darlingtons available with current ratings of 10 to 50 A and voltage ratings from 350 to 1000 V; and power diodes with fast recovery times and with current ratings of 40 to 50 A and voltage ratings from 200 to 1200 V.

Power Technology Components, 23201 South Normandie Ave., Torrance, CA 90501; (213) 534-3737.

CIRCLE 341

RESISTIVE COMPONENT SELECTION GUIDE

A compact catalog featuring specifications and applications information for trimming potentiometers, panel controls, resistor networks, and chip resistors is available. Featuring all the most popular styles, it provides the element type, resistance range, and package configuration for each component. Component schematics are also given.

Bourns Inc., 1200 Columbia Ave., Riverside, CA 92507; (714) 781-5500. **CIRCLE 342**

INTEGRATED CIRCUITS DATA BOOK

The *IC Data Book* from Siliconix presents complete data sheets for the company's IC line in an easy-to-read format. Types of ICs include data conversion, power conversion, display drivers, analog switches, and multiplexers. The publication includes more than 50 new products. Selector charts and cross references enable design engineers to specify components by function, performance, or industry-standard part numbers, and an electrical-table format simplifies the specification of key parameters.

Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, CA 95054; (408) 988-8000. **CIRCLE 343**

ANNUAL ELECTRONIC MARKET DATA BOOK

The *Electronic Market Data Book 1988* is an annual statistical encyclopedia which discusses the electronics industry. The 1988 edition supplies the latest facts and figures covering consumer electronics, communications equipment, computers and industrial electronics, government electronics, foreign trade, employment, and research and development. It contains numerous statistical tables and graphs, and detailed explanations of market trends. It is priced at $88.

EIA Marketing Services Dept., 2001 Eye St., N.W., Washington, D.C. 20006; (202) 457-4955.

CIRCLE 344

INDUSTRIAL AUTOMATION GUIDE

A comprehensive single-source reference on the use of IBM-compatible and Macintosh personal-computers in industrial automation includes 700 products from 300 vendors, representing every major application and technology. This 102-page guide includes application software, PC hardware, and industrial computers. Applications discussed are process-monitoring control, data acquisition, and cell control. The purchase price is $39.95.

Synopsis Corp., 2708 Salisbury Plain, Raleigh, NC 27612; (919) 872-5309. **CIRCLE 345**

REPORT ON PARALLEL PROCESSING ANALYSIS

The Impact of Parallel Processing on High Performance Computing is a 298-page report that analyzes parallel-processing architectures, applications, software-development strategies, and end-user markets. It goes into great detail for each one of these topics and many others. Figures, tables, and a glossary of terms enhance the reader's understanding. The report costs $1485.

Electronic Trend Publications, 12930 Saratoga Ave., Suite D1, Saratoga, CA 95070; (408) 996-7416.

CIRCLE 346

1988 SEMICONDUCTOR HANDBOOK

The *1988 Master Selection Guide*, a comprehensive catalog of National Semiconductor Corp.'s product line, is a 462-page guide consisting of condensed specifications, block diagrams and packaging information on semiconductor products including the company's ICs and devices added as a result of the Fairchild acquisition. The guide includes sections on advanced peripherals, application-specific ICs, microcontrollers, microprocessors, power and discrete devices, and telecommunications.

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 749-7377. **CIRCLE 347**

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UPCOMING MEETINGS

SEPTEMBER

International Test Conference 1988 (ITC), September 12-14. Sheraton Washington Hotel, Washington, DC. Doris Thomas, International Test Conference, P.O. Box 264, Mount Freedom, NJ 07970; (201) 895-5260.

OCTOBER

Fiber Optic Sensors, October 3-4. Hotel Royal Plaza, Orlando, FL. Technology Training Corp., Dept. FOS, P.O. Box 3608, 3420 Kashiwa St., Torrance, CA 90510-3608; (213) 534-3922.

IEEE 1988 Ultrasonics Symposium, October 2-5. McCormick Center Hotel, Chicago, IL. William O,Brien, Bioacoustics Research Laboratory Computer Engineering, University of Illinois, 1406 W. Green St., Urbana, IL 61801; (217) 333-2407.

Electronic Imaging Conference East '88, October 4-6. World Trade Center, Boston, MA; (800) 223-7126 or (617) 232-3972.

ITEA Symposium '88, October 5-7. Clarion Hotel, Colorado Springs, CO. Richard Snell, 1988 ITEA Symposium, P.O. Box 26248, Colorado Springs, CO 80936; (719) 576-2602.

Frontiers of Massively Parallel Computation, October 10-12. George Mason University, Fairfax, VA. James Fischer, Image Analysis Facility, Code 635, NASA/Goddard Space Flight Center, Greenbelt, MD 20771; (301) 286-9412.

Fall National Design Engineering Show and Conference, October 11-14. Javits Convention Center, New York, NY. Janet Schafer, Cahners Exposition Group, 1350 E. Touhy Ave., Des Plaines, IL 60017; (312) 299-9311.

IMEKO XI and ISA/88, October 16-21. Astrohall, Houston, TX. Instrument Society of America, 67 Alexander Dr., P.O. Box 12277, Research Triangle Park, NC 27709; (919) 549-8411.

DEXPO West '88, October 18-20. Disneyland Hotel, Anaheim, CA. Susan Werlinich, Expoconsul International, Inc., 3 Independence Way, Princeton, NJ 08540; (609) 987-9400.

Fifteenth Annual National Energy Division Conference, October 23-26. Palacio del Rio Hilton Hotel, San Antonio, TX. Charles Mills, Martin Marietta Energy Systems, Inc., P.O. Box Y, 9201-3, MS-002, Oak Ridge, TN 37831; (615) 574-0410.

Fifth Annual Flat Information Displays Conference & Exhibition, October 24-25. Santa Clara Convention Center, Santa Clara, CA. Murray Disman, International Planning Information, 465 Convention Way #1, Redwood City, CA 94063; (415) 364-9040.

High Performance Inorganic Thin Film Coatings, October 30. Monterey Beach Hotel, Moterey, CA. Carolyn Davidson, Gorham Advanced Materials Institute, P.O. Box 250, Gorham, ME 04038; (207) 892-5445.

Ninth International Conference on Computer Communication (ICCC '88), October 30-November 4. Hilton Hotel, Tel Aviv, Israel. The Secretariat, ICCC '88, P.O. Box 50006, Tel Aviv 61500, Israel; 972/3/654571.

Seventh International Congress on Applications of Lasers & Electro-Optics, October 30-November 4. Santa Clara Convention Center, Santa Clara, CA. Larry Lotridge, OPTCON '88, 1816 Jefferson Pl., N.W., Washington, DC 20036; (202) 223-8130.

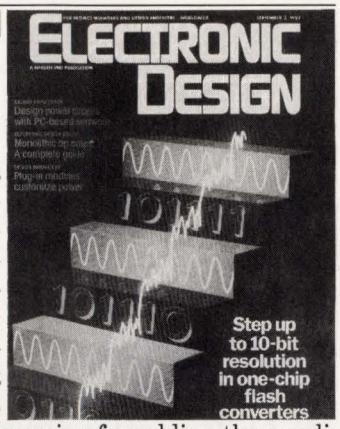
Autofact, October 31-November 2. McCormick Place East, Chicago, IL. Jill Vanderlin, SME, One SME Dr., P.O. Box 930, Dearborn, MI 48121; (313) 271-0023.

NOVEMBER

1988 IEEE GaAs IC Symposium, November 6-9. Opryland Hotel, Nashville, TN. William Roesch, TriQuint Semiconductor; (503) 644-3535, ext. 4143.

PUBLISHED SEPTEMBER 3, 1987

10-BIT FLASH ADC SHEDS A LINEAR AMPLIFIER



Leaving behind the process bugaboos that plagued it early in its history, Honeywell's HADC77600 10-bit flash analog-to-digital converter *(Sept. 3, 1987, p. 49)* is being readied in an optimized, less complex version for 1989. The 50-MHz flash converter was adorned at its introduction with a linear preamplifier with differential inputs and outputs that sat between each pair of input-signal lines to the chip's 1024 comparators. The company's reasoning for adding the amplifier was that there weren't any buffer amplifiers available that were deemed capable of driving the converter's input.

Since that time, however, Addacon Inc., of Greensboro, N.C., has come up with its AHT-1010 track-and-hold amplifier, which, according to Honeywell, does a great job of driving the 77600 converter's inputs. In fact, it does such a good job that the upcoming revision of the 77600 will appear sans linear preamplifier, saving on power consumption and heat dissipation. Not only that, the switch from an on-chip buffer amplifier to an off-chip track-and-hold will further boost the a-d converter's performance. Addacon will be offering its 30-MHz track-and-hold separately and, in the near future, packaged in a module with the 77600 converter.

In addition to removing the preamplifier, the converter is being examined "cell by cell" and optimized as necessary. Perhaps best of all, thanks to smoothing out of the company's 1.2-μm process, the chip's introduction price of $1295 in quantities of 100 has been pared down to a single-quantity price of $795. Addacon's AHT-1010 is available from stock to four weeks and costs $330 in quantities of 100 for the industrial-grade part.

FIRMWARE CHANGES BOLSTER SYNTHESIZER

At its introduction, Hewlett-Packard's HP 8904A digital synthesizer was already chock-full of functionality, generating sine waves up to 600 kHz, as well as square, ramp, and triangle signals to 50 kHz, white noise, and dc *(p. 75)*. The Palo Alto-based company now plans two special firmware options to add enhanced capabilities in the fm-stereo area as well as in signaling.

Although the 8904A generates fm-stereo signals with channel separation of better than 60 dB, doing so is a somewhat complicated process that involves adding channels. A special firmware option will do that for the operator. Soft keys will make the instrument function much like a dedicated stereo-signal generator.

A second special firmware option is an improvement on the original option 003 for the 8904A, which relies on hop RAM to permit external timing control for high-speed frequency, phase, or amplitude hopping. The special option, called hop-RAM sequencing, gives users the same frequency shift keying in the same 16 registers as the original option—each with its own frequency, phase, and amplitude. The difference is that the instrument now uses one of its four internal channels as a clock source to drive the hopping sequence. Also, the sequence memory has been enlarged to handle 750 states in a sequence as opposed to 250 states.

The company reports that many customers are using 8904A instrument's DTMF sequence mode for telephone applications, because the instrument gives them a synthesized HPIB-programmable DTMF generator.

Pricing for the two special firmware options for the digital synthesizer has not yet been set.

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ELECTROCHEMICAL METALLIZING

A revised six-page booklet entitled *Electronic Applications for Electrochemical Metallizing* explains how to deposit several conductive, solderable, or corrosion resistant metals in precise thicknesses on defined areas of electronic components and pc boards. Some electrochemical metallizing techniques are explained in detail. The repair methods covered are systems approved by the I.P.C.

Selectronics Ltd., 137 Mattatuck Heights Rd., P.O. Box 115, Waterbury, CT 06725; (203) 755-9900.

CIRCLE 348

RESONANT-MODE POWER SUPPLY DESIGN

A 25-page brochure (AN 510-13) describes the use of the LD405 controller IC in designing high-frequency, 125-watt resonant-mode power supplies. This chip provides an easy and cost-effective way to control and protect resonant and quasi-resonant converters. The brochure contains a typical power supply circuit, as well as the necessary design equations.

Gennum Corp., P.O. Box 489, Station A, Burlington, Ont., Canada L7R 3Y3; (800) 263-9353 or (416) 632-2996.

CIRCLE 349

64180 PROCESSOR APPLICATIONS GUIDE

The Guide to 64180 Applications Development provides a complete description of the use and programming of the 64180 microprocessor. It includes an introduction to the processor, in-depth coverage of all of the 64180's features, and it compares the 64180 to other similar processors. Detailed information about using the internal peripherals, along with example schematics and code segments, is included. A companion guide disk is also available that contains the executable listings. A description of hardware and software development environments is included, as well as sources of 64180 support products.

Softaid Inc., 8930 Route 108, Columbia, MD 21045; (800) 433-8812 or (301) 964-8455.

CIRCLE 350

VOLTAGE/FREQUENCY CONVERTERS

An eight-page bulletin on the A-8400 converter IC describes in detail the operation of this chip, which can function as either a voltage-to-frequency converter or as a frequency-to-voltage converter. Provided within are hookup instructions, along with information on device operation and parameters. Six design examples are also included.

Advanced Analog, a division of Intech, 2270 Martin Ave., Santa Clara, CA 95050; (408) 988-4930.

CIRCLE 351

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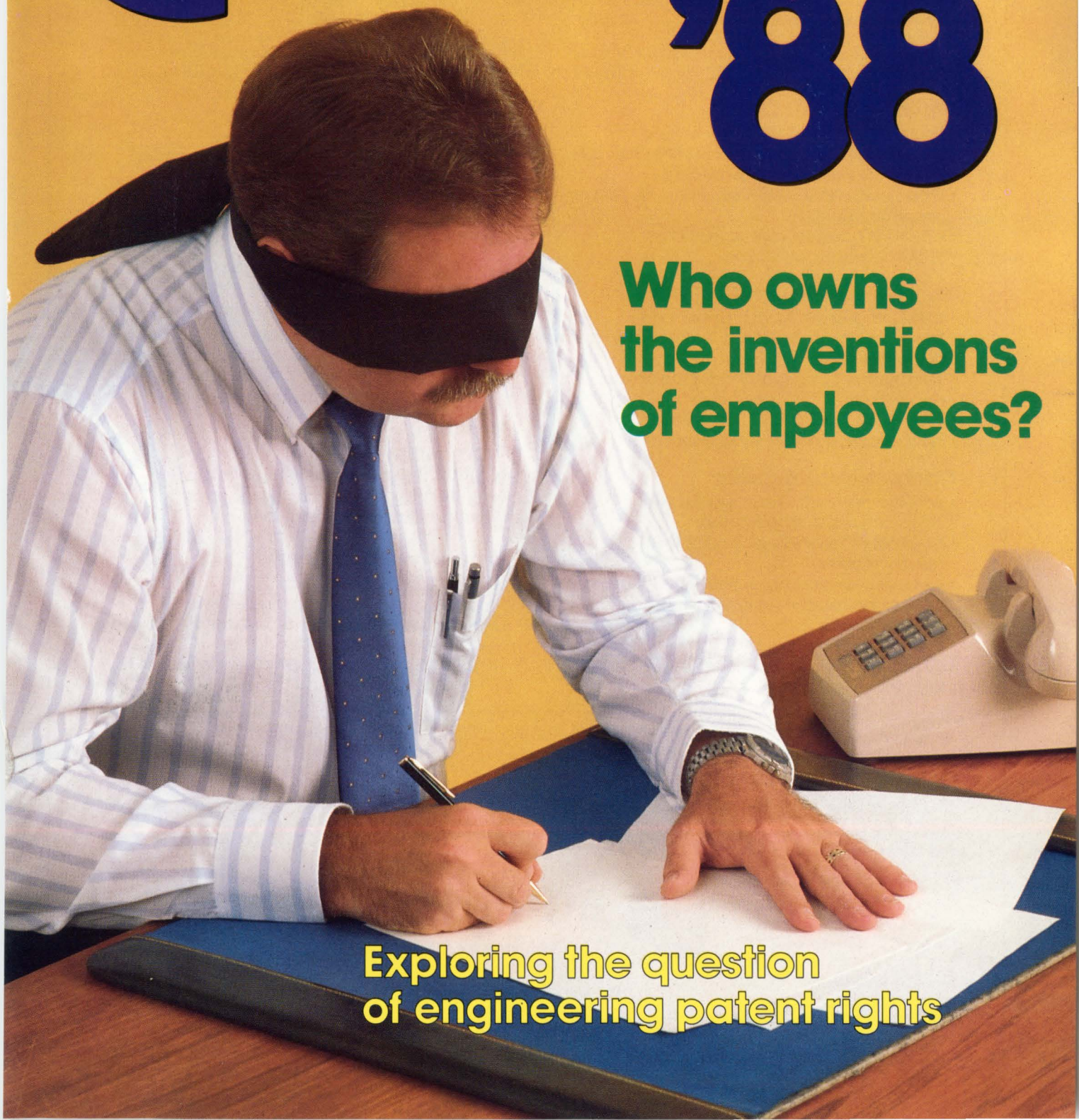

Who owns the inventions of employees?

Exploring the question of engineering patent rights

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As a condition of employment, engineers sign away patent rights. In all likelihood, they probably always will.

Who owns the inventions of employees?

EMPLOYEES WHO INVENT PRODucts that ultimately make millions for their employers are not likely to share in the profits. It's a fact of life in all but four Western countries, and has been for decades.

The engineering community breaks into two factions over this issue—those who believe the present system is fair to both parties, and those who believe employees are being taken for granted. Not surprisingly, most of those in the former faction are members of corporate management. The other faction consists of a loosely organized, not very vocal, group of engineers and academics.

In fact, finding someone to defend the sanctity of "intellectual property" for working engineers is difficult. The prevailing opinion is that employees are paid to perform. If, during their job performance, they unearth some major marketable product, they owe it to their employer to disclose it. The possibility that their employer may successfully develop that product, market it, and reap huge sums in return cannot be credited to the inventor, who merely came up with the idea. The employer, after all, took all the necessary risk:

- It paid to develop the idea into a marketable product.
- It paid to build the product and keep it in inventory.
- It paid to market and promote the product.

Since the employer took all the risk, it has every right to reap all the rewards, according to prevailing opinion. It's a difficult argument to counter, since in all probability the inventor would allow the creation to lie untested for fear of failure.

"The way we allocate risk and reward in our society is that the party who risked the most stands to gain the most," says Robert Spanner, a senior partner in the law firm of Beckford and Spanner (Palo Alto, CA), which specializes in trade secret litigation.

Stanley Green, a partner in the firm of Pollock, Vesande, and Priddy (Washington, DC), agrees: "I believe it is fair for a company to own an invention if it is job-related to the extent that the employee was directed to solve the problem, and salary and benefits were provided by the company." Green also believes that the failure of most employers to pursue bright ideas is a major reason for employee discontent.

Of course, there is a vast territory between the views of

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BARRY MANZ is President of Manz Communications, Inc., Montville, NJ.

WHO OWNS INVENTIONS / *CONTINUED FROM P. 3*

the two parties. In it, falls the honorarium—plaque, check, or handshake. The financial reward that some companies provide their inventors rarely amounts to more than a few thousand dollars. Such presentations also serve to establish the engineer as a novel fellow who should be regarded by his or her peers as a significant contributor to the company's future—a shining star.

However, after the check is spent, the plaque has yellowed, and the handshake is only a memory, the employer continues to reap the cash rewards, sometimes for decades. Thus, idealistic members of the engineering community sometimes express the hope that employers will someday pay their employees a royalty on each invention that generates income for the company.

ONLY A FEW STATES LIMIT PRE-ASSIGNMENT PACTS.

The plight of the employee inventor has generated considerable interest over the years. The Institute of Electrical & Electronics Engineers (IEEE), for example, included intellectual property rights in its Federal Legislative Agenda for the 100th Congress, and has adopted position statements on intellectual property protection. The IEEE also filed a "friend of the court" brief in 1985 protesting a California appeals court decision awarding ownership of an electronic-warfare training system to the employer, not the employee. The court had ruled that the invention could not be considered tangible until the patent was filed.

The IEEE stated that the decision "emasculated" an existing California statute. "Because of that conclusion [the court decision]," the IEEE wrote, "any employer resource used to further the invention, or intervening expansion of the employer's business as a consequence of knowledge of the invention, could be relied on to defeat the protection afforded by Section 2870 of the California Labor Code."

Section 2870 specifically defines the limits to which preassignment agreements can be taken by an employer. Only few states have such codes—California, Illinois, Minnesota, North Carolina, and Washington. The IEEE simultaneously adopted a statement urging the terms of these agreements be delineated "prior to, or simultaneous with, a monetary offer of employment."

The agreement to transfer to the employer the rights to an employee's invention is a staple of engineering employment, to be signed right from the start, during indoctrination. While there are hundreds of different versions of this form, they all say the same thing: When you join the company, the company owns everything you invent there, even if that invention does not appear to be in the company's areas of expertise, or in its marketing plans. In essence, the manufacturer owns the employee's work.

What happens if prospective employees refuse to sign such preassignment agreements? In most cases, they won't get the job, according to Green, because there will be another qualified applicant who will sign it. Challenging the agreement after employment begins is equally futile, according to Green: "You've got an uphill

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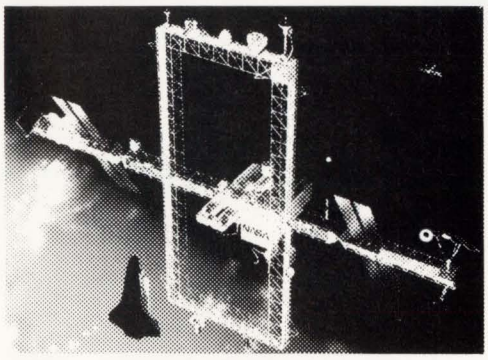

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WHO OWNS INVENTIONS / *CONTINUED FROM P. 4*

battle because you signed that form. These agreements really do work. Unless you live in one of the few states that have limitations on the agreements, there is no such thing as an overly restrictive agreement."

Surprisingly, the issue of "who owns what" does not even raise the ire of those critics quick to cite alleged abuses of working engineers in other areas—not even Irwin Feerst, the outspoken critic of the IEEE. "The only organization supporting this [patent rights for employee inventors] is the Committee of Concerned EEs," says Feerst, leader of the Committee.

However, Feerst feels there is certainly need for change and that patent rights have been usurped by employers. "The dearth of patents in the engineering field is due to the fact that the people who develop potential patents don't have any rights," says Feerst. "It seems to me that if you want to encourage US engineers and scientists to patent, you have to give them partial ownership of the invention. It's a national problem." Feerst also points out that the patent process is time-consuming, complicated, and expensive, so it is unlikely that engineers would have much interest in pursuing it on their own.

The same concern was expressed by several figures in the engineering world interviewed for *Careers '88*. For example, if an applicant wishes only domestic protection for his or her invention, the cost could be $10,000. However, if international protection is desired, the cost can jump to $60,000, requiring reams of paperwork and hundreds of hours of research. For inventors who feel their brainchild is noteworthy, but who have absolutely no idea how marketable it is, spending $60,000 to find out is often beyond reasonable levels of risk. It's entirely possible that the cost and complexity of obtaining a patent has risen so high that individuals can no longer afford to obtain one.

PRIVATE PARTIES CAN NO LONGER AFFORD PATENTS.

One argument used by most proponents of invention compensation for employees is the likelihood of increased initiative. There are only four Western countries that compensate

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WHO OWNS INVENTIONS

CONTINUED FROM P. 6

their employee inventors—Austria, The Netherlands, Sweden, and West Germany. Of the four, West Germany has the most established mechanism. There, every inventor is entitled to be compensated for his or her invention. The amount of the royalty is based on a complex formula centered on the importance of the invention, its sales value, the stature of the employee, as well as other factors. The law has been in effect for 30 years.

Erich Franke heads the patent trademark and licensing department at West Germany's Wacker-Chemie, the world's largest manufacturer of silicon-based material for semiconductor fabrication. He has been involved in the patent process for 30 years and has seen the company's total inventor awards rise to $900,000 in 1987. These awards are paid to each inventor every year that the patented product, process, or technology is in use, and that the patent is in force. Some inventors receive $1000 per year; a few receive as much as $30,000.

The law applies only to people employed by Wacker-Chemie in West Germany. The company also has a facility in Portland, OR, and is controlled by the Hoechst Co., which has a large American work force. These employees do not benefit from the German law.

"We calculate the award [to the employee inventor] as if we had received the invention from somebody outside the company," says Franke. "The figure is then reduced, since the inventor is an employee and gets a salary. The final consideration is the position of the inventor in the company."

As an example, Franke uses the case of the head of an R&D group. "If he creates an invention, he gets less money than a

lower-paid employee, since in a managerial capacity he may only be functioning as a laborer on the project to be patented," says Franke. "It could be said also that since the head of R&D gets a much higher salary and is more highly educated, we should expect such an invention from him." Has the law been an incentive to creativity? Franke feels that it has had a positive impact.

While there appear to be few US companies that routinely compensate their inventors the way West German companies do, some go beyond the simple honorarium. Tektronix (Beaverton, OR) practices what might be termed an "intrepreneurial" approach. Over the years, the company has worked with some of its employees to form new companies, divisions of the existing company, and even totally unrelated enterprises.

Tektronix Development Co., a wholly owned subsidiary of Tektronix, has as its only goal the development of Tektronix interests through exploitation of the resources within the main company and its divisions. "TDC functions as a venture capitalist," says Rick Hill, vice president. "We identify technology in our laboratories that we would like to get into the marketplace, as well as areas of the company we need to shore up.

"We have entrepreneurs within Tektronix who may not have the ability to start a company," Hill continues. "They are encouraged to talk to us about their creations, and we try to educate them about the market, and running a business. If after all this they still feel strongly, we evaluate the market, revenue stream, value of the technology in the long term—the P&L."

If the entrepreneur remains undaunted and wishes to continue, Hill says, TDC will fund the new company or will find funding from outside sources. Anthro Furniture Co., to cite one example, resulted from this process. Anthro was formed from the remains of the Tektronix campaign into the workstation business. Tektronix turned out the lights on the workstation business four years ago.

However, some employees felt very strongly that the operation's ability to make computer furniture represented a viable business opportunity. Tektronix funded the effort and eventually sold it to the employees because it didn't match Tek's product and marketing focus. The company is prospering. Planar Technology was founded in a similar manner, and Tektronix has a stake in the technological and financial developments of that company.

Cascade Microtech was formed because GaAs microwave monolithic-integrated-circuit manufacturers needed to test these extremely fast, high-frequency devices on the wafer. "The two principals in Cascade developed a probe station at Tektronix and approached our patent department," says Hill. "They cut a deal, and started the company. It has been profitable since

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WHO OWNS INVENTIONS / *CONTINUED FROM P. 9*

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early on. Our interest is maintained, since Tektronix gets a piece of every probe they sell."

Nevertheless, the general patent process at Tektronix is no different than that of most other companies. "The patent is assigned to Tektronix," says Rick Mootry, manager of licensing and technology transfer. "The normal return to the inventor is through job progression, options, and other things that are included in evaluation of the person's performance. The patent is taken into account as part of the overall profile."

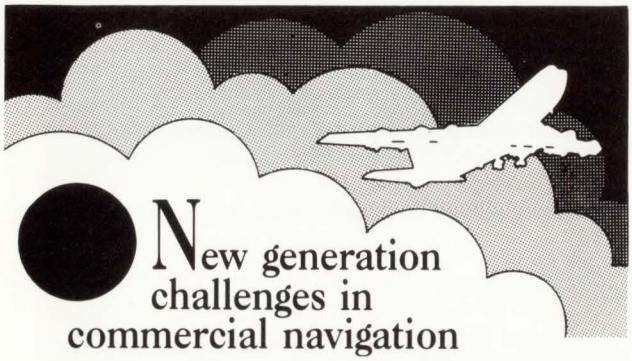
The lack of inventor compensation hasn't impeded the proliferation of patents within Tektronix. Its patent portfolio is growing at one of the highest rates of any US company. "Tektronix is in the top 20 list of patent receivers," says Mootry. "We have seen 12-percent annual growth over the last five years."

Based on his experience in working with inventors, Hill concludes that when faced with the enormous task of supporting an innovation with a company to produce and market it, inventors usually decline. "Let's say you, the inventor, quit Tektronix tomorrow. Perhaps we can get you $500,000 in financing. When you run out, that's it. You'll find pretty quickly that there is a lot of risk. Most engineers, when the whole picture is put in perspective, say: 'Well, I'm not likely to lose my job at Tek, Inc., so maybe I'll stay.' "

In 1984, the IEEE issued a position statement on intellectual property protection that supported the protection of new technologies by amending the patent and copyright laws, the reduction of the cost and complexity of obtaining and enforcing new patents, and the enactment of legislation that would stimulate activity in the US by providing additional incentives to independent and employed inventors.

While the IEEE has made its intentions clear on the issue of intellectual property, its effectiveness has been questioned. Some soul-searching comes from IEEE Intellectual Property Committee (IPC) Chairman Steuart Bjornsson, who has responsibility for these efforts.

Bjornsson believes that the



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IEEE's intentions may be commendable, but its track record is not. "The IPC is somewhat limited in its scope of operations," says Bjornsson. "We collect and distribute information, but there is some limit as to what we can do in that regard." He cites the lack of funding as one of the reasons. "On the Richter scale, our efforts are not visible," says Bjornsson. "The IEEE gives us $10,000 a year to support this activity from its $15-million budget.

"I have proposed half a dozen programs to increase the committee's effectiveness," Bjornsson continues, "but not a single one was supported. I proposed establishing an incentive for IEEE members who have received patents so they could increase their standing in their companies and use their strength to lobby more effectively for more appropriate legislation in this area. My conclusion is that I could actually have accomplished more without the IEEE than with it."

For the time being, officials of the US Patent Office have enough on their minds. The patent office is presently undergoing a $1-billion modernization program. This is an enormous task in an organization that is extremely dependent on documentation.

So, while the need to amend current patent laws to provide justice for both employer and employee inventor is cited as a worthy goal by members of the engineering community, implementing these changes is a daunting task, requiring massive lobbying efforts and large sums of time and money. Thus far, no large trade or industry organization has accepted the challenge.

Decades of status quo have virtually assured that the "national problem" alleged by Feerst will not be solved any time soon, even with a concerted effort by an extremely influential organization. The best the creative engineer with a great idea can hope for is a rush of entrepreneurial adrenalin, a flexible, supportive employer with money to invest, or more likely, a plaque. ••

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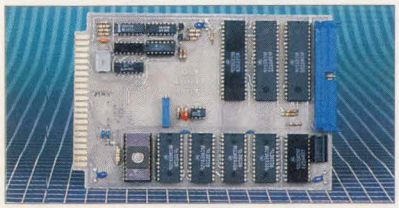

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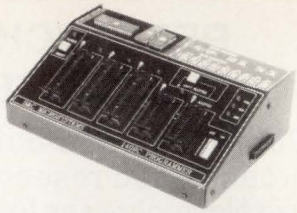

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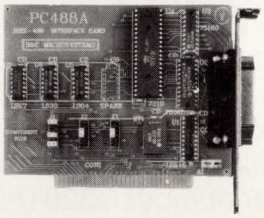

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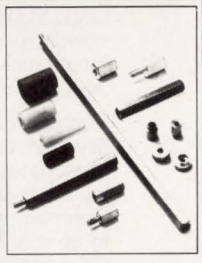

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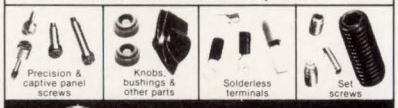

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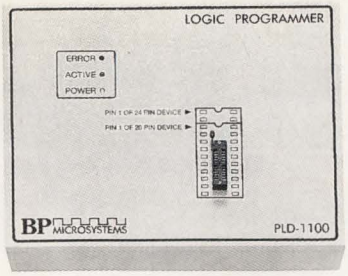

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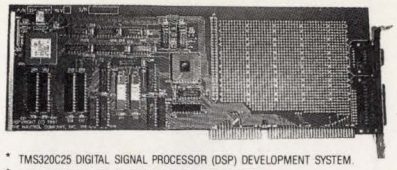

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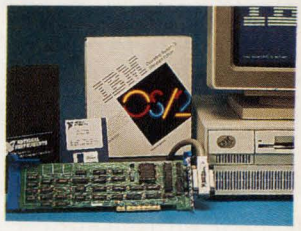

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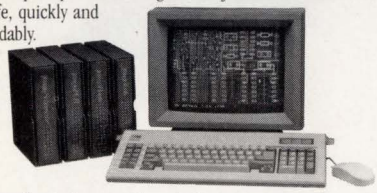

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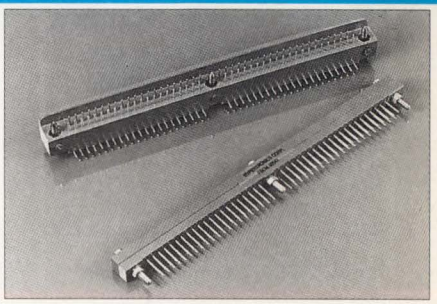

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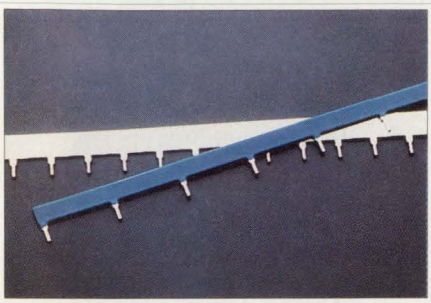

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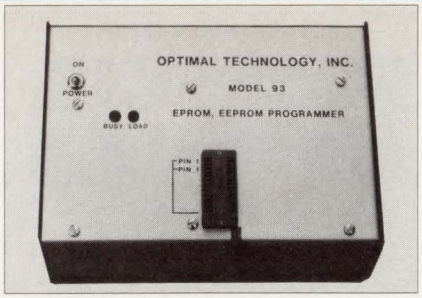

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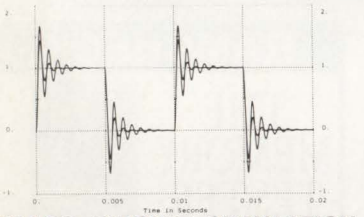

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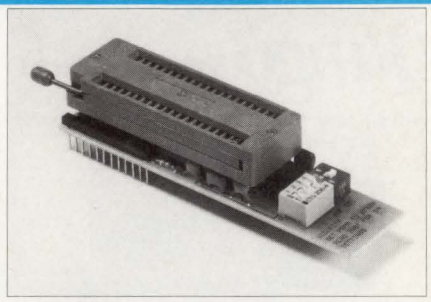

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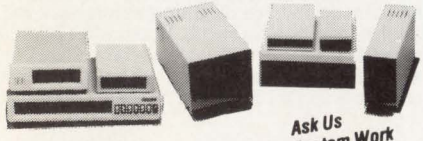

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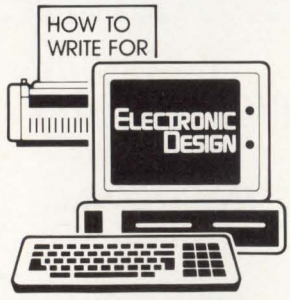

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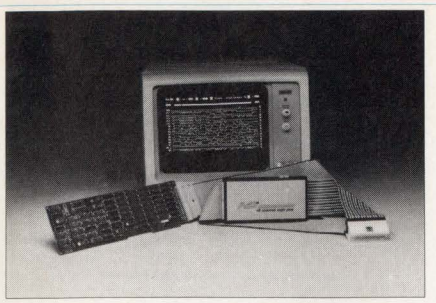

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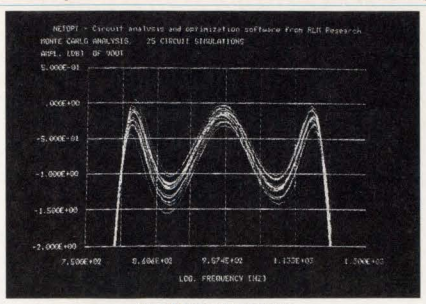

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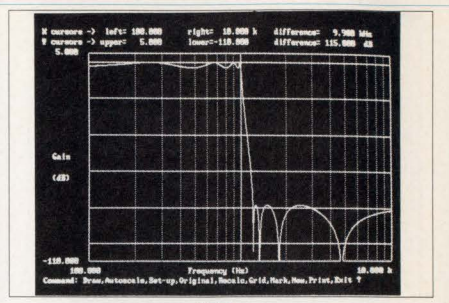

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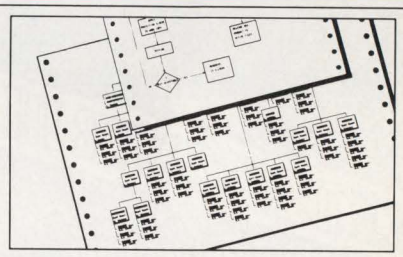

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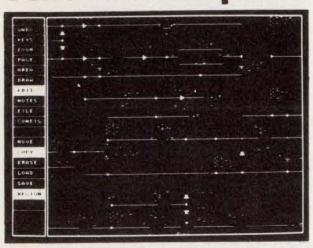

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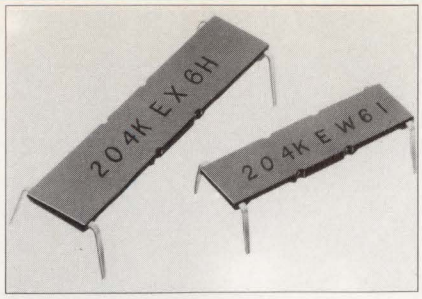

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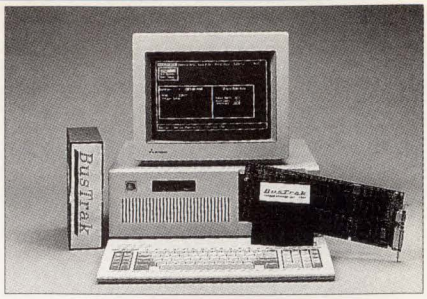

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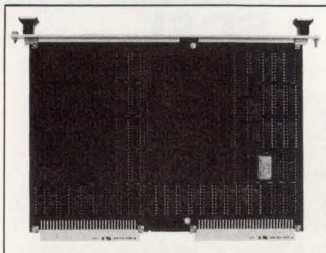

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The Cadnica EXTRA batteries run 40% longer than conventional Ni-Cd cells. So, with Sanyo Cadnica EXTRA batteries on board, your products will run longer. You get improved performance with no alteration in product design. And that means greater end-user satisfaction.

Longer Run Time

Energy Efficiency Improved

Charge-time is flexible. EXTRA series can meet virtually all your specifications. From extra-fast to standard or trickle-voltage rates.

For critical applications like handheld field communications gear and medical instruments, they're the best battery to use. They're also an obvious first choice for emerging portable personal computers and for household appliances.

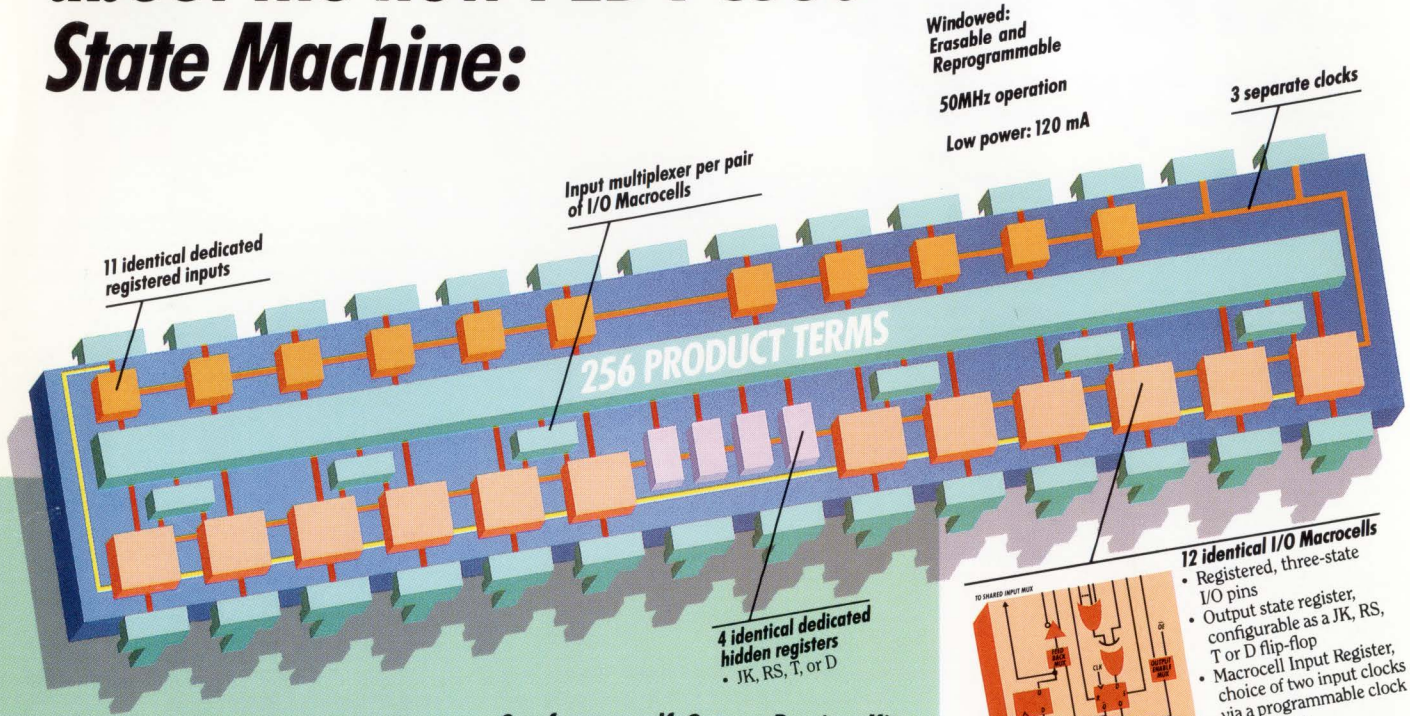
There's another important benefit. The Cadnica EXTRA series is part of the Sanyo No-Excuses Guarantee, your assurance of on-time, as-promised delivery; stable, fair prices; and the highest standards of performance. For further information on our latest technology, and for applications assistance, call or write: SANYO Energy Corp., 1201 Sanyo Ave., San Diego, CA 92073 (619) 690-6620.
In New Jersey: (201) 641-2333
In Chicago: (312) 595-5600
In Florida: (904) 376-6711

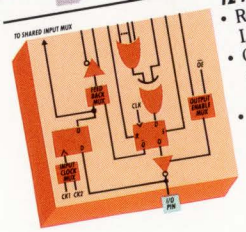
SANYO

There's something new going on at Sanyo.

CIRCLE 50

Why high performance designers are so excited about the new PLD 7C330 State Machine:





12 identical I/O Macrocells

- Registered, three-state I/O pins
- Output state register, configurable as a JK, RS, T or D flip-flop
- Macrocell Input Register, choice of two input clocks via a programmable clock multiplexer
- Output enable multiplexer, programmable, to select common $\overline{OE}$ signal or Macrocell $\overline{OE}$ product term
- Input feed-back multiplexer, programmable, to select either state register output or Macrocell Input Register output (creating a bi-directional I/O pin)

As state machines go, this one goes the fastest. With the highest functional density available.

A system that lets you design state machines that can execute control sequences at a full 50MHz without even breathing hard.

High performance designers are excited by the extensive features, led by the richness of 256 product terms.

By this part's ability to deliver twice the performance and density of previous generation PLDs, with about half the power.

By the ease of programming, using popular programming languages and machines.

And by the ability to design the highest performance state machines, with 1000 to 1500 gate functionality, using reprogrammable PLD technology.

See for yourself. Get our Preview Kit.

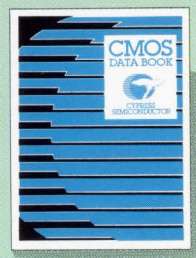
Our Preview Kit, with demo floppy and technical paper, even includes application ideas, like our step-by-step design example showing you how to create a 16 x 4 programmable multiplexer using a single CY7C330.

You'll also get the databook that has the information you need on this great part, and on ALL our high performance parts.

CMOS high speed SRAM.
CMOS high speed PROM.
CMOS high speed PLD.
CMOS high speed Logic.

PLD 7C330 Preview Kit and DataBook. Yours free, for a toll-free call.

DataBook Hotline:
1-800-952-6300
Ask for Dept. C33
(32) 2-672-2220 In Europe
(416) 475-3922 In Canada



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