Technical description and

general principles of HDD IDE (ATA) repair.

Version 4
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List of abbreviations used .

HDD - hard magnetic disk drive; SHIFU - pulse width
phase control; MG - magnetic head;
BMG - magnetic head unit;
AGC - automatic gain control; AM - addressable
marker;
GUN - voltage-controlled oscillator; MC -
microcircuit;
FABF - phase frequency autotuning; CCC -
control-cycle code;
ADC - analog-to-digital converter; LPF - low-pass
filter;
HOST, control computer; ECC, error
detection code; CRC, control-cycle
code;
FIFO is a "first in, first out" type of memory.

1. Technical description of the IDE HDD AT.

1.1. Structural diagram of IDE AT HDD.

The structural diagram of IDE AT HDD is shown in Fig.1
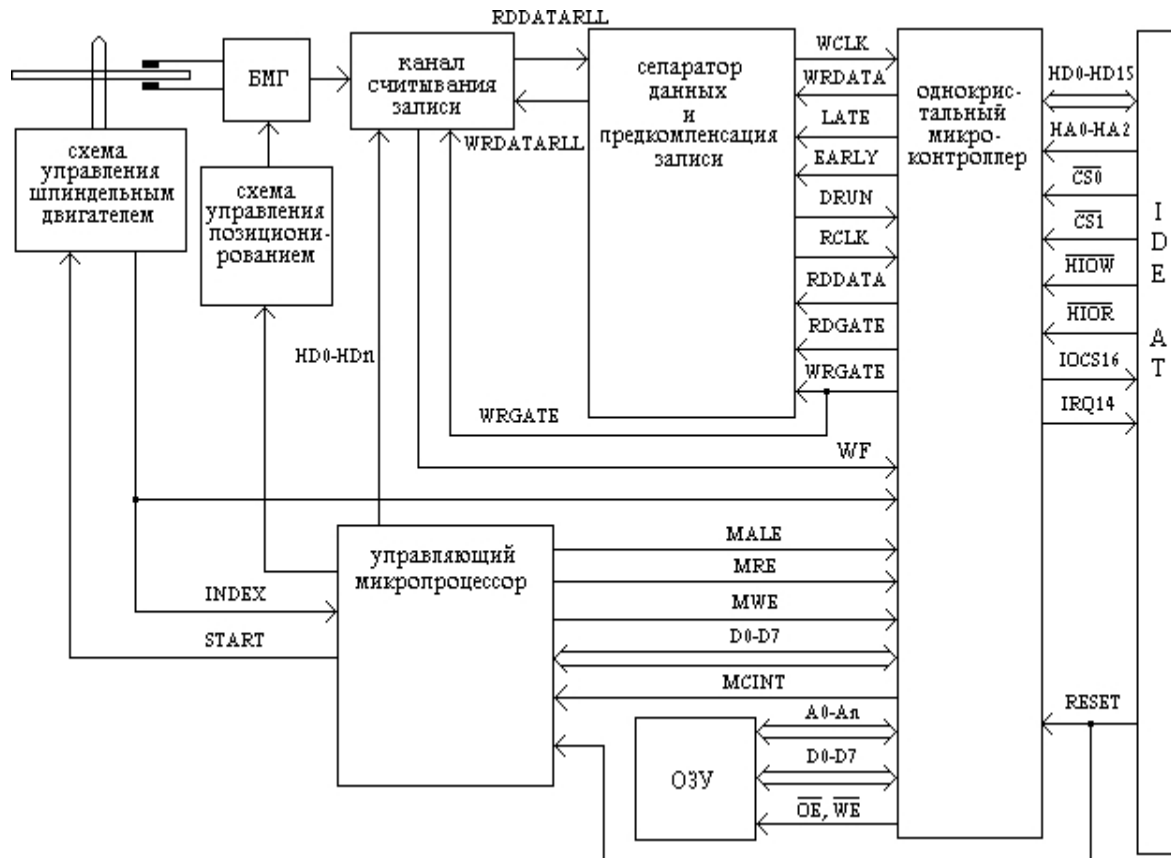
Fig.1. Structural diagram of IDE AT HDD.

INDEX - signal generated by the spindle motor control circuitry for one revolution of the disk; START - permission to start the spindle motor;
HD0-HDn - binary code of read/write head selection; RDDATARLL
- RLL read data;
WRDATARLL - RLL record data;
WF - signal generated by the recording circuit in case of error;
WCLK - synchronous pulses of the data being recorded;
WRDATA - recording data in NRZ code;
LATE, EARLY - control signals of the precompensation mode;
DRUN - output of the synchronization field detector;
RCLK - read data clock pulses; RDDATA - read data in
NRZ code; RDGATE - read strobe;
WRGATE - record strobe;
MALE - address strobe of the control microprocessor;
MRE - read strobe of the control microprocessor; MWE -
write strobe of the control microprocessor; D0-D7 -
internal data bus of the drive;
MCINT - interrupt signal from the single-chip microcontroller;
/OE - read strobe for buffer RAM;

/WE - write strobe for buffer RAM;
HD0-HD15, HA0-HA2, /CS0, /CS1, /HIOW, /HIOR, /IOCS16, IRQ14,
RESET - interface signals.

1.1.1. Cxema control of the spindle motor.

The spindle motor control scheme is described in detail in [1]. The spindle motor of IDE AT HDDs is usually three-phase, which provides a more stable rotation speed, which is especially important at higher write densities. For the same reason, such motors usually have three Hall sensors (ST157A, ST351A/X, WD9xxxxA, KL-343, KL-3120), which allows the spindle motor control chip to more accurately adjust the disk rotation speed. The higher requirements to the spindle motor control circuit are related not only to the increased density of IDE AT HDDs, but also to the fact that such HDDs have small dimensions, they use 3-inch disks, because of this the mechanical system of spindle-magnetic disks has low inertia, which, on the one hand, allows to spin up and stop magnetic disks faster, but on the other hand, such mechanical system is more susceptible to detonation. In the majority of drives with solenoid drive of magnetic heads for providing feedback of spindle motor control chip and spindle motor itself instead of Hall sensors built-in service information is used, it is used not only for positioning of magnetic heads, but also for stabilization of spindle motor rotation speed (ST1144A, ST3144A, ST3290A, ST3660A by Segate; CP3xxxxxA, CP3xxxxx, CFSxxx, CFAxxx by Coner; CAVIAR by Western Digital and others.). In such HDDs, when supply voltage is applied, the spindle motor spins up in a forced mode without analyzing the magnetic disk rotation speed. After that, a special circuit from the service information format allocates servo-mark pulses, which are fed to the spindle motor control chip; further stabilization of the rotation speed is performed according to these pulses. A distinctive feature of such drives is the presence of only three conductors (control phases) going to the spindle motor. In the first models of IDE AT HDDs the rotation speed of magnetic disks was usually 16.6 ms (ST157A, KL-343, KS-40GA, WD9xxx8A), in modern models of HDDs when using high-performance single-chip controllers to increase the exchange speed the rotation speed is significantly increased and reaches 8 ms in 1 Gbt models CFP1060S, CFP1040A of Sopner. Practically in all models of IDE AT HDDs the permission to start the motor is given from the control microprocessor after its initialization, so the spindle motor can stop when the RESET interface signal appears, moreover, in Segate drives the spindle motor is started only after a complete internal diagnostics of the drive.

1.1.2. Cxema for controlling the positioning system.

IDE AT HDDs use both stepper motor and solenoid-driven (voice coil) positioning systems, and recently the solenoid-driven positioning system has almost completely replaced the stepper motor positioning system. This is due, first of all, to such a characteristic of HDDs as the average access time. The second reason is the ever-increasing recording density due to the increasing number of cylinders on the working surface and, as a consequence, the decreasing distance between two neighboring tracks. Modern HDDs use balanced rotary positioning systems, which are more reliable and take up significantly less space than the linear positioning systems used in early HDDs. Solinoid drives use two types of SI to accommodate service information (necessary for positioning the magnetic heads):
        - SI on a separate (dedicated) surface (deedicated surfase) ST1144A, ST3144A, ST3283A, ST3655A, LXT340A, MXT540A;
        - Embedded SI (embedded).
The latter in its turn is subdivided into SI located between sectors and SI embedded in the format. The former includes models WDAC2120A, WDAC2200A, etc., of the CAVIAR agiteture-0 family; early models of the CP-3xxx family, CFA and CFS of the Conner company, etc. The number of servo marks on the track exactly corresponds to the number of sectors of the drive and they are located strictly between the sectors. In such models the number of servo tags on the track exactly corresponds to the number of sectors of the drive and they are located strictly between the sectors. Moreover, the number of servo tags on the track changes in accordance with the zone distribution.

modern drives use SI built into the format. In this case, the number of servo marks on all tracks is the same and equal, such as the ST3660A's 60. In such drives, the format is not bound to servo marks and a track can be formatted to a different number of sectors. When a servo tag is encountered, the physical format is interrupted (even if a data field is encountered) and continues only after the servo tag is identified.

The first IDE AT HDDs with ST157A, KL-343 stepper motor used conventional phase control of the stepper motor, which is discussed in detail in the literature [1] and consists in the fact that to move to a given track to the phases of the stepper motor it is necessary to apply sequentially discrete voltages to the phases of the stepper motor, at that the motor shaft will rotate by a given angle. There was no feedback on the position of the heads and the capacity of drives that used this positioning principle did not exceed 40 MBt. Later stepper motor HDDs started using pulse width phase control (ST351A/X, WD9xxxxA, KL3100, KL3120). These drives use an integrated servo format and therefore occupy an intermediate position between stepper motor drives and solenoid drives. The idea of pulse-width phase control is as follows: after moving the magnetic heads to a given track, the stepper motor is adjusted to the maximum amplitude of the read service information and only after that the data is read or written. The structural diagram of the latitude-pulse phase control of the stepper motor of the WD9xxxxA family of drives is shown in Fig. 2.
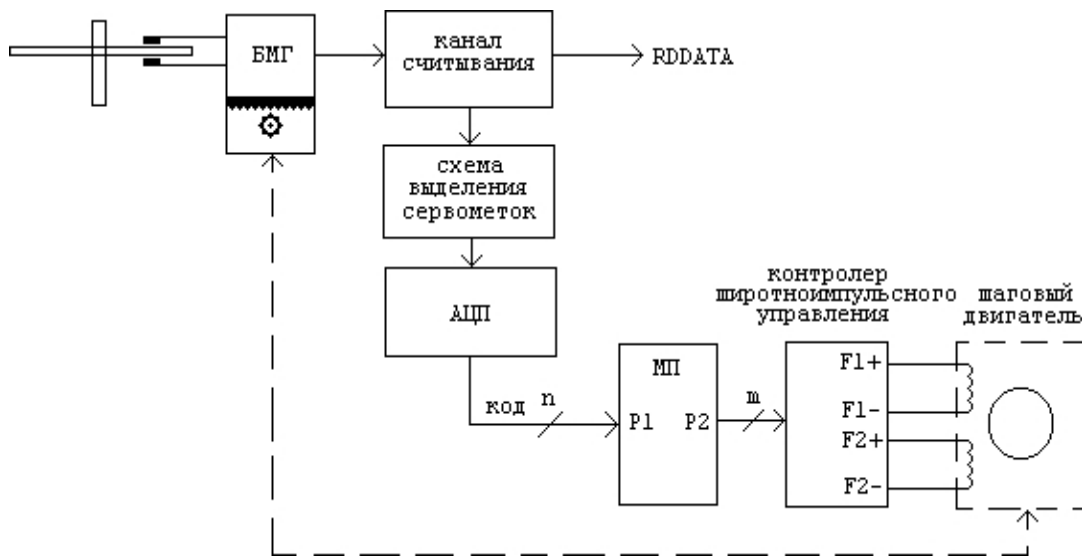
Fig.2. Structural diagram of pulse-width phase control of stepper motor.

To move the magnetic heads by one cylinder, the control microprocessor supplies code m to the SHIFU controller, which causes the MGs to be moved by approximately one cylinder, after which the microprocessor reads code n from the servo marking circuitry and compares this code to a reference value.
If there is a code mismatch (due to an offset from the track), the code m is corrected and the process is repeated.

Control systems with a solenoid motor (voice coil) are the most complex, but due to the advent of single-chip servo-modulators it has become possible to use a solenoid drive in inexpensive, mass-produced models of HDDs. At present practically all drive manufacturers have started to use the solenoid motor for positioning systems. The structural diagram of the control system with a dedicated servo-surface is shown in Fig.3., with a built-in servo-format is shown in Fig.4.

БМГ

канал чтения/записи

Read Data
Write Data

сервоканал

R/W

от
однокрист.
микроконт.

шпиндельный
двигатель

соленойдный
двигатель

требуемый
ток

серводемо-
дулятор
и серво-
контроллер

Index

схема
управления
шпиндельным
двигателем

токовая
схема
управления
позициониров.

сигнал
рассогласо-
вания

состояние
сервосист.
и действит.
положение

управ.
МП

требуемое
положение
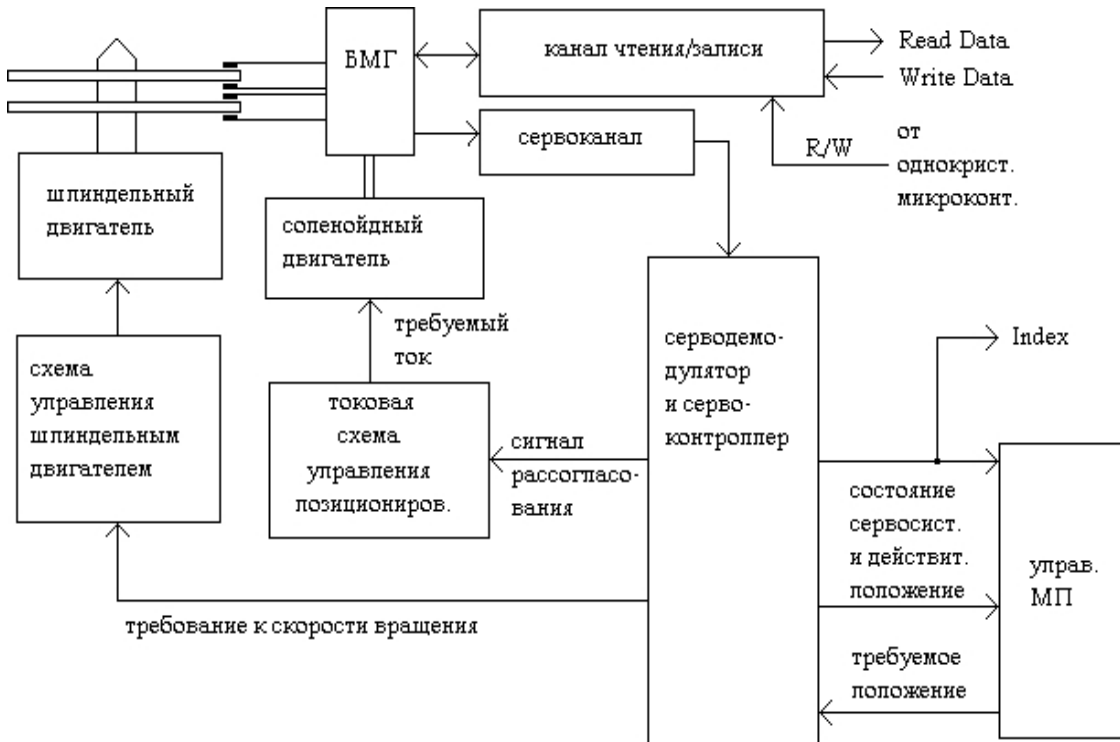
требование к скорости вращения

Fig.Z. Structure diagram of positioning control system with solenoid motor with dedicated servo surface.

The principle of building a system with a dedicated servo surface is as follows: When the drive germoblock is manufactured, special service information is written to one of the surfaces (usually the lowest surface of the disk package). A magnetic head, which is read-only, continuously reads the service information. The SI, amplified and filtered, is fed to the servo-modulator, where it is decoded and then the actual position of the magnetic head assembly is determined. Based on this information, the solenoid motor control unit is actuated. In this way, the fine-tuning is monitored.

Another task of the positioning system is to create a current pulse in each case when crossing the track. The initiator of such a pulse is the control micro-processor, which indicates the desired track number to the servo controller. Based on this, the servo-controller transmits the code of the required current pulse to the positioning control circuitry, where its exact value is formed using a DAC. Let us first consider the operation of the fine control device, whose task is to maintain the track once found as accurately as possible.

Position information is obtained by means of servo cells. Depending on the manufacturer, disk size, track density and complexity of servo cells, their number varies between 500 and Z000 per track. Figure 5 shows a simplified servo cell structure. Each cell consists of four magnetization directional shifts called dibits. The cell is bounded on both sides by synchronization fields. The position of the servo trap is strictly between the even and odd servo dibits. At this position, the signal shown in Fig.6 is induced in the servo trap. The positioning electronics generates an error voltage from this signal, which is obtained as the difference between the pulses labeled A and B. If the head is now positioned absolutely correctly, i.e., strictly between the servo tracks, this error voltage will be zero. If the head is shifted towards the odd track, then in the data signal the A pulse increases and the B pulse decreases. This creates a positive error voltage, and the servo system tries to compensate for it by moving the head toward the even track.
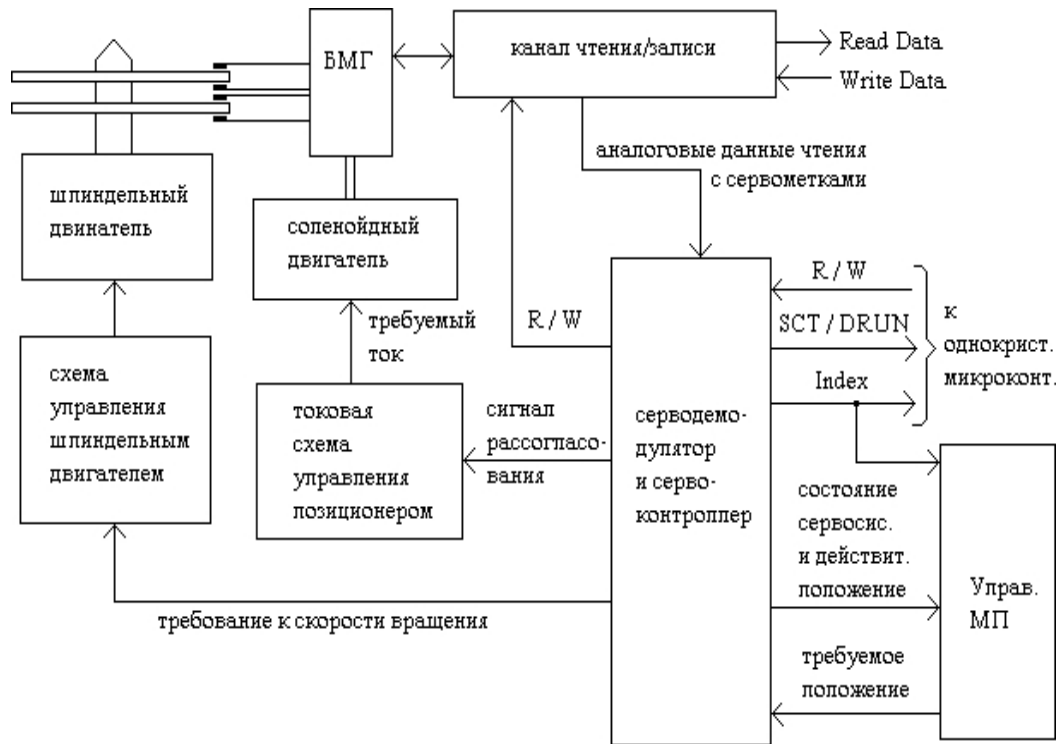
Fig.4. Structural diagram of the positioning control system with solenoid motor with integrated servoformat.
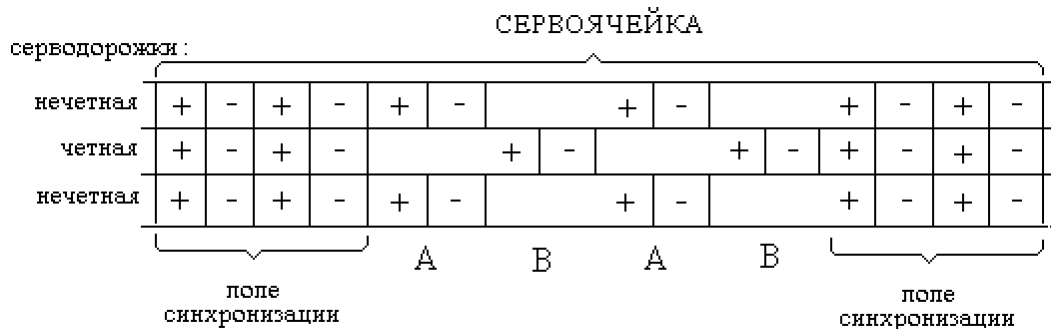
Figure 5. Simplified structure of the servo cell.
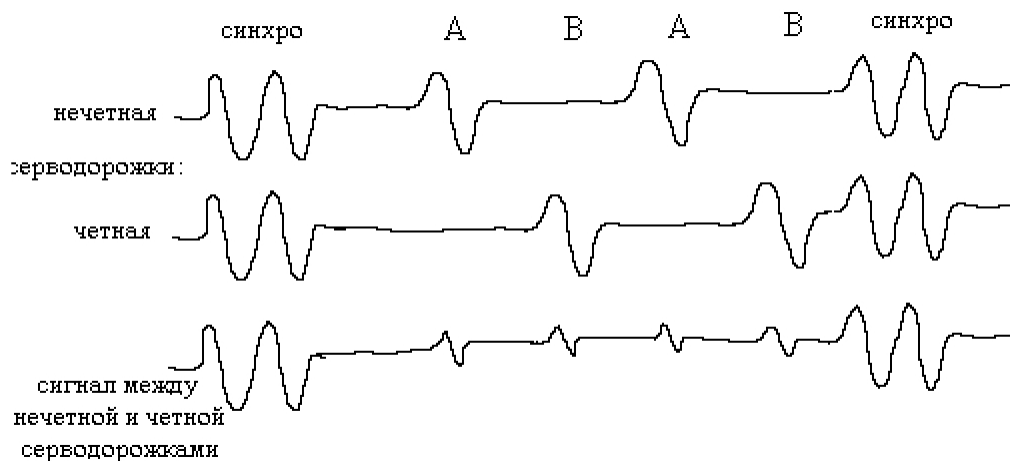
Figure 6. Induced signal in the servo trap.

To move to a given track, the positioning control circuitry must generate a current pulse as shown in Figure 7. After moving, the fine control system is switched on to fine tune to the track. Depending on the displacement length, the concept of positioning classes is introduced, (Fig.8), by which the displacement current pulses are generated. The more positioning classes the drive has, the faster the drive finds the desired track. In modern drives, the number of positioning classes is equal to the number of servo tracks of the drive - and each length of travel corresponds to a specific current pulse.
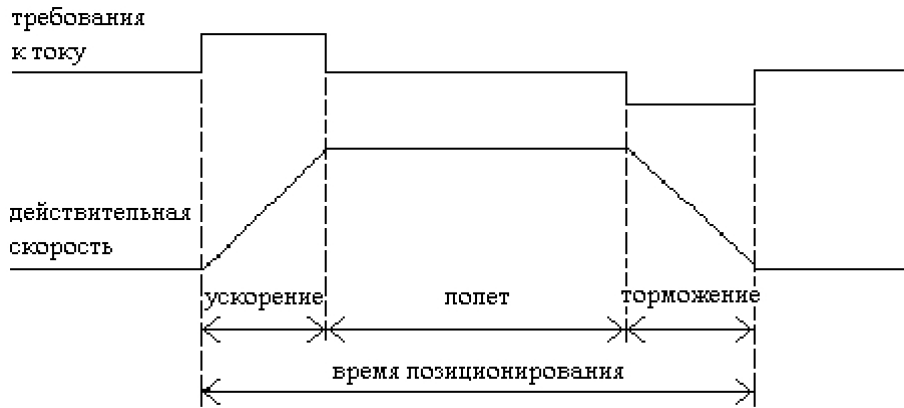
Figure 7. Positioning current pulse.

Figure 8. Classification of positioning length.
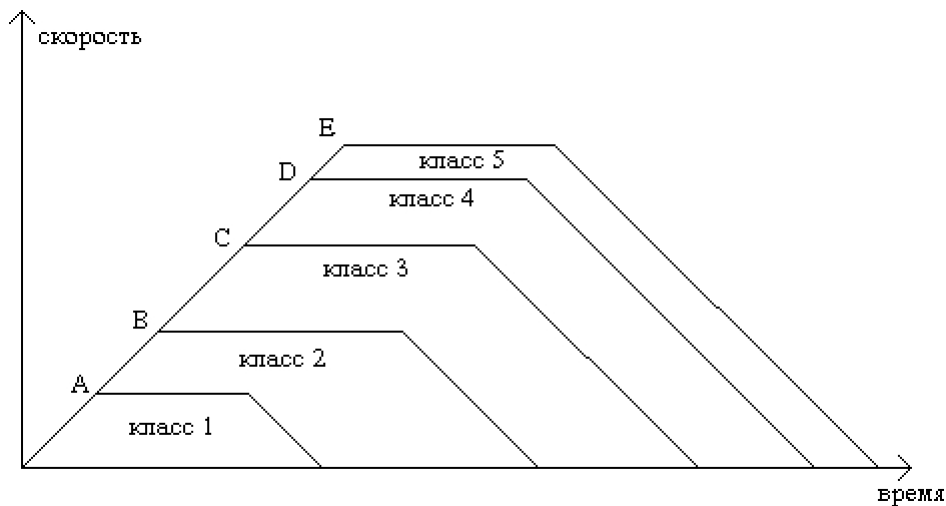
class	travel length
0	1
1	2...10
2	11...50
3	51...120
4	121...500
5	500...MAX

The servo information is placed in a completely different way when using the "Embedded servo" principle. During the manufacturing of the germoblock, the service information is recorded on each working surface with tags. The "micro-magnum" format is widely used as standard, Fig. 9.

СЕРВОМЕТКА

	синхрозона	код дорожки	код Грея		код проверки		сервоинформ. для подстройки		Формат данных
дор.0	00000000	0000XXX	0111	0111	XXXX	XXXX	AAA		
								BBB	
дор.1	00000000	0000XXX	0110	0110	XXXX	XXXX	AAA		
								BBB	
дор.2	00000000	0000XXX	0010	0010	XXXX	XXXX			

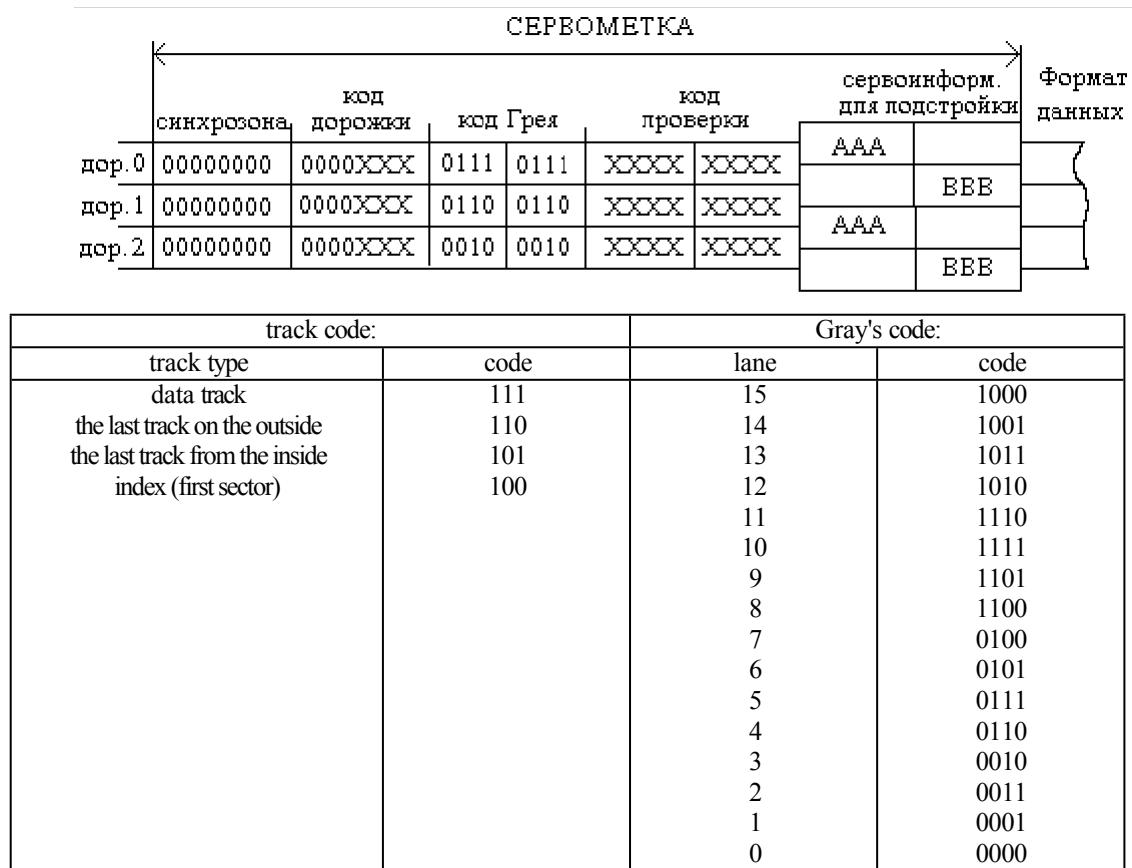| track code:		Gray's code:	
track type	code	lane	code
data track	111	15	1000
the last track on the outside	110	14	1001
the last track from the inside	101	13	1011
index (first sector)	100	12	1010
		11	1110
		10	1111
		9	1101
		8	1100
		7	0100
		6	0101
		5	0111
		4	0110
		3	0010
		2	0011
		1	0001
		0	0000

Figure 9. Servoformat "micro-magnum".

The servo system operates similarly to a dedicated servo surface system. The difference is that the service information between sectors is extracted from the drive data stream and arrives in batches. Therefore, after moving to the desired cylinder (even with head switching), it is necessary to skip several sectors to fine tune to the track. When performing write/read operations, in order to prevent the servo mark from being erased, the servo controller does not send a write signal to the channel until the servo mark has been completely read and identified. When it is read, the servo controller generates sector pulses SEC/DRUN, which are input to the single-chip microcontroller, Fig. 4.

1.1.3. Scoring/Recording Channel.

The read/write channel is discussed in detail in [1]. In IDE AT HDDs, the read/write channel has not changed much compared to the latest ST506/412 RLL drives. All changes are mainly due to new element base and denser information encoding methods such as ARLL [2]. An important feature of modern HDDs is the use of zone-by-section recording (ZBR), in which the entire disk space is divided into zones and in each zone a certain number of sectors per track are written. The number of zones on 3-inch magnetic disks can reach 20, and the number of sectors in the zones, depending on the capacity ranges from 90 - 140 in the very first zone and smoothly decreases to the last, where it can reach 40 - 70. This method is also called the method with constant recording density. Naturally, the read/write channel of such a drive must operate at different frequencies, with the first zone operating at the highest frequency and providing the highest data read rate. Such drives use tunable digital filters to correct the frequency response of the channel. IDE AT HDDs use data reading processors with AGC that support RLL coding, mainly 10206, 32P541 at the first

and 32P544, 32P3030, 32P4752 on later models. The well-proven chips 32R117, 32R510, 32R4610 are used as switches - read/write preamplifiers for ferrite MGs, and 32R520, 32R522, 32R2020, etc. for thin-film MGs.

1.1.4. Data Separator and Precompensation Records.

The data separator and the write precompensation circuit are often placed on the same chip, although they are practically unrelated to each other and function quite separately. The main purpose of the data separator is to clean the digital signal from read noise and to isolate the RCLK synchronization signals. The structure diagram of the data separator is shown in Fig.10.
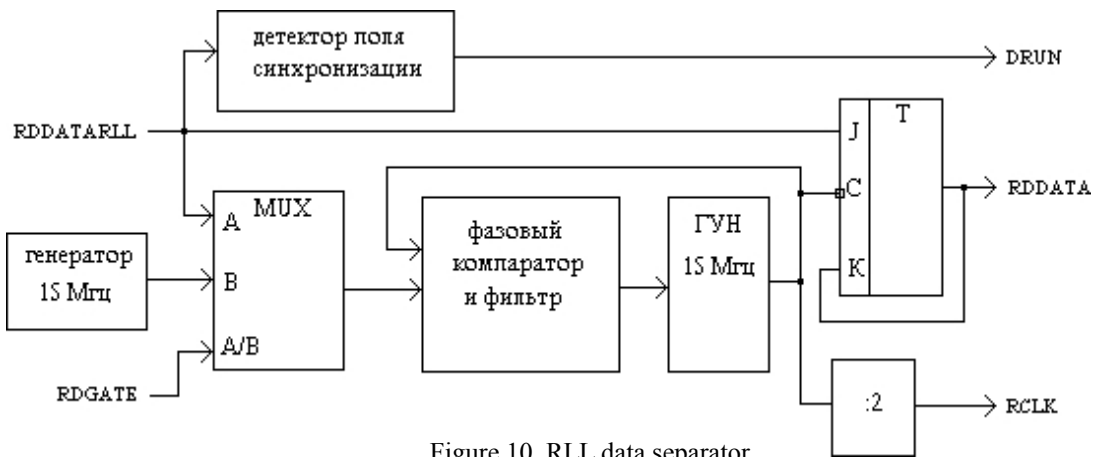

Figure 10. RLL data separator.

The RLL method (as well as any other non-zero return method) requires initial phasing of the data allocation strobe; for this purpose, special synchronization zones consisting of a sequence of zeros are available in the write format. The read data RDDATARLL (READ DATA RLL) from the read channel of the HDD enters the synchronization field detector, which extracts a zone of continuously consecutive ones or zeros from the stream of consecutive pulses. The detector is a resettable single-vibrator with a pulse width slightly longer than the period of the data pulses for zeros and ones. Thus, when a synchronization field passes under the read/write head, the detector produces a DRUN signal (DETEÑTOR RUN). In response to the DRUN signal, the single-chip microcontroller generates a read strobe RDGATE (READ GATE). This signal opens input A of the multiplexer and the read data RDDATARLL goes to the phase comparator, which produces an analog signal that controls the frequency of the GUN generator. The level of the analog signal depends on the phase mismatch between the RDDATARLL input data and the output signal of the GUN. The phase comparator, its ripple smoothing filter, and the GUN form a closed loop of phase frequency autotuning (PFA). In this way, the frequency change of the input signals is monitored and the reliability of the readout data is ensured. To ensure normal operation of FAPF in the absence of signal RDGATE multiplexer is switched to input B and synchronization of GUN is made from a quartz oscillator 15 MHz. It is necessary to make a note: since the pulse repetition period for zeros and ones coincides with Fig. 11, the DRUN signal will be erroneously formed not only when the synchronization field, but also in any other place where the sequence of zeros or ones is encountered. Therefore, in the track format, the synchronization field is followed by an address marker byte written in violation of coding rules (skipping one sync pulse). This byte cannot occur anywhere else in the track format. At the DRUN signal, the single-chip microcontroller starts searching for the address marker, if AM is not detected, therefore, this sequence of ones or zeros is not a synchronization field.

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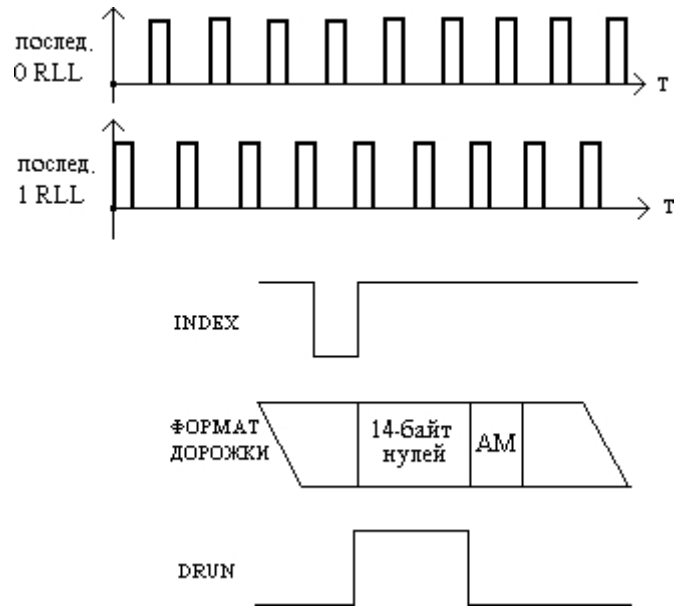
Figure 11. Assignment of address marker (AM).
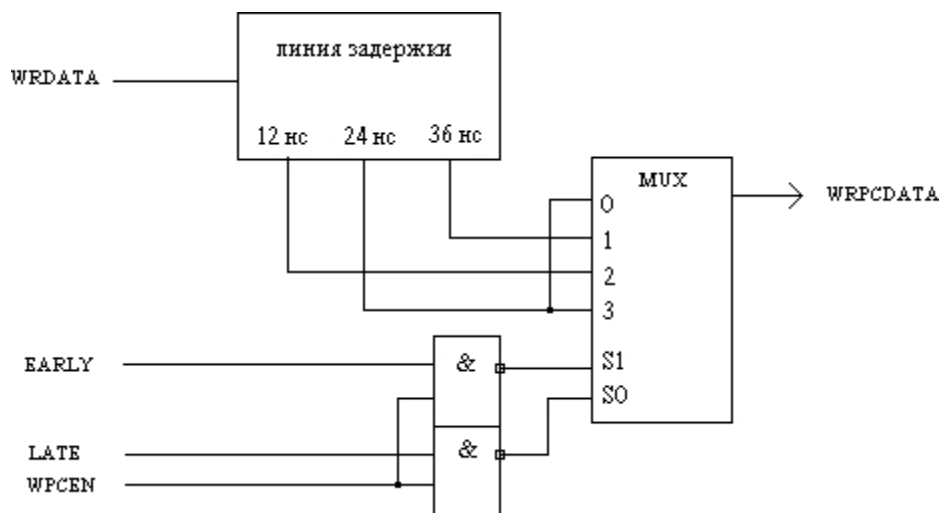
Figure 12. Schematic of precompensation.

The purpose and principle of precompensation are discussed in detail in [1]. The structural diagram of the precompensation node is shown in Fig. 12.

The EARLY and LATE signals are generated by a single-chip microcontroller based on the preliminary analysis of the recorded information. The WPCEN precompensation enable signal (WRITE PRECOMP. EN.) is generated by the control microprocessor. In the absence of precompensation WPCEN=0, the recorded data appears at the output delayed by 24 ns, which is considered zero deviation.

1.1.5. Single-chip microcontroller.

The single-chip microcontroller is the most complex element of the IDE AT HDD and is a determinant in the speed of data exchange between the HDD and HOST. The structural diagram of the single-chip microcontroller is shown in Fig.13.

Fig.13. Structural diagram of a single-chip microcontroller.

The microcontroller has four ports with which it is connected to HOST, local microprocessor, RAM buffer and data exchange channel with HDD. The microcontroller is a finite state machine controlled by the local microprocessor, from the HOST side only the standard registers of the job file are available. Programming of the single-chip microcontroller is performed at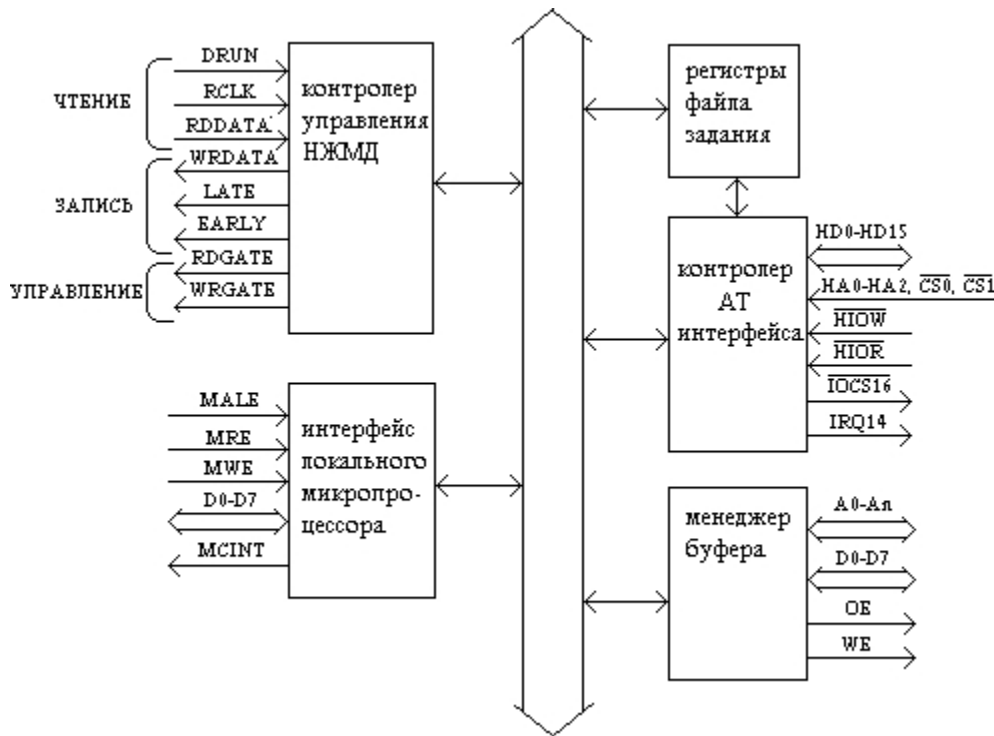 the initialization stage from the local microprocessor side, at that one of three coding methods MFM, RLL or NRZ is set, the SRS or ESS mode is selected [3], the mode of flexible or hard sector partitioning is set (flexible mode is used in IDE AT HDDs with zone-sectional recording, see below). The local microprocessor controls the buffer manager, the HDD controller, and the interface controller operating mode (some microcontrollers can operate in AT or XT mode). Typically, the local microprocessor is in the idle state until the microcontroller's MIÑINT (MIÑROÑONTROLLER INTERUPT) request is activated. In AT mode, MSINT is set when HOST writes to command register 1F7H . The buffer manager manages the buffer RAM, whose capacity ranges from 8 KBt to 256 KBt and depends on the specific micro-controller used. The buffer manager divides the entire buffer RAM into individual sector buffers. Special registers, accessible from the local microprocessor side, contain the starting addresses of these sector buffers. When HOST exchanges data with one of the sector buffers via FIFO, the HDD controller can exchange data with the other sector buffer. The HDD management controller is designed to exchange data between the data read/conversion channel, HDD write channel and together with the buffer manager - buffer RAM, in addition, the HDD management controller performs the formatting of the track, so in the reference documentation you can meet the name FORMATTER & DISK INTERFAÑE (FORMATTER & DISK INTERFAÑE). Fig.14 shows the read path of the HDD management controller, and Fig.15 shows the write path. When performing a read from the data separator comes the DRUN control signal (when the synchronization field is found). By this signal the address marker detector in the input data stream tries to detect AM and, if it is detected, the START signal is sent to the decoder, which starts converting the input data into a binary serial code. The scheme of the MCC check and error correction detects and, if possible, corrects the errors, the NO ERRORS signal is generated as a result of the check. The serial data is then converted to parallel data. When a write is performed, the data byte is converted into a post code and fed into the RLL oscillator circuitry, which generates WRDATA write data at WCLK frequency. Depending on the combination of the data bits, the EARLY and LATE correction signals used by the precompensation circuitry are generated. The MCC generator circuitry counts the control-cycle code of the input serial data stream. The generated MCC bytes are appended to the data being written.

The RLL generator generates a byte of address marker (generated with violation of coding rules). At the WRITE AM signal, the RLL generator generates a byte of address marker (generated with violation of coding rules).
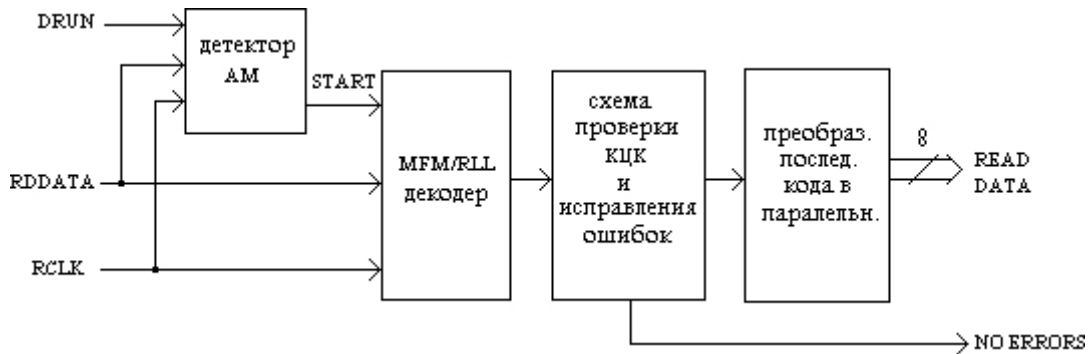
Figure 14. Reading path.
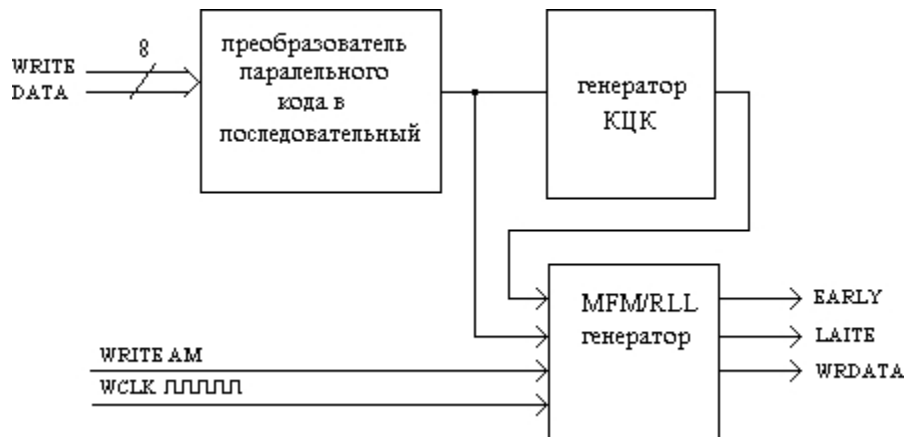
Figure 15. Recording path.

The LVMD control controller is the most complex part of a single-chip microcontroller and is a finite state machine that performs the functions:
- address marker search;
- reading the sector;
- reading all sectors on the track;
- sector record;
- recording all sectors on the track;
- ID record;
- formatting a single sector;
- track formatting.

The HDD controller is controlled by means of control registers accessible from the local microprocessor. The leading companies in the production of bottom-chip microcontrollers for IDE AT HDDs are: Adartes Inc., Cirrus Logic Inc., Western Digital Corp. and Chips & Technologies. A number of HDD manufacturers, Seagate Technology, Quantum Corp. and others, create their own controller BICs with the help of production service divisions of such firms as Texas Instruments Inc., Silicon Sistems Inc. Table 1 shows single-chip microcontrollers and models of HDDs in which they are used.

Table1.

Manufacturing company	Microcontroller	Models of HDDs where it is used
Adaptec Inc.	AIC-010 AIC-6060 AIC-6070 AIC-7160 AIC-7165, AIC-7166 AIC-7170, AIC-7171 AIC-8265, AIC-8267	ST157A family CP-3xxx, Samsung SHD-3062A ALPC DR311C91A, ST3290 Maxtor 7131AT, ST3390A. Maxtor 7171A, 7345AT. Maxtor 7425A CFA540A, Samsung PLS-31274A
Western Digital	WD42C22 WD61C25	WD9xxxxA families; PYRANHA; CAVIAR arh. 0; Family CAVIAR arh. 1; Ultra Lite
Cirrus Logic Inc.	CL-SH260/265 CL-SH360/362 CL-SH365/366	KC-40GA, ST351A/X, ST1144A, ST3144A; CP-3xxx family, Maxtor 7080AT, 7120AT. Maxtor MXT540A; CFSxxxA, CFAxxxA families.

Not so long ago the most widespread single-chip microcontroller was SL-SH260 and its modernized analog SL-SH265. This controller was used in approximately 60% of all 100 - 200 MBt IDE AT HDDs produced. Microcontroller AIS-6060 is compatible in pin layout and register assignment with the device SL-SH260, but surpasses the latter in speed by 50% and contains additional branching registers with write-only capability. The structural diagram of the SL-SH260 microcontroller is shown in Figure 16.

The SL-SH260 supports XT and AT interface protocol. The external plug-in buffer can have a capacity of 64 KBt of static memory. The maximum NRZ read data rate is up to 15 Mbps. The controller provides 16-bit SRS or 56-bit ESS error control and correction. The microprocessor interface is compatible with the Intel 8051 or Motorola 68HC11 families. It is manufactured in an 84-pin PLCC or 100-pin QFP package. Newer single-chip microcontrollers of the SL-SH360 family are the SL- SH361/364/366- provide NRZ data rates up to 32 Mbps and have hardware error detection and correction circuitry for 16-bit Reed-Solomon polynomial 16-bit SRS and 88-bit ESS. SL-SH4600 family microcontrollers provide NRZ data transfer rate up to 72 Mbit/s, external buffer capacity can reach 128 Kbt for static memory and 4 Mbt for dynamic memory.
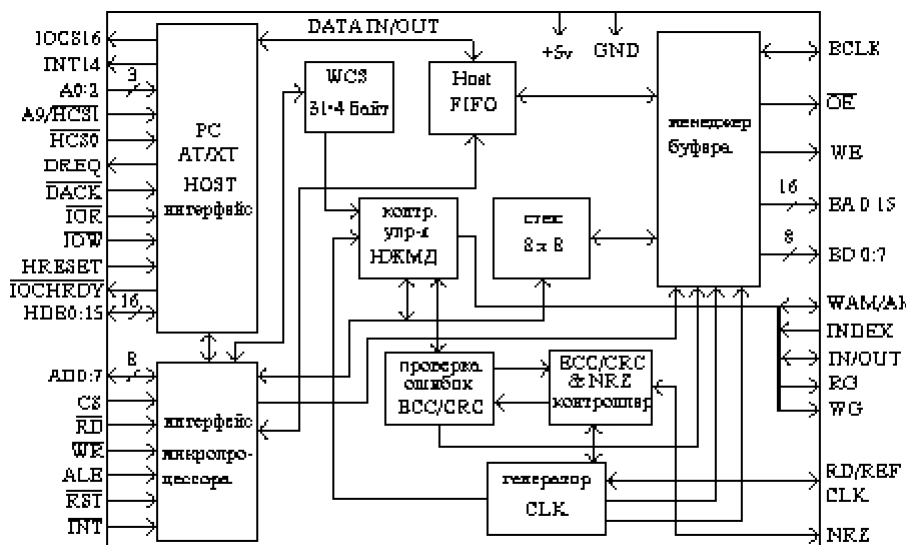

Fig.16. Structural diagram of the SL-SH260 microcontroller.

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1.2. IDE Interface AT.

1.2.1. OrsaniZation of the IDE AT interface.

The term IDE (Imbedded Drive Electronics) defines any system level interface, the abbreviation AT means that the system is an IBM AT or compatible computer. The IDE interface was proposed in 1988 for users of IBM PC/XT and AT computers. The distinctive feature of this interface is the implementation of controller functions on the HDD board. Despite the widespread use of this interface in IBM AT computers, it was not standardized until 1990 under the name ATA (ANSI X3T9.2/90- 143). This appendix describes the basic commands of the ATA interface, in addition to them, the ATA standard contains a number of additional commands that are not used by all HDDs:

- multisector data transfer commands Read Multiple, Write Multiple, Set Multiple;
- DMA mode data transfer commands Read DMA, Write Idle Immediate, Standby DMA;
- power saving commands (Power Mode) - Sleep, Idle, Standby, Immediate;
- commands for configuring the drive operation modes (Set

Features). The IDE AT interface configuration is shown in Figure
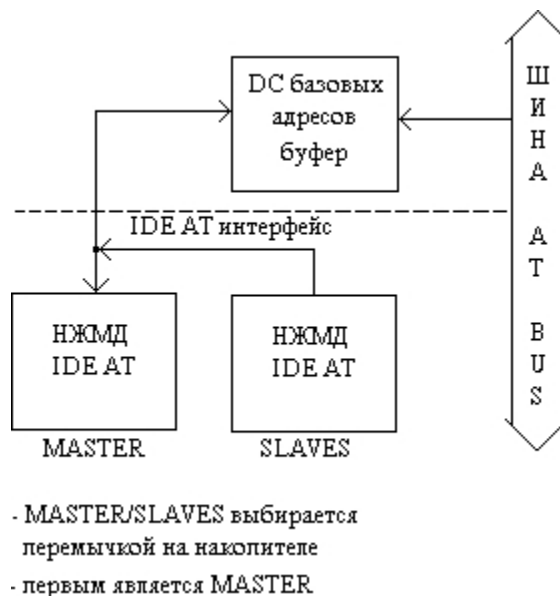
17.

Figure 17. IDE AT interface configuration.

The board, which is included between the system bus of the computer and the HDD, performs the functions of the controller base address decoder and interface signal shaper. In the IDE AT standard, two HDDs, MASTER and SLAVE, can be connected. The drive mode is switched by a jumper, with MASTER being the first logical drive. The IDE AT interface supports only program I/O using the IRQ14 hardware interrupt. Physically, the interface is implemented as a flat 40-pin cable, with a recommended length of 50 cm. Signal distribution by pins is shown in Table 2.

Table 2.

Contact	Symbol	Direction	Assignment
1	/HOST RESET	from HOST	Reset signal from system HOST
2	GND	General	
3	HOST DATA 7	bidirectional.	
4	HOST DATA 8	bidirectional.	16-bit bidirectional data bus between HOST and the drive
5	HOST DATA 6	bidirectional.	
6	HOST DATA 9	bidirectional.	
7	HOST DATA 5	bidirectional.	
8	HOST DATA 10	bidirectional.	

Continued Table 2.

9	HOST DATA 4	bidirectional.	16-bit bidirectional data bus between HOST and the drive
10	HOST DATA 11	bidirectional.	
11	HOST DATA 3	bidirectional.	
12	HOST DATA 12	bidirectional.	
13	HOST DATA 2	bidirectional.	
14	HOST DATA 13	bidirectional.	
15	HOST DATA 1	bidirectional.	
16	HOST DATA 14	bidirectional.	
17	HOST DATA 0	bidirectional.	
18	HOST DATA 15	bidirectional.	
19	GND	General	
20	KEY		The key, used to properly
21	DMARQ	to HOST	DMA Request
22	GND		General
23	/HOST IOW	from HOST	Strobe for writing data to registers
24	GND	General	
25	/HOST IOR	from HOST	Strobe for reading data from registers
26	GND	General	
27	IO CH RDY	to HOST	The readiness of the NJMD to exchange dan.
28	SPSYNC; CSEL	from HOST	Spindle synchronization signal
29	DMACK	from HOST	DMA Confirmation
30	GND		General
31	HOST IRQ14	to HOST	Interrupt request of HDD to HOST
32	/HOST IO CS16	to HOST	Indicating to HOST that it is addressed 16-.
33	HOST ADR1	from HOST	Used to select registers
34	/PDIAG		Used by SLAVE drive,
35	HOST ADR0	from HOST	Used to select registers
36	HOST ADR2	from HOST	Used to select registers
37	/HOST CS0	from HOST	Used to select registers
38	/HOST CS1	from HOST	Used to select registers
39	/HOST SLV/ACT	to HOST	It has a dual purpose:
40	GND		General

Note. The name of some signals in different technical documentation may differ.

All signals of the IDE AT interface can be categorized into groups.

Buffered standard ISA bus signals of the PC AT personal computer:

/HOST RESET (has a non-inverse value on the ISA bus);
HOST DATA 0-15;
/HOST IOR;
/HOST IOW;
IO CH RDY;
HOST ALE;
HOST IRQ14;
/HOST IO CS16;
HOST ADR0;
HOST ADR1;
HOST ADR2;
DMARQ;
DMACK.

Additional signals to address the job file:

HOST CS0;
HOST CS1.

MASTER/SLAVE interaction signals between MASTER/SLAVE HDDs:

PDIAG;
HOST SLV/ACT.

Control signal transmitters - TTL circuits must provide current:

IoL not less than 12 mA,
IoH - 400 uA

1.2.2. I/O ports, NMMD IDE AT commands.

Exchange between HOST and IDE AT HDD is carried out through program-accessible input/output registers, for addressing to which the area with addresses 1F0H - 1F7H, 3F6H, 3F7H is allocated. Program-accessible registers of IDE AT HDD are presented in Table 3.

Table 3.

Address (NEH)	Reading	Recording
1F0	Data register	Data register
1F1	Error register	Precompensation register
1F2	Sector counter register	Sector counter register
1F3	Sector number register	Sector number register
1F4	Cylinder number register ml.	Cylinder number register ml.
1F5	Cylinder number register st.	Cylinder number register st.
1F6	Drive/head register	Drive/head register
1F7	Status register	Command register
3F6	Register of Alternative Composition.	Drive status
3F7	Drive address register	Not used

The data register (1F0 read/write) is used when performing sector read or write operations in program I/O mode. This register is not available until a read or write operation is started. Data transfers are performed in 16-bit words. When performing long read or write operations (when MCC bytes are transferred along with data), 4 bytes of the ECC are transferred in bytes, bit 3 "Data request" of the Status Register is re-set before the ECC bytes are transferred.

The error register (1F1 read) determines the state of the HDD after an operation has been performed. The state of this register is valid:
- after the command is executed if the "Error" bit in the status register is set;
- after executing the "Diagnostics" command or after performing internal HDD diagnostics by system reset.
In diagnostic mode, the error register codes define the following: 01H - no error;
02H - microcontroller error; 03H -
buffer RAM error; 04H - ESS
hardware error; 05H -
microprocessor error 8XH - HDD
faulty.

The values of the error register bits after the command has been executed:

7	6	5	4	3	2	1	0
BBK	UNC	0	IDNF	0	ABRT	TONF	AMNF

Bit 0 - Data Adres Mark Not Found - set during the execution of the "Sector Read" command, if the data address marker of the corresponding sector is not found after the correct finding of this sector identifier.
Bit 1 - Trask 0 Not Found - set only in the command
"Recalibrate" if track 0 is not detected after 2048 steps.
Bit 2 - Aborted Command - is set when a "Write fault", "Not seek complete", "Drive not ready" status is received from the HDD or when an invalid command has been loaded. The cause of the error can be determined using the status and error registers.
Bit 3 - not used (equal to 0).

Bit 4 - ID Not Found - the desired cylinder, head, or sector could not be found or an ESS error occurred in the ID field.

Bit 5 - not used (equal to 0).

Bit 6 - Unsorrect Data - ESS error in the data field. It is set in case of uncorrectable error. Bit 7 - Bad Mark Lock - defective sector mark is detected in the identifier.

The precompensation register (1F1 entry) was used to specify the cylinder number from which to precompensate. In modern IDE AT HDDs, precompensation is controlled by the drive itself, so this register can be used for other purposes.

The sector counter register (1F2 read/write) contains the number of sectors for a write or read operation. The value of this register is decremented by 1 when each sector is processed. A single sector transfer occurs at a value of 1, while a value of 0 results in 256 sectors. If a write or read error occurs during a multi-sector transfer, the transfer is terminated and the sector counter register contains the number of sectors remaining after the error was detected. If the command is successfully completed, the contents of this register is 0.

The sector number register (1F3 read/write) contains the starting sector number for read/write operations. After each sector is processed, the contents of this register are incremented. After the command is executed, this register contains the number of the last processed sector or the number of the sector in which an error occurred.

Register of the low (1F4 read/write) and *high* (1F5 read/write) bytes of *cylinder number* define the cylinder number for which the command will be executed.

The NMMD/head number selection register (1F6 read/write) is as follows:

7	6	5	4	3	2	1	0
1	0	1	DRV	HS3	HS2	HS1	HS0

Bits 0 - 3 are the binary code of the selected head,

Bit 4 - HDD selection,   DRV = 0 HDD 0 is selected,

DRV = 1 selected HDD 1.

The status register (1F7 read) displays the current status of the IDE AT HDD. The value of this register is updated after each command is executed. If the BSY bit of this register is set, any accesses to the HDD are denied and the other bits of the status register are invalid. Reading this register resets the IRQ14 hardware interrupt. Status register bit values:

7	6	5	4	3	2	1	0
BSY	DRDY	WFT	DSC	DRQ	CORR	INX	ERR

Bit 0 - Error - indicates that the previous command ended with an error and that one or more bits are set in the error register. It is used for quick verification of successful completion of the command. It is reset when a new command is sent to the command register.

Bit 1 - Index - this bit is set to 1 at each revolution of the magnetic disk. It is not used in modern HDD models.

Bit 2 - Corrected Data - indicates that an error occurred while reading data from the disk, which was successfully corrected by the MCC hardware. Corrected errors do not stop multisector transmission.

Bit 3 - Data Request - this bit indicates that there is a request to exchange data with the sector buffer when executing read/write commands. This request is to read the buffer or send data to the buffer, depending on the command being executed.

Bit 4 - Drive Seek Complete - indicates that the read/write heads have completed the seek operation.

Bit 5 - Write Fault - indicates a fault in the drive or an attempt to execute a write command with incorrect parameters.

Bit 6 - Drive Redy - set to 1 means that the HDD is ready to execute the command.

Bit 7 - Busy - determines the state of the IDE AT HDD. It is set to 1 during command execution or HDD diagnostics after a system reset. When this bit is set, no other bits of the Status Register are valid. The Busy bit must be checked before reading any status register.

The command register (1F7 write) is used to load the command to be executed. Before writing a command to the command register it is necessary to prepare the Task File (write the necessary data to registers 1F1 - 1F6), when the HDD is in the "not busy" state (Busy=0). The command execution starts from the moment of writing to the command register.

The Alternate Status Register (3F6 read) contains the same information as the Status Register (1F7). The difference is that reading this register does not reset the set interrupt IRQ14 of the HDD.

7	6	5	4	3	2	1	0
BSY	DRDY	WFT	DSC	DRQ	CORR	INX	ERR

The ystroĭ status register (3F6 write) contains three control bits.

7	6	5	4	3	2	1	0
				HS3EN	SRST	/IEN	

Bit 1 - Interrupt Enable - The interrupt enable bit for the HDD to HOST. When this bit is active and the drive is selected, HOST is interrupted. The HOST IRQ14 signal must be enabled through a 3 - stable buffer. When this bit is not active or the HDD is not selected, the HOST IRQ14 signal will go high.
Bit 2 - Soft Reset is a software reset bit. The drive performs a reset when this bit is high.
Bit 3 - Heads 3 Enable - used to enable the selection of heads 8 through 15.

The drive address register (3F7 read) contains the head number and HDD selected in the previous operation.

7	6	5	4	3	2	1	0
	WG	/HS3	/HS2	/HS1	/HS0	/DS1	/DS0

Bits 0, 1 - /DS0, /DS1 - bits for selecting the corresponding drive 0 or 1. Bits 2...5 - /HS0.../HS3 - contain the binary code of the selected head.
Bit 6 - Write Gate - write execution bit, active during a write operation

1.2.3. Addressing the IDE AT NMMD Resistors.

Signals are used to address the registers of the IDE AT HDD:
HOST ADR0, HOST ADR1, HOST ADR2 - to select the HDD registers;
/HOST SS0, /HOST SS1 - to select the HDD registers;
/HOST IOW - strobe for writing data to HDD registers;
/HOST IOR - strobe for reading data from HDD registers.

Table 4.

/CS0	/CS1	HA0	HA1	HA2	Reading registers by strobe /IOW	Writing to registers by strobe /IOR
0	1	0	0	0	1F0	1F0
0	1	0	0	1	1F1	1F1
0	1	0	1	0	1F2	1F2
0	1	0	1	1	1F3	1F3
0	1	1	0	0	1F4	1F4
0	1	1	0	1	1F5	1F5

0	1	1	1	0	1F6	1F6
0	1	1	1	1	1F7	1F7
1	0	1	1	0	3F6	3F6
1	0	1	1	1	3F7	3F7

1.2.4. Description of NMMD IDE AT commands.

Commands from HOST are written to the command register 1F7 and are executed immediately. Before writing a command in registers 1F2-1F6, a task file (Task File) is formed, which contains the data. necessary to execute the command. The command codes are shown in Table 5.

Table 5.

Team	Command code	Registers used				
		1F2	1F3	1F4	1F5	1F6
Internal diagnostics	90H	-	-	-	-	D
Formatting a track	50H	Y	-	Y	Y	Y
HDD identification	UST	-	-	-	-	D
Initializing HDD parameters	91H	Y	-	-	-	Y
Recalibration	10H	-	-	-	-	D
Buffer reading	E4H	-	-	-	-	D
Reading sector(s)	2XH	Y	Y	Y	Y	Y
Verification	41H	-	Y	Y	Y	Y
Positioning	70H					
Writing buffer	E8H	-	-	-	-	D
Recording sector(s)	3XH	Y	Y	Y	Y	Y

Y - register contains data used in the execution of the command.

D - in register 1F6 (HDD selection and head number) only HDD selection is used X = 00LR -

low tetrad for sector read and write commands.

L - long operation mode:

L=0 - normal mode, SRS or ESS functions are performed;

L=1 - long operation mode. No CRC or ECC bytes are generated, occurrence of errors in the data field is not checked. When reading and writing a sector, 4 bytes of the user's MCC are added.

R - repeat mode when an error occurs:

R=0 - repetition is allowed; R=1 -

repetition is prohibited.

Internal diagnostics (90H) - internal diagnostics of the HDD is performed, after completion of which a termination code is formed in the error register. If there are no errors, the termination code is 01H.

Track Format (50H) - This command writes the lower level format to the specified HDD track. On many IDE AT drives, track formatting is performed when the process mode is enabled.

NMMD Identification (USN) - This command reads the disk passport into the sector buffer and generates a DRQ request in the status register.

Initialize HDD parameters (91H) - This command configures the HDD to the parameters set to the drive from HOST. This command must be executed after the HDD has been "reset".

Recalibrate (10H) - This command sets the LVMD heads to cylinder 0.

Buffer Read (E4H) - This command sets the DRQ request in the status register. HOST can read the contents of the 256 word buffer through the data register.

Read *Sector(s)* (2XH) - This command reads the specified sector into the sector buffer (typically 512 bytes) and generates a DRQ request. HOST can read the contents of the 256 word buffer through the data register. The L and/or R bits may be set in the command. The contents of register 1F2 indicates the number of sectors to be read (if 1F2=0, 256 sectors are written), the contents of register 1F3 indicates the starting sector.

Verify (41H) - this command verifies the format of the specified track.

Positioning (70H) - This command sets the HDD heads to the specified cylinder.

Buffer Write (E8H) - This command sets the DRQ request in the status register, after which HOST must forward 256 words through the data register.

Write Sector(s) (3XH) - This command sets the DRQ request in the status register and requires HOST to send 256 words through the data register. The data is then written to the magnetic disk. The L and/or R bits can be set in the command. The contents of register 1F2 indicates the number of sectors to be written (if 1F2=0, 256 sectors are written), the contents of register 1F3 indicates the starting sector.

1.3. Service Information HDD IDE AT.

Service information of an IDE AT HDD is necessary for the operation of the circuits of the HDD itself and is usually hidden from the user. Service information can be categorized by type:
Service Information;
Work programs;
Lower Level Format;
Configuration Table;
Disk Passport;
Faulty sector table.

Service information is required for operation of the servo system of the magnetic head drive system of solenoid-motor driven LVMDs and stepper-motor driven LVMDs with pulse-width phase control. On the majority of modern PLMDs service information is also used to stabilize the spindle motor rotation speed. The Dedicated type service information is located on a separate surface, while the Embedded type service information is located directly on the working surface between the sectors. There is no service information on the first models of IDE AT HDDs with a stepper motor (ST157A, KL-343). In such models, positioning and finding the zero track is performed by steady steps and the format of the lower level.

Working programs (microcode) of the control microprocessor represent a necessary set of programs for operation of the HDD hardware. They include programs for positioning hardware control, information exchange with the single-chip microcontroller and buffer RAM, initial diagnostics, etc. In the majority of HDD models the working programs are placed in the internal ROM of the control microprocessor, some models use external ROM (KALOK, Sopper, Maxtor, Samsung drives). In some models of HDDs the part of working programs is stored on the magnetic disk, and in the internal ROM of the control microprocessor the initial initialization, positioning programs and the primary loader for reading the working programs from the magnetic disk into the RAM are stored. So, for example, in the model ST351A / X external firmware occupies 19 sectors for work on the interface AT, and 19 sectors for work on the interface HT. Depending on the jumpers installed, either one or the other firmware is reloaded into the drive's RAM during initialization. In the ST3144AT family of drives, the external firmware occupies 32 sectors and is reloaded into RAM during initialization. In more modern ST3660A drives, the service information is presented in the form of an OSMS (operating system for managing the hard drive); all programs and tables are stored in the service area as modules under their own names. During initialization, a boot loader is read that contains the module location directory and the drive loads the individual modules into RAM during operation.
Hard disk drive manufacturers place some of the firmware on the surfaces not only to save space in the ROM, but also for possible replacement of it, if suddenly during the production process or

The firmware will be found to have an error. It is much easier to rewrite the firmware on disk than to re-solder "flashed" microprocessors, especially if the monthly volume of the manufacturing plant is 20 - 30 thousand drives.

Lower level format. The structure of the WD42C22A microcontroller track format is shown in Figure 18.

СЕКТОРА НА ДОРОЖКЕ

1-ЫЙ СЕКТОР

ПОЛЕ ИДЕНТИФИКАЦИИ — ПРОБЕЛ 1 — ПОЛЕ ДАННЫХ — ПРОБЕЛ 2 — ПРОБ.3

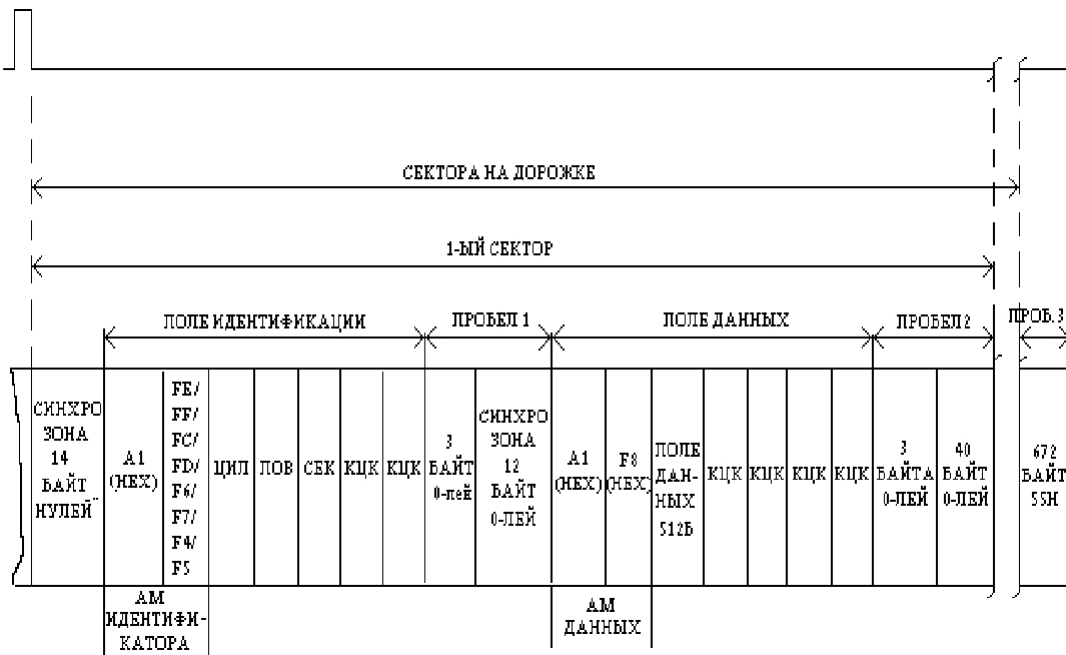| СИНХРО ЗОНА 14 БАЙТ НУЛЕЙ | A1 (HEX) | FE/ FF/ FC/ FD/ F6/ F7/ F4/ F5 | ЦИЛ | ПОВ | СЕК | КЦК | КЦК | 3 БАЙТ 0-ГЕЙ | СИНХРО ЗОНА 12 БАЙТ 0-ЛЕЙ | A1 (HEX) | F8 (HEX) | ПОЛЕ ДАН-НЫХ 512B | КЦК | КЦК | КЦК | КЦК | 3 БАЙТА 0-ЛЕЙ | 40 БАЙТ 0-ЛЕЙ | 672 БАЙТ 55H |

АМ ИДЕНТИФИ-КАТОРА

АМ ДАННЫХ

Fig.18. Structure of the track format.

The start of the track is defined by an index pulse. The number of sectors on the track depends on the encoding method used and the spindle motor speed. The format of each sector contains an identification field, a data field, synchrozones and spaces. At the beginning of the track is a synchrozone containing 14 bytes of zeros, which serves to phase and synchronize the data allocation strobe. The identification field contains the address marker, cylinder address, surface address, sector address, and two bytes of the control-cycle code. Byte A1, which is included in the address marker, is written in violation of the coding rules by skipping one synchronization pulse, this makes it different from any other A1 byte encountered on the track. The address marker of the identification field also includes the cylinder number code:

FE, cylinder 0-255; FF,
cylinder 255-511; FC,
cylinder 512-767;
FD, cylinder 768-1023; F6,
cylinder 1024-1279; F7,
cylinder 1280-1535; F4,
cylinder 1536-1791; F5,
cylinder 1792-2047.

Between the identification field and the data field is space 1, which includes 3 bytes of zeros and a synchrozone. The data field includes a data address marker containing bytes A1 and F8, data (the number of bytes is programmable) and 4 bytes of the MCC. Space 2 is used to avoid overlapping of two adjacent sectors if the disk was formatted at higher than nominal RPM and data is written at lower than nominal RPM. Space 3 serves as a damper of the disk speed deviation for the whole track. Different controller BICs tend to have their own format, but the format structure remains constant. The differences are mainly in the number of sectors on the track, the number of bytes in the data field, and the byte value of the check-cycle code. More recently, drives with constant density recording or what is also known as zone-section recording have been introduced. As it was discussed in detail in [1] in conventional HDDs, the recording density increases towards the center of the disk, and in HDDs with constant recording density, more sectors are placed on the outer tracks than on the inner tracks. This results in a significant increase in capacity compared to conventional HDDs.

The IDE AT drive *configuration table* provides information about the logical and physical organization of the disk space. This table is necessary so that the electronics board, which is the same for the entire family of drives, can be customized for a given model of the family. The point is that when you design a model, for example, 850 MBt on two disks, you automatically get a "half" model of 425 MBt on one disk. Thus, another sector of the market is blocked. In addition, the "half" model can use parts that do not fit the full model in any way. For example, spindle motors with increased runout or magnetic disks with defects in the last zone of the full model are used in the "half" model, which has fewer zones, etc. For example, Seagate's ST3660A family:

ST3660A 540 MBt - 7 zones, 4 work surfaces;
ST3490A 420 MBt - 5 zones, 4 work surfaces;
ST3295A 270 MBt - 7 zones, 2 work surfaces.

PLS-31274A Samsung Family:

PLS-31274A 1270 MBt - three working disks;
PLS-30850A 850 MBt - two working disks.

The IDE AT *drive disk data sheet* contains reference information about the configuration and characteristics of the HDD. The Disk Data Sheet occupies one sector (256 words) and is located in the service area and is intended for automatic system configuration or setting up software to work with the HDD. In some drives, the disk passport is stored in the ROM with the control firmware, and only the serial number is stored on the disk in the service area. To read the disk passport it is necessary to issue an identification command (USN) and then read the information from the sector buffer for analysis. Table 6 shows the main parameters read from the disk passport.

Table 6.

Word	Significance
0	The main word for configuration
1	Number of cylinders
2	Reserved
3	Number of heads
4	Number of bytes per track
5	Number of bytes in a sector
6	Number of sectors per track
10 - 19	Serial number (ASCII)
20	Buffer type
21	Buffer capacity divided by 512 bytes
23 - 26	Firmware version (ASCII)
27 - 46	Drive Model (ASCII)

According to Fast ATA-2 and Enhansed IDE specification, besides these data, the passport of a modern HDD IDE AT contains about 20 characteristics giving full information about the drive.

Defective Sector Table. In drives with ST506/412 interface, the table of defective tracks was placed on the germoblock case in the form of a sticker. Any drive had a capacity reserve, e.g. 20-ti MB ST225 HDD actually had 21.5 MB, i.e. 1.5 MB was allocated for faulty tracks. An IDE AT HDD also has excess capacity, but it is hidden from the user and is only available to the control microprocessor and the drive controller. Part of this excess capacity is allocated for the working programs of the HDD (if they are placed on the surfaces), the disk passport and the table of defective sectors. The remaining part is reserved for replacing bad sectors. Filling of the table of defective sectors is performed at the factory - manufacturer after formatting of the HDD, the numbers of all detected BAD-sectors are placed in the table. This procedure is called UPDATE DEFEÑT. Now, when the HDD is operating, if a hidden defective sector is accessed, the drive itself redirects the access to the backup sector. Therefore, all IDE AT drives that come from the factory do not have a single defective sector.

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Most models of modern HDDs have two defect tables: Primary and Grown. The Primary table is filled in at the factory during the process of technology testing. The Grown table is filled in during the drive's operation, when defective sectors appear in the drive, with the help of specialized technological utilities.

1.4. Logical organization of disk space.

In the ST506/412 HDD all disk space was available to the user, except for the following The "minus" tracks on which service information has been written in stepper motor drives or a separate servo surface in solenoid-driven HDDs. In IDE AT drives, a fairly large portion of the disk space is hidden from the user, containing service information and a reserve area for replacing failed sectors in the HDD. In normal drive operation it is only accessible to the internal microcontroller. This is possible because there is a concept of logical sector in IDE AT HDDs and HOST works with logical sectors rather than physical sectors of the drive. The physical sector identification field stores the value of the head, cylinder and sector similar to the ST506/412 drive format, the logical sector appears due to the recalculation of the parameters of the specified sector in the command (head, cylinder, sector) and the real disk space (physical format) by the drive's control microprocessor. The microcontroller can perform data writing and reading operations only on the surface on which the physical format is located (write sector, read sector, etc.), so the service information of an IDE AT HDD is also located in the data field of the physical format (service information is an exception). In the normal operation mode of the drive, during the zero sector read/write operation, the internal HDD controller "knowing" the structure of its disk space will recalculate logical sector parameters into physical ones and execute the command on the zero logical sector. When designing an IDE AT HDD model, the developers determine the service information required for the drive's operation and the number of cylinders occupied by it, so the logical zero cylinder is the first free cylinder following the last cylinder of service information. The structure of disk space in different models of IDE AT HDDs may differ from the one shown in Fig. 19, for example, in ST351A/X, ST3290A drives the logical zero cylinder starts from the eighth physical cylinder, in ST3144AT family - from the tenth, and in ST3660A family - from the fourth.
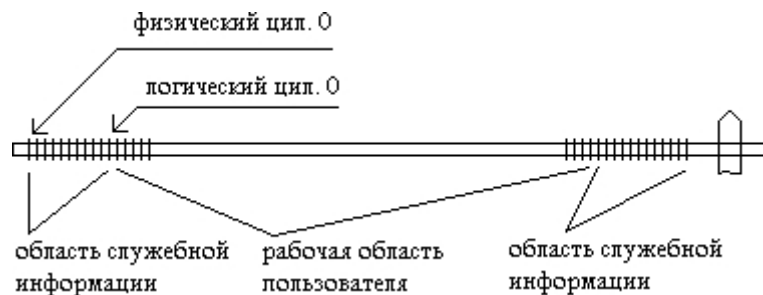
Fig.19. Example of logical organization of disk space of IDE AT HDD.

1.5. Mode broadcast.

The first models of ATA hard drives could work under their physical parameters and allowed to work with some logical type in SetUp of the computer. And in the disk passport of these hard drives were located exactly physical parameters, hence the term to set the drive under physical parameters.

Modern ATA drives support universal translation mode, where the main criterion for selecting drive parameters is the total number of user sectors for a given model. When setting parameters, the most important thing is to make sure that the product of the set cyl., gol., sec. does not exceed the total number of sectors of the drive. As a rule, the accompanying documentation on the

The best parameters in terms of capacity and the total number of sectors of the drive are specified. Most personal computer BIOSes have an auto-detect procedure that allows you to read the parameters from the drive's disk data sheet and set them in SetUp. Some hard disk drives, such as those made by Sopper, use the so-called adaptive translation mode, in which the drive itself alerts the user when its disk space is being used incorrectly. During initialization only two parameters, the number of heads and sectors, are passed to the drive, the drive itself adjusts its logical structure so that the total capacity does not change, the correction is made by changing the number of cylinders. If you read the data sheet of such a drive before initialization and after initialization, the read values of the parameters will be different, and the number of heads and sectors in the second case will correspond to the initialized parameters, and the number of cylinders will be corrected in accordance with the capacity. If the number of logical cylinders is greater than 1024 when initializing the computer, the user will lose some of the useful capacity of the hard drive.

1.6. Methods for hiding defects in IDE HDDs AT.

There are several algorithms for hiding defects:

Backup Sector Method. The essence of the method is that an additional sector is placed on each track of the drive, which is not available in the normal mode of operation, and if a defect is detected in any working sector of the track, a backup sector is included instead. In this way the drive can hide only one defective sector on a track. This method is ineffective if there are several defective sectors on the track. In addition, when using this method, there is a rather large loss of disk space due to the need to keep a backup sector on all tracks, regardless of whether they have defects or not. This defect hiding algorithm is used in Western Digital's WD93044A family of drives. In KALOK, HEWES drives, the backup sector is allocated per cylinder of the magnetic disk package, and the defect concealment capabilities are further reduced. There is a more improved algorithm when the reserve sector is allocated to a cylinder, but if it is occupied, the reserve is searched on the cylinder + (-) 1 from the defective one, if it is occupied there, then + (-) 2, etc. Such defect hiding algorithm is used in Piranha, Saviar architecture 0 and some Conner drives.

Backup track method. This method allows you to eliminate an entire track when a defect is detected on it. Drives using this defect hiding algorithm have a certain number of backup tracks outside the working area. The disadvantage of this method is, firstly, that it does not save disk space, since the entire track is excluded to hide one faulty sector, and secondly, the drive needs to position itself in the reserved area to read the reserved track. During initialization, a table of displaced tracks must be loaded into the drive controller "which track was moved where". This algorithm is used in Maxtor, Piranha, and Saviar architecture 0 drives to exclude tracks with corrupted servo labels.

Defective track skip method. In this method, a defective track is considered out of service and is "unnoticed" by the drive controller. To do this, a table of defective tracks is loaded into the controller during drive initialization. During operation, the drive takes the loaded defect table into account when calculating the track number and adds the number of the defect that was encountered before it to the calculated track number. In this way, the drive's workspace will move to the center of the drive, although there will be "empty" spaces. This method differs from the previous method in that it does not require additional positioning to the reserved area. This defect concealment algorithm is used in the ST157A family of drives.

Defective Sector Skip Method. This method is only applicable to drives that use the physical to logical parameter translation mode. In this method, as in the previous one, defective sectors are considered as non-working and are not "noticed" by the disk controller. A drive using this method contains special translator tables that are loaded into RAM during initialization and used by the translation program to calculate the physical sector number. This method is used by ST1144AT, ST3144AT, ST3290A, ST3660 and others. The method of skipping a defective sector provides the least loss of disk space and allows hiding almost any number of defective sectors. A more improved algorithm is used by Saviar architecture 1 drives, which contain absolute numbers of defective sectors in the translator table.

1.7. IDE HDD operation AT.

After the supply voltage is applied to the HDD or the /RESET interface signal is activated, the drive reset circuit supplies the RESET signal to the control microprocessor, which initializes the state of the I/O ports (this usually causes the spindle motor to stop), clears the working area of the data memory, and programs the single-chip microcontroller and all programmable chips located on the internal data bus of the HDD. After that, the control microprocessor polls the internal drive operation signals OZP, OSH.PIT, etc., and signals the spindle motor to start. The next stage of the microprogram operation is to perform an internal test of the HDD, which checks: Data buffer RAM, the single-chip microcontroller and the state of the microcontroller input signals on the port side of the HDD, see Fig.13. After that, the control microprocessor, analyzing the index pulse period, waits until the spindle motor does not gain the specified revolutions and, as soon as it happens, it, controlling the positioning circuit and single-chip microcontroller, moves the magnetic heads to the zone where the service information is recorded and sends it to the buffer RAM for further work. After that the control microprocessor sets bits 6 (DRDY) and 4 (DSC), resets bit 7 (BSY) in the HDD status register, and code 01 is sent to the error/precompensation register - no errors detected (these registers are located in the single-chip microcontroller). The drive can stay in this state for any length of time, waiting for a write to the command register - 1F7H. The IDE AT HDD is controlled by programmatically available registers 1F0H - 1F7H, 3F6H, 3F7H on the HOST side. Before writing a command to HOST- to check bit 7 (BSY) of the HDD status register, it must be reset. After that, the job file is prepared - the registers that are involved in the command to be executed (sector number register, drive/head register, etc.) are filled and the command is sent to 1F7H register. After writing to the command register, the single-chip microcontroller generates an interrupt request to the control microprocessor MCINT (Microcontroller Interupt), not to be confused with IRQ14. In processing the interrupt procedure, the drive's control microcontroller sets bit 7 (BSY) in the HDD status register and reads and interprets the contents of the command register. If a non-existing command was erroneously submitted, bit 2 (ABRT) is set in the error register and bit 0 (ERR) is set in the status register and bit 7 (BSY) is reset, then the HDD is ready to receive the next command. If the command code is recognized, the control microprocessor from the microcontroller reads the contents of the registers involved in the execution of this command, and control is transferred to the procedure for processing this command, upon completion of which bit 7 (BSY) of the status register is reset. If an error occurs, the error register is additionally formed and bit 0 (ERR) in the status register is set.

2. IDE HDD repair AT.

General principles of IDE AT HDD repair are described on the basis of using tests of the universal tester "PC-3000AT".

2.1. Interpreting Error Codes in IDE HDD Diagnostics AT.

After each command is executed, the HDD generates a status register and, if an error has occurred, an error register. Depending on the command issued and the value of the status and error registers, it is possible to judge the nature of the drive fault. If the command was executed without errors, only bits 6 (DRDY) and 4 (DSC) should be set when reading the status register. The following are the most typical faults that occur in IDE AT HDDs.

status register

BSY	DRDY	WFT	DSC	DRQ	CORR	INX	ERR

error register

BBK	UNC	0	IDNF	0	ABRT	TONF	AMNF

After all or most of the commands have been executed, the ABRT bit in the error register is set. This bit indicates that the command code is not recognized, therefore, either the control microprocessor incorrectly interprets them, or the single-chip microcontroller incorrectly translates them to the internal data bus of the HDD. The first reason can be either due to a malfunction of the microprocessor itself or due to destruction of the control program in the program memory. To check this, it is necessary to "RESET the HDD" and run "INTERNAL DIAGNOSTICS" from the "CONTROLLER TEST" menu. Many
Working programs are loaded from the disk into the buffer RAM (e.g. Seagate, Western Dig., etc.) and when they are destroyed, the ABRT error is generated, and an attempt to give any command, even internal diagnostics, may result in ABRT. The second reason may be due to a faulty chip of the single-chip microcontroller or, if some bus shaper on the internal data bus "undergrows" the signal, it can lead to distortion of the command code. The test "SECTOR BUFFER TEST" is used to check the internal data bus. ABRT error can also be caused by incorrectly selected configuration of the tested drive, we recommend using the tester database for correct testing.

The T0NF bit in the error register is set if the HDD failed to detect the zero track when executing the recalibrate command. This fault can occur because there is no physical format on track zero or because of a fault in the read/data conversion channel that prevents the HDD from reading the format. In linear motor drives, the T0NF error may occur because the service information has been destroyed and the HDD is unable to locate track 0. To check the correctness of finding the zero track it is necessary to apply the X->0 recalibration command in the "STORAGE TEST" mode and observe the result on the LED indicators of the status and error registers.

The remaining bits in the error register are related to HDD read/convert data channel faults, the faults are listed in decreasing order of fault severity:

IDNF - identifier not found. Identification field (specified head, cylinder and sector) is not found, more precisely address marker of the identification field is not found or, if AM of the identification field is found, the CCC of the identification field does not match, see Fig.10. Such an error can occur when the physical format is missing or destroyed. Also the error can occur when there is a malfunction in the reading channel - no reading, or due to a malfunction of the data conversion circuitry, or due to incorrect operation of the MCC circuitry in the single-chip microcontroller.

AMNF - the address marker of the data field is not found after the identification field has been found correctly. This error occurs mainly with a partially destroyed physical format. The read/write data channel appears to be working, as the address marker of the identity field is found and the MCC of the identity field matches.

UNC - data not corrected. When executing the sector read command, the identification field is read correctly, the address marker of the data field is found, but when reading the data field the MCC did not match and the error correction equipment was unable to correct this error. Such errors occur mainly due to defects of magnetic surfaces.

CORR - bit 2 of the status register - data corrected. When executing the sector read command, the identification field is read correctly, the address marker of the data field is found, but when reading the data field the MCC did not match and the error correction equipment successfully corrected this error. Such errors occur mainly due to defects in magnetic surfaces. Very often rewriting the physical format corrects these errors.

The BBK bit in the error register indicates that the sector being accessed is defective and is marked as BAD. This bit is not an error bit, but rather an informational bit. The WFT bit in the status register indicates that the sector identification field has been successfully found during the SECTOR WRITE operation and the internal circuits of the HDD generated the WRITE ERROR signal when writing data to the data field. Such an error may occur when the write channel is malfunctioning.

2.2. Basic principles of fault finding.

IDE AT HDD faults can be categorized into the following groups:
- fault with initialization;
- faulty spindle motor control circuitry;
- malfunction of the positioning control circuitry;
- malfunction of the data read-conversion channel;
- malfunction of the recording channel, data precompensation circuitry;
- destruction of proprietary information.

2.2.1. Malfunction with nacial initialization.

Initialization faults usually result in complete inoperability of the drive. It is very common for an HDD with this fault to not even start the spindle motor (due to the drive's control microprocessor not granting startup permission) or to start, then stop, then start again, etc., but in all cases the HDD fails to generate the 50H code in the status register (see status register bits). The main reasons why the drive's control microprocessor cannot perform initialization:
- faulty reset circuitry;
- Quartz clock malfunction;
- destruction of the control firmware in the program memory;
- malfunction of the control microprocessor;
- single-chip microcontroller malfunction.

In order to check how the microprocessor handles initialization, it is necessary to have a listing of the control firmware, then it is possible to check in what place and for what reason the HDD is stopped or reset. As a rule, the algorithm of the drive operation is unknown and, moreover, is a know-how of the HDD manufacturer, and the algorithms of different models (even of the same manufacturer) differ greatly. For all these reasons this approach to searching for the initial initialization fault is practically inapplicable. We propose the following methodology for troubleshooting.

It is necessary to check supply voltages on the control microprocessor of the single-chip microcontroller, excitation of the quartz resonator connected to the control microprocessor, or clock pulse arrival if an external generator is used, as well as all drive synchronization circuits. Next, it is necessary to check the HDD reset circuit. To do this, close and open pins 1 and 2 of the drive's interface connector and use an oscilloscope to observe the passage of the "RESET" signal to the control microprocessor and the single-chip microcontroller. As a control micro-processor in IDE AT HDDs, as a rule, 8-bit single-chip microcomputers are used: Zilog Z8, Motorola 68HC11, intel 8051 family, or 16-bit ones: Motorola 68HC16, Intel 80196 family. If the control microprocessor receives clock pulses (or excites the quartz resonator connected to the microprocessor) and the reset circuit works, the microprocessor must work the control program, as evidenced by the pulses on the pins ALE, /RD, /WR, and they must be monitored immediately after the signal "reset", otherwise you may not see the presence of pulses due to the hang-up of the microprocessor. If the quartz resonator connected directly to the microprocessor is not excited or there are no impulses on the ALE pin, the drive's control microprocessor is most likely defective. Do not "bite out" such micro-

When replacing the processor, it is necessary to use a soldering station to disassemble PLCC and QFP chips so that it can be used in case of incorrect diagnostics. When replacing the drive's control microprocessor, pay attention to the firmware code (firmware version) and replace the microprocessor with the same firmware code as it was, unless you know for sure that another firmware version is compatible. If the microprocessor's quartz resonator is excited and there are pulses on the ALE, /RD, /WR pins, then most likely the HDD spindle motor is rotating. In this situation, it is very common for the drive to fail to become ready because it cannot read control programs from the drive due to a malfunction in the hermetic block or the read channel.

This is especially common in drives with solenoid motor. To check the hermetic block it is necessary to use a serviceable board from a similar drive, it is only necessary not to forget about the compatibility of the firmware of the microprocessor and working programs stored on the magnetic disk. If there are pulses on the microprocessor pins ALE, /WR, /RD, and the permission to start the spindle motor is not given, most likely the microprocessor is waiting for some control or readiness signal from the internal circuits of the HDD. Without having a schematic diagram of the HDD and not knowing the algorithm of the drive operation, the internal readiness signals of the HDD can be checked in the following way. It is necessary to put a jumper on pins 1 and 2 of the drive's interface connector (to simulate the /RESET signal) and compare the logic levels at the pins of the control microprocessor and single-chip microcontroller with the logic levels taken from a similar working HDD. Any discrepancies found will help in determining the fault. If the drive proceeds to reading service information, which can be confirmed by the characteristic sound of the positioning system operation, the fault is most likely not related to initialization. It is convenient to monitor the status of the drive on the LEDs of the status register, which is constantly updated even if no commands are sent to the IDE AT HDD. When diagnosing a drive that fails initialization, the parameters are entered from the database. You can use the following command to verify initialization
"RESET" in the controller test mode. This command performs hardware reset of the HDD, initialization and recalibration. When executing the command it is necessary to observe the HDD status register.

2.2.2. *Spindle motor control circuit malfunction*.

The method of fault finding of the spindle motor control circuit is described in [1]. The criteria for starting the spindle motor are: the supply voltage on the control chip, the reference clock frequency, and the start enable signal. If all these conditions are met and the spindle motor does not start, then either the control chip or the spindle motor is defective. Spindle motor operation can be verified by using a serviceable control board. The reference clock frequency and the start enable signal should be monitored immediately after the power is turned ON for 2 to 4 seconds. This is because to prevent the spindle motor windings from burning out, the control chip will shut down if no index pulses are sent to the control microprocessor within a few seconds. The spindle motor may start to gain speed and then stop. This is most often due to the fact that the control microprocessor monitors the rotation speed of the magnetic disks by measuring the index pulse period, and if the rotation speed of the magnetic disks has not reached the nominal value within a certain period of time, the control microprocessor removes the permission to start the spindle motor or prohibits the reference clock frequency. It is rather difficult to find a fault of the spindle motor control circuit in HDDs in which built-in service information is used as feedback instead of hall sensors (Seagate ST3144A, ST3290A, ST3660A, Seagate CP-3xxx, CFA, CFS, Western Dig. Saviar, etc.). In such HDDs, the spindle motor is pre-spun by the control circuitry, up to some nominal speed, so that the magnetic heads take off and can read servo tags, after that the rotation is stabilized (it is especially well seen when powering up the Soppeg drive in the process mode). Therefore, due to destruction of service information, germoblock or servo read channel failure, the spindle motor can start and stop.

2.2.3. Malfunction of the positioning system.

If the positioning system in an IDE AT HDD malfunctions, it can result in random failures (read errors appearing on different cylinders) or complete inoperability of the drive due to the HDD being unable to read service information. The tests to verify the positioning system are: format check and random read. The format check test will verify that the positioning control circuitry is working properly, and the random read test will verify that the positioning mechanics are working properly. In a stepper motor HDD with a conventional phase-controlled stepper motor, a control circuit malfunction is expressed by the cyclic occurrence of an error on cylinder multiples of the stepper motor cycle. For example, in ST157A with stepper motor cycle 20 errors appear on cylinders: 8,9,11,28,29,31,48,49,51, etc. When such a fault occurs, it is necessary in the
"STEP TEST", using the step commands [STEP+] and [STEP-], position on these cylinders and observe with an oscilloscope the analog signal of the read data at the read channel reference point [1]. If the signal on these cylinders is blurred, and on the other cylinders is clear, then most likely the stepper motor control chip is faulty. When diagnosing the fault, it is also necessary to use a check of the static voltages on the stepper motor according to its cycle [1]. In a stepper motor HDD with pulse-width phase control, a control circuit malfunction manifests itself in very slow reading of data from the disk, or to the occurrence of numerous random errors due to the fact that the trim system is not working properly. To check the positioning system for pulse-width phase control of a stepper motor, it is necessary to move the positioner step by step from cylinder to cylinder using the commands [STEP+], [STEP-] in the "STEP TEST" mode. The analog signal to be read at the reference point of the reading channel must be monitored. If the positioning system is in good condition, the stepper motor shaft will rotate evenly, and a clear, non-blurred signal will be observed on the oscilloscope screen. If the reading signal is blurred or very slow to clear when the [STEP+] or [STEP-] command is executed, the positioning system is faulty. In this case it is necessary to make sure that the service information on the magnetic disks is in good working order, check the operability of the reading servo channel and the ADC circuit, the mismatch circuit and the SHIFU generator (see Fig. 2). To check the service information serviceability, it is better to use the control board removed from a similar working drive, thus the whole mechanical part is automatically checked
of the positioning system [1]. To check the read servo channel, it is necessary to check the read data passage to the ADC circuit input with an oscilloscope. The technique of checking the ADC circuit, mismatch circuit and SHIFU generator depends on the specific circuit solution of these functional devices. In solenoid-driven LVMDs, the mechanical part of the positioning system is very reliable due to its simplicity and almost all faults are related to the electronics of the control circuitry. The only fault in the germoblock that is not so rare is the breakage of the solenoid coil. The break usually occurs at the soldering point to the flexible loop and is easy enough to fix. Such a fault can be easily detected with an ohmmeter on the connector without opening the hermetic block. The resistance of the solenoid is about 30 ohms. As for the repair of the control circuit, we can advise the method of replacing the servo controller chip with a known serviceable one, removed from another drive. For this purpose it is better to use a soldering station for PLCC and QFP packages, or you can adapt a technological hair dryer for soldering linoleum with a hot air temperature of 200 - 300 ° C .

2.2.4. Data reading/preprocessing channel malfunction.

A malfunction in the read/data conversion channel of an IDE AT HDD can result in random read errors, no reads, or complete inoperability of the drive due to the HDD being unable to read service information from the disk. As a rule, these are IDNF errors, and the occurrence of AMNF, UNC, SORR errors or the occurrence of at least one track without errors indicates that the data conversion channel is most likely intact and the error should be looked for in the read channel, "broken" surfaces or a partially destroyed lower level format. To test the read/data conversion channel, the "FORMAT TEST" test should be performed. If the number of errors exceeds 50 when executing the test, the test can be aborted. In the listing of the test results, each error must be identified according to its code. It is also necessary to remember that most IDE AT

physical organization of the disk space does not correspond to the logical one due to the translation mode. Therefore, the occurrence of errors on all surfaces after a certain number of cylinders is possible due to the lack of reading on one particular physical surface. Fault finding in the reading channel is performed in the "TEST STORAGE" mode. In this mode, when switching the [GOAL] heads, the tester applies the 41H - Verify command to the drive, and the information about appearing errors is displayed on the LEDs of the status register and error register. In this mode the functionality of the switch chip and the data reading processor is checked, the read data passing to the separator chip can be checked using the ST506/ 412 ST506/ 412 drive reading channel test procedure [1]. To check the BMG switch chip and the BMG itself it is necessary to disable the translation mode. To do this, in the "SELECT STORAGE TYPE" menu, in User Type it is necessary to specify the physical parameters of the first zone of the drive under test, and then execute the "NMD Reset" command from the "CONTROLLER TEST" menu. The logical sector and head numbers on the zero logical cylinder will correspond to the physical ones. In case of faults in the read channel it is pointless to execute the write command [WRITE], because before writing data, the IDE AT HDD checks the identification field and, if it is not detected, it will not be written and an IDNF error will be generated. If the reading data is present at the input of the separator chip when switching all heads, then most likely the IDE AT HDD reading channel is correct. The next step is to check the data conversion channel which includes the separator chip and the single-chip microcontroller. The schematic diagram of the separator chip and the single-chip microcontroller is shown in Fig.20.
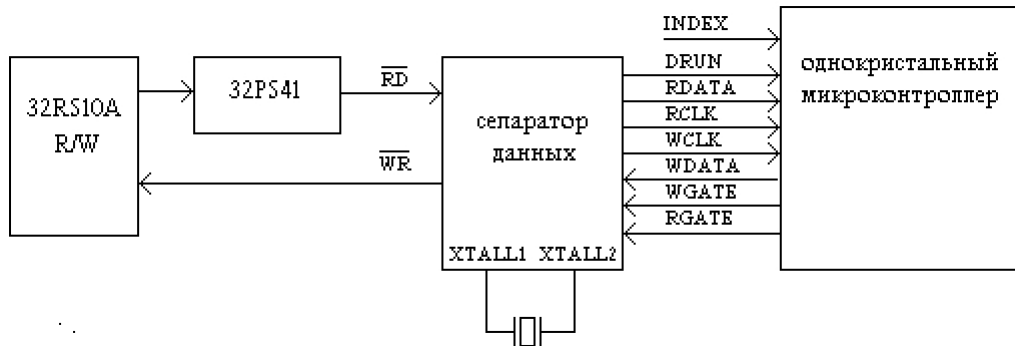

Fig.20. Circuit diagram of the separator and single-chip microcontroller.

A malfunction of the data conversion channel is indicated by an IDNF error on all surfaces and all cylinders. Checking the separator chip starts with measuring the supply voltages and clock frequency of the reference oscillator. As a rule, the reference frequency for the 2.7 RLL code is 15 MHz. Next, it is necessary in the "CONTROLLER TEST" mode to give the command "READ SECTOR IN CYCLE". At the tester's requests it is necessary to specify the number of head, cylinder and sector. It is only necessary to make sure that the lower level format on this track is serviceable (best done with a serviceable control board). If the lower level format is in good working order, the control signal diagram shown in Fig.21 should be observed.
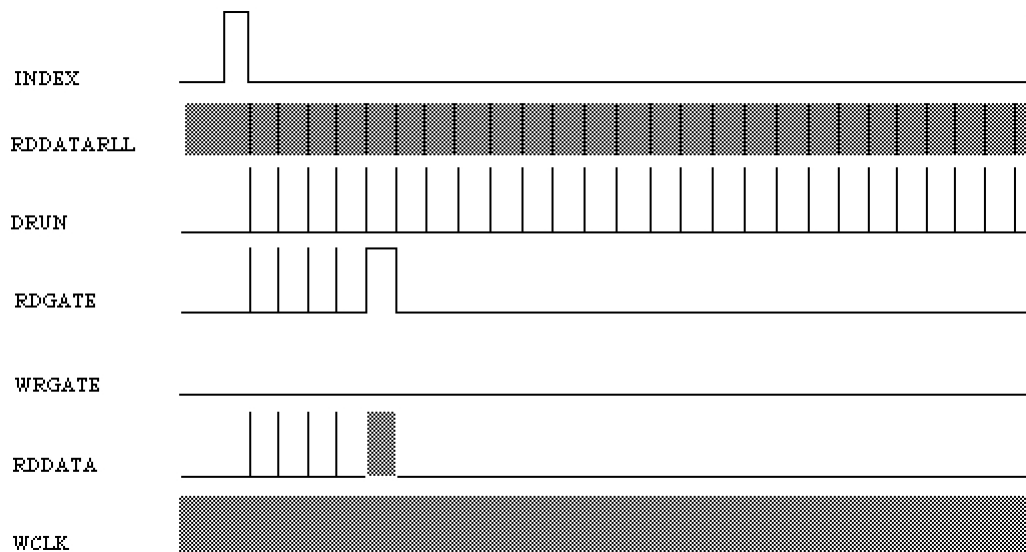
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Figure 21. Reading (5th sector is read).

It should be remembered that this diagram is generalized and only shows the method of checking the separator and single-chip microcontroller. The actual diagram depends on the chips used and the algorithm of the drive (in particular, the algorithm of sector reading) and can be taken from a similar working drive. When checking, you need a two-beam or two-channel oscilloscope, which must be synchronized from the INDEX pulses coming to the single-chip microcontroller. One channel "become" on the incoming index pulses, the other channel checks the incoming control and data signals. The sweep is chosen so that one or half of the period of the index pulses can be placed on the screen.

2.2.5. Faulty Write channel, precompensation circuitry data.

A faulty write channel usually results in an inability to write to an IDE AT HDD, although the drive reads normally. It should be reminded that when writing, the drive reads the track format beforehand, compares the read identification field with the specified one and, if they coincide, only then the data is directly written to the sector, Fig.22.

The main faults in the recording channel are as follows:
- no data to be recorded when a recording strobe is present;
- the recording current is outside the permissible limits;
- supply voltages outside the permissible limits.

In these cases, as a rule, the WRFT bit of the status register is formed. It is possible to check the recording channel in the "RECORDER TEST" mode. While in this mode it is necessary to monitor the read data with an oscilloscope at the reference point of the read channel [1]. Switching the heads with the command [Goal] it is necessary to make sure that the data are read on all surfaces and there is no reading error. After that it is necessary to record the track with any selected code. The signal on the oscilloscope screen should change, if necessary, you can re-record with another code. This operation should be performed for all heads. Please note that the selected recording code is converted in the HDD into one of the numerous recording codes: 1.7RLL, 1.8RLL, 2.7RLL, 2.8RLL, ARLL, etc. used in the given drive model, so the same recording code may have a different appearance on different IDE AT HDD models.
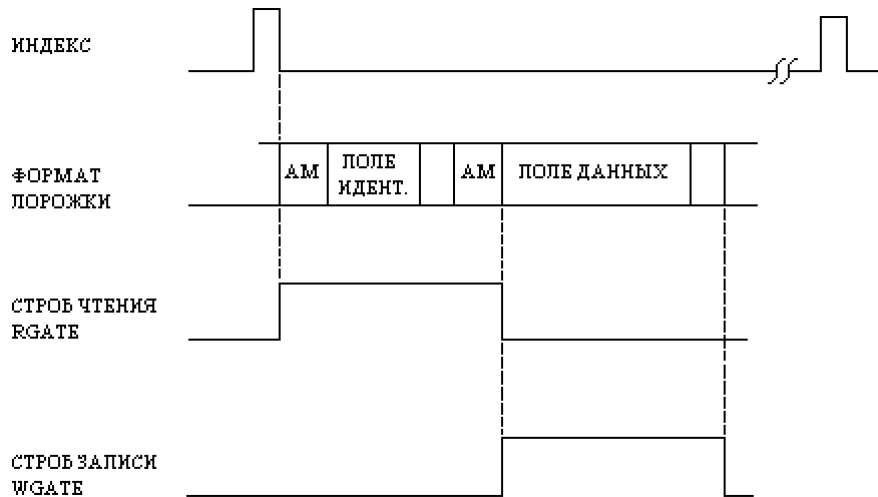
Figure 22. Data recording.

If the data are not recorded, it is necessary to check the control signals generated by the microprocessor and single-chip microcontroller. To do this, in the "CONTROLLER TEST" mode, select the "SECTOR RECORD IN CYCLE" command, enter the number of cylinder, head and sector. The check is performed in the same way as for reading. The generalized diagram of control signals when writing a sector is shown in Fig.23.
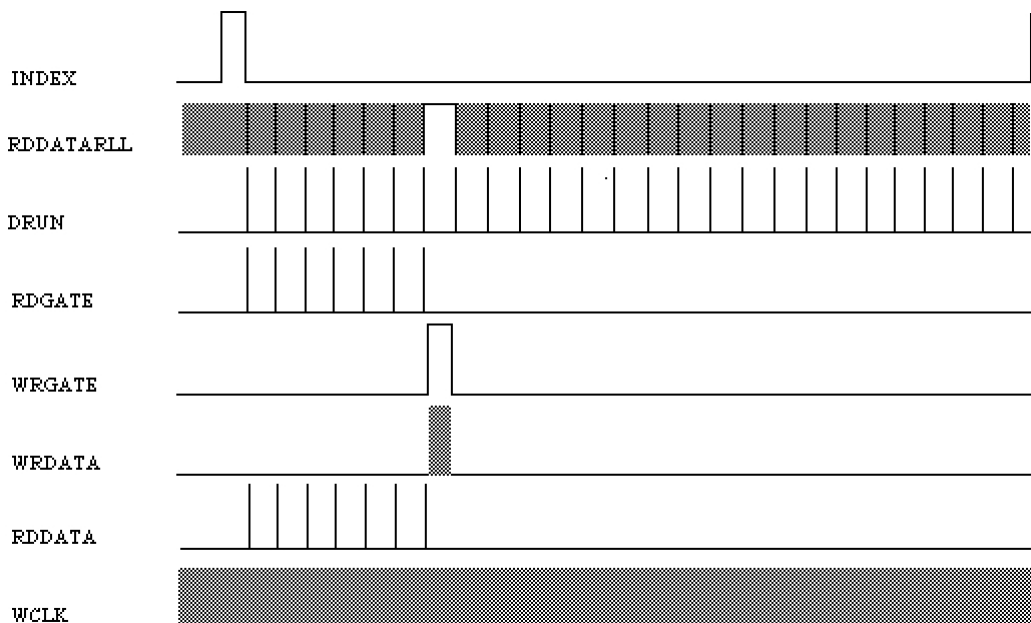

Fig.23. Recording (writing to the seventh sector).

Failure of the precompensation circuitry usually results in multiple read errors appearing on higher cylinders. Keep in mind that precompensation affects the data being written and errors will occur when reading such written data with a faulty read channel [1]. If the IDE AT HDD has read errors on the high cylinders, it is necessary to try to format the hermetic block with the help of a serviceable control board removed from a similar HDD

of a non-functional storage device. If after that the errors on the higher cylinders disappear during reading by the native control board, the precompensation circuitry is most likely defective. In modern IDE AT HDDs, a single-chip microcontroller, which performs coding of the data being written, produces EARLY and LATE (early and late) signals, Fig.15, which are necessary for operation of the precompensation circuitry, Fig.12. Normally, these signals are produced continuously, but permission to precompensate data is given from the control microprocessor from approximately the middle of each zone [1]. It is necessary to check the activation of precompensation when performing the test of erasing surfaces [Erase] in the mode "TEST STORAGE". Note that some IDE AT HDDs have write precompensation enabled from the very zero cylinder.

2.2.6. Disruption of service6 information.

Service information is strictly individual for different models of HDDs (see Section 1.3) and may differ for the same model of HDDs of different series. When service information is lost, almost all IDE AT HDD models become inoperable, although their electronics and mechanics are intact. Moreover, a drive that has lost service information cannot even be diagnosed in normal non-technological operation mode (for example, all Seagate models generate ABRT error). For reliability, the service information is duplicated in several places in the drive's process area.

Destruction of service information and defects generally occur due to the following reasons:
- Improper operating conditions of the drive. Shaking and shock during transportation and operation of the drive;
- incorrect low-level formatting;
- destruction of the magnetic layer of low-quality magnetic disks;
- destruction of the magnetic layer due to the natural aging of magnetic disks;
- failure of HDD recording path and as a consequence service information is overwritten;
- incorrect operation of some HDD models in case of power failures and on theRESET signal.

2.3. Recovery of proprietary information.

The need to restore service information and hide defects arises in most repair jobs.

To restore service information of IDE AT drives it is necessary to have special equipment and software. Thus, recovery of the lower level format, work programs, configuration table, disk passport and hiding of defective sectors (except for the assign mode) is carried out in the technological mode of the drive when it is enabled, the entire disk space of the drive becomes available. Enabling the process mode varies from drive model to drive model and occurs either by command from the interface or by using a special process connector. Some drives enable the process mode by installing a special ROM in the panel to replace the main ROM. After enabling the technological mode of the drive, a special set of commands becomes available to write or restore service information. In addition, in the process mode, many drive models allow for more rigorous diagnostics, for example, during surface testing (Media analysis), the drive narrows its detection window [1] for more rigorous testing of magnetic surfaces. To restore service information and diagnose the drives in the technological mode, the PC-3000 complex includes additional adapters and utilities (see the description of PC-3000 complex utilities). It is practically impossible to overwrite service information of drives with solenoid drive of magnetic heads in the conditions of service companies, as it is recorded at the manufacturing plants directly on magnetic disks in the assembled hermetic block with the help of special precision units - SERVOWRITER. A special technological window in the hermetic block of the drives is used to write service information. As a rule, servowriters write service information only for one drive family. These devices utilize precision mechanics, laser distance meters, etc. Drives with corrupted Embedded type service information can be repaired by excluding or replacing BAD sectors with redundant ones, excluding or replacing BAD tracks, excluding from the operation of the entire defective surface. The listed operations are individual for each family

drives and are performed in its technological operation mode (see the description of PC-3000 complex utilities). Restoration of servo information in drives with pulse-width phase control of the stepper motor is performed either by command in the technological mode as in KL3120 drives by KALOK and DX3120 drives b y Daeyoung or by servo writers as in drives with solenoid drive. For SI recovery of Western Digital WD93044A and Seagate ST351A/X drives, ACE Lab offers its own servo drivers SW-WD9X and SW-ST351.

2.4. Compatibility of IDE AT control boards and germoblocks for HDD IDE AT.

The internal drive firmware stored in the program memory of the control microprocessor closely interacts with the service information stored on the working surfaces of the HDD. The firmware version is indicated by a number on the drive's microprocessor case, and the service information version is indicated by a number on a label glued to the sealing unit, and in case of Seagate and Sopper HDDs this number is duplicated in the disk passport. For the same models of different versions of release should be observed the correspondence of the number of the processor firmware and the version of the operating programs written to the germoblock. Sometimes it happens that two perfectly identical drives of the same model but of different release versions, being perfectly serviceable, become inoperable when the electronics boards are rearranged (e.g. ST3660A by Seagate). In these cases, you have to rewrite the firmware using a special technological utility (see the description of utilities complex PC-3000), and if there is no such opportunity to memorize the corresponding firmware numbers of the microprocessor and germoblock suitable for each other germoblocks and electronics boards. This information will come in handy when repairing several drives of the same model, just by the method of rearranging the boards, or as it is also called brute force. PC-3000AT" tester, when performing a complex test, forms a test report, which contains all information about the drive, you only need to enter the firmware number of the microprocessor, and save the listing. As a rule, germoblocks and control boards of modern "half" models of drives are compatible. The firmware stored in the ROM during initialization is adjusted to the type of the used germoblock (for example, HDD of the Saviar family by Western Digital) or the adjustment is carried out by command in the technological mode of the drive (for example, HDD CFS850A and CFS425A by Conner, etc.).

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