adaptec

AHA-1540A/1542A
User's Manual

Preface

FCC Compliance

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications of Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television equipment reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that computer and receiver are on different branch circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Solve Radio-TV Interference Problems"

This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock No. 004-000-00345-4.

Warning: This equipment has been certified to comply with the limits for Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception. Also this equipment must be used with shielded power cables and shielded I/O cables.

AHA-1540A and AHA-1542A Industry PC/AT-to-SCSI Host Adapter
User's Manual and Specification

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Section One Introduction

1.1 DOCUMENT SCOPE

This manual provides the information required to install and program the AHA-1540A and the AHA-1542A Intelligent Host Adapters in AT bus-based systems.

1.2 PURPOSE

The Adaptec AHA-1540A and AHA-1542A provide a powerful multitasking interface between the Industry Standard Architecture (PC/AT compatible) bus and the Small Computer System Interface (SCSI) bus. The AHA-1540A/1542A are high performance intelligent host adapters supporting a maximum asynchronous SCSI rate of 2.0 MBytes/second and a synchronous transfer rate of 5 MBytes/second. The AHA-1540A/1542A support multithreaded I/O operations, allowing simultaneous operations on multiple targets/LUNs. Disconnect/Reconnect support maximizes bus utilization for multiple target systems. Target mode operation allow the AHA-1540A and AHA-1542A to receive information from other host adapters. Scatter-gather allows high-performance even in systems with fragmented memory buffers.

The Adaptec AHA-1540A/1542A provides a solution for system applications requiring very high performance, configuration flexibility and multithreaded I/O capability, and system redundancy. The Adaptec BIOS also allows the AHA-1540A/1542A to be used in place of a standard hard disk controller. The AHA-1540A host adapter provides only the high performance host adapter circuitry. The AHA-1542A host adapter provides identical host adapter circuitry, but adds an IBM compatible flexible diskette controller to the circuit board.

1.3 AHA-1540A/1542A PRODUCT FEATURES

- High performance Bus Master DMA with selectable or programmable data rates of up to 10 MBytes/second.
- 16- and 8-bit transfers
- Odd and Even starting address transfers and odd or even data lengths
- Maximum synchronous SCSI transfer rate of up to 5.0 MBytes/second
- Asynchronous and synchronous peripherals supported simultaneously
- Programmable AT bus burst transfer on and off time
- Jumper selectable DMA channel for bus arbitration (channels 0,5,6,7)
- Jumper selectable interrupt channels (IRQ 9, 10, 11, 12, 14, 15)
- True multithreaded operation supporting up to 255 tasks simultaneously
- Programmable mailbox architecture
- Adaptec BIOS for standard hard disk emulation
- Jumper selectable I/O port address
- Internal and external SCSI connectors
- Initiator and Target modes of operation fully supported
- On-board flexible diskette controller (AHA-1542A only)
- Scatter-gather

1.4 PRODUCT SPECIFICATIONS

- Physical Dimensions:

  Length : 13.25 " Width : 4.125" Height : 0.5"

  Standard PC/AT™ compatible form factor

- Power Requirements:

  +5.0 +/- 0.25 Volts at 2.1 Amps maximum.

- Environmental Requirements:

  Temperature 0-60 degrees C (operating or storage)

- Reliability Information

  Mean Time Between Failures: 15000 hours
  (calculated per Mil Handbook 217E, ground benign, 40 °C)

  Mean Time Between Failures: TBD hours
  (experimental)

  Mean Time to Repair: 30 minutes

- Industry Standard Architecture Interface

  Standard PC/AT bus electronic and physical interface.

  Driver output:

V_{OL}:	min:	0 volts	max.	0.4 volts	I_{OL}:	24 ma.
V_{OH}:	min:	2.4 volts	max.	5.25 volts	I_{OH}:	8 ma.

  Receiver Input

  V_{IL}: 0.8 volts
  V_{IH}: 2.0 volts

  Connector configuration as specified by IBM PC/AT Technical Reference Manual or manual of Industry Standard Architecture host computer.

- SCSI Interface:

Electrical Interface:

As specified by ANSI X3.131-1986 for single-ended operation.

Minimum driver output: 48 milliamps, sinking @ 0.5 volts

Signal true:	min:	0 volts	max:	0.8 volts
Signal false:	min:	2.0 volts	max:	5.25 volts
Input hysteresis:	min:	0.2 volts		
Terminator Power voltage:	min:	4.25 volts	max:	5.25 volts
Terminator Power current:	min:	800 ma.	max:	1.5 amp (fused)

Internal connector:

Unshrouded 50-pin header, compatible with unshielded alternative 1 connector as specified in ANSI X3.131-1986 Figure 4-1

For connector pin out, see Appendix B.

Partial list of compatible connector plugs (for reference only):

Manufacturer	Model	Part Number
3-M	N.A.	3425-6000
T&B Ansley	N.A.	609-5000M
Molex	N.A.	15-29-8505

Cable for internal SCSI connector should be good quality 50 conductor flat cable with 26 or 28 gauge conductors and a characteristic impedance (Z_0) of 100 ± 10 Ω. Cable shielding is necessary if extremely noisy circuitry or extremely noise sensitive circuitry is present inside the host computer frame.

External connector:

Shielded 50-pin connector as specified in ANSI X3.131-1986, Figure D-4.

For connector pin out, see Appendix B.

Partial list of compatible connector plugs or cable assemblies (for reference only):

Manufacturer	Model	Part Number
Amphenol	N.A. (Mates with 57-BC50B-AM200)	200-1M115-02003
AMP	Champ	
	Plug	554953-1
	Cover	554946 - x(1-2)
	Ferrule	554725 - x(1-6)

Cable for external SCSI connector should be good quality 100% shielded round cable with 25 twisted pairs. Each pair should have a characteristic impedance (Z_0) between 90 and 135 Ω. Wire gauge may be 26 or 28 AWG. All pairs should have the same impedance and should have the same delay per length of cable. Cables meeting these requirements will normally operate correctly in any SCSI configuration and should normally meet all FCC requirements.

- Floppy Disk Interface

  Standard Floppy Disk electronic and physical interface:

  - Driver output:

V_{OL}:	min: 0 volts	max.	0.5 volts	I_{OL}:	60 ma.
V_{OH}:	open collector	max.	5.25 volts	I_{OH}:	.1 ma.

    Receiver Input

    Tied to +5 volt supply through 150 Ω resistors.
    Schmidt Trigger with 0.8 volts hysteresis
    V_{T-}: max 1.0 volts
    V_{T+}: min 1.4 volts

  Connector:

  Unshrouded 34-pin header.

  For connector pin out, see Section 9.1

  Partial list of compatible connector plugs (for reference only):

Manufacturer	Model	Part Number
3-M	N.A.	3414-6000
T&B Ansley	N.A.	609-3400M

  Cable for floppy connector should be good quality 34 conductor flat cable with 28 gauge conductors. Addressing of the second drive may be generated by twisting connector signals 10 through 16 or by changing jumpers in the floppy disk drives.

- Meets radiation limits specified for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules. See FCC Compliance notes and recommendations in preface of this document.

1.5 REFERENCE DOCUMENTS

- IBM PC/AT Technical Reference Manual
- Small Computer System Interface, ANSI X3.131-1986, American National Standards Institute
- Adaptec AHA-1540A/AHA-1542A Host Adapter Installation Guide

Section Two Host Adapter Architecture

2.1 HARDWARE

2.1.1 Bus Master DMA

The AHA-1540A/1542A controls the host AT bus as a master and transfers data directly to and from main system memory. This implementation is known as Bus Master DMA. Bus Master DMA greatly reduces the host software overhead because the host CPU is no longer required to maintain the DMA channel's address pointers and word counts. Bus Master DMA also reduces the number of interrupts generated per I/O command. The Adaptec AIC-560L is the DMA controller.

Adaptec's implementation of Bus Master DMA can achieve a 10 MB/second burst data rate. This speed is especially valuable in multitasking systems where the tasks execute on a time shared basis. Appendix A shows a diagram of the timing required to achieve the DMA rates that are supported by the AHA-1540A/1542A.

The AHA-1540A/1542A DMA hardware will handle both odd-byte and odd-memory address data transfers with no performance degradation.

2.1.2 SCSI Protocol Chip (AIC-6250)

The AHA-1540A/1542A utilizes the AIC-6250 SCSI protocol chip to maximize the SCSI bus utilization. The AIC-6250 is an Adaptec VLSI device which allows the AHA-1540A/1542A to achieve greater than 2.0 MBytes/Sec asynchronous SCSI data transfer rates, and up to 5.0 MBytes/second synchronous transfer rates. The AIC-6250 will also enable the AHA-1540A/1542A to operate as both an initiator and as a target device.

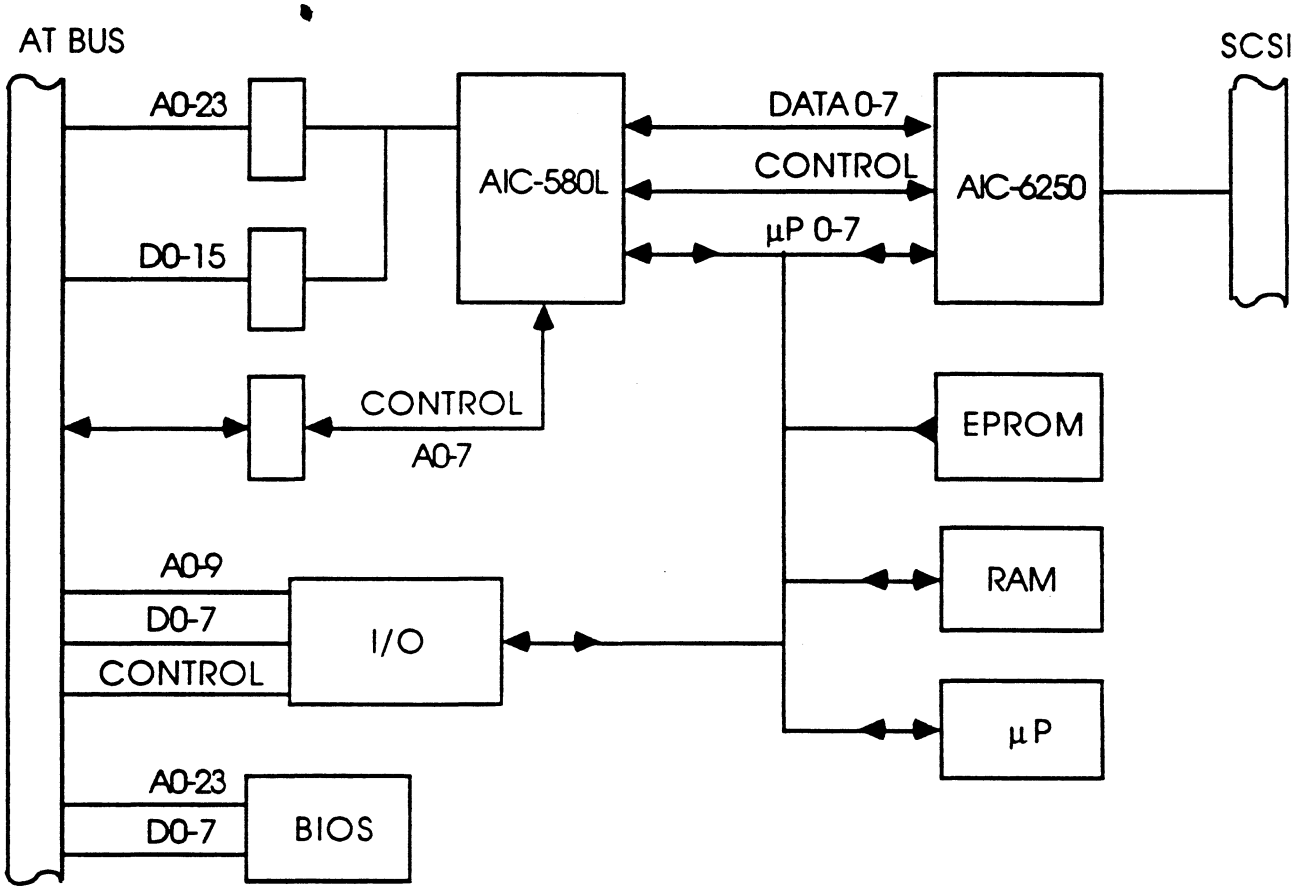
Through a 16-bit host interface, the AIC-6250 reduces bus busy time during data transfer by bursting data across the AT bus at up to 10 MBytes/second. The AIC-6250 has separate data busses for the local microprocessor and for the system data bus. This further increases the performance of the AHA-1540A/1542A by reducing the overhead associated with SCSI commands.

2.1.3 8 Bit Memory

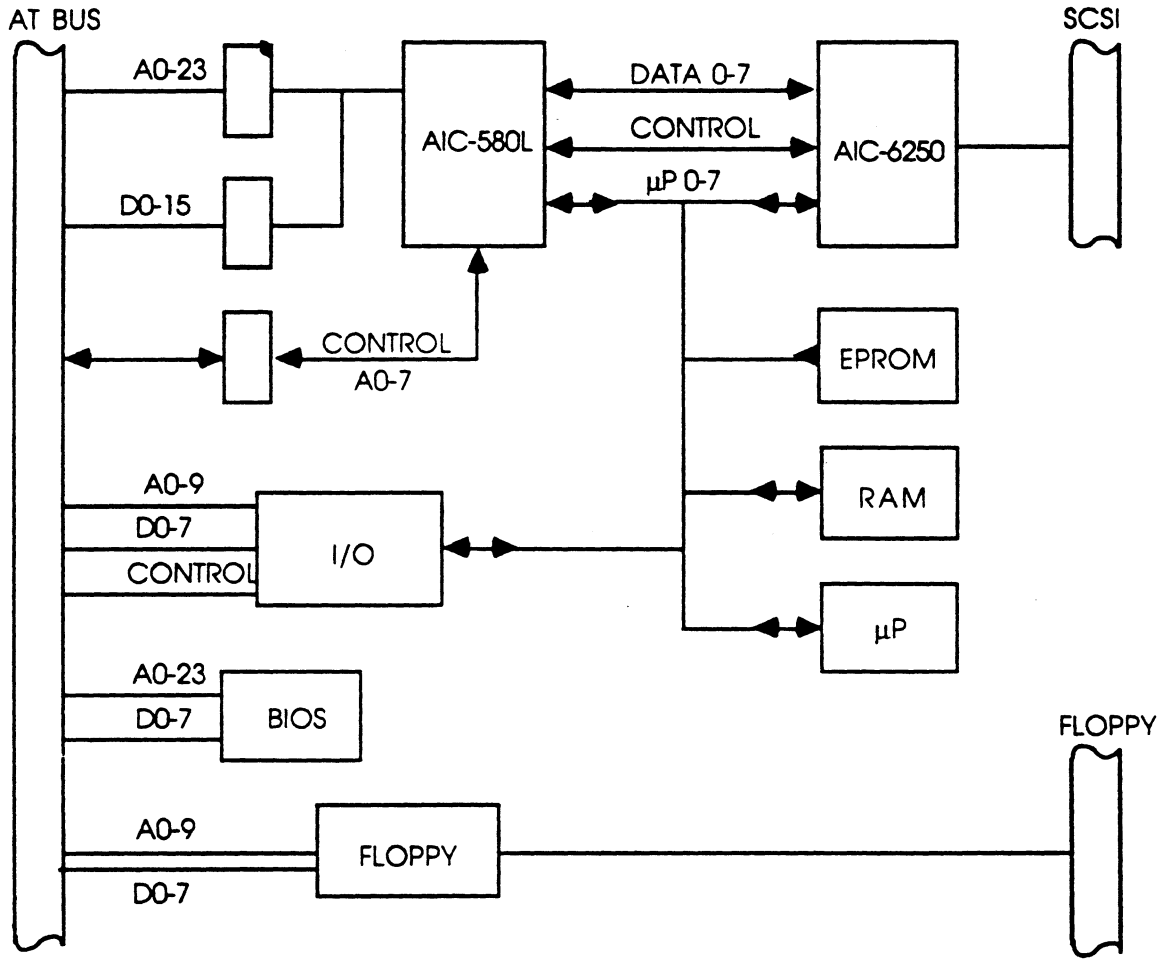
During normal DMA operations, nearly all transfers to and from memory are 16 bit transfers. At the very end, or the very beginning of an odd address boundary, an 8 bit transfer on the upper data bits (D8-D15) will occur according to the AT bus architecture. Some memory in the I/O space, such as video RAM, is 8 bits only and always transfers data only on the lower data bits (D0-D7). The AHA-1540A/1542A will transfer 16 bit or 8 bit memory in the address space between 0A0000 hex and 0BFFFF hex depending on the signal line MEM16 on the AT bus. If this signal is active, 16 bit memory is assumed, and if inactive 8 bit memory is assumed. Outside of this address space 16 bit memory is always assumed.

2.1.4 Hardware Block Diagram

BLOCK DIAGRAM OF AHA-1540A



BLOCK DIAGRAM OF AHA-1542A



2.2 FIRMWARE

The AHA-1540A/1542A supports multithreaded SCSI initiator operation through a simple mailbox protocol. The firmware accepts as many Command Control Blocks (CCB's) as required and executes them from its local RAM. The firmware controls all of the SCSI activity that a task may require. This includes: Arbitration, Selection, Disconnection, Reconnection, and Command completion.

Using the same mailbox protocol, the AHA-1540A/1542A can operate as a Processor type device serving as a multitasking target to other initiators. This feature allows high bandwidth communication between multiple hosts.

In addition, the AHA-1540A/1542A firmware cooperates with the BIOS installed on the host adapter to emulate the standard DOS BIOS calls. This allows booting operations and the execution of standard DOS operations from attached SCSI disks, allowing the SCSI subsystem to completely replace the usual internal disk functions.

2.2.1 Multithreaded Operation

A multiuser, multitasking operating system issues a large number of I/O tasks in a rapid sequence. The architecture of the AHA-1540A/1542A makes management of this activity very easy and straightforward for the operating system and its associated I/O drivers. This section briefly explains the interaction between the system and the AHA-1540A/1542A required to accomplish an I/O task.

2.2.1.1 Mailboxes

The AHA-1540A/1542A uses a mailbox architecture for task communication between the host and host adapter. This allows the host adapter to perform multithreaded operations with a minimum of host intervention.The mailboxes are located in main system memory . Each mailbox entry is four bytes long. After power up sequencing, host initialization procedures, and the boot procedure are completed, the host issues an initialization command to inform the host adapter of the mailbox location. There are always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). MBIs are located immediately after the MBOs. A typical mailbox structure is shown below:

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example there are four MBOs and four MBIs. The first byte of each MBO contains the MBO Command byte. The remaining three bytes point to a Command Control Block (CCB). The CCB provides all the rest of the information needed to complete a task. A MBO is available to accept a new entry if the first byte is zero.

The first byte of each MBI contains the status of a completed task. The remaining three bytes point to the CCB of the completed task. An MBI is free if the Status byte is zero. Mailboxes may point to CCB's controlling initiator tasks, controlling target tasks, or controlling error recovery tasks.

2.2.1.2 Command Control Block

A Command Control Block provides the information required to control a SCSI command sequence. The block contains pointers to the data area to be used by the command. It contains areas for presenting status of both the host adapter and the addressed SCSI device. In addition, it contains the SCSI Command Descriptor Block defining the action to be taken by the addressed SCSI device. An error information buffer area is also provided.

A Command Control Block is also used to service an operation requested by another initiator when the AHA-1540A/1542A is being addressed as a SCSI Processor device.

The CCB is defined completely in Section 5.

A typical CCB is shown below:

Byte					
0	Command Control Block Opcode				
+1	Tar/Init	Data Out	Data In	LUN	
+2	SCSI Command Length = m				
+3	Returned Sense Info Length = n				
+4	Data Length (MSB,MID,LSB)				
+7	Data Pointer (MSB,MID,LSB)				
+10	Link Pointer (MSB,MID,LSB)				
+13	Command Link ID				
+14	Host Status				
+15	Target Status				
+16	Reserved				
+17	Reserved				
+18	SCSI Command Bytes (m Bytes)				
18+m	Allocated for Sense Data (n Bytes)				

2.2.1.3 Command Descriptor Block

The Command Descriptor Block (CDB), a part of the Command Control Block, is a standard format command packet that is transmitted to the addressed SCSI device. It contains all the command information required by the SCSI device to perform the desired operation. The Command Descriptor Block contains the command Operation Code followed by a Logical Unit Number (LUN), command parameters if required, and a control byte. A typical Group 0 six byte CDB is shown below:

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	LUN			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	Vendor Unique		Reserved				Flag	Link

Please refer to the SCSI specification ANSI X3.131, the Common Command Set (CCS) revision 4B, and the SCSI 2 draft for additional information on Command Descriptor Blocks.

2.2.1.4 Principles of Operation

At power-up, the host must inform the host adapter of the location and number of mailboxes. To start a task, the host builds a CCB and stores its memory address into a free mailbox. A non-zero Mailbox Out command byte is then written to indicate that the mailbox entry is full and valid. The host then writes to an I/O port (defined in section 4) to indicate that the host adapter should scan the MBO area. When a full MBO is found, the host adapter copies the mailbox's CCB pointer into its internal RAM and clears the Mailbox entry by writing a zero to the MBO command byte. This frees the MBO so that it can be used to start another task.

After completing a task, the host adapter scans the MBI area for a free mailbox. When one is found, it is updated with the task's completion status and CCB pointer. The CCB pointer identifies the completed task. A MBI Stored interrupt is generated to notify the host that a task has been completed. The host scans the MBI area searching for a non-zero Status byte. When one is located, the host obtains the CCB pointer and frees the MBI by writing a zero into the Status byte. The host then examines the contents of the CCB to determine that the command was successfully completed. The freed MBI can now be used to indicate the completion of another task. The host adapter fills the MBI area and scans the MBO area in a round robin fashion. If the host saves the position of the last active MBI entry, it can determine the MBI of a new entry immediately without searching, since a new entry will be in the next MBI location.

The host adapter transmits a new MBO Available or MBI Full interrupt to the host whenever all non-Mailbox interrupts have been cleared and serviced by the host. The host should analyze the interrupts and clear them as soon as possible so that the host adapter can post any new interrupts quickly. The host adapter will not wait until an interrupt can be transmitted to the host before processing an MBO entry or creating a new MBI entry. Thus, in processing a single MBI

interrupt, the host may find several MBI entries waiting by the time the interrupt processing is finished. Similarly, a later MBI interrupt for the last of the later MBI entries may find nothing to service because the MBI entry was examined and processed as a result of the first MBI Full interrupt. If the interrupts are reset quickly by the host, the probability of an interrupt occurring when no MBI entry is available is much lower, providing an important performance improvement. If the MBI entries are emptied by the host in a round-robin order, the scan for the next full entry is very simple, since it is always the next MBI entry in the Mailbox area.

2.2.1.5 Task Queueing

Multiple tasks may be started against a target/LUN or against multiple targets/Logical Units. Since only one task can be active against any one given LUN at a time, all other tasks for the same LUN are queued. Other LUN's may have active tasks at the same time.

The host adapter dequeues on a first in, first out (FIFO) basis for each target/LUN combination. However, due to the optimization algorithm used by the host adapter, a task may sometimes be started earlier in spite of it's late entrance in the queue on multiple target/LUN systems. Task queueing should not be used where changes in the order of command execution may cause data integrity failures.

2.2.2 Single-Threaded Operation

A host adapter BIOS is provided to emulate the standard hard disk BIOS and boot functions. With this BIOS, the host adapter can be used in lieu of a standard hard disk controller on any ISA compatible system.

The BIOS is compatible with the standard hard disk BIOS. This allows DOS to access up to two hard disk devices on the SCSI bus without a driver. All normal I/O functions are supported including system booting. Single threaded operation and multithreaded operation do not operate simultaneously. Single threaded operation cannot be requested until all multithreaded operations are completed. Similarly, all multithreaded operations must be complete before a single threaded operation can be requested. For most multitasking operating systems, such as Xenix and OS/2, single threaded operation is normally used only for the early part of the boot operation, after which multithreaded drivers take over all control of the SCSI operations.

Section Three Installation

3.1 UNPACKING AND INSPECTION

The carrier is responsible for damage incurred during shipment. In case of damage, have the carrier note the damage on both the delivery receipt and the freight bill, then notify your freight company representative so that the necessary insurance claims can be initiated.

After opening the shipping container, use the packing slip to verify receipt of the individual items listed on the slip. Retain the shipping container and packing material for possible later reuse should return of the equipment to the factory necessary.

CAUTION: THE AHA-154XA IS CAREFULLY DESIGNED TO RESIST THE EFFECTS OF STATIC ELECTRICITY. HOWEVER, LIKE ALL ELECTRONIC EQUIPMENT , IT CAN BE DAMAGED OR ITS LIFE CAN BE SHORTENED BY UNUSUAL STATIC DISCHARGES. PLEASE TAKE THE PROPER PRECAUTIONS WHEN HANDLING THE BOARD. KEEP THE BOARD IN ITS CONDUCTIVE WRAPPING UNTIL IT IS READY TO BE INSTALLED IN YOUR SYSTEM. BE SURE THAT THE HOST COMPUTER AND THE PERSONNEL HANDLING THE BOARD ARE PROPERLY GROUNDED WHILE INSTALLING THE BOARD.

3.2 INSTALLATION

The following section details the installation procedure for the Adaptec AHA-1540A/1542A AT to SCSI host adapter. The installation of the board consists of setting the various on-board jumpers, preparing the SCSI devices, installing the correct terminations, inserting the board into a full-length AT compatible connector, and connecting a SCSI cable from the on-board connector to a SCSI target.

NOTE: The system must be turned off during the installation procedure.

3.2.1 System Configuration

The DOS operating system and the standard AT BIOS support two hard disk drives, drive C: and drive D:. If two standard hard disk drives are installed, they are the only hard disk drives accessible from the operating system. If one standard hard disk drive is installed, the AHA-154XA BIOS allows DOS to access the SCSI drive with the Target:LUN address of 0:0 as the second of the two supported drives (drive D:). If no standard hard disk drives are installed, the AHA-154XA BIOS allows DOS to access the SCSI drive with the address of 0:0 as the first of two supported drives (drive C:) and the SCSI drive with the address of 0:1 or 1:0 as the second of the drives (drive D:). System booting is performed from the floppy drive if a floppy diskette is installed. If no floppy is installed, system booting is attempted from the drive chosen as drive C: through the above process, whether the drive is a standard hard disk or a SCSI hard disk. The AHA-154XA BIOS fully supports the extended partitioning capabilities of DOS 3.3 for up to two drives. The AHA-154XA BIOS only supports the AHA-154XA if its I/O Port Address is set to 330h.

Adaptec provides a special DOS driver for the AHA-154XA that allows the support of up to 24 physical or logical devices under DOS. Many other operating systems, including SCO Xenix and Unix, do not have this limitation and will allow the access of any number of attached SCSI devices.

The term "standard hard disk" refers to the disks attached to the system by a standard ISA disk controller. These standard hard disks can be set to the "Installed" or "Not Installed" state by the SETUP program that is supplied with each ISA host computer. The SETUP program allows the user to select the number of standard hard disks that are recognized by the system regardless of whether or not they are physically installed.

3.2.2 Hardware Setup

Several preparatory steps must be taken to install the host adapter in the host computer. The initialization jumpers must be correctly placed in the AHA154XA. The SCSI Bus terminators must be installed in the correct SCSI devices. Finally, the correct SCSI addresses must be assigned to each peripheral device.

The Adaptec AHA-1540A/1542A 16-Bit AT bus to SCSI bus Host Adapter has been designed to operate as shipped in the majority of AT class computers. The host adapter's jumper settings should almost always remain in their original default positions. Refer to section 3.3 if conflicting memory or port assignments require that the host adapter jumpers be reconfigured. The AHA-1540A/1542A is shipped with the following default settings:

SCSI Address	7
SCSI Parity	Enabled
Terminators	Installed
Terminator Power	Supplying
Synchronous Negotiation	Disabled
DMA Channel	5
Interrupt Channel	11
AT Port Address	330H
AT BIOS Address	ODCOOOH
LA Enable Jumper	Installed

Termination

The SCSI bus must be terminated correctly to assure proper operation. The first and last physical SCSI devices on the SCSI cable must have terminators installed. All other SCSI devices must have terminators removed. The host adapter is shipped with terminators already installed at locations RN3, RN4, and RN5. The internal and external connectors connect to the same SCSI bus, so both internal and external cabling must be considered in determining where terminators are installed.

If only one cable (either internal or external) is connected to the host adapter, the terminators must remain installed in the host adapter. Terminators must also be installed on the device at the farthest end of the cable from the host adapter. Terminators must be removed from all other attached SCSI devices.

If both an internal and an external cable are connected to the host adapter, remove the terminators on the host adapter and install terminators on the devices at the farthest end of each cable. Terminators must be removed from all devices except the device at the end of each cable. The instruction manuals for each SCSI device will indicate how the terminators can be removed or replaced.

Addressing

The SCSI target address for each SCSI device to be attached must be selected by setting the proper jumpers or switches on the device. If the SCSI device is a hard disk that is to be used as the boot disk, it must have the Target Identifier (SCSI Address) set to zero and the Logical Unit Number set to zero. SCSI Addresses 0 and 1 should be reserved for SCSI hard disk drives. SCSI Address 2 is often used for tape devices. Each installed peripheral must have a different Target Identifier. The host adapter's default address is 7. Duplicate SCSI Addresses will cause errors that are extremely difficult to identify. Any jumpers that control operating modes must also be properly set. If there is a jumper that enables synchronous transfer negotiation, the jumper should be set to enable negotiation. Check the SCSI drive or controller to ensure that Parity Checking is enabled. If Parity checking on the device is disabled or not supported, the jumper at location J8 of the host adapter should be removed. Parity checking should only be enabled if all SCSI devices support it.

Installation Procedure

Now that the host adapter and the devices to be installed have been properly prepared, the devices should be installed in the following manner:

1) **Turn OFF the power to the computer system.**

2) Remove the system cover according to the directions of the computer manufacturer.

3) If only an external SCSI subsystem is to be used, no internal cabling is required. If an internal SCSI peripheral is to be used, install a 50 pin SCSI ribbon cable to the host adapter. This cable must be oriented correctly. Pin 1 of the SCSI cable is designated by a red stripe. Multi-color 50 pin ribbon cables signify pin 1 with a brown color. Pin 1 on the host adapter 50 pin SCSI header is located on the left hand side, farthest from the installation bracket and is designated by the words PIN 1 on the board adjacent to the header. After locating pin 1 on the host adapter and on the SCSI cable, carefully insert the connector located at the end of the long end of the cable into the host adapter connector. After ensuring that all pins are lined up and that the pin 1 orientation is correct, firmly seat the connector to the board. If it is ever necessary to remove the cable, gentle prying with a small thin-bladed screwdriver may be required.

4) After installing the SCSI cable, the host adapter can be installed in any one of the adapter slots in the host computer.

5) If an internal SCSI device is to be used, it should be installed in the drive bays in accordance with the directions on the peripheral. The proper power supply must be connected to the SCSI peripheral device.

6) The 50 pin SCSI ribbon cable can now be attached to each SCSI device. Refer to the device's installation instructions to ensure proper pin 1 orientation. Pin 1 orientation must be consistent throughout the system. Keep the ribbon cable neatly dressed away from the ventilation slots in the computer system. Keep the ribbon cable dressed away from possible electrical noise sources or noise sensitive components, particularly large microprocessors, memory boards, switching power supplies, and analog data acquisition boards. If the internal

configuration requires the cable to come near noise sensitive circuits , make sure that the cable crosses the boards at right angles and is near the noise sensitive circuits for the shortest distance possible.

7) Carefully reinstall the cover of the computer.

8) If an external SCSI subsystem is to be installed, it can now be cabled to the External SCSI Connector projecting from the shielding bracket on the back of the AHA-154XA Host Adapter. The proper shielded SCSI cable must be used for proper operation. The external connector on the AHA-1540A/1542A is a D shell connector that ensures correct pin 1 orientation on the host adapter. The subsystem, cables, and SCSI terminators must be installed in accordance with the directions provided with the external SCSI subsystem. The addresses selected for external SCSI devices must not overlap with the addresses of the host adapter or any other SCSI devices attached internally.

3.2.3 Checklist

Before applying power to your system, the following items should be completed and checked:

1. 50 pin SCSI ribbon cable is connected to the host adapter with proper pin 1 orientation.
2. The host adapter is firmly seated in the host computer's adapter slot.
3. The correct SCSI addresses are selected on all attached SCSI devices. Address 0 is reserved for the boot hard disk and address 1 is used for a second hard disk.
4. The correct operating modes are selected on all attached SCSI devices.
5. Terminators are installed or removed on the drives and host adapter as required.
6. External SCSI devices are properly installed and cabled.

3.2.4 Operation Using the BIOS Under DOS

To bring up the system for the first time with the host adapter installed, insert a bootable system diskette in drive A:, and close the door. After the system initialization and power-up diagnostics have completed, system error messages, such as "SYSTEM CONFIGURATION CHANGED, RUN SETUP" and prompts on how to continue, may be displayed. After following the instructions displayed on the screen, the system will boot from the flexible diskette drive.

Run your SETUP program to configure the system as required. **Remember that a SCSI drive can only be used as a boot device if both standard hard disks are mapped out.** When the SETUP parameters have been defined, follow the directions on the screen to re-initialize the system.

Most SCSI drives are shipped from the factory with a complete low-level format. A few SCSI drives and most bridge controllers, including the CCS compatible Adaptec ACB-4525Z, require a low-level SCSI format operation before they will operate. Section 7.4 describes how the low-level format utility that is available in the Adaptec BIOS Utilities should be used to format such SCSI devices.

Run the DOS FDISK program to partition the disk for the number of cylinders to be used by DOS. When using DOS 3.2 or under, it is generally a good idea to select 1 less cylinder than the maximum allowable per partition according to DOS. This eliminates the possibility of exceeding the 32 MB limit. Activate the first DOS partition before leaving the FDISK program if it is to be the boot partition. If you are not sure if a DOS partition exists, use the menu entry in FDISK to display partition data.

After the DOS partition has been created and activated, the drive is ready for a DOS FORMAT. Refer to the DOS manual for the format options that are available. If the system is going to boot from a SCSI disk, it is usually easiest to transfer the hidden system files to that disk during the FORMAT.

CAUTION: IF THE DRIVE YOU ARE USING WAS PREVIOUSLY FORMATTED OR PARTITIONED WITH A DIFFERENT HOST ADAPTER OR DISK CONTROLLER, A DOS PARTITION MAY ALREADY EXIST. IF SUCH A PARTITION DOES EXIST IT SHOULD BE DELETED AND RE-CREATED USING THIS HOST ADAPTER. IF THIS PRECAUTION IS NOT FOLLOWED, ERRATIC SYSTEM OPERATION MAY RESULT.

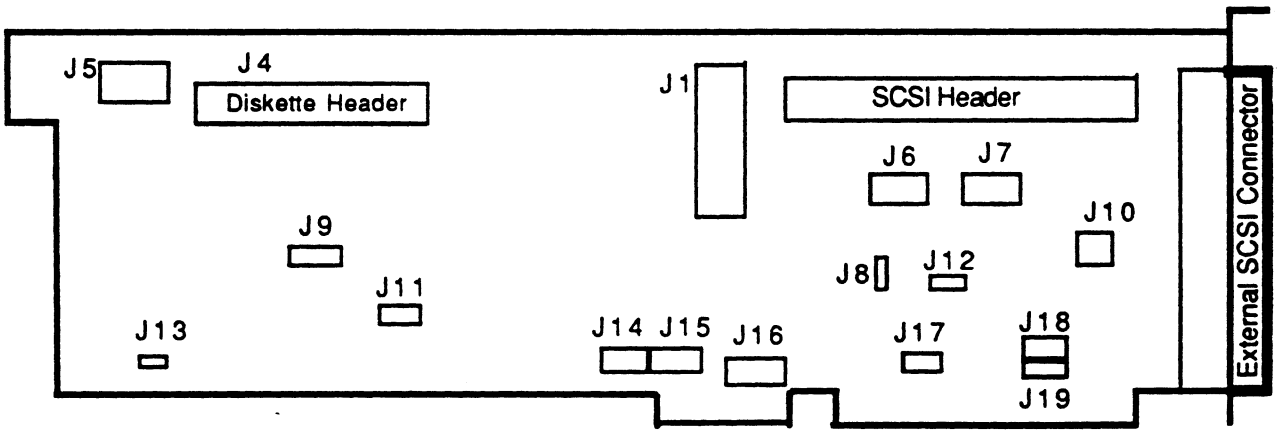
The host adapter and SCSI disks are now ready for normal operation. The host adapter's BIOS performs the necessary initialization procedures during the boot operation. This procedure is described in section 6.1.1

3.3 Jumper Configuration

All of the jumpers have been preset at the factory to ensure proper system operation with the majority of AT bus systems. This information is provided to help the OEM or system integrator to configure the system properly if other option boards present conflicts.

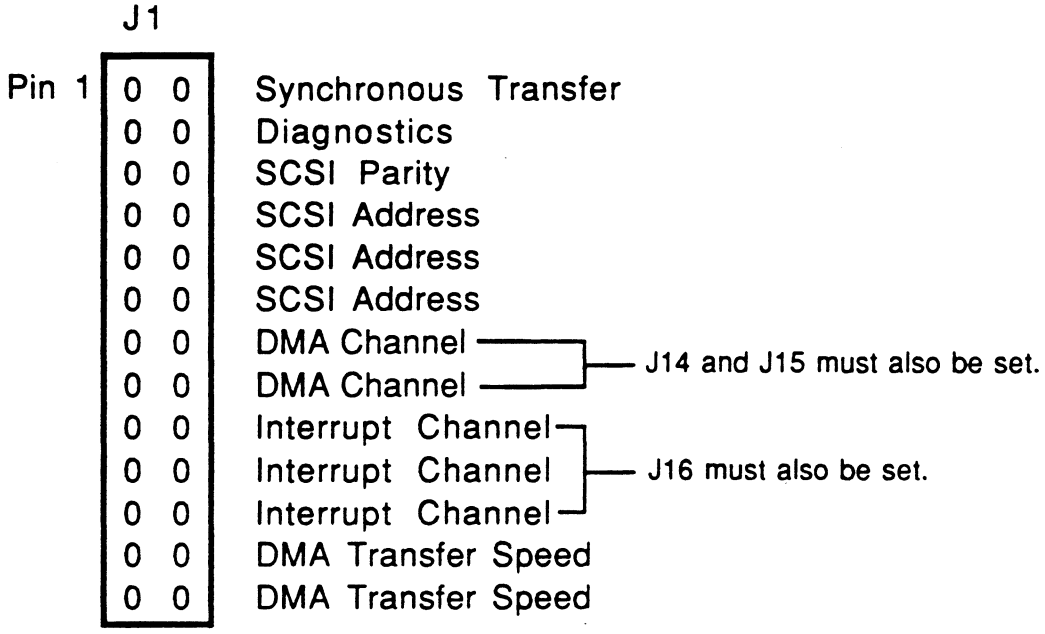
The following diagram shows the approximate location of the various customer configurable items on the AHA-1540A/1542A. Listed after the diagram are the functions, defaults, and set-up options for each jumper.

Jumper locations:



3.3.1 Jumper Block J1

Jumper block J1 is shown below:



Jumper block J1 is the large vertically oriented block of jumpers located near the center of the host adapter. Pin pair 1 is the topmost pair of pins.

3.3.1.1 SCSI Synchronous Negotiation

Pin-pair 1 of jumper block J1 is the synchronous negotiation enable jumper. The AHA-1540A/1542A will initiate SCSI synchronous negotiation during initialization, or after a SCSI reset if this jumper is installed. If the jumper is not installed, the AHA-1540A/1542A will still support synchronous SCSI transfers, but a different SCSI device must initiate the negotiation. **Default is jumper removed, synchronous negotiation initiation disabled.** If any attached SCSI devices support synchronous transfer, the initiation of negotiation should be enabled by both the AHA-154XA and the attached devices to fully implement the SCSI synchronous negotiation protocol.

3.3.1.2 Diagnostic Jumper

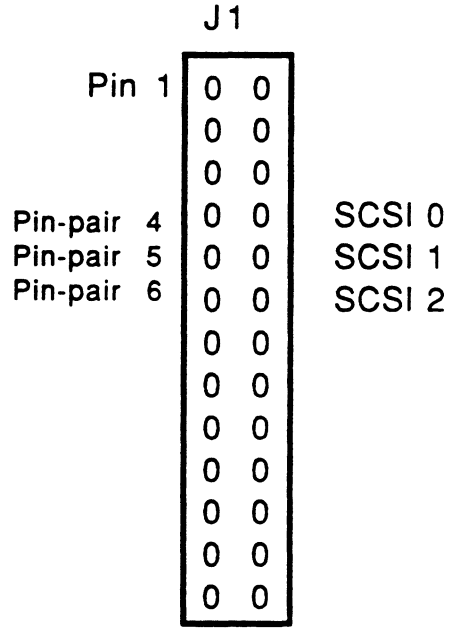
Pin-pair 2 of jumper block J1 is a factory diagnostic jumper. This jumper is reserved for Adaptec use and must not have a jumper shunt installed. If this jumper is installed, the firmware will loop through the power on diagnostics, preventing normal operation. **Default is jumper removed.**

3.3.1.3 SCSI Parity

Pin-pair 3 of jumper block J1 is the parity enable/disable jumper. The SCSI parity checking is disabled if this jumper is installed. **The default is parity checking enabled.**

3.3.2 SCSI Address

Pin-pairs 4, 5, and 6 of jumper block J1 define the SCSI address. The SCSI address is selected according to the following table. **The default address is 7.**



Pin-pair 4 5 6	SCSI Address	
O O O	7	Default
X O O	6	
O X O	5	
X X O	4	
O O X	3	
X O X	2	
O X X	1	
X X X	0	

X = Jumper Installed

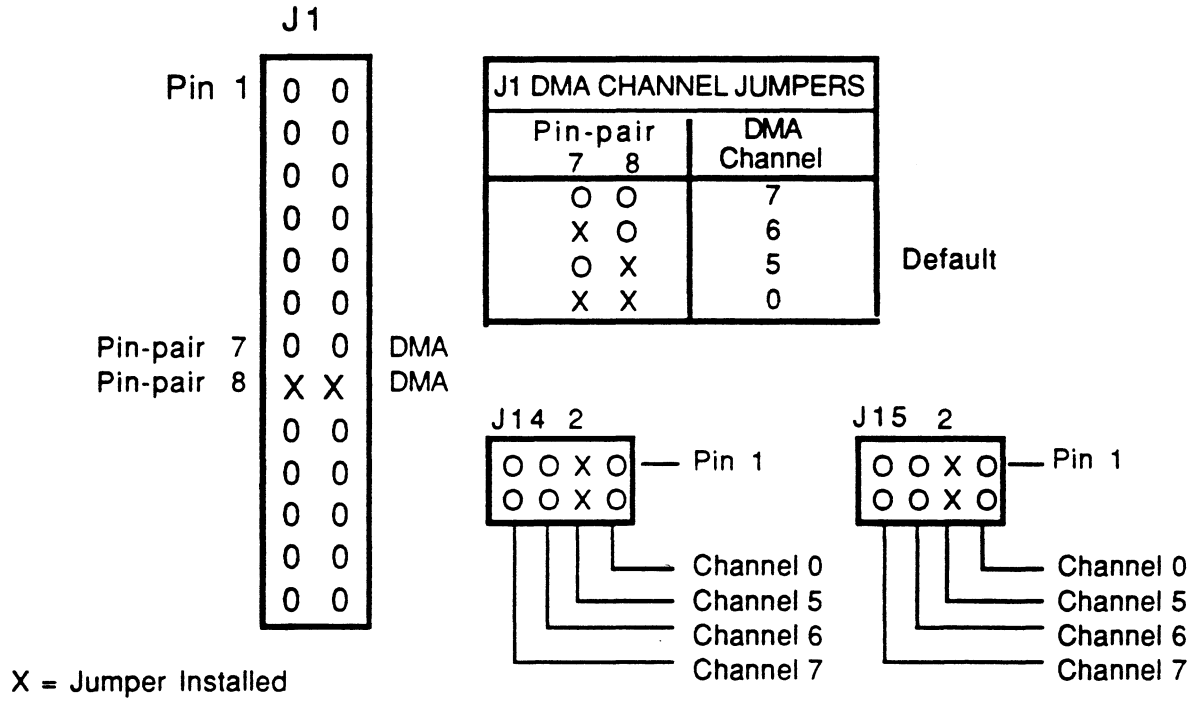
3.3.3 DMA Channel

There are three jumper blocks involved in selecting the DMA channel. These are J1, J14, and J15. The DMA channel selection jumpers consist of pin pairs 7 and 8 located in the large block of jumper pins J1. The DMA channel reported to the AT during the Return Configuration command is set by these jumpers according to the following table. **Default is DMA channel 5.**

Jumper set J14 selects the DMA REQ signal to be used by the AHA-1540A/1542A according to the following table. This jumper set is located near the bottom center of the host adapter. Pin pair 1 is the right most pair of pins.
The default is DMA Request 5.

Jumper set J15 selects the DMA ACK signal to be used by the AHA-1540A/1542A according to the following table. This jumper set is located near the bottom center of the host adapter. Pin pair 1 is the right most set of pins. **The default is DMA Acknowledge 5.**

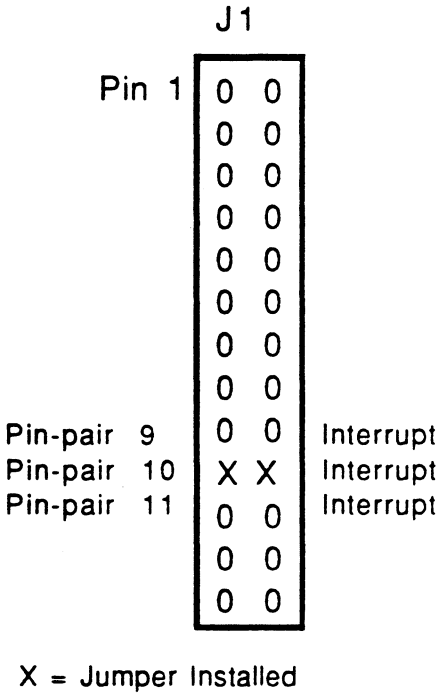
There are four DMA channels that may be chosen for use by the AHA-1540A/AHA-1542A, channels 0, 5, 6, and 7. The DMA channel is set up by using the three jumper blocks and pin-pairs previously described. The jumper settings for each channel are shown below:



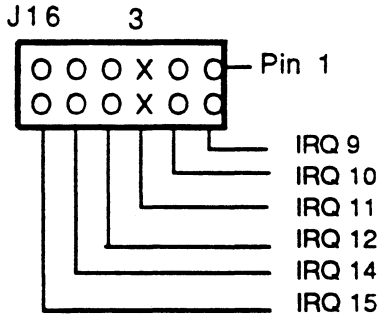
3.3.4 AT Interrupt Channel

There are two jumper blocks involved in selecting the AT interrupt channel. These are J1 and J16. The AT interrupt channel jumpers consist of pin pairs 9, 10, and 11 in the large block of jumper pin pairs J1. The interrupt channel reported to the AT during the Return Configuration Command is set by these jumpers according to the following table. **The default is interrupt channel 11.**

Jumper set J16 selects the AT interrupt channel to be used by the AHA-1540A/1542A. This jumper set is located near the bottom center of the host adapter. Pin pair 1 is the right most pair of pins. The interrupt channel used is set according to the following table. **The default interrupt channel is 11.**

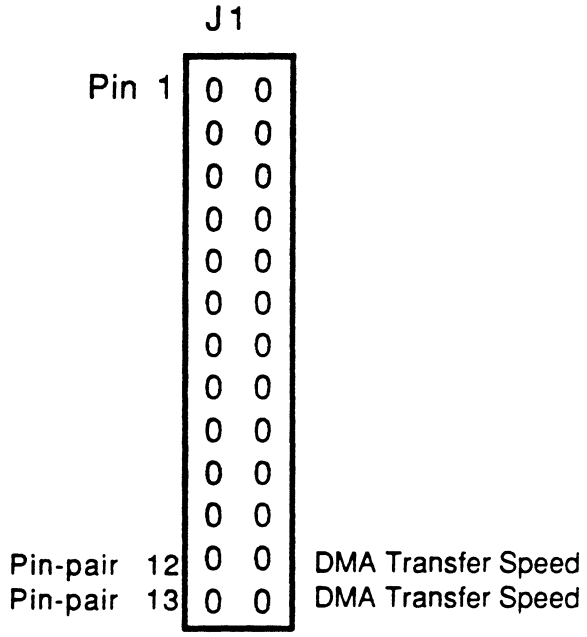


J1 INTERRUPT CHANNELS	
Pin-pair 9 10 11	Interrupt Channel
O O O	9
X O O	10
O X O	11
X X O	12
O O X	14
X O X	15



3.3.5 DMA Transfer Speed Default

Pin-pairs 12 and 13 of jumper block J1 set the default DMA transfer speed. Installing jumper shunts as shown below will set any of 4 default DMA transfer speeds. (See Appendix A for system timing requirements.) The default speed is selected after power on or after a hard reset occurs. This speed may also be tuned to allow for the fastest possible transfer (minimum bus on time) for any particular system by using the Host Adapter command Set Transfer Speed. The Host Adapter Command overrides the jumper settings. This command is detailed in section 5. **The default is no jumper installed.**

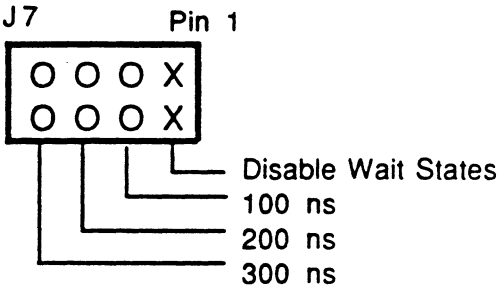


Pin-pair 12 13	DMA Speed	
O O	5.0 MB/s	Default
X O	5.7 MB/s	
O X	6.7 MB/s	
X X	8.0 MB/s	

X = Jumper Installed

3.3.6 AT BIOS Wait State

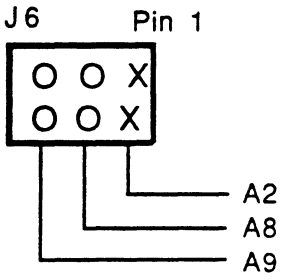
Jumper block J7 allows IOCHRDY on the AT bus to be driven not active during BIOS reads. The time may be set to 100ns, 200ns, 300ns, or the function may be disabled. **The default is Wait State Disabled.**



X = Jumper installed

3.3.7 AT Port Address

The starting address of the block of four I/O ports required by the AHA-1540A/1542A is selected by the jumpers in jumper block J6. Pin pair 1 is the right most pair of pins. The default address is 0330H. That port address is required by the BIOS. Other valid port addresses are 334H, 330H, 234H, 230H, 134H, and 130. These port addresses may be used by device drivers and operating systems that support multiple host adapters. **The default address is 330H.**

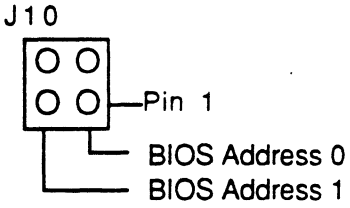


Default is 330H
X Jumper Installed

AT Port Address				
A9	A8	A2	Address	
O	O	O	334H	
O	O	X	330H	Default
O	X	O	234H	
O	X	X	230H	
X	O	O	134H	
X	O	X	130H	

3.3.8 AT BIOS Address

The starting address of the block of address space reserved for the Adaptec BIOS is selected by the jumper pins located in J10. **The default address is ODCOOOH.** This address must not conflict with any other BIOS or decoded address space in the system.

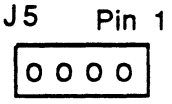


DEFAULT ADDRESS = 0DC000H
X = Jumper Installed

BIOS Address	
Jumpers 0 1	BIOS Address
O O	0DC000H
X O	0CC000H
O X	0D8000H
X X	OC8000H

3.3.9 Front Panel LED Connector

J5 is the front panel LED header. Pins 1 and 4 are connected to the same 220 ohm pull up resistor and pins 2 and 3 are pulled low by the same LED driver whenever the on board LED is on. This allows the Front Panel LED cable to be plugged in with either orientation. The driver is specified to pull 24 milliamps through the LED. J5 is located near the top left of the host adapter.



3.3.10 LA Enable Jumper (AHA-W1542A Only)

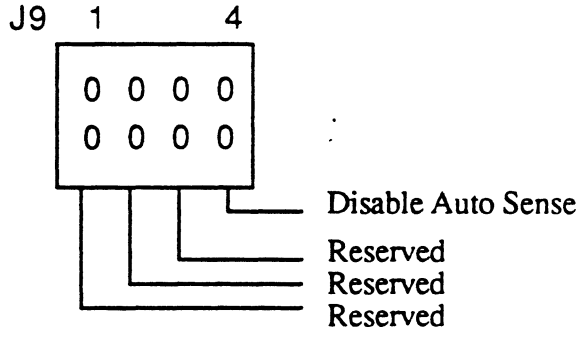
Note: This jumper exists only on the early production units. These are easily identified by a label on the board that has a model number of AHA-W1542A. Standard production AHA-1540A and AHA-1542A boards do not have this jumper.

When J8 is installed, address drivers LA17 - LA19 are enabled. When not installed these address lines are not driven. Some computers, especially 80386 based machines, short address lines LA17 and SA17, LA18 and SA18, and LA19 and SA19 together. If your computer system shorts these lines then remove jumper J8. Default is jumper installed.

CAUTION: INCORRECT INSTALLATION OF THIS JUMPER MAY NOT RESULT IN IMMEDIATE SYSTEM PROBLEMS. IF IT IS NECESSARY TO CHANGE THE STATE OF THIS JUMPER AFTER THE SYSTEM HAS BEEN CONFIGURED, THE SCSI HARD DISK MUST ALSO BE RE-FORMATTED. CONTACT THE COMPUTER SYSTEM MANUFACTURER IF THERE IS ANY DOUBT ON HOW THE SYSTEM IMPLEMENTS THESE ADDRESS LINES.

3.3.11 Auxiliary Jumpers

Installation of a jumper shunt on pin pair 4 of jumper block J9 will disable the automatic request sense function on the AHA-1540A/1542A. If the automatic Request Sense function is enabled, it may additionally be disabled on a command by command basis using the Request Sense Allocation Length Field of the CCB (see Section 5.3). All other pins-pairs on jumper block J9 are reserved for future use.



3.3.12 BIOS Enable/Disable

Only one host adapter BIOS should be enabled in any host system. That BIOS allows DOS to access up to two SCSI drives on the host adapter having a port address of 330H. Any other host adapters installed in the system must have their BIOS disabled. In addition, certain operating systems may require that the BIOS be disabled. The enabling of the BIOS is controlled by jumper J11, near the bottom left of the host adapter. When the jumper is installed on J11 the BIOS is enabled. When the jumper is removed, the BIOS is disabled and will not respond to host reads. **The default is jumper installed.**

3.3.13 SCSI Terminators

RN3, RN4, and RN5 are the SCSI terminators. If the AHA-1540A/1542A is not the first or the last SCSI device in a string of SCSI devices, or if in-line terminators are used, then all of these resistor networks must be removed. More information is provided in section 3.2.2 about the proper use of the SCSI terminators. **The default is terminators installed.**

3.3.14 SCSI Terminator Power

Fuse F1 controls the terminator power. If another SCSI device is supplying terminator power, then F1 may optionally be removed. No more than 5 SCSI devices should be configured to supply terminator power to a single SCSI bus. **The default is F1 installed** with the AHA-1540A/1542A supplying terminator power. The terminator power is protected with a 1.5 amp fuse to prevent short circuits from burning SCSI cables. The terminator power is additionally protected from terminator power back-flow with a low voltage-drop diode so that the SCSI bus will continue to operate even if one or more SCSI host adapters is powered down.

3.4 FLEXIBLE DISKETTE CONTROLLER CONFIGURATION JUMPERS (AHA-1542A ONLY)

3.4.1 Flexible Diskette Controller Secondary Address

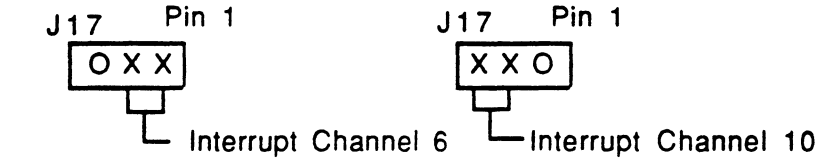
Jumper J12, located near the center right of the host adapter, controls the selection of the flexible diskette controller secondary address. When J12 is installed, the flexible diskette controller will respond to I/O addresses 370-377. When not installed, the flexible diskette controller will respond to I/O addresses 3F0-3F7. **The default is no jumper installed.**

3.4.2 Flexible Diskette Controller Enable

Jumper J13, located near the bottom left of the host adapter, enables or disables the flexible diskette controller. When this jumper is installed, the flexible diskette controller will respond to host reads and writes. When not installed, the flexible diskette controller will not respond to any signal. **The default is jumper installed.**

3.4.3 Flexible Diskette Controller Interrupt Channel

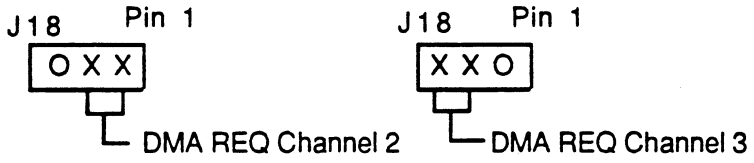
Jumper block J17, located near the bottom right of the host adapter, sets the interrupt channel for the flexible diskette controller. **The default is interrupt channel 6.**



X = Jumper Installed

3.4.4 Flexible Diskette Controller DMA Request Channel

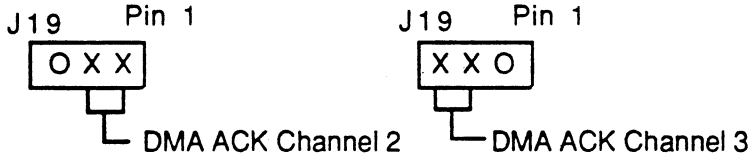
Jumper J18, located near the bottom right of the host adapter, selects the DMA Request channel for the flexible diskette controller. Jumper J19, the DMA Acknowledge jumper, must be set to the same position. **Default is DMA channel 2.**



X = Jumper Installed

3.4.5 Flexible Diskette Controller DMA Acknowledge Channel

Jumper J19, located near the bottom right of the host adapter, selects the DMA acknowledge channel for the flexible diskette controller. Jumper J18, the DMA Request jumper, must be set to the same position. **Default is DMA channel 2.**



X = Jumper Installed

4.0 HARDWARE FUNCTIONAL DESCRIPTION

4.1 HARDWARE OVERVIEW

This section provides a description of the AHA-1540A/1542A hardware functional interface to the PC/AT host software.

The hardware consists of a custom SCSI protocol chip, the AIC-6250, a FIFO buffer, a set of I/O ports, and a controlling microprocessor.

The DMA control logic on the host adapter controls the AT bus arbitration and data transfer hand shaking. During DMA data transfers, the AHA-1540A/1542A becomes a bus master. The DMA logic supports both odd and even starting addresses. For odd starting addresses, the first transfer will be an 8-bit transfer. Thereafter, 16 bit transfers will be used to complete the data transfer. Odd-byte transfers, and the the last transfer of an even number of bytes to an odd address are treated in a similar manner.

The SCSI port is controlled by the AIC-6250, an Adaptec SCSI protocol device which supports arbitration, selection, and reselection with a minimum of processor intervention. This VSLI device also supports target mode and synchronous SCSI transfers.

4.2 I/O PORT INTERFACE

The I/O port interface consists of three address locations. These three port addresses are decoded in the AT I/O address space. They form the primary communications channel between the host and the host adapter. The I/O ports are 8 bits wide. The base port is for control and status, the second port for command and data transfer, and the third port for interrupt flags.

I/O PORT INTERFACE BIT DEFINITION

PORT ADDRESS = BASE + 0

WRITE: Control Register		**READ: Status Register**	
Bit 7	Hard Reset (HRST)	Bit 7	Self Test in Progress (STST)
Bit 6	Soft Reset (SRST)	Bit 6	Internal Diagnostic Failure (DIAGF)
Bit 5	Interrupt Reset (IRST)	Bit 5	Mailbox Initialization Required (INIT)
Bit 4	SCSI Bus Reset (SCRST)	Bit 4	SCSI Host Adapter Idle (IDLE)
Bit 3	Reserved (0)	Bit 3	Command/Data Out Port Full (CDF)
Bit 2	Reserved (0)	Bit 2	Data In Port Full (DF)
Bit 1	Reserved (0)	Bit 1	Reserved (Undefined)
Bit 0	Reserved (0)	Bit 0	Invalid H A Command (INVDCMD)

PORT ADDRESS = BASE + 1

WRITE: Command / Data Out **READ: Data In**

Bit 7	Command/Data Out	Bit 7	Bit 7	Data In	Bit 7
Bit 6	"	Bit 6	Bit 6	"	Bit 6
Bit 5	"	Bit 5	Bit 5	"	Bit 5
Bit 4	"	Bit 4	Bit 4	"	Bit 4
Bit 3	"	Bit 3	Bit 3	"	Bit 3
Bit 2	"	Bit 2	Bit 2	"	Bit 2
Bit 1	"	Bit 1	Bit 1	"	Bit 1
Bit 0	"	Bit 0	Bit 0	"	Bit 0

PORT ADDRESS = BASE + 2

WRITE: Reserved, do not write **READ: Interrupt Flags**

Bit 7		Bit 7	Any Interrupt
Bit 6		Bit 6	Reserved
Bit 5		Bit 5	Reserved
Bit 4		Bit 4	Reserved
Bit 3		Bit 3	SCSI Reset Detected (SCRD)
Bit 2		Bit 2	HA Command Complete (HACC)
Bit 1		Bit 1	MBO Empty (MBOA)
Bit 0		Bit 0	MBI Full (MBIF)

4.2.1 Control and Status Port

Writing a one to the bits of the Control Port initiates certain special host adapter operations. There is no requirement to return the bits to the zero state, since they are reset automatically after the requested operation is initiated. Read operations to the Status port address return host adapter status information.

Base+0 Port, Write: Host Adapter Control Port.

Bit 7 Hard Reset (HRST): The setting of the Hard Reset bit to one forces the host adapter into a state identical to a normal power on state. Diagnostic functions are executed and all status for ongoing SCSI operations is lost. A Reset Condition is generated on the SCSI bus. While the reset is being processed, the Self Testing in Progress bit (Host Adapter Status Port bit 7) is set. When the reset is complete, that bit is reset and the Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set, indicating that the AHA-154XA mailbox structure must be re-initialized and that no other operations are active on the host adapter. See section 4.3, describing the overall reset structure.

Bit 6 Soft Reset (SRST): The Soft Reset bit clears all ongoing SCSI and host adapter commands. All Command Control Blocks are abandoned and all queued commands are abandoned. Mailbox In and Mailbox Out entries must be cleared by the host. No diagnostic functions are executed. No Reset Condition is generated on the SCSI bus. The Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set when the reset processing is completed. This indicates that the AHA-154XA Mailbox structure must be re-initialized and that no other operations are active on the Host Adapter. See section 4.3, describing the overall reset structure.

Bit 5 Interrupt Reset (IRST): The setting of this bit clears the interrupt port of all bits that have been set and resets the interrupt line. The host adapter manages the interrupt presentation to minimize the possibility of incorrectly resetting an interrupt. MBOE and MBIF interrupts are presented immediately unless an SCRD or HACC interrupt has not yet been cleared. An SCRD or HACC will only be presented after any interrupt bit has been cleared and DF is zero, indicating an operation is fully completed. The prompt resetting of MBOE and MBIF interrupts minimizes the chance of a reset of one also resetting the other. Host programs should, however, be aware that there is a small chance of falsely resetting a new MBIF reset while clearing an MBOE interrupt. This can be resolved by periodically scanning the MBI entries when activity is expected on the host adapter or by not enabling the MBOE interrupt.

Bit 4 SCSI Bus Reset (SCRST): The setting of this bit causes a SCSI Bus Reset to be generated on the SCSI bus. The SCSI Bus Reset is triggered at the time the SCRST bit is set to one and raises the RST line on the SCSI Bus for the architected 25 microsecond period. The reset is managed as a SCSI Soft Reset and will allow partially completed operations to continue after the reset occurs. See section 4.3, describing the overall reset structure.

Bits 0-3 Reserved: Reserved bits must be set to zero to avoid compatibility problems with future extensions of the Control Register.

Base+0 Port, Read: Host Adapter Status Port

Bit 7 Self Testing in progress (STST): This bit, when one, indicates that the host adapter is performing self-initialization and internal diagnostics. The bit is asserted after a power-on or hard reset (Control Port Bit 7 HRST = 1). When diagnostic operation is complete, the STST bit is set to zero and bit 5 or bit 6 is set to indicate the successful or unsuccessful completion of the diagnostics. If bit 7 remains on, it indicates that the initialization or diagnostic could not be completed. The error condition can be determined as described in section 10. In most cases, bit 6 (DIAGF) will be set to indicate that an internal diagnostic failure occurred.

Bit 6 Internal Diagnostic Failure (DIAGF): This bit, when one, indicates that the self-testing process has completed and that an error was detected. The host adapter must be reset by setting the Hard Reset bit (bit 7 of the Control Port) to clear the error. If the AHA-154XA again detects an error, troubleshooting procedures must be performed to identify and correct the error condition. The diagnostic LED will usually present a flash code that indicates the nature of the failure. Section 10 describes the corrective procedures.

Bit 5 Mailbox Initialization Required (INIT): This bit, when one, indicates that the self-testing process has completed successfully and that the AHA-154XA is ready for mailbox initialization to be performed. The base memory address of the Mailbox area must be established by execution of the Mailbox Initialization command. After execution of the Mailbox Initialization command and any other desired initialization operations, the AHA-154XA is ready for full operation.

Bit 4 SCSI Host Adapter Idle (IDLE): This bit, when one, indicates that the host adapter is in the idle state. The host adapter has no outstanding Adapter Commands or SCSI commands. The host processor must wait for the idle state before executing any Adapter Command except the Start SCSI (02) and Enable Mailbox Out Interrupt (05) commands.

Bit 3 Command / Data Out Port Full (CDF): The host uses the CDF bit to synchronize command and data transfers to the host adapter. An Adapter Command byte or an outbound parameter byte can be placed in the Command / Data Out Port when the port is empty, indicated by the CDF bit being zero. When a byte is placed in the Command / Data Out Port, the CDF bit is set to one and remains one until the host adapter has obtained and processed the byte. When the CDF bit returns to zero, the next Command or parameter byte can be placed in the port.

Bit 2 Data In Port Full (DF): The host uses the DF bit to synchronize transfers of data from the host adapter to the host. When the DF bit is set to one, the host adapter has placed a byte in the Data In Port for the host to remove and process. When the host performs a read to the Data In Port address, the DF bit is set back to zero automatically and not set to one again until a new data byte has been placed in the Data In Port by the host adapter for the host.

Bit 1 Reserved: This bit is zero.

Bit 0 Invalid Host Adapter Command (INVDCMD): The Invalid Host Adapter Command bit is set to one if an invalid command or parameter byte was received in the Command / Data Out Port . After sending a command byte or data byte, the host software determines that the next byte is ready to send by waiting for the CDF bit to be reset. If the command byte or parameter byte is not valid, the command sequence will instead be terminated by the host adapter. The host adapter always terminates a command by raising the Host Adapter Command Complete (HACC) interrupt. If the HACC interrupt is set to one and the INVDCMD bit is not set, the command terminated normally. If the INVDCMD bit is also set to one, the command or parameter bytes were determined to be invalid and the command terminated abnormally. The INVDCMD bit is only valid from the time the HACC interrupt is set until the HACC interrupt is reset. The bit's value is not predictable until a new HACC interrupt is set for a new Adapter Command.

4.2.2 Command/Data Out and Data In Port

The second I/O port address is used by the host to write Adapter Command bytes and accompanying parameter data bytes to the host adapter. It is also used by the host adapter to send parameters back to the host to be read. The Command / Data Out Port is used by the host to send host adapter initialization and management commands and parameters that cannot be sent by the standard Mailbox protocol. Information requested by the Adapter Commands placed in the Command / Data Out Port is returned through the Data In Port. The host should understand the format and number of bytes to be transmitted for each command so that extra invalid bytes are not passed across the interface. Bytes in addition to those required by the particular command are

likely to be interpreted as invalid, although they may instead cause the execution of valid commands that were not supposed to be performed.

The host should only write to the Command / Data Out Port when CDF is zero. This allows time for the host adapter to process a previously written command or parameter byte. CDF is automatically set to one when the host writes to the port and is reset to zero after the host adapter removes the byte from the port.

If an Adapter Command needs additional data bytes, the host waits until CDF is zero before writing the additional bytes to the Command / Data Out Port. Just as in the command transfer case, each parameter byte written will set the CDF. The host can write additional data bytes only after CDF is again zero. The HACC interrupt will indicate when the command has terminated, normally or abnormally. If INVDCMD is also set, the host adapter found either the command or data bytes to be invalid and terminated abnormally. The use of CDF as a hand-shaking bit is required to prevent the transfer of invalid data.

If an Adapter Command requires data transfer from the host adapter, the host adapter will place the data bytes in the Data In Port and set the DF bit (Status Port bit 2) to indicate that the requested parameter is ready for the host to read. When the host reads the Data port, DF is automatically reset. The host should wait until DF is again set before attempting to transfer the next parameter byte. The use of the DF bit to control the hand-shaking process is required to prevent the transfer of invalid data. After the last data byte has been transferred, the HACC interrupt bit will be set indicating command completion. If the Adapter Command was invalid, the HACC interrupt will occur before all data bytes have been transmitted and the INVDCMD bit will be set.

4.2.3 Interrupt Flag Port

The Interrupt Flag Port contains bits that indicate the reason that an interrupt was provided to the host from the host adapter. The host adapter uses the interrupt to notify the host that the host adapter is ready for immediate service from the host. The Interrupt Flag Port is a read-only port. When an interrupt bit is set by the host adapter to indicate that the host should respond, the Any Interrupt bit and the interrupt line are both also set. When the host begins to examine the returned registers and mailboxes to determine the cause of the interrupt and to perform the operations needed to service the interrupt, the host will first read the Interrupt Flag Port to record which interrupts must be serviced. The host will then clear the interrupts by setting the IRST bit (Host Adapter Control Port bit 5). The host adapter presents MBOA and MBIF interrupts immediately unless there is already an SCRD or HACC interrupt present. If the SCRD or HACC is present, the MBOA and/or MBIF interrupt will be posted after the SCRD or HACC interrupt is cleared. An SCRD or HACC interrupt will only be presented if the Any Interrupt signal is zero and the DF signal is zero, indicating the completion of all pending interrupt presentation. It is recommended that the MBOA interrupt be enabled only when required by the host. This prevents the possible presentation and resetting of MBIF interrupts before they are processed. Other reset operations will also reset the Interrupt Flag Port and the interrupt line, including the Hard Reset bit (HRST), the Soft Reset bit (SRST), and the power on reset issued by the motherboard.

Base+2 Port, Read only: Interrupt Flag Port

Bit 7 Any Interrupt: This bit, when one, indicates that the interrupt to the host has been established. The actual identify of the interrupting condition is provided in bits 0 to 3.

Bit 6 Reserved: Returned as zero.

Bit 5 Reserved: Returned as zero.

Bit 4 Reserved: Returned as zero.

Bit 3 SCSI Reset Detected (SCRD): This bit, when one, indicates that a SCSI Reset has been received on the SCSI bus. The Any Interrupt bit and the AT interrupt signal will also be set. The host adapter supports SCSI Soft Reset (see section 4.3). Any ongoing target or initiator activities will continue normally after first clearing the SCSI bus. In some rare cases, host intervention will be required to restart a SCSI command that was aborted by the reset operation. The host can convert the SCSI Soft Reset to a SCSI Hard Reset by setting the Control Register Soft Reset (Bit 6) to one, clearing all ongoing operations in the host adapter. In this case, the host must recognize that any operations not yet completed will never be completed and must perform appropriate error recovery operations. See section 4.3, describing the overall reset protocol. The SCRD bit is not set for host initiated SCSI Reset conditions caused by the setting of the HRST bit or the SCRST bit, since the host is already aware of the actions it has requested. If the Any Interrupt signal or DF signal is present, the SCRD interrupt will not be presented until the interrupts already present are cleared.

Bit 2 Host Adapter Command Complete (HACC): This bit, when one, indicates that an Adapter command has been completed, normally or abnormally. The Any Interrupt bit and the AT interrupt signal will also be set. If the command was completed normally, only the HACC bit will be on. If the command was completed abnormally or was aborted before it was completed, the HACC bit will be one and the Invalid Command Bit (Status Register bit 5) will also be one. During parameter transfers to or from the host adapter, the HACC bit should be examined to verify that the command is still being processed and has not been ended abnormally. If the Any Interrupt signal or DF signal is set, the HACC interrupt will not be presented until the interrupts already presented are cleared.

Bit 1 Mailbox Out Available (MBOA): This bit, when one, indicates that an outbound Mailbox entry is now available for use by the host. The Any Interrupt bit and the AT interrupt signal will also be set. Most operating systems will choose to leave this interrupt disabled to avoid the generation of extra interrupts. The host adapter will normally empty Mailbox Out entries to its local RAM so rapidly that round robin filling of the Mailbox Out entries will assure that a Mailbox Out entry will already be empty by the time that the host is ready to fill it again.

If the host finds that all Mailbox Out entries are full, it can enable the Mailbox Out Available interrupt by executing an Enable Mailbox Out Interrupt command through the I/O Command Port. The Enable Mailbox Out Interrupt command is one of the two commands that can be executed without waiting for the IDLE state of the host adapter. As soon as any Mailbox Out entry is cleared by the host adapter, an MBOA interrupt will be generated to indicate to the host that an MBO entry is available. An MBOA interrupt is generated after that each time a Mailbox Out entry is cleared by the host adapter until an Enable Mailbox Out Interrupt command is executed to force the reporting of MBOA interrupts to be disabled. If the SCRD or HACC interrupts are present, the MBOA interrupt is not presented until they are cleared. At all other times, MBOA is presented immediately.

Bit 0 Mailbox In Full (MBIF): This bit, when one, indicates that an entry has been placed by the host adapter in the Mailbox In. The interrupt should be reset as soon as possible so that any subsequent interrupts can be detected. The host adapter may return information in other Mailbox In entries, so the host should check the next

entry to determine if more than one set of information has been provided. The MBI entries are filled in round-robin order, so the host should simply check the next MBI entry after the last one that was found when a new MBIF interrupt occurs.

If an MBIF interrupt is set and other Mailbox In entries are made before the interrupt is cleared, then all the entries can be scanned as found. The new MBIF interrupt will be presented if the SCRD and HACC interrupts are cleared. A new MBIF interrupt will be presented regardless of the state of the MBOA interrupt bit. It is important to clear and record each interrupt as soon as possible to avoid the possible accidental resetting of a valid interrupt. In addition, it is desirable to enable the MBOA interrupt as rarely as possible. The host system software must be ready to scan for MBI entries even if no MBIF interrupt occurred.

4.3 RESET OVERVIEW

The reset functions provided by the AHA-154XA are extensive to allow the fullest flexibility and architectural consistency, both with SCSI and with the Industry Standard Architecture.

4.3.1 Hard Reset Operations

Resets may be generated by the hardware through two mechanisms. The RESET signal from the ISA socket is generated by the system board to reset or initialize all installed adapters upon power on or during a low line voltage condition. The system can also activate this signal under host program control. In addition to the RESET signal, the setting of the HRST bit (bit 7 of the Host Adapter Control Port) will force a hardware reset to the AHA-154XA. Regardless of the source, a Hard Reset forces the following actions on the AHA-154XA.

- All internal registers of the AHA-154XA are returned to their reset condition.
- The host adapter's microprocessor returns all internal information and parameters to their initial state.
- The host adapter performs all required internal diagnostics.
- A standard SCSI Reset condition is generated to all other attached SCSI devices.

During the Hard Reset process, the AHA-154XA will indicate to the attached host that self-testing is in process by raising the STST bit in the Host Adapter Status Port. After the Hard Reset process is complete, the AHA-154XA will indicate that initialization parameters are required from the host by raising the INIT bit in the Host Adapter Status Port.

4.3.2 SCSI Reset Operations

The SCSI Reset condition is defined in the SCSI Standard, X3.131-1986, section 5.2.2. A SCSI Reset condition may be forced by any SCSI device on the bus. The condition is forced by the assertion of the SCSI Reset signal.

The AHA-154XA has four mechanisms which may force a SCSI Reset condition. The SCSI Reset condition may be invoked from the host software if the software sets the SCRST bit (Bit 4 of the Host Adapter Control Port). In this case, the normal SCSI Reset operations will be performed by the Host Adapter and the SCSI Reset signal will be asserted on the SCSI bus. In this case, the SCRD bit (Interrupt Flag Port bit 3) will not be set, since the host itself caused the reset.

The SCSI Reset is invoked if a hard reset is generated, either by the system board RESET signal or by the setting of the HRST bit. This reset is described in Section 4.3.1.

The SCSI Reset condition may be invoked by the AHA-154XA as part of the recovery mechanism for a bus phase error. Bus phase errors may include detection of an invalid information transfer phase or detection of an impossible phase sequence (Command Phase after a Data Phase in the same command). In this case, the normal SCSI Reset operations will be performed and the SCSI Reset signal will be asserted on the SCSI bus. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate interrupt signal to be presented.

The SCSI Reset condition may be invoked by another SCSI device attached to the AHA-154XA as part of the other device's recovery mechanism or initialization procedure. In this case, the normal SCSI Reset operations will be performed. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate ISA interrupt signal to be presented.

4.3.2.1 SCSI "Soft" Reset Option

The SCSI standard indicates two optional methods of handling the normal SCSI Reset operations. The AHA-154XA implements the "Soft" Reset Option, described in section 5.2.2.2 of the SCSI specification. The "Soft" Reset Option is designed to allow a SCSI Reset signal to correctly clear the SCSI bus, but to allow ongoing system operations to continue without any major interruptions. When the SCSI Reset occurs, any activity on the SCSI bus is immediately halted and all bus lines are cleared from the bus. After the Reset condition ends, any operations in progress are again allowed to start up in the normal manner. No status or pointer information is destroyed. All disconnected commands are allowed to reselect and continue in the normal manner. This "Soft" Reset function allows a multiple initiator system to use reset to clear certain types of bus failures without damaging ongoing tasks from any initiator.

The SCSI "Soft" Reset option is useful in multitasking systems that cannot tolerate the overhead of a complex reconfiguration and reinitialization after a normal reset operation. For the SCSI "Soft" Reset option to operate correctly, all SCSI devices that communicate on the SCSI bus must support the "Soft" Reset option. If any SCSI devices support the "Hard" Reset option, it is likely that operations will be terminated without warning and the system will have to time out and monitor the requirement to restart some activities.

4.3.2.2 SCSI "Hard" Reset Option

The "Hard" Reset Option is designed to restore all attached SCSI devices, including both hosts and peripheral devices, to their power on reset state. All system activities that have not been recorded on a non-volatile memory device or through another SCSI path are completely lost and must be restarted. The system must be completely re-initialized. For certain types of systems that frequently do back-up or check point their transactions, that re-initialize quickly and easily, or that infrequently do resets, the "Hard" Reset Option is appropriate. The AHA-154XA responds to a SCSI Reset Condition by executing only the "Soft" Reset Option, but it notifies the host whenever a SCSI Reset condition has been established by causing an interrupt to the host. The host then has the option of converting the "Soft" Reset to a "Hard" Reset by forcing the host adapter to clear all the ongoing operations and return to its initial state. The host requests this by raising the SRST bit (bit 6 of the Host Adapter Control Port). The host must raise the SRST bit within 300 microseconds to disable the restarting of operations according to the rules of "Soft" Reset. The raising of the SRST bit causes the host adapter to abandon all CCB's and prepare itself to begin accepting new instructions from the host. No secondary SCSI Reset signals are activated. The Mailbox initialization and all normal SCSI initial conditions are reset by the SRST bit, so that reinitialization is required to restart the system. Of course the system still has the right at any time that the IDLE bit (bit 4 of the Host Adapter Status Port) is on to execute any of the Adapter Commands and modify the Mailbox Address or the SCSI initial conditions.

If the host requires that the SCSI be reset according to the SCSI "Hard" Reset option, the host raises the HRST bit. The host adapter will then set a SCSI Reset Condition on the SCSI Bus and clear all its CCB and status information, thus performing a SCSI "Hard" Reset with a single load to the Host Adapter Control Port. Reinitialization will be required.

Section Five Firmware Functional Description

5.1 HOST ADAPTER COMMAND OVERVIEW

The AHA-1540A/1542A supports two types of commands: SCSI and Adapter Commands. SCSI commands are issued using the mail box protocol and a Command Control Block. When SCSI commands are used, the AHA-1540A/1542A is operating in true multithreading mode. In this mode of operation, the AHA-1540A/1542A is capable of executing multiple commands for multiple targets concurrently. The AHA-1540A/1542A maximizes the I/O transaction throughput by managing SCSI disconnection and reconnection.

Adapter Commands are issued by writing to the Command / Data Out port. Most Adapter commands can not be issued when there are outstanding SCSI commands. Adapter commands are used to initialize the host adapter and to establish control conditions within the host adapter. Adapter commands are also used to transmit the special parameters for communication between the BIOS and the host adapter for the execution interrupt 13 operations.

5.1.1 Adapter Command Operation Codes

Below is a list of the Adapter Command operation codes.

00 -- No Operation
01 -- Mailbox Initialization
02 -- Start SCSI Command *
03 -- Start PC/AT BIOS Command
04 -- Adapter Inquiry
05 -- Enable Mailbox Out Available Interrupt*
06 -- Set Selection Time-out
07 -- Set Bus-On Time
08 -- Set Bus-Off Time
09 -- Set Transfer Speed
0A -- Return Installed Devices
0B -- Return Configuration Data
0C -- Enable Target Mode†
0D -- Return Setup Data†
1A -- Write Adapter Channel 2 Buffer†
1B -- Read Adapter Channel 2 Buffer†
1C -- Write Adapter FIFO Buffer
1D -- Read Adapter FIFO Buffer
1F -- ECHO Command Data

**Note: This command can be issued when the host adapter is executing a SCSI command.*
† These commands are not supported by the AHA-1540.

All Adapter Commands except Start SCSI (02) and Enable Mailbox-Out Available Interrupt (05) must be executed only when the IDLE bit (Status bit 4) is one. Many commands require additional parameter bytes which are then written to the Command / Data Out I/O port (base + 1). Before each byte is written by the host to the host adapter, the host must verify that the CDF bit (Status bit 3) is zero, indicating that the command port is ready for another byte of information. The host adapter usually clears the Command / Data Out Port within 100 microseconds. Some commands require information bytes to be returned from the host adapter to the host. In this case, the host monitors the DF bit (Status bit 2) to determine when the host adapter has placed a byte in the Data In I/O port for the host to read. The DF bit is reset automatically when the host reads the byte. The format of each Adapter Command is strictly defined, so the host adapter and host system can always agree upon the correct number of parameter bytes to be transferred during a command.

All Adapter Commands except Return Installed devices, Start SCSI, and Start PC/AT BIOS typically require less than 200µs to complete. Return installed devices will typically complete in less than 3 seconds. Start SCSI and Start PC/AT commands completion times will vary with the SCSI device and the command issued.

5.1.1.1 No Operation (Operation Code 00)

No host adapter action is taken, but HACC is set indicating command completion. No additional information bytes are exchanged.

5.1.1.2 Mailbox Initialization (Operation Code 01)

This command is used to specify the number of mailbox locations used by the host adapter and to specify the base memory location of the mailbox area. The host adapter requires that four bytes of outbound data follow the command byte. The definition of those four bytes is shown below.

00	Mailbox count	(>0)
01	Mailbox address	(MSB)
02	Mailbox address	
03	Mailbox address	(LSB)

Byte 0	Mailbox Count:	The Mailbox count must be greater than zero.
Byte 1,2,3	Mailbox Address:	The Mailbox address specifies the location of the first byte of the Mailbox area. Byte 1 is the most significant byte.

When the Mailbox Initialization command and parameters are received, the host adapter will then assume that the specified number of Mailbox Out entries and the same number of Mailbox In entries will be assigned beginning at the Mailbox address. The total number of bytes reserved for the Mailbox area will be eight times the Mailbox count. If the Mailbox Count is zero, the INVDCMD bit will be set with HACC to indicate that the parameter is invalid.

At command completion, HACC will be set to one and INIT will be reset to zero. HACC will be reset as specified by section 4.2.3.

5.1.1.3 Start SCSI Command (Operation Code 02)

This command indicates that the host has made at least one Mailbox Out entry and that the host adapter should begin to scan for active MBO entries. Once scanning has been started, it continues until all MBO entries have been serviced, either by beginning the requested operations or by queueing the activities for later execution. Since it is not easy for the host to determine that scanning is still taking place, the host should normally issue this command every time a Mailbox Out is filled. This command does not require additional data bytes. To avoid unnecessary interrupts, HACC is NOT set after command completion. HACC will be set with INVDCMD if the mailbox was not yet initialized.

5.1.1.4 Start PC/AT BIOS Command (Operation Code 03)

This command is used by the Adaptec BIOS to communicate with the host adapter firmware. The command is not available for use by programs other than the Adaptec BIOS.

5.1.1.5 Adapter Inquiry (Operation Code 04)

After receiving this command, the host adapter returns four bytes of data describing the host adapter firmware revision level. After completing the transfer of the four bytes of inbound data, the HACC interrupt is set indicating normal command completion. The bytes contain the following information:

00	Board Identification
01	Special Options Identification
02	Hardware Revision Level
03	Firmware Revision (ASCII)

Byte 0 Board ID: The value in this byte allows software supported on both the PC/AT and on the Microchannel™ to distinguish the type of supporting host adapter.

Value	Meaning
00H	Board is an AHA-1540 with 16 Head BIOS
30H ('0' ASCII)	Board is an AHA-1540 with 64 Head BIOS
41H ('A' ASCII)	Board is an AHA-1540A/1542A, 64 Head BIOS
42H ('B' ASCII)	Board is an AHA-1640, 64 Head BIOS
All Others	Reserved

Byte 1 Special Options ID: The value in this byte indicates what special options are supported on the AHA-154XA host adapter. Other host adapters use other values in this byte.

Value	Meaning
41H ('A' ASCII)	Board is standard model
All Others	Reserved

Byte 2	Firmware Revision:	This value indicates an ASCII value from 0-9,A-Z that indicates the firmware revision installed in the AHA-154XA.
Byte 3	Firmware Revision:	This value indicates an ASCII value from 0-9,A-Z that indicates the firmware revision installed in the AHA-154XA.

After completing this command, HACC will be asserted, indicating normal completion.

5.1.1.6 Enable Mailbox-Out Available Interrupt (Operation Code 05)

The Enable Mailbox Out Available Interrupt command specifies that a Mailbox Out Available Interrupt should be generated whenever a Mailbox Out entry has been cleared by the host adapter. One byte of outbound data is transmitted to indicate whether the interrupt should be enabled or disabled.

Byte 0	Enable/Disable Parameter:	The Enable/Disable parameter byte must be either 00H or 01H. If the Enable/Disable parameter byte is 00H, the Mailbox Out Available interrupt is not returned. If the Enable/Disable parameter byte is 01H, the Mailbox Out Available interrupt is returned as soon as a Mailbox Out has been cleared by the host adapter.

After completing this command, HACC will NOT be asserted to avoid generating additional interrupts. If the data byte is neither 00 nor 01, INVDCMD will be asserted indicating an invalid command. In this case, HACC will also be asserted.

The Mailbox Out Available interrupt is normally intended to be used by the host as an indicator that a Mailbox Out entry is available. This function should only be enabled if all Mailbox Out entries have been found full by the host. It should be disabled soon afterward. If used in other ways, the interrupt may generate a large number of relatively useless interrupt handling activities.

5.1.1.7 Set Selection Time-out (Operation Code 06)

This command sets the SCSI selection time out value. The SCSI Selection time out value is used to determine whether or not a SCSI selection was successful. If the SCSI BSY signal is not returned within the specified time out value, the selection will be terminated and an appropriate error message posted with the returned CCB. This command expects four outbound data bytes to be provided as defined below:

00	Enable/Disable Selection Time Out	
01	Reserved (00)	
02	Time Out Value	(MSB)
03	Time Out Value	(LSB)

Byte 0	Enable/Disable Selection Time Out:	This parameter byte specifies whether or not the Selection Time-out will be used. If the byte is set to 00H, no time-out will be performed. If the byte is set to 01H, the time specified in bytes 02 and 03 will be used as the Selection Time Out by the SCSI. The default value established by the reset process is 01H, indicating the time out is enabled.
Byte 1	Reserved:	This byte must be zero.
Byte 2,3	Time Out Value:	This two-byte value specifies the time in milliseconds that will be used for the Selection Time Out. The default value is 250 milliseconds.

After completing this command, HACC will be asserted, indicating normal completion. INVDCMD will be asserted if the data byte 0 is neither 00 nor 01 or if byte 1 is not zero, indicating an invalid command.

5.1.1.8 Set Bus-On Time (Operation Code 07)

This command specifies the time that the host adapter spends on the bus when transferring data. The Bus-On duration is adjustable from 2 to 15 microseconds. The default setting is 11us. One data byte is passed out to the host adapter to indicate the Bus-On duration in microseconds.

Data Byte 0 -- Bus On-Time (2 to 15 us)

After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 15. The valid range is 2 to 15 decimal.

5.1.1.9 Set Bus-Off Time (Operation Code 08)

This command sets the time that the host adapter will spend off the bus during a data transfer. The Bus-On duration is adjustable from 1 to 64 microseconds. The default setting is 4us. After receiving this command, the host adapter expects one byte of data which specifies the bus off time in microseconds.

Data Byte 0 -- Bus-Off Time (1 to 64 us)

After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 64. The valid range is 1 to 64 decimal. The actual time implemented by the host adapter is rounded down to the next four microsecond step at or below the specified value. The minimum value is approximately one microsecond.

5.1.1.10 Set Transfer Speed (Operation Code 09)

This command adjusts the Bus Master DMA circuitry to a specified maximum AT bus transfer speed to and from the host memory. Several speeds may be selected by setting the jumper configuration as explained in section 3.3. The selected jumper speeds are overridden if the Set Transfer Speed command is executed. The single data byte transmitted after the command byte either sets the read and write speed together, or establishes separate values for each. Appendix A gives the timings that result from the selected values. The default setting is the value set by the jumpers. The I/O Channel Ready signal automatically slows the system further if required by the host memory.

Data Byte 0 -- AT Bus Transfer Speed
00 -- 5.0 MB/second
01 -- 6.7 MB/second
02 -- 8.0 MB/second
03 -- 10 MB/second
04-- 5.7 MB/second
80-FF -- See Table

Custom Transfer Speed		
bit 7	1	
bit 6-4	000	Read pulse width (ns) 100
	001	150
	010	200
	011	250
	100	300
	101	350
	110	400
	111	450
bit 3	0	Strobe off time = 100ns
	1	Strobe off time = 150ns
bit 2-0	000	Write pulse width (ns) 100
	001	150
	010	200
	011	250
	100	300
	101	350
	110	400
	111	450

After completing this command HACC is set indicating normal completion.

5.1.1.11 Return Installed Devices (Operation Code 0A)

This command returns information about which SCSI Targets and Logical Units (LU's) are installed on the SCSI bus. The host adapter issues the SCSI Test Unit Ready command to each target/LUN combination and reports the results using eight bytes of data returned through the Data In Register. A bit having a value of one indicates that the associated LU is installed. Each byte is associated with the corresponding target. Each bit within a target byte is associated with a particular Logical Unit, bit 7 indicating the presence of LU 7 and so forth. The state of the target is analyzed using the SCSI TEST UNIT READY command, analyzing the returned data to determine if the addressed LU is available.

After receiving this command, the host adapter returns eight bytes of information which specify the installed configuration as shown below:

Byte 0	Target 0 Configuration:	
	Bit 7	LU 7 Installed
	Bit 6	LU 6 Installed
	Bit 5	LU 5 Installed
	Bit 4	LU 4 Installed
	Bit 3	LU 3 Installed
	Bit 2	LU 2 Installed
	Bit 1	LU 1 Installed
	Bit 0	LU 0 Installed
Byte 1	Target 1 Configuration	
Byte 2	Target 2 Configuration	
Byte 3	Target 3 Configuration	
Byte 4	Target 4 Configuration	
Byte 5	Target 5 Configuration	
Byte 6	Target 6 Configuration	
Byte 7	Target 7 Configuration	

The byte associated with the SCSI Device Identifier of the host adapter will always be zero. After completing the information transfer, the HACC bit will be set to indicate normal completion.

5.1.1.12 Return Configuration Data (Operation Code 0B)

The DMA arbitration priority, the Interrupt channel, and the SCSI ID of the adapter are returned by this command. The three bytes of information are returned in the following format:

Byte 0	DMA Arbitration Priority:	
	Bit 7	Channel 7
	Bit 6	Channel 6
	Bit 5	Channel 5
	Bits 4-1	Reserved (0)
	Bit 0	Channel 0
Byte 1	Interrupt Channel:	
	Bit 7	Reserved (0)
	Bit 6	Interrupt channel 15
	Bit 5	Interrupt channel 14
	Bit 4	Reserved (0)
	Bit 3	Interrupt channel 12
	Bit 2	Interrupt channel 11
	Bit 1	Interrupt channel 10
	Bit 0	Interrupt channel 9
Byte 2	SCSI Identifier	
	Bits 7-3	Reserved (0)
	Bits 2-0	Binary value of SCSI Identifier

After completing this command, HACC will be set indicating normal completion.

5.1.1.13 Enable Target Mode Command (Operation Code 0C)

A special host adapter command (0C) enables and disables target mode. The host adapter requires that two bytes of outbound information follow the command byte. The information bytes contain the following information:

Byte 0	Enable/Disable Target Mode:	This parameter specifies which operating modes the host adapter will use. If the byte is set to 00H, the AHA-1540A/1542A will operate only in Initiator Mode. If the byte is set to 01H, the host adapter will operate both as an initiator and as a Processor type Target SCSI Device. Any other value is invalid. The default value after a Hard Reset, Soft Reset, or Power On Reset is 00H (Initiator only).
Byte 1	Logical Unit Mask:	This parameter byte contains an eight bit bit-significant mask indicating the Logical Units which will respond in Target Mode. Bit 7 corresponds to LU 7, and so forth. If the bit is one, the corresponding LU will be treated as installed. If the bit is zero, the LU will be treated as not installed.

If the AHA-1540A/1542A does not have the Target Mode feature installed, the host adapter will indicate an invalid host adapter command. If an attempt is made to change from target mode while there are still target mode CCB's being processed by the host adapter, the host adapter will post an invalid host adapter command indication.

If the command disables Target Mode, the Logical Unit Mask byte will be ignored. If the command enables Target Mode, the Logical Unit Mask byte must contain at least one bit, indicating the presence of at least one Logical Unit.

The SCSI INQUIRY command will provide an indication to other initiators that the Logical Unit is installed or not installed in byte 1 of the returned inquiry data.

If target mode is not enabled, the host adapter will behave on the SCSI interface as if it were an ordinary SCSI initiator. Any attempt to select the host adapter will result in a SCSI selection time out. Most Reset Operation, including Soft Reset, Hard Reset, and Power-On Reset will return the AHA-1540A/1542A Target Mode to the disabled state. SCSI Resets, generated either by the host or by other SCSI Devices, will not change the previously established enabled or disabled state of Target Mode.

5.1.1.14 Return Setup Data (Operation Code 0D)

This command returns information describing the setup of the host adapter. The information returned reflects either the values supplied by previous host adapter commands or default values. The command is followed by an outbound data transfer and an inbound data transfer. The outbound transfer is a one byte parameter indicating the length of the required inbound data transfer. The inbound data transfer contains from zero to 255 bytes of information describing the setup of the host adapter. The inbound information normally transferred will be truncated or padded with zeros as necessary to transfer the requested number of bytes. The number of bytes normally transferred by the AHA-154XA is 16.

Outbound Data Byte:

Byte 0	Data In Length:	The number of data bytes requested can be from 0 to 255. A value of zero will be accepted and 256 bytes will be returned.

Inbound Data Summary:

00	SDT and Parity Status
01	Transfer Speed
02	Bus On Time
03	Bus Off Time
04	Number of Mailboxes
05	Mailbox Address (MSB)
06	Mailbox Address
07	Mailbox Address (LSB)
08-0F	Synchronous Transfer Agreements
10-FF	Reserved (00)

Inbound Data Bit Assignments:

Byte 0	SDT and Parity Status:	
	Bit	Meaning
	0	If this bit is zero, Synchronous Data Transfer negotiation will not be initiated by the host adapter, but will be responded to if requested by an attached SCSI Device. If the bit is one, Synchronous Data Transfer negotiation will be initiated by the host adapter under those conditions which require such negotiation. The state is set from jumper J1.
	1	If this bit is zero, parity checking on inbound SCSI transfers has been disabled. If this bit is one, parity checking on inbound SCSI transfers is enabled. The state is set from jumper J1.
	2-7	Reserved (0)
Byte 1	Transfer Speed	This byte returns the value passed in to the host adapter by the Set Transfer Speed command (See Section 5.1.1.10)
Byte 2	Bus On Time:	Indicates the Bus On Time in microseconds (See Section 5.1.1.8)
Byte 3	Bus Off Time:	Indicates the Bus Off Time specified by the Bus Off Time Value in microseconds. (See Section 5.1.1.9)

Byte 4	Number of Mailboxes:	The number of Mailboxes established by a previous Mailbox Initialization command will be returned in this byte. This number will be 00H if the Mailbox Initialization command has not yet been successfully completed.
Byte 5-7	Mailbox Address:	The base address of the Mailbox area established by a previous Mailbox Initialization command will be returned in these bytes. The Most Significant byte is byte 5. These bytes have no meaning if Mailbox Initialization has not yet been successfully completed.
Byte 8	Sync Neg, Target 0	Returns information about the synchronous negotiation with Target 0. The byte will be 00H for the address of the host adapter.
	Bit 7	Set to one if synchronous transfer is negotiated. Set to zero if asynchronous transfer is being performed.
	Bits 6-4	These bits contain a value between 0 and 7 that defines the synchronous transfer period according to the following equation. Period = 200 + 50 (value) nanoseconds
	Bits 3-0	These bits contain the negotiated offset value. The value will normally be between 1 and 7.
Byte 9	Sync Neg, Target 1	Same as byte 8, for target 1
Byte 10	Sync Neg, Target 2	Same as byte 8, for target 2
Byte 11	Sync Neg, Target 3	Same as byte 8, for target 3
Byte 12	Sync Neg, Target 4	Same as byte 8, for target 4
Byte 13	Sync Neg, Target 5	Same as byte 8, for target 5
Byte 14	Sync Neg, Target 6	Same as byte 8, for target 6
Byte 15	Sync Neg, Target 7	Same as byte 8, for target 7

If the command completes normally, the HACC interrupt will be set to one. If the Mailbox area has not been properly initialized, all 16 bytes are still requested by the host. If byte 4, the Number of Mailboxes, is zero, bytes 5-7 must be ignored.

5.1.1.15 Write Adapter Channel 2 Buffer (Operation Code 1A)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to will be transferred to the host adapter's Channel 2 Buffer using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the indicated buffer area to the host adapter, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Read Channel 2 Buffer command for host adapter diagnostics. The Channel 2 Buffer is used for transmission of all information except the actual data field between the host adapter and the host system.

Byte 0	Buffer area address, Most significant byte
Byte 1	Buffer area address
Byte 2	Buffer area address, Least significant byte

5.1.1.16 Read Adapter Channel 2 Buffer (Operation Code 1B)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to will be used as a buffer to receive 64 bytes of information transferred from the host adapter's Channel 2 Buffer to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the Channel 2 Buffer to the indicated host memory area, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Write Channel 2 Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte
Byte 1 Buffer area address
Byte 2 Buffer area address, Least significant byte

5.1.1.17 Write Adapter FIFO Buffer (Operation Code 1C)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to will be transferred to the host adapter's FIFO buffer using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the indicated buffer area to the host adapter, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Read Adapter FIFO Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte
Byte 1 Buffer area address
Byte 2 Buffer area address, Least significant byte

5.1.1.18 Read Adapter FIFO Buffer (Operation Code 1D)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to will be used as a buffer to receive 54 bytes of information transferred from the host adapter's FIFO to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the FIFO to the indicated buffer area, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Write Adapter FIFO Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte
Byte 1 Buffer area address
Byte 2 Buffer area address, Least significant byte

5.1.1.19 ECHO Command Data (Operation Code 1F)

This command is used to test the Command / Data Out Port, the Data In Port, and the associated control bits in the other I/O Ports. After receiving this command, the host adapter expects one byte of outbound information to be transferred through the Command / Data Out Port. The host adapter then sends (Echos) the same data value back to the host through the Data In Port. After the host has read the data value provided on the Data In Port, the host adapter will generate the HACC interrupt to indicate normal command completion.

Byte 0, Out Outbound Echo Value

Byte 0, In Returned Echo Value

5.2 MAILBOX OVERVIEW

The AHA-1540A/1542A uses a mailbox architecture for task communication between the host and the host adapter when executing SCSI commands. This allows the host adapter to perform multithreaded operations with a minimum of host intervention. The mailboxes are located in main system memory. Each mailbox entry is four bytes long. At power up, the host issues an initialization command to inform the host of the mailbox location. There are always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). The MBIs are located immediately after the MBOs. Initiator operations and target operations use the same mailboxes. Both initiator and target operations may be in process at the same time. A typical mailbox structure is shown below.

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example, there are four MBOs and four MBIs. The Mailbox Count in the Mailbox Initialization command was set to four. The base address is the address specified by the Mailbox Address field.

Note: The Adaptec BIOS initializes the AT DMA controller to accommodate Bus Master DMA. If the host adapter BIOS is removed or disabled, the host DMA controller must be initialized, via software, for Bus Master DMA operation. See section 5.5.

5.2.1 Mailbox Out Definition

The first byte of each MBO contains the Mailbox status byte. The remaining three bytes contain an address pointer to the first byte of a Command Control Block (CCB). The CCB provides additional task control information. A MBO is free if the first byte is zero. The host can make an entry in any free MBO and indicate that it is filled out or completed by placing the proper MBO command in the first byte of the MBO. After the MBO has been examined by the host adapter and all relevant information obtained by the host adapter, the host adapter sets the MBO command byte back to zero to allow the host to fill it again. For a multitasking operating system, it is desirable that the number of mailboxes be sufficient to allow at least one mailbox for each active independent task or activity.

The MBO format is described in detail below:

Byte 0	MBO Command	This byte specifies the state of the MBO entry.
	Value	Definition
	00H	Mailbox Out is free
	01H	SCSI or Host Adapter command is to be started. CCB pointer indicates location of CCB to be processed.
	02H	SCSI or Host Adapter command is to be aborted. CCB pointer indicates location of CCB to be terminated.
Byte 1	CCB Pointer (MSB)	
Byte 2	CCB Pointer	
Byte 3	CCB Pointer (LSB)	

The use of Mailbox Out (MBO) entries to pass pointers to CCB's is identical for target and initiator modes. The appropriate target mode CCB may be prepared early and posted to the host adapter in preparation for an operation that is expected to happen. If a SCSI operation occurs before the CCB is prepared, the host adapter processes as much of the transaction as possible, then requests a CCB from the host through the MBI. The host is fully responsible for preparing the correct CCB from the information provided through the MBI.

In target mode, one CCB may be presented for each unique combination of LUN, Initiator, and direction. If a second CCB to the same LUN and initiator with the same direction bit is sent to the AHA-1540A/1542A, the CCB will be returned with a host status of 19H, Duplicate CCB Received.

Initiator type CCB's may be queued for an LUN and Target. The host adapter will always search for new MBO entries in a round-robin order, beginning with the entry after the last MBO entry that was processed. By always placing the MBO entries in the MBO area consecutively, the host can assure that the SCSI commands will be started with a minimum scan overhead. Initiator CCB queueing must be used with caution, since under some circumstances it is possible for CCB's to be executed out of order.

If the Mailbox Out Available Interrupt is enabled by execution of Adapter Command 05 (Enable Mailbox Out Available Interrupt), the host adapter will take one of the following actions after each MBO entry is freed by the host adapter:

1) If the Any Interrupt bit in the Interrupt Flag Port is zero, indicating that there are no interrupts pending, the host adapter will set the Mailbox Out Available Interrupt and the Any Interrupt bit and indicate a hardware interrupt to the host.

2) If the Mailbox Out Available Interrupt has been set to one by the previous clearing of a Mailbox Out entry and the interrupt has not yet been cleared by the host, the host adapter will not change the MBOA interrupt bit and will continue to scan for other stored MBO entries.

3) If interrupts other than the Mailbox Out Available Interrupt are pending, the host adapter will wait for the pending interrupts to be cleared before setting the Mailbox Out Available Interrupt. This guarantees that the MBO Available Interrupt will not be cleared accidentally by clearing another interrupt.

5.2.2 Mailbox In Definition

The Mailbox In entries are used to pass completion information concerning a task from the host adapter to the host. In addition, requests for Target Mode CCB's are passed to the host using MBI entries. The first byte of each MBI contains the MBI Status byte, summarizing the type of information being passed from the host adapter to the host. The remaining three bytes contain specialized information that provides more detail about the information. In the case of a CCB Completed MBI, the bytes contain a pointer to the completed CCB. In the case of a CCB Required MBI, the bytes contain the information necessary for the host to prepare an appropriate CCB. Only those MBI's with a MBI Status that is non-zero have information for the host. When the host returns the MBI Status byte to zero, the MBI Free state, the host adapter is allowed to place a new set of information in the MBI entry.

When a SCSI command completes or if a new CCB is required, the host adapter scans the first byte of an MBI entry to find a free mailbox. If one is found, the host adapter will update the MBI's status byte with a non zero value and update the following bytes with the appropriate required pointers or parameters. The valid MBI formats are defined below:

Mailbox In Format for CCB Complete

Byte 0	MBI Status	This byte specifies the state of the MBI entry.
	Value	Definition
	00H	Mailbox In is free
	01H	CCB completed without error. CCB pointer indicates location of successfully completed CCB.
	02H	CCB aborted by host. CCB pointer indicates location of CCB that was aborted.
	03H	Aborted CCB not found. CCB pointer indicates the supposed location of the CCB that was to have been aborted. It is likely that the CCB was already presented to the host before the Abort CCB MBO entry was completed.
	04H	CCB Completed with Error. The CCB fields indicate the details of the error condition. This code allows normal CCB completion to be processed without bothering to examine the completion codes in the CCB.
Byte 1	CCB Pointer (MSB)	
Byte 2	CCB Pointer	
Byte 3	CCB Pointer (LSB)	

Mailbox In Format for CCB Required

Byte 0	MBI Status	This byte specifies the state of the MBI entry.
	Value	Definition
	10H	SCSI Target Command received with no CCB available. The host must prepare an appropriate CCB and place it in the MBO to complete the SCSI command. The remaining three bytes of the MBI specify the information necessary to prepare a SCSI command.
Byte 1	Initiator and LUN	
	Bit 7-5	Binary address of initiator that selected the host adapter in Target Mode.
	Bit 4	The SCSI Target Command received was a RECEIVE command. A CCB must be prepared to transmit data to the Initiator.
	Bit 3	The SCSI Target Command received was a SEND command. A CCB must be prepared to transmit data from the Initiator.
	Bits 2-0	Binary address of the logical unit of the Target Mode host adapter that was addressed by the Initiator.
Byte 2-3	Data Length	The high order two bytes of the data length specified in the SEND or the RECEIVE command. A CCB must be prepared to transmit this amount of data plus up to 256 more bytes. It is assumed that the data fields are self-defining or of a known length in such protocols.

The CCB Required Mailbox In entries are only generated when a command has been received by the host adapter in target mode. For the CCB Required Mailbox In entries, byte 0 takes on a distinctive value of 10H, indicating both that the MBI entry is filled and that the MBI entry is being presented to request a CCB appropriate to service a SCSI transaction for which no CCB was available. The host adapter will have disconnected on the SCSI after receiving the initiator and LU addresses and after having received either a SCSI SEND or a RECEIVE command. If the LU address is enabled by the Logical Unit Mask, the MBI will provide the addresses in bits 7-5 and bits 2-0 and will indicate by setting either bit 3 or bit 4 that a SCSI SEND or RECEIVE command was accepted from the initiator. The host system is then expected to prepare a CCB suitable for processing the Send or Receive command. The information in bytes 2 and 3 is a copy of bytes 2 and 3 of the Send or Receive command CDB. This provides the host an approximation of the length of the requested data transfer. This length is used by the host to allocate the correct amount of buffer to accept data in a SEND command or to control the maximum amount of data that can be transferred in a RECEIVE command. If the LU address received is disabled, no MBI will be presented and a check condition will be posted to the Initiator. A subsequent REQUEST SENSE command will recover an Invalid LUN error indication.

After each Mailbox In entry is stored by the host adapter, it will indicate that Mailbox In scanning must be performed in the following manner:

1) If the Any Interrupt bit is not set to one in the Interrupt Flag port, indicating that no interrupts are pending, the host adapter will set the Mailbox In Full interrupt bit, the Any Interrupt bit, and raise the hardware interrupt line to indicate that there is at least one Mailbox In entry to be examined by the host system.

2) If the Mailbox In Full interrupt bit has already been set to indicate that an entry was made in the Mailbox In area and if that interrupt has not yet been cleared by the host, no further notification is provided by the host adapter.

3) If interrupts other than the Mailbox In Full interrupt are pending, the host adapter will wait for all pending interrupts to be cleared before setting the Mailbox In Full interrupt.

Note that careful host Target Mode software design is necessary to prevent ambiguity in the notification process. If a CCB was just prepared but the MBO has not yet been searched by the host adapter at the time the MBI entry is made to the host, the host may choose to examine the MBI entry and not act on it, having already provided the needed CCB. The host should also examine the entire MBI space to be sure that a previously supplied CCB which should have been able to service the notification MBI entry was not already used for a previous operation that had been posted by the host adapter but not yet serviced by the host. Proper care in host system design will prevent these overlapping operations from becoming a problem.

5.3 COMMAND BLOCK DEFINITION

The CCB specifies detailed information about a SCSI command. The format of a CCB is shown below. Each of the fields is separately explained following the table.

COMMAND CONTROL BLOCK FORMAT

Byte 0	Command Control Block Operation Code	
	Value	Definition
	00H	SCSI Initiator Command
	01H	Target Mode Command
	02H	SCSI Initiator Command with Scatter/Gather
	81H	Bus Device Reset
Byte 1	Address and Direction Control	
	Bits 7-5	CCB Op Code = 00, 02: SCSI Target Id CCB Op Code = 01: SCSI Initiator Id
	Bit 4	Outbound data transfer, length is checked.
	Bit 3	Inbound data transfer, length is checked.
	Bit 2-0	Logical Unit Number
Byte 2	SCSI Command Length	
Byte 3	Request Sense Allocation Length/Disable Auto Sense	
Byte 4-7	Data Length (Byte 4 most significant)	
Byte 7-9	Data Pointer (Byte 7 most significant)	
Byte 10-12	Link Pointer (Byte 10 most significant)	
Byte 13	Command Linking Identifier	
Byte 14	Host Adapter Status (HASTAT)	
Byte 15	Target Device Status (TARSTAT)	
Byte 16-17	Reserved (00)	
Byte 18-n	SCSI Command Descriptor Block (Length specified by byte 2)	
Byte n-m	Reserved for REQUEST SENSE information bytes (Length of reserved space in byte 3)	

The standard format of the Command Control Block is shown in the following diagram:

Byte 0	Command Control Block Opcode			
+1	Tar/Init	Data Out	Data In	LUN
+2	SCSI Command Length = m			
+3	Request Sense Allocation			
+4	Data Length (MSB,MID,LSB)			
+7	Data Pointer (MSB,MID,LSB)			
+10	Link Pointer (MSB,MID,LSB)			
+13	Command Link ID			
+14	Host Status			
+15	Target Status			
+16	Reserved			
+17	Reserved			
+18	SCSI Command Bytes (m Bytes)			
18 + m	Allocated for Sense Data (n Bytes)			

The bytes of the CCB are defined further below:

Byte 0: Command Control Block Operation Codes

The AHA-1540A/1542A supports four CCB Operation Codes. The valid command values are shown below:

00	SCSI Initiator Command Control Block
01	SCSI Target Command Control Block
02	SCSI Initiator Command Control Block with Scatter/Gather
81	SCSI Bus Device Reset

If the Operation Code value is 00H, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed Target / LUN. The other fields of the CCB support the required Initiator functions of the AHA-1540A/1542A.

If the Operation Code value is 01H, the CCB is intended to service a SEND or RECEIVE command sent to the host adapter as a target from another initiator. The values in the other fields are used to service the Target Mode operation. If an Operation Code of 01H is specified to a host adapter that has not had its Target Mode enabled, the host adapter returns a Host Status indication of 18H, Invalid CCB Parameter.

If the Operation Code value is 02H, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed Target / LUN. The definition of the Data Length and the Data Pointer is modified to support the Scatter/Gather function. Refer to section 5.2.4.

If the value is 81(hex) a Bus Device Reset message will be sent to the addressed target. This command forces the host adapter to abort all outstanding tasks against the selected target. All remaining CCB Bytes are ignored. The host adapter will generate a Bus Device Reset message out to the specified target.

Any other command value generates a Host Adapter Detected Error (Host Status byte of 16H).

Byte 1: Address and Control Byte

This byte identifies the address of the devices that will be serviced and provides information about the expected direction of data flow.

If the CCB is an Initiator CCB, this byte identifies the target SCSI device in bits 7,6, and 5. If the CCB is a Target CCB, the byte identifies the initiator which the CCB will serve.

Bits 4 and 3 are set to determine the direction of data transfer. For an Initiator CCB, if neither bit is set, the direction of data transfer will be established by the SCSI command being executed. For a Target CCB, if neither bit is set or both bits are set, the CCB will be returned with an indication of Invalid CCB Parameters (18H) in the Host Status field, since each Target CCB must be identified as to whether it will service a SEND or a RECEIVE command. If both bits are set for an initiator CCB, the command must perform no data transfer. If only bit 3 is active, the data transfer will be to the host adapter and from the external SCSI device. If the CCB is a target CCB, the data transfer will be required to be a Data Out phase, while if the CCB is an initiator CCB, the data transfer will be required to be a Data In phase. If only bit 4 is active, the data transfer will be from the host adapter and to the external SCSI device. If the CCB is a target CCB, the data transfer must be a Data In phase, while if the CCB is an initiator CCB, the data transfer will be a Data Out phase.

If bits 3 or 4 are set for an Initiator CCB, the data length will be checked. If the amount of data transferred exceeds the specified amount, the CCB Host Status field will contain an indication of Data Over/Under Run (12H). For a Processor Target mode CCB, the handling of incorrect lengths is described in Section 8.2.4.

If a data underrun/overrun condition occurs for an operation that accesses the drive's media (READ/WRITE, EXTENDED READ/WRITE, WRITE AND VERIFY) and the direction bits are set to zero, the host adapter will complete the operation without error. However, some or all of the data specified by the host may not be transferred.

CAUTION: THE APPROPRIATE DIRECTION BIT SHOULD BE SET FOR ALL OPERATIONS THAT ACCESS THE DRIVE'S MEDIA.

This enables the host adapter to check the length of the data transfer and if a data underrun/overrun condition occurs, the CCB will be returned with an indication of Data Underrun/Overrun (12H) in the Host Status field. For operations that do not access the drive's media, the direction bits should be set to zero unless transfer length checking is desired. Setting both direction bits to one should be used only when no data transfer is expected or suppression of data transfer is desired for READ operations.

If the CCB is an initiator CCB, bits 2,1, and 0 define the target Logical Unit which will be addressed. If the target accepts an IDENTIFY message out, the value in bits 2,1, and 0 will be provided in the LUN field of the message byte. The LUN field in the SCSI Command Descriptor Block (CDB) is expected to be zero. If the target does not accept an IDENTIFY message out, the LUN field in the SCSI CDB must contain the correct Logical Unit address. SCSI devices with conformance level 2, including Common Command Set (CCS) disk drives and all SCSI-2 devices will always accept the IDENTIFY message out. The few SCSI devices not meeting those requirements must be examined on a case by case basis to determine whether the Logical Unit Address should be placed in CCB Byte 1 or in the CDB.

Byte 2: SCSI Command Length

This byte establishes the length, in bytes, of the SCSI Command Descriptor Block.

Byte 3: Request Sense Allocation Length

When a SCSI device terminates an operation with CHECK CONDITION status, it means that the device has error or status information as a result of execution of the operation. The SCSI specification indicates that a REQUEST SENSE command must be executed before any other command is executed in order for the host initiator to be sure of obtaining the error information. Since the AHA-154XA host adapter has the capability of queueing commands for execution, the host adapter itself must take charge of generating the Request Sense command. The automatic generation of Request Sense is inconvenient for some specialized operating systems, so the function can be disabled by installation of a jumper in J9 (See section 3.3.11). If the jumper is not installed, the function can also be disabled by specifying a value of 01H for the Request Sense Allocation Length.

This byte indicates the length, in bytes, of the area reserved for information that may be obtained by a REQUEST SENSE command. A value of 00H indicates that an allocation length of 14 bytes is to be used, sufficient to capture the sense key and error code of all normal extended sense type devices. A value of 01H requests that no automatic REQUEST SENSE be executed. The values from 02H to 07H are reserved. Values from 08H to FFH are valid allocation lengths. The value is used to notify the host adapter that the specified number of bytes have been reserved at the end of the CCB to receive possible Request Sense data bytes. The REQUEST SENSE also uses the indicated allocation length as its byte count in the Command Descriptor Block generated by the host adapter.

If an operation that treats the AHA-1540A/1542A as a Target Mode device fails and presents a Check Condition status byte, the Initiator should return a REQUEST SENSE command. The AHA-1540A/1542A will return appropriate sense information in response to the command. If the command that originally failed was a SEND or a RECEIVE command, the same REQUEST SENSE information bytes that will later be sent to the Initiator are also sent to the host when the CCB is returned. The sense information is placed in the specified Request Sense Allocation area with a length not exceeding the Request Sense Allocation Length.

Bytes 4, 5, 6: Data Length

These bytes determine the length, in bytes, of the data transfer. CCB host adapter error 12(hex) is posted if a data over run occurs.

If the CCB specifies a Scatter/Gather operation, the Data Length field contains the total number of bytes in the Data Segment List.

Bytes 7, 8, 9 : Data Pointer

These bytes specify the real address of the first byte of the data area to be used during the data phase of the SCSI command.

If the CCB specifies a Scatter/Gather operation, the Data Pointer field contains the pointer to the first byte of the Data Segment List.

Bytes 10, 11, 12: Link Pointer

These bytes are used when a SCSI command contains a LINK or LINK WITH TAG bit in the command. When a Linked command is completed, the host adapter will use the contents of this field as a pointer to the next CCB to execute. If the Linked Flag bit is set, an interrupt will be generated before the next command is started. A completed CCB is always reported back in an MBI, but MBIF interrupts are only reported if the linked set of commands is finished or if a Link with Flag message is presented. There must be enough MBI entries to receive the entire set of linked commands.

Target Mode does not support the linking function.

Byte 13 : Command Link ID

This byte is used in conjunction with linked commands. It is set by the host to identify commands in a command chain.

Linking is not supported in Target Mode.

Byte 14 : Host Status

This byte is used to report the host adapter status (HASTAT).

HASTAT has the following definitions:

00 H	No host adapter detected error The CCB was completed normally.
0A H	Linked command complete without error The SCSI command completed and linked normally.
0B H	Linked command complete without error, interrupt generated. The SCSI command completed and linked with a LINKED COMMAND COMPLETE WITH FLAG message.
11 H	Selection time out The initiator selection or target reselection was not complete within the Set SCSI Selection Time-out period.
12 H	Data over run/Under run The target attempted to transfer more data than was allocated by the Data Length field or the sum of the Scatter / Gather Data Length fields.
13 H	Unexpected bus free The target dropped the SCSI BSY at an unexpected time.
14 H	Target bus phase sequence failure An invalid bus phase or bus phase sequence was requested by the target. The host adapter will generate a SCSI Reset Condition, notifying the host with a SCRD interrupt.
15 H	MBO command was not 00, 01, or 02 The first byte of the MBO command was invalid. This usually indicates a software failure.
16 H	Invalid CCB Operation Code The first byte of the CCB was invalid. This usually indicates a software failure.
17 H	Linked CCB does not have the same LUN A subsequent CCB of a set of linked CCB's does not specify the same logical unit number as the first.
18 H	Invalid Target Direction received from Host The direction of a Target Mode CCB was invalid.
19 H	Duplicate CCB Received in Target Mode More than once CCB was received to service data transfer between the same target LUN and initiator SCSI ID in the same direction.
1A H	Invalid CCB or Segment List Parameter A segment list with a zero length segment or invalid segment list boundaries was received. A CCB parameter was invalid.

Byte 15: Target Status

For an initiator CCB, this byte is used to return the SCSI status byte sent to the host adapter from the initiator. If a SCSI command returns with BUSY status, the normal recovery process is to execute the command again. The AHA-154XA takes that burden off the host and periodically restarts the command automatically until the command completes with a status other than Busy.

For a target mode CCB, this byte is used to indicate to the host what status the host adapter returned to the initiator.

Target Status may have the following values in target mode

00 -- Good Status
02 -- Check Status (See REQUEST SENSE byte area)
08 -- LUN Busy

Byte 16: Reserved (must be 0)

Byte 17: Reserved (must be 0)

Byte 18: n: SCSI Command Descriptor Block

This field holds the SCSI Command Descriptor Block (CDB) as described in the SCSI specification. The length of this command is described in byte 02. For initiator mode CCB's, the CDB provided by the host is transmitted to the target. For target mode CCB's, the CDB provided from the initiator is returned to the host in this space.

Byte 18+n - 18+n+m : Allocated for Sense Data

If a Check Status condition is detected by the AHA-154XA as it completes an operation on the SCSI bus, the host adapter automatically executes a REQUEST SENSE command with the data length specified by Request Sense Allocation Length. The actual bytes returned, up to the maximum indicated by the Request Sense Allocation Length, are placed in the area Allocated for Sense Data. If the Request Sense Allocation Length was 01h, no REQUEST SENSE command is executed.

If a check condition is detected by the AHA-154XA while it is operating in Processor Target Mode, the same information that will later be recovered by the initiator that received the Check Status is also placed in the area Allocated for Sense Data so that the host processor is also aware of the failure.

5.3.1 SCATTER/GATHER LIST DEFINITION

Using the normal CCB Operation Codes of 00 and 01 (SCSI Initiator and SCSI Target CCB's), the CCB itself contains a pointer to the first byte of a contiguous area of data of a specified length. The direction of transfer with respect to the data area and the checking of the length of the data transfer to the data area are both managed by the AHA-1540A/1542A according to the requirements of the particular mode and control bit set-up.

Using the Scatter/gather Operation Code of 02, the CCB instead contains a pointer to a list of data segments and an indication of the length of the list of data segments. The data segment list contains pointers to the actual location in host memory of the data segments to be transferred as well as a precise indication of the length of each data segment. Each data segment list entry contains a three-byte pointer to the location of a data segment and three-byte length indicator telling how long that particular data segment shall be. The data segment list is arranged in the order in which data will be gathered or distributed, the first pointer in the list being used first.

A typical data segment list is shown in the following table. The data segment list describes the distribution of 4096 bytes distributed in four separate locations within the memory. The beginning of the data segment list is indicated by the data segment list pointer. The length of the data segment list (24 bytes) will be contained in the data segment list length field of the CCB.

	3 bytes	3 bytes
	(MSB) (LSB)	(MSB) (LSB)
Data Segment List Pointer →	Segment 0 L = 1024	Data Segment 0 Pointer
	Segment 1 L = 2	Data Segment 1 Pointer
	Segment 2 L= 2046	Data Segment 2 Pointer
	Segment 3 L= 1024	Data Segment 3 Pointer

A data segment list can have from one to sixteen segments. A list with 0 segments or a list with more than 16 segments causes an Invalid Segment List error to be posted in the host status field.

The AHA-154XA has certain constraints in the data segment address boundaries and lengths that are allowed. If these boundaries are violated, an Invalid Segment List error will be posted in the host status field of the CCB. The simplest way to assure that these boundaries are not violated is to require all boundaries between segments to be on even word boundaries. The first segment may begin on any boundary and the last segment may end on any boundary. All segments but the first and last should have even byte counts.

The actual boundary limitation is somewhat less restrictive. If the binary values of the starting address of a segment, the byte count of that segment, and the starting address of the next segment are all exclusive OR'd together, and the result of that exclusive or is an even number, the boundary between those two segments is valid. Another way to express the limitation is to require that the ending boundary of one segment must be the same as the beginning boundary of the next segment. If a segment ends on a word boundary, the next segment must begin on a word boundary. Similarly, if a segment ends on an odd-byte boundary, the next segment must begin on an odd-byte boundary.

5.4 DESCRIPTION OF OPERATION

This section describes the interface operations required to invoke the desired SCSI behavior. The AHA-1540A/1542A must be properly initialized before any of these operations can be performed.

After system initialization is done, the I/O Command Port initialization commands must be executed. The Mailbox Initialization command must be executed to assign the Mailbox area. The Enable Target Mode command may optionally be executed if Target Mode is to be allowed.

5.4.1 Execution of Initiator Mode operations

To begin an Initiator Mode SCSI command, the host first allocates a data buffer area. A CCB is then created to perform the desired operation to the correct peripheral device and a pointer to the data buffer area is placed in the CCB. Once the CCB is completely defined, the host places a pointer to the CCB in an empty MBO location, places an MBO full status in the MBO status byte, and transmits a Start SCSI Command to the I/O Command Port. If it is not already scanning the MBO for an active MBO entry, the Start SCSI Command to the I/O Port causes the host adapter to begin scanning for such an entry.

After finding an active MBO entry, the AHA-1540A/1542A copies the MBO Command field contents and CCB pointer into its internal RAM and clears the MBO Command byte, freeing the mailbox. Up to 16 initiator CCBs and 16 target CCBs can be stored in the host adapter's internal RAM concurrently. The AHA-1540A/1542A maximizes the SCSI bus utilization by starting the next available CCB as soon as the bus is free. Disconnection and reconnection on the bus are automatically taken care of by the AHA-1540A/1542A. As the host adapter starts the SCSI operation, it will first determine if the addressed target/LUN is busy. If the target/LUN is busy, then the command will be placed in the task queue to be tried again later.

Commands are removed from the queue in the order that they were received, establishing a (FIFO) first in first out command execution order. Of course, the order of task completion may vary due to the different amounts of time required to process and complete different commands. If the target/LUN is not busy, the new command is started at the next bus free phase. If BUSY status is received by the AHA-1540A/1542A, the CCB is placed at the end of the FIFO queue to be restarted later.

If a CHECK CONDITION status is received from the target, the AHA-1540A/1542A will issue a Request Sense command to get the sense data. The sense data is stored in the CCB after the SCSI command data. The driver software must reserve the allocated number of bytes at the end of the CCB to hold the sense data which is returned as result of a receiving a check status. Automatic Request Sense can be optionally disabled by jumpers or by using the CCB.

If the MBO Command is to abort a SCSI command, the host adapter first searches the active and queued CCBs. If the CCB is found, the task is aborted at the earliest possible moment and an MBI entry is made to indicate that the CCBs execution was successfully terminated. If the CCB is not found among the active or queued CCBs, the AHA-1540A/1542A completes the command and reports that fact in the MBI Status byte. The CCB may not be found because it has previously been aborted, because an intervening reset occurred, or because the CCB was already finished normally and returned.

The AHA-1540A/1542A scans the MBOs in a round robin fashion. This is to ensure that all of the mailboxes will be scanned with equal probability. A host can minimize the AHA-1540A/1542A MBO scan time by using MBO's sequentially.

When executing a START SCSI command, the AHA-1540A/1542A does not verify that the new CCB resides in an unused memory area. Therefore, the host must not reuse a CCB location until it has been returned through a Mailbox In entry and the host has examined all the pertinent information in the CCB. CCB addresses are used by the AHA-1540A/1542A as task identifiers.

5.4.2 Execution of Target Mode Operations

5.4.2.1 Target Mode with a Prepared CCB

Typical target operation is managed in the following way by the host software. After power-on initialization is complete, the host sends an Enable Target Mode command to the host adapter to enable Processor Target mode. After that, the host, from previous configuration knowledge, generates a pair of CCB's for each likely initiator and for each LUN supported by the host. One CCB is for outbound data from the initiator using the SEND command, while the other is for inbound data from the target to the initiator using the RECEIVE command. The SEND command CCB defines a data buffer for the expected network type command from the initiator. The RECEIVE command CCB defines a set of data which is known and expected by the initiator, typically a welcome or configuration type message packet. The host adapter tests to be sure that duplicate CCBs are not provided by the host.

As the initiator finishes its initialization procedure, it requests availability and configuration information using the TEST UNIT READY, REQUEST SENSE, and INQUIRY commands. Finally, it may choose to address SEND and RECEIVE commands to the targets it has located to transmit or request information packets.

When the initiator executes a SEND or a RECEIVE command, the target accepts the selection on the SCSI bus, accepts the command from the initiator, and executes the proper data transfer to or from the area specified by the proper CCB. When all SCSI activity is finished successfully, the CCB is posted back to the host program by an entry in the MBI. The host adapter updates the CCB byte count and CDB field contents to correctly reflect the operation performed. The host is notified that there is an entry in the MBI by an interrupt from the host adapter. The host then prepares a new CCB to control the target's next activity expected from the initiator.

5.4.2.2 Target Mode without a Prepared CCB

Alternatively, the processor type device may be addressed by an initiator when no CCB has yet been prepared for use by the host adapter. If the host adapter command enabling target mode has not yet been executed, the host adapter will act like any initiator. It will not accept any selection sequence and any attempts to select it by its target ID will cause the initiator to detect a selection time-out.

If the host adapter has been enabled as a Processor Target by a host adapter command, any selection to the host adapter's target address will be accepted. The availability commands and identification commands (TEST UNIT READY, REQUEST SENSE, and INQUIRY) will be executed completely and normally. If a SEND or RECEIVE command is received and if a CCB is not active, either because the host has not completed its program initialization or because the host has not finished analyzing the results of previous data transfers and has not generated a new CCB, the Processor Target will accept the selection, obtain the IDENTIFY Message Out to determine what Logical Unit has been selected, request the CDB from the SCSI, and then disconnect. The CDB will be partially interpreted so that the proper MBI can be generated to notify the host that a new CCB with a certain address, direction, and data length must be generated. When the new CCB is passed to the host adapter by an MBO entry, the CCB is filled up with the command information, the SCSI is reconnected, and the command is completed as described above.

5.5 DMA CHANNEL INITIALIZATION WITH THE HOST ADAPTER BIOS DISABLED

The DMA circuitry must be set to a special state to allow the Bus Master operation of the AHA-154XA to operate correctly. This state is normally established by the BIOS during initialization so that no other activity is required. If a DMA channel other than the default channel is being used or if the DMA channel is manipulated by other programs, the circuitry must be initialized in the following way before the AHA-154XA can be used.

For the DMA channel being used, 2 bytes of data must be written to the DMA controller port specified to initialize the Host DMA controller for Bus Master DMA operation. The following table specifies these values in HEX.

DMA Channel	DMA Controller Port	Data
0	0B	0C
	0A	00
5	D6	C1
	D4	01
6	D6	C2
	D4	02
7	D6	C3
	D4	03

5.6 INTERRUPT INITIALIZATION

This setup procedure is normally completed by the BIOS during initialization so that no other activity is required. If modifications to the interrupt handler are required, this information together with the programming information provided by the host system should be sufficient to properly set up the interrupt vectors.

The host adapter will drive one of several interrupts in the AT system. The particular interrupt used must be set up on power up initialization and be properly managed during usage. The AT interrupts of interest to the host adapter driver along with their corresponding vector locations are summarized below. All these interrupst are handled by a slave interrupt controller. The master controller handles all system interrupts such as keyboard, timer, etc. and is assumed to be correctly initialized to allow interrupts by the slave controller. Upon receiving an interrupt, the processor will be vectored to the contents of the corresponding vector location.

Hardware interrupt		Software interrupt vector location (hex)
int 9	--	INT71
int 10	--	INT72
int 11	--	INT73
int 12	--	INT74
int 13	--	INT76
int 14	--	INT77
int 15	--	INT78

The interrupt is initialized by clearing the corresponding interrupt mask bit in the slave controller. The mask register is a read/write register, and only the bit of interest should be cleared. The port address is A1 hex, and bit definitions follow.

Interrupt mask bit definition (port address A1 hex)

bit 0 -- int 8
bit 1 -- int 9
bit 2 -- int 10
bit 3 -- int 11
bit 4 -- int 12
bit 5 -- int 13
bit 6 -- int 14
bit 7 -- int 15

Section Six Single-Threaded Software Interface

6.1 SINGLE THREADED BIOS COMMAND INTERFACE

The AHA-1540A/1542A BIOS resides on the host adapter board. It provides support for up to two SCSI Common Command Set disk drives under DOS. If SCSI devices other than CCS disk drives or if support for more than two disk drives is required under DOS, the Adaptec DOS Driver, ASW-1110 must be used. The BIOS provides a very simple single threaded capability that does not make use of the Mailbox Interface used by more sophisticated programs. This capability allows the host system to boot from a SCSI disk drive and to support standard DOS calls from any standard program.

The BIOS communicates with the host adapter through a special set of commands passed under the I/O Command Port command 02H (Start Bios Command). These commands are not available to any programs except the Adaptec BIOS. The Adaptec BIOS provides a standard BIOS interface. The DOS interface to the standard BIOS is described in this section.

On an AT compatible machine, up to two hard disks are supported by the BIOS resident on the mother board. Any other drives must be managed through the Mailbox Interface using an appropriate driver. The operation of the AHA-1540A/1542A BIOS on attached SCSI devices depends on the number of standard hard disks installed directly on the system.

No standard hard disks installed:

> In this case, two SCSI drives can be supported by the AHA-1540A/1542A BIOS. SCSI Device 0 Logical Unit Number 0 is designated as drive 0 (Drive C:). Either SCSI Device 0 LUN 1 or SCSI Device 1 LUN 0 may be designated as drive 1 (Drive D:). This set of addresses allows the use of two drives with either embedded controllers or bridge controllers. Booting is only performed from SCSI Device 0 LUN 0. When no standard hard disks are installed, the AHA-1540A/1542A BIOS is operating in non-concurrent mode.

One standard hard disk installed:

> In this case, the internally installed hard disk is designated as drive 0 (Drive C:). SCSI Device 0 LUN 0 is designated as drive 1 (Drive D:). Booting is performed from the internally installed hard disk. This mode of operation is called concurrent operation, indicating that the internally installed drive and one SCSI drive can operate together under the BIOS.

Two standard internal hard disks installed:

> In this case, all the disks that can be supported by the BIOS are directly installed. The AHA-1540A/1542A BIOS will not support any SCSI drives. Therefore a device driver will need to be installed to access the SCSI drives.

6.2 BIOS COMMAND EXECUTION USING INTERRUPT 13

On IBM compatible systems, disk I/O requests are passed from the operating system to the BIOS through software interrupt 13H. CPU registers are used to pass information about the desired operation and the associated parameters.

The AHA-1540A/1542A BIOS provides SCSI support by intercepting each interrupt and managing the request according to the drive address. If the drive is a floppy or internally installed fixed disk, the call is managed by the mother board BIOS with no changes. If the selected drive is a SCSI disk drive, the request is handled by the Adaptec BIOS resident on the AHA-1540A/1542A. For concurrent operation, only calls to drive 81H (D:) are handled by the AHA-1540A/1542A BIOS. For nonconcurrent operation, calls to both drive 80H (C:) and 81H (D:) are managed by the AHA-1540A/1542A BIOS.

On each Interrupt 13 call, the correct host microprocessor registers are set by the operating system program to provide the required parameters to both the Adaptec BIOS and the mother board BIOS. Most commands use the registers as indicated in the following table.

Register	Function
AH	BIOS Function Code
AL	Number of Sectors
CH	Low Order Byte of Cylinder Number
CL	Cylinder and Sector Numbers Bits 7,6 High Order Cylinder Bits Bits 5-0 Sector Number
DH	Head Number
DL	Drive Number
ES:BX	Data Buffer Address

6.2.1 Physical to Logical Address Translation

As shown above, the starting sector address for read, write and verify requests is passed as a physical address including a 10 bit Cylinder Number, an 8 bit Head Number, and a 6 bit Sector Number. SCSI devices are addressed by logical block address without regard to the physical layout of the drive. For this reason, all SCSI devices are defined as drives with 64 heads and 32 sectors per track and with the appropriate number of cylinders to provide the full capacity of the drive using this physical to logical translation. The SCSI logical address is formed by the BIOS by concatenating the values as show below:

Cylinder (10 bits) || Head (6 bits) || Sector (5 bits)=SCSI Logical Block Address

6.2.2 BIOS Command Return Codes

The BIOS command, when complete, returns control to the requesting program at the next instruction after the software interrupt. A return code is set in the Carry Flag (CF) and a status code is placed in register AH for examination by the requesting program. The expected return codes placed in the Carry Flag are shown below.

CF Contents at Return	Return Code
CF = 1	Status is non-zero. Unusual condition or error detected.
CF = 0	Status is zero. Normal command completion occurred.

AH Contents at Return	Status of Operation
AH = 00H	No error: The operation completed successfully.
AH = 01H	Invalid Function Request: The operation code or an associated parameter provided by the Interrupt 13 operation was not valid.
AH = 02H	Unable to Read Address Mark: One of the following additional sense codes (SCSI ASC) was presented in the sense information returned by the REQUEST SENSE command: 12H (No AM Found on Data Field) 21H (Illegal Logical Block Address)
AH = 03H	Write Protect Error: Returned SCSI ASC was: 27H (Data Protect)
AH = 04H	Read Error: Returned SCSI ASC during a read operation was: 14H (No Record Found) 16H (Data Sync Error)
AH = 10H	Uncorrectable ECC Error in Data: Returned SCSI ASC during a read operation was: 10H (ID ECC Error) 11H (Unrecovered Read Error)
AH = 11H	ECC Corrected Data Error: Returned SCSI ASC during a read operation was: 17H (Recovered Read Error w/o ECC) 18H (Recovered Read Error w/ ECC)

AH = 20H	General Controller Failure: A host adapter detected failure occurred or one of the following SCSI ASC's was returned: 01H 08H 40H 46H 03H 09H 41H 47H 05H 1BH 42H 48H 06H 1CH 43H 49H 07H 1DH 44H
AH = 40H	Seek Operation Failed: Returned SCSI ASC was: 15H (Seek Positioning Error) 02H (No Seek Complete)
AH = 80H	Selection Time-out: A host adapter does not respond to BIOS.
AH = AAH	Device Not Ready: Returned SCSI ASC was: 04H (LUN Not Ready) 28H (Unit Attention, Ready) 29H (Unit Attention, Power On) 2AH (Unit Attention, Mode Select Change)
AH = BBH	Unknown Target Sense Error Occurred: A SCSI ASC other than those specified above was returned from the selected SCSI device.
AH = CCH	Write Error: Not Returned
AH = FFH	Sense Operation Failed: BIOS unable to retrieve sense information from target.

6.3 BIOS DISK COMMANDS

The commands that can be accepted from the operating system by the BIOS include all those commands required for normal DOS operation, for booting of the DOS operating system, for the booting of other operating systems, and for basic maintenance and verification of normal disk operation. The command set is summarized in the following table and each command is described in more detail in the sections following.

AH Register	Meaning
00 H	Reset Disk System
01 H	Read Status of Last Operation
02 H	Read Desired Sectors into Memory
03 H	Write Desired Sectors from Memory
04 H	Verify Desired Sectors
06 H	Identify SCSI Devices
08 H	Read Drive Parameters
09 H	Initialize Drive Pair Characteristics
0C H	Seek
0D H	Alternate Disk Reset
10 H	Test Drive Ready
11 H	Recalibrate
15 H	Read DASD Type

The Format commands (AH = 05, 06, 07, and 1AH) are not supported by the AHA-1540A/1542A BIOS. The format operation is performed under a special format utility installed in ROM and initiated through the DEBUG program.

The Diagnostic Reserved commands (AH = 0A, 0B, 0E, 0F, 12, and 14H) are not supported by the AHA-1540A/1542A BIOS.

The Park Heads command (AH = 19H) is not supported by the AHA-1540A/1542A BIOS.

The Reserved for Diskette commands (AH = 16, 17, 18) and the commands from 1BH up to FFH are not supported by the AHA-1540A/1542A BIOS. Any attempt to execute any of these unsupported commands will be ended by the BIOS and an error code of 01H (Invalid Function Request) will be returned in the AH register.

6.3.1 Reset Disk System

The BIOS is requested to reset the disk subsystem. A SCSI Reset operation is performed on the SCSI bus if the bus is busy at the time the Reset Disk System command is received by the host adapter. No other SCSI or host adapter activity occurs. The BIOS command is then passed on to the standard BIOS so that any internally installed hard disks and floppy disk devices can also be reset. If the BIOS is operating concurrently with an internally installed hard disk, the drive number is decremented by the AHA-1540A/1542A BIOS so that the standard BIOS does not attempt to reset the drive that is not installed.

Input Parameters: AH = 00H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.2 Read Status of Last Operation

The status of the last operation performed to the specified disk is returned. No SCSI activity occurs. The disk status is reset to zero.

Input Parameters: AH = 01H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.3 Read Desired Sectors Into Memory

The sectors requested by the parameters are read from the disk to the system memory. The SCSI command is executed as a READ (EXTENDED) command (SCSI Operation Code 28H). If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time. If a 11 Error (ECC Corrected Data Error) is returned, the data returned has been corrected and may be used with confidence.

Input Parameters:
AH = 02H
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder and Sector
AL = Number of Sectors to Read
ES:BX = Address of buffer area

Output Parameters:
AH = Status of Operation
CF = Return Code

6.3.4 Write Desired Sectors from Memory

The sectors requested by the parameters are written from the system memory to the indicated disk. The SCSI command is executed as a WRITE (EXTENDED) command (SCSI Operation Code 2AH). If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time.

Input Parameters:
AH = 03H
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder and Sector
AL = Number of Sectors to Write
ES:BX = Address of buffer area

Output Parameters:
AH = Status of Operation
CF = Return Code

6.3.5 Verify Desired Sectors

The sectors defined by the parameters are verified to be correctly written on the SCSI disk. The SCSI command is executed as a VERIFY command (SCSI Operation 2F) with the Byte Check bit set to zero. If the VERIFY command is not supported by the selected disk, the Verify Desired Sectors will perform a SCSI READ command (SCSI Operation Code 28H) and throw away the received data. If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time.

Input Parameters: AH = 04H
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder and Sector
AL = Number of Sectors to Verify

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.6 Identify SCSI Devices

This is a special AHA-1540A/1542A BIOS call that is used to return the number of the first supported SCSI drive. In the nonconcurrent case (2 SCSI drives), the returned value will be 80H. If only one SCSI drive is installed, the returned value will be 81H.

Input Parameters: AH = 06H

Output Parameters: AH = Status of Operation
AL = First Drive Supported
80H Nonconcurrent operation
81H Concurrent operation
CF = Return Code

6.3.7 Read Drive Parameters

A SCSI READ CAPACITY command is used to determine the maximum logical block of the selected drive. This information is then used to calculate the proper number of cylinders to be returned to the host system. The number of heads returned will always be 64 and the number of sectors per track will always be 32. The number of drives returned will include both internally installed drives and SCSI drives.

Input Parameters: AH = 08H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
DL = Number of BIOS accessible drives attached (1 or 2)
DH = Maximum value for head number (3FH)
CH = Maximum value for Cylinder Range (Low Byte)
CL = Maximum value for Sector, High Cylinder Bits
Bits 7,6 High Order Cylinder Bits
Bits 5-0 Sector Number Maximum Value (20H)
CF = Return Code

6.3.8 Initialize Drive Pair Characteristics

This command performs no operation, since SCSI CCS drives are self configuring.

Input Parameters: AH = 09H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.9 Seek

A seek to the logical block address defined by the physical parameters is performed. The seek is performed using the SEEK (EXTENDED) command (SCSI Operation 2BH). The SEEK commands are not mandatory CCS commands and are not required for proper functioning of SCSI devices. If the addressed disk drive reports an error indicating that the SEEK (EXTENDED) command is not supported, the BIOS command will complete normally anyway. Since the seek operation is performed automatically by a Read or a Write operation, there is no need to generate a separate seek operation to access data.

Input Parameters: AH = 0CH
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder. (Sector bits = 0)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.10 Alternate Disk Reset

The BIOS is requested to reset the disk subsystem. A SCSI Reset operation is performed on the SCSI bus if the bus is busy at the time the Reset Disk System command is received by the host adapter. No other SCSI or host adapter activity occurs. The BIOS command is then passed on to the standard BIOS so that any internally installed hard disks and floppy disk devices can also be reset. If the BIOS is operating concurrently with an internally installed hard disk, the drive number is decremented by the AHA-1540A/1542A BIOS so that the standard BIOS does not attempt to reset the drive that is not installed.

Input Parameters: AH = 00H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.11 Test Drive Ready

The BIOS command determines that the specified drive is available and ready by executing a TEST UNIT READY command (SCSI Operation Code 00H) to the SCSI device. The command may have to be executed a second time if a Unit Attention condition was detected in the first execution of the TEST UNIT READY.

Input Parameters: AH = 10H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.12 Recalibrate

The BIOS command transmits a REZERO UNIT command (SCSI Operation Code 01H) to the specified drive. Since the REZERO UNIT command is not a mandatory command and is not required for proper functioning of the SCSI device, the BIOS command will complete without indicating an error even if the SCSI device indicates that the command is invalid.

Input Parameters: AH = 11H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.13 Read DASD Type

The AHA-1540 BIOS executes this command by performing an INQUIRY (SCSI Operation Code 12H) and a READ CAPACITY (SCSI Operation Code 25H) to the selected SCSI drive. The INQUIRY command is used to verify that the device is a Direct Access Storage Device. The READ CAPACITY is used to determine the number of logical blocks available. A special return format is used to obtain the required information.

Input Parameters: AH = 15H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation (Special Format)

00H	Drive not present or DL invalid
01H	Reserved
02H	Reserved
03H	Fixed Disk installed

CX,DX Number of 512 byte blocks available on disk
CF = Return Code

7.1 PC/AT BIOS

The PC/AT BIOS is provided to allow the user to use the AHA-1540A/1542A in lieu of, or in addition to, a standard PC/AT hard disk controller. This compatibility includes booting from a SCSI device. Hard disk requests are sent to the BIOS via an INT 13 software interrupt. CPU register contents specify the desired I/O function and associated parameters. The BIOS then uses host adapter commands to emulate PC/AT functions. Again, since the mailbox architecture is circumvented, PC/AT BIOS functions run in a single-threaded mode.

The BIOS consists of three major functional components. These are:

1. Initialization Routine
2. System Boot Routine
3. Hard Disk I/O Routine

7.1.1 Initialization

The Initialization routine is called at power-up. This routine performs all of the necessary initialization functions and will display the following message if the system successfully recognizes the AHA-1540A/1542A BIOS.

ADAPTEC AHA-1540A/1542A HOST ADAPTER BIOS
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If any subsequent initialization of the AHA-1540A/1542A fails, the following message is displayed:

HOST ADAPTER NOT FOUND AT PORT 330H.

Otherwise, the AHA-1540A/1542A BIOS chooses a course of action based upon the number and types of hard disks already installed. In each case, the number of hard disks already installed is displayed along with the ID numbers of any SCSI devices that are successfully used by the BIOS.

Possible Messages:

HARD DISK #0 ALREADY INSTALLED.
HARD DISK #1 ALREADY INSTALLED.
HOST ADAPTER DIAGNOSTIC FAILURE.
SCSI DEVICE 0 : 0 NOT FOUND.
USING SCSI DEVICE 0 : 0 AS HARD DISK #0.
USING SCSI DEVICE 0 : 0 AS HARD DISK #1.
USING SCSI DEVICE 0 : 1 AS HARD DISK #1.
USING SCSI DEVICE 1 : 0 AS HARD DISK #1.

NOTE: No error message is displayed if a second SCSI drive is not available.

If the system reports an initial number of hard drives greater than 2, the following message is displayed:

SYSTEM CONFIGURATION ERROR.

The AHA-1540A/1542A BIOS allows the use of 0, 1, or 2 hard disks on the SCSI bus under DOS without a device driver.

If 2 hard disks are attached to an internal hard disk controller, and are already recognized by the system, the BIOS does nothing. A device driver will be needed to access SCSI devices.

If 1 hard disk is attached to an internal hard disk controller, and is already recognized by the system, the BIOS attempts to assign the SCSI device (Target : LUN) 0 : 0 as the second drive. (drive D:) If this is unsuccessful, an initialization error is reported to the system.

If there are 0 hard disks attached to an internal controller, the BIOS attempts to assign the first SCSI device (Target : LUN) 0 : 0 as the first drive. (drive C:) If this is unsuccessful an initialization error is reported to the system. If successful, the BIOS attempts to assign another SCSI device as the second drive. (drive D:) Device 0 : 1 is tried first, and if that fails, device 1 : 0 is tried. There is no initialization error reported if a second drive is not available.

7.1.2 System Boot

System boot is invoked by execution of an Interrupt 19. No interception of this interrupt is necessary, as the PC/AT BIOS manages the boot process. When the boot procedure attempts to read the boot track from drive C:, the AHA-154XA BIOS will respond if drive C: is a SCSI Drive. Only SCSI drive 0:0 can be assigned as a SCSI C: drive. Mother board BIOS's that use interrupt 13 to perform booting should boot normally from SCSI drives using the AHA-154XA.

7.1.3 Hard Disk I/O

The BIOS enables up to two SCSI drives to be accessed via interrupt 13 as described in Section 6.

7.2 XENIX/UNIX Drivers

SCO Xenix and Unix, Interactive Systems Unix, and Microport Unix all support the AHA-1540A/1542A at the time of this publication. Please consult with these Operating System companies for more information on their products.

7.3 DOS Driver

An optional DOS Driver is available that enables the AHA-1540A/1542A to access additional SCSI devices on the SCSI bus. When operating under DOS, a device driver is needed to access more than two hard disks, tape devices or other types of SCSI peripherals. In addition, DOS applications that use the virtual memory mode of the 80386 processor require this driver. If you are not running DOS programs that operate in the virtual 80386 mode, or if all DOS operations will be confined to two SCSI disks or one internal and one SCSI disk, a device driver is not needed because of the on-board BIOS.

The DOS driver is installed by creating a DOS configuration (CONFIG.SYS) file that calls the device driver at boot time. Please refer to your DOS manual for information on creating a CONFIG.SYS file. At initial system loading, the AHA-1540A/1542A device driver will determine the number of hard disks attached to the system. The device driver is normally only installed if one of the following cases is true.

1) There are two internal hard disks and one or more SCSI disks.
2) There is one internal hard disk and two or more SCSI disks.
3) There are no internal hard disks and more than two SCSI disks.

The following table shows how hard disks in a system are addressed:

Configuration	C:	D:	Device Driver
TWO INTERNAL HARD DISKS	1st Int. Disk	2nd Int. Disk	SCSI Devices
ONE INTERNAL HARD DISK	Internal Hard Disk	SCSI 0/0 Disk	Other SCSI Devices
NO INTERNAL HARD DISK	SCSI 0/0 Disk	SCSI 0/1 or 1/0	Other SCSI Devices

The SCSI disk drives that are accessed by the device driver are divided into 32 MB logical disks. There can be multiple logical disks on one physical SCSI disk drive. A utility program is also provided that performs the functions of the DOS FDISK and FORMAT utilities. This utility will perform FDISK and FORMAT to SCSI disks that can only be accessed through the device driver. These utility programs partition the disks and create file directories so that DOS files may be copied and accessed from SCSI drives. Please refer to your DOS manual for details of FDISK and FORMAT.

SCSI 2 compatible and QIC 104 command set 1/4" tape drives are also be supported by the DOS device driver. The user accesses a SCSI tape drive by building a CCB as described in Section Five. The device driver passes the CCB to the AHA-1540A/1542A and instructs the AHA-1540A/1542A to complete the command. Software products such as Sytron Corporations SYTOS Tape Operating System automatically interface to the Adaptec AHA-1540A/1542A DOS driver.

To install the driver into your boot routine, you must create, or edit the DOS configuration file named CONFIG.SYS. You can use any file editor to do this, or you can create it through the "COPY CON: CONFIG.SYS" DOS command. Refer to your DOS manual for more information on this command. Once installed, the driver operates transparently to the user.

7.3.1 DOS Driver Support of Virtual Mode

The use of high performance 16-bit Bus Master DMA on the AHA-1540A/1542A SCSI host adapter may result in incompatible operation with application programs that use the 80386 virtual memory mode of operation.

In real mode, the host adapter BIOS is passed a physical address. This is necessary since the host adapter controls all SCSI I/O without CPU intervention. This physical address may not be passed

to the host adapter when the system is in the V86 mode. Programs that use the V86 mode can only be run on 80386 machines.

The AHA-1540A/1542A DOS driver also allows this type of application program to run under DOS.

7.4 AHA-1540A/1542A On-board Utilities

The AHA-154XA BIOS contains a utility program that allows the user to perform the several important functions. The utility programs are accessed using a self explanatory menu.

The utilities are accessed using the DOS Debug function. To access the utilities, boot using a standard DOS system disk or diskette. When the DOS prompt symbol appears on the screen, enter the debug program by typing **debug** and pressing Enter. The debug program will load and present a new cursor, the - symbol. Enter the following line and press enter to invoke the On-board Utility program.

G=dc00:6

If a BIOS base address other than DC000H is being used on the adapter to be tested, replace the dc00 parameter with the actual BIOS base segment. The segment is the upper 16 bits of the 20 bit BIOS base address.

The menu options include the following items which are selected by pressing the index number of the menu function.

(1) A list of all devices installed on the SCSI bus may be requested. This information is retrieved via a RETURN INSTALLED DEVICES host IOCP command, followed by INQUIRY commands to all available targets.

(2) A device may be selected for execution of the following two functions. Pressing the '2' key toggles the selection from one installed device to the next.

(3) A low level, or primary, format of the selected Target/LUN can be requested. A MODE SELECT is issued first to set the block size at 512 bytes per sector. Then a FORMAT command is issued which will format the drive with factory as well as grown defects. Only one SCSI drive can be formatted at a time.

(4) Integrity of a target can be checked by verifying an entire drive. Any correctable errors found will automatically be handled through the SCSI Reassign Blocks Command. If any uncorrectable errors are found the user will first be asked via a screen prompt if reassignment of the effected block should be performed.

(5) The user can leave the AHA-154XA On-board Utility functions and return to normal DOS operation.

In addition to the On-Board Utilities, a DMA channel test also resides on the AHA-154XA BIOS. The test verifies that all DOS-available memory can be accessed correctly from the host adapter using first party DMA. The test takes from 2 to 10 minutes to execute, depending on the CPU speed and the amount of memory available. The test is invoked by entering the debug program as above and entering:

G=DC00:9

The program then is activated and verifies each segment of the memory, indicating with screen messages as each segment is verified. The test runs indefinitely or until an error is detected. In most cases of error, the error information cannot be presented since the host operating system is likely to be compromised. The error symptom is usually a system crash. The test is halted by rebooting.

8.0 SCSI FEATURES

8.1 SCSI DESCRIPTION, INITIATOR MODE

The AHA-1540A/1542A provides a very high performance SCSI interface connection. The host adapter meets the ANSI Standard X3.131-1986, describing the SCSI. The host adapter additionally meets conformance level 2 of the specification by implementing the following SCSI options:

Accepts or manages the following messages:

Command Complete
Disconnect
Message Reject
Identify
Save Data Pointer

Performs arbitration

The following alternatives are selected for the AHA-1540A/1542A SCSI interface connection from those described by X3.131-1986.

Single-ended SCSI driver/receivers are used.

The Termination Power is supplied through a removable fuse, allowing the user to select whether or not termination power is provided by the host adapter at installation time.

Parity is always generated. Parity checking can be disabled through the jumper selection.

The "Soft" Reset option is always performed by the AHA-1540A/1542A. If the user desires the "Hard" Reset, an interrupt servicing program that detects the SCSI Reset Detected interrupt in the Interrupt Flags Port must set the Soft Reset bit in the Control Port. This bit forces the host adapter to clear all SCSI related operations, but does not require execution of the diagnostic functions. If the Soft Reset bit has been set, the host software must re-initialize the AHA-1540A/1542A.

Synchronous data transfer is supported. Negotiation for the synchronous transfer initiated by another SCSI device will be accepted by the AHA-1540A/1542A at any time. If the jumper has been set to allow it, the AHA-1540A/1542A will also initiate synchronous data transfer negotiation when it has detected that such negotiation may be required.

Multitasking is fully supported.

Modify Data Pointers is supported to allow Zero Latency Read operations.

In addition to these SCSI functions, the SCSI Common Command Set at level 4B is also supported. While this document was never made a standard, it describes a widely available set of disk drive functions which are supported by the host adapter. The Host Adapter BIOS commands are all mapped in to SCSI CCS commands to allow the proper support of all the most common SCSI disk drives. The Adapter Command "Return Installed Devices" also uses CCS commands to determine which devices are available.

The draft ANSI standard for SCSI-2 has been used as a reference for the implementation of all SCSI functions with the expectation that the host adapter will be fully compatible with the final version of the SCSI-2 standard. In particular, the Processor type device command set has been selected from the SCSI-2 manual for Target Mode operation.

8.1.1 Linked SCSI Commands

The AHA-1540A/1542A supports linking of SCSI commands in initiator mode. When the link bit in the SCSI command control byte is set, the target will present either a 0A or 0B message at command completion. The AHA-1540A/1542A uses the the link pointer in a CCB to fetch another CCB. At the same time, the completed CCB status and address are stored in an MBI. If the target returns a 0B or 00 message, the AHA-1540A/1542A generates an interrupt to inform the host of the full MBI. If the target returns a 0A message, the MBIF interrupt is not posted until all linked commands are completed. The linked CCBs must address the same target and LUN since the target is not re-selected.

8.1.2 Zero Latency Read Operation

The AHA-1540A/1542A implements Zero Latency operation through the use of modify data pointer messages. Zero Latency can eliminate rotational latency, depending on the length of the data transfer, by supporting out of order data transfers. This advanced feature is currently only implemented on the ACB-4525Z SCSI to ESDI controller, and is supported transparently to the user.

Since the Adaptec host adapter family is the first to support Zero Latency Read operation, this section is intended to briefly explain the required target support. Please refer to the Adaptec ACB-4525Z SCSI to ESDI controller manual for complete details of Zero Latency Read operation.

After seeking to the target track, the ACB-4525Z (ACB-4525Z is assumed since it is the first SCSI controller to implement this feature) will begin reading block IDs. If the first block ID is within range of the data transfer, but not the last block of the the data transfer, the ACB-4525Z will begin reading the subsequent blocks into its buffer. Before transferring data the ACB-4525Z will issue a MODIFY DATA POINTER message to the AHA-1540A/1542A. This supplies a positive argument that is added to the value of the current data pointer. The ACB-4525Z will now send this portion of the data transfer to the host. The ACB-4525Z will resume reading data into its buffer as soon as the first block of the data transfer is detected. Before sending this data to the host, the ACB-4525Z will issue a second MODIFY DATA POINTER message to the AHA-1540A/1542A which supplies a negative argument. This returns the data pointer to its original position. This guarantees that a data transfer of one track or less will never require more than a single revolution since data can now be transferred out of order.

8.1.3 SCSI Messages

The AHA-154XA host adapter supports a number of special messages in addition to the messages required by meeting conformance level 2. Those messages are described in detail in the SCSI specification, X3.131-1986, and in this section where they are used. The messages are summarized in this table:

FUNCTION	MESSAGE	CAUSED BY
Standard Messages	Command Complete	Normal Sequencing
Error Management	Message Reject	Invalid Messages
	Bus Device Reset	Special CCB
	Abort	Special MBO
Disconnect / Reconnect	Identify	Normal Sequencing
	Disconnect	Normal Sequencing
	Save Data Pointer	Normal Sequencing
	Restore Pointers	Special Sequencing/ZLR
Synchronous Transfer	Synchronous Data Transfer Request	Initialization Sequencing
Zero Latency Operation	Modify Data Pointers	ZLR Sequencing
Linked Commands	Linked Command Complete	Command Linking
	Linked Command Complete With Flag	Command Linking

8.2 SCSI DESCRIPTION, TARGET MODE

8.2.1 Initiator Conformance Level Requirements

Initiators that execute commands against an AHA-1540A/1542A operating in Target Mode are required to have the following conformance levels, as described in Appendix E of the SCSI Specification, ANSI X3.131-1986. Conformance must be present with respect to each of the following items:

The initiator must use single-ended drivers.

Termination power may optionally be provided by the initiator, but must meet the SCSI specification in both its over-current protection and its reverse current diode protection. The terminators may be installed on the AHA-1540A/1542A board or installed as in-line terminators at the cable connectors.

The implementation of parity is optional, but desirable.

The initiator may support either "hard" reset or "soft" reset. All attached devices must support the same type of reset.

The initiator must meet the requirements of conformance level two. In particular, all LUN addressing must be performed by the IDENTIFY message, not by the LUN field in the CDB. Disconnection and reconnection must be supported.

The initiator and target functions have the same SCSI ID.

8.2.2 Support of Synchronous Transfer

Synchronous transfer is supported by the AHA-1540A/1542A in target mode without any instruction or support from the system processor. If an initiator invokes a synchronous transfer negotiation, the AHA-1540A/1542A will complete the negotiation of the required transfer offset and period. If the proper jumper has been set, the AHA-1540A/1542A will also attempt to negotiate synchronous transfer during the initial selection period of the first command after an initialization or after a SCSI reset.

8.2.3 SCSI Target Operation in Processor Target Mode

When the AHA-1540A/1542A has been set to respond in Processor Target Mode, the host adapter appears on the SCSI bus as a normal processor type device as defined by the SCSI specification. From one to eight LUN's may be supported, depending on the LUN mask byte in the Enable Target Mode command. Five SCSI commands are accepted:

TEST UNIT READY
REQUEST SENSE
INQUIRY
SEND
RECEIVE

All other commands are rejected with CHECK CONDITION status. The sense information will indicate a Sense Key of 05H (Illegal Request) with a Sense Code of 20H (Invalid Command Operation Code).

The commands that do not perform data transfer to or from the host are handled completely by the AHA-1540A/1542A with no CCB communication with the host system. Those commands are the TEST UNIT READY, REQUEST SENSE, and INQUIRY commands. The SEND and RECEIVE commands must have a CCB from the host with the proper direction bits, the proper initiator address, and the proper LUN number to complete the SCSI operation. The SEND and RECEIVE CCBs may be provided to the host adapter before a command is received on the SCSI or may be requested after the command is received.

Each time an initiator activates a command to the AHA-1540A/1542A, an internal sub-channel is activated to manage the command. The sub-channel is dedicated to that particular LUN-Initiator transaction until all operations associated with the command are completed. Such operations include disconnection to obtain a CCB, pending error conditions, and linked operations. If all sub-channels are busy, a selection to the AHA-1540A/1542A will result in the AHA-1540A/1542A accepting the command and then generating BUSY status immediately. If this occurs, the initiator must re-issue the command later.

8.2.3.1 TEST UNIT READY

BIT BYTE	7	6	5	4	3	2	1	0
0	Test Unit Ready Operation Code (00)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Reserved (00)							
5	Reserved (00)						Flag	Link

The TEST UNIT READY command follows the SCSI specification in all respects. If the AHA-1540A/1542A has been initialized by the Enable Target Mode command to the Processor Target Mode, the command will finish normally with GOOD status and a COMMAND COMPLETE message. The host adapter supports the normal definition of UNIT ATTENTION on the first operation after power on, after a SCSI Reset, or after a BUS DEVICE RESET.

If a TEST UNIT READY command is executed against an LUN which was not allowed by the Enable Target Mode command, then CHECK CONDITION status will be presented with sense data of Sense Key 5 (Invalid Request) and an Error Code of 25H (Invalid LUN).

8.2.3.2 REQUEST SENSE

BIT BYTE	7	6	5	4	3	2	1	0
0	Request Sense Operation Code (03h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

If the AHA-1540A/1542A has returned CHECK CONDITION status to a previous command, the REQUEST SENSE command will obtain the sense information associated with the error. The sense information will be sent in the extended sense format according to the SCSI standard. The data format is given in the following figure:

BIT / BYTE	7	6	5	4	3	2	1	0
0	Error Code (70h or Foh)							
1	Reserved (00h)							
2	00		ILI	0	Sense Key			
3 - 6	Information Bytes (Residue)							
7	Additional Sense Length (06h)							
8 - 11	Reserved (00000000h)							
12	Additional Sense Code							
13	Additional Sense Code Qualifier (00h)							

The following errors are detected and presented by the AHA-1540A/1542A while operating in Processor Target Mode:

Error	Sense Key	Additional Sense Code
No Sense Data	00	00
Invalid Command Operation Code	00	20
Invalid LUN	05	25
Invalid Command Parameter	05	26
Power Up Attention	06	29
Reset Attention	06	29
Interface Parity Error	0B	47
Initiator Detected Error	0B	48
Dumb Initiator	05	2B

One set of error data may be buffered for each initiator - LU association possible, up to a total of 56 sets of sense data. No Contingent Allegiance or Extended Contingent Allegiance state is established.

The Error Code (Byte 0) will be F0h if the residue field is valid and 70h if the residue field has no information.

The Incorrect Length Indicator (ILI) will be set if an incorrect data transfer length is executed as described in Section 8.2.4.

The residue is set equal to the transfer length requested in the initiator CDB minus the target host's specified data length specified as a four-byte two's complement number.

8.2.3.3 INQUIRY

BIT / BYTE	7	6	5	4	3	2	1	0
0	Inquiry Operation Code (12h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

The INQUIRY command provides the information necessary to uniquely identify the Adaptec AHA-1540A/1542A as a Processor-type device. The information is returned in the SCSI-2 format. The following information is returned to any selecting initiator from any selected AHA-1540A/1542A Logical Unit:

BIT / BYTE	7	6	5	4	3	2	1	0
0	Peripheral Qualifier			Processor Device Type (03h)				
1	Reserved (00h)							
2	Reserved (00h)					ANSI Version (02)		
3	Response Data Format (02h)							
4	Additional Length (1Dh)							
5	Reserved (00h)							
6	Reserved (00h)							
7	0	0	0	Sync =1	Lnk=1	0	0	0
8 - 15	Vendor Identification (ASCII) ADAPTEC *bbb*							
16 - 31	Product Identifiction (ASCII) AHA-1540*bbbbbbbb*							
32 - 35	Product Revision Level (ASCII)							

If the INQUIRY command is attempted against a Logical Unit that has not been enabled as a target, byte 0 is returned as 23h, indicating that the LUN is not installed, but would be a Processor Device if it were installed. The remaining bytes are returned normally.

If a length shorter than the required 36 bytes is specified by the INQUIRY command, the number of bytes specified by the command is transferred. If a length longer than 36 bytes is specified, the command will only transmit 36 bytes.

8.2.3.4 SEND

BIT BYTE	7	6	5	4	3	2	1	0
0	Send Operation Code (0Ah)							
1	LUN (unused = 00)			Reserved (00)				
2	Transfer Length (MSB)							
3	Transfer Length							
4	Transfer Length (LSB)							
5	Reserved (00)						Flag	Link

The SEND command has the format specified by the SCSI standard.

The SEND command transfers data from the initiator to the target. The information is placed in the area specified by the appropriate CCB. If an appropriate CCB has not already been provided to the host adapter by the host software, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI until the CCB is made available to the host adapter through the MBO protocol. An appropriate CCB must have the same initiator address, target LUN, and direction as is required to complete the command.

The transfer length in the SEND command specifies the length in bytes of data that is sent during the DATA OUT phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in Section 8.3.2.6.

The CDB information is included in the returned CCB so that the receiving host programming can determine whether or not the information transmitted by the SEND command was application data or asynchronous event notification data.

8.2.3.5 RECEIVE

BIT BYTE	7	6	5	4	3	2	1	0
0	Receive Operation Code (08h)							
1	LUN (unused = 00)			Reserved (00)				
2	Allocation Length (MSB)							
3	Allocation Length							
4	Allocation Length (LSB)							
5	Reserved (00)						Flag	Link

The RECEIVE command has the format specified by the SCSI standard

The RECEIVE command transfers data from the target to the initiator. The information is taken from the area specified by the appropriate CCB. If an appropriate CCB has not already been provided to the host adapter host software, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI until the CCB is made available to the host adapter through the MBO protocol. An appropriate CCB must have the same initiator address, target LUN, and direction as is required to complete the command.

The transfer length in the RECEIVE command specifies the length in bytes of data that is sent during the DATA IN phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in section 8.3.2.6.

8.2.4 Incorrect Length Management for Target Mode Operation

The messages transmitted using the SEND and RECEIVE commands are normally expected to have a length that has previously been agreed to by the initiator system software and by the target system software. If the transfer length specified by the command is equal to the transfer length specified by the CCB, normal operation takes place and no errors are posted.

If the transfer length specified by the initiator's command is shorter than the space defined by the target CCB, all data bytes expected and required by the initiator will be transmitted. The target AHA-1540A/1542A will indicate GOOD status on the SCSI at the end of the transfer. The target system's software however must be notified that the entire area of data defined by the CCB was not transmitted. A Target Status of GOOD will be presented in the returned CCB. At the same time, the Incorrect Length Indication bit (bit 5 of byte 2) will be set in the CCB Request Sense data area. Bytes 3 through 6 of the Request Sense data area will contain the residue in two's complement notation of the length requested in the initiator command minus the length of the data area defined by the CCB. In this case, the residue will be a negative number, since the requested length was less than the area specified by the CCB. The HA status stored in the CCB will be 12h, indicating a Data Over/Under Run. The MBI Status Byte will be set to 04 to indicate that the CCB was completed with an error.

If the transfer length specified by the initiator's command is longer than the space defined by the target CCB, only those bytes contained within the CCB's data transfer area will be transmitted. The target AHA-1540A/1542A must indicate with an error condition to the initiator that not all the requested bytes could be transferred. The target AHA-1540A/1542A presents a SCSI status of CHECK CONDITION at the end of the data transfer. The Request Sense information transmitted to the initiator as a result of an immediately following REQUEST SENSE command indicates that an Incorrect Length Indication is present by setting bit 5 of byte 2. Bytes 3 through 6 of the Request Sense information transmitted to the initiator will contain the residue in two's complement notation of the length requested in the initiator command minus the length of the data area defined by the target CCB. In this case, the residue will be a positive number, since the requested length was greater than the available area. The target system's software must also be notified that the transfer length requested by the initiator exceeded the assigned buffer area. A Target Status of CHECK CONDITION will be presented in the returned target CCB. A Host Status of '12'h will be returned indicating a Data Over/Under Run. At the same time, the information that will later be posted to the initiator by the REQUEST SENSE command will be posted to the target system in the CCB Request Sense data area. This includes both the Incorrect Length Indicator and the Residue. The MBI Status Byte will be set to 04 to indicate that the CCB was completed with an error.

Section Nine Flexible Disk Controller Specification

9.1 FLOPPY DISK INTERFACE

The floppy disk controller allows the attachment of any standard IBM compatible floppy disk drive to the AHA-1542A. The floppy disk controller is accessed by the standard IBM compatible BIOS through the standard IBM compatible floppy diskette program interface. The floppy disk controller section of the host adapter is completely independent of the host adapter function. The floppy disk controller section can be disabled by removing jumper J13 as described in section 3.4.2. The base address and interrupt and DMA channels can be modified by jumpers as described in section 3.4.

A floppy disk is attached to the host adapter using a 34 pin ribbon cable connector as specified in section 1.4. The pin out of the cable is described here, although that is usually not necessary, since all standard floppy disk drives have the same pin out. Some systems choose to use the same address for all floppy disk drives and to twist the cable, pins 10-16, to switch the address lines at the drive.

Signal Name	Pin	Pin	Signal Name
Ground	1	2	-LD
Ground	3	4	Reserved
Ground	5	6	Reserved
Ground	7	8	-INDEX
Ground	9	10	MOTOR ENB DRIVE A
Ground	11	12	DRIVE SELECT B
Ground	13	14	DRIVE SELECT A
Ground	15	16	MOTORO ENB DRIVE B
Ground	17	18	-DIRECTION
Ground	19	20	-STEP
Ground	21	22	-WRITE DATA
Ground	23	24	-WRITE ENABLE
Ground	25	26	-TRACK 0
Ground	27	28	-WRITE PROTECT
Ground	29	30	-READ DATA
Ground	31	32	-HEAD SELECT
Ground	33	34	-DSKCHNG

10.0 PROBLEM DETERMINATION

10.1 SELF DIAGNOSTIC CAPABILITY

The AHA-1540A/1542A executes self diagnostics upon power up or after a hard reset. These diagnostics test the CPU operation, perform a sum check on the EPROM, and check the data transfer paths on the board. The host system has the option of exercising more extensive diagnostics involving reads and writes to memory.

The red light emitting diode (LED) on the host adapter indicates the result of the self diagnostic process. When power is first applied to the board, the LED turns on. If the board is operating normally, the light will soon go off and stay off until SCSI or I/O port activity is requested by the host. If the board is not operating correctly, a flash code number is flashed on the LED to indicate which test failed. The flash code number is indicated by a series of 1 to 6 closely spaced flashes followed by a longer pause. The flash code is repeated continuously until the board is powered off, reset, or repaired. The SCSI interface should be disconnected if these diagnostic tests are being run for fault isolation purposes. At least one set of terminators must remain installed or the LED will stay on, indicating that the AHA-154XA is receiving an active RST signal. Continuous execution of the diagnostics can also be forced by inserting the diagnostic jumper (pin-pair 2 in jumper J1). The flash code and associated failure modes are indicated in the following table.

TABLE OF FLASH CODES

FLASH CODE	POSSIBLE MEANINGS OF FLASH CODE
LED Remains On	Host Adapter Control Processor inoperative/terminators missing or not powered.
1 Flash	Firmware EPROM check sum failed.
2 Flashes	RAM test failed.
3 Flashes	AIC-6250 SCSI protocol chip verification failed
4 Flashes	FIFO read data path test failed.
5 Flashes	FIFO write data path test failed.
6 Flashes	Channel 2 test failed.

If any of these failure conditions is identified, the host computer should be powered down, the host adapter removed, and the host adapter inspected for physical damage. Such damage can include EPROM's that are not correctly installed or not firmly seated, broken wires, missing or damaged components, or conductive debris on the board. If no such physical damage is found, the AHA-154XA should be returned for repair.

All boards are fully tested, burned in, cleaned, and inspected before they are shipped. Care should be taken to keep the board in its protective conductive wrapping until it is installed. With these simple precautions, mechanical damage can normally be avoided.

10.2 INDICATORS

The red light emitting diode (LED) on the AHA-154XA is used to provide the fault isolation information described above. In addition, the LED indicates when the host adapter is performing activities on the host interface and the SCSI interface. The LED is such a useful activity indicator that a connector is made available on the host adapter to allow the cable to an externally visible LED to be attached. (See Section 3.3.9).

As an activity indicator the LED is turned on from the time that an Adapter Command is transmitted to the host adapter until the HACC interrupt is generated to indicate that the Adapter Command is complete. In addition, the LED will be turned on whenever SCSI bus activity is occurring. This is roughly the same period of time that the SCSI BSY signal is present on the SCSI bus. If the light stays on when no activity is expected to be present on the bus, it is possible that the bus is hung, the processor has failed, that unexpected activity is occurring, or that the SCSI cables are incorrectly installed. If the SCSI cables are installed reversed, the host adapter is forced in to a solid SCSI reset state which halts normal operation.

10.3 PROBLEMS DETECTED DURING OPERATION

The information in section 10.3 is not intended for routine users of the AHA-1502A/1542A. It is intended to provide a reference for programmers preparing device drivers, error recovery procedures, and error information presentation programs.

Operation of the I/O Port interface is controlled and monitored by host system software. Two bits in the Status Port (Base + 0), described in section 4.2.1, are provided to indicate unusual conditions in the host adapter.

Internal Diagnostic Failure (Status Port, bit 6): This bit indicates that the self testing process after either a hard reset or a power on operation was terminated by an error condition. The error indicates that a critical failure was found in the AHA-154XA control circuitry or data paths. The error should be presented to the host video display to indicate that diagnostic actions are required. The diagnostic action uses the host adapter diagnostic flash codes to determine if the AHA-154XA is failing. The host system should be powered off, then opened so that the LED can be observed. All SCSI cables, both external and internal, should be removed from the host adapter. The system should then be powered on. If the LED flashes once and turns off, the host adapter has passed its diagnostics and should be accessible again. If the LED flashes one of the error flash codes, the AHA-154XA should be replaced. If the LED remains on and does not turn off, the host adapter is not able to begin operation at all. The host system may be holding the AHA-154XA in the reset state or the host adapter may have failed. To distinguish these two cases, the AHA-154XA should be replaced and the new host adapter operation should be verified. Be sure to power down the host system when removing or replacing the host adapter. If the diagnostics

indicate that the AHA-154XA must be replaced, it should be sent to an authorized service facility for repair.

Invalid Host Adapter Command (Status Port, bit 0): This bit is set to indicate that a command or parameter transmitted to the host adapter was invalid. This is an indication that the host software, usually an operating system, special application program, or device driver, has generated an invalid request. The responsible programming organization should be notified so that the invalid sequence or parameter can be corrected.

10.3.1 HA Status Error Indications and Corrective Actions

The Host Adapter Status indications, in addition to indicating several normal completion states, indicate three general groups of errors. One set describes software errors in the requests made to the host adapter. Even though most of these errors are caused by software design problems, the AHA-154XA may need to be replaced as an isolation step, since there exists a small chance that hardware failures in the AHA-154XA cause the appearance of a software error.

A second set describes errors detected by the host adapter firmware in the host adapter hardware. The most likely failing component in this case is the AHA-154XA, although certain system or cable failures may generate the appearance of a host adapter hardware error.

A third set describes the appearance of unexpected or incorrect sequences executed by the attached SCSI devices. In this case, the cables are the most likely failure point, with the peripheral device second and the AHA-154XA third. The host adapter status code should be returned to the host video display to indicate to the operator what errors have occurred and under what conditions the errors occurred. The following section describes those Host Adapter Status indications that indicate an error.

NUMBER	TYPE	ERROR	DESCRIPTION AND CORRECTIVE ACTION
11	SCSI	NO	Selection Time Out: The SCSI attempted to select a device that was not installed or that did not respond to selection due to a power, parity or addressing failure. Verify correct address values set to SCSI devices. Verify that SCSI cable routing includes the required devices. Verify SCSI cable integrity by replacement of cables. Verify that SCSI Selection Time Out value has been correctly established by Adapter Command.
12	HOST	NO	Data Over Run / Under Run: Data length or direction specified by CCB did not agree with the data length actually provided by the attached peripheral device. Often a normal error or accompanied by a check condition indicating transfer truncation. Verify program requested correct length or direction. Verify peripheral provided expected data length, number of blocks, or block length.

NUMBER	TYPE	ERROR	DESCRIPTION AND CORRECTIVE ACTION
13	SCSI	YES	Unexpected Bus Free: The target dropped BSY without executing the proper messages first. This normally indicates that the BSY and/or other portions of the SCSI bus failed or that the target encountered such an invalid sequence that no recovery was possible. Some targets may have sense information available to qualify the error condition. Verify SCSI cable integrity. Verify SCSI cables are all properly connected. Replace SCSI cables. Replace peripheral. Replace AHA-154XA.
14	SCSI	YES	Target bus phase sequence failure: The initiator detected an invalid phase or an invalid phase sequence. If this occurs, it is likely that the host adapter forces a SCSI reset on the bus as the first phase of the recovery process. Verify SCSI cable integrity. Verify SCSI cables are all properly connected. Replace SCSI cables. Replace peripheral. Replace AHA-154XA
15	HOST	YES	MBO Command Byte invalid: This indicates a software failure or bug in the host's development of the MBO entry. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
16	HOST	YES	Invalid CCB Operation Code: This indicates a software failure or bug in the host's development of the CCB. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
17	HOST	YES	Linked CCB does not have same LUN: This indicates that the host software generated an invalid combination of link commands. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.

NUMBER	TYPE	ERROR	DESCRIPTION AND CORRECTIVE ACTION
18	HOST	YES	Invalid Target Direction Parameters received from Host: This indicates that the host software generated an invalid Target Direction Parameter. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
19	HOST	YES	Duplicate CCB Received in Target Mode: This indicates that the host system was not keeping correct management information for target mode operation and incorrectly generated a second CCB identical to one already active. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
1A	HOST	YES	Invalid CCB Parameter or Segment List: A segment list was presented to the host adapter with a zero length segment or invalid segment boundaries. An invalid CCB parameter was presented to the host adapter. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.

10.3.2 SCSI Error Indications and Corrective Actions

Error conditions detected by SCSI peripherals usually cause a CHECK CONDITION Status byte to be presented. When this is presented, the host adapter automatically retrieves the sense information from the SCSI peripheral by executing a REQUEST SENSE command according to the SCSI standard. The information returned is mapped for single-threaded BIOS operation into the categories of error conditions described in section 5.2.2. For multitasking (mailbox) operation, the information returned is made available in the area allocated for Sense Data. In either case, an intelligent attempt is made by most operating systems to retry the operation at least one time. Such retry operations may require the management of queued operations that have already started execution. This attempt to retry the operation is rarely successful, since SCSI peripheral devices have very extensive automatic retry and correction mechanisms designed to be executed before the error information is returned in the first place.

Since it is rare that such an operation is successful, the host software and operating systems should make every attempt to make available key information about the error which can be analyzed by the system operator or customer engineer. In small systems, it may be sufficient to present the important Sense Data together with the command that created the error. Some simpler systems may perform a preliminary analysis of the error information and generate a code or descriptive text that describes the error and indicates the corrective action. In very complex systems, a logging process may take place, allowing a customer engineer to analyze the data at some future time. In all systems, such information is very important for host program verification and for system integrity

verification, even if the designers choose not to make the information available to any system users other than the design and maintenance engineers.

The SCSI Sense Data is generally self descriptive. The errors can be mapped in to four major categories, each category with its own diagnostic procedure.

The first category includes those errors caused by incorrect command or parameter bytes or by incorrect sequences of commands. These errors typically are presented only during the early development stages of an operating system or device driver, since a properly operating program will not generate invalid commands.

The second category includes those sense codes associated with peripheral status presentation. Such sense codes are not truly errors, in that they inform the host program of an unusual but not unexpected condition. Such sense codes include indications that a device is not ready, that the device has just become ready, that a device has reached the end of its media (End of Tape or Blank Check), or that the expected data length and actual data length differed. These sense codes are normally used by the device driver to execute the correct operation in response to the condition. Such sense codes are not normally presented to the system user except as text that requests some action. As one example, an End Of Tape condition may require the system user to replace the tape cartridge.

The third category of errors points to a particular hardware failure in the peripheral device or its supporting electronics. Such error conditions usually require the adjustment, repair, or replacement of the peripheral device or some of its components. In some cases, the error condition may also indicate possible cable or host adapter failures. These errors must be exposed to the system user so that the proper actions can be taken.

The fourth category of errors points to a media failure in the peripheral device. Such errors include bits that cannot be recovered from magnetic media and imperfections in the surface of optical media. Most such errors are recovered using the extensive retry and correction algorithms programmed into the peripheral device. In some peripheral device technologies, the errors may be caused by noise conditions or by marginal electronic failures in the read or write path. Those rare errors that cannot be recovered usually indicate that some data important to the operating system or application has been lost. The system must make this error information available to the system user so that the system user can replace the media or recover the data from a back up copy as required. In addition, logging of errors that were successfully recovered by the peripheral device is often useful as an indicator of the overall reliability of the device or of the requirement for periodic maintenance.

10.4 PROBLEMS DETECTED DURING INSTALLATION

This section may be useful to correct problems related to installation. The information in this section is included in the Host Adapter Installation Guide.

If the system will not boot from the flexible diskette drive after initial hardware installation the following items should be checked:

- AHA-1540A/1542A internal diagnostics: The LED on the AHA-1540A/1542A should come on briefly at system power up. If the LED begins to blink at regular intervals then the host adapter has detected an internal failure and should be returned for repair or replacement to the place of purchase. A message may also be posted to the screen.

- If the AHA-1540A/1542A LED and the SCSI drive LED are always on, the SCSI cable's pin 1 orientation has probably been reversed between the host adapter and the drive. See section 3.2.

- Is the AHA-1540A/1542A BIOS message displayed on the screen? If not, the AHA-1540A/1542A BIOS is not being recognized by the system.

  a) Check for BIOS address conflicts between the AHA-1540A/1542A and other option boards.
  b) Try a different BIOS address. See section 3.3.
  c) Change the BIOS wait state jumper. See section 3.3.

- If the HOST ADAPTER NOT FOUND AT PORT 330H message is displayed check the AT port address jumper setting. Also verify that the SCSI cable is correctly installed. A forced SCSI reset caused by an inverted or displaced internal SCSI cable may cause the problem. See Section 3.3.

Problems Booting the System from a SCSI drive:

- Make sure that both standard hard disks are mapped out of the system by using the AT SETUP program.

- Make sure that the SCSI boot drive address is set to SCSI ID 0:0. Check the drive installation manual for information about setting the SCSI ID for that device. The Return Installed Devices utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.

- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.

- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing Section 3.

- Power should be cycled off and on after changing any values on a HA, Setup program, or SCSI device to be sure that a DOS format operation has been successfully completed.

- Make sure that the SCSI bus is properly terminated.

- Make sure that the intended boot disk has an active DOS partition and a DOS format. See section 3.0 and the DOS manual for more information.

Problems using a SCSI drive as drive D: with a standard hard disk as drive C:

- Make sure that the second hard disk is mapped out of the system with the AT SETUP program.
- Make sure that the SCSI drive to be used as drive D: is set to SCSI ID 0:0. Check the drive manual for information on setting the SCSI ID for that device. The Return Installed Devices utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.
- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.
- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing Section 3.
- Power should be cycled off and on after changing any values on an HA, Setup program or SCSI device to be sure that the new initial values are loaded.
- Make sure that the SCSI bus is properly terminated. See Section 3.
- Make sure that the disk has a DOS partition and a DOS format. See section 5.0 and the system DOS manual for more information.

Problems using a SCSI drive as drive D: with another SCSI drive as drive C:

- Make sure that both standard hard disks are mapped out of the system with the AT SETUP program.
- Make sure that the SCSI drive to be used as drive D: is set to SCSI ID 0:1 or 1:0. Check the drive manual for information on setting the SCSI ID for that device. The Return Installed Devices utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.
- Power should be cycled off and on after changing any values on an HA, Setup program or SCSI device to be sure that the new initial values are loaded.
- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.
- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing section 3.
- Make sure that the SCSI bus is properly terminated. See section 3.
- Make sure that the disk has a DOS partition and a DOS format. See section 3.0 and the DOS manual for more information.

System works erratically. Hangs or the host adapter can't always find the drives.

- Check SCSI parity for consistency.
- Check Termination.
- Check cable length and integrity.
- If host adapter and drive light remain on during a hang condition, make sure that the SCSI drive conforms to the Common Command Set revision 4B. (CCS 4B)
- If only the host adapter LED remains on during a hang, it is probably a host adapter, system interface problem. The system may not be capable of First Party DMA transfers. Check with the System manufacturer for information.

Section Eleven Glossary

Adapter Command — A command transmitted to the host adapter using the Command/Data Out Port and the Data In Port. The commands are sequenced using the Control Port, the Status Port, and the Interrupt Flag Port. Abbreviated as IOCP command.

AEN — See Asynchronous Event Notification

AHA-1540 — Adaptec Host Adapter for connecting SCSI devices to the PC/AT backplane bus. The AHA-154XA is an enhancement of the AHA-1540 (see Appendix C)

AHA-1540A — The enhanced high performance Adaptec Host Adapter for connecting SCSI devices to the PC/AT backplane bus.

AHA-1542A — The enhanced high performance Adaptec Host Adapter for connecting SCSI devices and standard IBM compatible floppy disk devices to the PC/AT backplane bus.

AHA-154XA — Either the AHA-1540A or the AHA-1542A or both.

AHA-1540A/1542A — Either the AHA-1540A or the AHA-1542A or both.

Asynchronous Event Notification — A process by which a target can send unsolicited sense information to an initiator using the SEND command in order to inform the initiator about the occurrence of an important unusual occurrence.

Asynchronous Data Transfer — Data transfer performed by the SCSI interface involving the interlocking of a signal to the initiator (REQ) and a signal to the target (ACK) such that each step of the data transfer protocol must occur before the next step can begin. Characterized by a low data rate and independence of external timing constraints, including cable length and circuit response times.

AT Bus — The Industry Standard Architecture bus.

Bus Device Reset — A SCSI message that clears all activity in the target to which it is addressed.

Byte — An 8 bit unit of data. An octet. A byte is normally the smallest addressable unit of a memory and the unit of transfer on the SCSI.

CCB — See Command Control Block

CCS — See Common Command Set

CDB — See Command Descriptor Block

Command Control Block

A software object prepared by the host microcomputer software for the host adapter to provide it all the control information it needs to execute a SCSI command. Abbreviated CCB.

Command Descriptor Block

A block of information passed across the SCSI bus to provide the command, parameter, and address information necessary for the target to execute the desired functions. Prepared by the host software and placed in the CCB to be passed to the target by the host adapter. Abbreviated CDB.

Common Command Set

A defacto standard SCSI command set for communication with hard disk drives. The Common Command Set (CCS) is the basis for the SCSI-2 command set for all types of peripheral devices.

Control Microprocessor

An integrated circuit computer used to execute the software that controls the host adapter's operation.

Device Driver

A program that is linked with or attached to an operating system to map the software interface of the operating system to the requirements of attached peripheral devices and host adapters.

DMA

See Direct Memory Access

Direct Memory Access

A mechanism that allows hardware control of the transfer of streams of data to or from the main memory of a computing system. The mechanism may require set up the host software. After initialization, it automatically sequences the required data transfer and provides the necessary address information.

EPROM

Erasable Programmable Read Only Memory. An integrated circuit used to store the host adapter firmware and the host adapter BIOS.

FIFO

First In / First Out.

A queueing order in which items are removed from the queue for execution in the same order in which they are placed in the queue.

An integrated circuit that buffers data in such a manner that the each byte placed in the buffer is removed from the buffer in the same order.

Firmware

The software that controls and manages the host adapter. It is 'firm' as opposed to 'soft' because it is designed in to the host adapter and cannot be modified by the user.

IBM PC/AT Compatible

Any computer system that emulates exactly the IBM PC/AT and that uses an ISA backplane bus.

ISA — The Industry Standard Architecture

Industry Standard Architecture — The IBM PC/AT functions have been duplicated by a number of manufacturers. All the IBM PC/AT™ compatible machines use a backplane bus that very closely emulates the function of the backplane bus of the PC/AT™. Because of the broad usage of this bus structure, it has become known as the Industry Standard Architecture bus, even though there is no presently accepted standard for the bus.

initiator — A SCSI device that requests an operation to be performed by another SCSI device (the target). The initiator provides all the command information and parameters required to perform the operation, but the details of the operation are actually sequenced by the target.

host — A microcomputer in which a host adapter is installed. The host uses software to request the services of the host adapter in transferring information to and from peripheral devices attached to the SCSI bus connector of the host adapter.

host adapter — A hardware printed circuit board that installs in a standard microcomputer backplane and provides a SCSI bus connection so that SCSI devices can be connected to the microcomputer. A host adapter is "intelligent" if it has a simple high-level software interface to the microcomputer. A host adapter is "dumb" if the microcomputer must directly manage the SCSI protocol using the microcomputer processor.

Logical Unit — A physical or virtual device addressed through a target.

Logical Unit Number — An encoded three-bit identifier for a logical unit.

LU — See Logical Unit

LUN — See Logical Unit Number

Mailbox In — An area in main memory assigned by the host microcomputer software for communication with the host adapter. The host adapter places status and pointer information in entries in the Mailbox In (MBI) to indicate to the host microcomputer what operations have been completed or what information must be obtained from the host microcomputer.

Mailbox Out — An area in main memory assigned by the host microcomputer software for communication with the host adapter. The microcomputer software places commands and pointer information in entries in the Mailbox Out (MBO) to indicate what operations should be started by the host adapter.

MBI — See Mailbox In.

MBO — See Mailbox Out.

Multi-tasking Operation — The execution of commands in such a way that more than one command is in progress at the same time, allowing the system to take advantage of overlapping activities by using resources that are temporarily not required for other operations. More than one program or more than one portion of a program may be operating in parallel.

PC/AT — A family of small computers sold by IBM, also called the Personal Computer /AT family of computers. The name is trademarked by IBM.

RAM — Random Access Memory. Memory of which any byte can be accessed directly in a single memory cycle. Information can be read from and written to the memory.

SCSI — Small Computer System Interface.

SCSI ASC — SCSI Additional Sense Code. Byte 12 of the extended sense information. Provides a standardized description of the condition described by the sense information.

SCSI Device — A device attached to a Small Computer System Interface bus cable. The device may be an initiator, a target, or capable of both types of operation. The device may be a peripheral device, a host device, or a device mixing both roles.

Single Threaded Operation — Operation of the computing system such that only one program can be operating or active at a time. The computing system must wait until all resources are available before starting an operation and cannot start another operation until the first one is completed. No overlapping of latencies or program operation occurs.

Synchronous Data Transfer — A method of data transfer on the SCSI bus involving clocking data on to the bus with a fixed-length fixed-frequency strobe pulses. The acknowledgements may be delayed several clock periods from the data requests. Synchronous Data Transfer can be used only for data transmission on the SCSI bus. It is prohibited for command, message, and status transmission.

Synchronous Data Transfer Negotiation

The message exchange between the initiator and the target that allows the negotiation of the data transfer frequency and delay between requests and acknowledgements required for synchronous data transfer. Once negotiated, synchronous data transfer parameters remain unchanged until certain reinitialization activities occur.

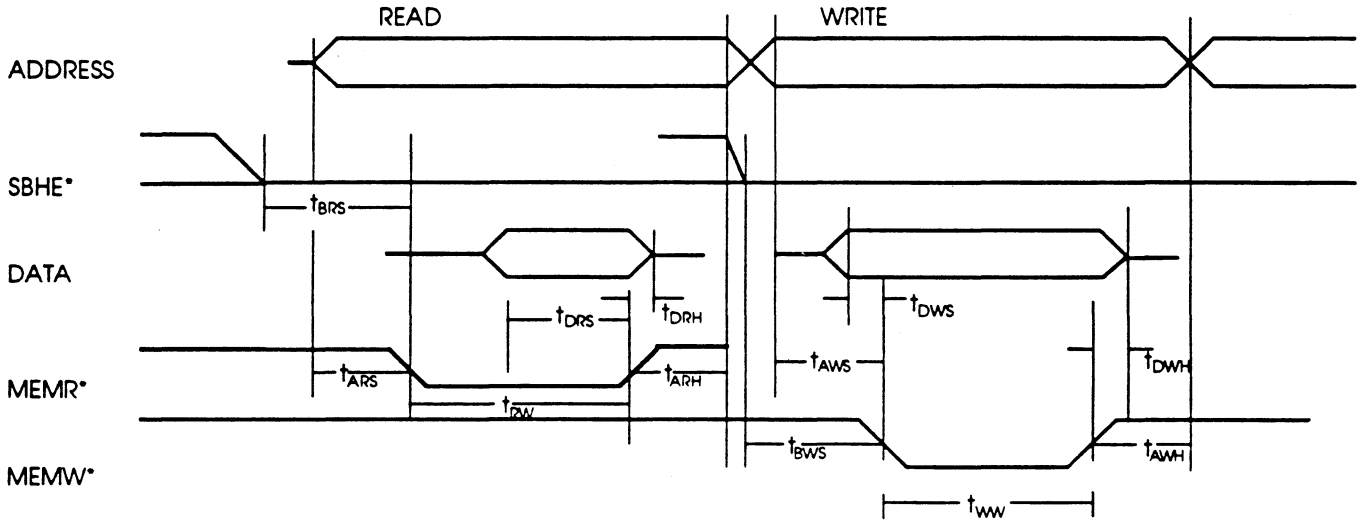
Target

A SCSI device that performs an operation requested by an initiator. The target may be a peripheral device performing a service for an initiator. The target may also be a host adapter performing a Processor type device service for an initiator.

Word

A two byte (16 bit) unit of data.

AHA-1540A/1542A MEMORY CYCLE TIMING



STANDARD SPEEDS	t_{RR} t_{WW}	TIMING
5.0 MB	250	A
5.7 MB	200	A
6.7 MB	200	A
8.0 MB	150	A
10.0 MB	100	B

SPEED	TIMING A	TIMING B
t_{ARS}	73	23
t_{ARH}	55	55
t_{BRS}	73	23
t_{DRS}	32	32
t_{DRH}	26	26
t_{AWS}	73	23
t_{AWH}	55	55
t_{BWS}	73	23
t_{DWS}	13	13
t_{DWH}	60	60

t_{ARS} Address Setup to MEMR Leading Edge
t_{ARH} Address Hold from MEMR Trailing Edge
t_{BRS} SBHE Setup to MEMR Leading Edge
t_{DRS} Data Setup to Trailing Edge of MEMR
t_{DRH} Data Hold from MEMR Trailing Edge
t_{RW} Read Pulsewidth

t_{AWS} Address Setup to MEMW Leading Edge
t_{AWH} Address Hold from MEMW Trailing Edge
t_{BWS} SBHE Setup to MEMW Leading Edge
t_{DWS} Data Setup to MEMW Leading Edge
t_{DWH} Data Hold from MEMW Trailing Edge
t_{WW} Write Pulsewidth

Note: I/O Channel Ready may slow the actual transfer rate

Appendix B CONNECTOR PINOUT

Internal Connector Pin Assignments

Signal Name	Pin	Pin	Signal Name
Ground	1	2	-DB(0)
Ground	3	4	-DB(1)
Ground	5	6	-DB(2)
Ground	7	8	-DB(3)
Ground	9	10	-DB(4)
Ground	11	12	-DB(5)
Ground	13	14	-DB(6)
Ground	15	16	-DB(7)
Ground	17	18	-DB(P)
Ground	19	20	Ground
Ground	21	22	Ground
Ground	23	24	Ground
Open	25	26	Term Power (Fused)
Ground	27	28	Ground
Ground	29	30	Ground
Ground	31	32	-ATN
Ground	33	34	Ground
Ground	35	36	-BSY
Ground	37	38	-ACK
Ground	39	40	-RST
Ground	41	42	-MSG
Ground	43	44	-SEL
Ground	45	46	-C/D
Ground	47	48	-REQ
Ground	49	50	-I/O

External Connector Pin Assignments

Signal Name	Pin	Pin	Signal Name
Ground	1	26	-DB(0)
Ground	2	27	-DB(1)
Ground	3	28	-DB(2)
Ground	4	29	-DB(3)
Ground	5	30	-DB(4)
Ground	6	31	-DB(5)
Ground	7	32	-DB(6)
Ground	8	33	-DB(7)
Ground	9	34	-DB(P)
Ground	10	35	Ground
Ground	11	36	Ground
Ground	12	37	Ground
Open	13	38	Term Power (Fused)
Ground	14	39	Ground
Ground	15	40	Ground
Ground	16	41	-ATN
Ground	17	42	Ground
Ground	18	43	-BSY
Ground	19	44	-ACK
Ground	20	45	-RST
Ground	21	46	-MSG
Ground	22	47	-SEL
Ground	23	48	-C/D
Ground	24	49	-REQ
Ground	25	50	-I/O

Appendix C AHA-1540/1640 FAMILY COMPATIBILITY INFORMATION

Brief summary of board characteristics:

AHA-1540:

High performance SCSI to ISA Bus Master host adapter. Most revisions support synchronous data transfer. Separate user's manual. Subset of AHA-154XA Adapter Commands available.

W AHA-1542A:

High performance SCSI to ISA Bus Master host adapter. Supports synchronous data transfer. Supports floppy disk drives. Higher level of host adapter integration.

AHA-1542A:

High performance SCSI to ISA Bus Master host adapter. Supports synchronous data transfer. Supports floppy disk drives. Higher level of host adapter integration. Improved SCSI connection pattern and jumper controls. Supports Target Mode operation.

AHA-1540A:

High performance SCSI to ISA Bus Master host adapter. Supports synchronous data transfer. Does not support floppy disk drives. Higher level of host adapter integration. Improved SCSI connection pattern and jumper controls. Supports Target Mode operation.

AHA-1640:

Very high-performance SCSI-to-Micro Channel Bus Master host adapter. Supports synchronous data transfer. Does not support floppy disk drives. High level of host adapter integration. Supports Target Mode Operation. See Adaptec's AHA-1640 User's Manual for details, including POS management, differences in interrupt presentation, differences in reset management and improvements in Adapter commands.

COMPATIBILITY CHART

Function	1540	W1542A	1542A	1540A	1640
Floppy Disk Controller	No	Yes	Yes	No	No
Synchronous Transfer	No	Yes	Yes	Yes	Yes
Selectable DMA Speeds	No	Yes	Yes	Yes	POS
Programmable DMA Speeds	Yes	Yes	Yes	Yes	Yes
Internal SCSI Connectors	Straight	Rt Angle	Rt Angle	Rt Angle	Straight
Scatter Gather	No	Yes	Yes	Yes	Yes
64 Head BIOS	Option	Yes	Yes	Yes	Yes
16 Head BIOS	Yes	No	No	No	No
LED Connector	No	Yes	Yes	Yes	Yes
Target Mode	No	No	Yes	Yes	Yes
LA 17-19 Jumper	Yes	Yes	No	No	NA
Micro Channel	No	No	No	No	Yes
PC/AT	Yes	Yes	Yes	Yes	No

Preface

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