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ADVANCED ELECTRONICS DESIGN, INC.
WINC-08 OPERATIONS AND MAINTENANCE MANUAL

PREFACE

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AED reserves the right to make changes in the product design without reservation and without notification to its users.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

LIST OF TABLES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

Section 1

INTRODUCTION

1.1 SCOPE AND PURPOSE OF MANUAL

This manual contains information on the performance, installation, operation, maintenance, and troubleshooting of the WINC-08 disk drive system. It is intended for operational and maintenance personnel.

1.2 REFERENCE DOCUMENTS

Reference documents include the following:

WINC-08 Documentation Package AED -- Part No. 180003-XX
FLEX-02 User's Guide AED -- Part No. 990000-01
FUJITSU M2301B/2302B Maintenance Manual -- FUJITSU LTD
Microcomputer Processors -- Digital Equipment Corporation
Minicomputer Handbook -- Digital Equipment Corporation
PDP-11 Peripherals Handbook -- Digital Equipment Corporation
Data Trak 8, Maintenance Manual -- Qume Corporation

1.3 OVERVIEW OF SYSTEM

The WINC-08 controller is unique in its utilization of single or dual 8-inch Winchester drives to emulate DEC RL02 drives; or you can order it with one 8-inch (single or dual head), floppy drive in place of the second Winchester.

The floppy disk drive option emulates the DEC RX02. Its dual head allows storage on both sides of the diskette, for a total capacity of one megabyte per diskette. Thus, in a single compact configuration, you can emulate both the RL02 and the RX02. A functional block diagram of the WINC-08 is shown in Figure 1-1.

Briefly, WINC-08 technology includes these features:

- o Reliability
- o Steel band stepping motor
- o Modular construction
- o No preventive maintenance
- o Easy access to subassemblies
- o Low power consumption
- o Optional floppy disk
- o Error correction code
- o Faster data throughput
- o Software compatibility
- o Unique diagnostic self-test

The WINC-08 controller is a state-sequential machine based on a bipolar microprocessor. The horizontally structured microprocessor improves reliability of the controller by minimizing the component usage and cost.

The WINC-08 controller is functionally equivalent to the DEC RL02, and so it is compatible with DEC software. You can run either RT-11 or RSX-11M without the need or concern for software modifications.

The WINC-08 also offers PDP-11 or LSI-11 users the ability to expand their system to a total storage capacity of 41.6 megabytes -- equal to a fully expanded DEC RL02 system with four disk drives.

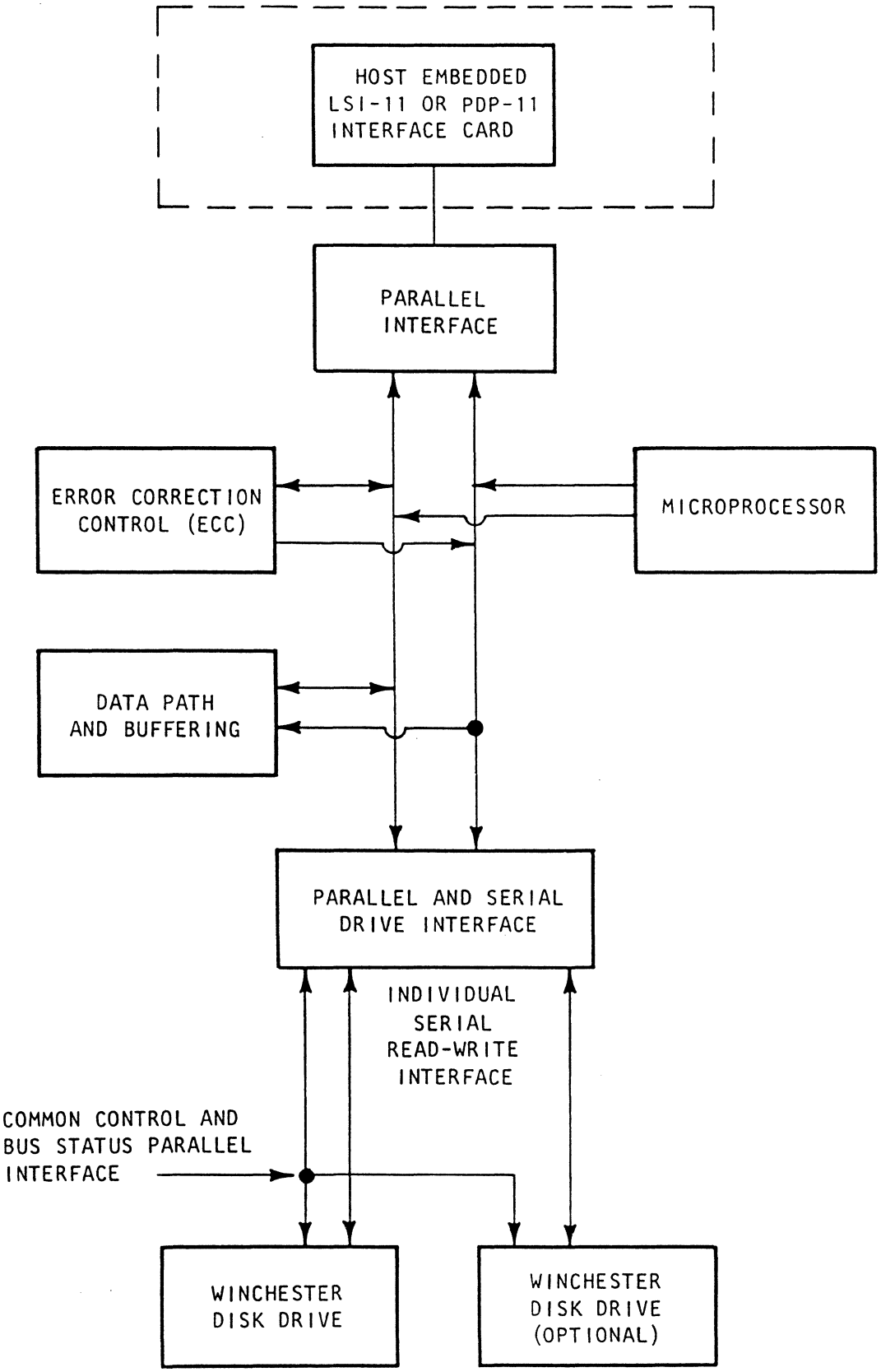


Figure 1-1. Typical WINC-08 Functional Block Diagram

1.4 DEFINITION OF AVAILABLE CONFIGURATIONS

The standard versions of WINC-08 are shown in Figure 1-2 and described below.

a. Single WINC consists of one WINC-08 controller and one Winchester disk drive interfaced to either an LSI-11 or a PDP-11; this emulates two RL02 drives.

b. Double WINC consists of one WINC-08 controller and two Winchester disk drives interfaced to either an LSI-11 or a PDP-11; this emulates four RL02 drives.

c. WINC/FLEX consists of one WINC-08 controller with one Winchester disk drive and one FLEX-02 controller with one floppy disk drive; this emulates two RL02 drives and one RX02 drive.

1.5 EMULATION CHARACTERISTICS

1.5.1 RL02 EMULATION

RT-11 or RSX-11M software transparency is achieved by two fundamental WINC design features:

a. The WINC firmware specifically emulates the RL02 disk system.

b. The dual 8-inch Winchester drives controlled by the WINC-08 have RL02-compatible formats with individual capacities of 20.8 megabytes per drive (23 megabytes per drive unformatted).

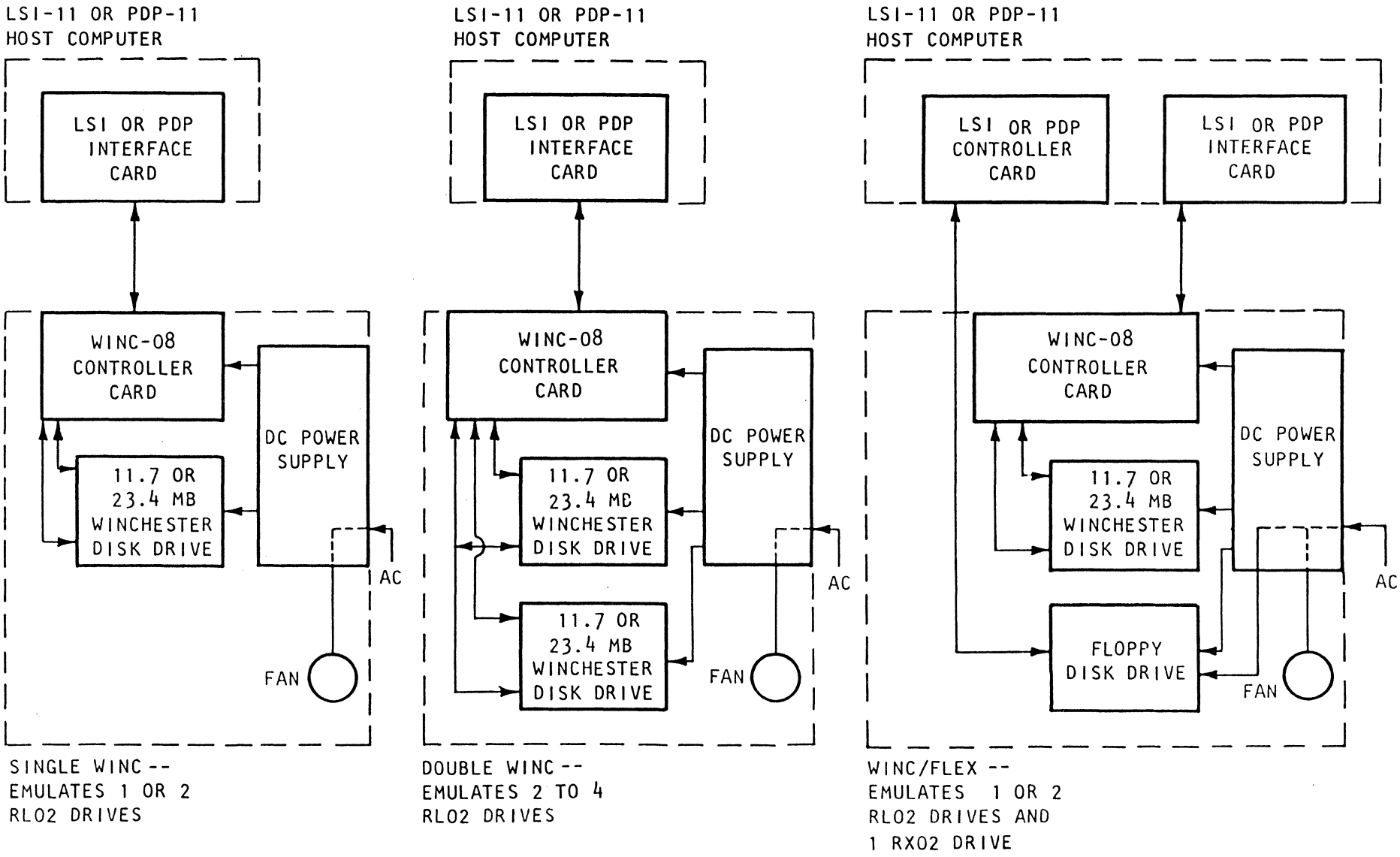


Figure 1-2. WINC-08 Standard Configurations

Note

A 10.4-megabyte Winchester disk drive is also supported by the WINC-08, but this unit is not available through AED.

1.5.2 RX02 EMULATION

The substitution of the second 8-inch Winchester drive with an 8-inch floppy disk drive allows DEC RX02 emulation. This floppy disk drive, attached to the AED FLEX-02 controller, emulates the RX02; the dual head of the floppy disk drive allows storage capacity of one megabyte per diskette. The format of the diskette is compatible with that of the RX01, RX02, or RX03 (double sided RX02).

1.6 SUPPLIED SOFTWARE

AED diagnostic programs are supplied on the Winchester drive or on a FLEX-02 diskette. If the WINC-08 controller is purchased separately, the diagnostic routines must be purchased separately from AED with RX01 or RX02 format specified. All AED diagnostics operate under the RT11 operating system. The RT11 operating system is not provided.

The diagnostic routines consist of:

a. Winchester media intitialize

b. ECC diagnostic

c. Data diagnostic

1.6.1 INITIALIZATION

Before the WINC-08 Winchester drives or the floppy diskettes may be used, they must be initialized with header information and data fields. Winchester drives received from AED will be preinitialized. Winchester drives not received from AED should be initialized using the initialization program described in paragraph 3.3 of this manual.

1.6.2 DATA DIAGNOSTIC (WINCHESTER) -- RLMFD

This diagnostic routine writes and checks data on the disk and is used to verify data integrity of the entire system, including media if desired. Complete information on the data diagnostic routine is presented in paragraph 4.4.

1.6.3 DATA DIAGNOSTIC (FLOPPY DISK)

The DEC diagnostic program (vendor no. #ZRXDA0.BIC) will run without modification on the FLEX-02 controller. Refer to the DEC User's Guide for operating instructions on this program. Additional information on the floppy disk data diagnostic is given in paragraph 4.6.

1.6.4 ECC DIAGNOSTIC (WINCHESTER DISK) -- RLMFC

The WINC-08 error correction code (ECC) diagnostic routine forces the disk sectors to contain data errors such that the ECC logic may be exercised and tested. Complete information on the ECC diagnostic is covered in paragraph 4.5.

1.7 **WINC-08 SPECIFICATIONS**

WINC-08 specifications are presented in Table 1-1.

Table 1-1. WINC-08 Specifications

Physical:

Chassis size: 5.25" H x 17.62" W x 26.5" L
Weight: single drive -- 40 lb
double drive -- 55 lb
Mounting method: desk top or standard 19-inch rack

Electrical:

	System Configuration	
Input Voltage Range	Single Drive	Dual Drive
100 or 115 VAC	157 watts	248 watts
50 or 60 Hz, Single Phase	1.19 amps	1.83 amps
200 or 230 VAC	157 watts	248 watts
50 or 60 Hz, Single Phase	0.60 amps	0.92 amps

Environmental:

Temperature
Operating: 41° through 113°F (5° through 45°C)
Maximum gradient is 10°C/hour
Non-operating: -40° through 140°F (-40° through 60°C)
Maximum gradient is 50°C/hour
Humidity: 20% through 80% R/H
Altitude:
Operating: 12,000 feet (3,700 meters) or below
Non-operating: 43,000 feet (12,900 meters)

1.8 DISK DRIVE SPECIFICATIONS (FLOPPY)

Floppy disk drive specifications are presented in Table 1-2.

1.9 DISK DRIVE SPECIFICATIONS (WINCHESTER)

Winchester disk drive specifications are presented in Table 1-3.

1.10 QUALITY ASSURANCE

At AED, quality and reliability stand as major objectives, supported and promoted throughout all levels of management and production. Quality controls meet or exceed industry and government standards and requirements. AED treats product quality as a matter of policy and of pride.

Product quality is not considered as solely a function of inspection and control; it underlies all policies, procedures, and management responsibilities. The complete quality program encompasses all management systems from product conception and planning through shipment and post-shipment support.

The formal quality assurance policy is documented in AED's Quality Assurance Manual. Additional information on AED's quality standards is available from AED.

Table 1-2. Disk Drive Specifications (Floppy)

Capacity (formatted)	1.0 Mbyte
Heads	2
Tracks	77
Sectors/track	26
Bytes/sector	256
Avg rotational latency	87 ms
Positioning times:	
minimum	18 ms
average	91 ms
maximum	243 ms
DMA transfer rate (peak)	64 Kbytes/s
Net throughput	18.3 Kbytes/s

Table 1-3. Disk Drive Specifications (Winchester)

	11.7 Mbyte Drive	23.4 Mbyte Drive
Total formatted capacity	10.4 Mbyte	20.8 Mbyte
Mapping emulation	1 ea. RL02	2 ea. RL02
Number of platters	2	4
Number of heads:		
R/W	4	8
clock	1	1
Number of cylinders	244	244
Tracks/cylinder	4	8
Sectors/track	42	42
Bytes/sector	256	256
Recording density	6100 BPI	6100 BPI
Recording density	MFM	MFM
Transfer rate (peak)	593 Kb/sec	593 Kb/sec
Net throughput	219 Kb/sec	219 Kb/sec
Track density	195 TPI	195 TPI
Rotational speed	2964 rpm	2964 rpm
Avg rotational latency	10.1 ms	10.1 ms
Positioning time:		
minimum	30 ms	30 ms
average	70 ms	70 ms
maximum	140 ms	140 ms

Section 2

INSTALLATION

2.1 GENERAL

Installation of your WINC-08 controller is simple and straightforward. It is designed for either desk-top or standard 19-inch rack mounting. As shipped from the factory, it is supplied with four rubber feet. When the supplied rubber feet are installed on the bottom of the WINC-08, it is ready to be set on a desk for installation.

For rack mounting (without chassis slides), the top/sides assembly is fastened to the rack. This forms a shell from which the base/back assembly -- which includes the drives, power supply, and AC wiring -- slides in or out of the top/sides assembly for servicing. Step-by-step rack mounting instructions are included in this section.

2.2 SITE REQUIREMENTS

The area intended for operation of your WINC-08 controller should be clean and well ventilated. Ambient temperature during operation should range from 41° through 113°F (5° through 45°C) and humidity should be 20% through 80% R/H. Altitude operating limits are from zero to 12,000 feet (to 3,700 m). Power to the WINC-08 controller must be single-phase, three-wire AC. The WINC-08 power requirements are as follows:

a. Voltage: 100 VAC or 115 VAC
200 VAC or 230 VAC

b. Frequency: 60 $\pm$3 Hz or 50 $\pm$3 Hz

c. Current:

	Single Winchester	Double Winchester	Winchester and Floppy
(100 or 115 VAC)	1.2 A max.	1.8 A max.	1.7 A max.
(200 or 230 VAC)	0.6 A max.	0.9 A max.	1.3 A max.

2.3 UNPACKING

The carrier is responsible for damage incurred during shipment. In case of damage, have the carrier note the damage on both the delivery receipt and the freight bill, then notify your AED customer service representative so that the necessary insurance claims can be initiated.

After opening the shipping container, use the packing slip to verify receipt of the individual items listed on the slip. Retain the shipping container and packing material for possible later reuse should return of the equipment to the factory be necessary.

Initial inspection of the WINC-08 is as follows:

a. Located on the rear panel is a black and white foil tag containing the unit configuration number, unit serial number, and unit power requirements. Verify that the power requirements of the unit match those that were ordered.

b. Set the WINC-08 unit on a flat, nonabrasive work surface.

c. Remove the ten screws securing the top cover assembly and remove the top cover for inspection of the interior.

d. Grasp the front panel (bezel) and pull it away from its snap-on fasteners.

CAUTION

Movement of the front panel is limited by the attached wiring cable.

e. Disconnect the cable connector to free the front panel (bezel) (see Figure 2-1f).

f. Verify that the WINC-08 drive(s) head locking mechanism is engaged, i.e., that the white nylon arm is in the right most position as shown in Figure 2-1b.

g. If WINC/FLEX configuration, verify that the cardboard shipping diskette is in place for double-sided floppy drives.

h. Look for any loose hardware that may have resulted from shipping shock and vibration.

i. Apply finger pressure to each connector to ensure that the cable connectors are firmly seated.

j. Raise the controller board around its hinged edge to gain access to the power supply board below.

k. Inspect for loose hardware or connectors on or near the power supply board.

l. Replace the top cover and its screws except for the two screws at the top rear, but leave the front panel (bezel) detached.

2.4 PHYSICAL INSTALLATION

With the WINC-08 unit unpacked and the initial inspection completed, proceed with the physical installation.

2.4.1 RACK MOUNTING

The WINC-08 is designed to mount in a rack that is 19 inches wide, 26 inches deep, and 5-1/4 inches high. Figures 2-1a through 2-1f illustrate the rack mounting procedure.

CAUTION

The head locking mechanism should remain in the "LOCKED" position during mechanical and electrical installation.

Step 1. Remove four screws and lock washers from the back panel. Save the screws and lock washers for later use (see Figure 2-1a).

Step 2. Turn the unit upside down on a nonabrasive surface. Remove the six screws holding the baseplate (see Figure 2-1a).

Step 3. Turn the unit upright and slide the base/back assembly out of the top/sides assembly (see Figure 2-1b).

Step 4. Two side rail extensions are provided in the accessory kit. Attach a side rail extension to each side of the top/sides assembly with the eight screws provided, but leave the screws loose (see Figure 2-1c).

Step 5. Install the top/sides assembly in the rack using four screws each in front of rack (see Figure 2-1c).

Step 6. Install four screws attaching the rail extensions to the rear of the rack. Adjust the length of the two rail extensions by extending or closing them until the length of the side rails matches the rack (front to rear) as shown in Figure 2-1c. Tighten all rail extension screws.

Step 7. Slide the base/back assembly into the top-sides assembly, making sure that the flat cable(s) is (are) routed over the top edge of the back panel in the groove provided (see Figure 2-1d).

Note

The topmost cable should be the WINC-08 cable. The optional bottom cable should be the FLEX-02.

Step 8. Install four screws from the rear of the racks as shown in Figure 2-1e. Attach the AC power cord to the WINC-08.

Note

DO NOT plug in the power until the Signal Interconnect flat cables have been connected to their associated interface cards as described in Section 2.6.

Step 9. Move the head locking mechanism(s), at the front of the WINC-08, to the "FREE" position (see Figure 2-1f).

Connect the front panel cable and push the front panel (bezel) onto its snap fasteners (see Figure 2-1f).

CAUTION

The head locking mechanism should be returned to the "LOCKED" position whenever

the system is to be moved. The heads must be at track 0 to allow the locking mechanism to hold the heads from movement. The heads are moved to track 0 by either a SEEK TO ZERO or by issuing a BUS INIT signal. See paragraph 3.2. NEVER move the drive heads when the disk is not spinning.

Step 10. Remove the cardboard "shipping" diskette on units equipped with the double-sided floppy option.

CAUTION

Failure to remove this cardboard protector could result in damage to the drive motor after power on.

2.5 ELECTRICAL INSTALLATION

2.5.1 AC POWER CONNECTION

The WINC-08 requires a single phase, three-wire AC power source as described in paragraph 2.2. The WINC-08 comes equipped with a detachable AC power cord.

2.5.2 SYSTEM GROUND

A single-point grounding scheme should be used to minimize ground loop problems. Figure 2-2 represents a typical single-point ground for a single-CPU system.

The common ground point, to which individual equipment grounds are connected, should be located electrically close to the building ground, which is typically available at the main power distribution panel.

(BOTTOM REAR VIEW)

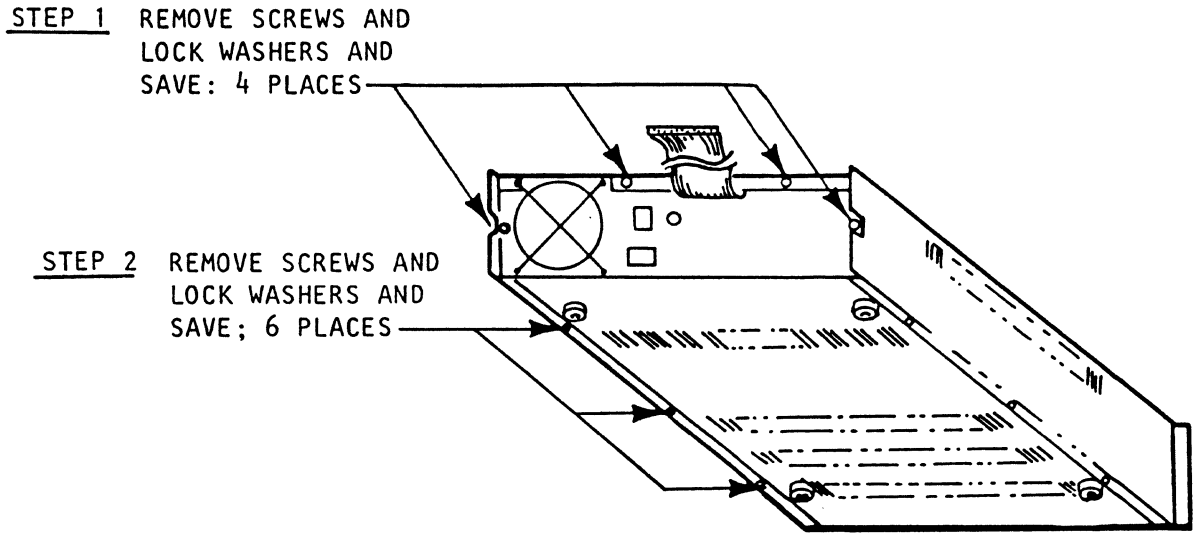


Figure 2-1a. Removal of Top/Sides Assembly

STEP 3

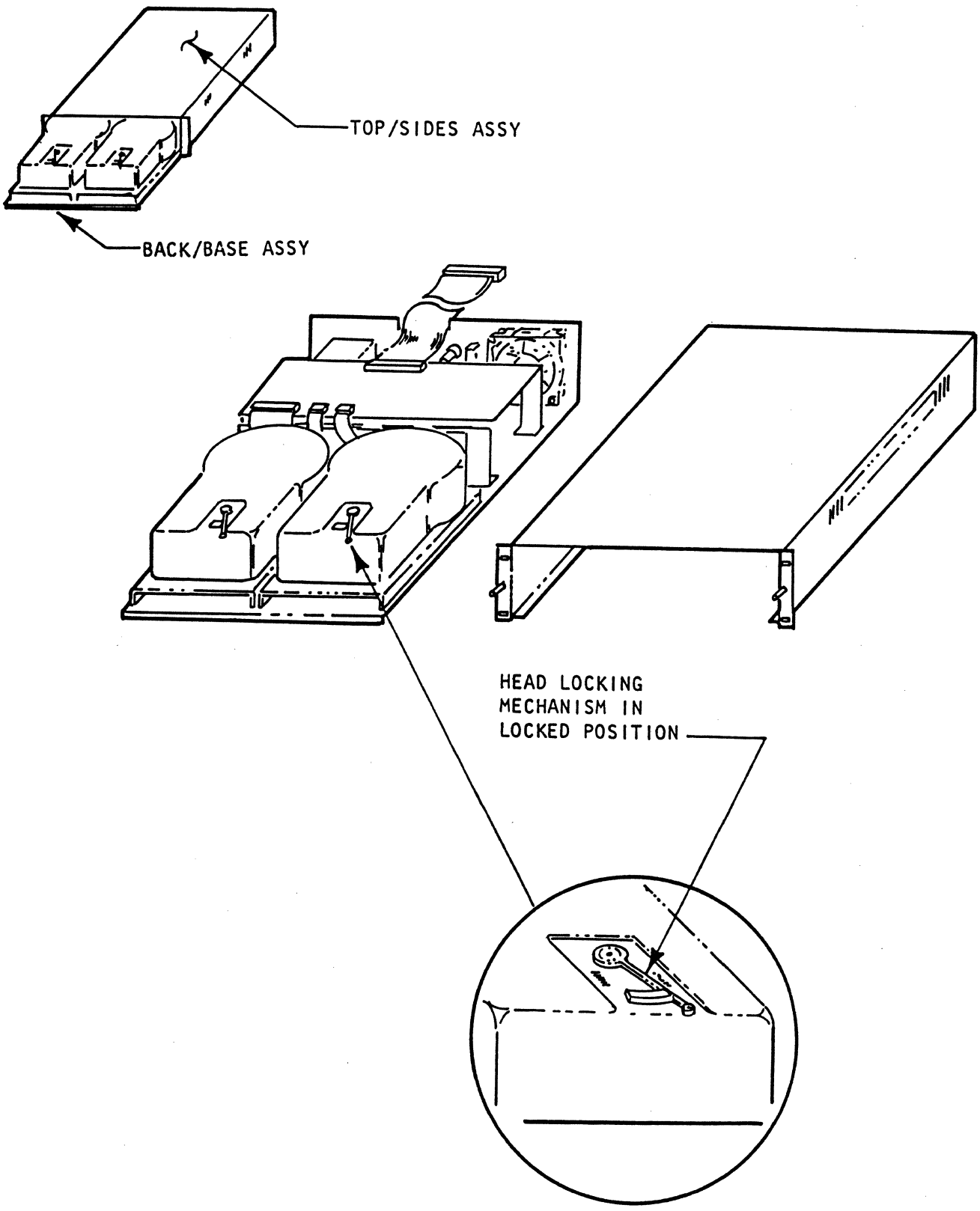


Figure 2-1b. Winchester Drive Head Lock Mechanism

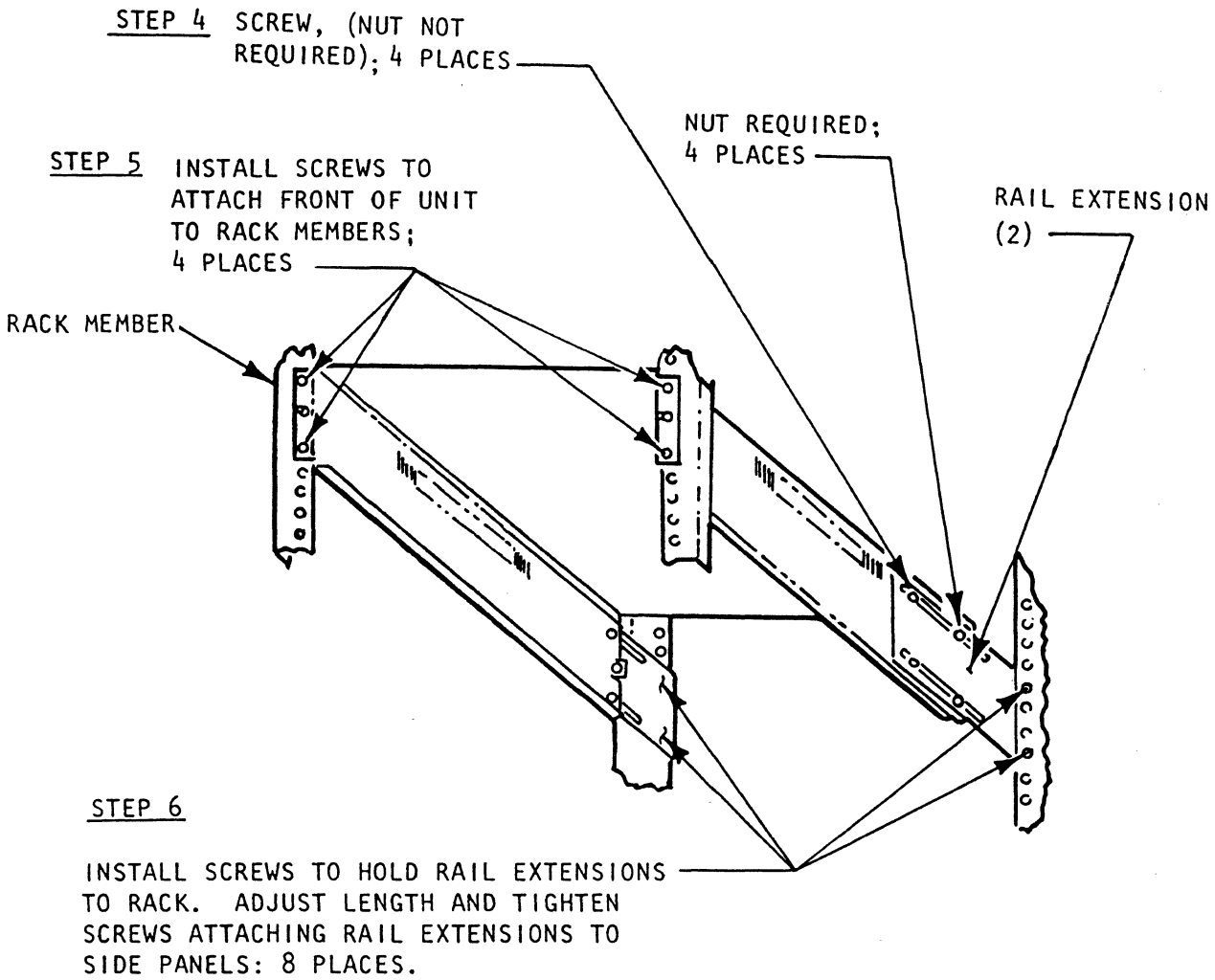


Figure 2-1c. Rack Installation

STEP 7

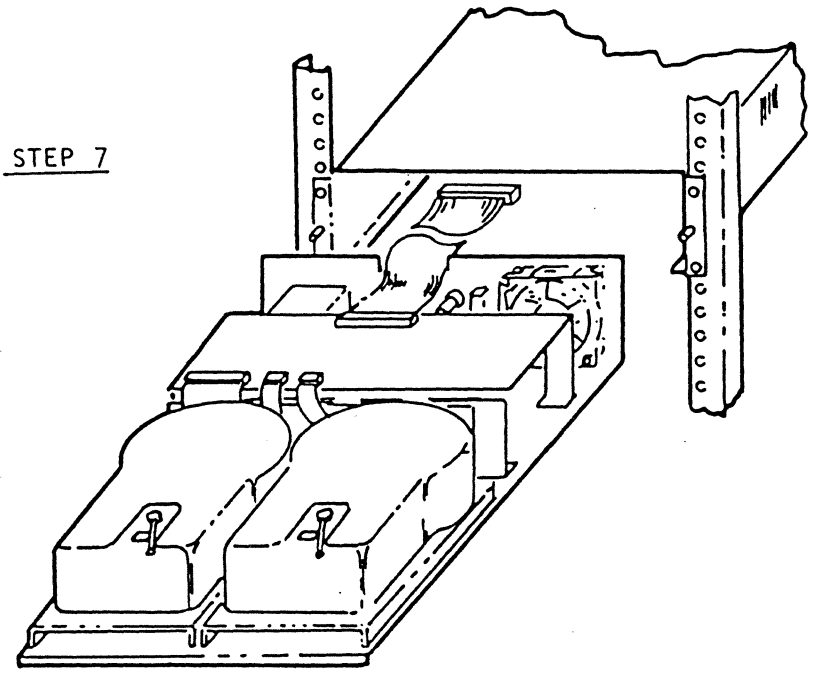


Figure 2-1d. Assembly into Top/Sides

STEP 8

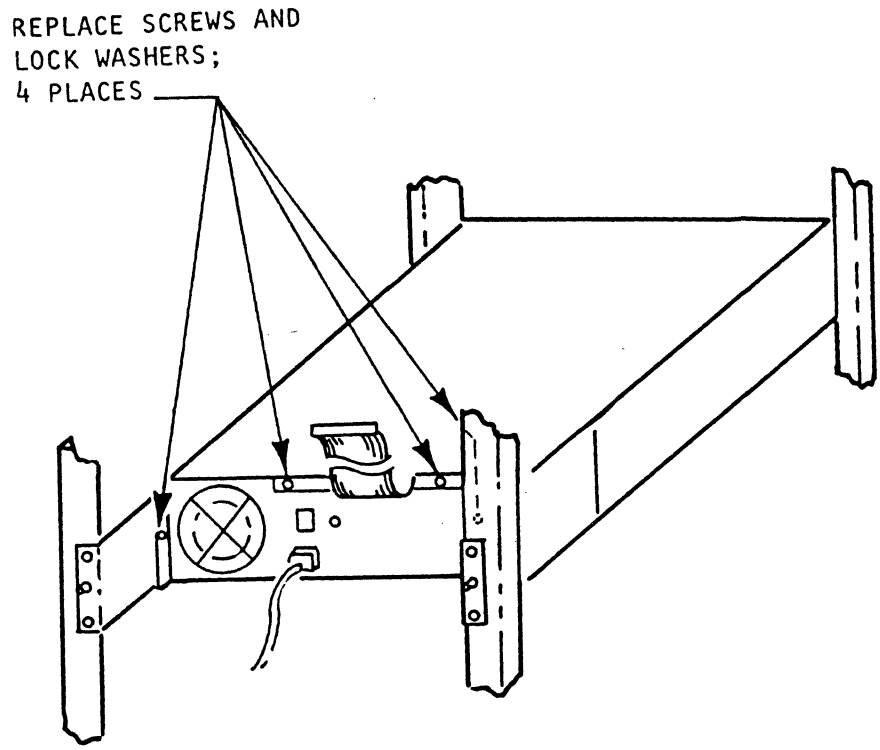


Figure 2-1e. Top/Sides Installation

STEP 9

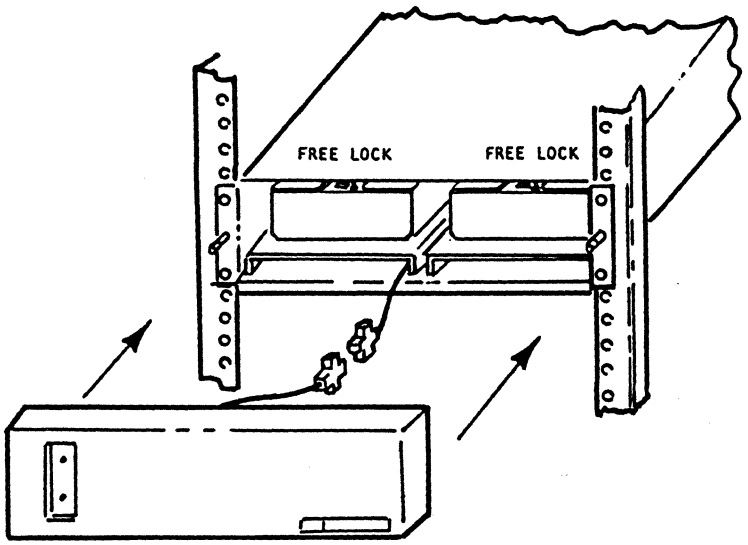


Figure 2-1f. Front Panel Installation

If the CPU is rack-mounted and if a good electrical connection between the CPU ground and the rack mount can be ensured, then a support rail attachment point may be used as the single-point ground. In such a system, all grounds (from controllers and drives and power supplies) should be returned to this single-point ground, thereby minimizing ground currents. The same single-point grounding system, shown in Figure 2-2, applies to desk-top system.

2.6 SIGNAL INTERCONNECTION TO HOST

There will be one or two flat cables between the WINC-08 unit and the host computer, depending on the mix of Winchester and floppy disk drives used in the particular configuration. Table 2-1 lists the various connections required for the standard configurations.

Table 2-1. WINC-08 Cable Configuration

WINC-08 Configuration	Number of Cables to Host Computer
One or two Winchester drives	One cable from WINC-08 to the host-imbedded interface card.
One Winchester drive and one floppy drive	Two cables from WINC-08. The top cable to the host-imbedded interface card and the bottom cable to the floppy drive's host-imbedded FLEX-02 controller card.

2.7 WINC-08 TO PDP-11 HOST INSTALLATION

2.7.1 PDP-11 INTERFACE CARD MODIFICATION INSTRUCTION

The interface card to connect the WINC-08 to the PDP-11 host computer (AED part no. 120068-01), is shown in Figure 2-3. As supplied, this

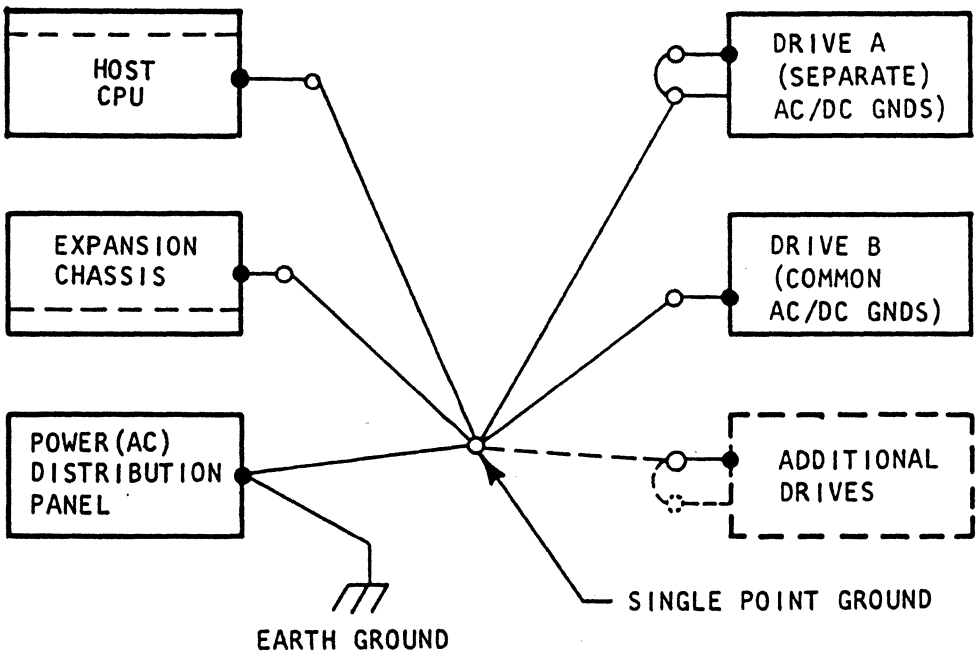


Figure 2-2. System Grounding Diagram

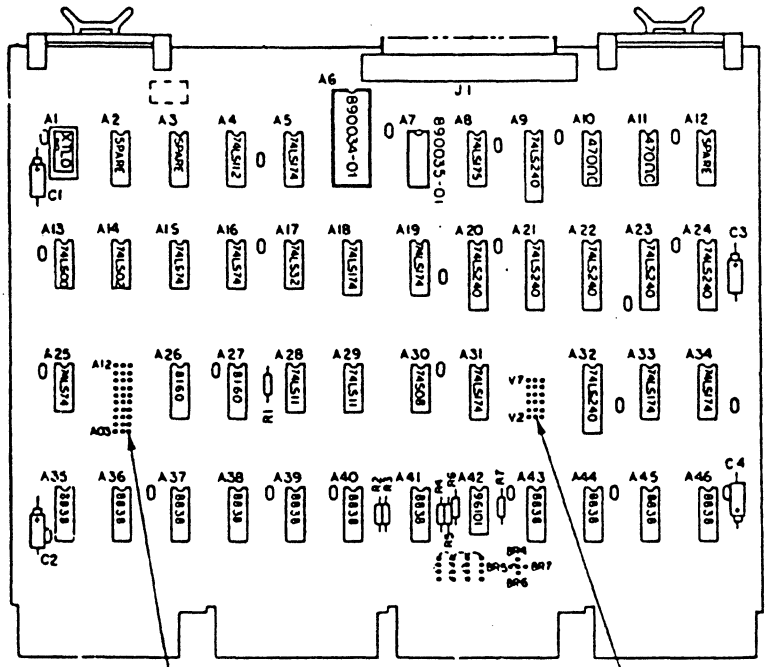


Figure 2-3. PDP-11 Interface Card

card is set for the standard Device Address and Interrupt Vector Address and for most applications will be used in this configuration. If the Device and Interrupt Vector Addresses used are not standard, they may be altered as described below. If standard Device and Vector Addresses are used proceed to paragraph 2.7.2.

The standard Device Address bits are A0 through A17; A0, A1, and A2 are factory-set to 0, and bits A13 through A17 are factory-set to 1. Device Address bits A3 through A12 are user-selectable, and are preset at the factory to the standard DEC configuration as shown in Figure 2-4.

Interrupt Vector Address bits V0, V1, and V8 are factory-set to 0 and are not user-selectable. Bits V2 through V7 are user-selectable and are preset at the factory to the standard DEC configuration as shown in Figure 2-4.

The Interrupt Priority Level is set for level 5 on the PDP-11 Interface board. It is selectable for levels 4 through 7. If the user finds it necessary to change the priority level the following steps must be followed:

a. Refer to the PDP-11 Interface card and Figure 2-5. On the lower right hand corner of the board, the etch between BR and BR5 must be cut.

b. Connect a jumper from BR to the desired priority level (BR4 through BR7).

c. Cut the connection between BG0 and G50.

d. Cut the connection between BG1 and G51.

e. Connect a jumper between BG0 and the desired level (G40 through G70).

DEVICE ADDRESS: PLUG SELECTABLE FROM 760,000 TO 777,777 OCTAL, IN FOUR WORD INCREMENTS

STANDARD OCTAL DEVICE ADDRESS:

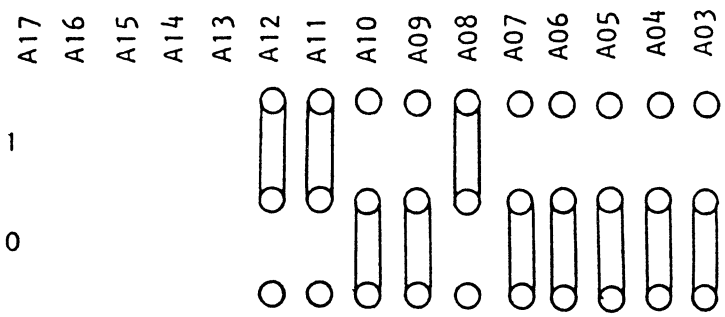
7	7	4	4	0	0

SET					SELECTABLE										SET		
1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0

STANDARD BINARY DEVICE ADDRESS:

PCB LABELING:

SHORTING PLUG PLACEMENT:



VECTOR ADDRESS: PLUG SELECTABLE FROM 000 TO 377 OCTAL, IN TWO WORD INCREMENTS

STANDARD OCTAL VECTOR ADDRESS:

1	6	0

SET		SELECTABLE						SET
0	0	1	1	1	0	0	0	0

STANDARD BINARY VECTOR ADDRESS:

PCB LABELING:

SHORTING PLUG PLACEMENT:

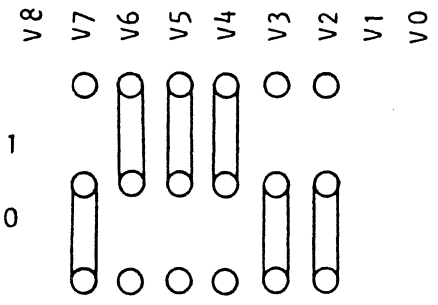


Figure 2-4. WINC-08/PDP-11 (Unibus) Interface

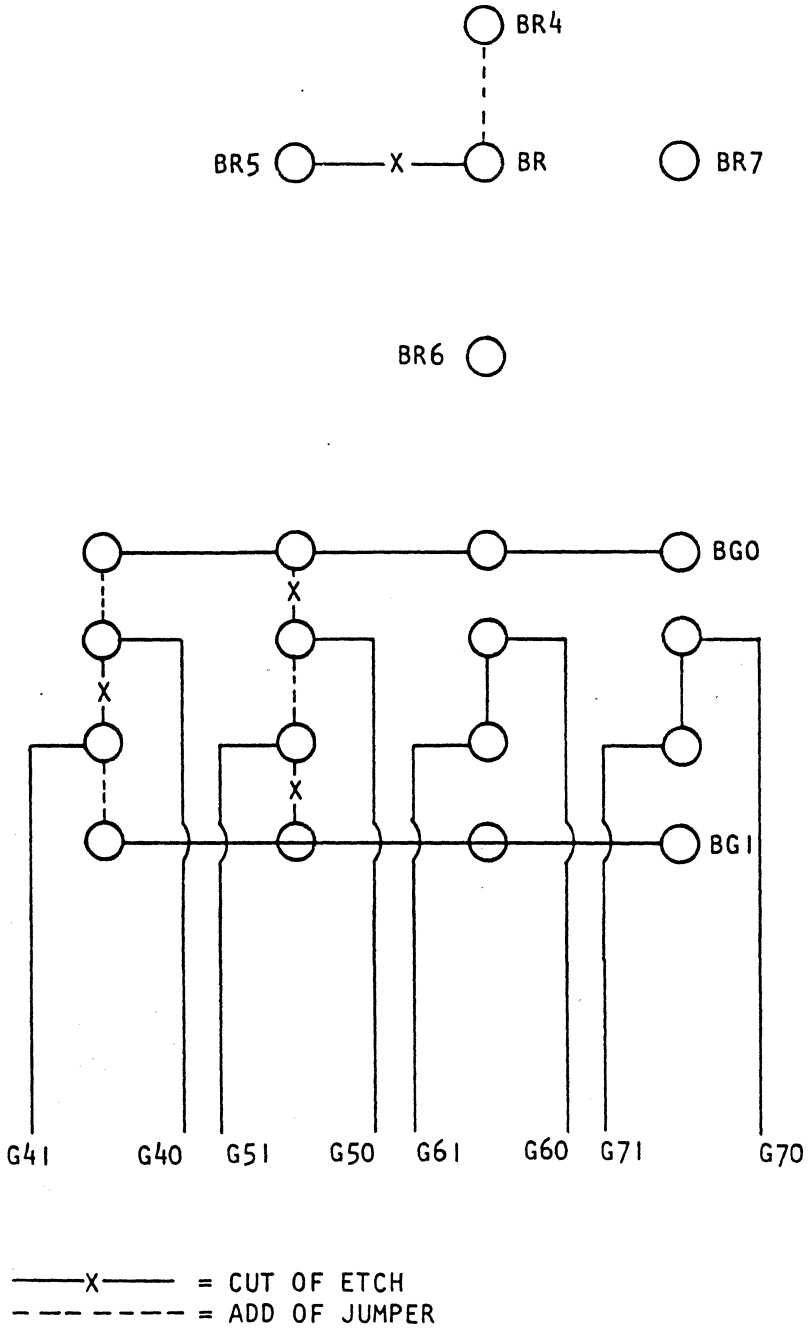


Figure 2-5. PDP-11 Interrupt Priority Level Jumpers

Note

Cable connectors are not keyed, therefore, it is necessary to identify the Pin 1 position on both the male and female plug connectors by means of the imprinted arrow on the top edge of each connector. The flat cable also identifies pin 1 by a red stripe. When connecting the plugs, these arrows (pin 1) must be aligned to ensure correct pin and circuit connections.

e. Connect the WINC-08 cable to its mating interface card connector, observing the arrow alignment requirement as mentioned in the above note.

f. Slide the PDP-11 chassis back into its rack mount, being careful not to tangle or distort the flat cable excessively.

g. Turn on the power to the host.

h. Plug in the WINC-08 AC power cord and place ON/OFF switch in ON position.

Note

Power to the WINC-08 and host should be applied simultaneously. If power is applied separately the WINC-08 should be the last unit to receive power.

j. Proceed with the software installation (see Section 3).

f. Connect a jumper between BGI and the desired level (G41 through G71).

g. Cut the connection between the desired GX0 and GXI level (G40 to G41, G50 to G51, G70 to G71).

h. Connect desired GX0 to the desired GXI. Figure 2-5 shows the changes required to change priority to level 4.

2.7.2 PDP-11 (UNIBUS) INSTALLATION

Standard installation instructions for the PDP-11 Unibus are as follows:

a. Remove power from the system.

b. Slide the PDP-11 chassis to its outermost position. This exposes the card slots located on the left hand side of the PDP-11 chassis, as viewed from the front.

c. Insert the WINC-08 Unibus interface card into the next available quad-wide small peripheral controller (SPC) slot. The WINC-08 is a DMA device so the Nonprocessor Grant Signal (NPG), wired to the SPC slot, must be broken. Break the connection (using a wire-unwrap tool) between pin CA1 and CB1 on the back panel corresponding to the slot in which the WINC-08 interface card resides (see Figure 2-6).

d. Route the WINC-08 flat interconnect cable through the chassis and rack members to enable it to be connected to the edge card connector on the Unibus interface card without severe twisting or bending of the flat cable.

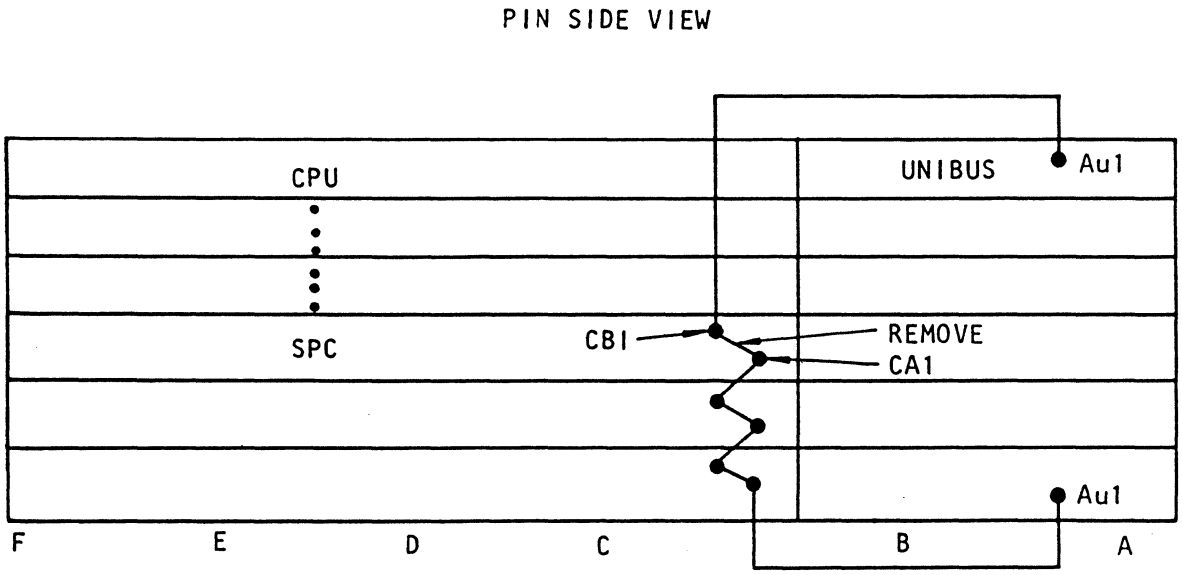


Figure 2-6. Removal of Nonprocessor Grant Signal

2.8 WINC-08 TO LSI-11 INSTALLATION

2.8.1 LSI-11 INTERFACE CARD MODIFICATION INSTRUCTIONS

The LSI-11 interface card is supplied with the standard DEC address, vector, and interrupt priority. Contact AED if modifications are required.

2.8.2 LSI-11 (Q-BUS) INSTALLATION

One WINC-08 flat cable is supplied with its respective LSI-11 interface card for configurations with one or two Winchester disk drives. If a floppy disk is supplied, perform the following installation steps for the Winchester and see paragraph 2.9 for the floppy disk drive installation.

a. Turn off the host computer (LSI-11) power supply.

b. Remove the LSI-11 front bezel (pull straight out on bezel). See Figure 2-7.

c. Plug the WINC-08 dual wide interface card (see Figure 2-8) into the next available dual wide slot (either left or right hand).

d. Connect the Q-bus (flat cable) from the WINC-08 to the edge connector on the Q-bus interface card.

Note

Cable connectors are not keyed, therefore, it is necessary to identify the pin 1 position on both the male and female plug connectors by means of the imprinted arrow on the top edge of each connector. The flat cable also identifies pin 1 by a red

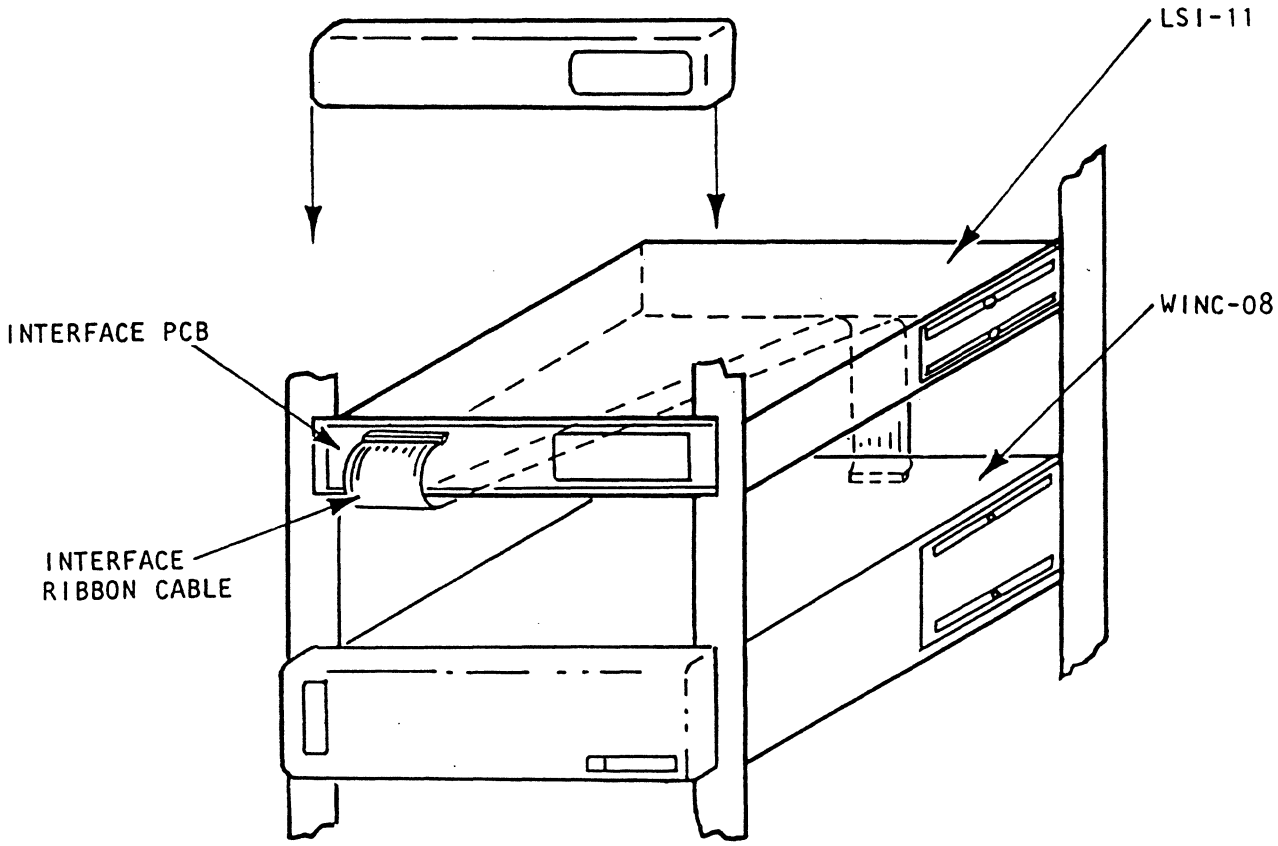


Figure 2-7. LSI-11 Installation

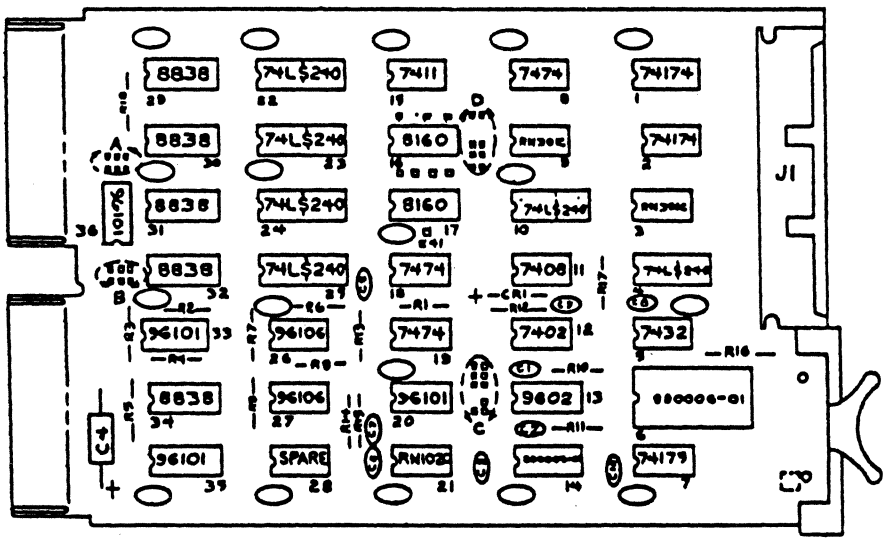


Figure 2-8. LSI-11 Interface Card

stripe. When connecting the plugs, these arrows must be aligned to ensure correct pin and circuit connections.

e. Proceed with paragraph 2.9 (FLEX-02 Installation) if you have a floppy disk drive. If you do not have a floppy proceed to the next step.

f. Replace the LSI-11 front bezel.

g. Turn on the LSI-11 power supply.

h. Plug in the WINC-08 AC power cord and place ON/OFF switch in ON position.

i. Proceed with the software installation (see Section 3).

2.9 FLEX CONFIGURATION JUMPERING AND FLEX-02 INSTALLATION LSI-11(Q-BUS)

The I/O address of the FLEX can be jumpered within the range of 160000 to 177774 (see Figure 2-9). Bits 15, 14, and 13 are factory set to 1, and bits 1 and 0 are factory set to 0. When shipped from AED, the standard I/O address of 177170 is set. The alternate address of 177150 is set as shown in Figure 2-9.

The interrupt vector and the bootstrap selection on the FLEX can be selected. The interrupt vector and Auto-bootstrap can be selected from a set of four as shown in Figure 2-10. Other vectors must be special ordered from AED. To inhibit the FLEX bootstrap, install a jumper from E13 to E14. If Auto-bootstrap is selected on the FLEX, then the CPU must be set for the bootstrap mode with power-up.

The bootstrap starting address is 173000. The bootstrap program occupies 512 bytes in the address range 173000 to 173776. All other bootstrap devices must be disabled when the FLEX-02 bootstrap is enabled.

The FLEX-02 is compatible with the LSI-11/23 four-level priority interrupt feature. It must be installed in the position-dependent configuration and can only be operated on priority level 4, as described in the LSI-11 microprocessor handbook.

a. Plug the dual-wide FLEX-02 controller card into the desired dual-wide slot (either left- or right-hand slot).

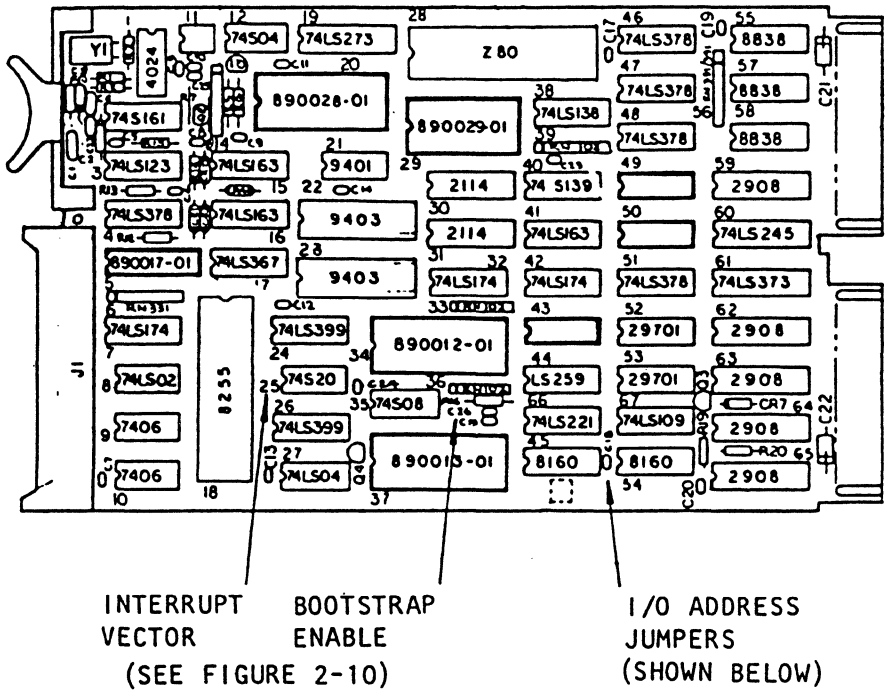
b. Connect the FLEX flat cable from the WINC-08 with a FLEX-02 unit to the edge connector of the FLEX-02 controller interface card.

> Note
>
> Cable connectors are not keyed, therefore, it is necessary to identify the pin 1 position on both the male and female plug connectors by means of the imprinted arrow on the top edge of each connector. The flat cable also identifies pin 1 by a red stripe. When connecting the plugs, these arrows must be aligned to ensure correct pin and circuit connections.

c. Proceed with paragraph 2.9 (FLEX-02 Installation) if you have a floppy disk drive. If you do not have a floppy proceed to the next step.

d. Replace the LSI-11 front bezel.

e. Turn on the LSI-11 power supply.



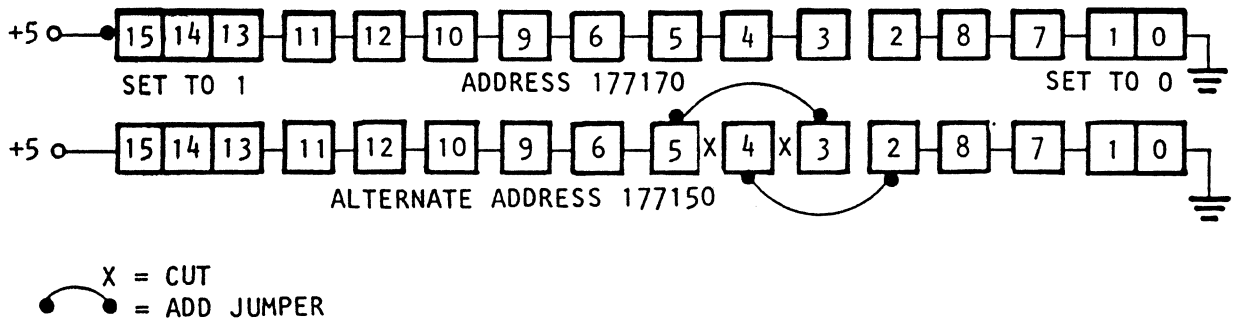


Figure 2-9. FLEX-02 Interface Card

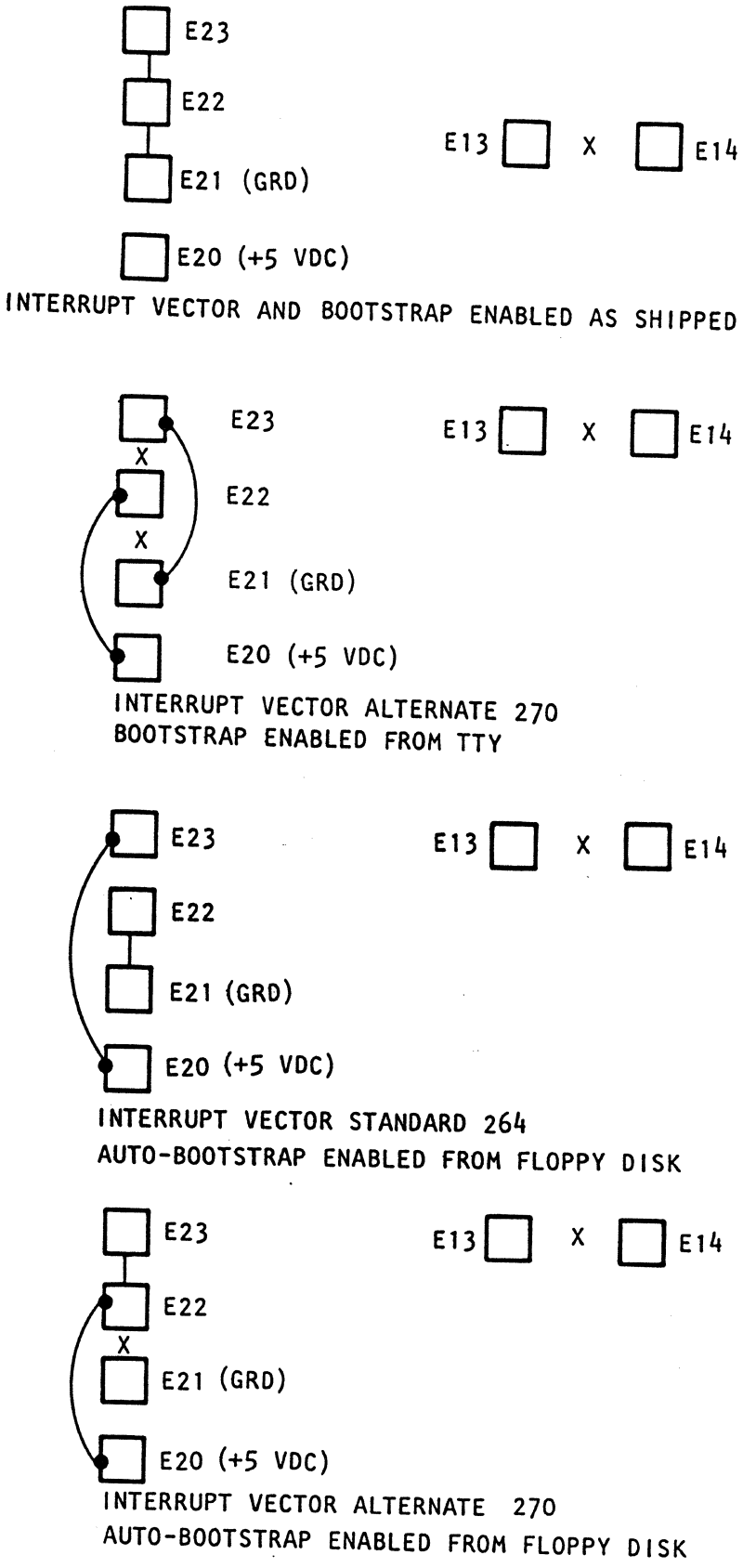


Figure 2-10. Interrupt Vector and Bootstrap Inhibit

f. Plug in the WINC-08 AC power cord and place ON/OFF switch in ON position.

g. Proceed with the software installation (see Section 3).

Section 3

SOFTWARE INSTALLATION

3.1 INTRODUCTION

After the WINC-08 is connected and the power is applied, software installation, including media initialization, may be performed. This section explains bootstrap operation and media initialization. Diagnostic operations are explained in Section 4. Media initialization and diagnostics are optional operations if the WINC-08 is received as a complete system, because these tasks have been performed at the factory.

Note

For WINC-08 operation a DEC-supplied DL driver must be a part of the user's Operating System. A SysGen is not needed if a loadable DL driver is used. Refer to DEC's Operating System manual for additional details.

The first phase of software installation is to verify the power-up sequence. When power is applied to the WINC-08, a power-up diagnostic will be executed to check the internal functions.

Microprocessor ALU operations and conditional branches are checked, and verification of the internal buffer follows. The WINC-08 then will attempt to become bus master, after which the controller and drive ready bits will be posted in the interface registers. After power is applied, the LED display for drive 0 should be lit. If no LED's are lit, refer to Section 4 for troubleshooting information. If the LED's for drive 0 and drive 1 are both lit, an error has occured in the unit. If an error is detected, the WINC-08 will trap and accept no other commands, and an error code will be posted in the internal LED display.

This internal LED display is located on the WINC-08 controller board. See Figure 3-1, which shows the controller board and the LED display.

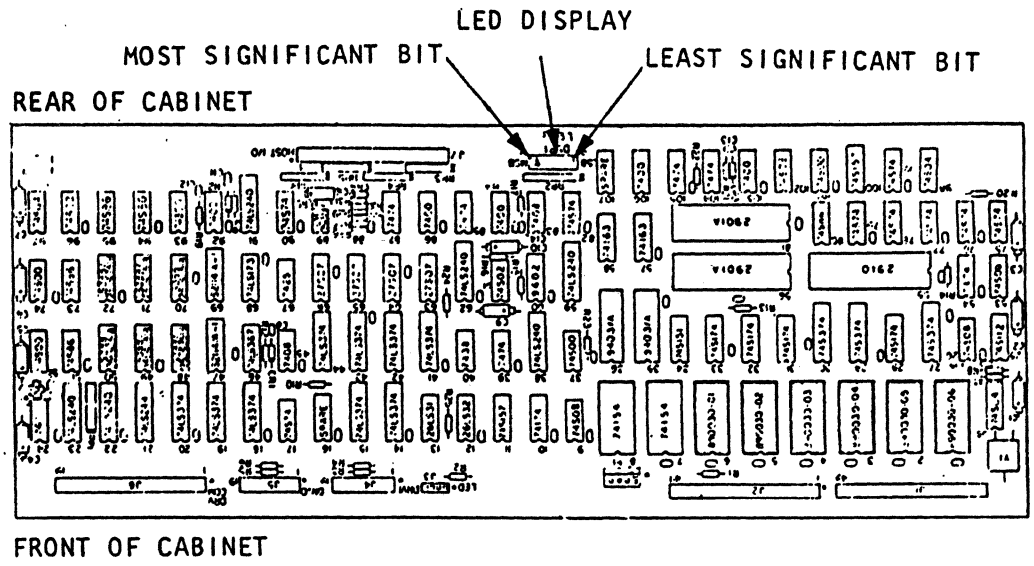


Figure 3-1. WINC-08 Controller Board with LED Display

The error codes, as displayed in the WINC-08 LED display (shown in Figure 3-1), are as follows:

Error Code (1 = LED lit) (0 = LED off)	Description
11000001	ALU or conditional test failure
11000010	FIFO status error
11000011	Buffer data/Address error
11000100	FIFO data error
11000101	Bus master error

The WINC-08 will remain in an error trap until a BUS INIT signal is received from the CPU, after which it will again attempt the power-up diagnostic tests. Section 4 of this manual contains troubleshooting information.

Following the power-up diagnostics, the WINC-08 will check to determine if the drives are up to speed; if they are, a rezero (restoring the heads to Track 0) will be issued. If the drives are not up to speed, the rezero will be postponed until the first seek command. On power-up, DRIVE ZERO will be selected and, when the drive is ready, the LED on the front panel of the WINC-08 will turn on.

3.2 BOOTSTRAP METHODS

The system can now be booted from any bootable device on the bus.

The WINC-08 will operate with any standard bootstrap procedure that is loaded onto the WINC-08. There is no bootstrap resident on the Winchester disk drives when shipped.

Note

A bootstrap is available with the FLEX-02.

The WINC-08 bootstrap may also be performed manually, using direct I/O commands.

First, generate a BUS INIT signal. With an LSI-11, this is done by storing a HALT instruction into location zero, then executing LOCATION ZERO as follows:

Enter		Display
BREAK KEY	(BREAK)	@ (prompt)
0/	(ZERO SLASH)	@ 0/04000_**0**
0 CR	(ZERO RETURN)	@ **0**/04000_**0**
0G	(ZERO G)	@ **0G**
--------	--------	@ 000002

On most PDP-11 (Unibus) systems, a BUS INIT signal can be generated by pressing an INIT switch.

3.2.1 EXAMPLE BOOTSTRAP FROM UNIT ZERO

The BUS INIT signal will cause the drives to rezero and the bus address, disk address, and word-count registers to be set to zero. Issuing a READ command will cause 40 sectors, starting with sector zero, from disk drive zero, to be read into memory. The memory is loaded starting from location zero and creates another BUS INIT signal, clearing the CSR ERROR STATUS.

For LSI to load the bootstrap program follow the procedure given below:

Enter		Display
774400/	(CSR ADDRESS SLASH)	@ **774400/00201**
14 CR	(READ COMMAND)	@ **774400/00201 14 CR**
0G	(ZERO G = START AT ZERO)	@ **0G**

This will return the title of the booted operating system and a prompt.

Usually, only sectors zero and one are needed (the others are read to avoid the requirement of setting the word-count register). In many systems, execution of an 0G (ZERO G) will result in a BUS INIT signal, which will clear the WINC-08 registers.

If a boot to a logical unit other than zero is required, the REGISTER CLEAR must be prevented. This may be done by setting the "PC" register and issuing a PROCEED request.

3.2.2 EXAMPLE BOOTSTRAP FROM UNIT TWO

For LSI Protocol only, generate a bus init signal, then:

Enter		Display
BREAK KEY	(BREAK)	@
0/	(ZERO SLASH)	@ **0/**040000
0 CR	(ZERO RETURN)	@ 0/040000_**0** (CR)
0G	(ZERO G)	@ **0G**
------	------	@ 000002
774400/	(CSR ADDRESS SLASH)	@ **774400/**000201
1014 CR	(UNIT NO. *256. + 14 RETURN)	@ 774400/000201_**1014**(CR)
/	(SLASH)	@ **/**113215_
0 CR	(ZERO RETURN)	@ /113215_**0** (CR)
$7/	(DOLLAR SIGN SEVEN SLASH)	@ **$7/**000002
0 CR	(ZERO RETURN)	@ $7/000002_**0** (CR)
P	(P)	@ **P**

This will return the title of the booted operating system and a prompt.

This sequence will read 40 sectors, starting at sector zero of disk drive two, and will then set the program counter to zero and start execution without creating a BUS INIT signal.

Note

In this sequence the BUS INIT signal, generated by the console "G" command, must be avoided as it will cause the WINC unit register to be reset to zero.

Some processors have a different console monitor or have only front panel switches. In these cases, equivalent sequences should be generated to match the examples given. A typical sequence would be as follows:

For PDP Protocol:

PRESS:	INIT SWITCH	(GENERATE BUS INIT)
ENTER:	L 774400 CR	(LOAD CSR ADDRESS)
ENTER:	D 14 CR	(ISSUE READ COMMAND)
ENTER:	L 0	(LOAD STARTING ADDRESS)
ENTER:	S	(START BOOTSTRAP)

Note

If a FLEX-02 is present, a bootable diskette may be used to boot the WINC-08 by entering the desired DY number.

3.2.3 FLOPPY DISK BOOTSTRAP METHODS

The FLEX-02 bootstrap starting address is 173000.

To boot from the FLEX-02, when power is applied and Autoboot is inhibited, perform the following:

Enter	Display
BREAK KEY	@
173000G	@ 173000G

This will return a $ prompt.

In this case enter the name of the drive where the boot resides.

Enter	Display
DY	$ DY

Note

DY0, DY1, DL0, DL1, DL2, DL3, or any other bootable device may be entered.

This will return the title of the operating system.

To boot from the FLEX-02 (after power is applied with Autoboot enabled) place a bootable diskette in Drive 0 and perform the following:

Enter	Display
BREAK KEY	@
173000G	@ 173000G

This will return the title of the operating system.

If the FLEX-02 Autoboot is enabled, the system will boot automatically from the floppy drive upon initial application of power and return the title of the operating system.

3.3 INITIALIZATION (RLMFV)

Before the WINC-08 drives may be used, the disk must be initialized by recording header information and data fields. Drives received from AED will be formatted and only an initialization of a directory is needed (i.e., INIT command). Drives not received from AED should be initialized using the program RLMFV.

3.3.1 RLMFV INTRODUCTION

The AED WINC-08 initialize-and-format routine (RLMFV) is used to write headers on the disk media and to fill-in and verify the data sectors; it places a record of any bad sectors in the bad block table at the end of the logical disk unit.

Note

RLMFV runs only under RT-11. It is assumed that RT-11 has been loaded into the CPU.

3.3.2 RLMFV DESCRIPTION

RLMFV starts execution by printing the program name and part number. The next operation is a request for more memory space to be used for the bad-block and data buffers. If there is not enough memory, a message is printed. To provide the greatest speed, RLMFV operates with a 40-sector buffer. With the buffers, RLMFV requires 18,000 words in addition to the memory required for the monitor.

Location 776 octal contains DEC's standard CSR address (774400). If an alternate CSR address is selected on the WINC-08 interface card, location 776 octal must be changed to reflect the selected address. The WINC-08 interrupt vector is not used by this routine.

The starting logical unit number is at octal location 764. This number is normally set to zero and can be changed by the user to 1, 2, or 3. The ending unit number is at octal location 774. This number must be changed to correspond to the last logical unit (DL) to be tested. Physical drive 0 is DL0 and DL1.

Once the memory buffers are set up, RLMFV issues a request for the

option. Options two, three, and four set a counter (or flag) and return to the option question. Options one and two first request the starting and ending unit numbers, then ask if the operator is sure; if so, they start the header-initialization or data-verification phase. Option one issues a format command to the WINC-08 to write data headers on the selected logical unit, which erases all data, and then proceeds with the data-verification phase.

Media verification is done one logical unit at a time. First, the bad-block buffer is filled to indicate no bad blocks, then the data buffer is filled with a 177376-octal (FE hex) data pattern. Each track is first written and writechecked. If there are no errors, the operation is repeated the specified number of times for each head and cylinder. When the last cylinder and head are reached, the bad-block data are written. The cylinder number is printed once each 32 cylinders up to the highest cylinder (244). The system will then display VERIFY DONE.

Whenever an error is detected, the sector causing the error is entered into the bad-block buffer unless the operation was a writecheck and the option was selected to enable ECC corrections. Then the sector in error is read into a scratch buffer and the data are compared byte by byte. If no error is detected due to a microcode ECC correction, the sector is considered acceptable and is not entered in the bad-block buffer.

Whenever a sector is entered in the bad-block buffer, a printout is displayed that shows the logical cylinder, head, and sector address. The WINC-08 hardware registers are displayed as well as the physical cylinder, head, and sector in error.

RLMFV allows up to 125 sector errors, after which no further entries will be made in the bad-block buffer. The program will continue to execute, however, and will continue to print additional errors as they are found. Only the first 125 errors will be available in the manufacturing portion of the bad-block file. The user portion will be

initialized to show no bad blocks. If desired, user utility may be generated to add sectors to the user portion of the bad-block file.

3.3.3 RLMFV EXECUTION

The initialize and verify program is started by typing:

ENTER: **R RLMFV**

The program will be loaded, and execution will start at location 1000 octal. RLMFV requires about 18 K words of memory plus the operating monitor (RT-11).

The program will identify itself with the following message:

```
AED WINC-08 INITIALIZER.  (800004-01 REV. A)
ENTER OPT  (OR?)
```

The user then may enter a question mark to have a list of the program options displayed on the screen, or a desired option may be entered. The available options are shown below:

OPT 0 -- Initialize Headers (Format)

This option will request a write to the logical units. It will completely format those units, writing headers and verifying the data sectors. Note that one of the two logical units on a physical drive may be initialized without affecting the other unit.

OPT 1 -- Verify Data Fields

This option will request a read from the logical units. It will skip the writing of the headers and perform the data-verify operation on the specified units.

OPT 2 -- Set Repeat Count

The program will normally write and writecheck each sector only one time. This option will print:

ENTER REPEAT COUNT

The number entered (1 to 32,767) will set a counter and then each sector must be repeated with a write and writecheck from 1 to 32,767 times without an error.

OPT 3 -- Set Error Limit

A bad sector is defined as any error detected after the write or writecheck operation. The default is to limit retries to those performed automatically by the microcode. The set error limit option, allows the user to remove the retry limit such that the program will attempt a read operation whenever a writecheck error is detected; if the read is successful, the sector will not be marked as bad. The following will be printed:

ENTER ERROR CODE (OR?)

The user may then enter an error code or a (?).

If a question mark is entered, the options will be displayed.

OPT 0 -- NO ERRORS ALLOWED

This is the writecheck-only mode.

OPT 1 -- ONLY CORRECTED ECC ERRORS ALLOWED

This is the mode that will not mark a sector as bad if the read

is successful.

Note

The writecheck operation performs retries but does not use the WINC-08 ECC capability. The writecheck operation may therefore detect errors that will be corrected with ECC and will not be reported when a read operation is performed.

OPT 4 -- SET INTERLEAVE

The WINC-08 data sectors may be interleaved by a factor of from 2 to 6 depending on system requirements. The interleave selected should be determined by the host CPU speed, memory speed, and system overhead. Most systems with reasonably fast CPUs and memory will be able to use an interleave factor of 2, allowing the WINC-08 to access every other sector during multiple-sector I/O operations. If the CPU "memory" or system overhead is too much for the selected interleave, the WINC-08 will miss sectors and will require extra revolutions, causing a dramatic reduction in system throughput. If this occurs, the interleave factor should be increased with this option which will allow additional time between sector accesses.

When this option is selected, the program will print:

INTERLEAVE FROM 2 to 6?

When the desired interleave (a number from 2 to 6) is entered, the program will echo the number and print the decimal number of the last sector on the first cylinder and head. This sector contains the extra bytes left over from the sector-byte counter roundoff.

OPT D -- DEBUG

This option is provided for service or other troubleshooting activities and operation of the debug routine is not covered in this manual.

Section 4

MAINTENANCE AND TROUBLESHOOTING

4.1 MAINTENANCE PHILOSOPHY

Preventive maintenance is not required on the WINC-08 unless a floppy disk drive is installed. Operator-performed preventive maintenance consists of cleaning the heads on the floppy disk drive each month. The procedure for cleaning the Read/Write heads is given on the package of commercially available cleaning kits. Corrective maintenance may be required if the diagnostic malfunctions.

In the event of a malfunction, review the list of possible symptoms described in this section and perform the suggested corrective actions. If a malfunction persists, AED offers a variety of service options which can be enacted by contacting the AED Service Department at either:

(West Coast)
Sunnyvale Service Center
(408)733-3555

or

(East Coast)
Chelmsford Service Center
(617)256-1700

4.2 TOOLS AND TEST EQUIPMENT

The only tools required for replacing a subassembly in the WINC-08 are common hand tools. A voltage meter is required to measure the output voltages of the power supply.

4.3 DIAGNOSTICS

Data and ECC diagnostics are provided with the WINC-08 to verify system operation. If available, the DEC RL02 Performance Exerciser Diagnostic may also be executed.

a. DATA DIAGNOSTIC -- The AED data diagnostic "RLMFD" may be used to check the data integrity of the system. An incremental data pattern is written, read, and verified on all sectors of the selected units (see Section 4.4.1 for details). A DEC diagnostic can be used for testing the data integrity of the floppy disk drive (see Section 4.6 for details).

b. ECC DIAGNOSTIC -- The WINC-08 Error Correction Code (ECC) may be verified using the "RLMFC" diagnostic. Refer to Section 4.4.3 for details of operation. Maintenance commands are used to force the data fields to contain errors so the WINC-08 correction capability may be checked.

4.4 DATA DIAGNOSTIC (WINCHESTER) -- RLMFD

This diagnostic writes and checks data on the disk and is used to verify the data integrity of the entire system, including media if desired.

4.4.1 RLMFD DESCRIPTION

When the program executes, it will write on logical unit zero and all data on that unit will be lost. The AED data diagnostic writes an incremental data pattern on all sectors of the unit. The diagnostic tests the writing, reading, and writecheck functions. The data is tested by microcode during the writecheck and by the host during read operations. When errors are detected, the bad block file is checked and if the sector in error is found, the error printout is skipped. If the sector is not found, a message is printed and the WINC-08 registers are

listed before the program jumps to the debug routine. Continuous looping or other debugging patches require the assembled source listing and use of the debug routine.

Location 776 octal contains DEC's standard CSR address (774400). If an alternate CSR address is selected on the WINC-08 interface card, location 776 octal must be changed to reflect the selected address. The WINC-08 interrupt vector is not used by this routine.

The starting logical unit number is at octal location 764. This number is normally set to zero and can be changed by the user to 1, 2, or 3. The ending unit number is at octal location 774. This number must be changed to correspond to the last logical unit (DL) to be tested. Physical drive 0 is DL0 and DL1. Remember that all data will be destroyed on the selected units without warning.

4.4.2 RLMFD EXECUTION

The data diagnostic is started by entering:

ENTER: R **RLMFD**

CAUTION

This routine does not request options or ask, "ARE YOU SURE?" Execution of RLMFD results in the immediate destruction of disk data.

The program will be loaded and execution will start at location 1000 octal. The program will identify itself by displaying:

RLMFD DISK DATA TEST (800004-01 Rev. B)

4.5 ECC DIAGNOSTIC -- RLMFC

The WINC-08 ECC diagnostic forces disk sectors to contain data errors such that the ECC logic may be exercised and tested.

4.5.1 RLMFC DESCRIPTION

This program writes a data pattern, then does a special read operation to fetch the ECC bytes. The program then changes some data bits and writes the "glitched" data with the original ECC bytes using a special write operation. The sector is then read and the complete data field is checked to verify that the "glitched" bits were properly corrected by the ECC logic and microcode. The program will cycle through one hundred times before returning to the system. If any error is detected, a message will be printed and the program will jump to the debug routine. Interpretation of the errors requires setting break points with the debug routine and examining the data buffers. A copy of the assembled program listing should be made before attempting the debug routine.

Location 776 octal contains DEC's standard CSR address (774400). If an alternate CSR address is selected on the WINC-08 interface card, location 776 octal must be changed to reflect the selected address. The WINC-08 interrupt vector is not used by this routine.

The starting logical unit number is at octal location 764. This number is normally set to zero and can be changed by the user to 1, 2, or 3. The ending unit number is at octal location 774. This number must be changed to correspond to the last logical unit (DL) to be tested. Physical drive 0 is DL0 and DL1.

Remember that all data will be destroyed on selected units without warning.

4.5.2 RLMFC EXECUTION

The ECC diagnostic is started by typing:

```
R RLMFC
```

The program will be loaded and execution will start at location 1000 octal. RLMFC will identify itself by typing:

```
RLMFC ECC TEST (800XXX-01 REV. A)
ENTER OPT (OR?)
```

Typing a question mark (?) will cause the options to be listed as follows:

OPT 0 -- Start test with default sector

Operation of RLMFC results in the writing of a "long" sector. To avoid erasing the header of the next sector, the long sector must be selected, which occurs during initialization. This sector is printed whenever the initialization program (RLMFV) is executed. For the normal interleave factor of two, the long sector is number 41, which is set as the default for the ECC test.

OPT 2 through 6 -- Set sector from interleave table

RLMFC contains a table of normal interleave factors and the corresponding long sector numbers. Entering a number from two to six will cause RLMFC to select the proper long sector from that table.

OPT 25 through 41 -- Select the ECC test sector

The interleave used by the initialization program may be changed by the user, or the user may wish to use a sector other than the long sector for debugging purpose. Sector numbers from 25 through 41 (decimal) may be entered to force RLMFC to use those sectors. Note

that the header of the following physical sector may be erased by using this option.

OPT D -- Go to debug

The debug option is provided for field service use or other troubleshooting activities. Operation of the debug routine is not covered in this manual.

4.6 FLOPPY DISK -- DATA DIAGNOSTICS

The DEC diagnostic program (vendor no. ZRXDA0.BIC) will run without modification on the FLEX-02 controller. Refer to the DEC User's Guide for operating instructions.

For the dual head floppy, supplied with the WINC-08/FLEX-02, a provision must be made for the second head.

With the DEC diagnostic program, the second head is tested as a separate unit from the first head. Testing a two-headed floppy is not explained in the DEC User's Guide. A sample dialog for this diagnostic for testing two-headed drives is shown in Table 4-1.

4.7 POWER SUPPLY CHECK

A procedure for checking and adjusting the +5 V, -12 V, and +24 V voltages from the power supply is as follows (refer to Figure 4-1):

a. +5 V is read (red wire) on the controller board at the DC connector and at the disk drive's DC cable.

b To adjust +5 V, place the red (+) lead from the meter on the red +5 VDC wire and the black (-) lead to the black DC wire (GND) as shown in Figure 4-1. Adjust meter reading to +5 VDC ($\pm$5%) using potentiometer shown in Figure 4-2.

Table 4-1. FLEX-02 Dual Head Floppy Data Diagnostics

DISPLAY	ENTER	COMMENTS
DS-B	START	Start test
UNITS?	2	2 heads on 1 drive
UN1 ADRS	CR	Use default address
VECTOR	CR	Use default vector
DRIVE	0 CR	Drive 0
EXPANSION	0 CR	Head 0
UN2 ADRS	CR	
VECT	CR	
DRIVE	0 CR	Drive 0
EXPANSION	1 CR	Head 1
CHANGE SWITCH?	Y CR	Yes
HELP?	Y CR	If desired
EXERCISE	3 CR	Or other; 3=write/read/compare
DATA PATTERN?	0 CR	Or other; 0=random data
TRACK SEQUENCE?	1 CR	Or other; 1=assending order
DOUBLE DENSITY?	Y CR	Double density
DELETED DATA?	CR	Default
FLAGS?	CR	
TRACK LIMITS	CR	Track 00-76
SECTOR LIMITS	Y CR	Specify limits
MIN	1 CR	Sectors 1 to 26; enter sector
MAX	26 CR	Min=1, max=1 to speed up test
FUTURE EXPANSION?	Y CR	Must be answered "Y" if any unit select expansion questions were answered "1"

(The diagnostic will begin running)

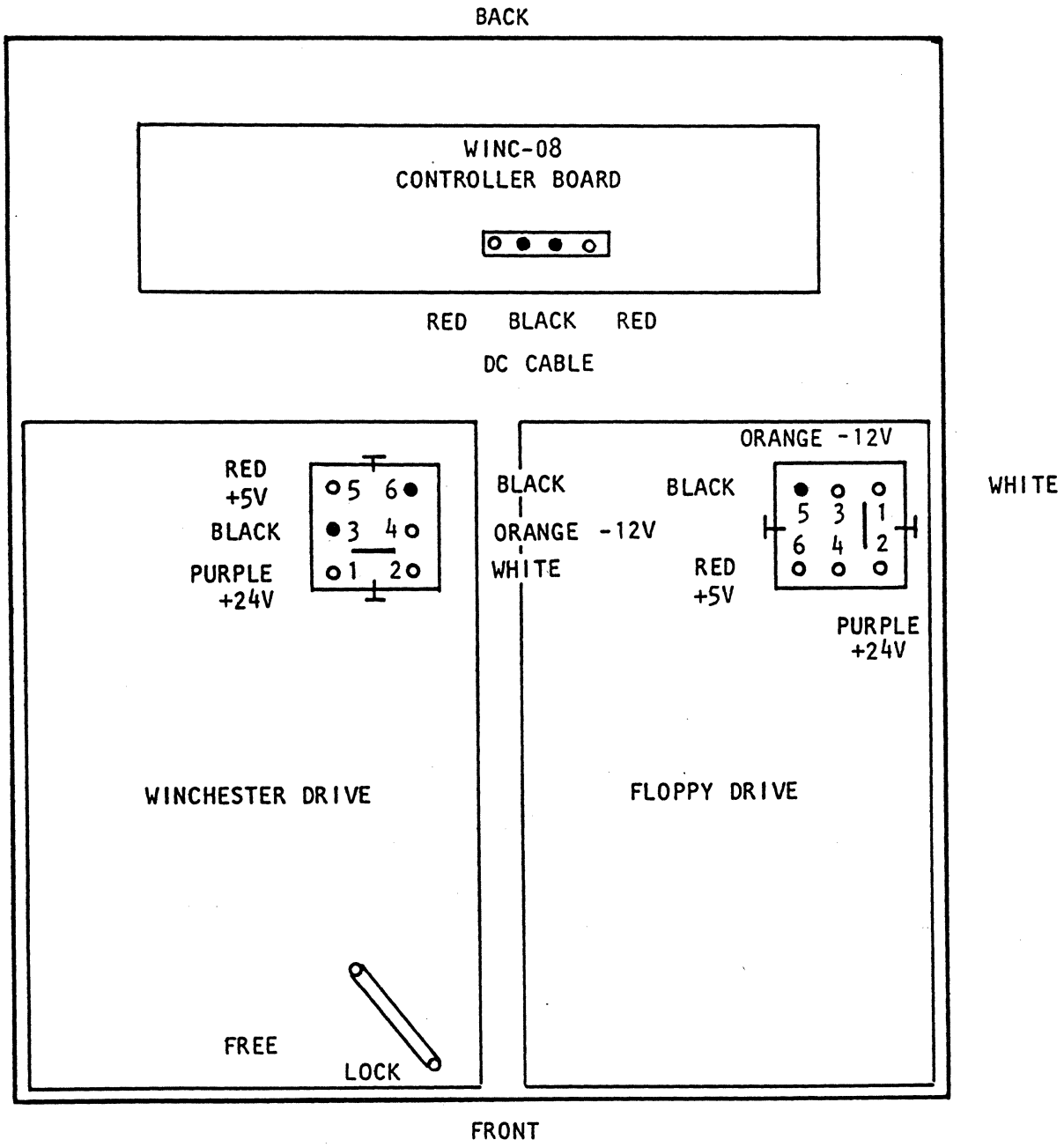


Figure 4-1. Top View of WINC-08

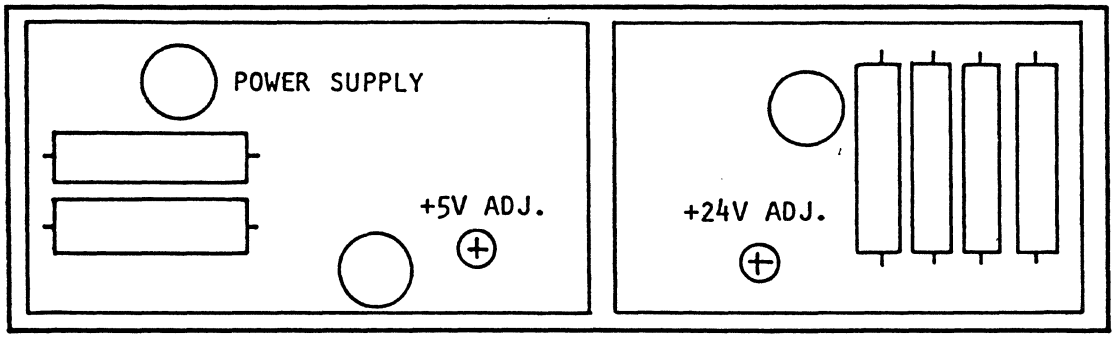


Figure 4-2. Adjustment Potentiometers

c. -12 V is read (orange wire) at the disk drive's DC connector. The -12 VDC is not adjustable, if outside specification replacement is recommended.

d. +24 V is read (purple wire) at the disk drive's DC connector.

e. To adjust +24 VDC place the red (+) lead from the meter on the DC drive connector, purple +24 VDC wire , and the black (-) lead to the DC drive black wire as shown in Figure 4-1. Adjust meter reading to +24 V (±10%) using potentiometer shown in Figure 4-2.

4.8 TROUBLESHOOTING GUIDE

If a malfunction should occur, the recommended troubleshooting procedure is given in Figure 4-3. This figure will direct you to other figures in

this section. This guide assumes availability of spare parts, tools, and skills necessary to analyze faults on a DEC system. This procedure also assumes the remaining elements of the system are performing to specifications.

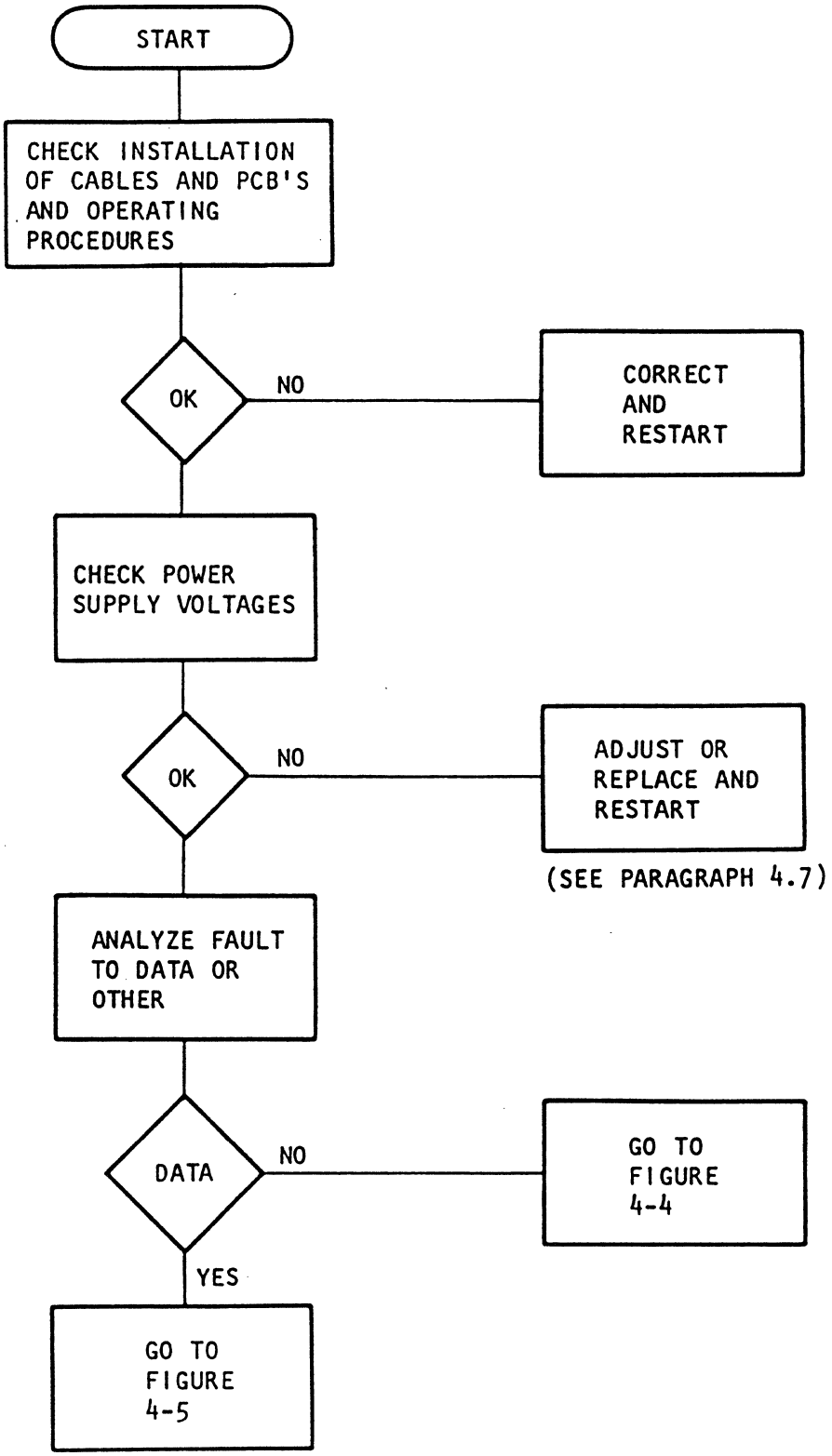


Figure 4-3. Basic Checks

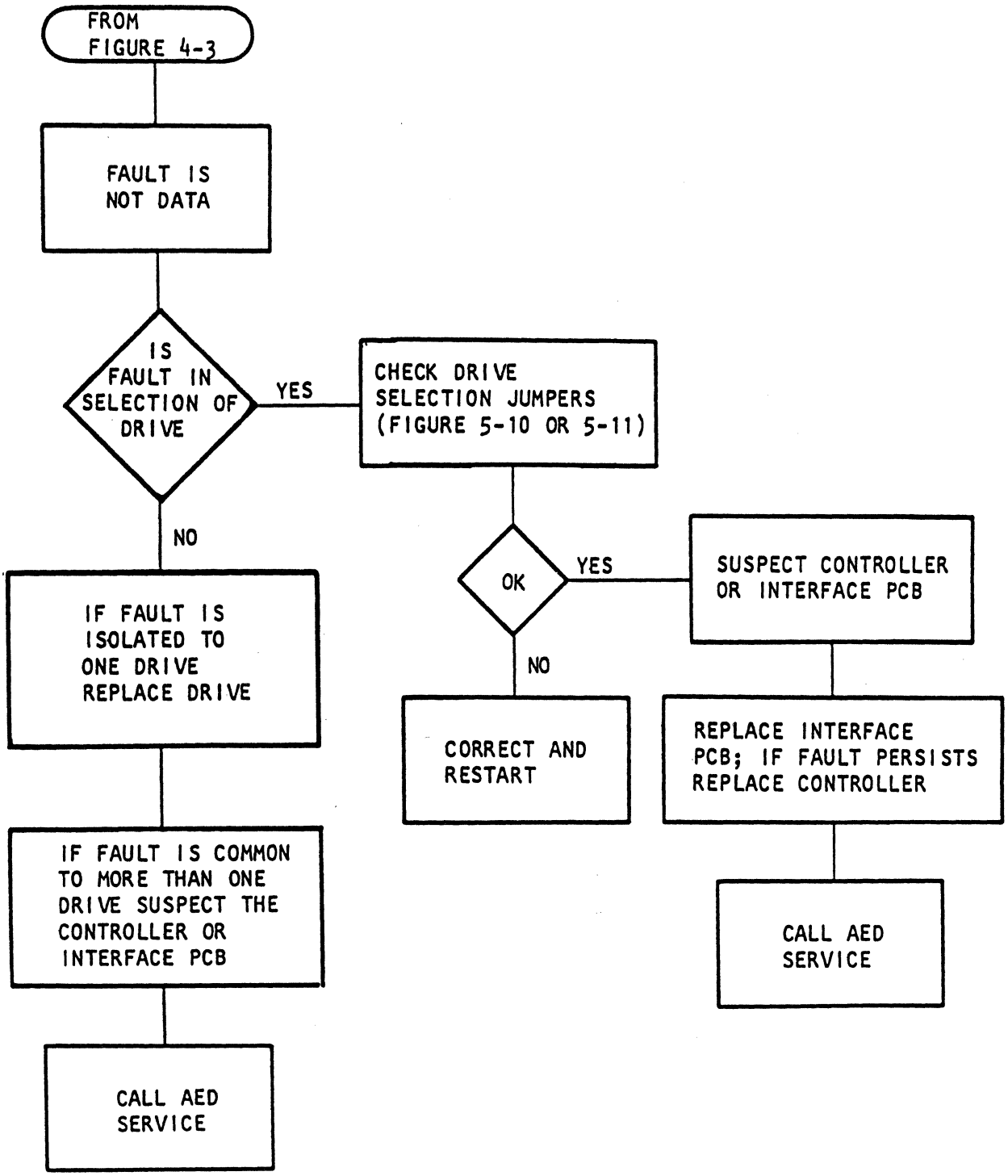


Figure 4-4. Other Than Data Related Fault

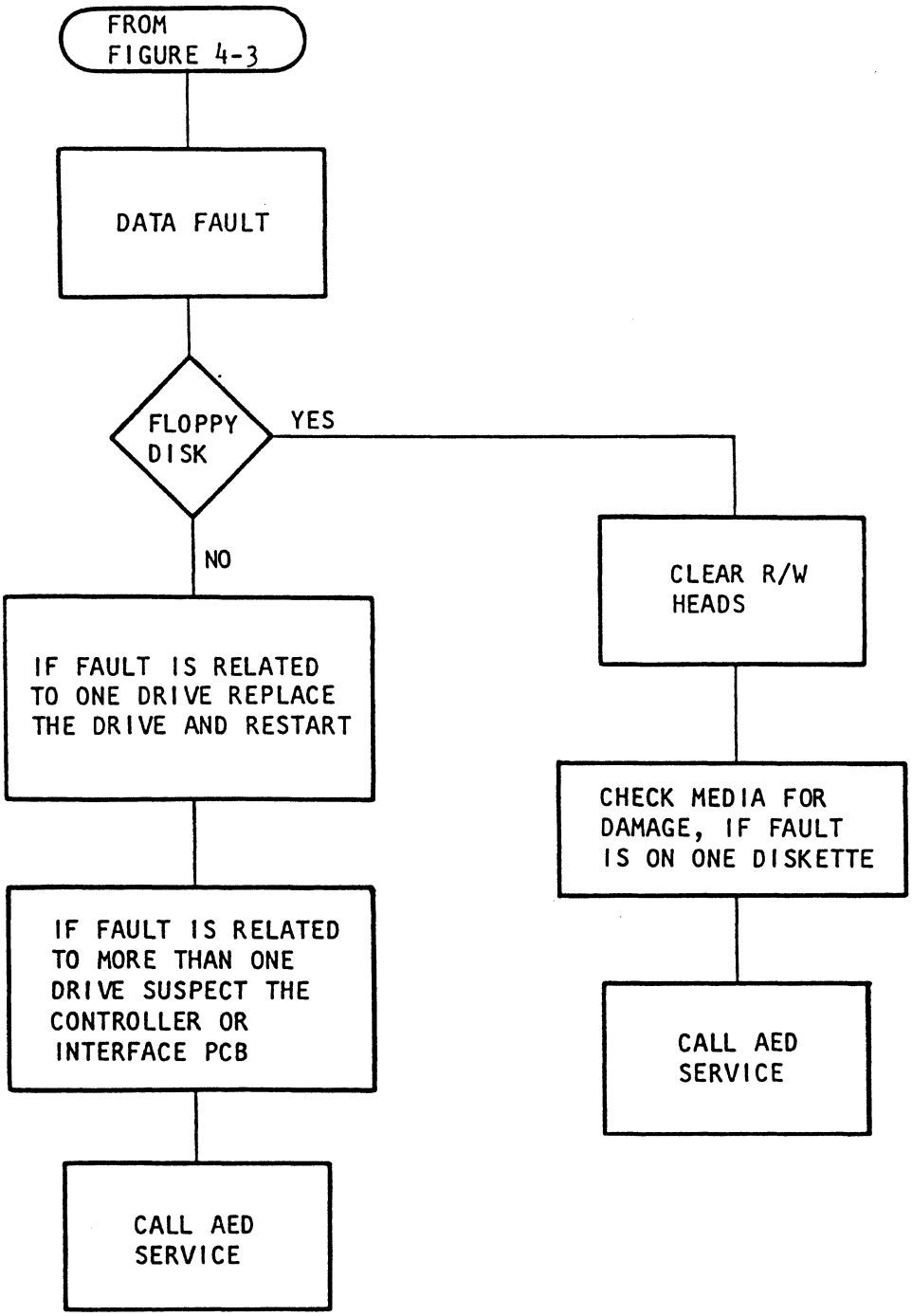


Figure 4-5. Data Related Fault

(To be supplied)

Figure 4-6. LED Display Indication

Section 5

PART NUMBERS OF REPLACEABLE ASSEMBLIES

5.1 REPLACEABLE PARTS

Table 5-1 provides part numbers and descriptions for AED replaceable parts. It is not intended to be a list of recommended spare parts.

Figure 5-1 is a chart showing the arrangement of the subassemblies available for the WINC-08. Figure 5-2 is a WINC-08 system interconnect diagram. Figures 5-3 through 5-11 are drawings showing the various assemblies and subassemblies.

5.2 ORDERING INFORMATION

Parts should be ordered by contacting the AED Order Processing Department at (408) 733-3555. Eastern state users call: (617) 256-1700.

Table 5-1. Replaceable Parts

Assembly	Description
170008-XX	WINC-08 Top Assembly
140058-02	Cover
140059-01	Base
140060-XX	Side Panel
140062-03	PWB Support Bracket
160030-XX	Front Panel Assembly
160025-XX	Rear Panel Assembly
140000-01	Rack Mount Bracket
120056-01	WINC-08 Controller PCB
890030-XX	WINC-08 PROM
554612-900	23.8 Mbyte Winchester Drive
552311-XXX	1 Mbyte Floppy Drive

Cables	Description
150023-XX	Harness Cable
150024-XX	Flat Cable - 20 pin
150025-XX	Controller Drive cable -- 50 pin
150026-01	AC OPT cable -- Qume
150028-XX	Interconnect Diagram
106243-11	Cable, Interface (Winchester)
150000-02	Cable, Interface (Floppy)
150031-XX	LED cable, WINC-08 board
150029-XX	Chassis ground cable
150031-XX	LED cable, front panel

Power Supply	Description
160034-01	Power Supply
120089-01	PWA Regulator, +5 V, -12 V
110089-01	PWB Regulator, +5 V, -12 V
160029-01	Choke -- PL
120092-01	PWA Regulator, +24 V
110092-01	PWA Regulator, +24 V

Table 5-1. Replaceable Parts (Cont'd)

Miscellaneous	Description
140020-02	Qume Drive spacer

Interface Boards	Description
120068-01	PDP-11 Interface Assembly
120013-01	FLEX-02 Interface Assembly
120041-01	LSI-11 Interface Assembly

Documentation	Description
150028-01	Interconnect Diagram WINC-08
190007-01	AED Drive Strapping Instrument -- WINC-08
120057-01	Schematic -- WINC-08
120090-01	Schematic -- 15 V P.S.
120093-01	Schematic -- 124 V P. S.
990004-01	Manual -- WINC-08
800000-02	Diagnostic Diskette -- FLEX-02
900004-01	Diagnostic, Write up
190002-xx	AED Drive Strapping Instrument -- FLEX-02
990000-02	Manual -- FLEX-02
900000-xx	Write-up -- FLEX-02
120042-01	LSI-11 Interface Schematic
120069-01	PDP-11 Interface Schematic

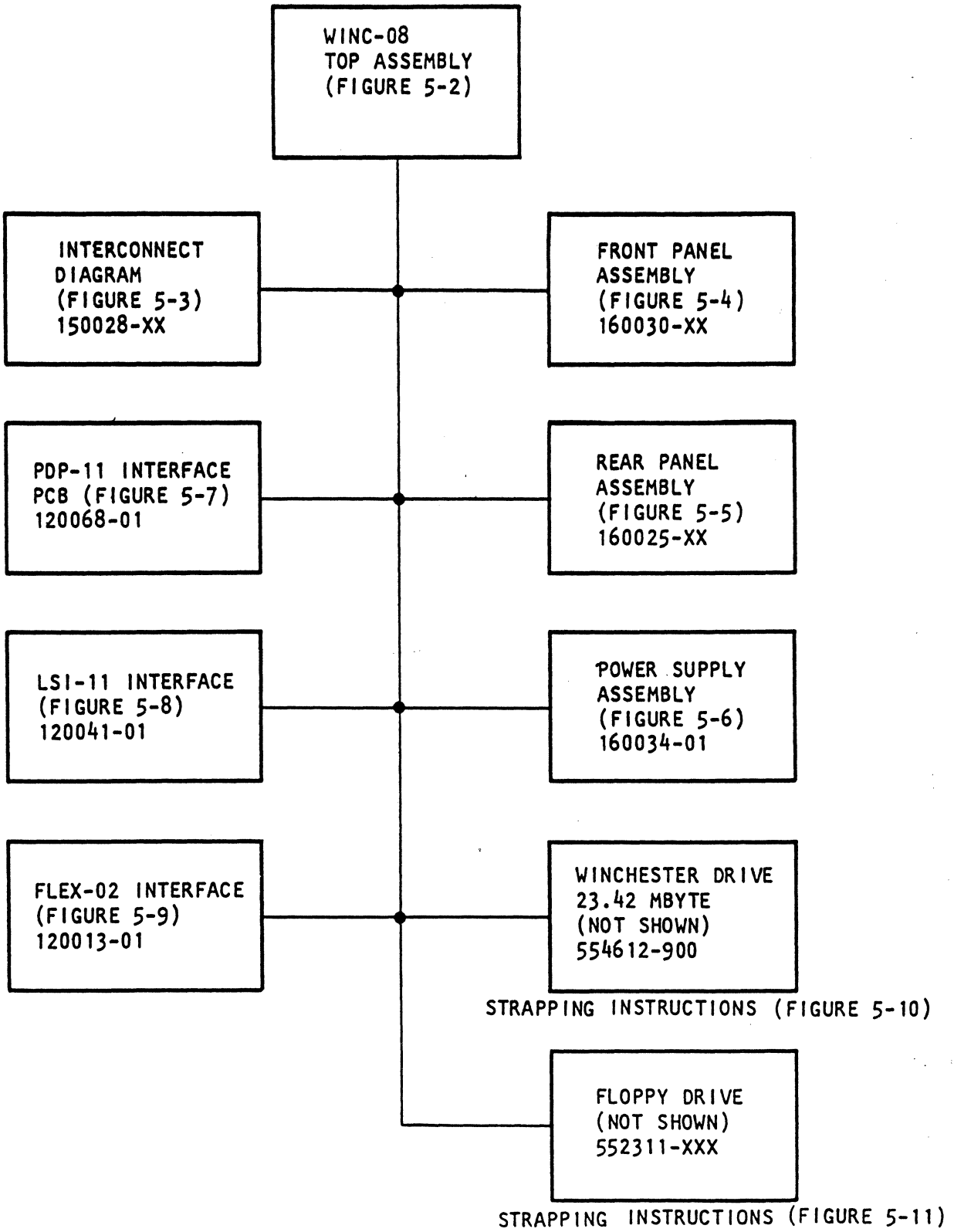


Figure 5-1. WINC-08 Subassembly Arrangement

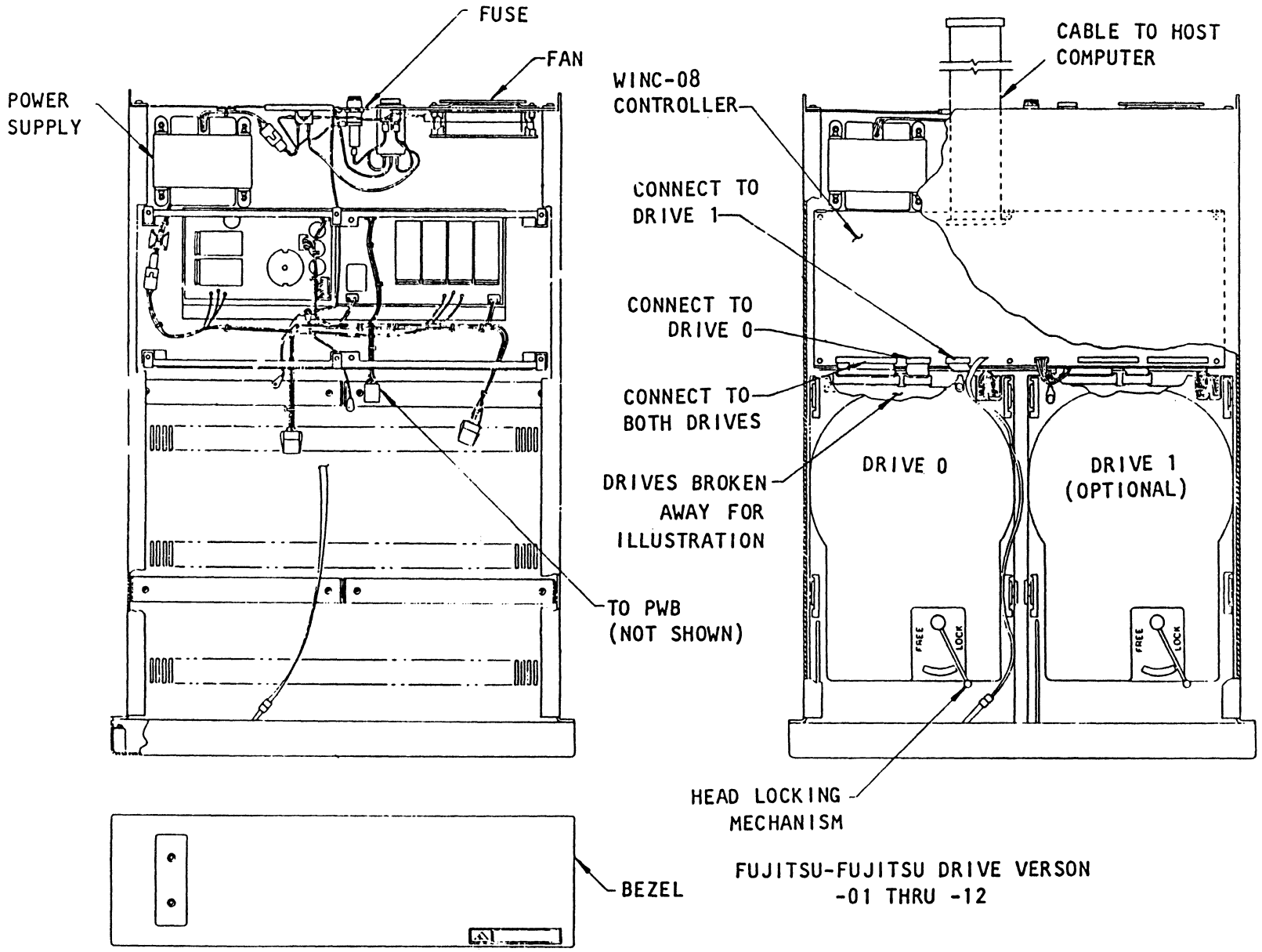
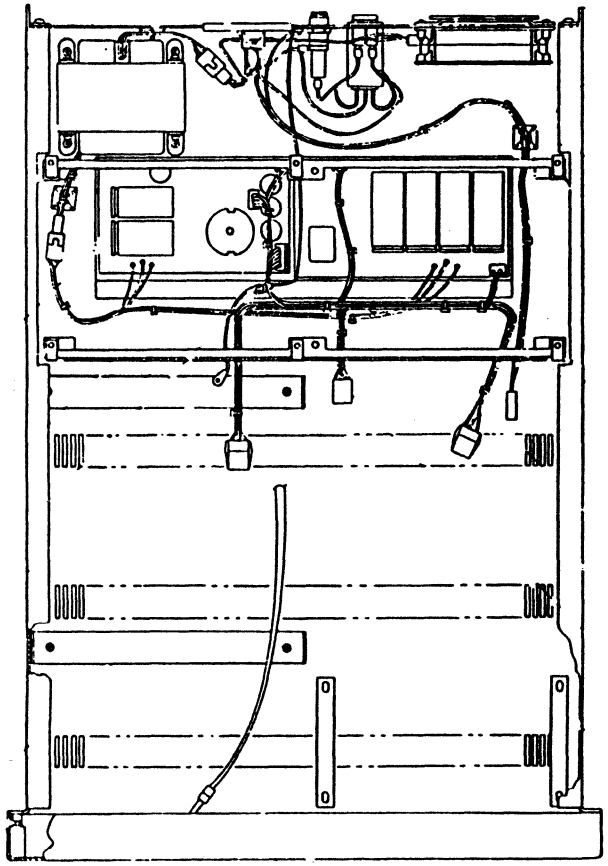
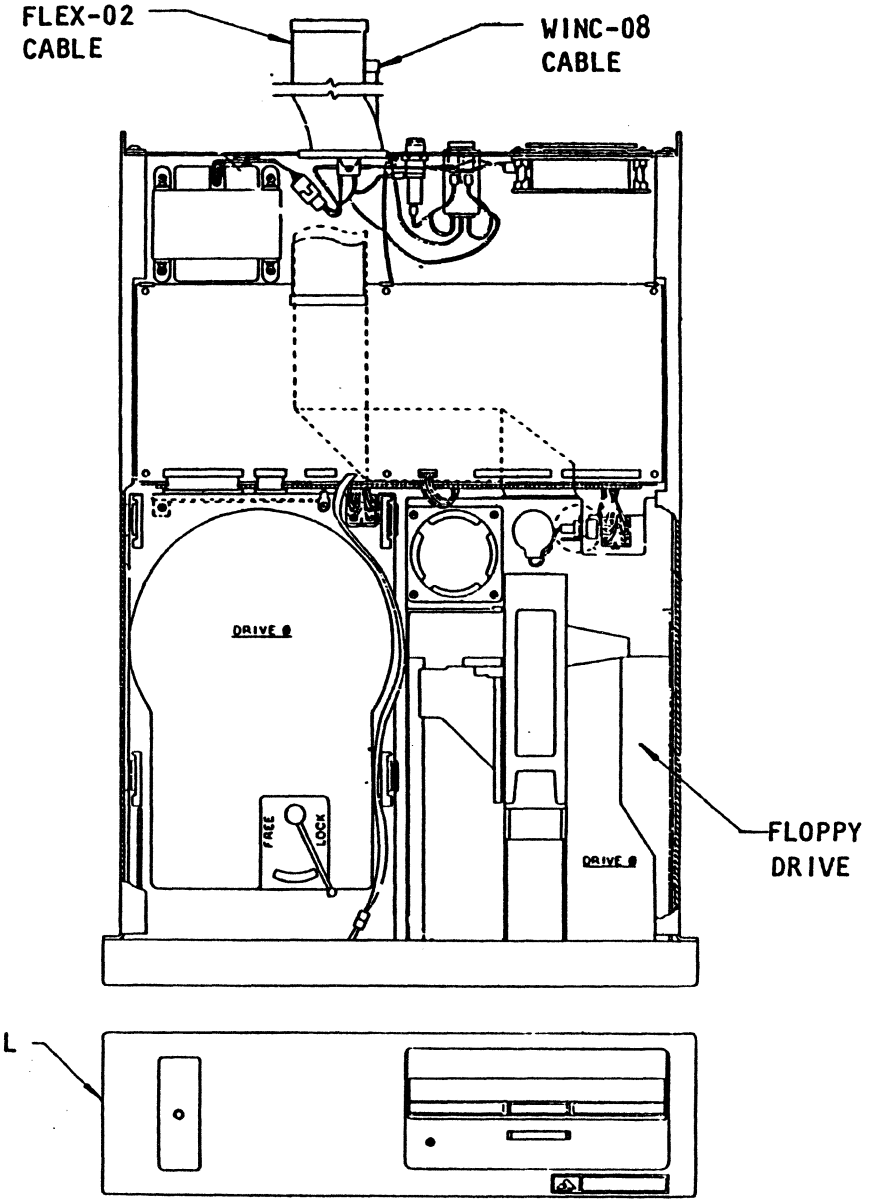


Figure 5-2. Top Assembly (Sheet 1 of 2)





WINC-QUME DRIVE VERSION
-13 THRU -26

Figure 5-2. Top Assembly (Sheet 2 of 2)

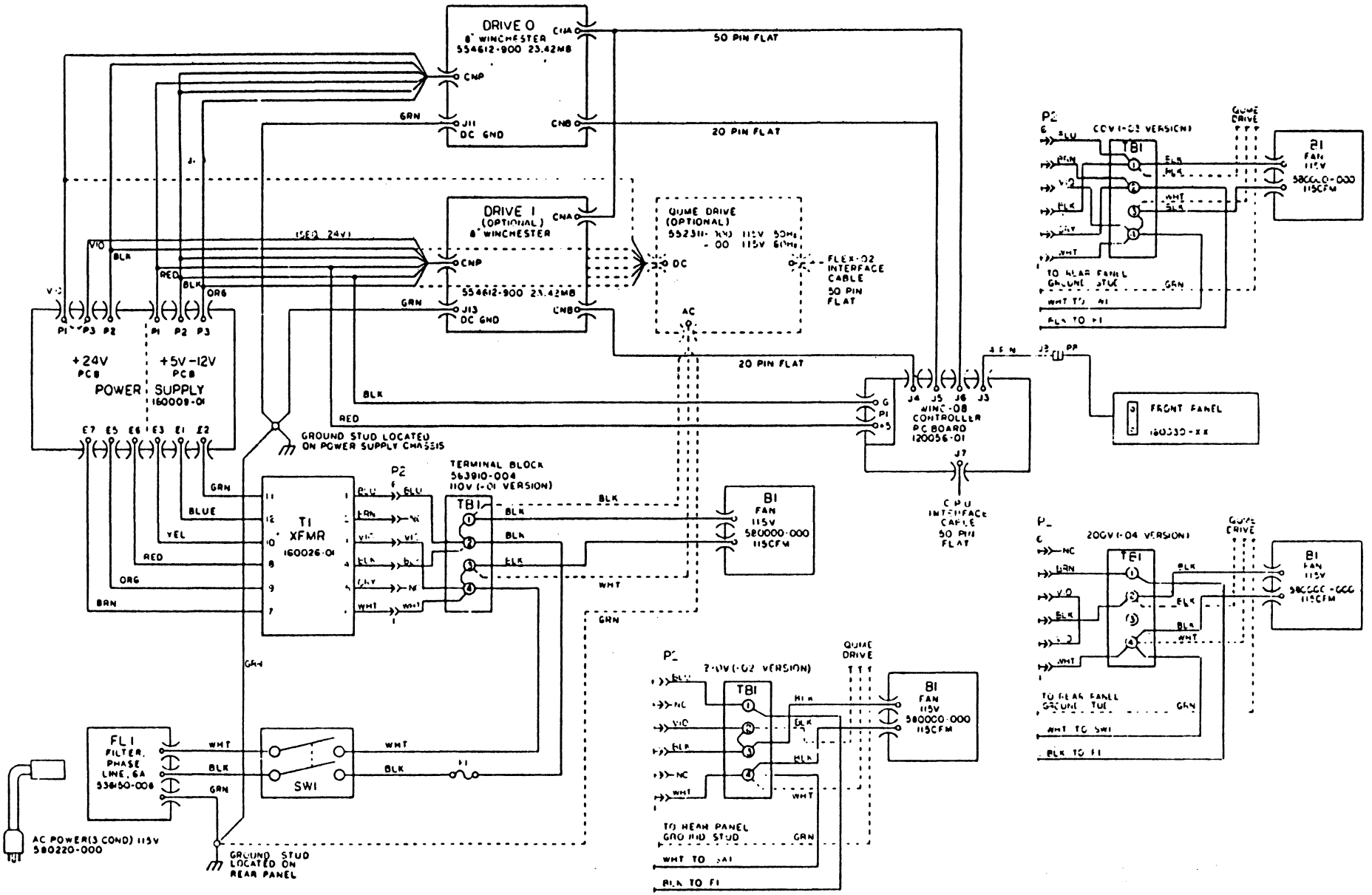
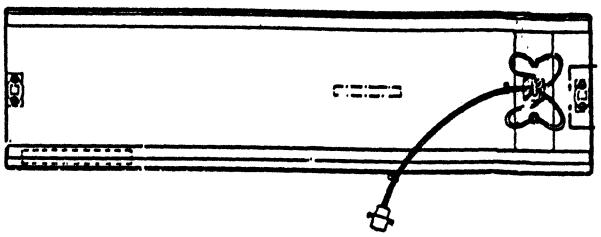
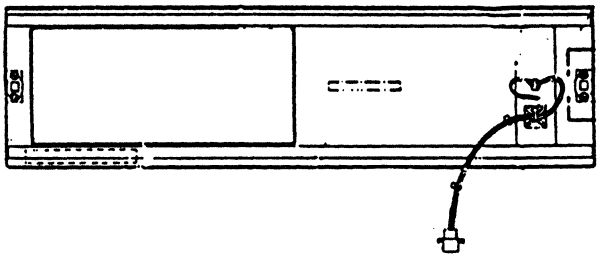


Figure 5-3. Interconnection Diagram

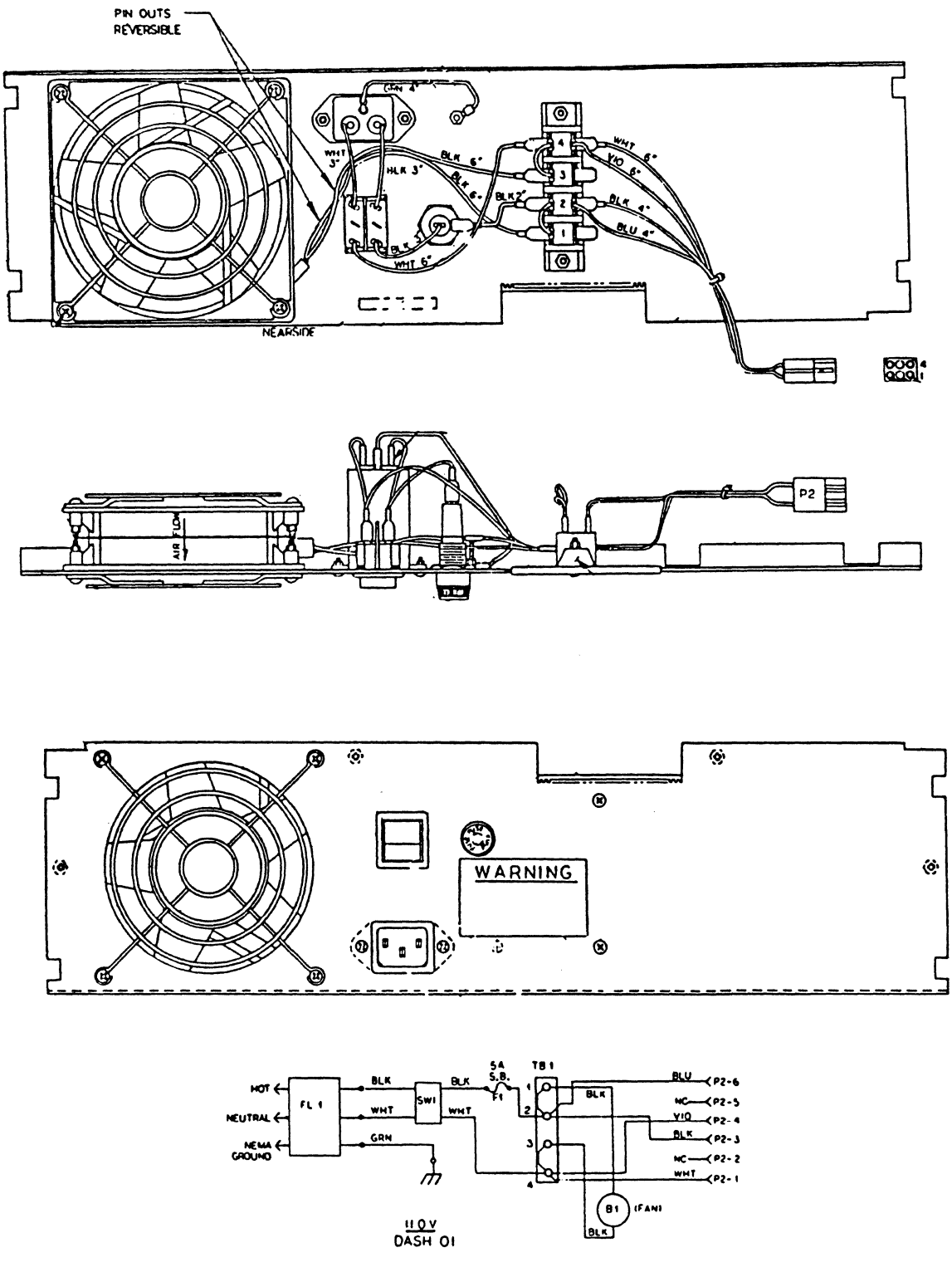


-01 FOR WINC-08 WITHOUT FLOPPY



-02 FOR WINC-08 WITH FLOPPY

Figure 5-4. Front Panel (Bezel) Assembly



DASH-01 110V (SHEET 1 OF 4)
DASH-02 220V (SEE SHT 2 OF 4)
DASH-03 100V (SEE SHT 3 OF 4)
DASH-04 200V (SEE SHT 4 OF 4)

Figure 5-5. Rear Panel Assembly (Sheet 1 of 4)

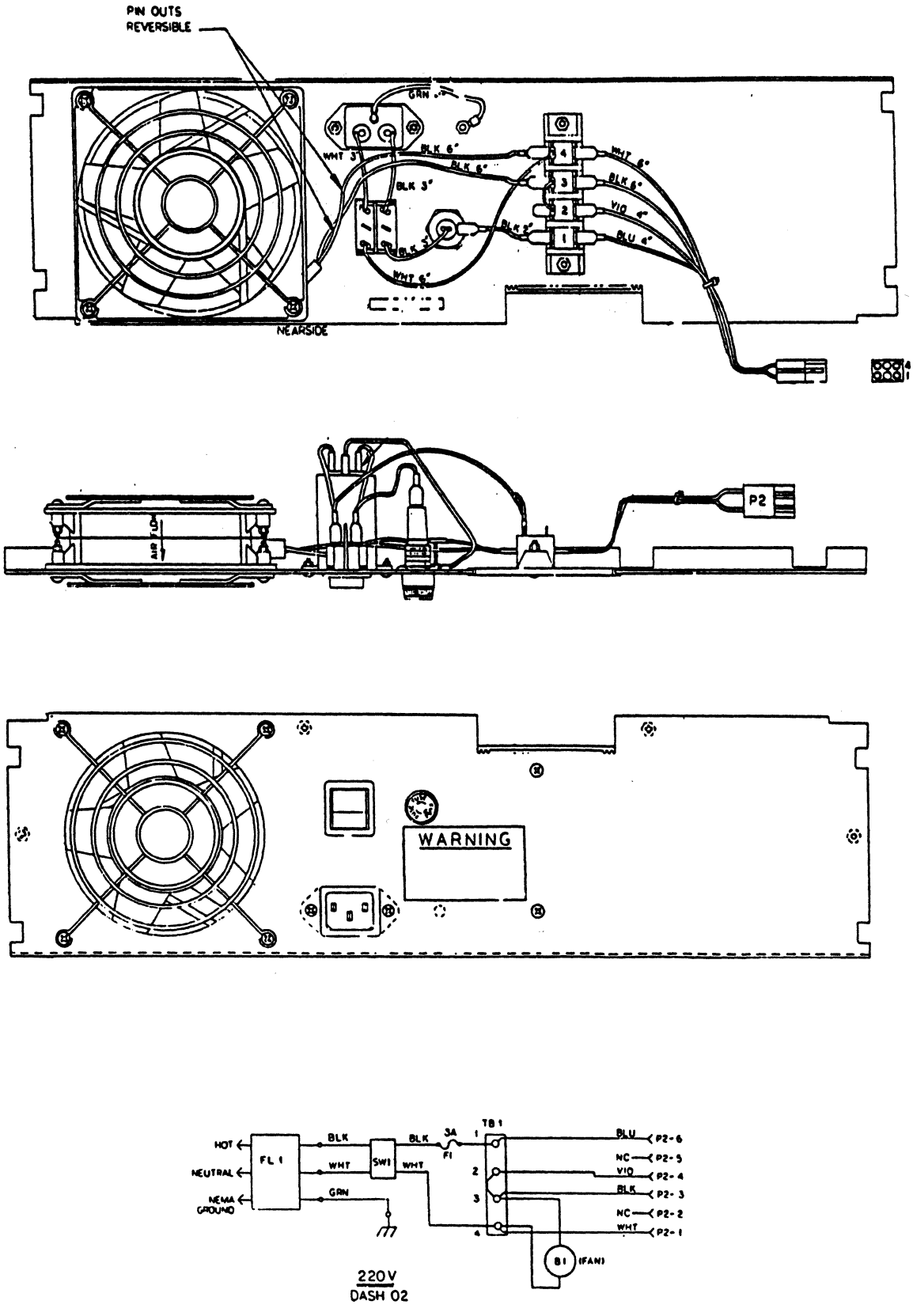


Figure 5-5. Rear Panel Assembly (Sheet 2 of 4)

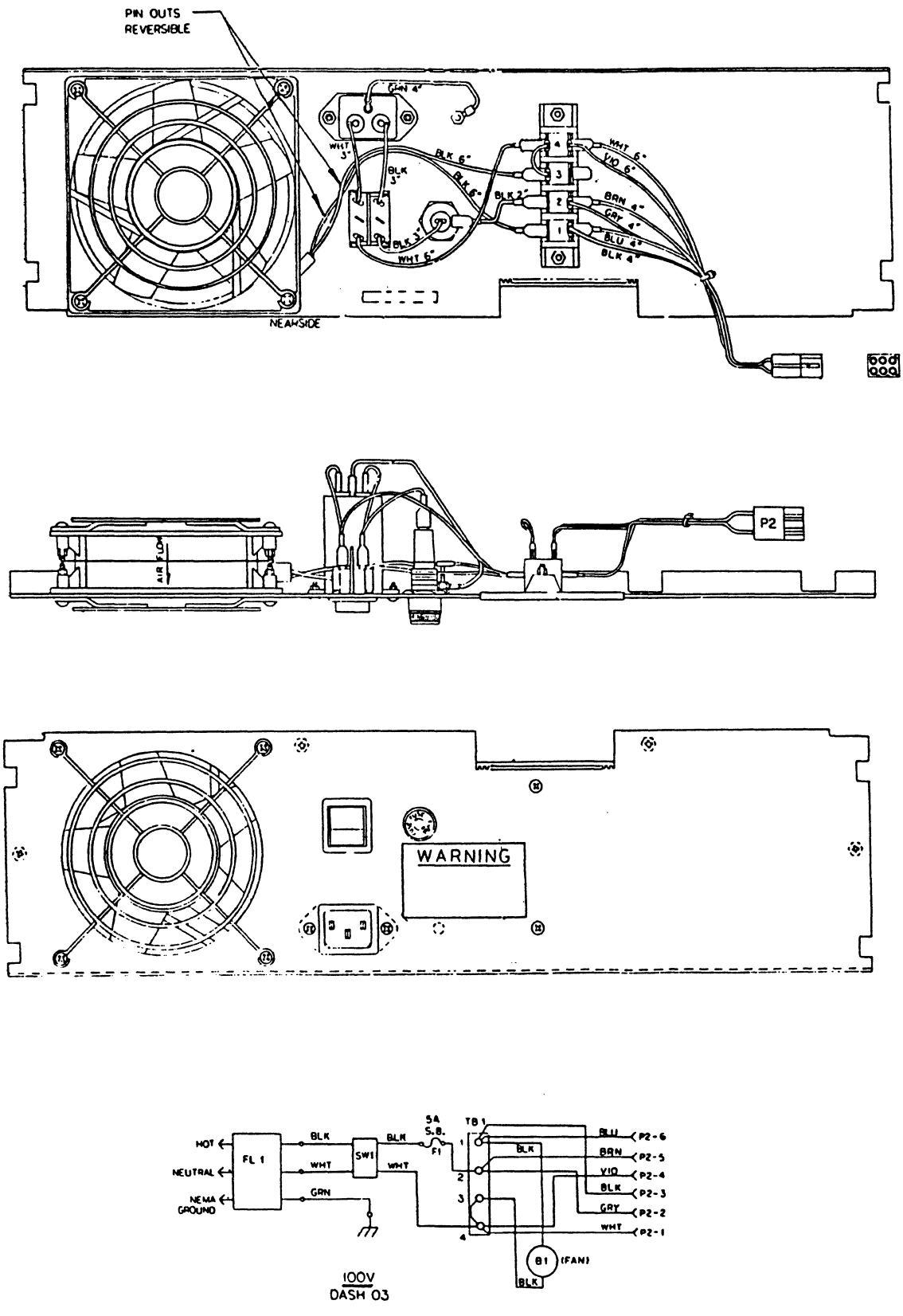


Figure 5-5. Rear Panel Assembly (Sheet 3 of 4)

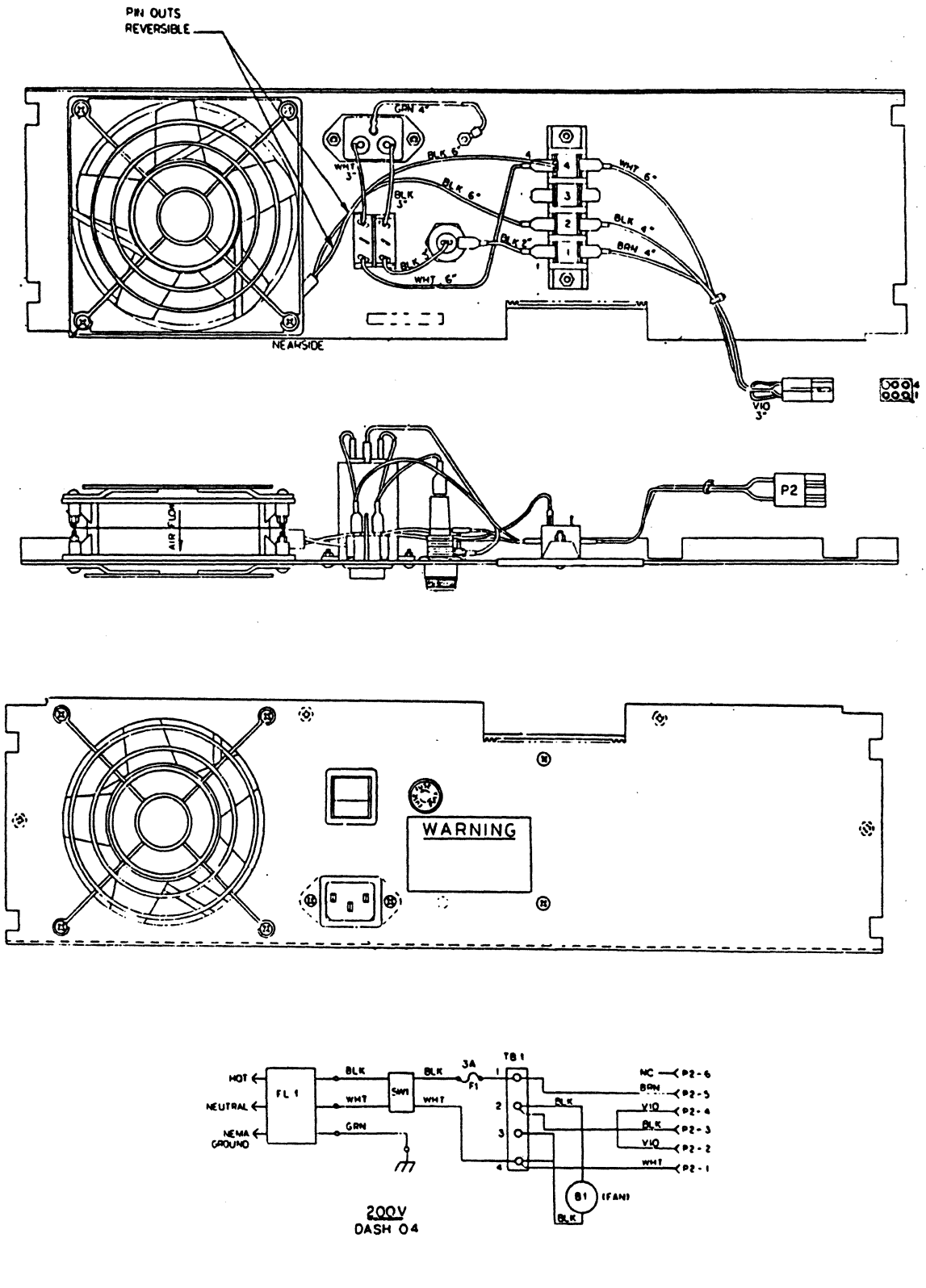


Figure 5-5. Rear Panel Assembly (Sheet 4 of 4)

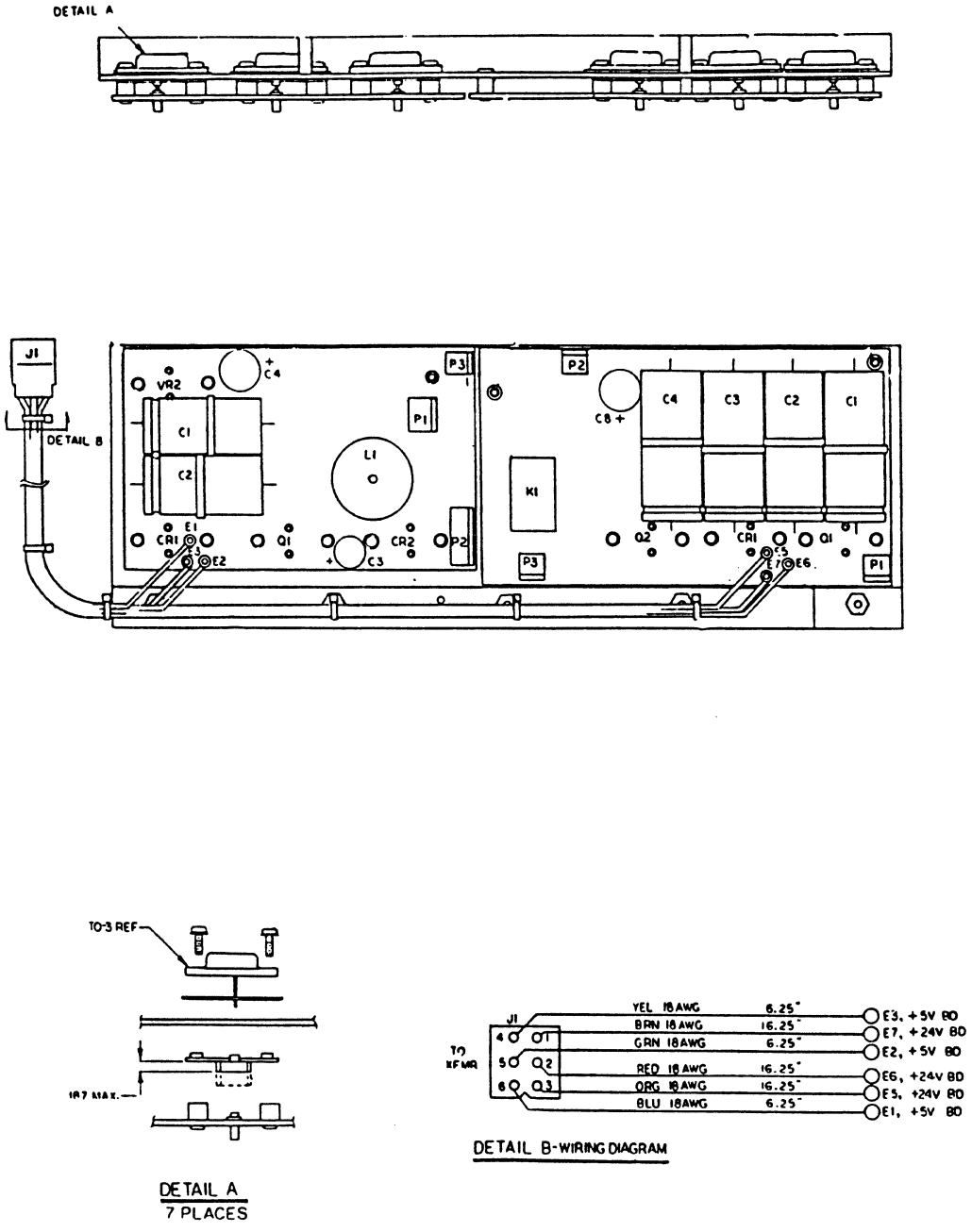


Figure 5-6. Power Supply Assembly

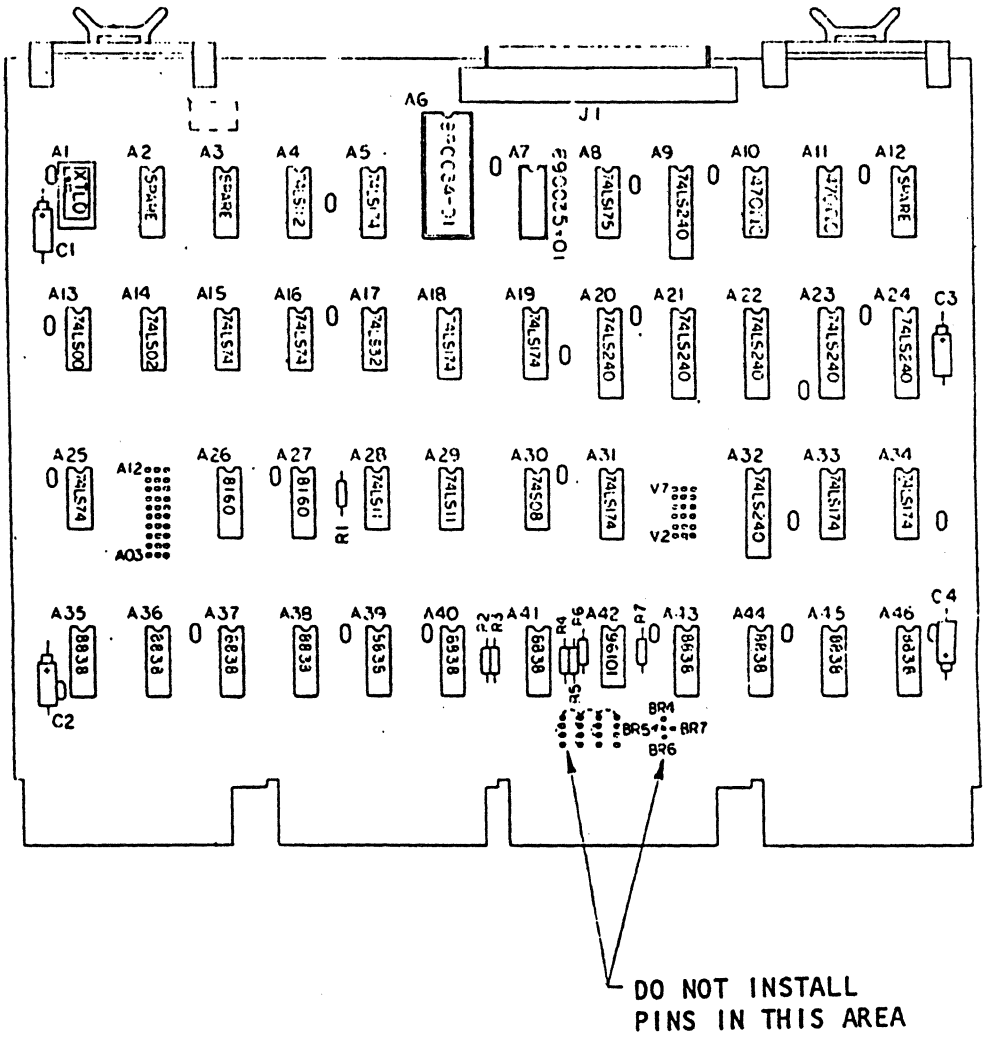
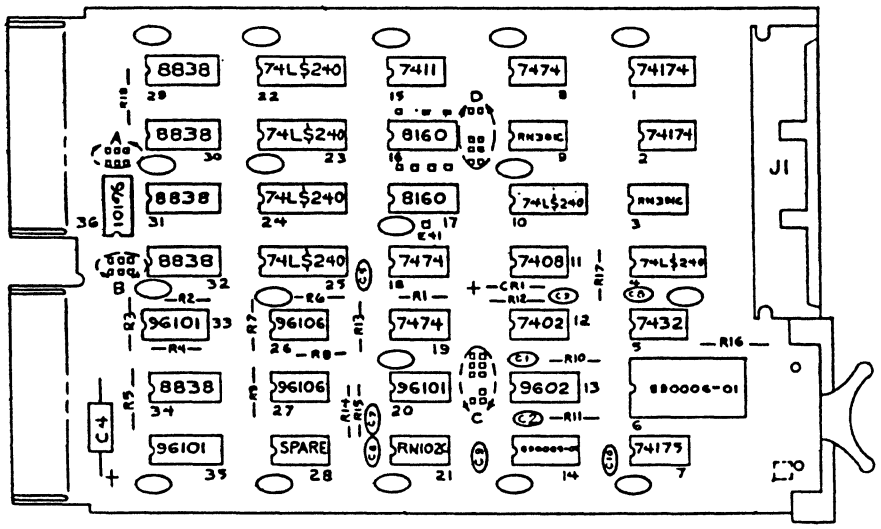


Figure 5-7. PDP11 Interface Assembly



DETAIL 'A'
SCALE: NONE

E16 O E18
E17 O E14
E13 O E15

DETAIL 'B'
SCALE: NONE

E21 O E19
E20 O E11
E12 O E10

DETAIL 'C'
SCALE: NONE

E10 O E2
E30 O E6
E40 O E5
O E8
E90 O E7

DETAIL 'D'
SCALE: NONE

E390 O E40
E370 O E38
E350 O E36
E330 O E34

DETAIL 'E'
SCALE: NONE

E26 O E27 O E28
A16
E22 O E23 O O E25 E24
A17
O E41

	INTERRUPT VECTOR TABLE								
	BITS								
	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8 TO 2^{15}
LOGICAL "0" (OPEN)	ALWAYS = 0	E19 TO E21	E16 TO E18	E10 TO E12	E7 TO E9	E13 TO E15	E4 TO E6	E1 TO E3	ALWAYS "0"
LOGICAL "1" (CLOSED)	——	E19 TO E20	E16 TO E17	E10 TO E11	E7 TO E8	E13 TO E14	E4 TO E5	E1 TO E2	——

Figure 5-8. WINC-08 Interface Assembly

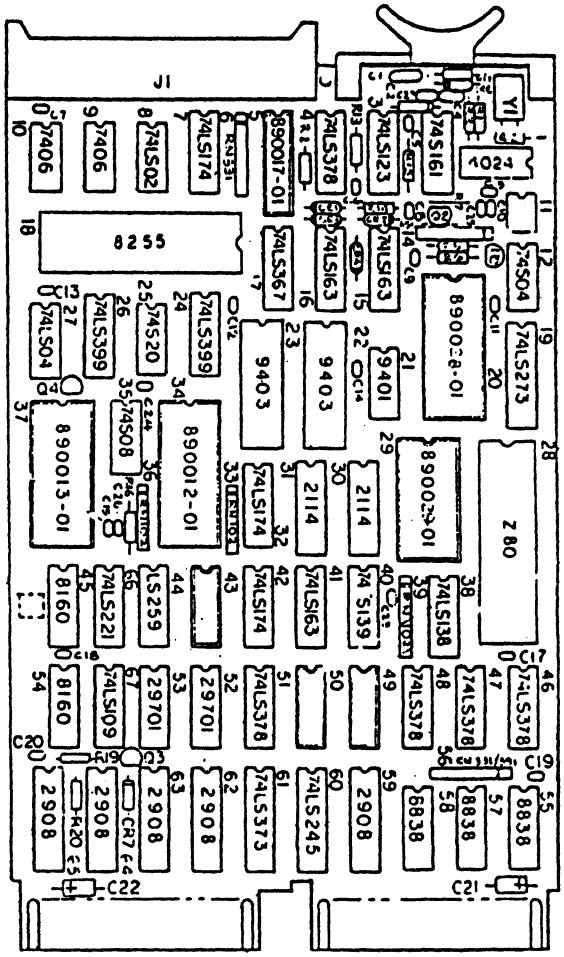


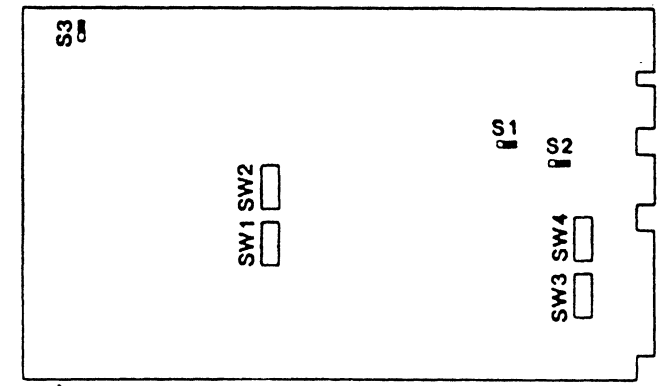
Figure 5-9. FLEX-02 Assembly

LOCATION	COMMENTS
JUMPER S1 — INSTALL SUPPLIED JUMPER (BLOCK) BETWEEN PINS 2 & 3 AS SHOWN	
JUMPER S2 — INSTALL SUPPLIED JUMPER (BLOCK) BETWEEN PINS 2 & 3 AS SHOWN	
JUMPER S3 — INSTALL SUPPLIED JUMPER (BLOCK) BETWEEN PINS 1 & 2 AS SHOWN	

SW1 - 1	OFF (OPEN)	SW2 - 1	OFF (OPEN)
SW1 - 2	OFF (OPEN)	SW2 - 2	OFF (OPEN)
SW1 - 3	OFF (OPEN)	SW2 - 3	ON
SW1 - 4	ON	SW2 - 4	ON
SW1 - 5	ON	SW2 - 5	OFF (OPEN)
SW1 - 6	ON	SW2 - 6	OFF (OPEN)
SW1 - 7	OFF (OPEN)	SW2 - 7	OFF (OPEN)
SW1 - 8	ON	SW2 - 8	ON

	FOR DRV 0 (LEFT HAND SIDE)	FOR DRV 1 (RIGHT HAND SIDE)
SW3 - 1	ON	ON
SW3 - 2	ON	ON
SW3 - 3	ON	ON
SW3 - 4	ON	ON
SW3 - 5	OFF (OPEN)	OFF (OPEN)
SW3 - 6	OFF (OPEN)	OFF (OPEN)
SW3 - 7	OFF (OPEN)	ON
SW3 - 8	ON	OFF (OPEN)

SW4 - 1 THRU SW4 8 ALL POSITIONS: OFF (OPEN)



BOTTOM VIEW OF FUJITSU M2301 / M2302 DRIVE BOARD

FOR ALL SWITCHES:

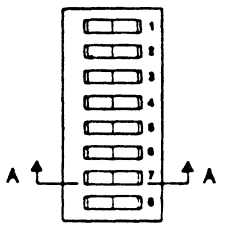
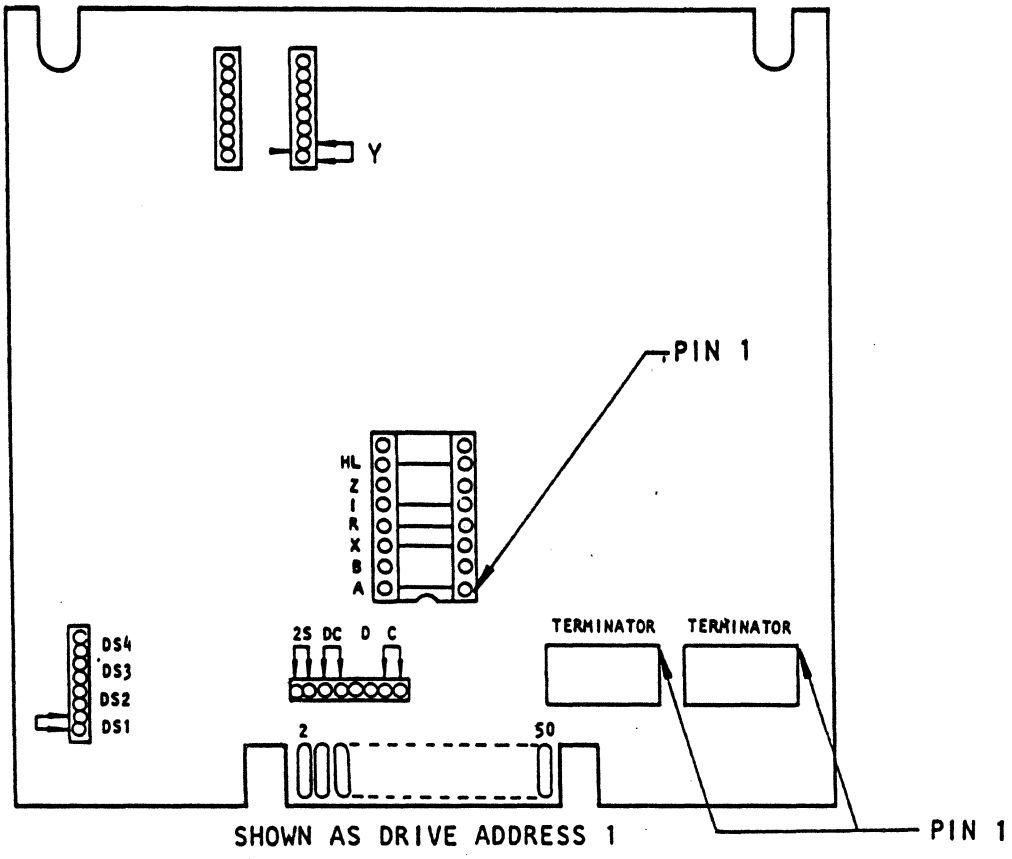


Figure 5-10. Drive Strapping Instructions, WINC-08



FLOPPY DRIVE

P/N 552311-100, 115 V/60 Hz
P/N 552311-200, 230 V/50 Hz
P/N 552311-000, 115 V/50 Hz
P/N 552311-300, 230 V/60 Hz

1. VERIFY THAT THE FOLLOWING JUMPERS ARE INSTALLED:

   Y
   2S
   DC

2. VERIFY THAT THE FOLLOWING JUMPERS ARE REMOVED:

   DS2, C TO D, AND ANY JUMPERS NOT IN STEP 1.

3. FOR DRIVE ADDRESS 1:

   VERIFY THAT JUMPERS DS1 AND C ARE INSTALLED AND THAT THE PROGRAM HEADER AND TERMINATORS (2) ARE INSTALLED.

4. MARK DRIVE ADDRESS ON DRIVE MOTOR.

Figure 5-11. FLEX-02 Drive Strapping Instructions

Section 6

PROGRAMMERS' GUIDE

6.1 GENERAL

A description of the registers and commands used for emulation and maintenance is included in this section. Included for quick reference at the top of each table is a bit layout of the information provided in that table.

6.2 SYSTEM CONSIDERATIONS

The WINC-08 performs emulation to the degree that system software drivers need no change and the higher level diagnostics operate without error. The major differences caused by emulation are in the area of sector addressing and physical partitions.

The WINC-08 partitions each Winchester physical drive into two separate logical drives by assigning the first four physical heads as one logical unit and the other four heads as a second logical unit. This partitioning allows initializing one logical unit without affecting the other logical unit. Only one half of the physical drive is initialized, because there are two logical units but only one head carriage. It is possible that a seek could be issued to the first unit and, before the I/O is initiated for that unit, a seek could be started for the second unit. This would cause the heads to be on the wrong track when the first unit's I/O was initiated.

To resolve this problem the WINC-08 performs an implied seek before all I/O operations. SEEK commands are allowed and executed, but are not necessary. Also, since the physical positioning of one logical unit will change the position of the other logical unit, doing a physical READ HEADER operation would result in an unexpected drive address.

Therefore, the WINC-08 performs the READ HEADER function as a logical operation and does not access the disk to get the address. Instead, the last logical disk address is saved in an internal memory and presented to the CPU during the READ HEADER function.

An additional consideration is address mapping from logical to physical addresses. The WINC-08 has 42 sectors per track and emulates a drive with 40 sectors per track. The result of logical-to-physical mapping is that physical track boundaries may be encountered during a logical, multiple-sector, I/O command. If an I/O command requires a physical seek or head switch, the WINC-08 will perform the operation transparent to the logical command, creating the possibility of a seek operation transparent to the logical command. Thus, there is the possibility of a seek operation occuring in the middle of a multiple-sector read or write command.

Comparison of the WINC-08 throughput to that of the emulated drive varies as a function of the seeks required and the number of sectors accessed per transfer request. The WINC-08 is faster for data transfers of seven sectors or less; DEC's RL02 is faster for transfers of greater than seven sectors. This is due to the tradeoffs between Winchester and cartridge technology.

6.3 DESCRIPTION OF REGISTERS

The remainder of this section provides useful information on the data stored in the following registers:

a. Control Status register

b. Bus Address register

c. Disk Address register

d. Multipurpose register

6.3.1 CONTROL STATUS REGISTER

Refer to Table 6-1. This is a 16-bit Control Status register (CSR).

Table 6-1. Control Status Register (774400)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERROR	DISK ERROR	NXM	HNF & DLT	HCRC & DCRC	OPI	DSI	DSO	CRDY	IE	BA17	BA16	FUNC 2	FUNC 1	FUNC 0	DRDY

Bit	Description	Explanation
15	ERROR	Set by any CSR bit 14 through 10. Cleared by clearing CSR bits 14 through 10 or by a BUS INIT.
14	DISK ERROR	Set by any disk drive error. Drive status may be obtained by executing a GET STATUS command. The drive error may be reset by setting bit 3 in the DA Register during a GET Status command or by issuing an BUS INIT.
13	NXM	NON-EXISTENT MEMORY. Indicates a response timeout during DMA access. Cleared by any CSR output with bit 7 = 0 or by a BUS INIT. This bit is also set whenever the WINC-08 is set in the special maintenance mode by issuing a GET STATUS function with a 364 octal in the DA register.

Table 6-1. Control Status Register (774400) (Cont'd)

12	HNF and DLT	HEADER NOT FOUND. When bit 12 and OPI (bit 10) are set, it indicates that the WINC-08 was unable to find the correct sector to read, write, or writecheck. This error will be set after searching 44 sector headers without finding the desired sector. HNF will also be set if the FIND HEADER routine detects a wrong cylinder address in a valid header and, after performing a rezero and reseek, the cylinder address still does not compare with the desired address. DATA LATE. Set to zero. Not used by WINC-08.
11	HCRC/DCRC	HEADER CRC/DATA CRC. If the command function is a READ function, this bit indicates an ECC error which the microcode was unable to correct. Eight rereads are performed with eight attempts to correct the data before setting the DCRC error bit. If the command function was a WRITECHECK, this bit indicates either an ECC error or a data miscomparison. Eight retries are performed before setting DCRC error bit. No ECC corrections are attempted.
10	OPI	OPERATION INCOMPLETE. A hardware timeout occurred during a microcode loop, such as waiting for serial data, or a microcode timeout occurred during a status loop, such as waiting for access to the CPU bus. The following is a list of microcode loops which might result in OPI errors. No SEEK done after one second. Seek timeout will also be set in the MP register during a GET STATUS request. Timeout while search for a header. Sector mark stayed on. Sector mark stayed off. FIFO output stayed empty. (No Sync?) FIFO byte time status stayed low. Timeout while writing predata gap. Status error while reading or writing. R/W DONE never found. Status errors consist of:

Table 6-1. Control Status Register (774400) (Cont'd)

Loss of DRIVE READY
Loss of SEEK COMPLETE
Drive fault
Sector mark found

Timeout while writing data.
FIFO input stayed full.
Status error while writing.
R/W DONE never found.

Timeout while reading data.
FIFO output stayed empty. (No Sync?)
Status error while reading.

Timeout while formatting.
MP register not 177400 octal.
Index or sector stayed high or low.
FIFO output stayed full.
Loss of DRIVE READY.
Loss of SEEK COMPLETE.
Drive fault.
R/W DONE never found.

9-8 DS1 and DS0 DRIVE SELECT BITS 1 AND 0. These bits determine which logical drive is selected. The logical versus physical drive selection is as follows:

LOGICAL UNIT	PHYSICAL UNIT	PHYSICAL HEADS
0	0	0 - 3
1	0	4 - 7
2	1	0 - 3
3	1	4 - 7

7 CRDY CONTROLLER READY. When this bit is set to zero, the function in CSR bits 3 through 1 is executed. This bit is a negative GO bit. When this bit is set, the WINC-08 is ready to accept another command. Changing any WINC-08 register while bit 7 is low may result in errors or loss of data.

6 IE INTERRUPT ENABLE. When bit 6 is set, the controller will issue an interrupt at the normal or error completion of a command.

Table 6-1. Control Status Register (774400) (Cont'd)

5-4	BA17 and BA16	BUS ADDRESS EXTENSION BITS 17 AND 16. Cleared by a BUS INIT. The complete bus address consists of BA17, BA16, and the BA register.
3-1	FUNC 2 FUNC 1 FUNC 0	FUNCTION. These three bits contain the command function to be performed by the WINC-08 when CSR bit 7 is set to zero. See paragraph 6.4 for additional details on commands.

FUNCTION	COMMAND	CSR CODE
000	NO-OP	0
001	WRITECHECK	2
010	GET STATUS	4
011	SEEK	6
100	READ HEADER	10
101	WRITE DATA	12
110	READ DATA	14
111	READ DATA WITHOUT HEADER	16

0	DRDY	DISK DRIVE READY. Indicates that the selected WINC-08 physical (and logical) disk drive is ready. This bit is reset during a SEEK operation on the selected logical unit.

6.3.2 BUS ADDRESS REGISTER (774402)

This is a 16-bit read/write bus address (BA) register. BA expansion bits 16 and 17 are contained in CSR bits 4 and 5. The contents of this 16-bit BA register plus the CSR expansion bits indicate the address of the CPU memory to be used for data transfers. The complete 18-bit address is updated at the completion of each sector. The BA is cleared with a BUS INIT, or by loading with all zeros.

6.3.3 DISK ADDRESS REGISTER (774404)

This read/write register is used for three different functions. These three functions comprise:

a. DA register during a SEEK command (see Table 6-2).

b. DA register during a READ/WRITE or WRITECHECK command (see Table 6-3).

c. DA register during a GET STATUS command (see Table 6-4).

The register is cleared by a BUS INIT or by loading with all zeros.

Table 6-2. Disk Address Register (774404)
(During SEEK Command)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Cylinder Address Difference (Bits 15 through 7)									ZERO	ZERO	HS	ZERO	DIR	ZERO	MARKER

Bit	Description	Explanation
15-7	DIFF	CYLINDER ADDRESS DIFFERENCE. Indicates the number of logical cylinders the heads are to move on a logical seek. The physical cylinder difference will be computed by microcode.
6-5	ZERO	These bits must be zeros.
4	HS	HEAD SELECT. Indicates the logical head to be selected. The logical and physical heads will normally have no particular correlation due to the microcode address mapping.
3	ZERO	This bit must be a zero.
2	DIR	DIRECTION. This bit specifies the direction of the head motion. A one indicates motion toward the center of the disk and a zero indicates motion towards the outside of the disk.
1	ZERO	This bit must be a zero.
0	MARKER	The marker bit must be a one.

Table 6-3. Disk Address Register (774404)
(During a READ/WRITE or WRITECHECK Command)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Cylinder Address (bits 15 through 7)									H S	Sector Address (bits 5 through 0)					
	CA8								CA0		SA5					SA0

Bit	Description	Explanation
15-7	CA	CYLINDER ADDRESS. Logical cylinder address from 0 to 511 for data transfer. This address will be mapped by microcode into the physical address for the data transfer. If the heads are not on the requested cylinder, the microcode will perform a SEEK operation before the I/O. Cylinder zero is on the outside of the disk.
6	HS	HEAD SELECT. This bit selects the logical head number to be selected.
5-0	SA	SECTOR ADDRESS. Logical address of the selected sector from 0 to 40. Addressing a sector greater than 40 causes a HEADER NOT FOUND error. The logical address is mapped by microcode into a physical address.

Table 6-4. Disk Address Register (774404)
(During a GET STATUS Command)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NOT USED								ZERO	ZERO	ZERO	ZERO	RST	ZERO	GS	GS

Bit	Description	Explanation
15-8		NOT USED
7-4	ZERO	These bits must be zeros.
3	RST	RESET. When this bit is set during a GET STATUS command, the microcode clears the drive error status register and issues a drive fault clear before sending the status to the CPU.

Table 6-4. Disk Address Register (774404) (Cont'd)

2	ZERO	This bit must be zero.
1-0	GS	GET STATUS CODE. These bits must be at 1 to enable the GET STATUS request. The DA register must contain either a 3 or a 13 for a valid GET STATUS command. If the DA is set to 364 octal the microcode will enter a special maintenance mode and interpret the next command as a maintenance command (see Section 6.4).

6.3.4 MULTIPURPOSE REGISTER (774406)

The MP register is used for either:

a. Status (see Table 6-5), or
b. Header data (see Table 6-6), or
c. READ/WRITE command word count (see paragraph below).

The MP register is used to specify the two's complement of the total number of words. Due to emulation requirements, the WINC-08 will not allow spiral read/write operations. The CPU must not issue data transfers that expect the disk address to advance to the next head or cylinder. Such a transfer will advance the sector number to 41, resulting in HEADER NOT FOUND error status. The maximum data transfer that can be made is 5120 words to maintain RL02 emulation.

Table 6-5. Multipurpose Register (774406)
(During a GET STATUS Command)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDE	CHE	WL	SKTO	SPE	WGE	VC	DSE	DT	HS	C0	H0	BH	ST0	STB	STA

Table 6-5. Multipurpose Register (774406) (Cont'd)

Bit	Description	Explanation
15	WDE	WRITE DATA ERROR. This bit is used to indicate a write fault condition, and is set if the selected drive's write fault status is true. It is reset by a DRIVE RESET GET STATUS command or by a BUS INIT.
14	CHE	CURRENT HEAD ERROR. Unused, set to zero.
13	WL	WRITE LOCK. Unused, set to zero.
12	SKTO	SEEK TIME OUT. This bit is set if the WINC-08 waits for one second without receiving DRIVE READY status from the selected physical drive. Reset by a DRIVE RESET GET STATUS command.
11	SPE	SPIN ERROR. This bit is used by the WINC-08 to indicate a drive fault condition. If a drive fault is detected during a data transfer operation, the OPI bit is set in the CSR register. Performing a GET STATUS command will show a spin error.
10	WGE	WRITE GATE ERROR. Unused, set to zero.
9	VC	VOLUME CHECK. Unused, set to zero.
8	DSE	DRIVE SELECT ERROR. Unused, set to zero.
7	DT	DRIVE TYPE. Set to one.
6	HS	HEAD SELECT. Indicates the logical head selected by a SEEK or READ/WRITE command.
5	CO	COVER OPEN. Unused, set to zero.
4	HO	HEADS OUT. Set to one.
3	BH	BRUSH HOME. Set to one.
2-0	STATE	BITS 2-0 are set to a one-zero-one configuration to indicate the LOCKON drive state.

Table 6-6. Multipurpose Register (774406)
(During a READ HEADER Command)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Logical Cylinder Address (Bits 15 through 7)									H	Sector Address (Bits 5 through 0)					
	CA8								CA0	S	SA5					SA0

Bit	Description	Explanation
15-7	CA	LOGICAL CYLINDER ADDRESS. Indicates the logical cylinder address of the selected logical unit at the time of the last SEEK or DATA TRANSFER.
6	HS	HEAD STATE. This bit indicates the logical head of the currently selected logical unit.
5-0	SA	SECTOR ADDRESS. Unused, set to zero. A READ HEADER command on the WINC-08 is a logical operation rather than a physical read.

6.4 WINCHESTER EMULATION COMMANDS

The following function codes are shown in paragraph 6.3.1.

6.4.1 NO-OP. FUNCTION CODE 0 (CSR OUTPUT 0)

The NO-OP command performs no explicit function. However, execution of the NO-OP will cause the microcode to perform the command dispatch and command completion functions resulting in an update of the interface status registers and an interrupt if IE is set.

6.4.2 WRITECHECK. Function Code 1 (CSR Output 2)

The WRITECHECK command is normally used to verify that a WRITE operation resulted in valid data on the disk. After a WRITE operation, a WRITECHECK may be performed which will read the data from the disk and compare it with the data in the CPU memory. An error will result if the data does not compare or if an ECC error is detected. Note that the WINC-08 does not use the ECC correction capability during a WRITECHECK operation. A sector could generate an error during a WRITECHECK

operation that may be correctable by the ECC during normal read operations.

The setup of the CSR register for a writecheck command is the same as used for the corresponding write command with only the function bits different. The BA register must be loaded with the address of the first location of the data block in the main memory. The word count register should be loaded with the negative of the data block, which may be a partial sector if desired. Partial sectors will be compared until the word counter reaches zero, then the microcode will verify the ECC at the end of the sector.

When the WRITECHECK command is issued, the microcode will seek to the desired cylinder and head if needed, and will then begin searching for the requested sector. When the sector is found, the data field is read into the WINC-08 internal buffer and then compared with the data in the CPU memory, unless an ECC error was detected. Any error will result in up to eight retries. If the retries are not successful, the DCRC bit in the CS register will be set. The number of retries is accumulated in the maintenance retry count register. The BA, DA, and MP registers are updated at the completion of an error-free sector.

6.4.3 GET STATUS. FUNCTION CODE 2 (CSR OUTPUT 4)

If the GS bits in the Disk Address (DA) register are set, the WINC-08 will place the drive status in the Multipurpose (MP) register, set CRDY, and interrupt if IE is set. If the GS and RST bits are set in the Disk Address (DA) register, the WINC-08 will perform a drive reset consisting of clearing all internal drive error status bits and issuing a FAULT CLEAR command to the drives; it will then perform the normal GET STATUS posting. Whenever a GET STATUS command is issued, the WINC-08 will post the status in the MP register, set the CRDY bit in the CS register, and interrupt if the IE bit is set. This function may be performed any time the controller is ready, even though the drive may not be ready, for

example, during a SEEK or while spinning up. The drive state code bits will always indicate a LOCKON condition. The DRDY bit in the Control Status (CS) register will be off during a SEEK and while spinning up. If the DA register is set to 364 octal, the WINC-08 will not perform a GET STATUS function, but will instead set an internal flag so that the next command received will be executed as a special maintenance command. All special maintenance commands will reset the flag, returning the WINC-08 to normal emulation operation. See Section 6.5 for the maintenance commands.

6.4.4 SEEK. FUNCTION CODE 3 (CSR OUTPUT 6)

If bit 0 in the Disk Address (DA) register is a one, the WINC-08 will set CRDY as soon as the difference count is sent to the drive and will interrupt if IE is set. Upon receipt of the difference count the drive will begin seeking. Since the WINC-08 comes ready and interrupts as soon as a SEEK is issued, it is possible to issue seeks to additional drives while the first is seeking. However, no interrupt occurs when the seeks are completed. So, it is recommended that the transfer command be issued as soon as all seeks are issued, to the drive that requires the shortest seek. In this way, the drive completing its seek first will immediately perform its transfer and interrupt when done.

Since the WINC-08 comes ready and interrupts as soon as the drive has received the seek command, it is possible to issue seeks to other logical or physical units while the first unit is still seeking. Attempting to perform overlapped seeks on two logical units both on the same physical drive will most likely result in disk crashing and is not recommended. A sequence that will seek Logical Unit Zero, seek Unit One, read Unit Zero, and then read Unit One is not recommended. Sequential seek commands to the same physical, but different logical, units will result in excessive seek operations. A better sequence would be to skip the seeks and just issue the two reads, letting the WINC-08 issue the implied seeks.

If the difference count results in an address greater than the innermost (Track 511) limit, the address will be set to the innermost limit. If the difference count results in an address less than the outermost (Track 0) limit, the WINC-08 will perform a rezero operation on the drive and will set the address to zero.

6.4.5 READ HEADER. FUNCTION CODE 4 (CSR OUTPUT 10)

When a READ HEADER command is decoded with CRDY cleared, the WINC-08 will place the header data in the Multipurpose (MP) register, will set CRDY, and interrupt if IE is set. The CPU may then access the MP register to read the header word to determine the current cylinder or head, or to calculate the difference count for a SEEK operation. Additional reads of the MP register will not cause the data to change, and will yield the same address word each time.

The WINC-08 READ HEADER command will not perform a physical read of the header data on the disk. Each physical WINC-08 drive contains two logical drives which may not be at the same logical cylinder addresses. Physically reading the header of one logical unit might result in the cylinder address of the other logical unit which would not be consistent with the address specified for the first unit. To avoid this conflict and to prevent the disk crashing which could occur, the disk address returned to the CPU will be the current logical position of the selected unit obtained from the WINC-08 internal storage registers.

Note that the primary purpose of the READ HEADER command is to provide an address for seek difference calculations, which are not required on the WINC-08. Both the READ HEADER and SEEK functions may be skipped if desired.

6.4.6 WRITE DATA. FUNCTION CODE 5 (CSR OUTPUT 12)

When a WRITE command is decoded with CRDY cleared, the WINC-08 will issue an implied seek, if needed, and then search for the requested sector header. If no error is detected and an address match is found, the sector specified in the Disk Address (DA) register will be written into the memory location specified in the Bus Address (BA) register. For partial sector writes, the remaining sector area is filled with zeros. At the end of each sector the BA, DA, and MP registers are updated. If the word count has not reached zero, the next sector is written.

Due to emulation requirements, the WINC-08 will not perform spiral write or read operations. When the last sector of a logical head is written, the sector number will be incremented to 41 which is an illegal sector number. If the word count has not reached zero, the WINC-08 will attempt to write sector 41, resulting in an HNF (HEADER NOT FOUND) error. At the end of the transfer CRDY will be set and an interrupt requested if the IE bit is set.

6.4.7 READ DATA. FUNCTION CODE 6 (CSR OUTPUT 14)

When a READ command is decoded with CRDY cleared, the WINC-08 will issue an implied seek, if needed, and then search for the requested sector header. If no error is detected and an address match is found, the sector specified in the DA register will be read into the memory location specified in the BA register. For partial sector reads, the transfer will end when the word count reaches zero, but the WINC-08 will still check the sector for an ECC error status. If any error is detected during any read, up to eight retries will be attempted with an attempted ECC correction each time, if possible. The BA, DA, and WC registers are updated at the end of each sector, and, if the word count register has not reached zero, the next sector will be read. At the end of the transfer, CRDY will be set and an interrupt will be requested if

IE is set. A count of all retries and ECC corrections is kept in WINC-08 internal maintenance registers. Refer to the special FILL/EMPTY BUFFER function description in paragraph 6.5.2 for the location of the ECC corrections and read retry counters.

6.4.8 READ DATA WITHOUT HEADER CHECK. FUNCTION CODE 7 (CSR OUTPUT 16)

This function is not supported by the WINC-08. Function 7 is treated the same as a NO-OP command (function 0).

6.5 WINCHESTER MAINTENANCE MODE

The WINC-08 may be switched into a special maintenance mode by issuing a GET STATUS function request with the DA register set to 364 octal (see paragraph 6.4.3, GET STATUS). The special maintenance mode flag is cleared at the completion of each special function and the WINC-08 returns to emulation mode.

The following paragraphs describe the registers and maintenance commands.

6.5.1 CONTROL STATUS REGISTER (774400)

The CSR bit definitions differ, when in maintenance mode, only in the specification of the function bits. See paragraph 6.3.1 for the other bit definitions. See Table 6-7 for the function bit descriptions when in the maintenance mode.

Table 6-7. Control Status Register (774400)
(Maintenance Mode)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERROR	DISK ERROR	NXM	HNF&DLT	HCRC&DCRC	OPI	DSI	DSO	CRDY	IE	BA17	BA16	FUNC2	FUNC1	FUNC0	DRDY

Bit	Description	Explanation
3-1	FUNC 2 FUNC 1 FUNC 0	These three bits contain the maintenance command function to be performed by the WINC-08 when CSR bit 7 is set to a zero. See paragraph 6.5.5 for additional details on these commands.

Function	Command	CSR Code
000	NO-OP	0
001	UNUSED (ERROR)	2
010	FILL/EMPTY BUFFER	4
011	UNUSED (ERROR)	6
100	UNUSED (ERROR)	10
101	WRITE DATA/ECC	12
110	READ DATA/ECC	14
111	DISK FORMAT	16

6.5.2 BUS ADDRESS REGISTER (774402)

This is a 16-bit Bus Address (BA) register. BA expansion bits 16 and 17 are contained in CSR bits 4 and 5. The contents of the BA register indicates the address of the CPU memory to be used for data transfers. During maintenance read or write functions, this register overflows into the expansion bits and is updated at the completion of the sector. The BA register is not changed when used with a fill/empty buffer function. The BA register is cleared with a BUS INIT command or by loading with all zeros.

6.5.3 DISK ADDRESS REGISTER (774404)

This register is used with the maintenance functions. The register is cleared by a BUS INIT command or by loading with all zeros.

Table 6-8. Disk Address Register (774404)
(Maintenance Mode)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Not Used (Bits 15 through 1)															DIR

Bit	Description	Explanation
15-1		NOT USED
0	DIR	DIRECTION. Set bit 0 to zero to empty the buffer into the CPU memory. Set bit 0 to one to fill the buffer from CPU memory.

The specification for this register during SPECIAL READ/WRITE is the same as when used for an emulation read or write function (see Table 6-3).

Table 6-8. Disk Address Register (774404)
(During Special Read or Write)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Cylinder Address (Bits 15 through 7)									H	Sector Address (Bits 5 through 0)					
	CA8								CA0	S	SA5					SA0

Table 6-8. Disk Address Register (774404) (Cont'd)

Bit	Description	Explanation
15-7	CA	CYLINDER ADDRESS. Logical cylinder address from 0 to 511 for data transfer. This address will be mapped by microcode into the physical address for the data transfer. If the heads are not on the requested cylinder, the microcode will perform a seek operation before the I/O.
6	HS	HEAD SELECT. This bit selects the logical head number to be selected.
5-0	SA	SECTOR ADDRESS. Logical address of the selected sector from 0 to 40. The logical address is mapped by microcode into physical address.

6.5.4 MULTIPURPOSE REGISTER (774406)

Table 6-10. MP Register During Special NO-OP Command (774406)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FBTM	Unused (Bits 14-11)				TIME	INT	MASTER	SECTOR	INDEX	TRK 0	DNRDY	SEEK	FAULT	RWDONE	BINIT

Bit	Description	Explanation
15	FBTM	FIFO BYTE TIME. This bit indicates that the WINC-08 FIFO has completed one byte of data. This bit is used by microcode during a header search operation and may be either a one or a zero during a special NO-OP.

Table 6-10. MP Register During Special NO-OP Command (774406) (Cont'd)

14-11		UNUSED. These bits are not used and may be either ones or zeros.
10	TIME	HARDWARE TIMEOUT STATUS BIT. The WINC-08 contains a hardware watchdog timer which must be periodically reset by the microcode. Because this timer is reset by the microcode, bit 10 will be a zero.
9	INT	LOW ACTIVE INTERRUPT IN PROGRESS. This bit is reset whenever the microcode requests an interrupt of the CPU. The bit will be set when the CPU accepts the interrupt.
8	MASTER	LOW ACTIVE MASTER STATUS. This bit indicates that the WINC-08 has control of the CPU BUS. The microcode does not post this bit until BUS MASTER has been obtained, therefore, this bit will always be a zero.
7	SECTOR	SECTOR PULSE. This bit is the sector pulse status received from the drive. This pulse will only be on for 1.68 microseconds at the start of each sector, which is 480 microseconds in length.
6	INDEX	INDEX PULSE. This bit is the index pulse status received from the drive. This pulse will only be on once for 1.68 microseconds of each 20.0 millisecond revolution of the disk platter.
5	TRK 0	TRACK ZERO STATUS. This bit will be a one whenever the selected physical drive heads are on physical track zero.
4	D NRDY	LOW ACTIVE DRIVE READY STATUS. This bit is the negative drive ready status from the selected physical drive. This signal shows that the drive is selected and is up to speed to the extent that the drive PLO circuit has synchronized with the clock track.
3	SEEK	LOW ACTIVE DRIVE SEEK COMPLETE STATUS. This bit indicates that the selected physical drive has finished seeking and that the heads are settled on track ready for a read or write operation.

Table 6-10. MP Register During Special NO-OP Command (774406) (Cont'd)

2	FAULT	DRIVE WRITE FAULT. This bit indicates that the selected physical drive has detected one of the following conditions: WRITE GATE WITHOUT DRIVE READY WRITE AND READ GATES BOTH ON WRITE GATE AND MULTI-HEAD SELECTED WRITE GATE WITHOUT SEEK COMPLETE WRITE GATE WITHOUT PROPER WRITE CURRENT
1	RW DONE	READ/WRITE DONE STATUS. This bit indicates that the WINC-08 read/write hardware circuits are in the completed state.
0	B INIT	BUS INIT STATUS. This bit is true when the CPU is issuing a BUS INIT signal. The WINC-08 is unable to obtain BUS MASTER until the BUS INIT signal is gone, therefore, this bit will always be zero.

6.5.4.1 MP Register During Special Data Transfer

Special data transfers include FILL/EMPTY BUFFER and SPECIAL READ/WRITE. The MP register is used to specify the two's complement of the total number of words to be transferred. The special functions operate on only one sector or buffer at a time; therefore, the word counts should be set to 128 bytes or less for all special functions.

6.5.4.2 MP Register During Special Disk Format

The MP register must contain an octal enable code of 177400 in order to write new headers on the drives. If a special format is requested without the enable code, an OPI status will be posted in the CS register and the command will be terminated.

6.5.5 MAINTENANCE COMMANDS

The commands described below are shown in paragraph 6.5.1.

6.5.5.1 **Special NO-OP. Function Code 0 (CSR Output 0)**

The SPECIAL NO-OP command performs two functions. First the MP register is loaded with status from the WINC-08 control board and from the selected drive. Next, the first 16 bytes of data in the WINC-08 internal buffer are pushed into the WINC-08 FIFO, the 16 bytes of data are pushed from the FIFO back into the buffer. The buffer should be filled and read, using the special fill/empty buffer command. The special mode flag is cleared, copy is set, and an interrupt is requested if IE is on.

6.5.5.2 **Special FILL/EMPTY BUFFER. Function Code 2 (CSR Output 4)**

The WINC-08 internal buffer area consists of two sections. The data I/O buffer is 256 bytes and is used during reading and writing to buffer the sector data. The internal register storage area is used by the microcode to keep the ECC corrections counter, and the retries counter as well as other microcode flags and variables. The BA register specifies the CPU memory area to be used during the fill or empty operation. The MP register specifies the negative word count and should not be more than 128 words. The DA register specifies the transfer direction. A zero indicates an empty transfer from the buffer to the CPU and a one indicates a fill transfer into the buffer from the CPU.

When the EMPTY BUFFER function is performed, the WINC-08 data buffer is first transferred into the CPU memory, then the register storage buffer is transferred into the data buffer which may be read by issuing another EMPTY BUFFER command. This results in reading the ECC corrections counter, the read retries counter, and the special read ECC data. The ECC counter consists of two bytes starting at octal buffer location 366.

The read retries counter is two bytes starting at octal buffer location 364. The special read ECC data begins at octal buffer location 362 and consists of three bytes of ECC data from the sector read, one byte of zeros, and three bytes of data from the hardware ECC registers.

When the FILL BUFFER function is performed, the WINC-08 data buffer is first filled from the CPU memory, then the register storage buffer is filled from the data buffer. The active microcode register storage area is not written to, however. Only the unused area, the ECC corrections counter the retries counter, and the SPECIAL READ ECC data areas are written. This function provides the means to clear or set the counters and ECC data.

6.5.5.3 Special Write. Function Code 5 (CSR Output 12)

This function provides a means of forcing a sector data field to contain an ECC error and is used in the WINC-08 ECC diagnostic. The FILL BUFFER special function must be used to set the ECC data into the WINC-08 register storage buffer. When a special write function is issued, the microcode will increase the sector byte count so that the hardware ECC data will be delayed beyond the normal sector ECC area. The microcode will then append the stored ECC data onto the end of the data field to simulate a hardware ECC which will be used during a normal read function. Due to the increased sector size caused by delaying the hardware ECC data, the sector will extend into the header area of the next physical sector unless the sector used is the last physical sector of the track. The last sector address on the track (41) will contain the extra bytes left from the division of the track into 42 sectors and will have enough room for the delayed hardware ECC data. Setup for the special write function is the same as for a normal write operation except that the register buffer must be filled with a known ECC and the WINC-08 must be set in the special maintenance mode before the special write is issued.

6.5.5.4 Special Read. Function Code 6 (CSR Output 14)

This function performs a normal read of the sector data field. At the end of the data, however, the microcode will move the three ECC bytes and the three hardware ECC registers into the register buffer area. This data may then be read by the CPU by using the special read command twice.

6.5.5.5 Disk Formatter. Function Code 7 (CSR Output 16)

Before the disk drives may be used in a WINC-08 system, they must be formatted with sector header fields. The special format function is provided for disk formatting. Initializing the data fields and creating the bad block files is a CPU function performed by the WINC-08 routine RLMFV (see paragraph 3.3). To execute the special format function, the microcode must first be in the special maintenance mode and the MP register must contain an octal 177400.

6.6 FLOPPY EMULATION

Emulation of the floppy is given in the FLEX-02 Operation and Maintenance Manual and is not repeated here.