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AMDAHL 4705
Communications Processor
Operation Manual

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REVISION NOTICE

The 01B version of this manual adds instructions for the RIPL (Remote Initial Program Load) and Remote Power Off features.

ABSTRACT

This manual provides the Amdahl representative at each Amdahl 4705 customer site with information on the Amdahl 4705 Communications Processor operating procedures.

READER COMMENT FORM

A reader comment form is provided at the end of this manual. If this form is not available, comments and suggestions may be sent to Amdahl Corporation, Technical Publications, Mail Stop 323, P.O Box 470, Sunnyvale, CA 94086. All comments and suggestions become the property of Amdahl Corporation.

PREFACE

This Operation Manual describes the operating procedures of the operator panel of the AMDAHL 4705 Communications Processor (CP), and is mainly applicable to the FE and operator.

This manual describes only the program-independent functions that are executed by hardware alone, except IFT operating procedures.

For a description of the program-dependent functions that are executed by both the hardware and particular CP control program (EP, NCP etc.) resident in the main storage of the CP, refer to the related software publications.

This manual is divided into five chapters and the reference material for maintenance is given in Appendixes.

Chapter 1	Basic Operating Procedures
Chapter 2	Advanced Operating Procedures
Chapter 3	Problem Solving Procedures
Chapter 4	Description of CP Operator Panel
Chapter 5	IFT Program Operating Procedures
Appendixes:	Reference material

Numbers corresponding to those used to identify the location of switches and lamps on the operator panel drawing, Fig. A.2 (in appendix), appear in text, on flowcharts and in drawings enclosed in boxes. "Channel Interface: Internal", for example, means "Depress the INTERNAL switch of the CHANNEL INTERFACE SWITCH (the "Internal" lamp will light)."

For the meaning of abbreviations used in this manual, refer to "Appendix A: Abbreviations".

WARNING - This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which cause the user at his own expense will be required to take whatever measures may be required to correct the interference.

CONTENTS

ILLUSTRATIONS

TABLES

CHAPTER 1
BASIC OPERATING PROCEDURES

This chapter describes the basic procedures for using the CP.

1.1 OPERATING PROCEDURE FROM TURNING POWER ON TO START OF PROGRAM OPERATION

The operation shown in Fig. 1.1 is required when using the CP.

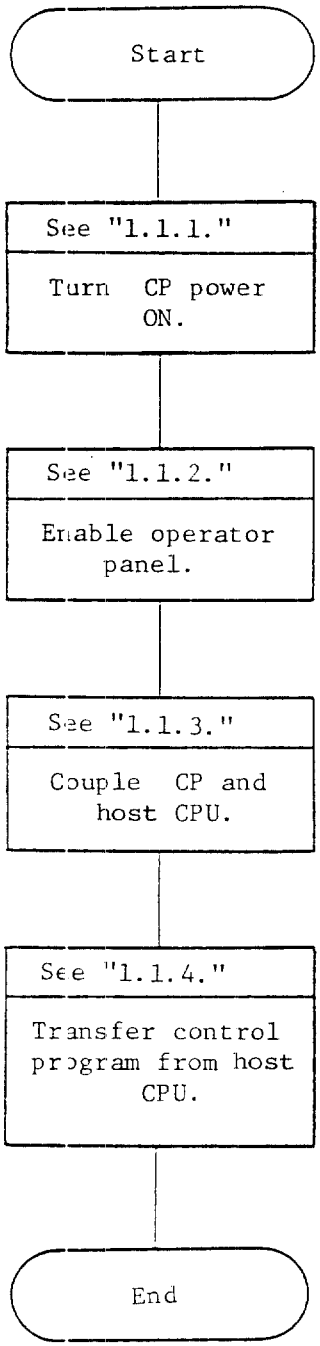


Fig. 1.1 Operating procedure from turning power ON to start of program operation

1.1.1 Power On Procedure

The operation shown in Fig. 1.2 is required for turning on the power of CP.

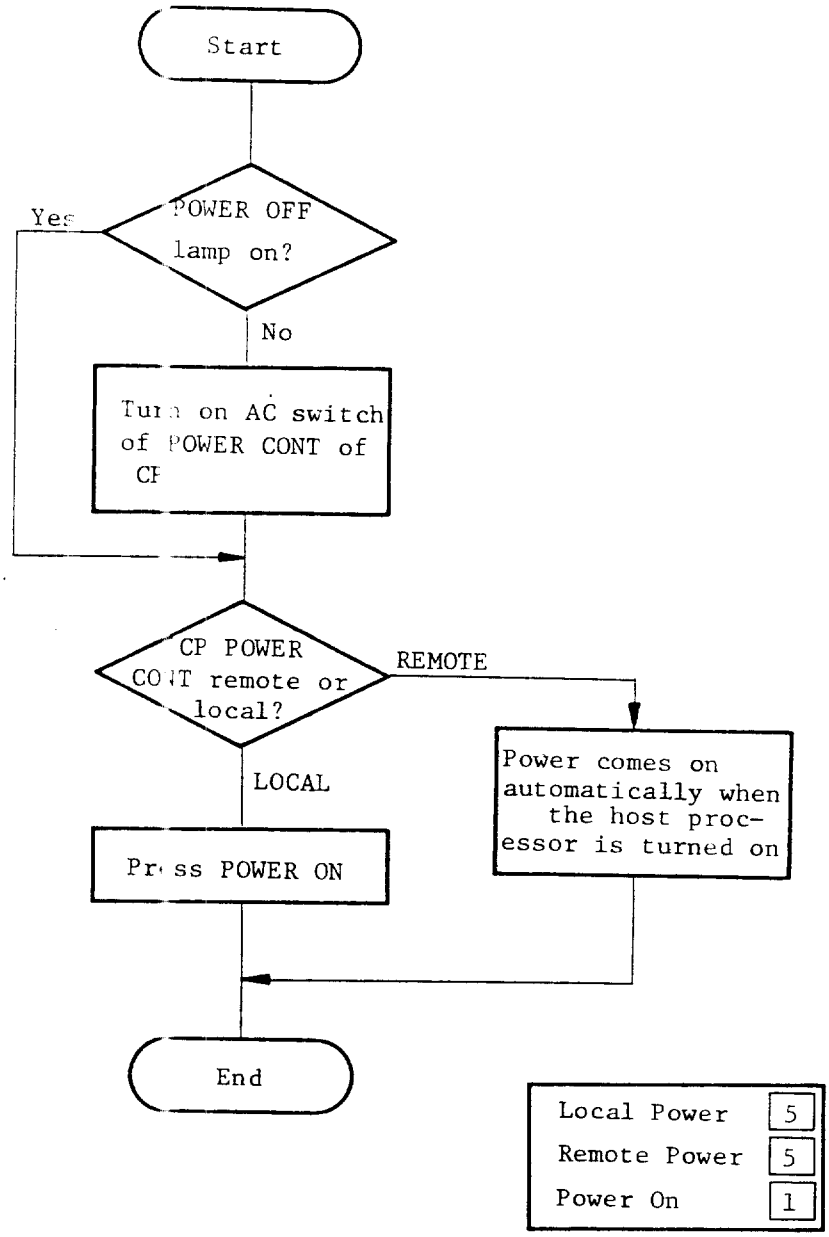


Fig. 1.2 Power ON procedure

1.1.2 Operator Panel Enable/Disable Procedure

When the power is turned on, the operator panel of the CP is in the disabled status. It is therefore necessary to change the operator panel into the enabled status before performing any operations. In addition, the operator panel must be placed in the disabled status during operation for the purpose of preventing erroneous operation from the operator panel. This enable/disable procedure is shown in Fig. 1.3.

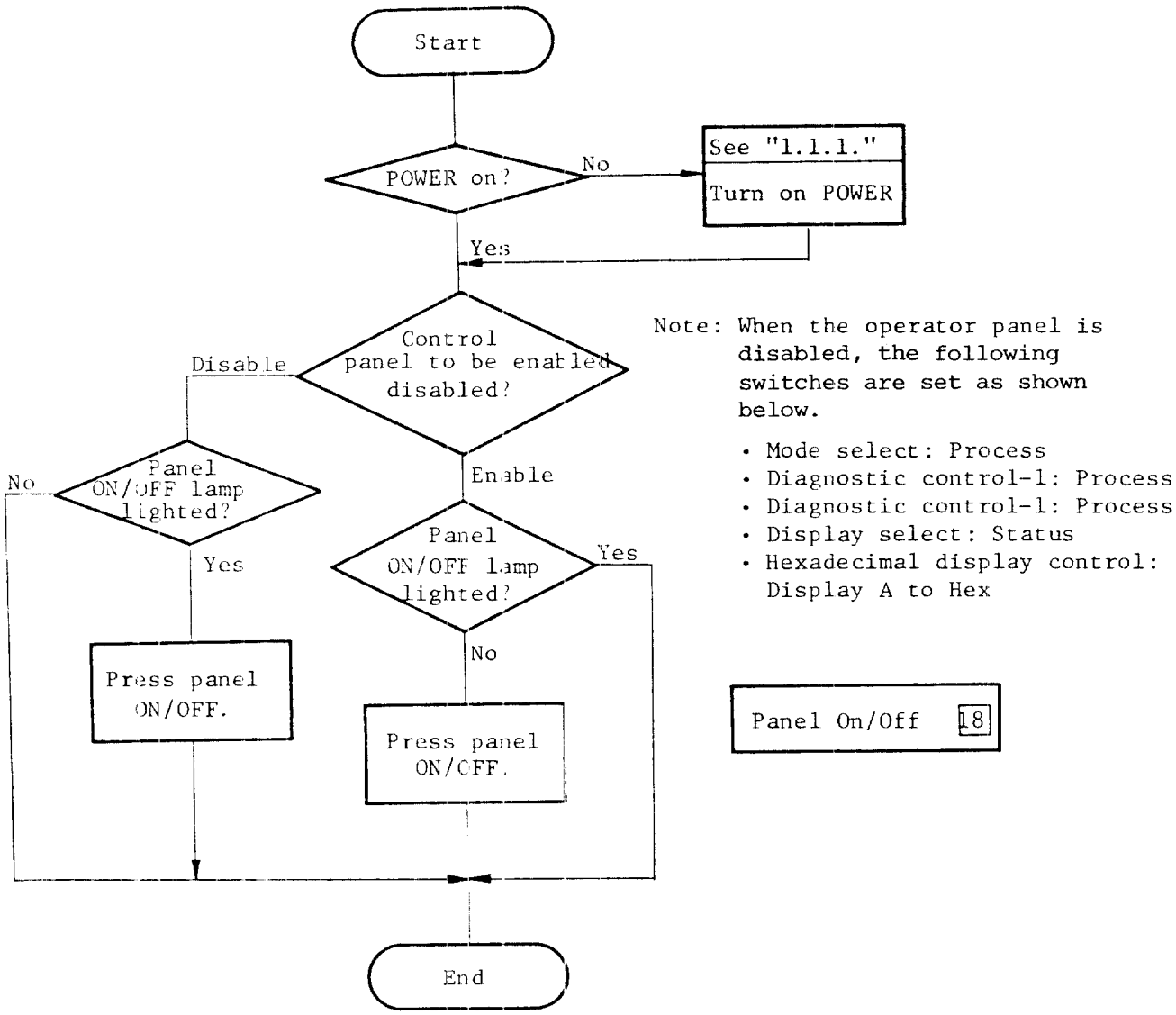


Fig. 1.3 Control panel enable/disable procedure

1.1.3 Channel Interface Coupling Procedure

When coupling the channel of the host CPU and the CP, it is necessary to specify the route of the channel interface through the operation shown in Fig. 1.4. If the route switching operation is made during operation of the channel adapter (CA), subsequent operation of the CP is indeterminant.

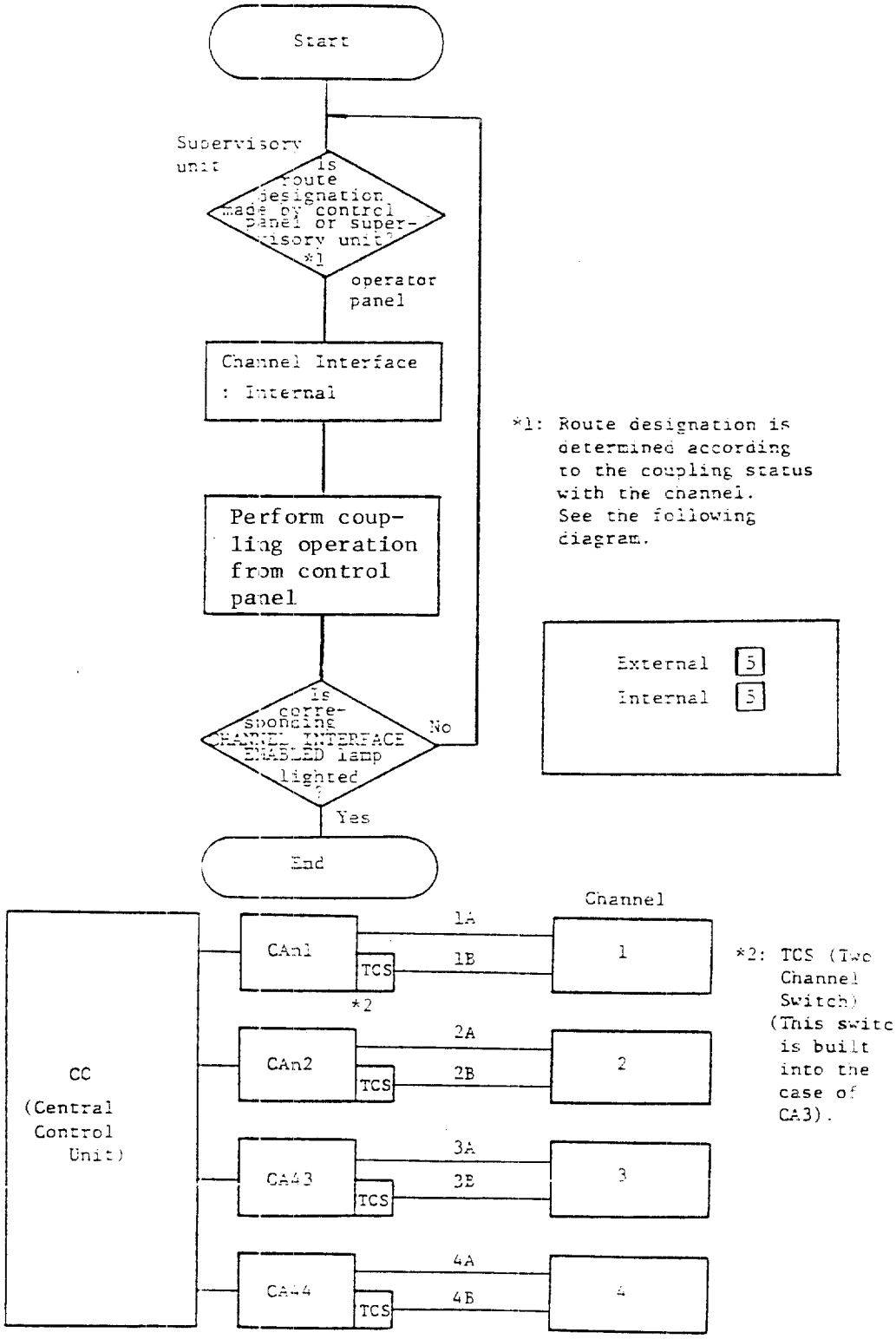
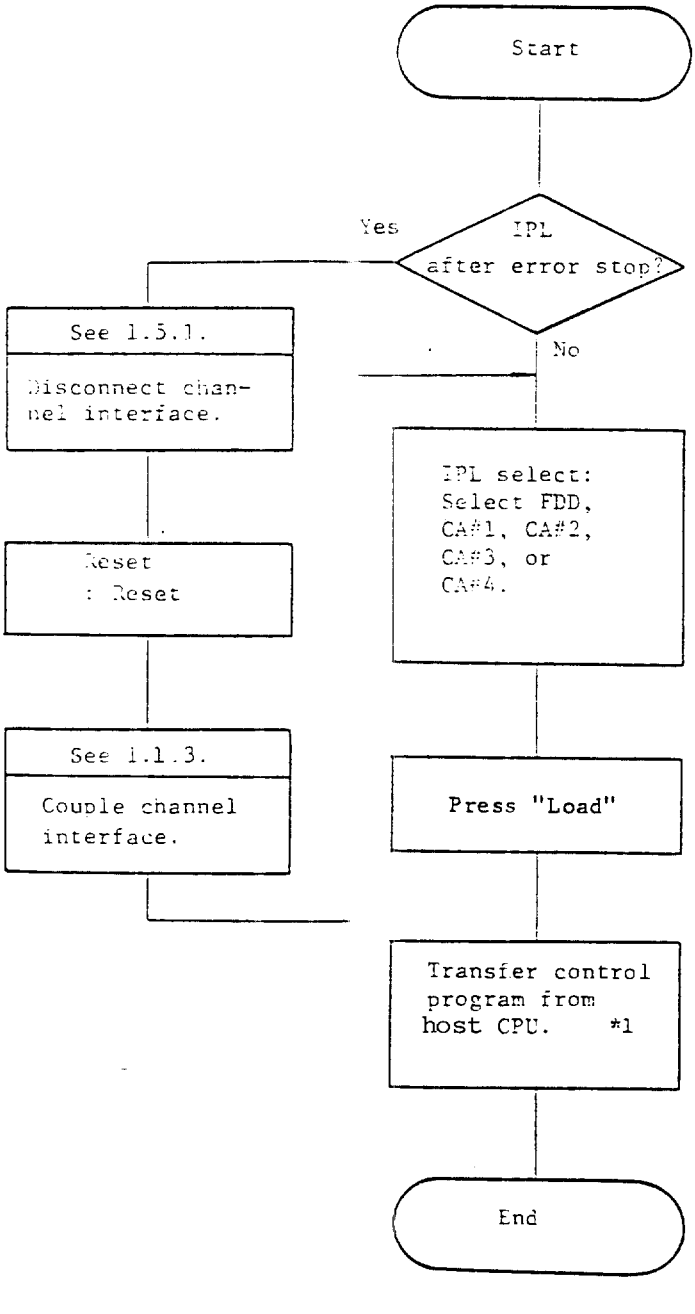


Fig. 1.4 Channel interface coupling procedure

1.1.4 Initial Program Loading (IPL) Procedure

When transferring the control program to the CP, the operation shown in Fig. 1.5 is required. In this case, however, software permitting IPL in the host CPU to which CP is connected must be in operation.



*1: When performing IPL by Flexible Disk Drive (FDD), disconnect the channel interface and change IPL Select to FDD.

Note: This selection is only required for CA4's when NROS is not in use.

FDD	6
CA#1	6
CA#2	6
CA#3	6
CA#4	6
Reset	14
Load	15

Fig. 1.5 IPL procedure

1.1.5 Remote Initial Program Load (RIPL) Procedure

Use the procedure shown in figure 1.6 to load the control program through the local controller from the remote 4705. Refer to the tables on the following pages for explanations of codes and displays.

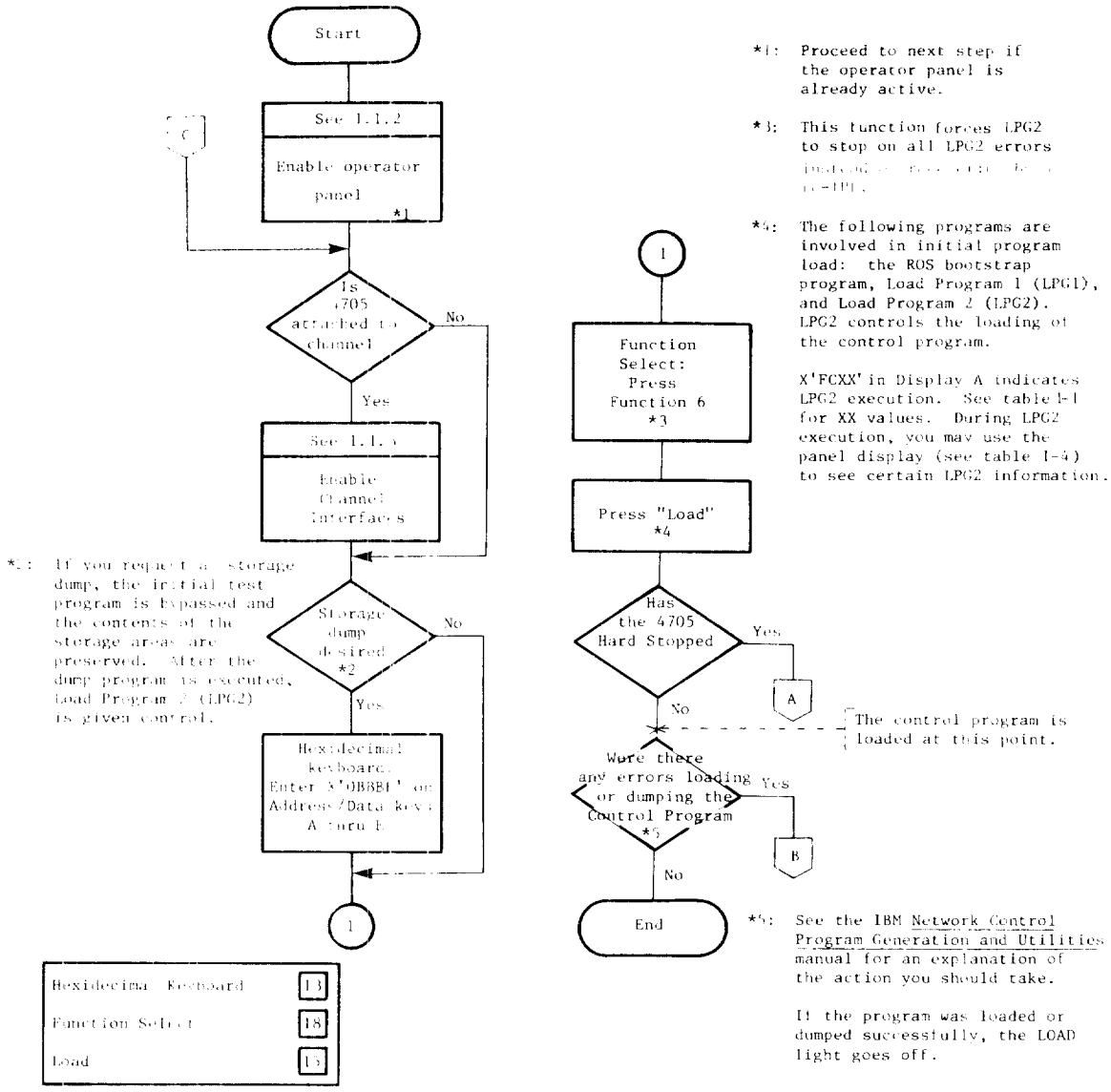


Fig. 1.6 RIPL Procedure

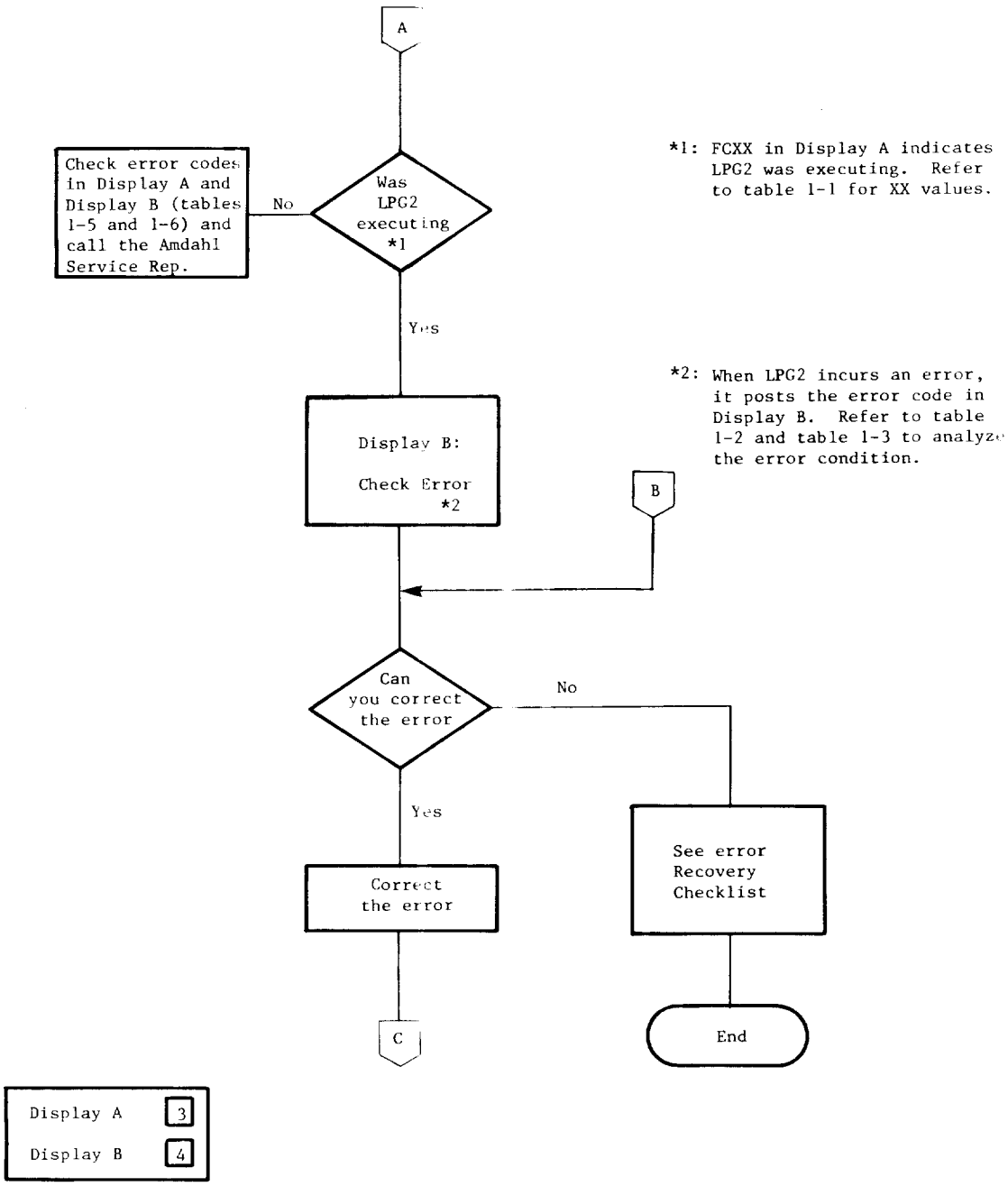


Fig. 1.6 RIPL Procedure (cont)

X'FCXX' in DISPLAY A indicates LPG2 execution. Values for XX -- the IPL sequence indicator -- are shown in table 1-1. These codes indicate the progress of the IPL procedure. Note that the values are OR'd. For example, after the entry point has been received during a load, bits 1.1 and 1.3 would be on. As a result, Display A would show a value of FC50.

Table 1-1. IPL Sequence Indications

XX = IPL Sequence Indicator	Descriptions
1...	Monitor IPL state
.1..	Load state
..1.	Dump state
...1	If load state - entry point received
...1	If dump state - dump-final received
.... 1...	PIU received, response not yet transmitted
.... .0..	Reserved
.... ..1.	High 8K of storage is in from disk
....1	Type 2 Scanner Indicator

Table 1-2 describes the error codes that cause LPG2 to unconditionally hardstop.

Table 1-2. LPG2 Error Codes

DISPLAY B	Error Descriptions
30F0	No SDLC lines defined as active in CDS*
30F2	CDS invalid

* CDS is the remote IPL configuration data set. It is defined as part of the 4705 installation procedure.

Table 1-3 describes the LPG2 abend codes for errors that cause LPG2 to automatically reload itself. If the DISPLAY/FUNCTION SELECT switch is set to FUNCTION 6, these errors cause a hard stop rather than automatic re-IPL.

Table 1-3. LPG2 Abend Codes (conditions causing re-IPL).

Abend code*	Error Descriptions
X'3F01'	No lines active (enable failed or transmit initial failed).
X'3F02'	SDRM (set disconnect response mode) received while monitoring one line. LPG2 re-IPLs to monitor all CDS lines.
X'3F03'	SNRM (set normal reponse mode) received while monitoring one line. LPG2 re-IPLs to monitor all lines.
X'3F04'	Timer expiration. User-specified inactive interval has expired.
X'3F05' X'3F10'	Level 1 error. SIM (set initialization mode) received during the load or dump state.

* If the Network Control Program was running and the DISPLAY/FUNCTION SELECT switch is set at FUNCTION 1, the NCP abend code is displayed in DISPLAY B if an abend occurred.

Table 1-4 describes the LPG2 control panel displays. These displays may be used during LPG2 execution to display certain LPG2 information.

Table 1-4. LPG2 Control Panel Displays

Always press INTERRUPT after setting the DISPLAY/FUNCTION SELECT switch.

DISPLAY/FUNCTION SELECT switch	ADDRESS/DATA switches A B C D E	DISPLAY A	DISPLAY B
Not invoked. Do not press INTERRUPT	Ignored	FCXX (See table 1-1 for XX values)	0XXX last line address (after hardware interrupt)
STORAGE ADDRESS	Address of storage loc	Address entered	Contents of storage location
REGISTER ADDRESS	ORORO R = reg desired	RORO	Contents of storage register
FUNCTION 1	Unused	Status i00s (see Note)	Abend Code (see table 1-3)
FUNCTION 2	00XXX line address	SCF/PDF	LCD/PCF DS leads
FUNCTION 3	Unused	PIU request code XX see table 1-1	Storage pointer
FUNCTION 4	00XXX line address	Receive SDLC Address Character Control Character	Transmit SDLC Address Character Control Character
FUNCTION 5	Receive≠0 Transmit=0 / Dis-plmt	Displacement into PIU	Contents of current PIU
FUNCTION 6	Forces the non-invoked display state and causes LPG2 to hardstop if an error condition occurs (see table 1-3).		

For status in Function 1:

i = IPL information from register X'6B' (see the IBM 3704 and 3705 Principles of Operation manual for information on register X'6B').

s = Four bits indicating which CDS line is in use.

LPG2 is loaded from tracks 6 and 7 (main tracks). When any read error occurs at the main track, it is loaded from tracks 12 and 13 (spare tracks). When the read error occurs at the spare tracks, the read of the main tracks and the spare tracks is alternately tried until the retry counter is exceeded. When the retry counter is exceeded, the hard-stop occurs and X'2222' is displayed on Display A and B. See table 1-5.

Table 1-5. Pane Display in LPG1

Display A (Hexadecimal)	Display B (Hexadecimal)	Contents
2222	2222	The hard-stop is made due to a read error of LPG2.
6B6B	6B6B	The hard-stop is made due to a hard error of the RPL register (See table 1-6)..
AAxx	--	The "xx" indicates the track number to be read.
--	EExx	Indicates that a read error occurred (the "xx" indicates the type of read error). 01 = LPG2 read error 02 = Read error of SAVE program 04 = Read error of SAVE program

Table 1-6 shows the contents of the OBR (Out Board Record) when an error occurs at the remote Communications Processor. The test is done to ensure that the input/output operation of the RPL(X'6B') register performs properly. If the operation is not correct, a hard-stop occurs and X'6B6B' is displayed on Display A and Display B of the panel. Record the contents of the OBR as it is displayed on your panel (See Storage Load/Store Procedure).

Table 1-6. Contents of OBR

Addresses (Hexidecimal)	Contents
0020 to 0021	X'0000' (Fixed)
0022 to 0023	X'2105' (Fixed)
0024 to 0025	IN X'7D' (CC Check Register)
0026 to 0027	IN X'76' (Adapter L1 Interrupt Requests)
0028 to 0029	IN X'7E' (CC L1 Interrupt Requests)
002A to 002B	IN X'79' (Utility Register)
002C to 002F	IN X'74' (LAR)
0030 to 0033	LAR of level 1

RIPL Error Recovery Checklist

Use the following steps as a checklist for determining the possible cause of an error condition.

1. Are all control panel switches set to the proper positions and push buttons pressed according to the procedure you are following?

2. Has the control panel been properly activated? See paragraph 1.1.1.

3. Have you checked all control panel lights for proper indications?

4. Is the channel enabled or disabled according to the procedure you are following?

5. Record all error codes on Display A and Display B.

1.2 HOW TO OBSERVE PROGRAM LEVEL AND CHECK STATUS

The operation shown in Fig. 1.6 is required to observe the program running level, interrupt level, interrupt mask level, and check status when a machine check of the CP occurs.

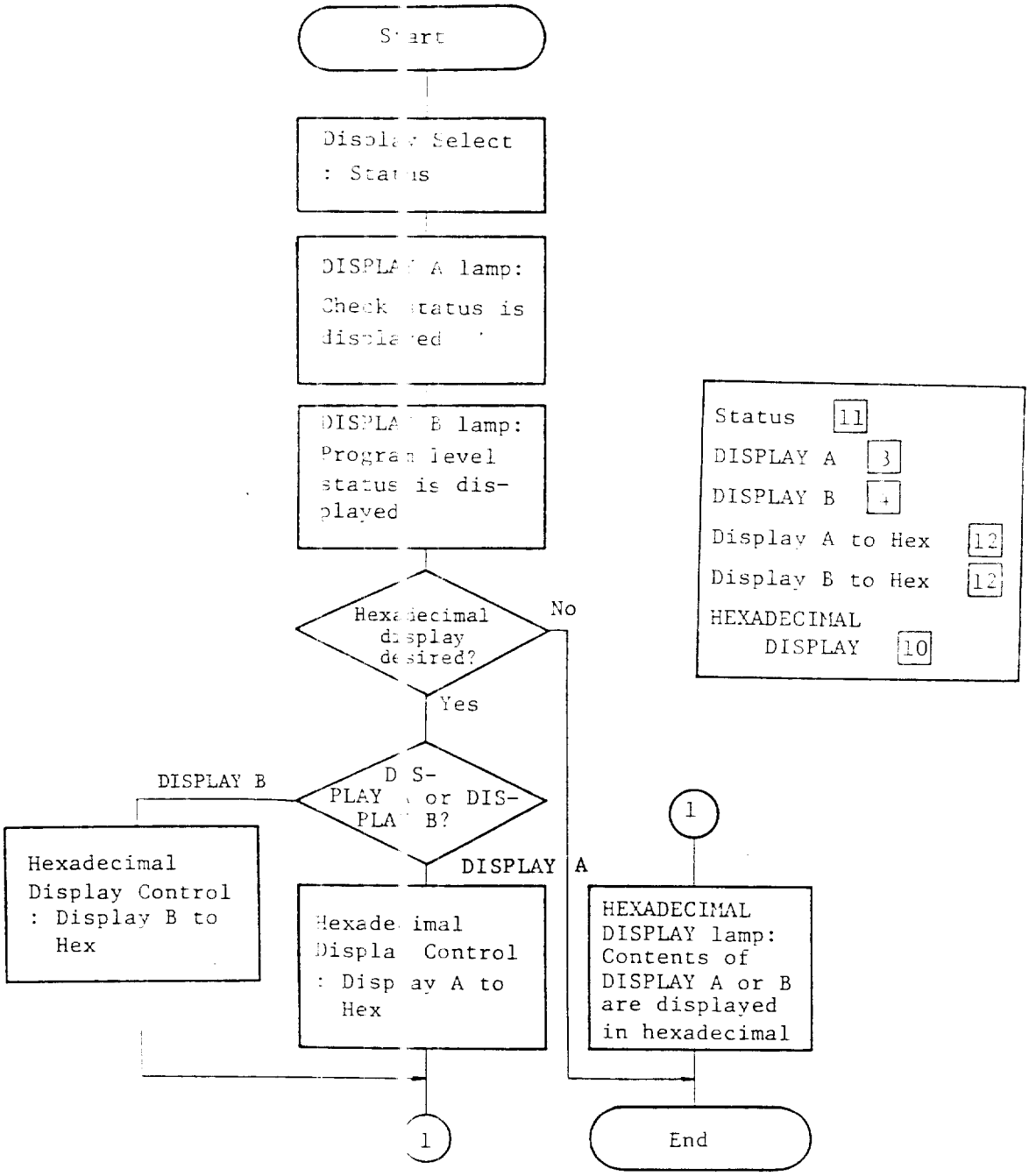


Fig. 1.7 How to observe program level and check status

1.3 CHECK RESET PROCEDURE

If the following checks occur in the CP, their causes can be reset by performing the operation shown in Fig. 1.7.

- CC machine check
- Program check
- Adapter check
- 1-bit check (only when diagnostic control-1 is in storage single read/write or storage scan read/write)

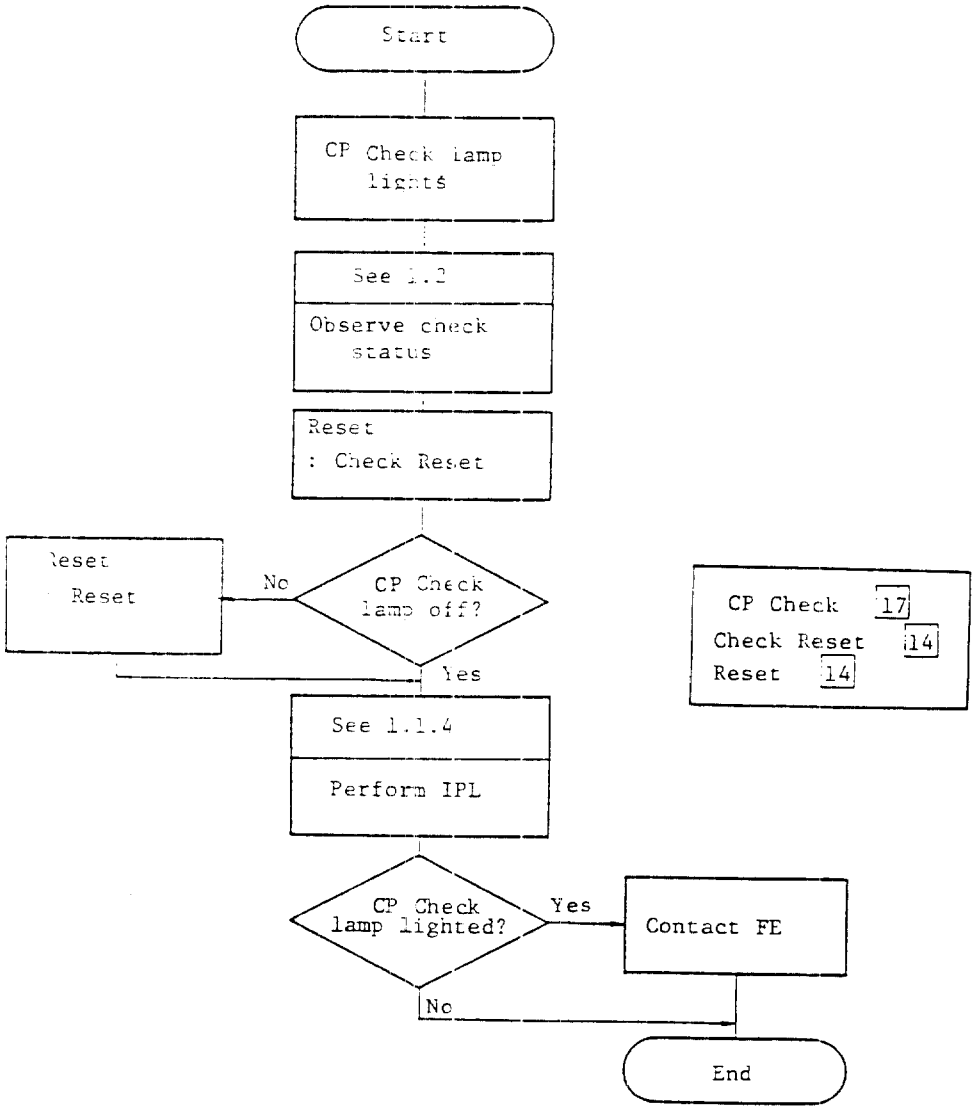


Fig. 1.8 Check reset procedure

1.4 LAMP TEST PROCEDURE

If the lighting status of a lamp seems unusual, lamp test should be made by the procedure shown in Fig. 1.8.

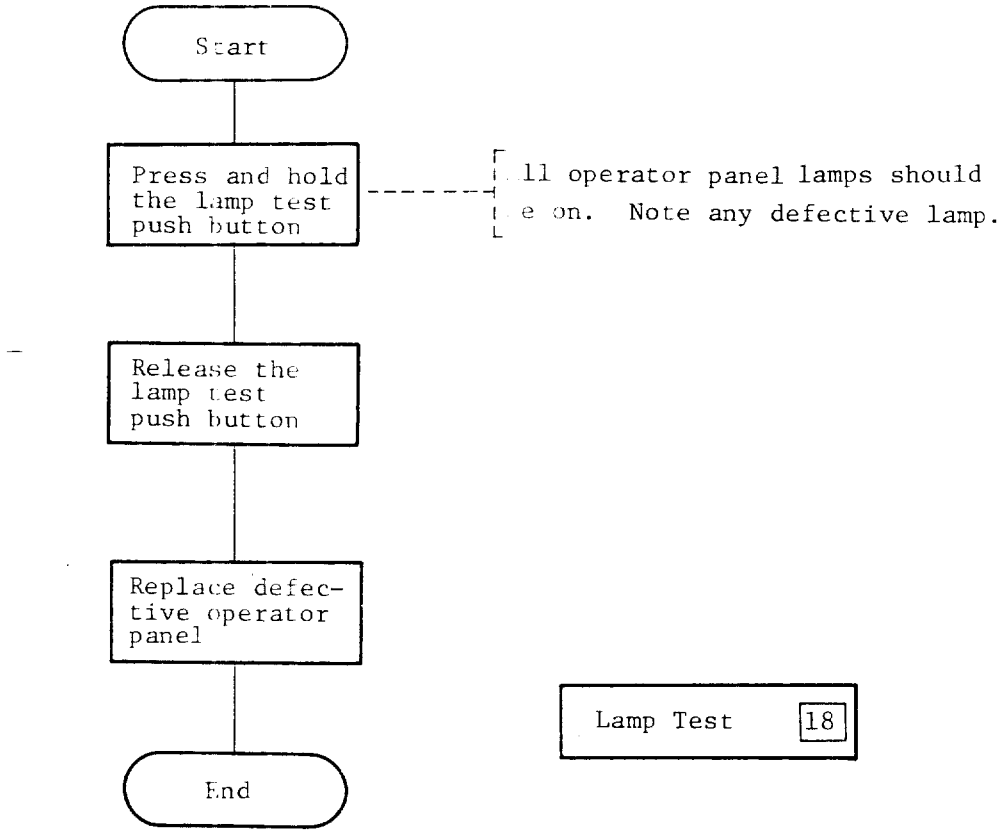


Fig. 1.9 Lamp test procedure

1.5 OPERATING PROCEDURE FROM TERMINATION OF PROGRAM OPERATION TO POWER OFF

The procedure from termination of CP program operation to power off is shown in Fig. 1.9.

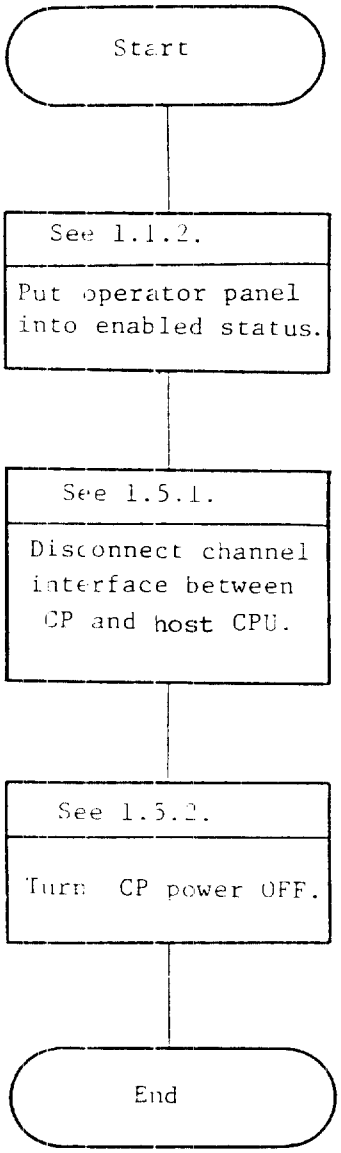


Fig. 1.10 Operating procedure from termination of program operation to power off

1.5.1 Channel Interface Disconnection Procedure

The operation shown in Fig. 1.10 is required for disconnecting the 4705 CP from the channel of host CPU. If the route switching operation is made during operation of the channel adapter, the subsequent operations of the 4705 are not guaranteed.

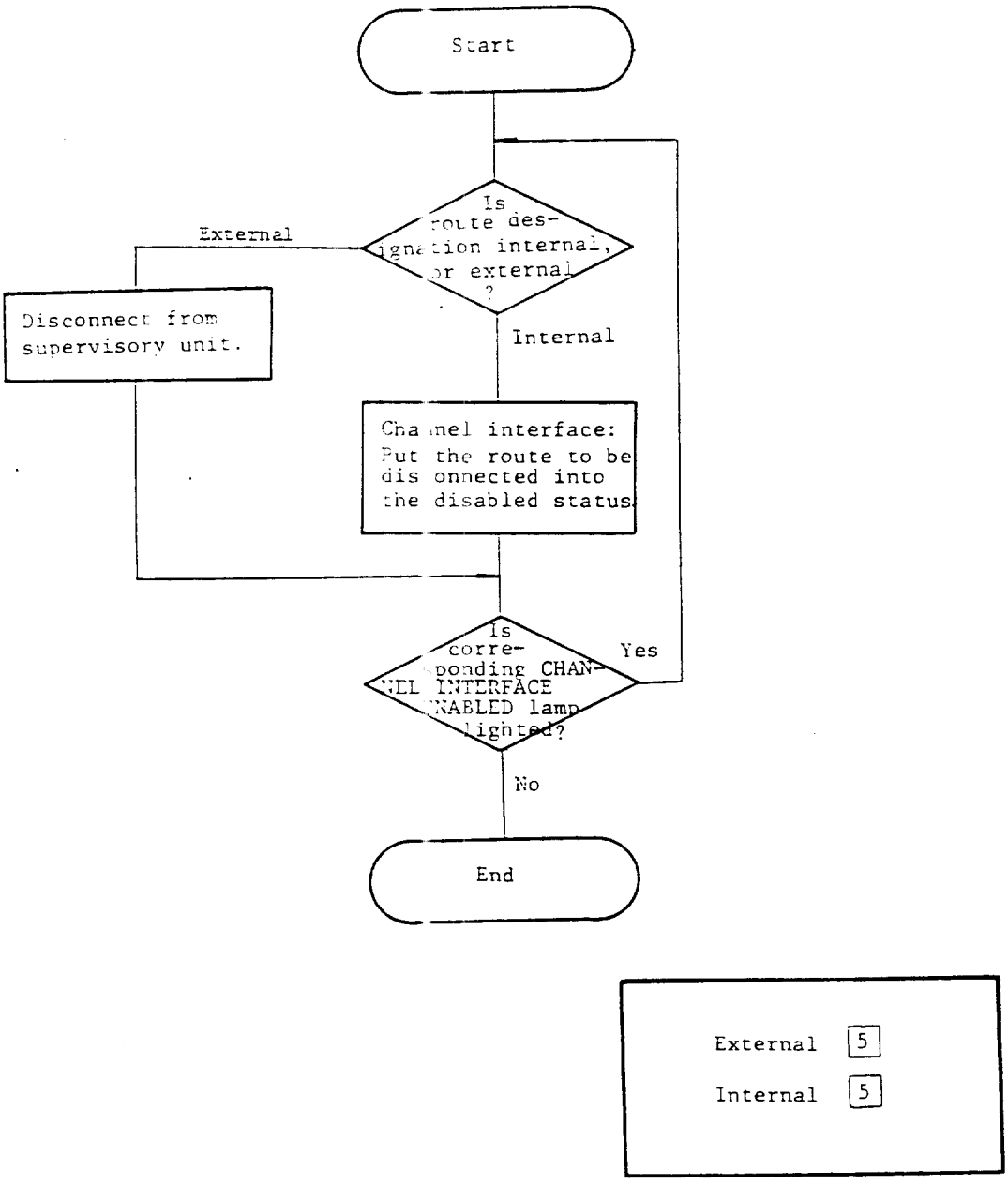


Fig. 1.11 Channel Interface disconnection procedure

1.5.2 Power OFF Procedure

The operation shown in Fig. 1.11 is required for turning CP power off.

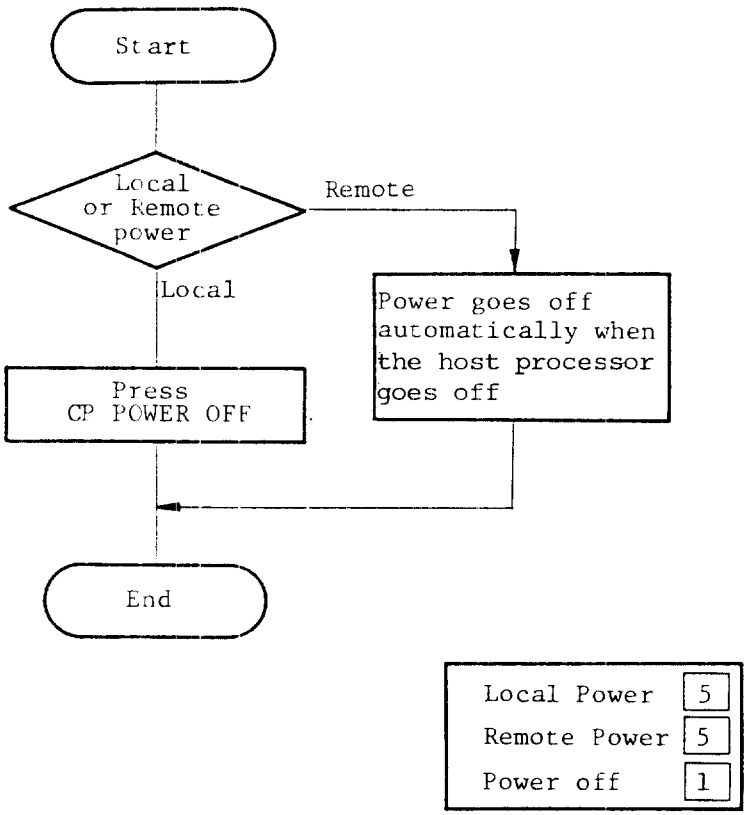


Fig. 1.12 Power OFF procedure

CHAPTER 2

ADVANCED OPERATING PROCEDURES

This chapter describes operating p ocedures for various operator panel functions.

2.1 HOW TO OBSERVE DISPLAY REGIS ER 1/2

The display register 1/2 is set wh n executing OUTPUT X '71' or X '72', or when performing storage load/store, reg ster load/store, storage single read/write, storage scan read/write operations from the operator panel, or when IPL phase is 1/2. The contents can be obser ed by the operation shown in Fig. 2.1.

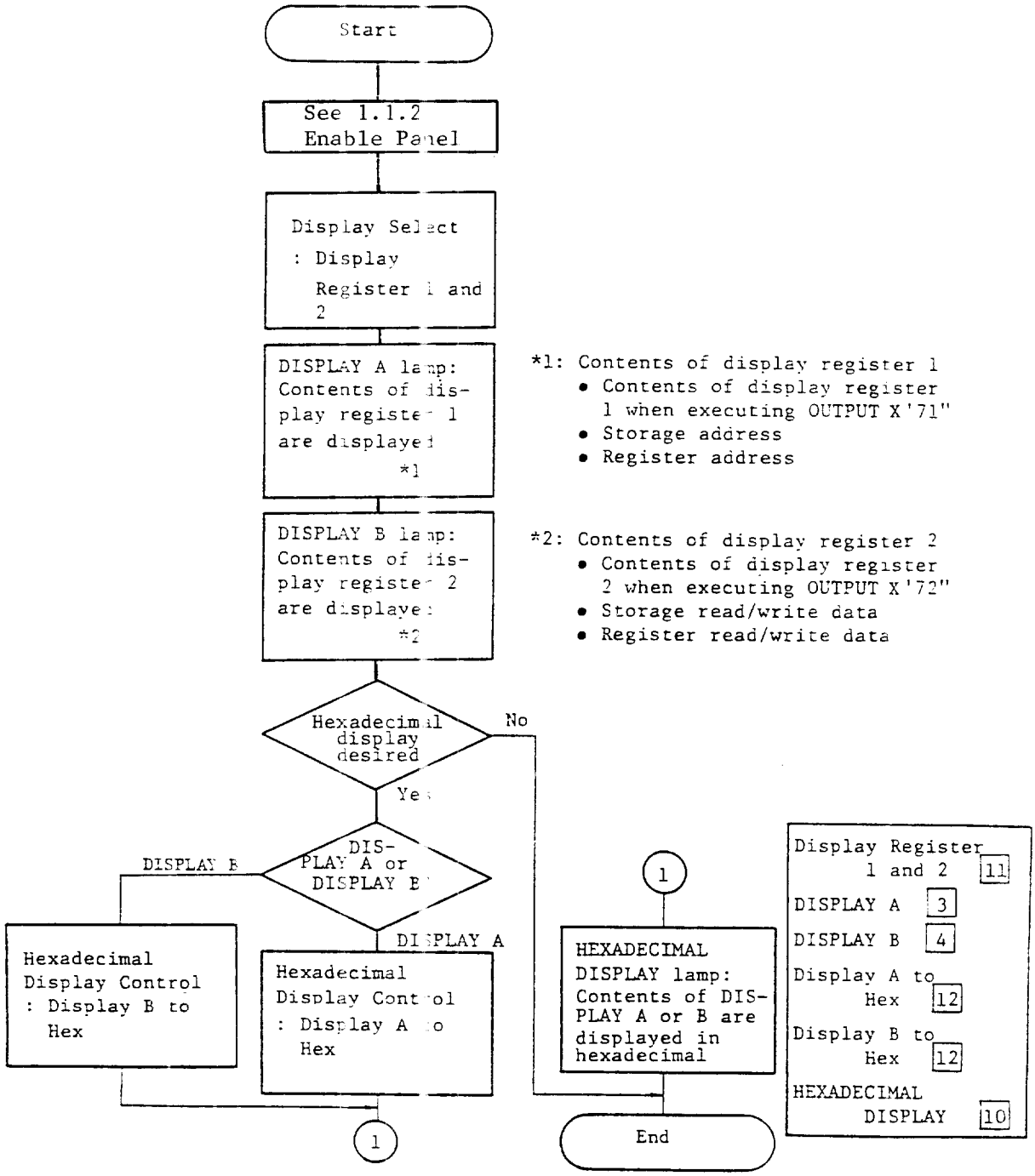


Fig. 2.1 How t observe display register 1/2

The operation shown in Fig. 2.2 is required for executing the instructions in a program one at a time.

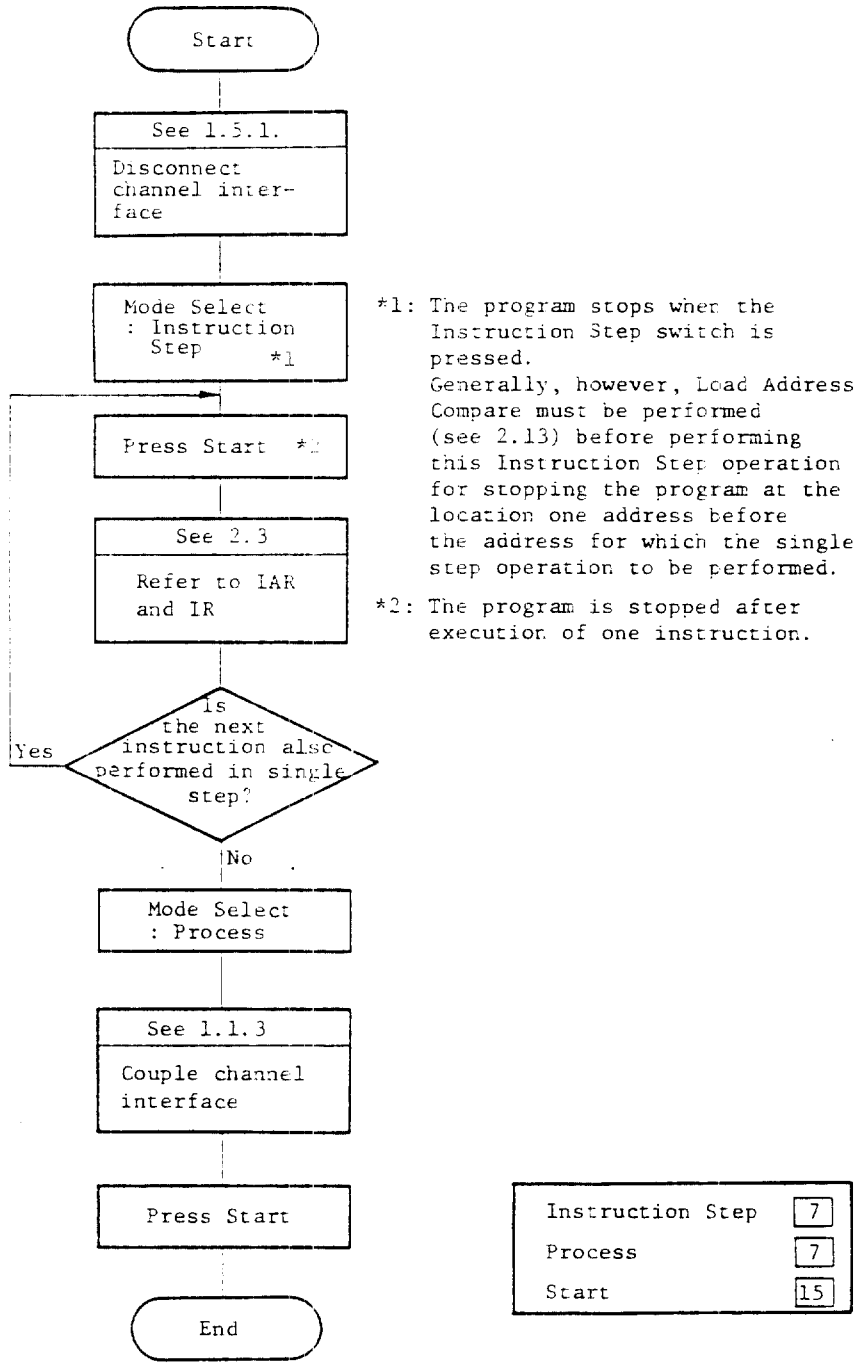


Fig. 2.2 Single-step instruction operating procedure

2.3 HOW TO OBSERVE INSTRUCTION ADDRESS REGISTER (IAR) AND INSTRUCTION REGISTER (IR)

The Instruction Address Register (IAR) contains the storage Address of the next instruction to be executed. (The IAR is called TAR in IBM3705.)

The Instruction Register (IR) contains the first 16 bits of the instruction executed. (The IR is called OP in IBM3705.)

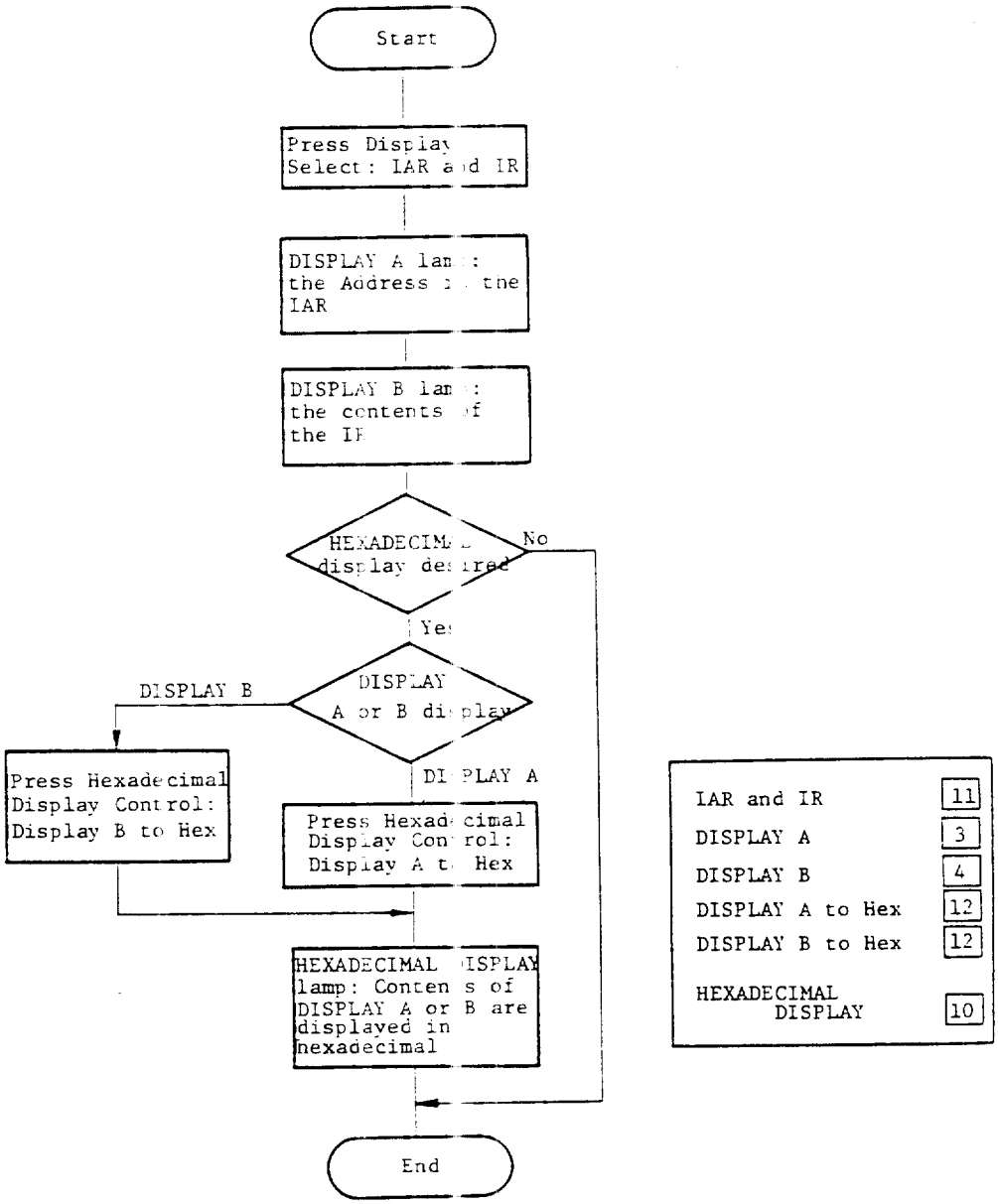


Fig. 2.3 How to observe IAR and IR

2.4 STORAGE LOAD/STORE PROCEDURE

The operation shown in Fig. 2.4 is required for data loading/storing to the storage.

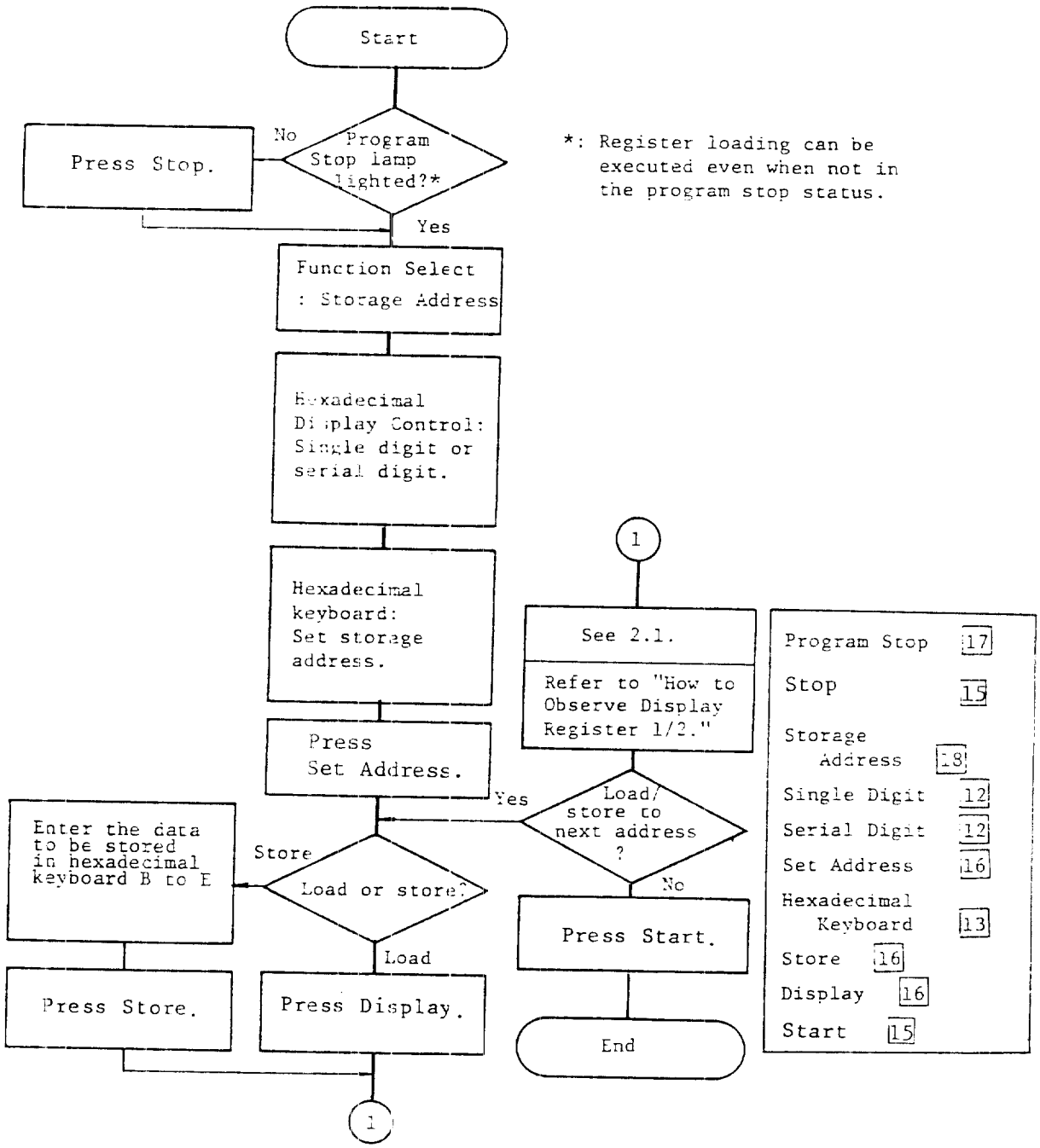


Fig. 2.4 Storage load/store procedure

2.5 REGISTER LOAD/STORE PROCEDURE

The operation of Fig. 2.5 is required for data loading/storing to the register.

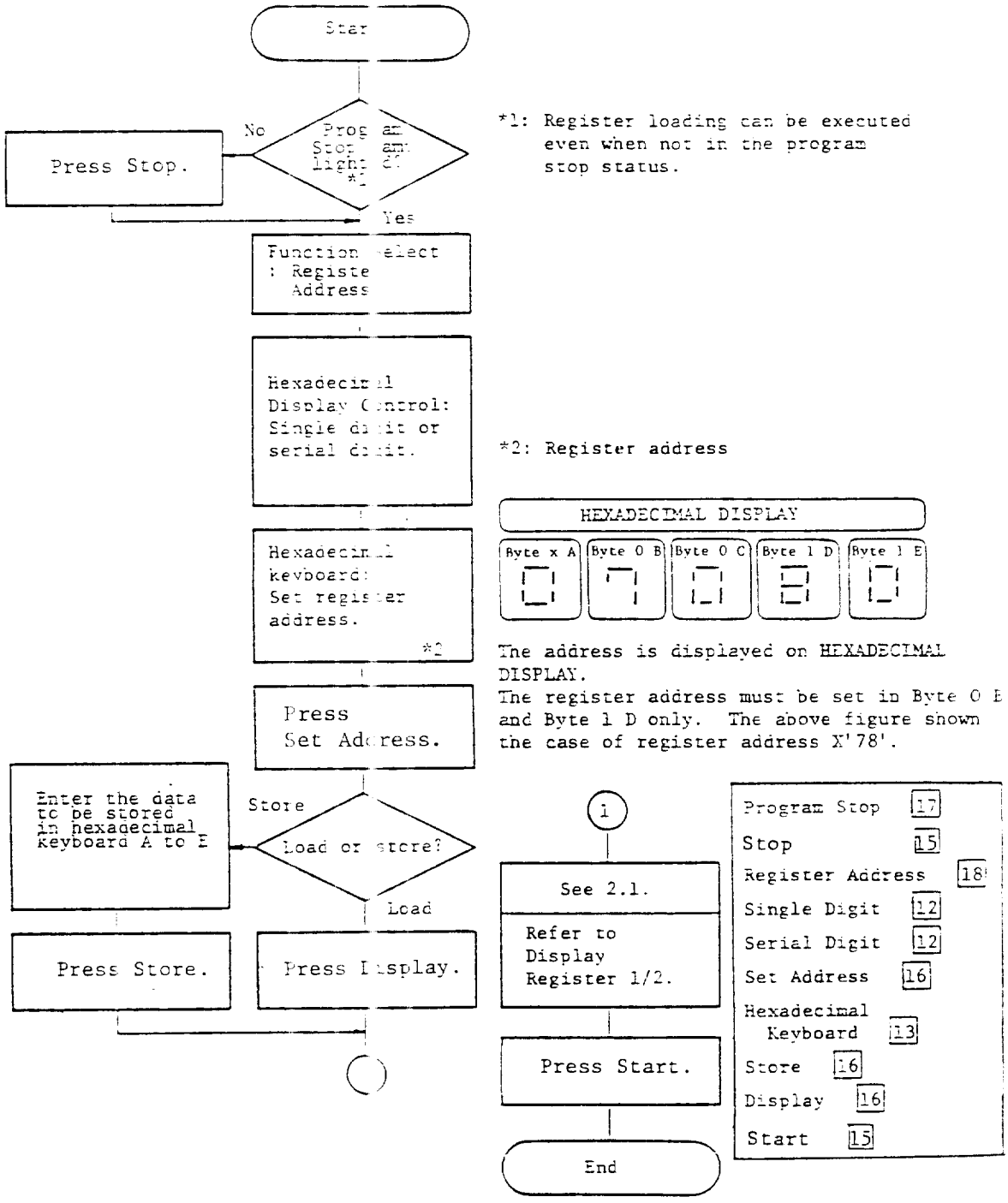


Fig. 2.5 Register load/store procedure

The operation shown in Fig. 2.6 is required for program stop or program interrupt by the execution address of any instruction address or load instructions (IC, ICT, L, LH) in the program.

The program is stopped or interrupted immediately after execution of the compare address instruction.

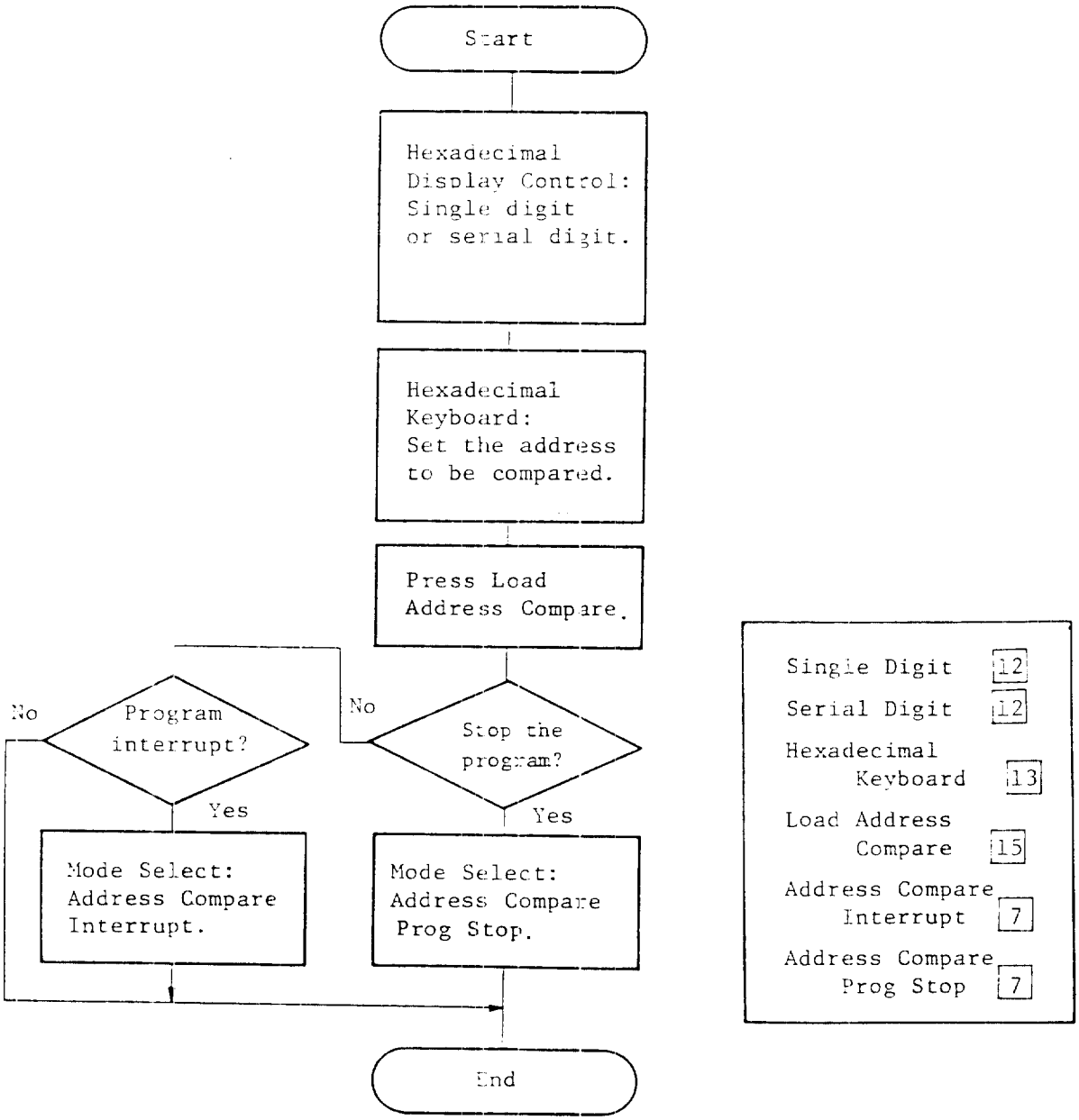


Fig. 2.6 Load address compare procedure

2.7 STORE ADDRESS COMPARE PROCEDURE

The operation shown in Fig. 2.7 is necessary for program stop or program interrupt by the execution address of the store instruction (STC, STCT, ST, STH) in the program.

The program is stopped or interrupted immediately after execution of the compare address instruction.

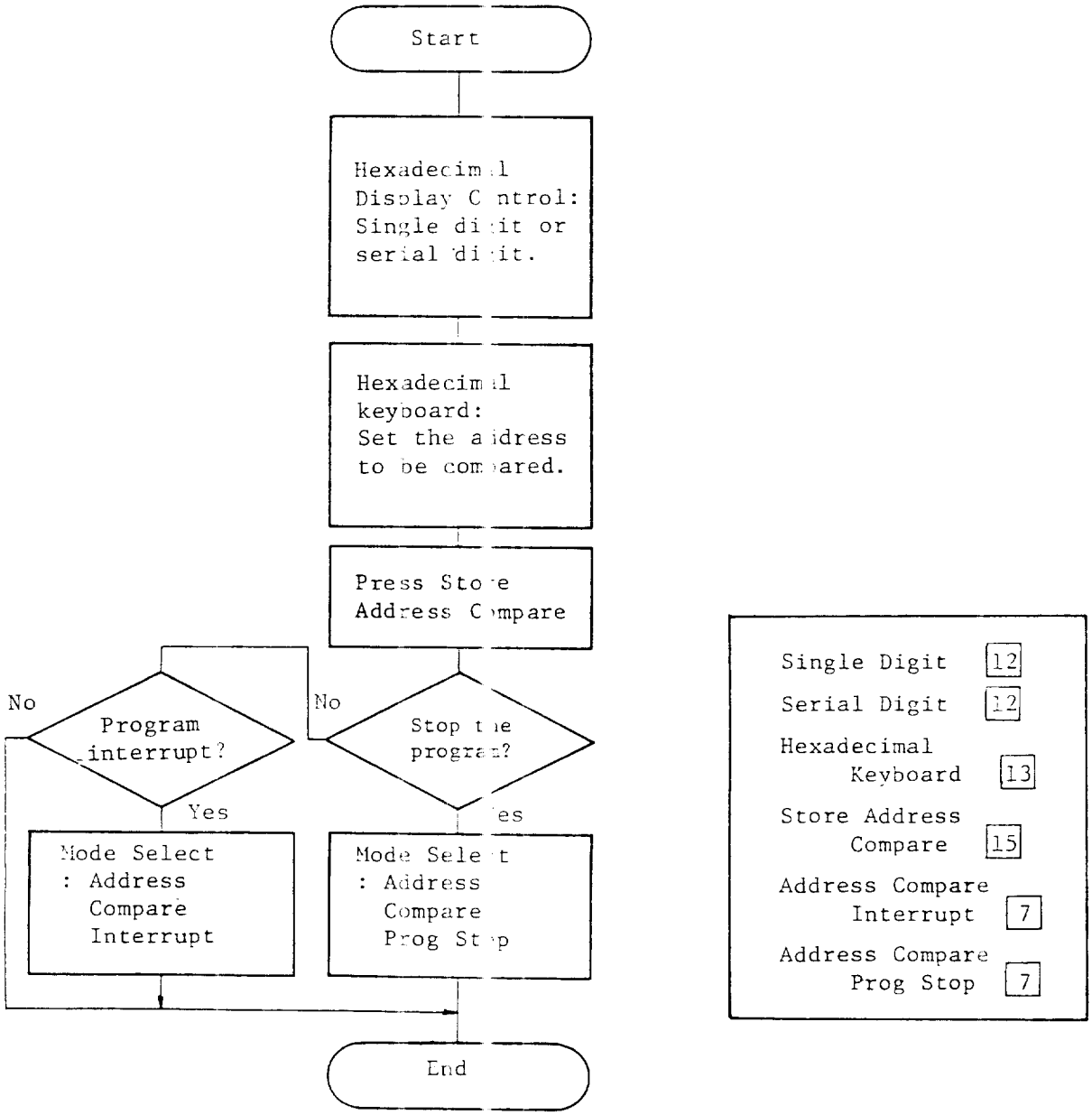


Fig. 2.7 Store address compare procedure

2.8 STORAGE SINGLE READ PROCEDURE

The operation shown in Fig. 2.8 is required for continuously reading to arbitrary address of the storage.

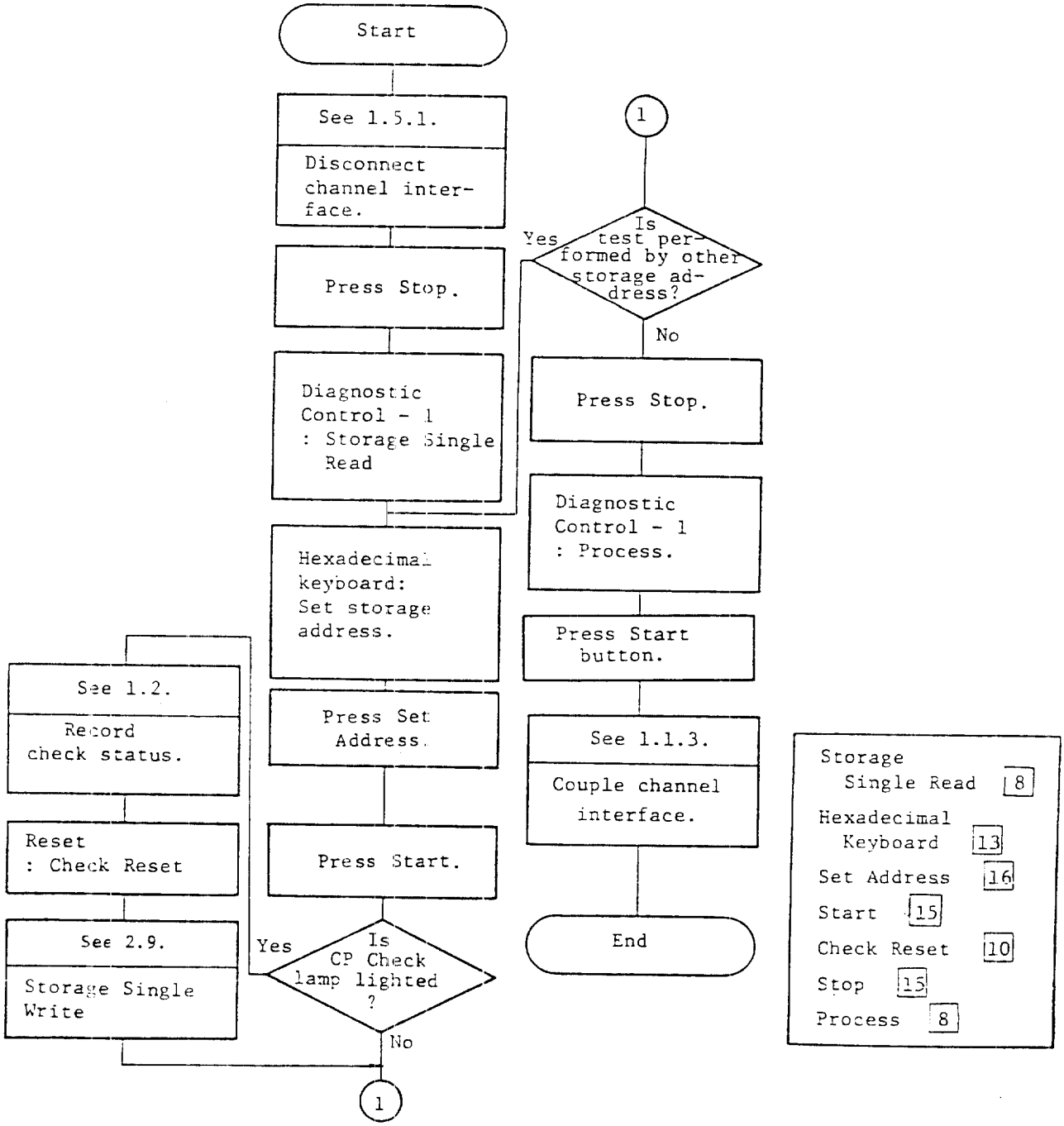


Fig. 2.8 Storage single read procedure

2.9 STORAGE SINGLE WRITE PROCEDURE

The operation shown in Fig. 2.9 is required for continuously writing into arbitrary address of the storage.

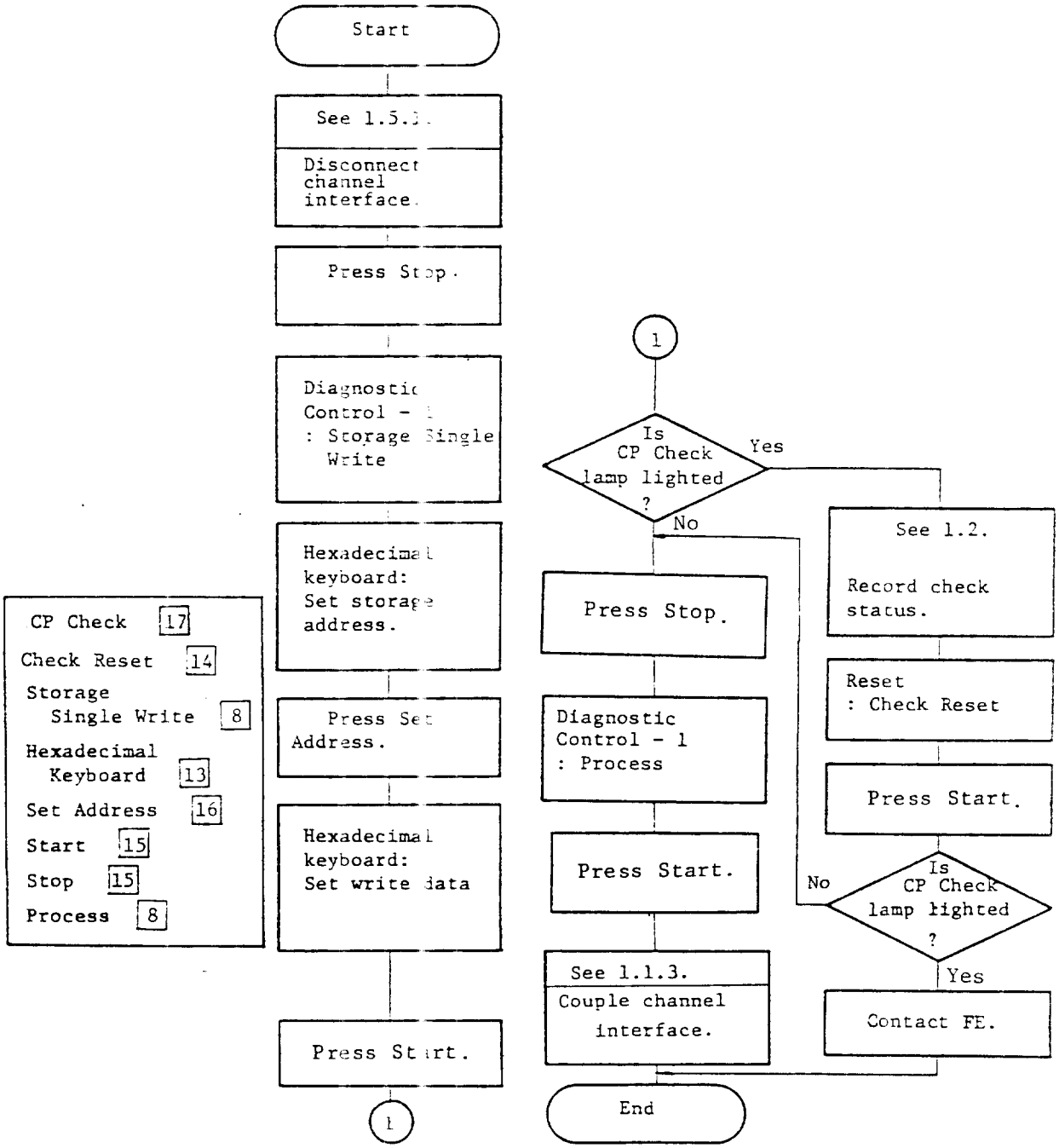


Fig. 2.9 Storage single write procedure

The operation shown in Fig. 2.10 is required for continuously reading all addresses of the storage.

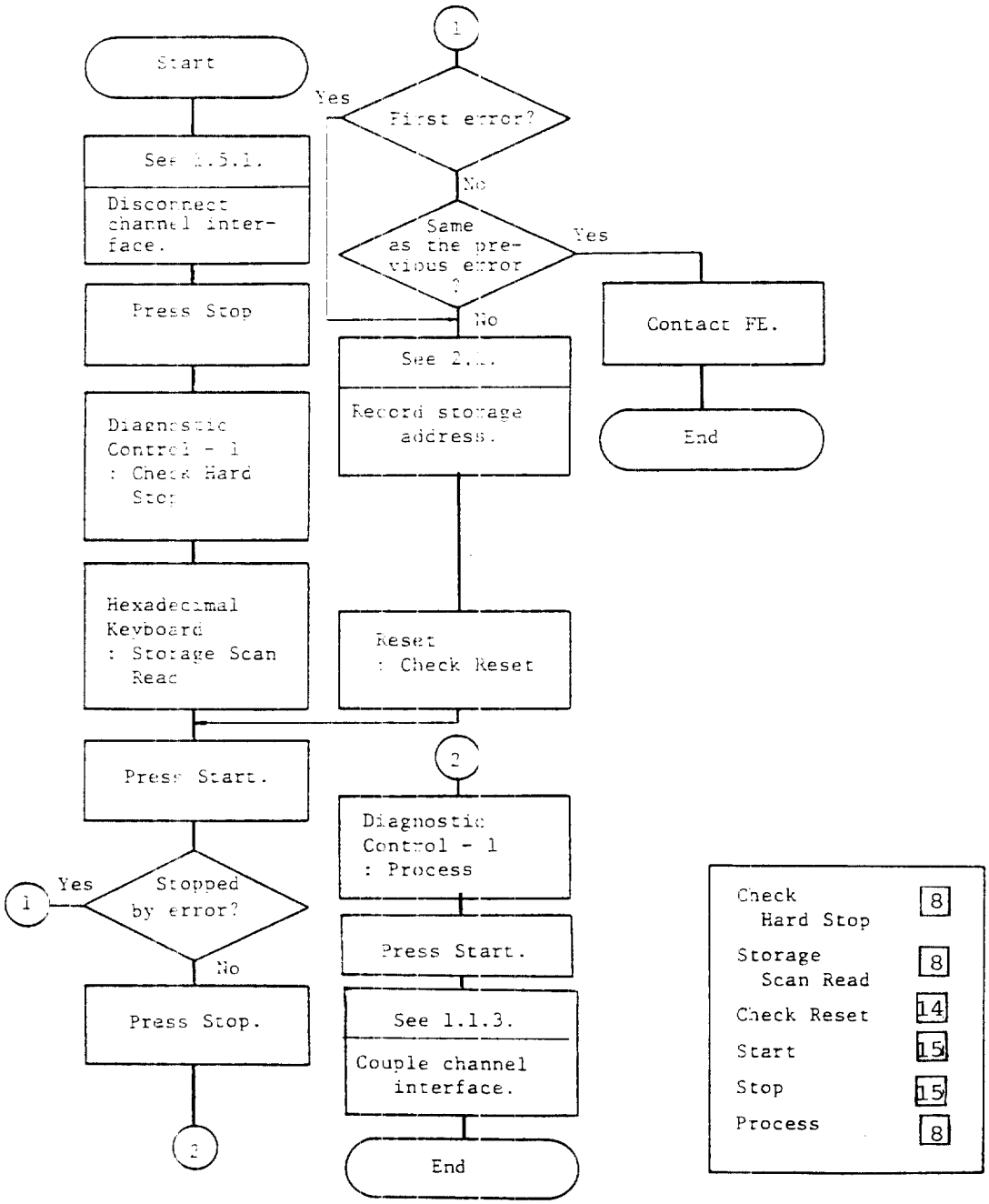


Fig. 2.10 Storage scan read procedure

2.11 STORAGE SCAN WRITE PROCEDURE

The operation shown in Fig. 2.11 is required for continously writing into all addresses of the storage.

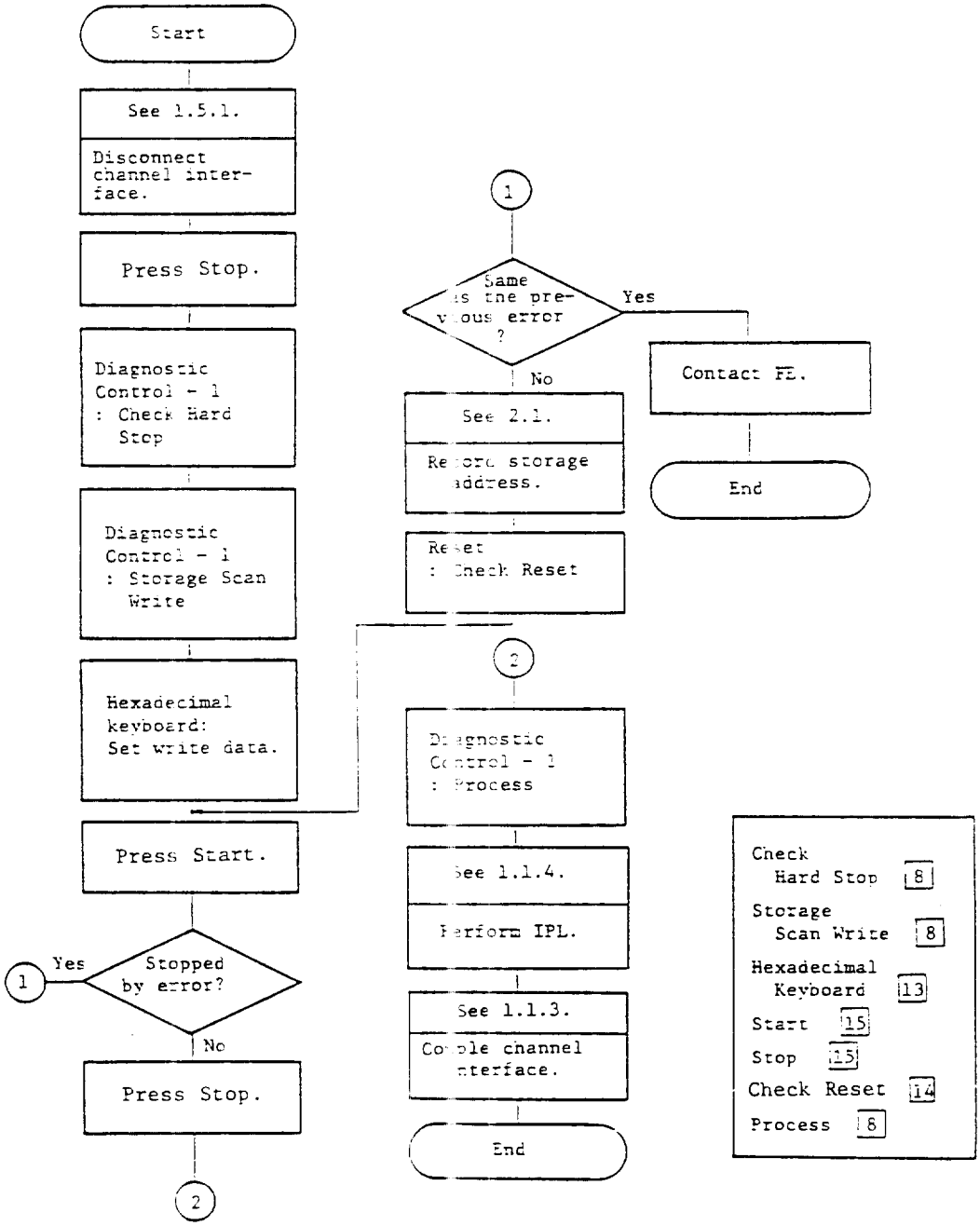


Fig. 2.11 Storage scan write procedure

2.12 ICW SINGLE READ/WRITE PROCEDURE

The operation of Fig. 2.12 is required for performing read/write to an arbitrary address of CS2-ICW (Interface Control Word).

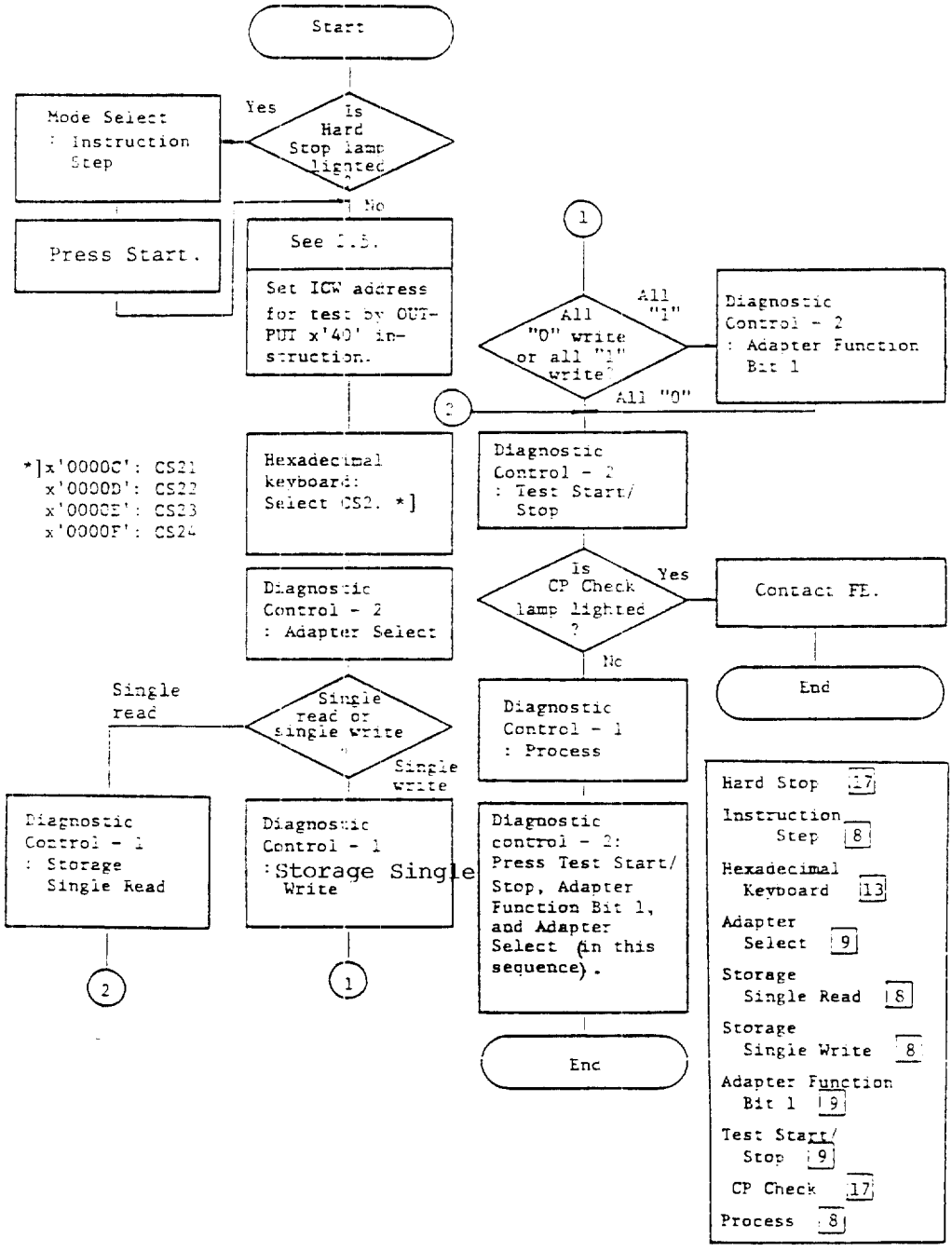


Fig. 2.12 ICW single read/write procedure

2.13 ICW SCAN READ/WRITE PROCEDURE

The operation shown in Fig. 2.13 is required for performing read/write to all adddresses of an arbitrary device number of CS2-ICW.

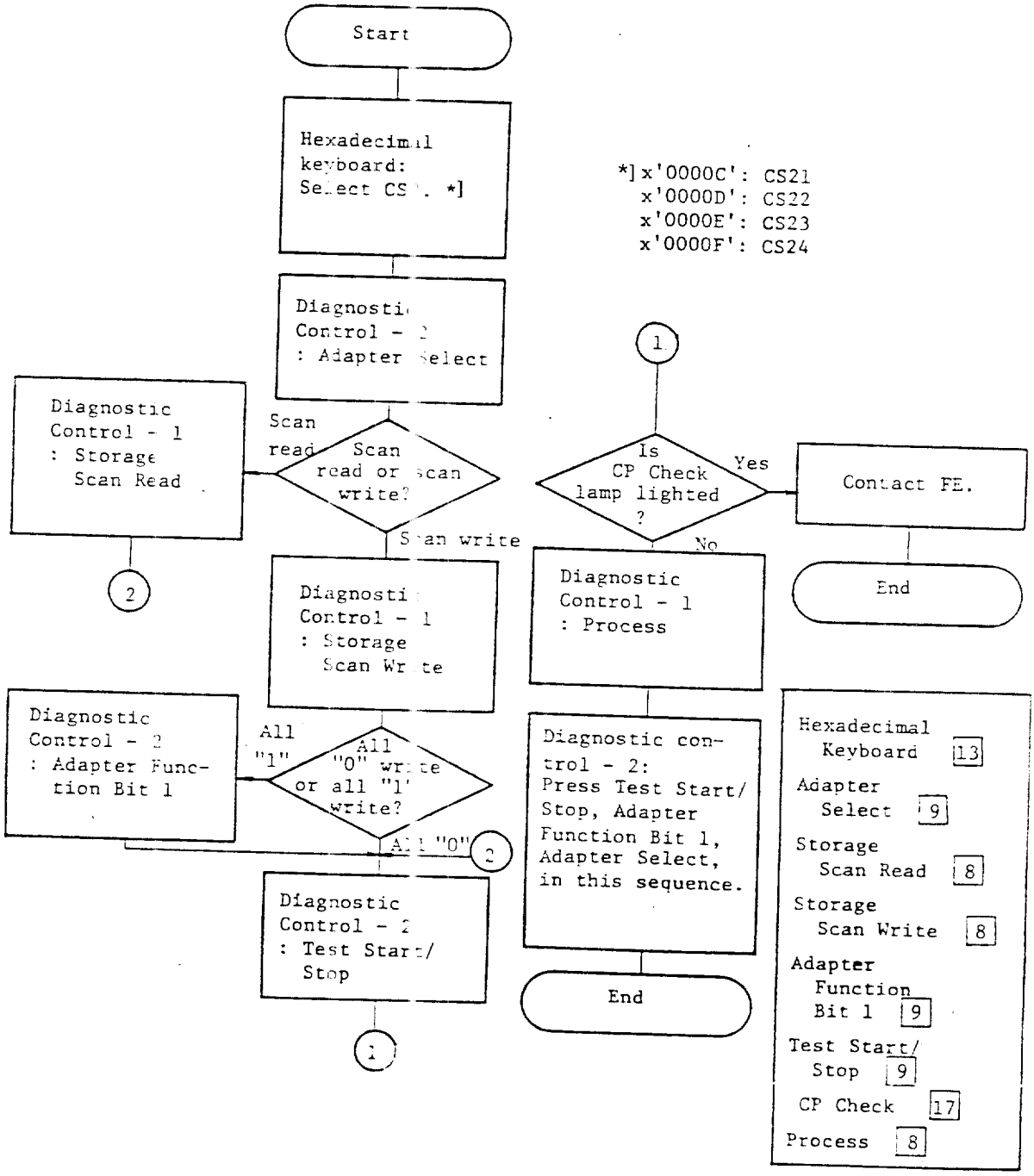


Fig. 2.13 ICW scan read/write procedure

2.14 CS2 (COMMUNICATION SCANNER 2)-1 TIMING CLOCK STOP PROCEDURE

The operation shown in Fig. 2.14 is required for providing clock stop at each write timing (T9) of the scan cycle of CS2.

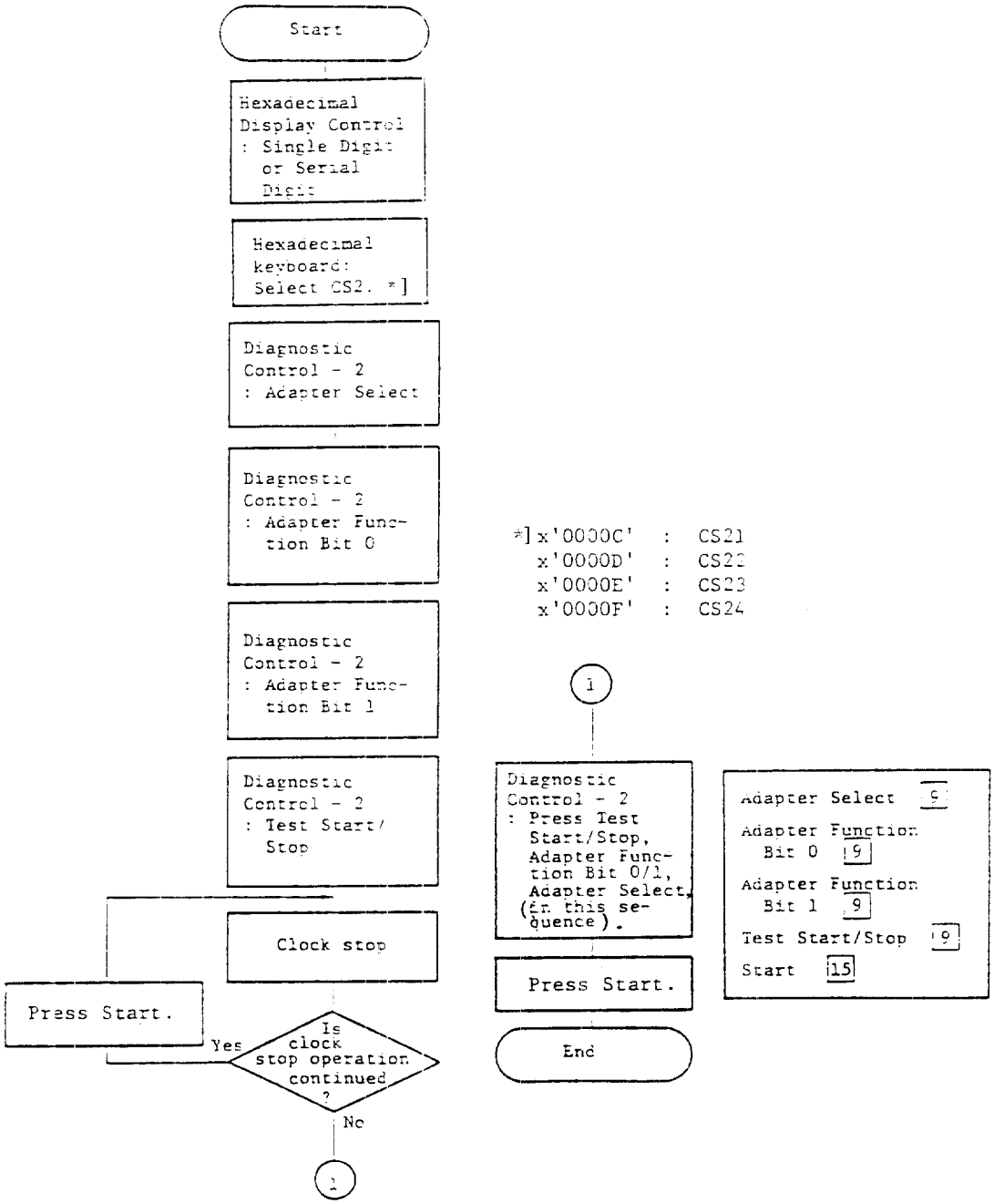


Fig. 2.14 CS2-1 timing clock stop procedure

The operation shown in Fig. 2.15 is required for providing clock stop (stop at write timing T9) at each scan period of the line address specified by OUTPUT X'40' instruction.

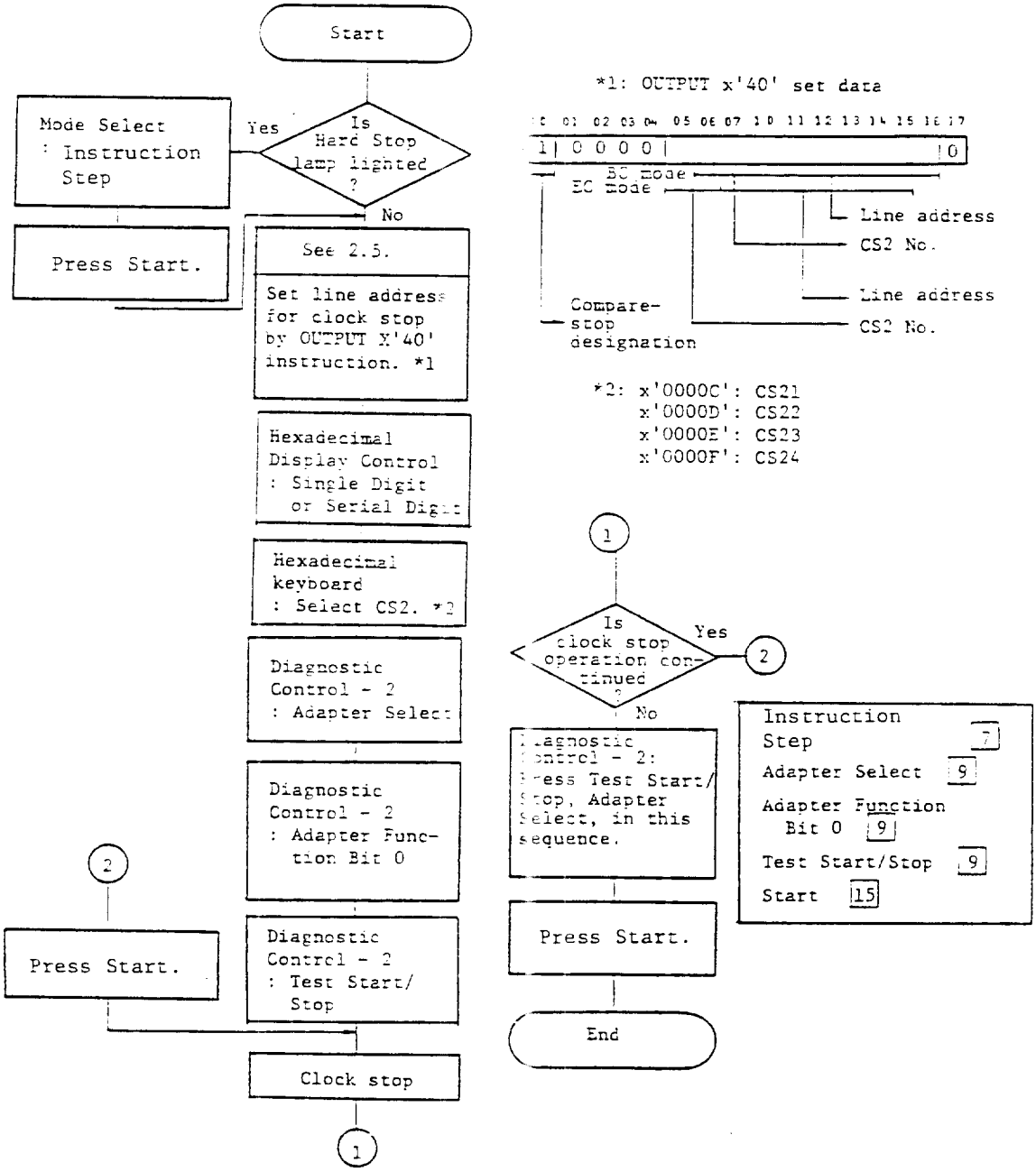


Fig. 2.15 CS2-1 scan clock stop procedure

2.16 COMPARE DISPLAY PROCEDURE

The operation shown in Fig. 2.16 is required for recording and displaying the logging data when coincidence is attained in the compare circuit set on the back panel.

It is also possible to cause clock stop at coincidence.

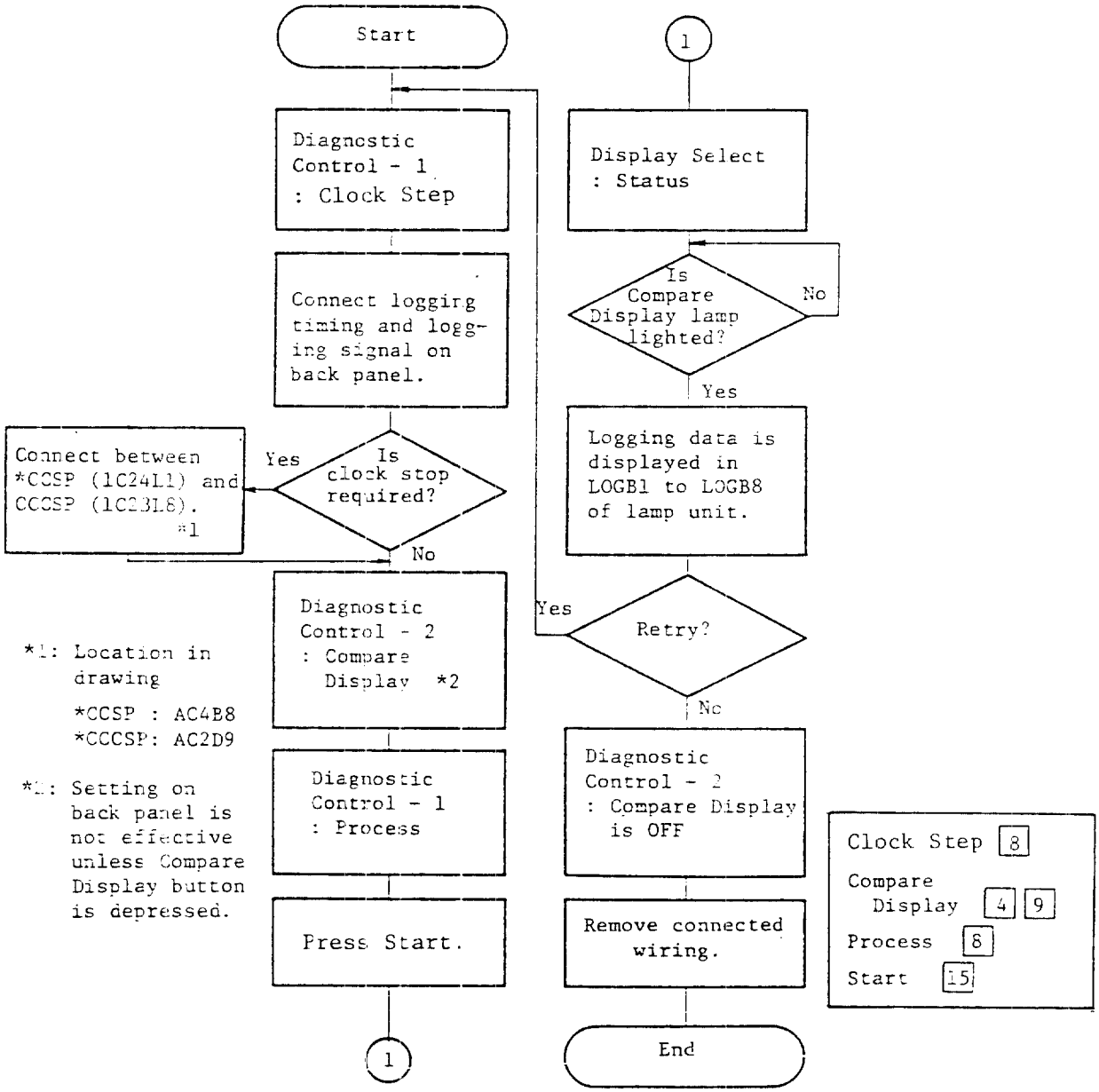


Fig. 2.16 Compare display procedure

2.17 PROGRAM TRACE PROCEDURE

The operation shown in Fig. 2. 7 is required for generating a level 1 interrupt after execution of each instruction during execution of program levels 2 to 5.

This function is not executed unless the Set Test Mode (byte 1, bit 2) is performed by OUTPUT X'79'.

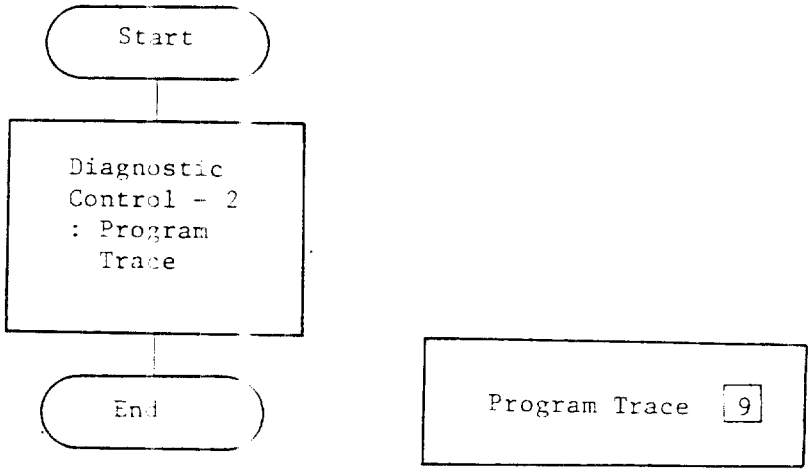
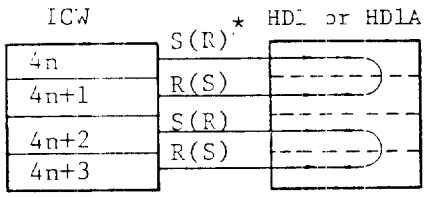


Fig. 2.17 Program trace procedure

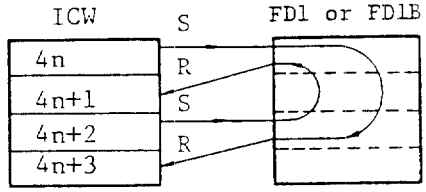
2.18 LINE UNIT (LUT) LOOP PROCEDURE

This operation is used when performing loop test in the line set (LS) by the test program, etc. Figure 2.18 shows the relation between the Interface Control Word (ICW) and LS, and the operating procedure.

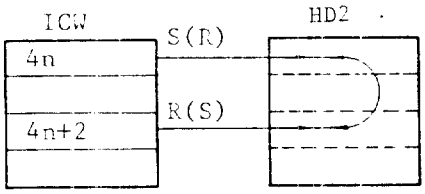
(1) For HD1 or HD1A



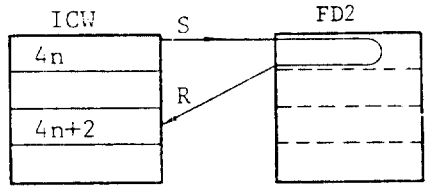
(2) For FD1 or FD1B



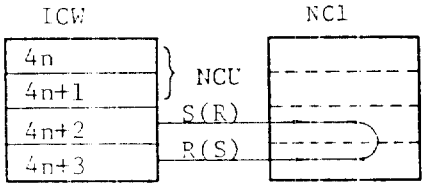
(3) For HD2



(4) For FD2

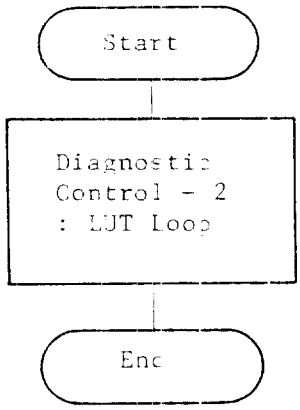


(5) For NC1



* S: Send
R: Receive

(Note)
The LA1 equivalent to (1) or (2).
(depend on setting board in the LA1)



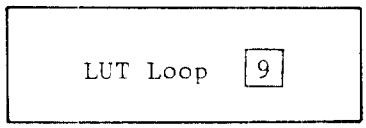


Fig. 2.18 LUT loop procedure

CHAPTER 3

PROBLEM-SOLVING PROCEDURES

This chapter describes the procedures to be performed by the operator when a problem occurs in the CP. If any problem occurs, the operator should first make sure that the switches on the operator panel are all in the specified positions. After confirming this, he can determine the cause of the problem by following the procedure described in this manual, and retry execution. If the system recovers by this retry operation, the service can be continued.

It is desirable to notify the FE of the problem cause and the results of retry.

3.1 CHECK LAMP PROCESSING PROCEDURE

This section describes the cause of CHECK lamp lighting on the operator panel and the processing procedure to be taken by the operator.

3.1.1 Causes of CHECK Lamp ON

The possible causes of the CHECK lamp lighting are as follows:

CP POWER CHECK lamp [1]

- Failure occurred in a power unit of CP
- Abnormal temperature rise in CP
- Cooling fan of CP failed

CP CHECK lamp [17]

This lamp lights upon occurrence of machine check, program check, adapter check and 1 bit check (only when operating storage single read/write and scan read/write functions) in CP.

For detailed information, refer to paragraph 4.1.4, "Status".

3.1.2 Processing Procedure

The processing when the CHECK lamp comes on should follow the procedure shown in Fig. 3.1.

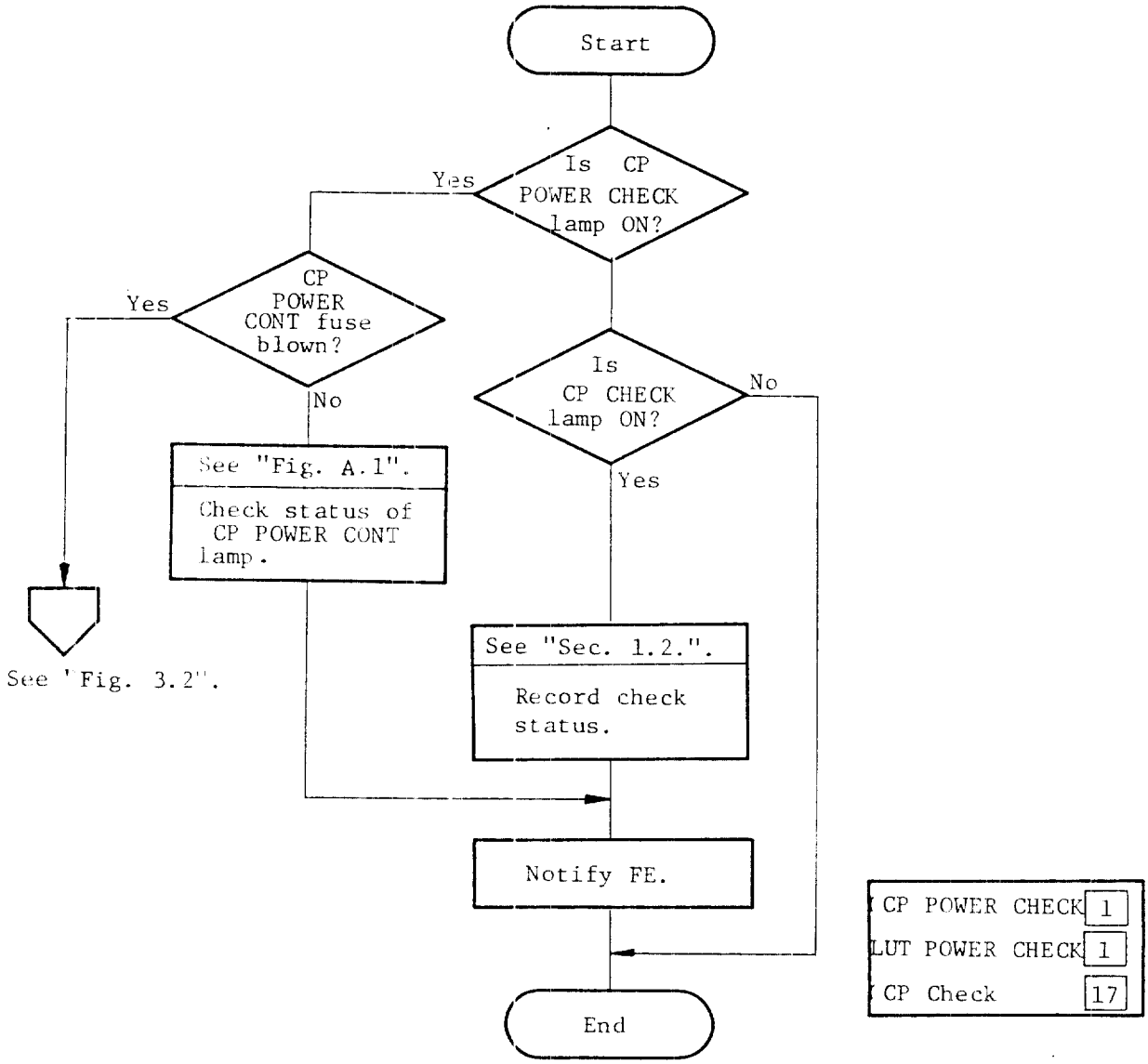


Fig. 3.1 CHECK lamp processing procedure

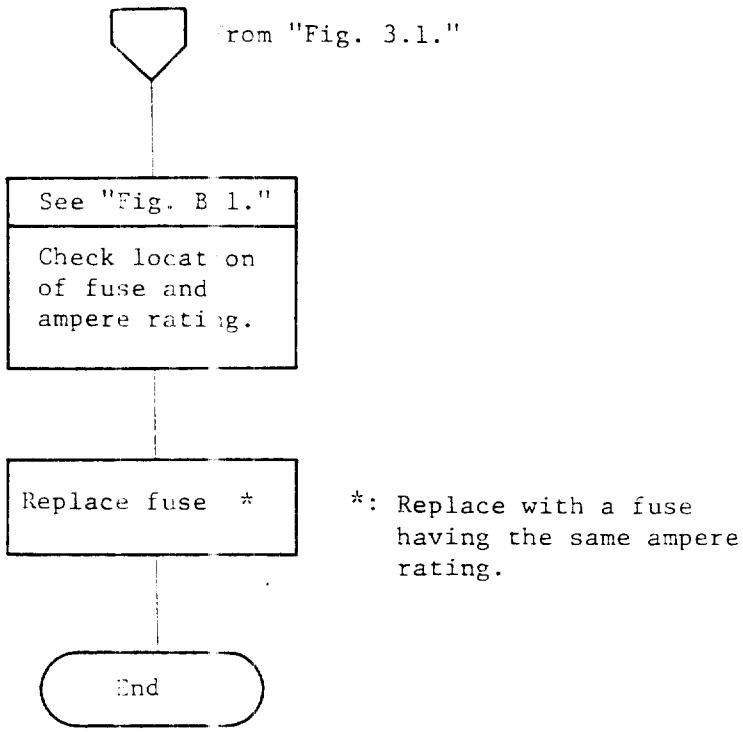


Fig. 3.2 Fuse replacement procedure

3.2 HARD STOP LAMP PROCESSING PROCEDURE

This section describes the caus s of lighting of the HARD STOP lamp [17] on the operator panel and the appr priate processing procedure.

3.2.1 Causes of HARD STOP Lam ON

The possible causes of HARD STO lamp lighting are as follows:

- Occurrence of machine check i CP (in case of Check Hard Stop mode only)
- When the control program dete ts a software error or hardware error

3.2.2 Processing Procedure

The processing to be performed when the HARD STOP lamp comes on should follow the procedure shown in Fig. 3.3

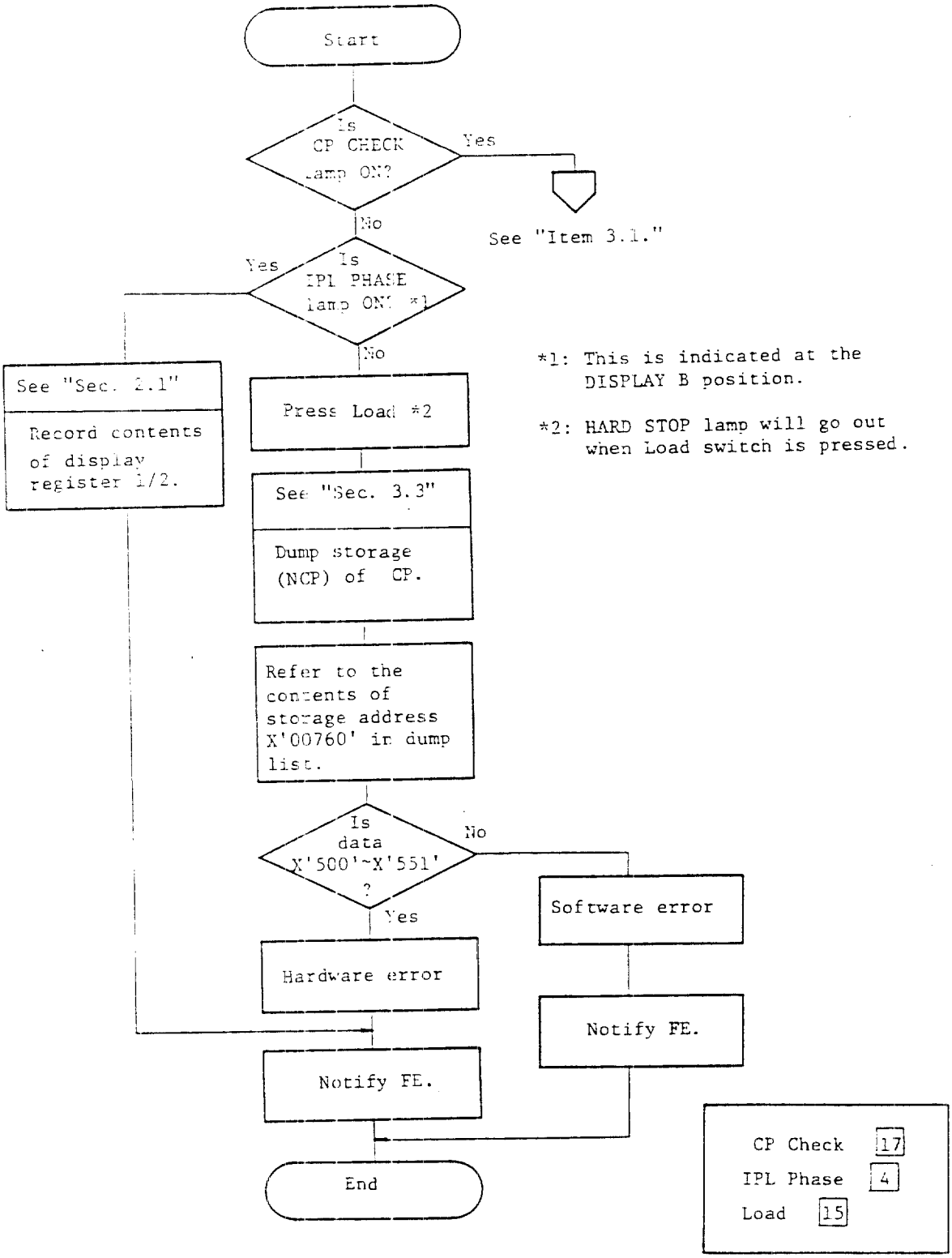


Fig. 3.3 HARD STOP lamp processing procedure

3.3 STORAGE DUMP UTILITY FOR NCP

The dump utility program is output in hexadecimal format in the data set for which the communication control processor storage is specified.

This dump list provides information on erroneous hardware operation and the address trace information.

The dump utility program consists of two sections: one section is executed by the host processor, and the other section by the communication control processor, At first, all the storage contents of the communication control processor are stored in the data set of the host processor, and the necessary area is listed in the required format according to the utility control statement. If required, the mnemonic code can be obtained by using this program.

Note that the area of hexadecimal 0000-01FF (when the number of CA is one) or hexadecimal 0000-03FF (when the number of CA is two), and the area of hexadecimal 0400-04FF for the dump utility program have been damaged.

Note that dumping the 4705 will terminate the execution of any control program running in the 4705. All host software utilizing the 4705 CP should be quiesced or cancelled. Also note that some access methods (such as VTAM, and TCAM) can dump the 4705 under operator control.

Refer to the appropriate utility reference manuals for the Job Control Statements required to perform a standalone dump or format of the 4705 Control Program.

CHAPTER 4

DESCRIPTION OF CP OPERATOR PANEL

This chapter describes the function of the various lamps, buttons and switches provided on the CP operator panel.

4.1 LAMPS

A number of lamps are used on the CP operator panel, and a lamp is fitted to each switch. In this section, the lamps not part of a switch assembly are described. The means by which each lamp is lighted are described below.

4.1.1 Rack Top Lamp [1]

This lamp indicates the power ON status of CP and their check status.

CP READY LAMP [1]

This lamp turns on when CP is ready for operation after turning power ON.

CP POWER CHECK lamp [1]

The possible causes by which this lamp turns ON are as follows:

- Trouble in a power unit of CP
- Abnormal temperature rise in CP
- Trouble in the cooling fan of CP

4.1.2 LUT RESERVED Lamp [2]

This lamp displays the connection status of CS and LUT.

LUT 1 lamp [2]

This lamp turns ON when CS No.1 and LUT are connected.

LUT 2 lamp [2]

This lamp turns ON when CS No.2 and LUT are connected.

LUT 3 lamp [2]

This lamp turns ON when Cs No.3 and LUT are connected.

LUT 4 lamp [2]

This lamp turns ON when CS No.4 and LUT are connected.

4.1.3 CHANNEL INTERFACE ENABLED Lamp [2]

This lamp displays the connection status of CA and the HOST CPU channel.

CH1 1A lamp [2]

This lamp turns ON when the A-side channel of CA No.1 is connected.

CH2 2A lamp [2]

This lamp turns ON when the B-side channel of CA No.1 is connected.

CH2 2A lamp [2]

This lamp turns ON when the A-side channel of CA No.2 is connected.

CH2 2B lamp [2]

This lamp turns ON when the B-side channel of CA No.2 is connected.

CH3 3A lamp [2]

This lamp turns ON when the A-sice channel of CA No.3 is connected.

CH3 3B lamp [2]

This lamp turns ON when the B-side channel of CA No.3 is connected.

CH4 4A lamp [2]

This lamp turns ON when the A-side channel of CA No.4 is connected.

CH4 4B lamp [2]

This lamp turns ON when the B-side channel of CA No.4 is connected.

4.1.4 DISPLAY A Lamp [3]

These lamps provide different display contents according to the status of the Display Select switch [11] ; check status, IAR, or contents of display register 1 are displayed.

If the Display A to Hex switch [13] of the Hexadecimal Display Control switch [12] is pressed, the contents of the DISPLAY lamp [3] are displayed in hexadecimal on the HEXADECIMAL DISPLAY lamp [10] .

The display of the DISPLAY A lamp [3] at each position of the Display Select switch [11] is described below:

Status [11]

When the Display Select switch is set in this position, the check status at machine check is displayed. Each check status corresponds to the "Adapter"-"Level 1 Program" stamped on the DISPLAY A lamp [3] , and the cause of lighting of each check status lamp is as follows:

Adapter lamp [3]

When program level 1 interrupt due to hardware error has occurred from various adapter (AE, CA3, CS2, etc.).

In/Out lamp [3]

- When I/O instruction is executed on program level 5
- When parity error has occurred in the In Bus during execution of an input instruction
- When an undefined I/O instruction is executed.

Address Exception lamp [3]

When the program has accessed an address exceeding the mounted storage capacity.

Protect lamp [3]

When the storage protection area is accessed by program level 5.

Invalid OP lamp [3]

When the program tries to execute an undefined instruction.

Byte X lamp [3]

When parity error occurs in the following Byte X.

- SAR (Storage Address Register)
- ALU (Arithmetic Logic Unit)
- LA Bus
- LB Bus
- In Bus

Byte 0 lamp [3]

When parity error occurs in byte 0 of Instruction Register (IR) and "item Byte X lamp [3] ".

Byte 1 lamp [3]

When parity error occurs in byte 1 of IR and "item Byte X lamp 3 ".

In Data lamp [3]

When parity error occurs in either of the following:

- LA Bus
- LB Bus
- In Bus

SAR lamp [3]

When parity error occurs in the storage address register

SD lamp [3]

When the following error occurs.

- 2BCK (2 Bit Check)
- MCCK (Main Storage Control Check)
- RFCK (Refresh Check)
- WDCK (Write Data Check)

IR lamp [3]

When parity error occurs in the instruction register.

Clock lamp [3]

When an abnormal status occurs in the clock pulse, cycle counter or Attachment Base (AB) timing.

Level 1 Program lamp [3]

When program check occurs during processing of program level 1.

IAR and IR [11]

When set to this position, the contents of IAR (instruction address to be executed next) are displayed on the DISPLAY A lamp [3] .

Display Register 1 and 2 [11]

When set in this position, the contents of display register 1 are displayed on the DISPLAY A lamp [3] .

The following data are set into the display register 1.

- The data at the time of execution of output instruction X'71'
- Storage address at execution of storage load/store
- Storage address at execution of storage single read/write
- Storage address at storage scan read/write
- Register address at execution of register load/store
- Storage address at IPL phase 1/2

4.1.5 DISPLAY B Lamp [4]

These lamps provide different display contents according to the status of the Display Select switch [11] ; program level, IR, or contents of display register 2 is displayed.

If the Display B to Hex switch [12] of the Hexadecimal Display Control switch [12] is pressed, the displayed contents of the DISPLAY B lamp [4] can be displayed in hexadecimal on the HEXADECIMAL DISPLAY lamp [10] .

The display of the DISPLAY B lamp [4] at each position of the Display Select switch [11] is described below:

Status [11]

When the Display Select switch is set in this position, the status of the IPL phase and program level is displayed on the Display B lamp [4] . Each status corresponds to the "Compare Display" to "Active Level Z" stamped on the DISPLAY B lamp [4] , and the cause of lighting of each lamp is as follows:

Compare Display lamp [4]

When the Compare Display switch [9] is effective and the coincidence condition (that is provided setting on the back panel) occurs.

Address Compare lamp [4]

When the storage address at execution of program and the storage address specified by the Hexadecimal Keyboard switch coincide. [13] when the load address compare and store address compare operations have been performed.

IPL Phase 0, 1 lamp [4]

This lamp indicates the program loading status, and IPL phases 1,2 and 3 are displayed on two lamps. Table 4.1 shows the relation between lamps and phases.

Table 4-1 Relation between IPL phase lamps 0 and 1, and IPL phases

IPL phase	IPL phase lamps	
	0	1
1	0	1
2	1	0
3	1	1

Note: 0 : Lamp OFF
1 : Lamp ON

These lamps will turn off when Reset IPL L1 and Not Initialized Bit (byte 0, bit 0) is executed by output instruction X'77'.

Bid Level 1 lamp [4]

This lamp turns on if:

- Hardware error occurs in a CP, CA or CS.
- Program check occurs.
- IPL Phase lamp [4] is ON.
- The storage address at program execution coincides with the storage address specified by the Hexadecimal Keyboard switch [13] when performing the load address/store address compare interrupt operations.
- A single instruction is executed at program levels 2 to 5 when the Program Trace switch [9] is active.
- 1 bit error occurs in the storage data.

Bid Level 2 lamp [4]

This lamp turns on if:

- A level 2 request is made from CS.
- Set Diagnostic L2 (byte 0, bit 6) is performed by output instruction X'77'.

Bid Level 3 lamp [4]

This lamp turns on if:

- Level 3 request is made from CA.
- Level 3 request is made from Flexible Disk Controller (FDC).
- Set Program Call Interrupt L3 is executed by output instruction X'7C'.
- Interrupt from 100ms timer occurs.
- Interrupt switch [15] is pressed.
- Auto Network Shutdown (ANS) L3 request is made.

Bid Level 4 lamp [4]

This lamp turns on if:

- Set Program Call Interrupt L3 is performed by output instruction X'7D'.
- Superviser Call L4 request is made.

Entered Interrupt Level 1 to 4 lamp [4]

This lamp displays the status of the current program level and the previous program level.

When the EXIT instruction is executed, the lamp corresponding to the current program level goes out.

Mask Level ECC 1 lamp [4]

This lamp turns on if:

- Reset switch [14] is pressed.
- Load switch [15] is pressed.

• Set Mask Bit [1 Bit Error Corrected L1 (byte 1, bit 0)] is executed by output instruction X'7E'.

And this lamp goes out when the Reset Mask Bit [1 Bit Error Corrected L1 (byte 1, bit 0)] is executed by output instruction X'7E'.

Mask Level ADP 1 to 5 lamp [4]

This lamp turns on if:

• Reset switch [14] is pressed
• Load switch [15] is pressed
• Set Mask Bit [Adapter Requests L1-Program L5 (byte 1, bit 1-bit 5)] is executed by output instruction X'7E'.

And this lamp goes out when the Reset Mask Bit [Adapter Requests L1-Program L5 (byte 1, bit 1-bit 5)] is executed by output instruction X'7F'.

Active level C, Z lamp [4]

This lamp displays the status of the C and Z latches at the current program level.

IAR and IR [11]

When set to this position, the contents of the instruction register (IR) are displayed on the DISPLAY B lamp [4].

Display Registers 1 and 2 [11]

When set to this position, the contents of display register 2 are displayed on the DISPLAY B lamp [4].

The following data is set in the display register 2.

• Data at the time of execution of output instruction X'72'
• Storage data at execution of storage load/store
• Storage data at execution of storage single read/write
• Storage data at execution of storage scan read/write
• Register data at execution of register load/store
• Storage data at IPL phase 2

4.1.6 HEXADECIMAL DISPLAY Lamp [10]

These lamps provide different display contents according to the position of the Hexadecimal Display Control switch [12]. The display on the HEXADECIMAL DISPLAY lamps [10] at each position of the Hexadecimal Display Control switch [12] is described below:

Single Digit [12]

When set to this position, the data set by the Hexadecimal Keyboard switch [13] is displayed in hexadecimal.

Serial Digit [12]

When set to this position, the data to be set by the Hexadecimal Keyboard switch [13] is displayed in hexadecimal, and are shifted from right to left at each setting.

Display A to Hex [12]

When set to this position, the contents of the DISPLAY A lamp [3] are displayed in hexadecimal.

Display B to Hex [12]

When set to this position, the contents of the DISPLAY B lamp [4] are displayed in hexadecimal.

4.1.7 Local Power Lamp [5]

This lamp turns on when the power controller switch of CP is set at Local.

4.1.8 Remote Power Lamp [5]

This lamp turns on when the power controller switch of CP is set at Remote.

4.1.9 LUT Local Power Lamp [5]

This lamp turns on when the power controller switch of CP is set at Local.

4.1.10 LUT Remote Power Lamp [5]

This lamp turns on when the power controller switch of CP is set at Remote.

4.1.11 CP Check Lamp [17]

This lamp turns on when the machine check, program check, adapter check, or 1-bit check (only when performing storage single read/write and scan read/write) occurs.

The cause is displayed on the DISPLAY A lamp [3] (Refer to 4.1.4, "Status".)

4.1.12 Program Display Lamp [17]

This lamp turns on when Output X'71' (display register 1) and Output X'72' (display register 2) are executed, and goes out when the Start switch [15] is pressed.

4.1.13 Wait Lamp [17]

This lamp turns on when the program is in the execution wait statuses listed below:

- When IPL phase is 1 or 2,
- When the Entered Interrupt Level is OFF and Mask Level 5 is ON.

4.1.14 Program Stop Lamp [17]

This lamp lights when the program stop status or hard stop status is entered by the causes listed below:

- When the Stop switch [15] is pressed.
- When the Instruction Step switch [7] is pressed.
- When the load address compare stop status is created (Refer to 4.2.5, when Load Address Compare switch [5] is ON.)
- When the store address compare stop status is entered (Refer to 4.2.5, when Store Address Compare switch [15] is ON.)
- When the hard stop status is entered (Refer to 4.1.15.)

4.1.15 Hard Stop Lamp [7]

This lamp lights when the CP is placed in the hard stop status by one of the causes listed below.

- When the Reset switch [14] is pressed.
- Hard stop is executed by Output X'70'.
- When machine check occurs in CC and the Check Hard Stop switch [8] is effective.
- When machine check occurs in CC, in the check stop mode, but not in the bypass CC check stop mode.

4.1.16 Test Lamp [17]

This lamp lights when the CP is placed in the test mode status by one of the causes listed below:

- When IPL Phase 0, 1 lamp [4] turns on.
- Set Test Mode (byte 1, bit 2) is executed by Output X'79'.
- Mode Select switch [7] is set at a position other than Process.
- Diagnostic Control-1 switch [8] is set at a position other than Process.

4.2 SWITCHES

The control panel of the CP uses pressure sensitive matrix switches (except the POWER ON/OFF switches), which are actuated easily at the touch of a finger.

When a switch is pressed, a lamp turns on or goes out with a "Beep" sound. The switch is active when the lamp is on, and inactive when off. The function of each switch will be described below.

4.2.1 POWER ON Button [1]

The CP and LUT power can be turned on by pressing this button when the power controller switch of CP is set at the Local position.

The lamp in this button turns on when the power is connected.

4.2.2 POWER OFF Button [1]

The power of CP can be cut off by pressing this button when the Local Power lamp [3] is on. If this button is pressed when the POWER Check lamp [1] is on, the POWER Check lamp [1] will go out.

4.2.3 Channel Interface Switch [5]

This switch is used to specify the connection route between CP and the HOST CPU channel.

External switch [5]

When set at this position, the connection route between CP and the HOST CPU channel can be specified from the supervisory unit.

Internal switch [5]

When set at this position, the connection route between the CP and the HOST CPU channel can be specified by using the 1A Enable/Disable-4B Enable/Disable switch [5] on the control panel

1A Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the A-side channel of the CA No.1 unit.

1B Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the B-side channel of the CA No.1 unit.

2A Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the A-side channel of the CA No.2 unit.

2B Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the B-side channel of the CA No.2 unit.

3A Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the A-side channel of the CA No.3 unit.

3B Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the B-side channel of the CA No.3 unit.

4A Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the A-side channel of the CA No.4 unit.

4B Enable/Disable switch [5]

This switch is used to specify connection/disconnection of the B-side channel of the CA No.4 unit.

4.2.4 IPL Select Switch [6]

This switch is used to specify the machine number of FDD or CA4 from which transfer of the initial program is to be made to the CP. CA select is only required when type-1 ROS is optioned.

FDD switch [6]

If Load switch [15] is pressed in this switch position, the initial program will be transferred from FDD.

CA 1 switch [6]

If Load switch [15] is pressed in this switch position, the initial program will be transferred from CA4, No. 1.

CA 2 switch [6]

If Load switch [15] is pressed in this switch position, the initial program will be transferred from CA4, No. 2.

CA 3 switch [6]

If Load switch [15] is pressed in this switch position, the initial program will be transferred from CA4, No. 3.

CA 4 switch [6]

If Load switch [15] is pressed in this switch position, the initial program will be transferred from CA4, No. 4.

4.2.5 Mode Select Switch [7]

This switch is used for selecting the operating mode of the CP.

Process switch [7]

This switch is used when the CP performs normal operations.

Instruction Step switch [7]

This switch is used when executing the instructions of a program one at a time. When this switch is pressed, the program is placed in the stop status, and one instruction is performed each time Start switch [15] is pressed.

Address Compare Prog Stop switch [7]

This switch is used together with the Load Address Compare switch [15] or Store Address Compare switch [5] for stopping the program when the conditions described below are satisfied.

When Load Address Compare switch [15] is on (active):

The program stops when the storage address specified by Hexadecimal Keyboard switch [13] coincides with the instruction address at execution of the program or the data address of load type instructions.

When Store Address Compare switch [15] is on (active):

The program stops when the storage address specified by Hexadecimal Keyboard switch [13] coincides with the data address of store type instructions at the execution of the program.

Address Compare Interrupt switch [7]

This switch is used together with the Load Address Compare switch [15] or Store Address Compare switch [5] for interrupting program level 1 when the conditions listed above are satisfied.

4.2.6 Diagnostic Control-1 Switch [8]

This switch is used for processing upon occurrence of a CP check and for performing read/write test to the storage.

Process switch [8]

This switch is used when not performing any test.

Bypass CC Check Stop switch [8]

This switch is used to prevent a hardware stop and does not start an IPL phase when a machine Check occurs in CC.

Check Hard Stop switch [8]

This switch is used to execute a hard stop when conditions that can cause the CP check lamp [17] to be lighted (refer to 4.1.11 "CP Check Lamp") have occurred.

Clock Step switch [8]

This switch is used to generate the control clock on a single clock basis. When this switch is pressed, the control clock is stopped, and one clock pulse is generated each time Start switch [15] is pressed.

The clock stop status is not released even if the Start switch [15] is turned OFF. The clock stop status can be released by pressing Start switch.

Storage Single Read switch [8]

This switch is used to continuously read the contents at any address of the storage or CS2-ICW. For the operating method, refer to 2.15.

Storage Single Write switch [8]

This switch is used to continuously write into any address of the storage or CS2-ICW. For the operating method, refer to 2.16.

Storage Scan Read switch [8]

This switch is used to continuously read the contents of all addresses of the storage or CS2-ICW. For the operating method, refer to 2.17 and 2.20.

Storage Scan Write switch [8]

This switch is used to continuously write the contents of all addresses of the storage or CS2-ICW. For the operating method, refer to 2.18 and 2.21.

4.2.7 Diagnostic Control-2 Switch [9]

This switch is used to test CP.

Adapter Select switch [9]

This switch is used to select the adapter to be tested, and the data specified by the Hexadecimal Keyboard switch [13] can be used as the adapter selecting address. This switch is only effective for CS.

Adapter Function Bit 0 switch [9]

This switch is used for testing the adapter (only CS).

Adapter Function Bit 1 switch [9]

This switch is used for testing the adapter (only CS).

Test Start/Stop switch [9]

This switch is used to specify start/end of the test of the adapter (only CS).

Compare Display switch [9]

This switch is used for troubleshooting, and is able to display the status of each signal on the lamp unit when coincidence is obtained in the compare circuit set on the back panel.

Program Trace switch [9]

This switch is used to generate a level 1 interrupt at the execution of each instruction when executing the program levels 2-5.

This function is effective when the Set Test Mode (byte 1, bit 2) is executed by Output X'79'.

LUT Offline switch [9]

This switch is used to logically separate LUT from CS.

LUT Loop switch [9]

This switch is used to issue a signal directing loop for all lines to LUT. By operating this switch, CP and communication lines are set in the all-line loop status in LS.

4.2.8 Display Select Switch [11]

This switch is used to select data to be displayed on the DISPLAY A lamp [3] and DISPLAY B lamp [4].

Status switch [11]

This switch is used to display the check status at the time of a CP check on the DISPLAY A lamp [3], and the program level on the DISPLAY B lamp [4].

IAR and IR switch [11]

This switch is used to display the contents of IAR on the DISPLAY A lamp [3] and the contents of IR on the DISPLAY B lamp [4].

Display Register 1 and 2 switch [11]

This switch is used to display the contents of display register 1 on the DISPLAY A lamp [3] and the contents of display register 2 on the DISPLAY B lamp [4].

4.2.9 Hexadecimal Display Control Switch [12]

This switch is used to select the data to be displayed by the HEXADECIMAL DISPLAY lamp [10] and to validate/invalidate operation of the Hexadecimal Keyboard switches [13] .

Single Digit switch [12]

When set to this position, operation of the Hexadecimal Keyboard switch [13] is validated, and the data set by the Hexadecimal Keyboard switch [13] is displayed by the HEXADECIMAL DISPLAY lamp [10] .

For the data setting method, refer to item 4.2.10, first paragraph.

Serial Digit switch [12]

When set to this position, operation of the Hexadecimal Keyboard switch [13] is validated, and the data set by the Hexadecimal Keyboard switch [13] is displayed on the HEXADECIMAL DISPLAY lamp [10] while being shifted from right to left.

For the data setting method, refer to item 4.2.10, second paragraph.

Display A to Hex switch [12]

When set to this position, the hexadecimal contents of the DISPLAY A register [3] are displayed on the HEXADECIMAL DISPLAY lamps [10] .

Display B to Hex switch [12]

When set to this position, the hexadecimal contents of the DISPLAY B register [4] are displayed on the HEXADECIMAL DISPLAY Lamp [10] .

4.2.10 Hexadecimal Keyboard Switches [13]

These switches are effective when the Single Digit switch [12] or Serial Digit switch [12] are ON, and the data setting method differs from the positions of the Single/Serial Digit switch.

When using the data set by the Hexadecimal Keyboard switches [13] as the storage address and register address, the Set Address switch [16] must be pressed.

Data setting method when Single Digit switch [12] is ON

Set any data by switches 0-F [13] of the Hexadecimal Keyboard switches [13], and select the corresponding byte by the Byte X A to Byte 1 E switch [13]. When Byte X A-Byte 1 E switch [13] is pressed, the data set by switches 0-F [13] is displayed by the HEXADECIMAL DISPLAY Lamp [10].

Data setting method when Serial Digit switch [12] is ON

Set any data by switches 0-F [13] of the Hexadecimal Keyboard switches [13].

The data will be shifted from right to left each time switches 0-F [13] are pressed, and displayed by the HEXADECIMAL DISPLAY Lamp [10].

4.2.11 Reset Switch [14]

This switch is used to reset each circuit of the CP and also to reset CP check.

Reset switch [14]

This switch is used to reset each circuit of the CP, and placing it in the hard stop status.

This hard stop status can be released by pressing Start switch [15], and the program starts execution from IPL Phase 3.

Check Reset switch [14]

This switch is used to reset the cause of lighting of the CP Check lamp [17].

4.2.12 Interrupt Switch [15]

This switch is used to cause a program level 3 interrupt. Normally, this switch is used for program-controlled operation panel procedures.

4.2.13 Load Switch [15]

This switch is used to transfer the initial program, and is operated in combination with the IPL Select switch [6].

The lamp of this switch lights:

- When power is turned ON.
- When Load switch [15] is pressed.
- When Reset switch [14] is pressed.
- When machine check occurs

- When Set IPL (byte 0, bit 2) is executed by Output X'79'.
  The lamp goes out:
- It is reset by Output X '79', byte 1, bit 1.

4.2.14 Load Address Compare Switch [15]

This switch is used in combination with the Address Compare Program Stop switch [7] or Address Compare Interrupt switch [7] for program stop or interrupt at program level 1 when the instruction address at execution of the program and the data address of load type instructions coincide with the storage address specified by the Hexadecimal Keyboard switches [13].

4.2.15 Store Address Compare Switch [15]

This switch is used in combination with the Address Compare Program Stop switch [7] or Address Compare Interrupt switch [7] for program stop or interrupt at program level 1 when the execution address of store type instructions at execution of the program coincides with the storage address specified by the Hexadecimal Keyboard switches [13].

4.2.16 Start Switch [15]

This switch has the following functions:
- To cancel the program stop status
- To cancel the hard stop status
- To cancel clock stop status
- To indicate the start of storage single read/write test
- To indicate the start of storage scan read/write test

When this switch is pressed while the Instruction Step switch [7] is on, one instruction is executed each time the switch is pressed.

When this switch is pressed while the Clock Step switch [8] is on, one clock pulse is generated each time the switch is pressed.

4.2.17 Stop Switch [15]

This switch has the following functions:
- To stop the program
- To indicate the end of the storage single read/write test
- To indicate the end of the storage scan read/write test

4.2.18 Set Address Switch [16]

This switch is used when the data set by the Hexadecimal Keyboard switches [13] is to be used as the storage address or register address.

4.2.19 Display Switch [16]

This switch is used in combination with the Storage Address switch [18] or Register Address switch [18], and is used for loading the contents of any address of the storage or register set by the Hexadecimal Keyboard switches [13] and Set Address switch [16]. When this switch is pressed, the DISPLAY A lamp [3] displays the address, and the DISPLAY B lamp [4] displays the load data.

If this switch is pressed when the Storage Address switch [18] is on, "2" is incremented to the storage address each time the switch is pressed.

4.2.20 Store Switch [16]

This switch is used in combination with the Storage Address switch [18] or Register Address switch [18], and is used for storing the data set by the Hexadecimal Keyboard switches [13] into any address of the storage or register set by the Hexadecimal Keyboard switches [13] and Set Address switch [16]. When this switch is pressed, the DISPLAY A lamp [3] displays the address and the DISPLAY B lamp [4] displays the stored data.

If this switch is pressed when the Storage Address switch [18] is on, the contents of storage address are incremented by 2 at each time the switch is pressed.

4.2.21 Function Select Switches [13]

These switches are used for conversation with the program, etc.

Function 1, 2, 3, 4, 5, 6 switches [8]

These switches are used for conversation with the program.

Storage Address switch [18]

This switch is used when the address set by the Hexadecimal Keyboard switches 13 and Set Address switch [16] is to be used as the storage address.

This switch is used when performing storage load/store operations.

Register Address switch [18]

This switch is used when the address set by the Hexadecimal Keyboard switches [13] and Set Address switch [16] is to be used as the register address.

This switch is used when performing register load/store operations.

4.2.22 Lamp Test Switch [18]

When this switch is pressed, all lamps except the top rack lamp will turn on.

4.2.23 Panel ON/OFF Switch [18]

This switch is used to put the control panel into the enabled or disabled status. When this switch is turned from ON to OFF, the following switches are placed in the normal status.

- Mode Select switch: Process [7]
- Diagnostic Control-1 switch: Process [8]
- Display Select switch: Status [11]
- Hexadecimal Display Control Switch: Display A to Hex [12]

This switch, however, does not function for the button (POWER ON/OFF [1]) on the top of the rack.

CHAPTER 5
IFT PROGRAM OPERATING PROCEDURES

This chapter describes the operating procedures of the IFT Program of CP. This IFT program is started when any abnormality occurs in CP to confirm the abnormal status of the equipment.

The operating procedure given in this chapter is only an example, and the data shown in the procedure must be changed depending on the system configuration and test method.

For further details on the operating method of the 4705 CP IFT program, refer to the following manuals:

- CP IFT OPERATING INSTRUCTIONS - DESCRIPTION (PUBLICATION NO. F1047.0)
- CP IFT OPERATING INSTRUCTIONS - OPERATION (PUBLICATION NO. F1048.0)
- CP IFT OPERATING INSTRUCTIONS - MESSAGE (PUBLICATION NO. F1049.0)

The IFT Program is operated by the procedure shown in Fig. 5.1.

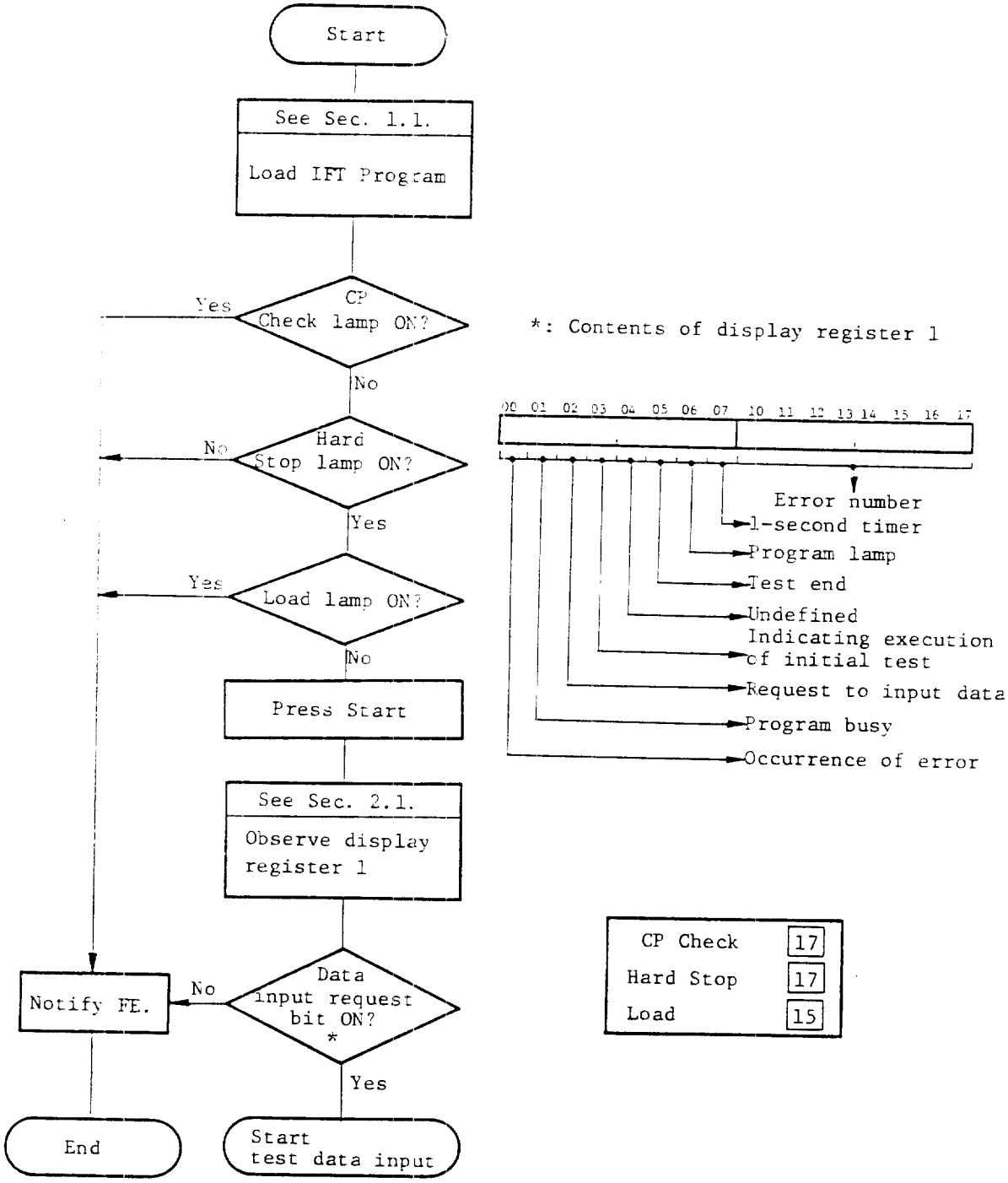


Fig. 5.1 IFT program operating procedure

5.2 CC TEST OPERATING PROCEDURE

CC can be tested by the operating procedure shown in Fig. 5.2.

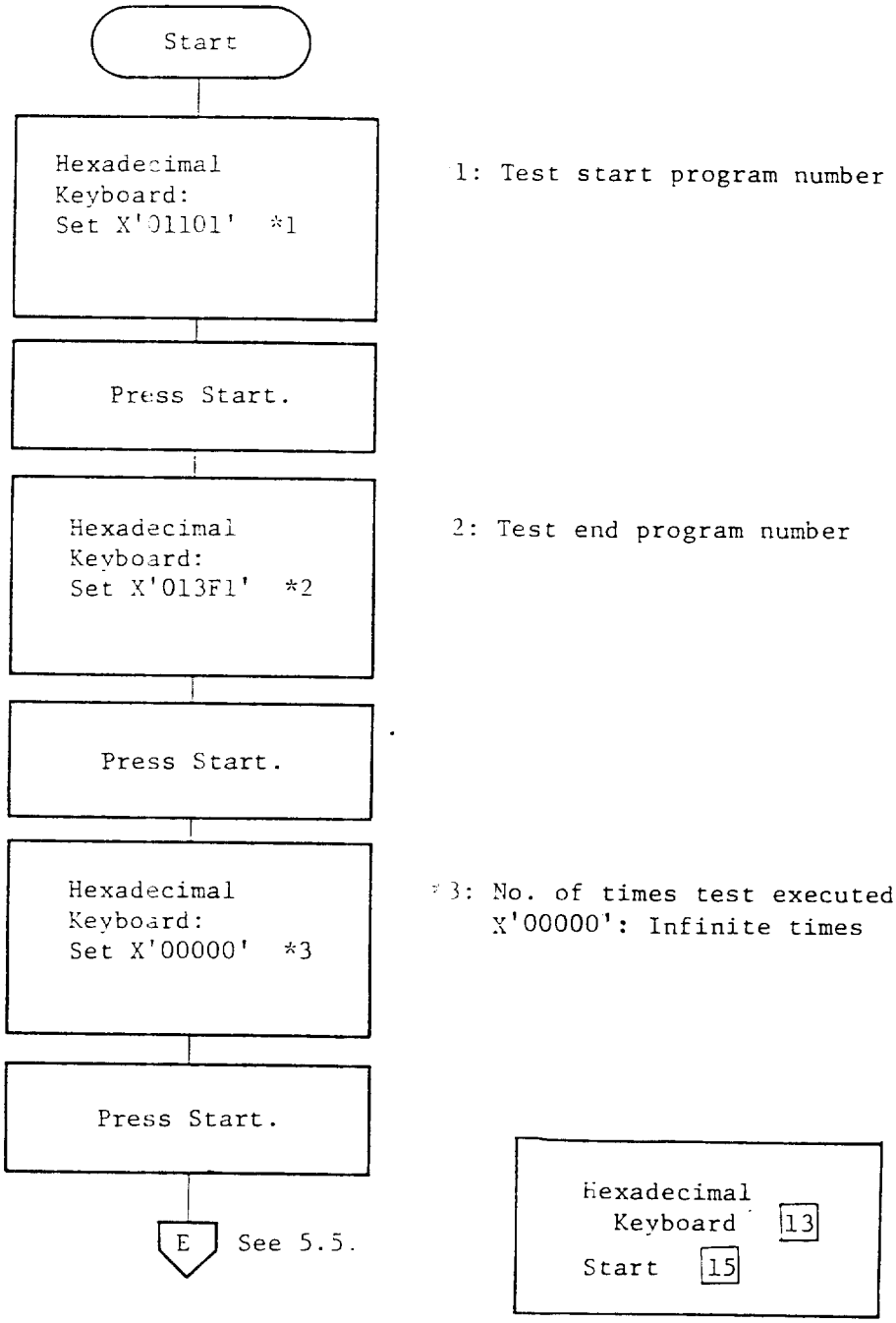


Fig. 5.2 CC test procedure

CS2 can be tested by the procedure shown in Fig. 5.3.

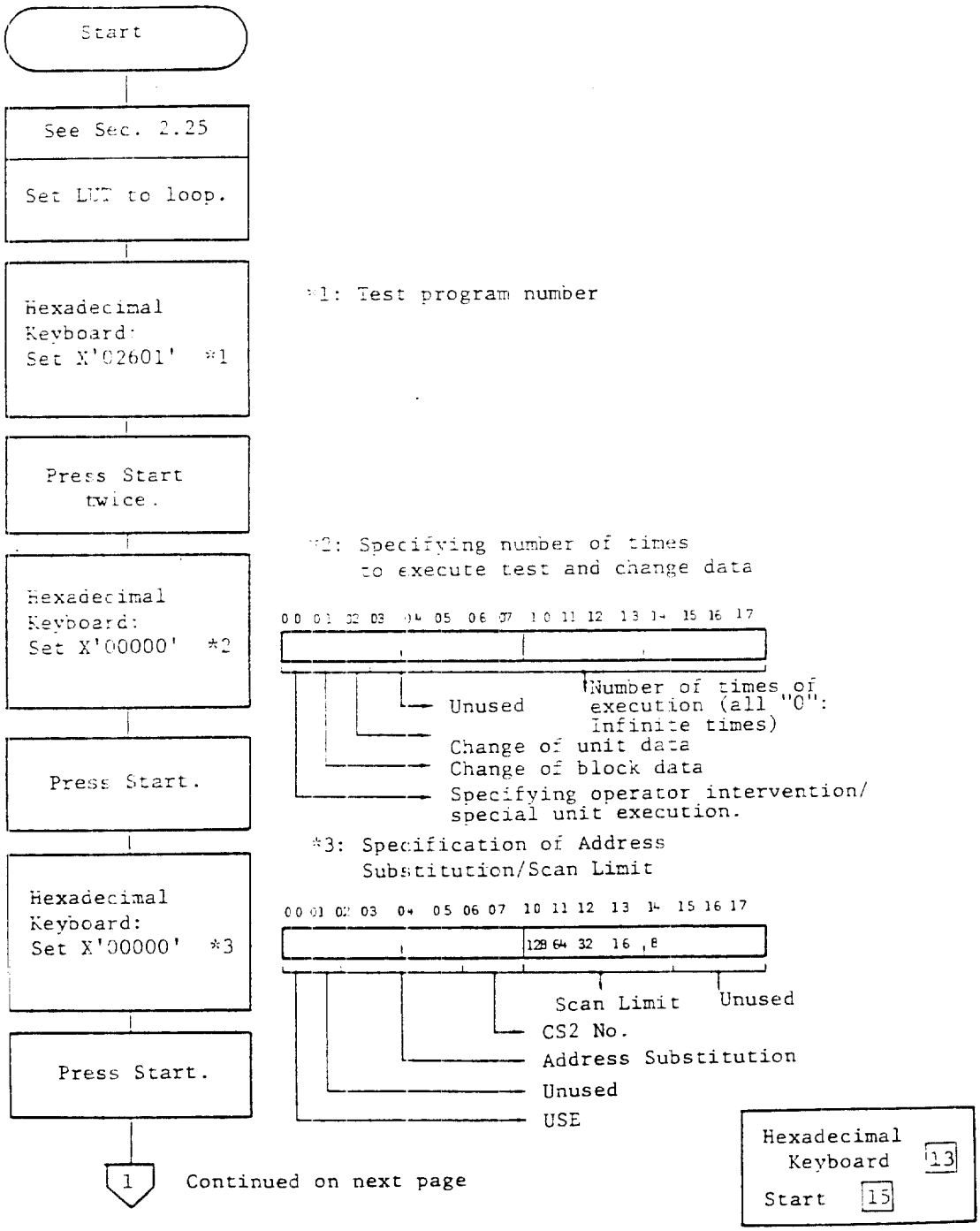


Fig. 5.3 CS2 test procedure

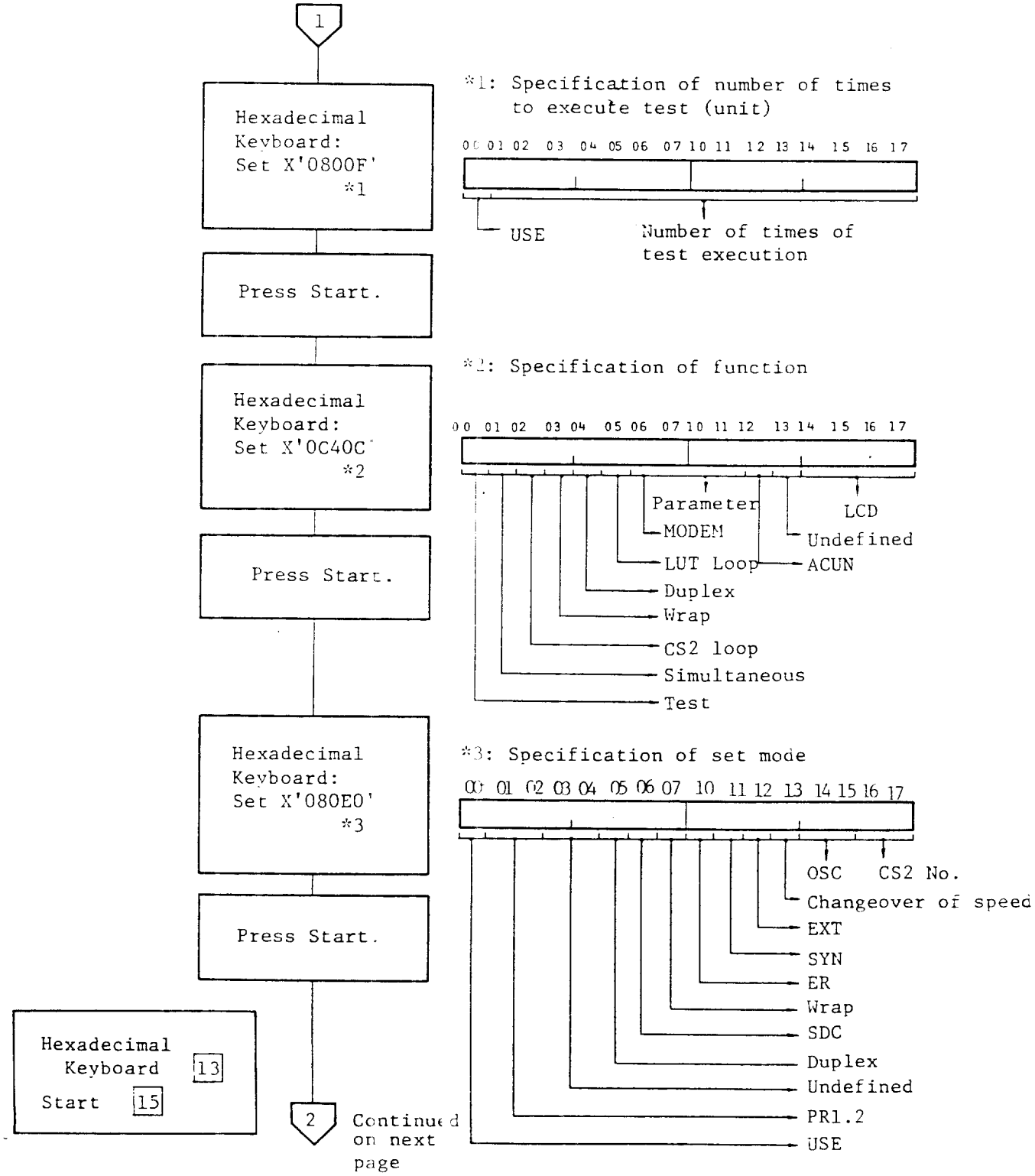


Fig. 5.3 - continued

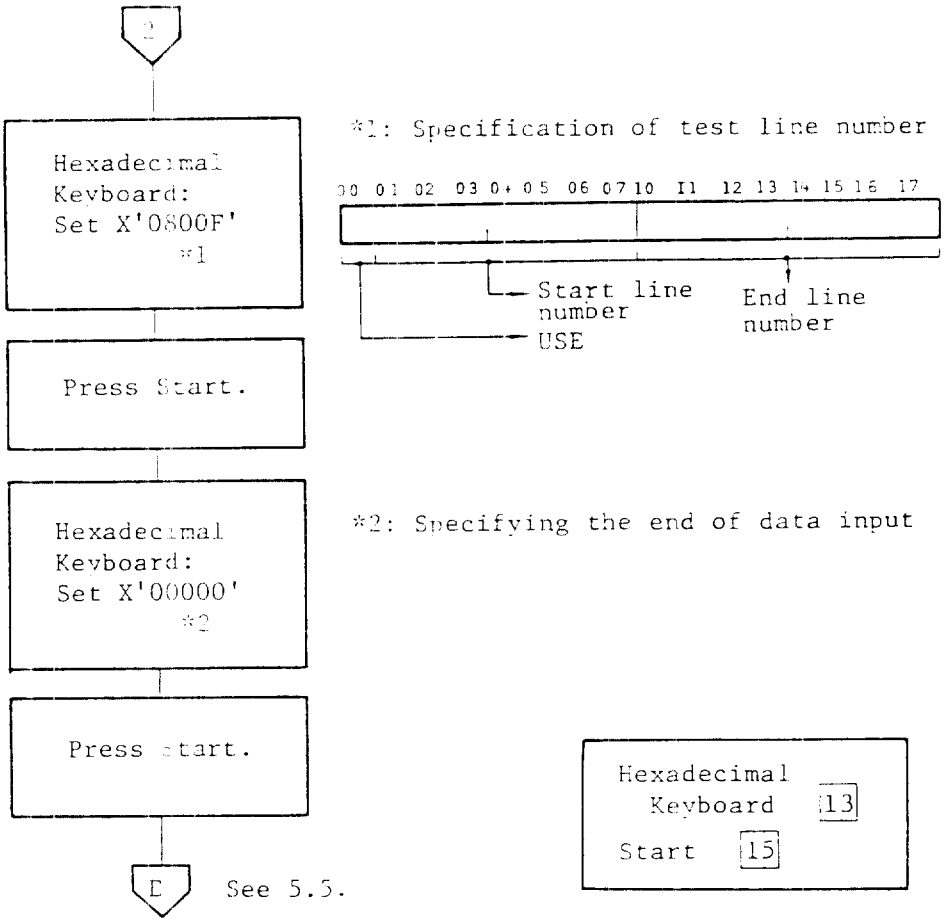


Fig. 5.3 - continued

5.4 CA2/3 TEST OPERATING PROCEDURE

CA2/3 can be tested by the operating procedure shown in Fig. 5.4.

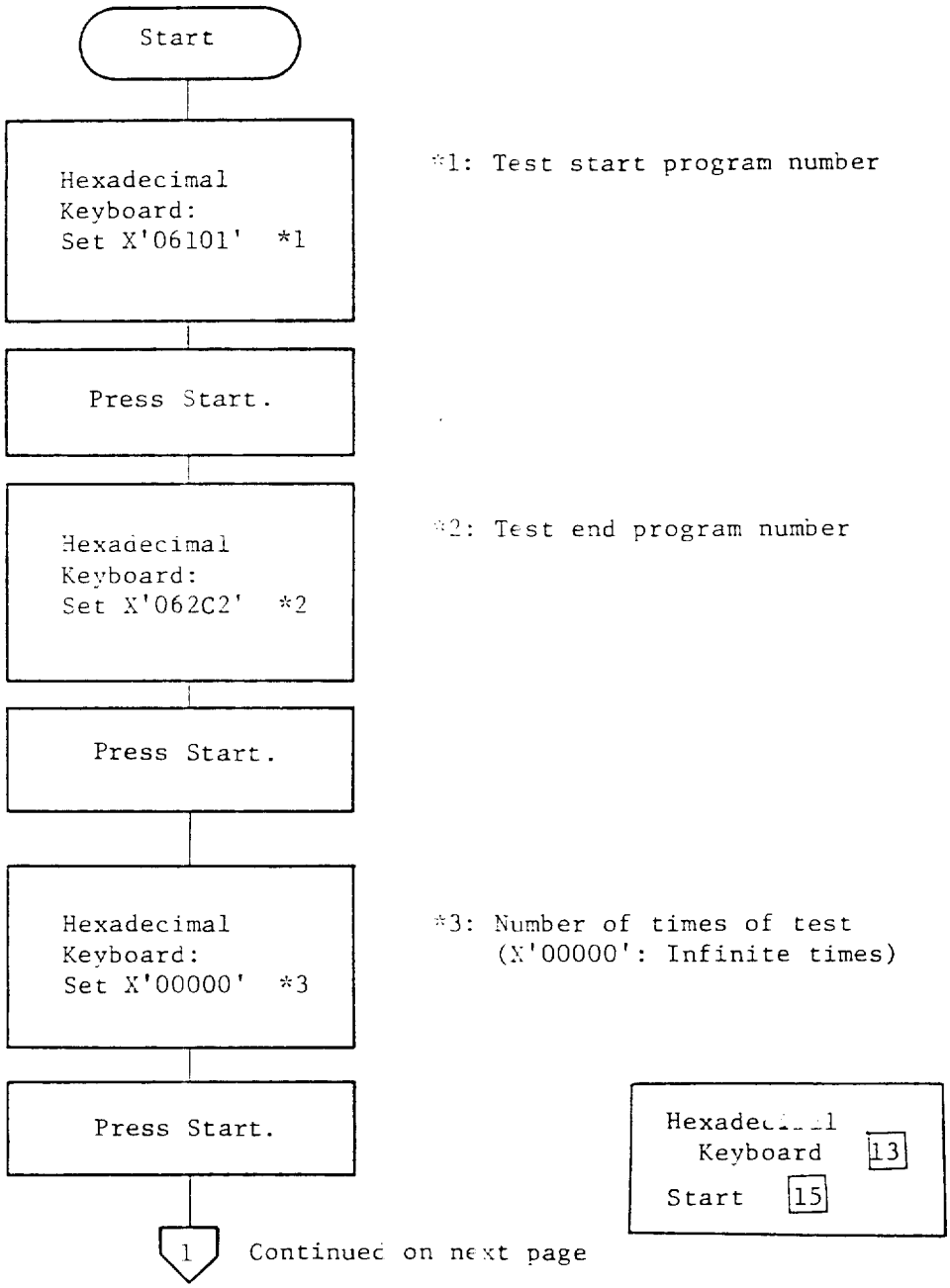


Fig. 5.4 CA2/3 test procedure

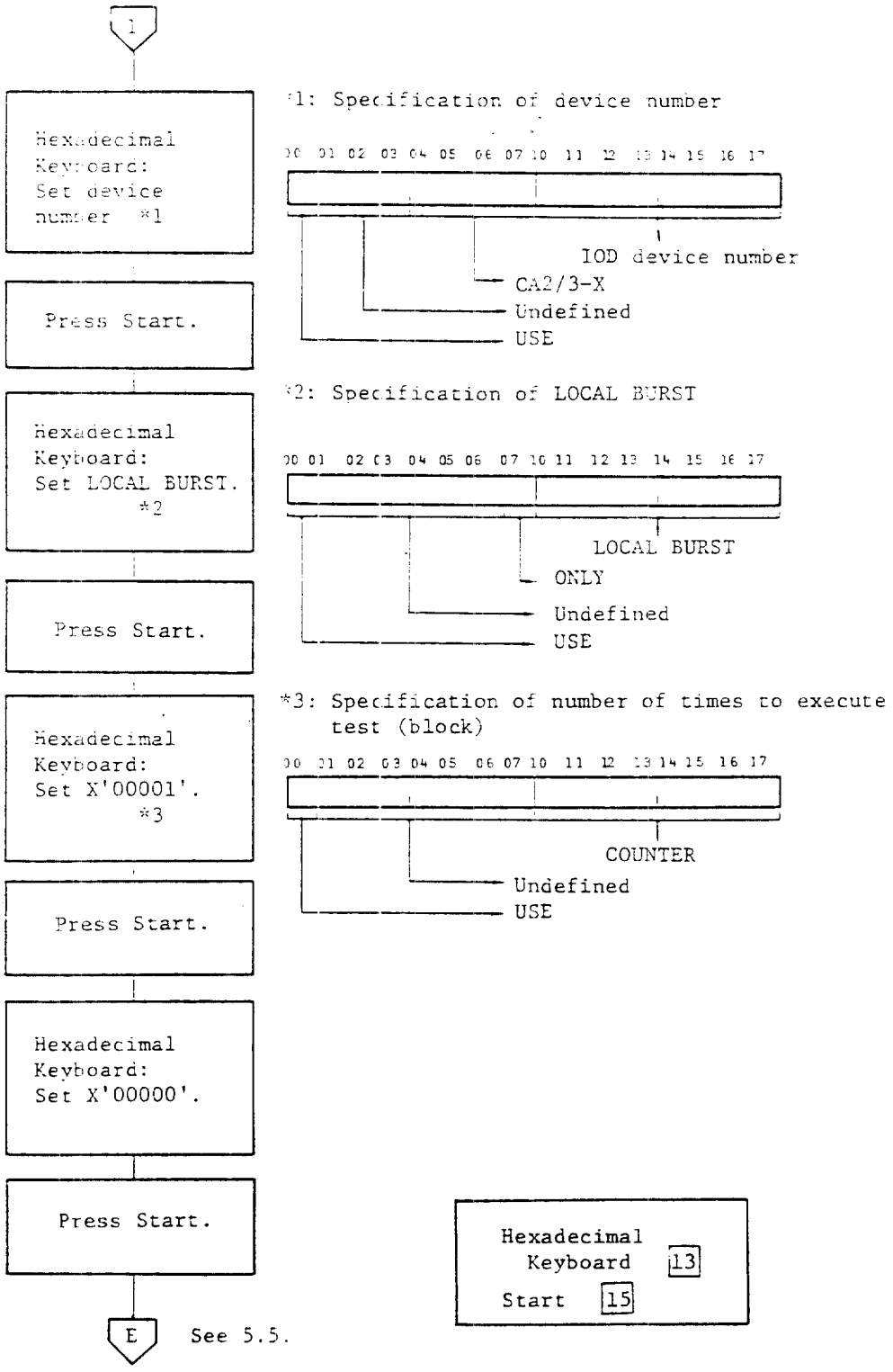


Fig. 5.4 - continued

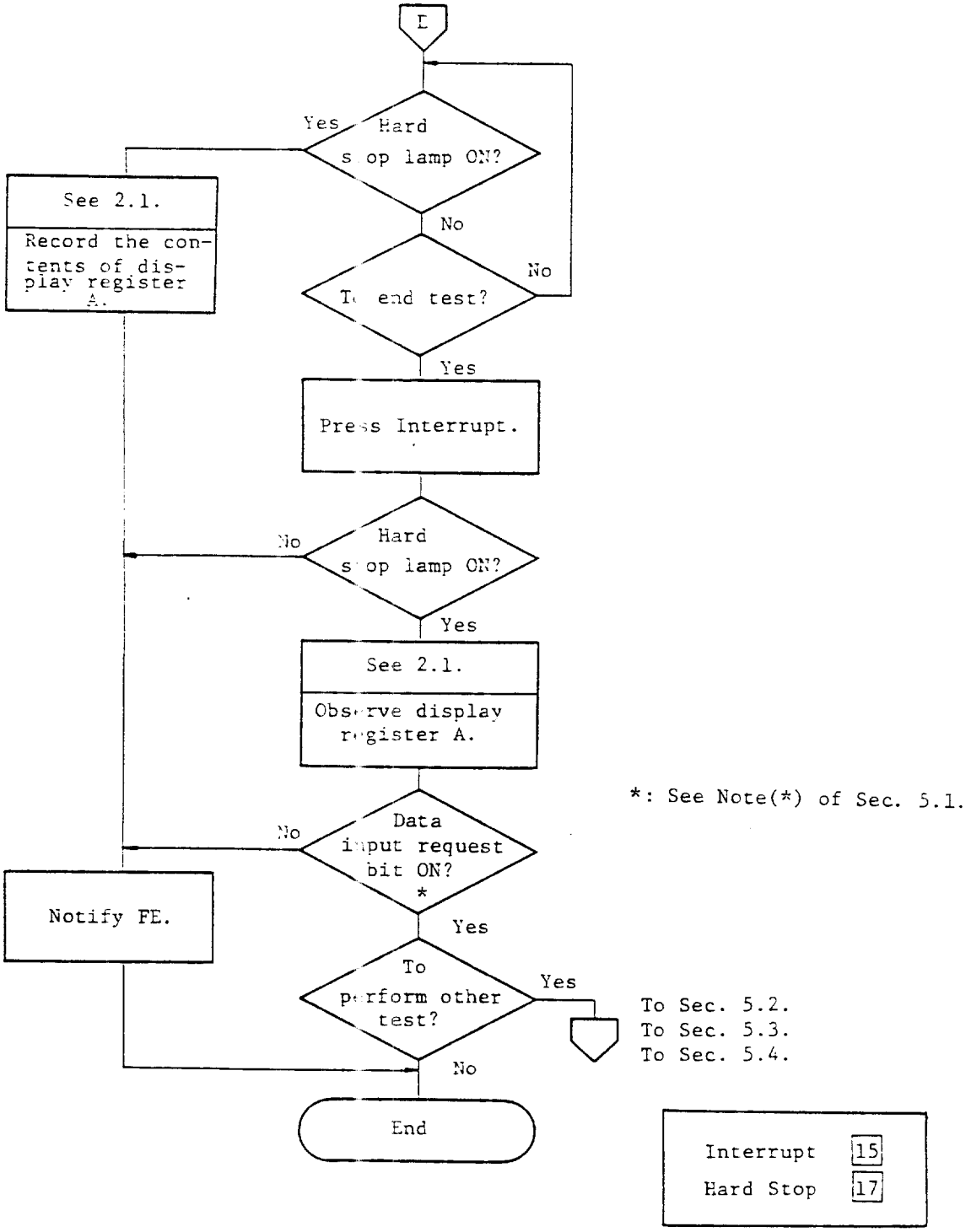


Fig. 5.5 Error processing procedure

MS can be tested by the operating procedure shown in Fig. 5.6.

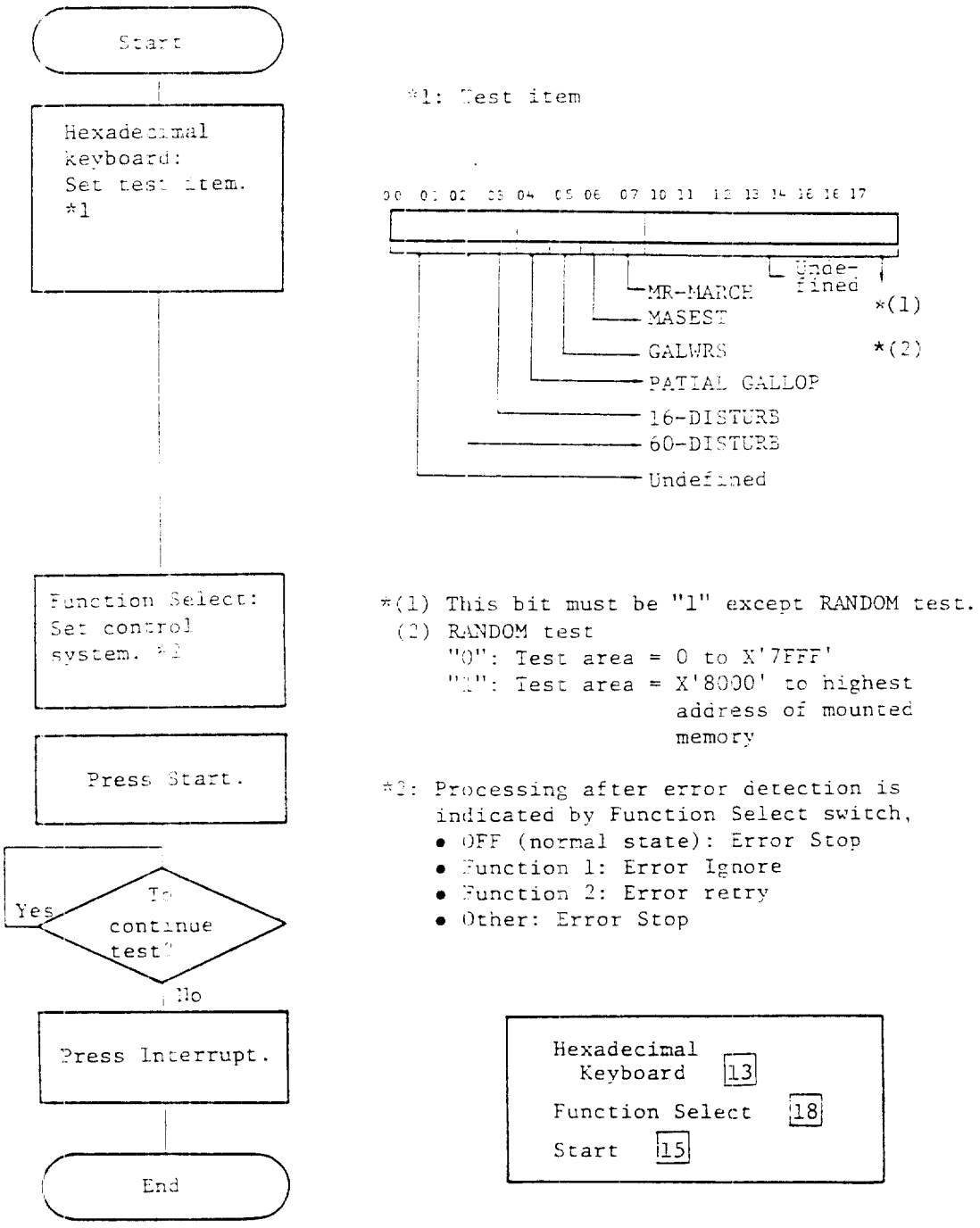


Fig. 5.6 MS test procedure

APPENDIX A

ABBREVIATIONS

AB: Attachment Base
One of the hardware features of the CP. Provides interface logic for the communication scanners.

ACU: Automatic Calling Unit
A dialing device supplied by the communication common carrier, that permits a CP to automatically dial calls over the communication network.

ALU: Arithmetic Logic Unit

BPS: Bits Per Second
Unit of signal transmission speed in serial transmission system. The number of bits transferred per second.

BSC: Binary Synchronous Communication
Method of transmission control.

BSP: Boot Strapping Program
Program for controlling IPL to CP

CA: Channel Adapter
A CP hardware feature that provides attachment of the CP to a host processor channel. There are 3 types channel adapter, Type 2 Channel Adapter (CA2), Type 3 Channe Adapter (CA3), and Type 4 Channel Adapter (CA4).

CC: Central Control Unit
A hardware feature of CP. Control circuits and data transfer buses necessary for executing instructions or for controlling the storage device and various types of adapters connected are included.

CP: Communications Processor
General name for the program built-in type communications processing equipment.

CPU: Central Processing Unit

The CP is connected to this unit through the channel. This executes the communication access program which supports the CP. (CPU is also called the host processor.)

CS: Communication Scanner

A CP hardware feature that provides the connection between the line interface base and the central control unit. The communication scanner monitors the communication lines for service request.

FDD: Flexible Disk Drive

A single magnetic disk unit. An optional hardware feature of CP. This FDD permits loading of maintenance and other control programs to CP by the boot strap program for FDD.

IAR: Instruction Address Register

Instruction address to be executed next by CP.

ICW: Interface Control Word

This provides a means by which the control program is able to exchange information with the CS2, LIB and LS Hardware. ICW is defined in the storage area of CS2, and the major functional area are listed below.

- Line Control Definer (LCD)

  This unit defines the type of line to be controlled by ICW. This unit is initialized by the control program so that it will coincide with the LS connected to LIB and the transmission control format.
- Primary Control Field (PCF)

  This unit defines the control status of the line. According to the transmission control format defined by LCD, control of the modem and supervision of its status, transmission and reception of data bits are defined sequentially.
- Parallel Data Field (PDF)

  Used as a character buffer when transmitting or receiving data.
- Secondary Control Field (SCF)

  This field is used by the control program for sensing the status of the communication line.
- Serial Data Field (SDF)

  Used to code the characters to be transmitted into a bit string, or to decode the received bits to characters. In the case of the switching line, however, this field is used as the NCU interface signal information buffer.
- In addition to the above listed fields, program level 2 interrupt request flag, and various control or status information of CS2 are defined in ICW.

IFT: Internal Function Test

A test program used to check whether the hardware of the CP is functioning normally.

IPL: Initial Program Load

A series of operations necessary for transferring the CP control program for the connected host processor at the beginning of use, and for storing into the storage.

IR: Instruction Register

This register retains the operation code of the instruction to be executed by the CP.

K byte: Kilobyte

Kilo is used in the sense of decimal 1,024 (2^{10}).

Namely, 1K byte = 1,024 bytes

LCD: See "ICW."

LIB: Line Interface Base

A hardware device of the CP. Provides interface logic for up to four line set features.

LN: Line Number

The number attached for convenience to the 96 communication lines connected to the line interface base through the line set.

LS: Line Set

A hardware feature of the CP. A line set supports one, two or four communication lines.

LUT: Line Unit

The general name is given for the line interface base and line set among the hardware device of the CP.

MS: Main Storage

The CP main storage stores the control program and messages. The storage capacity of the CP in the basic configuration is 64K bytes, and can be extended in 64K byte steps. The maximum configuration is 512K bytes.

PCF: (See "ICW.")

PDF: (See "ICW.")

SCF: (See "ICW.")

SDF: (See "ICW.")

SDLC: Synchronous Data Link Control

Although the "Basic Mode Control Procedure" is specified as the international standard (ISO recommendation, 1745) for the transmission control procedure, it has become inadequate because of the increased requirements for inter-computer communication in recent years, and this SDLC was proposed by the U.S.A. in 1970.

The International Organization for Standardization (ISO) changed the name to High-level Data Link Control Procedures (HLDC).

SVC: Supervisor Call

This indicates the request for starting the supervisory program, that is, the supervisor, among the CP control program. The supervisory program can be considered as a type of medium (control routine) necessary for setting the status of the source and for maintaining the proper processing flow.

SYN: Synchronous Idle Character

One of the function characters. If none of the other characters is available in the synchronous transmission system, this character can be used to issue the signal for synchronizing the data terminal, or for maintaining such state.

TCS: Two Channel Switch

A feature that allows the CP to be attached to two channels through one channel adapter.

VTAM: Virtual Tele-communication Access Method

A method of communication access to the terminal and terminal computer and other local devices via the communication line (for example, character display directly coupled to channel, and computer coupling with inter-channel coupling device, etc.).

The communication network composing devices and local devices are directly accessed by VTAM, and no particular attention is required for the CP, communication line and control equipment in performing communication.

VTAM not only has the data transmitting function like the conventional communication access method, but is also provided with functions that are able to cope with requirements for system diversification and effective use of network sources. It can therefore be applied widely to online systems ranging from small scale to large scale.

WIPL: Write IPL

A channel command issued from he host processor. This is used when loading the control program to the CP. Channel adapter 2/3, when detecting the WIPL command, re uires the CP to enter IPL operation, and the central control unit, pon accepting such request (that is, upon entering IPL operation), tarts the bootstrap program.

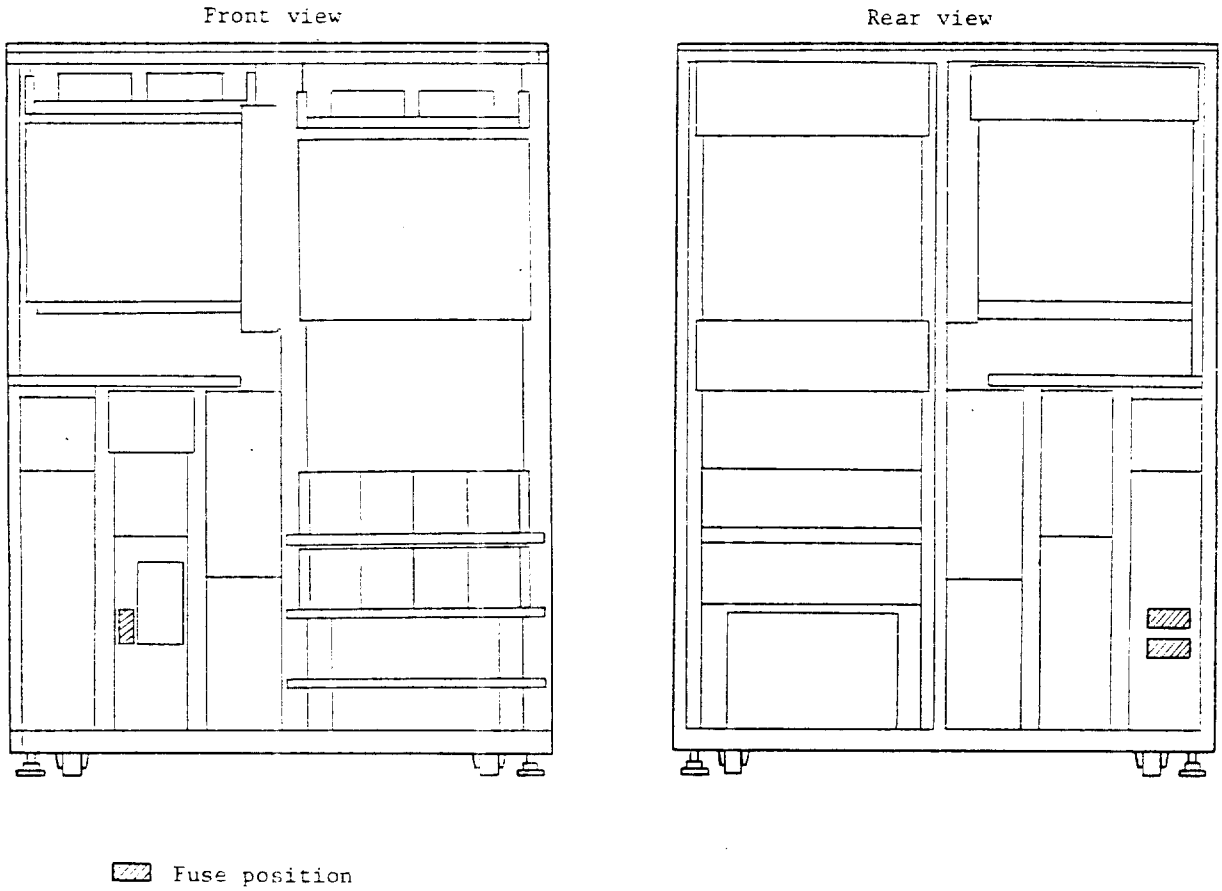


Fig. A.1 AMDAHL 4705 CP basi unit mounting diagram (1/2)

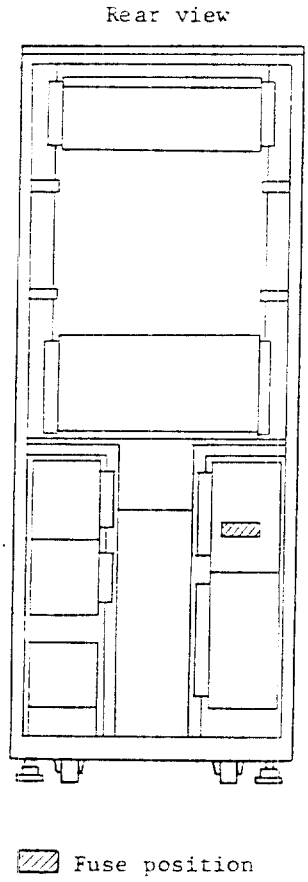


Fig. A.1 4705 CP expansion frame mounting diagram (2/2)

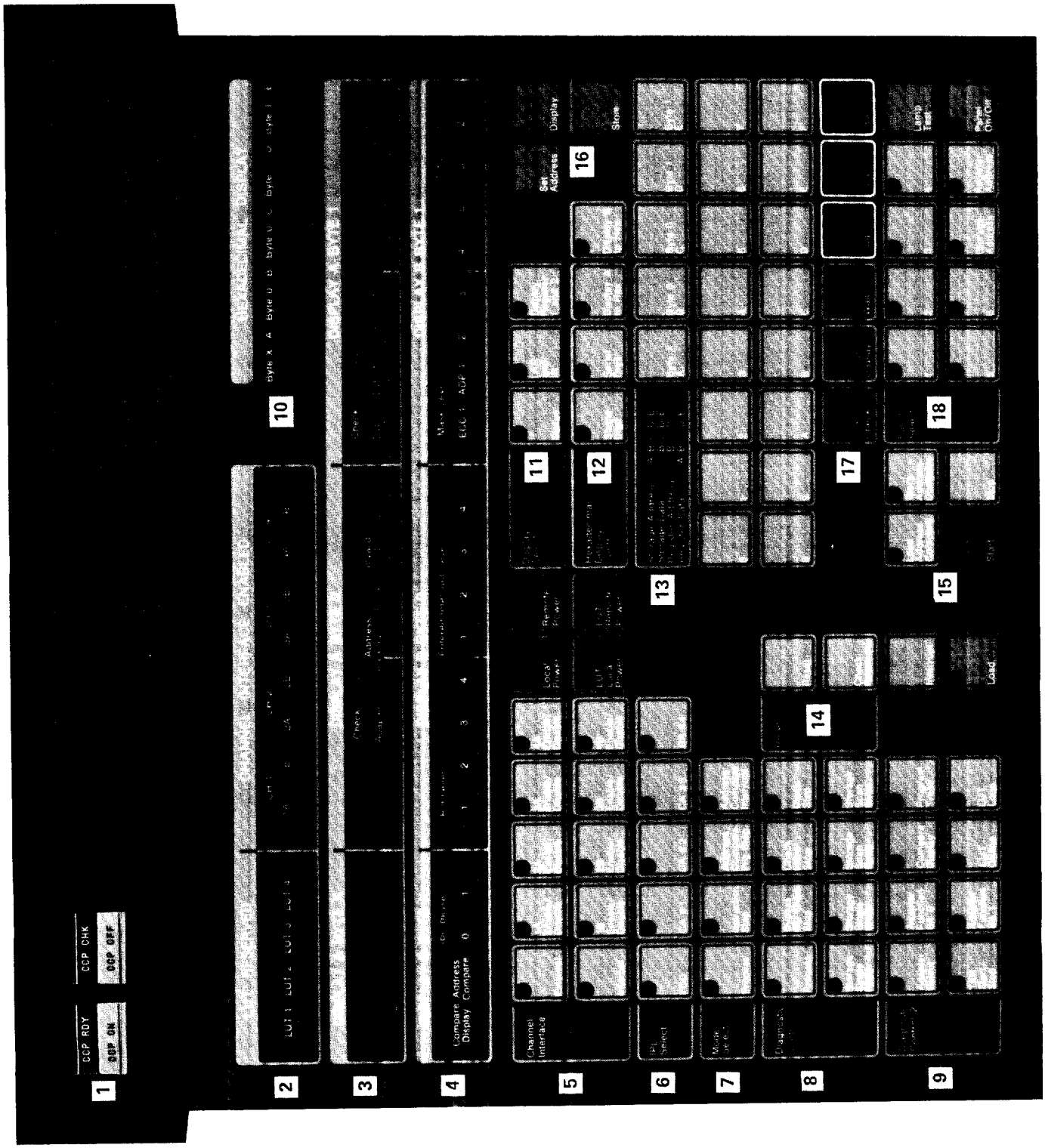


Fig. A.2 AMDAHL 705 CP operator panel diagram

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This revision history lists all versions of this publication along with their effective dates. Also listed is each page and its most recent version number. This version number is either 01A (if the page has never been revised) or the number of the most recent version in which the page was revised.

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