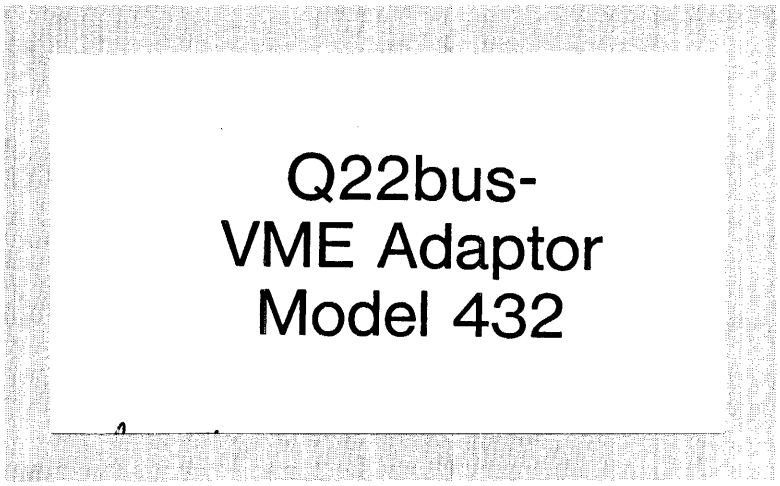
BUS ADAPTOR PRODUCTS
CHASSIS PRODUCTS



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SUN
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-SOLID
CONDUCTOR
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Q-BUS

IBM PS/2 MCA

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BIT 3
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INTRODUCTION

The Bit 3 Model 432 Q22 - VME ADAPTOR permits the interconnection of a Q22 system and a VMEbus system. The two systems can be configured in a TRANSMITTER/RECEIVER relationship or in a TRANSMITTER/TRANSMITTER relationship. A processor on the TRANSMITTER system can appear as a bus master processor on the other system. The memory windowing technique used to interconnect the two systems enables a bus master processor to communicate with memory or I/O on the other system without interim software drivers. Memory windowing maps memory addresses from the destination system's address space onto the host system's address space. The window size is jumper selectable and can range from 65 Kbytes to 16 Mbytes. A processor performing random access reads or writes to any address within the window in its address space has the read or write translated by the ADAPTOR into a read or write on the destination system. Hardware interrupts can be exchanged between the two systems.

The 432 Q22 - VME ADAPTOR consists of two printed circuit cards -- one for the VME card cage and one for the Q22 card cage.

Optional dual port RAM is available in the form of a daughter board that plugs into one of the two cards. The dual port RAM appears as a common memory to both systems. It is a convenient memory for electronic mail box or other applications where a processor needs to read or write to a common memory without using the other system's bus to access memory.

Multiple Q22 and VMEbus systems can be connected together in a star, daisy chain or combination star/daisy chain configuration. Other Bit 3 bus adaptor products permit MULTIBUS I and IBM PC/AT systems to be included in the configuration.

The ADAPTOR enables a bus master processor on the host system to directly address memory in the destination system as though it were local memory.

There are five ways to communicate between the two systems.

First, communication between the two systems can be via random access memory reads or writes. There is no need to pass data through intermediate software drivers. A processor in the host system can even execute code from memory on the destination system. This technique provides an easy to use, very flexible interface with low overhead. The high speed interconnect permits random access 16-bit read/writes to the destination system at speeds comparable to read/write speeds on bus memory cards on the host system. The user can establish the resulting host and destination address ranges in 24-bit VMEbus address space or in 22 bit Q-bus address space with BIAS jumpers.

Once the jumpers have been set up, the adaptor can be used as a bridge, invisible to the system software, between the two buses.

The system software does not have to check status of the adaptor card or execute any kind of setup program to initialize the adaptors. There are, however, additional features, (such as status on the interface) that are available if the applications system software is programmed to use them.

Up to 16 Mbytes of VMEbus memory can be assessed from the Q-bus. Up to 4 Mbytes of Q-bus memory can be accessed from the VMEbus.

A second method of communication is via 65 Kbyte paging.

A 65 Kbyte window in the Q-bus address space is coupled with an eight-bit programmable register. The address referenced within the window provides the lower sixteen address bits and the I/O register provides the upper eight bits of the 24-bit VMEbus address. The Q-bus system can then access up to 16 MBytes of memory in the VMEbus system by paging in 65K byte increments. The VMEbus system can access 4 Mbytes of Q-bus address space using 65 Kbyte to 1 Mbyte pages. A six-bit programmable register is used to provide the upper six bits of the Q-bus address.

A third method of communications is via block mode memory to memory DMA transfers. The Q-bus adaptor has a DMA controller that can be instructed to move up to 128 Kbytes of data between memory on the Q-bus and memory on the VMEbus. The DMA data rate is between 500 Kbytes and 700 Kbytes per second.

A fourth method of communication between the host and destination system is via I/O. Q22 I/O on the destination system can be directly addressed by a processor on the host VME system as host system I/O. VME host system short I/O reads or writes within the VMEbus I/O window are translated by the ADAPTOR into Q22 I/O reads or writes. Conversely, Q22 I/O reads or writes within the Q22 I/O space window are translated into VMEbus short I/O reads or writes.

A fifth method of communication between the two systems is via optional Dual Port Memory. Dual Port Memory is available in 32K, 128K, or 1 Mbyte sizes. It is a low profile daughter card that plugs into one of the ADAPTOR cards. This option provides a memory or DMA buffer available for use by both systems, and can save the cost of purchasing additional memory cards. Use of the dual port RAM can conserve bus bandwidth since neither system ties up the other system's bus when it reads or writes to the dual port RAM. The dual port RAM can be mapped into unused space on both systems with independent address jumpers on both boards.

An important feature of the Bit 3 Q22 - VME ADAPTOR is that it is not a simple repeater-type connection which links the timing of both buses together so that activity on either bus slows down the other bus. Instead, the Bit 3 model 432 ADAPTOR permits each bus to operate asynchronously and independently of the other. The two buses are linked only when a memory or I/O reference is made to an address in the window that translates to a reference on the other system.

Byte and word swapping (to adjust for the difference in addressing conventions between DEC and MOTOROLA type microprocessors) is supported by both jumper selection and command bit selection.

Interrupts on the VMEbus (IRQ1, IRQ2, IRQ3, or IRQ4) can be passed to the Q-bus. The VMEbus interrupt can be mapped into any of the four Q22 interrupt levels. Conversely, if there is no processor card in the Q22 system, any one of the four Q22 interrupts can be passed to one of the aforementioned VMEbus interrupts. It is also possible to pass interrupts between the two systems under program control. Either system can generate an interrupt acknowledge cycle on the other system. Interrupts are configured with jumpers.

If there is no system controller in the VMEbus application, the VME card can be configured with jumpers to drive the VME SYSCLK and to act as a single level bus arbiter on level 3. Also, if there is no processor card on the Q-bus, the Q22 card can be configured with jumpers to provide bus arbitration and to support interrupt acknowledgment. Additional system controller type cards are not needed.

Normally, one of the Bit 3 ADAPTOR cards is set with a jumper to allow its host bus to become a transmitter on the destination system. The companion receiver ADAPTOR card in the destination chassis is jumpered to accept commands from the host system but not to attempt reads and writes back to the host bus. Both cards, however, can be jumpered to permit them to become transmitters to the other bus.

The interface between the two cards is parity checked on address, control, and data lines.

I/O cables of eight feet, twenty-five feet, and fifty feet are available. A long line differential driver module is also available to extend cable distances to 300 feet.

Support software for MicroVMS users is available from Bit 3.

INSTALLATION

The Adaptor package contains the following items:

* A VME printed circuit card Model 432-202
* A Q22 printed circuit card Model 432-201
* This Manual Model 432-901
* An I/O cable to connect the two cards (purchased separately)

* A warranty card

Take time now to fill out and mail the warranty card. Your name will then be placed on our mailing list to receive update information on the Adaptor and other Bit 3 products.

INSTALLING THE ADAPTOR CARDS

It is necessary to study the rest of this manual to understand how to set the jumpers on the adaptor cards. Once the jumpers have been configured, the cards can be installed in their respective card cages by following the instructions below.

INSTALLING THE VME CARD

If a VME ADAPTOR card is to be the only bus master in the VME system, and hence the bus arbiter, it is necessary (per VME convention) to place the card in slot 1. Otherwise, the adaptor cards can be placed in any unused VME card slot. The two cable connectors mate with the I/O cable provided. The cable connectors are mechanically keyed as well as labeled to insure that they will not be connected upside down or backwards. Match the label on the connector to the label on the VME card bracket. The connectors fit tightly to provide a solid electrical and mechanical connection. (When removing the connectors use the pull tabs - don't pull on the wire.) A wire connected to the cable shield and terminated with a terminal lug is provided on each end of the cable.

The VMEbus has a bus priority scheme that permits bus masters to use other cards on the VMEbus. Before the VME adaptor card can talk to other VME cards in the same chassis, it must first gain control of the bus. A VMEbus functional module called the BUS ARBITER grants VME cards permission to use the VMEbus. The arbiter is sometimes located on a separate system controller board. Other times it is integrated into a processor card. It is beyond the scope of this manual to describe VMEbus arbitration but it is essential that the user understand how it works. The VMEbus Specification Manual rev C.1, available from VITA (VMEbus International Trade Association) 10229 N. Scottsdale RD., Suite E, Scottsdale, Az. 85253, describes the VMEbus and the bus arbiter in detail. Experience shows that a common problem users encounter is an inability to communicate with other VME cards because the bus arbiter has been incorrectly configured.

The adaptor can be configured with jumpers to work with an already-installed system controller board containing a bus arbiter. If necessary, the adaptor can provide the system controller function of driving the system clock and can be a single level bus arbiter on level 3. In single level bus arbitration mode, the adaptor is the highest priority bus master. It will respond to bus requests on level 3 from other masters and activate the level 3 bus grant line when the Bit 3 adaptor does

not need the VMEbus. The adaptor operates in RWD (release when done) mode.

The dual port RAM option does not require an extra card slot on the VMEbus.

INSTALLING THE Q22 CARD

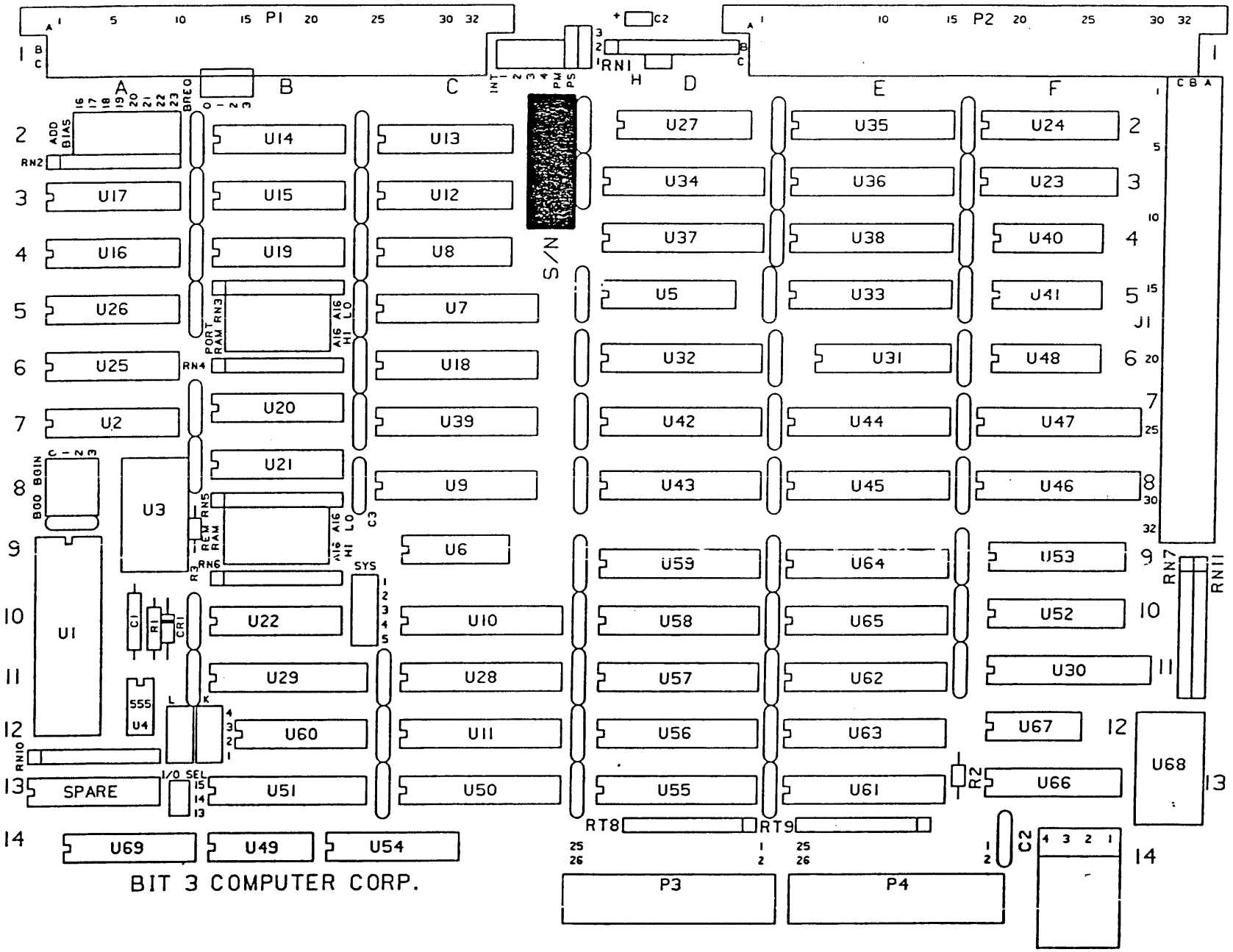
The Q22 card may be installed in any unoccupied quad slot in the Q22 card cage. It is necessary that the Q22 card receive bus grant and interrupt continuity. If there are unoccupied card slots in the chassis, it may be necessary to add bus grant continuity cards in the unused slots.

The MicroVAX chassis reserves the first three slots of an eight-slot backplane (and the first four slots of a twelve-slot backplane) for processor and memory cards. These slots are called Q/CD-type; the C- and D-connectors of these slots do not wire through the standard Q-bus signals. The remaining slots are for general use and are called Q/Q-type; the C- and D- connectors duplicate the standard Q-bus signals on the A- and B- connectors.

The BIT 3 Q-bus board is factory-jumpered to be installed in one of the general-use Q/Q slots in the backplane. If the user chooses to install the board in a Q/CD slot, the CONT jumpers at location A8 should be removed. (See page 36.)

If a dual port RAM card is installed on the Q22 card, the Q22 card may occupy two Q-bus card slots. A bus grant continuity card is provided with the dual port RAM card to insure that bus grant continuity to other cards in the Q-bus is maintained. (See page 37.)

The two cable connectors mate with the I/O cable provided. Match the label on the cable connector to the label above the connector on the Q22 card. The connectors are keyed so that the cables cannot be connected incorrectly. Connect the cable shield wire lug to the computer chassis.


P1
P2
C2
RN1
INT
PM
PS
A
B
C
D
E
F
BREQ
ADD BIAS
RN2
PORT RAM
RN3
A16 HI
A16 LO
RN4
REM RAM
RN5
RN6
SYS
C3
BOO
BOIN
U1
U2
U3
U4
U5
U6
U7
U8
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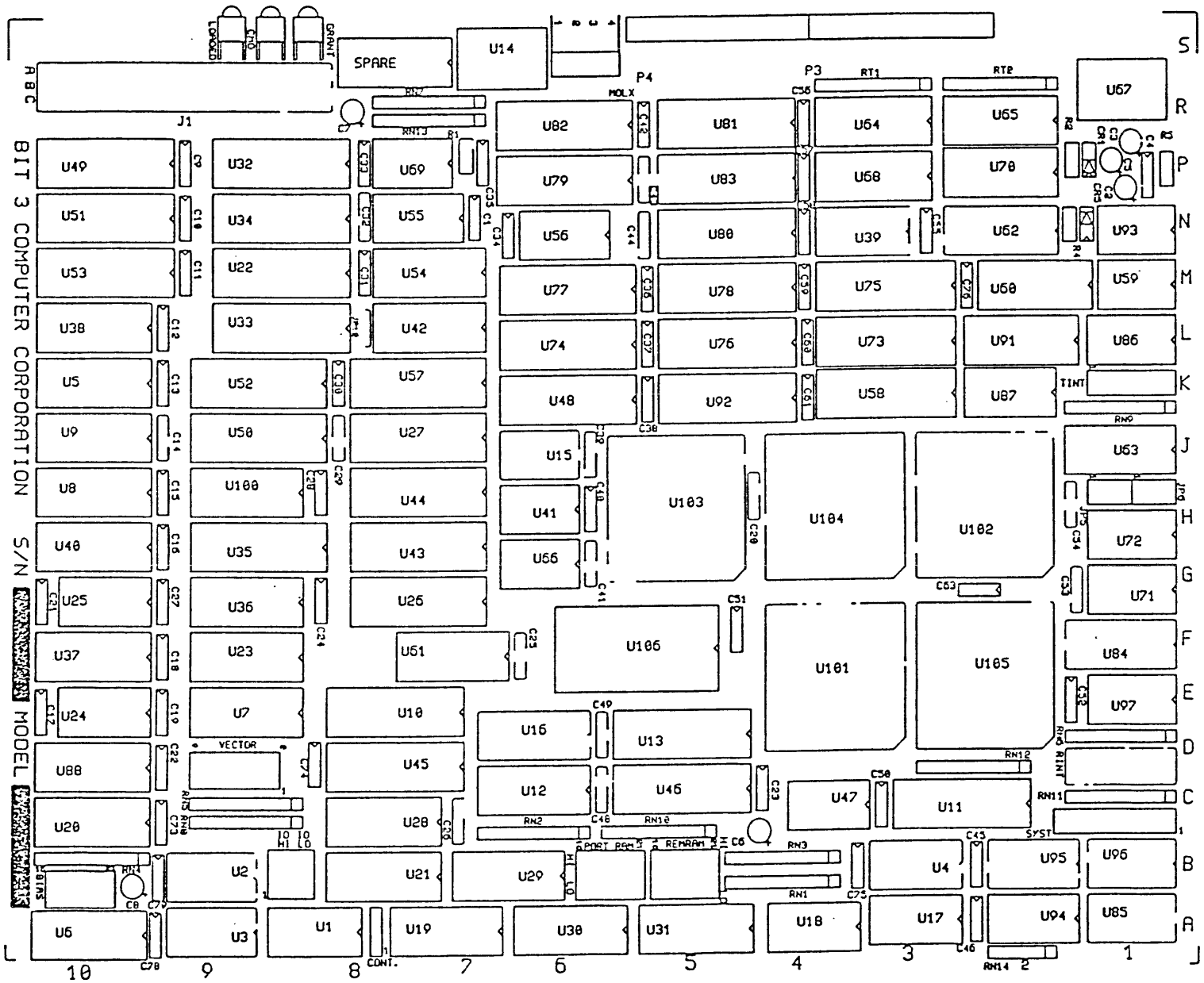
U69
U49
U54
C1
R1
CR1
555
I/O SEL
SPARE
RN10
RN7
RN11
R2
RT8
RT9
S/N
J1
P3
P4
BIT 3 COMPUTER CORP.



TOP SILKSCREEN

MEMORY MAPPING

The 432 adaptor works by mapping a portion of memory address space in the second chassis into memory address space on the first (host) chassis. The memory in the second chassis appears to the first chassis as though it was logically present in the first chassis and behaves as it would if the memory were located on a memory card in the first chassis. It is also possible to map a portion of memory space from the first chassis into memory space on the second chassis (transmit/transmit mode). With this hardware mechanism it is possible for a Q-bus processor to directly read and write to memory or I/O devices located on a VMEbus or for a VMEbus processor to directly read and write to memory or I/O devices on the Q-bus.

In Q-bus to VMEbus operations, the Q-bus processor can address both 24 bit VME memory space and short 16-bit VME memory space. The address modifier code presented to the VMEbus can be either the default values sent from the Q-bus adaptor card or it can be a value loaded into a register on the VME adaptor card from the Q-bus processor.

In VMEbus to Q-bus operations, a VME processor can address both normal Q22 address space and I/O page address space.

The absolute address of the memory window in one chassis might not be the same absolute address location that you want to get at in the other chassis. The 432 adaptor provides a means to reposition the window to a different location in the destination bus.

Once the jumpers have been set up, the adaptor can be used as a bridge, invisible to the system software, between the two buses. The system software does not have to status the adaptor card or execute any kind of setup program to initialize the adaptors. There are, however, several additional features built into the adaptor cards that can be useful if the system software is set up to take advantage of them. For example, parity on all transfers between buses is checked and any parity errors are recorded in an adaptor status bit. There is a "page mode" of operation which can be used under program control to access memory outside of the jumpered window boundaries, and the adaptor can be set up to use an address modifier from a programmable register instead of using the address modifier code presented with the memory address. In Q-bus to VMEbus applications, there is a memory-to-memory block mode DMA capability that will move up to 128 Kbytes of data back and forth between the two systems. Also, a "reset bus" command can be sent from one chassis to the other chassis. This information is presented in the section on functional programming of the adaptor.

The data path between the two buses is 16 bits wide and the address path is 24 bits wide. Both byte (8-bit) and word (16-bit) data paths are supported. Byte swapping, sometimes required because of the addressing differences in MOTOROLA and DEC

microprocessors, is supported.

The optional dual port RAM card supports full 32-bit longword data transfers (from the VMEbus to the dual port RAM card only) as well as word and byte transfers.

Before setting the jumpers, take a minute to consider your system architecture.

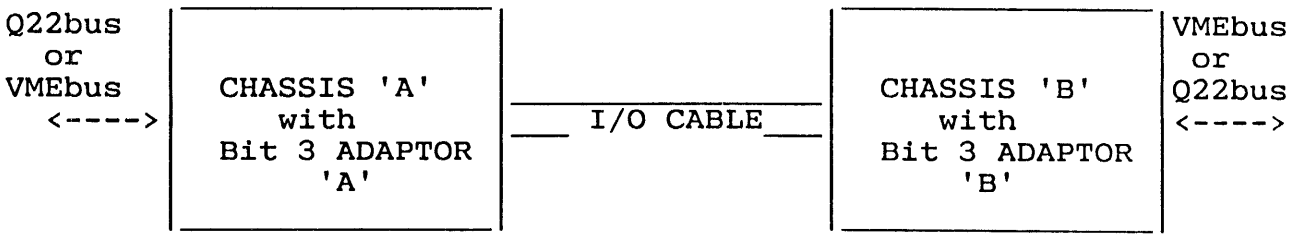


FIGURE 1 NOMENCLATURE

If a device in chassis 'A' performs reads or writes to memory or I/O on chassis 'B' but devices in chassis 'B' never perform reads or writes to memory or I/O cards inside chassis 'A', then, for the purposes of this manual, chassis 'A' is designated as the TRANSMIT (or host) chassis and chassis 'B' is designated as the RECEIVE (or destination) chassis. Jumpers in the SYS jumper block on each adaptor card configure an adaptor as either a transmit device or a receive device. In the above example, adaptor 'A' would be jumpered as a transmit adaptor and adaptor 'B' would be jumpered as a receive adaptor. Except for interrupts, the transmit adaptor has exclusive rights to use the I/O cable interface connecting the two adaptor cards. In this case, the optional dual port RAM card would be installed on the receive adaptor since, if the dual port RAM card was installed on the transmit card, it could not be accessed by the receive card (because the receive card cannot use the I/O cable for reads and writes). In any adaptor pair configuration, only one of the two adaptors can contain the optional dual port RAM memory card.

If devices in chassis 'A' sometimes perform reads or writes to chassis 'B' and devices in chassis 'B' sometimes perform reads or writes to chassis 'A', then both adaptors must be jumpered as transmitters. Either chassis can then control the other chassis. In this configuration, it is possible for a cable interference situation to develop if chassis 'A' tries to use the interface cable to talk to chassis 'B' at the same time that chassis 'B' tries to use the interface cable to talk to chassis 'A'. Hardware is not present to arbitrate this situation. If the flow of data between the two systems is sequenced such that both adaptors do not talk to the other chassis at the same time, then both adaptors can be jumpered as transmitters with no concern for

cable interference since it could not arise. A typical example would be a processor in chassis 'A' instructing a disk controller on chassis 'B' to read a file and DMA the file to memory in chassis 'A'. The processor in chassis 'A' would become a transmitter on chassis 'B' long enough to issue the command to the disk controller instructing it to do the operation and interrupt upon completion. The processor on chassis 'A' would then not use the adaptor interface until it had received the completion interrupt. Meanwhile, the disk controller in chassis 'B' would read the file and DMA transfer it into memory in chassis 'A' by becoming a transmitter over the adaptor interface. Cable interference cannot occur in this situation since the operation is sequenced such that both sides will not try to use the interface at the same time. Also, if communication between the two buses is through the dual port RAM, cable interference cannot occur since the dual port RAM interface is hardware arbitrated. If, on the other hand, communication between the systems is across the adaptor cable on each chassis and if it is bi-directional and asynchronous, cable interference could occur. The situation can be covered by a software semaphore in a number of ways. Consider the following sequence:

Chassis 'B' wants to get to a device in chassis 'A' but chassis 'A' is more frequently a transmitter to chassis 'B'.

The processor in Chassis 'B' does a local I/O write to its adaptor card, setting the PT interrupt flip-flop which sends an interrupt to chassis 'A'.

A processor in chassis 'A' detects the interrupt and does a read-modify-write operation (using a MOTOROLA TAS or DEC BBSSI/BBCCI type of indivisible instruction) to a semaphore flag in local chassis 'A' memory. If another 'A' bus co-processor has not reserved the adaptor to communicate with the 'B' bus, it sets the semaphore flag to indicate "don't use chassis 'B'" and then does an I/O write to the adaptor in chassis 'B' which clears the PT interrupt flip-flop.

The processor in chassis 'B' sees that its interrupt flag bit is reset by doing a local adaptor I/O status read. It is then free to use the adaptor interface to talk on chassis 'A' as long as it wants. When it is finished with chassis 'A', the processor in chassis 'A' clears the "don't use chassis 'B' semaphore flag" in memory on chassis 'A'.

If cable interference results from trying to communicate over the interface cable in both directions simultaneously, the data will probably be lost. Adaptor interface parity errors and interface timeouts will occur.

SETTING THE ADAPTOR CARD JUMPERS

The customary designation for active low VMEbus signals is to follow the signal name with an asterisk (*). This convention is

followed in this manual.

Jumpers are actually installed as shown here.

THE VME ADAPTOR CARD JUMPERS

The adaptor operating modes and memory mapping windows on each card are set by the user via jumpers to configure the cards for the applications system requirements. The VME adaptor card contains the following categories of jumpers:

1. System configuration jumpers -- SYS.
2. The bus arbitration jumpers (VME CARD ONLY) -- BGIN, BGO, BREQ.
3. The interrupt select jumpers -- INT.
4. The address and range of the memory window through which memory in the Q22 chassis is viewed -- REM RAM LO and REM RAM HI.
5. The destination memory address and range jumpers for transfers from the Q22bus to the VMEbus -- ADD BIAS.
6. The VME I/O range select jumpers -- I/O SEL.
7. The VME address and range of the dual port RAM -- PORT RAM HI and PORT RAM LO.

THE SYS JUMPERS

There is some configuration information that you need to know about your VMEbus system.

First, determine if the Bit 3 VME adaptor card is the only bus master in the VMEbus chassis. One of the bus master cards in a VME chassis must provide clocking for the rest of the cards in the system. The Bit 3 adaptor can drive the SYSCLK signal if you choose, but it should only be set to do so if some other card is not already sourcing the signal. The adaptor card will not work if there is no SYSCLK.

Locate the SYS jumper block at location B/C 10 on the VME board.

NOTE: The jumpers shown in place are the factory jumper settings.

```
   SYS
  o--o 1   jumper if the address modifier register is not used *
  o  o 2   jumper if this card is a TRANSMITTER **
  o  o 3   there should never be a jumper on these pins
  o--o 4   jumper if you want Bit 3 card to drive SYSCLK
  o  o 5   there should never be a jumper on these pins
```

* If this jumper is "ON", the address modifier presented to the VMEbus chassis holding this card comes from the default address modifier code sent from the Q22 adaptor card in the other chassis. If the jumper is removed, the address modifier comes from the address modifier register located on the VME adaptor card.

** The term "TRANSMITTER" here means transmitter card, which sends commands to the receiver card. It does not mean that the card is necessarily a VMEbus master.

Second, determine which bus priority scheme is being used to grant the bus masters permission to use the VMEbus. There are several choices. Now might be a good time to review the subject by re-reading the VMEbus specification manual.

If there is a bus arbiter in the VMEbus system, the VME adaptor card can be configured to use any of the four bus request/ bus grant levels. If there is no bus arbiter in the VMEbus system, the VME adaptor card can be set to become a single level arbiter on level 3.

Locate the bus grant out and bus grant in (BGO/BGIN) jumper block at location A8 on the VME board. Also locate the bus request (BREQ) jumper block at location B2.

CAUTION -- VME card cages have jumpers to connect these daisy-chained bus arbitration signals and the interrupt acknowledge signal around unused card locations. Make sure that these jumpers are removed for the card slot that the Bit 3 adaptor is plugged into.

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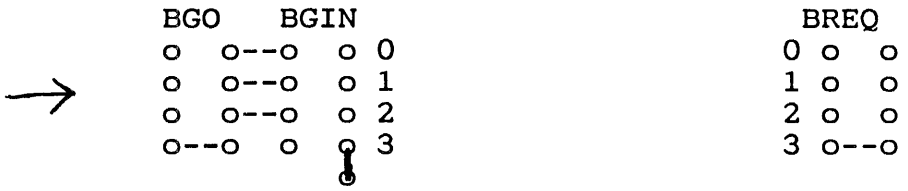
If the Bit 3 adaptor is to be the bus arbiter, configure the jumpers as follows:



If there is another VME bus arbiter and the Bit 3 adaptor is to be configured to use level 3, set the jumpers as follows:

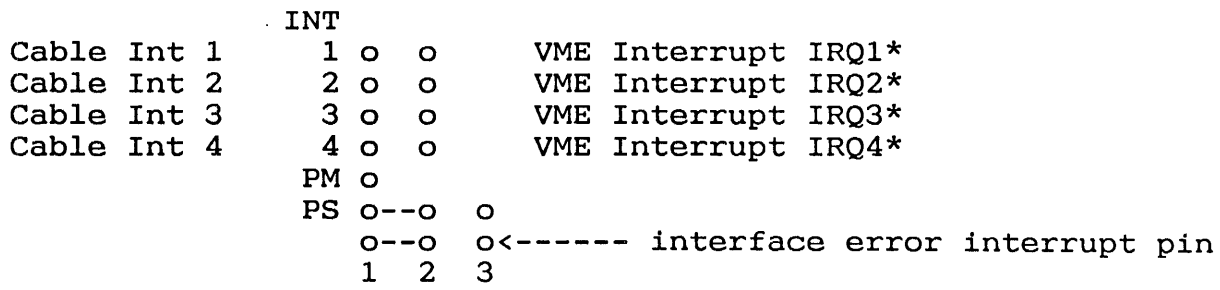
If there is another VME bus arbiter and the Bit 3 adaptor is to be configured to use level 2, set the jumpers as follows:

If there is another VME bus arbiter and the Bit 3 adaptor is to be configured to use level 1, set the jumpers as follows:

If there is another VME bus arbiter and the Bit 3 adaptor is to be configured to use level 0, set the jumpers as follows:

INTERRUPT JUMPERS (INT)

Locate the block of interrupt jumpers (INT) at location C1 on the VME adaptor card. This set of jumpers permits selection of VMEbus interrupt signals to connect between the VMEbus and the Q22bus.



Up to four interrupt lines can be connected between the two buses.

There are also three categories of interrupts. The categories are:

(1) Interrupts that are present on the VMEbus backpanel. Interrupt lines IRQ4*, IRQ3*, IRQ2*, or IRQ1* can be passed to the Q22bus.

(2) Programmed interrupts.

(3) An interface error interrupt.

BACKPANEL INTERRUPTS

Any of the four interrupts IRQ1-IRQ4 on the VMEbus (category 1 above) can be passed to the Q22bus. If the Q22bus adaptor card is connecting interrupts from the Q22bus to the VME adaptor card, then that cable interrupt line cannot be used at the same time to send a VME interrupt back to the Q22bus.

The INT jumper block selects the source of the interrupt lines that can be exchanged. If interrupts of category 1 above are to be sent to the Q22bus, then just put a jumper across one of the IRQ 1-4 lines on the VME adaptor card. On the Q22 adaptor card, make sure that there are no jumpers on the corresponding cable interrupt line pin (in the TINT Q22 card jumper block). If an interrupt is being sent from the Q22bus to the VMEbus, remove the associated INT jumper from the corresponding cable interrupt pin on the VME adaptor card.

PROGRAMMED INTERRUPTS

In addition to interconnecting "raw" backpanel interrupts between the two systems, there are two types of programmed interrupts that can be exchanged: PT interrupts and PR interrupts.

The term PT stands for programmed interrupt to the transmitter adaptor. This programmed interrupt does not require the local adaptor to use the read/write resources of the interface cable to send a programmed interrupt to the other bus (the four cable interrupts can always be sent between the two buses and are not considered to be in the same category as reads and writes).

PT interrupts work as follows:

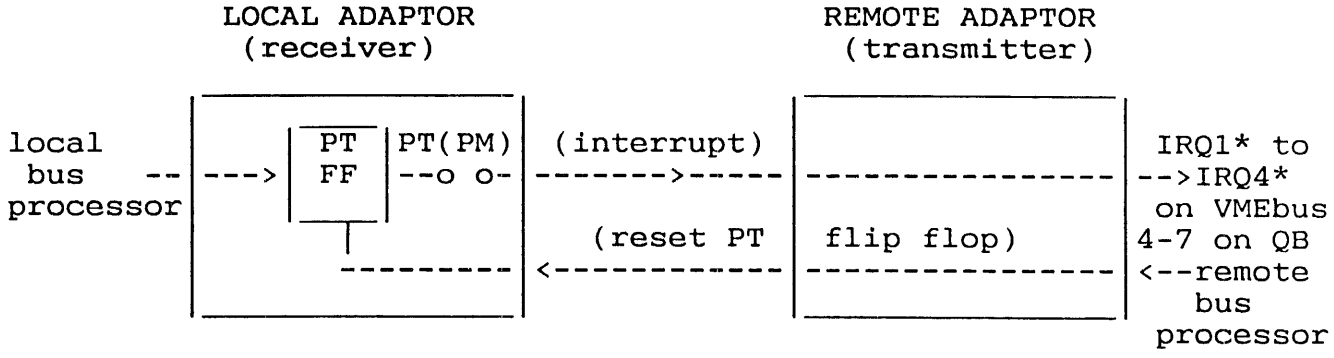


FIGURE 2 PT INTERRUPT

The pin at location PM in the interrupt jumper block area is a "0" when the PT flip flop in interrupt category 2 described above is active. This interrupt can be sent to the Q22bus over one of the four cable interrupt lines. The cable interrupt line selected to carry this PT interrupt back to the Q22bus adaptor cannot also be used to send a VMEbus IRQ line back to the Q22bus. Pin PM can be jumpered or wire wrapped to any of the four adaptor cable interrupt lines.

The programming sequence is:

1. A processor in the receiver chassis writes to the receiver adaptor card local node command register and sets the PT interrupt flip-flop on the receiver adaptor card in its chassis.

2. The PT interrupt flip-flop on the receiver adaptor card is jumpered to a line in the INT jumper block on the receiver adaptor which sends the PT interrupt back to the remote transmit chassis.

3. When the transmitter adaptor bus processor detects the PT interrupt, it clears the PT flip-flop by doing a remote write over the interface cable to the remote node command register on the receiver adaptor card.

The term PR stands for programmed interrupt to receive adaptor. This type of programmed interrupt does not require the receive adaptor to use the interface cable to reset a programmed interrupt from the transmit bus.

PR interrupts work as follows:

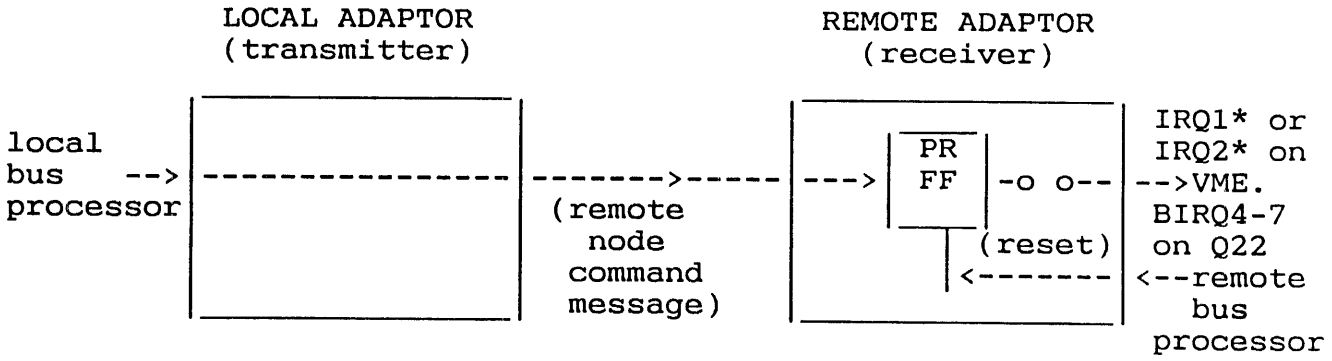


FIGURE 3 PR INTERRUPT

The programming sequence is:

1. A processor in the transmitter chassis writes over the interface cable to the receiver adaptor and sets the PR interrupt flip-flop on the receiver adaptor card.

2. The PR interrupt on the receiver adaptor card is jumpered to an interrupt line on the receiver bus backplane.

3. When the receiver bus processor detects the PR interrupt, it clears it by doing a local write to the adaptor card (the receiver card) in its chassis.

Pin 3 in the PS row of pins in the interrupt jumper block area is a "0" when the PR flip-flop in interrupt category 2 described above is being received by the VME adaptor card. This interrupt can be presented to the VMEbus as either IRQ1* or IRQ2*. To have the interrupt appear as IRQ1*, remove the jumper from pins 1 and 2 of the PS row of pins and place it on pins 2 and 3 of the same row. To have the interrupt appear as IRQ2*, remove the jumper from pins 1 and 2 of the bottom row of pins (the row containing the interface error interrupt pin) and wire wrap a wire from pin 2 in the same row to pin 3 in the PS row. If either IRQ1* or IRQ2* is used to present another type of interrupt to the VMEbus, the same interrupt line cannot also be used for the PR interrupt.

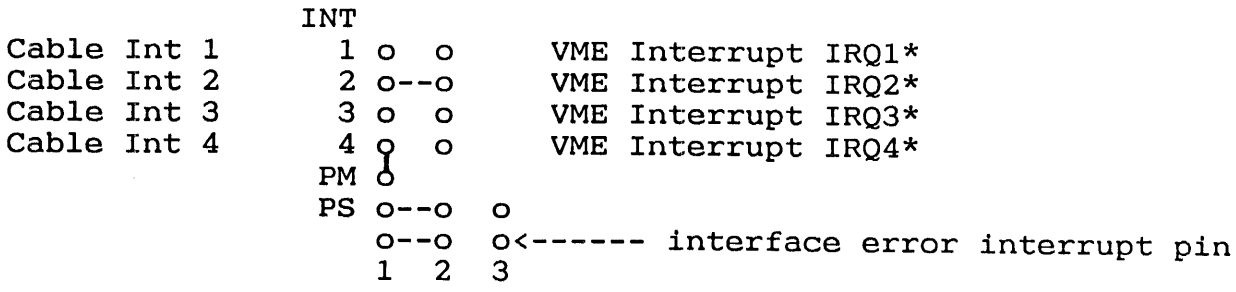
INTERFACE ERROR INTERRUPT

Interrupt category 3 described above (interface error interrupt) is presented to the VMEbus as either IRQ1* or IRQ2*. The

interface error interrupt pin is active when any of the two status error bits (timeout or parity error) are a "1". It is cleared with a "reset status errors" command and is not automatically cleared by a VME interrupt acknowledge. The interface error interrupt and status bit are meaningful if the adaptor card initiates communication over the interface cable to the other adaptor.

To have the interrupt appear as IRQ2*, remove the jumper from pins 1 and 2 of the bottom row of pins (the row containing the interface error interrupt pin) and place it on pins 2 and 3 of the same row. To have the interrupt appear as IRQ1*, remove the jumper from pins 1 and 2 of the PS row of pins and wire wrap a wire from the interface error interrupt pin to pin 2 in the PR row. If either IRQ1* or IRQ2* is used to present the interface error interrupt to the VMEbus, the same cable interrupt line cannot also be used to receive an interrupt from the Q22bus.

The following example shows a program generated interrupt from a VME processor card being sent to the Q22bus on VME level IRQ4* and IRQ2* backpanel interrupt being sent to the Q22 adaptor on VME level IRQ2*. The Q-bus interrupt level that it activates is selected by jumpers on the Q22 adaptor card.



EXAMPLE SETTING

THE VME ADAPTOR REM RAM HI and REM RAM LO JUMPERS

Locate the REM RAM HI and LO jumper block at location B8 on the VME adaptor card.

The REM RAM LO and HI (for remote bus RAM) jumper settings select the starting address and the address range that a VMEbus master will reference in its address space on the VMEbus when it wants to read from or write to the Q22bus. The REM RAM LO jumper block sets the starting VME address and the REM RAM HI selects the ending address. If the address range is translated to a different address range on the Q22bus (via the BIAS jumper settings on the Q22bus card), the VMEbus starting address should be an integral address multiple of the range selected, starting from address zero on the VMEbus. For example, if a 128 Kbyte

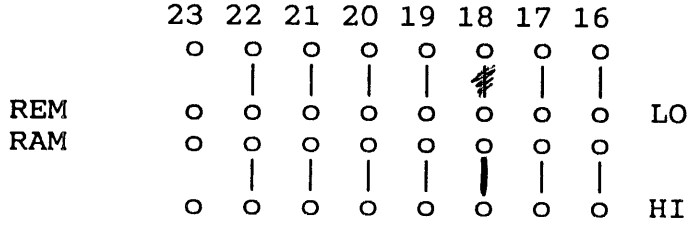
range is selected, the VME starting address should be set to a 128K boundary counting up from address zero on the VMEbus. The maximum possible setting for the range is 16 Mbytes, but a range greater than 4 Mbytes would not be useful since 4 Mbytes is the maximum range on the Q22bus. There cannot be any other VMEbus RAM in the same chassis at the addresses assigned for REMOTE BUS RAM since then there would then be two memories addressed at the same time and neither one could work properly.

Set the REM BUS RAM LO jumpers to the starting address of the first two digits of the 6 digit hex VME 24 bit address for the block of memory that you want mapped to the Q22bus. Assume that the remaining four digits of the hexidecimal address are all zeros. Set the REMOTE RAM HI jumpers to the first address after the end of the block of memory to be mapped to the Q22bus.

VMEbus address space equal to or greater than the REM RAM LO setting and less than the REM RAM HI setting is mapped to the Q22bus. If you do not want to use the REM BUS RAM function, set the REM RAM HI jumpers to a value less than the REM RAM LO value.

A jumper forms a logic "0" when it is installed (ON in the tables). It forms a logical "1" when it is removed (OFF in the tables).

The bit significance of the pins is shown below:



The jumpers are shown for the factory setting of 800000 for the LO address and 840000 for the HI address. With this setting any VMEbus memory reference using an address modifier of 39, 3A, 3D, or 3E and an address in the 256K range from 800000 through 83FFFF will be mapped to the Q22bus.

REMOTE BUS RAM FIRST DIGIT VALUE

A23	A22	A21	A20	VME REMOTE BUS RAM ADDRESS 1st DIGIT
ON	ON	ON	ON	0 hex
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

REMOTE BUS RAM SECOND DIGIT VALUE

A19	A18	A17	A16	VME REMOTE BUS RAM ADDRESS 2nd DIGIT
ON	ON	ON	ON	0 hex
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

THE VME ADAPTOR ADDRESS BIAS JUMPERS (ADD BIAS) AT LOCATION A2

When a bus master in the Q22bus chassis wants to reference memory in the VMEbus chassis, it does so by addressing within a window in Q22bus address space. The window is selected by the REM BUS RAM jumper settings on the Q22bus adaptor card. This address is convenient for the processor in the Q22bus chassis, but it may not be at the address that it wants to use in the VMEbus chassis.

The ADD BIAS jumpers permit you to offset the Q22bus address into a different address in VMEbus address space.

Be careful not to set the memory mapping jumpers such that a memory address from the first chassis that addresses in the second chassis would map through the second chassis and try to reappear again in the first chassis. This would cause an adaptor conflict and would not work.

NOTE: You can also use the adaptor cards in page mode where the upper eight VME address bits are supplied by an 8-bit address page register on the VME card. See FUNCTIONAL USE OF THE ADAPTOR.

When the Q22bus adaptor card addresses VMEbus RAM in the chassis containing the VME adaptor card, the lower sixteen Q22bus address lines are passed on "as is" to the VMEbus backpanel. This establishes the minimum contiguous block of VME addresses as 65 Kbytes in VMEbus memory. You can position this 65 Kbyte block anywhere in VMEbus address space so long as the VMEbus target address starts on a 65K boundary (from address zero). The jumpers give you three choices for the remaining eight higher VMEbus address lines:

1. You can set the destination VMEbus address bit to a "ZERO".

2. You can set the destination VMEbus address bit to a "ONE".

3. You can extend the VMEbus address range by connecting more Q22bus address bits to the VMEbus address.

The VME adaptor card is set at the factory to map a 256K VME address range from the Q22bus to start at address zero on the VMEbus. If you want to re-position the destination address in VMEbus memory so that it starts at an address other than zero, or if you want to map a larger or smaller block of memory to the VMEbus, you will have to change the jumpers.

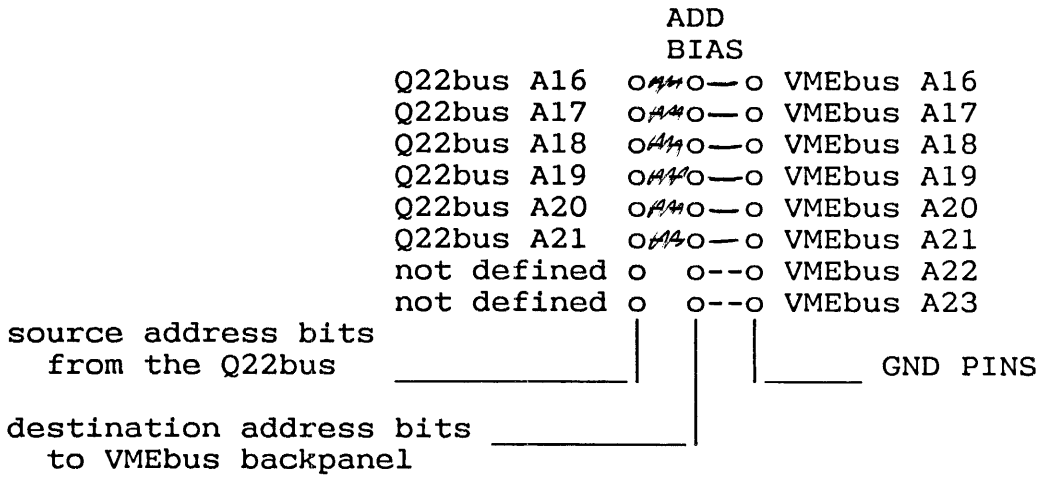
If you connect Q22bus address line 16 to VMEbus address line A16, you can address a 128K VMEbus block. Subsequently connecting A17, A18, A19, A20, and A21 from the Q22bus to address lines A17, A18, A19, A20, and A21 on the VME card permits extending the

range to 256K, 512K, 1MEG, 2MEG, and 4MEG.

Once the range has been established, the remaining higher VMEbus address bits must be jumpered to ground or left open to establish the starting address.

A bit left in the open position (i.e., not jumpered to ground or connected to a Q22bus address line) appears as a "ONE" bit in the VMEbus address.

A bit jumpered to one of the ground pins appears as a "ZERO" in the VMEbus address.



VME ADD BIAS JUMPER BLOCK AT LOCATION A2

NOTE: the jumper positions shown are for the factory jumper settings with the same address appearing on the VMEbus as is selected with the REM RAM jumpers on the Q-bus adaptor card.

The middle row of pins connect through a non-inverting buffer to drive the VMEbus address lines A16-A23. The right row of pins (by the address numbers) are all connected to ground. The left row of pins are the address bits received from the Q22bus chassis.

VME ADAPTOR DUAL PORT RAM JUMPER SETTINGS

The dual port RAM is an optional memory piggy back board that attaches to one of the adaptor cards. Only one dual port RAM card can be used at a time with the pair of adaptor cards. The RAM card should be added to the adaptor board which is normally a receiver, since the bus which holds the card can then directly access the dual port RAM without using the interface cable connecting the two adaptor cards. This leaves the interface cable free for use by the other chassis to access the dual port RAM or

to access devices on the bus holding the adaptor without concern for a possible cable interference situation. The VME adaptor still uses only one VME card slot after adding the dual port RAM card.

The dual port RAM looks to both systems as simply more RAM memory. The address of the dual port RAM is set by jumpers on both adaptor cards. The card can be set to respond to an address range in the VME system and to a different address range in the Q22bus system. The dual port RAM responds to VMEbus address modifier codes 39, 3A, 3D, or 3E.

The dual port RAM offers several advantages. First, there are some types of I/O cards that do not have on-board RAM but need some RAM, such as a DMA buffer, to perform their function. In that case, the dual port RAM can save the cost of purchasing another memory card. Second, a bus master can access the dual port RAM without using the other bus. This permits faster operation when reading and writing to the dual port RAM than is possible when reading and writing directly to the other bus, since a bus arbitration cycle to gain access to the other bus is not necessary. Third, use of the dual port RAM can conserve bus bandwidth since neither system ties up the other bus when it reads and writes to the dual port RAM. The dual port RAM can also be used as a common memory for interchange of information between processors in a multiprocessor environment. Fourth, as mentioned previously, adding the dual port RAM does not use another VMEbus slot. Unless the card-to-card spacing in the Q22bus card cage is 8/10 in., the dual port RAM card will require two card slots when it is mounted in the Q22bus card cage. Bit 3 has short bus grant continuity cards to be used if the dual port RAM card is mounted on the Q22 card.

Both systems can access the memory concurrently. The adaptor card housing the dual port RAM card arbitrates conflicts that occur if both systems try to use the memory at the same instant.

THE VME ADAPTOR PORT RAM HI and PORT RAM LO JUMPERS

Locate the PORT RAM HI and LO jumper block at location B5 on the VME adaptor card.

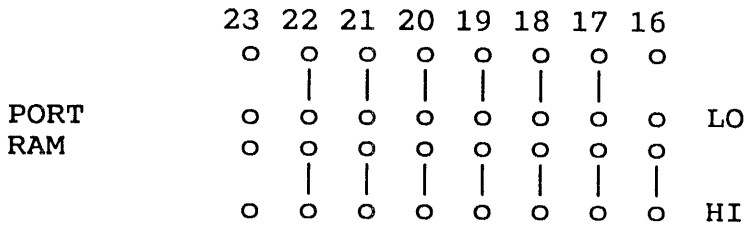
The PORT RAM LO and HI jumper settings select the starting address and the address range that a VME bus master in the VME chassis will reference when it wants to read or write to the dual port RAM. The PORT RAM LO jumper block sets the starting VME address and the PORT RAM HI selects the ending address. The minimum range is 65 Kbytes and the maximum range is 16 Mbytes. Set the range to match the size of your dual port memory. If the dual port memory is less than 65 Kbytes, set the range to 65K. There cannot be any other VMEbus RAM at the addresses assigned for dual port RAM since then there would then be two memories addressed at the same time and neither one could work properly.

Set the PORT RAM LO jumpers to the starting address of the first two digits of the six-digit hex VME 24-bit address for the block of memory that you want mapped to the dual port RAM. Assume that the remaining four digits of the hexidecimal address are all zeros. Set the PORT RAM HI jumpers to the first address after the end of the block of memory to be mapped to the dual port RAM.

VMEbus address space equal to or greater than the PORT RAM LO setting and less than the PORT RAM HI setting is mapped to the dual port RAM. If you do not want to use the dual port RAM function, set the PORT RAM HI jumpers to a value less than the PORT RAM LO value.

A jumper forms a logic "0" when it is installed (ON in the tables). It forms a logical "1" when it is removed (OFF in the tables).

The bit significance of the pins is shown below:



The jumpers are shown for the factory setting of 810000 for the LO address and 800000 for the HI address. With this setting the dual port RAM function is disabled since the HI value is less than the LO value.

PORT RAM FIRST DIGIT VALUE

A23	A22	A21	A20	VME PORT RAM ADDRESS 1st DIGIT
ON	ON	ON	ON	0 hex
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

PORT RAM SECOND DIGIT VALUE

A19	A18	A17	A16	VME PORT RAM ADDRESS 2nd DIGIT
ON	ON	ON	ON	0 hex
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

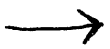
SETTING THE VME I/O ADDRESS RANGE

The "short address modifier codes" 29 and 2D are often used to identify a sixteen bit I/O address space on the VMEbus. Address modifier 29 is defined as short non-privileged access and address modifier 2D is defined as short Supervisory Access. There are two types of I/O operations that can be directed to the VME adaptor card from a VMEbus processor. First, there are the optional I/O commands that permit extended control of the adaptor through adaptor register reads and writes. Second, I/O reads and writes can be mapped through the adaptors to become I/O reads and writes on the Q22bus. The I/O SEL jumper block at location A/B 13 selects the I/O address range in VMEbus short I/O address space used for these two functions.

The 65 Kbyte I/O address range is divided into seven eight-Kbyte ranges, depending on the setting of the I/O SEL jumpers. A read or write within the selected 8K range with an address modifier code of 29 is passed to the Q22bus adaptor, where it becomes an I/O read or write at the same 8K address offset in the I/O page on the Q22bus system. A read or write within the selected 8K range with an address modifier code of 2D does not appear on the Q22bus chassis, but instead controls registers on the adaptor cards.

THE VME ADAPTOR I/O SELECT JUMPERS

Locate the I/O SEL jumper block at location A/B 13. This jumper block sets the I/O addresses of the VME adaptor card. VMEbus processor cards can perform I/O operations to the adaptor card to read status or control adaptor registers (see FUNCTIONAL USE OF THE ADAPTOR). Also, the VME chassis can perform I/O reads and writes on the Q22bus chassis. If your application does not use these features, it is possible to disable both functions by removing all of the jumpers from the I/O SEL jumper block.



```
I/O SEL
 o  o 15
 o  o 14    VME I/O disabled
 o  o 13
```

With no jumpers on, the card will not respond to the short address modifier codes and the I/O feature is disabled.

```
I/O SEL
 o--o 15
 o--o 14   VME I/O address is 0000-1FFF
 o--o 13
```

```
I/O SEL
 o--o 15
 o--o 14   VME I/O address is 2000-3FFF
 o  o 13
```

NOTE: This 2000-3FFF range is the factory setting.

```
I/O SEL
 o--o 15
 o  o 14   VME I/O address is 4000-5FFF
 o--o 13
```

```
I/O SEL
 o--o 15
 o  o 14   VME I/O address is 6000-7FFF
 o  o 13
```

```
I/O SEL
 o  o 15
 o--o 14   VME I/O address is 8000-9FFF
 o--o 13
```

```
I/O SEL
 o  o 15
 o--o 14   VME I/O address is A000-BFFF
 o  o 13
```

```
I/O SEL
 o  o 15
 o  o 14   VME I/O address is C000-DFFF
 o--o 13
```

OTHER VME ADAPTOR JUMPERS

The remaining jumpers on the VME adaptor at locations A/B 12 and D1 are preset at the factory and are not to be changed by the user.

VME ADAPTOR CARD FACTORY JUMPER SETTINGS

VMEbus REMOTE RAM ADDRESS (to Q-bus)	800000 - 840000
VMEbus ADDRESS OF PORT RAM	disabled
VMEbus RAM BIAS JUMPERS	4 Mbytes, same adr as Q-bus
VMEbus ADAPTOR VMEbus I/O ADDRESS	2000-3FFF, AM = 29 or 2D
VMEbus INTERRUPT JUMPERS	none
LEVEL 3 ARBITER	
DRIVES SYSCLK	
RECEIVER MODE	
USES DEFAULT ADDRESS MODIFIERS FROM Q22bus ADAPTOR	

THE 432 ADAPTOR Q22bus CARD JUMPERS (Q22bus CARD)

To properly set the jumpers on the Q22bus card, there is some configuration information that you must know about your Q22bus system.

Determine if there is a Q-bus processor card in your Q-bus chassis (the MicroVAX II processor acts like a Q-bus processor card). If there is no Q-bus processor card, the Bit 3 Q22bus adaptor can be jumpered to provide the bus arbitration and interrupt acknowledge functions normally provided by the Q-bus processor. When used in this mode (processor mode), the Q22bus adaptor must be placed in Q-bus card slot 1. The Q22bus adaptor does not have bus terminators which are sometimes provided by the Q-bus processor card. When using the card in processor mode, use a backplane that has terminator resistors or install a Q22 terminator resistor card in one of the card slots.

Usually there will be a Q-bus processor card in the Q-bus system, so it will not be necessary to use the Bit 3 Q22 card in processor mode. In that case, the Q22 adaptor can be installed in any quad card slot. It is necessary that the Q22 adaptor receive the bus grant and interrupt acknowledge signals from the processor card, so be sure that you have continuity cards in any unused card locations between the processor card and the Q22 adaptor card.

Locate the SYST jumper block at location C1 on the Q22bus board.

```
          1
      o   o     jumper if the card is used in  processor mode
      o   o     there should never be a jumper on these pins
      o--o      there should always be a jumper on these pins
      o   o     jumper if the card is used in processor mode
→     o—o       jumper if this card is a "transmitter" **
      o   o     Q-bus interrupt level select 0 ***
      o--o      Q-bus interrupt level select 1 ***
      o   o     jumper to word swap on VMEbus to Q-bus transfers *
      o   o     jumper to byte swap on VMEbus to Q-bus transfers *
      o   o     jumper to word swap on Q-bus to VMEbus transfers *
      o   o     jumper to byte swap on Q-bus to VMEbus transfers *
        T
        S
        Y
        S
```

* See the section on byte and word swapping

** The term "TRANSMITTER" means transmitter card, which sends commands to the RECEIVER card. It does not mean that the card is necessarily a Q22bus bus master.

*** This pair of jumpers selects which Q-bus interrupt level will

be activated when the Q22 adaptor card sends an interrupt to the Q-bus. The factory default setting is Q-bus interrupt level 5. The levels are selected per the following table:

Q-bus interrupt level 4 (BIRQ4)

```
Level 0 jumper  o--o  JUMPER ON
Level 1 jumper  o--o  JUMPER ON
```

Q-bus interrupt level 5 (BIRQ5)

```
Level 0 jumper  o  o  JUMPER OFF
Level 1 jumper  o--o  JUMPER ON
```

Q-bus interrupt level 6 (BIRQ6)

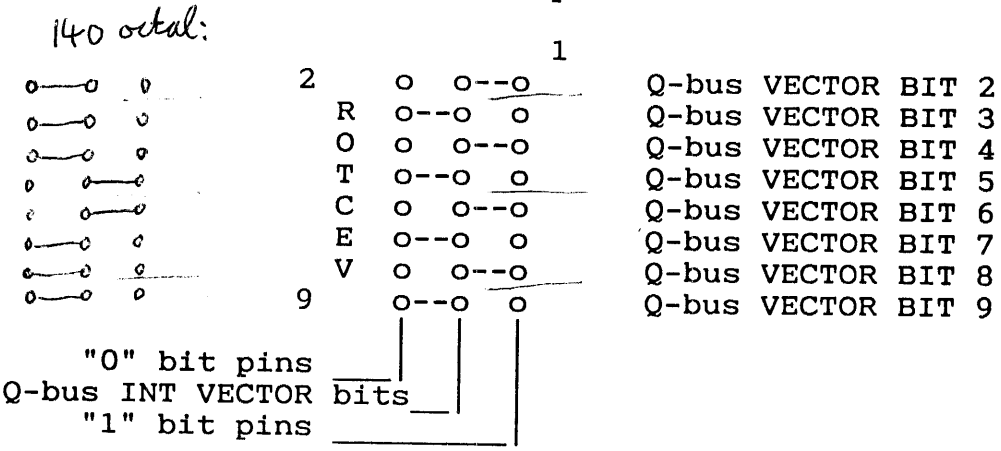
```
Level 0 jumper  o--o  JUMPER ON
Level 1 jumper  o  o  JUMPER OFF
```

Q-bus interrupt level 7 (BIRQ7)

```
Level 0 jumper  o  o  JUMPER OFF
Level 1 jumper  o  o  JUMPER OFF
```

ADDITIONAL Q22bus INTERRUPT JUMPERS (Q22bus CARD)

Locate the block of jumpers (VECTOR) at location D9 on the Q22bus card. This set of jumpers selects the interrupt vector transmitted on the Q-bus when the Q-bus processor acknowledges an interrupt from the Q22bus adaptor card.



Q-bus vector bits "0" and "1" are always zero. To make a vector bit a "0", place a jumper between the middle row pin for that bit and the corresponding "0" bit pin. To make a vector bit a "1", place a jumper between the middle row pin for that bit and the corresponding "1" bit pin.

The interrupt vector jumpers are shown for the factory default setting of Hex 154 (524 octal).

Locate the block of jumpers at location D1 on the Q22 adaptor card. This block is labeled RINT and is used for jumpering interrupts received from the VMEbus into Q-bus interrupts.

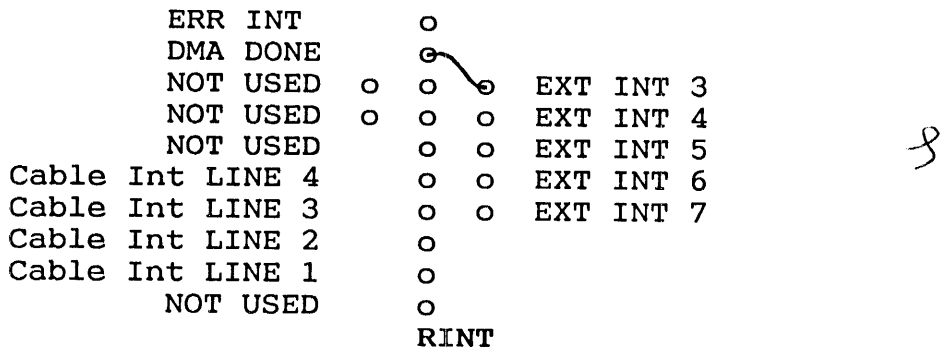
There are seven possible sources of interrupts from the Q22 adaptor card to the Q-bus. They are: (1) interface error interrupt, (2) DMA done interrupt, (3) the PR interrupt, programmed interrupt to receiver card, and (4) any one of the four possible interrupts sent from the VME adaptor card over the cable interrupt lines 1 - 4. An inactive to active transition of any of these interrupt sources can be captured by the Q22 adaptor card and will cause a Q-bus interrupt (BIRQ4, BIRQ5, BIRQ6, or BIRQ7, depending on the level jumpers in the SYST jumper block).

The Q-bus interrupt handler can determine the actual interrupt source by reading bits 9,10, and 11 in the CSR status register after the Q-bus interrupt acknowledge. The interrupt sources are priority encoded as follows:

PRIORITY LEVEL	INTERRUPT TYPE	CSR STATUS CODE BITS 11	10	9
0 (highest)	PR 0	0	0	0
1	PR 1	0	0	1
2	PR 2	0	1	0
3	EXT INT 3 (DMA DONE)	0	1	1
4	EXT INT 4	1	0	0
5	EXT INT 5	1	0	1
6	EXT INT 6	1	1	0
7 (lowest)	EXT INT 7	1	1	1

The PR interrupt does not have to be jumpered. It is hardwired to priority levels 0, 1, and 2. It is set when a VMEbus processor sets the PR flip-flop by writing a "1" to bit 5 in the Q22bus remote node command register. Along with setting the PR bit, the VMEbus processor must also set control bits 0 and 1 in the same register. If bit 0 is set, the PR interrupt flip-flop is interpreted as PR 1. If bit 1 is set, the PR interrupt is interpreted as PR 2. If neither bit 0 or bit 1 is set, the PR interrupt is interpreted as PR 0. After acknowledging the PR interrupt, the Q-bus processor can clear the PR flip-flop to inform the VMEbus processor that the requested Q-bus task has been completed. Note that only a "0" to "1" transition of the PR flip-flop will cause a Q-bus interrupt, so it is necessary for either the Q-bus processor or the VMEbus processor to clear it before it can cause another PR interrupt by setting it again.

The external interrupt sources are selected by jumpering or wire wrapping to the adjacent pins in the RINT jumper block that are possible sources for interrupts. Each interrupt is detected by the inactive-to-active transition of the interrupt source. If more than one interrupt source is active, the highest priority interrupt source will be acknowledged first, and the CSR status register will reflect the status for that source, but the Q-bus interrupt will remain active. When the interrupt is acknowledged a second time, the CSR status register will reflect the status for the next highest interrupt source. This will continue until all active interrupt sources have been acknowledged.



INTERFACE ERROR INTERRUPT

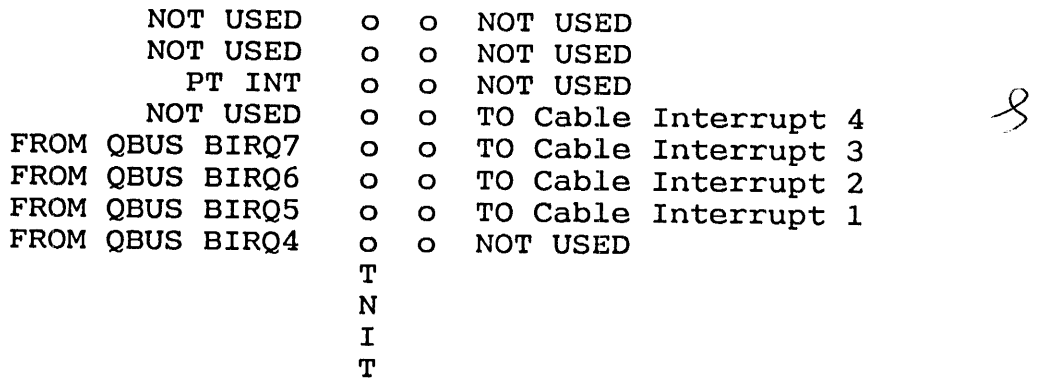
The ERR INT pin, interface error interrupt, is a "0" when any of the three status error bits (timeout, parity error, or BERR) are a "1". It is cleared with a "reset status error" command. Interface errors are only meaningful if the Q22bus adaptor card is the master and uses the I/O cable to send commands to the VME adaptor card. The ERR INT pin can be wire wrapped to any of the five external interrupt lines.

DMA DONE INTERRUPT

The DMA DONE interrupt pin is active if the interrupt enable DMA CSR bit is set and a block mode DMA operation has terminated, either successfully or unsuccessfully. It is cleared by a write to the Q22 adaptor card CSR register. The BIT 3 DMA DRIVER software for MicroVAX II applications expects to see the DMA DONE interrupt wired to external interrupt 3, as installed by the factory.

The other pins in the RINT jumper block are not used in the 432 adaptor configuration but are used in other adaptor applications that require this same Q22bus circuit card.

Locate the block of interrupt jumpers (TINT) at location K1 on the Q22bus card. This set of jumpers permits selection of Q22bus interrupt signals to send to the VMEbus.



Up to four interrupt lines are available to send interrupts from the Q-bus to the VMEbus. The four lines can be jumpered or wire wrapped to Q22bus interrupt source lines to select which Q22bus interrupts are sent to the VMEbus.

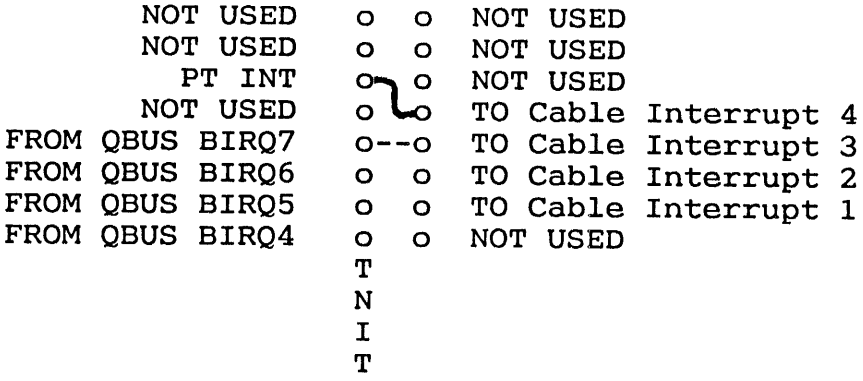
There are three types of interrupts that can be exchanged. See the section on VME adaptor card interrupt jumpers for a description of the three types of interrupts.

The TINT jumper block selects the sources of the three interrupt types.

Interrupts of type 1 (backpanel interrupts) are unique in that none of the four Q-bus interrupt lines BIRQ4-7 can be sent to the VMEbus if there is a Q-bus processor card in the Q-bus chassis. This is because the Q-bus processor card will acknowledge all interrupts on the Q-bus. Also, the Q-bus interrupt lines are encoded so that there is not a unique Q-bus interrupt line for each Q-bus interrupt. These interrupts should only be wired back to the VMEbus if the Q22 adaptor is being used in processor mode (see the section on the Q22 SYST jumper block). To send one of these four interrupt lines back to the VMEbus, wire wrap the Q-bus interrupt pin to one of the four interrupt lines that transmit to the VMEbus. Remove any jumpers that might be on the corresponding interrupt line pins on the VME adaptor card.

The pin at location PT in the interrupt jumper block area is a "0" when the PT interrupt flip-flop on the Q22bus adaptor card (type 2, programmed interrupts) has been set by a processor in the Q22bus chassis. This interrupt can be sent to the VMEbus over one of the four INT lines. The INT line selected to carry this interrupt to the VMEbus cannot also be used to send a Q22bus backpanel interrupt to the VMEbus. Pin PT can be wire wrapped to any of the four interrupt lines that carry interrupts back to the VMEbus.

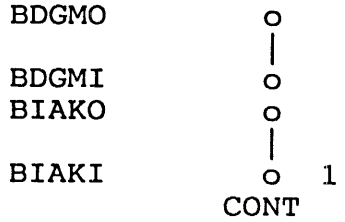
The following example shows Q22bus interrupt 7 sent to the VMEbus IRQ3 as well as a program generated interrupt (PT) from a Q22bus processor card sent to the VMEbus on line 4.



EXAMPLE SETTING

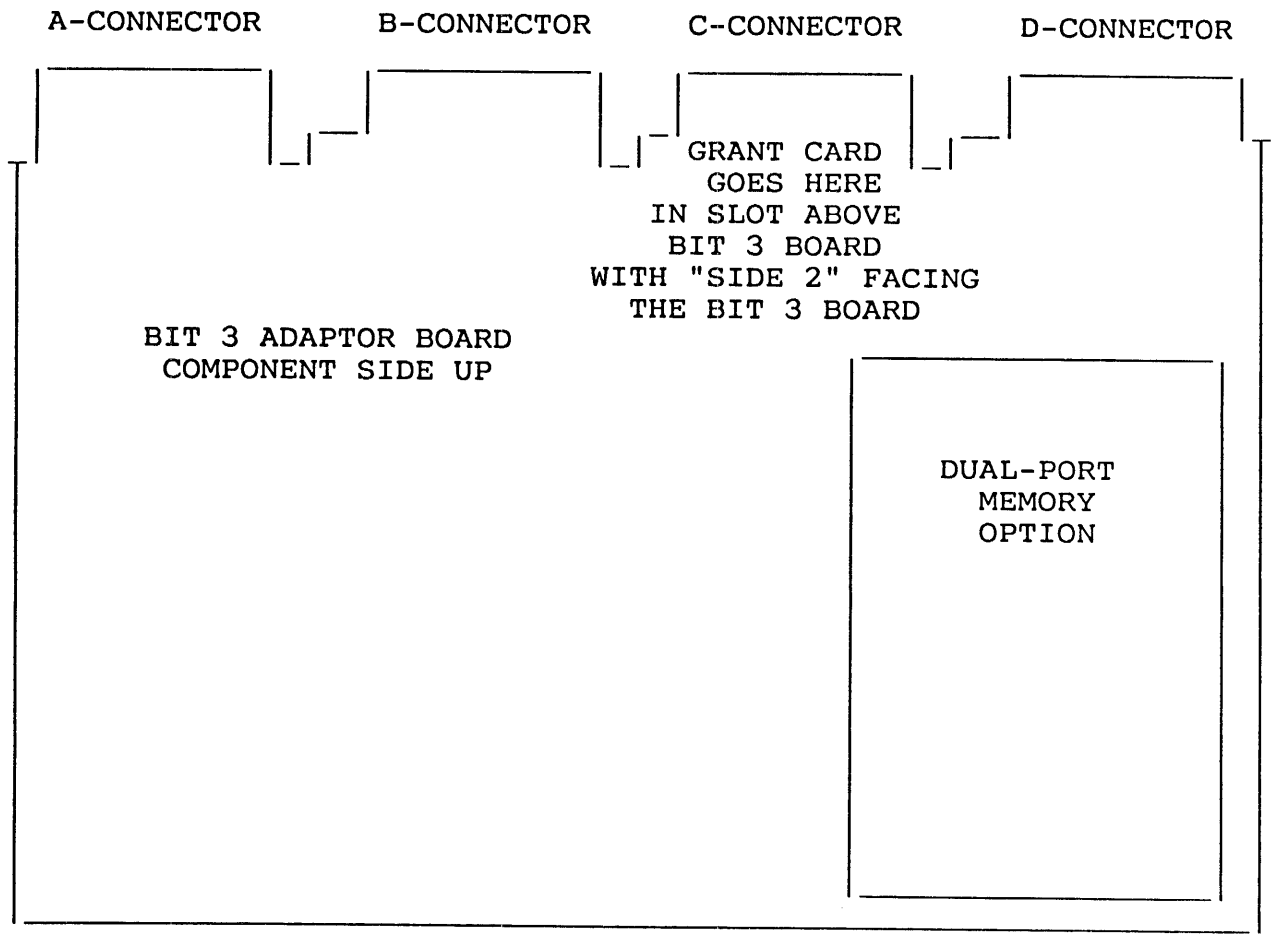
THE QBUS C/D ROW BUS GRANT AND INTERRUPT ACKNOWLEDGE CONTINUITY JUMPERS

Locate the CONT jumper block at location A8 on the Q22bus adaptor card. These two jumpers insure bus grant and interrupt acknowledge continuity for "downstream" cards on the C/D connectors of Q/Q type backplane slots. If the Q-bus backplane slot is a Q/CD-type, the jumpers should be removed. Either both jumpers are on or both jumpers are off. The factory setting is to have these jumpers installed.



USE OF BIT 3 Q-bus GRANT CONTINUITY CARD -- P/N 82602140

The BIT 3 Q-bus grant continuity card (model 400-801) is a short version of a standard DEC grant card, to be used with BIT 3 Q-bus adaptor boards with the Dual-Port memory option installed. The BIT 3 board requires the space of two Q-bus slots with the dual-port memory installed, and the short grant card allows passage of the bus grant (BDMGI/BDMGO) and interrupt acknowledge (BIAKI/BIAKO) signals on the C-connector of a Q/Q-type backplane slot. The grant card is not required on the C-connector of Q/CD-type backplane slots.



The A-connector and B-connector space in the slot above the BIT 3 board can be filled with a normal-size grant card or any normal dual-height Q-bus card.

THE Q22bus CARD REM RAM HI and REM RAM LO JUMPERS

Locate the REM RAM HI and LO jumper block at location B5 on the Q22bus adaptor card.

The REM RAM LO and HI (for remote bus RAM) jumper settings select the starting address and the address range that a Q22bus master will reference in its address space on the Q22bus when it wants to read or write to the VMEbus. The REM RAM LO jumper block sets the starting Q22bus address and the REM RAM HI selects the ending address. If the range is translated to a different address range on the VMEbus, the starting address should be an integral address multiple of the range selected, starting from address zero. For example, if a 128 Kbyte range is selected, the starting address should be set to a 128K boundary counting up from address zero. The maximum range is 4 megabytes. There cannot be any other Q22bus RAM in the same chassis at the addresses assigned for REM BUS RAM, since there would then be two memories addressed at the same time and neither could work properly.

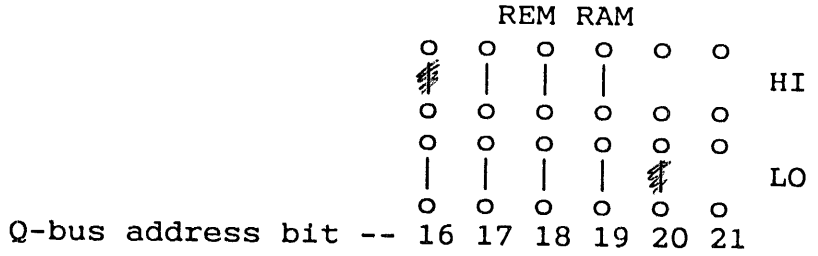
Q-bus address space in this manual is described using hexidecimal notation. An address in the 4 megabyte address range on the Q22bus can be described as a value between 000000 and 3FFFFF Hex.

Set the REM BUS RAM LO jumpers to the starting address of the first two digits of the 6-digit hex Q22bus 22-bit memory address for the block of memory to be mapped to the VMEbus. Assume that the remaining four digits of the hexidecimal address are all zeros. Set the REMOTE RAM HI jumpers to the first address after the end of the block of memory to be mapped to the VMEbus.

Q22bus address space equal to or greater than the REM RAM LO setting and less than the REM RAM HI setting is mapped to the VMEbus. If you do not want to use the REM BUS RAM function, set the REM RAM HI jumpers to a value less than the REM RAM LO value.

A jumper forms a logic "0" when it is installed (ON in the tables). It forms a logical "1" when it is removed (OFF in the tables).

The bit significance of the pins is shown below:



3 MB — 3 MB + 64 KB

The jumpers are shown for the factory setting of 200000 for the LO address and 300000 for the HI address. With this setting any Q22bus memory reference in the 1 megabyte range from 200000 through 2FFFFF will be mapped to the VMEbus.

REMOTE BUS RAM FIRST DIGIT VALUE

A21	A20	Q22bus REMOTE BUS RAM ADDRESS 1st DIGIT
ON	ON	0 hex
ON	OFF	1
OFF	ON	2
OFF	OFF	3

REMOTE BUS RAM SECOND DIGIT VALUE

A19	A18	A17	A16	Q22bus REMOTE BUS RAM ADDRESS 2nd DIGIT
ON	ON	ON	ON	0 hex
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

THE ADDRESS BIAS JUMPERS (BIAS) AT LOCATION B10 (Q22bus CARD)

When a VMEbus processor directly addresses memory in the Q22bus chassis, it does so by using an area in VME address space (REMOTE BUS RAM jumpers on the VME adaptor card) that you have selected. This address is convenient for the VMEbus, but might not be the same as the absolute address that the VME processor wants to use in Q22bus address space.

The ADD BIAS jumpers permit you to offset the VMEbus address into a different address in Q22bus address space.

Be careful not to set the memory mapping jumpers such that a memory address from the first chassis that addresses in the second chassis would map through the second chassis and try to reappear again in the first chassis. This would cause an adaptor conflict and would not work.

NOTE: You can also use the card in page mode where the upper six Q22bus address bits are supplied by an address page register on the Q22bus card. See FUNCTIONAL USE OF THE ADAPTOR.

When the VME device addresses Q22bus RAM, the lower sixteen VMEbus address lines are passed on "as is" to the Q22bus backpanel. This establishes the minimum contiguous block of VMEbus addresses as 65 Kbytes in Q22bus memory. (16 address bits = 65K). You can position this 65K block anywhere in Q22bus address space so long as the Q22bus target address starts on a 65K boundary (from address zero). The jumpers give you three choices for the remaining six high-order Q22bus address lines:

1. You can set the Q22bus address bit to a "ZERO".

2. You can set the Q22bus address bit to a "ONE".

3. You can extend the Q22bus address range by passing more VMEbus address bits to the Q22bus address.

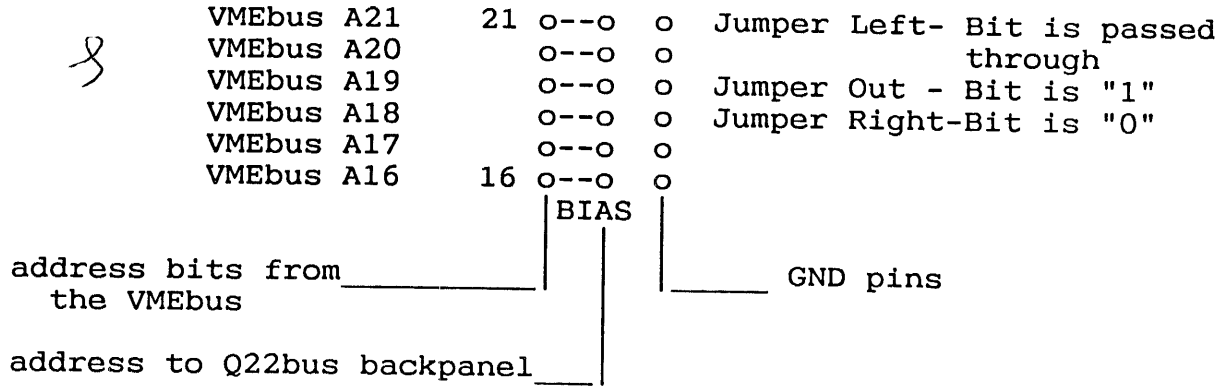
The Q22bus adaptor card is set at the factory to map to the same addresses on the Q-bus as are used on the VMEbus (VME address bits 22 and 23 are stripped off). If you want to re-position the address in Q22bus memory so that it starts at another address, you will have to change the jumpers.

If you connect VME address line A16 to Q22bus address line A16 you can address a 128K Q22bus block. Subsequently connecting VMEbus A17, A18, A19, A20, and A21 to Q22bus ADDRESS lines A17, A18, A19, A20, and A21 permits extending the range to 256K, 512K, 1MEG, 2MEG, and 4MEG.

Once the range has been established, the remaining higher Q22bus address bits must be jumpered to ground or left open to establish the starting address.

A bit left in the open position (i.e., not jumpered to ground or connected to a VMEbus address line) appears as a "ONE" bit in the Q22bus address.

A bit jumpered to one of the ground pins appears as a "zero" in the Q22bus address.



BIAS JUMPER BLOCK AT LOCATION B10

Note: The jumper positions shown are for factory jumper settings with all addresses from the VMEbus wired directly through to the same Q-bus addresses.

The middle row of pins connect through an inverting buffer to drive the Q22bus address lines A16-A21. The right row of pins are all connected to ground. The left row of pins are the adress bits received from the VMEbus.

THE Q22bus ADAPTOR CARD I/O SELECT JUMPERS

Locate the I/O jumper block at location B9. This jumper block is used to set the start address of the adaptor card in the I/O page. It is used when the Q-bus processor card wants to communicate with the 432 adaptor I/O registers. It is also used to map Q22bus I/O reads and writes into short I/O address space memory reads and writes on the VMEbus.

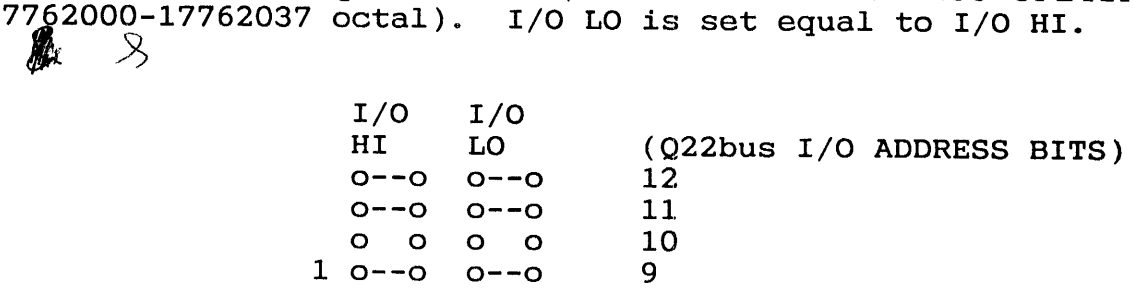
The Q-bus adaptor uses a minimum of 32 bytes in the I/O page. The first sixteen bytes are used to control the block mode DMA function. The next sixteen bytes are used for miscellaneous bus-to-bus communication control registers -- eight to communicate with the Q-bus adaptor card registers and the next eight to communicate with the VME adaptor card registers.

If the I/O HI address is set higher than the I/O LO address, then Q22bus I/O reads and writes to I/O page address space above I/O LO + 32 and less than the I/O HI jumper setting are converted into short I/O memory reads and writes on the VMEbus at the same

16-bit address on the VMEbus. The address modifier code presented to the VMEbus is 29.

The REMOTE I/O PAGE address range can be increased in 512 byte increments by setting the I/O HI jumper to a higher I/O page address than the I/O LO jumper.

The factory setting for the I/O address is 3FE400-3FE41F Hex (17762000-17762037 octal). I/O LO is set equal to I/O HI.



Q22bus CARD I/O RANGE JUMPERS

For the I/O LO start address, I/O page address bits 8,7,6,and 5 must be "0".

THE PORT RAM HI and LO ADDRESS JUMPERS (Q22bus CARD)

Locate the PORT RAM HI and LO jumpers at location B6.

The PORT RAM HI and LO jumpers select the starting address and the address range that a Q22bus master will reference in Q22bus address space when it wants to read or write to the DUAL PORT RAM. The PORT RAM LO jumper block sets the starting Q22bus address and the PORT RAM HI selects the ending address. The minimum range is 65 Kbytes and the maximum range is 4 Mbytes. Set the range to match the size of your DUAL PORT memory. If the DUAL PORT memory is less than 65 Kbytes, set the range to 65K.

Q-bus address space in this manual is described using hexidecimal notation. An address in the 4 Mbyte address range on the Q22bus can be described as a value between 000000 and 3F0000 Hex.

There cannot be any other Q22bus RAM at the addresses assigned for PORT RAM, since then there would then be two memories addressed at the same time and neither one could work properly.

Set the PORT RAM LO jumpers to the starting address of the first two digits of the six-digit hex Q22bus address for the block of memory to be mapped to the DUAL PORT memory. Assume that the remaining four digits of the hexidecimal address are all zeros. Set the PORT RAM HI jumpers to the first address after the end of the memory to be mapped to the DUAL PORT RAM.

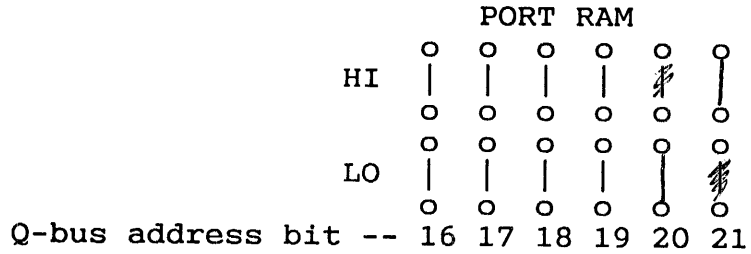
Q22bus address space equal to or greater than the PORT RAM LO setting and less than the PORT RAM HI setting is mapped to the

dual port memory. If you want to disable the PORT RAM function from the Q22bus, or if you do not install the PORT RAM option, set the PORT RAM HI jumpers to a value less than the PORT RAM LO jumpers. A DUAL PORT RAM on the Q22bus adaptor card cannot be accessed from the VMEbus through the REMOTE RAM address window on the VME card. To use the DUAL PORT RAM from the VMEbus, you must use the DUAL PORT RAM address window set on the VME adaptor card.

A jumper forms a logic "0" when it is installed (ON in the tables).

It forms a logical "1" when it is removed (OFF in the tables).

The bit significance of the pins is shown below:



The jumpers are shown for the factory setting of 100000 for the LO address and 200000 for the HI address. With this setting, the dual port RAM function occupies one megabyte of address space on the Q22bus from address 100000 through 1FFFFF.

PORT RAM FIRST DIGIT VALUE

A21	A20	Q22bus PORT RAM ADDRESS 1st DIGIT
ON	ON	0 hex
ON	OFF	1
OFF	ON	2
OFF	OFF	3

PORT RAM SECOND DIGIT VALUE

A19	A18	A17	A16	Q22bus PORT RAM ADDRESS 2nd DIGIT
ON	ON	ON	ON	0 hex
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

OTHER Q22bus ADAPTOR JUMPERS

The remaining jumpers (location H1) on the Q22bus adaptor are preset at the factory and are not to be changed by the user.

Q22bus ADAPTOR CARD FACTORY JUMPER SETTINGS

Q22bus REMOTE BUS RAM (to VME)	200000 - 300000 (Hex)
Q22bus ADDRESS OF DUAL PORT RAM	100000 - 200000 (Hex)
Q22bus ADDRESS BIAS (from VME)	PASS THRU (same addr as VME)
Q22bus ADAPTOR I/O ADDRESS	3FE400 - 3FE41F
Q22bus RINT JUMPERS	DMA DONE to EXT INT 3
Q22bus TINT JUMPERS	none
Q22bus BIRQ LEVEL	BIRQ5
Q22bus INTERRUPT VECTOR	154 (Hex) (524 Octal)
NO BYTE SWAP	
NO WORD SWAP	
NOT IN PROCESSOR MODE	
Q22bus card set to RECEIVER MODE	

FUNCTIONAL USE OF THE ADAPTOR

This section describes each of the adaptor card control and status registers. These registers are accessed through I/O address space selected by I/O range address jumpers on the cards.

The format of the register space is defined as follows:

The first eight bytes of the VME I/O space are used for a processor on the VME bus to talk to the adaptor card registers located on the VME adaptor card. These registers are called VME adaptor local node registers. The next eight bytes of the I/O space are used for a processor on the VMEbus to talk to the Q22 adaptor card registers. These registers are called Q22 adaptor remote node registers.

The first sixteen bytes of the Q22 I/O space are used for the Q-Bus processor card to control the block mode DMA function. The next eight bytes of the Q22 I/O space are used for a processor on the Q-Bus to talk to the adaptor card registers located on the Q-Bus adaptor card. These registers are called Q22 adaptor local node registers. The next eight bytes of the I/O space are used for a processor on the Q-Bus to talk to the VME adaptor card registers. These registers are called VME adaptor remote node registers.

THE Q22 ADAPTOR CARD DMA CONTROL REGISTERS

The first sixteen I/O addresses set in the Q-Bus I/O PAGE by the Q22 card I/O LO jumpers control the block mode memory to memory DMA function.

Q22 I/O ADDRESS	WRITE FUNCTION	READ FUNCTION
Q22 I/O LO + 0(Hex)	Q-bus DMA word count	Q-bus DMA word count
Q22 I/O LO + 2	Q-bus DMA addr & exten	Q-bus DMA addr & exten
Q22 I/O LO + 4	Q-bus CSR	Q-bus CSR
Q22 I/O LO + 6	-reserved-	-reserved-
Q22 I/O LO + 8	-reserved-	-reserved-
Q22 I/O LO + A	-reserved-	-reserved-
Q22 I/O LO + C	Cable DMA addr & exten	Cable DMA addr & exten
Q22 I/O LO + E	-reserved-	-reserved-

The Q22 adaptor I/O space contains some registers familiar to users of DEC Q-bus DMA interfaces, and has one additional address counter specific to the Bit 3 communication protocol. The CSR is also somewhat similar to the DEC DRV11-WA CSR, but is modified for the Bit 3 product.

Q-bus DMA Word Count Register -- This register is loaded in preparation for a DMA operation with the twos-complement of the number of words to be transferred. The register is sixteen bits wide (which allows up to 65,536 words of DMA), and increments once for every bus transfer operation. This register is only word-addressable.

Q-bus DMA Address Count Register and Extension -- This register is loaded in preparation for a DMA operation with the starting Q-bus address. For a DMA read operation, this will be the address to which data from the Q22 adaptor interface will be sent (the target address); for a DMA write operation, this will be the address from which data will be taken by the interface (the source address). The register is twenty-two bits wide, and is loaded as follows: the first write to the register forces counter bit 00 to a zero, and counter bits 15-01 are loaded with the corresponding bits of the data field. The next write to the same register loads counter bits 21-16 (the counter extension) with bits 05-00 of the data field, and the rest of the data field is ignored. (Address bit 00 is forced to a zero because DMA operations are only permitted on word boundaries.) The register is read in the same fashion: the first read will produce address bits 15-00; the next read will give address bits 21-16 in the lower-order six bits of the data field, and the rest of the data field is ignored. The counter increments by two for each bus transfer operation. This register is only word-addressable.

Cable DMA Address Count Register and Extension -- This register is loaded in preparation for a DMA operation with the starting cable address. (A "cable address" is the starting Q-bus address of the remote bus' RAM or dual port RAM for the adaptor card at the other end of the cable.) For a DMA read operation, this will be the address from which data will be taken by the interface (the source address); for a DMA write operation, this will be the address to which data from the Q22 adaptor interface will be sent (the target address). The register is twenty-four bits wide, and is loaded as follows: the first write to the register forces counter bit 00 to a zero, and counter bits 15-01 are loaded with the corresponding bits of the data field. The next write to the same register loads counter bits 23-16 (the counter extension) with bits 07-00 of the data field, and the rest of the data field is ignored. (Address bit 00 is forced to a zero because DMA operations are permitted only on word boundaries.) The register is read in the same fashion: the first read will produce address bits 15-00; the next read will give address bits 23-16 in the lower-order eight bits of the data field, and the rest of the data field is ignored. The counter increments by two for each bus transfer operation. This register is only word-addressable.

' VME

Q-bus CSR -- The Q-bus CSR, or control and status register, is a collection of single bits used primarily to run and monitor DMA operations. The bits are defined as follows:

```
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
ERR NEX  --  MNT ST2 ST1 ST0  --  RDY IEN  --  --  MEM RST R-W  GO
```

15 ERR R/O Error -- set by a DMA error; cleared by RST.

14 NEX R/O Non-Existent Memory -- set by a DMA access to non-existent or unmapped memory; cleared by RST. Sets the ERR bit.

13 --- --- UNUSED

12 MNT R/W Maintenance bit -- set only by a direct I/O write to the bit; cleared by same. No other function.

11 ST2 R/O
10 ST1
09 ST0

Status field -- these three bits reflect the status of any interrupt sent from the remote bus. The status may be read once the Q-bus is interrupted, and is interpreted as follows:

2 1 0		
0 0 0	Normal programmed int to receiver (PR 0)	
0 0 1	Programmed interrupt to receiver; (PR 1)	
0 1 0	Programmed interrupt to receiver; (PR 2)	
0 1 1	External interrupt 3 -- (DMA DONE)	
1 0 0	External interrupt 4	Remote interrupts as chosen on the RINT jumper pads
1 0 1	External interrupt 5	
1 1 0	External interrupt 6	
1 1 1	External interrupt 7 --	

08 --- --- UNUSED

07 RDY R/O Ready -- indicates that the Q22 adaptor is ready for another operation. Set by WORD COUNT DONE, ERR, or RST; cleared by GO.

06 IEN R/W Interrupt Enable -- allows the DMA DONE interrupt to occur on the Q-bus. Set by I/O access; cleared by same or by RST.

05 --- --- UNUSED
04 --- --- UNUSED

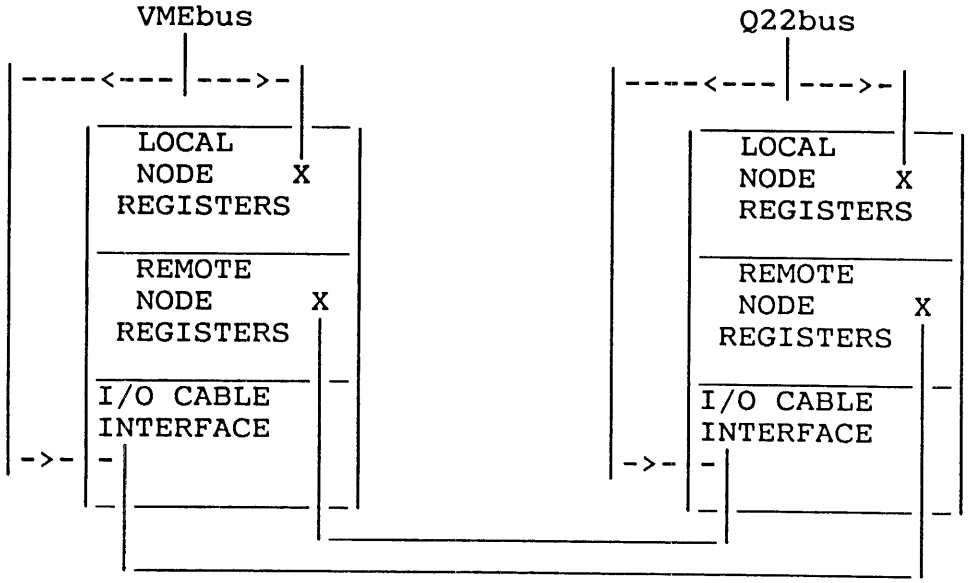
03 MEM R/W DMA Memory -- selects the type of remote memory to be accessed during DMA.
1 = Remote dual-port memory
0 = Remote RAM
Set by I/O access; cleared by same or by RST.

02	RST	W/O	Q-bus I/O Register Reset (Q22 adaptor INIT) -- resets the I/O bits noted and the Q-bus Word Count and Address Count Registers. One-shot write; reads as zero.
01	R-W	R/W	DMA Read/Write Flag -- signals direction of the DMA operation. 1 = DMA Read - read cable, then write Q-bus. 0 = DMA Write - read Q-bus, then write cable. Set by I/O access; cleared by same or by RST.
00	GO	W/O	DMA Go -- starts DMA operation. One-shot write; reads as zero.

KEY: R/O: Read-only bit
R/W: Read or write bit
W/O: Write-only bit

NODE CONTROL REGISTERS

Each adaptor card has a block of eight local node registers and a block of eight remote node registers. Local node registers are controlled by processors on the local bus. Remote node registers are controlled by processors on the remote bus.



A VME processor card addresses the VME and Q22bus adaptor card node registers with VME reads and writes using an address modifier 2D and an address within the 8 Kbyte field selected by the I/O SEL jumpers on the VME adaptor card. Within the 8 Kbyte I/O SEL field, only the first sixteen bytes are needed for adaptor control. Of these, the first eight I/O addresses control registers located on the Bit 3 adaptor card in the local VME chassis and the next eight I/O addresses are passed through the local VME adaptor card to the Q22bus card in the remote Q22bus.

A Q22bus processor card addresses VME and Q22bus adaptor card node registers with I/O reads and writes by addressing within the second sixteen byte address range (node control registers) selected by the Q22bus I/O LO jumper setting. The first eight of these I/O addresses control registers located on the Q22 adaptor card and the next eight I/O addresses are passed through the local Q22bus adaptor card to the VME card in the remote VMEbus.

REMEMBER THAT AN ADAPTOR CARD MUST HAVE ITS TRANSMITTER JUMPER IN THE SYS JUMPER BLOCK INSTALLED IN ORDER TO COMMUNICATE WITH THE REMOTE BUS OR WITH THE REMOTE NODE ADAPTOR REGISTERS.

VME ADAPTOR CARD LOCAL NODE REGISTERS

These registers are addressed by processors on the VMEbus.

The VME adaptor LOCAL NODE registers are:

VME I/O SEL ADDRESS	I/O WRITE FUNCTION	I/O READ FUNCTION
VME I/O SEL + 0	reserved	reserved
VME I/O SEL + 1	LOCAL NODE COMMAND REG	reserved
VME I/O SEL + 2	reserved	reserved
VME I/O SEL + 3	reserved	LOCAL NODE STATUS REG
VME I/O SEL + 4	reserved	reserved
VME I/O SEL + 5	reserved	reserved
VME I/O SEL + 6	reserved	reserved
VME I/O SEL + 7	reserved	reserved

LOCAL NODE COMMAND REGISTER -write only (located on VME adaptor card)

BIT	FUNCTION
7 ---	"1" = reset local status reg error bits
6 ---	"1" = clear PR interrupt flip-flop on VME card
5 ---	"1" = set PT interrupt flip-flop on VME card
4 ---	to be defined -- must be 0
3 ---	to be defined -- must be 0
2 ---	to be defined -- must be 0
1 ---	to be defined -- must be 0
0 ---	to be defined -- must be 0

LOCAL NODE STATUS REGISTER -read only (located on VME adaptor card)

BIT	FUNCTION
7	"1" = interface parity error
6	reserved for future use
5	"1" = PR interrupt flip-flop on VME card is set
4	always a "1"
3	reserved for future use
2	"1" = interface timeout occurred
1	"1" = PT interrupt flip-flop on VME card is set
0	"1" = remote Q22bus chassis powered down or the I/O cable is disconnected

The LOCAL NODE VME COMMAND REGISTER

RESET STATUS REGISTER ERRORS (BIT 7)

Communication between the two systems is monitored for various errors. Errors detected are I/O cable parity errors and interface timeouts (if the Q22bus system takes too long to respond).

An occurrence of any of these errors sets the corresponding bit in the LOCAL VME STATUS REGISTER. The error bit flip-flop stays set until it is cleared by writing to the LOCAL NODE VME COMMAND REGISTER with BIT 7 set to a "1".

CLEAR PR INTERRUPT (BIT 6)

Writing a "1" to bit 6 in the LOCAL NODE VME COMMAND REGISTER clears the PR interrupt flip-flop on the VME adaptor card.

SET PT INTERRUPT (BIT 5)

Writing a "1" to bit 5 in the LOCAL NODE VME COMMAND REGISTER sets the PT flip-flop on the VME adaptor card.

The LOCAL NODE VME STATUS REGISTER

LOCAL NODE VME STATUS REGISTER bit 7 is a "1" if a interface parity error or timeout has occurred.

LOCAL NODE VME STATUS REGISTER bit 5 is a "1" when the PR interrupt flip flop on the VME adaptor card is set.

LOCAL NODE VME STATUS REGISTER bit 2 is a "1" if an interface timeout occurred. The adaptor waits 1 millisecond for a response to a read or write command on the Q22bus. If the the other adaptor cannot complete the read or write within 1 millisecond the interface timeout status bit is set and the operation is terminated.

LOCAL NODE VME STATUS REGISTER bit 1 is a "1" when the PT flip flop on the VME adaptor card is set.

LOCAL NODE VME STATUS REGISTER bit 0 is a "1" if power is off at the Q22bus chassis or if the I/O cable is not connected. If this bit is a "1" there is no point in trying to communicate with the Q22bus since only timeout status errors will result.

VME ADAPTOR CARD REMOTE NODE REGISTERS

The VME adaptor card REMOTE NODE registers are controlled by a processor on the Q22bus. The REMOTE NODE registers are:

Q22 I/O LO ADDRESS	I/O WRITE FUNCTION	I/O READ FUNCTION
Q22 I/O LO + 18(Hex)	VME CARD COMMAND REG	VME CARD STATUS REG
Q22 I/O LO + 19	reserved	reserved
Q22 I/O LO + 1A	VME CARD ADDR PAGE REG	reserved
Q22 I/O LO + 1B	reserved	reserved
Q22 I/O LO + 1C	reserved	reserved
Q22 I/O LO + 1D	VME ADDR MODIFIER REG	reserved
Q22 I/O LO + 1E	reserved	IACK READ REG
Q22 I/O LO + 1F	reserved	IACK READ REG

VME CARD REMOTE NODE ADAPTOR COMMAND REGISTER - write only

BIT	FUNCTION
7	-- "1" = reset VMEbus (one shot, allow 1 sec)
6	-- "1" = clear PT interrupt FF on VME card
5	-- "1" = set PR interrupt FF on VME card "0" = no action
4	-- "1" = LOCK VMEbus BUS "0" = return to RWD mode
3	-- "1" = use address page register "0" = use address bias jumpers
2	-- VME IACK ADD3
1	-- VME IACK ADD2
0	-- VME IACK ADD1

VME CARD REMOTE NODE STATUS REGISTER -read only

BIT	FUNCTION
7 -------	reserved for future use
6 -------	reserved for future use
5 -------	"1" =PR interrupt FF on VME card is set
4 -------	"1" =LOCK VME BUS not set (this is the inverted state of the lock bus flip flop)
3 -------	"1" = USE ADDRESS PAGE REGISTER is selected
2 -------	reserved for future use
1 -------	"1" = PT interrupt FF on VME card is set
0 -------	always "0"

The VME CARD REMOTE NODE COMMAND REGISTER

These registers are located on the VME adaptor card and are controlled by the Q22bus system.

RESET VME BUS (BIT 7)

The VME adaptor card has a power on reset circuit that resets the VMEbus and the adaptor card when power is applied to the VME chassis. The time duration of the reset is normally 500 milliseconds. This reset circuit also can be activated on the remote adaptor by writing to the REMOTE NODE VME COMMAND REGISTER with bit 7 set to a "1". After triggering the reset, your program should wait about a second before starting another VME operation.

RESET PT INTERRUPT (BIT 6)

Writing a "1" to bit 6 of the remote node command register clears the PT flip flop on the VME adaptor.

SET PR INTERRUPT (BIT 5)

Writing a "1" to bit 5 of the remote node command register sets the PR flip flop on the VME adaptor.

LOCK VME BUS (BIT 4)

Writing a "1" to bit 4 in the remote node command register sets the LOCK BUS flip flop on the adaptor. Once the VME adaptor has been granted use of the VMEbus from the bus arbiter in the VMEbus system, it normally executes its VME cycle and immediately releases the bus for some other master to use (RWD mode). If the BUS LOCK flip flop is set, the VME adaptor will not release the bus after the read or write. This is useful in in a multiprocessor VME environment, it is common for processors to signal availability of a resource through an indivisible read-modify-write semaphore operation. The BUS LOCK feature permits the Q22bus system to keep the VME bus locked through a memory read followed by a memory write cycle. The bus can then be unlocked when the lock flip flop is cleared by the Q22bus

processor and other local VME processors can examine the semaphore using the read-modify-write instructions.

USE ADDRESS PAGE REGISTER (BIT 3)

The Q22bus system can address the remote VMEbus through either of two techniques:

(1) direct mode

(2) address page register mode

In the standard direct addressing mode, VMEbus RAM is addressed from the Q22bus by setting an address space window in the Q22bus address space as large as the block of VMEbus RAM to be addressed. For example, if you wanted to address 128 Kbytes of memory in the VMEbus, you would set the REM BUS RAM jumpers on the Q22bus card for a 128 Kbyte window. Page mode addressing is different in that it permits addressing all VMEbus RAM locations through a 65 Kbyte window in Q22bus address space. The upper eight address bits of the VMEbus address are set by an 8-bit page register located on the VME adaptor card. The remaining 16 lower VMEbus address bits are provided by the address offset in the local 65 Kbyte Q22bus RAM window. In page mode, the ADDRESS BIAS JUMPERS are bypassed and the upper eight address bits are provided by the address page register. It is possible to use both modes and switch between them under program control. This provides the capability to address outside of the normal windows or to execute short I/O instructions under program control of the PAGE MODE FLIP FLOP, the PAGE REGISTER, and the ADDRESS MODIFIER REGISTER. Page mode is selected when the page mode bit (bit 3) in the remote command register is set.

THE IACK CODE BITS (BITS 2,1,0)

A Q22bus processor can act as a local VMEbus interrupt handler and perform a IACK cycle on the VMEbus. The three VMEbus address lines that determine which VME interrupt is being acknowledged during a IACK READ cycle on the VMEbus are drawn from the IACK CODE BITS (bits 0-2) in the REMOTE NODE VME COMMAND REGISTER.

If the VME adaptor card is presenting an active interrupt on the VMEbus, it responds to an IACK cycle from another VMEbus processor with a vector of FFFF (hex).

The VME CARD REMOTE NODE STATUS REGISTER

REMOTE VME STATUS REGISTER bit 5 is a "1" if the PR flip flop on the VME adaptor card is set.

REMOTE VME STATUS REGISTER bit 4 shows the inverted state of the LOCK BUS flip flop controlled by BIT 4 in the REMOTE NODE VME COMMAND REGISTER.

REMOTE VME STATUS REGISTER bit 3 shows the state of the USE ADDRESS PAGE REGISTER flip flop controlled by BIT 3 in the REMOTE NODE VME COMMAND REGISTER.

REMOTE VME STATUS REGISTER bit 1 shows the state of the PT flip flop on the VME card.

VME ADDRESS PAGE REGISTER -write only

This register is gated to the VME address bus on Q22bus-VME cycles when the USE ADDRESS PAGE REGISTER command bit in the REMOTE NODE VME COMMAND REGISTER is set.

BIT	FUNCTION
7	VME ADDRESS BIT 23
6	VME ADDRESS BIT 22
5	VME ADDRESS BIT 21
4	VME ADDRESS BIT 20
3	VME ADDRESS BIT 19
2	VME ADDRESS BIT 18
1	VME ADDRESS BIT 17
0	VME ADDRESS BIT 16

VME ADDRESS MODIFIER REGISTER - write only

The VMEbus uses a 6-bit address modifier code in conjunction with the VME address bus to identify classes of data transfers. A common code is 3D for standard 24-bit supervisory data access and 2D for short supervisory (I/O) access, but there are several other classes defined for VMEbus devices. VMEbus devices must receive the expected address modifier code as well as the correct address or they will not respond. The ADDRESS MODIFIER REGISTER can be loaded by the Q22bus system and presented as the address modifier code on Q22bus-VME cycles.

Jumper position 1 in the VME adaptor card SYS jumper block selects the source of the address modifier code on reads and writes from the Q22bus to the VMEbus. The VME address modifier register provides the address modifier code if the jumper is not installed. In this case, a Q22bus processor card must load the register with the desired address modifier before performing reads and writes on the VMEbus. If the jumper is installed, the address modifier does not come from the address modifier register but instead comes from the default values that the Q22bus adaptor card sends. The Q22bus adaptor card default address modifier values are 3D for remote bus RAM reads and writes, and 29 for I/O

reads and writes.

BIT	FUNCTION
7	not used
6	not used
5	VME ADDRESS MODIFIER BIT 5
4	VME ADDRESS MODIFIER BIT 4
3	VME ADDRESS MODIFIER BIT 3
2	VME ADDRESS MODIFIER BIT 2
1	VME ADDRESS MODIFIER BIT 1
0	VME ADDRESS MODIFIER BIT 0

THE IACK READ REGISTER -read only

A Q22bus processor can instruct the VME adaptor card to perform an interrupt acknowledge cycle on the VMEbus. A Q22bus processor card does this by reading from the VME ADAPTOR CARD IACK READ REGISTER. The VME adaptor converts a read of this register address into an interrupt acknowledge cycle on the VMEbus. The VME interrupt vector is returned to the Q22bus processor as data from the read. The three-bit interrupt level address that must be presented on the VME address bus during the IACK cycle comes from the three IACK CODE bits in the REMOTE NODE VME COMMAND REGISTER.

If a VME processor card initiates an interrupt acknowledge cycle in response to an interrupt presented to the VMEbus by the VME adaptor card, the VME adaptor card responds to the interrupt acknowledge cycle on the VMEbus with a vector of FFFF.

Q22bus ADAPTOR CARD LOCAL NODE REGISTERS

These registers are located on the Q22bus adaptor card and are addressed by processors on the Q22bus.

Q22bus I/O LO ADD	I/O WRITE FUNCTION	I/O READ FUNCTION
Q22 I/O LO + 10(Hex)	Q22bus COMMAND REG	Q22bus COMMAND REG
Q22 I/O LO + 11	Q22bus CMD REG EXTENSION	Q22bus CMD REG EXT
Q22 I/O LO + 12	reserved	LOCAL NODE STATUS
Q22 I/O LO + 13	reserved	reserved
Q22 I/O LO + 14	reserved	HANDSHAKE MODE DATA
Q22 I/O LO + 15	reserved	HANDSHAKE MODE DATA
Q22 I/O LO + 16	ADDRESS PAGE REGISTER	reserved
Q22 I/O LO + 17	reserved	reserved

The I/O registers addressed from a Q22bus processor card are:

Q22bus LOCAL NODE COMMAND REGISTER (write/read register)

BIT		FUNCTION
7 ---	"1" =	clear status register errors
6 ---	"1" =	clear PR interrupt FF on Q22bus card
5 ---		not defined - must be 0
4 ---		not defined - must be 0
3 ---	"1" =	byte swap on Q22bus to VMEbus or Q22bus to dual port RAM transfers
2 ---	"1" =	word swap on Q22bus to VMEbus or Q22bus to dual port RAM transfers
1 ---	"1" =	set PT interrupt FF on Q22bus card
0 ---		not defined - must be 0

Following is a description of each of the bits in the Q22bus card LOCAL NODE COMMAND REGISTER:

CLEAR STATUS REGISTER ERRORS (BIT 7)

Communication between the two systems is monitored for various errors. Errors detected are: (1) I/O cable parity errors, (2) interface timeouts (if the VMEbus system takes too long to respond), and (3) if the VMEbus system responds to a Q22bus-VMEbus transfer with a BERR* instead of a DTACK*.

An occurrence of any of these errors sets the corresponding bit in the LOCAL NODE Q22bus STATUS REGISTER. The error bit flip flop stays set until it is cleared by writing to the LOCAL node Q22bus COMMAND REGISTER with BIT 7 set to a "1".

CLEAR PR INTERRUPT (BIT 6)

Writing a "1" to bit 6 in the Q22bus LOCAL NODE COMMAND REGISTER clears the PR interrupt flip flop on the Q22bus

adaptor card.

BYTE SWAP ON Q22bus to VMEbus or Q22bus to DUAL PORT RAM TRANSFERS (BIT 3)

If this bit is set to a "1", the least significant byte (data bits 0-7 on the Q22bus) is routed to VMEbus data bits 8-15. Also the most significant byte (bits 8-15 on the Q22bus) is routed to VMEbus data bits 0-7. The same effect can be accomplished by adding a jumper in the Q22bus adaptor card SYST jumper block. Use the jumper if you want byte swap always enabled. Use the byte swap control bit if you want to switch between swapped and non-swapped modes.

WORD SWAP ON Q22bus to VMEbus or Q22bus to DUAL PORT RAM TRANSFERS (BIT 2)

If this bit is set to a "1", address bit A1 from the Q22bus is inverted on transfers to the VMEbus or to the DUAL PORT RAM. The same effect can be accomplished by adding a jumper in the Q22bus adaptor card SYST jumper block. Use the jumper if you want word swap always enabled. Use the word swap control bit if you want to switch between swapped and non-swapped modes.

SET PT INTERRUPT (BIT 1)

Writing a "1" to bit 5 in the Q22bus LOCAL NODE COMMAND REGISTER sets the PT flip-flop on the Q22bus adaptor card.

Q22bus COMMAND REGISTER EXTENSION (write/read register)

BIT		FUNCTION
7 ---	"1" =	Handshake mode READ/WRITE DONE (read only bit)
6 ---		not defined - must be 0
5 ---		Q-Bus read byte select bit 1
4 ---		Q-Bus read byte select bit 0
3 ---		not defined - must be 0
2 ---		not defined - must be 0
1 ---		not defined - must be 0
0 ---	"1" =	Select HANDSHAKE MODE, 0 = DESELECT

Following is a description of each of the bits in the Q22bus card LOCAL NODE COMMAND REGISTER EXTENSION:

SELECT HANDSHAKE MODE (BIT 1)

Q-Bus operations are monitored by the Q-Bus processor to ensure that no Q-Bus read or write takes longer than about 12 microseconds. If the Q-Bus device does not respond within 12 microseconds, the Q-Bus processor times out and a machine check results. This 12-microsecond time is normally much longer than the round-trip time from the Q-Bus to the VMEbus, so the timeouts should not normally occur. However, if the Q-Bus processor

wants to talk to very slow VME devices, timeouts might occur.

Handshake mode provides a means for the Q-Bus processor to communicate with very slow VME devices. When the handshake mode bit is set, the Q22 adaptor always responds immediately with a reply to the Q-Bus without waiting for a reply from the VMEbus. This circumvents the Q-Bus timeout -- but before the Q-Bus processor can issue the next read or write to the VMEbus, it must check the handshake mode READ/WRITE DONE status bit to verify that the operation has actually been completed on the VMEbus.

If the operation was a read from the VMEbus to the Q-Bus, the data returned from the read is stored in the HANDSHAKE DATA register on the Q22 adaptor card. This data register can be read by the Q-Bus processor after detecting that the READ/WRITE DONE status bit is a "1".

Handshake mode will not work on block mode memory to memory DMA transfers.

HANDSHAKE MODE READ/WRITE DONE (BIT 7)

See "Select Handshake mode". The READ/WRITE DONE bit indicates that the read or write operation on the VMEbus has been completed and that the Q-Bus processor can issue another read or write command. The bit is automatically reset at the beginning of a read or write operation and is set when the VME adaptor indicates to the Q-Bus adaptor that the operation has been completed. If the operation was a VMEbus read, the data from the read is stored in the HANDSHAKE DATA register.

Q-Bus READ BYTE SELECT (BITS 5 and 4)

The Q-Bus can selectively write to either the high or low byte of a word address on the VMEbus, but reads are always word wide. There are some instances, particulary when addressing I/O devices on the VMEbus, when it is necessary to only do a byte read. The two READ BYTE SELECT bits determine weather the read is to be a word read, a high byte read, or a low byte read.

SELECT BIT 1	SELECT BIT 0	OPERATION
0	0	NORMAL WORD READ
0	1	READ LOW BYTE
1	0	READ HIGH BYTE
1	1	NOT DEFINED

These bits hold their value until they are re-written with a new value.

HANDSHAKE MODE DATA

This register holds the read data received from the VMEbus when handshake mode is selected and when the READ/WRITE DONE status bit is set.

Q22bus LOCAL NODE STATUS REGISTER (read only)

BIT			FUNCTION
7	---	"1"	= interface parity error
6	---	"1"	= BERR* on VMEbus during Q22bus to VMEbus transfer
5	---	"1"	= PR interrupt FF on Q22bus card is set
4	---		always a 1
3	---		not defined - reserved for future use
2	---	"1"	= Interface Timeout
1	---	"1"	= PT interrupt FF on Q22bus card is set
0	---	"1"	= VMEbus powered down or the I/O cable is off

The Q22bus LOCAL NODE STATUS REGISTER - read only register

LOCAL NODE Q22bus STATUS REGISTER bit 7 is a "1" if a interface parity error, remote BERR*, or interface timeout has occurred on a Q22bus to VMEbus transfer.

LOCAL NODE Q22bus STATUS REGISTER bit 6 is a "1" if a VME BERR* has occurred on a Q22bus to VMEbus transfer.

LOCAL NODE Q22bus STATUS REGISTER bit 5 is a "1" when the PR interrupt flip flop on the Q22bus adaptor card has been set by a processor on the VMEbus.

LOCAL NODE Q22bus STATUS REGISTER bit 2 is a "1" if an interface timeout occurred. The adaptor waits 10 microseconds for a response to a read or write command on the VMEbus. If the the VME adaptor cannot complete the read or write within 10 microseconds, the interface timeout status bit is set and the operation is terminated.

LOCAL NODE Q22bus STATUS REGISTER bit 1 is a "1" when the PT flip flop on the Q22bus adaptor card is set.

LOCAL NODE Q22bus STATUS REGISTER bit 0 is a "1" if power is off at the VMEbus chassis or if the I/O cable is not connected. If this bit is a "1" there is no point in trying to communicate with the VMEbus since only timeout status errors will result.

ADDRESS PAGE REGISTER (write only)

This register is gated to the Q-bus address bus on VME to Q-bus cycles when the USE ADDRESS PAGE REGISTER command bit in the Q-bus COMMAND REGISTER is set. It is also gated to the DUAL PORT RAM address bus when the VMEbus accesses DUAL PORT RAM if the command bit is set. It is physically the same register as the page register that is addressed from the VMEbus at address I/O LO + 0A.

Q22bus ADAPTOR CARD REMOTE NODE REGISTERS

The Q22bus adaptor card REMOTE NODE registers are controlled by processors on the VMEbus. The Q22bus REMOTE NODE registers are:

VME I/O SEL ADDRESS	I/O WRITE FUNCTION	I/O READ FUNCTION
VME I/O SEL + 8	Q22bus CARD PAGE CTRL	Q22bus CARD PAGE CTRL
VME I/O SEL + 9	Q22bus CARD COMMAND REG	Q22bus CARD STATUS REG
VME I/O SEL + A	reserved	reserved
VME I/O SEL + B	Q22bus CARD PAGE REG	Q22bus CARD PAGE REG
VME I/O SEL + C	reserved	reserved
VME I/O SEL + D	reserved	reserved
VME I/O SEL + E	reserved	IACK READ
VME I/O SEL + F	reserved	IACK READ

Q22bus CARD REMOTE NODE COMMAND REGISTER - write only register

BIT	FUNCTION
7 -- "1"	= reset Q22bus card (one shot, allow 1 sec)
6 -- "1"	= clear PT interrupt FF on Q22bus card
5 -- "1"	= set PR interrupt FF on Q22bus card "0" = reset interrupt
4 -- "1"	= LOCK Q22bus "0" = UNLOCK Q22bus
3 -- "1"	= use address page register "0" = use address bias jumpers
2 -- "1"	= select I/O page
1 --	PR mode bit 1
0 --	PR mode bit 0

Q22bus CARD REMOTE NODE STATUS REGISTER (read only)

BIT		FUNCTION
7 -------		reserved for future use
6 -------		reserved for future use
5 -------	"1"	=PR interrupt FF on Q22bus card is set
4 -------	"1"	=LOCK Q22bus BUS not set (this is the inverted state of the lock bus flip flop)
3 -------	"1"	= USE ADDRESS PAGE REGISTER is selected
2 -------	"1"	= I/O PAGE flip flop is set
1 -------	"1"	= PT interrupt FF on Q22bus card is set.
0 -------		reserved for future use

Q22bus CARD PAGE CONTROL REGISTER (write/read register)

```
BIT
 7 ------- "1" = byte swap on VME to Q22bus or
                 VME to DUAL PORT RAM transfers
 6 ------- "1" = word swap on VME to Q22bus or
                 VME to DUAL PORT RAM transfers
 5 -------       must be zero
 4 -------       must be zero
 3 -------   PAGE WINDOW SIZE SELECT BIT 3
 2 -------   PAGE WINDOW SIZE SELECT BIT 2
 1 -------   PAGE WINDOW SIZE SELECT BIT 1
 0 -------   PAGE WINDOW SIZE SELECT BIT 0
```

Q22bus CARD ADDRESS PAGE REGISTER (write/read register)

```
BIT                    FUNCTION
 7 -----------  not defined - must be 0
 6 -----------  not defined - must be 0
 5 -----------  Q22bus ADDRESS BIT 21
 4 -----------  Q22bus ADDRESS BIT 20
 3 -----------  Q22bus ADDRESS BIT 19
 2 -----------  Q22bus ADDRESS BIT 18
 1 -----------  Q22bus ADDRESS BIT 17
 0 -----------  Q22bus ADDRESS BIT 16
```

Q22bus CARD IACK READ REGISTER (16-bit read-only register)

```
BIT                      FUNCTION
15 -----------        Always a "0"
14 -----------        Always a "0"
13 -----------        Always a "0"
12 -----------        Always a "0"
11 -----------        Always a "0"
10 -----------        Always a "0"
 9 -----------  Q-bus interrupt vector bit  9
 8 -----------  Q-bus interrupt vector bit  8
 7 -----------  Q-bus interrupt vector bit  7
 6 -----------  Q-bus interrupt vector bit  6
 5 -----------  Q-bus interrupt vector bit  5
 4 -----------  Q-bus interrupt vector bit  4
 3 -----------  Q-bus interrupt vector bit  3
 2 -----------  Q-bus interrupt vector bit  2
 1 -----------        Always a "0"
 0 -----------        Always a "0"
```

THE Q22bus CARD REMOTE NODE COMMAND REGISTER (write only)

VMEbus processors can write to this register on the Q22bus adaptor card to configure it for various operating modes or to otherwise control the card.

A description of each of the bits in the Q22bus CARD REMOTE NODE COMMAND REGISTER follows here:

RESET Q22bus BUS (BIT 7)

The Q22bus card has a power-on-reset circuit that resets the the Q22bus adaptor card when power is applied to the Q22bus chassis. The time duration of the reset is normally 500 milliseconds. This reset circuit can be activated also from the VMEbus by writing to the Q22bus CARD REMOTE NODE COMMAND REGISTER with bit 7 set to a "1". After triggering the reset, your program should wait about a second before starting another Q22bus cycle.

If the Q-bus is used in processor mode, this remote reset will also go out onto the Q-bus BINIT pin and reset the other boards in the Q-bus backplane. (See page 30.)

CLEAR PT INTERRUPT FROM VMEbus (BIT 6)

If a Q22bus processor card has set the PT interrupt flip-flop on the Q22bus card, a VMEbus processor can clear it by writing a "1" to bit 6 in the Q22bus REMOTE NODE COMMAND REGISTER.

SEND PR INTERRUPT TO Q22bus (BIT 5)

If a VMEbus processor wants to send a PR interrupt to the Q22bus it does so by writing a "1" to bit 5 in the Q22bus REMOTE NODE COMMAND REGISTER. Writing a "0" will clear the interrupt.

LOCK Q22bus BUS (BIT 4)

Writing a "1" to bit 4 in the Q22bus REMOTE NODE COMMAND REGISTER sets the LOCK BUS flip-flop. Once the Q22bus adaptor has been granted use of the Q22bus, it executes its Q22bus cycle and then releases the bus. If the BUS LOCK flip flop is set, the Q22bus adaptor will immediately request and seize the Q-bus grant. This is useful in a multiprocessor applications where it is common for processors to signal availability of a resource through an indivisible read-modify-write semaphore operation. The BUS LOCK feature permits a VMEbus processor to keep the Q22bus bus locked through a VME memory read followed by a VME memory write cycle. The bus can then be unlocked when the lock flip-flop is cleared by the VMEbus processor and the Q22bus processor can examine the semaphore using the Q22bus read-modify-write instructions.

USE ADDRESS PAGE REGISTER (BIT 3)

VME bus masters can address Q22bus RAM or DUAL PORT RAM through either of two techniques:

(1) direct mode

(2) address page register mode

In the standard direct addressing mode, RAM is addressed from the VMEbus by setting a "window" in VMEbus address space as large as the block of RAM to be addressed. For example, if you wanted to address 128K bytes of memory in the Q22bus, you would then set the REMOTE BUS RAM jumpers on the VME adaptor card for a 128K byte window in VMEbus address space. Page mode permits you to address all Q22bus RAM locations from the VMEbus through a 65K byte to 1 megabyte window in VMEbus address space. The upper six address bits for the Q22bus are set by an 8-bit page register located on the Q22bus card. The remaining sixteen lower Q22bus address bits are provided by the address offset in the VMEbus REM RAM window. In page mode, the ADDRESS BIAS JUMPERS are bypassed and the upper six address bits are provided by the address page register. It is possible to use both modes and switch between them under program control. In that case, use the first 65 Kbytes of the REMOTE RAM window in the VMEbus for addressing when in page mode. The PAGE register bypasses the ADD BIAS jumpers when PAGE mode is selected.

The PAGE MODE bit also controls paging from the VMEbus to the optional DUAL PORT RAM. If the PAGE MODE bit is set, address bits A16 through A21 to the DUAL PORT memory from the VMEbus are provided by the value in the PAGE REGISTER.

I/O PAGE (BIT 2)

Setting this bit to a "1" selects I/O PAGE mode. In this mode, memory reads and writes to the REMOTE BUS RAM window are converted into I/O PAGE reads and writes on the Q22bus. This is useful if the I/O space window set by the VME card I/O SEL jumpers is too restrictive for your application. I/O page mode permits access to all 8K bytes of the Q22bus I/O PAGE address space through a 65K byte window in VMEbus RAM address space.

PR MODE BITS (BITS 1 and 0)

Along with setting the PR bit, the VMEbus processor must also set control bits 0 and bit 1 in the same register. If bit 0 is set, the PR interrupt flip-flop is interpreted as PR 1. If bit 1 is set, the PR interrupt is interpreted as PR 2. If neither bit 0 or bit 1 is set, the PR interrupt is interpreted as PR 0. After acknowledging the PR interrupt, the Q-Bus processor can clear the PR flip-flop to inform the VMEbus processor that the requested Q-Bus task has been completed. Note that only a "0" to "1" transition of the PR flip-flop will cause a Q-Bus interrupt, so it is necessary for either the Q-Bus processor or the VMEbus processor to clear it before it can cause another PR interrupt by setting it again.

ADDRESS PAGE REGISTER - write/read register

This register is gated to the Q22bus address bus on VMEbus to Q22bus cycles when the USE ADDRESS PAGE REGISTER command bit in

the Q22bus REMOTE NODE COMMAND REGISTER is set. If the command bit is set, the address page register is also gated to the DUAL PORT RAM address bus when the VMEbus accesses DUAL PORT RAM.

BIT	FUNCTION
7	not defined - must be 0
6	not defined - must be 0
5	Q22bus ADDRESS BIT 21
4	Q22bus ADDRESS BIT 20
3	Q22bus ADDRESS BIT 19
2	Q22bus ADDRESS BIT 18
1	Q22bus ADDRESS BIT 17
0	Q22bus ADDRESS BIT 16

Q22bus PAGE CONTROL REGISTER - write/read register

This register controls the size of the page window on the Q22bus adaptor card. It also controls byte and word swapping on VMEbus to Q22bus or VMEbus to dual port RAM transfers. The default page window size selected when the Q22bus adaptor card is reset is 65K. Larger sized page windows can be selected by writing to the Q22bus PAGE CONTROL REGISTER. For example, if a 128 Kbyte page window size is selected, the PAGE REGISTER would provide only the upper five address bits and the VMEbus would provide the lower seventeen address bits of the 22-bit address.

NOTE: For whatever page size used, the REMOTE RAM and DUAL PORT RAM windows selected by jumpers on the VME card must start at an address in the VMEbus that is an even multiple, starting from address zero, of the selected page window size. Thus, for a 65 Kbyte page window size, the window must start on a 65 Kbyte address in VMEbus address space. For a 128 Kbyte page window, the VMEbus address must start on a 128 Kbyte address in VMEbus address space.

The following table shows how bits in the Q22bus PAGE CONTROL REGISTER select various page window sizes.

PAGE CONTROL REGISTER BIT				PAGE WINDOW SIZE
BIT 3	BIT 2	BIT 1	BIT 0	
0	0	0	0	65 KBYTES
0	0	0	1	128 KBYTES
0	0	1	1	256 KBYTES
0	1	1	1	512 KBYTES
1	1	1	1	1024 KBYTES

Two bits in this register also control byte and word swapping on VMEbus to Q22bus or VMEbus to DUAL PORT RAM transfers.

BYTE SWAP ON VMEbus to Q22bus or VMEbus to DUAL PORT RAM TRANSFERS (BIT 7)

If this bit is set to a "1", VMEbus data bits 8-15 are routed to the least significant byte (data bits 0-7 on the Q22bus). Also, VMEbus data bits 0-7 are routed to the most significant byte (bits 8-15 on the Q22bus). The same effect can be accomplished by placing a jumper in the Q22bus adaptor card SYST jumper block. Use the jumper if you want byte swap always enabled. Use the byte swap control bit if you want to switch between swapped and non-swapped modes.

WORD SWAP ON VMEbus to Q22bus or VMEbus to DUAL PORT RAM TRANSFERS (BIT 6)

If this bit is set to a "1", address bit A1 from the VMEbus is inverted on transfers to the Q22bus or to the DUAL PORT RAM. The same effect can be accomplished by placing a jumper in Q22bus adaptor card SYST jumper block. Use the jumper if you want word swap always enabled. Use the word swap control bit if you want to switch between swapped and non-swapped modes.

Q22bus REMOTE NODE STATUS REGISTER

Q22bus REMOTE NODE STATUS REGISTER bit 5 shows the state of the PR interrupt controlled by bit 5 in the Q22bus REMOTE NODE COMMAND REGISTER.

Q22bus REMOTE NODE STATUS REGISTER bit 4 shows the inverted state of the LOCK BUS flip flop controlled by bit 4 in the Q22bus REMOTE NODE COMMAND REGISTER.

Q22bus REMOTE NODE STATUS REGISTER bit 3 shows the state of the USE ADDRESS PAGE REGISTER flip flop controlled by bit 3 in the Q22bus REMOTE NODE COMMAND REGISTER.

Q22bus REMOTE NODE STATUS REGISTER bit 2 shows the state of the I/O PAGE flip flop controlled by bit 2 in the Q22bus REMOTE NODE COMMAND REGISTER.

Q22bus REMOTE NODE STATUS REGISTER bit 1 shows the state of the PT interrupt flip flop controlled by bit 1 in the Q22bus REMOTE NODE COMMAND REGISTER.

THE IACK READ REGISTER -read only

A VMEbus processor can instruct the Q22bus adaptor card to perform an interrupt acknowledge cycle on the Q-bus. A VME processor card does this by reading from the Q22bus ADAPTOR CARD IACK READ REGISTER. The Q22bus adaptor converts a read of this register address into an interrupt acknowledge cycle on the Q-bus. The Q-bus interrupt vector is returned to the VME processor as data from the read. This operation is valid only if the Q22

adaptor card is jumpered for PROCESSOR MODE.

BYTE, WORD, and LONGWORD ADDRESSING

68000-type microprocessors address data differently than DEC type processors. This creates an opportunity for confusion when interchanging data between the two processor types. The Bit 3 adaptor maps data bits 0 through 7 on the VMEbus to data bits 0 through 7 on the Q22bus and data bits 8-15 on the VMEbus to data bits 8-15 on the Q22bus. In both the Q22bus environment and the VME environment, data bits 0-7 are considered the least significant byte and data bits 8-15 are considered the most significant byte.

Executing a byte instruction on the Q22bus causes a byte operation to occur on the VMEbus. The upper half of a 16-bit DEC processor register maps to VME data bus bits 8-15, and the lower half of a 16-bit DEC register maps to VME bits 0-7. Executing a word instruction on the Q22bus causes a word operation to occur on the VMEbus.

There are times, especially when dealing with strings of text information, where it is more convenient to swap the byte significance around. Jumper pins in the SYST jumper block on the Q22bus adaptor card control byte and word swapping in both directions. Register command bits on the Q22bus adaptor card also control byte and word swapping.

THE SETUP PROGRAM

If your application uses the adapter card status or control registers, it is necessary to run a simple setup program to initialize the card. The program would use the following sequence:

1. DO AN I/O READ from the local node status register to test if the remote chassis has power on.
2. DO AN I/O READ from the remote node status register to flush out interface errors caused by the power on transition.
3. DO AN I/O WRITE WITH DATA 80 hex to the local node command register to clear the status register power up errors.
4. DO AN I/O READ from the local node status register to see that no interface errors are present and that the preceding steps were successful.

TESTING THE ADAPTOR

The DEBUG facilities provided with many processor boards can be a useful tool to test if you can communicate between the two systems. You should be able to display memory and modify memory in the other system just as though it was memory on the local system chassis. This is a good way to initially test the adaptor cards and the configuration jumpers. Another good test is to execute a memory diagnostic in the local chassis that tests memory in the remote chassis. The Bit 3 432 adaptor software support includes test routines in the user programming example.

ACCESS TIMES BETWEEN SYSTEMS

Writes from the local bus to the remote bus are pipelined. The adaptor activates the acknowledge signal as soon as it has captured the address and write data. The local bus system can proceed with the next instruction while the adaptor is completing the write on the remote bus. If the local bus gets back to the adaptor with a second write before the first write was completed, the adaptor holds the acknowledge so that the second operation cannot begin until the first one has completed. Reads are not pipelined since it is necessary to wait for the data before the cycle can be completed. Reads and writes to the remote dual port memory are faster than reads and writes to remote bus memory since it takes additional time to gain access to, and resync timing to, the remote bus.

An 8-bit or 16-bit pipelined write to the remote dual port memory or remote bus memory from the VMEbus takes about 560 nanoseconds (AS* to DTACK*). An 8 or 16-bit read from the VMEbus to the remote dual port RAM takes about 1.6 microseconds. Depending upon bus arbitration and bus memory speeds, an 8 or 16-bit read from the VMEbus to the Q-Bus takes 2.4 microseconds.

Reads and writes from the VMEbus to a local dual port memory card take about 560 nanoseconds.

An 8-bit or 16-bit pipelined write to the remote dual port memory or remote VMEbus memory from the Q-Bus takes about 740 nanoseconds (SYNC to REPLY). A 16-bit read from the Q-Bus to the remote dual port RAM takes about 1.7 microseconds. Depending upon bus arbitration and bus memory speeds, a 16-bit read from the Q-Bus to the VMEbus takes 2.3 microseconds.

Reads and writes from the Q-Bus to a local dual port memory card take about 800 nanoseconds (SYNC to REPLY).

The Block mode DMA capability moves data at a rate of 500 Kbytes per second to 700 Kbytes per second.

VME ADAPTOR CARD FRONT PANEL CONNECTOR

Connector P5 on the VME adaptor card provides an optional reset switch capability. The switch is de-bounced on the card. The mating connector housing is MOLEX number 09-50-3041. The pins for the connector housing are MOLEX number 08-56-0106.

P5 PIN	DESCRIPTION
PIN 1	NORMALLY OPEN CONTACT OF RESET SWITCH
PIN 2	LOGIC GROUND SIGNAL (RESET SWITCH COMMON)
PIN 3	CONNECTED TO 560 OHM PULL UP RESISTOR
PIN 4	NOT CONNECTED

Q22bus ADAPTOR CARD LEDS

The GREEN LED on the Q22bus card at location S9 labeled "LOADED" is "on" when the programmable logic arrays on the card have be successfully loaded up after power on. The green LED must be on for the card to work.

The RED LED on the Q22bus card at location S9 labeled "CMD" is "on" when the card is processing a read or write command from the VME adaptor card.

The RED LED on the Q22bus card at location S9 labeled "GRANT" is "on" when the card is receiving a Q-Bus bus grant. This signal gives the card permission to gate commands out to the Q22bus backpanel.

POWER REQUIREMENTS

Q22bus ADAPTOR CARD	+5 VOLTS @ 5.0 AMPS
VME ADAPTOR CARD	+5 VOLTS @ 4.5 AMPS

ENVIRONMENTAL

Temperature	0 to 55 degrees C (operating)
	-15 to +85 degrees C (storage)
Humidity	0 to 90% (non-condensing)