Bus-to-Bus Adaptor

Model 467-1 Adaptor
Hardware Manual

Model 467-1 Adaptor Hardware Manual

Connects a SBus Computer to a VMEbus System

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Preface

This manual describes the Bit 3 Model 467-1 Adaptor that connects a Sun SBus® computer, such as a SPARCstation®, to a VMEbus system. It includes information about the Adaptor's operation, installation, configuration, and control and status registers.

To simplify installation and eliminate operation problems, Bit 3 recommends that you review this manual before beginning to install your new Adaptor cards. Please pay close attention to the sections on card configuration and Adaptor registers.

- Chapter 1 provides an executive overview of the Adaptor, product description, specifications, and requirements.
- Chapter 2 gets you started with information about the Adaptor package and cable.
- Chapter 3 gives a detailed description of the VMEbus Adaptor card configuration.
- Chapter 4 describes SBus Adaptor card configuration.
- Chapter 5 includes installation instructions.
- Chapter 6 details SBus window address mapping.
- Chapter 7 contains information about Adaptor registers accessed from the SBus.
- Chapter 8 provides information about Adaptor registers accessed from the VMEbus.
- Chapter 9 contains additional programming notes on setup sequences and Adaptor testing.
- Chapter 10 discusses the Utilities Diskette example programs.
- Appendix A is a glossary of terms used throughout this manual.
- Appendix B describes VMEbus addressing.
- Appendix C contains jumper configuration worksheets.

➔ Important Notes:

- *Do not* remove Adaptor cards from their anti-static bags until you have discharged yourself by touching a grounded object. Static electricity can damage integrated circuit components and cards.
- Be sure power is OFF before installing Adaptor cards.

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Chapter 1: Adaptor Functions

1.0 Executive Overview

The Bit 3 Model 467-1 Adaptor is an easy-to-use, cost-effective way to share memory and special purpose cards between a SBus computer and a VMEbus system. The Model 467-1 Adaptor provides high-speed data transfers between the two systems, and requires minimal software support.

Model 467-1 interconnects the SBus and VMEbus systems at the physical layer. Working at the lowest level, the bus, the Adaptor allows the two systems to share memory; memory appears to and is treated by each system as if it were its own. In addition, a card only available on one bus may be directly controlled by a device on another bus. For example, an Array Processor board in a VMEbus chassis can be directly controlled by the SBus processor.

The Adaptor supports bi-directional random access bus mastering from either system and also supports 32-bit data transfers using a built-in DMA Controller. This controller enables the Adaptor to transfer data from one system's memory to the other system's memory at sustained data transfer rates of up to 26 Megabytes per second (M Bytes/sec). It also allows a VMEbus DMA device to DMA through the Adaptor directly into SBus memory at data transfer rates in excess of 12M Bytes/sec.

Model 467-1 supports two methods of inter-system communications: Memory Mapping and Direct Memory Access (DMA). Memory Mapping controls random access (PIO transfers) to VMEbus RAM, dual-port memory, and VMEbus I/O, and provides an easy-to-use, flexible interface with low overhead. A SBus bus master can access memory in the VMEbus system through a window in SBus slot space. Conversely, a VMEbus bus master can access SBus memory from a window in VMEbus address space.

Seven mapping registers are available to steer accesses in 4M/32M byte segments from SBus slot space to VMEbus address space. Each register can be independently set to point to any address on the VMEbus.

A Page Register is available to control accesses from the VMEbus to the SBus. The Page Register provides the upper 16 - 12 bits of the 32-bit SBus address.

Memory Mapping also controls access to dual-port memory. Dual Port RAM is an optional card installed on the VMEbus Adaptor card. Dual Port RAM provides a memory buffer; saves the cost of additional memory cards; and requires no additional VMEbus card slots.

Bit 3's Dual Port RAM is a printed circuit card that plugs into the VMEbus Adaptor card as a daughter card. The following memory sizes are currently available: 32K, 128K, 1M, 2M, 4M, and 8M bytes.

Optional Dual Port RAM provides shared memory space that is accessible from either system. Dual Port RAM access uses only the bandwidth of the accessing bus. Consequently, data can be exchanged with minimal impact on the performance of the other system's bus. Both systems can access Dual Port RAM simultaneously; the Adaptor arbitrates accesses.

DMA, the other method of communication, is the automatic transfer of data from one memory address to another. Model 467-1 supports two DMA techniques: DMA Controller Mode and Slave Mode DMA.

DMA Controller Mode uses the Adaptor's DMA Controller to enable high-speed data transfers from one system's memory directly into the other system's memory. Data transfer in either direction can be initiated by the SBus or VMEbus processor. Each DMA cycle supports transfer lengths from 4 bytes to 16M bytes. The DMA Controller also allows data transfers between SBus memory and Dual Port RAM on the VMEbus Adaptor card.

To initiate a DMA Controller transfer, a processor sets the transmitting and receiving system's target addresses, and a word count. Bits in the command registers specify parameters, such as word width, destination address space (A32, A24 or A16), the address modifier, and Block or Non-Block transfer mode. Interrupts are prevented from being passed between the buses during the DMA transfer. Also, random access across the I/O cable must not occur during a DMA Controller transfer.

In Slave Mode DMA, the Adaptor card appears as a slave memory card. This type of DMA transfer is performed when a DMA device transfers data through the Adaptor directly into the SBus.

Model 467-1 Adaptor does not link the timing of the two buses (so that activity on one bus does not slow down the other). Instead, the Adaptor permits each bus to operate *independently*. The buses are linked only when a memory or I/O reference is made to an address on one system that translates to a reference on the other.

The Model 467-1 Adaptor consists of two cards: a SBus card and a 6U size VMEbus card. The two cards are connected by a round EMI-shielded copper-conductor cable purchased separately from Bit 3.

Cable is available in standard 8- or 25-foot lengths and custom lengths. Fiber-Optic Interface Cards and Modules are also available from Bit 3.

Optional Support Software is available from Bit 3. Model 943 and Model 944 Support Software provide a SBus device driver and example programs that demonstrate the use of the Model 467-1 Adaptor.

1.1 Card Specifications

Bus Communication Specifics:
Each Adaptor card may function as a transmitter device at one end of the Adaptor cable and as a receiver at the other. Communication may be specified as one way in either direction or as two-way. A dual-port memory option, Dual Port RAM, provides a convenient way for VMEbus masters to pass data to and from the SBus.

Accesses from the SBus to the VMEbus are A32, A24, or A16; data accesses are 1 byte, 2 bytes, 4 bytes, 16 byte burst mode, and 32 byte burst mode.

Accesses from the VMEbus to SBus are A32 or A24; data accesses are D32, D16, D8, or D32 Block Mode transfer.

Bus Arbitration:
VMEbus: Release-On-Request (ROR);
Release-On-Bus-Clear.

Access Times:
SBus read/write access to remote RAM: 2.1 µsec.
SBus read/write access to remote Dual Port RAM: 2.0 µsec.
VMEbus read/write access to local Dual Port RAM: 500 nsec.

Block Mode Transfer Rate:
SBus read/write access to remote RAM with 32 byte burst: 4M Bytes/sec.
VMEbus Block Mode access to SBus RAM -
VMEbus writes to SBus: 12M Bytes/sec.
VMEbus reads from SBus: 14M Bytes/sec.

DMA Controller Transfer Rate:
The Adaptor is capable of DMA data rates of:
26M Bytes/sec with 20 nsec Block Mode VMEbus cards;
20M Bytes/sec with 50 nsec Block Mode VMEbus memory cards;
10M Bytes/sec with 200 nsec Block Mode memory cards;
12M Bytes/sec DMA from SBus to Dual Port RAM.

Actual data rates measured from the application software level are also dependent on the capabilities of the SBus I/O channel controller and system software overhead.

DMA data transfer block length: 4 bytes to 16M bytes.

Interrupt Passing:
Up to four interrupts can be sent from the VMEbus system to the SBus. These interrupts are selected from eight possible sources: VMEbus IRQ1 - IRQ7 and the PT interrupt.

Although there are several potential VMEbus interrupt sources, only one SBus interrupt signal is available. Therefore, an 8-bit status register and an interrupt control register are provided for the SBus interrupt handling routine to use to determine the VMEbus interrupt source.

Two types of programmed interrupts, PT and PR interrupts, can be exchanged between the SBus and the VMEbus.

Interrupt Acknowledgment:
SBus acknowledgment of VMEbus interrupts and VMEbus vector passing is provided through an Adaptor card control register.

SBus - VMEbus Timeout:
SBus to VMEbus transfer cycles timeout within 1200 SBus clock cycles (48 μsec with 25 MHz SBus clock, or 75 μsec with a 16 MHz SBus clock). This results in an error bit being set and an interrupt generated if enabled.

The timeout period is implemented by asserting a retry acknowledgment at 240 SBus clock cycles after the SBus system initiates a VMEbus access. After four retries, if there is still no response from the VMEbus, the Adaptor issues a false acknowledgment, sets an error status bit, and generates an interrupt.

SBus Configuration ROM:
The SBus Configuration ROM includes driver and card information.

Read-Modify-Write:
Read-modify-write transactions from VMEbus to local dual-port memory are indivisible.

Read-modify-write to the VMEbus system is simulated by a bus-lock control bit in an Adaptor control register.

Read-modify-write from the VMEbus system into SBus memory is not supported.

Conformance:
The VMEbus Adaptor card meets IEEE 1014C specifications.

The SBus Adaptor card meets Revision B.0 of the SBus specification and does not use any of the extensions.

Power Requirements:
The VMEbus Adaptor card draws 3.5A at 5V.
The SBus Adaptor card draws 1.0A at 5V.

Environment:

Temperature:	0° to 60° C operating;	-15° to 85° C storage.
Humidity:	0% to 90% non-condensing.	

1.1.1 SBus Adaptor Card Notes

- There is one Compatibility Mode configuration jumper on the SBus Adaptor card. All other configuration is accomplished via register settings.

- Fixed window size of 32M bytes for A25 machines or 256M bytes for A28 machines.
  - Local and remote node I/O registers.
  - VMEbus I/O window is always 64K bytes.
  - Seven VMEbus / Dual Port RAM windows are 4M/32M bytes each.

- Interrupts are grouped on exactly one interrupt line.

- Possible sources of interrupts:
  - Pending VMEbus interrupts IRQ1 - IRQ7,
  - Error Interrupt,
  - DMA Done Interrupt,
  - PR Programmed Interrupt,
  - PT Programmed Interrupt.

- Interrupt enable control bit.

1.1.2 VMEbus Adaptor Card Notes

- All configuration is accomplished via jumpers.

- Adjustable VMEbus window size.
  - Local and remote node I/O registers.
  - SBus memory window size is adjustable to 1M bytes in increments of 64K bytes.
  - Dual Port RAM window size is adjustable to 16M bytes in increments of 64K bytes.

- Multiple interrupts are separately jumpered.

1.2 VMEbus Address Modifier Types Supported

- For SBus random access to the VMEbus, any address modifier, except VME64, can be supported via Window Mapping Registers or the VMEbus Adaptor card Address Modifier Register.
- For VMEbus access to Dual Port RAM, all A24 and A32 address modifiers are accepted.
- For VMEbus access to the SBus, all A24 and A32 address modifiers are accepted.
- For VMEbus access to Adaptor control and status register I/O space:
  - 2D for Short Supervisory access.
  - 29 for Short Non-Privileged access.
- For DMA Controller Mode, the VMEbus address modifier is selected by loading the required value into the VMEbus Adaptor card's Address Modifier Register.

1.3 Bus-To-Bus Mapping

The Model 467-1 Adaptor works by mapping a portion of memory address space in the transmitter chassis into memory address space on the receiver chassis. The SBus Adaptor card allocates sections of slot space in the SBus chassis. Accesses within that space become memory or I/O accesses on the VMEbus. The VMEbus address spaces appear to a SBus processor as though they were present in the SBus chassis and behave as if they were local memory.

It is also possible to map a portion of memory space to work in the *opposite* direction -- in effect, giving both systems the ability to be a transmitter system during one transfer and a receiver system through a different operation.

1.4 Dual Port RAM

Dual Port RAM is an optional memory card that attaches to the VMEbus Adaptor card and appears to both systems as simply more memory. The address of the Dual Port RAM is independently set on each Adaptor card, and may be set to respond to one address range in one system and a different range in the other. Both systems can access the memory at the same time with the Adaptor arbitrating simultaneous accesses.

The following sizes of Dual Port RAM are available from Bit 3: 32K, 128K, 1M, 2M, 4M, and 8M byte cards.

➔ All Dual Port RAM cards are designed to ignore unused upper address bits when a large window is used (these bits are still used to determine that access is in the window). Therefore, for a 1M byte memory Dual Port RAM card, only Address Lines A19-A0 are significant; Address Lines A31-A20 are ignored.

1.5 System Controller Operation

The Model 467-1 Adaptor has the ability to act as a link between the two chassis even when the VMEbus chassis has no arbiter. This form of operation is called **System Controller Mode.**

System Controller Mode is selected on the VMEbus Adaptor card by configuring the **SYS** jumper block to drive the system clock, system reset, and the Bus Error (BERR) global timeout. The VMEbus Adaptor card may be configured to be a single-level bus arbiter on VMEbus level three.

1.6 Adaptor CSR Registers

Access from the VMEbus to the Adaptor Control and Status Registers (**CSR**) requires a minimum of 32 bytes of VMEbus I/O space. The SBus has a fixed window size of 64K to access Adaptor **CSR**. Only the first 32 bytes of this space are actually used.

1.7 Direct Memory Access (DMA)

Direct Memory Access, DMA, is the automatic transfer of data from one memory address to another *without* intervention from a processor once the transfer starts. DMA logic is usually employed when large files or sections of data need to be moved. DMA is a highly efficient way to move data because it does not require processor overhead.

The Bit 3 Model 467-1 Adaptor supports two types of DMA operations: DMA Controller Mode and Slave Mode DMA. In DMA Controller Mode, the Adaptor becomes a bus master on both the SBus and the VMEbus. DMA Controller Mode is used when the programmer wants the Adaptor to move a large block of data from one system to the other system. Transfer sizes from 4 bytes to 16M bytes are supported.

Slave Mode DMA, the other type of DMA, is performed when a VMEbus DMA device, such as a disk controller card, does a DMA transfer through the Adaptor directly into the SBus. In this case, the VMEbus Adaptor card looks like a slave memory card and the SBus Adaptor card becomes the bus master during the operation.

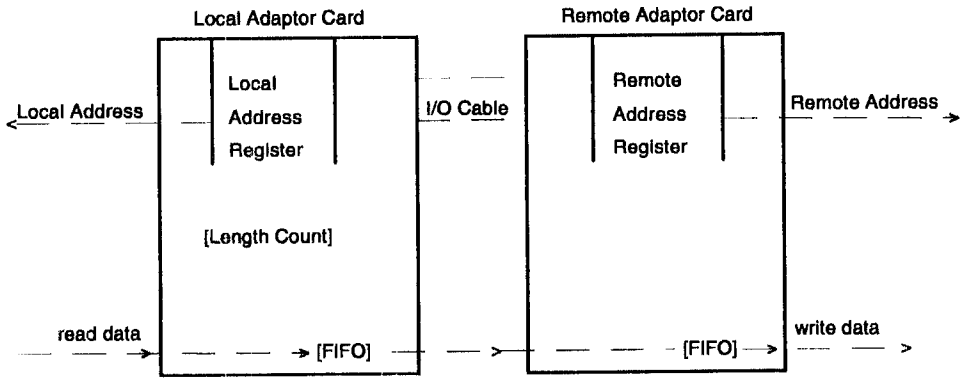
The DMA Controller is accessible from either a VMEbus or SBus processor through the Adaptor node I/O space. Consequently, a single processor can perform all DMA setup and start commands on *both* the local *and* remote Adaptor cards. To achieve the highest data transfer rates, a special mode (called Burst Mode on the SBus and Block Transfer or BLT on the VMEbus) can be selected. This special mode is capable of transferring several data words without generating a new address. Normally, a new address must be asserted for each word of data transferred. Up to 26M Bytes/sec (net throughput from system to system) in sustained DMA Controller operations is possible.

1.7.1 How DMA Controller Mode Transfers Occur

Each Adaptor card has a DMA Controller. The DMA Controllers are somewhat independent of each other. While they are synchronized to pass data across the interface cable, they also independently perform reads and writes in their respective chassis.

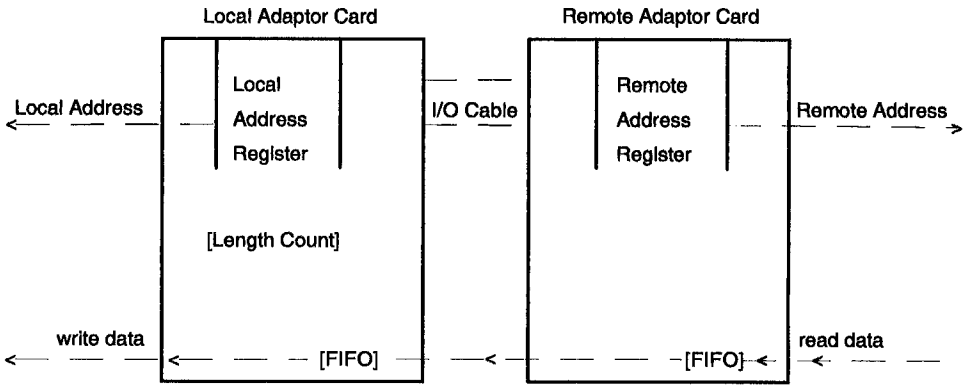
The basic operations in a DMA transfer from local to remote memory (DMA write), once the DMA transfer has started, are as follows:

1. The local Adaptor card presents an address to its bus from the local address register and signals a read.
2. The local read data are stored in the local FIFO (First In First Out) and the address register (a counter) increments.
3. When the FIFO has a complete packet of information, data are sent to the remote FIFO and the length counter decrements.
4. As the remote FIFO fills with data, the remote Adaptor card presents an address to the remote bus from the remote address register (also a counter) and signals a write. The data in the remote FIFO are written to its bus and the remote address register increments.
5. The DMA terminates when the length count equals zero.



DMA Transfer From Local To Remote
-- DMA Write --

The Model 467-1 Adaptor runs DMA transfers from remote to local (DMA read) in much the same way as described on the previous page. The remote bus controller begins by reading remote data and sending them from the remote FIFO to the local FIFO, where the local Adaptor card writes local FIFO data to local memory.



DMA Transfer From Remote To Local
-- DMA Read --

This form of DMA provides a very efficient, high-speed transfer because each bus is allowed to run at maximum speed. All data are moved without the intervention of a processor on either side of the Adaptor. Flow control is automatically provided between the two sets of FIFOs.

The side of the Adaptor that is reading data can fill its FIFO without waiting for data to be written to the other side of the Adaptor. Once the FIFO is full, it releases the bus for use by other devices and processors.

Similarly, the side of the Adaptor that is writing the data already has data available in the FIFO. When the FIFO becomes empty, the Controller releases the bus for use by other devices and processors.

The DMA set up routine includes setting a control bit on the VMEbus Adaptor card. This prevents interrupts from being sent to the SBus while the DMA is in progress. Random accesses across the cable from either side must not occur during a DMA Controller transfer.

A DMA transfer (read or write) can be initiated from either the SBus or VMEbus.

1.7.2 Slave Mode DMA

Slave Mode DMA is performed when a VMEbus DMA device, such as a disk controller card, does a DMA transfer through the Adaptor directly into the SBus. In this case, the VMEbus Adaptor card looks like a slave memory card.

If the VMEbus DMA device does not use VMEbus Block Mode transfer protocol, the operation defaults to a standard random access read or write. The maximum speed for this type of transfer is 2M Bytes/sec.

If the DMA device (i.e. the disk controller card) uses VMEbus Block Mode transfers, transfer rates through the Adaptor of 14M Bytes/sec are possible.

When the VMEbus Adaptor card receives a Block Mode write command, it buffers data through the DMA FIFOs before sending them to the SBus. Handshaking up and down the I/O cable only occurs when a data packet is sent, resulting in much higher throughput.

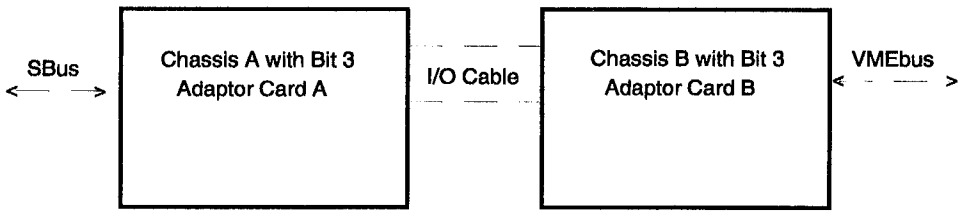
When the VMEbus Adaptor card receives a Block Mode read command, it pre-fetches up to 256 bytes of data from the SBus in 64 byte increments. If the pre-fetch causes the Adaptor to read more data than the VMEbus DMA Controller uses, the excess data are discarded. Pre-fetching the data into the FIFOs on the Adaptor card results in less handshaking and, therefore, greater throughput.

The Adaptor card never pre-fetches data across a 256-byte SBus address boundary.

Slave Block Mode DMA data transfers are supported in both directions. A SBus disk controller or a SBus processor executing burst transfers can directly DMA to VMEbus memory.

1.8 Conflict Control

Conflict control refers to the simultaneous use of the Adaptor I/O cable between the two Adaptor cards.



Assume a device in chassis **A** performs reads or writes to memory or I/O on chassis **B**, but devices in chassis **B** never perform reads or writes to cards inside chassis **A**. In this case, Adaptor card **A** would be the *transmitter* and Adaptor card **B** would be the *receiver*. Both cards can be a transmit device.

Except for interrupts, the transmit card has exclusive rights to use the I/O cable connecting the two Adaptor cards.

If devices in chassis **A** sometimes perform reads or writes to chassis **B** and devices in chassis **B** sometimes perform reads or writes to chassis **A**, then both Adaptor cards must be configured as transmitters. Either chassis can then control the other chassis. In this configuration, conflict could occur if chassis **A** tries to talk to chassis **B** at the same time that chassis **B** tries to talk to chassis **A**. If conflict occurs, the request from the SPARCstation is backed out by issuing a retry signal. The VMEbus request to the SBus is then processed, followed by the SBus retried command. Thus, the Adaptor can handle simultaneous reads and writes from both sides.

The Dual Port RAM interface is hardware-arbitrated; consequently conflicts are avoided when simultaneous reads and writes are made to the Dual Port RAM card.

1.9 Interrupt And Error Handling

Four cable interrupt or CINTx lines are used to pass the various types of interrupts between cards. A cable interrupt is the latched representation of a backpanel or programmed interrupt that is to be passed across the cable.

There are four sources of interrupts from the Adaptor:

- Cable interrupts from the VMEbus chassis to the SBus (backpanel interrupts).
- Programmed interrupts.
- An interface error interrupt.
- A DMA DONE interrupt.

1.9.1 Backpanel Interrupts

Up to four of seven VMEbus interrupts (IRQ1-IRQ7) may be passed to the SBus backplane. VMEbus interrupts are passed across the cable interrupt lines to the SBus Adaptor card. The SBus Adaptor card always interrupts at exactly one level.

1.9.2 Interface Error Interrupt

The interface error interrupt is active when any of several interface error conditions (timeout, parity error, or remote node bus error) are detected on the Adaptor card. It remains active until cleared with a reset status error command. The interface error interrupt and status bit are meaningful only if the Adaptor card initiates communication over the cable to the other Adaptor card.

➔ For the SBus Adaptor card, an error interrupt occurs only if both card interrupts are enabled and error interrupts are enabled.

1.9.3 DMA DONE Interrupt

The DMA DONE interrupt is active if the Interrupt Done enable bit of the DMA Command Register is set and a DMA Controller operation ended, either successfully or unsuccessfully. (An unsuccessful DMA transfer is indicated by error bits in the Local Status Register.) The interrupt remains active until cleared by forcing the DMA Command Register DMA DONE bit to zero or by starting another DMA operation.

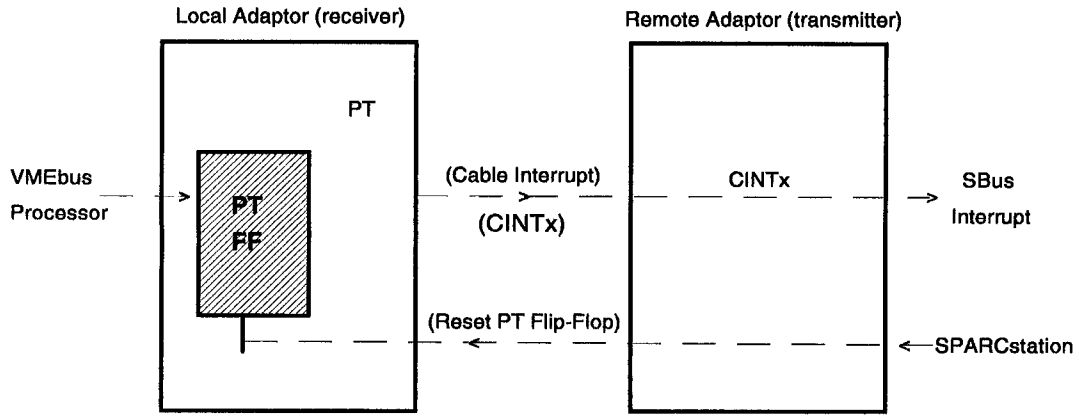
For the SBus Adaptor card, a DMA DONE interrupt occurs only if both card interrupts are enabled *and* DMA DONE interrupts are enabled.

1.9.4 Programmed Interrupts

Two types of programmed interrupts may be exchanged: PT (Programmed interrupt to Transmitter) and PR (Programmed interrupt to Receiver). See section 1.9.4.1 for information on PT interrupts. See section 1.9.4.2 for a description of PR interrupts.

1.9.4.1 Programmed Interrupt To Transmitter (PT)

The PT interrupt does not require the local Adaptor to use the cable read/write resources to send an interrupt to the other bus.



Programmed Interrupt To Transmitter
-- PT Interrupt --

The selection of the programmed interrupt to use (i.e. PT or PR) depends on if the programmed interrupt is being sent across the cable to an Adaptor card configured as a transmitter or as a receiver. If the remote Adaptor card is configured as a transmitter, send a PT interrupt. If the remote Adaptor card is configured as a receiver, send a PR interrupt.

PT interrupts work as follows:

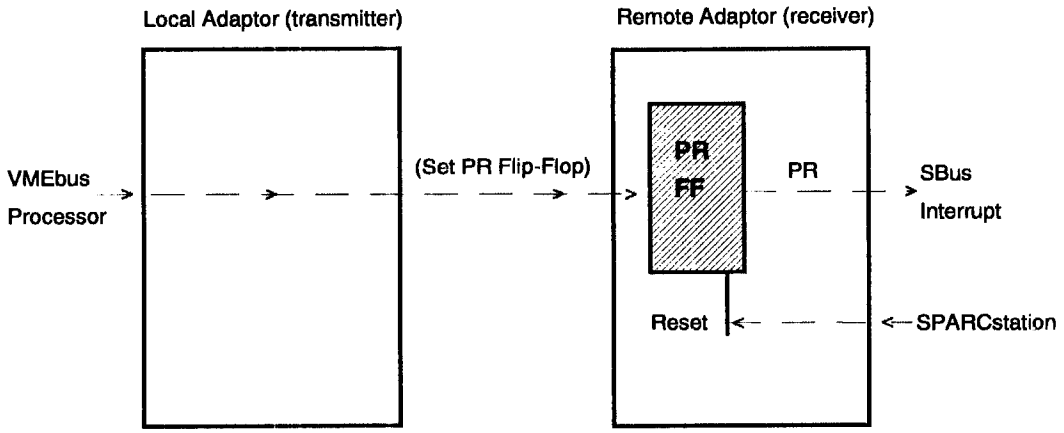
1. A local processor writes to the Adaptor card Local Node Command Register and sets the PT interrupt flip-flop on the Adaptor card in its chassis.

2. The PT interrupt line can be connected to any unused cable interrupt line (CINTx) that sends the interrupt to the remote chassis.

3. When the remote bus processor sees the PT interrupt, it clears the PT flip-flop by setting bit 6 of the Remote Node Command Register 1.

1.9.4.2 Programmed Interrupt to Receiver (PR)

The PR interrupt does not require the receiver Adaptor card to use the interface cable to reset the interrupt, and does not use a cable interrupt line to set the interrupt.



Programmed Interrupt To Receiver
-- PR Interrupt --

PR interrupts work as follows:

1. A local processor writes bit 5 of Remote Node Command Register 1 to set the PR interrupt flip-flop physically located on the remote Adaptor card.
2. If jumpered, the PR interrupt on the remote Adaptor card activates an interrupt line on the remote bus backplane. This interrupt can be jumpered to VMEbus Interrupt Request IRQ1 or IRQ2.
3. When the remote bus processor detects the bus interrupt, it can clear the interrupt by writing bit 6 of the Local Node Command Register 1 physically located on the Adaptor card in its chassis.

1.10 IACK Read Operation

A SBus processor can instruct the VMEbus Adaptor card to perform an Interrupt Acknowledge (IACK) cycle on the VMEbus by reading from the VMEbus Adaptor IACK Read Register. The Adaptor converts a read of this register into an interrupt acknowledge cycle on the VMEbus. The interrupt level to be acknowledged is determined by the IACK code bits in the Remote Node Command Register. The VMEbus interrupt vector is returned to the SBus processor as data from the read.

1.11 Mapping RAM

All accesses from SBus to VMEbus, except Adaptor I/O registers, are through Window Mapping Registers. Each of the seven Window Mapping Registers controls access to 4M / 32M bytes of VMEbus address space.

Chapter 2: Getting Started

2.0 Unpacking

The Bit 3 Model 467-1 Adaptor package contains the following items. Please identify each item and notify Bit 3 (**612-881-6955**) if any are missing:

- SBus circuit card - Part Number: 84903810.
- VMEbus circuit card - Part Number: 85154550.
- Utilities Diskette - Part Number: 84202300.
- Model 467-1 manual - Pub. Number: 84903890.
- One I/O cable to connect the two cards (purchased separately).
- Warranty card (please complete and mail).

➔ Eight-digit part numbers with card revision level are printed on white labels affixed to the Adaptor cards.

Bit 3 Adaptor cards are shipped in static-safe packages to protect the components on the card. It is important that you observe static safety precautions to prevent damage to the card during configuration and installation.

2.1 Adaptor Cables

Standard shielded cables to connect the two Adaptor cards are available in 8-foot and 25-foot lengths. Custom-length cables are also available from Bit 3. *All cables are purchased separately.*

2.2 Options

Adaptor Support Software, Dual Port RAM cards, and Fiber-Optic Interface Cards and Modules are also available from Bit 3. Please call **612-881-6955** for more information.

2.3 Help!

Please have the following items and information handy when calling Bit 3 for technical support:

- Model number of the Adaptor and revision level.
- Size of Dual Port RAM, if any.
- Configuration information including jumper settings on the VMEbus Adaptor card.
- This manual.

Technical support is available from 9 a.m. - 5 p.m. (Central Time) Monday - Friday, excluding holidays.

Contact Bit 3 at:

Mailing Address:	Bit 3 Computer Corporation 8120 Penn Avenue South Minneapolis, MN 55431-1393
Phone:	612-881-6955
FAX:	612-881-9674

2.4 Additional References

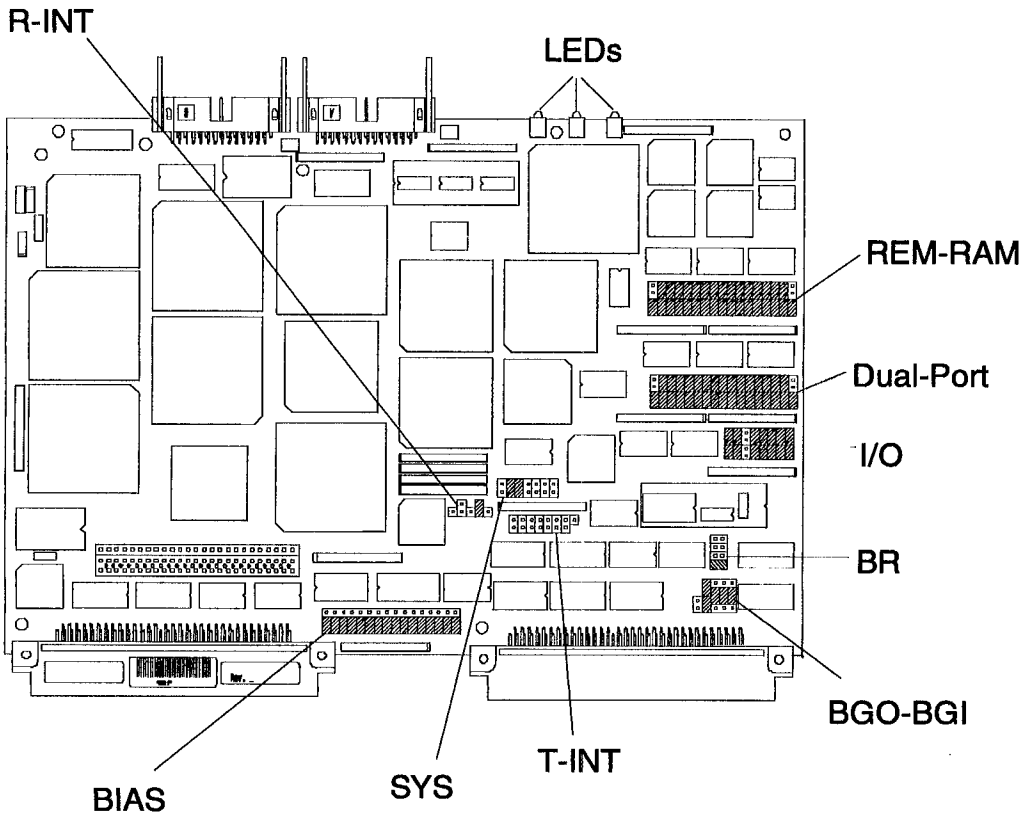
- *VMEbus Specification Manual*, VITA (VMEbus International Trade Association), 10229 N. Scottsdale RD., Suite E, Scottsdale, AZ 85253.
- *IEEE Standard 1014*, The Institute of Electrical and Electronics Engineers (IEEE), 445 Hoes Lane, Piscataway, NJ 08855-1331.
- *VMEbus Handbook*, Wade Peterson, VFEA International Trade Association, 10229 N. Scottsdale Road, Suite B, Scottsdale, AZ 85253.

Chapter 3: VMEbus Adaptor Card Configuration

3.0 Introduction

Chapter 3 provides detailed descriptions of jumper blocks on the VMEbus Adaptor card and instructions for their configuration. It is important that you understand how each feature is configured in order to use the Model 467-1 Adaptor correctly.

3.1 VMEbus Adaptor Card Diagram



Location of Jumper Blocks and LEDs

3.1.1 Configuration Notes

- Before configuring either Adaptor card, decide which cards will be transmitters. The SBus Adaptor card is always a transmitter. If the VMEbus is to be a transmitter, jumper 2 in the **SYS** block must be installed. For information about the **SYS** block see section 3.4.1.

- Refer to section 3.3 for VMEbus Adaptor card factory settings, then determine which jumpers need to be changed for your configuration.

- If a card is to be the VMEbus system controller, it must be installed in slot 1. Refer to Chapter 5 for installation instructions. Configure the VMEbus Adaptor card as shown in the first diagram in section 3.4.2.

- After installation, make sure the green **READY** LED on the VMEbus Adaptor card is lit. This LED must be on for the Adaptor card to operate.

3.2 Configuring For VMEbus System Controller Mode

➔ Correct system controller configuration is essential for communication with other VMEbus cards.

The VMEbus priority scheme permits other bus masters to use cards on the VMEbus. But before a VMEbus master can talk to other VMEbus cards, it first must gain control of the bus. A VMEbus functional module, the system controller, grants VMEbus cards permission to use the VMEbus. The system controller is either located on a separate system controller card or integrated into a processor card.

The VMEbus Adaptor card can be configured via jumpers to work with an already-installed system controller card that contains a bus arbiter. If necessary, the Adaptor can provide the system controller functions of driving the system clock and a single level bus arbiter on level three.

In single-level bus arbitration mode, the Adaptor is the highest priority bus master. It responds to bus requests on level three from other masters, and activates the level three bus grant line when the Adaptor does not need the VMEbus. The Adaptor operates in release-on-request mode except when the Bus Lock flip-flop is set.

3.3 VMEbus Adaptor Card Factory Settings

VMEbus Adaptor card is configured as follows when shipped:

VMEbus Dual Port RAM Range	Disabled
VMEbus Remote RAM	Disabled
VMEbus Address Bias	Passed Through
VMEbus Adaptor I/O Range	2000 - 201F (hex)
VMEbus RINT Jumpers	None
VMEbus TINT Jumpers	None
VMEbus IRQ Level	None
VMEbus Grant/Request Level	Bus Requester on Level 3

VMEbus card NOT driving VME SYSCLK
VMEbus card NOT driving VME SYSRESET
VMEbus card NOT driving VME bus timeout (BERR)

➔ The VMEbus Adaptor card is not the system controller.

3.4 VMEbus Adaptor Card Jumper Blocks

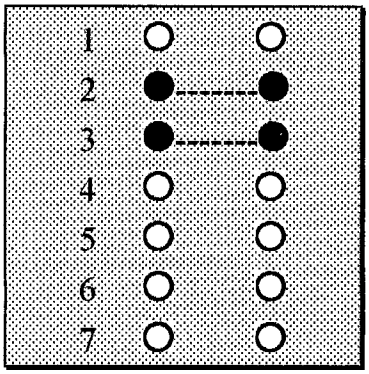
This section describes the jumper blocks on the VMEbus Adaptor card.

➔ Refer to the diagram in section 3.1 for jumper block locations.

3.4.1 System Jumpers

The SYS jumper block is shown here as the card is shipped:

➔ Jumper IN: ●-------● Jumper OUT: ○ ○



Jumper if the Address Modifier Register is used.
When this jumper is IN this card is a "transmitter".
Jumper is always IN.
Jumper if this card will drive VME SYSCLK.
Jumper if this card will drive VME SYSRESET.
Jumper if this card will detect bus timeouts.
Jumper is always OUT.

ADDRESS MODIFIER REGISTER (jumper 1): When this jumper is OUT, the address modifier presented to the VMEbus comes from the default values sent by the SBus Adaptor card. When this jumper is IN, the address modifier presented to the VMEbus comes from the Address Modifier Register on the VMEbus Adaptor card. If the jumper is OUT, a CSR bit can also enable use of the Address Modifier Register. The Address Modifier Register is always selected during DMA Controller transfers, regardless of the jumper and CSR settings. See section 7.2.5 for information about the Remote Address Modifier Register.

TRANSMITTER CARD SELECTION (jumper 2): This jumper is IN when the VMEbus Adaptor card requires the option to command the Adaptor cable (be a cable transmitter). It does not exclude the SBus Adaptor card from also being a cable transmitter. See section 1.8 for information on conflict control.

VME SYSCLK DRIVE (jumper 4): Allows the Adaptor card to supply the VMEbus SYSCLK signal to its VMEbus backplane. The card drives this signal (jumper IN) when it is the VMEbus system controller and no other device is driving SYSCLK. *There must be exactly one SYSCLK present for the Adaptor to function.*

VME SYSRESET DRIVE (jumper 5): Allows the Adaptor card to supply VMEbus SYSRESET to its VMEbus backplane, which may be either a VMEbus Adaptor card power-on reset or a programmed reset from the SBus.

VME BUS TIMEOUT (jumper 6): Allows the Adaptor card to drive the VMEbus BERR (bus error) signal to its VMEbus backplane if any transfer on the bus exceeds 48 µsec (bus timeout). When the VMEbus Adaptor card is the system controller, it is usually jumpered to detect bus timeout (jumper IN).

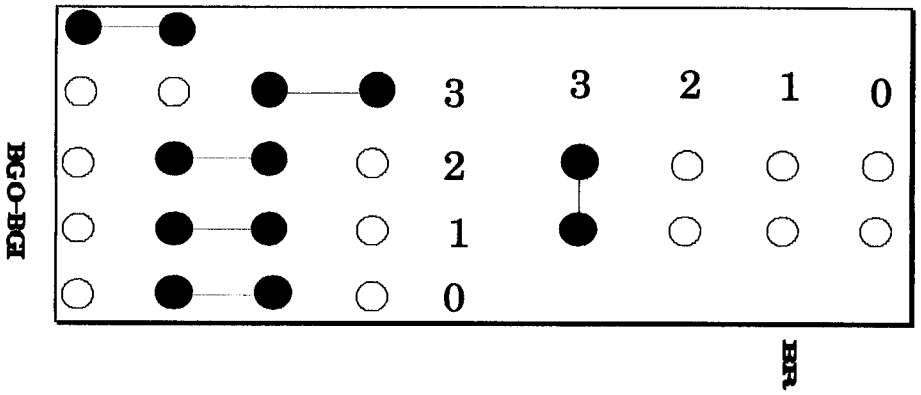
3.4.2 Bus Grant And Bus Request Jumpers

The **Bus Grant** (BGO-BGI) jumper block and the **Bus Request** (BR) jumper block establish the Adaptor card **Bus Grant** and **Request** levels.

If the VMEbus system has a system controller, the VMEbus Adaptor card can be configured to use any of the four **Bus Request/Bus Grant** levels. If there is no system controller in the VMEbus system, the Model 467-1 Adaptor can be set to become a single-level arbiter on level three. (In single-level bus arbitration mode, the VMEbus Adaptor card is the highest priority bus master. It responds to bus requests on level three and activates the level three **Bus Grant** line when the Adaptor does not need the bus.)

If the VMEbus Adaptor card *is to be the system controller*, configure the jumpers as follows:

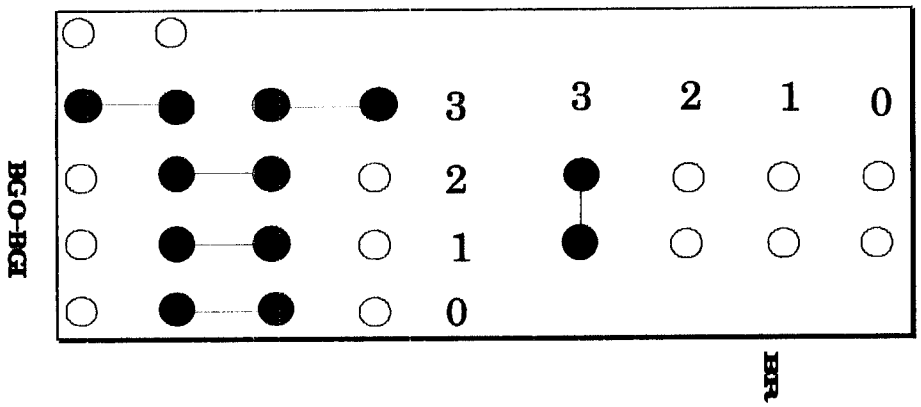
➔ Jumper IN: ●-------● Jumper OUT: ○ ○



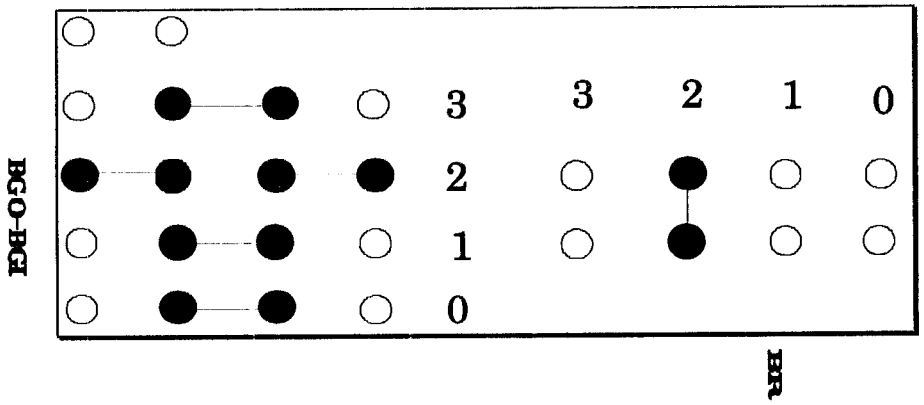
➔ If the Adaptor card is to be system controller, it must be installed in slot 1 of the VMEbus chassis and have jumper 4 in the **SYS** block installed (see **SYS** block diagram in section 3.4.1).

The following diagrams summarize the four configuration options for the VMEbus Adaptor card when the VMEbus chassis *is not the system controller* (the card may be installed in any slot except slot 1).

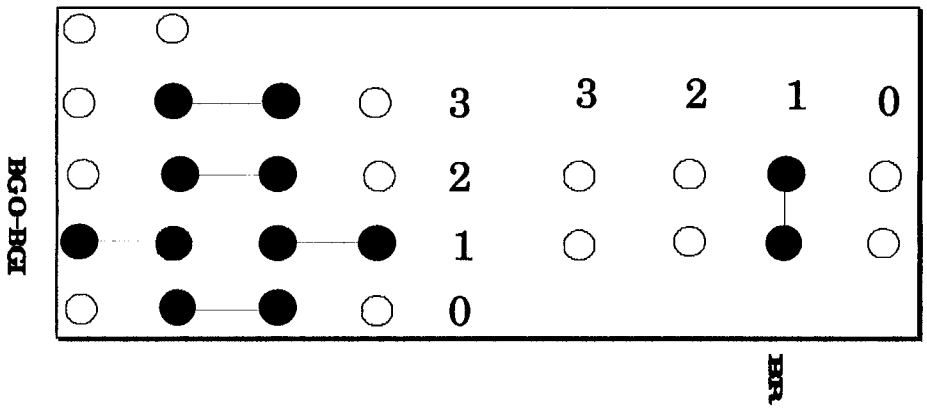
➔ In all four cases, the **Bus Request** level always matches the **Bus Grant Daisy Chain** level.



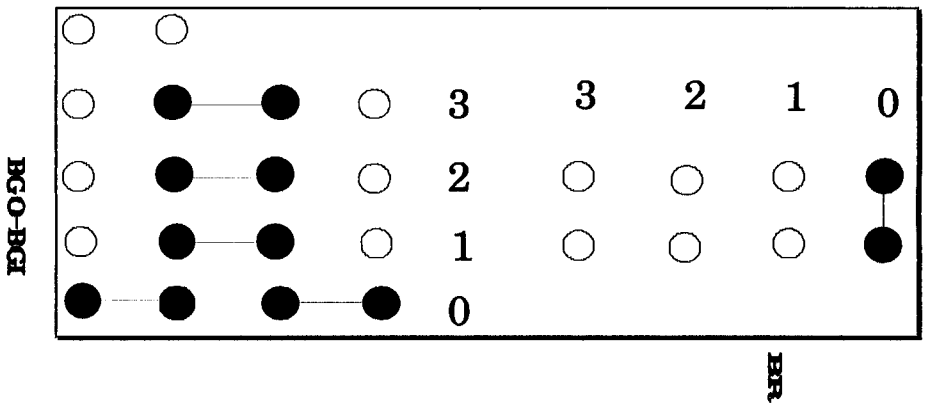
Bus Request 3
(Shipping configuration)



Bus Request 2



Bus Request 1

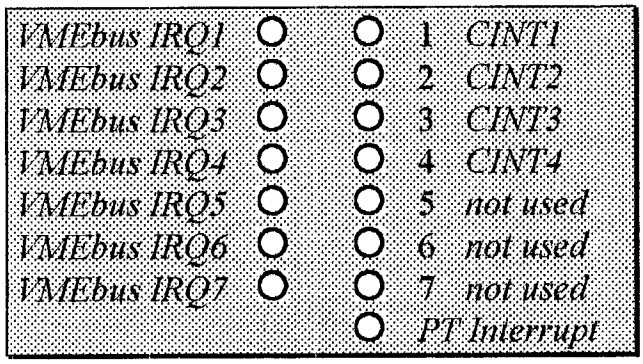


Bus Request 0

3.4.3 Transmitted Interrupt Jumpers

The TINT jumper block is shown here in the shipping configuration:

➔ Jumper IN: ●-------● Jumper OUT: ○ ○



T-INT

Four Cable Interrupt Lines (*CINTx*) can carry interrupts to the SBus

The seven lines (*IRQx*) connect to the VMEbus backpanel interrupts.

This group of jumpers permits selection of interrupts to go across the cable to the SBus Adaptor card. The outbound interrupt may also be the PT interrupt described in section 1.9.4.1.

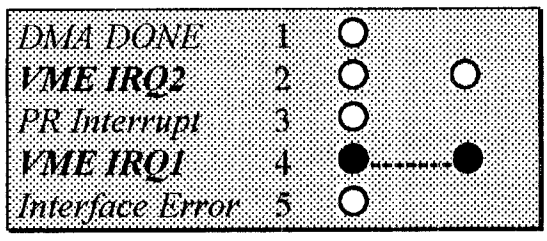
The pins in the left column are the choices for VMEbus interrupts to the SBus. The CINT pins in the right column are the four cable interrupt lines that allow the left-column signals to pass to the SPARCstation.

The PT INTERRUPT pin is for the PT (to SBus) programmed interrupt signal described in section 1.9.4.1. This pin may be connected to any CINTx pin.

3.4.4 Received Interrupt Jumpers

The RINT jumper block is shown here as the card is shipped:

➔ Jumper IN: ●-------● Jumper OUT: ○ ○



R-INT

Not Used (always inactive)

PT Interrupt (in from SBus Adaptor card)

The VMEbus IRQ1 and VMEbus IRQ2 pins, VMEbus backplane interrupt signals, *receive* interrupts from the other five pins in this block. IRQ1 and IRQ2 may be jumpered or wire-wrapped to any of the other five pins to permit them to cause an interrupt on the VMEbus backplane.

Cable interrupt line CINT1 in the right column can be used to bring PT interrupts in from the SBus Adaptor card to the VMEbus processor. The **Interface Error** and **DMA DONE** pins in the left column are available to bring interrupts caused by VMEbus Adaptor card operations to the VMEbus processor. The **PT interrupt** is a programmed interrupt set from the SPARCstation to interrupt a VMEbus processor (see section 1.9.4.1).

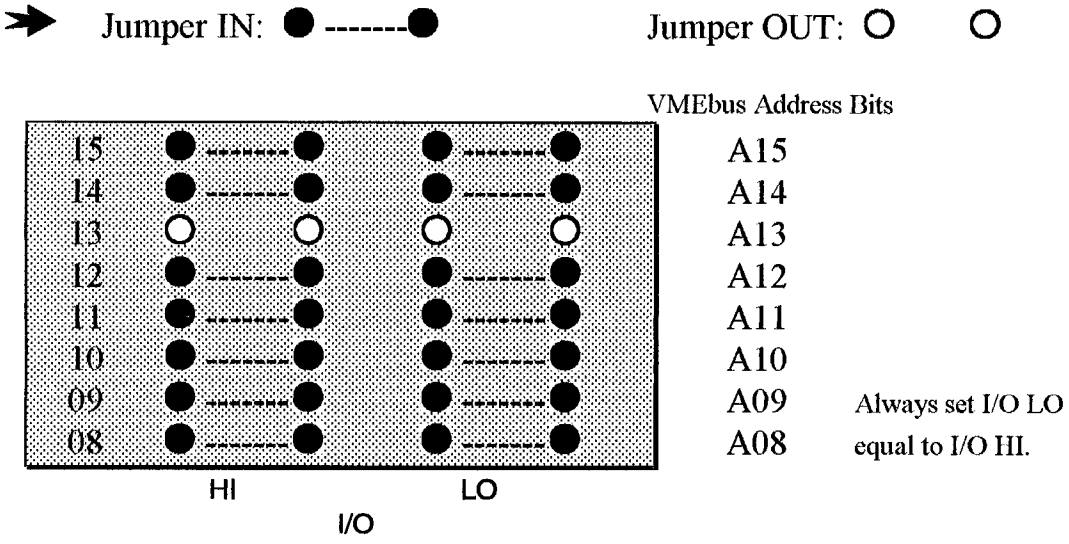
The five interrupt sources (one of the five is not used) in this jumper block are open-collector and more than one may be wire-OR'ed to the VMEbus IRQ1 and IRQ2 pins.

3.4.5 I/O Range Jumpers

The **I/O** jumper block sets the range of the VMEbus Adaptor card in VMEbus I/O space.

The VMEbus Adaptor uses 32 bytes of I/O space. The first 16 bytes are for CSR -- eight for the local and eight for the remote Adaptor card. The next 16 bytes are used for DMA Control and Status Registers -- eight for local and eight for remote DMA registers.

Always set the **I/O LO** and **I/O HI** jumpers to the same setting.



A jumper present (ON) causes the address bit to be "0". A jumper OFF causes the address bit to be "1". The I/O range factory setting is 2000-201F (hex). I/O LO is set equal to I/O HI.

A15 A11	A14 A10	A13 A09	A12: A08:	VME I/O ADDR FIRST HEX DIGIT VME I/O ADDR SECOND HEX DIGIT
ON	ON	ON	ON	0
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

The Adaptor I/O range logic responds to short I/O address modifiers 29 and 2D.

3.4.6 Remote RAM Jumpers

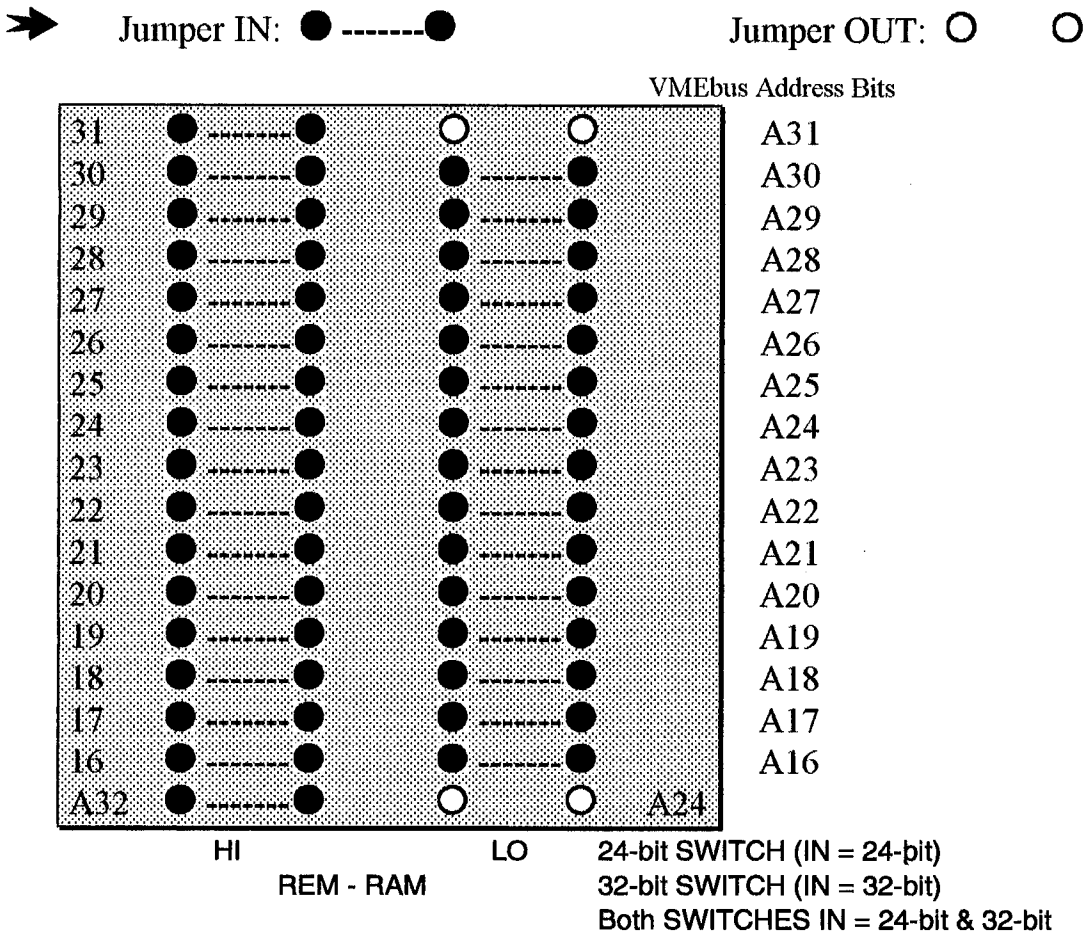
The REM RAM HI and LO jumpers select the starting address and the address range that a VMEbus master references in VMEbus address space to read from or write to memory in the remote (SPARCstation) chassis. The REM RAM LO jumpers set the starting VMEbus address and the REM RAM HI jumpers set the ending address of the memory window. Two additional jumpers (labeled A32 and A24) select whether the card uses 32-bit address space or 24-bit address space.

If the A32 jumper is installed, the window is decoded in VMEbus A32 address space. If the A24 jumper is installed, the window is decoded in A24 address space (bits 24 - 31 are ignored). If both jumpers are installed, the window is present in both A32 and A24 address space.

There cannot be any other VMEbus RAM or Dual Port RAM at the addresses assigned for REM RAM, because there would be two memories addressed at the same location; neither would work properly.

Set the **REM RAM LO** jumpers to the first four digits of the eight-digit hex VMEbus address for the block of memory to be mapped to the SPARCstation. Assume that the remaining four digits of the hexadecimal address are all zeros. Set the **REM RAM HI** jumpers to the first address space after the end of the memory to be mapped to remote RAM. VMEbus address space equal to or greater than the **REM RAM LO** setting and less than the **REM RAM HI** setting is mapped to the SPARCstation.

To disable REM RAM, set **REM RAM HI** less than **REM RAM LO**.



➔ If the A24 jumper is installed, the jumpers for A24 to A31 are ignored for A24 address modifiers.

In 32-bit mode, Adaptor remote RAM responds to address modifiers **09**, **0A**, **0B**, **0D**, **0E**, and **0F**. In 24-bit mode, Adaptor remote RAM responds to address modifiers **39**, **3A**, **3B**, **3D**, **3E**, and **3F**.

The VMEbus can perform D8, D16, and D32 random access to SBus but only D32 Block Mode transfers to SBus RAM.

The factory setting for the remote RAM range is **REM RAM HI** set less than **REM RAM LO**, thereby disabling the remote RAM window.

The jumper table below describes the REM RAM space in hex notation. An address in the 4G byte VMEbus address range may be described as a hex value in the range 0000xxxx-FFFFxxxx.

A31 A27 A23 A19	A30 A26 A22 A18	A29 A25 A21 A17	A28: A24: A20: A16:	FIRST HEX DIGIT SECOND HEX DIGIT THIRD HEX DIGIT FOURTH HEX DIGIT
ON	ON	ON	ON	0
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

VMEbus REM RAM ADDRESS

3.4.7 Dual Port RAM Jumpers

The DUAL PORT HI and LO jumpers select the address range a bus master on the VMEbus references to read or write to Dual Port RAM. The DUAL PORT LO jumper block sets the starting VMEbus address and the DUAL PORT HI selects the ending address. Two additional jumpers (marked A32 and A24) select whether the card responds to 32-bit or 24-bit address space.

If the A32 jumper is installed, the window is decoded in VMEbus A32 address space. If the A24 jumper is installed, the window is decoded in A24 address space (bits 24 - 31 are ignored). If both jumpers are installed, the window is present in both A32 and A24 address space.

The minimum address range is 64K bytes and the maximum is 4G bytes. Set the range to match the size of your Dual Port RAM. If the dual-port memory is less than 64K bytes, set the range to 64K bytes. Make sure no other VMEbus RAM or remote RAM are at the addresses assigned for Dual Port RAM; if two memories are addressed at the same location, neither memory can work properly.

Set the DUAL PORT LO jumpers to the first four digits of the eight-digit hex VMEbus address for the memory block to be mapped to Dual Port RAM. Assume that the remaining four digits of the hexadecimal address are all zeros. Set the DUAL PORT HI jumpers to the first address after the end of the memory to be mapped to the Dual Port RAM. VMEbus address space equal to or greater than the DUAL PORT LO setting and less than the DUAL PORT HI setting is mapped to Dual Port RAM.

If Dual Port RAM is not installed or to disable Dual Port RAM, set the DUAL PORT RAM HI jumpers to a value less than the DUAL PORT RAM LO jumpers.

➔ All dual-port memory cards are designed to ignore unused upper address bits when a large window is used (these bits are still used to determine that access is in the window). Therefore, for a 1M byte Dual Port RAM card, only Address Lines A19-A0 are significant; Address Lines A31-A20 are ignored.

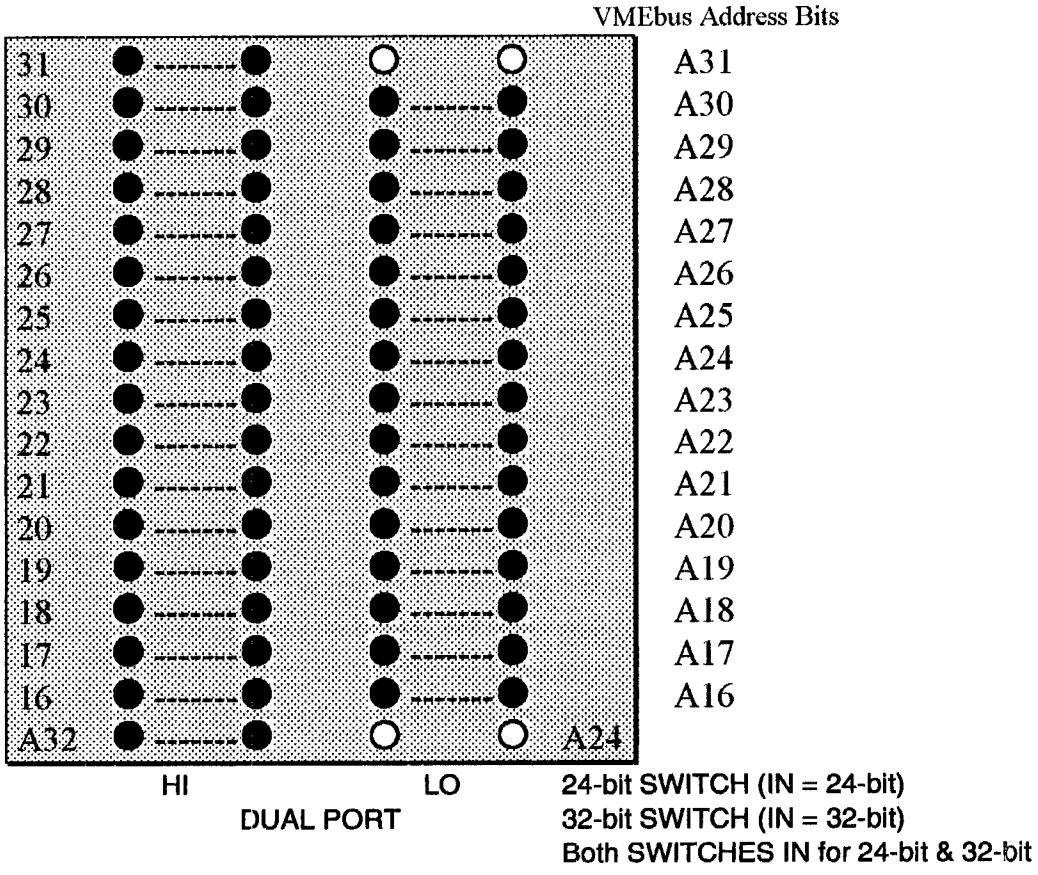
➔ For any size Dual Port RAM, the dual-port window must start at an address that is an integer multiple, starting from address zero, of the selected Dual Port RAM size. Thus, for a 128K byte Dual Port RAM, the window must start on a 128K byte address in the address space; for a 1M byte Dual Port RAM, the window must start on a 1M byte address, and so on.

In 32-bit mode, Dual Port RAM responds to address modifiers **09**, **0A**, **0B**, **0D**, **0E**, and **0F**. In 24-bit mode, Dual Port RAM responds to address modifiers **39**, **3A**, **3B**, **3D**, **3E**, and **3F**.

The Dual Port RAM module can respond to 8-bit, 16-bit, and 32-bit data transfers from the VMEbus.

➔ If the A24 jumper is installed, the jumpers for A24 to A31 are ignored for A24 address modifiers.

➔ Jumper IN: ●-------● Jumper OUT: ○ ○



The factory setting for the Dual Port range is **DUAL PORT HI** set less than **DUAL PORT LO**, thereby disabling the Dual Port RAM window.

The jumper table below describes the Dual Port RAM address space in hex notation. An address in the 4G byte VMEbus address range may be described as a hex value in the range 0000xxxx-FFFFxxxx.

A31 A27 A23 A19	A30 A26 A22 A18	A29 A25 A21 A17	A28: A24: A20: A16:	FIRST HEX DIGIT SECOND HEX DIGIT THIRD HEX DIGIT FOURTH HEX DIGIT
ON	ON	ON	ON	0
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	C
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

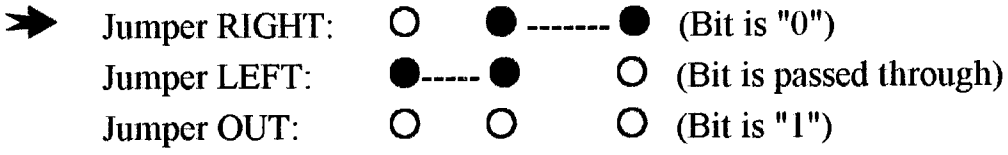
VMEbus DUAL PORT ADDRESS

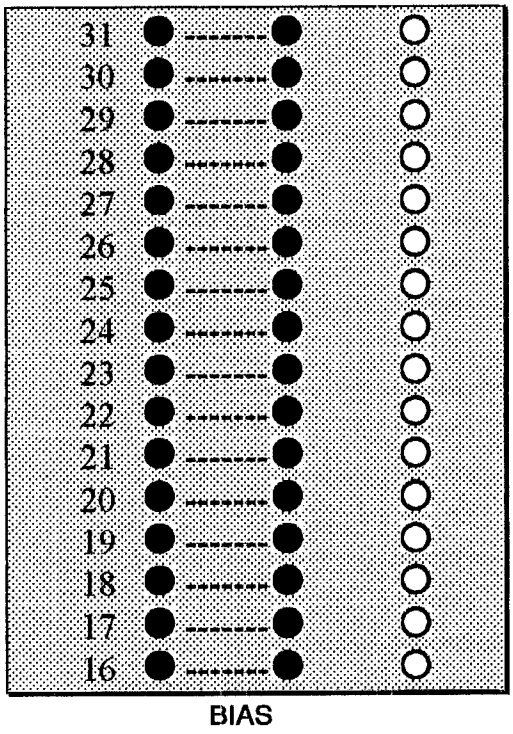
3.4.8 Address Bias Jumpers

The **Address Bias** function is not needed on the Model 467-1 Adaptor. The **Bias** jumpers must always be set to **Pass Through Mode**.

In the **Bias** jumper block, the middle column pins connect through a buffer to drive the VMEbus address lines A31-A16. All right column pins are grounded. The left column pins 16 - 31 are the address bits from the SBus.

The **Bias** factory jumper settings are shown in the diagram on the next page.





Passes A31 to the VMEbus
Passes A30 to the VMEbus
Passes A29 to the VMEbus
Passes A28 to the VMEbus
Passes A27 to the VMEbus
Passes A26 to the VMEbus
Passes A25 to the VMEbus
Passes A24 to the VMEbus
Passes A23 to the VMEbus
Passes A22 to the VMEbus
Passes A21 to the VMEbus
Passes A20 to the VMEbus
Passes A19 to the VMEbus
Passes A18 to the VMEbus
Passes A17 to the VMEbus
Passes A16 to the VMEbus

The jumper positions shown are the factory jumper settings, with address lines A16-A31 to the VMEbus passed through.

3.5 VMEbus Adaptor Card LEDs

There are three green LEDs on the VMEbus Adaptor card:

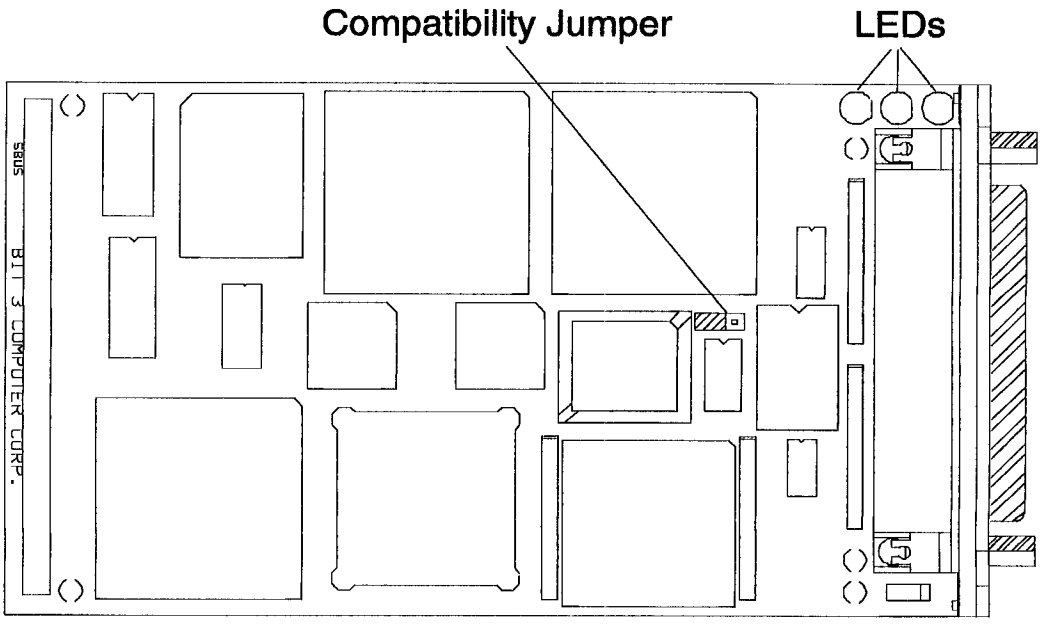
- The LED labeled **READY** is on when the logic arrays on the card are successfully loaded after power-on. *This LED must be on for the card to operate.*
- The LED labeled **REMOTE** is on when the VMEbus Adaptor card is processing a command from the SBus Adaptor card.
- The LED labeled **LOCAL** is on when the VMEbus Adaptor card is being addressed by its local VMEbus chassis. This LED is lit if the Adaptor card recognizes a VMEbus address even if no active cycle (address strobe) is in progress.

Chapter 4: SBus Adaptor Card Configuration

4.0 Introduction

There is only one jumper on the SBus Adaptor card. This jumper is used to configure the Adaptor's compatibility mode. It can be configured to be compatible with the older Model 467 Adaptor or set for Model 467-1 operation. When configured to be compatible with Model 467, window address mapping is disabled. When configured for Model 467-1 operation, Window Mapping Registers are enabled. See also Chapter 6.

4.1 SBus Adaptor Card Diagram



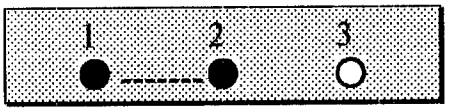
Location of Jumper Blocks and LEDs

4.1.1 Configuration Notes

- The SBus Adaptor card Compatibility configuration jumper is set at the factory to Model 467 Compatibility Mode (jumpered LEFT); Window Mapping Registers are disabled.

4.2 Compatibility Jumper Block

➔ Jumper RIGHT: O ● ------- ● (Bit is "0")
Jumper LEFT: ●----- ● O (Bit is "1")
Jumper OUT: O O O (Bit is "0")



Compatibility

When the jumper is installed LEFT, the Adaptor is set for compatibility with the original Model 467 Adaptor. Window Mapping Registers are disabled.

When no jumper is installed or the jumper is installed RIGHT, the Adaptor is set for the Model 467-1 mode. Window Mapping Registers are enabled.

4.3 SBus Adaptor Card LEDs

There are three green LEDs on the SBus Adaptor card:

- The LED labeled **RDY** is on when the logic arrays on the card are successfully loaded after power-on. *The **RDY** LED must be on for the card to operate.*

- The LED labeled **REM** is on when the SBus Adaptor card is processing a command from the VMEbus Adaptor card or a DMA command.

- The LED labeled **LOC** is on when the SBus Adaptor card is accessed by its local SBus devices.

Chapter 5: Installation

5.0 Caution!

The Adaptor cards are shipped in static-safe packages to protect the components on the cards. It is important that you observe static safety precautions to prevent damage to the cards.

➔ Make sure power is **OFF** before installing cards.

➔ Model 467-1 requires that the SPARCstation has an Open Boot PROM that is at or above revision 2.6. If the PROM is at a lower revision, the system will not be able to boot with the Bit 3 Adaptor card installed. The PROM version is displayed on the console screen each time the SPARCstation is powered up. Contact Sun if you need to upgrade to the current revision of the Open Boot PROM.

5.1 Configure The Adaptor Cards

Any required jumper configuration takes place before the Adaptor cards are installed. Refer to Chapter 3 for information about configuring the VMEbus Adaptor card. See Chapter 4 for information about the SBus Adaptor card's Compatibility Mode configuration jumper.

5.2 Installing The SBus Adaptor Card

➔ SPARCstation 10 (SS10) computers have a thin metal strip connected to the computer's backplane. This strip must be removed from the slot in which the SBus Adaptor card will be installed.

1. Locate a vacant card slot in the SBus chassis. If your SPARCstation has slot 3 designated as a **Slave-Only** slot, *do not* install the SBus Adaptor card in slot 3.
2. Remove the metal plate covering the cable exit at the rear of the chassis.
3. Insert the SBus Adaptor card into the connector.

5.3 Installing The VMEbus Adaptor Card

➔ VMEbus backplanes have jumpers to connect the daisy-chained bus request, bus grant and interrupt acknowledge signals around unused card locations. Make sure that these jumpers are removed from the slot in which the Adaptor card will be installed.

1. Decide if the VMEbus Adaptor card is the system controller. If it is, it must be installed in slot 1.
2. Locate an unoccupied 6U slot in the VMEbus card cage if the Adaptor card is not the system controller.
3. Insert the card into the connector of the selected slot.

5.4 Connecting The Adaptor Cable

The cable connectors on each Adaptor card are connected via I/O cable.

1. Match the **A/B** label on the cable connector to the label above the VMEbus Adaptor card faceplate. The connectors are keyed so that the cables cannot be installed incorrectly.
2. Connect the cable shield wire lug to the VMEbus chassis.
3. Plug the cable connector into its mate on the SBus Adaptor card. (When removing the connectors, lift the retaining clamps -- *do not* pull on the cable.)
4. Secure the cable with the two screws on the cable connector body.

➔ After installation, make sure the green **READY** LEDs on both the SBus and VMEbus Adaptor cards are lit. They must be on for the Adaptor to operate.

Chapter 6: SBus Address Mapping

6.0 SBus Addressing

The SBus uses geographical addressing to address cards residing on its backplane. The bus has 28 address lines and one device select line for each slot. Part of the physical address is presented to each SBus slave device as an individual slot select signal.

A virtual address is used by a SBus master to access a slave device. The virtual address is translated to a physical address by address mapping. Each SBus slot has a unique address range that appears to its installed card as if it starts from address zero. The physical address must be mapped to the virtual address before a VMEbus device can be accessed.

In the SPARCstation (sun4c) implementation, address lines 25 - 27 are not used in a SBus slot. For compatibility, the Adaptor can be configured either in A25 or A28 mode. In A25 mode, the Model 467-1 does not decode these address lines.

The Model 467-1 Adaptor can also be configured in Map Disable mode for backward compatibility with Model 467 Adaptors; see section 6.4.

6.1 SBus Adaptor Window Address Map

The SBus slot space is divided into eight segments. The first segment is used for ROM, node I/O and mapping registers. Other segments are mapped to remote bus or Dual Port RAM. See section 6.1.1 for the address map for A25 mode. See section 6.1.2 for the address map for A28 Mode.

6.1.1 Window Address Map For A25 Mode

The following table summarizes the window address map for the SBus Adaptor card when it is configured in **A25** mode. Only Address lines A0 through A24 are available. These addresses are the offsets from the beginning of a slot space.

	OFFSET IN SLOT SPACE (hex)	WINDOW TYPE	SIZE
(1)	000 0000 - 000 FFFF	Configuration ROM	64K bytes
(*)	001 0000 - 01F FFFF	reserved	
(2)	020 0000 - 020 FFFF	Node I/O	64K bytes
	021 0000 - 021 FFFF	Window Mapping Registers	64K bytes
(*)	030 0000 - 03F FFFF	reserved	
	040 0000 - 07F FFFF	Remote Bus / Dual Port RAM Window 1	4M bytes
	080 0000 - 0BF FFFF	Remote Bus / Dual Port RAM Window 2	4M bytes
	0C0 0000 - 0FF FFFF	Remote Bus / Dual Port RAM Window 3	4M bytes
	100 0000 - 13F FFFF	Remote Bus / Dual Port RAM Window 4	4M bytes
	140 0000 - 17F FFFF	Remote Bus / Dual Port RAM Window 5	4M bytes
	180 0000 - 1BF FFFF	Remote Bus / Dual Port RAM Window 6	4M bytes
	1C0 0000 - 1FF FFFF	Remote Bus / Dual Port RAM Window 7	4M bytes

(1) Configuration ROM contains boot information used by the SPARCstation.

(2) Node I/O contains the SBus and VMEbus Adaptor card Control and Status Registers.

(*) Accesses made to "reserved" regions result in a SBus timeout and require a timeout error handling routine to recover.

6.1.2 Window Address Map For A28 Mode

The following table summarizes the window address map for the SBus Adaptor card when it is configured in **A28** mode. Address lines A0 through A27 are available. These addresses are the offsets from the beginning of a slot space.

	OFFSET IN SLOT SPACE (hex)	WINDOW TYPE	SIZE
(1)	000 0000 - 000 FFFF	Configuration ROM	64K bytes
(*)	001 0000 - 01F FFFF	reserved	
(2)	020 0000 - 020 FFFF	Node I/O	64K bytes
	021 0000 - 021 FFFF	Window Mapping Registers	64K bytes
(*)	030 0000 - 1FF FFFF	reserved	
	040 0000 - 07F FFFF	Remote Bus / Dual Port RAM Window 1	4M bytes
	080 0000 - 0BF FFFF	Remote Bus / Dual Port RAM Window 2	4M bytes
	0C0 0000 - 0FF FFFF	Remote Bus / Dual Port RAM Window 3	4M bytes
	100 0000 - 13F FFFF	Remote Bus / Dual Port RAM Window 4	4M bytes
	140 0000 - 17F FFFF	Remote Bus / Dual Port RAM Window 5	4M bytes
	180 0000 - 1BF FFFF	Remote Bus / Dual Port RAM Window 6	4M bytes
	1C0 0000 - 1FF FFFF	Remote Bus / Dual Port RAM Window 7	4M bytes
(†)	200 0000 - 3FF FFFF	Remote Bus / Dual Port RAM Window 1	32M bytes
(†)	400 0000 - 5FF FFFF	Remote Bus / Dual Port RAM Window 2	32M bytes
(†)	600 0000 - 7FF FFFF	Remote Bus / Dual Port RAM Window 3	32M bytes
(†)	800 0000 - 9FF FFFF	Remote Bus / Dual Port RAM Window 4	32M bytes
(†)	A00 0000 - BFF FFFF	Remote Bus / Dual Port RAM Window 5	32M bytes
(†)	C00 0000 - DFF FFFF	Remote Bus / Dual Port RAM Window 6	32M bytes
(†)	E00 0000 - FFF FFFF	Remote Bus / Dual Port RAM Window 7	32M bytes

(1) Configuration ROM contains boot information used by the SPARCstation.

(2) Node I/O contains the SBus and VMEbus Adaptor card Control and Status Registers.

(*) Accesses made to "reserved" regions result in a SBus timeout and require a timeout error handling routine to recover.

(†) Available in A28 Mode only.

The seven 4M byte windows residing at SBus offset space 040 0000 - 1FF FFFF use the same Mapping Registers as the seven 32M byte windows at SBus offset space 200 0000 - FFF FFFF.

The seven 32M byte windows can only be used if the A28 select bit (bit 6 in the Configuration Control Register) is set. The 32M byte windows ignore Mapping Register bits 8 - 6 that correspond to remote address A26 - A22.

6.2 Window Mapping Registers

The VMEbus Address is formed by a combination of Window Mapping Registers and the SBus slot address. Window Mapping Registers provide the upper address lines and address modifiers for SBus to VMEbus / Dual Port RAM access depending on the window size accessed (32M/4M byte). The registers are accessed as 16-bit words only.

6.2.1 Window Mapping Registers Address Map

OFFSET FROM WINDOW MAPPING REGISTERS TABLE (hex)	REGISTER
00 - 01	reserved
02 - 03	Window 1 Map Register
04 - 05	Window 2 Map Register
06 - 07	Window 3 Map Register
08 - 09	Window 4 Map Register
0A - 0B	Window 5 Map Register
0C - 0D	Window 6 Map Register
0E - 1F	Window 7 Map Register

6.2.1.1 Bit Map For 4M Byte Windows

This is the bit map for Window Mapping Registers 1 - 7 of the 4M byte windows. They define the base VMEbus address and address modifier to be used.

BIT	FUNCTION
15 - 06	Remote Address A31 - A22
05 - 00	VMEbus Address Modifier Codes

➔ The VMEbus address modifier code 0x1X is reserved for Dual Port RAM access.

6.2.1.2 Bit Map For 32M Byte Windows

This is the bit map for Window Mapping Registers 1 - 7 of the 32M byte windows. They define the base VMEbus address and address modifiers to be used.

BIT	FUNCTION
15 - 09	Remote Address A31 - A25
08 - 06	reserved
05 - 00	VMEbus Address Modifier Codes

➔ The VMEbus address modifier code 0x1X is reserved for Dual Port RAM access.

➔ When in A28 mode, a change to a Window Mapping Register will affect both the 4M byte and the 32M byte windows.

6.3 Using Window Address Mapping Feature

➔VMEbus Address Bias jumpers must be passed through when the SBus window mapping feature is used.

To use the Model 467-1 window mapping feature:

1. Set the Compatibility jumper to Window Mode.

2. Set the Window Mode Enable bit in the Configuration Register.

3. Select A25 or A28 mode in the Configuration Register; this will determine the size of each mapping window.

4. Load the Window Mapping Register bit map.

   A25 mode:

   Bits 15 - 6 are the remote address A31 - A22.
   Bits 5 - 0 are VMEbus address modifier codes.

   A28 mode:

   Bits 15 - 11 are the remote address A31 - A27.
   Bits 10 - 6 are reserved.
   Bits 5 - 0 are VMEbus address modifier codes.

6.4 Address Map For Compatibility Mode

The following table summarizes the address map for the Model 467 SBus Adaptor card. These addresses are the offsets from the beginning of a slot space. The offsets are compatible with the original Model 467 Adaptor. The A25/A28 bit has no affect on this address map.

	OFFSET IN SLOT SPACE (hex)	WINDOW TYPE	SIZE
(1)	0000 0000 - 0000 FFFF	Configuration ROM	64K bytes
	0001 0000 - 001F FFFF	not decoded	
(2)	0020 0000 - 0020 FFFF	Node I/O	64K bytes
(*)	0021 0000 - 003F FFFF	reserved	
(3)	0040 0000 - 0040 FFFF	VMEbus I/O (A16)	64K bytes
(*)	0041 0000 - 005F FFFF	reserved	
(3)	0060 0000 - 007F FFFF	VMEbus A24 RAM	2M bytes
	0080 0000 - 00FF FFFF	Dual Port RAM	8M bytes
(3,4)	0100 0000 - 01FF FFFF	VMEbus A24/A32 RAM	16M bytes

(1) Configuration ROM contains boot information used by the SPARCstation.
(2) Node I/O contains the SBus and VMEbus Adaptor card Control and Status Registers.
(3) Enabled by bit 1 in the Configuration Control Register.
(4) A24/A32 mode is selected by Configuration Control Register bit 0.
(*) Accesses made to "reserved" regions result in a SBus timeout and require a timeout error handling routine to recover.

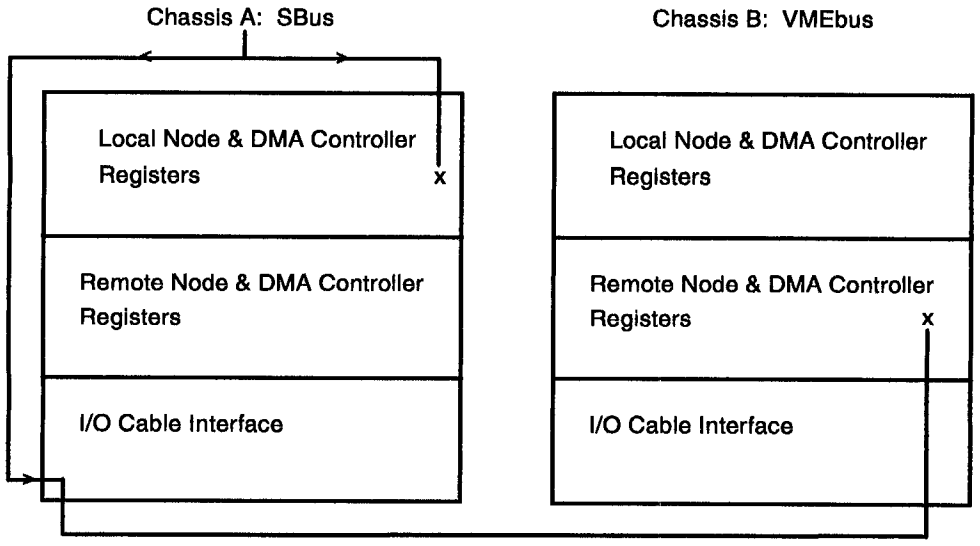
Chapter 7: CSR Registers Accessed From The SBus

7.0 Introduction

Chapter 7 describes SBus Adaptor card Control and Status Registers (CSR). The registers are accessed through SBus node I/O slot space.

The first eight bytes of the SBus Adaptor card I/O space are for a SBus processor to control and check status of the local Adaptor card in the SPARCstation -- the **Adaptor Local Node Registers**. The following eight bytes of the Adaptor I/O space are for a SBus processor to talk to the *remote* (VMEbus) Adaptor card registers -- the **Adaptor Remote Node Registers**.

The final 16 bytes of I/O space are for the SBus to talk to the DMA Controller Registers. Eight bytes comprise the Local Node (SBus) DMA Controller Registers and eight bytes are for the Remote Node (VMEbus) DMA Controller Registers.



I/O Base refers to the Adaptor node I/O window located at offset 020 0000 (hex) from the base of the SBus Adaptor card slot space. The following table shows the destination of Adaptor I/O accesses:

SBus I/O ADDR RANGE (hex)	DESTINATION
I/O Base + 0 - I/O Base + 7	Local Node I/O - SBus
I/O Base + 8 - I/O Base + 0F	Remote Node I/O - VMEbus
I/O Base + 10 - I/O Base + 17	Local DMA - SBus
I/O Base + 18 - I/O Base + 1F	Remote DMA - VMEbus

7.1 Local Node Registers

SBus Local Node Registers are located on the local (SBus) Adaptor card and are addressed by SBus processors.

SBus I/O ADDR (hex)	WRITE FUNCTION	READ FUNCTION
I/O Base + 0	Local Command 1	Local Command 1
I/O Base + 1	Local Command 2	Local Command 2
I/O Base + 2	-- reserved --	Local Status
I/O Base + 3	Configuration Control	Configuration Control
I/O Base + 4	Interrupt Control	Interrupt Control
I/O Base + 5	-- reserved --	-- reserved --
I/O Base + 6	Virtual ADDR Page	Virtual ADDR Page
I/O Base + 7	Virtual ADDR Page	Virtual ADDR Page

7.1.1 Local Node Command Register 1

The Local Node Command Register 1 is a read/write register located on the SBus Adaptor card.

BIT	FUNCTION
7	Clear Status Error (write only)
6	Clear PR Interrupt (write only)
5	Set PT Interrupt
4	reserved -- program to "0"
3	reserved -- program to "0"
2	Error Interrupt Enable
1	reserved -- program to "0"
0	Interrupt Enable

CLEAR STATUS REGISTER ERRORS (bit 7): Communication between the two systems is monitored for cable parity errors, VMEbus error, and interface timeouts (the VMEbus system takes too long to respond). These errors set their corresponding error bits in the Local Node Status Register. The error bit flip-flop stays set until cleared by writing "1" to bit 7. This bit always reads as "0".

CLEAR PR INTERRUPT (bit 6): Writing "1" to this bit clears the PR interrupt flip-flop on the SBus Adaptor card. Bit 6 always reads as "0".

SET PT INTERRUPT (bit 5): Writing "1" to bit 5 sets the PT interrupt flip-flop on the SBus Adaptor card. Writing "0" clears the interrupt flip-flop.

ERROR INTERRUPT ENABLE (bit 2): Must be set to "1" to enable the Adaptor to generate error interrupts. The Interrupt Enable bit (bit 0) must also be set.

INTERRUPT ENABLE (bit 0): Must be set to "1" to enable the SBus Adaptor card to activate a SBus interrupt signal.

7.1.2 Local Node Command Register 2

Local Node Command Register 2 is located on the SBus Adaptor card and is actually the VMEbus Remote Command Register 2 accessed from the SBus side of the Adaptor. See section 8.2.1 for details of the VMEbus Remote Command Register 2.

Before a VMEbus master can access SBus memory, the SBus processor must first allocate memory space on the SBus for the VMEbus master's use. The SPARCstation software driver must obtain this address from the operating system and load the upper bits into the Adaptor Page Register. Also, it must select the page size to use.

Access to Local Node Command Register 2 from the SBus allows the SPARCstation to set the Page Size Register.

7.1.3 Local Node Status Register

The Local Node Status Register is a read-only register located on the SBus Adaptor card.

BIT	FUNCTION
7	Interface Parity Error
6	Remote Bus Error
5	Received Parity Error
4	DMA Error
3	PR Interrupt Pending
2	Interface Timeout
1	LRC Error
0	Remote Power Off or I/O Cable Is Off

INTERFACE PARITY ERROR (bit 7): If an interface parity error occurs on a SBus to VMEbus transfer or on a VMEbus to SBus transfer, bit 7 is set to "1". It is cleared by clear status register.

REMOTE BUS ERROR (bit 6): If a VMEbus bus error (BERR signal) occurs on a SBus to VMEbus transfer, bit 6 is set to "1". It is cleared by **clear status register.**

RECEIVED PARITY ERROR (bit 5): If an interface parity error occurs on a VMEbus to SBus transfer, this bit is set to "1". It is cleared by **clear status register.**

DMA ERROR (bit 4): This bit is set by the SBus Adaptor card if an error acknowledgment or Late Error signal occurs on the SBus when a DMA transfer is in progress.

PR INTERRUPT PENDING (bit 3): This bit is set by the SBus Adaptor card when a Programmed Interrupt is received from the VMEbus. The VMEbus transmits this interrupt by setting the **PR** bit in the SBus Adaptor card's remote-accessed Command Register 1. Bit 3 is cleared by the SBus driver by writing "0" to the **Clear PR Interrupt** bit in the Local Command Register.

INTERFACE TIMEOUT (bit 2): If the VMEbus does not respond to a command from the SBus, an interface timeout occurs and bit 2 is set to "1". It is cleared by **clear status register.**

LRC ERROR (bit 1): Bit 1 is set to "1" if a Longitudinal Redundancy Check detects an error on a DMA transfer. It is cleared by **clear status register.**

REMOTE BUS POWER OFF or I/O CABLE IS OFF (bit 0): Bit 0 is set to "1" when the I/O cable is not active. The I/O cable is detected to be inactive if a valid clock signal is not received from the VMEbus (i.e. when remote power is off or when the cable is disconnected) or if SYSRESET is active on the VMEbus Attempts to communicate with the remote bus at this time will fail and result in interface errors.

7.1.4 Configuration Control Register

The Configuration Control Register is located on the SBus Adaptor card.

BIT	FUNCTION
7	Window Mode Enable
6	SBus A25/A28 Select
5	Receiver Enable
4	Burst Enable
3	Compatibility Mode
2	Burst Data Transfer Size
1	Timeout
0	VMEbus A24/A32 Select

WINDOW MODE ENABLE (bit 7): To emulate the address map of the Model 467 Adaptor, this bit must be set to "0" and the Compatibility Mode jumper installed to enable Compatibility Mode (see section 4.2). To enable the A28/A25 window address map, this bit must be set to "1" and the Compatibility Mode jumper must be set to enable the Window Mapping Registers (see section 4.2).

SBus A25/A28 SELECT (bit 6): This bit selects if the card is in A28 mode (bit 6 set to "1") or A25 mode (bit 6 set to "0").

RECEIVER ENABLE (bit 5): Must be set to "1" to enable VMEbus access to the SBus. This bit must be set if the VMEbus is to be allowed access to SBus Adaptor registers. In applications in which no devices on the VMEbus need access to SBus devices, it is recommended that this bit be cleared to protect system memory.

BURST ENABLE (bit 4): Must be set to "1" to enable the SBus Adaptor card to use Burst Mode transfers to SBus devices during DMA Controller and Block Mode transfers (Slave Mode DMA).

COMPATIBILITY MODE (bit 3): This read-only bit reads the Compatibility Mode jumper setting. When this bit reads as "1", the jumper is set for Compatibility Mode (a mode that is compatible with the Model 467 Adaptor). When this bit reads as "0", the Compatibility Mode jumper is set to Window Mapping Mode. See also Chapter 4 and section 6.4.

BURST DATA TRANSFER SIZE (bit 2): Used to select the data size for SBus Burst Mode transfers. Bit 2 is defined as follows:

BURST SIZE SELECT BIT 2	BURST SIZE
0	16 Bytes
1	32 Bytes

TIMEOUT (bit 1): If this bit is set to "0" (default setting), the Adaptor waits four RETRY cycles before initiating a false acknowledge cycle upon access to an invalid VMEbus address. If set to "1", the Adaptor does not initiate a false acknowledge cycle and the SBus system controller will timeout.

VMEbus A24/A32 SELECT (bit 0): This bit is used only if the Map Register Enable bit (bit 7) is cleared ("0") to emulate the address map mode of the Model 467 Adaptor. See also section 6.4.

7.1.5 Interrupt Control Register

The Interrupt Control Register is located on the SBus Adaptor card.

The SBus has seven open-drain interrupt lines, IntReq (1:7). Because interrupt lines are shared by all bus slaves, each slave must have a register that is readable by the CPU indicating when a slave is generating an interrupt.

Model 467-1 allows for only one IntReq (1:7) to be asserted at any time. The Interrupt Control Register determines which IntReq (1:7) is used to assert the interrupt. It also indicates that the slave is generating an interrupt.

Interrupt Control Register bits are defined as follows:

BIT	FUNCTION
7	Interrupt Level Select
6	Interrupt Level Select
5	Interrupt Level Select
4	Interrupt Pending
3	Latched Cable Interrupt - CINT4
2	Latched Cable Interrupt - CINT3
1	Latched Cable Interrupt - CINT2
0	Latched Cable Interrupt - CINT1

INTERRUPT LEVEL SELECT (bits 7-5): These bits determine which IntReq (1:7) line is asserted.

INTERRUPT LEVEL SELECT BITS	7	6	5	INTREQ
	0	0	0	none
	0	0	1	IntReq (1)
	0	1	0	IntReq (2)
	0	1	1	IntReq (3)
	1	0	0	IntReq (4)
	1	0	1	IntReq (5)
	1	1	0	IntReq (6)
	1	1	1	IntReq (7)

INTERRUPT PENDING (bit 4): Set to "1" when the Adaptor is generating an interrupt.

LATCHED CINT4 (bit 3): Set to "1" when the Adaptor is receiving a cable interrupt on CINT4.

LATCHED CINT3 (bit 2): Set to "1" when the Adaptor is receiving a cable interrupt on CINT3.

LATCHED CINT2 (bit 1): Set to "1" when the Adaptor is receiving a cable interrupt on CINT2.

LATCHED CINT1 (bit 0): Set to "1" when the Adaptor is receiving a cable interrupt on CINT1.

7.1.6 Virtual Address Page Registers

Virtual Address Page Registers are located on the SBus Adaptor card.

The Virtual Address Page Registers are physically the same registers as the VMEbus Remote Page Registers (see section 8.2.4). They can be accessed from the SBus only as a word.

Before a VMEbus master can access SBus memory, the SBus processor must allocate a memory space on the SBus for the VMEbus bus master's use. The SPARCstation device driver must obtain this address from the operating system and load the upper bits into the Adaptor Page Register. It must also select the page size to use.

7.2 Remote Node Registers

Eight Adaptor Remote Node registers are controlled by processors on the SBus chassis, but are located on the *remote* (VMEbus) Adaptor card.

SBus I/O ADDR	WRITE FUNCTION	READ FUNCTION
I/O Base + 8	Remote Command Reg 2	Remote Command Reg 2
I/O Base + 9	Remote Command Reg 1	Remote Node Status Reg
I/O Base + A	ADDR Page HIGH Reg	ADDR Page HIGH Reg
I/O Base + B	ADDR Page LOW Reg	ADDR Page LOW Reg
I/O Base + C	Remote ADDR Modifier	Remote ADDR Modifier
I/O Base + D	-- reserved --	Adaptor ID
I/O Base + E	-- reserved --	IACK Read HIGH Reg
I/O Base + F	-- reserved --	IACK Read LOW Reg

7.2.1 Remote Node Command Register 2

The Remote Node Command Register 2 is located on the VMEbus Adaptor card.

BIT	FUNCTION
7	DMA Controller Pause on 16 Transfers
6	Use ADDR Modifier Register
5	VMEbus Block Mode DMA Operation
4	Disable Passing of Remote Adaptor Card Interrupts
3	Page Size Select Bit 3
2	Page Size Select Bit 2
1	Page Size Select Bit 1
0	Page Size Select Bit 0

DMA CONTROLLER PAUSE ON 16 TRANSFERS (bit 7): Used only during DMA Controller operations to cause the VMEbus Adaptor card DMA Controller to pause after 16 longwords have been transferred. This pause allows other VMEbus masters to get a bus grant more often if a DMA operation is in progress. There is always a pause between 256-byte segments (64 or 128 transfers).

USE ADDR MODIFIER REGISTER (bit 6): This bit is the software-selectable switch analogous to the **Address Modifier** jumper in the VMEbus jumper block. Bit 6 may be enabled by setting it to "1". However, it does not need to be set during a DMA operation since the **Use Address Modifier** function is automatically invoked in DMA.

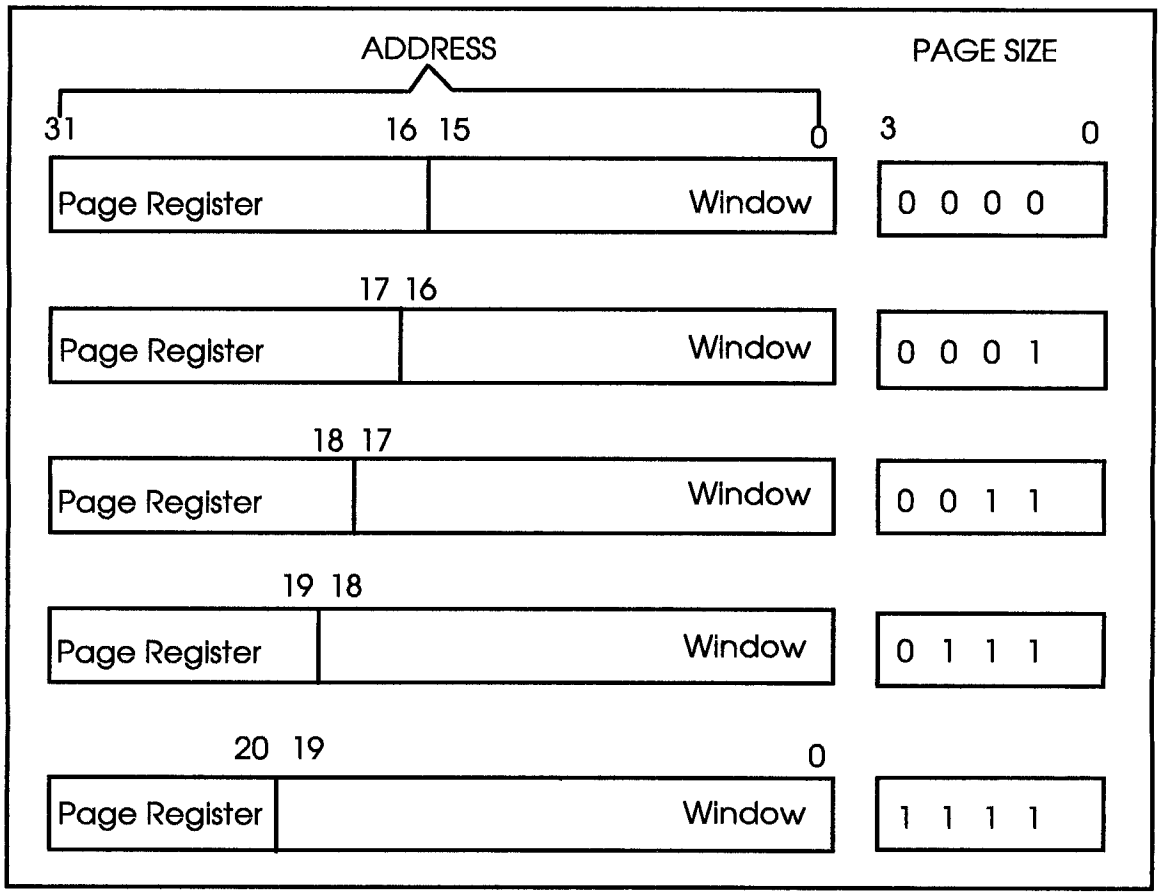
REMOTE BLOCK MODE DMA OPERATION (bit 5): Used during DMA Controller transfers to select Block Mode operation in the VMEbus Adaptor card.

DISABLE REMOTE ADAPTOR CARD INTERRUPT PASSING (bit 4): Writing a "1" to this bit prevents cable interrupts from the VMEbus to the SBus Adaptor card. This bit must be set before starting a DMA transfer from the SPARCstation.

PAGE SIZE SELECT (bits 0-3): The Remote Node Command Register 2 controls the size of the Page Mode window into VMEbus address space. These bits are not used in the Model 467-1 configuration. The default page window size, after the Adaptor card is reset, is 64K bytes. The Page Size Select bits are set as follows:

PAGE SIZE SELECT BIT:	3	2	1	0	PAGE SIZE
	0	0	0	0	64K byte
	0	0	0	1	128K byte
	0	0	1	1	256K byte
	0	1	1	1	512K byte
	1	1	1	1	1M byte

As the page size increases, more address bits from the SBus are passed to the VMEbus and fewer low order Page Register bits (16 - 19) are used.



➔ For any page size used, the Dual Port and remote RAM windows must start at an address that is an even multiple, starting from zero, of the selected page window size. For example, for a 64K byte window size, an offset XXX 0000 (hex) should be used in the mmap() routine.

7.2.2 Remote Node Command Register 1

Remote Node Command Register 1 is a write-only register located on the VMEbus Adaptor card.

BIT	FUNCTION
7	Reset VMEbus Card (one-shot, allow 1 sec)
6	Clear PT Interrupt Flip-Flop on VMEbus Card
5	Set PR Interrupt Flip-Flop on VMEbus Card
4	Lock VMEbus
3	Use Address Page Register
2	IACK Read Mode Address Bit 2
1	IACK Read Mode Address Bit 1
0	IACK Read Mode Address Bit 0

RESET VMEbus ADAPTOR Card (bit 7): The Adaptor card has a power-on-reset circuit that resets the Model 467-1 Adaptor when power is applied to the chassis. This reset may also be activated from the SPARCstation by writing a "1" to this bit. After triggering the reset, your program should wait one second before starting another remote access or VMEbus cycle.

Writing a "0" to this bit clears the **VMEbus Was Reset** flag in the Remote Node Status Register.

If the **SYSRESET** jumper in the **SYS** jumper block is installed, this reset also drives the VMEbus global reset signal. See section 3.4.1 for more information about the **SYS** jumper block.

CLEAR PT INTERRUPT ON VMEbus CARD (bit 6): If a VMEbus processor sets the PT interrupt flip-flop on the VMEbus Adaptor card, a SBus processor can clear it by writing a "1" to bit 6.

SET PR INTERRUPT ON VMEbus CARD (bit 5): A SBus processor sends a PR interrupt to the VMEbus chassis by writing a "1" to bit 5. Writing a "0" has no effect.

LOCK BUS (bit 4): Writing a "1" to bit 4 sets the Lock Bus flip-flop. If the Lock Bus flip-flop is set, the address strobe signal on the VMEbus remains active after the first VMEbus access to the VMEbus. This prevents any other VMEbus bus master from using the bus and permits the SBus to convert a read operation followed by a write operation into an atomic read-modify-write on the VMEbus.

To use this function, the SPARCstation user should set the Lock Bus flip-flop and perform a read followed by a write (to the same address on the VMEbus). Then, quickly clear the Lock Bus flip-flop.

The Lock Bus function is useful in multi-processor applications where processors often signal availability of a resource through an indivisible read-modify-write semaphore operation.

The Lock Bus flip-flop may also be used by the SBus to make accesses to Dual Port RAM indivisible.

Read-modify-write operations (such as TAS: test and set) from the VMEbus to Dual Port RAM are automatically indivisible.

USE ADDRESS PAGE REGISTER (bit 3): This bit must be set low for the Model 467-1 configuration.

IACK READ MODE ADDRESS BITS (bits 2-0): These bits indicate the interrupt level (1-7) being acknowledged when performing an IACK Read function. See also section 1.10.

7.2.3 Remote Node Status Register

The Remote Node Status Register is a read-only register located on the VMEbus Adaptor card.

BIT	FUNCTION
7	VMEbus Was Reset
6	IACK Read Mode Address Bit 1
5	PR Interrupt Flip-Flop Is Set (on VMEbus card)
4	Lock Bus Not Set (the *inverted* state of the Lock Bus flip-flop)
3	Use Address Page Register
2	IACK Read Mode Address Bit 2
1	PT Interrupt Flip-Flop Is Set (on VMEbus card)
0	IACK Read Mode Address Bit 0

VMEbus WAS RESET (bit 7): Set to "1" when SYSRESET occurs; cleared when "0" is written to Remote Node Command Register 1 bit 7.

IACK READ MODE ADDRESS BIT 1 (bit 6): Shows the state of the IACK Read Mode Address Bit 1 written to the Remote Node Command Register. This bit and bits 2 and 0 are non-contiguous to maintain compatibility with previous Bit 3 Adaptor models.

PR INTERRUPT FLIP-FLOP IS SET (bit 5): Bit 5 is "1" when the PR interrupt flip-flop on the VMEbus Adaptor card is set.

LOCK BUS NOT SET (bit 4): Shows the *inverted* state of the Lock Bus flip-flop controlled by bit 4 of the Remote Node Command Register 1.

USE ADDRESS PAGE REGISTER (bit 3): Shows the state of the **Use Address Page Register** control bit written in Remote Node Command Register 1.

IACK READ MODE ADDRESS BIT 2 (bit 2): Shows the state of the IACK Read Mode Address Bit 2 written to Remote Node Command Register 1.

PT INTERRUPT FLIP-FLOP IS SET (bit 1): This bit is "1" when the PT interrupt flip-flop on the VMEbus Adaptor card is set.

IACK READ MODE ADDRESS BIT 0 (bit 0): Shows the state of the IACK Read Mode Address Bit 0 written to Remote Node Command Register 1.

7.2.4 VMEbus Page Registers

➔ These registers are used only when the Adaptor is set in Map Disable mode. They are not used in the Model 467-1 configuration.

The read/write VMEbus Page Registers are located on the VMEbus Adaptor card; they may be accessed as a word or individually as bytes.

BIT	FUNCTION	
7	VMEbus Address Bit 31	
6	VMEbus Address Bit 30	
5	VMEbus Address Bit 29	
4	VMEbus Address Bit 28	Address Page HIGH
3	VMEbus Address Bit 27	
2	VMEbus Address Bit 26	
1	VMEbus Address Bit 25	
0	VMEbus Address Bit 24	
7	VMEbus Address Bit 23	
6	VMEbus Address Bit 22	
5	VMEbus Address Bit 21	
4	VMEbus Address Bit 20	Address Page LOW
3	VMEbus Address Bit 19	
2	VMEbus Address Bit 18	
1	VMEbus Address Bit 17	
0	VMEbus Address Bit 16	

The VMEbus Page Registers are gated to the VME address bus when the **Use Address Page Register** command bit is set. The two registers together provide the upper 16 address bits of a 32-bit Dual Port or VMEbus RAM address.

The Address Page LOW Register provides the upper eight address bits of a 24-bit Dual Port or VMEbus RAM address when accessing memory in 24-bit mode.

In the case of Dual Port RAM, the Dual Port RAM card ignores any address bits larger than the size of the memory. For example, for a 1M byte Dual Port RAM card, only A16 - A19 are significant. Setting the Page Register with a value of F0xxxx or 00xxxx results in the exact same section of dual-port memory being accessed.

7.2.5 Address Modifier Register

VMEbus addresses consist of 16, 24, or 32 address bits and a 6-bit address modifier.

The Address Modifier Register is a read/write register located on the VMEbus Adaptor card. It allows a SBus processor to select the VMEbus address modifier code used during a DMA Controller operation. The Address Modifier Register also provides the VMEbus address modifier code during random access cycles if the **Use Address Modifier** jumper or CSR bit is enabled.

BIT	FUNCTION
7	Not Defined - must be "0"
6	Not Defined - must be "0"
5	VMEbus Address Modifier Bit 5
4	VMEbus Address Modifier Bit 4
3	VMEbus Address Modifier Bit 3
2	VMEbus Address Modifier Bit 2
1	VMEbus Address Modifier Bit 1
0	VMEbus Address Modifier Bit 0

When the Address Modifier Register is not enabled, the SBus Adaptor card provides an address modifier from the Window Mapping Registers.

Definitions for the various address modifiers may be found in a published VMEbus specification. See section 2.4 for names and availability of publications.

7.2.6 Adaptor ID Register

A byte read of the Adaptor ID Register returns the hex value **80** that identifies the card on the other end of the cable as a Model 467-1 VMEbus Adaptor card.

7.2.7 Remote Node IACK Read Register

When a VMEbus device interrupts the SBus, the VMEbus interrupt must be acknowledged and an interrupt vector read from the VMEbus. The interrupt vector is not used directly on the SBus (as it would be on a VMEbus system) to point to an interrupt handler, but could be used by the SBus to identify the original VMEbus interrupter.

A SBus processor can instruct the Adaptor to perform an interrupt acknowledge cycle on the VMEbus by reading from the IACK Read Register. The Adaptor converts a read from these registers (in the SPARCstation) into a remote interrupt acknowledge cycle (on the VMEbus chassis), activating the VMEbus IACK line and presenting a 3-bit IACK code corresponding to the interrupt level being acknowledged. When the VMEbus interrupting device sees the acknowledgment, it posts an interrupt vector on the VMEbus that is returned to the SBus processor performing the read of the IACK Read Register.

The IACK Read Register is a read-only register located on the VMEbus Adaptor card. The register is addressed as a word. Only the lower byte contains data; the upper byte should be masked off.

Two IACK Reads cause *two* IACKs to occur; the second read induces a VMEbus bus error. The 3-bit IACK code presented by the VMEbus Adaptor card is set by writing to Remote Node Command Register 1 bits 2-0. See also section 7.2.2.

7.3 DMA Controller Registers

This section covers the DMA Controller Registers accessed from the SBus. Refer to section 1.7 for additional information about DMA. DMA Controller Registers accessed from VMEbus are discussed in Chapter 8.

7.3.1 DMA Controller And Error Status Registers Accessed From The SBus

The DMA Controller Registers listed in the table below are located on the local (SBus) Adaptor card and are accessed by a SBus processor to initiate a DMA Controller operation.

SBus I/O ADDR (hex)	WRITE FUNCTION	READ FUNCTION
I/O Base + 10	Local DMA Command	Local DMA Command
I/O Base + 11	DMA Packet Remainder	DMA Packet Remainder
I/O Base + 12	DMA SBus ADDR 24-31	DMA ADDR 24-31
I/O Base + 13	DMA SBus ADDR 16-23	DMA ADDR 16-23
I/O Base + 14	DMA SBus ADDR 8-15	DMA ADDR 8-15
I/O Base + 15	DMA SBus ADDR 0-7	DMA ADDR 0-7
I/O Base + 16	DMA Packet Count 16-23	DMA Packet Count 16-23
I/O Base + 17	DMA Packet Count 8-15	DMA Packet Count 8-15

The DMA Controller Registers outlined in the following table are located on the remote (VMEbus) Adaptor card and are accessed by a SBus processor to initiate a DMA Controller operation.

SBus I/O ADDR (hex)	WRITE FUNCTION	READ FUNCTION
I/O Base + 18	-- reserved --	-- reserved --
I/O Base + 19	DMA Packet Remainder	DMA Packet Remainder
I/O Base + 1A	DMA VME ADDR 24-31	DMA VME ADDR 24-31
I/O Base + 1B	DMA VME ADDR 16-23	DMA VME ADDR 16-23
I/O Base + 1C	DMA VME ADDR 8-15	DMA VME ADDR 8-15
I/O Base + 1D	DMA VME ADDR 0-7	DMA VME ADDR 0-7
I/O Base + 1E	-- reserved --	-- reserved --
I/O Base + 1F	Error Status	Error Status

7.3.2 Local DMA Controller Command Register

The Local DMA Controller Command Register is located on the SBus Adaptor card.

BIT	FUNCTION
7	Start DMA (read/write)
6	Remote RAM/Dual Port RAM Select
5	DMA Transfer Direction (read/write)
4	DMA Transfer Size Word/Longword Select
3	reserved -- must be programmed to "0"
2	Enabled DMA Done Interrupt (read/write)
1	DMA Done Flag (read/write)
0	reserved -- must be programmed to "0"

START DMA (bit 7): Writing "1" to bit 7 starts a DMA Controller operation. This bit should be set only after all other DMA Controller registers are ready.

REMOTE RAM/DUAL PORT RAM SELECT (bit 6): Writing "1" to bit 6 causes the DMA Controller to transfer data between the SBus and Dual Port RAM. Writing "0" causes a transfer between SBus and VMEbus memory.

DMA may only occur between local and remote memory; not between VMEbus memory and Dual Port RAM.

DMA TRANSFER DIRECTION (bit 5): Writing "1" to bit 5 causes the DMA Controller to transfer data from SBus RAM to VMEbus RAM. Writing "0" causes a data transfer from VMEbus RAM to SBus RAM.

DMA TRANSFER SIZE WORD/LONGWORD SELECT (bit 4): Writing "1" to bit 4 causes the DMA Controller to perform longword (32-bit) data transfers on the VMEbus. Writing "0" causes word (16-bit) data transfers on the VMEbus. This bit must be set.

ENABLE DMA DONE INTERRUPT (bit 2): Writing "1" to bit 2 activates the DMA DONE interrupt on the SBus Adaptor card at the completion of a DMA operation. Switching this bit permits software control (masking) of the DMA DONE interrupt.

The Interrupt Enable bit in the Local Node Command Register must also be set in order for the DMA DONE interrupt to occur.

DMA DONE FLAG (bit 1): Bit 1 presents the status of a DMA operation to software in the same manner as the DMA DONE interrupt does for the hardware. It clears itself when a new DMA operation begins. Writing "0" to bit 1 also clears the DMA DONE status.

An error during a DMA Controller transfer stops the operation and sets the DMA Done Flag. Software should check for errors after the DMA operation to make sure the operation terminated successfully.

7.3.3 DMA Controller Packet Remainder Register

The DMA Controller Packet Remainder Register is an 8-bit read/write register located on the SBus Adaptor card.

Before starting a DMA transfer, the DMA Controller Packet Remainder Register is loaded with the lowest eight bits of the number of bytes to be transferred by the DMA Controller. The value in this register must be a multiple of 4 bytes. The same value must also be loaded in the VMEbus DMA Controller Packet Remainder Register. See also section 7.3.7.

7.3.4 SBus DMA Controller Address Register

The Local DMA Controller Address Register, located on the SBus Adaptor card, is found at node I/O locations 12 - 15 hex. The register's four bytes are loaded before starting the DMA Controller operation with the first SBus address to be accessed. As the DMA Controller operation progresses, the contents of the register increment by four for longword operations. An I/O read of this register during DMA produces the address count at that time in the DMA (the next address to be accessed).

The four bytes that form the SBus DMA Controller address must be accessed in word-wide (16-bit) operations. SBus DMA Controller address bit 31 (written to bit 7 of I/O location 12) is the most significant bit of the address; bit 0 (written to bit 0 of I/O location 15) is the least significant address bit.

The SBus address must be longword-aligned; the lowest two bits of the address counter must be "0".

7.3.5 DMA Controller Packet Count Register

The DMA Controller Packet Count Register, a 16-bit read/write word- or byte-addressable register located on the SBus Adaptor card, is found at node I/O locations 16 - 17 hex.

Before starting the DMA, this register is loaded with the number of packets (one packet equals 256-bytes) to be transferred by the DMA Controller. As the DMA operation progresses, the contents of the register decrement for every 256 bytes of data transferred.

The bits in the DMA Controller Packet Count Register are numbered as though it was a 24-bit register. However, you can access only the most significant 16 bits (bits 08-23). The lowest eight bits are in the DMA Controller Packet Remainder Register.

DMA Controller Packet Counter bit 23 (written to bit 7 of I/O location 17) is the most significant bit of the counter.

DMA Controller Packet Count Register bits 8-23 also may be viewed as the number of 256-byte packets of data to be transferred.

7.3.6 DMA Controller VMEbus Address Registers

The DMA Controller VMEbus Address Registers are located on the VMEbus Adaptor card.

The 4-byte DMA Controller VMEbus Address Registers are loaded by the user (before starting the DMA) with the first address to be accessed. As the DMA operation progresses, the contents of the registers increment by four for longword operations.

The four I/O bytes that make up the DMA VMEbus address may be written to in byte-wide or word-wide I/O operations. DMA VMEbus address bit 31 (written to bit 7 of I/O location 1A) is the most significant bit of the address. DMA VMEbus address bit 0 (written to bit 0 of I/O location 1D) is the least significant address bit.

The VMEbus address must be longword-aligned; the lowest two bits of the VMEbus address must be "0".

If the remote DMA memory is Dual Port RAM, the lowest-order 15, 17, or 20 bits in the address counter are used to access the 32K byte, 128K byte, 1M byte, 2M byte, 4M byte, or 8M byte Dual Port RAM. The upper bits in the DMA Controller VMEbus Address Registers, beyond the size of the Dual Port RAM, should be set to "0".

➔ You should not load the DMA Controller VMEbus Address Registers with the address of the dual-port window on the VMEbus.

➔ The SBus processor or a VMEbus master should never attempt to read remote I/O registers, remote bus I/O, or remote bus RAM during a DMA Controller operation.

7.3.7 DMA Controller Packet Remainder Register

The DMA Controller Packet Remainder Register is located on the VMEbus Adaptor card.

Before starting DMA, the DMA Controller Packet Remainder Register is loaded with the lowest eight bits of the number of bytes to be transferred by the Adaptor DMA Controller. The value in this register must be a multiple of 4 bytes.

The same value must also be written to the DMA Controller Packet Remainder Register on the SBus Adaptor card. See also section 7.3.3.

7.3.8 Error Status

A read of the Error Status Register (I/O Base + 1F) provides the same information to the SBus as a read of the Local Node Status Register from the VMEbus. See section 8.1.2.

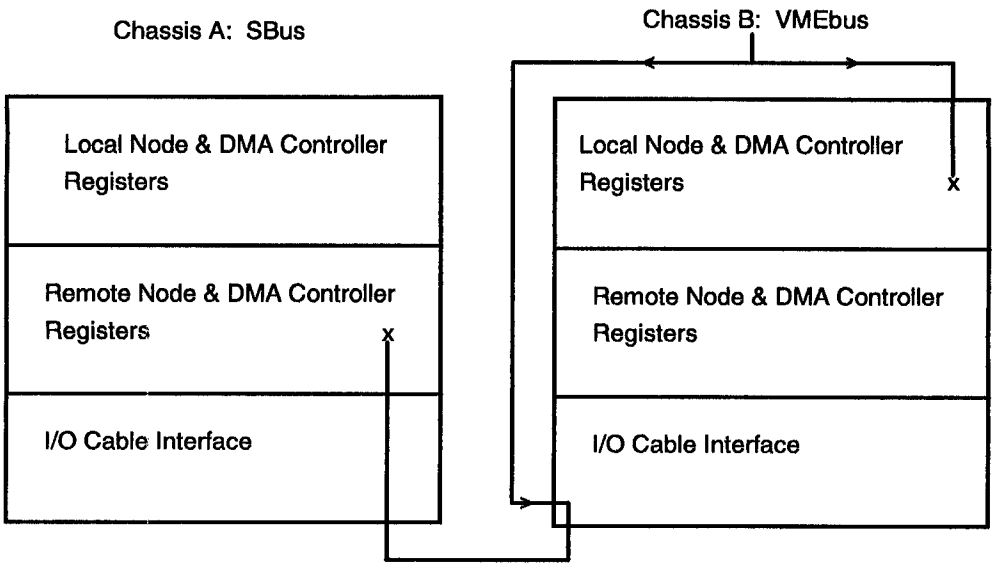
A write to this register (I/O Base + 1F) with data bit 7 set clears the status errors. It provides the same function as a write by the VMEbus to bit 7 of the Local Node Command Register. See section 8.1.1.

Chapter 8: CSR Registers Accessed From The VMEbus

8.0 Introduction

Chapter 8 describes the VMEbus Adaptor card Control and Status Registers (CSR). These registers are accessed by a VMEbus master through I/O space selected with the **I/O HI** and **I/O LO** jumpers on the VMEbus Adaptor card.

The first eight bytes of the VMEbus Adaptor card's I/O space are for a VMEbus processor to talk to *its* Adaptor **Local Node Registers**. The second eight bytes are for the VMEbus processor to talk to its **Remote Node** (SBus) **Registers**. The next eight bytes of the I/O space are for the VMEbus to talk to the **Local Node** (VMEbus) **DMA Controller Registers**. The final eight bytes comprise the **Remote Node** (SBus) **DMA Controller Registers**.



8.1 Local Node Registers

The following table shows the location and definition of the first eight bytes of I/O on the VMEbus Adaptor card. These registers are addressed by processors on the VMEbus.

VMEbus I/O ADDR (hex)	WRITE FUNCTION	READ FUNCTION
I/O LO + 0	-- reserved --	-- reserved --
I/O LO + 1	Local Node Command	Local Node Command
I/O LO + 2	-- reserved --	-- reserved --
I/O LO + 3	-- reserved --	Local Node Status
I/O LO + 4	Address Modifier	Address Modifier
I/O LO + 5	-- reserved --	-- reserved --
I/O LO + 6	-- reserved --	-- reserved --
I/O LO + 7	Interrupt Vector	Interrupt Vector

8.1.1 Local Node Command Register

The VMEbus Local Node Command Register is a read/write register located on the VMEbus Adaptor card.

BIT	FUNCTION
7	Clear Status Register Errors
6	Clear PR Interrupt Flip-Flop On The VMEbus Adaptor Card
5	Set PT Interrupt Flip-Flop On The VMEbus Adaptor Card
4	Disable All Interrupts From The Adaptor Card to the VMEbus
3	Not Defined - must be "0"
2	Disable All Interrupts From The VMEbus to the Adaptor Card
1	Not Defined - must be "0"
0	Not Defined - must be "0"

CLEAR STATUS REGISTER ERRORS (bit 7): Communication errors are indicated by the Local Node Status Register. Error bits stay set until cleared by writing "1" to bit 7. However, this bit will automatically clear and will not be set when the Local Node Command Register is read.

CLEAR PR INTERRUPT FLIP-FLOP (bit 6): Writing "1" to this bit clears the PR interrupt flip-flop on the VMEbus Adaptor card.

SET PT INTERRUPT FLIP-FLOP (bit 5): Writing "1" to bit 5 sets the PT interrupt flip-flop on the VMEbus Adaptor card. Writing "0" clears this interrupt.

DISABLE ALL INTERRUPTS FROM THE ADAPTOR CARD TO THE VMEbus (bit 4): If bit 4 is set to "1", the Adaptor card cannot pass interrupts to the VMEbus backplane.

DISABLE ALL INTERRUPTS FROM THE VMEbus TO THE ADAPTOR CARD (bit 2): Set bit 2 to "1" prior to a DMA Controller operation to block interrupts during the DMA transfer. Clear this bit after the DMA Controller operation is completed.

8.1.2 Local Node Status Register

The Local Node Status Register is a read-only register located on the VMEbus Adaptor card.

BIT	FUNCTION
7	Interface Parity Error
6	Remote Node Bus Error
5	PR Interrupt Flip-Flop Is Set (on the VMEbus Adaptor card)
4	Not Defined - reserved for future use
3	LRC Error (DMA master only)
2	Interface Timeout (DMA only)
1	PT Interrupt Flip-Flop Is Set (on the VMEbus Adaptor card)
0	Remote Bus Power Off or I/O Cable Is Off

INTERFACE PARITY ERROR (bit 7): Set to "1" if an interface parity error occurs on a chassis-to-chassis transfer.

REMOTE NODE BUS ERROR (bit 6): This bit is "1" if an error acknowledgment or Late Error Signal occurs on the SBus for VMEbus initiated transfers.

PR INTERRUPT FLIP-FLOP IS SET (bit 5): Set to "1" when the PR interrupt flip-flop on the VMEbus Adaptor card is set by a SBus processor.

LRC ERROR (bit 3): Bit 3 is set to "1" if a Longitudinal Redundancy Check detects an error on a DMA transfer.

INTERFACE TIMEOUT (bit 2): A DMA Controller interface timeout occurs when a packet transfer is unable to complete within 16 msec.

PT INTERRUPT FLIP-FLOP IS SET (bit 1): Set to "1" when the PT flip-flop on the VMEbus Adaptor card is set.

REMOTE BUS POWER OFF or I/O CABLE IS OFF (bit 0): Bit 0 is "1" if the SBus power is off or if the I/O cable is not connected. If this bit is "1", attempts to communicate with the SBus result in interface errors.

8.1.3 Address Modifier Register

This read/write register is always used during Adaptor DMA Controller operations to present an appropriate address modifier to the VMEbus. The Address Modifier Register is located on the VMEbus Adaptor card.

The register is loaded, before starting the DMA Controller operation, with an address modifier signaling the proper address width and transfer mode to the VMEbus.

8.1.4 Interrupt Vector Register

This read/write register located on the VMEbus Adaptor card holds the interrupt vector transmitted to a VMEbus processor when an interrupt is acknowledged. The interrupt vector is the response to an interrupt caused by the VMEbus Adaptor card *or* to an interrupt passed from the SBus Adaptor card *through* the VMEbus Adaptor card (such as PT or PR interrupts).

If the VMEbus Adaptor card sends an interrupt, it passes the contents of the Interrupt Vector Register to the local VMEbus processor during the interrupt acknowledge cycle.

The Interrupt Vector Register is preset to FF at power-on time and is read from and written to by a VMEbus processor -- *not* by a SBus processor.

8.2 Remote Node Registers

These eight registers are controlled by processors on the VMEbus, but are located on the *remote* (SBus) Adaptor card.

VMEbus I/O ADDR (hex)	WRITE FUNCTION	READ FUNCTION
I/O LO + 8	Remote Command Reg. 2	Remote Command Reg. 2
I/O LO + 9	Remote Command Reg. 1	Remote Status
I/O LO + A	Address Page High	Address Page High
I/O LO + B	Address Page Low	Address Page Low
I/O LO + C	-- reserved --	Adaptor ID
I/O LO + D	-- reserved --	-- reserved --
I/O LO + E	-- reserved --	-- reserved --
I/O LO + F	-- reserved --	-- reserved --

8.2.1 Remote Node Command Register 2

Remote Node Command Register 2 is a read/write register located on the SBus Adaptor card. See also section 7.1.6 for information on SBus Virtual Page Registers.

BIT	FUNCTION
7	reserved -- program to "0"
6	reserved -- program to "0"
5	reserved -- program to "0"
4	Disable PT Interrupt From The SBus (set by the VMEbus processor during DMA)
3	Page Size Select Bit 3
2	Page Size Select Bit 2
1	Page Size Select Bit 1
0	Page Size Select Bit 0

This register controls the size of the page window into SBus address space. The default page window size (after the Adaptor card is reset) is 64K bytes.

DISABLE PT INTERRUPT (bit 4): The VMEbus processor should set this bit to "1" before starting a DMA transfer; it should set this bit to "0" after receiving the DMA DONE signal.

PAGE SIZE SELECT BITS (bits 3-0): These bits are set as follows:

PAGE SIZE SELECT BIT:	3	2	1	0	PAGE SIZE
	0	0	0	0	64K byte
	0	0	0	1	128K byte
	0	0	1	1	256K byte
	0	1	1	1	512K byte
	1	1	1	1	1M byte

For any page size used, the SBus RAM window must start at an address that is an even multiple, starting from address zero, of the selected page window size. Thus, for a 64K byte page window size, the window must start on a 64K byte address in SBus address space; for a 128K byte page window, the window must start on a 128K byte address, etc.

Example: If a 128K byte page size is selected, the Page Register supplies address bits A17 through A31 to the SBus, and the VMEbus supplies bits A0 through A16. As the page size increases, the Page Register supplies fewer address bits and the VMEbus supplies more bits.

8.2.2 Remote Node Command Register 1

Remote Node Command Register 1 is a write-only register located on the SBus Adaptor card.

BIT	FUNCTION
7	reserved
6	Clear PT Interrupt
5	Set PR Interrupt
4	reserved
3	reserved
2	reserved
1	reserved
0	reserved

CLEAR PT INTERRUPT (bit 6): If a SPARCstation processor set the PT interrupt flip-flop on the SBus Adaptor card, a VMEbus processor can clear it by writing a "1" to bit 6 of the Remote Node Command Register 1.

SET PR INTERRUPT (bit 5): To send a PR interrupt to the SPARCstation, a VMEbus processor writes a "1" to bit 5 of the Remote Node Command Register 1. Writing a "0" does nothing. The SBus processor receiving the PR interrupt must clear the PR flip-flop to signal the interrupt was received.

8.2.3 Remote Node Status Register

The Remote Node Status Register is a read-only register located on the SBus Adaptor card.

BIT	FUNCTION
7	reserved
6	reserved
5	PR Interrupt Flip-Flop Set
4	reserved
3	reserved (always reads back as "1")
2	reserved
1	PT Interrupt Flip-Flop Set
0	reserved

PR INTERRUPT FLIP-FLOP SET (bit 5): Set to "1" when the PR interrupt flip-flop on the SBus Adaptor card is set.

PT INTERRUPT FLIP-FLOP SET (bit 1): Set to "1" when the PT interrupt flip-flop on the SBus Adaptor card is set.

8.2.4 Remote Node Page Registers

The Remote Node Page Registers are read/write registers located on the SBus Adaptor card. These registers can be accessed from the SBus or VMEbus processor (see also section 7.1.6). Access from the VMEbus is either byte-wide or word-wide. Access from the SBus is word-wide only.

BIT	FUNCTION	
7	SBus Address Bit 31	
6	SBus Address Bit 30	
5	SBus Address Bit 29	
4	SBus Address Bit 28	Address Page HIGH
3	SBus Address Bit 27	
2	SBus Address Bit 26	
1	SBus Address Bit 25	
0	SBus Address Bit 24	
7	SBus Address Bit 23	
6	SBus Address Bit 22	
5	SBus Address Bit 21	
4	SBus Address Bit 20	Address Page LOW
3	SBus Address Bit 19	
2	SBus Address Bit 18	
1	SBus Address Bit 17	
0	SBus Address Bit 16	

The Remote Node Page Registers are gated to the SBus address on VMEbus to SBus cycles. The two registers together provide the upper 16 address bits of a 32-bit SBus address.

8.2.5 Adaptor ID Register

A byte read of the Adaptor ID Register returns the hex value DF that identifies the card on the other end of the cable as a Model 467-1 SBus Adaptor card.

8.3 DMA Controller Registers

This section covers the DMA Controller Registers accessed from the VMEbus. Refer to section 1.7 for additional information about DMA. DMA Controller Registers accessed from the SBus are discussed in Chapter 7. The DMA Controller Registers are used when a VMEbus processor card initiates a DMA Controller operation to the SBus.

8.3.1 DMA Controller Registers Accessed From The VMEbus

The registers listed in the following table are located on the VMEbus Adaptor card and are addressed by processors on the VMEbus system.

VMEbus I/O ADDR (hex)	WRITE FUNCTION	READ FUNCTION
I/O LO + 10	VME DMA Command	VME DMA Command
I/O LO + 11	DMA Packet Remainder	DMA Packet Remainder
I/O LO + 12	DMA VME ADDR 24-31	DMA VME ADDR 24-31
I/O LO + 13	DMA VME ADDR 16-23	DMA VME ADDR 16-23
I/O LO + 14	DMA VME ADDR 8-15	DMA VME ADDR 8-15
I/O LO + 15	DMA VME ADDR 0-7	DMA VME ADDR 0-7
I/O LO + 16	DMA Packet Count 16-23	DMA Packet Count 16-23
I/O LO + 17	DMA Packet Count 8-15	DMA Packet Count 8-15

The registers listed in the table below are located on the SBus Adaptor card and are addressed by processors in the VMEbus system.

VMEbus I/O ADDR (hex)	WRITE FUNCTION	READ FUNCTION
I/O LO + 18	-- reserved --	-- reserved --
I/O LO + 19	DMA Packet Remainder	DMA Packet Remainder
I/O LO + 1A	DMA SBus ADDR 24-31	DMA SBus ADDR 24-31
I/O LO + 1B	DMA SBus ADDR 16-23	DMA SBus ADDR 16-23
I/O LO + 1C	DMA SBus ADDR 8-15	DMA SBus ADDR 8-15
I/O LO + 1D	DMA SBus ADDR 0-7	DMA SBus ADDR 0-7
I/O LO + 1E	-- reserved --	-- reserved --
I/O LO + 1F	-- reserved --	-- reserved --

8.3.2 DMA Controller VMEbus Command Register

The DMA Controller VMEbus Command Register is located on the VMEbus Adaptor card.

BIT	FUNCTION
7	Start DMA Controller
6	reserved - must be zero
5	DMA Transfer Direction
4	DMA Transfer Size Word/Longword Select
3	DMA Local Pause
2	Enable DMA Done Interrupt
1	DMA Done Flag
0	Block Mode DMA on the VMEbus Adaptor Card

START DMA CONTROLLER (bit 7): Writing "1" to bit 7 starts a DMA Controller operation. This bit should be set only after all other DMA registers are ready.

DMA may occur only between VMEbus and SBus memory; not between VMEbus memory and Dual Port RAM.

DMA TRANSFER DIRECTION (bit 5): Writing "1" to bit 5 causes the DMA Controller to transfer data from VMEbus RAM to SBus RAM. Writing "0" causes a data transfer from SBus RAM to VMEbus RAM.

DMA TRANSFER SIZE WORD/LONGWORD SELECT (bit 4): Writing "1" to bit 4 causes the DMA Controller to perform longword (32-bit) data transfers. This bit must always be set.

DMA LOCAL PAUSE (bit 3): Writing "1" to this bit causes the VMEbus Adaptor card DMA Controller to pause after 16 longwords have been transferred. This pause allows other VMEbus masters to receive a bus grant quickly during a DMA operation. There is always a pause between 256-byte segments (64 transfers).

ENABLE DMA DONE INTERRUPT (bit 2): Writing "1" to bit 2 enables the DMA DONE interrupt on the VMEbus Adaptor card at the completion of a DMA operation. Switching this bit permits software control (masking) of the DMA DONE interrupt.

DMA DONE FLAG (bit 1): Presents the status of a DMA operation to software in the same manner as the DMA DONE interrupt does for the hardware. It clears itself when a new DMA operation begins. Writing "0" to bit 1 also clears the DMA DONE status and stops any DMA transfer in progress.

BLOCK MODE DMA ON VMEbus ADAPTOR CARD (bit 0): Writing "1" to this bit allows the VMEbus Adaptor card DMA Controller to perform Block Mode operations in the VMEbus chassis.

8.3.3 DMA Controller VMEbus Address Registers

There are two DMA Controller VMEbus Address Registers: DMA VMEbus Address High and DMA VMEbus Address Low. Both are 16-bit read/write registers located on the VMEbus Adaptor card.

The DMA Controller VMEbus Address Registers are found at I/O locations 12 - 15 hex. The registers' four bytes are loaded (before starting the DMA) with the first address to be accessed on the VMEbus. Address Bias jumpers do not alter the value of this register; this is the physical VMEbus address. As the DMA operation progresses, the contents of the registers increment by four for longword operations. An I/O read of these registers during DMA produces the address count at that time in the DMA (the *next* address to be accessed).

The four I/O bytes that make up the DMA VMEbus address may be written to or read from in byte-wide or word-wide I/O operations. DMA VMEbus address bit 31 (written to bit 7 of I/O location 12) is the most significant bit of the address. DMA VMEbus address bit 0 (written to bit 0 of I/O location 15) is the least significant address bit.

The address must be longword-aligned; the lowest two bits of the VMEbus address must be "0".

8.3.4 DMA Controller Packet Count Registers

The DMA Controller Packet Count Registers, located on the VMEbus Adaptor card, are found at I/O locations 16 - 17 hex.

Before starting the DMA, the registers are loaded with the number of packets (one packet equals 256-bytes) to be transferred by Adaptor DMA. As the DMA Controller operation progresses, the contents of the registers decrement for every data packet transferred. A VMEbus I/O read of the local node registers during DMA produces the number of packets remaining to be transferred at that time (within 256 bytes).

The bits in the registers are numbered as though they were a 24-bit register. However, you can access only the most significant 16 bits (bits 08 - 23).

The two bytes that make up the DMA Packet Counter may be written to or read from in byte-wide or word-wide I/O operations. DMA Packet Counter bit 23 (written to bit 7 of I/O location 16) is the most significant bit of the counter.

The DMA Controller Packet Count Register bits 8 - 23, also, may be viewed as the number of 256-byte packets of data to be transferred.

8.3.5 DMA Controller Packet Remainder Register

The DMA Controller Packet Remainder Register is an 8-bit read/write register located on the VMEbus Adaptor card.

Before starting DMA, the DMA Controller Packet Remainder Register is loaded with the lowest eight bits of the number of bytes to be transferred by the DMA. The values in the register must be multiples of 4 bytes.

The same value must also be written to the DMA Controller Packet Remainder Register on the SBus Adaptor card. See also section 8.3.6.

8.3.6 DMA Controller SBus Packet Remainder Register

The DMA Controller SBus Packet Remainder Register is a byte-addressable register located on the SBus Adaptor card. See also section 8.3.5.

8.3.7 DMA Controller SBus Address Registers

The DMA Controller SBus Address Registers are located on the SBus Adaptor card.

The DMA Controller SBus Address Registers are loaded from the VMEbus (before starting the DMA) with the first address to be accessed on the SBus. As the DMA operation progresses, the contents of the registers increment by four in each cycle.

The two I/O words that make up the DMA Controller SBus address are word-addressable. DMA Controller SBus address bit 31 (written to bit 7 of I/O location 1A) is the most significant bit of the address. DMA Controller SBus address bit 0 (written to bit 0 of I/O location 1D) is the least significant address bit.

The address must be longword-aligned; the lowest two bits of the SBus address must be "0".

➔ A VMEbus processor should never attempt to read or write SBus I/O registers or SBus RAM during a DMA Controller operation.

Chapter 9: Additional Programming Notes

9.0 Setup Sequence

If your application uses the Adaptor card CSR, you must execute a simple setup procedure to initialize the card. The following is a program sequence for initialization:

1. I/O READ from the Local Node Status Register to test if the remote chassis has power on.

2. I/O READ from the Remote Node Status Register to flush interface errors caused by the power-on transition.

3. I/O WRITE with data **80** (hex) to the Local Node Command Register to clear status register power-on errors.

4. I/O READ from the Local Node Status Register to see that no interface errors occurred and that the preceding steps were successful.

9.1 DMA Setup Sequence

The sequences in sections 9.1.1 and 9.1.2 are samples of program steps to arm the Adaptor DMA Controllers for DMA operations.

9.1.1 Initiated By The SBus

1. Write to the Remote Node Command Register 1 to disable the **Use Address Page Register** bit.

2. Load the SBus DMA Address Counter with the first SBus DMA address to be accessed.

3. Load the VMEbus DMA Address Counter with the first VMEbus DMA address to be accessed *and* the Address Modifier Register with the appropriate address modifier.

4. Load the SBus DMA Packet Counter with the number of packets (one packet equals 256-bytes) to be transferred.

5. Load Remote Node Command Register 2 on the VMEbus Adaptor card with the correct selections for remote Block Mode/Non-Block Mode and VMEbus pause. In the same register, disable remote interrupts.

6. Write the lowest eight bits of the number of bytes to be transferred to the SBus and VMEbus DMA Packet Remainder Registers.

7. Load the SBus DMA Controller Command Register with the correct selections for Dual Port/remote RAM transfer, transfer direction, and word/longword transfer.

8. Enable the **DMA DONE** interrupt (if desired) and the **DMA Start** bit.

After the DMA operation finishes:

1. Write a "0" to the **DMA DONE** bit (in the SBus DMA Command Register) to clear the **DMA DONE** interrupt.

2. Write Remote Node Command Register 2 to re-enable interrupts from the VMEbus to the SBus.

3. Write to Remote Node Command Register 1 to re-enable the **Use Address Page Register** bit, if desired.

4. Write to the Address Page Low Register.

5. Write to the Address Page High Register.

After the steps above are completed, any pending interrupts are passed through the Adaptor.

9.1.2 Initiated By The VMEbus

1. Load the VMEbus DMA Address Counter with the first VMEbus DMA address to be accessed *and* the Address Modifier Register with the appropriate address modifier.

2. Load the SBus DMA Address Counter with the first SBus DMA address to be accessed.

3. Write the lowest eight bits of the number of bits to be transferred to the VMEbus and SBus DMA Packet Remainder Registers.

4. Load the VMEbus DMA Packet Counter with the number of packets (one packet equals 256-bytes) to be transferred.

5. Write a "1" to bit 2 of the VMEbus Local Node Command Register to prevent VMEbus interrupts from passing to the SBus.

6. Load the DMA Controller Command Register with the correct selections for Dual Port/remote RAM transfer, transfer direction, word/longword transfer, local bus pause, and local Block Mode/Non-Block Mode transfers.

7. Enable the **DMA DONE** interrupt (if desired) and the **DMA Start** bit.

After the DMA operation completes:

1. Write a "0" to the **DMA DONE** bit (in the DMA Controller Command Register) to clear the **DMA DONE** interrupt.

2. Write a "0" to bit 2 of the Local Node Command Register to re-enable interrupts through the VMEbus Adaptor card to the SBus.

9.1.3 Slave Mode DMA Set Up Sequence

1. Allocate SBus memory space to receive the DMA data, and set the page size and page value registers on the SBus Adaptor card accordingly.

2. Initialize the DMA Controller device on the VMEbus. Make sure the VMEbus address presented by the DMA Controller device is within the VMEbus Adaptor card's REM RAM HI and REM RAM LO settings.

Chapter 10: Utilities Diskette

10.0 Introduction

Chapter 10 describes the files contained on the Utilities Diskette, how to use each file, and how the programs work.

10.1 Theory Of Operation

The UNIX® operating system uses virtual memory addressing; therefore, before an application can access the Adaptor, a section of virtual address space must be mapped to a fixed physical address. The mmap() device driver routine is used to accomplish the mapping. Parameters for the mmap() device driver call are described in Appendix D of the *Writing Device Drivers* publication available from Sun Microsystems.

For the SPARCstation, Sun provides four device drivers (/dev/sbus0, /dev/sbus1, /dev/sbus2, and /dev/sbus3), one for each of the four SBus slots available. Each device driver supports the mmap() call, and will map to a given address on that slot. For example, the /dev/sbus1 device driver only maps to addresses of the SBus card in slot one.

Solaris 2.x does not predefine /dev/sbus<n> where <n> is the slot number.

To define /dev/sbus1 on a sun4c machine, login as **root** and enter the following command:

```
# ln -s /devices/sbus*/sbusmem@1*:slot1 /dev/sbus1
```

To define /dev/sbus1 on a sun4m machine, login as **root** and enter the following command:

```
# ln -s /devices/iommu*/sbus*/sbusmem@1*:slot1 /dev/sbus1
```

To define other slots, in one of the two commands above simply replace each 1 with the desired slot number.

The device drivers provided are sufficient for accessing Adaptor registers, remote I/O, remote memory, and/or Dual Port RAM. They do not, however, allow the receipt of interrupts. A specific device driver for the Bit 3 SBus Adaptor card is required to receive interrupts. Optional Models 943 and 944 Support Software include a device driver that can be customized for your specific system. Contact Bit 3 for more information about optional Support Software.

All example programs provided on the Utilities Diskette use the /dev/sbus[0-3] device drivers.

When calling the mmap() routine, parameters for the offset in the device and size of the memory area to map must be provided. For /dev/sbus[0-3] devices, the offset is the SBus address of the device. Address zero will always be the configuration ROM; other addresses are documented in Chapter 6.

Appendix A of the SBus specification includes a recommendation that not more than 1M byte of memory be mapped because mapping more memory may degrade system performance. This 1M byte limit refers to the maximum amount that can be transferred via a DMA operation. By using the mmap() interface all 32M bytes of slot space on the SBus can be mapped without affecting system performance.

10.2 Installing The Software

➔ All files on the Utilities diskette are also provided with Model 943 and Model 944 SBus Support Software. You do not need to install the Utilities diskette if you installed Model 943 or 944 Support Software.

➔ The Utilities files are stored on a 3.5" HD diskette in **TAR** format.

1. Create a directory for the files and make it your default directory. For example:

   ```
   # cd /usr/local
   # mkdir 805
   # cd Bit3
   ```

2. Insert the diskette in the drive.

3. Type the following command:

   ```
   # tar xovf /dev/rfd0
   ```

   The following files should be extracted:

FILE	DESCRIPTION
84903810.fth	The Forth source code for the FCode PROM of the Bit 3 SBus Adaptor card
bts.h	An include file that defines many of the constants needed and a structure for accessing the Adaptor registers
dumpport.c	A simple program that dumps the first few characters contained in the Dual Port RAM section
dumpram.c	A program that uses the Page Mode feature of the Adaptor to dump a specific address on the remote bus

The default protection on the /dev/sbus[0-3] device drivers requires root privileges. To have a normal application open and use these drivers, log into the supervisor account and change the protection. For example, to allow anyone to use the device driver for an Adaptor card located in slot 1, enter the following commands:

```
# cd /dev
# chmod a+rw sbus1
```

10.3 Files Provided

Each file contained on the Utilities Diskette is discussed individually in the following sections.

10.3.1 84903810.fth

84903810.fth is the Forth source code for the configuration PROM on the Bit 3 Adaptor card. All SBus cards have a configuration PROM that defines the characteristics of the card and, possibly, contains a device driver. The Bit 3 Adaptor card is not a boot device; consequently, it only requires configuration information.

Most likely, this source code will never require modification. If, however, you need to reprogram the PROM with your own FCode, part of the space in the PROM is used to initialize the chips on the Adaptor card. This information is never visible to the SBus. If you require a custom PROM for your card, please contact Bit 3.

10.3.2 bts.h

The bts.h include file contains the offsets from the beginning of SBus address space into each section used on the card. It also contains a structure suitable for accessing the device registers on the Model 467-1 Adaptor. Both the dumpport.c and dumpram.c programs use this include file.

10.3.3 dumpport.c

The dumpport.c program reads and displays, in hexadecimal format, the first few characters contained in Dual Port RAM.

Assuming the SBus Adaptor card is located in slot one, the following commands compile and execute the program:

```
# cc -02 -0 dumpport  dumpport.c
# dumpport 1
```

The parameter 1 in the dumpport command indicates the slot in which the SBus Adaptor card is installed. The program checks only that this number is in the valid range. No attempt is made to verify that the Adaptor card is actually the device in that slot. If no slot number is specified, the program will assume the number DEFAULT_SLOT.

When compiling modules using the SBus Adaptor card, the optimization level on the compiler is set at two (-02). Higher levels of optimizations allow the compiler to optimize out some accesses to the SBus Adaptor card, causing side effects. Currently, there is no way to tell the C compiler not to optimize accesses to the device.

First, the program opens the /dev/sbus[0-3] device driver and maps the Adaptor Node registers. This program directly accesses the Node I/O registers through a pointer to a structure. This method works well, however, in your own programs you may want to hide the access to the Node I/O registers inside functions or #define macros. By hiding the access in this way, if you change your design so that register access is controlled from one program or special device driver, program conversion will be easier.

After checking the local status register, the program proceeds to dump the beginning of the Dual Port RAM area in hexadecimal and ASCII. It then checks the status register for errors, and returns to the command shell.

10.3.4 dumpram.c

The dumpram.c program is similar to the dumpport.c program except that it uses Page Mode access and accesses remote memory rather than Dual Port RAM. Assuming the Adaptor card is located in slot 1, the following commands compile and execute the program:

```
# cc -02 -0 dumpram dumpram.c
# dumpram 1
```

The program prompts for the beginning address and sets the page register based on this address. It then dumps the memory, using a method identical to that used by the dumpport program.

Use the setup( ) routine as a starting point for initializing the Adaptor. Note that the procedure does a remote node register read before clearing the error status register. It then performs additional remote node I/O before checking the status register and indicating that the Adaptor is ready to be used. The first remote access is suggested to flush any incomplete transactions on the cable; this data should always be ignored. Later transactions perform a simple test to ensure the basic interface is functional. In a functional system, a remote node I/O can always complete without errors.

All other comments made about the dumpport program apply to the dumpram program.

Appendix A: Glossary

The following terms are used throughout this manual:

"0": Zero.

"1": One.

Adaptor Node Input/Output: Any access to the I/O registers contained on either the local or remote Adaptor card. These are referred to as local node I/O and remote node I/O, respectively.

Bit: A single digit in a binary number (0 or 1).

Byte: 8 bits.

CSR: Adaptor Control and Status Registers.

Direct Memory Access Transfers (DMA): The Adaptor may be programmed to transfer large blocks of data across the cable to or from the remote chassis, rather than requiring a processor to move data.

Dual Port RAM: An optional dual-port memory card installed on the VMEbus Adaptor card.

Exchanging Interrupts: Sending interrupts to and receiving interrupts from the remote chassis. This would also include any processing an application should do to acknowledge the receipt of an interrupt.

FIFO: First In First Out. A memory device in which data are retrieved in the same sequence as stored.

G byte: Gigabyte. Two to the thirtieth power (exactly 1,073,741,824 bytes).

Geographic Addressing: A mechanism by which a part of the physical address is presented to each SBus slave as an individual select signal, so that at any given time only one slave is selected.

Hex: Hexadecimal notation. A numbering system that uses 16 digits (0123456789ABCDEF) to denote a number.

K byte: Kilobyte. Two to the tenth power (exactly 1024) bytes.

Local: Pertaining to the system accessing either Adaptor card. Implies that it is not necessary to go across the interface cable to access the resource.

Longword: 32 bits; in the SBus specification, 32-bit data are called words.

M byte: Megabyte. Two to the twentieth power (exactly 1,048,576) bytes.

M Bytes/sec: Megabytes per second. Exactly 1,048,576 bytes per second.

msec: Millisecond. 1/1,000 of a second.

nsec: Nanosecond. 1/1,000,000,000 of a second.

Physical Address: The actual or machine address of an item or device.

PIO: Programmed I/O.

Programmed Interrupts: Interrupts caused by setting a flip-flop in one of the Adaptor node I/O registers. The two types of programmed interrupts are the PT (Programmed to Transmitter) interrupt and the PR (Programmed to Receiver) interrupt.

Receiver: An Adaptor card that is not allowed to transmit messages across the interface cable, thus preventing it from accessing the remote node I/O, remote bus I/O and memory, or a remotely-installed Dual Port RAM card.

Remote: Pertaining to the system accessing either Adaptor card. Implies that the resource is located at the other end of the Adaptor interface cable.

Remote Bus Input/Output: Any access to the I/O registers of devices which are physically located in the remote system chassis (not the remote Adaptor card).

Remote Bus Memory: Any access to the memory space in the remote chassis. This may be a shared memory section, a device buffer, or any device that responds to a memory access. This does not include Dual Port RAM located on the remote Adaptor card.

Transmitter: An Adaptor card that is allowed to transmit messages across the interface cable. There must always be at least one transmitter in any pair of Adaptor cards.

µsec: Microsecond. 1/1,000,000 of a second.

Virtual Address: An address that references a location in a virtual address space.

Virtual Address Space: A contiguous range of virtual memory locations.

Virtual Memory: A facility whereby the effective range of addressable memory locations provided to a process is independent of the size of main memory. This means that the virtual address space of a process is independent of the physical address space of the CPU.

Window: A range of addresses that the Adaptor responds to for a specific function; a reserved area of main memory.

Word: 16 bits; in the SBus specification, 16-bit data are called halfwords.

Appendix B: VMEbus Addressing

The VMEbus specification defines three types of address spaces: extended (A32), standard (A24) and short (A16). Extended (A32) addressing uses 32 address bits. Standard (A24) addressing uses 24 address bits. Short (A16) addressing uses 16 address bits. The VMEbus does not have an address 0 (A0) line. Byte addressing is controlled by the signals DS0 and DS1.

Each address space is independent of the other address spaces and can be thought of as a logically separate address bus. A32 addressing uses address lines A31-01. A24 uses A23-01, and A31-24 are unused. A16 uses A15-A01, and A31-16 are unused. Address lines A03-A01 are used during Interrupt Acknowledge cycles (IACK cycles). The following table summarizes the use of the address bus.

ACTIVE PORTION OF ADDRESS BUS - ADDRESS ROUTING				
A31 - A24	A23 - A16	A15 - A04	A03 - A01	Address Modifier Codes (hex)
A31 ----------A01				Extended (32-bit) 08 - 0F
▨	A23----------A01			Standard (24-bit) 38 - 3F
▨	▨	A15----------A01		Short I/O (16-bit) 29, 2D
▨	▨	▨	A03 - A01	Interrupt Acknowledge

▨ = Unused portion of address bus; should be ignored by slave device.

The value of the address modifier lines, AM[0..5], determines which address space is used. The VMEbus master is responsible for supplying the proper address modifier at the same time it drives the address lines. Slaves are designed to respond to cycles with a particular address modifier; however, some slaves are capable of responding to several address modifiers.

The address modifier generated when the SBus accesses the VMEbus is determined by the value in the Remote Address Modifier register. The programmer should determine which address modifier the target slave responds to, then write that value to the Remote Address Modifier register. Any subsequent memory references to the VMEbus will use this address modifier. IACK cycles do not use the address modifier lines. The following table summarizes address modifier codes.

ADDRESS MODIFIER (HEX)	# OF ADDRESS BITS	TRANSFER TYPE
3F	24	Standard supervisory block transfer
3E	24	Standard supervisory program access
3D	24	Standard supervisory data access
3B	24	Standard non-privileged block transfer
3A	24	Standard non-privileged program access
39	24	Standard non-privileged data access
2D	16	Short supervisory access
29	16	Short non-privileged access
10 - 1F	undefined	User defined
0F	32	Extended supervisory block transfer
0E	32	Extended supervisory program access
0D	32	Extended supervisory data access
0B	32	Extended non-privileged block transfer
0A	32	Extended non-privileged program access
09	32	Extended non-privileged data access
don't care state	3	Interrupt acknowledge cycle (uses A01-A03)

The following tables of VMEbus pin assignments are provided for reference.

P1/J1			
Pin #	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 VDC	+5VSTDBY	+12 VDC
32	+5 VDC	+5 VDC	+5 VDC

* = active low

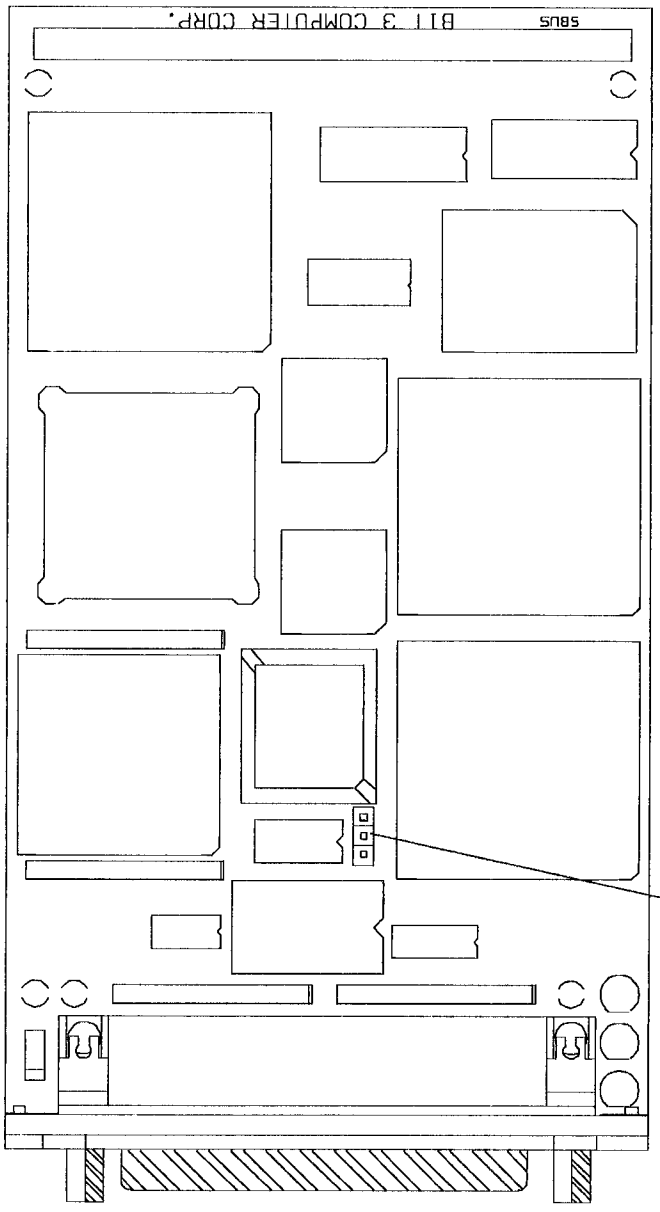
P2/J2			
Pin #	Row A	Row B	Row C
1	User Defined	+5 VDC	User Defined
2	User Defined	GND	User Defined
3	User Defined	RESERVED	User Defined
4	User Defined	A24	User Defined
5	User Defined	A25	User Defined
6	User Defined	A26	User Defined
7	User Defined	A27	User Defined
8	User Defined	A28	User Defined
9	User Defined	A29	User Defined
10	User Defined	A30	User Defined
11	User Defined	A31	User Defined
12	User Defined	GND	User Defined
13	User Defined	+5 VDC	User Defined
14	User Defined	D16	User Defined
15	User Defined	D17	User Defined
16	User Defined	D18	User Defined
17	User Defined	D19	User Defined
18	User Defined	D20	User Defined
19	User Defined	D21	User Defined
20	User Defined	D22	User Defined
21	User Defined	D23	User Defined
22	User Defined	GND	User Defined
23	User Defined	D24	User Defined
24	User Defined	D25	User Defined
25	User Defined	D26	User Defined
26	User Defined	D27	User Defined
27	User Defined	D28	User Defined
28	User Defined	D29	User Defined
29	User Defined	D30	User Defined
30	User Defined	D31	User Defined
31	User Defined	GND	User Defined
32	User Defined	+5 VDC	User Defined

Appendix C: Jumper Configuration Worksheets

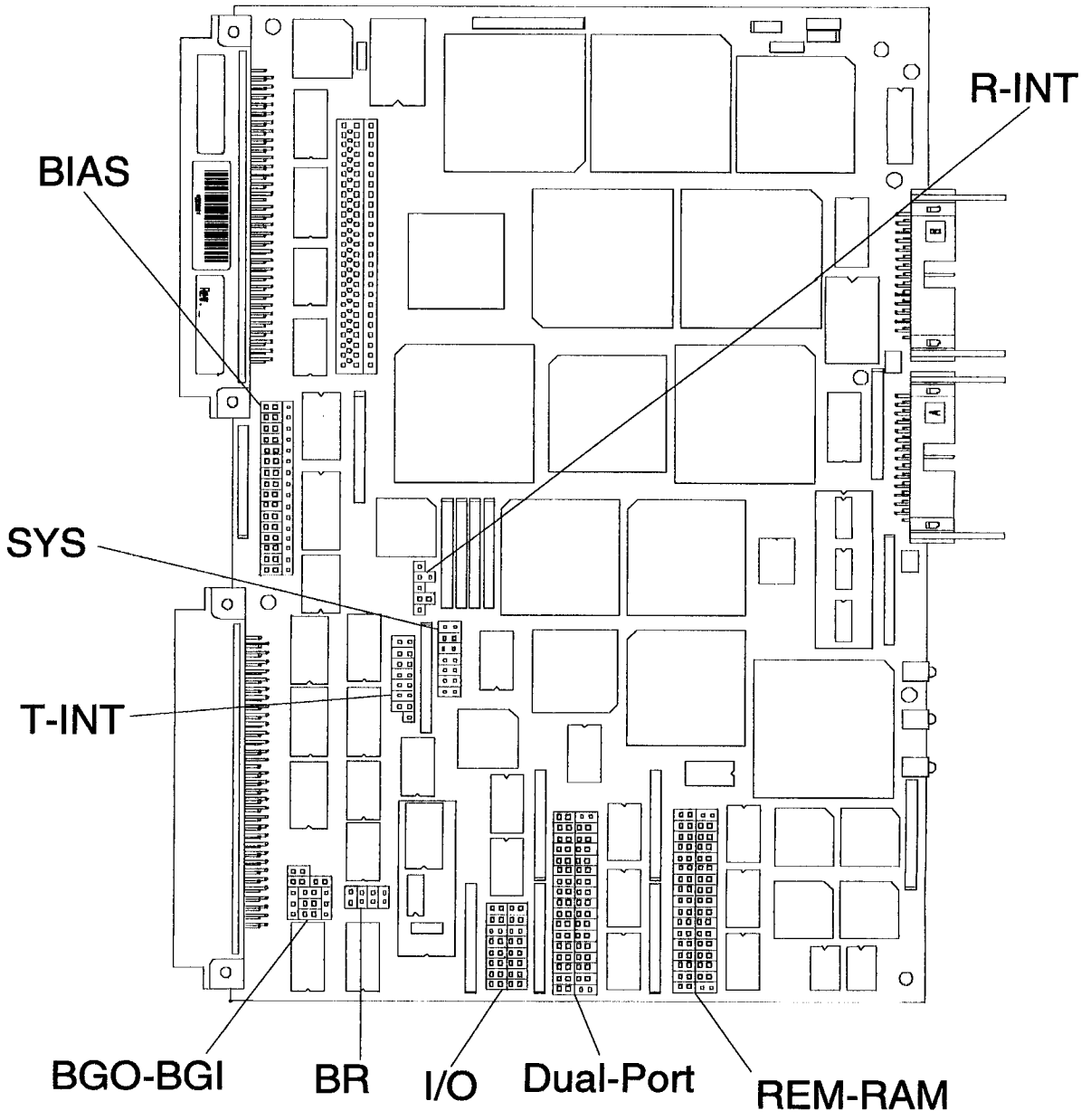
Use the following worksheets to document how you have set the jumpers on your Model 467-1 Adaptor cards.

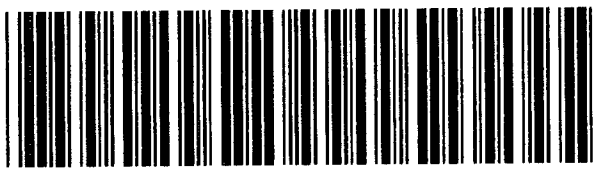
Please have the completed worksheets available when calling Bit 3 for technical support.

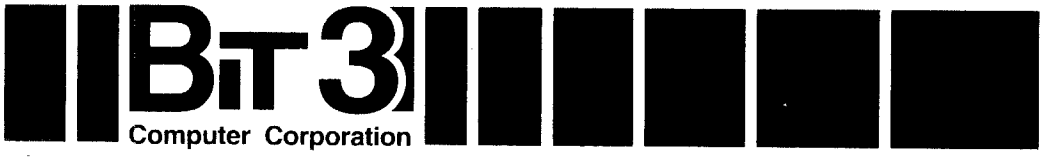
C.1 SBus Adaptor Card Worksheet



C.2 VMEbus Adaptor Card Worksheet







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